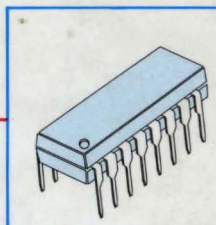
SAMSUNG

Data Book

Linear IC

VOL. 2, 1989



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LINEAR IC DATA BOOK

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LM339/A	Quad Differential Comparator	14 DIP/14 SOP	557
LM348	Qual Operational Amplifier	14 DIP/14 SOP	509
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LM3302	Quad Differential Comparator	14 DIP/14 SOP	557
MC1458/C/I	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	529
MC3303	Quad Operational Amplifier	14 DIP/14 SOP	533
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MC4558/C/A/I	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	540
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**KAD0206	6 Bit A/D Converter (20 MSPS)	32SOIC/30 SDIP	Vol. 3
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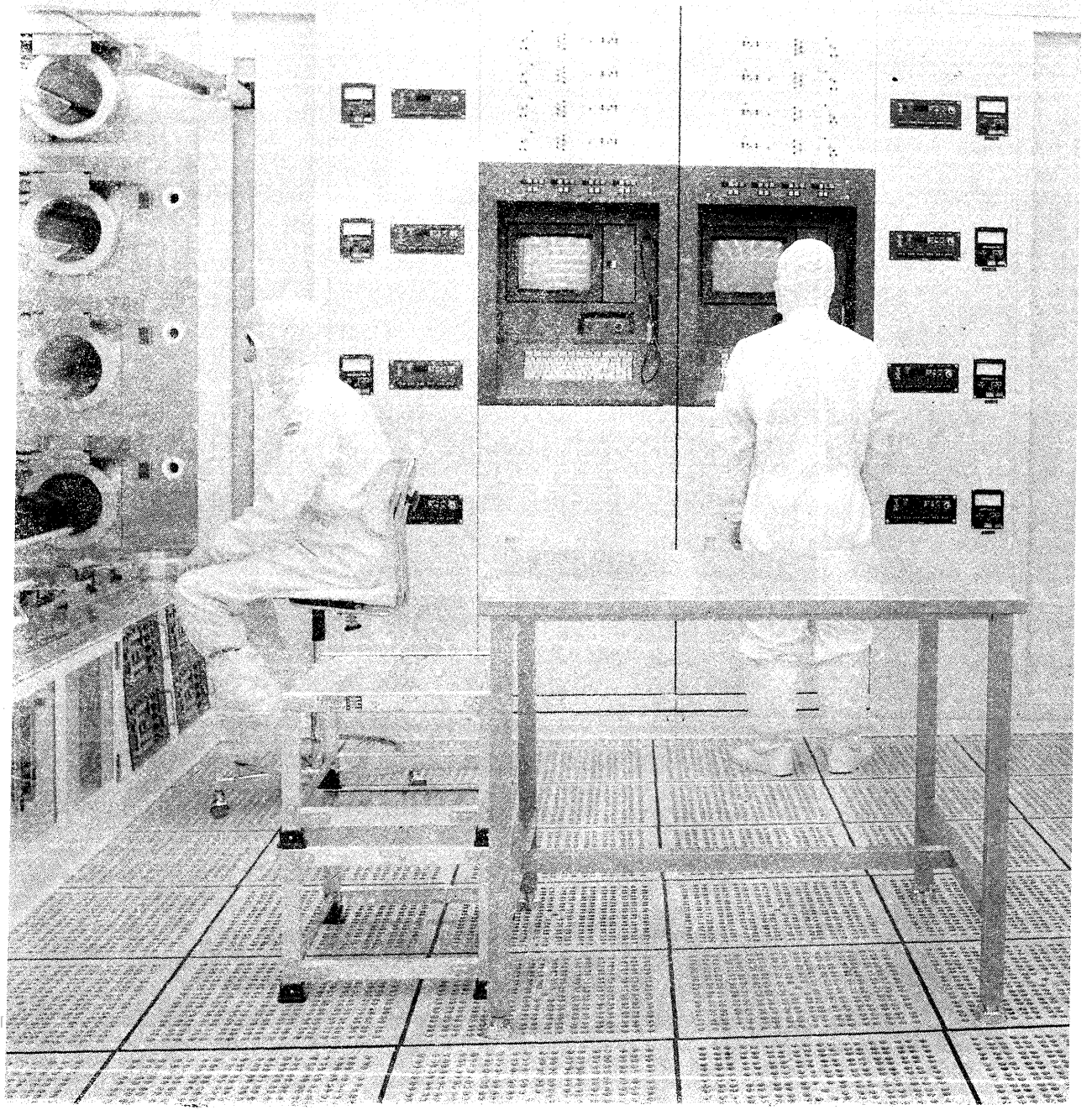
*KAD0817	8 Bit up-Compatible A/D Converter (16 CH)	40 DIP	Vol. 3
KAD0820	8 Bit up-Compatible A/D Converter	20 DIP	Vol. 3
KS7126	3 1/2 Digit A/D Converter	40 DIP	Vol. 3
**KDA0406	Tripple 6 Bit D/A Converter (20 MSPS)	28SOIC/28 SDIP	Vol. 3
*KDA3310	10 Bit D/A Converter	28 CERDIP	Vol. 3
KDA0800/08	8 Bit D/A Converter	16 DIP	Vol. 3
KS25C02	8 Bit CMOS Successive Approximation Register	16 DIP	Vol. 3
KS25C03	8 Bit CMOS Successive Approximation Register	16 DIP	Vol. 3
KS25C04	12 Bit CMOS Successive Approximation Register	16 DIP	Vol. 3

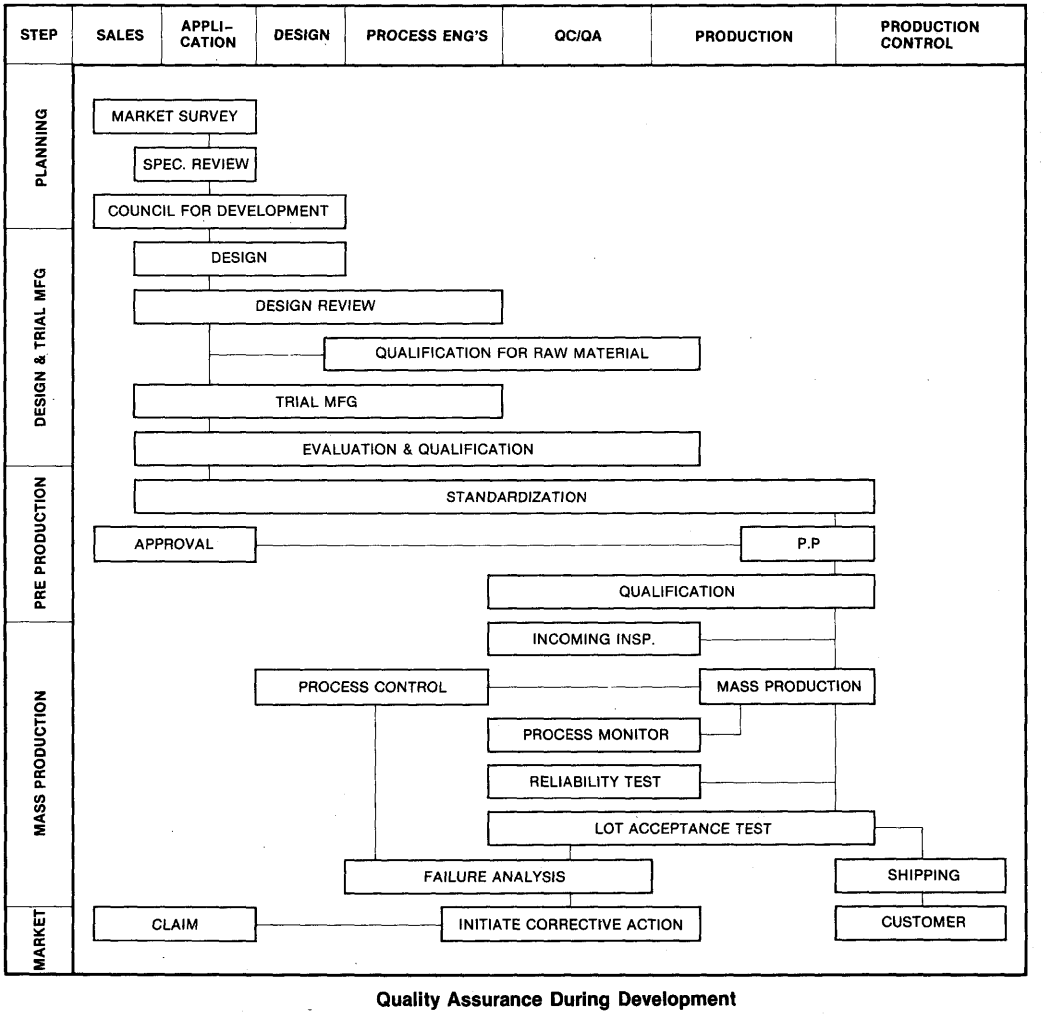
*: New Product
**: Under Development

QUALITY & RELIABILITY 1



INTRODUCTION

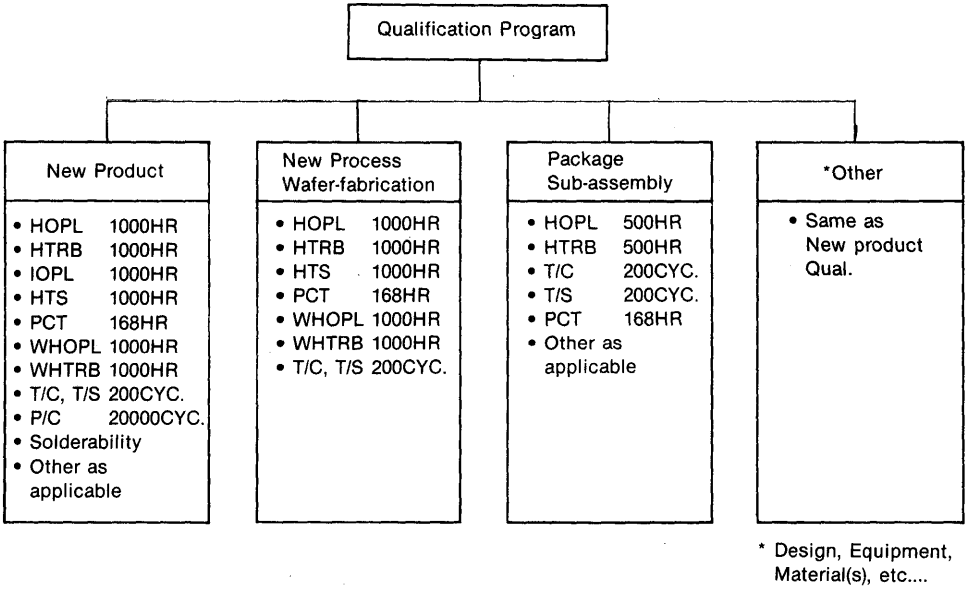
Samsung's linear IC products are among the most reliable in the industry. Samsung has always made a commitment to achieve the highest possible quality, reliability, and customer satisfaction with its products.
Extensive qualification, monitor and outgoing programs are used to scrutinize product quality and reliability. Stringent controls are applied to every wafer fabrication and assembly lot to achieve reproducibility, and therefore maintain product reliability.
In this chapter, the quality and reliability programs established at Samsung will be discussed. In addition, a description of reliability theory, reliability tests and various support efforts provides a broad framework from which to comprehend Samsung quality and reliability.
To better understand the Quality Department's role in product develoment and manufacturing, a detailed diagram is listed below. As can be noted, Quality Engineering is involved in all phases, save that of initial product planning.



Quality Assurance During Development

QUALIFICATION

Procedures to qualify devices are listed below. There are both general and product-specific requirements. Procedures are detailed for new products, die-only qualifications, and package-only qualifications. The latter two are for products and/or packages already qualified, but where there is room for further product optimization.



Qualification Programs.

A) New Product Qualification Test Items

No.	Test Item	Test Condition	Part		Sample Size	LTPD	ACC. No	Reference Method	Note
			L-IC	Discrete					
1	High Temperature Reverse Bias (HTRB)	$Ta = T_j(max)$ $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES	45	10	1		48HR for PRT
2	High Temperature Operating Life (HOPL)	$Ta = T_{opr}(max)$ $V_{CC} = V_{CC}$ (max) Static, Dynamic 1000HRS	YES	—	45	10	1	MIL-STD-883 1005	48HR for PRT
3	High Temperature Storage (HTS)	$Ta = T_j(max)$ 1000HRS	YES	YES	45	10	1		
4	Operating Life (OPL)	$Ta = 25°C$ $Pc = Pc(max)$ 1000HRS	—	YES	45	10	1	MIL-STD-750 1026.3	for Small-Signal Device
5	Intermittent OPL (IOPL)	$Ta = 25°C$ $Pc = Pc(max)$ 2min/2min On/Off 1000HRS	—	YES	45	10	1	MIL-STD-750 1036.3	
6	Power Cycle (P/C)	$\triangle T_j = 125°C$ 45Sec/90Sec On/Off 20000CYC.	YES	YES	45	10	1		For PWR TR, PWR IC
7	Pressure Cooker Test (PCT)	$Ta = 121°C \pm 2°C$ RH = 100% 15PSIG 168HRS	YES	YES	45	10	1		48HR for PRT
8	Wet High Temperature Reverse Bias (WHTRB)	$Ta = 85°C$, RH = 85% $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES	45	10	1		
9	Wet High Temperature Operating Life (WHOPL)	$Ta = 85°C$, RH = 85% $V_{CC} = V_{CC}(opr)$, P_{dmin} 1000HRS	YES	—	45	10	1		
10	Thermal Shock (T/S)	$-65°C \rightarrow 150°C$ (Liquid) 5min < 10Sec, 5min 200 Cycles	YES	YES	45	10	1	MIL-STD-883 1011	
11	Temperature Cycle (T/C)	$-65°C \rightarrow 25°C \rightarrow 150°C$ 10min, 5min, 10min 200 Cycles	YES	YES	45	10	1	MIL-STD-883 1011	

A) New Products Qualification Test Item (Continued)

No.	Test Item	Test Condition	Part		Sample Size	LTPD	ACC. No	Reference Method	Note
			L-IC	Discrete					
12	Solder Heat Resistance (S/H)	Ta = 260°C ± 5°C t = 10 ± 0.5sec	YES	YES	10	N/A	0	MIL-STD-750 2031	
13	Solderability	Ta = 245°C ± 5°C t = 10 ± 1SEc	YES	YES	10	N/A	0	MIL-STD-883 2003	
14	Salt Atmosphere	Ta = 35°C, 5% NaCl 24HRS	YES	YES	10	N/A	0	MIL-STD-883 1009A	
15	Mechanical Shock	1500G, 0.5ms 3 Times each direction of X, Y and Z Axis	YES	YES	10	N/A	0	MIL-STD-750 2016	For Hermetic
16	Vibration	20G, 3Axis f = 20 to 2000 cps for 4min, 4 cycles	YES	YES	10	N/A	0	MIL-STD-883 2007	For Hermetic
17	Constant Acceleration	2000G X, Y, Z Axis 1min for each Axis	YES	YES	10	N/A	0	MIL-STD-883 2001	For Hermetic
18	ESD (Human Body (Model)	R = 1.5KΩ C = 100pF 5 Discharge V ≥ ± 1000V	YES	YES	5	N/A	0	MIL-STD-883 3015	
19	Latch-up Test		YES	—	5	N/A	0	—	For CMOS
20	Fine Leak Gross Leak	Helium Fluoro carbon	YES	YES	45	10	1	MIL-STD-883 1014	For Hermetic

Note) • N/A: Not available
• SOT-23, TO-92S PKG: PCT 48HR
• PRT: Process Reliability Test (all outgoing Lots)

B) New Process, Wafer Fabrication Qualification

No	Test Item	Test Condition	Package		Sample Size	LTPD	ACC No
			L-IC	Discrete			
1	High Temperature Operating Life (HOPL)	$Ta = T_{opr}(max)$ $V_{CC} = V_{CC}(max)$ STATIC, DYNAMIC 1000HRS	YES	—	45	10	1
2	High Temperature Reverse Bias (HTRB)	$Ta = T_j(max)$ $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES	45	10	1
3	High Temperature Storage (HTS)	$Ta = T_j(max)$ 1000HRS	YES	YES	45	10	1
4	Pressure Cooker Test (PCT)	$Ta = 121°C \pm 2°C$ RH = 100% 15 PSIG 168HRS	YES	YES	45	10	1
5	Wet High Temperature Operating Life (WHOPL)	$Ta = 85°C$, RH = 85% $V_{CC} = V_{CC(opr)}$ 1000HRS	YES	—	45	10	1
6	Wet High Temperature Reverse Bias (WHTRB)	$Ta = 85°C$, RH = 85% $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES	45	10	1
7	Thermal Shock (T/S)	$-65°C \rightarrow 150°C$(Liquid) 5min < 10sec, 5min 200 Cycles	YES	YES	45	10	1
8	Temperature Cycle (T/C)	$-65°C \rightarrow 25°C \rightarrow 150°C$ 10min, 5min, 10min 200 Cycles	YES	YES	45	10	1

C) Package Sub-Assembly Qualification

No	Test Item	Test Condition	Package		Sample Size	LTPD	ACC No	Notes
			Plastic	Hermetic				
1	High Temperature Reverse Bias (HTRB)	$Ta = T_j(max)$ $V_{CB} = V_{CBO} \times 0.8$ 500HRS	YES	YES	45	10	1	For Discrete
2	High Temperature Operating Life (HOPL)	$Ta = Topr(max)$ $V_{CC} = V_{CC}(max)$ Static, Dynamic 500HRS	YES	YES	45	10	1	For L-IC
3	Temperature Cycle (T/C)	$-65°C \rightarrow 25°C \rightarrow 150°C$ 10min, 5min, 10min 200 Cycles	YES	YES	45	10	1	
4	Pressure Cooker Test (PCT)	$Ta = 121°C \pm 2°C$ RH = 100%, 15PSIG 168HRS	YES	—	45	10	1	
5	Thermal Shock (T/S)	$-65°C \rightarrow 150°C$ (Liquid) 5min < 10sec, 5min 200 Cycles	YES	YES	45	10	1	
6	Solder Heat Resistance (S/H)	$260°C \pm 5°C$ 10 ± 1 sec	YES	YES	10	N/A	0	
7	Vibration (Variable-Frequency)	100 – 200 – 100Hz 20G, 5min, 5Times, X, Y, Z	—	YES	10	N/A	0	For Discrete, others as applicable
8	Mechanical Shock (M/S)	1500G, 0.5ms 3 Times, X, Y, Z	—	YES	10	N/A	0	same as above
9	Constant Acceleration	20000G X, Y, Z Axis 1 min for each Axis	—	YES	10	N/A	0	same as above

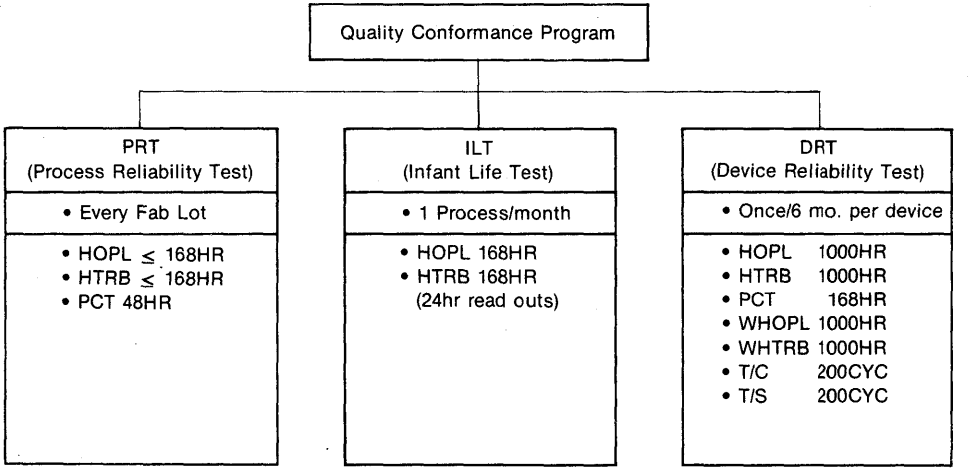
Note) • N/A: not available

Product Reliability (Quality Conformance) Monitors

Samsung implements periodic testing to monitor the ongoing reliability of its products. A subset of stresses used for qualification are run; they are seen as most critical for basic device reliability. Formally this is known as the Device Reliability Test System, or simply as DRT.

Lot-by-lot infant mortality reliability testing is also accomplished at Samsung. The purpose of this is to verify process integrity in a full QA step. Formally this is known as Process Reliability Testing, or more simply as PRT. Normally a short term accelerated lifetest and package reliability test are done, although exceptions are made in the case of special devices.

Although Samsung scrupulously utilizes statistical controls throughout it's production process, DRT and PRT serve as confirmation that indeed the customer does receive only high-grade units. The tables on the following give details of DRT and PRT processing.



Note: Test descriptions given on following pages.

Quality Conformance Program

DESCRIPTION

Samsung has established a comprehensive reliability program to monitor and ensure the ongoing reliability of the linear IC family. This program involves not only reliability data collection and analysis on existing parts, but also rigorous in-line quality controls for all products.

Listed below are details of tests performed to ensure that manufactured product continues to meet Samsung's stringent quality standards. In line quality controls are reviewed extensively in later sections.

The tests run by the quality department are accelerated tests, serving to model "real world" applications through boosted temperature, voltage, and/or humidities. Accelerated conditions are used to derive device knowledge through means quicker than that of typical application situtations. These accelerated conditions are then used to assess differing failure rate mechanisms that correlate directly with ambient conditions. Following are summaries of various stresses (and their conditions) run by Samsung on linear IC products.

HIGH TEMPERATURE OPERATING LIFE TEST (HOPL)

(T_j = 125°C, V_{CC} = V_{CC} max, static)

High temperature operating life test is performed to measure actual field reliability. Life tests of 1000HR to 2000HR durations are used to accelerate failure mechanisms by operating the device at an elevated ambient temperature (125°C). Data obtained from this test are used to predict product infant mortality, early life, and random failure rates. Data are translated to standard operating temperatures via failure analysis to determine the activation energy of each of the observed failures, using the Arrhenius relationship as previously discussed.

WET HIGH TEMPERATURE OPERATING LIFE TEST (WHOPL)

(Ta = 85°C, R.H. = 81%, V_{CC} = V_{CC} opt, static)

Wet high temperature operating life test is performed to evaluate the moisture resistance characteristics of plastic encapsulated components. Long time testing is performed under static bias conditions at 85°C/81 percent relative humidity with nominal voltages. To maximize metal corrosion, the biasing configuration utilizes low power levels.

INTERMITTENT OPERATING LIFE (IOPL)

(Pmax, 25°C, 2min on/2 min off)

This test is normally applied to scrutinize die bond thermal fatigue. A stressed device undergoes an "ON" cycle, where there is thermal heating due to power dissipation, and an "OFF " cycle, where there is thermal cooling due to lack of inputted power. Die attach (between die and package) and bond attach (between wire and die) are the critical areas of concern.

HIGH TEMPERATURE STORAGE TEST (HTS)

(Ta = 125°C, UNBIASED)

High temperature storage is a test in which devices are subjected to elevated temperatures with no applied bias. The test is used to detect mechanical instabilities such as bond integrity, and process wearout mechanisms.

PRESSURE COOKER TEST (PCT)

(121°C, 15PSIG, 100% R.H., UNBIASED)

The pressure cooker test checks for resistance to moisture penetration. A highly pressurized vessel is used to force water (thereby promoting corrosion) into packaged devices located within the vessel.

TEMPERATURE CYCLING (T/C)

(−65°C to +150°C, AIR, UNBIASED)

This stess uses a chamber with alternating temperatures of −65°C and +150°C (air ambient) to thermally cycle devices within it. No bias is applied. The cycling checks for mechanical integrity of the packaged device, in particular bond wires and die attach, along with metal/polysilicon microcracks.

THERMAL SHOCK (T/S)

(−65°C to +150°C, LIQUID, UNBIASED)

This stress uses a chamber with alternting temperatures of −65°C to +150°C (liquid ambient) to thermally cycle devices within it. No bias is applied. The cycling is very rapid, and primarily checks for die/package compatibility.

RESISTANCE TO SOLDER HEAT
(Unbiased, 260°C, 10 sec)

Solder Heat Resistance is performed to establish that devices can withstand the thermal effects of solder dip, soldering iron, or solder wave operations.

MECHANICAL SHOCK
(Unbiased, 1500g, Pulse = 0.5msec)

This test determines the suitability of a device to be used in equipment where mechanical "shocks" may occur. Such shocks result from sudden or abrupt changes produced by rough (non-standard) handling, transportation, or field operations.

VARIABLE FREQUENCY VIBRATION
(Unbiased, Range = 100 to 2000Hz)

Variable Frequency Vibration is done to model the effects of differential vibration in the specified range. Die attach and bonding integrity are particularly stressed, testing the mechanical soundness of device packaging.

CONSTANT ACCELERATION
(Unbiased, 10kg to 20kg)

This is an accelerated test designed to indicate types or modes of structural and mechanical weaknesses not necessarily detectable in Mechanical Shock and Variable Frequency Vibration stressing.

RELATIVE STRESS COMPARISONS

Many stresses are run at Samsung on many different devices. Through both theoretical and actual results, it was clearly determined which stresses were most effective. Also established were the stresses which weren't fully effective.

Comparisons have been made on the basis of defects able to be determined, efficiency in detection, and cost. For the reader's benefit, Samsung provides the results of its conclusions on the following pages.

COMPARISON OF RELIABILITY TEST METHODS

Test Method	Defect	Effectiveness	Cost	Remarks
Internal Visual Inspection	Lead Structure Metalization Oxide Film Foreign Particles Die Bond Wire Bond Contamination Corroded Substrate	Good	Slightly Inexpensive to Moderate	This method of screening must be performed for high reliability devices. Cost is affected by the degree of visual inspection
Infrared ray	Design (thermal)	Very Good	Expensive	For use in design evaluation only
Radiography	Die Bond Lead Structure (Gold) Foreign Particles Manufacturing (Gross Error) Seal Package Contamination	Extremely Good Good Good Good Good Good Good	Moderate	Advantage to using this screening method lies in the ability t test die frame/ header bonding, and to be able to perform inspection after sealing. However, some materials being transparent to X-rays (for example, Al and Si) are not able to be analyzed. The use of the complex test system results in cost six times that of visual inspection.
High Temperature Storage	Electrical stability Metalization Bulk Silicon Corrosion	Good	Very Inexpensive	This is a highly desirable screening method
Temperature Cycling	Package Seal Die Bond Wire Bond Cracked Substrate Thermal Mismatching	Good	Very Inexpensive	This screening method is one of the most effective for use
Thermal Shock	Package Seal Die Bond Wire Bond Cracked Substrate Thermal Mismatching	Good	Inexpensive	While this screening method is similar to temperature cycling, it enables high stress levels as well. It is probably equal to the temperature cycling method.
Constant Acceleration	Lead Structure Die Bond Wire Bond Cracked Substrate	Good	Moderate	Doubt exists as to the effectiveness of screening aluminum wires with stress levels in the range of 0 – 20,000 G

COMPARISON OF RELIABILITY TEST METHODS (Continued)

Test Method	Defect	Effectiveness	Cost	Remarks
Shock (Without Monitoring)	Lead Structure	Fairly Poor	Moderate	Drop shock testing is thought to be inferior to constant acceleration methods. However, the pneupactor shock test is more effective. Shock test is a destructive test method.
Shock (With Monitoring)	Particles Intermittent Short Intermittent Open	Fairly Poor Fairly Good Fairly Good	Expensive	Visual inspection or radiography is more desirable for detection of particles
Vibration Fatigue	Lead Structure Package Die Bond Wire Bond Cracked Substrage	Fairly Poor	Expensive	This test is destructive and without merit.
Variable Frequency Vibration (Without Monitoring)	Package Die Bond Wire Bond Substrate	Fairly Poor	Expensive	
Variable Frequency Vibration (Without Monitoring)	Foreign Particles Lead Structure Intermittent Open	Fairly Good Good Good	Very Expensive	The effectiveness of the method for detecting particles depends on the type of particle
Random Vibration (Without Monitoring)	Package Die Bond Wire Bond Substrate	Good	Expensive	This screening method is more effective than variable frequency vibration (without monitoring), when used with equipment intended for space vehicle operation, although it is more expensive
Random Vibration (Without Monitoring)	Foreign Particle Lead Structure Intermittent Open	Fairly Good Good Good	Very Expensive	This is one of the most expensive screening methods
Vibrational Noise	Foreign Particles	Good	Expensive	
Radioisotope Leak Test	Package Seal	Good	Moderate	This screening method is effective for detecting leakage in the range 10E6 – 10E12 atm. ml/sec

COMPARISON OF RELIABILITY TEST METHODS (Continued)

Test Method	Defect	Effectiveness	Cost	Remarks
Helium Leak Test	Package Seal	Good	Moderate	This screening method is effective for detecting leak in the range 10E6 – 10E12 atm. ml/sec
Gross Leak Test	Package Seal	Good	Inexpensive	Effectiveness is dependent upon volume. Testing is possible for detecting leaks above 10E-3 atm. ml/sec.
High Voltage Test	Oxide Film	Good	Inexpensive	Effectiveness Depends on Structure
Insulation Resistance	Lead Structure Metallization Contamination	Fairly Good	Inexpensive	
Intermittent Operation	Metallization Bulk Silicon Oxide Film Inversion/Channeling Design Parmeter Drift Contamination	Good	Expensive	Probably about the same as AC operating life
AC Operation	Metallization Bulk Silicon Oxide Film Inversion/Channeling Design Parmeter Drift Contamination	Very Good	Expensive	
DC Operation	Basically the Same as Intermittent Operation	Good	Expensive	The AC operation life method is more effective for any failure mechanism
High Temperature AC Operation	Same as AC Operation Life Test	Extremely Good	Very Expensive	Failures are accelerated by temperature. This is probably the most expensive and one of the most effective screening methods.
High Temperature Reverse Bias	Inversion /Channeling	Fairly Poor	Expensive	

RELIABILITY TEST RESULTS

This section is divided into two parts-actual and predicted test results. Actual test results are those derived via accelerated stressing done by the QA department. Predicted results are calculated by taking actual test results and derating them using statistical and mathematical models to determine device performance in "real-time" user conditions.

ACTUAL TEST RESULTS

Stress	Conditions	Number of Devices	Number of Hours/Cycles	Number of Device Hours/Cycles	Number of Failures	% Failures per 1000HRS (Cycles) (60% UCL)
HOPL	$T_j = 125°C$ $V_{CC} = V_{CC}$ max	180	1,000	180,000	0	0.51%/1K HR
WHOPL	85°C/81% R.H. $V_{CC} = V_{CC}$ opt	180	1,000	180,000	0	0.51%/1K HR
IOPL	$Ta = 25°C$ $V_{CC} = V_{CC}$ max	180	1,000	180,000	0	0.51%/1K HR
HTS	$Ta = 125°C$ Unbiased	135	1,000	135,000	0	0.67%/1K HR
PCT	121°C 15 PSIG	225	168	37,800	1	0.89%/168 HR
T/C	−65°C to 150°C Air to Air	180	200	36,000	0	0.51%/200 CL
T/S	−65°C to 150°C Liquid to Liquid	135	200	27,000	0	0.67%/200 CL

PREDICTED TEST RESULTS

The Arrhenius equation, which is reviewed in another section of this chapter, can be applied to derive typical "user-condition" device failure rates.

STESS: HOPL

180,000 Device Hours at 125°C
Average Activation Energy: 1.0 eV.
De-Rating to User Conditions Yields:

70°C Operation

Equivalent Device Hours	% Failures Per 1000 Hours (60% UCL)	*FITs	**MTTF (Years)
1.93×10^7	0.0047	47	2435

55°C Operation

Equivalent Device Hours	% Failures Per 1000 Hours (60% UCL)	*FITs	**MTTF (Years)
9.07×10^7	0.0010	10	11447

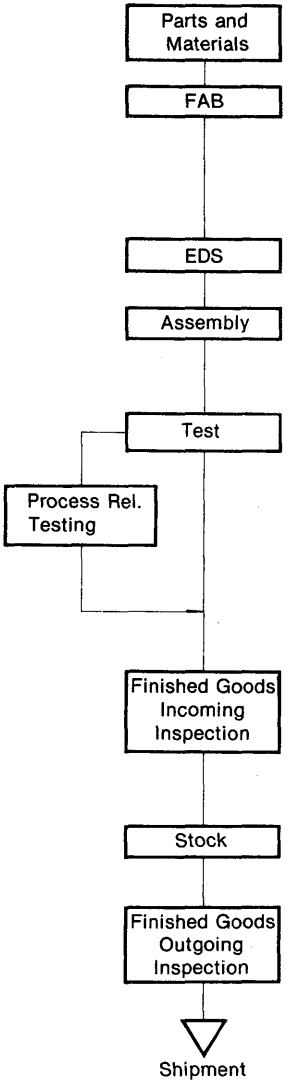
* FIT : Failure in time or failure unit. Represents the number of failures expected for 10^9 (one billion) device hours.

** MTTF: Mean time to failures.

PROCESS CONTROL

GENERAL PROCESS CONTROL

The general process flow in Samsung is shown in Figure 8. This illustration contains the standard process flow from incoming parts and materials to customer shipment.



Acceptance inspection (according to acceptance inspection plan)

Process quality control
- Check of each condition by process quality control procedures
- Process inspection
- Lot control
- Equipment calibration and maintenance

100% Electrical Die Sorting

Process Quality Control and screening of infant mortality defects
- Mechanical screen
- Thermal shock
- Burn-in

100% package sorting of electrical characteristics and marking

Reliability monitoring
1. PRT (Process Reliability Testing)
2. DRT (Device Reliability Testing)

- High Temperature Operating Life Test
- Environmental test
- Life Test

Sampling Inspection
- Dimensions
- Visual
- Electrical characteristics
- Periodic calibration of measuring equipment

Stock control
- Age control

Sampling Inspection (when applicable)

General Process Flow Chart

WAFER FABRICATION

Process Controls

The Quality Control program utilizes the following methods of control to achieve its previously stated objectives: process audits, environmental monitors, process monitors, lot acceptance inspections, and process integrity audits.

Definitions

The essential method of the Quality Control Program is defined as follows:

1. Process Audit-Performed on all operations critical to product quality and reliability.
2. Environmental Monitor-Monitors concerning the process environment, *i.e.,* water purity, temperature, humidity, particle counts.
3. Process Monitor-Periodic inspection at designated process steps for verification of manufacturing inspection and maintenance of process average. These inspections provide both attribute and variable data.
4. Lot Acceptance-Lot-by-lot sampling. This sampling method is reserved for those operations deemed as critical, and require special attention.

Environmental Monitor

Process	Control Item	Spec. Limit	Insp. Frequency
Clean Room	• Temperature • Humidity • Particle • Air Velocity	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	24 Hrs. 24 Hrs. 24 Hrs. 24 Hrs.
D.I. Water	• Particle • Bacteria • Resistivity	• 5 ea/50ml (0.8μ) • 50 colonies/100ml (0.45μ) • Main (Line): More than 16 Mohm-cm • Using point: More than 14 Mohm-cm	24 Hrs. Weekly 24 Hrs. 24 Hrs.

* Instruments
- FMS (Facility Monitoring System) HIAC/ROYCO
- CPM (Central Particle Monitoring System-Dan Scientific)
- Liquid Dust Counter Etch Rate
- Filtration System for Bacterial check
- Air Particle counter
- Air Velocity meter

Process Monitor

Process	Control Item	Spec. Limit	Insp. Frequency
Photo	• Aligner N_2 Flow Rate • Aligner Vacuum • Aligner Air • Aligner Pressure • Aligner Intensity • Coater Soft Bake Temperature Vacuum	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift
Etch	• Etchant Temp. • Etch Rate • Spin Dryer N_2 Flow RPM • Hard Bake Temp. N_2 Flow	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift

Process Monitor (Continued)

Process	Control Item	Spec. Limit	Insp. Frequency
Thin Film	• Cooling Water Temp. • Thickness	• 26 ± 3°C • Individual Spec.	Once/Shift Once/Shift
CVD	• Pin Hole • Thickness	• Individual Spec. • Individual Spec.	Once/Shift Once/Shift
Diffusion	• Tube Temp. • C-V Plot Run Tube • Sheet Resistance • Thickness	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	Once/Shift Once/Shift Once/10days Once/Shift Once/Shift

Raw Material Incoming Inspection

1. Mask Inspection

Defect Detection	• Pinhole & Clear-extension • Opaque Projections & Spots • Scratch/Particle/Stain • Substrate Crack/Glass-chip • Others	All Masks	• Defect Size ≤ 1.5μm • Defect Density ≤ 0.124EA/cm²
Registration	• Run-out (X-Y Coordinate) • Orthogonality • Drop-in Accuracy • Die Fit/Rotation	20% • All New Masks	± 0.75μm ± 0.75μm ± 0.50μm ± 0.50μm
Critical Dimension	• Critical Dimension	All Masks	Purchasing Spec.

* Instrument
  - Auto mask inspection system for defect-detection (NJS 5MD-44)
  - Comparator for registration (MVG 7X7)
  - Automatic linewidth measuring system for CD (MPV-CD)

2. Wafer Inspection

Purpose	Insp. Items	Sample	Remarks
Structural	• Crystallographic Defect	All Lots	• Sirtl Etch
Electrical	• Resistivity • Conductivity	All Lots	• Monitor Water
Dimensional	• Thickness • Diameter • Orientation • Flatness	All Lots	TTV, NTV, Epi-thickness TIR (FPD) Local Slope
Visual	• Surface Quality • Cleanliness	All Lots	Purchasing Spec.

* Instrument
  - 4 point probe for resistivity (Kokusai VR-40A, Tencor sonogage, ASM AFPP)
  - Flatness measuring system (Siltec)
  - Epi. layer thickness gauge (Digilab FTG-12, Qualimatic S-100)
  - Automatic Surface Insp. System (Aeronca Wis-150)
  - Non-contact thickness gauge (ADE6034)

In-Process Quality Inspection (FAB)

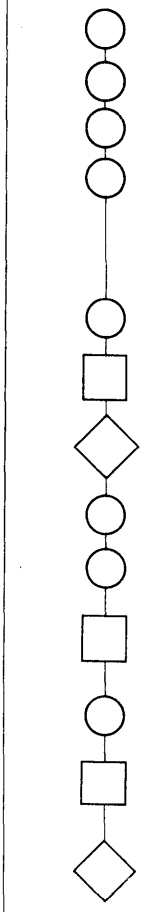
1. Manufacturing Section

Process Step	Process Control Insp.	Frequency
Oxidation	Oxide Thickness	All Lots
Diffusion	Oxide Thickness Sheet Resistance Visual	All Lots All Lots All Lots
Photo	Critical Dimension Visual Mask Clean Inspection	All Lots (MOS) All Lots All Masks with Spot Light (MOS) or Microscope (BIP)
Etch	Critical Dimension Visual	All Lots All Wafers
Thin Film	Metal Thickness Visual	All Lots All Lots
Ion Implant	Sheet Resistance	All Lots (Test Wafer)
Low Temp. Oxide	Thickness	All Lots
	Visual	All Lots
E-Test	Electrical Characteristics	All Lots
Fab. Out	Visual	All Wafers

2. FAB, QC Monitor/Gate

Process Step	FAB, QC Insp.	Frequency
Oxidation	Oxide Thickness C-V Test on Tubes Visual	Once/Shift Once/10 Days and After CLN Once/Shift
Diffusion	Oxide Thickness C-V Test on Tubes Visual	Once/Shift Once/10 Days and After CLN Once/Shift
Photo	Critical Dimension Visual Mask CLN Inspection	All Lots (MOS) Once/Shift All Masks After 10 Times Use
Etch	Critical Dimension Visual	All Lots (MOS) All Lots
Thin Film	C-V Test on Tubes on Lots Reflectivity	Once/10 Days and After CLN Once/Shift Once/Shift
Low Temp. Oxide	Refractive Index, Wt% of Phosphorus Visual	1 Test Wafer/Lot 1 Test Wafer/Lot 1 Test Wafer/Lot
E-Test	Measuring Data	All Lots
Calibration	Instrument for Thickness and C.D. Measuring	Once/week

3. Photo/Etch process quality control

Process Flow	Process Step	MFG. Control Item	QC Monitor/Gate
	Prebake	Oven PM, Temperature Time	Oven Particle Temp. N_2 Flow Rate
	Photo Resist (PR) —spin	Thickness Machine PM	
	Soft Bake	Oven PM, Temperature Time	Temp. N_2 Flow Rate
	Align/Expose	Light Uniformity Alignment, Focus Test Mask Clean Inspection Mask Clean Exposure Light Intensity	Light Intensity Mask Clean Insp.
	Develop	Equipment PM Solution Control	Vacuum
	Develop Check	PR/C.D.'S Alignment Particles Mask and Resist Defects	
	QC Inspection		Critical Dimension (CD)
	Hard Bake	Oven PM, Temperature Time	Temp. N_2 Flow Rate
	Etch	Etch rate, Equipment PM & Settings, Etch Time to Clear	Etchant Temp. Etch Rate
	Inspection	Over/Under	
	PR Strip	Machine-PM	
	Final Check	C.D.'S Over and under Etch, Particles, PR Residue, Defects, Scratches	
	QC Inspection		Same as Final Check, However, More Intense on limited Sample Basis. (AQL 6.5%)

Note: PM represents Preventive Maintenance

4. Reliability-related Interlayer Dielectric, Metallization, and Passivation Process Quality Control Monitor

Item	Frequency
Wt% Phosphorus Content of the Dielectric Glass	1/Shift
Metallization Interconnect	1/Month
Al Step Coverage	1/Month
Metallization Reflectivity	1/Shift
Passivation Thickness and Composition	1/Shift
Thin Film Defect Density	1/Shift

Figure 9. General Wafer Fabrication Flow

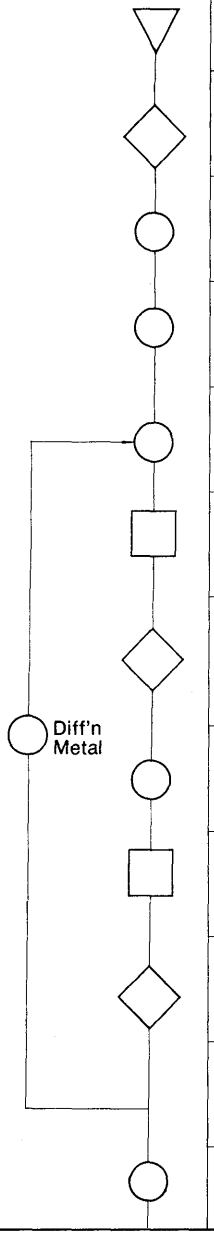
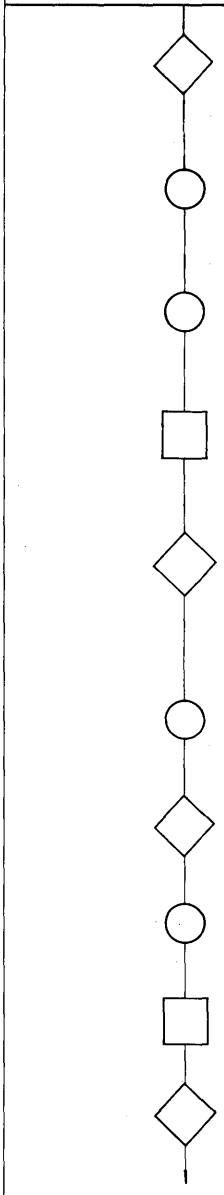
Process Flow	Process Step	Major Control Item
	Wafer and Mask Input	
	Starting Material Incoming Inspection	Mask: (See mask Inspection) Wafer: (See wafer Inspection)
	Wafer Sorting and Labelling	Resistivity
	Initial Oxidation	Oxide Thickness
	Photo	• (See manufacturing section) • (See FAB, QC Monitor/gate)
	Inspection	• Critical Dimension • Visual/Mech — Major: AQL 1.0% — Minor: AQL 6.5%
	QC Gate	• Critical Dimension
	Etch	• (See manufacturing section) • (See FAB, QC Monitor/gate)
	Inspection	• Critical Dimension • Visual/Mech — Major: AQL 1.0% — Minor: AQL 6.5%
	QC Gate	• Critical Dimension • Visual/Mech
	Diffusion Metalization	• (See in-process Quality Inspection)
	E-test	• Electrical Characteristics

Figure 9. General Wafer Fabrication Flow (Continued)

Process Flow	Process Step	Major Control Item
 Die Attach	QC Gate	• Electrical Characteristics
	Back-Lap	• Thickness
	Back Side Evaporation	• Thickness, Time Evaporation Rate
	Final Inspection	• All Wafers Screened (Visual/Mech)
	QC Fab. Final Gate	• Visual/Mech. — Major: AQL 1.0% — Minor: AQL 6.5%
	EDS (Electrical Die Sorting)	
	QC Gate	• Function Monitor
	Sawing	
	Inspection	• Chip Screen
	QC Final Inspection	• AQL 1.0% • Fab. Defect • Test Defect • Sawing Defect

ASSEMBLY

The process control and inspection points of the assembly operation are explained and listed below:

1. Die Inspection:

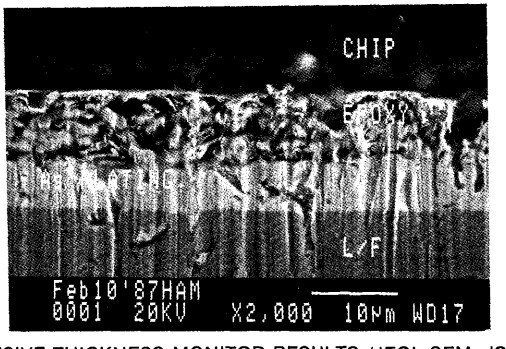
   Following 100% inspection by manufacturing, in-process Quality Control samples each lot according to internal or customer specifications and standards.

2. Die Attach Inspection:

   Visual inspection of samples is done periodically on a machine/operator basis. Die Attach techniques are monitored and temperatures are verified.

3. Die Shear Strength:

   Following Die Attach, Die Shear Strength testing is performed periodically on a machine/operator basis. Either manual or automatic die attach is used.



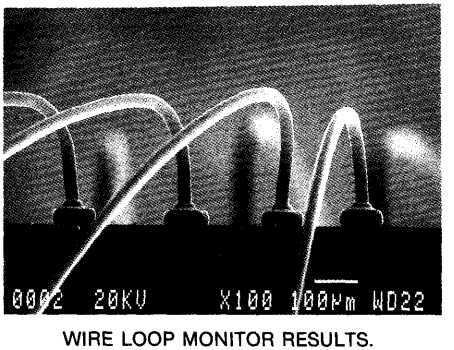
DIE ADHESIVE THICKNESS MONITOR RESULTS.(JEOL SEM, JSM IC845)

4. Wire Bond Inspection:

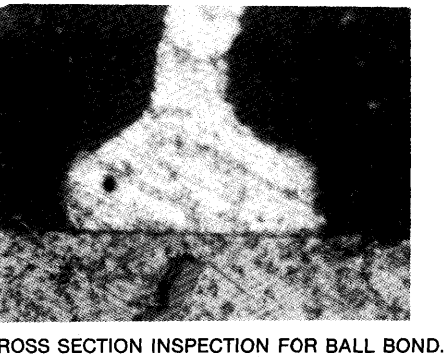
   Visual inspection of samples is complemented by a wire pull test done periodically during each shift. These checks are also done on a machine/operator basis and XR data is maintained.

5. Pre-Seal/Pre-Encapsulation Inspection:

   Following 100% inspection of each lot, samples are taken on a lot acceptance basis and are inspected according to internal or customer criteria.



WIRE LOOP MONITOR RESULTS.



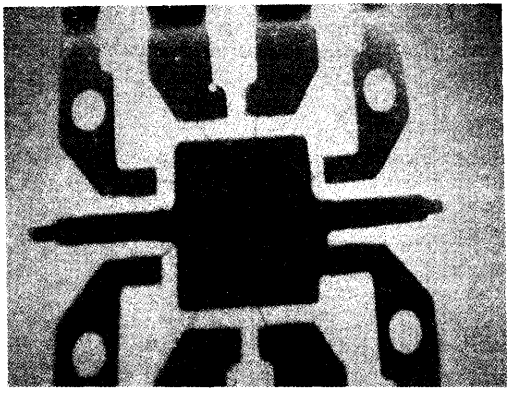
CROSS SECTION INSPECTION FOR BALL BOND.

6. Seal Inspection:

   Periodic monitoring of the sealing operation checks the critical temperature profile of the sealing oven for both glass and metal seals.

7. Post-Seal Inspection:

   Subsequent to a 100% visual inspection, In-Process Quality Control samples each for conformance to visual criteria.



X-RAY MONITOR RESULT (PHILIPS MG161)

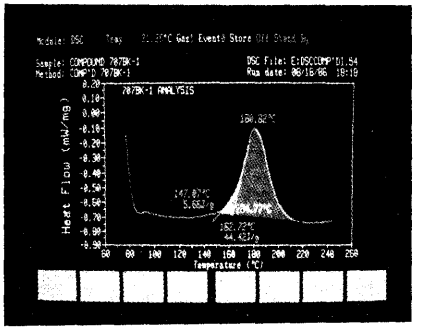
8. General Assembly Flow is shown in Figure 11.

Sampling Plans

1. Sampling plans are based on an AQL (Acceptable Quality Level) concept and are determined by internal or by customer specifications.

2. Raw Material Incoming Inspection. (confined)

Material	Inspection Item	Acceptable Quality Level
Lead Frame	1) Visual Inspection 2) Dimension Inspection 3) Function Test 4) Work Test	LTPD 10%, C = 2 LTPD 20%, C = 0 LTPD 20%, C = 0 LTPD 20%, C = 0
Wafer	1) Visual Inspection	AQL 0.65%
Au/Al Wire	1) Visual Inspection 2) Bond Pull Strength Test 3) Bondability Test 4) Chemical Composition Analysis	n:5, C = 0 n: 13, C = 0 Critical Defect: 0.65% Major Defect: 1.0% Minor Defect: 1.5% n: 5, C = 0
Molding Compound	1) Visual Inspection 2) Moldability Test 3) Chemical Composition Analysis	n: 5, C = 0 Critical Defect: 0.15% Major Defect: 1.0% Minor Defect: 1.5% n: 5, C = 0



MOLDING COMPOUND INCOMING INSPECTION
(THERMAL ANALYSER, DUPONT 9900)

(Continued)

Material	Inspection Item	Acceptable Quality Level
Packing Tube & Pin	1) Visual Inspection 2) Dimension Inspection 3) Electro-Static Inspection 4) Hardness Test	LTPD 15%, C=2 LTPD 15% C=2 n: 5, C=0 n: 5, C=0
Solder	1) Visual Inspection 2) Weight Inspection 3) Chemical Composition Analysis	LTPD 20% C=0 LTPD 20% C=0 LTPD 20% C=0
Flux	1) Acidity Test 2) Specific Gravity Test 3) Chemical Composition Analysis	LTPD 20% C=0 LTPD 20% C=0 LTPD 20% C=0
Solder Preform	1) Visual Inspection 2) Work Test 3) Chemical Composition Analysis	AQL 1.0% AQL 1.0% AQL 1.0%
Coating Resin	1) Visual Inspection 2) Work Test 3) Chemical Composition Analysis	AQL 1.0% AQL 1.0% AQL 1.0%
Marking Ink	1) Work Test 2) Mark Permanency Test	Critical Defect: 0.15% Major Defect: 1.0% Minor Defect: 1.5% n: 5, C=0
Chip Carrier	1) Visual Inspection 2) Dimension Inspection 3) Electro-Static Inspection 4) Hardness Test	LTPD 15% C=2 LTPD 15% C=0 n: 5, C=0 n: 5, C=0
Vinyl Pack	1) Visual Inspection 2) Work Test 3) Electro-Static Inspection	LTPD 20% C=0 LTPD 20% C=0 LTPD 15% C=0
Ag Epoxy	1) Work Test 2) Chemical Composition Analysis	n:8, C=0 n:8, C=0
Letter Marking	1) Visual Inspection 2) Work Test	
Spare Parts & Others	1) Dimension Inspection 2) Visual Inspection	n:5, C=0 n:5, C=0

3. In-Process Quality Inspection

A. Assembly Lot Acceptance Inspection

(1) Acceptance quality level for wire bond gate inspection

Defect Class	Inspection Level	Type of Defect	
Critical Defect	AQL 0.65%	— Missing Metal — Chip Crack — No Probe — Epoxy on Die — Mixed Device — Wrong Bond — Missing Bond	— Diffusion Defect — Ink Die — Exposed Contact — Bond Short — Die Lift — Broken Wire
Major Defect	AQL 1.0%	— Metal Missing — Metal Adhesion — Pad Metal Discolored — Tilted Die — Die Orientation — Partial Bond	— Oxide Defect — Probe Damage — Metal Corrosion — Incomplete Wetting — Weakened Wire
Minor Defect	AQL 1.5%	— Adjacent Die — Passivation Glass — Die Attach Defect — Wire Loop Height — Extra Wire	— Contamination — Ball Size — Wire Clearance — Bond Deformation

(2) Acceptance quality level for Mold/Trim gate inspection

Defect Class	Inspection Level	Kind of Defect	
Critical Defect	AQL 0.15%	— Incomplete Mold — Void, Broken Package — Misalignment	— Deformation — No Plating — Broken Lead
Major Defect	AQL 0.4%	— Ejector Pin Defect — Package Burr — Flash on Lead	— Crack, Lead Burr — Rough Surface — Squashed Lead
Minor Defect	AQL 0.65%	— Lead Contamination — Poor Plating — Package Contamination	— Bent Lead

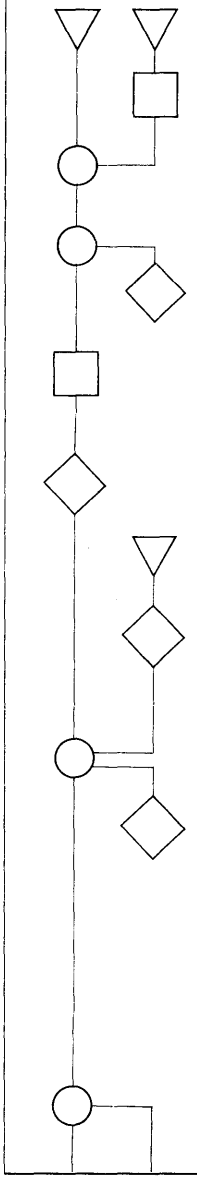
B. In-process monitor inspection

Inspection Item	Frequency	Reference
• Die Shear Test	Each Lot	MIL-STD-883C, 2019-2
• Bond Strength Test	Each Lot	MIL-STD-883C, 2011-4
• Solderability Test	Weekly	MIL-STD-883C, 2003-3
• Mark Permanency Test	Weekly	MIL-STD-883C, 2015-4
• Lead Integrity Test	Weekly	MIL-STD-883C, 2004-4
• In-Process Monitor Inspection for Product	4 Times/Shift/Each Process	Identify for Each Control Limit
• X-Ray Monitor Inspection for Molding	2 Times/Shift/Mold Press	Identify for Each Control Limit
• Monitor Inspection for Production Equipment	2 Times/Shift/Each Unit of Equipment	Identify for Each Control Limit

4. Outgoing quality inspection plan (LTPD)

Defect Class	Discrete	LSI	Kind of Defect
Critical Defect electrical visual	1%	2%	Open, short Wrong configuration, no marking
Major Defect electrical visual	1.5%	3%	Items which affect reliability most strongly
Minor Defect electrical visual	2%	5%	Items which minimally or do not affect reliability at all (cosmetic, appearance, etc.)

Figure 10. General Assembly Flow

Process Flow	Process Step	Major Control Item
	Wafer	
	Wafer Incoming Inspection	Q.C. Wafer Incoming Inspection AQL 4.0%
	Tape Mount	
	Sawing Q.C. Monitor	Q.C. Monitoring: — Chip-out — Scratch — Crack — Sawing Discoloration — Sawing-speed — Cut Count — D.I. Purity — CO_2 Bubble Purity
	Visual Inspection	100% Screen: — FAB Defect — EDS Test Defect — Sawing & Scratch Defect
	Q.C. Gate	1st AQL 1.0% Reinspection AQL: 0.65%
	Lead Frame (L/F)	
	Lead Frame Incoming	*Q.C.L/F Incoming Inspection 1. Acceptance Quality Level — Dimension LTPD 20%, C=0 — Visual & Mechanical: LTPD 10%, C=2 — Functional Work Test: LTPD 10%, C=2
	Die Attach (D/A)	
	Q.C. Monitor	*Q.C.D/A Monitor Inspection 1. Bond force 2. Frequency: 4 Times/Station/Shift 3. Sample: 24 ea Time 4. Acceptance Criteria
	Cure	

Defect	Acceptance	Reject
Critical	0	1
Major	1	2

Figure 10. General Assembly Flow (Continued)

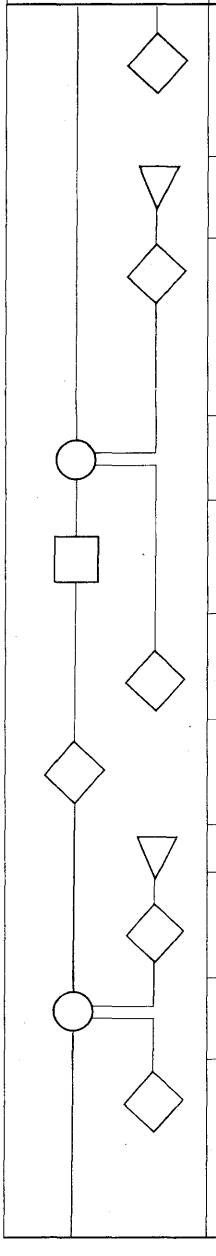
Process Flow	Process Step	Major Control Item
	Q.C. Monitor	*Q.C. Cure Monitor Inspection 1. Control Item — Temperature — In/out Time 2. Frequency — 1 Time/Shift
	Au Wire	
	Bonding Wire Incoming Inspection	*Q.C Au Wire Incoming Inspection 1. Visual Inspection: N = 5, C = 0 2. Bond Pull Test Strength Test: N = 13, C = 0 3. Bondability Test — Critical Defect: AQL 0.65% — Major Defect: AQL 1.0% — Minor Defect: AQL 1.5%
	Wire Bonding (W/B)	
	100% Visual Inspection	
	Q.C. Monitor	*Q.C. W/B Monitor Inspection 1. Frequency: 6 Times/Mach/Shift
	Q.C. Gate	1. Q.C. Acceptance Quality Level — Critical Defect: AQL 0.65% — Major Defect: AQL 1.0% — Minor Defect: AQL 1.5%
	Mold Compound	
	Incoming Inspection Mold	*Moldability Test — Critical Defect: AQL 0.15% — Major Defect: AQL 1.0% — Minor Defect: AQL 1.5%
	Mold	
	Q.C. Monitor	*Q.C. Mold Monitor Inspection 1. In-Process Monitor Inspection — Frequncy: 4 Times/Station/Shift — Sample: 200 Units/Time 2. Acceptance Quality Level — Critical Defect: AQL 0.25% — Major Defect: AQL 0.4%

Figure 10. General Assembly Flow (Continued)

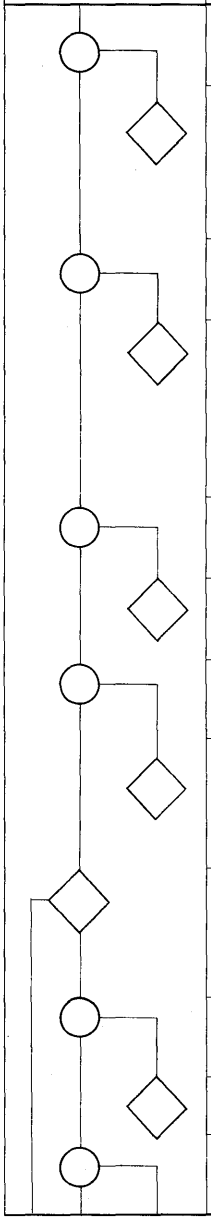
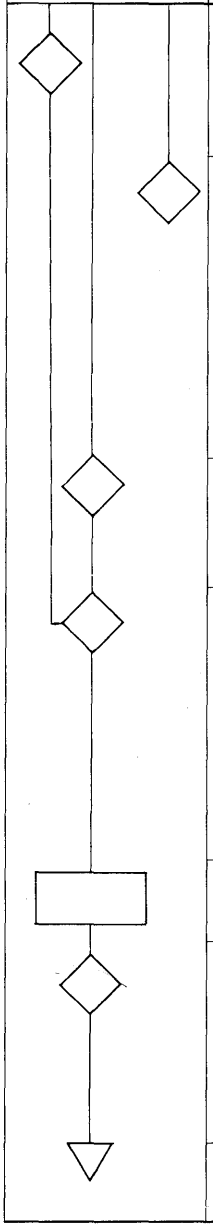
Process Flow	Process Step	Major Control Item
	Cure	
	Q.C. Monitor	*Q.C. Cure Monitor Inspection 1. Control Item — Temperature — In/out Time 2. Frequency — 1 Time/shift
	Deflash	
	Q.C. Monitor	*Q.C. Deflash Monitor Inspection 1. Control Item — Pressure — Belt Speed — Visual/Mechanical Inspection 2. Frequency: 4 Times/Mach/Shift 3. Identify each Defect Control Limit
	TRIM/BEND	
	Q.C. Monitor	*Q.C. Trim/Bend Monitor Inspection 1. Visual Inspection 2. Frequency: 4 Times/Station/Shift
	Solder	100% Visual Inspection
	Q.C. Monitor	*Q.C. Solder Monitor Inspection 1. Frequency: 4 Times/Mach/Shift 2. Criteria — Critical Defect: AQL 0.65% — Major Defect: AQL 1.0%
	Q.C. Gate	*Q.C. Mold Gate — Acceptance Criteria Critical Defect: AQL 0.15% Major Defect: AQL 0.4% Minor Defect: AQL 0.65%
	Test	100% Electrical Test
	Q.C. Monitor	Correlation Sample Reading for Initial Device Test
	Mark	100% Visual Inspection

Figure 10. General Assembly Flow (Continued)

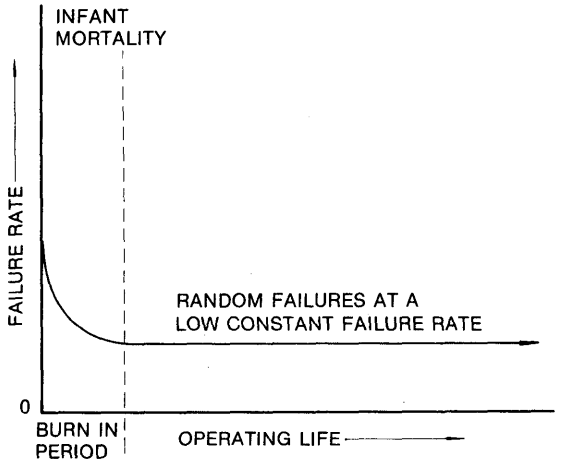
Process Flow	Process Step	Major Control Item
	PRT Monitoring (Process Reliability Testing)	1. PRT — HOPL (168 HRS), PCT (48 HRS) — Other (when applicable) 2. Acceptance Criteria: LTPD 10%
	Q.C. Monitor	*Q.C. Marking Monitor Inspection — Frequency: 4 Times/Station/Shift — Sample: 24 Units/Time — Identify for Each C.L. — Acceptance Criteria Defect / Acceptance / Reject Critical / 0 / 1 Major / 1 / 2
	Q.C. Gate	*Q.C. Final Acceptance Level — Critical Defect: AQL 0.15% — Major Defect: AQL 0.4% — Minor Defect: AQL 0.65%
	Q.A. Gate	*Q.C. Incoming Inspection 1. Critical Defect: — Electrical Test: LTPD 2% (N = 116, C = 0) — Visual Test: LTPD 2% (N = 116, C = 0) 2. Major Defect: — Electrical Test: LTPD 3% (N = 116, C = 1) — Visual Test: LTPD 3% (N = 116, C = 1) 3. Minor Defect: — Electrical Test: LTPD 5% (N = 116, C = 2) — Visual Test: LTPD 5% (N = 116, C = 2)
	Stock	*Age Control
	Q.A. Gate	*Q.A. Outgoing Inspection 1. Quantity 2. Customer 3. Packing 4. Sampling Inspection (when applicable) — Sampling plan is same as incoming Inspection
	Shipment	

SAMSUNG's BEST PROGRAM

The SAMSUNG Best Program has been designed to offer the customer an alternative to standard off-the-shelf plastic encapsulated LINEAR circuits. The Best Program will significantly reduce incoming inspection requirements as well as early device failures (infant mortalify). These results are achieved by a tightened AQL inspection plan and a burn-in of each unit for 160 +8, −0 hours at 125°C or equivalent conditions established from a time/temperature regression curve.

The AQL Plan. Acceptable Quality Levels (AQL) are a measure of the quality of outgoing LINEAR circuits. These levels are established by the manufacturer to show the process percent defective being produced and to ensure that the customer is receiving material that meets his requirements. The SST Best Program has tightened these AQL levels to a point at which incoming inspection by the customer is no longer a necessity. Best product quality is monitored significantly more closely than standard product; those lots which fail the AQL level are 100% reworked before resubmission to the AQL gate.

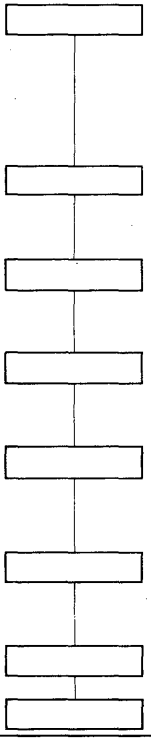
The Reliability Plan. Reliability is the statistical probability that a product will give satisfactory performance for a specified period of time when used under specified conditions. A typical rate curve is shown below:



eliability theory assumes that devices fail according to the above curve. When a group of devices is manufactured a small portion of the units will be inherently weaker than the average. These weak units will probably fail during the first few hours of operation—hence the term "infant mortality." If the units are burned-in however, thereby allowing the weak units to fail, there is a much lower probability that those finally put into system use will fail.

The SAMSUNG Best Flow. In order to achieve an extremely high quality unit and reduce infant mortality failures the following flow has been established:

Process Flow

FLOW CHART	DESCRIPTION
	WAFER FABRICATION LINEAR PROCESS CV PLOTS OXIDE THICKNESS MEASUREMENTS OPTICAL INSPECTIONS SEM ANALYSIS
	ENCAPSULATION MOLDING COMPOUND ULTRA PURE FOR LINEAR APPLICATIONS
	POST MOLD BAKE 6 HOURS AT 175 DEG. C. CURES PLASTIC STRESSES ALL WIRE BONDS AND DIE
	O/S FUNCTIONAL ELECTRICAL 100% TESTING OPENS/SHORTS AND INTERMITTENTS REMOVE
	HIGH TEMPERATURE BURN-IN 160 HOURS AT 125 DEG. C. OR EQUIVALENT CONDITIONS ESTABLISHED FROM A TIME/ TEMPERATURE REGRESSION CURVE. 0.96 eV
	FULL FUNCTIONAL AND PARAMETRIC ELECTRICAL TESTING 100% ELECTRICAL TESTING AC, DC 88 DEG. C.
	TIGHT AQL SAMPLING PLAN ELECTRICAL – 0.05% AQL AT 88 DEG. C. MECHANICAL – 0.01% AQL CRITICAL & MAJOR
	SHIP UNITS

RELIABILITY AND PREDICTION THEORY

RELIABILITY

Reliability can be loosely characterized as long term product quality.

There are two types of reliability tests: those performed during design and development, and those carried out in production. The first type is usually performed on a limited sample, but for long periods or under very accelerated conditions to investigate wearout mechanisms and determine tolerances and limits in the design process. The second type of tests is performed periodically during production to check, maintain, and improve the assured quality and reliability levels. All reliability tests performed by Samsung are under conditions more severe than those encountered in the field, and although accelerated, are chosen to simulate stresses that devices will be subjected to in actual operation. Care is taken to ensure that the failure modes and mechanisms are unchanged.

FUNDAMENTALS

A semiconductor device is very dependent on its conditions of use (*e.g.,* junction temperature, ambient temperature, voltage, current, *etc.*). Therefore, to predict failure rates, accelerated reliability testing is generally used. In accelerated testing, special stress conditions are considered as parametrically related to actual failure modes. Actual operating life time is predicted using this method. Through accelerated stresses, component failure rates are ascertained in terms of how many devices (in percent) are expected to fail for every 1000 hours of operation. A typical failure rate versus time of activity graph is shown below (the so-called "bath tub curve")

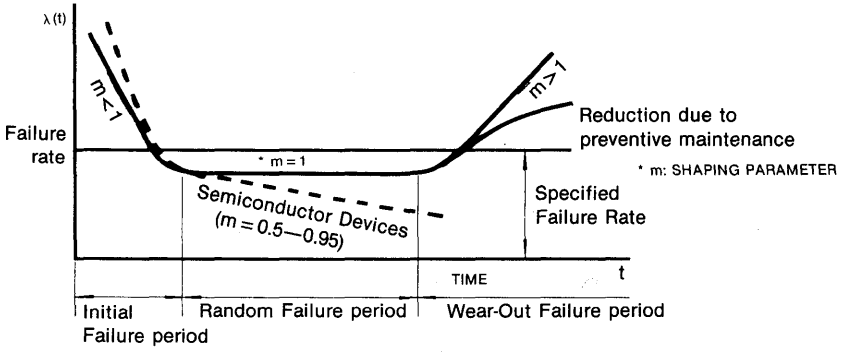


Figure 3. Failure Rate Curve ("Bath Tub Curve")

During their initial time period, products are affected by "infant mortality," intrinsic to all semiconductor technologies. End users are very sensitive to this parameter, which causes early assembly/operation failures in their own system. Periodically, Samsung reviews and publishes life time results. The goal is a steady shift of the limits as shown below.

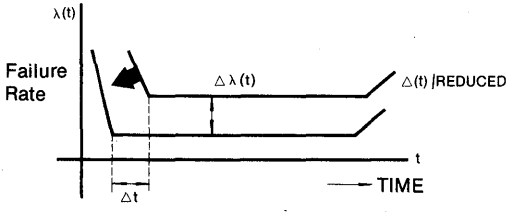


Figure 4. Failure Rate

ACCELERATED HUMIDITY TESTS

To evaluate the reliability of products assembled in plastic packages, Samsung performs accelerated humidity stressing, such as the Pressure Cooker Test (PCT) and Wet High Temperature Operating Life Test (WHOPL).

Figure 5 shows some results obtained with these tests, which illustrate the improvements in recent years. These improvements result mainly from the introduction of purer molding resins, new process methods, and improved cleanliness.

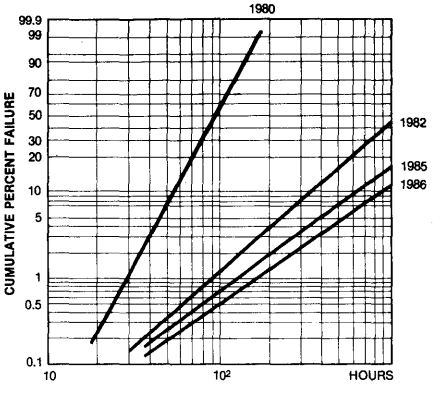


Figure 5. Improvement in Humidity Reliability

ACCELERATED TEMPERATURE TESTS

Accelerated temperature tests are carried out at temperatures ranging from 75°C to 200°C for up to 2000 hours. These tests allow Samsung to evaluate reliability rapidly and economically, as failure rates are strongly dependent on temperature.

The validity of these tests is demonstrated by the good correlation between data collected in the field and laboratory results obtained using the Arrhenius model. Figure 6 shows the relationship between failure rates and temperatures obtained with this model.

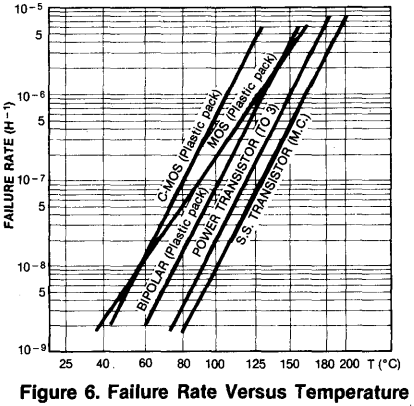


Figure 6. Failure Rate Versus Temperature

FUNDAMENTAL THEORY FOR ACCELERATED TESTING

Accelerated life testing is powerful because of its strong relation to failure physics. The Arrhenius model, which is generally used for failure modelling, is explained below.

1. Arrhenius model

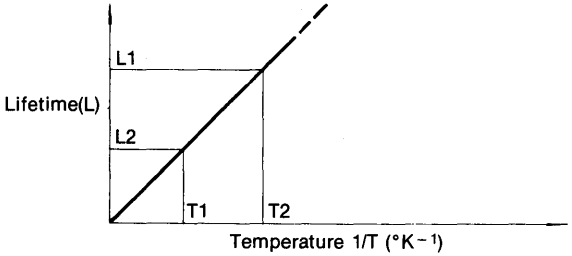
This model can be applied to accelerated Operating Life Tests and uses absolute (Kelvin) temperatures.

$L = A + Ea/K \cdot Tj$

- L : Lifetime
- A : Constant
- Ea : Activation Energy
- K : Boltzman's constant
- Tj : Absolute Junction temperature

If Lifetimes L1 and L2 correspond to Temperatures T1 and T2:

$$L1 = L2 \exp \frac{Ea}{K} \left(\frac{1}{T1} - \frac{1}{T2} \right)$$



Actual junction temperature should always be used, and can be computed using the following relationship.

$$Tj = Ta + (P \times \theta ja)$$

Where Tj = Junction temperature
Ta = Ambient temperature
P = Actual power consumption
θ ja = Junction to Ambient thermal resistance (typically 100 degrees celsius/watt for a 16-Pin PDIP).

2. Activation Energy Estimate

Clearly the choice of an appropriate activation energy, Ea, is of paramount importance. The different mechanisms which could lead to circuit failure are characterized by specific activation energies whose values are published in the literature. The Arrhenius equation describes the rate of many processes responsible for the degradation and failure of electronic components. It follows that the transition of an item from an initially stable condition to a defined degraded state occurs by a thermally activated mechanism. The time for this transition is given by an equation of the form:

MTBF = B EXP (Ea/KT)
MTBF = Mean time between failures
B = Temperature-independent constant

MTBF can be defined as the time to suffer a device degradation. The dramatic effect of the choice of the Ea value can be seen by plotting the MTBF equation. The acceleration effect for a 125°C device junction stress with respect to 70°C actual device junction operation is equal to 1000 for Ea = 1eV and 7 for Ea = 0.3eV.

Some words of caution are needed about published values of Ea:

A. They are often related to high-temp tests where a single Ea (with high value) mechanism has become dominant.
B. They are specifically related to the devices produced by that supplier (and to its technology) for a given period of time
C. They could be modified by the mutual action of other stresses (voltage, mechanical, etc.)
D. Field device-application condition(s) should be considered.

(Activation energy for each failure mode)

Failure Mechanism	Ea
Contamination	1 ~ 1.4 eV
Polarization	1 eV
Aluminum Migration	0.5 ~ 1 eV
Trapping	1 eV
Oxide Breakdown	0.3 eV
Silicon Defects	0.3 ~ 0.5 eV

THE CORRECT PROCEDURE

ACCELERATED TEST → CALCULATED AT TEST CONDITIONS AND WITH A CERTAIN CONFIDENCE LEVEL

FAILURE ANALYSIS

CHOICE OF Ea → CALCULATED AT OTHER TEMPERATURES

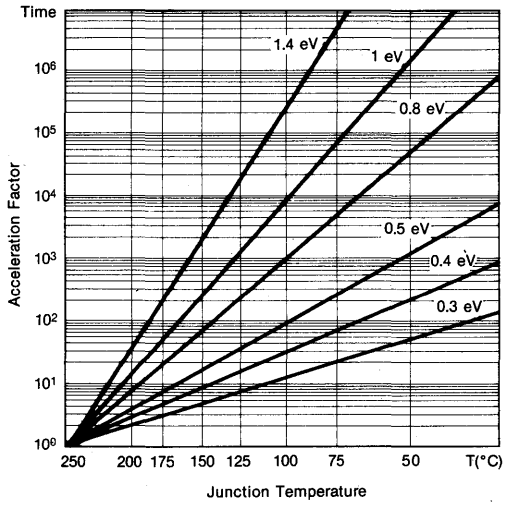


Figure 7. Acceleration Factor Vesus Temperature

Failure Rate Prediction

Accelerated testing defines the failure rate of products. By derating the data at different conditions, the life expectancy at actual operating conditions can be predicted. In its simplest form the failure rate (at a given temperature) is:

$$FR = \frac{N}{DH}$$

Where FR = Failure Rate
N = Number of failures
D = Number of components
H = Number of testing hours

If we intend to determine the FR at different temperatures, an acceleration factor must be considered. Some failure modes are accelerated via temperature stressing based upon the accelerations of the Arrhenius Law.

For two different temperatures:

$$FR(T1) = FR(T2) \exp \frac{Ea}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)$$

FR (T1) is a point estimate, but to evaluate this data for an interval estimate, we generally use a X^2 (chi square) distribution. An example follows:

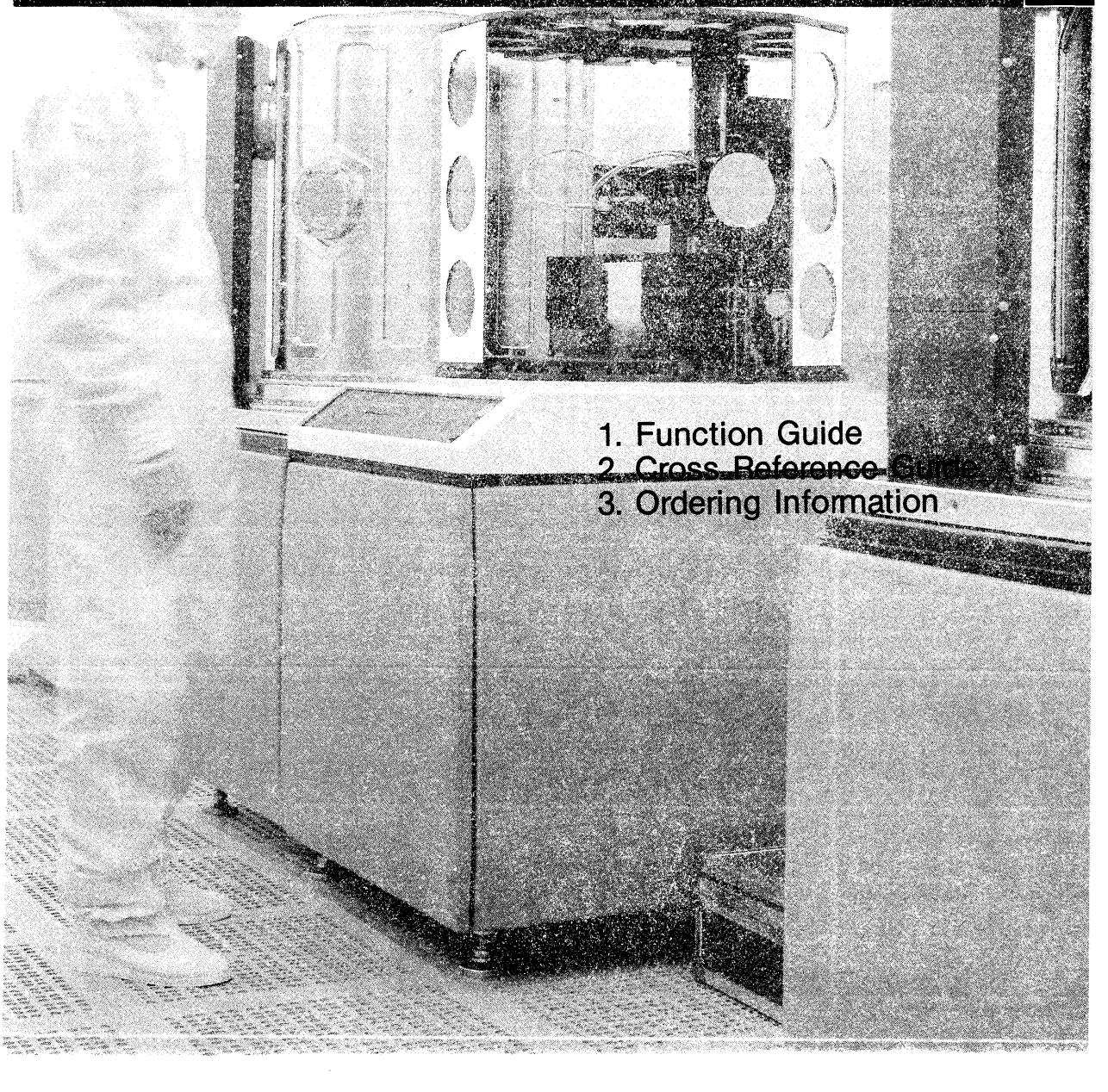
Failure Rate Elaluation

Unit: %/1000HR

Dev. x Hours at 125°C	Fail	Failure Rate at 60% Confidence Level			
		Point Estimate	85°C	70°C	55°C
1.7×10^6	2	0.18	0.0068	0.0018	0.00036

The activation energy, from analysis, was chosen as 1.0 eV based upon test results. The failure rate at the lower operating temperature can be extrapolated by an Arrhenius plot.

PRODUCT GUIDE 2



1. Function Guide
2. Cross Reference Guide
3. Ordering Information

1. TELECOMMUNICATION APPLICATION FUNCTION

Application	Type	Package	Circuit Function
•Tone Ringer	KA2410 KA2411	8 DIP	Adjustable warbling and 2 frequency tone External triggering or ringer disable (KA2410) Adjustable supply initiating current (KA2411) Built-in hysteresis
Tone Ringer with Bridge Rectifier	KA2418	8 DIP	Protect against over voltage Low current consumption Allow the parallel operation of 4 devices Built-in hysteresis External component's are minimized High output voltage
DTMF Dialer	KS5808	16 DIP	Direct telephone line operation Standard 2 of 8 key board use Tone output: Bipolar output Mute output: N-CH open drain
	††KS5809	16 DIP	Low power dissipation Single contact key board use Tone output: Bipolar output Mute output: N-CH open drain
	††KS5810	16 DIP	Low power dissipation Single contact key board use 31 digit redial (Column 4 keys) Tone output: Bipolar output Mute output: N-CH open drain
	††KS5811	16 DIP	Low power dissipation Standard 2 of 8 key board use 31 digit redial (# key) Tone output: Bipolar output Mute output: N-CH open drain
	KA2413	16 DIP	Wide operating line voltage and current range Short start up time External components are minimized Internal protection of all inputs
Pulse Dialer with Redial	KS5805A/B	18 DIP	KS5805A: Pin 2; V_{ref} KS5805B: Pin 2; Tone output RC oscillator used as frequency reference $\overline{DP}$ out, 17 digit redial
	†KS58C/D05	18 DIP	KS58C05: Pin 2; V_{ref} KS58D05: Pin 2; Tone output RC oscillator used as frequency reference $\overline{DP}$ output, 32 digit redial
	†KS58E05	16 DIP	$\overline{DP}$ output RC oscillator used as frequency reference 32 digit redial

TELECOMMUNICATION APPLICATION (Continued)

Application	Type	Package	Circuit Function
DTMF/Pulse Switchable Dialer	KS58A/B/C/D19 KS58A/B/C/D20	22 DIP 18 DIP	Tone/pulse switchable dialing, touch key or slide switch 32 digit redialing & PABX auto-pause time Make/break ratio pin selectable
DTMF/Pulse Switchable with 10 No Memory	†KS5822	22 DIP	10 No × 16 digit memory including a redial memory Including PABX auto pause time 10 pps/20 pps pin selectable Make/Break pin selectable On/Off hook memory
	†KS58A/B/C/D23	18 DIP	10 No × 16 digit memory including a redial memory Including PABX auto pause time Make/Break pin selectable
Speech Network	KA2412A	14 DIP	Transmit/Receiver amplifier Side tone control On chip regulator
Low Voltage Speech Network with Dialer Interface	KA2425A/B	18 DIP	Low Voltage Operation (1.5V) Tx, Rx & side tone gain set by external resistor Loop length equalization for Tx, Rx & sidetone Provides regulated voltage for CMOS dialer DTMF level adjustable with a single resistor A: Mute active low B: Mute active high
DTMF Receiver	†KT3170	18 DIP	Full DTMF Receiver Provides DTMF high and low group filtering Dial tone suppression Adjustabe acquisition and release times Integrated bandsplit filter and digital decoder functions High quality and performance Single +5 Volt power supply
Tone Decoder	LM567C/L	8 DIP †8 SOP	Touch tone decoding Sequential tone decoding Communication paging High stable center frequency LM567L: Micropower (4mW at 5V) dissipation
FM IF Amplifier	MC3361	16 DIP †16 SOP	Small current dissipation (Typ. 3.5mA: V_{CC} 4.0V) Excellent input sensitivity Communication paging Used to cordless telephone parts required Work from 1.8V to 7.0V
Codec	KT5116 †KT8520 ††KT8521	16 CERDIP 24 CERDIP 22 CERDIP	μ-Law: KT5116 μ-Law: KT8520 A-Law: KT8521 ±5V operation Low power consumption Synchronous or asynchronous operation

TELECOMMUNICATION APPLICATION (Continued)

Application	Type	Package	Circuit Function
Codec Filter	KT3040/A	16 CERDIP	Exceeds all D3/D4 and CCITT spec. ±5V operation Low power consumption 20dB gain adjust range Sin X/X correction in receive filter TTL and CMOS compatible logic
Combo Codec	†KT8554 †KT8557 †KT8564 ††KT8567	16 CERDIP 16 CERDIP 20 CERDIP 20 CERDIP	Exceeds all D3/D4 and CCITT spec. Complete CODEC and filtering system including ±5V operation Low power consumption TTL and CMOS compatible logic Receive push-pull power amp (KT8564/7)
TSAC	†KT8555	20 CERDIP	Controls up to 8 COMBO CODEC/Filters Low power consumption Single 5V operation Up to 32 time slots per frame
Line Driver	MC1488 ††KS5788	14 DIP †14 SOP	Conformance EIA standard No. RS-232C & V28 (CCITT) Quad line driver Interface between data terminal equipment (DTE) and data communication equipment (DCE) Current limited output: ±10mA typ. Power-off source impedance 300 ohms min. Compatible with DTL and TTL, HCTLS families Flexible operating supply range KS5788: Low power CMOS version
Line Receiver	MC1489/A ††KS5789A	14 DIP †14 SOP	Conformance EIA standard No. RS-232C & V28 (CCITT) Quad line receiver Interface between data terminal equipment (DTE) and data communication equipment (DCE) Input signal range ±30 volts Input threshold hysteresis built in Response control a) Logic threshold shifting b) Input noise filtering KS5789A: Low Power CMOS version
Line Transceiver	††KA2654	8 DIP	Conformance EIA Standard No RS-232C & V28 (CCITT) One Driver & One Receiver on chip Wide supply voltage (±4.5V-±15V) Including reference regulator Response control provides TTL compatible
	††KS5706	16 DIP 16 SOP	Conformance EIA Standard No RS-232 & V28 (CCITT) Low power consumption (CMOS) 3 Drivers & 3 Receivers one chip

TELECOMMUNICATION APPLICATION (Continued)

Application	Type	Package	Circuit Function
Peripheral Driver Array	†KA2655/6/7/8/9	16 DIP 16 SOP	Including 7 NPN darlington-connected transistors These arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. High breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads
Fluorescent Display Driver	KA2651	18 DIP	Consisting of 8 NPN darlington output stages and associated common-emitter input stages Digit or segment drivers Low input current, internal output pull-down resistor High output breakdown voltage Single or split supply operation
8-Channel Source Driver	KA2580A	18 DIP	TTL, CMOS, PMOS, NMOS compatible High output current ratings Internal transient suppression Efficient input/output pin structure Drive telephone relays, incandescent lamps, and LEDS
	KA2588A	20 DIP	KA2588A: Separated logic and driver supply line
Universal Asynchronous Receiver and Transmitter (UART)	††KS5824 KS5812	24 DIP 40 DIP	The data formatting and control to interface serial asynchronous data communications between main system and subsystems. Low power, high speed CMOS process Serial/parallel conversion of data 8 and 9 bit transmission Programmable control register Optional ÷1, ÷16, and ÷64 clock modes Peripheral/modem control functions Double buffered Included 4 UART in one chip (KS5812)

† New Product
†† Under Development

2. VOLTAGE REGULATOR

A. 3-Terminal Fixed Positive Voltage Regulator

Function	Type	Package	Features	Application
Very High Output Current (3A)	KA78T05 ††KA78TXX	TO-220 TO-3P	Output current in excess of 3A Internal thermal overload protection Internal short circuit current limiting	5V, 6V, 8V, 12V, 15V, 18V and 24V fixed output voltage
	LM323	TO-3P		5V output voltage
High Output Current (I_O = 1A)	MC78XX series	TO-220	Maximum output current 1A External components are minimized Internal protection circuit for output short Positive voltage regulator Variable application control	5V, 5.2V, 6V, 8V, 8.5V, 9V, 10V, 11V, 12V, 15V, 18V and 24V fixed output voltage
	†KA340XX series	TO-220	Output current in excess of 1A Very low line regulation: 0.01% Very low load regulation: 0.3%	5V, 6V, 8V, 9V, 10V, 11V, 12V, 15V, 18V and 24V fixed output voltage
Medium Output Current (I_O = 500mA)	MC78MXX series	TO-220	Maximum output current 500mA External components are minimized Internal protection circuit for output short Positive fixed output voltage regulator Variable application circuit	5V, 6V, 8V, 10V, 12V, 15V, 18V, 20V and 24V fixed output voltage
Low Output Current (I_O = 100mA)	MC78LXXAC series	TO-92	Output current in excess of 100mA External components minimized Internal protection circuit for output short Positive voltage regulator Variable application circuit	2.6V, 5V, 6.2V, 8V, 8.2V, 9V, 12V 15V, 18V and 24V fixed output voltage

B. 3-Terminal Fixed Negative Voltage Regulator

Function	Type	Package	Features	Application
High Output Current (I_O = 1A)	MC79XX series	TO-220	Output current in excess of 1A Internal thermal overload protection Internal short circuit current limiting	−2V, −5V, −6V, −8V, −12V, −15V, −18V and −24V fixed output
Medium Output Current (I_O = 500mA)	MC79MXX series	TO-220	Output current in excess of 500mA Internal thermal over load protection Internal short circuit current limiting	−5V, −6V, −8V, −12V, −15V, −18V and −24V fixed output voltage
Low Output Current (I_O = 100mA)	MC79L05AC ††MC79LXXAC series	TO-92	Output current in excess of 100mA Internal short circuit current limiting External components minimized	−5V, −12V, −15V, −18V and −24V fixed output voltage

† New Product
†† Under Development

C. Precision Voltage Regulator

Function	Type	Package	Features	Application
Adjustable Regulator	LM723	14 DIP 14 SOP	Positive or negative supply operation Series, shunt, switching or floating operation 0.01% line and load regulation Output current up to 150mA without external pass transistor	Output voltage adjustable from 2 to 37V
Adjustable Regulator	LM317	TO-220	Output current in excess of 1.5A Positive output adjustable from 1.2V to 37V Internal short circuit current limiting	Floating operation for high voltage operation Eliminates stocking many fixed voltages
	KA337	TO-220	Output current in excess of 1.5A Negative output adjustable from −1.2V to −37V Internal short circuit current limiting	Floating operation for high voltage operation Eliminates stocking many fixed voltages
	†KA350	TO-3P	Output current in excess of 3A Positive output adjustable from 1.2V to 33V Internal short circuit current limiting	Floating operation for high voltage operation Eliminates stocking many fixed voltages
	††KA7501	TO-92	Output current in excess of 100mA Positive output adjustable from 1.2V to 37V Internal short circuit current limiting	Floating operation for high voltage operation Eliminates stocking many fixed voltages
	††KA7502	TO-220	Output current in excess of 500mA Positive output adjustable from 1.2V to 37V Internal short circuit current limiting	Floating operation for high voltage operation Eliminates stocking many fixed voltages
	††KA7503	TO-92	Output current in excess of 100mA Negative output adjustable from −1.2V to −37V Internal short circuit current limiting	Floating operation for high voltage operation Eliminates stocking many fixed voltages
	††KA7504	TO-220	Output current in excess of 500mA Negative output adjustable from −1.2V to 37V Internal short circuit current limiting	Floating operation for high voltage operation Eliminates stocking many fixed voltages

† New Product
†† Under Development

D. Switching Voltage Regulator

Function	Type	Package	Features	Application
Adjustable 1.25V to 40V	KA78S40	16 DIP 16 SOP	Peak output current of 1.5A without external transistor. 80dB line and load regulation Operation from 25V to 40V	Step-down converter Step-up converter Inverter
Voltage Mode PWM Control IC	KA3524	16 DIP	Complete PWM power control circuitry Internal short circuit current limiting Complementary output Output current up to 100mA	Flyback converter Voltage inverter Voltage step-down Voltage step-up
	KA7500	16 DIP	Complete PWM power control circuitry Dead-time control Complementary output Output current up to 200mA	Voltage inverter Voltage step-down Voltage step-up
	KA7506	16 DIP	Adjustable dead-time control Internal soft-start Separate oscillator sync terminal Pulse-by-pulse shutdown Input undervoltage lockout with hysteresis	Flyback coverter Voltage inverter Voltage step-down Voltage step-up
Current Mode PWM Control IC	KA7505	8 DIP	Automatic feed forward compensation Pulse-by-pulse current limiting Undervoltage lockout with hysteresis Double pulse suppression High current totem pole output	Flyback converter Voltage inverter Voltage step-down Voltage step-up
DC to DC Converter	KA7507	8 DIP	Low standby current Current Limiting Output switch current of 1.5A Output voltage adjustable from 1.25 to 40V	Voltage inverter Voltage step-down Voltage step-up

3. VOLTAGE REFERENCE

Function	Type	Package	Features	Application
Adjustable Reference	KA431	TO-92 8 DIP 8 SOP	Programmable output voltage from V_{ref} to 36V Voltage reference tolerance: ±1.0% Low output noise voltage	Switching regulator Constant current source Constant current sink
Reference	KA336	TO-92	Adjustable 4V to 6V Low temperature coefficient 0.6Ω dynamic impedance Fast turn-on	Adjustable shunt regulator Precision power regulator
33V Reference	KA33V	TO-92	Low temperature coefficient Low dynamic resistance	Electronic tuning system

4. OPERATIONAL AMPLIFIER

Function	Type	Package	Features	Application
OP AMP	LM741	8 DIP 8 SOP	Internal frequency compensation Short circuit protection	Comparator, DC amp, Multivibrator, Summing amp, Integrator or differentiator, Narrow band or BPF
	LM301A	8 DIP 8 SOP	Short circuit protection External frequency compensation	Variable capacitance Multiplier Sine wave oscillator
	KF351	8 DIP 8 SOP	Internally trimmed offset Voltage: 10mV Low input bias current High input impedance: $10^{12}\Omega$ High slew rate: 13V/μs Wide gain bandwidth: 4MHz	Hi-Zin inverting amp Ultra low duty cycle pulse generator sample and Hold
Dual OP AMP	MC4558	8 DIP 8 SOP 9 SIP	Internal frequency compensation Low noise operation	Phone pre-amplifier Tape playback amplifier
	MC1458	8 DIP 8 SOP 9 SIP	Internal frequency compensation Short circuit protection	Filter Schmitt trigger Comparator Multivibrator
	LM358/A LM258/A LM2904	8 DIP 8 SOP 9 SIP	Internal frequency compensation for unit gain Large DC voltage gain Wide power supply range	DC summing amplifier Power amplification RC active bandpass filter Compatible with all forms of logic.
	††KA3000	8 DIP 8 SOP 9 SIP	Low input noise voltage High gain bandwidth: 10MHz High slew rate: 10V/μs Large supply voltage range: ± 3 to ± 20V	DC Amp Telephone channel amplifiers Audio equipment
	KA9256	10 SIP H/S	Internal current limiting: $I_{SC} = 350$mA Internal frequency compensation Minimal cross over distortion	High power amplifier CD motor driver
	†KF442	8 DIP 8 SOP 9 SIP	Low supply current: 500μA (max) Low input bias current High input impedance High gain bandwidth: 1MHz High slew rate: 1V/μs	Active filter DC summing amplifier Oscillator
	KS272	8 DIP	Wide range of supply voltage : 3V ~ 16V Common mode input voltage including the negative rail	Battery-powered application Active filter Signal buffer

†† Under Development
† New Product

OPERATIONAL AMPLIFIER (Continued)

Function	Type	Package	Features	Application
Quad OP AMP	LM324/A LM224/A LM2902	14 DIP 14 SOP	Internal frequency compensation Wide supply voltage range Single supply: DC 3V ~ 32V Dual supply: DC ± 1.5V ~ ± 16V	Audio power booster DC amp, Multivibrator Switch, Comparator Schmitt trigger
	LM348 LM248	14 DIP 14 SOP	Each amplifier is functionally equivalent to the LM741C Pin compatible with LM324 Short circuit protection	Comparator with hysteresis Voltage reference
	MC3403 MC3303	14 DIP 14 SOP	Class AB output stage for minimal crossover distortion Single or split supply operation Internal frequency compensation	Comparator with hysteresis BI-Quad filter
	†KF347	14 DIP 14 SOP	Low bias current Wide gain bandwidth: 4MHz High slew rate: 13V/μs High input impedance	D/A converter Sample and hold Integrator
	KS274	14 DIP	Wide range of supply voltage : 3V ~ 16V Single supply operation Very low input bias current, Typ 1pA	Battery-powered application Energy-conserving application
	††KA3001	14 DIP 14 SOP	Low supply current: 200μA Single supply operation: 5V to 30V Low input offset voltage	Remote line filters DC Amps Battery powered application

†New Product
†† Under Development

5. VOLTAGE COMPARATOR

Function	Type	Package	Features	Application
Single Comparator	LM311	8 DIP 8 SOP	Operates from single 5V supply Maximum input current: 250nA Maximum offset current: 50nA Differential input voltage range: ± 30V	Multivibrator output is compatible with DTL and as well as MOS circuits voltage controlled oscillator
	KA710C	14 DIP	Low offset and thermal drift Compatible with practically all types of integrated logic	Line receiver A/D converter Memory sense amplifier
Dual Comparator	LM393/A LM2903 LM293/A	8 DIP 8 SOP 9 SIP	High precision comparators Reduced V_{OS} drift over temperature Eliminates need for dual supply Allows sensing near ground Compatible with all form of logic Power drain suitable for battery operation Low input biasing current: 25nA Low output saturation voltage 250mA at 4mA	Output voltage compatible with TTL, DTL, ECL and CMOS logic system Basic comparator Pulse generator MOS clock driver
	LM319 LM219	14 DIP	Two independent comparators Operates from a single 5V High common mode slew rate	Relay driver Window detector
	KA711C	14 DIP 14 SOP	Separate differential input and single output Strobing each side	Sense amplifier for core memory Dual comparator with ORed output Double-ended limit detector
Quad Comparator	LM339/A LM2901 LM239/A LM3302	14 DIP 14 SOP	Wide single supply voltage range or dual supplies Very low supply current drain (0.8mA)-independent of supply voltage (2mW/Comparator at +5V DC) Low input biasing current: 25nA Input common-mode voltage range included GND Low output saturation voltage 250mV at 4mA	Compatible with all forms of logic Bi-stable multivibrator One-shot multivibrator Time delay generator Square wave oscillator Pulse generator Limit comparator Crystal controlled oscillator

†† Under Development

6. TIMER

Function	Type	Package	Features	Application
Single Timer	NE555	8 DIP 8 SOP	Maximum operating frequency: 500KHz Adjustable duty cycle	Precision timing Pulse generator
	KS555 KS555H	8 DIP 8 SOP	Low power consumption by using CMOS process High speed operation Wide operation supply voltage: 2 to 18 volts Pin compatible with NE555	Precision timing Pulse generator
Dual Timer	NE556	14 DIP 14 SOP	TTL Compatible Dual NE555	Time delay generation
	KS556	14 DIP 14 SOP	Low power consumption by using CMOS process Pin compatible with NE556	Time delay generation
Quad Timer	NE558	16 DIP	Wide supply voltage range: 4.5 to 16V 100mA output current per section Time period equal RC	Quad monostable Sequential timing Precision timing

7. MISCELLANEOUS ICs

Function	Type	Package	Features	Application
Voltage to Frequency Converter	††KA331	8 DIP	V-F Conversion F-V Conversion Wide range of full scale frequency: 1Hz to 100KHz	Light intensity to frequency converter Temperature to frequency converter
Earth Leakage Detector	KA2803	8 DIP	Low power consumption Built-in voltage regulator 1mA output current pulse to trigger SCR's	Earth leakage detector
Zero Voltage Switch	KA2804	8 DIP	Very few external compontents Reference voltage output Supply voltage control	On-Off temperature control Time proportional temperature control
Earth Leakage	KA2807	8 DIP	Full advantage of the UL943 Direct interface to SCR Trim time in normal	Earth leakage detector
Video Amplifier	KA733C	14 DIP	120MHz bandwidth Selectable gains of 10000 and 400 No frequency compansation required	Video recorder systems Video amplifier Pulse amplifier in communications Magnetic memories

1. TELECOMMUNICATION ICs

A. Dialer

Application	SAMSUNG	MOSTEK	AMI	UMC	SHARP	Others
Pulse Dialer	KS5805A KS5805B †KS58C05 †KS58D05 †KS58E05	*MK50992 *MK50993 MK50981 MK50982 MK50991/2	S2560A/B	*T40992 *T40993 UM9151 UM9151-3	*LR40992 *LR40993	
DTMF Dialer	KS5808 ††KS5809 ††KS5810 ††KS5811 KA2413	*MK5089 MK5087 MK5380	*S25089	*UM95089 UM95087 UM9559	*LR4089 LR4087	*SBA5089 SBA5091 SBA5099 *PBD3535
DTMF/Pulse Switchable with Redial	KS5819 KS5820	MK5370		*UM91230 *UM91210	LR48081 LR48082	*S7230A/B S7235 *LC7360
DTMF/Pulse Switchable with 10 No. Memory	†KS5822 †KS5823	MK5375/6		*UM91261 *UM91260	LR4803	PCD3315

B. Tone Ringer

Application	SAMSUNG	MOTOROLA	SGS	MITEL	CHERRY	Others
Tone Ringer	KA2410 KA2411			*ML8204 *ML8205	*CS8204 *CS8205	*TA31001 *TA31002
1 Chip Tone Ringer	KA2418	MC34012 MC34017	*LS1240 LS3240			Included Bridge Diode

C. Speech Network

Application	SAMSUNG	SGS	RIFA	ITT	ERSO	Others
Subset Amplifier	KA2412A	*LS285/A	PBL3726	TEA1045	*CIC9185	
Speech Network with Dialer Interface	KA2425A KA2425B	LS356	PBL3781			U4053/7 U4055/6 TP5700

D. Tone Decoder

Application	SAMSUNG	NATIONAL	SHARP	SIGNETICS	Others
Tone Decoder	LM567C	*LM567	*IR3N05	*NE567	*XR567 (EXAR)
	LM567L				*XRL567 (EXAR)

E. FM IF Amplifier

Application	SAMSUNG	MOTOROLA	SHARP	SPRAGUE	Others
FM IF Amplifier	MC3361	*MC3361	IR3N06	ULN3859	*LM3361

F. DTMF Receiver

Application	SAMSUNG	MITEL	GTE	Others
DTMF Receiver	†KT3170	*MT8870	*G8870	

† New Product †† Under Development * Direct Replacement

G. CODEC, CODEC FILTER, COMBO CODEC

Application	SAMSUNG	N.S	FAIRCHILD	SGS	INTEL	MOTOROLA	THOMSON
μ-Law CODEC	KT5116	*TP5116	*μA5116	*M5116	2910		
CODEC FILTER	KT3040	*TP3040	*μA5912	*M5912	*2912		*ETC5040
μ-Law COMBO CODEC	†KT8564	*TP3064			2913	MC14400-5	*ETC5064
μ-Law COMBO CODEC	†KT8554	*TP3054	*μA3054		*2916		*ETC5054
A-Law COMBO CODEC	††KT8567	*TP3067					*ETC5067
A-Law COMBO CODEC	†KT8557	*TP3057	*μA3057		*2917		*ETC5057
μ-Law DODEC	†KT8520	*TP3020	μA5151		*2910		
A-Law CODEC	††KT8521	*TP3021			*2911		
TSAC	†KT8555	*TP3155					

H. INTERFACES

Application		SAMSUNG	MOTOROLA	TI	N/S	FAIRCHILD	SIGNETICS
RS-232C	Line Driver	††KS5788			*DS14C88		
		MC1488	*MC1488	*SN75188	*DS1488	*μA1488	*MC1488
	Line Receiver	MC1489	*MC1489	*SN75189	*DS1489	*μA1489	*MC1489
		MC1489A	*MC1489A	*SN75189A	*DS1489A	*μA1489A	*MC1489A
		††KS5789A			*DS14C89A		
	Transceiver	††KA2654		*SN751701			
		††KS5706	*MC145406				

I. Driver

Application	SAMSUNG	SPRAGUE	EXAR	MOTOROLA	TI	Others
8ch Source Driver	KA2580A	*UDN2580A				
	KA2588A	*UDN2588A				
Flouscent Display Driver	KA2651	*UDN6118	*XR6118			
Peripheral Driver Array	†KA2655	*ULN2001		*MC1411	SN75476	
	†KA2656	*ULN2002		*MC1412	SN75477	
	†KA2657	*ULN2003		*MC1413	SN75478	
	†KA2658	*ULN2004		*MC1416		
	†KA2659	*ULN2005				

J. UART

Application	SAMSUNG	HITACHI	MOTOROLA	Others
Single UART	††KS5824	*HD6350	*MC6850	
Quad UART	KS5812			

† New Product †† Under Development * Direct Replacement

2. VOLTAGE REGULATOR

A. 3-Terminal Fixed Positive Voltage Regulator

Description	SAMSUNG	MOTOROLA	FAIRCHILD	NEC	MATSUSHITA	Package
KA78TXX Series (I_O = 3A)	KA78T05 ††KA78T06 ††KA78T08 ††KA78T12 ††KA78T15 ††KA78T18 ††KA78T24	MC78T05 MC78T06 MC78T08 MC78T12 MC78T15 MC78T18 MC78T24				TO-220 TO-3P
LM323 (I_O = 3A)	LM323	LM323				TO-3P
MC78XXAC/C Series (I_O = 1A)	MC7805AC/C MC7852C MC7806AC/C MC7808AC/C MC7885AC/C MC7809AC/C MC7810AC/C MC7811AC/C MC7812AC/C MC7815AC/C MC7818AC/C MC7824AC/C	MC7805AC/C MC7806AC/C MC7808AC/C MC7812AC/C MC7815AC/C MC7818AC/C MC7824AC/C	μA7805 μA7806 μA7808 μA7885 μA7812 μA7815 μA7818 μA7824	μPC7805 μPC7808 μPC7812 μPC7815 μPC7818 μPC7824	AN7805 AN7806 AN7808 AN7812 AN7815 AN7818 AN7824	TO-220
KA340XX Series (I_O = 1A)	†KA340T05 †KA340T06 †KA340T08 †KA340T09 †KA340T10 †KA340T11 †KA340T12 †KA340T15 †KA340T18 †KA340T24	LM340-5.0 LM340-6.0 LM340-8.0 LM340-12 LM340-15 LM340-18 LM340-24				TO-220
MC78MXXC Series (I_O = 0.5A)	MC78M05C MC78M06C MC78M08C MC78M10C MC78M12C MC78M15C MC78M18C MC78M20C MC78M24C	MC78M05C MC78M06C MC78M08C MC78M12C MC78M15C MC78M18C MC78M20C MC78M24C	μA78M05C μA78M06C μA78M08C μA78M12C μA78M15C μA78M20C μA78M24C	μPC78M05 μPC78M08 μPC78M10 μPC78M12 μPC78M15 μPC78M18 μPC78M20 μPC78M24	AN78M05 AN78M06 AN78M08 AN78M10 AN78M12 AN78M15 AN78M18 AN78M20 AN78M24	TO-220
MC78LXXAC (I_O = 0.1A)	MC78L26AC MC78L05AC MC78L62AC MC78L08AC MC78L82AC MC78L09AC MC78L12AC MC78L15AC MC78L18AC MC78L24AC	 MC78L05AC MC78L08AC MC78L12AC MC78L15AC MC78L18AC MC78L24AC	 μA78L05AC μA78L62AC μA78L82AC μA78L09AC μA78L12AC μA78L15AC			TO-92

† New Product
†† Under Development

B. 3-Terminal Fixed Negative Voltage Regulator

Description	SAMSUNG	MOTOROLA	FAIRCHILD	NEC	MATSUSHITA	Package
MC79XXC Series (I_O = 1A)	MC7902C MC7905C MC7906C MC7908C MC7912C MC7915C MC7918C MC7924C	 MC7905C MC7906C MC7908C MC7912C MC7915C MC7918C MC7924C	 μA7905 μA7908 μA7912 μA7915	 μPC7905 μPC7908 μPC7912 μPC7915 μPC7918 μPC7924	 AN7905 AN7906 AN7908 AN7912 AN7915 AN7918 AN7924	
MC79MXXC (I_O = 0.5A)	MC79M05C MC79M06C MC79M08C MC79M12C MC79M15C MC79M18C MC79M24C	MC79M05C MC79M12 MC79M15	μA79M05 μA79M08 μA79M12 μA79M15			TO-220
MC79LXXAC (I_O = 0.1A)	MC79L05AC ††MC79L12AC ††MC79L15AC ††MC79L18AC ††MC79L24AC	MC79L05AC MC79L12AC MC79L15AC MC79L18AC MC79L24AC				TO-92

C. Precision Voltage Regulator

Description	SAMSUNG	MOTOROLA	FAIRCHILD	NEC	MATSUSHITA	Package
Adjustable Voltage	LM723	MC1723	μA723	LM723		14 DIP/14 SOP
	LM317	LM317	μA317	LM317		TO-220
	KA337	LM337		LM337		TO-220
33V Regulator	KA33V				μPC574	TO-92
Adjustable Voltage	†KA350 ††LM317L ††LM317M ††KA337L ††KA337M	LM350 LM317L LM317M LM337L LM337M	μA350	LM350 LM317M LM337M		

D. Switching Voltage Regulator

Description	SAMSUNG	MOTOROLA	FAIRCHILD	NEC	MATSUSHITA	Package
Adjustable 1.25V to 40V (f_O = 100KHz)	KA78S40	μA78S40	μA78S40			16 DIP
PWM Controller IC	KA3524	SG3524		LM3524	SG3524	16 DIP
	**KA7500	TL494			TL494	16 DIP

3. PRECISION VOLTAGE REFERENCE

Description		SAMSUNG	MOTOROLA	FAIRCHILD	N/S	TI	Package
Adjustable Reference (2.5V ~ 36V)		KA431	TL431	μA431		TL431	TO-92 8 DIP 8 SOP
Reference	5V	KA336			LM336		TO-92
	2.5V	KA336			LM336		TO-92

4. OPERATIONAL AMPLIFIER

Description	SAMSUNG	MOTOROLA	NATIONAL	FAIRCHILD	JRC	Others
Single OP Amp	LM741 KA301 KF351	MC1741 LM301 LF351	LM741 LM301 LF351	μA741 μA301	NJM741	μPC301A TL081
Dual OP Amp	LM358/A LM258/A LM2904 MC1458 MC4558 KA9256 †KF442 ††KA3000	LM358/A LM258 LM2904 MC1458 MC4558	LM358/A LM258/A LM2904 LM1458 LF442	 μA1458 μA4558	NJM358 NJM2904 NJM458 NJM4558 NJM4558	TA75358 BA4558 TA7256 TLC272, ICL7621
Quad OP Amp	LM324/A LM224/A LM2902 LM348 LM248 MC3403 MC3303 †KF347 KS274 ††KA3001	LM324/A LM224 LM2902 LM348 LM248 LM3403 MC3303 LF347	LM324/A LM224/A LM2902 LM348 LM248 LF347	μA324 μA224 μA2902 μA348 μA248 μA3403 μA3303	NJM324 NJM2902 NJM340J	TA75324 CA224 μPC451 μPC3403 μPC452 TLC274, ICL7641 OP-420

5. VOLTAGE COMPARATOR

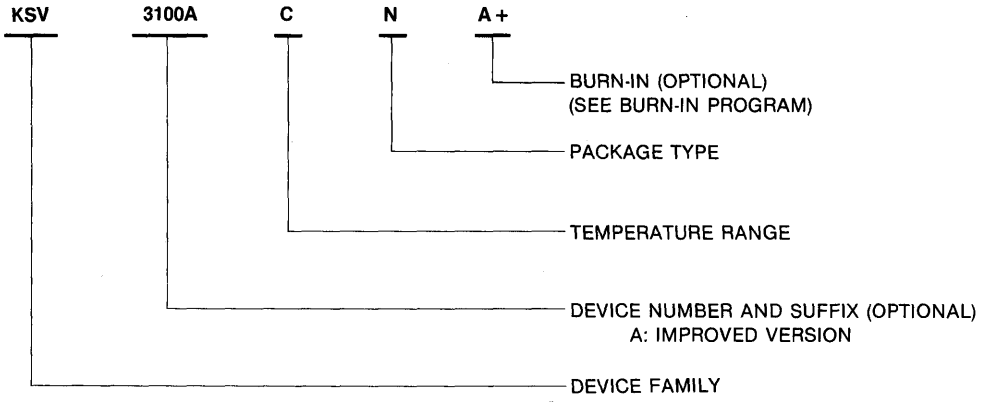
Description	SAMSUNG	MOTOROLA	NATIONAL	FAIRCHILD	JRC	Others
Single Comparator	LM311 KA710C	LM311 MC710C	LM311 LM710	LM311 μA710	NJM311	μPC311 MB4001
Dual Comparator	LM393/A LM2903 LM293 KA319 KA219 KA711C	LM393/A LM2903 LM293	LM393/A LM2903 LM293 LM319 LM219 LM711	μA393 μA711C	 NJM2903 NJM2903 NJM319	TA75393 μPC277
Quad Comparator	LM339/A LM2901 LM239 LM3302	LM339/A LM2901 LM239	LM339/A LM2901 LM239 LM3302	μA339 μA2901 μA239 μA3302	 NJM2901	TA75339 μPC177 CA239 CA3302

6. TIMER

Function	SAMSUNG	MOTOROLA	NATIONAL	SIGNETICS	TI	Others
Single Timer	NE555 KS555 KS5357	MC1455	LM555	NE555	TA75555 TLC555	ICM7555
Dual Timer	NE556 KS556		LM556	NE556	NE555 TLC556	ICM7556
Quad Timer	NE558			NE558		

7. MISCELLANEOUS ICs

Function	SAMSUNG	TOSHIBA	NATIONAL	MATSUSHITA	NEC	Others
Toy Radio Control Actuator	KA2303					3 Function
	KA2304					2 Function
	†KA2309	TA7657D			Turbo +	7 Function (RX)
	†KA2310	TA7330			Turbo +	7 Function (TX)
DC Motor Speed Controller	KA2401				μPC1470H	
	KA2402			AN6612		*LA5521D
	KA2404			AN6610		μPC1470H
	†KA2407			*AN6651		
Earth Leakage Detector	KA2803		LM1851			*M54123
Earth Leakage Detector	KA2807		LM1851			
Zero Voltage SW	KA2804				μPC1701C	
FDD Read AMP	KA6201					*HA16631P
Smoke Detector	KS3502					S566
Conventional Timer	KS8701	TD6347S				
Flasher Controller	KA8702	TA8027P				UAA1041
V/F Converter	KA331		LM331			



TEMPERATURE RANGE

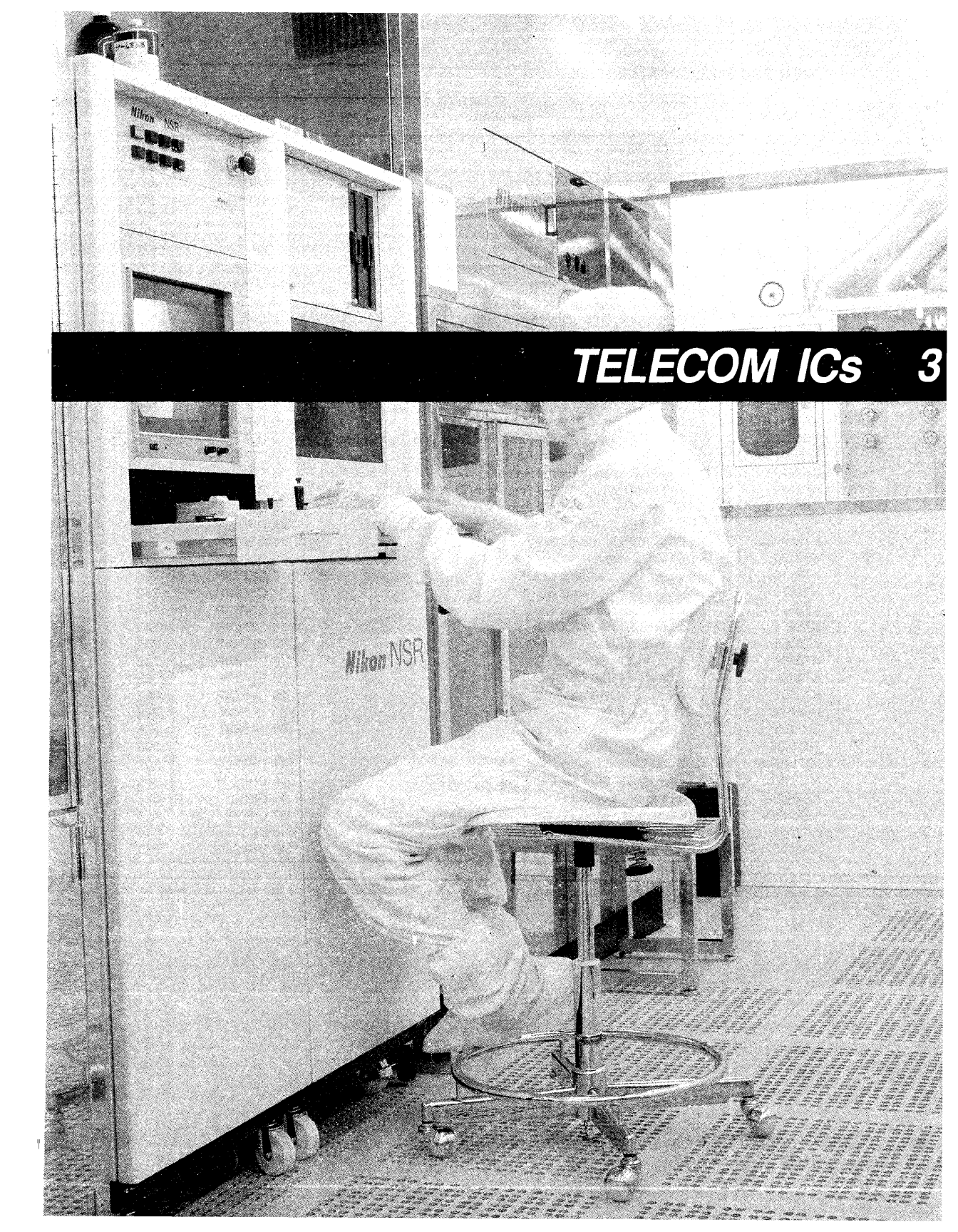
BLANK	SEE INDIVIDUAL SPEC
C	COMMERCIAL 0 ~ +70°C
I	INDUSTRIAL −25 ~ +85°C −40 ~ +85°C
M	MILITARY −55 ~ +125°C

INTEGRATED CIRCUIT

KA	LINEAR IC
KS	CMOS IC
KT	TELECOM IC
LM	NATIONAL
MC	MOTOROLA
NE	SIGNETICS
KSV	A/D-D/A CONVERTER
KAD	A/D CONVERTER
KDA	D/A CONVERTER

PACKAGE TYPE

CODE	PKG. TYPE
D	SOIC
J	CERAMIC DIP
N	PLASTIC DIP (300/600 mil)
S	SIP
Q	FQP
E	SD (400 mil)
B	SSD (Skinny Shrink DIP) (400 mil. Small Pitch)
P	SHD (Shrink DIP) (300 mil. Small Pitch)
W	ZIP
U	PGA
L	LCC
PL	PLCC
M	TO-3
H	TO-3P
Z	TO-92
V	TO-92L
A	TO-126
T	TO-220
X	TO-247
G	BARE CHIP



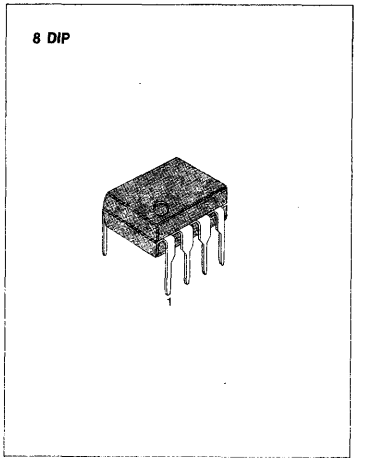
TELECOM ICs 3

Telecommunication Application

Device	Function	Package	Page
KA2410	Tone Ringer	8 DIP	81
KA2411	Tone Ringer	8 DIP	81
KA2412A	Telephone Speech Circuits	14 DIP	87
KA2413	Dual Tone Multi Frequency Generator	16 DIP	95
KA2418	Tone Ringer with Bridge Diode	8 DIP	101
KA2425A/B	Telephone Speech Network with Dialer Interface	18 DIP	104
KA2654	Line Transceiver	8 DIP	111
KS5706	3 Line Drivers and 3 Line Receivers	16 DIP/SOP	115
KS5788	Quad CMOS Line Driver	14 DIP/SOP	119
KS5789A	Quad CMOS Line Receiver	14 DIP/SOP	122
KS5805A/B	Telephone Pulse Dialer with Redial	18 DIP	125
KS58C/D05	Telephone Pulse Dialer with Redial	18 DIP	131
KS58E05	Telephone Pulse Dialer with Redial	16 DIP	136
KS5808	Dual Tone Multi Frequency Dialer	16 DIP	140
KS5809	DTMF Dialer	16 DIP	146
KS5810	DTMF Dialer with Redial	16 DIP	146
KS5811	DTMF Dialer with Redial	16 DIP	146
KS5812	Quad Universial Asychronos Receiver and Transmitter	40 DIP	150
KS58A/B/C/D19	Tone/Pulse Dialer with Redial	22 DIP	160
KS58A/B/C/D20	Tone/Pulse Dialer with Redial	18 DIP	170
KS5822	10 Memory Tone/Pulse Repertory Dialer	22 DIP	178
KS58A/B/C/D23	10 Memory Tone/Pulse Repertory Dialer	18 DIP	186
KS5824	Universial Asychronous Receiver and Transmitter	24 DIP	194
KT3040/A	PCM Monolithic Filter	16 CERDIP	205
KT3170	DTMF Receiver	18 DIP	217
KT5116	μ-Law Companding CODEC	16 CERDIP	227
KT8520	μ-Law Companding CODEC	24 CERDIP	240
KT8521	A-Law Companding CODEC	22 CERDIP	240
KT8554	μ-Law COMBO CODEC	16 CERDIP	249
KT8555	Time Slot Assignment Circuit	20 CERDIP	260
KT8557	A-Law COMBO CODEC	16 CERDIP	249
KT8564	μ-Law COMBO CODEC	20 CERDIP	268
KT8567	A-Law COMBO CODEC	20 CERDIP	268
LM567C	Tone Decoder	8 DIP/SOP	278
LM567L	Micropower Tone Decoder	8 DIP/SOP	286
MC1488	Quad Line Driver	14 DIP/SOP	296
MC1489/A	Quad Line Receiver	14 DIP/SOP	301
MC3361	Low Power Narrow Band FM IF	16 DIP/SOP	305
KA2580A	8-Channel Source Drivers	18 DIP	611
KA2588A	8-Channel Source Drivers	20 DIP	611
KA2651	Fluorescent Display Drivers	18 DIP	616
KA2655/6/7/8/9	High Voltage, High Current Darlingtor Arrays	16 DIP/SOP	619

TONE RINGER

The KA2410/KA2411 is a bipolar integrated circuit designed for telephone bell replacement.



FUNCTIONS

- Two oscillators
- Output amplifier
- Power supply control circuit

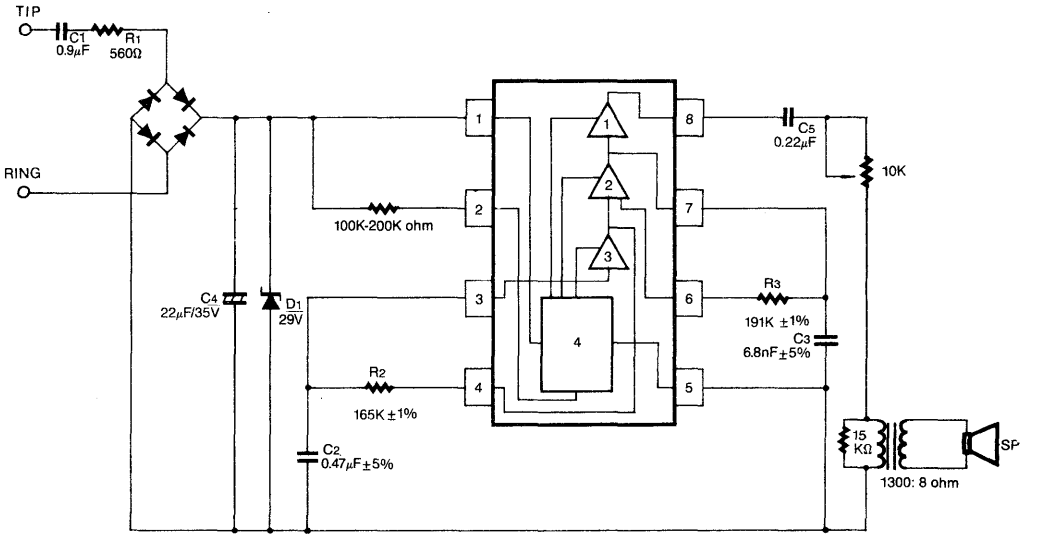
FEATURES

- **Designed for telephone bell replacement**
- **Low current drain.**
- **Small size 'MINIDIP' package.**
- **Adjustable 2-frequency tone.**
- **Adjustable warbling rate.**
- **Built-in hysteresis prevents false triggering and rotary dial 'CHIRPS'**
- **Extension tone ringer modules**
- **Alarms or other alerting devices.**
- **External triggering or ringer disable (KA2410).**
- **Adjustable for reduced supply initiation current (KA2411)**

ORDERING INFORMATION

Device	Operating Temperature
KA2410N	−45 ~ +65°C
KA2411N	

APPLICATION CIRCUIT 1 (KA2410)



Note: 1. Output amplifier
2. High frequency oscillator
3. Low frequency oscillator
4. Hysteresis regulator

Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	30	V
Power Dissipation	P_D	400	mW
Operating Temperature	T_{opr}	−45 to 65	°C
Storage Temperature	T_{stg}	−65 to 150	°C

ELECTRICAL CHARACTERISTICS (T_a =25°C)

(All voltage referenced to GND unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}				29.0	V
Initiation Supply Voltage[1]	V_{SI}	See Fig. 2	17	19	21	V
Initiation Supply Current[1]	I_{SI}	KA2411-6.8K-Pin 2 to GND	1.4	2.5	4.2	mA
Sustaining Voltage[2]	V_{SUS}	See Fig. 2	9.7	11.0	12.0	V
Sustaining Current[2]	I_{SUS}	No Load V_{CC}=V_{SUS}, See Fig. 2	0.7	1.4	2.5	mA
Trigger Voltage[3]	V_{TR}	KA2410 Only V_{CC}=15V	9.0	10.5	12.0	V
Trigger Current[3]	I_{TR}	KA2410 Only		20.0	1000[5]	μA
Disable Voltage[4]	V_{DIS}	KA2410 Only			0.5	V
Disable Current[4]	I_{DIS}	KA2410 Only	−40	−50		μA
Output Voltage High	V_{OH}	V_{CC}=21V, I_s=−15mA Pin 6=6V, Pin 7=GND	17.0	19.0	21.0	V
Output Voltage Low	V_{O1}	V_{CC}=21V, I_s=15mA Pin 6=GND, Pin 7=6V			1.6	V
I_{IN} (Pin 3) I_{IN} (Pin 7)		Pin 3=6V, Pin 4=GND Pin 7=6V, Pin 6=GND	— —	— —	500 500	nA nA
High Frequency 1 High Frequency 2 Low Frequency	f_{H1} f_{H2} f_L	R_3=191K, C_3=6800pF R_3=191K, C_3=6800pF R_2=165K, C_2=0.47μF	461 576 9.0	512 640 10	563 704 11.0	Hz Hz Hz

• NOTE (see electrical characteristics sheet)

1. Initiation supply voltage (V_{SI}) is the supply voltage required to start the tone ringer oscillating.
2. Sustaining voltage (Vsus) is the supply voltage required to maintain oscillation.
3. V_{TR} and I_{TR} are the conditions applied to trigger in to start oscillation for $V_{SUS} \leqq V_{CC} \leqq V_{SI}$
4. V_{DIS} and I_{DIS} are the conditions applied to trigger in to inhibit oscillation for $V_{SI} \leqq V_{CC}$
5. Trigger current must be limited to this value externally.

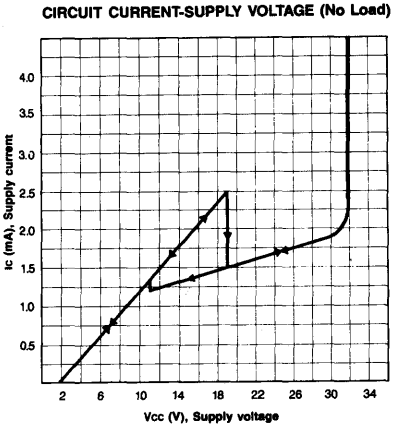


Fig. 2

APPLICATION NOTE

The application circuit illustrates the use of the KA2410/KA2411 devices in typical telephone or extension tone ringer application.

The AC ringer signal voltage appears across the TIP and RING inputs of the circuit and is attenuated by capacitor C_1 and resistor R_1.

C_1 also provides isolation from DC voltages (48V) on the exchange line.

After full wave rectification by the bridge diode, the waveform is filtered by capacitor C_4 to provide a DC supply for the tone ringer chip.

As this voltage exceeds the initiation voltage (V_{SI}),oscillation starts.

With the components shown, the output frequency chops between 512 (f_{h1}) and 640Hz (f_{h2}) at a 10Hz (f_L) rate.

The loudspeaker load is coupled through a 1300Ω to 8Ω transformer.

The output coupling capacitor C_5 is required with transformer coupled loads.

When driving a piezo-ceramic transducer type load, the coupling C_5 and transformer (1300Ω: 8Ω) are not required. However, a current limiting resistor is required.

The low frequency oscillator oscillates at a rate (f_L) controlled by an external resistor (R_2) and capacitor (C_2).

The frequency can be determined using the relation $f_L = 1/1.289\ R_2.\ C_2$. The high frequency oscillates at a f_{H1}, f_{H2} controlled by an external resistor (R_3) and capacitor (C_3). The frequency can be determined using the relation $f_{HI} = 1/1.504\ R_3.\ C_3$. $f_{H2} = 1/1.203\ R_3,\ C_3$.

Pin 2 of the KA2411 allows connection of an external resistor R_{SL}, which is used to program the slope of the supply current vs supply voltage characteristics (see Fig 4), and hence the supply current up to the initiation voltage (Vsi). This initiation voltage remains constant independent of R_{SL}.

The supply current drawn prior to triggering varies inversely with R_{SL}. decreasing for increasing value of resistance. Thus, increasing the value of R_{SL}, will decrease the amount of AC ringing current required to trigger the device. As such, longer sucribser loops are possible since less voltage is dropped per unit length of loop wire due to the lower current level. R_{SL} can also be used to compensated for smaller AC coupling capacitors (C_5 on Fig 3) (higher impedance) to the line which can be used to alter the ringer equivalence number of a tone ringer circuit.

The graph in Fig. 4 illustrates the variation of supply current with supply voltage of the KA2411. Three curves are drawn to show the variation of initiation current with R_{SL}. Curve B ($R_{SL} \mp 6.8K$) shows the I-V characteristic for the KA2411 tone ringer. Curve A is a plot with $R_{SL} < 6.8K\Omega$ and shows an increase in the current drawn up to the initiation voltage Vsi. The I-V characteristic after initiation remains unchanged. Curve C illurates the effect of increasing RSL above 6.8K Initiation current decreases but again current after triggering is unchanged.

APPLICATION CIRCUIT 2 (KA2411)

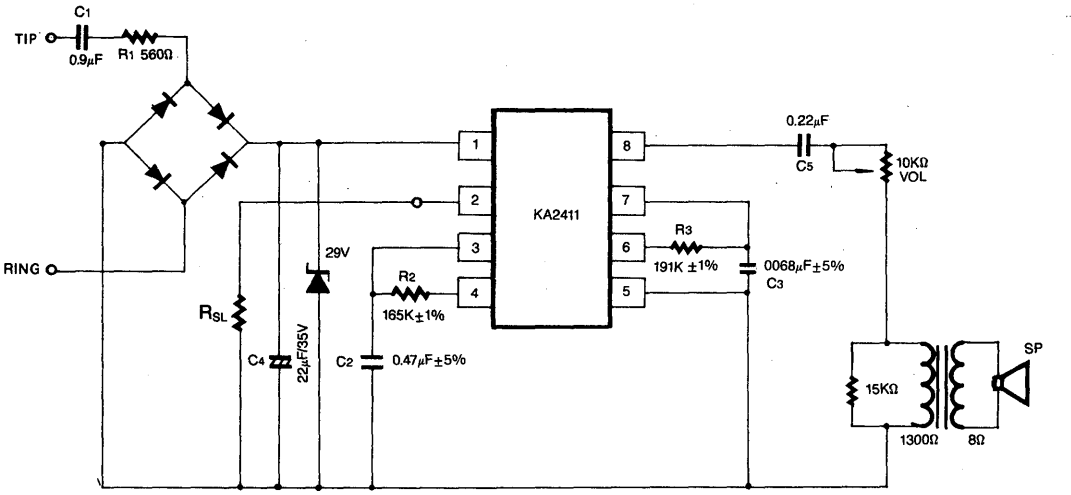


Fig. 3

LINEAR INTEGRATED CIRCUIT

KA2411 Supply Current (No Load) Vs. Supply Voltage

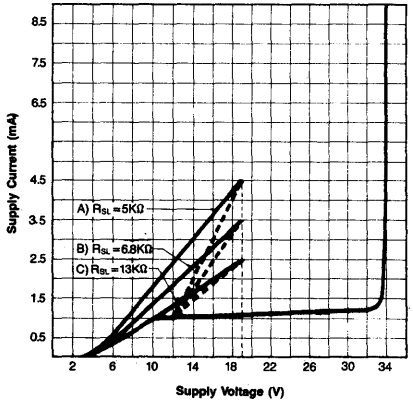


Fig. 4

EQUIVALENT CIRCUIT (Pin 2 Input)

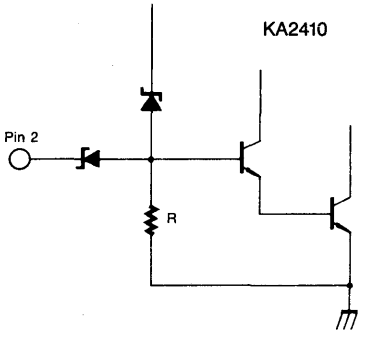


Fig. 5

INHIBITING OSCILLATION

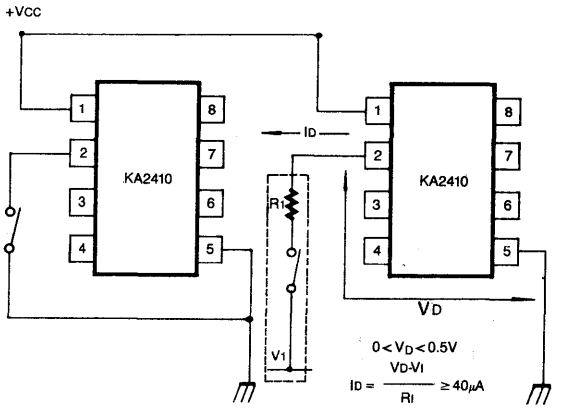


Fig. 6

PROGRAMMING THE KA2410 INITIATION SUPPLY VOLTAGE

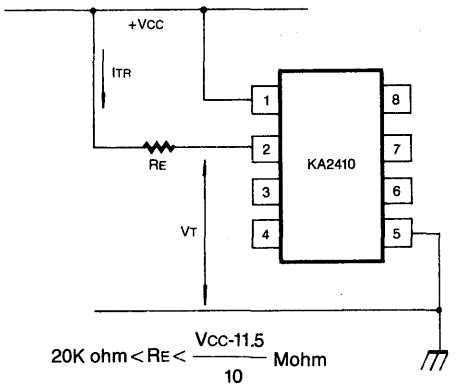


Fig. 7

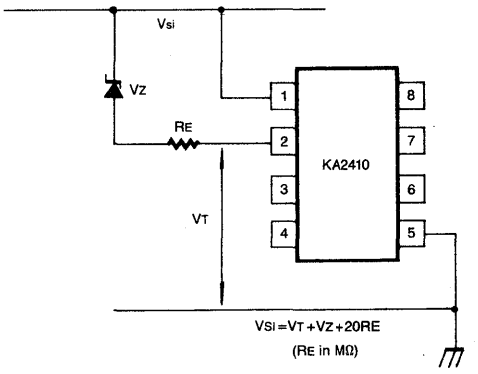


Fig. 8

TRIGGERING KA2410 FROM CMOS OR TTL LOGIC

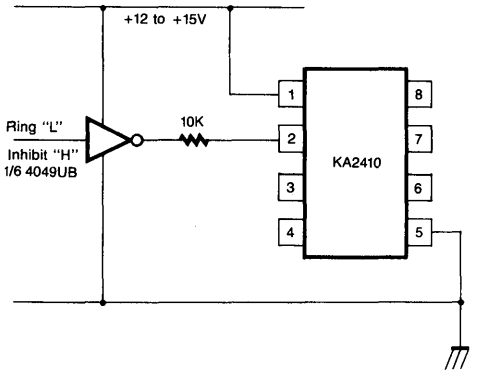


Fig. 9

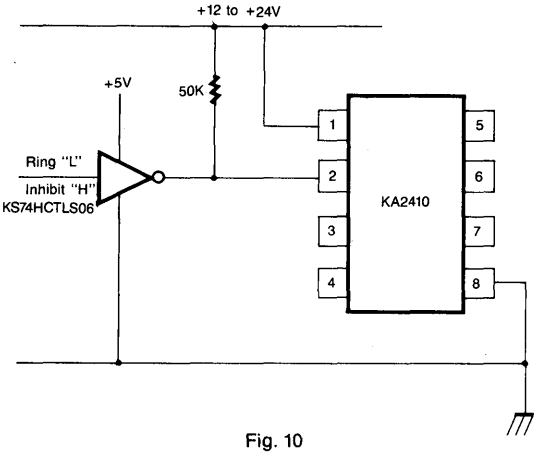
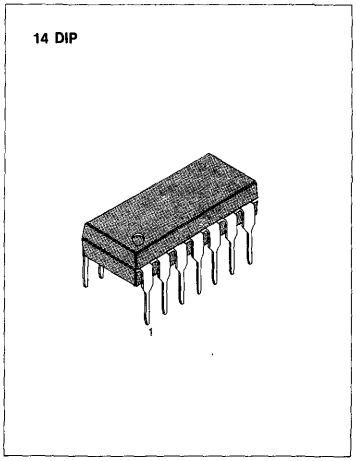


Fig. 10

TELEPHONE SPEECH CIRCUITS

The KA2412 A is designed for replacement of the hybrid circuit (2 ~ 4 wire interface) in conventional telephone.



FEATURES

- **Adjustable sending and receiving gain to compensate for line attenuation by sensing the line current.**
- **The same type of transducer can be used for both transmitter and receiver, usually a 350Ω dynamic type.**
- **Output impedance can be matched to the line, independent of transducer impedance.**
- **Minimum number of external parts required**

BLOCK DIAGRAM

ORDERING INFORMATION

Device	Operating Temperature
KA2412AN	−20 ~ +70°C

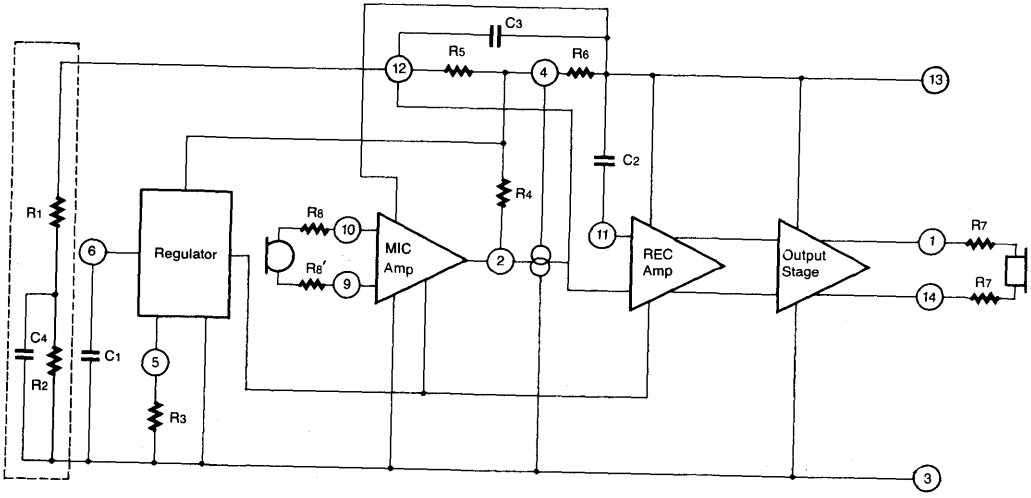


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Line Voltage (3 msec pulse duration)	V_L	22	V
Forword Line Current	I_{LF}	120	mA
Reverse Line Current	I_{LR}	−150	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a = −15°C ~ +45°C, f = 300Hz ~ 3400Hz unless otherwise specified. Refer to the test circuit.)

Characteristic	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit
Line Voltage	V_L	Fig 2	I_L = 80mA I_L = 20mA I_L = 10mA	9.5 4.8 3.2		11.0 5.6 4.5	V
Sending Gain	G_S	Fig 3	T_a = 25°C, f = 1KHz I_L = 10mA I_L = 20mA I_L = 60mA I_L = 80mA	 46.0 46.0 38.5 38.5		 50.0 50.0 42.5 42.5	dB
Sending Gain Variation vs Temp	$\triangle G_{ST}$	Fig 3	−15°C < Tamb < +45°C		±0.8		dB
Sending Gain Flatness	$\triangle G_{SF}$	Fig 3	G_S = 0dB at f = 1KHz I_L = 10 80mA			±0.5	dB
Sending Distortioin	THD_S	Fig 3	I_L = 20mA V_{SO} = $1V_{p-p}$ I_L = 80mA V_{SO} = 400mVrms			2.0 2.0	% %
Sending Noise	V_{NS}		V_{MI} = 0, I_L = 60mA			130	μV
Maximum Sending Output	V_S(max)	Fig 3	I_L = 10 V_{MI} = 707mVrms			6.0	V_{p-p}
Receiving Gain	G_R	Fig 4	T_a = 25°C, f = 1KHz I_L = 10mA I_L = 20mA I_L = 60mA I_L = 80mA	 −12.1 −12.1 −19.8 −21.4		 −9.9 −9.9 −17.2 −18.8	dB
Receiving Gain Variation vs Temp	$\triangle G_{RT}$	Fig 4	−15°C < Tamb < 45°C		±0.8		dB
Receiving Gain Flatness	$\triangle G_{RF}$	Fig 4	G_R = 0dB at f = 1KHz I_L = 10 80mA			±0.5	dB

ELECTRICAL CHARACTERISTICS (Continued)

(T_a = −15°C ~ +45°C, f=300Hz ~ 3400Hz, unless otherwise specified refer to the test circuit)

Characteristic	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit
Receiving Distortion	THD_R	Fig 4	I_L =20mA ~ 80mA V_{RO} =200mVrms			2.0	%
Receiving Noise	V_{NR}	Fig 4	V_{RI} =OV, I_L =60mA Posphometric			75	μV
Max Receiving Output Current		I_{om}	I_L =10mA V_{RI} =707mVrms			2.0	mA
Side Tone	ST	Fig 5	f=1KHz, T_a =25°C I_L =20mA I_L =60mA		7.0 0.0		dB
Return Loss	R_L	Fig 6	S2 in a S2 in b		14 14		dB

PIN DESCRIPTION

1. PIN 1, PIN 14 : Recevier output
2. PIN 2 : Line impedance adjust
3. PIN 3 : Ground
4. PIN 4 : DC regulator
5. PIN 5 : Bias
6. PIN 6 : AC loop opening
7. PIN 7 : No connection
8. PIN 8 : No connection
9. PIN 9, PIN 10 : Mic input
10. PIN 11 : Input receive Amp (−)
11. PIN 12 : Input receive Amp (+)
12. PIN 13 : V_{CC}

TEST CIRCUIT

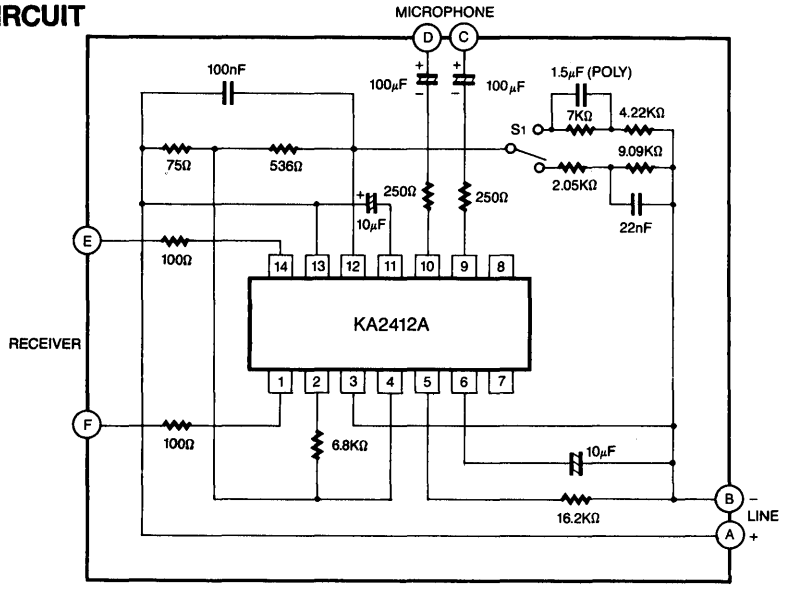


Fig. 2

Sending Gain

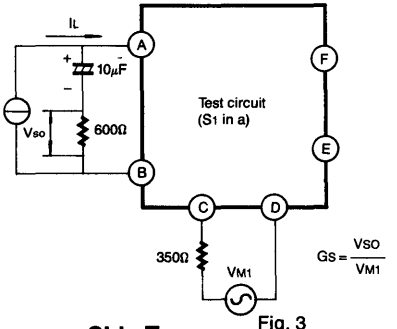


Fig. 3

Receiving Gain

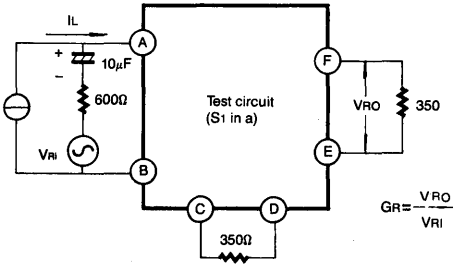


Fig. 4

Side Tone

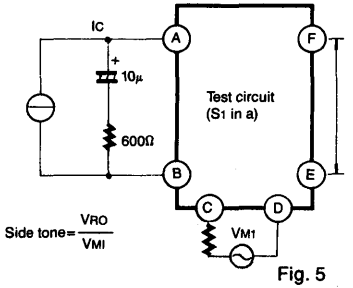


Fig. 5

Return Loss

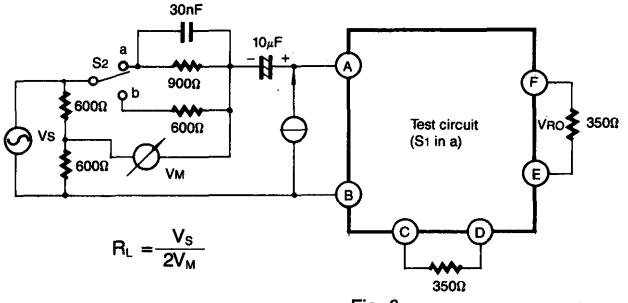


Fig. 6

APPLICATION INFOMRATION

The following table shows the recommended for the Fig 1. Different values can be used and notes are added in order to help designer.

Component	Recommended Value	Purpose	Note
R_1	2.05K	Balance network	In order to optimize the sidetone it is possible to change R_1 and R_2 values. In any case: $\frac{Z_B}{Z_L} = \frac{R_5}{R_6}$ where $Z_B = R_1 + R_2 // C_4$
R_2	9.09K		
R_3	16.2K	Bias resistor	Changing R_3 value, it is possible to shift the gain characteristics. The value can be chosen from 15K to 20K. The recommended value assures the maximum swing
R_5	536	Bridge resistors	The ratio R_5/R_6 fixes the amount of the signal delivered to the line.
R_6	75		
R_7, R_7'	100	Receiver impedance matching	R_7 and R_7' must be equal; 100Ω is a typical value for dynamic capsules
R_8, R_8'	250	Microphone impedance matching	R_8 and R_8' must be equal; 250Ω is a typical value for dynamic capsules. Furthermore, they determine a sending gain variation according to; $G_S = 20 \log \frac{R_X}{850}$ where $R_X = R_8 + R_8' + R_{MIC}$
C_1	10uF	AC loop opening	Ensures a high regulator impedance for AC signals (=20KΩ). This capacitor should not be higher than 10uF in order to have a short response time of the system.
C_2	1uF	DC decoupling for receiving input	
C_3	82nF	High frequency roll-off	C_3 determines the high frequency response of the circuit. It also acts as RF by pass.
C_4	22nF	Balance network	See note for R_1 and R_2

DESCRIPTION

1. Circuit Description:

The KA2412A is based on a bridge configuration. The KA2412A contains a regulator block, a sending amplifier and a receiving amplifier. The regulator monitors the line current and adjusts the amplifier gain to compensate for the line length.

The transmit/receiver amplifiers are connected to the line via an external bridge to provide side tone attenuation. When the subscriber is talking, A controlled amount of the sending signal is allowed to reach the receiver to give a feedback to the subscriber. The phenomenon is caused by mismatching of the wheastone bridge and is called the signal of side tone.

The line current compensation ensures that when the subscriber is talking, the signal delivered to the line is increased in according to the line length. When he is hearing, the signal level on the receiver capsule is constant.

Gain variation over the operating temperature range is less than ±1dB. The impedance to the line can be adjusted; without any change in circuit parameters; by changing an external resistor (6.8KΩ at Pin 2).

The KA2412A works with the same type of transducers for both transmitter and receiver (typically 350Ω Dynamic units).

2. Two to four wires conversion

1) In the case of the traditional telephone set:

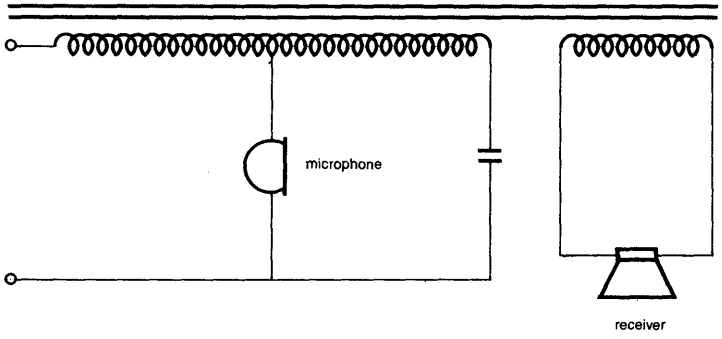


Fig. 10

A traditional speech circuit is equivalently equal to the circuit as described in Fig. 7. The microphone is composed of carbon powder. It converts the sound presure into the variation of resistance and so a AC signal is generated when the bias current flows through the microphone and a subscriber is talking. The current actuated by microphone does not affect receiver because it is compensated by the coil polarity.

But the incoming signal is transferred to receiver, so and this circuit is called 2 — 4 wires conversion, which is incoming 2 wires and Mic, Receivers 4 wires.

2) In the case of the KA2412 A

KA2412A performs the two wires (Telephone line) to four wires (Microphone, Receiver) conversion by means of a wheastone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see Fig. 8)

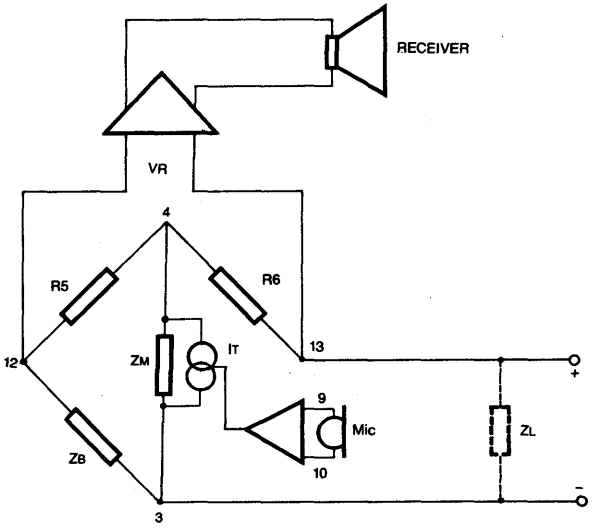


Fig. 8

For a perfect balancing of the bridge $\frac{Z_B}{Z_L} = \frac{R5}{R6}$

* In sending mode;

The AC signal from the microphone is sent to one diagonal of the bridge (pin 3 and pin 4). A small percentage of the signal power is lost on Z_B (being $Z_B >> Z_L$); the main part is sent to the line Via R6.

The impedance A_M is defined as $\frac{V_{4\text{-}3}}{I_{4\text{-}3}}$

$$V_R = \frac{(R6+Z_B)//(R5+Z_L)}{Z_M+(R6+Z_B)//(R5+Z_L)} \left(\frac{Z_L}{R6+Z_L} - \frac{Z_B}{R5+Z_B}\right) Z_M I_T$$

To reduce the receiving input signal,

$$\frac{Z_L}{R6+Z_L} = \frac{Z_B}{R5+Z_B} \rightarrow \frac{R6}{Z_L} = \frac{R5}{Z_B}$$

also, In order to reduce power loss in R5 & Z_B and to transfer the maximum power to the line via R6.

$R5+Z_B >> R6+Z_L$

$R6+Z_M = Z_L$

Then the line impedance Z_L grows from 600 ohm up to 900 ohm when the line length increases.
The voltage driven to the line is

$$V_L = \frac{Z_L}{R6+Z_M+Z_L} \times Z_{MIT}$$

In order to maximize sending Gain
$Z_L >> R6$

Therefore, in the case of the KA2412 test circuit:
$R6=75$, $Z_M=6.8K/11$, $Z_L=600$

$$V_L = \frac{Z_L}{Z_M+R6+Z_L} \times Z_M I_T = 286.82 I_T$$

* In receiving mode:
The AC signal coming from the line is sensed across the second diagonal of the wheastone bridge (pin 11 and pin 13). After amplification it is applied to the receiver.

$$V_R = \frac{V_I}{Z_L+R_6+(R_5+Z_B)//Z_M} (R_6+R_5+Z_B)//Z_M \left(1-\frac{Z_B}{Z_B+R_5}\right)$$

$$= \frac{V_I}{Z_L+R_6+(R_5+Z_B)//Z_M} \left(R_6+\frac{Z_M R_5}{Z_M+R_5+R_6}\right)$$

To avoid the reflection
$Z_L=R_6+Z_M$, $10\,Z_M=R_5+Z_B$

Therefore

$$V_R = \frac{V_I}{2R_6+1.91\,Z_M}\left(R_6+\frac{Z_B}{11}\right)$$

In the case of the KA2412A test circuit
$Z_L=600\Omega$, $R_6=75\Omega$, $Z_M=6.8K\Omega/11=6.8\Omega$
$R_5=536\Omega$, $Z_B=6.076K\Omega$ ($f_{REF}=1KHz$)

$$\frac{V_R}{V_I}=0.093$$

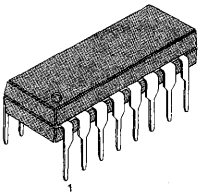
3. Automatic Gain Control.

The KA2412A automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation Maximum gain is reached for a line current of range 10 — 20mA and minimum gain can also be reached for a line current of range 60 — 100mA.

DUAL TONE MULTI FREQUENCY GENERATOR

The KA2413 is a monolithic integrated DTMF generator designed for use in a telephone set in parallel with an electronic speech circuit. The DC characteristic to the line is set by the speech circuit.

16 DIP



FEATURES

- **Wide operating line voltage and current range**
- **Operates with a standard crystal at 3.58MHz**
- **Operates with a single contact or matrix key-board**
- **Levels from the high and low frequency group can be adjusted separately.**
- **No individual level adjustment is necessary for every circuit**
- **The signal levels are stabilized against variations in temperature and line voltage.**
- **Short start-up time**
- **All tones can be generated separately for testing.**
- **Easy PCB layout; all keyboard connections on one side of the chip**
- **Internal protection of all inputs**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Operating Temperature
KA2413N	−20 ~ +70°C

BLOCK DIAGRAM

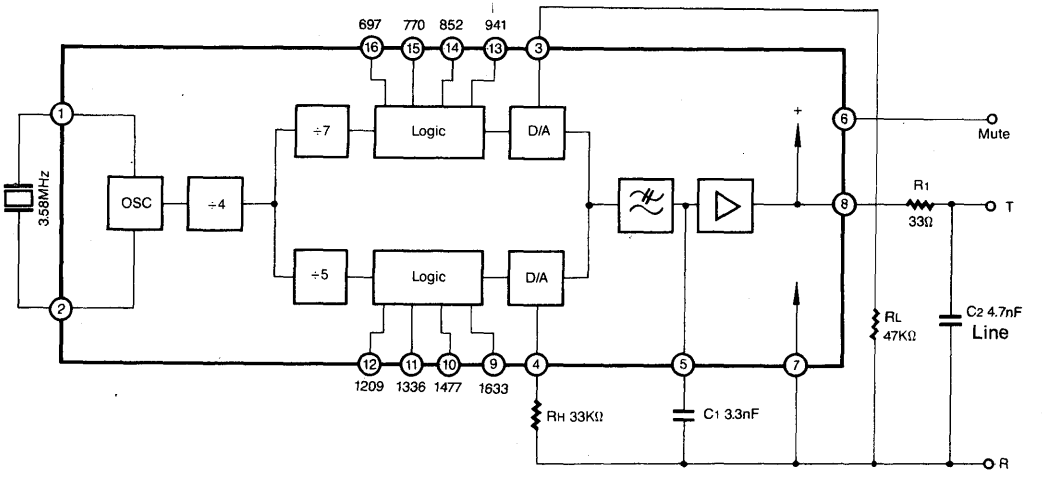


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Line Voltage (Peak) t_P=2 sec	V_L (peak)	20	V
Line Voltage (Peak) t_P=20m sec	V_L (peak)	22	V
Line Voltage (Conditions)	V_L (cont)	15	V
Power Dissipation	P_D	400	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (T_a=25°C)

(V_L=4.3 ~ 9V, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Line Voltage		V_L (opr)	Tone Generation 1.3 V_P Signal	4.3		9.0	V
Stand-By Line Voltage		V_L (std)	Stand-By 2.0 V_P Signal	4.3		9.0	V
Operating Line Current		I_L (opr)	V_L=4.3V			10.0	mA
Stand-By Line Current		I_L (std)	No Key Pressed V_L=4.3V			250	μA
Mute Current		I_M	One or More Keys Pressed	125.0			μA
Key Resistance		R_K	Key Circuit Closed			1.0	kΩ
Tone Output Frequency		Δf	f_{OSC}=3.5795 MHz				
Low (Row)	f_1=697 Hz			−1.0	−0.32	+1.0	%
	f_2=770 Hz			−1.0	+0.02	+1.0	%
	f_3=852 Hz			−1.0	+0.03	+1.0	%
	f_4=941 Hz			−1.0	−0.11	+1.0	%
High (Column)	f_5=1209 Hz			−1.0	−0.03	+1.0	%
	f_6=1336 Hz			−1.0	−0.03	+1.0	%
	f_7=1477 Hz			−1.0	−0.68	+1.0	%
	f_8=1633 Hz			−1.0	−0.36	+1.0	%

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Signal level	High	V_H	R_H=46.4KΩ R_L=69.8KΩ		-9.0		dBm
	Low	V_L			-11.0		
	High	V_H	R_H=33.0KΩ R_L=47.0KΩ	-8.0	-6.0	-4.0	dBm
	Low	V_L		-10.0	-8.0	-6.0	
	High	V_H	R_H=26.1KΩ R_L=39.2KΩ		-4.0		dBm
	Low	V_L			-6.0		
Ratio Signal Level		V_H/V_L		1.0	2.0	3.0	dB
Impedance to Line		Z_L	Tone Generation Stand-By	6.0 50.0			KΩ
Total Harmonic Distortion		THD	Tone Generation			-31.0	dBm
Output Noise		V_{NO}	Stand-By			-80.0	dBm
Harmonics			300 — 3400Hz			-33.0	dBm
			3.4 — 50KHz			-33.0	dBm
			≥50KHz			-80.0	dBm
Start-up Time		t_S	Output level within 1dB from final level		3	5	mS

TEST CIRCUIT

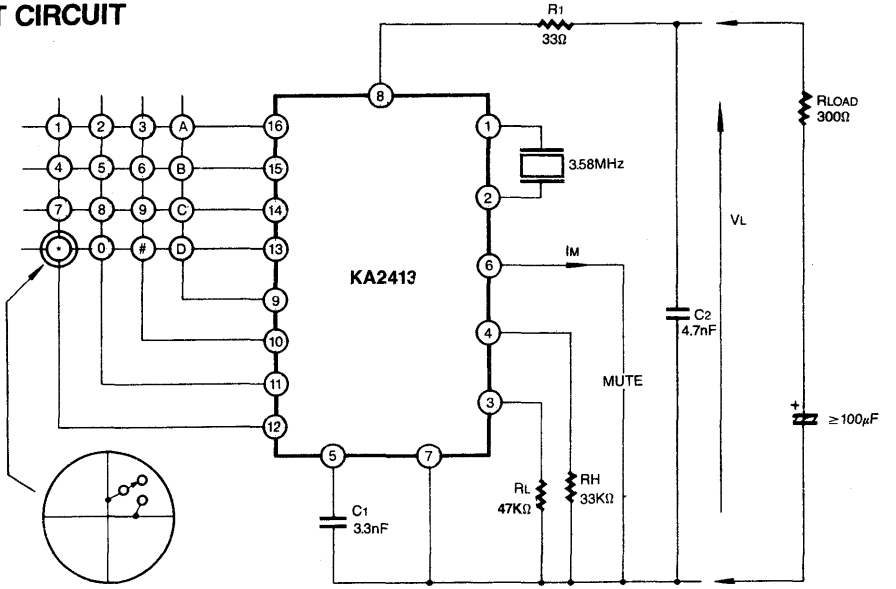


Fig. 2

- KA2413 can also be controlled by a microprocessor (see Fig 5). The negative branch of the microprocessor voltage supply is connected to pin 7 of KA2413 and the inputs (8) are connected with resistors.
  For tone-generating one input of the low group (pin 13 — 16) is connected to the positive voltage and one input of the high group (pin 9 — 12) is connected to the negative voltage, then KA2413 is activated and the mute output is put in High state.

Microcomputer interface

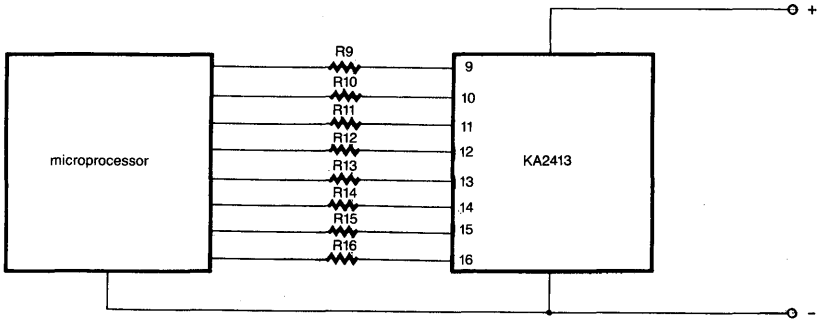


Fig. 5

1) R9, R10, R11, R12 (60K — 80K)
   The resistors have two functions are:
   — To raise the OFF/ON voltage
   — To limit the current when the input levels are high. Too high current will interfere with the functions of the other three inputs (the resistors can be exchanged with diodes directly away from KA2413)

High-frequency group resistors to microcomputer

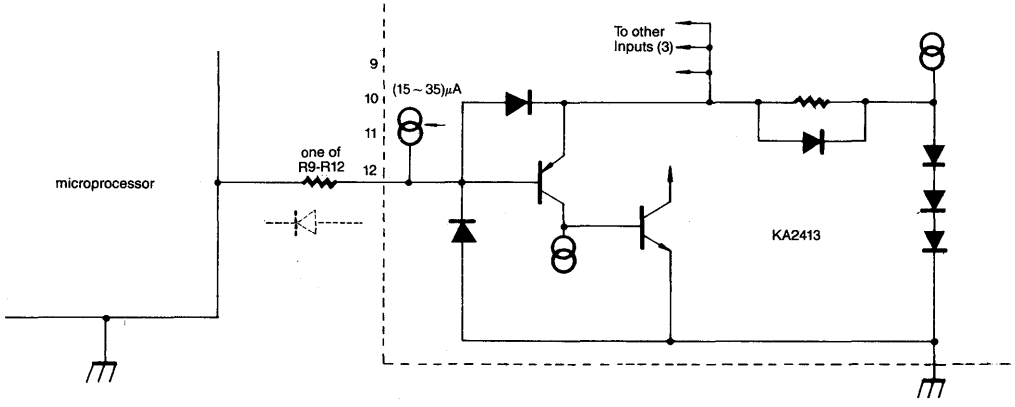


Fig. 6

2) R13, R14, R15, R16 (20K — 30K)
The two functions of the resistors are:
— To raise the OFF/ON voltage
— To limit the current when the input levels are high.

Low-frequency group resistors for microcomputer

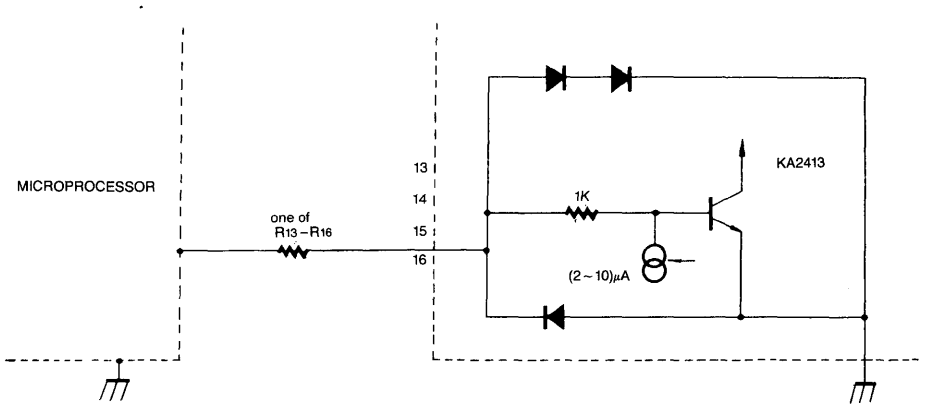


Fig. 7

TELEPHONE TONE RINGER WITH BRIDGE DIODE

The KA2418 is monolithic integrated circuit telephone tone ringer with bridge diode, when coupled with an appropriate transducer, replace the electromechanical bell. This device is designed for use with either a piezo transducer or an inexpensive transformer coupled speaker to produce a pleasing tone composed of a high frequency (f_H) alternating with a low frequency (f_L) resulting in a warble frequency. The supply voltage is obtained from the AC ring signal and the circuit is designed so that noise on the line or variations of the ringing signal cannot affect correct operation of the device.

8 DIP

FEATURES

- **On chip high voltage full wave diode bridge rectifier**
- **Low current consumption, in order to allow the parallel operation of the 4 devices**
- **Low external component count**
- **Tone and switching frequencies adjustable by external components**
- **High noise immunity due to built-in voltage-current hysteresis**
- **Activation voltage adjustable**
- **Internal zener diodes to protect against over voltages**
- **Ringer impedance adjustable with external components.**

ORDERING INFORMATION

Device	Operating Temperature
KA2418N	−20 ~ +70°C

APPLICATIONS

- Electronic telephone ringers
- Extension ringers

BLOCK DIAGRAM

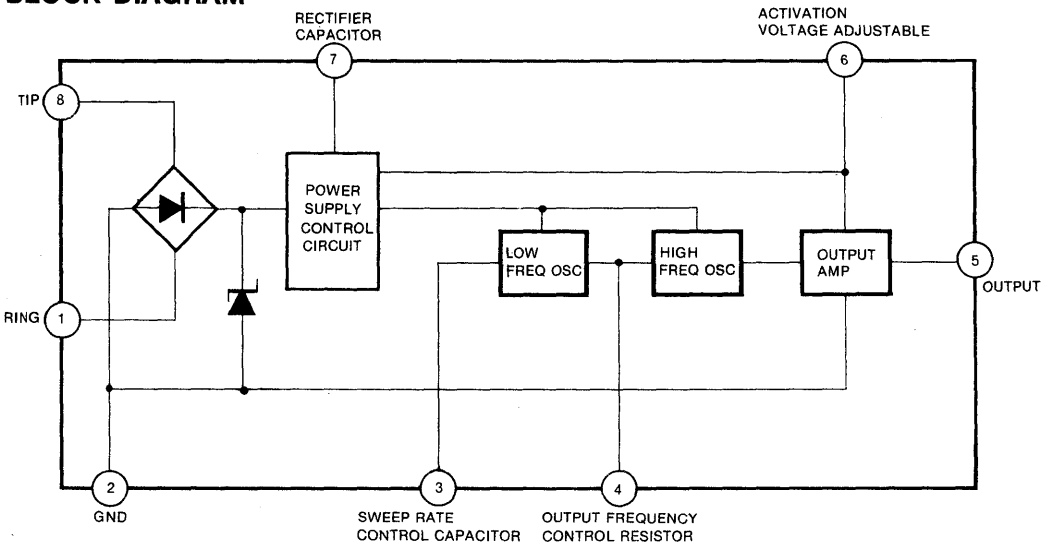


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Calling Voltage (f=50Hz) Continuous	V_{AB}	120	Vrms
Calling Voltage (f=50Hz) 5 Sec ON/10 Sec OFF	V_{AB}	200	Vrms
Supply Current	I_{CC}	22	mA
Operating Temperature	T_{OP}	−20 ~ +70	°C
Storage and Junction Temperature	T_{stg}	−65 ~ +150	°C

Absolute maximum ratings are those values beyond which peramanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

3

ELECTRICAL CHARACTERISTICS

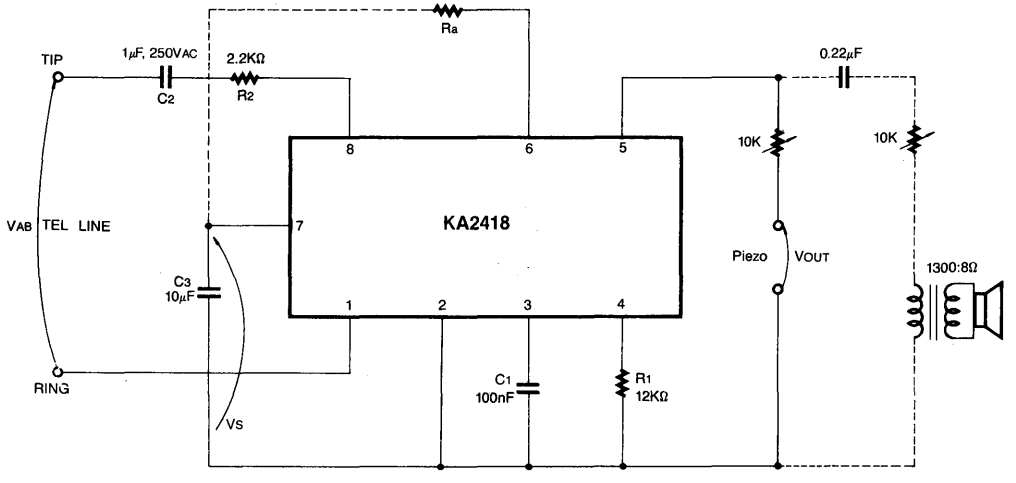
(T_a = 25°C *unless otherwise specified*)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{CC}				26	V
Current Consumption without Load	I_{CC}	V_S =8.8 to 26V		1.5	1.8	mA
Activiation Voltage	V_{ON}		12.2		13	V
Activiation Voltage Range	V_{ONR}	R_A =1kΩ	8		10	V
Sustaining Voltage	V_{SUS}		8		8.8	V
Differential Resistance in Off Condition	R_D		6.4			kΩ
Output Voltage Swing	V_{OUT}			V_{CC} −3		V
Short Circuit Current	I_{OUT}	V_S = 26V		35		mA

AC OPERATION

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Output Frequencies		V_{CC} =26V, R_1 =14kΩ				
f_{H1}	f_{H1}	V_{CC} =0V		1,900		Hz
f_{H2}	f_{H2}	V_{CC} =6V		1,300		Hz
f_{H1} Range		R_1 =27kΩ to 1.7kΩ	0.1		15	KHz
Sweep Frequency	f_L	R_1 = 14kΩ, C_1 = 100nF		10		Hz

TEST AND APPLICATION CIRCUIT



$$f_1 = \frac{2.67 \cdot 10^4}{R_1(K\Omega)} \qquad f_2 = \frac{5}{7} f_1 \qquad f_{sweep} = \frac{1000}{C_1(nF)}$$

Fig. 2

DESCRIPTION

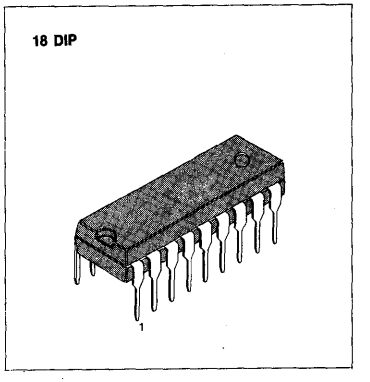
The KA2418 tone ringer derive its power supply by rectifying the AC ringing signal. It uses this power to activate two tone generators. The two tone frequencies generated are switched by an internal oscillator in a fast sequence and made audible across an output amplifier in the loudspeaker; both tone frequencies and the switching frequency can be externally adjusted.

The device can drive either directly a piezo ceramic converter (buzzer) or small loudspeaker. In case of using a loudspeaker, a transformer is needed.

An internal shunt voltage Regulator provides DC voltage to output stage, low frequency oscillator, an High frequency oscillator. To protect the IC from telephone line transients, a zener Diode is included.

SPEECH NETWORK WITH DIALER INTERFACE

The KA2425A/B is a telephone speech network integrated circuit which includes transmit amp, receive amp, sidetone amp, DC loop interface function, DTMF input, voltage regulator for speech, a regulated output voltage for a dialer, and equalization circuit.



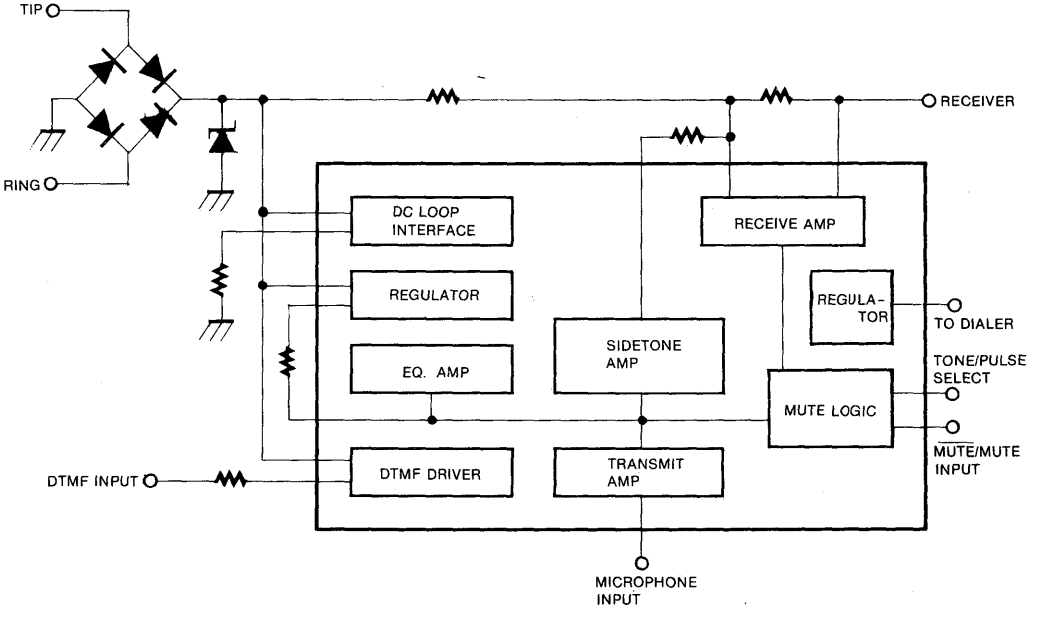
FEATURES

- **Low voltage operation (1.5V: speech)**
- **Transmit, receive, side tone and DTMF level are controled by external resistors**
- **Regulated voltage for dialer**
- **Loop length equalization**
- **$\overline{\text{MUTE}}$: KA2425A MUTE: KA2425B**
- **Linear interface for DTMF**

ORDERING INFORMATION

Device	Package	Function	Operating Temperature
KA2425AN	18 DIP	$\overline{\text{MUTE}}$	−20 ~ +60°C
KA2425BN	18 DIP	MUTE	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Value	Unit
V_+ Voltage	−1.0 ~ +18	V
V_{DD} ($V_+ = 0$)	−1.0 ~ +6	V
$\overline{MT}$, MT, MS Inputs	−1.0 ~ V_{DD} + 1	V
V_{LR}	−1.0 ~ V_+ − 3.0	V
Storage Temperature	−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Value	Unit
I_{TXO} (Instantaneous)	0 ~ 10	mA
V_+ Voltage: Speech Mode	+1.5 ~ +15	V
Tone Dialing Mode	+3.3 ~ +15	V
Operating Temperature	−20 ~ +60	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, Refer to Fig. 1)

Characteristic	Test Conditions	Min	Typ	Max	Unit
SYSTEM SPECIFICATIONS (Refer to Fig. 1	**Fig. 4)**				
Tip-Ring Voltage (including polarity guard bridge drop of 1.4V) (Speech Mode)	I_L = 5.0mA	—	2.4	—	V_{dc}
	I_L = 10mA	—	3.9	—	
	I_L = 20mA	—	4.6	—	
	I_L = 40mA	—	5.6	—	
	I_L = 60mA	—	6.6	—	
Transmit					
Gain from V_S to V+	Figure 3 (I_L = 20mA)	28	29.5	31	dB
Gain Change	I_L = 60mA	−6.0	−4.5	−3.6	dB
Distortion		—	2.0	—	%
Output Noise		—	11	—	dBmc
Receive					
V_{RXO}/V_S	f = 1.0KHz, I_L = 20mA	−16	−15	−13	dB
Receive Gain Change	(See Figure 4) I_L = 60mA	−5.0	−3.0	−2.0	dB
Distortion		—	2.0	—	%
Sidetone Level					dB
$V_{RXO}/V+$ (Figure 3)	I_L = 20mA	—	−36	—	
	I_L = 60mA	—	−21	—	
Sidetone Cancellation		20	26	—	dB
$\{\frac{V_{RXO}}{V+}$(Figure 4)$\}$dB − $\{\frac{V_{RXO}}{V+}$(Figure 3)$\}$dB	I_L = 20mA				
DTMF Driver		3.2	4.8	6.2	dB
$V+V_{IN}$ (Figure 2)	I_L = 20mA				
AC Impedance					Ω
Speech mode (incl. C_6, See Figure 4)	I_L = 20mA	—	750	—	
$Z_{ac} = (600)V+/(V_S - V+)$	I_L = 60mA	—	300	—	
Tone Mode (including C_6)	20mA < I_L < 60mA	—	1650	—	

Note: Typicals are not tested or guaranteed.

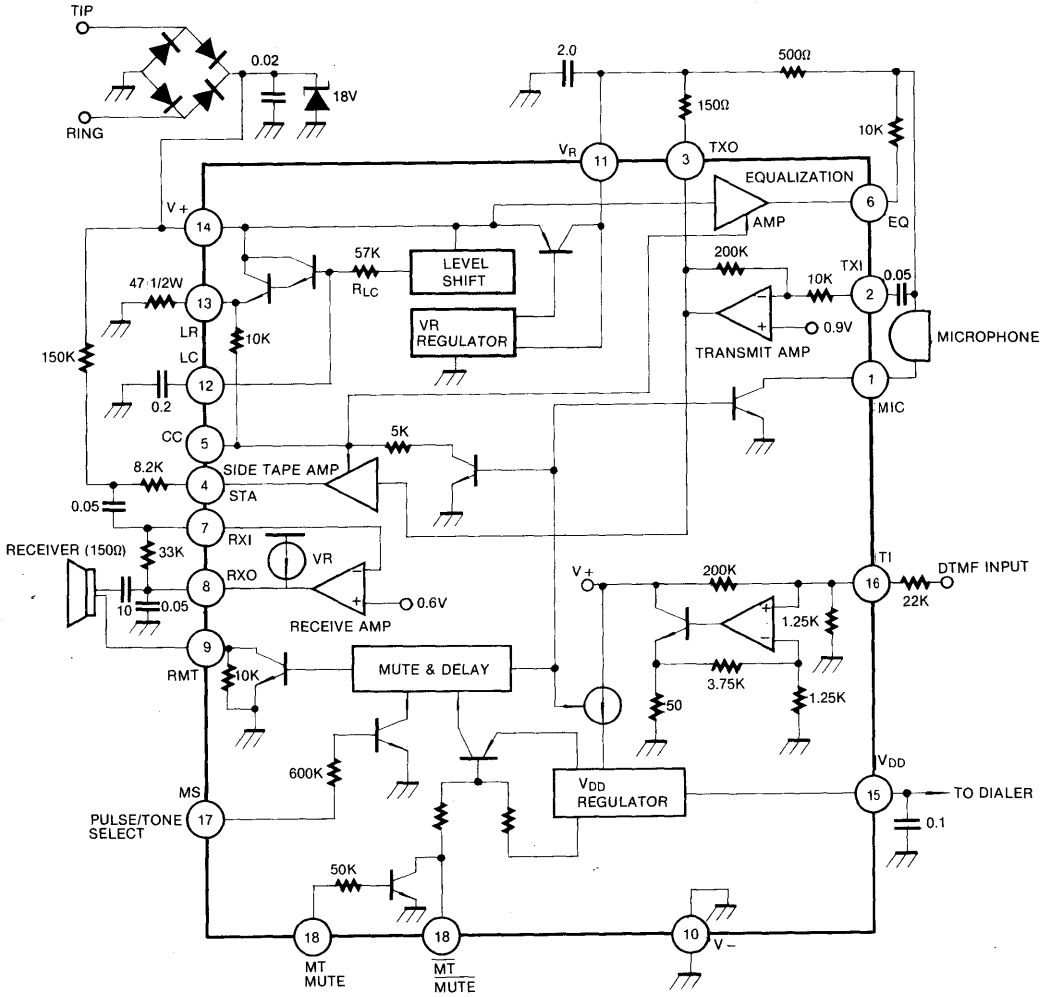
ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
SPEECH AMPLIFIERS						
Transmit Amplifier						
Gain	A_{TXO}	TXI to TXO	22	24	26	dB
TXO Bias Voltage	V_{TXOSP}	Speech/Pulse Mode	0.45	0.52	0.60	$\times V_R$
TXO Bias Voltage	V_{TXOL}	Tone Mode	VR – 25	VR – 5.0	—	mV
TXO High Voltage	V_{TXCH}	Speech/Pulse Mode	VR – 25	VR – 5.0	—	mV
TXO Low Voltage	V_{TXCL}	Speech/Pulse Mode	—	125	250	mV
TXI Input Resistance	R_{TXI}		—	10	—	KΩ
Receive Amplifier						
RXO Bias Voltage	V_{RXO}	All Mode	0.45	0.52	0.60	$\times V_R$
RXO Source Current	I_{RXOSP}	Speech Mode	1.5	2.0	—	mA
RXO Source Current	I_{RXOCL}	Pulse/Tone Mode	200	400	—	μA
RXO High Voltage	V_{RXCH}	All Mode	VR – 100	VR – 50	—	mV
RXO Low Voltage	V_{RXOL}	All Mode	—	50	150	mV
SIDETONE AMPLIFIER						
Gain (TXO to STA)	A_{STA}					dB
Speech Mode		@V_{LR} = 0.5V	—	– 15	—	
Speech Mode		@V_{LR} = 2.5V	—	– 21	—	
Pulse Mode		@V_{LR} = 0.2V	—	– 15	—	
Pulse Mode		@V_{LR} = 1.0V	—	– 21	—	
STA Bias Voltage	V_{STA}	All Modes	0.65	0.8	0.9	$\times V_R$
MICROPHONE, RECEIVER CONTROLS						
MIC Saturation Voltage	V_{OLMIC}	Speech Mode, I = 500μA	—	50	125	mV
MIC Leakage Current	I_{MICLK}	Dialing Mode, Pin 1 = 3.0V	—	0	5.0	μA
RMT Resistance	R_{RMTSP}	Speech Mode	—	8.0	15	Ω
	R_{RMTDL}	Dialing Mode	5.0	10	18	KΩ
RMT Delay	t_{RMT}	Dialing to Speech	2.0	4.0	20	ms
EQUALIZATION AMPLIFIER						
Gain (V + to EQ)	A_{EQ}					dB
Speech Mode		@V_{LR} = 0.5V	—	– 12	—	
Speech Mode		@V_{LR} = 2.5V	—	– 2.5	—	
Pulse Mode		@V_{LR} = 0.2V	—	– 12	—	
Pulse Mode		@V_{LR} = 1.0V	—	– 2.5	—	
EQ Bias Voltage	V_{EQ}					V_{dc}
Speech Mode		@V_{LR} = 0.5V	—	0.66	—	
Pulse Mode		@V_{LR} = 0.5V	—	1.3	—	
Speech, Pulse Mode		@V_{LR} = 2.5V	—	3.3	—	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
DIALING INTERFACE						
$\overline{MT}$ Input Resistance	H_{MT}		50	100		KΩ
MT Input Resistance			—	50	—	KΩ
$\overline{MT}$, MT Input High Voltage	V_{IHMI}		$V_{DD}-0.3$	—		V_{dc}
$\overline{MT}$, MT Input Low Voltage	V_{ILMT}		—	—	1.0	V_{dc}
MS Input Resistance	R_{MS}		280	600		KΩ
MS Input High Voltage	V_{IHMS}		2.0	—	—	V_{dc}
MS Input Low Voltage	V_{ILMS}		—		0.3	V_{dc}
TI Input Resistance	R_{TI}		—	1.25	—	KΩ
DTMF Gain	A_{DTMF}	See Figure 2 ($V+/V_{IN}$)	3.2	4.8	6.2	dB
LINE INTERFACE						
V+ Current (Pin 12 Grounded)	I+					mA
Speech Mode		V+ = 1.7V	4.5	7.1	9.0	
Speech/Pulse Modes		V+ = 12V	5.5	8.4	12.5	
Tone Mode		V+ = 12V	6.0	8.8	14.0	
V+ Voltage	V+					V_{dc}
Speech/Pulse Mode		I_L = 20mA	2.6	3.2	3.8	
Speech/Pulse Mode		I_L = 30mA	3.0	3.7	4.4	
Speech/Pulse Mode		I_L = 120mA	7.0	8.2	9.5	
Tone Mode		I_L = 20mA	4.1	4.9	5.7	
Tone Mode		I_L = 30mA	4.5	6.4	6.2	
LR Level Shift	$\triangle V_{LR}$					V_{dc}
Speech/Pulse Mode		V+ − V_{LR}	—	2.7	—	
Tone Mode			—	4.3	—	
LC Terminal Resistance	R_{LC}		36	57	94	KΩ
VOLTAGE REGULATORS						
VR Voltage	V_R	(V+ = 1.7V)	1.1	1.2	1.3	V_{dc}
Load Regulation	$\triangle V_{RLD}$	0mA < I_R < 6.0mA	—	20	—	mV
Line Regulation	$\triangle V_{RLE}$	2.0V < V+ < 6.5V	—	25	—	mV
V_{DD} Voltage	V_{DD}	(V+ = 4.5V)	3.0	3.3	3.8	V_{dd}
Load Regulation (Dialing Mode)	$\triangle V_{DDLD}$	0 < I_{DD} < 1.6mA	—	0.25	—	V_{dd}
Line Regulation (All Modes)	$\triangle V_{DDLM}$	4.0V < V+ < 9.0V	—	50	—	mV
Max. Output Current	I_{DDSM}	Speech Mode	375	550	1000	μA
Max Output Current	I_{DDOL}	Dialing Mode	1.6	2.0	3.6	mA
V_{DD} Leakage Current	I_{DDLK}	V+ = 0, V_{DD} = 3.0V		—	1.5	μA

Fig. 1 Test Circuit



PIN DESCRIPTION (See Fig. 1)

No.	Name	Description
1	MIC	Microphone negative supply pin
2	TXI	Transmit amplifier input. Input impedance is 10KΩ
3	TXO	Transmit amplifier output. The AC signal current from this output flows through the V_R series pass transistor via R_9 to drive the line at V+. Increasing R_9 will decrease the signal at V+.
4	STA	Sidetone amplifier output. The signal level at STA increases with loop length.
5	CC	Compensation capacitor. In most application, CC remains open. A capacitor from CC to GND will compensate the loop length equalization circuit when additional stability is required.
6	EQ	Equalization amplifier output. A portion of the V+ signal is present on this pin to provide negative feed back around the transmit amplifier. The feedback decreases with increasing loop length, causing the AC impedance of the circuit to increase.
7	RXI	Receive amplifier input. Input impedance is>100KΩ.
8	RXO	Receive amplifier output.
9	RMT	Receiver mute.
10	V−	Negative supply.
11	VR	Regulated voltage output. The VR voltage is regulated at 1.2V.
12	LC	AC load capacitor.
13	LR	DC load resistor. This resistor determines the DC resistance of the telephone, and removes power dissipation from the chip.
14	V+	Positive supply.
15	V_{DD}	V_{DD} regulator. V_{DD} is the output of a shunt type regulator with a nomina voltage of 3.3V.
16	TI	DTMF input. Increasing R_7 will reduce the DTMF output levels.
17	MS	Mode select. A logic "I" (>2.0V) selects the pulse dialing mode. A logic "O" (<1.0V) selects the tone dialing mode.
18	$\overline{MT}$	Mute input for KA2425A. $\overline{MT}$ is connected through an internal 100KΩ resistor to the base of an NPN transistor, with the emitter at V_{DD}. A logic "O" (<1.0V) will mute the network for dialing. A logic "I" (>V_{DD} − 0.3V) puts the KA2425A into the speech mode.
	MT	Mute input for KA2425B. MT is connected through an internal 50KΩ to the base of a NPN transistor, with the collector to the base of a PNP transistor. A logic "I" (>V_{DD} − 0.3V) will mute the network for dialing. A logic "O" (<1.0V) puts the KA2425B into the speech mode.

Fig. 2 DTMF Driver Test

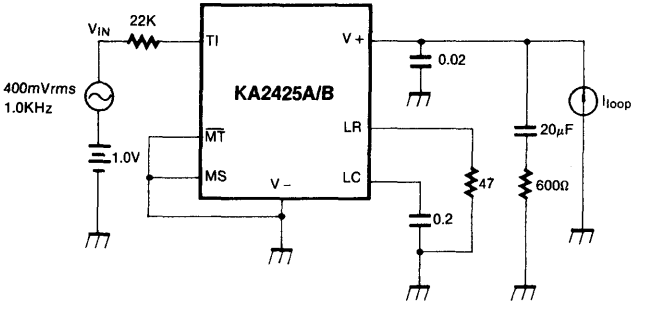


Fig. 3 Transmit and Sidetone Level Test

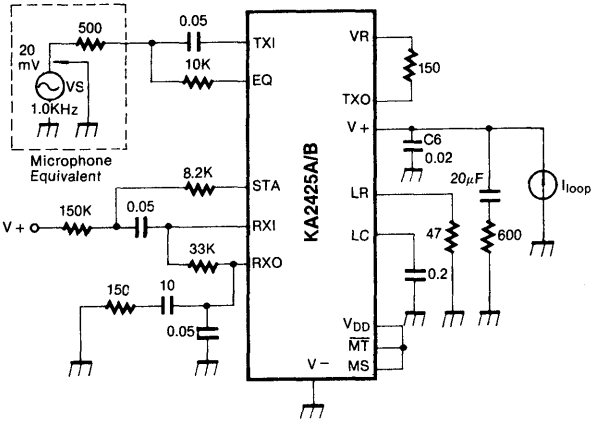
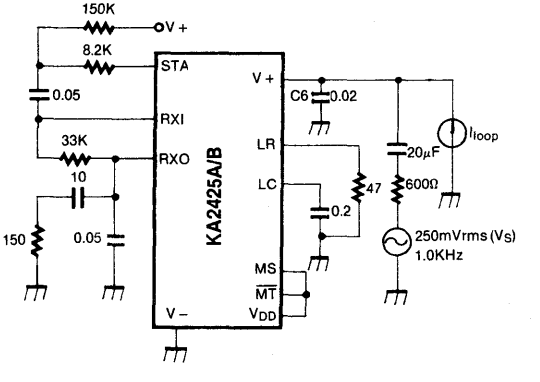
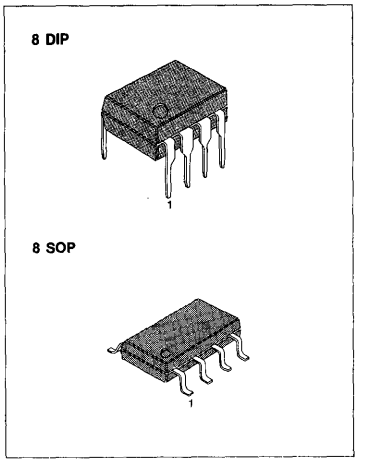


Fig. 4 AC Impedance, Receive and Sidetone Cancellation Test



LINE DRIVER AND RECEIVER

The KA2654 is a monolithic one line driver and one line receiver designed to interface DTE (Data Terminal Equipment) with DCE (Data Communication Equipment) in conformance with the specifications of EIA standard No.RS-232C.
The driver is similar to the MC1488. The receiver is similar to the MC1489 and that a separate response control terminal is provided for.
A resistor or a resistor and bias voltage can be connected between this terminal and ground to shift the input threshold voltage level. An external capacitor can be connected from terminal to ground to provide input noise filtering.



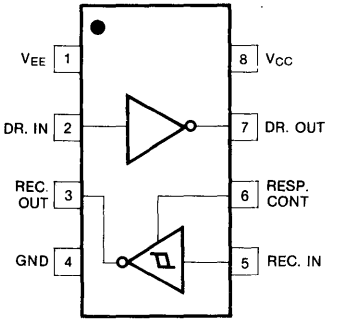
FEATURES

- **Meet specifications of EIA RS-232C**
- **Current limited output: 12mA (Typ)**
- **Wide supply voltage: ±4.5 ~ ±15V**
- **Low power consumption: 117mW**
- **Power off source impedance: 300 ohms**
- **Response Control Provides**
- **Receiver output compatible with TTL**

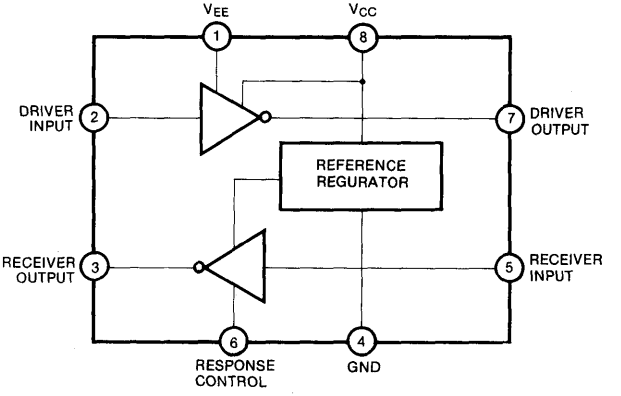
ORDERING INFORMATION

Device	Package	Operating Temperature
KA2654N	8 DIP	−20 ~ +85°C
KA2654D	8 SOP	−20 ~ +70°C

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Characteristic		Symbol	Value	Unit
Positive Supply Voltage		V_{CC}	−0.4 ~ +18	V
Negative Supply Voltage		V_{EE}	0.4 ~ −18	V
Input Voltage Range of Driver		V_{ird}	−5 ~ 18	V
Input Voltage Range of Receiver		V_{irr}	−30 ~ 30	V
Output Voltage Range of Driver		V_{ord}	−25 ~ 25	V
Output Voltage Range of Receiver		V_{orr}	−0.4 ~ 7	V
Output Current of Driver		I_{cd}	50	mA
Response Control Current		I_{res}	−10 ~ 10	mA
Power Dissipation	DIP	P_d	762	mW
	SOP	P_d	543	mW
Operating Temperature Range	DIP	T_a	−20 ~ 85	°C
	SOP	T_a	−20 ~ 70	°C
Storage Temperature Range		T_{stg}	−65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	4.5 ~ 15	V
Negative Supply Voltage	V_{EE}	−4.5 ~ −15	V
Response Control Current	I_{RES}	−5.5 ~ 5.5	mA
Input Voltage of Driver	V_{ID}	15	V
Input Voltage of Receiver	V_{IR}	−25 ~ 25	V
Output Current of Receiver	I_{OR}	24	mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12V, V_{EE} = −12V, Ta = −20°C ~ 85°C, unless otherwise noted)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Positive Supply Current	V_{CC} = 5V	I_{CC1}	V_{ID} = 2.0V		6.3	8.1	mA
	V_{CC} = 9V		V_{IR} = 2.3V		9.1	11.9	
	V_{CC} = 12V		No Load		10.4	14.0	
	V_{CC} = 5V	I_{CC2}	V_{ID} = 0.8V		2.5	3.4	
	V_{CC} = 9V		V_{IR} = 0.6V		3.7	5.1	
	V_{CC} = 12V		No Load		4.1	5.6	
Negative Supply Current	V_{EE} = −5V	I_{EE1}	V_{ID} = 2.0V		−2.4	−3.1	
	V_{EE} = −9V		V_{IR} = 2.3V		−3.9	−4.9	
	V_{EE} = −12V		No Load		−4.8	−6.1	
	V_{EE} = −5V	I_{EE2}	V_{ID} = 0.8V		−0.20	−0.35	
	V_{EE} = −9V		V_{IR} = 0.6V		−0.25	−0.40	
	V_{EE} = −12V		No Load		−0.27	−0.45	
Positive Supply Current	V_{CC} = 5V	I_{CC3}	V_{ID} = 0V, V_{IR} = 2.3V		4.8	6.4	
	V_{CC} = 12V		V_{EE} = 0V, No Load		6.7	9.1	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
DRIVER							
Input Voltage High		V_{IH}		2.0			V
Input Voltage Low		V_{IL}				0.8	V
Output Voltage High	$V_{CC}=5V$, $V_{EE}=-5V$	V_{OH}	$V_{ID}=0.8V$, $R_L=3K\Omega$	3.2	3.7		V
	$V_{CC}=9V$, $V_{EE}=-9V$			6.5	7.1		
	$V_{CC}=12V$, $V_{EE}=-12V$			8.9	9.8		
Output Voltage Low	$V_{CC}=5V$, $V_{EE}=-5V$	V_{OL}	$V_{ID}=2.0V$, $R_L=3K\Omega$		−3.6	−3.2	V
	$V_{CC}=9V$, $V_{EE}=-9V$				−7.1	−6.4	
	$V_{GC}=12V$, $V_{EE}=-12V$				−9.7	−8.8	
Input Current High		I_{IH}	$V_{ID}=7.0V$			5	μA
Input Current Low		I_{IL}	$V_{ID}=0.0V$		−0.73	−1.2	mA
Output Short Circuit Current (Positive)		I_{OSH}	$V_{ID}=0.8V$, $V_O=0.0V$	−7.0	−12.0	−14.5	mA
Output Short Circuit Current (Negative)		I_{OSL}	$V_{ID}=2.0V$, $V_O=0.0V$	6.5	11.5	14.0	mA
Output Impedance		R_O	$V_{CC}=V_{EE}=0V$, $V_O=\pm 2V$	300			Ω
RECEIVER							
Input Threshold Voltage (Positive)		V_{T+}		1.2	1.9	2.3	V
Input Threshold Voltage (Negative)		V_{T-}		0.6	0.95	1.2	
Input Hysteresis		V_{HYS}		0.6			V
Output Voltage High	$V_{CC}=5V$, $V_{EE}=-5V$	V_{OH}	$V_{IR}=0.6V$, $I_{OH}=-10\mu A$	3.7	4.1	4.5	V
	$V_{CC}=12V$, $V_{EE}=-12V$			4.4	4.7	5.2	
	$V_{CC}=5V$, $V_{EE}=-5V$	V_{OH}	$V_{IR}=0.6V$, $I_{OH}=0.4mA$	3.1	3.4	3.8	
	$V_{CC}=12V$, $V_{EE}=-12V$			3.6	4.0	4.5	
Output Voltage Low		V_{OL}	$V_{IR}=2.3V$, $I_{OL}=24mA$		0.2	0.3	V
Input Current High		I_{IH}	$V_{IR}=25V$	3.6	6.7	8.3	mA
			$V_{IR}=3V$	0.43	0.67	1.0	
Input Current Low		I_{IL}	$V_{IR}=-25V$	−3.6	−6.7	−8.3	mA
			$V_{IR}=-3V$	−0.43	−0.74	−1.0	
Output Short Circuit Current		I_{OS}	$V_{IR}=0.6V$		−2.8	−3.7	mA

SWITCHING CHARACTERISTICS

(V_{CC} = 12V, V_{EE} = −12V, Ta = −25°C, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
DRIVER						
Propagation Delay Time Low to High	t_{PLH}	R_L = 3KΩ, C_L = 50pF		340	480	ns
Propagation Delay Time High to Low	t_{PHL}			100	150	ns
Transition Time Low to High	t_{TLH}			120	180	ns
Transition Time High to Low	t_{THL}			105	160	ns
Transition Time Low to High	t_{TLH}	R_L = 3KΩ ~ 7KΩ, C_L = 2500pF		2.1	3.0	μs
Transition Time High to Low	t_{THL}			2.1	3.0	μs
RECEIVER						
Propagation Delay Time Low to High	t_{PLH}	R_L = 400Ω, C_L = 50pF		150	240	ns
Propagation Delay time High to Low	t_{PHL}			50	100	ns
Transition Time Low to High	t_{TLH}			250	360	ns
Transition Time High to Low	t_{THL}			18	35	ns

Note: Measured between +3V and −3V points on the output waveform.

TEST CIRCUIT

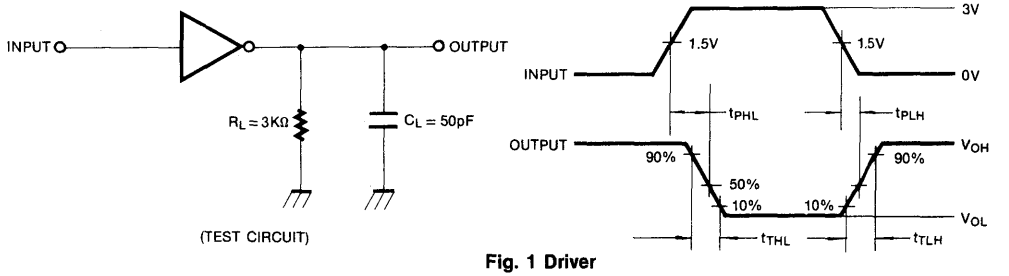


Fig. 1 Driver

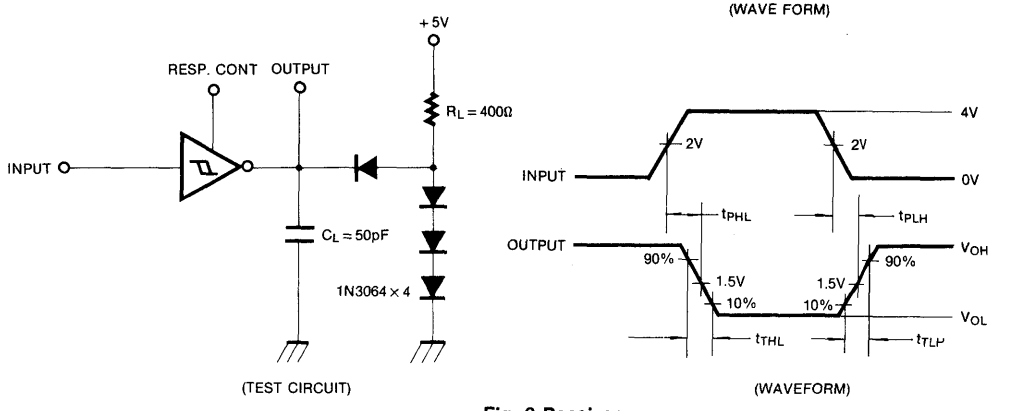
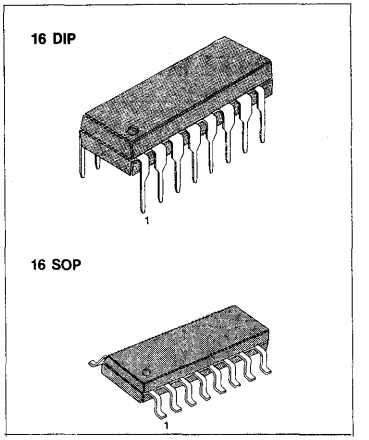


Fig. 2 Receiver

NOTES

3 LINE DRIVERS AND 3 LINE RECEIVERS

The KS5706 is a CMOS 3 line drivers and 3 line receivers in a single chip designed to interface data terminal equipment with data communications equipment in conformance with the electrical specifications of EIA standard RS-232-C and CCITT V.28.



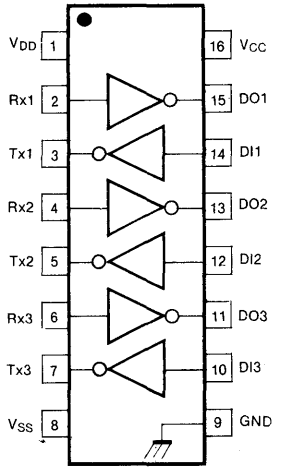
FEATURES

- **Current limited output**
- **Power-off source impedance: 300 Ohms**
- **Compatible with TTL**
- **Flexible operating supply range (±5 to ±12V)**
- **Output voltage swing selectable**
- **Input resistance (3 to 7 KΩ)**
- **Input voltage range: ±25V**
- **Input threshold hysteresis built in**

ORDERING INFORMATION

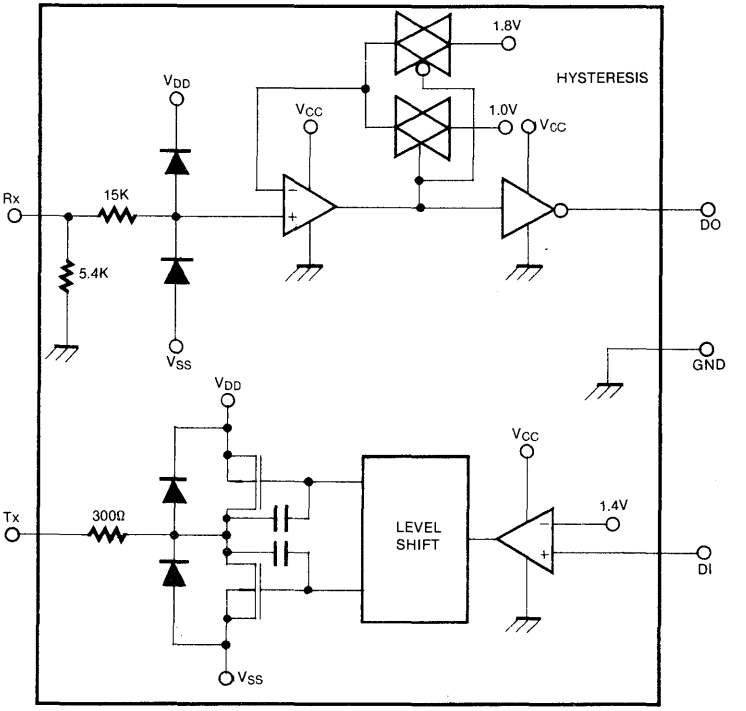
Device	Package	Operating Temperature
KS5706N	16 DIP	−40 ~ +85°C
KS5706D	16 SOP	

PIN CONFIGURATION



SCHEMATIC DIAGRAM

(1/3 OF CIRCUIT SHOWN)



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Value	Unit
Power Supply Voltage ($V_{DD} \geq V_{CC}$)	V_{DD} V_{SS} V_{CC}	−0.5 ~ 13.5 +0.5 ~ −13.5 −0.5 ~ 6.0	V_{dc}
Input Voltage Range Receiver Input (Rx1-3) Driver Input (DI1-3)	V_{IR}	 −25 ~ 25 −0.5 ~ V_{DD} + 0.5	V_{dc}
Maximum Current Per Pin	I_{max}	±60	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_a	−40 ~ 85	°C
Storage Temperature	T_{stg}	−85 ~ 150	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5 to +12V, V_{SS} = −5 to −12V, $V_{DD} \geq V_{CC}$, Ta = −40° to 85°C, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITIONS						
Power Supply Voltage V_{DD} V_{SS} V_{CC}	V_{DD} V_{SS} V_{CC}	 $V_{DD} \geq V_{CC}$	4.5 −4.5 4.5	5 to 12 −5 to −12 5.0	13.2 −13.2 5.5	V_{dc}
Quiescent Current (Inputs tied to GND, outputs unloaded)	I_{DD} I_{SS} I_{CC}	V_{DD} = +12.0V V_{SS} = −12.0V V_{CC} = +5.0V		140 340 300	400 600 450	μA
DRIVER (V_{CC} = +5V ± 5%)						
Input Voltage (DI1-3)	V_{IL} V_{IH}	Low High	 2.0		0.8	V_{dc}
Input Leakage Current (DI1-3)	I_{IN}	DI1-3 = V_{CC}			±1.0	μA
Output Voltage High (DI1-3 = 0.8V, R_L = 3.0KΩ), Tx1-3	V_{OH}	V_{DD} = 5.0V, V_{SS} = −5.0V V_{DD} = 6.0V, V_{SS} = −6.0V V_{DD} = 12.0V, V_{SS} = −12.0V	3.5 4.3 9.2	3.9 4.7 9.5		V_{dc}
Output Voltage Low (DI1-3 = 2.0V, R_L = 3.0KΩ), Tx1-3	V_{OL}	V_{DD} = 5.0V, V_{SS} = −5.0V V_{DD} = 6.0V, V_{SS} = −6.0V V_{DD} = 12.0V, V_{SS} = −12.0V	−4.0 −4.5 −10.0	−4.3 −5.2 −10.3		V_{dc}
Output Short Circuit Current	I_{SC}	(V_{DD} = 12.0V, V_{SS} = −12.0V) Tx1-3 shorted to Gnd Tx1-3 shorted to ±15.0V		 ±10 ±40	 ±20 ±60	mA
Power Off Source Resistance (Tx1-3)	R_n	V_{DD} = V_{SS} = Gnd = 0V, Tx1-3 = ±2.0V	300			Ω

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
RECEIVER						
Input Turn-On Threshold Voltage, Rx1-3	V_{IH}	DO1-3 = V_{OL}, V_{CC} = 5.0 ~ 6.0V	1.35	1.80	2.35	V_{dc}
Input Turn-Off Threshold Voltage, Rx1-3	V_{IL}	DO1-3 = V_{OH}, V_{CC} = 5.0 ~ 6.0V	0.75	1.00	1.25	V_{dc}
Input Threshold Hysteresis, Rx1-3	V_{HY}	$V_{IH} - V_{IL}$	0.6	0.8		V_{dc}
Input Resistance, Rx1-3	R_{IN}	Rx1-3 = ±3 ~ ±25V	3.0	5.4	7.0	KΩ
Output Voltage High, DO1-3 (Rx1-3 = −3 ~ −25V)	V_{OH}	I_{OUT} = −20μA, V_{CC} = 5.0V I_{OUT} = −1mA, V_{CC} = 5.0V	4.9 3.8	 4.3		V_{dc}
Output Voltage Low, DO1-3 (Rx1-3 = 3 ~ 25V)	V_{OL}	I_{OUT} = 20μA, V_{CC} = 5.0V I_{OUT} = 2mA, V_{CC} = 5.0V I_{OUT} = 4mA, V_{CC} = 5.0V		0.01 0.2 0.5	0.1 0.5 0.7	V_{dc}
SWITCHING CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{DD} = 6V ~ 12V, V_{SS} = −6V ~ −12V. Fig 2)						
Drivers Propagation Delay Time, Tx1-3	t_{PLH} t_{PHL}	R_L = 3KΩ, C_L = 50pF, Low to High R_L = 3KΩ, C_L = 50pF, High to Low		200 200	325 325	nS
Drivers Output Slew Rate, Tx1-3	SR	R_L = 3KΩ, C_L = 50pF		±6	±30	V/μS
Receivers Propagation Delay Time, DO1-3	t_{PLH} t_{PHL}	C_L = 50pF, Low to High C_L = 50pF, High to Low		150 150	300 300	nS
Receivers Output Rise Time, DO1-3	t_r	C_L = 50pF		250	400	nS
Receivers Output Fall Time DO1-3	t_f	C_L = 50pF		40	80	nS

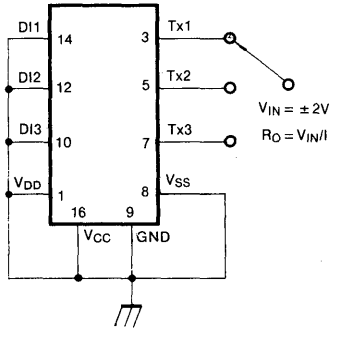


Fig. 1 Power Off Source Resistance

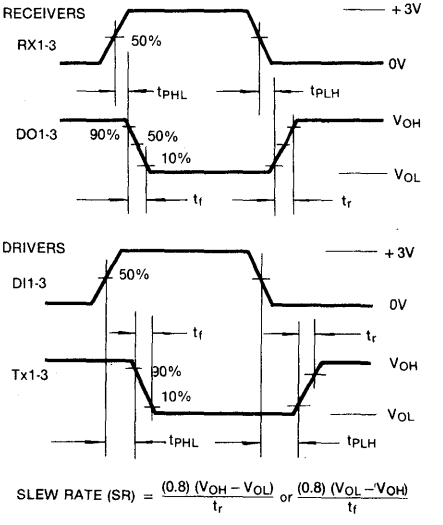


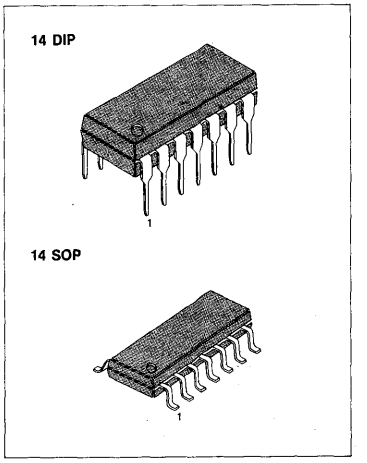
Fig. 2 Switching Characteristics

PIN DESCRIPTION

Pin	Name	Functions
1	V_{DD}	Positive power supply. Typically 5 to 12V
8	V_{SS}	Negative power supply. Typically −5 to −12V
16	V_{CC}	Digital power supply. This pin is connected to the logic power supply (Max. 5.5V). V_{CC} must be less than or equal to V_{DD}
9	GND	Ground. All voltage levels are referenced to this pin
10, 12, 14	DI1, DI2, DI3	Driver data input. These are the high impedance digital input pins. These input levels are compatible with TTL
3, 5, 7	Tx1, Tx2, Tx3	Transmit data output. These are the RS-232-C transmit signal output pins. A logic "0" causes the output to swing to V_{DD} and a logic "1" causes the output to swing to V_{SS}
2, 4, 6	Rx1, Rx2, Rx3	Receive data input. These are the RS-232-C receive signal input pins which swing from +25 to −25V. A voltage between +3 and +25V causes the correspanding DO pin to swing to GND and a voltage between −3 and −25V causes the DO pin to swing to V_{CC}
11, 13, 15	DO1, DO2, DO3	Receive data output. Swing from V_{CC} to GND. Each output pin is capable of driving TTL input load

QUAD CMOS LINE DRIVER

The KS5788 is designed to interface data terminal equipment (DTE) with data communications equipment (DCE) in conformance with the specifications of EIA RS-232-C, CCITT V.24 standards. The KS5788 is direct replacement for the bipolar device (MC1488).



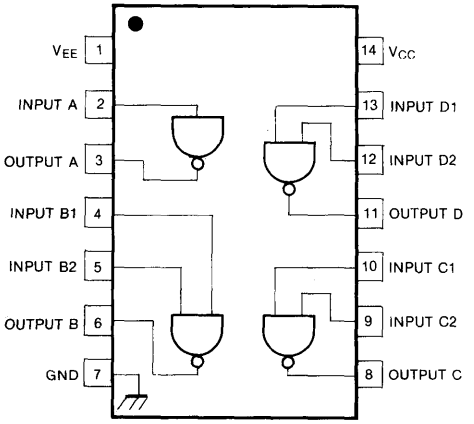
FEATURES

- **Low power consumption & low delay slew**
- **Pin for pin equivalent to MC1488**
- **Power-off source impedance: 300Ω (min)**
- **Compatible with TTL and HCTLS families**
- **Flexible operating supply range: 4.5~12.6V**

ORDERING INFORMATION

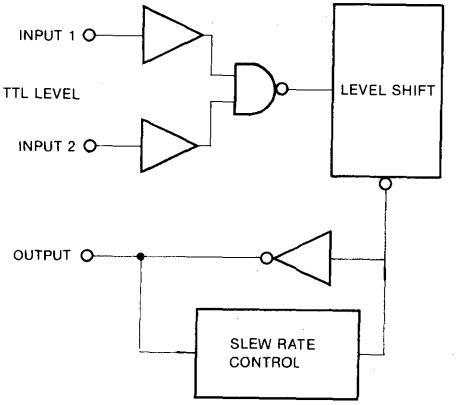
Device	Package	Operating Temperature
KS5788N	14 DIP	−40 ~ +85°C
KS5788D	14 SOP	

PIN CONFIGURATION



BLOCK DIAGRAM

(1/4 OF CIRCUIT SHOWN)



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	−0.5 ~ 13.5 0.5 ~ −13.5	V_{dc}
Input Voltage (Any Input Pin)	V_{IN}	−0.3 ~ V_{CC} + 0.3	V_{dc}
Output Voltage (Any Output Pin)	V_{OUT}	−25 ~ 25	V_{dc}
Power Dissipation	P_D	1.0	W
Operating Temperature	T_a	−40 ~ 85	°C
Storage Temperature	T_{stg}	−65 ~ 150	°C

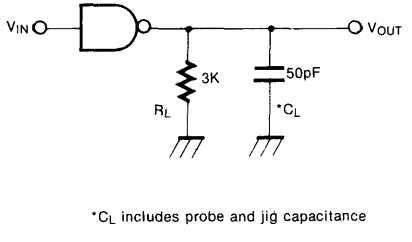
ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5 to 12V, V_{EE} = −4.5 to −12V, GND = 0V, Ta = −40° to 85°C, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITIONS						
Power Supply Voltage V_{CC} V_{EE}	V_{CC} V_{EE}		4.5 −4.5		12.6 −12.6	V_{dc}
DC ELECTRICAL CHARACTERISTICS						
Input Current 1	I_{IL}	V_{IN} = GND	−10		10	μA
Input Current 2	I_{IH}	V_{IN} = V_{CC}	−10		10	μA
Positive Supply Current 1 (V_{IN} = V_{IL}, R_L = ∞, per package)	I_{CC1}	V_{CC} = 4.5V, V_{EE} = −4.5V V_{CC} = 9.0V, V_{EE} = −9.0V V_{CC} = 12.0V, V_{EE} = −12.0V			10 30 60	μA μA μA
Positive Supply Current 2 (V_{IN} = V_{IH}, R_L = ∞, per package)	I_{CC2}	V_{CC} = 4.5V, V_{EE} = −4.5V V_{CC} = 9.0V, V_{EE} = −9.0V V_{CC} = 12.0V, V_{EE} = −12.0V			30 190 425	μA μA μA
Negative Supply Current 1 (V_{IN} = V_{IL}, R_L = ∞, per package)	I_{EE1}	V_{CC} = 4.5V, V_{EE} = −4.5V V_{CC} = 9.0V, V_{EE} = −9.0V V_{CC} = 12.0V, V_{EE} = −12.0V			−10 −10 −10	μA μA μA
Negative Supply Current 2 (V_{IN} = V_{IH}, R_L = ∞, per package)	I_{EE2}	V_{CC} = 4.5V, V_{EE} = −4.5V V_{CC} = 9.0V, V_{EE} = −9.0V V_{CC} = 12.0V, V_{EE} = −12.0V			−30 −30 −60	μA μA μA
Input Voltage High	V_{IH}		2.0		V_{DD}	V_{dc}
Input Voltage Low	V_{IL}	$V_{CC} \geqq 7V$, $V_{EE} \leqq -7V$ $V_{CC} \leqq 7V$, $V_{EE} \geqq -7V$	GND GND		0.8 0.6	V_{dc}

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High ($V_{IN}=V_{IL}$, $R_L=3K\Omega\sim7K\Omega$)		V_{OH}	$V_{CC}=4.5V$, $V_{EE}=-4.5V$ $V_{CC}=9.0V$, $V_{EE}=-9.0V$ $V_{CC}=12V$, $V_{EE}=-12V$	3.0 6.5 9.0			V_{dc}
Output Voltage Low ($V_{IN}=V_{IH}$, $R_L=3K\Omega\sim7K\Omega$)		V_{OL}	$V_{CC}=4.5V$, $V_{EE}=-4.5V$ $V_{CC}=9.0V$, $V_{EE}=-9.0V$ $V_{CC}=12V$, $V_{EE}=-12V$			-3.0 -6.5 -9.0	V_{dc}
Output Short Circuit Current	$V_{IN}=V_{IL}$	I_{OS}	$V_O=GND$			45	mA
	$V_{IN}=V_{IH}$		$V_{CC}=12V$, $V_{EE}=-12V$			-45	
Power Off Output Resistance		R_O	$V_{CC}=V_{EE}=0V$, $V_{OUT}=\pm2V$	300			Ω
SWITCHING CHARACTERISTICS ($V_{CC}=4.5V$ to $12V$, $V_{EE}=-4.5V$ to $-12V$, $Ta=-40°C\sim85°C$, Fig. 1)							
Propagation Delay		t_{pd}	$V_{CC}=4.5V$, $V_{EE}=-4.5V$ $V_{CC}=9.0V$, $V_{EE}=-9.0V$ $V_{CC}=12V$, $V_{EE}=-12V$			6.0 5.0 4.0	μS
Output Rise Time		t_r	V_{OUT} = from $-3V$ to $3V$	0.2			μS
Output Fall Time		t_f	V_{OUT} = from $3V$ to $-3V$	0.2			μS
Output Slew Rate		S_R	$R_L=3K\Omega$ to $7K\Omega$ $15pF<C_L<2.5nF$			30	V/μS
Typical Propagation Delay Skew		t_{SK}	$V_{CC}=12V$, $V_{EE}=-12V$		400		nS



*C_L includes probe and jig capacitance

Fig. 1 AC Test Circuit

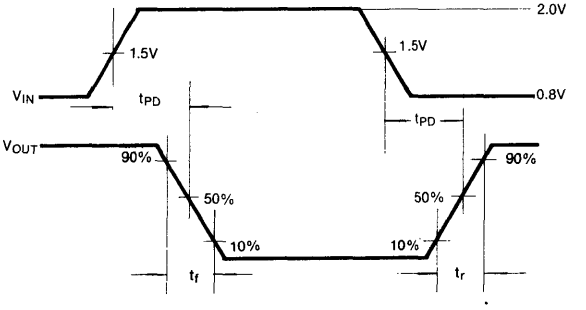
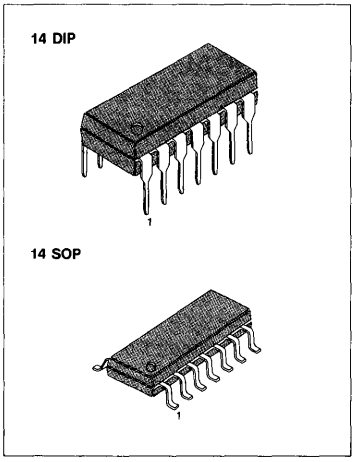


Fig. 2 Switching Waveforms

QUAD CMOS LINE RECEIVER

The KS5789A is designed to interface data terminal equipment (DTE) with data communications equipment (DCE) in conformance with the specifications of EIA RS-232-C, CCITT V.24 standards. The KS5789A is direct replacement for the bipolar device (MC1489/A).



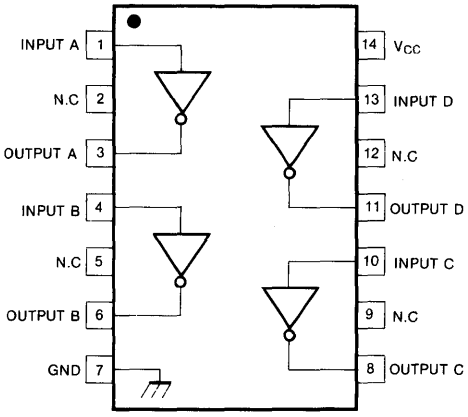
FEATURES

- **Low power consumption & low delay slew**
- **Pin for pin equivalent to MC1489/A**
- **Inputs withstand ±30V**
- **Fail-safe operating mode**
- **Internal noise filter**
- **Internal input threshold with hysteresis**

ORDERING INFORMATION

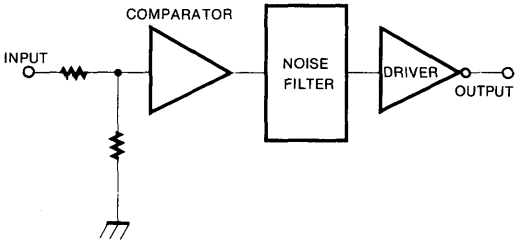
Device	Package	Operating Temperature
KS5789AN	14 DIP	−40 ~ +85°C
KS5789AD	14 SOP	

PIN CONFIGURATION



BLOCK DIAGRAM

(1/4 OF CIRCUIT SHOWN)



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 ~ 7.0	V_{dc}
Input Voltage	V_{IN}	−30 ~ 30	V_{dc}
Output Voltage	V_{OUT}	−0.3 ~ V_{CC} + 0.3	V_{dc}
Power Dissipation (85°C)	P_D	500	mW
Operating Temperature	T_a	−40 ~ 85	°C
Storage Temperature	T_{stg}	−65 ~ 150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 0.5V, Ta = −40° to 85°C, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
DC ELECTRICAL CHARACTERISTICS						
Input Voltage High	V_{IH}		1.3		2.5	V_{dc}
Input Voltage Low	V_{IL}		0.5		1.7	V_{dc}
Input Hysteresis Voltage	V_H	$V_{IH} - V_{IL}$		1.0		V_{dc}
Input Current	I_{IN}	V_{IN} = 3V V_{IN} = −3V V_{IN} = 25V V_{IN} = −25V	0.43 −0.43 3.6 −3.6		1.0 −1.0 8.3 −8.3	mA
Output Voltage High	V_{OH}	$V_{IN} = V_{IL(min)}$, I_{OUT} = −3.2mA	2.8			V_{dc}
Output Voltage Low	V_{OL}	$V_{IN} = V_{IH(max)}$, I_{OUT} = 3.2mA			0.4	V_{dc}
Supply Current	I_{CC}	$R_L = \infty$, $V_{IN} = V_{IL(min)}$ to $V_{IH(max)}$			600	μA
SWITCHING CHARACTERISTICS (V_{CC} = 4.5V to 5.5V, Ta = −40°~85°C, C_L = 50pF, Note 1)						
Propagation Delay	t_p	Input pulse width ≧ 10μS			6.5	μS
Output Rise Time	t_r				300	nS
Output Fall Time	t_f				300	nS
Pulse Width Assumed to be Noise	t_{nw}				1.0	μS
Propagration Delay Skew	t_{sk}			400		nS

Note 1: Test waveform $t_r = t_f$ = 200ns, V_{IH} = +3V, V_{IL} = −3V, f = 20KHz

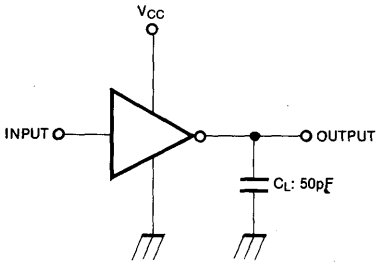


Fig. 1 AC Test Circuit

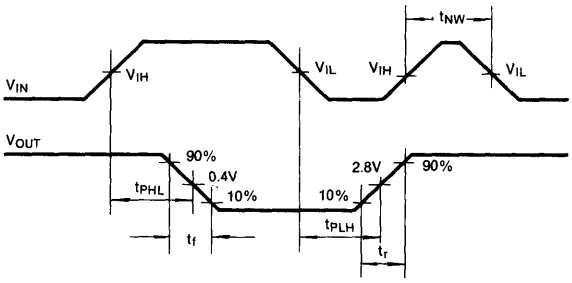
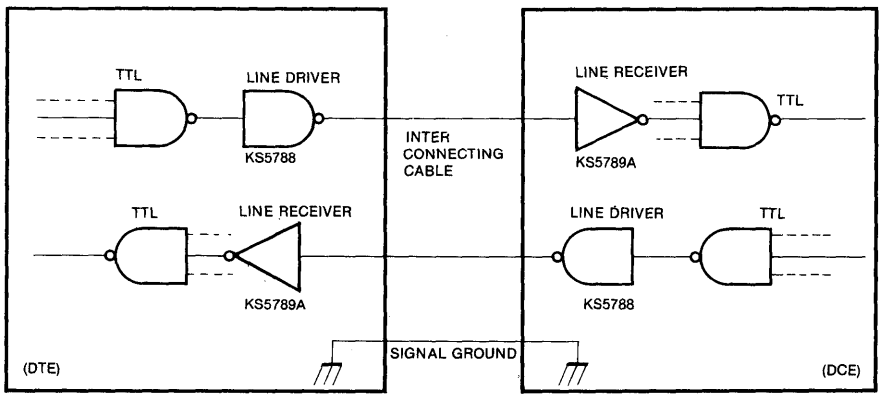


Fig. 2 Switching Waveforms

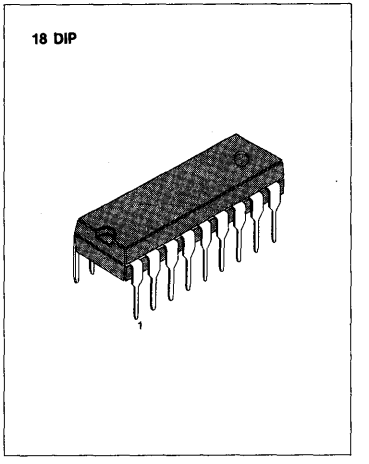
TYPICAL APPLICATION



RS-232-C Data Transmission

TELEPHONE PULSE DIALER WITH REDIAL

The KS5805A/B is a monolithic CMOS integrated circuit and provides all the features required for implementing a pulse dialer with redial.



FUNCTIONS

- $\overline{\text{Mute}}$ output logic "0"
- $\overline{\text{Pulse}}$ output logic "0"
- RC oscillation for reference frequency
- Designed to operate directly from the telephone line
- Used CMOS technology for low voltage, low power operation
- Power up clear circuitry
- KS5805A pin 2: V_{REF}
- KS5805B pin 2: Tone out

FEATURES

- **Uses either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard**
- **Make/Break ratio can be selected**
- **Redial with * or #**
- **Continuous $\overline{\text{MUTE}}$**
- **Tone signal output or on-chip reference Voltage by bonding option on chip**
- **10 pps/20 pps can be selected**

ORDERING INFORMATION

Device	Package	Function	Operating Temperature
KS5805AN	18 DIP	Pin 2 = V_{ref}	−30 ~ +60°C
KS5805BN	18 DIP	Pin 2 = Tone Out	

TEST CIRCUIT

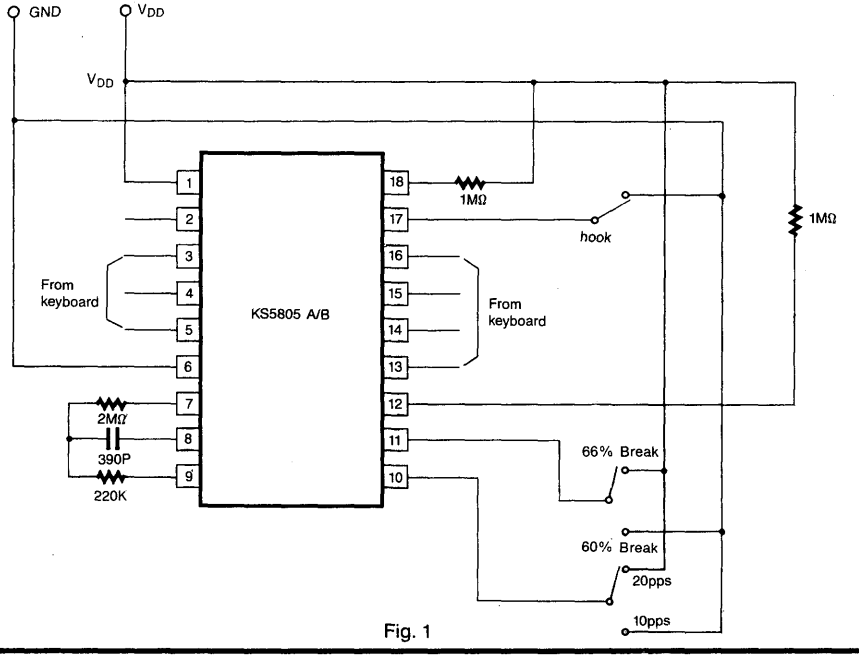


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	6.2	V
Voltage on Any Pin	V_{IN}	V_{DD} +0.3, Gnd−0.3	V
Power Dissipation	P_D	500.0	mW
Operating Temperature	Topr	−30 ~ +60	°C
Storage Temperature	Tstg	−65 ~ +150	°C

DC ELECTRICAL CHARACTERISTICS

(T_a =25°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}		2.5		6.0	V	
Key Contract Resistance	R_{KI}				1	KΩ	1
Keyboard Capacitance	C_{KI}				30	pF	
Key Input Voltage	K_{IH}	2 of 7 input mode	0.8V_{DD}		V_{DD}	V	1
	K_{IL}		Gnd		0.2V_{DD}		
Key Pull-Up Resistance	K_{IRU}	V_{DD} = 6.0V		100		KΩ	
Key Pull-Down Resistance	K_{IRD}	V_{IN} = 4.8V		4.0		KΩ	
Mute Sink Current	I_M	V_{DD} = 2.5V V_O = 0.5V	500			μA	2
Pulse Output Sink Current	I_P	V_{DD} = 2.5V V_O = 0.5V	1.0			mA	3
Tone Output Sink Current	I_{TL}	V_{DD} = 2.5V V_O = 0.5V	250			μA	4
Tone Output Source Current	I_{TH}	V_{DD} = 2.5V V_O = 0.5V	250			μA	4
Memory Retention Current	I_{MR}	All outputs under no load		0.7		μA	6
Operating Current	I_{OP}	All outputs under no load		100	150	μA	
Mute or Pulse Off Leakage	I_{LKG}	V_{DD} = 6.0V V_O = 6.0V		0.001	1.0	μA	2.3
V_{REF} Output Source Current	I_{REF}	V_{DD} − V_{REF} = 6.0V	1.0	7.0		mA	5

Note 1) Applies to key input pin. (R_1-R_4, C_1-C_3)
2) Applies to MUTE output in.
3) Applies to PULSE output pin.
4) Applies to TONE pin (KS5805B)
5) Applies to V_{REF} pin (KS5805A)
6) Current necessary for memory to be maintained. All outputs unloaded.

* Typical values are to be used as a design aid are not subject to production testing.

AC ELECTRICAL CHARACTERISTICS (T_a =25°C)

Charactistic	Symbol	Min	Typ	Max	Unit	Notes
Oscilator Frequency	F_{OSC}		4		KHz	1
Key Input Debounce Time	T_{DB}		10		ms	3,4
Key Down Time for Valid Entry	T_{KD}	40			ms	4,5
Key Down Time During Two-Key Roll Over	t_{KR}	5			ms	4
Oscillator Stat-Up Time (V_{DD} = 2.5V)	t_{os}		1		ms	
Mute Valid After Last Outpulse	t_{MO}		5		ms	3,4
Pulse Output Pulse Rate	P_R		10		PPS	2
On-Hook Time Required to Clear Memory	t_{OH}	300			ms	4
Pre-Digital Pause	T_{PDP}		800		ms	3,4
Inter-Digital Pause	T_{IDP}		800		ms	3,4
Frequency Stability V_{DD} = 2.5 ~ 3.5V	Δf		±4		%	
Frequency Stability V_{DD} = 3.5 ~ 6.0V	Δf		±4		%	
Tone Output Frequency	F_{TONE}		1		KHz	4,6

Note: 1) R_S =2MΩ, R=220KΩ, C=390pF.
2) If pin 10 is tied to V_{CC}, the output pulse rate will be 20pps.
3) If the 20pps option is selected, the time will be 1/2 these shown.
4) These times are directly proportional to the oscillator frequency.
5) Debounce plus oscillator start-up time ≤ 40ms.
6) If the 20pps option is selected, the tone output frequency will be 2KHz. (KS5805B ONLY)

PIN CONNECTIONS

Pin 1: V_{DD}
Pin 2: V_{ref} (KS5805A)/Pacifier tone (KS5805B)
Pin 3: $\overline{\text{Column 1}}$
Pin 4: $\overline{\text{Column 2}}$
Pin 5: $\overline{\text{Column 3}}$
Pin 6: GND
Pin 7: RC Oscillator
Pin 8: RC Oscillator
Pin 9: RC Oscillator
Pin 10: 10/20pps Select
Pin 11: Make/Break Select
Pin 12: $\overline{\text{Mute}}$ Output
Pin 13: $\overline{\text{ROW 4}}$
Pin 14: $\overline{\text{ROW 3}}$
Pin 15: $\overline{\text{ROW 2}}$
Pin 16: $\overline{\text{ROW 1}}$
Pin 17: On-Hook/Test
Pin 18: $\overline{\text{Pulse}}$ $\overline{\text{Output}}$

TIMING CHARACTERISTICS

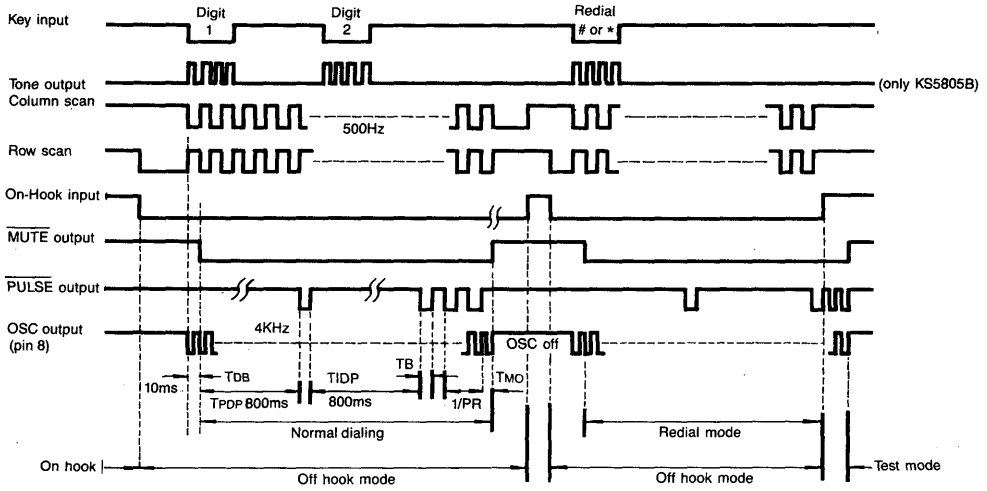


Fig. 2

PIN DESCRIPTIONS

1. V_{DD} (Pin 1)

This is positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150μA current source. This voltage should be regulated to less than 6.0 volts using on external form or regulation.

2. Tone signal output/V_{REF} (Pin 2)

Tone signal out pin is CMOS comperementaly output and drives external bipolar transistor. This pin generates a tone signal when a key is depressed. Tone signal frequency is 1KHz when 10pps pulse rate is selected. (the frequency is 2KHz when 20pps pulse rate is selected). Only the pin 2 of KS5805A is V_{REF} (on-chip reference voltage).

TYPICAL I-V CHARACTERISTICS

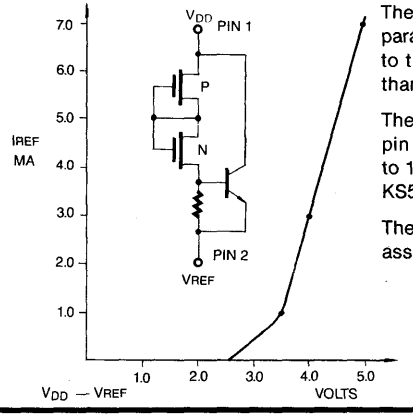


Fig. 3

The V_{REF} output provides a reference voltage that tracks internal parameters of the KS5805A. V_{REF} provides a negative voltage reference to the V_{DD} supply. Its magnitude will be approximately 0.6 volt higher than the minimum operating voltage of each particular KS5805A.

The typical application would be to connect the V_{REF} pin to the GND pin (Pin 6). The supply to the V_{DD} pin (Pin 1) should then be regulated to 150μA (I_{OP} max). With this amount of supply current, operation of the KS5805A is guaranteed.

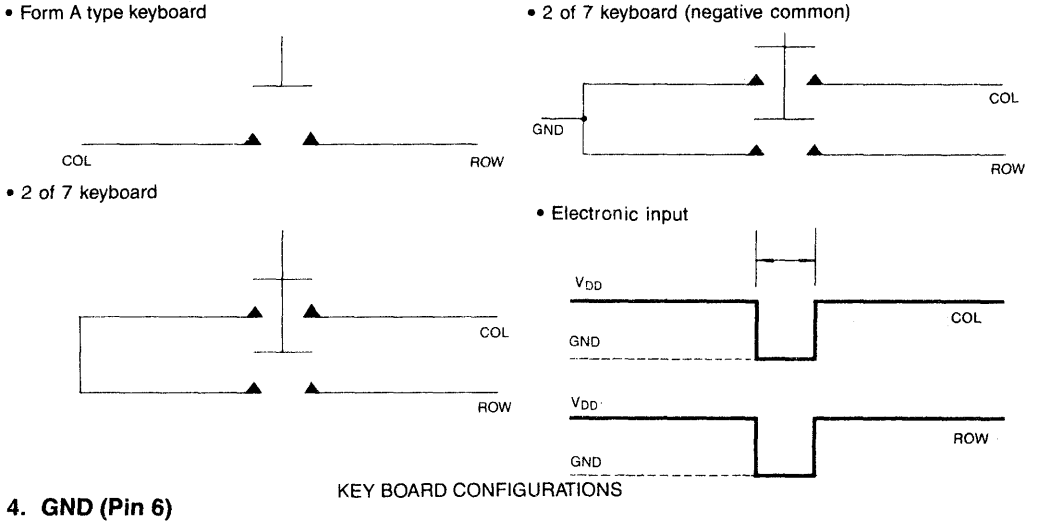
The internal circuit of the V_{REF} function is shown in Figure 3 with its associated I-V characteristic.

3. Keyboard inputs (Pin 3, 4, 5, 13, 14, 15, 16,)

The KS5805A/B incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used.

A valied key entry is defined by either a single row being connected to a single column or GND being simultaneously presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high and no keyboard inputs are accepted.

When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are scanned alternately (pulled high, then low) to verify the varied input. The input must remain valid for 10msec of debounce time to be accepted.



KEY BOARD CONFIGURATIONS

4. GND (Pin 6)

This is the negative supply pin and is connected to the common part in the general applications.

5. OSCILLATOR (Pins 7, 8, 9)

The KS5805A/B contains on-chip inverters to provide oscillator which will operate with a minimum external components.

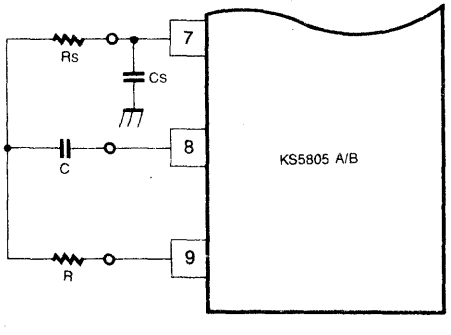
Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K=R_S/R$ equal to 10.

The oscillator period is given by:

$$T=RC\,(1.386+(3.5KC_S)/C-(\pm K/(K+1))\,\ln\,(K/(1.5K+0.5))$$

Where C_S is the stray capacitance on Pin 7.

Accuracy and stability will be enhanced with this capacitance minimized.



6. 20/10 pps (Pin 10)

Connecting this pin to GND (pin 6) will select an output pulse rate of 10pps.
Connecting the pin V_{DD} (pin 1) will select an output pulse rate of 20pps.

7. MAKE/BREAK (Pin 11)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connection V_{DD} or GND to this pin as shown in the following table.

Input	Make	Break
V_{DD} (Pin 1)	34%	66%
GND (Pin 6)	40%	60%

8. $\overline{\text{MUTE}}$ OUTPUT (Pin 12)

The $\overline{\text{mute}}$ output is an open-drain N-channel transistor designed to drive external bipolar transistor.
This circuitry is usually used to $\overline{\text{mute}}$ the receiver during outpulsing. As shown in Fig. 2 the KS5805 $\overline{\text{mute}}$ output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break.
The delay from the end of the last break until the $\overline{\text{mute}}$ output turns off is $\overline{\text{mute}}$ overlap and is specified as t_{MO}.

9. ON-HOOK/TEST (Pin 17)

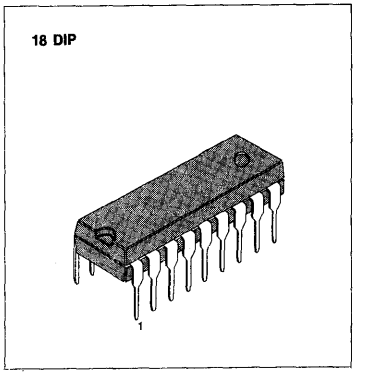
The "ON-HOOK" or "Test" input of the KS5805A/B has a 100KΩ pull-up to the positive supply. A V_{CC} input or allowing the pin to float sets the circuit in its on-hook or test mode while a V_{GND} input sets it in the off-hook or normal mode. When off-hook the KS5805A/B will accept key inputs and outputs the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.
Switching the KS5805A/B to on-hook while it is outpulsing causes the remaining digits to be outpulsed at 100x the normal rate (M/B ratio is then 50/50).
This feature provides a means of rapidly testing the device and is also on efficient method by which the circuitry is reset. When the outpulsing in this mode, which can be up to 300msec, is completed, the circuit is deactivated and will require current only necessary to sustain the memory and power-up-clear detect circuity (refer to the electrical specifications).
Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is eithr a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

10. $\overline{\text{PULSE}}$ OUTPUT (Pin 18)

The $\overline{\text{pulse}}$ output is an open drain N-channel transistor designed to drive external bipolar transistor. These transistor would normally be used to $\overline{\text{pulse}}$ the telephone line by disconnecting and connecting the network. The KS58A/B05 pulse output is an open circuit during make and pulls to the GND supply during break.

PULSE DIALER WITH REDIAL

The KS58C/D05 is a monolithic CMOS integrated circuit which uses an inexpensive RC oscillator for its frequency reference and provides all the features required for implementing a pulse dialer with 32 digit redial.



FUNCTIONS

- Mute output logic "0"
- Pulse output logic "0"
- RC oscillation for reference frequency
- Designed to operate directly from the telephone line
- Used CMOS technology for low voltage, low power operation

FEATURES

- **Wide operating voltage range (2.0 ~ 6.0V)**
- **Low power dissipation**
- **Use either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard**
- **Make/Break ratio can be selected**
- **Redial with * or #**
- **Continuous $\overline{\text{MUTE}}$**
- **Power up clear circuitry on chip**
- **KS58C05 pin 2: V_{ref}, KS58D05 pin 2: Tone output**
- **10 pps/20 pps can be selected**

ORDERING INFORMATION

Device	Package	Function	Operating Temperature
KS58C05N	18 DIP	Pin 2 = V_{ref}	−20 ~ +70°C
KS58D05N	18 DIP	Pin 2 = Tone Out	

TEST CIRCUIT

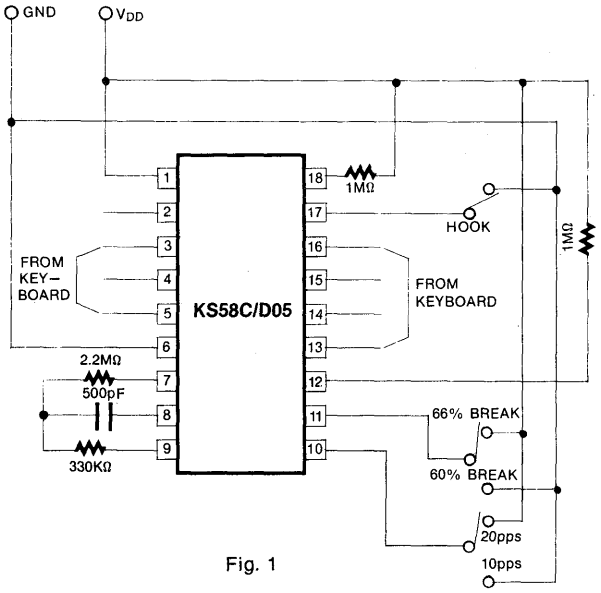


Fig. 1

PIN CONNECTIONS

Pin 1: V_{DD}
Pin 2: V_{ref} (KS58C05)/Pacifier tone (KS58D05)
Pin 3: $\overline{\text{Column 1}}$
Pin 4: $\overline{\text{Column 2}}$
Pin 5: $\overline{\text{Column 3}}$
Pin 6: GND
Pin 7: RC Oscillator
Pin 8: RC Oscillator
Pin 9: RC Oscillator
Pin 10: 10/20pps Select
Pin 11: Make/Break Select
Pin 12: $\overline{\text{Mute}}$ Output
Pin 13: $\overline{\text{ROW 4}}$
Pin 14: $\overline{\text{ROW 3}}$
Pin 15: $\overline{\text{ROW 2}}$
Pin 16: $\overline{\text{ROW 1}}$
Pin 17: On-Hook/Test
Pin 18: $\overline{\text{Pulse}}$ Output

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.2	V
Input Voltage	V_{IN}	Gnd – 0.3, V_{DD} + 0.3	V
Output Voltage	V_{OUT}	Gnd – 0.3, V_{DD} + 0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_a	– 20 ~ + 70	°C
Storage Temperature	T_{stg}	– 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.5V, f_{OSC} = 2.4KHz, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.0		6.0	V
Memory Retention Voltage	V_{DR}		1.0			V
Input High Voltage	V_{IH}	$\overline{R_1} \sim \overline{R_4}$, $\overline{C_1} \sim \overline{C_4}$, $\overline{HS}$, DRS, M/B	0.8V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL}		Gnd		0.2V_{DD}	V
Operating Current	I_{DD}	All output under no load		100	150	μA
Output Leakage Current	I_{OL}	V_{CC} = 6.0V, $\overline{MUTE}$, $\overline{PULSE}$ = 6.0V		0.001	1	μA
Output Current ($\overline{MUTE}$, $\overline{PULSE}$)	I_{O1}	V_O = 0.4V, V_{DD} = 2.5V	0.5	1.5		mA
	I_{O2}	V_O = 0.4V, V_{DD} = 3.5V	1.7	5.0		mA
Oscillator Frequency	f_{OSC}			2.4		KHz
Valid Key Entry Time	T_{KD}		14		20	mS
On Hook Time Required to Clear Memory	T_{OH}		300			mS
Inter Digital Pause	T_{IDP}			800		mS
Frequency Stability	△f	V_{DD} = 2.0 ~ 6.0V		± 10		%
Tone Output Frequency	f_{TONE}			1.2		KHz

FUNCTION DESCRIPTION

1. "ON-HOOK" MODE

When "ON-HOOK," key inputs will not be recognized because the oscillator is disabled which prevents the circuit from drawing excessive current.

2. "DIAL" MODE

When "OFF-HOOK," the device senses key down condition by detecting one key input and enters the key's code into an on-chip memory.

The memory can be store up to 32 digits, and it allows key strobes to be entered at rates comparable to tone dialing telephone. Output pulsing will continue until all entered digits have been dialed. To implement the pulse dialer function, two outputs, one to pulse the telephone line and one to mute the receiver, are provided.

3. "REDIAL" MODE

The first 32 digits entered will be stored in the on-chip redial memory and can be redialed by pressing either * or #, provided that the receiver is "ON-HOOK" for minimum T_{OH} (on hook time required to clear memory).

4. POWER UP CLEAR

The on-chip "POWER UP CLEAR" circuit reliable operation of the device. If the supply to the circuit is not sufficient to retain data in the memory, a "POWER UP CLEAR" will help regaining a proper supply level.

This function will prevent the "Redial" or spontaneous outputing of incorrect data.

TIMING CHARACTERISTICS

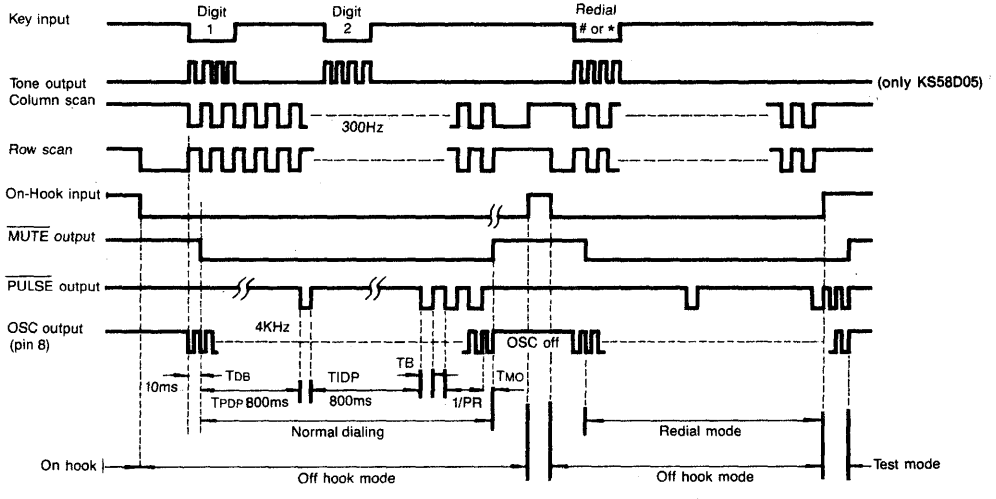


Fig. 2

PIN DESCRIPTIONS

1. V_{DD} (Pin 1)

This is positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150μA current source. This voltage should be regulated to less than 6.0 volts using on external form or regulation.

2. Tone signal output/V_{REF} (Pin 2)

Tone signal out pin is CMOS complementally output and drives external bipolar transistor. This pin generates a tone signal when a key is depressed. Tone signal frequency is 1.2KHz when 10pps pulse rate is selected.

TYPICAL I-V CHARACTERISTICS

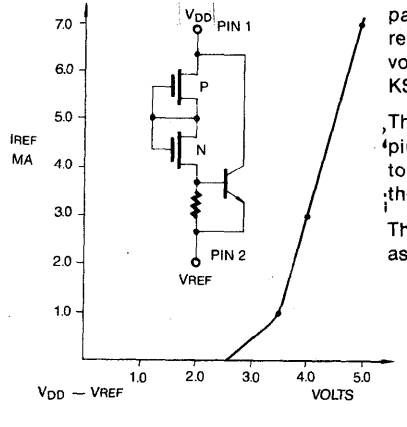


Fig. 3

The V_{REF} output provides a reference voltage that tracks internal parameters of the KS58C05. V_{REF} provides a negative voltage reference to the V_{DD} supply. Its magnitude will be approximately 0.6 volt higher than the minimum operating voltage of each particular KS58C05.

The typical application would be to connect the V_{REF} pin to the GND pin (Pin 6). The supply to the V_{DD} pin (Pin 1) should then be regulated to 150μA (I_{OP} max). With this amount of supply current, operation of the KS58C05 is guaranteed.

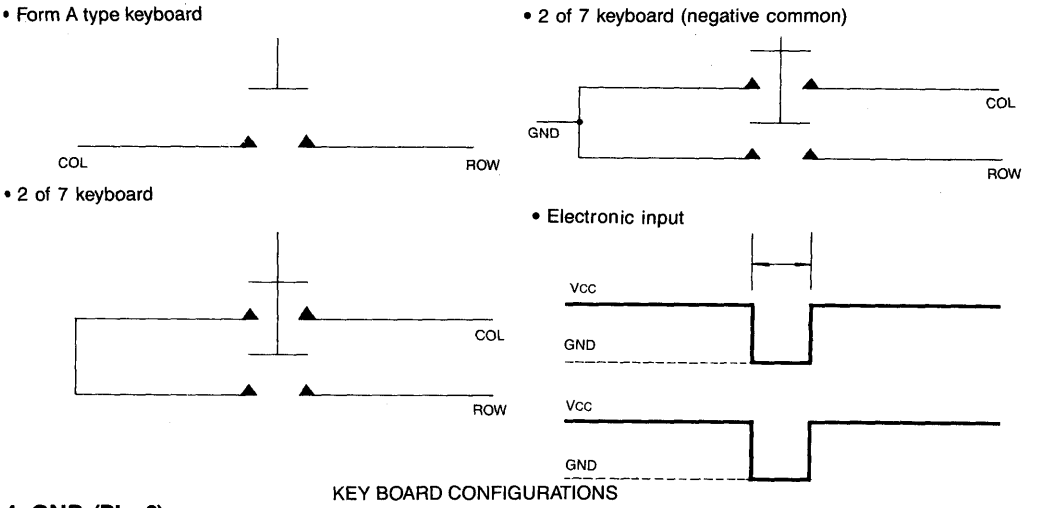
The internal circuit of the V_{REF} function is shown in Figure 3 with its associated I-V characteristic.

3. Keyboard inputs (Pin 3, 4, 5, 13, 14, 15, 16)

The KS58C/D05 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used.

A valied key entry is defined by either a single row being connected to a single column or GND being simultaneously presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high are no keyboard inputs are accepted.

When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are scanned alternately (pulled high, then low) to verify the varied input. The input must remain valid for 14-20 msec of debounce time to be accepted.



KEY BOARD CONFIGURATIONS

4. GND (Pin 6)

This is the negative supply pin and is connected to the common part in the general applications.

5. OSCILLATOR (Pin 7, 8, 9)

The KS58C/D05 contains on-chip inverters to provide oscillator which will operate with a minimum external components.

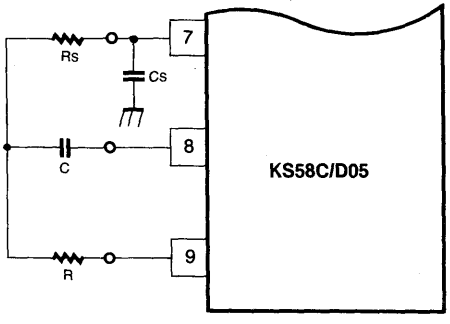
Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K = R_S/R$ equal to 6.67.

The oscillator period is given by:

$$T = RC\ \{1.386 + (3.5K_{CS})/C\text{-}(2K/CK + 1)\ \text{In}\ CK/(1.5K + 0.5)\}$$

Where C_S is the stray capacitance on Pin 7.

Accuracy and stability will be enhanced with this capacitance minimized.



6. 20/10 pps (Pin 10)

Connecting this pin to GND (pin 6) will select an output pulse rate of 10pps.
Connecting the pin V_{DD} (pin 1) will select an output pulse rate of 20pps.

7. MAKE/BREAK (Pin 11)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connection V_{DD} or GND to this pin as shown in the following table.

Input	Make	Break
V_{DD} (Pin 1)	33.4%	66.6%
GND (Pin 6)	40%	60%

8. $\overline{\text{MUTE}}$ OUTPUT (Pin 12)

The mute output is an open-drain N-channel transistor designed to drive external bipolar transistor.
This circuitry is usually used to mute the receiver during outpulsing. As shown in Fig. 2 the KS58C/D05 $\overline{\text{mute}}$ output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break.
The delay from the end of the last break until the $\overline{\text{mute}}$ output turns off is $\overline{\text{mute}}$ overlap and is specified as t_{MO}.

9. ON-HOOK/TEST (Pin 17)

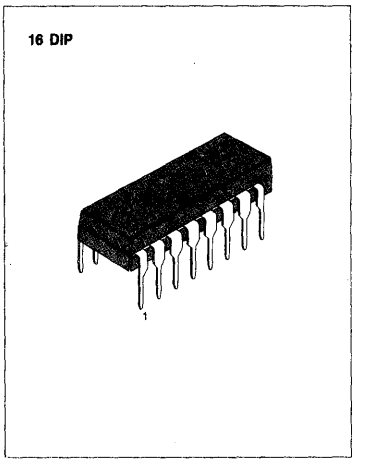
This pin detects the state of the hook switch contact "OFF HOOK" corresponds to V_{SS} condition. "ON HOOK" corresponds to V_{DD} condition. When outpulsing in this mode, which can be up to 300msec, is completed, the circuit is deactivated and will require current only necessary to sustain the memory and power-up-clear detect circuitry (refer to the electrical specifications).
Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

10. $\overline{\text{PULSE}}$ OUTPUT (Pin 18)

The $\overline{\text{pulse}}$ output is an open drain N-channel transistor designed to drive external bipolar transistor. These transistor would normally be used to pulse the telephone line by disconnecting and connecting the network. The KS58C/D05 $\overline{\text{pulse}}$ output is an open circuit during make and pulls to the GND supply during break.

PULSE DIALER WITH REDIAL

The KS58E05 is a monolithic CMOS integrated circuit which uses an inexpensive RC oscillator for its frequency reference and provides all the features required for implementing a pulse dialer with 32 digit redial.



FUNCTIONS

- $\overline{\text{Mute}}$ output logic "0"
- $\overline{\text{Pulse}}$ output logic "0"
- RC oscillation for reference frequency
- Designed to operate directly from the telephone line
- Used CMOS technology for low voltage, low power operation

FEATURES

- **Wide operating voltage range (2.0 6.0V)**
- **Low power dissipation**
- **Use either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard**
- **Make/Break ratio can be selected**
- **Redial with * or #**
- **Continuous $\overline{\text{MUTE}}$**
- **Power up clear circuitry on chip**
- **10 pps only.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KS58E05N	16 DIP	−20 ~ +70°C

TEST CIRCUIT

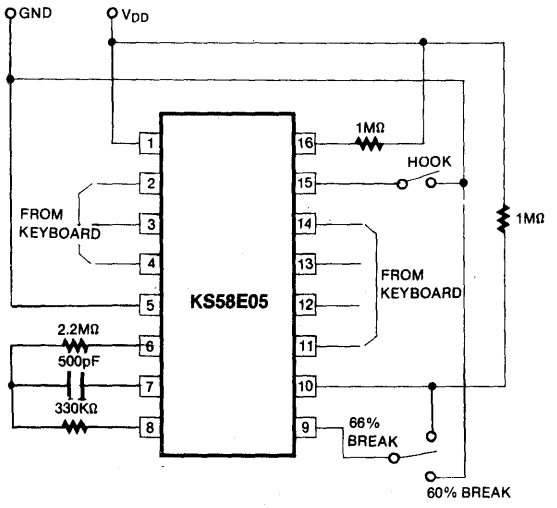


Fig. 1

PIN CONNECTIONS

Pin 1: V_{DD}
Pin 2: $\overline{\text{Column 1}}$
Pin 3: $\overline{\text{Column 2}}$
Pin 4: $\overline{\text{Column 3}}$
Pin 5: GND
Pin 6: RC Oscillator
Pin 7: RC Oscillator
Pin 8: RC Oscillator
Pin 9: Make/Break Select
Pin 10: $\overline{\text{Mute}}$ Output
Pin 11: $\overline{\text{ROW 4}}$
Pin 12: $\overline{\text{ROW 3}}$
Pin 13: $\overline{\text{ROW 2}}$
Pin 14: $\overline{\text{ROW 1}}$
Pin 15: On-Hook/Test
Pin 16: $\overline{\text{Pulse}}$ Output

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.2	V
Input Voltage	V_{IN}	GND – 0.3, V_{DD} + 0.3	V
Output Voltage	V_{OUT}	GND – 0.3, V_{DD} + 0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_a	– 20 ~ + 70	°C
Storage Temperature	T_{stg}	– 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.5V, f_{OSC} = 2.4KHz, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.0		6.0	V
Memory Retention Voltage	V_{DR}		1.0			V
Input High Voltage	V_{IH}	$\overline{R_1} \sim \overline{R_4}$, $\overline{C_1} \sim \overline{C_4}$, $\overline{HS}$, M/B	0.8V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL}		GND		0.2V_{DD}	V
Operating Current	I_{DD}	All output under no load		100	150	μA
Output Leakage Current	I_{OL}	V_{CC} = 6.0V, $\overline{MUTE}$, $\overline{PULSE}$ = 6.0V		0.001	1	μA
Output Current ($\overline{MUTE}$, $\overline{PULSE}$)	I_{O1}	V_O = 0.4V, V_{DD} = 2.5V	0.5	1.5		mA
	I_{O2}	V_O = 0.4V, V_{DD} = 3.5V	1.7	5.0		mA
Oscillator Frequency	f_{OSC}			2.4		KHz
Valid Key Entry Time	T_{KD}		14		20	mS
On Hook Time Required to Clear Memory	T_{OH}		300			mS
Inter Digital Pause	T_{IDP}			800		mS
Frequency Stability	$\triangle f$	V_{DD} = 2.0 ~ 6.0V		± 10		%
Tone Output Frequency	f_{TONE}			1.2		KHz

FUNCTION DESCRIPTION

1. "ON-HOOK" MODE

When "ON-HOOK," key inputs will not be recognized because the oscillator is disabled which prevents the circuit from drawing excessive current.

2. "DIAL" MODE

When "OFF-HOOK," the device senses key down condition by detecting one key input and enters the key's code into at on-chip memory.

The memory can be store up to 32 digits, and it allows key strobes to be entered at rates comparable to tone dialing telephone. Output pulsing will continue until all entered digits have been dialed. To implement the pulse dialer function, two outputs, one to pulse the telephone line and one to mute the receiver, are provided.

3. "REDIAL" MODE

The first 32 digits entered will be stored in the on-chip redial memory and can be redialed by pressing either * or #, provided that the receiver is "ON-HOOK" for minimum ton (on hook time required to clear memory).

4. POWER UP CLEAR

The on-chip "POWER UP CLEAR" circuit reliable operation of the device. If the supply to the circuit is not sufficient to retain data in the memory, a "POWER UP CLEAR" will help regaining a proper supply level.

This function will prevent the "Redial" or sportaneous outputing of incorrect data.

TIMING CHARACTERISTICS

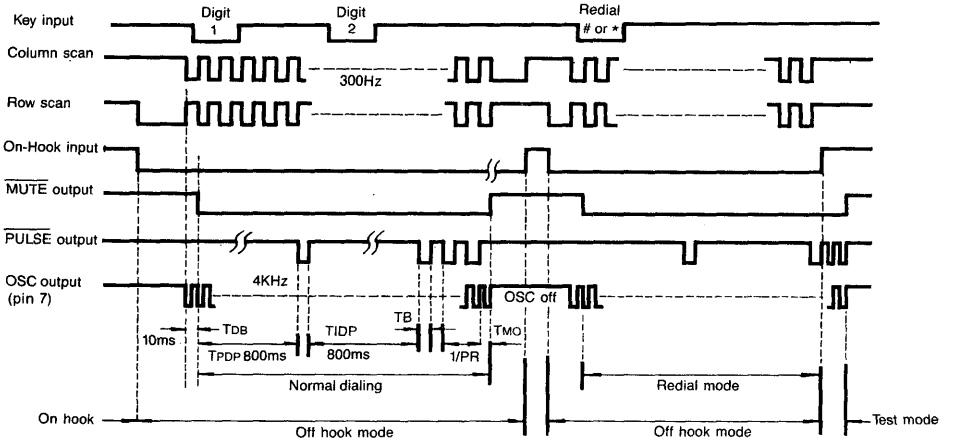


Fig. 2

1. V_{DD} (Pin 1)

This is positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150μA current source. This voltage should be regulated to less than 6.0 volts using on external form or regulation.

2. Keyboard inputs (Pin 2, 3, 4, 11, 12, 13, 14)

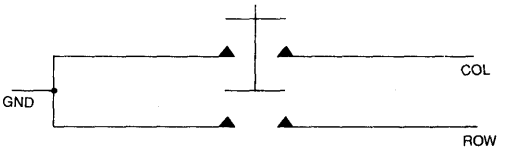
The KS58E05 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used.

A valied key entry is defined by either a single row being connected to a single column or GND being simultaneously presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high and no keyboard inputs are accepted.

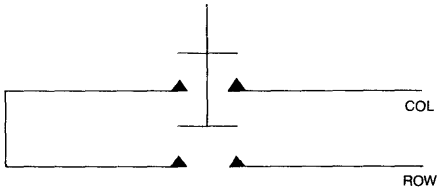
When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is varied. The input must remain valid continuously for 14-20 msec of debounce time to be accepted.

• Form A type keyboard

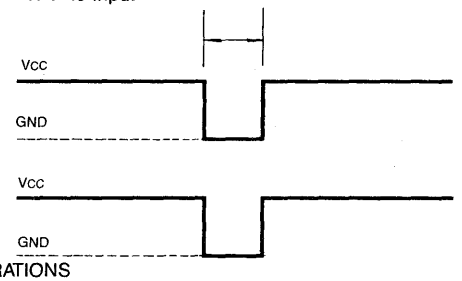
• 2 of 7 keyboard (negative common)



• 2 of 7 keyboard



• Electronic input



KEY BOARD CONFIGURATIONS

3. GND (Pin 5)

This is the negative supply pin and is connected to the common part in the general applications.

4. OSCILLATOR (Pin 6, 7, 8)

The KS58E05 contains on-chip inverters to provide oscillator which will operate with a minimum external components.

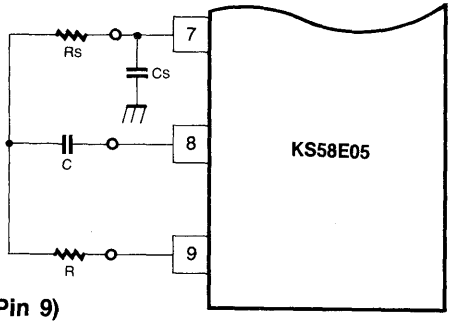
Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K = R_S/R$ equal to 6.67.

The oscillator period is given by:

$$T = RC\ \{1.386 + (3.5K_{CS})/C\text{-}(2K/CK + 1)\ \text{In}\ CK/(1.5K + 0.5)\}$$

Where C_S is the stray capacitance on Pin 6.

Accuracy and stability will be enhanced with this capacitance minimized.



5. MAKE/BREAK (Pin 9)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connection V_{DD} or GND to this pin as shown in the following table.

Input	Make	Break
V_{DD} (Pin 1)	33.4%	66.6%
GND (Pin 5)	40%	60%

6. $\overline{\text{MUTE}}$ OUTPUT (Pin 10)

The mute output is an open-drain N-channel transistor designed to drive external bipolar transistor.

This circuitry is usually used to mute the receiver during outpulsing. As shown in Fig. 2 the KS58E05 mute output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break.

The delay from the end of the last break until the mute output turns off is mute overlap and is specified as t_{MO}.

7. ON-HOOK/TEST (Pin 15)

This pin detects the state of the hook switch contact "OFF HOOK" corresponds to V_{SS} condition. "ON HOOK" corresponds to V_{DD} condition. When outpulsing in this mode, which can be up to 300msec, is completed, the circuit is deactivated and will require current only necessary to sustain the memory and power-up-clear detect circuitry (refer to the electrical specifications).

Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

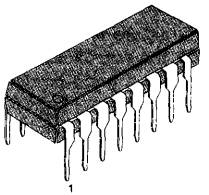
8. $\overline{\text{PULSE}}$ OUTPUT (Pin 16)

The pulse output is an open drain N-channel transistor designed to drive external bipolar transistor. These transistor would normally be used to pulse the telephone line by disconnecting and connecting the network. The KS58E05 pulse output is an open circuit during make and pulls to the GND supply during break.

DUAL TONE MULTI FREQUENCY DIALER

The KS5808 is a monolithic integrated circuit fabricated using CMOS process and is designed specifically for integrated tone dialer applications.

16 DIP



FUNCTIONS

- Fixed supply operation
- Negative-true keyboard input
- Tone disable input
- Stable-output level

FEATURES

- **Minimum number of external parts required.**
- **High accuracy tones.**
- **Digital divider logic, resistive ladder network and CMOS operational amplifier on single chip.**
- **Uses inexpensive 3.579545 MHz television color burst crystal.**
- **Invalid key entry can result in either single tone or no tone.**
- **Tone disable allows any key down output to function from keyboard input without generating tones.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KS5808N	16 DIP	−30 ~ +60°C

BLOCK DIAGRAM

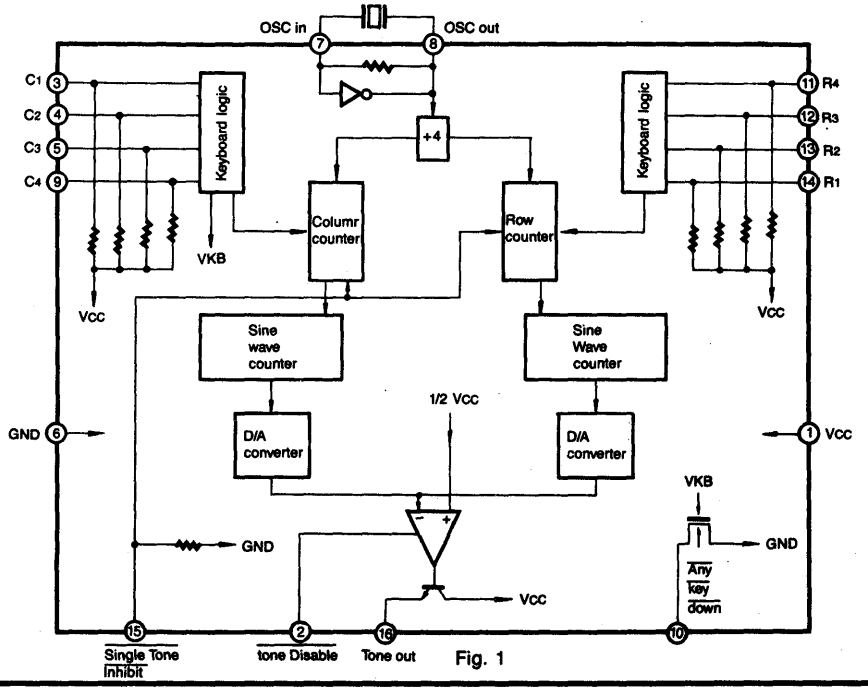


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10.5	V
Any Input Relative to V_{CC} (Except Pin 10)	V_N	0.3	V
Any Input Relative to GND (Except Pin 10)	V_N	−0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	Topr	−30 ~ +60	°C
Storage Temperature	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(−30°C < T_a < 60°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		3		10	V
Input "0"	V_{IL}		0		0.3V_{CC}	V
Input "1"	V_{IH}		0.7V_{CC}		V_{CC}	V
Input Pull-Up Resister	R_I		20		100	KΩ
$\overline{\text{Tone Disable}}$	$\overline{TD}$	Note 4	0		0.3V_{CC}	V
Tone Output	V_{OUT}	Note 1	−10		−7	dBm
Preemphasis, High Band			2.4	2.7	3	dB
Output Distortion, Measured in Terms of Total Out-of-Band Power Relative to RMS sum of Row and Column fundamental Power		Note 2			−20	dB
Rise Time	T_{RISE}	Note 3		2.8	5	mS
$\overline{\text{Any Key Down}}$ Sink Current to GND	I_{AKD}	At V_{OUT} =0.5V	500			uA
$\overline{\text{ADK}}$ Off Leakage Current	I_{AKDO}	At V_{OUT} =5V			2	uA
Supply Current Operating	I_{SO}	At V_{CC} =3.5V Note 6			2	mA
Supply Current Standby	I_{SST}	At V_{CC} =10V Note 5			200	uA
Tone Output-No Key Down	NKD				−80	dBm

Note: 1. Single-tone, low-group. Any V_{CC} between 3.4V and 3.6V, odBm=0.775V, R_{LOAD} =10K see test circuit Fig 2.
2. Any dual-tone. Any V_{CC} between 3.4V to 10.0V.
3. Time from a valid keystroke with no bounce to allow the waveform to go from min to 90% of the final magnitude of either frequency. Crystal parameters defined as R_S=100Ω L=96mH, C=0.02pF, and C_n=5pF, $V_{CC} \cong$ 3.4V, f=3.57954MHz±0.02%.
4. Only tones will be disabled when $\overline{TD}$ is taken to logical "0". Other chip functions may activate. Pull-up resistor on $\overline{TD}$ input will meet same spec as other inputs. Logic 0=GND
5. Stand-by condition is defined as no keys activated, $\overline{TD}$=Logical 1, $\overline{\text{Single Tone Inhibit}}$=Logical 0.
6. One key depressed only. Outputs unloaded.

PIN CONNECTIONS

PIN 1: Supply Voltage V_{CC}
PIN 2: $\overline{\text{Tone Disable}}$ Input
PIN 3: $\overline{\text{Column Input}}$ C_1
PIN 4: $\overline{\text{Column Input}}$ C_2
PIN 5: $\overline{\text{Column Input}}$ C_3
PIN 6: GND
PIN 7: OSC IN
PIN 8: OSC OUT
PIN 9: $\overline{\text{Column Input}}$ C_4
PIN 10: $\overline{\text{Any Key Down}}$
PIN 11: $\overline{\text{Row Input}}$ R_4
PIN 12: $\overline{\text{Row Input}}$ R_3
PIN 13: $\overline{\text{Row Input}}$ R_2
PIN 14: $\overline{\text{Row Input}}$ R_1
PIN 15: $\overline{\text{Single Tone Inhibit}}$
PIN 16: Tone Output

Tone Output Test Circuit

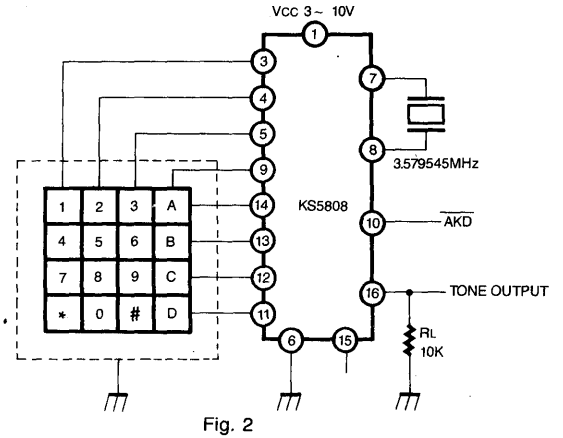


Fig. 2

FUNCTION DESCRIPTION

1. Oscillator

The network contains an on-board inverter with sufficient loop gain to provide oscillation when used with a low cost television color-burst crystal. The inverter's input is osc in (pin 7) and output is osc out (pin 8). The circuit is designed to work with a crystal cut to 3.579545MHz to give the frequencies in table 1. The oscillator is disabled whenever a keyboard input is not sensed.

Table 1: Standard DTMF and output frequencies of the KS5808

Item / Key	f	Standard DTMF Hz	Tone Output Frequency using 3.57954MHz Crystal Hz	Deviation from Standard %
ROW	f1	697	701.3	+0.62
	f2	770	771.4	+0.19
	f3	852	857.2	+0.61
	f4	941	935.1	−0.63
COL	f5	1209	1215.9	+0.57
	f6	1336	1331.7	−0.32
	f7	1477	1471.9	−0.35
	f8	1633	1645.0	+0.73

Most crystals don't vary more than 0.02%. Any crystal frequency deviation from 3.5795MHz will be reflected in the tone output frequency.

2. Output Waveform

The row and column output waveforms are shown in Figure 3. These waveforms are digitally synthesized using on-chip D/A converters. Distortion measurement of these unfiltered waveforms will show a typical distortion of 7% or less. The on-chip operational amplifier of the KS5808 mixes the row and column tones together to result in a dual-tone waveform.

Spectral analysis of this waveform will show that typically all harmonic and intermodulation distortion components will be -30dB down when referenced to the strongest fundamental (column tone). Figures 6 and 7 show a typical dual tone waveform and its spectral analysis.

Typical Sinewave Output

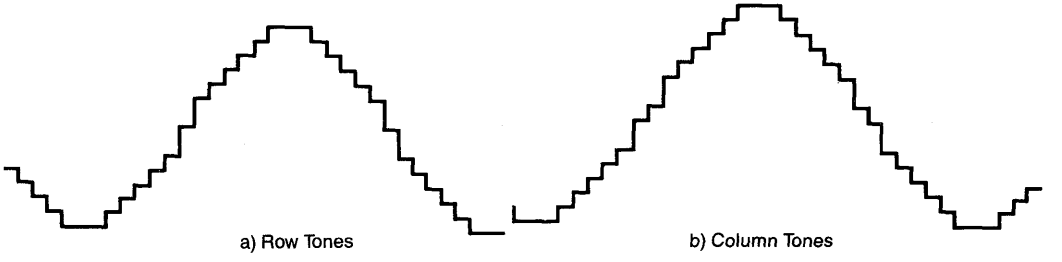


Fig. 3

3. Output Tone Level

The output tone level of the KS5808 is proportional to the applied DC supply voltage. Operation will normally be with a requlated supply. This results in enhanced temperature stability, since the supply voltage may be made temperature stable.

4. Keyboard Configuration

Each keyboard input is standard CMOS with a pull-up resistor to V_{CC}. These inputs may be controlled by a keyboard or electronic means. Open collector TTL or standard CMOS (operated off same supply as the KS5808) may be used for electronic control.

The switch contacts used in the keyboards may be void of precious metals, due to the CMOS network's ability to recognize resistance up to 1KΩ as a valid key closure.

2 of 8 DTMF keyboard

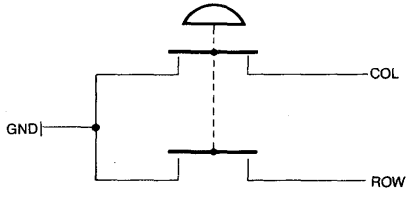


Fig. 4

Electronic Input Pulses

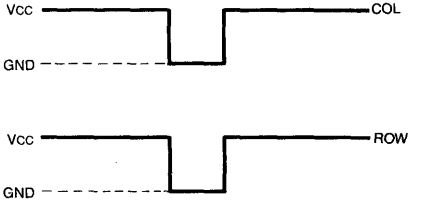


Fig. 5

TYPICAL DUAL TONE WAVEFORM

(ROW 1, Column 1)

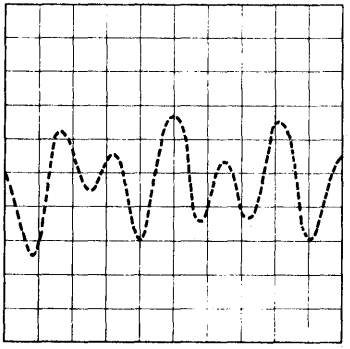


Fig. 6

SPECTRAL ANALYSIS OF WAVEFORM

(Vert: 10dB/Div, Horl: 1KHz/Div)

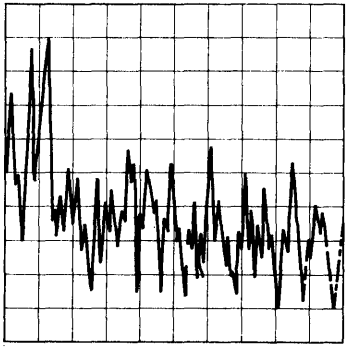


Fig. 7

POWER DISSIPATION VERSUS TEMPERATURE

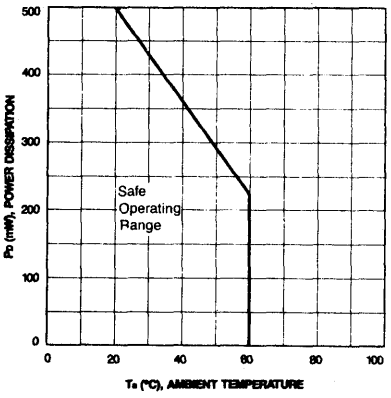


Fig. 8

PIN DESCRIPTIONS

1. Row and Column Input (Pin 3, 4, 5, 9, 11, 12, 13, 14)

With Single Tone Inhibit at V_{CC}, connection of GND to a single column will cause the generation of that column tone. Connection of GND to more than one column will result in no tones being generated. The application of GND to only a row pin or pins has no effect on the circuit. There must always be at least one column connected to GND for row tones to be generated. If a single row tone is desired, it mey be generated by tying any two column pins and the desired row pin to GND. Dual tones will be generated if a single row pin and a single column pin are connected to GND.

2. Any Key Down Output (Pin10)

The any key down output is used for electronic control of receiver and/or transmitter switching and other desired functions. It switches to GND when a keyboard button is pushed and is open circuited when not. The AKD output switches regardless of the tone disable and single tone inhibit inputs.

3. Tone Disable Input (Pin 2)

The Tone Disable input is used to defeat tone generation when the keyboard is used for other functions besides DTMF signaing. It has a pull-up to V_{CC} and when tied to GND tones are inhibited. All other chip functions operate normally.

4. Single Tone Inhibit Input (Pin 15)

The Single Tone Inhibit input is used to inhibit the generation of other than dual tones. It has a pull-down to GND and when floating or tied to GND, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

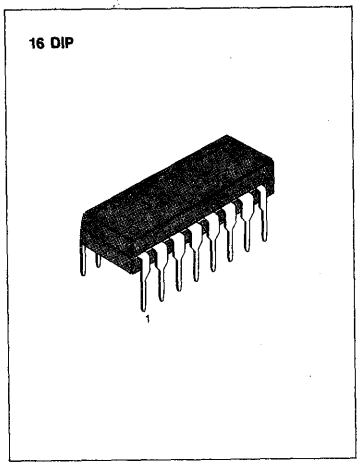
When forced to V_{CC} single or dual tones may be generated as described in the paragraph under row and column inputs.

5. Tone Output (Pin 16)

The tone output pin is connected internally in the KS5808 to the emitter of an NPN transistor whose collector is tied to V_{CC}. The input to this transistor is the on-chip operational ampifier which mixes the row and column tones together and provides output level regulation.

DTMF DIALER WITH REDIAL

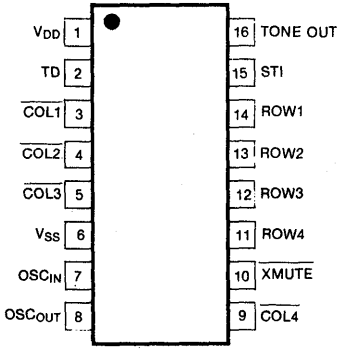
The KS5809/KS5810/KS5811 are monolithic CMOS Integrated circuit which use an 3.579545MHz oscillator for its frequency reference and provides all the features required for implementing a tone dialer.
The required sinusoidal wave form for each individual tone is digitally synthesized on the chip. The wave form so generated has very low total harmonic distortion (7 % Max). A voltage reference is generated on the chip.



FEATURES

- **Wide supply voltage range (2.0~5.5V)**
- **Low power dissipation**
- **Use inexpensive TV crystal (3.579545MHz)**
- **Tone disable input**
- **Low standby current**
- **Continuous mute**
- **Uses either the inexpensive Form A type keyboard or the standard 2 of 7 matrix keyboard with negative common**

PIN CONFIGURATION



ORDERING INFORMATION

Device	Redial Function	Operating Temperature
KS5809N	No Redial	−20 ~ +70°C
KS5810N	Column 4 Key (A, B, C, D) Redial	
KS5811N	# Key Redial	

ARRANGEMENT OF KEYBOARD

1	2	3	A
4	5	6	B
7	8	9	C
*	0	#	D

DTMF FREQUENCIES

Input	Specified	Actual	% Error
R_1	697	699.1	+0.31
R_2	770	766.2	−0.49
R_3	852	847.4	−0.54
R_4	941	948.0	+0.74
C_1	1209	1215.7	+0.57
C_2	1336	1331.7	−0.32
C_3	1477	1471.9	−0.35
C_4	1633	1645.0	+0.73

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Operating Temperature	T_a	$-20 \sim +70$	°C
Storage Temperature	T_{stg}	$-40 \sim +125$	°C
Power Dissipation	P_D	500	mW

ELECTRICAL CHARACTERISTICS

($V_{DD}=3.5V$, $V_{SS}=0V$, $f_{osc}=3.579545MHz$, $Ta=25°C$, unless otherwise specified)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Supply Voltage	V_{DD}			2.0		5.5	V
Memory Retention Voltage	V_{DR}			1.0			V
Key Input High Voltage	V_{IH}	$R_1 \sim R_4$, $C_1 \sim C_4$		0.8 V_{DD}		V_{DD}	V
Key Input Low Voltage	V_{IL}			V_{SS}		0.2 V_{DD}	V
Operating Current	I_{DD}	All outputs unloaded			1.0	2.0	mA
Output Leakage Current	I_{OL}	$V_{DD}=5.5V$				1.0	μA
Oscillator Frequency	f_{osc}				3.57954		MHz
Valid Key Entry Time	T_{KD}			23		25.3	mS
Tone Output	V_{or}	ROW TONE ONLY	$V_{DD}=2.5V$, $R_L=5K$	−16.0		−12.0	dBV
			$V_{DD}=3.5V$, $R_L=5K$	−14.0		−11.0	dBV
Ratio of Column to Row Tone	dB_{cr}			1.0	2.0	3.0	dB
Distortion	% DIS				1.2	7	%

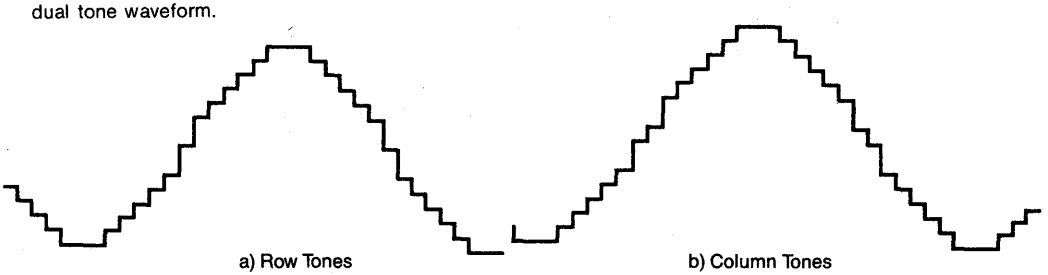
FUNCTION DESCRIPTION

1. Oscillator

When Tone Disable is connect V_{SS} oscillator is disable. This oscillator inhibit prevent the circuit from drawing excessive current. The circuit is designed to work with a crystal out to 3.579545MHz to tone frequency.

2. Output Waveform

The Row and Column output waveform are shown in Fig. 1. These waveform are digitally synthesized using on-chip D/A converter. Distortion measurement of these unfiltered waveform will show a typical distortion 7% or less. The on-chip OP AMP of the KS5809/5810/5811 mix the Row and Column tones together to result in a dual tone waveform.



a) Row Tones b) Column Tones

Fig. 1

PIN DESCRIPTION

1. V_{DD} (Pin 1)

This is the positive supply Pin.
The voltage on this Pin is measured relative to V_{SS} (Pin 6).

2. Tone Disable (Pin 2)

When tone disable input is connected to V_{SS}, key input and oscillator is disable. When this pin is connected to V_{DD}, key input is sensed.

3. Keyboard Inputs (Pin 3, 4, 5, 9, 11, 12, 13, 14)

The KS5809/5810 can use inexpensive Form A keyboard, standard 2-of-7 keyboard or standard 2-of-7 keyboard with negative common. The KS5811 can use standard 2-of-8 keyboard or standard 2-of-8 keyboard with negative common (refer to Fig. 2, Fig. 3, Fig. 4). A valid key entry is defined by either a single Row being connected to a single column or V_{SS} being simulateneously presented to both a single Row and Column. When tone disable $-V_{SS}$, the Row and Column inputs are held high and no keyboard inputs are accepted.
When tone disable $-V_{DD}$ the keyboard is completly static until the initial valid key input is sensed.
The oscillator is then enable and the Rows and Columns are alternately scanned to verify the input is varied (refer to Fig. 5).

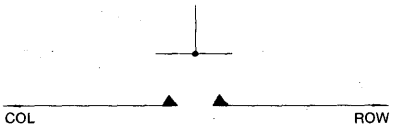


Fig. 2 Form A Keyboard

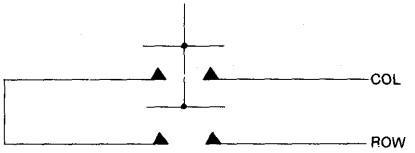


Fig. 3 2 of 7 (2 of 8) Keyboard

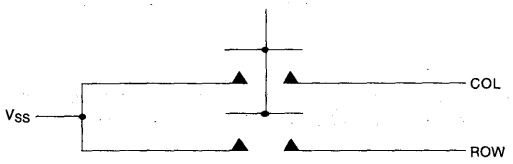


Fig. 4 2 of 7 (2 of 8) Keyboard Negative Common

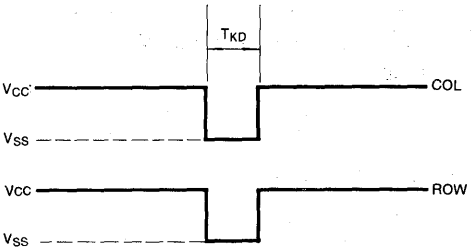


Fig. 5 Electronic Input

4. V_{SS} (Pin 6)

This is negative supply pin and is connected to the common part in the general application.

5. Oscillator In (Pin 7), Oscillator Out (Pin 8)

The network contains an on-board inverter with sufficient loop gain to provides oscillation. The inverter input is Oscillator In, output is Oscillator Out.

6. $\overline{\text{XMUTE}}$ (Pin 10)

The XMUTE output is a N-channel open drain.

Key-in \ $\overline{\text{Tone-Dis}}$	Connected to V_{SS}	Connected to V_{DD}
Key is senced	ON	ON
Key is no senced	ON	OPEN

ON: $\overline{\text{XMUTE}}$ is connected to V_{SS}
OPEN: $\overline{\text{XMUTE}}$ is opened

7. Single Tone Enable (Pin 15)

The single tone enable input is used to generation single tone for test. It has pull down to V_{SS} and when floating or tied to V_{SS}, single tone is inhibited. When tied to V_{DD}, single tone is enable.

8. Tone Output (Pin 16)

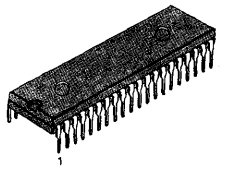
The tone out is connected internally in the KS5809/5810/5811 to the emitter of an NPN transistor whose collector is tied to V_{DD}. The input to this transistor is the on-chip OP AMP which mixes the Row and Column tones together and provides output level regulation.

QUAD UNIVERSIAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

The KS5812, QUAD-UART, is a Si-Gate CMOS IC which provides the data formatting and control to interface serial asynchronous data communications between main system and subsystems.

The parallel data of the bus system is serially transmitted and by the asynchronous data interface with proper formatting and error checking. The KS5812 includes Transmit part, Receive part, Programmable control part, Status check part, and Select part. The control register that is programmed via the data bus during system initialization, provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control.

40 DIP



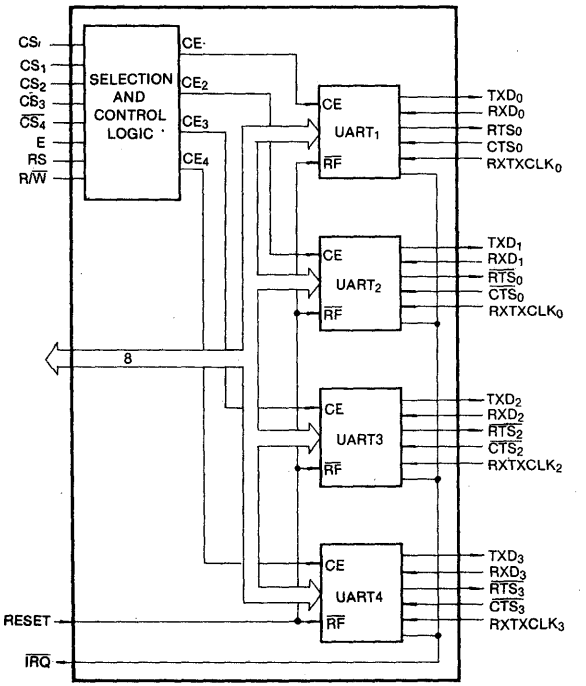
FEATURES

- **Low power, High speed CMOS process.**
- **Serial/Parallel conversion of Data**
- **8-and 9-bit Transmission**
- **Optional Even and Odd Parity**
- **Parity, Overrun and Framing Error Checking**
- **Programmable Control Register**
- **Optional ÷1, ÷16, and ÷64 Clock Modes**
- **Peripheral/Modem Control Functions**
- **Double Buffered**
- **One-or Two-Stop Bit Operation**

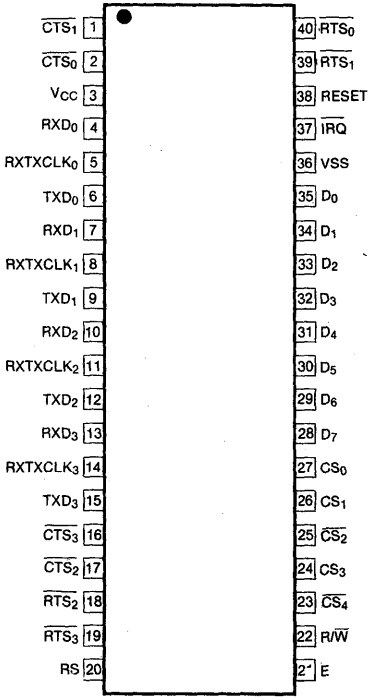
ORDERING INFORMATION

Device	Package	Operating Temperature
KS5812N	40 DIP	−20 ~ +75°C

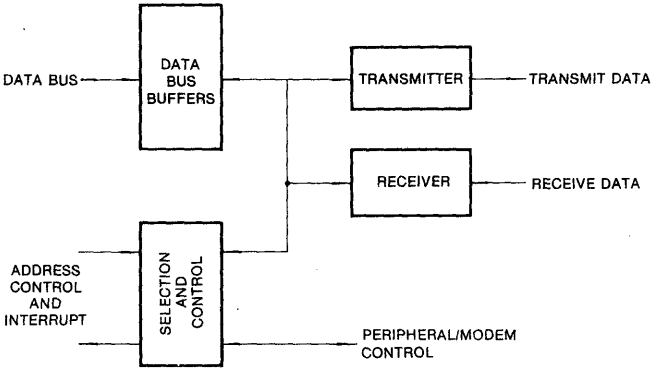
BLOCK DIAGRAM



PIN CONFIGURATION



UART BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage*	V_{CC}*	−0.3 to +7.0	V
Input Voltage*	V_{in}*	−0.3 to +7.0	V
Maximum Output Current**	I_C**	10	mA
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +150	°C

*With respect to V_{SS} (System GND)

**Maximum output current is the maximum current which can flow out from one output terminal or I/O common terminal ($D_0 \sim D_7$, $\overline{RTS}$, Tx Data, $\overline{IRQ}$)

(Note) Permanent IC damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions are exceeded, it could affect reliability of IC.

RECOMMENDED OPERATING CONDITIONS

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}*	4.5	5.0	5.5	V
Input "Low" Voltage		V_{IL}*	0	—	0.8	V
Input "High" Voltage	$D_0 \sim D_7$, RS, $\overline{CTS_i}$, RxD_i	V_{IH}*	2.0	—	V_{CC}	V
	CS_0, CS_2, CS_1 R/$\overline{W}$, E, CS_3, $\overline{CS_4}$, RXTXCLK$_i$		2.2	—	V_{CC}	
Operating Temperature		T_{opr}	−20	25	75	°C

* With respect to V_{SS} (System GND)

DC CHARACTERISTICS ($V_{CC} = +5V \pm 5\%$, $V_{SS} = 0V$, $Ta = -20 \sim +75°C$, unless otherwise noted.)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Input "High" Voltage	$D_0 \sim D_7$, RS, CTSi,	V_{IH}		2.0	—	V_{CC}	V
	CS_0, CS_2, CS_1, R/$\overline{W}$, E, CS_3, $\overline{CS_4}$ RXTXCLKi			2.2	—	V_{CC}	
Input "Low" Voltage	All inputs	V_{IL}		−0.3	—	0.8	V
Input Leakage Current	R/$\overline{W}$, CS_0, CS_1, CS_2, E, CS_3, $\overline{CS_4}$	I_{IN}	$V_{IN} = 0 \sim V_{CC}$	−2.5	—	2.5	μA
Three-State (Off State) Input Current	$D_0 \sim D_7$	I_{TSI}	$V_{IN} = 0.4 \sim V_{CC}$	−10	—	10	μA
Output "High" Voltage	$D_0 \sim D_7$	V_{OH}	$I_{OH} = -400\mu A$	4.1	—	—	V
			$I_{OH} \leq -10\mu A$	V_{CC}-0.1	—	—	
	TXDi, $\overline{RTSi}$		$I_{OH} = -400$	4.1	—	—	
			$I_{OH} \leq -10\mu A$	V_{CC}-0.1	—	—	
Output "Low" Voltage	All outputs	V_{OL}	$I_{OH} = 1.6mA$	—	—	0.4	V
Output Leakage Current (off state)	$\overline{IRQ}$	I_{LOH}	$V_{OH} = V_{CC}$	—	—	10	μA
Input Capacitance	$D_0 \sim D_7$	C_{IN}	$V_{IN} = 0V$, $Ta = 25°C$, $f = 1.0$ MHz	—	—	12.5	pF
	E, RXTXCLKi, R/$\overline{W}$, RS, RXDi, CS_0, CS_1, CS_2, CTS, CS_3, $\overline{CS_4}$			—	—	7.5	
Output Capacitance	$\overline{RTS}$, TXDi	C_{out}	$V_{IN} = 0V$, $Ta = 25°C$, $f = 1.0$ MHz	—	—	10	pF
	$\overline{IRQ}$			—	—	5.0	
Supply Current	• Under transmitting and Receiving operation • 500 kbps • Data bus in R/$\overline{W}$ operation	I_{CC}	E = 1.0 MHz	—	—	3	mA
			E = 1.5 MHz	—	—	4	
			E = 2.0 MHz	—	—	5	
	• Chip is not selected • 500 kbps • Under non transmitting and receiving operation • Input level (Except E) V_{IH} min = $V_{CC} - 0.8V$ V_{IL} max = 0.8V		E = 1.0 MHz	—	—	200	μA
			E = 1.5 MHz	—	—	250	
			E = 2.0 MHz	—	—	300	

AC CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $Ta = -20 \sim +75°C$, unless otherwise noted.)

1. TIMING OF DATA TRANSMISSION

Characteristic		Symbol	Test Conditions	KS5812 Min	KS5812 Max	Unit
Minimum Clock Pulse Width	÷1 Mode	PW_{CL}	Fig. 1	900	—	ns
	÷16, ÷64 Modes			600	—	ns
	÷1 Mode	PW_{CH}	Fig. 2	900	—	ns
	÷16, ÷64 Modes			600	—	ns
Clock Frequency	÷1 Mode	f_C		—	500	KHz
	÷16, ÷64 Modes			—	800	KHz
Clock-to-Data Delay for Transmitter		t_{TDD}	Fig. 3	—	600	ns
Receive Data Setup Time	÷1 Mode	t_{RDSU}	Fig. 4	250	—	ns
Receive Data Hold Time	÷1 Mode	t_{RDH}	Fig. 5	250	—	ns
$\overline{IRQ}$ Release Time		t_{IR}	Fig. 6	—	1200	ns
$\overline{RTS}$ Delay Time		t_{RTS}	Fig. 6	—	560	ns
Rise Time and Fall Time	Except E	t_r, t_f		—	1000*	ns

* 1.0μs or 10% of the pulse width, whichever is smaller.

2. BUS TIMING CHARACTERISTICS

1) READ

Characteristic	Symbol	Test Conditions	KS5812 Min	KS5812 Max	Unit
Enable Cycle Time	$t_{cyc}E$	Fig. 7	1000	—	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 7	450	—	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 7	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 7	80	—	ns
Data Delay Time	t_{DDR}	Fig. 7	—	290	ns
Data Hold Time	t_H	Fig. 7	20	100	ns
Address Hold Time	t_{AH}	Fig. 7	10	—	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 7	—	25	ns

2) WRITE

Characteristic	Symbol	Test Conditions	KS5812		Unit
			Min	Max	
Enable Cycle Time	$t_{cyc}E$	Fig. 8	1000	—	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 8	450	—	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 8	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 8	80	—	ns
Data Setup Time	t_{DSW}	Fig. 8	165	—	ns
Data Hold Time	t_H	Fig. 8	10	—	ns
Address Hold Time	t_{AH}	Fig. 8	10	—	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 8	—	25	ns

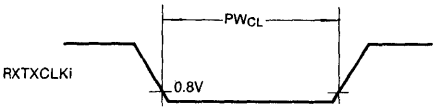


Fig. 1 Clock Pulse Width, "Low" State

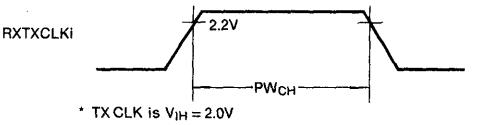


Fig. 2 Clock Pulse Width, "High" State

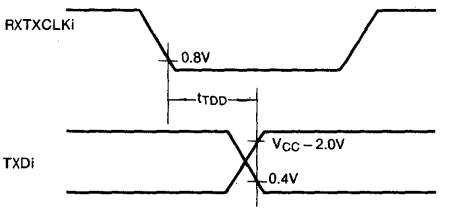


Fig. 3 Transmit Data Output Delay

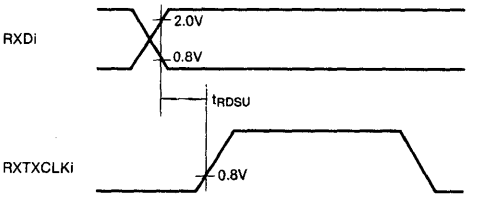


Fig. 4 Receive Data Setup Time (÷1 Mode)

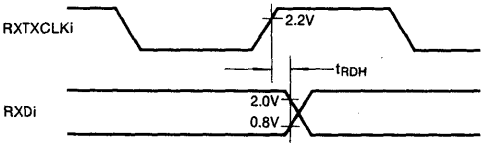
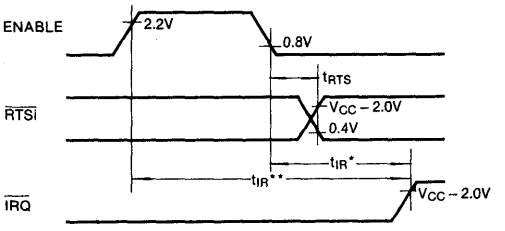


Fig. 5 Receive Data Hold Time (÷1 Mode)



* (1) $\overline{IRQ}$ Release Time applied to R_XDi Register read operation
(2) $\overline{IRQ}$ Release Time applied to T_XDi Register write operation
(3) $\overline{IRQ}$ Release Time applied to control Register write TIE = 0, RIE = 0 operation.

** $\overline{IRQ}$ Release Time applied to R_X Data Register read operation right after read status register, when $\overline{IRQ}$ is asserted by DCD rising edge.

Note: Note that following take place when $\overline{IRQ}$ is asserted by the detection of transmit data register empty status. $\overline{IRQ}$ is released to "High" asynchronously with E signal when $\overline{CTSi}$ goes "High". (Refer to Figure 14)

Fig. 6 $\overline{RTSi}$ Delay and $\overline{IRQ}$ Release Time

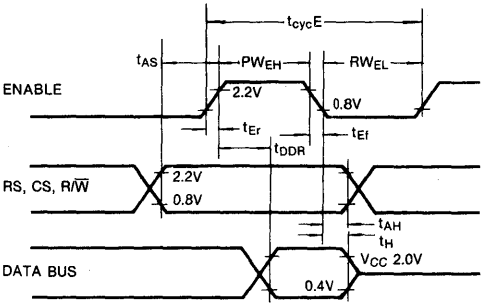


Fig. 7 Bus Read Timing Characteristics (Read information from UART)

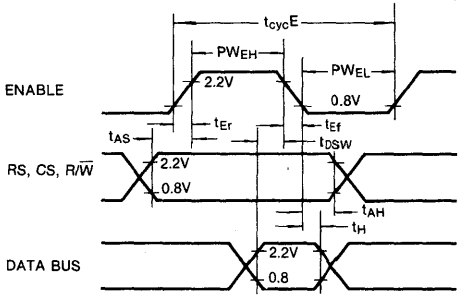


Fig. 8 Bus Write Timing Characteristics (Write information into UART)

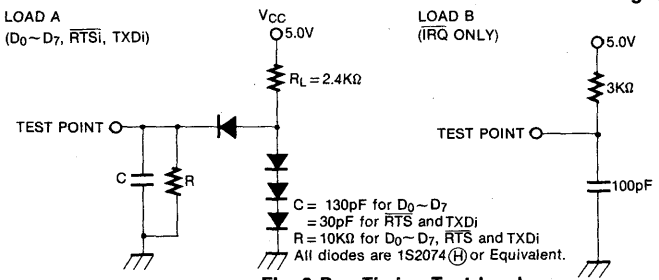


Fig. 9 Bus Timing Test Loads

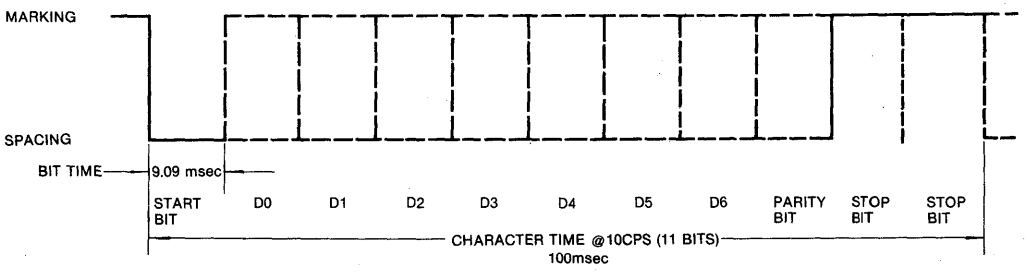


Fig. 10 110 Baud Serial ASCII Data Timing

DEVICE OPERATION

At the bus interface, the UARTi appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the UARTi functional configuration when the communications channel is required. During the first master reset, the $\overline{IRQ}$ and $\overline{RTSi}$ outputs are held at level 1. On all other master resets, the $\overline{RTSi}$ output can be programmed high or low with the $\overline{IRQ}$ output held high. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTSi}$ whenever master reset is utilized. The UARTi also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset which must be applied prior to operating the UARTi. After master resetting the UARTi, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

TRANSMIT

A typical transmitting sequence consists of reading the UARTi. Status Register either as a result of an interrupt or in the UARTi's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the|Register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of 8 or 32 low samples on the receive line in the divide-by-16 and 64 modes respectively. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit UARTi bus when a Read Data command is received from the MPU. When parity has been selected for a 7-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

UART INTERFACE SIGNALS FOR MPU

The KS5812 interfaces to the MPU with an 8-bit bidirectional data bus, five chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals permit the MPU to have complete control over the KS5812.

UART Bidirectional Data (D0-D7) — The bidirectional data lines (D0-D7) allow for data transfer between the KS5812 and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an UARTi read operation.

UART Enable (E) — The Enable signal, E, is a high-impedance TTL-compatible input that enables the bus

input/output data buffers and clocks data to and from the KS5812.

Read/Write (R/$\overline{W}$) — The Read/Write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the UARTi's input/output data bus interface. When Read/Write is high (MPU Read cycle), KS5812 output drivers are turned on and a selected register is read. When it is low, the KS5812 output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the KS5812.

Chip Select (CS0, CS1, CS2, CS3, $\overline{CS4}$) — These five high-impedance TTL-compatible input lines are to select and address the KS5812. Each UART can be enabled when CS2 and CS3 are high and $\overline{CS4}$ is low. CS0 and CS1 are used to select individual UART.

CS0	CS1	CS2	CS3	CS4	UARTi
0	0	1	1	0	UART1
0	1	1	1	0	UART2
1	0	1	1	0	UART3
1	1	1	1	0	UART4

Register Select (RS) — The Register Select line is a high-impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request ($\overline{IRQ}$) — Interrupt Request is a TTL-compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the KS5812 is set. The $\overline{IRQ}$ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the UARTi. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5•$\overline{CR6}$), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTSi}$) being high or the UARTi being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTSi}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the UARTi. Interrupts caused by Overrun is cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the UARTi. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

CLOCK INPUTS

High-impedance TTL-compatible inputs is provided for clocking of transmitted and received data. Clock frequencies of 1, 16, or 64 times the data rate may be selected.

RECEIVE AND TRANSMITTER CLOCK (RXTXCLKi)

—The RXTXCLKi input are both used for the clocking of transmitted data and for synchronization of received data. (In the /1 mode, the clock and data must be synchronized extenally.) The transmitter initiates data on the negative transition of the clock and the receiver samples the data on the positive transition of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (RXDi) — The Receive Data line is a high-impedance TTL-compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used.

Transmit Data (TXDi) — The Transmit Data output line transfers serial data to a modem or other peripheral.

PERIPHERAL/MODEM CONTROL

The UARTi includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTSi}$) — This high-impedance TTL-compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTSi}$) — The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTSi}$ output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTSi}$ output is low (the active state). This output can also be used for Data Terminal Ready ($\overline{DTR}$).

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the UARTi has been addressed with RS high and R/$\overline{W}$ low. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take plaoe within 1-bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the UARTi and selecting the Receive Data Register with RS and R/$\overline{W}$ high when the UARTi is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

CONTROL REGISTER

The UARTi Control Register consists of eight bits of write-only buffer that are selected when RS and R/$\overline{W}$ are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) — The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the UARTi. Additionally, these bits are used to provide a master reset for the UARTi which clears the Status Register (except for external conditions on $\overline{CTSi}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the UARTi. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) — The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows;

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) — Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTSi}$) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTSi}$ = low, Transmitting Interrupt Disabled.
0	1	$\overline{RTSi}$ = low, Transmitting Interrupt Enabled.
1	0	$\overline{RTSi}$ = high, Transmitting Interrupt Disabled.
1	1	RTS = low, Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

Receive Interrupt Enable Bit (CR7) — The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7). Receive Data Register Full Overrun.

STATUS REGISTER

Information on the status of the UARTi is available to the MPU by reading the UARTi Status Register. This read only register is selected when RS is low and R/$\overline{W}$ is high. Information stored in this register indicates the

status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the UARTi

Receive Data Register Full (RDRF), Bit 0 — Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 — The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Clear-to-Send ($\overline{CTS}$), Bit 3 — The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the Clear-to-Send status bit.

Framing Error (FE), Bit 4 — Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

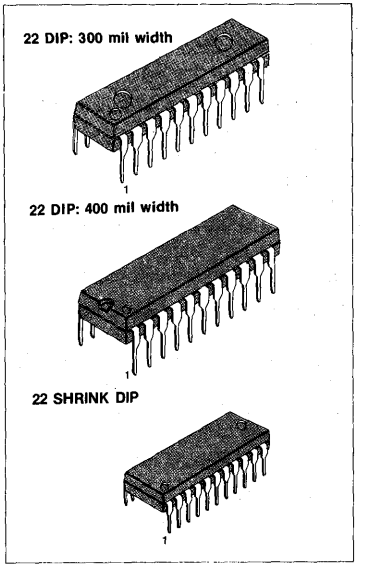
Receiver Overrun (OVRN), Bit 5 — Overrun is an error flag the indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the HDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

Parity Error (PE), Bit 6 — The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request ($\overline{IRQ}$), Bit 7 — The $\overline{IRQ}$ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is low the $\overline{IRQ}$ bit will be high to indicate the interrupt or service request status. $\overline{IRQ}$ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

TONE/PULSE DIALER WITH REDIAL

The KS5819 is a DTMF/PULSE switchable dialer with a 32-digit redial memory. Through pin selection, switching from pulse to DTMF mode can be done using slide switch or by depressing [T] key. All necessary dual-tone frequencies are derived from a 3.579545MHz TV crystal, providing very high accuracy and stability. The required sinusoidal wave form for each individual tone is digitally synthesized on the chip. The wave form so generated has very low total harmonic distortion (7% max). A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet telephone industry specifications. CMOS technology is applied to this device, for very low power requirements, high noise immunity, and easy interface to a variety of telephones requiring few external components.



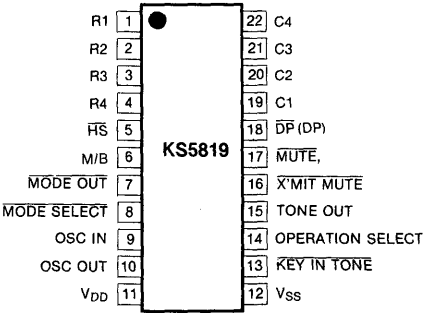
FEATURES

- **Tone/Pulse switchable (touch key or slide switch).**
- **32 digit capacity for redial**
- **Automatic mix redialing (last number dial) of PULSE→DTMF with multiple auto access pause (3.5 sec)**
- **Key-in-tone output for valid key entry in pulse mode (Fkf = 1.75KHz, Tkf = 23mS).**
- **Low power CMOS process (2.0 to 5.5V)**
- **Numbers dialed manually after redial are cascadable and stored as additional numbers for next redialing**
- **Uses inexpensive TV crystal (3.579545MHz)**
- **Make/Break ratio (33 1/3~66 2/3 or 40/60) pin selectable**
- **Touch key hooking (604ms)**
- **Low standby current**
- **4 x 4 or (2 of 8) keyboard available**

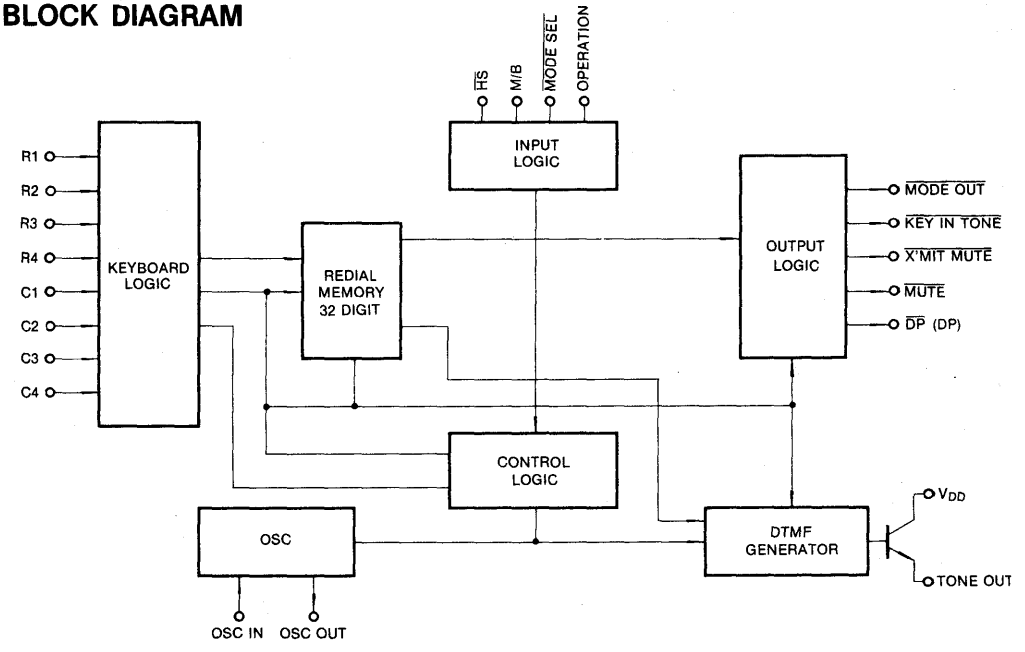
ORDERING INFORMATION

Device	Package	Dial Pulse	PPS
KS58A19N	300mil	DP	10
KS58B19N	Width	DP	20
KS58C19N	Size	$\overline{DP}$	10
KS58D19N		$\overline{DP}$	20
KS58A19E	400mil	DP	10
KS58B19E	Width	DP	20
KS58C19E	Size	$\overline{DP}$	10
KS58D19E		$\overline{DP}$	20
KS58A19P	Shrink	DP	10
KS58B19P	Package	DP	20
KS58C19P	Type	$\overline{DP}$	10
KS58D19P		$\overline{DP}$	20

PIN CONFIGURATION



BLOCK DIAGRAM



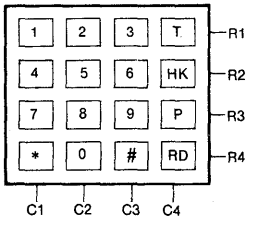
TONE DURATION & PAUSE IN REDIAL

Characteristic	Symbol	Typ	Unit
Tone Duration	T_D	110	mS
Minimum Pause	ITP	110	mS
Cycle Time	T_C	220	mS

TONE FREQUENCIES

Input	Specified	Actual	% Error
R1	697	699.1	+0.31
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.7	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35

ARRANGMENT OF KEYBOARD



T : PULSE-DTMF SWITCHING
HK : HOOKING (604ms)
P : PAUSE (3.5 second)
RD : REDIAL

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$\leqq V_{DD}$ ($\overline{DP}$, $\overline{MUTE}$, $\overline{XMUTE}$)	V
Tone Output Current	I_{TONE}	50	mA
Power Dissipation	P_D	500	mW
Operating Temperature	T_{opr}	$-20 \sim +70$	°C
Storage Temperature	T_{stg}	$-40 \sim +125$	°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 3.5V, fx'tal = 3.579545MHz, Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions			Min	Typ	Max	Unit
Operating Voltage Range	$V_{DD}P$	Pulse Mode	All inputs connected to V_{DD} or V_{SS}		2.0		5.5	V
	$V_{DD}T$	Tone Mode			2.0		5.5	
Memory Retention Voltage	V_{DR}				1.0			V
Operating Supply Current	$I_{DD}P$	$\overline{MODE} = V_{DD}$	One key selected $\overline{HS} = V_{SS}$. All outputs unloaded			0.3	0.5	mA
	$I_{DD}T$	$\overline{MODE} = V_{SS}$				0.5	1.0	
Standby Current	$I_{SD}1$	$\overline{HS} = V_{DD} = 1.5V$	No key selected. All outputs unloaded				0.05	μA
	$I_{SD}2$	$\overline{HS} = V_{SS}$					50	
Output Current	$I_{OL}1$	$\overline{DP}$, $\overline{MUTE}$ $\overline{XMUTE}$	$V_{OL} = 0.4V$	$V_{DD} = 3.5V$	1.7	5.0		mA
	$I_{OL}2$			$V_{DD} = 2.5V$	0.5	1.5		
Output Leakage Current	I_{OFF}	$\overline{MODE\ OUT}$, $\overline{KT}$	$V_{OUT} = 2.5V$				1.0	μA
Input Voltage	V_{IH}	R1-R4, C1-C3, $\overline{HS}$, M/B			$0.8V_{DD}$		V_{DD}	V
	V_{IL}	OPERATION SELECT, $\overline{MODE\ SELECT}$			V_{SS}		$0.2V_{DD}$	
Input Current	$I_{IN}1$	$V_{DD} = 3.5V$ $V_{IN} = 0V$	R1-R4				116	μA
	$I_{IN}2$	$V_{DD} = 2.5V$ $V_{IN} = 0V$					50	
Valid Key Entry Time	T_{kd}				23		25.3	mS
Column and Row Scanning Frequency	F_{cr}					437		Hz
Key-In Tone Output Duration	T_{kt}					23		mS
Key-In Tone Frequency	F_{kt}					1.75		KHz
Auto Access Pause Time	T_{ap}					3.5		sec
Tone Output	V_{or}	$V_{DD} = 2.5V$, $R_L = 5K$	ROW TONE ONLY		−16.0		−12.0	dBV
		$V_{DD} = 3.5V$ $R_L = 5K$			−14.0		−11.0	
Ratio of Column to Row Tone	dB_{cr}	$V_{DD} = 3.5V$			1.0	2.0	3.0	dB
Distortion	%DIS	$V_{DD} = 3.5V$					7	%
Tone Output Delay Time	T_{psd}					1.5		mS

PIN DESCRIPTION

<table>
<tr><th>Pin</th><th>Name</th><th>Description</th></tr>
<tr><td>1-4
15-22</td><td>R1-R4
C1-C4</td><td>Keyboard (R1, R2, R3, R4, C1, C2, C3, C4)
These inputs can be interfaced to an XY matrix keyboard. $C_1 \sim C_4$ & $R_1 \sim R_4$ are set to low at On Hook ($\overline{HS}$ = high). $C_1 \sim C_4$ key inputs are set to low and R1-R4 are set to high at OFF HOOK ($\overline{HS}$ = low) which enables the key-input operation. Oscillator starts running when a key press is detected.
Scanning signals are presented at both column and row inputs (TYP: 437Hz) until the input key is released. Key inputs are compatible with standard 2-of-8 form or single-contact keyboard. Debouncing is provided to avoid false entry (TYP: 25mS).</td></tr>
<tr><td>5</td><td>$\overline{HS}$</td><td>Hook Switch
This input detects the state of the hook switch contact.
"Off Hook" corresponds to V_{SS} condition.
"On Hook" corresponds to V_{DD} condition.</td></tr>
<tr><td>6</td><td>M/B</td><td>Make/Break Ratio
This input provides the selection of the Make/Break ratio (33.3: 66.6/40:60) when M/B is connected to V_{DD}/V_{SS}.</td></tr>
<tr><td>7</td><td>$\overline{\text{MODE OUT}}$</td><td>Mode Output
This output indicates whether the chip is operating in pulse or tone mode. Pulse/Tone mode corresponds to OFF/ON state (N channel open drain). Mode state is controlled with Operation Select, $\overline{\text{Mode Select}}$ and [T] key inputs.</td></tr>
<tr><td>8</td><td>$\overline{\text{MODE SELECT}}$</td><td>Mode Select Input
Pulse/DTMF mode is selected as shown in the following table.
Initial Mode means the state after going Off Hook ($\overline{HS} \rightarrow$ "V_{SS}")
<table>
<tr><th>OPERATION SELECT</th><th>$\overline{\text{MODE SELECT}}$</th><th>INITIAL MODE</th><th>SWITCHING ENTRY MODE</th><th>NOTES</th></tr>
<tr><td rowspan="2">V_{DD}</td><td>V_{DD}</td><td>Pulse</td><td>[T] Key-In</td><td rowspan="2">$\overline{\text{MODE SELECT}}$ defines only initial mode after going Off Hook and is latched at first key entry.</td></tr>
<tr><td>V_{SS}</td><td>Tone</td><td>N/A</td></tr>
<tr><td rowspan="2">V_{SS}</td><td>V_{DD}</td><td>Pulse</td><td>$\overline{\text{MODE SELECT}}$ input = V_{SS}</td><td rowspan="2">[T] key is disabled under this condition.</td></tr>
<tr><td>V_{SS}</td><td>Tone</td><td>N/A</td></tr>
</table>
If choice of switching method is desired (either [T] key or $\overline{\text{MODE SELECT}}$). Operation select should be connected to $\overline{\text{MODE SELECT}}$ in order to avoid false operation.</td></tr>
<tr><td>9
10</td><td>OSC IN
OSC OUT</td><td>Oscillator Input/Output
These pins are provided to connect an external 3.58MHz crystal. Oscillator starts (at Off Hook) and is sustained until pulse or DTMF signal are finished.</td></tr>
<tr><td>11
12</td><td>V_{DD}
V_{SS}</td><td>Power
These are the power supply inputs. The device is designed to be operated on 2.0V to 5.5V.</td></tr>
</table>

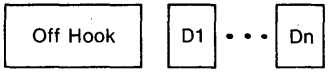
PIN DESCRIPTION (Continued)

<table>
<tr><th>Pin</th><th>Name</th><th>Description</th></tr>
<tr><td>13</td><td>$\overline{\text{KEY IN TONE}}$</td><td>Key In Tone Output
Key in tone signal is provided only in pulse mode for all Key-ins except [T] key-in. No $\overline{\text{KEY IN TONE}}$ is generated in DTMF mode. Fkt: 1.75KHz, Tkt: 23mS.
(N channel open drain)</td></tr>
<tr><td>14</td><td>OPERATION SELECT</td><td>Operation Select Input
Mode switching (from Pulse to DTMF) entry is selectable with this input, i.e. whether [T] key entry or $\overline{\text{MODE SELECT}}$ input entry is selectable.</td></tr>
<tr><td>15</td><td>TONE OUT</td><td>DTMF Signal Output
When a valid keypress is detected in DTMF mode appropriate low and high group frequencies are generated which hybrided the Dual Tone Output.
Tone out is Off State in pulse mode.</td></tr>
<tr><td>16</td><td>$\overline{\text{X'MIT MUTE}}$</td><td>$\overline{\text{X'mit Mute Output}}$
<table>
<tr><th>$\overline{\text{HS}}$</th><th>$\overline{\text{X'mit Mute Output}}$</th></tr>
<tr><td>V_{DD}</td><td>"ON"</td></tr>
<tr><td>V_{SS}</td><td>Normally "OFF"
"ON" during pulse and DTMF dialing</td></tr>
</table>
(N channel open drain)</td></tr>
<tr><td>17</td><td>$\overline{\text{MUTE}}$</td><td>$\overline{\text{Mute Output}}$
<table>
<tr><th>$\overline{\text{HS}}$</th><th>$\overline{\text{MUTE OUTPUT}}$</th></tr>
<tr><td>V_{DD}</td><td>"ON"</td></tr>
<tr><td>V_{SS}</td><td>Normally "OFF" in DTMF mode.
"ON" during pulse dialing</td></tr>
</table>
(N channel open drain)</td></tr>
<tr><td>18</td><td>$\overline{\text{DP}}$, DP</td><td>Dial Pulse Out. $\overline{\text{DP}}$: C/D, DP: A/B
DP: The normal output will be "OFF" during break and "ON" during make at "OFF HOOK."
The output will be "ON" at "ON HOOK,"
$\overline{\text{DP}}$: The normal output will be "ON" during break and "OFF" during make at "OFF HOOK."
The output will be "OFF" at "ON HOOK."</td></tr>
</table>

KEYBOARD OPERATION

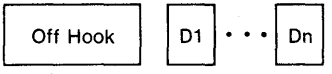
1. SINGLE MODE OPERATION

- **Pulse Mode Operation**

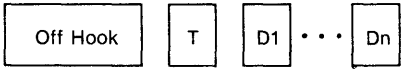


Pulse mode is defined by the initial mode after going Off Hook and latched at [D1] key entry. This is the condition under $\overline{\text{Mode Select}} = V_{DD}$.

- **Tone Mode Operation**

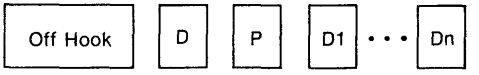


Tone mode is defined by the initial mode after going Off Hook and latched at [D1] key entry. This condition is under $\overline{\text{Mode Select}} = V_{SS}$.



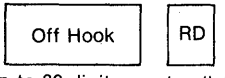
If initial mode is at pulse mode after going Off Hook and $\overline{\text{Mode Select}} = V_{DD}$, Operation Select = V_{DD}. Switching mode from pulse to tone can be done by [T] key entry and latched at [D1] key entry.

- **Manual Dialing with Automatic Access Pause**



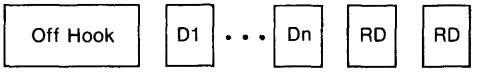
Multiple Pause key entries can be accepted and stored in the redial memory, each as a digit. Each [P] key provides 3.5 seconds pause time, but [P] key entry as first digit after going Off Hook is ignored. [*] key can also be used as pause key in pulse mode. Pause (s) can be cancelled with [P], [T] or [RD] key during pause time in redialing. [D] = Any numeric key.

- **Redialing**



Up to 32 digits can be dialed with [RD] key. [RD] key is disabled while pulse or DTMF signals are transmitted. When more then 32 digits are stored, redial is also inhibited.
[#] key can be used as [RD] key in pulse mode.

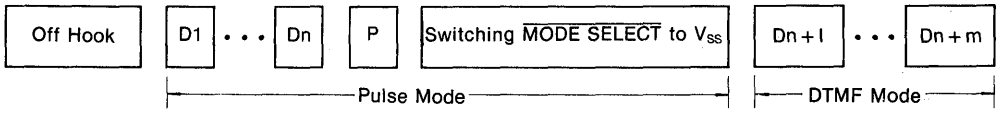
- **Inhibiting Redial**



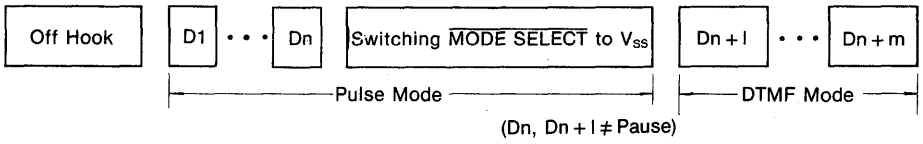
Redial can be inhibited by depressing [RD] [RD] keys after DTMF or pulse signals are transmitted.

2. PULSE/TONE SWITCHABLE OPERATION

• **Mode Switching by $\overline{\text{MODE SELECT}}$ Input (OPERATION SELECT = V_{SS})**

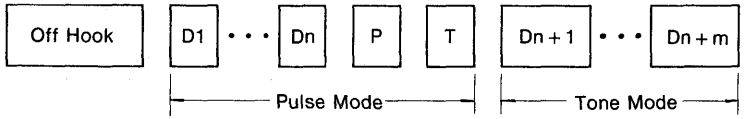


Pulse mode is initially defined $\overline{\text{MODE SELECT}} = V_{DD}$, mode switching to DTMF can be accepted by $\overline{\text{MODE SELECT}} = V_{SS}$, DTMF mode will be set up after pulse mode is finished. In this mode, digits [Dn+I] ... [Dn+m] are transmitted from Tone Out as DTMF signals by depressing corresponded keys.
If no [P] key is contained serially before or after mode switching, following condition is obtained.

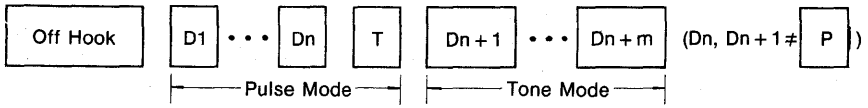


If digit [Dn+1] is depressed after pulse mode is finished, DTMF mode will be set up after last pulse signal ([Dn]) is generated. In this mode, digits [Dn+1] ... [Dn+m] are transmitted from Tone Out as DTMF signals by depressing corresponded keys. If digit [Dn+1] is depressed during dialing pulse signals, DTMF mode but in Hold State will be set up after last pulse signal [Dn] is finished. MODE OUT will flash to indicate this Hold State [Dn+1] ... [Dn+m] are stored in redial memory as DTMF data and not transmitted from Tone Out. When it is ready to transmit DTMF data in redial memory, [T], [RD] or [P] keys is depressed to reset this Hold State and [Dn+1] ... [Dn+m] data are serially transmitted.

• Mode Switching by [T] key (OPERATION SELECT = V_{DD})



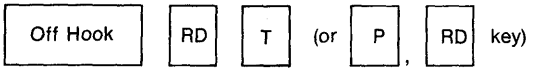
Pulse mode is initially defined with $\overline{\text{MODE SELECT}} = V_{DD}$. Mode switching to DTMF can be accepted by [T] key. In DTMF mode, digits [Dn+1] ... [Dn+m] are transmitted from Tone Out as DTMF signals by depressing corresponding key. If no [P] key is contained serially before or after [T] key.



It results the next condition:
If digit [Dn+1] is depressed after pulse mode is finished DTMF mode will be set up after last pulse signal [Dn] is out. In this mode, digits [Dn+1] ... [Dn+m] are transmitted from TONE OUT as DTMF signals by depressing corresponded key

If digit [Dn + 1] is depressed during dialing pulse signal, the Hold State will be set up after last pulse signal [Dn] is finished. When DTMF MODE is set up. MODE OUT will flash to indicate this Hold State.
Digits [Dn + 1] ... [Dn + m] are stored in redial memory as DTMF data and not transmitted from Tone Out.
When it is ready to transmit DTMF data in redial memory, [T], [RD] or [P] keys is depressed to reset this Hold State and [Dn + 1] ... [Dn + m] data are serially transmitted.

- Redial with Hold State Cancell



Pause can be cancelled with [P], [T] or [RD] keys in redialing. Any pause in series corresponding with pause is also cancelled. When no pause is stored before or after mode switching, chip will go into the Hold State when DTMF mode is set up. MODE OUT will flash to indicate this Hold State. DTMF data are stored in redial memory and not transmitted from tone out.
[T], [RD] or [P] keys is depressed to reset this Hold State and DTMF data are serially transmitted.

Single Tone Operation in DTMF Mode (Test mode)

1. The M/B pin is used to trig the chip into test made by applying a positive or negative pulse after "Off Hook." Test mode is sustained until On Hook. The single tone is shown in the following table which contrast with normal mode.

Normal mode

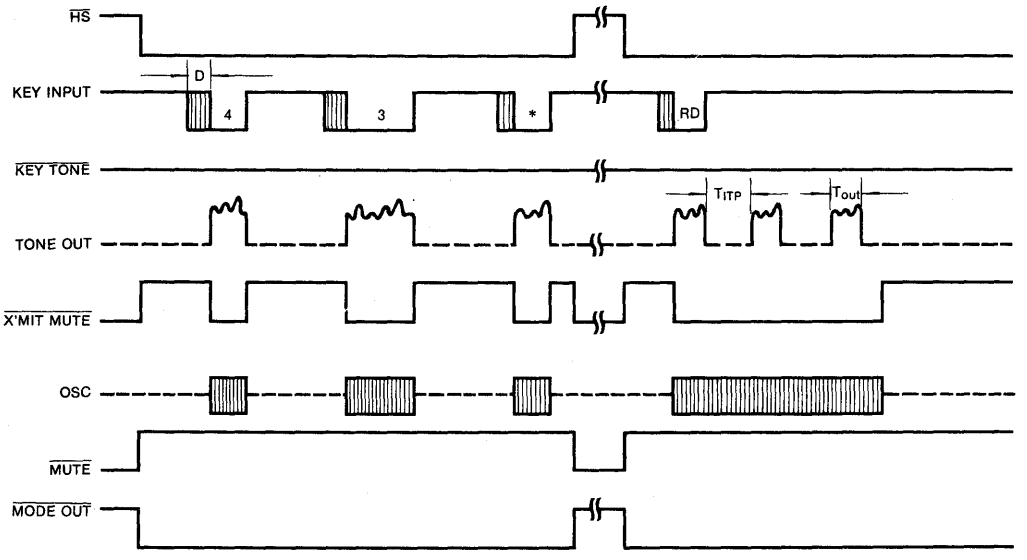
	C1	C2	C3
R1	1	2	3
R2	4	5	6
R3	7	8	9
R4	*	0	#

Single tone mode

	C1	C2	C3
R1	R1	C2	C3
R2	C1	C2	R2
R3	R3	C2	C3
R4	C1	R4	C3

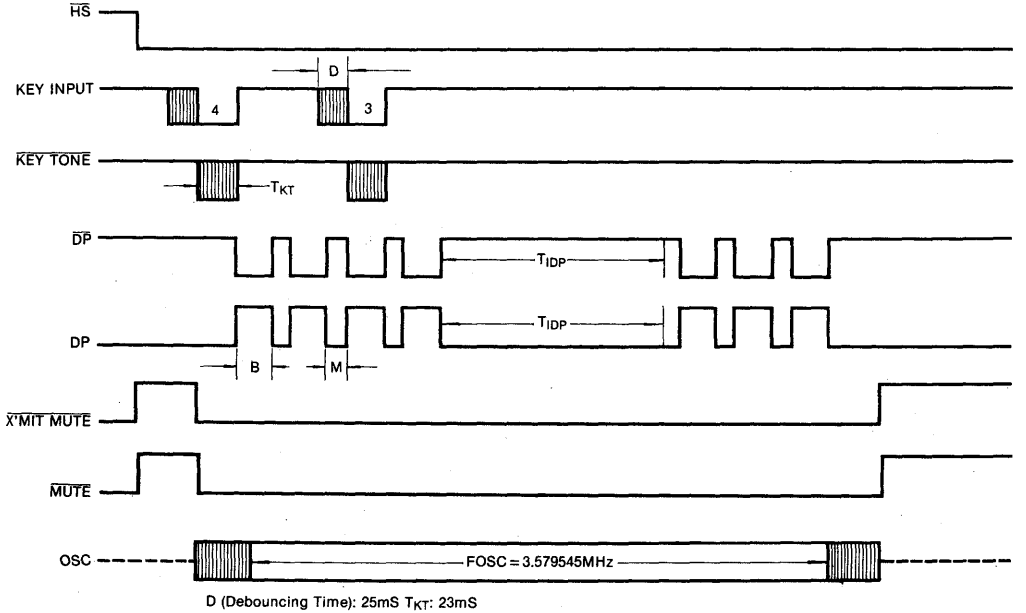
2. Single tone can be generated by simultaneously depressing two digit keys in the appropriate Row and Column. If two digit keys, not in the same Row or Column, the dual tone disabled and no output is provided.

TONE MODE TIMING (MODE SELECT = V_{SS})



D: Debouncing time: 25mS
T_{ITP}: 110mS T_{out}: 110mS

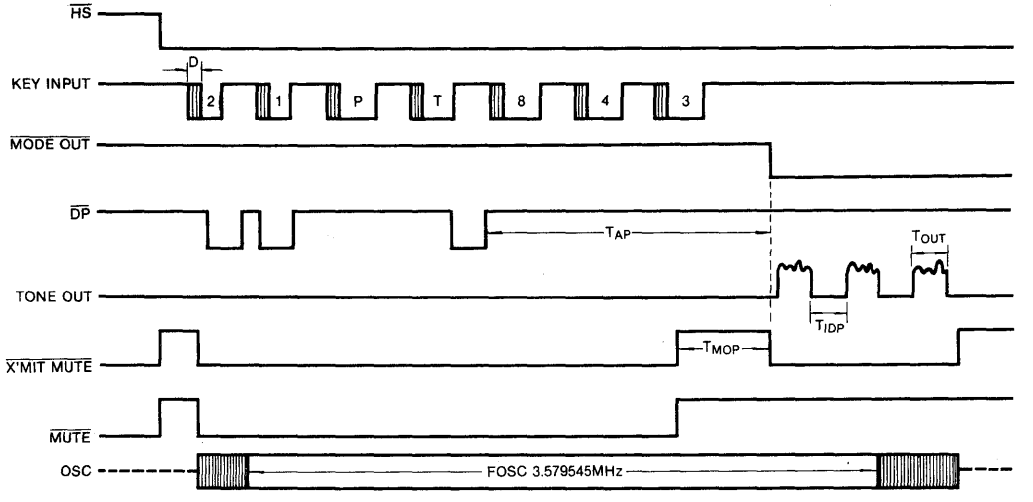
PULSE MODE TIMING ($\overline{\text{MODE SELECT}}$ = V_{DD})



D (Debouncing Time): 25mS T_{KT}: 23mS
T_{IDP}: 879mS f_{KT}: 1.75KHz

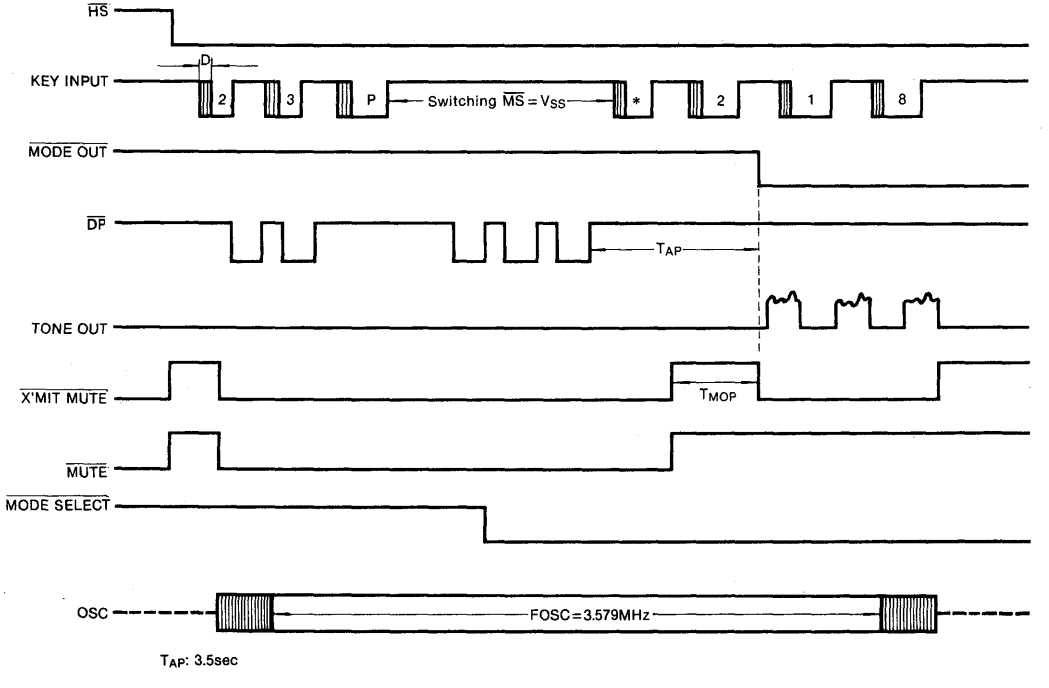
TIMING DIAGRAM

(for Switching Mode Operation by [T] key) (OPERATION SELECT, $\overline{\text{MODE SELECT}}$ = = V_{DD})



TIMING DIAGRAM

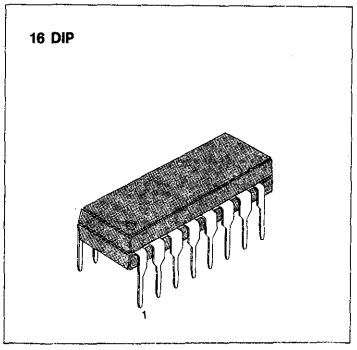
(for Switching Mode Operation by $\overline{\text{MODE SELECT}}$ Input) (OPERATION SELECT = V_{SS})



TAP: 3.5sec

TONE/PULSE DIALER WITH REDIAL

The KS5820 is a DTMF/PULSE switchable dialer with a 32-digit redial memory. Through pin selection, switching from pulse to DTMF mode can be done using slide switch. All necessary dual-tone frequencies are derived from a 3.579545MHz TV crystal, providing very high accuracy and stability. The required sinusoidal wave form for each individual tone is digitally synthesized on the chip. The wave form so generated has very low total harmonic distortion (7% Max). A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the single levels of the dual tone to meet telephone industry specifications. CMOS technology is applied to this device, for very low power requirements high noise immunity, and easy interface to a variety of telephones requiring external components.



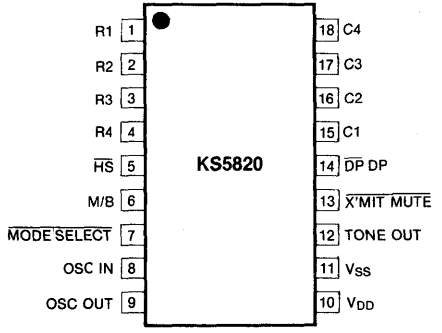
FEATURES

- **Tone/Pulse switchable (slide switch).**
- **32 digit capacity for redial**
- **Automatic mix redialing (last number dial) of PULSE→DTMF with multiple auto access pause**
- **PABX auto-pause for 3.5 sec.**
- **4 x 4 or (2 of 8) keyboard available**
- **Low power CMOS process (2.0 to 5.5V)**
- **Numbers dialed manually after redial are cascadable and stored as additional numbers for next redialing**
- **Uses inexpensive TV crystal (3.579545MHz)**
- **Make/Break ratio (33 1/3 ~ 66 2/3 or 40/60) pin selectable**
- **Touch key hooking (604ms)**
- **Low standby current**

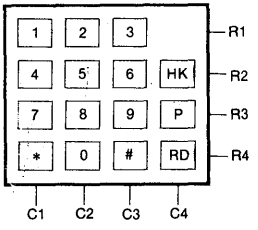
ORDERING INFORMATION

Device	Dial Pulse	PPS	Make/Break Ratio
KS58A20N	DP	10	V_{DD}: 33.3/66.6
			V_{SS}: 40/60
KS58B20N	DP	20	V_{DD}: 33.3/66.6
			V_{SS}: 40/60
KS58C20N	$\overline{DP}$	10	V_{DD}: 33.3/16.6
			V_{SS}: 40/60
KS58D20N	$\overline{DP}$	20	V_{DD}: 33.3/66.6
			V_{SS}: 40/60

PIN CONFIGURATION

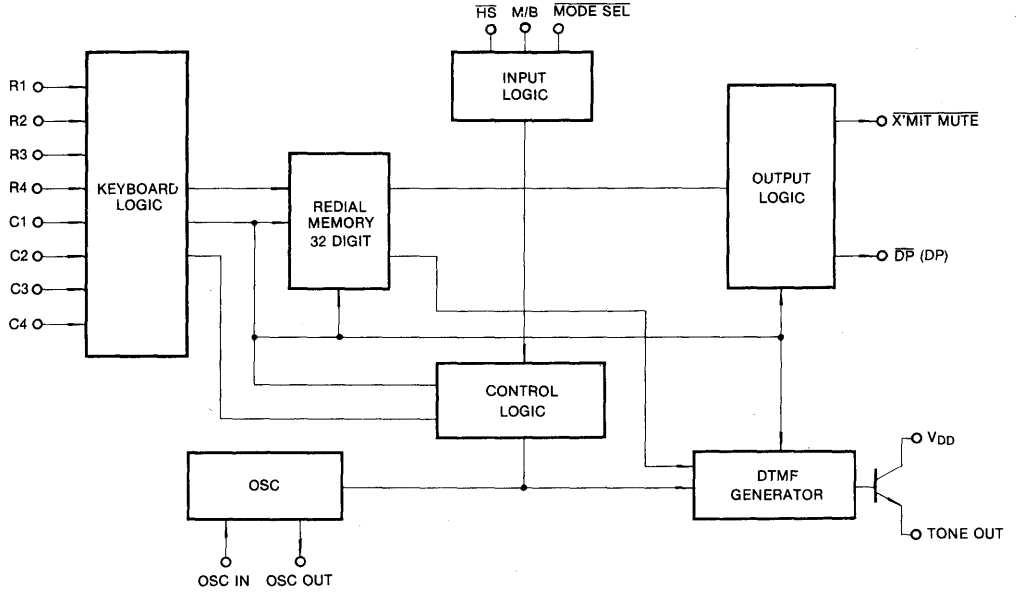


ARRANGEMENT OF KEYBOARD



HK : HOOKING (604ms)
P : PAUSE (3.5 second)
RD : REDIAL

BLOCK DIAGRAM



TONE DURATION & PAUSE IN REDIAL

Characteristic	Symbol	Typ	Unit
Tone Duration	T_D	110	mS
Minimum Pause	ITP	110	mS
Cycle Time	T_C	220	mS

TONE FREQUENCIES

Input	Specified	Actual	% Error
R1	697	699.1	+0.31
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.7	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$V_{SS}-0.3$, $V_{DD}+0.3$	
Output Voltage	V_{OUT}	$\leqq V_{DD}$, ($\overline{DP}$, $\overline{X'MITMUTE}$)	V
Tone Output Current	I_{TONE}	50	mA
Power Dissipation	P_D	500	mW
Operating Temperature	T_{opr}	$-20 \sim +70$	°C
Storage Temperature	T_{stg}	$-40 \sim +125$	

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 3.5V, fx'tal = 3.579545MHz, Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions			Min	Typ	Max	Unit
Operating Voltage Range	$V_{DD}P$	Pulse Mode	All inputs connected to V_{DD} or V_{SS}		2.0		5.5	V
	$V_{DD}T$	Tone Mode			2.0		5.5	
Memory Retention Voltage	V_{DR}				1.0			
Operating Supply Current	$I_{DD}P$	$\overline{MODE} = V_{DD}$	One key selected $\overline{HS} = V_{SS}$. All outputs unloaded			0.3	0.5	mA
	$I_{DD}T$	$\overline{MODE} = V_{SS}$				0.5	1.0	
Standby Current	$I_{SD}1$	$\overline{HS} = V_{DD} = 1.5V$	No key selected. All outputs unloaded				0.05	μA
	$I_{SD}2$	$\overline{HS} = V_{SS}$					50	
Output Current	$I_{OL}1$	$\overline{DP}$	$V_{OL} = 0.4V$	$V_{DD} = 3.5V$	1.7	5.0		mA
	$I_{OL}2$	$\overline{X'MIT\ MUTE}$		$V_{DD} = 2.5V$	0.5	1.5		
Input Voltage	V_{IH}	R1-R4. C1-C3. $\overline{HS}$. M/B			$0.8V_{DD}$		V_{DD}	V
	V_{IL}	$\overline{MODE\ SELECT}$			V_{SS}		$0.2V_{DD}$	
Input Current	$I_{IN}1$	$V_{DD} = 3.5V$ $V_{IN} = 0V$	R1-R4				116	μA
	$I_{IN}2$	$V_{DD} = 2.5V$ $V_{IN} = 0V$					50	
Valid Key Entry Time	T_{kd}				23		25.3	mS
Column and Row Scanning Frequency	F_{cr}					437		Hz
Auto Access Pause Time	T_{ap}					3.5		sec
Tone Output	V_{or}	ROW TONE ONLY	$V_{DD} = 2.5V$ $R_L = 5K$		−16.0		−12.0	dBV
			$V_{DD} = 3.5V$ $R_L = 5K$		−14.0		−11.0	
Ratio of Column to Row Tone	dB_{cr}	$V_{DD} = 3.5V$			1.0	2.0	3.0	dB
Distortion	%DIS	$V_{DD} = 3.5V$					7	%
Tone Output Delay Time	T_{psd}					1.5		mS

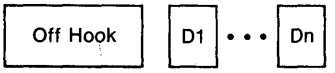
PIN DESCRIPTION

<table>
<tr><th>Pin</th><th>Name</th><th>Description</th></tr>
<tr><td>1-4
15-18</td><td>R1-R4
C1-C4</td><td>Keyboard (R1, R2, R3, R4, C1, C2, C3, C4)
These inputs can be interfaced to an XY matrix keyboard.
C1-C4 & R1-R4 are set to low at On Hook ($\overline{HS}$ = high). C1-C4 key inputs are set to low and R1-R4 are set to high at OFF HOOK ($\overline{HS}$ = low) which enables the key-input operation. Oscillator starts running when a keypress is detected. Scanning signals are presented at both column and row inputs (TYP: 437Hz) until the input key is released. Key inputs are compatible with standard 2-of-8 form or single-contact keyboard. Debouncing is provided to avoid false entry (TYP: 25mS).</td></tr>
<tr><td>5</td><td>$\overline{HS}$</td><td>Hook Switch
This input detects the state of the hook switch contact. "Off Hook" corresponds to V_{SS} condition. "On Hook" corresponds to V_{DD} condition.</td></tr>
<tr><td>6</td><td>M/B</td><td>Make/Break Ratio
This input provides the selection of the Make/Break ratio (33.3: 66.6/40:60) when M/B is connected to V_{DD}/V_{SS}.</td></tr>
<tr><td>7</td><td>$\overline{\text{MODE SELECT}}$</td><td>Mode Select Input
Pulse/DTMF mode is selected as shown in the following table.
Initial Mode means the state after going Off Hook ($\overline{HS}$→"V_{SS}")
<table>
<tr><th>$\overline{\text{MODE SELECT}}$</th><th>INITIAL MODE</th><th>SWITCHING ENTRY MODE</th></tr>
<tr><td>V_{DD}</td><td>Pulse</td><td>$\overline{\text{MODE SELECT}}$ Input = V_{SS}</td></tr>
<tr><td>V_{SS}</td><td>Tone</td><td>N/A</td></tr>
</table></td></tr>
<tr><td>8-9</td><td>OSC IN
OSC OUT</td><td>Oscillator Input/Output
These pins are provided to connect an external 3.58MHz crystal. Oscillator starts (at Off Hook) and is sustained until pulse or DTMF signals are finished.</td></tr>
<tr><td>10-11</td><td>V_{DD}, V_{SS}</td><td>Power
These are the power supply inputs. The device is designed to be operated on 2.0V to 5.5V.</td></tr>
<tr><td>12</td><td>TONE OUT</td><td>DTMF Signal Output
When a valid keypress is detected in DTMF mode appropriate low and high group frequencies are generated which hybrided the Dual Tone Output.
Tone out is Off State in pulse mode.</td></tr>
<tr><td>13</td><td>$\overline{\text{X'MIT MUTE}}$</td><td>X'mit Mute Output
<table>
<tr><th>$\overline{HS}$</th><th>$\overline{\text{X'mit Mute Output}}$</th></tr>
<tr><td>V_{DD}</td><td>"ON"</td></tr>
<tr><td>V_{SS}</td><td>Normally "OFF"
"ON" during pulse and DTMF dialing</td></tr>
</table>
(N channel open drain)</td></tr>
<tr><td>14</td><td>$\overline{DP}$, DP</td><td>Dial Pulse Out
DP: The normal output will be "OFF" during break and "ON" during make at "OFF HOOK." The output will be "ON" at "ON HOOK,"
$\overline{DP}$: The normal output will be "ON" during break and "OFF" during make at "OFF HOOK." The output will be "OFF" at "ON HOOK."</td></tr>
</table>

KEYBOARD OPERATION

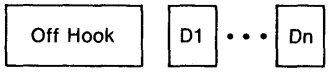
1. SINGLE MODE OPERATION

• Pulse Mode Operation



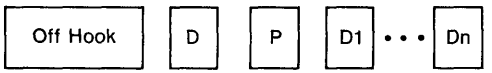
Pulse mode is defined by the initial mode after going Off Hook and latched at [D1] key entry. This is the condition under $\overline{\text{Mode Select}} = V_{DD}$.

• Tone Mode Operation



Tone mode is defined by the initial mode after going Off Hook and latched at [D1] key entry. This condition is under $\overline{\text{Mode Select}} = V_{SS}$.

• Manual Dialing with Automatic Access Pause

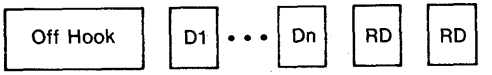


Multiple Pause key entries can be accepted and stored in the redial memory, each as a digit. Each [P] key provides 3.5 seconds pause time, but [P] key entry as first digit after going Off Hook is ignored. [*] key can also be used as pause key in pulse mode. Pause (s) can be cancelled with [P], or [RD] key during pause time in redialing.
[D] = Any numeric key.

• Redialing

Up to 32 digits can be dialed with [RD] key. [RD] key is disabled while pulse or DTMF signals are transmitted. When more then 32 digits are stored, redial is also inhibited.
[#] key can be used as [RD] key in pulse mode.

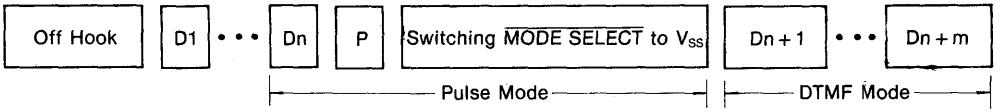
• Inhibiting Redial



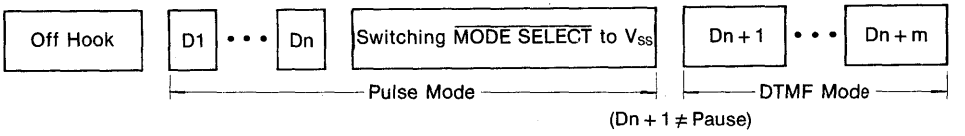
Redial can be inhibited by depressing [RD] [RD] keys after DTMF or pulse signals are transmitted.

2. PULSE/TONE SWITCHABLE OPERATION

• **Mode Switching by $\overline{\text{MODE SELECT}}$ Input**



Pulse mode is initially defined $\overline{\text{MODE SELECT}} = V_{DD}$, mode switching to DTMF can be accepted by $\overline{\text{MODE SELECT}} = V_{SS}$, DTMF mode will be set up after pulse mode is finished. In this mode, digits [Dn + 1] ... [Dn + m] are transmitted from Tone Out as DTMF signals by depressing corresponded keys.
If no [P] key is contained serially before or after mode switching, following condition is obtained.



If digit [Dn + 1] is depressed after pulse mode is finished, DTMF mode will be set up after last pulse signal ([Dn]) is generated. In this mode, digits [Dn + 1] ... [Dn + m] are transmitted from Tone Out as DTMF signals by depressing corresponded keys. If digit [Dn + 1] is depressed during dialing pulse signals. When DTMF mode is set up Hold State will be set up after last pulse signal [Dn] is finished. MODE OUT will flash to indicate this Hold State [Dn + 1] ... [Dn + m] are stored in redial memory as DTMF DATA and not transmitted from Tone Out. When it is ready to transmit DTMF data in redial memory, [RD] or [P] keys is depressed to reset this Hold State and [Dn + 1] ... [Dn + m] data are serially transmitted.

Single Tone Operation in DTMF Mode (Test mode)

1. The M/B pin is used to trig the chip into test made by applying a positive or negative pulse after "Off Hook." Test mode is sustained until On Hook. The single tone is shown in the following table which contrast with normal mode.

Normal mode

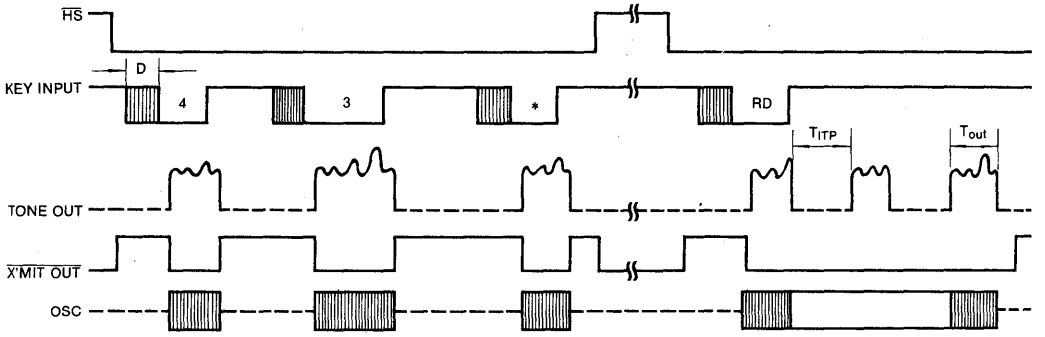
R1	1	2	3
R2	4	5	6
R3	7	8	9
R4	*	0	#
	C1	C2	C3

Single tone mode

R1	R1	C2	C3
R2	C1	C2	R2
R3	R3	C2	C3
R4	C1	R4	C3
	C1	C2	C3

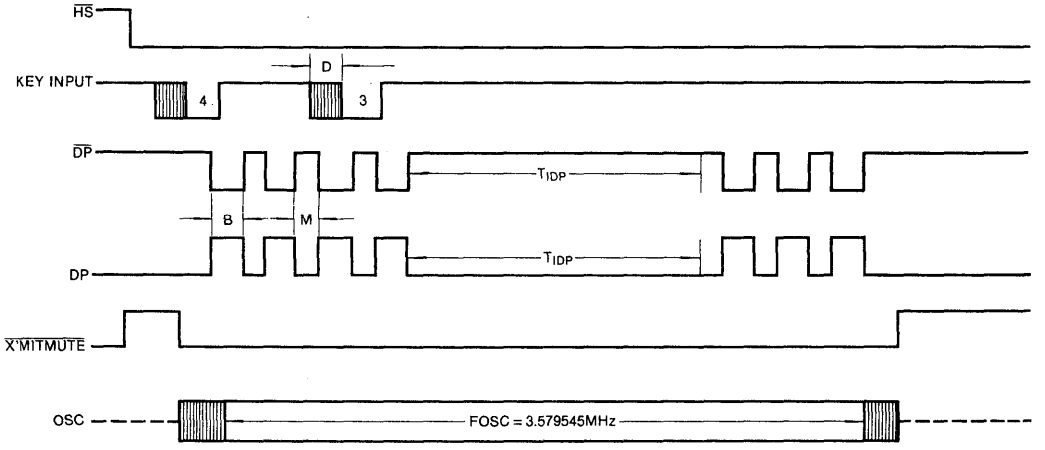
2. Single tone can be generated by simultaneously depressing two digit keys in the appropriate Row and Column. If two digit keys, not in the same Row or Column, the dual tone disabled and no output is provided.

TONE MODE TIMING ($\overline{\text{MODE SELECT}} = V_{SS}$)



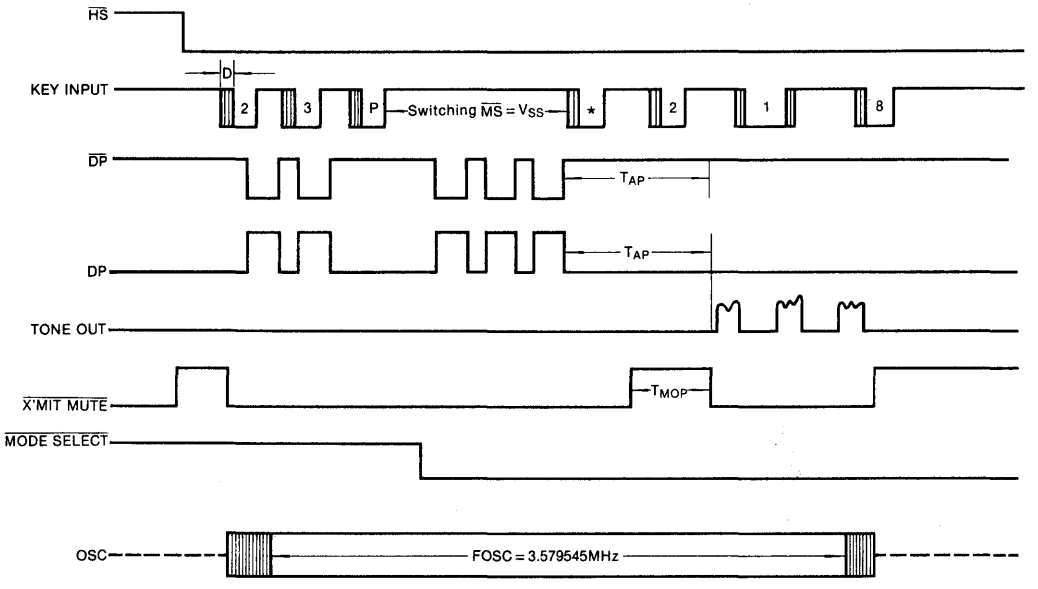
D: Debouncing Time: 25mS T_{out}: 110mS
T_{ITP}: 110mS

PULSE MODE TIMING ($\overline{\text{MODE SELECT}} = V_{DD}$)



D: Debouncing Time: 25mS
T_{IDP}: Inter Digit Pause: 879mS

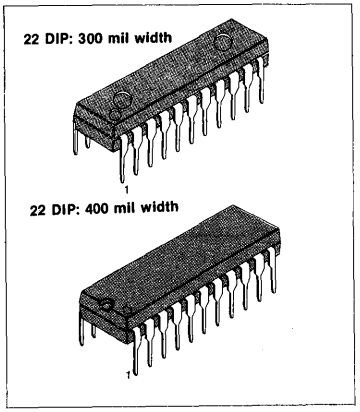
TIMING DIAGRAM (for Switching Mode Operation by $\overline{\text{MODE SELECT}}$ Input)



T_{AP}: Auto Pause Time 3.5sec

10 MEMORY TONE/ PULSE REPERTORY DIALER

The KS5822, a CMOS digital LSI, is a 10 number by 16 digit tone/pulse switchable dialer, with 32 digit redial memory. Through pin selection, switching from pulse to tone mode, 10 or 20pps and make/break ratio can be done.



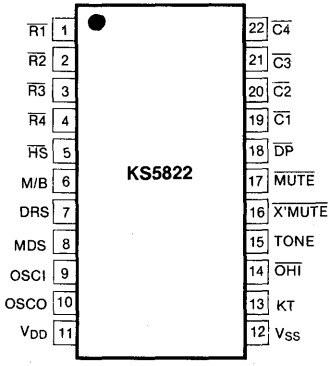
FEATURES

- **32 digit redial memory with buffer**
- **10 No x 16 digit repertory memory**
- **Tone/Pulse switchable via slide switch with multiple auto access pause (3.5 sec)**
- **Uses inexpensive TV crystal (3.579545MHz)**
- **Make/Break ratio pin selectable (1/2, 2/3)**
- **Dialing pulse rate pin selectable 10pps/20pps**
- **Two key single tone operation**
- **Redial memory cascadable with normal dialing**
- **Fully debounced 4 x 4 keyboard**
- **Low voltage operating: 2.0 ~ 5.5V**
- **Low standby current**
- **Includes power on reset function**
- **Minimum tone duration: 110mS**
- **Minimum interdigit tone pause time: 110mS**

ORDERING INFORMATION

Device	Package	Operating Temperature
KS5822N	300 mil Width	−20 ~ +70°C
KS5822E	400 mil Width	

PIN CONFIGURATION



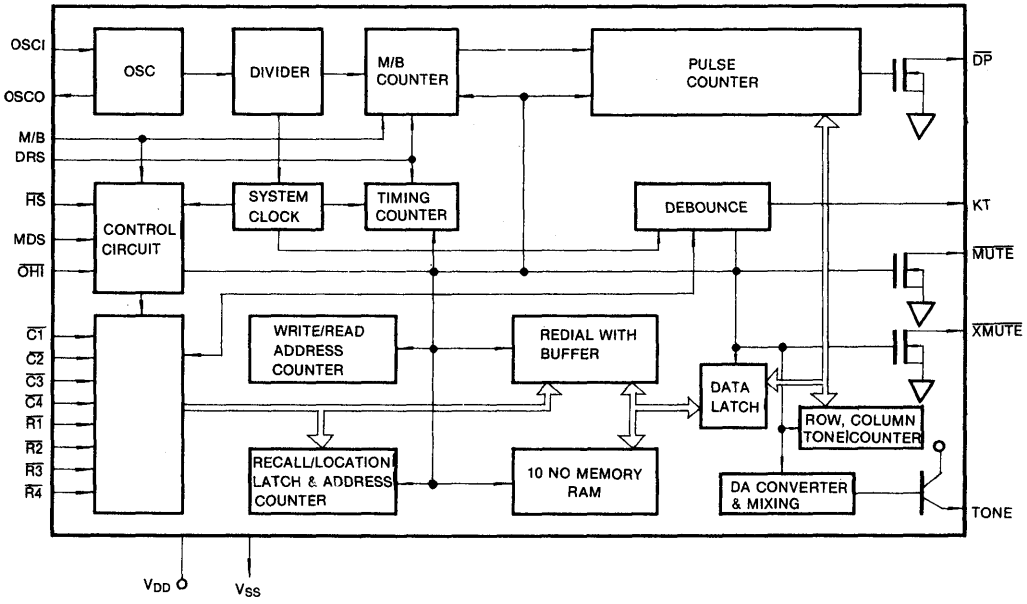
ARRANGEMENT OF KEYBOARD

1	2	3	ST	ST : Store
4	5	6	R/L	R/L : Recall/Location
7	8	9	P	P : Pause
*	0	#	RD	RD : Redial

PIN DESCRIPTION

Pin	Name	Description
1-4 19-22	$\overline{R1}$-$\overline{R4}$ $\overline{C1}$-$\overline{C4}$	Keyboard Input These inputs can be interfaced to an XY matrix keyboard.
5	$\overline{HS}$	Hook Switch Input. V_{DD} = On Hook, V_{SS} = Off Hook
6	M/B	Make/Break Ratio Select. V_{DD} = 1:2 (M/B), V_{SS} = 2:3 (M/B)
7	DRS	Dial Pulse Ratio Select V_{DD} = 20pps, V_{SS} = 10pps
8	MDS	Mode Select. V_{DD} = Pulse mode, V_{SS} = Tone mode
9	OSC IN	Oscillator Input/Output
10	OSC OUT	
11	V_{DD}	Power. This device is designed to operate on 2.0V to 5.5V
12	V_{SS}	
13	KT	Key In Tone Output.(In Pulse & Tone Mode) f_{KT} = 1.785KHz, t_{KT} = 36.6mS
14	$\overline{OHI}$	On Hook Store Inhibitive Input. V_{DD} = Store available, V_{SS} = Inhibitive store function
15	TONE	DTMF Signal Output
16	$\overline{XMUTE}$	$\overline{XMUTE}$ Output. This is a N-channel open drain output. Operating pulse and tone mode.
17	$\overline{MUTE}$	$\overline{MUTE}$ Output. Operating only pulse mode.
18	$\overline{DP}$	Dial Pulse Output. (N-chnanel open drain)

BLOCK DIAGRAM



TONE DURATION & PAUSE

Characteristic	Symbol	Typ	Unit
Tone Duration	T_D	110	mS
Minimum Pause	I_{TP}	110	mS

TONE FREQUENCIES

Input	Specified	Actual	% Error
R1	697	699.1	+0.31
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1,209	1,215.9	+0.57
C2	1,336	1,331.7	+0.32
C3	1,477	1,471.8	−0.35

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ 6.0	V
Input Voltage	V_{IN}	−0.3 ~ V_{DD} + 0.3	V
Output Voltage	V_{OUT}	−0.3 ~ V_{DD} + 0.3	V
Operating Temperature	T_a	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C
Power Dissipation	P_D	500	mW

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.5V, V_{SS} = 0V, f_{OSC} = 3.579545MHz, Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		2.0		5.5	V
Memory Retention Voltage	V_r		1.0			V
Operating Supply Current	I_{DDP}	Pulse Mode, all outputs unloaded			0.5	mA
	I_{DDT}	Tone Mode, all outputs unloaded			1.0	mA
Standby Current	I_{DD1}	$\overline{HS}$ = V_{DD} = 1.0V, all outputs unloaded		0.03	0.05	μA
	I_{DD2}	$\overline{HS}$ = V_{SS}, all outputs unloaded		30	50	μA
Output Sink Current ($\overline{DP}$, $\overline{XMUTE}$, $\overline{MUTE}$)	I_{OL1}	V_{OL} = 0.4V	1.7	5.0		mA
	I_{OL2}	V_{OL} = 0.4V, V_{DD} = 2.5V	0.5	1.5		mA
Key In Tone Current	I_{OHK}	V_{OH} = 0.4V	1.7	5.0		mA
	I_{OHL}	V_{OL} = 3.0V	1.8	5.2		mA
Input Voltage ($\overline{R1}$-$\overline{R4}$, $\overline{C1}$-$\overline{C4}$, $\overline{HS}$, MDS, M/B, DRS)	V_{IH}		0.8V_{DD}		V_{DD}	V
	V_{IL}		V_{SS}		0.2V_{DD}	V
Input Current (R1-R4, C1-C4)	I_{IH}	V_{IN} = V_{SS}			116	μA
	I_{IL}	V_{IN} = V_{SS}, V_{DD} = 2.5V			50	μA
Row Tone Level	V_{TH}	V_{DD} = 3.5V, R_L = 5KΩ	−14		−11	dBV
	V_{TL}	V_{DD} = 2.5V, R_L = 5KΩ	−16		−12	
Ratio of Column to Row Tone	dB_{cr}		1	2	3	dB
Distortion	THD				7	%
Valid Key Entry Time	T_{KD}			9.1	19.1	mS
Pause Time	t_{pa}			3.51		sec

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Pulse Interdigit Pause Time	t_{IDP1}	DRS = V_{SS}, 10pps		805.6		mS
	t_{IDP2}	DRS = V_{DD}, 20pps		402.8		
Tone Interdigit Pause Time	t_{IDT}			109.8		mS
Minimum Tone Duration	t_{TD}			109.8		mS
Minimum Key In Tone Duration	t_{KT}			36.6		mS
Key In Tone Frequency	f_{KT}			1.785		KHz
Make/Break Time	$t_{M/B}$	DRS = V_{SS}, M/B = V_{DD}, 10pps		34.33 68.66		mS
		DRS = V_{SS}, M/B = V_{SS}, 10pps		41.19 61.79		mS
Make/Break Time	$t_{M/B}$	DRS = V_{DD}, M/B = V_{DD}, 20pps		17.17 34.33		mS
		DRS = V_{DD}, M/B = V_{SS}, 20pps		20.60 30.90		mS

KEY DESCRIPTION

• 1, 2, 3, 4, 5, 6, 7, 8, 9, 0 KEYS

These are Tone/Pulse dialing signal keys in normal state but their entry right after store mode or recall mode provides store memory location.

• *, # KEYS

These are served as dialing signal at tone mode. But during pulse mode * key modulates pause and # key redials.

• PAUSE KEY

Pause key is stored in RAM as a digit and while this digit is processed no dialing can be operated. During the pause time (3.51 sec) no output is generated.

• REDIAL KEY

The redial key is valid only when it is pressed as the 1st key after OFF-HOOK operation.

• RECALL/LOCATION KEY

Location or recall number selection is enabled by detecting R/L key input.

• STORE KEY

If the ST key is allowed when the dialer is set to the corresponding condition, pressing the ST key will change the dialer into the ST mode.
The ST mode is released after the memory transfer operation is executed. This pin is a master control key. The dialing sequence will be interrupted when the key is activated.

OPERATION OF TONE/PULSE

• SYMBOL DEFINITION

T/p = Tone Mode t/P = Pulse Mode
Dp = Pulse Data: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0 Keys
Dt = Tone Data: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, *, #
Dm = Memory Location
R// = R/L Key for Recalling
r/L = R/L Key for Location
RD = Redial Key
P = Pause Key
ST = Store Key
Conv = Conversation Mode

• NORMAL DIALING IN PULSE MODE

Off Hook, t/P; Dp_1, Dp_2, ... Dpn; Conv; On Hook

• NORMAL DIALING IN TONE MODE

Off Hook, T/p; Dt_1, Dt_2, ... Dtn; Conv; On Hook

• NORMAL DIALING IN PULSE TO TONE MODE

Off Hook, t/P; Dp_1, Dp_2, ... Dpn; T/p; Dt_1, Dt_2, ... Dtn; Conv; On Hook

• REDIALING

Off Hook; RD; Conv; On Hook
Note: More than 33 digit in redial memory inhibits redial function and RD input after Off Hook is ignored.

• STORING A NUMBER FOR PULSE MODE

1) $\overline{OHI}$ = Low
Off Hook, t/P; ST; Dp_1, Dp_2, ... Dpn; r/L; Dm; On Hook
(Return to Normal Mode)

2) $\overline{OHI}$ = High
On Hook, t/P; ST; Dp_1, Dp_2, ... Dpn; r/L; Dm;
(Return to Normal Mode)

• STORING A NUMBER FOR PULSE-TO-TONE MIXED DIALING

On (Off) Hook (By Condition), t/P; ST; Dp_1, Dp_2, ... Dpn; T/p; Dt_1, Dt_2, ... Dtn; r/L; Dm; On Hook
(Return to Normal Mode)

• STORING A NUMBER FOR TONE MODE

On (Off) Hook (By Condition), T/p; ST; Dt_1, Dt_2, ... Dtn; r/L; Dm; On Hook (Return to Normal Mode)
Note: The tone data is a one digit in tone mode and the device provides 31 digit redial memory and 15 digit storing memory in tone mode.

• A NUMBER REPERTORY DIALING

Off Hook; R//; Dm; Conv; On Hook

• REPERTORY DIALING FOR CASCADED MEMORIES

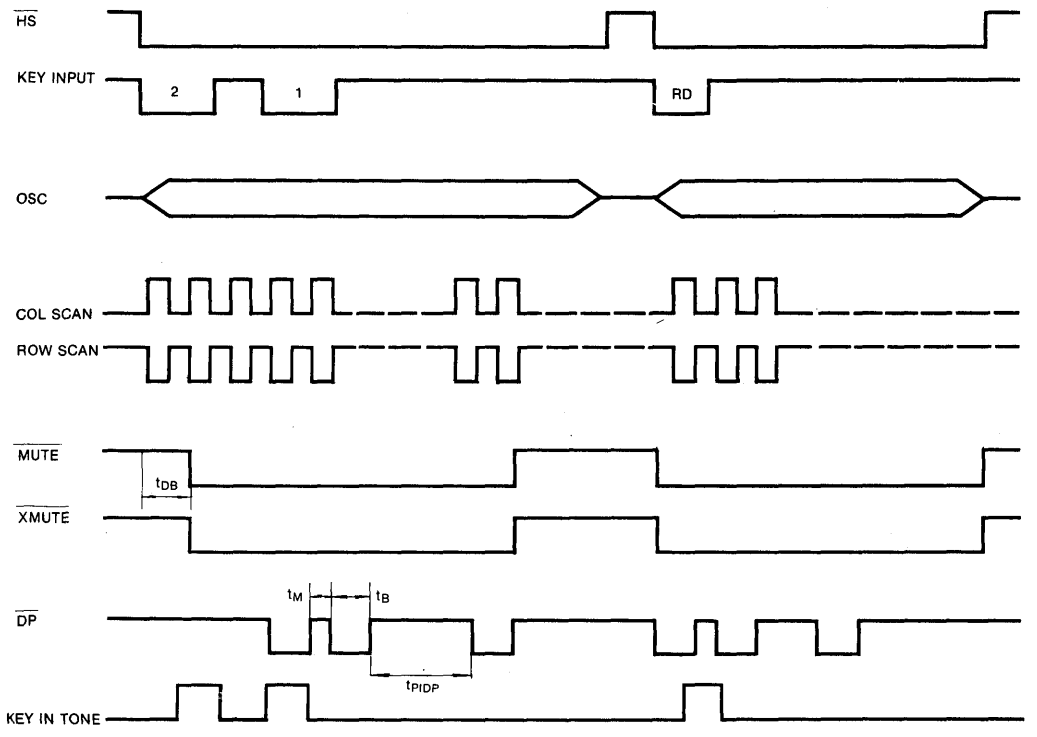
Off Hook; R//; Dm; ..... ; R//, Dm; Conv; On Hook
Note: If cascade number exceeds 32 digits, the next digit is ignored. The number cannot be redialed by being truncated.

TONE GENERATOR

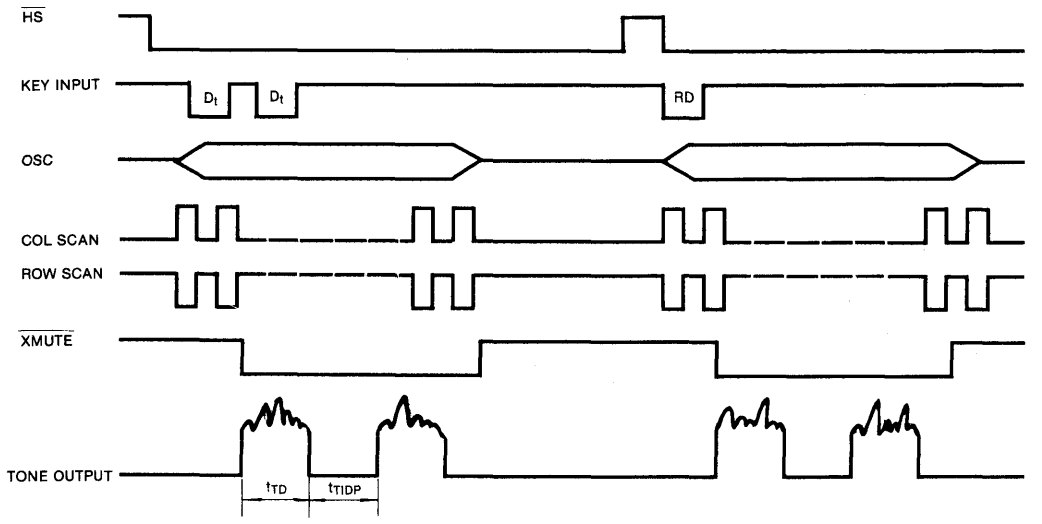
Single tone generated consists of 14 level and 28 segments. It's column tone output is 2dB pre-emphasized than row tone output.

TIMING DIAGRAM

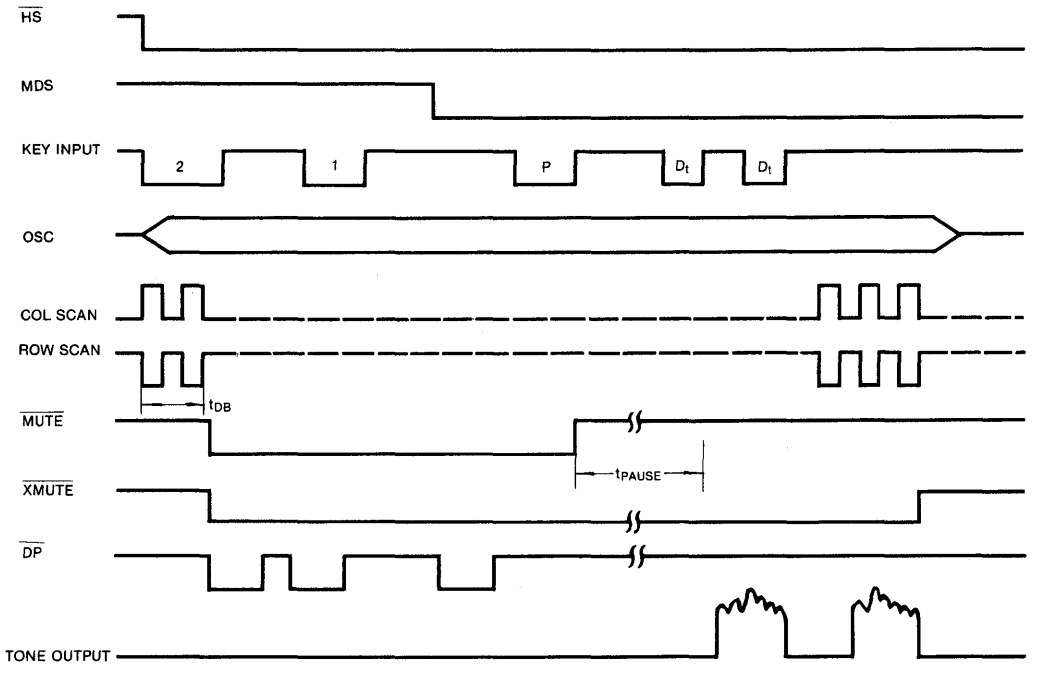
PULSE MODE



TONE MODE

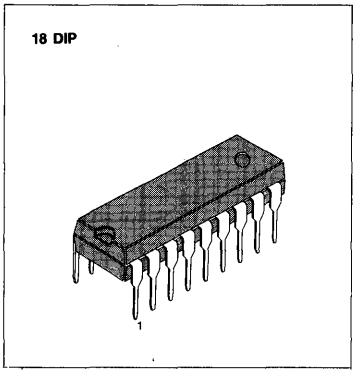


PULSE TO TONE DIALING



10 MEMORY TONE/ PULSE REPERTORY DIALER

The KS5823 series, a CMOS digital LSI, is a 10 number by 16 digit tone/pulse switchable dialer, with 32 digit redial memory. Through pin selection, switching from pulse to tone mode and make/break ratio can be done.



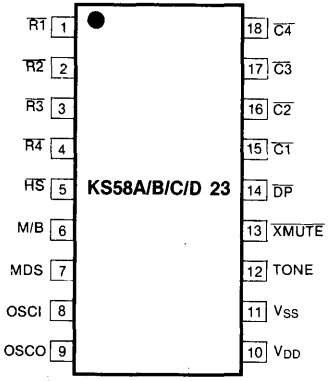
FEATURES

- **32 digit redial memory with buffer**
- **10 No x 16 digit repertory memory**
- **Tone/Pulse switchable via slide switch with multiple auto access pause (3.5 sec)**
- **Uses inexpensive TV crystal (3.579545MHz)**
- **Make/Break ratio pin selectable (1/2, 2/3)**
- **Two key single tone operation**
- **Redial memory cascadable with normal dialing**
- **Fully debounced 4 x 4 keyboard**
- **Low voltage operating: 2.0 ~ 5.5V**
- **Low standby current**
- **Includes power on reset function**
- **Minimum tone duration: 110mS**
- **Minimum interdigit tone pause time: 110mS**

ORDERING INFORMATION

Device	PPS	Storage Mode	Operating Temperature
KS58A23N	10pps	Off Hook Only	−20 ~ +70°C
KS58B23N	20pps	On/Off Hook	
KS58C23N	10pps	On/Off Hook	
KS58D23N	20pps	Off Hook Only	

PIN CONFIGURATION



ARRANGEMENT OF KEYBOARD

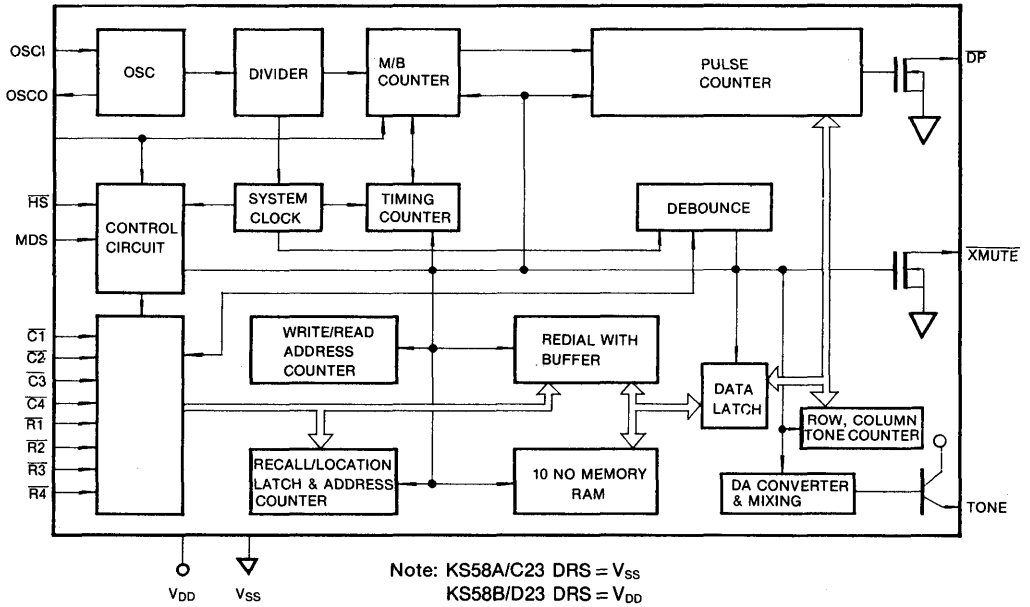
1	2	3	ST
4	5	6	R/L
7	8	9	P
*	0	#	RD

ST : Store
R/L : Recall/Location
P : Pause
RD : Redial

PIN DESCRIPTION

Pin	Name	Description
1-4	$\overline{R1}$-$\overline{R4}$	Keyboard Input These inputs can be interfaced to an XY matrix keyboard.
15-18	$\overline{C1}$-$\overline{C4}$	
5	$\overline{HS}$	Hook Switch Input. V_{DD} = On Hook, V_{SS} = Off Hook
6	M/B	Make/Break Ratio Select. V_{DD} = 1:2 (M/B), V_{SS} = 2:3 (M/B)
7	MDS	Mode Select. V_{DD} = Pulse mode, V_{SS} = Tone mode
8	OSC IN	Oscillator Input/Output
9	OSC OUT	
10	V_{DD}	Power. This device is designed to operate on 2.0V to 5.5V
11	V_{SS}	
12	TONE	DTMF Signal Output.
13	$\overline{XMUTE}$	XMUTE Output. This is a N-channel open drain output.
14	$\overline{DP}$	Dial Pulse Output. (N-chnanel open drain)

BLOCK DIAGRAM



Note: KS58A/C23 DRS = V_{SS}
KS58B/D23 DRS = V_{DD}
KS58A/D23 OHI = V_{SS}
KS58B/C23 OHI = V_{DD}

TONE DURATION & PAUSE

Characteristic	Symbol	Typ	Unit
Tone Duration	T_D	110	mS
Minimum Pause	I_{TP}	110	mS

TONE FREQUENCIES

Input	Specified	Actual	% Error
$\overline{R1}$	697	699.1	+0.31
$\overline{R2}$	770	766.2	−0.49
$\overline{R3}$	852	847.4	−0.54
$\overline{R4}$	941	948.0	+0.74
$\overline{C1}$	1,209	1,215.9	+0.57
$\overline{C2}$	1,336	1,331.7	+0.32
$\overline{C3}$	1,477	1,471.8	−0.35

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ 6.0	V
Input Voltage	V_{IN}	−0.3 ~ V_{DD} + 0.3	V
Output Voltage	V_{OUT}	−0.3 ~ V_{DD} + 0.3	V
Operating Temperature	T_a	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C
Power Dissipation	P_D	500	mW

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.5V, V_{SS} = 0V, f_{OSC} = 3.579545MHz, Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		2.0		5.5	V
Memory Retention Voltage	V_r		1.0			V
Operating Supply Current	I_{DDP}	Pulse Mode, all outputs unloaded			0.5	mA
	I_{DDT}	Tone Mode, all outputs unloaded			1.0	mA
Standby Current	I_{DD1}	$\overline{HS}$ = V_{DD} = 1.0V, all outputs unloaded		0.03	0.05	μA
	I_{DD2}	$\overline{HS}$ = V_{SS}, all outputs unloaded		30	50	μA
Output Sink Current ($\overline{DP}$, $\overline{XMUTE}$)	I_{OL1}	V_{OL} = 0.4V	1.7	5.0		mA
	I_{OL2}	V_{OL} = 0.4V, V_{DD} = 2.5V	0.5	1.5		mA
Input Voltage ($\overline{R1}$-$\overline{R4}$, $\overline{C1}$-$\overline{C4}$, $\overline{HS}$, MDS, M/B)	V_{IH}		0.8V_{DD}		V_{DD}	V
	V_{IL}		V_{SS}		0.2V_{DD}	V
Input Current (R1-R4, C1-C4)	I_{IH}	V_{IN} = V_{SS}			116	μA
	I_{IL}	V_{IN} = V_{SS}, V_{DD} = 2.5V			50	μA
Row Tone Level	V_{TH}	V_{DD} = 3.5V, R_L = 5KΩ	−14		−11	dBV
	V_{TL}	V_{DD} = 2.5V, R_L = 5KΩ	−16		−12	
Ratio of Column to Row Tone	dB_{cr}		1	2	3	dB
Distortion	THD				7	%
Valid Key Entry Time	T_{KD}			9.1	19.1	mS
Pause Time	t_{pa}			3.51		sec

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Pulse Interdigit Pause Time	t_{IDP1}	(KS58A/C23)		805.6		mS
	t_{IDP2}	(KS58B/D23)		402.8		
Tone Interdigit Pause Time	t_{IDT}			109.8		mS
Minimum Tone Duration	t_{TD}			109.8		mS
Make/Break Time	$t_{M/B}$	M/B = V_{DD}, KS58A/C23		34.33 68.66		mS
		M/B = V_{SS}, KS58A/C23		41.19 61.79		mS
Make/Break Time	$t_{M/B}$	M/B = V_{DD}, KS58B/D23		17.17 34.33		mS
		M/B = V_{SS}, KS58B/D23		20.60 30.90		mS

KEY DESCRIPTION

- **1, 2, 3, 4, 5, 6, 7, 8, 9, 0 KEYS**
  These are Tone/Pulse dialing signal keys in normal state but their entry right after store mode or recall mode provides store memory location.
- ***, # KEYS**
  These are served as dialing signal at tone mode. But during pulse mode * key modulates pause and # key redials.
- **PAUSE KEY**
  Pause key is stored in RAM as a digit and while this digit is processed no dialing can be operated. During the pause time (3.51 sec) no output is generated.
- **REDIAL KEY**
  The redial key is valid only when it is pressed as the 1st key after OFF-HOOK operation.
- **RECALL/LOCATION KEY**
  Location or recall number selection is enabled by detecting R/L key input.
- **STORE KEY**
  If the ST key is allowed when the dialer is set to the corresponding condition, pressing the ST key will change the dialer into the ST mode.
  The ST mode is released after the memory transfer operation is executed. This pin is a master control key. The dialing sequence will be interrupted when the key is activated.

OPERATION OF TONE/PULSE

- **SYMBOL DEFINITION**

T/p = Tone Mode t/P = Pulse Mode
Dp = Pulse Data: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0 Keys
Dt = Tone Data: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, *, #
Dm = Memory Location
R/l = R/L Key for Recalling
r/L = R/L Key for Location
RD = Redial Key
P = Pause Key
ST = Store Key
Conv = Conversation Mode

- **NORMAL DIALING IN PULSE MODE**

  Off Hook, t/P; Dp_1, Dp_2, ... Dpn; Conv; On Hook

- **NORMAL DIALING IN TONE MODE**

  Off Hook, T/p; Dt_1, Dt_2, ... Dtn; Conv; On Hook

- **NORMAL DIALING IN PULSE TO TONE MODE**

  Off Hook, t/P; Dp_1, Dp_2, ... Dpn; T/p; Dt_1, Dt_2, ... Dtn; Conv; On Hook

- **REDIALING**

  Off Hook; RD; Conv; On Hook
  Note: More than 33 digit in redial memory inhibits redial function and RD input after Off Hook is ignored.

- **STORING A NUMBER FOR PULSE MODE**

  1) $\overline{OHI}$ = Low (KS58A/D23)
  Off Hook, t/P; ST; Dp_1, Dp_2, ... Dpn; r/L; Dm; On Hook
  (Return to Normal Mode)

  2) $\overline{OHI}$ = High (KS58B/C23)
  On Hook, t/P; ST; Dp_1, Dp_2, ... Dpn; r/L; Dm;
  (Return to Normal Mode)

- **STORING A NUMBER FOR PULSE-TO-TONE MIXED DIALING**

  On (Off) Hook (By Condition), t/P; ST; Dp_1, Dp_2, ... Dpn; T/p; Dt_1, Dt_2, ... Dtn; r/L; Dm; On Hook
  (Return to Normal Mode)

- **STORING A NUMBER FOR TONE MODE**

  On (Off) Hook (By Condition), T/p; ST; Dt_1, Dt_2, ... Dtn; r/L; Dm; On Hook (Return to Normal Mode)
  Note: The tone data is a one digit in tone mode and the device provides 31 digit redial memory and 15 digit storing memory in tone mode.

- **A NUMBER REPERTORY DIALING**

  Off Hook; R//; Dm; Conv; On Hook

- **REPERTORY DIALING FOR CASCADED MEMORIES**

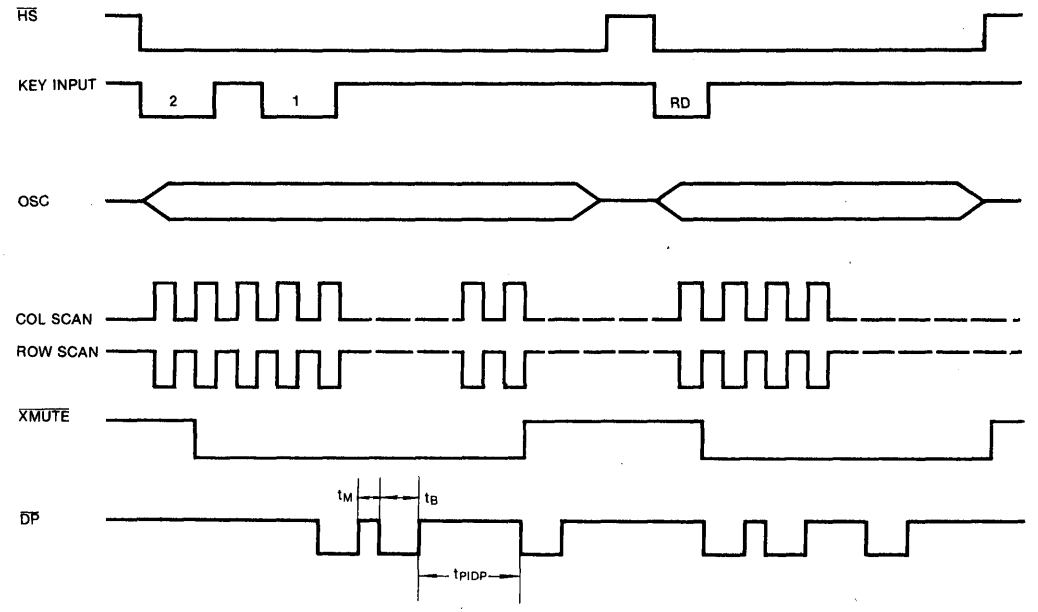
  Off Hook; R//; Dm; ..... ; R//, Dm; Conv; On Hook
  Note: If cascade number exceeds 32 digits, the next digit is ignored. The number cannot be redialed by being truncated.

TONE GENERATOR

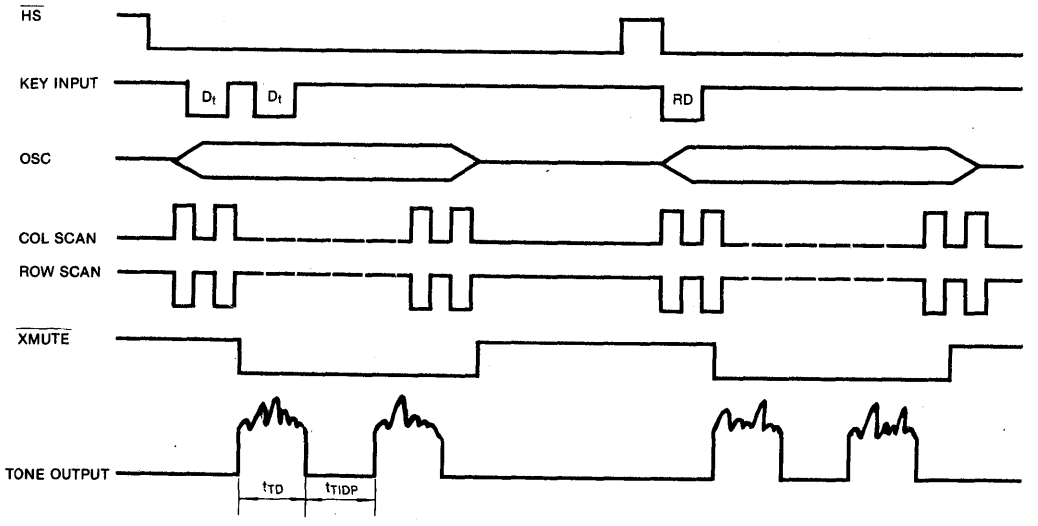
Single tone generated consists of 14 level and 28 segments. It's column tone output is 2dB pre-emphasized than row tone output.

TIMING DIAGRAM

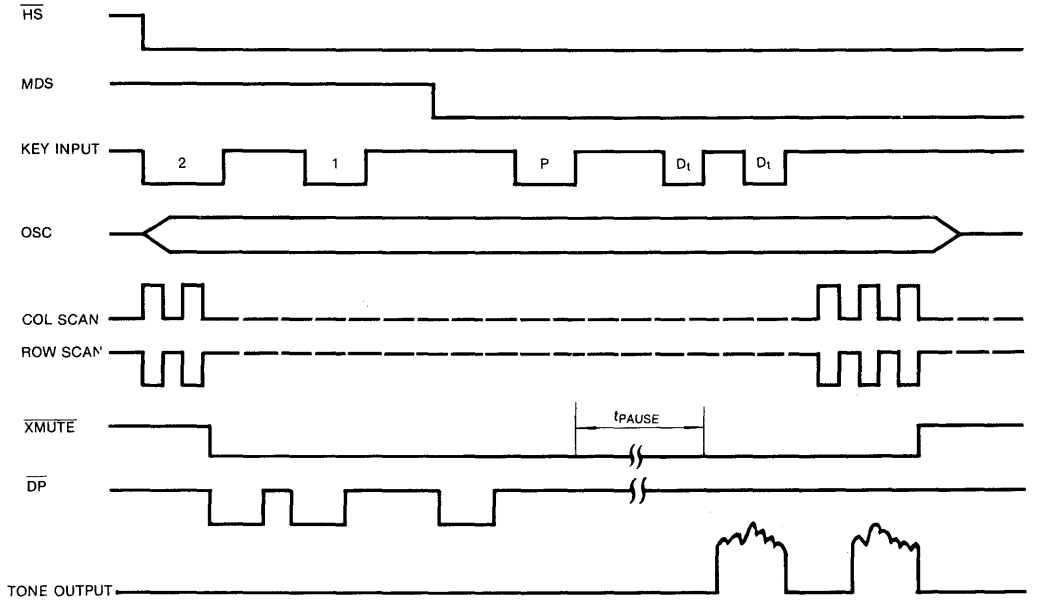
PULSE MODE



TONE MODE



PULSE TO TONE DIALING

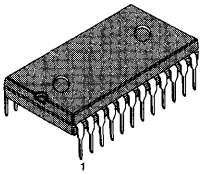


UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

The KS5824 UART, is a Si-gate CMOS IC which provides the data formatting and control to interface serial asynchronous data communications between main system and subsystems.

The bus interface of the KS5824 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially, transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the UART is programmed via the data bus during system initialization. A programmable control register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided. Exceeding Low Power dissipation is realized due to adopting CMOS process.

24 DIP



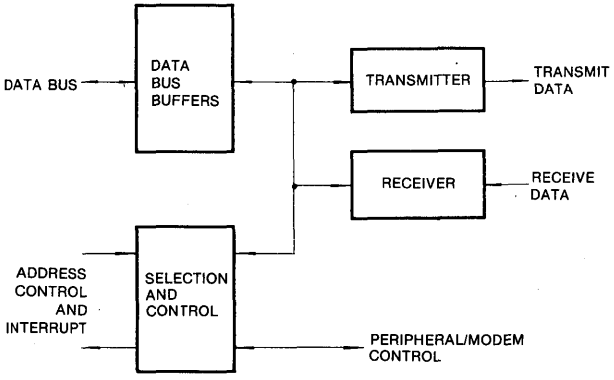
FEATURES

- **Low-power, high-speed, CMOS process**
- **Serial/parallel conversion of data**
- **8-and 9-bit transmission**
- **Optional even and odd parity**
- **Parity, overrun and framing error checking**
- **Programmable control register**
- **Optional ÷1, ÷16, and ÷64 clock modes**
- **Peripheral/modem control functions**
- **Double buffered**
- **One-or two-stop bit operation**

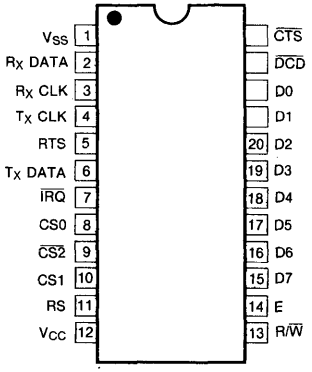
ORDERING INFORMATION

Device	Package	Operating Temperature
KS5824N	24 DIP	−20 ~ +75°C

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}*	−0.3 to +7.0	V
Input Voltage	V_{IN}*	−0.3 to +7.0	V
Maximum Output Current	I_O**	10	mA
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* With respect to V_{SS} (SYSTEM GND)

** Maximum output current is the maximum current which can flow out from one output terminal or I/O common terminal (D_0~D_7, $\overline{RTS}$, T_X Data, $\overline{IRQ}$).

Note: Permanent IC damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions are exceeded, it could affect reliability of IC.

3

RECOMMENDED OPERATING CONDITIONS

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}*	4.5	5.0	5.5	V
Input "Low" Voltage		V_{IL}*	0	—	0.8	V
Input "High" Voltage	D_0~D_7, RS, T_X CLK, $\overline{DCD}$, $\overline{CTS}$, R_X Data	V_{IH}*	2.0	—	V_{CC}	V
	CS_0, $\overline{CS_2}$, CS_1, R/$\overline{W}$, E, R_X CLK		2.2	—	V_{CC}	
Operating Temperature		T_{opr}	−20	25	75	°C

* With respect to V_{SS} (SYSTEM GND)

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Input "High" Voltage	D_0 ~ D_7, RS, T_X CLK, $\overline{DCD}$, $\overline{CTS}$, R_X Data	V_{IH}		2.0		V_{CC}	V
	CS_0, $\overline{CS_2}$, CS_1, R/$\overline{W}$, E, R_X CLK			2.2		V_{CC}	
Input "Low" Voltage	All inputs	V_{IL}		−0.3		0.8	V
Input Leakage Current	R/$\overline{W}$, CS_0, CS_1, $\overline{CS_2}$, E	I_{IN}	V_{IN} = 0 ~ V_{CC}	−2.5		2.5	μA
Three-State (Off State) Input Current	D_0 ~ D_7	I_{TSI}	V_{IN} = 0.4 ~ V_{CC}	−10		10	μA
Output "High" Voltage	D_0 ~ D_7	V_{OH}	I_{OH} = −205μA	2.4			V
	T_X data, $\overline{RTS}$		I_{OH} = −100μA	2.4			
Output "Low" Voltage	All outputs	V_{OL}	I_{OH} = 1.6mA			0.4	V

DC CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Output Leakage Current (Off State)	$\overline{IRQ}$	I_{LOH}	$V_{OH} = V_{CC}$	—	—	10	μA
Input Capacitance	$D_0 \sim D_7$	C_{IN}	$V_{IN} = 0V$, $Ta = 25°C$, $f = 1.0MHz$	—	—	12.5	pF
	E, T_X CLK, R_X CLK, R/$\overline{W}$, $\overline{RS}$, R_X Data, CS_0, CS_1, $\overline{CS_2}$, $\overline{CTS}$, $\overline{DCD}$			—	—	7.5	
Output Capacitance	$\overline{RTS}$, T_X Data	C_{OUT}	$V_{IN} = 0V$, $Ta = 25°C$ $f = 1.0MHz$	—	—	10	pF
	$\overline{IRQ}$			—	—	5.0	
Supply Current	• Under transmitting and receiving operation • 500 kbps • Data bus in R/$\overline{W}$ operation	I_{CC}	E = 1.0MHz	—	—	3	mA
			E = 1.5MHz	—	—	4	
			E = 2.0MHz	—	—	5	
	• Chip is not selected • 500 kbps • Under non transmitting and receiving operation • Input level (Except E) V_{IH} min = $V_{CC} - 0.8V$ V_{IL} max = 0.8V		E = 1.0MHz	—	—	200	μA
			E = 1.5MHz	—	—	250	
			E = 2.0MHz	—	—	300	

AC CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $Ta = -20 \sim +75°C$, unless otherwise noted.)

1. TIMING OF DATA TRANSMISSION

Characteristic		Symbol	Test Conditions	Min	Max	Unit
Minimum Clock Pulse Width	÷1 Mode	PW_{CL}	Fig. 1	900	—	ns
	÷16, ÷64 Modes			600	—	ns
	÷1 Mode	PW_{CH}	Fig. 2	900	—	ns
	÷16, ÷64 Modes			600	—	ns
Clock Frequency	÷1 Mode	f_C		—	500	KHz
	÷16, ÷64 Modes			—	800	KHz
Clock-to-Data Delay for Transmitter		t_{TDD}	Fig. 3	—	600	ns
Receive Data Setup Time	÷1 Mode	t_{RDSU}	Fig. 4	250	—	ns
Receive Data Hold Time	÷1 Mode	t_{RDH}	Fig. 5	250	—	ns
$\overline{IRQ}$ Release Time		t_{IR}	Fig. 6	—	1200	ns
$\overline{RTS}$ Delay Time		t_{RTS}	Fig. 6	—	560	ns
Rise Time and Fall Time	Except E	t_r, t_f		—	1000*	ns

* 1.0μs or 10% of the pulse width, whichever is smaller.

2. BUS TIMING CHARACTERISTICS

1) READ

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Enable Cycle Time	$t_{cyc}E$	Fig. 7	1000	—	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 7	450	—	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 7	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 7	80	—	ns
Data Delay Time	t_{DDR}	Fig. 7	—	290	ns
Data Hold Time	t_H	Fig. 7	20	100	ns
Address Hold Time	t_{AH}	Fig. 7	10	—	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 7	—	25	ns

2) WRITE

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Enable Cycle Time	$t_{cyc}E$	Fig. 8	1000	—	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 8	450	—	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 8	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 8	80	—	ns
Data Setup Time	t_{DSW}	Fig. 8	165	—	ns
Data Hold Time	t_H	Fig. 8	10	—	ns
Address Hold Time	t_{AH}	Fig. 8	10	—	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 8	—	25	ns

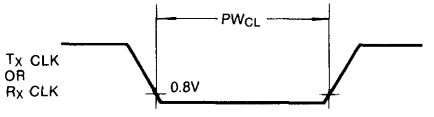


Fig. 1 Clock Pulse Width, "Low" State

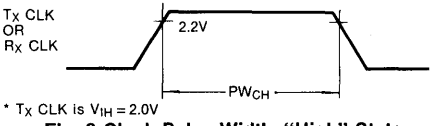


Fig. 2 Clock Pulse Width, "High" State

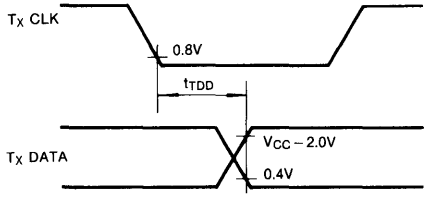


Fig. 3 Transmit Data Output Delay

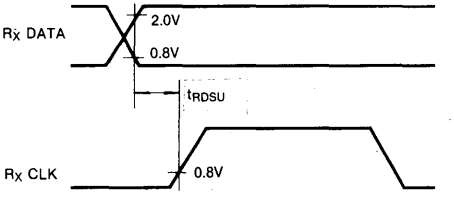


Fig. 4 Receive Data Setup Time (÷1 Mode)

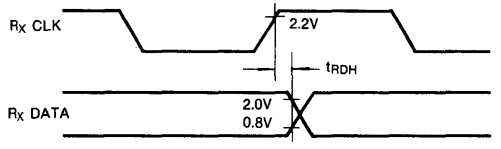


Fig. 5 Receive Data Hold Time (÷1 Mode)

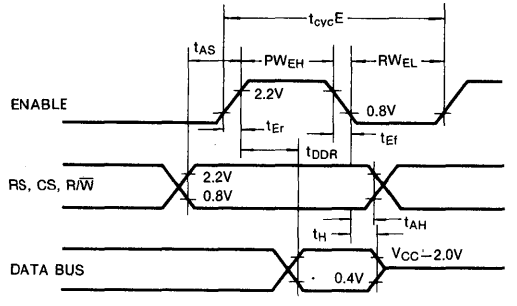
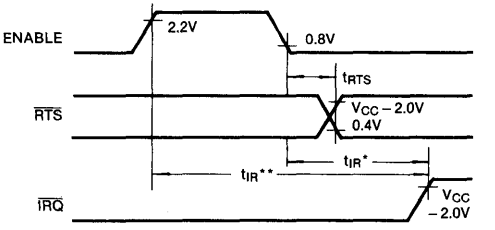


Fig. 7 Bus Read Timing Characteristics (Read information from UART)



* (1) $\overline{IRQ}$ Release Time applied to R_X Data Register read operation.
(2) $\overline{IRQ}$ Release Time applied to T_X Data Register write operation
(3) $\overline{IRQ}$ Release Time applied to control Register write TIE = 0, RIE = 0 operation.

** $\overline{IRQ}$ Release Time applied to R_X Data Register read operation right after read status register, when $\overline{IRQ}$ is asserted by $\overline{DCD}$ rising edge.

Note: Note that following take place when $\overline{IRQ}$ is asserted by the detection of transmit data register empty status. $\overline{IRQ}$ is released to "High" asynchronously with E signal when $\overline{CTS}$ goes "High". (Refer to Figure 14)

Fig. 6 $\overline{RTS}$ Delay and $\overline{IRQ}$ Release Time

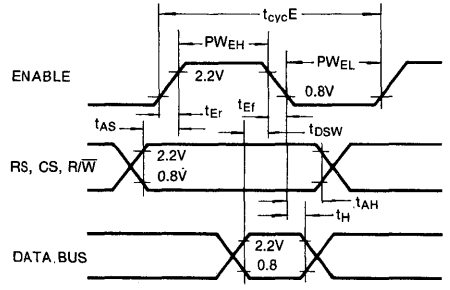
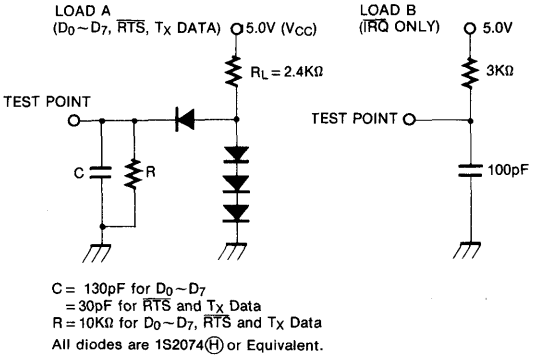


Fig. 8 Bus Write Timing Characteristics (Write information into UART)



C = 130pF for $D_0 \sim D_7$
= 30pF for $\overline{RTS}$ and T_X Data
R = 10KΩ for $D_0 \sim D_7$, $\overline{RTS}$ and T_X Data
All diodes are 1S2074(H) or Equivalent.

Fig. 9 Bus Timing Test Loads

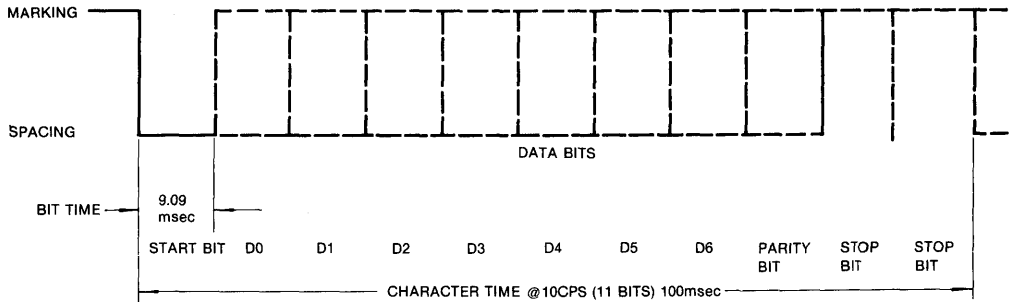


Fig. 10 110 Baud Serial ASCII Data Timing

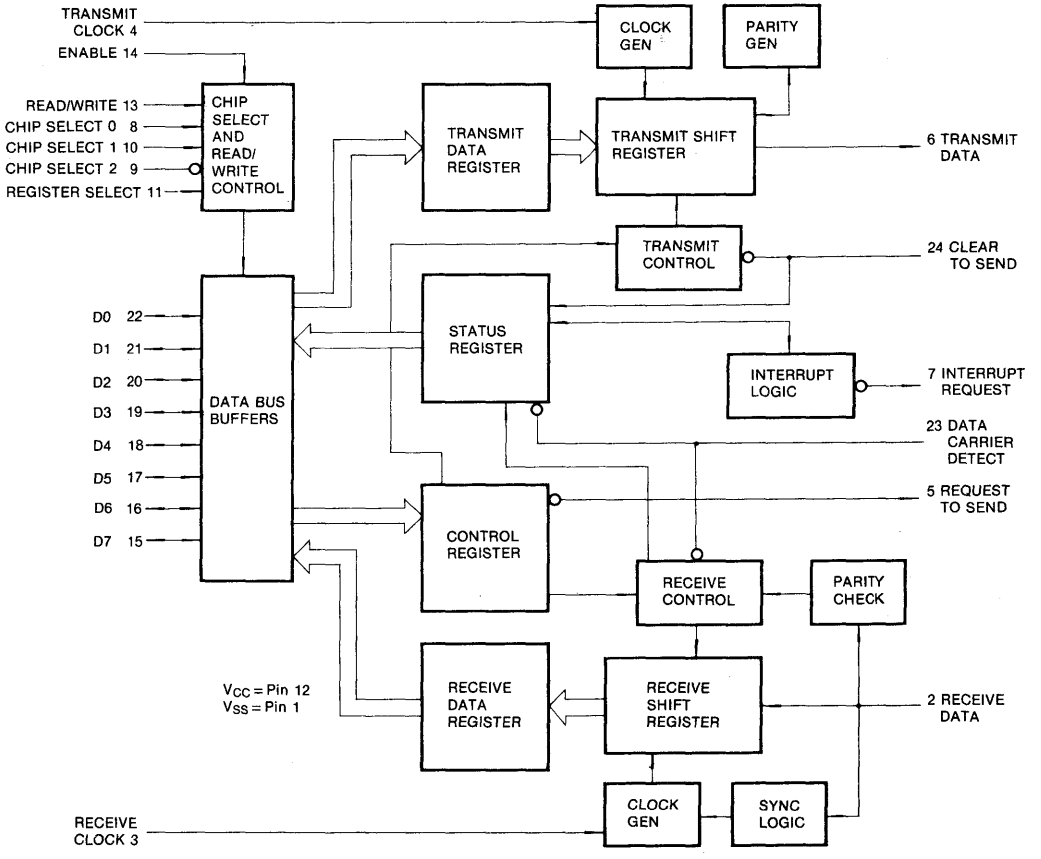


Fig. 11 Expanded Block Diagram

DEVICE OPERATION

At the bus interface, the UART appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the UART functional configuration when the communications channel is required. During the first master reset, the $\overline{IRQ}$ and $\overline{RTS}$ outputs are held at level 1. On all other master resets, the $\overline{RTS}$ output can be programmed high or low with the $\overline{IRQ}$ output held high. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTS}$ whenever master reset is utilized. The UART also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset which must be applied prior to operating the UART. After master resetting the UART, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

TRANSMIT

A typical transmitting sequence consists of reading the UART. Status Register either as a result of an interrupt or in the UART's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of 8 or 32 low samples on the receive line in the divide-by-16 and 64 modes respectively. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit UART bus when a Read Data command is received from the MPU. When parity has been selected for a 7-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

UART INTERFACE SIGNALS FOR MPU

The KS5824 interfaces to the MPU with an 8-bit bidirectional data bus, three chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals permit the MPU to have complete control over the KS5824.

UART Bidirectional Data (D0-D7) — The bidirectional data lines (D0-D7) allow for data transfer between the KS5824 and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an UART read operation.

UART Enable (E) — The Enable signal, E, is a high-impedance TTL-compatible input that enables the bus input/output data buffers and clocks data to and from the KS5824.

Read/Write (R/$\overline{W}$) — The Read/Write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the UART's input/output data bus interface. When Read/Write is high (MPU Read cycle), KS5824 output drivers are turned on and a selected register is read. When it is low, the KS5824 output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the KS5824.

Chip Select (CS0, CS1, $\overline{CS2}$) — These three high-impedance TTL-compatible input lines are used to address the KS5824. The KS5824 is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from the KS5824, are then performed under the control of the Enable Signal, Read/Write, and Register Select.

Register Select (RS) — The Register Select line is a high-impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request ($\overline{IRQ}$) — Interrupt Request is a TTL-compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the UART is set. The $\overline{IRQ}$ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the UART. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5•CR6), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTS}$) being high or the UART being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTS}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred, or Data Carrier Detect ($\overline{DCD}$) has gone high. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the UART. Interrupts caused by Overrun or loss of $\overline{DCD}$ are cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the UART. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

CLOCK INPUTS

Separate high-impedance TTL-compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16, or 64 times the data rate may be selected.

Transmit Clock (T_X CLK) —The Transmit Clock input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

Receive Clock (R_X CLK) — The Receive Clock input is used for synchronization of received data. (In the ÷1 mode, the clock and data must be synchronized externally.) The receiver samples the data on the positive transition of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (R_X Data) — The Receive Data line is a high-impedance TTL-compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used.

Transmit Data (T_X Data) — The Transmit Data output line transfers serial data to a modem or other peripheral.

PERIPHERAL/MODEM CONTROL

The UART includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTS}$) — This high-impedance TTL-compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTS}$) — The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTS}$; output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTS}$ output is low (the active state). This output can also be used for Data Terminal Ready (DTR).

Data Carrier Detect ($\overline{DCD}$) — This high-impedance TTL-compatible input provides automatic control, such as in the receiving end of a communications link by means of a modem Data Carrier Detect output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the UART when high. A low-to-high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receive Interrupt Enable bit is set. The Rx CLK must be running for proper $\overline{DCD}$ operation.

UART REGISTERS

The expanded block diagram for the UART indicates the internal registers on the chip that are used for the status, control, receiving, and transmitting of data. The content of each of the registers is summarized in Table 1.

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the UART has been addressed with RS high and R/$\overline{W}$ low. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within 1-bit time of the training edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the UART and selecting the Receive Data Register with RS and R/$\overline{W}$ high when the UART is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

DEFINITION OF UART REGISTER CONTENTS

Data Bus Line Number	Buffer Address			
	RS • R/$\overline{W}$ Transmit Data Register (Write Only)	RS • R/$\overline{W}$ Receive Data Register (Read Only)	$\overline{RS}$ • R/$\overline{W}$ Control Register (Write Only)	$\overline{RS}$ • R/$\overline{W}$ Status Register (Read Only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR0)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect ($\overline{DCD}$)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear-to-Send ($\overline{CTS}$)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Receive Interrupt Enable (CR7)	Interrupt Request ($\overline{IRQ}$)

* Leading bit = LSB = Bit 0

** Data bit will be zero in 7 bit plus parity modes

*** Data bit is "don't care" in 7 bit plus parity modes.

CONTROL REGISTER

The UART Control Register consists of eight bits of write-only buffer that are selected when RS and R/$\overline{W}$ are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) — The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the UART. Additionally, these bits are used to provide a master reset for the UART which clears the Status Register (except for external conditions on $\overline{CTS}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the UART. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) — The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows;

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) — Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTS}$) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled.
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled.
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled.
1	1	RTSi: low. Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

Receive Interrupt Enable Bit (CR7) — The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7): Receive Data Register Full Overrun or a low-to-high transition on the Data Carrier Detect ($\overline{DCD}$) signal line.

STATUS REGISTER

Information on the status of the UART is available to the MPU by reading the UART Status Register. This read-only register is selected when RS is low and R/$\overline{W}$ is high. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the UART.

Receive Data Register Full (RDRF), Bit 0 — Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 — The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{DCD}$), Bit 2 — The Data Carrier Detect bit will be high when the $\overline{DCD}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes and Interrupt Request to be generated when the Reoeive Interrupt Enable is set. It remains high after the $\overline{DCD}$ input is returned low until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the $\overline{DCD}$ input remains high after read

status and read data or master reset has occurred, the interrupt is cleared, the $\overline{DCD}$ status bit remains high and will follow the $\overline{DCD}$ input.

Clear-to-Send ($\overline{CTS}$), Bit 3 — The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the Clear-to-Send status bit.

Framing Error (FE), Bit 4 — Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 — Overrun is an error flag the indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

Parity Error (PE), Bit 6 — The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request ($\overline{IRQ}$), Bit 7 — The $\overline{IRQ}$ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is low the $\overline{IRQ}$ bit will be high to indicate the interrupt or service request status. $\overline{IRQ}$ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

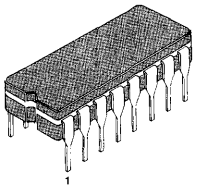
PCM TRANSMIT/RECEIVE FILTER

The KT3040 PCM CODEC Filter is a monolithic circuit that provides the transmit and receive filtering necessary to interface a voice telephone circuit to a time division multiplexed application in 8KHz sampling system. The device consists of two switched capacitor filters, transmit and receive, and power amplifiers which may be used to drive a transformer hybrid (2 to 4 wire converter) or an electronic hybrid (SLIC). If an electronic hybrid is used, the power amplifiers are not needed and may be deactivated to minimize power dissipation. The transmit filter is a fifth order low pass filter in series with a fourth order high pass filter. It provides a flat band pass filter which will pass frequencies between 200Hz and 3400Hz and provides rejection of the 50/60Hz power line frequency as well as the anti aliasing needed in an 8KHz sampling system. The receive filter is a low pass filter which smooths the voltage steps present in the CODEC output waveform and provides the sin x/x correction necessary to give unity gain in the passband for the CODEC-decoder-and-receive-filter pair.

FEATURES

- **Exceeds all D3/D4 and CCITT specifications**
- **Low power consumption: 45 mW (0 dBm0 into 600Ω)**
  30 mW (power amps disabled)
- **Power down mode: 0.5 mW**
- **External gain adjustment, both transmit and receive filters.**
- **Transmit filter includes 50/60Hz rejection**
- **Receive filter includes sin x/x compensation**
- **Direct interface with transformer or electronic telephone hybrids**
- **TTL and CMOS compatible logic**
- **Power supplies: + 5V, − 5V**
- **All inputs protected against static discharge due to handling**
- **300 mil ceramic package available**

16 CERDIP



ORDERING INFORMATION

Device	Package	Operating Temperature
KT3040N	Plastic	− 25 ~ + 125°C
KT3040AN	Plastic	
KT3040J	Ceramic	
KT3040AJ	Ceramic	

3

BLOCK DIAGRAM

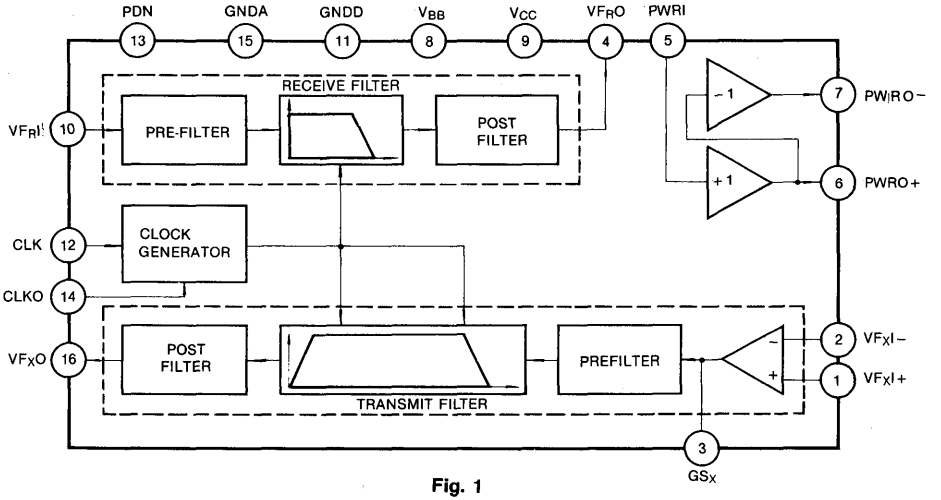
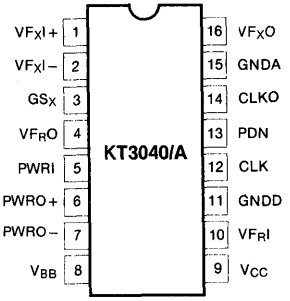


Fig. 1

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltages	V_{CC}, V_{BB}	±7	V
Power Dissipation	P_D	1	W/PKG
Input Voltage	V_{IN}	±7	V
Output Short-Circuit Duration	$T_{S.C\ OUT}$	Continuous	sec
Operating Temperature Range	Ta	−25 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Lead Temperature (Soldering 10 seconds)	T_L	300	°C

DC ELECTRICAL CHARACTERISTICS

(Ta = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, f_C = 2.048MHz, GNDA = 0V, GNDD = 0V; unless otherwise specified)

Characteristic	Symbol	Test Conditions	KT3040			KT3040A			Unit
			Min	Typ	Max	Min	Typ	Max	
POWER CONSUMPTION									
V_{CC} Standby Current	I_{CC}	PDN = High		50	400		50	100	μA
V_{BB} Standby Current	I_{BB}	PDN = High		50	400		50	100	μA
V_{CC} Operating Current	I_{CC1}	PWRI = V_{BB}, Power amp inactive		3	4		3	4	mA
V_{BB} Operating Current	I_{BB1}	PWRI = V_{BB}, Power amp inactive		3	4		3	4	mA
V_{CC} Operating Current	I_{CC2}	R_L = 600Ω connected between PWRO+ and PWRO−, Input Level = 0 dBm0 (Note 1)		4.6	6.4		4.6	6.4	mA
V_{BB} Operating Current	I_{BB2}	(Note 1)		4.6	6.4		4.6	6.4	mA
DIGITAL INTERFACE									
CLK Input Current	I_{INC}	$V_{BB} \leq V_{IN} \leq V_{CC}$	−10		10	−10		10	μA
PDN Input Current	I_{INP}	$V_{BB} \leq V_{IN} \leq V_{CC}$	−100			−100			μA
CLKO Input Current	I_{INO}	$V_{BB} \leq V_{IN} \leq V_{CC} - 0.5$	−10		0.1	−10		0.1	μA
High Level Input Voltage	V_{IH}	Except CLKO	2.2		V_{CC}	2.2		V_{CC}	V
Low Level Input Voltage	V_{IL}	Except CLKO	0		0.8	0		0.8	V
High Level Input Voltage	V_{IHO}	CLKO Pin	$V_{CC} - 0.5$		V_{CC}	$V_{CC} - 0.5$		V_{CC}	V
Low Level Input Voltage	V_{ILO}	CLKO Pin	V_{BB}		$V_{BB} + 0.5$	V_{BB}		$V_{BB} + 0.5$	V
Input Intermediate Voltage	V_{IIO}	CLKO Pin	−0.8		0.8	−0.8		0.8	V

DC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	KT3040			KT3040A			Unit
			Min	Typ	Max	Min	Typ	Max	
TRANSMIT FILTER GAIN SETTING AMPLIFIER									
V_{FXI} Input Leakage Current	IB_XI	$V_{BB} \leq V_{FXI} \leq V_{CC}$	−100		100	−100		100	nA
V_{FXI} Input Resistance	RI_XI	$V_{BB} \leq V_{FXI} \leq V_{CC}$	10			10			MΩ
V_{FXI} Input Offset Voltage	VOS_XI	$-2.5V \leq V_{IN} \leq +2.5V$	−20		20	−20		20	mV
V_{FXI} Common Mode Range	V_{CM}		−2.5		2.5	−2.5		2.5	V
Common Mode Rejection Ratio	CMRR	$-2.5V \leq V_{IN} \leq 2.5V$	60			60			dB
Power Supply Rejection Ratio of V_{CC} or V_{BB}	PSRR		60			60			dB
Open Loop Output Resistance of GS_X	R_{OL}			1			1		KΩ
Minimum Load Resistance of GS_X	R_{LXI}		10			10			KΩ
Maximum Load Capacitance of GS_X	C_{OL}				100			100	pF
Output Voltage Swing of GS_X	V_{OXI}	$R_L \geq 10K\Omega$	±2.5			±2.5			V
Open Loop Voltage Gain of GS_X	A_{VOL}	$R_L \geq 10K\Omega$	5,000			5,000			V/V
Open Loop Unity Gain Bandwidth of GS_X	f_C			2			2		MHz

AC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta = 25°C. All parameters are specified for a signal level of 0dBm0 at 1KHz. The 0dBm0 level is assumed to be $1.54V_{rms}$ measured at the output of the transmit or receive filter)

Characteristic	Symbol	Test Conditions	KT3040			KT3040A			Unit
			Min	Typ	Max	Min	Typ	Max	
TRANSMIT FILTER (Transmit filter input OP amp set to the non-inverting unity gain mode, with $V_{FXI} = 1.09V_{rms}$ unless otherwise noted)									
Minimum Load Resistance of V_{FXO}	RL_X	$-2.5V < V_{OUT} < 2.5V$ $-3.2V < V_{OUT} < 3.2V$	3 10			3 10			KΩ KΩ
Load Capacitance V_{FXO}	CL_X				100			100	pF
Power Supply Rejection Ratio, V_{FXO}	PSRR1	$f = 1KHz$, $V_{FXI} = 0V_{rms}$, V_{CC} Pin	30			30			dB
Power Supply Rejection Ratio, V_{FXO}	PSRR2	$f = 1KHz$, $V_{FXI} = 0V_{rms}$, V_{BB} Pin	35			35			dB
Absolute Gain	G_{AX}	f = 1KHz	2.875	3.0	3.125	2.9	3.0	3.1	dB
Gain Relative to G_{AX}	G_{RX}	Below 50Hz			-35			-35	dB
		50Hz		-41	-35		-41	-35	dB
		60Hz		-35	-30		-35	-30	dB
		200Hz	-1.5		0.05	-1.5		0	dB
		300Hz to 3KHz	-0.15		0.15	-0.125		0.125	dB
		3.3KHz	-0.35		0.03	-0.35		0.03	dB
		3.4KHz	-0.7		-0.1	-0.7		-0.1	dB
		4.0KHz		-15	-14		-15	-14	dB
		4.6KHz and above			-32			-32	dB
Absolute Delay at 1KHz	D_{AX}				230			230	μS
Differential Envelope Delay from 1KHz to 2.6KHz	D_{DX}				60			60	μS
Single Frequency Distortion Products	D_{PX1}				-48			-48	dB
Distortion at Maximum Signal Level	D_{PX2}	Gain = 20dB, $R_L = 10K$ $0.16V_{rms}$, 1KHz Signal Applied to V_{FXI}			-45			-45	dB
Total C Message Noise at V_{FXO}	N_{CX2}	Gain setting OP amp at 20dB Gain		3	6		2	5	dB_{rnco}
Total C Message Noise at V_{FXO}	N_{CX2}	Gain setting OP amp at 20dB Gain		3	6		3	6	dB_{rnco}
Temperature Coefficient of 1KHz Gain	G_{AXT}			0.0004			0.0004		dB/°C
Supply Voltage Coefficient of 1KHz Gain	G_{AXS}	$V_{CC} = 5.0V \pm 5\%$ $V_{BB} = -5.0V \pm 5\%$		0.01			0.01		dB/V

AC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	KT3040			KT3040A			Unit
			Min	Typ	Max	Min	Typ	Max	
Crosstalk, Rx to Tx 20 log $\frac{V_{FXO}}{V_{FRO}}$	CT_{RX}	Rx filter output = $2.2V_{rms}$ $V_{FXI} = 0V_{rms}$, f = 0.2KHz to 3.4KHz measure V_{FXO}			−70			−70	dB
Gain Tracking Relative to G_{AX}	G_{RXL}	Output Level = +3dBm0 +2dBm0 to −40dBm0 −40dBm0 to −55dBm0	−0.1 −0.05 −0.1		0.1 0.05 0.1	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sinx/x filter with an input signal level of $1.54V_{rms}$)									
Input Leakage Current, V_{FRI}	I_{IR}	$-3.2V \leq V_{IN} \leq 3.2V$	−100		100	−100		100	nA
Input Resistance, V_{FRI}	R_{IR}		10			10			MΩ
Output Resistance, V_{FRO}	R_{OR}			1	3		1	3	Ω
Load Capacitance, V_{FRO}	C_{LR}				100			100	pF
Load Resistance, V_{FRO}	R_{LR}		10			10			KΩ
Power Supply Rejection of V_{CC} or V_{BB}, V_{FRO}	PSRR3	V_{FRI} connected to GNDA, f = 1KHz	35			35			dB
Output DC Offset, V_{FRO}	V_{OS}	V_{FRI} connected to GNDA	−200		200	−200		200	mV
Absolute Gain	G_{AR}	f = 1KHz	−0.125		0.125	−0.1		0.1	dB
Gain Relative to Gain at 1KHz	G_{RR}	Below 300Hz 300Hz to 3.0KHz 3.3KHz 3.4KHz 4.0KHz 4.6KHz and above	 −0.15 0.35 −0.7		0.125 0.15 0.03 −0.1 −14 −32	 −0.125 0.35 −0.7		0.125 0.125 0.03 −0.1 −14 −32	dB dB dB dB dB dB
Absolute Delay at 1KHz	D_{AR}				100			100	μS
Differential Envelope Delay 1KHz to 2.6KHz	D_{DR}				100			100	μS
Single Frequency Distortion Products	D_{PR1}	f = 1KHz			−48			−48	dB
Distortion at Maximum Signal Level	D_{PR2}	$2.2V_{rms}$ Input sinx/x filter, f = 1KHz, R_L = 10K			−45			−45	dB
Total C Message Noise at V_{FRO}	N_{CR}			3	5		3	5	dB_{rnco}
Temperature Coefficient of 1KHz Gain	G_{ART}			0.0004			0.0004		dB/°C
Supply Voltage Coefficient of 1KHz Gain	G_{ARS}			0.01			0.01		dB/V

AC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	KT3040			KT3040A			Unit
			Min	Typ	Max	Min	Typ	Max	
Crosstalk, Transmit to Receive $20 \log \frac{V_{FRO}}{V_{FXO}}$	CT_{XR}	Transmit filter output $=2.2V_{rms}$, $V_{FRI}=0V_{rms}$, $f=0.3KHz$ to $3.4KHz$ measure V_{FRO}			−70			−70	dB
Gain Tracking Relative to G_{AR}	G_{RRL}	Output level = +3dBmO +2dBmO to −40dBmO −40dBmO to −55dBmO (Note 5)	−0.1 −0.05 −0.1		0.1 0.05 0.1	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB
RECEIVE OUTPUT POWER AMPLIFIER									
Input Leakage Current, PWRI	I_{BP}	$-3.2V \leq V_{IN} \leq 3.2V$	0.1		3	0.1		3	μA
Input Resistance, PWRI	R_{IP}		10			10			MΩ
Output Resistance, PWRO+, PWRO−	R_{OP1}	Amplifier Active		1			1		Ω
Load Capacitance, PWRO+, PWRO−	C_{LP}				500			500	pF
Gain, PWRI to PWRO+ Gain, PWRI to PWRO−	G_{AP+} G_{AP-}	$R_L=600Ω$ connected between PWRO+ and PWRO−, input Level = 0dBm0 (Note 4)		1 −1			1 −1		V/V V/V
Gain Tracking Relative to 0dBm0 Output Level. Including Receive Filter	G_{RPL}	$V=2.05V_{rms}$, $R_L=600Ω$ (Note 4, 5) $V=1.75V_{rms}$, $R_L=300Ω$	−0.1 −0.1		0.1 0.1	−0.1 −0.1		0.1 0.1	dB
Signal/Distortion	S/D_P	$V=2.05V_{rms}$, $R_L=600Ω$ $V=1.75V_{rms}$, $R_L=300Ω$ (Note 4, 5)			−45 −45			−45 −45	dB dB
Output DC Offset PWRO+, PWRO−	V_{OSP}	PWRI connected to GNDA	−50		50	−50		50	mV
Power Supply Rejection Ratio of V_{CC} or V_{BB}	PSRR5	PWRI connected to GNDA	45			45			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power Amplifier. This specification listed assumes $0dB_m$ is delivered to 600Ω connected from PWRO+ to PWRO−.

Note 2: Voltage input to receive filter at 0V. V_{FRO} connected to PWRI, 600Ω from PWRO+ to PWRO−. Output measured from PWRO+ to PWRO−.

Note 3: The 0dBm0 level for the filter is assumed to be $1.54V_{rms}$ measured at the output of the XMT or RCV filter.

Note 4: The 0dBm0 level for the power amplifiers is load dependent. For $R_L=600Ω$ to GNDA, the 0dBm0 level is $1.43V_{rms}$ measured at the amplifier output for $R_L=300Ω$ the 0dBm0 level is $1.22V_{rms}$.

Note 5: V_{FRO} connected to PWRI, input signal applied to V_{FRI}.

PIN DESCRIPTION

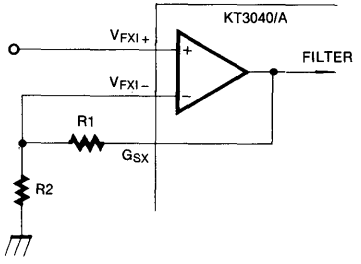
Pin No.	Designation	Function
1	V_{FXI+}	The non-inverting input of the gain adjustment OP amp in the transmit filter. The signal applied to this pin typically comes from the 2 to 4 wire hybrid in the case of a 2 wire line and goes through the frequency rejection and antialiasing filters before being sent to the CODEC for encoding.
2	V_{FXI-}	Inverting input of the gain adjustment operational amplifier on the transmit filter.
3	G_{SX}	Output of the gain adjustment operational amplifier on the transmit filter. Used for gain setting of the transmit filter.
4	V_{FRO}	Analog output of the receive filter. This output is capable of driving high impedance electronic hybrids. The gain of the receive signal may be attenuated by using a resister divider. For a transformer hybrid application, V_{FRO} is tied to PWRI and a dual balanced output is provided on pins PWRO+ and PWRO−.
5	PWRI	Input to the power driver amplifiers on the receive side for interface to transformer hybrids. High impedance input. When tied to V_{BB}, the power amplifiers are powered down.
6	PWRO+	Non-inverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
7	PWRO−	Inverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
8	V_{BB}	The negative power supply pin. The recommended input is −5V.
9	V_{CC}	The positive power supply pin. The recommended input is 5V.
10	V_{FRI}	Analog input of the receive filter, interface to the CODEC analog output for PCM applications. The receive filter provides the sinx/x correction needed for sample and hold types CODEC outputs to give unity gain.
11	GNDD	Digital ground return for internal clock generator.
12	CLK	The master clock input. Three clock frequencies can be used: 1.536MHz, 1.544MHz or 2.048MHz. For proper operation this clock should be tied to the receive clock of the CODEC.
13	PDN	Control input for the stand-by power down mode. Power down occurs when the signal on this input is pulled high. An internal pull up to the positive supply is provided.
14	CLK0	Master clock (pin 12, CLK) frequency selection. If tied to V_{BB}, CLK should be 1.536MHz. If tied to GNDD, CLK should be 1.544MHz. If tied to V_{SS}, CLK should be 2.048MHz. An internal pull up is provided.
15	GNDA	Analog return common to the transmit and receive analog circuits. Not internally connected to GNDD.
16	V_{FXO}	The analog output of the transmit filter. The output voltage range is ±3.2V.

FUNCTIONAL DESCRIPTION

The KT3040/A provides the transmit and receive filters found on the analog termination of a PCM line or trunk. The transmit filter performs the anti-aliasing function needed for an 8KHz sampling system, and the 50/60Hz rejection. The receive filter has a low pass transfer characteristic and also provides the sinx/x correction necessary to interface μ-Law and A-Law CODECs which have a non-return-to zero output of the digital to analog conversion. Gain adjustment is provided in the receive and transmit directions. The KT3040/A can interface directly with a transformer hybrid (2 to 4 wire conversion) or with electronic hybrids.

Transmit Filter

The input stage provides gain adjustment in the passband. The CMOS operational amplifier has a common mode range of ±2.5V, a DC offset of less than ±20mV, a voltage gain greater than 5,000 and a unity gain bandwidth of 2MHz. The load impedance connected to the amplifier output (G_{SX}) must be greater than 10KΩ in parallel with 25pF. The input operational amplifier can also be used in the inverting mode of differential amplifier mode. It can be connected to provide a gain of 20dB without degrading the overall filter performance.



$R1 + R2 \geq 10K\Omega$

Input OP Amp Gain $= \frac{R1 + R2}{R2}$

Tx Voltage Gain $= \frac{R1 + R2}{R2} \times \sqrt{2}$

(The Tx filter itself introduces, a 3dB gain)

The Tx input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched capacitor band pass filter. A band pass filter provides rejection of 200Hz or lower noise which may exist in the signal path, and stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

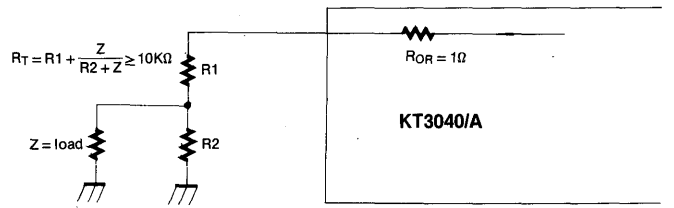
The output stage of the transmit filter, the post filter is also a two pole RC active low pass filter which attenuate clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a $\pm 3.2V_{p\text{-}p}$ signal into a 10KΩ load in parallel with up to 25pF.

Receive Filter

The Rx input stage is a prefilter which is similar to the Tx prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter provides stopband rejection, sinx/x gain correction and passband flatness.

The receive filter output V_{FRO} lead is capable of driving high impedance electronic hybrids. The gain of the receive section from V_{FRI} to V_{FRO} is $(\pi f/8000)/\text{Sin}\ (\pi f/8000)$.

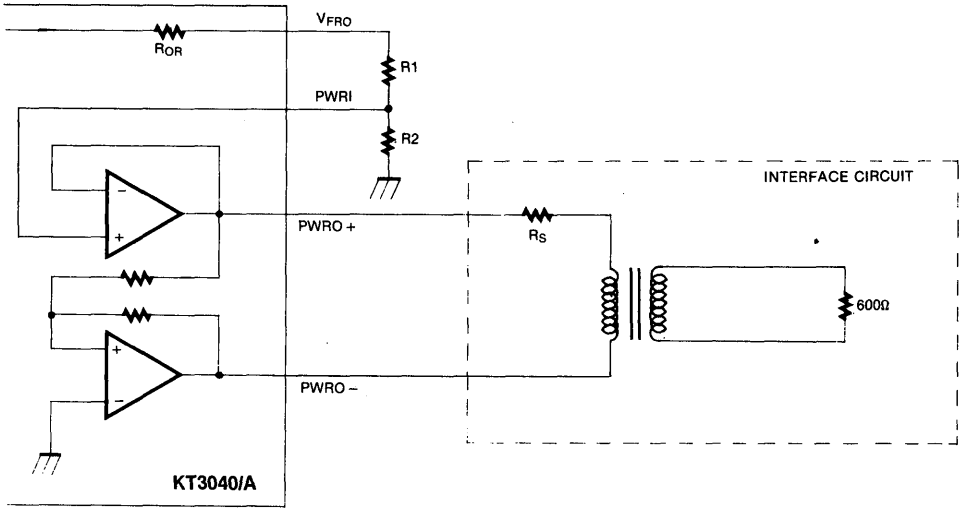
The filter gain can be adjusted downward by a resistor voltage divider as shown below. The total load impedance R_T connected to the filter output (V_{FRO}) must be greater than 10KΩ.



Receive Filter Output Gain Adjustment

Receive Filter Power Amplifier

A balanced power amplifier is provided in order to transformer coupled line circuits. The receive filter output V_{FRO} is connected through gain setting resistors R1 and R2 to the amplifier input PWRI. The input voltage range on PWRI is ±3.2V. The series combination of R_S and the hybrid transformer must present a minimum AC load resistance of 600Ω to the amplifier in the bridge configuration. A typical connection of the output driver amplifier is shown below.



Typical Connection of Output Driver Amp

The power amps can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

Power Down Mode

Pin 13 (PDN) provides the power down control. When the level on this pin is high, the KT3040/A goes into standby, power down mode. The total filter power consumption will reduce to less than 1mW. This feature allows multiple KT3040/A to drive the same analog bus on a time shared basis. Connect PDN to GNDD for normal operation.

APPLICATION INFORMATION

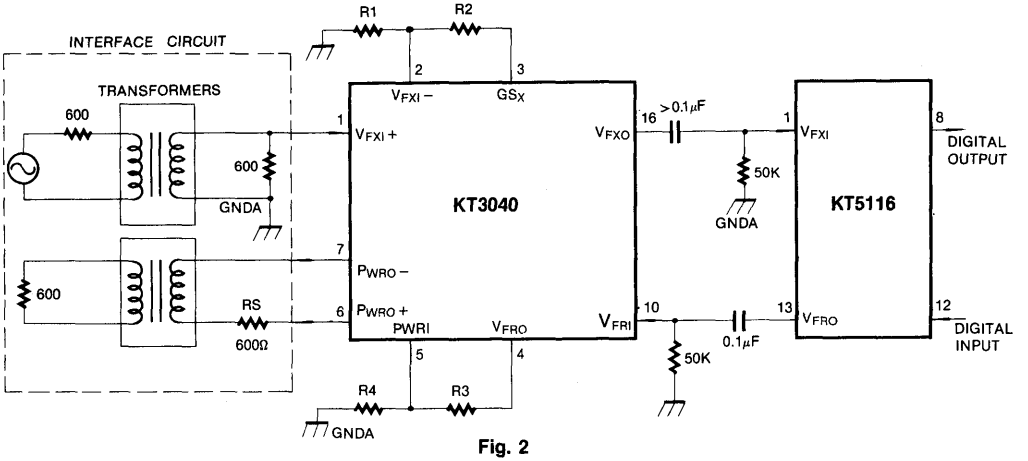


Fig. 2

Note 1: Transmit voltage gain $= \frac{R_1 + R_2}{R_2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain), $(R_1 + R_2 \geq 10K)$

Note 2: Receive Gain $= \frac{R_4}{R_3 + R_4}$ $(R_3 + R_4 \geq 10K)$

Note 3: In the configuration shown, the receive filter amplifiers will drive a 600Ω T to R termination to a maximum signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω lesistor, R_S, will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

Gain Adjust

Fig. 2 shows the signal path interconnections between the KT3040 and KT5116 single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the KT3040 filter when operated with system peak overload voltages of ±2.5 to ±3.2V at V_{FXO} and V_{FRO}. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the KT3040 filter can be used with the KT3000 series CODEC which has a 5.5V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

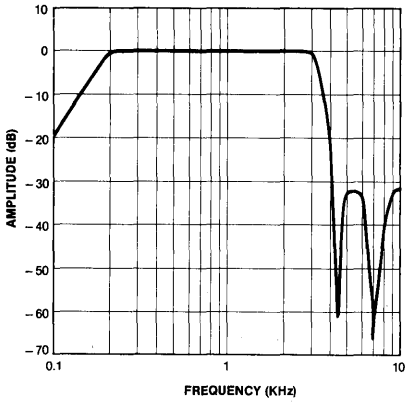
Decoupling Recommendations

PC board decoupling should be sufficient to prevent power supply transients from exceeding the absolute maximum rating of the device. A minimum of 1μF is recommended for each power supply.

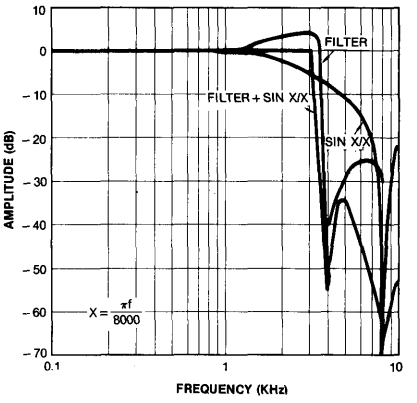
A 0.05μF bypassing capacitor should also be connected from each power supply to GNDA. However, this decoupling may be reduced depending on board design and performance. Ground loops should be avoided.

TYPICAL PERFORMANCE CURVE

TRANSMIT FILTER STAGE

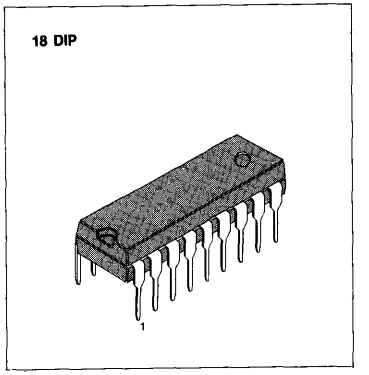


RECEIVE FILTER STAGE



LOW POWER DTMF RECEIVER

The KT3170 is a complete Dual Tone Multiple Frequency (DTMF) receiver which is fabricated by the low power CMOS and the Switched-Capacitor Filter technology. This LSI consists of band split filters, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus. It decodes all 16 DTMF tone pairs into a 4bits digital code.
The externally required components are minimized by on chip provision of a differential input AMP, clock oscillator and latched three state interface. The on chip clock generator requires only a low cost TV crystal as an external component.



FEATURES

- **Detects all 16 standard tones.**
- **Low power consumption: 15mW (Typ)**
- **Single power supply: 5V**
- **Uses inexpensive 3.58MHz crystal**
- **Three state outputs for microprocessor interface**
- **Good quality and performance for using in exchange system**
- **Package options include standard plastic and ceramic 300 mil DIPs**
- **Power down mode/input inhibit**

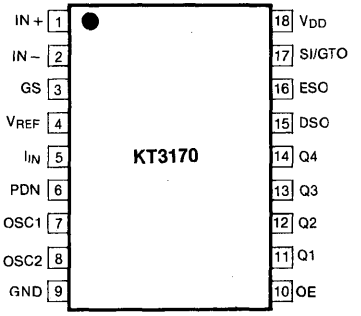
ORDERING INFORMATION

Device	Package	Operating Temperature
KT3170N	Plastic	−40 ~ +85°C
KT3170J	Ceramic	

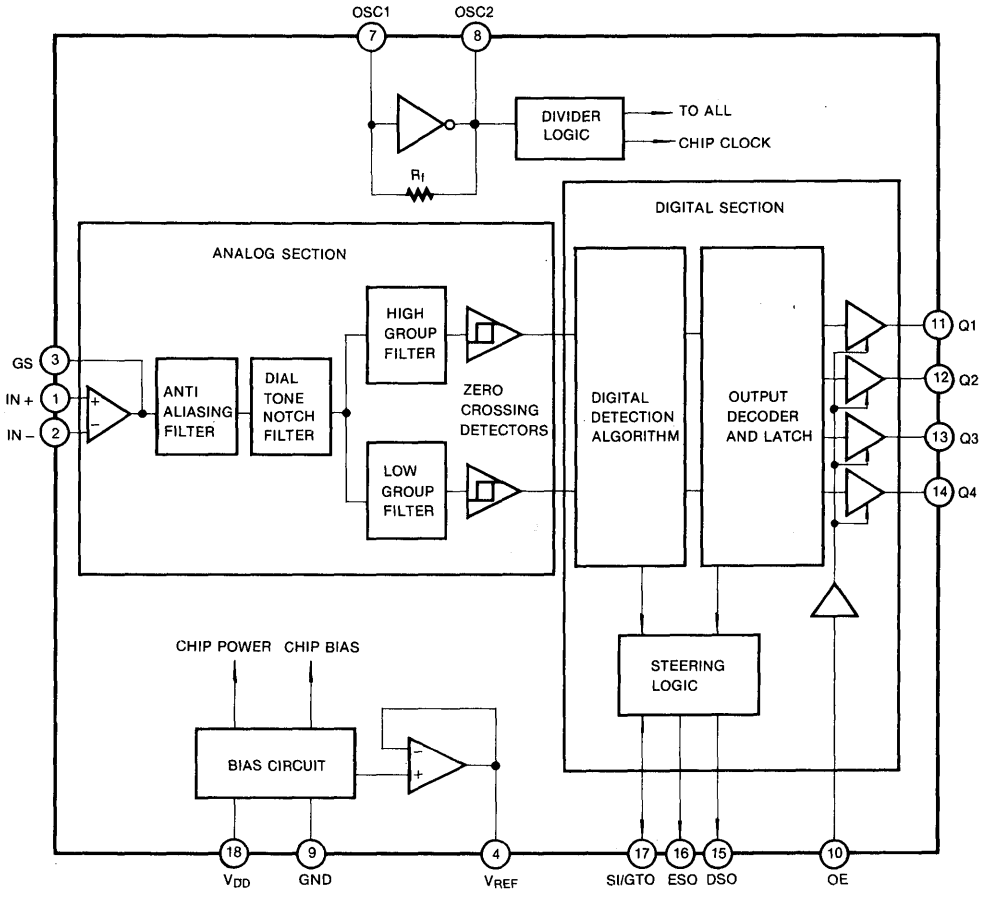
APPLICATIONS

- PABX
- Central Office
- Paging Systems
- Remote Control
- Credit Card Systems
- Key Phone System
- Answering Phone
- Home Automation System
- Mobile Radio
- Remote Data Entry

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	6	V
Analog Input Voltage Range	V_{INA}	$-0.3 \sim V_{DD}+0.3$	V
Digital Input Voltage Range	V_{IND}	$-0.3 \sim V_{DD}+0.3$	V
Output Voltage Range	V_O	$-0.3 \sim V_{DD}+0.3$	V
Current On Any Pin	I_{IN}	10	mA
Operating Temperature	T_a	$-40 \sim +85$	°C
Storage Temperature	T_{stg}	$-60 \sim +150$	°C

*Absolute Maximum Ratings are these value beyond which permanent damage to the device may occur. These are stress rating only and functional operation of the device at or beyond them is not implied. Long exposure to these condition may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, Ta = 25°C, unless otherwise noted)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage	V_{DD}		4.75		5.25	V
Operating Supply Current	I_{DD}			3.0	9.0	mA
Power Dissipation	P_D			15	45	mW
Input Voltage Low	V_{IL}				1.5	V
Input Voltage High	V_{IH}		3.5			V
Input Leakage Current	I_{IH}/I_{IL}	V_{IN} = GND or V_{DD}		0.1		μA
Pull Up Current On OE Pin	I_{PU}	OE = GND		7.5	15	μA
Analog Input Impedance	R_{IN}	f_{IN} = 1KHz	8	10		MΩ
Steering Input Threshold Voltage	V_{TS}		2.2		2.5	V
Output Voltage Low	V_{OL}	No Load			0.03	V
Output Voltage High	V_{OH}	No Load	4.97			V
Output Current	I_{sink}	V_{OL} = 0.4V	1	2.5		mA
Output Current	I_{source}	V_{OH} = 4.6V	0.4	0.8		mA
V_{ref} Output Voltage	V_{ref}		2.4		2.8	V
V_{ref} Output Resistance	R_{ref}			10		KΩ
Analog Input Offset Voltage	V_{OS}			25		mW
Power Supply Rejection Ratio	PSRR	Gain Setting Amp at 1KHz		60		dB
Common Mode Rejection Ratio	CMRR	$-3.0V < V_{IN} < 3.0V$		60		dB
Open Loop Voltage Gain	A_V	Gain Setting Amp at 1KHz		65		dB
Open Loop Unit Gain Bandwidth	BW			1.5		MHz
Analog Output Voltage Swing	V_{AO}	R_L = 100K		4.5		V_{p-p}
Acceptable Capacitive Load	C_L	GS		100		pF
Acceptable Resistive Load	R_L	GS		50		KΩ
Analog Input Common Mode Voltage Range	V_{CM}	No Load		3.0		V_{p-p}

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, Ta = 25°C, f_C = 3.579545MHz)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Valid Input Signal Range (each tone of composite signal)	V_{INA}		− 29		1.0	dBm
Dual Tone Twist Accept	TW			± 10		dB
Acceptable Frequency Deviation	FDA				± 1.5% ± 2Hz	
Frequency Deviation Reject	FDR		± 3.5%			
Third Tone Tolerance	T3		− 25	− 16		dB
Noise Tolerance	NT			− 12		dB
Dial Tone Tolerance	DT		18	22		dB
Crystal Clock Frequency	f_c		3.5759	3.5795	3.5831	MHz
Maximum Clock Input Rise Time	t_r	External Clock			110	nS
Maximum Clock Input Fall Time	t_f	External Clock			110	nS
Acceptable Clock Input Duty Cycle	DC	External Clock	40	50	60	%
Acceptable Capacitive Load	CLO	OSC2 PIN			30	pF
Tone Present Detect Time	TDP		5	11	14	mS
Tone Absent Detect Time	TDA		0.5	4	8.5	mS
Minimum Tone Duration Accept	TUA	User Adjustable			40	mS
Maximum Tone Duration Reject	TUR	User Adjustable	20			mS
Acceptable Interdigit Pause	TAID	User Adjustable			40	mS
Rejectable Interdigit Pause	TRID	User Adjustable	20			mS
Propagation Delay Time SI to Q	TPSQ	OE = High		8	11	μS
Propagation Delay Time SI to DSO	T_{psds}	OE = High		12		μS
Output Data Setup Q to DSO	TSU	OE = High		3.4		μS
Propagation Delay Time OE to Q (Enable)	TPEQ	R_L = 10K, C_L = 50pF		50	60	nS
Propagation Delay Time OE to Q (Disable)	TPDQ	R_L = 10K, C_L = 50pF		300		nS

Notes:
1. Digit sequence consists of all 16 DTMF tones.
2. Tone duration = 40mS, Tone pause = 40mS.
3. Nominal DTMF frequencies are used.
4. Both tones in the composite signal have an equal amplitude.
5. Tone pair is deviated by ± 1.5% ± 2Hz.
6. Bandwidth limited (3KHz) Gaussian Noise.
7. The precise dial tone frequencies are (350Hz and 440Hz) ± 2%.
8. For an error rate of better than 1 in 10000.
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. This item also applies to a third tone injected onto the power supply.
12. Referenced to Fig. 1 Input DTMF tone level at − 28dBm.

PIN DESCRIPTION

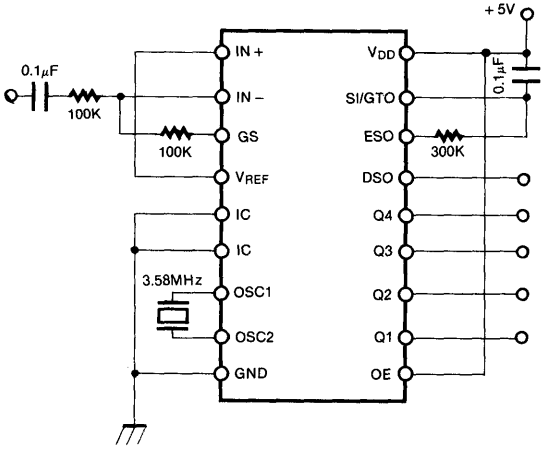
Pin	Name	Description
1	IN +	Non inverting Input of the op amp.
2	IN −	Inverting Input of the op amp.
3	GS	Gain Select. The output used for gain adjustment of analog input signal with a feedback resistor.
4	V_{ref}	Reference Voltage output (V_{DD}/2, Typ) can be used to bias the op amp input of V_{DD}/2.
5	I_{IN}	Input inhibit. High input states inhibits the detection of tones. This pin is pulled down internally.
6	P_{DN}	Control input for the stand-by power down mode. Power down occurs when the signal on this input is high states. This pin is pulled down internally.
7, 8	OSC1 OSC2	Clock input/output. A inexpensive 3.579545MHz crystal connected between these pins completes internal oscillator. Also, external clock can be used.
9	GND	Ground pin.
10	OE	Output Enable input. Outputs Q1-Q4 are CMOS push pull when OE is High and open circuited (High impedence) when disabled by pulling OE low. Internal pull up resistor built in.
11-14	Q1-Q4	Three state data output. When enabled by OE, these digital outputs provide the hexadecimal code corresponding to the last valid tone pair received.
15	DSO	Delayed Steering Output. Indicates that valid frequencies have been present for the required guard time, thus constituting a valid signal. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on SI/GTO falls below V_{TS}.
16	ESO	Early Steering Outputs. Indicates detection of valid tone outputs a logic high immediately when the digital algorithm detects a recognizable tone pair. Any momentary loss of signal condition will cause ESO to return to low.
17	SI/GTO	Steering Input/Guard Time Output. A voltage greater than V_{TS} detected at SI causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TS} frees the device to accept a new tone pair. The GTO output acts to reset the external steering time constant, and its state is a function of ESO and the voltage on SI.
18	V_{DD}	Power Supply (+5V, Typ)

APPLICATION INFORMATION

The KT3170 is complete Touch-Tone detection system. It combines high precision active filter with analog circuits and digital control logic on a monolithic CMOS chip. This application information describes device operation of each block, performance and typically application circuit.

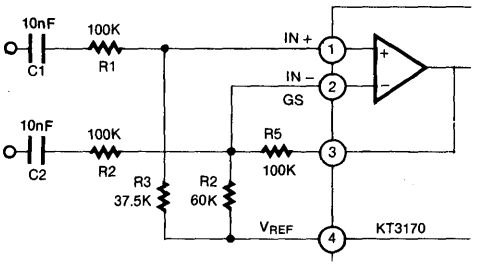
ANALOG INPUT CONFIGURATION

The KT3170 is designed to accept sinusoidal input waveforms but will operate satisfactorily with any input that has the correct fundamental frequency. The input arrangement provides a differential input op amp, bias source (reference voltage V_{REF}) which is used to bias the inputs at mid-rail. Connection of a feedback resistor to the op amp output (GS) makes gain of op amp adjust. The signal level at the input must be operated in power supply range on the data sheet. In a single ended configuration, the input pins are connected as shown in application circuit with unity gain and V_{REF} biasing. In a differential ended configuration the input pins are connected as shown in Fig. 2 with voltage gain (R5/R1).



All resistors are 1% tolerance
All capacitors are 5% tolerance

Fig. 1 Single Ended Input Configuration



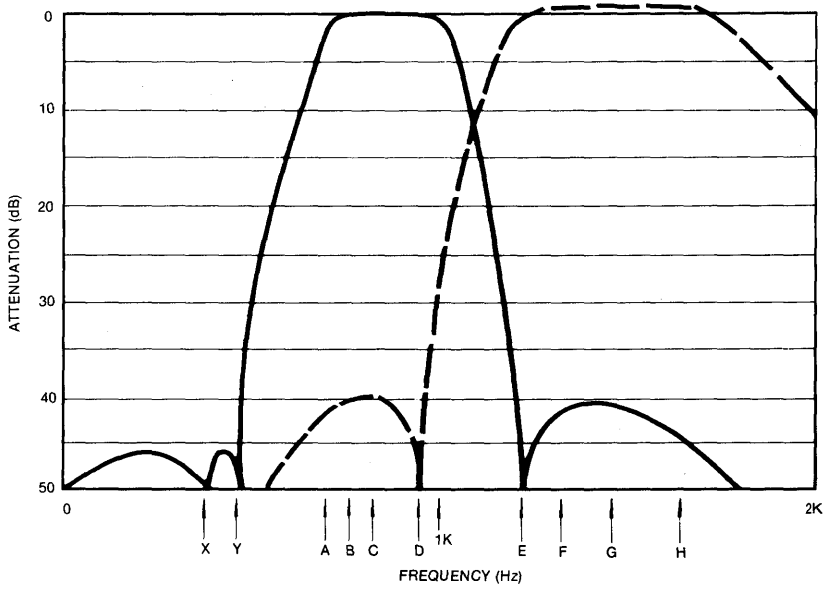
R3 = R2R5/(R2 + R5), VOLTAGE GAIN = R5/R1
INPUT IMPEDANCE: $2\sqrt{R_1^2 + (1/wC)^2}$

All resistors are 1% tolerance
All capacitors are 5% tolerance

Fig. 2 Differential Ended Input Configuration

FILTER SECTION

After analog signal is passed op amp, separation of the low group and high group tones is achieved by applying the DTMF signal to the inputs of two 9th-order switched capacitor band pass filter, the bandwidths of which correspond to the low and high group frequencies. The band split filters are actually rejecting all frequencies except the 16 DTMF tone pairs. The filter section also incorporates notches at 350 and 440Hz for exceptional dial tone rejection as shown below. Each filter output is followed by a single order switched capacitor section which smoothes the signals prior to limiting. Limiting is performed by high-gain comparator which are provided with hysteresis to prevent detection of unwanted low level signals. The outputs of teh comparators provide full-rail logics swing at the frequencies of the incoming DTMF signals.



PRECISE DIAL TONES
X = 350Hz
Y = 440Hz

DTMF TONES

A = 697Hz	E = 1209Hz
B = 770Hz	F = 1336Hz
C = 852Hz	G = 1477Hz
D = 941Hz	H = 1633Hz

Fig. 3 Typical Filter Characteristics

DECODER SECTION

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations.

The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (ESO). Any loss of signal condition will cause ESO to fall.

OSCILLATOR SECTION

The KT3170 contains an on chip inverter with sufficient gain a feedback resistor Rf to provide oscillation when connected to a low cost television "color-burst" crystal. The oscillator circuit is connected as shown in application circuit. It is possible to operate several KT3170 devices employing only a single crystal oscillator. The oscillator output of the first devices in the chain is coupled through a 30pF capacitor to the oscillator input (OSC1) of the next device, subsequent devices are connected in a simuliar fashion as shown Fig. 4. The problems for unbalanced loading are not a concern with the arrangement shown, i.e., balancing capacitors are not required.

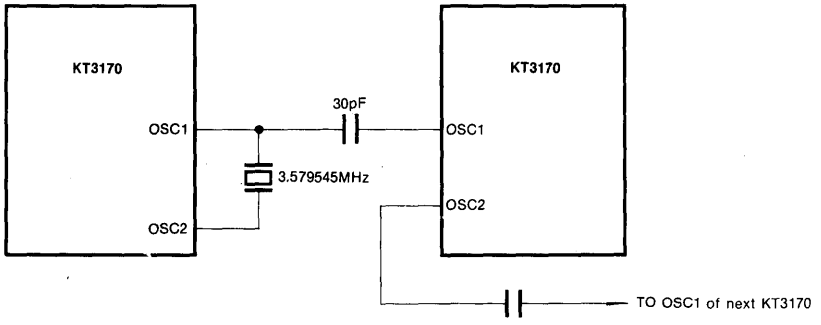


Fig. 4 Oscillator Connection

STEERING CIRCUIT

Before registration of a decoded tone pair, the receiver checks for a valid signal duration. This check is performed by an external RC time constant driven by ESO. A logic high on ESO causes V_C (see Fig. 5) to rise as the capacitor discharges. Providing signal condition is maintained (ESO remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TST}) of the steering logic to register the tone pair, thus latching its corresponding 4bits code (see Table 1) into the output latch. At this point, the GTO output is activated and drives V_C to V_{DD}. GTO continues to drive high as long as ESO remains high, finally after a short delay to allow the output latch to settle, the "delayed steering" output flag (STO) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (OE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruption (drop outs) too short to be considered a valid pause. This capability, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

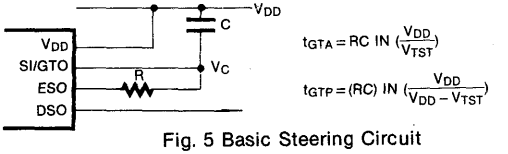


Fig. 5 Basic Steering Circuit

DIGITAL OUTPUT

Outputs Q1-Q4 are CMOS push pull when enabled (EO = High) and open circuited (high impedance) when disabled by pulling EO = Low. These digital outputs provide the hexadecimal code corresponding to the DTMF signals. The table below describes the hexadecimal.

NO	LOW FREQUENCY	HIGH FREQUENCY	OE	Q4	Q3	Q2	Q1
1	697	1209	H	0	0	0	1
2	697	1336	H	0	0	1	0
3	697	1477	H	0	0	1	1
4	770	1209	H	0	1	0	0
5	770	1336	H	0	1	0	1
6	770	1477	H	0	1	1	0
7	852	1209	H	0	1	1	1
8	852	1336	H	1	0	0	0
9	852	1477	H	1	0	0	1
0	941	1336	H	1	0	1	0
*	941	1209	H	1	0	1	1
#	941	1477	H	1	1	0	0
A	697	1633	H	1	1	0	1
B	770	1633	H	1	1	1	0
C	852	1633	H	1	1	1	1
D	941	1633	H	0	0	0	0
ANY	—	—	L	Z	Z	Z	Z

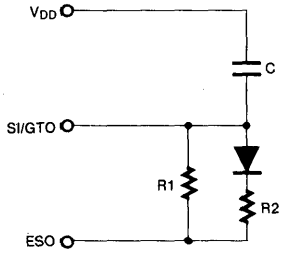
Z: High Impedance
H: High Logic Level
L: Low Logic Level

GUARD TIME ADJUSTMENT

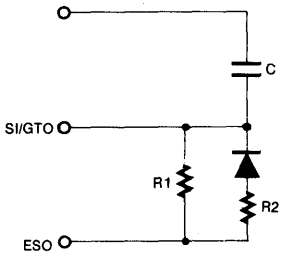
In a situations which do not require independent selection of receive and pause, the simple steering of Fig. 5 is applicable. Component values are chosen according to the following formula:

$t_{REC} = t_{DP} + t_{GTP}$, $t_{GTP} = 0.63RC$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1μF is recommended for most application, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 miliseconds would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication application are satisfied with this circuits. Different steering arrangements may be used to select independently the guard times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications which place both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameter such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustments is shown in Figure 6.



$t_{GTP} = (R1C)\ln(V_{DD}/V_{DD} - V_{TST})$
$t_{GTA} = (RpC)\ln(V_{DD}/V_{TST})$
$Rp = R1R2/(R1 + R2)$
(a) Decreasing t_{GTA}($t_{GTP} > t_{GTA}$)



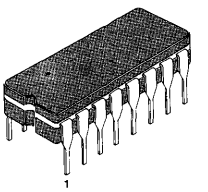
$t_{GTP} = (RpC)\ln(V_{DD}/V_{DD} - V_{TST})$
$t_{GTA} = (R1C)\ln(V_{DD}/V_{TST})$
$Rp = R1R2/(R1 + R2)$
(a) Decreasing t_{GTP}($t_{GTP} < t_{GTA}$)

Figure 6. Guard Time Adjustment

μ-LAW COMPANDING CODEC

The KT5116 is a monolithic CMOS companding CODEC which contains two parts: (1) an analog-to-digital converter (2) a digital to-analog converter which have transfer characteristics conforming to the μ-Law companding code.
These two parts form a coder-decoder function designed to meet the needs of the telecommunications industry for per-channel voice-frequency codes used in telephone digital switching and transmission systems.
Digital input and output are in serial format using sign-plus-amplitude coding.
A sync pulse input is provided for reception of multichannel information being multiplexed and synchronizing transmission over a single transmission line.
Practical transmission and reception of 8bit data words which contain the analog information is done from 64Kb/s to 2.1Mb/s rate with analog signal sampling occuring at an 8KHz rate.

16 CERDIP



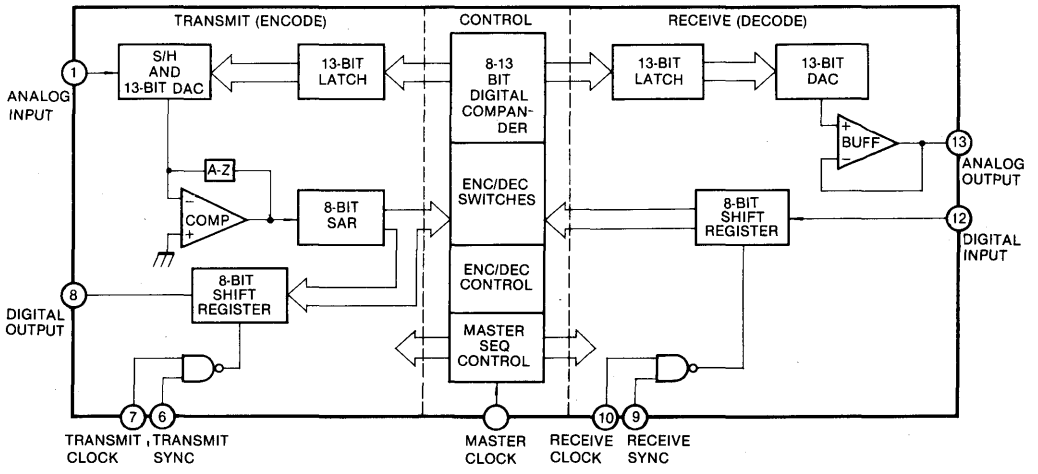
FEATURES

- **The simple ±5V power supply operation**
- **Typically 30mW low power dissipation**
- **Follows the μ-255 companding law**
- **Synchronous and asynchronous operation**
- **On-chip offset null circuit eliminates long term drift, drift error and need for trimming**
- **Minimum external circuitry required**
- **Separate analog and digital grounding pins reduce system noise problems**
- **On-chip sample and hold.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KT5116N	Plastic	0 ~ 70°C
KT5116J	Ceramic	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
DC Power Supply	V+ (V−)	+6 (−6)	V
Ambient Operating Temperature	T_a	0 to 70	°C
Storage Temperature	T_s	−55 to 125	°C
Package Dissipation at 25°C	P_D	500	mW
Digital Input Voltage	V_{DI}	−0.5 to 6	V
Analog Input Voltage	V_{AI}	−6 to 6	V
Positive Reference Voltage	V_{ref+}	−0.5 to 6	V
Negative Reference Voltage	V_{ref-}	−6 to 0.5	V

DIGITAL OUTPUT CODE μ-LAW

No	Chord Code	Chord Value	Step Value
1	0 0 0	0.0mV	0.613mV
2	0 0 1	10.11mV	1.226mV
3	0 1 0	30.3mV	2.45mV
4	0 1 1	70.8mV	4.90mV
5	1 0 0	151.7mV	9.81mV
6	1 0 1	313mV	19.61mV
7	1 1 0	637mV	39.2mV
8	1 1 1	1284mV	78.4mV

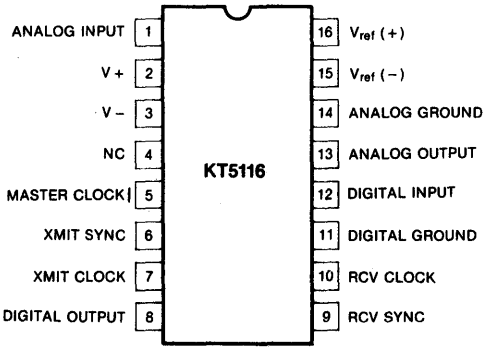
EXAMPLE;

1 0 1 1 0 0 1 0 = +70.8mV+ (2×4.90mV)

sign bit chord step bit = 80.6mV

If the sign bit were a zero, then both plus signs would be changed to minus signs

PIN CONFIGURATION



DC CHARACTERISTICS

(Condition; $V^+ = 5V$, $V^- = -5V$, $V_{ref+} = 2.5V$, $V_{ref-} = -2.5V$)

Parameter	Symbol	Min	Typ	Max	Unit
Analog Input Resistance During Sampling	R_{INAS}		2		KΩ
Analog Input Resistance Non-Sampling	R_{INANS}		100		MΩ
Analog Input Capacitance	C_{INA}		150	250	pF
Analog Input Offset Voltage	V_{offINA}		±1	±8	mV
Analog Output Resistance	R_{OUTA}		1	10	Ω
Analog Output Current	$I_{out/A}$	0.25	0.5		mA
Analog Output Offset Voltage	$V_{off/O}$		±20	±850	mV
Logic Input Low Current ($V_{IN} = 0.8V$) Digital Input, Clock Input, SYNC Input	I_{IL}		±0.1	±10	μA
Logic Input High Current ($V_{IN} = 2.4V$)	I_{IH}		−0.25	−0.8	mA
Digital Output Capacitance	$C_{D/O}$		8	12	pF
Digital Output Leakage Current	I_{DOL}		±0.1	±10	μA
Digital Output Low Voltage	V_{OL}			0.4	V
Digital Output High Voltage	V_{OH}	3.9			V
Positive Supply Current	I^+		4	10	mA
Negative Supply Current	I^-		2	6	mA
Positive Reference Current	I_{ref+}		4	20	μA
Negative Reference Current	I_{ref-}		4	20	μA

AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency	f_m	1.5	1.544	2.1	MHz
RCV, XMIT Clock Frequency	f_r, f_x	0.064	1.544	2.1	MHz
Clock Pulse Width (MASTER, XMIT, RCV)	PW_{CLK}	200			ns
Clock Rise, Fall Time (MASTER, XMIT, RCV)	t_{rc}, t_{fc}			25% of PW_{CLK}	ns
SYNC Rise, Fall Time (XMIT, RCV)	t_{rs}, t_{fs}			25% of PW_{CLK}	ns
SYNC Pulse Width (XMIT, RCV)			$\frac{8}{fx\ (fr)}$		μs
Data Input Rise, Fall Time	t_{DIR}, t_{DIF}			25% of PW_{CLK}	ns
SYNC Pulse Period (XMIT, RCV)	t_{ps}		125		μs
XMIT Clock-to-XMIT SYNC Delay	t_{xcs}	50% of t_{fc} (t_{rs})			ns
XMIT Clock-to-XMIT SYNC (Negative Edge) Delay	t_{xcsn}	200			ns
XMIT SYNC Set-Up Time	t_{xss}	200			ns
XMIT Data Delay	t_{xdd}	0		200	ns
XMIT Data Present	t_{xdp}	0		200	ns
XMIT Data Three State	t_{xdt}			150	ns
Digital Output Fall Time	t_{dof}		50	100	ns
Digital Output Rise Time	t_{dor}		50	100	ns
RCV SYNC-to-RCV Clock Delay	t_{src}	50% t_{rc} (t_{fs})			ns
RCV Data Set-Up Time	t_{rds}	50			ns
RCV Data Hold Time	t_{rdh}	200			ns
RCV Clock-to-RCV SYNC Delay	t_{rcs}	200			ns
RCV SYNC Set-Up Time	t_{rss}	200			ns
RCV SYNC-to-Analog Output Delay	t_{sao}		7		μs
Analog Output Positive Slew Rate	Slew +		1		V/μs
Analog Output Negative Slew Rate	Slew −		1		V/μs
Analog Output Drop Rate	Droop		25		μV/μs

POWER SUPPLY REQUIREMENTS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	$V+$	4.75	5.0	5.25	V
Negative Supply Voltage	$V-$	−5.25	−5.0	−4.75	V
Positive Reference Voltage	V_{ref}^{+}	2.375	2.5	2.625	V
Negative Reference Voltage	V_{ref}^{-}	−2.625	−2.5	−2.375	V

SYSTEM CHARACTERISTICS

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Signal-to-Distortion	Analog Input: 0 ~ −30dBm0	S/D	35	39		dB
	Analog Input: −40dBm0		29	34		dB
	Analog Input: −45dBm0		24	29		dB
Gain Tracking	Analog Input: +3 ~ −37dBm0	GT		±0.1	±0.4	dB
	Analog Input: −37 ~ −50dBm0			±0.1	±0.8	dB
	Analog Input: −50 ~ −55dBm0			±0.2	±2.5	dB
Idle Channel Noise	Analog Input = 0V	N_{IC}		10	18	dBrnc0
Transmission Level Point	600Ω	T_{LP}		+4		dB

PIN DESCRIPTION

1. Analog Input (Pin 1)

At this pin, employs voice-frequency analog signals which are bandwidth-limited to 4KHz. Then, they are sampled at an 8KHz rate. The Analog Input must remain between V_{ref} (+) and V_{ref} (−) for accurate conversion.

2. Positive Supply Voltage and Negative Supply Voltage (Pin 2, 3)

Pin 2, 3 is a pin which employs supply voltage. Typically, the voltages of these pins are ±5V.

3. NC (Pin 4)

This pin is a pin of non-connection.

4. Master Clock (Pin 5)

This signal provides the basic timing and control signals required for all internal conversions. It is not necessary for synchronizing with RCV SYNC, RCV Clock, XMIT SYNC or XMIT Clock. It is not internally related to them.

5. XMIT SYNC (Pin 6)

This input is synchronized with XMIT Clock. If XMIT SYNC goes High, the Digital Output is activated and the A/D conversion begins on the next positive edge of Master Clock. Otherwise, if XMIT SYNC goes Low, the Digital Output become 3 state. XMIT SYNC must go Low for at least 1 Master Clock prior to the transmission of the next digital word.

6. XMIT Clock (Pin 7)

The on-chip 8-bit output shift register of the KT5116 is unloaded at the clock rate present on this pin. Clock rates of 64KHz to 2.1MHz can be used for XMIT Clock. When the positive edge of XMIT SYNC occurs after the positive edge of XMIT Clock, XMIT SYNC will determine when the first positive edge of the internal clock will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

7. Digital Output (Pin 8)

The Digital Output is composed of a sign bit, 3 chord bits and 4 step bits. The sign bit indicates the polarity of the Analog Input while the chord and step bits indicate the magnitude. The KT5116 output register stores the 8 bit encoded sample of the Analog Input. The 8 bit-word is shifted out under control of XMIT SYNC and XMIT CLOCK. If XMIT SYNC is Low, the Digital Output is an open circuit, otherwise when XMIT SYNC is High, the state of the Digital Output is determined by the value of the output bit in the serial shift register.

8. RCV SYNC (Pin 9): Refer to Figure 3

This input is synchronized with RCV CLOCK, and serial data is clocked in by RCV CLOCK. Duration of the RCV pulse is approximately eight RCV Clock periods. The conversion from digital to analog starts after the negative edge of RCV SYNC pulse (see Fig. 6). The negative edge of RCV SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV SYNC must stay low for 17 Master Clocks (minimum) before the digital word is to be received (see Fig. 11).

9. RCV Clock (Pin 10): Refer to Figure 3

Valid data should be applied to the digital input before the positive edge of the internal clock. (refer to Fig. 3) This SYNC pulse is approximately eight RCV CLOCK periods. The conversion from digital to analog starts after the negative the internal clock transfers the data to the slave of the master-slave flip-flop. A hold time, t_{rdh}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV occurs after the first rising edge of RCV CLOCK, RCV SYNC will determine when the first positive edge of internal clock will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

10. Digital Ground (Pin 11)

11. Digital Input (Pin 12)

The KT5116 input register accepts the 8-bit sample of an analog value and loads it under control of RCV SYNC and RCV CLOCK (refer to Figure 3). When RCV SYNC goes High, the KT5116 uses RCV CLOCK to clock to clock the serial data into its input register RCV SYNC goes Low to indicate the end of serial input data. The eight bits of the input data have the same functions described for the Digital Output.

12. Analog Output (Pin 13)

The Analog Output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This wave form is then filtered with an external low-pass filter with sin x/x correction to recreate the sample voice signal.

13. Analog Ground (Pin 14)

14. Positive and Negative Reference Voltages, (Pin 15, 16) V_{ref} (−), V_{ref} (+)

These inputs provide the conversion reference for the digital-to-analog converter in the KT5116. V_{ref} (+) and V_{ref} (−) must maintain 100ppm/°C regulation over the operating temperature. Variation of the reference directly affects system again.

RECOMMENDED ANALOG INPUT CIRCUIT

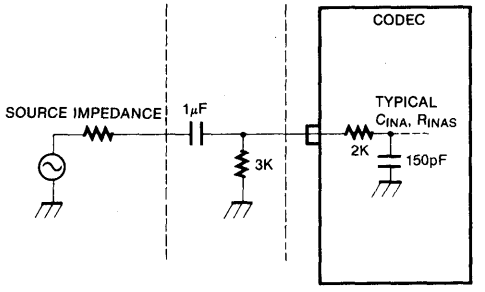


Fig. 1

TRANSMITTER SECTION TIMING

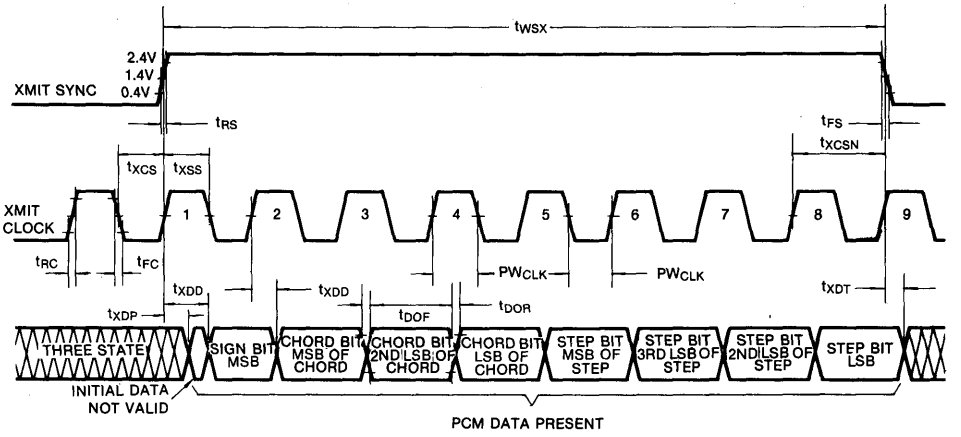


Fig. 2

RECEIVER SECTION TIMING

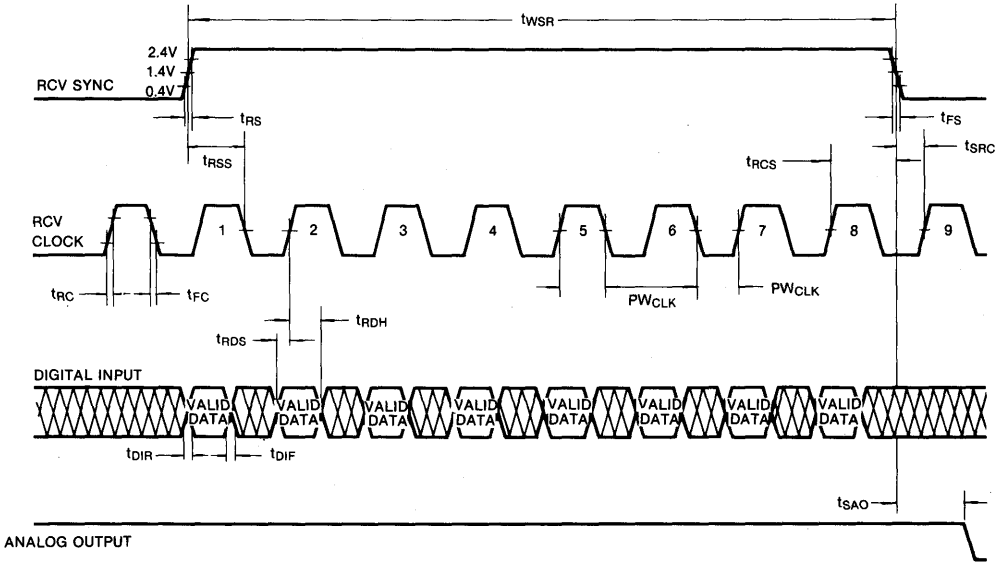


Fig. 3

Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Fig. 4 S/D RATIO VS INPUT LEVEL

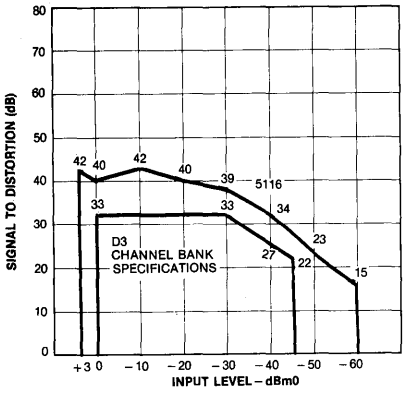
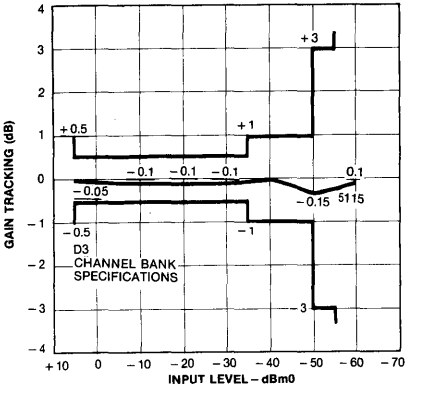


Fig. 5 GAIN TRACKING PERFORMANCE



A/D, D/A CONVERSION TIMING

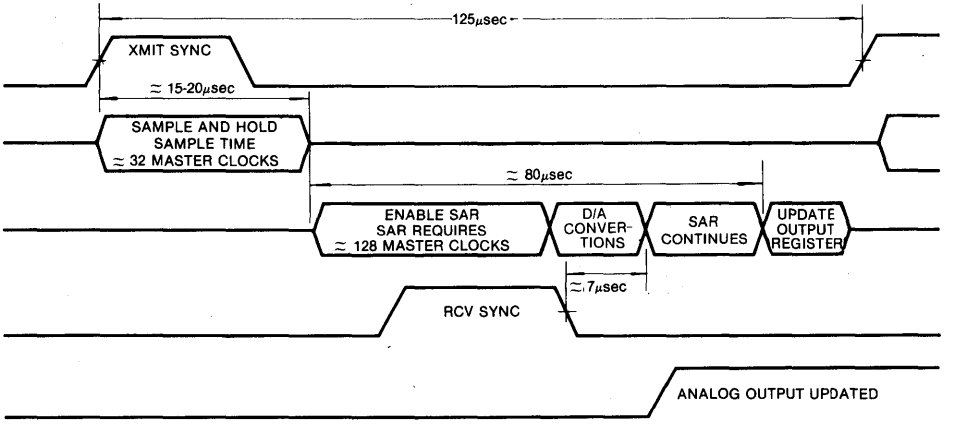
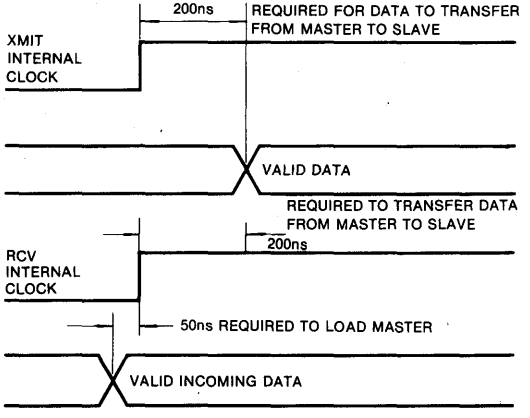


Fig. 6

DATA INPUT/OUTPUT TIMING



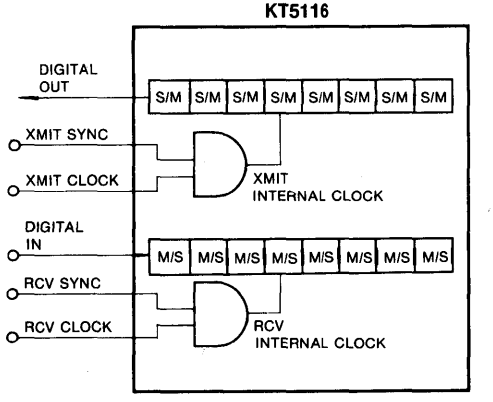


Fig. 7

A/D CONVERTER (μ-Law Encoder) TRANSFER CHARACTERISTIC

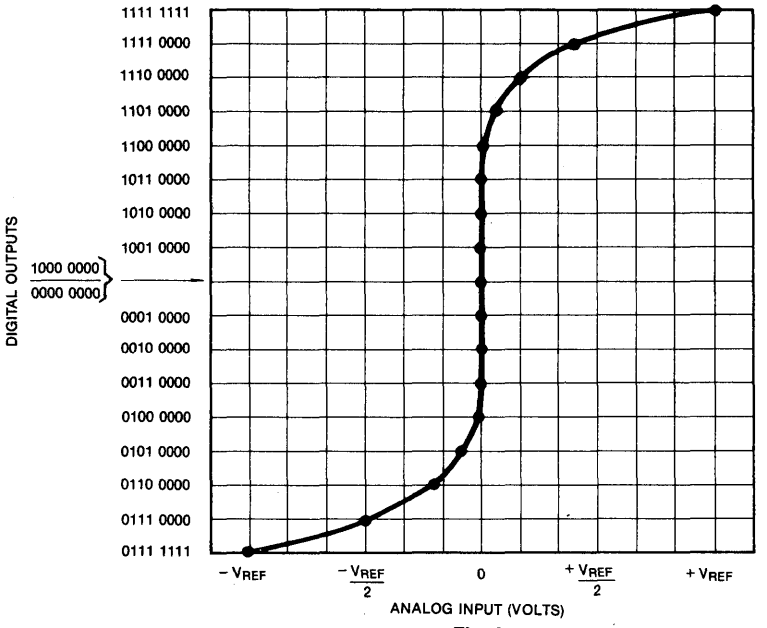


Fig. 8

D/A CONVERTER (μ-Law Decoder) TRANSFER CHARACTERISTIC

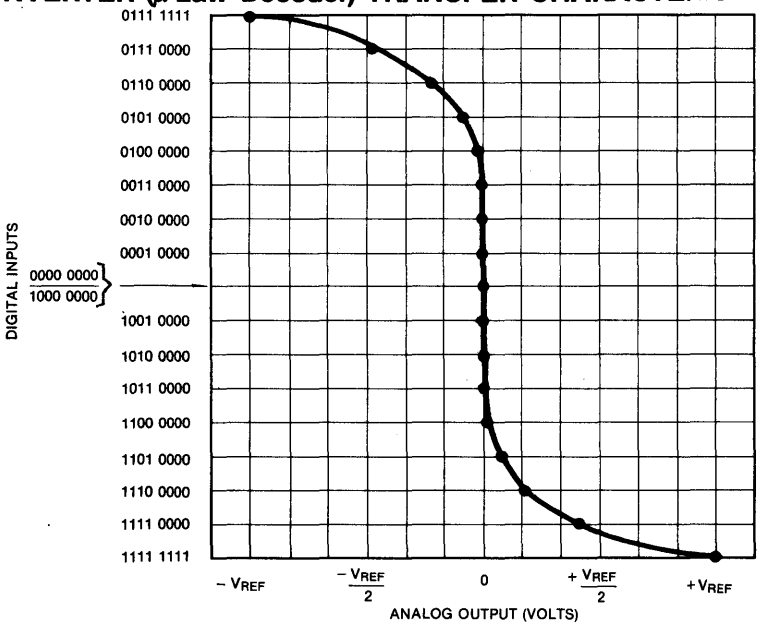


Fig. 9

64KHz OPERATION, TRANSMITTER SECTION TIMING

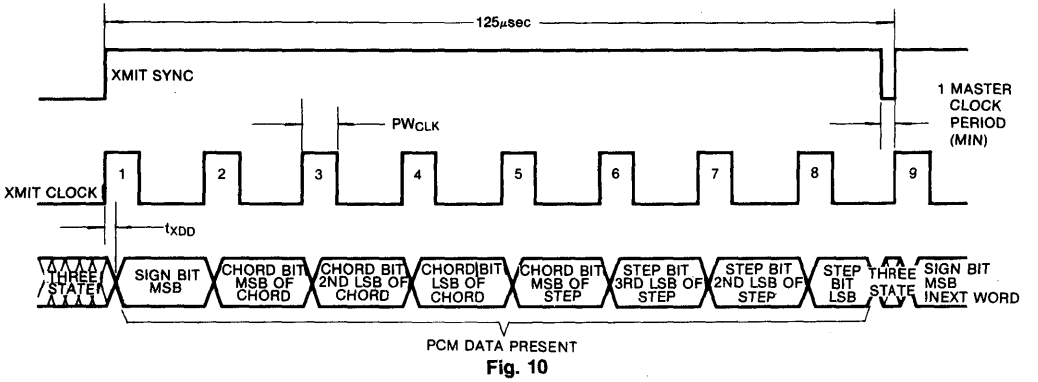


Fig. 10

Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64KHz OPERATION, RECEIVER SECTION TIMING

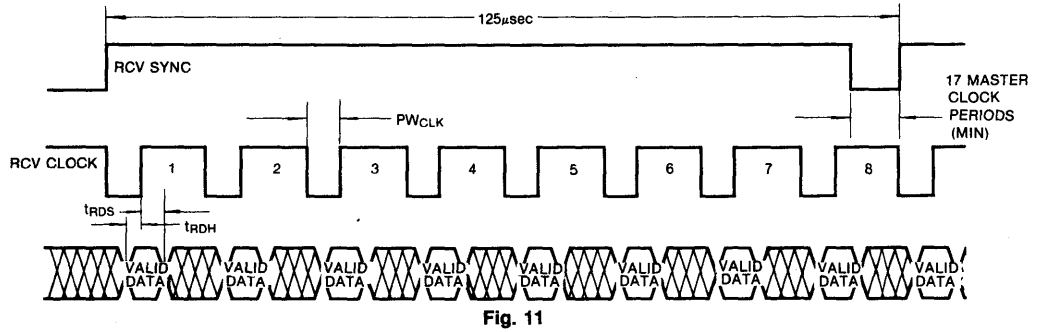
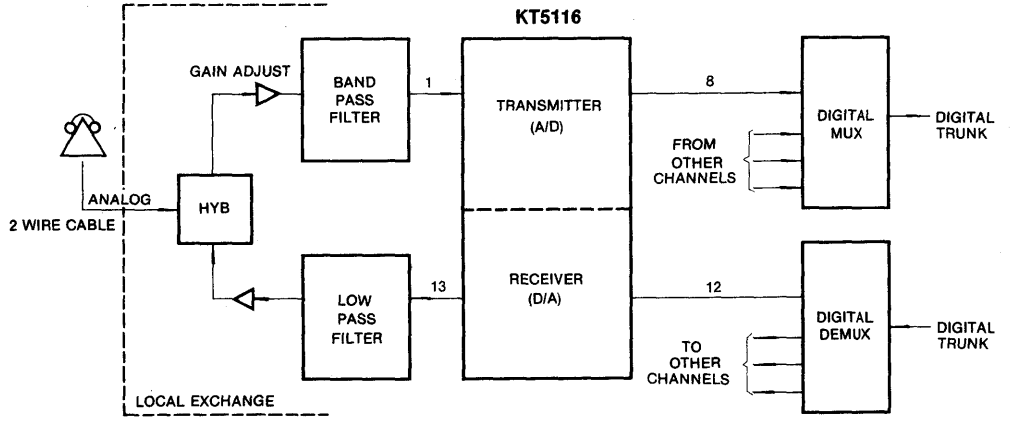


Fig. 11

Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

PCM SYSTEM BLOCK DIAGRAM



SYSTEM CHARACTERISTICS TEST CONFIGURATION

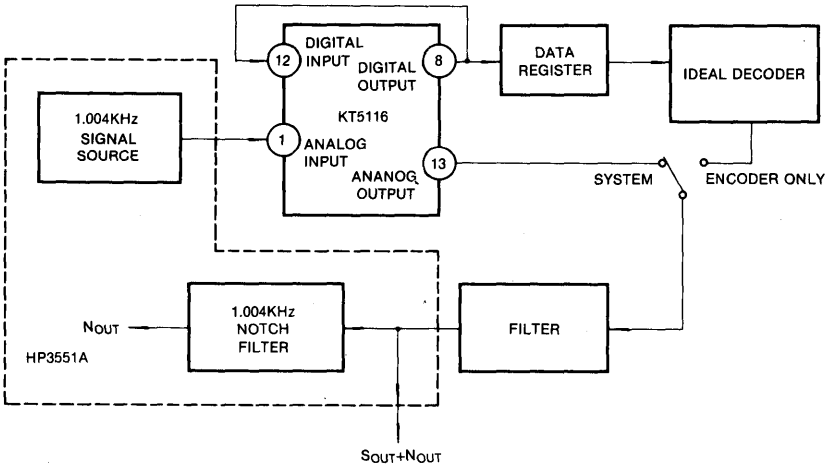


Fig. 12

Note: The ideal decoder consists of a digital decomponder and a 13-bit precision DAC.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 12 can be used to evaluate the performance of the KT5116. An analog signal provided by the HP3551 a transmission test set is connected to the Analog Input (Pin 1) of the KT5116. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3551A.

Remaining pins of the KT5116 are connected as follows:

1. RCV SYNC is tied to XMIT SYNC.
2. XMIT CLOCK is tied to Master CLOCK. The signal is inverted and tied to RCV clock.

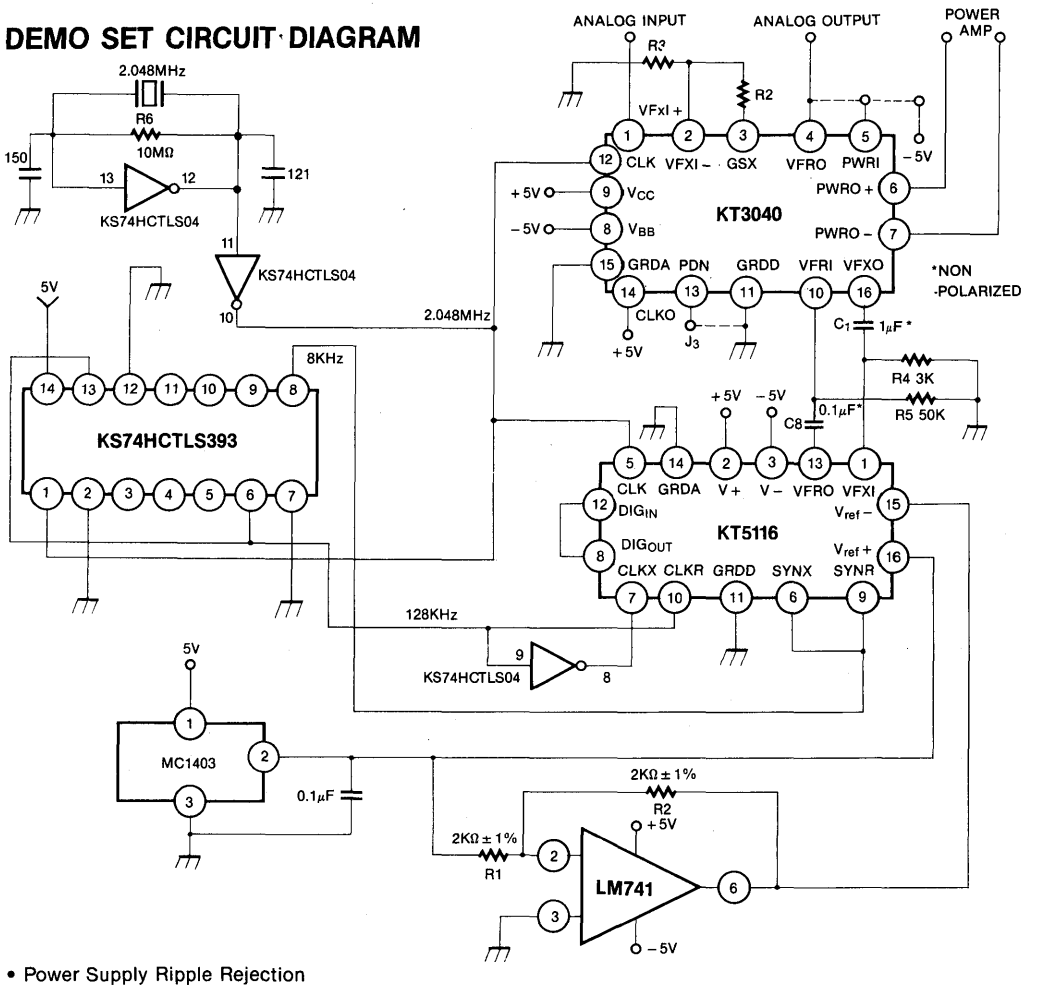
The following timing signals are required:

1. Master CLOCK=2.048MHz
2. XMIT SYNC repetition rate=8KHz
3. XMIT SYNC width=8 XMIT CLOCK periods.

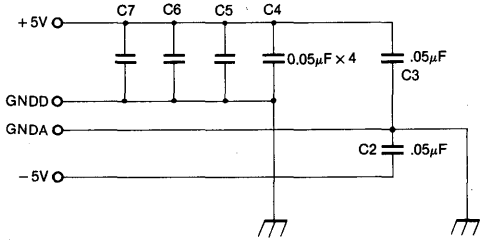
when all the above requirements are met, the set-up of Figure 12 permits the measurement of synchronous system performance over a wide range of Analog Inputs.

The data register and ideal decoder provide a means of checking the encoder portion of the KT5116 independently of the decoder section. To test the system in the asynchronous mode, Master CLOCK should be separated from RCV CLOCK. XMIT CLOCK and RCV CLOCK are separated also.

DEMO SET CIRCUIT DIAGRAM



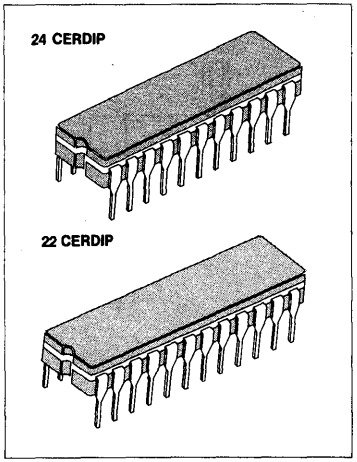
• Power Supply Ripple Rejection



NOTE: All unused input connected to GNDD or V_{CC}, only in HCT series.

MONOLITHIC CODECS

The devices are monolithic PCM CODECs implemented with high reliability CMOS technology. The KT8520 is intended for μ-law applications and the KT8521 is intended for A-law applications.
Integrated into the CODECs are circuits for signaling interface, PCM time-slot control logic, analog-to-digital (A/D) conversion, and digital-to-analog (D/A) conversion. The devices are intended to be used with the KT3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sinx/x distortion introduced by the decoder sample and hold output.



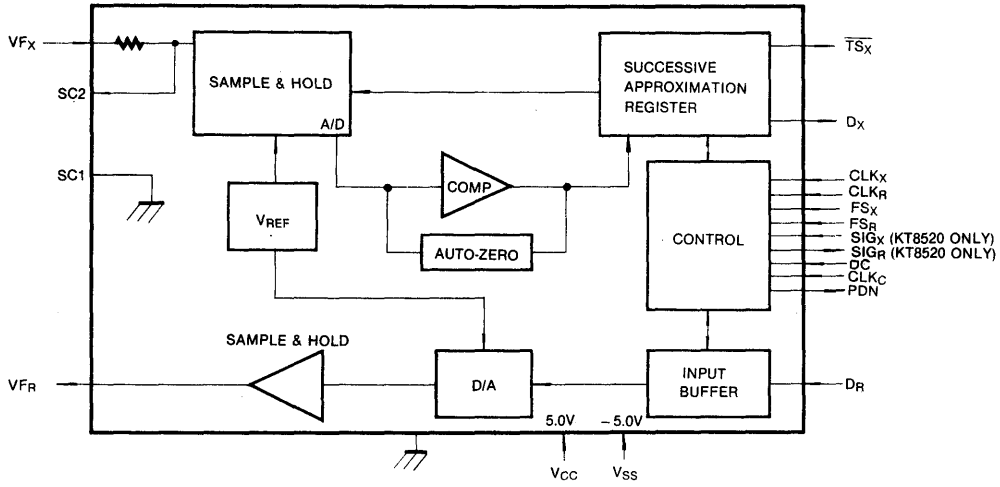
FEATURES

- **Low power consumption: 45 mW (operation)**
  1 mW (standby)
- **±5V power supplies.**
- **TTL compatible digital inputs and outputs**
- **Optional programmable time slot selection**
- **Internal sample and hold capacitors, auto zero circuit**
- **KT8520: μ-law, 24 DIP**
- **KT8521: A-law, 22 DIP**
- **Synchronous or asynchronous operation**

ORDERING INFORMATION

Device	Package	Operating Temperature
KT8520N	Plastic	−25 ~ +125°C
KT8521N	Plastic	
KT8520J	Ceramic	
KT8521J	Ceramic	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
V_{CC}	V_{CC}	7	V
V_{BB}	V_{BB}	−7	V
Any Analog Input or Output	Analog I/O	V_{BB} − 0.3 to V_{CC} + 0.3	V
Any Digital Input or Output	Digital I/O	GND − 0.3 to V_{CC} + 0.3	V
Operating Temperature Range	Ta	−25 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C
Lead Temperature (Soldering, 10 secs)	T_L	300	°C

3

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{CC} = 5.0V ± 5%, V_{BB} = −5.0V ± 5%, Ta = 0°C to 70°C, typical characteristics specified at V_{CC} = 5.0V, V_{BB} = −5.0V, Ta = 25°C. All signals referenced to GND.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
POWER DISSIPATION						
Operating Current, V_{CC}	I_{CC1}			4.5	8.0	mA
Operating Current, V_{BB}	I_{BB1}			4.5	8.0	mA
Standby Current, V_{CC}	I_{CCO}			0.1	0.4	mA
Standby Current, V_{BB}	I_{BBO}			0.03	0.1	mA
DIGITAL INTERFACE						
Input Current	I_I	$0 < V_{IN} < V_{CC}$	−10		10	μA
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2.2			V
Output Low Voltage	V_{OL}	D_X, I_{OL} = 4.0mA SIG_R, I_{OL} = 0.5mA $\overline{TS_X}$, I_{OL} = 3.2mA, Open Drain PDN, I_{OL} = 1.6mA			0.4 0.4 0.4 0.4	V V V V
Output High Voltage	V_{OH}	D_X, I_{OH} = 6.0mA SIG_R, I_{OH} = 0.6mA	2.4 2.4			V V
ANALOG INTERFACE						
VFX Input Impedance when Sampling	Z_I	Resistance in series with 70pF	2.0			KΩ
Output Impedance at VFR	Z_O	−3.1V < VFR < 3.1V		10	20	Ω
Output Offset Voltage at VFR	V_{OS}	DR = PCM Zero Code (KT8520) or Alternating ± 1 Code (KT8521)	−25		25	mV
Analog Input Bias Current	I_{IN}	V_{IN} = 0V	−0.1		0.1	μA
DC Blocking Time Constant	R1·C1		4.0			mS
Input Bias Resistor	R1				160	KΩ
DC Blocking Capacitor	C1		0.1			μF

AC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, the analog input is a 0dBm0, 1.02KHz sine wave. $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, $Ta = 0°C$ to $70°C$, typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, $Ta = 25°C$. All signals referenced to GND.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Absolute Transmit Gain	G_{XA}	$V_{CC} = 5V$, $V_{BB} = -5V$, $T = 25°C$	−0.375		−0.025	dB
Absolute Transmit Gain Variation with Temperature	G_{XAT}	$T = 0°C$ to $70°C$	−0.05		0.05	dB
Absolute Transmit Gain Variation with Supply Voltage	G_{XAV}	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$	−0.07		0.07	dB
Absolute Receive Gain	G_{RA}	$V_{CC} = 5V$, $V_{BB} = -5V$, $T = 25°C$	−0.175		0.175	dB
Absolute Receive Gain Variation with Temperature	G_{RAT}	$T = 0°C$ to $70°C$	−0.05		0.05	dB
Absolute Receive Gain Variation with Supply Voltage	G_{RAV}	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$	−0.07		0.07	dB
Absolute Receive & Transmit Gain Variation with Level	G_{RAL} G_{XAL}	CCITT Method 2 Relative to −10dBm0 0dBm0 to 3dBm0 −40dBm0 to 0dBm0 −50dBm0 to −40dBm0 −55dBm0 to −50dBm0	 −0.3 −0.2 −0.4 −1.0		 0.3 0.2 0.4 1.0	 dB dB dB dB
Receive & Transmit Signal to Distortion Ratio	S/D_R S/D_X	Sinusoidal Test Method Input Level −30dBm0 to 0dBm0 −40dBm0 −45dBm0	 35 29 25			 dBc dBc dBc
Idle Channel Noise, Receive	N_R	DR = Steady State PCM Code			6	$dB_{rnc}0$
Idle Channel Noise, Transmit	N_X	No Signaling (KT8520) Note 1 (KT8521)			13 −66*	$dB_{rnc}0$ dBnOp
Receive & Transmit Harmonic Distortion	HD_R HD_X	2nd or 3rd Harmonic			−47	dB
Transmit Positive Power Supply Rejection	$PPSR_X$	Input Level = 0V, $V_{CC} = 5.0V_{dc}$ + $300mV_{rms}$, f = 1.02KHz	50			dB
Receive Positive Power Supply Rejection	$PPSR_R$	D_R = Steady PCM Code $V_{CC} = 5.0V_{dc} + 300mV_{rms}$, f = 1.02KHz	40			dB
Transmit Negative Power Supply Rejection	$NPSR_X$	Input Level = 0V, $V_{BB} = -5.0V_{dc}$ + $300mV_{rms}$, f = 1.02KHz	50			dB

AC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Receive Negative Power Supply	$NPSR_R$	D_R = Steady PCM Code $V_{BB} = -5.0V_{dc} + 300mV_{rms}$ f = 1.02KHz	45			dB
Transmit to Receive Crosstalk	CT_{XR}	D_R = Steady PCM Code			−75	dB
Receive to Transmit Crosstalk	CTR_X	Transmit Input Level = 0V KT8520 KT8521 (Note 2)			 −70 −65	 dB dB

Note 1: Measured by extrapolation from the distortion test result at −50dBm0 level.
Note 2: Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

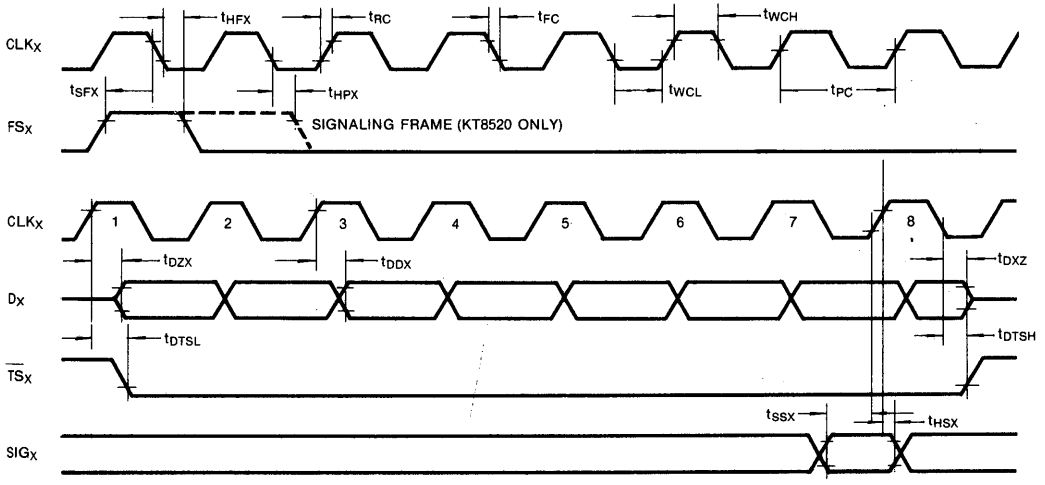
TIMING CHARACTERISTICS

(Unless otherwise noted, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, Ta = 0°C to 70°C, typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, Ta = 25°C. All signals referenced to GND. All timing parameters are measured at $V_{OH} = 2.0V$, $V_{OL} = 0.7V$.)

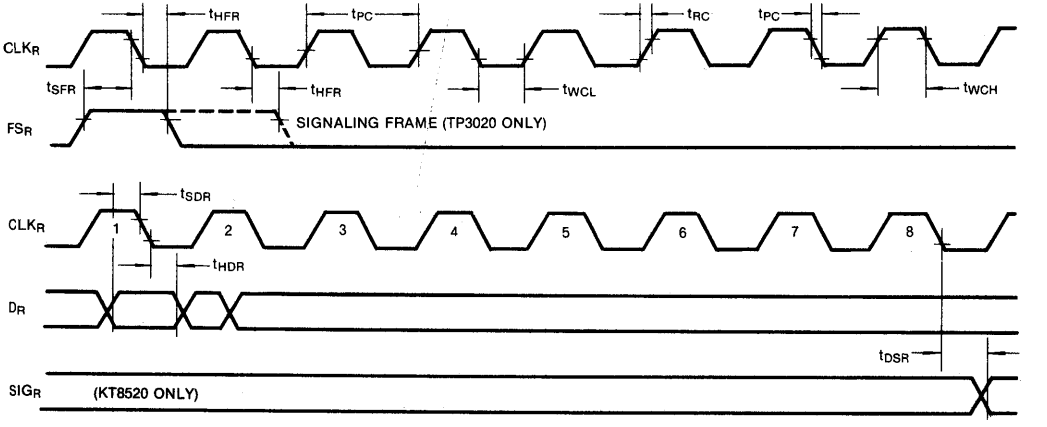
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Clock Period	t_{PC}	CLK_C, CLK_R, CLK_X	485			nS
Clock Rise and Fall Time	t_{RC}, t_{FC}	CLK_C, CLK_R, CLK_X			30	nS
Clock Pulse Width (High, Low)	$t_{WCH/L}$	CLK_C, CLK_R, CLK_X	165			nS
A/D Conversion Time	$t_{A/D}$	From end of encoder time Slot to completion of conversion			16	Time Slots
D/A Conversion Time	$t_{D/A}$	From end of decoder time Slot to transition of VF_R			2	Time Slots
D_C to CLK_C Set-Up Time	t_{SDC}		100			nS
CLK_C to D_C Hold Time	t_{HDC}		100			nS
FS_X to CLK_X Set-Up Time	t_{SFX}		100			nS
CLK_X to FS_X Hold Time	t_{HFX}		100			nS
Delay Time to Enable D_X on TS Entry	t_{DZX}	$C_L = 150pF$	25		125	nS
Delay Time, CLK_X to D_X	t_{DDX}	$C_L = 150pF$			125	nS
Delay Time, D_X to High Impedance State on TS Exit	t_{DXZ}	$C_L = 0pF$	50		165	nS
Delay to $\overline{TS}_X$ Low	t_{DTSL}	$0 \leq C_L \leq 150pF$	30		185	nS
Delay to $\overline{TS}_X$ Off	t_{DTSH}	$C_L = 0pF$	30		185	nS
Delay Time, CLK_R to SIG_R	t_{DSR}	$C_L = 100pF$			300	nS
SIG_X to CLK_X Set-Up Time	t_{SSX}		100			nS
CLK_X to SIG_X Hold Time	t_{HSX}		100			nS
FS_R to CLK_R Set-Up Time	t_{SFR}		100			nS
CLK_R to FS_R Hold Time	t_{HFR}		100			nS
D_R to CLK_R Set-Up Time	t_{SDR}		40			nS
CLK_R to D_R Hold Time	t_{HDR}		30			nS

TIMING DIAGRAM

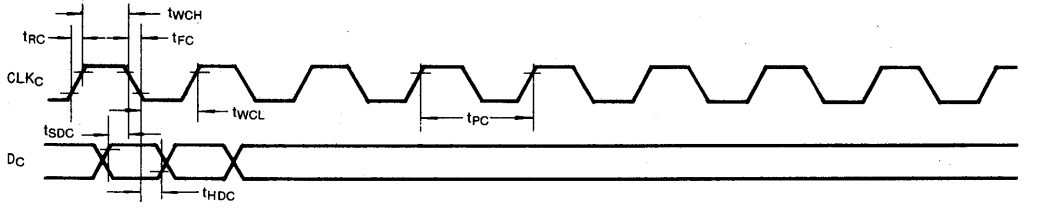
TRANSMIT TIMING



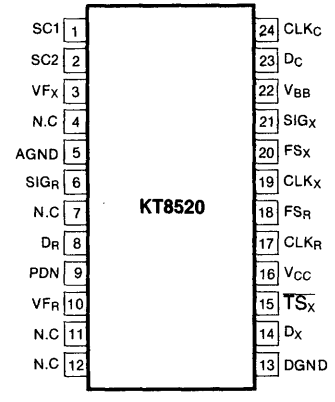
RECEIVE TIMING

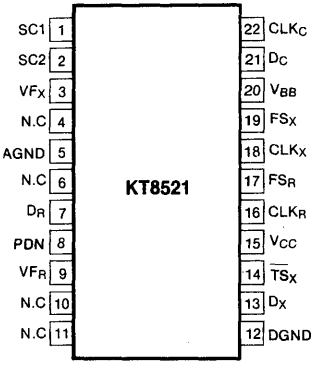


CONTROL TIMING



PIN CONFIGURATION





PIN DESCRIPTION

Name	Function
SC1	Internally connected to GNDA.
SC2	Connects VF_X to an external sample/hold capacitor if fitted for use with pin-compatible NMOS CODECs. Ensures gain compatibility.
VF_X	Analog input to be encoded into a PCM word. The signal in this pin is sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
NC	No connect. Recommended practice is to strap the NC pin to GND.
A/D GND	Analog & Digital ground. All analog & digital signals are referenced to this pin.
SIG_R	Receive signaling bit output. During receive signaling frames the LSB (Least Significant Bit) shifted into D_R is internally latched and appears at this output-SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, MSB (most significant bit) first, on the falling edge of CLK_R.
PDN	Power down output is active high when the CODEC is in the power down state. The open drain output is capable of sinking one TTL load.
VF_R	Analog output.
D_X	Serial PCM output from the encoder (Three-state output). During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, MSB first, on the rising edge of CLK_X.
$\overline{TS_X}$	Time slot output. (TTL compatible open drain). This output pulses low during the encoder time slot.
V_{CC}	+5V ± 5%, referenced to GND.
CLK_R	Master decoder clock input. This input used to shift in the PCM data on D_R and to operate the decoder sequencer. Operating at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_X or CLK_C.

PIN DESCRIPTION (Continued)

Name	Function
FS_R	Decoder frame synchronous pulse. Normally occurring at an 8KHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.
CLK_X	Master encoder clock input. This input used to shift out the PCM data on D_X and to operate the encoder sequencer. Operating at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_R or CLK_C.
FS_X	Encoder frame synchronous pulse. Normally occurring at an 8KHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_R to two or more cycles of CLK_X signifies a transmit signaling frame.
SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the last bit of PCM data.
V_{BB}	$-5V \pm 5\%$, referenced to GND.
DC	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power down input.
CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting this pin continuously high, the CODEC, into the fixed time slot mode.

FUNCTIONAL DESCRIPTION

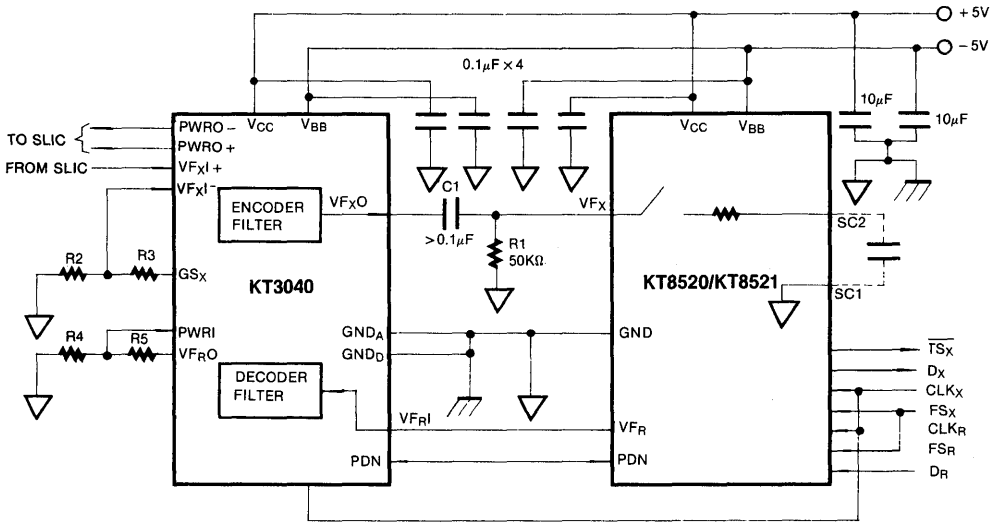
The CODECs are capable of operating as transmitters and receivers in any of the 64 channels of a PCM system. The receive and transmit sections can be assigned to the same channel (time slot) or to different channels, and assignments can be changed under microcomputer control to meet changing system needs. Table 1 shows the control options.

<table>
<tr><th>Control
CLK_C</th><th>Signals
DC</th><th>Operation</th></tr>
<tr><td>L</td><td>X</td><td>Undefined operation</td></tr>
<tr><td>V_{CC}</td><td>H</td><td>Power-down or standby operational status</td></tr>
<tr><td>V_{CC}</td><td>L</td><td>Direct-control operation. Receive and transmit in the first time slot.</td></tr>
<tr><td>↓</td><td>X</td><td>Microcomputer-control operation. Clock in one of 8 bits of the control word at the D_C input.
<table>
<tr><th>B1</th><th>B2</th><th colspan="5">Action</th></tr>
<tr><td>0</td><td>0</td><td colspan="5">Assign time slot to encoder & decoder</td></tr>
<tr><td>0</td><td>1</td><td colspan="5">Assign time slot to encoder</td></tr>
<tr><td>1</td><td>0</td><td colspan="5">Assign time slot to decoder</td></tr>
<tr><td>1</td><td>1</td><td colspan="5">Power-down CODEC</td></tr>
<tr><th>B3</th><th>B4</th><th>B5</th><th>B6</th><th>B7</th><th>B8</th><th>Time Slot</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>3</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>4</td></tr>
<tr><td>·</td><td>·</td><td>·</td><td>·</td><td>·</td><td>·</td><td>·</td></tr>
<tr><td>·</td><td>·</td><td>·</td><td>·</td><td>·</td><td>·</td><td>·</td></tr>
<tr><td>·</td><td>·</td><td>·</td><td>·</td><td>·</td><td>·</td><td>·</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>63</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>64</td></tr>
</table>
Bits 3 through 8 for time-slot assignments 1 through 64. The time-slot numbers equal one more than the decimal equivalent represented by bits 3 (MSB) through 8 (LSB) using positive logic.</td></tr>
</table>

Note: H = High Level, L = Low Level, X = Irrelevant, ↓ = From V_{CC} to Low Transition

TABLE 1. OPERATION CONTROL CONFIGURATIONS

APPLICATION CIRCUIT (TYPICAL)



Analog Ground

Digital Ground

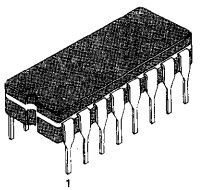
Transmit Gain = $20 \times \log \left(\frac{R3 + R2}{R2}\right) + 3dB$

Receive Gain = $20 \times \log \left(\frac{R4}{R2 + R5}\right)$ for each power amp

COMBO CODECS

The KT8554 and KT8557 are single-chip PCM encoders and decoders (PCM CODECs) and PCM line filters. These devices provide all the functions required to interface a full-duplex voice telephone circuit with a time-division-multiplexed (TDM) system.
These devices are designed to perform the transmit encoding and receive decoding as well as the transmit and receive filtering functions in PCM system. They are intended to be used at the analog termination of a PCM line or trunk.
These devices provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signaling and supervision information.

16 CERDIP



FEATURES

- **Complete CODEC and filtering system**
- **Meets or exceeds AT&T D3/D4 and CCITT specifications**
  μ-Law: KT8554, A-Law: KT8557
- **On-chip auto zero, sample and hold, and precision voltage references**
- **Low power dissipation: 60mW (operating)**
  3mW (standby)
- **$\pm$5V operation**
- **TTL or CMOS compatible**
- **Automatic power down**

ORDERING INFORMATION

Device	Package	Operating Temperature
KT8554N	Plastic	$-25 \sim +125°C$
KT8557N	Plastic	
KT8554J	Ceramic	
KT8557J	Ceramic	

BLOCK DIAGRAMS

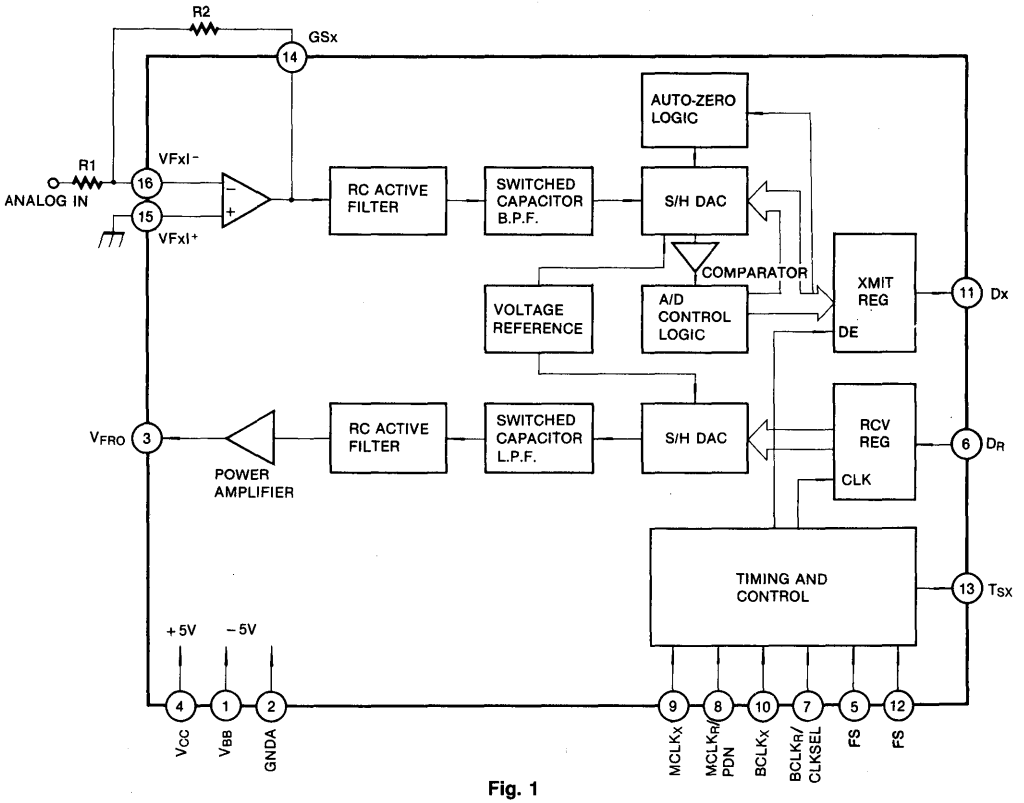


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic.	Symbol	Value	Unit
V_{CC} to GNDA	V_{CC}	7	V
V_{BB} to GNDA	V_{BB}	−7	V
Voltage at Any Analog Input or Output	AI/O	$V_{CC}+0.3$ to $V_{BB}-0.3$	V
Voltage at Any Digital Input or Output	DI/O	$V_{CC}+0.3$ to GNDA − 0.3	V
Operating Temperature Range	Ta	−25 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (Soldering, 10 secs)	T_L	300	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, GNDA = 0V, Ta = 0°C to 70°C; typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, Ta = 25°C; all signals referenced to GNDA.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Power Dissipation						
Power-Down Current	$I_{CC}0$	No Load		0.5	1.5	mA
Power-Down Current	$I_{BB}0$	No Load		0.05	0.3	mA
Active Current	$I_{CC}1$	No Load		6.0	9.0	mA
Active Current	$I_{BB}1$	No Load		6.0	9.0	mA
Digital Interface						
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2.2			V
Input Low Current	I_{IL}	$GNDA \leq V_{IN} \leq V_{IL}$, all digital inputs	−10		10	μA
Input High Current	I_{IH}	$V_{IH} \leq V_{IN} \leq V_{CC}$	−10		10	μA
Output Low Voltage	V_{OL}	D_X, $I_L = 3.2mA$ SIG_R, $I_L = 1.0mA$ $\overline{TS}_X$, $I_L = 3.2mA$, open drain			0.4 0.4 0.4	V V V
Output High Voltage	V_{OH}	D_X, $I_H = -3.2mA$ SIG_R, $I_H = -1.0mA$	2.4 2.4			V V
Output Current in High Impedance State (TRI-STATE)	I_{OZ}	D_X, $GNDA \leq V_O \leq V_{CC}$	−10		10	μA
Analog Interface with Receive Filter						
Output Resistance	$R_O RF$	Pin VF_RO		1	3	Ω
Load Resistance	$R_L RF$	$VF_RO = \pm 2.5V$	600			Ω
Load Capacitance	$C_L RF$				500	pF
Output DC Offset Voltage	VOS_RO		−200		200	mV
Analog Interface with Transmit Input Amplifier						
Input Leakage Current	$I_I XA$	$-2.5V \leq V \leq +2.5V$, VF_XI+ or VF_XI-	−200		200	nA
Input Resistance	$R_I XA$	$-2.5V \leq V \leq +2.5V$, VF_XI+ or VF_XI-	10			MΩ
Output Resistance	$R_O XA$	Closed loop, unity gain		1	3	Ω
Load Resistance	$R_L XA$	GS_X	10			KΩ
Load Capacitance	$C_L XA$	GS_X			50	pF
Output Dynamic Range	$V_O XA$	GS_X, $R_L \leq 10K\Omega$	±2.8			V
Voltage Gain	$A_V XA$	VF_XI+ to GS_X	5,000			V/V
Unity Gain Bandwidth	$F_U XA$		1	2		MHz
Offset Voltage	$V_{OS} XA$		−20		20	mV
Common-Mode Voltage	$V_{CM} XA$	CMRRXA > 60dB	−2.5		2.5	V
Common-Mode Rejection Ratio	CMRRXA	DC Test	60			dB
Power Supply Rejection Ratio	PSRRXA	DC Test	60			dB

TIMING CHARACTERISTICS

(Unless otherwise noted, $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, GNDA = 0V, Ta = 0°C to 70°C; typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, Ta = 25°C; all signals referenced to GNDA.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency of Master Clocks	$1/t_{PM}$	Depends on the device used and the $BCLK_R$/CLKSEL Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
Rise Time of Bit Clock	t_{RB}	$t_{PB} = 488ns$			50	ns
Fall Time of Bit Clock	t_{FB}	$t_{PB} = 488ns$			50	ns
Holding Time from Bit Clock Low to Frame Sync	t_{HBFL}	Long frame only	0			ns
Holding Time from Bit Clock High to Frame Sync	t_{HOLD}	Short frame only	0			ns
Set-Up Time from Frame Sync to Bit Clock Low	t_{SFB}	Long frame only	80			ns
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load = 150pF plus 2 LSTTL loads	0		180	ns
Delay Time to $\overline{TS_X}$ Low	t_{XDP}	Load = 150pF plus 2 LSTTL loads			140	ns
Delay Time from $BCLK_X$ Low to Data Output Disabled	t_{DZC}		50		165	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	t_{DZF}	$C_L = 0pF$ to 150pF	20		165	ns
Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low	t_{SDB}		50			ns
Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	t_{HBD}		50			ns
Delay Time from $BCLK_{R/X}$ Low to SIG_R Valid	t_{DFSSG}	Load = 50pF plus 2 LSTTL loads			300	ns
Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	t_{SF}	Short frame sync pulse (1 or 2 bit clock periods long) (Note 1)	50			ns
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160			ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160			ns
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$			50	ns
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$			50	ns
Set-Up Time from $BCLK_X$ High (and FS_X In Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First bit clock after the leading edge of FS_X				
Period of Bit Clock	t_{PB}		485	488	15,725	ns
Width of Bit Clock High	t_{WBH}	$V_{IH} = 2.2V$	160			ns
Width of Bit Clock Low	t_{WBL}	$V_{IL} = 0.6V$	160			ns

TIMING CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	t_{HF}	Short frame sync pulse (1 or 2 bit clock periods long) (Note 1)	100			ns
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	t_{HBFI}	Long frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K bit/s operating mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

TIMING DIAGRAM

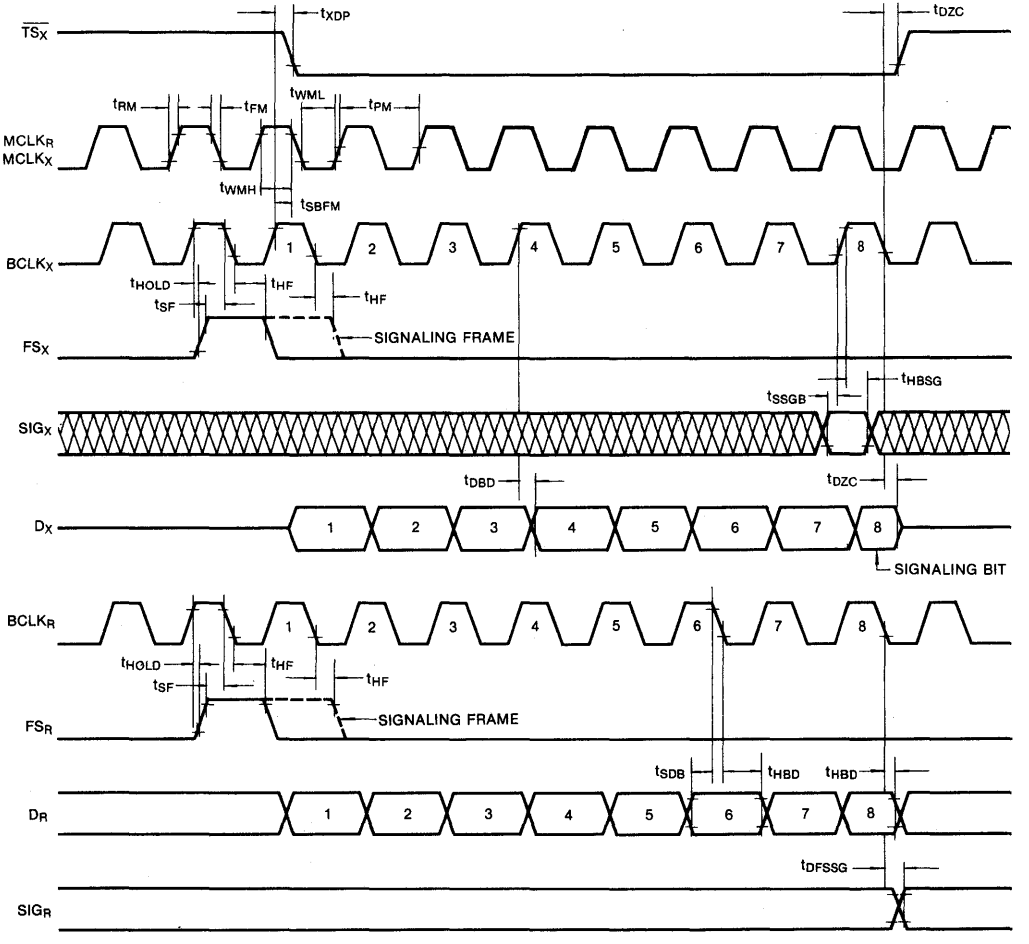


Fig. 2. Short Frame Sync Timing

TIMING DIAGRAM (Continued)

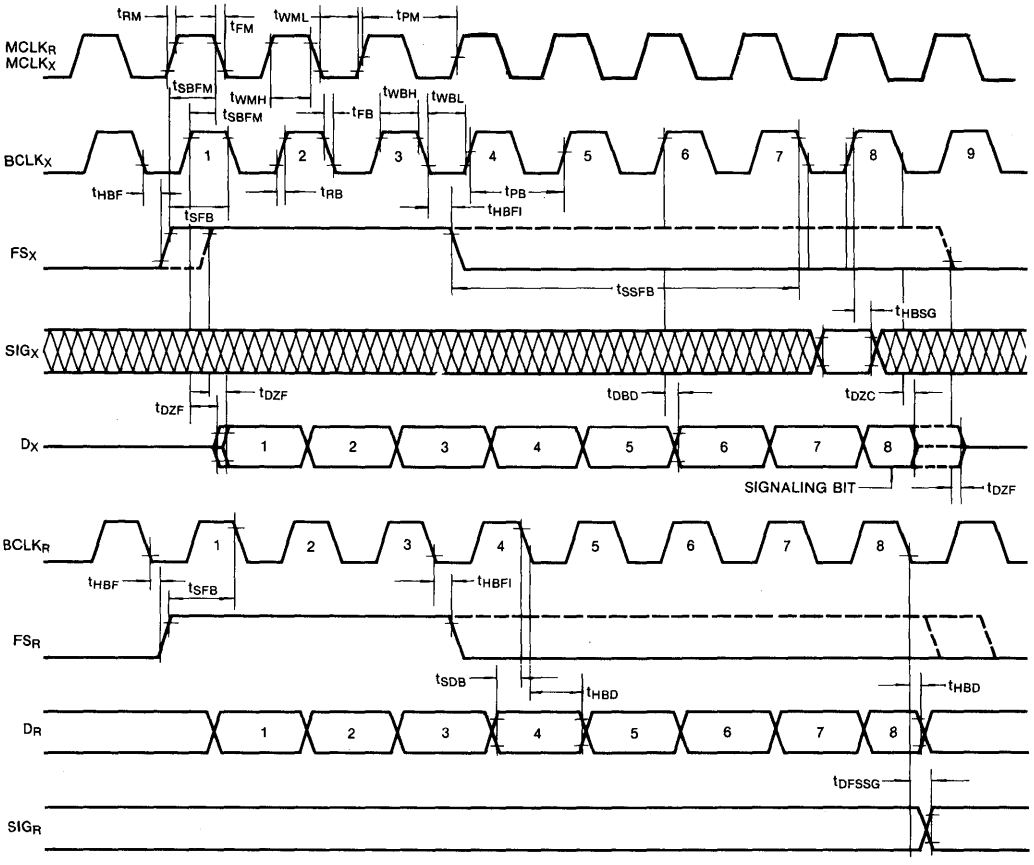


Fig. 3 Long Frame Sync Timing

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, GNDA = 0V, f = 1.02KHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Amplitude Response						
Receive Gain, Absolute	G_{RA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input = Digital code sequence for 0dBm0 signal at 1020Hz	−0.15		0.15	dB
Receive Gain, Relative to G_{RA}	G_{RR}	f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
Absolute Receive Gain Variation with Temperature	G_{RAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Receive Gain Variation with Supply Voltage	G_{RAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Receive Gain Variations with Level	G_{RRL}	Sinusoidal test method; reference input PCM code corresponds to an Ideally encoded −10dBm0 signal PCM level = −40dBm0 to +3dBm0 PCM level = −50dBm0 to −40dBm0 PCM level = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
Receive Output Drive Level	V_{RO}	R_L = 600Ω	−2.5		2.5	V
Absolute Levels	A_L	Nominal 0dBm0 level is 4dBm (600Ω) 0dBm0		1.2276		V_{rms}
Max Overload Level	t_{MAX}	Max overload level (3.17dBm0): KT8554 Max overload level (3.14dBm0): KT8557		2.501		V_{PK}
Transmit Gain, Absolute	G_{XA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input at GS_X = 0dBm0 at 1020Hz	−0.15		0.15	dB
Transmit Gain, Relative to G_{XA}	G_{XR}	f = 16Hz f = 50Hz f = 60Hz f = 200Hz f = 300Hz − 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure response from 0Hz to 4000Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
Absolute Transmit Gain Variation with Temperature	G_{XAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Transmit Gain Variation with Supply Voltage	G_{XAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Transmit Gain Variations with Level	G_{XRL}	Sinusoidal test method Reference level = −10dBm0 VF_XI+ = −40dBm0 to +3dBm0 VF_XI+ = −50dBm0 to −40dBm0 VF_XI+ = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB

3

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Envelope Delay Distortion with Frequency						
Receive Delay, Absolute	D_{RA}	f = 1600Hz		180	200	μs
Receive Delay, Relative to D_{RA}	D_{RR}	f = 500Hz – 1000Hz	– 40	– 25		μs
		f = 1000Hz – 1600Hz	– 30	– 20		μs
		f = 1600Hz – 2600Hz		70	90	μs
		f = 2600Hz – 2800Hz		100	125	μs
		f = 2800Hz – 3000Hz		145	175	μs
Transmit Delay, Absolute	D_{XA}	f = 1600Hz		290	315	μs
Transmit Delay, Relative to D_{XA}	D_{XR}	f = 500Hz – 600Hz		195	220	μs
		f = 600Hz – 800Hz		120	145	μs
		f = 800Hz – 1000Hz		50	75	μs
		f = 1000Hz – 1600Hz		20	40	μs
		f = 1600Hz – 2600Hz		55	75	μs
		f = 2600Hz – 2800Hz		80	105	μs
		f = 2800Hz – 3000Hz		130	155	μs
Noise						
Receive Noise, C Message Weighted	N_{RC}	PCM code equals alternating positive and negative zero, KT8554		8	11	dBrnc0
Receive Noise, P Message Weighted	N_{PP}	PCM code equals, positive zero, KT8557		– 82	– 79	dBm0p
Transmit Noise, C Message Weighted	N_{XC}	KT8554		12	15	dBrnc0
Transmit Noise, P Message Weighted	N_{XP}	KT8557		– 74	– 67	dBm0p
Noise, Single Frequency	N_{RS}	f = 0KHz to 100KHz, loop around measurement, $VF_XI+ = 0V_{rms}$			– 53	dBm0
Positive Power Supply Rejection, Transmit	$PPSR_X$	$VF_XI+ = 0V_{rms}$, $V_{CC} = 5.0V_{DC} + 100mV_{rms}$ f = 0KHz – 50KHz	40			dBC
Negative Power Supply Rejection, Transmit	$NPSR_X$	$VF_XI+ = 0V_{rms}$, $V_{BB} = -5.0V_{DC} + 100mV_{rms}$ f = 0KHz – 50KHz	40			dBC
Positive Power Supply Rejection, Receive	$PPSR_R$	PCM code equals positive zero $V_{CC} = 5.0V_{DC} + 100mV_{rms}$				
		f = 0Hz – 4000Hz	40			dBC
		f = 4KHz – 25KHz	40			dB
		f = 25KHz – 50KHz	36			dB
Negative Power Supply Rejection, Receive	$NPSR_R$	PCM code equals positive zero $V_{BB} = -5.0V_{DC} + 100mV_{rms}$				
		f = 0Hz – 4000Hz	40			dBC
		f = 4KHz – 25KHz	40			dB
		f = 25KHz – 50KHz	36			dB

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious Out-of-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0, 300Hz – 3400Hz input applied to VF_XI+, Measure individual image signals at VF_RO 4600Hz – 7600Hz 7600Hz – 8400Hz 8400Hz – 100,000Hz			 – 32 – 40 – 32	 dB dB dB
Distortion						
Signal to Total Distortion	STD_X	Sinusoidal test method				
Transmit or Receive Half-Channel	STD_R	Level = 3.0dBm0 = 0dBm0 to 30dBm0 = – 40dBm0 XMT RCV = – 55dBm0 XMT RCV	33 36 29 30 14 15			dBC dBC dBC dBC dBC dBC
Single Frequency Distortion, Transmit	SFD_X				– 46	dB
Single Frequency Distortion, Receive	SFD_R				– 46	dB
Intermodulation Distortion	IMD	Loop around measurement, VF_X+ = – 4dBm0 to – 21dBm0, two frequencies in the range 300Hz – 3400Hz			– 41	dB
Crosstalk						
Transmit to Receive Crosstalk, 0dBm0 Transmit Level	CT_{X-R}	f = 300Hz – 3400Hz D_R = Steady PCM code		– 90	– 75	dB
Receive to Transmit Crosstalk, 0dBm0 Receive Level	CT_{R-X}	f = 300Hz – 3400Hz, VF_XI = 0V		– 90	– 70 (Note 1)	dB

Note 1. CT_{R-X} is measured with a – 40dBm0 activating signal applied at VF_XI+

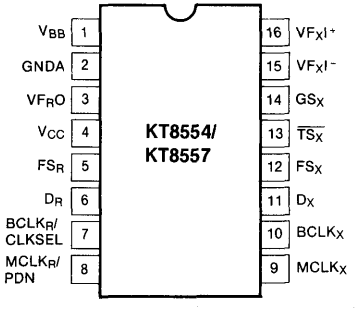
ENCODING FORMAT AT Dx OUTPUT

	μ-Law KT8554	A-Law KT8557
V_{IN} (at GS_X) = + Full – Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} (at GS_X) = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_{IN} (at GS_X) = – Full – Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

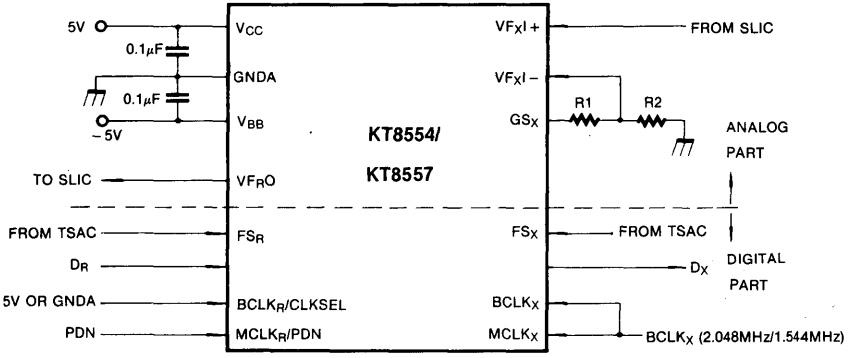
PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{BB}	Negative power supply. $V_{BB} = -5V \pm 5\%$.
2	GNDA	Analog ground. All signals are referenced to this pin.
3	VF_RO	Analog output of the receive filter.
4	V_{CC}	Positive power supply. $V_{CC} = +5V \pm 5\%$.
5	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8KHz pulse train.
6	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
7	$BCLK_R$/ CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. Many vary from 64KHz to 2.048MHz. Alternatively, may be a logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions.
8	$MCLK_R$/ PDN	Receive master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continously low, $MCLK_R$ is selected for all internal timing. When $MCLK_R$ is connected continuously high the device is powered down.
9	$MCLK_X$	Transmit master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_R$.
10	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$.
11	D_X	The TRI-STATE PCM data output which is enabled by FS_X.
12	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8KHz pulse train.
13	$\overline{TS_X}$	Open drain ouptut which pulses low during the encoder time slot.
14	GS_X	Analog output of the transmit input amplifier. Used to externally set again.
15	$V_{FXI}-$	Inverting input of the transmit input amplifier.
16	$V_{FXI}+$	Non-inverting input of the transmit input amplifier.

PIN CONNECTION



APPLICATION CIRCUITS

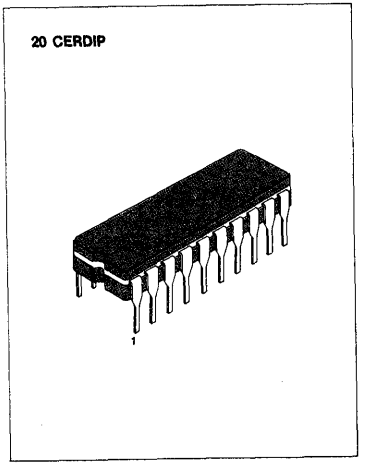


Note: XMIT gain $= 20 \times \log(\frac{R1+R2}{R2})$, $(R1+R2) > 10K\Omega$.

Fig. 4

TIME SLOT ASSIGNMENT CIRCUIT (TSAC)

The KT8555 is a per channel Time Slot Assignment Circuit (TSAC) that produces 8-bit receive and transmit time slots for 4 COMBO CODEC/Filters.
Each frame synchronization pulse may be independently assigned to a time slot in a frame of up to 64 time slots.



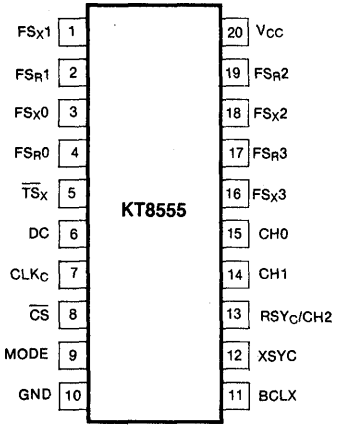
FEATURES

- **Single, 5V operation**
- **Low power consumption: 5mW**
- **Controls 4 COMBO CODEC/Filters**
- **Independent transmit and receive frame syncs and enables**
- **8 channel unidirectional mode**
- **Up to 64 time slots per frame**
- **Compatible with KT8554/7, KT8564/7, KT8520/1 CODECs**
- **TTL and CMOS compatible**

ORDERING INFORMATION

Device	Package	Operating Temperature
KT8555N	20 Plastic DIP	−20 ~ +125°C
KT8555J	20 Ceramic DIP	

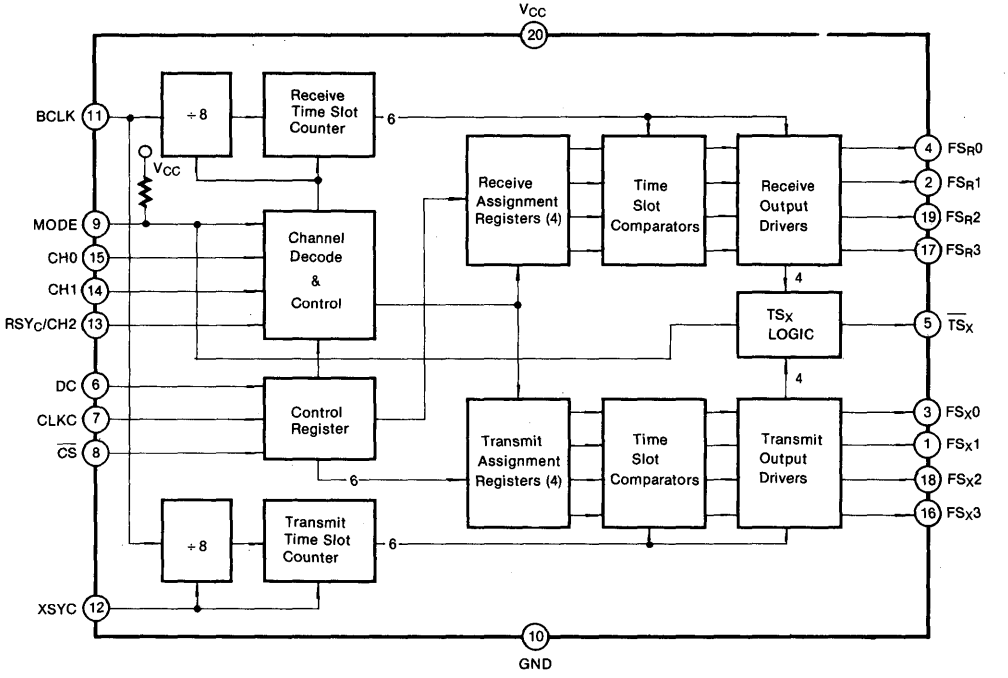
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Function
3 1 18 16	FS_X0 FS_X1 FS_X2 FS_X3	A frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid transmit time slot assignment is made.
4 2 19 17	FS_R0 FS_R1 FS_R2 FS_R3	A frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid receive time slot assignment is made.
5	$\overline{TS_X}$	This pin pulls low during any active transmit time slot. (N-channel open drain)
6	D_C	The input for an 8 bit serial control word. $\overline{X}$ is the first bit clocked in.
7	CLK_C	The clock input for the control interface.
8	$\overline{CS}$	The active-low chip select for the control interface.
9	MODE	Mode 1 = Open or V_{CC} Mode 2 = Gnd
10	GND	Ground
11	BCLK	The bit clock input
12	XSYC	The transmit TSO sync pulse input. Must be synchronous with BCLK.
13	RSY_C/CH2	This input function is determined by the MODE input (Pin 9). In mode 1 this input is the receive TSO sync pulse, RSY_C, which must be synchronous with BCLK. In mode 2 this is the CH2 input for the MSB of the channel select word.
14	CH1	The input for the NSB (next significant bit) of the channel select word.
15	CH0	The input for the LSB (last significant bit) of the channel select word, which defines the frame sync output affected by the following control word.
20	V_{CC}	Power supply pin. 5V ± 5%

BLOCK DIAGRAM



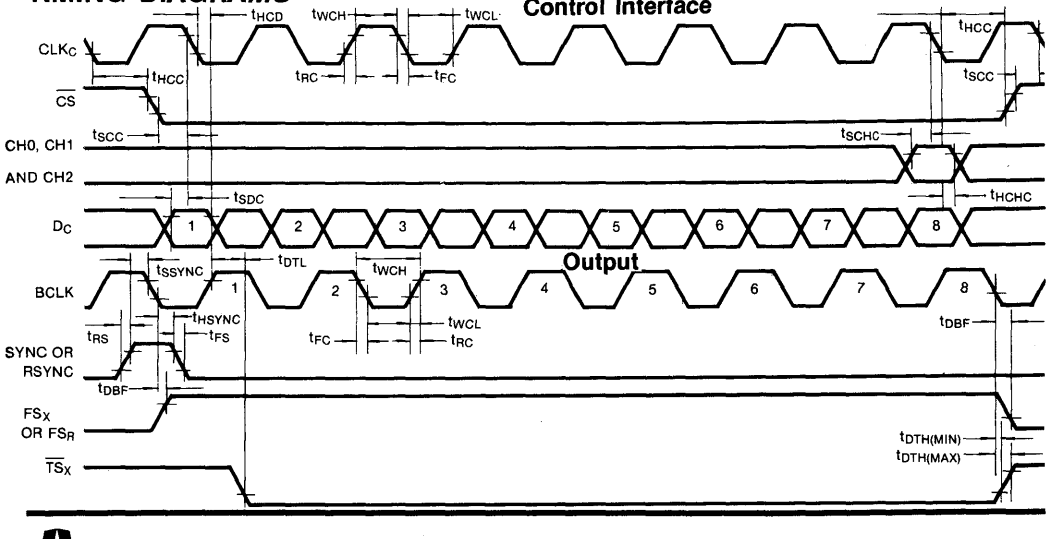
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
V_{CC} to GND	V_{CC}	7.0	V
Any Input Voltage	V_I	$V_{CC}+0.3 \sim -0.3$	V
Any Output Voltage	V_O	$V_{CC}+0.3 \sim -0.3$	V
Operating Temperature Range	Ta	$-25 \sim 125$	°C
Storage Temperature Range	T_{stg}	$-65 \sim 150$	°C
Lead Temperature (Soldering, 10 secs)	T_L	300	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted; $V_{CC}=5.0V\pm5\%$, $Ta=0°C\sim70°C$)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Current	I_{CC}	BCLK = 4.096MHz, All outputs open		1	1.5	mA
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.7	V
Input Current 1	I_{I1}	All Inputs Except Mode, $V_{IL}<V_{IN}<V_{IH}$	−1		1	μA
Input Current 2	I_{I2}	Mode, $V_{IN}=0V$	−100			μA
Output Voltage High	V_{OH}	FS_X and FS_R Ouputs, $I_{OH}=3mA$	2.4			V
Output Voltage Low	V_{OL}	FS_X and FS_R Outputs, $I_{OL}=3mA$			0.4	V
		TS_X output, $I_{OL}=3mA$			0.4	V
Rise and Fall Time of Clock	t_{RC}, t_{FC}	BCLK, CLKC			50	nS
Delay to $\overline{T_{SX}}$ Low	t_{DTL}	$C_L=50pF$			140	nS
Delay to $\overline{T_{SX}}$ High	t_{DTH}	$R_L=1K\Omega$ to V_{CC}	30		100	nS
Hold Time from BCLK to Frame Sync	t_{HS}		50			nS
Set-Up Time from Frame Sync to BLCK	t_{SS}		30			nS
Delay Time from BLCK Low to $S_{X/R}$ 0-3 High or Low	t_{DBF}	$C_L=50pF$			50	nS
Hold Time from Channel Select to CLKC	t_{HCH}		50			nS
Set-Up Time from Channel Select to CLKC	t_{SCH}		30			nS
Period of Clock	t_{PC}	BCLK, CLKC	240			nS
Width of Clock High	t_{WCH}	BCLK, CLKC	50			nS
Width of Clock Low	t_{WCL}	BCLK, CLKC	50			nS
Set-Up Time from D_C to CLKC	t_{SDC}		30			nS
Hold Time from CLKC to D_C	t_{HCD}		50			nS
Set-Up Time from CS to CLKC	t_{SCC}		30			nS
Hold Time from CLKC to CS	t_{HCC}		100			nS

TIMING DIAGRAMS



FUNCTION DESCRIPTION

Operating Modes

The KT8555 is a control interface which requires an 8 bit serial control word. The device is compatible with KT8520/KT8521 CODECs. Either one of the frame sync output group, FS_X0 to FS_X3 or FS_R0 to FS_R3, affected by the control word is defined by the two bits, $\overline{X}$ and $\overline{R}$. Time slot selected from 0 to 63 is specified. A frame sync output is highly active for one time slot which is equivalent to 8 cycles of BLCK. Up to 64 time slots are allowed to form a frame. There are two operational mode. In mode 1, each channel of transmit and receive direction has different time slot assigned. This mode can be selected by either leaving pin 9 (MODE) opened or connecting it with V_{CC}. In such a case, pin 13 is RSYNC input defining the start of each receive frame while four outputs, FS_R0 to FS_R3, are assigned with respect to RSYNC. On the other hand, start of each transmit frame is defined by XSYNC input by which output FS_X0 to FS_X3, are assigned. XSYNC and RSYNC can be phase related. Channels from 0-3 are selected by the input CH0 and CH1 (refer to the table 1). In mode 2, all 8 frame sync outputs can be assigned with respect to XSYNC input. The mode 2, selected by connecting pin 9 (MODE) to GND, enables the KT8555 TSAC suitable for an 8-channel undirectional controller and for a system where both transmit and receive direction of each channel have same time slot assigned. For instance, FS_X and FS_R input of COMBO CODEC/FILTER are hard wired together. The channel assigned has its channel selected by CH0, CH1 and CH2 (refer to table 2).

$\overline{X}$	$\overline{R}$	T5	T4	T3	T2	T1	T0

$\overline{X}$ is the first bit clocked into DC input

CONTROL DATA FORMAT

T5	T4	T3	T2	T1	T0	Time Slot
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
						.
						.
						.
0	1	1	1	1	0	30
0	1	1	1	1	1	31
1	0	0	0	0	0	32
1	0	0	0	0	1	33
						.
						.
						.
1	1	1	1	1	1	63

CH1	CH0	Channel Selected
0	0	Assign to FS_X0 and/or FS_R0
0	1	Assign to FS_X1 and/or FS_R1
1	0	Assign to FS_X2 and/or FS_R2
1	1	Assign to FS_X3 and/or FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to both selected FS_X and FS_R
0	1	Assign time slot to seleced FS_X only
1	0	Assign time slot to selected FS_R only
1	1	Disable both selected FS_X and FS_R

TABLE 1. CONTROL MODE 1

CH2	CH1	CH0	Channel Selected
0	0	0	Assign to FS_X0
0	0	1	Assign to FS_X1
0	1	0	Assign to FS_X2
0	1	1	Assign to FS_X3
1	0	0	Assign to FS_R0
1	0	1	Assign to FS_R1
1	1	0	Assign to FS_R2
1	1	1	Assign to FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to selected output
0	1	Assign time slot to selected output
1	0	Assign time slot to selected output
1	1	Disable selected output

TABLE 2. CONTROL MODE 2

3

Loading Control Data

While control data is loaded, the binary cord for the selected channel should be set on inputs CH0 and CH1 (and CH2 in mode 2). Please refer table 1 and table 2.
Control data is clocked into the DC input on the falling edges of CLKC with low $\overline{CS}$. A newly assigned time slot is transferred to the assignment register, selected on the high going of $\overline{CS}$, and it is re-synchronized to the system clock. As a result the newly generated FS output pulse will start at the next complete valid time slot after the rising edge of $\overline{CS}$.

Power Up Initialization

All frame sync outputs, FS_X0-FS_X3 and FS_R0-FS_R3, are inhibited and held low during power-up period. Therefore no output is active until a valid time slot is assigned.

Time Slot Counter Operation

As TSO of each transmit frame starts, defined by the first falling edge of BCLK after XSYNC goes high, the transmit time slot counter is reset to 000000. Then it starts increasing once every 8 cycles of BLCK. When a match is found by comparing each count with the 4 transmit assignment register, a frame sync pulse is generated at the FS_X output.
Like wise the start of the receive TSO is defined by the falling edge of BCLK after RSYNC goes high. The output, FS_R0-FS_R3, are generated with respect to TSO when the receive time counter is matched with an appropriate receive assignment register.

$\overline{TS}_X$ Output

In mode 1, where there are separate transmit and receive assignments, the output is pulled low of FS_X output pulse is detected. During the mode 2, the output is pulled low if either of FS_X or FS_R is generated. Other than such cases, it is an open circuit allowing $\overline{TS}_X$ outputs of TSACs to be wire-ANDed together with a common pull-up resistor. The output can control the TRI-STATE enable input of a line driver to buffer the transmit PCM bus provided from the CODEC/Filter to the backplane.

APPLICATION CIRCUIT

The KT8555 TSAC combined with any kind of COMBO from KT8554/7 or KT8564/7 series can obtain data timing as illustrated in Fig. 1. Even though FS_X output goes high before BCLK gets high, the D_X output of the combo remains in the TRI-STATE mode until both outputs are high. The eight bit period is shortened to avoid a bus clash as on the KT8520/1 CODECs.

Alternatively, full 8 bits can be obtained by inverting the BCLK to the combo devices, thereby rising edges of BLCK and $FS_{X/R}$ are aligned.

Fig. 2 is typical timing of the control data interface.

Fig. 3 is the digital interconnections of a typical line card application.

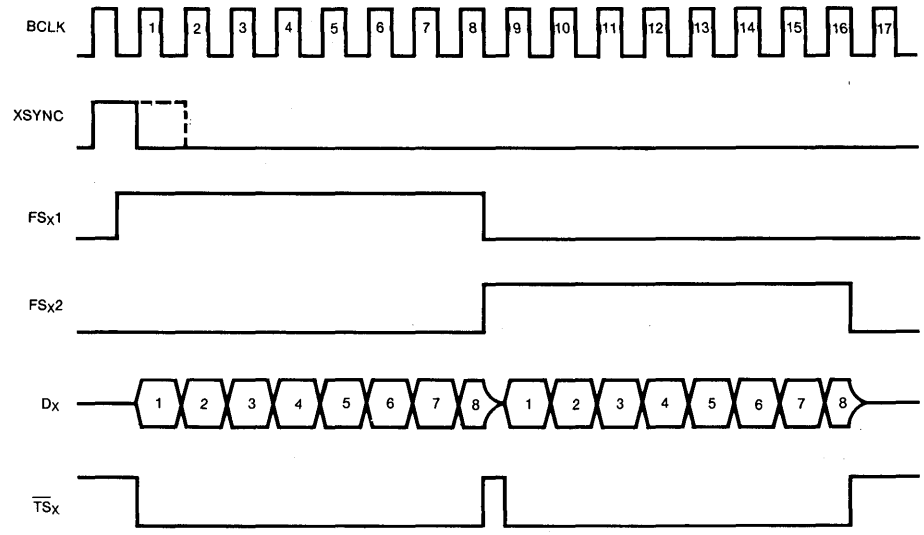


Fig. 1 Transmit Data Timing

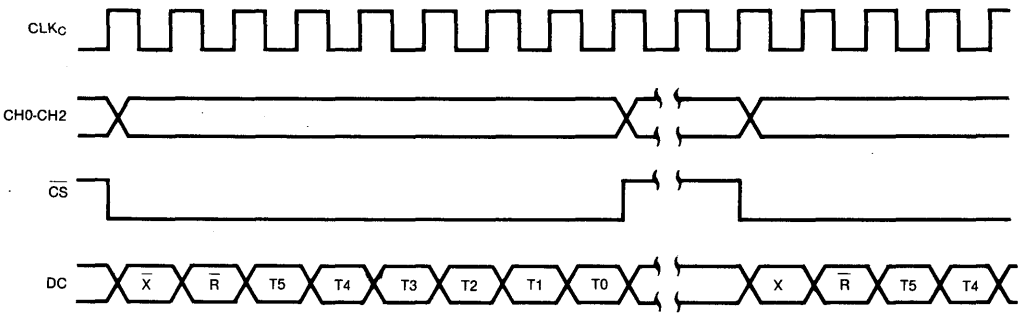


Fig. 2 Control Data Timing

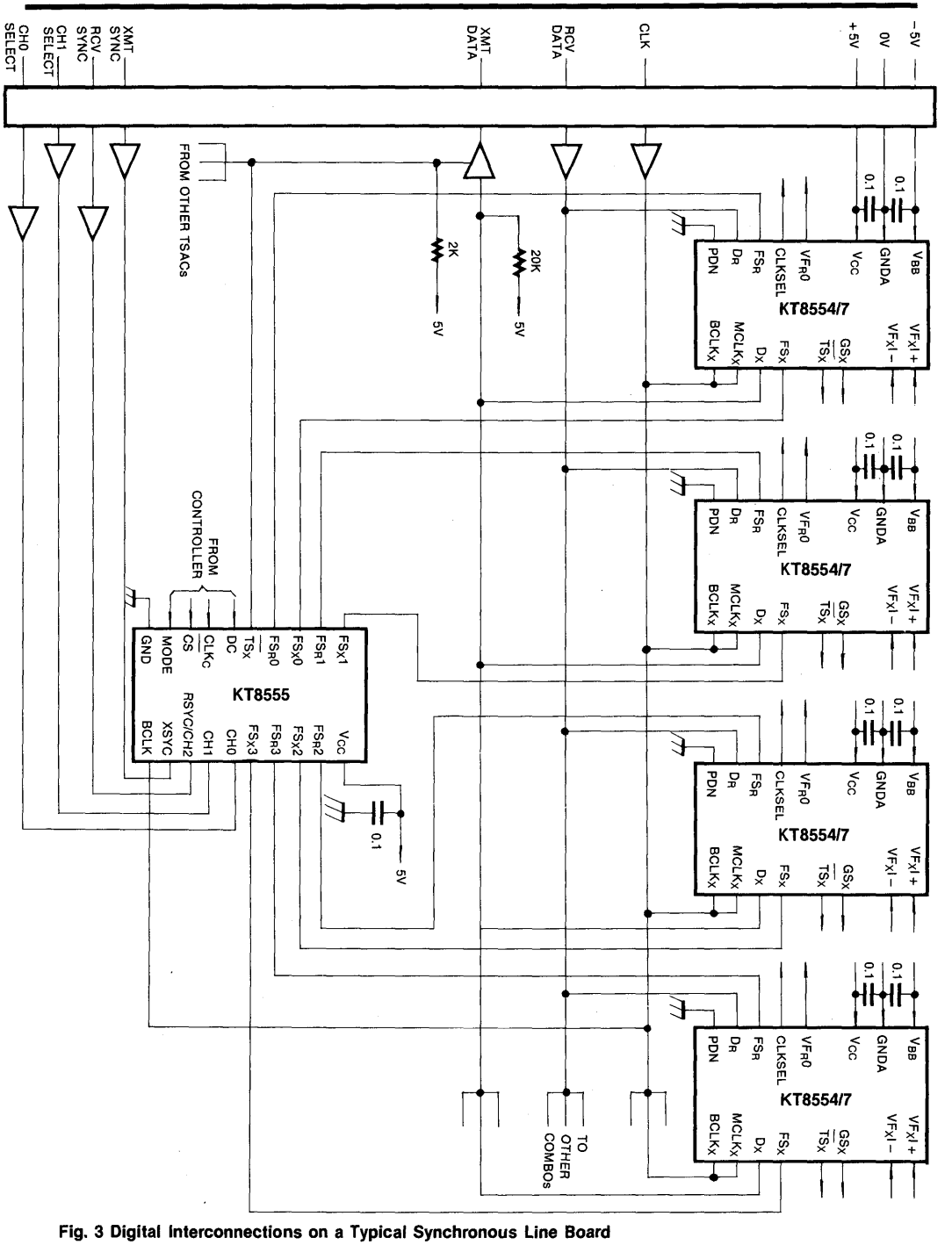
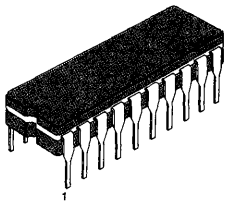


Fig. 3 Digital Interconnections on a Typical Synchronous Line Board

COMBO CODECS

The KT8564 and KT8567 are single-chip PCM encoders and decoders (PCM CODECs), PCM line filter and receive power amp.
These devices provide all the functions required to interface a full-duplex voice telephone circuit with a time-division-multiplexed (TDM) system.
These devices are designed to perform the transmit encoding and decoding as well as the transmit and receive filtering functions in PCM system.
They are intended to be used at the analog termination of a PCM line or trunk.
These devices provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signalling and supervision information.

20 CERDIP



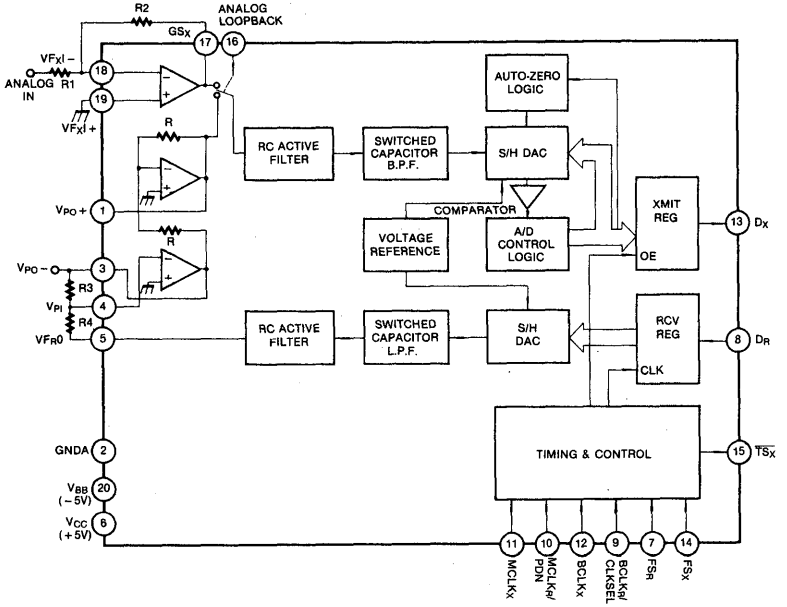
FEATURES

- **Complete CODEC and filtering system**
- **Meets or exceeds D3/D4 and CCITT specifications. μ-Law: KT8564 A-Law: KT8567**
- **On-chip auto zero, sample and hold and precision voltage references.**
- **Receive push-pull power amplifiers**
- **Low power dissipation: 70mW (operating) 3mW (standby)**
- **±5V operation**
- **TTL or CMOS compatible**
- **Automatic power down**

ORDERING INFORMATION

Device	Package	Operating Temperature
KT8564N	Plastic	−25 ~ +125°C
KT8567N	Plastic	
KT8564J	Ceramic	
KT8567J	Ceramic	

TYPICAL I-V CHARACTERISTICS



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
V_{CC} to GNDA	V_{CC}	7	V
V_{BB} to GNDA	V_{BB}	−7	V
Voltage at Any Analog Input or Output	I/O	$V_{CC}+0.3$ to $V_{BB}-0.3$	V
Voltage at Any Digital Input or Output	I/O	$V_{CC}+0.3$ to GNDA − 0.3	V
Operating Temperature Range	T_a	−25 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C
Lead Temperature (Soldering 10 secs)	T_L	300	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: $V_{CC}=5.0V\pm5\%$, $V_{BB}=-5V\pm5\%$, GNDA = 0V, Ta = 0°C to 70°C; typical characteristics specified at $V_{CC}=5.0V$, Ta = 25°C; all signals are referenced to GNDA)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Power Dissipation						
Active Current	$I_{CC}1$	Power amplifiers active, VPI = 0V		7.0	10.0	mA
Active Current	$I_{BB}1$	Power amplifiers active, VPI = 0V		7.0	10.0	mA
Power-Down Current	I_{CCO}			0.5	1.5	mA
Power-Down Current	I_{BBO}			0.05	0.3	mA
Digital Interface						
Input Low Current	I_{IL}	$GNDA\leq V_{IN}\leq V_{IL}$, All digital inputs	−10		10	μA
Input High Current	I_{IH}	$V_{IH}\leq V_{IN}\leq V_{CC}$	−10		10	μA
Output Current in High Impedance State (TRI-STATE)	I_{OZ}	D_X, $GNDA\leq V_O\leq V_{CC}$	−10		10	μA
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2.2			V
Output Low Voltage	V_{OL}	D_X, $I_L=3.2mA$ SIG_R, $I_L=1.0mA$ $\overline{TS_X}$, $I_L=3.2mA$, Open Drain			0.4 0.4 0.4	V
Output High Voltage	V_{OH}	D_X, $I_H=-3.2mA$ SIG_R, $I_H=-1.0mA$	2.4 2.4			V
Analog Interface with Transmit Input Amplifier						
Input Leakage Current	I_IXA	$-2.5V\leq V\leq+2.5V$, VF_XI+ or VF_XI-	−200		200	nA
Input Resistance	R_IXA	$-2.5V\leq V\leq+2.5V$, VF_XI+ or VF_XI-	10			MΩ
Output Resistance	R_OXA	Closed loop, unity gain		1	3	Ω
Load Resistance	R_LXA	GS_X	10			KΩ
Load Capacitance	C_LXA	GS_X			50	pF
Output Dynamic Range	V_OXA	GS_X, $R_L\geq10K\Omega$	±2.8			V

ELECTRICAL CHARACTERISTICS (Continued)

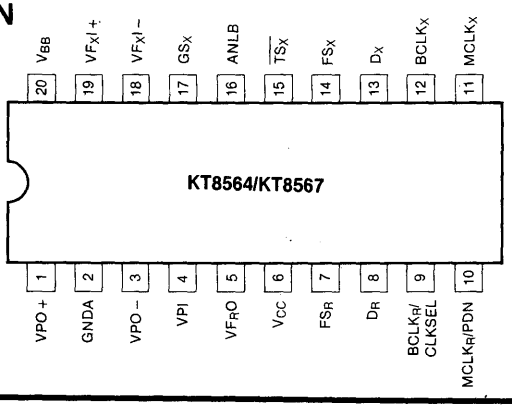
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Gain	A_VXA	VF_XI+ to GS_X	5000			V/V
Unity-Gain Bandwidth	F_UXA		1	2		MHz
Offset Voltage	$V_{OS}XA$		−20		20	mV
Common-Mode Voltage	$V_{CM}XA$	CMRRXA>60dB	−2.5		2.5	V
Common-Mode Rejection Ratio	CMRRXA	DC Test	60			dB
Power Supply Rejection Ratio	PSRRXA	DC Test	60			dB
Analog Interface with Receive Filter						
Output Resistance	R_ORF	Pin VF_RO		1	3	Ω
Output DC Offset Voltage	VOS_RO	Measure from VF_RO to GND A	−200		200	mV
Load Resistance	R_LRF	$VF_RO = \pm 2.5V$	10			KΩ
Load Capacitance	C_LRF	Connect from VF_RO to GND A			25	pF
Analog Interface with Power Amplifiers						
Input Leakage Current	IPI	$-1.0V \leq VPI \leq 1.0V \leq VPI \leq 1.0V$	−100		100	nA
Input Resistance	RIPI	$-1.0V \leq VPI \leq 1.0V$	10			MΩ
Input Offset Voltage	VI_{OS}		−25		25	mV
Output Resistance	ROP	Inverting unity gain at VPO+ or VPO−		1		Ω
Unity-Gain Bandwidth	F_C	Open loop (VPO−)		400		KHz
Load Capacitance	C_{LP}	$R_L \geq 1500\Omega$ VPO+ or $R_L = 600\Omega$ VPO− to $R_L = 300\Omega$ GNDA			100 500 1000	pF pF pF
Gain from VPO− to VPO+	GA_P+	$R_L = 300\Omega$ VPO+ to GNDA level at VPO− = −1.77Vrms (+3dBmo)		−1		V/V
Power Supply Rejection of V_{CC} or V_{BB}	$PSRR_P$	VPO− connected to VPI 0KHz−4KHz 0KHz−50KHz	 60 36			 dB dB
Frequency of Master Clock	I/t_{PM}	Depends on the device used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160			ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160			ns
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$			50	ns
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$			50	ns
Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First bit clock after the leading edge of FS_X	100			ns
Period of Bit Clock	t_{PB}		485	488	15,725	ns
Width of Bit Clock High	t_{WBH}	$V_{IH} = 2.2V$	160			ns
Width of Bit Clock Low	t_{WBL}	$V_{IL} = 0.6V$	160			ns
Rise Time of Bit Clock	t_{RB}	$t_{PB} = 480ns$			50	ns
Fall Time of Bit Clock	t_{FB}	$t_{PB} = 488ns$			50	ns

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Holding Time from Bit Clock Low to Frame Sync	t_{HBF}	Long frame only	0			ns
Holding Time from Bit Clock High to Frame Sync	t_{HOLD}	Short frame only	0			ns
Set-Up Time for Frame Sync to Bit Clock Low	t_{SFB}	Long Frame Only	80			ns
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load = 150pF plus 2 LSTTL loads	0		180	ns
Delay Time to $\overline{TS_X}$ Low	t_{XDP}	Load = 150pF plus 2 LSTTL loads			140	ns
Delay Time from $BCLK_X$ Low to Data Output Disabled	t_{DEC}		50		165	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, whichever Comes Later	t_{DZF}	C_L = 0pF to 150pF	20		165	ns
Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low	t_{SDB}		50			ns
Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	t_{HBD}		50			ns
Delay Time from $BCLK_{R/X}$ Low to SIG_R Valid	t_{DFSSF}	Load = 50pF plus 2 LSTTL loads			300	ns
Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	t_{SF}	Short frame sync pulse (1 or 2 bit clock periods long)(Note 1)	50			ns
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	t_{HF}	Short frame sync pulse (1 or 2 bit clock periods long)(Note 1)	100			ns
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X of FS_R)	t_{HBFI}	Long frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K bit/s operating mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

PIN CONFIGURATION



TIMING DIAGRAM

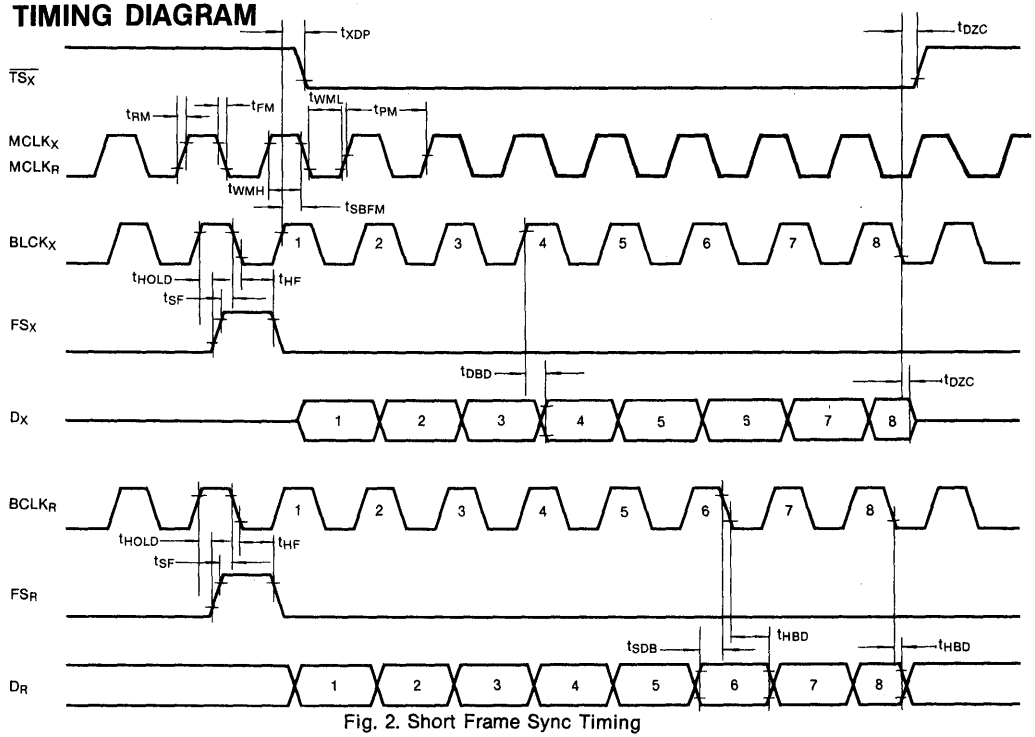


Fig. 2. Short Frame Sync Timing

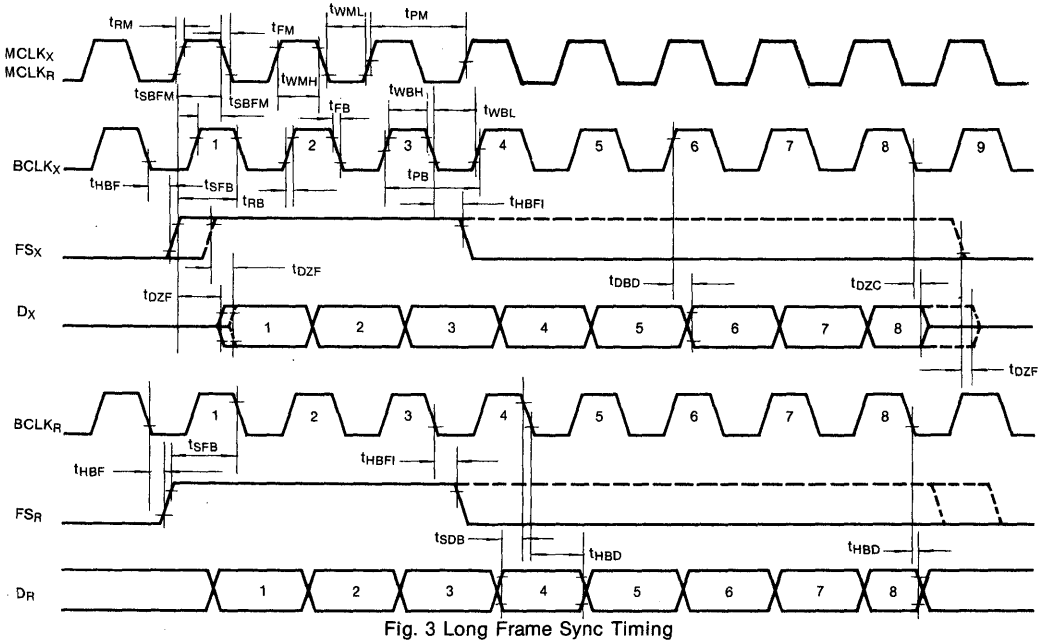


Fig. 3 Long Frame Sync Timing

PIN DESCRIPTION

Pin	Name	Function
1	VPO^+	The non-inverted output of the receive power amplifier.
2	GNDA	Analog ground. All signals are referenced to this pin.
3	VPO^-	The inverted output of the receive power amplifier.
4	VPI	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}.
5	VF_RO	Analog output of the receive filter.
6	V_{CC}	Positive power supply pin $V_{CC} = +5V \pm 5\%$.
7	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R, FS_R is an 8KHz pulse train. (refer to Fig 2 and 3 for timing details)
8	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
9	$BCLK_R$/ CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64KHz to 2.048MHz. Alternatively, may be a logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions. (see Table 1)
10	$MCLK_R$/ PDN	Receive master clock. Must be 1.536MHz or 2.048MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
11	$MCLK_X$	Transmit master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_R$.
12	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$.
13	D_X	The TRI-STATE PCM data output which is enabled by FS_X.
14	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data a on D_X, FS_X is an 8KHz pulse train. (refer to Fig 2, 3)
15	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
16	ANLB	Analog loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is dis connected from the output of the preamplifier and connected to the VPO^+ output of the receive power, amplifier.
17	GS_X	Analog output of the transmit input amplifier. Used to externally set again.
18	VF_XI^-	Inverting input of the transmit input amplifier.
19	VF_XI^+	Non-inverting input of the transmit input amplifier.
20	V_{BB}	Negative power supply pin $V_{BB} = -5V \pm 5\%$.

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, GNDA = 0V, f = 1.02KHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
AMPLITUDE RESPONSE						
Receive Gain, Absolute	G_{RA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input = Digital code sequence for 0dBm0 signal at 1020Hz	−0.15		0.15	dB
Receive Gain, Relative to G_{RA}	G_{RR}	f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
Absolute Receive Gain Variation with Temperature	G_{RAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Receive Gain Variation with Supply Voltage	G_{RAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Receive Gain Variations with Level	G_{RRL}	Sinusoidal test method; reference input PCM code corresponds to an Ideally encoded − 10dBm0 signal PCM level = −40dBm0 to +3dBm0 PCM level = −50dBm0 to −40dBm0 PCM level = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
Receive Filter Output at VF_RO	V_{RO}	R_L = 10Ω	−2.5		2.5	V
Absolute Levels	A_L	Nominal 0dBm0 level is 4dBm (600Ω) 0dBm0		1.2276		V_{rms}
Max Transmit Overload Level	t_{MAX}	Max transmit overload level KT8564(3.17dBm0), KT8567(3.14dBm0)		2.501 2.492		V_{PK}
Transmit Gain, Absolute	G_{XA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input at GS_X = 0dBm0 at 1020Hz	−0.15		0.15	dB
Transmit Gain, Relative to G_{XA}	G_{XR}	f = 16Hz f = 50Hz f = 60Hz f = 200Hz f = 300Hz − 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure Response from 0Hz to 4000Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
Absolute Transmit Gain Variation with Temperature	G_{XAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Transmit Gain Variation with Supply Voltage	G_{XAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Transmit Gain Variations with Level	G_{XRL}	Sinusoidal test method Reference level = −10dBm0 VF_XI+ = −40dBm0 to +3dBm0 VF_XI+ = −50dBm0 to −40dBm0 VF_XI+ = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
Transmit Delay, Absolute	D_{XA}	f = 1600Hz		290	315	μs
Transmit Delay, Relative to D_{XA}	D_{XR}	f = 500Hz – 600Hz f = 600Hz – 800Hz f = 800Hz – 1000Hz f = 1000Hz – 1600Hz f = 1600Hz – 2600Hz f = 2600Hz – 2800Hz f = 2800Hz – 3000Hz		195 120 50 20 55 80 130	220 145 75 40 75 105 155	μs μs μs μs μs μs μs
Receive Delay, Absolute	D_{RA}	f = 1600Hz		180	200	μs
Receive Delay, Relative to D_{RA}	D_{RR}	f = 500Hz – 1000Hz f = 1000Hz – 1600Hz f = 1600Hz – 2600Hz f = 2600Hz – 2800Hz f = 2800Hz – 3000Hz	– 40 – 30	– 25 – 20 70 100 145	 90 125 175	μs μs μs μs μs
NOISE						
Transmit Noise, C Message Weighted	N_{XC}	$VF_XI+ = 0V$, KT8564		12	15	dBrnc0
Transmit Noise, P Message Weighted	N_{XP}	$VF_XI+ = 0V$, KT8567		– 74	– 67	dBm0p
Receive Noise, C Message Weighted	N_{RC}	PCM code equals alternating positive and negative zero, KT8564		8	11	dBrnc0
Receive Noise, P Message Weighted	N_{RP}	PCM code equals positive zero, KT8567		– 82	– 79	dBm0p
Noise, Single Frequency	N_{RS}	f = 0KHz to 100KHz, loop around measurement, $VF_XI+ = 0V_{rms}$			– 53	dBm0
Positive Power Supply Rejection, Transmit	$PPSR_X$	$VF_XI+ = 0V_{rms}$, $V_{CC} = 5.0V_{DC} + 100mV_{rms}$ f = 0KHz – 50KHz	40			dBC
Negative Power Supply Rejection, Transmit	$NPSR_X$	$VF_XI+ = 0V_{rms}$, $V_{BB} = -5.0V_{DC} + 100mV_{rms}$ f = 0KHz – 50KHz	40			dBC
Positive Power Supply Rejection, Receive	$PPSR_R$	PCM code equals positive zero $V_{CC} = 5.0V_{DC} + 100mV_{rms}$ f = 0Hz – 4000Hz f = 4KHz – 25KHz f = 25KHz – 50KHz	 40 40 36			 dBC dB dB
Negative Power Supply Rejection, Receive	$NPSR_R$	PCM code equals positive zero $V_{BB} = -5.0V_{DC} + 100mV_{rms}$ f = 0Hz – 4000Hz f = 4KHz – 25KHz f = 25KHz – 50KHz	 40 40 36			 dBC dB dB

3

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious Out-of-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0, 300Hz – 3400Hz input applied to VF_XI+, measure individual image signals at VF_RO 4600Hz – 7600Hz 7600Hz – 8400Hz 8400Hz – 100,000Hz			 – 32 – 40 – 32	 dB dB dB
Distortion						
Signal to Total Distortion	STD_X	Sinusoidal test method				
Transmit or Receive Half-Channel	STD_R	Level = 3.0dBm0 = 0dBm0 to 30dBm0 = – 40dBm0 XMT RCV = – 55dBm0 XMT RCV	33 36 29 30 14 15			dBC dBC dBC dBC dBC dBC
Single Frequency Distortion, Transmit	SFD_X				– 46	dB
Single Frequency Distortion, Receive	SFD_R				– 46	dB
Intermodulation Distortion	IMD	Loop around measurement, VF_X+ = – 4dBm0 to – 21dBm0, two frequencies in the range 300Hz – 3400Hz			– 41	dB
Crosstalk						
Transmit to Receive Crosstalk	CT_{X-R}	f = 300Hz – 3400Hz D_R = Steady PCM code		– 90	– 75	dB
Receive to Transmit Crosstalk	CT_{R-X}	f = 300Hz – 3000Hz, VF_XI = 0V		– 90	– 70 (Note 1)	dB
Power Amplifiers						
Maximum 0dBm0 Level for Better than ± 0.1dB Linearity Over the Range – 10dBm0 to + 3dBm0	V_{OL}	Balanced load, R_L connected between VPO+ and VPO– R_L = 600Ω R_L = 1200Ω R_L = 30KΩ	 3.3 3.5 4.0			 Vrms Vrms Vrms
Signal/Distortion	S/Dp	R_L = 600Ω, 0dBm0	50			dB

Note 1. CT_{R-X} is measured with a – 50dBm0 activating signal applied at VF_XI+.

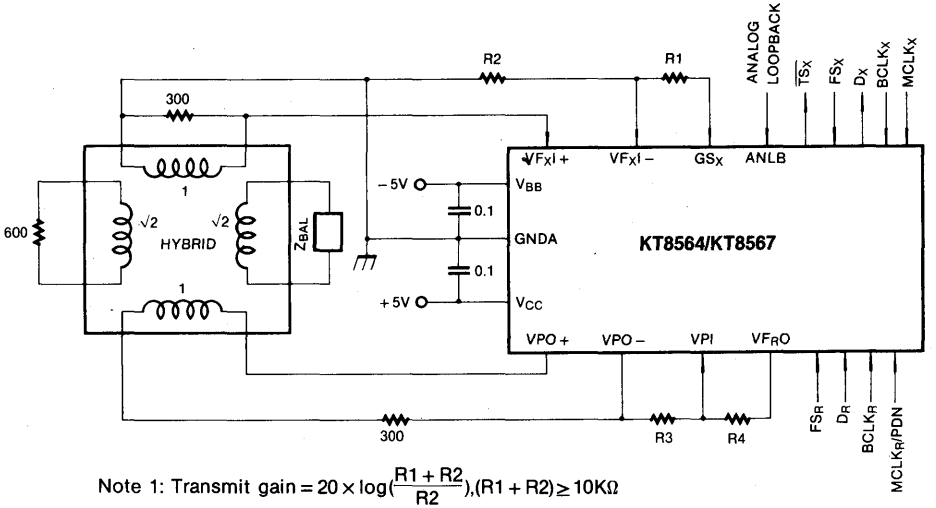
SELECTION OF MASTER CLOCK FREQUENCIES

$BCLK_R$/CLKSEL	MASTER CLOCK FREQUENCY SELECTED	
	KT8564	KT8567
Clocked	1.536MHz or 1.544MHz	2.048MHz
0	2.048MHz	1.536MHz or 1.544MHz
1 (or open circuit)	1.544MHz	2.048MHz

ENCODING FORMAT AT Dx OUTPUT

	KT8564 (μ-Law)	KT8567 (A-Law, Includes Even Bit Inversion)
V_{IN} = + Full Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_{IN} = – Full Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

APPLICATION CIRCUIT

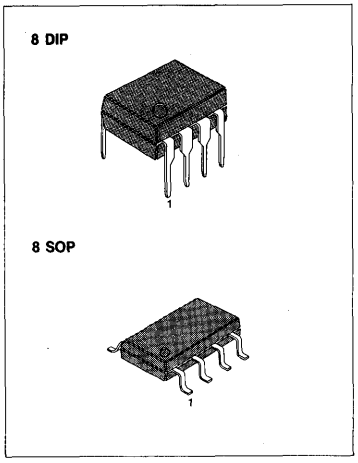


Note 1: Transmit gain $= 20 \times \log(\frac{R1 + R2}{R2})$, $(R1 + R2) \geq 10K\Omega$

Note 2: Receive gain $= 20 \times \log(\frac{2 \times R3}{R4})$, $R4 \geq 10K\Omega$

TONE DECODER

The LM567C is a monolithic phase locked loop system designed to provide a saturated transistor switch to GND, when an input signal is present within the passband. External components are used to independently set center frequency bandwidth and output delay.



FEATURES

- **Wide frequency range (0.01Hz — 500kHz).**
- **Bandwidth adjustable from 0 to 14%**
- **Logic compatible output with 100mA current sinking capability.**
- **Inherent immunity to false signals.**
- **High rejection of out-of-band signals and noise.**
- **Frequency range adjustable over 20:1 range by an external resistor.**

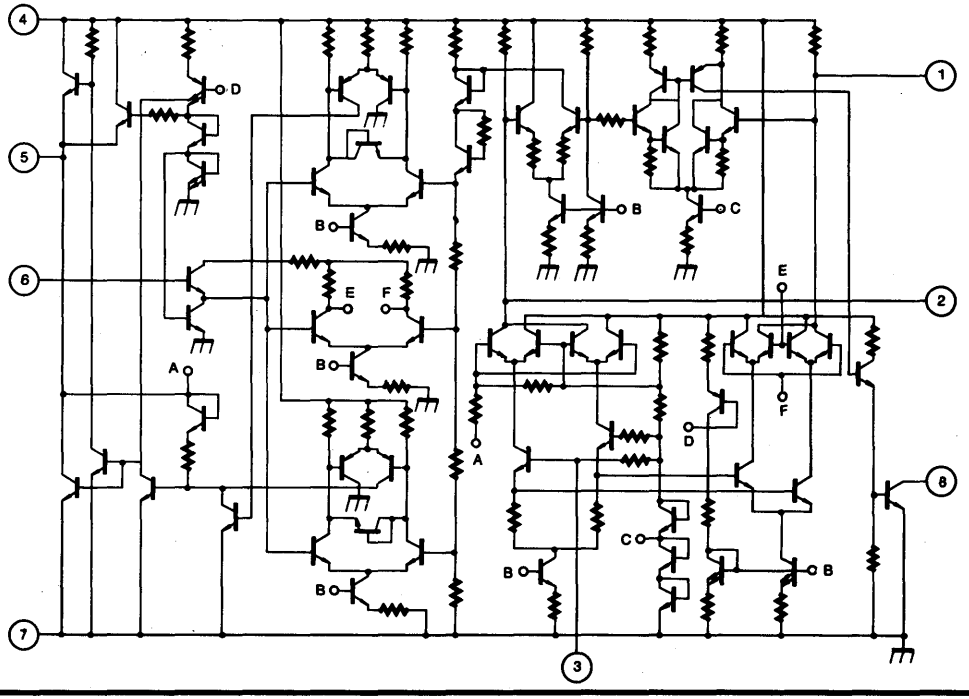
APPLICATIONS

- Touch Tone Decoder
- Wireless Intercom.
- Communications paging decoders
- Frequency monitoring and control.
- Ultrasonic controls (remote TV etc.)
- Carrier current remote controls.
- Precision oscillator.

ORDERING INFORMATION

Device	Package	Operating Temperature
LM567CN	8 DIP	0 ~ +70°C
LM567CD	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{CC}	10	V
Input Voltage	V_{IN}	−10 ~ V_{CC} +0.5	V
Output Voltage	V_O	15	V
Power Dissipation	Pd	300	mW
Operating Temperature	Topr	0 ~ +70	°C
Storage Temperature	Tstg	−65 ~ +150	°C

3

ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V, T_a=25°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage Range	V_{CC}		4.75	5.0	9.0	V
Supply Current Quiescent	I_{CC}-1	R_L=20K		7	10	mA
Supply Current Activated	I_{CC}-2			12	15	mA
Quiescent Power Dissipation	P_{QD}			35		mW
Highest Center Frequency	H_{FO}	R_L=20K	100	500		KHz
Center Frequency Stability	F_{SE}	0°C to 70°C		±60		ppm/°C
Center Frequency Shift With Supply Voltage	F_{CS}			0.7	2	%/V
Largest Detection Bandwidth	B.W		10	14	18	% of fo
Largest Detection B.W Skew	B.Ws			2	3	% of fo
Largest Detection Bandwidth Variation With Supply Voltage	B.Wv			±2	±5	%/V
Largest Detection Bandwidth Variation With Temperature	B.Wt			±0.1		%/°C
Input Resistance	R_{IN}			20		Kohm
Smallest Detectable Input Voltage	V_{IN}-1	I_L=100mA, fi=fo		20	25	mVrms
Largest No Output Input Voltage	V_{IN}-2		10	15		mVrms
Greatest Simultaneous Outband Signal To Inband Signal Ratio	S1/Sd	R_L=20k V_{IN}=300mV_{RMS} fi=fo=100KHz		+6		dB
Minimum Input Signal to Wideband Noise Ratio	S2/Sd	fi_1=140KHz fi_2=60KHz		−6		dB
Fastest On-Off Cycling Rate	F_{OUT}	R_L=20K		fo/20		
Output Leakage Current	I_{CO}	V_{IN}=25mV_{RMS}		0.01	25	μA
Output Saturaton Voltage	V_{SAT}-1	I_L=30mA, V_{IN}=25mVrms		0.2	0.4	V
	V_{SAT}-2	I_L=100mA, V_{IN}=25mVrms		0.6	1.0	V
Output Fall Time	T_F	R_L=50		30		nS
Output Rise Time	T_R	R_L=50		150		nS

CIRCUIT DESCRIPTION

The LM567C monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection on in-band signals. The device has a normally high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500 kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in-band signal triggers the device.

BLOCK DIAGRAM

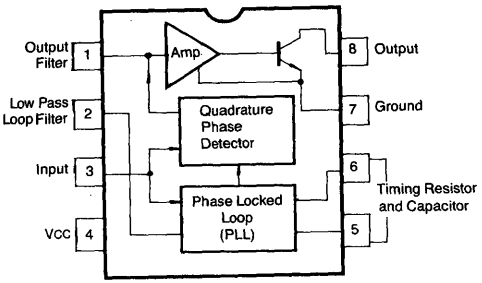


Fig. 1

DEFINITION OF LM567C PARAMETERS

CENTER FREQUENCY f_O

f_O is the free-running frequency of the C_L controlled oscillator with no input signal. It is determined by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground f_O can be approximated by

$$f_O \approx \frac{1}{R_1 C_1}$$

where R_1 is in ohms and C_1 is in farads.

LARGEST DETECTION BANDWIDTH

The largest detection bandwidth is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

DETECTION BANDWIDTH (BW)

The detection bandwidth is the frequency range centered about f_O, within which an input signal larger than the threshold voltage (typically 20mVrms) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass bandwidth filter. The bandwidth of the filter, as a percent of f_O, can be determined by the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_O C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance at pin 2 in μF.

DETECTION BAND SKEW

The detection band skew is a measure of how accurately the largest detection band is centered about the center frequency, f_O. It is defined as $(f_{max} + f_{min} - 2f_O)/f_O$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment.

PIN DESCRIPTION

OUTPUT FILTER — C_3 (Pin 1)

Capacitor C_3 connected from pin 1 to ground forms a simple low-pass post detection filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3 (4.7kΩ) is the internal impedance at pin 1.

The precise value of C_3 is not entical for most applications. To eliminate the possibility of false triggering by spurious signals, it is recommended that C_3 be $\geq 2\ C_2$, where C_2 is the loop filter capacitance at pin 2.

If the value of C_3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C_3 is too small, the beat rate at the output of the quadrature detector may cause a false logic level change at the output. (Pin 8)

The average voltage (during lock) at pin 1 is a function of the inband input amplitude in accordance with the given transfer characteristic.

LOOP FILTER — C_2 (Pin 2)

Capacitor C_2 connected from pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the LM567C The filter time constant is given by $T_2 = R_2C_2$, where R_2 (10 kΩ) is the impedance at pin 2.

The selection of C_2 is determined by the detection bandwidth requirements. For additional information see section on "Definition of LM567C Parameters".

The voltage at pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 to 1.05 f_O, with a slope of approximately 20 mV/% frequency deviation.

INPUT (Pin 3)

The input signal is applied to pin 3 through a coupling capacitor. This terminal is internally biased at a dc level 2 volts above ground, and has an input impedance level of approximately 20 kΩ

TIMING RESISTOR R_1 AND CAPACITOR C_1 (Pins 5 and 6)

The center frequency of the decoder is set by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground, as shown in Figure 3.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately V_{CC} — 1.4V and an average dc level of $V_{CC}/2$. A 1 kΩ load may be driven from this point. The voltage at pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to pin 6 avoid disturbing the temperature stability or duty cycle of the oscillator.

LOGIC OUTPUT (Pin 8)

Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, "base-collector" power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from pin 8 to the positive supply.

When an in-band signal is present, the output transistor at pin 8 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ $\leq$ 20 volts.

OPERATING INSTRUCTIONS

SELECTION OF EXTERNAL COMPONENTS

A typical connection diagram for the LM567C is shown in Figure 3. For most applications, the following procedure will be sufficient for determination of the external components R_1, C_1, C_2, and C_3.

1. R_1 and C_1 should be selected for the desired center frequency by the expression $f_O = 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that 2kΩ, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.
2. Low-pass capacitor, C_2, can be determined from the Bandwidth versus Input Signal Amplitude graph of Figure 7. One approach is to select an area of operation from the graph, and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_OC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires $V_i > 200$mV rms. Then, as noted on the graph, bandwidth will be controlled solely by the f_OC_2 product.
3. Capacitor C_3 sets the band edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminales spurious outputs. If C_3 is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. a typical minimum value of C_3 is 2 C_2.

Conversely, if C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C_3 passes the threshold value.

PRINCIPLE OF OPERATION

The LM567C is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. the system is comprised of a phase-locked loop, a quadrature AM detector, a voltage comparator, and an output logic driver. The four sections are internally interconnected as shown in Figure 1.

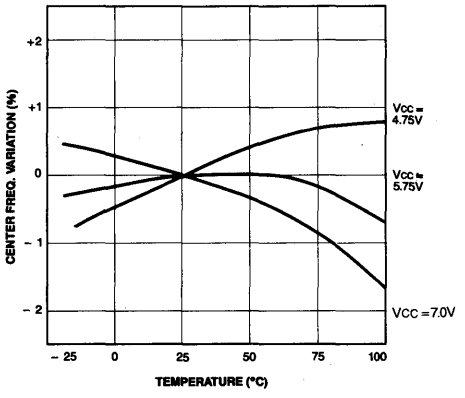
When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the dc voltage at the output of the detector is shifted. This dc level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic driver is a "bare collector" transistor stage capable of switching 100 mA loads.

The logic output at pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at pin 8 goes to a "low" state.

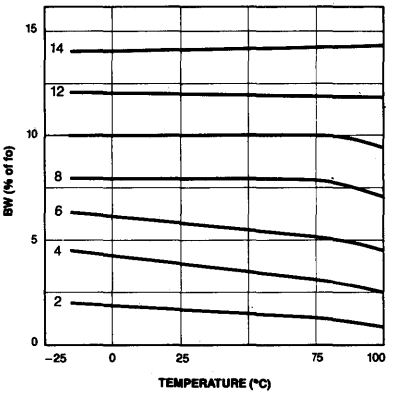
The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_O, is determined by the selection of R_1 and C_1 connected to pins 5 and 6, as shown in Figure 3. The detection bandwidth is determined by the size of the PLL filter capacitor, C_2; and the output response speed is controlled by the output filter capacitor, C_3

TYPICAL CHARACTERISTICS

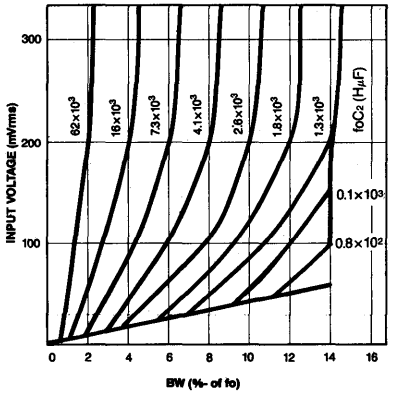
CENTER FREQ. VS TEMPERATURE



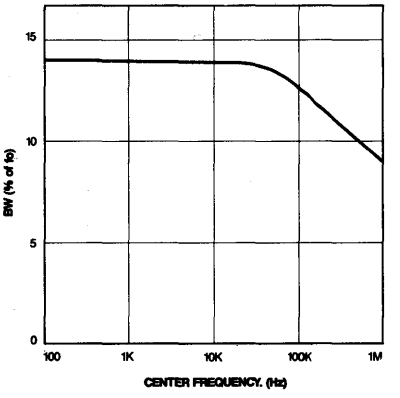
TYP. BW VS TEMPERATURE



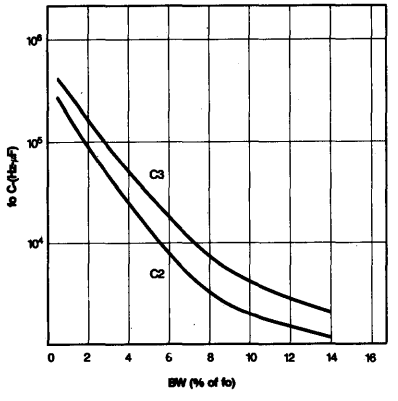
BW VS INPUT VOLTAGE.



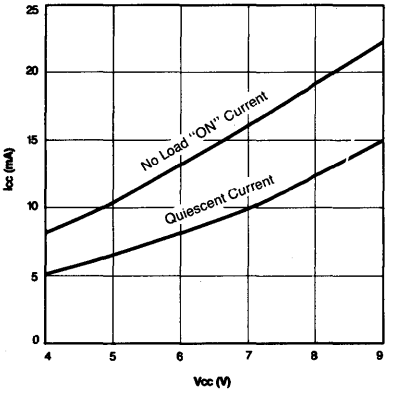
BW VS CENTER FREQUENCY



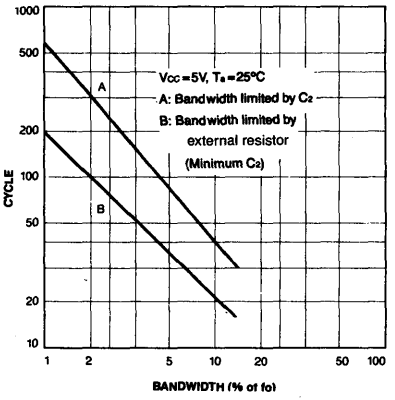
BW (C2, C3 CHARCT.)



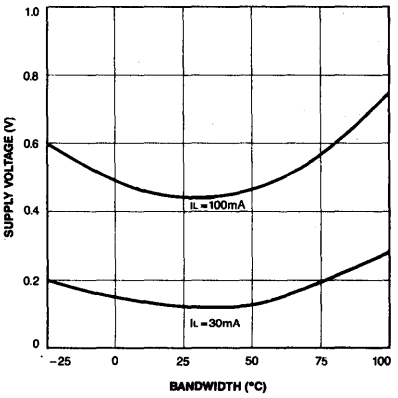
CURRENT DRAIN VS. VCC



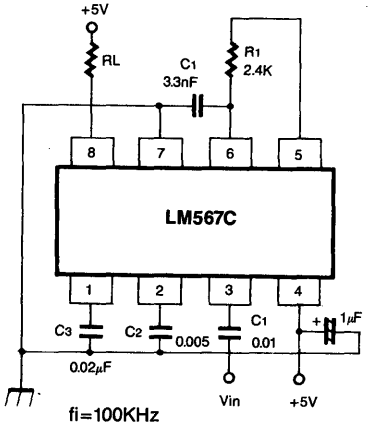
OPERATING CYCLE VS BANDWIDTH



OUTPUT SATURATION VOLTAGE VS AMBIENT TEMPERATURE



AC TEST CIRCUIT



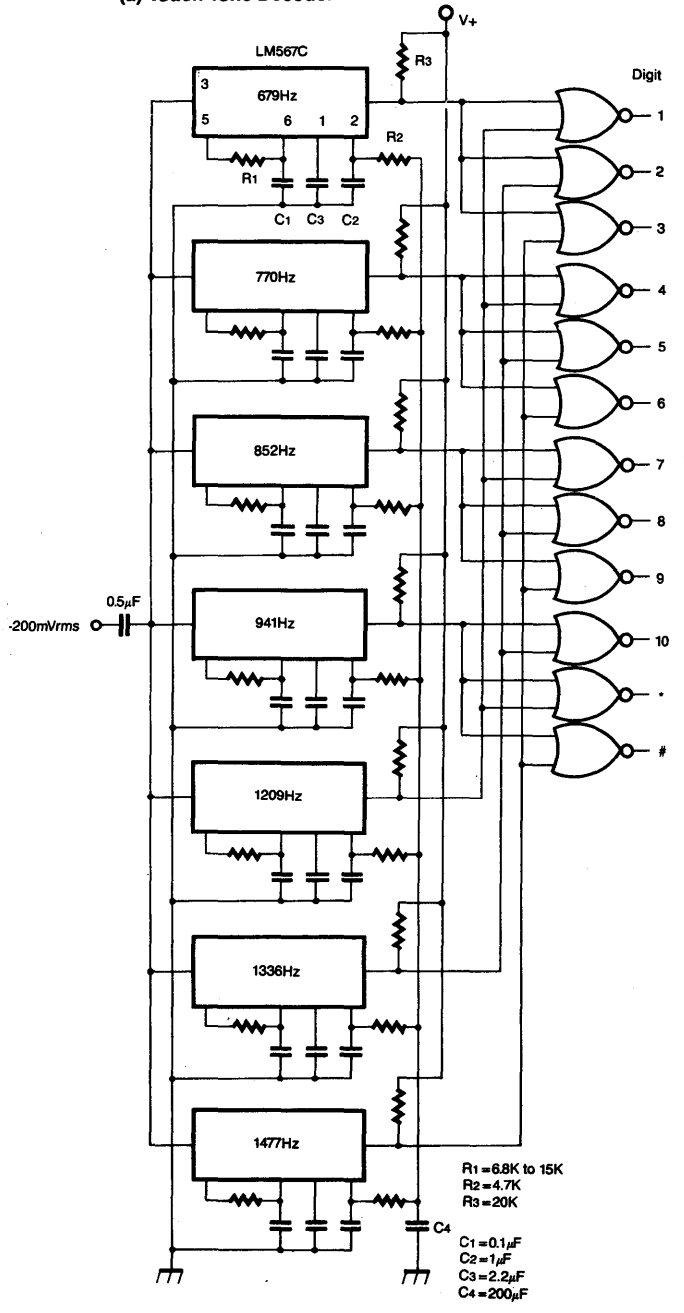
fi=100KHz

Note: Adjust for fo=100KHz

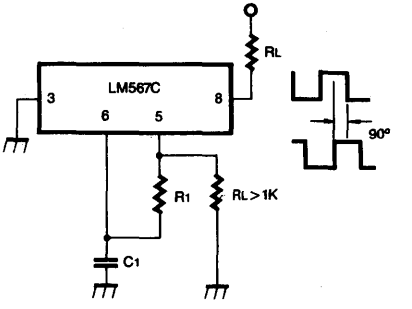
Fig. 2

APPLICATION CIRCUIT

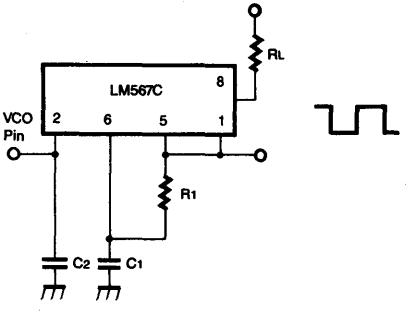
(a) Touch Tone Decoder



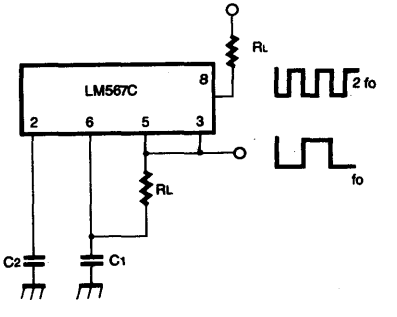
(b) 2-Phase Oscillator



(c) Variable Oscillator



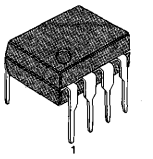
(d) Frequency Doubler



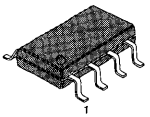
MICROPOWER TONE DECODER

The LM567L is a micropower phase-locked loop (PLL) circuit designed for general purpose tone and frequency decoding. In applications requiring very low power dissipation, the LM567L can replace the popular 567 type decoder with only minor component value changes. The LM567L offers approximately 1/10th the power dissipation of the conventional 567 type tone decoder, without sacrificing its key features such as the oscillator stability, frequency selectivity, and detection threshold. Typical quiescent power dissipation is less than 4mW at 5 volts.

8 DIP



8 SOP



FEATURES

- **Very low power dissipation (4mW at 5V)**
- **Bandwidth adjustable from 0 to 14% of f_O**
- **Logic compatible output with 10mA current sinking capability.**
- **Highly stable center frequency.**
- **Center frequency adjustable from 0.01Hz to 60KHz.**
- **Inherent immunity to false signals.**
- **High rejection of out-of-band signals and noise.**
- **Frequency range adjustable over 20:1 range by external resistor.**

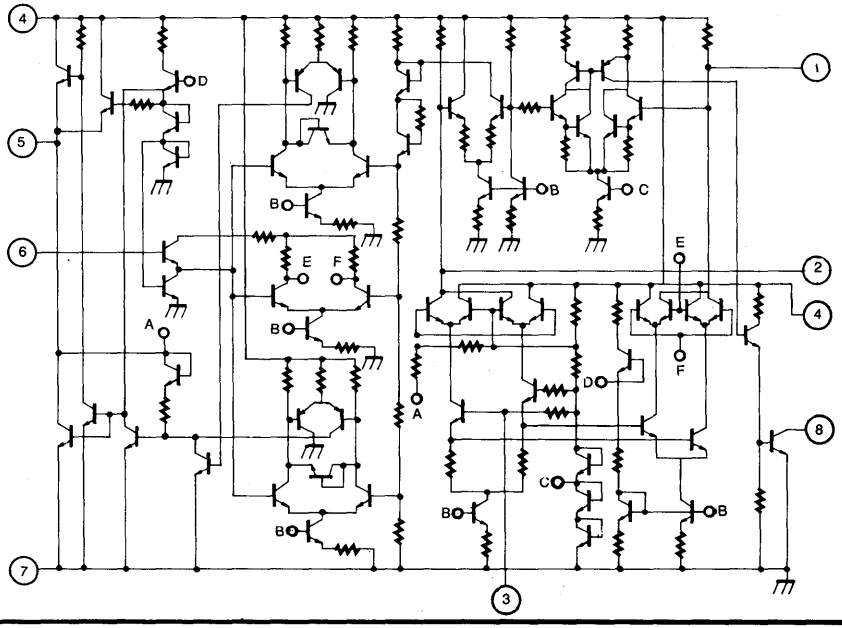
APPLICATIONS

- **Battery-operated tone detection**
- **Touch-tone decoding**
- **Sequential tone decoding**
- **Communications paging**
- **Ultrasonic remote-control**
- **Telemetric decoding**

ORDERING INFORMATION

Device	Package	Operating Temperature
LM567LN	8 DIP	0 ~ + 70°C
LM567LD	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

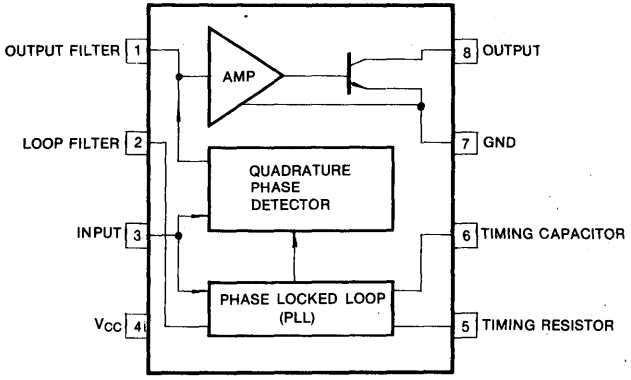
Characteristic	Symbol	Value	Unit
Power Supply	V_{CC}	10	V
Power Dissipation			
Plastic Package	P_d	300	mW
Derate Above +25°C		2.5	mW/°C
Operating Temperature	Topr	0 ~ +70	°C
Storage Temperature	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_a = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}		4.75		8.0	V
Supply Current/Quiescent	I_{CC-1}	R_L = 20KΩ,		0.6	1.0	mA
Supply Current/Activated	I_{CC-2}	R_L = 20KΩ, V_{IN} = 300mV_{rms}, $f_i = f_o$		0.8	1.4	mA
Highest Center Frequency	H_{fo}	R1 = 3KΩ − 5KΩ	10	60		KHz
Center Frequency Drift						
Temperature						
0<T_a<70°C		See Figures 15 and 16		−150		ppm/°C
Supply Voltage		f_o = 10KHz, V_{CC} = 4.75 5.75V		0.5	3.0	%/V
Largest Detection Bandwidth	B.W	f_o = 10KHz, V_{IN} = 300mV_{rms} R_L = 20KΩ	10	14	18	% of f_o
Largest Detection Bandwidth Skew	B.Ws	See Figure 4 for Definition		2	3	% of f_o
Largest Detection Bandwidth Variation With Temperature	B.Wt	V_{IN} = 300mV_{rms}, R_L = 20KΩ		±0.1		%/°C
Largest Detection Bandwidth Variation With Spply Voltage	B.Wv	V_{IN} = 300mV_{rms}, R_L = 20KΩ		±2		%/V
Input Resistance	R_{IN}			100		KΩ
Smallest Detectable Input Voltage	V_{IN-1}	I_L = 10mA, $f_i = f_o$ = 10KHz		20	25	mV_{rms}
Largest No-Output Input Voltage	V_{IN-2}	I_L = 10mA, $f_i = f_o$ = 10KHz	10	15		mV_{rms}
Greatest Simultaneous Outband Signal to Inband Signal Ratio	S_1/S_d	V_{IN} = 300mV_{rms}, f_i'1 = 6KHz $f_i = f_o$ = 10KHz		+6		dB
Minimum Input Signal to Wideband Noise Ratio	S_2/S_d	V_{IN} = 300mV_{rms}, f_i'2 = 14KHz $f_i = f_o$ = 10KHz		−6		dB
Output Saturation Voltage	V_{SAT-1}	I_L = 2mA, V_{IN} = 25mV_{rms}		0.2	0.4	V
	V_{SAT-2}	I_L = 10mA, V_{IN} = 25mV_{rms}		0.3	0.6	V
Output Leakage Current	I_{CO}			0.01	25	μA
Fastest On/Off Cycling Rate	F_{OUT}	$f_i = f_o$ = 10KHz	f_o/20			
Output Rise Time	T_r	R_L = 1KΩ		150		nS
Output Fall Time	T_f	R_L = 1KΩ		30		nS

BLOCK DIAGRAM



TEST CIRCUIT

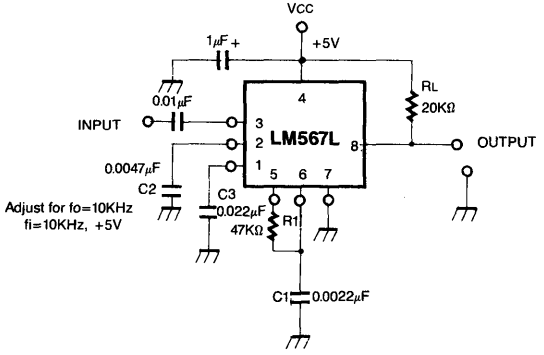


Fig. 1

TYPICAL APPLICATION CIRCUIT

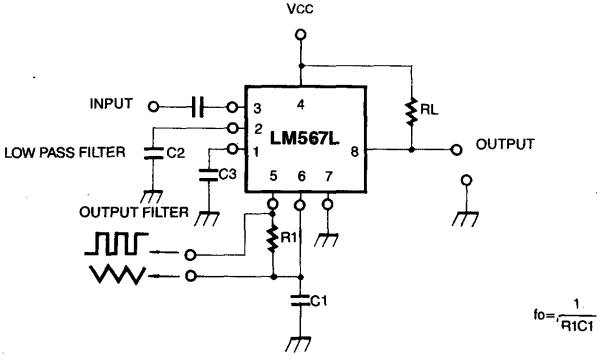


Fig. 2

CIRCUIT DESCRIPTION

The LM567L monolithic circuit consists of a phase detector, low pass filter, and current controlled oscillater which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output.
The input signal is applied to Pin 3 (100KΩ nominal input resistance). Free running frequency is controlled by an RC network at pins 5 and 6. A capacitor on pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; band-width and skew are also dependent upon the circuitry here. Pin 4 is $+V_{CC}$ (4.75 to 8V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is the open collector output, pulling low when an in-band signal triggers the device.
The LM567L is pin-for-pin compatible with the standard LM567-type decoder. Internal resistors have been scaled up by a factor of ten, thereby reducing power dissipation and allowing use of smaller capacitors for the same applications compared to the standard part. This scaling also lowers maximum device center frequency and load current sinking capabilities.

3

PRINCIPLES OF OPERATION

The LM567L is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. The system is comprised of a phase-locked loop, a quadrature detector, a voltage comparator, and an output logic driver.
When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the DC voltage at the output of the detector is shifted. This DC level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic output at Pin 8 is an "open-collector" NPN transistor stage capable of switching 10mA current loads.
The logic output at Pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at Pin 8 goes to a "low" state.
Fig 3 shows the typical output response of the circuit for a tone-burst applied to the input, within the detection band.
The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_o, is determined by the selection of R1 and C1 connected to Pins 5 and 6, as shown in Fig 2.
The detection bandwidth is determined by the size of the PLL filter capacitor, C2 (see Fig 10); and the output response speed is controlled by the output filter capacitor, C3.

DEFINITION OF DEVICE PARAMETERS

CENTER FREQUENCY f_O

f_O is the free-running frequency of the current-controlled oscillator with no input signal. It is determined by resistor R1 between Pins 5 and 6, and capacitor C1 from Pin 6 to ground, f_O can be approximated by

$$f_O = \frac{1}{R1C1} \text{ Hz} \quad \text{where R1 is in ohms and C1 is in farads.}$$

DETECTION BANDWIDTH (BW)

The largest detection bandwidth is the frequency range centered about f_O, within which an input signal larger than the threshold voltage (typically $20mV_{rms}$) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass loop filter at Pin 2. Typical dependence of detection bandwidth on the filter capacitance and the input signal amplitude is shown in Figs 10 and 11, or may be calculated by the approximation.

$$B\cdot W\ (\%) = 338\sqrt{\frac{V_i\ (RMS)}{f_O\ (Hz)\cdot C_2\ (\mu F)}}$$

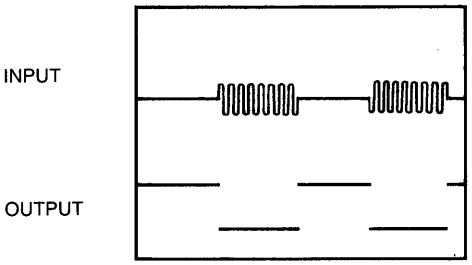
LARGEST DETECTION BANDWIDTH

The largest detection bandwidth is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

DETECTION BANDWIDTH SKEW

The detection bandwidth skew is a measure of how accurately the largest detection band is centered about the center frequency f_o. This parameter is graphically illustrated in Fig 4. In the figure, f_{min} and f_{max} correspond to the lower and the upper ends of the largest detection band, and f1 corresponds to the apparent center of the detection band, and is defined as the arithmetic average of fmin and fmax and f_O is the free running frequency of the LM567L oscillator section. The bandwidth skew Δf_X is the difference between these frequencies. Normalized to f_o, this bandwidth skew can be expressed as:

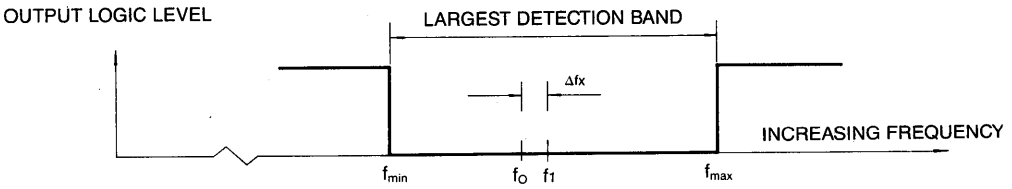
$$\text{Bandwidth Skew} = \frac{\Delta f_X}{f_O} = \frac{(f_{max} + f_{min} - 2f_O)}{2f_O}$$



Response to $100mV_{rms}$ tone burst. $R_L = 1K\Omega$

Fig. 3. Typical Output Response to 100mV Input Tone-Burst

If necessary, the detection bandwidth skew can be reduced to zero by an optional centering adjustment. (see optional controls.)



f_O = PLL free-running frequency
f1 = Center freq of detection band = $(f_{max} + f_{min})/2$

Fig. 4. Definition of Bandwidth Skew

PIN DESCRIPTION AND EXTERNAL COMPONENTS

PIN 3: INPUT

The input signal is applied to Pin 3 through a coupling capacitor. This terminal is internally biased at a DC level 2 volts above ground, and has an input impedance level of approximately 100KΩ.

PIN 5 and 6: TIMING RESISTOR R1 and CAPACITOR C1

The center frequency of the decoder is set by resistor R1 between Pins 5 and 6, and capacitor C1 from Pin 6 to ground, as shown in Fig 2.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately V_{CC}-1.4V and an average DC level of $V_{CC}/2$. A 5KΩ load may be driven from this point. The voltage at pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of $=(V_{CC}-1.3)/3.5$ volts and an average DC level of $V_{CC}/2$. Only high impedance loads should be connected to Pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

PIN 2: LOOP FILTER-C2

Capacitor C2 connected from Pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the LM567L. The filter time constant is given by T2=R2C2, where R2 (100KΩ) is the impedance at Pin 2.

The selection of C2 is determined by the detection bandwidth requirements, as shown in Fig 10. For additional information see section on "Definition of Device Parameters."

The voltage at Pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 f_O to 1.05 f_O, with a slope of approximately 20mV/% frequency deviation.

PIN 1: OUTPUT FILTER-C3

Capacitor C3 connected from Pin 1 to ground forms a simple low-pass post detection filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as T3=R3C3, where R3 (47KΩ) is the internal impedance at Pin 1.

If the value of C3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C3 is too small, the beat rate at the output of the quadrature detector may cause a false logic level change at the output (Pin 8).

The average voltage (during lock) at Pin 1 is a function of the in-band input amplitude in accordance with the given transfer characteristic.

PIN 8: LOGIC OUTPUT

Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, open-collector power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, RL, connected from Pin 8 to the positive supply.

When an in-band signal is present the output transistor at Pin 8 saturates with a collector voltage of less than 0.6V at full rated output current of 10mA. If large output voltage swings are needed, RL can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ ≤15 volts.

OPERATING INSTRUCTIONS

SELECTION OF EXTERNAL COMPONENTS

A typical connection diagram for the LM567L is shown in Fig 2. For most applications, the following procedure will be sufficient for determination of the external components R1, C1, C2, and C3.

1. R1 and C1 should be selected for the desired center frequency by the expression $f_O \approx 1/R1C2$. For optimum temperature stability, R1 should be selected such that 20KΩ ≤ R1 ≤ 200KΩ, and the R1C1 product should have sufficient stability over the projected operating temperature range.
2. Low-pass capacitor, C2, can be determined from the bandwidth versus input signal amplitude graph of Fig 10. One approach is to select an area of operation from the graph, and then adjust the input level and value of C2 accordingly. Or if the input amplitude variation is known, the required f_O C2 product can be found to give the desired bandwidth. Constant bandwidth operation requires $V_i > 200mV_{rms}$. Then, as noted on the graph, bandwidth will be controlled solely by the f_O C2 product.
3. Capacitor C3 sets the band edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If C3 is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. A typical minimum value for C3 is 2 C2.

   Conversely, if C3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C3 passes the threshold value.

PRECAUTIONS

1. The LM567L will lock on signals near (2n+1) f_O and produce an output for signals near (4n+1) f_O, for n=0, 1, 2 etc. Signals at 5 f_O and 9 f_O can cause an unwanted output and should, therefore, be attenuated before reaching the input of the circuit.
2. Operating the LM567L in a reduced bandwidth mode of operation at input levels less than $200mV_{rms}$ results in maximum immunity to noise and out-band signals. Decreased loop damping, however, causes the worst-case lock-up time to increase, as shown by the graph of Fig 13.

3. Bandwidth variations due to changes in the in-band signal amplitude can be eliminated by operating the LM567L in the high input level mode, above 200mV_{rms}. The input stage is then limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. In addition, the limited input stage will create in-band components from subharmonic signals so that the circuit becomes sensitive to signals at $f_O/3$, $f_O/5$ etc.
4. Care should be exercised in lead routing and lead lengths should be kept as short as possible. Power supply leads should be properly bypassed close to the integrated circuit and grounding paths should be carefully determined to avoid ground loops and undesirable voltage variations. In addition, circuits requiring heavy load currents should be provided by a separate power supply, or filter capacitors increased to minimize supply voltage variations.

OPTIONAL CONTROLS

PROGRAMMING

Varying the value of resistor R1 and/or capacitor C1 will change the center frequency. The value of R1 can be changed either mechanically or by solid state switches. Additional C1 capacitors can be added by grounding them through saturated npn transistors.

SPEED OF RESPONSE

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transients becomes greater. Thus maximum operating speed is obtained when the value of capacitor C2 is minimum. At the instant an input signal is applied, its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C2 and C3, in microfarads, which allow the maximum operating speeds for various center frequencies where f_O is Hz.

$$C2 = \frac{13}{f_O}, \quad C3 = \frac{26}{f_O} \ \mu F$$

The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_O/10$ baud. In situations where minimum turn-off is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Fig 5 can be used to bring the quiescent C3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

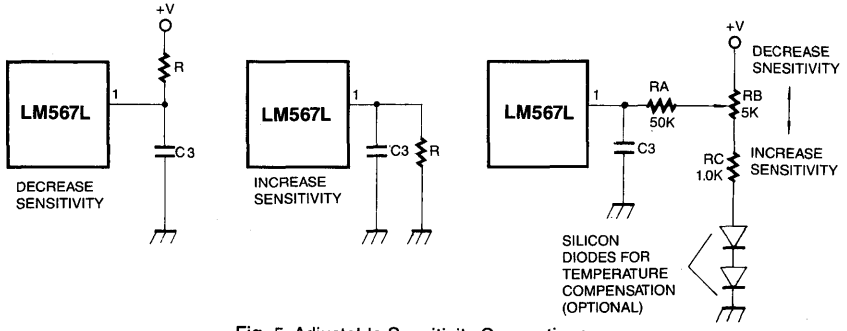


Fig. 5. Adjustable Sensitivity Connections

CHATTER

When the value of C3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, logic may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input (Pin 1) or, by increasing the size of capacitor C3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Fig 6. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

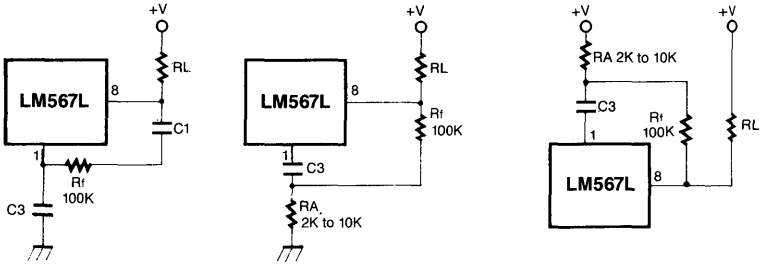


Fig. 6. Methods of Reducing Chatter

SKEW ADJUSTMENT

The circuits shown in Fig 7 can be used to change the position of the detection band (capture range) within the largest detection band (lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only, since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

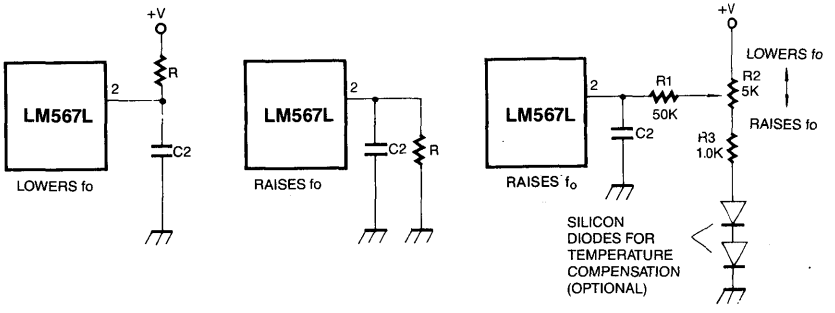


Fig. 7. Detection Band Skew Adjustment

TYPICAL PERFORMANCE CHARACTERISTICS

FIG 8. SUPPLY CURRENT
V_S SUPPLY VOLTAGE

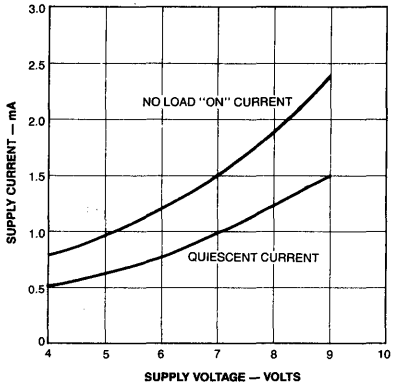


FIG 9. LARGEST DETECTION BANDWIDTH
V_S OPERATING FREQUENCY

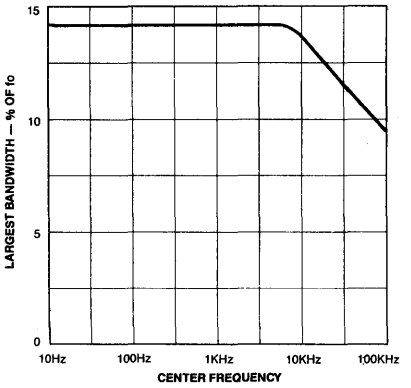


FIG 10. DETECTION BANDWIDTH
V_S A FUNCTION OF C2 AND C3

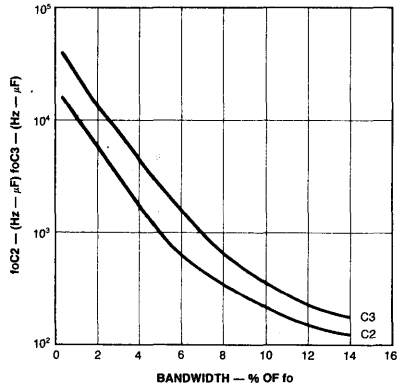


FIG 11. BANDWIDTH V_S INPUT SIGNAL
AMPLITUDE (C2 IN μF)

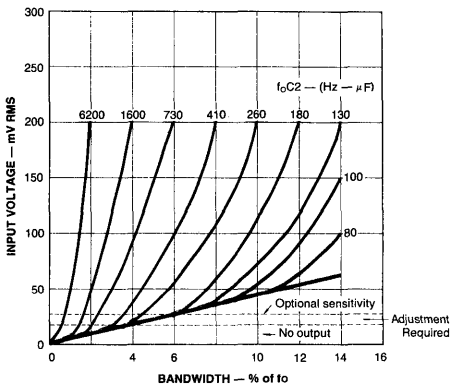


FIG 12. BANDWIDTH VARIATION
WITH TEMPERATURE

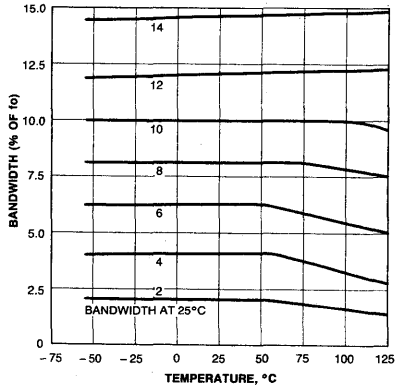


FIG 13. GREATEST NUMBER OF
CYCLES BEFORE OUTPUT

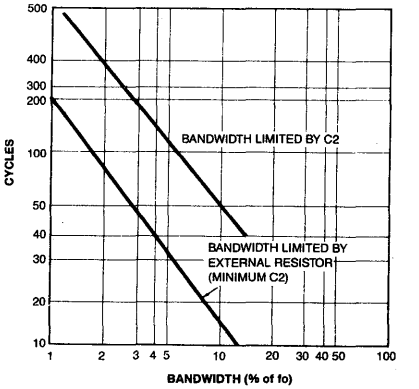


FIG 14. POWER SUPPLY DEPENDENCE OF CENTER FREQUENCY

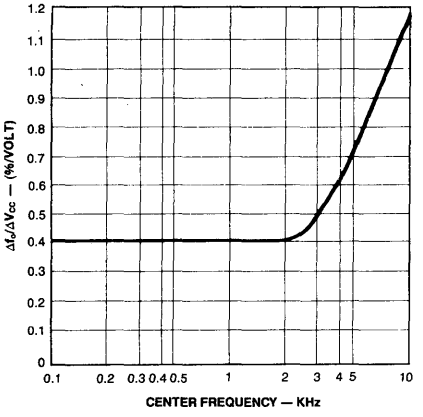


FIG 15. TYPICAL CENTER FREQUENCY DRIFT WITH TEMPERATURE(V_{CC} = 5V, R1 = 80kΩ, fo = 1KHz)

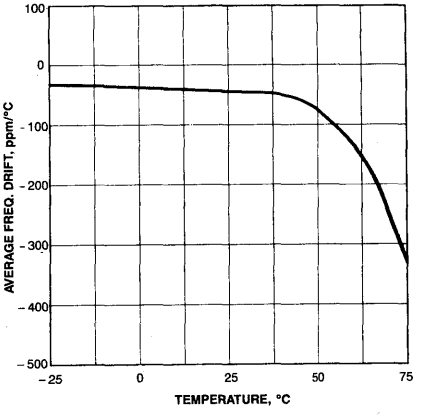
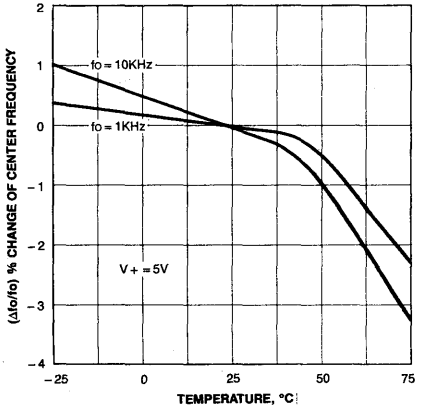


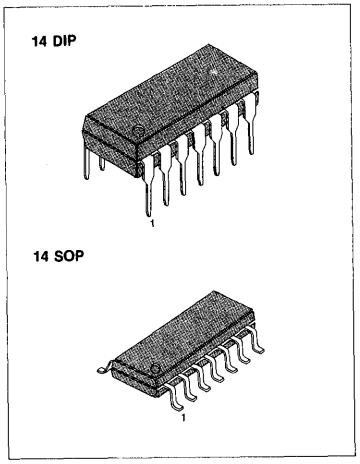
FIG 16. TYPICAL FREQUENCY DRIFT AS A FUNCTION OF TEMPERATURE



3

QUAD LINE DRIVER

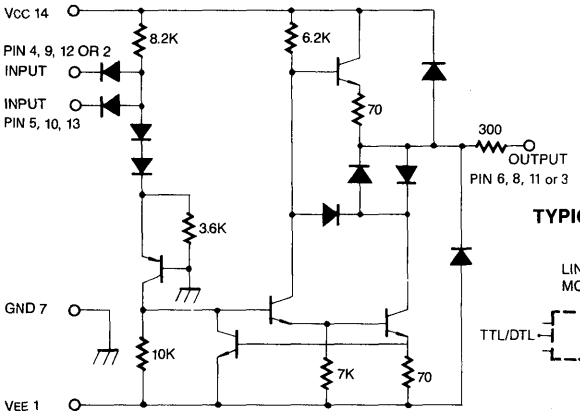
The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.



FEATURES

- **Current Limited Output: ± 10mA typ**
- **Power-Off Source Impedance: 300 Ohms (min)**
- **Simple Slew Rate Control with External Capacitor**
- **Flexible Operating Supply Range**
- **Compatible with DTL and TTL, HCTLS Families**

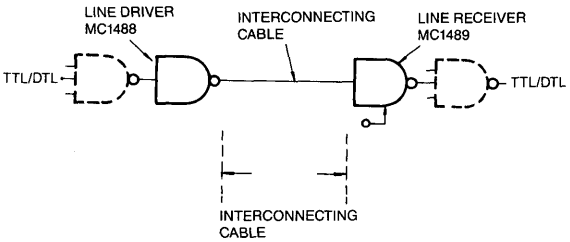
SCHEMATIC DIAGRAM (1/4 of Circuit Shown)



ORDERING INFORMATION

Device	Package	Operating Temperature
MC1488N	14 DIP	0 ~ +70°C
MC1488D	14 SOP	

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 −15	V_{DC}
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	V_{DC}
Output Signal Voltage	V_D	±15	V_{DC}
Power Dissipation	P_D	1000	mW
Derate Above T_a = +25°C	$1/R\theta_{JA}$	6.7	mW/°C
Operating Temperature Range	T_a	0 ~ +70	°C
Storage Temperature Range	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 9.0±1%V, V_{EE} = −9.0 ± 1%V, T_a = 0 ~ 70°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Input Current 1	I_{IL}	Low Logic State (V_{IL} = 0)		1.0	1.6	mA	1
Input Current 2	I_{IH}	High Logic State (V_{IH} = 5.0V)			10	μA	1
Output Voltage-High Logic State	V_{OH}	V_{IL} = 0.8V, R_L = 3.0KΩ V_{CC} = 9.0V, V_{EE} = −9.0V	6	7		V	2
		V_{IL} = 0.8V, R_L = 3.0KΩ V_{CC} = 13.2V, V_{EE} = −13.2V	9	10.5			
Output Voltage-Low Logic State	V_{OL}	V_{IH} = 1.9V, R_L = 3.0KΩ V_{CC} = 9.0V, V_{EE} = −9.0V	−6	−7		V	2
		V_{IH} = 1.9V, R_L = 3.0KΩ V_{CC} = 13.2V, V_{EE} = −13.2V	−9	−10.5			
Output Short Circuit Current	I_{OS+}	Positive	−6	−10	−12	mA	3
Output Short Circuit Current	I_{OS-}	Negative	6	10	12	mA	3
Output Resistance	R_O	V_{CC} = V_{EE} = 0, V_O = ±2.0V	300			Ω	
Positive Supply Current (RL=∞)	I_{CC}	V_{IH} = 1.9V, V_{CC} = +9.0V		15	20	mA	5
		V_{IL} = 0.8V, V_{CC} = +9.0V		4.5	6		
		V_{IH} = 1.9V, V_{CC} = +12V		19	25		
		V_{IL} = 0.8V, V_{CC} = +12V		5.5	7		
		V_{IH} = 1.9V, V_{CC} = +15V			34		
		V_{IL} = 0.8V, V_{CC} = +15V			12		
Negative Supply Current (RL=∞)	I_{EE}	V_{IH} = 1.9V, V_{EE} = −9.0V		−13	−17	mA	5
		V_{IL} = 0.8V, V_{EE} = −9.0V			−15	μA	
		V_{IH} = 1.9V, V_{EE} = −12V		−18	−23	mA	
		V_{IL} = 0.8V, V_{EE} = −12V			−15	μA	
		V_{IH} = 1.9V, V_{EE} = −15V			−34	mA	
		V_{IL} = 0.8V, V_{EE} = −15V			−2.5	mA	
Power Consumption	P_C	V_{CC} = 9.0V, V_{EE} = −9.0V			333	mW	
		V_{CC} = 12V, V_{EE} = −12V			576		

* Maximum package power dissipation may be exceeded if all outputs are shorted simultaneously.

SWITCHING CHARACTERISTICS

(V_{CC} = 9.0 ± 1%V, V_{EE} = −9.0 ± 1%V, T_a = 0 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Propagation Delay Time	t_{PLH}	Z_L = 3.0K and 15pF		275	350	nS	6
Fall Time	t_{THL}	Z_L = 3.0K and 15pF		45	75	nS	6
Rise Time	t_{TLH}	Z_L = 3.0K and 15pF		55	100	nS	6
Propagation Delay Time	t_{PHL}	Z_L = 3.0K and 15pF		110	175	nS	6

DC TEST CIRCUIT

FIGURE 1 INPUT CURRENT

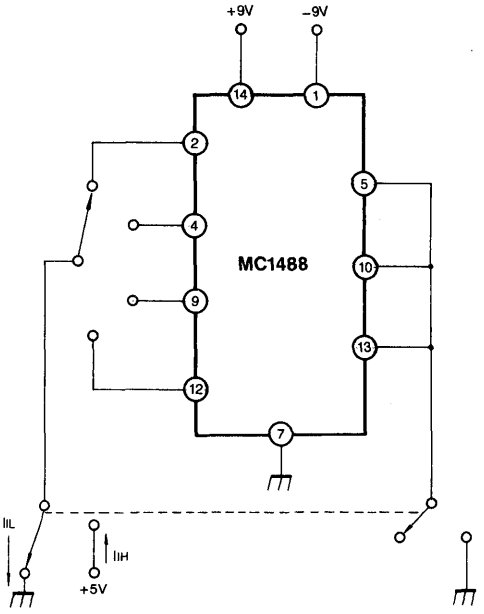


FIGURE 2 OUTPUT VOLTAGE

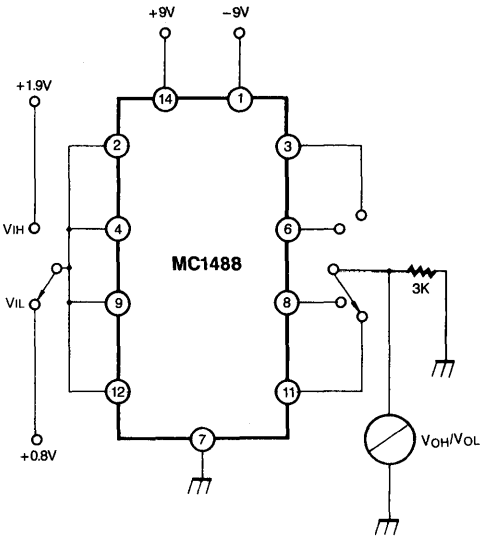


FIGURE 3 OUTPUT SHORT CIRCUIT CURRENT

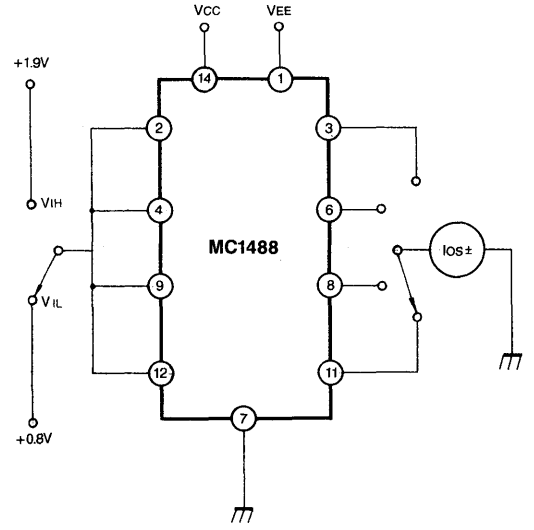


FIGURE 4 OUTPUT RESISTANCE (POWER OFF)

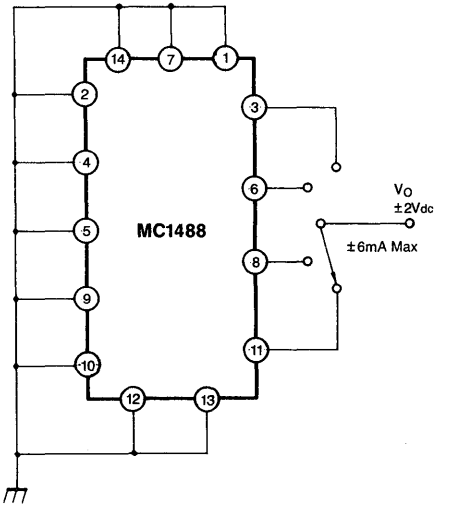


FIGURE 5 POWER SUPPLY CURRENTS

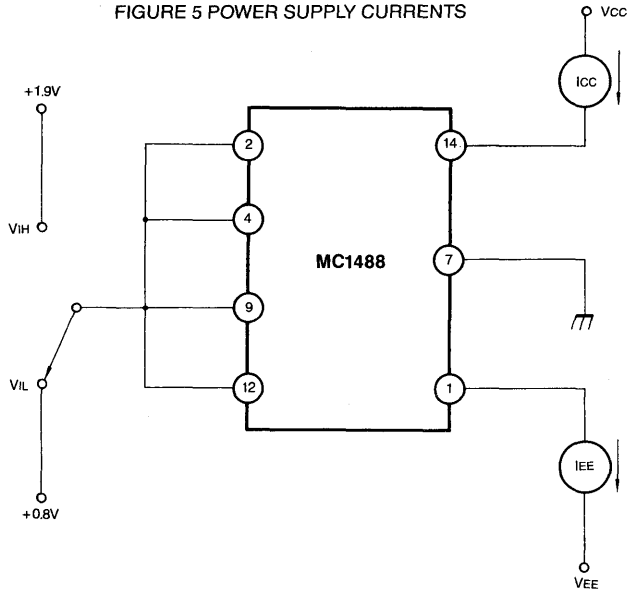
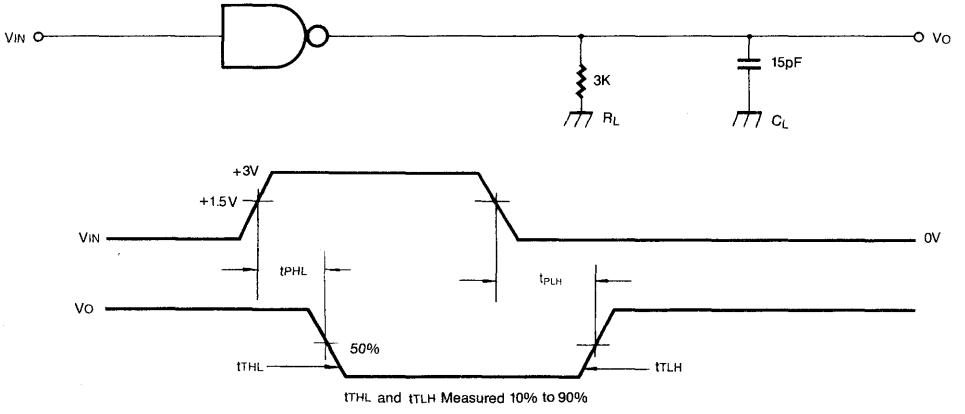


FIGURE 6 SWITCHING RESPONSE



tTHL and tTLH Measured 10% to 90%

TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 7 — TRANSFER CHARACTERISTICS
V_S POWER-SUPPLY VOLTAGE

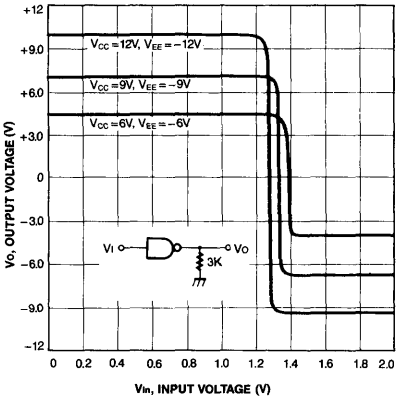


FIGURE 8 — SHORT CIRCUIT OUTPUT CURRENT
V_S TEMPERATURE

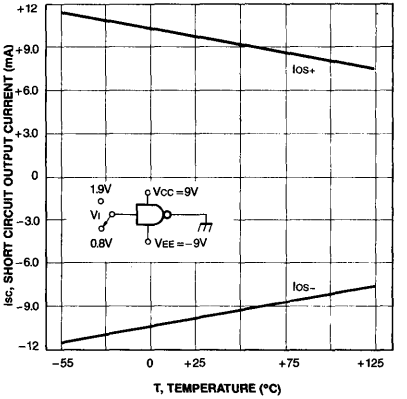


FIGURE 9 — OUTPUT SLEW RATE V_S LOAD CAPACITANCE

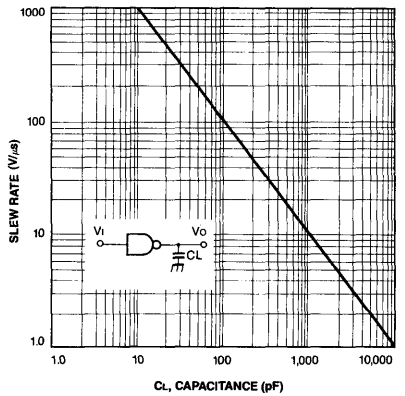


FIGURE 10 — OUTPUT VOLTAGE AND CURRENT LIMITING CHARACTERISTICS

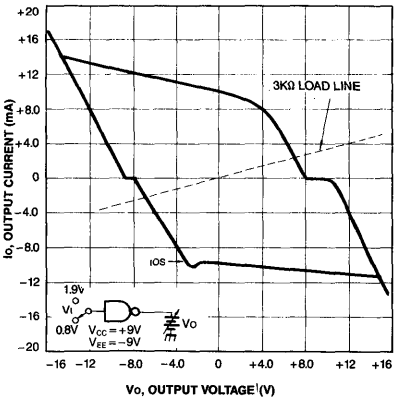
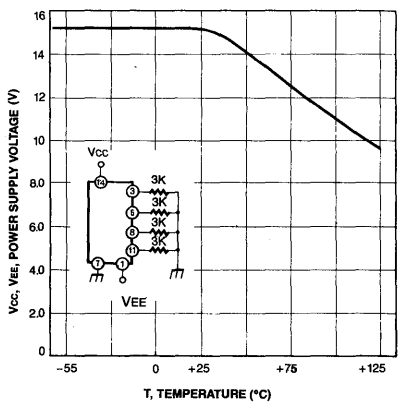
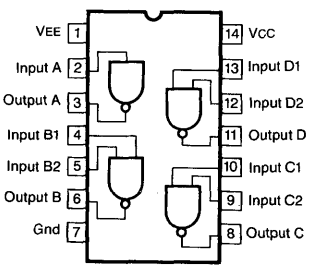


FIGURE 11 — MAXIMUM OPEATING TEMPERATURE
V_S POWER SUPPLY VOLTAGE

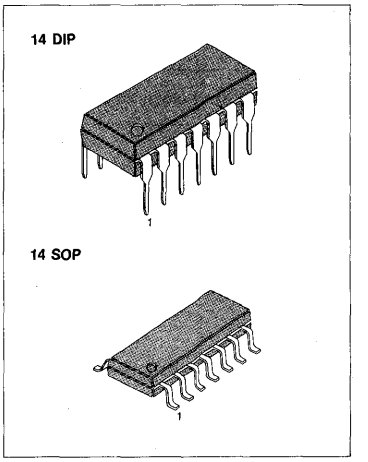


PIN CONNECTIONS



QUAD LINE RECEIVER

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

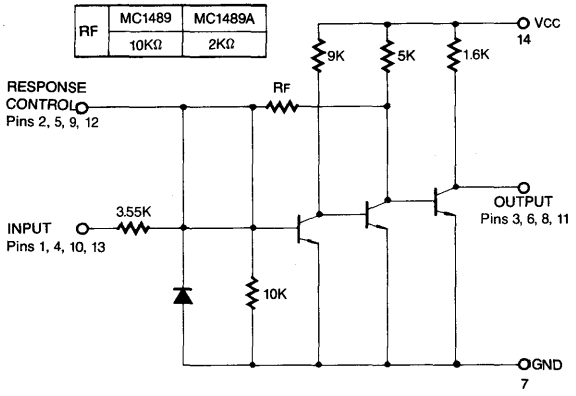


FEATURES

- **Input Resistance: 3.0KΩ to 7.0KΩ**
- **Input Signal Range: ±30 Volts**
- **Response Control**
  - **a) Logic Threshold Shifting**
  - **b) Input Noise Filtering**
- **Input Threshold Hysteresis Built in**

SCHEMATIC DIAGRAM

(1/4 OF CIRCUIT SHOWN)



ORDERING INFORMATION

Device	Package	Operating Temperature
MC1489N	14 DIP	0 ~ +70°C
MC1489AN		
MC1489D	14 SOP	
MC1489AD		

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	V_{DC}
Input Voltage Range	V_{IR}	±30	V_{DC}
Output Load Current	I_L	20	mA
Power Dissipation Derate Above T_a = +25°C	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Temperature	T_a	0 to +70	°C
Storage Temperature	Tstg	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_a = 0 ~ 70°C unless otherwise noted)

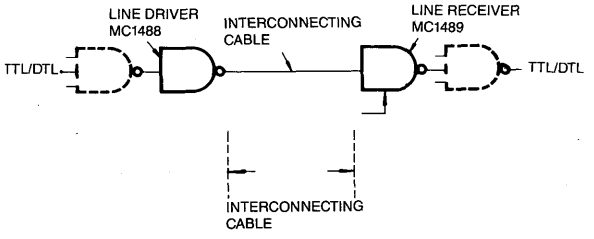
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Positive Input Current	I_{IH}	V_{IH} = 25Vdc	3.6		8.3	mA
		V_{IH} = 3.0Vdc	0.43			
Negative Input Current	I_{IL}	V_{IL} = −25Vdc	−3.6		−8.3	mA
		V_{IL} = −3.0Vdc	−0.43			
Input Turn-On Thereshold Voltage MC1489 MC1489A	V_{IH}	T_a = 25°C, $V_{OL} \leq$ 0.45V I_L = 10mA	 1.0 1.75	 1.95	 1.5 2.25	Vdc
Input Turn-Off Threshold Voltage	V_{IL}	T_a = 25°C, $V_{OH} \geq$ 2.5V, I_L = −0.5mA	0.75		1.25	Vdc
Output Voltage High	V_{OH}	V_{IN} = 0.75V, I_L = −0.5mA	2.5	4.0	5.0	Vdc
		Input Open, I_L = −0.5mA	2.5	4.0	5.0	
Output Voltage Low	V_{OL}	V_{IN} = 3.0V, I_L = 10mA		0.2	0.45	Vdc
Output Short Circuit Current	I_{OS}	V_{IN} = 0.75V		−3.0	−4.0	mA
Power Supply Current	I_{CC}	All gates "on", I_{OUT} = 0mA, V_{IH} = 5.0V		16	26	mA
Power Consumption	P_C	V_{IH} = 5.0V		80	130	mW

SWITCHING CHARACTERISTICS

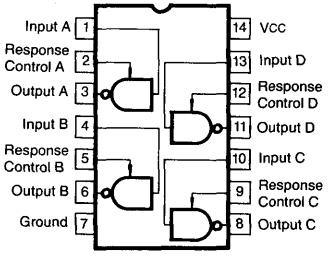
(V_{CC} = 5.0V ± 1%, T_a = 25°C, See Fig. 1)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time	t_{PLH}	R_L = 3.9KΩ		25	85	nS
Rise Time	t_{TLH}	R_L = 3.9KΩ		120	175	nS
Propagation Delay Time	t_{PHL}	R_L = 390Ω		25	50	nS
Fall Time	t_{THL}	R_L = 390Ω		10	20	nS

TYPICAL APPLICATION

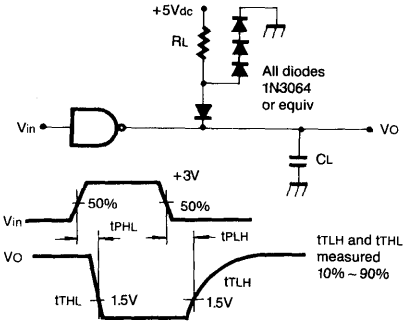


PIN CONNECTIONS



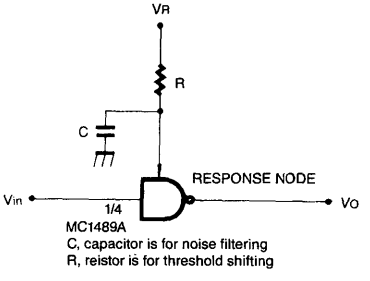
TEST CIRCUIT

Fig 1 — SWITCHING RESPONSE



CL=15pF=total parasitic capacitance, which includes probe and wiring capacitances

Fig 2 — RESPONSE CONTROL NODE



C, capacitor is for noise filtering
R, reistor is for threshold shifting

TYPICAL PERFORMANCE CHARACTERISTICS

(VCC=5.0 Vdc Ta=+25°C unless otherwise noted)

Fig. 3 — TYPICAL TURN-ON THRESHOLD V_S CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

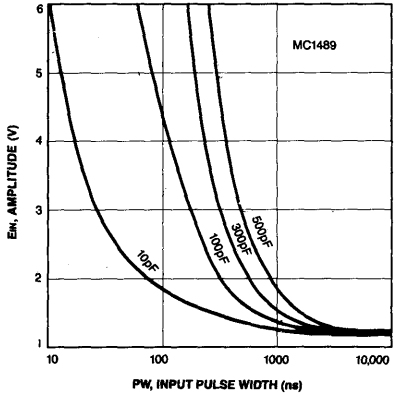


Fig. 4 — TYPICAL TURN-ON THRESHOLD V_S CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

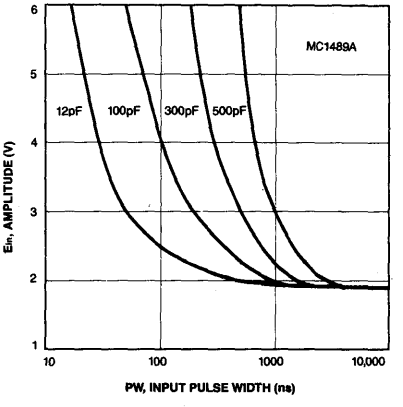


Fig. 5 — INPUT CURRENT

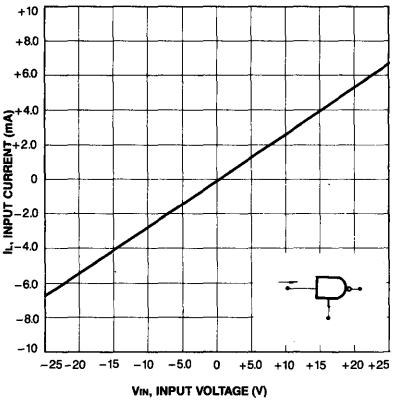


Fig. 6 — MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

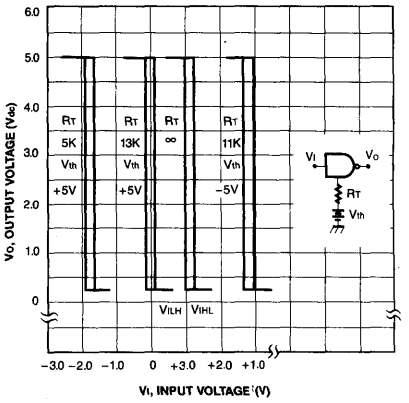


Fig. 7 — MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

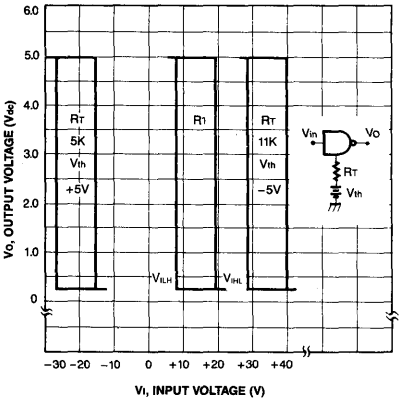


Fig. 8 — INPUT THRESHOLD VOLTAGE Vs. TEMPERATURE

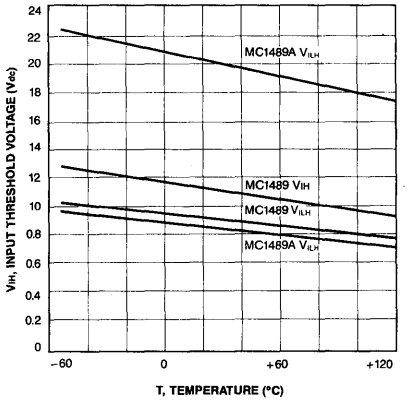
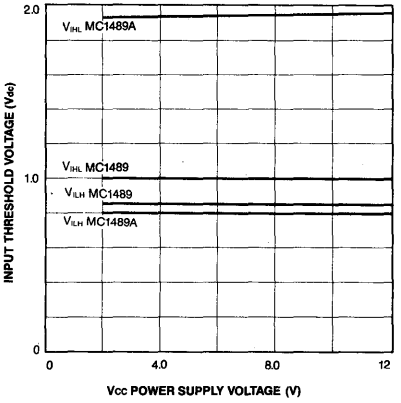
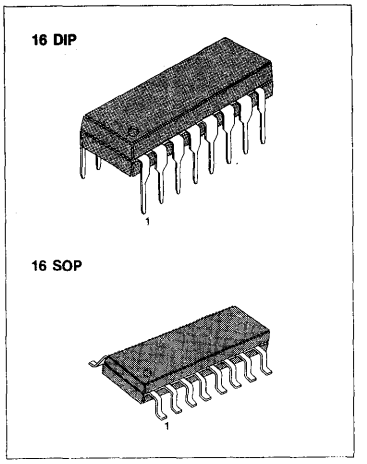


Fig. 9 — INPUT THRESHOLD Vs. POWER SUPPLY VOLTAGE



LOW VOLTAGE/POWER NARROW BAND FM IF

The MC3361 is designed for use in FM dual conversion communication. It contains a complete narrow band FM demodulation system operable to less than 2.5V supply voltage. This low-power narrow-band FM IF system provides the second converter, second IF, demodulator. Filter Amp and squelch circuitry for communications and scanning receivers.



FEATURES

- **Stable operation with wide supply voltage (2.5V to 7.0V)**
- **Low power consumption (4.0mA typ. at V_{CC} = 4.0V)**
- **Excellent input sensitivity (−3dB limiting, 2.0μV_{rms} typ)**
- **Minimum number of external components required.**

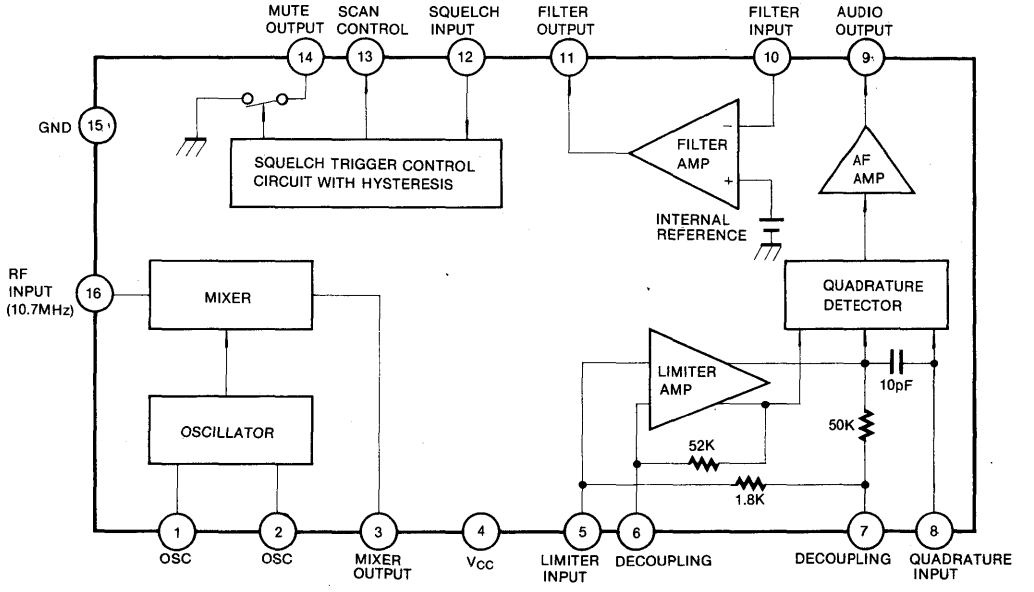
APPLICATION

- Cordless phone (for home use)
- FM dual conversion communications equipment

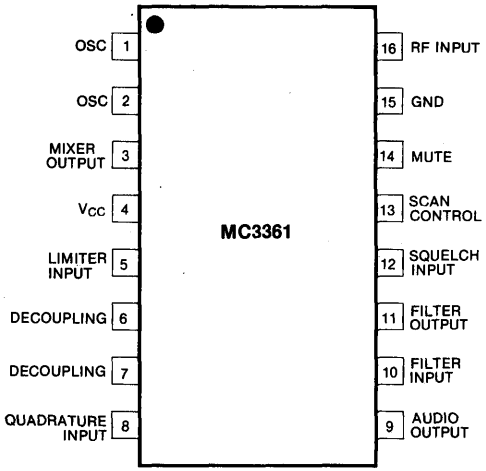
ORDERING INFORMATION

Device	Package	Operating Temperature
MC3361N	16DIP	−20 ~ +70°C
MC3361D	16 SOP	

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC} (max)	10	V
Operating Voltage Range	V_{CC}	2.5 to 7.0	V
Detector Input Voltage	V_8	1.0	V_{p-p}
RF Input Voltage ($V_{CC} \geq 4.0V$)	V_{16}	1.0	V_{rms}
Mute Function	V_{14}	−0.5 ~ +5.0	V_{peak}
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

Absolute maximum ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

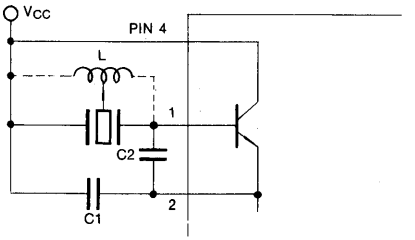
ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.0V, fo = 10.7MHz, △f = ±3KHz, f_{MOD} = 1KHz, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	Squelch off (V_{12} = 2V) Squelch on (V_{12} = GND)		4.0 6.0		mA mA
Input Limiting Voltage	V_{INL}	−3.0dB limiting		2.0		μV
Detector Output Voltage	V_9			2.0		V_{dc}
Detector Output Impedance	Z_{OD}			400		Ω
Audio Output Voltage	V_O	V_{in} = 10mV	100	160		mV_{rms}
Filter Gain	A_{VF}	f = 10KHz, V_{in} = 5mV	40	48		dB
Filter Output DC Voltage	V_{OF}			1.5		V_{dc}
Trigger Hysteresis of Filter	V_{TH}			50		mV
Mute Switch-on Resistance	R_{ON}	Mute "Low"		10		Ω
Mute Switch-off Resistance	R_{OFF}	Mute "High"		10		MΩ
Scan Control "Low" Output	V_{13L}	Mute off (V_{12} = 2V)			0.5	V_{dc}
Scan Control "High" Output	V_{13H}	Mute on (V_{12} = GND)	3.0			V_{dc}
Mixer Conversion Gain	A_{VM}			24		dB
Mixer Input Resistance	R_{IM}			3.3		KΩ
Mixer Input Capacitance	C_{IM}			2.2		pF

3

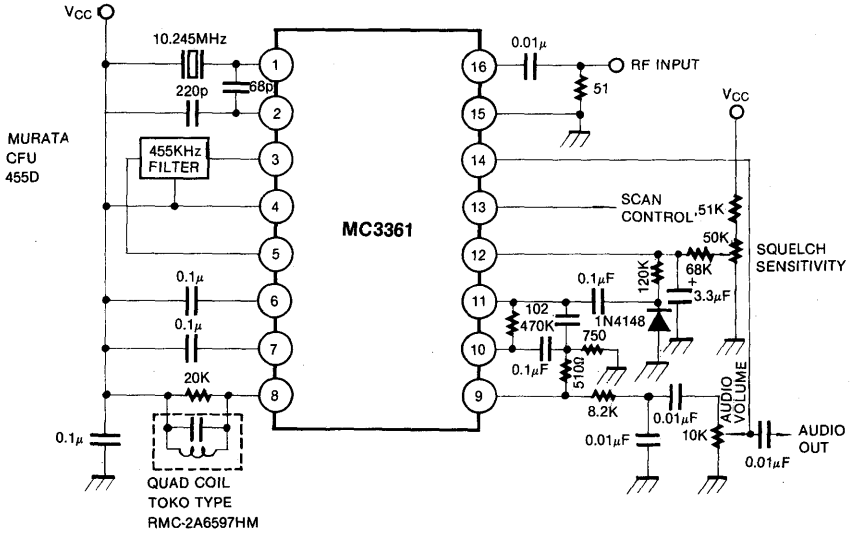
PIN DESCRIPTION

Pin No.	Name	Function
1, 2	OSC	The crystal oscillator terminals for mixer conversion. The colpitts oscillator is internally biased with a regulated current source which assures proper operation over a wide supply range. The collector, base and emitter terminals are at pins 4, 1, and 2 respectively. The crystal which is used in the parallel resonant mode, may be replaced with an appropriate inductor if the application does not require the stability of a crystal oscillator. 
3, 16	Mixer Input, (RF Input) Mixer Output	The mixer input/output terminals. The mixer converts the input frequency (10.7MHz) down to 455KHz. The mixer is double balanced to reduce spurious response. The mixer output impedance will properly match the input impedance of a ceramic filter which is used as a bandpass filter coupling the mixer output to the IF limiting amplifier. Following the mixer, a ceramic bandpass filter is recommended. The 455KHz types come in bandwidth from ±2KHz to ±15KHz.
4	V_{CC}	Power supply pin.
5, 6, 7	Limiter Amp Input, Decoupling	Limiter Amp inputs and decoupling terminals. The IF limiter amplifier consists of five differential gain stages, with the input impedance set by 1.8KΩ resistor to properly terminate the ceramic filter driving the IF. The IF output is connected to the external quad coil at pin 8 via an internal 10pF capacitor. The frequency limitation is due to the high resistance values in the IF, which were necessary to meet the low power requirement. The output of the limiter is internally connected to the quadrature detector.
8, 9	Quadrature Input, Audio Output	Quadrature detector input and output terminals. A conventional quadrature detector is used to demodulate the FM signal. The Q of the quad coil, which is determined by the external resistor placed across it, has multiple affects on the audio output. ($Q \propto R$) Increasing the Q increases audio output level but because of non-linearities in the tank phase characteristic, also increases distortion. For proper operation, the voltage swing on pin 9 should be adequate to prevent distortion (160mV_{rms} typ). The detector output is amplified and buffered to the audio output pin 9, which has an output impedance of approximately 400Ω.

PIN DESCRIPTION (Continued)

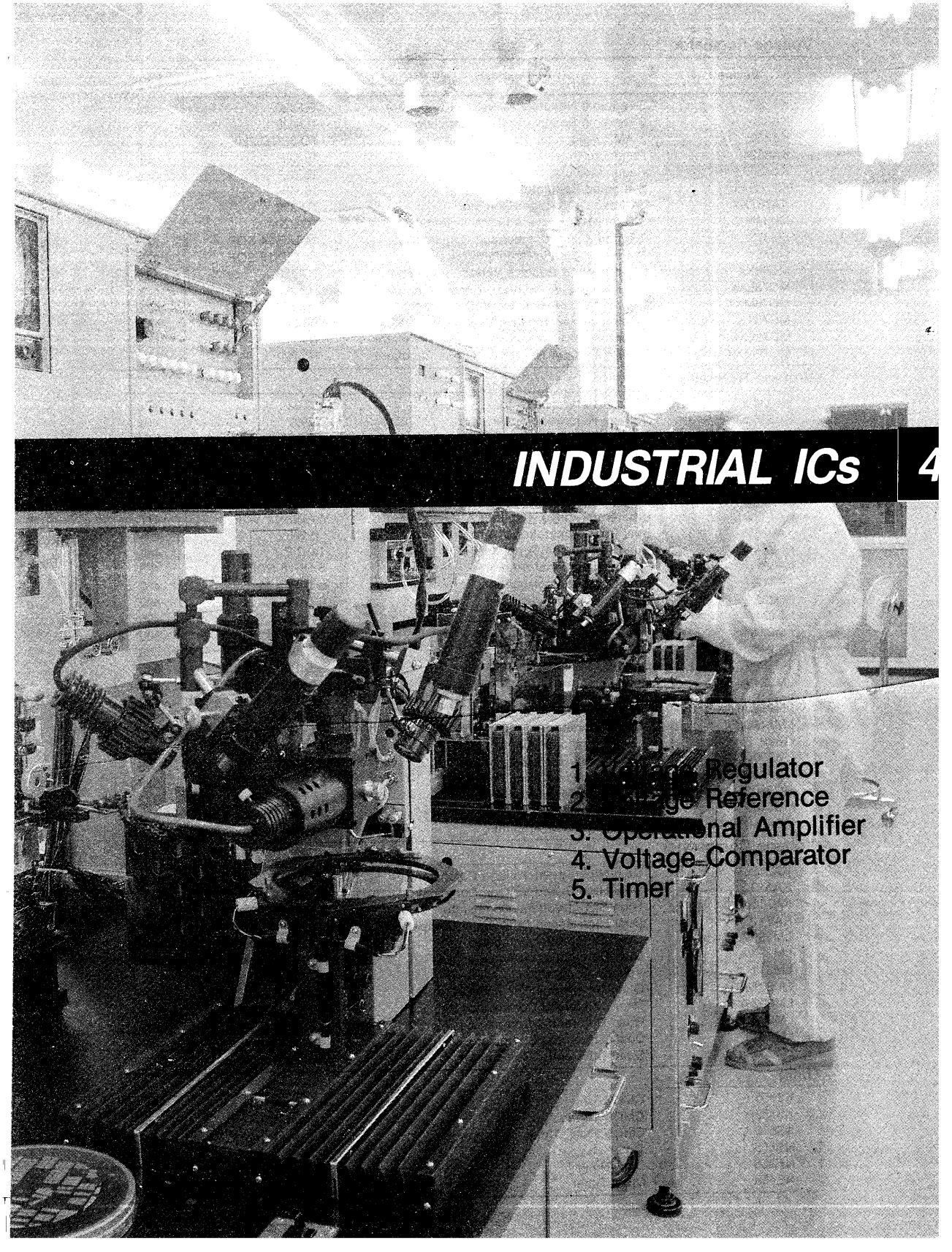
Pin No.	Name	Function
10, 11	Filter Input/ Output	Filter Amp input/output terminals. The inverting OP Amp is provided with an output at pin 11 providing dc bias (externally) to the input at pin 10 which is referred internally to 0.7V. The OP Amp is normally utilized as either a bandpass filter to extract a specific frequency from the audio output, such as a ring or dial tone, or as a high pass filter to detect noise due to no input at the mixer.
12, 13, 14	Squelch In, Scan Control, Mute Output	Squelch control input, scan control output, mute output terminals. A low bias to pin 12 sets up the squelch trigger circuit such that pin 13 is high, and the audio mute (pin 14) is internally short circuited to ground (typically 10Ω to GND). If pin 12 is raised above mute threshold (0.7V) by the noise or tone detector, pin 13 (scan control output) will become low level output and the audio mute will be an open circuit. There is 50mV of hysteresis at pin 12 which effectively prevents jitter.
15	GND	GND pin.

TYPICAL APPLICATION CIRCUIT



In the above typical application, the audio signal is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitered by an active filter and a detector. A squelch trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

NOTES



INDUSTRIAL ICs 4

1. Voltage Regulator
2. Voltage Reference
3. Operational Amplifier
4. Voltage Comparator
5. Timer

Voltage Regulator

Device	Function	Package	Page
KA337	3-Terminal Negative Adjustable Regulator	TO-220	313
KA340	3-Terminal Positive Voltage Regulator	TO-220	317
KA350	3 AMP Adjustable Positive Voltage Regulator	TO-3P/TO-220	329
KA3524	Regulator Pulse Width Modulator	16 DIP	337
KA7500	Regulator Pulse Width Modulator	16 DIP	345
KA78S40	Switching Regulator	16 DIP	349
KA78TXX	3A Positive Voltage Regulator	TO-220	355
LM317	3-Terminal Positive Adjustable Regulator	TO-220	366
LM323	3-Terminal Positive Voltage Regulator	14 DIP/14 SOP	371
LM723	Precision Voltage Regulator	14 DIP/14 SOP	376
MC78XX	3-Terminal 1A Positive Voltage Regulator	TO-220	382
MC78LXX	3-Terminal 0.1A Positive Voltage Regulator	TO-92	413
MC78MXX	3-Terminal 0.5A Positive Voltage Regulator	TO-220	424
MC79XX	3-Terminal 1A Negative Voltage Regulator	TO-220	437
MC79LXX	3-Terminal 0.1A Negative Voltage Regulator	TO-92	447
MC79MXX	3-Terminal 0.5A Negative Voltage Regulator	TO-220	452

Voltage Reference

KA336-2.5	Voltage Reference Diode	TO-92	458
KA336-5.0	Voltage Reference Diode	TO-92	462
KA431	Programmable Precision Reference	TO-92/8 DIP/8 SOP	466

Operational Amplifier

KA201A	Single Operational Amplifier	8 DIP/8 SOP	472
KA301A	Single Operational Amplifier	8 DIP/8 SOP	472
KA733C	Differential Video Amplifier	14 DIP/14 SOP	477
KA9256	Dual Power Operational Amplifier	10 SIP	484
KF347	Quad Operational Amplifier	14 DIP	486
KF351	Single Operational Amplifier	8 DIP/8 SOP	488
KF442	Dual Operational Amplifier	8 DIP	490
KS272	Dual Operational Amplifier	8 DIP	492
KS274	Quad Operational Amplifier	14 DIP	496
LM224/A	Quad Operational Amplifier	14 DIP/14 SOP	500
LM248	Quad Operational Amplifier	14 DIP/14 SOP	509
LM258/A	Quad Operational Amplifier	8 DIP/8 SOP/9 SIP	515
LM324/A	Quad Operational Amplifier	14 DIP/14 SOP	500
LM348	Quad Operational Amplifier	14 DIP/14 SOP	509
LM358/A	Quad Operational Amplifier	8 DIP/8 SOP/9 SIP	515
LM741C/E/I	Single Operational Amplifier	8 DIP/8 SOP	523
LM2902	Quad Operational Amplifier	14 DIP/14 SOP	500
LM2904	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	515
MC1458AC/C/S/I	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	529
MC3303	Quad Operational Amplifier	14 DIP/14 SOP	533
MC3403	Quad Operational Amplifier	14 DIP/14 SOP	533
MC4558C/AC/I	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	540

Voltage Comparator

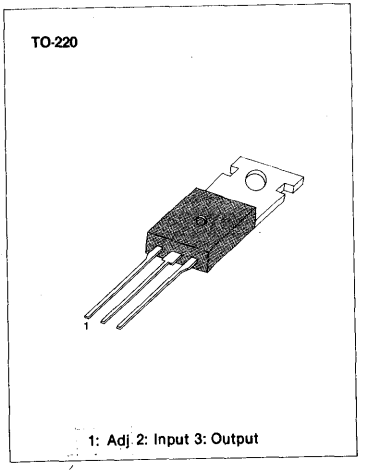
KA219	Dual High Speed Voltage Comparator	14 DIP/14 SOP	545
KA319	Dual High Speed Voltage Comparator	14 DIP/14 SOP	545
KA710C/I	High Speed Voltage Comparator	14 DIP/14 SOP	550
KA711C/I	Dual High Speed Differential Comparator	14 DIP/14 SOP	554
LM239/A	Quad Differential Comparator	14 DIP/14 SOP	557
LM293/A	Dual Differential Comparator	8 DIP/8 SOP/9 SIP	565
LM311	Voltage Comparator	8 DIP/8 SOP	572
LM339/A	Quad Differential Comparator	14 DIP/14 SOP	557
LM393/A	Dual Differential Comparator	8 DIP/8 SOP/9 SIP	565
LM2901	Quad Differential Comparator	14 DIP/14 SOP	557
LM2903	Dual Differential Comparator	8 DIP/8 SOP	565
LM3302	Quad Differential Comparator	14 DIP/14 SOP	557

Timer

KS555	CMOS Timer	8 DIP/8 SOP	577
KS555H	CMOS Timer	8 DIP/8 SOP	582
KS556	CMOS Dual Timer	14 DIP/14 SOP	586
NE555	Timer	8 DIP/8 SOP	590
NE556	Dual Timer	14 DIP/14 SOP	594
NE558	Quad Timer	16 DIP/16 SOP	597

3-TERMINAL NEGATIVE ADJUSTABLE REGULATOR

The KA337 is a 3-terminal negative adjustable regulator. It supply in excess of −1.5A over an output voltage range of −1.2V to −37V.
This regulator requires only two external resistor to set a output voltage and 1 capacitor to compensate frequency.



FEATURES

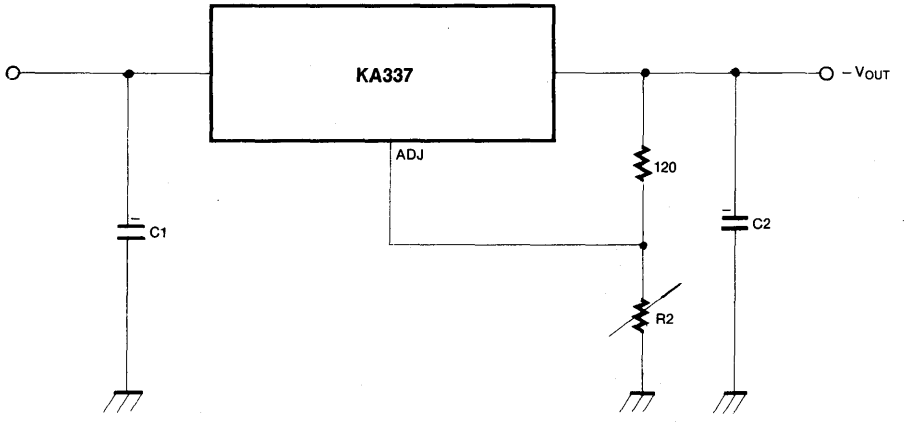
- **Output current in excess of −1.5A**
- **Output voltage adjustable between −0.2V & −37V**
- **Internal thermal-overload protection**
- **Internal short-circuit current-limiting constant with temperature**
- **Output transistor safe-area compensation**
- **Floating operation for high-voltage applications**
- **Standard 3-pin, TO-220 package**

ORDERING INFORMATION

Device	Package	Operation Temperature
KA337T	TO-220	0 ~ +125°C
**KA237T	TO-220	−25 ~ +150°C

** Under development

APPLICATION CIRCUIT



* $-V_{OUT} = -1.25V\ (1 + R2/120\Omega) + (-I_{adj} * R2)$
* Output current depends on maximum power dissipation

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input-Output Voltage Differential	V_{IN}-V_{OUT}	40	V
Power Dissipation	P_D	Internally limited	
Operating Temperature Range	T_{opr}	0 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

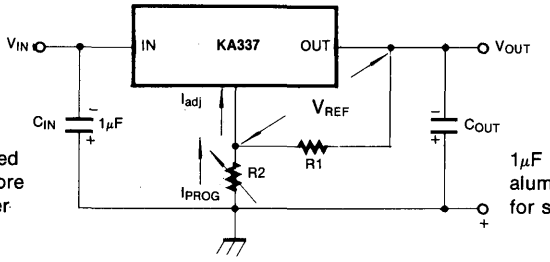
ELECTRICAL CHARACTERISTICS

($V_{in} - V_{out} = 5V$, $I_{out} = -0.5A$, $0°C \leq T_j \leq 125°C$, $P_{max} = 20W$, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Line Regulation	V_O	Ta = 25°C $-40V \leq V_{OUT} - V_{IN} \leq -3V$		0.01	0.04	%/V
		$-40V < V_{OUT} - V_{IN} \leq -3V$		0.02	0.07	
Load Regulation	V_O	Ta = 25°C $10mA \leq I_{OUT} \leq 1.5A$		15	50	mV
		$10mA \leq I_{OUT} \leq 1.5A$		15	150	
Adjustable Pin Current	I_{adj}			50	100	μA
Adjustable Pin Current Change		Ta = 25°C $10mA \leq I_{OUT} \leq 1.5A$ $-40V \leq V_{OUT} - V_{IN} \leq -3V$		2	5	μA
Reference Voltage	V_{ref}	Ta = 25°C	−1.213	−1.250	−1.287	V
		$-40V \leq V_{OUT} - V_{IN} \leq -3V$ $10mA \leq I_{OUT} \leq 1.5A$	−1.200	−1.250	−1.300	
Temperature Stability	T_S			0.6		%
Minimum Load Current to Maintain Rejection	I_I (min)	$-40V \leq V_{OUT} - V_{IN} \leq -3V$		2.5	10	mA
		$-10V \leq V_{OUT} - V_{IN} \leq -3V$		1.5	6	
Output Noise	en	Ta = 25°C $10Hz \leq f \leq 10KHz$		$30 \times V_{OUT}$		$V/10^6$
Ripple Rejection	RR	$V_{OUT} = -10V$, f = 120Hz		60		dB
		$C_{adj} = 10\mu F$	66	77		
Long Term Stability		$T_j = 125°C$, 1000 hours		0.0003	0.001	$\%/H_{OUT}$
Thermal Resistance Junction to Case	$R_{\theta JC}$			4		°C/W

TYPICAL APPLICATION

FIG. 2 ADJUSTABLE VOLTAGE REGULATOR



1μF solid tantalum required only if the regulator is more than 10cm from the power supply filter capacitor

1μF solid tantalum or 10μF aluminum electrolytic required for stability

R1 is 120Ω Typical

$R2 = R1\ (\frac{V_{OUT}}{V_{REF}} - 1)$ where $V_{REF} = -1.25V$ Typical

The KA337 is a 3-terminal floating regulator. In operation, the KA337 develops and maintains a nominal −1.25 volt reference V_{REF} between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see FIG. 2), and this constant current flows through R2 from ground. The regulated output voltage is given by:

$$V_{OUT} = V_{REF}\ (1 + \frac{R2}{R1}) + I_{adj}\ R2$$

Since the current into the adjustment terminal (I_{adj}) represents an error term in the equation, the KA337 was designed to control I_{adj} to less than 100μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will increase.
Since the KA337 is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

LOAD REGULATION

The KA337 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

TYPICAL PERFORMANCE CHARACTERISTIC

Fig. 3 ADJUSTMENT CURRENT

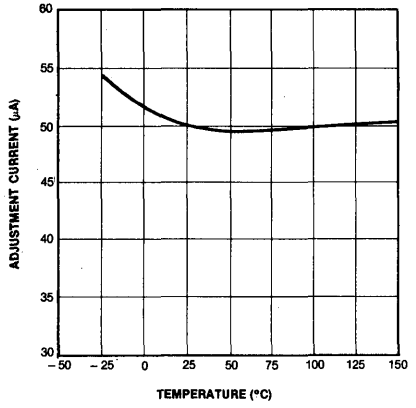


Fig. 4 CURRENT LIMIT

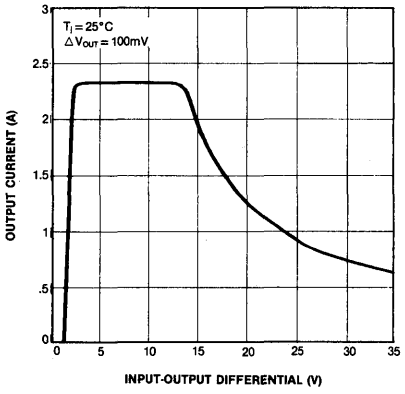


Fig. 5 LOAD REGULATION

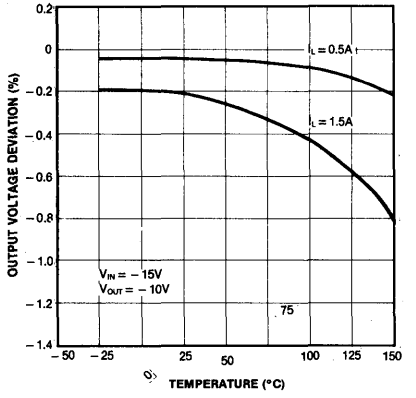
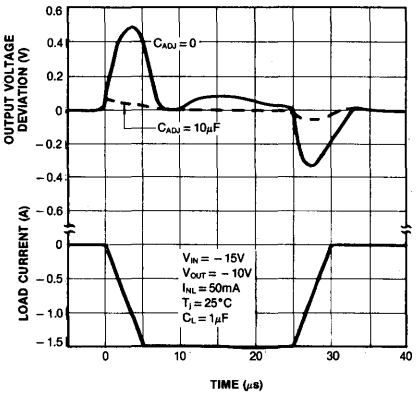


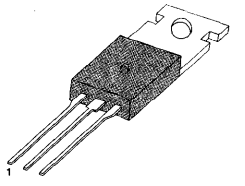
Fig. 6 LOAD TRANSIENT RESPONSE



3-TERMINAL POSITIVE VOLTAGE REGULATORS

The KA340XX series of three-terminal positive voltage regulators are available in TO-220 package and with several fixed output voltages, providing better performance than 78XX series regulators. These are designed to have outstanding ripple rejection, superior line and load regulation in high power applications (over 15W). Each type employs internal current limiting, thermal shutdown and safe area protection.
Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltage and currents.

TO-220



1: Input 2: GND 3: Output

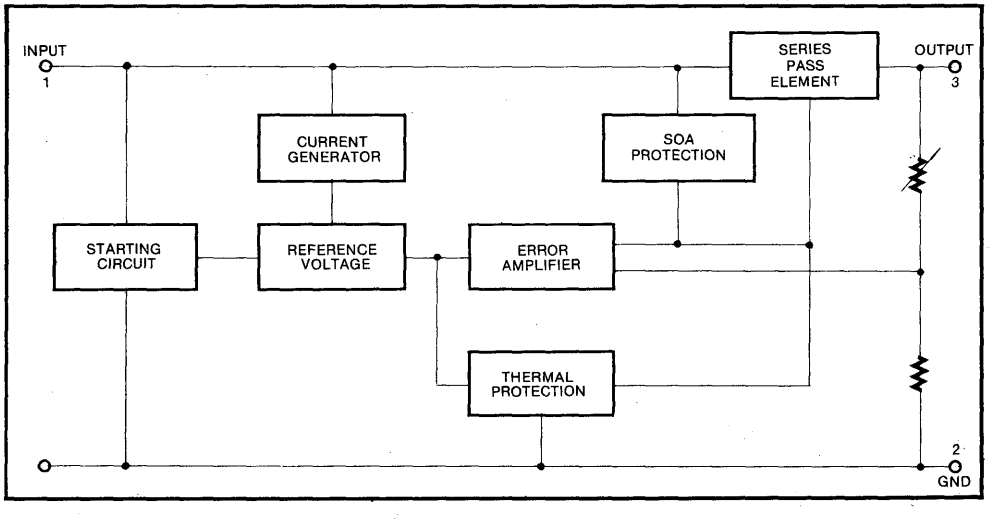
FEATURES

- **Maximum output current: 1.5A**
- **Output voltage of 5, 6, 8, 9, 10, 11, 12, 15, 18, 24V**
- **Superior line and load regulation than 78XX series**
- **Output transistor SOA protection**
- **Internal short-circuit current limit**
- **Thermal overload protection**
- **Output voltage tolerances of ±4% at 25°C and ±5% over the temperature range**

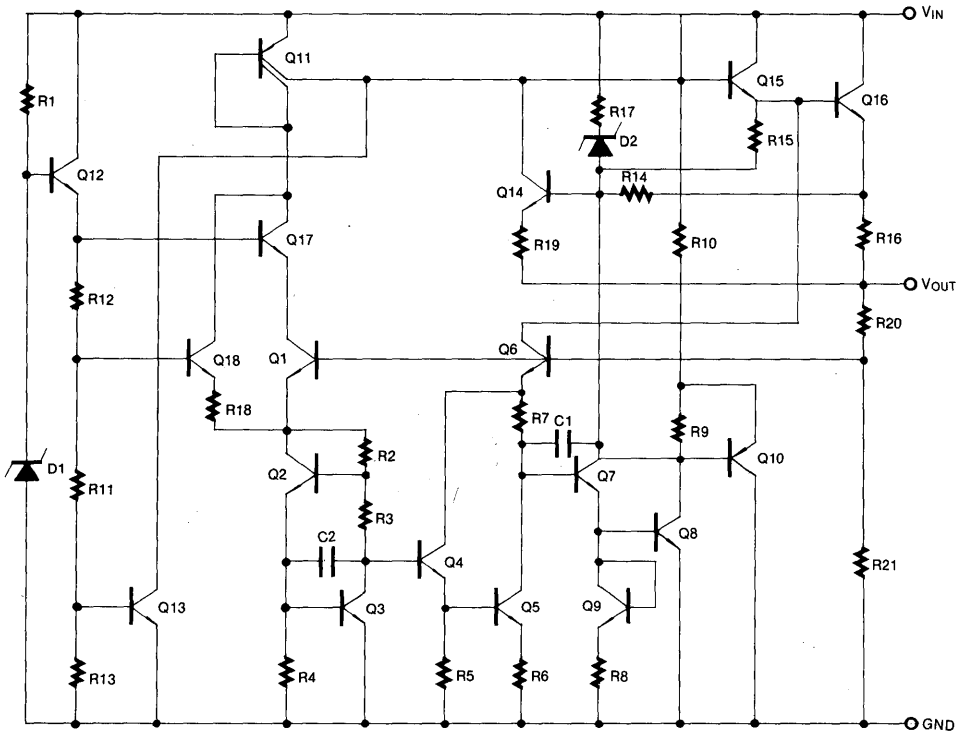
ORDERING INFORMATION

Device	Package	Operating Temperature
KA340TXX	TO-220	0 ~ +125°C

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (for $V_O = 5V$)	V_i	35	V
Thermal Resistance Junction-Cases	θ jc	5	°C/W
Thermal Resistance Junction-Air	θ ja	65	°C/W
Junction Operating Temperature	T_{opr}	0 ~ +150	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS KA340T05

(Refer to test circuit, $0°C \leq T_j \leq 125°C$, $V_i = 10V$, $I_O = 0.5A$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	$T_j = 25°C$, $5mA \leq I_O \leq 1.0A$		4.80	5.00	5.20	V
		$5mA \leq I_O \leq 1.0A$, $PD \leq 15W$ $V_i = 7.5V$ to $20V$		4.75	—	5.25	
Line Regulation	$\triangle V_O$	$T_j = 25°C$, $V_i = 7V$ to $25V$		—	3	50	mV
		$V_i = 8V$ to $20V$		—	—	50	
		$I_O \leq 1A$	$V_i = 8V$ to $12V$	—	—	25	
			$V_i = 7.5V$ to $20V$ $T_j = 25°C$	—	—	50	
Load Regulation	$\triangle V_O$	$T_j = 25°C$	$5mA \leq I_O \leq 1.5A$	—	10	50	mV
			$0.25A \leq I_O \leq 0.75A$	—	—	25	
		$5mA \leq I_O \leq 1A$		—	—	50	
Quiescent Current	I_d	$I_O = 1A$	$T_j = 25°C$	—	—	8	mA
			$0°C \leq T_j \leq 125°C$	—	—	8.5	
Quiescent Current Change	$\triangle I_d$	$5mA \leq I_O \leq 1A$		—	—	0.5	mA
		$T_j = 25°C$ $I_O \leq 1A$, $V_i = 7.5V$ to $20V$		—	—	1.0	
		$V_i = 7V$ to $25V$		—	—	1.0	
Output Noise Voltage	V_n	$T_a = 25°C$, $f = 10Hz$ to $100KHz$		—	40	—	μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 8V$ to $18V$ $T_j = 25°C$		62	80	—	dB
		$f = 120Hz$, $V_i = 8V$ to $18V$ $0°C \leq T_j \leq 125°C$		62	—	—	
Dropout Voltage	V_d	$I_O = 1A$, $T_j = 25°C$		—	2.0	—	V
Peak Output Current	I_{peak}	$T_j = 25°C$		—	2.2	—	A
Short-Circuit Current	I_{sc}	$V_i = 35V$, $T_j = 25°C$		—	250	—	mA
Average TC of V_{out}	$\triangle V_O / \triangle T$	$I_O = 5mA$		—	−0.6	—	mV/°C
Output Resistance	R_O	$f = 1KHz$		—	17	—	mΩ

* Load and line regulation are specified at a constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA340T06

(Refer to test circuit, $0°C \leq T_j \leq 125°C$, $V_i = 11V$, $I_O = 0.5A$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	$T_j = 25°C$, $5mA \leq I_O \leq 1.0A$		5.75	6.00	6.26	V
		$5mA \leq I_O \leq 1.0A$, $PD \leq 15W$ $V_i = 8.5V$ to $21V$		5.70	—	6.30	
Line Regulation	$\triangle V_O$	$T_j = 25°C$, $V_i = 8V$ to $25V$		—	3	60	mV
		$V_i = 9V$ to $21V$		—	—	60	
		$I_O \leq 1A$	$V_i = 9V$ to $13V$	—	—	30	
			$V_i = 8.5V$ to $21V$ $T_j = 25°C$	—	—	60	
Load Regulation	$\triangle V_O$	$T_j = 25°C$	$5mA \leq I_O \leq 1.5A$	—	10	60	mV
			$0.25A \leq I_O \leq 0.75A$	—	—	30	
		$5mA \leq I_O \leq 1A$		—	—	60	
Quiescent Current	I_d	$I_O = 1A$	$T_j = 25°C$	—	—	8	mA
			$0°C \leq T_j \leq 125°C$	—	—	8.5	
Quiescent Current Change	$\triangle I_d$	$5mA \leq I_O \leq 1A$		—	—	0.5	mA
		$T_j = 25°C$ $I_O \leq 1A$, $V_i = 8.5V$ to $22V$		—	—	1.0	
		$V_i = 8V$ to $25V$		—	—	1.0	
Output Noise Voltage	V_n	$T_a = 25°C$, $f = 10Hz$ to $100KHz$		—	45	—	μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 9V$ to $19V$ $T_j = 25°C$		59	75	—	dB
		$f = 120Hz$, $V_i = 9V$ to $19V$ $0°C \leq T_j \leq 125°C$		59	—	—	
Dropout Voltage	V_d	$I_O = 1A$, $T_j = 25°C$		—	2.0	—	V
Peak Output Current	I_{peak}	$T_j = 25°C$		—	2.2	—	A
Short-Circuit Current	I_{sc}	$V_i = 35V$, $T_j = 25°C$		—	250	—	mA
Average TC of V_{out}	$\triangle V_O / \triangle T$	$I_O = 5mA$		—	−0.7	—	mV/°C
Output Resistance	R_O	$f = 1KHz$		—	18	—	mΩ

* Load and line regulation are specified at a constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA340T08

(Refer to test circuit, $0°C \leq T_j \leq 125°C$, $V_i = 14V$, $I_O = 0.5A$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	$T_j = 25°C$, $5mA \leq I_O \leq 1.0A$		7.70	8.00	8.30	V
		$5mA \leq I_O \leq 1.0A$, $PD \leq 15W$ $V_i = 10.5V$ to $23V$		7.60	—	8.40	
Line Regulation	$\triangle V_O$	$T_j = 25°C$, $V_i = 10.5V$ to $25V$		—	3	80	mV
		$V_i = 11V$ to $23V$		—	—	80	
		$I_O \leq 1A$	$V_i = 11.5V$ to $17V$	—	—	40	
			$V_i = 10.5V$ to $23V$ $T_j = 25°C$	—	—	80	
Load Regulation	$\triangle V_O$	$T_j = 25°C$	$5mA \leq I_O \leq 1.5A$	—	10	80	mV
			$0.25A \leq I_O \leq 0.75A$	—	—	40	
		$5mA \leq I_O \leq 1A$		—	—	80	
Quiescent Current	I_d	$I_O = 1A$	$T_j = 25°C$	—	—	8	mA
			$0°C \leq T_j \leq 125°C$	—	—	8.5	
Quiescent Current Change	$\triangle I_d$	$5mA \leq I_O \leq 1A$		—	—	0.5	mA
		$T_j = 25°C$ $I_O \leq 1A$, $V_i = 10.5V$ to $23V$		—	—	1.0	
		$V_i = 10.5V$ to $25V$		—	—	1.0	
Output Noise Voltage	V_n	$T_a = 25°C$, $f = 10Hz$ to $100KHz$		—	52	—	μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 11.5V$ to $21.5V$ $T_j = 25°C$		56	72	—	dB
		$f = 120Hz$, $V_i = 11.5V$ to $21.5V$ $0°C \leq T_j \leq 125°C$		56	—	—	
Dropout Voltage	V_d	$I_O = 1A$, $T_j = 25°C$		—	2.0	—	V
Peak Output Current	I_{peak}	$T_j = 25°C$		—	2.2	—	A
Short-Circuit Current	I_{sc}	$V_i = 35V$, $T_j = 25°C$		—	250	—	mA
Average TC of V_{out}	$\triangle V_O / \triangle T$	$I_O = 5mA$		—	−0.9	—	mV/°C
Output Resistance	R_O	$f = 1KHz$		—	20	—	mΩ

* Load and line regulation are specified at a constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA340T09

(Refer to test circuit, $0°C \leq T_j \leq 125°C$, $V_i = 15V$, $I_O = 0.5A$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	$T_j = 25°C$, $5mA \leq I_O \leq 1.0A$		8.65	9.00	9.35	V
		$5mA \leq I_O \leq 1.0A$, $PD \leq 15W$ $V_i = 11.5V$ to $24V$		8.60	—	9.40	
Line Regulation	$\triangle V_O$	$T_j = 25°C$, $V_i = 11.5V$ to $25V$		—	3	90	mV
		$V_i = 12V$ to $24V$		—	—	90	
		$I_O \leq 1A$	$V_i = 12V$ to $19V$	—	—	45	
			$V_i = 11.5V$ to $24V$ $T_j = 25°C$	—	—	90	
Load Regulation	$\triangle V_O$	$T_j = 25°C$	$5mA \leq I_O \leq 1.5A$	—	10	90	mV
			$0.25A \leq I_O \leq 0.75A$	—	—	45	
		$5mA \leq I_O \leq 1A$		—	—	90	
Quiescent Current	I_d	$I_O = 1A$	$T_j = 25°C$	—	—	8	mA
			$0°C \leq T_j \leq 125°C$	—	—	8.5	
Quiescent Current Change	$\triangle I_d$	$5mA \leq I_O \leq 1A$		—	—	0.5	mA
		$T_j = 25°C$ $I_O \leq 1A$, $V_i = 11.5V$ to $24V$		—	—	1.0	
		$V_i = 11.5V$ to $25V$		—	—	1.0	
Output Noise Voltage	V_n	$T_a = 25°C$, $f = 10Hz$ to $100KHz$		—	58	—	μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 12.5V$ to $22.5V$ $T_j = 25°C$		56	72	—	dB
		$f = 120Hz$, $V_i = 12.5V$ to $22.5V$ $0°C \leq T_j \leq 125°C$		56	—	—	
Dropout Voltage	V_d	$I_O = 1A$, $T_j = 25°C$		—	2.0	—	V
Peak Output Current	I_{peak}	$T_j = 25°C$		—	2.2	—	A
Short-Circuit Current	I_{sc}	$V_i = 35V$, $T_j = 25°C$		—	250	—	mA
Average TC of V_{out}	$\triangle V_O / \triangle T$	$I_O = 5mA$		—	−1.0	—	mV/°C
Output Resistance	R_O	$f = 1KHz$		—	22	—	mΩ

* Load and line regulation are specified at a constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA340T10

(Refer to test circuit, $0°C \leq T_j \leq 125°C$, $V_i = 16V$, $I_O = 0.5A$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	$T_j = 25°C$, $5mA \leq I_O \leq 1.0A$		9.60	10.00	10.40	V
		$5mA \leq I_O \leq 1.0A$, $PD \leq 15W$ $V_i = 12.5V$ to $25V$		9.50	—	10.50	
Line Regulation	$\triangle V_O$	$T_j = 25°C$, $V_i = 12.5V$ to $25V$		—	3	100	mV
		$V_i = 13V$ to $25V$		—	—	100	
		$I_O \leq 1A$	$V_i = 13V$ to $20V$	—	—	50	
			$V_i = 12.5V$ to $25V$ $T_j = 25°C$	—	—	100	
Load Regulation	$\triangle V_O$	$T_j = 25°C$	$5mA \leq I_O \leq 1.5A$	—	10	100	mV
			$0.25A \leq I_O \leq 0.75A$	—	—	50	
		$5mA \leq I_O \leq 1A$		—	—	100	
Quiescent Current	I_d	$I_O = 1A$	$T_j = 25°C$	—	—	8	mA
			$0°C \leq T_j \leq 125°C$	—	—	8.5	
Quiescent Current Change	$\triangle I_d$	$5mA \leq I_O \leq 1A$		—	—	0.5	mA
		$T_j = 25°C$ $I_O \leq 1A$, $V_i = 12.6V$ to $25V$		—	—	1.0	
		$V_i = 12.6V$ to $25V$		—	—	1.0	
Output Noise Voltage	V_n	$T_a = 25°C$, $f = 10Hz$ to $100KHz$		—	58	—	μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 13V$ to $23V$ $T_j = 25°C$		56	72	—	dB
		$f = 120Hz$, $V_i = 13V$ to $23V$ $0°C \leq T_j \leq 125°C$		56	—	—	
Dropout Voltage	V_d	$I_O = 1A$, $T_j = 25°C$		—	2.0	—	V
Peak Output Current	I_{peak}	$T_j = 25°C$		—	2.2	—	A
Short-Circuit Current	I_{sc}	$V_i = 35V$, $T_j = 25°C$		—	250	—	mA
Average TC of V_{out}	$\triangle V_O / \triangle T$	$I_O = 5mA$		—	−1.1	—	mV/°C
Output Resistance	R_O	$f = 1KHz$		—	24	—	mΩ

* Load and line regulation are specified at a constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA340T11

(Refer to test circuit, $0°C \leq T_j \leq 125°C$, $V_i = 18V$, $I_O = 0.5A$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	$T_j = 25°C$, $5mA \leq I_O \leq 1.0A$		11.60	11.00	11.40	V
		$5mA \leq I_O \leq 1.0A$, $PD \leq 15W$ $V_i = 13.5V$ to $26V$		10.50	—	11.50	
Line Regulation	$\triangle V_O$	$T_j = 25°C$, $V_i = 13.5V$ to $25V$		—	3	110	mV
		$V_i = 14V$ to $26V$		—	—	110	
		$I_O \leq 1A$	$V_i = 14V$ to $21V$	—	—	55	
			$V_i = 13.5V$ to $26V$ $T_j = 25°C$	—	—	110	
Load Regulation	$\triangle V_O$	$T_j = 25°C$	$5mA \leq I_O \leq 1.5A$	—	10	110	mV
			$0.25A \leq I_O \leq 0.75A$	—	—	55	
		$5mA \leq I_O \leq 1A$		—	—	110	
Quiescent Current	I_d	$I_O = 1A$	$T_j = 25°C$	—	—	8	mA
			$0°C \leq T_j \leq 125°C$	—	—	8.5	
Quiescent Current Change	$\triangle I_d$	$5mA \leq I_O \leq 1A$		—	—	0.5	mA
		$T_j = 25°C$ $I_O \leq 1A$, $V_i = 13.7V$ to $26V$		—	—	1.0	
		$V_i = 13.5V$ to $25V$		—	—	1.0	
Output Noise Voltage	V_n	$T_a = 25°C$, $f = 10Hz$ to $100KHz$		—	70	—	μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 14V$ to $24V$ $T_j = 25°C$		55	72	—	dB
		$f = 120Hz$, $V_i = 14V$ to $24V$ $0°C \leq T_j \leq 125°C$		55	—	—	
Dropout Voltage	V_d	$I_O = 1A$, $T_j = 25°C$		—	2.0	—	V
Peak Output Current	I_{peak}	$T_j = 25°C$		—	2.2	—	A
Short-Circuit Current	I_{sc}	$V_i = 35V$, $T_j = 25°C$		—	250	—	mA
Average TC of V_{out}	$\triangle V_O / \triangle T$	$I_O = 5mA$		—	−1.3	—	mV/°C
Output Resistance	R_O	$f = 1KHz$		—	26	—	mΩ

* Load and line regulation are specified at a constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA340T12

(Refer to test circuit, $0°C \leq T_j \leq 125°C$, $V_i = 19V$, $I_O = 0.5A$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	$T_j = 25°C$, $5mA \leq I_O \leq 1.0A$		11.50	12.00	12.50	V
		$5mA \leq I_O \leq 1.0A$, $PD \leq 15W$ $V_i = 14.5V$ to $27V$		11.40	—	12.60	
Line Regulation	$\triangle V_O$	$T_j = 25°C$, $V_i = 14.5V$ to $30V$		—	4	120	mV
		$V_i = 15V$ to $27V$		—	—	120	
		$I_O \leq 1A$	$V_i = 16V$ to $22V$	—	—	60	
			$V_i = 14.6V$ to $27V$ $T_j = 25°C$	—	—	120	
Load Regulation	$\triangle V_O$	$T_j = 25°C$	$5mA \leq I_O \leq 1.5A$	—	12	120	mV
			$0.25A \leq I_O \leq 0.75A$	—	—	60	
		$5mA \leq I_O \leq 1A$		—	—	120	
Quiescent Current	I_d	$I_O = 1A$	$T_j = 25°C$	—	—	8	mA
			$0°C \leq T_j \leq 125°C$	—	—	8.5	
Quiescent Current Change	$\triangle I_d$	$5mA \leq I_O \leq 1A$		—	—	0.5	mA
		$T_j = 25°C$ $I_O \leq 1A$, $V_i = 14.8V$ to $27V$		—	—	1.0	
		$V_i = 14.5V$ to $30V$		—	—	1.0	
Output Noise Voltage	V_n	$T_a = 25°C$, $f = 10Hz$ to $100KHz$		—	75	—	μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 15V$ to $25V$ $T_j = 25°C$		55	72	—	dB
		$f = 120Hz$, $V_i = 15V$ to $25V$ $0°C \leq T_j \leq 125°C$		55	—	—	
Dropout Voltage	V_d	$I_O = 1A$, $T_j = 25°C$		—	2.0	—	V
Peak Output Current	I_{peak}	$T_j = 25°C$		—	2.2	—	A
Short-Circuit Current	I_{sc}	$V_i = 35V$, $T_j = 25°C$		—	250	—	mA
Average TC of V_{out}	$\triangle V_O / \triangle T$	$I_O = 5mA$		—	−1.5	—	mV/°C
Output Resistance	R_O	$f = 1KHz$		—	28	—	mΩ

* Load and line regulation are specified at a constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA340T15

(Refer to test circuit, $0°C \leq T_j \leq 125°C$, $V_i = 23V$, $I_O = 0.5A$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	$T_j = 25°C$, $5mA \leq I_O \leq 1.0A$		14.40	15.00	15.60	V
		$5mA \leq I_O \leq 1.0A$, $PD \leq 15W$ $V_i = 17.5V$ to $30V$		14.25	—	15.75	
Line Regulation	$\triangle V_O$	$T_j = 25°C$, $V_i = 17.5V$ to $30V$		—	4	150	mV
		$V_i = 18.5V$ to $30V$		—	—	150	
		$I_O \leq 1A$	$V_i = 20V$ to $26V$	—	—	60	
			$V_i = 17.7V$ to $30V$ $T_j = 25°C$	—	—	120	
Load Regulation	$\triangle V_O$	$T_j = 25°C$	$5mA \leq I_O \leq 1.5A$	—	12	150	mV
			$0.25A \leq I_O \leq 0.75A$	—	—	75	
		$5mA \leq I_O \leq 1A$		—	—	150	
Quiescent Current	I_d	$I_O = 1A$	$T_j = 25°C$	—	—	8	mA
			$0°C \leq T_j \leq 125°C$	—	—	8.5	
Quiescent Current Change	$\triangle I_d$	$5mA \leq I_O \leq 1A$		—	—	0.5	mA
		$T_j = 25°C$ $I_O \leq 1A$, $V_i = 17.9V$ to $30V$		—	—	1.0	
		$V_i = 17.5V$ to $30V$		—	—	1.0	
Output Noise Voltage	V_n	$T_a = 25°C$, $f = 10Hz$ to $100KHz$		—	90	—	μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 18.5V$ to $28.5V$ $T_j = 25°C$		54	70	—	dB
		$f = 120Hz$, $V_i = 15V$ to $25V$ $0°C \leq T_j \leq 125°C$		54	—	—	
Dropout Voltage	V_d	$I_O = 1A$, $T_j = 25°C$		—	2.0	—	V
Peak Output Current	I_{peak}	$T_j = 25°C$		—	2.2	—	A
Short-Circuit Current	I_{sc}	$V_i = 35V$, $T_j = 25°C$		—	250	—	mA
Average TC of V_{out}	$\triangle V_O / \triangle T$	$I_O = 5mA$		—	−1.8	—	mV/°C
Output Resistance	R_O	$f = 1KHz$		—	29	—	mΩ

* Load and line regulation are specified at a constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA340T18

(Refer to test circuit, $0°C \leq T_j \leq 125°C$, $V_i = 27V$, $I_O = 0.5A$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	$T_j = 25°C$, $5mA \leq I_O \leq 1.0A$		17.30	18.00	18.70	V
		$5mA \leq I_O \leq 1.0A$, $PD \leq 15W$ $V_i = 21V$ to $33V$		17.10	—	18.90	
Line Regulation	$\triangle V_O$	$T_j = 25°C$, $V_i = 21V$ to $33V$		—	5	180	mV
		$V_i = 22V$ to $33V$		—	—	180	
		$I_O \leq 1A$	$V_i = 24V$ to $30V$	—	—	90	
			$V_i = 21V$ to $33V$ $T_j = 25°C$	—	—	180	
Load Regulation	$\triangle V_O$	$T_j = 25°C$	$5mA \leq I_O \leq 1.5A$	—	12	180	mV
			$0.25A \leq I_O \leq 0.75A$	—	—	90	
		$5mA \leq I_O \leq 1A$		—	—	180	
Quiescent Current	I_d	$I_O = 1A$	$T_j = 25°C$	—	—	8	mA
			$0°C \leq T_j \leq 125°C$	—	—	8.5	
Quiescent Current Change	$\triangle I_d$	$5mA \leq I_O \leq 1A$		—	—	0.5	mA
		$T_j = 25°C$ $I_O \leq 1A$, $V_i = 21.5V$ to $33V$		—	—	1.0	
		$V_i = 21V$ to $33V$		—	—	1.0	
Output Noise Voltage	V_n	$T_a = 25°C$, $f = 10Hz$ to $100KHz$		—	110	—	μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 22V$ to $32V$ $T_j = 25°C$		53	69	—	dB
		$f = 120Hz$, $V_i = 22V$ to $32V$ $0°C \leq T_j \leq 125°C$		53	—	—	
Dropout Voltage	V_d	$I_O = 1A$, $T_j = 25°C$		—	2.0	—	V
Peak Output Current	I_{peak}	$T_j = 25°C$		—	2.2	—	A
Short-Circuit Current	I_{sc}	$V_i = 35V$, $T_j = 25°C$		—	250	—	mA
Average TC of V_{out}	$\triangle V_O / \triangle T$	$I_O = 5mA$		—	−2.2	—	mV/°C
Output Resistance	R_O	$f = 1KHz$		—	32	—	mΩ

* Load and line regulation are specified at a constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA340T24

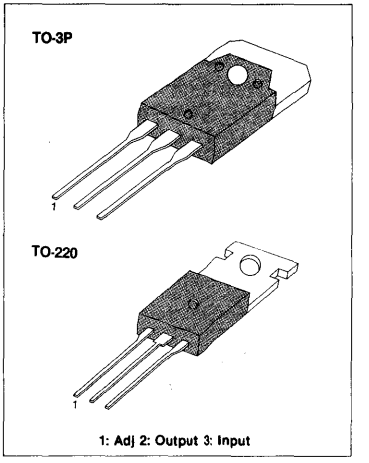
(Refer to test circuit, $0°C \leq T_j \leq 125°C$, $V_i = 33V$, $I_O = 0.5A$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	$T_j = 25°C$, $5mA \leq I_O \leq 1.0A$		23.00	24.00	25.00	V
		$5mA \leq I_O \leq 1.0A$, $PD \leq 15W$ $V_i = 27V$ to $38V$		22.80	—	25.20	
Line Regulation	$\triangle V_O$	$T_j = 25°C$, $V_i = 27V$ to $38V$		—	5	240	mV
		$V_i = 28V$ to $38V$		—	—	240	
		$I_O \leq 1A$	$V_i = 30V$ to $36V$	—	—	120	
			$V_i = 27V$ to $38V$ $T_j = 25°C$	—	—	240	
Load Regulation	$\triangle V_O$	$T_j = 25°C$	$5mA \leq I_O \leq 1.5A$	—	12	240	mV
			$0.25A \leq I_O \leq 0.75A$	—	—	120	
		$5mA \leq I_O \leq 1A$		—	—	240	
Quiescent Current	I_d	$I_O = 1A$	$T_j = 25°C$	—	—	8	mA
			$0°C \leq T_j \leq 125°C$	—	—	8.5	
Quiescent Current Change	$\triangle I_d$	$5mA \leq I_O \leq 1A$		—	—	0.5	mA
		$T_j = 25°C$ $I_O \leq 1A$, $V_i = 28V$ to $38V$		—	—	1.0	
		$V_i = 27V$ to $38V$		—	—	1.0	
Output Noise Voltage	V_n	$T_a = 25°C$, $f = 10Hz$ to $100KHz$		—	170	—	μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 28V$ to $38V$ $T_j = 25°C$		50	66	—	dB
		$f = 120Hz$, $V_i = 28V$ to $38V$ $0°C \leq T_j \leq 125°C$		50	—	—	
Dropout Voltage	V_d	$I_O = 1A$, $T_j = 25°C$		—	2.0	—	V
Peak Output Current	I_{peak}	$T_j = 25°C$		—	2.2	—	A
Short-Circuit Current	I_{sc}	$V_i = 35V$, $T_j = 25°C$		—	250	—	mA
Average TC of V_{out}	$\triangle V_O / \triangle T$	$I_O = 5mA$		—	−2.8	—	mV/°C
Output Resistance	R_O	$f = 1KHz$		—	37	—	mΩ

* Load and line regulation are specified at a constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

3A ADJUSTABLE POSITIVE VOLTAGE REGULATOR

The KA350 is adjustable 3-terminal positive voltage regulator capable of supplying in excess of 3.0A over an output voltage range of 1.2V to 33V. This voltage regulator is exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof. All overload protection circuitry remains fully functional even if the adjustment terminal is accidentally disconnected.

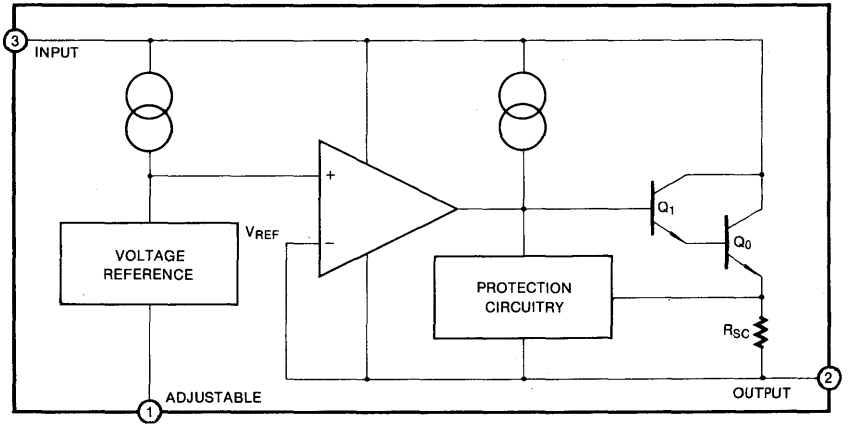


FEATURES

- **Output adjustable between 1.2V and 33V**
- **Guaranteed 3A output current**
- **Internal thermal overload protection**
- **Load regulation typically 0.1%**
- **Line regulation typically 0.005%/V**
- **Internal short-circuit current limiting constant with temperature.**
- **Output transistor safe-area compensation**
- **Floating operation for high voltage application**
- **Standard 3-lead transistor package**
- **Eliminates stocking many fixed voltages**

Device	Package	Operating Temperature
KA350H	TO-3P	0 ~ 125°C
KA350T	TO-220	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input-Output Voltage Differential	$V_{IN} - V_{OUT}$	35	V_{DC}
Lead Temperature (Soldering, 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	Internally limited	
Operating Junction Temperature Range	T_{opr}	0 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

($V_{IN} - V_{OUT} = 5V$, $I_{OUT} = 1.5A$, $T_j = 0°C$ to $125°C$; P_{max}, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	$\triangle V_o$	$Ta = 25°C$, $3V \leq V_I - V_o \leq 35V$ (Note 1)		0.005	0.03	%/V
Load Regulation	$\triangle V_o$	$Ta = 25°C$, $10mA \leq I_o \leq 3A$ $V_o \leq 5V$ (Note 1) $V_o \geq 5V$ (Note 1)		 5 0.1	 25 0.5	 mV %
Adjustment Pin Current	I_{adj}			50	100	μA
Adjustment Pin Current Change	$\triangle I_{adj}$	$3V \leq V_I - V_o \leq 35V$, $10mA \leq I_L \leq 3A$, $P_D \leq P_{MAX}$		0.2	5.0	μA
Thermal Regulation	REG_{therm}	Pulse = 20mS, $Ta = 25°C$		0.002		%/W
Reference Voltage	V_{REF}	$3V \leq V_I - V_o \leq 35V$, $10mA \leq I_o \leq 3A$, $P \leq 30W$	1.2	1.25	1.30	V
Line Regulation	$\triangle V_o$	$3.0V \leq V_I - V_o \leq 35V$		0.02	0.07	%/V
Load Regulation	$\triangle V_o$	$10mA \leq I_O \leq 3.0A$ $V_o \leq 5.0V$ $V_O \geq 5.0V$		 20 0.3	 70 1.5	 mV %
Temperature Stability	T_S	$T_j = 0°C$ to $125°C$		1.0		%
Maximum Output Current	I_{MAX}	$V_I - V_o \leq 10V$, $P_D \leq P_{MAX}$	3.0	4.5		A
		$V_I - V_o = 30V$, $P_D \leq P_{MAX}$, $Ta = 25°C$	0.25	1.0		A
Minimum Load Current	I_{MIN}	$V_I - V_o = 35V$		3.5	10	mA
RMS Noise, % of V_{OUT}	V_N	$10Hz \leq f \leq 10KHz$, $Ta = 25°C$		0.003		%
Ripple Rejection	RR	$V_o = 10V$, $f = 120Hz$, $C_{adj} = 0$ $C_{adj} = 10\mu F$	 66	 65 80		 dB dB
Long-Term Stability	S	$T_j = 125°C$		0.3	1	%

Note 1: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL PERFORMANCE CHARACTERISTIC

Fig. 1 LOAD REGULATION

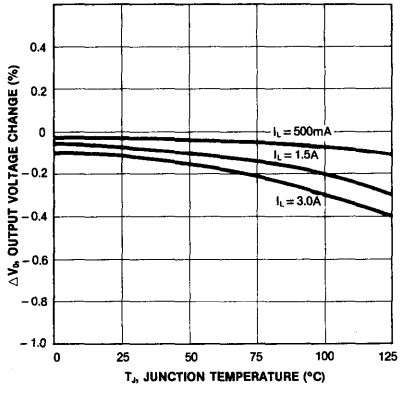


Fig. 2 WRREN UMIT

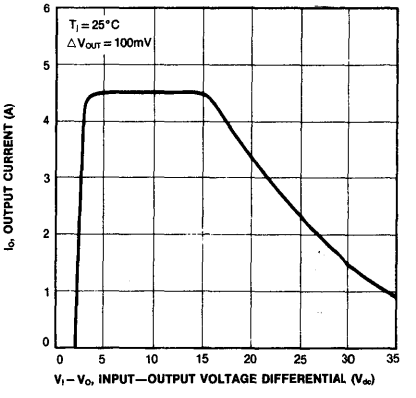


Fig. 3 ADJUSTMENT PIN CURRENT

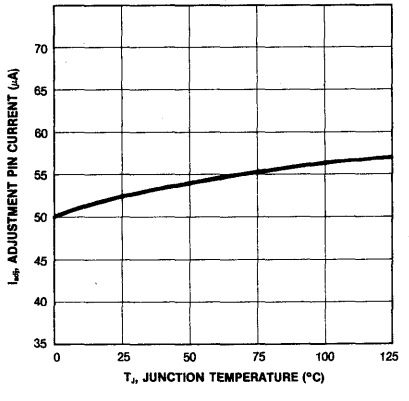


Fig. 4 DROPOUT VOLTAGE

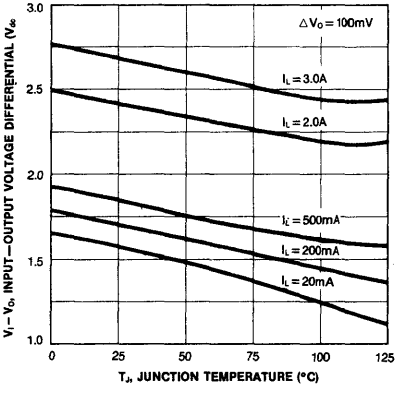


Fig. 5 TEMPERATURE STABILITY

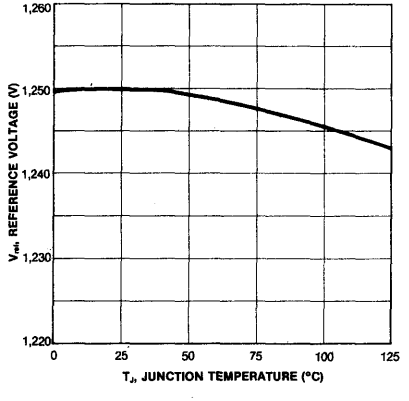
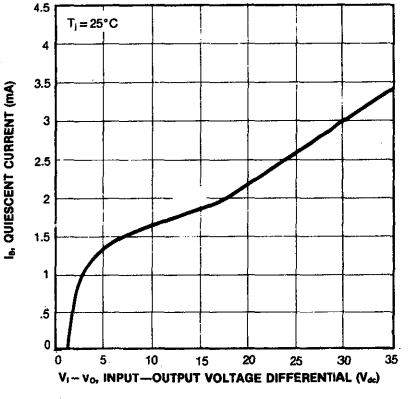


Fig. 6 MINIMUM LOAD CURRENT



TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 7 RIPPLE REJECTION vs V_{OUT}

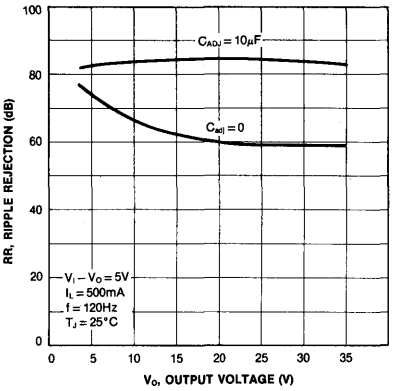


Fig. 8 RIPPLE REJECTION vs I_{OUT}

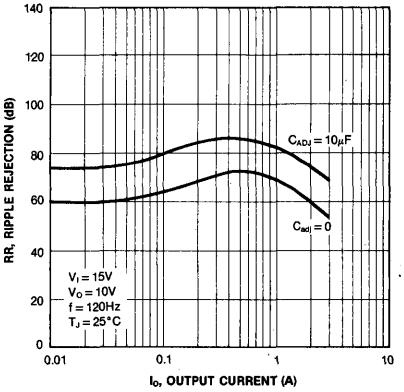


Fig. 9 RIPPLE REJECTION vs FREQUENCY

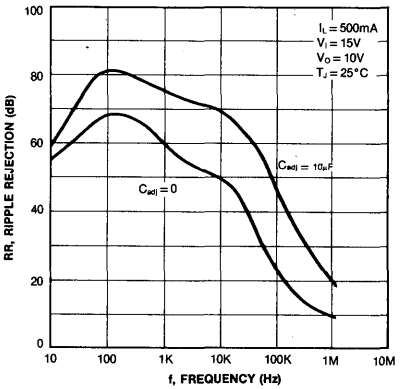


Fig. 10 OUTPUT IMPEDANCE

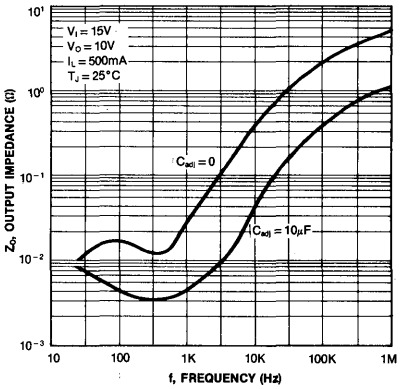


Fig. 11 LINE TRANSIENT RESPONSE

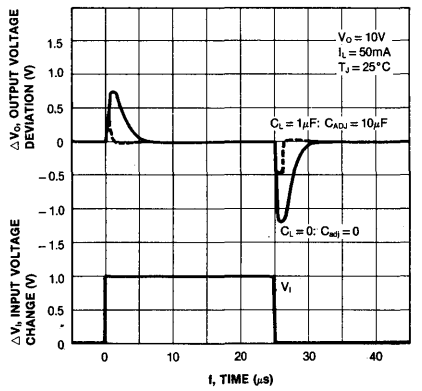
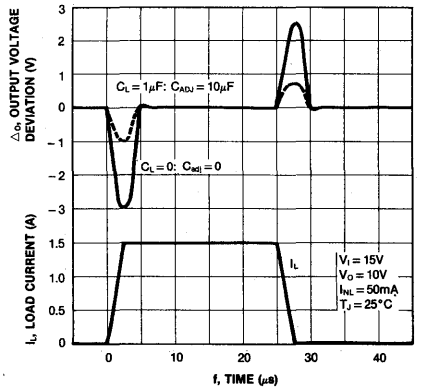


Fig. 12 LOAD TRANSIENT RESPONSE



APPLICATION INFORMATION

STANDARD APPLICATION

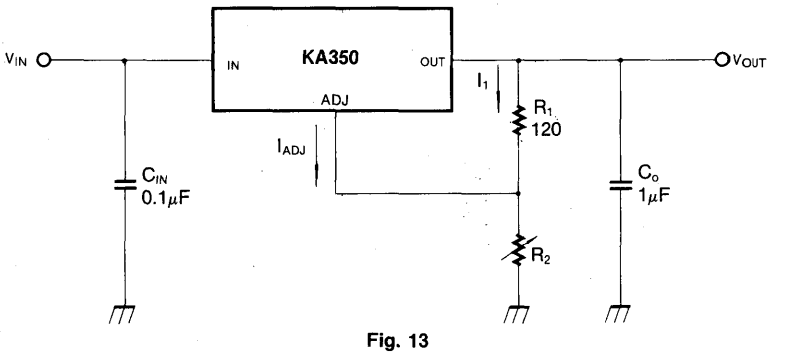


Fig. 13

C_{in}: C_{in} is required if regulator is located an appreciable distance from power supply filter.
C_o: Output capacitors in the range of 1μF to 100μF of aluminum or tantalum electrontic are commonly used to provide improved output impedance and rejection of transients.

In operation, KA350 develops a nominal 1.25V reference voltage, V_{ref}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R_1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R_2, giving an output voltage of

$$V_{out} = 1.25V\ (1 + \frac{R_2}{R_1}) + I_{ADJ}\ R_2$$

Since I_{ADJ} current (less than 100μA) from the adjustment terminal represents an error term, the KA350 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output voltage will rise.

Since the KA350 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltage with respect to ground is possible.

TYPICAL APPLICATIONS

Fig. 14 LIGHT CONTROLLER

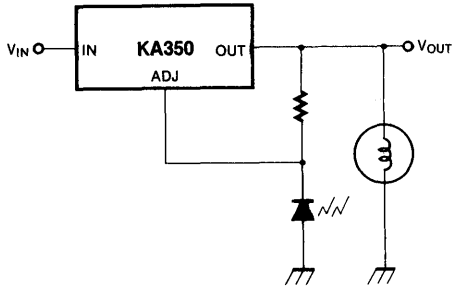


Fig. 15 PRECISION POWER REGULATOR WITH LOW TEMPERATURE COEFFICIENT

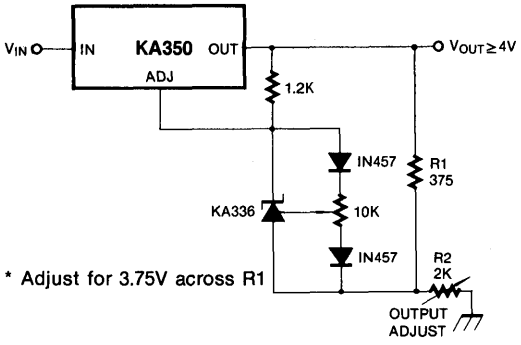


Fig. 16 ADJUSTABLE REGULATOR WITH IMPROVED RIPPLE REJECTION

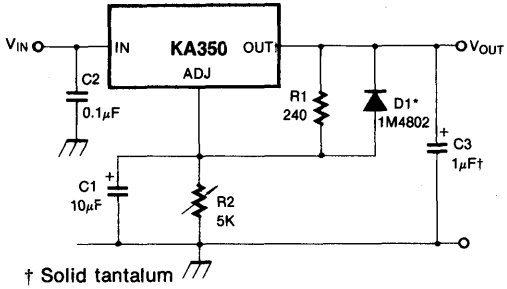


Fig. 17 SLOW TURN-ON 15V REGULATOR

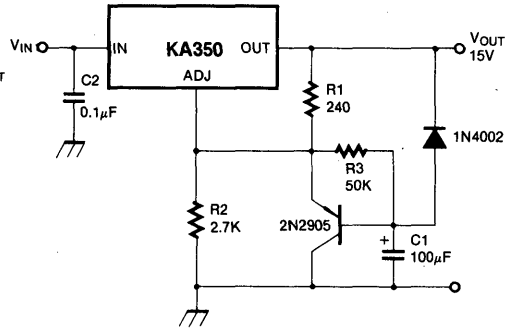


Fig. 18 0 TO 30V REGULATOR

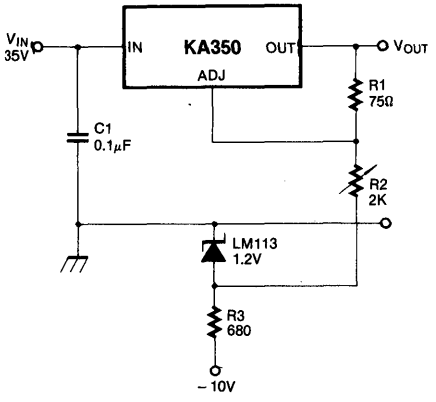
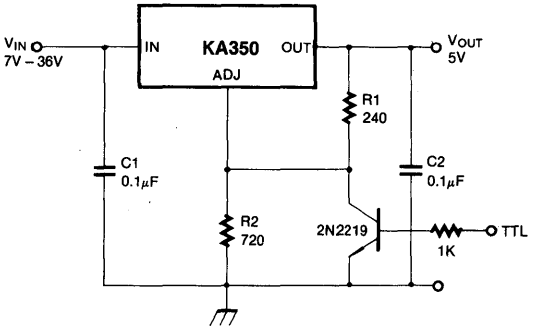


Fig. 19 5V LOGIC REGULATOR WITH ELECTRONIC SHUTDOWN*



TYPICAL APPLICATIONS (Continued)

Fig. 20 PRECISION CURRENT LIMITER

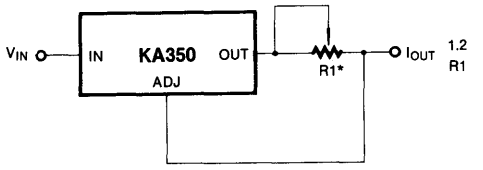


Fig. 21 1.2V – 20V REGULATOR WITH MINIMUM PROGRAM CURRENT

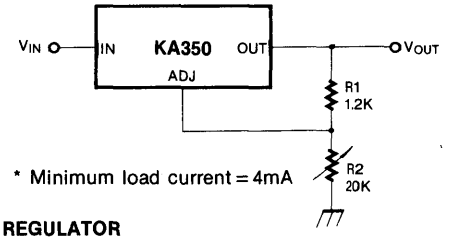


Fig. 22 5A CONSTANT VOLTAGE/CONSTANT CURRENT REGULATOR

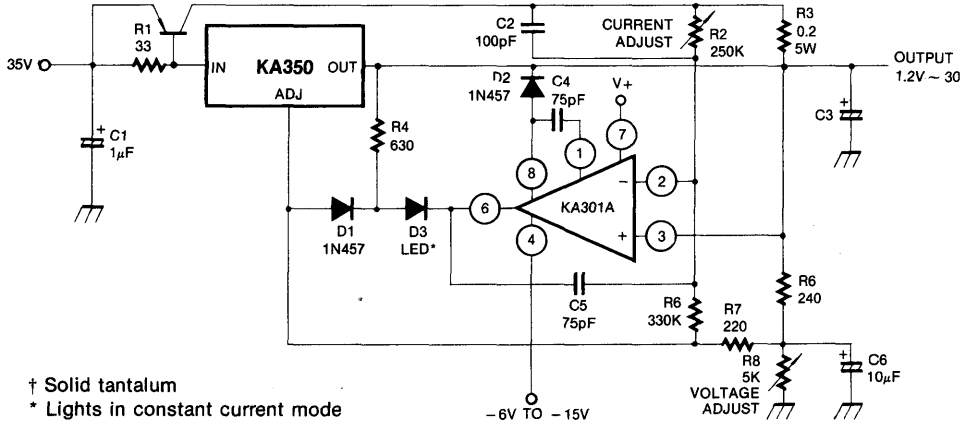


Fig. 23 12V BATTERY CHARGER

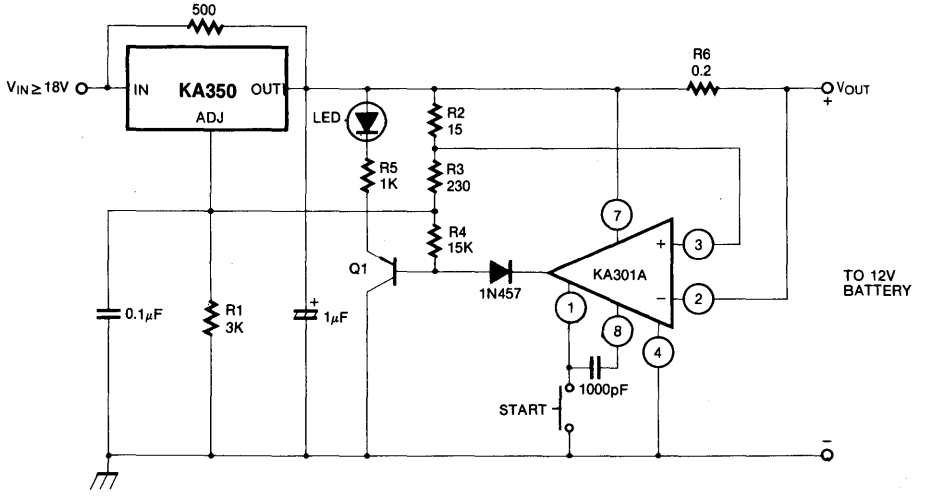


Fig. 24 TRACKING PREREGULATOR

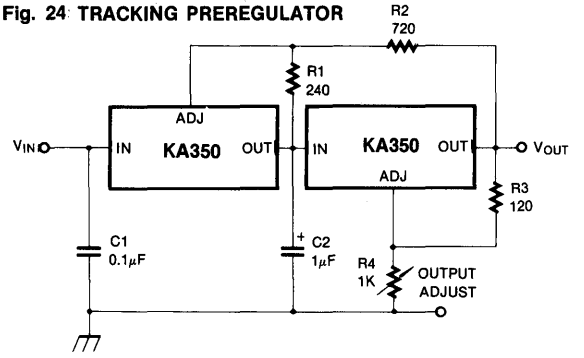


Fig. 25 3A CURRENT REGULATOR

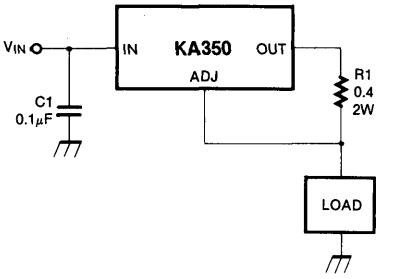
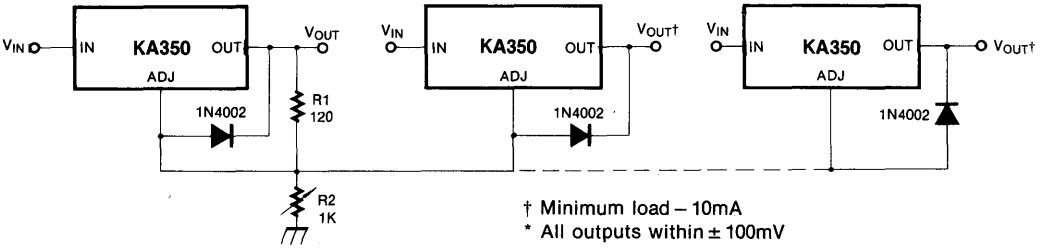


Fig. 26 ADJUSTING MULTIPLE ON-CARD REGULATORS WITH SINGLE CONTROL*



† Minimum load – 10mA
* All outputs within ± 100mV

Fig. 27 AC VOLTAGE REGULATOR

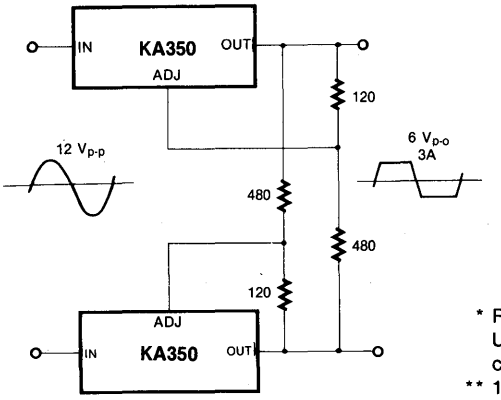
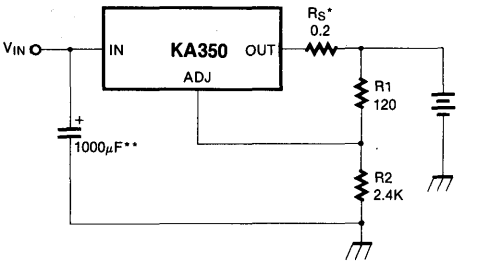


Fig. 28 SIMPLE 12V BATTERY CHARGER

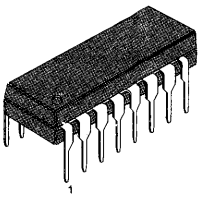


* R_S – sets output impedance of charger $Z_{OUT} = R_S\left(1 + \frac{R_2}{R_1}\right)$
Use of R_S allows low charging rates with fully charged battery.
** 1000μF is recommended to filter out any input transients.

REGULATOR PULSE WIDTH MODULATOR

The KA3524 regulating pulse width modulator contains all of the control circuitry necessary to implement switching regulators of either polarity, transformer coupled DC to DC converters, transformerless polarity converters and voltage doublers, as well as other power control applications. This device includes a 5V voltage regulator capable of supplying up to 50mA to external circuitry, a control amplifier, an oscillator, a pulse width modulator, a phase splitting flip-flop, dual alternating output switch transistors, and current limiting and shut-down circuitry. Both the regulator output transistor and each output switch are internally current limiting and, to limit junction temperature, an internal thermal shutdown circuit is employed.

16 DIP



FEATURES

- **Complete PWM power control circuitry**
- **Operation beyond 100KHz**
- **2% frequency stability with temperature**
- **Total quiescent current less than 10mA**
- **Single ended or push-pull outputs**
- **Current limit amplifier provides external component protection**
- **On-chip protection against excessive junction temperature and output current**
- **5V, 50mA linear regulator output available to user**

ORDERING INFORMATION

Device	Package	Operation Temperature
KA3524N	16 DIP	0 ~ 70°C
**KA2524N	16 DIP	-25 ~ 85°C

** Under development

BLOCK DIAGRAM

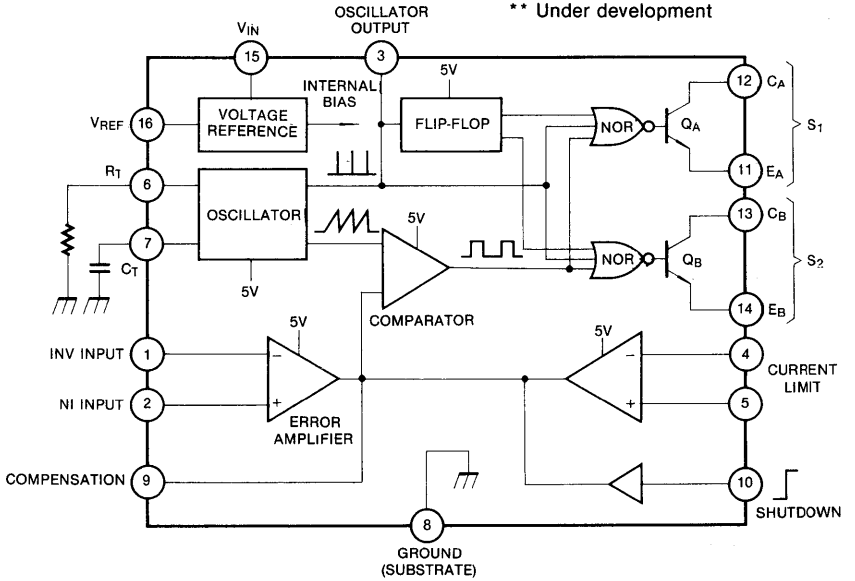


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Reference Output Current	I_{REF}	50	mA
Output Current (Each Output)	I_O	100	mA
Oscillator Changing Current (pin 6 or 7)	I_{charge}	5	mA
Lead Temperature (Soldering, 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	1000	mW
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 20V, f = 20KHz, Ta = 0 to 70°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
REFERENCE SECTION						
Output Voltage	V_O		4.6	5.0	5.4	V
Line Regulation	$\triangle V_O$	V_{IN} = 8 ~ 40V		10	30	mV
Load Regulation	$\triangle V_O$	I_L = 0 ~ 20mA		20	50	mV
Ripple Rejection	RR	f = 120Hz, Ta = 25°C		66		dB
Short-Circuit Output Current	I_{SC}	V_{ref} = 0, Ta = 25°C		100		mA
Temperature Stability	T_S			0.3	1	%
Long Term Stability	S	Ta = 25°C		20		mV/Khr
OSCILLATOR SECTION						
Maximum Frequency	f_{MAX}	CT = 0.001μF, RT = 2KΩ		350		KHz
Initial Accuracy		RT and CT constant		5		%
Frequency Change with Voltage	$\triangle f$	V_{IN} = 8 ~ 40V, Ta = 25°C			1	%
Frequency Change with Temperature	$\triangle f$	Over operating temperature range			2	%
Output Amplitude (Pin 3)	VA3	Ta = 25°C		3.5		V
Output Pulse Width (Pin 3)	V3PW	CT = 0.01μF, Ta = 25°C		0.5		μs
ERROR AMPLIFIER SECTION						
Input Offset Voltage	V_{IO}	VCM = 2.5V		2	10	mV
Input Bias Current	I_{IB}	VCM = 2.5V		2	10	μA
Open Loop Voltage Gain	A_{VO}		60	80		dB
Common-Mode Input Voltage Range	V_{CR}	Ta = 25°C	1.8		3.4	V
Common-Mode Rejection Ratio	CMRR	Ta = 25°C		70		dB
Small Signal Bandwidth	BW	A_V = 0dB, Ta = 25°C		3		MHz
Output Voltage Swing	V_{OSW}	Ta = 25°C	0.5		3.8	V

ELECTRICAL CHARACTERISTICS (Continued)

(V_{IN} = 20V, f = 20KHz, Ta = 0 ~ 70°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
COMPARATOR SECTION						
Maximum Duty Cycle	DC_{max}	% Each output on	45			%
Input Threshold (Pin 9)	V_{TH1}	Zero duty cycle		1		V
Input Threshold (Pin 9)	V_{TH2}	Maximum duty cycle		3.5		V
Input Bias Current	I_B			1		μA
CURRENT LIMITING SECTION						
Sense Voltage	V_{sense}	V(Pin 2) – V(Pin 1) ≥ 50mV Pin 9 = 2V, Ta = 25°C	180	200	220	mV
Sense Voltage T.C.				0.2		mV/°C
Common-Mode Voltage			0.7		1	V
OUTPUT SECTION (EACH OUTPUT)						
Collector-Emitter Voltage	V_{CEO}		40			V
Collector Leakage Current	I_{LKg}	V_{CE} = 40V		0.1	50	μA
Saturation Voltage	V_{SAT}	IC = 50mA		1	2	V
Emitter Output Voltage	V_E	V_{IN} = 20V,	17	18		V
Rise Time (10% to 90%)	t_r	RC = 2KΩ, Ta = 25°C		0.2		μs
Fall Time (90% to 10%)	t_f	RC = 2KΩ, Ta = 25°C		0.1		μs
Total Standby Current	I_{STD}	V_{IN} = 40V, PINS 1, 4, 7, 8, 11 and 14 are grounded, Pin 2 = 2V All other inputs and outputs open		5	10	mA

APPLICATION INFORMATION

Voltage Reference

An internal series regulator provides a nominal 5 volt output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5 volt supply by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5 volt source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher current with an external PNP as shown in Figure 2.

EXPANDED REFERENCE CURRENT CAPABILITY

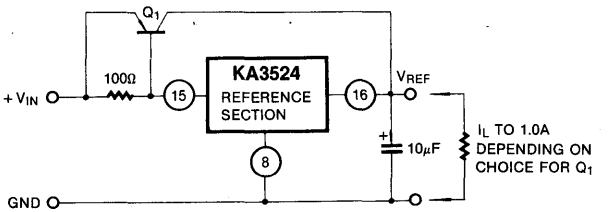


Fig. 2

Oscillator

The oscillator in the KA3524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to $3.6V \div R_T$ and should be kept within the range of approximately 30μA to 2mA, i.e., $1.8K < R_T < 100K$. The range of values for C_T also has limits as the discharge time of C_T determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 6. A pulse width below approximately 0.5 microseconds may allow faise triggering of one output by removing the blanking pulse prior to the flip-flops reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance (= 100pF) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 0.1 microfarad.

The oscillator period is approximately $t = R_T C_T$ where t is in microseconds when R_T = ohms and C_T = microfarads. The use of Figure 7 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each outputs duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the KA3524 to an external clock, a pulse of = +3 volts may be applied to the oscillator output terminal with $R_T C_T$ set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2K ohms.

If two or more KA3524s must be synchronized together, one must be designated as master with its $R_T C_T$ set for the correct period. The slaves should each have an $R_T C_T$ set for approximately 10% longer period than the master with the added requirement that C_T (slave) = one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse—which occurs first and has a wider pulse width—will reset the slave units.

Error Amplifier

This circuit is a simple differential-input, transconductance amplifier. The output is the compensation terminal, pin 9, which is a high impedance node ($R_L = 5M\Omega$). The gain is

$$A_V = gmR_L = \frac{8I_C R_L}{2K_T} = .002\ R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from pin 9 to ground, as shown in Figure 8.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 5 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain cross-over at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly power frequency. Therefore, the best stabilizing network is a series R-C combination between pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50KΩ plus .001 microfarad.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5 volt reference voltage must be divided down as shown in Figure 3. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open loop test circuit.

Current Limiting

The current limiting circuitry of the KA3524 is shown in Figure 4.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R_1:

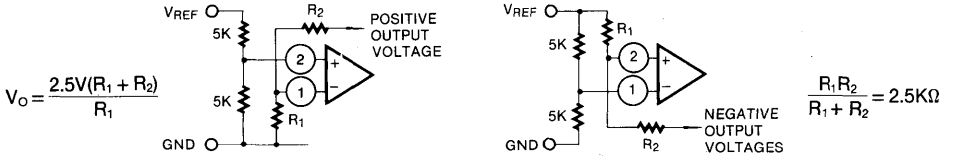
$$\text{Threshold} = V_{BE}(Q1) + I_1R_2 - V_{BE}(Q2)$$
$$= I_1R_2 = 200mV$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur. Another application is to ground pin 5 and use pin 4 as an additional shutdown terminal: i.e., the output will be off with pin 4 open and on when it is grounded. Finally, foldback current limitting can be provided with the network of Figure 5. This circuit can reduce the shortcircuit current (I_{SC}) to approximately onethird the maximum available output current (I_{MAX}).

Fig. 3 ERROR AMPLIFIER BIASING CIRCUITS



Note change in input connections for opposite polarity outputs.

Fig. 4 CURRENT LIMITING CIRCUITRY OF THE KA3524

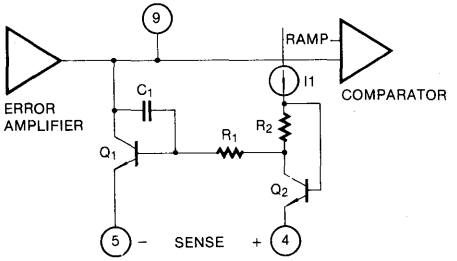
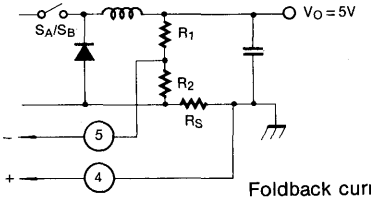


Fig. 5 FOLDBACK CURRENT LIMITING



$$I_{MAX} = \frac{1}{R_S} \quad V_{TH} + \frac{V_OR_2}{R_1 + R_2}$$

$$I_{SC} = \frac{V_{TH}}{R_S} \quad \text{where}$$

$$V_{TH} = 200mV$$

Foldback current limiting can be used to reduce power dissipation under shorted output conditions

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 6 OUTPUT STAGE DEAD TIME AS A FUNCTION OF THE TIMING CAPACITOR VALUE

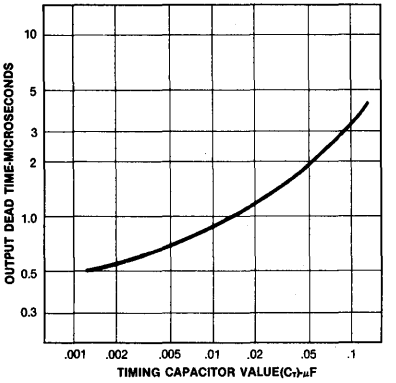


Fig. 7 OSCILLATOR PERIOD AS A FUNCTION OF R_T AND C_T

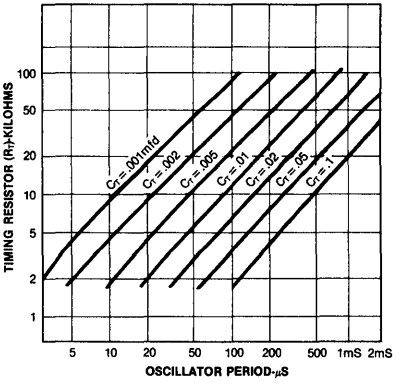
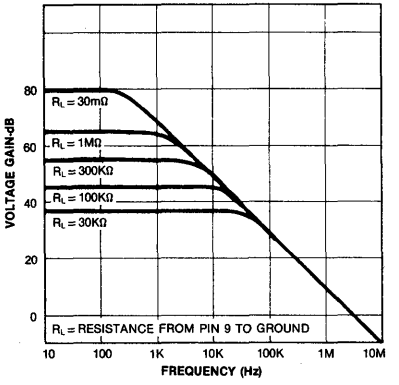


Fig. 8 AMPLIFIES OPEN-LOOP GAIN AS A FUNCTION OF FREQUENCY AND LOADING ON PIN 9



TYPICAL APPLICATION

Fig. 9 CAPACITOR-DIODE OUTPUT CIRCUIT

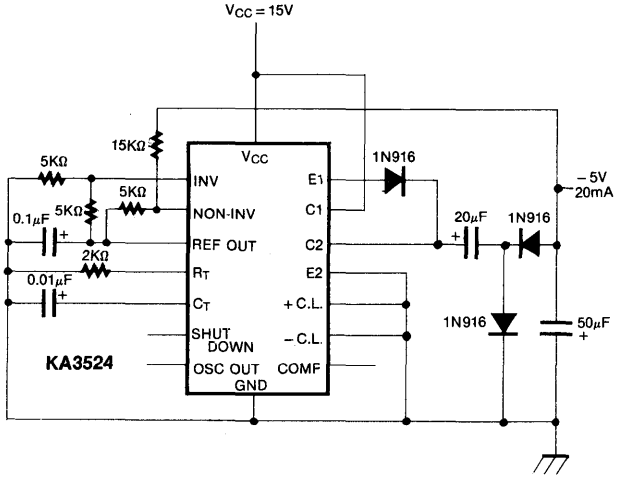


Fig. 10 FLYBACK CONVERTER CIRCUIT

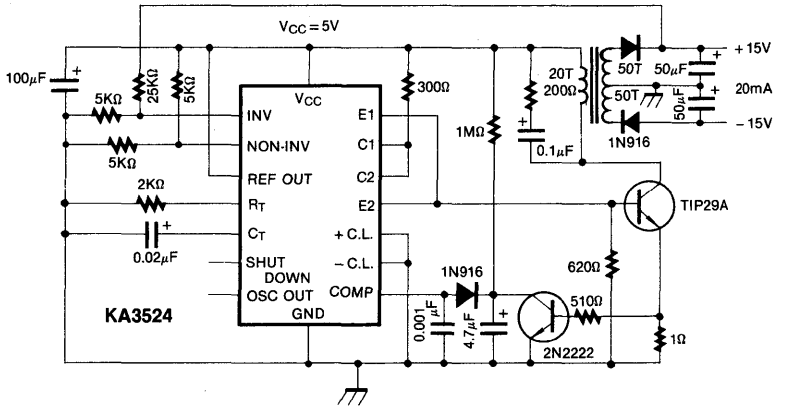


Fig. 11 SINGLE-ENDED LC CIRCUIT

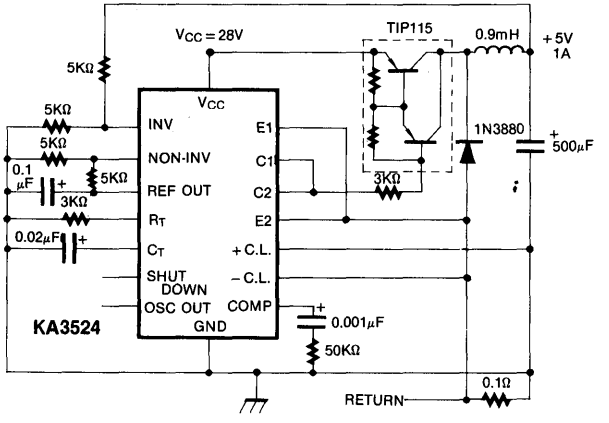
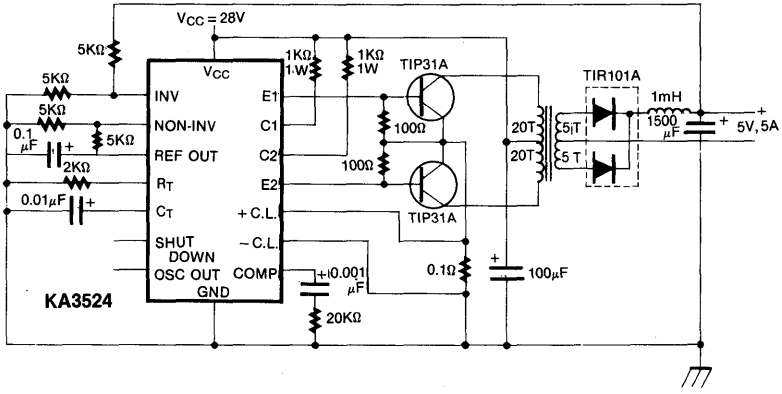


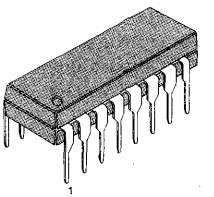
Fig. 12 PUSH-PULL TRANSFORMER-COUPLED CIRCUIT



REGULATOR PULSE WIDTH MODULATOR

The KA7500 is used for control circuit of pulse width modulation switching regulator. KA7500 consists of 5V reference voltage circuit, two error amplifiers, flip-flop, output control circuit, PWM comparator, dead time comparator, and oscillator. This device can be operated in the range of switching frequency, 1KHz to 300KHz.

16 DIP



FEATURES

- ***Internal regulator provides a stable 5V reference supply trimmed to 1%***
- **Uncommitted output TR for 200mA sink or source *current***
- **Output control for push-pull or single-ended operation**
- ***Variable duty cycle by dead time control (pin 4)***
- **Complete PWM control circuitry**
- **On-chip oscillator with master or slave operation**
- **Internal circuitry prohibits double pulse at either output**

ORDERING INFORMATION

Device	Package	Operation Temperature
KA7500	16 DIP	0 ~ 70°C

BLOCK DIAGRAM

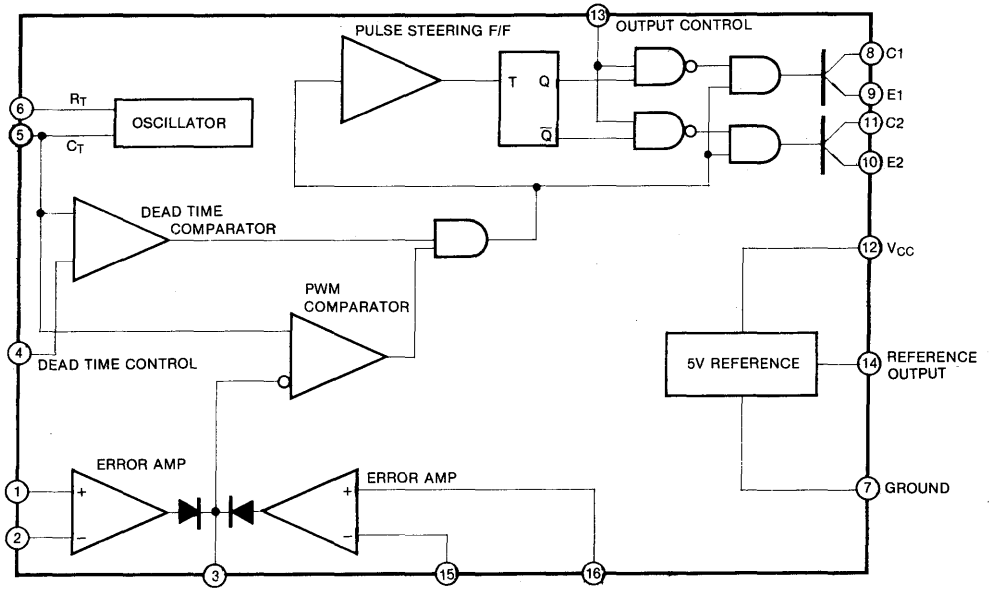


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	42	V
Collector Output Voltage	V_{CO}	42	V
Collector Output Current	I_{CO}	250	mA
Amplifier Input Voltage	V_{IN}	V_{CC} + 0.3	V
Power Dissipation	P_d	1	W
Operating Temperature Range	T_{opr}	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTIC

(V_{CC} = 20V, f = 10KHz, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
REFERENCE SECTION						
Reference Output Voltage	V_O	I_{ref} = 1mA	4.75	5.0	5.25	V
Line Regulation	$\triangle V_O$	V_{CC} = 7V to 40V		2.0	25	mV
Temperature Coefficient		Ta = 0°C to 70°C		0.01	0.03	%/°C
Load Regulation	$\triangle V_O$	I_{ref} = 1mA to 10mA		1.0	15	mV
Short-Circuit Output Current	I_{SC}	V_{ref} = 0	10	35	50	mA
OSCILLATOR SECTION						
Oscillation Frequency	F_{OSC}	C_T = 0.01μF, R_T = 12K		10		KHz
Frequency Change with Temperature	F_{OSC}/T	C_T = 0.01μF, R_T = 12K			2	%
DEAD TIME CONTROL SECTION						
Input Bias Current	I_B	V_{CC} = 15V, 0 < V_4 < 5.25V		−2.0	−10	μA
Maximum Duty Cycle	DC_{max}	V_{CC} = 15V, Pin 4 = 0V O.C Pin = V_{ref}	45			%
Input Threshold Voltage	V_{TH}	Zero Duty Cycle		3.0	3.3	V
		Max. Duty Cycle	0			
ERROR AMP SECTION						
Input Offset Voltage	V_{IO}	V_3 = 2.5V		2.0	10	mV
Input Offset Current	I_{IO}	V_3 = 2.5V		25	250	mA
Input Bias Current	I_B	V_3 = 2.5V		0.2	1.0	μA
Common Mode Input Voltage	V_{OR}	7V < V_{CC} < 40V	−0.3		V_{CC}	V
Open-Loop Voltage Gain	A_{VO}	0.5V < V_3 < 3.5V	70	95		dB
Unit-Gain Bandwidth	BW			650		KHz

ELECTRICAL CHARACTERISTIC (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
PWM COMPARATOR SECTION						
Input Threshold Voltage	V_{TH}	Zero Duty Cycle		4	4.5	V
Input Sink Current	I_{IS}	$V_3 = 0.7V$	−0.3	−0.7		mA
OUTPUT CONTROL SECTION						
Single-Ended Operation	V_{OCL}				0.4	V
Push-Pull Operation	V_{OCH}		2.4			
OUTPUT SECTION						
Output Saturation Voltage Commen Emitter	$V_{CE}(sat)$	$V_E = 0$, $I_C = 200mA$		1.1	1.3	V
Commen Collector	$V_{CC}(sat)$	$V_C = 15V$, $I_E = -200mA$		1.5	2.5	
Collector Off-State Current	$I_C(off)$	$V_{CC} = 40V$, $V_{CE} = 40V$		2	100	μA
Emitter Off-State Current	$I_E(off)$	$V_{CC} = V_C = 40V$, $V_E = 0$			−100	
TOTAL DEVICE						
Standby Supply Current	I_{CC}	Pin 6 = V_{ref}, $V_{CC} = 15V$		6	10	mA
OUTPUT SWITCHING CHARACTERISTIC						
Rise Time	T_R					
Commen Emitter				100	200	nS
Commen Collector				100	200	
Fall Time	T_F					
Commen Emitter				25	100	nS
Commen Collector				40	100	

4

TYPICAL APPLICATION

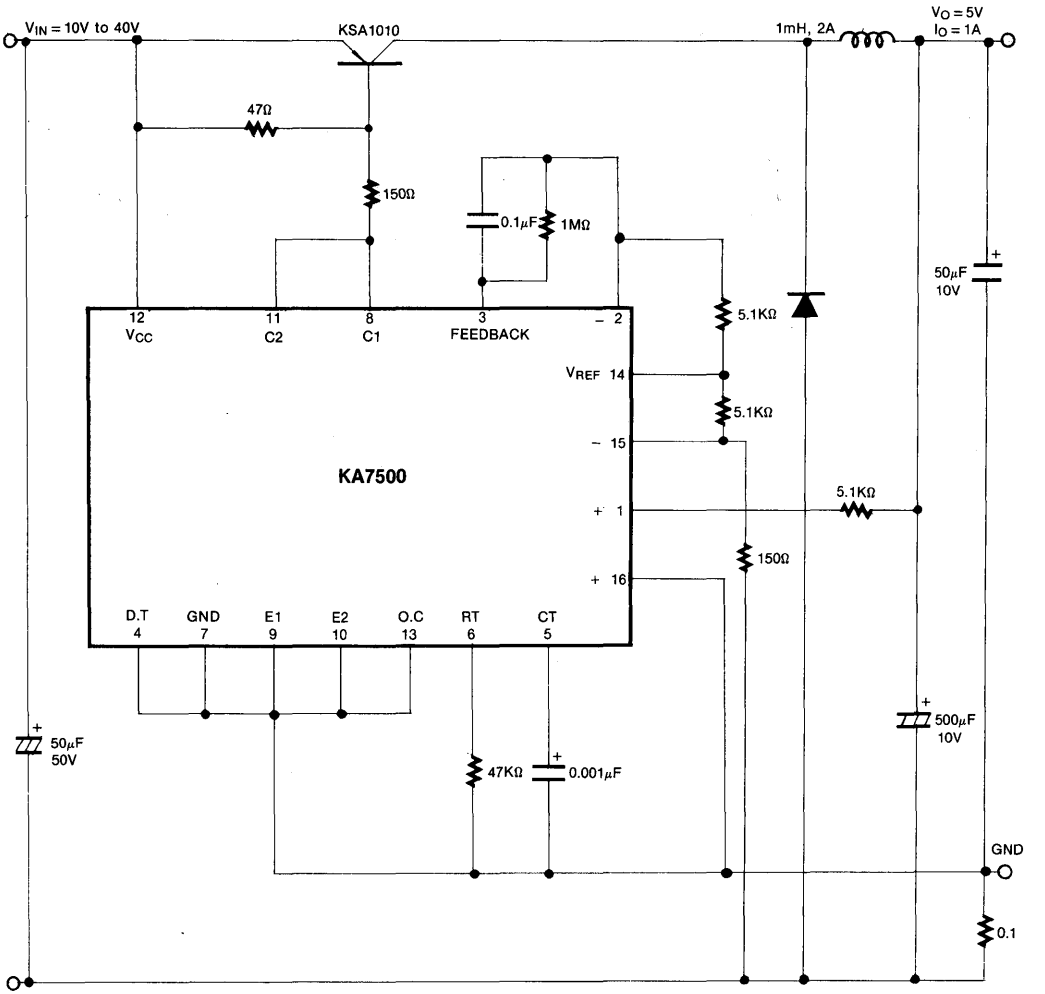
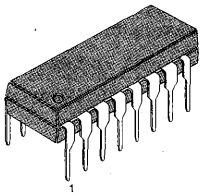


Fig. 1 PULSE WIDTH MODULATED STEP-DOWN CONVERTER

SWITCHING REGULATOR

The KA78S40 is a monolithic switching regulator subsystem consisting of all the active building blocks necessary for switching regulator systems.

16 DIP



FUNCTIONS

- High-current, high-voltage output switch a power transistor and a diode
- A temperature compensated voltage reference
- A comparator
- A duty cycle controllable oscillator with an active current limit circuit
- Independent operational amplifier.

FEATURES

- **Step-up, step-down or inverting switching regulators**
- **Output current to 1.5A without external transistors**
- **Output adjustable from 1.3 to 40V**
- **Operation from 2.5 to 40V input**
- **80dB line and load regulation**
- **Low standby current drain**
- **High gain, high current independent OP Amp.**

ORDERING INFORMATION

Device	Package	Operation Temperature
KA78S40N	16 DIP	0 ~ 70°C
**KA78S40IN	16 DIP	- 25 ~ 85°C

** Under development

BLOCK DIAGRAM

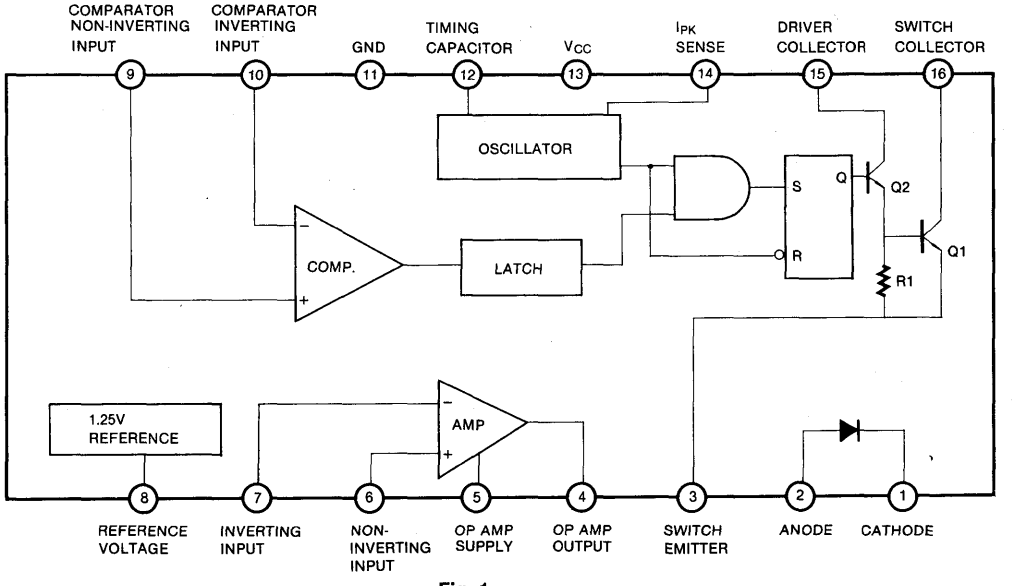


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
OP Amp Power Supply Voltage	V_{OP}	40	V
Common Mode Input Voltage Range	V_{ICM}	$-0.3 \sim V_{CC}$	V
Differential Input Voltage Range (Note)	V_{ID}	$-30 \sim 30$	V
Output Short Circuit Duration (OP Amp)	I_{SC}	Continuous	
Current from V_{REF}	I_{REF}	10	mA
Voltage from Switch Collector to GND	V_{CG}	40	V
Voltage from Switch Emitter to GND	V_{EG}	40	V
Voltage from Switch Collector to Emitter	V_{CE}	40	V
Voltage from Power Diode to GND	V_{DG}	40	V
Reverse Power Diode Voltage	V_{DR}	40	V
Current Through Power Switch	I_{SW}	1.5	A
Current Through Power Diode	I_D	1.5	A
Power Dissipation	P_D	1.5	W
Lead Temperature (Soldering, 10 Sec)	T_{lead}	260	°C
Operating Temperature Range	T_{opr}	0 +70	°C
Storage Temperature Range	T_{stg}	−65 +150	°C

NOTE: For supply voltage less than 30V, the absolute maximum voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, $V_{OP\ Amp}$ = 5.0V, 0° < Ta < 70°, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
General Characteristic						
Supply Voltage	V_{CC}		2.5		40	V
Supply Current Disconnected OP Amp	I_{CC1}	V_{CC} = 5.0V		2.2	3.5	mA
		V_{CC} = 40V		3.5	5.0	
Supply Current Connected OP Amp	I_{CC2}	V_{CC} = 5.0V			4.0	mA
		V_{CC} = 40V			5.5	
Reference Section						
Reference Voltage	V_{REF}	I_{REF} = 1.0mA	1.180	1.245	1.310	V
Reference Voltage Line Regulation	$\triangle V_{REF}$	V_{CC} = 3.0V to 40V I_{REF} = 1.0mA, Ta = 25°C		0.04	0.2	mV/V
Reference Voltage Load Regulation	$\triangle V_{REF}$	I_{REF} = 1.0mA to 10mA Ta = 25°C		0.2	0.5	mV/mA
Oscillation Section						
Charging Current	I_{CHG}	V_{CC} = 5.0V, Ta = 25°C	20		50	μA
		V_{CC} = 40V, Ta = 25°C	20		70	μA
Discharging Current	I_{DCH}	V_{CC} = 5.0V, Ta = 25°C	150		250	μA
		V_{CC} = 40V, Ta = 25°C	150		350	μA

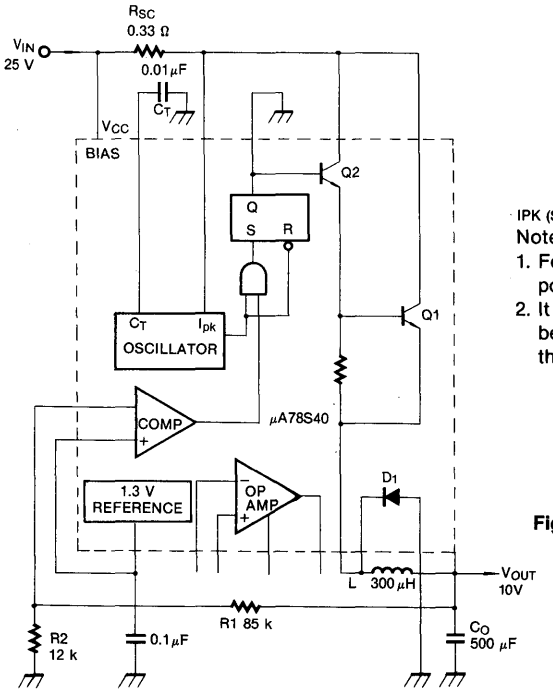
ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator Voltage Swing	V_{osc}	V_{CC} = 5.0V, Ta = 25°C		0.5		V
t_{on}/t_{off}	t_r			6.0		μS/μS
Current Limit Section						
Current Limit Sense Voltage	V_{SEN}	Ta = 25°C	250		350	mV
Output Switch Section						
Output Saturation Voltage	V_{SAT}	I_{SW} = 1.0A, step-down		1.1	1.3	V
		I_{SW} = 1.0A, step-up		0.45	0.7	V
Output Transistor h_{FE}	h_{FE}	I_C = 1.0A, V_{CE} = 5.0V, Ta = 25°C		70		
Output Leakage Current	I_{leak}	V_{OUT} = 40V, Ta = 25°C		10		nA
Power Diode						
Forward Voltage Drop	V_D	I_D = 1.0A		1.25	1.5	V
Diode Leakage Current	I_{leak}	V_D = 40V, Ta = 25°C		10		nA
Comparator						
Input Offset Voltage	V_{IO}	$V_{CM} = V_{REF}$		1.5	15	mV
Input Bias Current	I_B	$V_{CM} = V_{REF}$		35	200	nA
Input Offset Current	I_{IO}	$V_{CM} = V_{REF}$		5.0	75	nA
Common Mode Voltage Range	V_{CM}	Ta = 25°C	0		V_{CC}-2	V
Power Supply Rejection Ratio	PSRR	V_{CC} = 3.0V to 40V, Ta = 25°C	70	96		dB
Operational Amplifier						
Input Offset Voltage	V_{IO}	V_{CM} = 2.5V		4.0	15	mV
Input Bias Current	I_{IB}	V_{CM} = 2.5V		30	200	nA
Input Offset Current	I_{IO}	V_{CM} = 2.5V		5.0	75	nA
Voltage Gain (Positive)	A_{VOL+}	R_L = 2.0 kΩ to GND, V_o = 1.0 to 2.5V, Ta = 25°C	25	250		V/mV
Voltage Gain (Negative)	V_{VOL-}	R_L = 2.0 kΩ to V_+ OP Amp V_o = 1.0 to 2.5V, Ta = 25°C	25	250		V/mV
Common Mode Voltage Range	V_{CM}	Ta = 25°C	0		V_{CC}-2	V
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 3.0V, Ta = 25°C	76	100		dB
Power Supply Rejection Ratio	PSRR	V_{op} = 3.0 to 40V, Ta = 25°C	76	100		dB
Output Source Current	I_{SOUR}	Ta = 25°C	75	100		mA
Output Sink Current	I_{SINK}	Ta = 25°C	10	35		mA
Slew rate	S.R	Ta = 25°C		0.6		V/μS
Output Low Voltage	V_{OL}	I_L = −5.0mA, Ta = 25°C			1.0	V
Output High Voltage	V_{OH}	I_L = 50mA, Ta = 25°C	V_{op} − 3.0			V

APPLICATION INFORMATION

Design Formulas

Characteristic	Step Down	Step Up	Inverting	Unit
I_{pk}	$2\ I_{OUT(Max)}$	$2\ I_{OUT(Max)} \bullet \frac{V_{OUT}+V_D-V_{sat}}{V_{IN}-V_{sat}}$	$2I_{OUT(Max)} \bullet \frac{V_{IN}+\lvert V_{OUT}\rvert+V_D-V_{sat}}{V_{IN}-V_{sat}}$	A
R_{SC}	$0.33/I_{pk}$	$0.33/I_{pk}$	$0.33/I_{pk}$	Ω
$\frac{t_{on}}{t_{off}}$	$\frac{V_{OUT}+V_D}{V_{IN}-V_{sat}-V_{OUT}}$	$\frac{V_{OUT}+V_D-V_{IN}}{V_{IN}-V_{sat}}$	$\frac{\lvert V_{OUT}\rvert+V_D}{V_{IN}-V_{sat}}$	
L	$\frac{V_{OUT}+V_D}{I_{pk}} \bullet t_{off}$	$\frac{V_{OUT}+V_D-V_{IN}}{I_{pk}} \bullet t_{off}$	$\frac{\lvert V_{OUT}\rvert+V_D}{I_{pk}} \bullet t_{off}$	μH
t_{off}	$\frac{I_{pk} \bullet L}{V_{OUT}+V_D}$	$\frac{I_{pk} \bullet L}{V_{OUT}+V_D-V_{IN}}$	$\frac{I_{pk} \bullet L}{\lvert V_{OUT}\rvert+V_D}$	μs
C_T (μF)	$45 \times 10^{-5}\ t_{off}$ (μs)	$45 \times 10^{-5}\ t_{off}$ (μs)	$45 \times 10^{-5}\ t_{off}$ (μs)	μF
C_O	$\frac{I_{pk} \bullet (t_{on}+t_{off})}{8\ V_{ripple}}$	$\frac{(I_{pk}-I_{OUT})^2 \bullet t_{off}}{2\ I_{pk} \bullet V_{ripple}}$	$\frac{(I_{pk}-I_{OUT})^2 \bullet t_{off}}{2\ I_{pk} \bullet V_{ripple}}$	μF
Efficiency	$\frac{V_{IN}-V_{sat}+V_D}{V_{IN}} \bullet \frac{V_{OUT}}{V_{OUT}+V_D}$	$\frac{V_{IN}-V_{sat}}{V_{IN}} \bullet \frac{V_{OUT}}{V_{OUT}+V_D-V_{sat}}$	$\frac{V_{IN}-V_{sat}}{V_{IN}} \bullet \frac{\lvert V_{OUT}\rvert}{V_{OUT}+V_D}$	
I_{IN}(Avg) (Max load condition)	$\frac{I_{pk}}{2} \bullet \frac{V_{OUT}+V_D}{V_{IN}-V_{sat}+V_D}$	$\frac{I_{pk}}{2}$	$\frac{I_{pk}}{2} \bullet \frac{\lvert V_{OUT}\rvert+V_D}{V_{IN}+\lvert V_{OUT}\rvert+V_D-V_{sat}}$	A



IPK (SWITCH)

Notes

1. For $I_{OUT} \geq 200$mA use external diode to limit on chip power dissipation.
2. It is recommended that the internal reference (pin 8) be bypassed by a 0.1μF capacitor directly to (pin 11) the ground point of the KA78S40.

Fig. 2. Typical step-down operation (Ta = 25°C)

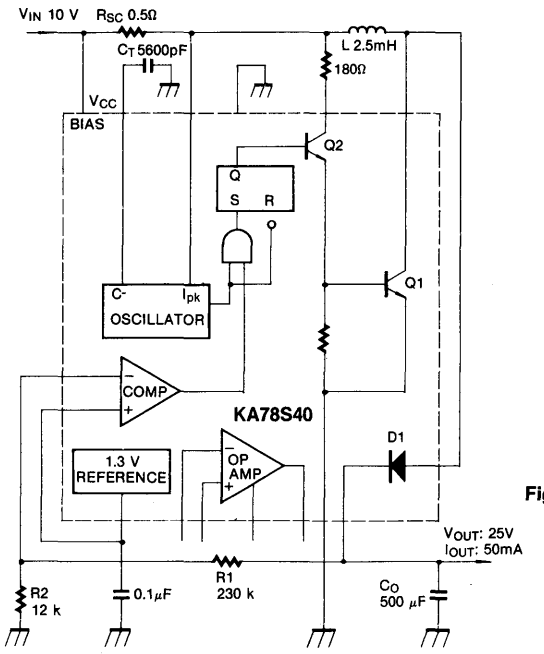


Fig. 3. Typical step-up operation (Ta = 25°C)

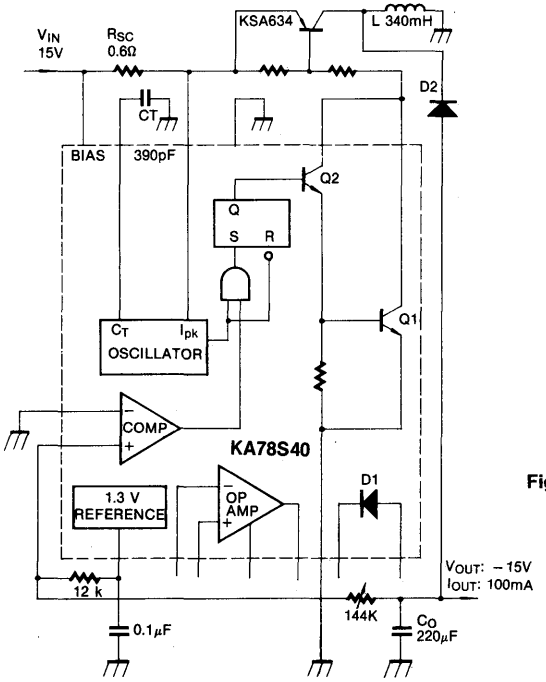


Fig. 4. Typical inverting operation (Ta = 25°C)

TYPICAL CHARACTERISTICS

Fig. 5. C_T V_S t_{off}

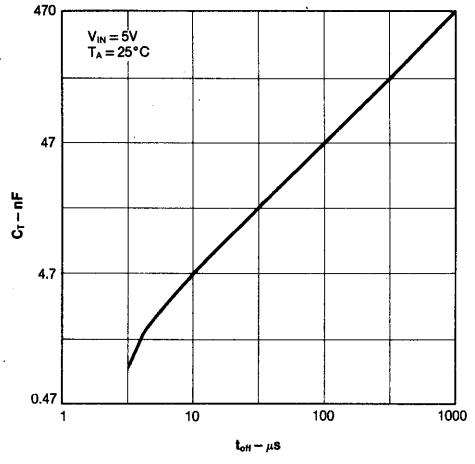


Fig. 6. V_{REF} V_S T_j

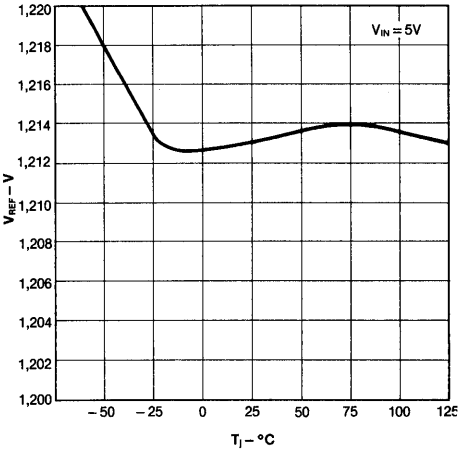


Fig. 7. $I_{discharge}$ V_S V_{IN}

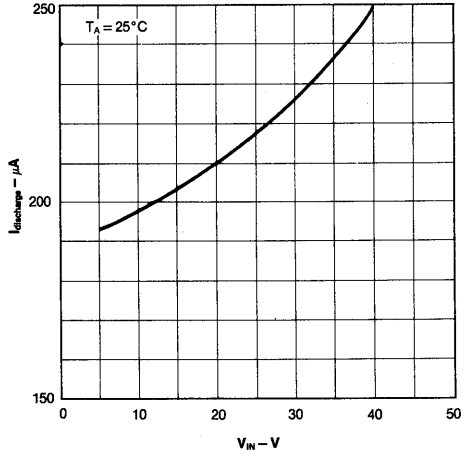
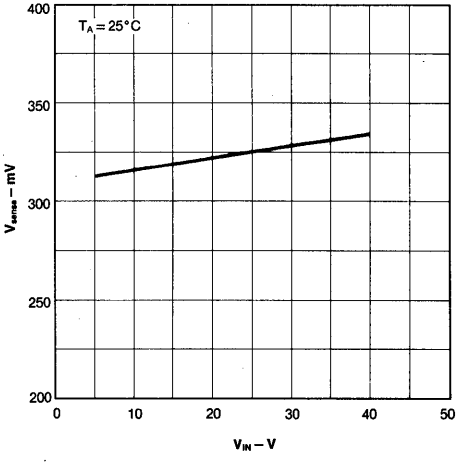
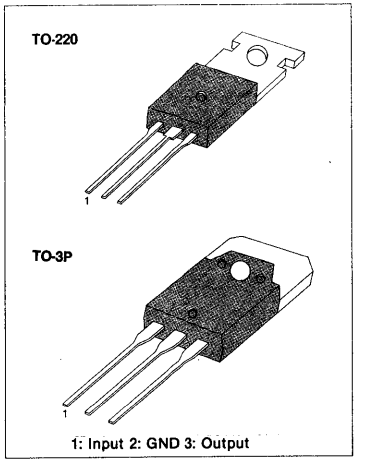


Fig. 8. V_{sense} V_S V_{IN}



3A POSITIVE VOLTAGE REGULATOR

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 3.0 amperes. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance on AC – suffix 5, 12 and 15 volts device types.
Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



1: Input 2: GND 3: Output

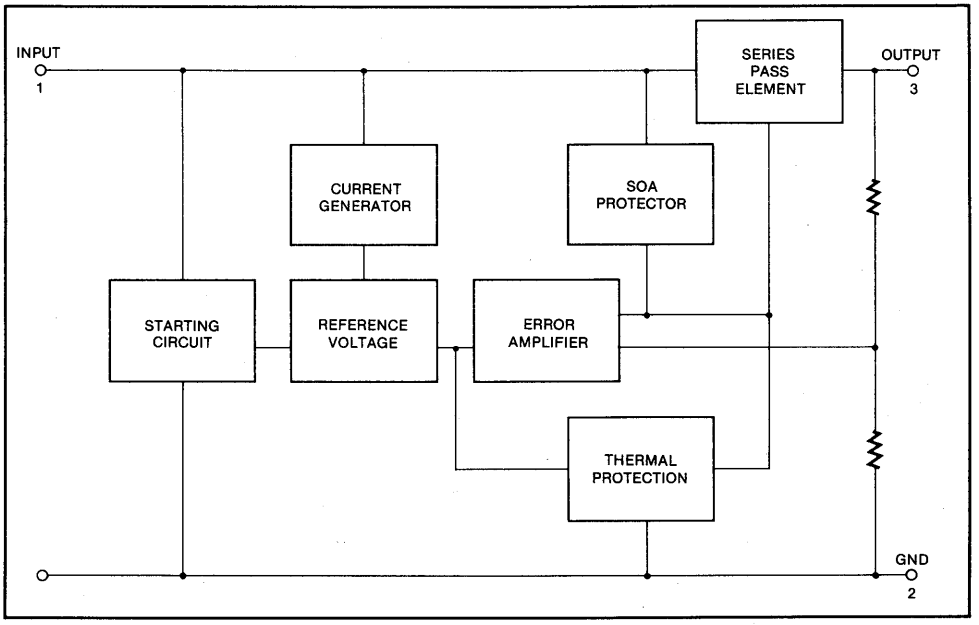
FEATURES

- **Output current in excess of 3.0 ampere**
- **Output transistor safe-area compensation**
- **Power dissipation: 25W (To-220)**
- **Internal short-circuit current limiting**
- **Internal thermal overload protection**
- **Output voltage offered in 2% and 4% tolerance (2% regulators are available in 5, 12 and 15 volt devices)**
- **No external components required**
- **Thermal regulation is specified**
- **Output voltage of 5; 6; 8; 12; 15; 18; 24V**
- **Mass production: KA78T05**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA78TXXCT	TO-220	0 ~ 125°C
KA78TXXACT		
KA78TXXCH	TO-3P	
KA78TXXACH		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (5.0V – 12V) (15V – 24V)	V_{IN}	35 40	V V
Power Dissipation	P_D	Internally limited	
Thermal Resistance, Junction to Air Tc = 25°C	Θ_{JA}	65	°C/W
Thermal Resistance, Junction to Case	Θ_{JC}	2.5	°C/W
Operating Temperature Range	T_{opr}	0 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

KA78T05C, KA78T05AC ELECTRICAL CHARACTERISTICS

(V_{IN} = 10V, I_o = 3.0A, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA78T05AC			KA78T05C			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	5mA ≤ I_o ≤ 3.0A, T_j = 25°C 5mA ≤ I_o ≤ 3A; 7.3V ≤ V_{IN} ≤ 20V, 5mA ≤ I_o ≤ 2A	4.9 4.8	5 5	5.1 5.2	4.8 4.75	5.0 5.0	5.2 5.25	V_{DC}
Line Regulation	$\triangle V_o$	7.2V ≤ V_{IN} ≤ 35V, I_o = 5mA, T_j = 25°C 7.2V ≤ V_{IN} ≤ 35V, I_o = 1.0A, T_j = 25°C 7.5V ≤ V_{IN} ≤ 20V, I_o = 2.0A 8.0V ≤ V_{IN} ≤ 12V, I_o = 3.0A		3.0	10		3.0	25	mV
Load Regulation	$\triangle V_o$	5mA ≤ I_o ≤ 3.0A, T_j = 25°C 5mA ≤ I_o ≤ 3.0A		10 15	25 50		10 15	30 80	mV mV
Thermal Regulation	REG_{therm}	Pulse = 10ms, P = 20W, Ta = 25°C		0.001	0.01		0.002	0.03	%V_o/W
Quiescent Current	I_d	5mA ≤ I_o ≤ 3A, T_j = 25°C 5mA ≤ I_o ≤ 3A		3.5 4.0	5.0 6.0		3.5 4.0	5.0 6.0	mA mA
Quiescent Current Change	$\triangle I_d$	7.2V ≤ V_{IN} ≤ 35V, I_o = 5mA, T_j = 25°C; 7.5V ≤ V_{IN} ≤ 20V, I_o = 2A; 5mA ≤ I_o ≤ 3A		0.1	0.5		0.1	0.8	mA
Ripple Rejection	RR	8V ≤ V_{IN} ≤ 18V, f = 120Hz, I_o = 2.0A	68	75		65	75		dB
Dropout Voltage	V_D	I_o = 3A, T_j = 25°C		2.2	2.5		2.2	2.5	V_{DC}
Output Noise Voltage	V_N	10Hz ≤ f ≤ 100KHz, T_j = 25°C		10			10		μV/V_o
Output Resistance	R_o	f = 1.0KHz		2.0			2.0		mΩ
Short Circuit Current Limit	I_{SC}	V_{IN} = 35V, T_j = 25°C		1.5	2.5		1.5	2.5	A
Peak Output Current	I_{peak}	T_j = 25°C		5.0			5.0		A
Average Temperature Coefficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		0.2			0.2		mV/°C

KA78T06C ELECTRICAL CHARACTERISTICS

(V_{IN} = 11V, I_o = 3.0V, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA78T06C			Unit
			Min	Typ	Max	
Output Voltage	V_o	5.0mA ≤ I_o ≤ 3A, T_j = +25°C 5.0mA ≤ I_o ≤ 3A; 8.3V ≤ V_{IN} ≤ 21V, 5mA ≤ I_o ≤ 2A	5.75 5.7	6.0 6.0	6.25 6.3	V
Line Regulation	$\triangle V_o$	8.25V ≤ V_{IN} ≤ 35V I_o = 5.0mA, T_j = +25°C; 8.25V ≤ V_{IN} ≤ 35V I_o = 1.0A, T_j = +25°C; 8.6V ≤ V_{IN} ≤ 21V I_o = 2.0A 9.0V ≤ V_{IN} ≤ 13V I_o = 3.0A		4.0	30	mV
Load Regulation	$\triangle V_o$	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		10 15	30 80	mV
Thermal Regulation	REG_{therm}	Pulse = 10ms, P = 20W, Ta = 25°C		0.002	0.03	% V_o/W
Quiescent Current	I_d	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		3.5 4.0	5.0 6.0	mA
Quiescent Current Change	$\triangle I_d$	8.25V ≤ V_{IN} ≤ 35V, I_o = 5mA, T_j = +25°C; 8.6V ≤ V_{IN} ≤ 21V, I_o = 2A; 5mA ≤ I_o ≤ 3.0A		0.1	0.8	mA
Ripple Rejection	RR	9V ≤ V_{IN} ≤ 19V, f = 120Hz, I_o = 2A	61	71		dB
Dropout Voltage	V_D	I_o = 3A, T_j = +25°C		2.2	2.5	V
Output Noise Voltage	V_N	10Hz ≤ f ≤ 100KHz, T_j = +25°C		10		$\mu V/V_o$
Output Resistance	R_o	f = 1.0KHz		2.0		mΩ
Short Circuit Current Limit	I_{SC}	V_{IN} = 35V, T_j = +25°C		1.5	2.5	A
Peak Output Current	I_{peak}	T_j = +25°C		5.0		A
Average Temperature Cofficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		0.3		mV/°C

KA78T08C ELECTRICAL CHARACTERISTICS

(V_{IN} = 14V, I_o = 3.0V, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA78T08C			Unit
			Min	Typ	Max	
Output Voltage	V_o	5.0mA ≤ I_o ≤ 3A, T_j = +25°C 5.0mA ≤ I_o ≤ 3A; 10.4V ≤ V_{IN} ≤ 23V, 5mA ≤ I_o ≤ 2A	7.7 7.6	8.0 8.0	8.3 8.4	V_{DC}
Line Regulation	$\triangle V_o$	10.3V ≤ V_{IN} ≤ 35V, I_o = 5mA, T_j = +25°C 10.3V ≤ V_{IN} ≤ 35V, I_o = 1.0A, T_j = +25°C 10.7V ≤ V_{IN} ≤ 23V, I_o = 2.0A 11V ≤ V_{IN} ≤ 17V, I_o = 3.0A		4.0	35	mV
Load Regulation	$\triangle V_o$	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		10 15	30 80	mV
Thermal Regulation	REG_{therm}	Pulse = 10ms, P = 20W, Ta = 25°C		0.002	0.03	$\%V_o/W$
Quiescent Current	I_d	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		3.5 4.0	5.0 6.0	mA
Quiescent Current Change	$\triangle I_d$	10.3V ≤ V_{IN} ≤ 35V, I_o = 5mA, T_j = +25°C 10.7V ≤ V_{IN} ≤ 23V, I_o = 2A 5mA ≤ I_o ≤ 3A		0.1	0.8	mA
Ripple Rejection	RR	11V ≤ V_{IN} ≤ 21V, f = 120Hz, I_o = 2A	61	71		dB
Dropout Voltage	V_D	I_o = 3A, T_j = +25°C		2.2	2.5	V_{DC}
Output Noise Voltage	V_N	10Hz ≤ f ≤ 100KHz, T_j = +25°C		10		$\mu V/V_o$
Output Resistance	R_o	f = 1.0KHz		2.0		mΩ
Short Circuit Current Limit	I_{SC}	V_{IN} = 35V, T_j = +25°C		1.5	2.5	A
Peak Output Current	I_{peak}	T_j = +25°C		5.0		A
Average Temperature Cofficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		0.3		mV/°C

KA78T12C, KA78T12AC ELECTRICAL CHARACTERISTICS

(V_{IN} = 19V, I_o = 3.0A, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise noted)

Characteristic	Symbol	Test Conditions	KA78T12AC			KA78T12C			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	5mA≤I_o≤3A, T_j = 25°C 5mA≤I_o≤3A; 5mA≤I_o≤2A, 14.5V≤V_{IN}≤27V	11.75 11.5	12 12	12.25 12.5	11.5 11.4	12 12	12.5 12.6	V_{DC}
Line Regulation	$\triangle V_o$	14.5V_{DC}≤V_{IN}≤35V_{DC}, I_o = 5mA, T_j = +25°C; 14.5V_{DC}≤V_{IN}≤35V_{DC}, I_o = 1.0A, T_j = +25°C; 14.9V_{DC}≤V_{IN}≤27V_{DC}, I_o = 2.0A; 16V_{DC}≤V_{IN}≤22V_{DC}, I_o = 3.0A		6.0	18		6.0	45	mV
Load Regulation	$\triangle V_o$	5mA≤I_o≤3A, T_j = +25°C 5mA≤I_o≤3A		10 15	25 50		10 15	30 80	mV
Thermal Regulation	REG_{therm}	Pulse = 10ms, P = 20W, Ta = 25°C		0.001	0.01		0.002	0.03	%V_o/W
Quiescent Current	I_d	5mA≤I_o≤3A, T_j = +25°C 5mA≤I_o≤3A		3.5 4.0	5.0 6.0		3.5 4.0	5.0 6.0	mA
Quiescent Current Change	$\triangle I_d$	14.5V_{DC}≤V_{IN}≤35V_{DC}, I_o = 5mA, T_j = 25°C; 14.9V_{DC}≤V_{IN}≤27V_{DC}, I_o = 2A; 5.0mA≤I_o≤3.0A		0.1	0.5		0.1	0.8	mA
Ripple Rejection	RR	15V_{DC}≤V_{IN}≤25V_{DC}, f = 120Hz, I_o = 2.0A	61	67		57	67		dB
Dropout Voltage	V_D	I_o = 3A, T_j = +25°C		2.2	2.5		2.2	2.5	V_{DC}
Output Noise Voltage	V_N	10Hz≤f≤100KHz, T_j = +25°C		10			10		$\mu V/V_o$
Output Resistance	R_o	f = 1.0KHz		2.0			2.0		mΩ
Short Circuit Current Limit	I_{SC}	V_{IN} = 35V, T_j = +25°C		1.5	2.5		1.5	2.5	A
Peak Output Current	I_{peak}	T_j = +25°C		5.0			5.0		A
Average Temperature Coefficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		0.5			0.5		mV/°C

KA78T15C, KA78T15AC ELECTRICAL CHARACTERISTICS

(V_{IN} = 23V, I_o = 3.0A, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise noted)

Characteristic	Symbol	Test Conditions	KA78T15AC			KA78T15C			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A; 17.5V_{DC} ≤ V_{IN} ≤ 30V_{DC}, 5mA ≤ I_o ≤ 2A	14.7 14.4	15 15	15.3 15.6	14.4 14.25	15 15	15.6 15.75	V_{DC}
Line Regulation	$\triangle V_o$	17.6V ≤ V_{IN} ≤ 40V, I_o = 5mA, T_j = +25°C 17.6V ≤ V_{IN} ≤ 40V, I_o = 1A, T_j = +25°C; 18V ≤ V_{IN} ≤ 30V, I_o = 2.0A; 20V ≤ V_{IN} ≤ 26V, I_o = 3.0A		7.5	22		7.5	55	mV
Load Regulation	$\triangle V_o$	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		10 15	25 50		10 15	30 80	mV
Thermal Regulation	REG_{therm}	Pulse = 10ms, P = 20W, Ta = 25°C		0.001	0.01		0.002	0.03	%V_o/W
Quiescent Current	I_d	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		3.5 4.0	5.0 6.0		3.5 4.0	5.0 6.0	mA
Quiescent Current Change	$\triangle I_d$	17.6V ≤ V_{IN} ≤ 40V, I_o = 5mA, T_j = +25°C; 18V ≤ V_{IN} ≤ 30V, I_o = 2A; 5mA ≤ I_o ≤ 3A		0.1	0.5		0.1	0.8	mA
Ripple Rejection	RR	18.5V_{DC} ≤ V_{IN} ≤ 28.5V_{DC}, f = 120Hz, I_o = 2.0A	60	65		55	65		dB
Dropout Voltage	V_D	I_o = 3A, T_j = +25°C		2.2	2.5		2.2	2.5	V_{DC}
Output Noise Voltage	V_N	10Hz ≤ f ≤ 100KHz, T_j = +25°C		10			10		$\mu V/V_o$
Output Resistance	R_o	f = 1.0KHz		2.0			2.0		mΩ
Short Circuit Current Limit	I_{SC}	V_{IN} = 40V, T_j = +25°C		1.0	2.0		1.0	2.0	A
Peak Output Current	I_{peak}	T_j = +25°C		5.0			5.0		A
Average Temperature Coefficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		0.6			0.6		mV/°C

KA78T18C ELECTRICAL CHARACTERISTICS

(V_{IN} = 27V, I_o = 3.0V, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA78T18C			Unit
			Min	Typ	Max	
Output Voltage	V_o	5.0mA ≤ I_o ≤ 3A, T_j = +25°C 5.0mA ≤ I_o ≤ 3A; 20.6V ≤ V_{IN} ≤ 33V, 5mA ≤ I_o ≤ 2A	17.3 17.1	18 18	18.7 18.9	V_{DC}
Line Regulation	$\triangle V_o$	20.7V ≤ V_{IN} ≤ 40V, I_o = 5mA, T_j = +25°C; 20.7V ≤ V_{IN} ≤ 40V, I_o = 1A, T_j = +25°C; 21.2V ≤ V_{IN} ≤ 33V, I_o = 2.0A 24V ≤ V_{IN} ≤ 30V, I_o = 3A		9.0	80	mV
Load Regulation	$\triangle V_o$	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		10 15	30 80	mV
Thermal Regulation	REG_{therm}	Pulse = 10ms, P = 20W, Ta = 25°C		0.002	0.03	%V_o/W
Quiescent Current	I_d	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		3.5 4.0	5.0 6.0	mA
Quiescent Current Change	$\triangle I_d$	20.7V ≤ V_{IN} ≤ 40V, I_o = 5mA, T_j = +25°C; 21.2V ≤ V_{IN} ≤ 33V, I_o = 2.0A; 5mA ≤ I_o ≤ 3.0A		0.1	0.8	mA
Ripple Rejection	RR	22V ≤ V_{IN} ≤ 32V, f = 120Hz, I_o = 2.0A	54	64		dB
Dropout Voltage	V_D	I_o = 3A, T_j = +25°C		2.2	2.5	V_{DC}
Output Noise Voltage	V_N	10Hz ≤ f ≤ 100KHz, T_j = +25°C		10		$\mu V/V_o$
Output Resistance	R_O	f = 1.0KHz		2.0		mΩ
Output Circuit Current Limit	I_{SC}	V_{IN} = 40V, T_j = +25°C		1.0	2.0	A
Peak Output Current	I_{peak}	T_j = +25°C		5.0		A
Average Temperature Coefficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		0.7		mV/°C

KA78T24C ELECTRICAL CHARACTERISTICS

(V_{IN} = 33V, I_o = 3.0A, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA78T24C			Unit
			Min	Typ	Max	
Output Voltage	V_o	5.0mA ≤ I_o ≤ 3A, T_j = +25°C 5.0mA ≤ I_o ≤ 3A; 27.3V ≤ V_{IN} ≤ 39V, 5mA ≤ I_o ≤ 2A	23 22.8	24 24	25 25.2	V_{DC}
Line Regulation	$\triangle V_o$	27V ≤ V_{IN} ≤ 40V, I_o = 5mA, T_j = +25°C; 27V ≤ V_{IN} ≤ 40V, I_o = 1.0A, T_j = +25°C; 27.5V ≤ V_{IN} ≤ 39V, I_o = 2.0A; 30V ≤ V_{IN} ≤ 36V, I_o = 3.0A		12	90	mV
Load Regulation	$\triangle V_o$	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		10 15	30 80	mV
Thermal Regulation	REG_{therm}	Pulse = 10mS, P = 20W, Ta = 25°C		0.002	0.03	%V_o/W
Quiescent Current	I_d	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		3.5 4.0	5.0 6.0	mA
Quiescent Current Change	$\triangle I_d$	27V ≤ V_{IN} ≤ 40V, I_o = 5mA, T_j = +25°C; 27.5V ≤ V_{IN} ≤ 39V, I_o = 2A; 5mA ≤ I_o ≤ 3A		0.1	0.8	mA
Ripple Rejection	RR	28V ≤ V_{IN} ≤ 38V, f = 120Hz, I_o = 2.0A	51	61		dB
Dropout Voltage	V_D	I_o = 3A, T_j = +25°C		2.2	2.5	V_{DC}
Output Noise Voltage	V_N	10Hz ≤ f ≤ 100KHz, T_j = +25°C		10		$\mu V/V_o$
Output Resistance	R_O	f = 1.0KHz		2.0		mΩ
Short Circuit Current Limit	I_{SC}	V_{IN} = 40V, T_j = +25°C		1.0	2.0	A
Peak Output Current	I_{peak}	T_j = +25°C		5.0		A
Average Temperature Coefficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		1.0		mV/°C

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 TEMPERATURE STABILITY

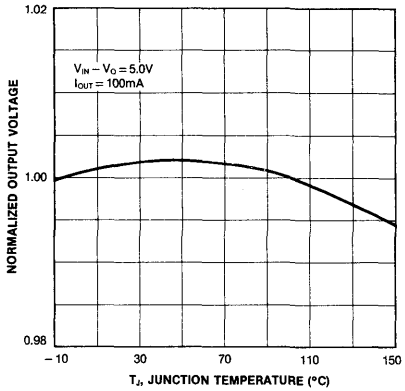


Fig. 2 OUTPUT IMPEDANCE

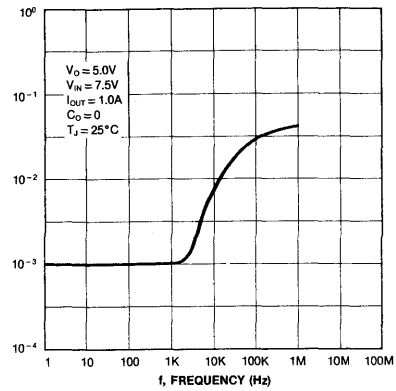


Fig. 3 RIPPLE REJECTION V_S FREQUENCY

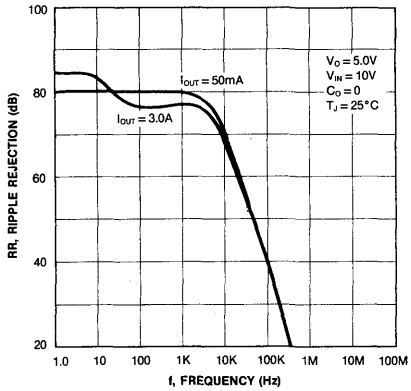


Fig. 4 RIPPLE REJECTION V_S OUTPUT CURRENT

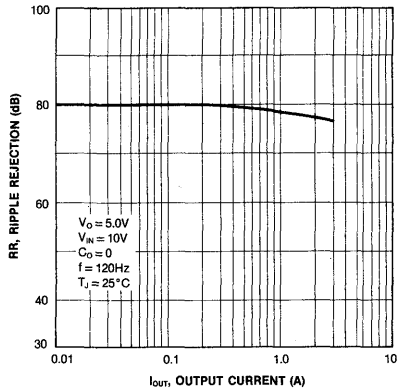


Fig. 5 QUIESCENT CURRENT V_S INPUT VOLTAGE

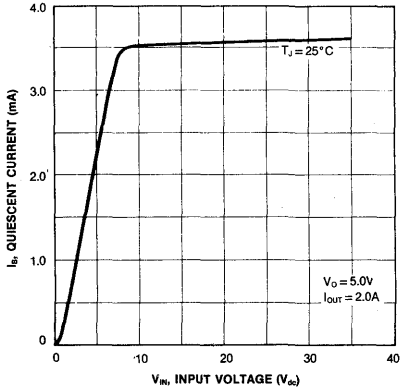


Fig. 6 QUIESCENT CURRENT V_S OUTPUT CURRENT

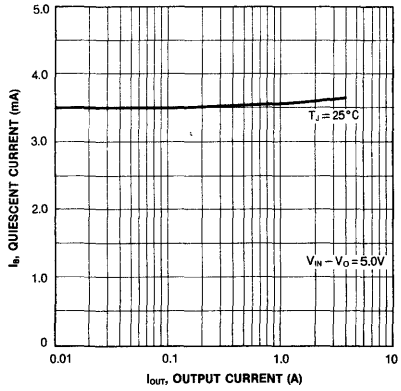


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Fig. 7 DROPOUT VOLTAGE

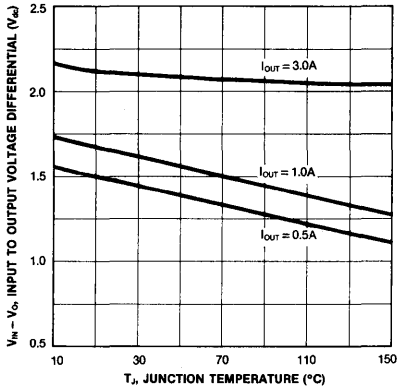


Fig. 8 PEAK OUTPUT CURRENT

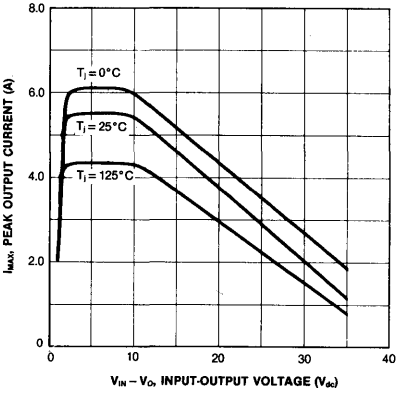


Fig. 9 LINE TRANSIENT RESPONSE

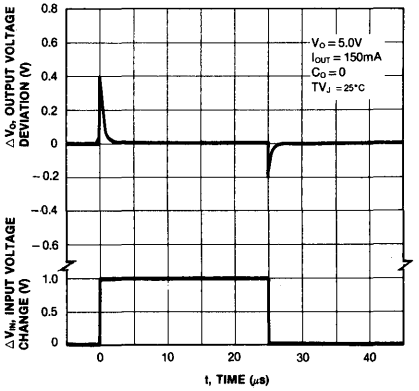


Fig. 10 LOAD TRANSIENT RESPONSE

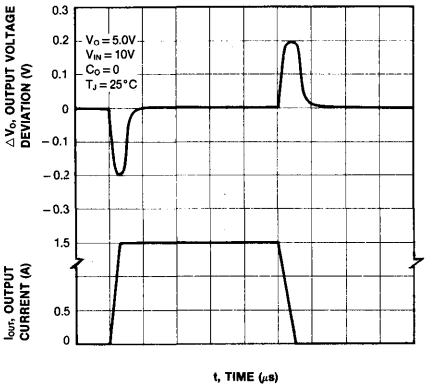
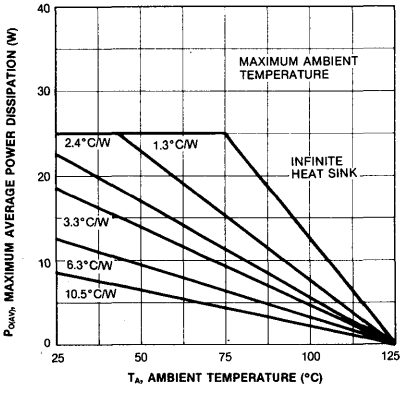


Fig. 11 MAXIMUM AVERAGE POWER DISSIPATION

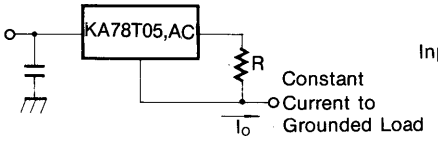


APPLICATION INFORMATIONS

The KA78T00,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provided good high-frequency characteristics to insure stable operation under all load conditions. A 0.33μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Fig. 12—CURRENT REGULATOR



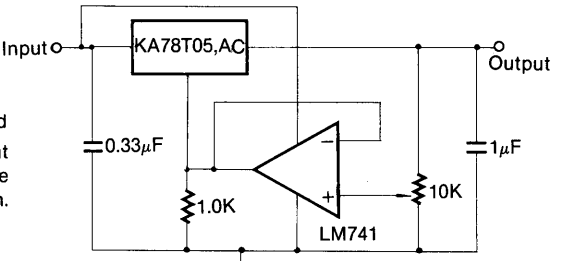
The KA78T05 regulator can also be used as a current source when connected as above. In order to minimize dissipation, the KA78T05 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0V}{R} + I_B$$

$\triangle I_B = 0.7mA$ over line, load and temperature changes
$I_B = 3.5mA$

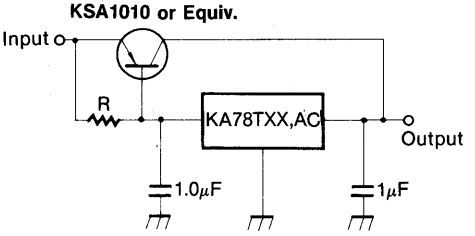
For example, a 2-ampere current source would require R to be a 2.5 ohm, 15W resistor and the output voltage compliance would be the input voltage less 7.5 volts.

Fig. 13—ADJUSTABLE OUTPUT REGULATOR



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.

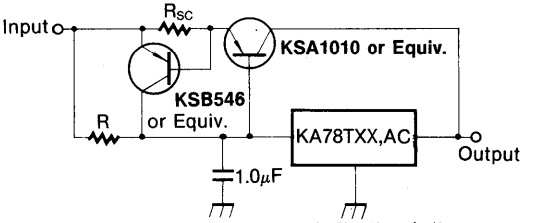
Fig. 14—CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The KA78T00,A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

Fig. 15—CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



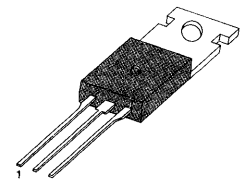
XX = 2 digits of type number indicating voltage.

The circuit of Figure 18 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

3-TERMINAL POSITIVE ADJUSTABLE REGULATOR

The LM317 is a 3-terminal adjustable positive voltage regulator capable of supplying in excess of 1.5A over an output voltage range of 1.2V to 37V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current-limiting, thermal-shutdown and safe area compensation, making it essentially blow-out proof. The LM317 serves a wide variety of applications including local, on-card regulation. This device also makes an especially simple adjustable switching regulator, and a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

TO-220



1: Adj 2: Output 3: Input

FEATURE

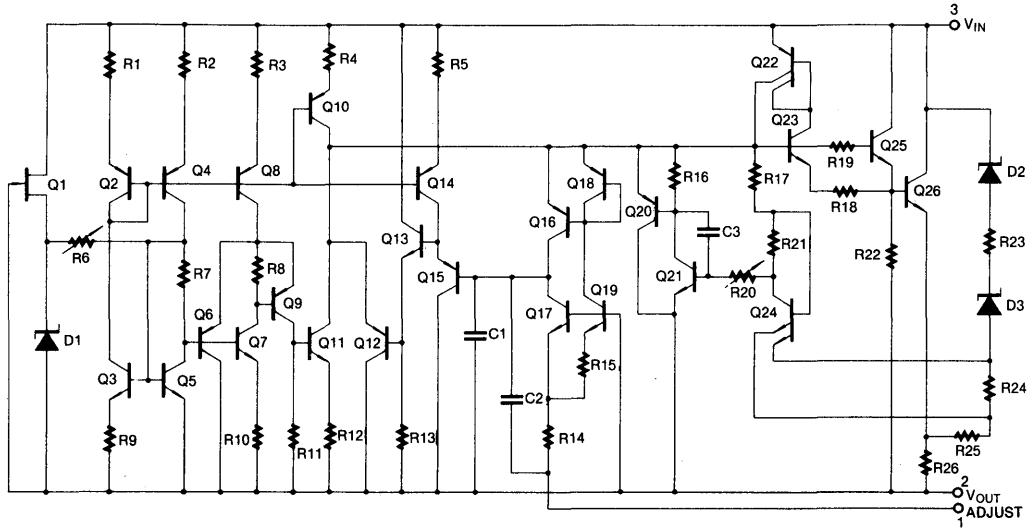
- **Output current in excess of 1.5A**
- **Output adjustable between 1.2V and 37V**
- **Internal thermal-overload protection**
- **Internal short-circuit current-limiting constant with temperature**
- **Output transistor safe-area compensation**
- **Floating operation for high-voltage applications**
- **Standard 3-pin transistor packages**

ORDERING INFORMATION

Device	Package	Operation Temperature
LM317T	TO-220	0 ~ 125°C
**LM217T	TO-220	− 25 ~ + 150°C

** Under development

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input-Output Voltage Differential	$V_{IN} - V_{OUT}$	40	V_{DC}
Lead Temperature	T_{lead}	230	°C
Power Dissipation	P_D	Internally limited	—
Operating Temperature Range	T_{opr}	0 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

($V_{IN} - V_{OUT} = 5V$, $I_{OUT} = 0.5A$, $0°C \leq T_j \leq 125°C$, $I_{max} = 1.5A$, $P_{max} = 20W$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	$\triangle V_o$	Ta = 25°C, $3V \leq V_{IN} - V_{OUT} \leq 40V$		0.01	0.04	%/V
		Ta = 25°C, $3V \leq V_{IN} - V_{OUT} \leq 40V$		0.02	0.07	%/V
Load Regulation	$\triangle V_o$	Ta = 25°C, $10mA \leq I_{OUT} \leq I_{MAX}$ $V_{OUT} \leq 5V$ $V_{OUT} \geq 5V$		5 0.1	25 0.5	mV $\%V_o$
		$10mA \leq I_{OUT} \leq I_{MAX}$ $V_{OUT} \leq 5V$ $V_{OUT} \geq 5V$		20 0.3	70 1.5	mV $\%V_o$
Adjustable Pin Current	I_{adj}			50	100	μA
Adjustable Pin Current Change	$\triangle I_{adj}$	$2.5V \leq V_{IN} - V_{OUT} \leq 40V$ $10mA \leq I_{OUT} \leq I_{MAX}$ $P \leq P_{MAX}$		0.2	5	μA
Reference Voltage	V_{REF}	$3V \leq V_{IN} - V_{OUT} \leq 40V$ $10mA \leq I_{OUT} \leq I_{MAX}$ $P_D \leq P_{MAX}$	1.20	1.25	1.30	V
Temperature Stability	T_S			0.7		$\%V_o$
Minimum Load Current to Maintain Regulation	I_{MIN}	$V_{IN} - V_{OUT} = 40V$		3.5	10	mA
Maximum Output Current	I_{MAX}	$V_{IN} - V_{OUT} \leq 15V$, $P_D \leq P_{MAX}$ $V_{IN} - V_{OUT} = 40V$, $P_D \leq P_{MAX}$	1.5 0.15	2.2 0.4		A
RMS Noise, % of V_{OUT}	e_N	Ta = 25°C, $10Hz \leq f \leq 10KHz$		0.003		$\%V_o$
Ripple Rejection	RR	$V_{OUT} = 10V$, f = 120Hz without C_{ADJ} $C_{ADJ} = 10\mu F$	 66	 65 80		dB
Long-Term Stability, $T_j = T_{high}$	S	Ta = 25°C for end point measurements, 1000HR		0.3	1	%
Thermal Resistance Junction to Case	$R_{\theta JC}$			5		°C/W

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 LOAD REGULATION

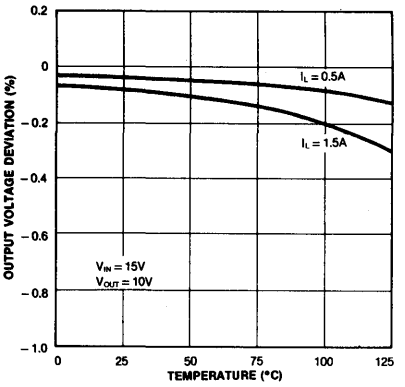


Fig. 2 ADJUSTMENT CURRENT

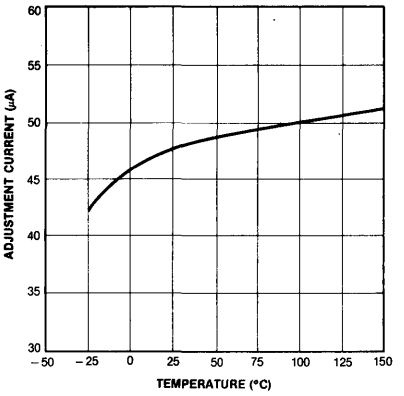


Fig. 3 DROPOUT VOLTAGE

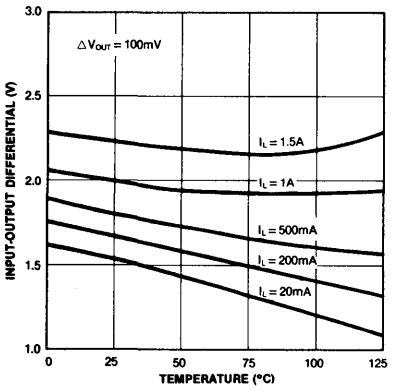


Fig. 4 TEMPERATURE STABILITY

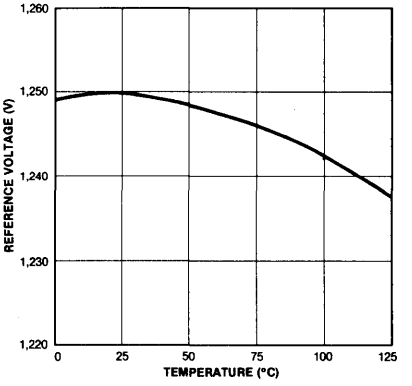


Fig. 5 RIPPLE REJECTION

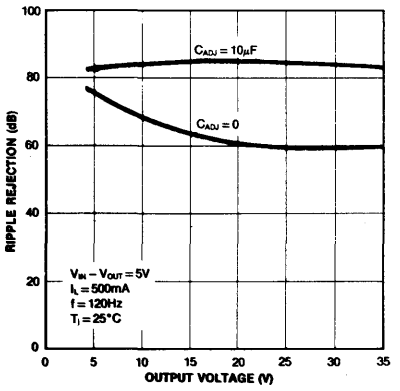


Fig. 6 RIPPLE REJECTION

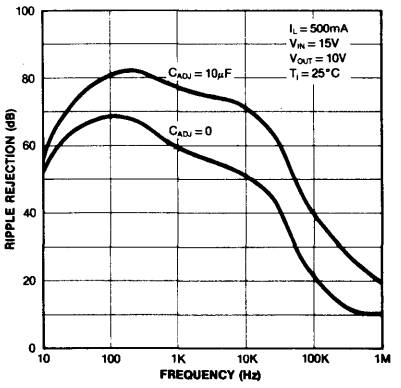


Fig. 7 RIPPLE REJECTION

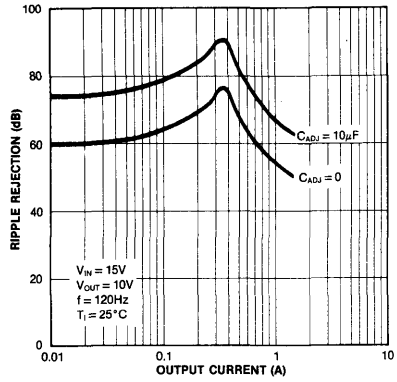


Fig. 8 OUTPUT IMPEDANCE

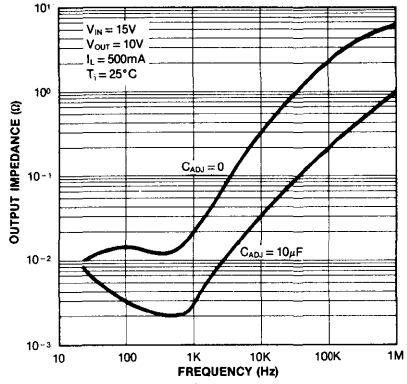


Fig. 9 LINE TRANSIENT RESPONSE

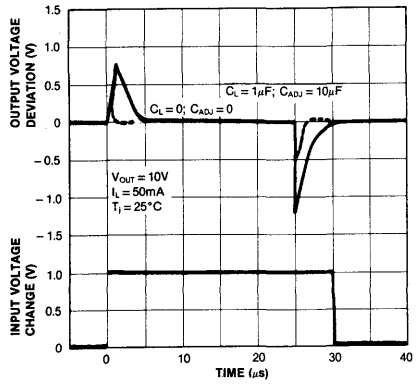


Fig. 10 LOAD TRANSIENT RESPONSE

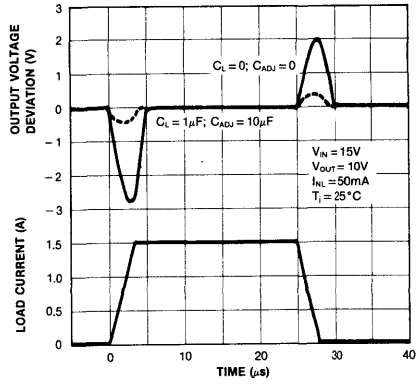
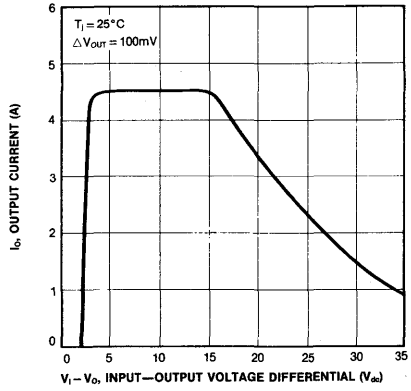


Fig. 11 MAXIMUM OUTPUT CURRENT



4

TYPICAL APPLICATIONS

Fig. 12 AC Voltage Regulator

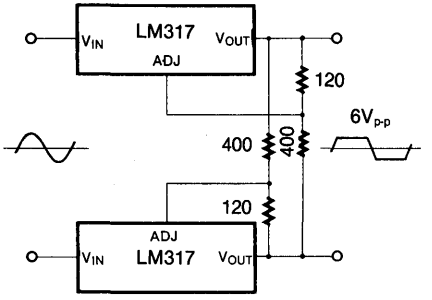
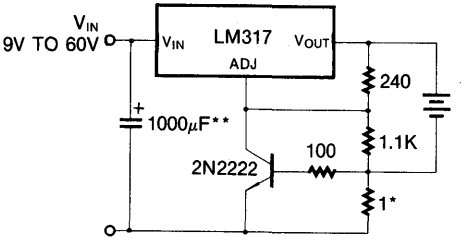
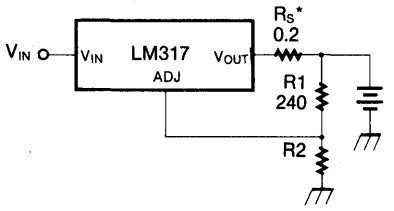


Fig. 13 Current Limited 6V Charger



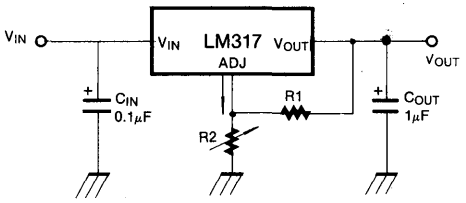
* Sets peak current (0.6A for 1Ω)
** The 1000μF is recommended to filter out input transients

Fig. 14 12V Battery Charger



* R_S—sets output impedance of charger
$Z_{OUT} = R_S (1 + \frac{R2}{R1})$ Use of R_S allows low charging rates with fully charged battery.

Fig. 15 Programmable Regulator



$V_{OUT} = 1.25V\ (1 + \frac{R_2}{R_1}) + I_{adj}\ R_2$

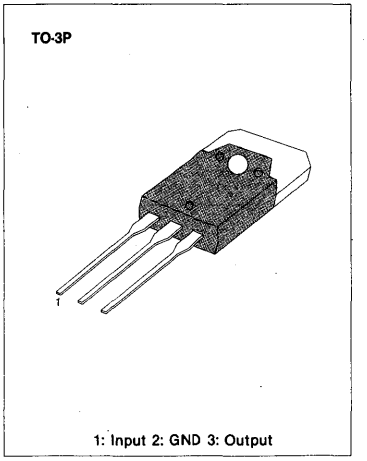
C_{IN} is required when regulator is located an appreciable distance from power supply filter.
C_{OUT} is not need for stability, however it does improve transient response
Since I_{adj} is controlled to less than 100μA, the error associated with this term is negligible in most applications.

3-TERMINAL POSITIVE VOLTAGE REGULATOR

The LM323 is a three-terminal positive regulator with a preset 5V output and a load driving capability of 3 Amps.

New circuit design and processing techniques are used to provide the high output current without sacrificing the regulation characteristics of lower current devices.

The LM323 can be used with a external transistor to supply up to 15A at 5 Volts.



FEATURES

- **3 Amp output current**
- **Internal current and thermal limiting**
- **0.01Ω typical output impedance**
- **7.5V *minimum* input voltage**
- **Output transistor safe area compensation**

ORDERING INFORMATION

Device	Package	Operation Temperature
LM323H	TO-3P	0 ~125°C
LM323T	TO-220	0 ~125°C

SCHEMATIC DIAGRAM

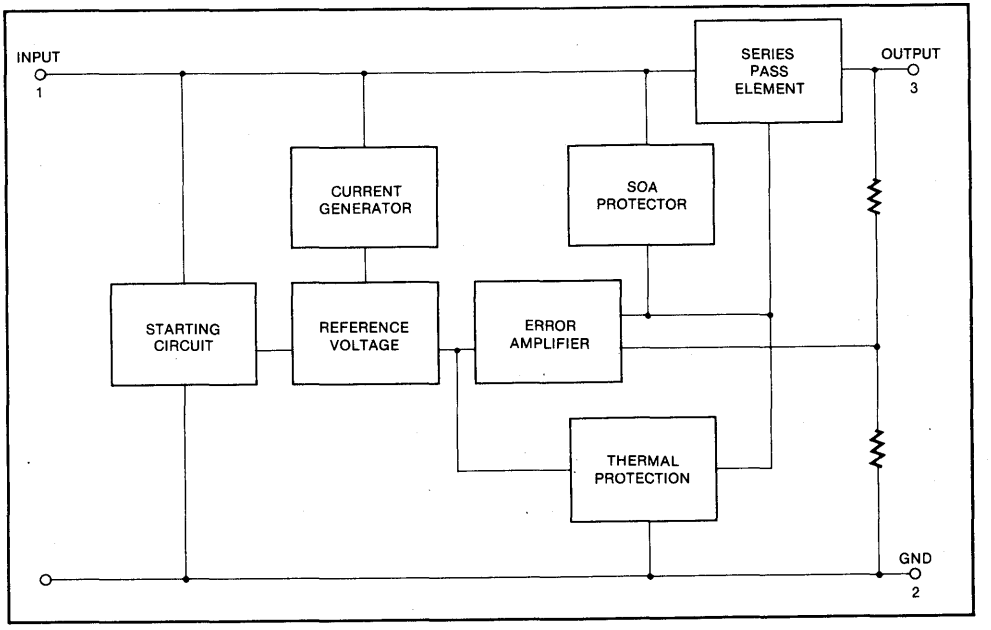


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage	V_{IN}	20	V
Operating Temperature Range	T_{opr}	0 ~ + 125	°C
Storage Temperature Range	T_{stg}	− 65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(0°C ≤ T_J ≤ 125°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	T_J = 25°C V_{IN} = 7.5V, I_{OUT} = 0	4.8	5	5.2V	
		7.5V ≤ V_{IN} ≤ 15V 0 ≤ I_{OUT} ≤ 3A, P ≤ 30W	4.75		5.25	V
Line Regulation	ΔV_O	T_J = 25°C 7.5V ≤ V_{IN} ≤ 15V		5	25	mV
Load Regulation	ΔV_O	T_J = 25°C, V_{IN} = 7.5V 0 ≤ I_{OUT} ≤ 3A		25	100	mV
Quiescent Current	I_d	7.5V ≤ V_{IN} ≤ 15V 0 ≤ I_{OUT} ≤ 3A		3	20	mA
Output Noise Voltage	V_N	T_J = 25°C, 10Hz ≤ f ≤ 100KHz		40		μV_{rms}
Short Circuit Current	I_{SC}	T_J = 25°C, V_{IN} = 15V		4.5		A
		T_J = 25°C, V_{IN} = 7.5V		5.5		A
Thermal Resistance Junction to Case	Θ_{JC}			3		°C/W

Fig. 2 MAXIMUM AVERAGE POWER DISSIPATION

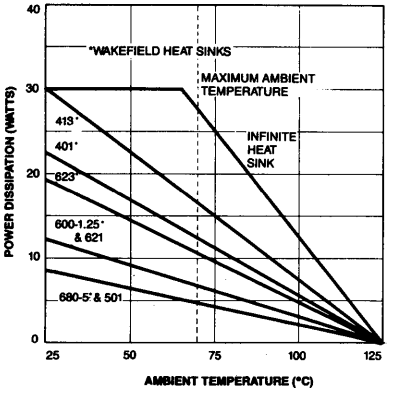


Fig. 3 OUTPUT IMPEDANCE

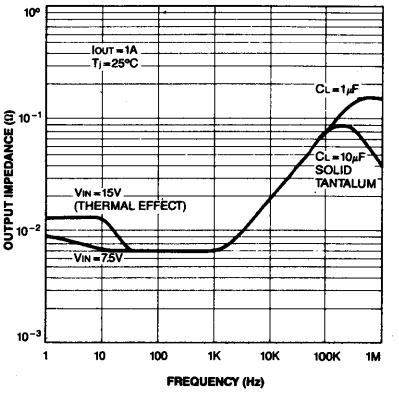


Fig. 4 SHORT CIRCUIT CURRENT

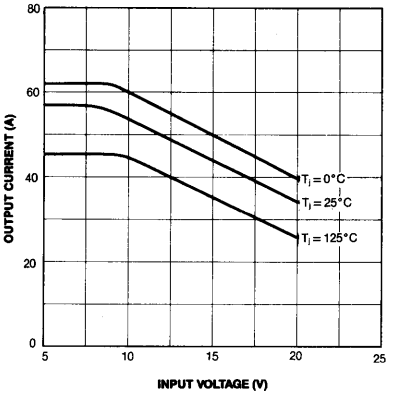


Fig. 5 RIPPLE REJECTION

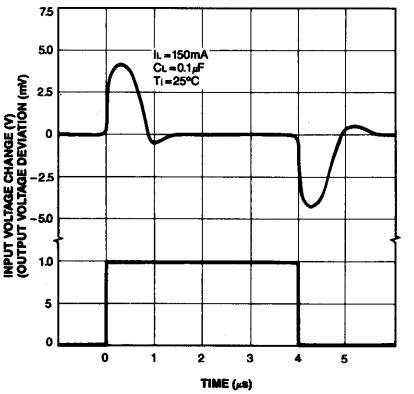


Fig. 6 DROPOUT VOLTAGE

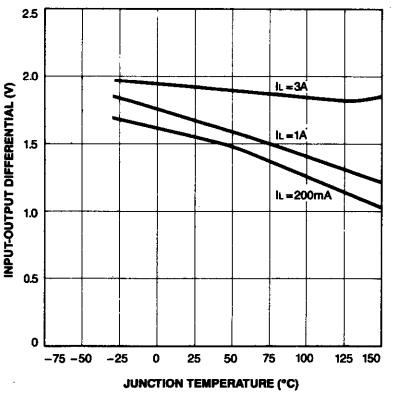


Fig. 7 LINE TRANSIENT RESPONSE

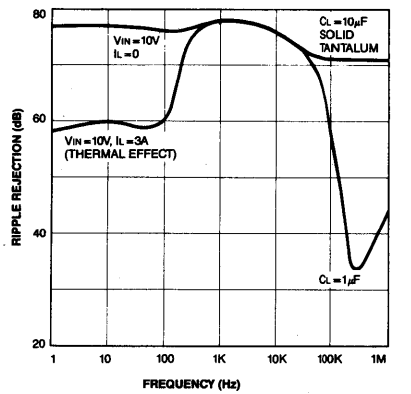


Fig. 8 OUTPUT VOLTAGE

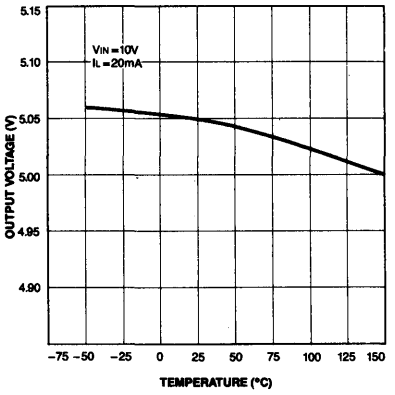


Fig. 9 QUIESCENT CURRENT

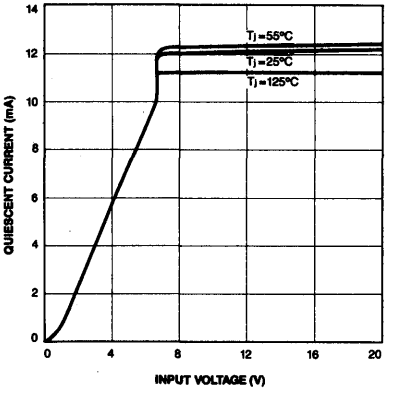


Fig. 10 LOAD TRANSIENT RESPONSE

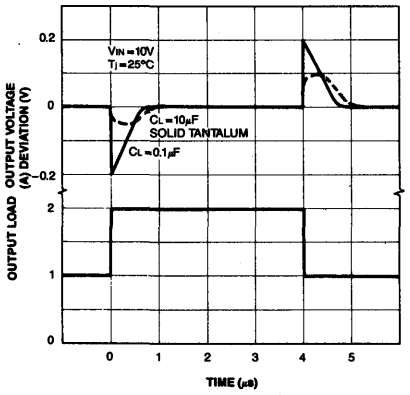
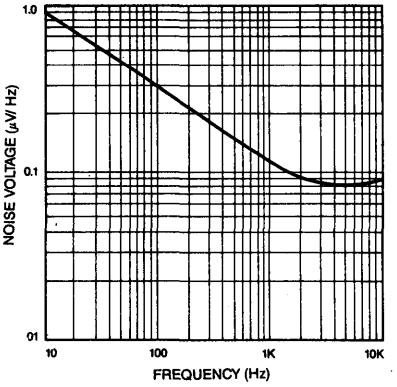


Fig. 11 OUTPUT NOISE VOLTAGE

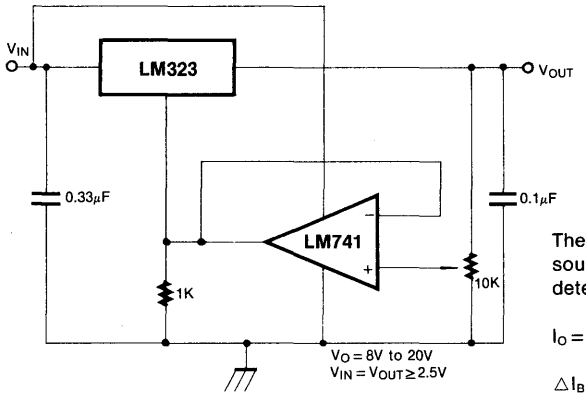


TYPICAL APPLICATION

The LM323 fixed voltage regulator is designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

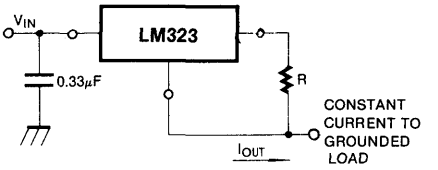
In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIG. 13 ADJUSTABLE OUTPUT REGULATOR



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.

FIG. 14 CURRENT REGULATOR



The LM323 regulator can also be used as a current source when connected as above. Resistor R determines the current as follows:

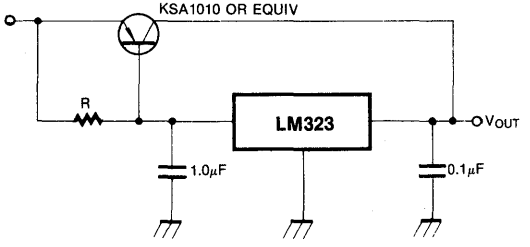
$$I_O = \frac{5.0V}{R} + I_B$$

$\triangle I_B = 0.7mA$ over line, load and temperature changes

$I_B = 3.5mA$

For example, a 2-ampere current source would require R to be a 2.5 ohm, 15W resistor and the output voltage compliance would be the input voltage less 7.5 volts.

FIG. 15 CURRENT BOOST REGULATOR

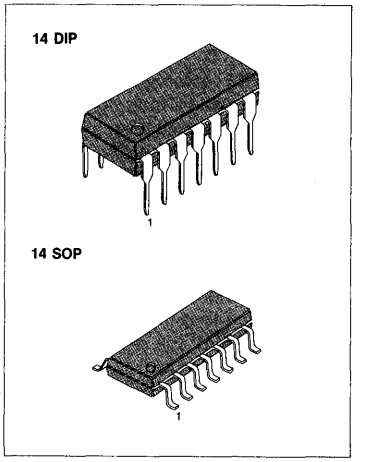


The LM323 can be current boosted with a PNP transistor. The KSA1010 provides current to 15 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

PRECISION VOLTAGE REGULATOR

The LM723C/LM723I are monolithic integrated circuit voltage regulator featuring high ripple rejection, excellent output and load regulation, excellent temperature stability, and low standby current.

The LM723C/LM723I are also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller. LM723C is characterized for operation from 0°C to 70°C, and LM723I from −25°C to +85°C.



FEATURES

- **Positive or Negative Supply Operation.**
- **0.01% line and load regulation**
- **Output voltage adjustable from 2 to 37 volts.**
- **Output current to 150mA without external pass transistor**

BLOCK DIAGRAM

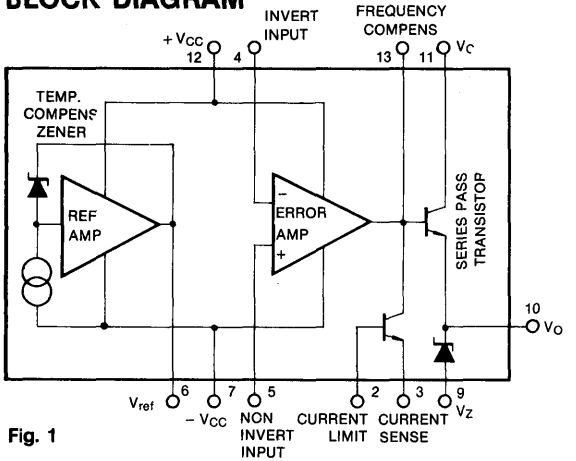


Fig. 1

ORDERING INFORMATION

Device	Package	Operating Temperature
LM723CN	14 DIP	0 ~ +70°C
LM723CD	14 SOP	
LM723IN	14 DIP	−25 ~ +85°C
LM723ID	14 SOP	

SCHEMATIC DIAGRAM

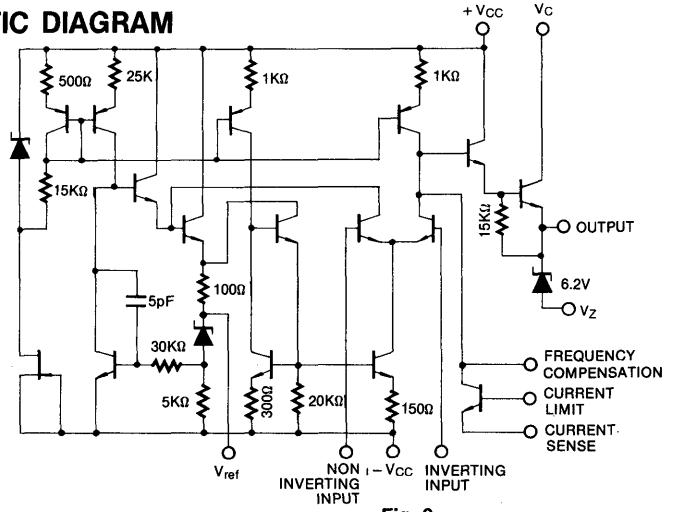


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Pulse Voltage from V+ to V− (50ms)	$V_{IN(P)}$	50	V_{peak}
Continus Voltage from V+ to V−	V_{IN}	40	V
Input-Output Voltage Differential	$V_{IN} - V_{OUT}$	40	V
Maximum Output Current	I_O	150	mA
Differential Input Voltage	V_{ID}	±5	V
Voltage Between Non-Inverting Input and V−	V_{IE}	8	V
Current from V_Z	I_Z	25	mA
Current from V_{REF}	I_{REF}	15	mA
Power Dissipation	P_D	1000	mW
Operating Temperature Range LM7231 LM723C	T_{opr}	−25 ~ +85 0 ~ +70	°C °C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(unless otherwise specified, Ta = 25°C, $V_I = V_{CC} = V_C = 12V$, $V_O = +5V$, $I_L = 1.0mA$, $R_{SC} = 0$, $C_I = 100pF$, $C_{ref} = 0$ and devider impedance as seen by error Amplifier ≤ 10KΩ connected as shown in figure 3)

Characteristic	Symbol	Test Conditions	LM7231/LM723C Min	Typ	Max	Unit
Line Regulation	$\triangle V_O$	$V_I = 12V$ to $15V$ $V_I = 12V$ to $40V$		0.01 0.1	0.1 0.5	%
		$T_{MIN} \leq T_A \leq T_{MAX}$ $V_I = 12V$ to $15V$			0.3	
Load Regulation	$\triangle V_O$	$I_O = 1mA$ to $50mA$		0.03	0.2	%
		$T_{MIN} \leq T_A \leq T_{MAX}$ $I_O = 1$ to $50mA$			0.6	
Ripple Rejection	RR	$f = 100Hz$ to $10KHz$, $C_{REF} = 0$		74		dB
		$f = 100Hz$ to $10KHz$, $C_{REF} = 5\mu F$		86		
Average Temperature Coefficient of Output Voltage	$\triangle V_O/\triangle T$	$T_{MIN} \leq T_A \leq T_{MAX}$		0.003	0.015	%/°C
Short Circuit Current Limit	I_{SC}	$R_{SC} = 10\Omega$, $V_O = 0$		65		mA
Reference Voltage	V_{REF}		6.80	7.15	7.50	V
Output Noise Voltage	V_N	$f = 100Hz$ to $10KHz$, $C_{REF} = 0$		20		μV_{rms}
		$f = 100Hz$ to $10KHz$, $C_{REF} = 5\mu F$		2.5		
Long-term Stability	V_O/T			0.1		%/1000HR
Standby Current Drain	I_D	$I_L = 0$, $V_{IN} = 30V$		2.0	4.0	mA
Input Voltage Range	V_I		9.5		40	V
Output Voltage Range	V_O		2.0		37	V
Input-Output Voltage Differential	V_D		3.0		38	V

* Note: $T_{MIN} = 0°C$ for LM723C, $= -25°C$ for LM723I; $T_{MAX} = 70°C$ for LM723C, $= 85°C$ for LM723I

Table 1 — Resistor values (KΩ) for standard output voltage

Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10%			Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10%		
		R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3	3, 6	4.12	3.01	1.8	0.5	1.2	−6*	5	3.57	2.43	1.2	0.5	0.75
+5	3, 6	2.15	4.99	0.75	0.5	2.2	−9	5	3.48	5.36	1.2	0.5	2
+6	3, 6	1.15	6.04	0.5	0.5	2.7	−12	5	3.57	8.45	1.2	0.5	3.3
+9	4, 6	1.87	7.15	0.75	1	2.7	−15	5	3.65	11.5	1.2	0.5	4.3
+12	4, 6	4.87	7.15	2	2	3	−28	5	3.57	24.3	1.2	0.5	10
+15	4, 6	7.87	7.15	3.3	1	3							
+28	4, 6	21	7.15	5.6	1	2							

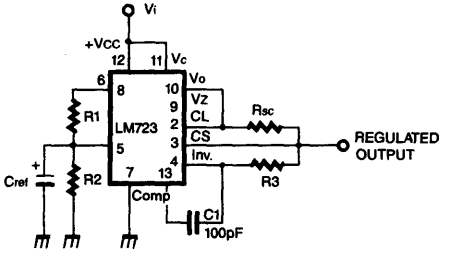
Note: *V_{CC} must be connected to a +3V or greater supply.

Table II — Formulae for intermediate output voltages

Outputs from +2 to +7 volts Fig. 3 $V_o = [V_{ref} \times \frac{R_2}{R_1 + R_2}]$	Foldback Current Limiting $I_{KNEE} = [\frac{V_o R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts Fig. 4, 6 $V_o = [V_{ref} \times \frac{R_1 + R_2}{R_2}]$	Output from −6 to −250 volts Fig. 5 $V_o = [\frac{V_{ref}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	

APPLICATION INFORMATION

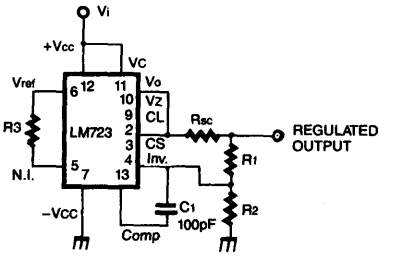
Fig. 3 Basic low voltage regulator ($V_O = 2$ to 7V)



Note: R3=R1 • R2/(R1+R2) for minimum temperature drift.
R3 may be eliminated for minimum component count.

Typical performance
Regulated Output Voltage 5V
Line Regulation ($\Delta V_i = 3V$) 0.5mV
Load Regulation ($\Delta I_o = 50mA$) 1.5mV

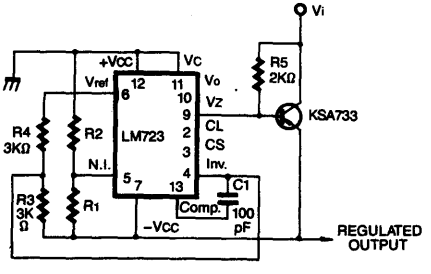
Fig. 4 Basic high voltage regulator ($V_O = 7$ to 37V)



Note: R1•R2/(R1+R2)for minimum temperature drift.
R3 may be eliminated for minimum component count.

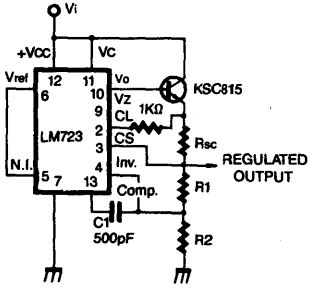
Typical performance
Regulated Output Voltage 15V
Line Regulation ($\Delta V_i = 3V$) 1.5mV
Load Regulation ($\Delta I_o = 50mA$) 4.5mV

Fig. 5 Negative voltage regulator



Typical performance
Regulated output Voltage ..... -15V
Line Regulation ($\Delta V_i = 3V$) 1mV
Load Regulation ($\Delta I_o = 100mA$) 2mV

Fig. 6 Positive voltage regulator
(Extenal NPN Pass Transistor)



Typical performance
Regulated Output Voltage ..... +15V
Line Regulation ($\Delta V_i = 3V$) 1.5mV
Load Regulation ($\Delta I_o = 1A$) 15mV

Fig. 7 MAXIMUM OUTPUT CURRENT VS. VOLTAGE DROP

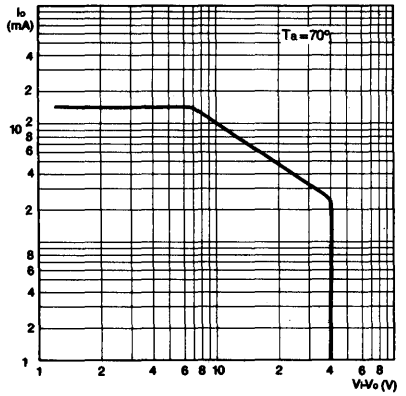


Fig. 8 CURRENT LIMITING CHARACTERISTICS

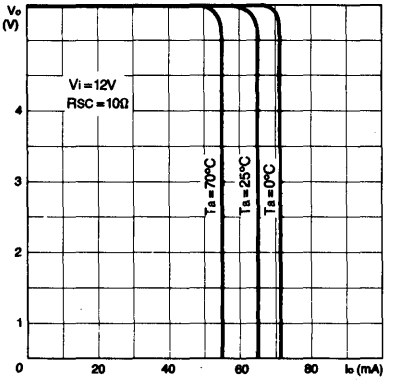


Fig. 9 CURRENT LIMITING CHARACTERISTICS VS. JUNCTION TEMPERATURE

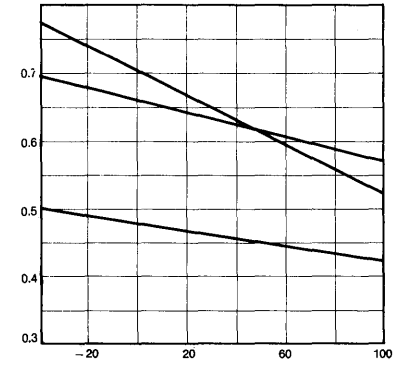


Fig. 10 LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

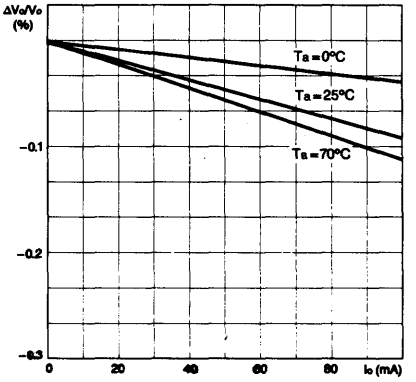


Fig. 11 LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

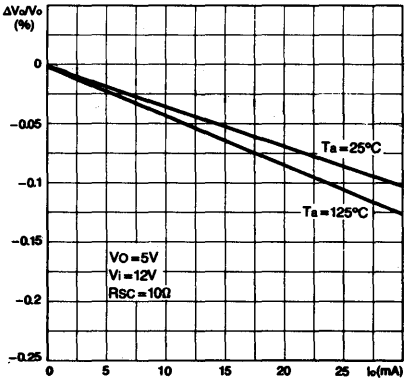


Fig. 12 LOAD REGULATION CHARACTERISTIC WITH CURRENT LIMITING

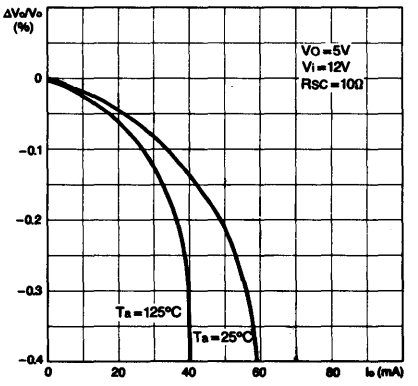


Fig. 13 LINE REGULATION—VOLTAGE DROP

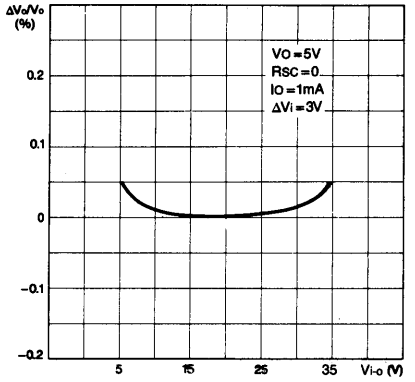


Fig. 14 LOAD REGULATION—VOLTAGE DROP

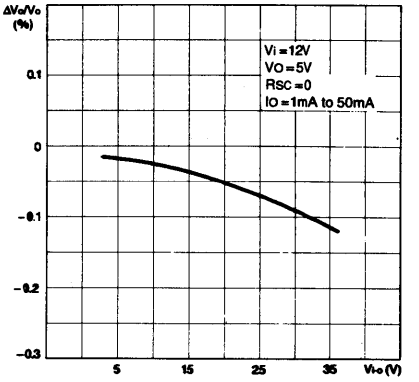


Fig. 15 QUIESCENT DRAIN CURRENT VS. INPUT VOLTAGE

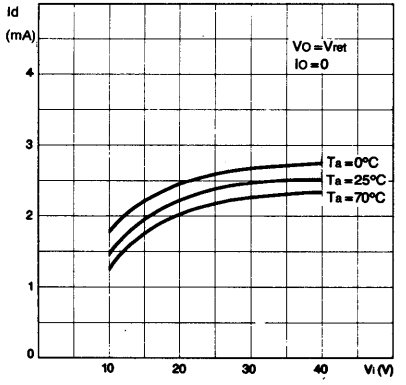


Fig. 16 LINE TRANSIENT RESPONSE

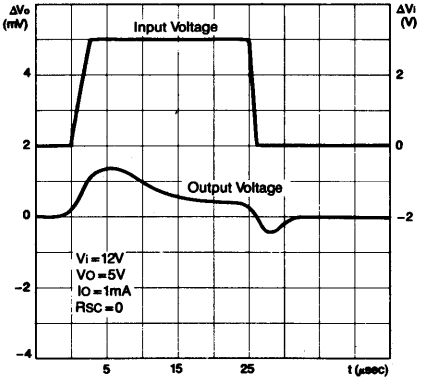


Fig. 17 LOAD TRANSIENT RESPONSE

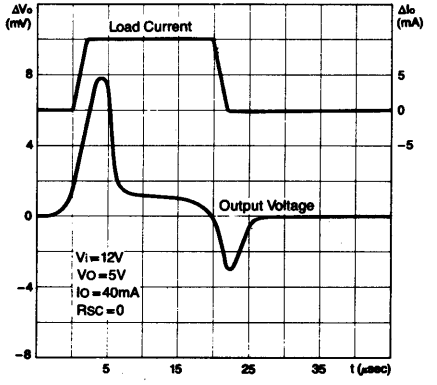
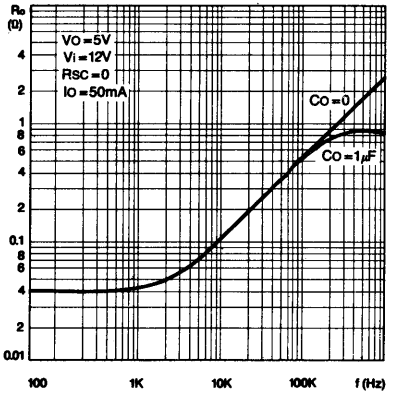


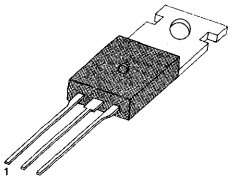
Fig. 18 OUTPUT IMPEDANCE VS. FREQUENCY



3-TERMINAL 1A POSITIVE VOLTAGE REGULATORS

The MC78XX/MC78XXA series of three-terminal positive regulators are available in TO-220 package and with several fixed output voltages, making it useful in a wide range of applications. These Regulators can provide local oncard regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.
MC78XXI is characterized for operation from −40°C to +125°C, and MC78XXC from 0°C to +125°C.

TO-220



1: Input 2: GND 3: Output

FEATURES

- **Output Current up to 1.5A**
- **Output voltages of 5; 6; 8; 8.5; 9; 10; 11; 12; 15; 18; 24V**
- **Thermal Overload Protection**
- **Short Circuit Protection**
- **Output Transistor SOA Protection**
- **No external components required**
- **Output current in excess of 1A**
- **Industrial and commercial temperature range**

ORDERING INFORMATION

Device	Package	Operating Temperature
MC78XXIT	TO-220	−40 ~ +125°C
MC78XXCT	TO-220	0 ~ +125°C
MC78XXACT	TO-220	

BLOCK DIAGRAM

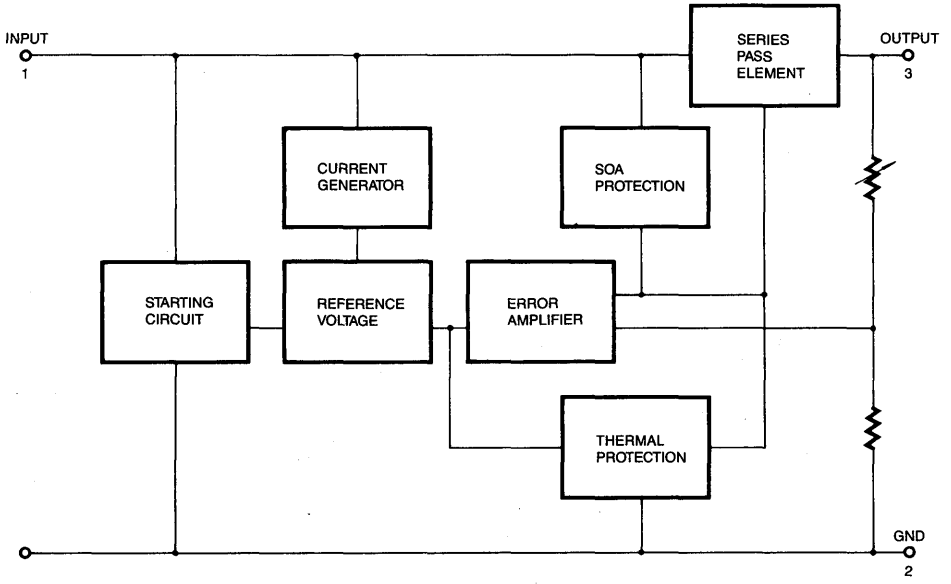


Fig. 1

SCHEMATIC DIAGRAM

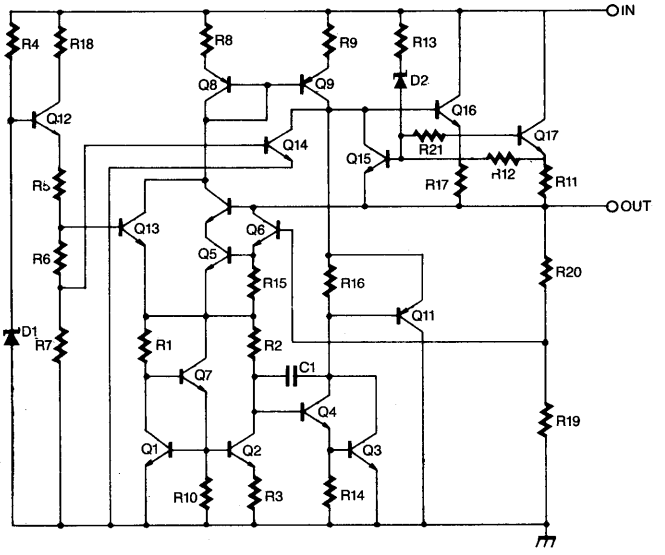


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_{IN} V_{IN}	35 40	V V
Thermal Resistance Junction-Cases	θ_{JC}	5	°C/W
Thermal Resistance Junction-Air	θ_{JA}	65	°C/W
Operating Temperature Range MC78XXI MC78XXC/AC	T_{opr}	−40 ~ +125 0 ~ +125	°C °C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS MC7805

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 10V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7805I			MC7805C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		4.8	5.0	5.2	4.8	5.0	5.2	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 7V$ to $20V$ $V_i = 8V$ to $20V$		4.75	5.0	5.25	4.75	5.0	5.25	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 7V$ to $25V$		5.0	100		5.0	100	mV
			$V_i = 8V$ to $12V$		1.5	50		1.5	50	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $1.5A$		9	100		9	100	mV
			$I_o = 250mA$ to $750mA$		3	50		3	50	
Quiescent Current	I_d	$T_j = 25°C$			5.0	8		5.0	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 7V$ to $25V$							1.3	
		$V_i = 8V$ to $25V$				1.3				
Output Voltage Drift	$\triangle V_o / \triangle T$	$I_o = 5mA$			-0.8			-0.8		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			40			40		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 8$ to $18V$		62	78		62	78		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			17			17		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			250			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
  MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
  MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$
* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7806

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 11V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7806I			MC7806C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		5.75	6.0	6.25	5.75	6.0	6.25	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 8.0V$ to $21V$ $V_i = 9.0V$ to $21V$		5.7	6.0	6.3	5.7	6.0	6.3	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 8V$ to $25V$		5	120		5	120	mV
			$V_i = 9V$ to $13V$		1.5	60		1.5	60	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		9	120		9	120	mV
			$I_o = 250mA$ to $750mA$		3	60		3	60	
Quiescent Current	I_d	$T_j = 25°C$			5.0	8		5.0	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$				0.5			0.5	mA
		$V_i = 8V$ to $25V$							1.3	
		$V_i = 9V$ to $25V$				1.3				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			−0.8			−0.8		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			45			45		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 9$ to $19V$		59	75		59	75		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			19			19		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			250			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

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ELECTRICAL CHARACTERISTICS MC7808

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 14V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7808I			MC7808C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		7.7	8.0	8.3	7.7	8.0	8.3	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 10.5V$ to $23V$ $V_i = 11.5V$ to $23V$		7.6	8.0	8.4	7.6	8.0	8.4	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 10.5V$ to $25V$		6.0	160		6.0	160	mV
			$V_i = 11.5V$ to $17V$		2.0	80		2.0	80	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $1.5A$		12	160		12	160	mV
			$I_o = 250mA$ to $750mA$		4.0	80		4.0	80	
Quiescent Current	I_d	$T_j = 25°C$			5.0	8		5.0	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 10.5V$ to $25V$							1.0	
		$V_i = 11.5V$ to $25V$				1.0				
Output Voltage Drift	$\triangle V_o / \triangle T$	$I_o = 5mA$			-0.8			-0.8		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			52			52		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 11.5V$ to 21.5		56	72		56	72		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			16			16		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			250			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7885

(Refer to test circuit $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 14.5V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7885I			MC7885C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		8.15	8.5	8.85	8.15	8.5	8.85	V
		$I_o = 5mA$ to $1.0A$, $P_D \leq 15W$ $V_i = 11V$ to $23.5V$ $V_i = 12V$ to $23.5V$		8.1	8.5	8.9	8.1	8.5	8.9	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 11V$ to $25V$		6	170		6	170	mV
			$V_i = 11.5V$ to $18V$		2	85		2	85	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		12	170		12	170	mV
			$I_o = 250mA$ to $750mA$		4	85		4	85	
Quiescent Current	I_d	$T_j = 25°C$			5.0	8.0		5.0	8.0	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 11V$ to $25V$							1.0	
		$V_i = 12V$ to $25V$				1.0				
Output Voltage Drift	$\triangle V_o / \triangle T$	$I_o = 5mA$			−1.0			−1.0		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$, $Ta = 25°C$			55			55		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 12V$ to $22V$		56	72		56	72		dB
Dropout Voltage	V_D	$I_o = 1.0A$, $T_j = 25°C$			2.0			2.0		V
Output Resistance	R_0	$f = 1KHz$			17			17		mΩ
Short Circuit Current	I_{sc}	$V_i = 35V$, $T_j = 25°C$			250			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC: $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7809

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 15V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7809I			MC7809C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		8.65	9	9.35	8.65	9	9.35	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 11.5V$ to $24V$ $V_i = 12.5V$ to $24V$		8.6	9	9.4	8.6	9	9.4	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 11.5V$ to $25V$		6	180		6	180	mV
			$V_i = 12V$ to $25V$		2	90		2	90	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		12	180		12	180	mV
			$I_o = 250mA$ to $750mA$		4	90		4	90	
Quiescent Current	I_d	$T_j = 25°C$			5.0	8		5.0	8.0	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 11.5V$ to $26V$							1.3	
		$V_i = 12.5V$ to $26V$				1.3				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-1			-1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			58			58		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 13V$ to $23V$		56	71		56	71		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			17			17		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			250			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
  MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
  MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$
* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7810

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 16V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7810I			MC7810C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		9.6	10	10.4	9.6	10	10.4	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 12.5V$ to $25V$ $V_i = 13.5V$ to $25V$		9.5	10	10.5	9.5	10	10.5	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 12.5V$ to $25V$		10	200		10	200	mV
			$V_i = 13V$ to $20V$		3	100		3	100	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		12	200		12	200	mV
			$I_o = 250mA$ to $750mA$		4	100		4	100	
Quiescent Current	I_d	$T_j = 25°C$			5.1	8		5.1	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 12.5V$ to $29V$							1.0	
		$V_i = 13.5V$ to $29V$				1.0				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-1			-1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			58			58		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 14V$ to $23V$		56	71		56	71		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			17			17		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			250			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

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ELECTRICAL CHARACTERISTICS MC7811

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 18V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7811I			MC7811C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		10.6	11	11.4	10.6	11	11.4	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 13.5V$ to $26V$ $V_i = 14.5V$ to $26V$		10.5	11	11.5	10.5	11	11.5	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 13.5$ to $25V$		10	220		10	220	mV
			$V_i = 14$ to $21V$		3.0	110		3.0	110	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $1.5A$		12	220		12	220	mV
			$I_o = 250mA$ to $750mA$		4	110		4	110	
Quiescent Current	I_d	$T_j = 25°C$			5.1	8		5.1	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$				0.5			0.5	mA
		$V_i = 13.5V$ to $29V$							1.0	
		$V_i = 14.5V$ to $29V$				1.0				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			−1			−1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			70			70		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 14V$ to $24V$		55	71		55	71		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			18			18		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			250			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7812

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 19V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7812I			MC7812C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		11.5	12	12.5	11.5	12	12.5	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_{in} = 14.5V$ to $27V$ $V_i = 15.5V$ to $27V$		11.4	12	12.6	11.4	12	12.6	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 14.5$ to $30V$		10	240		10	240	mV
			$V_i = 16$ to $22V$		3.0	120		3.0	120	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		12	240		12	240	mV
			$I_o = 250mA$ to $750mA$		4.0	120		4.0	120	
Quiescent Current	I_d	$T_j = 25°C$			5.1	8		5.1	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 14.5V$ to $30V$							1.0	
		$V_i = 15V$ to $30V$				1.0				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-1			-1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			75			75		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 15V$ to $25V$		55	71		55	71		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			18			18		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			250			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

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ELECTRICAL CHARACTERISTICS MC7815

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 23V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7815I			MC7815C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		14.4	15	15.6	14.4	15	15.6	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 17.5V$ to $30V$ $V_i = 18.5V$ to $30V$		14.25	15	15.75	14.25	15	15.75	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 17.5$ to $30V$		11	300		11	300	mV
			$V_i = 20$ to $26V$		3	150		3	150	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $1.5A$		12	300		12	300	mV
			$I_o = 250mA$ to $750mA$		4	150		4	150	
Quiescent Current	I_d	$T_j = 25°C$			5.2	8		5.2	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 17.5V$ to $30V$							1.0	
		$V_i = 18.5V$ to $30V$				1.0				
Output Voltage Drift	$\triangle V_o / \triangle T$	$I_o = 5mA$			-1			-1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			90			90		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 18.5V$ to $28.5V$		54	70		54	70		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			19			19		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			250			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
  MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
  MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$
* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7818

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 27V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7818I			MC7818C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		17.3	18	18.7	17.3	18	18.7	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 21V$ to $33V$					17.1	18	18.9	
		$V_i = 22V$ to $33V$		17.1	18	18.9				
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 21$ to $33V$		15	360		15	360	mV
			$V_i = 24$ to $30V$		5	180		5	180	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		15	360		15	360	mV
			$I_o = 250mA$ to $750mA$		5.0	180		5.0	180	
Quiescent Current	I_d	$T_j = 25°C$			5.2	8		5.2	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$				0.5			0.5	mA
		$V_i = 21V$ to $33V$							1	
		$V_i = 22V$ to $33V$				1				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-1			-1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			110			110		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 22V$ to $32V$		53	69		53	69		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			22			22		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			250			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

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ELECTRICAL CHARACTERISTICS MC7824

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 33V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7824I			MC7824C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		23	24	25	23	24	25	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 27V$ to $38V$ $V_i = 28V$ to $38V$		22.8	24	25.2	22.8	24	25.2	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 27V$ to $38V$		18	480		18	480	mV
			$V_i = 30V$ to $36V$		6	240		6	240	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		15	480		15	480	mV
			$I_o = 250mA$ to $750mA$		5.0	240		5.0	240	
Quiescent Current	I_d	$T_j = 25°C$			5.2	8		5.2	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$				0.5			0.5	mA
		$V_i = 27V$ to $38V$							1	
		$V_i = 28V$ to $38V$				1				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			−1.5			−1.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			170			170		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 28V$ to $38V$		50	66		50	66		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			28			28		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			250			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7805AC

(Refer to the test circuits, T_j=0 to 125°C, I_o=1A, V_i=10V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	4.9	5	5.1	V
		I_o=5mA to 1A, $P_D \leq$15W V_i=7.5 to 20V	4.8	5	5.2	
*Line Regulation	ΔV_o	V_i=7.5 to 25V, I_o=500mA		5	50	mV
		V_i=8 to 12V		3	50	
		T_j=25°C, V_i=7.3 to 25V		5	50	
		T_j=25°C, V_i=8 to 12V		1.5	25	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A		9	100	mV
		I_o=5mA to 1A		9	100	
		I_o=250 to 750mA		4	50	
Quiescent Current	I_d	T_j=25°C		5.0	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=8 to 25V, I_o=500mA			0.8	
		V_i=7.5 to 20V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=5mA		−0.8		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz: T_a=25°C		10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA V_i=8 to 18V		68		dB
Dropout Voltage	V_D	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		17		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		250		mA
Peak Current	I_{peak}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7806AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=11V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	5.88	6	6.12	V
		I_o=5mA to 1A, $P_D \leq$ 15W, V_i=8.6 to 21V	5.76	6	6.24	
*Line Regulation	ΔV_o	V_i=8.6 to 25V, I_o=500mA		5	60	mV
		V_i=9 to 13V		3	60	
		T_j=25°C, V_i=8.3 to 21V		5	60	
		T_j=25°C, V_i=9 to 13V		1.5	30	
*Load Regulation	ΔV_o	T_j=25°C, I_o=5mA to 1.5A		9	100	mV
		I_o=5mA to 1A		4	100	
		I_o=250 to 750mA		5.0	50	
Quiescent Current	I_d	T_j=25°C		4.3	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=9 to 25V, I_o=500mA			0.8	
		V_i=8.6 to 21V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=5mA		-0.8		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz, T_a=25°C		10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA, V_i=9 to 19V		65		dB
Dropout Voltage	V_d	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		17		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		250		mA
Peak Current	I_{peak}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7808AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1 A, V_i=14V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	7.84	8	8.16	V
		I_o=5mA to 1A, $P_D \leq$15W V_i=10.6 to 23V	7.7	8	8.3	
*Line Regulation	ΔV_o	V_i=10.6 to 25V, I_o=500mA		6	80	mV
		V_i=11 to 17V		3	80	
		T_j=25°C, V_i=10.4 to 23V		6	80	
		T_j=25°C, V_i=11 to 17V		2	40	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A		12	100	mV
		I_o=5mA to 1A		12	100	
		I_o=250 to 750mA		5	50	
Quiescent Current	I_d	T_j=25°C		5.0	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=11 to 25V, I_o=500mA			0.8	
		V_i=10.6 to 23V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=5mA		-0.8		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz T_a=25°C		10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA V_i=11.5 to 21.5V		62		dB
Dropout Voltage	V_D	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		18		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		250		mA
Peak Current	I_{peak}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7885AC

(Refer to the test circuits, $T_j = 0$ to 125°C, $I_o = 1A$, $V_i = 14V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	8.33	8.5	8.67	V
		$I_o = 5mA$ to 1.0A, $P_D \leq 15W$ $V_i = 11.2V$ to 23.5V	8.15	8.5	8.85	
Line Regulation	$\triangle V_o$	$V_i = 11.2V$ to 25V $I_o = 500mA$		6	85	mV
		$V_i = 11.5V$ to 18V		3	43	
		$T_j = 25°C$, $V_i = 11V$ to 23.5V		6	85	
		$T_j = 25°C$, $V_i = 11.5V$ to 18V		2	43	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to 1.5A		12	100	mV
		$I_o = 5mA$ to 1.0A		12	100	
		$I_o = 250mA$ to 750mA		5	50	
Quiescent Current	I_d	$T_j = 25°C$		5.0	6.0	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to 1.0A			0.5	mA
		$V_i = 11.5V$ to 25V, $T_j = 25°C$			0.8	
		$V_i = 11.2V$ to 23.5V, $I_o = 500mA$			0.8	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$		−1.0		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to 100KHz, $Ta = 25°C$		10		$\mu V/V_o$
Ripple Rejection	RR	$f = 120Hz$, $V_i = 12V$ to 22V $I_o = 500mA$		62		dB
Dropout Voltage	V_D	$I_o = 1.0A$, $T_j = 25°C$		2.0		V
Output Resistance	R_o	$f = 1KHz$		17		m
Short Circuit Current	I_{short}	$V_i = 35V$, $T_a = 25°C$		250		mA
Peak Current	I_{peak}	$T_j = 25°C$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7809AC

(Refer to the test circuits, $T_j = 0$ to 125°C, $I_o = 1A$, $V_i = 15V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		8.82	9.0	9.18	V
		$I_o = 5mA$ to 1.0A, $P_D \leq 15W$ $V_i = 11.2V$ to 24V		8.65	9.0	9.35	
Line Regulation	$\triangle V_o$	$V_i = 11.7V$ to 25V $I_o = 500mA$			6	90	mV
		$V_i = 12.5V$ to 19V			4	45	
		$T_j = 25°C$	$V_i = 11.5V$ to 24V		6	90	
			$V_i = 12.5V$ to 19V		2	45	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to 1.0A			12	100	mV
		$I_o = 5mA$ to 1.0A			12	100	
		$I_o = 250mA$ to 750mA			5	50	
Quiescent Current	I_d	$T_j = 25°C$			5.0	6.0	mA
Quiescent Current Change	$\triangle I_d$	$V_i = 11.7V$ to 24V, $T_j = 25°C$				0.8	mA
		$V_i = 12V$ to 25V, $I_o = 500mA$				0.8	
		$I_o = 5mA$ to 1.0A				0.5	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			−1.0		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, Ta = 25°C			10		$\mu V/V_o$
Ripple Rejection	RR	f = 120Hz, $V_i = 12V$ to 22V $I_o = 500mA$			62		dB
Dropout Voltage	V_D	$I_o = 1.0A$, $T_j = 25°C$			2.0		V
Output Resistance	R_o	f = 1KHz			17		m
Short Circuit Current	I_{short}	$V_i = 35V$, $T_j = 25°C$			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7811AC

(Refer to the test circuits, $T_j = 0$ to 125°C, $I_o = 1A$, $V_i = 18V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	10.8	11.0	11.2	V
		$I_o = 5mA$ to 1.0A, $P_D \leq 15W$ $V_i = 13.8V$ to 26V	10.6	11.0	11.4	
Line Regulation	$\triangle V_o$	$V_i = 13.8V$ to 27V $I_o = 500mA$		10	110	mV
		$V_i = 15V$ to 21V		4	55	
		$T_j = 25°C$, $V_i = 13.5V$ to 26V		10	110	
		$T_j = 25°C$, $V_i = 15V$ to 21V		3	5.5	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to 1.5A		12	100	mV
		$I_o = 5mA$ to 1.0A		12	100	
		$I_o = 250mA$ to 750mA		5	50	
Quiescent Current	I_d	$T_j = 25°C$		5.1	6.0	mA
					6.0	
Quiescent Current Change	$\triangle I_d$	$V_i = 13.8V$ to 26V, $T_j = 25°C$			0.8	mA
		$V_i = 14V$ to 27V, $I_o = 500mA$			0.8	
		$I_o = 5mA$ to 1.0A			0.5	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$		-1.0		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, Ta = 25°C		10		$\mu V/V_o$
Ripple Rejection	RR	f = 120Hz, $V_i = 14V$ to 24V $I_o = 500mA$		61		dB
Dropout Voltage	V_D	$I_o = 1.0A$, $T_j = 25°C$		2.0		V
Output Resistance	R_o	f = 1KHz		18		m
Short Circuit Current	I_{short}	$V_i = 35V$, $T_j = 25°C$		250		mA
Peak Current	I_{peak}	$T_j = 25°C$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7812AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=19V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	11.75	12	12.25	V
		I_o=5mA to 1A, $P_D \leq$ 15W, V_i=14.8 to 27V	11.5	12	12.5	
*Line Regulation	ΔV_o	V_i=14.8 to 30V, I_o=500mA		10	120	mV
		V_i=16 to 22V		4	120	
		T_j=25°C, V_i=14.5 to 27V		10	120	
		T_j=25°C, V_i=16 to 22V		3	60	
*Load Regulation	ΔV_o	T_j=25°C, I_o=5mA to 1.5A		12	100	mV
		I_o=5mA to 1A		12	100	
		I_o=250 to 750mA		5	50	
Quiescent Current	I_d	T_j=25°C		5.1	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=15 to 30V, I_o=500mA			0.8	
		V_i=14.8 to 27V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=5mA		-1		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz, T_a=25°C		10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA, V_i=15 to 25V		60		dB
Dropout Voltage	V_D	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		18		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		250		mA
Peak Current	I_{peak}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7815AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=23V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C		14.7	15	15.3	V
		I_o=5mA to 1A, $P_D \leq$ 15W V_i=17.7 to 30V		14.4	15	15.6	
*Line Regulation	ΔV_o	V_i=17.9 to 30V, I_o=500mA			10	150	mV
		V_i=20 to 26V			5	150	
		T_j=25°C	V_i=17.5 to 30V		11	150	
			V_i=20 to 26V		3	75	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A			12	100	mV
		I_o=5mA to 1A			12	100	
		I_o=250 to 750mA			5	50	
Quiescent Current	I_d	T_j=25°C			5.2	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A				0.5	mA
		V_i=17.5 to 30V, I_o=500mA				0.8	
		V_i=17.5 to 30V, T_j=25°C				0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=5mA			−1		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz T_a=25°C			10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA V_i=18.5 to 28.5V			58		dB
Dropout Voltage	V_D	I_o=1A, T_j=25°C			2		V
Output Resistance	R_o	f=1KHz			19		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C			250		mA
Peak Current	I_{peak}	T_j=25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7818AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=27V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	17.64	18	18.36	V
		I_o=5mA to 1A, $P_D \leq$ 15W, V_i=21 to 33V	17.3	18	18.7	
*Line Regulation	ΔV_o	V_i=21 to 33V, I_o=500mA		15	180	mV
		V_i=24 to 30V		5	180	
		T_j=25°C, V_i=20.6 to 33V		15	180	
		T_j=25°C, V_i=24 to 30V		5	90	
*Load Regulation	ΔV_o	T_j=25°C, I_o=5mA to 1.5A		15	100	mV
		I_o=5mA to 1A		15	100	
		I_o=250 to 750mA		7	50	
Quiescent Current	I_d	T_j=25°C		5.2	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=21 to 33V, I_o=500mA			0.8	
		V_i=21 to 33V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=5mA		-1		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz, T_a=25°C		10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA, V_i=22 to 32V		57		dB
Dropout Voltage	V_D	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		19		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		250		mA
Peak Current	I_{peak}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7824AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=33V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	23.5	24	24.5	V
		I_o=5mA to 1A, $P_D \leq$ 15W V_i=27.3 to 38V	23	24	25	
*Line Regulation	ΔV_o	V_i=27 to 38V, I_o=500mA		18	240	mV
		V_i=30 to 36V		6	240	
		T_j=25°C, V_i=26.7 to 38V		18	240	
		T_j=25°C, V_i=30 to 36V		6	120	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A		15	100	mV
		I_o=5mA to 1A		15	100	
		I_o=250 to 750mA		7	50	
Quiescent Current	I_d	T_j=25°C		5.2	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=27.3 to 38V, I_o=500mA			0.8	
		V_i=27.3 to 38V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=1mA		−1.5		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz T_a=25°C		10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA V_i=28 to 38V		54		dB
Dropout Voltage	V_D	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		20		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		250		mA
Peak Current	I_{peak}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TEST CIRCUIT

Fig. 3 DC Parameters

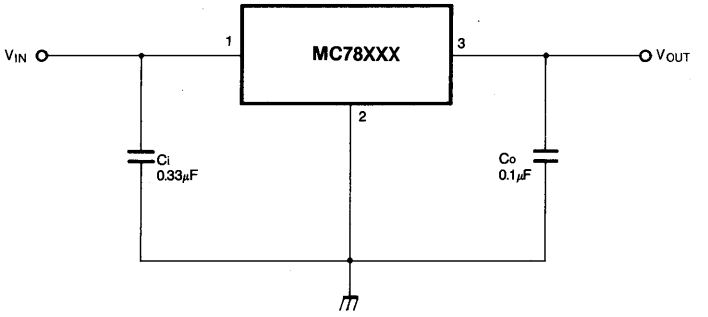


Fig. 4 Load Regulation

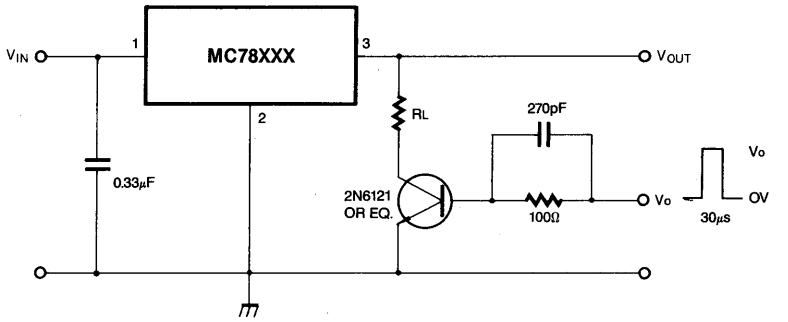
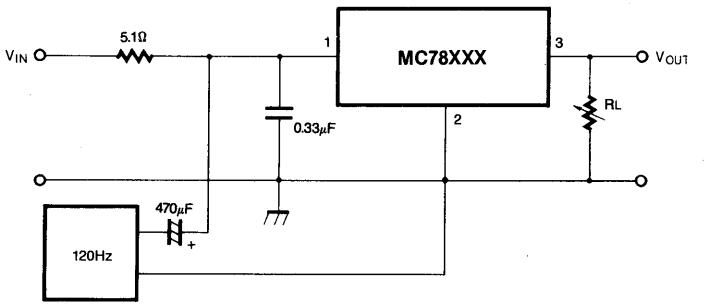


Fig. 5 Ripple Rejection



APPLICATION CIRCUIT

Fig. 6 Fixed Output Regulator

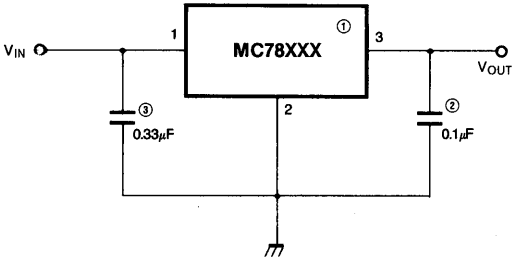
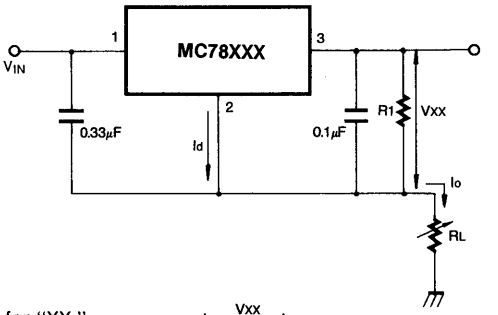


Fig. 7 Constant Current Regulator



$$I_o = \frac{V_{XX}}{R1} + I_d$$

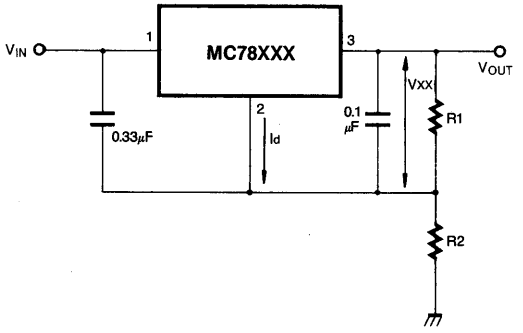
Notes:

(1) To specify an output voltage, substitute voltage value for "XX." A common ground is required between the input and the output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.

(2) C_{IN} is required if regulator is located an appreciable distance from power supply filter.

(3) C_{OUT} improves stability and transient response.

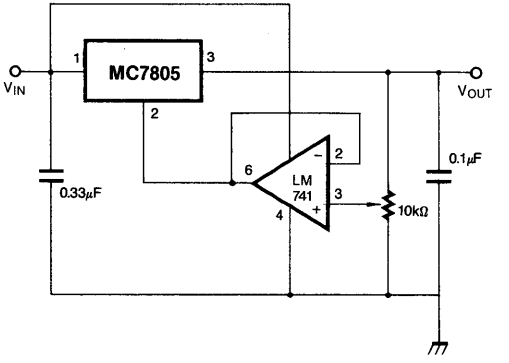
Fig. 8 Circuit for Increasing Output Voltage



$I_{R1} \geq 5I_d$

$V_O = V_{XX}(1+R_2/R_1)+I_d R_2$

Fig. 9 Adjustable Output Regulator (7 to 30V)



APPLICATION CIRCUIT (continued)

Fig. 10 0.5 to 10V Regulator

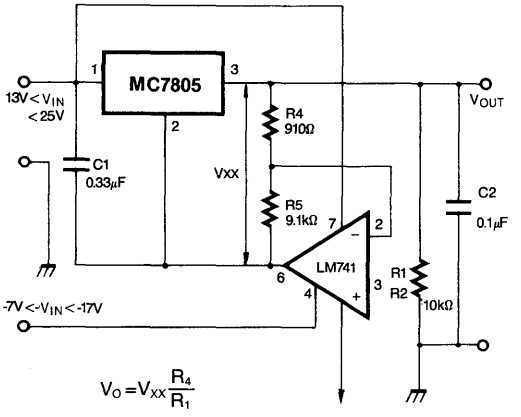


Fig. 11 High Current Voltage Regulator

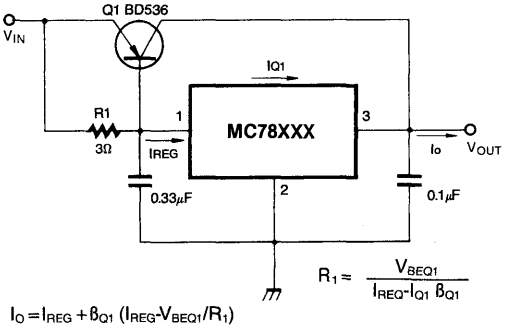


Fig. 12 High Output Current with Short Circuit Protection

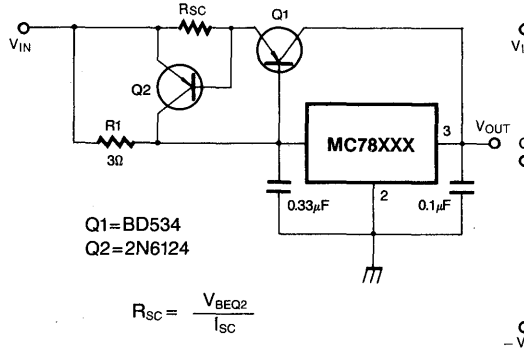


Fig. 13 Tracking Voltage Regulator

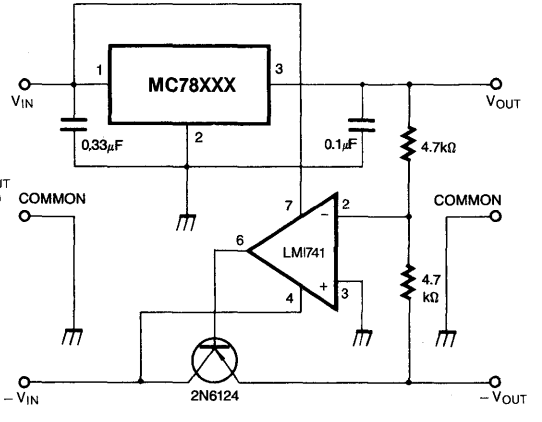


Fig. 14 Split Power Supply (±15V – 1A)

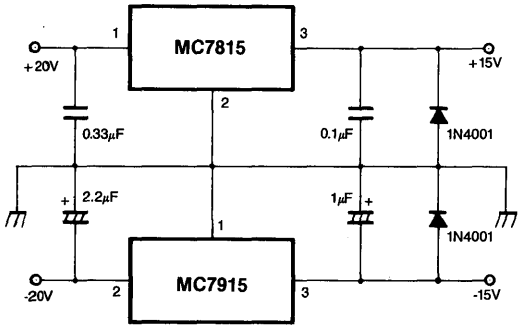


Fig. 15 Negative Output Voltage Circuit

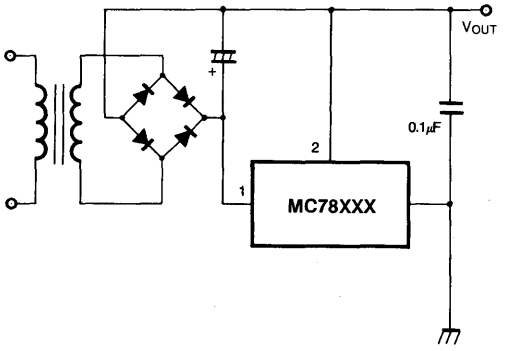


Fig. 16 Switching Regulator

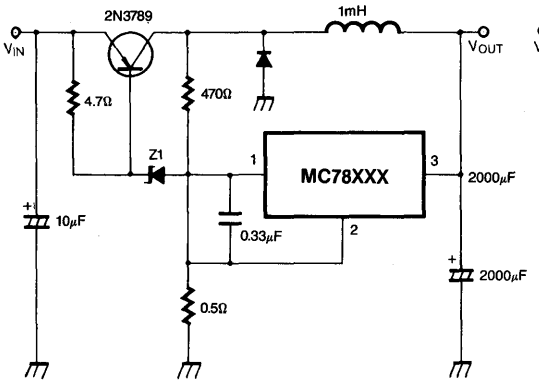
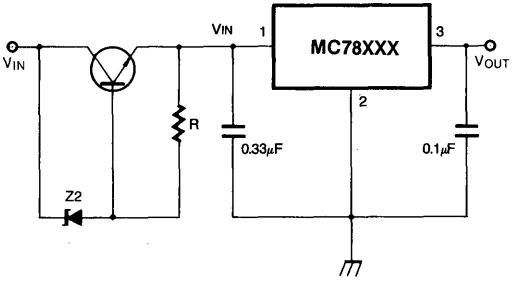


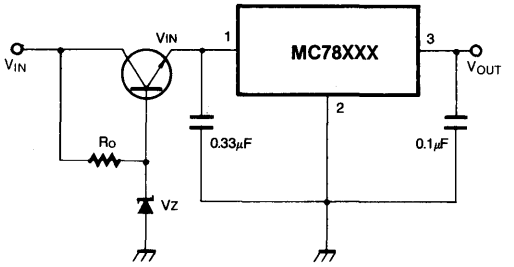
Fig. 17 High Input Voltage Circuit



$V_{IN} = V_i - (V_Z + V_{BE})$

APPLICATION CIRCUIT (continued)

Fig. 18 High Input Voltage Circuit



$V_{IN} = V_Z - V_{BE}$

Fig. 19 High Output Voltage Regulator

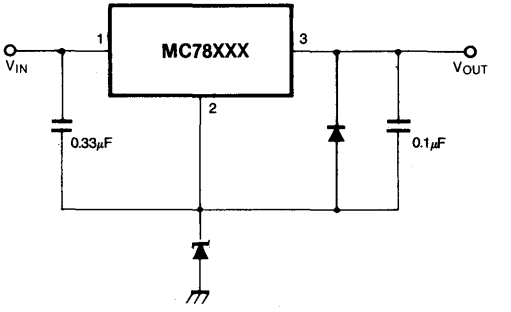
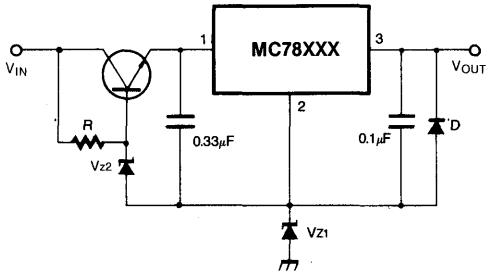
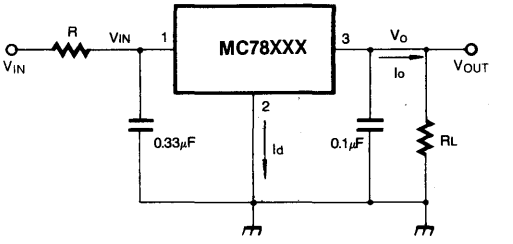


Fig. 20 High Input and Output Voltage



$V_O = V_{XX} + V_{Z1}$

Fig. 21 Reducing Power Dissipation with Dropping Resitor



$$R = \frac{V_{i\,(min)} - V_{XX} - V_{DROP\,(max)}}{I_{O\,(max)} + I_{O\,(max)}}$$

APPLICATION CIRCUIT (continued)

Fig. 22 Remote Shuntdown

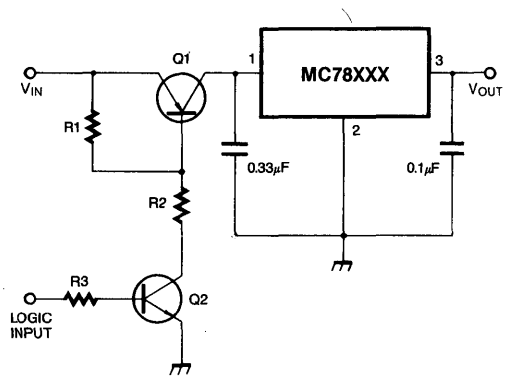
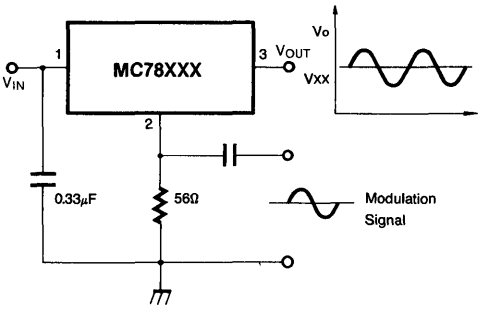
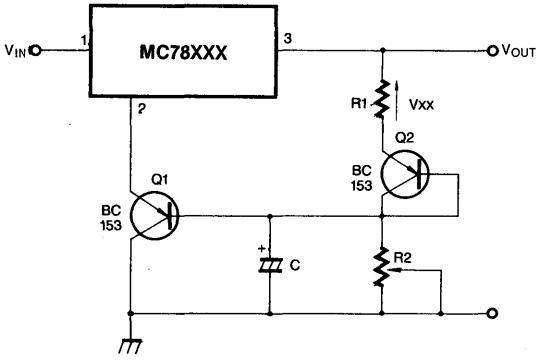


Fig. 23 Power AM Modulator



Note: The circuit performs well up to 100 KHz.

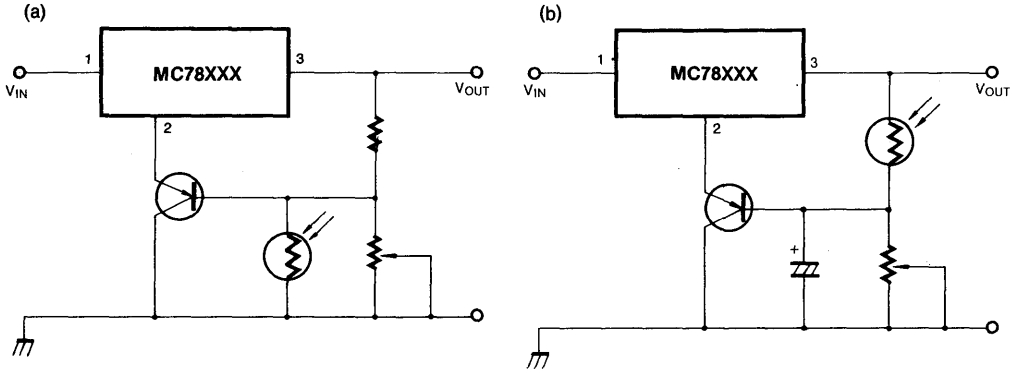
Fig. 24 Adjustable Output Voltage with Temperature Compensation



Note: Q2 is connected as a diode in order to compensate the variation of the Q1 V_{BE} with the temperature. C allows a slow rise-time of the V_O

$$V_O = V_{XX}\left(1+\frac{R_2}{R_1}\right) + V_{BE}$$

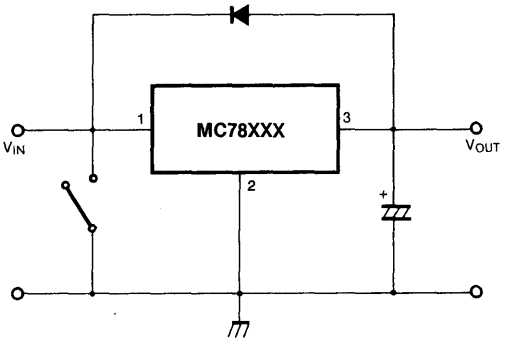
Fig. 25 Light Controllers (V_O min = V_{XX} + V_{BE})



V_O falls when the light goes up

V_O rises when the light goes up

Fig. 26 Protection Against Input Short-Circuit with High Capacitance Loads



Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 26) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the transistor may be destroyed. The external diode by-passes the current from the IC to ground.

TYPICAL PERFRMANCE CHARACTERISTIC

FIG. 27 QUIESCENT CURRENT

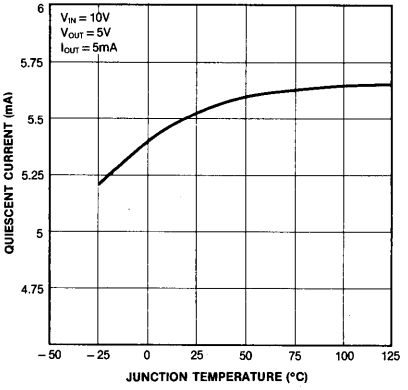


FIG. 28 PEAK OUTPUT CURRENT

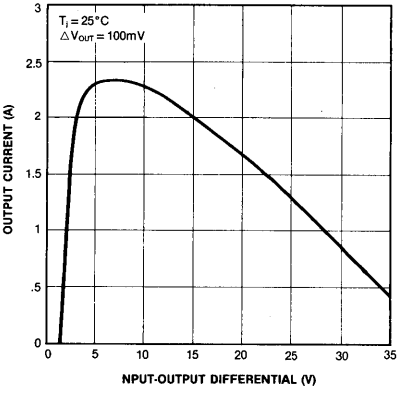


FIG. 29 OUTPUT VOLTAGE

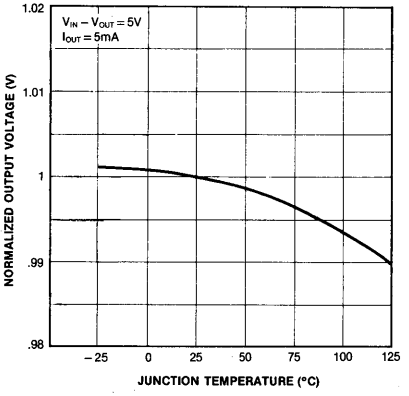
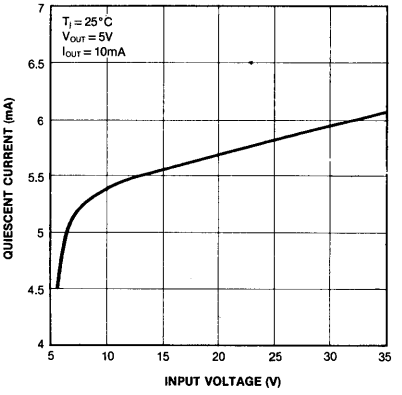


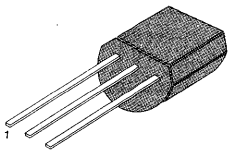
FIG. 30 QUIESCENT CURRENT



3-TERMINAL POSITIVE VOLTAGE REGULATORS

These regulators employ internal current-limiting and thermal-shutdown, making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 100mA output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high-current voltage regulators. The MC78LXXAC used as a Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnitude, along with lower quiescent current and lower noise.

TO-92



1: Output 2: GND 3: Input

FEATURES

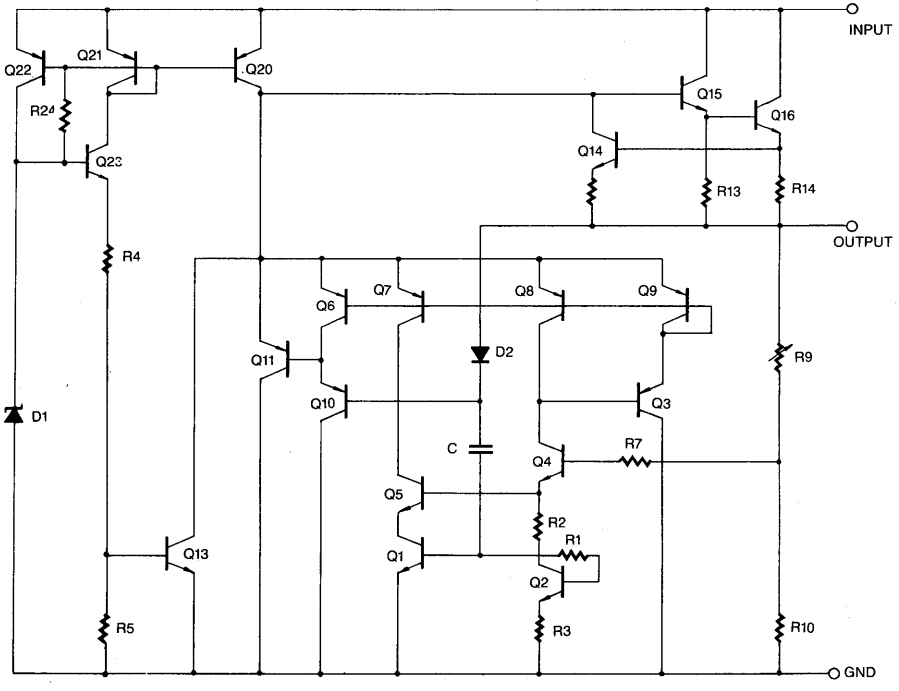
- **Output current up to 100mA.**
- **No external components required**
- **Internal thermal overload protection.**
- **Internal short circuit current limiting.**
- **Output voltage of 2.6V, 5V, 6.2V, 8V, 8.2V, 9V, 12V, 15V, 18V, and 24V.**
- **Output voltage tolerances of ±5% over the temperature range.**
- **Complementary negative regulators offered (MC79LXXAC)**

ORDERING INFORMATION

Device	Package	Operating Temperature
S78LXXACZ	TO-92	0 ~ +125°C
** S78LXXAIZ	TO-92	−40 ~ +125°C

** Under Development

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Input Voltage (for V_O = 2.6V to 9V) (for V_O = 12V to 18V) (for V_O = 24V)	V_{IN}	30 35 40	V V V
Operating Junction Temperature Range	T_{opr}	0 ~ + 125	°C
Storage Temperature Range	T_{stg}	− 65 ~ + 150	°C

MC78L26AC ELECTRICAL CHARACTERISTICS

V_{IN} =9V, I_{OUT} =40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j =25°C		2.5	2.6	2.7	V
Line Regulation		ΔV_O	T_j =25°C	4.75V ≤ V_{IN} ≤ 20V		40	100	mV
				5V ≤ V_{IN} ≤ 20V	30	75		mV
Load Regulation		ΔV_O	T_j =25°C	1mA ≤ I_{OUT} ≤ 100mA		10	50	mV
				1mA ≤ I_{OUT} ≤ 40mA		4.0	25	mV
Output Voltage		V_O	4.75V ≤ V_{IN} ≤ 20V	1mA ≤ I_{OUT} ≤ 40mA	2.45		2.75	V
			4.75V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	2.45		2.75	V
Quiescent Current		I_d	T_j =25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI_d	5V ≤ V_{IN} ≤ 20V				2.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a =25°C, 10Hz ≤ f ≤ 100KHz			30		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			− 0.4		mV/°C
Ripple Rejection		RR	f=120Hz, 6V ≤ V_{IN} ≤ 16V, Tj=25°C		43	51		dB
Dropout Voltage		V_D	T_j =25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j =25°C			140		mA

MC78L05AC ELECTRICAL CHARACTERISTICS

V_{IN} =10V, I_{OUT} =40mA, 0°C≤Tj≤125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j=25°C		4.8	5.0	5.2	V
Line Regulation		ΔV_O	T_j=25°C	7V≤V_{IN}≤20V		55	150	mV
				8V≤V_{IN}≤20V		45	100	mV
Load Regulation		ΔV_O	T_j=25°C	1mA≤I_{OUT}≤100mA		11	60	mV
				1mA≤I_{OUT}≤40mA		5.0	30	mV
Output Voltage		V_O	7V≤V_{IN}≤20V	1mA≤I_{OUT}≤40mA	4.75		5.25	V
			7V≤V_{IN}≤V_{max} (Note 2)	1mA≤I_{OUT}≤70mA	4.75		5.25	V
Quiescent Current		I_d	T_j=25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI_d	8V≤V_{IN}≤20V				1.5	mA
	with load	ΔI_d	1mA≤I_{OUT}≤40mA				0.1	mA
Output Noise Voltage		V_N	T_a=25°C, 10Hz≤f≤100KHz			40		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT}=5mA			−0.65		mV/°C
Ripple Rejection		RR	f=120Hz, 8V≤V_{IN}≤18V, Tj=25°C		41	49		dB
Dropout Voltage		V_D	T_j=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j=25°C			140		mA

MC78L62AC ELECTRICAL CHARACTERISTICS

V_{IN} =12V, I_{OUT} =40mA, 0°C≤Tj≤125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j=25°C		5.95	6.2	6.45	V
Line Regulation		ΔV_O	T_j=25°C	8.5V≤V_{IN}≤20V		65	175	mV
				9V≤V_{IN}≤20V		55	125	mV
Load Regulation		ΔV_O	T_j=25°C	1mA≤I_{OUT}≤100mA		13	80	mV
				1mA≤I_{OUT}≤40mA		6.0	40	mV
Output Voltage		V_O	8.5V≤V_{IN}≤20V	1mA≤I_{OUT}≤40mA	5.90		6.5	V
			8.5V≤V_{IN}≤V_{max} (Note 2)	1mA≤I_{OUT}≤70mA	5.90		6.5	V
Quiescent Current		I_d	T_j=25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI_d	8V≤V_{IN}≤20V				1.5	mA
	with load	ΔI_d	1mA≤I_{OUT}≤40mA				0.1	mA
Output Noise Voltage		V_N	T_a=25°C, 10Hz≤f≤100KHz			50		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT}=5mA			−0.75		mV/°C
Ripple Rejection		RR	f=120Hz, 10V≤V_{IN}≤20V, Tj=25°C		40	46		dB
Dropout Voltage		V_D	T_j=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j=25°C			140		mA

MC78L08AC ELECTRICAL CHARACTERISTICS

V_{IN} =14V, I_{OUT} =40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j=25°C		7.7	8.0	8.3	V
Line Regulation		ΔV_O	T_j=25°C	10.5 ≤ V_{IN} ≤ 23V		80	17.5	mV
				11V ≤ V_{IN} ≤ 23V		70	125	mV
Load Regulation		ΔV_O	T_j=25°C	1mA ≤ I_{OUT} ≤ 100mA		15	80	mV
				1mA ≤ I_{OUT} ≤ 40mA		8.0	40	mV
Output Voltage		V_O	10.5V ≤ V_{IN} ≤ 23V	1mA ≤ I_{OUT} ≤ 40mA	7.6		8.4	V
			10.5V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	7.6		8.4	V
Quiescent Current		I_d	T_j=25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI_d	11V ≤ V_{IN} ≤ 23V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a=25°C, 10Hz ≤ f ≤ 100KHz			60		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} =5mA			−0.8		mV/°C
Ripple Rejection		RR	f=120Hz, 11V ≤ V_{IN} ≤ 21V, T_j = 25°C		39	45		dB
Dropout Voltage		V_D	Tj=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	Tj=25°C			140		mA

MC78L82AC ELECTRICAL CHARACTERISTICS

V_{IN} =14V, I_{OUT} =40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j=25°C		7.87	8.2	8.53	V
Line Regulation		ΔV_O	T_j=25°C	11V ≤ V_{IN} ≤ 23V		80	175	mV
				12V ≤ V_{IN} ≤ 23V		70	125	mV
Load Regulation		ΔV_O	T_j=25°C	1mA ≤ I_{OUT} ≤ 100mA		15	80	mV
				1mA ≤ I_{OUT} ≤ 40mA		8.0	40	mV
Output Voltage		V_O	11V ≤ V_{IN} ≤ 23V	1mA ≤ I_{OUT} ≤ 40mA	7.8		8.6	V
			11V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	7.8		8.6	V
Quiescent Current		I_d	T_j=25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI_d	12V ≤ V_{IN} ≤ 23V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a=25°C, 10Hz ≤ f ≤ 100KHz			60		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			−0.8		mV/°C
Ripple Rejection		RR	f=120Hz, 12V ≤ V_{IN} ≤ 22V, Tj=25°C		39	45		dB
Dropout Voltage		V_D	T_j=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j=25°C			140		mA

MC78L09AC ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, I_{OUT} = 40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, unless otherwise specified. (Note 1)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_j = 25°C		8.64	9.0	9.36	V
Line Regulation	ΔV_O	T_j = 25°C	11.5V ≤ V_{IN} ≤ 24V		90	200	mV
			13V ≤ V_{IN} ≤ 24V		100	150	mV
Load Regulation	ΔV_O	T_j = 25°C	1mA ≤ I_{OUT} ≤ 100mA		20	90	mV
			1mA ≤ I_{OUT} ≤ 40mA		10	45	mV
Output Voltage	V_O	11.5V ≤ V_{IN} ≤ 24V	1mA ≤ I_{OUT} ≤ 40mA	8.55		9.45	V
		11.5V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	8.55		9.45	V
Quiescent Current	I_d	T_j = 25°C			2.1	6.0	mA
Quiescent Current Change with line	ΔI_d	13V ≤ V_{IN} ≤ 24V				1.5	mA
Quiescent Current Change with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage	V_N	T_a = 25°C, 10Hz ≤ f ≤ 100KHz			70		μV
Temperature Coefficient of V_{OUT}	$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			−0.9		mV/°C
Ripple Rejection	RR	f = 120Hz, 12V ≤ V_{IN} ≤ 22V, T_j = 25°C		38	44		dB
Dropout Voltage	V_D	T_j = 25°C			1.7		V
Peak Output/Short-Circuit Current	I_{SC}	T_j = 25°C			140		mA

MC78L12AC ELECTRICAL CHARACTERISTICS

V_{IN} = 19V, I_{OUT} = 40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, unless otherwise specified. (Note 1)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_j = 25°C		11.5	12	12.5	V
Line Regulation	ΔV_O	T_j = 25°C	14.5V ≤ V_{IN} ≤ 27V		120	250	mV
			16V ≤ V_{IN} ≤ 27V		100	200	mV
Load Regulation	ΔV_O	T_j = 25°C	1mA ≤ I_{OUT} ≤ 100mA		20	100	mV
			1mA ≤ I_{OUT} ≤ 40mA		10	50	mV
Output Voltage	V_O	14.5V ≤ V_{IN} ≤ 27V	1mA ≤ I_{OUT} ≤ 40mA	11.4		12.6	V
		14.5V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	11.4		12.6	V
Quiescent Current	I_d	T_j = 25°C			2.1	6.0	mA
Quiescent Current Change with line	ΔI_d	16V ≤ V_{IN} ≤ 27V				1.5	mA
Quiescent Current Change with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage	V_N	T_a = 25°C, 10Hz ≤ f ≤ 100KHz			80		μV
Temperature Coefficient of V_{OUT}	$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			−1.0		mV/°C
Ripple Rejection	RR	f = 120Hz, 15V ≤ V_{IN} ≤ 25V, Tj = 25°C		37	42		dB
Dropout Voltage	V_D	T_j = 25°C			1.7		V
Peak Output/Short-Circuit Current	I_{SC}	T_j = 25°C			140		mA

MC78L15AC ELECTRICAL CHARACTERISTICS

V_{IN} =23V, I_{OUT} =40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j=25°C		14.4	15	15.6	V
Line Regulation		ΔV_O	T_j=25°C	17.5V ≤ V_{IN} ≤ 30V		130	300	mV
				20V ≤ V_{IN} ≤ 30V		110	250	nV
Load Regulation		ΔV_O	T_j=25°C	1mA ≤ I_{OUT} ≤ 100mA		25	150	mV
				1mA ≤ I_{OUT} ≤ 40mA		12	75	mV
Output Voltage		V_O	17.5V ≤ V_{IN} ≤ 30V	1mA ≤ I_{OUT} ≤ 40mA	14.25		15.75	V
			17.5V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	14.25		15.75	V
Quiescent Current		I_d	T_j=25°C			2.2	6.0	mA
Quiescent Current Change	with line	ΔI_d	20V ≤ V_{IN} ≤ 30V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a=25°C, 10Hz ≤ f ≤ 100KHz			90		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			−1.3		mV/°C
Ripple Rejection		RR	f=120Hz, 18.5V ≤ V_{IN} ≤ 28.5V, Tj=25°C		34	39		dB
Dropout Voltage		V_D	T_j=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j=25°C			140		mA

MC78L18AC ELECTRICAL CHARACTERISTICS

V_{IN} =27V, I_{OUT} =40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j=25°C		17.3	18	18.7	V
Line Regulation		ΔV_O	T_j=25°C	21V ≤ V_{IN} ≤ 33V		145	300	mV
				22V ≤ V_{IN} ≤ 33V		135	250	mV
Load Regulation		ΔV_O	T_j=25°C	1mA ≤ I_{OUT} ≤ 100mA		30	170	mV
				1mA ≤ I_{OUT} ≤ 40mA		15	85	mV
Output Voltage		V_O	21V ≤ V_{IN} ≤ 33V	1mA ≤ I_{OUT} ≤ 40mA	17.1		18.9	V
			21V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	17.1		18.9	V
Quiescent Current		I_d	T_j=25°C			2.2	6.0	mA
Quiescent Current Change	with line	ΔI_d	21V ≤ V_{IN} ≤ 33V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a=25°C, 10Hz ≤ f ≤ 100KHz			150		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			−1.8		mV/°C
Ripple Rejection		RR	f=120Hz, 23V ≤ V_{IN} ≤ 33V, Tj=25°C		34	48		dB
Dropout Voltage		V_D	T_j=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j=25°C			140		mA

MC78L24AC ELECTRICAL CHARACTERISTICS

V_{IN} = 33V, I_{OUT} = 40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j = 25°C		23	24	25	V
Line Regulation		ΔV_O	T_j = 25°C	27V ≤ V_{IN} ≤ 38V		160	300	mV
				28V ≤ V_{IN} ≤ 38V		150	250	mV
Load Regulation		ΔV_O	T_j = 25°C	1mA ≤ I_{OUT} ≤ 100mA		40	200	mV
				1mA ≤ I_{OUT} ≤ 40mA		20	100	mV
Output Voltage		V_O	27V ≤ V_{IN} ≤ 38V	1mA ≤ I_{OUT} ≤ 40mA	22.8		25.2	V
			27V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	22.8		25.2	V
Quiescent Current		I_d	T_j = 25°C			2.2	6.0	mA
Quiescent Current Change	with line	ΔI_d	28V ≤ V_{IN} ≤ 38V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a = 25°C, 10Hz ≤ f ≤ 100KHz			200		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			−2.0		mV/°C
Ripple Rejection		RR	f=120Hz, 28V ≤ V_{IN} ≤ 38V, Tj=25°C		34	45		dB
Dropout Voltage		V_D	T_j = 25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j = 25°C			140		mA

Notes

1. The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The date above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.
2. Power dissipation ≤ 0.75W.

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 QUIESCENT CURRENT vs A FUNCTION OF INPUT VOLTAGE

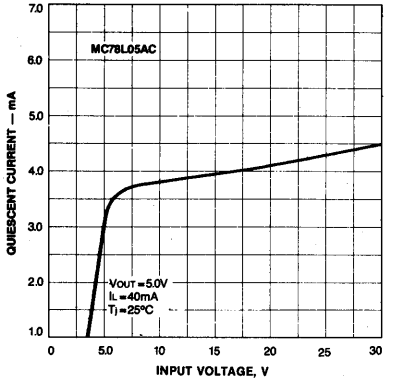


Fig. 2 DROPOUT VOLTAGE vs A FUNCTION O FJUNCTION TEMPERATURE

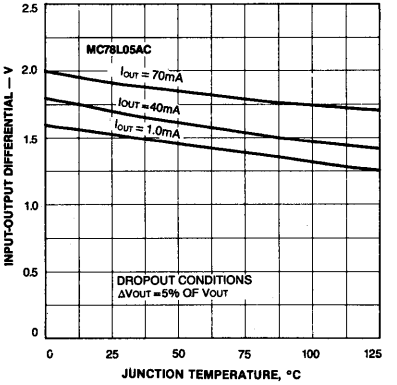


Fig. 3 QUIESCENT CURRENT vs A FUNCTION OF TEMPERATURE

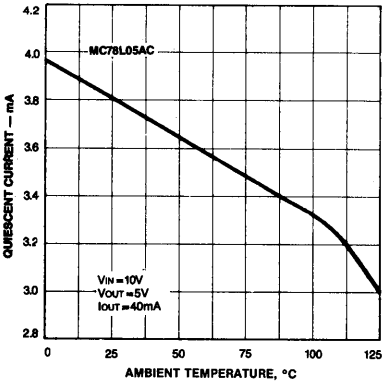


Fig. 4 DROPOUT CHARACTERISTICS

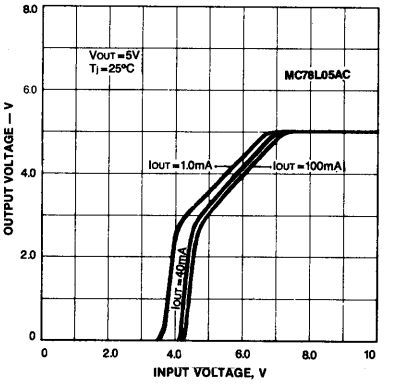


Fig. 5 RIPPLE REJECTION vs A FUNCTION OF FREQUENCY

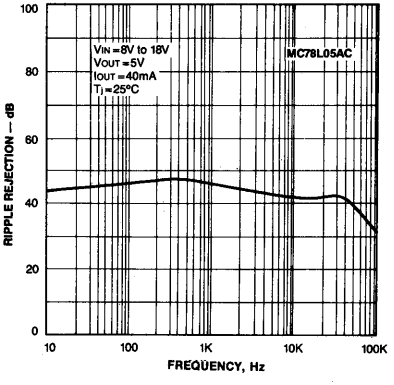


Fig. 6 LINE TRANSIENT RESPONSE

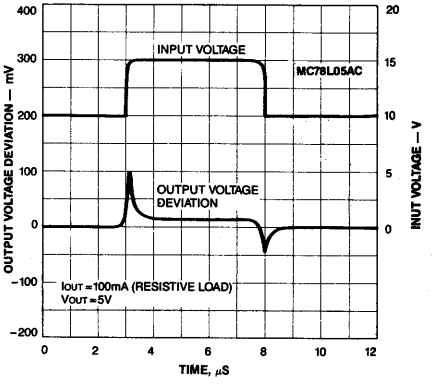


Fig. 7 LOAD TRANSIENT RESPONSE

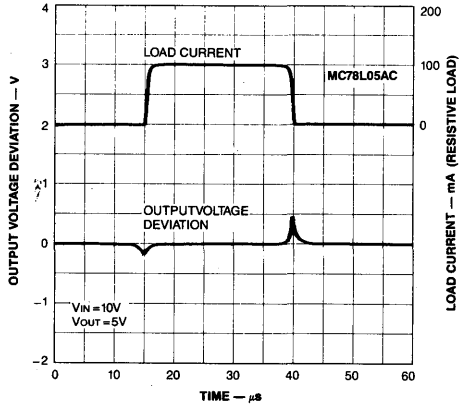
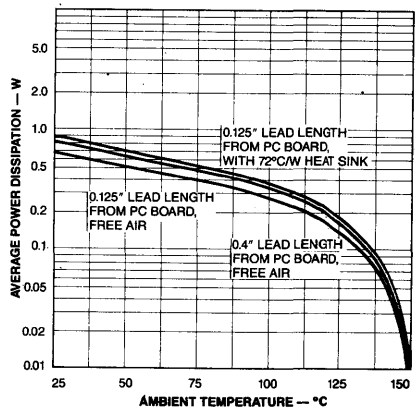


Fig. 8 TO-92 WORST CASE POWER DISSIPATION vs AMBIENT TEMPERATURE



4

APPLICATION INFORMATION

The MC78LXXAC series regulators have thermal overload protection from excessive power, internal short-circuit protection which limits each circuit's maximum current, and output transistor safe-area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (125°C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Thermal Considerations

The TO-92 molded package manufactured by SST is capable of unusually high power dissipation due to the lead frame design. However, its thermal capabilities are generally overlooked because of a lack of understanding of the thermal paths from the semiconductor junction to ambient temperature. While thermal resistance is normally specified for the device mounted 1cm above an infinite heat sink, very little has been mentioned of the options available to improve on the conservatively rated thermal capability.

An explanation of the thermal paths of the TO-92 will allow the designer to determine the thermal stress he is applying in any given application.

The TO-92 Package

The TO-92 package thermal paths are complex. In addition to the path through the molding compound to ambient temperature, there is another path through the pins, in parallel with the case path, to ambient temperature, as shown in Figure 9.

The total thermal resistance in this model is then:

$$\theta_{JA} = \frac{(\theta_{JC} + \theta_{CA})(\theta_{JL} + \theta_{LA})}{\theta_{JC} + \theta_{CA} + \theta_{JL} + \theta_{LA}}$$

Where: θ_{JC} = thermal resistance of the case between the regulator die and a point on the case directly above the die location.

θ_{CA} = thermal resistance between the case and air at ambient temperature.

θ_{JL} = thermal resistance from transistor die through the collector lead to a point 1/16 inch below the regulator case.

θ_{LA} = total thermal resistance of the collector-base-emitter pins to ambient temperature.

θ_{JA} = junction to ambient thermal resistance.

TO-92 Thermal Equivalent Circuit

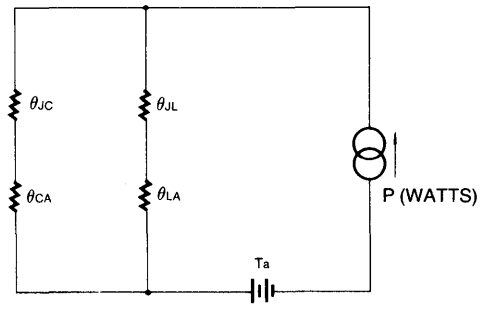


Fig. 9

TO-92 Thermal Equivalent Circuit (PIN at Other Than Ambient Temperature)

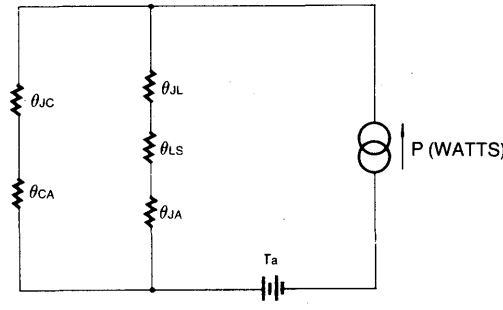


Fig. 10

Methods of Heat Sinking

With two external thermal resistances in each leg of a parallel network available to the circuit designer as variables, he can choose the method of heat sinking most applicable to his particular situation. To demonstrate, consider the effect of placing a small 72°C/W flag type heat sink, such as the Staver F1-7D-2, on the 78LXX molded case. The heat sink effectively replaces the θ_{CA} (Figure 10) and the new thermal resistance, $\theta_{JA} = 145°C/W$ (assuming, 0.125 inch led length).

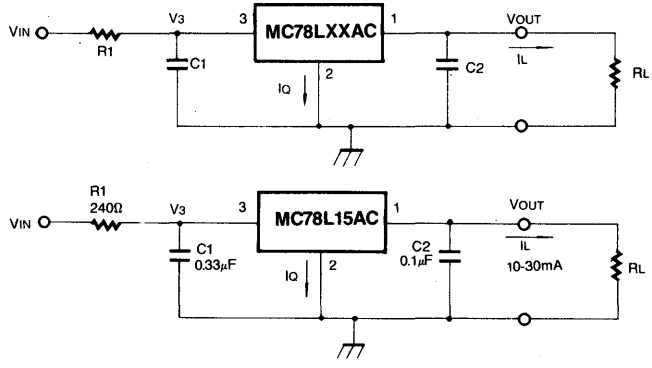
The net change of 15°C/W increases the allowable power dissipation to 0.86W with an inserted cost of 1-2 cents. A still further decrease in θ_{JA} could be achieved by using a heat sink rated at 46°C/W, such as the Staver FS-7A. Also, if the case sinking does not provide an adequate reduction in total θ_{JA}, the other external thermal resistance, θ_{LA}, may be reduced by shortening the lead length from package base to mounting medium. However, one point must be kept in mind. The lead thermal path includes a thermal resistance, θ_{SA}, from the pins at the mounting points to ambient, that is, the mounting medium, θ_{LA} is then equal to $\theta_{LS} + \theta_{SA}$. The new model is shown in Figure 10.

In the case of a socket, θ_{SA} could be as high as 270°C/W, thus causing a net increase in θ_{JA} and a consequent decrease in the maximum dissipation capability. Shortening the lead length may return the net θ_{JA} to the original value, but pin sinking would not be accomplished.

In those cases where the regulator is inserted into a copper clad printed circuit board, it is advantageous to have a maximum area of copper at the entry points of the pins. While it would be desirable to rigorously define the effect of PC board copper, the real world variables are too great to allow anything more than a few general observations.

The best analogy for PC board copper is to compare it with parallel resistors. Beyond some point, additional resistors are not significantly effective; beyond some point, additional copper area is not effective.

High Dissipation Applications



When it is necessary to operate a MC78LXXAC regulator with a large input-output differential voltage, the addition of series resistor R1 will extend the output current range of the device by sharing the total power dissipation between R1 and the regulator.

$$R1 = \frac{V_{IN\,(MIN)} - V_{OUT} - 2.0V}{I_{L\,(MAX)} + I_Q}$$

Where I_o is the regulator quiescent current.

Regulator power dissipation at maximum input voltage and maximum load current is now

$$P_{D\,(MAX)} = (V_3 - V_{OUT})\, I_{L\,(MAX)} + V_3 I_Q$$

where $V_3 = V_{IN\,(MAX)} - (I_{C\,(MAX)} + I_Q)\, R_1$

The presence of R1 will affect load regulation according to the equation:
load regulation (at constant V_{IN})
=load regulation (at constant V_3)
+(line regulation, mV per V)
×(R1)×(ΔIL).

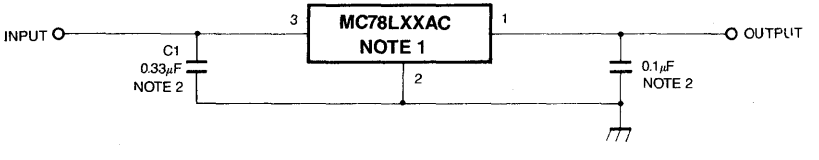
As an example, consider a 15V regulator with a supply voltage of 30±5V, required to supply a maximum load current of 30mA. I_Q is 4.3mA, and minimum load current is to be 10mA.

$$R_1 = \frac{25 - 15 - 2}{30 + 4.3} = \frac{34.3}{8} = 240\Omega$$

$V_3 = 35 - (30 + 4.3) \times 0.24 = 35.82 = 26.8V$
$P_{D\,(MAX)} = (26.8 - 15)\, 30 + 26.8\, (4.3)$
$= 354 + 115$
=470mW, which permit operation up to 70°C
in most applications.

Line regulation of this circuit is typically 110mV for an input range of 25 ~ 35V at a constant load current; i.e. 11mV/V
Load regulation=constant V_1 load regulation (typically 10mV, 10 ~ 30mA I_L)
+(11mV/V×0.24×20mA (typically 53mV)
=63mV for a load current change of 20mA at a constant V_{IN} of 30V.

Typical Application



Notes

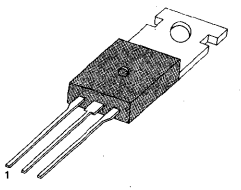
1. To specify an output voltage, substitute voltage value for "xx".
2. Bypass Capacitors are recommended for optimum stability and transient response and should be locate as close as possible to the regulator.

3-TERMINAL 0.5A POSITIVE VOLTAGE REGULATOR

The MC78MXXC series of three-terminal positive regulators are available TO-220 package with several fixed output voltages, making it useful in a wide range of applications. These reglators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 0.5A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

MC78MXXC is characterized for operation from 0°C to 125°C, and MC78MXXI from −40°C to 125°C.

TO-220



1: Input 2: GND 3: Output

FEATURES

- **Output Current up to 0.5A**
- **Output Voltages of 5; 6; 8; 10; 12; 15; 18; 20; 24V**
- **Thermal Overload Protection**
- **Short Circuit Protection**
- **Output Transistor SOA Protection**
- **Industrial and commercial temperature range**

ORDERING INFORMATION

Device	Package	Operating Temperature
**MC78MXXIT	TO-220	−40 ~ +125°C
MC78MXXCT	TO-220	0 ~ +125°C

** Under Development

BLOCK DIAGRAM

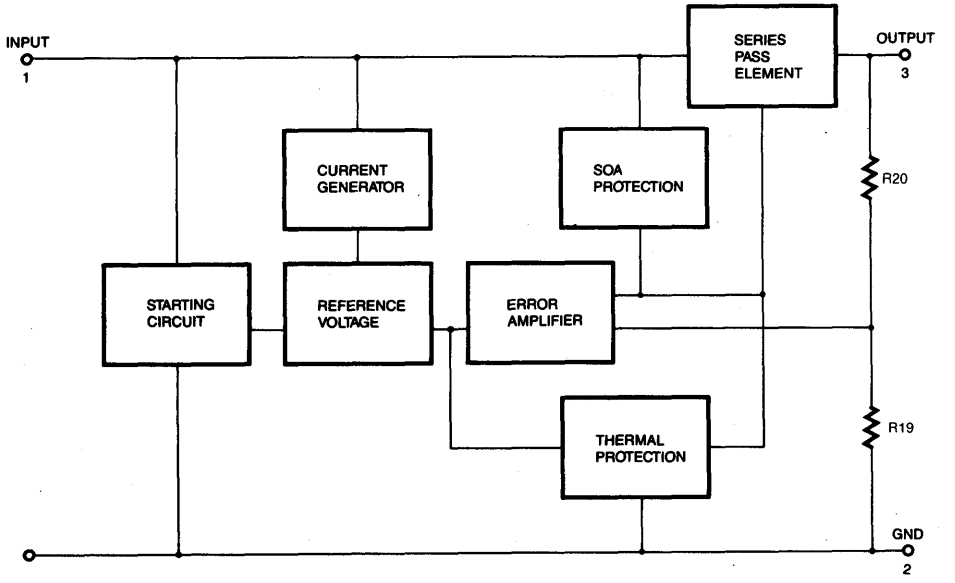


Fig. 1

SCHEMATIC DIAGRAM

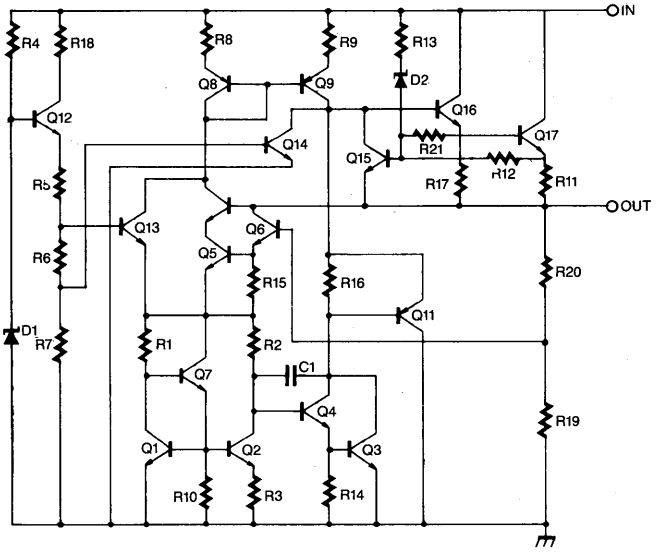


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_i V_i	35 40	V V
Thermal Resistance Junction-Cases	θ_{JC}	5	°C/W
Thermal Resistance Junction-Air	θ_{JA}	65	°C/W
Operating Temperature Range MC78XXI MC78XXC/AC	T_{opr}	−40 ~ +125 0 ~ +125	°C °C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS MC78M05C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 10V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		4.8	5	5.2	V
		$I_o = 5$ to $350mA$ $V_i = 7$ to $20V$		4.75	5	5.25	
Line Regulation	$\triangle V_o$	$I_o = 200mA$ $T_j = 25°C$	$V_i = 7$ to $25V$			100	mV
			$V_i = 8$ to $25V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$, $T_j = 25°C$				100	mV
		$I_o = 5mA$ to $200mA$, $T_j = 25°C$				50	
Quiescent Current	I_d	$T_j = 25°C$			4.0	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$				0.5	mA
		$I_o = 200mA$ $V_i = 8$ to $25V$				0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$			-0.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$			40		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$ $V_i = 8$ to $18V$		62			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$			2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$			300		mA
Peak Current	I_{peak}	$T_j = 25°C$			700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

ELECTRICAL CHARACTERISTICS MC78M06C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 11V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		5.75	6	6.25	V
		$I_o = 5$ to $350mA$ $V_i = 8$ to $21V$		5.7	6	6.3	
Line Regulation	$\triangle V_o$	$I_o = 200mA$ $T_j = 25°C$	$V_i = 8$ to $25V$			100	mV
			$V_i = 9$ to $25V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$, $T_j = 25°C$				120	mV
		$I_o = 5mA$ to $200mA$, $T_j = 25°C$				60	
Quiescent Current	I_d	$T_j = 25°C$			4.0	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$				0.5	mA
		$I_o = 200mA$ $V_i = 9$ to $25V$				0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$			-0.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$			45		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$ $V_i = 9$ to $19V$		59			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$			2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$			300		mA
Peak Current	I_{peak}	$T_j = 25°C$			700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

4

ELECTRICAL CHARACTERISTICS MC78M08C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 14V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	7.7	8	8.3	V
		$I_o = 5$ to $350mA$ $V_i = 10.5$ to $23V$	7.6	8	8.4	
Line Regulation	$\triangle V_o$	$I_o = 200mA$, $T_j = 25°C$, $V_i = 10.5$ to $25V$			100	mV
		$I_o = 200mA$, $T_j = 25°C$, $V_i = 11$ to $25V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$, $T_j = 25°C$			160	mV
		$I_o = 5mA$ to $200mA$, $T_j = 25°C$			80	
Quiescent Current	I_d	$T_j = 25°C$		4.0	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$			0.5	mA
		$I_o = 200mA$ $V_i = 10.5$ to $25V$			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$		−0.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$		52		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$ $V_i = 11.5$ to $21.5V$	56			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$		300		mA
Peak Current	I_{peak}	$T_j = 25°C$		700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

ELECTRICAL CHARACTERISTICS MC78M10C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 17V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		9.6	10	10.4	V
		$I_o = 5$ to $350mA$ $V_i = 12.5$ to $25V$		9.5	10	10.5	
Line Regulation	$\triangle V_o$	$I_o = 200mA$ $T_j = 25°C$	$V_i = 12.5$ to $25V$			100	mV
			$V_i = 13$ to $25V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$, $T_j = 25°C$				200	mV
		$I_o = 5mA$ to $200mA$, $T_j = 25°C$				100	
Quiescent Current	I_d	$T_j = 25°C$			4.1	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$				0.5	mA
		$I_o = 200mA$ $V_i = 12.5$ to $25V$				0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$			-0.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$			65		μV
Ripple Rejection	RR	$f = 120Hz$, $I_o = 300mA$ $V_i = 13$ to $23V$		55			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$			2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$			300		mA
Peak Current	I_{peak}	$T_j = 25°C$			700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

ELECTRICAL CHARACTERISTICS MC78M12C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 19V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		11.5	12	12.5	V
		$I_o = 5$ to $350mA$ $V_i = 14.5$ to $27V$		11.4	12	12.6	
Line Regulation	$\triangle V_o$	$I_o = 200mA$ $T_j = 25°C$	$V_i = 14.5$ to $30V$			100	mV
			$V_i = 16$ to $30V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$, $T_j = 25°C$				240	mV
		$I_o = 5mA$ to $200mA$, $T_j = 25°C$				120	
Quiescent Current	I_d	$T_j = 25°C$			4.1	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$				0.5	mA
		$I_o = 200mA$ $V_i = 14.5$ to $30V$				0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$			−0.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$			75		μV
Ripple Rejection	RR	$f = 120Hz$, $I_o = 300mA$ $V_i = 15$ to $25V$		55			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$			2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$			300		mA
Peak Current	I_{peak}	$T_j = 25°C$			700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

ELECTRICAL CHARACTERISTICS MC78M15C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 23V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	14.4	15	15.6	V
		$I_o = 5$ to $350mA$, $V_i = 17.5$ to $30V$	14.25	15	15.75	
Line Regulation	$\triangle V_o$	$I_o = 200mA$, $T_j = 25°C$, $V_i = 17.5$ to $30V$			100	mV
		$I_o = 200mA$, $T_j = 25°C$, $V_i = 20$ to $30V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$, $T_j = 25°C$			300	mV
		$I_o = 5mA$ to $200mA$, $T_j = 25°C$			150	
Quiescent Current	I_d	$T_j = 25°C$		4.1	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$			0.5	mA
		$I_o = 200mA$, $V_i = 17.5$ to $30V$			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$, $T_j = 0$ to $125°C$		−1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$		90		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$, $V_i = 18.5$ to $28.5V$	54			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$		300		mA
Peak Current	I_{peak}	$T_j = 25°C$		700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

4

ELECTRICAL CHARACTERISTICS MC78M18C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 26V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		17.3	18	18.7	V
		$I_o = 5$ to $350mA$ $V_i = 20.5$ to $33V$		17.1	18	18.9	
Line Regulation	$\triangle V_o$	$I_o = 200mA$ $T_j = 25°C$	$V_i = 21$ to $33V$			100	mV
			$V_i = 24$ to $33V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$, $T_j = 25°C$				360	mV
		$I_o = 5mA$ to $200mA$, $T_j = 25°C$				180	
Quiescent Current	I_d	$T_j = 25°C$			4.2	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$				0.5	mA
		$I_o = 200mA$ $V_i = 21$ to $33V$				0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$			-1.1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$			100		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$ $V_i = 22$ to $32V$		53			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$			2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$			300		mA
Peak Current	I_{peak}	$T_j = 25°C$			700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

ELECTRICAL CHARACTERISTICS MC78M20C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 29V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	19.2	20	20.8	V
		$I_o = 5$ to $350mA$ $V_i = 23$ to $35V$	19	20	21	
Line Regulation	$\triangle V_o$	$I_o = 200mA$, $T_j = 25°C$, $V_i = 23$ to $35V$			100	mV
		$I_o = 200mA$, $T_j = 25°C$, $V_i = 24$ to $35V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$, $T_j = 25°C$			400	mV
		$I_o = 5mA$ to $200mA$, $T_j = 25°C$			200	
Quiescent Current	I_d	$T_j = 25°C$		4.2	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$			0.5	mA
		$I_o = 200mA$ $V_i = 23$ to $35V$			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$		-1.1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$		110		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$ $V_i = 24$ to $34V$	53			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$		300		mA
Peak Current	I_{peak}	$T_j = 25°C$		700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

4

ELECTRICAL CHARACTERISTICS MC78M24C

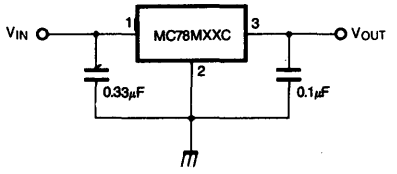
(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 33V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$	23	24	25	V
		$I_o = 5$ to $350mA$ $V_i = 27$ to $38V$	22.8	24	25.2	
Line Regulation	ΔV_o	$I_o = 200mA$, $T_j = 25°C$, $V_i = 27$ to $38V$			100	mV
		$I_o = 200mA$, $T_j = 25°C$, $V_i = 28$ to $38V$			50	
Load Regulation	ΔV_o	$I_o = 5mA$ to $0.5A$, $T_j = 25°C$			480	mV
		$I_o = 5mA$ to $200mA$, $T_j = 25°C$			240	
Quiescent Current	I_d	$T_j = 25°C$		4.2	6	mA
Quiescent Current Change	ΔI_d	$I_o = 5mA$ to $350mA$			0.5	mA
		$I_o = 200mA$ $V_i = 27$ to $38V$			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$		−1.2		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$		170		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$ $V_i = 28$ to $38V$	50			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$		2		V
Short Circuit Current	I_{sc}	$V_i = 35V$		300		mA
Peak Current	I_{peak}	$T_j = 25°C$		700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

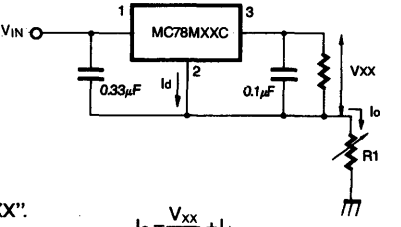
APPLICATION CIRCUIT

Fig. 1 Fixed output regulator



Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Fig. 2 Constant current regulator



$$I_O = \frac{V_{XX}}{R_1} + I_d$$

Fig. 3 Circuit for increasing output voltage

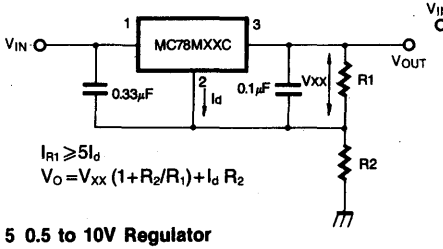


Fig. 4 Adjustable output regulator (7 to 30V)

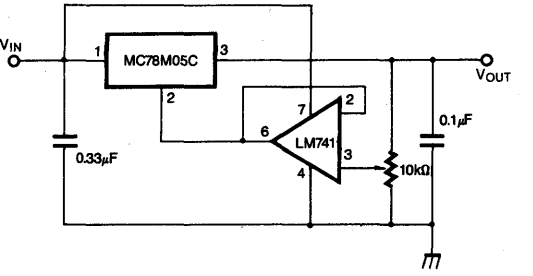
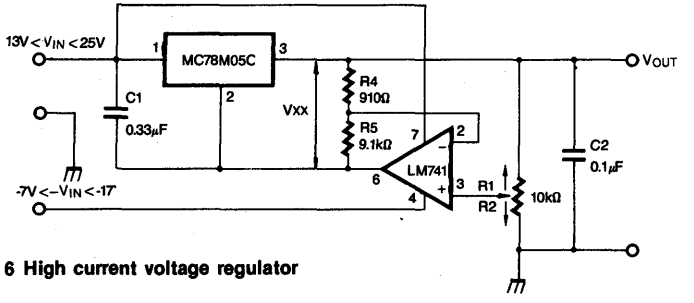
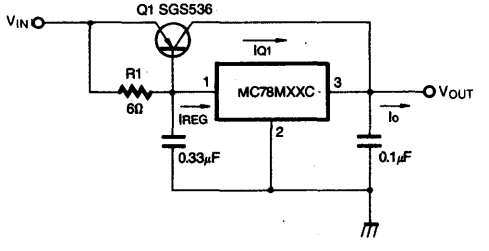


Fig. 5 0.5 to 10V Regulator



$$V_O = V_{XX}\frac{R_4}{R_1}$$

Fig. 6 High current voltage regulator

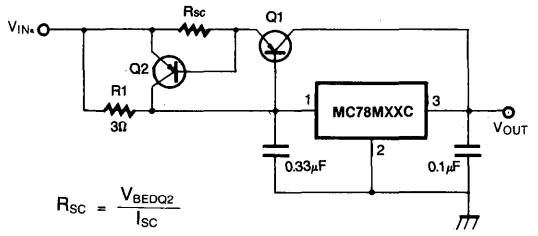


$$R_1 = \frac{V_{BEQ1}}{I_{REG} - \frac{I_{Q1}}{\beta_{Q1}}}$$

$$I_O = I_{REG} + \beta_{Q1}\left(I_{REG} - \frac{V_{BEQ1}}{R_{R1}}\right)$$

APPLICATION CIRCUIT (continued)

Fig. 7 High output current with short circuit protection



$$R_{SC} = \frac{V_{BEDQ2}}{I_{SC}}$$

Fig. 8 Tracking voltage regulator

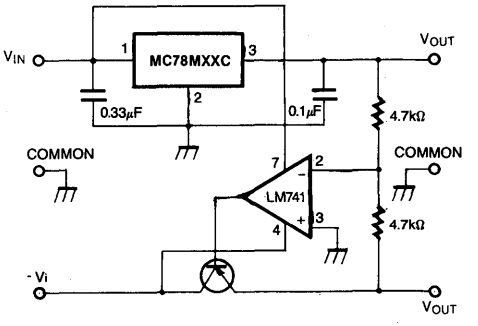
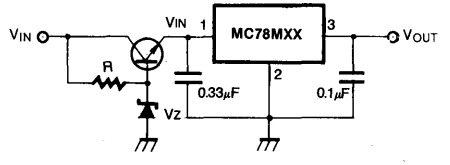
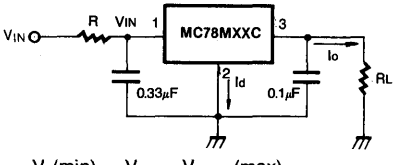


Fig. 9 High input voltage circuit



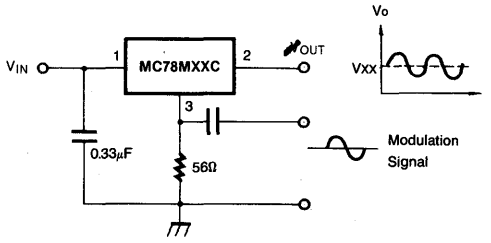
$$V_{IN} = V_Z - V_{BE}$$

Fig. 10 Reducing power dissipation with dropping resistor



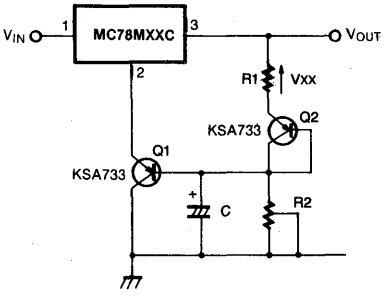
$$R = \frac{V_i\,(min) - V_{XX} - V_{DROP}\,(max)}{I_O\,(max) + I_d\,(max)}$$

Fig. 11
(unity voltage gain, $I_O \leq 0.5$)



Note: The circuit performs well up to 100 KHz.

Fig. 12 Adjustable output voltage with temperature compensation



Note: Q2 is connected as a diode in order to compensate the variation of the Q1 V_{BE} with the temperature. C allows a slow rise-time of the V_O

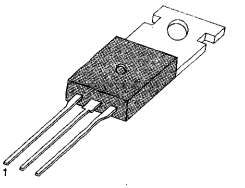
$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

3-TERMINAL NEGATIVE VOLTAGE REGULATOR

The MC79XXC series of three-terminal negative regulators are available in TO-220 package and with several output voltages. They canprovides local on-card regulation, eliminating the distribution problems associated with single point regulation; furthermore, having the same voltage options as the MC78XXC positive standard series, they are particularly suited for split power supplies.

If adequate heat sinking is provided, the MC79XXC series can deliver an output current in excess of 1.5A. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

TO-220



1: GND 2: Input 3: Output

FEATURES

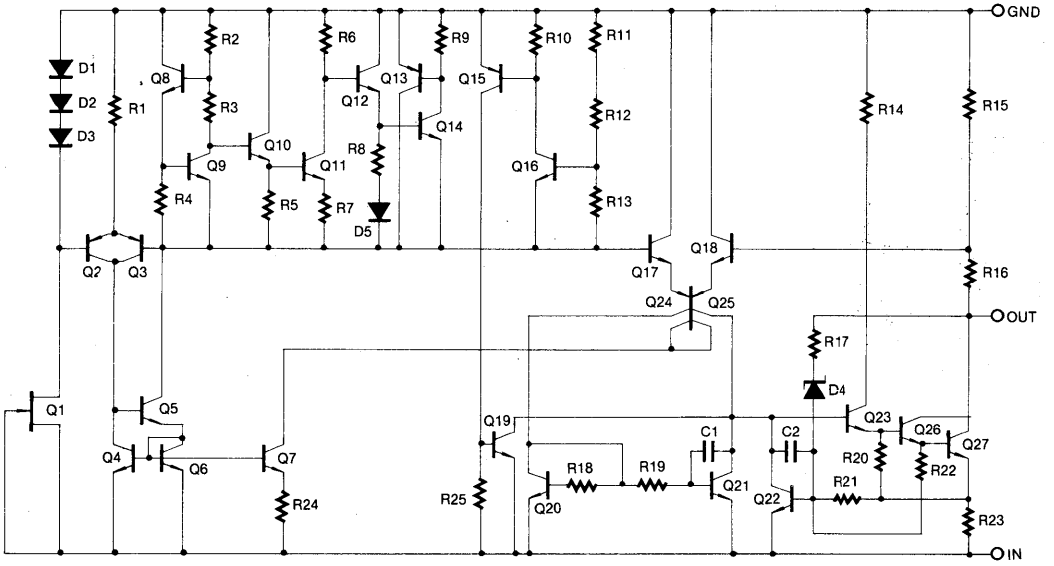
- **Output current in excess of 1A**
- **Output voltages of −2V, −5V, −6V, −8V, −12V, −15V, −18V, −24V**
- **Internal thermal overload protection**
- **Short circuit protection**
- **Output transistor safe-area compensation**

ORDERING INFORMATION

Device	Package	Operation Temperature
MC79XXCT	TO-220	0 ~ 125°C
**MC79XXIT	TO-220	− 40 ~ 125°C

** Under development

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (for V_o = −2 to −18V) (for V_o = −24V)	V_{IN}	−35 −40	V V
Thermal Resistance Junction-Case Junction-Air	θ_{JC} θ_{JA}	5 65	°C/W °C/W
Operating Temperature Range	T_{opr}	0 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS MC7902C

(C_i = 2.2μF, C_o = 1μF, T_j = 0 to 125°C, I_o = 500mA, V_i = 10V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	−1.92	−2	−2.08	V
		I_o=5mA to 1A $P_D \leq$ 15W V_i = −7 to −20V	−1.9	−2	−2.1	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i = −7 to −25V		10	40	mV
		T_j=25°C, V_i = −8 to −12V		5	20	
Load Regulation	$\triangle V_o$	T_j=25°C I_o=5mA to 1.5A		10	120	mV
		T_j=25°C I_o=250 to 750mA		3	60	
Quiescent Current	I_d	T_j=25°C		3	6	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i = −7 to −25V			1.3	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		−0.4		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_j=25°C		40		μV
Ripple Rejection	RR	f=120Hz $\triangle V_i$=10V	54	60		dB
Dropout Voltage	V_D	T_j=25°C I_o=1A		3.5		V
Short Circuit Current	I_{sc}	T_j=25°C, V_i = −35V		300		mA
Peak Current	I_{peak}	T_j=25°C		2.2		A

ELECTRICAL CHARACTERISTICS MC7905C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 10V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−4.8	−5	−5.2	V
		$I_o = 5mA$ to $1A$, $P_o \leq 15W$ $V_i = -8$ to $-20V$	−4.75	−5	−5.25	
Line Regulation	ΔV_o	$T_j = 25°C$, $V_i = -7$ to $-25V$		10	100	mV
		$T_j = 25°C$, $V_i = -8$ to $-12V$		5	50	
Load Regulation	ΔV_o	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$		10	100	mV
		$T_j = 25°C$ $I_o = 250$ to $750mA$		3	50	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	ΔI_d	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -8$ to $-25V$			1.3	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	$I_o = 5mA$		−0.4		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		100		μV
Ripple Rejection	RR	$f = 120Hz$ $\Delta V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = -35V$		300		mA
Peak Current	I_{peak}	$T_j = 25°C$		2.2		A

ELECTRICAL CHARACTERISTICS MC7906C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 11V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−5.75	−6	−6.25	V
		$I_o = 5mA$ to $1A$, $P_o \leq 15W$ $V_i = -9$ to $-21V$	−5.7	−6	−6.3	
Line Regulation	$\triangle V_o$	$T_j = 25°C$, $V_i = -8$ to $-25V$		10	120	mV
		$T_j = 25°C$, $V_i = -9$ to $-13V$		5	60	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$		10	120	mV
		$T_j = 25°C$ $I_o = 250$ to $750mA$		3	60	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -9$ to $-25V$			1.3	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$		−0.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		130		μV
Ripple Rejection	RR	$f = 120Hz$ $\triangle V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = -35V$		300		mA
Peak Current	I_{peak}	$T_j = 25°C$		2.2		A

ELECTRICAL CHARACTERISTICS MC7908C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 14V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−7.7	−8	−8.3	V
		$I_o = 5mA$ to $1A$, $P_o \leq 15W$ $V_i = -11.5$ to $-23V$	−7.6	−8	−8.4	
Line Regulation	$\triangle V_o$	$T_j = 25°C$, $V_i = -10.5$ to $-25V$		10	160	mV
		$T_j = 25°C$, $V_i = -11$ to $-17V$		5	80	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$		12	160	mV
		$T_j = 25°C$ $I_o = 250$ to $750mA$		4	80	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -11.5$ to $-25V$			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$		−0.6		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		175		μV
Ripple Rejection	RR	$f = 120Hz$ $\triangle V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = -35V$		300		mA
Peak Current	I_{peak}	$T_j = 25°C$		2.2		A

ELECTRICAL CHARACTERISTICS MC7912C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 18V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−11.5	−12	−12.5	V
		$I_o = 5mA$ to $1A$, $P_o \leq 15W$ $V_i = -15.5$ to $-27V$	−11.4	−12	−12.6	
Line Regulation	$\triangle V_o$	$T_j = 25°C$, $V_i = -14.5$ to $-30V$		12	240	mV
		$T_j = 25°C$, $V_i = -16$ to $-22V$		6	120	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$		12	240	mV
		$T_j = 25°C$ $I_o = 250$ to $750mA$		4	120	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -15$ to $-30V$			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$		−0.8		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		200		μV
Ripple Rejection	RR	$f = 120Hz$ $\triangle V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = -35V$		300		mA
Peak Current	I_{peak}	$T_j = 25°C$		2.2		A

ELECTRICAL CHARACTERISTICS MC7915C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 23V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−14.4	−15	−15.6	V
		$I_o = 5mA$ to $1A$, $P_o \leq 15W$ $V_i = -18$ to $-30V$	−14.25	−15	−15.75	
Line Regulation	ΔV_o	$T_j = 25°C$, $V_i = -17.5$ to $-30V$		12	300	mV
		$T_j = 25°C$, $V_i = -20$ to $-26V$		6	150	
Load Regulation	ΔV_o	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$		12	300	mV
		$T_j = 25°C$ $I_o = 250$ to $750mA$		4	150	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	ΔI_d	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -18.5$ to $-30V$			1	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	$I_o = 5mA$		−0.9		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		250		μV
Ripple Rejection	RR	$f = 120Hz$ $\Delta V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = -35V$		300		mA
Peak Current	I_{peak}	$T_j = 25°C$		2.2		A

4

ELECTRICAL CHARACTERISTICS MC7918C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 27V$, unless otherwise specified) .

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−17.3	−18	−18.7	V
		$I_o = 5mA$ to $1A$, $P_o \leq 15W$ $V_i = -22.5$ to $-33V$	−17.1	−18	−18.9	
Line Regulation	ΔV_o	$T_j = 25°C$, $V_i = -21$ to $-33V$		15	360	mV
		$T_j = 25°C$, $V_i = -24$ to $-30V$		8	180	
Load Regulation	ΔV_o	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$		15	360	mV
		$T_j = 25°C$ $I_o = 250$ to $750mA$		5	180	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	ΔI_d	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -22$ to $-33V$			1	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	$I_o = 5mA$		−1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		300		μV
Ripple Rejection	RR	$f = 120Hz$ $\Delta V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = -35V$		300		mA
Peak Current	I_{peak}	$T_j = 25°C$		2.2		A

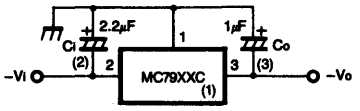
ELECTRICAL CHARACTERISTICS MC7924C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 33V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−23	−24	−25	V
		$I_o = 5mA$ to $1A, P_o \leq 15W$, $V_i = -27$ to $-38V$	−22.8	−24	−25.2	
Line Regulation	$\triangle V_o$	$T_j = 25°C$, $V_i = -27$ to $-38V$		15	480	mV
		$T_j = 25°C$, $V_i = -30$ to $-36V$		8	240	
Load Regulation	$\triangle V_o$	$T_j = 25°C$, $I_o = 5mA$ to $1.5A$		15	480	mV
		$T_j = 25°C$, $I_o = 250$ to $750mA$		5	240	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -27$ to $-38V$			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$		−1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$, $T_j = 25°C$		400		μV
Ripple Rejection	RR	$f = 120Hz$, $\triangle V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = -35V$		300		mA
Peak Current	I_{peak}	$T_j = 25°C$		2.2		A

APPLICATION INFORMATION

Fig. 1 — Fixed output regulator



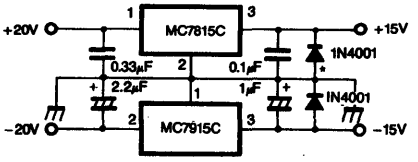
Notes:

(1) To specify an output voltage, substitute voltage value for "XXC".

(2) Required for stability. For value given, capacitor must be solid tantalum. If aluminium electrolitics are used, at least ten times value shown should be selected. Ci is required if regulator is located an appreciable distance from power supply filter.

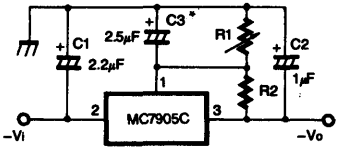
(3) To improve transient response. If large capacitors are used, a high current diode from input to output (1N4001 or similar) should be introduced to protect the device from momentary input short circuit.

Fig. 2 — Split power supply (±15V/1A)



* Against potential latch-up problems.

Fig. 3 — Circuit for increasing output voltage



$$V_o = V_{XX} \cdot \frac{R1 + R2}{R2}$$

$V_{XX}/R2 > 3\ I_d$

* C3 optional for improved transient response and ripple rejection.

Fig. 4 — High current negative regulator (-5V/4A with 5A current limiting)

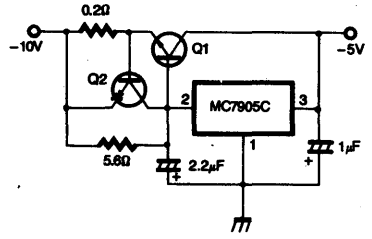
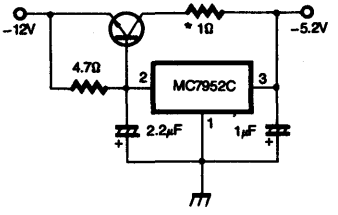


Fig. 5 — Typical ECL system power supply (-5.2V/4A)

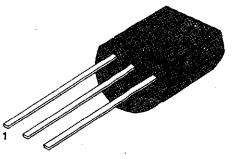


* Optional dropping resistor to reduce the power dissipated in the boost transistor.

3-TERMINAL NEGATIVE VOLTAGE REGULATOR

These regulators employ internal current limiting and thermal—shutdown, making them essentially indestructible. The are intended as fixed voltage regulators in a wide range of application including local regulator for eliminatation of noise and distribution problems associated with single—point regulation.

TO-92



1: GND 2: Input 3: Output

FEATURES

- **Output current up to 100mA**
- **No external components**
- **Internal thermal over load protection**
- **Internal short circuit current limiting**
- **Available in JEDEC TO-92**
- **Mass production: MC79L05**
- **Under development: −12; −15; −18; −24V**

ORDERING INFORMATION

Device	Package	Operation Temperature
S79LXXACZ	TO-92	0 ~ 125°C
** S79LXXAIZ	TO-92	− 40 ~ 125°C

** Under development

SCHEMATIC DIAGRAM

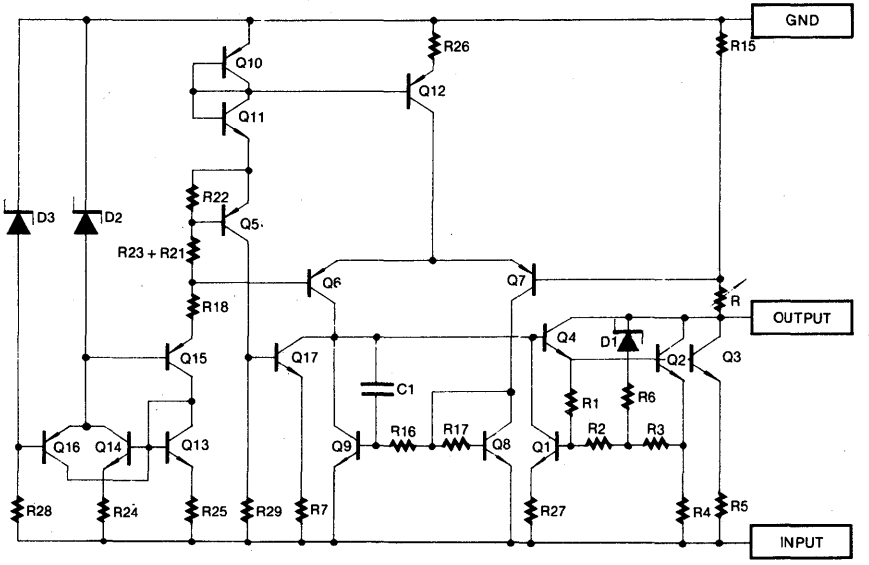


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Input Voltage (−5V) (−12V to −18V) (−24V)	V_I	−30 −35 −40	V_{DC}
Operating Temperature Range	T_{opr}	0 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

MC79L05AC ELECTRICAL CHARACTERISTICS

(V_i = −10V, I_o = 40mA, C_i = 0.33μF, C_o = 0.1μF, 0°C ≤ T_j ≤ +125°C, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_o	T_j = 25°C		−4.8	−5.0	−5.2	V
Line Regulation		$\triangle V_o$	T_j = 25°C	−7.0V ≥ V_i ≥ −20V			150	mV
				−8.0V ≥ V_i ≥ −20V			100	
Load Regulation		$\triangle V_o$	T_j = 25°C	1.0mA ≤ I_o ≤ 100mA			60	mV
				1.0mA ≤ I_o ≤ 40mA			30	
Output Voltage		V_o	−7.0V > V_i > −20V, 1.0mA ≤ I_o ≤ 40mA		−4.75		−5.25	V
			V_i = −1.0V, 1.0mA ≤ I_o ≤ 70mA		−4.75		−5.25	
Quiescent Current		I_d	T_j = +25°C				6.0	mA
			T_j = +125°C				5.5	
Quiescent Current Change	With Line	I_d	−8V ≥ V_i ≥ −20V				1.5	mA
	With Load		1.0mA ≤ I_o ≤ 40mA				0.1	
Output Noise Voltage		V_N	Ta = 25°C, 10Hz ≤ f ≤ 100KHz			40		μV
Ripple Rejection		RR	f = 120Hz, −8.0 ≥ V_i ≥ −18V T_j = 25°C		41	49		dB
Dropout Voltage		V_D	T_j = 25°C			1.7		V

MC79L12AC ELECTRICAL CHARACTERISTICS

($V_i = -19V$, $I_o = 40mA$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, $0°C \leq T_j \leq +125°C$, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_o	$T_j = 25°C$		-11.5	-12.0	-12.5	V
Line Regulation		$\triangle V_o$	$T_j = 25°C$	$-14.5V \geq V_i \geq -27V$			250	mV
				$-16V \geq V_i \geq -27V$			200	
Load Regulation		$\triangle V_o$	$T_j = 25°C$	$1.0mA \leq I_o \leq 100mA$			100	mV
				$1.0mA \leq I_o \leq 40mA$			50	
Output Voltage		V_o	$-14.5V > V_i > -27V$, $1.0mA \leq I_o \leq 40mA$		-11.4		-12.6	V
			$V_i = -19V$, $1.0mA \leq I_o \leq 70mA$		-11.4		-12.6	
Quiescent Current		I_d	$T_j = +25°C$				6.5	mA
			$T_j = +125°C$				6.0	
Quiescent Current Change	With Line	I_d	$-16V \geq V_i \geq -27V$				1.5	mA
	With Load		$1.0mA \leq I_o \leq 40mA$				0.1	
Output Noise Voltage		V_N	$Ta = 25°C$, $10Hz \leq f \leq 100KHz$			80		μV
Ripple Rejection		RR	$f = 120Hz$, $-15V \geq V_i \geq -25V$, $T_j = 25°C$		37	42		dB
Dropout Voltage		V_D	$T_j = 25°C$			1.7		V

MC79L15AC ELECTRICAL CHARACTERISTICS

($V_i = -23V$, $I_o = 40mA$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, $0°C \leq T_j \leq +125°C$, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_o	$T_j = 25°C$		-14.4	-15.0	-15.6	V
Line Regulation		$\triangle V_o$	$T_j = 25°C$	$-17.5V \geq V_i \geq -30V$			300	mV
				$-27V \geq V_i \geq -30V$			250	
Load Regulation		$\triangle V_o$	$T_j = 25°C$	$1.0mA \leq I_o \leq 100mA$			150	mV
				$1.0mA \leq I_o \leq 40mA$			75	
Output Voltage		V_o	$-17.5V > V_i > -30V$, $1.0mA \leq I_o \leq 40mA$		-14.25		-15.75	V
			$V_i = -23V$, $1.0mA \leq I_o \leq 70mA$		-14.25		-15.75	
Quiescent Current		I_d	$T_j = +25°C$				6.5	mA
			$T_j = +125°C$				6.0	
Quiescent Current Change	With Line	I_d	$-20V \geq V_i \geq -30V$				1.5	mA
	With Load		$1.0mA \leq I_o \leq 40mA$				0.1	
Output Noise Voltage		V_N	$Ta = 25°C$, $10Hz \leq f \leq 100KHz$			90		μV
Ripple Rejection		RR	$f = 120Hz$, $-18.5V \geq V_i \geq -28.5V$, $T_j = 25°C$		34	39		dB
Dropout Voltage		V_D	$T_j = 25°C$			1.7		V

MC79L18AC ELECTRICAL CHARACTERISTICS

($V_i = -27V$, $I_o = 40mA$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, $0°C \leq T_j \leq +125°C$, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_o	$T_j = 25°C$		-17.3	-18.0	-18.7	V
Line Regulation		$\triangle V_o$	$T_j = 25°C$	$-20.7V \geq V_i \geq -33V$			325	mV
				$-21V \geq V_i \geq -33V$			275	
Load Regulation		$\triangle V_o$	$T_j = 25°C$	$1.0mA \leq I_o \leq 100mA$			170	mV
				$1.0mA \leq I_o \leq 40mA$			85	
Output Voltage		V_o	$-20.7V > V_i > -33V$, $1.0mA \leq I_o \leq 40mA$		-17.1		-18.9	V
			$V_i = -27V$, $1.0mA \leq I_o \leq 70mA$		-17.1		-18.9	
Quiescent Current		I_d	$T_j = +25°C$				6.5	mA
			$T_j = +125°C$				6.0	
Quiescent Current Change	With Line	I_d	$-21V \geq V_i \geq -33V$				1.5	mA
	With Load		$1.0mA \leq I_o \leq 40mA$				0.1	
Output Noise Voltage		V_N	$Ta = 25°C$, $10Hz \leq f \leq 100KHz$			150		μV
Ripple Rejection		RR	$f = 120Hz$, $-23V \geq V_i \geq -33V$ $T_j = 25°C$		33	48		dB
Dropout Voltage		V_D	$T_j = 25°C$			1.7		V

MC79L24AC ELECTRICAL CHARACTERISTICS

($V_i = -33V$, $I_o = 40mA$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, $0°C \leq T_j \leq +125°C$, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_o	$T_j = 25°C$		-23	-24	-25	V
Line Regulation		$\triangle V_o$	$T_j = 25°C$	$-27V \geq V_i \geq -38V$			350	mV
				$-28V \geq V_i \geq -38V$			300	
Load Regulation		$\triangle V_o$	$T_j = 25°C$	$1.0mA \leq I_o \leq 100mA$			200	mV
				$1.0mA \leq I_o \leq 40mA$			100	
Output Voltage		V_o	$-27V > V_i > -38V$, $1.0mA \leq I_o \leq 40mA$		-22.8		-25.2	V
			$V_i = -33V$, $1.0mA \leq I_o \leq 70mA$		-22.8		-25.2	
Quiescent Current		I_d	$T_j = +25°C$				6.5	mA
			$T_j = +125°C$				6.0	
Quiescent Current Change	With Line	I_d	$-28V \geq V_i \geq -38V$				1.5	mA
	With Load		$1.0mA \leq I_o \leq 40mA$				0.1	
Output Noise Voltage		V_N	$Ta = 25°C$, $10Hz \leq f \leq 100KHz$			200		μV
Ripple Rejection		RR	$f = 120Hz$, $-29V \geq V_i \geq -35V$ $T_j = 25°C$		31	47		dB
Dropout Voltage		V_D	$T_j = 25°C$			1.7		V

TYPICAL APPLICATION

Design Considerations

The MC79L00AC Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Fig. 1 POSITIVE AND NEGATIVE REGULATOR FIG.

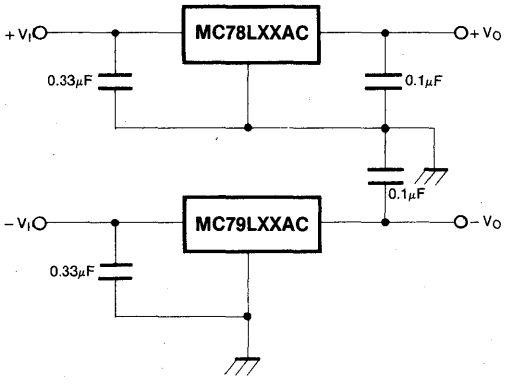
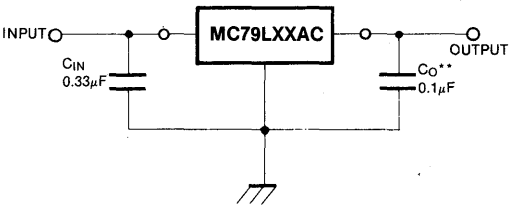


Fig. 2 TYPICAL APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.

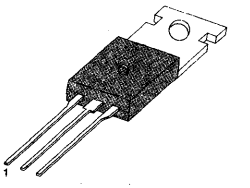
* = C_{IN} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

3-TERMINAL 0.5A NEGATIVE VOLTAGE REGULATOR

The MC79MXX series of 3-Terminal medium current negative voltage regulators are monolithic integrated circuits designed as fixed voltage regulators. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 500mA output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

TO-220



1: Input 2: GND 3: Output

FEATURES

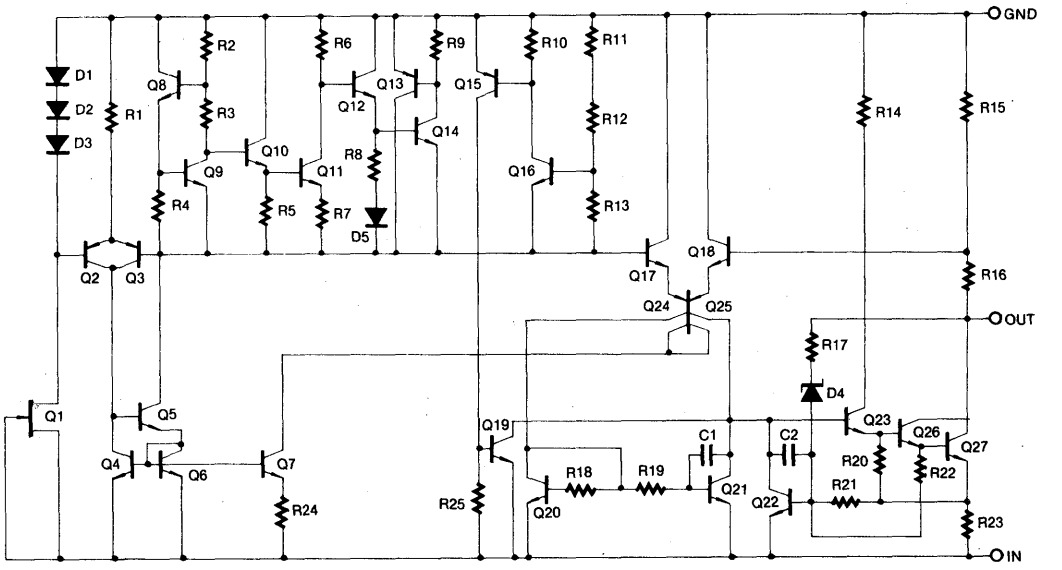
- **No external components required**
- **Output current in excess of 0.5A**
- **Internal thermal-overload protection**
- **Internal short circuit current limiting**
- **Output transistor safe-area compensation**
- **Available in JEDEC TO-220**
- **Output voltages of −5V, −6V, −8V, −12V, −15V, −18V, −24V**

ORDERING INFORMATION

Device	Package	Operation Temperature
MC79MXXCT	TO-220	0 ~ 125°C
**MC79MXXIT	TO-220	−40 ~ 125°C

** Under development

SCHEMATHIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (for $V_o = -5$ to $-1.8V$) (for $V_o = 24V$)	V_{IN}	-35 -40	V V
Thermal Resistance Junction-Case Junction-Air	0_{JC} 0_{JA}	5 65	°C/W °C/W
Operating Temperature Range	T_{opr}	$0 \sim +125$	°C
Storage Temperature Range	T_{stg}	$-65 \sim +150$	°C

ELECTRICAL CHARACTERISTICS MC79M05C

(Refer to test circuit, $0°C < T_j < 125°C$, $I_o = 350mA$, $V_i = -10V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		-4.8	-5.0	-5.2	V
		$5.0mA \leq I_o \leq 350mA$ $V_i = -7V$ to $-25V$		-4.75	-5.0	-5.25	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = -7V$ to $-25V$		7.0	50	mV
			$V_i = -8V$ to $-18V$		2.0	30	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $500mA$		30	100	mV
Quiescent Current	I_d	$T_j = 25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5.0mA$ to $350mA$				0.4	mA
		$V_i = -8V$ to $-25V$				0.4	
Output Voltage Drift	$\triangle V_o / \triangle T$	$I_o = 5mA$			0.2		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			40		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = -8$ to $-18V$		54	60		dB
Dropout Voltage	V_D	$I_o = 500mA$, $T_j = 25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i = -35V$, $T_j = 25°C$			140		mA
Peak Current	I_{peak}	$T_j = 25°C$			650		mA

ELECTRICAL CHARACTERISTICS MC79M06C

(Refer to test circuit, $0°C < T_j < 125°C$, $I_o = 350mA$, $V_i = -11V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		-5.75	-6.0	-6.25	V
		$5.0mA \leq I_o \leq 350mA$ $V_i = -8.0V$ to $-25V$		-5.7	-6.0	-6.3	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = -8V$ to $-25V$		7.0	60	mV
			$V_i = -9V$ to $-19V$		2.0	40	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $500mA$		30	120	mV
Quiescent Current	I_d	$T_j = 25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5.0mA$ to $350mA$				0.4	mA
		$V_i = -8.0V$ to $-25V$				0.4	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			0.4		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			50		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = -9$ to $-19V$		54	60		dB
Dropout Voltage	V_D	$I_o = 500mA$, $T_j = 25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i = -35V$, $T_j = 25°C$			140		mA
Peak Current	I_{peak}	$T_j = 25°C$			650		mA

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC79M08C

(Refer to test circuit, $0°C < T_j < 125°C$, $I_o = 350mA$, $V_i = -14V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		-7.7	-8.0	-8.3	V
		$5.0mA \leq I_o \leq 350mA$ $V_i = -10.5V$ to $-25V$		-7.6	-8.0	-8.4	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = -10.5V$ to $-25V$		7.0	80	mV
			$V_i = -11V$ to $-21V$		2.0	50	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $500mA$		30	160	mV
Quiescent Current	I_d	$T_j = 25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5.0mA$ to $350mA$				0.4	mA
		$V_i = -10.5V$ to $-25V$				0.4	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-0.6		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			60		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = -11.5V$ to $-21.5V$		54	59		dB
Dropout Voltage	V_D	$I_o = 500mA$, $T_j = 25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i = -35V$, $T_j = 25°C$			140		mA
Peak Current	I_{peak}	$T_j = 25°C$			650		mA

ELECTRICAL CHARACTERISTICS MC79M12C

(Refer to test circuit, $0°C<T_j<125°C$, $I_o=350mA$, $V_i=-19V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j=25°C$		-11.5	-12	-12.5	V
		$5.0mA\leq I_o\leq 350mA$, $V_i=-14.5V$ to $-30V$		-11.4	-1.2	-12.6	
Line Regulation	$\triangle V_o$	$T_j=25°C$	$V_i=-14.5V$ to $-30V$		8.0	80	mV
			$V_i=-15V$ to $-25V$		3.0	50	
Load Regulation	$\triangle V_o$	$T_j=25°C$	$I_o=5.0mA$ to $500mA$		30	240	mV
Quiescent Current	I_d	$T_j=25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o=5.0mA$ to $350mA$				0.4	mA
		$V_i=-14.5V$ to $-30V$				0.4	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o=5mA$			-0.8		mV/°C
Output Noise Voltage	V_N	$f=10Hz$ to $100KHz$ $T_j=25°C$			75		μV
Ripple Rejection	RR	$f=120Hz$, $V_i=-15V$ to $-25V$		54	60		dB
Dropout Voltage	V_D	$I_o=500mA$, $T_j=25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i=-35V$, $T_j=25°C$			140		mA
Peak Current	I_{peak}	$T_j=25°C$			650		mA

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC79M15C

(Refer to test circuit, $0°C<T_j<125°C$, $I_o=350mA$, $V_i=-23V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j=25°C$		-14.4	-15	-15.6	V
		$5.0mA\leq I_o\leq 350mA$, $V_i=-17.5V$ to $-30V$		-14.25	-15	-15.75	
Line Regulation	$\triangle V_o$	$T_j=25°C$	$V_i=-17.5V$ to $-30V$		9.0	80	mV
			$V_i=-18V$ to $-28V$		5.0	50	
Load Regulation	$\triangle V_o$	$T_j=25°C$	$I_o=5.0mA$ to $500mA$		30	240	mV
Quiescent Current	I_d	$T_j=25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o=5.0mA$ to $350mA$				0.4	mA
		$V_i=-17.5V$ to $-28V$				0.4	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o=5mA$			-1.0		mV/°C
Output Noise Voltage	V_N	$f=10Hz$ to $100KHz$ $T_j=25°C$			90		μV
Ripple Rejection	RR	$f=120Hz$, $V_i=-18.5V$ to $-28.5V$		54	59		dB
Dropout Voltage	V_D	$I_o=500mA$, $T_j=25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i=-35V$, $T_j=25°C$			140		mA
Peak Current	I_{peak}	$T_j=25°C$			650		mA

ELECTRICAL CHARACTERISTICS MC79M18C

(Refer to test circuit, $0°C<T_j<125°C$, $I_o=350mA$, $V_i=-27V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j=25°C$		−17.3	−18	−18.7	V
		$5.0mA \le I_o \le 350mA$ $V_i=-21V$ to $-33V$		−17.1	−18	−18.9	
Line Regulation	$\triangle V_o$	$T_j=25°C$	$V_i=-21V$ to $-33V$		9.0	80	mV
			$V_i=-24V$ to $-30V$		5.0	60	
Load Regulation	$\triangle V_o$	$T_j=25°C$	$I_o=5.0mA$ to 500mA		30	360	mV
Quiescent Current	I_d	$T_j=25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o=5.0mA$ to 350mA				0.4	mA
		$V_i=-21V$ to $-33V$				0.4	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o=5mA$			−1.0		mV/°C
Output Noise Voltage	V_N	$f=10Hz$ to 100KHz $T_j=25°C$			110		μV
Ripple Rejection	RR	$f=120Hz$, $V_i=-22V$ to $-32V$		54	59		dB
Dropout Voltage	V_D	$I_o=500mA$, $T_j=25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i=-35V$, $T_j=25°C$			140		mA
Peak Current	I_{peak}	$T_j=25°C$			650		mA

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC79M24C

(Refer to test circuit, $0°C<T_j<125°C$, $I_o=350mA$, $V_i=-33V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j=25°C$		−23	−24	−25	V
		$5.0mA \le I_o \le 350mA$ $V_i=-27V$ to $-38V$		−22.8	−24	−25.2	
Line Regulation	$\triangle V_o$	$T_j=25°C$	$V_i=-27V$ to $-38V$		9.0	80	mV
			$V_i=-30V$ to $-36V$		5.0	70	
Load Regulation	$\triangle V_o$	$T_j=25°C$	$I_o=5.0mA$ to 500mA		30	300	mV
Quiescent Current	I_d	$T_j=25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o=5.0mA$ to 350mA				0.4	mA
		$V_i=-27V$ to $-38V$				0.4	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o=5mA$			−1.0		mV/°C
Output Noise Voltage	V_N	$f=10Hz$ to 100KHz $T_j=25°C$			180		μV
Ripple Rejection	RR	$f=120Hz$, $V_i=-28V$ to $-38V$		54	58		dB
Dropout Voltage	V_D	$I_o=500mA$, $T_j=25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i=-35V$, $T_j=25°C$			140		mA
Peak Current	I_{peak}	$T_j=25°C$			650		mA

TYPICAL APPLICATION

Bypass capacitors are recommended for stable operation of the MC79MXXC series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.
The bypass capacitors, (2μF on the input, 1μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fig. 1 Fixed Output Regulator

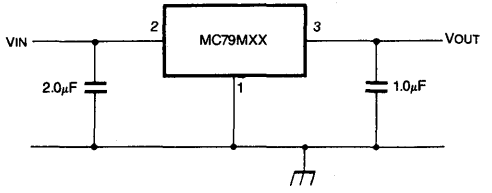
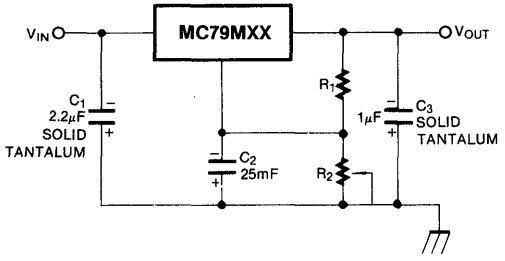


Fig. 2 Variable Output



Note

1. Required for stability. For value given, capacitor must be solid tantalum. 25μF aluminum electrolytic may be substituted.
2. C_2 improves transient response and ripple rejection. Do not increase beyond 50μF.

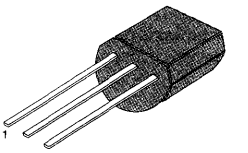
$$V_{OUT} = V_{SET}\left(\frac{R_1 + R_2}{R_1}\right)$$

Select R_2 as follows
MC79M05: 300Ω, MC79M12: 750Ω, MC79M15: 11Ω

VOLTAGE REFERENCE DIODE

The KA336-2.5 integrated circuit is precision 2.5V shunt regulator. The monolithic IC voltage references operates as a low temperature coefficient 2.5V zener with 0.2Ω dynamic impedance.
A third terminal on the KA336-2.5 allows the reference voltage and temperature coefficient to be trimmed easily.
KA336-2.5 is useful as a precision 2.5V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 2.5V make it convenient to obtain a stable reference from low voltage supplies.
Further, since the KA336-2.5 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

TO-92



1: ADJ, 2: +, 3: –

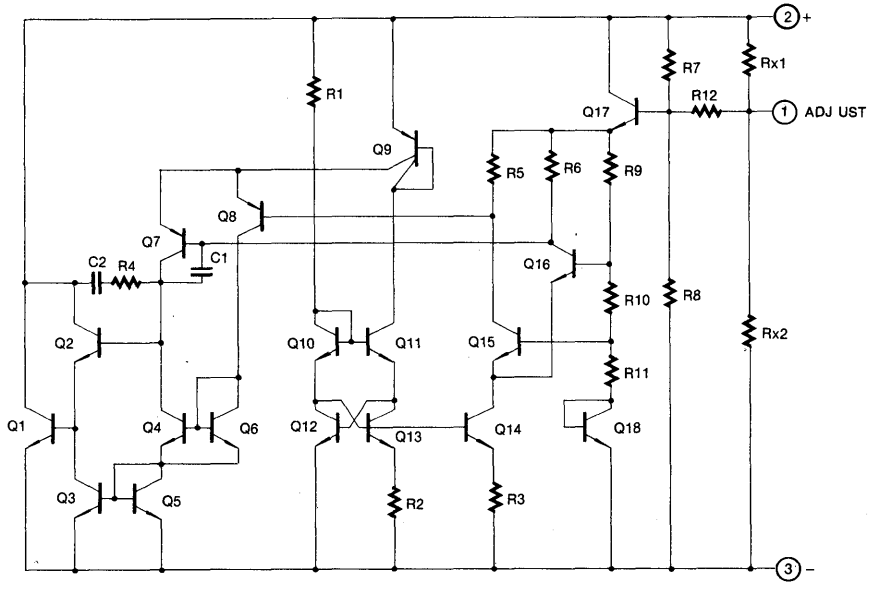
FEATURE

- **Low temperature coefficient**
- **Guaranteed temperature stability 4mV typical**
- **0.2Ω dynamic impedance**
- **±1.0% initial tolerance available.**
- **Easily trimmed for minimum temperature drift.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA336Z-2.5	TO-92	0 ~ 70°C
KA236Z-2.5		– 25 ~ +85°C

SCHEMATIC DIAGRAM



Rx1, Rx2: External Resistors

ABSOLUTE MAXIMUM RATINGS

Characteristic		Symbol	Value	Unit
Reverse Current		I_R	15	mA
Forward Current		I_F	10	mA
Operating Temperature Range	KA236-2.5 KA336-2.5	T_{opr}	$-25 \sim +85$ $0 \sim +70$	°C °C
Storage Temperature Range		T_{stg}	$-60 \sim +150$	°C

ELECTRICAL CHARACTERISTICS ($T_{min} < Ta < T_{max}$, unless otherwise specified)

Characteristic	Symbol	Test Condition	KA336/236			KA336B/236B			Unit
			Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	V_R	$Ta = 25°C$ $I_R = 1mA$	2.44	2.49	2.54	2.465	2.49	2.515	V
Reverse Breakdown Change with Current	$\triangle V_R$	$Ta = 25°C$ $400\mu A \leq I_R \leq 10mA$		2.6	6		2.6	10	mV
Reverse Dynamic Impedance	Z_D	$Ta = 25°C$ $I_R = 1mA$		0.2	0.6		0.2	1	Ω
Temperature Stability	$\triangle V_R T_1$	$I_R = 1mA$ $T_{min} \leq Ta \leq T_{max}$		1.8	6		1.8	6	mV
Reverse Breakdown Change with Current	$\triangle V_R T_2$	$T_{min} \leq Ta \leq T_{max}$ $400\mu A \leq I_R \leq 10mA$		3	10		3	12	mV
Reverse Dynamic Impedance	Z_{DT}	$I_R = 1mA$ $T_{min} \leq Ta \leq T_{max}$		0.4	1		0.4	1.4	Ω
Long Term Stability	S	$I_R = 1mA$ $T_{min} \leq Ta \leq T_{max}$		20			20		ppm

* $T_{min} \leq Ta \leq T_{max}$
KA236: $T_{min} = -25°C$, $T_{max} = 85°C$
KA336: $T_{min} = 0°C$, $T_{max} = 70°C$

4

TYPICAL PERFORMANCE CHARACTERISTIC

Fig. 1. REVERSE VOLTAGE CHANGE

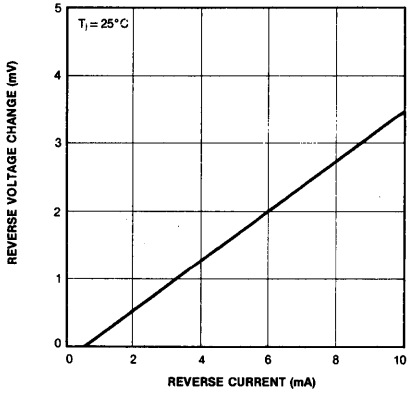


Fig. 2 REVERSE CHARACTERISTICS

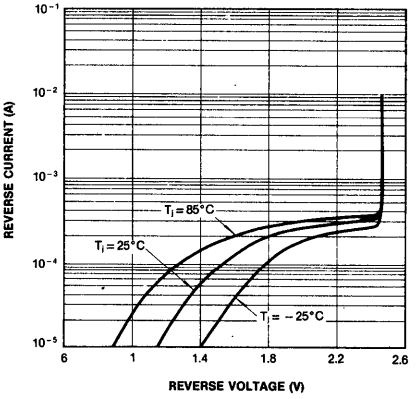


Fig. 3 TEMPERATURE DRIFT

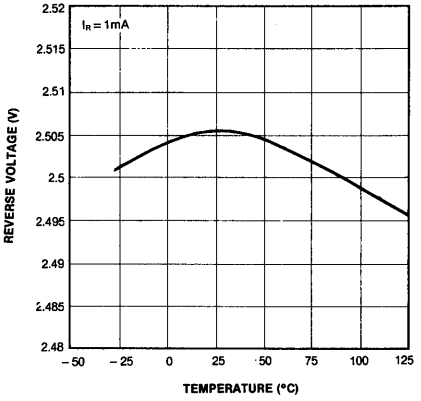
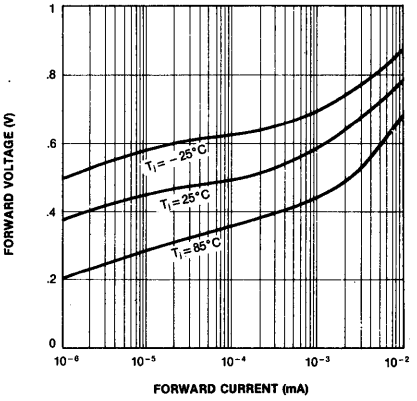


Fig. 4 FORWARD CHARACTERISTICS



TYPICAL APPLICATIONS

Fig. 5 2.5V REFERENCE

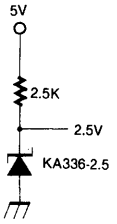
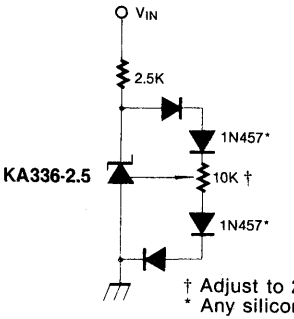
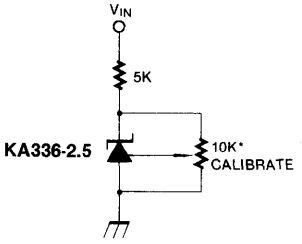


Fig. 6 2.5V Reference with minimum temperature coefficient



† Adjust to 2.490V
* Any silicon signal diode

Fig. 7 Trimmed 4V to 6V reference with temperature coefficient of breakdown voltage independent



* Does not affect temperature coefficient

Fig. 8 Precision power regulator with low temperature coefficient

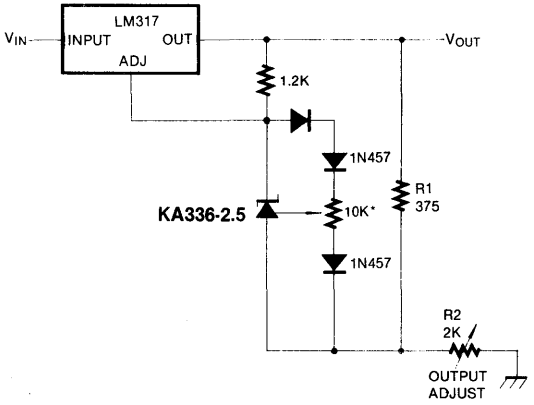
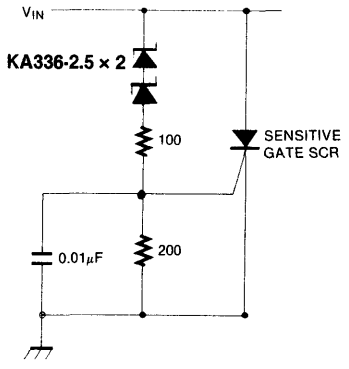


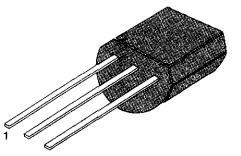
Fig. 9 5V Crowbar



VOLTAGE REFERENCE DIODE

The KA236/KA336-5.0 integrated circuit is precision 5.0V shunt regulator. The monolithic IC voltage references operate as a low temperature coefficient 5.0V zener with 0.6 ohm dynamic impedance. A third terminal on the KA236/KA336-5.0 allows the reference voltage and temperature coefficient to be trimmed easily.
KA236/KA336-5.0 is useful as a precision 5.0V low voltage references for digital voltmeters, power supplies or op amp circuitry. The 5.0V make it convenient to obtain a stable reference from low voltage supplies. Further, since the KA236/KA336-5.0 operates as a shunt regulators, it can be used as either a positive or negative voltage reference.
KA236 is characterized for operation from $-25°C$ to $85°C$, and KA336 from $0°C$ to $70°C$.

TO-92



1: ADJ, 2: +, 3: –

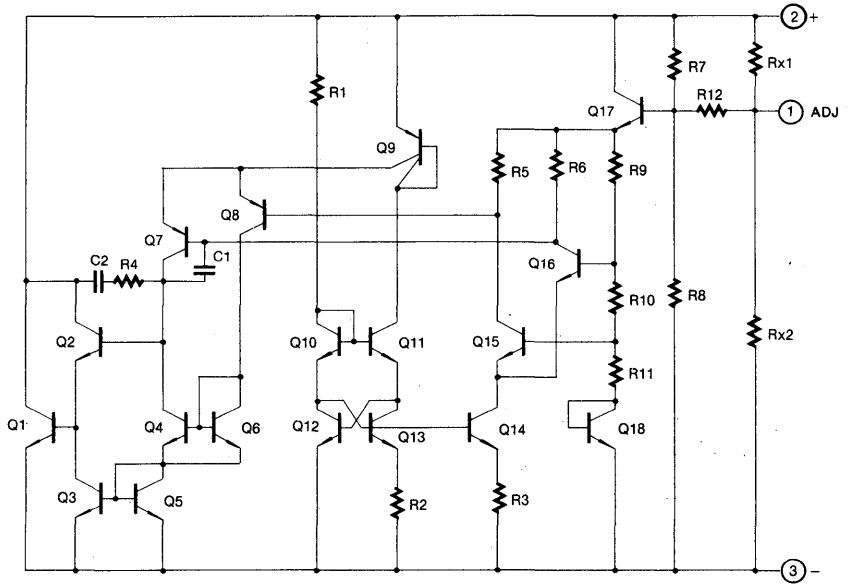
FEATURES

- **Low temperature coefficient**
- **Adjustable 4V to 6V**
- **Wide operating range current of 400μA to 10mA**
- **Three lead transistor package (To-92)**
- **0.6 ohm dynamic impedance**
- **±1.0% initial tolerance available**
- **Guaranteed temperature stability**
- **Easily trimmed for minimum temperature drift**
- **Fast turn on**

ORDERING INFORMATION

Device	Package	Operation Temperature
S336Z-5.0	TO-92	0 ~ 70°C
S236Z-5.0		– 25 ~ 85°C

SCHEMATIC DIAGRAM



Rx1, Rx2: External Resistors

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Reverse Current	I_R	15	mA
Forward Current	I_F	10	mA
Operating Temperature Range KA236-5.0 KA336-5.0	T_{opr}	 $-25 \sim +85$ $0 \sim +70$	°C
Storage Temperature Range	T_{stg}	$-60 \sim +150$	°C

ELECTRICAL CHARACTERISTICS

($T_{min} \leq T_a \leq T_{max}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA336/236			KA336B/236B			Unit
			Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	V_R	$T_a = 25°C$, $I_R = 1mA$	4.8	5.0	5.2	4.9	5.0	5.1	V
Reverse Breakdown Change with Current	$\triangle V_R$	$T_a = 25°C$ $600\mu A \leq I_R \leq 10mA$	—	6	20	—	6	20	mV
Reverse Dynamic Impedance	Z_D	$T_a = 25°C$, $I_R = 1mA$	—	0.6	2	—	0.6	2	Ω
Temperature Stability	$\triangle V_R T_1$	$I_R = 1mA$ $T_{min} \leq T_a \leq T_{max}$	—	4	12	—	4	12	mV
Reverse Breakdown Change with Current	$\triangle V_R T_2$	$600\mu A \leq I_R \leq 10mA$ $T_{min} \leq T_a \leq T_{max}$	—	6	24	—	6	24	mV
Reverse Dynamic Impedance	Z_{DT}	$I_R = 1mA$ $T_{min} \leq T_a \leq T_{max}$	—	0.8	2.5	—	0.8	2.5	Ω
Long Term Stability	S	$I_R = 1mA$ $T_{min} \leq T_a \leq T_{max}$	—	20	—	—	20	—	ppm

* $T_{min} \leq T_a \leq T_{max}$
KA236: $T_{min} = -25°C$, $T_{max} = 85°C$
KA336: $T_{min} = 0°C$, $T_{max} = 70°C$

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 REVERSE VOLTAGE CHANGE

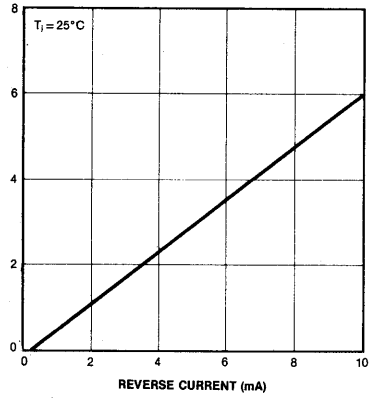
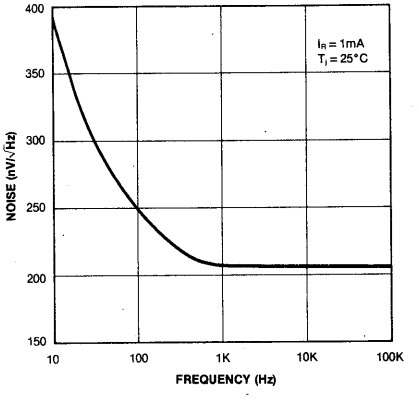


Fig. 2 ZENER NOISE VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 DYNAMIC IMPEDANCE

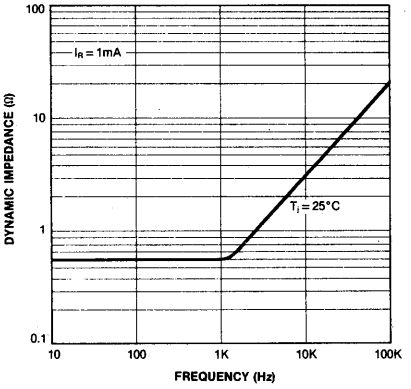


Fig. 4 RESPONSE TIME

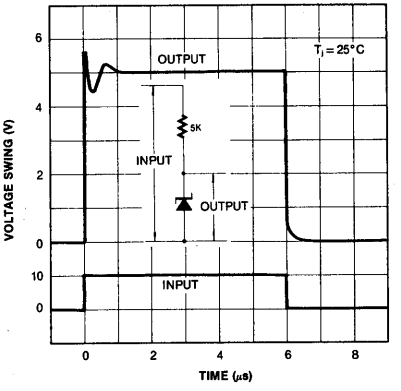


Fig. 5 REVERSE CHARACTERISTICS

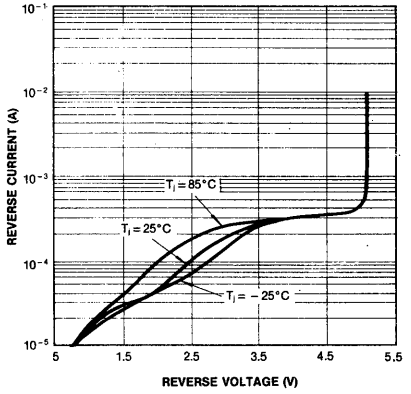


Fig. 6 TEMPERATURE DRIFT

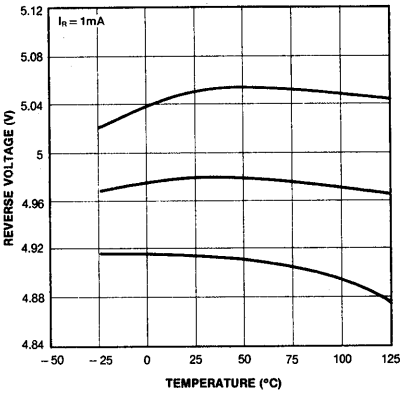
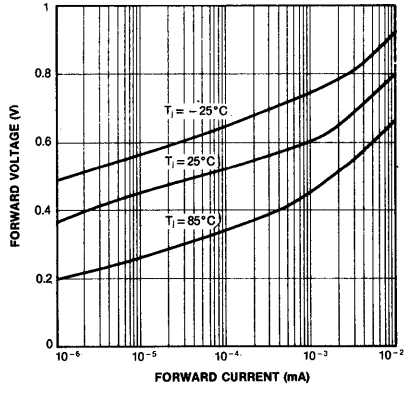


Fig. 7 FORWARD CHARACTERISTICS



TYPICAL APPLICATIONS

Fig. 8 5.0V REFERENCE

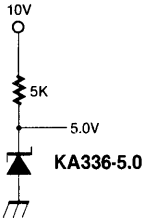
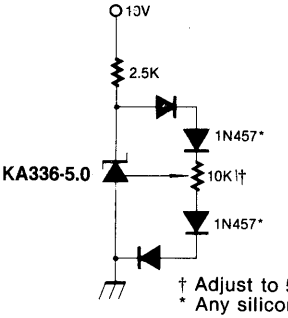
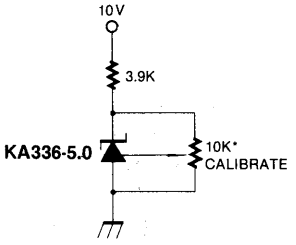


Fig. 9 5.0V REFERENCE WITH MINIMUM TEMPERATURE COEFFICIENT



† Adjust to 5V
* Any silicon signal diode

Fig. 10 TRIMMED 4V TO 6V REFERENCE WITH TEMPERATURE COEFFICIENT INDEPENDENT OF BREAKDOWN VOLTAGE



* Does not affect temperature coefficient

FIGURE 10

Fig. 11 PRECISION POWER REGULATOR WITH LOW TEMPERATURE COEFFICIENT

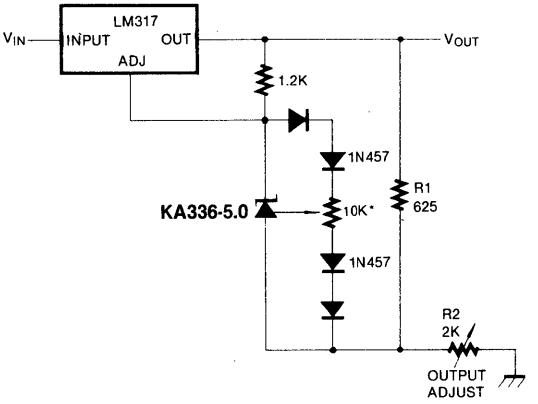
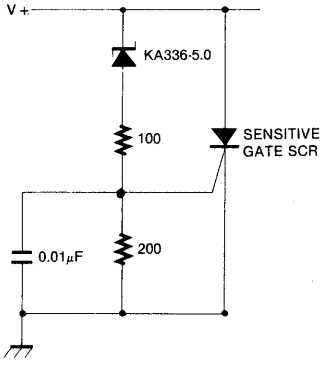
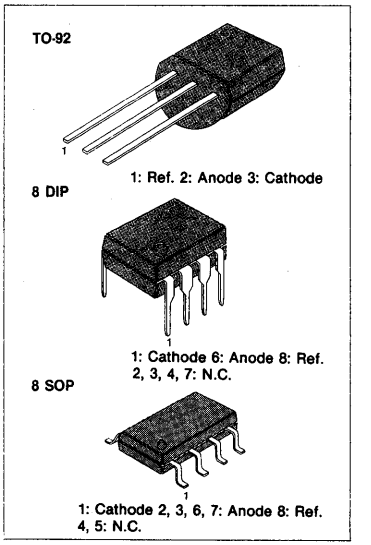


Fig. 12 5V CROWBAR



PROGRAMMABLE PRECISION REFERENCES

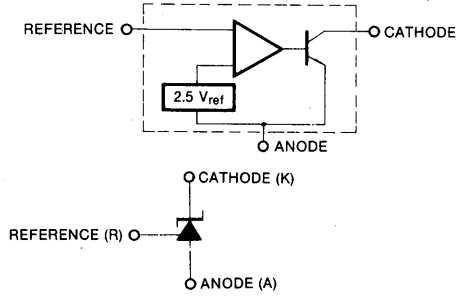
The KA431 is a three-terminal adjustable regulator series with guaranteed thermal stability over applicable temperature ranges. The output voltage may be set to any value between V_{ref} (approximately 2.5 volts) and 36 volts with two external resistors. These devices have a typical dynamic output impedance of 0.2Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacement for zener diodes in many applications.
KA431I is characterized for operation from −40°C to +85°C, and KA431C from 0°C to 70°C.



FEATURES

- **Programmable output voltage to 36 volts**
- **Low dynamic output impedance 0.2Ω typical**
- **Sink current capability of 1.0 to 100mA**
- **Equivalent full-range temperature coefficient of 50ppm/°C typical**
- **Temperature compensated for operation over full rated operating temperature range**
- **Low output noise voltage**
- **Fast turn on response**

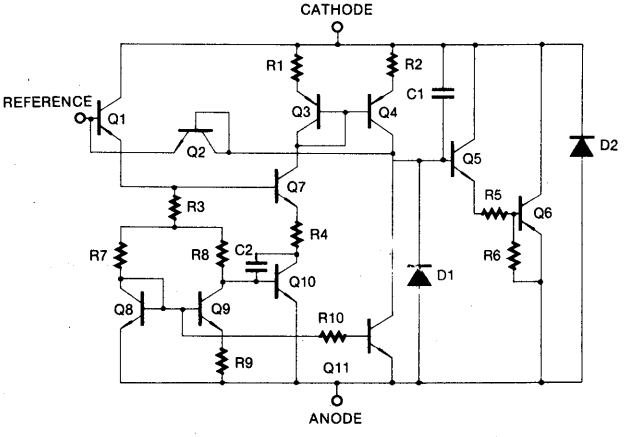
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Operating Temperature	Package
S431CZ	0 ~ +70°C	TO-92
KA431CN	0 ~ +70°C	8 DIP
KA431CD	0 ~ +70°C	8 SOP
S431IZ	−40 ~ +85°C	TO-92
KA431IN	−40 ~ +85°C	8 DIP

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operating temperature range applies unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Cathode Voltage	V_{KA}	37	V
Cathode Current Range (Continuous)	I_K	$-100 \sim +150$	mA
Reference Input Current Range	I_{REF}	$0.05 \sim +10$	mA
Power Dissipation D, Z Suffix Package N Suffix Package	P_D	 770 1000	 mW mW
Operating Temperature Range KA431CZ, KA431CN, KA431CD KA431IZ, KA431IN	T_{opr}	 $0 \sim +70$ $-40 \sim +85$	 °C °C
Storage Temperature Range	T_{stg}	$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS

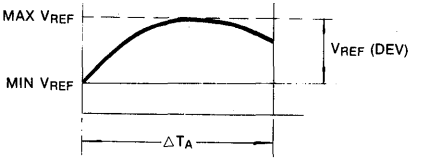
Characteristic	Symbol	Min	Typ	Max	Unit
Cathode Voltage	V_{KA}	V_{REF}		36	V
Cathode Current	I_K	1.0		100	mA

ELECTRICAL CHARACTERISTICS (Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit	*T/C
Reference Input Voltage	V_{REF}	$V_{KA} = V_{REF}$ $I_K = 10mA$	Ta = 25°C	2.440	2.495	2.550	V	1
			Ta = 0°C to 70°C	2.423		2.567		
Deviation of Reference Input Voltage Over Temperature 1	$V_{REF(dev)}$	$V_{KA} = V_{REF}$, $I_K = 10mA$ Ta = 0°C to 70°C			8	17	mV	1
Ratio of Change in Reference Input Voltage to the Change in Cathode Voltage	$\frac{V_{REF}}{V_{KA}}$	$I_K = 10mA$	$V_{KA} = V_{REF}$ to 10V		−1.4	−2.7	mV/V	2
			$V_{KA} = 10V$ to 36V		−1.0	−2.0		
Reference Input Current	I_{REF}	$I_K = 10mA$ R1 = 10KΩ R2 = ∞	Ta = 25°C		2.0	4.0	μA	2
			Ta = 0°C to 70°C			5.2		
Reference Input Current Deviation Over Temperature Range	I_{REF}	$I_K = 10mA$, R1 = 10KΩ R2 = ∞ Ta = 0°C to 70°C			0.4	1.2	μA	2
Minimum Cathode Current for Regulation	I_{Kmin}	$V_{KA} = V_{REF}$			0.5	1.0	mA	1
Off-State Cathode Current	I_{Koff}	$V_{KA} = 36V$, $V_{REF} = 0V$			2.6	1000	nA	3
Dynamic Impedance 2	Z_{KA}	$V_{KA} = V_{REF}$ $I_K = 1.0$ to 100mA $f \leq 1.0KHz$			0.22	0.5	Ω	1

* Test Circuit

Note: 1. The deviation parameters $V_{REF(dev)}$ and $I_{REF(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The equivalent full-range temperature coefficient of the reference input voltage, αV_{REF} is defined as:



Max V_{REF} Min V_{REF} ΔT_A $V_{REF(dev)}$

$$\alpha V_{REF} \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}@25°C}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device.
αV_{REF} can be positive or negative depending on whether minimum V_{REF} or maximum V_{REF} respectively, occurs at the lower temperature

Example: Max $V_{REF} = 2500mV@30°C$, Min $V_{REF} = 2492mV@0°C$, $V_{REF} = 2495mV@25°C$, $\Delta T_A = 70°C$ for KA431C

$$\left|\alpha V_{REF}\right| = \frac{\left(\frac{8mV}{2495mV}\right) \times 10^6}{70°C} = 46ppm/°C$$

Because minimum V_{REF} occurs at the lower temperature, the coefficient is positive.

2. The dynamic impedance is defined as:

$$\left|Z_{KA}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operated with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$$\left|Z'\right| = \frac{\Delta V}{\Delta I} = \left|Z_{KA}\right| \left(1 + \frac{R1}{R2}\right)$$

TEST CIRCUIT

Fig. 1 Test Circuit for $V_{KA} = V_{REF}$

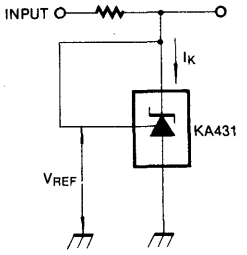


Fig. 2 Test Circuit for $V_{KA} \geq V_{REF}$

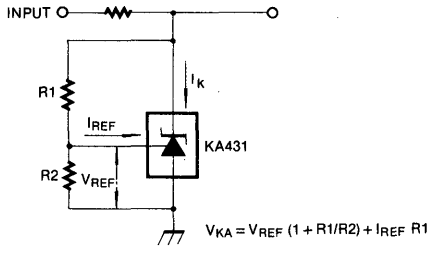
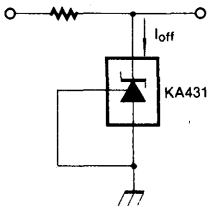


Fig. 3 Test Circuit for I_{off}



TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 4 CATHODE CURRENT VS CATHODE VOLTAGE

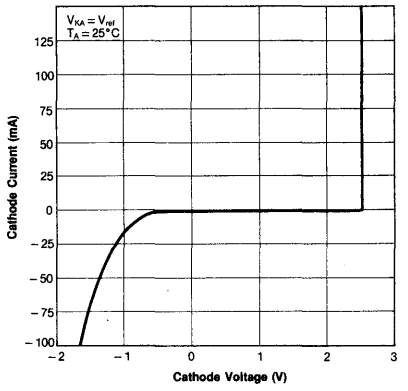


Fig. 5 CATHODE CURRENT VS CATHODE VOLTAGE

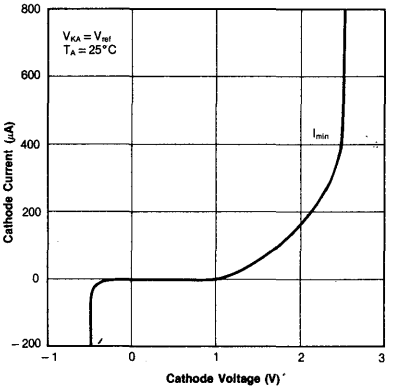


Fig. 6 CHANGE IN REFERENCE INPUT VOLTAGE VS CATHODE VOLTAGE

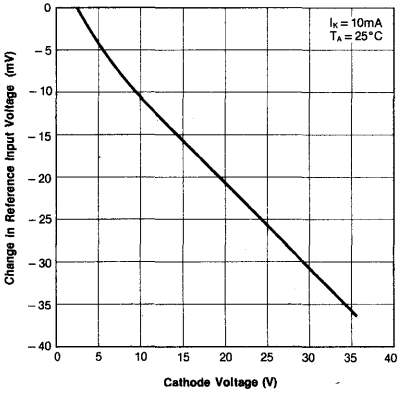


Fig. 7 NOISE VOLTAGE VS FREQUENCY

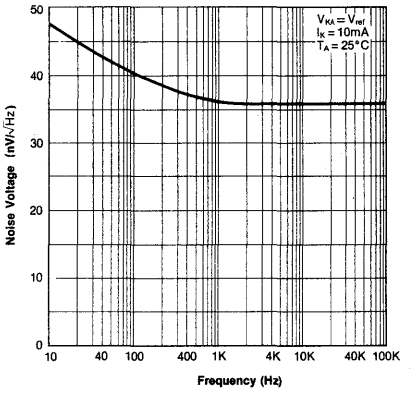


Fig. 8 DYNAMIC IMPEDANCE VS FREQUENCY

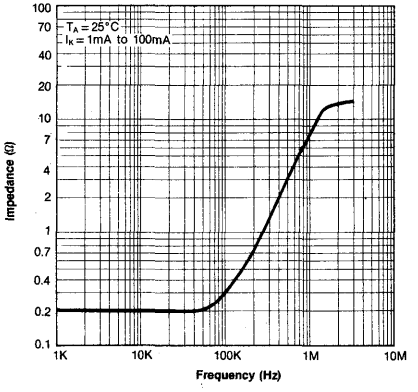
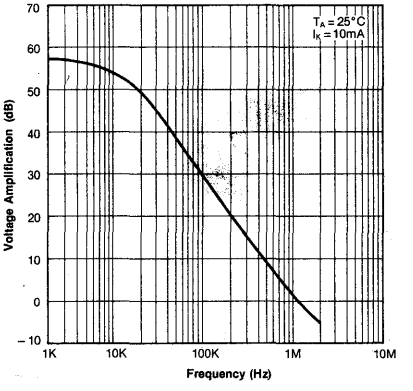


Fig. 9 SMALL SIGNAL VOLTAGE AMPLIFICATION VS FREQUENCY



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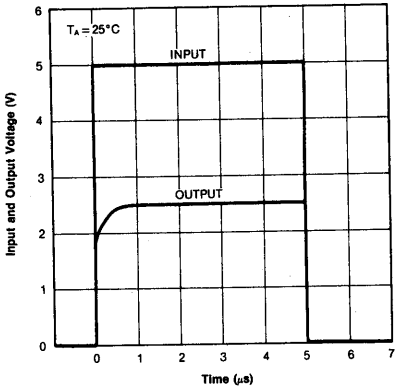
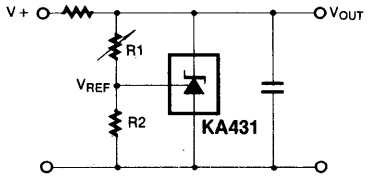
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 10 PULSE RESPONSE



TYPICAL APPLICATIONS

FIGURE 11—SHUNT REGULATOR



$$V_{out} = (1 + \frac{R1}{R2})V_{ref}$$

FIGURE 12—SINGLE-SUPPLY COMPARATOR WITH TEMPERATURE-COMPENSATED THRESHOLD

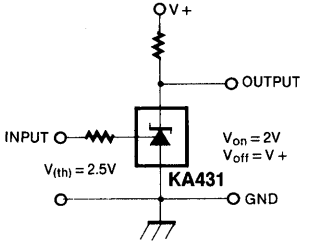
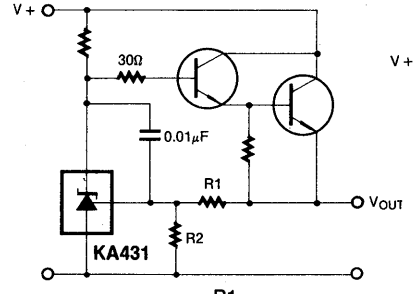
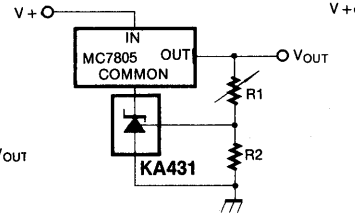


FIGURE 13—SERIES REGULATOR



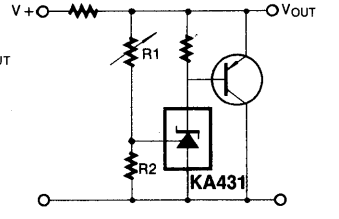
$$V_{out} = (1 + \frac{R1}{R2})V_{ref}$$

FIGURE 14—OUTPUT CONTROL OF A THREE-TERMINAL FIXED REGULATOR



$$V_{OUT} = V_{REF}(1 + \frac{R1}{R2})$$

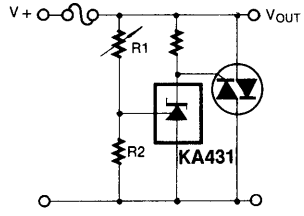
FIGURE 15—HIGHER-CURRENT SHUNT REGULATOR



$$V_{OUT} = (1 + \frac{R1}{R2})V_{ref}$$

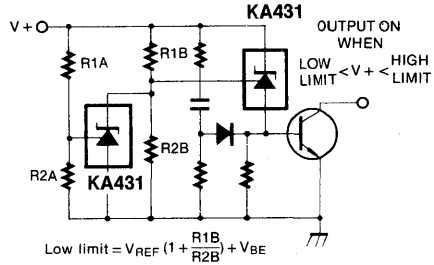
TYPICAL APPLICATIONS (Continued)

FIGURE 16—CROWBAR



$$V_{limit} = (1 + \frac{R1}{R2})V_{REF}$$

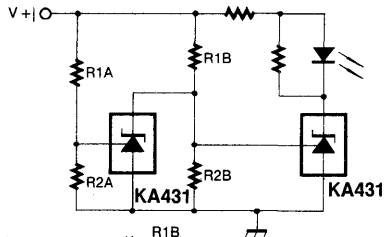
FIGURE 17—OVER-VOLTAGE/UNDER-VOLTAGE PROTECTION CIRCUIT



$$\text{Low limit} = V_{REF}(1 + \frac{R1B}{R2B}) + V_{BE}$$

$$\text{High limit} = V_{REF}(1 + \frac{R1A}{R2A})$$

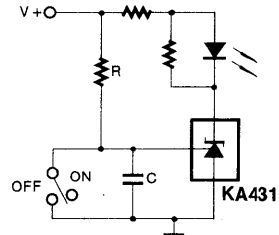
FIGURE 18—VOLTAGE MONITOR



$$\text{Low limit} = V_{REF}(1 + \frac{R1B}{R2B})$$

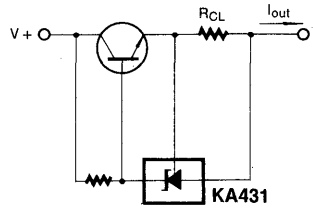
$$\text{High limit} = V_{REF}(1 + \frac{R1A}{R2A})$$

FIGURE 19—DELAY TIMER



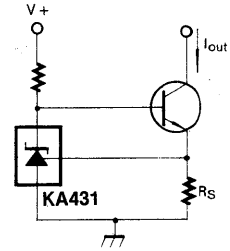
$$\text{Delay} = R\text{-}C\text{-}\ln\frac{V+}{(V+) - V_{REF}}$$

FIGURE 20—CURRENT LIMITER OR CURRENT SOURCE



$$I_{out} = \frac{V_{REF}}{R_{CL}}$$

FIGURE 21—CONSTANT-CURRENT SINK



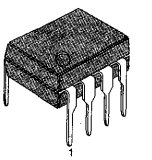
$$I_{out} = \frac{V_{REF}}{R_S}$$

4

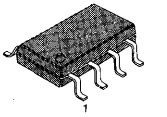
SINGLE OPERATIONAL AMPLIFIER

The KA201A and KA301A are general-purpose operational amplifiers which are externally phase compensated, permit a choice of operation for optimum high-frequency performance at a selected gain: unity-gain compensation can be obtained with a single capacitor.

8 DIP



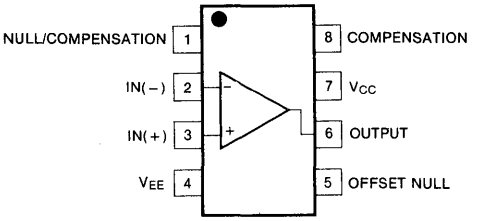
8 SOP



FEATURES

- **Short-circuit protection and latch-free operation**
- **Slew rate of 10V/μs as a summing amplifier**
- **Class AB output provides excellent linearity**
- **Low bias current**

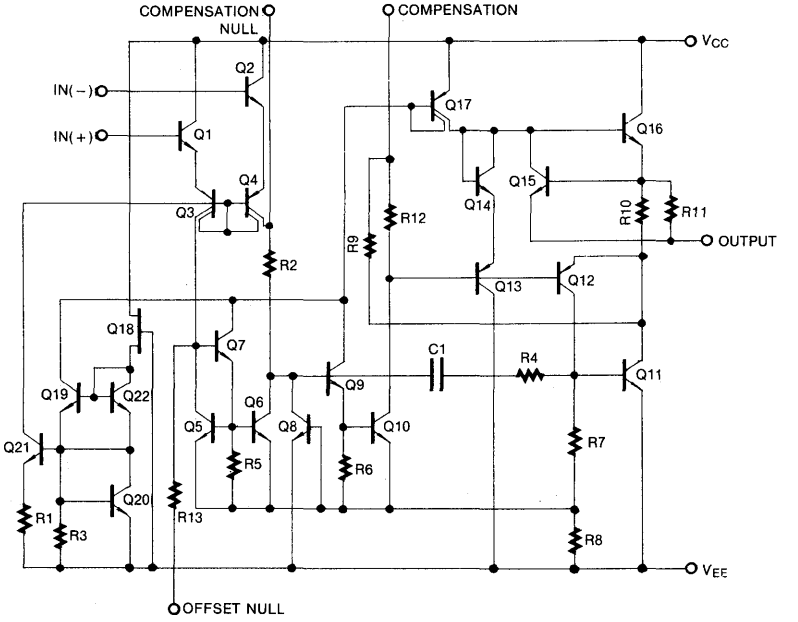
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KA201AN	8 DIP	−25 ~ +85°C
KA301AN		0 ~ +70°C
KA201AD	8 SOP	−25 ~ +85°C
KA301AD		0 ~ +70°C

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	KA201A	KA301A	Unit
Supply Voltage	V_S	±22	±18	V
Differential Input Voltage	V_{ID}	±30	±30	V
Input Voltage	V_I	±15	±15	V
Output Short Circuit Duration		Continuous	Continuous	
Power Dissipation	P_D	500	500	mW
Operating Temperature Range	T_{opr}	−25 ~ +85	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

($Ta = +25°C$, $V_{CC} = +15V$, $V_{EE} = -15V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		KA201A Min	KA201A Typ	KA201A Max	KA301A Min	KA301A Typ	KA301A Max	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 50K\Omega$			0.5	2.0		2.0	7.5	mV
			NOTE 1			3			10	mV
Input Offset Current	I_{IO}				1.5	10		4.5	50	nA
			NOTE 1			20			70	nA
Input Bias Current	I_{IB}				40	75		60	250	nA
			NOTE 1			100			300	nA
Supply Current	I_S	$V_S = \pm 20V$			2.0	3.0				mA
		$V_S = \pm 15V$						2.0	3.0	mA
		$V_S = \pm 20V$, $T_a = T_{amax}$			1.7	2.5				mA
Large Signal Voltage Gain	A_V	$V_{CC} = \pm 15V$, $R_L \geq 2K\Omega$, $V_o = \pm 10V$		50	160		25	160		V/mV
			NOTE 1	25			15			V/mV
Average Temperature Coefficient of Input Offset Voltage	$\triangle V_{IO}/\triangle T$	NOTE 1			3.0	15		6.0	30	μV/°C
Average Temperature Coefficient of Input Offset Current	$\triangle I_{IO}/\triangle T$	$25°C \leq T_a \leq T_{amax}$			0.01	0.1		0.01	0.3	nA/°C
		$T_{amin} \leq T_a \leq 25°C$			0.02	0.2		0.02	0.6	nA/°C
Input Voltage Range	V_{ICR}	$V_S = \pm 20V$	NOTE 1	±15						V
		$V_S = \pm 15V$	NOTE 1				±12			V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 50K\Omega$	NOTE 1	80	100		70	95		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 50K\Omega$	NOTE 1	80	100		70	100		dB
Output Voltage Swing	V_{OUT}	$V_S = \pm 15V$	$R_L = 10K\Omega$	±12	±14		±12	±14		V
			$R_L = 2.0K\Omega$	±10	±13		±10	±13		V
Input Resistance	R_i			1.5	4.0		0.5	2.0		MΩ

NOTE 1 KA201A: $-25 \leq T_a \leq +85°C$
KA301A: $0 \leq T_a \leq +70°C$

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

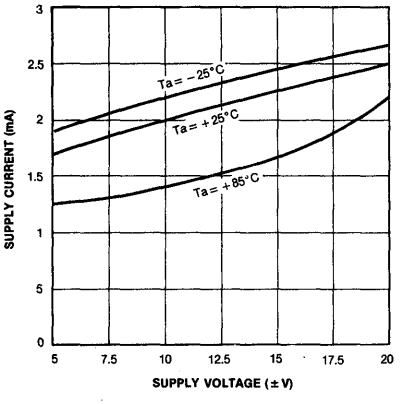


Fig. 2 VOLTAGE GAIN

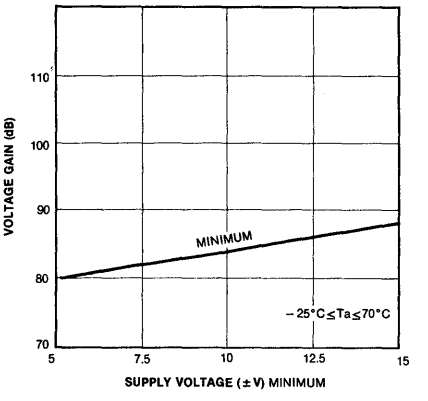


Fig. 3 CURRENT LIMITING

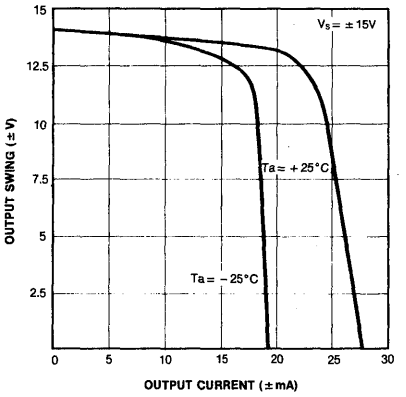


Fig. 4 INPUT CURRENT

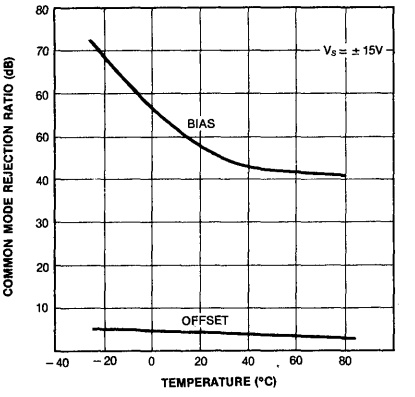


Fig. 5 POWER SUPPLY REJECTION

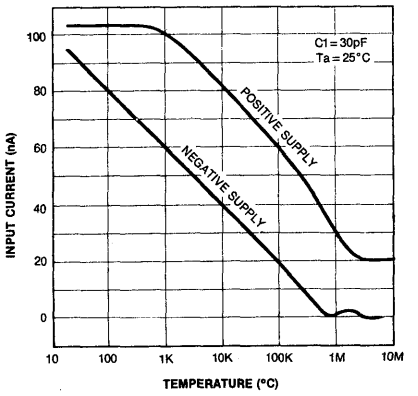


Fig. 6 COMMON MODE REJECTION

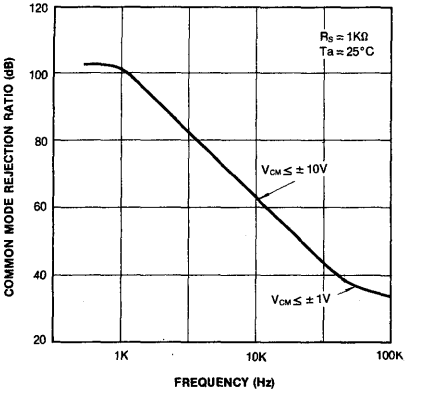
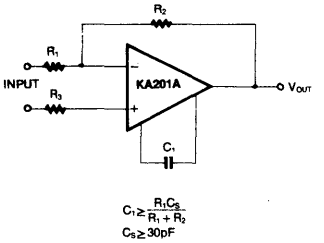


Fig. 7 SINGLE POLE COMPENSATION



$C_1 \geq \frac{R_1 C_S}{R_1 + R_2}$

$C_S \geq 30pF$

Fig. 8 OPEN LOOP FREQUENCY RESPONSE

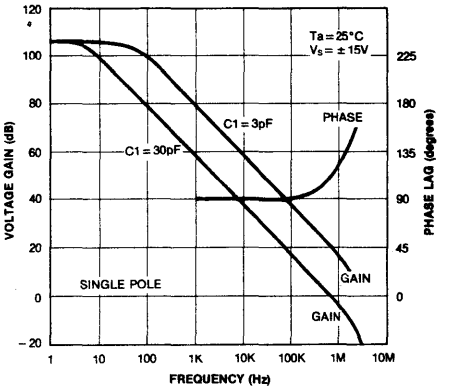


Fig. 9 LARGE SIGNAL FREQUENCY RESPONSE

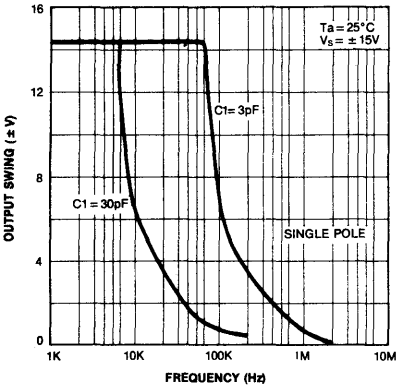


Fig. 10 VOLTAGE FOLLOWER PULSE RESPONSE

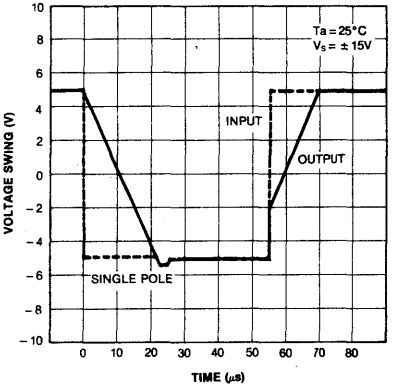
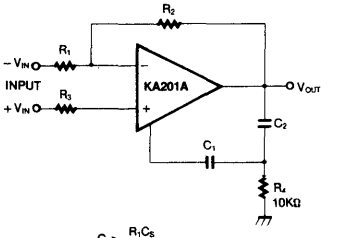


Fig. 11 TWO POLE COMPENSATION



$C_1 \geq \frac{R_1 C_S}{R_1 + R_2}$

$C_S = 30pF$

$C_2 = 10C_1$

Fig. 12 OPEN LOOP FREQUENCY RESPONSE

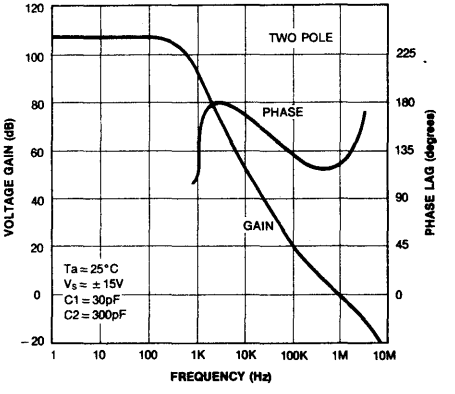


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Fig. 13 LARGE SIGNAL FREQUENCY RESPONSE

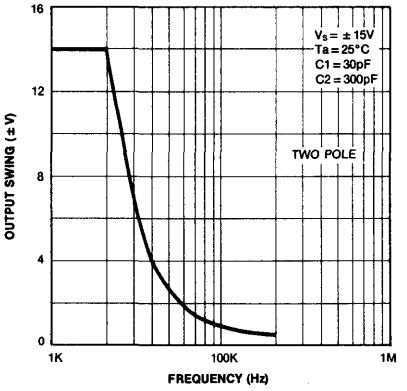


Fig. 14 VOLTAGE FOLLOWER PULSE RESPONSE

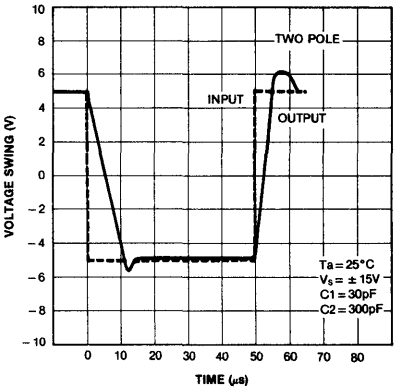


Fig. 15 FEEDFORWARD COMPENSATION

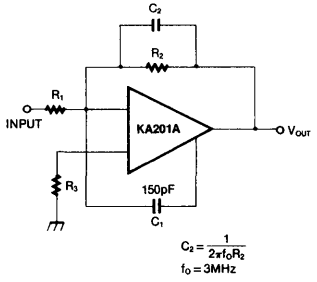


Fig. 16 OPEN LOOP FREQUENCY RESPONSE

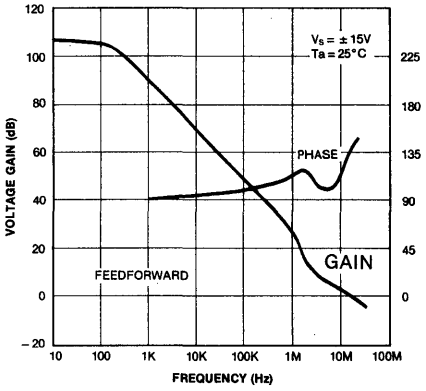


Fig. 17 LARGE SIGNAL FREQUENCY RESPONSE

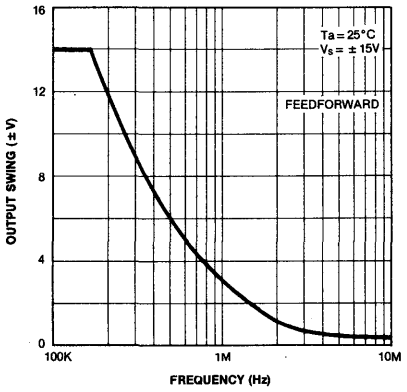
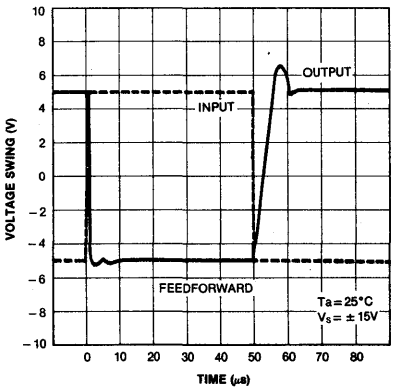
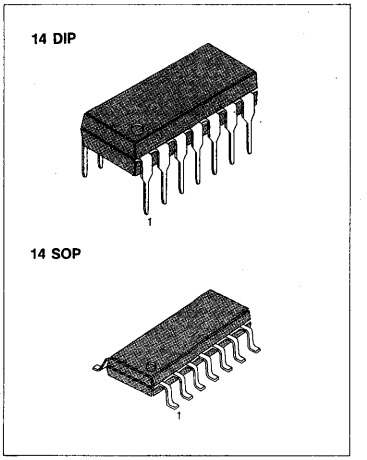


Fig. 18 INVERTER PULSE RESPOSE



DIFFERENTIAL VIDEO AMPLIFIER

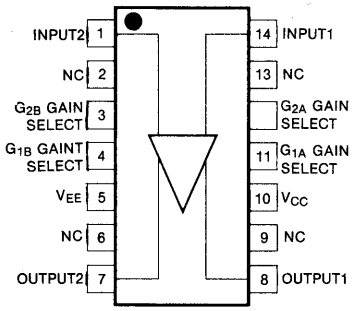
The KA733C is a monolithic differential input, differential output, wideband video amplifier.
The use of internal series-shunt feedback gives wide bandwidth with low phase distortion and high gain stability. The KA733C offers fixed gains 10,100,400 without external components, and adjustable gains from 10 to 400 by use of an external resistor.
The KA733C is intended for use as a high performance video and pluse amplifier in communications, magnetic memories, displays and video recorder systems.



FEATURES

- **120MHz bandwidth**
- **250KΩ input resistance**
- **Selectable gains of 10,100,400**
- **No frequency compensation required**

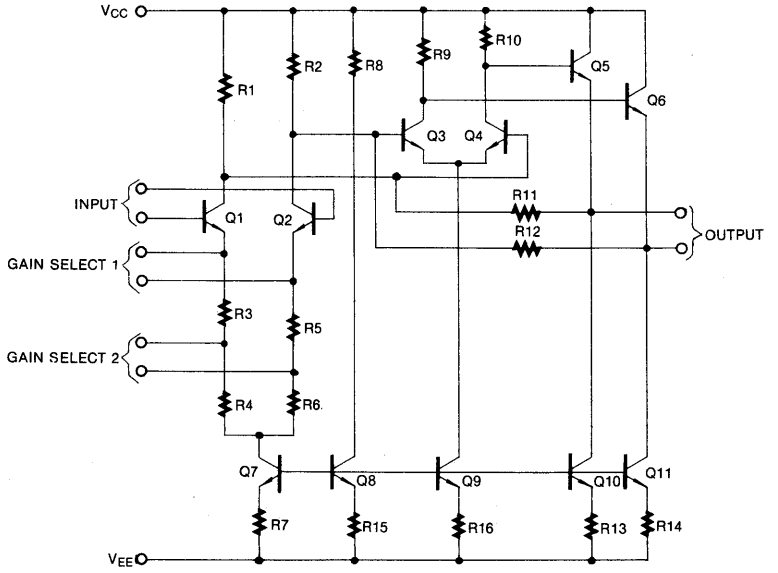
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KA733CN	14 DIP	0 ~ +70°C
KA733CD	14 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Differential Input Voltage	V_{ID}	±5	V
Common mode input Voltage	V_I	±6	V
Power Supply Voltage	V_S	±8	V
Output Current	I_O	10	mA
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{opr}	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +6V, V_{EE} = −6V, Ta = 25°C, unless otherwise specified)

Characteristic	Test Figure	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Voltage Gain Gain 1 (Note 1) Gain 2 (" 2) Gain 3 (" 3)	1	A_V	R_L = 2KΩ, V_{out} = $3V_{p-p}$	 250 80 8	 400 100 10	 600 120 12	V/V
Bandwidth Gain 1 (" 1) Gain 2 (" 2) Gain 3 (" 3)	2	BW	R_S = 50Ω		 40 90 120		MHz
Rise Time Gain 1 (" 1) Gain 2 (" 2) Gain 3 (" 3)	2	t_r	R_S = 50Ω V_{OUT} = $1V_{p-p}$		 10.5 4.5 2.5	 12	ns
Propagation Delay Gain 1 (" 1) Gain 2 (" 2) Gain 3 (" 3)	2	t_{pd}	R_S = 50Ω V_{OUT} = $1V_{p-p}$		 7.5 6.0 3.6	 10	ns
Input Resistance Gain 1 (" 1) Gain 2 (" 2) Gain 3 (" 3)	3	R_i	$V_{OD} \leq 1V$	 10	 4.0 30 250		KΩ
Input Offset Current		I_{IO}			0.4	5	μA
Input Bias Current		I_{IB}			9	30	μA
Input Voltage Range	1	V_{ICR}		±1			V
Common Mode Rejection Ratio Gain 2 Gain 2	4	CMRR	V_{CM} = ±1V, f ≤ 100KHz V_{CM} = ±1V, f = 5MHz	60	86 60		dB dB
Power Supply Rejection Ratio Gain 2	1	PSRR	$\triangle V_S$ = ±0.5V	50	70		dB
Output Offset Voltage Gain 1 Gain 2 and 3	1	V_{OO}	R_L = ∞		0.6 0.35	1.5 1.5	V V
Input Capacitance			Gain 2		2.0		pF

ELECTRICAL CHARACTERISTIC (Continued)

Characteristic	Test Figure	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Common Mode Voltage	1	V_{OCM}	$R_L = \infty$	2.4	2.9	3.4	V
Output Voltage Swing	1	V_{OUT}	$R_L = 2K\Omega$	3.0	4.0		V
Output Sink Current		I_{sink}		2.5	3.6		mA
Power Supply Current	1	I_S	$R_L = \infty$		18	24	mA
Output Resistance		R_o			20		Ω

ELECTRICAL CHARACTERISTICS

The following specifications apply over the range of $0°C \leq Ta \leq 70°C$ $V_{CC} = +6V$, $V_{EE} = -6V$

Characteristic	Test Figure	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Voltage Gain Gain 1 (Note 1) Gain 2 (Note 2) Gain 3 (Note 3)	1	A_V	$R_L = 2K\Omega$ $V_{out} = 3V_{p\text{-}p}$	 250 80 80		 600 120 12	V/V
Input Bias Current		I_{IB}				40	μA
Input Offset Current		I_{IO}				6.0	μA
Input Voltage Range	1	V_{ICR}		±1.0			V
Input Impedance (Gain 2)	3	R_i		8.0			KΩ
Common Mode Rejection Ratio Gain 2 (Note 2)	4	CMRR	$V_{CM} = \pm 1V$, $f \leq 100KHz$	50			dB
Power Supply Rejection Ratio Gain 2 (Note 2)	1	PSRR	$\triangle V_{CC} = \pm 0.5V$ $\triangle V_{EE} = \pm 0.5V$	50			dB
Output Offset Voltage Gain 1 (Note 1) Gain 2 and Gain 3 (Note 2, 3)	1	V_{OO}				 1.5 1.5	V
Output Voltage Swing	1	V_{OP}		2.8			V
Output Sink Current		I_{sink}		2.5			mA
Power Supply Current		I_S				27	mA

Notes 1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUITS

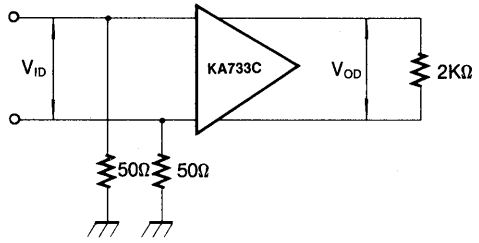


Fig. 1

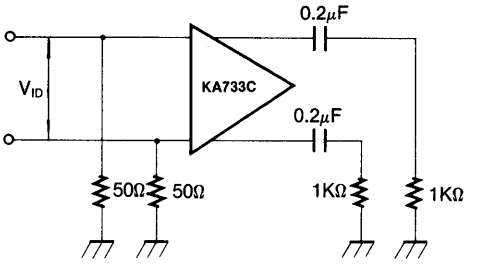


Fig. 2

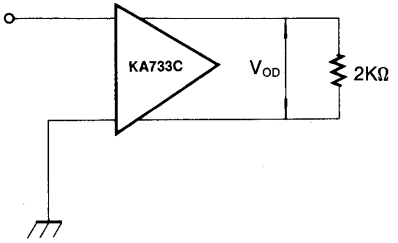


Fig. 3

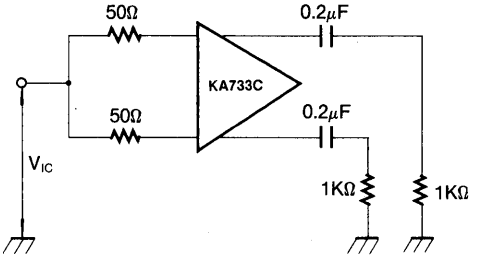


Fig. 4

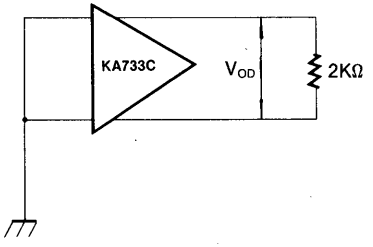
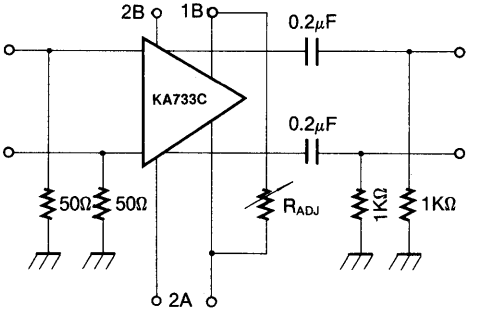


Fig. 5



VOLTAGE AMPLIFICATION ADJUSMENT

Fig. 6

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 7 PHASE SHIFT vs FREQUENCY

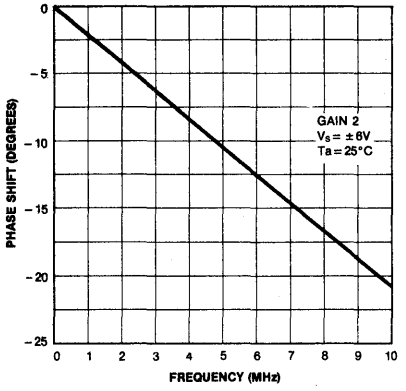


Fig. 8 PHASE SHIFT vs FREQUENCY

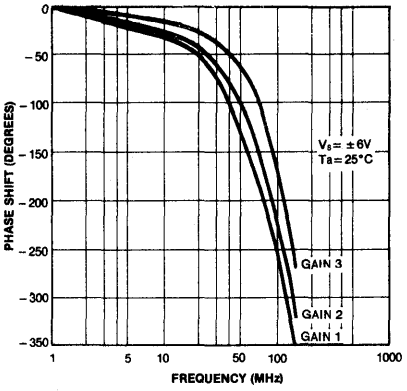


Fig. 9 VOLTAGE GAIN vs FREQUENCY

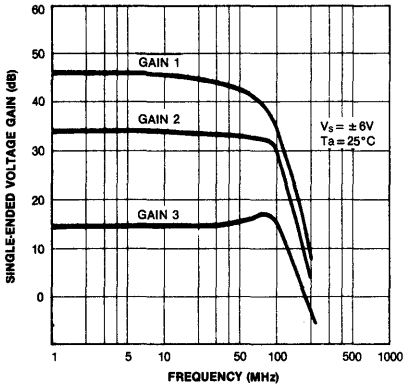


Fig. 9

Fig. 10 PULSE RESPONSE

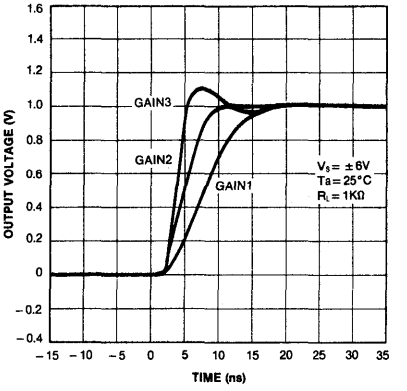


Fig. 11 PULSE RESPONSE vs SUPPLY VOLTAGE

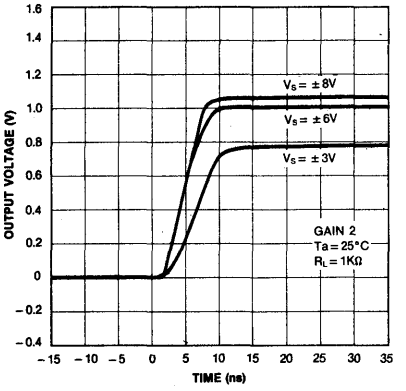


Fig. 12 PULSE RESPONSE vs TEMPERATURE

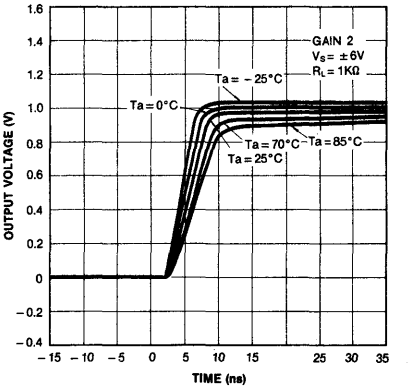


Fig. 13 COMMON MODE REJECTION RATIO vs FREQUENCY

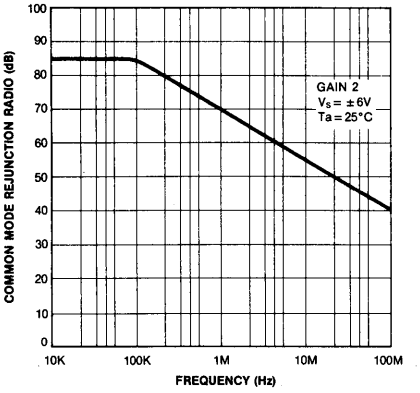


Fig. 14 OUTPUT VOLTAGE SWING vs FREQUENCY

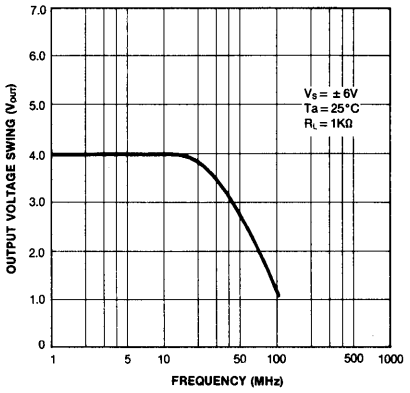


Fig. 15 DIFFERENTIAL OVERDRIVE RECOVERY TIME

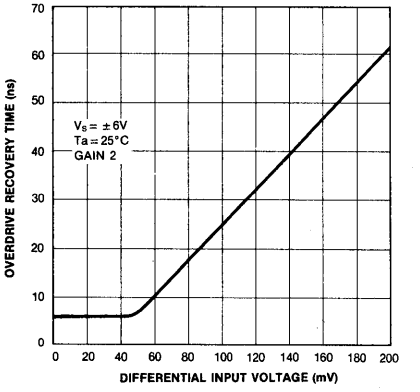


Fig. 16 VOLTAGE GAIN vs SUPPLY VOLTAGE

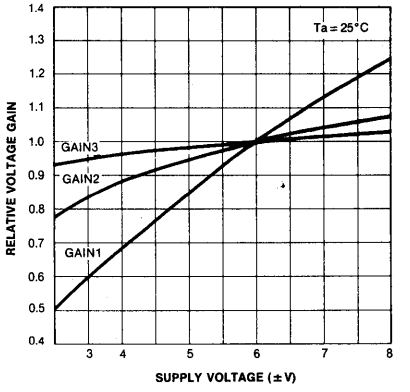


Fig. 17 OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

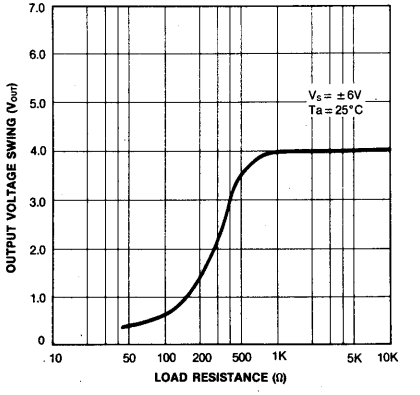


Fig. 18 GAIN vs FREQUENCY vs SUPPLY VOLTAGE

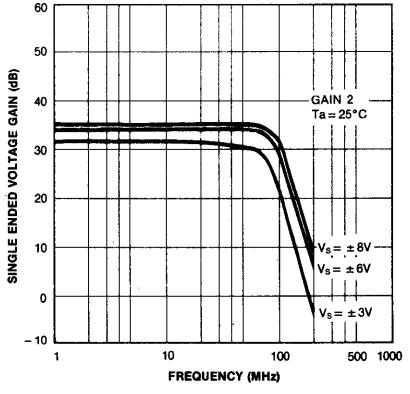


Fig. 19 SUPPLY CURRENT vs TEMPERATURE

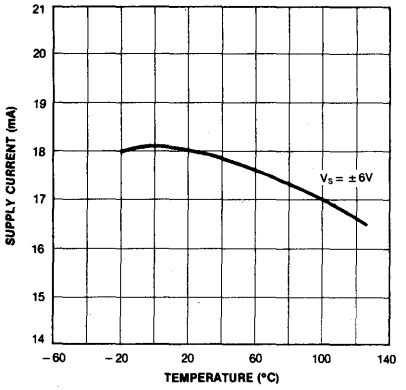


Fig. 20 SUPPLY CURRENT vs SUPPLY VOLTAGE

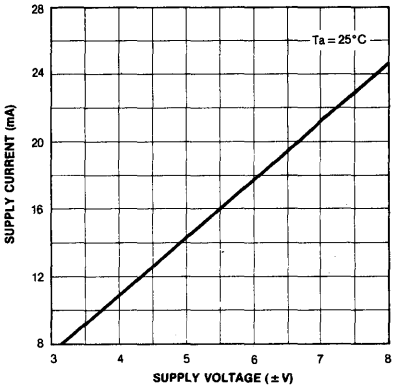


Fig. 21 VOLTAGE GAIN vs R_{ADJ}

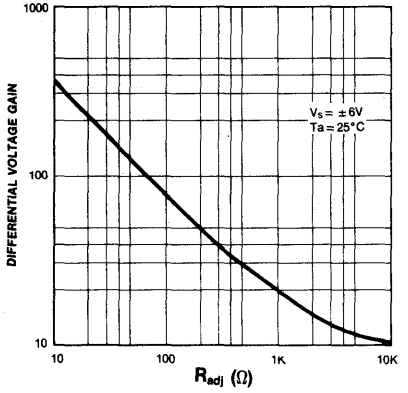
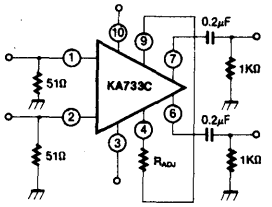


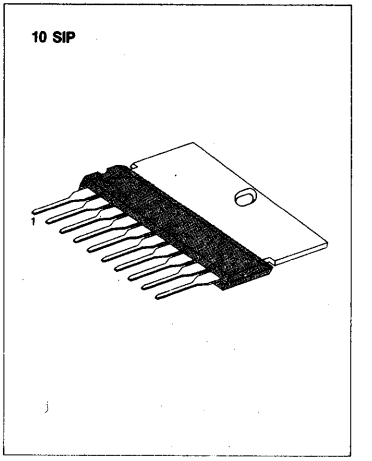
Fig. 22 VOLTAGE GAIN ADJUST CIRCUIT



4

DUAL POWER OPERATIONAL AMPLIFIER

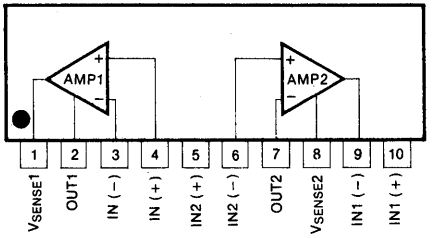
. The KA9256 is a dual power operational amplifier and it is output maximum current is 1.0A ($V_S = \pm 15V$). It can be used in arm driver for player, driver for brush motors forward and reverse rotation control and CD output driver for hole motor.



FEATURES

- **Interal current limiting: $I_{SC} = 350mA$ ($R_{SC} = 2.2\Omega$)**
- **High output current: $I_o = 500mA$ max**
- **10 SIP H/S package**
- **Internal phase compensated**

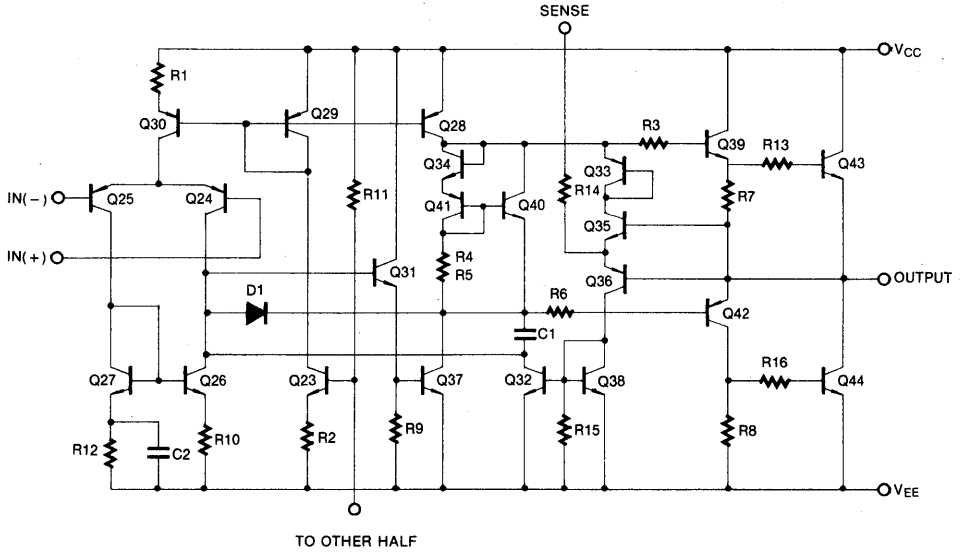
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KA9256	10 SIP H/S	−20 ~ +70°C

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_S	±18	V
Output Current	I_o	1.0	A
Power Dissipation	P_D	12.5	W
Operating Temperature Range	T_{opr}	−20 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

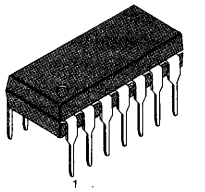
(V_{CC} = +15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}			2	6	mV
Input Offset Current	I_{IO}			10	200	nA
Input Bias Current	I_{IB}			100	700	nA
Supply Current	I_S			10	20	mA
Output Voltage Swing	V_{OUT}	R_L = 33Ω	±12	±13		V
Large Signal Voltage Gain	A_V			100		dB
Input Voltage Range	V_{ICR}		±12	±14		V
Common Mode Rejection Ratio	CMRR		70	90		dB
Power Supply Rejection Ratio	PSRR			50	150	μV/V
Bandwidth	BW			1.0		MHz
Slew Rate	SR	A_V = 1, R_L = 33Ω, R = 10Ω, C = 0.1μF		0.15		V/μs
Limiting Current	I_{OS}	R_{SC} = 2.2Ω		0.35		A
Cross Talk	CT	R_L = 33Ω, V_o = $1V_{p-p}$		60		dB

QUAD JFET INPUT OPERATIONAL AMPLIFIERS

The KF347 is a high speed quad JFET input operational amplifiers. This feature high impedance, wide bandwidth, high slew rate, and low input offset and bias currents. The KF347 may be used in circuits requiring high input impedance, high slew rate and wide bandwidth, low input bias current.

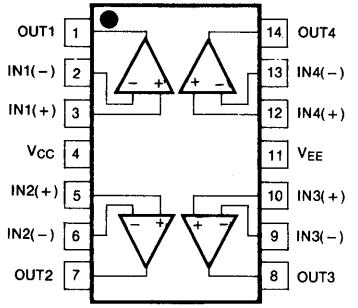
14 DIP



FEATURES

- **Low input bias**
- **High input impedance**
- **Wide bandwidth: 4 MHz (Typ)**
- **High slew rate: 13 V/μs (Typ)**

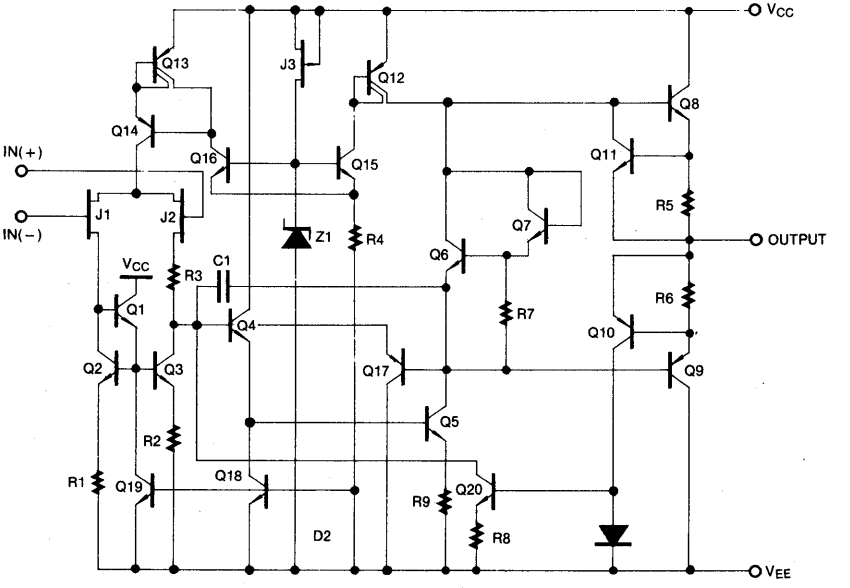
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KF347CN KF347ACN	14 DIP	0 ~ +70°C
KF347IN KF347AIN		−25 ~ +85°C

SCHEMATIC DIAGRAM (One Section Only)



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply Voltage	V_S	±18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range	V_I	±15	V
Output Short Circuit Duration		Continuous	
Power Dissipation	P_D	570	mV
Operating Temperature Range KF347C/AC	T_{opr}	0 ~ +70	°C
KF347I/AI		−25 ~ +85	
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = ±15V, V_{EE} = ±15V, Ta = 25°C, unless otherwise specified)

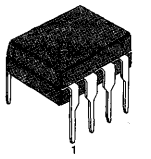
Characteristic	Symbol	Test Conditions		KF347AC/AI			KF347C/I			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	R_S = 10KΩ			3	5		5	10	mV
			NOTE1			7			13	
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$	R_S = 10KΩ			10				10	μV/°C
Input Offset Current	I_{IO}				25	100		25	100	pA
			NOTE1			4			4	
Input Bias Current	I_{IB}				50	200		50	200	pA
			NOTE1			8			8	
Large Signal Voltage Gain	A_V	R_L = 2KΩ, V_O = ±10V		50	100		25	100		V/mV
			NOTE1	15			15			
Output Voltage Swing	V_{OUT}	R_S = 10KΩ		±12	±13.5		±12	±13.5		V
Input Voltage Range	V_{ICR}			±11	+15 −12		±11	+15 −12		V
Common-Mode Rejection Ratio	CMRR	$R_S \leq$ 10KΩ		80	100		80	100		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq$ 10KΩ		80	100		80	100		dB
Input Resistance	R_I				10^{12}		10^{12}			Ω
Supply Current	I_S				7.2	11		7.2	11	mA
Slew Rate	SR				13		13			V/μs
Gain Bandwidth Product	GBW				4		4			MHz

NOTE 1. KF347C/AC: $0 \leq Ta \leq +70°C$
2. KF347I/AI: $-25 \leq Ta \leq +85°C$

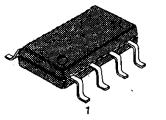
SINGLE OPERATIONAL AMPLIFIER

The KF351 is JFET input operational amplifier with an internally compensated input offset voltage. The JFET input device provides wide bandwidth, low input bias currents and offset currents.

8 DIP



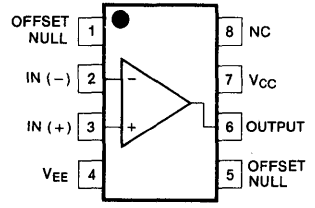
8 SOP



FEATURES

- **Internally trimmed offset voltage: 10mV**
- **Low input bias current: 50pA**
- **Wide gain bandwidth: 4MHz**
- **High slew rate: 13V/μs**
- **Low supply current: 1.8mA**
- **High input impedance: $10^{12}\Omega$**

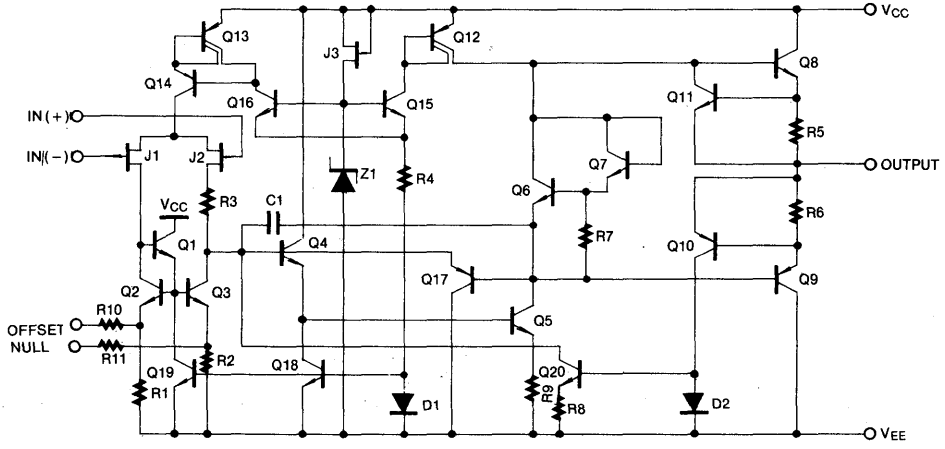
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KF351N	8 DIP	0 ~ +70°C
KF351D	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply Voltage	V_S	±18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range	V_I	±15	V
Output Short Circuit Duration		Continuous	
Power Dissipation	P_D	500	mV
Operating Temperature Range	T_{opr}	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

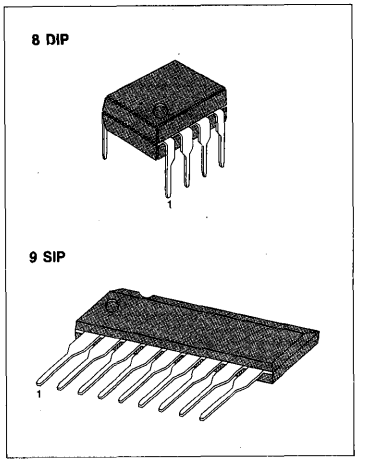
ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	R_S = 10K			5.0	10	mV
			0°C≤Ta≤+70°C			13	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	R_S = 10K	0°C≤Ta≤+70°C		10		μV/°C
Input Offset Current	I_{IO}				25	100	pA
			0°C≤Ta≤+70°C			4	nA
Input Bias Current	I_{IB}				50	200	pA
			0°C≤Ta≤+70°C			8	nA
Input Resistance	R_i				10^{12}		Ω
Large Signal Voltage Gain	A_V	V_O = ±10V, R_L = 2KΩ		25	100		V/mV
			0≤Ta≤+70°C	15			
Output Voltage Swing	V_{OUT}	R_L = 10KΩ		±12	±13.5		V
Input Voltage Range	V_{ICR}			±11	±15		V
Common Mode Rejection Ratio	CMRR	R_S≤10KΩ		70	100		dB
Power Supply Rejection Ratio	PSRR	R_S≤10KΩ		70	100		dB
Power Supply Current	I_S				2.3	3.4	mA
Slew Rate	SR	A_V = 1			13		V/μs
Gain-Bandwidth Product	GBW				4		MHz

DUAL JFET INPUT OPERATIONAL AMPLIFIERS

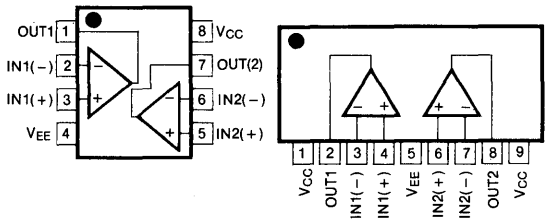
The LF442 is dual low power operational amplifiers. The key feature of this op amp are low power, low input offset voltage, high slew rate, high gain bandwidth.



FEATURES

- **Low supply current: 400μA MAX**
- **Low input bias current: 50pA MAX**
- **Low input offset voltage: 1mV MAX**
- **High slew rate: 1V/μs**
- **High gain bandwidth: 1MHz**

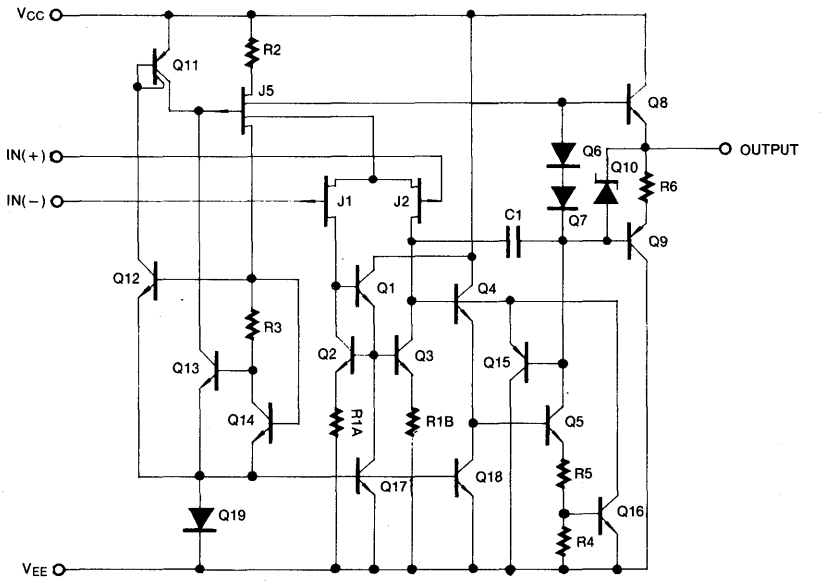
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KF442CN KF442ACN	8 DIP	0 ~ +70°C
KF442CS KF442ACS	9 SIP	
KF442IN KF442AIN	8 DIP	−25 ~ +85°C
KF442CS KF442ACS	9 SIP	

SCHEMATIC DIAGRAM (One Section Only)



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply Voltage	V_S	±18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range	V_I	±15	V
Output Short Circuit Duration		Continuous	
Power Dissipation	P_D		mV
Operating Temperature Range KF442C/AC KF442I/AI	T_{opr}	0 ~ +70 −25 ~ +85	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = ±15V, V_{EE} = ±15V, Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KF442AC/AI			KF442C/I			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	R_S = 10KΩ		0.5	1.0		1.0	5.0	mV
		NOTE1						7.5	
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$	R_S = 10KΩ		7	10		7		μV/°C
Input Offset Current	I_{IO}			5	25		5	50	pA
		NOTE1			10			10	nA
Input Bias Current	I_{IB}			10	50		10	100	pA
		NOTE1			20			20	nA
Large Signal Voltage Gain	A_V	R_L = 10KΩ	50	200		25	200		V/mV
		V_O = ±10V NOTE1	25	200		15	200		
Output Voltage Swing	V_{OUT}	R_S = 10KΩ	±12	±13		±12	±13		V
Input Voltage Range	V_{ICR}		±16	+18 −17		±11	+14 −12		V
Common-Mode Rejection Ratio	CMRR	$R_S \leq$ 10KΩ	80	100		70	95		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq$ 10KΩ	80	100		70	90		dB
Input Resistance	R_I			10^{12}		10^{12}			
Supply Current	I_S			300	400		400	500	μA
Slew Rate	SR		0.8	1		0.6	1		V/μs
Gain Bandwidth Product	GBW		0.8	1		0.6	1		MHz

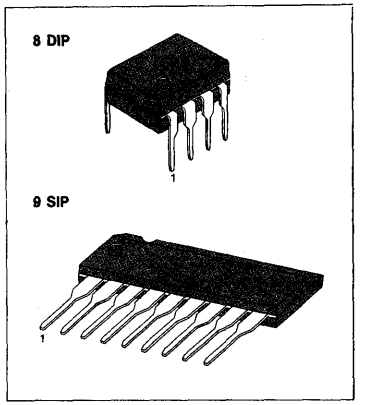
NOTE 1. KF442C/AC: $0 \leq Ta \leq +70°C$
2. KF442I/AI: $-25 \leq Ta \leq +85°C$

DUAL CMOS OPERATIONAL AMPLIFIER

KS272 is CMOS operational amplifier designed to operate with single or dual supplies.

This device has extremely high input impedance, low input bias and offset current.

Application areas include transducer amplifier, amplifier blocks, active filters, signal buffers, and all the conventional OP Amp circuits which can be easily implemented in single power supply systems.

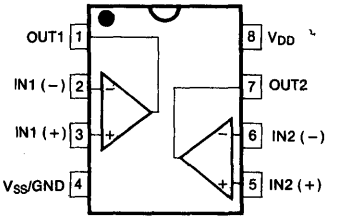


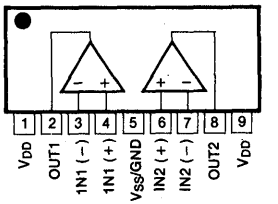
FEATURES

- **Wide operating voltage range; 3V to 18V or or ±1.5V to ±8V**
- **High input impedance: $10^{12}\Omega$**
- **Very low input bias current**
- **Common-mode input voltage range includes the negative rail**
- **Single-supply voltage operation.**

Device	Package	Operating Temperature
KS272CN	8 DIP	0 ~ $70°C
KS272ACN		
KS272CS	9 SIP	
KS272ACS		
KS272IN	8 DIP	−25 ~ +85°C
KS272AIN		
KS272IS	9 SIP	
KS272AIS		

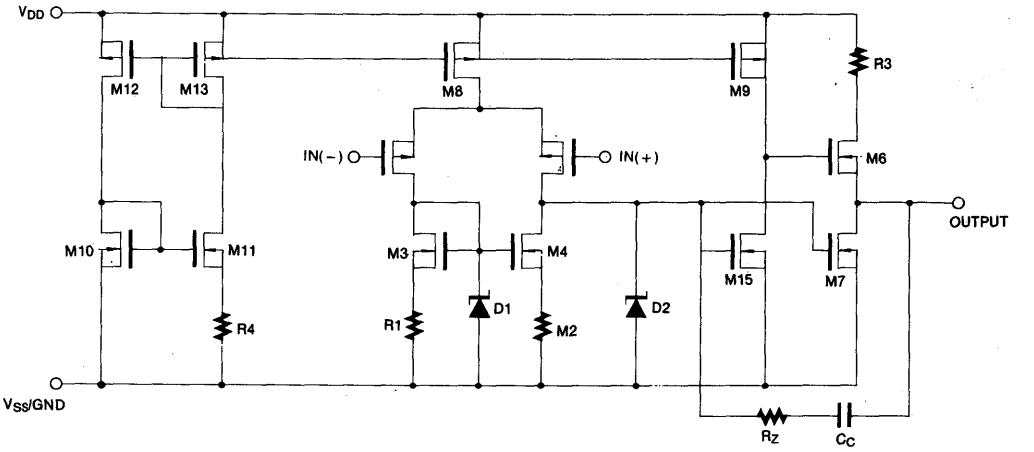
BLOCK DIAGRAM





SCHEMATIC DIAGRAM

(one section only)



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	18	V
Differential Input Voltage	V_{ID}	18	V
Input Voltage	V_I	−0.3 ~ +18	V
Duration of Short Circuit (Note 1)		unlimited	
Power Dissipation	P_D	500	mW
Operating Temperature Range KS272C/AC	T_{opr}	0 ~ +70	°C
KS272I/AI		−25 ~ +85	
Storage Temperature	T_{stg}	−65 ~ +150	°C

(Note 1) The output may be shorted to ground or either supply, for $V_{DD} \leq 14V$. Care must be taken to insure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

($V_{DD} = 10V$, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KS272C/KS2721 Min	KS272C/KS2721 Typ	KS272C/KS2721 Max	KS272AC/KS272AI Min	KS272AC/KS272AI Typ	KS272AC/KS272AI Max	Unit
Input Offset Voltage	V_{IO}	$V_O = 1.4V$			10			5	mV
		$R_S = 50\Omega$ NOTE2			12			12	
Input Offset Current	I_{IO}	$V_{IC} = 5V$		1			1		pA
		$V_O = 5V$ NOTE2			100			100	
Input Bias Current	I_{IB}	$V_{IC} = 5V$		1			1		pA
		$V_O = 5V$ NOTE2			150			150	
Common-Mode Input Voltage Range	V_{ICR}		−0.2 to 9			−0.2 to 9			V
Output Voltage Swing	V_{OUT}	$V_{ID} = 100mV$	8	8.6		8	8.6		V
		NOTE2	7.8			7.8			
Large Signal Voltage Gain	A_V	$V_O = 1$ to $6V$	80	92		80	92		dB
		$R_S = 50\Omega$ NOTE2	77.5			77.5			
Common-Mode Rejection Ratio	CMRR	$V_O = 1.4V$, $V_{IC} = V_{ICR}$ min	70	88		70	88		dB
Power Supply Rejection Ratio	PSRR	$V_{DD} = 5$ to $10V$, $V_O = 1.4V$	65	82		65	82		dB
Output Current	I_{source}	$V_O = 0V$, $V_{ID} = 100mV$		−55			−55		mA
	I_{sink}	$V_O = V_{DD}$, $V_{ID} = -100mV$		15			15		
Supply Current (each amplifier)	I_{DD}	No load, $V_{IC} = 5V$		1	2		1	2	mA
		$V_O = 5V$ NOTE2			2.2			2.2	
Unity Gain Bandwidth	BW	$A_V = 40dB$, $C_L = 10pF$, $R_S = 50\Omega$		4.5			4.5		MHz
Slew Rate	SR	Unity Gain, $R_L \geq 2K\Omega$, $C_L = 100pF$		2.3			2.3		V/μs
Channel Seperation	CS	$A_V = 100$		120			120		dB

NOTE 1. KS272C/AC: $0 \leq Ta \leq +70°C$
2. KS272I/AI: $-25 \leq Ta \leq +85°C$

TYPICAL APPLICATION INFORMATION

Latch Up Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure that can function as an SCR, and under certain conditions may be triggered into a low impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3V beyond the supply rails may be applied any pin. In general, the OP amp supplies should be established simultaneously with, or before any input signals are applied.

Output Stage Considerations

The amplifier's output stage consists of a source-follower connected pull up transistor and an open-drain pull-down transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

Circuit Layout Precaustions

The user is caustioned that, due to extremely high input impedance, care must be exercised in layout, construction board cleanliness, and supply filtering to avoid hum and noise pick up.

TYPICAL APPLICATIONS

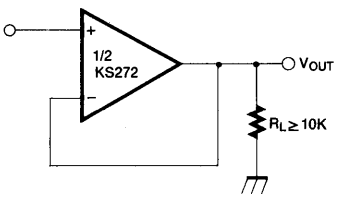


Fig. 1

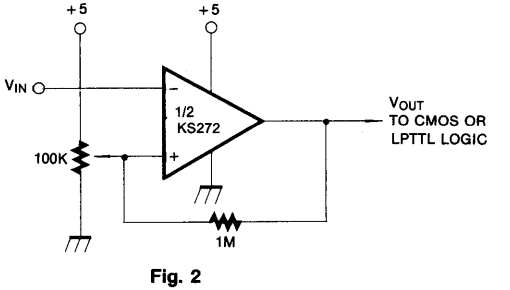


Fig. 2

AC Coupled Non-Inverting Amplifier

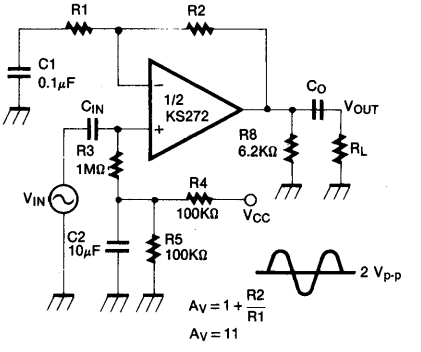


Fig. 3

Pulse Generator

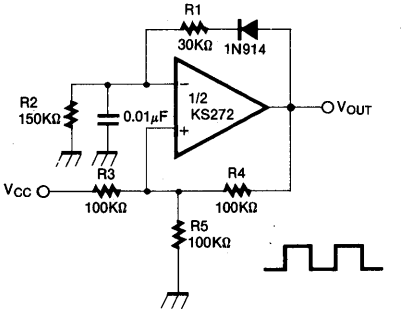


Fig. 4

TYPICAL APPLICATION

Bi-Quad Filter

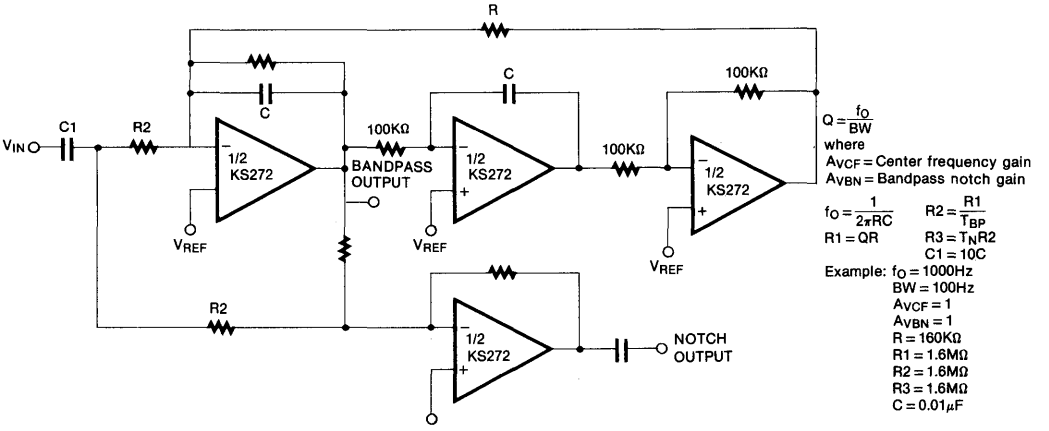


Fig. 5

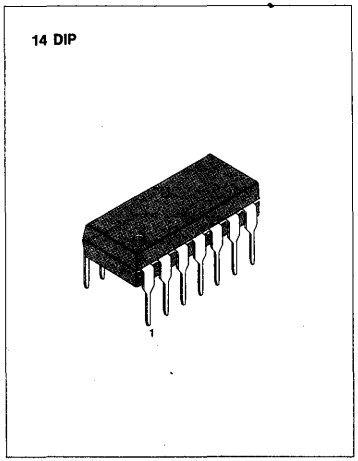
4

QUAD CMOS OPERATIONAL AMPLIFIER

KS274 is CMOS operational amplifier designed to operate with single or dual supplies.

This device has extremely high input impedance, low input bias and offset current.

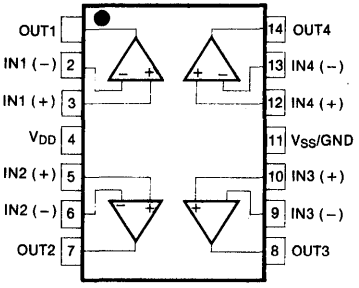
Application areas include translucer amplifier, amplifier blocks, active filters, signal buffers, and all the conventional OP Amp circuits which can be easily implemented in single power supply systems.



FEATURES

- **Wide operating voltage range; 3V to 16V or or ±1.5V to ±8V**
- **High input impedance: $10^{12}\Omega$**
- **Very low input bias current**
- **Common-mode input voltage range includes the negative rail**
- **Single-supply voltage operation.**

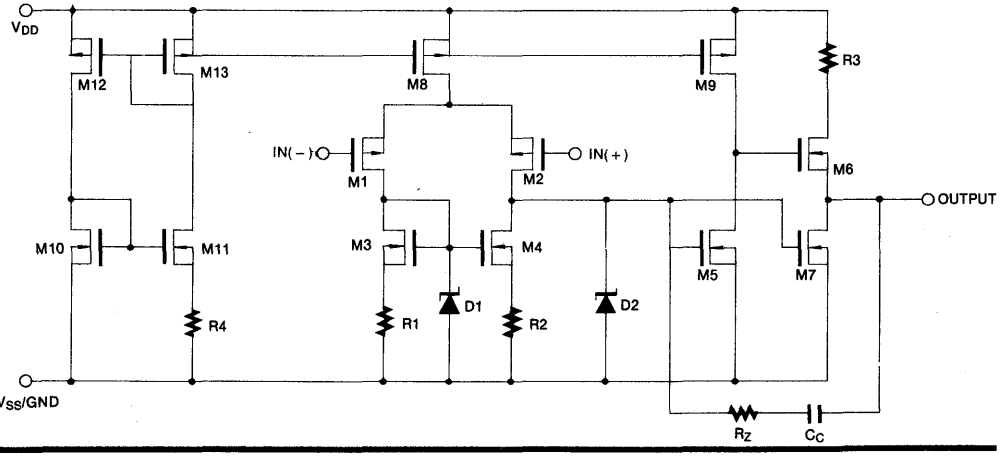
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KS274CN	14 DIP	0 ~ +70°C
KS274ACN		
KS274IN	14 DIP	−25 ~ +85°C
KS274AIN		

SCHEMATIC DIAGRAM (One Section Only)



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	18	V
Differential Input Voltage	V_{ID}	18	V
Input Voltage	V_I	−0.3 ~ +18	V
Duration of Short Circuit (Note 1)		unlimited	
Power Dissipation	P_D	570	mW
Operating Temperature Range KS274C/AC	T_{opr}	0 ~ +70	°C
KS274I/AI		−25 ~ +85	
Storage Temperature	T_{stg}	−65 ~ +150	°C

(Note 1) The output may be shorted to ground or either supply, for $V_{DD} \leq 14V$. Care must be taken to insure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

($V_{DD} = 10V$, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KS274C/KS2741 Min	KS274C/KS2741 Typ	KS274C/KS2741 Max	KS274AC/KS274AI Min	KS274AC/KS274AI Typ	KS274AC/KS274AI Max	Unit
Input Offset Voltage	V_{IO}	$V_O = 1.4V$			10			5	mV
		$R_S = 50\Omega$ NOTE2			12			12	
Input Offset Current	I_{IO}	$V_{IC} = 5V$		1			1		pA
		$V_O = 5V$ NOTE2			100			100	
Input Bias Current	I_{IB}	$V_{IC} = 5V$		1			1		pA
		$V_O = 5V$ NOTE2			150			150	
Common-Mode Input Voltage Range	V_{ICR}		−0.2 to 9			−0.2 to 9			V
Output Voltage Swing	V_{OUT}	$V_{ID} = 100mV$	8	8.6		8	8.6		V
		NOTE2	7.8			7.8			
Large Signal Voltage Gain	A_V	$V_O = 1$ to 6V	80	92		80	92		dB
		$R_S = 50\Omega$ NOTE2	77.5			77.5			
Common-Mode Rejection Ratio	CMRR	$V_O = 1.4V$, $V_{IC} = V_{ICR}$ min	70	88		70	88		dB
Power Supply Rejection Ratio	PSRR	$V_{DD} = 5$ to 10V, $V_O = 1.4V$	65	82		65	82		dB
Output Current	I_{source}	$V_O = 0V$, $V_{ID} = 100mV$		−55			−55		mA
	I_{sink}	$V_O = V_{DD}$, $V_{ID} = -100mV$		15			15		
Supply Current (each amplifier)	I_{DD}	No load, $V_{IC} = 5V$		1	2		1	2	mA
		$V_O = 5V$ NOTE2			2.2			2.2	
Unity Gain Bandwidth	BW	$A_V = 40dB$, $C_L = 10pF$, $R_S = 50\Omega$		2.3			2.3		MHz
Slew Rate	SR	Unity Gain, $R_L \geq 2K\Omega$, $C_L = 100pF$		4.5			4.5		V/μs
Channel Seperation	CS	$A_V = 100$		120			120		dB

NOTE 1. KS274C/AC: $0 \leq Ta \leq +70°C$
2. KS274I/AI: $-25 \leq Ta \leq +85°C$

TYPICAL APPLICATION INFORMATION

Latch Up Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure that can function as an SCR, and under certain conditions may be triggered into a low impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3V beyond the supply rails may be applied any pin. In general, the OP amp supplies should be established simultaneously with, or before any input signals are applied.

Output Stage Considerations

The amplifier's output stage consists of a source-follower connected pull up transistor and an open-drain pull-down transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

Circuit Layout Precautions

The user is cautioned that, due to extremely high input impedance, care must be exercised in layout, construction board cleanliness, and supply filtering to avoid hum and noise pick up.

TYPICAL APPLICATIONS

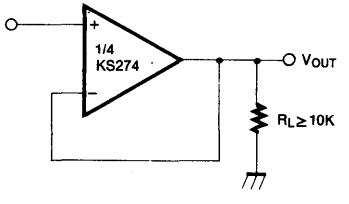


Fig. 1

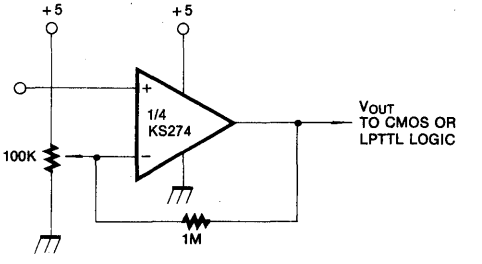


Fig. 2

AC Coupled Non-Inverting Amplifier

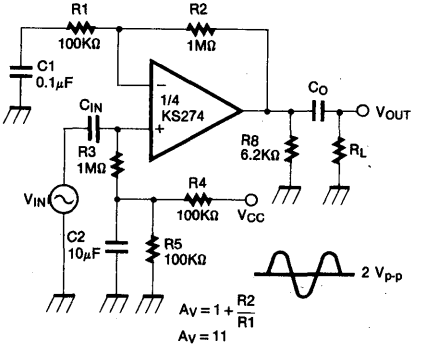


Fig. 3

Pulse Generator

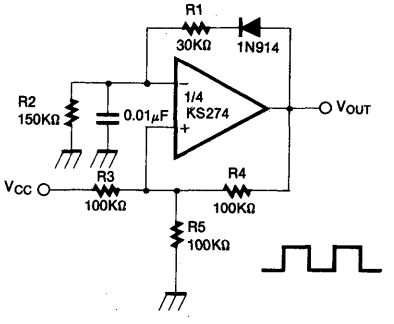


Fig. 4

TYPICAL APPLICATION INFORMATION

Bi-Quad Filter

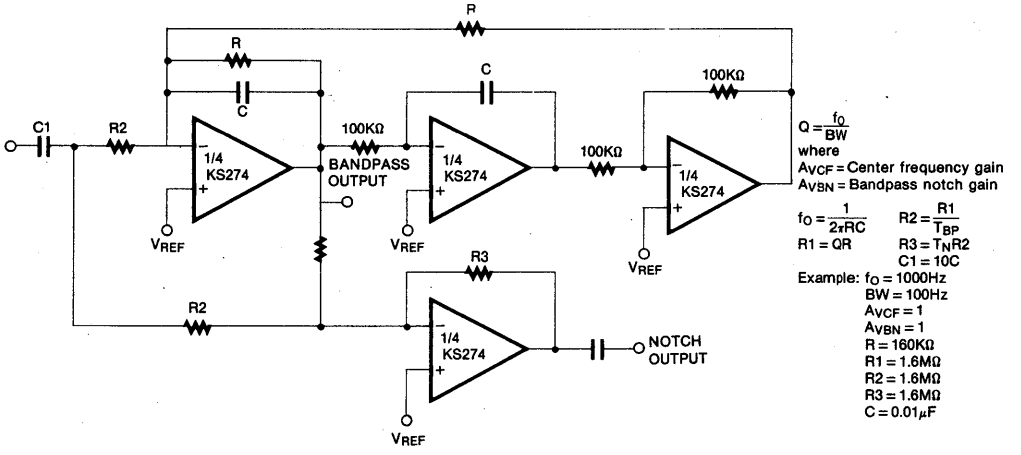


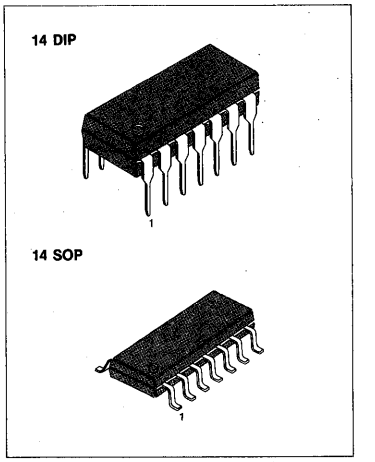
Fig. 5

QUAD OPERATIONAL AMPLIFIERS

The LM224 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage.

Operation from split power supplies is also possible so long as the difference between the two supplies is 3 volts to 32 volts.
voltage.

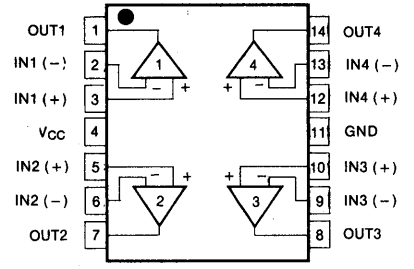
Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single power supply systems.



FEATURES

- **Internally frequency compensated for unity gain**
- **Large DC voltage gain: 100dB**
- **Wide power supply range: LM224/A, LM324/A: 3V ~ 32V (or ± 1.5V ~ 16V)**
  LM2902: 3V ~ 26V (or ± 1.5V ~ 13V)
- **Input common-mode voltage range includes ground**
- **Large output voltage swing: 0V DC to V_{CC}-1.5V DC**
- **Power drain suitable for battery operation.**

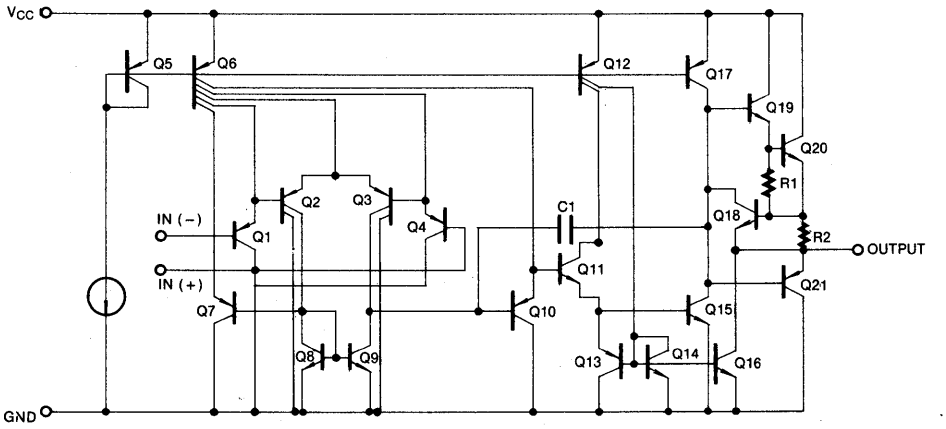
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
LM324N LM324AN	14 DIP	0 ~ + 70°C
LM324D LM324AD	14 SOP	
LM224N LM224AN	14 DIP	− 25 ~ + 85°C
LM224D LM224AD	14 SOP	
LM2902	14 DIP	− 40 ~ + 85°C
LM2902D	14 SOP	

SCHEMATIC DIAGRAM (One Section Only)



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	LM224/LM224A	LM324/LM324A	LM2902	Unit
Power Supply Voltage	V_S	± 18 or 32	± 18 or 32	± 13 or 26	V
Differential Input Voltage	V_{ID}	32	32	26	V
Input Voltage	V_I	−0.3 to +32	−0.3 to +32	−0.3 to +26	V
Output Short Circuit to GND $V_{CC} \leq 15V$ Ta = 25°C (One Amp)		Continuous	Continuous	Continuous	
Power Dissipation	P_D	570	570	570	mW
Operating Temperature Range	T_{opr}	−25 ~ +85	0 ~ +70	−40 ~ +85	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	−65 ~ +150	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM224			LM324			LM2902			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} − 1.5V, V_o = 1.4V, R_S = 0Ω		1.5	5.0		1.5	7.0		1.5	7.0	mV
Input Offset Current	I_{IO}			2.0	30		3.0	50		3.0	50	nA
Input Bias Current	I_{IB}			40	150		40	250		40	250	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V (V_{CC} = 26V for LM2902)	0		V_{CC} -1.5	0	V_{CC} -1.5		0		V_{CC} -1.5	V
Supply Current	I_{CC}	$R_L = \infty$, V_{CC} = 30V (all Amps) (V_{CC} = 26V for LM2902)		1.0	3		1.0	3		1.0	3	mA
		$R_L = \infty$, V_{CC} = 5V (all Amps)		0.7	1.2		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq 2K\Omega$, V_O = 1V to 11V	50	100		25	100			100		V/mV
Output Voltage Swing	V_{OH} V_{OL}	V_{CC} = 30V, R_L = 2KΩ	26			26			22			V
		V_{CC} = 26V for 2902, R_L = 10KΩ	27	28		27	28		23	24		V
		V_{CC} = 5V, $R_L \geq 10K\Omega$		5	20		5	20		5	100	mV
Common-Mode Rejection Ratio	CMRR		70	85		65	75		50	75		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		50	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120			120		dB
Short Circuit to GND	I_{OS}			40	60		40	60		40	60	mA
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V, V_{CC} = 15V, V_o = 2V	20	40		20	40		20	40		mA
	I_{sink}	V_{in+} = 0V, V_{in-} = 1V, V_{CC} = 15V, V_o = 2V	10	13		10	13		10	13		mA
		V_{in+} = 0V, V_{in-} = 1V, V_{CC} = 15V, V_o = 200mV	12	45		12	45					μA
Differential Input Voltage	V_{ID}				V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)
The following specification apply over the range of $-25°C \leq Ta \leq +85°C$ for the LM224; and the $0°C \leq Ta \leq +70°C$ for the LM324; and the $-40°C \leq Ta \leq +85°C$ for the LM2902

Characteristic	Symbol	Test Conditions		LM224			LM324			LM2902			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V V_O = 1.4V, R_S = 0Ω				7.0			9.0			10.0	mV
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$				7.0			7.0			7.0		μV/°C
Input Offset Current	I_{IO}					100			150			200	nA
Input Offset Current Drift	$\triangle I_{IO}/\triangle T$				10			10			10		pA/°C
Input Bias Current	I_{IB}					300			500			500	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V (V_{CC} = 26V for LM2902)		0		V_{CC} -2.0	0		V_{CC} -2.0	0		V_{CC} -2.0	V
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq 2.0K\Omega$ V_O = 1V to 11V		25			15			15			V/mV
Output Voltage Swing	V_{OH}	V_{CC} = 30V	$R_L = 2K\Omega$	26			26			22			V
		V_{CC} = 26V for 2902	$R_L = 10K\Omega$	27	28		27	28		23	24		V
	V_{OL}	V_{CC} = 5V, $R_L \geq 10K\Omega$			5	20		5	20		5	100	mV
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V V_{CC} = 15V, V_O = 2V		10	20		10	20		10	20		mA
	I_{sink}	V_{in+} = 0V, V_{in-} = 1V V_{CC} = 15V, V_O = 2V		10	13		5	8		5	8		mA
Differential Input Voltage	V_{ID}					V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM224A			LM324A			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V V_O = 1.4V, R_S = 0			1.0	3.0		1.5	3.0	mV
Input Offset Current	I_{IO}				2	15		3.0	30	nA
Input Bias Current	I_{IB}				40	80		40	100	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V		0		V_{CC} -1.5	0		V_{CC} -1.5	V
Supply Current (All Amps)	I_{CC}	R_L = , V_{CC} = 30V			1.5	3		1.5	3	mA
		R_L = , V_{CC} = 5V			0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq 2K\Omega$ V_O = 1V to 11V		50	100		25	100		V/mV
Output Voltage Swing	V_{OH}	V_{CC} = 30V	$R_L = 2K\Omega$	26			26			V
		V_{CC} = 26V for 2902	$R_L = 10K\Omega$	27	28		27	28		V
	V_{OL}	V_{CC} = 5V, $R_L \geq 10K\Omega$			5	20		5	20	mV
Common-Mode Rejection Ratio	CMRR			70	85		65	85		dB
Power Supply Rejection Ratio	PSRR			65	100		65	100		dB
Channel Separation	CS	f = 1KHz to 20KHz			120			120		dB
Short Circuit to GND	I_{OS}				40	60		40	60	mA
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V V_{CC} = 15V		20	40		20	40		mA
	I_{sink}	V_{in+} = 0V, V_{in-} = 1V V_{CC} = 15V, V_O = 2V		10	20		10	20		mA
		V_{in+} = 0V, V_{in-} = 1V V_{CC} = 15V, V_O = 200mV		12	50		12	50		μA
Differential Input Voltage	V_{ID}					V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)
The following specification apply over the range of $-25°C \leq Ta \leq +85°C$ for the LM224A; and the $0°C \leq Ta \leq +70°C$ for the LM324A

Characteristic	Symbol	Test Conditions	LM224A			LM324A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V V_O = 1.4V R_S = 0Ω			4.0			5.0	mV
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$			7.0	20		7.0	30	μV/°C
Input Offset Current	I_{IO}				30			75	nA
Input Offset Current Drift	$\triangle I_{IO}/\triangle T$			10	200		10	300	pA/°C
Input Bias Current	I_{IB}			40	100		40	200	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V	0		V_{CC} -2.0	0		V_{CC} -2.0	V
Large Signal Voltage Gain	A_V	V_{CC} = 15V $R_L \geq 2.0K\Omega$	25			15			V/mV
Output Voltage Swing	V_{OH} V_{OL}	V_{CC} = 30V R_L = 2KΩ	26			26			V
		R_L = 10KΩ	27	28		27	28		
		V_{CC} = 5V $R_L \leq 10K\Omega$		5	20		5	20	mV
Output Current	I_{source}	V_{in+} = 1V V_{in-} = 0V V_{CC} = 15V	10	20		10	20		mA
	I_{sink}	V_{in+} = 0V V_{in-} = 1V V_{CC} = 15V	5	8		5	8		mA
Differential Input Voltage	V_{ID}				V_{CC}			V_{CC}	V

APPLICATION NOTE

The LM224 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger the V_{CC} without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3V_{DC}$ (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case noninverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

The bias network of the LM224 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V_{CC}/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Fig. 1 INPUT VOLTAGE RANGE

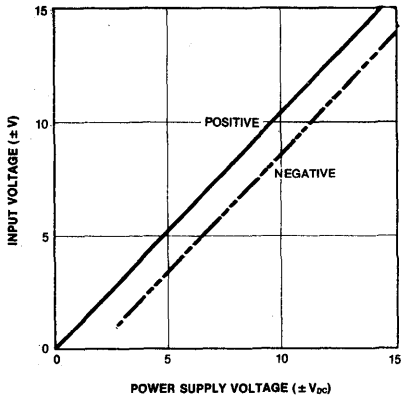


Fig. 2 INPUT CURRENT

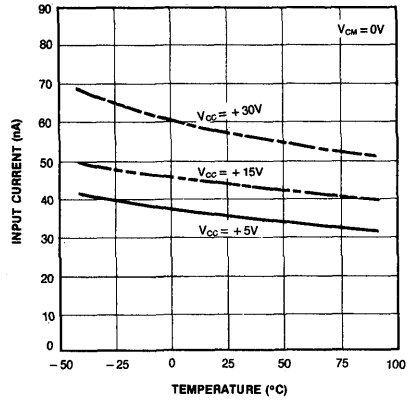


Fig. 3 SUPPLY CURRENT

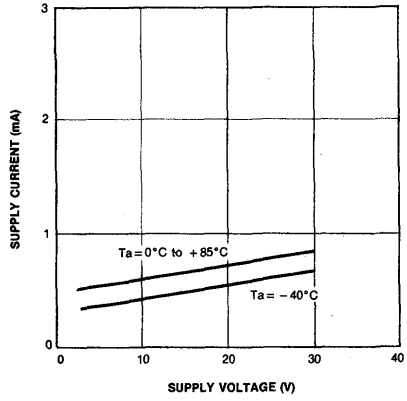


Fig. 4 VOLTAGE GAIN

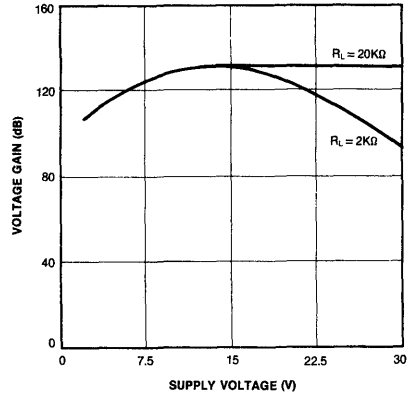


Fig. 5 OPEN LOOP FREQUENCY RESPONSE

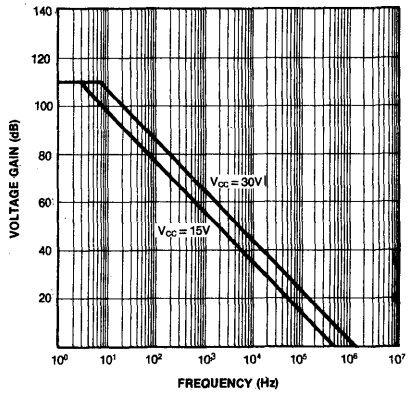
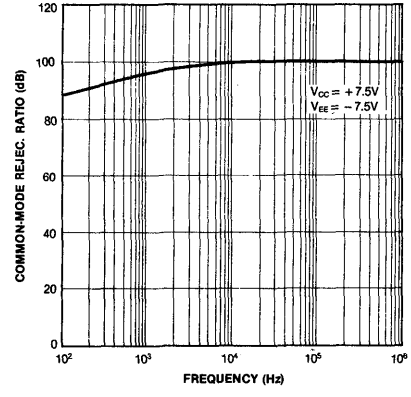


Fig. 6 COMMON-MODE REJECTION RATIO



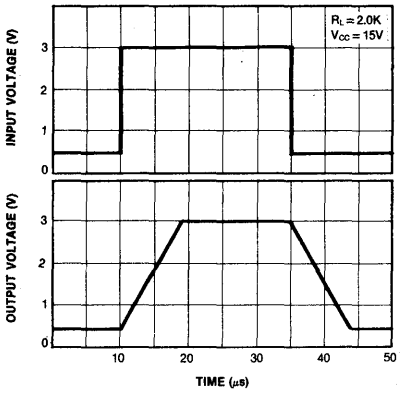


Fig. 9 LARGE SIGNAL FREQUENCY RESPONSE

Fig. 8 VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

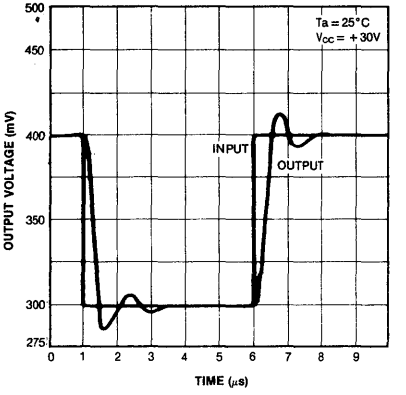


Fig. 10 OUTPUT CHARACTERISTICS CURRENT SOURCING

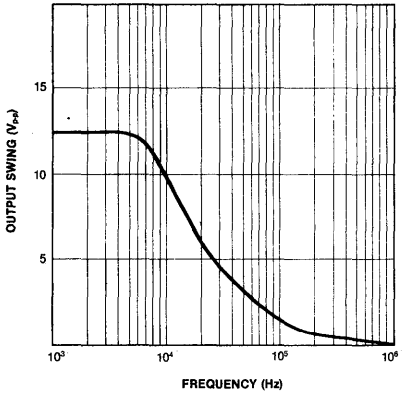


Fig. 11 OUTPUT CHARACTERISTICS CURRENT SINKING

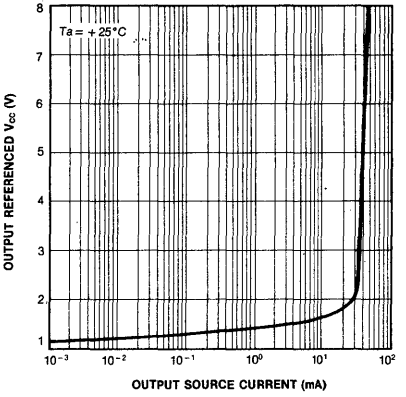
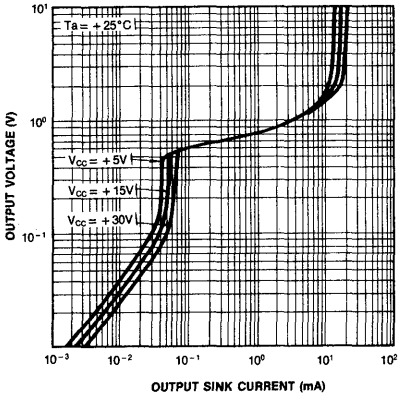
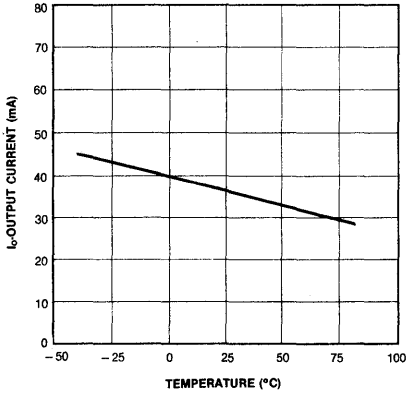


Fig. 12 CURRENT LIMITING





TYPICAL APPLICATIONS (V_{CC} = 5.0V)

Fig. 13 Voltage Reference

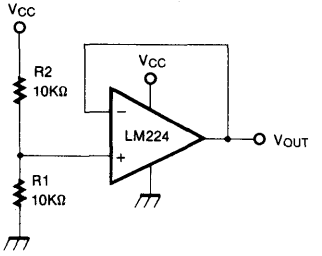


Fig. 14 Non-Inverting DC Gain

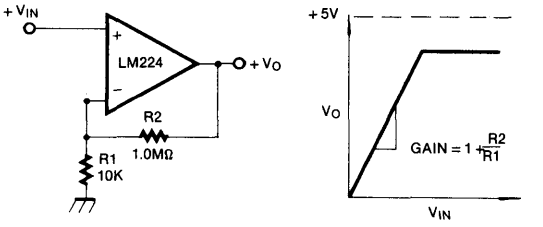


Fig. 15 AC Coupled Non-Inverting Amplifier

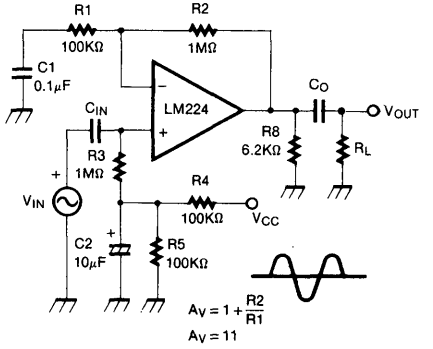


Fig. 16 Pulse Generator

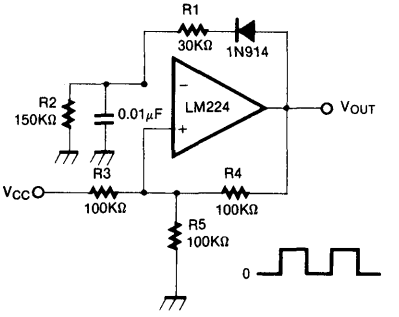
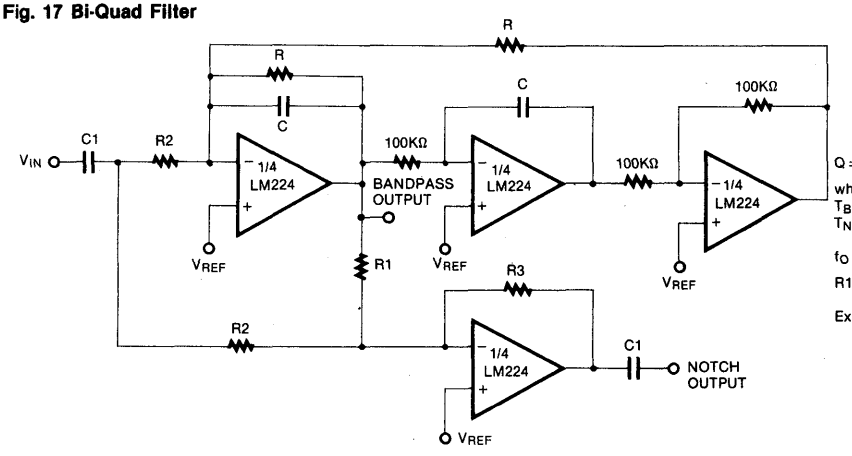


Fig. 17 Bi-Quad Filter



$Q = \frac{BW}{f_O}$

where

T_{BP} = Center frequency gain

T_N = Bandpass notch gain

$f_O = \frac{1}{2\pi RC}$ $R2 = \frac{R1}{T_{BP}}$

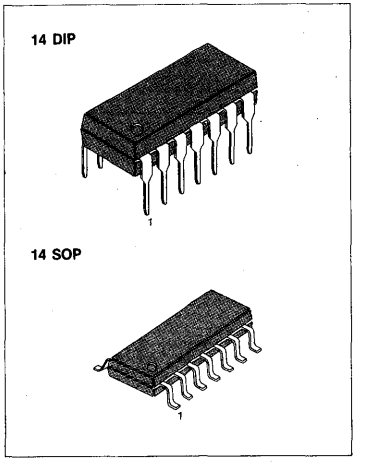
$R1 = QR$ $R3 = T_N R2$

$C1 = 10C$

Example: f_O = 1000Hz
BW = 100Hz
T_{BP} = 1
T_N = 1
R = 160KΩ
R1 = 1.6MΩ
R2 = 1.6MΩ
R3 = 1.6MΩ
C = 0.01μF

QUAD OPERATIONAL AMPLIFIERS

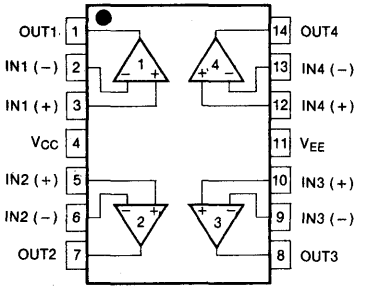
The LM248/LM348 is a true quad LM741. It consists of four independent, high-gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar LM741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single LM741 type OP Amp. Other features include input offset currents and input bias current which are much less than those of a standard LM741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.



FEATURES

- **LM741 OP Amp operating characteristics**
- **Low supply current drain**
- **Class AB output stage-no crossover distortion**
- **Pin compatible with the LM324 & MC3403**
- **Low input offset voltage-1mV Typ.**
- **Low input offset current-4nA Typ.**
- **Low input bias current-30nA Typ.**
- **Gain bandwidth product for LM348 (unity gain)-1.0MHz Typ.**
- **High degree of isolation between amplifiers-120dB**
- **Overload protection for inputs and outputs**

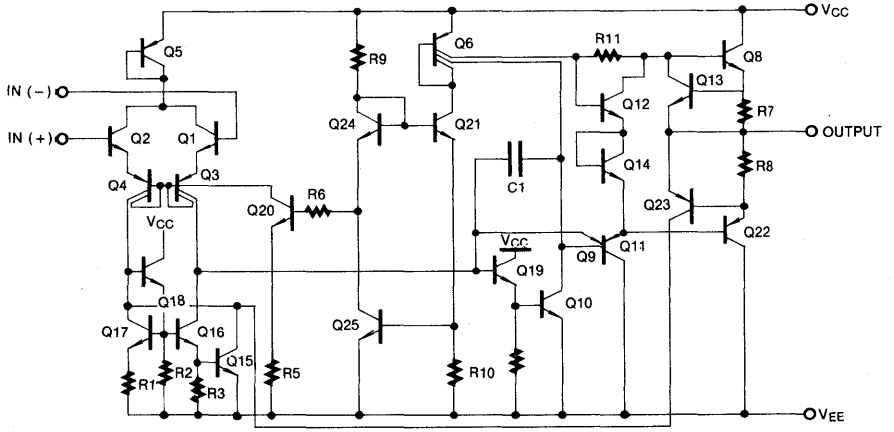
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
LM348N	14 DIP	0 ~ +70°C
LM348D	14 SOP	
LM248N	14 DIP	−25 ~ +85°C
LM248D	14 SOP	

SCHEMATIC DIAGRAM (One Section Only)



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_S	± 18	V
Differential Input Voltage	V_{ID}	± 36	V
Input Voltage	V_I	± 18	V
Output Short Circuit Duration		Continuous	
Operating Temperature LM248	T_{opr}	− 25 ~ + 85	°C
LM348		0 ~ + 70	°C
Storage Temperature	T_{stg}	− 65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15V, V_{EE} = − 15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM248			LM348			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 10K\Omega$			1	6.0		1	6.0	mV
			NOTE 1			7.5			7.5	
Input Offset Current	I_{IO}				4	50		4	50	nA
			NOTE 1			125			100	
Input Bias Current	I_{IB}				30	200		30	200	nA
			NOTE 1			500			400	
Input Resistance	R_i			0.8	2.5		0.8	2.5		MΩ
Supply Current (all Amplifiers)	I_S				2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	A_V	$R_L \geq 2K\Omega$		25	160		25	160		V/mV
			NOTE 1	15			15			
Channel Separation	CS	f = 1KHz to 20KHz			120			120		dB
Common Mode Input Voltage Range	V_{ICR}	NOTE 1		± 12			± 12			V
Small Signal Bandwidth	BW	$A_V = 1$			1.0			1.0		MHz
Phase Margin	ϕ_m	$A_V = 1$			60			60		Degrees
Slew Rate	SR	$A_V = 1$			0.5			0.5		V/μs
Output Short Circuit Current	I_{OS}				25			25		mA
Output Voltage Swing	V_{OUT}	$R_L \geq 10K\Omega$	NOTE 1	± 12	± 13		± 12	± 13		V
		$R_L \geq 2K\Omega$		± 10	± 12		± 10	± 12		
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K$	NOTE 1	70	90		70	90		dB
Supply Voltage Rejection Ratio	PSRR	$R_S \leq 10K$	NOTE 1	77	96		77	96		dB

* NOTE 1
LM348: $0 \leq T_a \leq +70°C$
LM248: $-25 \leq T_a \leq +85°C$

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

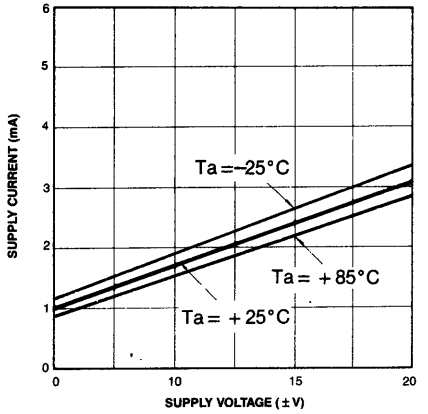


Fig. 2 VOLTAGE SWING

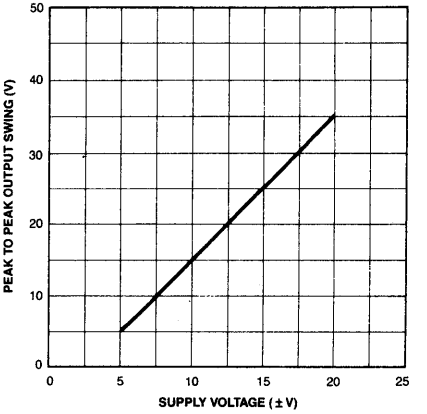


Fig. 3 SOURCE CURRENT LIMIT

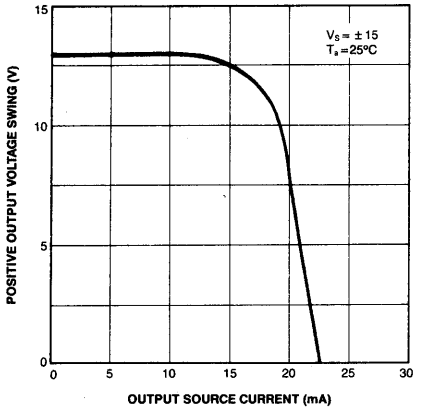


Fig. 4 SINK CURRENT LIMIT

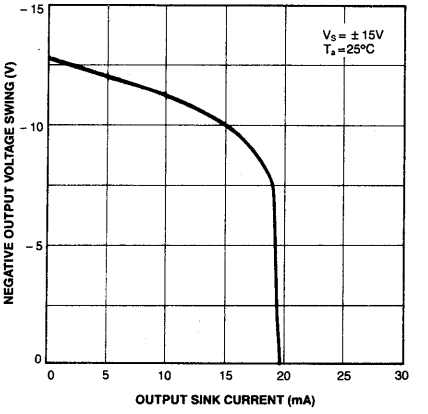


Fig. 5 OUTPUT IMPEDANCE

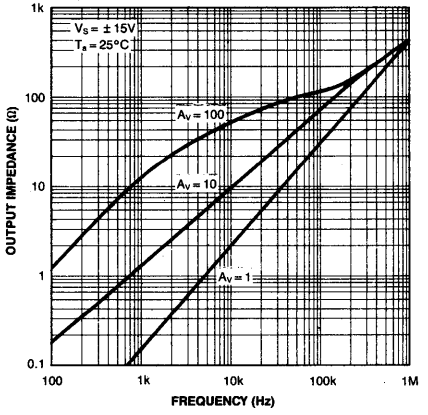
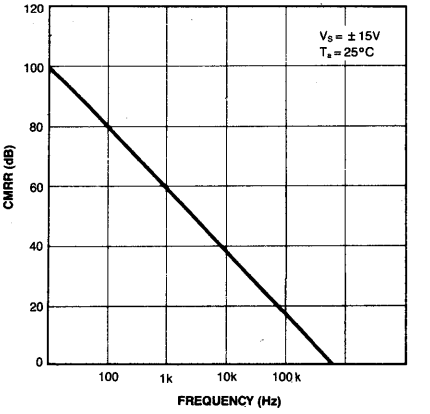


Fig. 6 COMMON-MODE REJECTION RATIO



4

Fig. 7 OPEN LOOP FREQUENCY RESPONSE

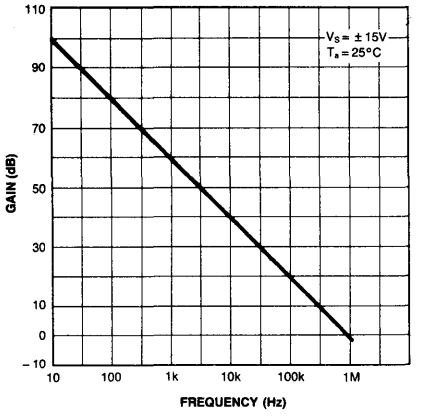


Fig. 8 BODE PLOT

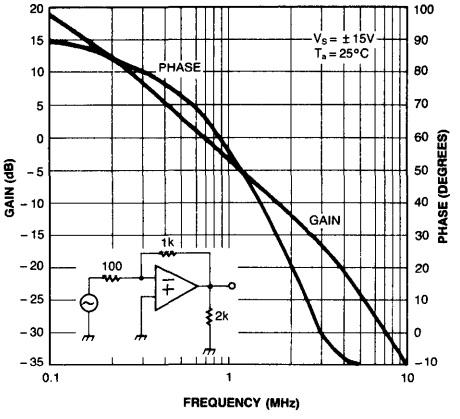


Fig. 9 LARGE SIGNAL PULSE RESPONSE

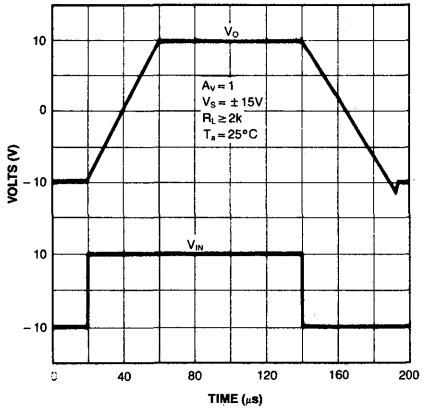


Fig. 10 SMALL SIGNAL PULSE RESPONSE

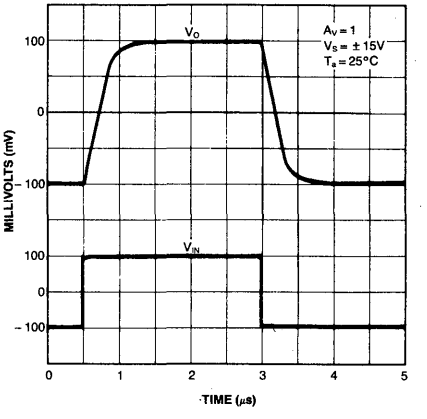


Fig. 11 UNDISTORTED OUTPUT VOLTAGE SWING

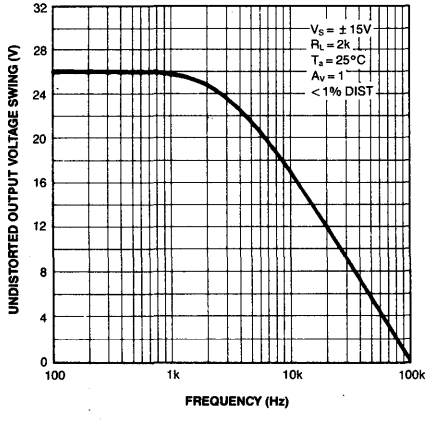


Fig. 12 INVERTING LARGE SIGNAL PULSE RESPONSE

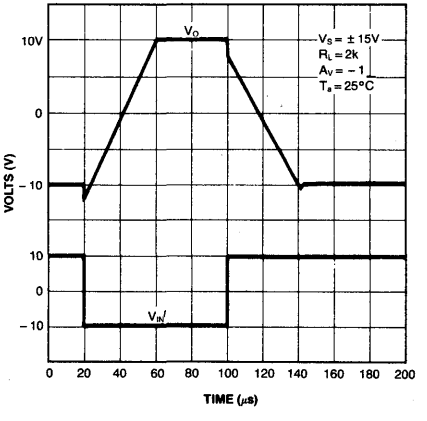


Fig. 13 INPUT NOISE VOLTAGE AND NOISE CURRENT

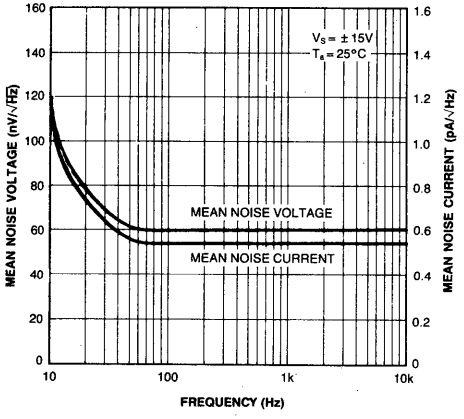


Fig. 14 POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT

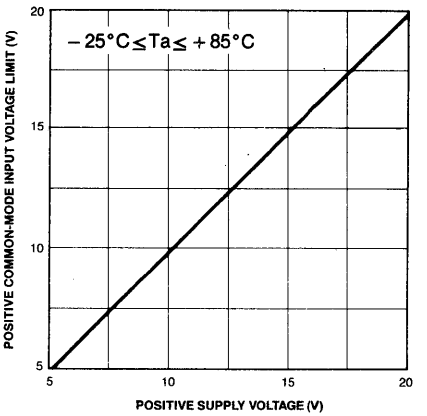
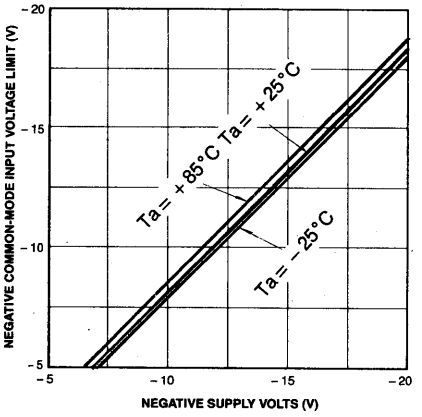


Fig. 15 NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT



4

TYPICAL APPLICATIONS

Fig. 16 Function Generator

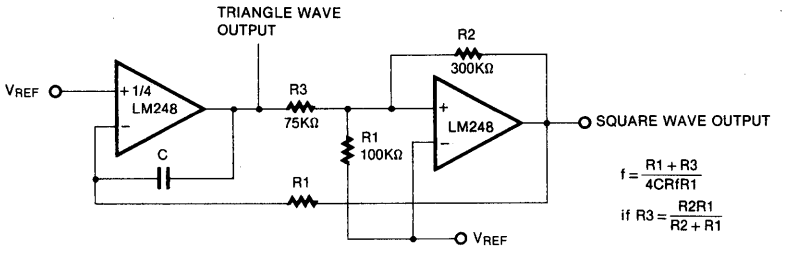


Fig. 16

Fig. 17 Bi-Quad Filter

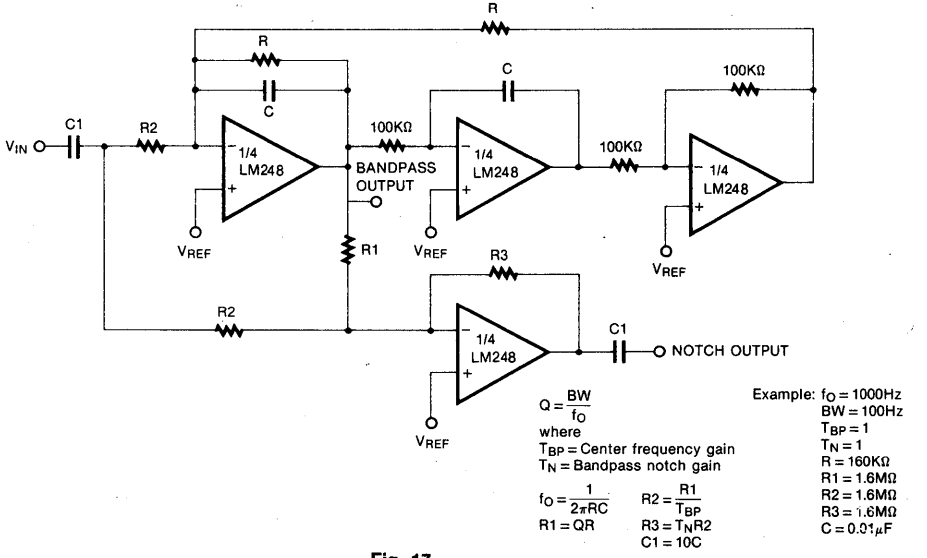


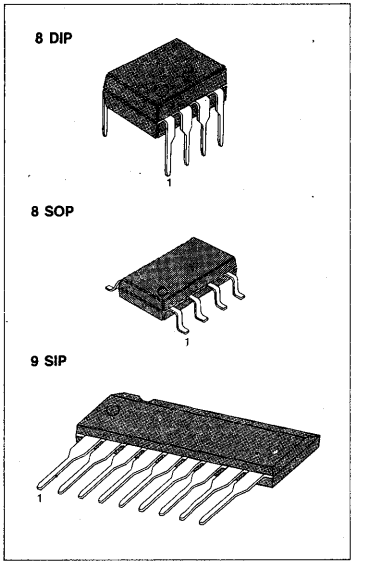
Fig. 17

DUAL OPERATIONAL AMPLIFIERS

The LM258 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage.

Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

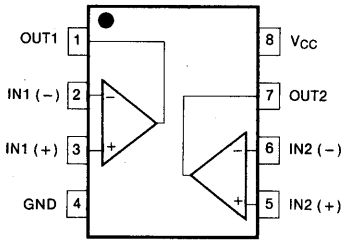
Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single power supply systems.

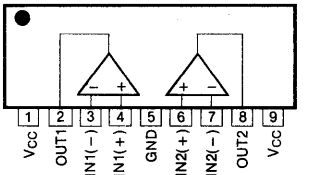


FEATURES

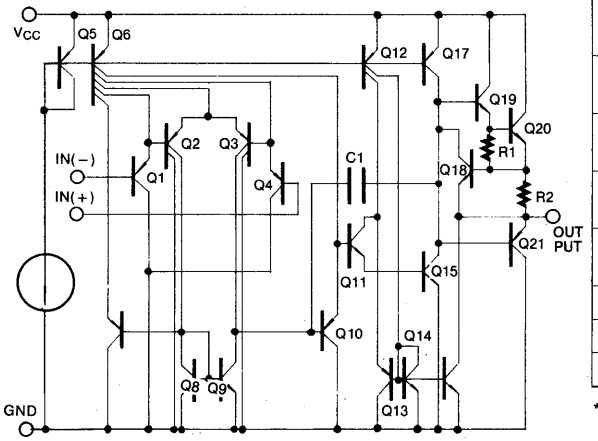
- **Internally frequency compensated for unity gain**
- **Large DC voltage gain: 100dB**
- **Wide power supply range: LM258/A, LM358/A: 3V ~ 32V (or ± 1.5V ~ ± 16V)**
  LM2904: 3V ~ 26V (or ± 1.5V ~ ± 13V)
- **Input common-mode voltage range includes ground**
- **Large output voltage swing: 0V DC to V_{CC} – 1.5V DC**
- **Power drain suitable for battery operation.**

BLOCK DIAGRAM





SCHEMATIC DIAGRAM (One section only)



ORDERING INFORMATION

Device	Package	Operation Temperature
LM358N LM358AN	8 DIP	0 ~ + 70°C
LM358S LM358AS	9 SIP	
LM358D LM358AD	8 SOP	
LM258N LM258AN	8 DIP	– 25 ~ + 85°C
LM258S LM258AS	9 SIP	
LM258D LM258AD	8 SOP	
LM2904N	8 DIP	– 40 ~ + 85°C
LM2904S	9 SIP	
LM2904D	8 DIP	

** Under development

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	LM258/LM258A	LM358/LM358A	LM2904	Unit
Power Supply Voltage	V_S	± 16 or 32	± 16 or 32	± 13 or 26	V
Differential Input Voltage	V_{ID}	± 32	± 32	± 26	V
Input Voltage	V_I	−0.3 to +32	−0.3 to +32	−0.3 to +26	V
Output Short Circuit to GND $V_{CC} \leq 15V$ Ta = 25°C (One Amp)		Continuous	Continuous	Continuous	
Operating Temperature Range	T_{opr}	−25 ~ +85	0 ~ +70	−40 ~ +85	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	−65 ~ +150	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM258			LM358			LM2904			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} − 1.5V V_o = 1.4V, R_S = 0Ω		2.9	5.0		2.9	7.0		2.9	7.0	mV
Input Offset Current	I_{IO}			3	30		5	50		5	50	nA
Input Bias Current	I_{IB}			45	150		45	250		45	250	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V (LM2904, V_{CC} = 26V)	0		V_{CC} -1.5	0		V_{CC} -1.5	0		V_{CC} -1.5	V
Supply Current	I_{CC}	$R_L = \infty$, V_{CC} = 30V (LM2902, V_{CC} = 26V)		0.8	2.0		0.8	2.0		0.8	2.0	mA
		$R_L = \infty$, over full temperature range		0.5	1.2		0.5	1.2		0.5	1.2	mA
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq 2K\Omega$ V_o = 1V to 11V	50	100		25	100		25	100		V/mV
Output Voltage Swing	V_{OH} V_{OL}	V_{CC} = 30V $R_L = 2K\Omega$	26			26			22			V
		V_{CC} = 26V for 2904 $R_L = 10K\Omega$	27	28		27	28		23	24		V
		V_{CC} = 5V $R_L \geq 10K\Omega$		5	20		5	20		5	100	mV
Common-Mode Rejection Ratio	CMRR		70	85		65	80		50	80		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		50	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120			120		dB
Short Circuit to GND	I_{OS}			40	60		40	60		40	60	mA
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V V_{CC} = 15V, V_o = 2V	10	30		10	30		10	30		mA
	I_{sink}	V_{in+} = 0V, V_{in-} = 1V V_{CC} = 15V, V_o = 2V	10	15		10	15		10	15		mA
		V_{in+} = 0V, V_{in-} = 1V V_{CC} = 15V, V_o = 200mV	12	100		12	100					μA
Differential Input Voltage	V_{ID}				V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)
The following specification apply over the range of $-25°C \leq Ta \leq +85°C$ for the LM258; and the $0°C \leq Ta \leq +70°C$ for the LM358; and the $-40°C \leq Ta \leq +85°C$ for the LM2904

Characteristic	Symbol	Test Conditions		LM258			LM358			LM2904			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V V_O = 1.4V, R_S = 0Ω				7.0			9.0			10.0	mV
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$	R_S = 0Ω			7.0			7.0			7.0		μV/°C
Input Offset Current	I_{IO}					100			150		45	200	nA
Input Offset Current Drift	$\triangle I_{IO}/\triangle T$				10			10			10		pA/°C
Input Bias Current	I_{IB}				40	300		40	500		40	500	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V (LM2904, V_{CC} = 26V)		0		V_{CC} -2.0	0		V_{CC} -2.0	0		V_{CC} -2.0	V
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq 2.0K\Omega$ V_O = 1V to 11V		25			15			15			V/mV
Output Voltage Swing	V_{OH}	V_{CC} = 30V	$R_L = 2K\Omega$	26			26			26			V
		V_{CC} = 26V for 2904	$R_L = 10K\Omega$	27	28		27	28		27	28		V
	V_{OL}	V_{CC} = 5V, $R_L \geq 10K\Omega$			5	20		5	20		5	100	mV
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V V_{CC} = 15V, V_O = 2V		10	30		10	30		10	30		mA
	I_{sink}	V_{in+} = 0V, V_{in-} = 1V V_{CC} = 15V, V_O = 2V		5	8		5	9		5	9		mA
Differential Input Voltage	V_{ID}					V_{CC}			V_{CC}			V_{CC}	V

4

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM258A			LM358A			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V V_O = 1.4V, R_S = 0			1.0	3.0		2.0	3.0	mV
Input Offset Current	I_{IO}				2	15		5	30	nA
Input Bias Current	I_{IB}				40	80		45	100	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V		0		V_{CC} -1.5	0		V_{CC} -1.5	V
Supply Current	I_{CC}	R_L = ∞, V_{CC} = 30V			0.8	2.0		0.8	2.0	mA
		R_L = ∞, over full temperature range			0.5	1.2		0.5	1.2	mA
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq 2K\Omega$ V_O = 1V to 11V		50	100		25	100		V/mV
Output Voltage Swing	V_{OH}	V_{CC} = 30V	$R_L = 2K\Omega$	26			26			V
		V_{CC} = 26V for 2904	$R_L = 10K\Omega$	27	28		27	28		V
	V_{OL}	V_{CC} = 5V, $R_L \geq 10K\Omega$			5	20		5	20	mV
Common-Mode Rejection Ratio	CMRR			70	85		65	85		dB
Power Supply Rejection Ratio	PSRR			65	100		65	100		dB
Channel Separation	CS	f = 1KHz to 20KHz			120			120		dB
Short Circuit to GND	I_{OS}				40	60		40	60	mA
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V V_{CC} = 15V, V_O = 2V		20	30		20	30		mA
	I_{sink}	V_{in+} = 0V, V_{in-} = 1V V_{CC} = 15V, V_O = 2V		10	15		10	15		mA
		V_{in+} = 0V, V_{in-} = 1V V_O = 200mV		12	100		12	100		μA
Differential Input Voltage	V_{ID}					V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)

The following specification apply over the range of $-25°C \leq Ta \leq +85°C$ for the LM258A; and the $0°C \leq Ta \leq +70°C$ for the LM358A

Characteristic	Symbol	Test Conditions		LM258A			LM358A			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V V_O = 1.4V, R_S = 0Ω				4.0			5.0	mV
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$				7.0	15		7.0	20	μV/°C
Input Offset Current	I_{IO}					30			75	nA
Input Offset Current Drift	$\triangle I_{IO}/\triangle T$				10	200		10	300	pA/°C
Input Bias Current	I_{IB}				40	100		40	200	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V		0		V_{CC} -2.0	0		V_{CC} -2.0	V
Output Voltage Swing	V_{OH}	V_{CC} = 30V	R_L = 2KΩ	26			26			V
		V_{CC} = 30V	R_L = 10KΩ	27	28		27	28		V
	V_{OL}	V_{CC} = 5V, $R_L \geq$ 10KΩ			5	20		5	20	mV
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq$ 2.0KΩ V_O = 1V to 11V		25			15			V/mV
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V V_{CC} = 15V, V_O = 2V		10	30		10	30		mA
	I_{sink}	V_{in+} = 0V, V_{in-} = 1V V_{CC} = 15V, V_O = 2V		5	9		5	9		mA
Differential Input Voltage	V_{ID}					V_{CC}			V_{CC}	V

4

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

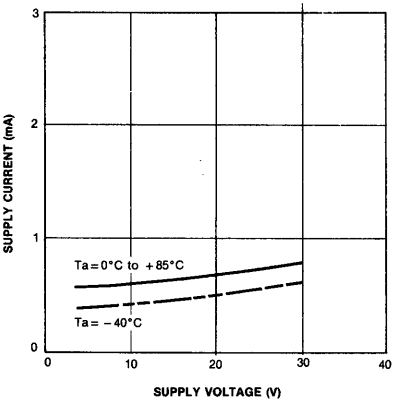


Fig. 2 VOLTAGE GAIN

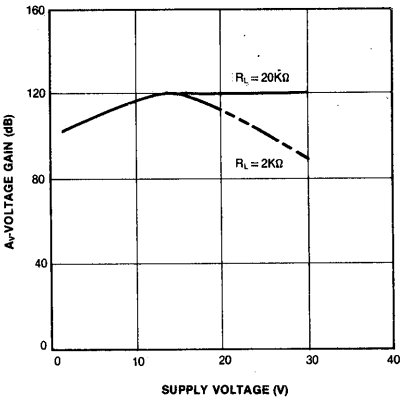


Fig. 3 OPEN LOOP FREQUENCY RESPONSE

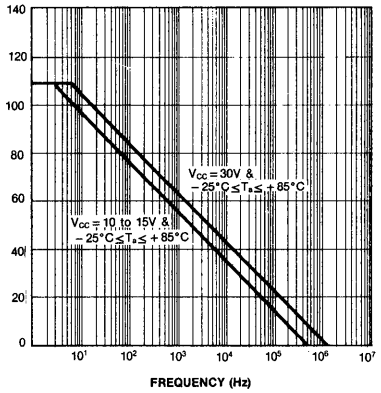


Fig. 4 LARGE SIGNAL FREQUENCY

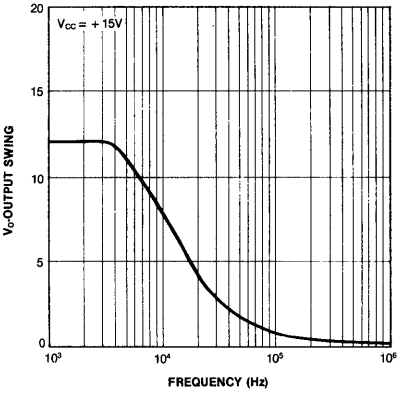


Fig. 5 OUTPUT CHARACTERISTICS CURRENT SOURCING

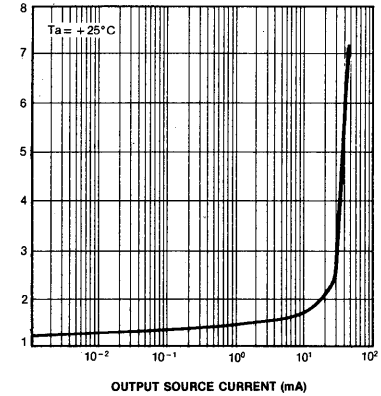


Fig. 6 OUTPUT CHARACTERISTICS CURRENT SINKING

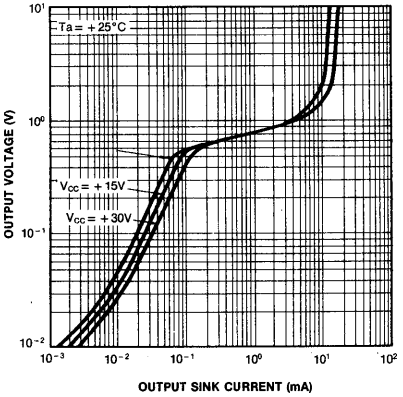


Fig. 7 INPUT VOLTAGE RANGE

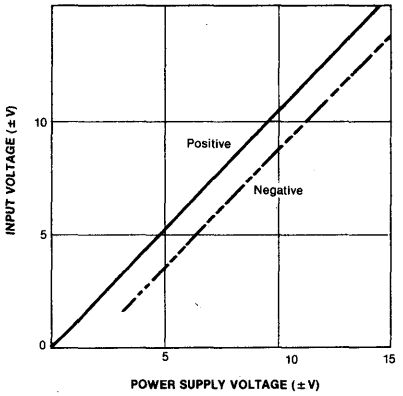


Fig. 8 COMMON-MODE REJECTION RATIO

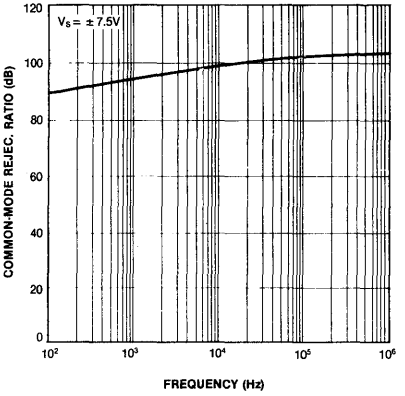


Fig. 9 CURRENT LIMITING

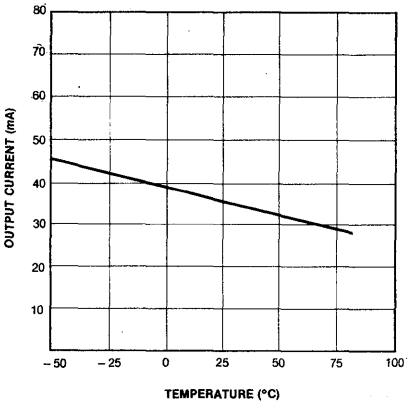


Fig. 10 INPUT CURRENT

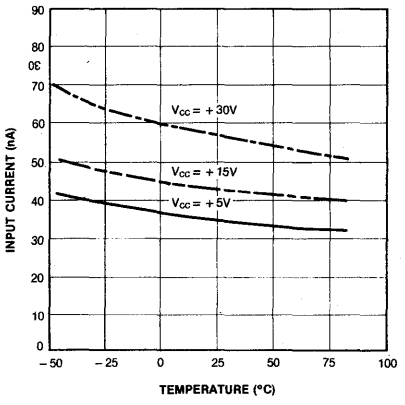


Fig. 11 VOLTAGE FOLLOWER PULSE RESPONSE

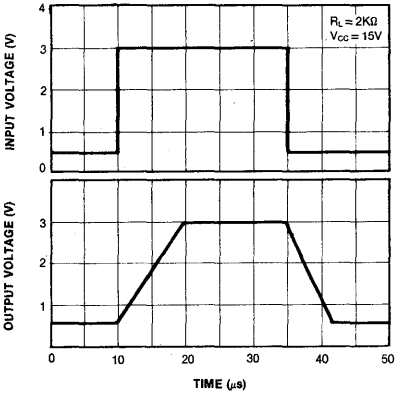
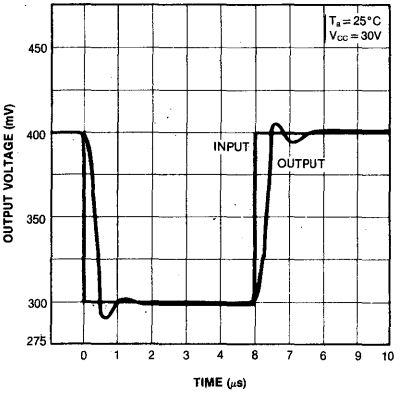


Fig. 12 VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



4

TYPICAL APPLICATIONS (V_{CC} = 5.0V)

Fig. 13 Voltage Reference

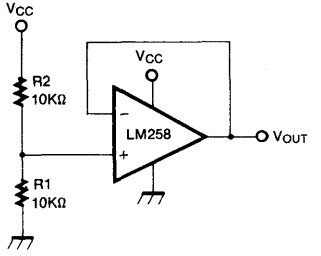


Fig. 14 Non-Inverting DC Gain

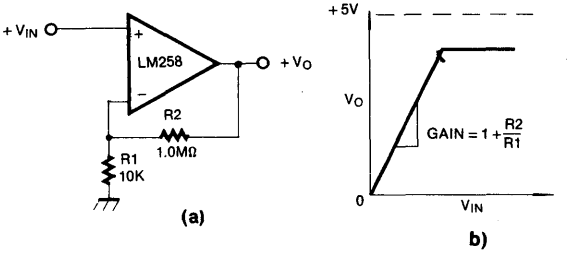


Fig. 15 AC Coupled Non-Inverting Amplifier

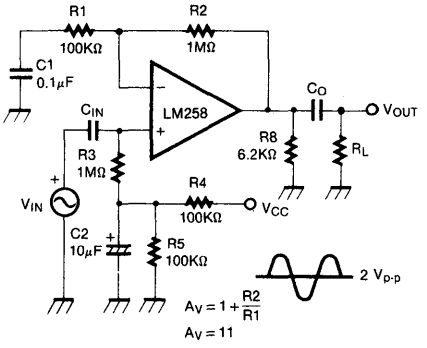


Fig. 16 Pulse Generator

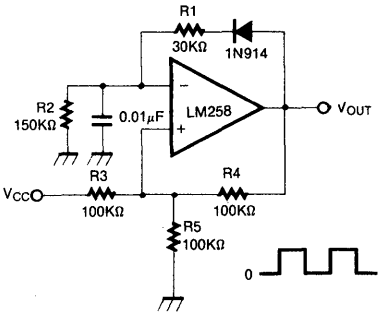
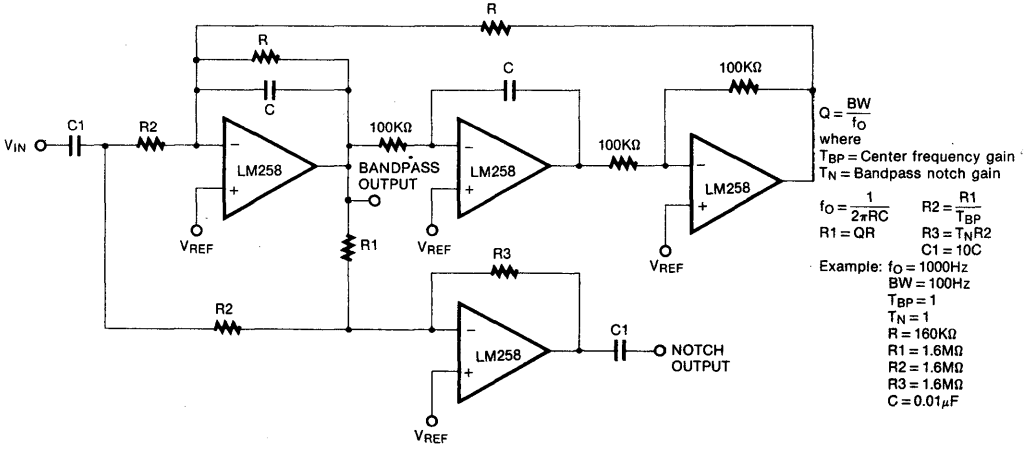


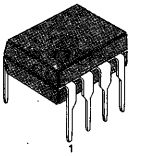
Fig. 17 Bi-Quad Filter



SINGLE OPERATIONAL AMPLIFIERS

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. It is intended for a wide range of analog applications.
The high gain and wide range of operating voltage provide superior performance in intergrator, summing amplifier, and general feedback applications.

8 DIP



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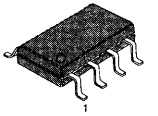
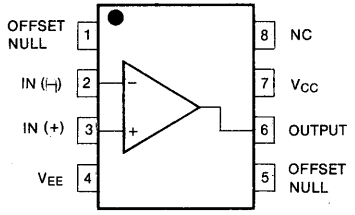


FEATURES

- **Short circuit protection**
- **Excellent temperature stability**
- **Internal frequency compensation**
- **High input voltage range**
- **Null of offset**

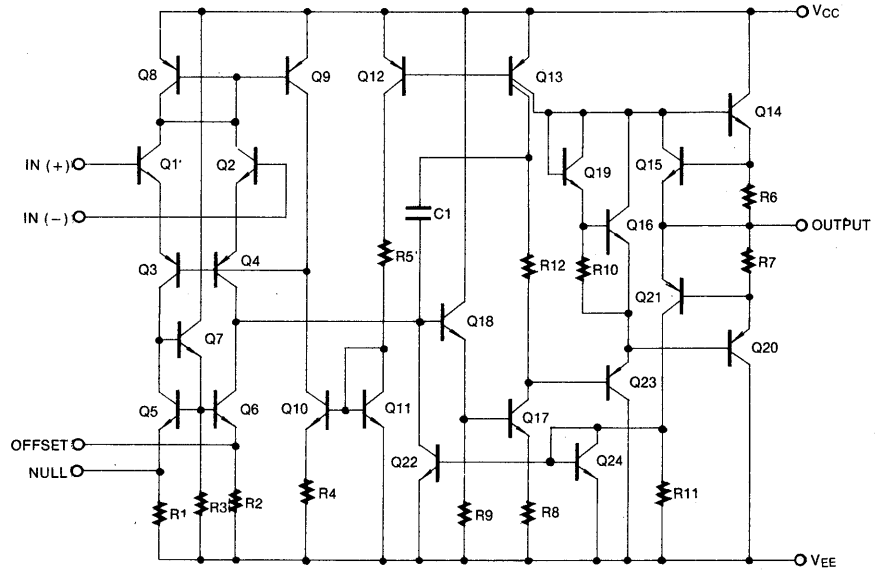
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operation Temperature
LM741ECN LM741CN	8 DIP	0 ~ +70°C
LM741ECD LM741CD	8 SOP	
LM741IN LM741EIN	8 DIP	−25 ~ +85°C
LM741ID LM741EID	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	LM741C	LM741E	LM741I	Unit
Power Supply Voltage	V_S	±18	±22	±18	V
Differential Input Voltage	V_{ID}	±30	±30	±30	V
Input Voltage	V_I	±15	±15	±15	V
Output Short Circuit Duration		Indefinite	Indefinite	Indefinite	
Power Dissipation	P_D	500	500	500	mW
Operating Temperature Range	T_{opr}	0 ~ +70	0 ~ +70	−25 ~ +85	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	−65 ~ +150	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM741E			LM741C/LM741I			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 10K\Omega$						2.0	6.0	mV
		$R_S \leq 50\Omega$			0.8	3.0				
Input Offset Voltage Adjustment Range	V_{IOR}	$V_S = \pm 20V$		±10				±15		mV
Input Offset Current	I_{IO}				3.0	30		20	200	nA
Input Bias Current	I_{IB}				30	80		80	500	nA
Input Resistance	R_i	$V_S = \pm 20V$		1.0	6.0		0.3	2.0		MΩ
Input Voltage Range	V_{ICR}			±12	±13		±12	±13		V
Large Signal Voltage Gain	A_V	$R_L \geq 2K\Omega$	$V_S = \pm 20V$, $V_O = \pm 15V$	50						V/mV
			$V_S = \pm 15V$, $V_O = \pm 10V$				20	200		
Output Short Circuit Current	I_{OS}			10	25	35		25		mA
Output Voltage Swing	V_{OUT}	$V_S = \pm 20V$	$R_L \geq 10K\Omega$	±16						V
			$R_L \geq 2K\Omega$	±15						
		$V_S = \pm 15V$	$R_L \geq 10K\Omega$				±12	±14		
			$R_L \geq 2K\Omega$				±10	±13		
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K\Omega$, $V_{CM} = \pm 12V$					70	90		dB
		$R_S \leq 50K\Omega$, $V_{CM} = \pm 12V$		80	95					
Power Supply Rejection Ratio	PSRR	$V_S = \pm 20V$ to $V_S = \pm 5V$, $R_S \leq 50\Omega$		86	96					dB
		$V_S = \pm 15V$ to $V_S = \pm 5V$, $R_S \leq 10K\Omega$					77	96		

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Conditions	LM741E			LM741C/LM741I			Unit
				Min	Typ	Max	Min	Typ	Max	
Transient Response	Rise Time	t_r	Unity Gain		0.25	0.8		0.3		μs
	Overshoot	OS			6.0	20		10		%
Bandwidth		BW		0.43	1.5					MHz
Slew Rate		SR	Unity Gain	0.3	0.7			0.5		V/μs
Supply Current		I_S	$R_L = \infty\ \Omega$					1.5	2.8	mA
Power Consumption		P_C	$V_S = \pm 20V$		80	150				mW
			$V_S = \pm 15V$					50	85	

ELECTRICAL CHARACTERISTICS

($-25°C \leq Ta \leq 85°C$ for the LM741I, $0°C \leq Ta \leq 70°C$ for the LM741C and LM741E, $V_{CC} = \pm 15V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM741E			LM741C/LM741I			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 50\Omega$				4.0				mV
		$R_S \leq 10K\Omega$							7.5	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$				15					μV/°C
Input Offset Current	I_{IO}					70			300	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$					0.5				nA/°C
Input Bias Current	I_{IB}					0.21			0.8	μA
Input Resistance	R_i	$V_S = \pm 20V$		0.5						MΩ
Input Voltage Range	V_{ICR}			±12	±13		±12	±13		V
Output Voltage Swing	V_{OUT}	$V_S = \pm 20V$	$R_L \geq 10K\Omega$	±16						V
			$R_L \geq 2K\Omega$	±15						
		$V_S = \pm 15V$	$R_L \geq 10K\Omega$				±12	±14		
			$R_L \geq 2K\Omega$				±10	±13		
Output Short Circuit Current	I_{OS}			10		40	10		40	mA
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K\Omega$, $V_{CM} = \pm 12V$					70	90		dB
		$R_S \leq 50K\Omega$, $V_{CM} = \pm 12V$		80	95					
Power Supply Rejection Ratio	PSRR	$V_S = \pm 20V$ to $\pm 5V$	$R_S \leq 50\Omega$	86	96					dB
			$R_S \leq 10K\Omega$				77	96		
Large Signal Voltage Gain	A_V	$R_L \geq 2K\Omega$	$V_S = \pm 20V$, $V_o = \pm 15V$	32						V/mV
			$V_S = \pm 15V$, $V_O = \pm 10V$				15			
			$V_S = \pm 15$, $V_O = 2V$	10						

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 7 OUTPUT RESISTANCE vs FREQUENCY

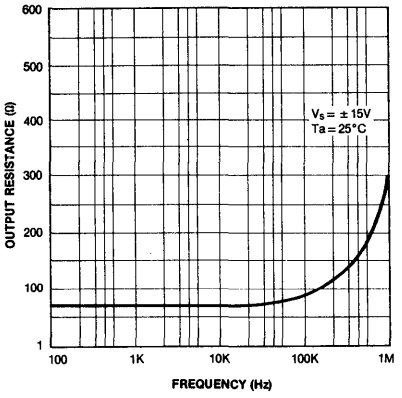


Fig. 8 INPUT RESISTANCE AND INPUT CAPACITANCE vs FREQUENCY

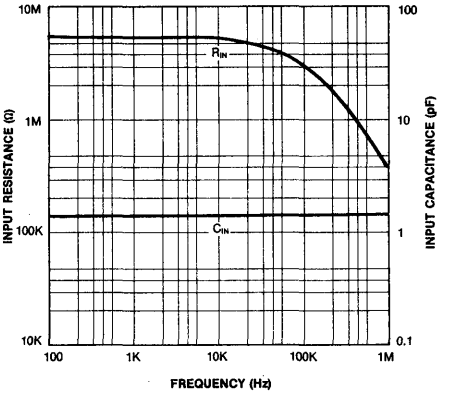


Fig. 9 INPUT BIAS CURRENT vs AMBIENT TEMPERATURE

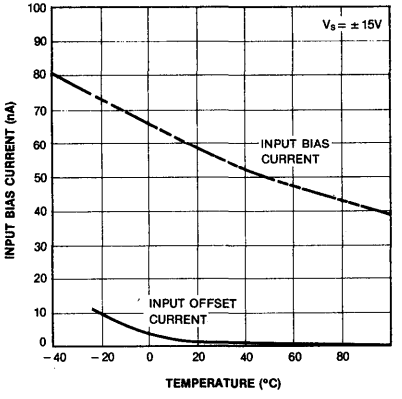


Fig. 10 POWER CONSUMPTION vs AMBIENT TEMPERATURE

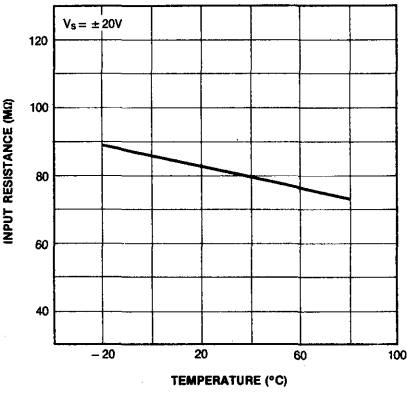


Fig. 11 INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE

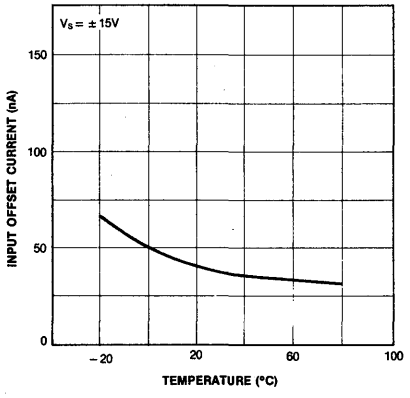


Fig. 12 INPUT RESISTANCE vs AMBIENT TEMPERATURE

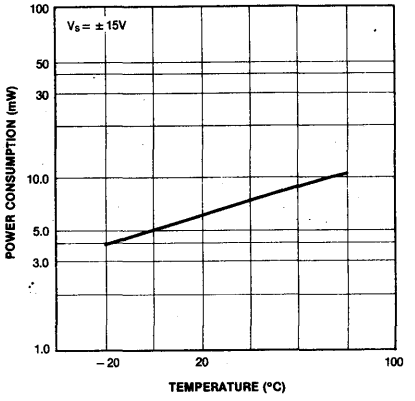


Fig. 13 NORMALIZED DC PARAMETERS vs AMBIENT TEMPERATURE

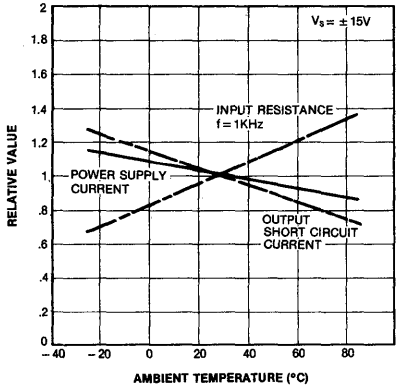


Fig. 14 FREQUENCY CHARACTERISTICS vs AMBIENT TEMPERATURE

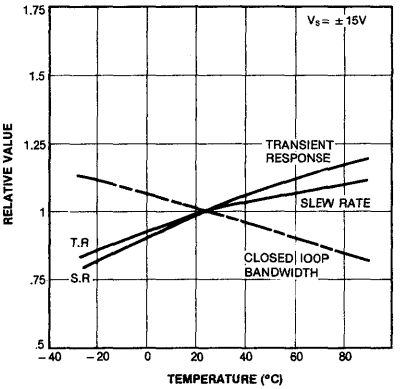


Fig. 15 FREQUENCY CHARACTERISTICS vs SUPPLY VOLTAGE

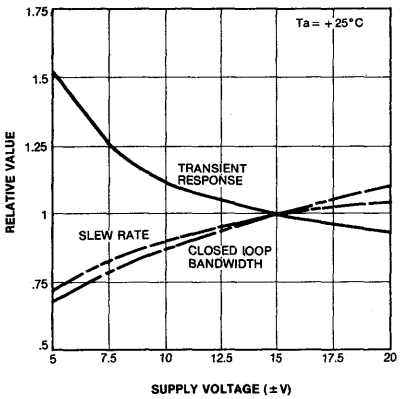


Fig. 16 OUTPUT SHORT CIRCUIT CURRENT vs AMBIENT TEMPERATURE

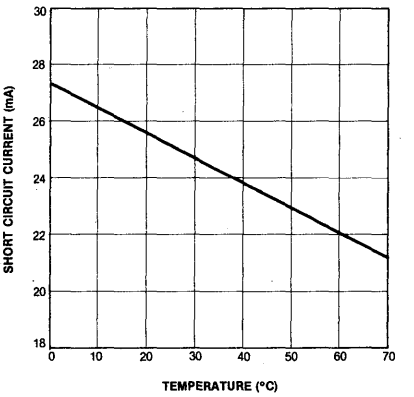


Fig. 17 TRANSIENT RESPONSE

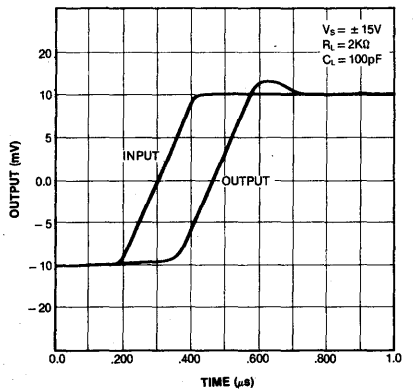


Fig. 18 COMMON-MODE REJECTION RATIO vs FREQUENCY

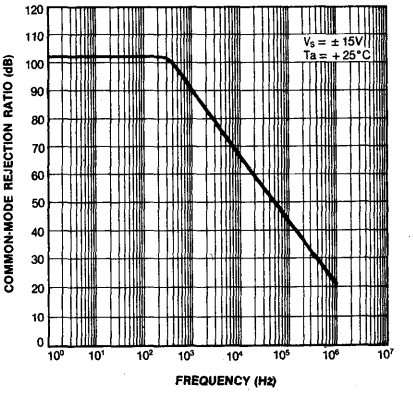


Fig. 18 VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

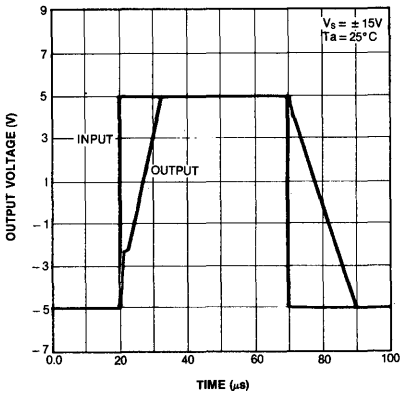
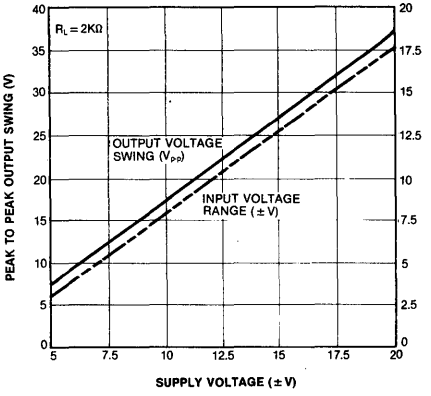
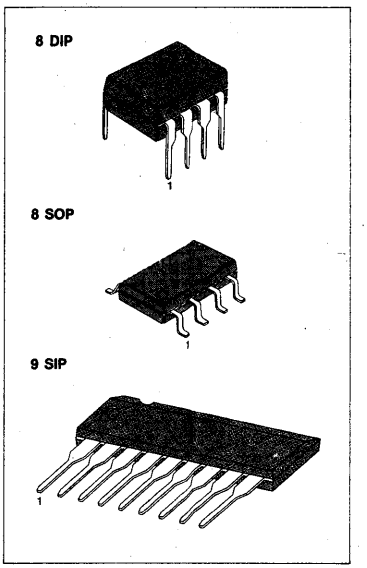


Fig. 19 OUTPUT SWING AND INPUT RANGE vs SUPPLY VOLTAGE



DUAL OPERATIONAL AMPLIFIERS

The MC1458 series is a dual general purpose operational amplifier. The MC1458 series is a short circuit protected and require no external components for frequency compensation.
High common mode voltage range and absence of "latch up" make the MC1458 ideal for use as voltage followers.
The high gain and wide range of operating voltage provides superior performance in intergrator, summing amplifier and general feedback applications.

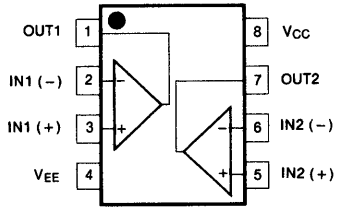


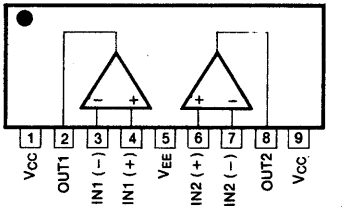
FEATURES

- **Interal frequency compensation**
- **Short circuit protection**
- **Large common mode and differential voltage range**
- **No latch up**
- **Low power consumption**

4

BLOCK DIAGRAM

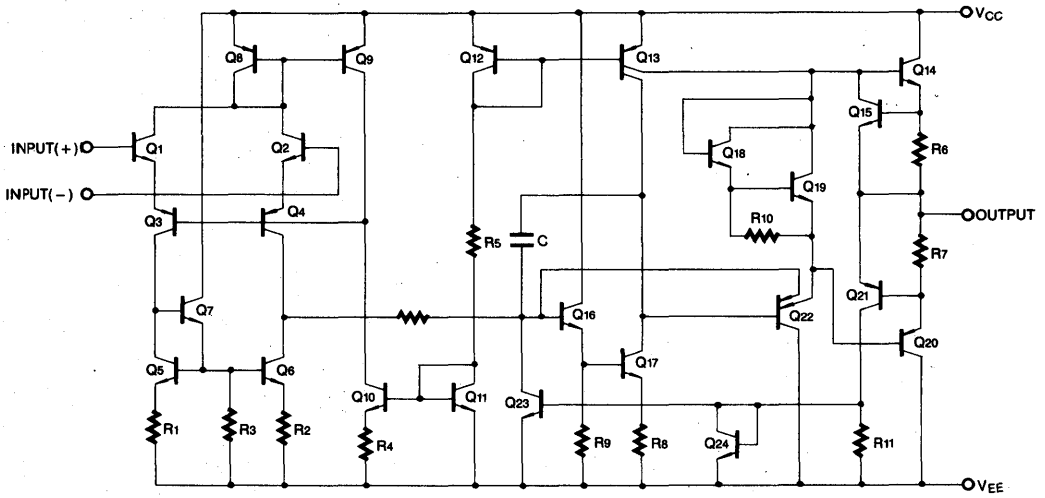




ORDERING INFORMATION

Device	Package	Operation Temperature
MC1458CN MC1458ACN	8 DIP	0 ~ +70°C
MC1458CS MC1458ACS	9 SIP	
MC1458CD MC1458ACD	8 SOP	
MC1458IN MC1458AIN	8 DIP	−25 ~ +85°C
MC1458IS MC1458AIS	9 SIP	
MC1458ID MC1458AID	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_S	±18	V
Input Differential Voltage	V_{ID}	±30	V
Input Voltage	V_I	±15	V
Operating Temperature Range MC1458I	T_{opr}	−25 ~ +85	°C
MC1458AC/C		0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	MC1458/MC1458I			MC1458C			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 10K\Omega$		2.0	6.0		2.0	10	mV
Input Offset Current	I_{IO}			20	200		20	300	nA
Input Bias Current	I_{IB}			80	500		80	700	nA
Large Signal Voltage Gain	A_V	$V_o = \pm 10V$, $R_L \geq 2.0K\Omega$	20	200		20	200		V/mV
Input Voltage Range	V_{ICR}		±12	±13		±11	±13		V
Input Resistance	R_I		0.3	1.0			1.0		MΩ
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K\Omega$	70	90		60	90		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10K\Omega$	77	90		77	90		dB
Supply Current (Both Amplifier)	I_S			2.3	5.6		2.3	8.0	mA
Output Voltage Swing	V_{OUT}	$R_L = 10K\Omega$	±12	±14		±11	±14		V
		$R_L = 2K\Omega$	±10	±13		±9	±13		
Output Short Circuit Current	I_{OS}			20			20		mA
Power Consumption	P_C	$V_o = 0V$		70	170		70	240	mA
Transient Response (Unity Gain)									
Rise Time	t_r	$V_i = 20mV$, $R_L \geq 2K\Omega$, $C_L \leq 100pF$		0.3			0.3		μs
Overshoot	OS	$V_i = 20mV$, $R_L \geq 2K\Omega$, $C_L \leq 100pF$		15			15		%
Slew Rate	SR	$V_i = 10V$, $R_L \geq 2K\Omega$, $C_L \leq 100pF$		0.5			0.5		V/μs

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, NOTE 1, unless otherwise specified)

Characteristic	Symbol	Test Conditions	MC1458/MC1458I			MC1458C			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 10K\Omega$			7.5			12	mV
Input Offset Current	I_{IO}				300			400	nA
Input Bias Current	I_{IB}				800			1000	nA
Large Signal Voltage Gain	A_V	$V_o = \pm 10V$, $R_L \geq 2.0K$	15			15			V/mV
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K$	70	90		70	90		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10K$	77	90		77	90		dB
Output Voltage Swing	V_{OUT}	$R_L = 10K$	±12	±14		±11	±14		V
		$R_L = 2K$	±10	±13		±9	±13		
Input Voltage Range	V_{ICR}		±12			±12			V

NOTE 1
MC1458AC/C: $0 \leq Ta \leq 70°C$
MC1458I: $-25 \leq Ta \leq +85°C$

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 OPEN-LOOP VOLTAGE GAIN vs POWER SUPPLY VOLTAGES

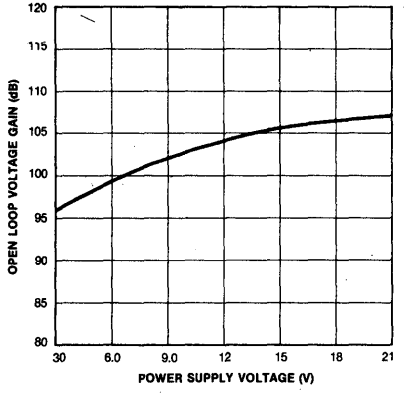


Fig. 2 OPEN-LOOP FREQUENCY RESPONSE

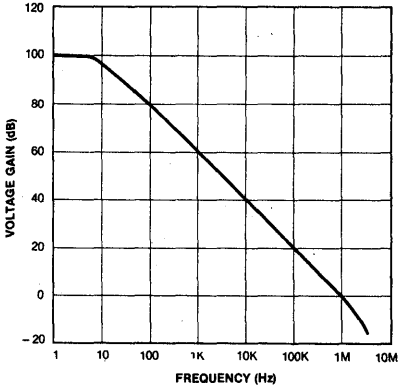


Fig. 3 POWER BANDWIDTH (LARGE SIGNAL SWING vs FREQUENCY)

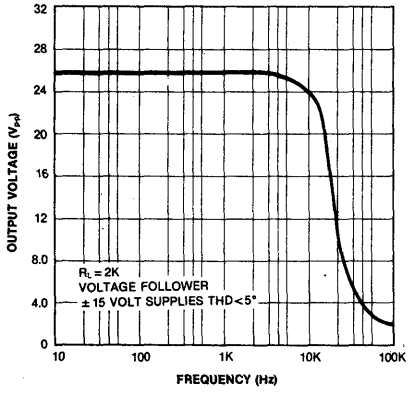
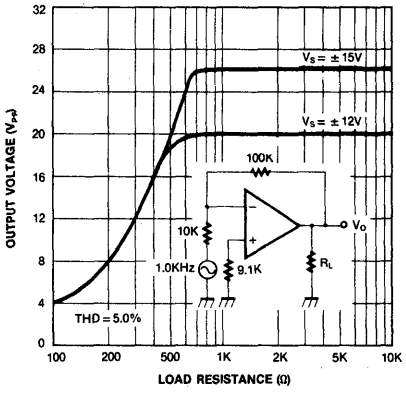


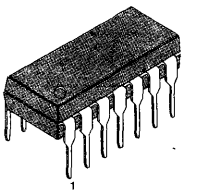
Fig. 4 OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



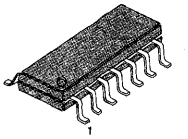
QUAD OPERATIONAL AMPLIFIER

The MC3303 series is a monolithic Quad operational amplifier consisting of four independent amplifiers. The device has high gain, internally frequency, compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common made input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications.

14 DIP



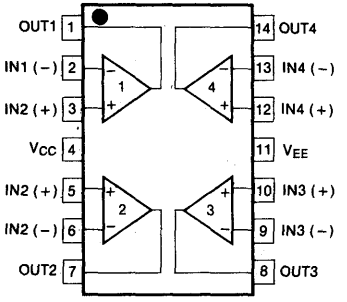
14 SOP



FEATURES

- **Output voltage can swing to GND or negative supply**
- **Wide power supply range;**
  Single supply of 3.0V to 36V
  Dual supply of ±1.5V to ±18V
- **Electrical characteristics similar to the popular LM741**
- **CLASS AB output stage for minimal crossover distortion**
- **Short circuit protected output.**

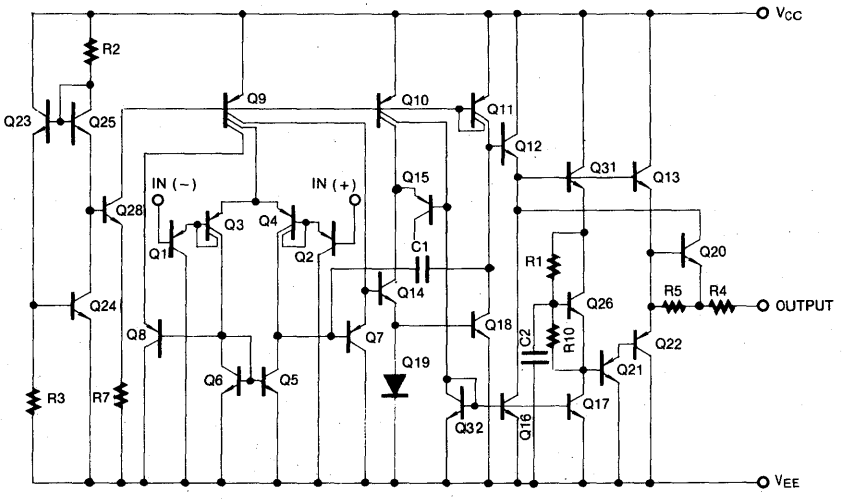
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operation Temperature
MC3303N	14 DIP	−40 ~ +85°C
MC3303D	14 SOP	
MC3403N	14 DIP	0 ~ +70°C
MC3403D	14 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_S	±18 or 36	V
Differential Input Voltage	V_{ID}	±36	V
Input Voltage	V_I	±18	V
Output Short Circuit Duration		Continuous	
Power Dissipation	P_D	670	mW
Operating Temperature MC3303	T_{opr}	−40 ~ +85	°C
MC3403		0 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V for MC3403, V_{CC} = +14V, V_{EE} = GND for MC3303, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	MC3303			MC3403			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}			1.5	8.0		1.5	10	mV
		NOTE 1			10			12	
Input Offset Current	I_{IO}			5	75		5	50	nA
		NOTE 1			150			100	
Input Bias Current	I_{IB}			30	200		30	200	nA
		NOTE 1			500			400	
Large Signal Voltage Gain	A_V	V_o = ±10V, R_L = 2KΩ	20	200		20	200		V/mV
		NOTE 1	15			15			
Input Impedance	R_i		0.3	1		0.3	1.0		MΩ
Output Voltage Swing	V_{OUT}	R_L = 10KΩ	12	12.5		±12	±13.5		V
		R_L = 2KΩ	10	12		±10	±13		
		R_L = 2KΩ NOTE 1	10			10			
Input Common Mode Voltage Range	V_{ICR}		12V-V_{EE}	12.5V-V_{EE}		13V-V_{EE}	13.5V-V_{EE}		V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K\Omega$	70	90		70	90		dB
Power Supply Current	I_S	V_o = 0, R_L = ∞		2.8	7.0		2.3	7.0	mA
Output Short Circuit Current	I_{OS}	Each amplifier	±10	±30	±45	±10	±20	±45	mA
Positive Supply Rejection Ratio	$PSRR^+$			30	150		30	150	μV/V
Negative Supply Rejection Ratio	$PSRR^-$						30	150	μV/V
Average Temperature Coefficient of Input Offset Current	$\Delta I_{io}/\Delta T$			50			50		pA/°C

ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC} = +15V, V_{EE} = −15V for MC3403, V_{CC} = +14V, V_{EE} = GND for MC3303, unless otherwise specified)

Characteristic	Symbol	Test Conditions	MC3303			MC3403			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$			10			10		μV/°C
Power Bandwidth	GBW	A_V = 1, R_L = 2KΩ, V_o = $20V_{p-p}$, THD = 5%		9.0			9.0		KHz
Small Signal Bandwidth	BW	A_V = 1, R_L = 10KΩ, V_o = 50mV		1.0			1.0		MHz
Slew Rate	SR	A_V = 1, V_{IN} = −10V to +10V		0.4			0.4		V/μs
Rise Time	t_r	A_V = 1, R_L = 10KΩ, V_o = 50mV		0.35			0.35		μs
Fall Time	t_f	A_V = 1, R_L = 10KΩ, V_o = 50mV		0.35			0.35		μs
Over Shoot	OS	A_V = 1, R_L = 10KΩ, V_O = 50mV		20			20		%
Phase Margin	ϕ_m	A_V = 1, R_L = 2KΩ, C_L = 200pF		60			60		Degrees
Crossover Distortion	CD	V_{IN} = $30mV_{p-p}$, V_o = $2.0V_{p-p}$, f = 10KHz		1.0			1.0		%

NOTE 1
MC3403: $0 \leq Ta \leq +70°C$
MC3303: $-25 < Ta \leq +85°C$

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, Ta = 25°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	MC3303			MC3403			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}				10		2.0	10	mV
Input Offset Current	I_{IO}				75		30	50	nA
Input Bias Current	I_{IB}				500		200	500	nA
Large Signal Open Loop Voltage Gain	A_V	R_L = 2.0KΩ	10	200		10	200		V/mV
Power Supply Rejection Ratio	PSRR				150			150	μV/V
Output Voltage Range	V_{OUT}	R_L = 10K, V_{CC} = 5.0V	3.3	3.5		3.3	3.5		V
		R_L = 10K, $5.0V \leq V_{CC} \leq 30V$	V_{CC}-2.0	V_{CC}-1.7		V_{CC}-2.0	V_{CC}-1.7		
Supply Current	I_{CC}			2.5	7.0		2.5	7.0	mA
Channel Separation	CS	f = 1KHz to 20KHz		120			120		dB

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 OPEN LOOP FREQUENCY RESPONSE

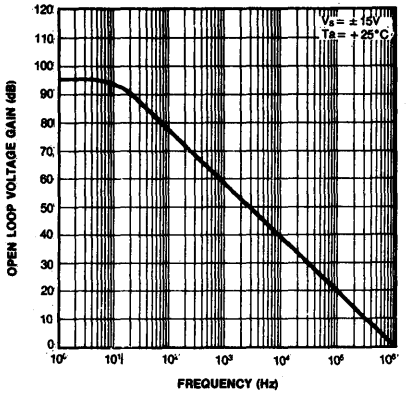


Fig. 2. Wave Response

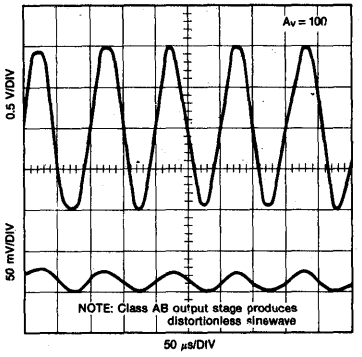


Fig. 3 OUTPUT SWING

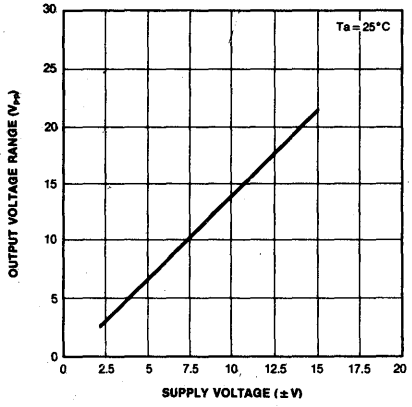


Fig. 4 OUTPUT VOLTAGE vs FREQUENCY

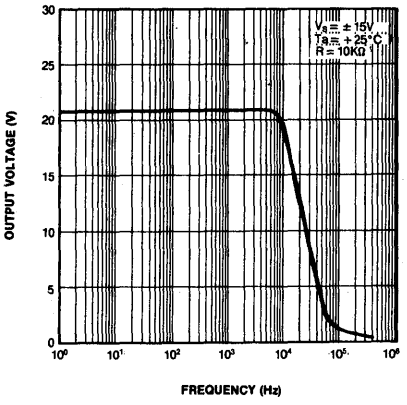


Fig. 5 INPUT BIAS CURRENT vs TEMPERATURE

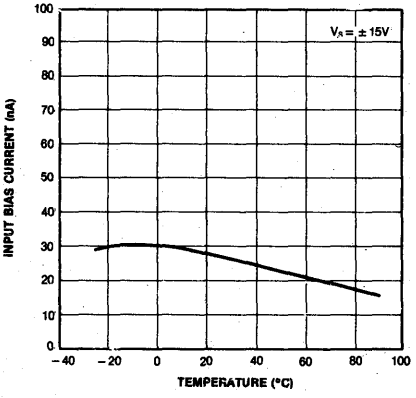
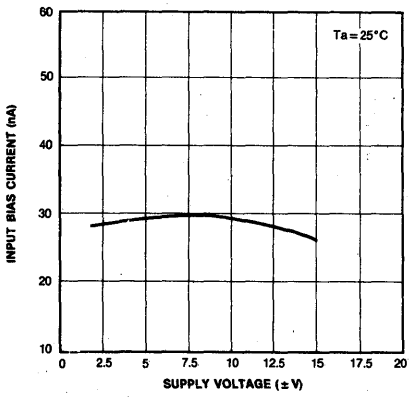
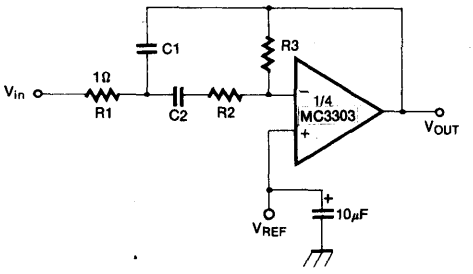


Fig. 6 INPUT BIAS CURRENT vs SUPPLY VOLTAGE



TYPICAL APPLICATIONS

Fig. 7. Multiple feedback bandpass filter



f_o = center frequency

BW = Bandwidth

R in kΩ

C in μF

$$Q = \frac{f_o}{BW} < 10$$

$$C1 = C2 = \frac{Q}{3}$$

$$\left.\begin{array}{l} R1 = R2 = 1 \\ R3 = 9Q^2 - 1 \end{array}\right\}$$ Use scaling factors in these expressions.

If source impedance is high or varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Design example:

given: $Q = 5$, $f_o = 1$ kHz

Let $R1 = R2 = 10$ kΩ

then $R3 = 9(5)^2 - 10$

$R3 = 215$ kΩ

$$C = \frac{5}{3} = 1.6 \text{ nF}$$

Fig. 8. Wein bridge oscillator

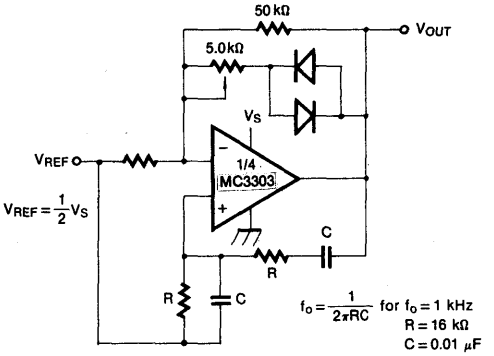
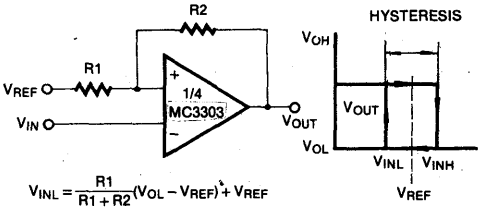


Fig. 9. Comparator with hysteresis



$$V_{INL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{INH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

Fig. 10. High impedance differential amplifier

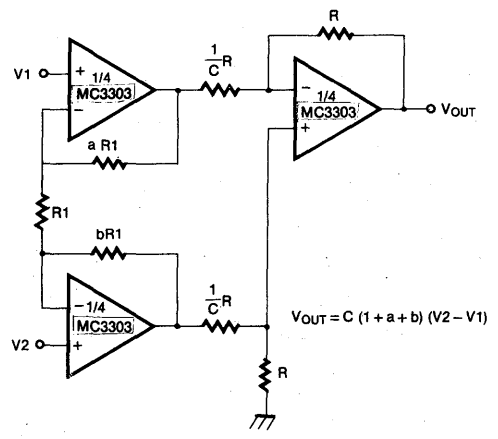


Fig. 11. AC Coupled Inverting amplifier

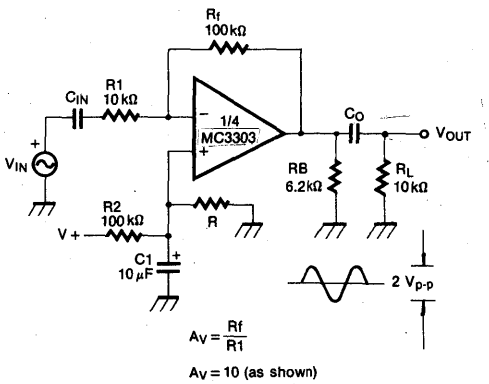


Fig. 12. Ground referencing a differential input signal

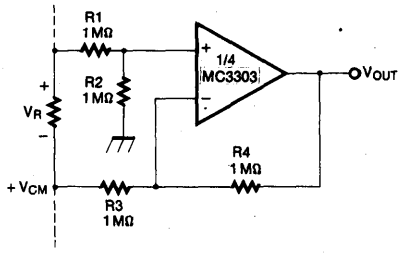


Fig. 13. Voltage reference

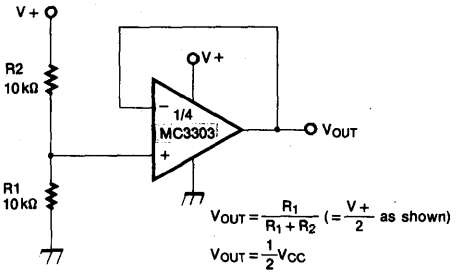


Fig. 14. AC Coupled non-inverting amplifier

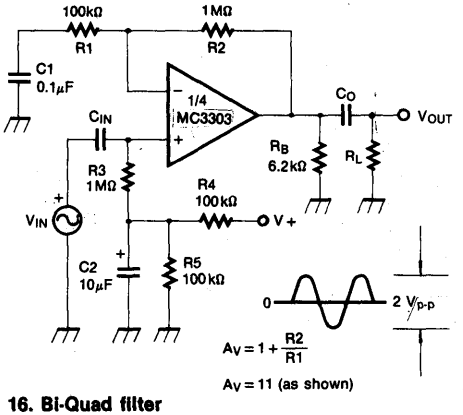


Fig. 15. Pulse generator

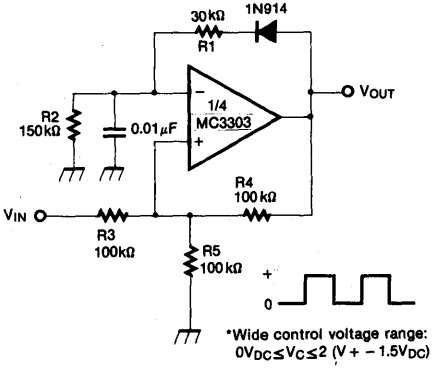


Fig. 16. Bi-Quad filter

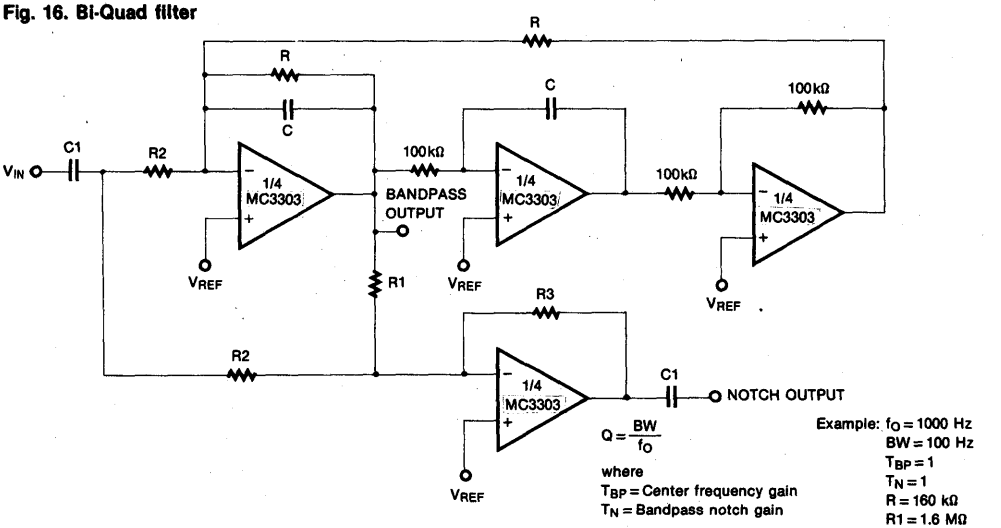


Fig. 17. Voltage controlled oscillator

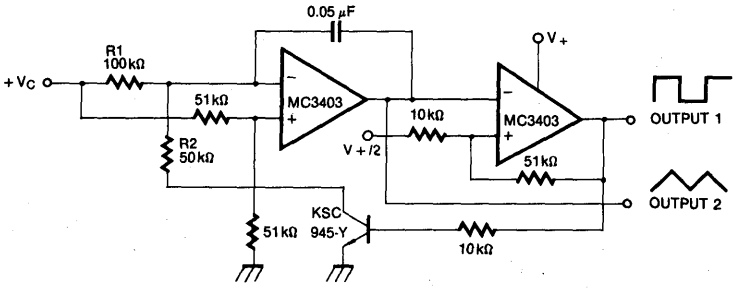
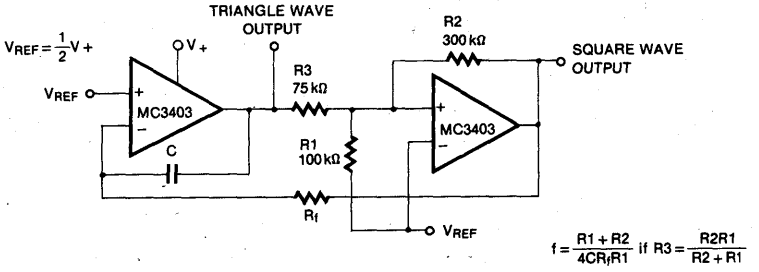
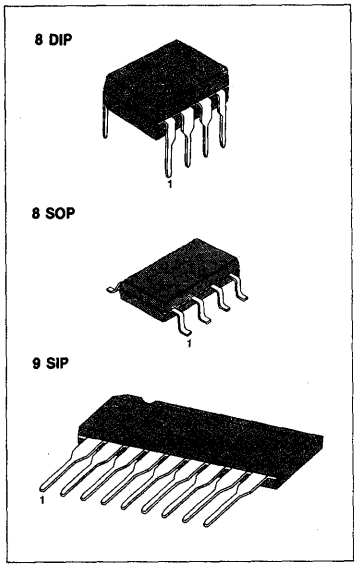


Fig. 18. Function generator



DUAL OPERATIONAL AMPLIFIER

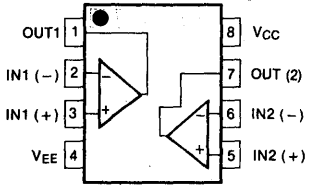
The MC4558 series is a monolithic integrated circuit designed for dual operational amplifier.

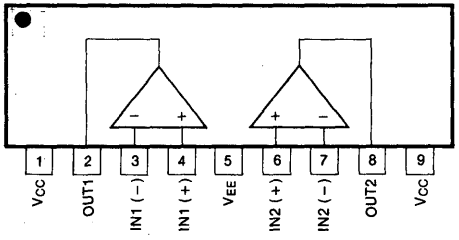


FEATURES

- **No frequency compensation required.**
- **No latch-up.**
- **Large common mode and differential voltage range.**
- **Parameter tracking over temperature range.**
- **Gain and phase match between amplifiers.**
- **Internally frequency compensated.**
- **Low noise input transistors.**

BLOCK DIAGRAM

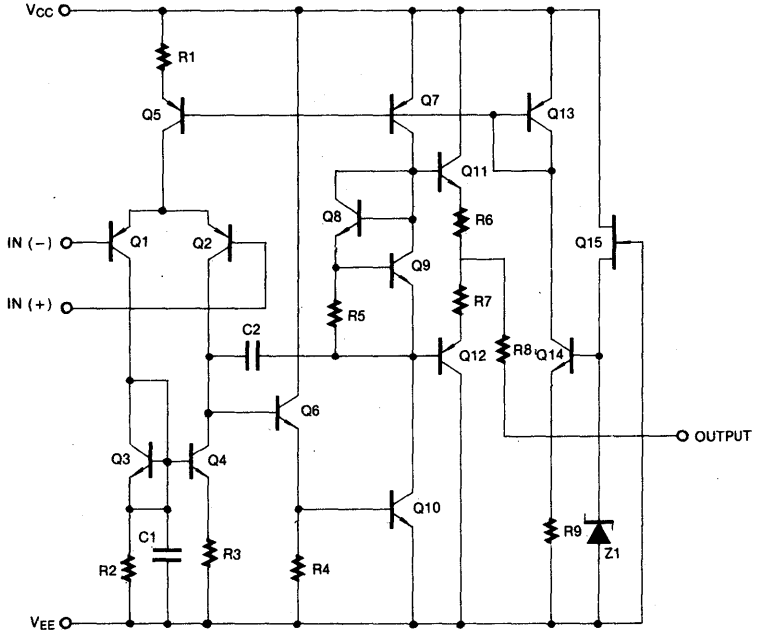




ORDERING INFORMATION

Device	Package	Operation Temperature
MC4558CN MC4558ACN	8 DIP	0 ~ +70°C
MC4558CS MC4558ACS	9 SIP	
MC4558CD MC4558ACD	8 SOP	
MC4558IN MC4558AIN	8 DIP	−25 ~ +85°C
MC4558IS MC4558AIS	9 SIP	
MC4558ID MC4558AID	8 SOP	

SCHEMATIC DIAGRAM (One Section Only)



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage MC4558AC	V_S	±22	V
MC4558C/I		±18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage	V_i	±15	V
Power Dissipation	P_D	400	mW
Operating Temperature Range MC4558I	T_{opr}	−40 ~ +85	°C
MC4558AC/MC4558C		0 ~ 70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC4558I/MC4558AC			MC4558C			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 10K\Omega$			1	5		2	6	mV
			NOTE 1		1	6			7.5	
Input Offset Current	I_{IO}				5	200		5	200	nA
			$T_a = T_{max}$		3	200			300	
			$T_a = T_{min}$		20	500			300	
Input Bias Current	I_{IB}				30	500		30	500	nA
			$T_a = T_{max}$		20	500			800	
			$T_a = T_{min}$		100	1500			800	
Large Signal Voltage Gain	A_V	$V_O = \pm 10V$ $R_L \geq 2.0K\Omega$		50	200		20	200		V/mV
			NOTE 1	25			15			
Common Mode Input Voltage Range	V_{ICR}			±12	±13		±12	±13		V
			NOTE 1	±12	±13					
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K\Omega$		70	90		70	90		dB
			NOTE 1	70	90					
Supply Voltage Rejection Ratio	PSRR	$R_S \leq 10K\Omega$		76	90		76	90		dB
			NOTE 1	76	90		76	90		
Output Voltage Swing	V_{OUT}	$R_L \geq 10K\Omega$	NOTE 1	±12	±14		±12	±14		V
		$R_L \geq 2K\Omega$		±10	±13		±10	±13		
Supply Current (Both Amplifiers)	I_S				3.5	5.0		3.5	5.6	mA
			$T_a = T_{max}$			4.5			5.0	
			$T_a = T_{min}$			6.0			6.7	
Power Consumption (Both Amplifiers)	P_C				70	150		70	170	mV
			$T_a = T_{max}$			135			150	
			$T_a = T_{min}$			180			200	
Slew Rate	SR	$V_i = 10V$, $R_L \geq 2K\Omega$ $C_L \leq 100pF$		1.0			1.0			V/μs
Rise Time	t_r	$V_i = 20mV$, $R_L \geq 2K\Omega$, $C_L \leq 100pF$			0.3			0.3		μs
Overshoot	OS	$V_i = 20mV$, $R_L \geq 2K\Omega$, $C_L \leq 100pF$			15			15		%

NOTE 1

MC4558AC/C: $T_{min} \leq Ta \leq T_{max} = 0 \leq Ta \leq +70°C$

MC4558I: $T_{min} \leq Ta \leq T_{max} = -25 \leq Ta \leq +85°C$

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 BURST NOISE vs SOURCE RESISTANCE

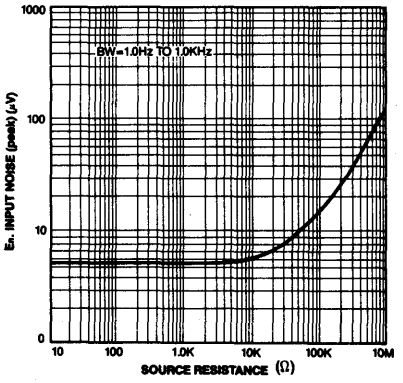


Fig. 2 RMS NOISE vs SOURCE RESISTANCE

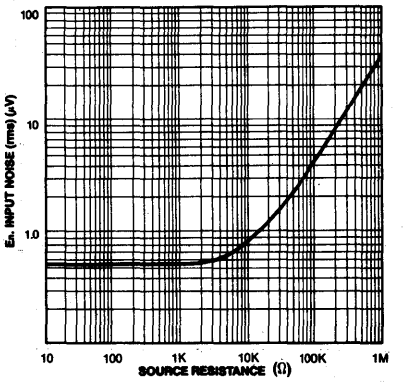


Fig. 3 OUTPUT NOISE vs SOURCE RESISTANCE

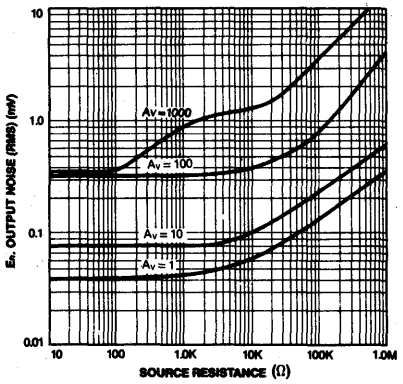


Fig. 4 SPECTRAL NOISE DENSITY

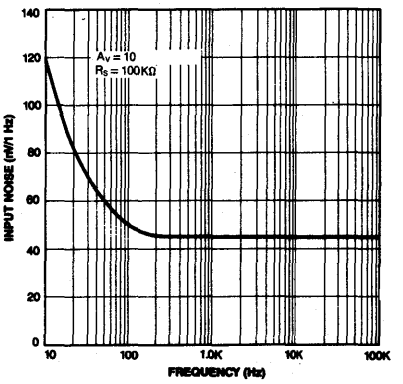


Fig. 5 OPEN LOOP FREQUENCY RESPONSE

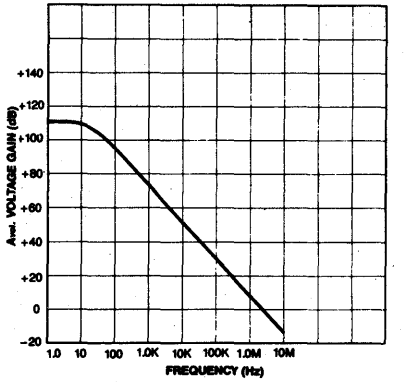


Fig. 6 PHASE MARGIN vs FREQUENCY

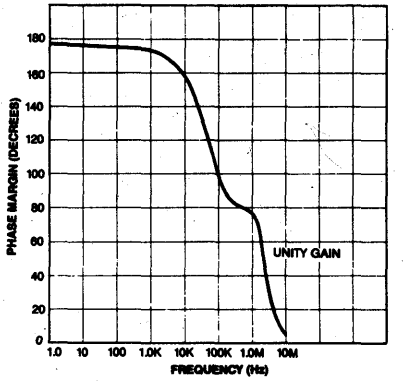


Fig. 7 POSITIVE OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

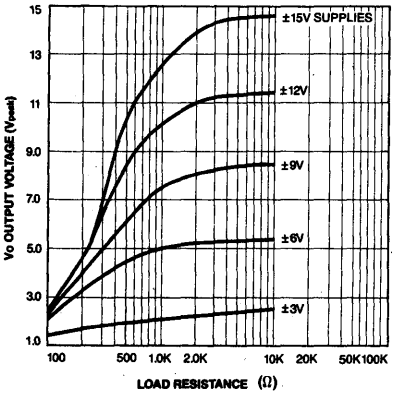


Fig. 8 NEGATIVE OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

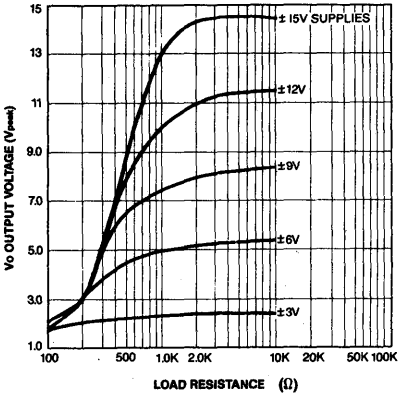


Fig. 9 POWER BANDWIDTH (LARGE SIGNAL SWING VERSUS FREQUENCY)

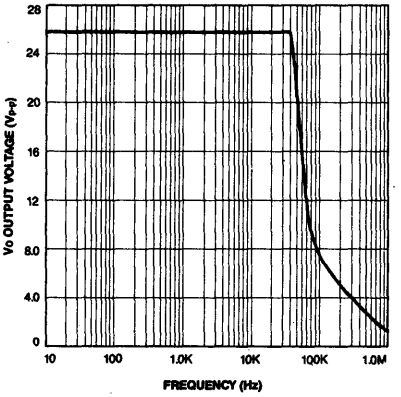
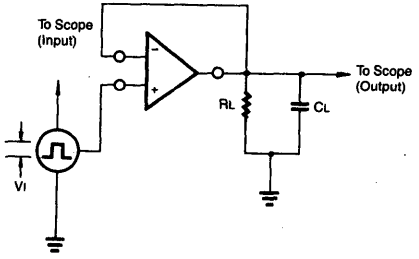


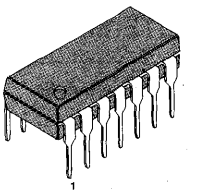
Fig. 10 TRANSIENT RESPONSE TEST CIRCUIT



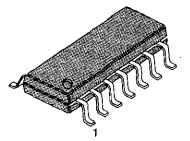
DUAL HIGH SPEED VOLTAGE COMPARATOR

The KA219 is a dual high speed voltage comparator designed to operate from a single +5V supply up to ±15V dual supplies.
Open collector of the output stage makes the KA219 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25mA. Typical response time of 80ns with ±15V power supplies makes the KA219 ideal for application in fast A/D converts, level shifters, oscillaters, and multivibrators.

14 DIP



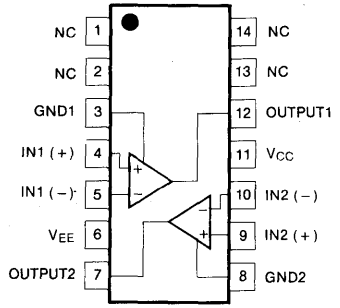
14 SOP



FEATURES

- **Operates form a single 5V supply**
- **Typically 80ns response time at ±15V**
- **Open collector outputs: up to +35V**
- **High output drive current: 25mA**
- **Inputs and outputs can be isolated from system ground**
- **Minimum fan-out of 2 (each side)**
- **Two independent compators**

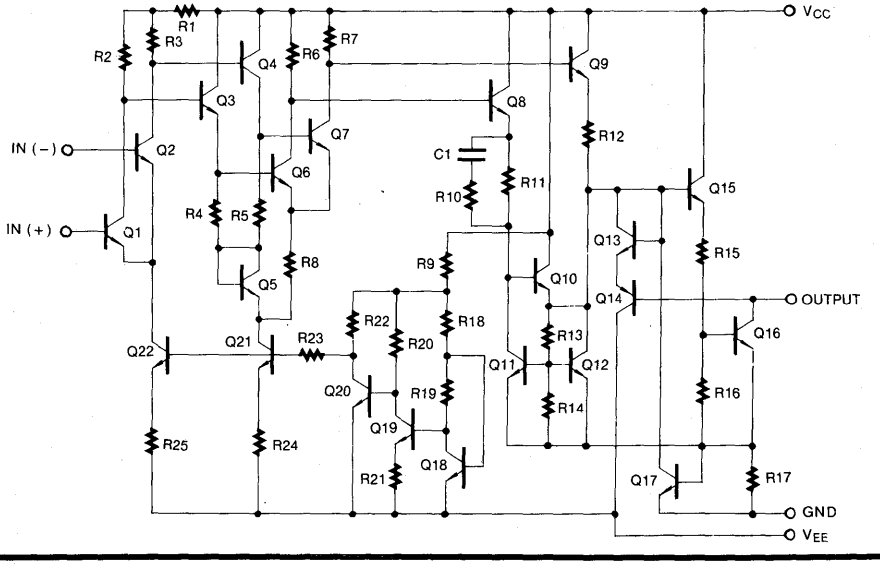
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KA319N	14 DIP	0 ~ +70°C
KA319D	14 SOP	
KA219N	14 DIP	−25 ~ +85°C
KA219D	14 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_S	36	V
Output to Negative Supply Voltage	$V_O - V_{EE}$	36	V
Ground to Negative Supply Voltage	$GND - V_{EE}$	25	V
Ground to Positive Supply Voltage	$GND - V_{CC}$	18	V
Differential Input Voltage	V_{ID}	±5	V
Input Voltage	V_I	±15	V
Output Short Circuit Duration		10	sec
Power Dissipation	P_D	500	mW
Operating Temperature Range 219	T_{opr}	−25 ~ +85	°C
319		0 ~ +70	
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		KA219			KA319			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 1)	V_{IO}	$R_S \leq 5K\Omega$			0.7	4.0		2.0	8.0	mV
			Note 3			7.0			10	
Input Offset Current (Note 1)	I_{IO}				10	75		10	200	nA
			Note 3			100			300	
Input Bias Current	I_{IB}				150	500		250	1000	nA
			Note 3			1000			1200	
Voltage Gain	A_V			10	40		8	40		V/mV
Response Time (Note 2)	t_r	V_S = ±15V			80			80		ns
Saturation Voltage	V_{OL}	$V_{in} \leq -5mV$, I_o = 25mA			0.6	1.5				V
		$V_{in} \leq -10mV$, I_o = 25mA						0.6	1.5	V
		$V_{CC} \geq 4.5V$, V_{EE} = 0V $V_{in} \leq -6mV$, $I_{sink} \leq 3.2mA$			0.23	0.4				V
		$V_{CC} \geq 4.5V$, V_{EE} = 0V $V_{in} \leq -10mV$, $I_{sink} \leq 3.2mA$						0.3	0.4	V
Output Leakage Current	I_{OL}	$V_{in} \geq 5mV$, V_O = 35V			0.2	2				μA
			Note 3		1	10				
		$V_{in} \geq 10mV$, V_O = 35V						0.2	10	μA
Input Voltage Range	V_{ICR}	Note 3	V_S = ±15V		±13			±13		V
			V_{CC} = 5V, V_{EE} = 0V	1		3	1		3	

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA219			KA319			Unit
			Min	Typ	Max	Min	Typ	Max	
Differential Input Voltage	V_{ID}		±5			±5			V
Positive Supply Current	I_{CC1}	V_{CC}=5V, V_{EE}=0V		3.6			3.6		mA
Positive Supply Current	I_{CC2}	V_S = ±15V		7.5	11.5		7.5	12.5	mA
Negative Supply Current	I_{EE}	V_S = ±15V		3	4.5		3	5	mA

Note: 1. The offset voltage and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impeance.

2. The response time specified is for a 100mV input step with 5mV overdrive.

Note 3. KA319: $0 \leq Ta \leq +70°C$

KA219: $-25 \leq Ta \leq +85°C$

4

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 INPUT CURRENT

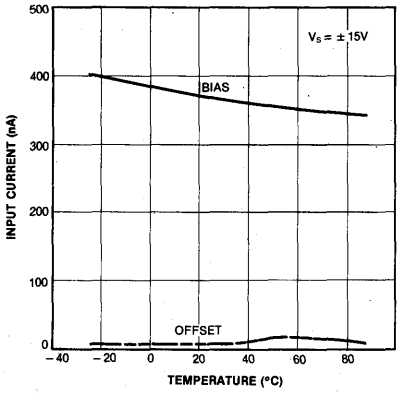


Fig. 2 OUTPUT SATURATION VOLTAGE

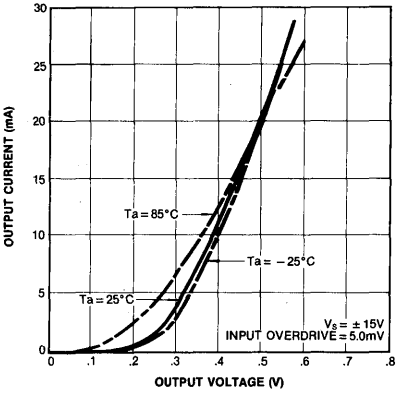


Fig. 3 TRANSFER FUNCTION

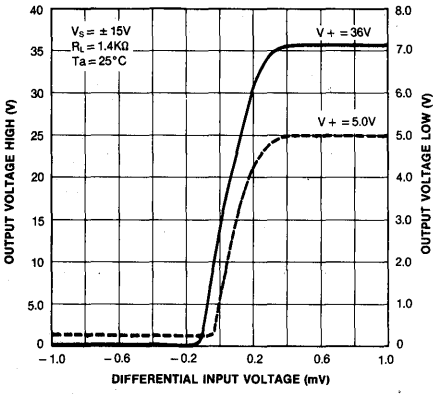


Fig. 4 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVER

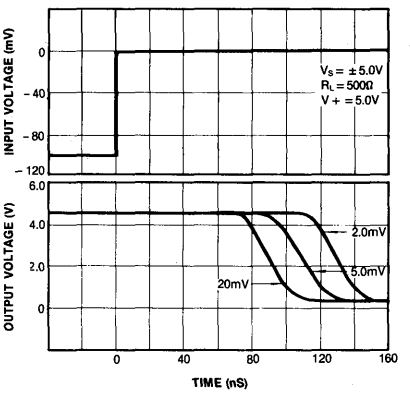


Fig. 5 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVER

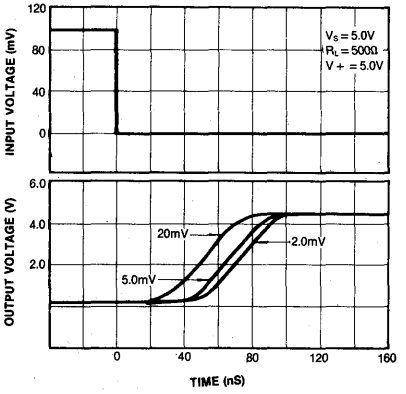


Fig. 6 INPUT CHARACTERISTICS

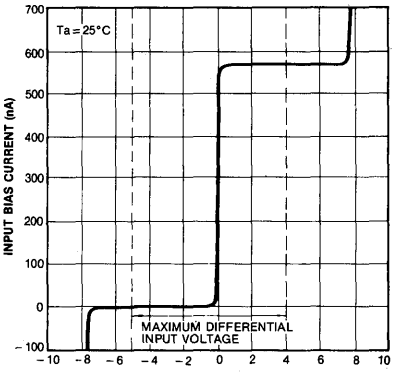


Fig. 7 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVER

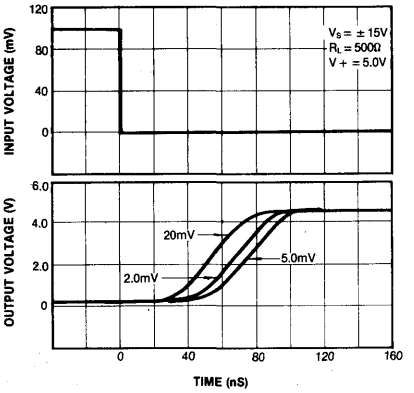


Fig. 8 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVER

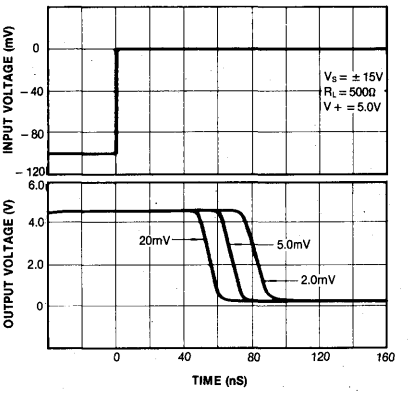


Fig. 9 SUPPLY CURRENT

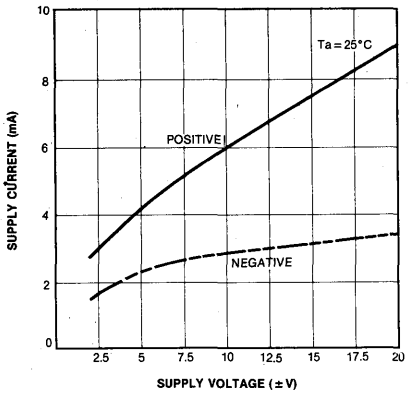


Fig. 10 SUPPLY CURRENT

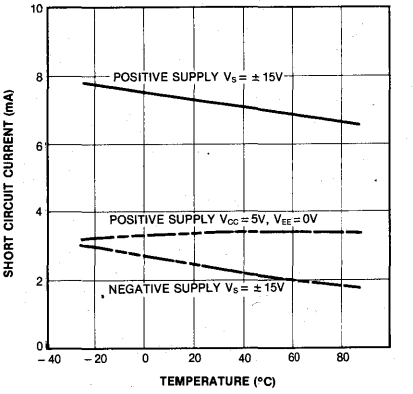


Fig. 11 COMMON MODE LIMITS

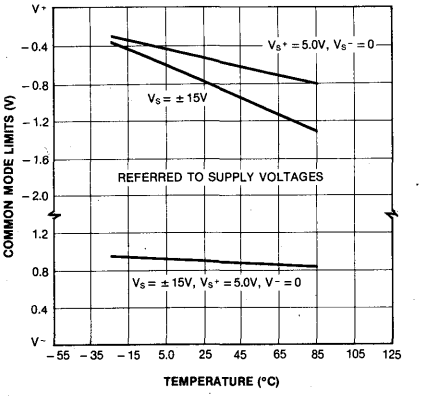
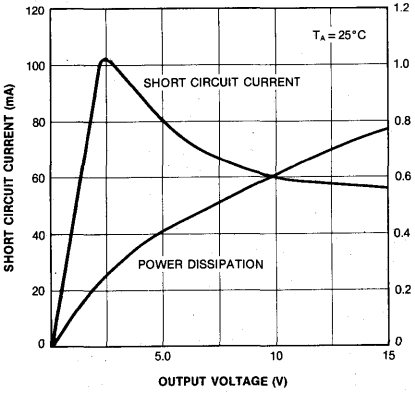
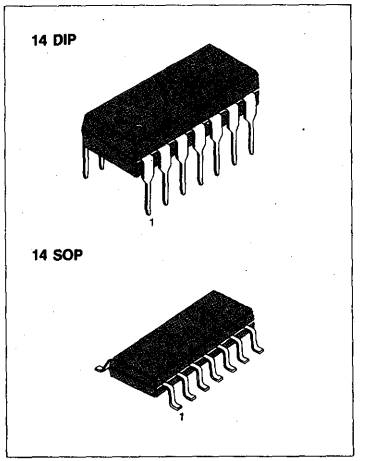


Fig. 12 OUTPUT LIMITING CHARACTERISTICS



HIGH SPEED VOLTAGE COMPARATOR

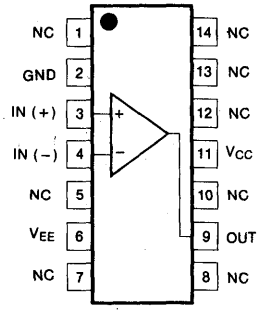
The KA710C/I is a high speed voltage comparator intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance.
The output of the comparator is compatible with all intergrated logic forms.
The KA710C/I is useful as pulse height disciminators, a variable threshold schmitt trigger, voltage comparators in high-speed A/D converters, a memory sense amplifier or a high noise immunity line receiver.



FEATURES

- **Low offset voltage: 5mV**
- **High gain: 1000 V/V**
- **High speed: 40ns Typ**

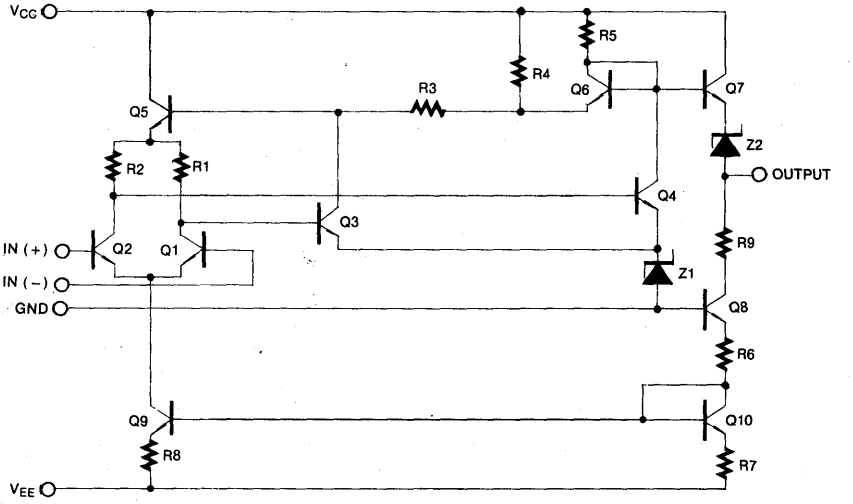
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operation Temperature
KA710CN	14 DIP	0 ~ +70°C
KA710CD	14 SOP	
KA710IN	14 DIP	−25 ~ +85°C
KA710ID	14 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	+14	V
Negative Supply Voltage	V_{EE}	−7	V
Peak Output Current	I_{peak}	10	mA
Output Short Circuit Duration		10	Sec
Differential Input Voltage	V_{ID}	±5	V
Input Voltage	V_I	±7	V
Power Dissipation	P_D	300	mW
Operating Temperature Range KA710C	T_{opr}	0 ~ +70	°C
KA710I		−25 ~ +85	
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} = +12V, V_{EE} = −6V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA710I			KA710C			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 200\Omega$, NOTE 1		0.6	2.0		1.6	5.0	mV
		Note 2			3.0			6.5	
Input Offset Current (Note 1)	I_{IO}	NOTE 1		0.75	3.0		1.8	5.0	μA
		Note 2		1.8	7.0			7.5	
Input Bias Current	I_{IB}			5.0	20		7.0	25	μA
		Note 2		27	45		25	40	
Large Signal Voltage Gain	A_V		1250	1800		1000	1700		V/V
		Note 2							
Input Voltage Range	V_{ICR}	V_{CC} = −7V	±5.0			±5.0			V
Common Mode Rejection Ratio	CMRR	$R_S \leq 200\Omega$, NOTE 2	80	95		70	94		dB
Differential Input Voltage Range	V_{IDR}		±5.0			±5.0			V
Positive Output Level	V_{OH}	$0 \leq I_O < 5mA$, $V_{in} \geq 5mV$	2.5	2.9	4.0	2.5	2.9	4.0	V
Negative Output Level	V_{OL}	$V_{in} \geq 5mV$	−1.0	−0.5	0	−1.0	−0.5	0	V
Output Sink Current	I_{sink}	V_O = 0V $V_{in} \geq 5mV$	2.0	2.2		1.6	2.2		mA
Positive Supply Current	I_{CC}	$V_O \leq 0V$		4.7	9.0		4.7	9.0	mA
Negative Supply Current	I_{EE}	V_O = 0V, V_{in} = +5mV		4.0	7.0		4.0	7.0	mA
Power Consumption	P_D	V_O = 0V, V_{in} = 10mV		80	150			150	mV
Response Time	t_r	(Note 3)		40			40		nS

Note 1: The input offset voltage and input offset current are specified for a logic threshold voltage as follows: For 710I, 1.65V at −25°C, 1.4V at +25°C, 1.15V at +85°C. For 710C, 1.5V at 0°C, 1.4V at +25°C, 1.2V at +70°C.

Note 2: KA710C: $0 \leq Ta \leq +70°C$
KA710I: $-25 \leq Ta \leq +85°C$

Note 3: The response time specified is a 100mV input step with 5mV overdrive (KA710I) or a 10mV overdrive (KA710C)

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

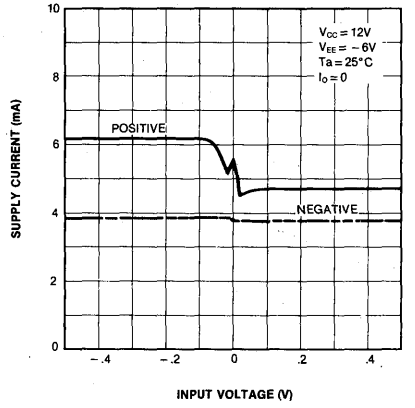


Fig. 2 VOLTAGE GAIN

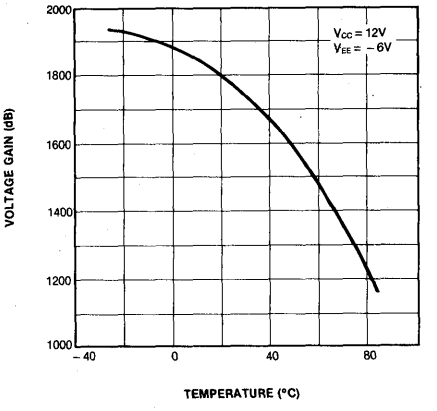


Fig. 3 INPUT OFFSET CURRENT

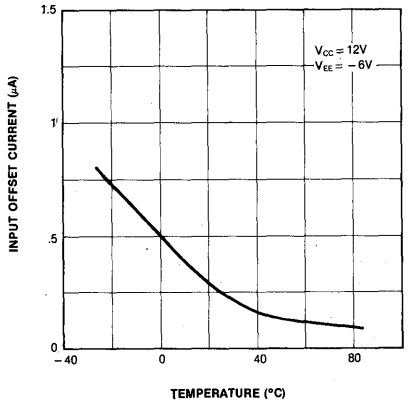


Fig. 4 INPUT BIAS CURRENT

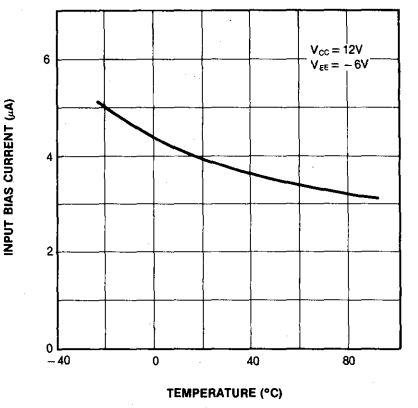


Fig. 5 OUTPUT VOLTAGE LEVEL

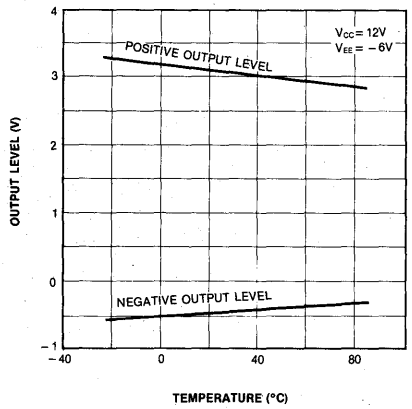


Fig. 6 OUTPUT SINK CURRENT

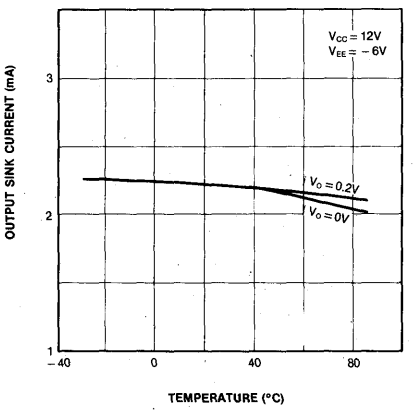


Fig. 7 RESPONSE TIME

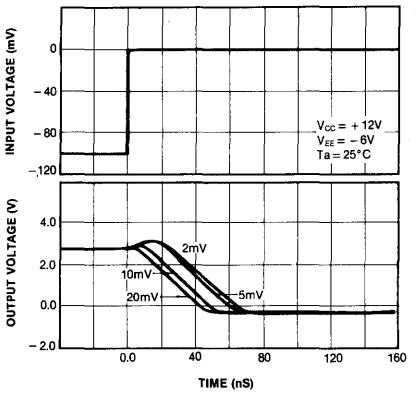
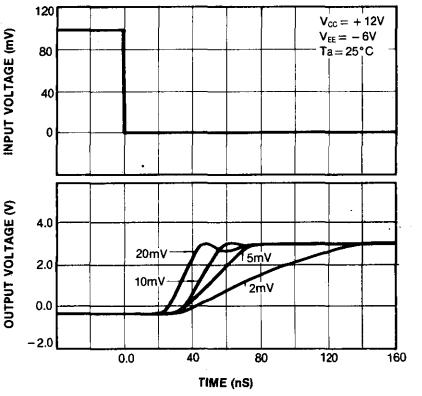


Fig. 8 RESPONSE TIME

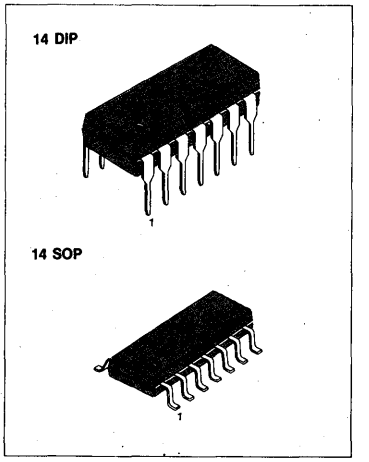


4

DUAL HIGH-SPEED DIFFERENTIAL COMPARATOR

The KA711C/I contain two voltage comparators with separate differential inputs, a common output and provision for strobing each side independently. The device features high accuracy, fast response, low offset voltage, a large input voltage range, low power consumption and compatibility with practically all integrated logic forms.

The KA711C/I can be used as a sense amplifier for core memories, and a dual comparator with OR'ed outputs is required, such as a double-ended limit detector.



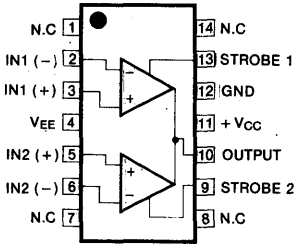
FEATURES

- **Fast response time: 40ns (Typ)**
- **Output compatible with most TTL circuits**
- **Independent strobing of each comparator**
- **Low offset voltage**

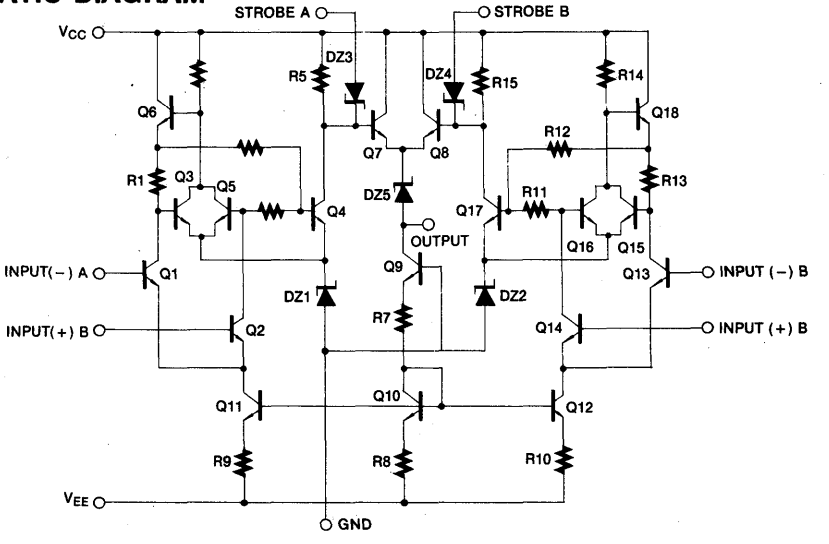
ORDERING INFORMATION

Device	Package	Operating Temperature
KA711CN	14 DIP	0 ~ +70°C
KA711CD	14 SOP	
KA711IN	14 DIP	−25 ~ +85°C
KA711ID	14 SOP	

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	+14	V
Negative Supply Voltage	V_{EE}	−7	V
Differential Input Voltage	V_{ID}	±5	V
Input Voltage	V_I	±7	V
Strobe Voltage	V_{st}	0 ~ 6	V
Peak Output Current	I_{peak}	50	mA
Continuous Total Power Dissipation	P_D	500	mW
Operating Temperature Range KA711C	T_{opr}	0 ~ +70	°C
KA711I		−65 ~ +150	
Storage Temperature Range	T_{stg}	−25 ~ +85	°C

ELECTRICAL CHARACTERISTICS

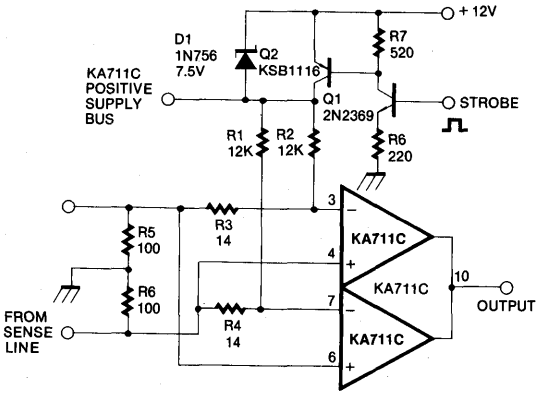
(V_{CC} = +12V, V_{EE} = −6V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA710I			KA711C			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 200\Omega$, $V_{CM} = 0V$		1.0	3.5		1.0	5.0	mV
		$V_{OUT} = 1.4V$ NOTE 2			4.5			6.0	
Input Offset Current	I_{IO}	$V_{OUT} = 1.4V$		0.5	10.0		0.5	15	μA
		NOTE 2			20			25	
Input Bias Current	I_{IB}			25	75		25	100	μA
		Ta = 0°C			150			150	
Large Signal Voltage Gain	A_V		750	1500		700	1500		V/V
		NOTE 2	500			500			
Input Voltage Range	V_{ICR}	$V_{EE} = -7.0V$	±5.0			±5.0			V
Differential Input Voltage Range	V_{IDR}		±5.0			±5.0			V
Output Resistance	R_O			200			200		Ω
Output Voltage (High)	V_{OH}	$V_{IN} \geq 10mV$		4.5	5.0		4.5	5.0	V
Output Voltage (Low)	V_{OL}	$V_{IN} \leq 10mV$	−1.0		0	−1.0	−0.5	0	V
Loaded Output High Level	V_{LOM}	$V_{IN} \geq 10mV$, $I_O = 5mA$	2.5	3.5		2.5	3.5		V
Strobed Output Level	V_{SO}	$V_{strobe} \leq 0.3V$	−1.0		0	−1.0		0	V
Output Sink Current	I_{sink}	$V_{IN} \geq 10mV$, $V_O \geq 0V$	0.5	0.8		0.5	0.8		mA
Positive Supply Current	I_{CC}	$V_O = 0V$, $V_{IN} = 10mV$		8.6			8.6		mA
Negative Supply Current	I_{EE}	$V_O = 0V$, $V_{IN} = 10mV$		3.9			3.9		mA
Strobe Current	I_{st}	$V_{strobe} = 100mV$		1.2	2.5		1.2	2.5	mA
Power Consumption	P_D	$V_O = 0V$, $V_{IN} \geq 10mV$		130	200		130	230	mW
Response Time	t_r	(NOTE 1)		40			40		ns
Strobe Release Time	t_{rs}			12			12		ns

Note: 1. The response time specified is for a 100mV input step with 10mV overdrive (LM710) or 0.1mV overdriver (KA710C).
2. KA711C: $0 \leq Ta \leq +70°C$
KA711I: $-25 \leq Ta \leq +85°C$
3. The input offset voltage and input offset current are specified for a logic threshold voltage of 711I, 1.65V at −25°C, 1.4V at +25°C, 1.15V at +85°C, for 711C, 1.5V at 0°C, 1.4V at +25°C, 1.2V at +70°C.

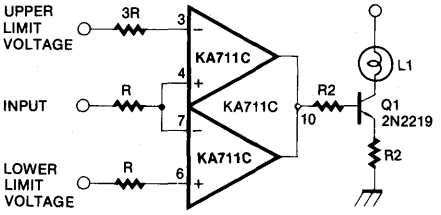
TYPICAL APPLICATIONS

Fig. 1 Sense Amplifier With Supply Strobing for Reduced Power Consumption*



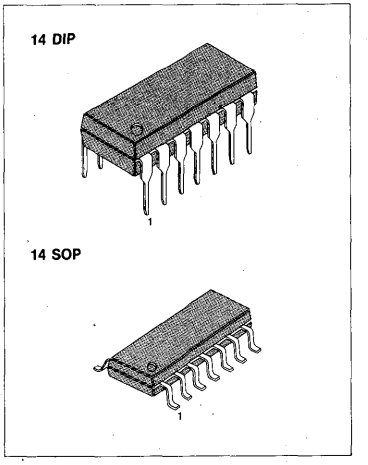
* Stanby dissipation is about 40mW

Fig. 2 Double-Ended Limit Detactor With Lamp Driver



QUAD DIFFERENTIAL COMPARATOR

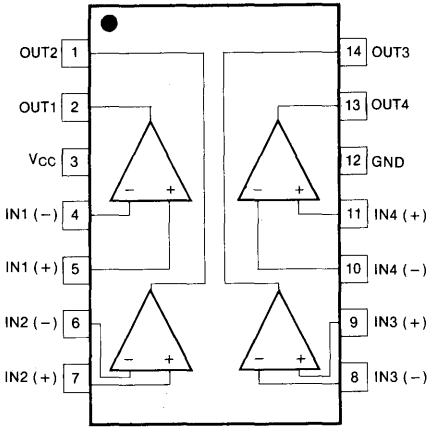
The LM239 series consists of four independent voltage comparators that one designed to operate from single power supply over a wide range of voltage.



FEATURES

- **Single or dual supply operation**
- **Wide range of supply voltages LM239/A, LM339/A: 2 ~ 36V**
  LM2901 ,(or ±1 ~ ±18V)
  LM3302: 2 ~ 28V
  (or ±1 ~ ±14V)
- **Low supply current drain 800μA Typ.**
- **Open collector outputs for wired and connectors**
- **Low input bias current 25nA Typ.**
- **Low input offset current ±2.3nA Typ.**
- **Low input offset voltage ±1.4mV Typ.**
- **Common mode input voltage range includes ground.**
- **Low output saturation voltage**
- **Output compatible with TTL, DTL and MOS logic system**

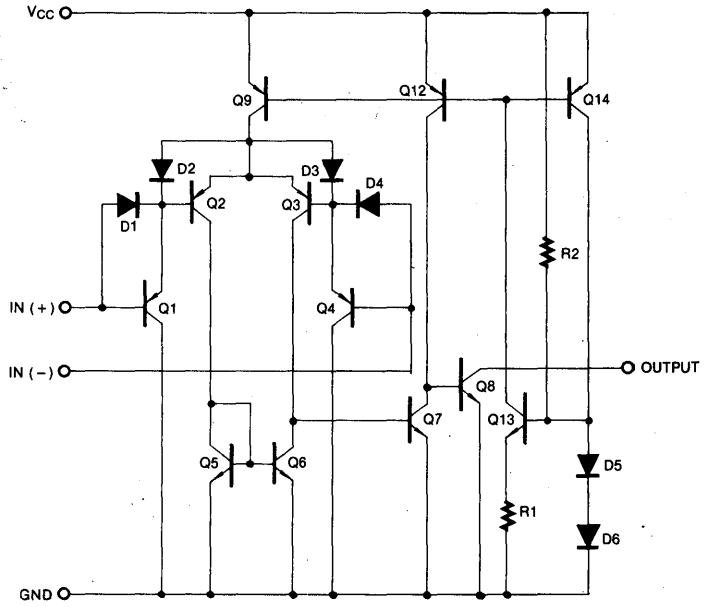
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
LM239N LM239AN	14 DIP	−25 ~ +85°C
LM239D LM239AD	14 SOP	
LM339N LM339AN	14 DIP	0 ~ 70°C
LM339D LM339AD	14 SOP	
LM2901N LM2901D LM3302N	14 DIP 14 SOP 14 DIP	−45 ~ +85°C

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_S	±18 or 36	V
Power Supply Voltage Only LM3302	V_S	±14 or 28	V
Differential Input Voltage	V_{ID}	36	V
Differential Input Voltage Only LM3302	V_{ID}	28	V
Input Voltage	V_I	−0.3 to +36	V
Input Voltage Only LM3302	V_I	−0.3 to +28	V
Output Short Circuit to GND		Continuous	
Power Dissipation	P_D	570	mW
Operating Temperature LM239/LM239A	T_{opr}	−25 ~ +85	°C
LM339/LM339A		0 ~ +70	°C
LM2901/LM3302		−40 ~ +85	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM239A/LM339A			LM239/LM339			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} − 1.5V			±1	±2		±1.4	±5	mV
		V_O = 1.4V, R_S = 0	NOTE 1			±4.0			±9.0	
Input Offset Current	I_{IO}				±2.3	±50		±2.3	±50	nA
			NOTE 1			±150			±150	
Input Bias Current	I_B				57	250		57	500	nA
			NOTE 1			400			400	
Input Common Mode Voltage Range	V_{ICR}			0		V_{CC}-1.5	0		V_{CC}-1.5	V
			NOTE 1	0		V_{CC}-2	0		V_{CC}-2	
Supply Current	I_{CC}		R_L = ∞		1.1	2.0		1.1	2.0	mA
Voltage Gain	A_{VOL}	V_{CC} = 15V, R_L ≥ 15KΩ (for large swing)		50	200		50	200		V/mV
Large Signal Response Time	t_{RES}	V_{IN} = TTL Logic Swing V_{ref} = 1.4V, V_{RL} = 5V, R_L = 5.1KΩ			350			350		ns
Response Time	t_{RES}	V_{RL} = 5V, R_L = 5.1KΩ			1.4			1.4		μs
Output Sink Current	I_{sink}	V_{IN}^- ≥ 1V, V_{IN}^+ = 0V, V_O ≤ 1.5V		6	18		6	18		mA
Output Saturation Voltage	V_{sat}	V_{IN}^- ≥ 1V, V_{IN}^+ = 0V			140	400		140	400	mV
		I_{sink} = 4mA	NOTE 1			700			700	
Output Leakage Current	I_{leak}	V_{IN}^- = 0	V_O = 5V		0.1			0.1		nA
		V_{IN}^+ = 1V	V_O = 30V			1.0			1.0	μA
Differential Voltage	V_{ID}		NOTE 1			36			36	V

* NOTE 1
LM339/A: 0 ≤ Ta ≤ + 70°C
LM239/A: − 25 ≤ Ta ≤ + 85°C
LM2901/3302: − 40 ≤ Ta < + 85°C

4

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM2901			LM3302			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} = 1.5V			2	7		2	20	mV
		V_O = 1.4V, R_S = 0	NOTE 1		9	15			40	
Input Offset Current	I_{IO}				2.3	50		3	100	nA
			NOTE 1		50	200			300	
Input Bias Current	I_B				57	250		57	500	nA
			NOTE 1		200	500			1000	
Input Common Mode Voltage Range	V_{ICR}			0		V_{CC}-1.5	0		V_{CC}-1.5	V
			NOTE 1	0		V_{CC}-2	0		V_{CC}-2	
Supply Current	I_{CC}		$R_L = \infty$,		1.1	2.0		1.1	2.0	mA
			$R_L = \infty$, V_{CC} = 30V		1.6	2.5				
Voltage Gain	A_{VOL}	V_{CC} = 15V, $R_L \geq 15K\Omega$ (for large swing)		25	100		2	30		V/mV
Large Signal Response Time	t_{REST}	V_{IN} = TTL Logic Swing V_{ref} = 1.4V, R_{RL} = 5V, R_L = 5.1KΩ			350			350		ns
Response Time	t_{RES2}	V_{RL} = 5V, R_L = 5.1KΩ			1.4			1.4		μs
Output Sink Current	I_{sink}	$V_{IN-} \geq 1V$, V_{IN+} = 0V, $V_O \leq 1.5V$		6	18		6	18		mA
Output Saturation Voltage	V_{sat}	$V_{IN-} \geq 1V$, V_{IN+} = 0V			140	400		140	400	mV
		I_{sink} = 4mA	NOTE 1			700			700	
Output Leakage Current	I_{leak}	V_{IN+} = 0	V_O = 5V		0.1			0.1		nA
		V_{IN+} = 1V	V_O = 30V			1.0			1.0	μA
Differential Voltage	V_{ID}		NOTE 1	0		36			28	V

NOTE 1 LM339/A: $0 \leq Ta \leq +70°C$
LM239/A: $-25 \leq Ta \leq +85°C$
LM2901/3302: $-40 \leq Ta < +85°C$

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

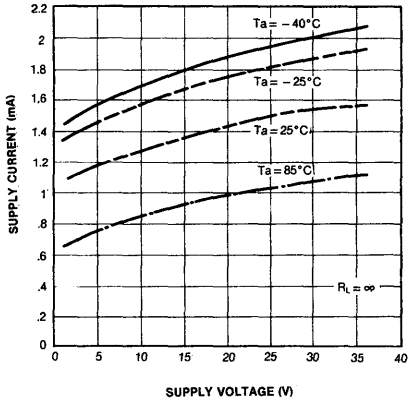


Fig. 2 INPUT CURRENT

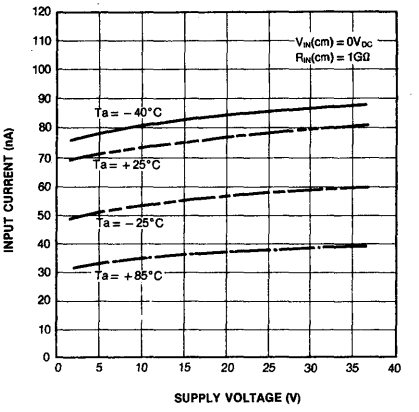


Fig. 3 OUTPUT SATURATION VOLTAGE

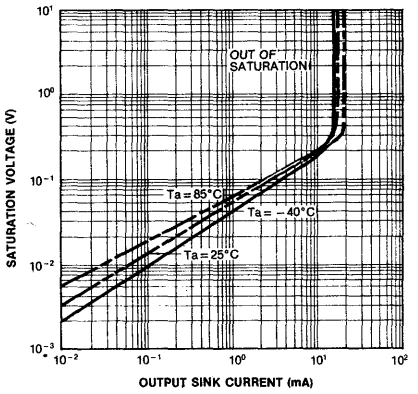


Fig. 4 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-NEGATIVE TRANSITION

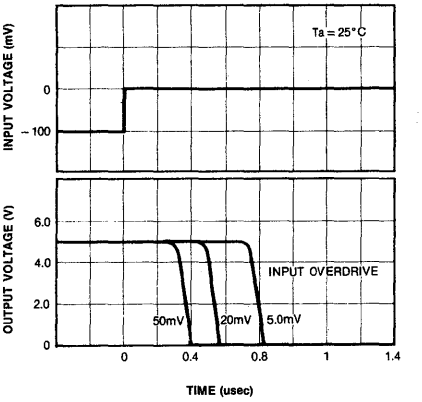
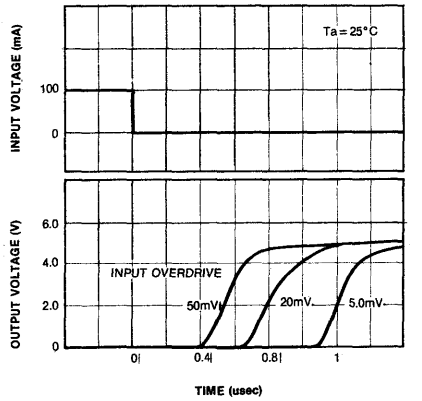


Fig. 5 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-POSITIVE TRANSITION



APPLICATION INFORMATION

The LM239 series includes four high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. That occurs during the output voltage transitions, when the comparator changes state.

To minimize this problem, PC board layout should be designed to reduce stray input output coupling; reducing the input resistors to less than 10KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.

It is good design practice to ground all unused pins.

The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than −0.3V should not be used: an input clamping diode can be used as protection.

The output LM339 is the uncommitted collector of a NPN transistor with grounded emitter. This allows the device to be used like any open-collector gate providing the OR-wide facility.

The output sink current capability is approximately 16 mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltage will rise very rapidly.

Under this limit, the output saturation voltageis limited by the approximatively 60Ω r_{sat} of the output transistor.

TYPICAL APPLICATIONS (V_{CC} = + 15V)

Fig. 6 Basic comparator

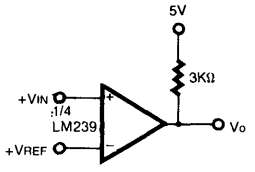


Fig. 7 Non-inverting comparator with Hysteresis

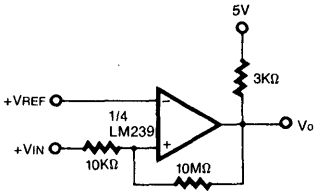


Fig. 8 Inverting comparator with Hysteresis

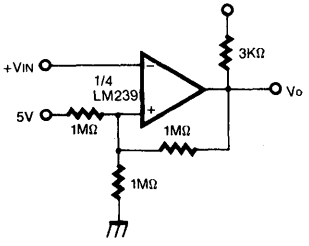


Fig. 9 Driving C/MOS

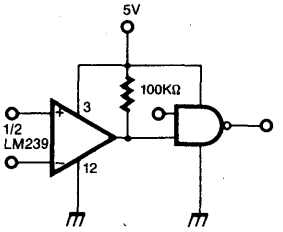


Fig. 10 Driving TTL

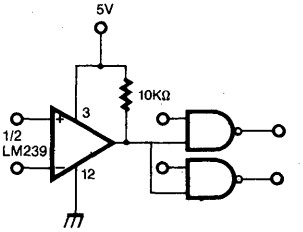


Fig. 11 AND gate

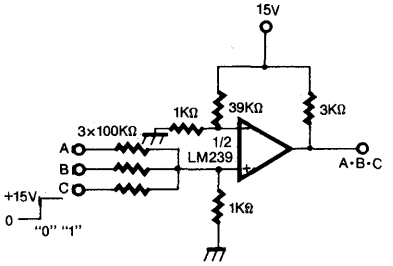


Fig. 12 OR gate

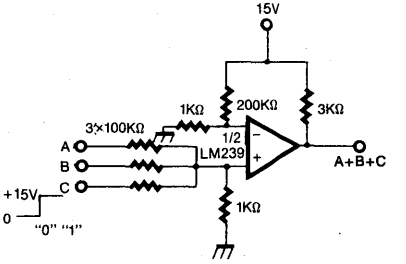


Fig. 13 Large fan-in AND gate

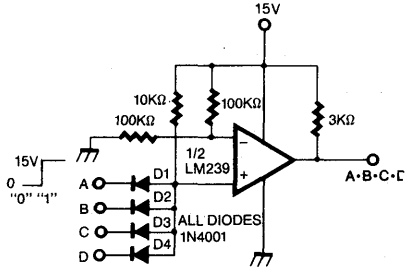


Fig. 14 Squarewave oscillator

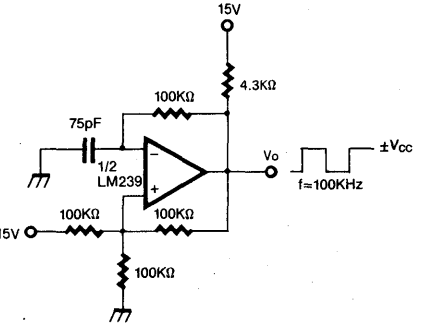


Fig. 15 ORing the outputs

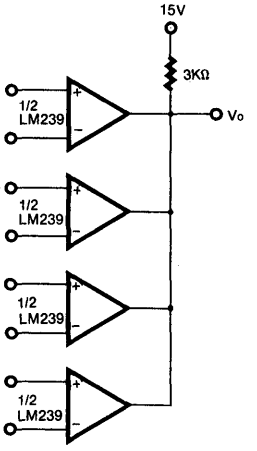


Fig. 16 Peak audio level display

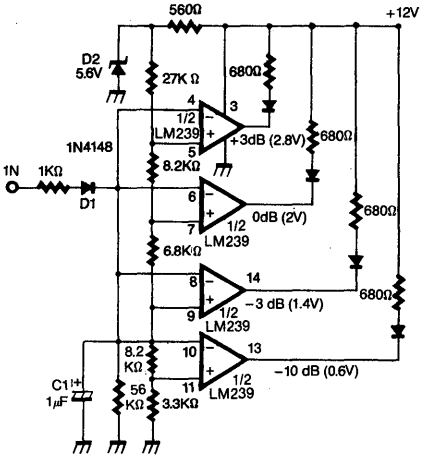


Fig. 17 Zero crossing detector (single supply)

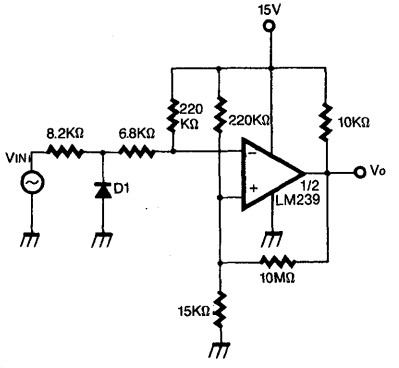
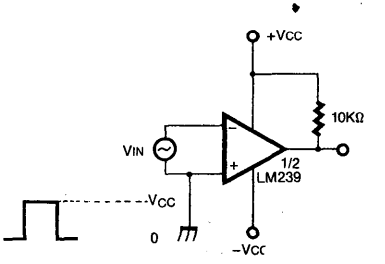


Fig. 18 Zero crossing detector (split supplies)

$V_{INmin} \approx 0.4V$ peak for 1% phase distortion ($\Delta\theta$)



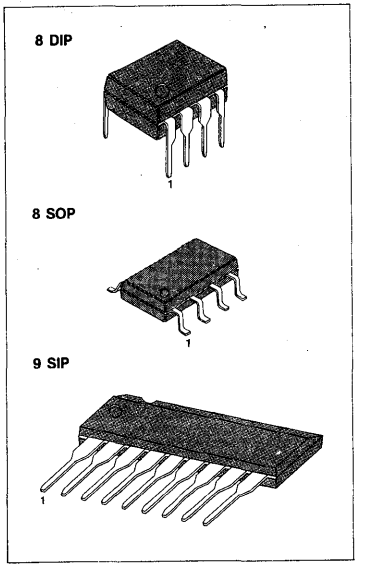
D1 prevents input from going negative by more than 0.6V:

$R1+R2=R3$

$R3 \leqslant R5/10$ for smaller error in zero crossing

DUAL DIFFERENTIAL COMPARATOR

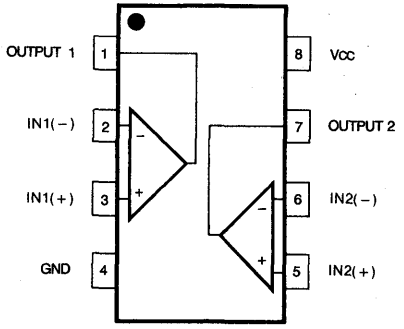
The LM293 series consists of two independent voltage comparators that one designed to operate from a single power supply over a wide range of voltage.

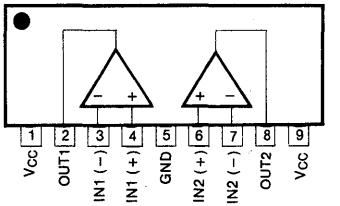


FEATURES

- **Single Supply Operation: 2V to 36V**
- **Dual Supply Operation: ±1V to ±18V**
- **Allow Comparison of Voltages Near Ground Potential**
- **Low Current Drain 800μA Typ**
- **Compatible with all Forms of Logic**
- **Low Input Bias Current 25nA Typ**
- **Low Input Offset Current ±5nA Typ**
- **Low Offset Voltage ±1mV Typ**

BLOCK DIAGRAM

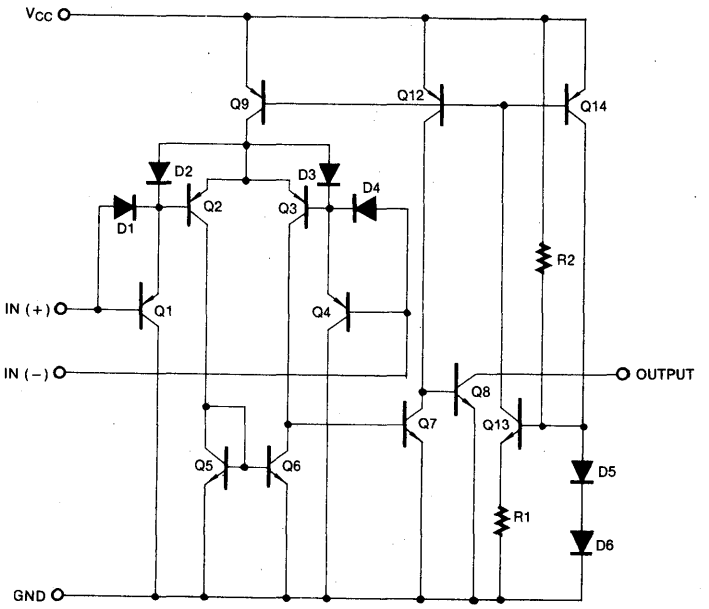




ORDERING INFORMATION

Device	Package	Operation Temperature
LM293N LM293AN	8 DIP	−25 ~ +85°C
LM293S LM293AS	9 SIP	
LM293D LM293AD	8 SOP	
LM393N LM393AN	8 DIP	0 ~ +75°C
LM393S M393AS	9 SIP	
LM393D LM393AD	8 SOP	
LM2903N	8 DIP	−40 ~ +85°C
LM2903D	8 SOP	
LM2903S	9 SIP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_S	±18 or 36	V
Differential Input Voltage	V_{ID}	36	V
Input Voltage	V_I	−0.3 to +36	V
Output Short Circuit to GND		Continuous	
Power Dissipation	P_D	570	mW
Operating Temperature LM293/LM293A LM393/LM393A LM2903	T_{opr}	 −25 ~ +85 0 ~ +70 −40 ~ +85	 °C °C °C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM293A/LM393A			LM293/LM393			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} − 1.5V, V_o = 1.4V, R_s = 0			±1	±2		±1	±5	mV
			NOTE 1			±4.0			±9.0	
Input Offset Current	I_{IO}				±5	±50		±5	±50	nA
			NOTE 1			±150			±150	
Input Bias Current	I_B				65	250		65	250	nA
			NOTE 1			400			400	
Input Common Mode Voltage Range	V_{ICR}			0		V_{CC}-1.5	0		V_{CC}-1.5	V
			NOTE 1	0		V_{CC}-2	0		V_{CC}-2	
Supply Current	I_{CC}	R_L = ∞			0.6	1		0.6	1	mA
		R_L = ∞ V_{CC} = 30V			0.8	2.5		0.8	2.5	
Voltage Gain	A_V	V_{CC} = 15V, R_L ≥ 15KΩ(for large V_o swing)		50	200		50	200		V/mV
Large Signal Response Time	t_{RES1}	V_{IN} = TTL Logic Swing, V_{ref} = 1.4V, V_{RL} = 5V, R_L = 5.1KΩ			350			350		nS
Response Time	t_{RES2}	V_{RL} = 5V, R_L = 5.1KΩ			1.4			1.4		μS
Output Sink Current	I_{sink}	V_{IN}^- ≥ 1V, V_{IN}^+ = 0V, V_o ≤ 1.5V		6	18		6	18		mA
Output Saturation Voltage	V_{sat}	V_{IN}^- ≥ 1V, V_{IN}^+ = 0V, I_{sink} = 4mA			160	400		160	400	mV
			NOTE 1			700			700	
Output Leakage Current	I_{leak}	V_{IN}^- = 0, V_{in}^+ = 1V	V_o = 5V		0.1			0.1		nA
			V_o = 30V			1.0			1.0	μA

NOTE 1
LM293/A: −25 ≤ Ta ≤ +85°C
LM393/A: 0 ≤ Ta ≤ +70°C
LM2903: −40 ≤ Ta ≤ +85°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM2903			Unit
				Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} − 1.5V, V_o = 1.4V, R_s = 0			± 1	± 7	mV
			NOTE 1		± 9	± 15	
Input Offset Current	I_{IO}				± 5	± 50	nA
			NOTE 1		± 50	± 200	
Input Bias Current	I_B				65	250	nA
			NOTE 1			500	
Input Common Mode Voltage Range	V_{ICR}			0		V_{CC}-1.5	V
			NOTE 1	0		V_{CC}-2	
Supply Current	I_{CC}	R_L = ∞			0.6	1	mA
		R_L = ∞ V_{CC} = 30V			1	2.5	
Voltage Gain	A_V	V_{CC} = 15V, R_L ≥ 15KΩ (for large V_o swing)		25	100		V/mV
Large Signal Response Time	t_{RES1}	V_{IN} = TTL Logic Swing, V_{ref} = 1.4V, V_{RL} = 5V, R_L = 5.1KΩ			350		nS
Response Time	t_{RES2}	V_{RL} = 5V, R_L = 5.1KΩ			1.5		μS
Output Sink Current	I_{sink}	V_{IN}^- ≥ 1V, V_{IN}^+ = 0V, V_o ≤ 1.5V		6	16		mA
Output Saturation Voltage	V_{sat}	V_{IN}^- ≥ 1V, V_{IN}^+ = 0V, I_{sink} = 4mA			160	400	mV
			NOTE 1			700	
Output Leakage Current	I_{leak}	V_{IN}^- = 0, V_{in}^+ = 1V	V_o = 5V		0.1		nA
			V_o = 30V			1.0	μA

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

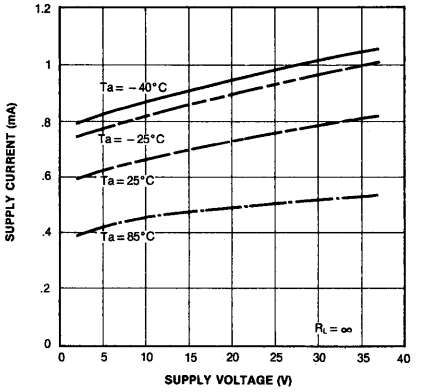
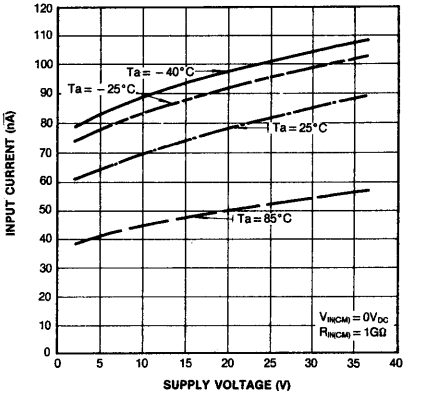


Fig. 2 INPUT CURRENT



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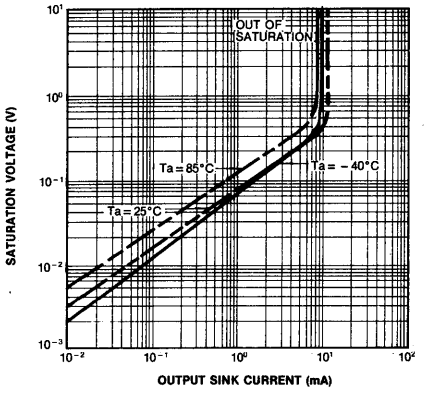

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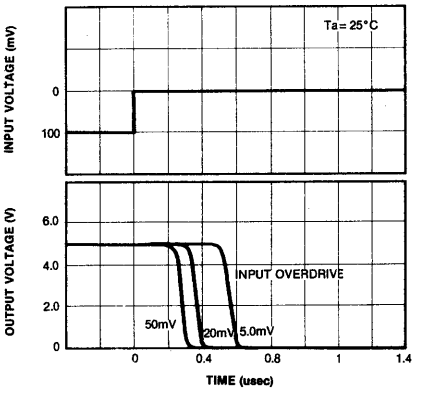
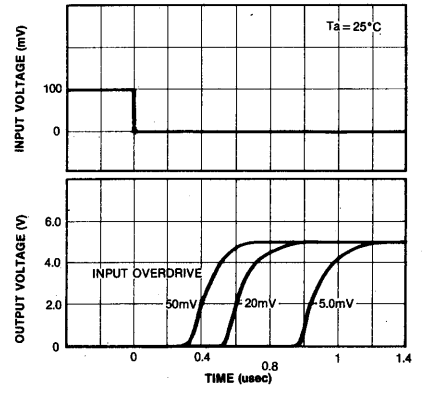


Fig. 5 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-POSITIVE TRANSITION



4

APPLICATION INFORMATION

The LM293 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output is inadvertently allowed to capacitively couple to the inputs via stray capacitance. That occurs during the output voltage transitions, when the comparator changes state.

To minimize this problem, PC board layout should be designed to reduce stray input-output coupling, reducing the input resistors to less than 10KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.

If is good design practice to ground all unused pins.

The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than −0.3V should not used: an input clamping diode can be used as protection.

The output of the LM239 series is the uncommitted collector of a NPN transistor with grounded emitter. The allows the device to be used like any open-collector gate providing the OR-wide facility.

The output sink current capability is approximately 16mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltate will rise very rapidly.
Under this limit, the output saturation voltage is limited by the approximatively 60Ω r_{sat} of the output transistor.

TYPICAL APPLICATIONS (V_{CC} = + 15V)

Fig. 6 Basic comparator

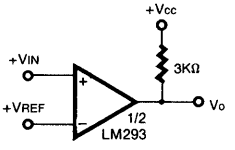


Fig. 7 Non-inverting comparator with Hysteresis

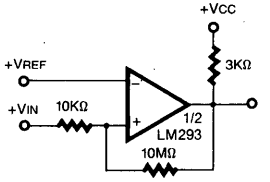


Fig. 8 Inverting comparator with Hysteresis

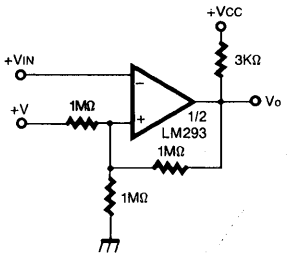


Fig. 9 Driving C-MOS

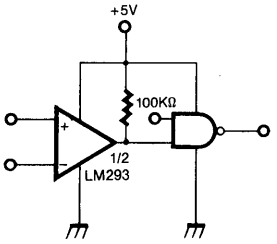
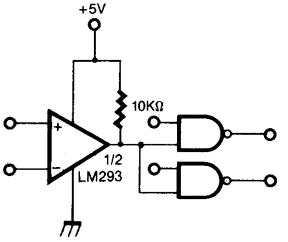


Fig. 10 Driving TTL



APPLICATION INFORMATION (continued)

Fig. 11 AND gate

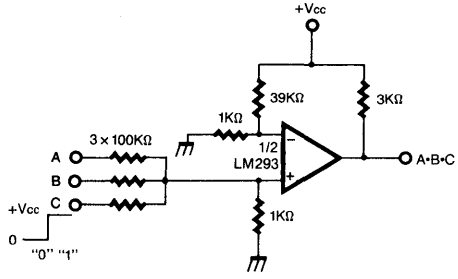


Fig. 12 OR gate

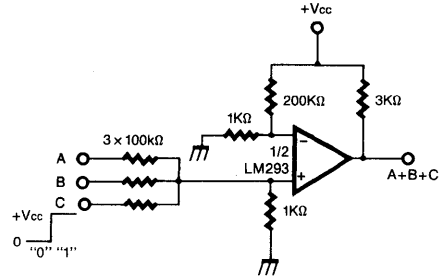


Fig. 13 Large fan-in AND gate

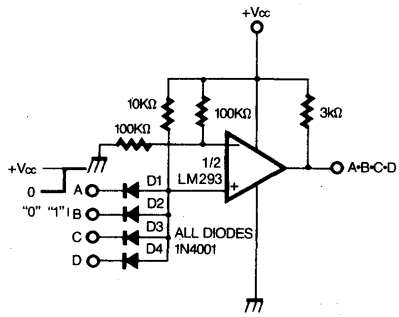


Fig. 14 Squarewave oscillator

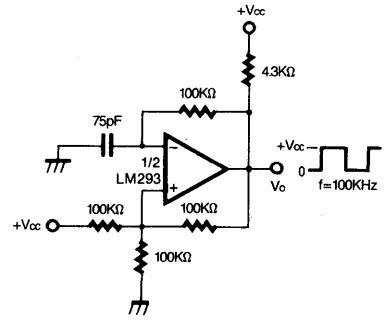


Fig. 15 Pulse generator

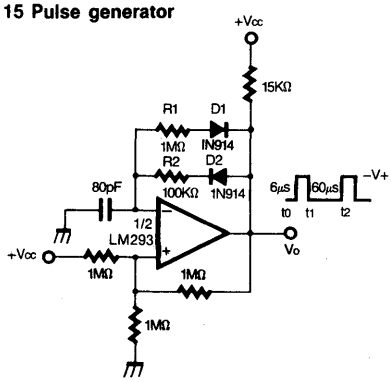
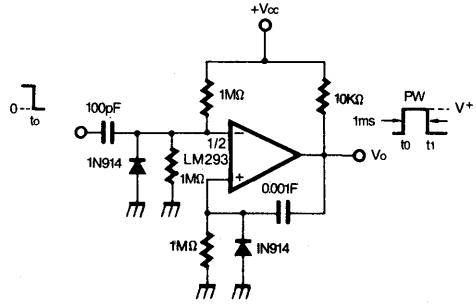


Fig. 16 One-shot multivibrator



4

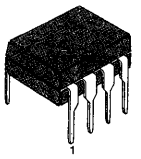
VOLTAGE COMPARATOR

The LM311 series is a monolithic, low input current voltage comparator.
The device is also designed to operate from dual or single supplies voltage.

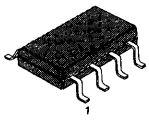
FEATURE

- **Low input bias current: 250nA (Max)**
- **Low input offset current: 50nA (Max)**
- **Differential Input Voltage: ±30V.**
- **Power supply voltage: single 5.0V supply to ±15V.**
- **Offset voltage null capability.**
- **Strobe capability.**

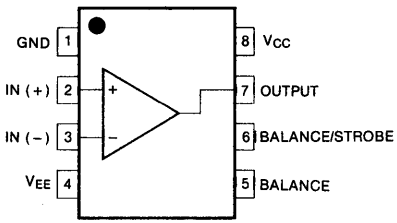
8 DIP



8 SOP



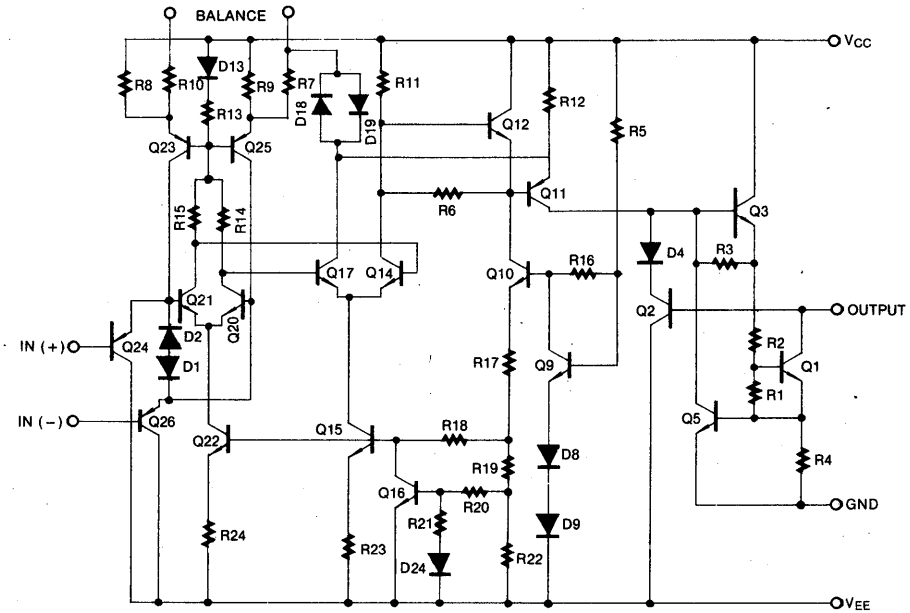
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operation Temperature
LM311N	8 DIP	0 ~ +70°C
LM311D	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Total Supply Voltage	V_S	36	V
Output to Negative Supply Voltage LM311	$V_O - V_{EE}$	40	V
Ground to Negative Supply Voltage	V_{EE}	30	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage	V_{IN}	±15	V
Output Short Circuit Duration		10	sec
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{opr}	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} = 15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 50K\Omega$		1.0	7.5	mV
		NOTE 1			10	
Input Offset Current	I_{IO}			6	50	nA
		NOTE 1			70	
Input Bias Current	I_{IB}			100	250	nA
		NOTE 1			300	
Voltage Gain	A_V		40	200		V/mV
Response Time	t_r	NOTE 2		200		nS
Saturation Voltage	V_{sat}	$I_O = 50mA$, $V_{IN} \leq -10mV$		0.75	1.5	
		$V_{CC} \geq 4.5V$, $V_{EE} = 0V$ $I_{sink} \leq 8mA$, $V_{IN} \leq -10mV$, NOTE 1		0.23	0.4	
Strove "ON" Current	I_S			3		mA
Output Leakage Current	I_{leak}	$I_{strobe} = 3mA$, $V_{IN} \geq 10mV$ $V_O = 35V$, $V_{EE} = V_{GND} = -5V$		0.2	50	nA
Input Voltage Range	V_{ICR}	NOTE 1	−14.5 to 13.0	−14.7 to 13.8		V
Positive Supply Current	I_{CC}			3.0	7.5	mA
Negative Supply Current	I_{EE}			−2.2	−5.0	mA
Strobe Current	I_{strobe}			3		mA

NOTE 1: $0 \leq T_A \leq +70°C$
NOTE 2: The response time specified is for a 100mV input step with 5mV over drive

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 INPUT BIAS CURRENT

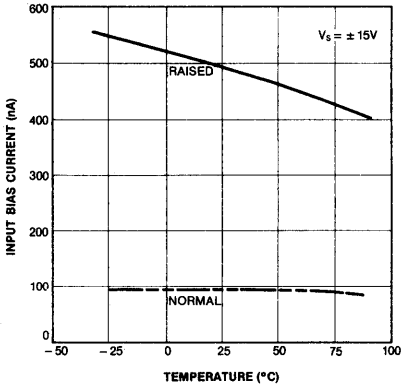


Fig. 2 INPUT OFFSET CURRENT

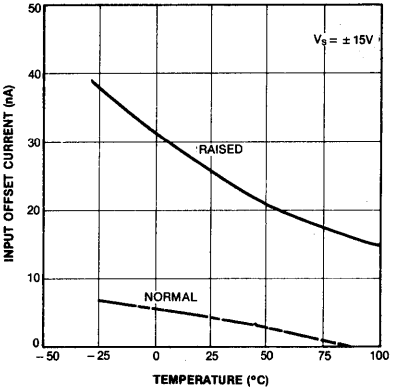


Fig. 3 OFFSET VOLTAGE V_S INPUT RESISTANCE

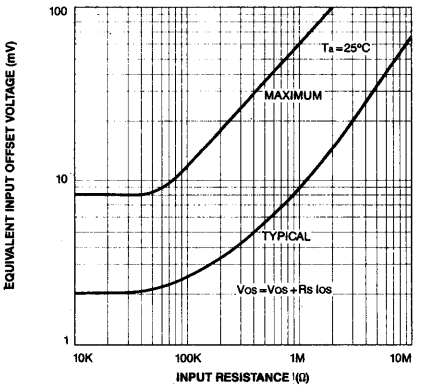


Fig. 4 INPUT BIAS CURRENT V_S DIFFERENTIAL INPUT VOLTAGE

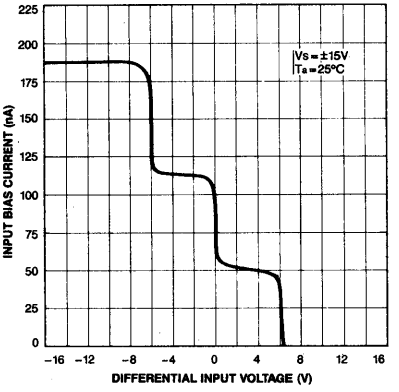


Fig. 5 COMMON MODE LIMITS V_S TEMPERATURE

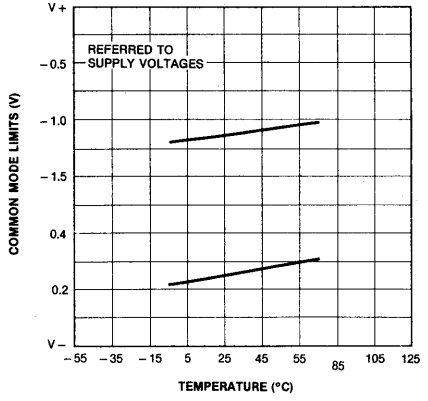


Fig. 6 OUTPUT VOLTAGE V_S DIFFERENTIAL INPUT VOLTAGE

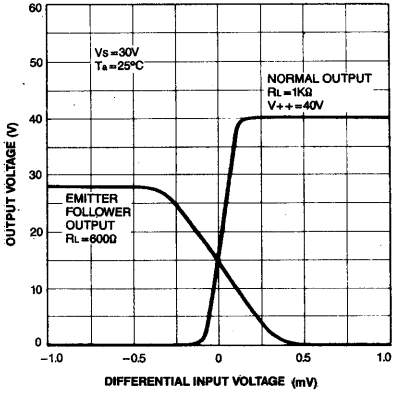


Fig. 7 SATURATION VOLTAGE V_S CURRENT

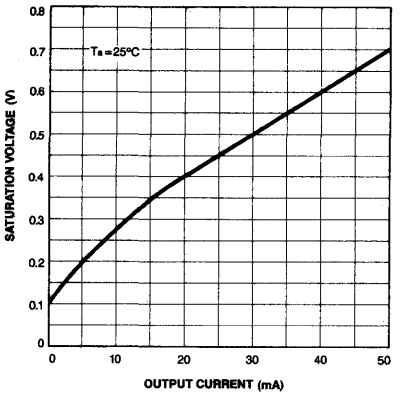


Fig. 8 SUPPLY CURRENT V_S TEMPERATURE

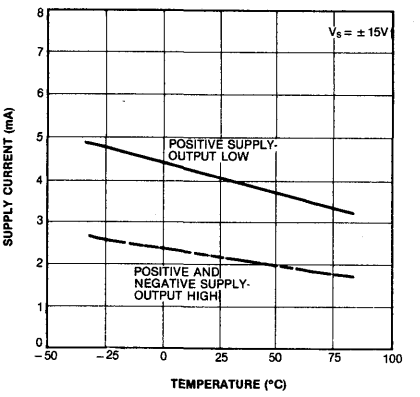


Fig. 9 LEAKAGE CURRENTS V_S TEMPERATURE

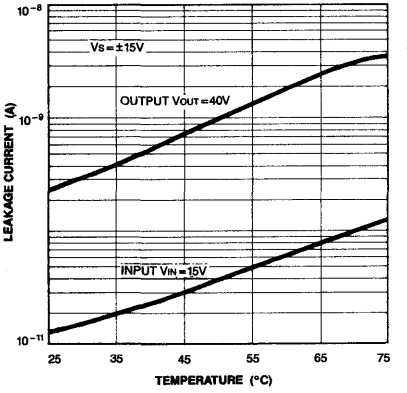


Fig. 10 SUPPLY CURRENT V_S SUPPLY VOLTAGE

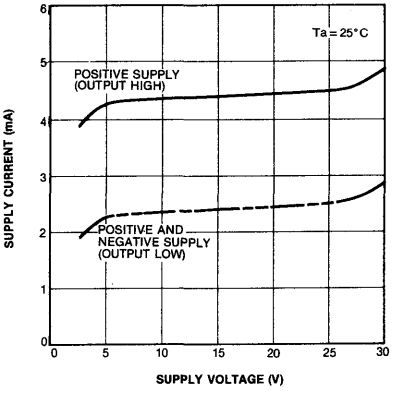


Fig. 11 OUTPUT SATURATION VOLTAGE

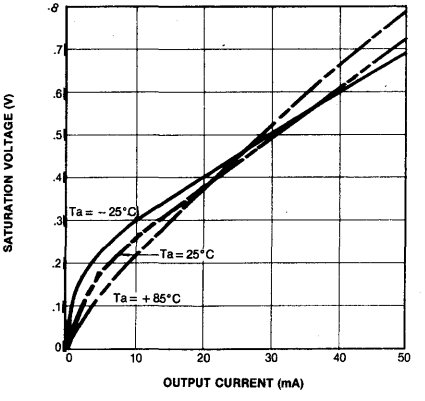
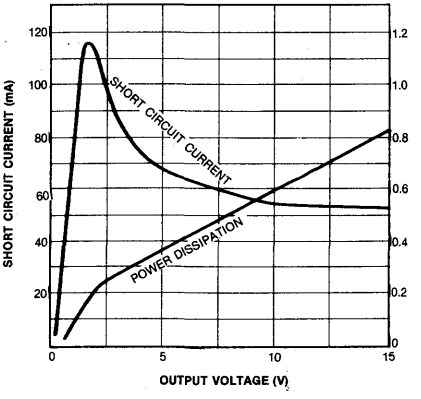


Fig. 12 OUTPUT LIMITING CHARACTERISTICS



4

TYPICAL APPLICATIONS

Fig. 1 Switching Power Amplifier

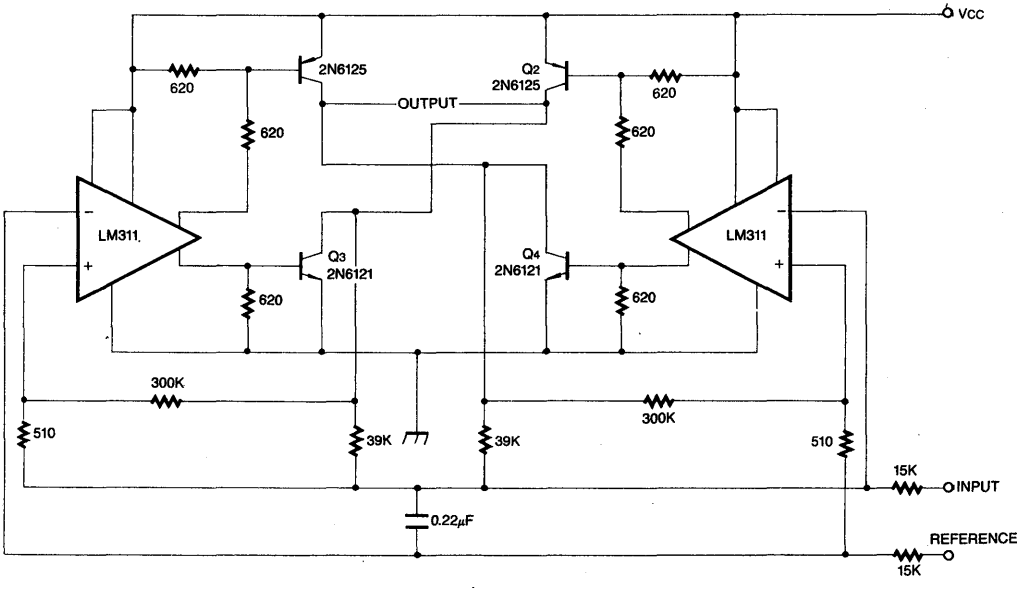


Fig. 2 Relay Driver with Strobe

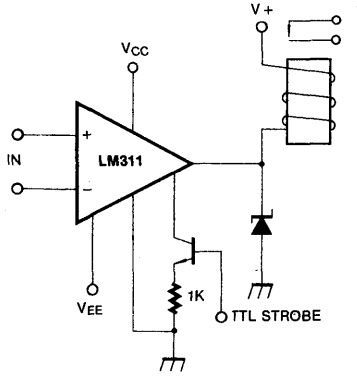
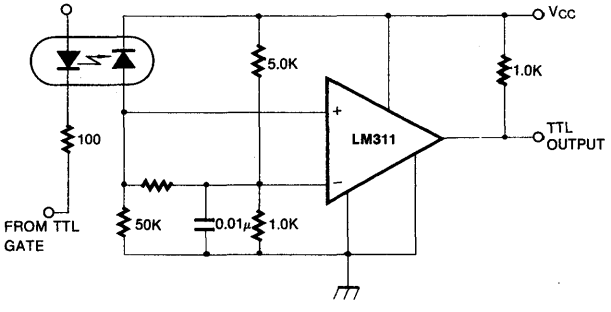


Fig. 3 Digital Transmission Isolator



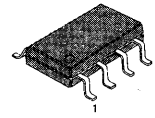
CMOS TIMER

The KS555 is CMOS timer with improved performance over the standard bipolar one. Due to its high-impedance inputs, it is capable of producing accurate time delays and oscillations with less expensive (smaller) timing capacitors than the standard bipolar timer.

Its dramatic advantages over bipolar ones are very low power consumption and wide operating voltage range especially stable low voltage operations.

8 DIP

8 SOP



FEATURES

- **Low power consumption**
- **Pin to pin operation with bipolar timer in most cases**
- **Extremely low trigger, threshold, and reset pin current**
- **High speed operation (500KHz)**
- **Stable low voltage operation (possible 1.5V operation with most samples)**
- **Wide operating voltage range: 2 to 18V**
- **High output source/sink driver meet TTL/CMOS**
- **Immunized to static charge with inner protection devices**

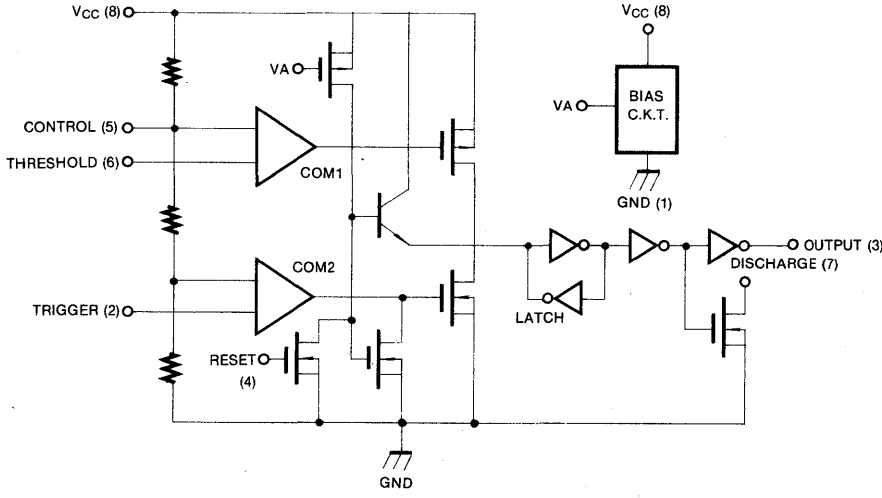
APPLICATIONS

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

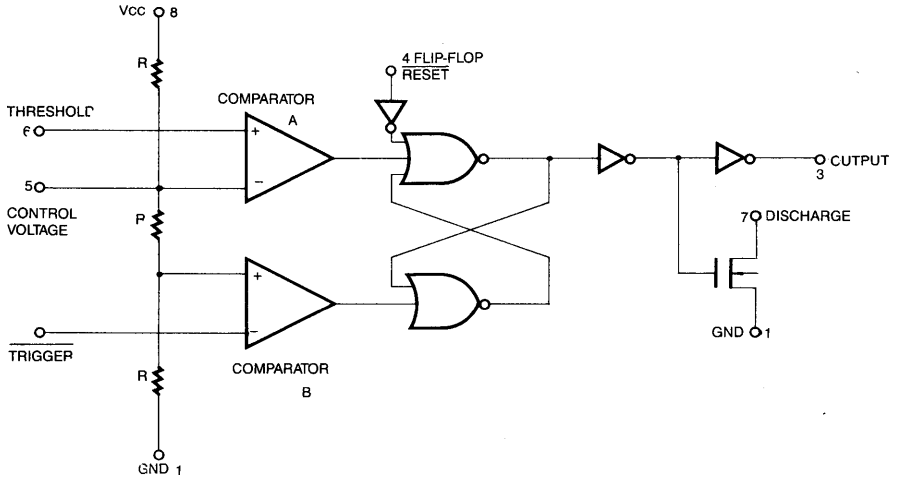
ORDERING INFORMATION

Device	Package	Operating Temperature
KS555N	8 DIP	−20 ~ +85°C
KS555D	8 SOP	

SCHEMATIC DIAGRAM



BLOCK DIAGRAM



This block diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs.
R = 100KΩ ± 20% Typ.

TRUTH TABLE

Threshold Voltage	Trigger Voltage	Reset	Output	Discharge Switch
Don't Care	Don't Care	Low	Low	On
> 2/3 (V_{CC})	> 1/3 (V_{CC})	High	Low	On
< 1/3(V_{CC}) ~ 2/3(V_{CC})	> 1/3(V_{CC}) ~ 2/3(V_{CC})	High	Stable	Stable
Don't Care	< 1/3 (V_{CC})	High	High	Off

Note: $\overline{\text{RESET}}$ will dominate all other input.$\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Input Volage (Trigger, Control Voltage, Threshold and Reset)	V_{IN}	− 0.3 V_{CC} + 0.3	V
Power Dissipation	P_D	200	mW
Operating Temperature Range	T_{opr}	− 20 ~ + 85	°C
Storage Temperature Range	T_{stg}	− 65 ~ + 150	°C

Note 1: Stresses above those listed under absolute maximum rating may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS

($T_a = 25°C$, $V_{CC} = 2$ to 15 Volts unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}	$-20°C < T_a < +70°C$	2		18	V
Supply Current	I_{CC}	$V_{CC} = 2V$		30		μA
		$V_{CC} = 18V$		60		μA
Timing Error Initial Accuracy	MT	$R_a = R_b = 1K\Omega$ to $100K\Omega$ $C = 0.1\mu F$, $5V \leq V_{CC} \leq 15V$		2.0	10.0	%
Drift With Temperature		$V_{CC} = 5V$		50		ppm/°C
		$V_{CC} = 10V$		75		ppm/°C
		$V_{CC} = 15V$		100		ppm/°C
Drift With Supply Voltage		$V_{CC} = 5V$		1.0	3.0	%/V
Threshold Voltage	V_{TH}	$V_{CC} = 5V$		0.66		V_{CC}
Trigger Voltage	V_{TR}	$V_{CC} = 5V$		0.33		V_{CC}
Trigger Current	I_{TR}	$V_{CC} = 18V$		50		pA
		$V_{CC} = 5V$		10		pA
		$V_{CC} = 2V$		1		pA
Threshold Current	I_{TH}	$V_{CC} = 18V$		50		pA
		$V_{CC} = 5V$		10		pA
		$V_{CC} = 2V$		1		pA
Reset Current	I_{RE}	$V_{RST} = GND$ $V_{CC} = 18V$		100		pA
		$V_{RST} = GND$ $V_{CC} = 5V$		20		pA
Reset Voltage	V_{RE}	$V_{CC} = 18V$	0.4	0.7	1.0	V
		$V_{CC} = 2V$	0.4	0.7	1.0	V
Control Voltage	V_C	$V_{CC} = 5V$		0.66		V_{CC}
Output Voltage Drop	V_{OL}	$V_{CC} = 18V$, $I_{SINK} = 3.2mA$		0.1	0.4	V
		$V_{CC} = 5V$, $I_{SINK} = 3.2mA$		0.15	0.4	V
	V_{OH}	$V_{CC} = 18V$, $I_{source} = 1.0mA$	17.25	17.8		V
		$V_{CC} = 5V$, $I_{source} = 1.0mA$	4.0	4.5		V
Rise Time of Output	T_r	$R_L = 10M\Omega$, $C_L = 10pF$, $V_{CC} = 5V$	35	40	75	ns
Fall Time of Output	T_f		35	40	75	ns
Guaranteed Max Osc. Freq.	F_{max}	Astable Operation	500			KHz

4

APPLICATION NOTES

General Description

The KS555 is CMOS timer and in most cases, may replace bipolar timer such as NE555 or SE555. Beside it is possible to reduce component counts. Because the bipolar device can produce a large crowbar currents in the output driver, it is necessary to decouple the power supply lines with good capacitor close to the device. The KS555 device produces no such transients. (See Fig. 1).

The KS555 produces supply current spikes of only 2-3mA instead of 300mA to 400mA and supply decoupling is normally not necessary, in most cases, the CONTROL VOLTAGE decoupling capacitors are required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved by using the KS555.

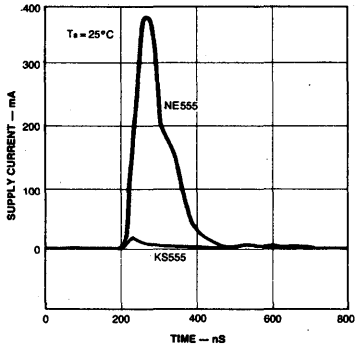


Fig 1. Supply current transient compared with a standard bipolar 555 during an output transition

Astable Operating

KS555 can free run as multi-vibrator by triggering itself. Refer to Fig. 2. The output can swing from V_{CC} to GND and have 50% duty cycle square wave. Less than 1% frequency deviation can be observed, over a voltage range of 2 to 5V. f = 1/1.4RC

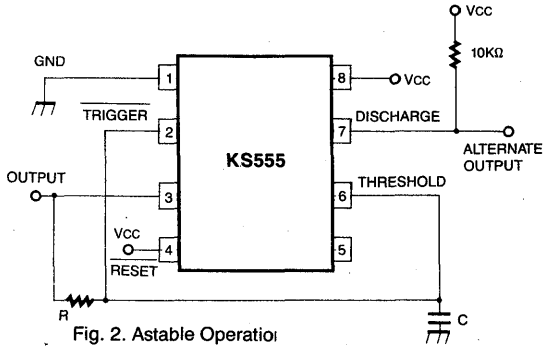


Fig. 2. Astable Operation

Monostable Operation

KS555 can be used as a one-shot, i.e. monostable multivibrator. Initially, because inside discharge transistor is on state, external timing capacitor is held to GND potential. Upon application of a negative TRIGGER pulse to pin 2, internal discharge transistor is off state and the voltage across the capacitor increases with time constant t = RaC and OUTPUT goes to high state. When the voltage across the capacitor equals 2/3 V_{CC} the inner comparator is reset by THRESHOLD input and discharge transistor goes to on state, which in turn discharge the capacitor rapidly and also drives the OUTPUT to its low state.

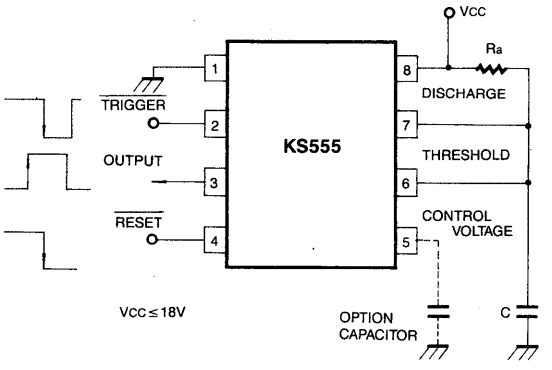
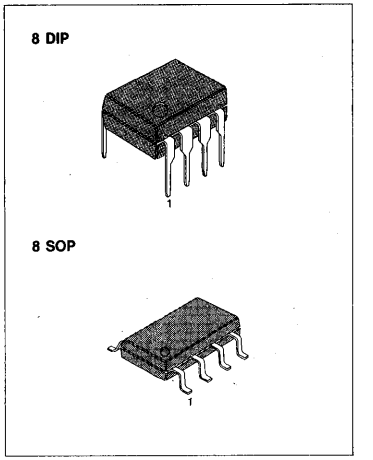


Fig. 3. Monostable Operation

CMOS TIMER

The KS555H is monolithic integrated circuit fabricated using CMOS process. Due to its high impedance inputs (threshold, trigger, reset), it is capable of producing accurate time delay and oscillation using less expensive, smaller timing capacitors than NE555.
Another features are very low power consumption and high speed astable operation and very low voltage operation.



FEATURES

- **Very low power consumption: 1.2mW**
- **Very high speed operation: 2MHz**
- **Complementary CMOS output capable of switching rail-to-rail**
- **Output fully CMOS-, TTL-, and MOS- compatible**
- **Exactly equivalent in most cases for NE555 or 556 (dual timer) or the 355**
- **Well behaved reset function**
- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **Highly immuned to static charge**

APPLICATIONS

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

ORDERING INFORMATION

Device	Package	Operation Temperature
KS555HN	8 DIP	0 ~ +70°C
KS555HD	8 SOP	
**KS555HIN	8 DIP	−25 ~ +85°C
**KS555HID	8 SOP	

** Under development

BLOCK DIAGRAM

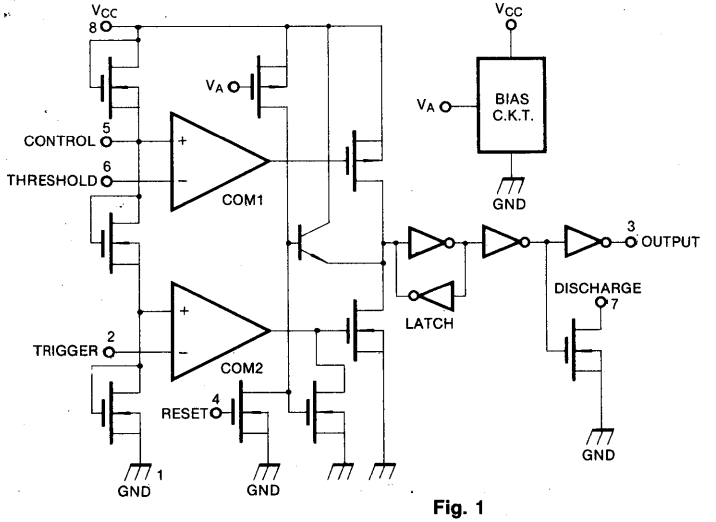


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Input Voltage (Trigger, Reset, Threshold)	V_{IN}	$-0.3 \sim V_{CC}$	V
Lead Temperature (Soldering 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_{opr}	$0 \sim +70$	°C
Storage Temperature Range	T_{stg}	$-65 \sim +150$	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5V, refer to application circuit unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		3		18	V
Supply Current	I_{CC}			140		μA
		V_{CC} = 15V		180		μA
Control Voltage	V_C			3.33		V
		V_{CC} = 15V		10		V
Threshold Voltage	V_{TH}			3.33		V
		V_{CC} = 15V		10		V
Threshold Current	I_{TH}	V_{CC} = 5V		50		PA
Trigger Voltage	V_{TR}			1.67		V
		V_{CC} = 15V		5		V
Trigger Current	I_{TR}			50		PA
Reset Voltage	V_{RE}			0.7	1	V
Reset Current	I_{RE}			50		PA
Low Level Output Voltage	V_{OL}	I_{OL} = 5mA		0.1		V
		I_{OL} = 8mA		0.15		V
		V_{CC} = 15V				
		I_{OL} = 10mA		0.1		V
		I_{OL} = 50mA		0.5		V
		I_{OL} = 100mA		1		V
High Level Output Voltage	V_{OH}	$I_{OH} = -1$mA		4.5		V
		$I_{OH} = -2$mA		4		V
		V_{CC} = 15V				
		$I_{OH} = -1$mA		14.8		V
		$I_{OH} = -5$mA		14		V
		$I_{OH} = -10$mA		12.7		V

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Initial Error of Timing Interval	T_{EI}	V_{CC} = 5 to 15V, $R_A = R_B$ = 1 to 100K, C_T = 0.1μF		1		%
Timing Error Due to Supply Drift	T_{ES}			0.1		%/V
Rise Time of Output	T_r	R_l = 10MΩ, C_l = 10pF		20		nS
Fall Time of Output	T_f			20		nS
Maximum Astable Oscillation	F_{MAX}	R_A = 470Ω, R_B = 200Ω, C_T = 200pF		2		MHz

APPLICATION CIRCUIT

1) ASTABLE

The circuit can be connected to trigger itself and free run as multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}.
As in the trigger mode, the charging and discharging times, and therefore the frequency are essentially independently of the supply voltage.
The frequency of oscillation is given by

$f = 1/T = 1.44/(R_A + 2 \times R_B)/C_T$

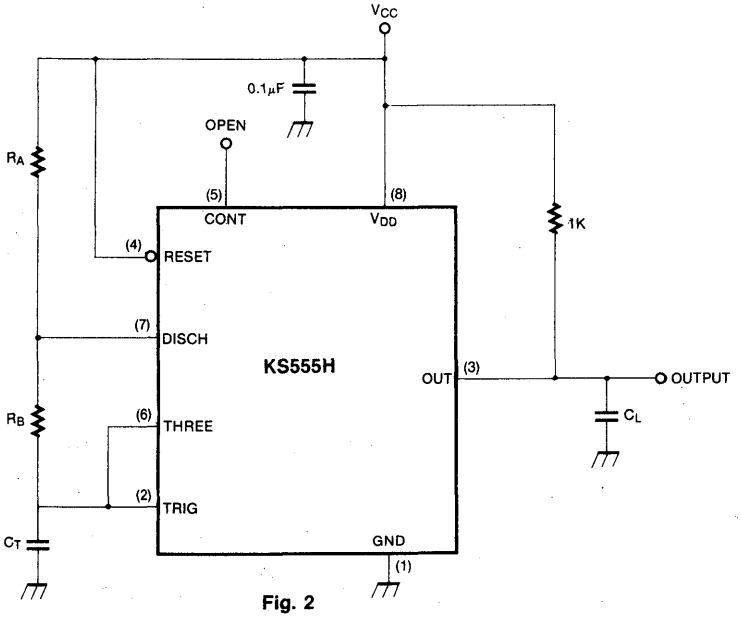


Fig. 2

2) MONOSTABLE

In this mode of operation, the timer functions as one shot. Initially, the external capacitor C is held discharged by a transistor inside timer. Upon application of negative trigger pulse to pin 2, the flip flop is set which releases the short circuit across the external capacitor and drives the output high.
The voltage across the external capacitor now increases exponentially with a time constant T = RA*C. When the voltage across the external capacitor equals 2/3*V_{CC}, the comparator resets the flip flop, which in turn discharges the capacitor repidly and also drives the output to its state.

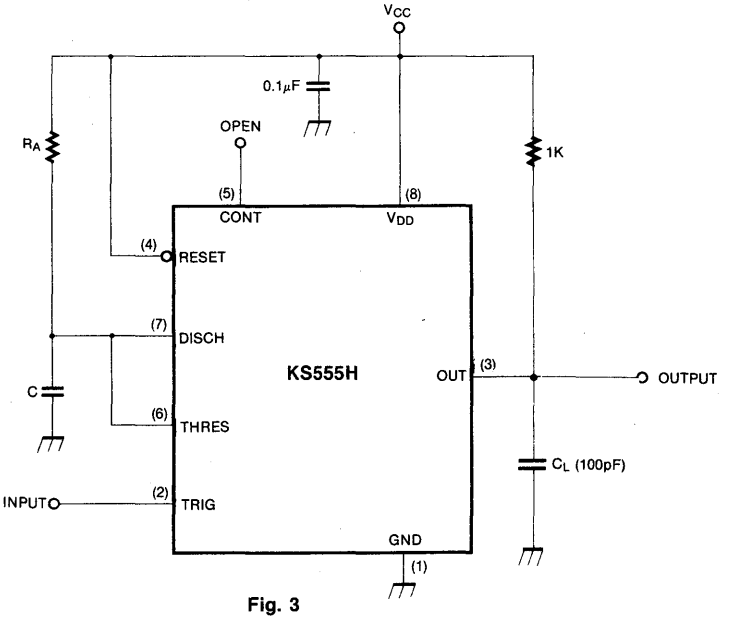


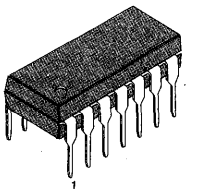
Fig. 3

CMOS TIMER

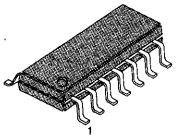
The KS556 is monolithic integrated circuit fabricated using C-MOS process. Due to high impedance inputs (Trigger, Threshold, Reset), it is capable of producing accurate time delay using less expensive, smaller timing capacitor than NE556.

Another features are one very low power consumption and high speed astable operation and very low voltage operation.

14 DIP



14 SOP



FEATURES

- **Very low power consumption: 2.4mW**
- **Very high speed operation: 2MHz**
- **Output fully CMOS, TTL, and MOS compatible**
- **Timing from microseconds through hours**
- **Adjustable duty cycle**

APPLICATIONS

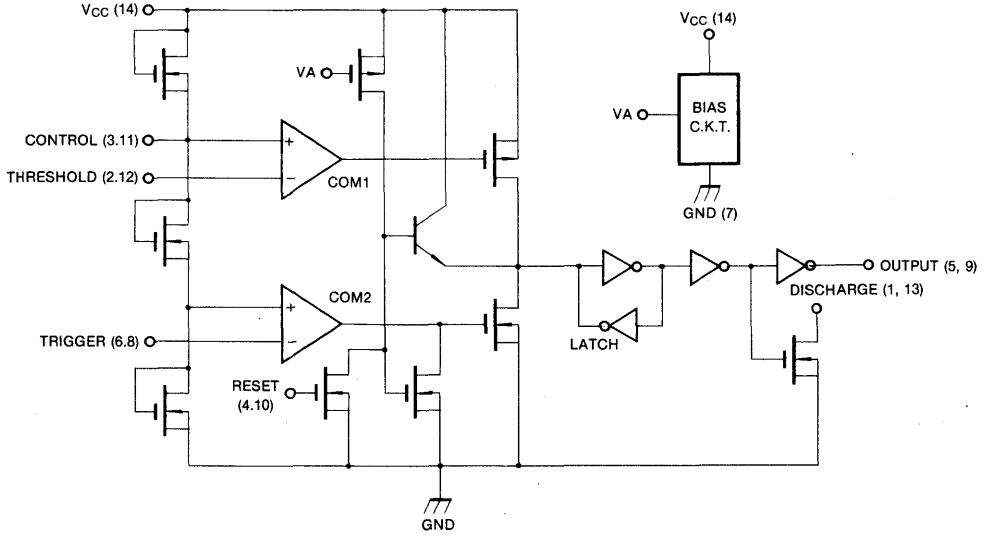
- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation

ORDERING INFORMATION

Device	Package	Operation Temperature
KS556N	14 DIP	0 ~ +70°C
KS556D	14 SOP	
**KS556IN	8 DIP	−25 ~ +85°C
**KS556ID	8 SOP	

** Under development

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Input Voltage (Trigger, Reset, Threshold)	V_{IN}	$-0.3 \sim V_{CC}$	V
Lead Temperature (Soldering 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_{opr}	$0 \sim +70$	°C
Storage Temperature Range	T_{stg}	$-65 \sim +150$	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5V, refer to application circuit unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		3		18	V
Supply Current	I_{CC}			240		μA
		V_{CC} = 15V		480		
Control Voltage	V_C			3.33		V
		V_{CC} = 15V		10		
Threshold Voltage	V_{TH}			3.33		V
		V_{CC} = 15V		10		
Threshold Current	I_{TH}			50		pA
Trigger Voltage	V_{TR}			1.67		V
		V_{CC} = 15V		5		
Trigger Current	I_{TR}			50		pA
Reset Voltage	V_{RE}			0.7	1	V
Reset Current	I_{RE}			50		pA
Low Level Output Voltage	V_{OL}	I_{OL} = 5mA		0.1		V
		I_{OL} = 8mA		0.15		
		V_{CC} = 15V I_{OL} = 10mA		0.1		
		V_{CC} = 15V I_{OL} = 50mA		0.5		
		V_{CC} = 15V I_{OL} = 100mA		1		
High Level Output Voltage	V_{OH}	I_{OH} = −1mA		4.5		V
		I_{OH} = −2mA		4		
		V_{CC} = 15V I_{OH} = −1mA		14.8		
		I_{OH} = −5mA		14		
		I_{OH} = −10mA		12.7		

ELECTRICAL CHARACTERISTICS (Continued)

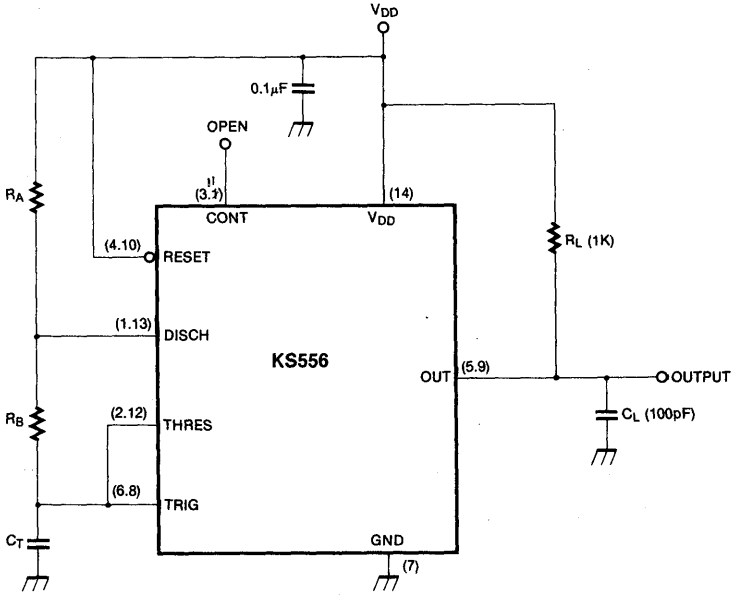
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Initial Error of Timing Interval	T_{EI}	$V_{CC}=5$ to 15V $R_A=R_B=1$ to 100K $C_T=0.1\mu F$		1		%
Supply Voltage Sensitivity of Timing Interval	T_{ES}			0.1		%/V
Rise Time	T_r	$R_L=10M\Omega$, $C_L=10pF$		20		nS
Fall Time	T_f	$R_L=10M\Omega$, $C_L=10pF$		20		nS
Maximum Astable Oscillation	F_{max}	$R_A=470\Omega$, $R_B=200\Omega$ $C_T=200pF$		2		MHz

APPLICATION CIRCUIT

1) Astable

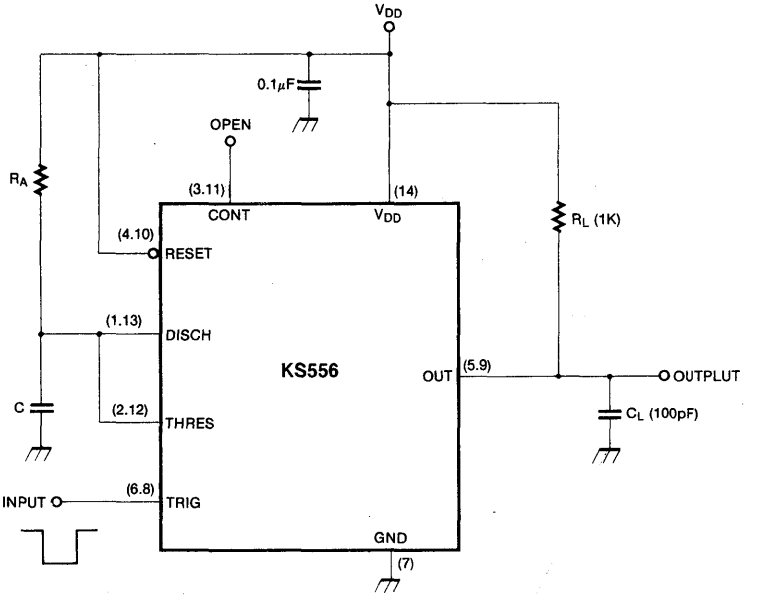
The circuit can be connected to trigger itself and free runs as multivibrator. The external capacitor chrages through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}.
As in the trigger mode, the charging and discharging times, and therefore the frequency, are essentially independently of the supply voltage. These frequency of oscillation is given by

$$F = 1/T = 1.44/(R_A + 2*R_B)/C_T$$



2) Monostable

In this mode of operation, the timer functions as one shot. Initially, the external capacitor (C) is held discharged by a transistor inside timer. Upon application of negative trigger pulse to trigger pin the flip flop is set which releases the short circuit across the external capacitor and drives the output high.
The voltage across the external capacitor now increases exponentially with time constant $T = R_A \times C$. When the voltage across the external capacitor equals $2/3 \times V_{CC}$, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the output to its state.



TIMER

The NE555 series are a monolithic integrated circuit and high stable device for generating accurate time delay or oscillation. NE555I is characterized for operation from −40°C to +85°C, and NE555C from 0°C to 70°C.

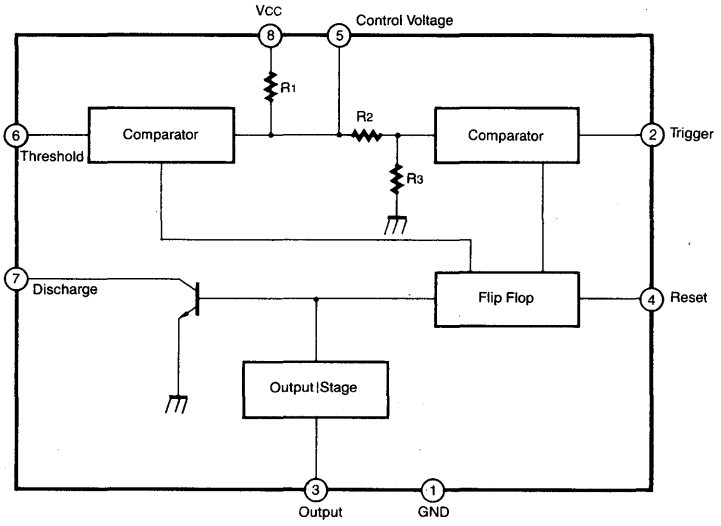
FEATURES

- **Turn off time less than 2μs**
- **Maximum operating frequency greater than 500KHz**
- **Timing from microseconds to hours**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **Temperature stability of 0.005% per °C**

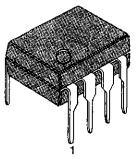
APPLICATIONS

- Precision timing
- Time delay generation
- Pulse generation
- Pulse position modulation
- Sequential timing
- Missing pulse detector

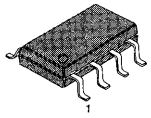
BLOCK DIAGRAM



8 DIP



8 SOP



ORDERING INFORMATION

Device	Package	Operating Temperature
NE555IN	8 DIP	−40 ~ +85°C
NE555ID	8 SOP	
NE555CN	8 DIP	0 ~ +70°C
NE555CD	8 SOP	

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lead Temperature (soldering 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range NE555I NE555C	T_{opr}	−40 ~ +85 0 ~ +70	°C °C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=5 ~ 15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
Supply Current *1(low stable)	I_{CC}	V_{CC} = 5V, R_L = ∞		3	6	mA
		V_{CC} = 15V, R_L = ∞		10	15	mA
*Timing Error (Monsotable) 2Initial Accurary Drift with Temperature Drift with Supply Voltage	MT_1	 R_A = 1KΩ to 100KΩ C = 0.1μF		 1.0 50 0.1	 3.0 0.5	 % ppm/°C %/V
*Timing Error (astable) 2Initial Accurary Drift with Temperature Drift with Supply Voltage	MT_2	 R_A = 1K to 100KΩ C = 0.1μF		 2.25 150 0.3		 % ppm/°C %/V
Control Voltage	V_C	V_{CC} = 15V	9.0	10.0	11.0	V
		V_{CC} = 5V	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	V_{CC} = 15V		10.0		V
		V_{CC} = 5V		3.33		V
*3Threshold Current	I_{TH}			0.1	0.25	μA
Trigger Voltage	V_{TR}	V_{CC} = 5	1.1	1.67	2.2	V
Trigger Voltage	V_{TR}	V_{CC} = 15V	4.5	5	5.6	V
Trigger Current	I_{TR}	V_T = 0V		0.5	2.0	μA
Reset Voltage	V_{RE}		0.4	0.7	1.0	V
Reset Current	I_{RE}			0.1	0.4	mA

ELECTRICAL CHARACTERISTICS

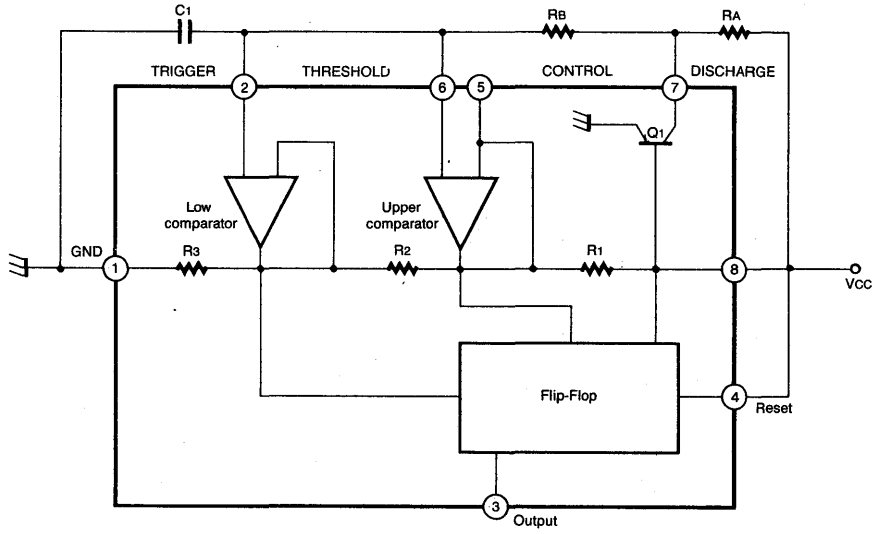
(T_a=25°C, V_{CC}=5~15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage (low)	V_{OL}	V_{CC}=15V I_{sink}=10mA I_{sink}=50mA		0.1 0.4	0.25 0.75	V V
		V_{CC}= 5V I_{sink}=5mA		0.25	0.35	V
Output Voltage (high)	V_{OH}	V_{CC}=15V I_{source}=200mA I_{source}=100mA	 12.75	12.5 13.3		V V
		V_{CC}=5V I_{source}=100mA	2.75	3.3		V
Rise Time of Output	T_r			100		nsec
Fall Time of Output	T_f			100		nsec
Discharge Leakage Current	I_D			20	100	nA

Notes:

1. Supply current when output is high is typically 1mA less at V_{CC}=5V.
2. Tested at V_{CC}=5.0V and V_{CC}=15V
3. This will determine the maximum value of R_A+R_B for 15V operation, the max total R=20MΩ, and for 5V operation the max total R=6.7MΩ.

APPLICATION CIRCUIT



APPLICATION NOTE

The application circuit shows astable mode.
The pin 6 (threshold) tied to the pin 2 (trigger) and pin 4 (reset) tied to V_{CC} (pin 8).
The external capacitor C_1 of pin 6 and pin 2 charges through R_A, R_B and discharges through R_B only.
In the internal circuit of the NE555, one input of upper comparator is the 2/3 V_{CC} ($*R_1 = R_2 = R_3$), another input of it connected pin 6.
As soon as charging C_1 is higher than 2/3 V_{CC}, discharge transistor Q_1 turn on and C_1 discharges to collector of transistor Q_1.
Therefore flip-flop circuit is reset and output is low.
One input of lower comparator is the 1/3 V_{CC}, discharge transistor Q_1 turn off and C_1 charges through R_A and R_B.
Therefore flip-flop circuit is set and output is high.
So to say, when C_1 charges through R_A and R_B output is high and when C_1 discharges through R_b output is low
The charge time (output is high) T_1 is 0.693 $(R_A + R_B)$ C_1 and the discharge time (output is low) T_2 is 0.693 $(R_B C_1)$.

$$\left(\ln \frac{V_{CC}-1/3V_{CC}}{V_{CC}-2/3V_{CC}} = 0.693\right)$$

Thus the total period time T is given by
$T = T_1 + T_2 = 0.693\,(R_A + 2R_B).\,C_1$.
Then the frequency of astable mode is given by

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C_1}$$

The duty cycle is given by

$$D.C = \frac{T_2}{T} = \frac{R_B}{R_A + 2R_B}$$

If you make use of the NE556 you can make two astable mode.
If you want another application note, request information on our timer IC application circuit designer.

DUAL TIMER

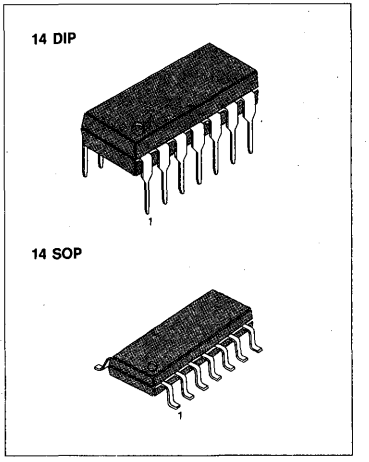
The NE556 series dual monolithic timing circuits are a highly stable controller capable of producing accurate time delays or oscillation.

The NE556 is a dual NE555. Timing is provided an external resistor and capacitor for each timing function.

The two timers operate independently of each other, sharing only V_{CC} and ground.

The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

NE556I is characterized for operation from −40°C to +85°C, and NE556C from 0°C to 70°C.



FEATURES

- **Direct replacement for NE556**
- **Replaces two NE555 timers**
- **Operates in both astable and monostable modes**
- **High output current**
- **TTL compatible**
- **Timing from microsecond to hours**
- **Adjustable duty cycle**
- **Temperature stability of 0.005% per °C**

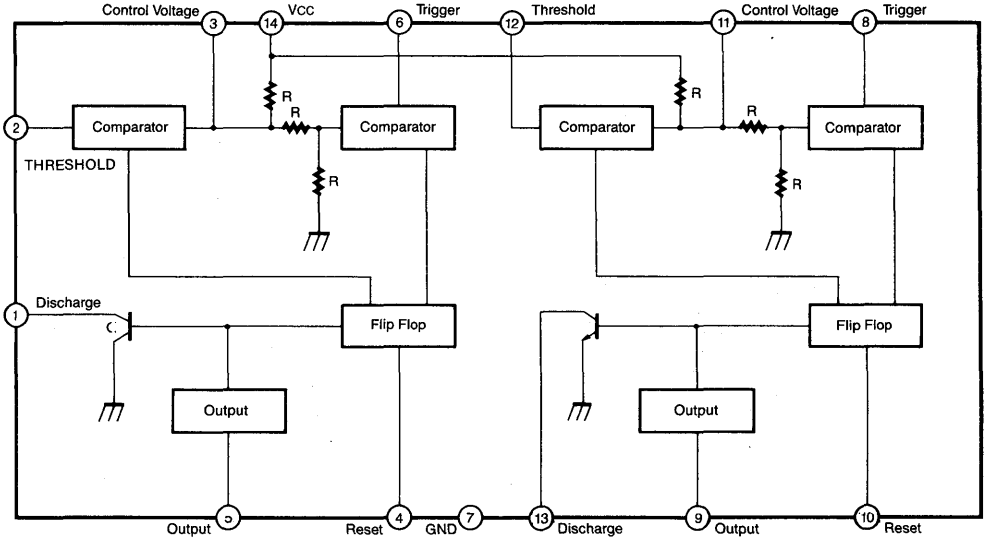
APPLICATIONS

- Precision timing
- Pulse shaping
- Pulse width modulation
- Frequency division
- Traffic light control
- Sequential timing
- Pulse generator
- Time delay generator
- Touch tone encoder
- Tone burst generator

ORDERING INFORMATION

Device	Package	Operating Temperature
NE556IN	14 DIP	−40 ~ +85°C
NE556ID	14 SOP	
NE556CN	14 DIP	0 ~ +70°C
NE556CD	14 SOP	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lead Temperature (soldering 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range NE556I NE556C	T_{opr}	−40 ~ +85 0 ~ +70	°C °C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V to +15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
*1 Supply Current (Two timers) (low state)	I_{CC}	V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞		5 16	12 30	mA mA
*2 Timing Error (monostable) Initial Accuracy Drift with Temperature Drift with Supply Voltage	MT_1	R_A = 2KΩ to 100KΩ C = 0.1μF T = 1.1R_C		 0.75 50 0.1		 % ppm/°C %/V
Control Voltage	V_C	V_{CC} = 15V	9.0	10.0	11.0	V
		V_{CC} = 5V	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	V_{CC} = 15V		10.0		V
		V_{CC} = 5V		3.33		V
*3 Threshold Current	I_{TH}			30	250	nA
Trigger Voltage	V_{TR}	V_{CC} = 15V	4.5	5.0	5.6	V
		V_{CC} = 5V	1.1	1.67	2.2	V
Trigger Current	I_{TR}	V_T = 0V		0.5	2.0	μA
*5 Reset Voltage	V_{RE}		0.4	0.7	1.0	V
Reset Current	I_{RE}			0.1	0.6	mA
Output Voltage Low	V_{OL}	V_{CC} = 15V I_{sink} = 10mA I_{sink} = 50mA I_{sink} = 100mA I_{sink} = 200mA V_{CC} = 5V I_{sink} = 8mA I_{sink} = 5mA		 0.1 0.4 2.0 2.5 0.25 0.15	 0.25 0.75 3.2 (.3 0.25	 V V V V V V

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V to +15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage (high)	V_{OH}	V_{CC} = 15V I_{source} = 200mA I_{source} = 100mA	 12.75	 12.5 13.3		 V V
		V_{CC} = 5V I_{source} = 100mA	2.75	3.3		V
Rise Time of Output	T_r			100	300	nsec
Fall Time of Output	T_f			100	300	nsec
Discharge Leakage Current	I_D			20	100	nA
*4 Matching Characteristics Initial Accuracy Drift with Temperature Drift with Supply Voltage	M_{CH}			 1.0 10 0.2	 2.0 0.5	 % ppm/°C %/V
*2 Timing Error (astable) Initial Accuracy Drift with Temperature Drift with Supply Voltage	MT_2	R_A, R_B = 1kΩ to 100kΩ C = 0.1μF V_{CC} = 15V		 2.25 150 0.3		 % ppm/°C %/V

Notes:

*1. Supply current when output is high is typically 1.0mA less at V_{CC} = 5V.

*2. Tested at V_{CC} = 5V and V_{CC} = 15V

*3. This will determine the maximum value of $R_A + R_B$ for 15V operation.
The maximum total R = 20MΩ, and for 5V operation the maximum total R = 6.6MΩ.

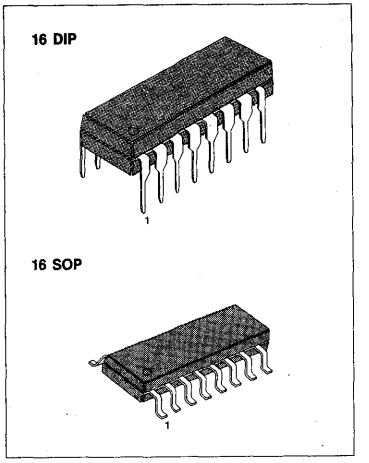
*4. Matching characteristic refer to the difference between performance characteristics of each timer section in the monostable mode.

*5. As reset voltage lowers, timing is inhibited and then the output goes low.

QUAD TIMER

The NE558 series are a monolithic Quad Timers which can be used to produce four entirely independent timing functions. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays, from microseconds to hours. The time is precisely controlled by one external resistor and one capacitor in the time delay mode. A stable mode can be operated by using two of four timer sections.

NE558I is characterized for operation from −40°C to +85°C, and NE558C from 0°C to 70°C.



FEATURES

- **Wide supply voltage range: 4.5V to 16V**
- **100mA output current per section**
- **Edge triggered without coupling capacitor**
- **Time period equals RC**
- **Output independent of trigger conditions.**

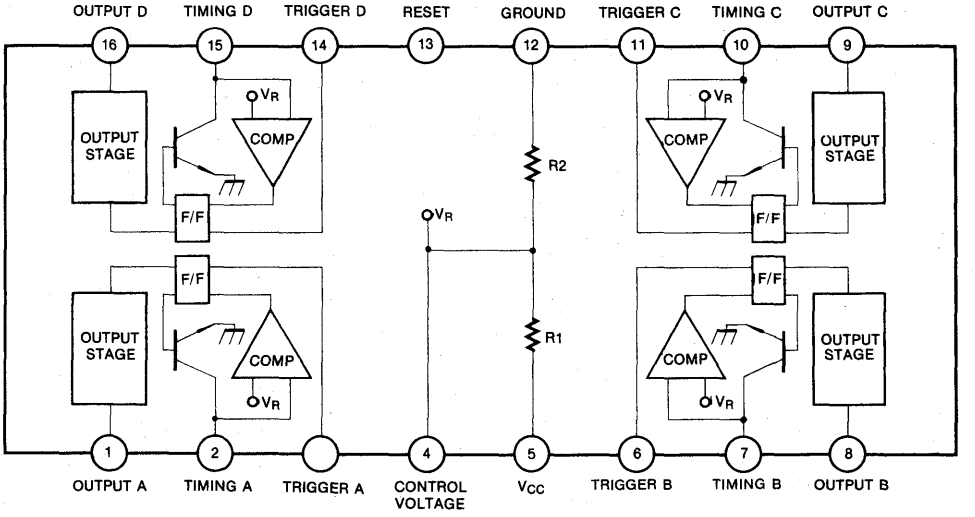
APPLICATIONS

- Quad one-shot
- Sequential timing
- Precision timing
- **Time delay generation**

ORDERING INFORMATION

Device	Package	Operating Temperature
NE558IN	14 DIP	−40 ~ +85°C
NE558CN	14 DIP	0 ~ +70°C
NE558CD	14 SOP	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lead Temperature (soldering 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range NE556I	T_{opr}	−40 ~ +85	°C
NE556C		0 ~ 70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ~ 15V, Ta = 25°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
Supply Current	I_{CC}	V_{CC} = 15V, reset voltage = 15V		16	36	mA
Timing Error (T = RC) Initial Accuracy	M_T	R = 2KΩ to 100KΩ, C = 1μF		±2	5	%
Drift with Temperature				30	150	PPM/°C
Drift with Supply Voltage				0.1	0.9	%/V
[1]Trigger Voltage	V_{TR}	V_{CC} = 15V	0.8	1.5	2.4	V
[1]Trigger Current	I_{TR}	Trigger voltage = 0V		5.0	100	μA
[2]Reset Voltage	V_{RE}	Reset	0.8	1.5	2.4	V
[2]Reset Current	I_{RE}	Reset		50	500	μA
Threshold Voltage	V_{TH}			0.63 × V_{CC}		V
Threshold Current	I_{TL}			15		nA
[3]Output Voltage	V_{OUT}	I_L = 10mA		0.1	0.4	V
		I_L = 100mA		1.0	2.0	
Output Leakage Current	I_{OL}			10	500	nA
Propagation Delay Time	T_P			1.0		μS
Rise Time	T_r	I_L = 100mA		100		nS
Fall Time	T_f	I_L = 100mA		100		nS

NOTES: 1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8V, outputs set low and trigger inhibited.
3. Output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is nomally low sinking current.

APPLICATIONS

Fig. 1 Long-Time Delay

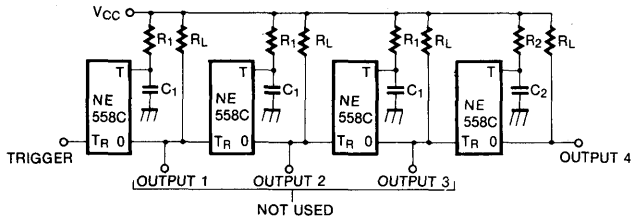


Fig. 2 Timing Chart

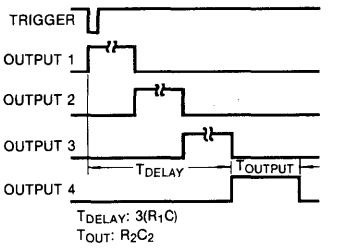


Fig. 3 Ring Counter

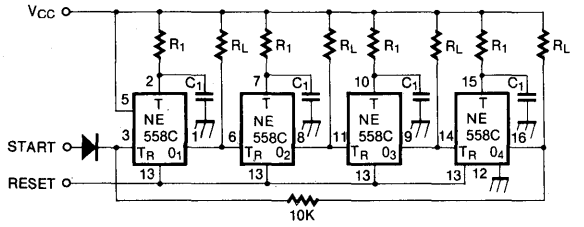
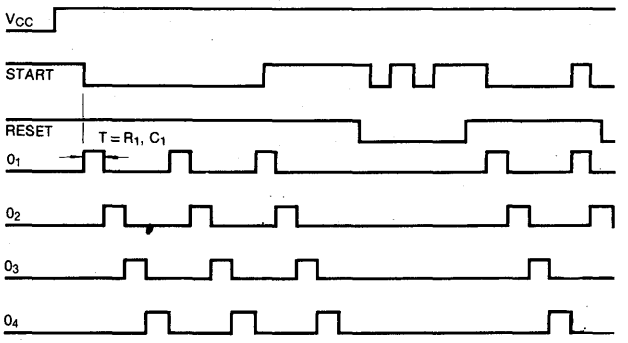
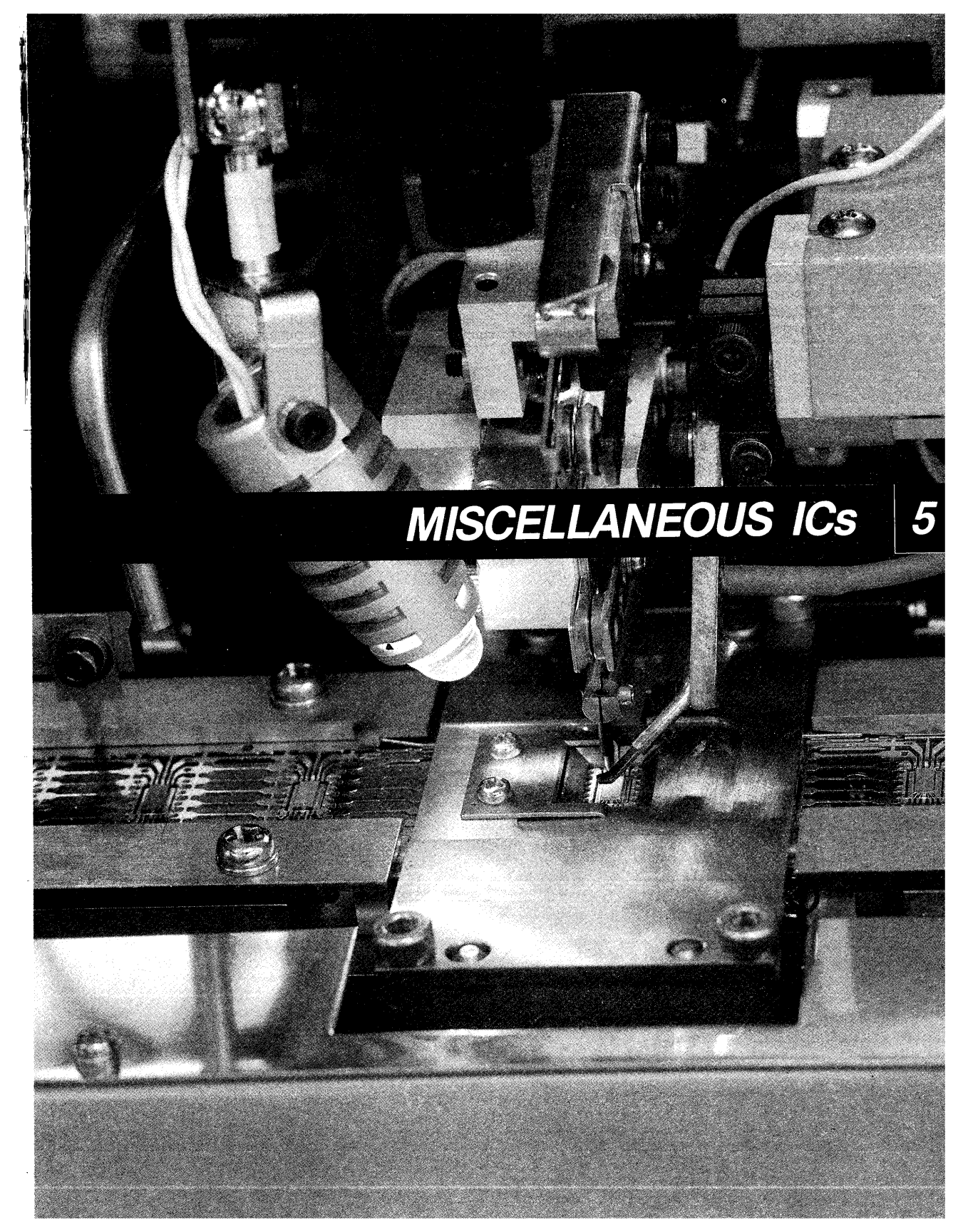


Fig. 4 Timing Chart



NOTES

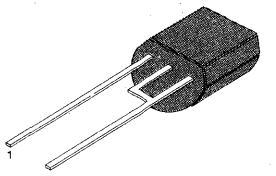


MISCELLANEOUS ICs 5

SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT VOLTAGE STABILIZAER FOR ELECTRONIC TUNER

The KA33V is a monolithic integrated voltage stabilizer especially designed as voltage supplier for electronic tuners.

TO-92



1: Anode 2: Cathode

FEATURES

- **Low Temperature Coefficient**
- **Low Dynamic Resistance**
- **Typical Reference Voltage of 33V**

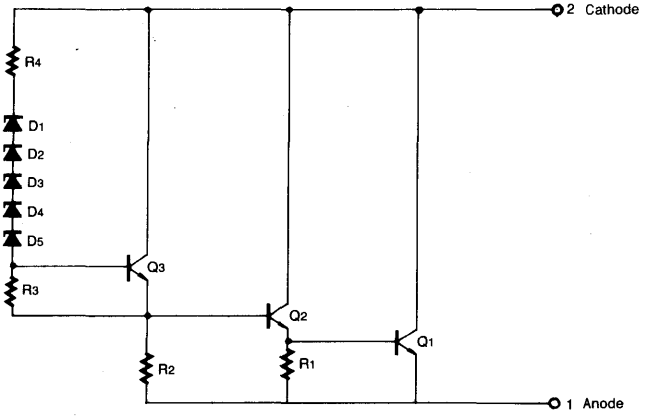
ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Zener Current	I_Z	10	mA
Power Dissipation (T_a=75°C)	P_D	200	mW
Operating Ambient Temperature-Range	T_{opr}	−20~75	°C
Storage Temperature Range	T_{stg}	−40~125	°C

ELECTRICAL CHARACTERISTICS (T_a=25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Stabilized Voltage	V_Z	I_Z=5mA	31		35	V
Stabilized Voltage-Temperature Drift	$\triangle V_Z/\triangle T$	I_Z=5mA, T_a=−20 to 75°C	−1	0	1	mV/°C
Dynamic Resistance	r_Z	I_Z=5mA, f=1KHz		10	25	

SCHEMATIC DIAGRAM



5

MEASURING CIRCUITS

Fig. 1 Measuring Circuit for Stabilized Voltage V_Z

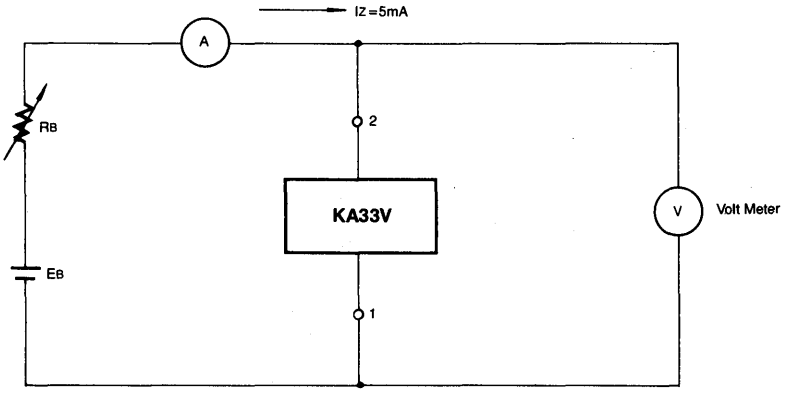


Fig. 2 Measuring Circuit for Dynamic Resistance

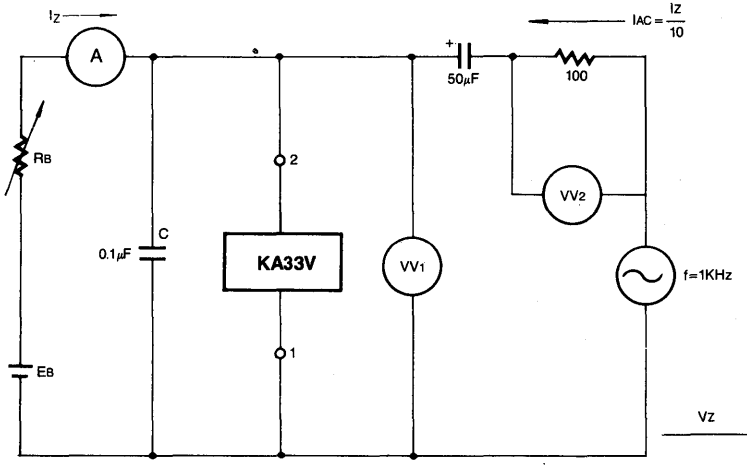
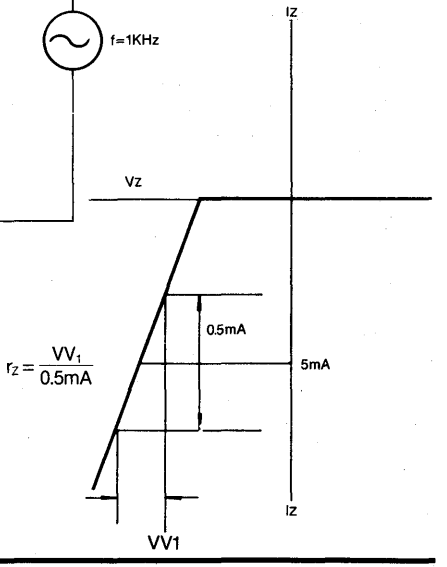
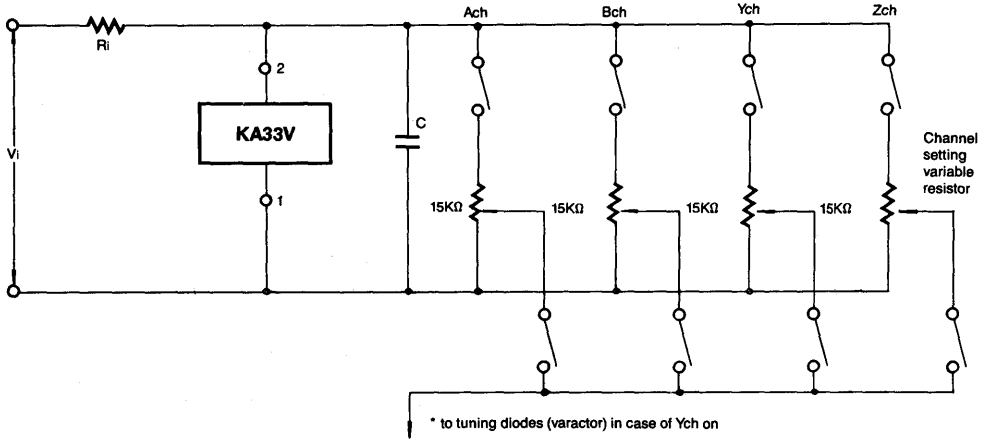


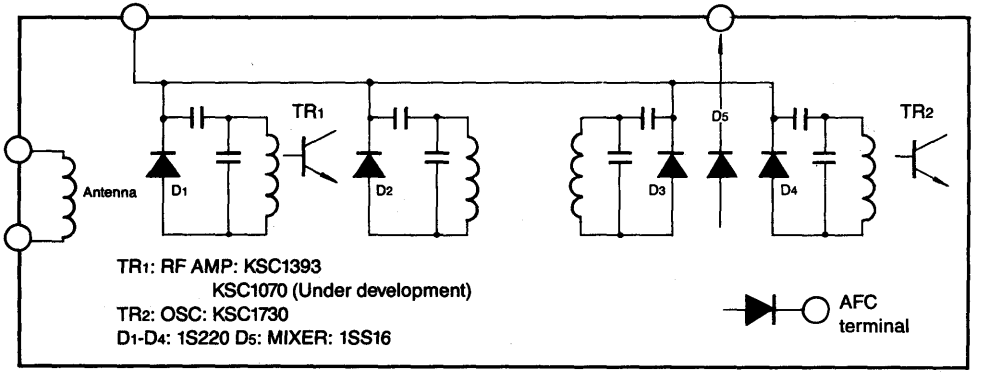
Fig. 3



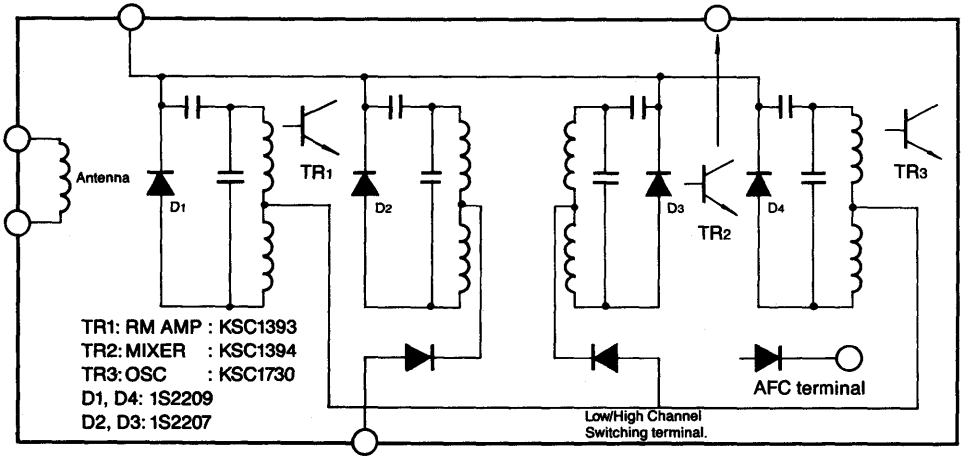
TYPICAL APPLICATION



(1) UHF TUNER

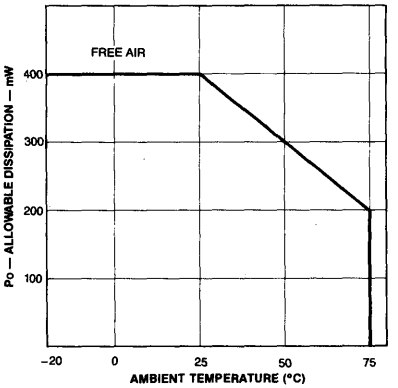


(2) VHF TUNER



POWER-TEMPERATURE DERATING CURVE

Fig. 7 ALLOWABLE DISSIPATION vs. AMBIENT TEMPERATURE



TYPICAL CHARACTERISTIC CURVES (T_a=25°C)

Fig. 8 DYNAMIC RESISTANCE vs. ZENER CURRENT

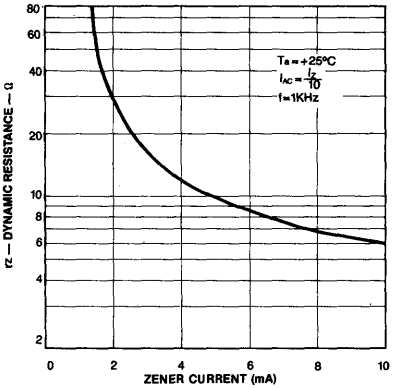


Fig. 9 STABILIZED VOLTAGE TEMPERATURE DRIFT vs. ZENER CURRENT

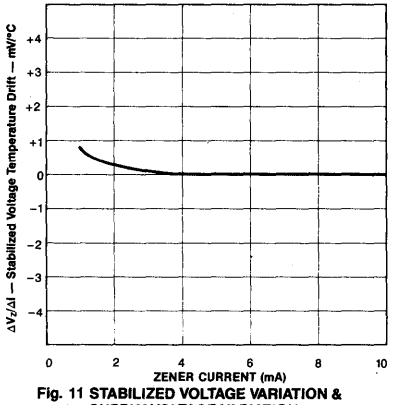


Fig. 10 STABILIZED VOLTAGE VARIATION vs. TIME

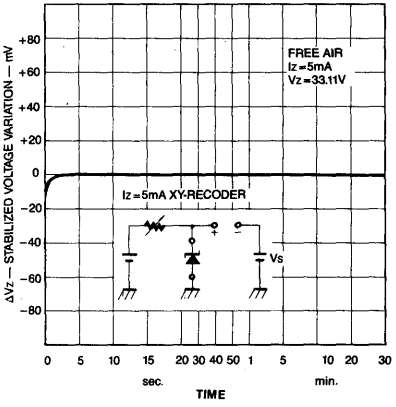
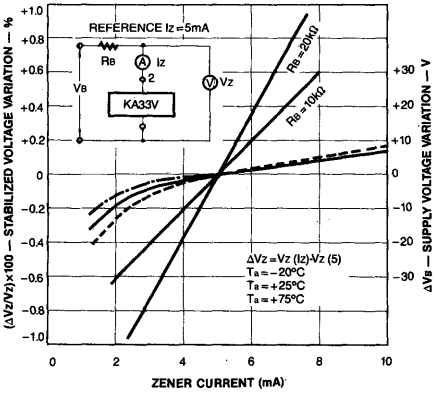
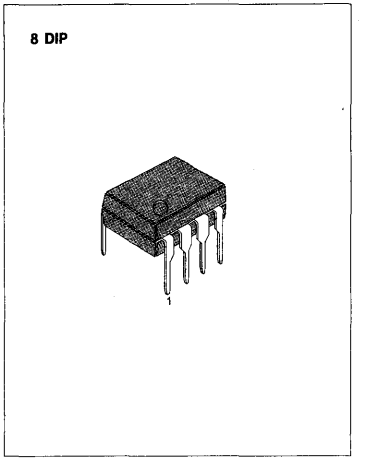


Fig. 11 STABILIZED VOLTAGE VARIATION & SUPPLY VOLTAGE VARIATION vs. ZENER CURRENT



PRECISION VOLTAGE-TO-FREQUENCY CONVERTER

This voltage-to-frequency converter provides the output pulse train at a frequency precisely proportional to the applied input voltage. The KA331 can operate at power supplies as low as 4.0V and be changed output frequency from 1Hz to 100KHz.
It is ideally suited for use in simple low-cost circuit for analog-to-digital conversion, long-term integration, linear frequency modulation or demodulation, frequency-to-voltage conversion, and many other functions.



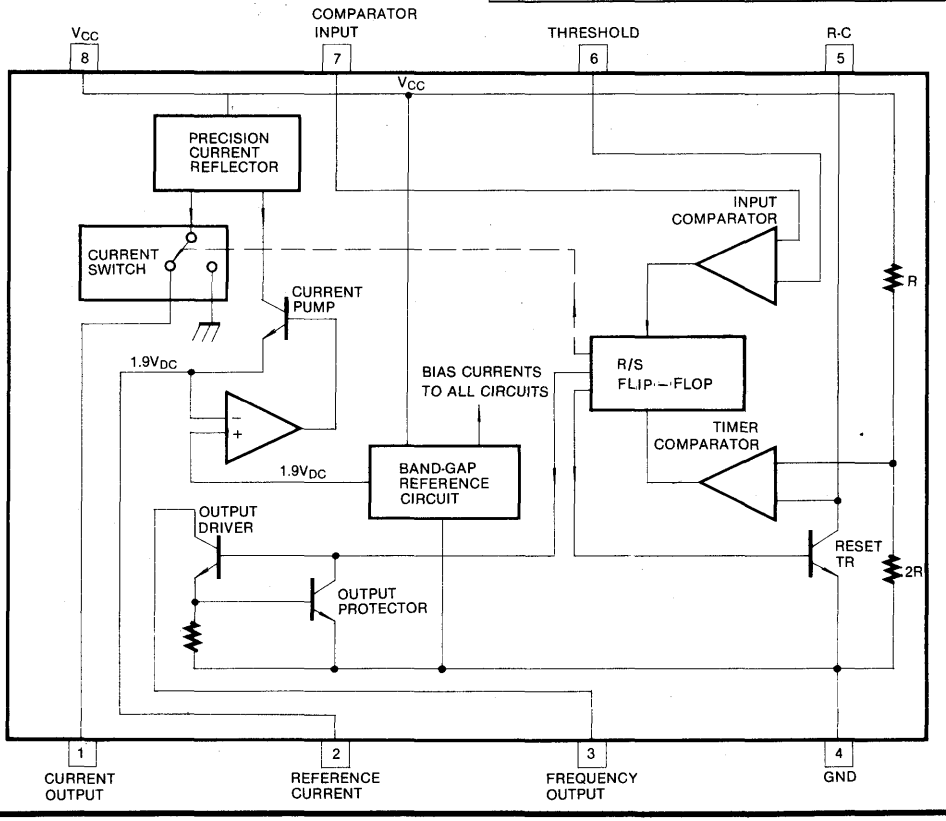
FEATURES

- **Guaranteed linearity: 0.01% max**
- **Low power dissipation: 15mW at 5V**
- **Wide range of full scale frequency: 1Hz to 100KHz**
- **Pulse output compatible with all logic forms**
- **Wide dynamic range: 100dB min at 10KHz full scale frequency**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA331CN	8 DIP	0 ~ +70°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 0°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_S	40	V
Input Voltage	V_{IN}	-0.2 to $+V_S$	V
Operating Temperature Range	T_{opr}	0 to 70	°C
Power Dissipation	P_D	500	mW

ELECTRICAL CHARACTERISTICS

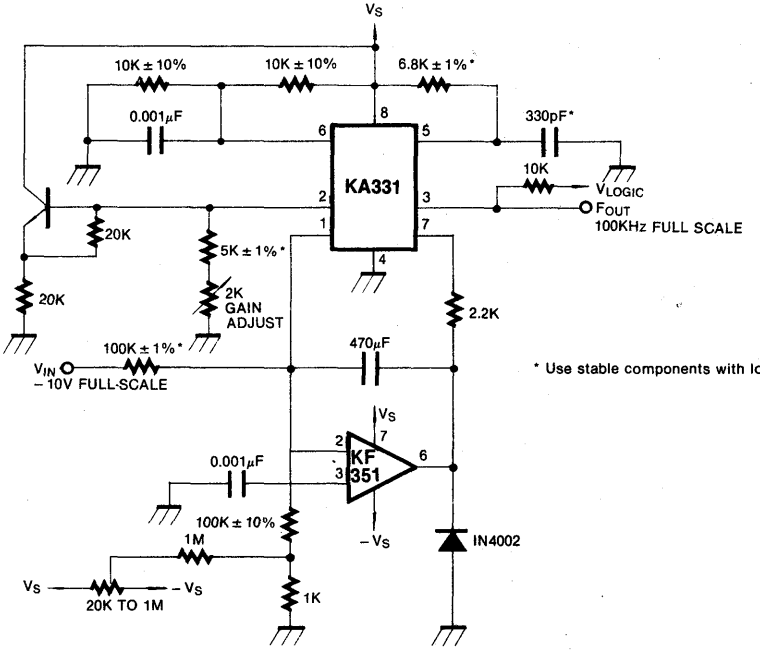
Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
VFC Non-Linearity	VFCNL	$4.5V \leq V_S \leq 20V$	—	±0.003	±0.01	% Full-Scale
Conversion Accuracy Scale Factor	ACCUR	$V_{IN} = -10V$, $R_S = 14K\Omega$	0.90	1.00	1.10	KHz/V
Change of Gain With V_S	△A	$4.5V \leq V_S \leq 10V$	—	0.01	0.1	%/V
		$10V \leq V_S \leq 40V$	—	0.006	0.06	
Rated Full-Scale Frequency	F_{OUT}	$V_{IN} = -10V$	10.0	—	—	KHz
INPUT COMPARATOR						
Offset Voltage	V_{OS}	$T_{MIN} \leq T_A \leq T_{MAX}$	—	±3	±10	mV
Bias Current	I_B		—	−80	−300	nA
Offset Current	I_{OS}		—	±8	±100	nA
Common-Mode Range	V_{CM}	$T_{MIN} \leq T_A \leq T_{MAX}$	−0.2	—	V_{CC}-2.0	V
TIMER (PIN 5)						
Timer Threshold Voltage	V_{TH}		0.63	0.667	0.70	xV_S
Input Bias Current	I_{B5}	$V_S = 15V$, $0V \leq V_{PIN\ 5} \leq 9.9V$	—	±10	±100	nA
		$V_{PIN5} = 10V$	—	200	1000	nA
Saturation Voltage	$V_{SAT\ 5}$	$I = 5mA$	—	0.22	0.5	V
CURRENT SOURCE (PIN 1)						
Output Current	I_{OI}	$R_S = 14K\Omega$, $V_{PIN1} = 0$	116	136	156	μA
Change with Voltage	$\triangle I_O$	$0V \leq V_{PIN1} \leq 10V$	—	0.2	1.0	μA
Current Source Off Leakage	I_{L1}		—	0.02	10.0	nA
REFERENCE VOLTAGE (PIN 2)						
Reference Voltage	V_{ref}		1.70	1.89	2.08	V_{DC}
Stability vs Temperature	V_{TEMP}		—	±60	—	ppm/°C
Stability vs Time, 1000 Hours	V_{TIME}		—	±0.1	—	%

ELECTRICAL CHARACTERISTICS (Continued)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
LOGIC OUTPUT (PIN 3)						
Saturation Voltage	V_{SAT3}	I = 5mA	—	0.15	0.50	V
		I = 3.2mA	—	0.10	0.40	
Off Leakage	I_{L3}		—	± 0.05	1.0	μA
SUPPLY CURRENT						
Supply Current	I_S	V_S = 5V	1.5	3.0	6.0	mA
		V_S = 40V	2.0	4.0	8.0	

TYPICAL APPLICATIONS

Fig. 1 Precision Voltage-to-Frequency Converter, 100KHz Full-Scale



* Use stable components with low temperature coefficients

Fig. 2 Simple Frequency-to-Voltage Converter, 10KHz Full-Scale

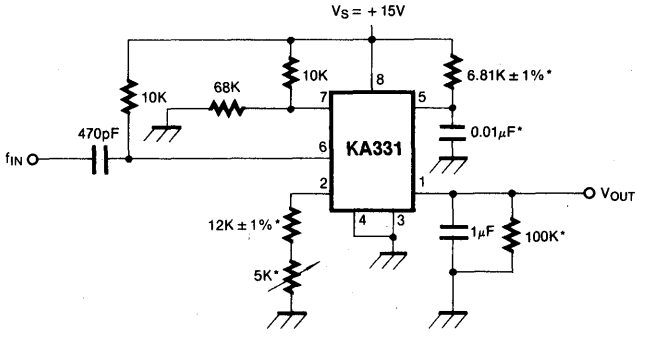
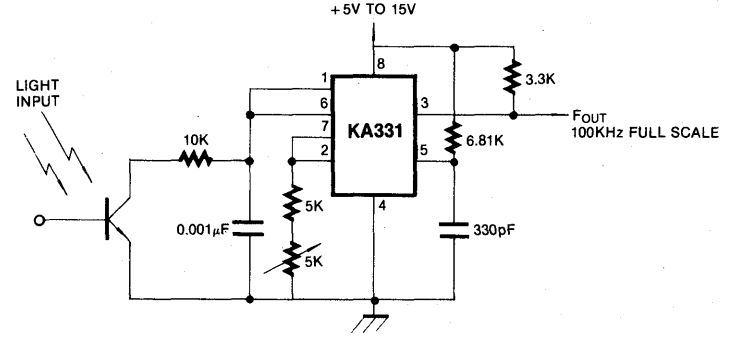


Fig. 3 Light Intesity to Frequency Converter



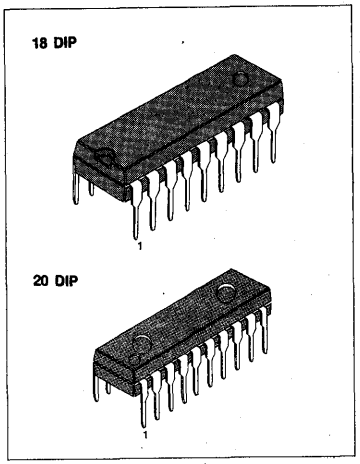
8-CHANNEL SOURCE DRIVERS

These integrated circuits, rated for operation with output voltages of up to 50V and designed to link NMOS logic with high-current inductive loads, will work with many combinations of logic-and load-voltage levels, meeting interface requirements beyond the capabilities of standard logic buffers.

KA2580A is a high current source driver used to switch the ground ends of loads that are directly connected to a negative supply. Typical loads are telephone relays, PIN diodes, and LEDs.

KA2588A is a high-current source driver similar to KA2580A, has separated logic and driver supply lines. Its eight drivers can serve as an interface between positive logic (TTL, CMOS, MOS) or negative logic (NMOS) and either negative or split-load supplies.

KA2580A is furnished in 18-pin dual in-line plastic package; KA2588A is supplied in a 20-pin dual in-line plastic package. All input connections are on one side of the packages, output pins on the other, to simplify printed wiring board layout.



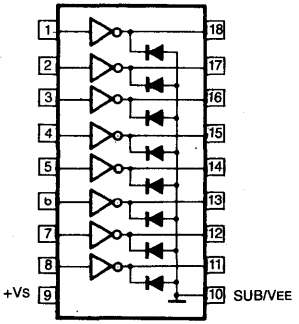
FEATURES

- **TTL, CMOS, PMOS, NMOS Compatible**
- **High Output Current Ratings**
- **Internal Transient Suppression**
- **Efficient Input/Output Pin Structure**

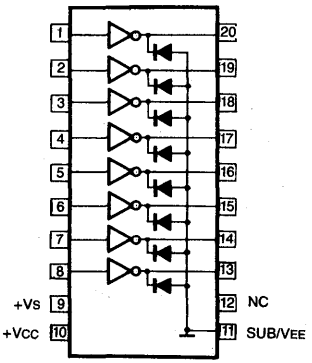
ORDERING INFORMATION

Device	Package	Operating Temperature
KA2580AN	18 DIP	−20 ~ +85°C
KA2588AN	20 DIP	

SCHEMATIC DIAGRAM



KA2580A



KA2588A

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C, for Any One Driver unless otherwise noted)

Characteristic	Symbol	Value	Unit
Output Voltage	V_{CE}	50	V
Supply Voltage (ref, sub)	V_S	50	V
Supply Voltage (ref, sub, KA2588A)	V_{CC}	50	V
Input Voltage (ref, Vs)	V_{IN}	−30	V
Total Current	$I_{CC}+I_S$	−500	mA
Substrate Current	I_{SUB}	3.0	A
Power Dissipation (single output)	Pd	1.0	W
(total Package)*		2.2	W
Operating Temperature	T_a	−20 ~ +85	°C
Storage Temperature	Tstg	−65 ~ +150	°C

* Derate at the rate of 18mW/°C above 25°C

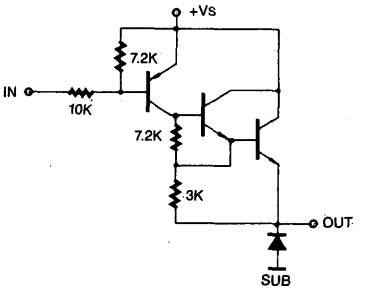
TYPICAL OPERATING VOLTAGE

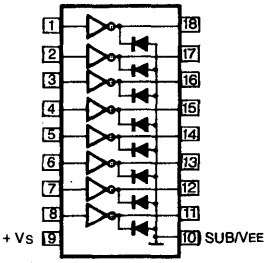
V_S	V_{IN} (on)	V_{IN} (off)	V_{CC}	V_{EE}(max)	DVC Type
0V	−15V ~ −3.6V	−0.5V ~ 0V	NA	−50V	KA2580A
+5V	0V ~ +1.4V	+4.5V ~ +5V	NA ≤5V	−45V −45V	KA2580A KA2588A
+12V	0V ~ +8.4V	+11.5V ~ +12V	NA ≤12V	−38V −38V	KA2580A KA2588A
+15V	0V ~ +11.4V	+14.5V ~ +15V	NA ≤15V	−35V −35V	KA2580A KA2588A

Notes

1) For simplication, these devices are characterized to the above with specific voltages for inputs, logic supply (V_s), load supply (V_{EE}), and collector supply (V_{CC}).
2) Typical use of the KA2580A is with negative referenced logic. The more common application of the KA2588A is with positive referenced logic supplies.
3) In application, the devices are capable of operation over a wide range of logic and supply voltage levels.
4) The substrate must be tied to the most negative point in the external circuit to maintain isolation drivers and to provide for normal circuit operation.

PARTIAL SCHEMATIC (KA2580A)





ELECTRICAL CHARACTERISTICS (KA2580A)

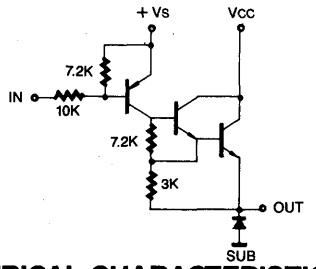
(T_a = 25°C, V_S = 0V, V_{EE} = −45V unless otherwise noted)

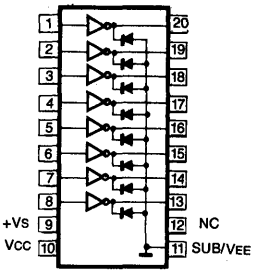
Characteristic	Symbol	Test Conditions	Min	Max	Unit
Output Leakage Current	I_{CEX}	V_{In} = −0.5V, V_{OUT} = V_{EE} = −50V		50	μA
		V_{IN} = −0.4V, V_{OUT} = V_{EE} = −50V, T_a = 70°C		100	μA
Output Sustaining Voltage (Note 1, 2)	V_{CE} (sus)	V_{IN} = −0.4V, I_{OUT} = −25mA	35		V
Output Saturation Voltage	V_{CE} (sat)	V_{IN} = −2.4V, I_{OUT} = −100mA		1.8	V
		V_{IN} = −3.0V, I_{OUT} = −225mA		1.9	V
		V_{IN} = −3.6V, I_{OUT} = −350mA		2.0	V
Input Current	I_{IN} (on)	V_{IN} = −3.6V, I_{OUT} = −350mA		−500	μA
		V_{IN} = −15V, I_{OUT} = −350mA		−2.1	mA
	I_{IN} (off)	I_{OUT} = −500μA, T_a ≈ 70°C (Note 3)	−50		μA
Input Voltage (Note 4)	V_{IN} (on)	I_{OUT} = −100mA, V_{CE} ≤ 1.8V		−2.4	V
		I_{OUT} = −225mA, V_{CE} ≤ 1.9V		−3.0	V
		I_{OUT} = −350mA, V_{CE} ≤ 2.0V		−3.6	V
	V_{IN} (off)	I_{OUT} = −500μA, T_a = 70°C	−0.2		V
Clamp Diode Leakage Current	I_R	V_R = 50V, T_a = 70°C		50	μA
Clamp Diode Forward Voltage	Vf	If=350mA		2.0	V
Input Capacitance	C_{IN}			25	pF
Turn-On Delay	t_{PHL}	0.5 V_{IN} to 0.5 V_{OUT}		5.0	μS
Turn-Off Delay	t_{PLH}	0.5 V_{IN} to 0.5 V_{OUT}		5.0	μS

Notes

1) Pulsed test, tp ≤ 300uS, duty cycle ≤ 2%.
2) Negative current is defined as coming out of specified device pin.
3) The Iin (off) current limit guarantees against partial turn-on of the output.
4) The Vin (on) voltage limit guarantees a minimum output source per the specified conditions.
5) The substrate must always be tied to the most negative point and must be at least 4.0V below V_s.

PARTIAL SCHEMATIC (KA2588A)





ELECTRICAL CHARACTERISTICS (KA2588A)

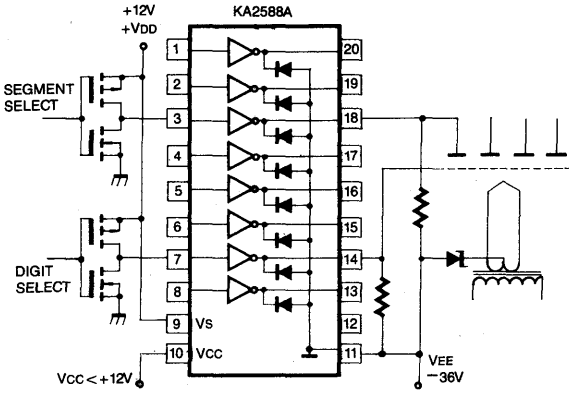
(T_a=25°C, V_S=V_{CC}=5.0V, V_{EE}=−40V unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Output Leakage Current	I_{CEX}	V_{IN}≥4.5V, V_{OUT}=V_{EE}=−45V		50	μA
		V_{IN}≥4.6V, V_{OUT}=V_{EE}=−45V T_a=70°C		100	μA
Output Sustaining Voltage (Note 1, 2)	V_{CE} (sus)	V_{IN}≥4.6V, I_{OUT}=−25mA	35		V
Output Saturation Voltage	V_{CE} (sat)	V_{IN}=2.6V, I_{OUT}=−100mA Ref. V_{CC}		1.8	V
		V_{IN}=2.0V, I_{OUT}=−225mA Ref. V_{CC}		1.9	V
		V_{IN}=1.4V, I_{OUT}=−350mA Ref. V_{CC}		2.0	V
Input Current	I_{IN} (on)	V_{IN}=1.4V, I_{OUT}=−350mA		−500	μA
		V_S=15V, V_{EE}=−30V, V_{IN}=0V, I_{OUT}=−350mA		−2.1	mA
	I_{IN} (off)	I_{OUT}=−500μA, T_a=70°C (Note 3)	−50		μA
Input Voltage (Note 4)	V_{IN} (on)	I_{OUT}=−100mA, V_{CE}≤1.8V		2.6	V
		I_{OUT}=−225mA, V_{CE}≤1.9V		2.0	V
		I_{OUT}=−350mA, V_{CE}≤2.0V		1.4	V
	V_{IN} (off)	I_{OUT}=−500μA, T_A=70°C	4.8		V
Clamp Diode Leakage Current	I_R	V_R=50V, T_a=70°C		50	μA
Clamp Diode Forward Voltage	Vf	If=350mA		2.0	V
Input Capacitance	C_{IN}			25	pF
Turn-On Delay	t_{PHL}	0.5 V_{IN} to 0.5 Vout		5.0	μS
Turn-Off Delay	t_{PLH}	0.5 V_{IN} to 0.5 Vout		5.0	μS

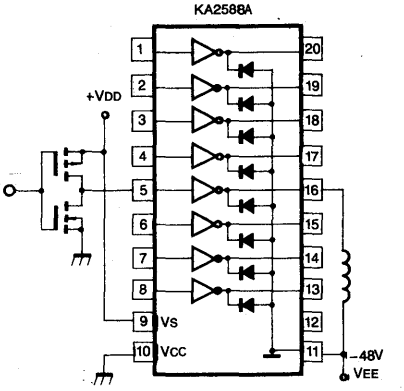
Notes

1) Pulsed test, tp≤300uS, duty cycle≤2%.
2) Negative current is defined as coming out of specified device pin.
3) The Iin (off) current limit guarantees against partial turn-on of the output.
4) The Vin (on) voltage limit guarantees a minimum output source per the specified conditions.
5) The substrate must always be tied to the most negative point and must be at least 4.0V below V_s.
6) V_{CC} must never be more positive than V_S.

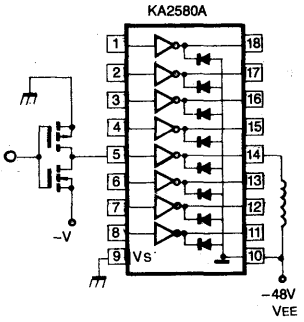
TYPICAL APPLICATIONS



Vacuum Fluorescent Display Driver (Split Supply)



Telecommunicaiton Relay Driver (Positive Logic)



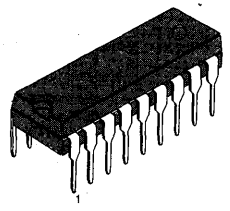
Telecommunication Relay Driver (Negative Logic)

5

FLUORESCENT DISPLAY DRIVERS

Consisting of eight NPN Darlington output stages and the associated common-emitter input stages, these drivers are designed to interface between low-level digital logic and vacuum fluorescent displays. KA2651 is capable of driving the digits and/or segments of these displays and is designed to permit all outputs to be activated simultaneously. Pull-down resistors are incorporated into each output and no external components are required for most fluorescent display applications.

18 DIP



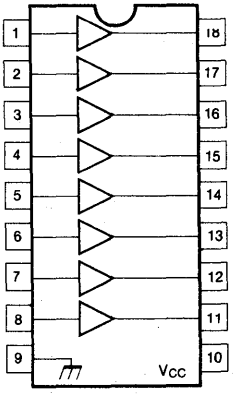
FEATURES

- **Digit or Segment Drivers**
- **Low Input Current**
- **Internal Output Pull-Down Resistors**
- **High Output Breakdown Voltage**
- **Single or Split Supply Operation**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2651N	18 DIP	−20 ~ +85°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C, Voltages are with reference to ground unless otherwise noted)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	65	V
Input Voltage	V_{IN}	20	V
Output Current	I_{out}	−40	mA
Operating Temperature	Ta	−20 ~ +85	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.0 ~ 50	V
Input ON Voltage	V_{IN}	2.4 ~ 15	V
Output ON Current*	I_{outON}	−25	mA

* Positive (negative) current is defined as going into (coming out of) the specified device pin.

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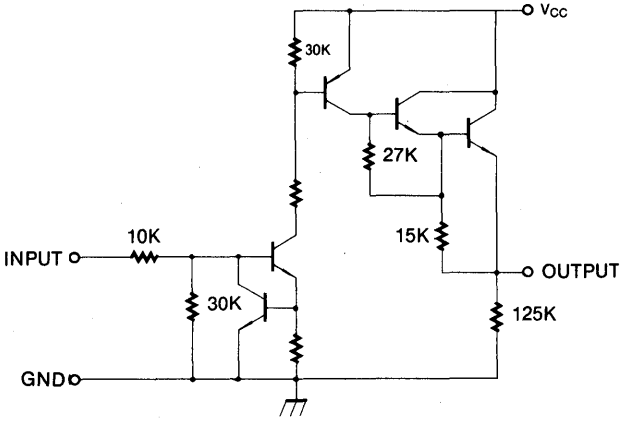
ELECTRICAL CHARACTERISTICS

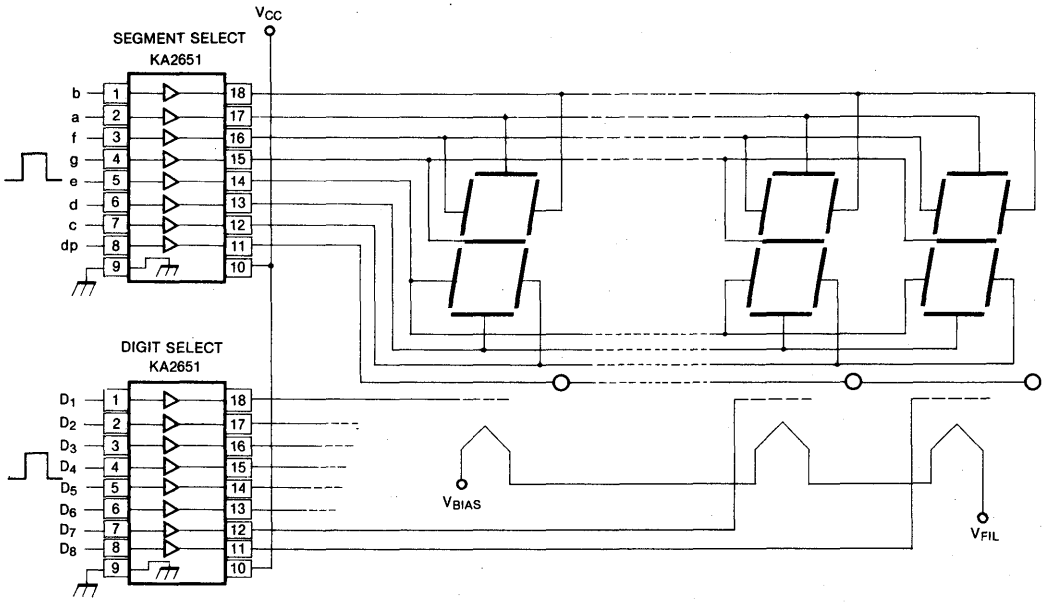
(Ta = 25°C, V_{CC} = 60V, unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Leakage Current	I_{OUTLK}	V_{IN} = 0.4V			15	μA
Output OFF Voltage	V_{OUTOFF}	V_{IN} = 0.4V			1.0	V
Output Pull-Down Current	I_{OUTPD}	Input Open, $V_{OUT} = V_{CC}$	350	550	775	μA
Output ON Voltage	V_{OUTON}	V_{IN} = 2.4V I_{OUT} = −25mA	57	58		V
Input ON Current	I_{IN}	V_{IN} = 2.4V		120	225	μA
		V_{IN} = 5.0V		450	650	μA
Supply Current	I_{CC}	All Inputs Open		10	100	μA
		All Inputs = 2.4V		5.5	8.0	mA

PARTIAL SCHEMATIC



TYPICAL MULTIPLEXED FLUORESCENT DISPLAY



HIGH VOLTAGE, HIGH CURRENT DARLINGTON ARRAYS

The KA2655, KA2656, KA2657, KA2658 and KA2659 are comprised of seven high voltage, high current NPN darlington transistors arrays with common emitter, open collector outputs. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout. Peak inrush currents to 600mA permit them to drive incandescent lamps.

The KA2655 is a general purpose array for use with DTL, TTL, PMOS or CMOS logic directly.

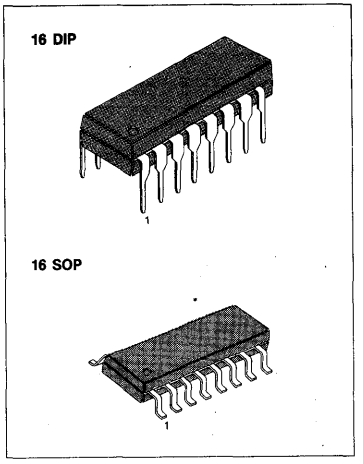
The KA2656 version does away with the need for any external discrete resistors, since each unit has a resistor and a zener diode in series with the input. The KA2656 is designed for use with 14 to 25V PMOS devices. The zener diode also gives these devices excellent noise immunity.

The KA2657 has a series base resistor to each darlington pair, and thus allows operation directly with TTL or CMOS operating at supply voltages of 5V. The KA2657 will handle numerous interfaces needs-particularly those beyond the capabilities of standard logic buffers.

The KA2658 has an appropriate input resistor to allow direct operation from CMOS or PMOS outputs operating supply voltages of 6 to 15V.

The KA2659 is designed for use with standard TTL and Schottky TTL, with which higher output currents are required and loading of the logic output is not a concern. These devices will sink a minimum of 350mA when driven from a "totempole" logic output.

These versatile devices are useful for driving a wide range of loads including Solenoids, Relays, DC motors, LED displays, Filament lamps, thermal printheads and high power buffer. Applications requiring sink currents beyonds the capability of a single output may be accomodated by paralleling the outputs.



ORDERING INFORMATION

Device	Package	Input Level	Operating Temperature
KA2655N	16 DIP	DTL, TTL, PMOS, CMOS	−20 ~ +85°C
KA2655D	16 SOP		
KA2656N	16 DIP	PMOS	
KA2656D	16 SOP		
KA2657N	16 DIP	TTL, CMOS	
KA2657D	16 SOP		
KA2658N	16 DIP	CMOS, PMOS	
KA2658D	16 SOP		
KA2659N	16 DIP	TTL	
KA2659D	16 SOP		

APPLICATIONS

- Relay driver
- DC motor driver
- Solenoids driver
- LED display driver
- Filament lamp driver
- High power buffer
- Thermal print head driver

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (KA2656/7/8)	V_{IN}	30	V
(KA2659)		15	
Continuous Collector Current	I_C	500	mA
Continuous Input Current	I_{IN}	25	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	Ta	−20 ~ +85	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, unless otherwise noted)

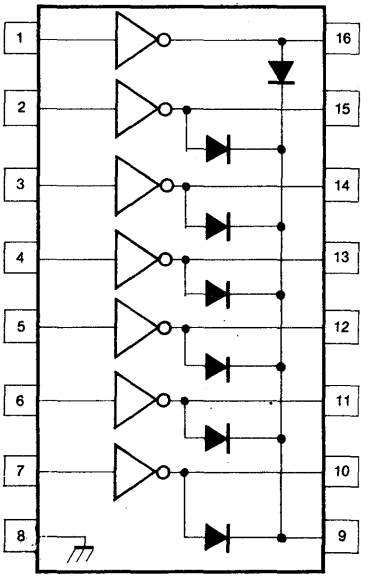
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Output Leakage Current	I_{LK}	V_{CE} = 50V, Ta = 25°C V_{IN} = open			50	μA
		V_{CE} = 50V, Ta = 70°C V_{IN} = open			100	
		V_{CE} = 50V, Ta = 70°C V_{IN} = 6.0V (KA2656)			500	
		V_{CE} = 50V, Ta = 70°C V_{IN} = 1.0V (KA2658)			500	
Output Saturation Voltage	V_{sat}	I_C = 100mA, I_{IN} = 250μA		0.9	1.1	V
		I_C = 200mA, I_{IN} = 350μA		1.1	1.3	
		I_C = 350mA, I_{IN} = 500μA		1.25	1.6	
Input Current 1 (Off Condition)	$I_{IN}1$	I_C = 500μA, Ta = 70°C	50	65		μA
Input Current 2 (On Condition)	$I_{IN}2$	V_{IN} = 17V (KA2656), V_O = open		0.85	1.3	mA
		V_{IN} = 3.85V (KA2657), V_O = open		0.93	1.35	
		V_{IN} = 5V (KA2658), V_O = open		0.35	0.5	
		V_{IN} = 12V (KA2658), V_O = open		1.0	1.45	
		V_{IN} = 3.0V (KA2659), V_O = open		1.5	2.4	
Input Voltage	V_{IN}	V_{CE} = 2.0V, I_C = 300mA (KA2656)			13	V
		V_{CE} = 2.0V, I_C = 200mA (KA2657)			2.4	
		V_{CE} = 2.0V, I_C = 250mA (KA2657)			2.7	
		V_{CE} = 2.0V, I_C = 300mA (KA2657)			3.0	
		V_{CE} = 2.0V, I_C = 125mA (KA2658)			5.0	
		V_{CE} = 2.0V, I_C = 200mA (KA2658)			6.0	
		V_{CE} = 2.0V, I_C = 275mA (KA2658)			7.0	
		V_{CE} = 2.0V, I_C = 350mA (KA2658)			8.0	
		V_{CE} = 2.0V, I_C = 350mA (KA2659)			2.4	

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, unless otherwise noted)

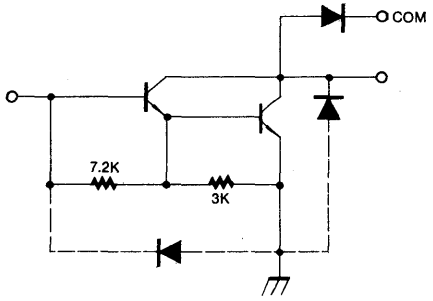
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
DC Current Gain	h_{FE}	V_{CE} = 2.0V, I_C = 350mA (KA2655)	1000			
Input Capacitance	C_{IN}			15	30	pF
Propagation Delay Time	t_{ON}	0.5 V_{IN} to 0.5 V_O		0.25	1.0	μS
	t_{OFF}	0.5 V_{IN} to 0.5 V_O		0.25	1.0	μS
Clamp Diode Leakage Current	I_R	V_{IN} = open, V_O = GND, V_R = 50V, Ta = 25°C			50	μA
		V_{IN} = open, V_O = GND, V_R = 50V, Ta = 70°C			100	μA
Clamp Diode Forward Voltage	V_F	I_F = 350mA		1.7	2.0	V

PIN CONFIGURATION



SCHEMATIC DIAGRAMS

KA2655 (each driver)



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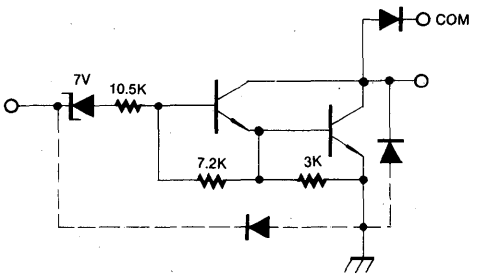
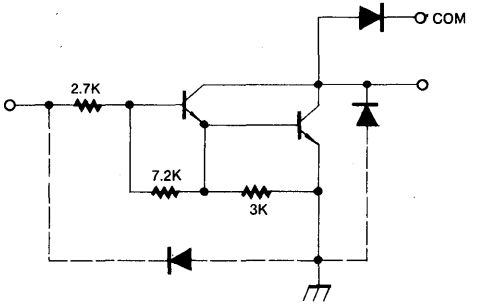
SCHEMATIC DIAGRAMS

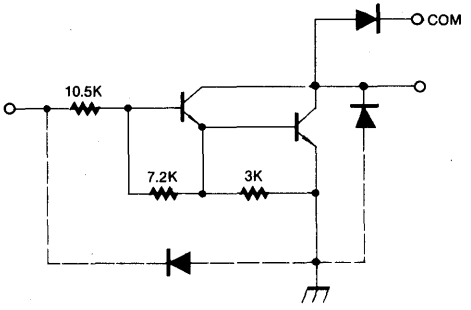
KA2656 (each driver)



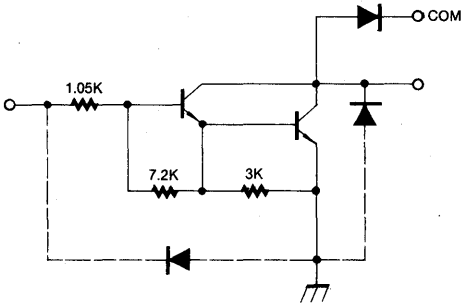
KA2657 (each driver)



KA2658 (each driver)



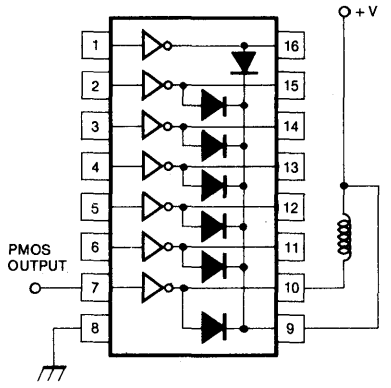
KA2659 (each driver)



TYPICAL APPLICATIONS

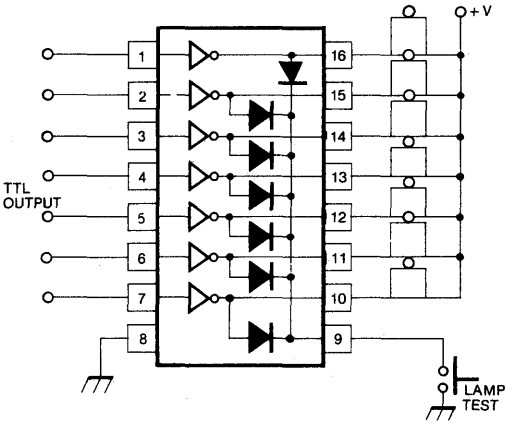
PMOS TO LOAD

KA2656



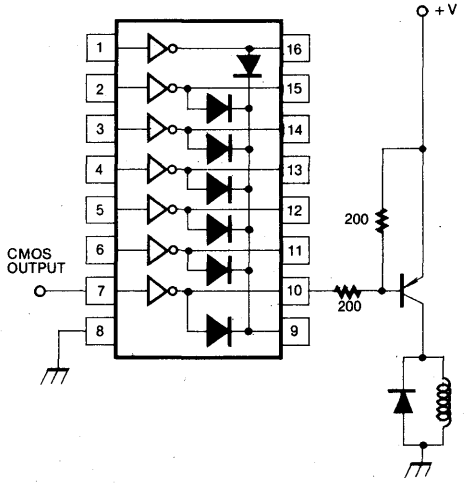
TTL TO LOAD

KA2657/9



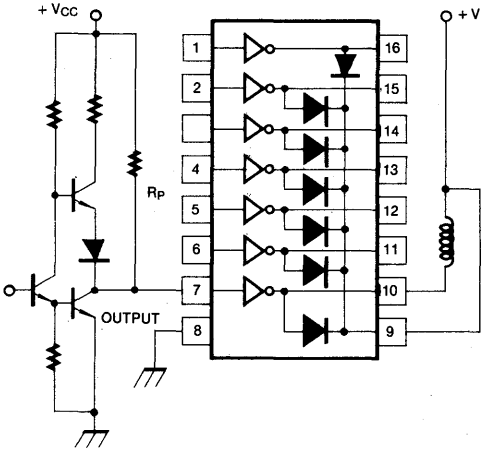
BUFFER FOR HIGH-CURRENT LOAD

KA2658



USE OF PULL-UP RESISTORS TO INCREASE DRIVE CURRENT

KA2657

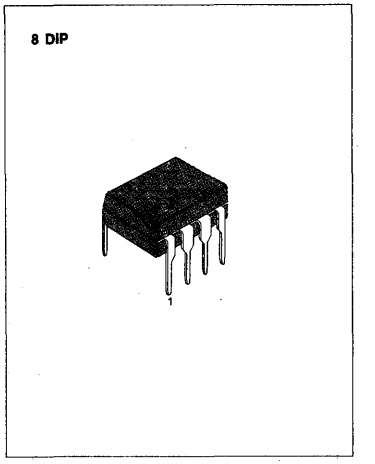


5

LOW POWER CONSUMPTION EARTH LEAKAGE DETECTOR

The KA2803 is designed for use in earth leakage circuit interrupters, for operation directly off the AC line in breakers. The input of the differential amplifier is connected to the secondary coil of ZCT (Zero Current Transformer). The amplified output of differential amplifier is integrated at external capacitor to gain adequate time delay that is specified in KSC4613.

The level comparator generates high level when earth leakage current is greater than some level.



FUNCTIONS

- Differential amplifier
- Level camparator
- Latch circuit

FEATURES

- **Low power consumption (P_d=5mW, 100V/200V)**
- **Built-in voltage regulator**
- **High gain differential amplifier (V_T=13.5mV)**
- **1mA output current pulse to trigger SCR'S**
- **Low external part count, economic**
- **Mini-dip package (8 Dip), high packing density**
- **High noise immunity, large surge margin**
- **Super temperature characteristic of input sensitivity**
- **Wide operating temperature range (T_a=−25°C ~ +80°C)**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2803N	8 DIP	−20 ~ +80°C
KA2803D	8 SOP	

APPLICATION CIRCUIT

1. Full Wave Application Circuit

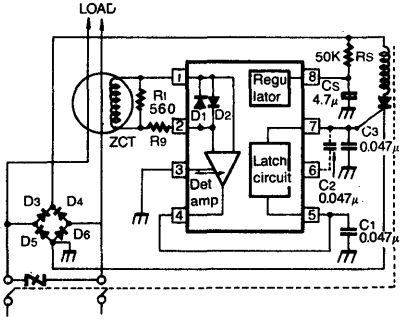


Fig. 1

2. Half Wave Application Circuit

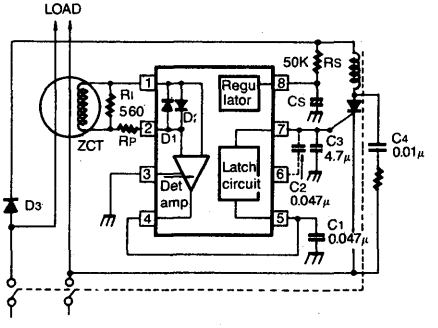


Fig. 2

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	20	V
Supply Current	I_S	8	mA
Power Dissipation	P_D	300	mW
Lead Temperature (soldering 10 sec)	T_{lead}	260	°C
Operating Temperature	T_{opr}	−25 ~ +80	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS (T_a=25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current 1	I_{S1}	V_{CC}=12V (−25°C) V_R-V_I=300mV (25°C) (80°C)		400	580 530 480	μA μA μA
Trip Voltage		V_{CC}=16V (−25°C ~ 80°C) V_R-V_I=X	10	13.5	17	mVrms
Differential Amplifier Output Current 1	I_{TDI}	V_{CC}=16V (25°C) V_R-V_I=30mV V_{OD}=1.2V	12		30	μA
Differential Amplifier Output Current 2	I_{TD2}	V_{CC}=16V (25°C) V_{OD}=0.6V V_R, V_1 short	17		37	μA
Output Current	I_O	V_{SC} = 1.4V V_{OS}=0.8V V_{CC} = 12V (−25°C) (+25°C) (+80°C)	 −200 −100 −75			 μA μA μA
Latch on Voltage	V_{scon}	V_{CC}=16V (25°C)	0.7		1.4	V
Latch Input Current	I_{scon}	V_{CC}=12V (25°C)			5	μA
Output Low Current	I_{OSL}	V_{CC}=12V (−25 ~ 80°C) V_{OSL}=0.2V	200			μA
Diff. Input Clamp Voltage	V_{IDC}	I_{IDC}=100mA (−25 ~ 80°C)	0.4		2	V
Maximum Current Voltage	V_{SM}	I_{SM}=7mA (−25°C)	20		28	V
Supply Current 2	I_{S2}	V_R-V_I=X (25 ~ 80°C) V_{OS}=0.6			900	μA
Latch Off Supply Voltage	V_{soff}	V_{os}=high (25°C)	7.0			V
Response Time	T_{on}	V_{CC}=16V (25°C) V_R-V_I=0.3V	2		4	msec

5

APPLICATION NOTE

(refer to full wave application circuit Fig. 1)

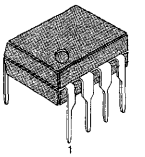
The Fig 1 shows the KA2803 connected in a typical leakage current detector system.
The power is applied to the V_{CC} terminal (Pin 8) of the KA2803 directly from the power line.
The resistor R_S and capacitor C_S are chosen so that pin 8 voltage is at least 12V.
The value of C_S is recommended above 1μF at this time.
If the leakage current is at the load, it is detected by the zero current transformer (ZCT).
The output voltage signal of ZCT is amplified by the differential amplifier of the KA2803 internal circuit and appears as half-cycle sine wave signal referred to input signal at the output of the amplifier.
The amplifier closed loop gain is fixed about 1000 times with internal feedback resistor to compensate for zero current transformer (ZCT) Variations.
The resistor R_L should be selected so that the breaker satisfies the required sensing current.
The protection resistor R_P is not usually used put when the high current is injected at the breaker, this resistor should be used to protect the earth leakage detector IC the KA2803.
The range of R_P is from several hundred Ω to several kΩ.
The capacitor C_1 is for the noise canceller and standard value of C_1 is 0.047μF. Also the capacitor C_2 is noise canceller capacitance but it is not usually used.
When high noise is only appeared at this system 0.047μF capacitor may be connected between pin 6 and pin 7.
The amplified signal is finally appeared to the Pin 7 with pulse signal through the internal latch circuit of the KA2803.
This signal drivies the gate of the external SCR which energizes the trip coil which opens the circuit breaker.
The trip time of breaker is decided by the capacitor C_3 and the mechanism breaker.
This capacitor should be selected under 1μF for the required the trip time.
The full wave bridge supplies power to the KA2803 during both the positive and negative half-cycles of the line voltage.
This allows the hot and neutral lines to be interchanged.
If your application want the detail information, request it on our application circuit designer of KA2803.

ZERO VOLTAGE SWITCH

The KA2804 is a TRIAC controller providing a complete solution for temperature controlled electric panel heaters, cookers, film processing baths etc.

Switching occurs at the zero voltage point in order to minimize radio frequency interference. The device is suitable for mains-on-line operation and requires minimal components.

8 DIP



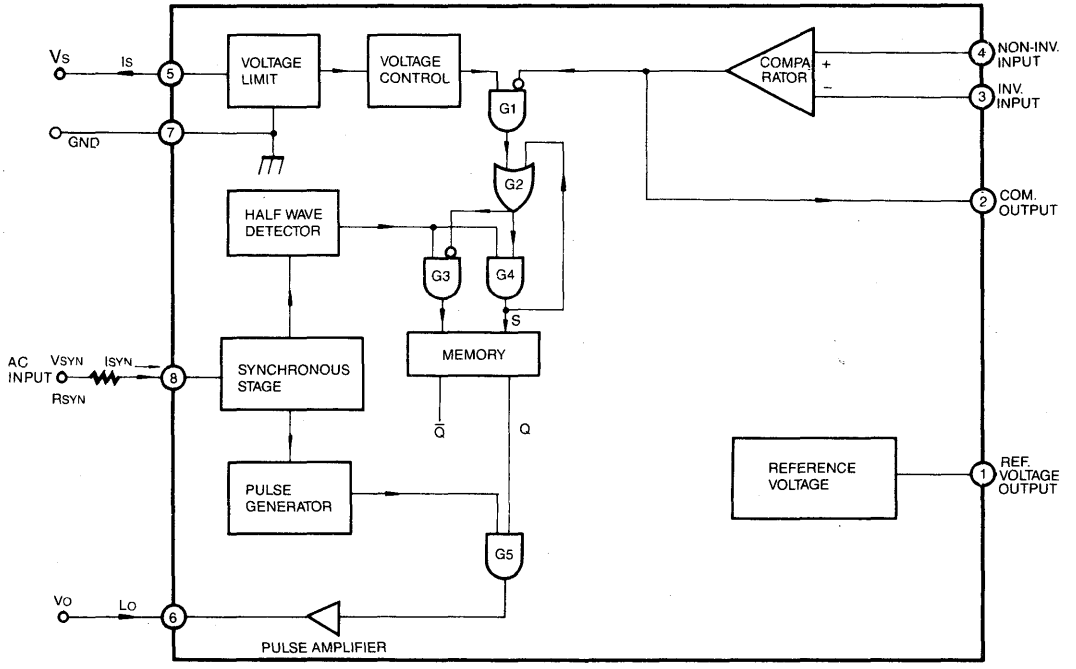
FEATURES

- **Easy operation either through the AC line or a DC supply.**
- **Supply voltage control.**
- **Very few external components.**
- **Symmetrical burst control — No DC current components in the load circuit.**
- **Negative output current pulse up to 250mA-short circuit protection.**
- **Reference voltage output.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2804N	8 DIP	-20 ~ +70°C
KA2804D	8 SOP	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	$-V_S$	8.2	V
Supply Current	$-I_S$	40 (average)	mA
Synchronous Current	I_{SYN}	5.0 (rms)	mA
Input Voltage	V_I	$\leqq \lvert V_S \rvert$	V
Power Dissipation	P_D	350	mW
Junction Temperature	T_J	125	°C
Operating Ambient Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

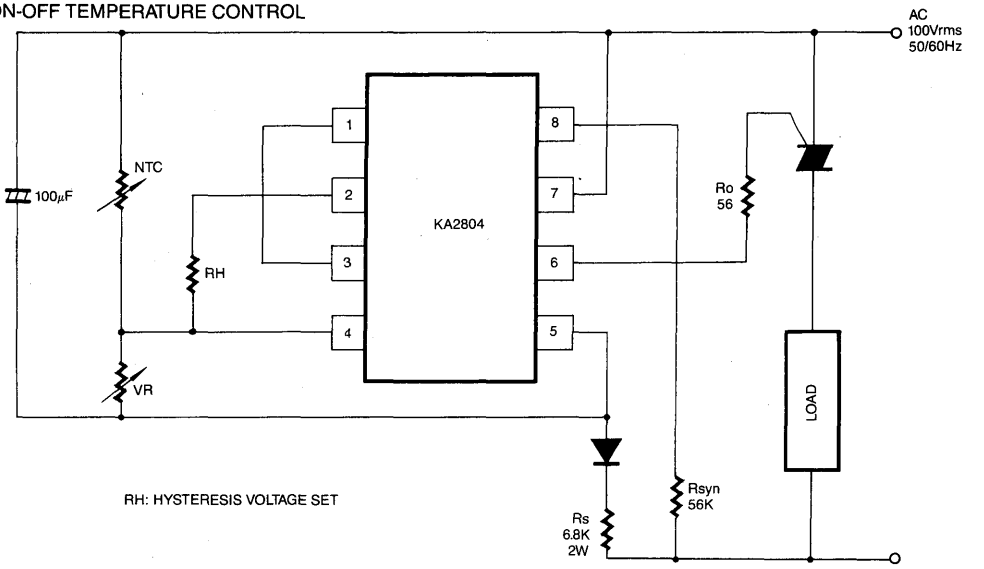
ELECTRICAL CHARACTERISTICS

(V_S =8.0V, V_{SYN} =100 to 115V_{rms}, T_a =25°C, f=50/60Hz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current	$-I_S$	Pin 5, R_{SYN} =56K	—	2.0	2.5	mA
Supply Voltage 1	$-V_S$ 1	Pin 5, I_S =2.5mA R_{SYN} =56K	7.2	—	8.4	V
Supply Voltage 2	$-V_S$ 2	Pin 5, I_S =20mA R_{SYN} =56K	7.2	—	8.6	V
Synchronous Current	I_{SYN}	Pin 8	0.3	—	—	mA
Output Pulse Width	T_P	Pin 6, R_{SYN} =56K	—	200	—	μS
Output Voltage	V_O	Pin 6, $I_O \leqq$ 200mA	4.2	5.2	—	V
Output Current	I_O	Pin 6, $R_O \leqq$ 25	200	250	—	mA
Output Leakage Current	I_{LO}	Pin 6	—	—	2.0	μA
Input Offset Voltage	V_{IO}	Pin 3, 4	—	2.0	5.0	mV
Input Bias Current	I_I	Pin 3, 4	—	0.5	1.0	μA
Common Mode Input Voltage Range	$-V_{ICM}$	Pin 3, 4	0	—	5.7	V
Output Leakage Current	I_{LC}	Pin 2	—	—	0.2	μA
Reference Voltage	$-V_R$	Pin 1, $I_R \leqq$ 1uA	—	3.6	—	V

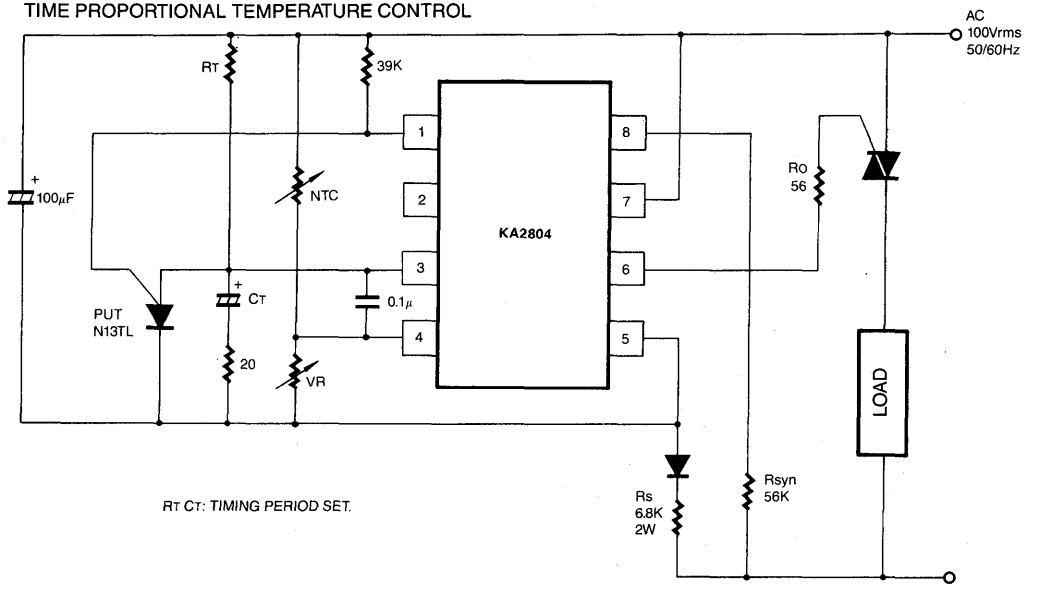
APPLICATIONS

ON-OFF TEMPERATURE CONTROL



RH: HYSTERESIS VOLTAGE SET

TIME PROPORTIONAL TEMPERATURE CONTROL

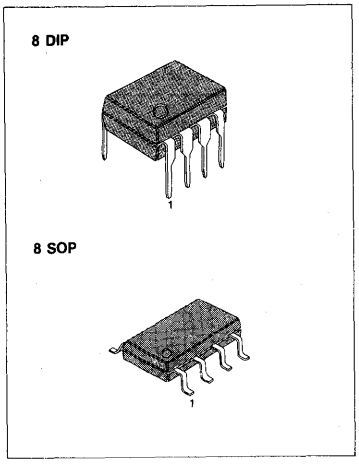


RT CT: TIMING PERIOD SET.

EARTH LEAKAGE DETECTOR

The KA2807 is designed for use in earth circuit interrupters, for operation directly off the AC line interrupters.

Full advantage of the U.S. UL943 timing specification is taken to insure maximum immunity to false triggering due to line noise.



FEATURES

- **Full advantage of the UL943**
- **Externally programmable fault current threshold**
- **Direct interface to SCR**
- **Operates under line reversally both load V_S line and hot V_S neutral**
- **Power supply shunt regulator in chip**
- **Sense coil: 1000:1**
- **GND/Neutral coil: 200:1**
- **Normal fault sensitivity current is 5mA typical**
- **Trip time in normal fault and ground neutral fault is 18ms typical**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2807N	8 DIP	−40 ~ +70°C
KA2807D	8 SOP	

BLOCK DIAGRAM

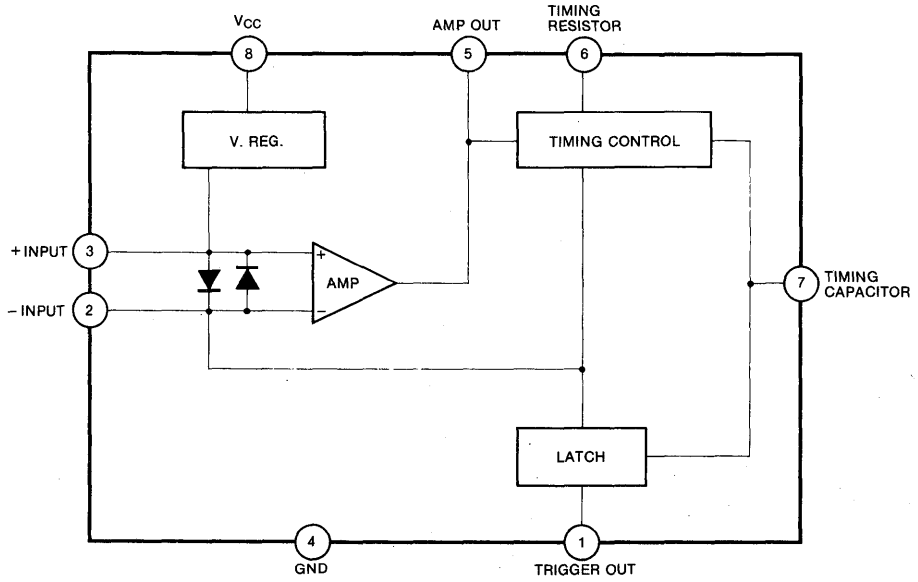


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Current	I_{CC}	19	mA
Power Dissipation	P_D	1250	mW
Operating Temperature Range	T_{opr}	$-40 \sim +70$	°C
Storage Temperature Range	T_{stg}	$-55 \sim +150$	°C

ELECTRICAL CHARACTERISTICS ($Ta = 25°C$, $I_{CC} = 5mA$)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Shunt Regulator Voltage	V_{reg}	Pin 8, S1:2, S2:OFF	22	26	30	V
Amp Reference Voltage	V_{int}	Pin 3, S1:2, S2:OFF	9	10.5	12	V
Amp Output High Voltage	V_{OH}	Pin 5, S1:3, S2:ON Sig: 800Hz, $3.0V_{p-p}$ Sinewave	17	19	21	V
Amp Output Low Voltage	V_{OL}	Pin 5, S1:3, S2:ON Sig: 800Hz, $3.0V_{p-p}$ Sinewave	1	2.5	4	V
Amp Sensitivity Current	I_{SEN}	Pin 2, S1:3, S2:ON Sig: 800Hz, $1.0V_{p-p} \sim 2.5V_{p-p}$ Sinewave	3	5	7	μArms
Latch On Voltage	V_{ON}	Pin 7, S1:3, S2:ON Sig: 800Hz, $3.0V_{p-p}$ Sinewave	15	17.5	20	V
SCR Trigger Current	I_{TR}	Pin 1, S1:3, S2:ON Sig: 800Hz, $3.0V_{p-p}$ Sinewave	0.5	1	2.4	mA
Output Low Voltage	V_S1	Pin 1, S1:2, S2:OFF		100	240	mV
Output Impedance	R_O	Pin 1, S1:2, S2:OFF		100		Ω
Output Sink Current	I_{sink}	Pin 1, S1:2, S2:OFF	2.0	5		mA

5

TEST CIRCUIT

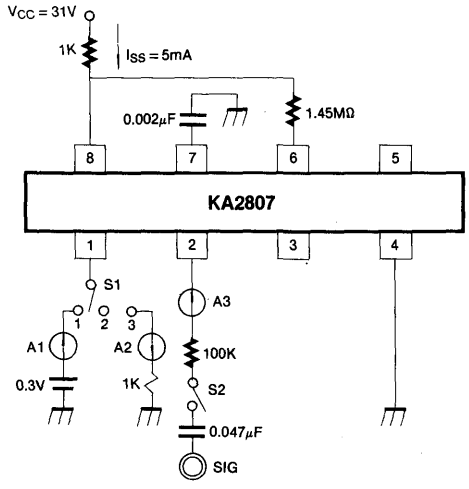
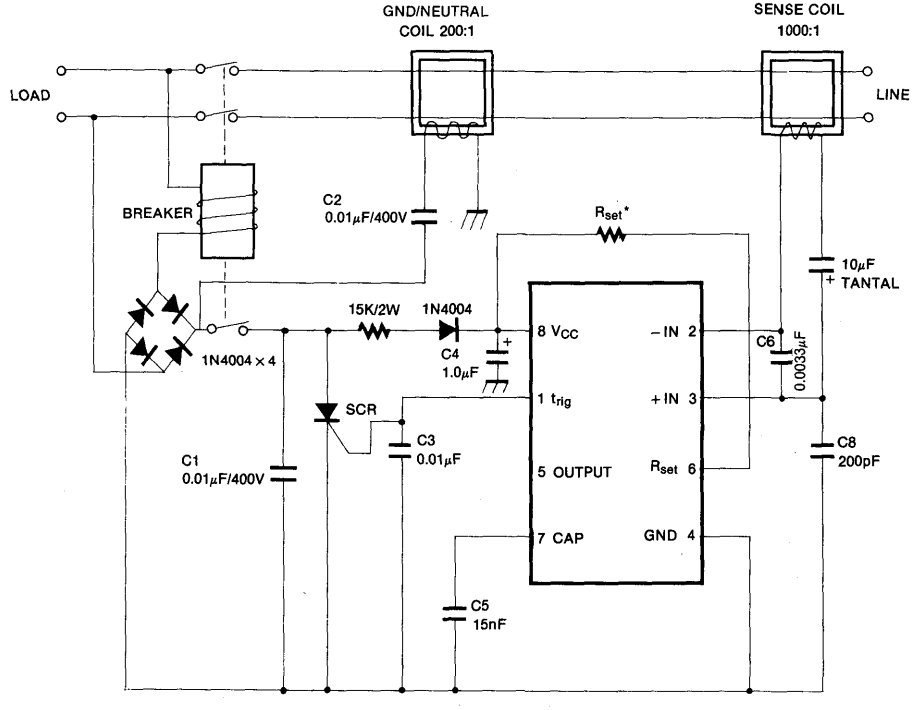


Fig. 2

APPLICATION CIRCUIT



* Adjust R_{set} for desired sensitivity leakage current.

Fig. 3

Typical earth leakage detector circuit is shown in Fig. 3. This is designed to operate on 120V AC line voltage with 5mA normal fault sensitivity. Full-wave rectifier diode and 15K/2W resistor are used to supply the DC power supply required by the KA2807 C4 (1μF) is used to filter the ripple of the supply voltage and peak current when fault current generate over 5mA typical, SCR is turned ON and a large current can flow through the breaker coil to pull the contact open. Once opened, the fault condition is removed and the discharge current 3 I_{th} reset both the timing capacitor and output latch causing the SCR to turn off.
A1000:1 Sense coil is used to detect the normal fault. The fault current generated is stepped down by 1000 and fed into the input pins of the OP amp through C7 (10μF) capacitor.
C6 (0.0033μF) and C8 (200pF) are added to obtain better noise immunity. The normal fault sensitivity current is determined by discharging current of timing capacitor.

Discharging current I_{th} is $\frac{7V}{R_{set} \times 2}$ ..... (1)

Because the average fault current just equals the threshold current I_{th} at the decision point.

$I_{th} = \frac{I_{f(rms)} \times 0.91}{2}$ ..... (2)

The factor 0.91 converts the rms value to an average value.

in (1) and (2) $R_{set} = \frac{7V}{I_{f(rms)} \times 0.91}$ ..... (3)

The precision value of R_{set} depends on the specific sense coil used KA2807 tolerances in as much as UL943 specifies a sensitivity "window" of 4mA-6mA, provision should be made to adjust R_{set} on a per-product bisic. You can be obtained the desired integration time through proper selection of the timing capacitor C5.
The sense amplifier is capacitively coupled to a 200-turn coil in order to detect the grounded neutral fault.
In FIG. 3, grounded neutral detection is accomplished by feeding the neutral coil with 120Hz energy continuously and allowing some of this energy to couple into the sense coil during conditions of neutral fault.

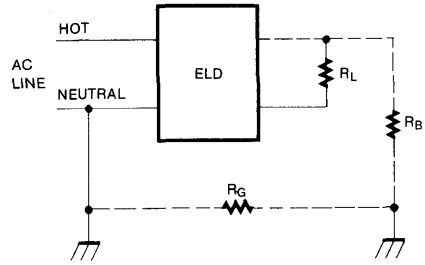


FIG. 4 NORMAL FAULT

Explain: An unintentional electrical path, R_B, between the load terminal of the hot line and the ground, as shown by the dashed lines.

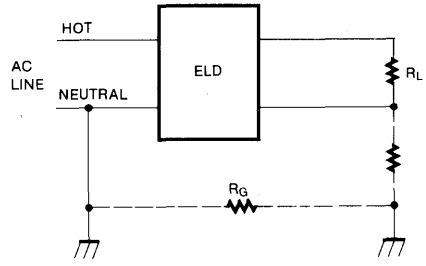


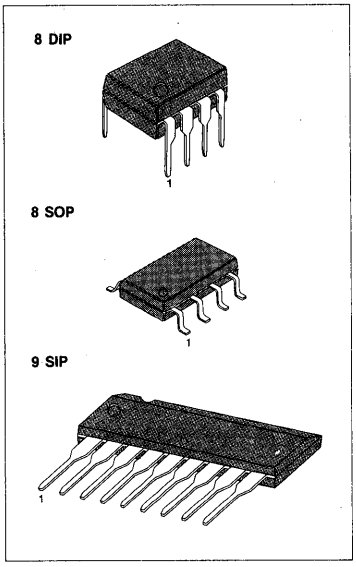
FIG. 5 GROUNDED NEUTRAL FAULT

Explain: An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines.

LOW VOLTAGE AUDIO POWER AMPLIFIER

The LM386/S/D is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 30 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.



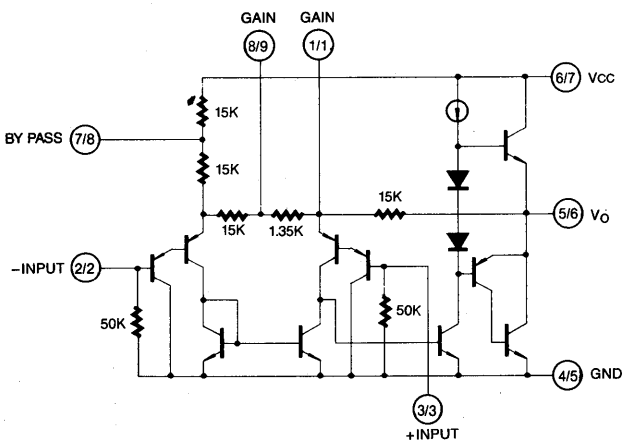
FEATURES

- **Battery operation.**
- **Minimum external parts.**
- **Wide supply voltage range: 4V ~ 12V (LM386)**
  4V ~ 9V (LM386S/D)
- **Low quiescent current drain (4mA.)**
- **Voltage gains : 20 ~ 200.**
- **Ground referenced input.**
- **Self-centering output quiescent voltage.**
- **Low distortion.**
- **3 kinds of package types**
  LM386 (8 Dip), LM386S (9 Sip), LM386D (8 Sop)

ORDERING INFORMATION

Device	Package	Operating Temperature
LM386N	8 DIP	−20°C ~ +70°C
LM386S	9 SIP	
LM386D	8 SOP	

SCHEMATIC DIAGRAMS



⊘ : LEFT (LM386/D)
RIGHT (LM386S)

Fig. 1

CONNECTION DIAGRAM

(LM386/D)

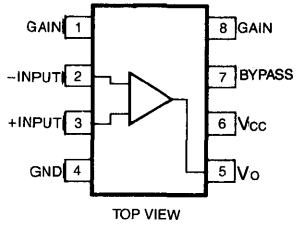


Fig. 2

(LM386S)

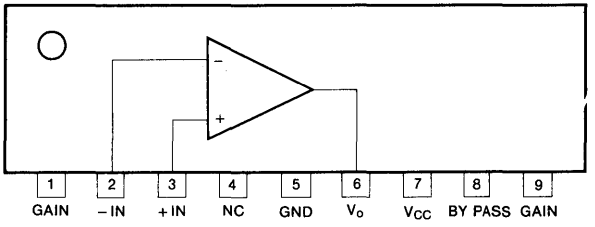


Fig. 3

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	15	V
Power Dissipation	LM386	P_d	660	mW
	LM386S		500	
	LM386D		300	
Input Voltage		V_i	±0.4	V
Operating Temperature		T_{opr}	−20 ~ +70	°C
Storage Temperature		T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 6V, R_L = 8Ω, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescient Circuit Current	I_{CC}	V_i = 0		4	8	mA
Output Power	P_o	V_{CC} = 6V, THD = 10%	250	325		mW
		V_{CC} = 9V, THD = 10%	500	700		mW
Voltage Gain (D-Type)	A_V	Pins 1 and 8 Open		26		dB
		10μF from Pin 1 to 8		46		
Bandwidth (D-Type)	BW	Pins 1 and 8 Open		300		KHz
		10μF from Pin 1 to 8		60		
Total Harmonic Distortion (D-Type)	THD	P_o = 125mW, Pins 1 and 8 Open		0.2		%
Input Resistance	R_i			50		KΩ
Input Bias Current	I_b	Pins 1 and 8 Open		250		nA

TYPICAL APPLICATIONS (LM386/D)

Amplifier with Gain=50 (34 dB)

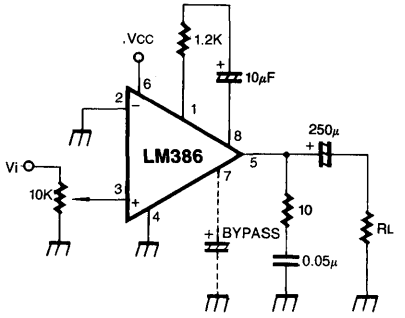


Fig. 4

Low Distortion Power Wienbridge Oscillator

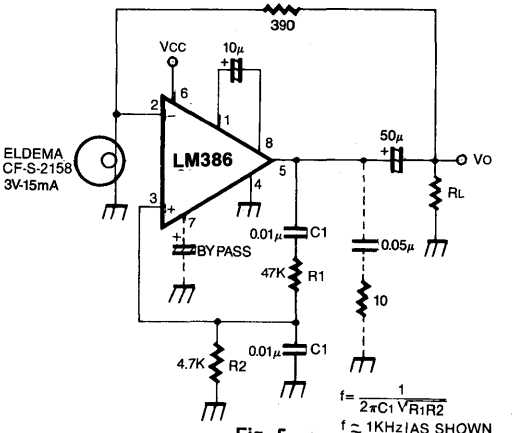


Fig. 5

Square Wave Oscillator

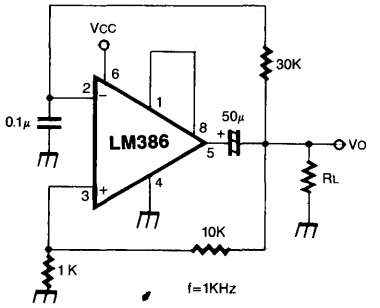


Fig. 6

Amplifier with Bass Boost

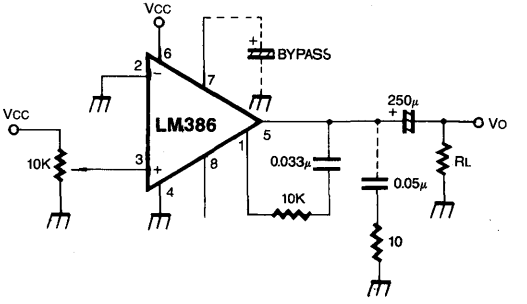


Fig. 7

AM Radio Power Amplifier

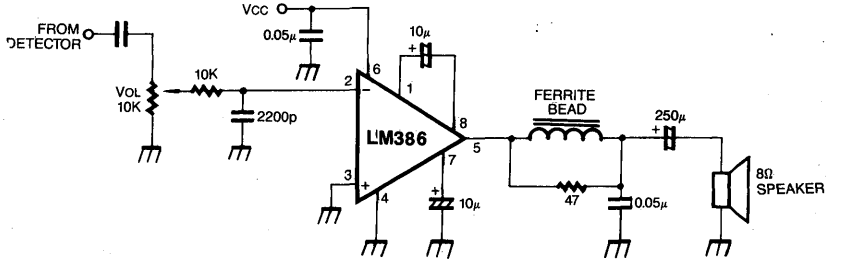
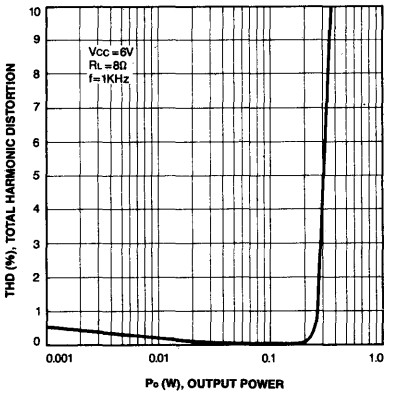
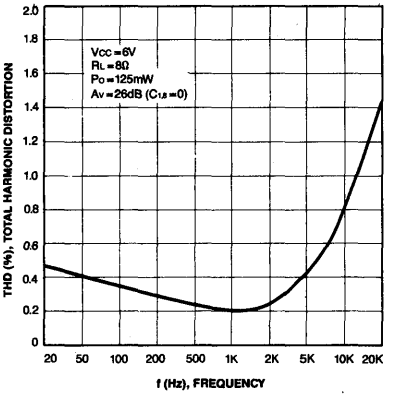


Fig. 8

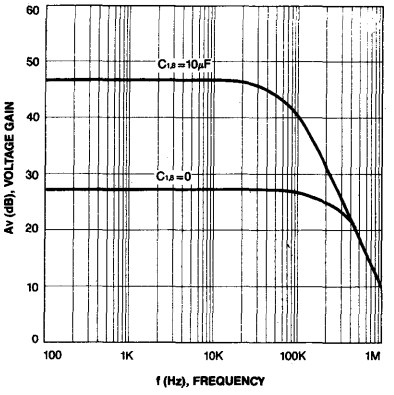
TOTAL HARMONIC DISTORTION-OUTPUT POWER



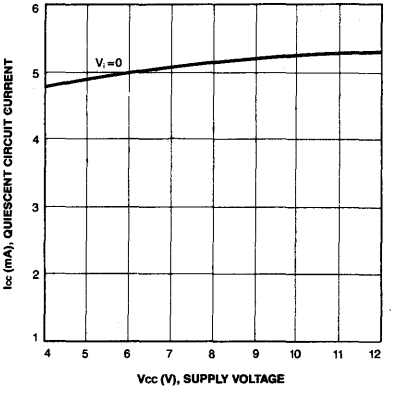
TOTAL HARMONIC DISTORTION-FREQUENCY



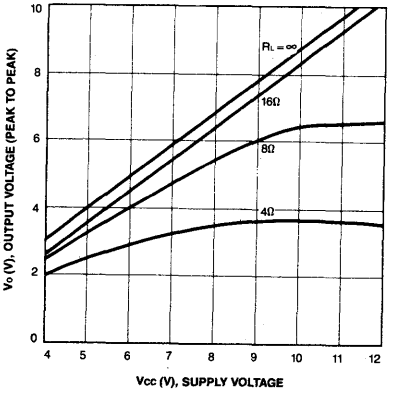
VOLTAGE GAIN—FREQUENCY



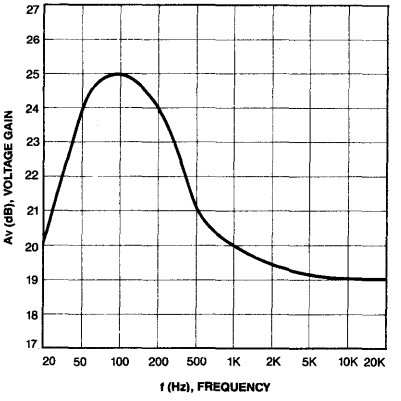
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING-SUPPLY VOLTAGE

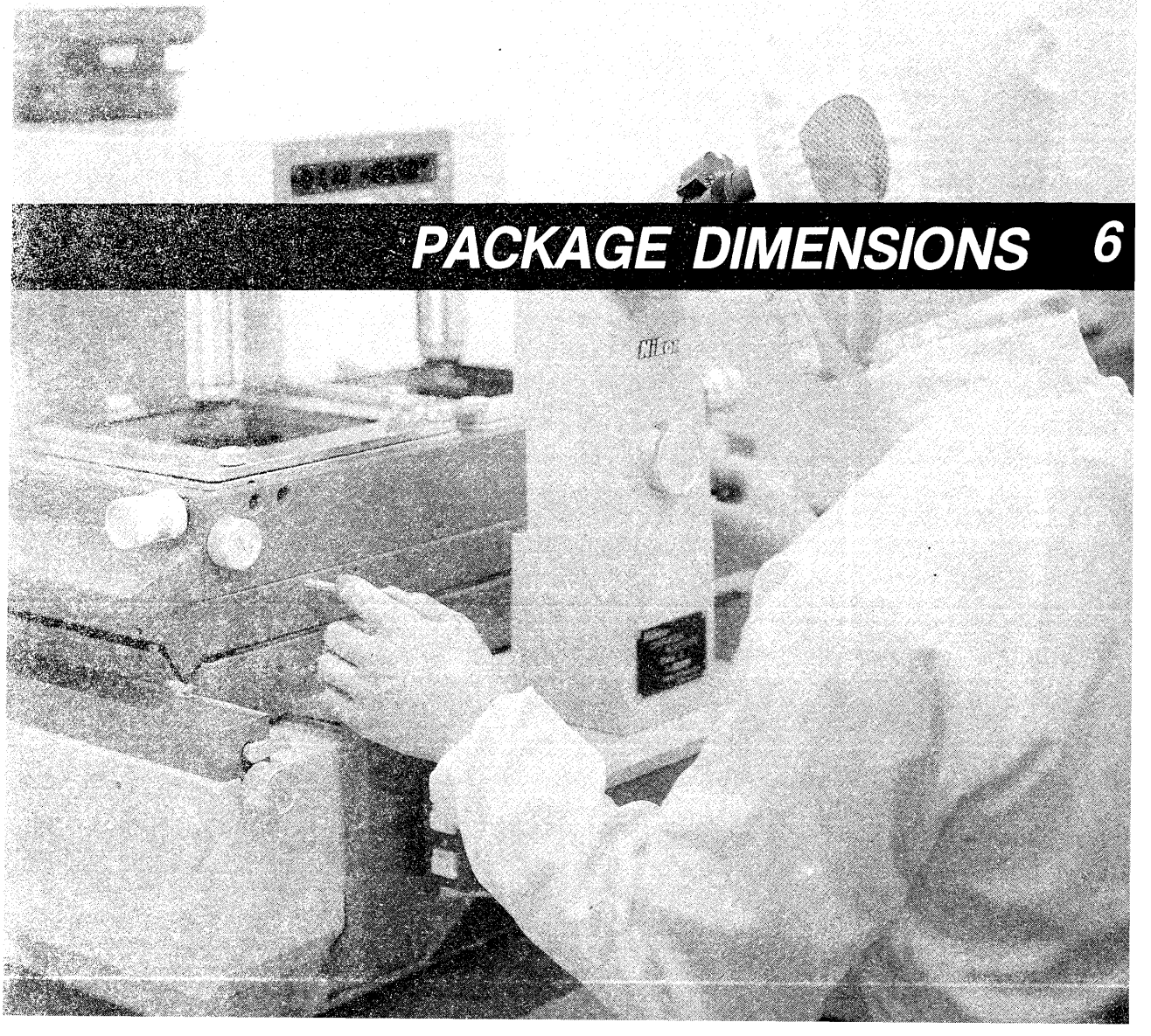


FREQUENCY RESPONSE WITH BASS BOOST



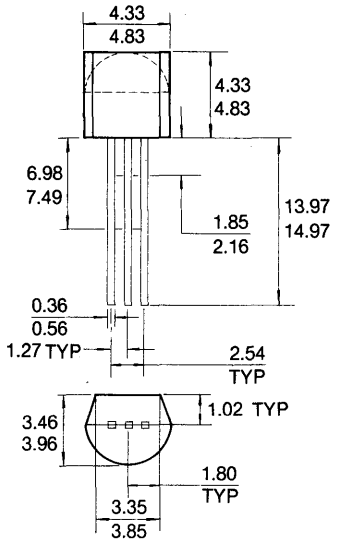
NOTES

PACKAGE DIMENSIONS 6



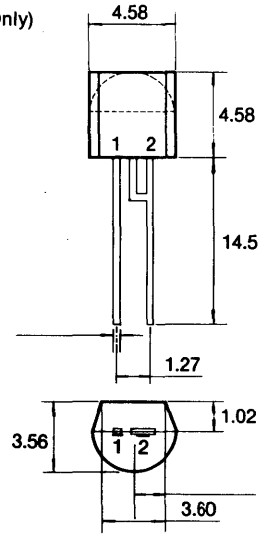
PACKAGE DIMENSIONS

TO-92 **Unit: mm**



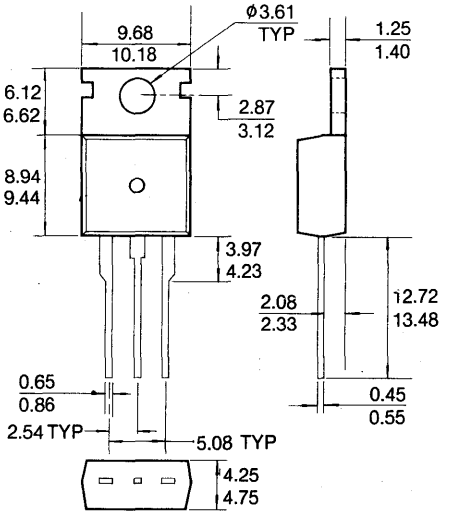
TO-92 **Unit: mm**

(KA33V Only)

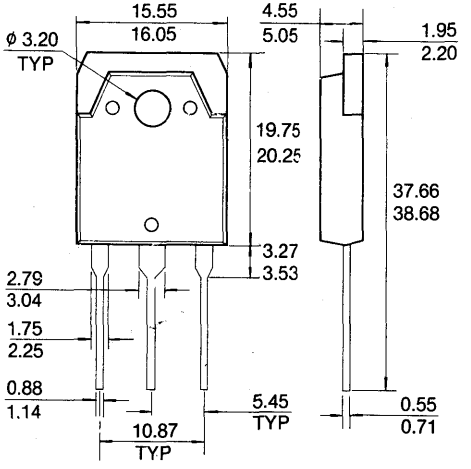


1. Anode 2. Cathode

TO-220 **Unit: mm**



TO-3P **Unit: mm**

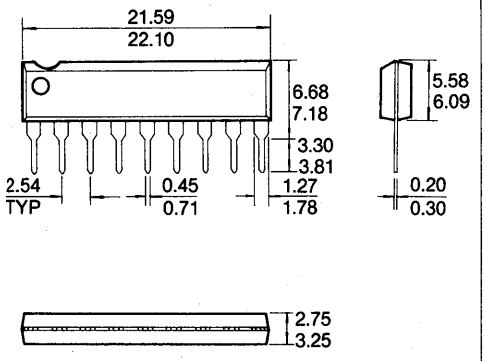


6

PACKAGE DIMENSIONS

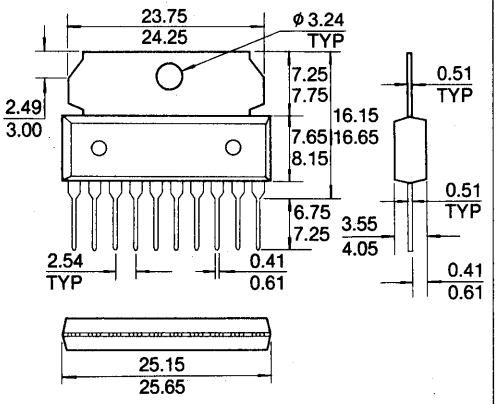
9 SIP

Unit: mm



10 SIP H/S

Unit: mm



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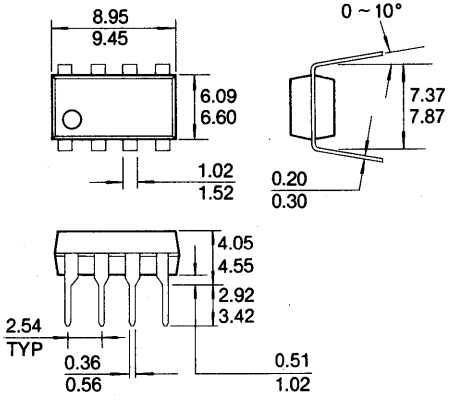
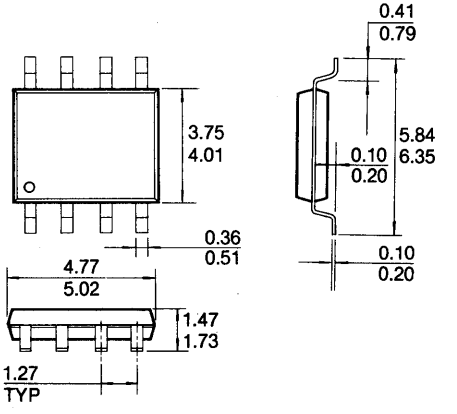
Unit: mm



8 SOP

Unit: mm



PACKAGE DIMENSIONS

14 DIP

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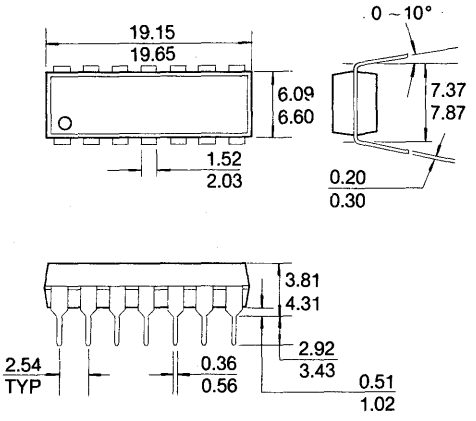

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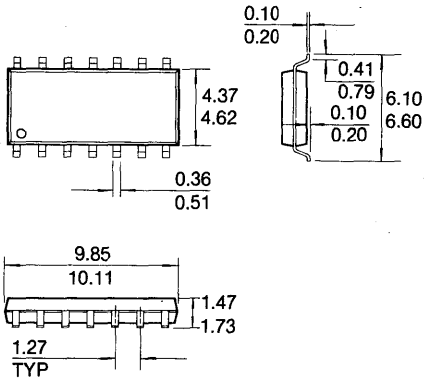

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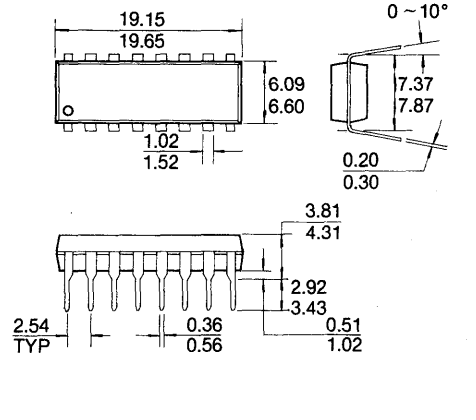

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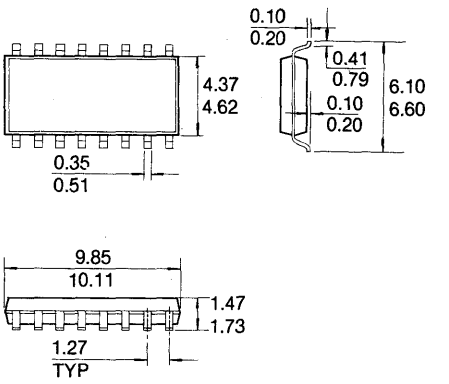

PACKAGE DIMENSIONS

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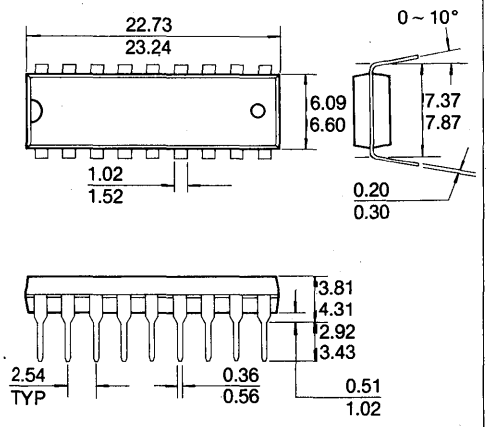
Unit: mm



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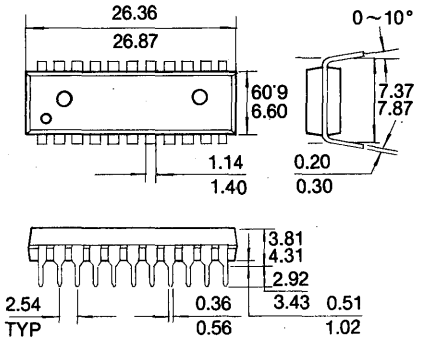
Unit: mm



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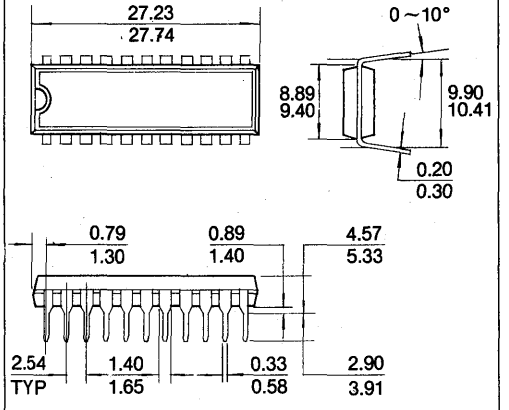

22 DIP (Shrink)

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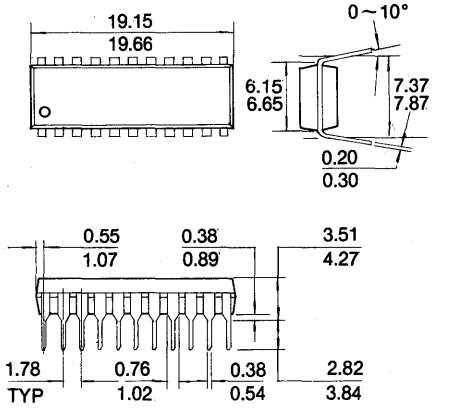

PACKAGE DIMENSIONS

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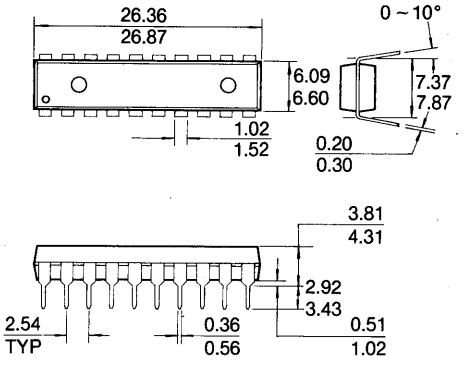
Unit: mm



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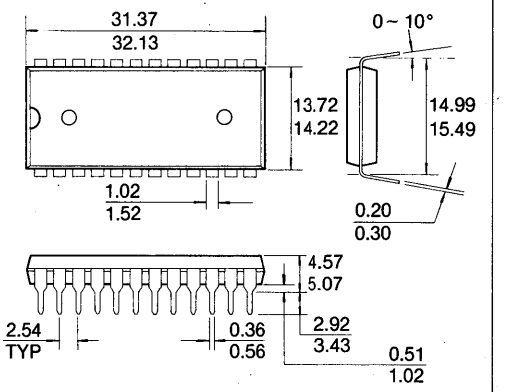

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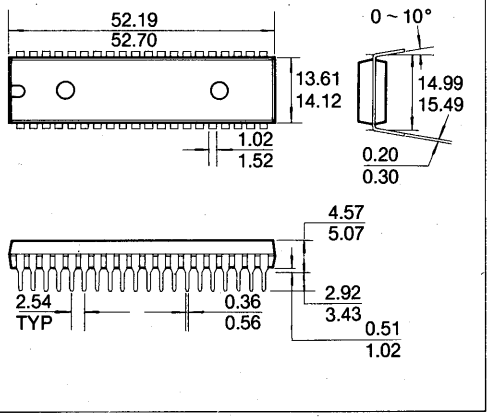

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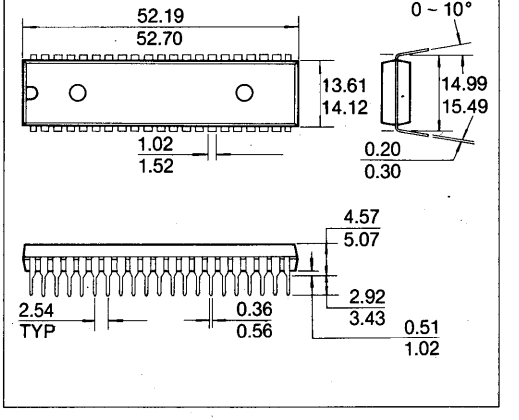

6

PACKAGE DIMENSIONS

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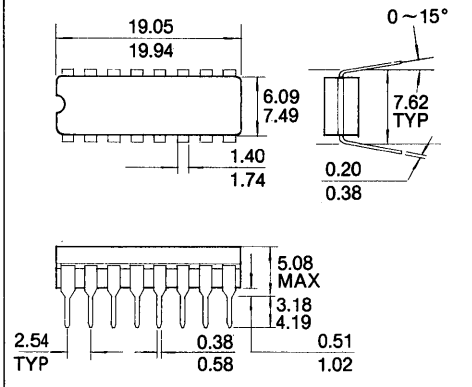

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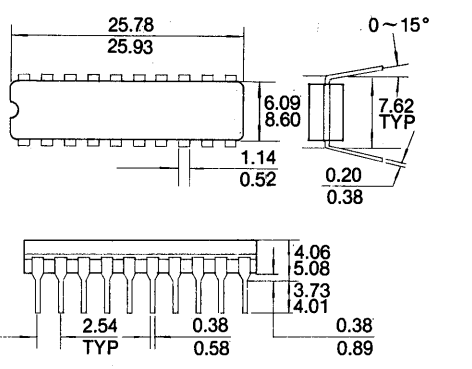

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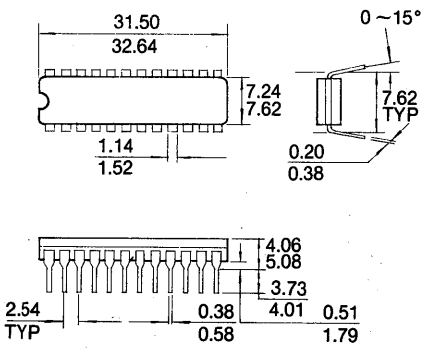

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