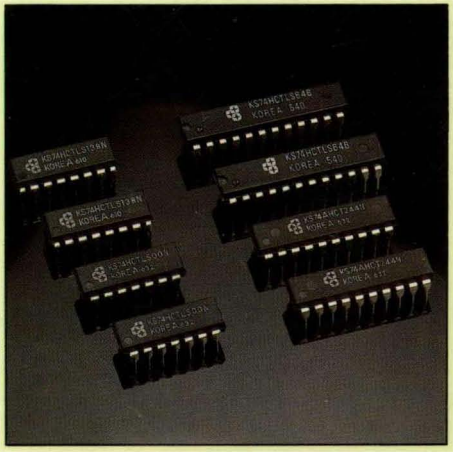
SAMSUNG

High Performance CMOS Logic Data Book



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INTRODUCTION

Samsung Semiconductor is a broad-line manufacturer of semiconductors that range from VLSI circuits such as memories (DRAM, SRAM, EPROM and EEPROM), microprocessors, gate arrays and programmable logic to transistors, linear circuits and telecommunications products.

The KS54/74AHCT and the KS54/74HCTLS high-performance CMOS logic families are Samsung's entry into the general purpose digital logic area.

The KS54/74AHCT advanced high-speed CMOS family is designed to provide performance equivalent to or better than that of the bipolar 54/74ALS (Advanced Low-power Scholttky) family with the additional CMOS advantages of low power dissipation and high noise immunity. The AHCT parts can therefore be used as direct plug-in replacements for their ALS counterparts (and in most applications for FAST and Schottky) and improve the system performance.

The 54/74HCTLS high-speed CMOS family offers similar benefits as a replacement for industry-standard 54/74LS (Low-power Schottky), 54/74HCT and 54/74HC. While meeting all of the HCT electrical specifications, it also provides improved speed and drive capability, so that LS parts can be replaced with no performance degradation.

High Performance CMOS Logic Data Book

KS54/74AHCT
Advanced High-Speed CMOS

KS54/74HCTLS
High-Speed CMOS

SAMSUNG SEMICONDUCTOR DATA BOOK LIST

I. Semiconductor Product Guide

II. Transistor Data Book

III. Linear IC Data Book

IV. MOS Product Data Book

V. High Performance CMOS Logic Data Book

VI. MOS Memory Data Book

VII. SFET Data Book

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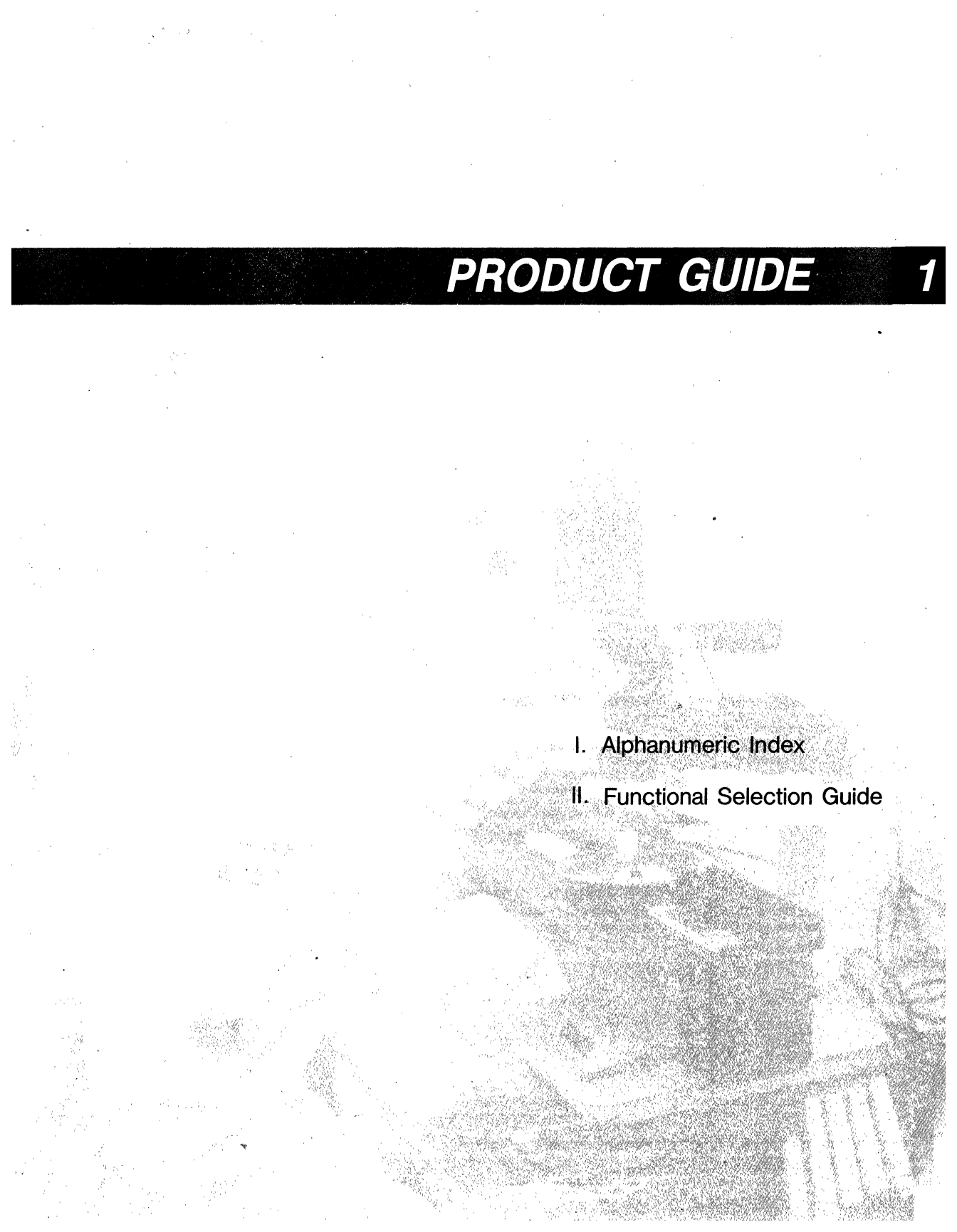

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KS54/74AHCT Family (continued)

KS54/74AHCT Family (continued)

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2. Functional Selection Guide

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	02	Quad 2-Input NOR Gates	14 DIP
	03	Quad 2-Input NAND Gates with Open-Drain Outputs	14 DIP
	04	Hex Inverters	14 DIP
	05	Hex Inverters with Open-Drain Outputs	14 DIP
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	10	Triple 3-Input NAND Gates	14 DIP
	11	Triple 3-Input AND Gates	14 DIP
	12	Triple 3-Input NAND Gates with Open-Drain Outputs	14 DIP
	14	Hex Schmitt-Trigger Inverters	14 DIP
	20	Dual 4-Input NAND Gates	14 DIP
	21	Dual 4-Input AND Gates	14 DIP
	22	Dual 4-Input NAND Gates with Open-Drain Outputs	14 DIP
	27	Triple 3-Input NOR Gates	14 DIP
	30	8-Input NAND Gate	14 DIP
	32	Quad 2-Input OR Gates	14 DIP
	51	Dual AND-OR-Invert Gates	14 DIP
	58	Dual AND-OR Gates	14 DIP
	86	Quad 2-Input Exclusive-OR Gates	14 DIP
	132	Quad 2-Input NAND Gates with Schmitt-Trigger Inputs	14 DIP
	133	13-Input NAND Gates	16 DIP
	266	Quad Exclusive-NOR Gates with Open Drain Outputs	14 DIP
Buffers and Line Drivers	125	Quad Buffers with 3-State Outputs	14 DIP
	126	Quad Buffers with 3-State Outputs	14 DIP
	210	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	240	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	241	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	244	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	365	Hex Bus-Drivers with 3-State Outputs	16 DIP
	366	Hex Bus-Drivers with 3-State Outputs	16 DIP
	367	Hex Bus-Drivers with 3-State Outputs	16 DIP
	368	Hex Bus-Drivers with 3-State Outputs	16 DIP
	465	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	466	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	467	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
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	78	Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear and Common Clock	14 DIP
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	109	Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flops with Preset and Clear	16 DIP

Functional Selection Guide (continued)

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	174	Hex D-Type Flip-Flops with Clear	16 DIP
	175	Quad D-Type Flip-Flops with Clear	16 DIP
	273	Octal D-Type Flip-Flops with Clear	20 DIP
	374	Octal D-Type Flip-Flops with 3-State Outputs	20 DIP
	377	Octal D-Type Flip-Flops with Clock Enable	20 DIP
	399	Quad 2-Port Registers	16 DIP
	534	Octal D-Type Flip-Flops with 3-State	20 DIP
	564	Octal D-Type Flip-Flops with 3-State	20 DIP
	574	Octal D-Type Flip-Flops with 3-State	20 DIP
	670	4-By-4-Register Files with 3-State Outputs	16 DIP
	794	Octal Register with Readback	20 DIP
	821	10 Bit BUS Interface Registers with 3-State Outputs	24 DIP
	822	10 Bit BUS Interface Registers with 3-State Outputs	24 DIP
	823	9-Bit BUS Interface Registers with 3-State Outputs	24 DIP
	824	9-Bit BUS Interface Registers with 3-State Outputs	24 DIP
	825	8-Bit BUS Interface Registers with 3-State Outputs	24 DIP
	826	8-Bit BUS Interface Registers with 3-State Outputs	24 DIP
Latches	75	Quad Bistable Transparent Latches	16 DIP
	77	Quad D-Type Latches	14 DIP
	259	8-Bit Addressable Latches	16 DIP
	373	Octal D-Type Transparent Latches with 3-State Outputs	20 DIP
	533	Octal D-Type Transparent Latches with 3-State Outputs	20 DIP
	563	Octal D-Type Transparent Latches with 3-State Outputs	20 DIP
	573	Octal D-Type Transparent Latches with 3-State Outputs	20 DIP
	793	Octal D-Type Transparent Latches with Readback	20 DIP
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	842	10-Bit Bus Interface D-Type latches with 3-State Outputs	24 DIP
	843	9-Bit Bus Interface D-Type latches with 3-State Outputs	24 DIP
	844	9-Bit Bus Interface D-Type latches with 3-State Outputs	24 DIP
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	258	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs	16 DIP
	352	Dual 1-of-4 Data Selectors/Multiplexers	16 DIP
	353	1-of-4 Data Selectors/Multiplexers with 3-State Outputs	16 DIP
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	165	8-Bit Parallel-IN/Serial-Out Shift Registers	16 DIP
	166	8-Bit Parallel-IN/Serial-Out Shift Registers	16 DIP
	194	4-Bit Bidirectional Universal Shift Registers	16 DIP
	195	4-Bit Bidirectional Universal Shift Registers	16 DIP
	299	8-Bit Universal Shift/Storage Registers with 3-State Outputs	20 DIP

Functional Selection Gude (continued)

Function	Part Number KS54/74AHCT KS54/74HCTLS	Description	Package
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	596	8-Bit Shift Registers with Output Latches	16 DIP
	597	8-Bit Shift Registers with Input Latches	16 DIP
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	243	Quad Bus Transceivers with 3-State Outputs	14 DIP
	245	Ouad Bus Transceivers with 3-State Outputs	20 DIP
	640	Ouad Bus Transceivers with 3-State Outputs	20 DIP
	643	Ouad Bus Transceivers with 3-State Outputs	20 DIP
	645	Ouad Bus Transceivers with 3-State Outputs	20 DIP
	646	Octal 3-State Bus Transceivers with Registers	24 DIP
	648	Octal 3-State Bus Transceivers with Registers	24 DIP
	651	Octal 3-State Bus Transceivers with Registers	24 DIP
	652	Octal 3-State Bus Transceivers with Registers	24 DIP
	658	Octal Bus Transceivers with Parity	24 DIP
	659	Octal Bus Transceivers with Parity	24 DIP
	664	Octal Bus Transceivers with Parity	24 DIP
	665	Octal Bus Transceivers with Parity	24 DIP
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	161	Synchronous 4-Bit Binary Counters	16 DIP
	162	Synchronous 4-Bit Decade Counters	16 DIP
	163	Synchronous 4-Bit Binary Counters	16 DIP
	168	Synchronous 4-Bit Up/Down Decade Counters	16 DIP
	169	Synchronous 4-Bit Up/Down Binary Counters	16 DIP
	190	Presettable Synchronous BCD Decade Up/Down Counter	16 DIP
	191	Synchronous 4-Bit Up/Down Binary Counters	16 DIP
	192	Synchronous 4-Bit Up/Down Binary Counters	16 DIP
	193	Synchronous 4-Bit Up/Down Binary Counters with Dual Clock	16 DIP
	390	Dual 4-Bit Decade Counters	16 DIP
	393	Dual 4-Bit Binary Counters	16 DIP
	590	8-Bit Binary Counters with 3-State Output Register	16 DIP
	591	8-Bit Binary Counters with 3-State Output Register	16 DIP
	592	8-Bit Binary Counters with Input Register	16 DIP
	593	8-Bit Binary Counters with Bidirectional Input Register/Counter Output	20 DIP
Decocers Encoders	42	BCD-to-Decimal Decoder	16 DIP
	138	3-Line to 8-Line Decoders/Demultiplexers	16 DIP
	139	Dual 1-of-4 Decoders/Demultiplexers	16 DIP
	148	8-Line to 3-Line Priority Encoders	16 DIP
	154	4-Line to 16-Line Decoders/Demultiplexers	24 DIP
	155	Dual 2-to-4 Line Decoders/Demultiplexers	16 DIP
	238	3-Line to 8-Line Decoders/Demultiplexers	16 DIP
	239	Dual 1-of-4 Decoders/Demultiplexers	16 DIP
Multivibrators	121	Monostable Multivibrators with Schmit-Trigger Inputs	14 DIP
	123	Dual Retriggerable Monostable Multivibrators	16 DIP
	423	Dual Retriggerable Monostable Multivibrators	16 DIP
Arithmetic Circuits	181	4-Bit Arithmetic Logic Unit	24 DIP
	182	Look-Ahead Carry Generator	16 DIP
	183	Dual High Speed Adder	14 DIP
	280	9-Bit Parity Generators/Checkers	14 DIP

Functional Selection Guide (contnued)

Function	Pant Namber KS54/74AHCT KS54/74HCTLS	Description	Package
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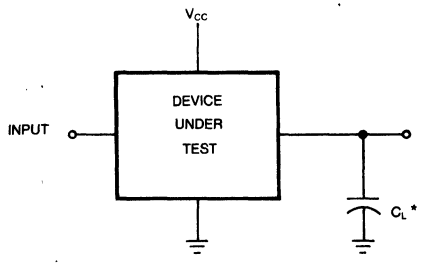
	519	8-Bit Identity Comparators	20 DIP
	520	8-Bit Identity Comparators	20 DIP
	521	8-Bit Identity Comparators	20 DIP
	522	8-Bit Identity Comparators	20 DIP
	679	12-Bit Address Comparators	20 DIP
	680	12-Bit Address Comparators	20 DIP
	682	8-Bit Magnitude Comparators	20 DIP
	684	8-Bit Magnitude Comparators	20 DIP
	686	8-Bit Magnitude Comparators	20 DIP
	688	8-Bit Magnitude Comparators	20 DIP
	689	8-Bit Identity Comparators with Open-Drain Outputs	20 DIP

PARAMETER MEASUREMENT INFORMATION

2

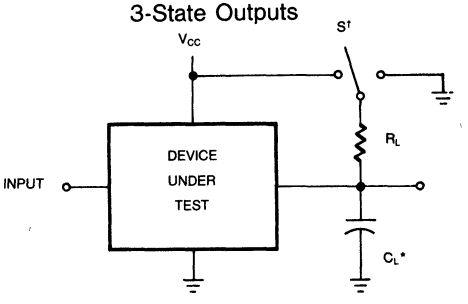
AC SWITCHING TEST CIRCUITS

Totem-Pole Outputs



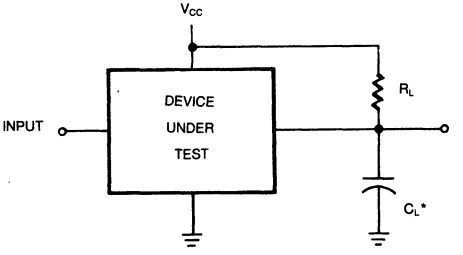
*C_L includes load and test jig capacitance

3-State Outputs



*C_L Includes load and test jig capacitance
S† = V_{CC} for t_{PZL} and t_{PLZ} measurements
S = GND for t_{PZH} and t_{PHZ} measurements.

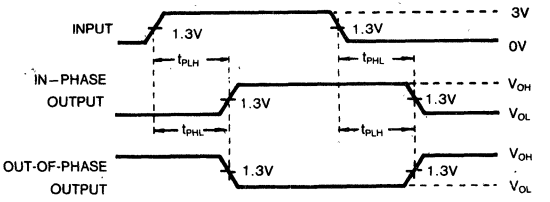
Open-Drain Outputs



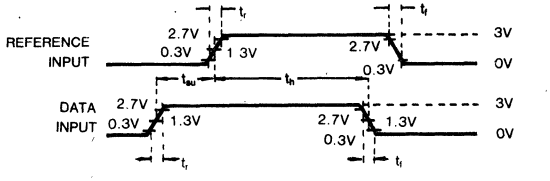
*C_L includes load and test jig capacitance

TIMING WAVEFORMS

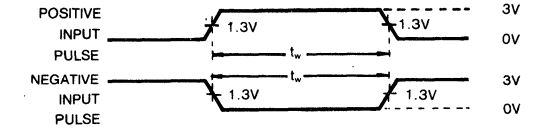
Propagation Delays



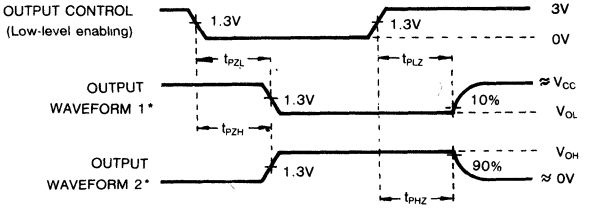
Setup & Hold Times, Input Rise & Fall Times



Input Pulse Width



Enable & Disable Time for 3-State Outputs



* Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. This waveform is applicable to both 3-state and open-drain outputs.

* Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

PARAMETER MEASUREMENT INFORMATION

DEFINITIONS OF TERMS & SYMBOLS

FUNCTION TABLE SYMBOLS

H = Steady state high level
L = Steady state low level
↑ = Transition from low to high level
↓ = Transition from high to low level
X = Don't care (high, low states or transitions)
Z = High-impedance state of a 3-state output
a..h = The level of steady-state inputs at inputs A thru H, respectively
Q_0 = Level of Q before the indicated steady-state input conditions were established
$\bar{Q}_0$ = Complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state conditions were established
Q_n = Level of Q before the most recent active transition indicated by ↑ or ↓
⎍ = One high-level pulse
⎏ = One low-level pulse
TOGGLE = each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as level (H, L, Q_0, or $\bar{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as pulse, ⎍ or ⎏, the pulse follows the indicated input transition and persists for an interval dependent on the circuit)

DC Characteristics Terms

V_{IH} High-Level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-Level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum is specified that is the most-postive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} High-Level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} Low-Level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} Positive-Going threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

PARAMETER MEASUREMENT INFORMATION

V_{T-} Negative-Going threshold level

The voltage at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

I_O Output Current

The current into* an output with input conditions applied that, according to the product specification, will establish a high or a low level at the output.

I_{IN} Input Curent·

The current into* an input when a high or a low level voltage is applied to that input.

I_{OZ} Off-State (high-impedance-state) output current (of a three-state output)

The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output level voltage applied to the output.

This parameter is measured with other input conditions established that would cause the output to be at a low-voltage level (if it were enabled) when the externally applied voltage is high; or high-voltage level when the externally applied voltage is low.

I_{CC} Supply current

The current into* the V_{CC} supply terminal of an integrated circuit.

*Current out of a terminal is given as negative value.

AC CHARACTERISTICS TERMS

t_r Rise time

The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the high level.

t_f Fall time

The time interval between two reference points (90% and 10% unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

f_{max} Maximum clock frequency

The highest rate at which the cock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of a logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

t_{PLH} Propagation delay time, low-to-high-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PHL} Propagation delay time, high-to-low-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PZH} Enable time (of a three-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state outputs changing from a high-impedance (off) state to the defined high level.

t_{PZL} Enable time (of a three-state output) to low level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state outputs changing from a high-impedance (off) state to the defined low level.

t_{PHZ} Disable time (of a three-state output) from high level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state outputs changing from the defined high level to high-impedance (off) state.

t_{PLZ} Disable time (of a three-state output) from low level

The time interval between the specified reference points on the input ano output voltage waveforms with the three-state outputs changing from the defined high level to high-impedance (off) state.

t_w Pulse width

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

t_{su} Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_h Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

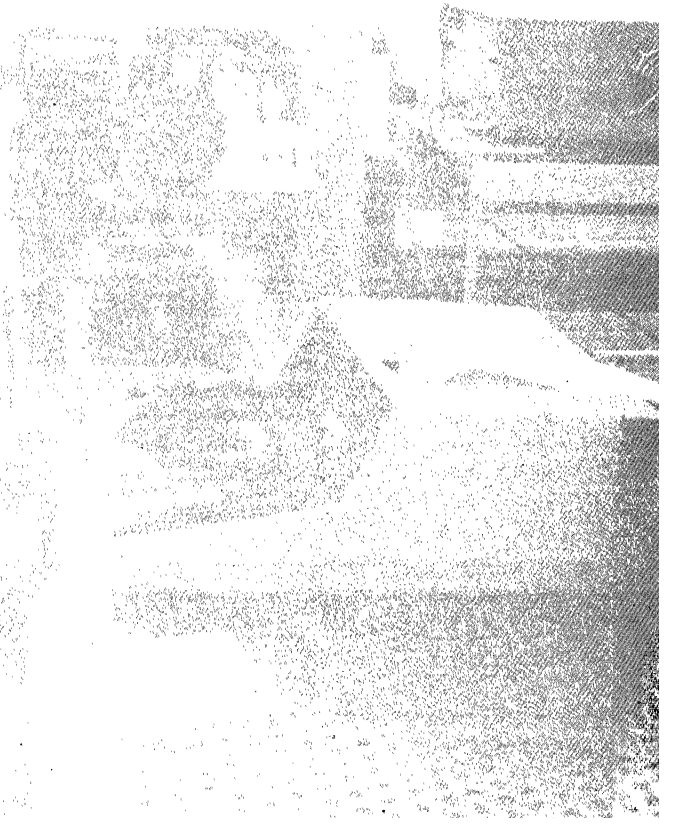
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

C_{PD} Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

NOTES

TECHNICAL OVERVIEW 3



INTRODUCTION

The 54/74AHCT Advanced High-Speed CMOS and the 54/74HCTLS High-Speed CMOS logic families were designed to offer the most desirable features of their CMOS and bipolar predecessors. They have the low power dissipation, superior noise immunity, wide voltage and temperature ranges and the very low input currents of the other high-speed CMOS logic families, in addition to the high speed and drive capability of LS and ALS bipolar logic.

The AHCT family is an exact equivalent of the bipolar ALS and can readily replace ALS in existing applications to reduce power dissipation. In many applications, AHCT parts can also be used as replacements for FAST™ and S (Schottky).

The HCTLS parts, on the other hand, meet and exceed all of industry-standard LS and HCT specifications, and can be used as replacements to these to lower the power dissipation and improve performance. Figure 1 shows how AHCT and HCTLS families rank with the other bipolar technologies in terms of speed and power dissipation.

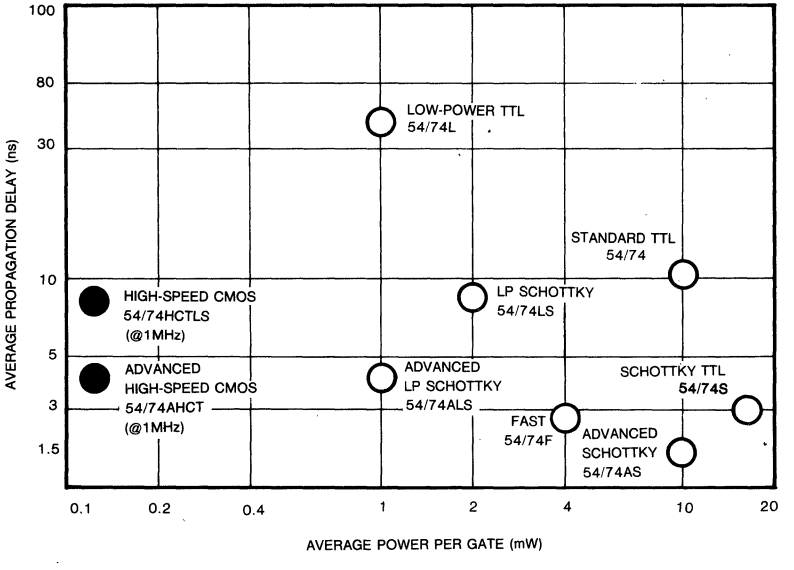


FIGURE 1. Power dissipation vs gate dely characteristics for a two-input NAND gate (74XXX00) implemented in various bipolar and CMOS technologies

Both families feature TTL input voltage levels which enable them to interface with all TTL, NMOS or CMOS outputs without any external components. All AHCT and HCTLS parts are fully characterized and specified over the 4.5 to 5.5V voltage range, and the industrial (−40 to 85°C) and military (−55 to 125°C) temperature ranges. This is a significant improvement over the older biploar logic families, where, for example LS would specify DC specs over 4.75V to 5.25V and AC specs only at 5V and room temperature. (ALS is specified over 4.5 to 5.5V and 0 to 70°C). A comparison of the key characteristics for an octal buffer illustrates these improvements clearly in Figure 2. The DC characteristics common to all AHCT and HCTLS parts are listed in Figure 3.

FAST is a trademark of Fairchild camera and Instrument

		TTL			SAMSUNG CMOS		OTHER CMOS	
		74LS244	74ALS244	74F244	74HCTLS244	74AHCT244	74HC244	74HCT244
Operating Voltage Range (Commercial)		4.75V to 5.25V	4.5V to 5.5V	4.75V to 5.25V	4.5V to 5.5V	4.5V to 5.5V	2V to 6V	4.5V to 5.5V
Operating Temperature Range (Commercial)		0°C to 70°C	0°C to 70°C	0°C to 70°C	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C
Maximum Propagation Delay (C_L = 50 pF)		18 ns (V_{CC} = 5V, T_a = 25°C)	10 ns (Over Operating Conditions)	6.5 ns (Over Operating Conditions)	18 ns (V_{CC} = 5V, T_a = 25°C)	10 ns (Over Operating Conditions)	20 ns (V_{CC} = 5V, T_a = 25°C)	18 ns (V_{CC} = 5V, T_a = 25°C)
Maximum Quiescent Current		54 mA	27 mA	90 mA	0.08 mA	0.08 mA	0.08 mA	0.08 mA
Typical Power Dissipation	Static	120 mW	70 mW	260 mW	0.004 mW	0.004 mW	0.004 mW	0.004 mW
	At 100 kHz (All inputs toggling)	120 mW	70 mW	260 mW	0.6 mW	0.6 mW	1.0 mW	1.8 mW
Output Drive Currents	I_{OH}	−3 mA (V_{OH} = 2.4V) −15 mA (V_{OH} = 2.0V)	−3 mA (V_{OH} = 2.4V) −15 mA (V_{OH} = 2.0V)	−15 mA (V_{OH} 2.0V)	−6 mA (V_{OH} = 3.84V)	−6 mA (V_{OH} = 3.84V)	−6 mA (V_{OH} = 3.84V)	−6 mA (V_{OH} = 3.84V)
	I_{OL}	12 mA (V_{OL} = 0.4V) 24 mA (V_{OL} = 0.5V)	12 mA (V_{OL} = 0.4V) 24 mA (V_{OL} = 0.5V)	64 mA (V_{OL} = 0.55V)	12 mA (V_{OL} = 0.4V) 24 mA (V_{OL} = 0.5V)	12 mA (V_{OL} = 0.4V) 24 mA (V_{OL} = 0.5V)	6 mA (V_{OL} = 0.33V)	6 mA (V_{OL} = 0.33V)
Input Threshold Voltages	V_{IL}	0.8V	0.8V	0.8V	0.8V	0.8V	0.9V (V_{CC} = 4.5V)	0.8V
	V_{IH}	2.0V	2.0V	2.0V	2.0V	2.0V	3.15V (V_{CC} = 4.5V)	2.0V
Input Currents	I_{IL}	−0.2 mA (V_I = 0.4V)	−0.1 mA (V_I = 0.4V)	−1.6 mA (V_I = 0.5V)	−1.0 μA	−1.0 μA	−1.0 μA	−1.0 μA
	I_{IH}	20 μA (V_I = 2.7V)	20 μA (V_I = 2.7V)	20 μA (V_I = 2.7V)	1.0 μA	1.0 μA	1.0 μA	1.0 μA

FIGURE 2. Key performance characteristics for 74XXXX244 octal buffer

The Samsung CMOS logic families include a comprehensive set of buffers, registers, latches and transceivers that are offered in 8, 9 and 10-bit versions. A wide variety of gates, flip-flops, multiplexers, shift registers, encoder/decoders, schmitt triggers and multivibrators complete the family of 157 part types. Each function is available in both AHCT and HCTLS version.

Characteristic	Symbol	Conditions		$T_a = 25°C$	Commercial $T_a = -40°C$ to $+85°C$	Military $T_a = -55°C$ to $+125°C$	Unit
				Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}				2.0	2.0	2.0	V
Minimum Low-Level Input Voltage	V_{IL}				0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	CMOS loads $I_{OH}=-20\mu A$	V_{CC}	$V_{CC}-0.1$	$V_{CC}-0.1$	$V_{CC}-0.1$	V
			Standard Outputs $I_{OH}=-4$ mA	4.2	3.98	3.84	3.7	
			Bus-Driver Outputs $I_{OH}=-6$ mA	4.2	3.98	3.84	3.7	
Minimum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	CMOS loads $I_{OL}=20\ \mu A$	0.1	0.1	0.1	0.1	V
			Standard Outputs $I_{OL}=4$ mA $I_{OL}=8$ mA	0.2 0.3	0.26 0.39	0.33 0.5	0.4	
			Bus-Driver Outputs $I_{OL}=12$ mA $I_{OL}=24$ mA	0.2 0.3	0.26 0.39	0.33 0.5	0.4	V
Maximum Input Leakage Current	I_I	V_{CC}=Max, $V_{IN}=V_{CC}$ or GND			±0.1	±1.0	1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	V_{CC}=Max, Enable=V_{IH} or V_{IL} $V_{OUT}=V_{CC}$ or GND			±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{CC}=Max $V_{IN}=V_{CC}$ or GND All Outputs Open	SSI Circuits		2.0	20.0	40.0	μA
			Dual and Quad Flip-Flops & Latches		4.0	40.0	80.0	
			MSI Circuits & Circuits with High-Current Outputs		8.0	80.0	160.0	

FIGURE 3. DC characteristics of the 54/74AHCT and 54/74 HCTLS Families ($V_{CC}=5.0V\ \pm10\%$)

PROCESS TECHNOLOGY

The high performance of the AHCT and HCTLS is a result of a unique self-aligned metal-gate CMOS process technology that features 1.2μm effective gate lengths and double metallization. The following table compares the general characteristics of this process with other existing CMOS and bipolar technologies used for logic circuits:

	SAMSUNG CMOS	INDUSTRY CMOS (HC & HCT)	INDUSTRY ALS
Number of Masking Steps	8	12-14	13
Number of Metal Layers	2	1	2
Minimum Feature Size (drawn)	2 μm	3-4 μm	4 μm
Interconnections	All Metal	Poly & Metal	All Metal
Relative Die Size	1X	2.5-5X	1.5-2X
Manufacturing Equipment	Standard	Standard	Standard

Samsung's CMOS process was designed from the ground up to be a scaled two-layer metal CMOS process (see *Figure 4* for a cross section). The goal was to make the process as simple as possible, and be able to readily control gate length and gate dielectric thickness. The process uses 8 masking steps. Other semiconductor manufactures, in trying to go to two-layer metal short-channel processes have generally embellished pre-existing silicon-gate processes and have wound up with 12-14 masking steps. More masking steps, of course, make wafers more costly, but most importantly, reduce yield because of more chances for random defects.

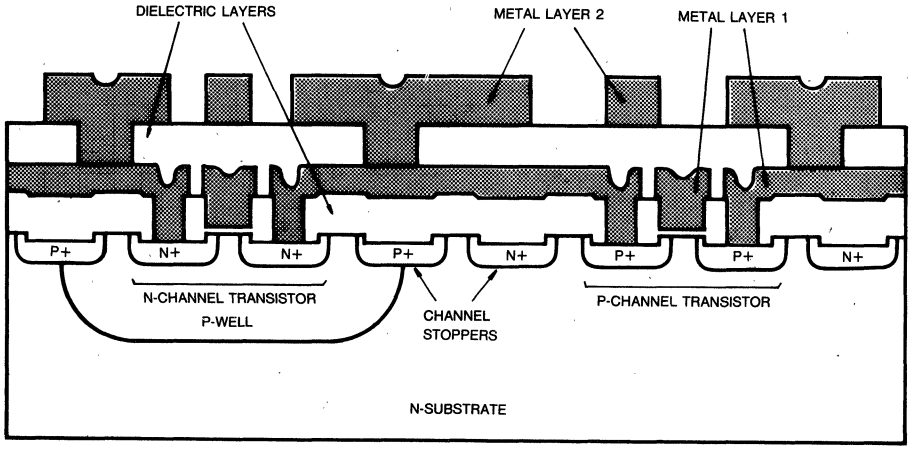


FIGURE 4. Samsung CMOS process cross section for an inverter stage

The Samsung process, with the short 2 μm channel lengths (1.2 μm effective), yields gate delays as fast as those of the bipolar LS and ALS processes, and the same short channel lengths allow high-current output drivers to occupy a modest silicon area. Generally, the AHCT and HCTLS logic chips are much smaller than their CMOS and bipolar equivalents (see *Figure 5*). In achieving this small size, two-layer metal is as important as having short channels. For example, in the on-chip busing of ground and V_{CC} to the output drivers, very wide metal lines have to be used that take considerable area. In this case, if these lines are in Metal 2, no extra area is wasted since the circuitry can be placed underneath.

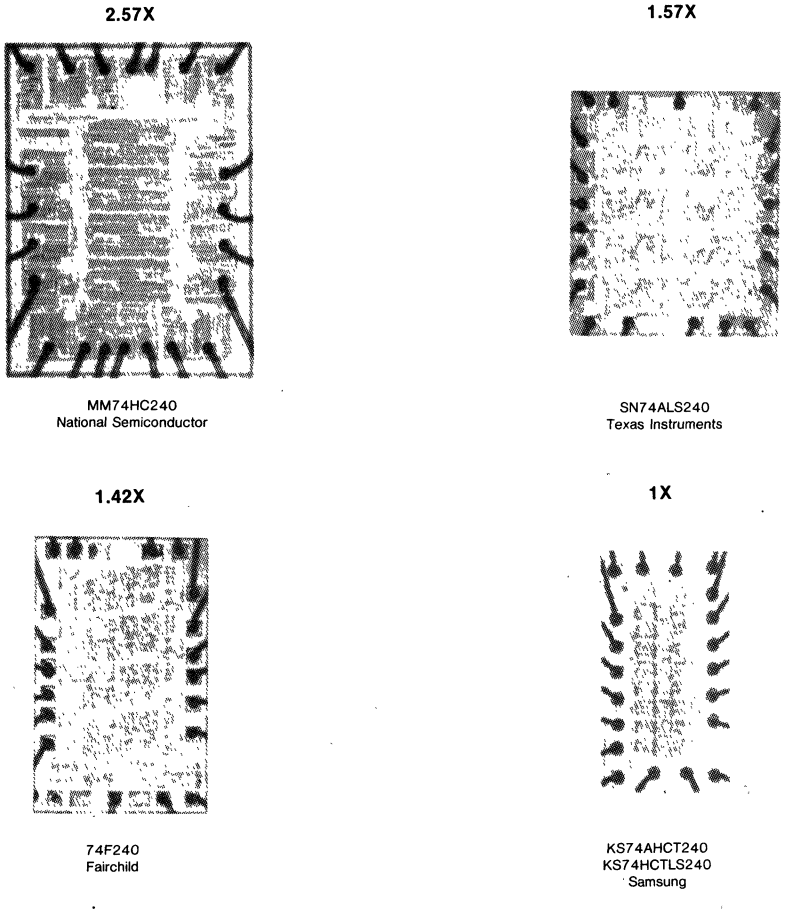


FIGURE 5. Die size comparison for a 74XXX244 from various technologies.

INPUT CHARACTERISITICS

The input stage of an AHCT or HCTLS circuit is illustrated in *Figure 6*. It consists of a diode protection network and a CMOS inverter stage that has very high input impedance. The ultra-low input current specified in the data sheets (1 μA maximum) is due to the reverse leakage currents of the diodes and is not used for "driving" the CMOS transistors i.e. the inputs are voltage-driven. This makes AHCT and HCTLS inputs very easy to drive and results in a very high fan-in capability.

TTL-compatible input threshold voltages of 0.8V V_{IL} and 2.0V V_{IH} are accomplished by properly sizing the p- and n-channel transistors of the CMOS inverter stage. The actual logic transition takes place mid-way between these values, at 1.4V, and is very sharp compared to TTL logic due to the very high gain of the first inverter stage. This is illustrated in *Figure 7* for a two-input NAND gate. Note that the input threshold for CMOS is much more stable with temperature than that for LS.

While the AHCT and HCTLS parts are recommended as direct replacements for ALS and LS, one needs to pay attention to not leaving any inputs floating, i.e. unconnected. Since the inputs have very high impedance, they can easily pick up external noise which can result in random switching of the device and high power consumption. Therefore, all unused inputs must be terminated to either V_{CC} or ground.

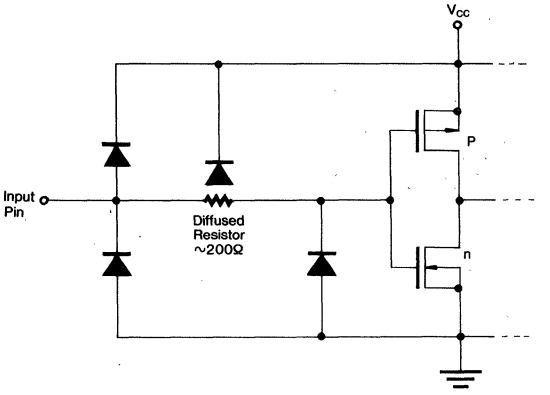


FIGURE 6. The input circuit of AHCT and HCTLS parts.

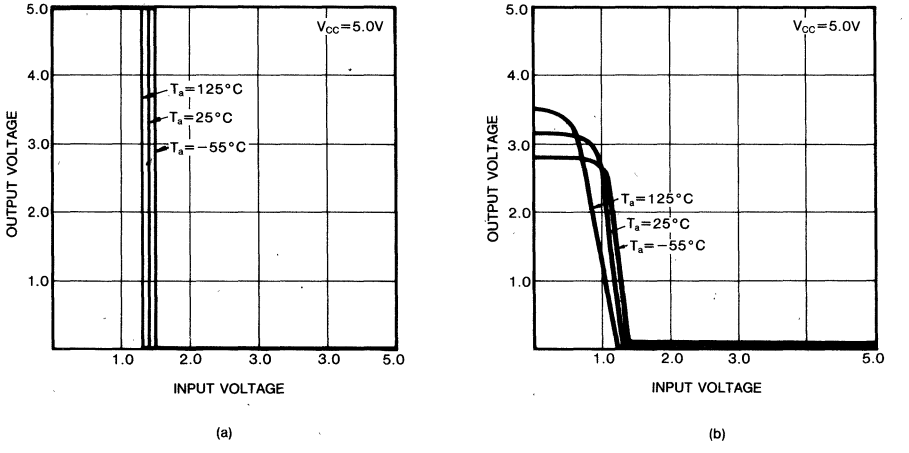


FIGURE 7. Input-Output transfer characteristics for (a) AHCT/HCTLS00, (b) LS00.

OUTPUT CHARACTERISTICS

A typical output stage of an AHCT or HCTLS part consists of a complementary pair of transistors and a diode protection network (see *Figure 8*). Unlike the bipolar outputs, the voltage swing is rail-to-rail, which is responsible for the improved noise margine of AHCT/HCTLS systems. The drive capability of these outputs is similar to the bipolar parts, i.e. 24mA or 8mA I_{OL} (at 0.5V V_{OL}) for bus-driver and standard outputs, respectively. This means that AHCT and HCTLS parts can drive as many loads or as large bus capacitances as their ALS and LS counterparts. *Figure 9* shows a comparison of the output drive capabilities of AHCT/HCTLS and LS/ALS outputs. *Figure 10* illustrates the variations of I_{OL} and I_{OH} with supply voltage and temperature for a standard output ('00) and a bus driver ('244).

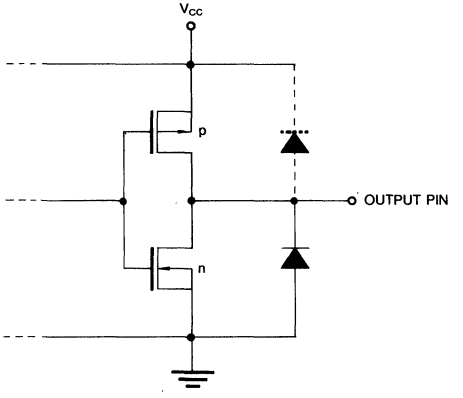


FIGURE 8. A typical output circuit of an AHCT or HCTLS part. The upper diode is parasitic and embedded in the p-channel transistor.

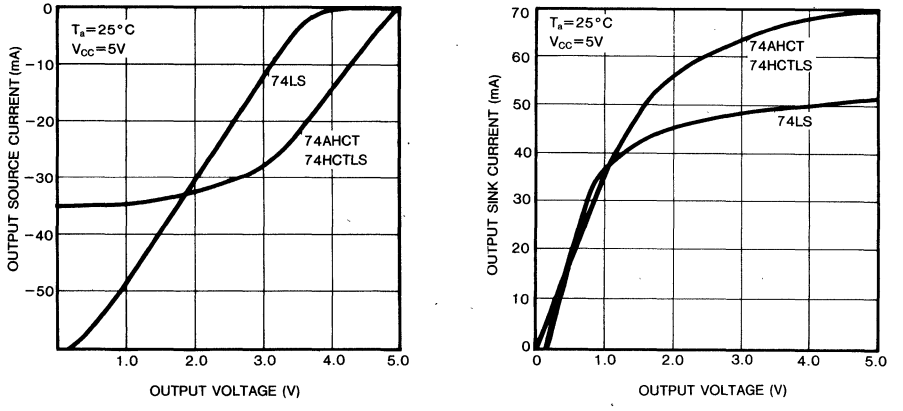
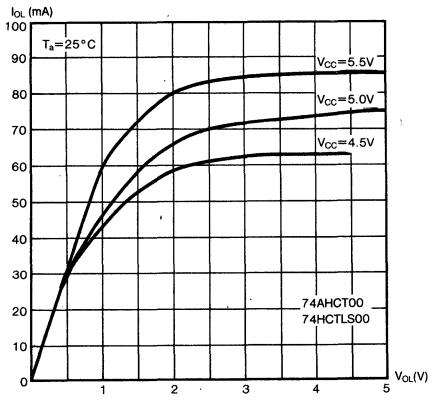
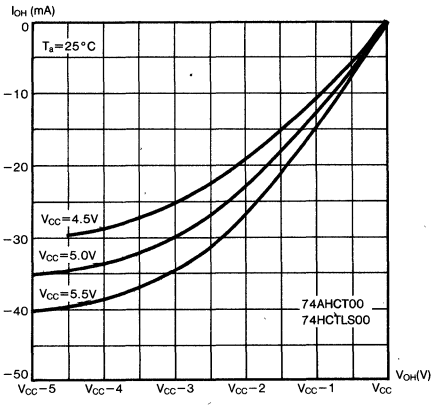


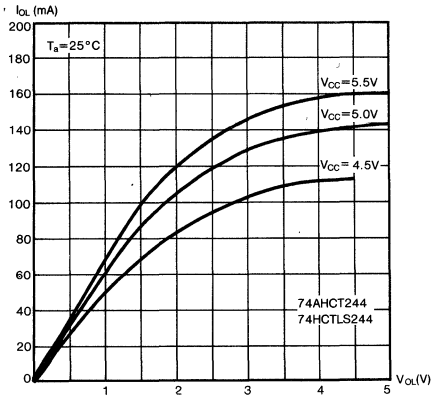
FIGURE 9. Comparison of standard AHCT/HCTLS and standard LS output (a) Source, and (b) sink currents.


I_{OL} (mA)
T_a=25°C
V_{CC}=5.5V
V_{CC}=5.0V
V_{CC}=4.5V
74AHCT00
74HCTLS00
V_{OL}(V)

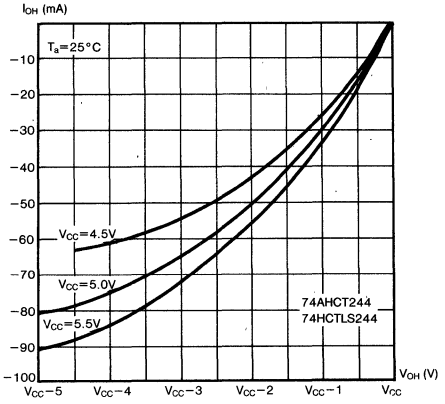
(a)


I_{OH} (mA)
T_a=25°C
V_{CC}=4.5V
V_{CC}=5.0V
V_{CC}=5.5V
74AHCT00
74HCTLS00
$V_{CC}-5$ $V_{CC}-4$ $V_{CC}-3$ $V_{CC}-2$ $V_{CC}-1$ V_{CC}
V_{OH}(V)

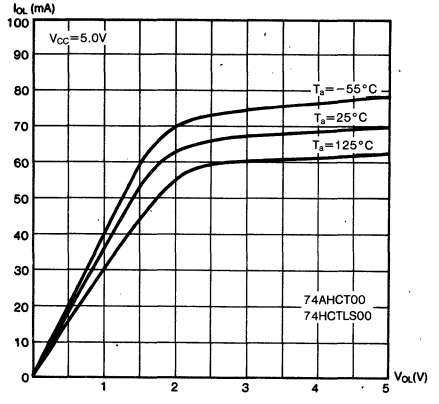
(b)


I_{OL} (mA)
T_a=25°C
V_{CC}=5.5V
V_{CC}=5.0V
V_{CC}= 4.5V
74AHCT244
74HCTLS244
V_{OL}(V)

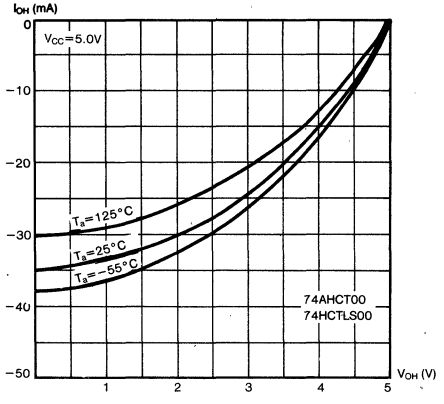
(c)


I_{OH} (mA)
T_a=25°C
V_{CC}=4.5V
V_{CC}=5.0V
V_{CC}=5.5V
74AHCT244
74HCTLS244
$V_{CC}-5$ $V_{CC}-4$ $V_{CC}-3$ $V_{CC}-2$ $V_{CC}-1$ V_{CC}
V_{OH} (V)

(d)


I_{OL} (mA)
V_{CC}=5.0V
T_a=−55°C
T_a=25°C
T_a=125°C
74AHCT00
74HCTLS00
V_{OL}(V)

(e)


I_{OH} (mA)
V_{CC}=5.0V
T_a=125°C
T_a=25°C
T_a=−55°C
74AHCT00
74HCTLS00
V_{OH} (V)

(f)

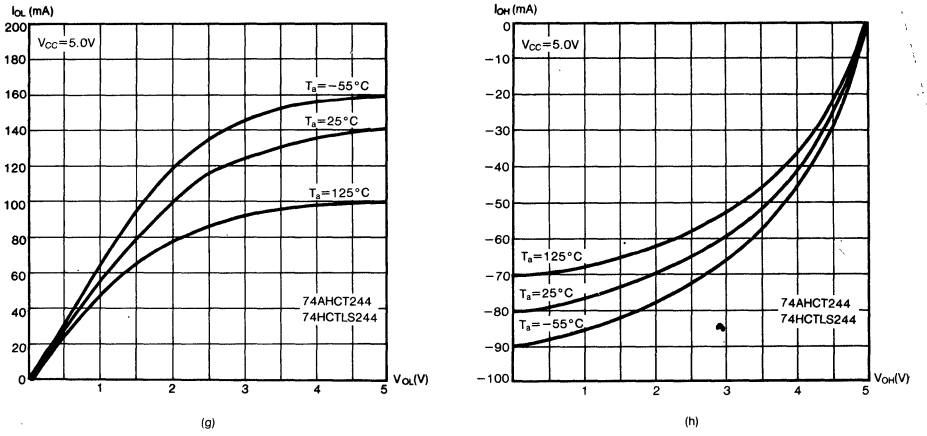


FIGURE 10. Output current variations with supply voltage and temperature for standard [(a), (b), (e) (f)] and bus driver [(c), (d), (g), (h)] outputs.

3

NOISE IMMUNITY & NOISE MARGINS

The term "noise" in the context of digital circuits and systems means unwanted transient variations of voltages and currents at logic nodes. Typically noise is transferred to logic nodes or interconnecting lines by unwanted capacitive or inductive coupling, as illustrated in *Figure 11*.

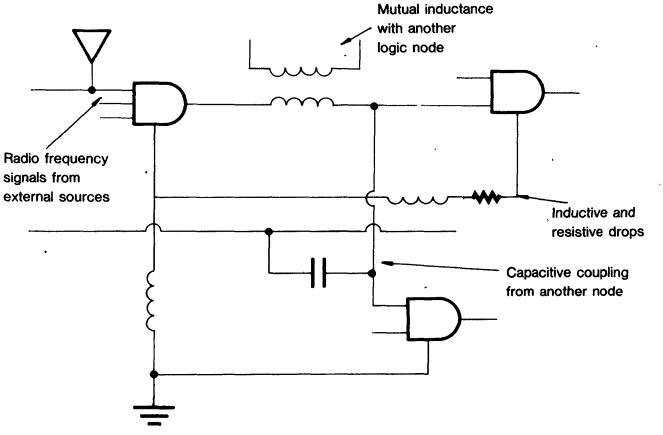
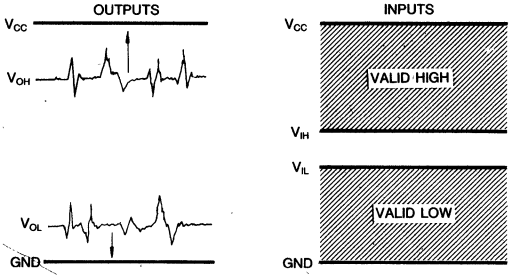


FIGURE 11. Sources of noise in digital systems.

Noise becomes a particularly critical issue in high-speed systems where fast voltage transitions accentuate these parasitic capacitances and inductances. Also, higher speeds allow the device to respond more quickly to noise transients. Therefore, special board layout and decoupling techniques have to be employed to confine noise to an "acceptable range". Obviously, the wider this range, the easier it is to design a clean system. This range is dictated by the input and output characteristics of the ICs in the system, as illustrated in Figure 12, and is measured in terms of "noise margins".

The output signals should be as close to the supply rails as possible. This allows more margin for noise to distort the output signal without violating the logic level requirements of the driven inputs.



The voltage range for each logic level should be as wide as possible. This relaxes the requirements for the cleanliness of incoming signals.

FIGURE 12. Requirements for good noise immunity.

Noise margins specify the maximum amplitude noise pulse that will not change the state of a driven stage, assuming the driving stage presents a worst-case logic level to the driven stage. Specifically, the high-level and the low-level noise margins (NM_H and NM_L) are defined as:

$NM_H = V_{OH} - V_{IH}$,
$NM_L = V_{IL} - V_{OL}$,

where the voltage values are the guaranteed worst-case extremes for each case. *Figure 13* shows the noise margins for several different interfaces.

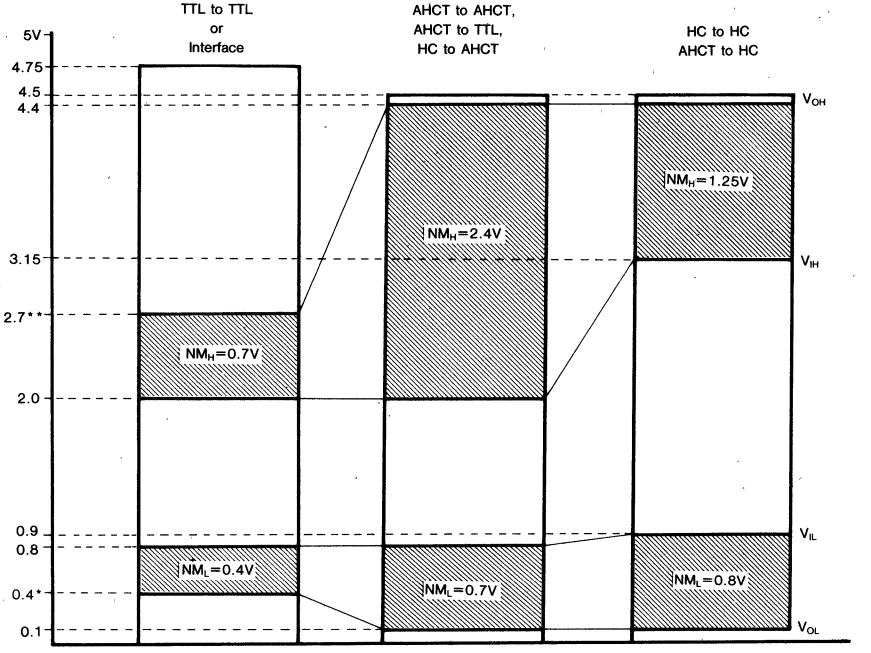


FIGURE 13. Noise margins for various interfaces. Noise margins for HCTLS are the same as those for AHCT.

* When an AHCT output drives TTL loads the V_{OH} level will be dependent on how many loads are driven. For example if an AHCT244 drives 60LS loads, the V_{OH} will rise to 0.4V

** For some, TTL parts, V_{OH} is 2.4V, instead of 2.7V

It is immediately obvious that the TTL-to-TTL interfaces have the poorest noise immunity and those driven by CMOS have the best. This is due to the rail-to-rail voltage swings of CMOS outputs.

Note the HC logic has almost symmetrical noise margins while AHCT (or HCTLS) has a very large noise margin for high level and a smaller low-level one. This is due to the fact that AHCT (or HCTLS) inputs are designed for direct interface with TTL and NMOS outputs as well as other CMOS. Notice, however, that the low-level noise margin (NM_L) for AHCT is only 0.1V less than that for HC, which means that it provides nearly as much immunity to ground noise. In addition, since AHCT drive capability is two to four times better than HC, it is less susceptible to noise currents coupled to its outputs. That is, lower stray voltages are induced for a given amount of current coupling than for HC.

ESD PROTECTION

Historically, MOS devices have always been considered to be more susceptible to damages due to electrostatic discharges (ESD), which can occur during handling and assembly procedures. However, the new protection circuitry, design, and special processing used for AHCT and HCTLS have improved the ESD immunity for these devices where it is now much better than that of bipolar logic.

Figure 6 and *8* show the input and output ESD protection circuitry employed. All AHCT and HCTLS pins are protected to ESD levels typically greater than±2kV, the tests are conducted using the "human-body" model that is shown in *Figure 14*.

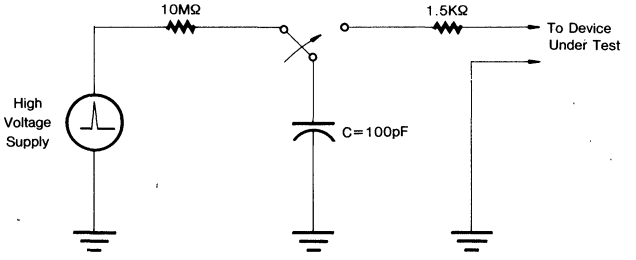


FIGURE 14. Test circuit used to measure ESD damage in AHCT and HCTLS circuits.

LATCHUP CHARACTERISTICS

SCR iatchup is an undesirable parasitic phenomenon which is inherent in circuits fabricated using bulk CMOS technology. A parasitic four-layer (P-N-P-N) SCR structure that appears between V_{CC} and ground can be triggered when voltages greater than V_{CC} or less than ground are applied to inputs or outputs. When this happens, V_{CC} gets effectively shorted to ground, and the only way to get the device off the latchup mode is to shut off the power supply. If large currents are allowed to flow through the chip, it may be destroyed. Samsung CMOS logic parts have been designed and processed to virtually eliminate this possibility in real-life situations where voltages out of the supply range many appear at the input or output pins (overshoots, undershoots, power-up & power-down situations).

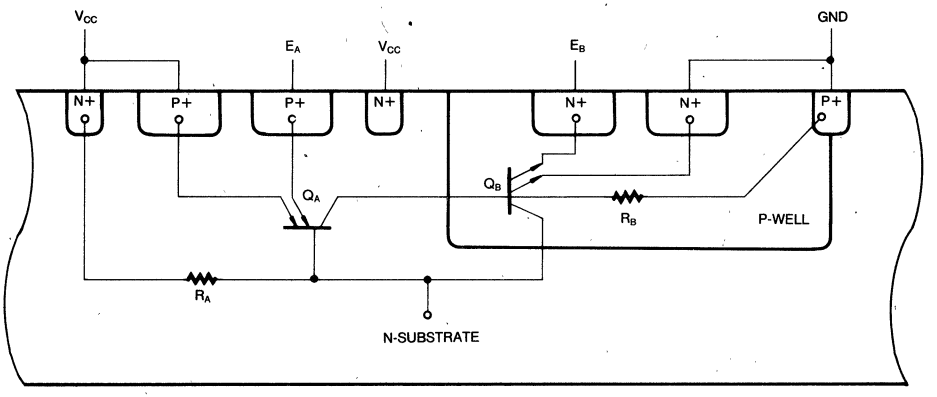


FIGURE 15. Simplified cross section of a CMOS inverter

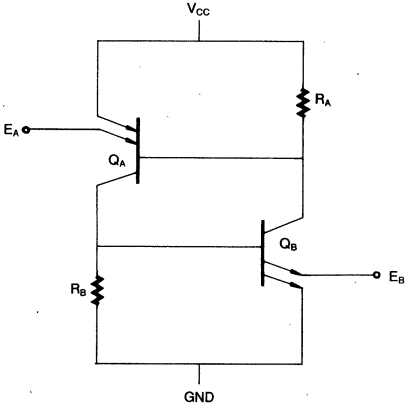


FIGURE 16. CMOS SCR structure

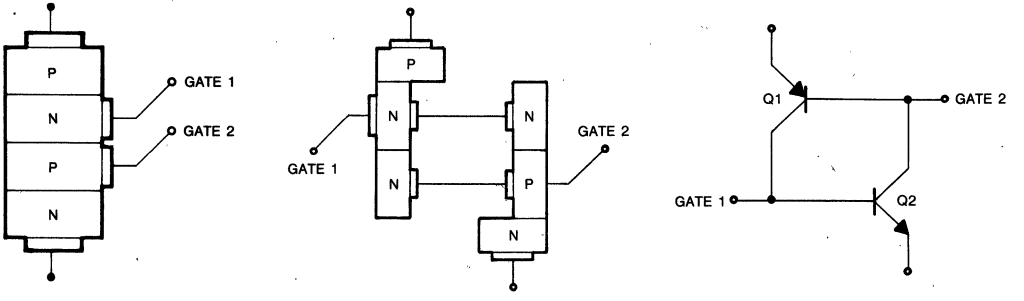


FIGURE 17. Simplified four layer SCR structure

The parasitic SCR structure in a CMOS inverter cross section is illustrated in *Figure 15,* where vertical and lateral NPN and PNP transistors are formed back-to-back by the N and P diffusions. R_A and R_B are the P-well and the N-substrate power supply connections. *Figure 16* is a schematic representation of this parasitic structure that looks like a cross-coupled transistor model of an SCR *(Figure 17).* The exceptions are the R_A and R_B resistors and the fact that the real SCR is triggered at the gates, while the CMOS parasitic SCR is triggered at its emitters. This happens when either the E_A is raised above V_{CC} enough to turn on Q_A, or E_B is lowered below ground enough to turn on Q_B. When E_A is brought above V_{CC}, current is injected from the emitter of Q_A and is swept to its collector. This current, in turn, will increase the voltage at the Q_B gate and once it is above 0.7V, Q_B will turn on and feed current from its collector back into R_A and into Q_A. When 0.7V drop appears across R_A, Q_A will turn on even more.

If the two transistors have enough gain and enough current is provided by the supply to sustain the SCR, it will turn on and remain on even after E_A and E_B are returned to the rail voltages. Notice that low resistor values effectively reduce the gain of the transistors by stealing current away from their bases. Therefore, transistors should actually have much higher gains in order to have an overall SCR loop gain greater than one and enable SCR to trigger.

Samsung CMOS logic parts are designed and processed to have very low R_A, R_B values and low gains for the parasitic transistors. In addition, large diodes exist between each signal pin and the supply rails to shunt out voltages above V_{CC} and below ground. In fact, traditionally, one refers to the current that flows through these diodes as the element that triggers latchup, i.e. we talk of "latchup trigger currents", not voltages.

Measured on a static basis, i.e. by applying DC voltages above V_{CC} and below ground, Samsung parts can withstand currents typically well above 200mA-even under the worst-case conditions of 7V V_{CC} and +125°C operation. *Figure 18* illustrates the test set-up used for static latchup tests.

A common occurence of voltages above V_{CC} and below ground in systems is overshoots and undershoots that are caused by signal line ringing and power supply transients. In this case, unlike the static operation, only short pulses cause forward-bias diode currents and hence possible latch-up. It turns out, fortunately, that the parasitic SCR has extremely slow response time to transients, i.e. very poor frequency characteristics. *Figure 19* shows the increased peak currents required to latch an AHCT or HCTLS device up when the pulse width is decreased. For pulse widths in the range of several tens of nanoseconds, it is virtually impossible to latch the device up.

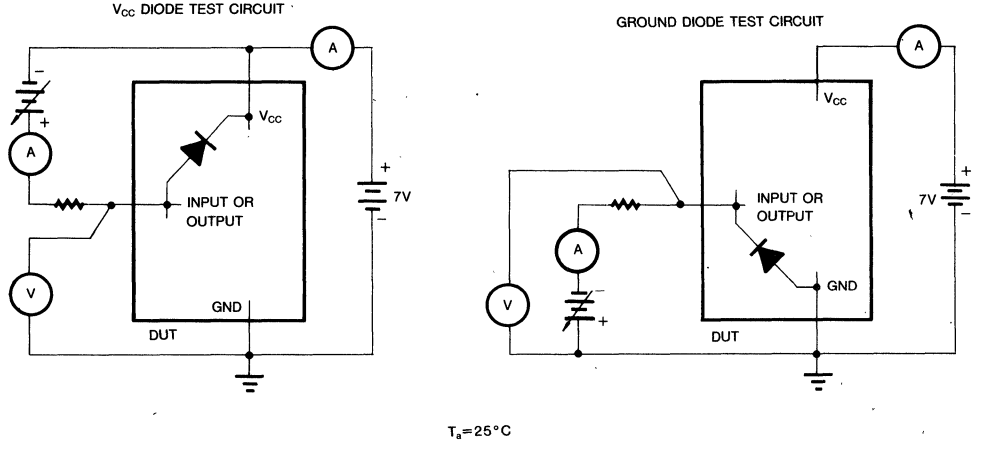


FIGURE 18. Test setup for measuring DC latch-up

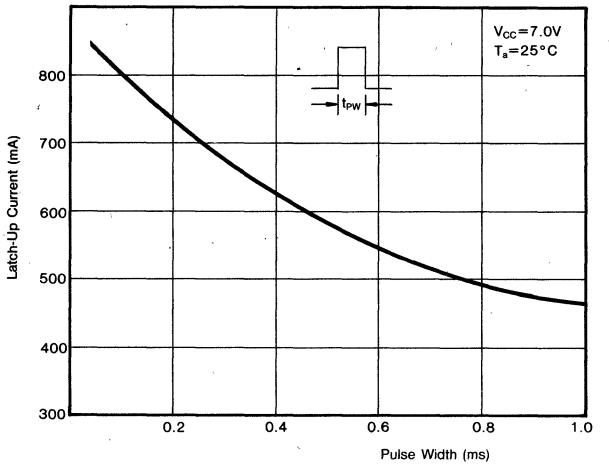


FIGURE 19. Pulsed latch-up characteristics

POWER DISSIPATION

Low power dissipation is by far the most important advantage of CMOS over any other technology. Particularly in the quiescent state, the AHCT and HCTLS circuits consume up to seven orders of magnitude less power than the equivalent TTL functions. This makes them ideal for battery-operated or ultra-low power systems where the system may be put to "sleep" by shutting off the system clock.

The dynamic power dissipation, however, depends on:

1. Cross-over currents of the internal CMOS transistors,
2. Internal load capacitances,
3. External load capacitances, and
4. Input voltage levels.

All of the above add up every time there is a logic transition and dynamic power dissipation is the sum of these contributions averaged at a given operating frequency. A practical formula is developed to calculate the dynamic power dissipation (P_D) resulting from the first three items: (input voltage transitions are rail-to-rail)

$$P_D=(C_L+C_{PD})\ V_{CC}^2 f,$$

where C_L is the load capacitance; C_{PD} is the "internal power dissipation capacitance", V_{CC} is the supply voltage and f is the operating frequency. The C_{PD} value, as specified in each data sheet, sums up the contributions of the first two factors (crossover currents and internal load capacitances) as a capacitance value for purposes of this calculation. The equation indicates that the dynamic power dissipation is directly proportional to frequency.

The contribution of the fourth factor listed above, the input voltage levels, can also be significant when AHCT or HCTLS inputs are driven by TTL outputs. *Figure 20* shows the typical crossover currents generated at the input inverer stage as the input voltage swings from O to V_{CC}. This is because both the n-channel and the p-channel transistors turn on partially and provide a low-resistance current path between V_{CC} and ground when the input voltage is near the threshold voltage of the complementary pair. At 2.7V, which is the worst case V_{OH} for TTL parts, the I_{CC} can be as high as 0.5mA per input. This has to be taken into account when calculating the worst-case power dissipation of an AHCT or HCTLS part operating in a TTL environment.

Figure 21 shows the internal power dissipation for an AHCT244 (same for HCTLS244) and compares it with the dynamic power dissipation for LS, ALS and F244. It can be seen that the curves for the bipolar parts are essentially flat for frequencies up to 1 MHz where the quiescent currents mask out the dynamic effects. However, as the frequency goes up, the currents that charge the internal capacitances start adding to the quiescent currents and increase the overall power dissipation. The AHCT244 driven by worst-case TTL voltage levels (all inputs, 50% duty cycle) displays a similar trend but still dissipates an order of magnitude less power than the lowest-power TTL. When CMOS input voltage levels are used, however, the power dissipation is directly proportional to frequency as predicted by the above mentioned formula, and is less than those for the TTL parts, Although the power dissipation becomes comparable to ALS levels at around 10MHz, a crossover does not happen below 50MHz, which is already beyond the maximum clock frequencies of most systems. This behaviour is pretty much the same for all parts in the AHCT and HCTLS families.

In calculating the power dissipation of a system, however, note that only a small percentage of the devices operate at the maximum clock frequency while others operate at a fraction of that. Therefore the average operating frequency tends to be much lower where CMOS has a clear advantage.

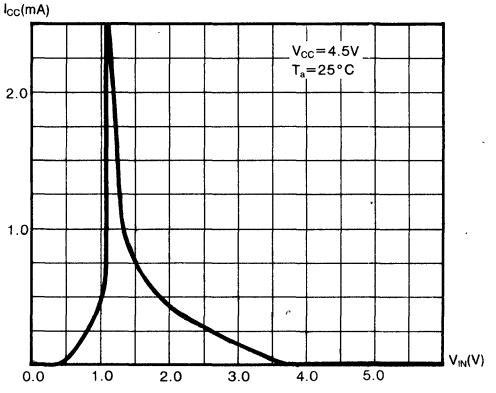


FIGURE 20. Typical crossover current of an AHCT or HCTLS input.

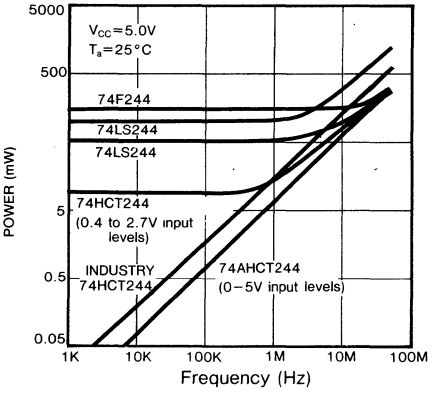


FIGURE 21. Typical dynamic power consumption (no-load) of the 74XXX240 octal buffer with all inputs toggling.

AC CHARACTERISTICS

All AHCT and HCTLS parts are designed to meet or exceed the ALS and LS propagation delay specifications, respectively. Coupled with the equivalent drive capability, this makes them ideal replacements for the ALS and LS in existing designs.

In addition the AC specifications for AHCT and HCTLS parts are improved to reflect more realistic design situations. First of all, unlike LS, the AHCT & HCTLS propagation delays are specified with a 50pF load for all part types and guaranteed over the entire voltage and temperature ranges (5V±10%, −40°C to +85°C). Standard LS propagation delays are specified with a 15pF load and guaranteed only at room temperature and 5V V_{CC}. In addition, all bus drivers specify the propagation delays with a 150pF load capacitance to enable the designer to predict a worst-case maximum speed degradation due to capacitive loading.

The effect of the supply voltage variations on propagation delay is illustrated in *Figure 22* for a bus-driver (AHCT244). It can be seen that the parts are functional over a very wide range of voltages and that they slow down as V_{CC} goes down. However, propagation delays are specified and guaranteed only over the 4.5 to 5.5V range.

Figure 23 shows the effect of temperature on the propagation delays for the same part. As for all CMOS circuits, AHCT and HCTLS parts slow down as temperature goes up. Typically speeds derate linearly from 25°C at about 0.02 ns/°C. The propagation delay at any temperature (between −55°C and +125°C) can therefore be calculated using the following formula:

$$t_{PD}(T) = t_{PD}(25°C) + k_T(T - 25°C)$$

where:

$t_{PD}(T)$=Propagation delay at the desired T temperature,
$t_{PD}(25°C)$=Propagation delay at 25°C,
k_T=Temperature derating factor=0.02 ns/°C

The effect of capacitive loading of the outputs on the propagation delay is illustrated in *Figure 24*: the higher the load capacitance, the slower the propagation delay gets. To determine the maximum limit for propagation delay at any value of capacitive loading up to 500pF, the following equation is used:

$$t_{PD}(C_L) = t_{PD}(50pF) + k_C(C_L - 50pF)$$

where:

$t_{PD}(C_L)$=Maximum propagation delay at the desired C_L,
$t_{PD}(50pF)$=Maximum propagation delay from device data sheet,
k_C=Maximum multiplicative factor (ns/pF):

- 0.04 for standard outputs, and
- 0.02 for bus-drivers.

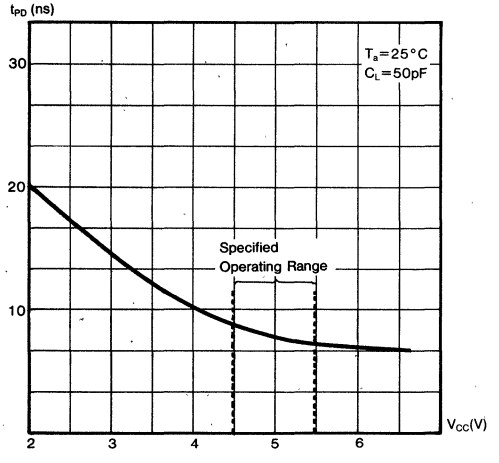


FIGURE 22. Propagation delay versus supply voltage for an AHCT244.

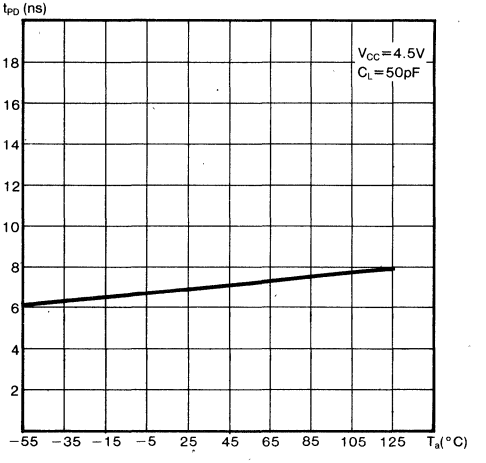


FIGURE 23. Propagation delay versus ambient temperature for an AHCT244.

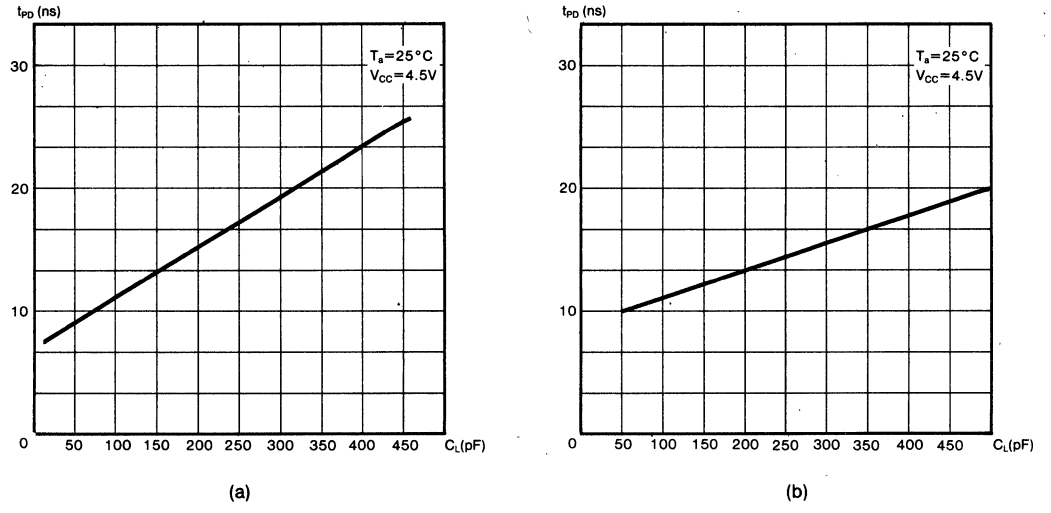


FIGURE 24. Propagation delay versus capacitive load for a (a) standard output (HCTLS00), (b) bus-driver output (HCTLS374)

INTERFACING 54/74AHCT AND 54/74HCTLS WITH OTHER LOGIC FAMILIES AND LOADS

Speed and power, while paramount in the initial choice of a logic family, are not the only basis of decision. Another very important factor is the interface flexibility: the inherent capacity of a family to interface with other types of logic and to drive various loads. The Samsung CMOS logic families have this very attractive feature that they can easily be interfaced to all other kinds of digital logic with minimal or no external components.

AHCT and HCTLS parts can be coupled directly with all other TTL, NMOS and CMOS parts if they operate from the same supply voltage. The list includes Standard TTL, Schottky(S), Low-Power Schottky(LS), Advanced Low-Power Schottky(ALS), Advanced Schottky (AS and FAST); all industry-standard CMOS logic families (HC, HCT, CD4000, 14000); all bipolar, NMOS and CMOS microprocessors, microcontrollers, peripherals and memory circuits (see figure 25). This is due to the TTL-compatible input voltage levels coupled with CMOS (rail-to-rail) output voltage swings.

Interface with ECL logic, however, requires external components as shown in *Figure 26*.

Methods of interfacing with standard CMOS logic families (4000 and 14000), when supply voltages are different, are illustrated in *Figure 27* and *28*.

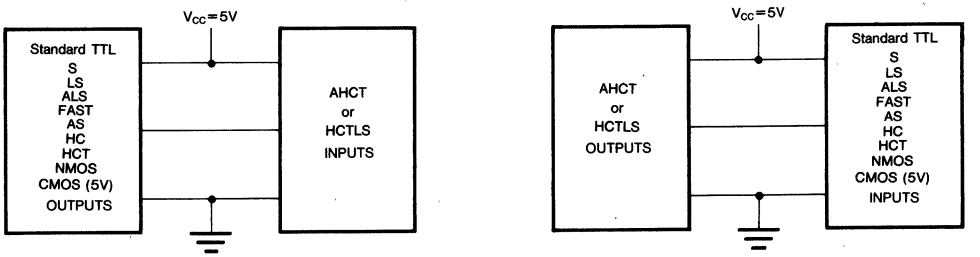
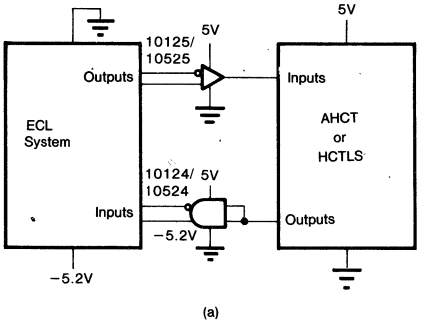


FIGURE 25. Interfacing with TTL, NMOS and other CMOS logic. No extra components are needed.



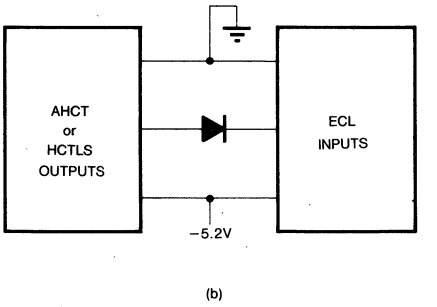


FIGURE 26. (a) General ECL interface

(b) Driving ECL from same power supply.

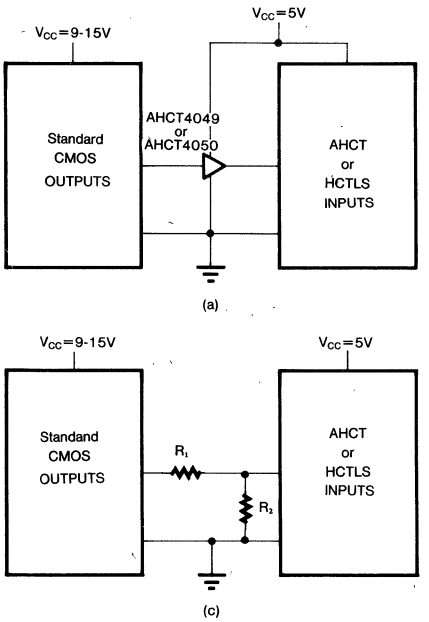


FIGURE 27. Methods of interfacing standard CMOS (4000 and 14000 series) outputs with AHCT and HCTLS inputs when supply voltages are different.

(a) Using logic down converters,
(b) Using Open-drain CMOS
(b) Using resistor divider ($V_{OH} \cdot R_2/(R_1+R_2) \leqslant 5V$)
(d) Using series resistor

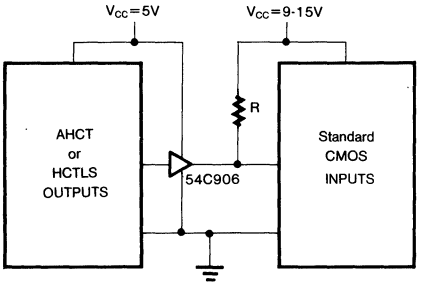


FIGURE 28. Interfacing AHCT and HCTLS outputs with standard CMOS (4000 and 14000) using an open-drain CMOS circuit.

High Voltage and Industrial Control Interfaces

Interfacing with high voltage industrial control circuitry where 4000 or 14000-type of CMOS logic is used has been described in *Figure 27* and *28*. In rugged industrial and automotive environments, more care may be required to prevent large transients from harming AHCT and HCTLS logic. *Figure 29* shows a typical connection that utilizes external diode clamps for input and output protection. The values of R_1 and R_2 depend on the output voltage of the driving circuit and C depends on the noise level and speed. The values of R_3 and R_4 depend on supply voltage and transistor type.

Driving Relays

The high-drive of AHCT and HCTLS outputs enable direct interface with relays, but additional isolation is recommended. Clamp diodes can be used to prevent spikes generated by the relay from harming the circuit. For higher current drive, an external transistor may be employed (*Figures 30* (a) and (b)). Alternatively, multiple gates may be connected in parallel to increase the current sinking and sourcing capability.

Driving LED's

Any AHCT or HCTLS output can be used to drive light-emitting diodes (LED's) directly. *Figure 31* shows two methods of doing this. The resistor performs the founction of current limiter. The luminous intensity of the LED depends on the amount of forward current.

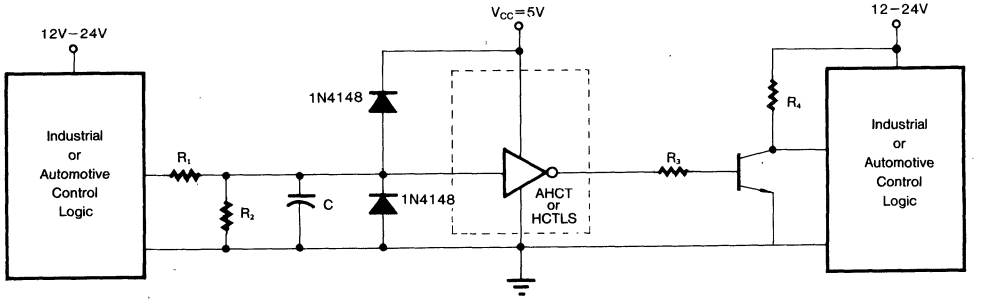


FIGURE 29. Interfacing between AHCT/HCTLS logic and high-voltage industrial and automotive circuitry in rugged environments.

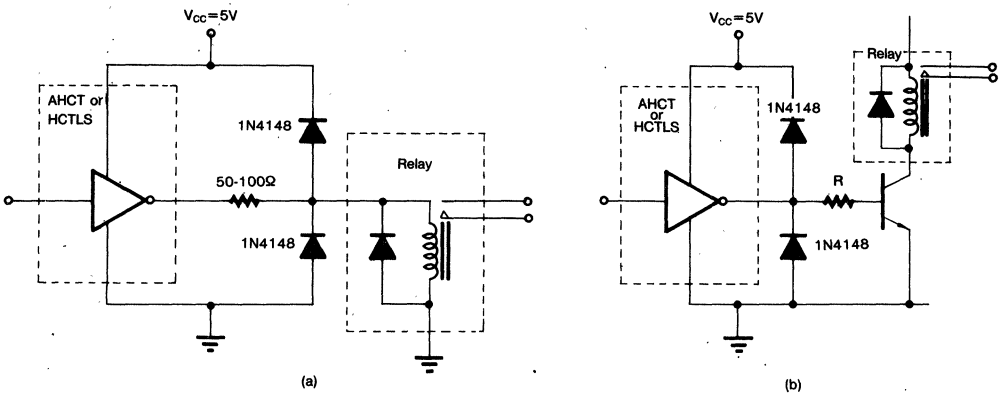


FIGURE 30. Methods of driving relays. (a) Direct and (b) Through a transistor for higher drive ($R = V_{CC} - 0.7)/I_C/\beta$).

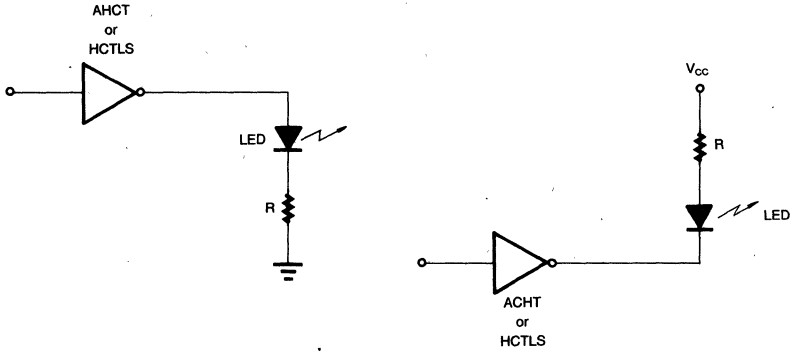


FIGURE 31. Methods of driving LED's

Design Tips

Although the AHCT and HCTLS families are functionally equivalent to the ALS and LS families, some conditions have to be satisfied in order to be able to simply replace them in existing designs. The AHCT and HCTLS families essentially integrate TTL and CMOS characteristics into one family. Therefore, in general, the do's and don'ts of both families apply to the AHCT and HCTLS.

• Don't leave any AHCT or HCTLS input floating. This is frequency overlooked problem with bipolar devices although it is discouraged by every bipolar manufacturer. CMOS inputs have extremely high input impedance and if left unterminated, can pick up noise that causes excursions through the threshold. The result is random switching of the device and high power consumption which can be excessive, especially if the inputs stay very close to the device threshold. Prolonged exposure to these conditions can damage the device. The thing to do is to simply tie the unused inputs to V_{CC} or ground (or they can be tied to nearest operational pin although this may cause more power consumption).

• Don't power up inputs before both V_{CC} and ground are connected, and don't plug boards into or out of powered connectors unless input currents are limited to the absolute maximum ratings specified for the device, and are short-lived. Both conditions can forward bias the input and output ESD protection diodes, resulting in excessive diode currents (see *Figure 32*). If these conditions cannot be avoided, one of the following methods should be used to prevent damage to the AHCT/HCTLS circuits:

— Use connectors that apply power before signals.

— Add series resistors at each input to limit currents to the absolute maximum ratings (*Figure 33a*).

— Add logic to board interfaces that forces all outputs to either ground or high-impedance state when they are connected to unpowered devices (*Figure 33b*).

— Add logic to board inputs to prevent direct interface with unpowered HCTLS inputs (*Figure 33c*). Circuits designed for this purpose are 74AHCT4049 (Hex Inverting Logic Level Down Converter) and 74AHCT4050 (Hex Logic Level Down Converter). These parts have a modified input protection structure that enables them to be used as logic level translators which convert high-level logic to low-level logic while operating from the low logic supply. In this case, since the low logic supply is zero (unpowered), the outputs of the 4049 and 4050 will always be zero regardless of the inputs.

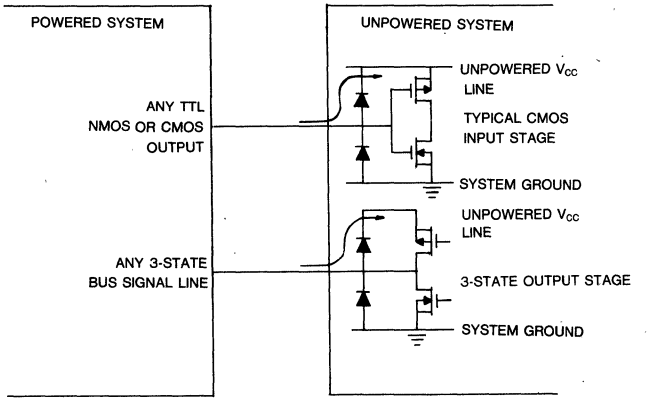


FIGURE 32. Direct interface to unpowered CMOS ICs presents a dangerous situation where high-level signals forward-bias input and output protection diodes and try to "power-up" the V_{CC} line. Excessive currents at such an interface can cause damage to the circuitry.

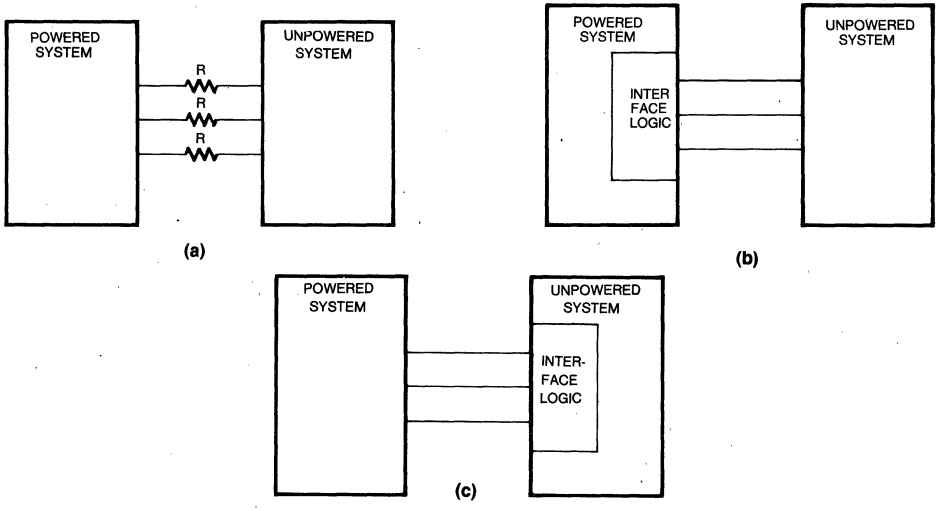


FIGURE 33. Methods of protection in power-down situations: (a) Use of series resistors to limit input currents to absolute maximum ratings, (b) Interface logic circuitry that forces all outputs to either ground or high-impedance state, (c) Interface circuitry at board inputs that acts as buffer between powered and unpowered devices; ideal components for this purpose are the 74AHCT4049 and 74AHCT 4050 Hex Logic Level Down Converters that lack the V_{CC} diode in their protection circuitry.

• In bus-oriented systems, don't allow the bus to stay in high-impedance state for extended periods of time if it is not terminated, because this will have the same effect as leaving inputs open. Two simple ways of terminating the bus are illustrated in *Figure 34*. Most microprocessor-based systems, however, do not keep the bus in 3-state for long periods, in which case, the bus capacitance can maintain valid logic levels. In these cases, pull-up or pull-down circuitry may not be necessary.

•The edge-rates of the AHCT and HCTLS part are similar to the very high-speed TTL parts. Therefore, system grounding and supply-decoupling techniques normally employed in high-speed TTL designs should be duplicated in AHCT/HCTLS designs to ensure proper operation. A good rule of thumb to reduce the affects of PC board trace inductance is to place 0.01 to 0.1 μF RF-grade capacitors every two-to-five ICs (octal flip-flops and buffers may require more decoupling). This, of course, has to be accompanied by careful pc board layout to minimize these inductances.

• The testing problems encountered in ALS, LS and FAST apply also to AHCT and HCTLS. Most of these problems result from the noise produced by the interactions of the device being tested and the test system. Typical test fixtures have lead inductances several times that of a PC board socket. This inductance, especially in the device ground path is the source of these problems.

The outputs, for example, can cause transient currents in the 50 to 200 mA range within a couple of nanoseconds while changing state. These appear as changes in the voltage drop across the device ground lead. The test system's input and output reference voltages are set with respect to tester ground and are not affected by these transients. Consequently the effective input voltages to the device will vary. If the ground pin goes up 1 volt, all the inputs effectively go down 1 volt. This must be considered in selecting input and output voltage levels. In functional tests, for example, solid input logic levels should be applied, instead of 0.8 and 2.0 volts.

Furthermore, if TTL test programs are to be used, one must be particularly careful not to apply voltages to inputs and outputs that are below ground or above V_{CC} in excess of the absolute maximum limits specified in the data sheets.

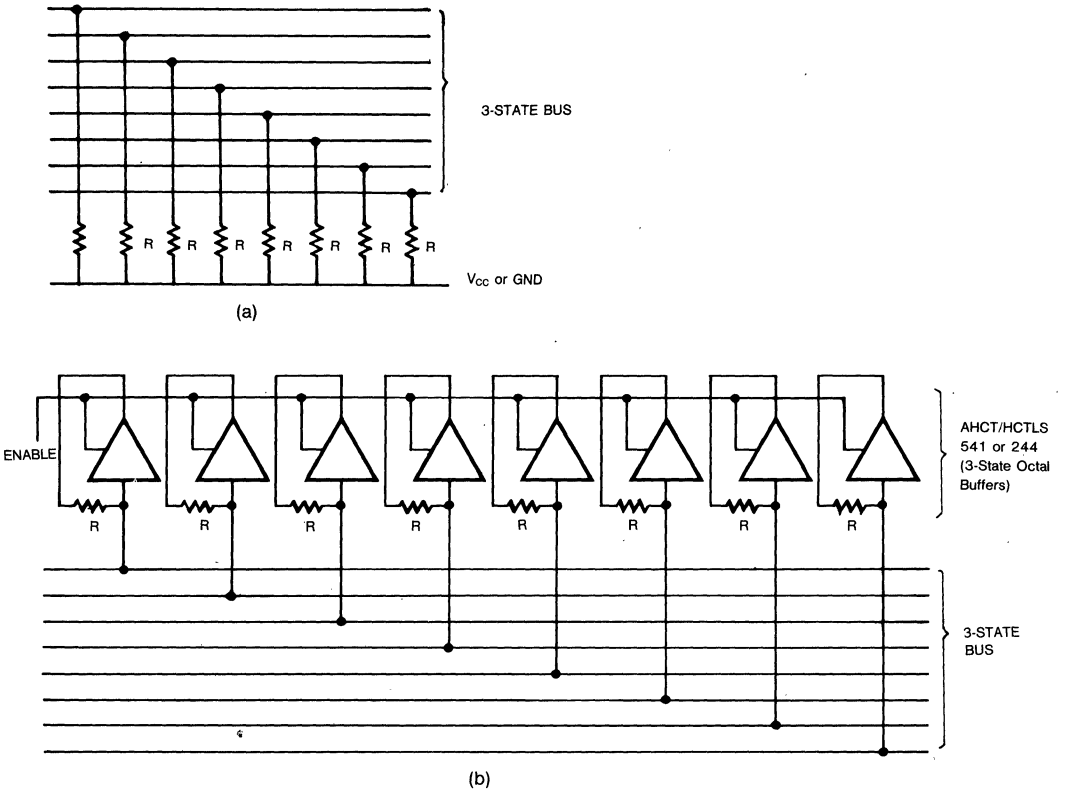
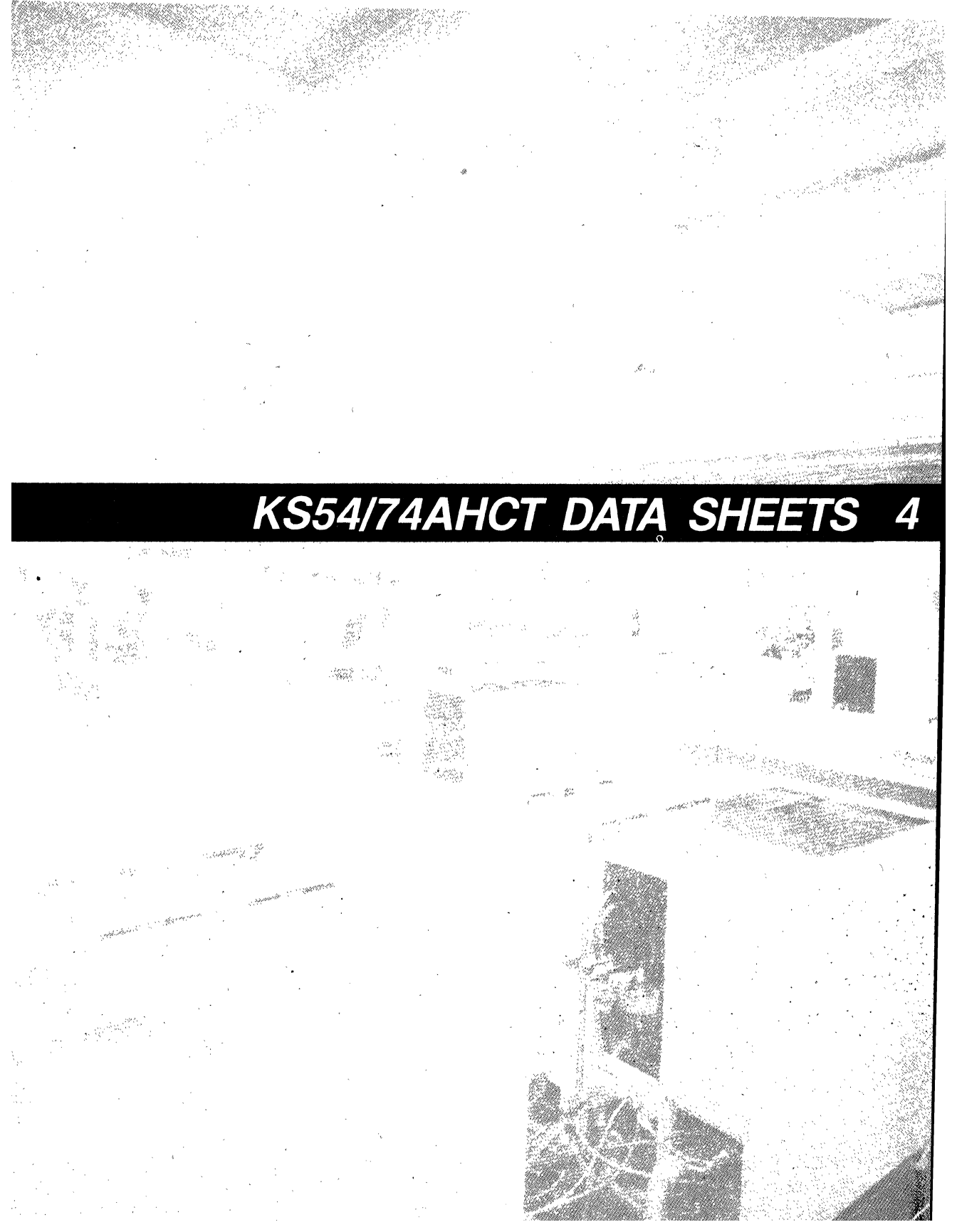


FIGURE 34. Methods of terminating 3-state buses; (a) Pullup or pulldown resistors (b) Use of 3-state buffers. The latter approach terminates the bus to the last active logic level and dissipates no static power.

NOTES

KS54/74AHCT DATA SHEETS 4



Quad 2-Input NAND Gates

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

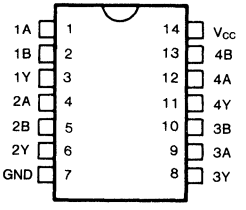
DESCRIPTION

These devices contain four independent 2-input NAND gates that perform the Boolean functions $Y=\overline{A \bullet B}$ or $Y=\overline{A}+\overline{B}$

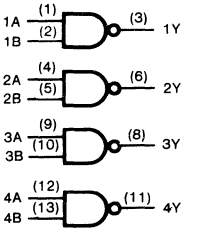
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	**B**	**Y**
H	H	L
L	X	H
X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT00

Characteristic	Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C V_{CC} = 5.0V ± 10%		KS54AHCT T_a = −55°C to +125°C V_{CC} = 5.0V ± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF	7		11		14	ns
	t_{PHL}		7		11		14	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Quad 2-Input NAND Gates with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

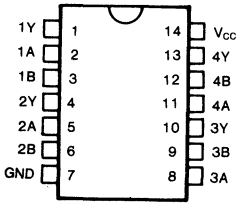
DESCRIPTION

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

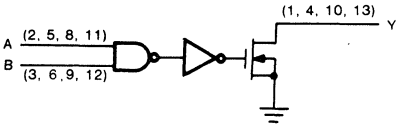
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq$2 ns), AHCT01

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF R_L=1kΩ	17		25		29	ns
	t_{PHL}		10		16		19	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Quad 2-Input NOR Gates

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

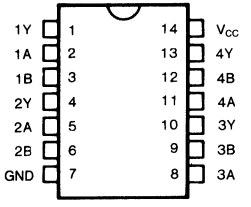
DESCRIPTION

These devices contain four independent 2-input NOR gates that perform the Boolean functions $Y=\overline{A+B}$ or $Y=\overline{A}\bullet\overline{B}$.

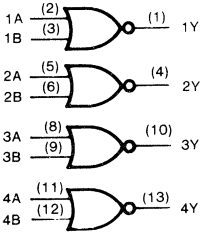
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	**B**	**Y**
H	X	L
X	H	L
L	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT02

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF	7		12		14	ns
	t_{PHL}		7		12		14	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Quad 2-Input NAND Gates with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

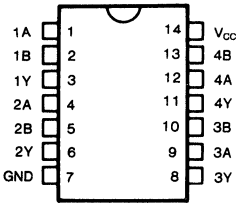
DESCRIPTION

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

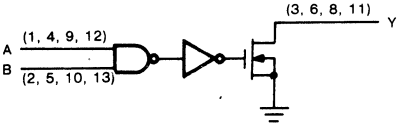
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	**B**	**Y**
H	H	L
L	X	H
X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq$2 ns), AHCT03

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF R_L=1kΩ	17		25		29	ns
	t_{PHL}		10		16		19	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

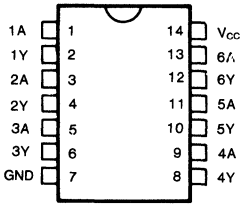
DESCRIPTION

These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

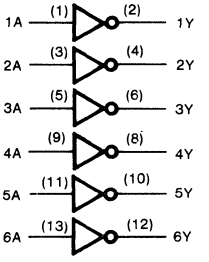
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Inverter)

Input	Output
A	**Y**
H	L
L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT04

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF	7		11		14	ns
	t_{PHL}		7		11		14	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Hex Inverters with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

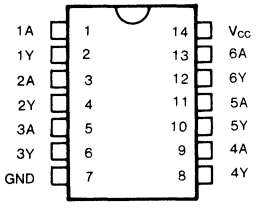
DESCRIPTION

These devices contain six independent inverters with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

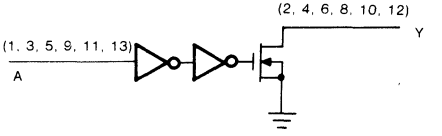
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Inverter)

Input A	Output Y
H	L
L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT05

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF R_L=1kΩ	17		25		29	ns
	t_{PHL}		8		14		33	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per inverter)	15					pF

C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

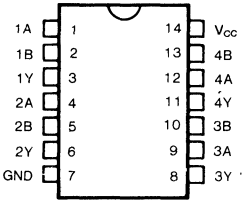
DESCRIPTION

These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$.

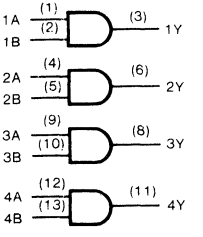
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	B	Y
H	H	H
L	X	L
X	L	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT08

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF	8		14		17	ns
	t_{PHL}		8		14		17	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

Quad 2-Input AND Gates with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

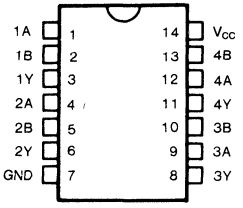
DESCRIPTION

These devices contain four independent 2-input AND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

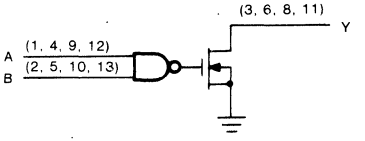
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	B	Y
H	H	H
L	X	L
X	L	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq$ 2 ns), AHCT09

Characteristic	Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C V_{CC} = 5.0V±10%		KS54AHCT T_a = −55°C to +125°C V_{CC} = 5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF R_L=1kΩ	18		27		31	ns
	t_{PHL}		9		15		18	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

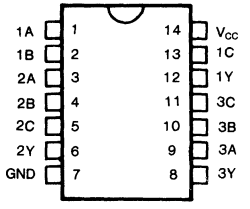
DESCRIPTION

These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y=\overline{A \bullet B \bullet C}$ or $Y=\overline{A}+\overline{B}+\overline{C}$.

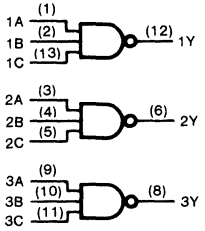
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs			Output
A	**B**	**C**	**Y**
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT10

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF	9		15		18	ns
	t_{PHL}		9		15		18	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Triple 3-Input AND Gates

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

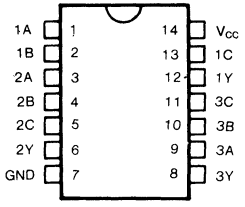
DESCRIPTION

These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y=A \bullet B \bullet C$ or $Y=\overline{A}+\overline{B}+\overline{C}$.

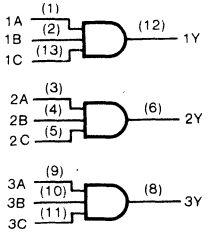
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs			Output
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT11

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF R_L=1kΩ	9		15		18	ns
	t_{PHL}		9		15		18	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

Triple 3-Input NAND Gates with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

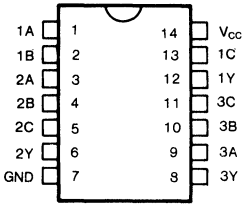
These devices contain three independent 3-input NAND gates with open-drain outputs. They perform the Boolean functions $Y=\overline{A \bullet B \bullet C}$ or $Y=\overline{A}+\overline{B}+\overline{C}$.

Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

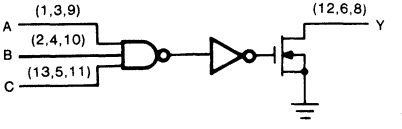
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs			Output
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT12

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF	19		27		31	ns
	t_{PHL}		11		18		22	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74AHCT: −40°C to +85°C KS54AHCT: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

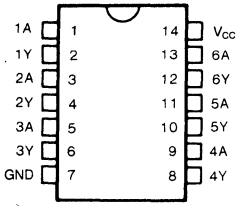
DESCRIPTION

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

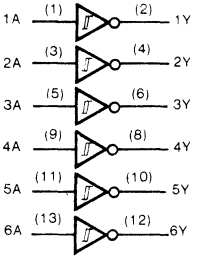
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Inverter)

Input A	Output Y
H	L
L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a= −40°C to +85°C	KS54AHCT T_a= −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.11 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	T_a=25°C		KS74AHCT T_a= −40°C to +85°C		KS54AHCT T_a= −55°C to +125°C		Unit
			Min	Max	Min	Max	Min	Max	
Positive-Going Threshold Voltage	V_{T+}	V_{CC}=4.5V	1.2	1.9	1.2	1.9	1.2	1.9	V
		V_{CC}=5.5V	1.4	2.1	1.4	2.1	1.4	2.1	
Negative-Going Threshold Voltage	V_{T-}	V_{CC}=4.5V	0.5	1.2	0.5	1.2	0.5	1.2	V
		V_{CC}=5.5V	0.6	1.4	0.6	1.4	0.6	1.4	
Hysteresis (V_{T+}-V_{T-})	V_H	V_{CC}=4.5V	0.4	1.4	0.4	1.4	0.4	1.4	V
		V_{CC}=5.5V	0.4	1.5	0.4	1.5	0.4	1.5	

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT14

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	$C_L = 50pF$	8		14		17	ns
	t_{PHL}		8		15		19	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

Dual 4-Input NAND Gates

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

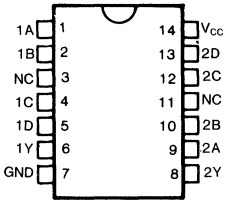
DESCRIPTION

These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y=\overline{A \bullet B \bullet C \bullet D}$ or $Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic.

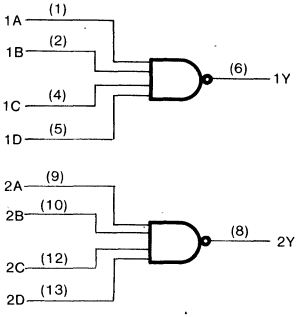
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT20

Characteristic	Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C V_{CC} = 5.0V±10%		KS54AHCT T_a = −55°C to +125°C V_{CC} = 5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Y	t_{PLH}	C_L=50pF	7		11		13	ns
	t_{PHL}		7		11		13	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

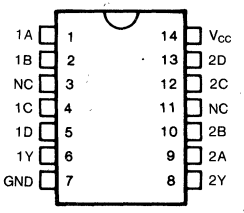
DESCRIPTION

These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y=A \bullet B \bullet C \bullet D$ or $Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic.

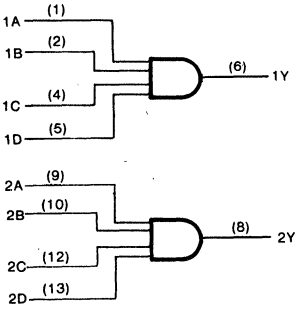
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT21

Characteristic	Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C V_{CC} = 5.0V±10%		KS54AHCT T_a = −55°C to +125°C V_{CC} = 5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Y	t_{PLH}	C_L=50pF	8		14		17	ns
	t_{PHL}		8		14		17	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

Dual 4-Input NAND Gates with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

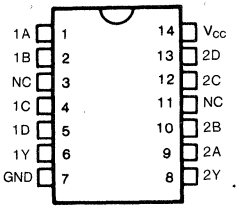
DESCRIPTION

These devices contain two independent 4-input NAND gates. These gates perform the Boolean fucntions $Y=\overline{A \bullet B \bullet C \bullet D}$ or $Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active low wired-OR or active high wired-AND functions.

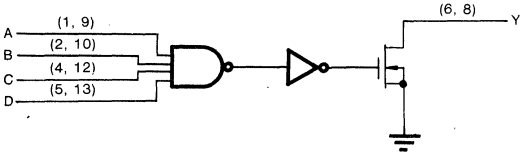
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT22

Characteristic	Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C V_{CC} = 5.0V±10%		KS54AHCT T_a = −55°C to +125°C V_{CC} = 5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Y	t_{PLH}	C_L=50pF R_L=1kΩ	19		29		34	ns
	t_{PHL}		11		18		22	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

Triple 3-Input NOR Gates

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

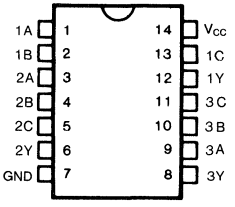
DESCRIPTION

These devices contain two independent 3-input NOR gates. They perform the Boolean functions $Y=\overline{A+B+C}$ or $Y=\overline{A}\bullet\overline{B}\bullet\overline{C}$ in positive logic.

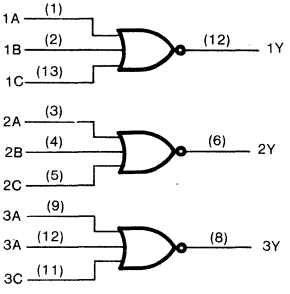
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT27

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Y	t_{PLH}	C_L=50pF	8		14		17	ns
	t_{PHL}		10		16		20	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

8-Input Nand Gate

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '30 contains a single 8-input NAND gate. It performs the boolean functions (in positive logic):

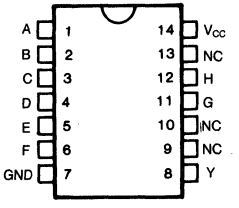
$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$

$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$

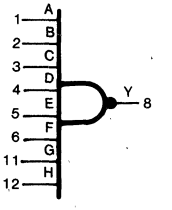
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inputs A Through H		Output Y
All Inputs	H	L
One or more inputs	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f. . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$		0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT30

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF	6		11		14	ns
	t_{PHL}		6		11		14	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}		15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD}\,V_{CC}^2\,f + I_{CC}\,V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Quad 2-Input OR Gates

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

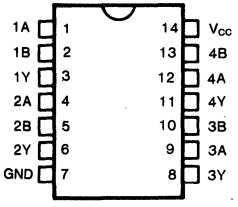
DESCRIPTION

These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y=A+B$ or $Y=\overline{A \bullet B}$.

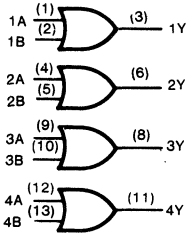
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL. NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damaged due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Outputs
A	B	Y
H	X	H
X	H	H
L	L	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0:39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT32

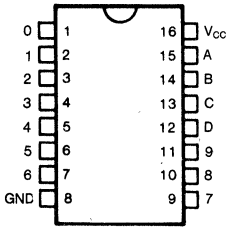
Characteristic	Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C V_{CC} = 5.0V ± 10%		KS54AHCT T_a = −55°C to +125°C V_{CC} = 5.0V ± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF	8		14		17	ns
	t_{PHL}		8		14		17	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Full decoding of Input Logic**
- **All outputs are High for Invalid BCD Conditions**
- **Also for application as 3-Line to 8-Line Decoders**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



FUNCTION TABLE

No.	Inputs				Outputs								
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

DESCRIPTION

The '42 decoder accepts for active-high BCD inputs and provides 10 mutually exclusive active-low outputs, as shown by logic symbol or diagram. The active-low outputs facilitate addressing other MSI units with active low input enables.

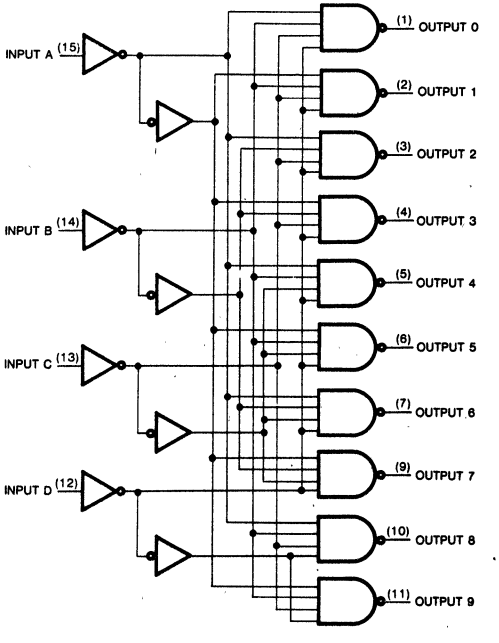
The logic design of the '42 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant input, D, produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The D input can also be used as the Data input in an 8-output demultiplexer application.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT42

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Y	t_{PLH}	C_L=50pF	11		18		22	ns
	t_{PHL}		11		18		22	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

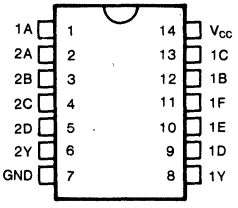
The '51 performs the following Boolean functions:
$1Y=\overline{(1A \bullet 1B \bullet 1C)+(1D \bullet 1E \bullet 1F)}$
$2Y=\overline{(2A \bullet 2B)+(2C \bullet 2D)}$

The '58 performs:
$1Y=(1A \bullet 1B \bullet 1C)+(1D \bullet 1E \bullet 1F)$
$2Y=(2A \bullet 2B)+(2C \bullet 2D)$

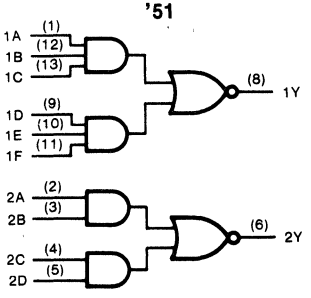
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



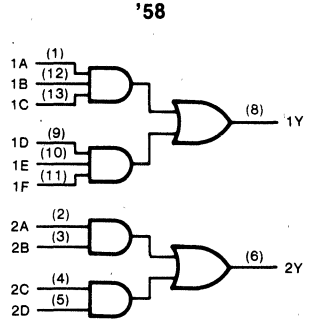
LOGIC DIAGRAMS



FUNCTION TABLES

Inputs						Output 1Y	
1A	1B	1C	1D	1E	1F	'51	'58
H	H	H	X	X	X	L	H
X	X	X	H	H	H	L	H
Any other combination						H	L

Inputs				Output 2Y	
2A	2B	2C	2D	'51	'58
H	H	X	X	L	H
X	X	H	H	L	H
Any other combination				H	L



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT51, AHCT58

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF	9		15		18	ns
	t_{PHL}		9		15		18	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

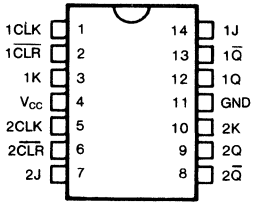
DESCRIPTION

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at $\overline{CLR}$ input resets the outputs regardless of the levels of the other inputs. When $\overline{CLR}$ is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

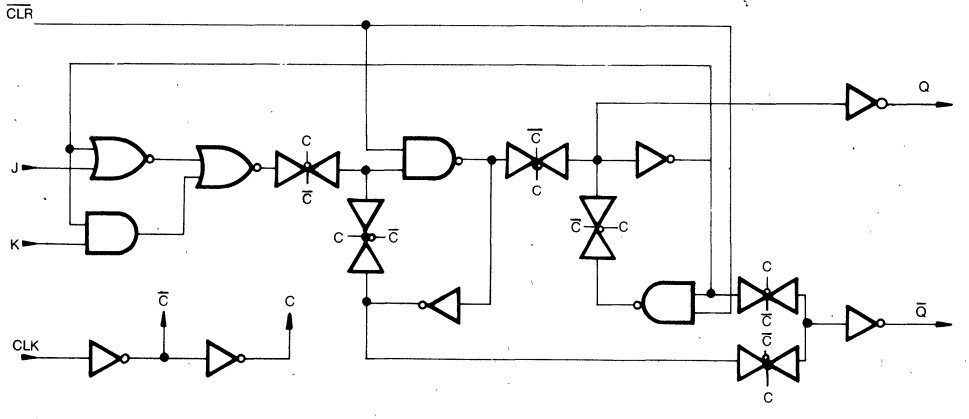
PIN CONFIGURATION



FUNCTION TABLE

Inputs				Outputs	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

LOGIC DIAGRAM



Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT73

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	45	30		25		MHz
Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Propagation Delay, $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Setup Time before CLK↓	J or K	t_{su}		8	13		15		ns
	$\overline{CLR}$ Inactive			8	13		15		
Hold Time, J or K after CLK↓		t_h		−3	0		0		ns
Pulse Width	CLK High or Low	t_w		8	13		15		ns
	$\overline{CLR}$ Low			8	13		15		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per flip-flop)	40					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

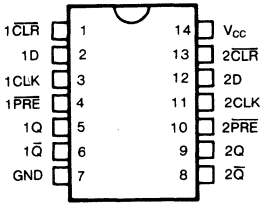
DESCRIPTION

These devices contain two independent positive-edge-triggered D-type flip-flops. Each flip-flop has its own data, clock, preset and clear inputs and complementary Q and $\overline{Q}$ outputs. The preset and clear inputs are active-low and operate independently of the clock. Data at the D input is transferred to the Q outputs on the positive transition of the clock, provided setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

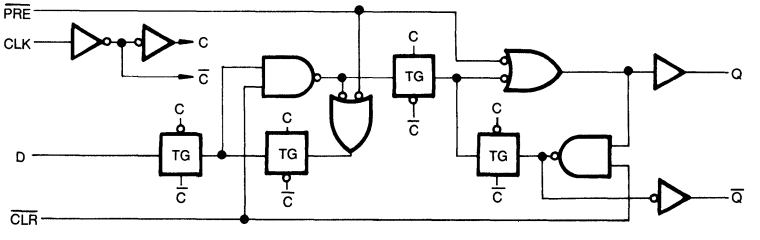


FUNCTION TABLE

Inputs				Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

* Both outputs will remain high as long as $\overline{PRE}$ and $\overline{CLR}$ are low, but the output states are unpredictable if $\overline{PRE}$ and $\overline{CLR}$ go high simultaneously.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT74

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	55	34		30		MHz
Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Propagation Delay, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		9		15		18	ns
		t_{PHL}		9		15		18	
Setup Time before CLK↑	Data	t_{su}		7	12		15		ns
	$\overline{PRE}$ or $\overline{CLR}$ Inactive			5	8		10		
Hold Time, Data after CLK↑		t_h		−3	0		0		ns
Pulse Width	CLK High or Low	t_w		9	15		17		ns
	$\overline{PRE}$ or $\overline{CLR}$ Low			9	15		17		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

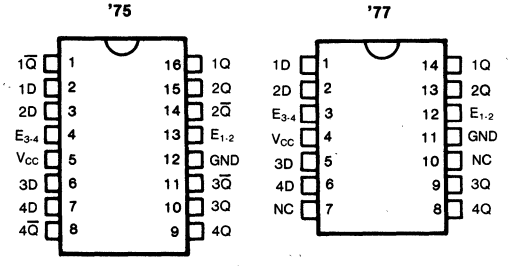
The '75 and '77 consist of 4 high-speed D-type latches that can be used as temporary storage for binary information between processing units. The '75 features complementary Q and $\overline{Q}$ output while the '77 features single nail output. These devices are ideal for high component density application.

The latches are transparent: when the enable (E) is high, the Q output will follow the data input. When the enable goes low, the output latches at the level that was set up at the D-input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

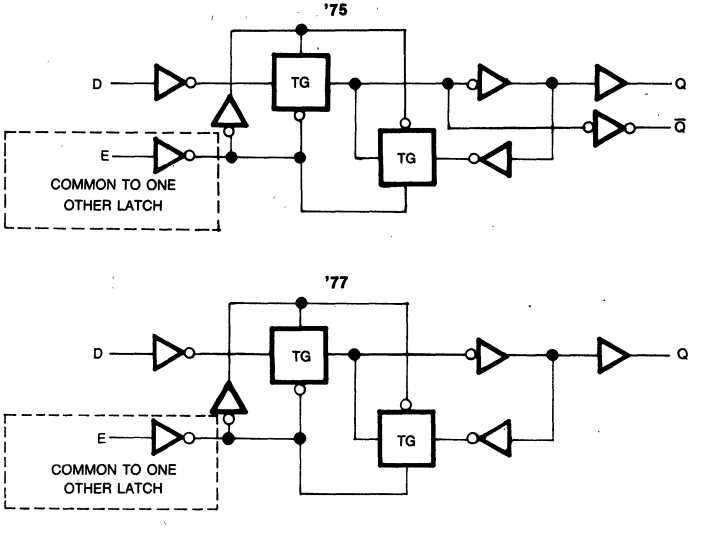


FUNCTION TABLE

Inputs		Outputs	
D	E	Q	$\overline{Q}$*
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

*$\overline{Q}$: '75 only

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT75

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	$C_L = 50pF$	10		16		20	ns
E to Q or $\overline{Q}$	t_{PHL}		10		16		20	
Propagation Delay	t_{PLH}	$C_L = 50pF$	9		15		18	ns
D to Q or $\overline{Q}$	t_{PHL}		9		15		18	
Data Set up Time D to Enable	t_{SU}		6	10		12		ns
Data Hold Time Enable to D	t_h		3		5		6	ns
Input Capacitance	C_{IN}		5					pF
Power disipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT77

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	$C_L = 50pF$	8		14		17	ns
E to Q	t_{PHL}		8		14		17	
Propagation Delay	t_{PLH}	$C_L = 50pF$	8		13		15	ns
D to $\overline{Q}$	t_{PHL}		8		13		15	
Data Set up Time D to Enable	t_{SU}		6	10		12		ns
Data Hold Time Enable to D	t_h		3		5		6	ns
Input Capacitance	C_{IN}		5					pF
Power disipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

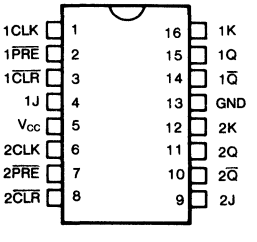
DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

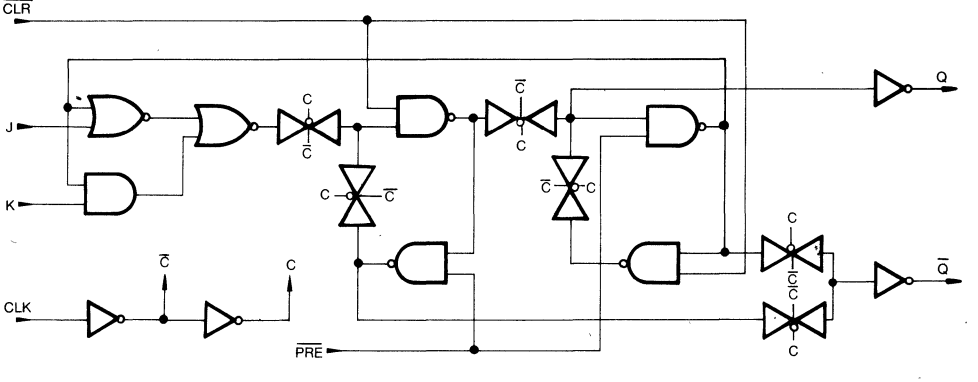


FUNCTION TABLE

Inputs					Outputs	
PRE	CLR	CLK	J	K	Q	Q
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT76

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	45	30		25		MHz
Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Propagation Delay, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Setup Time before CLK↓	J or K	t_{su}		10	17		20		ns
	$\overline{PRE}$ or $\overline{CLR}$ Inactive			10	17		20		
Hold Time, Data after CLK↓		t_h		−3	0		0		ns
Pulse Width	CLK High or Low	t_w		8	13		15		ns
	$\overline{PRE}$ or $\overline{CLR}$ Low			8	13		15		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per flip-flop)	40					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

Dual J-K Flip-Flops with Preset, Common Clear & Common Clock

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

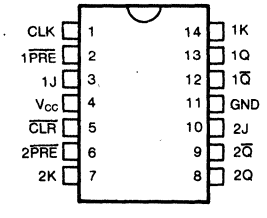
DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K and preset inputs and complementary outputs. The clear and clock inputs are common to both flip-flops. The J-K inputs are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

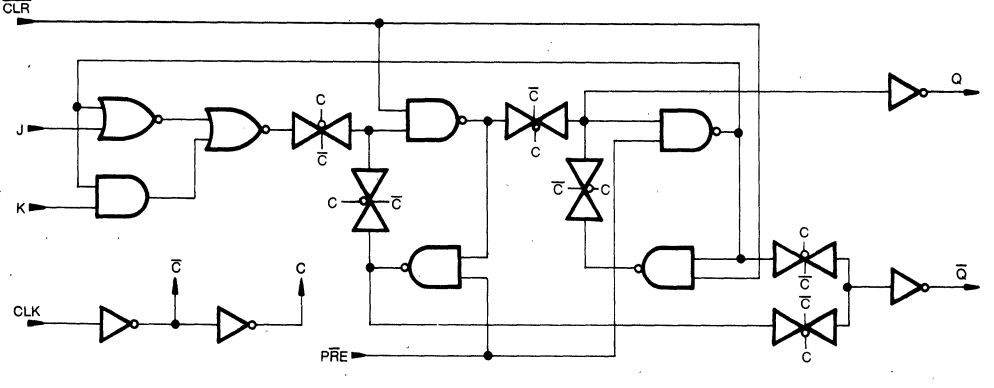


FUNCTION TABLE

Inputs					Outputs	
PRE	CLR	CLK	J	K	Q	Q
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT78

Characteristic		Symbol	Conditions†	$T_a=25°C$ $V_{CC}=5.0V$	KS74AHCT $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54AHCT $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L=50pF$	45	30		25		MHz
Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Propagation Delay, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Setup Time before CLK↓	J or K	t_{su}		10	17		20		ns
	$\overline{PRE}$ or $\overline{CLR}$ Inactive			10	17		20		
Hold Time, J or K after CLK↓		t_h		−3	0		0		ns
Pulse Width	CLK High or Low	t_w		8	13		15		ns
	$\overline{PRE}$ or $\overline{CLR}$ Low			8	13		15		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per flip-flop)	40					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

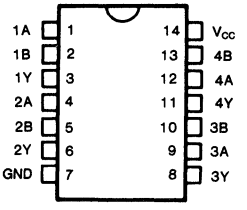
DESCRIPTION

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y=A\oplus B$ or $Y=\overline{A}B+A\overline{B}$.

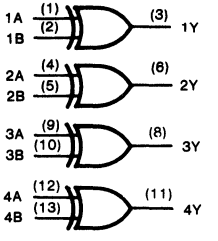
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT86

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to Y (Other Input Low)	t_{PLH}	$C_L = 50pF$	10		16		19	ns
	t_{PHL}		10		16		19	
Propagation Delay, A or B to Y (Other Input High)	t_{PLH}		12		20		24	ns
	t_{PHL}		12		20		24	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per flip-flop)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

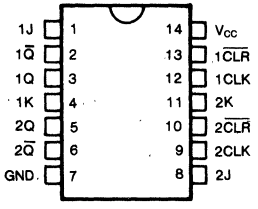
DESCRIPTION

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the $\overline{CLR}$ input resets the outputs regardless of the levels of the other inputs. When $\overline{CLR}$ is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

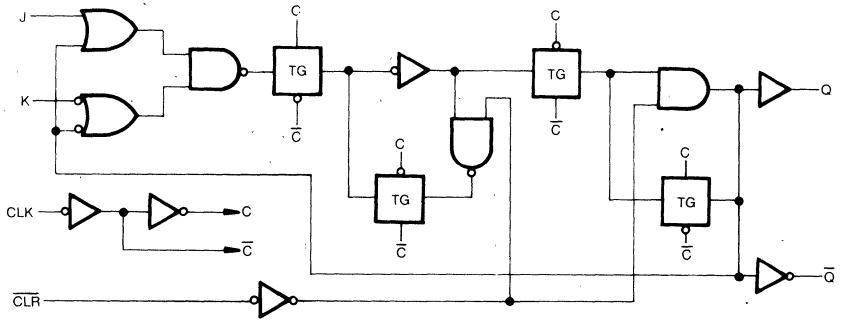
PIN CONFIGURATION



FUNCTION TABLE

Inputs				Outputs	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT107

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	45	30		25		MHz
Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Propagation Delay, $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Setup Time before CLK↓	J or K	t_{su}		10	17		20		ns
	$\overline{CLR}$ Inactive			10	17		20		
Hold Time, J or K after CLK↓		t_h		−3	0		0		ns
Pulse Width	CLK High or Low	t_w		8	13		15		ns
	$\overline{CLR}$ Low			8	13		15		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per flip-flop)	40					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flops with Preset and Clear

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

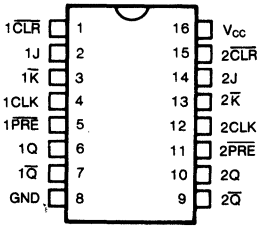
DESCRIPTION

These devices contain two positive-edge-triggered J-$\overline{K}$ flip-flops with independent preset and clear inputs and complementary Q and $\overline{Q}$ outputs. The present and clear inputs are active-low and operate independently of the clock Data at the J and $\overline{K}$ inputs are transferred to the ouptuts on the positive transition of the clock provided setup requirements have been met. These versatile flip-flops can perform as toggel flip-flops by grounding K and tying J high. They can also perform as D-type flops if J and $\overline{K}$ are tied together.

These devices provide speeds and drive capability equivalent to their ALST'. counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

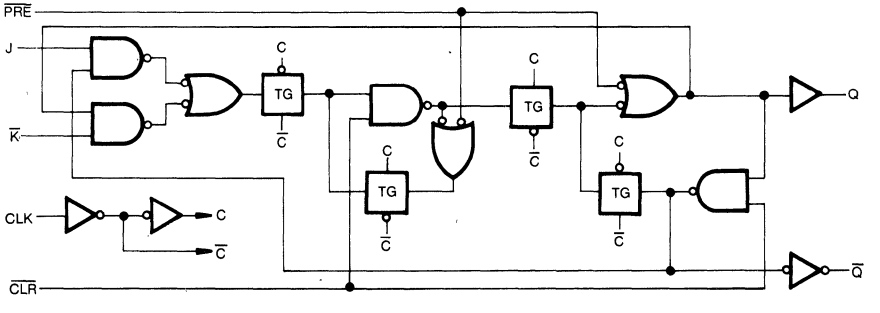


FUNCTION TABLE

Inputs					Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

*Both outputs will remain high as long as $\overline{PRE}$ and $\overline{CLR}$ are low, but the output states are unpredictable if $\overline{PRE}$ and $\overline{CLR}$ go high simultaneously.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT109

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	55	34		30		MHz
Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Propagation Delay, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Setup Time before CLK↑	Data	t_{su}		7	12		15		ns
	$\overline{PRE}$ or $\overline{CLR}$ Inactive			5	8		10		
Hold Time, Data after CLK↑		t_h		−3	0		0		ns
Pulse Width	CLK High or Low	t_w		9	15		17		ns
	$\overline{PRE}$ or $\overline{CLR}$ Low			9	15		17		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

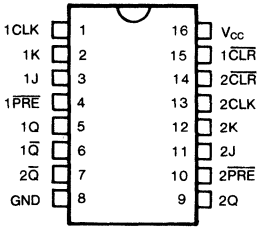
DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

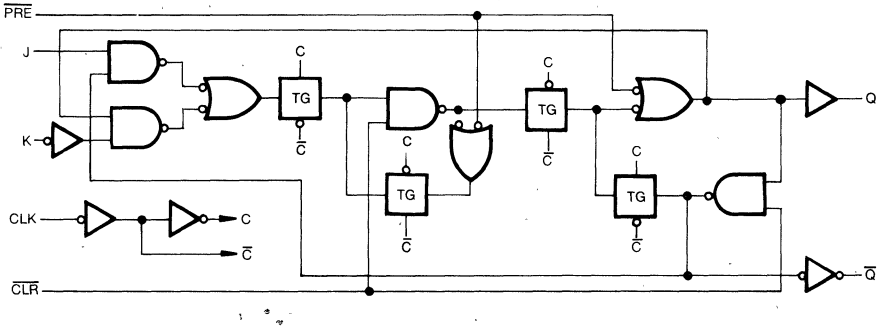


FUNCTION TABLE

Inputs					Outputs	
PRE	CLR	CLK	J	K	Q	Q
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*Both outputs will remain high as long as PRE and CLR are low, but the output states are unpredictable if PRE and CLR go high simultaneously.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT112

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	50	30		25		MHz
Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Propagation Delay, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Setup Time before CLK↓	J or K	t_{su}		10	17		20		ns
	$\overline{PRE}$ or $\overline{CLR}$ Inactive			10	17		20		
Hold Time, Data after CLK↓		t_h		−3	0		0		ns
Pulse Width	CLK High or Low	t_w		10	17		20		ns
	$\overline{PRE}$ or $\overline{CLR}$ Low			6	10		15		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per flip-flop)	40					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

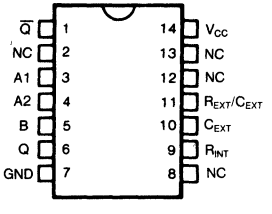
Monostable Multibrators with Schmitt-Trigger Inputs

Preliminary Specifications

FEATURES

- **Schmitt-trigger for slow input transitions**
- **Internal timing resistor**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range; 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74AHCT: −40°C to +85°C KS54AHCT: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	X	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎌
↓	H	H	⎍	⎌
↓	↓	H	⎍	⎌
L	X	↑	⎍	⎌
X	L	↑	⎍	⎌

H= HIGH Voltage level
L= LOW voltage level
X= Don't care
↑= LOW-to-HIGH transition
↓= HIGH-to-LOW transition
⎍= one HIGH level output pulse
⎌= one LOW level output pulse

DESCRIPTION

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{INT} connected to V_{CC}, C_{EXT} and C_{EXT}/C_{EXT} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of extermal timing components.

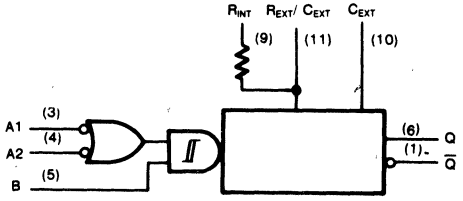
Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10μF) and more than one decade of timing resistance (2 kΩ to 40 kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_{EXT} R_{EXT} \ln 2 = 0.7\ C_{EXT}\ R_{EXT}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_{EXT}. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts any yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external compoennts.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

4

LOGIC DIAGRAM



Notes: 1. An external capacitor may be connected between C_{EXT} (positive) and R_{EXT}/C_{EXT}.
2. To use the internal timing resistor, connect R_{INT} to V_{CC}. For improved pulse width accuracy and repeatability connect on external resistor between R_{EXT}/C_{EXT} V_{CC} with R_{INT} open-circuited.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I<−0.5V or V_I>V_{CC}+0.5V) ..... ±20 mA
DC Output Diode Current, I_{Ok}
(V_O<−0.5V or V_O>V_{CC}+0.5V) ..... ±20 mA
Continuous OUtput Current Per Pin, I_O
(−0.5V<V_O<V_{CC}+0.5V) ..... ±35 mA
Continuous Current Through
V_{CC} or GND pins ..... ±125 mA
Storage Temperature Range, T_{stg} −65°C to +150°C
Power Dissipation Per Package, P_d† ..... 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package(N): −12mW/°C from 65°C to 85°C
Ceramic Package(J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} ..... 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f ..... Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT121

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay A, B to Q, $\overline{Q}$	t_{PLH}	$C_L = 50pF$ $C_{ext} = 80pF$ R_{int} to V_{CC}	40		54		65	ns
	t_{PHL}		40		54		65	
Propagation Delay B to Q & $\overline{Q}$ output	t_{PLH}		30		43		51	ns
	t_{PHL}		30		43		51	
Minimum Output pulse width	t_w	$C_{ext} = 0pF$ R_{int} to V_{CC}	35		52		52	ns
Output pulse width	t_w	$C_{ext} = 80pF$ R_{int} to V_{CC}	110	67	156	67	156	ns
		$C_{ext} = 100pF$ $R_{ext} = 10k\Omega$	700	602	798	595	805	ns
		$C_{ext} = 1\mu F$ $R_{ext} = 10k\Omega$	7	6	8	5.9	8.1	ms
Minimum input pulse width to trigger	t_w			40		40		ns
External timing tesistor range	R_{ext}		10	1.4	40	1.4	40	kΩ
External timing capacitance range	C_{ext}			0	1,000	0	1,000	μF
Output Duty cycle		$R_{ext} = 2k\Omega$			67		67	%
		$R_{ext} = R_{ext(max)}$			90		90	%
Input Capacitance	C_{in}							
Power dissipation Capacitance	C_{PD}							

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

Dual Retriggerable Monostable Multivibrator with Clear

Preliminary Specifications

FEATURES

- **Simple pulse width formula $t_W = 0.45RC$**
- **DC triggered from active HIGH or active Low inputs**
- **Retriggerable for very long output pulses up to 100% duty cycle**
- **Overriding clear terminates output pulse**
- **Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs**
- **Functions, pin-out, speed and drive compativility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High drive current outputs: $I_{OL} = 8mA$ @ $V_{OL} = 0.5V$**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range; 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74AHCT: −40°C to +85°C KS54AHCT: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '123 contains dual retriggerable monostable multivibrators with output pulse width control by three methods.

The basic pulse time is programmed by selection of an external resistor (Rext) and capacitor (Cext). The external resistor and capacitor are normally connected as shown timing component.

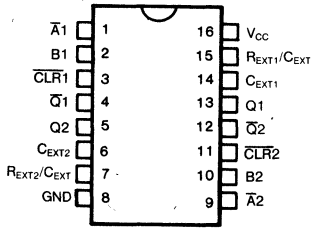
Once triggered, the basic output pulse width may be extended by retriggering the gated active Low going edge input (Ai) or the active HIGH going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH, $n\overline{Q}$=LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a Low-going edge on input CLR, which also inhibits the triggering.

An internal connection from CLR to the input gates makes it possible to trigger the circuit by a positive-going signal at input CLR as shown in the function table when $C_{EXT} > 10nF$, the typical output pulse width is defined as; $t_W = 0.45 \times R_{EXT} \times C_{EXT}$(typ).

Where t_w is in seconds. R is in ohm. and C is in fards.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Outputs	
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H= HIGH voltage level
L= LOW voltage level
X= don't care
↑= LOW to HIGH transition
↓= HIGH to LOW transition
⎍= one HIGH level output pulse
⎎= one LOW level output pulse

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I<−0.5V or V_I>V_{CC}+0.5V) ..... ±20 mA
DC Output Diode Current, I_{Ok}
(V_O<−0.5V or V_O>V_{CC}+0.5V) ..... ±20 mA
Continuous OUtput Current Per Pin, I_O
(−0.5V<V_O<V_{CC}+0.5V) ..... ±35 mA
Continuous Current Through
V_{CC} or GND pins ..... ±125 mA
Storage Temperature Range, T_{stg} −65°C to +150°C
Power Dissipation Per Package, P_d† ..... 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package(N): −12mW/°C from 65°C to 85°C
Ceramic Package(J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} ..... 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f ..... Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT123

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	$C_L = 50pF$ $C_{ext} = 0$, $R_{ext} = 5k\Omega$	18		33		39	ns
$\overline{A}$, B to Q, $\overline{Q}$	t_{PHL}		18		33		39	
Propagation Delay	t_{PLH}		16		27		32	ns
$\overline{CLR}$ to Q, $\overline{Q}$	t_{PHL}		16		27		32	
Output Pulse Width 1	t_{WQ1}		116		207		209	ns
Output Pulse Width 2	t_{WQ2}	$C_L = 50pF$ $C_{ext} = 1000pF$ $R_{ext} = 10k\Omega$	4.5	3.8	5.2	3.8	5.2	μs
Trigger Pulse Width	t_w	$C_L = 50pF$ A_i = LOW	5		16		20	ns
Trigger Pulse Width	t_w	$C_L = 50pF$ B_i = High	5		16		20	ns
Clear Pulse Width	t_w	$C_L = 50pF$ CLR_i = LOW	6		16		20	ns
External Timing Resistance	R_{ext}			2	1,000	2	1,000	kΩ
External Timing Capacitance	C_{ext}		no restriction					
Input Capacitance	C_{in}		5					pF
Power Dissipation Capacitance	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Application Information

The basic output pulse width is determined by the value of external capacitance and timing resistance.
For output pulse widths greater than 100μs or external capacitance greater than 1000pF the following equation should be used.

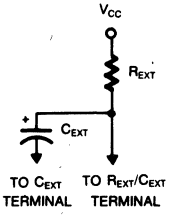
$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

t_w is in second
K is the multiplying factor
and is approximately 0.45 for $C_{ext} \geq 1000pF$
C_{ext} is in F

For best results, system ground should be applied to the C_{ext} terminal. These devices do not require a switching diode in series with the R_{ext}/C_{ext} terminal (as required by some other monostable multivibrators)

TIMING COMPONENT



FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

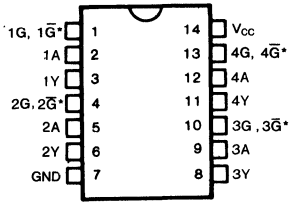
DESCRIPTION

These bus buffers feature four independent line drivers with 3-state outputs. The output enable functions for the '125 buffers are active-low, while those for '126 are active high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



*$\bar{G}$ for '125: G for '126

FUNCTION TABLES

'125

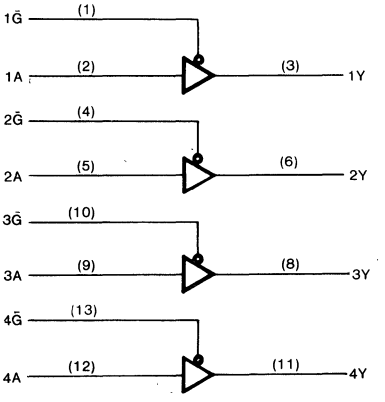
Inputs		Output
A	$\bar{G}$	Y
H	L	H
L	L	L
X	H	Z

'126

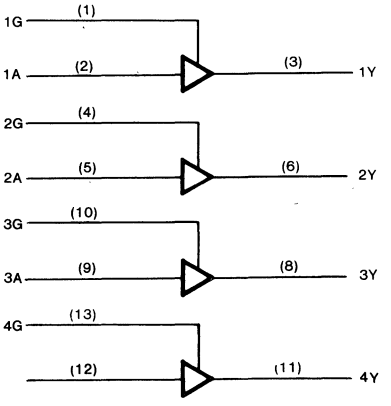
Inputs		Output
A	G	Y
H	H	H
L	H	L
X	L	Z

LOGIC DIAGRAMS

'125



'126



4

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} . . . . . −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT125, AHCT126

Characteristic	Symbol	Conditions†	$T_a=25°C$ $V_{CC}=5.0V$	KS74AHCT $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54AHCT $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A to Y	t_{PLH}	$C_L=50pF$	6		10		12	ns
		$C_L=150pF$	9		15		18	
	t_{PHL}	$C_L=50pF$	6		10		12	
		$C_L=150pF$	9		15		18	
Output Enable Time Enable to Y	t_{PZH}	$R_L=1k\Omega$, $C_L=50pF$	11		18		22	ns
		$R_L=1k\Omega$, $C_L=150pF$	14		23		28	
	t_{PZL}	$R_L=1k\Omega$, $C_L=50pF$	11		18		22	
		$R_L=1k\Omega$, $C_L=150pF$	14		23		28	
Output Disable Time, Enable to Y	t_{PHZ}	$R_L=1k\Omega$, $C_L=50pF$	13		18		22	ns
	t_{PLZ}		13		18		22	
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	G or $\overline{G}=V_{CC}$	5					pF
		G or $\overline{G}=GND$	30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

Quad Schmitt-Trigger NAND Gates

Preliminary Specifications

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

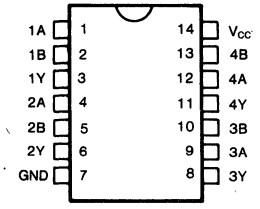
These Schmitt-trigger devices contain four independent NAND gates. They perform the Boolean function $Y=\overline{A \bullet B}=\bar{A}+\bar{B}$ in positive logic.

The input threshold levels are temperature compensated and can be triggered from the slowest of input ranges and still give jitter-free output signals.

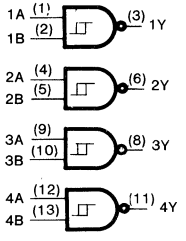
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a= −40°C to +85°C	KS54AHCT T_a= −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.11 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	T_a=25°C		KS74AHCT T_a= −40°C to +85°C		KS54AHCT T_a= −55°C to +125°C		Unit
			Min	Max	Min	Max	Min	Max	
Positive-Going Threshold Voltage	V_{T+}	V_{CC}=4.5V	1.2	1.9	1.2	1.9	1.2	1.9	V
		V_{CC}=5.5V	1.4	2.1	1.4	2.1	1.4	2.1	
Negative-Going Threshold Voltage	V_{T-}	V_{CC}=4.5V	0.5	1.2	0.5	1.2	0.5	1.2	V
		V_{CC}=5.5V	0.6	1.4	0.6	1.4	0.6	1.4	
Hysteresis (V_{T+}-V_{T-})	V_H	V_{CC}=4.5V	0.4	1.4	0.4	1.4	0.4	1.4	V
		V_{CC}=5.5V	0.4	1.5	0.4	1.5	0.4	1.5	

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT132

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Y	t_{PLH}	$C_L = 50pF$	8		14		17	ns
	t_{PHL}		8		14		17	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

13-Input NAND Gates

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '133 contains a single 13-input NAND gate. It performs the boolean functions (in positive logic):

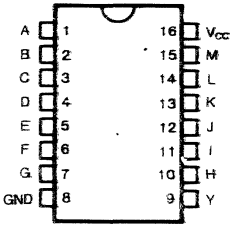
$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$

$Y = \overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+\overline{F}+\overline{G}+\overline{H}+\overline{I}+\overline{J}+\overline{K}+\overline{L}+\overline{M}$

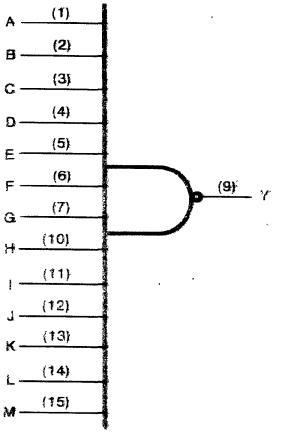
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS A THRU M		OUTPUT Y
All inputs	H	L
One or more inputs	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT133

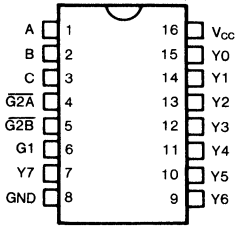
Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Y	t_{PLH}	C_L=50pF	11		18		22	ns
	t_{PHL}		11		18		22	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Designed specifically for high-speed memory decoders and data transmission systems**
- **Incorporates 3 enable inputs to simplify cascading and/or data reception**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



FUNCTION TABLE

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

DESCRIPTION

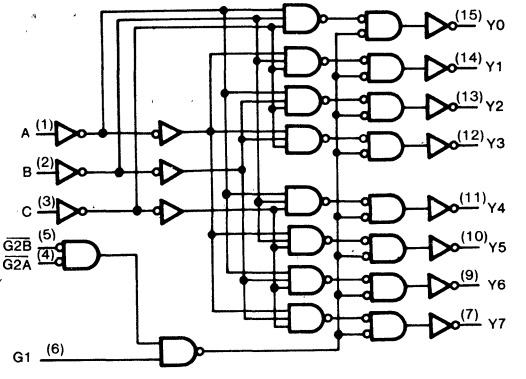
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} . . . . . −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT138

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A, B, C or any Y	t_{PLH}	$C_L = 50pF$	12		20		24	ns
	t_{PHL}		12		20		24	
Propagation Delay, G1 to any Y	t_{PLH}		10		17		20	ns
	t_{PHL}		10		17		20	
Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to any Y	t_{PLH}		10		17		20	ns
	t_{PHL}		10		17		20	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}		50					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

Dual 1-of-4 Decoders/Demultiplexers

FEATURES

- **Designed specifically for high-speed memory decoders and data transmission systems**
- **Incorporates 2 enable inputs to simplify cascading and/or data reception**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

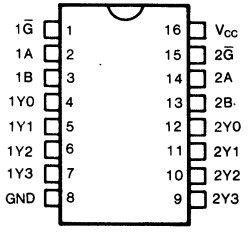
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory, this means that the effective system delay introduced by the decoder is negligible.

The '139 consists of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

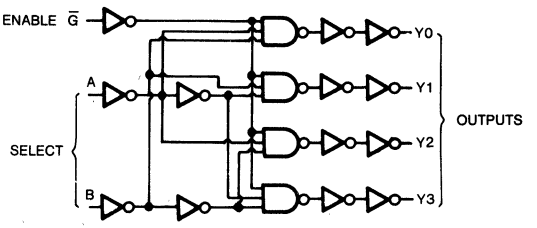
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM

(Each Decoder/Demultiplexer)



FUNCTION TABLE

Inputs			Outputs			
Enable G̅	Select B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

4

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT139

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to Y	t_{PLH}	$C_L = 50pF$	11		17		20	ns
	t_{PHL}		11		17		20	
Propagation Delay, $\overline{G}$ to any Y	t_{PLH}		11		18		21	ns
	t_{PHL}		11		18		21	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}		50					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

FEATURES

- **Encodes eight data lines in priority**
- **Provides 3-bit binary priority code**
- **Input enable capability**
- **Easily cascadable**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

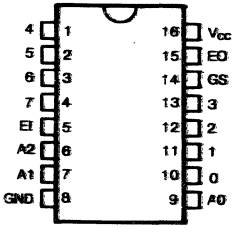
DESCRIPTION

The '148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

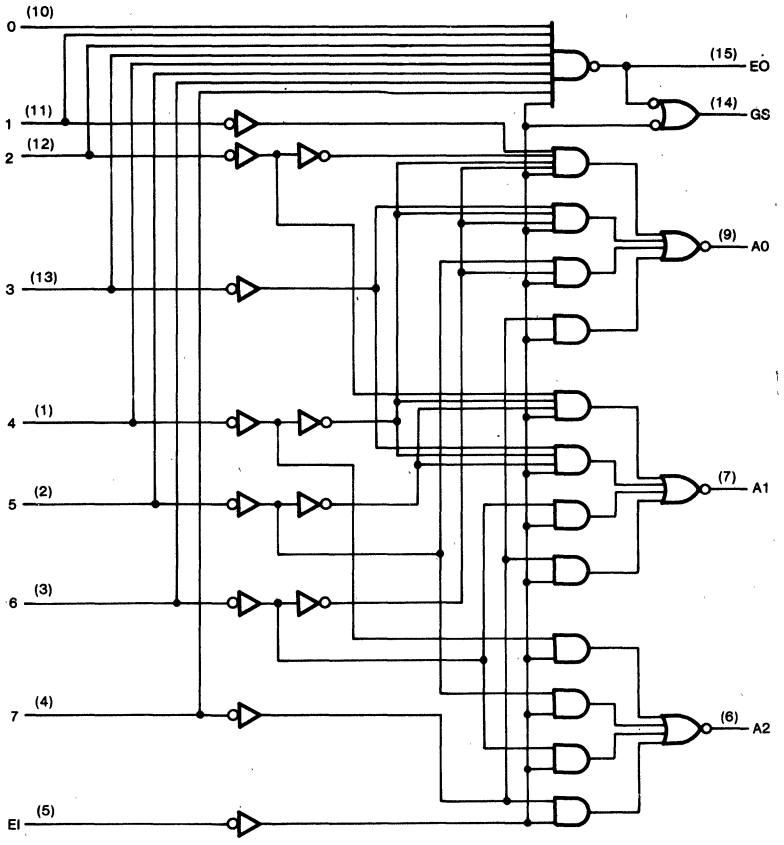
PIN CONFIGURATION



FUNCTION TABLE

Inputs									Outputs				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT148

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, 1-7 to A0, A1 or A2	t_{PLH}	C_L=50pF	10		17		20	ns
	t_{PHL}		10		17		20	
Propagation Delay, 0-7 to EO	t_{PLH}		11		18		22	ns
	t_{PHL}		11		18		22	
Propagation Delay, 0-7 to GS	t_{PLH}		14		24		29	ns
	t_{PHL}		14		24		29	
Propagation Delay, EI to A0, A1 or A2	t_{PLH}		10		16		19	ns
	t_{PHL}		10		16		19	
Propagation Delay, EI to GS	t_{PLH}		10		17		20	ns
	t_{PHL}		10		17		20	
Propagation Delay, EI to EO	t_{PLH}		11		18		22	ns
	t_{PHL}		11		18		22	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}		50					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Can perform as:**
  - **Boolean Function Generators**
  - **Parallel-to-Serial Converters**
  - **Data Source Selectors**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High drive currents outputs (I_{OL} =24 mA @ V_{OL} =0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

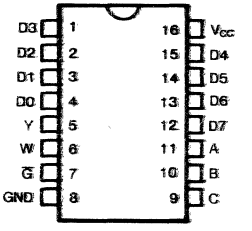
DESCRIPTION

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ($\overline{G}$) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
D0, D1 ... D7 = the level of the D respective input

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} . . . . . −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

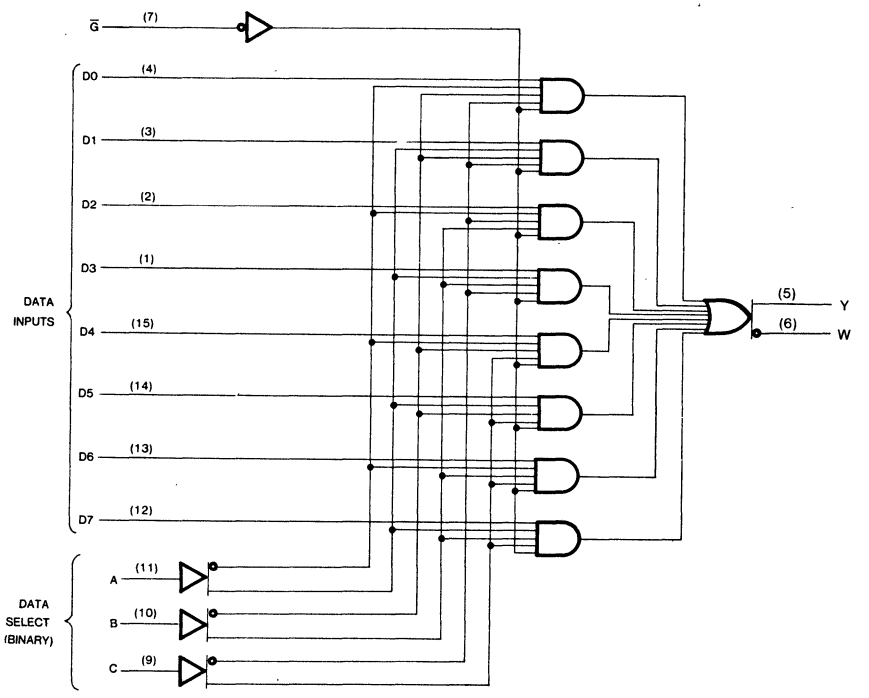
† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT151

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A, B or C to Y	t_{PLH}	$C_L = 50pF$	13		21		25	ns
		$C_L = 150pF$	16		26		31	
	t_{PHL}	$C_L = 50pF$	13		21		25	
		$C_L = 150pF$	16		26		31	
Propagation Delay, A, B or C to W	t_{PLH}	$C_L = 50pF$	15		24		27	ns
		$C_L = 150pF$	18		29		33	
	t_{PHL}	$C_L = 50pF$	15		24		27	
		$C_L = 150pF$	18		29		33	
Propagation Delay, Any D to Y	t_{PLH}	$C_L = 50pF$	9		15		18	ns
		$C_L = 150pF$	12		20		24	
	t_{PHL}	$C_L = 50pF$	9		15		18	
		$C_L = 150pF$	12		20		24	
Propagation Delay Any D to W	t_{PLH}	$C_L = 50pF$	8		15		18	ns
		$C_L = 150pF$	11		20		24	
	t_{PHL}	$C_L = 50pF$	8		15		18	
		$C_L = 150pF$	11		20		24	
Propagation Delay, $\overline{G}$ to Y	t_{PLH}	$C_L = 50pF$	12		19		23	ns
		$C_L = 150pF$	15		24		29	
	t_{PHL}	$C_L = 50pF$	12		19		23	
		$C_L = 150pF$	15		24		29	
Propagation Delay, $\overline{G}$ to W	t_{PLH}	$C_L = 50pF$	13		21		25	ns
		$C_L = 150pF$	16		26		31	
	t_{PHL}	$C_L = 50pF$	13		21		25	
		$C_L = 150pF$	16		26		31	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Allows Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N lines to n lines)**
- **'253 is the 3-State Version of this part**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High drive currents Outputs (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

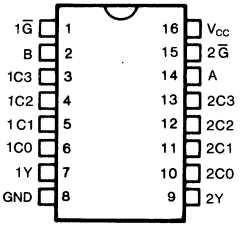
DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drives to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

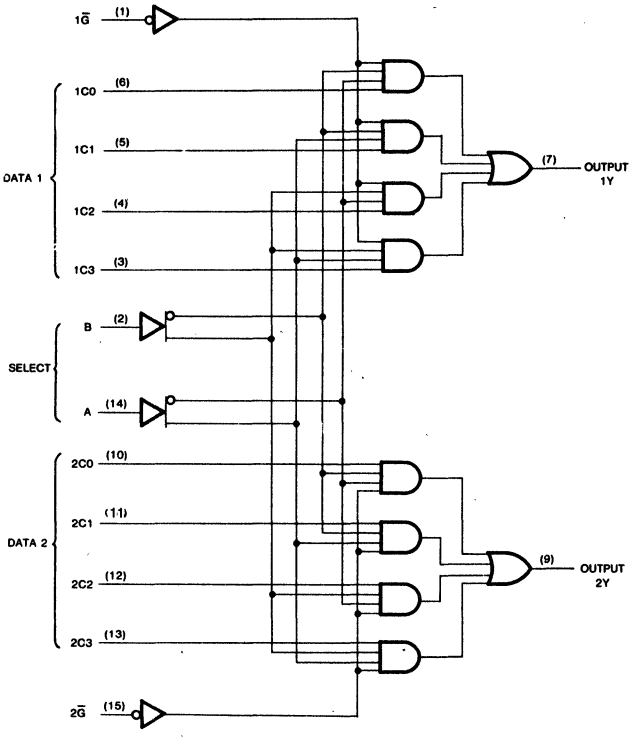


FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT153

Characteristic	Symbol	Conditions[1]	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to Y	t_{PLH}	C_L=50pF C_L=150pF	13 16		21 26		25 31	ns
	t_{PHL}	C_L=50pF C_L=150pF	13 16		21 26		25 31	
Propagation Delay, Data (Any C) to Y	t_{PLH}	C_L=50pF C_L=150pF	9 12		15 20		18 24	ns
	t_{PHL}	C_L=50pF C_L=150pF	9 12		15 20		18 24	
Propagation Delay, $\overline{G}$ to Y	t_{PLH}	C_L=50pF C_L=150pF	11 14		18 23		22 28	ns
	t_{PHL}	C_L=50pF C_L=150pF	11 14		18 23		22 28	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per package)						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs**
- **Performs the Demultiplexing Function by Distributing Data From One Input to Any One of 16 Outputs**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

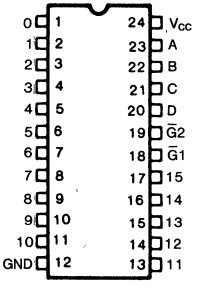
DESCRIPTION

These monolithic, 4-line to 16-line decoders decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs. $\overline{G}1$ and $\overline{G}2$, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are idenally suited for implementing high-performance memory decoders.

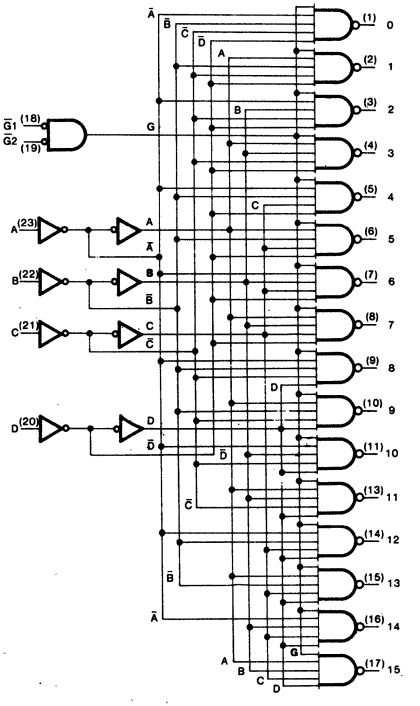
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inputs						Outputs														
$\overline{G1}$	$\overline{G2}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

4

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−8mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT154

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A, B, C, D to Any Output	t_{PLH}	C_L=50pF	12		20		24	ns
	t_{PHL}		12		20		24	
Propagation Delay, $\overline{G1}$ or $\overline{G2}$ to Any Output	t_{PLH}		12		20		24	ns
	t_{PHL}		12		20		24	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}		50					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Typical applications:**
  Dual 2-to-4 line decoder
  Dual 1-to-4 line demultiplexer
  3-to-8 line decoder
  1-to-8 line demultiplexer
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

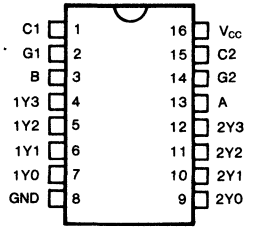
The '155 consists of two 1-to-4 line demultiplexers with independent strobes and common binary address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8 line decoder, or 1-to-8 line demultiplexer, without gating.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

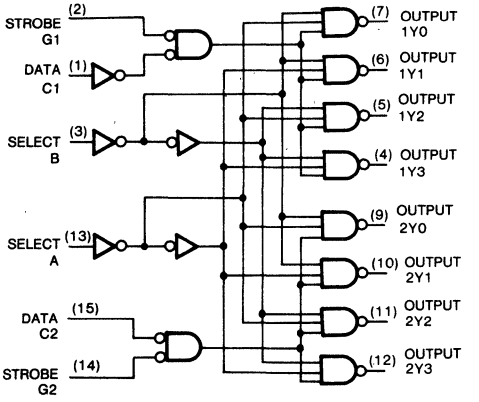
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

4

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLES

2-to-4 Line Decoder or 1-to-4 Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-to-8 Line Decoder or 1-to-8 Line Demultiplexer

Inputs		Outputs							
Select	Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
ICB A	IG	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X X X	H	H	H	H	H	H	H	H	H
L L L	L	L	H	H	H	H	H	H	H
L L H	L	H	L	H	H	H	H	H	H
L H L	L	H	H	L	H	H	H	H	H
L H H	L	H	H	H	L	H	H	H	H
H L L	L	H	H	H	H	L	H	H	H
H L H	L	H	H	H	H	H	L	H	H
H H L	L	H	H	H	H	H	H	L	H
H H H	L	H	H	H	H	H	H	H	L

IC = Inputs C1 and C2 connected together
IG = Inputs G1 and G2 connected together

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT155

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Maximum Propagation Delay, A, B, C2, G1 or G2 to any Output (2 levels of logic)	t_{PLH}	C_L=50pF	12		20		24	ns
	t_{PHL}		12		20		24	
Maximum Propagation Delay, A or B to any Y (3 levels of logic)	t_{PLH}		14		23		28	ns
	t_{PHL}		14		23		28	
Maximum Propagation Delay, C1 to any Y	t_{PLH}		13		22		26	ns
	t_{PHL}		13		22		26	
Maximum Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

4

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

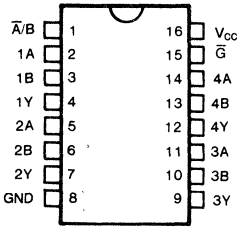
DESCRIPTION

These are data selectors multiplexers which select a 4-bit word from one of two sources via the control of a common select input ($\overline{A}$/B). A separate strobe input ($\overline{G}$) is provided. The '157 presents true data whereas the '158 presents inverted data at the outputs.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

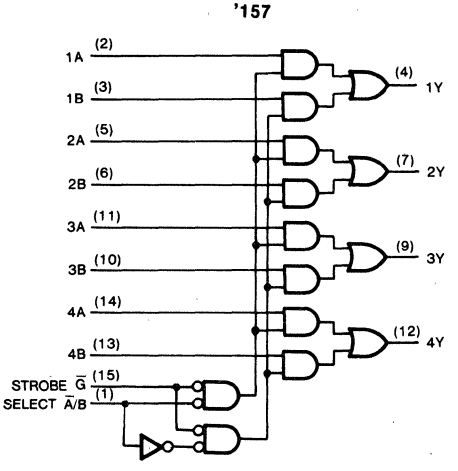
PIN CONFIGURATION

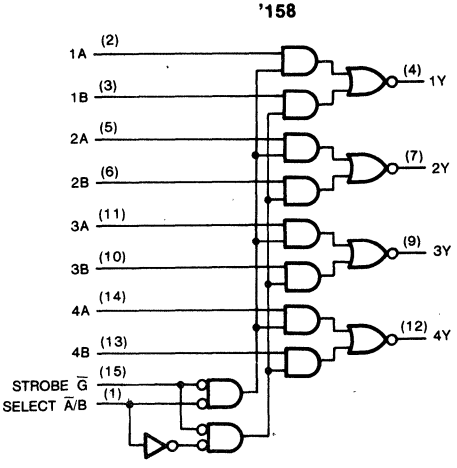


FUNCTION TABLE

Inputs				Output Y	
Strobe	Select	Data		'157	'158
$\overline{G}$	$\overline{A}$/B	A	B		
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT157, AHCT158

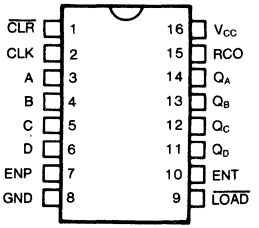
Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to Y	t_{PLH}	$C_L = 50pF$	9		14		18	ns
	t_{PHL}		9		14		18	
Propagation Delay, $\overline{A}$/B to Y	t_{PLH}		13		22		26	ns
	t_{PHL}		13		22		26	
Propagation Delay, $\overline{G}$ to Y	t_{PLH}		12		19		23	ns
	t_{PHL}		12		19		23	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Internal Look Ahead for Fast Counting**
- **Carry Output for n-bit cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74AHCT: −40°C to +85°C KS54AHCT: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



FUNCTION TABLES

'160, '161

CLK	$\overline{CLR}$	ENP	ENT	$\overline{LOAD}$	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

'162, '163

CLK	$\overline{CLR}$	ENP	ENT	$\overline{LOAD}$	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment counter

DESCRIPTION

These are synchronous, presettable 4-bit binary counters featuring internal carry-look-ahead for high-speed counting. The '160 and '162 are decade counters, and the '161 and '163 are 4-bit binary counters. The buffered clock input triggers all flip-flops simultaneously on the rising edge of the input waveform. This eliminates the output counting spikes normally associated with asynchronous counters.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs.

The clear function for the '162 and 163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter.

Two enable inputs and a ripple carry output allow easy cascading of the counters. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

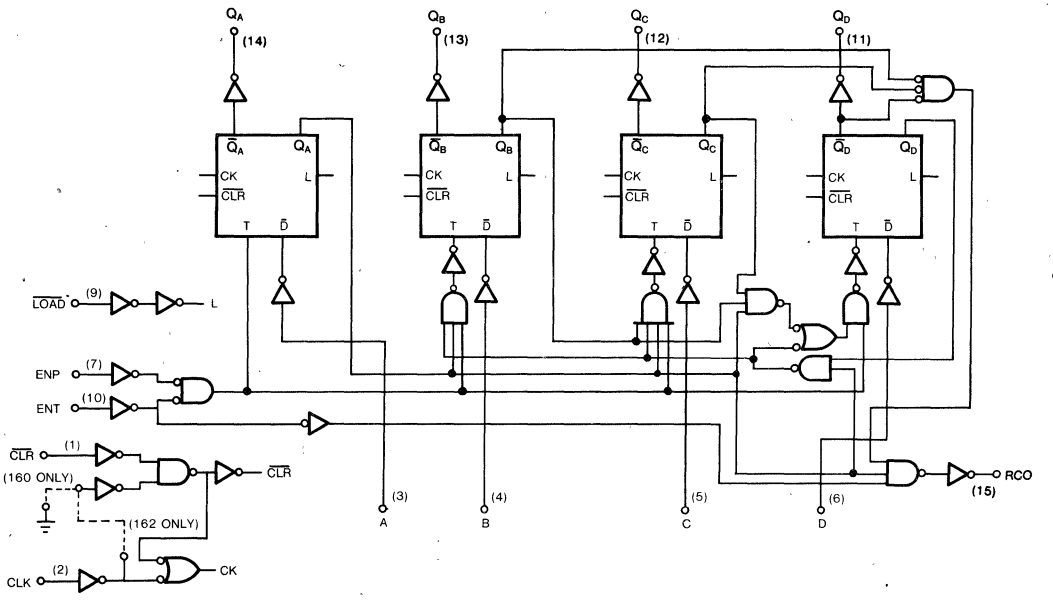
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that will modify the operating model have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

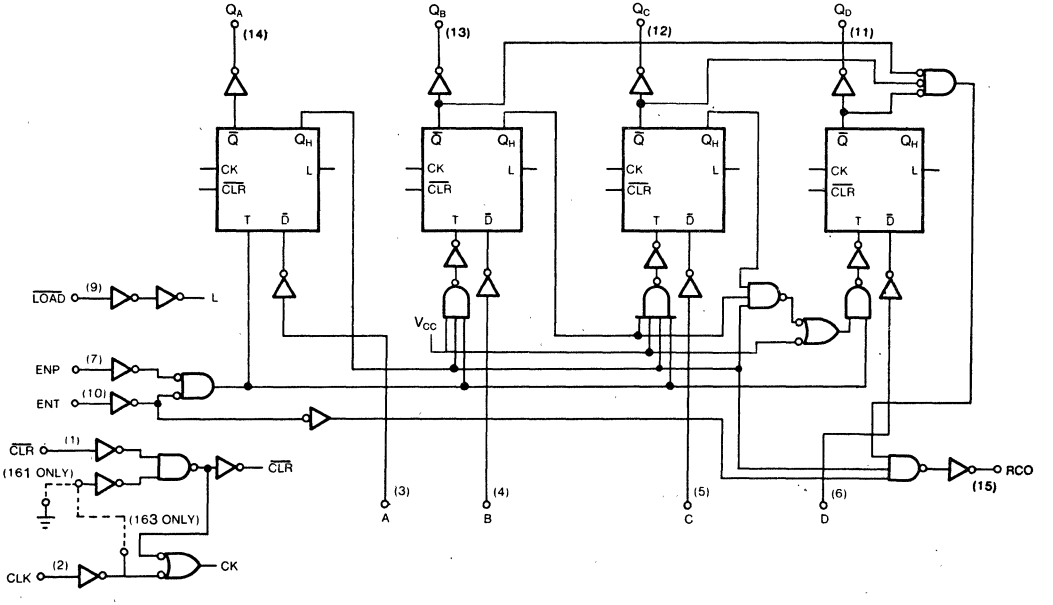
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAMS

'160 or '162

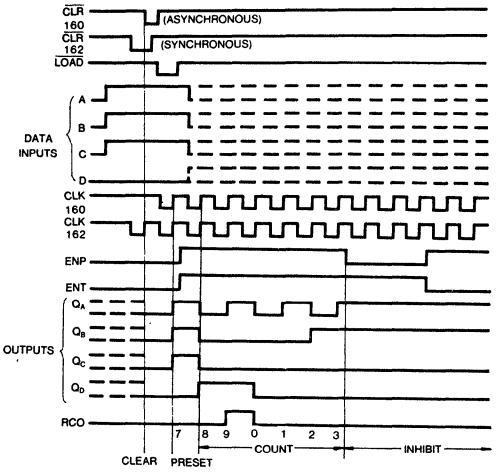


'161 or '163



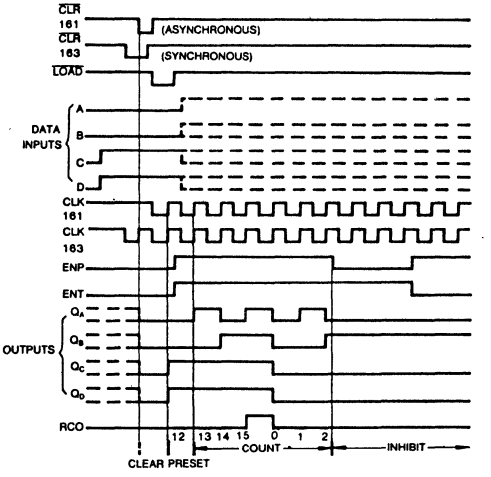
Typical Clear, Preset, Count and Inhibit Sequences

'160 and '162



Sequence:
(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

'161 and '163



Sequence:
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one and two
(4) Inhibit

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT160, AHCT161

Characteristic		Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	C_L=50pF	50	40		35		MHz
Propagation Delay, CLK to RCO		t_{PLH}		15		20		24	ns
		t_{PHL}		15		20		24	
Propagation Delay, CLK to any Q		t_{PLH}		10		16		19	ns
		t_{PHL}		10		16		19	
Propagation Delay, ENT to RCO		t_{PLH}		8		13		16	ns
		t_{PHL}		8		13		16	
Propagation Delay, $\overline{CLR}$ to any Q		t_{PHL}		15		24		29	ns
Propagation Delay, $\overline{CLR}$ to RCO		t_{PHL}		17		23		33	ns
Pulse Width	CLK High or Low	t_w		10	15		20		ns
	$\overline{CLR}$ Low			10	15		20		
Setup Time before CLK↑	A, B, C, D	t_{su}		10	15		20		ns
	$\overline{LOAD}$			10	15		20		
	ENP, ENT			10	15		20		
	$\overline{CLR}$ inactive			6	10		10		
Hold time, All Synchronous Inputs after CLK↑		t_h		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		80					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT162, AHCT163

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	50	40		35		MHz
Propagation Delay, CLK to RCO		t_{PLH}		15		20		24	ns
		t_{PHL}		15		20		24	
Propagation Delay, CLK to any Q		t_{PLH}		10		16		20	ns
		t_{PHL}		10		16		20	
Propagation Delay, ENT to RCO		t_{PLH}		9		15		18	ns
		t_{PHL}		9		15		18	
Pulse Width, CLK High or Low		t_w		8	12.5		20		ns
Setup Time before CLK↑	A, B, C, D	t_{su}		10	15		20		ns
	$\overline{LOAD}$			10	15		20		
	ENP, ENT			15	15		20		
	$\overline{CLR}$ inactive			6	10		10		
	$\overline{CLR}$ Low			6	15		20		
Hold time, All Synchronous Inputs after CLK↑		t_h		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		80					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

FEATURES

- **AND—Gated (enable/disable) serial inputs**
- **Fully buffered clock and serial inputs**
- **Direct clear**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

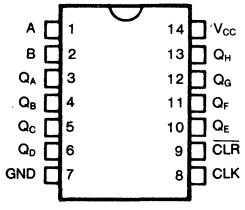
These are high-speed 8-bit registers with AND-gated serial inputs and an asynchronous clear. Data is entered serially through either one of the two inputs, A and B. A high on one input enables the other one, which will then determine the state of the first flip-flop. A low at either or both inputs inhibits data entry and resets the first flip-flop to a low level at the next positive clock transition.

Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of their clock input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

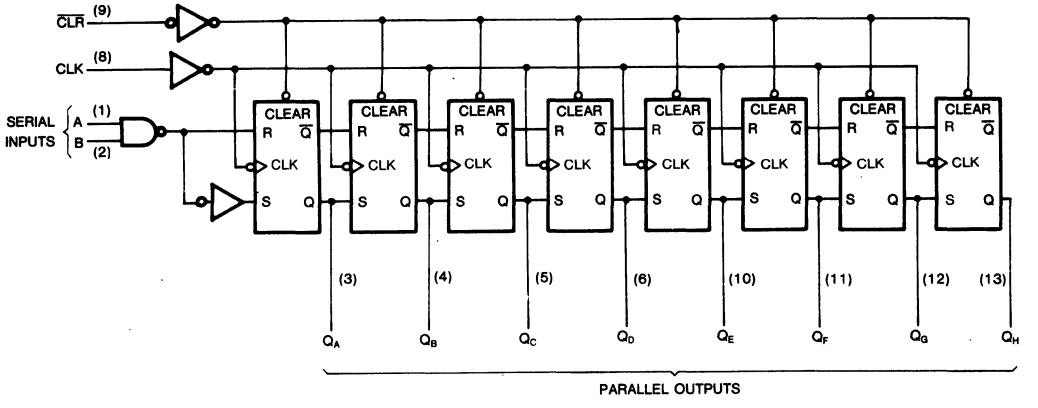


FUNCTION TABLE

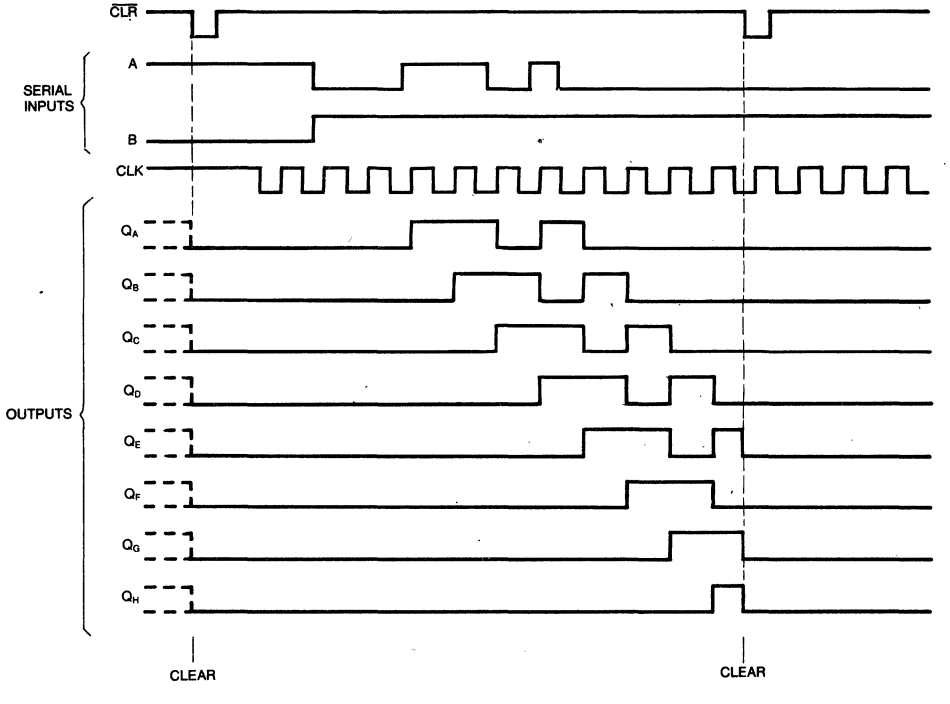
Inputs				Outputs		
$\overline{CLR}$	CLK	A	B	Q_A	Q_B . . . Q_H	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B or Q_H, respectively, before the indicate steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

LOGIC DIAGRAMS



Typical Clear, Shift, and Clear Sequences



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	* 0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT164

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	60	36		30		MHz
Propagation Delay, $\overline{CLR}$ to any Q		t_{PHL}		12		20		24	ns
Propagation Delay, CLK to any Q		t_{PLH}		11		18		21	ns
		t_{PHL}		11		18		21	
Pulse Width	$\overline{CLR}$ Low	t_w		8	12		15		ns
	CLK High or Low			8	12		15		
Setup Time before CLK↑	Data	t_{su}		8	12		15		ns
	$\overline{CLR}$ Inactive			8	12		15		
Hold Time Data after CLK↑		t_h		1	4		5	6	ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per package)	120					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

FEATURES

- **Complementary outputs**
- **Direct overriding load (data) inputs**
- **Gated clock inputs**
- **Parallel-to-Serial data conversion**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

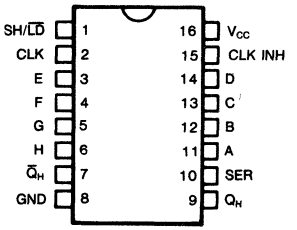
These are high-speed 8-bit parallel-load or serial-in shift registers with complementary serial outputs available from the last stage. Parallel-in access is asynchronous and is enabled by pulling the SH/$\overline{LD}$ input low. When SH/$\overline{LD}$ is high, data is entered serially at the SER input and shifted one place to the right with each positive clock transition.

Clocking is accomplished through a 2-input NOR gate which permits one of the clocks to be used as a clock inhibit function. Holding either clock input high inhibits clocking. Either clock input is enabled by holding the other clock input low while the SH/$\overline{LD}$ input is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

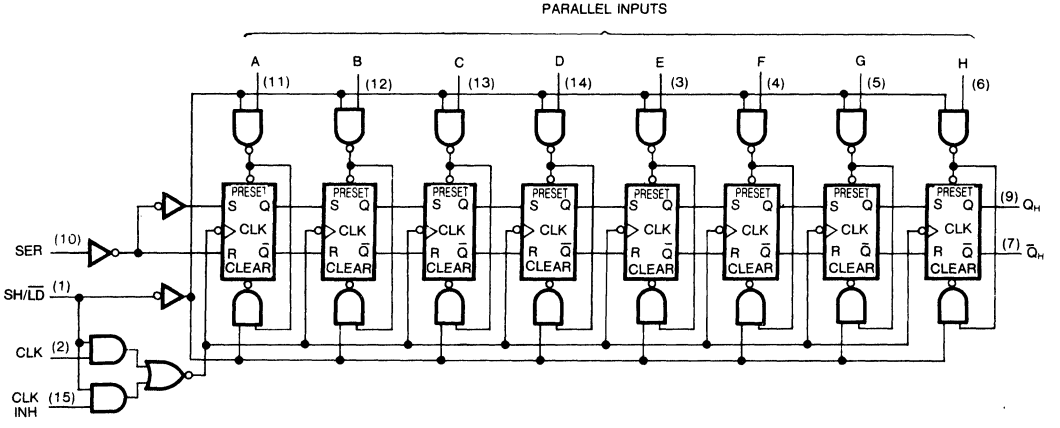


FUNCTION TABLE

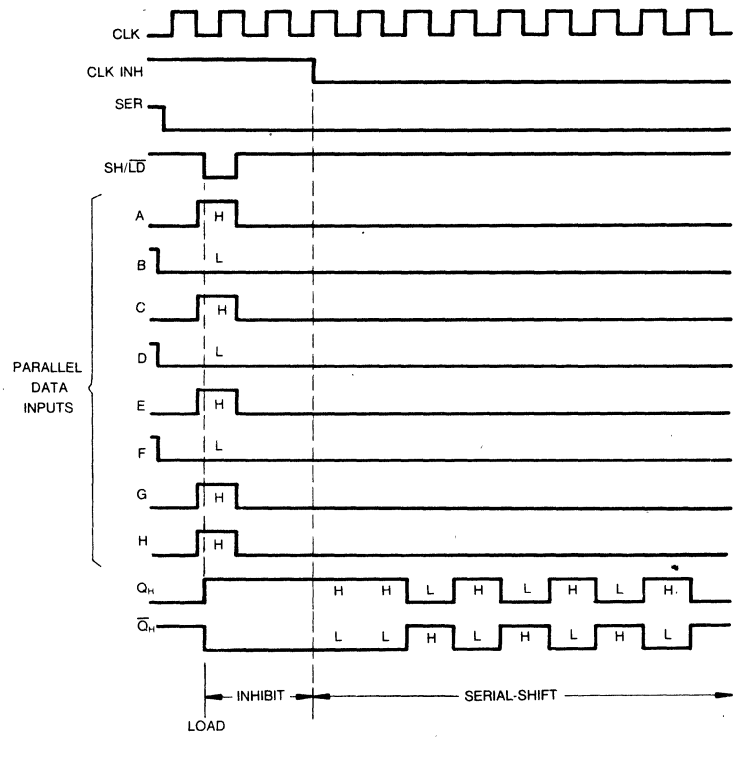
Inputs			Function
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	PARALLEL LOAD
H	H	X	NO CHANGE
H	X	H	NO CHANGE
H	L	↑	SHIFT*
H	↑	L	SHIFT*

*Content of each internal register shifts toward output Q_H. Data at serial input is shifted into first register.

LOGIC DIAGRAMS



Typical Shift, Load and Inhibit Sequences



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT165

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	50	30		25		MHz
Propagation Delay, SH/$\overline{LD}$ to Q_H or $\overline{Q}_H$		t_{PLH}		15		25		30	ns
		t_{PHL}		15		25		30	
Propagation Delay, CLK to Q_H or $\overline{Q}_H$		t_{PLH}		19		31		37	ns
		t_{PHL}		19		31		37	
Propagation Delay, H to Q_H or $\overline{Q}_H$		t_{PLH}		12		20		24	ns
		t_{PHL}		12		20		24	
Pulse Width	SH/$\overline{LD}$ Low	t_W		8	12		15		ns
	CLK High or Low			8	12		15		
Setup Time	SH/$\overline{LD}$ High before CLK↑	t_{SU}		7	15		20		
	SER before CLK↑			8	12		15		
	CLK INH Low before CLK↑			7	15		20		ns
	CLK INH High before CLK↓			7	15		20		
	Data before SH/$\overline{LD}$↑			5	8		10		
Hold Time	SER Data after CLK↑	t_h		−3	0		0		ns
	PAR Data after SH/$\overline{LD}$↑			−3	0		0		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		100					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

8-Bit Parallel-In/Serial-Out Shift Registers with Clear

FEATURES

- **Synchronous load**
- **Direct overriding clear**
- **Parallel to serial conversion**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

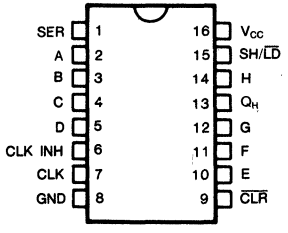
These devices feature parallel-in or serial-in, serial-out registers, gated clock inputs and an overriding clear input.

The paralled-in or serial-in modes are established by the shift/load input. When high, the input enables the serial data input and couples the eight fill-flops for serial shifting with each clock pulse. When low, the paralled data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

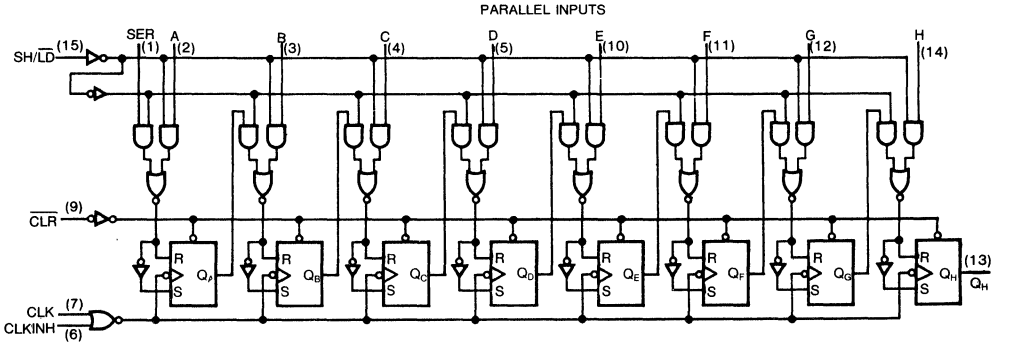
PIN CONFIGURATION



FUNCTION TABLE

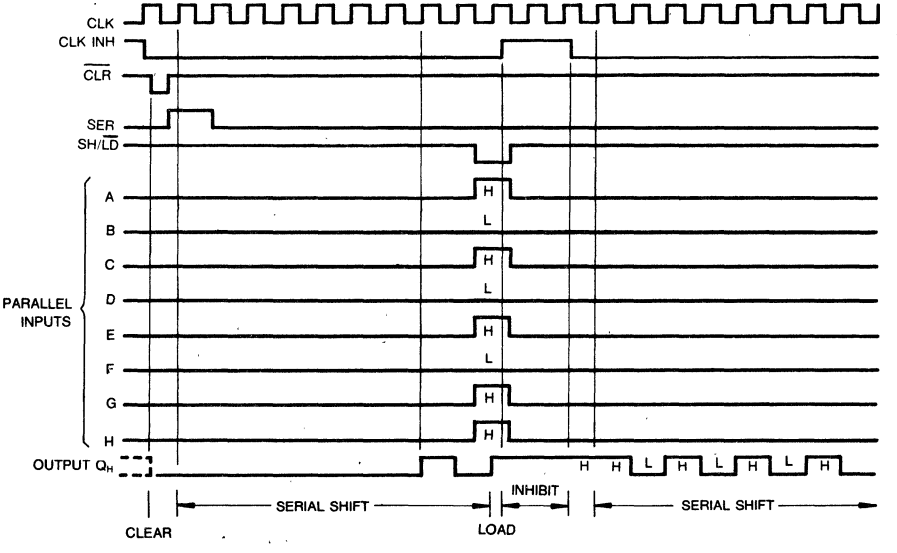
Inputs						Internal Outputs		Output
$\overline{CLR}$	SH/$\overline{LD}$	CLK INH	CLK	SER	Parallel A ... H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a ... h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	G_{A0}	Q_{B0}	Q_{H0}

LOGIC DIAGRAM



4

Typical Clear, Shift, Load, Inhibit, and Shift Sequences



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT166

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	60	36		30		MHz
Propagation Delay, $\overline{CLR}$ to Q_H		t_{PHL}		10		17		20	ns
Propagation Delay, CLK to Q_H		t_{PLH}		13		21		25	ns
		t_{PHL}		13		21		25	
Pulse Width	$\overline{CLR}$ Low	t_w		8	12		15		ns
	CLK High or Low			8	12		15		
Setup Time	SH/$\overline{LD}$ High before CLK↑	t_{su}		8	12		15		ns
	SER before CLK↑			8	12		15		
	CLK INH before before CLK↑			8	12		15		
	Data before SH/$\overline{LD}$↑			8	12		15		
	$\overline{CLR}$ Inactive before CLK			8	12		15		
Hold Time	SH/$\overline{LD}$ High after CLK↑	t_h		5	8		10		ns
	SER after CLK↑			5	8		10		
	CLK INH after CLK↑			5	8		10		
	Data after SH/$\overline{LD}$↑			5	8		10		
	$\overline{CLR}$ Active after CLK↑			5	8		10		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

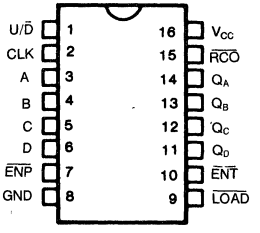
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

FEATURES

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look Ahead for Fast Counting**
- **Carry Output for N-bit Cascading**
- **Fully Independent Clock Circuit**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The '168 is a decade counter and the '169 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the U/$\overline{D}$ input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The ripple carry output ($\overline{RCO}$) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transition at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input.

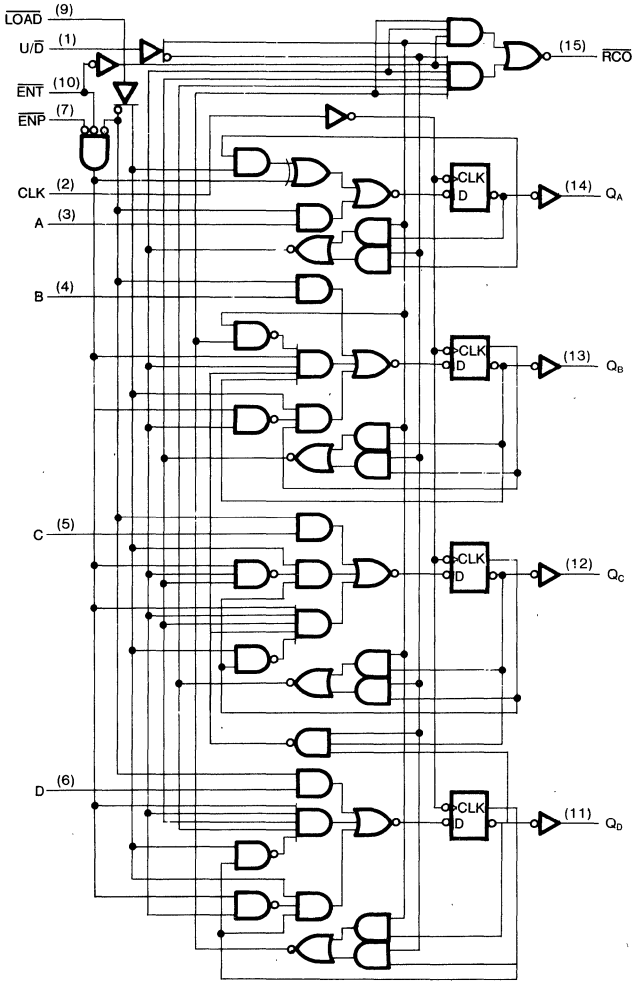
These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

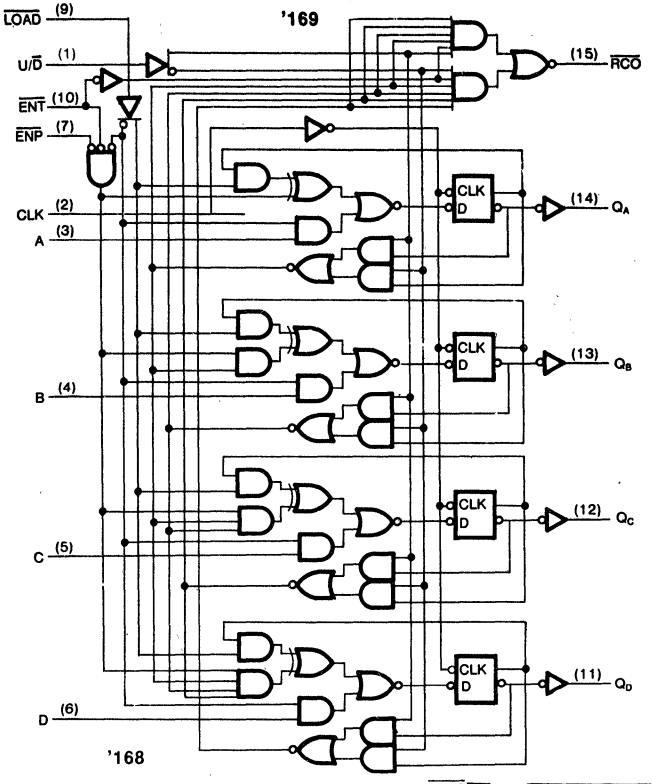
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

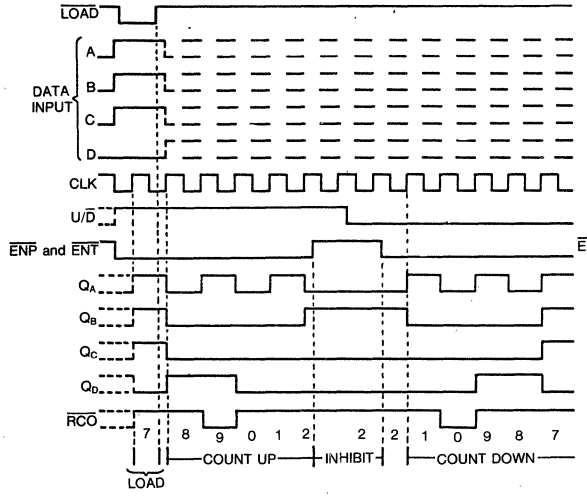
LOGIC DIAGRAMS

'168



LOGIC DIAGRAMS (continued)

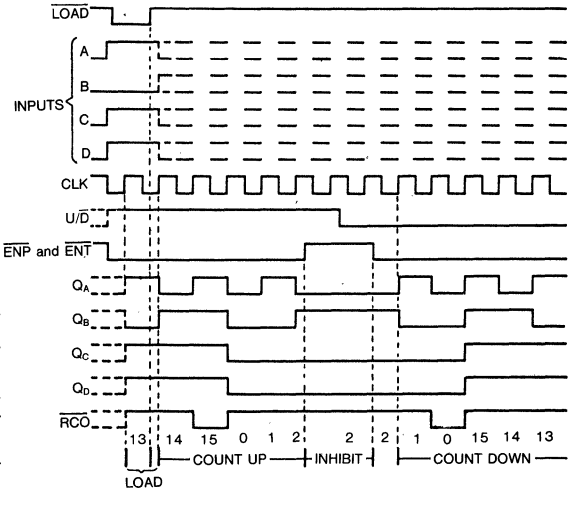




Illstrated above is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

'169



Illstrated above is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CLK	U/$\overline{D}$	$\overline{ENP}$	$\overline{ENT}$	$\overline{LOAD}$	D_n	Q_n	$\overline{RCO}$
Parallel Load	↑	X	X	X	l	i	L	(1)
	↑	X	X	X	i	h	H	(1)
Count Up	↑	h	l	l	h	X	Count Up	(1)
Count Down	↑	l	l	l	h	X	Count Down	(1)
Hold	↑	X	h	X	h	X	q_n	(1)
	↑	X	X	h	h	X	q_n	H

H=HIGH voltage level steady state
h=HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L=LOW voltage level steady state
l=LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X=Don't care
q=Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
↑=LOW-to-HIGH clock transition

NOTE:

1. The $\overline{RCO}$ is LOW when $\overline{ENT}$ is LOW and the counter is at Terminal Count Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169.
   The $\overline{RCO}$ is LOW when $\overline{ENT}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168.

4

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O= −4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT168, AHCT169

Characteristic		Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
				Typ	Min	Max	Min	Max	
Maximum Operating Frequency		f_{max}	C_L=50pF	50	30		25		MHz
Propagation Delay, CLK to $\overline{RCO}$		t_{PLH}		19		28		32	ns
		t_{PHL}		19		28		32	
Propagation Delay, CLK to Any Q		t_{PLH}		12		18		22	ns
		t_{PHL}		12		18		22	
Propagation Delay, $\overline{ENT}$ to $\overline{RCO}$		t_{PLH}		10		16		19	ns
		t_{PHL}		10		16		19	
Propagation Delay, U/$\overline{D}$ to $\overline{RCO}$		t_{PLH}		14		23		25	ns
		t_{PHL}		14		23		25	
Pulse Duration, CLK high or low		t_w		10	16		20		ns
Setup Time, Before CLK↑	A, B, C or D			9	15		20		ns
	$\overline{ENP}$ or $\overline{ENT}$			12	20		25		
	$\overline{LOAD}$			9	15		20		
	U/$\overline{D}$			9	15		20		
Hold Time, Data after CLK↑		t_h		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Gated output control lines for enabling or disabling the outputs**
- **Fully independent clock for operation in parallel-load or hold modes**
- **For application as bus buffer registers**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 24 mA @ V_{OL} = 0.5V for direct bus interface
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

These 4-bit registers contain D-type flip-flops with 3-state outputs, capable of driving highly-capacitive or low-impedance loads. This provides the device with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gated output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

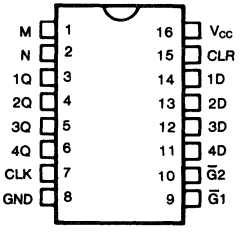
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

4

PIN CONFIGURATION

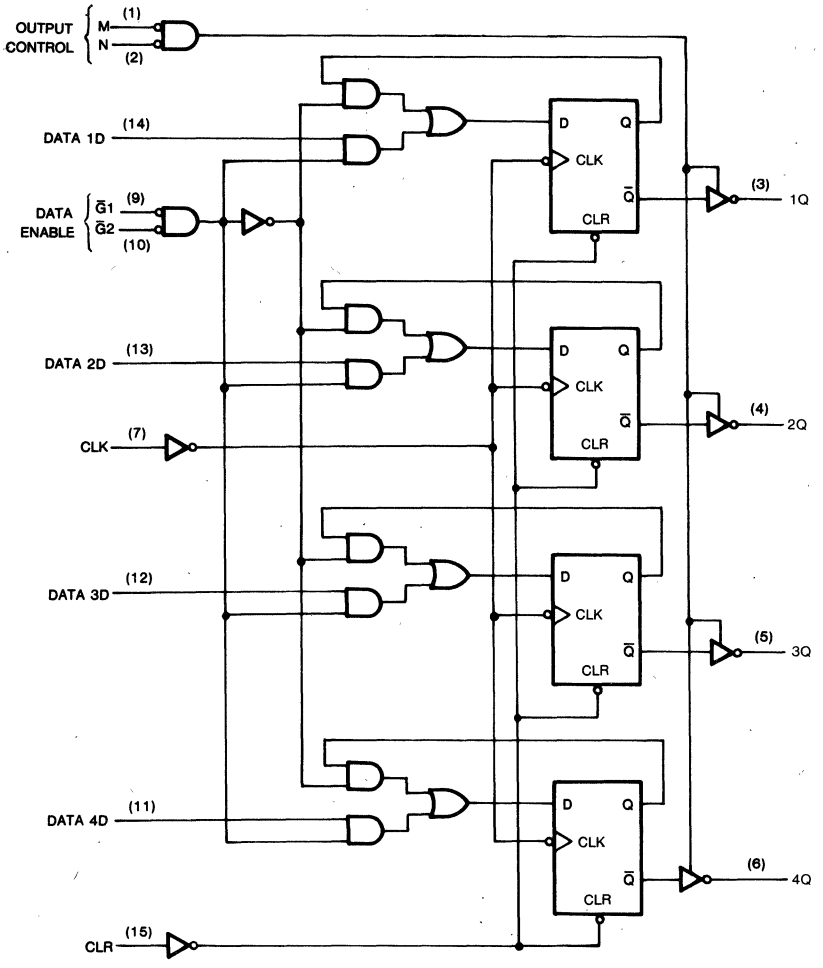


FUNCTION TABLE

Input					Output
CLR	CLK	Data Enable		Data	Q
		$\overline{G1}$	$\overline{G2}$	D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT173

Characteristic		Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
					Typ*	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}			50	30		25		MHz
Propagation Delay, CLK to any Q		t_{PLH}	$C_L = 50pF$ $C_L = 150pF$		13 16		21 26		25 31	ns
		t_{PHL}	$C_L = 50pF$ $C_L = 150pF$		13 16		21 26		25 31	
Propagation Delay, CLR to any Q		t_{PHL}	$C_L = 50pF$ $C_L = 150pF$		15 18		25 30		30 36	ns
Output Enable Time, M or N to any Q		t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$ $C_L = 150pF$	12 15		20 25		24 30	ns
		t_{PZL}		$C_L = 50pF$ $C_L = 150pF$	12 15		20 25		24 30	
Output Disable Time, M or N to any Q		t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$		10		17		20	ns
		t_{PLZ}			10		17		20	
Pulse Width	CLK High or Low	t_w			7	12		15		ns
	CLR High				7	12		15		
Setup Time, before CLK↑	$\overline{G}1$ and $\overline{G}2$	t_{su}			8	15		20		ns
	Data				7	12		15		
	CLR Inactive				7	12		15		
Hold Time After CLK↑	$\overline{G}1$ and $\overline{G}2$	t_h			−3	0		0		ns
	Data				−3	0		0		
Input Capacitance		C_{IN}			5					pF
Output Cipacitance		C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance*		C_{PD}								pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Hex/Quad D-type Flip-Flops with Clear

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '174 contains six, and the '175 contains four D-type filp-flops all sharing a common clock and a common clear. The '174 features single nail outputs for every flip-flops whereas the '175 has complementary outputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

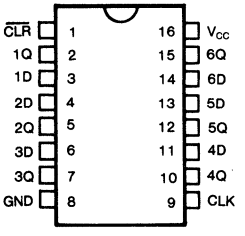
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

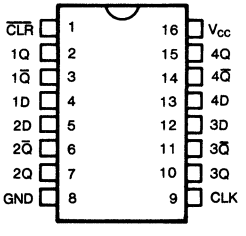
4

PIN CONFIGURATIONS

'174



'175



FUNCTION TABLE

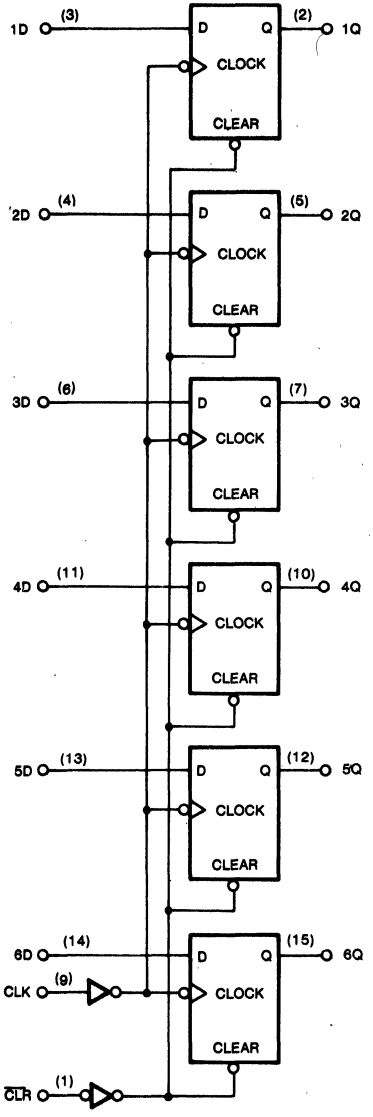
(Each Flip-Flop)

Inputs			Outputs	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

† '175 only

LOGIC DIAGRAMS

'174



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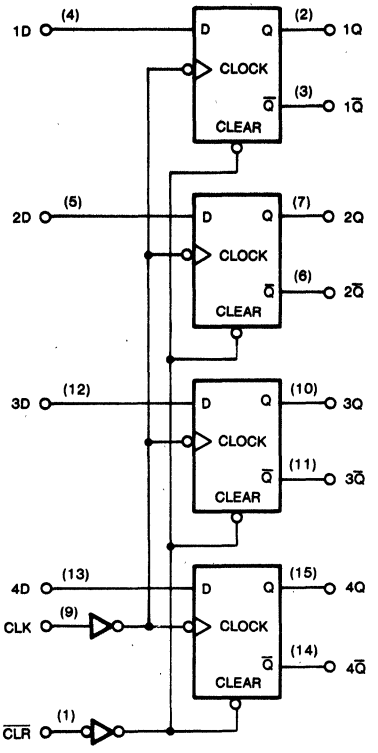


Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT174, AHCT175

Characteristic		Symbol	Conditions†	$T_A=25°C$ $V_{CC}=5.0V$	KS74AHCT $T_A=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54AHCT $T_A=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L=50pF$	70	50		40		MHz
Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		11		17		20	ns
		t_{PHL}		11		17		20	
Propagation Delay, $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		12		21		25	ns
		t_{PHL}		12		21		25	
Setup Time before CLK↑	Data	t_{su}		6	10		15		ns
	$\overline{CLR}$ Inactive			4	6		8		
Hold Time, Data after CLK↑		t_h		−3	0		0		ns
Pulse Width	CLK High or Low	t_w		6	10		15		ns
	$\overline{CLR}$ Low			6	10		15		
Input Capacitace		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

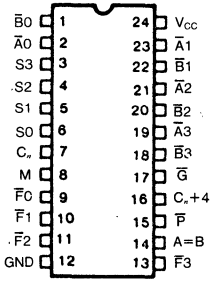
Arithmetic Logic Unit/ Function Generator

Preliminary Specifications

FEATURES

- **Arithmetic operating modes:**
  - **Addition**
  - **Subtraction**
  - **Shift operand A one position**
  - **Magnitude comparison**
  - **Plus 12 other arithmetic operations**
- **Logic function modes:**
  - **Exclusive-OR**
  - **Comparator**
  - **AND, NAND, OR, NOR**
  - **Plus 10 other logic operations**
- **Full look-ahead for high-speed operations on long words**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current Outputs:** I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

The '181 is an Arithmetic Logic Unit (ALU)/Function Generator that performs 16 binary arithmetic operations on two 4-bit words as shown in table 1 and 2. These operations are selected by the four functions select lines (S0, S1, S2, S3) and include addition, subtraction, decrement and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low level voltage to the mode control input(M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of 2 cascade-outputs ($\overline{P}$ and $\overline{G}$) for the 4-bits in the package. When used in conjunction with AHCT182, high-speed arithmetic operation can be performed. The typical addition times shown in table below illustrates how little is required for addition of longer words when full carry look-ahead is employed.

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small lengths can be performed without external circuitry.

The '181 will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires and end-around or forced carry to provide A-B.

The '181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of the equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with C_n=H when performing the comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subract mode by placing the function select input S3, S2, S1, S0 at L,H,H,L respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two boolean variables without the use of external circuitry. These logical functions are selected by use of the four function select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry.

The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, OR and NOR functions.

Pin number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low Data (Table1)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_n+4	$\overline{P}$	$\overline{G}$
Active-High Data (Table 2)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_n$+4	X	Y

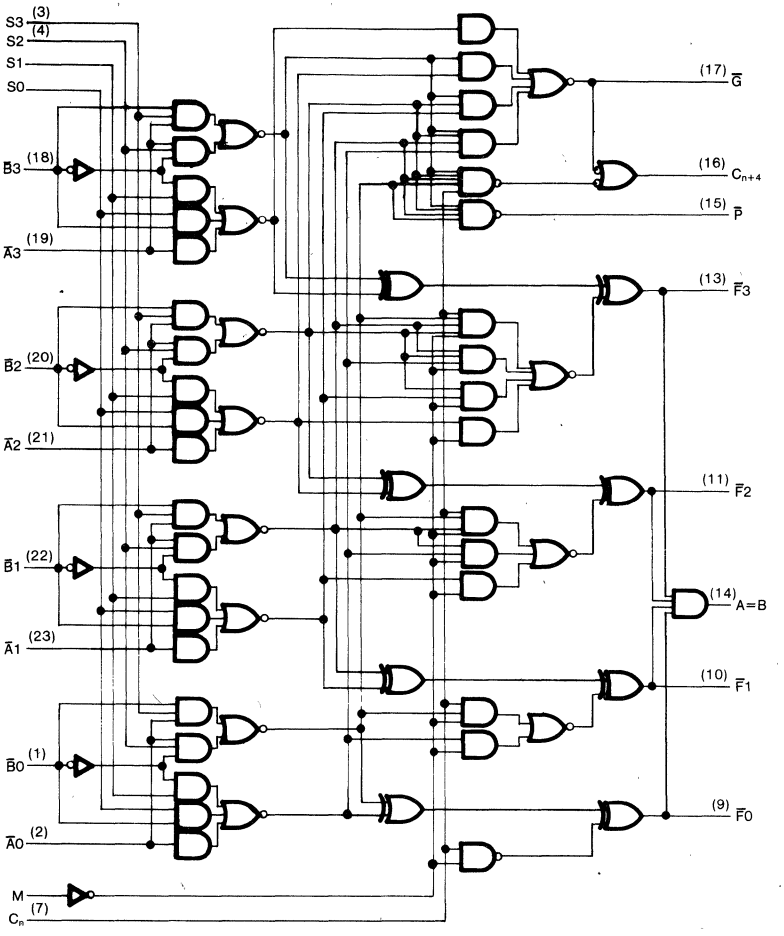
ALU SIGNAL DESIGNATION

The '181 can be used with the signal designations. The logic functions and arithmetc operations obtained with signal designations as in Table 1.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



○ **Table 1**

Selection				Active-Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n=L (no carry)	C_n=H (with carry)
L	L	L	L	F=$\overline{A}$	F=A Minus 1	F=A
L	L	L	H	F=$\overline{AB}$	F=AB Minus 1	F=AB
L	L	H	L	F=$\overline{A}$ + B	F=A$\overline{B}$ Minus 1	F=A$\overline{B}$
L	L	H	H	F=1	F=Minus 1 (2's Comp)	F=Zero
L	H	L	L	F=$\overline{A + B}$	F=A Plus (A + $\overline{B}$)	F=A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F=$\overline{B}$	F=AB Plus (A + $\overline{B}$)	F=AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F=$\overline{A \oplus B}$	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	F=A + $\overline{B}$	F=A + $\overline{B}$	F=(A + $\overline{B}$) Plus 1
H	L	L	L	F=$\overline{A}$B	F=A Plus (A + B)	F=A Plus (A + B) Plus 1
H	L	L	H	F=A ⊕ B	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F=A$\overline{B}$ Plus (A + B)	F=A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F=A + B	F=(A + B)	F=(A + B) Plus 1
H	H	L	L	F=0	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	F=A$\overline{B}$	F=AB Plus A	F=AB Plus A Plus 1
H	H	H	L	F=AB	F=A$\overline{B}$ Plus A	F=A$\overline{B}$ Plus A Plus 1
H	H	H	H	F=A	F=A	F=A Plus 1

○ **Table 2**

Selection				Active-High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	$\overline{C}_n$=L (no carry)	$\overline{C}_n$=H (with carry)
L	L	L	L	F=$\overline{A}$	F=A	F=A Plus 1
L	L	L	H	F=$\overline{A + B}$	F=A + B	F=(A + B) Plus 1
L	L	H	L	F=$\overline{A}$B	F=A + $\overline{B}$	F=(A + $\overline{B}$) Plus 1
L	L	H	H	F=0	F=Minus 1 (2's Comp)	F=Zero
L	H	L	L	F=$\overline{AB}$	F=A Plus A$\overline{B}$	F=A Plus A$\overline{B}$ Plus 1
L	H	L	H	F=$\overline{B}$	F=(A + B) Plus A$\overline{B}$	F=(A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F=$\overline{A \oplus B}$	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	F=A$\overline{B}$	F=A$\overline{B}$ Minus 1	F=A$\overline{B}$
H	L	L	L	F=$\overline{A}$ + B	F=A Plus AB	F=A Plus AB Plus 1
H	L	L	H	F=$\overline{A \oplus B}$	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F=(A + $\overline{B}$) Plus AB	F=(A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F=AB	F=AB Minus 1	F=AB
H	H	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	F=A + $\overline{B}$	F=(A + B) Plus A	A=(A + B) Plus A Plus 1
H	H	H	L	F=A + B	F=(A + $\overline{B}$) Plus A	F=(A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F=A	F=A Minus 1	F=A

* Each bit is shifted to the next more significant position

4

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

INPUT PAIRS HIGH/NOT HIGH TEST TABLE
FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$	In-Phase
t_{PHL} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	C_n+4	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_n+4	Out-of-Phase

PARAMETER MEASUREMENT INFORMATION

$\overline{SUM}$ MODE TEST TABLE
FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phone
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_n+4	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_n+4	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_n+4	Out-of-Phase

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT181

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
		$C_L = 50pF$	Typ	Min	Max	Min	Max	
Propagation Delay, C_n to C_{n+4}	t_{PLH}	M=0V, $\overline{\text{Sum}}$ or $\overline{\text{Diff}}$ Mode	8		14		17	ns
	t_{PHL}		8		14		17	
Propagation Delay, $\overline{A}$ or $\overline{B}$ to C_{n+4}	t_{PLH}	M=S1=S2=0V S0=S3=4.5V	16		24		29	ns
	t_{PHL}		16		24		29	
Propagation Delay, $\overline{A}$ or $\overline{B}$ to C_{n+4}	T_{PLH}	M=S0=S3=0V S1=S2=4.5V	17		25		30	ns
	t_{PHL}		17		25		30	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$	t_{PLH}	M=S1=S2=0V S0=S3=4.5V	17		25		30	ns
	t_{PHL}		17		25		30	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$	t_{PLH}	M=S0=S3=0V S1=S2=4.5V	17		25		30	ns
	t_{PHL}		17		25		30	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$	t_{PLH}	M=S0=S3=0V S1=S2=4.5V	15		23		27	ns
	t_{PHL}		15		23		27	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$	t_{PLH}	M=S1=S2=0V S0=S3=4.5V	16		24		29	ns
	t_{PHL}		16		24		29	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F_i}$	t_{PLH}	M=S1=S2=0V S0=S3=4.5V	20		29		35	ns
	t_{PHL}		20		29		35	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F_i}$	t_{PLH}	M=S0=S3=0V S1=S2=4.5V	19		27		32	ns
	t_{PHL}		19		27		32	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F_i}$	t_{PLH}	M=4.5V	16		24		29	ns
	t_{PHL}		16		24		29	
Propagation Delay $\overline{A}$ or $\overline{B}$ to A=B	t_{PLZ}	M=S0=S3=0V S1=S2=4.5V	19		27		32	ns
	t_{PZL}		16		24		29	
Propagation Delay C_n to any $\overline{F}$	t_{PLH}		15		23		24	ns
	t_{PHL}		15		23		27	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase

INPUT BITS EQUAL/NOT EQUAL TEST TABLE
FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_n+4	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_n+4	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_n+4	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_n+4	Out-of Phase

4

$\overline{DIFF}$ MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A=B	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A=B	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_n+4 or any $\overline{F}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_n+4	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_n+4	In-Phase

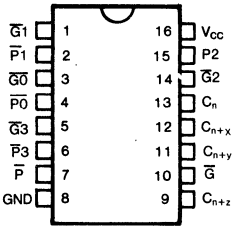
Look Ahead Carry Generator

FEATURES

- **Compatible Carry Functions for direct ALU connection**
- **Cascadable to perform look-ahead across n-bit adders.**
- **High output current drive: I_{OL} = 8mA @ V_{OL} = 0.5V**
- **Low power consumption characteristic of CMOS**
- **Direct interface capability to TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**

  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

The '182 is a high-speed, look-ahead carry generator, capable of anticipating a carry across four binary adders or group of adders. These devices can be cascaded to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjuction with the AHCT181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each 182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true from, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the 182 are:

$$Cn+x = G0 + P0\ Cn$$
$$Cn+y = G1 + P1\ G0 + P1\ P0\ Cn$$
$$Cn+z = G2 + P2\ G1 + P2\ P1\ G0 + P2\ P1\ P0\ Cn$$
$$\overline{G} = \overline{G3 + P3\ G2 + P3\ P2\ G1 + P3\ P2\ P1\ G0}$$
$$\overline{P} = \overline{P3\ P2\ P1\ P0}$$

PIN DESIGNATIONS

Designation	Pin No	Function
$\overline{G0}$,$\overline{G1}$,$\overline{G2}$,$\overline{G3}$	3,1,14,5	Active Low Carry Generate Inputs
$\overline{P0}$,$\overline{P1}$,$\overline{P2}$,$\overline{P3}$	4,2,15,6	Active Low Carry Propagate Inputs
Cn	13	Carry Input, Active HIGH
Cn+x, Cn+y, Cn+z	12,11,9	Carry Outputs
$\overline{G}$	10	Active Low Carry Generate Output
$\overline{P}$	7	Active Low Carry Propagae Output
V_{CC}	16	Supply Voltage
GND	8	Ground

FUNCTION TABLES

FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FOR C_n+ x OUTPUT

INPUTS			OUTPUT
$\overline{G}0$	$\overline{P}0$	C_n	C_n+ x
L	X	X	H
X	L	H	H
All other combinations			L

Cn+y OUTPUT

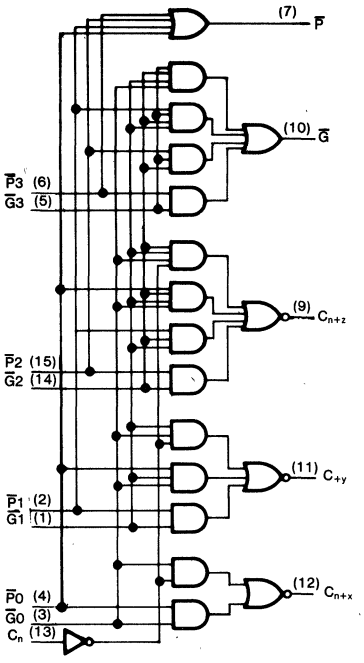
INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

Cn+z OUTPUT

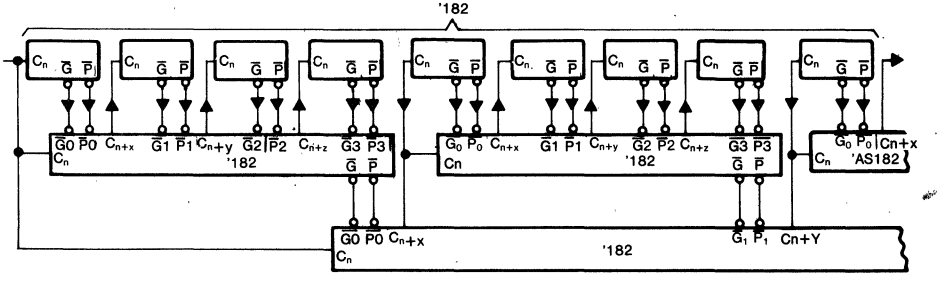
INPUTS							OUTPUT
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high-level, L = low level, X = don't care
Any inputs not shown in a given table are don't care with respect to that output.

LOGIC DIAGRAM



Figure; THE '182 IN A 64-BIT LOOK-AHEAD CARRY CIRCUIT



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT182

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, $\overline{P}i$ or $\overline{G}i$ to $C_{n+x}C_{n+y}$, C_{n+z}	t_{PLH}	$C_L = 50pF$	12		20		24	ns
	t_{PHL}		12		20		24	
Propagation Delay, $\overline{P}i$ or $\overline{G}i$ to $\overline{G}$	t_{PLH}	$C_L = 50pF$	12		20		24	ns
	t_{PHL}		12		20		24	
Propagation Delay, C_n to C_{n+x}, C_{n+y}, C_{n+z}	t_{PLH}	$C_L = 50pF$	15		21		26	ns
	t_{PHL}		15		21		26	
Propagation Delay $\overline{P}i$ to $\overline{P}$	t_{PLH}	$C_L = 50pF$	11		18		21	ns
	t_{PHL}		11		18		21	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- For use in high-speed wallace-tree summing
- Fast addition operation
- Low power consumption characteristic of CMOS
- High output current drive: I_{OL} = 8mA @ V_{OL} = 0.5V
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74AHCT: −40°C to + 85°C
  KS54AHCT: −55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

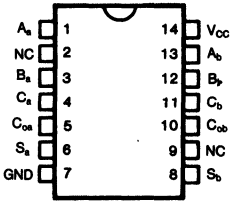
DESCRIPTION

The '183 is a dual full adder features an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than 2 gate delays.

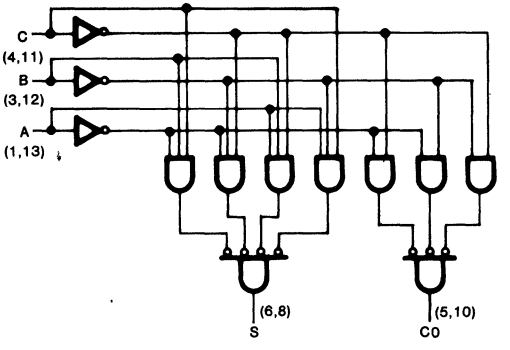
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Half)

Inputs			Output	
A	B	C	S	C_o
L	L	L	L	L
H	L	L	H	L
L	H	L	H	L
L	L	H	H	L
H	H	L	L	H
H	L	H	L	H
L	H	H	L	H
H	H	H	H	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), AHCT183

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF	10		15		18	ns
	t_{PHL}		13		20		24	
Input Capacitance	C_{IN}		5					pF
Power dissipation Capacitance*	C_{PD}							pF

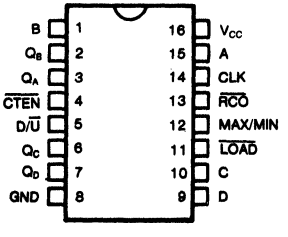
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Synchronous 4-Bit Up/Down Decade Counters

FEATURES

- **Single down/up count control line**
- **Look-ahead circuit enhances speed of cascaded counters**
- **Fully synchronous in count modes**
- **Asynchronously presettable with load control**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{LOAD}$	D/$\overline{U}$	$\overline{CTEN}$	CLK	Input	O_n
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	l	↑	X	count up
count down	H	H	l	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

$\overline{RCO}$ AND MAX/MIN FUNCTION TABLE

INPUTS		TERMINAL COUNT STATE					OUTPUTS	
D/$\overline{U}$	$\overline{CTEN}$	CLK	Q_A	Q_B	Q_C	Q_D	MAX/MIN	$\overline{RCO}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊔	H	X	X	H	⊓	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	⊓	⊔

H = HIGH voltage level
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
X = Don't care
↑ = LOW-to-HIGH CLK transition
⊔ = one LOW level pulse
⊓ = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no affect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

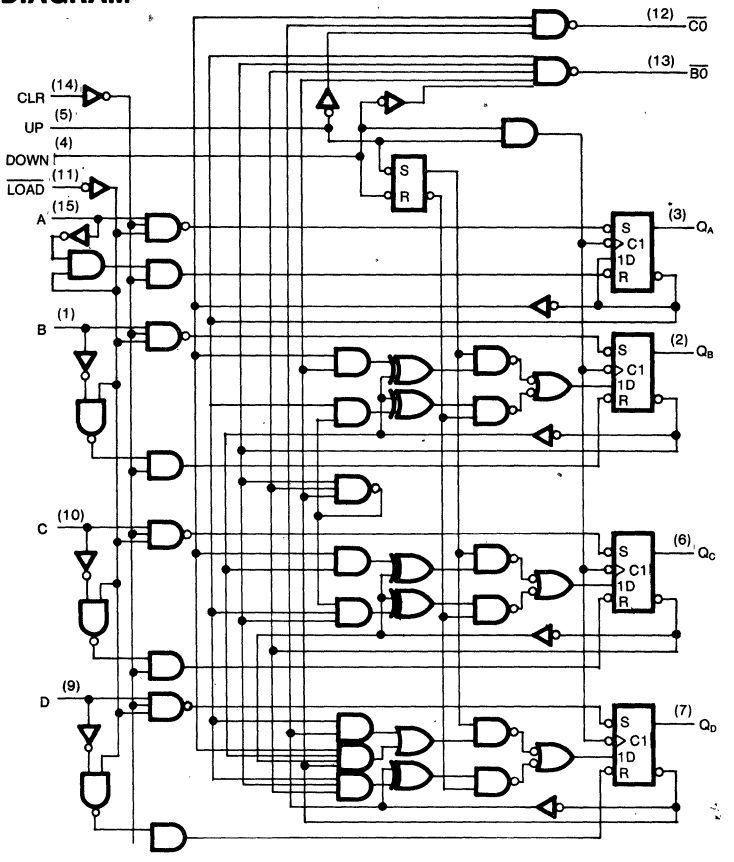
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

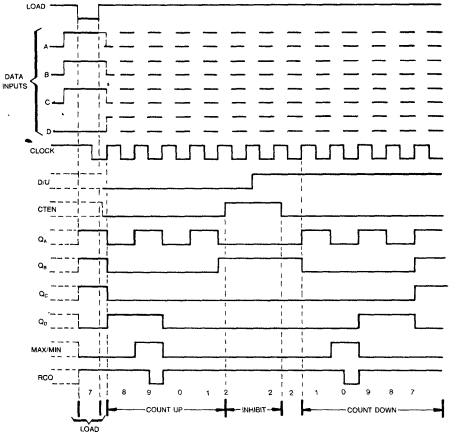
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Typical load, count, and inhibit sequences



Sequence;
(1) Load (preset) to BCD seven.
(2) Count up to eight, mine(maximum) zero, one, and two.
(3) Inhibit
(4) Count down to one, zero (minimum), nine, egiht, and seven

NOTE A: Clear overrides load data, and count inputs.
Note B: When count up, count-down input must be high; when counting down, countup intput must be high.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT190

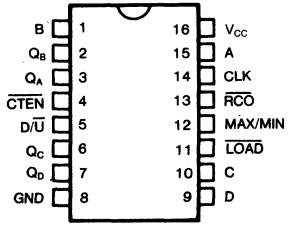
Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	50	30		25		MHz
Propagation Delay, $\overline{LOAD}$ to any Q		t_{PLH}		18		30		36	ns
		t_{PHL}		18		30		36	
Propagation Delay, A,B,C, D to any Q		t_{PLH}		13		21		25	ns
		t_{PHL}		13		21		25	
Propagation Delay, CLK to $\overline{RCO}$		t_{PLH}		12		20		24	ns
		t_{PHL}		12		20		24	
Propagation Delay, CLK to any Q		t_{PLH}		11		18		22	ns
		t_{PHL}		11		18		22	
Propagation Delay, CLK to MAX/MIN		t_{PLH}		19		31		37	ns
		t_{PHL}		19		31		37	
Propagation Delay, D/$\overline{U}$ to $\overline{RCO}$		t_{PLH}		19		32		38	ns
		t_{PHL}		19		32		38	
Propagation Delay, D/$\overline{U}$ to MAX/MIN		t_{PLH}		15		25		30	
		t_{PHL}		15		25		30	
Propagation Delay, $\overline{CTEN}$ to $\overline{RCO}$		t_{PLH}		11		18		22	ns
		t_{PHL}		11		18		22	
Pulse Width	CLK High or Low	t_w		10		17		20	ns
	$\overline{LOAD}$ Low			12		20		25	
Setup Time	Data before $\overline{LOAD}$↑	t_{su}		10	17		20		ns
	$\overline{CTEN}$ before CLK↑			10	17		20		
	D/$\overline{U}$ before CLK↑			10	17		20		
	$\overline{LOAD}$ Inactive before CLK↑			10	17		20		
Hold Time	Data after $\overline{LOAD}$↑	t_h		2	4		5		ns
	$\overline{CTEN}$ after CLK↑			−3	0		0		
	D/$\overline{U}$ after CLK↑			−3	0		0		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		80					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Single down/up count control line**
- **Look-ahead circuitry enhances speed of cascaded counters**
- **Fully synchronous in count modes**
- **Asynchronously presettable with load control**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{LOAD}$	D/$\overline{U}$	$\overline{CTEN}$	CLK	Input	O_n
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	l	↑	X	count up
count down	H	H	l	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

$\overline{RCO}$ AND MAX/MIN FUNCTION TABLE

INPUTS		TERMINAL COUNT STATE					OUTPUTS	
D/$\overline{U}$	$\overline{CTEN}$	CLK	Q_A	Q_B	Q_C	Q_D	MAX/MIN	$\overline{RCO}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊓	H	X	X	H	⊓	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	⊓	⊓

H = HIGH voltage level
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
X = Don't care
↑ = LOW-to-HIGH CLK transition
⊓ = one LOW level pulse
⊓ = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

DESCRIPTION

These are high-speed synchronous, reversible 4-bit binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no affect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

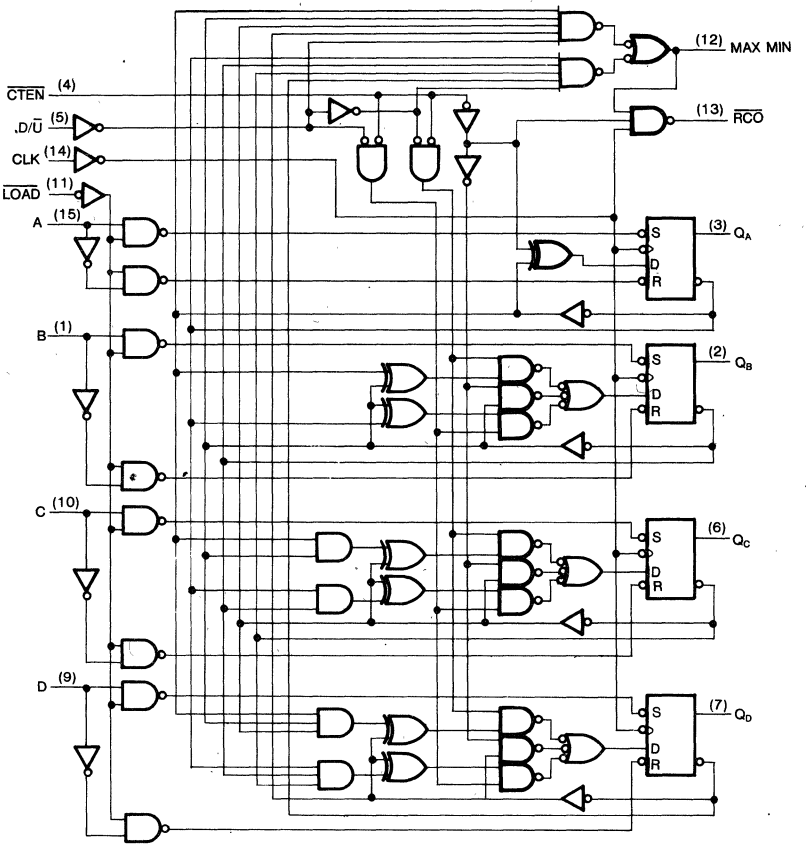
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The nipple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

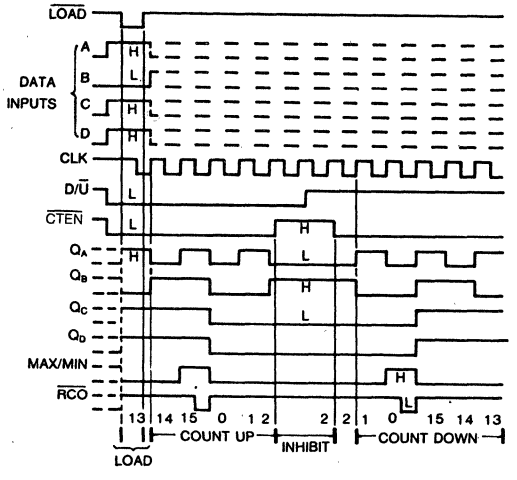
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Typical Load, Count, and Inhibit Sequence



Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

4

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT191

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	C_L=50pF	50	30		25		MHz
Propagation Delay, $\overline{LOAD}$ to any Q		t_{PLH}		18		30		36	ns
		t_{PHL}		18		30		36	
Propagation Delay, A,B,C, D to any Q		t_{PLH}		13		21		25	ns
		t_{PHL}		13		21		25	
Propagation Delay, CLK to $\overline{RCO}$		t_{PLH}		12		20		24	ns
		t_{PHL}		12		20		24	
Propagation Delay, CLK to any Q		t_{PLH}		11		18		22	ns
		t_{PHL}		11		18		22	
Propagation Delay, CLK to MAX/MIN		t_{PLH}		19		31		37	ns
		t_{PHL}		19		31		37	
Propagation Delay, D/$\overline{U}$ to $\overline{RCO}$		t_{PLH}		19		32		38	ns
		t_{PHL}		19		32		38	
Propagation Delay, D/$\overline{U}$ to MAX/MIN		t_{PLH}		15		25		30	
		t_{PHL}		15		25		30	
Propagation Delay, $\overline{CTEN}$ to $\overline{RCO}$		t_{PLH}		11		18		22	ns
		t_{PHL}		11		18		22	
Pulse Width	CLK High or Low	t_w		10		17		20	ns
	$\overline{LOAD}$ Low			12		20		25	
Setup Time	Data before $\overline{LOAD}$↑	t_{su}		10	17		20		ns
	$\overline{CTEN}$ before CLK↑			10	17		20		
	D/$\overline{U}$ before CLK↑			10	17		20		
	$\overline{LOAD}$ Inactive before CLK↑			10	17		20		
Hold Time	Data after $\overline{LOAD}$↑	t_h		2	4		5		ns
	$\overline{CTEN}$ after CLK↑			−3	0		0		
	D/$\overline{U}$ after CLK↑			−3	0		0		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		80					pF

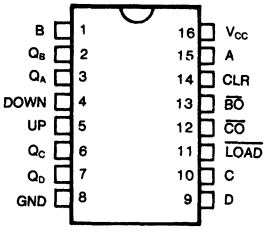
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Synchronous 4-Bit Up/Down Decade Counters with Dual Clock

FEATURES

- **Look-ahead circuit enhances cascaded counters**
- **Fully synchronous in count modes**
- **Parallel asynchronous load for modulo-N count lengths**
- **Asynchronous clear**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output ($\overline{BO}$) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

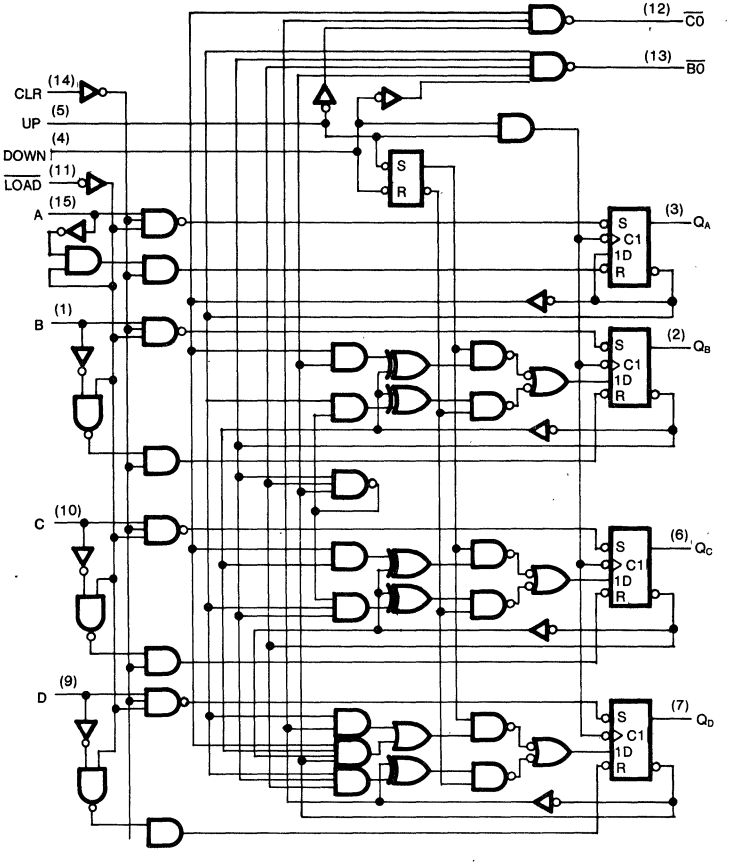
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

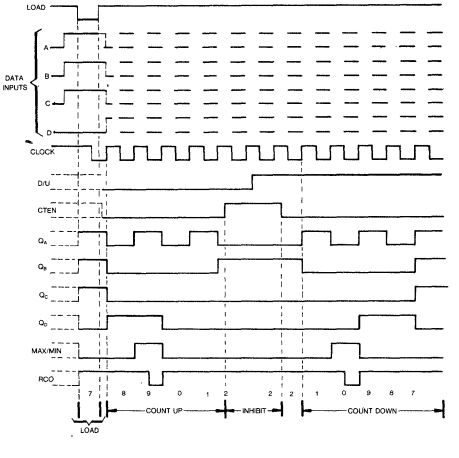
OPERATING MODE	INPUTS								OUTPUTS					
	CLR	$\overline{LOAD}$	UP	DOWN	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{CO}$	$\overline{BO}$
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
paraiel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	A	B	C	D	L	H
	L	L	H	X	H	X	X	H	A	B	C	D	H	H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X		count down				H	H**

* $\overline{CO}$=Up at terminal count up (HHHH)
** $\overline{BO}$=Down at terminal count down (LLLL)
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW to HIGH clock transition

LOGIC DIAGRAM



Typical load, count, and inhibit sequences



Sequence;
(1) Load (preset) to BCD seven.
(2) Count up to eight, mine(maximum) zero, one, and two.
(3) Inhibit
(4) Count down to one, zero (minimum), nine, egiht, and seven

NOTE A: Clear overrides load data, and count inputs.
Note B: When count up, count-down input must be high; when counting down, countup intput must be high.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT192

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	50	30		25		MHz
Propagation Delay, UP to $\overline{CO}$		t_{PLH}		11		18		22	ns
		t_{PHL}		11		18		22	
Propagation Delay, DOWN to any Q		t_{PLH}		11		18		22	ns
		t_{PHL}		11		18		22	
Propagation Delay, UP or DOWN to any Q		t_{PLH}		11		19		23	ns
		t_{PHL}		11		19		23	
Propagation Delay, $\overline{LOAD}$ to any Q		t_{PLH}		17		29		35	ns
		t_{PHL}		17		29		35	
Propagation Delay, CLR to any Q		t_{PLH}		10		17		20	ns
Pulse Width	CLR High	t_w		6	10		15		ns
	$\overline{LOAD}$ Low			10	17		20		
	UP or DOWN High or Low			10	17		20		
Setup Time	Data before $\overline{LOAD}$↑	t_{su}		10	17		29		ns
	CLR Inactive before UP↑ or DOWN↑			10	17		20		
	LOAD Inactive before UP↑ or DOWN↑			10	17		20		
	UP high before DOWN↑			10	17		17		
	Down high before UP↑			8	15		15		
Hold Time	Data after $\overline{LOAD}$↑	t_h		−3	0		0		ns
	UP High after DOWN↑			−3	0		0		
	DOWN High after UP↑			3	8		6		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		80					pF

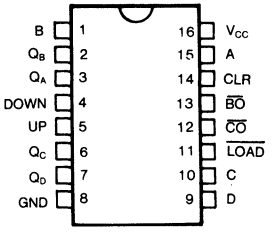
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Synchronous 4-Bit Up/Down Binary Counters with Dual Clock

FEATURES

- Look-ahead circuitry enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



DESCRIPTION

These are high-speed synchronous reversible 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output ($\overline{BO}$) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

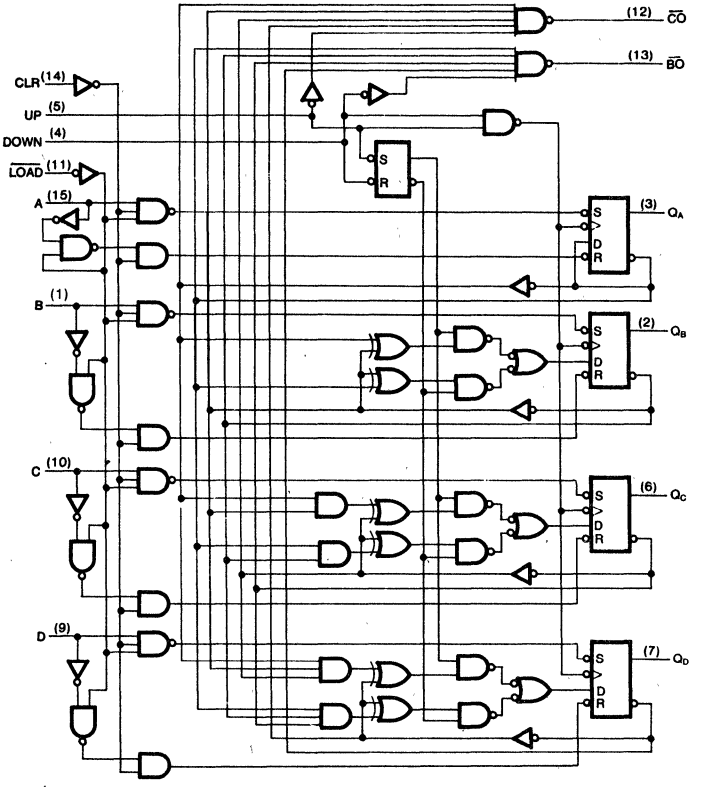
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

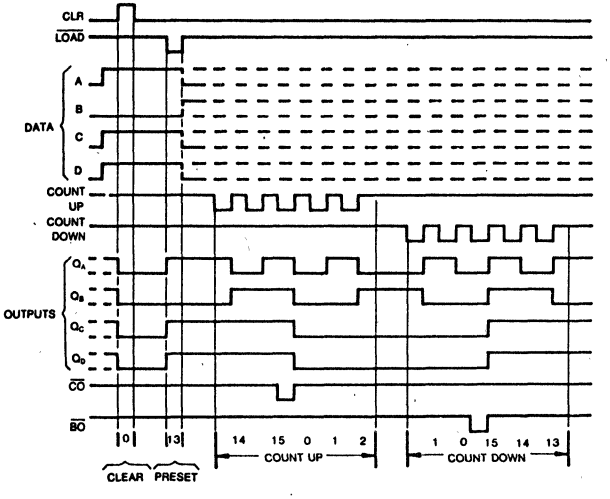
OPERATING MODE	INPUTS								OUTPUTS					
	CLR	$\overline{LOAD}$	UP	DOWN	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{CO}$	$\overline{BO}$
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X		count down				H	H**

H= HIGH voltage level
L= LOW voltage lovel
X= don't care
↑= LOW-to-HIGH clock transition
* $\overline{CO}$ = UP at terminal count up (HHHH)
** $\overline{BO}$ = DOWN at terminal count down (LLLL)

LOGIC DIAGRAM



Typical Clear, Load, and Count Sequences



Sequence:

(1) Clear outputs to zero.

(2) Load (preset) to binary thirteen.

(3) Count up to fourteen, fifteen, carry, zero, one and two.

(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Note A: Clear overrides load data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT193

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	50	30		25		MHz
Propagation Delay, UP to $\overline{CO}$		t_{PLH}		11		18		22	ns
		t_{PHL}		11		18		22	
Propagation Delay, DOWN to any Q		t_{PLH}		11		18		22	ns
		t_{PHL}		11		18		22	
Propagation Delay, UP or DOWN to any Q		t_{PLH}		11		19		23	ns
		t_{PHL}		11		19		23	
Propagation Delay, $\overline{LOAD}$ to any Q		t_{PLH}		17		29		35	ns
		t_{PHL}		17		29		35	
Propagation Delay, CLR to any Q		t_{PLH}		10		17		20	ns
Pulse Width	CLR High	t_w		6	10		15		ns
	$\overline{LOAD}$ Low			10	17		20		
	UP or DOWN High or Low			10	17		20		
Setup Time	Data before $\overline{LOAD}$↑	t_{su}		10	17		29		ns
	CLR Inactive before UP↑ or DOWN↑			10	17		20		
	$\overline{LOAD}$ Inactive before UP↑ or DOWN↑			10	17		20		
	UP high before DOWN↑			10	17		17		
	Down high before UP↑			8	15		15		
Hold Time	Data after $\overline{LOAD}$↑	t_h		−3	0		0		ns
	UP High after DOWN↑			−3	0		0		
	DOWN High after UP↑			3	8		6		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		80					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4-Bit Bidirectional Universal Shift Registers

FEATURES

- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Left or Right Shifts**
- **Parallel Synchronous Loading**
- **Direct Overriding Clear**
- **Temporary Data Latching Capability**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74AHCT: −40°C to +85°C KS54AHCT: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

These bidirectional shift registers feature parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

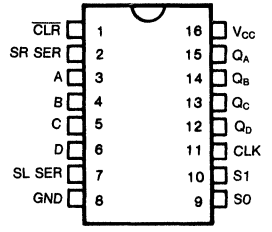
— Inhibit clock (temporary data latch/do nothing)
— Shift-right (in the direction Q_A toward Q_D)
— Shift-left (in the direction Q_D toward Q_A)
— Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift-right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

4

PIN CONFIGURATION

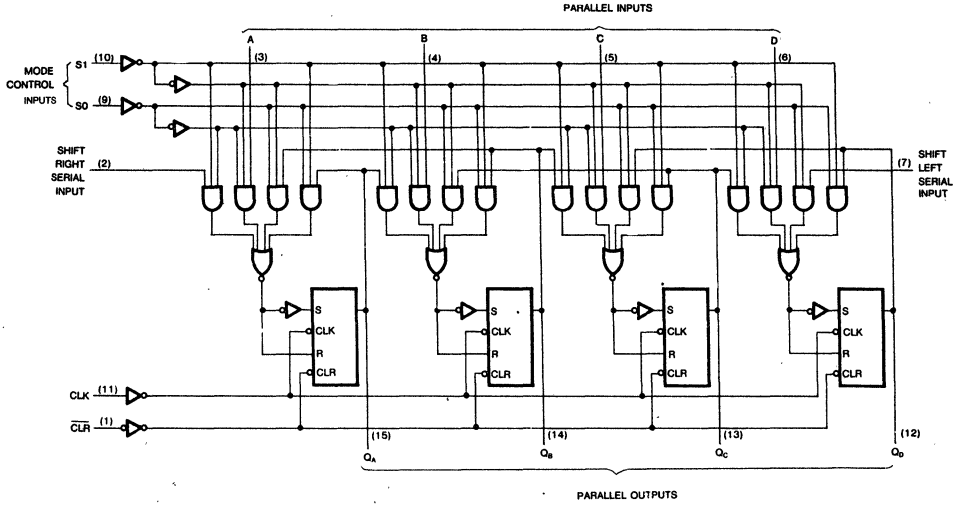


FUNCTION TABLE

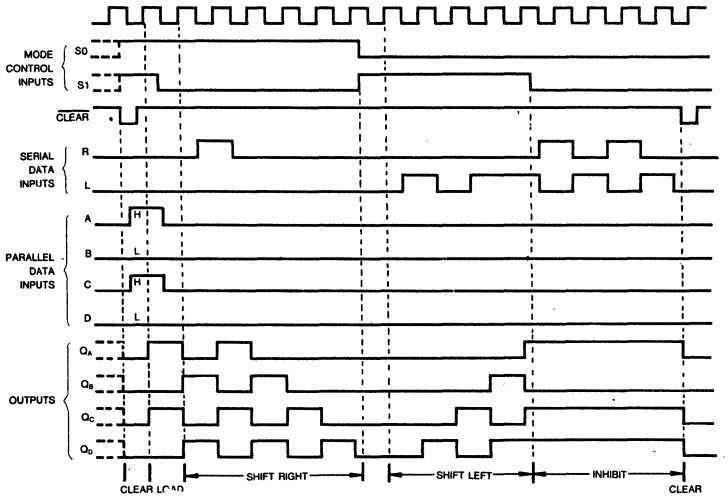
INPUTS										OUTPUTS			
$\overline{CLR}$	MODE		CLK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{DN}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H=high level (steady state)
L=low level (steady state)
X=irrelevant (any input, including transitions)
↑=transition from low to high level
a,b,c,d=the level of steady-state input at inputs A,B,C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}=the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}=the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

LOGIC DIAGRAM



typical clear, load, right-shift, inhibit, and clear sequences



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT194

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	60	35		30		MHz
Propagation Delay, CLK to Q_H		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Propagation Delay, $\overline{CLR}$ to Q_H		t_{PHL}		11		19		22	ns
Pulse Width	$\overline{CLR}$ LOW	t_w		10	17		20		ns
	CLK High or LOW			10	17		20		
Setup Time, Any Input before CLK↑		t_s		10	17		20		ns
Hold Time, Data after CLK↑		t_s		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		80					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Parallel Synchronous Loading**
- **J and K Inputs to First Stage**
- **Right-shift Only with Complementary Outputs on Last Stage**
- **Direct Overriding Clear**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

These 4-bit rigisters feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction A_A toward Q_D)

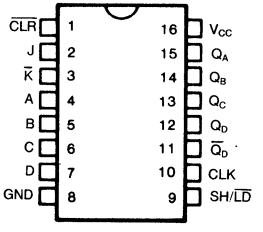
Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

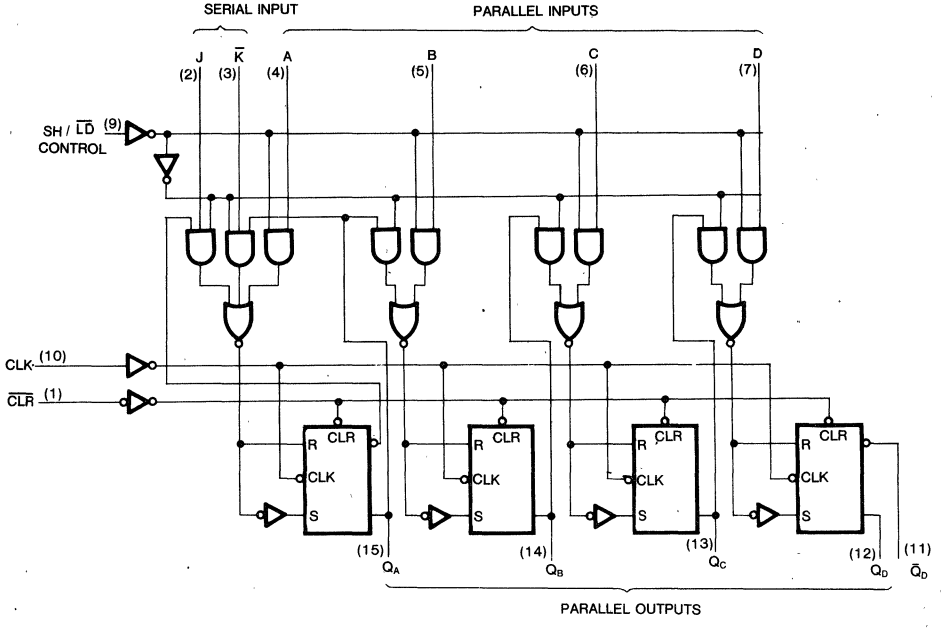


FUNCTION TABLE

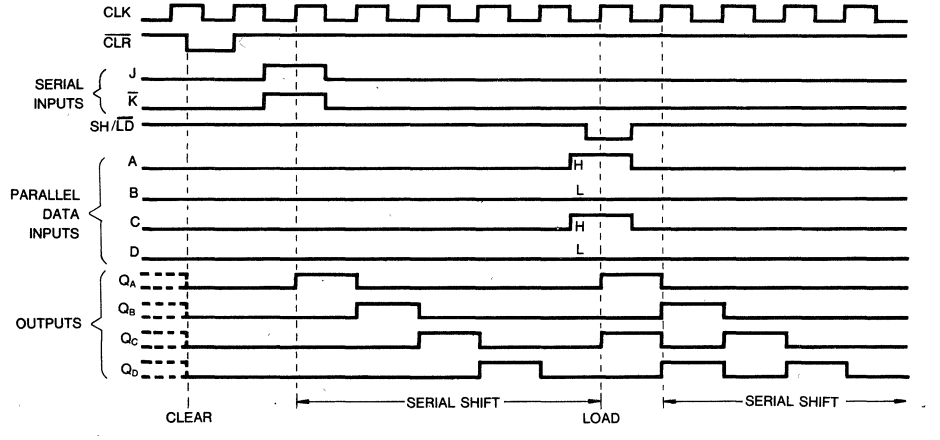
INPUTS									OUTPOUTS				
			SERIAL		PARALLEL								
$\overline{CLR}$	SH/$\overline{LD}$	CLK	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H=high level (steady state)
L=low level (steady state)
X=irrelevant (any input, including transitions)
↑=transition from low to high level
a,b,c,d=the level of steady-state input at A,B,C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}=the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}=the level of Q_A, Q_B or Q_C, respectively, before the mostrecent transition of the clock.

LOGIC DIAGRAMS



typical clear, shift, and load sequences



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT195

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	60	35		30		MHz
Propagation Delay, CLK to Q_H		t_{PLH}		10		17		20	ns
		t_{PHL}		10		17		20	
Propagation Delay, $\overline{CLR}$ to Q_H		t_{PHL}		11		19		22	ns
Pulse Width	$\overline{CLR}$ Low	t_w		10	17		20		ns
	CLK High or Low			10	17		20		
Setup Time before CLK↑	SH/$\overline{LD}$ High	t_{su}		10	17		20		ns
	Serial or Parallel Data			10	17		20		
	$\overline{CLR}$ inactive			10	17		20		
Hold Time after CLK↑	SH/$\overline{LD}$ High			−3	0		0		ns
	Serial or Parallel Data			−3	0		0		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Octal Buffers and Line Drivers with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 24 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

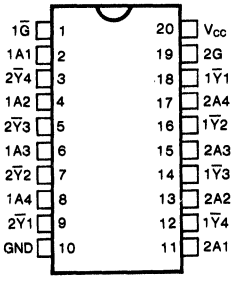
These high-speed octal buffers and line drivers are designed specificaly to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The designer has the choice of combinations of inverting non-inverting outputs and symmetrical complementary input control (both active-low, or one active-low, the other active-high).

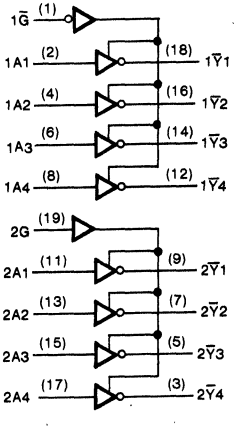
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Input		Output
$\bar{G}$	A	Y
L	L	H
L	H	L
H	X	Z

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT210

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay, A to $\overline{Y}$	t_{PLH}	$C_L = 50pF$		6		10		12	ns
		$C_L = 150pF$		9		15		18	
	t_{PHL}	$C_L = 50pF$		7		10		12	
		$C_L = 150pF$		11		16		19	
Output Enable Time, Enable to $\overline{Y}$	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	12		20		24	ns
			$C_L = 150pF$	15		25		30	
	t_{PZL}		$C_L = 50pF$	12		20		24	
			$C_L = 150pF$	15		25		30	
Output Disable Time, Enable to $\overline{Y}$	t_{PHZ}	$R_L = 1k\Omega$		13		18		22	ns
	t_{PLZ}	$C_L = 50pF$		13		18		22	
Input Capacitance	C_{IN}			5					pF
Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance*	C_{PD}*	Output Disabled		5					pF
		Output Enabled		30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

FEATURES

- **Designed specifically for high-speed memory decoders and data transmission systems.**
- **Incorporates 2 enable inputs to simplify cascading and/or data reception**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

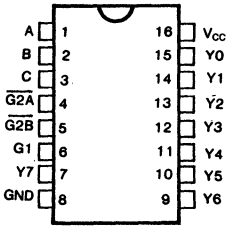
This conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding.

A 24-line decoder can be implemented without external inverters and a 31-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

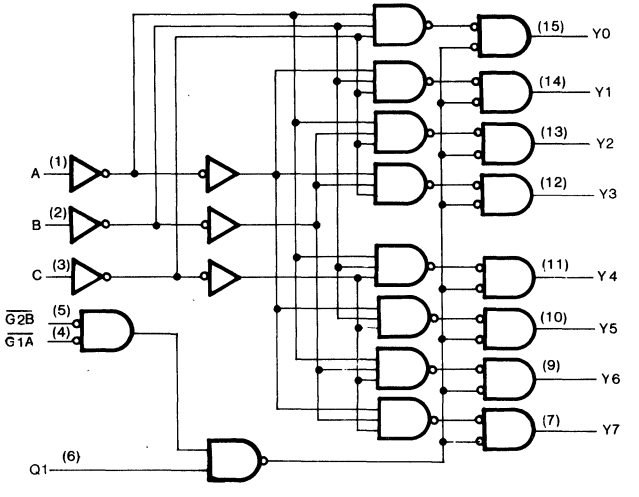


FUNCTION TABLE

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	H	L	L	L	H	L	L	L	L	L
H	L	H	L	L	L	L	L	H	L	L	L	L
H	L	H	L	L	L	L	L	L	H	L	L	L
H	L	H	L	H	L	L	L	L	L	H	L	L
H	L	H	H	L	L	L	L	L	L	L	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H

* $\overline{G2} = \overline{G2A} + \overline{G2B}$

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_A=25°C	KS74AHCT T_A=−40°C to +85°C	KS54AHCT T_A=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT238

Characteristic	Symbol	Conditions†	T_A=25°C V_{CC}=5.0V	KS74AHCT T_A=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_A=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A, B, C or Y	t_{PLH}	C_L=50pF	12		20		24	ns
	t_{PHL}		12		20		24	
Propagation Delay, G1 to any Y	t_{PLH}		10		17		20	ns
	t_{PHL}		10		17		20	
Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to any Y	t_{PLH}		10		17		20	ns
	t_{PHL}		10		17		20	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}		50					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

Dual 1-of-4 Decoder/Demultiplexers

FEATURES

- **Designed specifically for high-speed memory decoders and data transmission systems**
- **Incorporates 2 enable inputs to simplify cascading and/or data reception**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times in high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory.

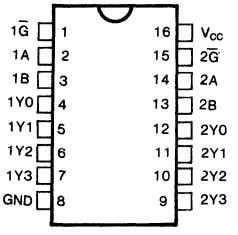
This means that the effective system delay introduced by the decoder is negligible.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

4

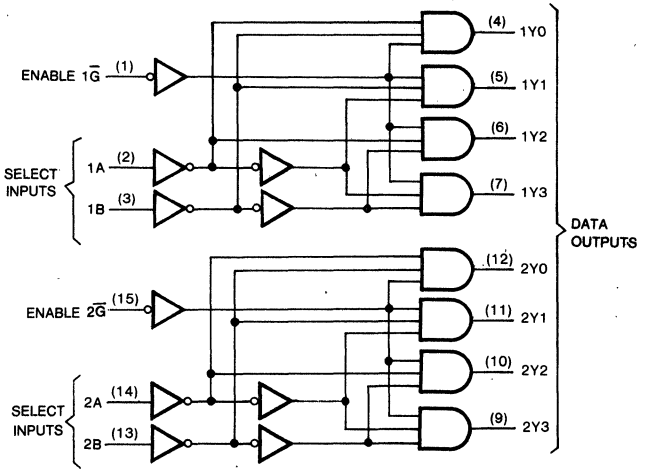
PIN CONFIGURATION



FUNCTION TABLE

Inputs			Outputs			
Enable	Select					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	L	H	L	H	L	L
L	H	L	L	L	H	L
L	H	H	L	L	L	H

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT239

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to any Y	t_{PLH}	C_L=50pF	12		20		24	ns
	t_{PHL}		12		20		24	
Propagation Delay, $\overline{G}$ to any Y	t_{PLH}		10		17		20	ns
	t_{PHL}		10		17		20	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}		50					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

4

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

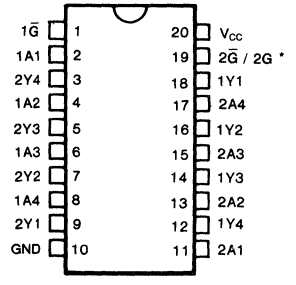
These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The designer has the choice of combinations of inverting/non-inverting outputs and symmetrical complementary input control (both active-low, or one active-low, the other active-high).

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

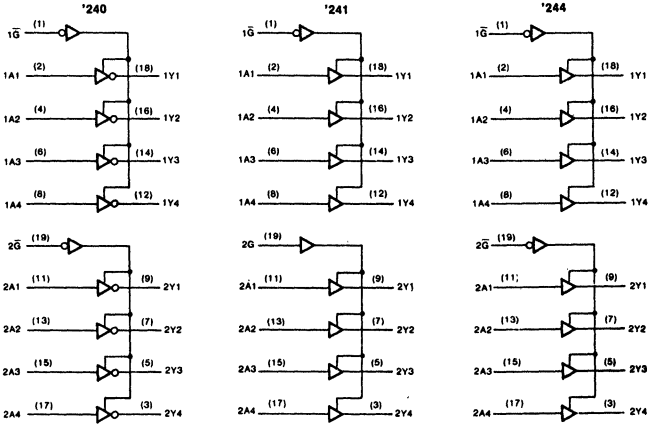
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



*2G̅ for '240 and '244
2G for '241

LOGIC DIAGRAMS



FUNCTION TABLE

Input			'241, '244	'240
			Output	Output
G	$\overline{G}$	A	Y	Y
H	L	L	L	H
H	L	H	H	L
L	H	X	Z	Z

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT240, AHCT241, AHCT244

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay, A to Y	t_{PLH}	$C_L = 50pF$		6		10		12	ns
		$C_L = 150pF$		9		15		18	
	t_{PHL}	$C_L = 50pF$		6		10		12	
		$C_L = 150pF$		9		15		18	
Output Enable Time, Enable to Y	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	12		20		24	ns
			$C_L = 150pF$	15		25		30	
	t_{PZL}		$C_L = 50pF$	12		20		24	
			$C_L = 150pF$	15		25		30	
Output Disable Time, Enable to Y	t_{PHZ}	$R_L = 1k\Omega$		13		18		22	ns
	t_{PLZ}	$C_L = 50pF$		13		18		22	
Input Capacitance	C_{IN}			5					pF
Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance*	C_{PD}	Output Disabled		5					pF
		Output Enabled		30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

Quad Bus Transceivers with 3-State Outputs

Preliminary Specifications

FEATURES

- **2-Way Asynchronous Communication Between Data Buses**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

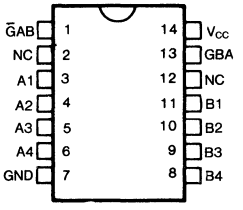
DESCRIPTION

These four-data line transceivers are designed for asynchronous two-way communications between data buses.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

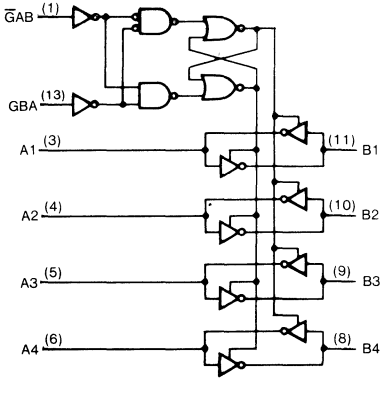


FUNCTION TABLE

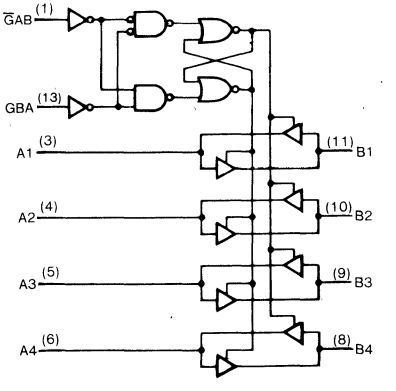
INPUTS		'242	'243
$\overline{GAB}$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	B to A	B to A
H	L	Isolation	Isolation
L	H	Isolation	Isolation

LOGIC DIAGRAMS

'242



'243



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT242, AHCT243

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay, A to B or B to A	t_{PLH}	$C_L = 50pF$		7		11		15	ns
		$C_L = 150pF$		10		16		21	
	t_{PHL}	$C_L = 50pF$		7		11		15	
		$C_L = 150pF$		10		16		21	
Output Enable Time $\overline{G}$AB to B, GBA to A	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	12		20		25	ns
			$C_L = 150pF$	15		25		21	
	t_{PZL}		$C_L = 50pF$	12		20		25	
			$C_L = 150pF$	15		25		21	
Output Disable Time, $\overline{G}$AB to B, GBA to A	t_{PHZ}	$R_L = 1k\Omega$		12		20		25	ns
	t_{PLZ}	$C_L = 50pF$		12		20		25	
Input Capacitance	C_{IN}			5					pF
Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance*(per stage)	C_{PD}	Output Enabled		30					pF
		Output Disabled		5					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

Octal Bus Transceivers with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

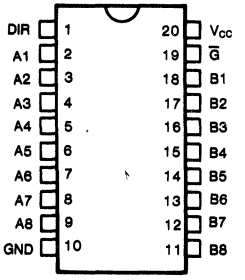
These high-speed octal bus transceivers are designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

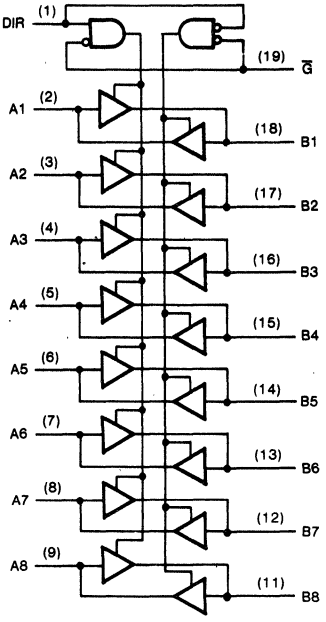
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Operation
$\overline{G}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT245

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A to B or B to A	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	6 9		10 15		14 20	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	6 9		10 15		14 20	ns
Output Enable Time $\overline{G}$ to A or B	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	12 15		20 25		25 31	ns
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	12 17		20 25		25 31	ns
Output Disable Time, $\overline{G}$ to A or B	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	13		18		22	ns
	t_{PLZ}		13		18		22	ns
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*	C_{PD}	$\overline{G} = V_{CC}$ $\overline{G} = GND$ (per stage)	5 30					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

1-of-8 Data Selectors/Multiplexers with 3-State Outputs

FEATURES

- **Three-State Version of '151**
- **Three-State Outputs Interface Directly with System Bus**
- **Performs Parallel-to-Serial Conversion**
- **Complementary Outputs Provide True and Inverted Data**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

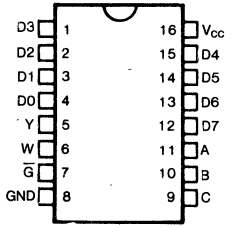
The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ($\overline{G}$). The outputs are disabled when $\overline{G}$ is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

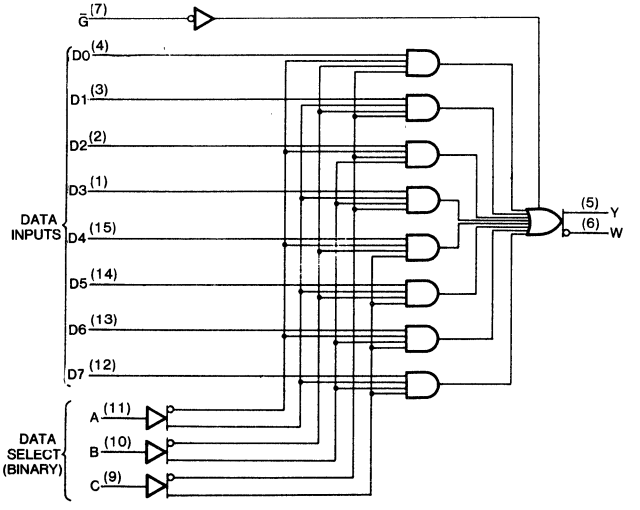
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

4

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{G}$		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O= −6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT251

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A, B or C to Y	t_{PLH}	$C_L=50pF$	13		21		25	ns
		$C_L=150pF$	16		26		31	
	t_{PHL}	$C_L=50pF$	13		21		25	
		$C_L=150pF$	16		26		31	
Propagation Delay, A, B or C to W	t_{PLH}	$C_L=50pF$	15		24		27	ns
		$C_L=150pF$	18		29		33	
	t_{PHL}	$C_L=50pF$	15		24		27	
		$C_L=150pF$	18		29		33	
Propagation Delay, Any D to Y	t_{PLH}	$C_L=50pF$	9		15		18	ns
		$C_L=150pF$	12		20		24	
	t_{PHL}	$C_L=50pF$	9		15		18	
		$C_L=150pF$	12		20		24	
Propagation Delay, Any D to W	t_{PLH}	$C_L=50pF$	8		15		18	ns
		$C_L=150pF$	11		20		24	
	t_{PHL}	$C_L=50pF$	8		15		18	
		$C_L=150pF$	11		20		24	
Output Enable Time, $\overline{G}$ to Y or W	t_{PZH}	$R_L=1k\Omega$, $C_L=50pF$	11		18		22	ns
		$R_L=1k\Omega$, $C_L=150pF$	14		23		28	
	t_{PZL}	$R_L=1k\Omega$, $C_L=50pF$	11		18		22	
		$R_L=1k\Omega$, $C_L=150pF$	14		23		28	
Output Disable Time, $\overline{G}$ to Y or W	t_{PHZ}	$R_L=1k\Omega$, $C_L=50pF$	13		18		22	ns
	t_{PLZ}		13		18		22	
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

Dual 1-of-4 Data Selectors/Multiplexers with 3-State Outputs

FEATURES

- **Three-State Version of '153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

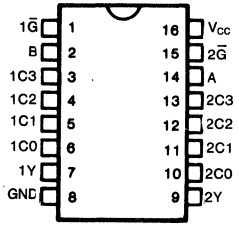
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

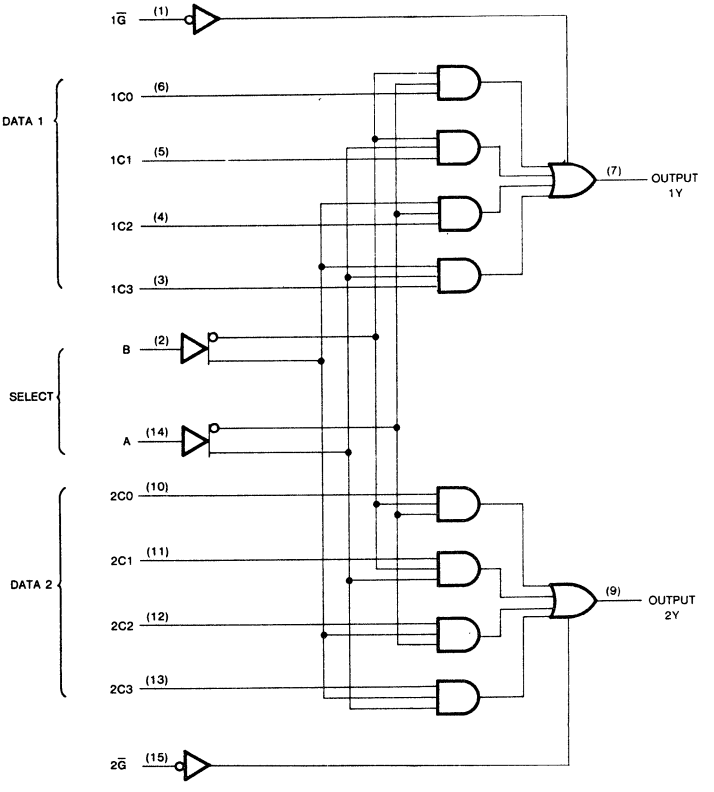


FUNCTION TABLE

SELECT		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT253

Characteristic	Symbol	Conditions†		T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay, A or B to any Y	t_{PLH}	C_L=50pF C_L=150pF		13 16		21 26		25 31	ns
	t_{PHL}	C_L=50pF C_L=150pF		13 16		21 26		25 31	
Propagation Delay, Data (any C) to any Y	t_{PLH}	C_L=50pF C_L=150pF		9 12		15 20		18 34	ns
	t_{PHL}	C_L=50pF C_L=150pF		9 12		15 20		18 34	
Output Enable Time $\overline{G}$ to Y	t_{PZH}	R_L=1kΩ	C_L=50pF C_L=150pF	10 13		16 21		19 35	ns
	t_{PZL}		C_L=50pF C_L=150pF	10 13		16 21		19 35	
Output Disable Time, $\overline{G}$ to Y	t_{PHZ}	R_L=1kΩ C_L=50pF		13		18		22	ns
	t_{PLZ}			13		18		22	
Input Capacitance	C_{IN}			5					pF
Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance*	C_{PD}								pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

KS54AHCT 257/258 KS74AHCT Quad 2-Line to 1-Line Data Selector/ Multiplexers with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

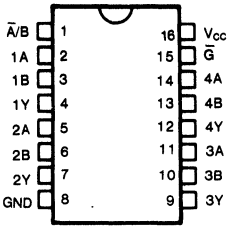
DESCRIPTION

The '257 and '258 multiplex signals from for-bit data sources to four-output data lines in bus organized systems. The data presented at the outputs is non-inverted for the '257, and inverted for the '258.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

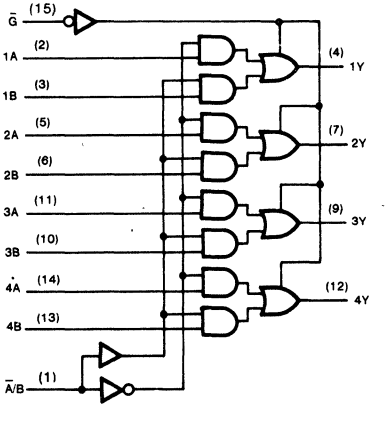


FUNCTION TABLE

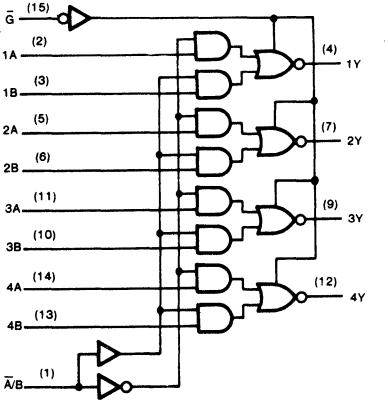
Inputs				Output Y	
Output Control	Select	Data		'257	'258
$\overline{G}$	A/B	A	B		
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

LOGIC DIAGRAMS

'257



'258



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT257

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to any Y	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	7 10		12 17		14 20	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	7 10		12 17		14 20	
Propagation Delay, $\overline{A}$/B to any Y	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	12 15		20 25		24 30	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	12 15		20 25		24 30	
Output Enable Time, $\overline{G}$ to any Y	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	13 16		18 23		22 28	ns
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	13 16		18 23		22 28	
Output Disable Time, $\overline{G}$ to any Y	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	13		18		22	ns
	t_{PLZ}		13		18		22	
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT258

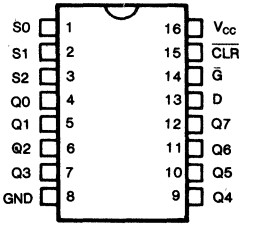
Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to any Y	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	7 10		12 17		14 20	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	9 12		14 19		16 22	
Propagation Delay, $\overline{A}$/B to any Y	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	14 17		23 28		28 34	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	14 17		23 28		28 34	
Output Enable Time, $\overline{G}$ to any Y	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	11 14		18 23		22 28	ns
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	11 14		18 23		22 28	
Output Disable Time, $\overline{G}$ to any Y	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	13		18		22	ns
	t_{PLZ}		13		18		22	
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **8-Bit parallel-out storage register performs serial-to-parallel conversion with storage**
- **Asynchronous parallel clear**
- **Active high decoder**
- **Enable/Disable input simplifies expansion**
- **Expandable for N-bit applications**
- **Four distinct functional modes**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

The '259 is a high-speed addressable latch designed for general purpose storage applications in digital systems. It can be used for implementing working registers, serial-holding registers and active-high decoders or demultiplexers.

The '259 has four distinct modes of operation that are selected via the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs: 1) addressable latch; 2) memory; 3) active-high eight-channel demultiplexer; and 4) clear.

In the addressable latch mode, data on the data input (D) is written into the addressed latch. In this mode, data will be written into the addressed latch with all non-addressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous state and are unaffected by the data of address inputs.

In the demultiplexing mode, addressed outputs will follow the state of the D input and all other outputs will remain low.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

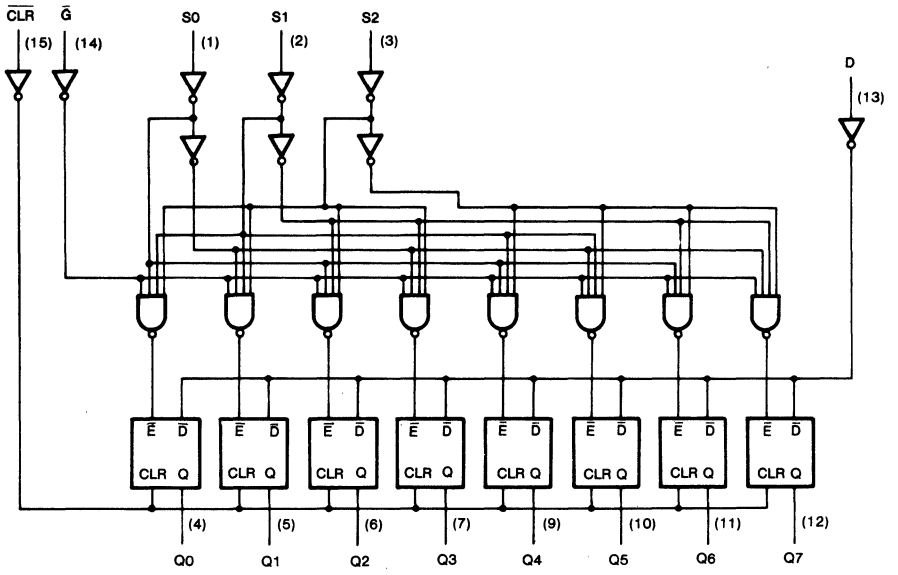
Inputs		Output of Addressed Latch	Each Other Output	Function
$\overline{CLR}$	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

D = the level at the data input.
Q_{i0} = the level of Q_{i0} (i = Q, 1, ... 7, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

Select Inputs			Latch Addressed
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT259

Characteristic		Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C V_{CC} = 5.0V ± 10%		KS54AHCT T_a = −55°C to +125°C V_{CC} = 5.0V ± 10%		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay $\overline{CLR}$ to any Q		t_{PHL}	C_L=50pF	9		15		18	ns
Propagation Delay, Data to any Q		t_{PLH}		12		19		23	ns
		t_{PHL}		12		19		23	
Propagation Delay, Address to any Q		t_{PLH}		13		22		27	ns
		t_{PHL}		13		22		27	
Propagation Delay, $\overline{G}$ to any Q		t_{PLH}		12		20		24	ns
		t_{PHL}		12		20		24	
Pulse Width	$\overline{CLR}$ Low	t_w		6	10		10		ns
	$\overline{G}$ Low			9	15		20		
Setup Time Data or Address before $\overline{G}$↑		t_{su}		10	15		20		ns
Hold Time, Data or Address before $\overline{G}$↑		t_h		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		80					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

Quad Exclusive-NOR Gates with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

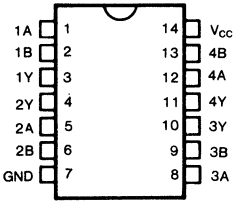
DESCRIPTION

These devices contain four independent exclusive-NOR gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

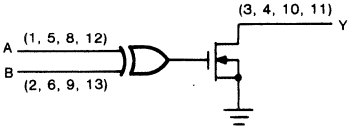
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT266

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF R_L=1kΩ	19		29		35	ns
	t_{PHL}		11		18		22	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Eight positive-edge-triggered D-type flip-flops with single-rail outputs**
- **Buffered common clock and asynchronous clear**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 24mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

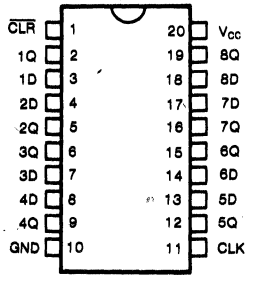
These devices are high-speed octal registers. They consist of eight positive-edge-triggered D-type flip-flops with individual D inputs and Q outputs. All flip flops are loaded and cleared simultaneously by the common buffered clock (CLK) and clear ($\overline{CLR}$) inputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

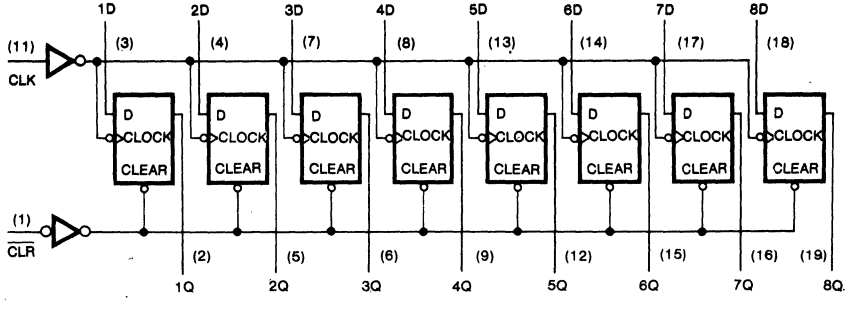


FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT273

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	50	35		30		MHz
Propagation Delay, CLK to any Q		t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	12 13		16 20		19 34	ns
		t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	12 13		16 20		19 34	ns
Propagation Delay, $\overline{CLR}$ to any Q		t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	11 14		18 23		22 28	ns
Pulse Width	$\overline{CLR}$ Low	t_w		8	14		17		ns
	CLK High or Low			8	14		17		
Setup Time before CLK↑	Data	t_{su}		6	10		10		ns
	Clear inactive State			9	15		15		
Hold time, Data after CLK↑		t_h		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per package)	150					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

FEATURES

- **Generates Odd or Even Parity for Nine Data Lines**
- **Cascadable for N-Bits Parity**
- **Can be used to Upgrade Existing Systems using MSI Parity Circuits**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

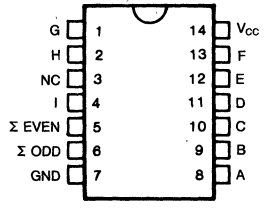
These universal, nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker, Although the '280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the '280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

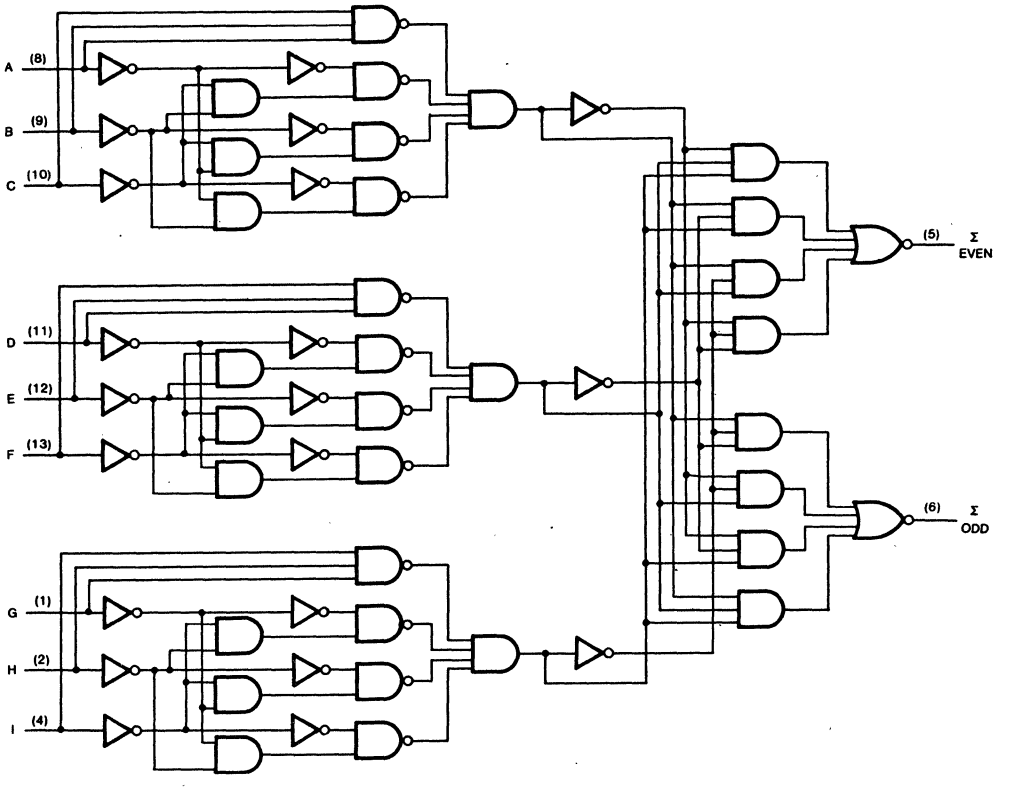
PIN CONFIGURATION



FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT280

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Σ Even	t_{PLH}	C_L=50pF C_L=150pF	12 15		20 25		24 30	ns
	t_{PHL}	C_L=50pF C_L=150pF	12 15		20 25		24 30	
Propagation Delay, Any input to Σ Odd	t_{PLH}	C_L=50pF C_L=150pF	13 16		22 27		26 32	ns
	t_{PHL}	C_L=50pF C_L=150pF	13 16		22 27		26 32	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

8-Bit Universal Shift/Storage Registers with 3-State Outputs

FEATURES

- **Multiplexed I/O ports provides improved bit density**
- **Four modes of operation: hold (store), shift right, shift left, and load data**
- **Operates with outputs enabled or at high impedance**
- **Can be cascaded for N-bit word lengths**
- **Direct overriding clear**
- **Application:**
  Stacked or push-down registers, buffer storage, and accumulator registers
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with drive current**
  (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

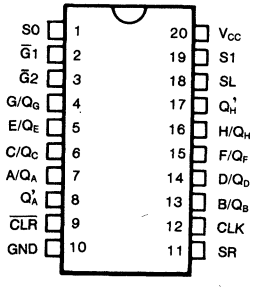
These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when $\overline{CLR}$ is low. Pulling either of the output controls, $\overline{G}1$ or $\overline{G}2$, high disables the outputs but this has no effect on clearing, shifting, or storage of data

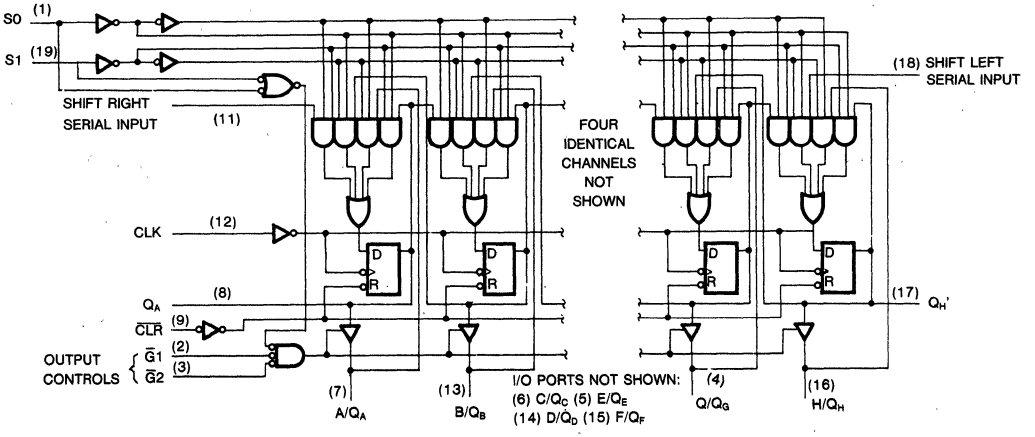
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

	Inputs							I/O Ports								Outputs	
Mode	$\overline{CLR}$	S1	S0	Output Control $\overline{G1}$	Output Control $\overline{G2}$	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA Q'A and Q'H outputs: I_O=−4mA Q_A thru Q_H outputs: I_O=−6mA	V_{CC} 4.2 4.2	V_{CC} −0.1 3.98 3.84	V_{CC} −0.1 3.84 3.7	V_{CC} −0.1 3.7	V
Miximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA Q'A and Q'H outputs: I_O=4mA I_O=8mA Q_A thru Q_H outputs: I_O=12mA I_O=24mA	0 	0.1 0.26 0.39 0.26 0.39	0.1 0.33 0.5 0.33 0.5	0.1 0.4 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable = V_{IN} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

4

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT299

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}		50	30		25		MHz
Propagation Delay, CLK to Q'_A or Q'_H		t_{PLH}	$C_L = 50pF$	10		17		20	ns
		t_{PHL}		10		17		20	
Propagation Delay, $\overline{CLR}$ to Q'_A or Q'_H		t_{PHL}		13		22		26	ns
Propagation Delay, CLK to Q_A thru Q_H		t_{PLH}	$C_L = 50pF$	10		16		19	ns
			$C_L = 150pF$	13		21		25	
		t_{PHL}	$C_L = 50pF$	10		16		19	
			$C_L = 150pF$	13		21		25	
Propagation Delay, $\overline{CLR}$ to Q_A thru Q_H		t_{PHL}	$C_L = 50pF$	13		22		26	ns
			$C_L = 150pF$	16		27		31	
Output Enable Time, $\overline{G1}$, $\overline{G2}$, to Q_A thru Q_H		t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$	11		19		23	ns
			$C_L = 150pF$	14		24		29	
		t_{PZL}	$C_L = 50pF$	11		19		23	
			$C_L = 150pF$	14		24		29	
Output Disable Time, $\overline{G1}$, $\overline{G2}$ to Q_A thru Q_H		t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	11		18		22	ns
		t_{PLZ}		11		18		22	
Pulse Width	CLK High or Low	t_w		9	15		20		ns
	$\overline{CLR}$ Low			5	8		10		
Setup time before CLK↑	S0 and S1	t_{su}		12	20		10		ns
	High-Level Inputs			8	13		15		
	Low-Level Inputs			8	13		15		
	$\overline{CLR}$ Inactive			8	13		15		
Hold Time after CLK↑	S0 and S1	t_h		0	0		0		ns
	All Inputs			0					
Input Capacitance		C_{IN}		5					pF
Output Capacitance		C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Dual 4-Line to 1-Line Data Selectors/Multiplexers

FEATURES

- **Inverting Version of '153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High drive current outputs (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

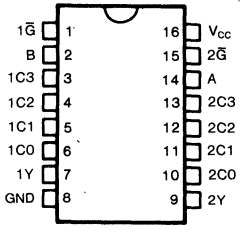
DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

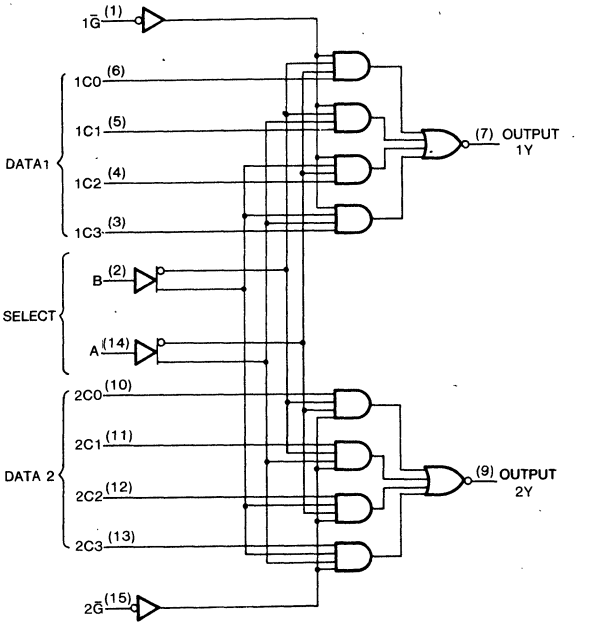
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT352

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to Y	t_{PLH}	$C_L = 50pF$	14		23		28	ns
		$C_L = 150pF$	17		28		34	
	t_{PHL}	$C_L = 50pF$	14		23		28	
		$C_L = 150pF$	17		28		34	
Propagation Delay, Data (Any C) to Y	t_{PLH}	$C_L = 50pF$	11		18		21	ns
		$C_L = 150pF$	14		23		27	
	t_{PHL}	$C_L = 50pF$	11		18		21	
		$C_L = 150pF$	14		23		27	
Propagation Delay, $\overline{G}$ to Y	t_{PLH}	$C_L = 50pF$	12		20		24	ns
		$C_L = 150pF$	15		25		30	
	t_{PHL}	$C_L = 50pF$	12		20		24	
		$C_L = 150pF$	15		25		30	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

Dual 1-of-4 Data Selectors/Multiplexers with 3-State Outputs

FEATURES

- **Inverting Version of '253**
- **Permits Multiplexing from N lines to 1 line**
- **Performs Parallel-to-Serial Conversion**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

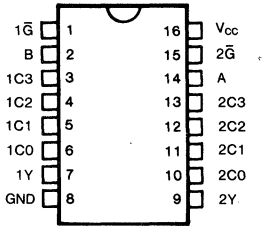
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

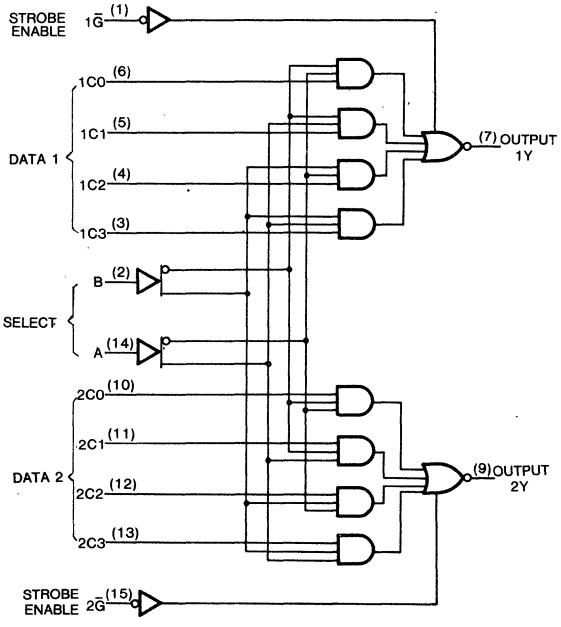
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT353

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to any Y	t_{PLH}	$C_L = 50pF$	14		24		28	ns
		$C_L = 150pF$	17		29		34	
	t_{PHL}	$C_L = 50pF$	14		24		28	
		$C_L = 150pF$	17		29		34	
Propagation Delay, Data (Any C) to Any Y	t_{PLH}	$C_L = 50pF$	10		18		21	ns
		$C_L = 150pF$	13		23		27	
	t_{PHL}	$C_L = 50pF$	10		18		21	
		$C_L = 150pF$	13		23		27	
Output Enable Time, $\overline{G}$ to Y	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$	10		16		19	ns
		$R_L = 1k\Omega$, $C_L = 150pF$	13		21		25	
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$	10		16		19	
		$R_L = 1k\Omega$, $C_L = 150pF$	13		21		25	
Output Disable Time, $\overline{G}$ to Y	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	10		18		22	ns
	t_{PLZ}		10		18		22	
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

These high-speed Hex bus drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus oriented receivers and transmitters.

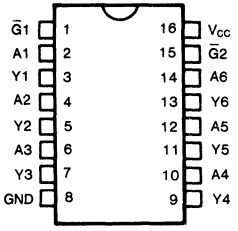
The '365 and '366 have two output enables ($\overline{G}1$ and $\overline{G}2$) NOR'ed together to control all six gates. The '367 and '368 have two output enables which are configured so that one enable ($\overline{G}1$) controls four gates and the other ($\overline{G}2$) controls the remaining two gates. The '366 and '368 have inverting data paths. The '365 and '367 have noninverting data paths.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

4

PIN CONFIGURATION



FUNCTION TABLES

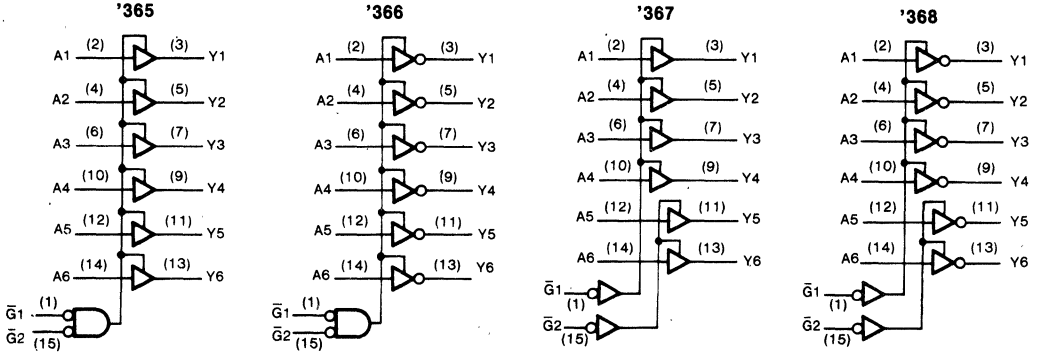
'365 and '356

Inputs			Y Outputs	
$\overline{G}1$	$\overline{G}2$	A	'365	'366
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

'367 and '368

Inputs		Y Outputs	
G1 & G2	A	'367	'368
L	L	L	H
L	H	H	L
H	X	Z	Z

LOGIC DIAGRAMS



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} +0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} +0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} +0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT365, AHCT366, AHCT367, AHCT368

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A to Y,	t_{PLH}	$C_L = 50pF$	8		14		17	ns
		$C_L = 150pF$	11		19		33	
	t_{PHL}	$C_L = 50pF$	8		14		17	
		$C_L = 150pF$	11		19		33	
Output Enable Time, $\overline{G}$ to Y	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$	14		23		28	ns
		$R_L = 1k\Omega$, $C_L = 150pF$	17		28		34	
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$	14		23		28	
		$R_L = 1k\Omega$, $C_L = 150pF$	17		28		34	
Output Disable Time, $\overline{G}$ to Y	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	15		20		22	ns
	t_{PLZ}		15		20		22	
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per driver)	C_{PD}	$\overline{G} = V_{CC}$ / $\overline{G} = GND$	5					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

Octal D-Type Transparent Latches with 3-State Outputs

FEATURES

- 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

The '373 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

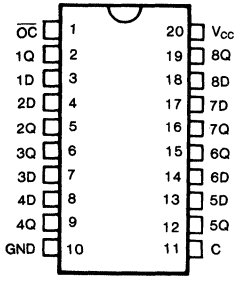
The latches are transparent: when the enable (C) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs at a high-impedance state when it is taken high. The $\overline{OC}$ signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

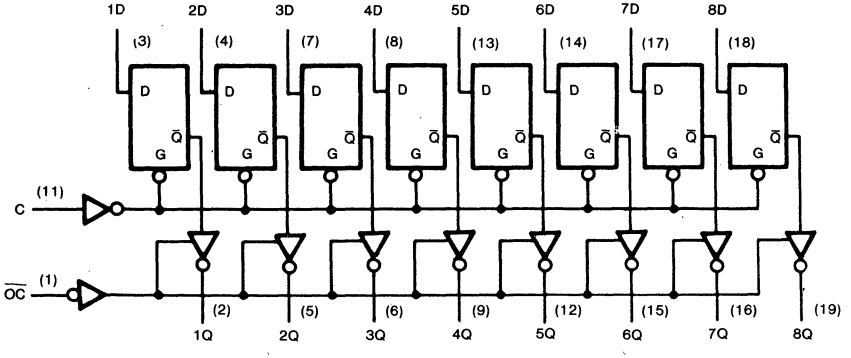


FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	Enable C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT373

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay, D to Q	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$		8 11		14 19		17 23	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$		8 11		14 19		17 23	
Propagation Delay, C to Q	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$		14 17		23 28		27 33	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$		14 17		23 28		27 33	
Output Enable Time, $\overline{OC}$ to any Q	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$ $C_L = 150pF$	12 15		20 25		24 30	ns
	t_{PZL}		$C_L = 50pF$ $C_L = 150pF$	12 15		20 25		24 30	
Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	$R_L = 1k\Omega$ $C_L = 50pF$		13		18		22	ns
	t_{PLZ}			13		18		22	
Pulse Width, C High	t_w			9	15		18		ns
Setup Time, D before C↓	t_{SU}			6	10		10		ns
Hold Time, D after C↓	t_h			3	5		7		ns
Input Capacitance	C_{IN}			5					pF
Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance* (per latch)	C_{PD}	$\overline{OC} = V_{CC}$ $\overline{OC} = GND$		5 30					pF

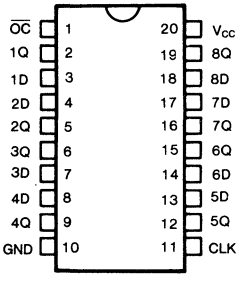
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Octal D-Type Flip-Flops with 3-State Outputs

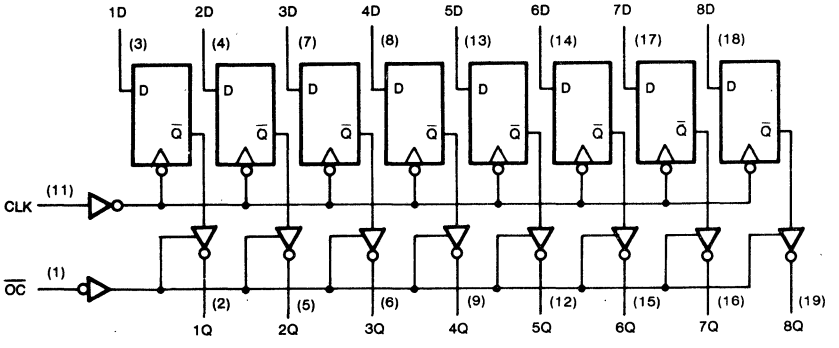
FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



LOGIC DIAGRAM



DESCRIPTION

The '374 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs at a high-impedance state when it is taken high. The OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT374

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Operating Frequency	f_{max}	C_L= 50pF		50	35		30		MHz
Propagation Delay, CLK to any Q	t_{PLH}	C_L= 50pF C_L=150pF		8 11		14 19		17 23	ns
	t_{PHL}	C_L= 50pF C_L=150pF		8 11		14 19		17 23	
Output Enable Time, $\overline{OC}$ to any Q	t_{PZH}	R_L=1kΩ	C_L= 50pF C_L=150pF	11 14		18 23		22 28	ns
	t_{PZL}		C_L= 50pF C_L=150pF	11 14		18 23		22 28	
Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	R_L=1kΩ C_L=50pF		13		18		22	ns
	t_{PLZ}			13		18		22	
Pulse Width, CLK High or Low	t_w			7	15		18		ns
Setup Time, D before CLK↑	t_{su}			9	14		13		ns
Hold Time, D after CLK↑	t_h			−3	0		0		ns
Input Capacitance	C_{IN}			5					pF
Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance*		$\overline{OC}$=V_{CC} $\overline{OC}$=GND (per stage)		5 30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

Octal D-Type Flip-Flops with Clock Enable

FEATURES

- **Can be used for implementing**
  - **— Buffer/Storage Registers**
  - **— Shift Registers**
  - **— Pattern Generators**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

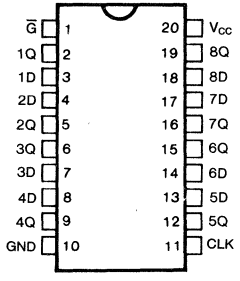
The '377 contains eight positive-edge-triggered D-type flip-flops with an enable input. This part is similar to '273 but features a latched clock enable ($\overline{G}$) instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitioins at the $\overline{G}$ input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

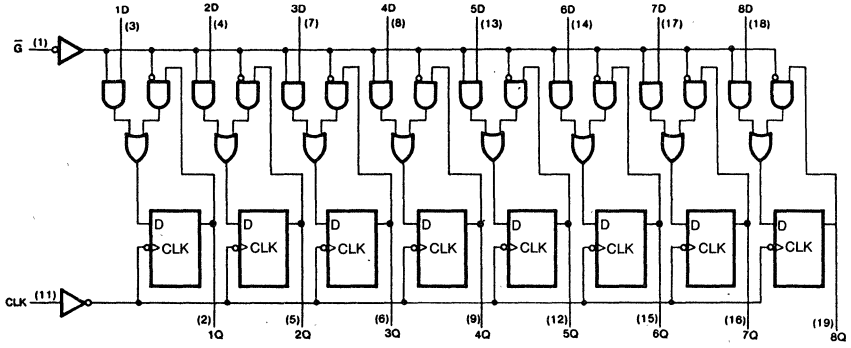


FUNCTION TABLE

(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{G}$	CLK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT377

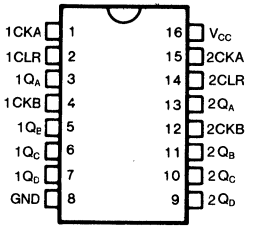
Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}		50	35		30		MHz
Propagation Delay, CLK to any Q		t_{PLH}	$C_L = 50pF$	10		16		19	ns
		t_{PHL}		10		16		19	
Pulse Width	$\overline{G}$ Low	t_w		8	14		17		ns
	CLK High or Low			8	14		17		
Setup time before CLK↑	Data	t_{su}		6	10		10		ns
	$\overline{G}$ High or Low			9	15		15		
Hold Time, Data after CLK↑		t_h		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	per package	50					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Individual clock for A and B flip-flops provide dual ÷2 and ÷5 counters**
- **Direct clear for each 4-bit counter**
- **Significant improvement in system density through reduced counter package count.**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: (I_{OL} = 8 mA @ V_{OL} = 0.5V)**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74HCTLS: −40°C to +85°C KS54HCTLS: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These devices incorporate dual divide-by-two and divide-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiple of 2 and/or 5 up to divide-by-100. When conneoted as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square ware) at the final outpur stage. The '390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-tow circuit can be used to provide symmetry (a square wave) at the final outpur stage. The '390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

4

FUNCTION TABLES

BCD COUNT SEQUENCE (EACH COUNTER) (See Note A)

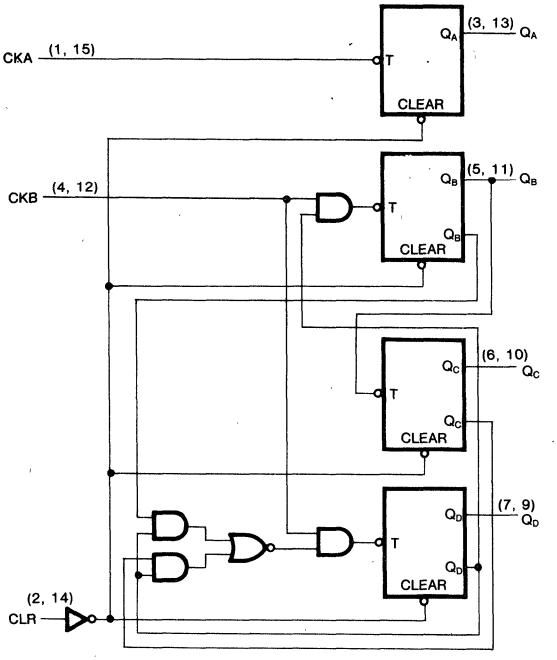
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BIQUINARY (5-2) (EACH COUNTER) (See Note B)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES A. Output Q_A is connected to input $\overline{CKB}$ for BCD count.
B. Output Q_D is connected to input $\overline{CKA}$ for biquinary count.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT390

Characteristic		Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay, CKA to Q_A or CKB to Q_B		f_{max}	C_L=50pF	50	30		25		MHz
Propagation Delay, CKA to Q_A		t_{PLH}		9		15		18	ns
		t_{PHL}		9		15		18	ns
Propagation Delay, CKA to Q_C		t_{PLH}		24		40		48	ns
		t_{PHL}		24		40		48	ns
Propagation Delay, CKB to Q_B		t_{PLH}		10		17		21	ns
		t_{PHL}		10		17		21	ns
Propagation Delay, CKB to Q_C		t_{PLH}		16		27		33	ns
		t_{PHL}		16		27		33	ns
Propagation Delay, CKB to Q_D		t_{PLH}		10		17		21	ns
		t_{PHL}		10		17		21	ns
Propagation Delay, CLR to Any Q		t_{PHL}		14		24		29	ns
Pulse Width	CKA or CKB High or Low	t_w		7	12		15		ns
	CLR High			7	12		15		
Minimum Setup Time, CLR inactive before CKA or CKB		t_{SU}		5	8		10		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capocitance		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

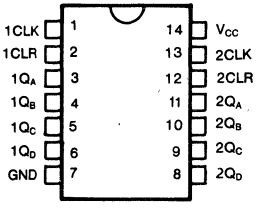
DESCRIPTION

The '393 consists of two independent 4-bit binary counters each with its own clear and clock inputs. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. parallel outputs from each counter stage provided any submultiple of the input count frequency for system timing signals.

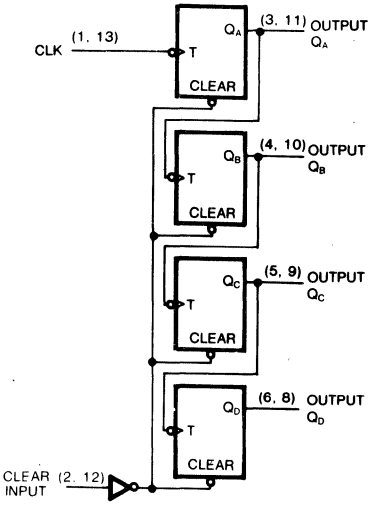
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

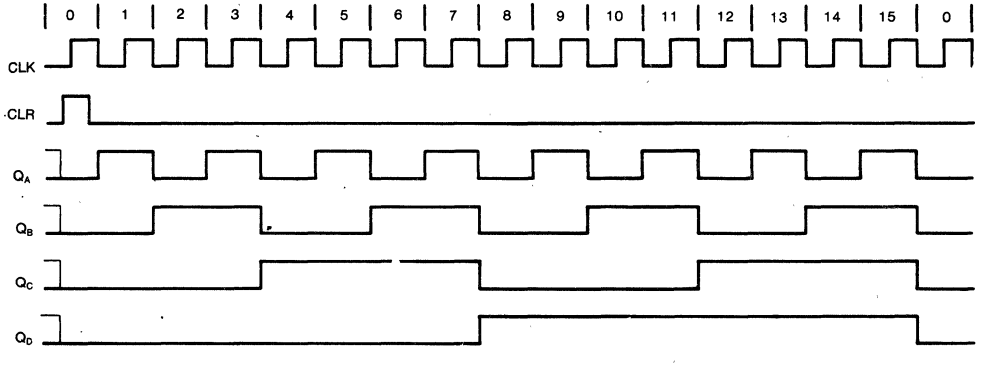
PIN CONFIGURATION



LOGIC DIAGRAM



LOGIC TIMING WAVEFORMS



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT393

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	C_L=50pF	50	30		25		MHz
Propagation Delay, A to Q_A		t_{PLH}		14		22		26	ns
		t_{PHL}		14		22		26	
Propagation Delay, A to Q_B		t_{PLH}		18		27		32	ns
		t_{PHL}		18		27		32	
Propagation Dealy, A to Q_C		t_{PLH}		20		33		40	ns
		t_{PHL}		20		33		40	
Propagation Delay, A to Q_D		t_{PLH}		26		40		48	ns
		t_{PHL}		26		40		48	
Propagation Dealy, CLR to any Q		t_{PHL}		15		25		30	ns
Pulse Width	A Input High or Low	t_w		7	12		15		ns
	CLR High			7	12		15		
Setup Time, CLR Inactive before A		t_{su}		5	8		10		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per counter)	40					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

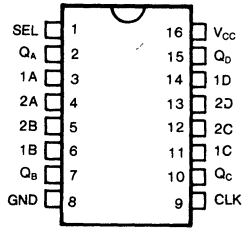
DESCRIPTION

These are high-speed quad 2-port registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A common select input (SEL) selects between two 4-bit input ports. The selected data is transferred to the output register on the low-to-high transition of the clock input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

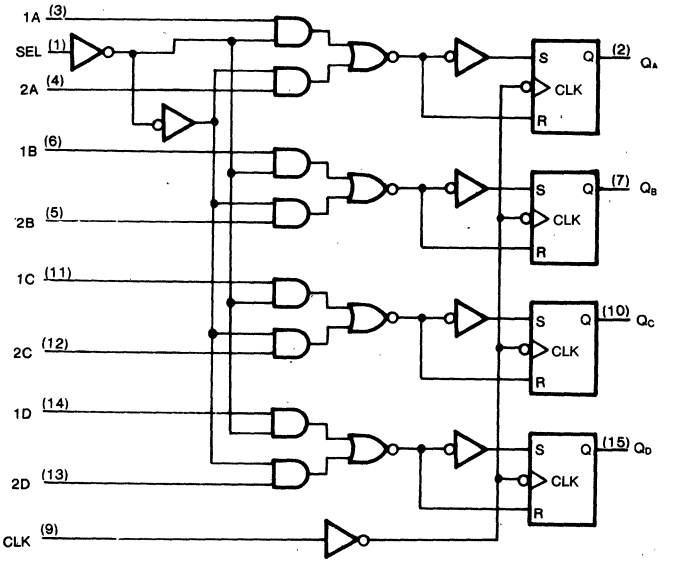


FUNCTION TABLE

Inputs			Output
SEL	**Port 1**	**Port 2**	**Q**
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

l = Low Voltage Level one setup time prior to the low-to-high clock transition
h = High Voltage Level one setup time prior to the low-to-high clock transition

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT399

Characteristic		Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74AHCT T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay, CLK to $\overline{Q}$		t_{PLH}	C_L=50pF	12		19		23	ns
		t_{PHL}		12		19		23	
Pulse Width, CLK High or Low		t_w		6	10		15		ns
Time before CLK↑	Data	t_{su}		6	10		15		ns
	Word Select			6	10		15		
Hold Time, Data after CLK↑		t_h		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

KS54AHCT 423
KS74AHCT

Dual Retriggerable Monostable Multivibrator with Clear

Preliminary Specifications

FEATURES

- **Simple pulse width formula $t_W = 0.45RC$**
- **DC triggered from active HIGH or active Low inputs**
- **Retriggerable for very long output pulses up to 100% duty cycle**
- **Overriding clear terminates output pulse**
- **Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs**
- **Functions, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High drive current outputs: $I_{OL} = 8mA$ @ $V_{OL} = 0.5V$**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range; 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74AHCT: −40°C to +85°C KS54AHCT: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '423 contains dual retriggerable monostable multivibrators with output pulsewidth control by two methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low-going edge input (Ai) or the active High-going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH, $n\overline{Q}$=LOW) can be made as long as desired.

Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques.

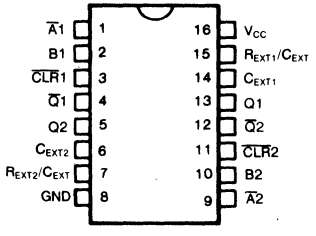
The output pulse equation is simply;

$t_W = 0.45 \times (R_{EXT})\ (C_{EXT})$

Where t_w is in seconds. R is in ohm. and C is in fards.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Outputs	
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

H= HIGH voltage level
L= LOW voltage level
X= don't care
↑= LOW to HIGH transition
↓= HIGH to LOW transition
⎍= one HIGH level output pulse
⎎= one LOW level output pulse

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I<−0.5V or V_I>V_{CC}+0.5V) ..... ±20 mA
DC Output Diode Current, I_{Ok}
(V_O<−0.5V or V_O>V_{CC}+0.5V) ..... ±20 mA
Continuous OUtput Current Per Pin, I_O
(−0.5V<V_O<V_{CC}+0.5V) ..... ±35 mA
Continuous Current Through
V_{CC} or GND pins ..... ±125 mA
Storage Temperature Range, T_{stg} −65°C to +150°C
Power Dissipation Per Package, P_d† ..... 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package(N): −12mW/°C from 65°C to 85°C
Ceramic Package(J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} ..... 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f ..... Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT423

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	$C_L = 50pF$ $C_{ext} = 0$, $R_{ext} = 5k\Omega$	18		33		40	ns
$\overline{A}$, B to Q, $\overline{Q}$	t_{PHL}		18		33		40	
Propagation Delay	t_{PLH}		16		27		33	ns
$\overline{CLR}$ to Q, $\overline{Q}$	t_{PHL}		16		27		33	
Output Pulse Width 1	t_{WQ1}		116		207		209	ns
Output Pulse Width 2	t_{WQ2}	$C_L = 50pF$ $C_{ext} = 1000pF$ $R_{ext} = 10k\Omega$	4.5	3.8	5.2	3.8	5.2	μs
Trigger Pulse Width	t_w	$C_L = 50pF$ $A_i = LOW$	5		16		20	ns
Trigger Pulse Width	t_w	$C_L = 50pF$ $B_i = High$	5		16		20	ns
Clear Pulse Width	t_w	$C_L = 50pF$ $CLR_i = LOW$	6		16		20	ns
External Timing Resistance	R_{ext}			2	1,000	2	1,000	kΩ
External Timing Capacitance	C_{in}		no restriction					
Input Capacitance	C_{in}		5					pF
Power Dissipation Capacitance	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Application Information

The basic output pulse width is determined by the value of external capacitance and timing resistance.
For output pulse widths greater than 100μs or external capacitance greater than 1000pF the following equation should be used.

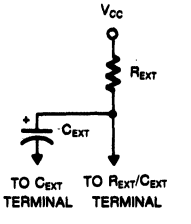
$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

t_w is in second
K is the multiplying factor
and is approximately 0.45 for $C_{ext} \geq 1000pF$
C_{ext} is in F

For best results, system ground should be applied to the C_{ext} terminal. These devices do not require a switching diode in series with the R_{ext}/C_{ext} terminal (as required by some other monostable multivibrators)

TIMING COMPONENT



Octal Buffers and Line Drivers with 3-State Outputs

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

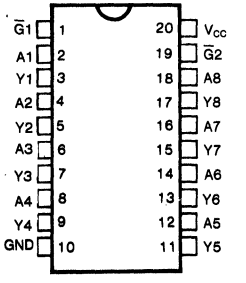
These high-speed octal buffers and drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has the choice of inverting/ noninverting outputs and various types of output controls.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

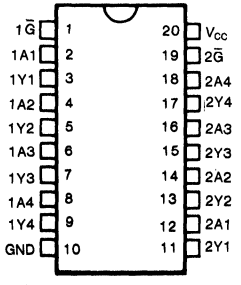
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS

'465 and '466



'467 and '468



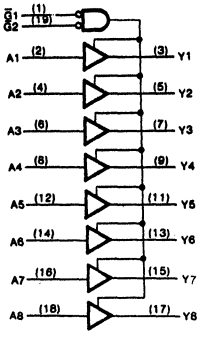
FUNCTION TABLE

Input			Output	
$\overline{G}_1$	$\overline{G}_2$	A	'465	'466
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

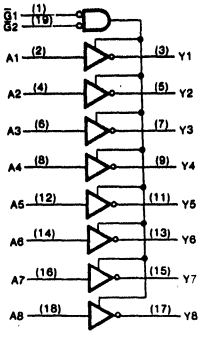
Input			Output	
G	$\overline{G}$	A	'467	'468
H	L	L	L	H
H	L	H	H	L
L	H	X	Z	Z

LOGIC DIAGRAMS

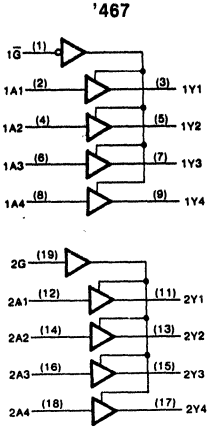
'465



'466



'467



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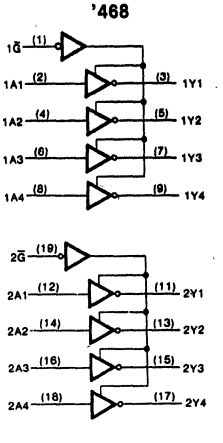


Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT465, AHCT466, AHCT467, AHCT468

Parameter	Symbol	Conditions	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		54AHCT $T_a = +55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A to Y	t_{PLH}	$C_L = 50pF$	7		12		14	ns
		$C_L = 150pF$	10		17		20	
	t_{PHL}	$C_L = 50pF$	7		12		14	
		$C_L = 150pF$	10		17		20	
Output Enable Time, Enable to Y	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$	12		20		24	ns
		$C_L = 150pF$	15		25		30	
	t_{PZL}	$C_L = 50pF$	12		20		24	
		$C_L = 150pF$	15		25		30	
Output Disable Time, Enable to Y	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	13		18		22	ns
	t_{PLZ}		13		18		22	
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	Output Disabled	5					pF
		Output Enabled	30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
For AC switching test circuits and timing waveforms see section 2.

4

FEATURES

- **Compares two 8-bit words**
- **'518, '520 and 522 have 20kΩ pull-up Resistors on Q Inputs**

TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
'518	Yes	P=Q Open-Drain
'519	No	P=Q Open-Drain
'520	Yes	$\overline{P=Q}$ Totem-Pole
'521	No	$\overline{P=Q}$ Totem-Pole
'522	Yes	$\overline{P=Q}$ Open-Drain

† '521 is identical to '688

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

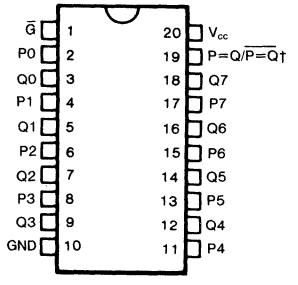
DESCRIPTION

These identity comparators perform comparisons on two eight-bit binary or BCD words. The '518 and '519 provide P=Q outputs, while the '520, 521, and '522 provide $\overline{P=Q}$ outputs. The '518, '519, and '522 have open-drain outputs. The '518, '520, and '522 feature 20-kΩ inputs for analog or switch data.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



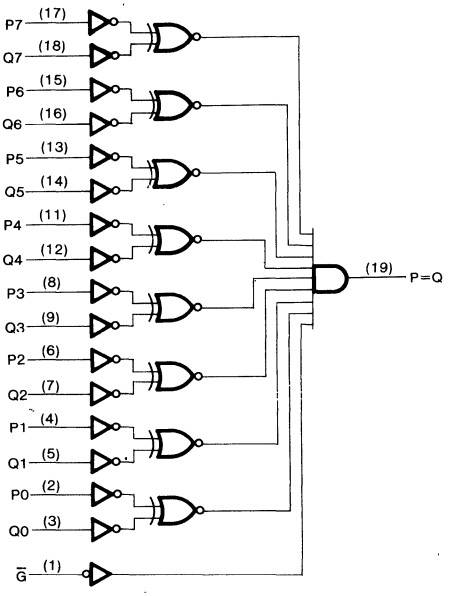
† P=Q for '518 and '519;
$\overline{P=Q}$ for '520, '521, '522.

FUNCTION TABLE

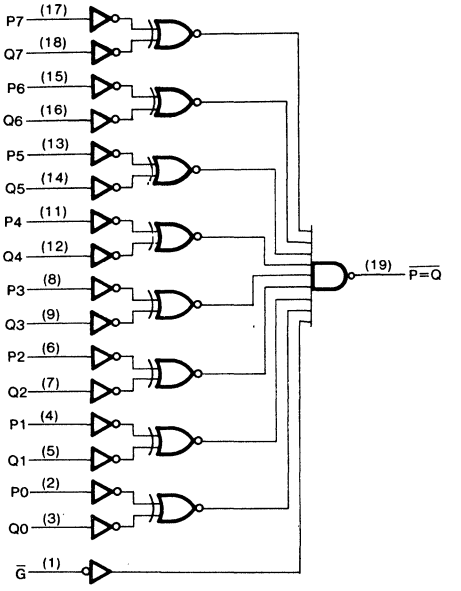
INPUTS		OUTPUTS	
DATA P, Q	ENABLE $\overline{G}$	P=Q	$\overline{P=Q}$
P=Q	L	H	L
P>Q	L	L	H
P<Q	L	L	H
X	H	L	H

LOGIC DIAGRAMS

'518/'519



'520/'521/'522



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

4

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Parameter	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_A=−40°C to +85°C	54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (Totem-pole Outputs)	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.93	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage (All Outputs)	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current, ('518, '520 and '522 Q input)		V_{CC}=Max V_{IN}=2.7V V_{IN}=0.4V		−0.2 −0.6	−0.2 −0.6	−0.2 −0.6	mA
Maximum Input Current (All other Inputs)	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current (Open-Drain Outputs)	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	For '518, '520 and '522: V_{IN}=GND (Q0-Q7) V_{IN}=V_{CC} or GND (all other inputs)		3.5	3.5	3.5	mA
		For '519 and '521: V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT518, AHCT519

Characteristic	Symbol	Conditions	54/74ACHT $T_a = 25°C$ $V_{CC} = 5V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5V \pm 10\%$		54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typical	Min	Max	Min	Max	
Propagation Delay, P or Q to P=Q	t_{PLH}	$C_L = 50pF$	20		30		35	ns
		$C_L = 150pF$	23		35		41	
	t_{PHL}	$C_L = 50pF$	15		25		30	
		$C_L = 150pF$	18		30		36	
Propagation Delay, $\overline{G}$ to P=Q	t_{PLH}	$C = 50pF$	16		23		27	ns
		$C_L = 150pF$	19		28		33	
	t_{PHL}	$C_L = 50pF$	11		18		22	
		$C_L = 150pF$	14		23		28	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT520, AHCT521

Characteristic	Symbol	Conditions	54/74ACHT $T_A = 25°C$ $V_{CC} = 5V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5V \pm 10\%$		54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typical	Min	Max	Min	Max	
Propagation Delay, P or Q to $\overline{P}=\overline{Q}$	t_{PLH}	$C_L = 50pF$	12		19		23	ns
		$C_L = 150pF$	15		24		29	
	t_{PHL}	$C_L = 50pF$	12		19		23	
		$C_L = 150pF$	15		24		29	
Propagation Delay, $\overline{G}$ to $\overline{P}=\overline{Q}$	t_{PLH}	$C = 50pF$	11		17		20	ns
		$C_L = 150pF$	14		22		26	
	t_{PHL}	$C_L = 50pF$	11		17		20	
		$C_L = 150pF$	14		22		26	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHC522

Characteristic	Symbol	Conditions	54/74ACHT $T_A = 25°C$ $V_{CC} = 5V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5V \pm 10\%$		54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typical	Min	Max	Min	Max	
Propagation Delay, P or Q to $\overline{P}=\overline{Q}$	t_{PLH}	$C_L = 50pF$	19		28		33	ns
		$C_L = 150pF$	22		33		39	
	t_{PHL}	$C_L = 50pF$	14		23		28	
		$C_L = 150pF$	17		28		34	
Propagation Delay, $\overline{G}$ to $\overline{P}=\overline{Q}$	t_{PLH}	$C = 50pF$	16		23		27	ns
		$C_L = 150pF$	19		28		33	
	t_{PHL}	$C_L = 50pF$	11		18		22	
		$C_L = 150pF$	14		27		33	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Octal D-Type Transparent Latches with 3-State Outputs

FEATURES

- **8 latches in a single package**
- **Full parallel access for loading**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '533 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

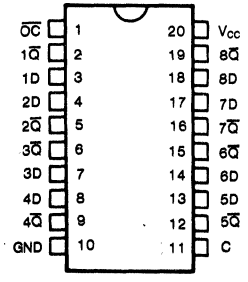
The latches are transparent: when the enable (C) is high, the $\overline{Q}$ outputs follow the complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs at high-impedance state when it is taken high. The $\overline{OC}$ signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

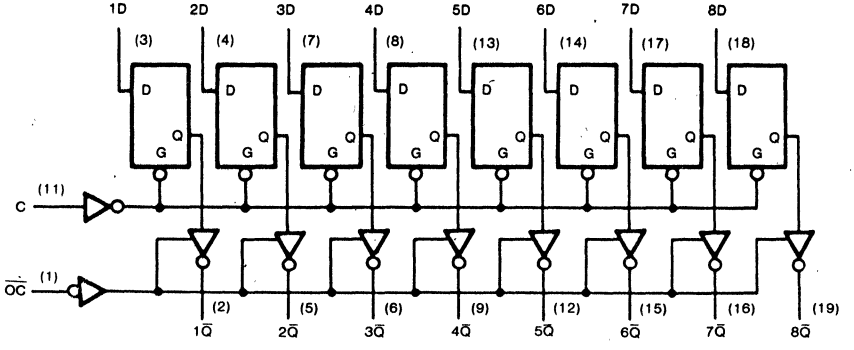


FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	Enable C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} . . . . . −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT533

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, D to $\overline{Q}$	t_{PLH}	$C_L = 50pF$	10		16		19	ns
		$C_L = 150pF$	13		21		25	
	t_{PHL}	$C_L = 50pF$	10		16		19	
		$C_L = 150pF$	13		21		25	
Propagation Delay, C to $\overline{Q}$	t_{PLH}	$C = 50pF$	13		21		25	ns
		$C_L = 150pF$	16		26		31	
	t_{PHL}	$C_L = 50pF$	13		21		25	
		$C_L = 150pF$	16		26		31	
Output Enable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$	11		18		22	ns
		$R_L = 1k\Omega$, $C_L = 150pF$	14		23		28	
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$	11		18		22	
		$R_L = 1k\Omega$, $C_L = 150pF$	14		23		28	
Output Disable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	13		18		22	ns
	t_{PLZ}		13		18		22	
Pulse Width, C High	t_w		9	15		18		ns
Setup Time, D before C↓	t_{su}		9	15		18		ns
Hold Time, D after C↓	t_h		3	5		7		ns
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{out}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC} = V_{CC}$	5					pF
		$\overline{OC} = GND$	30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Octal D-Type Flip-Flops with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '534 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

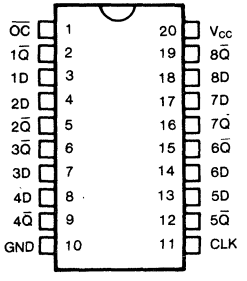
The flip-flops are edge-triggered on the positive transition of the clock: the $\overline{Q}$ outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs in high-impedance state when it is taken high, the OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

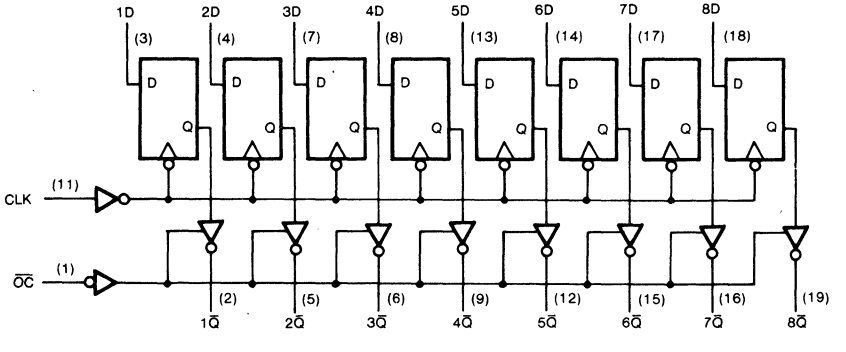


FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	 V_{CC} 4.2	 V_{CC} −0.1 3.98	 V_{CC} −0.1 3.84	 V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	 0	 0.1 0.26 0.39	 0.1 0.33 0.5	 0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT534

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Operating Frequency	f_{max}	$C_L = 50pF$	50	35		30		MHz
Propagation Delay, CLK to any $\overline{Q}$	t_{PLH}	$C_L = 50pF$	8		14		17	ns
		$C_L = 150pF$	11		19		23	
	t_{PHL}	$C_L = 50pF$	8		14		17	
		$C_L = 150pF$	11		19		23	
Output Enable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$	11		18		22	ns
		$R_L = 1k\Omega$, $C_L = 150pF$	14		23		28	
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$	11		18		22	
		$R_L = 1k\Omega$, $C_L = 150pF$	14		23		28	
Output Disable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	13		18		22	ns
	t_{PLZ}		13		18		22	
Pulse Width, CLK High or Low	t_w		9	15		18		ns
Setup Time, D before CLK↑	t_{su}		9	14		17		ns
Hold Time, D after CLK↑	t_h		−3	0		0		ns
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC} = V_{CC}$	5					pF
		$\overline{OC} = GND$	30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

4

KS54AHCT 540/541
KS74AHCT

Octal Buffers and Line Drivers with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

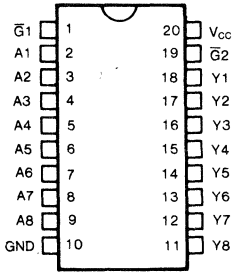
The '540 and '541 are general purpose high-speed octal line drivers/buffers with 3-state outputs. The inputs and outputs are located on opposite sides of the 20-pin package, thus improving circuit board density. The '540 provides inverted data and the '541 provides true data at the outputs.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high impedance state.

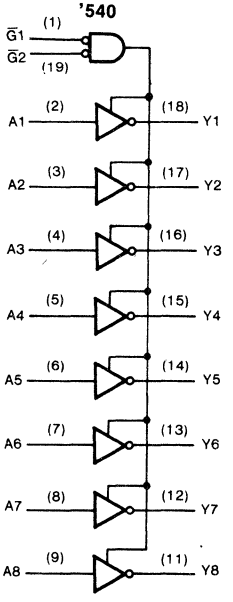
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

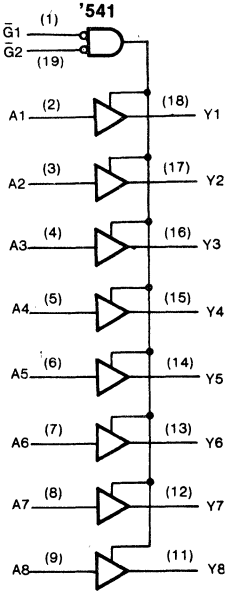
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAMS





FUNCTION TABLE

Input			Output	
$\overline{G}_1$	$\overline{G}_2$	A	'540	'541
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT540, AHCT541

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay, A to Y	t_{PLH}	C_L= 50pF		7		12		14	ns
		C_L=150pF		10		17		20	
	t_{PHL}	C_L= 50pF		7		12		14	
		C_L=150pF		10		17		20	
Output Enable Time, $\overline{G}$ to Y	t_{PZH}	R_L=1kΩ	C_L= 50pF	12		20		24	ns
			C_L=150pF	15		25		30	
	t_{PZL}		C_L=50pF	12		20		24	
			C_L=50pF	15		25		30	
Output Disable Time $\overline{G}$ to Y	t_{PHZ}	R_L=1kΩ C_L=50pF		14		19		23	ns
	t_{PLZ}			14		19		23	
Input Capacitance	C_{IN}			5					pF
Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{G}=V_{CC}$		5					pF
		$\overline{G}$=GND		30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Octal D-Type Transparent Latches with 3-State Outputs

FEATURES

- **8 latches in a single package**
- **Full parallel access for loading**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to + 85°C
  KS54AHCT: −55°C to + 125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

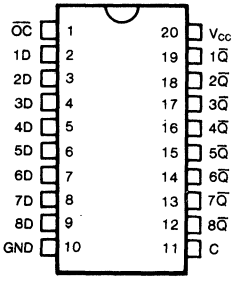
The '563 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer register, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (C) is high, the Q outputs follow complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at a high-impedance stage when it is taken high. The OC signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

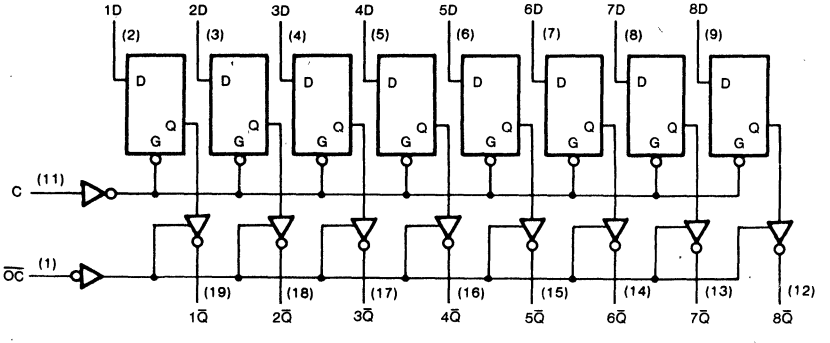


FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	Enable C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT563

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay, D to $\overline{Q}$	t_{PLH}	C_L= 50pF		12		18		22	ns
		C_L=150pF		15		23		28	
	t_{PHL}	C_L= 50pF		12		18		22	
		C_L=150pF		15		23		28	
Propagation Delay, C to $\overline{Q}$	t_{PLH}	C= 50pF		14		22		27	ns
		C_L=150pF		17		27		33	
	t_{PHL}	C_L= 50pF		14		22		27	
		C_L=150pF		17		27		33	
Output Enable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PZH}	R_L=1kΩ	C_L= 50pF	11		18		22	ns
			C_L=150pF	14		23		28	
	t_{PZL}		C_L= 50pF	11		18		22	
			C_L=150pF	14		23		28	
Output Disable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PHZ}	R_L=1kΩ		13		19		22	ns
	t_{PLZ}	C_L=50pF		13		19		22	
Pulse Width, C High	t_w			9	15		18		ns
Setup Time, D before C↓	t_{su}			6	10		10		ns
Hold Time, D after C↓	t_h			3	5		7		ns
Input Capacitance	C_{IN}			5					pF
Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC}$=V_{CC}		5					pF
		$\overline{OC}$=GND		30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

4

Octal D-Type Flip-Flops with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C + 85°C
  KS54HACT: −55°C + 125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '564 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

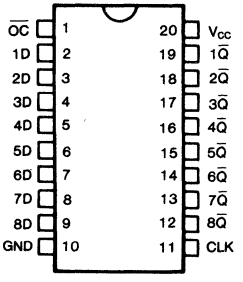
The flip-flops are edge-triggered: on the positive transition of the clock, the $\bar{Q}$ outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs at high impedance stat when it is taken high. The OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

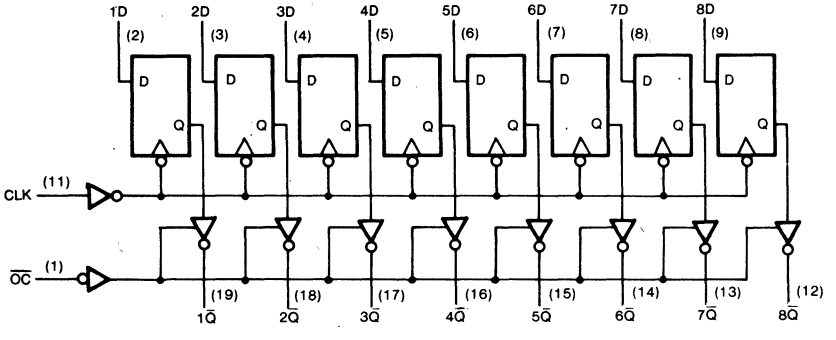


FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
$\overline{OC}$	CLK	D	$\bar{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT564

Characteristic	Symbol	Conditions†		T_a = 25°C, V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C, V_{CC} = 5.0V ± 10%		KS54AHCT T_a = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Unit
				Typ	Min	Max	Min	Max	
Maximum Operating Frequency	f_{max}	C_L = 50pF		50	35		30		MHz
Propagation Delay, CLK to any $\overline{Q}$	t_{PLH}	C_L = 50pF C_L = 150pF		8 11		14 19		17 23	ns
	t_{PHL}	C_L = 50pF C_L = 150pF		8 11		14 19		17 23	
Output Enable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PZH}	R_L = 1kΩ	C_L = 50pF C_L = 150pF	11 14		18 23		22 28	ns
	t_{PZL}		C_L = 50pF C_L = 150pF	11 14		18 23		22 28	
Output Disable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PHZ}	R_L = 1kΩ C_L = 50pF		13		19		22	ns
	t_{PLZ}			13		19		28	
Pulse Width, CLK High or Low	t_w			9	15		18		ns
Setup Time, D before CLK↑	t_{su}			9	14		17		ns
Hold Time, D after CLK↑	t_h			−3	0		0		ns
Input Capacitance	C_{IN}			5					pF
Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC}$ = V_{CC} $\overline{OC}$ = GND		5 30					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

Octal D-Type Transparent Latches with 3-State Outputs

FEATURES

- 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compability with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface direcity with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74AHCT: −40°C to + 85°C
  KS54HACT: −40°C to + 125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

The '573 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing bufer registers, I/O ports, bidirectional bus drivers and working registers.

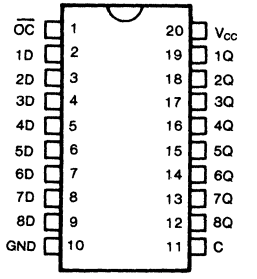
The latches are transparent: when the enable (C) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at a high-impedance state when it is taken high. The $\overline{OC}$ signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

There devices provide speeds and drive capability equivalent ot their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

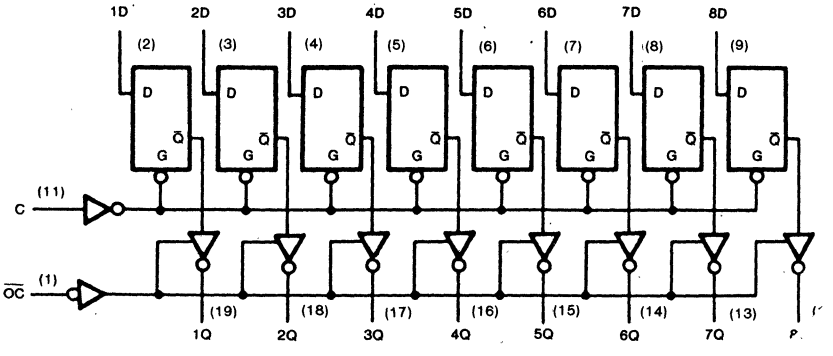


FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	Enable C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT573

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, D to Q	t_{PLH}	C_L= 50pF	9		14		17	ns
		C_L=150pF	12		19		23	
	t_{PHL}	C_L= 50pF	9		14		17	
		C_L=150pF	12		19		23	
Propagation Delay, C to Q	t_{PLH}	C=50pF	12		20		24	ns
		C_L=150pF	15		25		30	
	t_{PHL}	C_L= 50pF	12		20		24	
		C_L=150pF	15		25		30	
Output Enable Time $\overline{OC}$ to any Q	t_{PZH}	R_L=1kΩ, C_L= 50pF	11		18		22	ns
		R_L=1kΩ, C_L=150pF	14		23		28	
	t_{PZL}	R_L=1kΩ, C_L= 50pF	11		18		22	
		R_L=1kΩ, C_L=150pF	14		23		28	
Output Disable Time $\overline{OC}$ to any Q	t_{PHZ}	R_L=1kΩ, C_L=50pF	13		19		22	ns
	t_{PLZ}		13		19		22	
Pulse Width, C High	t_w		9	15		18		ns
Setup Time, D before C↓	t_{su}		6	10		12		ns
Hold Time, D after C↓	t_h		4	7		9		ns
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC}$=V_{CC}	5					pF
		$\overline{OC}$=GND	30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Octal D-Type Flip-Flops with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '574 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

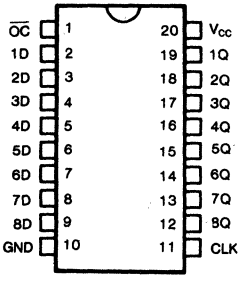
The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs at a high-impedance state when it is taken high. The $\overline{OC}$ signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

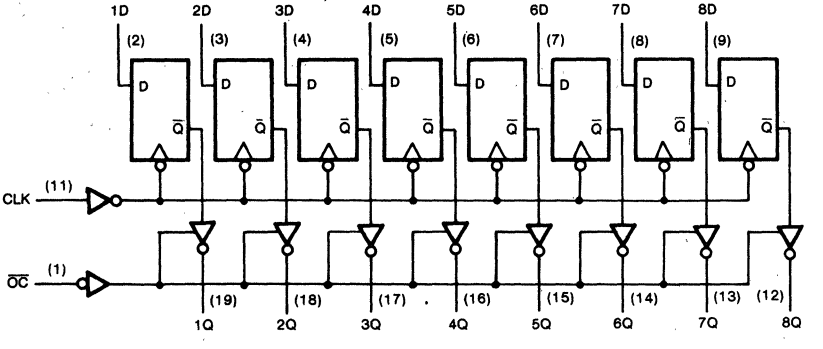


FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT574

Characteristic	Symbol	Conditions†	$T_a = 25°C$, $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Operating Frequency	f_{max}	C_L= 50pF	50	35		30		MHz
Propagation Delay, CLK to any Q	t_{PLH}	C_L= 50pF C_L=150pF	8 11		14 19		17 23	ns
	t_{PHL}	C_L= 50pF C_L=150pF	8 11		14 19		17 23	
Output Enable Time, $\overline{OC}$ to any Q	t_{PZH}	R_L=1kΩ, C_L= 50pF R_L=1kΩ, C_L=150pF	11 14		18 23		22 28	ns
	t_{PZL}	R_L=1kΩ, C_L= 50pF R_L=1kΩ, C_L=150pF	11 14		18 23		22 28	
Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	R_L=1kΩ, C_L=50pF	13		18		22	ns
	t_{PLZ}		13		18		22	
Pulse Width, CLK High or Low	t_w		9	15		18		ns
Setup Time, D before CLK↑	t_{su}		9	14		17		ns
Hold Time, D after CLK↑	t_h		−3	0		0		ns
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC}$=V_{CC} $\overline{OC}$=GND	5 30					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

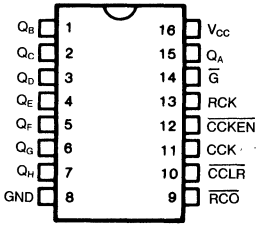
† For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

FEATURES

- **Choice of 3-State ('590) and Open-Drain ('591) Outputs**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These devices each consist of an 8-bit binary counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{CCKEN}$, is low. When the counter increments to the all ones condition, ripple carry out, $\overline{RCO}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{RCO}$ of the first stage to the $\overline{CCKEN}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the $\overline{RCO}$ of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed the outputs which are enabled when the enable input, $\overline{G}$, is taken low. This enables connection of this part to a system bus. The Q outputs of the '590 are 3-State and those for '591 are Open-drain.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

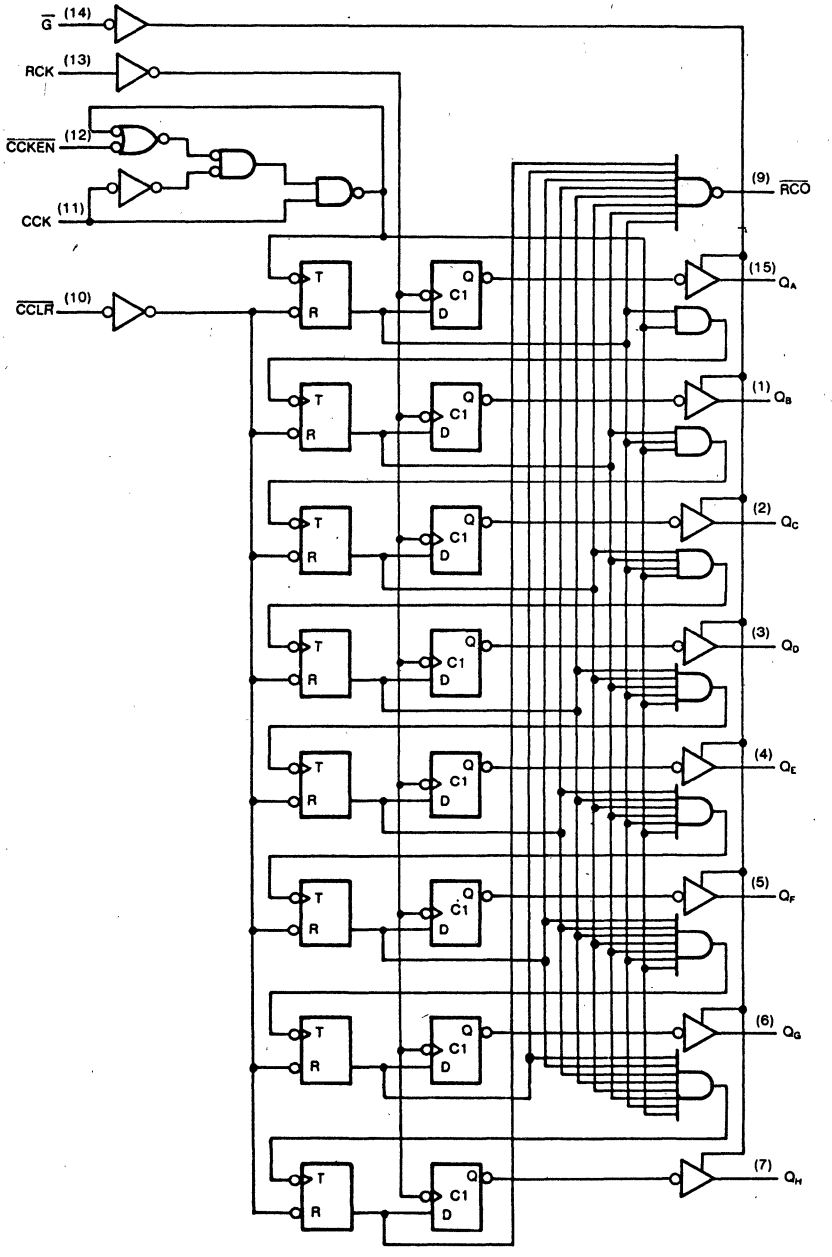
INPUTS					FUNCTION
$\overline{G}$	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q Outputs disable
L	X	X	X	X	Q Outputs enable
L	↑	X	X	X	Counter data is stored into register
L	↓	X	X	X	Register state is not changed
L	X	L	X	X	Counter clear
L	X	H	L	↑	Advance one count
L	X	H	L	↓	No count
L	X	H	H	X	No count

X: Don't care

$$\overline{RCO} = \overline{Q_A' \cdot Q_B' Q_C' \cdot Q_D' Q_E' \cdot Q_F' Q_G' \cdot Q_H'}$$

($Q_A' \sim Q_H'$: Internal outputs of the counter)

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (All '590 Outputs and '591 $\overline{RCO}$ Output)	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC}		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT590

Characteristic		Symbol	Conditions†	54/74ACHT $T_a = 25°C$ $V_{CC} = 5V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5V \pm 10\%$		54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typical	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	50	30		25		ns
Propagation Delay, CCK↑ to $\overline{RCO}$		t_{PLH}		15		25		29	ns
		t_{PHL}		15		25		29	
Propagation Delay, $\overline{CCLR}$↓ to $\overline{RCO}$		t_{PHL}		17		28		33	ns
Propagation Delay, RCK↑ to Q		t_{PLH}		10		16		19	ns
		t_{PHL}		10		16		19	
Output Enable Time, $\overline{G}$↓ to Q		t_{PZH}	$C_L = 50pF$ $R_L = 1K\Omega$	13		18		22	ns
		t_{PZL}		13		18		22	
Output Disable Time, $\overline{G}$↑ to Q		t_{PHZ}		13		18		22	ns
		t_{PLZ}		13		18		22	
Pulse Duration	CCK or RCK High or Low	t_w		10	15		20		ns
	$\overline{CCLR}$ Low			10	15		20		
Setup Time	$\overline{CCKEN}$↓ before CCK↑	t_{su}		10	15		20		ns
	$\overline{CCLR}$↑ before CCK↑			6	10		10		
	CCK↑ to RCK↑††			15	20		25		
Input Capacitance		C_{IN}		5					pF
Output Capacitance (Q Outputs)		C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

†† This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT591

Characteristic		Symbol	Conditions†	54/74ACHT $T_a = 25°C$ $V_{CC} = 5V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5V \pm 10\%$		54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typical	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$ $R_L = 1k\Omega$	50	30		25		MHz
Propagation Delay, CCK↑ to $\overline{RCO}$		t_{PLH}		15		25		29	ns
		t_{PHL}		15		25		29	
Propagation Delay, $\overline{CCLR}$↓ to $\overline{RCO}$		t_{PHL}		17		28		33	ns
Propagation Delay, RCK↑ to Q		t_{PLH}		18		31		37	ns
		t_{PHL}		10		16		19	
Propagation Delay, $\overline{G}$↓ to Q		t_{PHL}		14		20		24	ns
Propagation Delay, $\overline{G}$↑ to Q		t_{PLH}		14		20		24	ns
Pulse Duration	CCK or RCK High or Low	t_w		10	15		20		ns
	$\overline{CCLR}$ Low			10	15		20		
Setup Time	$\overline{CCKEN}$↓ Low to CCK↑	t_{su}		10	15		20		ns
	$\overline{CCLR}$↑ High to CCK↑			6	10		10		
	CCK↑ to RCK↑††			15	20		25		
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

†† This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

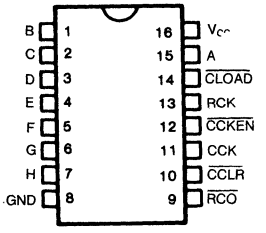
Preliminary Specifications

FEATURES

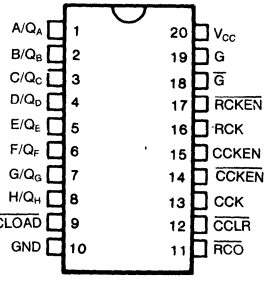
- **Parallel Register Inputs ('592)**
- **Parallel 3-State I/O: Register Inputs/Counter Outputs ('593)**
- **Counter Has Direct Overriding Load and Clear**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'592



'593



DESCRIPTION

The '592 and '593 both contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{CCKEN}$, is low. When the counter increments to the all ones condition, ripple carry out, $\overline{RCO}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{RCO}$ or the first stage to the $\overline{CCKEN}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the RCO of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, $\overline{CLOAD}$, input is taken low.

The '592 differs from the '593 in that the latter device has bidirectional I input/output pins. The 3-state outputs of the counter can be enabled and are active when enable input, $\overline{G}$, is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The '593 also has a second clock enable pin, $\overline{CCKEN}$, which is active high and it also has an active low register clock enable, $\overline{RCKEN}$.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

INPUTS					FUNCTION
RCK	$\overline{CLOAD}$	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
X	L	H	X	X	Register data is loaded into counter
X	H	L	X	X	Counter clear
↑	H	H	X	X	The data of a thru H inputs is stored into register
↓	H	H	X	X	Register state is not changed
X	H	H	L	↑	Counter advances the count
X	H	H	L	↓	No count
X	H	H	H	X	No count

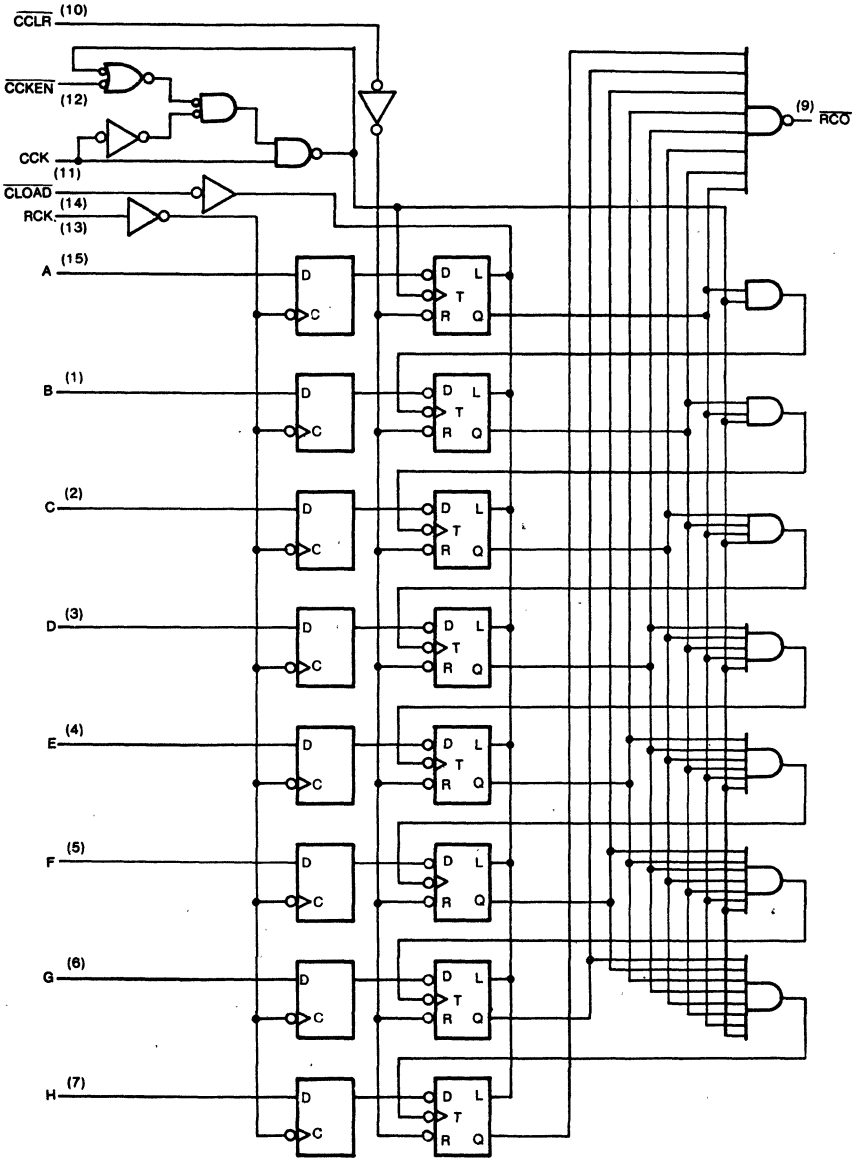
X: Don't care

$$RCO = \overline{Q_A' \bullet Q_B' Q_C' \bullet Q_D' Q_E' \bullet Q_F' Q_G' \bullet Q_H'}$$

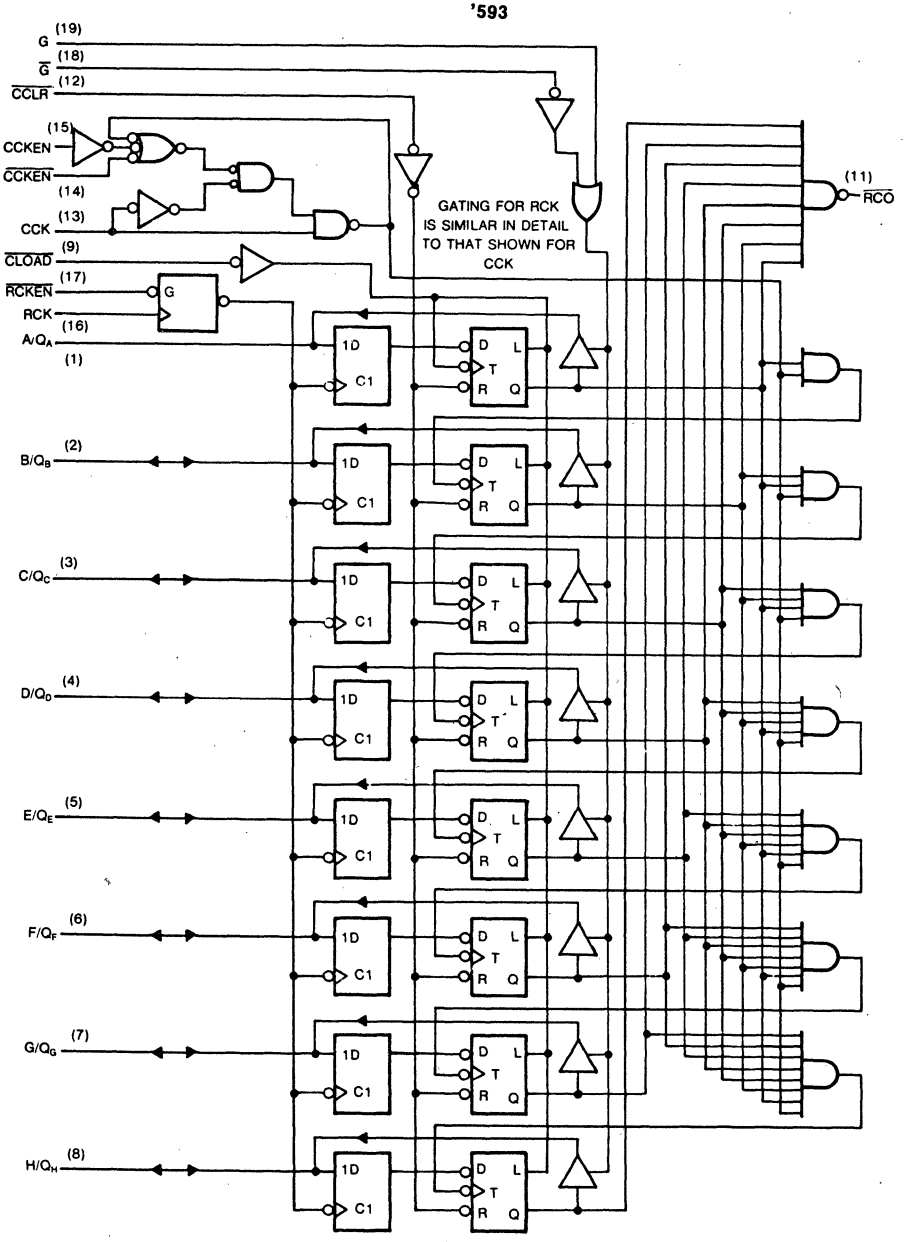
($Q_A' \sim Q_H'$: Internal outputs of the counter)

LOGIC DIAGRAMS

'592



LOGIC DIAGRAMS (Continued)



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT592

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}		50	30		25		MHz
Propagation Delay, CCK↑ to $\overline{RCO}$		t_{PLH}	$C_L = 50pF$	15		25		29	ns
		t_{PHL}		15		25		29	
Propagation Delay, $\overline{CLOAD}$↓ to $\overline{RCO}$		t_{PLH}		15		25		29	ns
		t_{PHL}		15		25		29	
Propagation Delay, $\overline{CCLR}$↓ to $\overline{RCO}$		t_{PHL}		15		25		29	ns
Propagation Delay, RCK↑ to $\overline{RCO}$		t_{PLH}	$C_L = 50pF$ $\overline{CLOAD} = GND$	18		30		36	ns
		t_{PHL}		18		30		36	
Pulse Width	CCK or RCK High or Low	t_w		10	15		20		ns
	$\overline{CCLR}$ Low			10	15		20		
	$\overline{CLOAD}$ Low			10	15		20		
Setup Time	$\overline{CCKEN}$↓ before CCK↑	t_{su}		10	15		20		ns
	$\overline{CCLR}$↑ before CCK↑			6	10		10		
	RCK↑ before CCK↑††			10	15		20		
	Data A-H↑ before RCK↑			10	15		20		
Hold Time		t_h		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.
†† The RCK↑ to CCK↑ setup time ensures that the counter will see stable data from the register output.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT593

Characteristic		Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
					Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}			50	30		25		MHz
Propagation Delay, CCK↑ to Q		t_{PLH}	$C_L = 50pF$		15		25		29	ns
			$C_L = 150pF$		18		30		35	
		t_{PHL}	$C_L = 50pF$		15		25		29	
			$C_L = 150pF$		18		30		35	
Propagation Delay, CCK↑ to $\overline{RCO}$		t_{PLH}	$C_L = 50pF$		15		25		29	ns
		t_{PHL}			15		25		29	
Propagation Delay, $\overline{CLOAD}$↓ to Q		t_{PLH}	$C_L = 50pF$		15		25		29	ns
			$C_L = 150pF$		18		30		35	
		t_{PHL}	$C_L = 50pF$		15		25		29	
			$C_L = 150pF$		18		30		35	
Propagation Delay, $\overline{CLOAD}$↓ to $\overline{RCO}$		t_{PLH}	$C_L = 50pF$		15		25		29	ns
		t_{PHL}			15		25		29	
Propagation Delay, RCK↑ to $\overline{RCO}$		t_{PLH}	$C_L = 50pF$		18		30		36	ns
		t_{PHL}	$\overline{CLOAD} = GND$		18		30			
Propagation Delay, $\overline{CCLR}$↓ to Q		t_{PHL}	$C_L = 50pF$		15		25		29	ns
			$C_L = 150pF$		18		30		35	
Propagation Delay, $\overline{CCLR}$↓ to $\overline{RCO}$		t_{PLH}	$C_L = 50pF$		15		25		29	ns
Enable Time, G↑ or $\overline{G}$↓ to Q		t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	13		20		24	ns
				$C_L = 150pF$	16		25		30	
		t_{PZL}		$C_L = 50pF$	13		20		24	
				$C_L = 150pF$	16		25		30	
Disable Time, $\overline{G}$↓ or G↑ to Q		t_{PHZ}	$R_L = 1k\Omega$		13		20		24	ns
		t_{PLZ}	$C_L = 50pF$		13		20		24	
Pulse Width	CCK or RCK High or Low	t_w			10	15		20		ns
	$\overline{CCLR}$ Low				10	15		20		
	$\overline{CLOAD}$ Low				10	15		20		
Setup Time	$\overline{CCKEN}$↓ before CCK↑	t_{su}			10	15		20		ns
	$\overline{RCKEN}$↓ to RCK↑				10	15		20		
	$\overline{CCLR}$↓ before CCK↑				6	10		10		
	RCK↑ before CCK↑††				10	15		20		
	Data A-H before RCK↑				10	15		20		
Hold Time		t_h			−3	0		0		ns
Input Capacitance		C_{IN}			5					pF
Output Capacitance		C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance*		C_{PD}								pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

†† The RCK↑ to CCK↑ setup time ensures that the counter will see stable data from the register output.

FEATURES

- **8-Bit Serial-In, Parallel-Out Shift Registers With Storage.**
- **Choice of 3-State ('595) or Open-Drain ('596) Parallel Outputs.**
- **Shift Register Has Direct Clear.**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

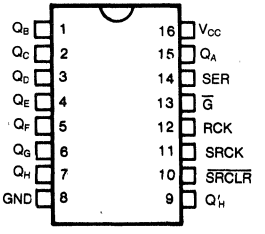
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('595) or open-drain ('596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



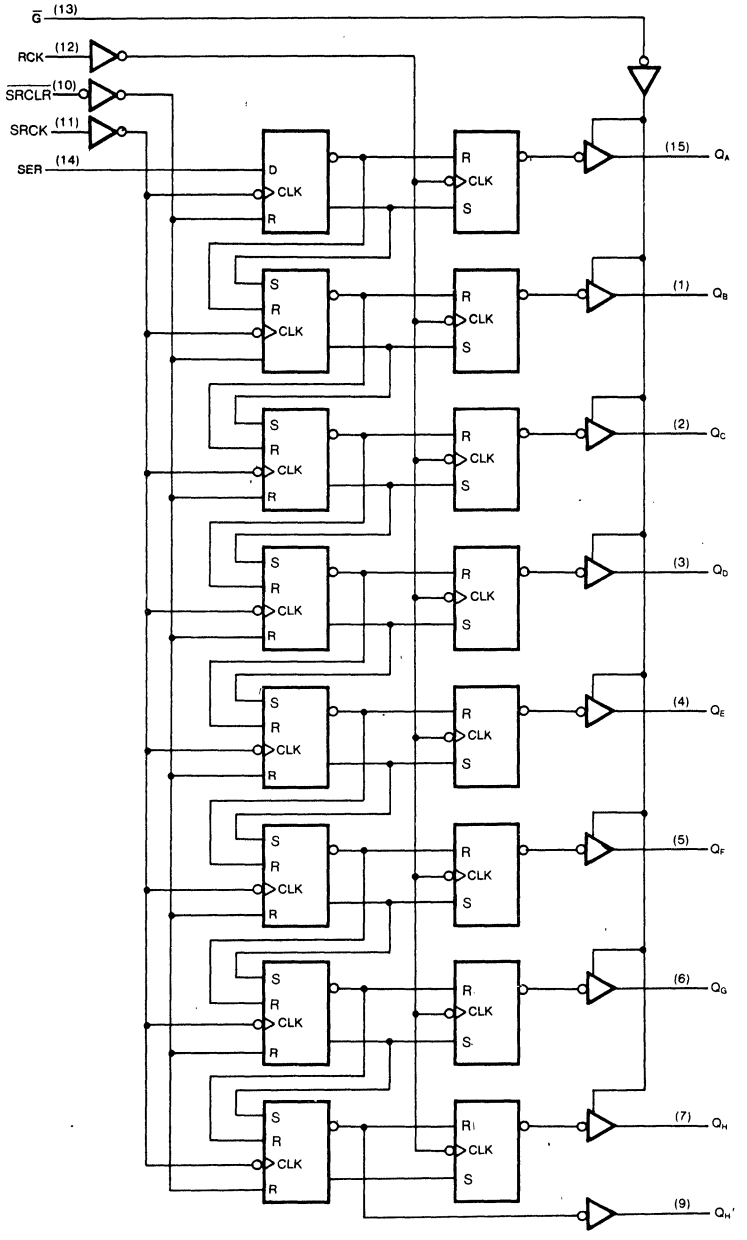
FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCK	$\overline{SRCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	Q_A thru Q_H outputs disable
X	X	X	X	L	Q_A thru Q_H outputs enable
X	X	L	X	X	Shift register is cleared.
L	⌐	H	X	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	⌐	H	X	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X	¬	H	X	X	State of S.R. is not changed.
X	X	X	⌐	X	S.R. data is stored into storage register.
X	X	X	¬	X	Storage register state is not changed.

X: DON'T CARE

LOGIC DIAGRAM

'595 or '596



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (All '595 Outputs and '596 Q_H' Output)	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	 V_{CC} 4.2	 V_{CC} −0.1 3.98	 V_{CC} −0.1 3.84	 V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	 0	 0.1 0.26 0.39	 0.1 0.33 0.5	 0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT595, AHCT596

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay, SRCK↑ to Q'_H		t_{PLH}	$C_L = 50pF$	9		25		18	ns
		t_{PHL}		9		15		18	
Propagation Delay, RCK↑ to Q_A thru Q_H		t_{PLH}	$C_L = 50pF$	11		16		19	ns
			$C_L = 150pF$	14		21		25	
		t_{PHL}	$C_L = 50pF$	11		17		20	
			$C_L = 150pF$	14		22		26	
Output Enable Time, $\overline{G}$↓ to Q_A thru Q_H ('595 only)		t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$	14		20		24	ns
			$C_L = 150pF$	17		25		30	
		t_{PZL}	$C_L = 50pF$	14		20		24	
			$C_L = 150pF$	17		25		30	
Output Disable Time, $\overline{G}$↑ to Q_A thru Q_H ('595 only)		t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	14		20		24	ns
		t_{PLZ}		14		20		24	
Propagation Delay, $\overline{G}$↑ to Q_A thru Q_H ('596 only)		t_{PLH}	$C_L = 50pF$	14		20		24	ns
			$C_L = 150pF$	17		25		30	
Propagation Delay, $\overline{G}$↓ to Q_A thru Q_H ('596 only)		t_{PHL}	$C_L = 50pF$	14		20		24	ns
			$C_L = 150pF$	17		25		30	
Pulse Width	SRCK or RCK	t_w		10	15		20		ns
	$\overline{SRCLR}$ Low			10	15		20		
Setup Time	$\overline{SRCLR}$↑ to SRCK↑	t_{su}		6	10		12		ns
	SER to SRCK↑			10	15		20		
	SRCK↑ to RCK↑↑			15	20		25		
Hold Time,		t_h		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Output Capacitance		C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

†† The RCK↑ to CCK↑ setup time ensures that the counter will see stable data from the register output.

8-Bit Shift-Registers with Input Latches

FEATURES

- **8-Bit Parallel Storage Register Inputs**
- **shift Register has Direct Overiding Load and Clear.**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

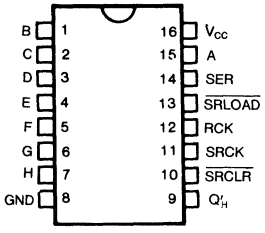
DESCRIPTION

The '597 consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

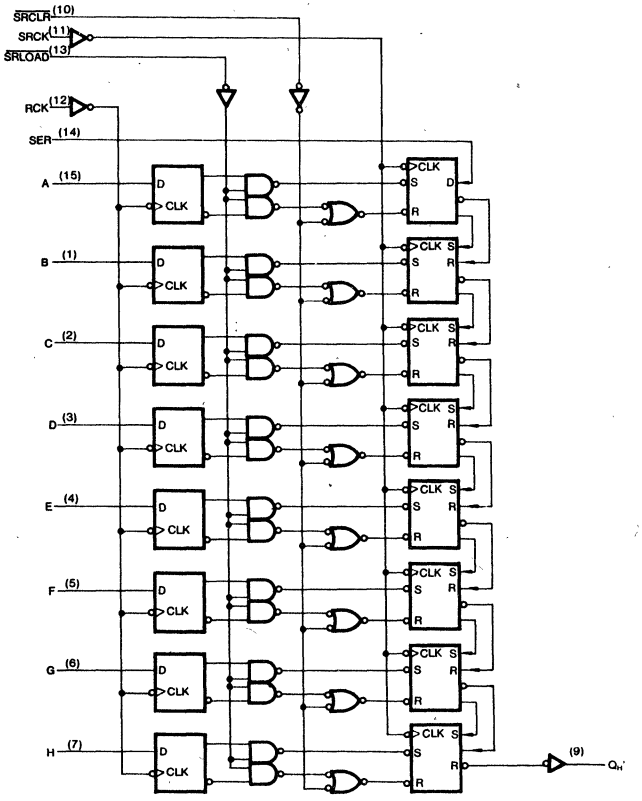
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCK	$\overline{SRCLR}$	$\overline{SRLOAD}$	RCK	
X	X	L	H	X	S.R. is cleared to "L"
X	X	H	J	X	Input register data is stored into S.R.
L	↓	H	H	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	↓	H	H	X	First stage of S.R. becomes "H". Other stages stores the data of previous stage, respectively.
X	X	X	X		State of S.R. is not changed.
X	X	X	X	↓	Input data on A~H line is stored into input register
X	X	X	X	↑	Storage register state is not changed.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4$ mA $I_O=8$ mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT597

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	50	30		25		MHz
Propagation Delay, SRCK↑ to Q'_H		t_{PLH}		9		15		18	ns
		t_{PHL}		9		15		18	
Propagation Delay, $\overline{SRLOAD}$↓ to Q'_H		t_{PLH}		14		20		24	ns
		t_{PHL}		14		20		24	
Propagation Delay, $\overline{SRCLR}$↓ to Q'_H		t_{PHL}		11		18		21	ns
Propagation Delay, RCK↑ to Q'_H		t_{PLH}	$C_L = 50pF$ $\overline{SLOAD}$=Low	15		25		29	ns
		t_{PHL}		15		25		29	
Pulse Width	RCK or SRCK High or Low	t_w		10	15			20	ns
	$\overline{SRCLR}$ or $\overline{SRLOAD}$ Low			10	15		20		
Setup Time	$\overline{SRCLR}$↑ before SRCK↑	t_{su}		6	10		12		ns
	RCK↑ before SRCK↑††			15	20		25		
	SER before SRCK↑			10	15		20		
	A thru H before RCK↑			10	15		20		
Hold Time		t_h		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.
†† The RCK↑ to CCK↑ setup time ensures that the counter will see stable data from the register output.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

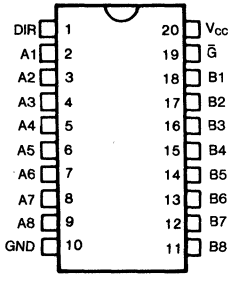
DESCRIPTION

These high-speed octal/bus transceivers are designed for asynchronous two-way communication between data buses. A direction control input (DIR) controls the flow direction of data. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The '643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus. The '640 transfers inverted data in both directions.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

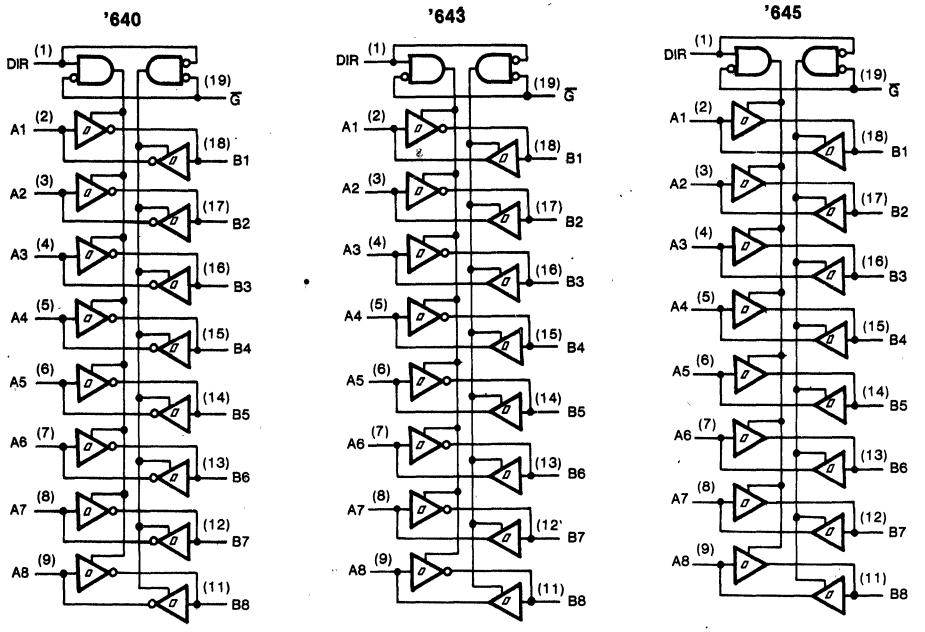
PIN CONFIGURATION



FUNCTION TABLE

Control Inputs		Operation		
$\bar{G}$	DIR	'640	'643	'645
L	L	Inverted data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A
L	H	Inverted data transmitted from Bus A to Bus B	Inverted data transmitted from Bus A to Bus B	Data transmitted from Bus A to Bus B
H	X	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)

LOGIC DIAGRAMS



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT640, AHCT643

Characteristic	Symbol	Conditions†		T_a = 25°C V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C V_{CC} = 5.0V ± 10%		KS54AHCT T_a = −55°C to +125°C V_{CC} = 5.0V ± 10%		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay, A to B, or B to A	t_{PLH}	C_L=50pF C_L=150pF		7 10		12 17		14 20	ns
	t_{PHL}	C_L=50pF C_L=150pF		7 10		12 17		14 20	
Output Enable Time, $\overline{G}$ to A or B	t_{PZH}	R_L=1kΩ	C_L=50pF C_L=150pF	12 15		20 25		25 31	ns
	t_{PZL}		C_L=50pF C_L=150pF	12 15		20 25		25 31	
Output Disable Time, $\overline{G}$ to A or B	t_{PHZ}	R_L=1kΩ C_L=50pF		13		18		22	ns
	t_{PLZ}			13		18		22	
Input Capacitance	C_{IN}			5					pF
Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance*	C_{PD}*	$\overline{G}$=V_{CC} $\overline{G}$=GND	(per stage)	5 30					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT645

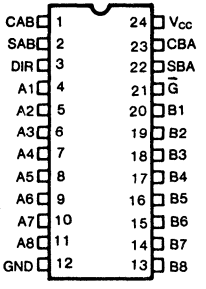
Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A to B, or B to A	t_{PLH}	$C_L = 50pF$	6		10		14	ns
		$C_L = 150pF$	9		19		25	
	t_{PHL}	$C_L = 50pF$	6		10		14	
		$C_L = 150pF$	9		19		25	
Output Enable Time $\overline{G}$ to A or B	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$	12		20		25	ns
		$C_L = 150pF$	18		29		36	
	t_{PZL}	$C_L = 50pF$	12		20		25	
		$C_L = 150pF$	18		29		36	
Output Disable Time, $\overline{G}$ to A or B	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	13		18		22	ns
	t_{PLZ}		13		18		22	
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*	C_{PD}*	$\overline{G} = V_{CC}$ (per stage)	5					pF
		$\overline{G} = GND$	30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **8 bi-directional data paths**
- **Transmits direct or stored data in either direction**
- **24-pin slim DIP package**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to + 85°C
  KS54HACT: −55°C to + 125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

The '646 and '648 are bi-directional bus transceivers with D-type flip-flops and control circuitry to facilitate high speed multiplexed data transmission. The '646 transmits true data and the '648 transmits inverted data.

Data can be transmitted directly from one port to the other in either direction. It also can be stored in the flip-flops from either or both ports for subsequent transmission to the opposite port. Six control inputs govern the data flow:

$\overline{G}$ (output enable) when high, all outputs are disabled, isolating the A and B ports. When low, one port is enabled at a time as determined by the DIR pin.

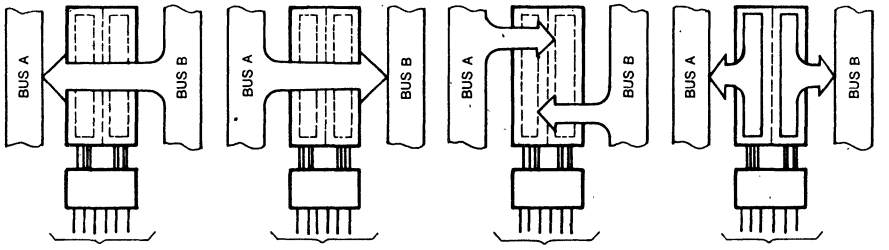
DIR (direction control) disables A or B outputs permitting the pins to be used as inputs thus determining the direction of a data flow. When DIR=high, data flows from A to B.

SAB,SBA (data source AB and BA) determines whether data transmitted is from the data inputs or the registers associated with those inputs.

CAB,CBA (Clock AB and BA) clocks data from the A inputs and the B inputs, respectively, into their associated registers. Since the clocks are not gated with the $\overline{G}$ and DIR pins, data at the A and B pins can be clocked into the flip-flops at any time.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

Real-Time transfer bus B to bus A

(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	X	X	L	X

Real-Time transfer bus A to bus B

(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Storage from A AND/OR B

(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	H
L	H	X	X	H	X

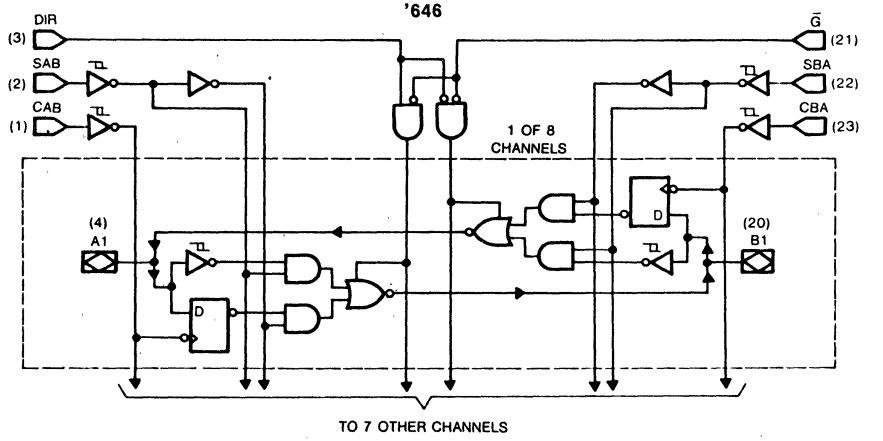
Transfer stored data to A AND/OR B

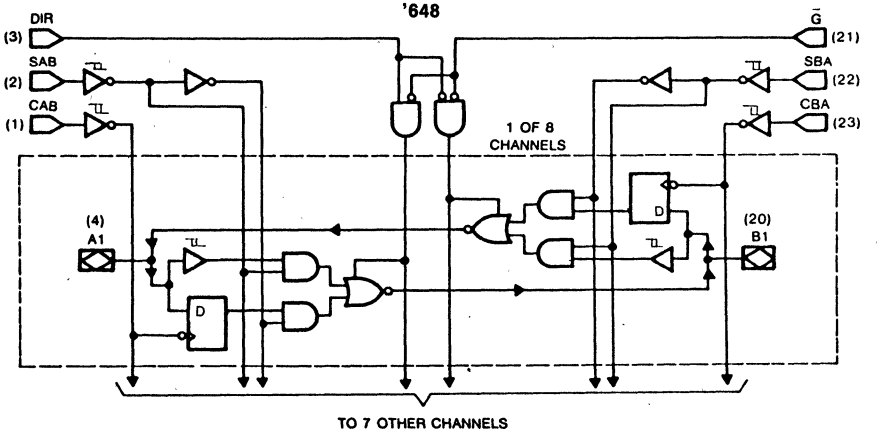
FUNCTION TABLE

Inputs						Data I/O*		Operation or Function	
$\bar{G}$	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	'646	'648
X	X	↑	X	X	X	input	input'	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Not specified	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage	isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B data to A bus	Real-Time $\bar{B}$ data to A bus
L	L	X	H or L	X	H			Stored B data to A bus	Stored $\bar{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-Time A data to B bus	Real-Time $\bar{A}$ data to B bus
L	H	H or L	X	H	X			Stored A data to B bus	Stored $\bar{A}$ data to B bus

*The data output functions may be enabled or disabled by various signals at the $\bar{G}$ and DIR inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT646, AHCT648

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Frequency	f_{max}	C_L=50pF	45		30		25	MHz
Propagation Delay, A or B Input to B or A Output	t_{PLH}	C_L=50pF C_L=150pF	11 14		18 23		22 28	ns
	t_{PHL}	C_L=50pF C_L=150pF	11 14		18 23		22 28	
Propagation Delay, CBA or CAB Input to A or B Output	t_{PLH}	C_L=50pF C_L=150pF	15 18		25 30		30 36	ns
	t_{PHL}	C_L=50pF C_L=150pF	15 18		25 30		30 36	
Propagation Delay,†† SBA or SAB Input to A or B Output (with A or High)	t_{PLH}	C_L=50pF C_L=150pF	16 19		27 33		32 38	ns
	t_{PHL}	C_L=50pF C_L=150pF	16 19		27 33		32 38	
Propagation Delay,†† SBA or SAB Input to A or B Output (with A or Low)	t_{PLH}	C_L=50pF C_L=150pF	15 18		25 30		30 36	ns
	t_{PHL}	C_L=50pF C_L=150pF	15 18		25 30		30 36	
Out Enable Time, $\overline{G}$ or DIR Input to A or B Output	t_{PZH}	R_L=1kΩ, C_L=50pF R_L=1kΩ, C_L=150pF	14 17		22 27		26 32	ns
	t_{PZL}	R_L=1kΩ, C_L=50pF R_L=1kΩ, C_L=150pF	14 17		22 27		26 32	
Output Disable Time, $\overline{G}$ or DIR Input to A or B Output	t_{PHZ}	R_L=1kΩ, C_L=50pF	13		22		26	ns
	t_{PLZ}		13		22		26	
Pulse Duration, Clocks High or low	t_w		8	12		15		ns
Set up Time, A before CAB↑ or B before CBA↑	t_{su}		8	12		15		ns
Hold Time, A after CAB↑ or B after CBA↑	t_h		−3	0		0		ns
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

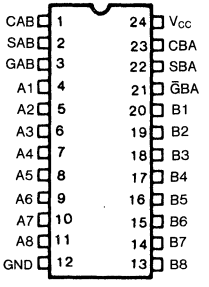
†† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Preliminary Specifications

FEATURES

- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored-Data**
- **Choice of True and Inverting Data Paths**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



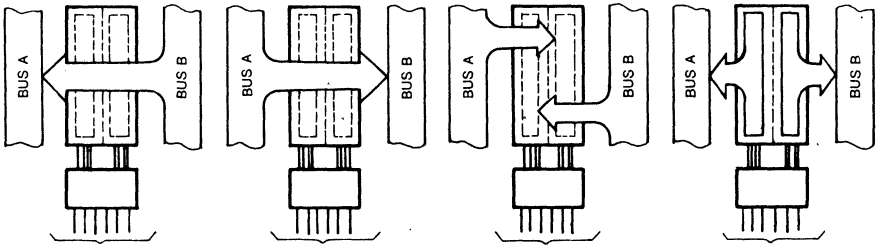
DESCRIPTION

These devices consist of bus transceiver circuits. D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{G}$BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.



(3) GAB	(21) $\overline{G}$BA	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

Real-Time transfer bus B to bus A

(3) GAB	(21) $\overline{G}$BA	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	X	X	L	X

Real-Time transfer bus A to bus B

(3) GAB	(21) $\overline{G}$BA	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Storage from A AND/OR B

(3) AB	(21) $\overline{G}$BA	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	H
L	H	X	X	H	X

Transfer stored data TO A AND/OR B

FUNCTION TABLE

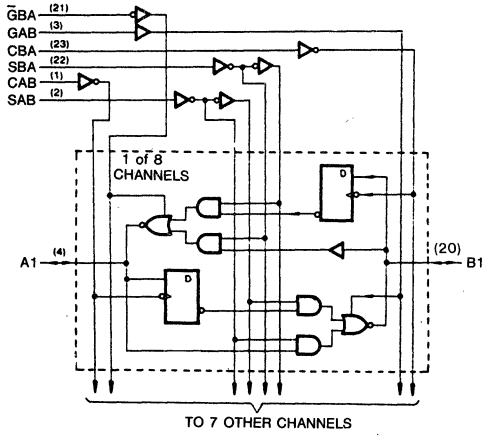
INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'651	'652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B	Store A Hold B
H	H	↑	↑	X**	X	Input	Output*	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X**	Output*	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to a Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

* The data output functions may be enabled or disabled by various signals at the GAB and $\overline{GBA}$ inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

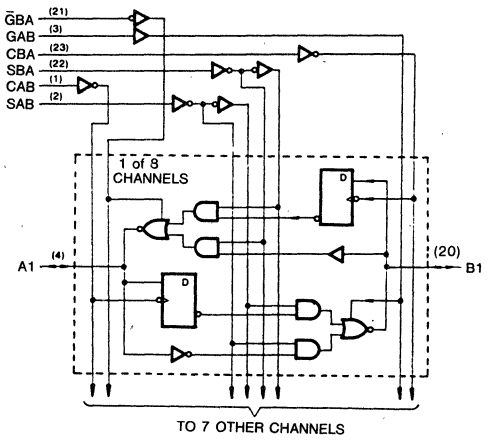
** Select control=L: clocks can occur simultaneously
Select control=H: clocks must be staggered in order to load both registers

LOGIC DIAGRAMS

'651



'652



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT651, AHCT652

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Clock Frequency	f_{max}	C_L=50pF	45	30		25		MHz
Propagation Delay, A or B Input to B or A Ouput	t_{PLH}	C_L=50pF C_L=150pF	11 14		18 23		22 28	ns
	t_{PHL}	C_L=50pF C_L=150pF	11 14		18 23		22 28	
Propagation Delay, CBA or CAB Input to A or B Output	t_{PLH}	C_L=50pF C_L=150pF	15 18		25 30		30 36	ns
	t_{PHL}	C_L=50pF C_L=150pF	15 18		25 30		30 36	
Propagation Delay, SBA or SAB Input to A or B Output (with A or B High)	t_{PLH}	C_L=50pF C_L=150pF	16 19		27 32		32 38	ns
	t_{PHL}	C_L=50pF C_L=150pF	16 19		27 32		32 38	
Propagation Delay, SBA or SAB Input to A or B Output (with A or B Low)	t_{PLH}	C_L=50pF C_L=150pF	15 18		25 30		30 36	ns
	t_{PHL}	C_L=50pF C_L=150pF	15 18		25 30		30 36	
Output Enable Time, $\overline{G}$BA to A or GAB to B	t_{PZL}	R_L=1kΩ, C_L=50pF R_L=1kΩ, C_L=150pF	19 22		32 37		38 44	ns
	t_{PZH}	R_L=1kΩ, C_L=50pF R_L=1kΩ, C_L=150pF	19 22		32 37		38 44	
Output Disable Time, $\overline{G}$BA to A or GAB to B	t_{PHZ}	R_L=1kΩ, C_L=50pF	13		22		26	ns
	t_{PLZ}		13		22		26	
Pulse Width Clocks High or Low	t_w		8	12		15		ns
Setup Time, A before CAB↑ or B before CBA↑	t_{su}		8	12		15		ns
Hold Time, A after CAB↑ or B after CBA↑	t_h		−3	0		0		ns
Maximum Input Capacitance	C_{IN}		5					pF
maximum Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*	C_{PD}							pF

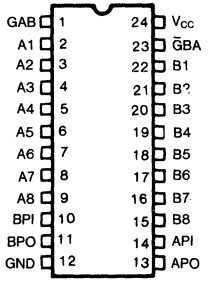
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

FEATURES

- **Bus Transceivers with Inverting Outputs ('658) or True Outputs ('659)**
- **Generates a Parity Bit for A Bus and B Bus**
- **Easily Cascadable**
- **Internal Active Pull-Ups and Pull-Downs**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus, or from the B Bus to the A Bus, depending on the levels at the direction control inputs, GAB and $\overline{GBA}$. These devices also generate parity outputs. APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuits on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuits.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

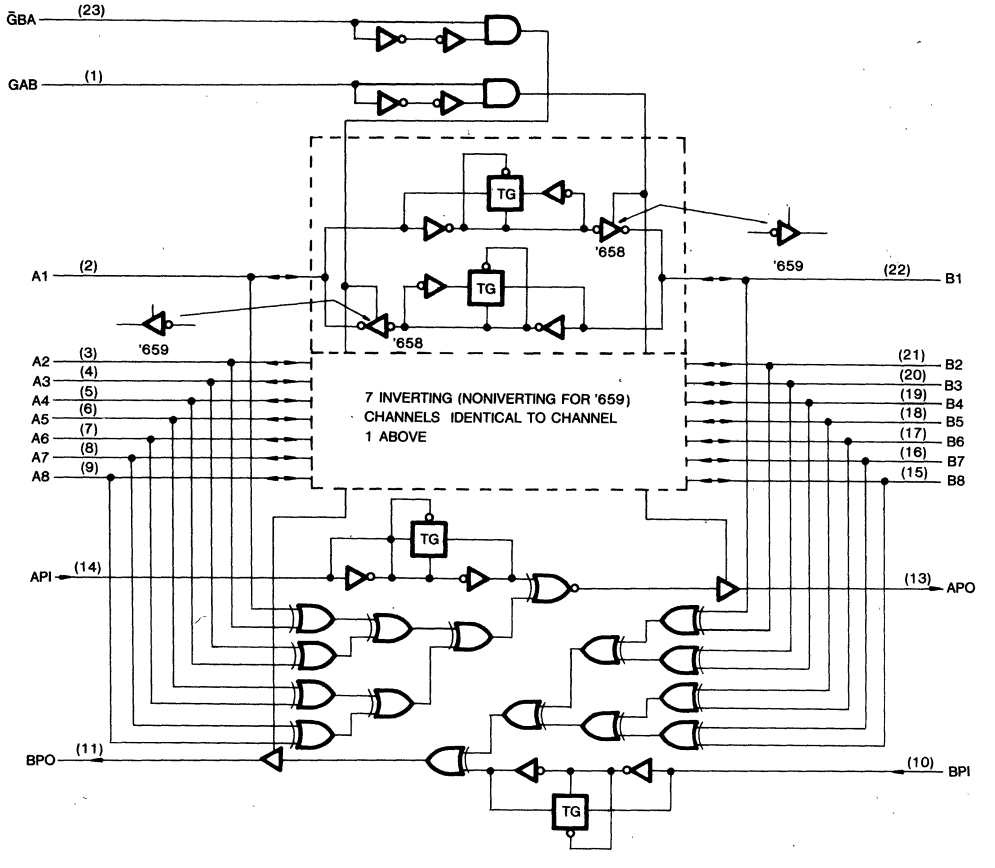
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

4

FUNCTION TABLE

CONTROL INPUTS		NUMBER OF HIGH INPUTS ON A BUS AND API	NUMBER OF HIGH INPUTS ON B BUS AND BPI	OUTPUTS		OPERATION	
$\overline{GBA}$	GAB			APO	BPO	'658	'659
L	L	X	0, 2, 4, 6, 8	Z	H	$\overline{B}$ Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
H	H	0, 2, 4, 6, 8	X	H	Z	$\overline{A}$ Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	L	X	X	Z	Z	Isolation	Isolation
L	H	X	0, 2, 4, 6, 8		H	$\overline{B}$ Data to A Bus, $\overline{A}$ Data to B Bus	B Data to A Bus, A Data to B Bus
		X	1, 3, 5, 7, 9		L		
		0, 2, 4, 6, 8	X	H			
		1, 3, 5, 7, 9	X	L			

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a =25°C	KS74AHCT T_a= −40°C to +85°C	KS54AHCT T_a= −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O= −6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT658, AHCT659

Characteristic	Symbol	Conditions†	T_a =25°C V_{CC}=5.0V	KS74AHCT T_a = −40°C to +85°C V_{CC}=5.0V±10%		KS54AHCT T_a = −55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to B or A	t_{PLH}	C_L=50pF C_L=150pF	11 14		18 23		22 28	ns
	t_{PHL}	C_L=50pF C_L=150pF	11 14		18 23		22 28	
Propagation Delay, A or B to APO or BPO	t_{PLH}	C_L=50pF C_L=150pF	16 19		27 32		32 38	ns
	t_{PHL}	C_L=50pF C_L=150pF	16 19		27 32		32 38	
Propagation Delay, API or BPI to APO or BPO	t_{PLH}	C_L=50pF C_L=150pF	11 14		18 23		22 28	ns
	t_{PHL}	C_L=50pF C_L=150pF	11 14		18 23		22 28	
Enable Time, GAB or $\overline{GBA}$ to APO or BPO	t_{PZH}	R_L=1kΩ, C_L=50pF R_L=1kΩ, C_L=150pF	16 19		27 32		32 38	ns
	t_{PZL}	R_L=1kΩ, C_L=50pF R_L=1kΩ, C_L=150pF	16 19		27 32		32 38	
Disable Time, GAB or $\overline{GBA}$ to APO or BPO	t_{PLZ}	R_L=1kΩ C_L=50pF	16		27		32	ns
	t_{PHZ}		16		27		32	
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}							pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.

† For AC switching test circuits and timing waveforms see section 2.

KS54AHCT 664/665
KS74AHCT

Octal Bus Transceivers with Parity

Preliminary Specifications

FEATURES

- **Bus Transceivers with Inverting Outputs ('664) or True Outputs ('665)**
- **Generates a Parity Bit for A Bus and B Bus**
- **Easily Cascadable**
- **Internal Active Pull-Ups and Pull-Downs**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

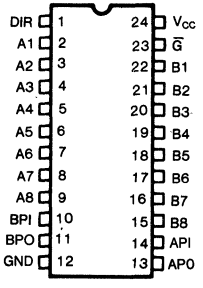
These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input, $\overline{G}$, can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is tht when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

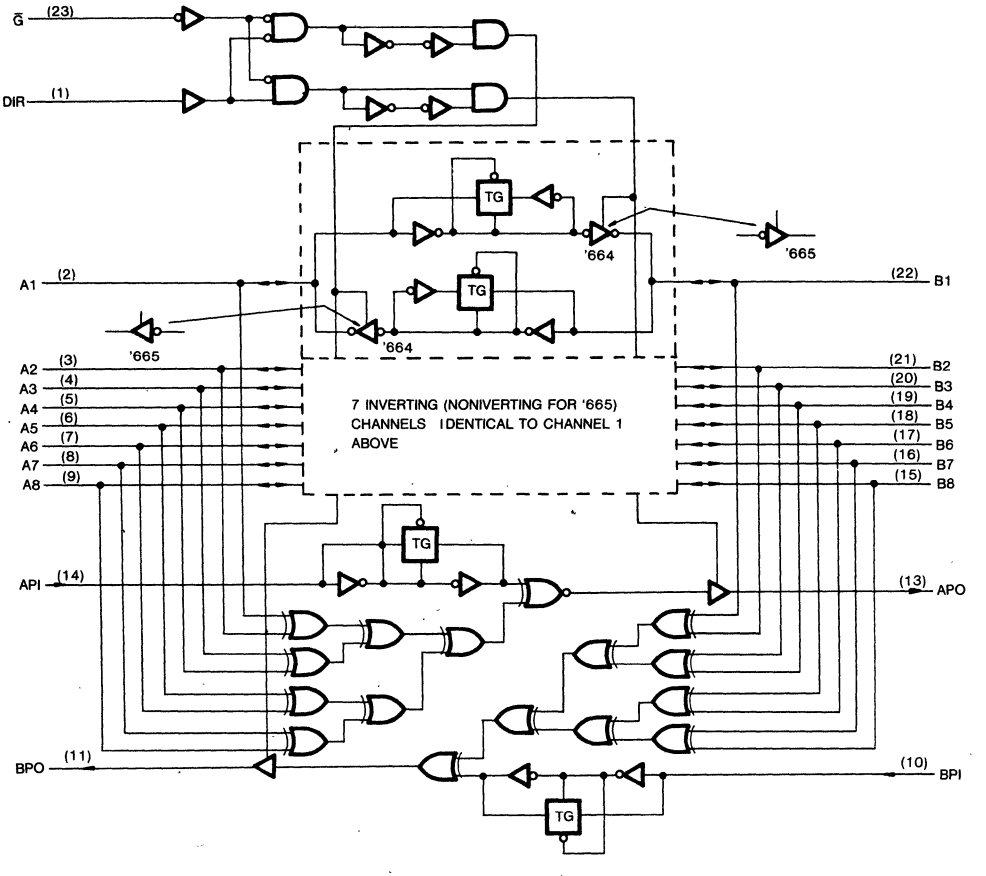
PIN CONFIGURATION



FUNCTION TABLE

CONTROL INPUTS		NUMBER OF HIGH INPUTS ON A BUS AND API	NUMBER OF HIGH INPUTS ON B BUS AND BPI	OUTPUTS		OPERATION	
$\overline{G}$	DIR			APO	BPO	'664	'665
L	L	X	0, 2, 4, 6, 8	Z	H	$\overline{B}$ Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
L	H	0, 2, 4, 6, 8	X	H	Z	$\overline{A}$ Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	X	X	X	Z	Z	Isolation	Isolation

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O= −6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT664, AHCT665

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Propagation Delay, A or B to B or A	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$		11 14		18 23		22 28	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$		11 14		18 23		22 28	ns
Propagation Delay, A or B to APO or BPO	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$		16 19		27 32		32 38	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$		16 19		27 32		32 38	ns
Propagation Delay, API or BPI to APO or BPO	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$		11 14		18 23		22 28	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$		11 14		18 23		22 28	ns
Output Enable Time, $\bar{G}$ to A or B	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$ $C_L = 150pF$	16 19		27 32		32 38	ns
	t_{PZL}	$R_L = 1k\Omega$	$C_L = 50pF$ $C_L = 150pF$	16 19		27 32		32 38	ns
Output Disable Time, $\bar{G}$ to A or B	t_{PHZ}	$R_L = 1k\Omega$ $C_L = 50pF$		16		27		32	ns
	t_{PLZ}			16		27		32	ns
Output Enable Time, DIR to A or B	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$ $C_L = 150pF$	16 19		27 32		32 38	ns
	t_{PZL}	$R_L = 1k\Omega$	$C_L = 50pF$ $C_L = 150pF$	16 19		27 32		32 38	ns
Output Disable Time, DIR to A or B	t_{PHZ}	$R_L = 1k\Omega$ $C_L = 50pF$		16		27		32	ns
	t_{PLZ}			16		27		32	ns
Input Capacitance	C_{IN}			5					pF
Output Capacitance	C_{OUT}	Output Disabled							pF
Power Dissipation Capacitance*	C_{PD}								pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

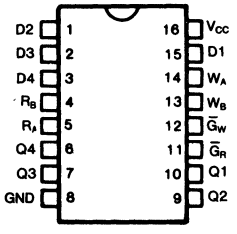
† For AC switching test circuits and timing waveforms see section 2.

4

FEATURES

- **Seperate Read Write Addressing Permits Simultaneous Reading and Writing**
- **Expandable to 512 Words of 7-bits**
- **For use as:**
  - **— Scratch pad memory**
  - **— Buffer Storage between processors**
  - **— Bit storage in fast multiplication designs**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

The '670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and enable inputs are available, permititng simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the Write Enable ($\overline{G}_W$) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{G}_W$ is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when $\overline{G}_W$ is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A and R_B). The addressed word appears at the four outputs when the Read Enable ($\overline{G}_R$) is LOW. Data outputs are in the HIGH impedance "off" state when the read enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull-up resistors to the outputs to increase the I_{OH} current available. Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES[a]
	$\overline{G}_W$	D_n	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

NOTE:

a. The Write Address (W_A and $\overline{W}_B$) to the "Internal latches" must be stable while $\overline{G}_W$ is LOW for conventional operation.

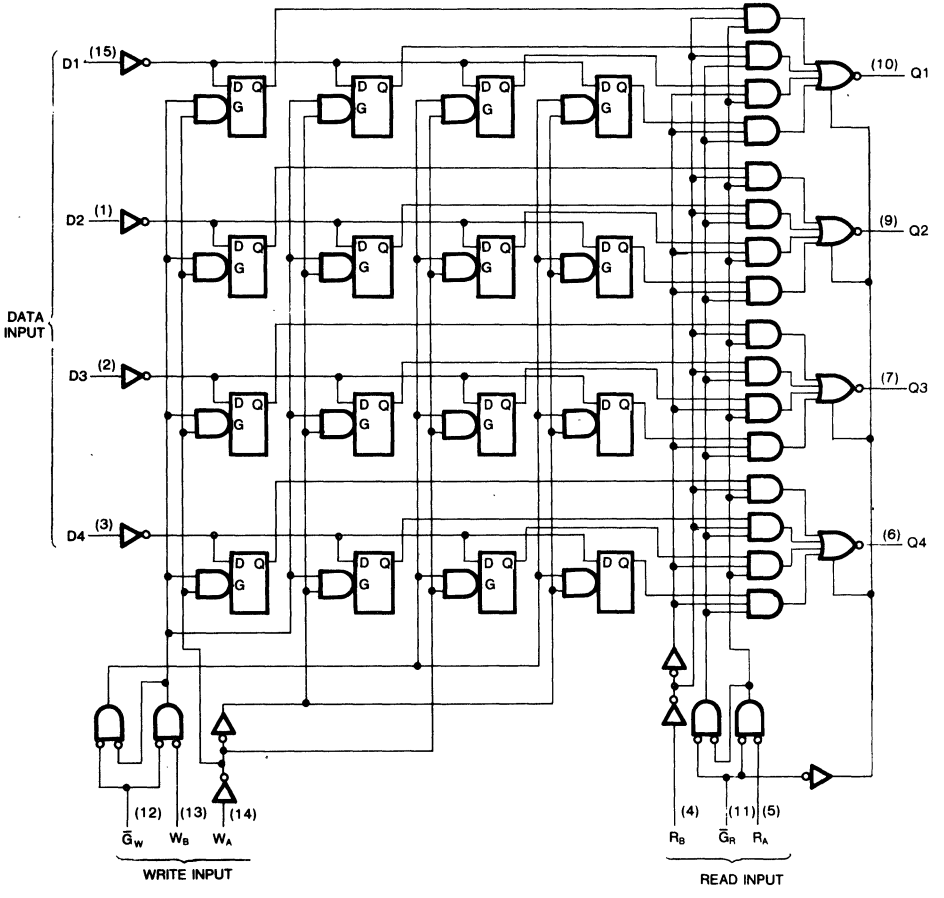
READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT Q_n
	$\overline{G}_R$	INTERNAL LATCHES[b]	
Read	L	L	L
	L	H	H
Disabled	H	H	(Z)

NOTE:

b. The selection of the "internal latches" by Read Address ($\overline{R}_A$ and R_B) are not constrained by $\overline{G}_W$ or $\overline{G}_R$ operation.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT670

Characteristic	Symbol	Conditions†		T_a = 25°C V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C V_{CC} = 5.0V ± 10%		KS54AHCT T_a = −55°C to +125°C V_{CC} = 5.0V ± 10%		Unit
				Typ	Min	Max	Min	Max	
Maximum Propagation Delay, R_A or R_B to Output	t_{PLH}	C_L=50pF C_L=150pF		14 17		23 28		28 34	ns
	t_{PHL}	C_L=50pF C_L=150pF		14 17		23 28		28 34	
Propagation Delay, $\overline{G}_W$ to Output	t_{PLH}	C_L=50pF C_L=150pF		15 18		25 30		30 36	ns
	t_{PHL}	C_L=50pF C_L=150pF		15 18		25 30		30 36	
Propagation Delay, Data to Output	t_{PLH}	C_L=50pF C_L=150pF		14 17		23 28		28 34	ns
	t_{PHL}	C_L=50pF C_L=150pF		14 17		23 28		28 34	
Output Enable Time $\overline{G}_R$ to Output	t_{PZH}	R_L=1kΩ	C_L=50pF C_L=150pF	13 16		21 26		25 31	ns
	t_{PZL}		C_L=50pF C_L=150pF	13 16		21 26		25 31	
Output Disable Time $\overline{G}_R$ to Output	t_{PHZ}	R_L=1kΩ C_L=150pF		17		28		34	ns
	t_{PLZ}			17		28		39	
Input Capacitance	C_{IN}			5					pF
Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance*	C_{PD}								pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

FEATURES

- **'679: 12-bit to 4-bit comparator with enable**
- **'680: 12-bit to 4-bit comparator with latch**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74AHCT: −40°C to +85°C KS54AHCT: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '679 and '680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The '679 features an enable inpu ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs. The '680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

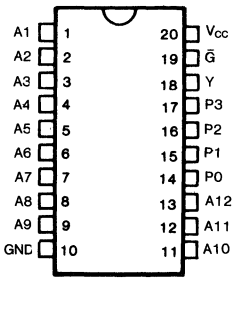
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

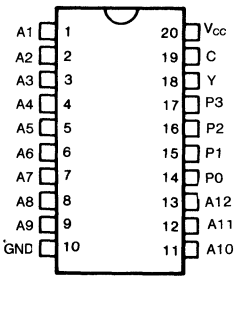
4

PIN CONFIGURATIONS

'679

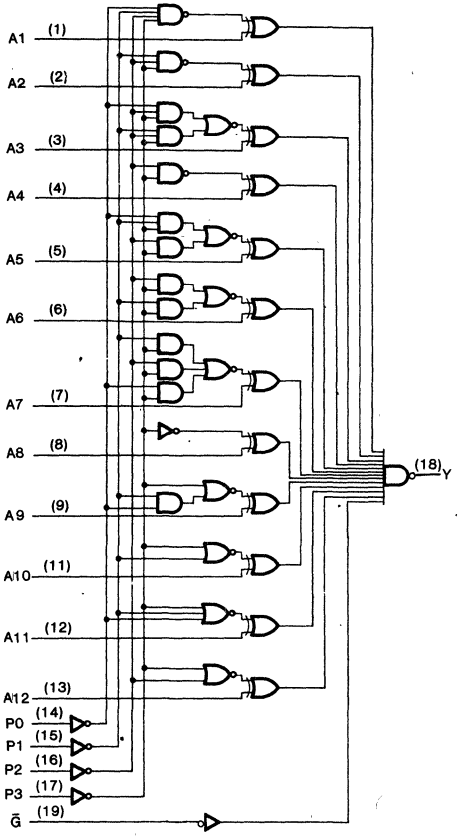


'680

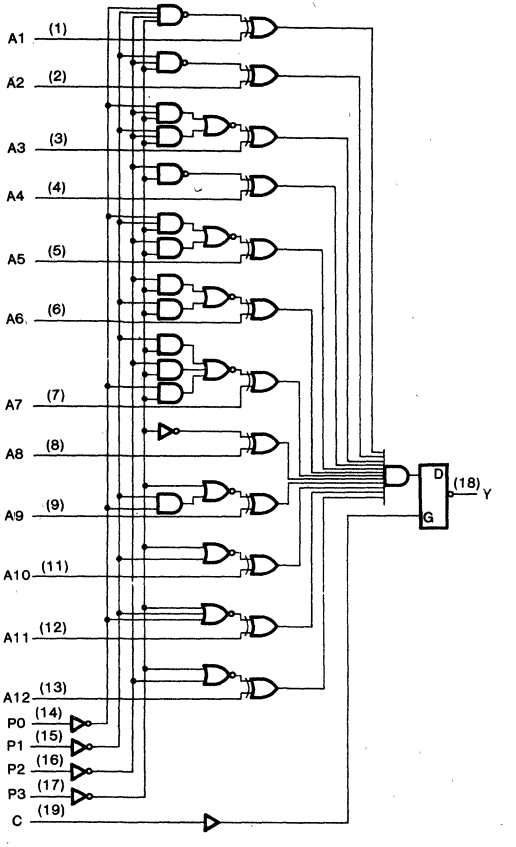


LOGIC DIAGRAMS

'679



'680



FUNCTION TABLE

'679	'680	INPUTS COMMON TO '679 AND '680																OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L*
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	H	H	L	L*
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L*
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	All other combinations																H
H		'679: Any combination																H
	L	'680: Any combination																Latched

* These three rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for all combinations in which P=12, 13 and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P≥9 to P=9 ... 11/13... 15, P≥10 to P=10/11/14/15, and P≥11 to P=11/15.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT679

Characteristic	Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C V_{CC} = 5.0V ± 10%		KS54AHCT T_a = −55°C to +125°C V_{CC} = 5.0V ± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Any P to Y	t_{PLH}	C_L=50pF C_L=150pF	18 21		30 35		36 42	ns
	t_{PHL}	C_L=50pF C_L=150pF	18 27		30 35		36 42	
Propagation Delay, Any A to Y	t_{PLH}	C_L=50pF C_L=150pF	16 19		26 31		31 37	ns
	t_{PHL}	C_L=50pF C_L=150pF	16 19		26 31		31 37	
Propagation Delay, $\overline{G}$ to Y	t_{PLH}	C_L=50pF C_L=150pF	12 15		19 24		23 29	ns
	t_{PHL}	C_L=50pF C_L=150pF	12 15		19 24		23 29	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT680

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Any P to Y	t_{PLH}	$C_L = 50pF$	21		35		42	ns
		$C_L = 150pF$	24		40		48	
	t_{PHL}	$C_L = 50pF$	21		35		42	
		$C_L = 150pF$	24		40		48	
Propagation Delay, Any A to Y	t_{PLH}	$C_L = 50pF$	18		30		36	ns
		$C_L = 150pF$	21		35		42	
	t_{PHL}	$C_L = 50pF$	18		30		36	
		$C_L = 150pF$	21		35		42	
Propagation Delay, C to Y	t_{PLH}	$C_L = 50pF$	13		21		25	ns
		$C_L = 150pF$	16		26		31	
	t_{PHL}	$C_L = 50pF$	13		21		25	
		$C_L = 150pF$	16		26		31	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

FEATURES

- **Compares Two 8-Bit Words**
- **'682 has 20kΩ pullup Resistors on the Q Inputs**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

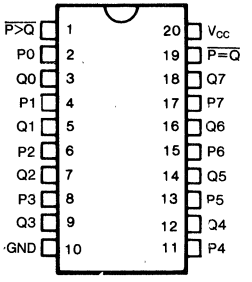
These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overline{P=Q}$ and $\overline{P>Q}$ outputs. The '682 features 20-kΩ pullup termination resistors on the Q inputs for analog or switch data.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

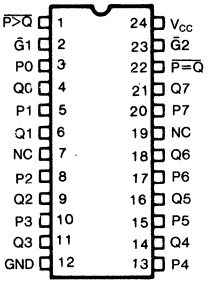
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS

'682 and '684



'686



NC—No internal connection

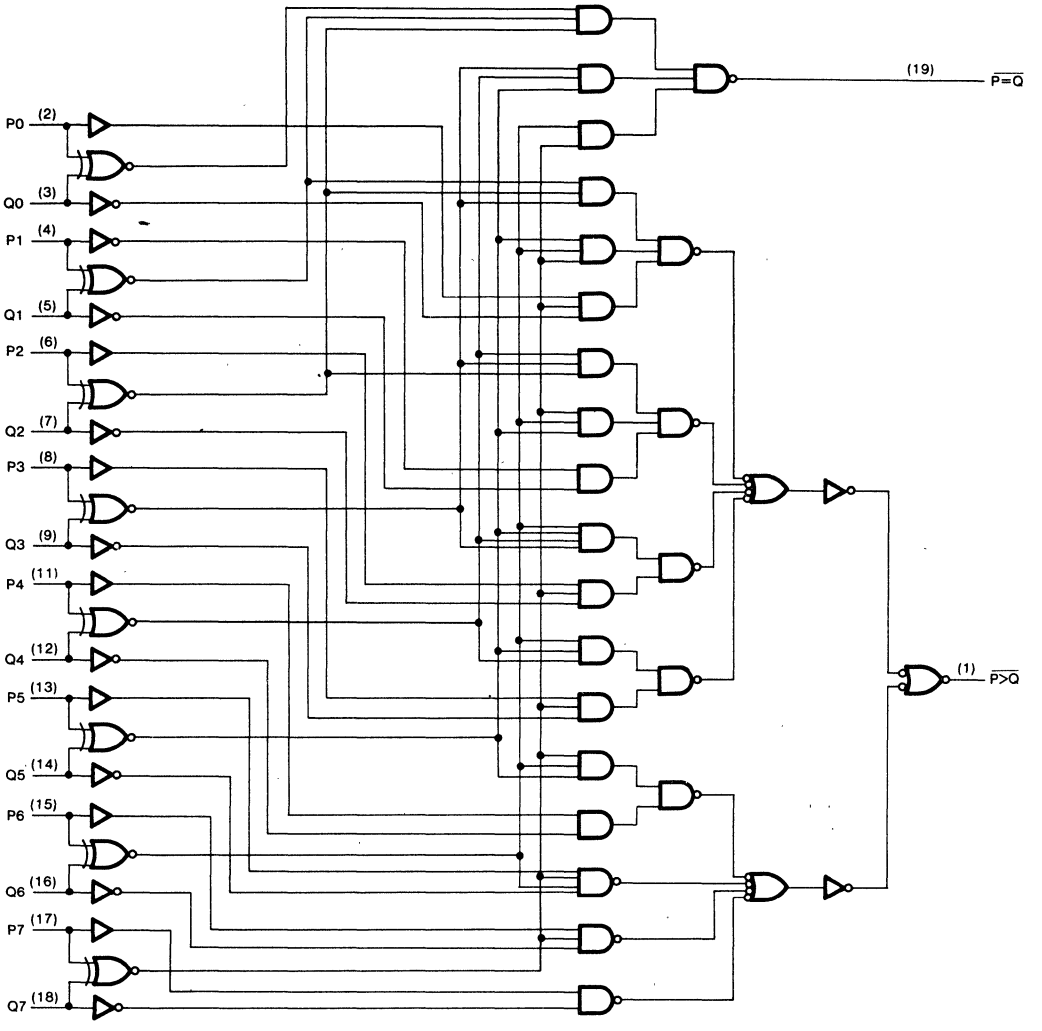
FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES			
P, Q	$\overline{G}1$	$\overline{G}2$	$\overline{P=Q}$	$\overline{P>Q}$
P=Q	L	X	L	H
P>Q	X	L	H	L
P<Q	X	X	H	H
P=Q	H	X	H	H
P>Q	X	H	H	H
X	H	H	H	H

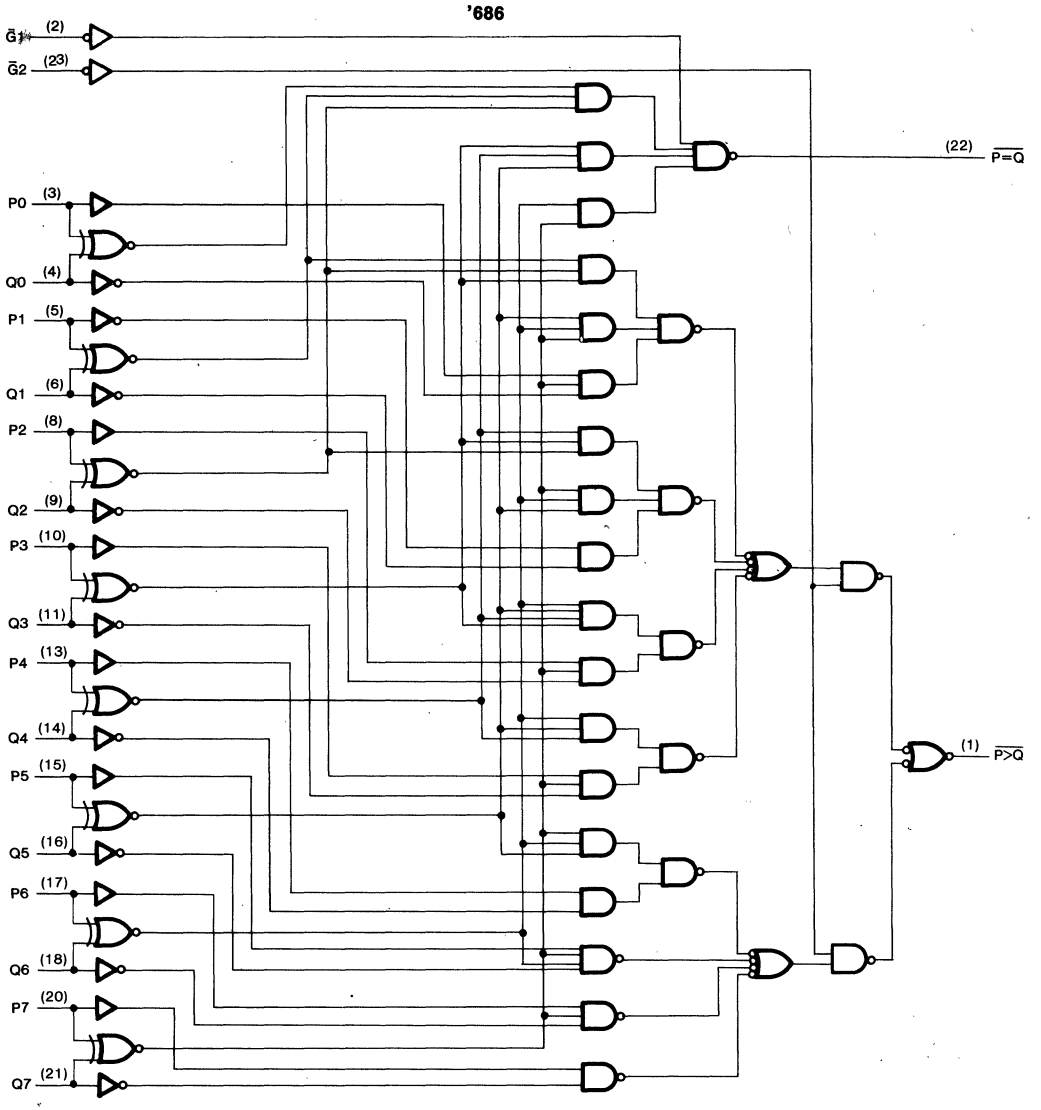
NOTES: 1. The last 3 lines of the function table apply only to the device having enable inputs, i.e., '686.
2. The $\overline{P<Q}$ function can be generated by applying the $\overline{P=Q}$ and $\overline{P>Q}$ outputs to a 2-input NAND gate.

LOGIC DIAGRAMS

'682 or '684



LOGIC DIAGRAMS (continued)



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Parameter	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (Totem-pole Outputs)	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.93	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage (All Outputs)	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current, ('682 Q Inputs)		V_{CC}=Max V_{IN}=2.7V V_{IN}=0.4V		−0.2 −0.4	−0.2 −0.4	−0.2 −0.4	mA
Maximum Input Current (All other Inputs)	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	For '682: V_{IN}=GND (Q0-Q7) $V_{IN}=V_{CC}$ or GND (all other inputs)		3.5	3.5	3.5	mA
		For '684 and '688 $V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT682, AHCT684, AHCT686

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Propagation Delay, P or Q to $\overline{P=Q}$	t_{PLH}	$C_L=50pF$	13		22		27	ns
		$C_L=150pF$	16		27		33	
	t_{PHL}	$C_L=50pF$	13		22		27	
		$C_L=150pF$	16		27		33	
Propagation Delay, P or Q to $\overline{P>Q}$	t_{PLH}	$C_L=50pF$	16		27		32	ns
		$C_L=150pF$	19		32		38	
	t_{PHL}	$C_L=50pF$	16		27		32	
		$C_L=150pF$	19		32		38	
Propagation Delay, $\overline{G1}$ to $\overline{P=Q}$ ('686 Only)	t_{PLH}	$C_L=50pF$	10		16		19	ns
		$C_L=150pF$	13		21		25	
	t_{PHL}	$C_L=50pF$	10		16		19	
		$C_L=150pF$	13		21		25	
Propagation Delay, $\overline{G2}$ to $\overline{P<Q}$ ('686 Only)	t_{PLH}	$C_=50pF$	11		19		23	ns
		$C_L=150pF$	14		24		29	
	t_{PHL}	$C_L=50pF$	11		19		23	
		$C_L=150pF$	14		24		29	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Compares Two 8-Bit Words**
- **Choice of Totem-pole ('688) and open-drain ('689) outputs ('688 is identical to '521)**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High output drive**
  (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

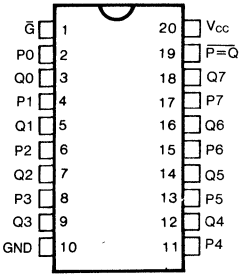
DESCRIPTION

These identity comparators perform comparisons of two 8-bit binary or BCD words. The outputs of the '688 are totempole, while '688's are open-drain.

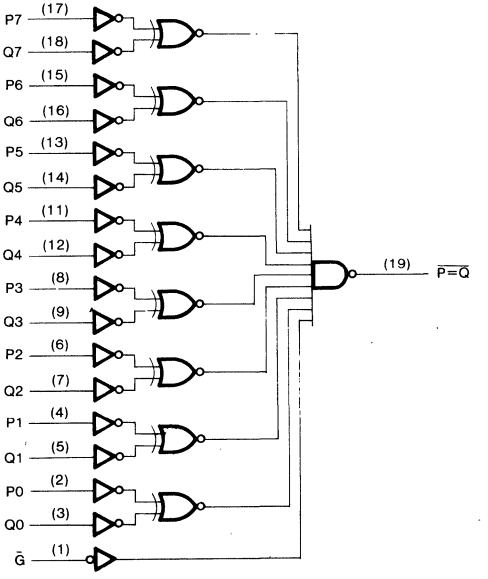
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	P=Q
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage ('688 only)	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current ('689 only)	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT688

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, P to $\overline{P=Q}$	t_{PLH}	$C_L = 50pF$	12		19		23	ns
		$C_L = 150pF$	15		24		29	
	t_{PHL}	$C_L = 50pF$	12		19		23	
		$C_L = 150pF$	15		24		29	
Propagation Delay, Q to $\overline{P=Q}$	t_{PLH}	$C_L = 50pF$	12		19		23	ns
		$C_L = 150pF$	15		24		29	
	t_{PHL}	$C_L = 50pF$	12		19		23	
		$C_L = 150pF$	15		28		29	
Propagation Delay, $\overline{G}$ to $\overline{P=Q}$	t_{PLH}	$C_L = 50pF$	11		17		20	ns
		$C_L = 150pF$	14		22		26	
	t_{PHL}	$C_L = 50pF$	11		17		20	
		$C_L = 150pF$	14		22		26	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT689

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, P to $\overline{P=Q}$	t_{PLH}	$C_L = 50pF$	19		28		33	ns
		$C_L = 150pF$	22		33		39	
	t_{PHL}	$C_L = 50pF$	14		23		28	
		$C_L = 150pF$	17		28		34	
Propagation Delay, Q to $\overline{P=Q}$	t_{PLH}	$C_L = 50pF$	19		28		33	ns
		$C_L = 150pF$	22		33		39	
	t_{PHL}	$C_L = 50pF$	14		23		28	
		$C_L = 150pF$	17		28		34	
Propagation Delay, $\overline{G}$ to $\overline{P=Q}$	t_{PLH}	$C_L = 50pF$	16		23		27	ns
		$C_L = 150pF$	19		28		33	
	t_{PHL}	$C_L = 50pF$	11		18		22	
		$C_L = 150pF$	16		23		28	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

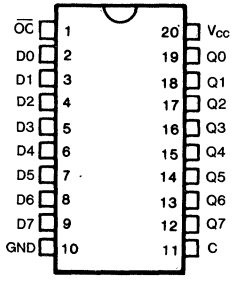
Preliminary Specifications

FEATURES

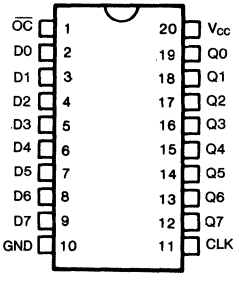
- **I/O port configuration enables output data back onto input bus**
- **Latch ('793) and and Register ('794) options**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'793



'794



DESCRIPTION

These are 8-bit latches/registers that allow temporary storage and retrievel of data on a bus. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in a '793 or '794, for verification and/or updating.

The Data is loaded in the registers on the positive-edge of the clock (CLK) for the '794. The data is passed through the '793 when C is high, and it is latched when C goes low. The output control ($\overline{OC}$) is used to erable data on the D0-D7 pins. when $\overline{OC}$ is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When $\overline{OC}$ is high, D0-D7 are inputs to the latches/registors configuring D as an input bus.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

'793

C	$\overline{OC}$	Q	D
L	L	Q_0**	Output, Q
L	H	Q_0**	Input
H†	L	D*	Output, Q*
H	H	D	Input

* In this case the output of the latch feeds the input, and a "race" condition results.

** Q_0 represents the previous "latched" state.

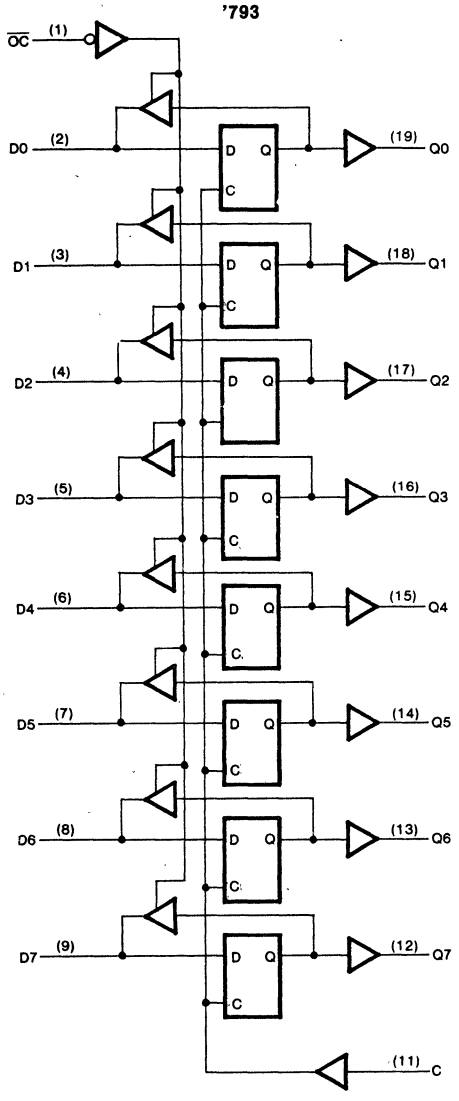
† This transition is not a normal mode of operation and may produce hazards.

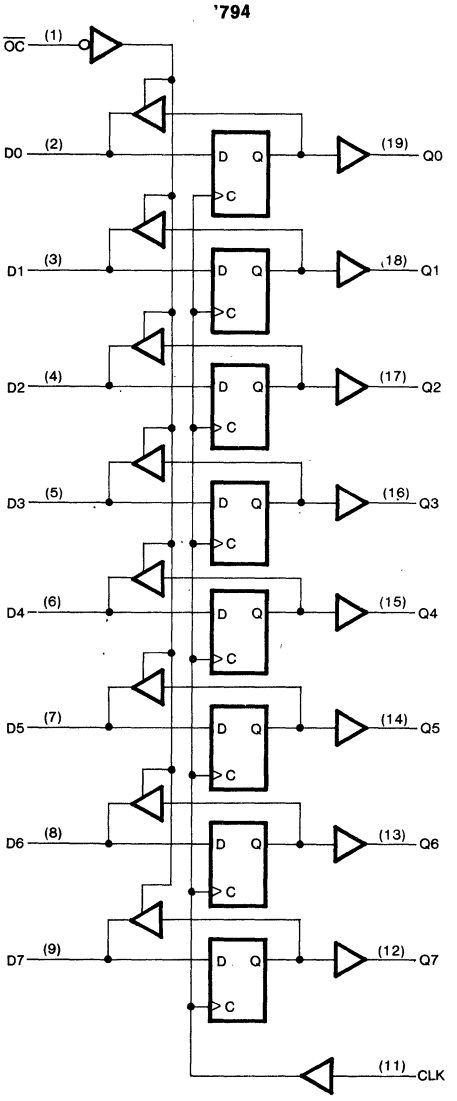
'794

CLK	$\overline{OC}$	Q	D
L or H or ↓	L	Q_0	Output, Q
L or H or ↓	H	Q_0	Input
↑	L	Q_0	Output, Q*
↑	H	D	Input

* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_0.

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a =25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT793, AHCT794

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Operating Frequency ('794 only)	t_{max}	$C_L = 50pF$	60	40		35		MHz
Propagation Delage D to Any Q ('793 only)	t_{PLH}	$C_L = 50pF$	10		16		19	ns
		$C_L = 150pF$	13		21		25	
	t_{PHL}	$C_L = 50pF$	10		16		19	
		$C_L = 150pF$	13		21		25	
Propagation Delage CLK/C to Any Q	t_{PLH}	$C_L = 50pF$	12		20		24	ns
		$C_L = 150pF$	15		25		30	
	t_{PHL}	$C_L = 50pF$	12		20		24	
		$C_L = 150pF$	15		25		30	
Enable Time, $\overline{OC}$ to D	t_{PZH}	$R_L = 1k\Omega$ (C=Low for '793) $C_L = 50pF$	11		18		22	ns
		$C_L = 150pF$	14		23		28	
	t_{PZL}	$C_L = 50pF$	11		18		22	
		$C_L = 150pF$	13		23		28	
Disable Time $\overline{OC}$ to D	t_{PHZ}	$R_L = 1K\Omega$ $C_L = 50pF$ (C=Low for '793)	11		18		22	ns
	t_{PLZ}		11		18		22	
Pulse Width, CLK/C High or low	t_W		9	14		19		ns
Setup time D before C↓ ('793)	t_{su}		6	10		12		ns
D before CLK↑('794)			10	15		20		
Hold Time D after C↓ ('793)	t_h		9	10		12		ns
D after CLK↑ ('794)			−3	0		0		
Input Capcitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	$\overline{OC}$=GND	10					pF
Power Dissipation Capacitance*	C_{PD}							ns

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

4

KS54AHCT / KS74AHCT 821/822

10-Bit Bus Interface Flip-Flops with 3-State Outputs

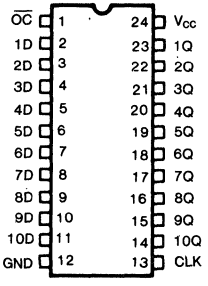
Preliminary Specifications

FEATURES

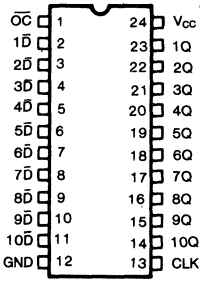
- **Functionally Equivalent to AMD's Am29821 and Am29822**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Power-Up-High-Impedance State**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'821



'822



DESCRIPTION

These 10-bit bus-interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

All of the flip-flops are edge-triggered and D-type. On the positive transition of the clock the Q outputs on the '821 will be true, and on the '822 will be complementary to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

(Each Flip-Flop)
'821

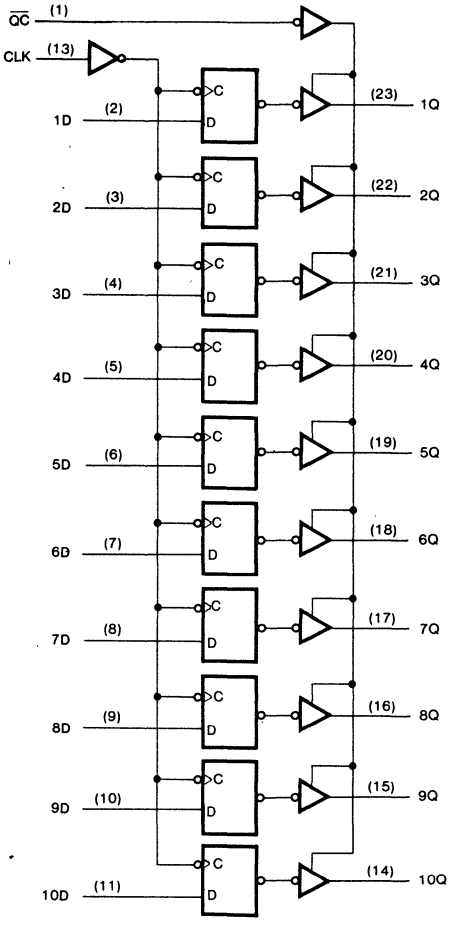
Inputs			Output
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
L	H	X	Q_0
H	X	X	Z

'822

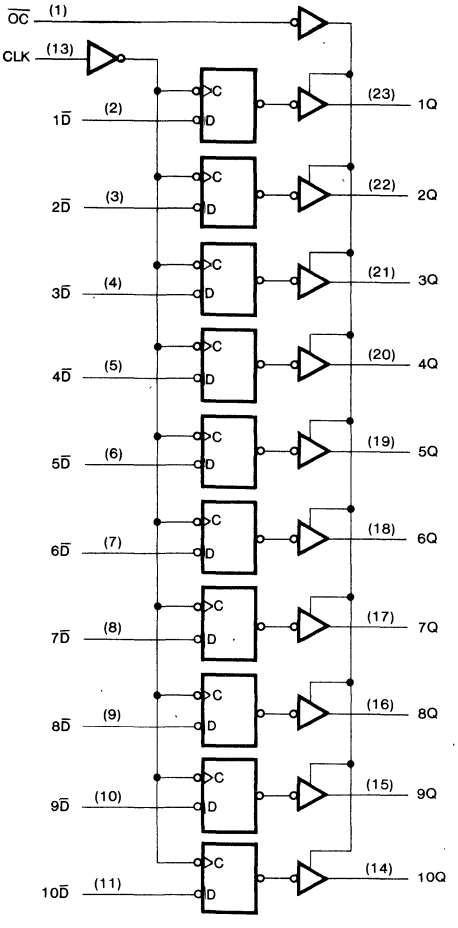
Inputs			Output
$\overline{OC}$	CLK	$\overline{D}$	Q
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
L	H	X	Q_0
H	X	X	Z

LOGIC DIAGRAMS

'821



'822



4

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT821, AHCT822

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Operating Frequency	f_{max}	$C_L = 50pF$	50	35		30		MHz
Propagation Delay CLK to any Q	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	8 11		14 19		17 23	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	8 11		14 19		17 23	
Output Enable Time, $\overline{OC}$ to any Q	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	11 14		18 23		22 28	ns
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	11 14		18 23		22 28	
Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	13		18		22	ns
	t_{PLZ}		13		18		22	
Pulse Width, CLK High or Low	t_w		9	15		18		ns
Setup Time, Data before CLK†	t_{su}		9	14		17		ns
Hold Time, Data after CLK†	t_h		−3	0		0		ns
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC} = V_{CC}$ $\overline{OC} = GND$	5 30					pF pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4

KS54AHCT 823/824
KS74AHCT

9-Bit Bus Interface Flip-Flops with 3-State Outputs

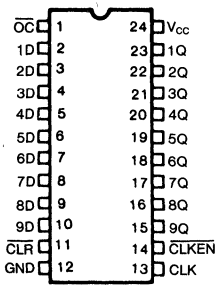
Preliminary Specifications

FEATURES

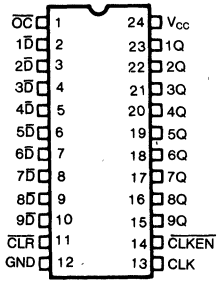
- **Functionally Equivalent to AMD's Am29823 and Am29824**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Power-Up-High-Impedance State**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'823



'824



DESCRIPTION

These 9-bit bus interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable ($\overline{CLKEN}$) low, the D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The '823 has noninverting D inputs and the '824 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ($\overline{OC}$) can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

'823

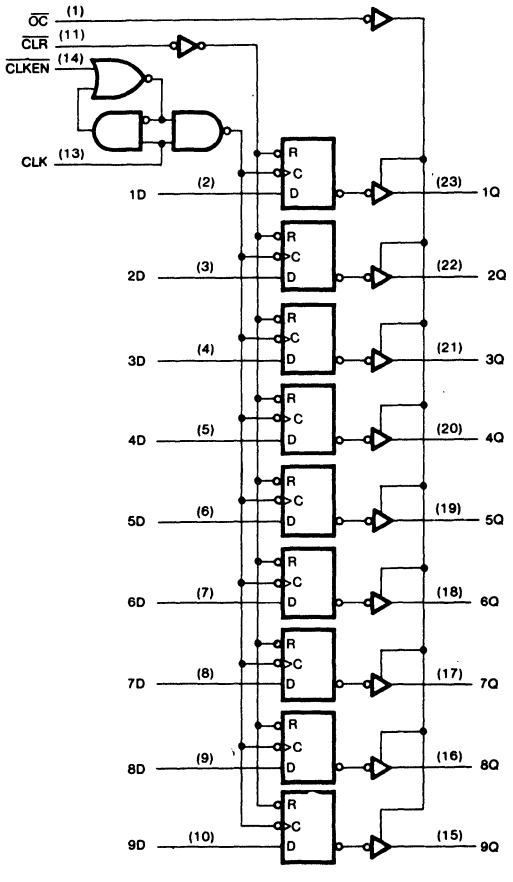
INPUT					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'824

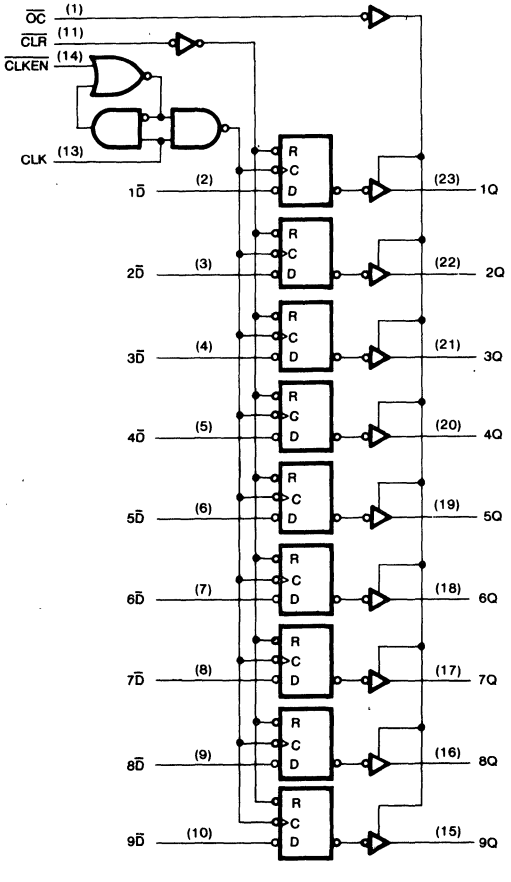
INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

LOGIC DIAGRAMS

'823



'824



4

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT823, AHCT824

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Min	Max	Min	Max	
Maximum Operating Frequency		f_{max}	$C_L = 50pF$	50	35		30		MHz
Propagation Delay CLK to any Q		t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	8 11		14 19		17 23	ns
		t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	8 11		14 19		17 23	ns
Propagation Delay, CLR to Any Q		t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	10 13		17 22		21 27	ns
Output Enable Time, $\overline{OC}$ to any Q		t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	11 14		18 23		22 28	ns
		t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	11 14		18 23		22 28	ns
Output Disable Time, $\overline{OC}$ to any Q		t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	13		18		22	ns
		t_{PLZ}		13		18		22	
Pulse Width	$\overline{CLR}$ low	t_w		9	15		18		ns
	CLK high or low			9	15		18		
Setup Time before CLK↑	$\overline{CLR}$ inactive	t_{su}		9	14		17		ns
	Data			9	14		17		
	$\overline{CLKEN}$ high or low			9	14		17		
Hold Time, $\overline{CLKEN}$ or data after CLK↑		t_h		−3	0		0		ns
Input Capacitance		C_{IN}		5					pF
Output Capacitance		C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)		C_{PD}	$\overline{OC} = V_{CC}$ $\overline{OC} = GND$	5 30					pF pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

4

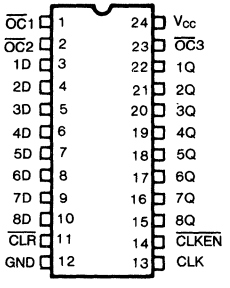
Preliminary Specifications

FEATURES

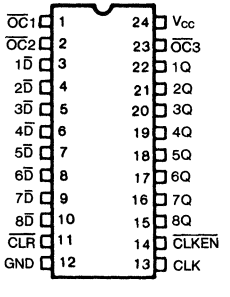
- **Functionally Equivalent to AMD's Am29825 and Am29826**
- **Improved I_{OH} Specifications**
- **Multiple Output Enables Allow Multiuser Control of the Interface**
- **Power-Up High-Impedance State**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'825



'826



DESCRIPTION

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing multi-user buffer registers, I/O ports, bus drivers and working registers.

With the clock enable ($\overline{CLKEN}$) low, all D-type edge-triggered flip-flops enter data on the low-to-high transition of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The '825 has non-inverting D inputs and the '826 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ inputs low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

'825

Inputs					Output
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

* $\overline{OC}$ = H if any of $\overline{OC}$1, $\overline{OC}$2, or $\overline{OC}$3 are high.
$\overline{OC}$ = L if all of $\overline{OC}$1, $\overline{OC}$2, and $\overline{OC}$3 are low.

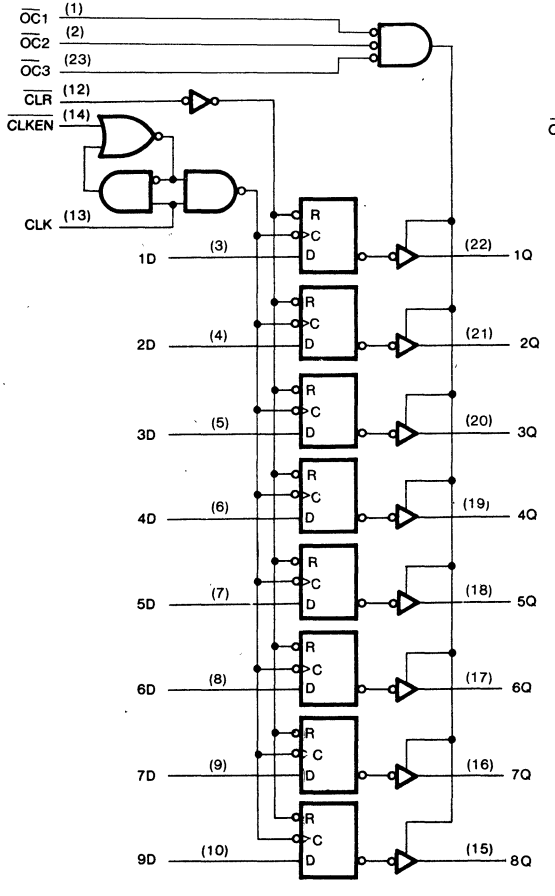
'826

Inputs					Output
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

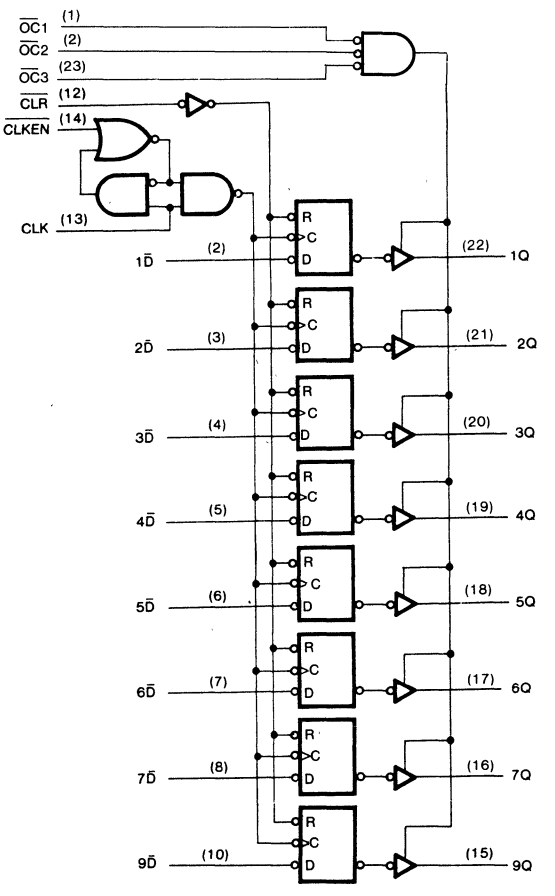
* $\overline{OC}$ = H if any of $\overline{OC}$1, $\overline{OC}$2, or $\overline{OC}$3 are high.
$\overline{OC}$ = L if all of $\overline{OC}$1, $\overline{OC}$2, and $\overline{OC}$3 are low.

LOGIC DIAGRAMS

'825



'826



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT825, AHCT826

Characteristic		Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
					Typ	Min	Max	Min	Max	
Maximum Operating Frequency		f_{max}	C_L=50pF		50	35		30		MHz
Propagation Delay CLK to any Q		t_{PLH}	C_L=50pF C_L=150pF		8 11		14 19		17 23	ns
		t_{PHL}	C_L=50pF C_L=150pF		8 11		14 19		17 23	
Propagation Delay, $\overline{CLR}$ to Any Q		t_{PHL}	C_L=50pF C_L=150pF		10 13		17 22		21 27	ns
Output Enable Time, $\overline{OC}$ to any Q		t_{PZH}	R_L=1kΩ	C_L=50pF C_L=150pF	11 14		18 23		22 28	ns
		t_{PZL}	R_L=1kΩ	C_L=50pF C_L=150pF	11 14		18 23		22 28	
Output Disable Time, $\overline{OC}$ to any Q		t_{PHZ}	R_L=1kΩ		13		18		22	ns
		t_{PLZ}	C_L=50pF		13		18		22	
Pulse Width	$\overline{CLR}$ low	t_w			9	15		18		ns
	CLK high or low				9	15		18		
Setup Time before CLK↑	$\overline{CLR}$ inactive	t_{su}			9	14		17		ns
	Data				9	14		17		
	$\overline{CLKEN}$ high or low				9	14		17		
Hold Time, $\overline{CLKEN}$ or data after CLK↑		t_h			−3	0		0		ns
Input Capacitance		C_{IN}			5					pF
Output Capacitance		C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance* (per stage)		C_{PD}	$\overline{OC}$=V_{CC} $\overline{OC}$=GND		5 30					pF pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

KS54AHCT KS74AHCT 841/842

10-Bit Bus Interface D-Type Latches with 3-State Outputs

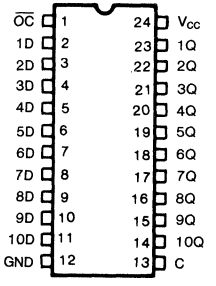
Preliminary Specifications

FEATURES

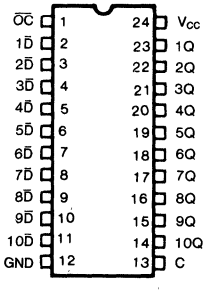
- **Bus-Structured Pinout**
- **Provides Extra Bus Driving Latches**
- **Necessary for Wider Address/Data Paths or Buses with Parity**
- **Power-Up High-Impedance State**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'841



'842



DESCRIPTION

These 10-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The '841 has noninverting data (D) inputs and the '842 has inverting ($\overline{D}$) inputs.

A buffered output control ($\overline{OC}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

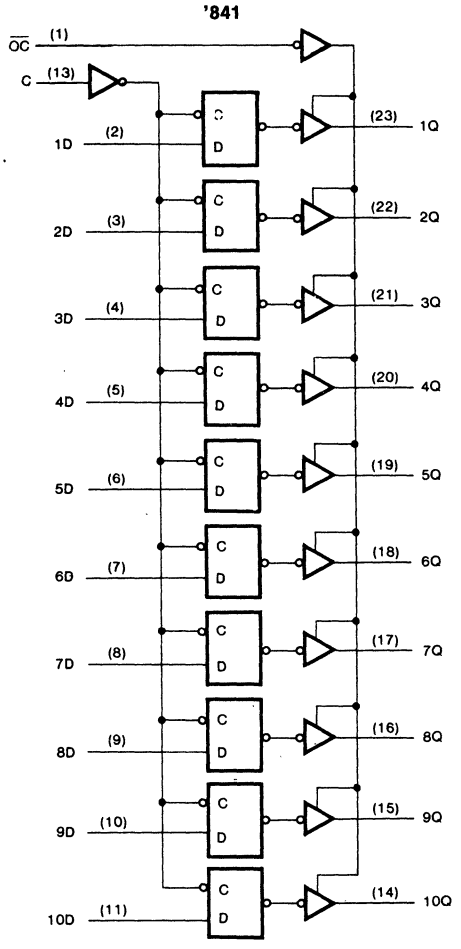
'841

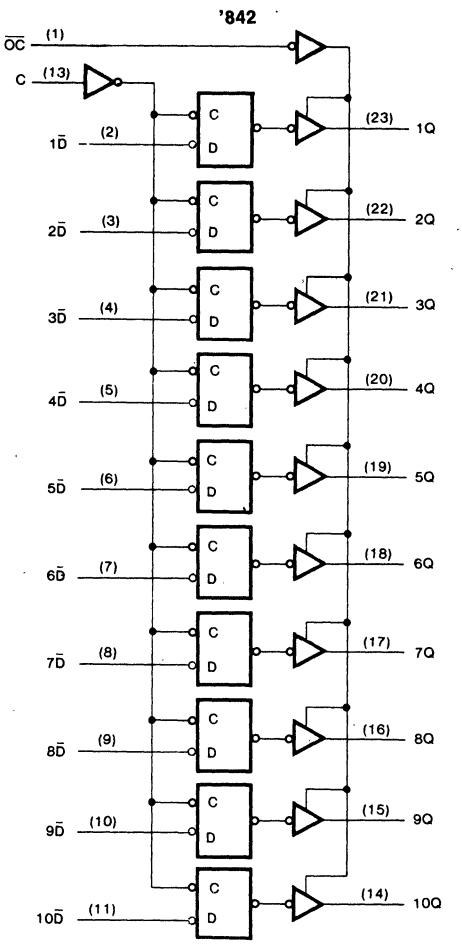
Inputs			Output
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'842

Inputs			Output
$\overline{OC}$	C	$\overline{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM S





Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT841, AHCT842

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Data to Q	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	10 13		16 21		19 25	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	10 13		16 21		19 25	
Propagation Delay, C to any Q	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	15 18		24 29		29 35	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	15 18		24 29		29 35	
Output Enable Time, $\overline{OC}$ to any Q	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	13 16		18 23		22 28	ns
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	13 16		18 23		22 28	
Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	13		18		22	ns
	t_{PLZ}		13		18		22	
Pulse Width, C High	t_w		12	20		25		ns
Setup Time, Data before C↓	t_{su}		6	10		12		ns
Hold Time, Data after C↓	t_h		3	5		7		ns
Input Capcitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC} = V_{CC}$ $\overline{OC} = GND$	5 30					pF pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

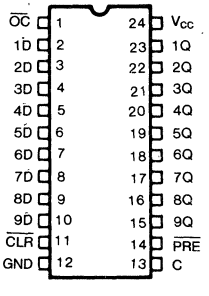
4

FEATURES

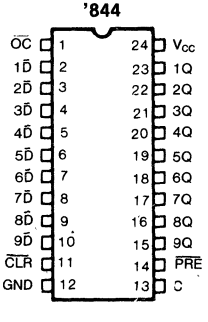
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Power-Up High Impedance**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'843



'844



DESCRIPTION

These 9-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers and working registers.

The nine latches are transparent D-type. The '843 has noninverting data (D) inputs and the '844 has inverting $\overline{D}$ inputs.

A buffered output control ($\overline{OC}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

'843

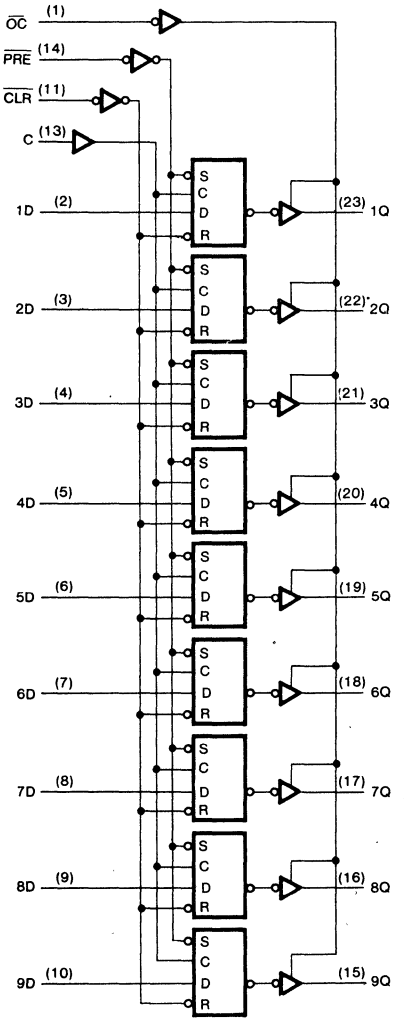
INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

'844

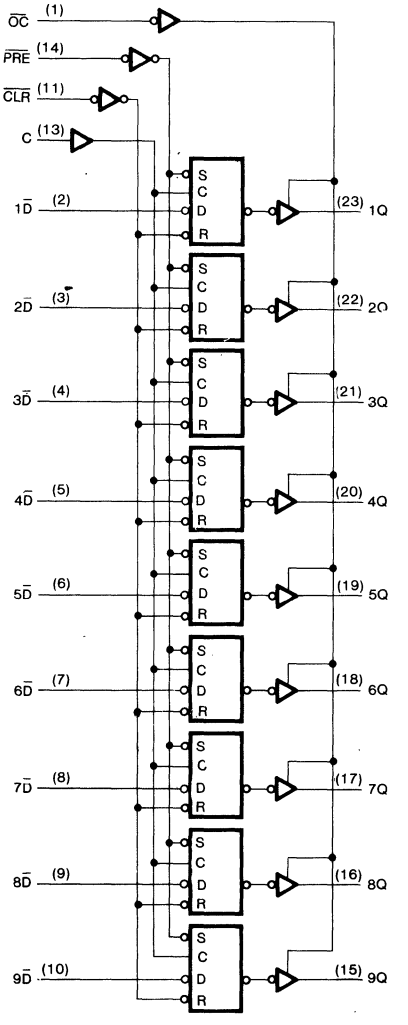
INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	$\overline{D}$	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	Q_0
X	X	H	X	X	Z

LOGIC DIAGRAMS

'843



'844



4

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O= −6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT843, AHCT844

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Data to Q	t_{PLH}	$C_L = 50pF$	13		18		22	ns
		$C_L = 150pF$	16		23		28	
	t_{PHL}	$C_L = 50pF$	13		18		22	
		$C_L = 150pF$	16		23		28	
Propagation Delay, C to any Q	t_{PLH}	$C_L = 50pF$	16		26		31	ns
		$C_L = 150pF$	19		31		37	
	t_{PHL}	$C_L = 50pF$	16		26		31	
		$C_L = 150pF$	19		31		37	
Propagation Delay, $\overline{PRE}$ to Q	t_{PLH}	$C_L = 50pF$	17		27		32	ns
		$C_L = 150pF$	20		32		38	
Propagation Delay, $\overline{CLR}$ to Q	t_{PHL}	$C_L = 50pF$	17		27		32	ns
		$C_L = 150pF$	20		32		38	
Output Enable Time, $\overline{OC}$ to any Q	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$	11		18		22	ns
		$R_L = 1k\Omega$, $C_L = 150pF$	14		23		28	
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$	11		18		22	
		$R_L = 1k\Omega$, $C_L = 150pF$	14		23		28	
Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	13		18		22	ns
	t_{PLZ}		13		18		22	
Pulse Width, C High	t_w		12	20		25		ns
Setup Time, Data before C↓	t_{SU}		8	10		12		ns
Hold Time, Data after C↓	t_h		3	5		7		ns
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC} = V_{CC}$	5					pF
		$\overline{OC} = GND$	30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

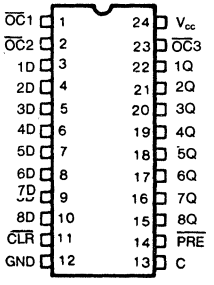
Preliminary Specifications

FEATURE

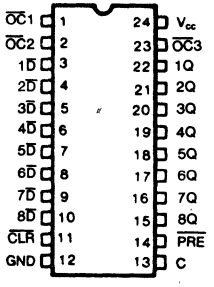
- **3-state buffer-type outputs drive bus-lines directly**
- **Bus-structured pinout**
- **Provides extra bus driving latches necessary for wider address/data paths or buses with parity**
- **Low power consumption characteristic of CMOS devices**
- **3-state outputs with high drive current (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface**
- **Direct interface capability with TTL, NMOS and CMOS devices**
- **Wide operating volage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to 125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'845



'846



DESCRIPTION

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The '845 has noninverting data(D) inputs. The '846 has inverting D inputs. Since $\overline{CLR}$ and $\overline{PRE}$ are independent of the clock, taking the $\overline{CLR}$ input low will cause the eight Q outputs to go low. Taking the $\overline{PRE}$ input low will cause the eight Q outputs to go high. When both $\overline{PRE}$ and $\overline{CLR}$ are taken low, the outputs will follow the preset condition.

The buffered output control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impendance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

'845

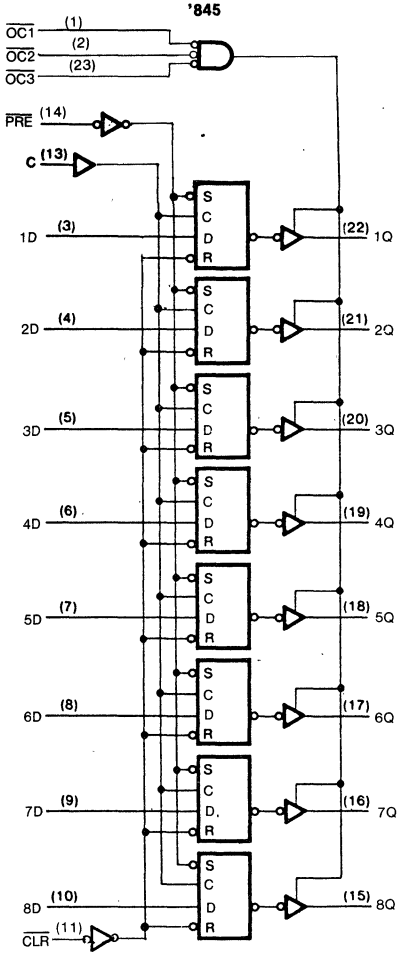
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

'846

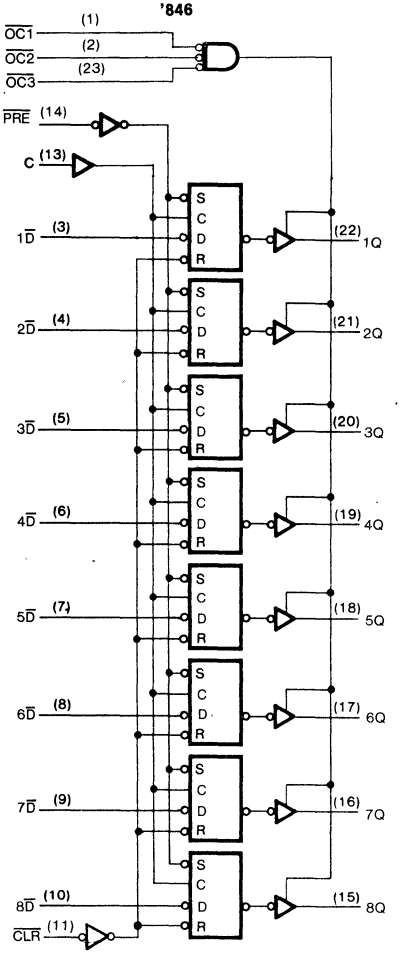
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	$\overline{D}$	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

LOGIC DIAGRAMS

'845



'846



4

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT845

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay Clk to Q	t_{PLH}		13		22		26	ns
	t_{PHL}		13		22		26	
Propagation Delay D to Q	t_{PLH}		8		15		20	ns
	t_{PHL}		8		15		20	
Propagation Delay $\overline{CLR}$ to Q	t_{PLH}		16		26		31	ns
	t_{PHL}		16		26		31	
Propagation Delay $\overline{PRE}$ to Q	t_{PLH}		16		26		31	ns
	t_{PHL}		16		26		31	
Propagation Delay $\overline{OC}$ to Q	t_{PZH}		12		20		24	ns
	t_{PZL}		12		20		24	
Propagation Delay $\overline{OC}$ to Q	t_{PHZ}		12		20		24	ns
	t_{PLZ}		12		20		24	
Input Capacitance	C_{IN}		5					pF
Power dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT846

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay Clk to Q	t_{PLH}		14		24		32	ns
	t_{PHL}		14		24		32	
Propagation Delay $\overline{D}$ to Q	t_{PLH}		10		17		22	ns
	t_{PHL}		10		17		22	
Propagation Delay $\overline{CLR}$ to Q	t_{PLH}		13		22		26	ns
	t_{PHL}		13		22		26	
Propagation Delay $\overline{PRE}$ to Q	t_{PLH}		13		22		26	ns
	t_{PHL}		13		22		26	
Propagation Delay $\overline{OC}$ to Q	t_{PZH}		12		20		24	ns
	t_{PZL}		12		20		24	
Propagation Delay $\overline{OC}$ to Q	t_{PHZ}		12		20		24	ns
	t_{PLZ}		12		20		24	
Input Capacitance	C_{IN}		5					pF
Power dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Modified input structure allows voltages up to 15V**
- **High-Drive-current Outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Low power consumption characteristic of CMOS**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

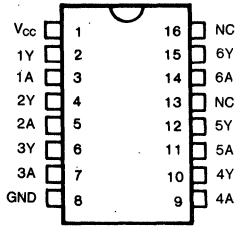
DESCRIPTION

The '4049 and '4050 have a modified input protection structure that enable them to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0-15V logic can be corverted to 0-5V logic when using a 5V supply. The modified input protection has no diode connected to V_{CC}, thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition the '4049 and '4050 can be used as simple buffers or inverters without level translation.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

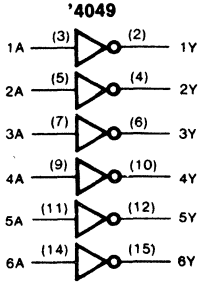
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

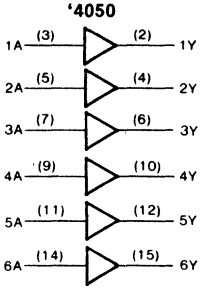


LOGIC DIAGRAMS

'4049



'4050



FUNCTION TABLE

Input A	Output Y	
	'4049	'4050
H	L	H
L	H	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > +15.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND V_{IN}=15V		±0.1	±1.0 ±10.0	±1.0 ±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT4049, AHCT4050

Characteristic	Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C V_{CC} = 5.0V±10%		KS54AHCT T_a = −55°C to +125°C V_{CC} = 5.0V± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	C_L=50pF	7		12		14	ns
	t_{PHL}		7		12		14	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

NOTES

KS54/74HCTLS DATA SHEETS 5

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

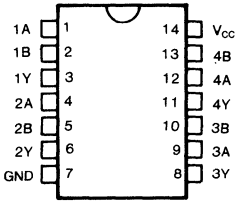
DESCRIPTION

These devices contain four independent 2-input NAND gates that perform the Boolean functions $Y=\overline{A \bullet B}$ or $Y=\overline{A}+\overline{B}$.

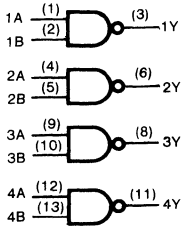
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	**B**	**Y**
H	H	L
L	X	H
X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS00

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay	t_{PLH}	C_L=50pF	10	15	18	22	ns
	t_{PHL}		10	15	18	22	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Quad 2-Input NAND Gates with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

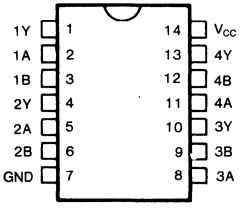
DESCRIPTION

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

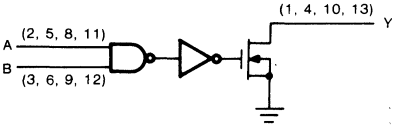
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

5

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq$6 ns), HCTLS01

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Guaranteed Limits				
Maximum Propagation Delay	t_{PLH}	C_L=50pF R_L=1kΩ	24	30	36	43		ns
	t_{PHL}		15	20	25	30		
Maximum Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Quad 2-Input NOR Gates

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

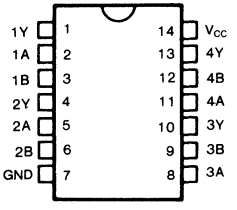
DESCRIPTION

These devices contain four independent 2-input NOR gates that perform the Boolean functions $Y=\overline{A+B}$ or $Y=\overline{A}\bullet\overline{B}$.

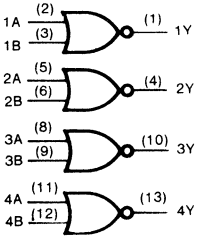
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	B	Y
H	X	L
X	H	L
L	L	H

5

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS02

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay	t_{PLH}	C_L=50pF	9	15	18	22	ns
	t_{PHL}		10	15	18	22	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}
† For AC switching test circuits and timing waveforms see section 2.

Quad 2-Input NAND Gates with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current Outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

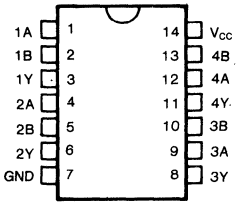
DESCRIPTION

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

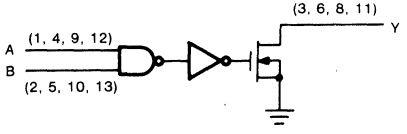
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS03

Characteristic	Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V	KS74HCTLS T_a = −40°C to +85°C V_{CC} = 5.0V ± 10%		KS54HCTLS T_a = −55°C to +125°C V_{CC} = 5.0V ± 10%		Unit
			Typ	Guaranteed Limits				
Maximum Propagation Delay	t_{PLH}	C_L=50pF R_L=1kΩ	24	30	36	43		ns
	t_{PHL}		15	20	25	30		
Maximum Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

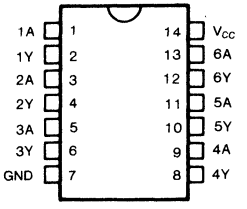
DESCRIPTION

These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

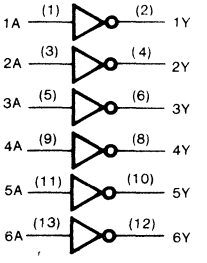
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Inverter)

Input A	Output Y
H	L
L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS04

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54 HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay	t_{PLH}	C_L=50pF	9	15	18	22	ns
	t_{PHL}		10	15	18	22	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

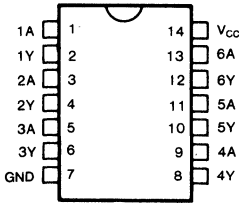
DESCRIPTION

These devices contain six independent inverters with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

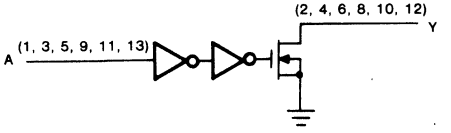
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Inverter)

Input	Output
A	**Y**
H	L
L	H

5

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS05

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54 HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Guaranteed Limits				
Maximum Propagation Delay	t_{PLH}	C_L=50pF R_L=1kΩ	24	30	36	43		ns
	t_{PHL}		16	22	28	33		
Maximum Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Quad 2-Input AND Gates

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

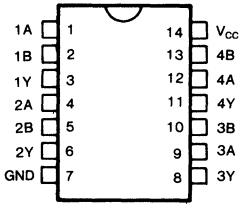
DESCRIPTION

These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$.

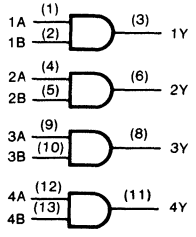
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	**B**	**Y**
H	H	H
L	X	L
X	L	L

5

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS08

Characteristic	Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V		KS74HCTLS T_a = −40°C to +85°C V_{CC} = 5.0V ± 10%	KS54HCTLS T_a = −55°C to +125°C V_{CC} = 5.0V ± 10%	Unit
			Typ		Guaranteed Limits		
Maximum Propagation Delay	t_{PLH}	C_L=50pF	10	15	18	22	ns
	t_{PHL}		10	20	25	30	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Quad 2-Input AND Gates with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

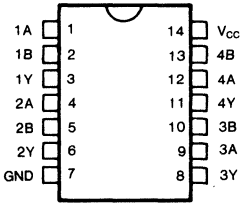
DESCRIPTION

These devices contain four independent 2-input AND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

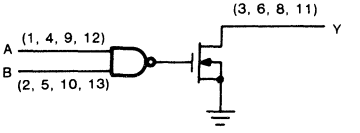
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	B	Y
H	H	H
L	X	L
X	L	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS09

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits		
Maximum Propagation Delay	t_{PLH}	C_L=50pF R_L=1kΩ	26	32	38	45	ns
	t_{PHL}		16	22	28	33	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Triple 3-Input NAND Gates

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

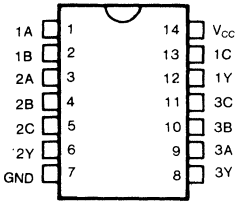
DESCRIPTION

These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y=\overline{A \bullet B \bullet C}$ or $Y=\overline{A}+\overline{B}+\overline{C}$.

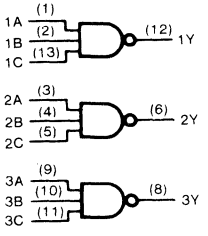
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs			Output
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS10

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74 HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay	t_{PLH}	C_L=50pF	11	15	19	23	ns
	t_{PHL}		11	15	19	23	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Triple 3-Input AND Gates

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

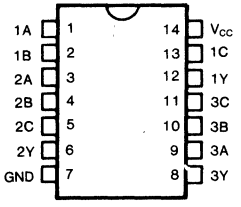
DESCRIPTION

These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \bullet B \bullet C$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$.

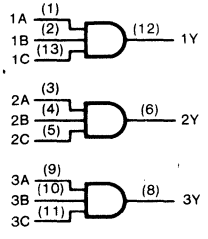
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs			Output
A	**B**	**C**	**Y**
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

5

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS11

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Guaranteed Limits				
Maximum Propagation Delay	t_{PLH}	C_L=50pF	13	18	22	26		ns
	t_{PHL}		13	18	22	26		
Maximum Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Triple 3-Input NAND Gates with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

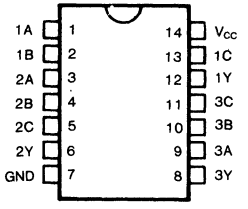
These devices contain three independent 3-input NAND gates with open-drain outputs. They perform the Boolean functions $Y=\overline{A \bullet B \bullet C}$ or $Y=\overline{A}+\overline{B}+\overline{C}$.

Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

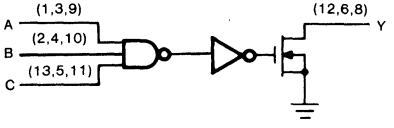
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs			Output
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS12

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits		
Maximum Propagation Delay	t_{PLH}	C_L=50pF R_L=1kΩ	26	32	38	45	ns
	t_{PHL}		16	22	28	33	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

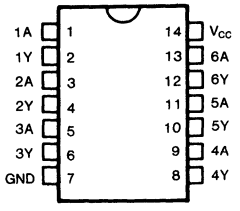
DESCRIPTION

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y=\overline{A}$.

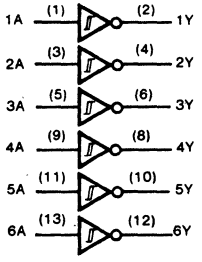
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Inverter)

Input	Output
A	**Y**
H	L
L	H

5

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} +0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} +0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} +0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a= −40°C to +85°C	KS54HCTLS T_a= −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.11 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	T_a=25°C		KS74HCTLS T_a= −40°C to +85°C		KS54HCTLS T_a= −55°C to +125°C		Unit
			Min	Max	Min	Max	Min	Max	
Positive-Going Threshold Voltage	V_{T+}	V_{CC}=4.5V	1.2	1.9	1.2	1.9	1.2	1.9	V
		V_{CC}=5.5V	1.4	2.1	1.4	2.1	1.4	2.1	
Negative-Going Threshold Voltage	V_{T-}	V_{CC}=4.5V	0.5	1.2	0.5	1.2	0.5	1.2	V
		V_{CC}=5.5V	0.6	1.4	0.6	1.4	0.6	1.4	
Hysteresis (V_{T+}-V_{T-})	V_H	V_{CC}=4.5V	0.4	1.4	0.4	1.4	0.4	1.4	V
		V_{CC}=5.5V	0.4	1.5	0.4	1.5	0.4	1.5	

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS14

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74 HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay	t_{PLH}	$C_L = 50pF$	15	20	25	30	ns
	t_{PHL}		16	22	28	33	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

5

Dual 4-Input NAND Gates

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

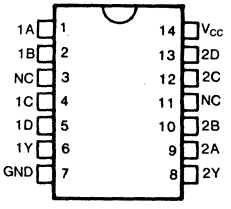
DESCRIPTION

These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y=\overline{A \bullet B \bullet C \bullet D}$ or $Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic.

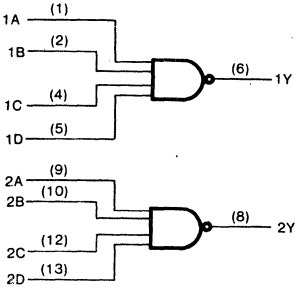
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS20

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54 HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits		
Maximum Propagation Delay Any Input to Y	t_{PLH}	C_L=50pF	11	15	19	23	ns
	t_{PHL}		11	15	19	23	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

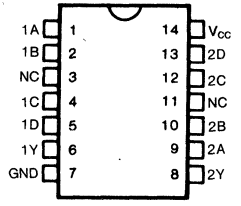
DESCRIPTION

These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y=A\bullet B\bullet C\bullet D$ or $Y=\overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$ in positive logic.

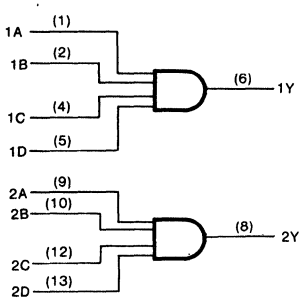
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS21

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ		Guaranteed Limits		
Maximum Propagation Delay Any Input to Y	t_{PLH}	C_L=50pF	12	18	22	27	ns
	t_{PHL}		12	18	22	27	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

Dual 4-Input NAND Gates with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

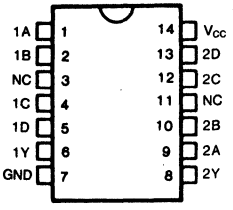
DESCRIPTION

These devices contain two independent 3-input NOR gates. gates. These gates perform the Boolean fucntions $Y=\overline{A \bullet B \bullet C \bullet D}$ or $Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They many be connected to other open-drain outputs to implement active low wired-OR or active high wired-AND functions.

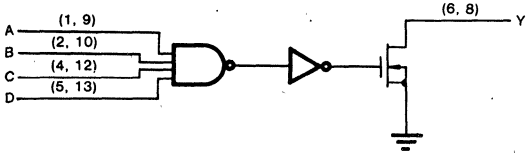
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS22

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay Any Input to Y	t_{PLH}	C_L=50pF	26	33	40	47	ns
	t_{PHL}		15	20	25	30	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

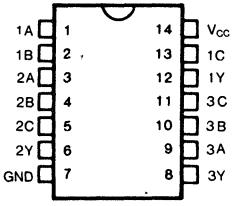
DESCRIPTION

These devices contain two independent 3-input NOR gates. They perform the Boolean functions $\overline{Y=A+B+C}$ or $Y=\overline{A}\bullet\overline{B}\bullet\overline{C}$ in positive logic.

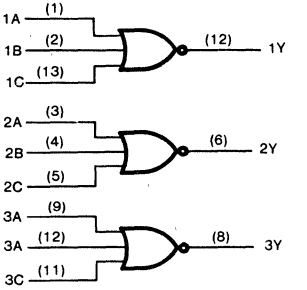
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O= −4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS27

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay Any Input to Y	t_{PLH}	C_L=50pF	11	15	19	23	ns
	t_{PHL}		13	17	22	26	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

8-Input Nand Gate

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '30 contains a single 8-input NAND gate. It performs the boolean functions (in positive logic):

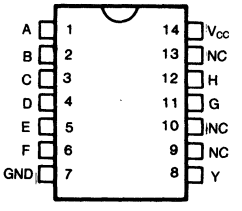
$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$

$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$

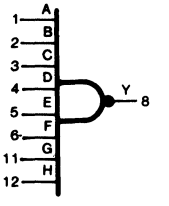
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inputs A Through H		Output Y
All Inputs	H	L
One or more inputs	L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA		0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS30

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits			
Propagation Delay	t_{PLH}	C_L=50pF	11	15	19	22	ns
	t_{PHL}		11	15	19	22	
Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}		15				pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

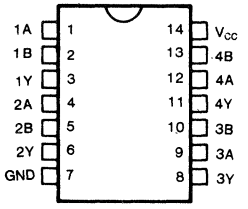
DESCRIPTION

These devices contain four independent 2-input OR gates. They perform the Boolean functions Y=A+B or Y=$\overline{\overline{A}\bullet\overline{B}}$.

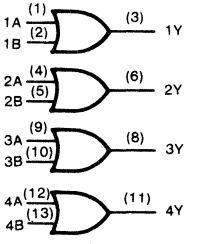
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL. NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damaged due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	B	Y
H	X	H
X	H	H
L	L	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS32

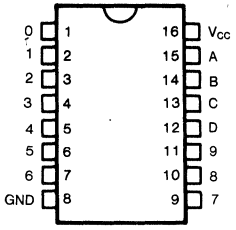
Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54 HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits		
Maximum Propagation Delay	t_{PLH}	C_L=50pF	13	17	22	26	ns
	t_{PHL}		13	17	22	26	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Full decoding of Input Logic**
- **All outputs are High for Invalid BCD Conditions**
- **Also for application as 3-Line to 8-Line Decoders**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



FUNCTION TABLE

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

DESCRIPTION

The '42 decoder accepts for active-high BCD inputs and provides 10 mutually exclusive active-low outputs, as shown by logic symbol or diagram. The active-low outputs facilitate addressing other MSI units with active-low input enables.

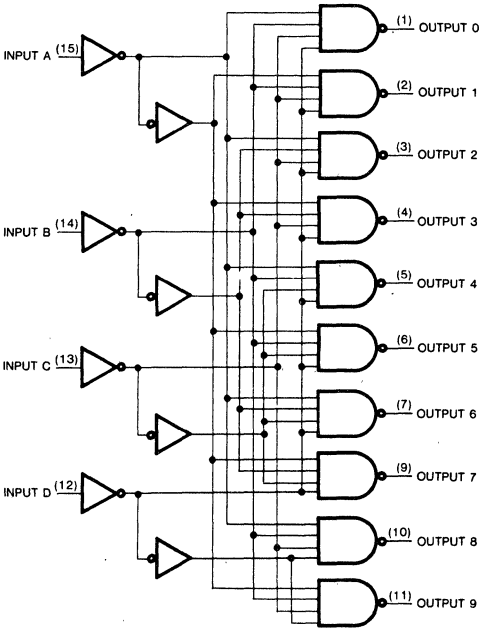
The logic design of the '42 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant input, D, produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The D input can also be used as the Data input in an 8-output demultiplexer application.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS42

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74 HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54 HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits		
Maximum Propagation Delay Any Input to Y	t_{PLH}	C_L=50pF	19	25	32	38	ns
	t_{PHL}		19	25	32	38	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74HCTLS: −40°C to +85°C KS54HCTLS: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

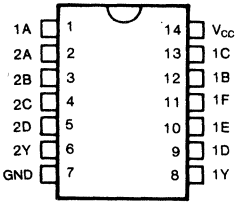
The '51 performs the following Boolean functions:
$1Y=\overline{(1A \bullet 1B \bullet 1C)+(1D \bullet 1E \bullet 1F)}$
$2Y=\overline{(2A \bullet 2B)+(2C \bullet 2D)}$

The '58 performs:
$1Y=(1A \bullet 1B \bullet 1C)+(1D \bullet 1E \bullet 1F)$
$2Y=(2A \bullet 2B)+(2C \bullet 2D)$

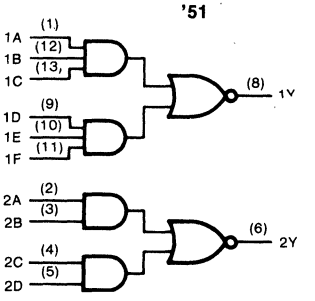
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

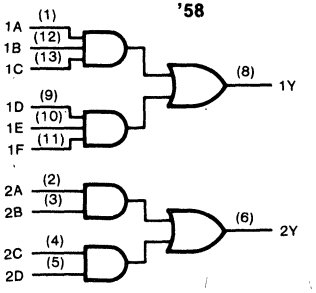
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAMS





FUNCTION TABLES

Inputs						Output 1Y	
1A	1B	1C	1D	1E	1F	'51	'58
H	H	H	X	X	X	L	H
X	X	X	H	H	H	L	H
Any other combination						H	L

Inputs				Output 2Y	
2A	2B	2C	2D	'51	'58
H	H	X	X	L	H
X	X	H	H	L	H
Any other combination				H	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS51, HCTLS58

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ		Guaranteed Limits		
Maximum Propagation Delay	t_{PLH}	C_L=50pF	13	18	23	27	ns
	t_{PHL}		13	18	23	27	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

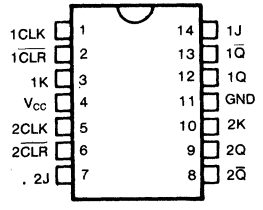
DESCRIPTION

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at $\overline{CLR}$ input resets the outputs regardless of the levels of the other inputs. When $\overline{CLR}$ is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle filp-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

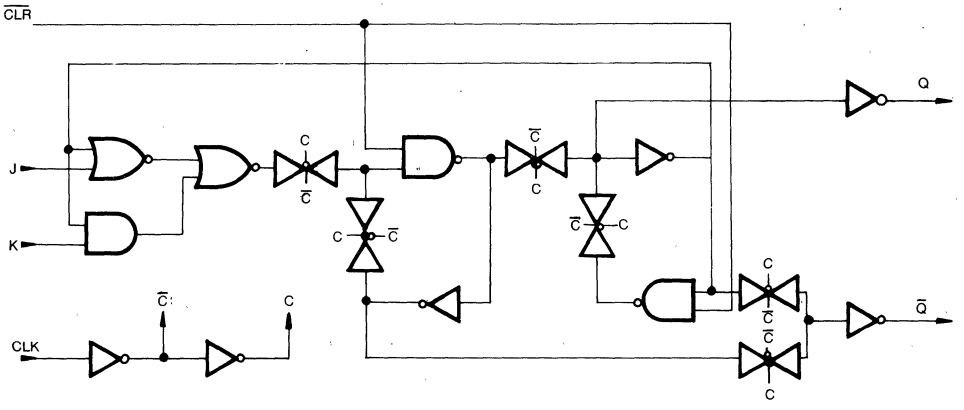
PIN CONFIGURATION



FUNCTION TABLE

Inputs				Outputs	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS73A

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30		25	21	MHz
Maximum Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		15	20		25	30	ns
		t_{PHL}		15	20		25	30	
Maximum Propagation Delay, $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		15	20		25	30	ns
		t_{PHL}		15	20		25	30	
Minimum Setup Time before CLK↓	J or K	t_{su}		10	13		17	20	ns
	$\overline{CLR}$ Inactive			10	13		17	20	
Minimum Hold Time, J or K after CLK↓		t_h		−3	0		0	0	ns
Minimum Pulse Width	CLK High or Low	t_w		10	13		17	20	ns
	$\overline{CLR}$ Low			10	13		17	20	
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per flip-flop)	40					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS / KS74HCTLS 74A

Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

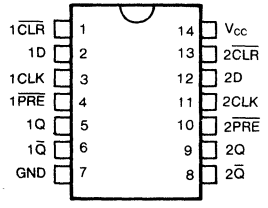
DESCRIPTION

These devices contain two independent positive-edge-triggered D-type flip-flops. Each flip-flop has its own data, clock, preset and clear inputs and complementary Q and $\overline{Q}$ outputs. The preset and clear inputs are active-low and operate independently of the clock. Data at the D input is transferred to the Q outputs on the positive transition of the clock, provided setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

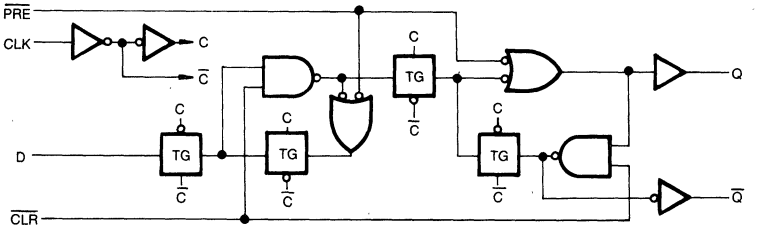


FUNCTION TABLE

Inputs				Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

*Both outputs will remain high as long as $\overline{PRE}$ and $\overline{CLR}$ are low, but the output states are unpredictable if $\overline{PRE}$ and $\overline{CLR}$ go high simultaneously.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} +0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} +0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} +0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS74A

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30	25		20	MHz
Maximum Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		18	25	31		37	ns
		t_{PHL}		30	40	50		60	
Maximum Propagation Delay, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		18	25	31		37	ns
		t_{PHL}		30	40	50		60	
Minimum Setup Time before CLK↑	Data	t_{su}		10	13	17		20	ns
	$\overline{PRE}$ or $\overline{CLR}$ Inactive			10	13	17		20	
Minimum Hold Time, J or K after CLK↓		t_h		−3	0	0		0	ns
Minimum Pulse Width	CLK High or Low	t_w		8	15	20		25	ns
	$\overline{PRE}$ or $\overline{CLR}$ Low			8	15	20		25	
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per flip-flop)	40					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

5

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '75 and '77 consist of 4 high-speed D-type latches that can be used as temporary storage for binary information between processing units. The '75 features complementary Q and $\overline{Q}$ output while the '77 features single nail output. These devices are ideal for high component density application.

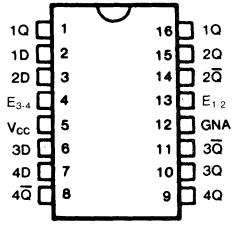
The latches are transparent: when the enable (E) is high, the Q output will follow the data input. When the enable goes low, the output latches at the level that was set up at the D-input.

These device provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

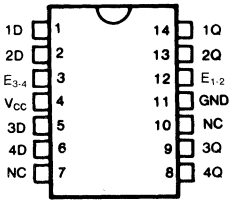
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

'75



'77



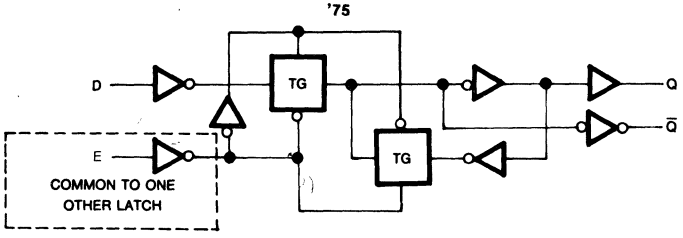
FUNCTION TABLE

Inputs		Outputs	
D	E	Q	$\overline{Q}$*
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

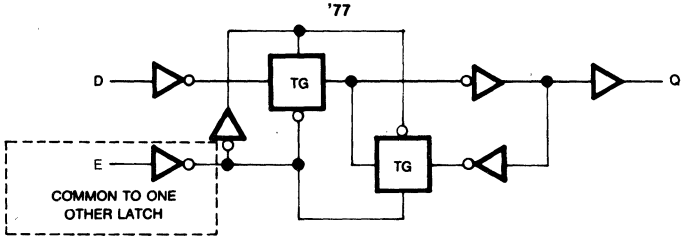
*$\overline{Q}$: '75 only

LOGIC DIAGRAM

'75



'77



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS75

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Propagation Delay, E to Q or $\overline{Q}$	t_{PLH}	$C_L = 50pF$	19	25	31	38	ns
	t_{PHL}		19	25	31	38	
Propagation Delay, D to Q or $\overline{Q}$	t_{PLH}	$C_L = 50pF$	13	21	26	32	ns
	t_{PHL}		13	21	26	32	
Data Set up Time D to E	t_{SU}		15	20	25	30	ns
Data Hold Time E to D	t_h		4	5	6	8	ns
Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS77

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Propagation Delay, E to Q	t_{PLH}	$C_L = 50pF$	13	18	23	27	ns
	t_{PHL}		13	18	23	27	
Propagation Delay, D to Q or $\overline{Q}$	t_{PLH}	$C_L = 50pF$	13	18	23	27	ns
	t_{PHL}		13	18	25	27	
Data Set up Time D to E	t_{SU}		15	20	25	30	ns
Data Hold Time E to D	t_h		4	5	6	8	ns
Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

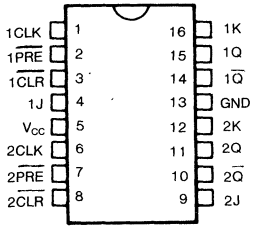
DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

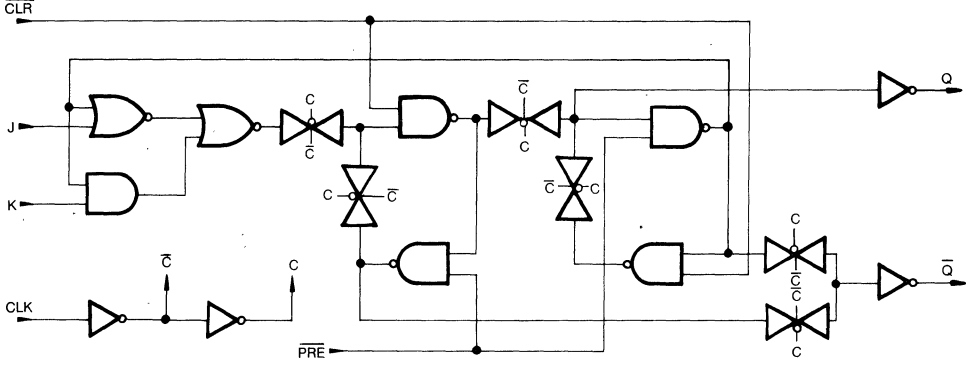


FUNCTION TABLE

Inputs					Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS76A

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30		25	21	MHz
Maximum Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		15	20		25	30	ns
		t_{PHL}		15	20		25	30	
Maximum Propagation Delay, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		15	20		25	30	ns
		t_{PHL}		15	20		25	30	
Minimum Setup Time before CLK↓	Data	t_{su}		10	13		17	20	ns
	$\overline{PRE}$ or $\overline{CLR}$ Inactive			10	13		17	20	
Minimum Hold Time, J or K after CLK↓		t_h		−3	0		0	0	ns
Minimum Pulse Width	CLK High or Low	t_w		10	13		17	20	ns
	$\overline{PRE}$ or $\overline{CLR}$ Low			10	13		17	20	
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per flip-flop)	40					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

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FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

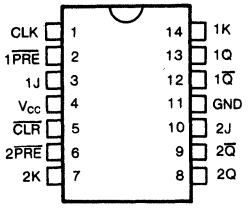
DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K and preset inputs and complementary outputs. The clear and clock inputs are common to both flip-flops. The J-K inputs are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

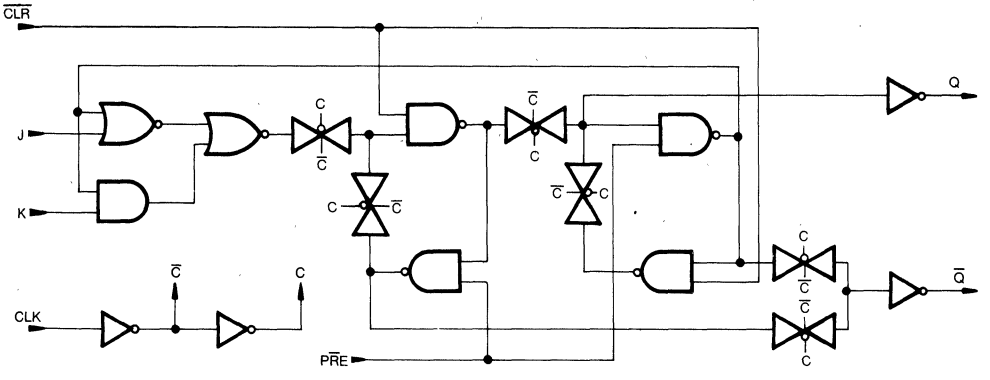


FUNCTION TABLE

Inputs					Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS78A

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30		25	21	MHz
Maximum Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		15	20		25	30	ns
		t_{PHL}		15	20		25	30	
Maximum Propagation Delay, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		15	20		25	30	ns
		t_{PHL}		15	20		25	30	
Minimum Setup Time before CLK↓	J or K	t_{su}		10	13		17	20	ns
	$\overline{PRE}$ or $\overline{CLR}$ Inactive			10	13		17	20	
Minimum Hold Time, J or K after CLK↓		t_h		−3	0		0	0	ns
Minimum Pulse Width	CLK High or Low	t_w		10	13		17	20	ns
	$\overline{PRE}$ or $\overline{CLR}$ Low			10	13		17	20	
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per flip-flop)	40					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

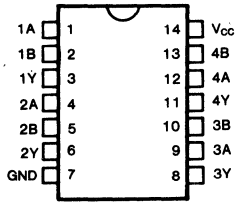
DESCRIPTION

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$.

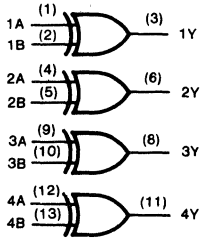
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

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Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS86

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74 HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54 HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, A or B to Y (Other Input Low)	t_{PLH}	$C_L = 50pF$	15	20	25	30	ns
	t_{PHL}		15	20	25	30	
Maximum Propagation Delay, A or B to Y (Other Input High)	t_{PLH}		18	25	31	37	ns
	t_{PHL}		18	25	31	37	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

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KS54HCTLS 107A
KS74HCTLS

Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current Outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

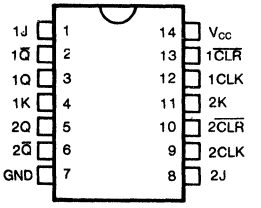
DESCRIPTION

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the $\overline{CLR}$ input resets the outputs regardless of the levels of the other inputs. When $\overline{CLR}$ is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

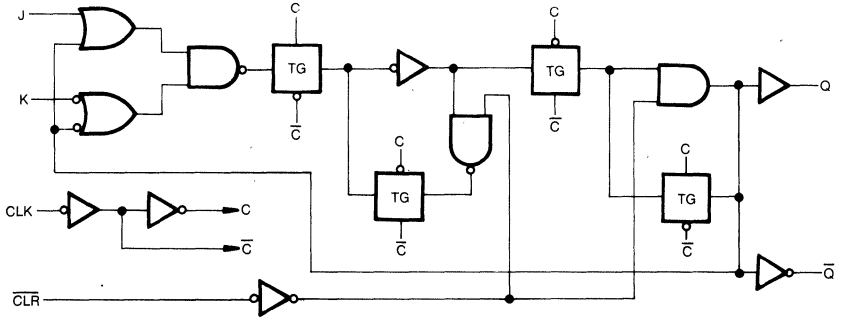
PIN CONFIGURATION



FUNCTION TABLE

Inputs				Outputs	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS107A

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30		25	21	MHz
Maximum Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		15	20		25	30	ns
		t_{PHL}		15	20		25	30	
Maximum Propagation Delay, $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		15	20		25	30	ns
		t_{PHL}		15	20		25	30	
Minimum Setup Time before CLK↓	J or K	t_{su}		10	13		17	20	ns
	$\overline{CLR}$ Inactive			10	13		17	20	
Minimum Hold Time, J or K after CLK↓		t_h		−3	0		0	0	ns
Minimum Pulse Width	CLK High or Low	t_w		10	13		17	20	ns
	$\overline{CLR}$ Low			10	13		17	20	
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per flip-flop)	40					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current Outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

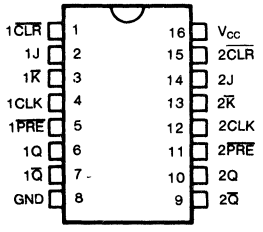
DESCRIPTION

These devices contain two positive-edge-triggered J-$\overline{K}$ flip-flops with independent preset and clear inputs and complementary Q and $\overline{Q}$ outputs. The present and clear inputs are active-low and operate independently of the clock Data at the J and $\overline{K}$ inputs are transferred to the ouptuts on the positive transition of the clock provided setup requirements have been met. These versatile flip-flops can perform as toggel flip-flops by grounding $\overline{K}$ and tying J high. They can also perform as D-type flops if J and $\overline{K}$ are tied together.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

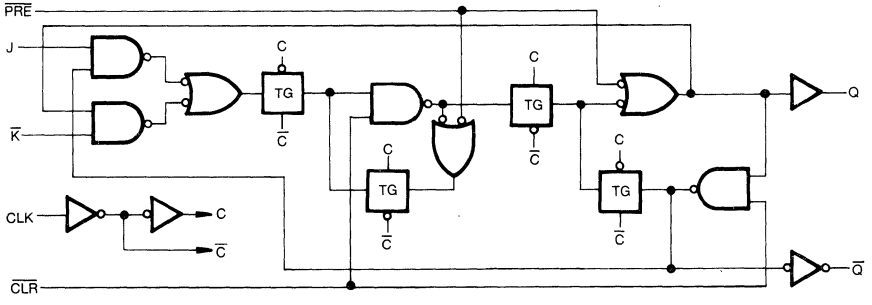


FUNCTION TABLE

Inputs					Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

*Both outputs will remain high as long as $\overline{PRE}$ and $\overline{CLR}$ are low, but the output states are unpredictable if $\overline{PRE}$ and $\overline{CLR}$ go high simultaneously.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS109A

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30		25	20	MHz
Maximum Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		18	25		31	37	ns
		t_{PHL}		30	40		50	60	
Maximum Propagation Delay, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		18	25		31	37	ns
		t_{PHL}		30	40		50	60	
Minimum Setup Time before CLK↑	Data	t_{su}		10	13		17	20	ns
	$\overline{PRE}$ or $\overline{CLR}$ Inactive			10	13		17	20	
Minimum Hold Time, Data after CLK↓		t_h		−3	0		0	0	ns
Minimum Pulse Width	CLK High or Low	t_w		8	15		20	25	ns
	$\overline{PRE}$ or $\overline{CLR}$ Low			8	15		20	25	
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}	(per flip-flop)	40					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

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KS54HCTLS / KS74HCTLS 112A

Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current Outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

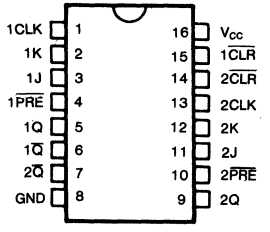
DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

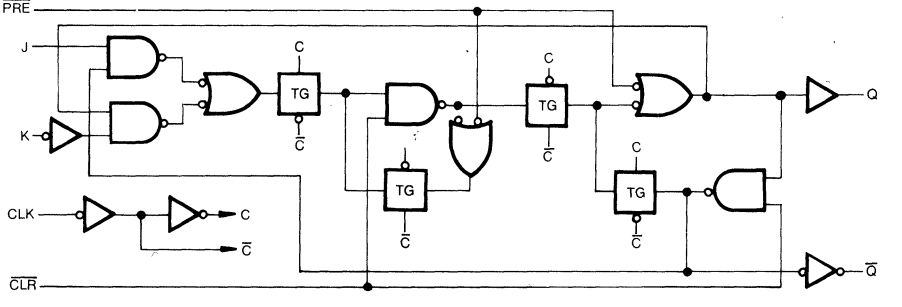


FUNCTION TABLE

Inputs					Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*Both outputs will remain high as long as $\overline{PRE}$ and $\overline{CLR}$ are low, but the output states are unpredictable if $\overline{PRE}$ and $\overline{CLR}$ go high simultaneously.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS112A

Characteristic		Symbol	Conditions†	$T_a=25°C$ $V_{CC}=5.0V$	KS74HCTLS $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54HCTLS $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}	$C_L=50pF$	40	30	25	21	MHz
Maximum Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		15	20	25	30	ns
		t_{PHL}		15	20	25	30	
Maximum Propagation Delay, $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		15	20	25	30	ns
		t_{PHL}		15	20	25	30	
Minimum Setup Time before CLK↓	J or K	t_{su}		10	13	17	20	ns
	$\overline{CLR}$ Inactive			10	13	17	20	
Minimum Hold Time, Data after CLK↓		t_h		−3	0	0	0	ns
Minimum Pulse Width	CLK High or Low	t_w		10	13	17	20	ns
	$\overline{PRE}$ or $\overline{CLR}$ Low			10	13	17	20	
Maximum Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}	(per flip-flop)	40				pF

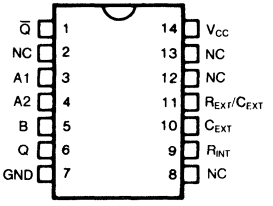
* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

FEATURES

- **Schmitt-trigger for slow Input transitions**
- **Internal timing resistor**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range; 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Outputs	
A1	A2	B	Q	Q̄
L	X	X	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

H= HIGH Voltage level
L= LOW voltage level
X= Don't care
↑= LOW-to-HIGH transition
↓= HIGH-to-LOW transition
⎍= one HIGH level output pulse
⎎= one LOW level output pulse

DESCRIPTION

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{INT} connected to V_{CC}, C_{EXT} and C_{EXT}/C_{EXT} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10μF) and more than one decade of timing resistance (2 kΩ to 40 kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_{EXT}R_{EXT}\ \ln 2 = 0.7\ C_{EXT}\ R_{EXT}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_{EXT}. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts any yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external compoennts.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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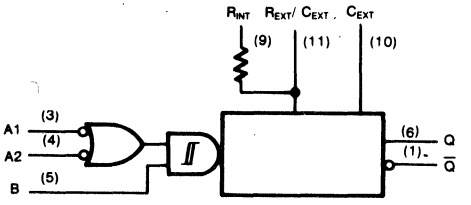
LOGIC DIAGRAM



Notes: 1. An external capacitor may be connected between C_{EXT} (positive) and R_{EXT}/C_{EXT}.
2. To use the internal timing resistor, connect R_{INT} to V_{CC}. For Improved pulse width accuracy and repeatability connect on external resistor between R_{EXT}/C_{EXT} V_{CC} with R_{INT} open-circuited.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I<−0.5V or V_I>V_{CC}+0.5V) ..... ±20 mA
DC Output Diode Current, I_{Ok}
(V_O<−0.5V or V_O>V_{CC}+0.5V) ..... ±20 mA
Continuous OUtput Current Per Pin, I_O
(−0.5V<V_O<V_{CC}+0.5V) ..... ±35 mA
Continuous Current Through
V_{CC} or GND pins ..... ±125 mA
Storage Temperature Range, T_{stg} −65°C to +150°C
Power Dissipation Per Package, P_d† ..... 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package(N): −12mW/°C from 65°C to 85°C
Ceramic Package(J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} ..... 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f ..... Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS121

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
		$C_L = 50pF$	Min	Max	Min	Max	Min	Max	
Propagation Delay	t_{PLH}	$C_L = 50pF$		70		87		105	ns
A, B to Q, $\overline{Q}$	t_{PHL}	$C_{ext} = 80pF$		70		87		105	
Propagation Delay	t_{PLH}	R_{int} to V_{CC}		55		68		82	ns
B to Q & $\overline{Q}$ output	t_{PHL}			55		68		82	
Minimum Output pulse width	t_w	$C_{ext} = 0pF$ R_{int} to V_{CC}	20	50		52		52	ns
Output pulse width	t_w	$C_{ext} = 80pF$ R_{int} to V_{CC}	70	150		156		156	ns
		$C_{ext} = 100pF$ $R_{ext} = 10k\Omega$	630	770	602	798	595	805	ns
		$C_{ext} = 1\mu F$ $R_{ext} = 10k\Omega$	6.3	7.7	6.0	8	5.9	8.1	ns
Minimum input pulse width to trigger	t_w		50		63		75		ns
External timing tesistor range	R_{ext}		1.4	40	1.4	40	1.4	40	kΩ
External timing capacitance range	C_{ext}		0	1,000	0	1,000	0	1,000	μF
Output Duty cycle		$R_{ext} = 2k\Omega$		67		67		67	%
		$R_{ext} = R_{ext(max)}$		90		90		90	%
Input Capacitance	C_{in}								pF
Power dissipation Capacitance	C_{PD}								

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

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KS54HCTLS 123
KS74HCTLS 123

Dual Retriggerable Monostable Multivibrator with Clear

Preliminary Specifications

FEATURES

- **Simple pulse width formula $t_W = 0.45RC$**
- **DC triggered from active HIGH or active Low inputs**
- **Retriggerable for very long output pulses up to 100% duty cycle**
- **Overriding clear terminates output pulse**
- **Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs**
- **Functions, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High drive current outputs: $I_{OL} = 8mA$ @ $V_{OL} = 0.5V$**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range; 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74HCTLS: −40°C to +85°C KS54HCTLS: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '123 contains dual retriggerable monostable multivibrators with output pulse width control by three methods.

The basic pulse time is programmed by selection of an external resistor (Rext) and capacitor (Cext). The external resistor and capacitor are normally connected as shown timing component.

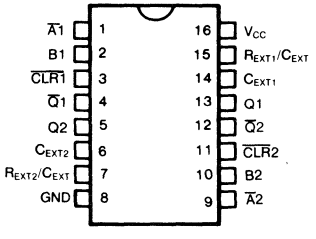
Once triggered, the basic output pulse width may be extended by retriggering the gated active Low going edge input (Ai) or the active HIGH going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH, $n\overline{Q}$=LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a Low-going edge on input CLR, which also inhibits the triggering.

An internal connection from CLR to the input gates makes it possible to trigger the circuit by a positive-going signal at input CLR as shown in the function table when $C_{EXT} > 10nF$, the typical output pulse width is defined as; $t_W = 0.45 \times R_{EXT} \times C_{EXT}$(typ).

Where t_w is in seconds. R is in ohm. and C is in fards.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Outputs	
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H= HIGH voltage level
L= LOW voltage level
X= don't care
↑= LOW to HIGH transition
↓= HIGH to LOW transition
⎍= one HIGH level output pulse
⎎= one LOW level output pulse

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I<−0.5V or V_I>V_{CC}+0.5V) ..... ±20 mA
DC Output Diode Current, I_{Ok}
(V_O<−0.5V or V_O>V_{CC}+0.5V) ..... ±20 mA
Continuous OUtput Current Per Pin, I_O
(−0.5V<V_O<V_{CC}+0.5V) ..... ±35 mA
Continuous Current Through
V_{CC} or GND pins ..... ±125 mA
Storage Temperature Range, T_{stg} −65°C to +150°C
Power Dissipation Per Package, P_d† ..... 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package(N): −12mW/°C from 65°C to 85°C
Ceramic Package(J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} ..... 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f ..... Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS123

Characteristic	Symbol	Conditions†	$T_a=25°C$ $V_{CC}=5.0V$	KS74HCTLS $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54HCTLS $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits				
Propagation Delay	t_{PLH}	$C_L=50pF$ $C_{ext}=0$, $R_{ext}=5k\Omega$	23	33		41	50	ns
$\overline{A}$, B to Q, $\overline{Q}$	t_{PHL}		23	33		41	50	
Propagation Delay	t_{PLH}		20	27		34	41	ns
$\overline{CLR}$ to Q, $\overline{Q}$	t_{PHL}		20	27		34	41	
Output Pulse Width 1	t_{WQ1}		116	200		207	209	ns
Output Pulse Width 2	t_{WQ2}	$C_L=50pF$ $C_{ext}=1000pF$ $R_{ext}=10k\Omega$	4.5	4.0 5.0		3.8(min) 5.2(max)	3.8 (min) 5.2(max)	μs
Trigger Pulse Width	t_w	$C_L=50pF$ A_i=LOW	7	20		25	30	ns
Trigger Pulse Width	t_w	$C_L=50pF$ B_i=High	7	20		25	30	ns
Clear Pulse Width	t_w	$C_L=50pF$ CLR_i=LOW	8	20		25	30	ns
External Timing Resistance	R_{ext}			2 1000		2(min) 1000(max)	2(min) 1000(max)	kΩ
External Timing Capacitance	C_{in}		no restriction					
Input Capacitance	C_{in}		5					pF
Power Dissipation Capacitance	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Application Information

The basic output pulse width is determined by the value of external capacitance and timing resistance.
For output pulse widths greater than 100μs or external capacitance greater than 1000pF the following equation should be used.

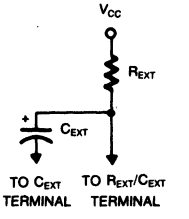
$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

t_w is in second
K is the multiplying factor
and is approximately 0.45 for
$C_{ext} \geq 1000pF$
C_{ext} is in F

For best results, system ground should be applied to the C_{ext} terminal. These devices do not require a switching diode in series with the R_{ext}/C_{ext} terminal (as required by some other monostable multivibrators)

TIMING COMPONENT



FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

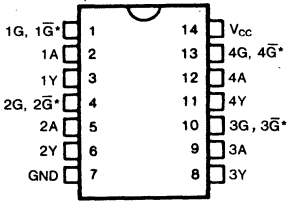
DESCRIPTION

These bus buffers feature four independent line drivers with 3-state outputs. The output enable functions for the '125 buffers are active-low, while those for '126 are active high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

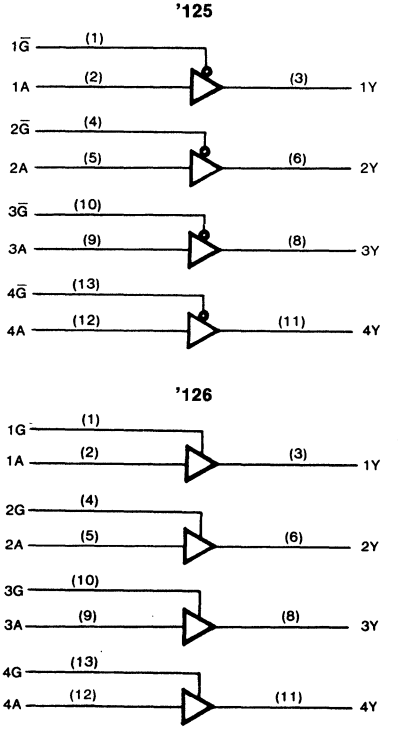
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



* $\overline{G}$ for '125; G for '126

LOGIC DIAGRAMS



FUNCTION TABLES

'125

Inputs		Output
A	$\overline{G}$	Y
H	L	H
L	L	L
X	H	Z

'126

Inputs		Output
A	G	Y
H	H	H
L	H	L
X	L	Z

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS125, HCTLS126

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Propagation Delay, A to Y	t_{PLH}	$C_L = 50pF$		13	18	22	27	ns
		$C_L = 150pF$		16	21	27	33	
	t_{PHL}	$C_L = 50pF$		13	18	22	27	
		$C_L = 150pF$		16	21	27	33	
Maximum Output Enable Time, Enable to Y	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	17	23	29	34	ns
			$C_L = 150pF$	20	26	34	40	
	t_{PZL}		$C_L = 50pF$	17	23	29	34	
			$C_L = 150pF$	20	26	34	40	
Maximum Output Disable Time, Enable to Y	t_{PHZ}	$R_L = 1k\Omega$		16		26	32	ns
	t_{PLZ}	$C_L = 50pF$		16		26	32	
Maximum Input Capacitance	C_{IN}			5				pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10				pF
Power Dissipation Capacitance* (per stage)	C_{PD}*	Output Disabled		5				pF
		Output Enabled		30				

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

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Preliminary Specifications

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

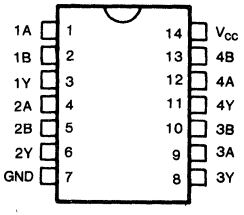
These Schmitt-trigger devices contain four independent NAND gates. They perform the Boolean function $Y=\overline{A \bullet B}=\overline{A}+\overline{B}$ in positive logic.

The input threshold levels are temperature compensated and can be triggered from the slowest of input ranges and still give jitter-free output signals.

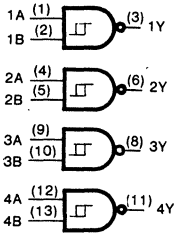
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.11 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	T_a=25°C		KS74HCTLS T_a=−40°C to +85°C		KS54HCTLS T_a=−55°C to +125°C		Unit
			Min	Max	Min	Max	Min	Max	
Positive-Going Threshold Voltage	V_{T+}	V_{CC}=4.5V	1.2	1.9	1.2	1.9	1.2	1.9	V
		V_{CC}=5.5V	1.4	2.1	1.4	2.1	1.4	2.1	
Negative-Going Threshold Voltage	V_{T-}	V_{CC}=4.5V	0.5	1.2	0.5	1.2	0.5	1.2	V
		V_{CC}=5.5V	0.6	1.4	0.6	1.4	0.6	1.4	
Hysteresis (V_{T+}-V_{T-})	V_H	V_{CC}=4.5V	0.4	1.4	0.4	1.4	0.4	1.4	V
		V_{CC}=5.5V	0.4	1.5	0.4	1.5	0.4	1.5	

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS132

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74 HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54 HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay Any Input to Y	t_{PLH}	$C_L = 50pF$	17	22	28	33	ns
	t_{PHL}		17	22	28	33	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '133 contains a single 13-input NAND gate.
It performs the Boolean functions (in positive logic):

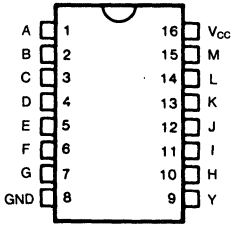
$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$

$Y = \bar{A}+\bar{B}+\bar{C}+\bar{D}+\bar{E}+\bar{F}+\bar{G}+\bar{H}+\bar{I}+\bar{J}+\bar{K}+\bar{L}+\bar{M}$

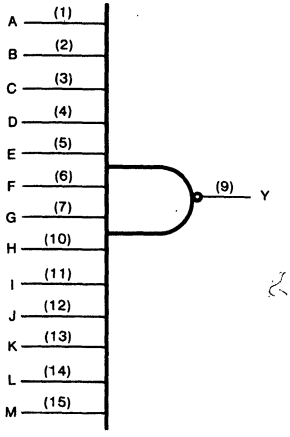
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS A THRU M	OUTPUT Y
All inputs H	L
One or more inputs L	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS133

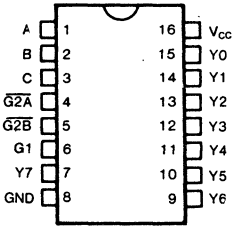
Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay Any Input to Y	t_{PLH}	C_L=50pF	18	24	30	36	ns
	t_{PHL}		18	25	30	36	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Designed specifically for high-speed memory decoders and data transmission systems**
- **Incorporates 3 enable inputs to simplify cascading and/or data reception**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



FUNCTION TABLE

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

DESCRIPTION

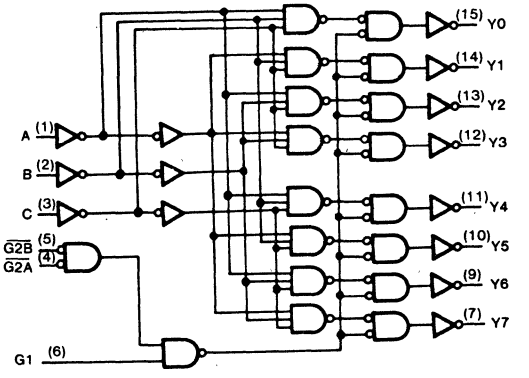
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS138

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74 HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, A or B to Y	t_{PLH}	$C_L = 50pF$	22	30	37	45	ns
	t_{PHL}		22	30	37	45	
Maximum Propagation Delay, G1 to any Y	t_{PLH}		24	32	40	48	ns
	t_{PHL}		24	32	40	48	
Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to any Y	t_{PLH}		18	25	31	37	ns
	t_{PHL}		18	25	31	37	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	')	50				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

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FEATURES

- **Designed specifically for high-speed memory decoders and data transmission systems**
- **Incorporates 2 enable inputs to simplify cascading and/or data reception**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

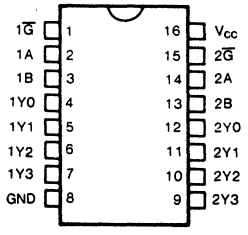
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiriring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The '139 consists of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

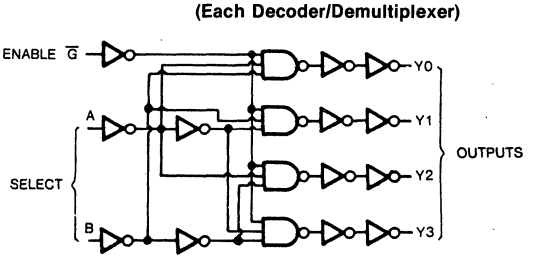
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Outputs			
Enable $\overline{G}$	Select B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS139

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, A or B to Y	t_{PLH}	$C_L = 50pF$	22	30	37	45	ns
	t_{PHL}		22	30	37	45	
Maximum Propagation Delay, $\overline{G}$ to any Y	t_{PLH}		21	28	35	42	ns
	t_{PHL}		21	28	35	42	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}		50				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

FEATURES

- **Encodes eight data lines in priority**
- **Provides 3-bit binary priority code**
- **Input enable capability**
- **Easily cascadable**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

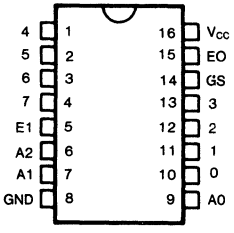
DESCRIPTION

The '148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

Inputs									Outputs				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

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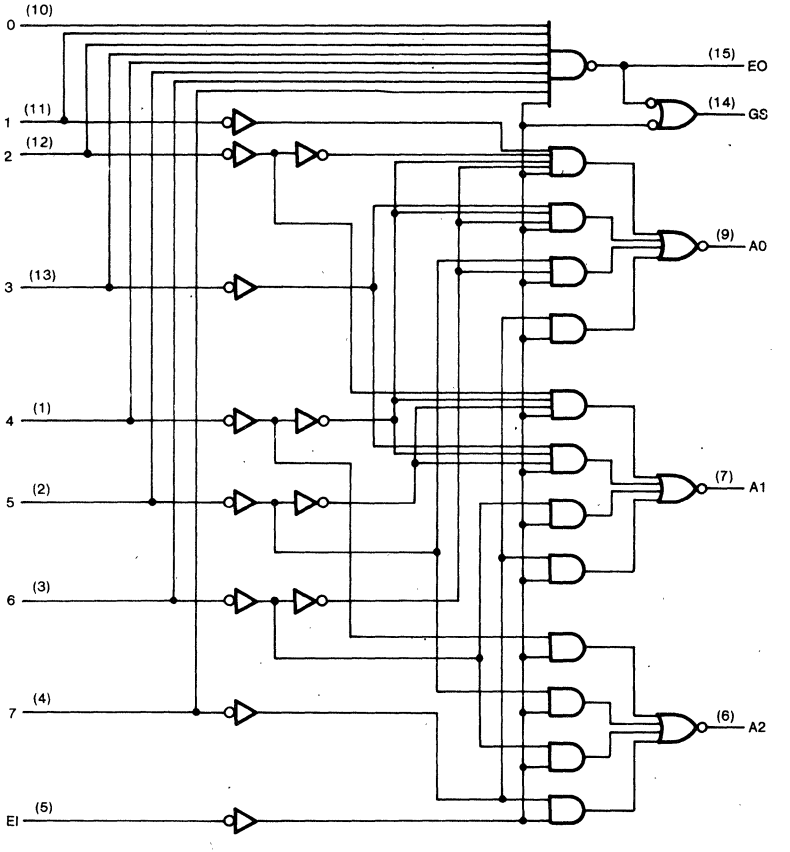
LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS148

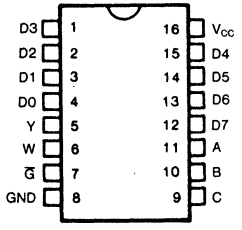
Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%		Unit
			Typ	Guaranteed Limits				
Maximum Propagation Delay, 1-7 to A0, A1 or A2	t_{PLH}	C_L=50pF	20	27	34	41		ns
	t_{PHL}		20	27	34	41		
Maximum Propagation Delay, 0-7 to EO	t_{PLH}		22	29	36	44		ns
	t_{PHL}		22	29	36	44		
Maximum Propagation Delay, 0-7 to GS	t_{PLH}		28	38	47	57		ns
	t_{PHL}		28	38	47	57		
Maximum Propagation Delay, EI to A0, A1 or A2	t_{PLH}		19	25	31	38		ns
	t_{PHL}		19	25	31	38		
Maximum Propagation Delay, EI to GS	t_{PLH}		20	26	33	39		ns
	t_{PHL}		20	26	33	39		
Maximum Propagation Delay, EI to EO	t_{PLH}		21	28	35	42		ns
	t_{PHL}		21	28	35	42		
Maximum Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	50					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Can perform as:**
  - **Boolean Function Generators**
  - **Parallel-to-Serial Converters**
  - **Data Source Selectors**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ($\overline{G}$) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
D0, D1 ... D7 = the level of the D respective input

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

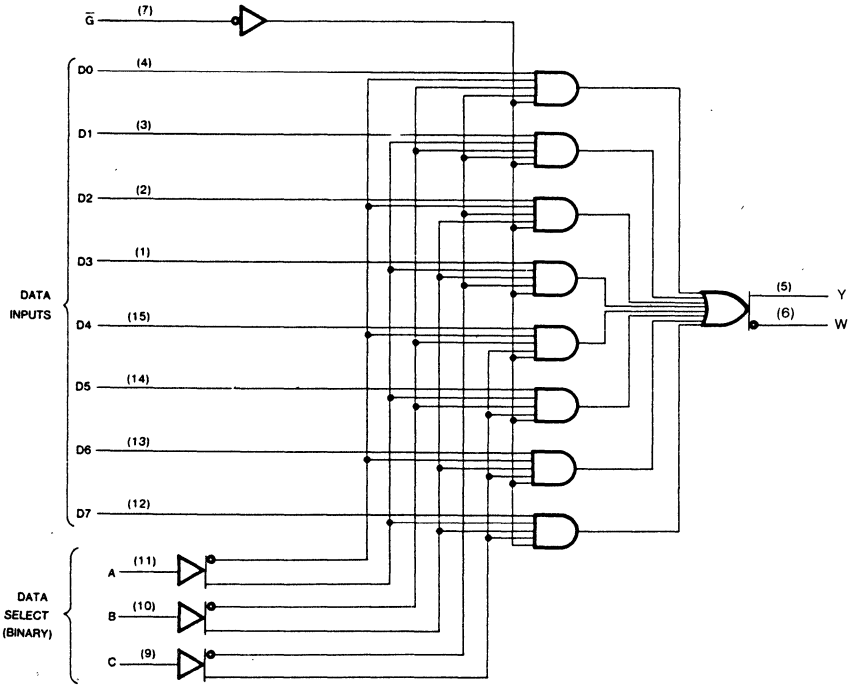
† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS151

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, A, B or C to Y	t_{PLH}	$C_L = 50pF$	24	32	40	48	ns
		$C_L = 150pF$	27	35	45	54	
	t_{PHL}	$C_L = 50pF$	24	32	40	48	
		$C_L = 150pF$	27	35	45	54	
Maximum Propagation Delay, A, B or C to W	t_{PLH}	$C_L = 50pF$	27	36	45	54	ns
		$C_L = 150pF$	30	39	50	60	
	t_{PHL}	$C_L = 50pF$	27	36	45	54	
		$C_L = 150pF$	30	39	50	60	
Maximum Propagation Delay, Any D to Y	t_{PLH}	$C_L = 50pF$	20	26	33	39	ns
		$C_L = 150pF$	23	29	38	45	
	t_{PHL}	$C_L = 50pF$	20	26	33	39	
		$C_L = 150pF$	23	29	38	45	
Maximum Propagation Delay, Any D to W	t_{PLH}	$C_L = 50pF$	16	21	26	32	ns
		$C_L = 150pF$	19	24	31	38	
	t_{PHL}	$C_L = 50pF$	16	21	26	32	
		$C_L = 150pF$	19	24	31	38	
Maximum Propagation Delay, $\overline{G}$ to Y	t_{PLH}	$C_L = 50pF$	20	26	33	39	ns
		$C_L = 150pF$	23	29	38	45	
	t_{PHL}	$C_L = 50pF$	20	26	33	39	
		$C_L = 150pF$	23	29	38	45	
Maximum Propagation Delay, $\overline{G}$ to W	t_{PLH}	$C_L = 50pF$	20	26	33	39	ns
		$C_L = 150pF$	23	29	38	45	
	t_{PHL}	$C_L = 50pF$	20	26	33	39	
		$C_L = 150pF$	23	29	38	45	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Allows Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N lines to n lines)**
- **'253 is the 3-State Version of this port**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74HCTLS: −40°C to +85°C KS54HCTLS: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

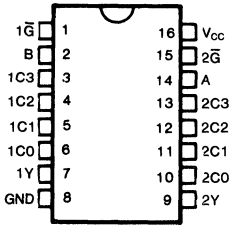
DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

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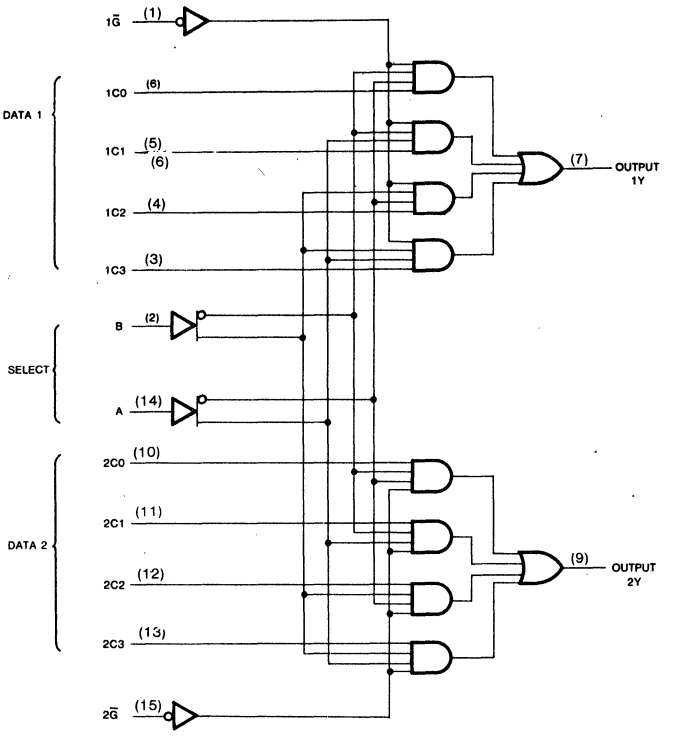
LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS153

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ		Guaranteed Limits		
Maximum Propagation Delay, A or B to Y	t_{PLH}	C_L=50pF C_L=150pF	23 26	30 33	38 43	45 51	ns
	t_{PHL}	C_L=50pF C_L=150pF	23 26	30 33	38 43	45 51	ns
Maximum Propagation Delay, Data (Any C) to Y	t_{PLH}	C_L=50pF C_L=150pF	15 18	20 23	25 30	30 36	ns
	t_{PHL}	C_L=50pF C_L=150pF	15 18	20 23	25 30	30 36	ns
Maximum Propagation Delay, $\overline{G}$ to Y	t_{PLH}	C_L=50pF C_L=150pF	21 24	28 31	35 40	42 48	ns
	t_{PHL}	C_L=50pF C_L=150pF	21 24	28 31	35 40	42 48	ns
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

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FEATURES

- **Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs**
- **Performs the Demultiplexing Function by Distributing Data From One Input to Any One of 16 Outputs**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

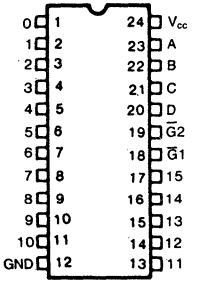
DESCRIPTION

These monolithic, 4-line to 16-line decoders decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs. $\overline{G}1$ and $\overline{G}2$, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders.

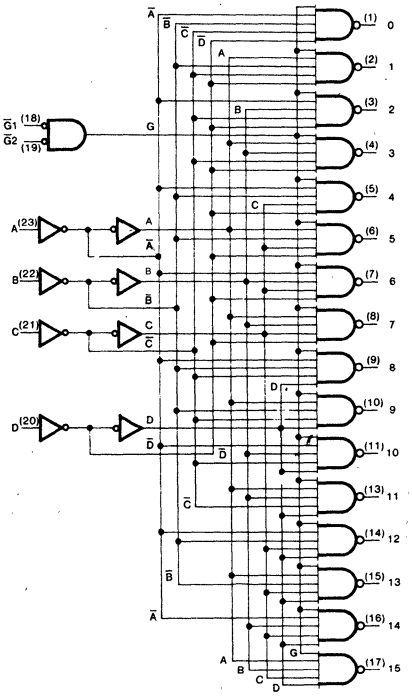
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inputs						Outputs													
$\bar{G}1$	$\bar{G}2$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

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Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS154

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74 HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, A, B, C or D to Any Output	t_{PLH}	C_L=50pF	21	28	35	42	ns
	t_{PHL}		21	28	35	42	
Maximum Propagation Delay, G1 or G2 to Any Output	t_{PLH}		21	28	35	42	ns
	t_{PHL}		21	28	35	42	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Typical applications:**
  Dual 2-to-4 line decoder
  Dual 1-to-4 line demultiplexer
  3-to-8 line decoder
  1-to-8 line demultiplexer
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

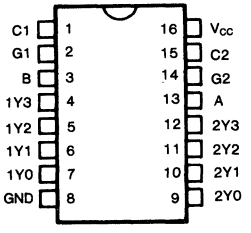
DESCRIPTION

The '155 consists of two 1-to-4 line demultiplexers with independent strobes and common binary address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each secton. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8 line decoder, or 1-to-8 line demultiplexer, without gating.

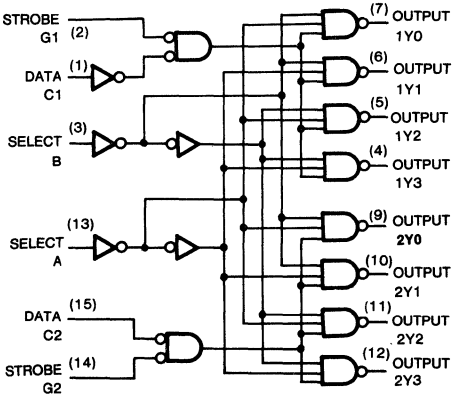
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



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FUNCTION TABLES

2-to-4 Line Decoder or 1-to-4 Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-to-8 Line Decoder or 1-to-8 Line Demultiplexer

Inputs		Outputs							
Select	Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
IC B A	IG	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X X X	H	H	H	H	H	H	H	H	H
L L L	L	L	H	H	H	H	H	H	H
L L H	L	H	L	H	H	H	H	H	H
L H L	L	H	H	L	H	H	H	H	H
L H H	L	H	H	H	L	H	H	H	H
H L L	L	H	H	H	H	L	H	H	H
H L H	L	H	H	H	H	H	L	H	H
H H L	L	H	H	H	H	H	H	L	H
H H H	L	H	H	H	H	H	H	H	L

IC = Inputs C1 and C2 connected together
IG = Inputs G1 and G2 connected together

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS155

Characteristic	Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V	KS74 HCTLS T_a = −40°C to +85°C V_{CC} = 5.0V ± 10%		KS54 HCTLS T_a = −55°C to +125°C V_{CC} = 5.0V ± 10%		Unit
			Typ	Guaranteed Limits				
Maximum Propagation Delay, A, B, C2, G1 or G2 to any Output (2 levels of logic)	t_{PLH}	C_L=50pF	17	23	29	35		ns
	t_{PHL}		17	23	29	35		
Maximum Propagation Delay, A or B to any Y (3 levels of logic)	t_{PLH}		21	28	35	42		ns
	t_{PHL}		21	28	35	42		
Maximum Propagation Delay, C1 to any Y	t_{PHL}		20	27	34	41		ns
	t_{PHL}		20	27	34	41		
Maximum Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

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FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

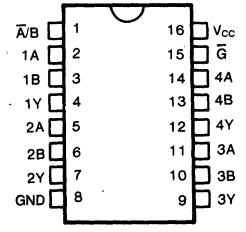
DESCRIPTION

These are data selectors/multiplexers which select a 4-bit word from one of two sources via the control of a common select input ($\overline{A}$/B). A separate strobe input ($\overline{G}$) is provided. The '157 presents true data whereas the '158 presents inverted data at the outputs.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

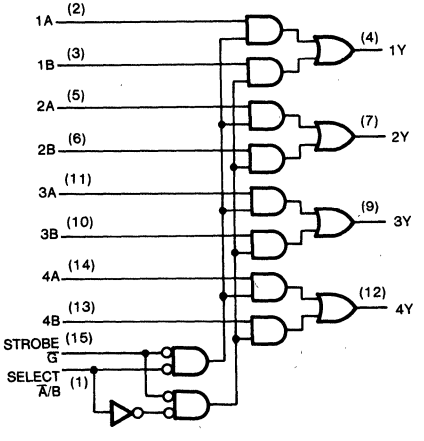


FUNCTION TABLE

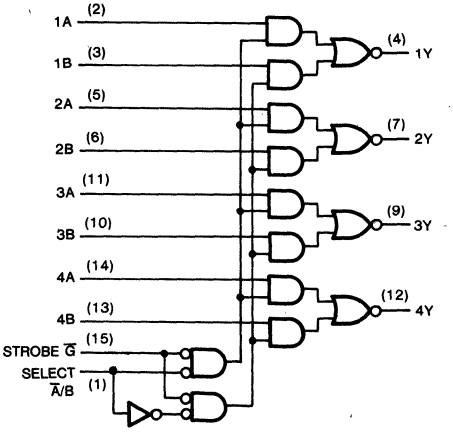
Inputs				Output Y	
Strobe	Select	Data		'157	'158
$\overline{G}$	$\overline{A}$/B	A	B		
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

LOGIC DIAGRAMS

'157



'158



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS157, HCTLS158

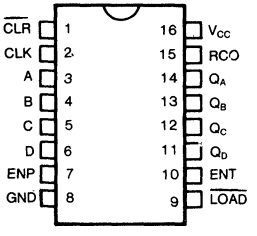
Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54 HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, A or B to Y	t_{PLH}		11	15	19	22	ns
	t_{PHL}		11	15	19	22	
Maximum Propagation Delay, $\overline{A}$/B to Y	t_{PLH}		17	23	29	34	ns
	t_{PHL}		17	23	29	34	
Maximum Propagation Delay, $\overline{G}$ to Y	t_{PLH}		15	20	25	30	ns
	t_{PHL}		15	20	25	30	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Internal Look Ahead for Fast Counting**
- **Carry Output for n-bit cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline"** packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



FUNCTION TABLES

'160, '161

CLK	$\overline{CLR}$	ENP	ENT	$\overline{LOAD}$	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

'162, '163

CLK	$\overline{CLR}$	ENP	ENT	$\overline{LOAD}$	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

DESCRIPTION

These are synchronous, presettable 4-bit binary counters featuring internal carry-look-ahead for high-speed counting. The '160 and '162 are decade counters, and the '161 and '163 are 4-bit binary counters. The buffered clock input triggers all flip-flops simultaneously on the rising edge of the input waveform. This eliminates the output counting spikes normally associated with asynchronous counters.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs.

The clear function for the '162 and 163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter.

Two enable inputs and a ripple carry output allow easy cascading of the counters. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

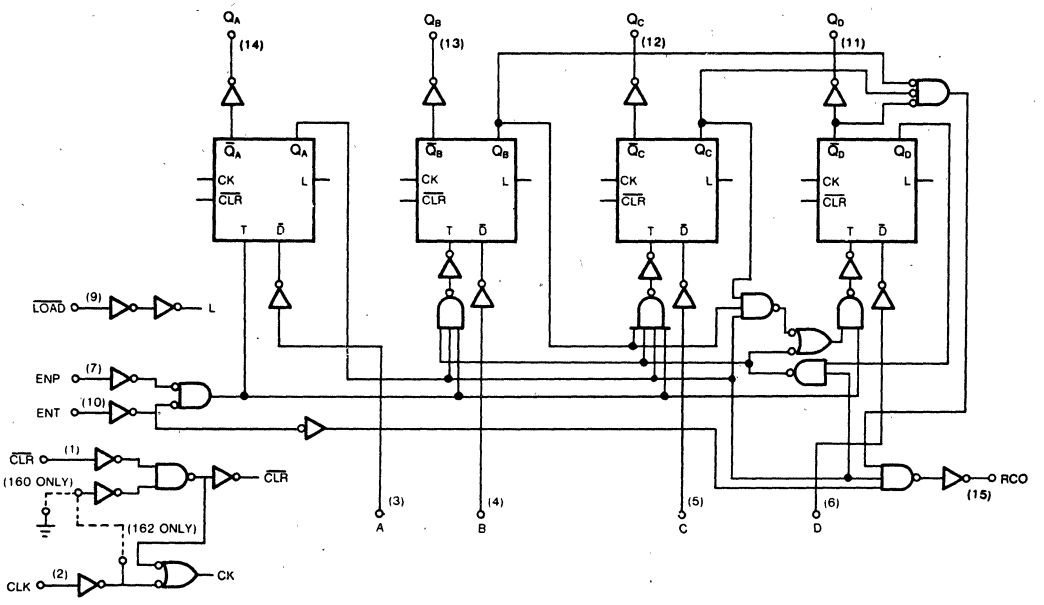
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that will modify the operating model have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

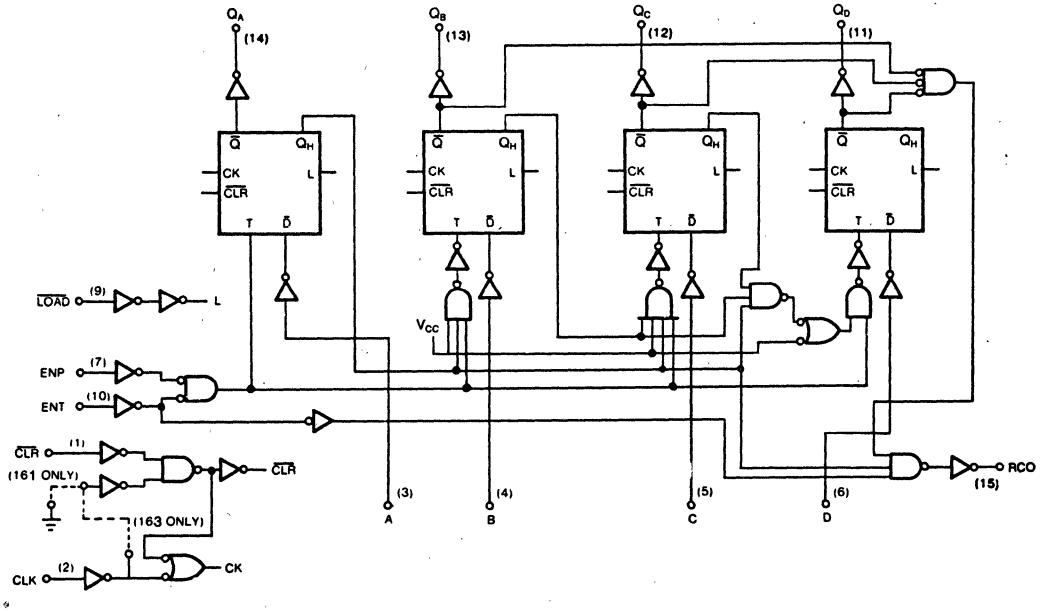
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAMS

'160A or '162A

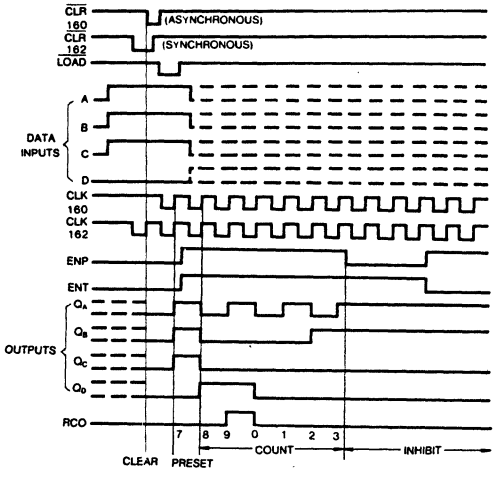


'161A or '163A



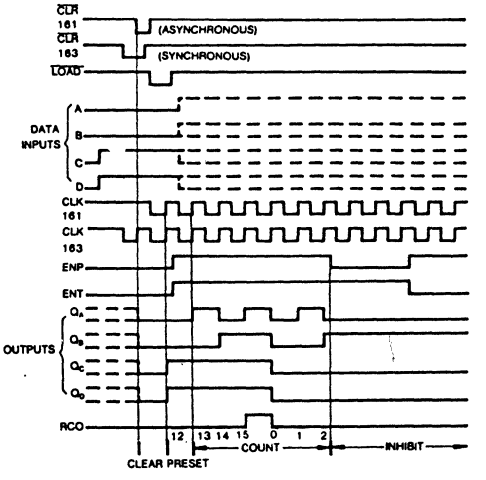
Typical Clear, Preset, Count and Inhibit Sequences

'160A or '162A



Sequence:
(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

'161A or '163A



Sequence:
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one and two
(4) Inhibit

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Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS160A, HCTLS161A

Characteristic		Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
				Typ	Guaranteed Limits		
Maximum Clock Frequency		f_{max}	C_L=50pF	40	30	25	20	MHz
Maximum Propagation Delay, CLK to RCO		t_{PLH}		26	35	44	53	ns
		t_{PHL}		26	35	44	53	
Maximum Propagation Delay, CLK to any Q		t_{PLH}		20	26	33	39	ns
		t_{PHL}		20	26	33	39	
Maximum Propagation Delay, ENT to RCO		t_{PLH}		11	14	18	21	ns
		t_{PHL}		11	14	18	21	
Maximum Propagation Delay, $\overline{CLR}$ to any Q		t_{PHL}		21	28	35	42	ns
Maximum Propagation Delay, $\overline{CLR}$ to RCO		t_{PHL}		21	28	35	42	ns
Minimum Pulse Width	CLK High or Low	t_w		10	13	17	20	ns
	$\overline{CLR}$ Low			10	13	17	20	
Minimum Setup Time before CLK↑	A, B, C, D	t_{su}		10	13	17	20	ns
	$\overline{LOAD}$			10	13	17	20	
	ENP, ENT			10	13	17	20	
	$\overline{CLR}$ inactive			10	13	17	20	
Minimum Hold Time, All Synchronous Inputs after CLK↑		t_h		0	0	0	0	ns
Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}		80				pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS162A, HCTLS163A

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30	25	20	MHz
Maximum Propagation Delay, CLK to RCO		t_{PLH}		26	35	44	53	ns
		t_{PHL}		26	35	44	53	
Maximum Propagation Delay, CLK to any Q		t_{PLH}		20	26	33	39	ns
		t_{PHL}		20	26	33	39	
Maximum Propagation Delay, ENT to RCO		t_{PLH}		11	14	18	21	ns
		t_{PHL}		11	14	18	21	
Maximum Propagation Delay, $\overline{CLR}$ to any Q		t_{PHL}		21	28	35	42	ns
Maximum Propagation Delay, $\overline{CLR}$ to RCO		t_{PHL}		21	28	35	42	ns
Minimum Pulse Width	CLK High or Low	t_w		10	13	17	20	ns
	$\overline{CLR}$ Low			10	13	17	20	
Minimum Setup Time before CLK↑	A, B, C, D	t_{su}		10	13	17	20	ns
	$\overline{LOAD}$			10	13	17	20	
	ENP, ENT			10	13	17	20	
	$\overline{CLR}$ inactive			10	13	17	20	
	$\overline{CLR}$ Low			10	13	17	20	
Minimum Hold Time, All Synchronous Inputs after CLK↑		t_h		−3	0	0	0	ns
Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}		80				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

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FEATURES

- **AND—Gated (enable/disable) serial inputs**
- **Fully buffered clock and serial inputs**
- **Direct clear**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

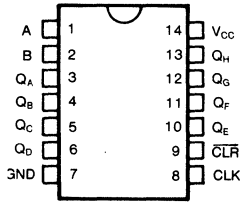
These are high-speed 8-bit registers with AND-gated serial inputs and an asynchronous clear. Data is entered serially through either one of the two inputs, A and B. A high on one input enables the other one, which will then determine the state of the first flip-flop. A low at either or both inputs inhibits data entry and resets the first flip-flop to a low level at the next positive clock transition.

Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of their clock input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

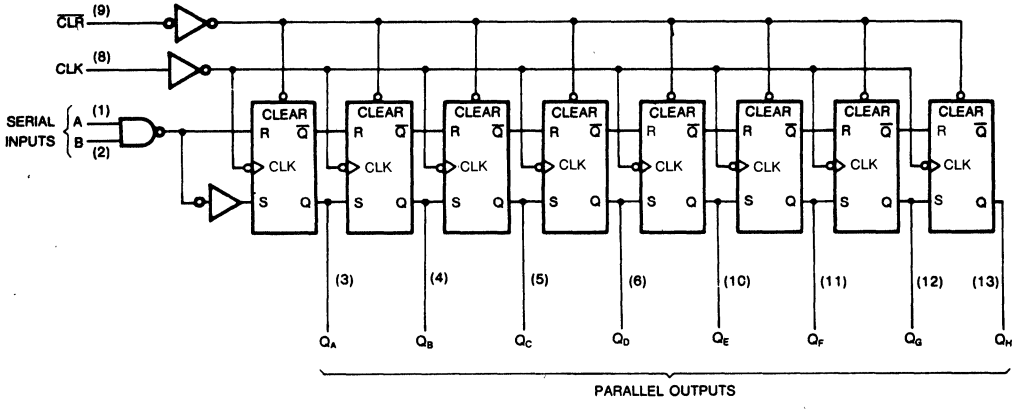


FUNCTION TABLE

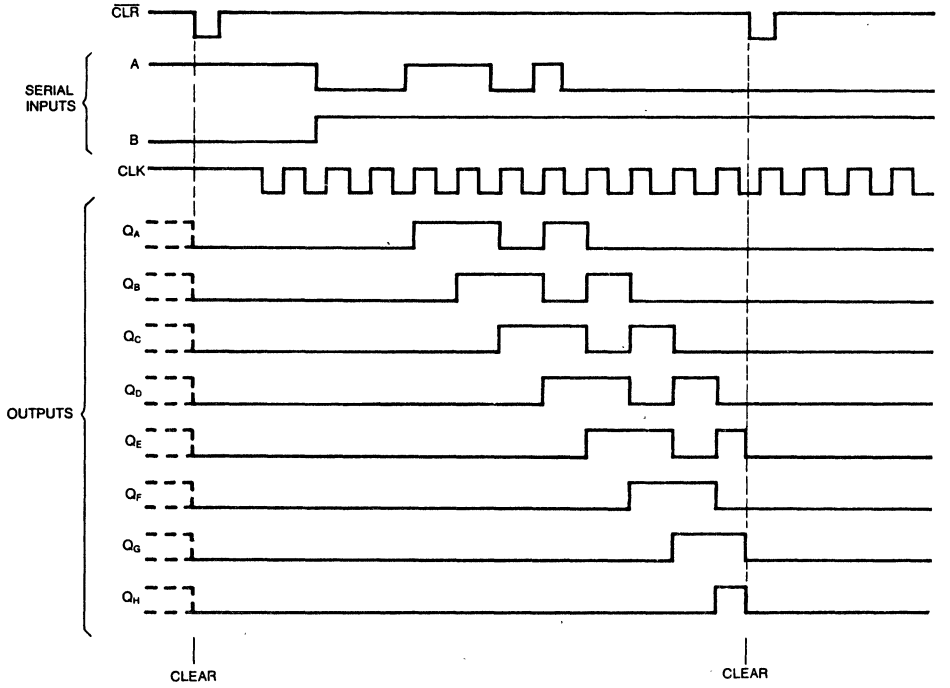
Inputs				Outputs		
$\overline{Clear}$	Clock	A	B	Q_A	Q_B . . . Q_H	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B or Q_H, respectively, before the indicate steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

LOGIC DIAGRAM



Typical Clear, Shift, and Clear Sequences



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS164

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30	25	20	MHz
Maximum Propagation Delay, $\overline{CLR}$ to any Q		t_{PLH}		27	36	45	54	ns
Maximum Propagation Delay, CLK to any Q		t_{PLH}		22	30	37	45	ns
		t_{PHL}		22	30	37	45	
Minimum Pulse Width	$\overline{CLR}$ Low	t_w		10	13	17	20	ns
	CLK High or Low			10	13	17	20	
Minimum Setup Time before CLK↑	Data	t_{su}		8	10	13	15	ns
	$\overline{CLR}$ Inactive			8	10	13	15	
Minimum Hold Time Data after CLK↑		t_h		0	5	5	5	ns
Maximum Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}	(per package)	120				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

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FEATURES

- **Complementary outputs**
- **Direct overriding load (data) inputs**
- **Gated clock inputs**
- **Parallel-to-Serial data conversion**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

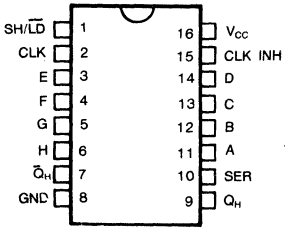
These are high-speed 8-bit parallel-load or serial-in shift registers with complementary serial outputs available from the last stage. Parallel-in access is asynchronous and is enabled by pulling the SH/$\overline{LD}$ input low. When SH/$\overline{LD}$ is high, data is entered serially at the SER input and shifted one place to the right with each positive clock transition.

Clocking is accomplished through a 2-input NOR gate which permits one of the clocks to be used as a clock inhibit function. Holding either clock input high inhibits clocking. Either clock input is enabled by holding the other clock input low while the SH/$\overline{LD}$ input is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

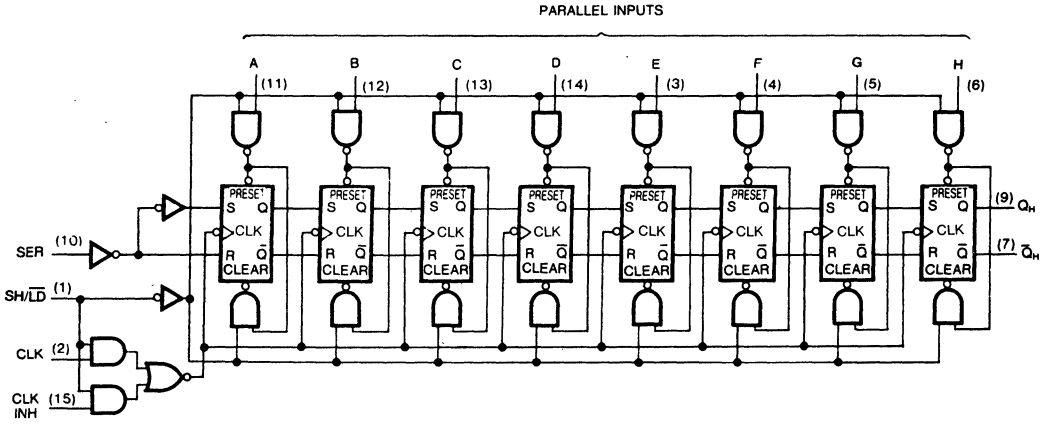


FUNCTION TABLE

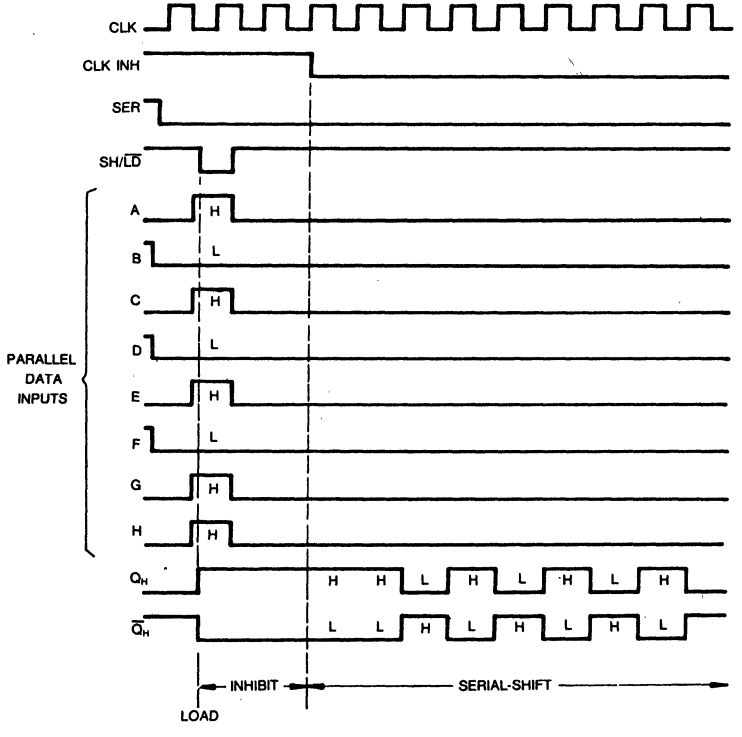
Inputs			Function
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	PARALLEL LOAD
H	H	X	NO CHANGE
H	X	H	NO CHANGE
H	L	↑	SHIFT*
H	↑	L	SHIFT*

*Content of each internal register shifts toward output Q_H. Data at serial input is shifted into first register.

LOGIC DIAGRAM



Typical Shift, Load and Inhibit Sequences



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Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS165

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30	25	20		MHz
Maximum Propagation Delay, SH/$\overline{LD}$ to Q_H or $\overline{Q}_H$		t_{PLH}		26	35	44	53		ns
		t_{PHL}		26	35	44	53		
Maximum Propagation Delay, CLK to Q_H or $\overline{Q}_H$		t_{PHL}		30	40	50	60		ns
		t_{PHL}		30	40	50	60		
Maximum Propagation Delay, H to Q_H or $\overline{Q}_H$		t_{PLH}		20	27	34	41		ns
		t_{PHL}		20	27	34	41		
Minimum Pulse Width	SH/$\overline{LD}$ Low	t_w		7	10	13	15		ns
	CLK High or Low			13	16	20	25		
Minimum Setup Time	SH/$\overline{LD}$ High before CLK↑	t_{su}		13	16	20	25		ns
	SER before CLK↑			10	13	17	20		
	CLK INH Low before CLK↑			13	16	20	25		
	CLK INH High before CLK↓			13	16	20	25		
	Data before SH/$\overline{LD}$↑			5	7	8	10		
Minimum Hold Time	SER Data after CLK↑	t_h		−3	0	0	0		ns
	PAR Data after SH/$\overline{LD}$↑			−3	0	0	0		
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		100					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

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8-Bit Parallel-In/Serial-Out Shift Registers with Clear

FEATURES

- **Synchronous load**
- **Direct overriding clear**
- **Parallel to serial conversion**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

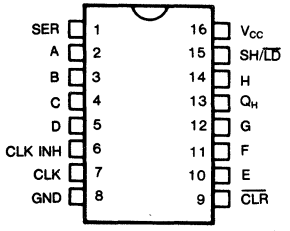
DESCRIPTION

These devices feature parallel-in or serial-in, serial-out registers, gated clock inputs and an overriding clear input. The paralled-in or serial-in modes are established by the shift/load input. When high, the input enables the serial data input and couples the eight fill-flops for serial shifting with each clock pulse. When low, the paralled data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

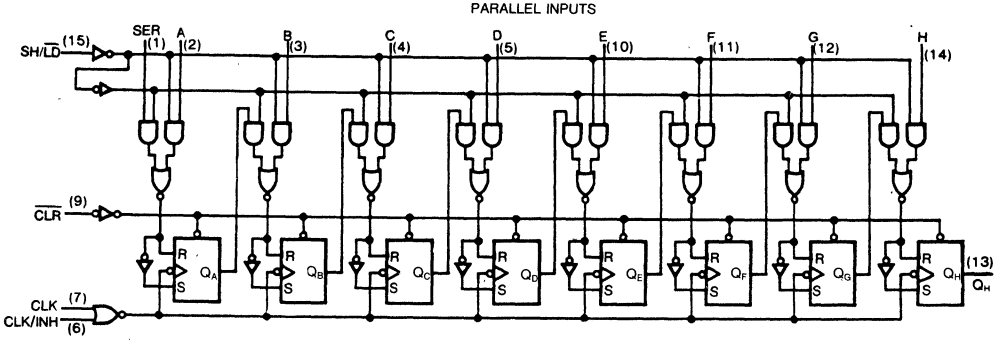
PIN CONFIGURATION



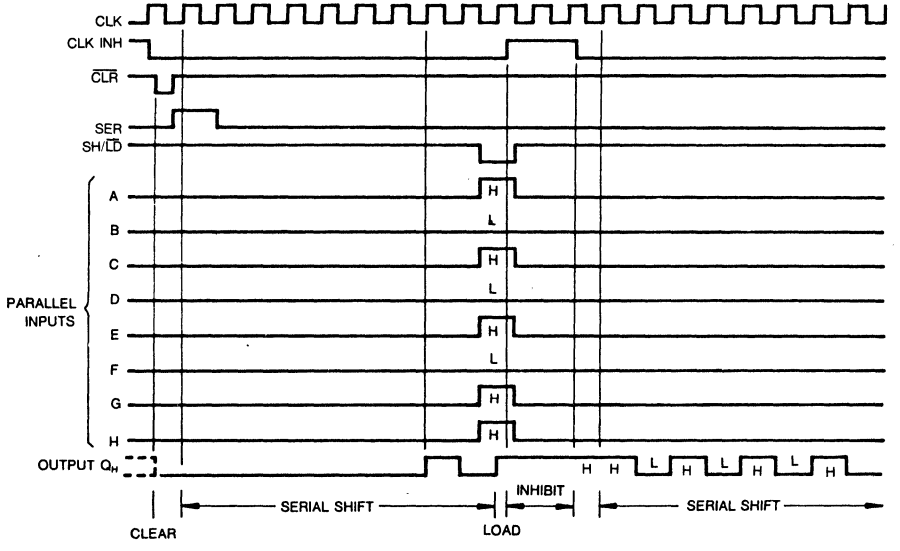
FUNCTION TABLE

Inputs						Internal Outputs		Output
$\overline{CLR}$	SH/$\overline{LD}$	CLK INH	CLK	SER	Parallel A ... H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a ... h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	G_{A0}	Q_{B0}	Q_{H0}

LOGIC DIAGRAM



Typical Clear, Shift, Load, Inhibit, and Shift Sequences



5

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS166

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30	25	20	MHz
Maximum Propagation Delay, $\overline{CLR}$ to Q_H		t_{PHL}		22	30	37	45	ns
Maximum Propagation Delay, CLK to Q_H		t_{PLH}		26	36	44	53	ns
		t_{PHL}		26	35	44	53	
Minimum Pulse Width	$\overline{CLR}$ Low	t_w		10	13	17	20	ns
	CLK High or Low			10	13	17	20	
Minimum Setup Time	SH/$\overline{LD}$ High before CLK↑	t_{su}		10	13	17	20	ns
	SER before CLK↑			10	13	17	20	
	CLK INH before CLK↑			10	13	17	20	
	Data before SH/$\overline{LD}$↑			10	13	17	20	
	$\overline{CLR}$ Inactive before CLK ↑			10	13	17	20	
Minimum Hold Time	SH/$\overline{LD}$ High after CLK↑	t_h		7	10	12	15	ns
	SER after CLK↑			7	10	12	15	
	CLK INH after CLK↑			7	10	12	15	
	Data after SH/$\overline{LD}$↑			7	10	12	15	
	$\overline{CLR}$ Active after CLK↑			7	10	12	15	
Maximum Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}						pF

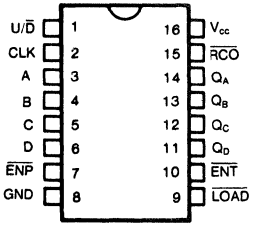
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

5

FEATURES

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look Ahead for Fast Counting**
- **Carry Output for N-bit Cascading**
- **Fully Independent Clock Circuit**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The '168 is a decade counter and the '169 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the U/$\overline{D}$ input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The ripple carry output ($\overline{RCO}$) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transition at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input.

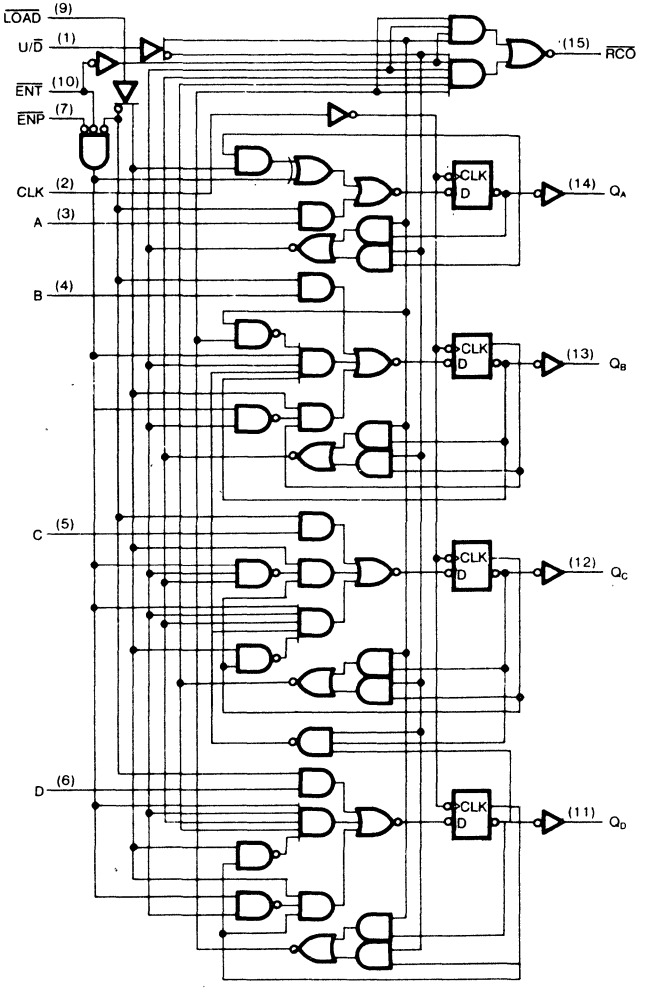
These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

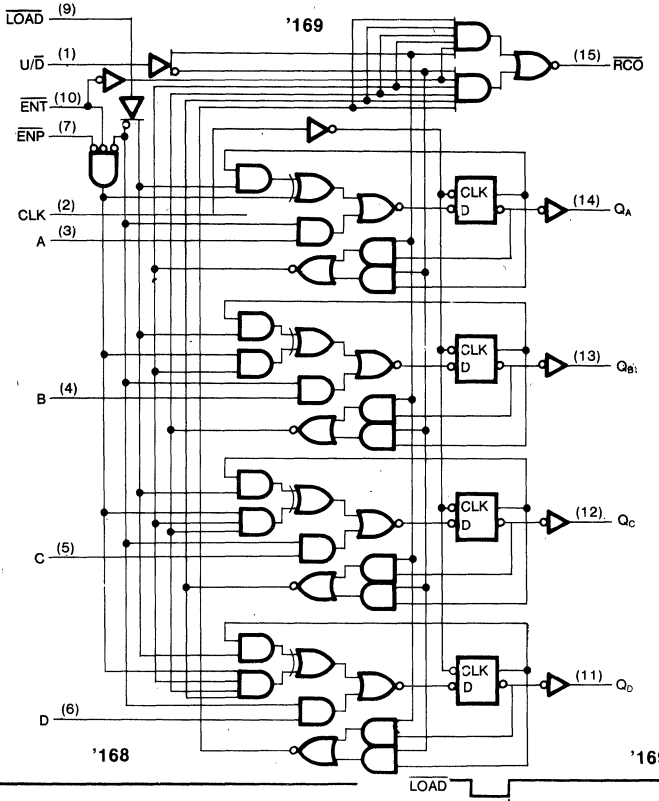
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

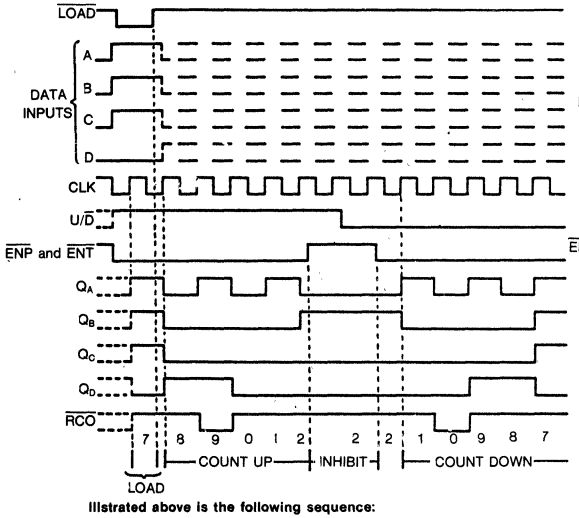
LOGIC DIAGRAMS

'168



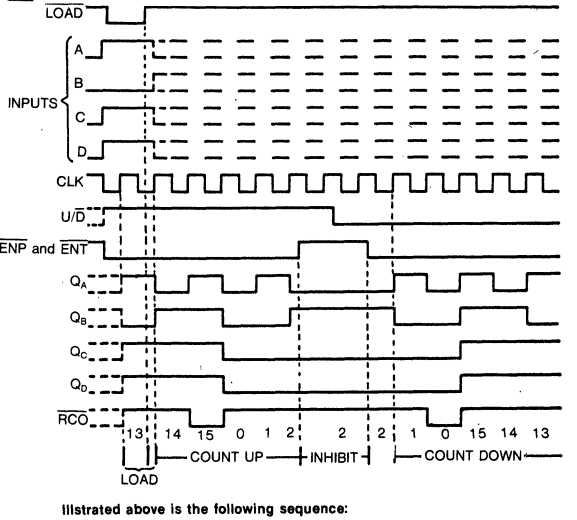
LOGIC DIAGRAMS (Continued)





Illstrated above is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



Illstrated above is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CLK	U/$\overline{D}$	$\overline{ENP}$	$\overline{ENT}$	$\overline{LOAD}$	D_n	Q_n	$\overline{RCO}$
Parallel Load	↑	X	X	X	l	i	L	(1)
	↑	X	X	X	i	h	H	(1)
Count Up	↑	h	l	l	h	X	Count Up	(1)
Count Down	↑	l	l	l	h	X	Count Down	(1)
Hold	↑	X	h	X	h	X	q_n	(1)
	↑	X	X	h	h	X	q_n	H

H=HIGH voltage level steady state
h=HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L=LOW voltage level steady state
l=LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X=Don't care
q=Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
↑=LOW-to-HIGH clock transition

NOTE:

1. The $\overline{RCO}$ is LOW when $\overline{ENT}$ is LOW and the counter is at Terminal Count Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169.
   The $\overline{RCO}$ is LOW when $\overline{ENT}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168.

5

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS168, HCTLS169

Characteristic		Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
				Typ	Guaranteed Limits			
Maximum Operating Froguency		f_{max}	C_L=50pF	35	30	25	20	MHz
Maximum Propagation Delay, CLK to $\overline{RCO}$		t_{PLH}		26	35	44	52	ns
		t_{PHL}		26	35	44	52	
Maximum Propagation Delay, CLK to Ary Q		t_{PLH}		17	22	28	33	ns
		t_{PHL}		17	22	28	33	
Maximum Propagation Delay, $\overline{ENT}$ to $\overline{RCO}$		t_{PLH}		15	20	25	30	ns
		t_{PHL}		15	20	25	30	
Maximum Propagation Delay, U/$\overline{D}$ to $\overline{RCO}$		t_{PLH}		20	27	34	40	ns
		t_{PHL}		20	27	34	40	
Minimum Pulse Duration, CLK high or low		t_w		12	16	20	24	ns
Minimum Setup Time Before CLK†	A, B, C or D	t_{su}		12	16	20	24	ns
	$\overline{ENP}$ or $\overline{ENT}$			12	16	20	24	ns
	$\overline{LOAD}$			12	16	20	24	ns
	U/$\overline{D}$			12	16	20	24	ns
Minimum Hold Time, Data after CLK†		t_h		−3	0	0	0	ns
Maximum Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

Objective Specifications

FEATURES

- **Gated output control lines for enabling or disabling the outputs**
- **Fully independent clock for operation in parallel-load or hold modes**
- **For application as bus buffer registers**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 24 mA @ V_{OL} = 0.5V for direct bus interface
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

These 4-bit registers contain D-type flip-flops with 3-state outputs, capable of driving highly-capacitive or low-impedance loads. This provides the device with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gated output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

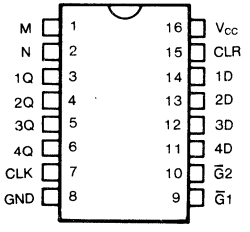
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

5

PIN CONFIGURATION

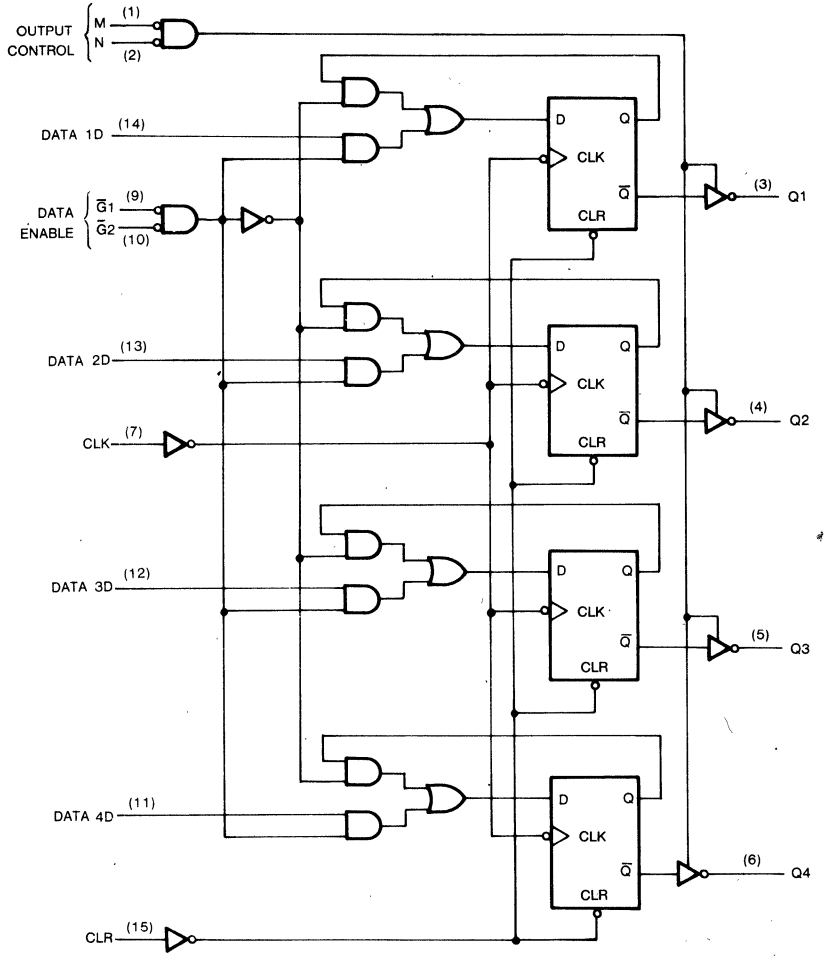


FUNCTION TABLE

Input					Output
Clear	Clock	Data Enable		Data	Q
		$\bar{G}1$	$\bar{G}2$	D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either $\bar{M}$ or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

5

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS173

Characteristic		Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
					Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}			45	30		25		20	MHz
Maximum Propagation Delay, CLK to any Q		t_{PLH}	$C_L = 50pF$		20	27		34		41	ns
			$C_L = 150pF$		23	30		39		47	
		t_{PHL}	$C_L = 50pF$		20	27		34		41	
			$C_L = 150pF$		23	30		39		47	
Maximum Propagation Delay, CLR to any Q		t_{PHL}	$C_L = 50pF$		22	30		37		45	ns
			$C_L = 150pF$		25	33		42		51	
Maximum Output Enable Time, M or N to any Q		t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	18	25		31		37	ns
				$C_L = 150pF$	21	28		36		43	
		t_{PZL}		$C_L = 50pF$	18	25		31		37	
				$C_L = 150pF$	21	28		36		43	
Maximum Output Disable Time, M or N to any Q		t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$		15	20		25		30	ns
		t_{PLZ}			15	20		25		30	
Minimum Pulse Width	CLK High or Low	t_w			10	13		17		20	ns
	CLR High				10	13		17		20	
Minimum before CLK↑	$\overline{G}1$ and $\overline{G}2$	t_{su}			15	20		25		30	ns
	Data				8	11		14		17	
	CLR Inactive				5	7		8		10	
Minimum Hold Time After CLK↑	$\overline{G}1$ and $\overline{G}2$	t_h			−3	0		0		0	ns
	Data				−3	0		0		0	
Maximum Input Capacitance		C_{IN}			5						pF
Maximum Output Capacitance		C_{OUT}	Output Disabled		10						pF
Power Dissipation Capacitance*		C_{PD}									pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '174 contains six, and the '175 contains four D-type flip-flops all sharing a common clock and a common clear. The '174 features single rail outputs for every flip-flops whereas the '175 has complementary outputs.

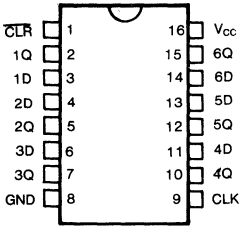
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

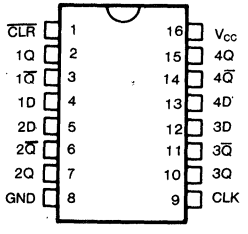
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS

'174



'175



FUNCTION TABLE

(Each Flip-Flop)

Inputs			Outputs	
$\overline{CLR}$	CLK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

† '175 only

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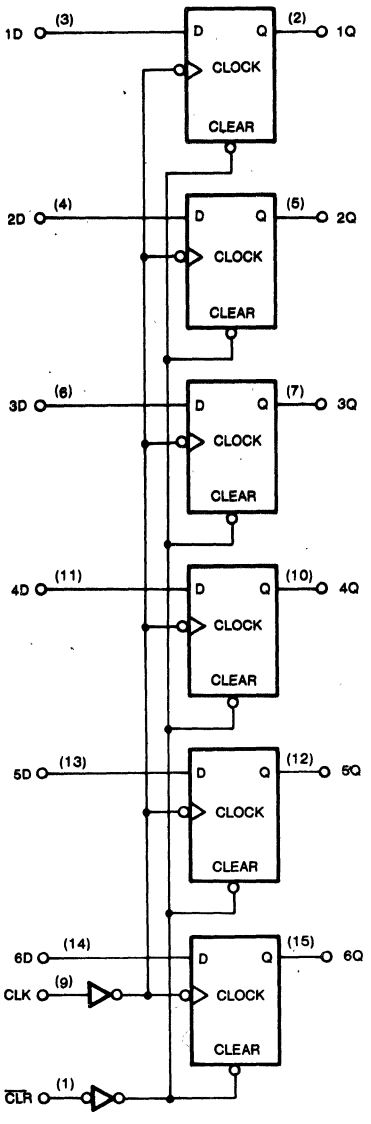
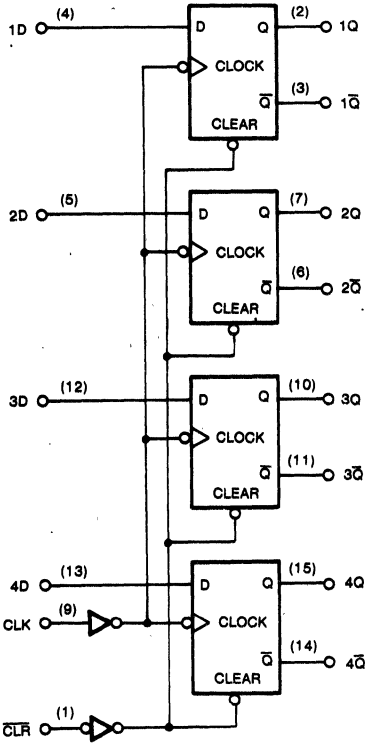
LOGIC DIAGRAMS

'174



'175



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS174, HCTLS175

Characteristic		Symbol	Conditions†	$T_A=25°C$ $V_{CC}=5.0V$	KS74HCTLS $T_A=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		$T_A=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}	$C_L=50pF$	40	30	25	20	MHz
Maximum Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}		22	30	37	45	ns
		t_{PHL}		22	30	37	35	
Maximum Propagation Delay, $\overline{CLR}$ to Q or $\overline{Q}$		t_{PLH}		26	35	43	52	
		t_{PHL}		26	35	43	52	
Minimum Setup Time before CLK↑	Data	t_{su}		10	13	17	20	ns
	$\overline{CLR}$ Inactive			12	16	20	25	
Minimum Hold Time, Data after CLK↑		t_h		−3	0	0	0	ns
Minimum Pulse Width	CLK High or Low	t_w		10	13	17	20	ns
	$\overline{CLR}$ Low			10	13	17	20	
Maximum Input Capacitace		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}						pF

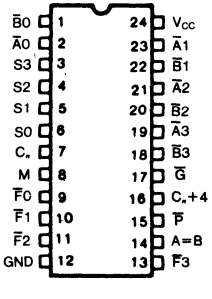
* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

FEATURES

- **Arithmetic operating modes:**
  - **Addition**
  - **Subtraction**
  - **Shift operand A one position**
  - **Magnitude comparison**
  - **Plus 12 other arithmetic operations**
- **Logic function modes:**
  - **Exclusive-OR**
  - **Comparator**
  - **AND, NAND, OR, NOR**
  - **Plus 10 other logic operations**
- **Full look-ahead for high-speed operations on long words**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current Outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline"** packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



DESCRIPTION

The '181 is an Arithmetic Logic Unit (ALU)/Function Generator that performs 16 binary arithmetic operations on two 4-bit words as shown in table 1 and 2. These operations are selected by the four functions select lines (S0, S1, S2, S3) and include addition, subtraction, decrement and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low level voltage to the mode control input(M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of 2 cascade-outputs ($\overline{P}$ and $\overline{G}$) for the 4-bits in the package. When used in conjunction with HCTLS182, high-speed arithmetic operation can be performed. The typical addition times shown in table below illustrates how little is required for addition of longer words when full carry look-ahead is employed.

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small lengths can be performed without external circuitry.

The '181 will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires and end-around or forced carry to provide A-B.

The '181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of the equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with C_n=H when performing the comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subract mode by placing the function select input S3, S2, S1, S0 at L,H,H,L respectively.

These circuits have been d to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two boolean variables without the use of external circuitry. These logical functions are selected by use of the four function select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry.
The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, OR and NOR functions.

Pin number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low Data (Table1)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_n+4	$\overline{P}$	$\overline{G}$
Active-High Data (Table 2)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_n+4$	X	Y

ALU SIGNAL DESIGNATION

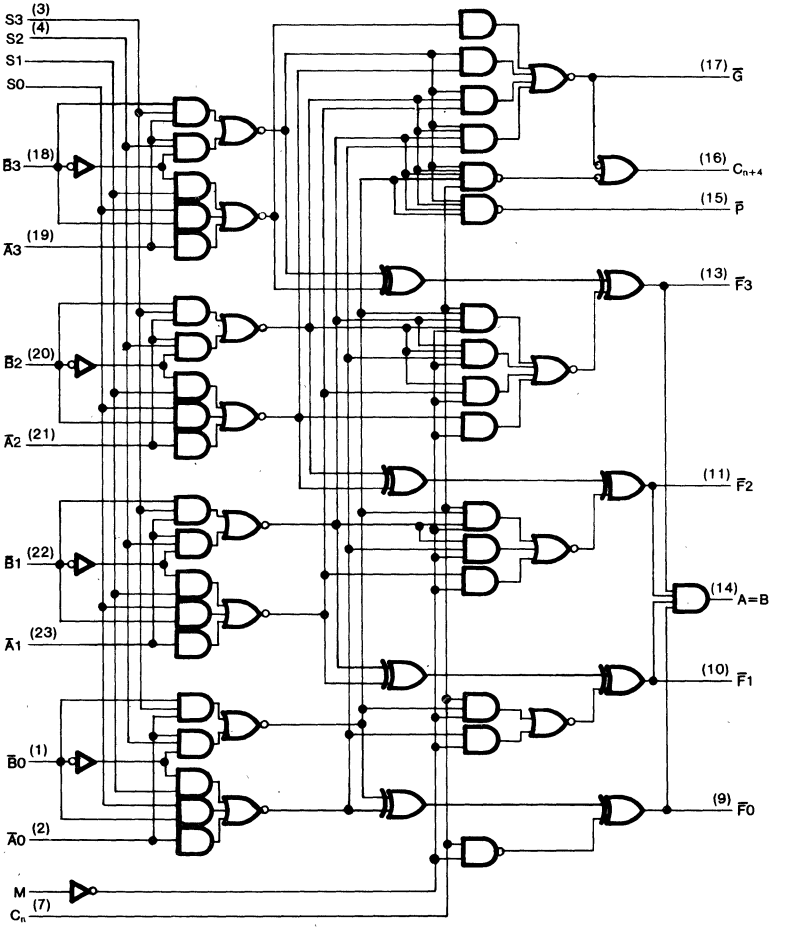
The '181 can be used with the signal designations.

The logic functions and arithmetc operations obtained with signal designations as in Table 1.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

LOGIC DIAGRAM



○ **Table 1**

Selection				Active-Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n=L (no carry)	C_n=H (with carry)
L	L	L	L	F=$\overline{A}$	F=A Minus 1	F=A
L	L	L	H	F=$\overline{AB}$	F=AB Minus 1	F=AB
L	L	H	L	F=$\overline{A}$ + B	F=A$\overline{B}$ Minus 1	F=A$\overline{B}$
L	L	H	H	F=1	F=Minus 1 (2's Comp)	F=Zero
L	H	L	L	F=$\overline{A + B}$	F=A Plus (A + $\overline{B}$)	F=A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F=$\overline{B}$	F=AB Plus (A + $\overline{B}$)	F=AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F=$\overline{A \oplus B}$	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	F=A + $\overline{B}$	F=A + $\overline{B}$	F=(A + $\overline{B}$) Plus 1
H	L	L	L	F=$\overline{A}$B	F=A Plus (A + B)	F=A Plus (A + B) Plus 1
H	L	L	H	F=A $\oplus$ B	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F=A$\overline{B}$ Plus (A + B)	F=A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F=A + B	F=(A + B)	F=(A + B) Plus 1
H	H	L	L	F=0	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	F=A$\overline{B}$	F=AB Plus A	F=AB Plus A Plus 1
H	H	H	L	F=AB	F=A$\overline{B}$ Plus A	F=A$\overline{B}$ Plus A Plus 1
H	H	H	H	F=A	F=A	F=A Plus 1

○ **Table 2**

Selection				Active-High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	$\overline{C}_n$=L (no carry)	$\overline{C}_n$=H (with carry)
L	L	L	L	F=$\overline{A}$	F=A	F=A Plus 1
L	L	L	H	F=$\overline{A + B}$	F=A + B	F=(A + B) Plus 1
L	L	H	L	F=$\overline{A}$B	F=A + $\overline{B}$	F=(A + $\overline{B}$) Plus 1
L	L	H	H	F=0	F=Minus 1 (2's Comp)	F=Zero
L	H	L	L	F=$\overline{AB}$	F=A Plus A$\overline{B}$	F=A Plus A$\overline{B}$ Plus 1
L	H	L	H	F=$\overline{B}$	F=(A + B) Plus A$\overline{B}$	F=(A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F=$\overline{A \oplus B}$	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	F=A$\overline{B}$	F=A$\overline{B}$ Minus 1	F=A$\overline{B}$
H	L	L	L	F=$\overline{A}$ + B	F=A Plus AB	F=A Plus AB Plus 1
H	L	L	H	F=$\overline{A \oplus B}$	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F=(A + $\overline{B}$) Plus AB	F=(A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F=AB	F=AB Minus 1	F=AB
H	H	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	F=A + $\overline{B}$	F=(A + B) Plus A	A=(A + B) Plus A Plus 1
H	H	H	L	F=A + B	F=(A + $\overline{B}$) Plus A	F=(A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F=A	F=A Minus 1	F=A

* Each bit is shifted to the next more significant position

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

INPUT PAIRS HIGH/NOT HIGH TEST TABLE
FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$	In-Phase
t_{PHL} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_n+4	Out-of-Phase

PARAMETER MEASUREMENT INFORMATION

$\overline{SUM}$ MODE TEST TABLE
FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phone
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_n+4	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_n+4	Out-of-Phase

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS181

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
		$C_L = 50pF$	Typ	Guaranteed Limits			
Propagation Delay, C_n to C_n+4	t_{PLH}	M=0V	14	18	23	27	ns
	t_{PHL}	$\overline{Sum}$ or $\overline{Diff}$ Mode	14	18	23	27	
Propagation Delay, $\overline{A}$ or $\overline{B}$ to C_n+4	t_{PLH}	M=S1=S2=0V	20	28	35	42	ns
	t_{PHL}	S0=S3=4.5V	20	28	35	42	
Propagation Delay, $\overline{A}$ or $\overline{B}$ to C_n+4	t_{PLH}	M=S0=S3=0V	25	34	42	50	ns
	t_{PHL}	S1=S2=4.5V	25	34	42	50	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$	t_{PLH}	M=S1=S2=0V	22	31	39	47	ns
	t_{PHL}	S0=S3=4.5V	22	31	39	47	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$	t_{PLH}	M=S0=S3=0V	23	32	40	48	ns
	t_{PHL}	S1=S2=4.5V	23	32	40	48	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$	t_{PLH}	M=S0=S3=0V	25	34	43	51	ns
	t_{PHL}	S1=S2=4.5V	25	34	43	51	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$	t_{PLH}	M=S1=S2=0V	25	34	42	50	ns
	t_{PHL}	S0=S3=4.5V	25	34	42	50	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F_i}$	t_{PLH}	M=S1=S2=0V	25	34	42	50	ns
	t_{PHL}	S0=S3=4.5V	25	34	42	50	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F_i}$	t_{PLH}	M=S0=S3=0V	25	34	42	50	ns
	t_{PHL}	S1=S2=4.5V	25	34	42	50	
Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F_i}$	t_{PLH}	M=S1=S2=0V	25	34	42	50	ns
	t_{PHL}	S1=S2=4.5V	25	34	42	50	
Propagation Delay $\overline{A}$ or $\overline{B}$ to A=B	t_{PLH}	M=4.5V	20	29	35	42	ns
	t_{PHL}		20	28	35	42	
Propagation Delay A or B to A=B	t_{PLH}	M=S0=S3=0V	25	34	42	50	ns
	t_{PHL}	S1=S2=4.5V	25	34	42	50	
Propagation Delay C_n to any $\overline{F}$	t_{PLH}		20	28	35	42	ns
	t_{PHL}		20	28	35	42	
Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase

INPUT BITS EQUAL/NOT EQUAL TEST TABLE
FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_n+4	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_n+4	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_n+4	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_n+4	Out-of Phase

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$\overline{\text{DIFF}}$ MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A=B	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A=B	Out-of-Phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_n+4 or any F	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{a}i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_n+4	In-Phase

FEATURES

- **Compatible Carry Functions for direct ALU connection**
- **Cascadable to perform look-ahead across n-bit adders.**
- **High output current drive: I_{OL} = 8mA @ V_{OL} = 0.5V**
- **Low power consumption characteristic of CMOS**
- **Direct interface capability to TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**

  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline"** packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

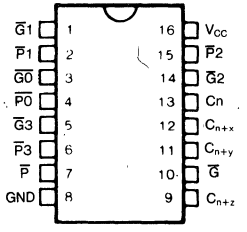
The '182 is a high-speed, look-ahead carry generator, capable of anticipating a carry across four binary adders or group of adders. These devices can be cascaded to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjuction with the AHCT181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each 182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true from, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the 182 are

$$Cn+x = G0 + P0\ Cn$$
$$Cn+y = G1 + P1\ G0 + P1\ P0\ Cn$$
$$Cn+z = G2 + P2\ G1 + P2\ P1\ G0 + P2\ P1\ P0\ Cn$$
$$\overline{G} = \overline{G3 + P3\ G2 + P2\ G1 + P3\ P2\ P1\ G0}$$
$$\overline{P} = \overline{P3\ P2\ P1\ P0}$$

PIN CONFIGURATION



PIN DESIGNATIONS

Designation	Pin No	Function
$\overline{G0}$,$\overline{G1}$,$\overline{G2}$,$\overline{G3}$	3,1,14,5	Active Low Carry Generate Inputs
$\overline{P0}$,$\overline{P1}$,$\overline{P2}$,$\overline{P3}$	4,2,15,6	Active Low Carry Propagate Inputs
Cn	13	Carry Input, Active High
Cn+x, Cn+y, Cn+z	12,11,9	Carry Outputs
$\overline{G}$	10	Active Low Carry Generate Output
$\overline{P}$	7	Active Low Carry Propagae Output
V_{CC}	16	Supply Voltage
GND	8	Ground

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FUNCTION TABLES

FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FOR C_n+ x OUTPUT

INPUTS			OUTPUT
$\overline{G}0$	$\overline{P}0$	C_n	C_n+ x
L	X	X	H
X	L	H	H
All other combinations			L

Cn+y OUTPUT

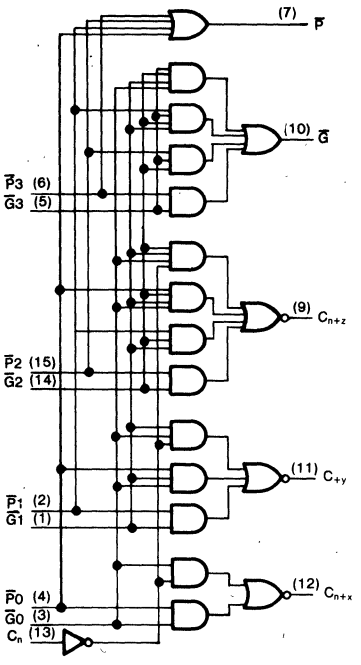
INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

Cn+z OUTPUT

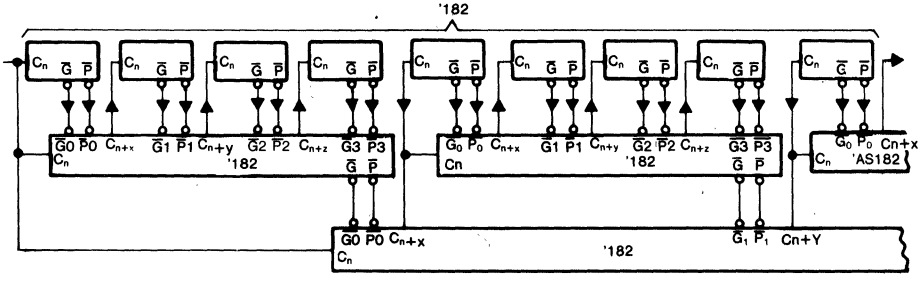
INPUTS							OUTPUT
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high-level, L = low level, X = dont' care
Any inputs not shown in a given table are don't care with respect to that output.

LOGIC DIAGRAM



Figure; THE '182 IN A 64-BIT LOOK-AHEAD CARRY CIRCUIT



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS182

Characteristic	Symbol	Conditions†	$T_a=25°C$ $V_{CC}=5.0V$		KS74HCTLS $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$	KS54HCLTS $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Propagation Delay $\overline{Pi}$ or $\overline{Gi}$ to C_{n+x} C_{n+y}, C_{n+z}	t_{PLH}	$C_L=50pF$	19	26	32	39	ns
	t_{PHL}		19	26	32	39	
Propagation Delay $\overline{Pi}$ or $\overline{Gi}$ to $\overline{G}$	t_{PLH}	$C_L=50pF$	19	26	32	39	ns
	t_{PHL}		19	26	32	39	
Propagation Delay C_n to C_{n+x}, C_{n+y}, C_{n+z}	t_{PLH}	$C_L=50pF$	25	27	34	41	ns
	t_{PHL}		25	27	34	41	
Propagation Delay $\overline{Pi}$ to $\overline{P}$	t_{PLH}	$C_L=50pF$	15	20	25	30	ns
	t_{PHL}		15	20	25	30	
Input Capacitance	C_{IN}		5				pF
Power Disipation Capacitance*	C_{PD}						pF

*C_{PD} determines the no-load dynamic power dissipation: $PD=C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$.
†For Acc switching test circuits and timing waveforms see section 2.

FEATURES

- **For use in high-speed wallace-tree summing**
- **Fast addition operation**
- **Low power consumption characteristic of CMOS**
- **High output current drive: I_{OL} = 8mA @ V_{OL} = 0.5V**
- **Direct interface capability with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

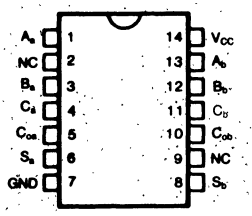
DESCRIPTION

The '183 is a dual full adder features an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than 2 gate delays.

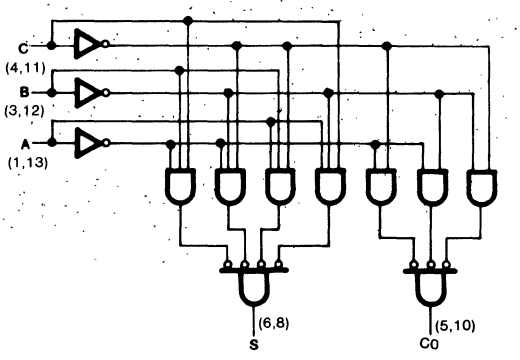
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Half)

Inputs			Output	
A	B	C	S	C_o
L	L	L	L	L
H	L	L	H	L
L	H	L	H	L
L	L	H	H	L
H	H	L	L	H
H	L	H	L	H
L	H	H	L	H
H	H	H	H	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS 183

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits		
Propagation Delay	t_{PLH}	C_L=50pF	15	22	27	33	ns
	t_{PHL}		17	23	29	35	
Input Capacitance	C_{IN}						pF
Power dissipation Capacitance*	C_{PD}						pF

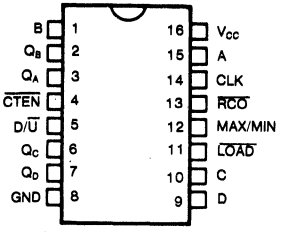
* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

Synchronous 4-Bit Up/Down Decade Counters

FEATURES

- **Single down/up count control line**
- **Look-ahead circuitry enhances speed of cascaded counters**
- **Fully synchronous in count modes**
- **Asynchronously presettable with load control**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{LOAD}$	D/$\overline{U}$	$\overline{CTEN}$	CLK	Input	O_n
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	l	↑	X	count up
count down	H	H	l	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

$\overline{RCO}$ AND MAX/MIN FUNCTION TABLE

INPUTS		TERMINAL COUNT STATE					OUTPUTS	
D/$\overline{U}$	$\overline{CTEN}$	CLK	Q_A	Q_B	Q_C	Q_D	MAX/MIN	$\overline{RCO}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊓	H	X	X	H	⌐	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	⌐	⊓

H = HIGH voltage level
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
X = Don't care
↑ = LOW-to-HIGH CLK transition
⊓ = one LOW level pulse
⌐ = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with a synchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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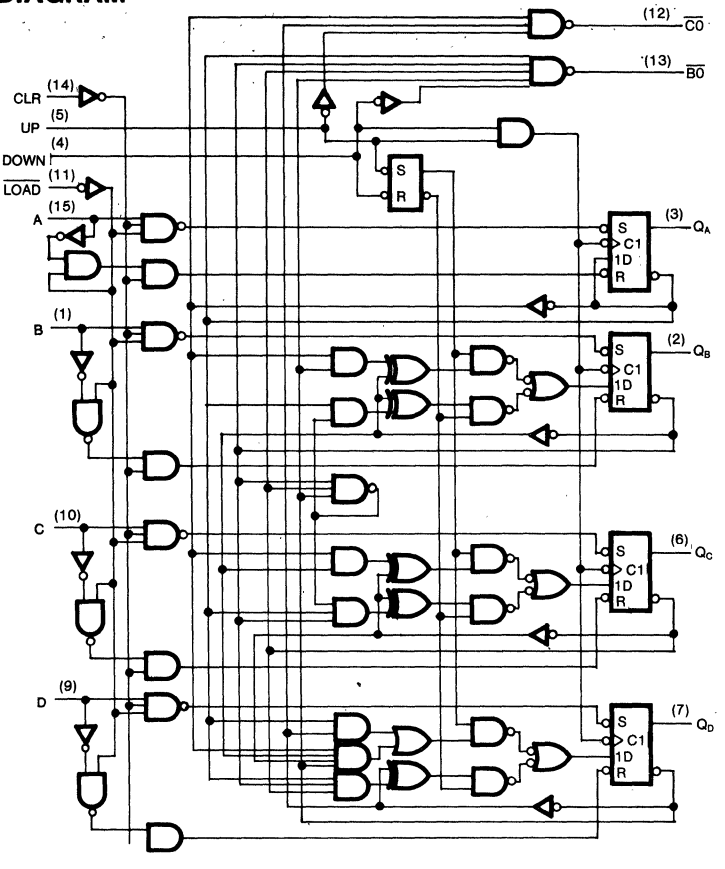
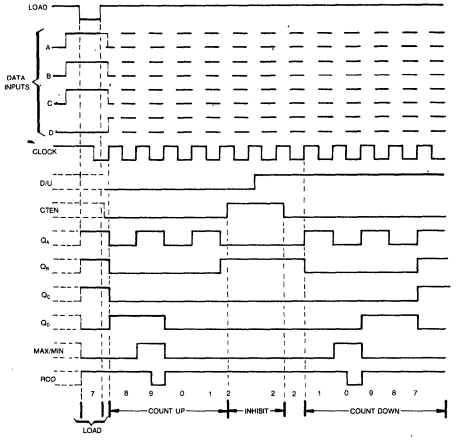
LOGIC DIAGRAM



Typical load, count, and inhibit sequences



Sequence;
(1) Load (preset) to BCD seven.
(2) Count up to eight, mine(maximum) zero, one, and two.
(3) Inhibit
(4) Count down to one, zero (minimum), nine, eight, and seven

NOTE A: Clear overrides load data, and count inputs.
Note B: When count up, count-down input must be high; when counting down, countup intput must be high.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS190

Characteristic		Symbol	Conditions†	$T_a=25°C$ $V_{CC}=5.0V$	KS74HCTLS $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54HCTLS $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}	$C_L=50pF$	30	20	16	14	MHz
Maximum Propagation Delay, $\overline{LOAD}$ to any Q		t_{PLH}		30	40	50	60	ns
		t_{PHL}		30	40	50	60	
Maximum Propagation Delay, A,B,C, D to any Q		t_{PLH}		27	36	45	64	ns
		t_{PHL}		27	36	45	54	
Maximum Propagation Delay, CLK to $\overline{RCO}$		T_{PLH}		17	22	28	33	ns
		t_{PHL}		17	22	28	33	
Maximum Propagation Delay, CLK to any Q		t_{PLH}		23	30	37	45	ns
		t_{PHL}		23	30	37	45	
Maximum Propagation Delay, CLK to MAX/MIN		t_{PLH}		35	47	59	70	ns
		t_{PHL}		35	47	59	70	
Maximum Propagation Delay, D/$\overline{U}$ to $\overline{RCO}$		t_{PLH}		33	45	56	67	ns
		t_{PHL}		33	45	56	67	
Maximum Propagation Delay, D/$\overline{U}$ to MAX/MIN		t_{PLH}		25	33	41	50	
		t_{PHL}		25	33	41	50	
Maximum Propagation Delay, $\overline{CTEN}$ to $\overline{RCO}$		t_{PLH}		25	33	41	50	ns
		t_{PHL}		25	33	41	50	
Minimum Pulse Width	CLK High or Low	t_w		13	17	21	25	ns
	$\overline{LOAD}$ Low			13	17	21	25	
Minimum Setup Time	Data before $\overline{LOAD}$↑	t_{su}		10	13	17	20	ns
	$\overline{CTEN}$ before CLK↑			20	26	34	40	
	D/$\overline{U}$ before CLK↑			10	13	17	20	
	$\overline{LOAD}$ Inactive before CLK↑			15	20	25	30	
Minimum Hold Time	Data after $\overline{LOAD}$↑	t_h		1	3	5	5	ns
	$\overline{CTEN}$ after CLK↑			−3	0	0	0	
	D/$\overline{U}$ after CLK↑			−3	0	0	0	
Maximum Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}		80				pF

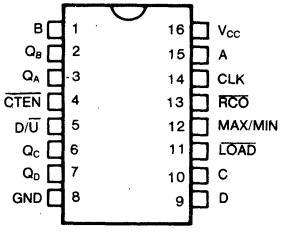
* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Synchronous 4-Bit Up/Down Binary Counters

FEATURES

- **Single down/up count control line**
- **Look-ahead circuitry enhances speed of cascaded counters**
- **Fully synchronous in count modes**
- **Asynchronously presettable with load control**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{LOAD}$	D/$\overline{U}$	$\overline{CTEN}$	CLK	Input	O_n
parallel load	L L	X X	X X	X X	L H	L H
count up	H	L	↑	↑	X	count up
count down	H	H	↑	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

$\overline{RCO}$ AND MAX/MIN FUNCTION TABLE

INPUTS		TERMINAL COUNT STATE					OUTPUTS	
D/$\overline{U}$	$\overline{CTEN}$	CLK	Q_A	Q_B	Q_C	Q_D	MAX/MIN	$\overline{RCO}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊔	H	X	X	H	⊓	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	⊓	⊔

H = HIGH voltage level
L = LOW voltage level
I = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
X = Don't care
↑ = LOW-to-HIGH CLK transition
⊔ = one LOW level pulse
⊓ = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

DESCRIPTION

These are high-speed synchronous, reversible 4-bit binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with a synchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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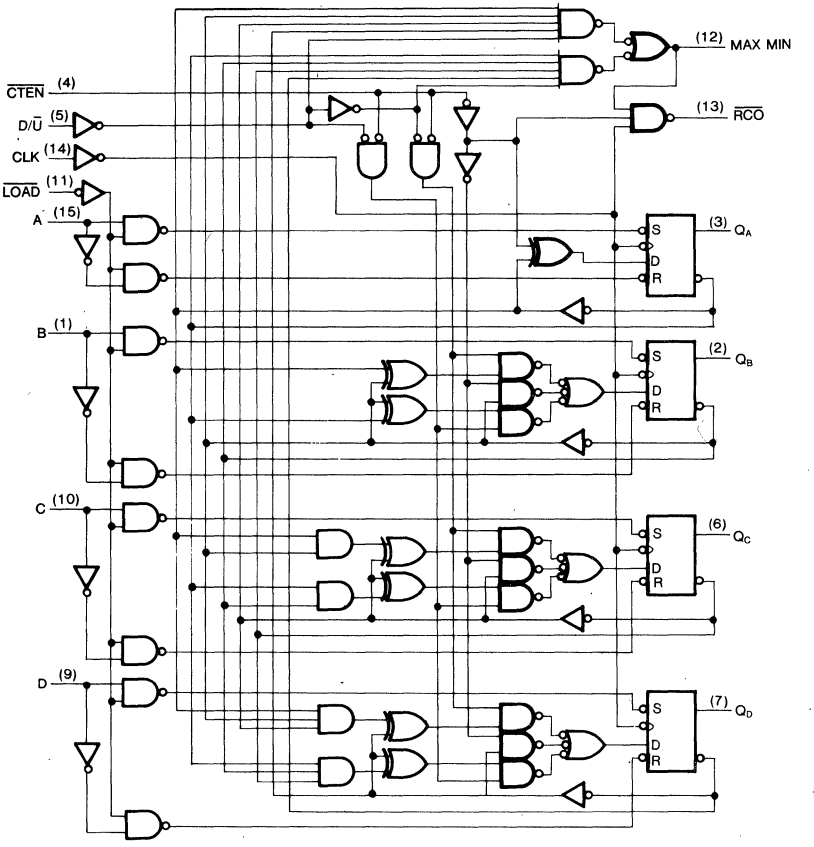
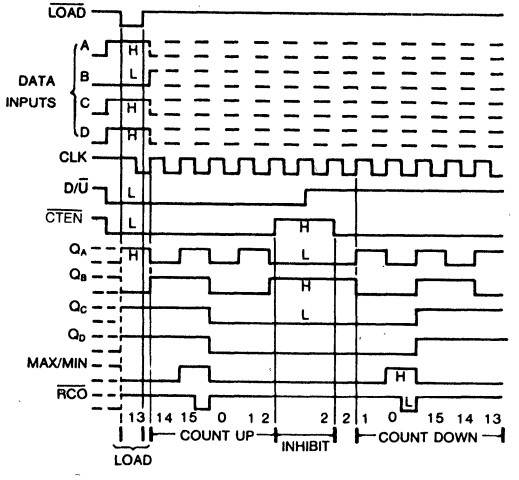
LOGIC DIAGRAM



Typical Load, Count, and Inhibit Sequence



Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS191

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	30	20	16		14	MHz
Maximum Propagation Delay, $\overline{LOAD}$ to any Q		t_{PLH}		30	40	50		60	ns
		t_{PHL}		30	40	50		60	
Maximum Propagation Delay, A,B,C, D to any Q		t_{PLH}		27	36	45		64	ns
		t_{PHL}		27	36	45		54	
Maximum Propagation Delay, CLK to $\overline{RCO}$		T_{PLH}		17	22	28		33	ns
		t_{PHL}		17	22	28		33	
Maximum Propagation Delay, CLK to any Q		t_{PLH}		23	30	37		45	ns
		t_{PHL}		23	30	37		45	
Maximum Propagation Delay, CLK to MAX/MIN		t_{PLH}		35	47	59		70	ns
		t_{PHL}		35	47	59		70	
Maximum Propagation Delay, D/$\overline{U}$ to $\overline{RCO}$		t_{PLH}		33	45	56		67	ns
		t_{PHL}		33	45	56		67	
Maximum Propagation Delay, D/$\overline{U}$ to MAX/MIN		t_{PLH}		25	33	41		50	
		t_{PHL}		25	33	41		50	
Maximum Propagation Delay, $\overline{CTEN}$ to $\overline{RCO}$		t_{PLH}		25	33	41		50	ns
		t_{PHL}		25	33	41		50	
Minimum Pulse Width	CLK High or Low	t_w		13	17	21		25	ns
	$\overline{LOAD}$ Low			13	17	21		25	
Minimum Setup Time	Data before $\overline{LOAD}$↑	t_{su}		10	13	17		20	ns
	$\overline{CTEN}$ before CLK↑			20	26	34		40	
	D/$\overline{U}$ before CLK↑			10	13	17		20	
	$\overline{LOAD}$ Inactive before CLK↑			15	20	25		30	
Minimum Hold Time	Data after $\overline{LOAD}$↑	t_h		1	3	5		5	ns
	$\overline{CTEN}$ after CLK↑			−3	0	0		0	
	D/$\overline{U}$ after CLK↑			−3	0	0		0	
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		80					pF

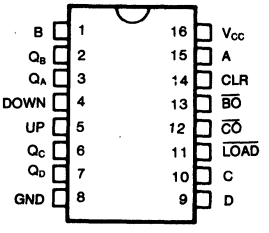
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Synchronous 4-Bit Up/Down Decade Counters with Dual Clock

FEATURES

- **Look-ahead circuit enhances cascaded counters**
- **Fully synchronous in count modes**
- **Parallel asynchronous load for modulo-N count lengths**
- **Asynchronous clear**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

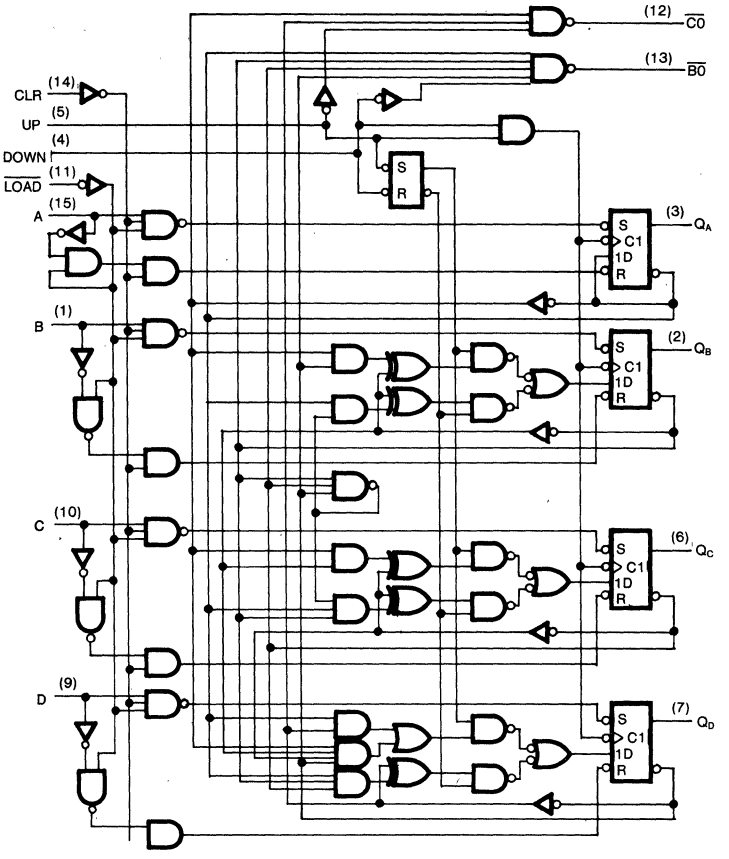
These counters were designed to be cascaded without the need for external circuitry. The borrow output ($\overline{BO}$) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

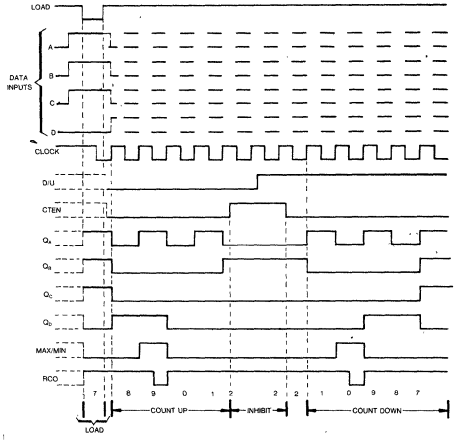
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

5

LOGIC DIAGRAM



Typical load, count, and inhibit sequences



Sequence;
(1) Load (preset) to BCD seven.
(2) Count up to eight, mine(maximum) zero, one, and two.
(3) Inhibit
(4) Count down to one, zero (minimum), nine, egiht, and seven

NOTE A: Clear overrides load data, and count inputs.
Note B: When count up, count-down input must be high; when counting down, countup intput must be high.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS192

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	35	25	20		18	MHz
Maximum Propagation Delay, UP to $\overline{CO}$		t_{PLH}		18	25	31		37	ns
		t_{PHL}		18	25	31		37	
Maximum Propagation Delay, DOWN to $\overline{BO}$		t_{PLH}		18	24	30		36	ns
		t_{PHL}		18	24	30		36	
Maximum Propagation Delay, UP or DOWN to any Q		T_{PLH}		32	42	52		63	ns
		t_{PHL}		32	42	52		63	
Maximum Propagation Delay, $\overline{LOAD}$ to any Q		t_{PLH}		30	40	50		60	ns
		t_{PHL}		30	40	50		60	
Maximum Propagation Delay, CLR to any Q		t_{PHL}		18	24	30		36	ns
Minimum Pulse Width	CLR High	t_w		10	13	17		20	ns
	$\overline{LOAD}$ Low			10	13	17		20	
	UP or DOWN High or Low			10	13	17		20	
Minimum Setup Width	Data before $\overline{LOAD}$↑	t_{su}		10	13	17		20	ns
	CLR Inactive before UP↑ or DOWN↑			10	13	17		20	
	$\overline{LOAD}$ Inactive before UP↑ or DOWN↑			10	13	17		20	ns
	UP high before DOWN↑			10	13	17		20	
	DOWN high before UP↑			10	13	17		20	
Minimum Hold Time	Data after $\overline{LOAD}$↑	t_h		1	3	5		5	ns
	UP High after DOWN↑			−3	0	0		0	
	DOWN High after UP↑			−3	0	0		0	
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		80					pF

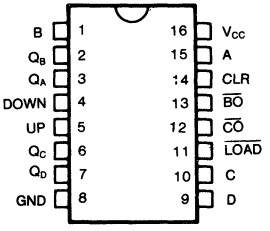
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Synchronous 4-Bit Up/Down Binary Counters with Dual Clock

FEATURES

- **Look-ahead circuitry enhances cascaded counters**
- **Fully synchronous in count modes**
- **Parallel asynchronous load for modulo-N count lengths**
- **Asynchronous clear**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These are high-speed synchronous reversible 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output ($\overline{BO}$) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

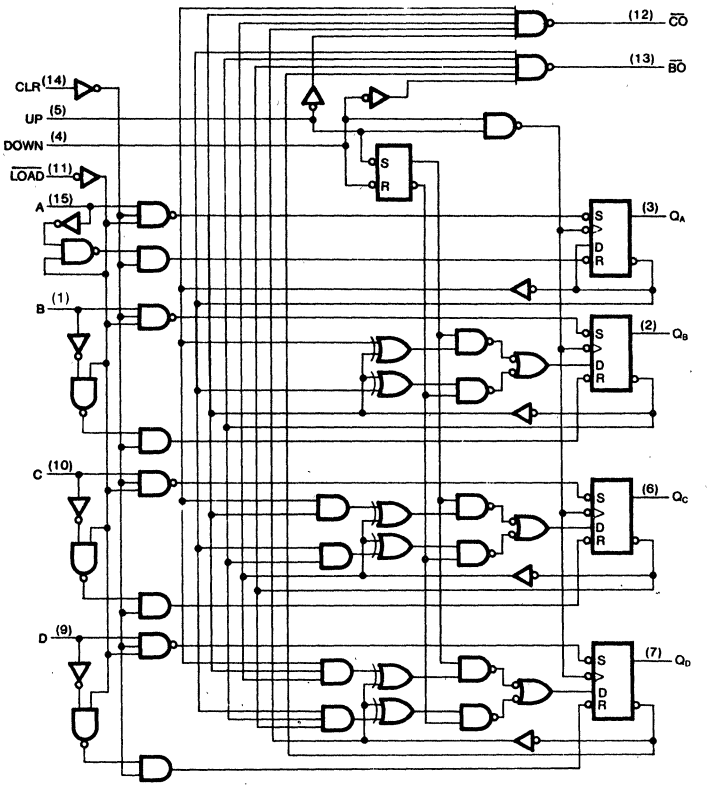
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

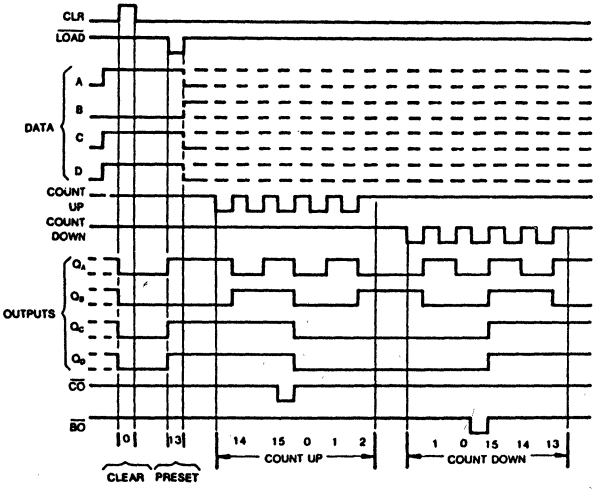
OPERATING MODE	INPUTS								OUTPUTS					
	CLR	$\overline{LOAD}$	UP	DOWN	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{CO}$	$\overline{BO}$
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X		count down				H	H**

H= HIGH voltage level
L= LOW voltage lovel
X= don't care
↑= LOW-to-HIGH clock transition
* $\overline{CO}$ = UP at terminal count up (HHHH)
** $\overline{BO}$ = DOWN at terminal count down (LLLL)

LOGIC DIAGRAM



Typical Clear, Load, and Count Sequences



Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.
Note A: Clear overrides load data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS193

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	35	25		20	18	MHz
Maximum Propagation Delay, UP to $\overline{CO}$		t_{PLH}		18	25		31	37	ns
		t_{PHL}		18	25		31	37	
Maximum Propagation Delay, DOWN to $\overline{BO}$		t_{PLH}		18	24		30	36	ns
		t_{PHL}		18	24		30	36	
Maximum Propagation Delay, UP or DOWN to any Q		T_{PLH}		32	42		52	63	ns
		t_{PHL}		32	42		52	63	
Maximum Propagation Delay, $\overline{LOAD}$ to any Q		t_{PLH}		30	40		50	60	ns
		t_{PHL}		30	40		50	60	
Maximum Propagation Delay, CLR to any Q		t_{PHL}		18	24		30	36	ns
Minimum Pulse Width	CLR High	t_w		10	13		17	20	ns
	$\overline{LOAD}$ Low			10	13		17	20	
	UP or DOWN High or Low			10	13		17	20	
Minimum Setup Width	Data before $\overline{LOAD}$↑	t_{su}		10	13		17	20	ns
	CLR Inactive before UP↑ or DOWN↑			10	13		17	20	
	$\overline{LOAD}$ Inactive before UP↑ or DOWN↑			10	13		17	20	
	UP high before DOWN↑			10	13		17	20	
	DOWNhigh before UP↑			10	13		17	20	
Minimum Hold Time	Data after $\overline{LOAD}$↑	t_h		1	3		5	5	ns
	UP High after DOWN↑			−3	0		0	0	
	DOWN High after UP↑			−3	0		0	0	
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}		80					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Left or Right Shifts**
- **Parallel Synchronous Loading**
- **Direct Overriding Clear**
- **Temporary Data Latching Capability**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74HCTLS: −40°C to +85°C KS54HCTLS: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

These bidirectional shift registers feature parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

— Inhibit clock (temporary data latch/do nothing)
— Shift-right (in the direction Q_A toward Q_D)
— Shift-left (in the direction Q_D toward Q_A)
— Parallel (broadside) load

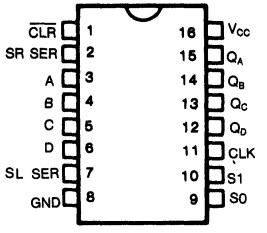
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift-right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



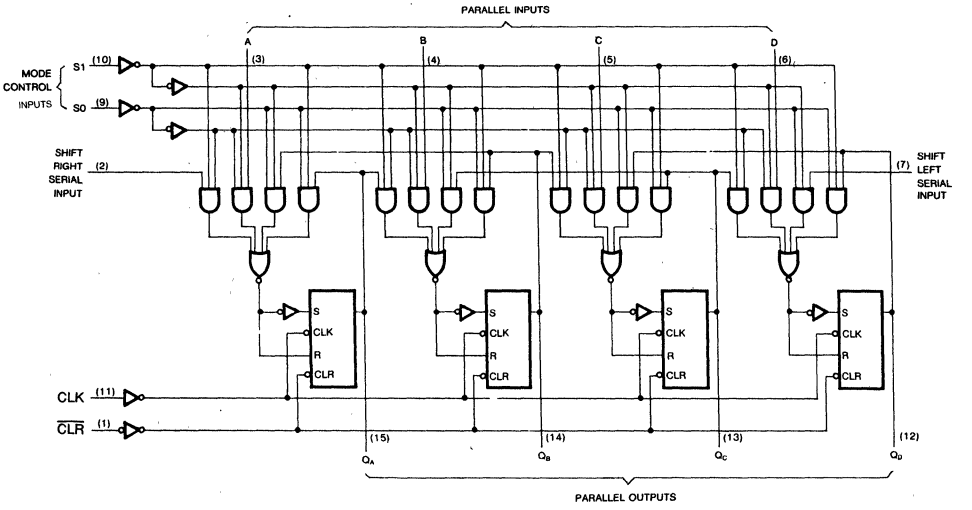
FUNCTION TABLE

INPUTS										OUTPUTS			
CLR	MODE		CLK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

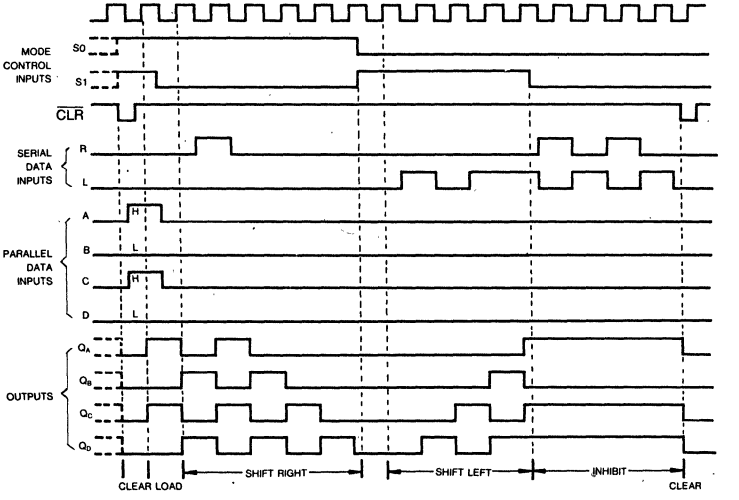
H=high level (steady state)
L=low level (steady state)
X=irrelevant (any input, including transitions)
↑=transition from low to high level
a,b,c,d=the level of steady-state input at inputs, A,B,C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}=the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}=the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

LOGIC DIAGRAM

(positive logic)



typical clear, load, right-shift, inhibit, and clear sequences



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} +0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} +0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} +0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS194

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30		25	20	MHz
Maximum Propagation Delay, CLK to Q_H		t_{PLH}		18	24		30	36	ns
		t_{PHL}		18	24		30	36	
Maximum Propagation Delay, $\overline{CLR}$ to Q_H		t_{PHL}		21	28		35	42	ns
Minimum Pulse Width	$\overline{CLR}$ to Low	t_w		12	16		20	24	ns
	CLK High or Low			12	16		20	24	
Minimum Setup Time, Any Input before CLK↑		t_s		10	17		20	20	ns
Minimum Hold Time, Data after CLK↑		t_s		−3	0		0	0	ns
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

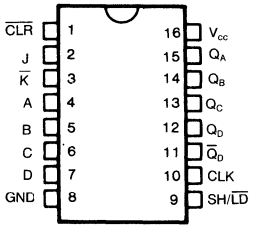
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

4-Bit Bidirectional Universal Shift Registers

FEATURES

- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Parallel Synchronous Loading**
- **J and K Inputs to First Stage**
- **Right-shift Only with Complementary Outputs on Last Stage**
- **Direct Overriding Clear**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction A_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associate flip-flops and appears at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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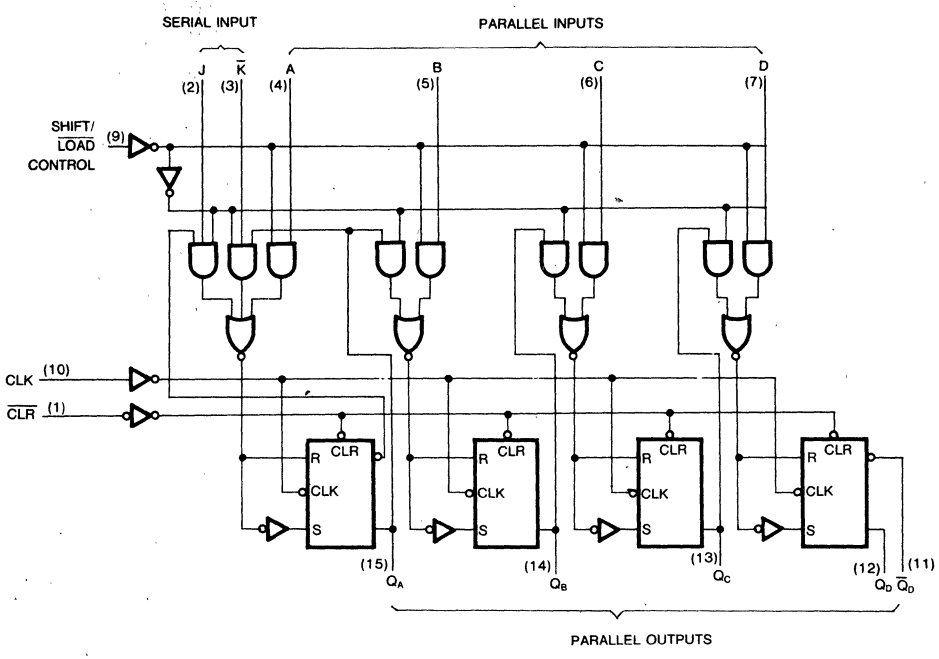
FUNCTION TABLE

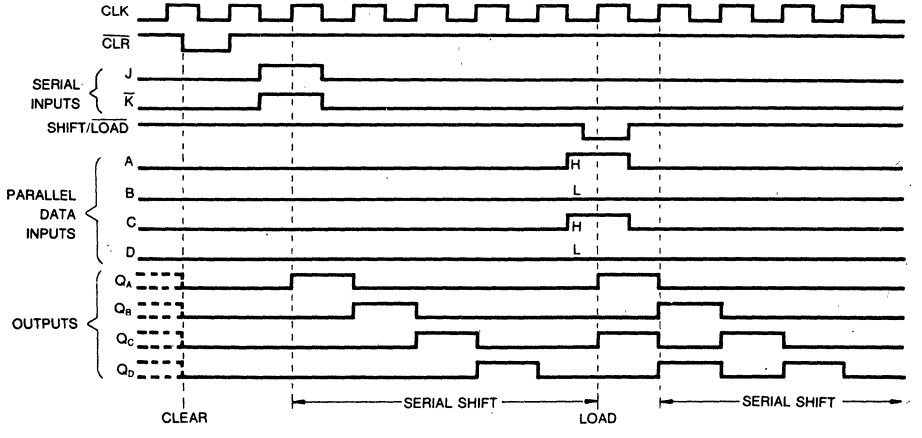
INPUTS									OUTPOUTS				
$\overline{CLR}$	SHIFT/$\overline{LOAD}$	CLK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H=high level (steady state)
L=low level (steady state)
X=irrelevant (any input, including transitions)
↑=transition from low to high level
a,b,c,d=the level of steady-state input at A,B,C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}=the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}=the level of Q_A, Q_B or Q_C, respectively, before the mostrecent transition of the clock.

LOGIC DIAGRAM



typical clear, shift, and load sequences



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS195

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	50	30	25	20	MHz
Maximum Propagation Delay, CLK to Q_H		t_{PLH}		18	24	30	36	ns
		t_{PHL}		18	24	30	36	ns
Maximum Propagation Delay, $\overline{CLR}$ to Q_H		t_{PHL}		21	28	35	42	ns
Maximum Pulse Width	$\overline{CLR}$ Low	t_w		10	12	15	20	ns
	CLK High or Low			12	16	20	24	
Minimum Setup Time before CLK↑	SH/$\overline{LD}$ High	t_{su}		15	20	25	25	ns
	Serial or Parallel			12	15	20	24	
	$\overline{CLR}$ inactive			15	20	25	25	
Minimum Hold Time after CLK↑	SH/$\overline{LD}$ High	t_h		−3	0		0	ns
	Serial or Parallel Data			−3	0		0	
Maximum Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Octal Buffers and Line Drivers with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 24mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

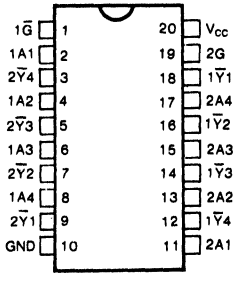
DESCRIPTION

These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

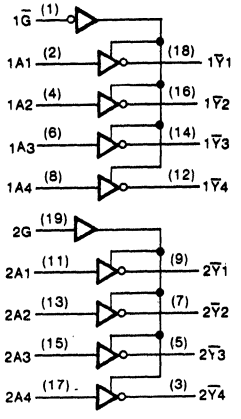
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Input		Output
G̅	A	Y
L	L	H
L	H	L
H	X	Z

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Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS210

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Propagation Delay, A to $\overline{Y}$	t_{PLH}	$C_L = 50pF$		13	18		22	27	ns
		$C_L = 150pF$		16	21		27	33	
	t_{PHL}	$C_L = 50pF$		13	18		22	27	
		$C_L = 150pF$		16	21		27	33	
Maximum Output Enable Time, Enable to $\overline{Y}$	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	17	23		29	34	ns
			$C_L = 150pF$	20	26		34	40	
	t_{PZL}		$C_L = 50pF$	17	23		29	34	
			$C_L = 150pF$	20	26		34	40	
Maximum Output Disable Time, Enable to $\overline{Y}$	t_{PHZ}	$R_L = 1k\Omega$		16	21		26	32	ns
	t_{PLZ}	$C_L = 50pF$		16	21		26	32	
Maximum Input Capacitance	C_{IN}			5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	Output Disabled		5					pF
		Output Enabled		30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

5

FEATURES

- **Designed specifically for high-speed memory decoders and data transmission systems**
- **Incorporates 2 enable inputs to simplify cascading and/or data reception**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used with high-speed memories utilizing a fast enable circuit. The delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

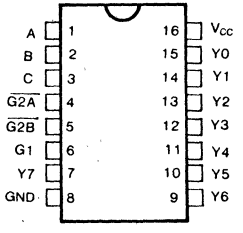
The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding.

A 24-line decoder can be implemented without external inverters and a 31-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

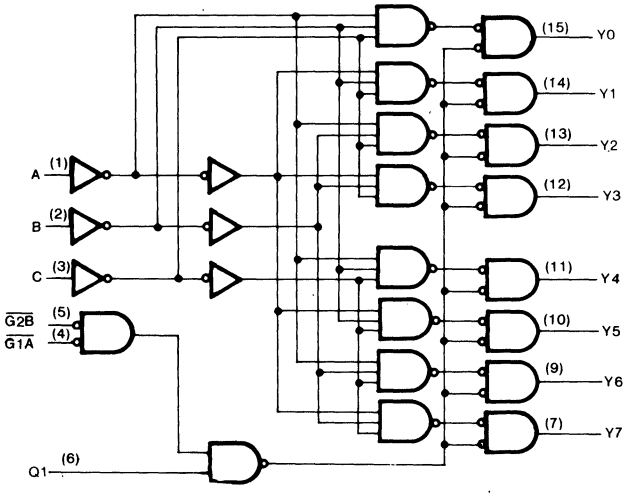


FUNCTION TABLE

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	H	L	L	L	H	L	L	L	L	L
H	L	H	L	L	L	L	L	H	L	L	L	L
H	L	H	L	L	L	L	L	L	H	L	L	L
H	L	H	L	H	L	L	L	L	L	H	L	L
H	L	H	H	L	L	L	L	L	L	L	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H

*$\overline{G2} = \overline{G2A} + \overline{G2B}$.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

5

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_Z=2.4V Other Inputs: At V_{CC} or GND I_O=0		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS238

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ		Guaranteed Limits		
Maximum Propagation Delay, A, B, C or any Y	t_{PLH}	C_L=50pF	22	30	37	45	ns
	t_{PHL}		22	30	37	45	
Maximum Propagation Delay, G1 to any Y	t_{PLH}		24	32	40	48	ns
	t_{PHL}		24	32	40	48	
Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to any Y	t_{PLH}		18	25	31	37	ns
	t_{PHL}		18	25	31	37	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}		50				pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Designed specifically for high-speed memory decoders and data transmission systems**
- **Incorporates 2 enable inputs to simplify cascading and/or data reception**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline"** packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

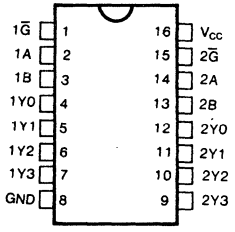
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory.

This means that the effective system delay introduced by the decoder is negligible.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

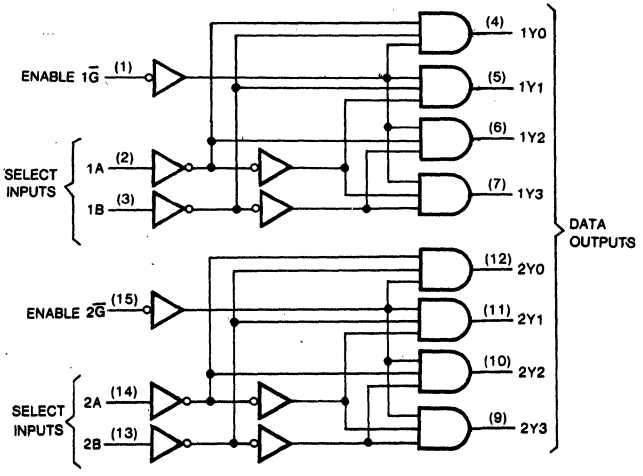
PIN CONFIGURATION



FUNCTION TABLE

Inputs			Outputs			
Enable	Select		Y0	Y1	Y2	Y3
$\overline{G}$	B	A				
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	L	H	L	H	L	L
L	H	L	L	L	H	L
L	H	H	L	L	L	H

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS239

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, A or B any Y	t_{PLH}	C_L=50pF	22	30	37	45	ns
	t_{PHL}		22	30	37	45	
Maximum Propagation Delay, $\overline{G}$ to any Y	t_{PLH}		21	8	35	42	ns
	t_{PHL}		22	8	35	42	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}		50				pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

5

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

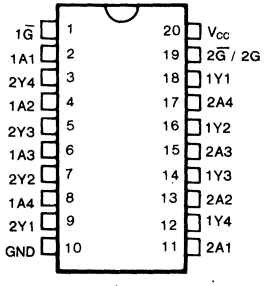
These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The designer has the choice of combinations of inverting/non-inverting outputs and symmetrical complementary input control (both active-low, or one active-low, the other active-high).

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

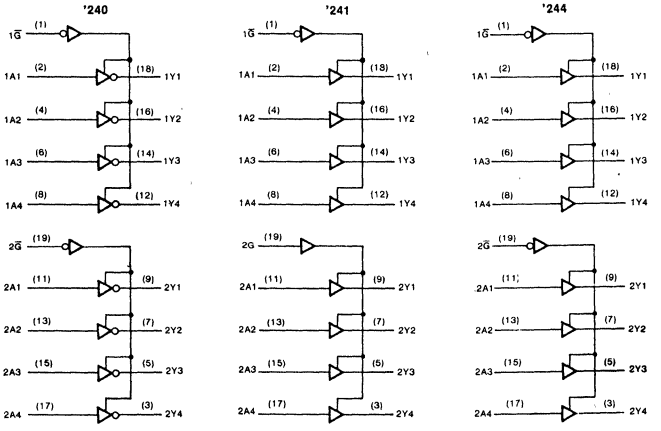
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



*2G̅ for '240 and '244
2G for '241

LOGIC DIAGRAMS



FUNCTION TABLE

Input			'241, '244 Output	'240 Output
G	G̅	A	Y	Y
H	L	L	L	H
H	L	H	H	L
L	H	X	Z	Z

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS240, HCTLS241, HCTLS244

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits				
Maximum Propagation Delay, A to Y	t_{PLH}	$C_L = 50pF$	13	18		22	27	ns
		$C_L = 150pF$	16	21		27	33	
	t_{PHL}	$C_L = 50pF$	13	18		22	27	
		$C_L = 150pF$	16	21		27	33	
Maximum Output Enable Time, Enable to Y	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$	17	23		29	34	ns
		$R_L = 1k\Omega$, $C_L = 150pF$	20	26		34	40	
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$	17	23		29	34	
		$R_L = 1k\Omega$, $C_L = 150pF$	20	26		34	40	
Maximum Output Disable Time, Enable to Y	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	16	21		26	32	ns
	t_{PLZ}		16	21		26	32	
Maximum Input Capacitance	C_{IN}		5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	Output Disabled	5					pF
		Output Enabled	30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS/KS74HCTLS 242/243

Quad Bus Transceivers with 3-State Outputs

Preliminary Specifications

FEATURES

- **2-Way Asynchronous Communication Between Data Buses**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

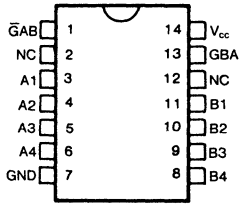
DESCRIPTION

These four-data line transceivers are designed for asynchronous two-way communications between data buses.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

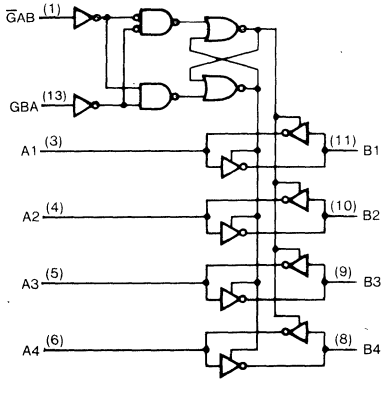


FUNCTION TABLE

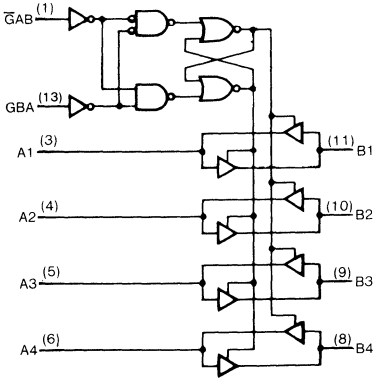
INPUTS		'242	'243
$\overline{G}AB$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	B to A	B to A
H	L	Isolation	Isolation
L	H	Isolation	Isolation

LOGIC DIAGRAMS

'242



'243



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Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS242, HCTLS243

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Propagation Delay, A to B or B to A	t_{PLH}	$C_L = 50pF$		14	18		22	27	ns
		$C_L = 150pF$		17	21		27	33	
	t_{PHL}	$C_L = 50pF$		14	18		22	27	
		$C_L = 150pF$		17	21		27	33	
Maximum Output Enable Time $\overline{G}AB$ to B, GBA to A	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	23	30		38	45	ns
			$C_L = 150pF$	26	33		43	51	
	t_{PZL}		$C_L = 50pF$	23	30		38	45	
			$C_L = 150pF$	26	33		43	51	
Maximum Output Disable Time, $\overline{G}AB$ to B, GBA to A	t_{PHZ}	$R_L = 1k\Omega$		18	25		31	37	ns
	t_{PLZ}	$C_L = 50pF$		18	25		31	37	
Maximum Input Capacitance	C_{IN}			5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	Output Disabled		5					pF
		Output Enabled		30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

5

Octal Bus Transceivers with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-state outputs with high drive current (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

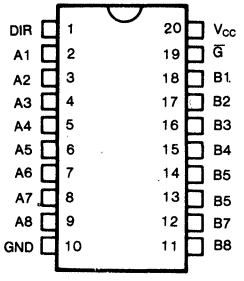
These high-speed octal bus transceivers are designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

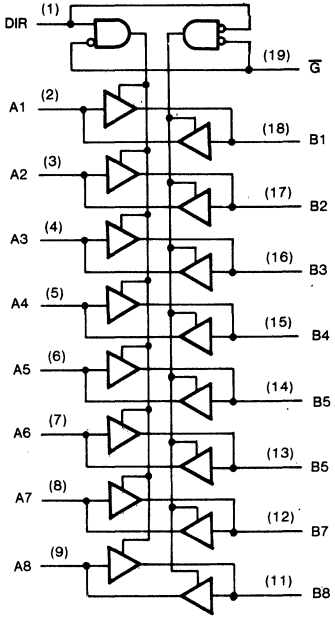
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Operation
$\overline{G}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS245

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Propagation Delay, A to B or B to A	t_{PLH}	$C_L = 50pF$		9	12		15	18	ns
		$C_L = 150pF$		12	15		20	34	
	t_{PHL}	$C_L = 50pF$		9	12		15	18	
		$C_L = 150pF$		12	15		20	34	
Maximum Output Enable Time, $\overline{G}$ to A or B		t_{PZH} $R_L = 1k\Omega$	$C_L = 50pF$	30	40		50	60	ns
			$C_L = 150pF$	33	43		55	66	
	t_{PZL}		$C_L = 50pF$	30	40		50	60	
			$C_L = 150pF$	33	43		55	66	
Maximum Output Disable Time, $\overline{G}$ to A or B	t_{PHZ}	$R_L = 1k\Omega$		18	25		31	37	ns
	t_{PLZ}	$C_L = 50pF$		18	25		31	37	
Maximum Input Capacitance	C_{IN}			5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{G} = V_{CC}$		5					pF
		$\overline{G} = GND$		30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

1-of-8 Data Selectors/Multiplexers with 3-State Outputs

FEATURES

- **Three-State Version of '151**
- **Three-State Outputs Interface Directly with System Bus**
- **Performs Parallel-to-Serial Conversion**
- **Complementary Outputs Provide True and Inverted Data**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

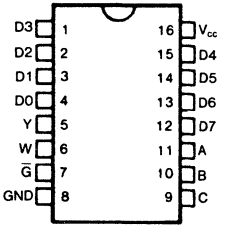
These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ($\overline{G}$). The outputs are disabled when $\overline{G}$ is high.

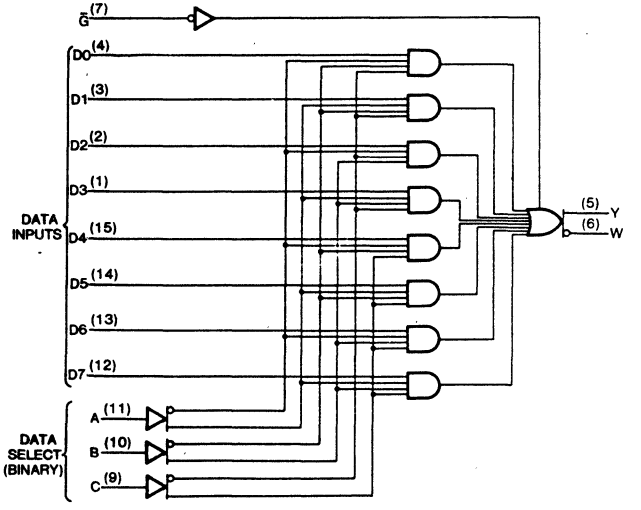
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS251

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Propagation Delay, A, B or C to Y	t_{PLH}	$C_L = 50pF$		20	26		33	40	ns
		$C_L = 150pF$		23	29		38	46	
	t_{PHL}	$C_L = 50pF$		20	26		33	40	
		$C_L = 150pF$		23	29		38	46	
Maximum Propagation Delay, A, B or C to W	t_{PLH}	$C_L = 50pF$		25	34		42	50	ns
		$C_L = 150pF$		28	37		47	56	
	t_{PHL}	$C_L = 50pF$		25	34		42	50	
		$C_L = 150pF$		28	37		47	56	
Maximum Propagation Delay, Any D to Y	t_{PLH}	$C_L = 50pF$		11	15		19	22	ns
		$C_L = 150pF$		14	18		24	28	
	t_{PHL}	$C_L = 50pF$		11	15		19	22	
		$C_L = 150pF$		14	18		24	28	
Maximum Propagation Delay, Any D to W	t_{PLH}	$C_L = 50pF$		17	22		28	33	ns
		$C_L = 150pF$		20	25		33	39	
	t_{PHL}	$C_L = 50pF$		17	22		28	33	
		$C_L = 150pF$		20	25		33	39	
Maximum Output Enable Time, $\overline{G}$ to Y or W	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	24	32		40	48	ns
			$C_L = 150pF$	27	35		45	54	
	t_{PZL}		$C_L = 50pF$	24	32		40	48	
			$C_L = 150pF$	27	35		45	54	
Maximum Output Disable Time, $\overline{G}$ to Y or W	t_{PHZ}	$R_L = 1k\Omega$	$C_L = 50pF$	24	32		40	48	ns
			$C_L = 150pF$	27	35		45	54	
	t_{PLZ}		$C_L = 50pF$	24	32		40	48	
			$C_L = 150pF$	27	35		45	54	
Maximum Input Capacitance	C_{IN}			5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance*	C_{PD}			0					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

5

Dual 1-of-4 Data Selectors/Multiplexers with 3-State Outputs

FEATURES

- **Three-State Version of '153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to—Serial Conversion**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

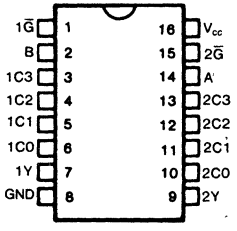
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

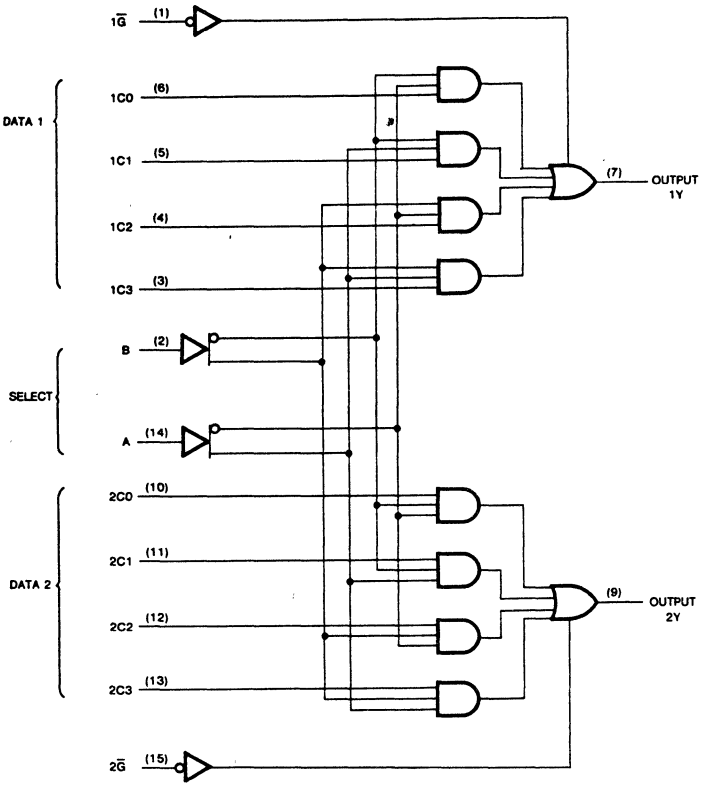


FUNCTION TABLE

SELECT		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS253

Characteristic	Symbol	Conditions†		T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
				Typ	Guaranteed Limits		
Maximum Propagation Delay, A or B to Any Y	t_{PLH}	C_L=50pF		24	32	40	48	ns
		C_L=150pF		27	35	45	54	
	t_{PHL}	C_L=50pF		24	32	40	48	
		C_L=150pF		27	35	45	54	
Maximum Propagation Delay, Data (any C) to any Y	t_{PLH}	C_L=50pF		15	20	25	30	ns
		C_L=150pF		18	23	30	36	
	t_{PHL}	C_L=50pF		15	20	25	30	
		C_L=150pF		18	23	30	36	
Maximum Output Enable Time, $\overline{G}$ to Y	t_{PZH}	R_L=1kΩ	C_L=50pF	17	22	28	33	ns
			C_L=150pF	20	25	33	39	
	t_{PZL}		C_L=50pF	17	22	28	33	
			C_L=150pF	20	25	33	39	
Maximum Output Disable Time, $\overline{G}$ to Y	t_{PHZ}	R_L=1kΩ		17	22	28	33	ns
	t_{PLZ}	C_L=50pF		17	22	28	33	
Maximum Input Capacitance	C_{IN}			5				pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10				pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS/KS74HCTLS 257/258 Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

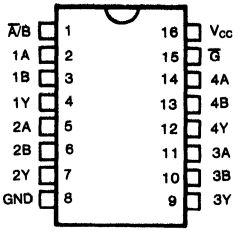
DESCRIPTION

The '257 and '258 multiplex signals from for-bit data sources to four-output data lines in bus organized systems. The data presented at the outputs is non-inverted for the '257 and inverted for the '258.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

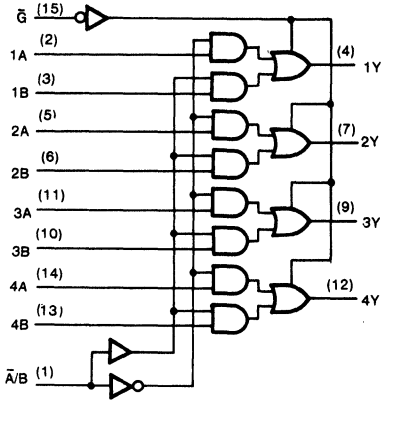


FUNCTION TABLE

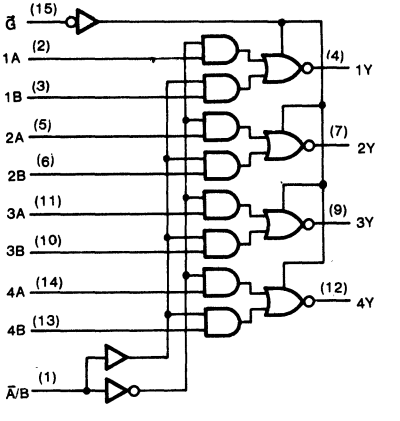
Inputs				Output Y	
Output Control	select	Data		'257	'258
$\overline{G}$	A/B	A	B		
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

LOGIC DIAGRAMS

'257



'258



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS257, HCTLS258

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Propagation Delay, A to B to any Y	t_{PLH}	$C_L = 50pF$		14	18		23	27	ns
		$C_L = 150pF$		17	21		28	33	
	t_{PHL}	$C_L = 50pF$		14	18		23	27	
		$C_L = 150pF$		17	21		28	33	
Maximum Propagation Delay, $\overline{A}$/B to any Y	t_{PLH}	$C_L = 50pF$		16	21		26	31	ns
		$C_L = 150pF$		19	24		31	37	
	t_{PHL}	$C_L = 50pF$		16	21		26	31	
		$C_L = 150pF$		19	24		31	37	
Maximum Output Enable Time, $\overline{G}$ to any Y	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	22	30		37	45	ns
			$C_L = 150pF$	25	33		42	51	
	t_{PZL}		$C_L = 50pF$	22	30		37	45	
			$C_L = 150pF$	25	33		42	51	
Maximum Output Disable Time, $\overline{G}$ to any Y	t_{PHZ}	$R_L = 1k\Omega$		20	27		34	41	ns
	t_{PLZ}	$C_L = 50pF$		20	27		34	41	
Maximum Input Capacitance	C_{IN}			5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance*	C_{PD}								pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

5

FEATURES

- **8-Bit parallel-out storage register performs serial-to-parallel conversion with storage**
- **Asynchronous parallel clear**
- **Active high decoder**
- **Enable/Disable input simplifies expansion**
- **Expandable for N-bit applications**
- **Four distinct functional modes**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '259 is a high-speed addressable latch designed for general purpose storage applications in digital systems. It can be used for implementing working registers, serial-holding registers and active-high decoders or demultiplexers.

The '259 has four distinct modes of operation that are selected via the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs: 1) addressable latch; 2) memory; 3) active-high eight-channel demultiplexer; and 4) clear.

In the addressable latch mode, data on the data input (D) is written into the addressed latch. In this mode, data will be written into the addressed latch with all non-addressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous state and are unaffected by the data of address inputs.

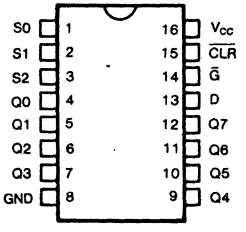
In the demultiplexing mode, addressed outputs will follow the state of the D input and all other outputs will remain low.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

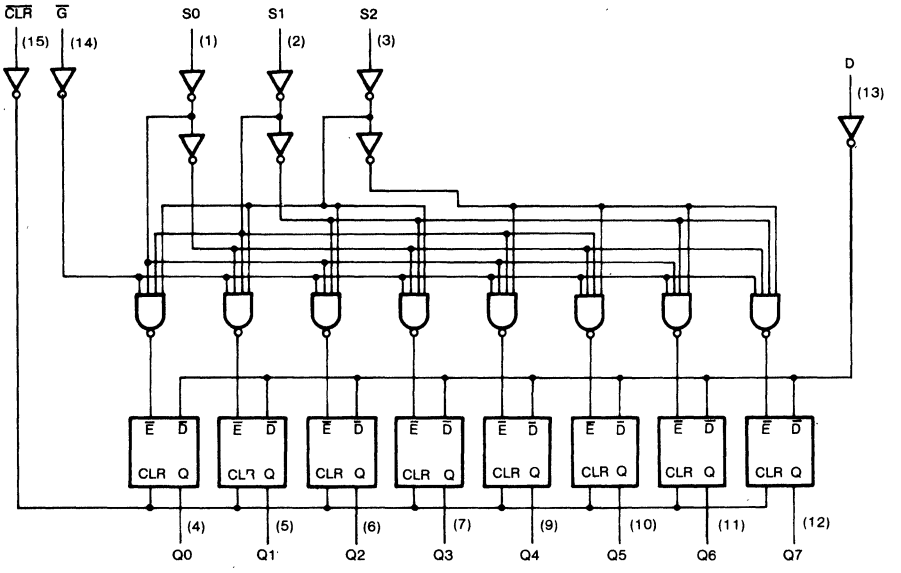
Inputs		Output of Addressed Latch	Each Other Output	Function
$\overline{CLR}$	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

D = the level at the data input.
Q_{i0} = the level of Q_{i0} (i = Q, 1, ... 7, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

Select Inputs			Latch Addressed
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

LOGIC DIAGRAM



5

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS259

Characteristic		Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
				Typ	Guaranteed Limits			
Maximum Propagation Delay $\overline{CLR}$ to any Q		t_{PHL}	C_L=50pF	22	30	37	45	ns
Maximum Propagation Delay, Data to Any Q		t_{PLH}		20	27	34	41	ns
		t_{PHL}		20	27	34	41	
Maximum Propagation Delay, Address to any Q		t_{PLH}		26	34	43	51	ns
		t_{PHL}		26	34	43	51	
Maximum Propagation Delay, $\overline{G}$ to any Q		t_{PLH}		22	30	37	45	ns
		t_{PHL}		22	30	37	45	
Minimum Pulse Width	$\overline{CLR}$ LOW	t_w		8	10	13	15	ns
	$\overline{G}$ Low			8	10	13	15	
Minimum Setup Time, Data or Address before $\overline{G}$↑		t_{su}		8	10	13	15	ns
Minimum Hold Time, Data or Address before $\overline{G}$↑		t_h		−3	0	0	0	ns
Maximum Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}		80				pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

Quad Exclusive-NOR Gates with Open-Drain Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

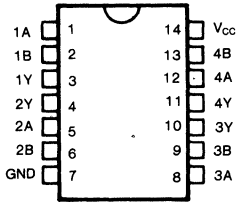
DESCRIPTION

These devices contain four independent exclusive-NOR gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

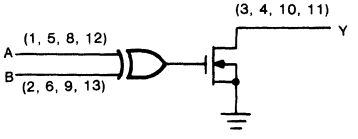
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS266

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74 HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54 HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay	t_{PLH}	C_L=50pF R_L=1kΩ	18	25	31	37	ns
	t_{PHL}		16	22	28	33	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Eight positive-edge-triggered D-type flip-flops with single-rail outputs**
- **Buffered common clock and asynchronous clear**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74HCTLS: −40°C to +85°C KS54HCTLS: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

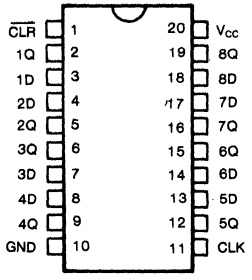
These devices are high-speed octal registers. They consist of eight positive-edge-triggered D-type flip-flops with individual D inputs and Q outputs. All flip flops are loaded and cleared simultaneously by the common buffered clock (CLK) and clear ($\overline{CLR}$) inputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

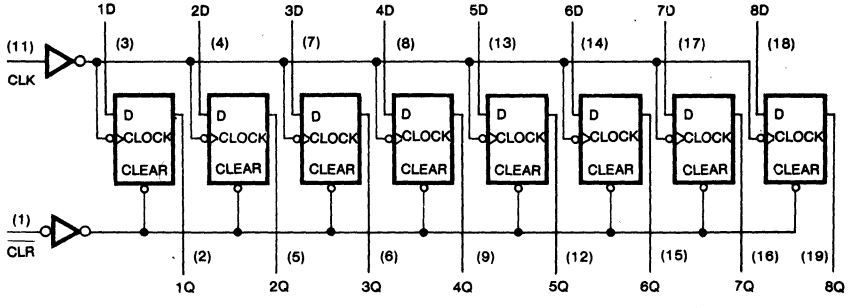


FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS273

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30	25	20	MHz
Maximum Propagation Delay, CLK to any		t_{PLH}	$C_L = 50pF$	20	27	33	40	ns
			$C_L = 150pF$	23	30	38	46	
		t_{PHL}	$C_L = 50pF$	20	27	33	40	
			$C_L = 150pF$	23	30	38	46	
Maximum Propagation Delay, $\overline{CLR}$ to any Q		t_{PHL}	$C_L = 50pF$	20	27	33	40	ns
			$C_L = 150pF$	23	30	38	46	
Minimum Pulse Width	$\overline{CLR}$ Low	t_w		10	13	17	20	ns
	CLK High or Low			10	13	17	20	
Minimum Setup Time before CLK↑	Data	t_{su}		10	13	17	20	ns
	Clear inactive State			13	17	21	25	
Minimum Hold Time, Data after CLK↑		t_h		−3	0	0	0	ns
Maximum Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}	(per package)	150				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

5

FEATURES

- **Generates Odd or Even Parity for Nine Data Lines**
- **Cascadable for N-Bits Parity**
- **Can be used to Upgrade Existing Systems using MSI Parity Circuits**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74HCTLS: −40°C to +85°C KS54HCTLS: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

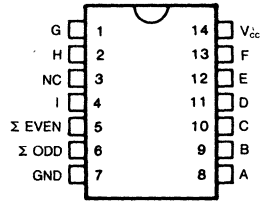
These universal, nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker, Although the '280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the '280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

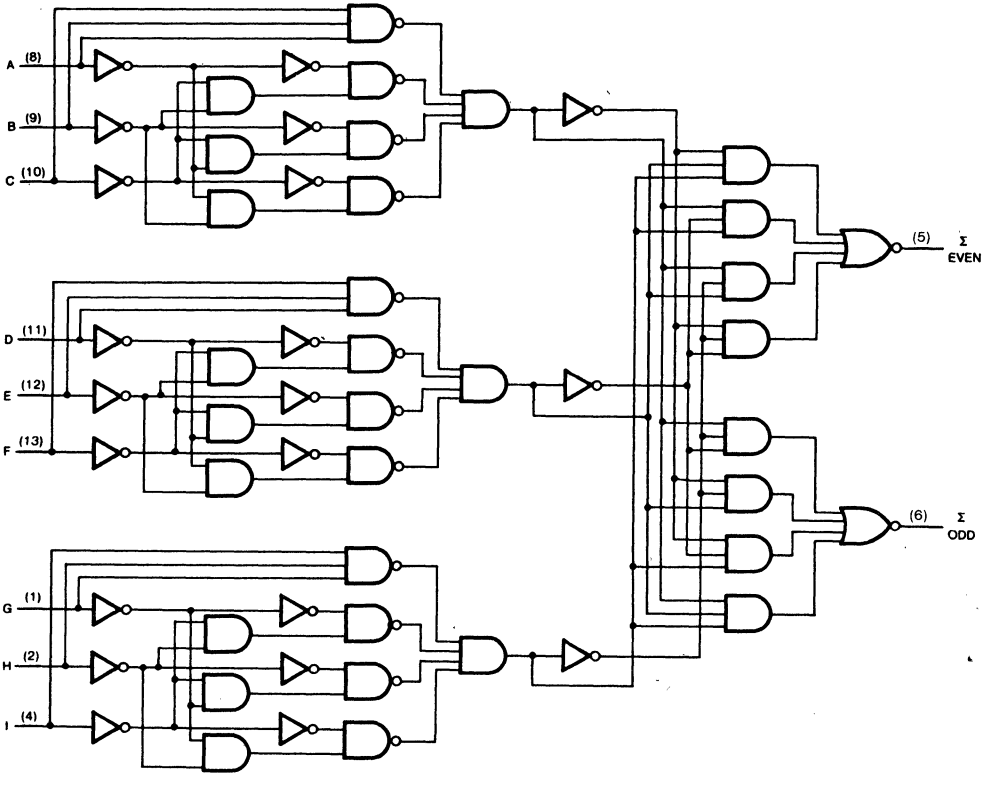
PIN CONFIGURATION



FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,4,5,9	L	H

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

5

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS280

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits		
Maximum Propagation Delay, Any input to Σ Even	PLH	C_L=50pF	30	40	50	60	ns
		C_L=150pF	33	43	55	66	
	t_{PHL}	C_L=50pF	30	40	50	60	
		C_L=150pF	33	43	55	66	
Maximum Propagation Delay, Any input to ΣOdd	t_{PLH}	C_L=50pF	30	40	50	60	ns
		C_L=150pF	33	43	55	66	
	t_{PHL}	C_L=50pF	30	40	50	60	
		C_L=150pF	33	43	55	66	
Minimum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

8-Bit Universal Shift/Storage Registers with 3-State Outputs

FEATURES

- **Multiplexed I/O ports provides improved bit density**
- **Four modes of operation: hold (store), shift, shift left, and load data**
- **Operates with outputs enabled or at high impedance**
- **Can be cascaded for N-bit word lengths**
- **Direct overriding clear**
- **Application:**
  Stacked or push-down registers, buffer storage, and accumulator registers
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with drive current**
  (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

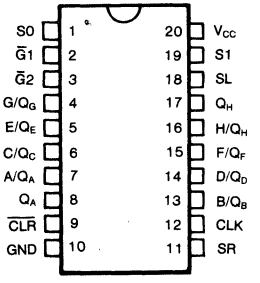
Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when $\overline{CLR}$ is low. Pulling either of the output controls, $\overline{G}1$ or $\overline{G}2$, high disables the outputs but this has no effect on clearing, shifting, or storage of data.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

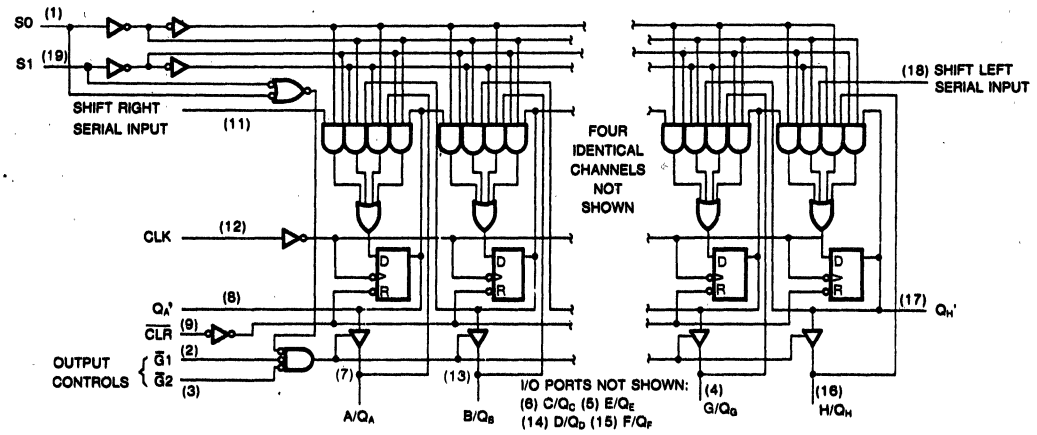
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

5

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

Mode	Inputs							I/O Ports								Outputs	
	$\overline{CLR}$	S1	S0	Output Control $\overline{G1}$	Output Control $\overline{G2}$	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA Q'A and Q'H outputs: I_O=−4mA Q_A thru Q_H outputs: I_O=−6mA	V_{CC} 4.2 4.2	V_{CC} −0.1 3.98 3.84	V_{CC} −0.1 3.84 3.7	V_{CC} −0.1 3.7 —	V
Miximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA Q'A and Q'H outputs: I_O=4mA I_O=8mA Q_A thru Q_H outputs: I_O=12mA I_O=24mA	0 0.26 0.39 0.26 0.39	0.1 0.33 0.5 0.33 0.5	0.1 0.4 — 0.4 —	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable = V_{IN} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS299

Characteristic		Symbol	Conditions†		$T_a=25°C$ $V_{CC}=5.0V$	KS74HCTLS $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54HCTLS $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$		Unit
					Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}			35	25		20		MHz
Maximum Propagation Delay, CLK to Q'_A or Q'_H		t_{PLH}	$C_L=50pF$		26	35		4	53	ns
		t_{PHL}			26	35		44	53	
Maximum Propagation Delay, $\overline{CLR}$ to Q'_A or Q'_H		t_{PHL}			30	40		50	60	ns
Maximum Propagation Delay, CLK to Q_A thru Q_H		t_{PLH}	$C_L=50pF$		24	32		40	48	ns
			$C_L=150pF$		27	35		45	54	
		t_{PHL}	$C_L=50pF$		24	32		40	48	
			$C_L=150pF$		27	35		45	54	
Maximum Propagation Delay, $\overline{CLR}$ to Q_a thru Q_H		t_{PHL}	$C_L=50pF$		30	40		50	60	ns
			$C_L=150pF$		33	43		55	66	
Maximum Output Enable Time, $\overline{G1}$, $\overline{G2}$, to Q_A thru Q_H		t_{PZH}	$R_L=1k\Omega$	$C_L=50pF$	20	26		33	39	ns
				$C_L=150pF$	23	29		38	45	
		t_{PZL}		$C_L=50pF$	20	26		33	39	
				$C_L=150pF$	23	29		38	45	
Maximum Output Disable Time, $\overline{G1}$, $\overline{G2}$ to Q_A thru Q_H		t_{PHZ}	$R_L=1k\Omega$ $C_L=50pF$		13	17		21	26	ns
		t_{PLZ}			13	17		21	26	
Minimum Pulse Width	CLK High or Low	t_w			10	13		17	20	ns
	$\overline{CLR}$ Low				10	13		17	20	
Minimum Setup time before CLK↑	S0 and S1	t_{su}			13	17		21	25	ns
	High-Level Inputs				10	13		17	20	
	High-Level Inputs				10	13		17	20	
	$\overline{CLR}$ Inactive				10	13		17	20	
Minimum Hold Time after CLK↑	S0 and S1	t_h			5	7		8	10	ns
	All Inputs				−3	0		0	0	
Maximum Input Capacitance		C_{IN}				5				pF
Maximum Output Capacitance		C_{OUT}	Output Disabled			10				pF
Power Dissipation Capacitance*		C_{PD}								pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Dual 4-Line to 1-Line Data Selectors/Multiplexers

FEATURES

- **Inverting Version of '153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74AHCT: −40°C to +85°C KS54AHCT: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

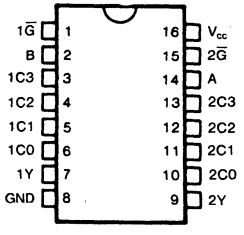
DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\bar{G}$) are provided for each of the two four-line sections.

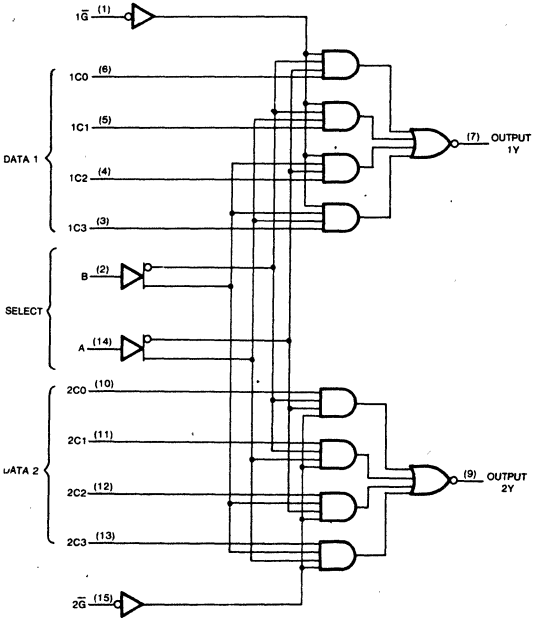
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

SELECT		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\bar{G}$	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS352

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, A or B to Y	t_{PLH}	$C_L = 50pF$	23	30	38	45	ns
		$C_L = 150pF$	26	33	43	51	
	t_{PHL}	$C_L = 50pF$	23	30	38	45	
		$C_L = 150pF$	26	33	43	51	
Maximum Propagation Delay, Data (Any C) to Y	t_{PLH}	$C_L = 50pF$	19	26	32	39	ns
		$C_L = 150pF$	21	29	37	45	
	t_{PHL}	$C_L = 50pF$	19	26	32	39	
		$C_L = 150pF$	21	29	37	45	
Maximum Propagation Delay, $\overline{G}$ to Y	t_{PLH}	$C_L = 50pF$	19	26	32	39	ns
		$C_L = 150pF$	21	29	37	45	
	t_{PHL}	$C_L = 50pF$	19	26	32	39	
		$C_L = 150pF$	21	29	37	45	
Maximum Input Capacitance	C_{IN}			5			pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

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KS54HCTLS 353
KS74HCTLS 353

Dual 1-of-4 Data Selectors/Multiplexers with 3-State Outputs

FEATURES

- **Inverting Version of '253**
- **Permits Multiplexing from N lines to 1 line**
- **Performs Parallel-to-Serial Conversion**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

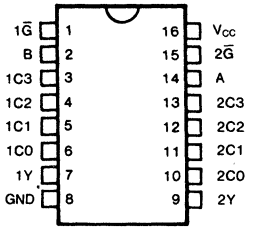
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

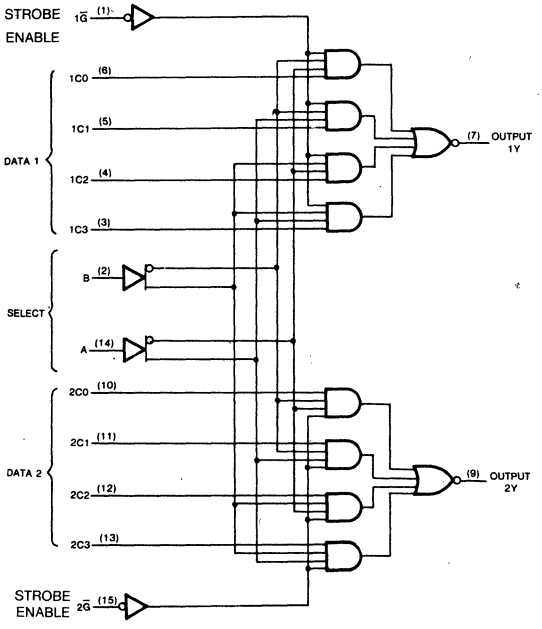


FUNCTION TABLE

SELECT		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA =−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS353

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits		
Maximum Propagation Delay, A or B to Any Y	t_{PLH}	$C_L = 50pF$	24	32	40	48	ns
		$C_L = 150pF$	27	35	45	54	
	t_{PHL}	$C_L = 50pF$	24	32	40	48	
		$C_L = 150pF$	27	35	45	54	
Maximum Propagation Delay, Data (any C) to any Y	t_{PLH}	$C_L = 50pF$	15	20	25	30	ns
		$C_L = 150pF$	18	23	30	36	
	t_{PHL}	$C_L = 50pF$	15	20	26	31	
		$C_L = 150pF$	18	23	31	37	
Maximum Output Enable Time, $\overline{G}$ to Y	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$	17	23	29	35	ns
		$R_L = 1k\Omega$, $C_L = 150pF$	20	26	34	41	
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$	17	23	29	35	
		$R_L = 1k\Omega$, $C_L = 150pF$	20	26	34	41	
Maximum Output Disable Time, $\overline{G}$ to Y	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	20	27	34	41	ns
	t_{PLZ}		20	27	34	41	
Maximum Input Capacitance	C_{IN}		5				pF
Maximum Output Capacitance	C_{OUT}		10				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

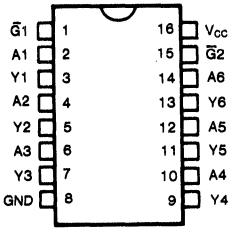
These high-speed Hex bus drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus oriented receivers and transmitters.

The '365 and '366 have two output enables ($\overline{G}1$ and $\overline{G}2$) NOR'ed together to control all six gates. The '367 and '368 have two output enables which are configured so that one enable ($\overline{G}1$) controls four gates and the other ($\overline{G}2$) controls the remaining two gates. The '366 and '368 have inverting data paths. The '365 and '367 have noninverting data paths.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLES

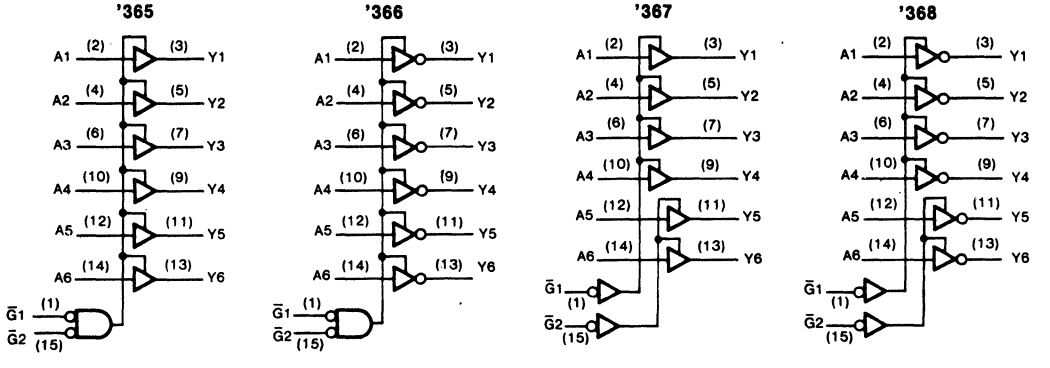
'365 and '366

Inputs			Y Outputs	
$\overline{G}1$	$\overline{G}2$	A	'365	'366
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

'367 and '368

Inputs		Y Outputs	
$\overline{G}1$ & $\overline{G}2$	A	'367	'368
L	L	L	H
L	H	H	L
H	X	Z	Z

LOGIC DIAGRAMS



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$*		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS365A, HCTLS367A

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Propagation Delay, A to Y	t_{PLH}	$C_L = 50pF$		14	19	24	28	ns
		$C_L = 150pF$		17	22	29	34	
	t_{PHL}	$C_L = 50pF$		14	19	24	28	
		$C_L = 150pF$		17	22	29	34	
Maximum Output Enable Time, $\overline{G}$ to Y	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	26	35	44	52	ns
			$C_L = 150pF$	29	38	49	58	
	t_{PZL}		$C_L = 50pF$	26	35	44	52	
			$C_L = 150pF$	29	38	49	58	
Maximum Output Disable Time, $\overline{G}$ to Y	t_{PHZ}	$R_L = 1k\Omega$		26	35	44	52	ns
	t_{PLZ}	$C_L = 50pF$		26	35	44	52	
Maximum Input Capacitance	C_{IN}			5				pF
Maximum Output Capacitance	C_{OUT}	Output disabled		10				pF
Power Dissipation Capacitance* (per driver)	C_{PD}	$\overline{G} = V_{CC}$		5				pF
		$\overline{G} = GND$		30				

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS366A, HCTLS368A

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Propagation Delay, A to Y	t_{PLH}	$C_L = 50pF$		13	17	21	25	ns
		$C_L = 150pF$		16	20	26	31	
	t_{PHL}	$C_L = 50pF$		13	17	21	25	
		$C_L = 150pF$		16	20	26	31	
Maximum Output Enable Time, $\overline{G}$ to Y	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	26	35	44	52	ns
			$C_L = 150pF$	29	38	49	58	
	t_{PZL}		$C_L = 50pF$	26	35	44	52	
			$C_L = 150pF$	29	38	49	58	
Maximum Output Disable Time, $\overline{G}$ to Y	t_{PHZ}	$R_L = 1k\Omega$		26	35	44	52	ns
	t_{PLZ}	$C_L = 50pF$		26	35	44	52	
Maximum Input Capacitance	C_{IN}			5				pF
Maximum Output Capacitance	C_{OUT}	Output disabled		10				pF
Power Dissipation Capacitance* (per driver)	C_{PD}	$\overline{G} = V_{CC}$		5				pF
		$\overline{G} = GND$		30				

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

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FEATURES

- **8 latches in a single package**
- **Full parallel access for loading**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '373 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

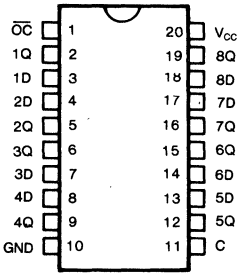
The latches are transparent: when the enable (C) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs at a high-impedance state when it is taken high. The $\overline{OC}$ signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

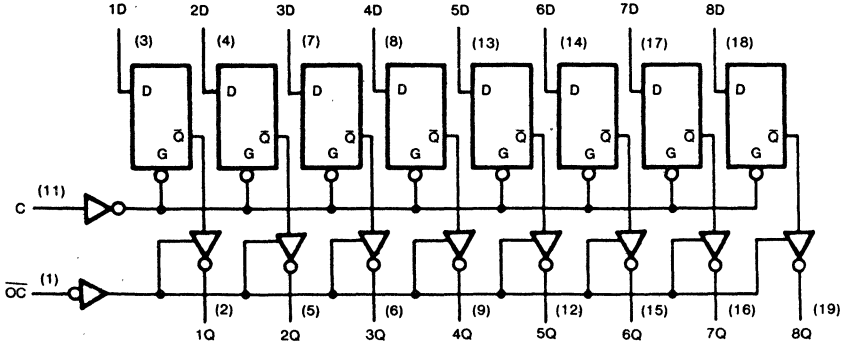


FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	Enable C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} . . . . . −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_A=25°C	KS74HCTLS T_A=−40°C to +85°C	KS54HCTLS T_A=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_Z=2.4V Other Inputs: At V_{CC} or GND I_O=0		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS373

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Propagation Delay, D to Q	t_{PLH}	$C_L = 50pF$		14	18	23	27	ns
		$C_L = 150pF$		17	21	28	33	
	t_{PHL}	$C_L = 50pF$		14	18	23	27	
		$C_L = 150pF$		17	21	28	33	
Maximum Propagation Delay, C to any Q	t_{PLH}	$C_L = 50pF$		22	30	37	45	ns
		$C_L = 150pF$		25	33	42	51	
	t_{PHL}	$C_L = 50pF$		22	30	37	45	
		$C_L = 150pF$		25	33	42	51	
Maximum Output Enable Time, $\overline{OC}$ to any Q	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	24	32	40	48	ns
			$C_L = 150pF$	27	35	45	54	
	t_{PZL}		$C_L = 50pF$	24	32	40	48	
			$C_L = 150pF$	27	35	45	54	
Maximum Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	$R_L = 1k\Omega$ $C_L = 50pF$		19	25	31	37	ns
	t_{PLZ}			19	25	31	37	
Minimum Pulse Width, C High	t_w			6	10	12	15	ns
Minimum Setup Time, D before C↓	t_{su}			2	3	4	5	ns
Minimum Hold Time, D after C↓	t_h			6	10	12	15	ns
Maximum Input Capacitance	C_{IN}			5				pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10				pF
Power Dissipation Capacitance* (per latch)	C_{PD}	$\overline{OC} = V_{CC}$		5				pF
		$\overline{OC} = GND$		30				

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '374 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

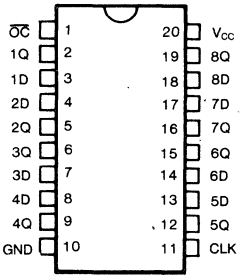
The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs at a high-impedance state when it is taken high. The $\overline{OC}$ signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

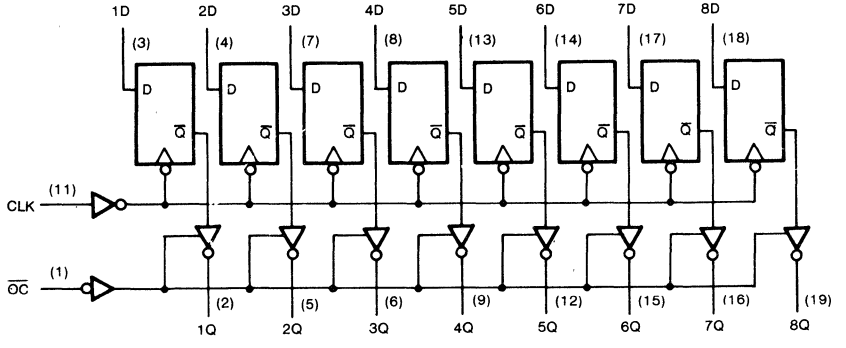


FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	 V_{CC} 4.2	 V_{CC} −0.1 3.98	 V_{CC} −0.1 3.84	 V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	 0	 0.1 0.26 0.39	 0.1 0.33 0.5	 0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS374

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Operating Frequency	f_{max}	$C_L = 50pF$		45	35		30	25	MHz
Maximum Propagation Delay, CLK to any Q	t_{PLH}	$C_L = 50pF$		21	28		35	42	ns
		$C_L = 150pF$		24	31		40	48	
	t_{PHL}	$C_L = 50pF$		21	28		35	42	
		$C_L = 150pF$		24	31		40	48	
Maximum Output Disable Time, $\overline{OC}$ to any Q	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	21	28		35	42	ns
			$C_L = 150pF$	24	31		40	48	
	t_{PZL}		$C_L = 50pF$	21	28		35	42	
			$C_L = 150pF$	24	31		40	48	
Maximum Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	$R_L = 1k\Omega$		19	25		31	37	ns
	t_{PLZ}	$C_L = 50pF$		19	25		31	37	
Minimum Pulse Width, CLK High or Low	t_w			7	10		12	15	ns
Minimum Setup Time, D before CLK↑	t_{su}			10	13		17	20	ns
Minimum Hold Time, D after CLK↑	t_h			−3	0		0	0	ns
Maximum Input Capacitance	C_{IN}			5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC} = V_{CC}$		5					pF
		$\overline{OC} = GND$		30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

Octal D-Type Flip-Flops with Clock Enable

FEATURES

- **Can be used for implementing**
  - **— Buffer/Storage Registers**
  - **— Shift Registers**
  - **— Pattern Generators**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

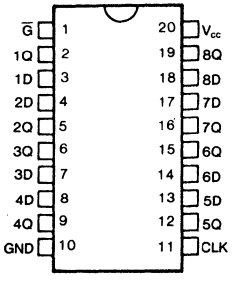
The '377 contains eight positive-edge-triggered D-type flip-flops with an enable input. This part is similar to '273 but features a latched clock enable ($\overline{G}$) instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitioins at the $\overline{G}$ input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

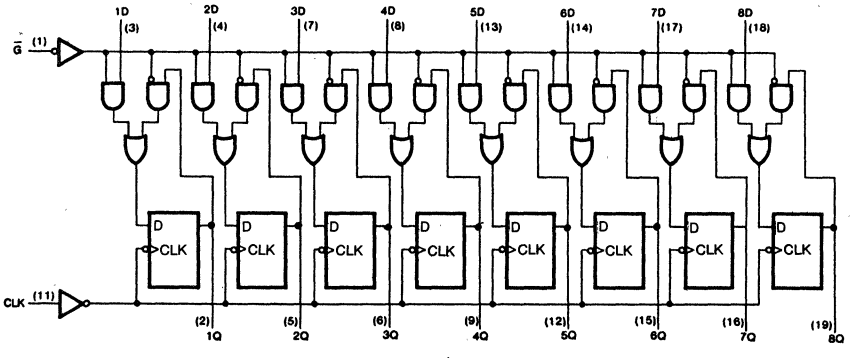


FUNCTION TABLE

(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{G}$	CLK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS377

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}		45	35	30	25	MHz
Maximum Propagation Delay, CLK to Any Q		t_{PLH}	$C_L = 50pF$	18	27	32	38	ns
		t_{PHL}		18	27	32	38	
Minimum Pulse Width	$\overline{G}$ Low	t_w		12	16	20	25	ns
	CLK high or Low			12	16	20	25	
Minimum Setup Time before CLK†	Data	t_{su}		6	10	15	20	ns
	$\overline{G}$ high or LOW			15	20	25	25	
Minimum Hold Time, Data after CLK†		t_h		−3	0	0	0	ns
Maximum Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}						pF

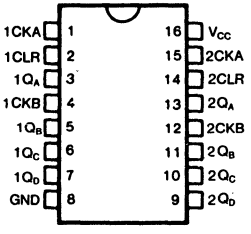
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Individual clock for A and B flip-flops provide dual ÷2 and ÷5 counters**
- **Direct clear for each 4-bit counter**
- **Significant provement in system density through reduced counter package count.**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These devices incorporate dual divide-by-two and divide-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiple of 2 and/or 5 up to divide-by-100. When conneoted as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square ware) at the final outpur stage. The '390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-tow circuit can be used to provide symmetry (a square wave) at the final outpur stage. The '390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

BCD COUNT SEQUENCE
(Each Counter)
(See Note A)

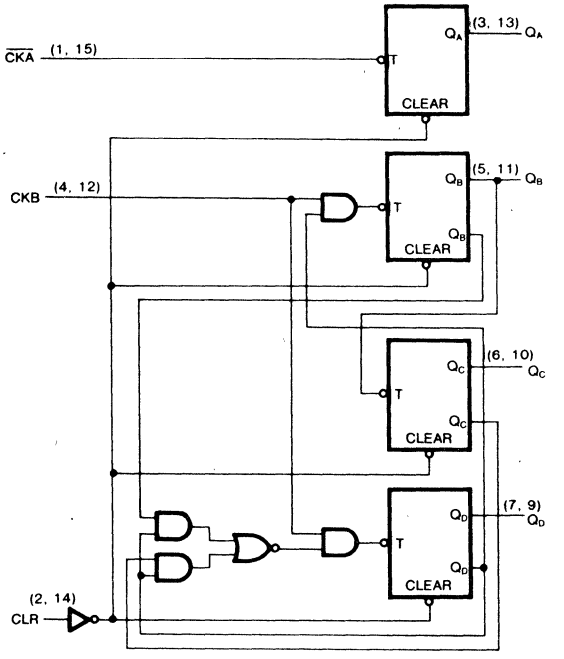
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BIQUINARY (5-2)
(Each Counter)
(See Note B)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKA for biquinary count.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} . . . . . −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS390

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits		
Maximum Clock Frequency CKA to Q_A or CKB to Q_B	f_{max}	C_L=50pF	35	25	20	20	MHz
Maximum Propagation Delay, CKA to Q_A	t_{PLH}		15	20	25	30	ns
	t_{PHL}		15	20	25	30	
Maximum Propagation Delay, CKA to Q_C	t_{PLH}		36	48	60	72	ns
	t_{PHL}		36	48	60	72	
Maximum Propagation Delay, CKB to Q_B	t_{PLH}		16	21	26	31	ns
	t_{PHL}		16	21	26	31	
Maximum Propagation Delay, CKB to Q_C	t_{PLH}		24	32	40	48	ns
	t_{PHL}		24	32	40	48	
Maximum Propagation Delay, CKB to Q_D	t_{PLH}		16	21	26	31	ns
	t_{PHL}		16	21	26	31	
Maximum Propagation Delay, CLR to Any Q	t_{PHL}		24	32	40	48	ns
Minimum Pulse Width: CKA or CKB high or low	t_{su}		12	16	20	24	ns
Minimum Pulse Width: CLR high	t_{su}		12	16	20	24	ns
Minimum Setup Time, CLR inactive before CKA or CKB	t_{su}		15	20	25	30	ns
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capocitance	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

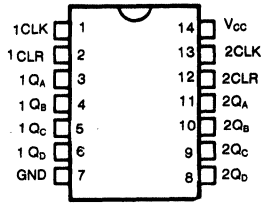
DESCRIPTION

The '393 consists of two independent 4-bit binary counters each with its own clear and clock inputs. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. Parallel outputs from each counter stage provide any submultiple of the input count frequency for system timing signals.

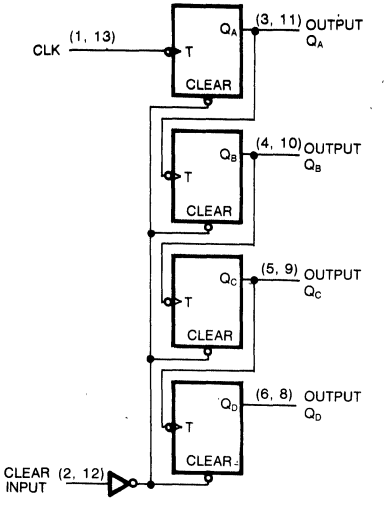
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

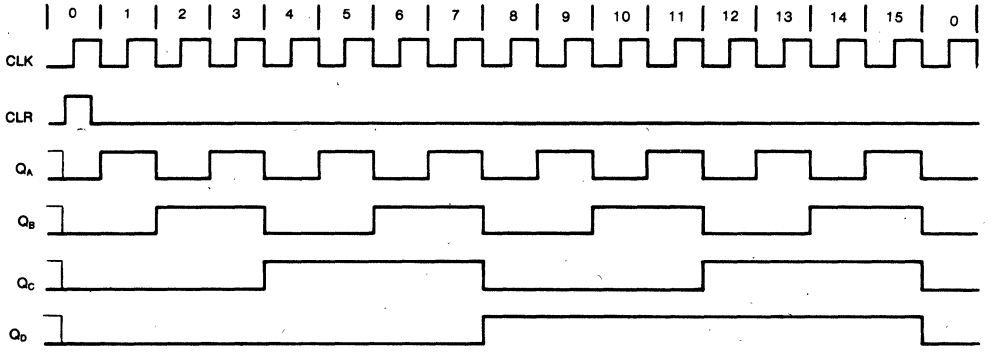
PIN CONFIGURATION



LOGIC DIAGRAMS



LOGIC TIMING WAVEFORMS



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS393

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	40	30	25	20	MHz
Maximum Propagation Delay, A to Q_A		t_{PLH}		15	20	25	30	ns
		t_{PHL}		15	20	25	30	
Maximum Propagation Delay, A to Q_B		t_{PLH}		26	35	44	53	ns
		t_{PHL}		26	35	44	53	
Maximum Propagation Delay, A to Q_C		t_{PLH}		34	45	56	67	ns
		t_{PHL}		34	45	56	67	
Maximum Propagation Delay, A to Q_D		t_{PLH}		45	60	75	90	ns
		t_{PHL}		45	60	75	90	
Maximum Propagation Delay, CLR to any Q		t_{PHL}		29	39	49	58	ns
Minimum Pulse Width	A Input High or Low	t_w		10	13	17	20	ns
	CLR High			10	13	17	20	
Minimum Hold Time, CLR Inactive before A		t_{su}		10	13	17	20	ns
Maximum Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}	(per counter)	40				pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

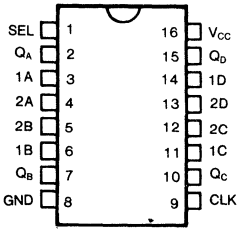
DESCRIPTION

These are high-speed quad 2-port registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A common select input (SEL) selects between two 4-bit input ports. The selected data is transferred to the output register on the low-to-high transition of the clock input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Output
SEL	**Port 1**	**Port 2**	**Q**
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

l = Low Voltage Level one setup time prior to the low-to-high clock transition
h = High Voltage Level one setup time prior to the low-to-high clock transition

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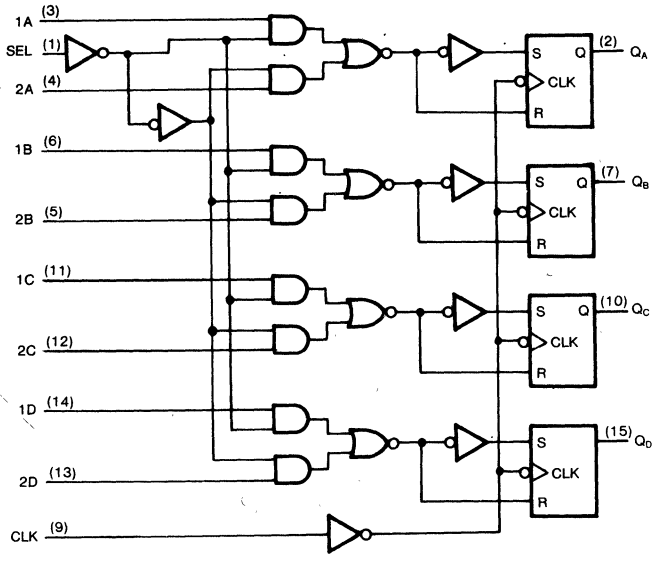
LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS399

Characteristic		Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
				Typ	Guaranteed Limits			
Propagation Delay, CLK to Q or $\overline{Q}$		t_{PLH}	C_L=50pF	22	30	37	45	ns
		t_{PHL}		22	30	37	45	
Minimum Pulse Width, CLK High or Low		t_w		10	13	17	20	ns
Minimum Setup Time before CLK↑	Data	t_{su}		10	13	17	20	ns
	Word Select			10	13	17	20	
Minimum Hold Time after CLK↑	Data	t_h		−3	0	0	0	ns
	Word Select			−3	0	0	0	
Maximum Input Capacitance		C_{IN}		5				pF
Power Dissipation Capacitance*		C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

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FEATURES

- **Simple pulse width formula $t_W = 0.45RC$**
- **DC triggered from active HIGH or active Low inputs**
- **Retriggerable for very long output pulses up to 100% duty cycle**
- **Overriding clear terminates output pulse**
- **Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs**
- **Functions, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High drive current outputs: $I_{OL} = 8mA$ @ $V_{OL} = 0.5V$**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range; 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74HCTLS: −40°C to +85°C KS54HCTLS: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '423 contains dual retriggerable monostable multivibrators with output pulsewidth control by two methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low-going edge input (Ai) or the active High-going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH, $n\overline{Q}$=LOW) can be made as long as desired.

Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques.

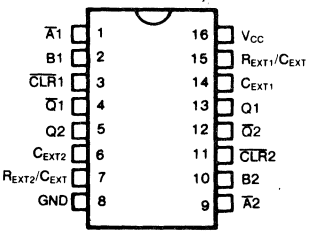
The output pulse equation is simply;

$t_W = 0.45 \times R_{EXT} \times C_{EXT}$(typ).

Where t_w is in seconds. R is in ohm. and C is in fards.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Outputs	
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

H= HIGH voltage level
L= LOW voltage level
X= don't care
↑= LOW to HIGH transition
↓= HIGH to LOW transition
⎍= one HIGH level output pulse
⎎= one LOW level output pulse

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I<−0.5V or V_I>V_{CC}+0.5V) ..... ±20 mA
DC Output Diode Current, I_{Ok}
(V_O<−0.5V or V_O>V_{CC}+0.5V) ..... ±20 mA
Continuous OUtput Current Per Pin, I_O
(−0.5V<V_O<V_{CC}+0.5V) ..... ±35 mA
Continuous Current Through
V_{CC} or GND pins ..... ±125 mA
Storage Temperature Range, T_{stg} −65°C to +150°C
Power Dissipation Per Package, P_d† ..... 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package(N): −12mW/°C from 65°C to 85°C
Ceramic Package(J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} ..... 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f ..... Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

5

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS423

Characteristic	Symbol	Conditions†	$T_a=25°C$ $V_{CC}=5.0V$	KS74AHCTLS $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54AHCTLS $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits				
Propagation Delay	t_{PLH}	$C_L=50pF$ $C_{ext}=0$, $R_{ext}=5k\Omega$	23	33	41	50		ns
$\overline{A}$, B to Q, $\overline{Q}$	t_{PHL}		23	33	41	50		
Propagation Delay	t_{PLH}		20	27	34	41		ns
$\overline{CLR}$ to Q, $\overline{Q}$	t_{PHL}		20	27	34	41		
Output Pulse Width 1	t_{WQ1}		116	200	207	209		ns
Output Pulse Width 2	t_{WQ2}	$C_L=50pF$ $C_{ext}=1000pF$ $R_{ext}=10k\Omega$	4.5	4.0 5.0	3.8(min) 5.2(max)	2.7(min) 7.5(max)		μs
Trigger Pulse Width	t_w	$C_L=50pF$ A_i=LOW	7	20	25	30		ns
Trigger Pulse Width	t_w	$C_L=50pF$ B_i=High	7	20	25	30		ns
Clear Pulse Width	t_w	$C_L=50pF$ CLR_i=LOW	8	20	25	30		ns
External Timing Resistance	R_{ext}			2 1000	2(min) 1000(max)	2(min) 1000(max)		kΩ
External Timing Capacitance	C_{in}		no restriction					
Input Capacitance	C_{in}		5					pF
Power Dissipation Capacitance	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Application Information

The basic output pulse width is determined by the value of external capacitance and timing resistance.
For output pulse widths greater than 100μs or external capacitance greater than 1000pF the following equation should be used.

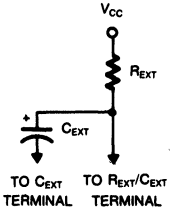
$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

t_w is in second
K is the multiplying factor
and is approximately 0.45 for
$C_{ext} \geq 1000pF$
C_{ext} is in F

For best results, system ground should be applied to the C_{ext} terminal. These devices do not require a switching diode in series with the R_{ext}/C_{ext} terminal (as required by some other monostable multivibrators)

TIMING COMPONENT



Octal Buffers and Line Drivers with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

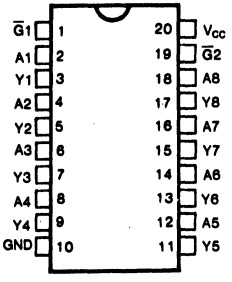
These high-speed octal buffers and drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has the choice of inverting/noninverting outputs and various types of output controls.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

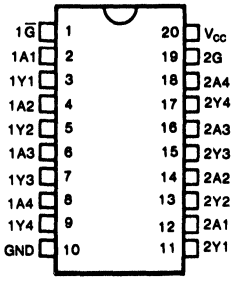
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS

'465 and '466



'467 and '468



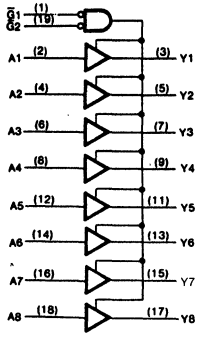
FUNCTION TABLE

Input			Output	
$\overline{G}_1$	$\overline{G}_2$	A	'465	'466
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

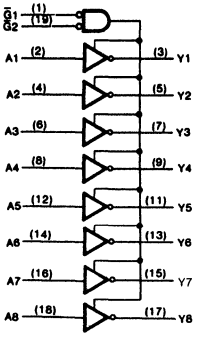
Input			Output	
G	$\overline{G}$	A	'467	'468
H	L	L	L	H
H	L	H	H	L
L	H	X	Z	Z

LOGIC DIAGRAMS

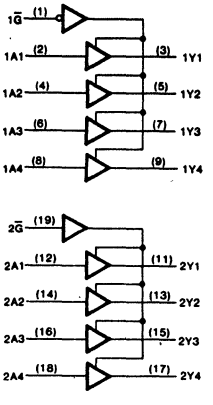
'465



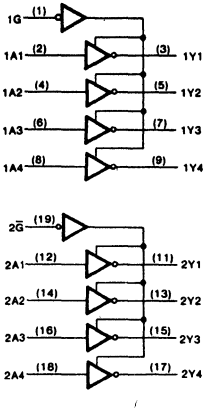
'466



'467



'468



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O= −6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS465, HCTLS466, HCTLS467, HCTLS468

Characteristic	Symbol	Conditions		54/74ACHT $T_a=25°C$ $V_{CC}=5V$	KS74HCTLS $T_a=-40°C$ to $+85°C$ $V_{CC}=5V\pm10\%$		54HCTLS $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V\pm10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Propagation Delay, A to Y	t_{PLH}	$C_L=50pF$		11	15	19	22	ns
		$C_L=150pF$		14	18	24	28	
	t_{PHL}	$C_L=50pF$		11	15	19	22	
		$C_L=150pF$		14	18	24	28	
Maximum Output Enable Time, Enable to Y	t_{PZH}	$R_L=1k\Omega$	$C_L=50pF$	24	32	40	48	ns
			$C_L=150pF$	27	35	45	54	
	t_{PZL}		$C_L=50pF$	24	32	40	48	
			$C_L=150pF$	27	35	45	54	
Maximum Output disable Time, Enable to Y	t_{PHZ}	$R_L=1k\Omega$		24	32	40	48	ns
	t_{PLZ}	$C_L=50pF$		24	32	40	48	
Maximum Input Capacitance	C_{IN}			4				pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10				pF
Power Dissipation Capacitance* (per stage)	C_{PD}	Output Disabled		5				pF
		Output Enabled		30				

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD}\,V_{CC}^2\,f + I_{CC}\,V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

5

FEATURES

- **Compares two 8-bit words**
- **'518, '520 and '522 have 20KΩ Pull-up resistors on Q inputs**

TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
'518	Yes	P=Q open-drain
'519	No	P=Q open-drain
'520	Yes	$\overline{P=Q}$ totem-pole
'521	No	$\overline{P=Q}$ totem-pole
'522	Yes	$\overline{P=Q}$ open-drain

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

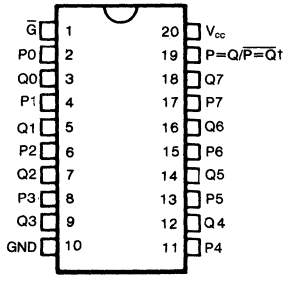
DESCRIPTION

These identity comparators perform comparisons on two eight-bit binary or BCD words. The '518 and '519 provide P=Q outputs, while the '520, '521, and '522 provide $\overline{P=Q}$ outputs. The '518, '519, and '522 have open-drain outputs. The '518, '520, and '522 feature 20-kΩ inputs for analog or switch data.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



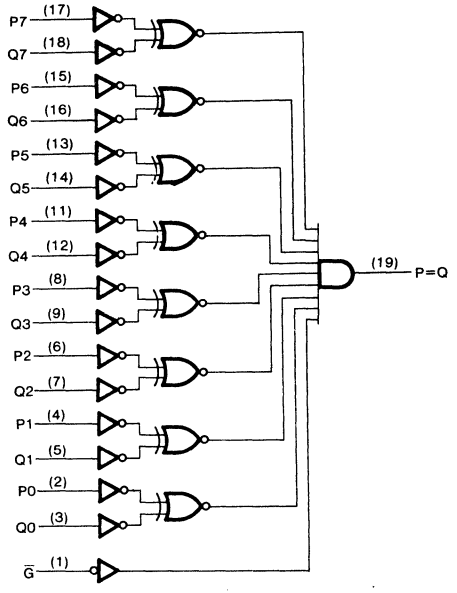
† P=Q for '518 and '519; $\overline{P=Q}$ for '520, '521, '522.

FUNCTION TABLE

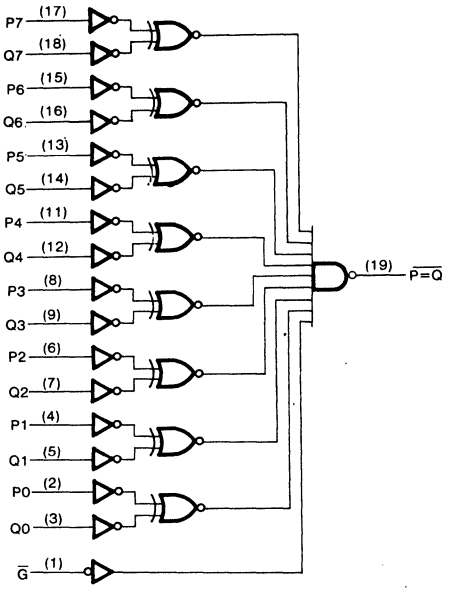
INPUTS		OUTPUTS	
DATA P, Q	ENABLE $\overline{G}$	P=Q	$\overline{P=Q}$
P=Q	L	H	L
P>Q	L	L	H
P<Q	L	L	H
X	H	L	H

LOGIC DIAGRAMS

'518/'519



'520/'521/'522



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Parameter	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_A=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (Totem-pole Outputs)	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.93	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage (All Outputs)	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current, ('518, '520 and '522 Q input)		V_{CC}=Max V_{IN}=2.7V V_{IN}=0.4V		−0.2 −0.6	−0.2 −0.6	−0.2 −0.6	mA
Maximum Input Current (All other Inputs)	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current (Open-Drain Outputs)	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	For '518, '520 and '522: V_{IN}=GND (Q0-Q7) V_{IN}=V_{CC} or GND (all other inputs)		3.5	3.5	3.5	mA
		For '519 and '521: V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS518, HCTLS519

Characteristic	Symbol	Conditions	54/74ACHT $T_a = 25°C$ $V_{CC} = 5V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5V \pm 10\%$	54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, from P or Q to P=Q	t_{PLH}	C_L=50pF	26	33	40	47	ns
		C_L=150pF	29	36	45	53	
	t_{PHL}	C_L=50pF	21	28	35	42	
		C_L=150pF	24	31	40	48	
Maximum Propagation Delay, from $\overline{G}$ to P=Q	t_{PLH}	C=50pF	23	29	35	41	ns
		C_L=150pF	26	32	40	47	
	t_{PHL}	C_L=50pF	18	24	30	36	
		C_L=150pF	21	27	35	42	
Maximum Input Capacitance	C_{IN}		5				pF
Maximum Output Capacitance	C_{OUT}						pF
Power Dissipation Capacitance*	C_{PD}						pF

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS520, HCTLS521

Characteristic	Symbol	Conditions	54/74ACHT $T_a = 25°C$ $V_{CC} = 5V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5V \pm 10\%$	54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, from P or Q to $\overline{P=Q}$	t_{PLH}	C_L=50pF	12	22	28	33	ns
		C_L=150pF	15	25	33	39	
	t_{PHL}	C_L=50pF	16	22	28	33	
		C_L=150pF	19	25	33	39	
Maximum Propagation Delay, from $\overline{G}$ to $\overline{P=Q}$	t_{PLH}	C=50pF	15	20	25	30	ns
		C_L=150pF	18	23	30	36	
	t_{PHL}	C_L=50pF	15	20	25	30	
		C_L=150pF	18	23	30	36	
Maximum Input Capacitance	C_{IN}		5				pF
Maximum Output Capacitance	C_{OUT}						pF
Power Dissipation Capacitance*	C_{PD}						pF

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS522

Characteristic	Symbol	Conditions	54/74ACHT $T_a = 25°C$ $V_{CC} = 5V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5V \pm 10\%$	54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, from P or Q to $\overline{P=Q}$	t_{PLH}	C_L=50pF	24	31	37	43	ns
		C_L=150pF	27	34	42	49	
	t_{PHL}	C_L=50pF	19	26	32	38	
		C_L=150pF	22	29	37	44	
Maximum Propagation Delay, from $\overline{G}$ to $\overline{P=Q}$	t_{PLH}	C=50pF	23	29	35	41	ns
		C_L=150pF	27	32	40	47	
	t_{PHL}	C_L=50pF	18	24	30	36	
		C_L=150pF	21	27	35	42	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS / KS74HCTLS 533

Octal D-Type Transparent Latches with 3-State Outputs

FEATURES

- **8 latches in a single package**
- **Full parallel access for loading**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '533 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

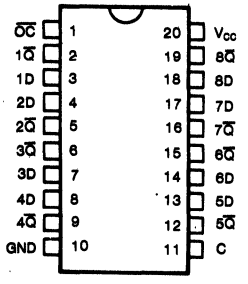
The latches are transparent: when the enable (C) is high, the $\overline{Q}$ outputs follow the complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs at high-impedance state when it is taken high. The $\overline{OC}$ signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

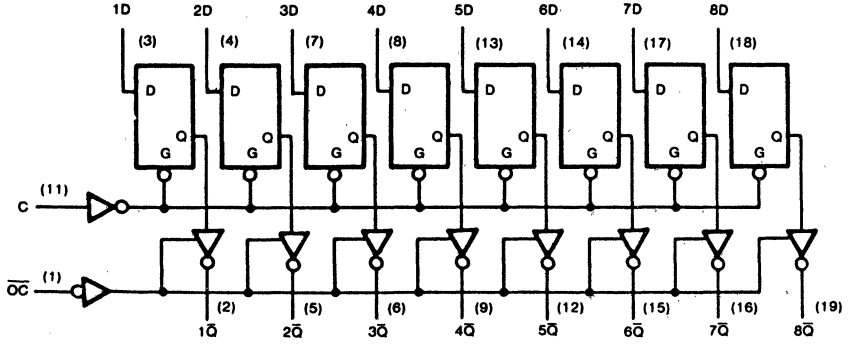


FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	Enable C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS533

Characteristic	Symbol	Conditions†	$T_a=25°C$ $V_{CC}=5.0V$	KS74HCTLS $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$	KS54HCTLS $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits		
Maximum Propagation Delay, D to $\overline{Q}$	t_{PLH}	$C_L=50pF$	14	18	23	27	ns
		$C_L=150pF$	17	21	28	33	
	t_{PHL}	$C_L=50pF$	14	18	23	27	
		$C_L=150pF$	17	21	28	33	
Maximum Propagation Delay C to $\overline{Q}$	t_{PLH}	$C=50pF$	22	30	37	45	ns
		$C_L=150pF$	25	33	43	41	
	t_{PHL}	$C_L=50pF$	22	30	37	48	
		$C_L=150pF$	25	33	43	54	
Maximum Output Enable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PZH}	$R_L=1k\Omega$, $C_L=50pF$	24	32	40	48	ns
		$R_L=1k\Omega$, $C_L=150pF$	27	35	45	54	
	t_{PZL}	$R_L=1k\Omega$, $C_L=50pF$	24	32	40	48	
		$R_L=1k\Omega$, $C_L=150pF$	27	35	45	54	
Maximum Output Disable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PHZ}	$R_L=1k\Omega$, $C_L=50pF$	19	25	31	37	ns
	t_{PLZ}		19	25	31	37	
Minimum Pulse Width, C High	t_w		6	10	12	15	ns
Minimum Setup Time, D before C↓	t_{su}		2	3	4	5	ns
Minimum Hold Time, D after C↓	t_h		6	10	12	15	ns
Maximum Input Capacitance	C_{IN}		5				pF
Maximum Output Capacitance	C_{OUT}	Output Disabled	10				pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC}=V_{CC}$	5				pF
		$\overline{OC}=GND$	30				

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '534 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

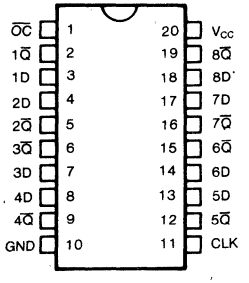
The flip-flops are edge-triggered on the positive transition of the clock: the $\overline{Q}$ outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs in high-impedance state when it is taken high. The OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

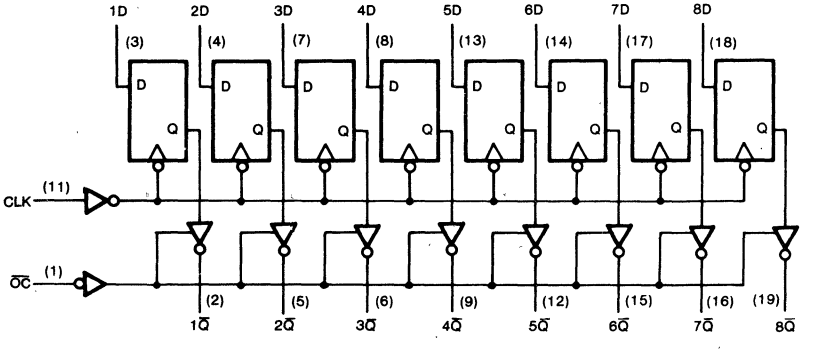


FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0\ 5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS534

Characteristic	Symbol	Conditions†		$T_a=25°C$ $V_{CC}=5.0V$	KS74HCTLS $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54HCTLS $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Operating Frequency	f_{max}	$C_L=50pF$		50	35		30	25	MHz
Maximum Propagation Delay, CLK to any $\overline{Q}$	t_{PLH}	$C_L=50pF$		21	28		35	42	ns
		$C_L=150pF$		24	31		40	48	
	t_{PHL}	$C_L=50pF$		21	28		35	42	
		$C_L=150pF$		24	31		40	48	
Maximum Output Enable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PZH}	$R_L=1k\Omega$	$C_L=50pF$	21	28		35	42	ns
			$C_L=150pF$	24	31		40	48	
	t_{PZL}		$C_L=50pF$	21	28		35	42	
			$C_L=150pF$	24	31		40	48	
Maximum Output Disable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PHZ}	$R_L=1k\Omega$ $C_L=50pF$		19	25		31	37	ns
	t_{PLZ}			19	25		31	37	
Minimum Pule Width, CLK High or Low	tw			9	13		15	18	ns
Minimum Setup Time, D before CLK↑	t_{su}			10	13		17	20	ns
Minimum Hold Time, D after CLK↑	t_h			−3	0		0	0	ns
Maximum Input Capacitance	C_{IN}			5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC}=V_{CC}$		5					pF
		$\overline{OC}=GND$		30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS / KS74HCTLS 540/541

Octal Buffers and Line Drivers with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

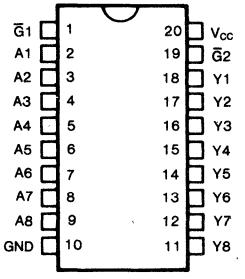
The '540 and '541 are general purpose high-speed octal line drivers/buffers with 3-state outputs. The inputs and outputs are located on opposite sides of the 20-pin package, thus improving circuit board density. The '540 provides inverted data and the '541 provides true data at the outputs.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high impedance state.

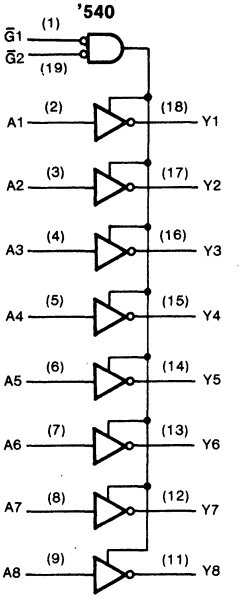
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

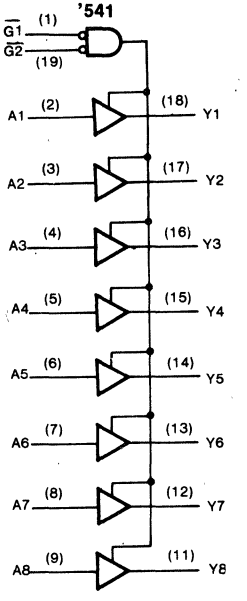
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground

PIN CONFIGURATION



LOGIC DIAGRAMS





FUNCTION TABLE

Input			Output	
$\overline{G}_1$	$\overline{G}_2$	A	'540	'541
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS540, HCTLS541

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Propagation Delay, A to Y	t_{PLH}	C_L= 50pF		11	15		19	23	ns
		C_L=150pF		14	18		24	29	
	t_{PHL}	C_L= 50pF		11	15		19	23	
		C_L=150pF		14	18		24	29	
Maximum Output Enable Time, $\overline{G}$ to Y	t_{PZH}	R_L=1kΩ	C_L= 50pF	18	25		25	37	ns
			C_L=150pF	21	28		30	43	
	t_{PZL}		C_L=50pF	18	25		31	37	
			C_L=50pF	21	28		36	43	
Maximum Output Disable Time, $\overline{G}$ to Y	t_{PHZ}	R_L=1kΩ		13	18		23	27	ns
	t_{PLZ}	C_L=50pF		13	18		23	27	
Maximum Input Capacitance	C_{IN}			5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{G}$=V_{CC}		5					pF
		$\overline{G}$=GND		30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **8 latches in a single package**
- **Full parallel access for loading**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to + 85°C
  KS54AHCT: −55°C to + 125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '563 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer register, I/O ports, bidirectional bus drivers and working registers.

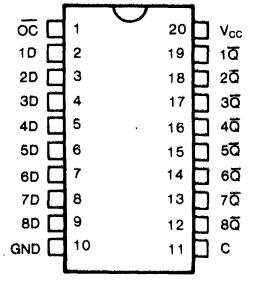
The latches are transparent; when the enable (C) is high, the Q outputs follow complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at a high-impedance stage when it is taken high. The OC signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

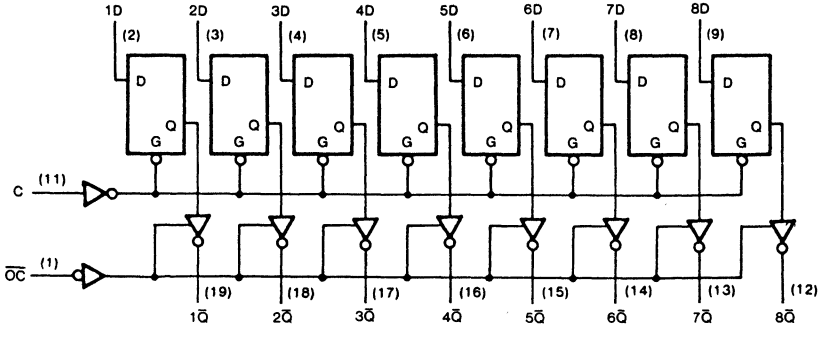


FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	Enable C	D	$\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS563

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits				
Maximum Propagation Delay, D to $\overline{Q}$	t_{PLH}	$C_L = 50pF$	14	18		23	27	ns
		$C_L = 150pF$	17	21		28	33	
	t_{PHL}	$C_L = 50pF$	14	18		23	27	
		$C_L = 150pF$	17	21		28	33	
Maximum Propagation Delay C to $\overline{Q}$	t_{PLH}	$C = 50pF$	22	30		37	45	ns
		$C_L = 150pF$	25	33		42	51	
	t_{PHL}	$C_L = 50pF$	22	30		37	45	
		$C_L = 150pF$	25	33		42	51	
Maximum Output Enable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$	24	32		40	48	ns
		$R_L = 1k\Omega$, $C_L = 150pF$	27	35		45	54	
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$	24	32		40	48	
		$R_L = 1k\Omega$, $C_L = 150pF$	27	35		45	54	
Maximum Output Disable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	19	25		31	37	ns
	t_{PLZ}		19	25		31	37	
Minimum Pulse Width, C High	t_w		9	13		15	18	ns
Minimum Setup Time, D before C↓	t_{su}		6	8		10	10	ns
Minimum Hold Time, D after C↓	t_h		6	10		12	15	ns
Maximum Input Capacitance	C_{IN}		5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC} = V_{CC}$	5					pF
		$\overline{OC} = GND$	30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

5

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '564 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

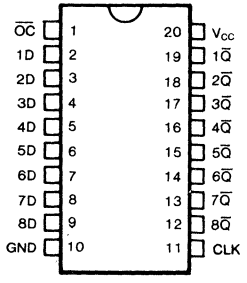
The flip-flops are edge-triggered: on the positive transition of the clock, the $\overline{Q}$ outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs at high impedance state when It is taken high. The $\overline{OC}$ signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

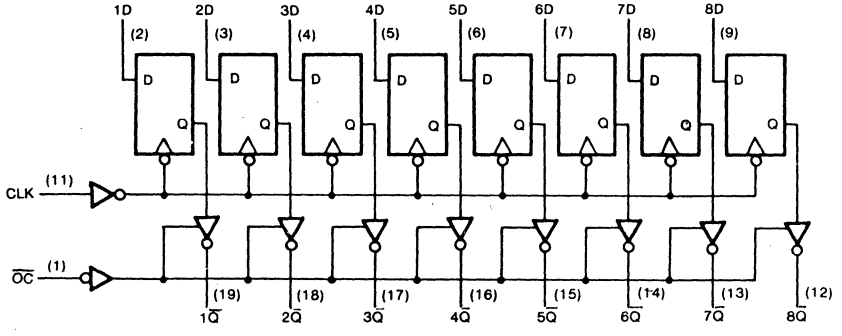


FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS564

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits				
Maximum Operating Frequency	f_{max}	C_L= 50pF	45	35		30	25	MHz
Maximum Propagation Delay, CLK to any $\overline{Q}$	t_{PLH}	C_L= 50pF	21	28		35	42	ns
		C_L=150pF	24	31		40	48	
	t_{PHL}	C_L= 50pF	21	28		35	42	
		C_L=150pF	24	31		40	48	
Maximum Output Enable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PZH}	R_L=1kΩ, C_L= 50pF	21	28		35	42	ns
		R_L=1kΩ, C_L=150pF	24	31		40	48	
	t_{PZL}	R_L=1kΩ, C_L= 50pF	21	28		35	42	
		R_L=1kΩ, C_L=150pF	24	31		40	48	
Maximum Output Disable Time, $\overline{OC}$ to any $\overline{Q}$	t_{PHZ}	R_L=1kΩ, C_L=50pF	19	25		31	37	ns
	t_{PLZ}		19	25		31	37	
Minimum Pulse Width, CLK High or Low	t_w		9	12		15	18	ns
Minimum Setup Time, D before CLK↑	t_{su}		10	13		17	20	ns
Minimum Hold Time, D after CLK↑	t_h		−3	0		0	0	ns
Maximum Input Capacitance	C_{IN}		5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC}$=V_{CC}	5					pF
		$\overline{OC}$=GND	30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **8 latches in a single package**
- **Full parallel access for loading**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74AHCT: −40°C to + 85°C
  KS54HACT: −40°C to + 125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '573 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

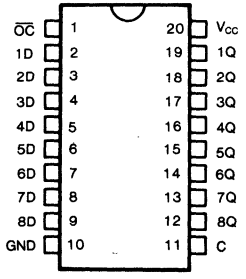
The latches are transparent: when the enable (C) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs at a high-impedance state when it is taken high. The $\overline{OC}$ signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

There devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

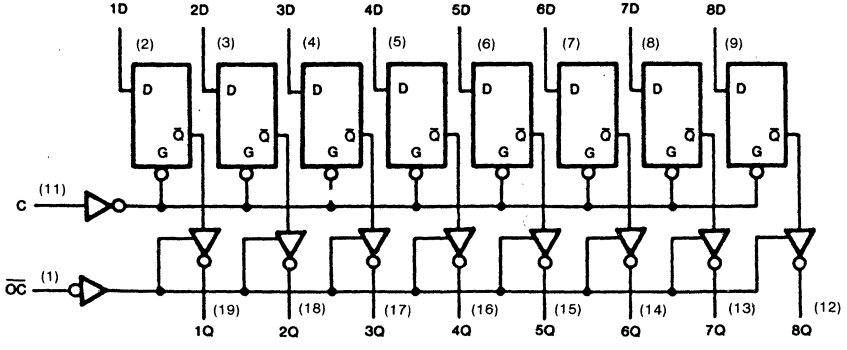


FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	Enable C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS573

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Propagation Delay, D to Q	t_{PLH}	$C_L = 50pF$		14	18	23	27	ns
		$C_L = 150pF$		17	21	28	33	
	t_{PHL}	$C_L = 50pF$		14	18	23	27	
		$C_L = 150pF$		17	21	28	33	
Maximum Propagation Delay C to Q	t_{PLH}	$C = 50pF$		22	30	37	45	ns
		$C_L = 150pF$		25	33	42	51	
	t_{PHL}	$C_L = 50pF$		22	30	37	45	
		$C_L = 150pF$		25	33	42	51	
Maximum Output Enable Time, $\overline{OC}$ to any Q	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	24	32	40	48	ns
			$C_L = 150pF$	27	35	45	54	
	t_{PZL}		$C_L = 50pF$	24	32	40	48	
			$C_L = 150pF$	27	35	45	54	
Maximum Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	$R_L = 1k\Omega$		19	25	31	37	ns
	t_{PLZ}	$C_L = 50pF$		19	25	31	37	
Minimum Pulse Width, C High	t_w			9	12	15	18	ns
Minimum Setup Time, D before C↓	t_{su}			6	8	10	12	ns
Minimum Hold Time, D after C↓	t_h			6	10	12	15	ns
Maximum Input Capacitance	C_{IN}			5				pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10				pF
Power Dissipation Capacitance*	C_{PD}	$\overline{OC} = V_{CC}$ (per stage)		5				pF
		$\overline{OC} = GND$		30				

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

5

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '574 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

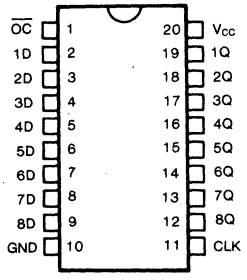
The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs at a high-impedance state when it is taken high. The $\overline{OC}$ signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

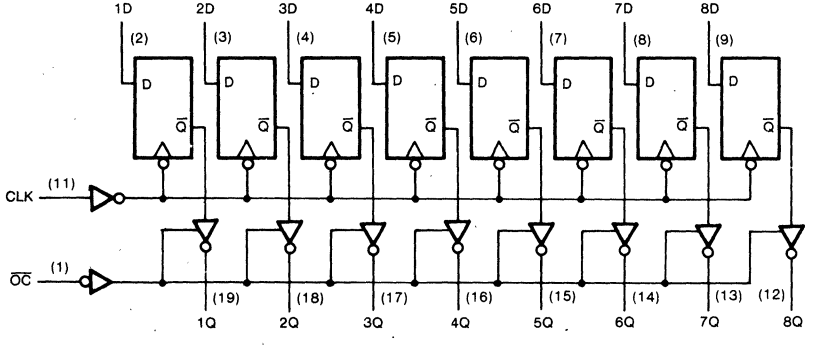


FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS574

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Operating Frequency	f_{max}	C_L= 50pF		45	35	30	25	MHz
Maximum Propagation Delay, CLK to any Q	t_{PLH}	C_L= 50pF		21	28	35	42	ns
		C_L=150pF		24	31	40	48	
	t_{PHL}	C_L= 50pF		21	28	35	42	
		C_L=150pF		24	31	40	48	
Maximum Output Enable Time, $\overline{OC}$ to any Q	t_{PZH}	R_L=1kΩ	C_L= 50pF	21	28	35	42	ns
			C_L=150pF	24	31	40	48	
	t_{PZL}		C_L= 50pF	21	28	35	42	
			C_L=150pF	24	31	40	48	
Maximum Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	R_L=1kΩ		19	25	31	37	ns
	t_{PLZ}	C_L=50pF		19	25	31	37	
Minimum Pulse Width, CLK High or Low	t_w			9	12	15	18	ns
Minimum Setup Time, D before CLK↑	t_{su}			10	13	17	20	ns
Minimum Hold Time, D after CLK↑	t_h			−3	0	0	0	ns
Maximum Input Capacitance	C_{IN}			5				pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10				pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC}$=V_{CC}		5				pF
		$\overline{OC}$=GND		30				

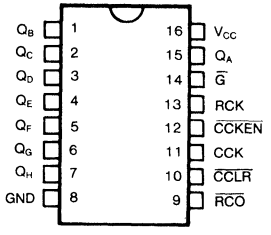
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

FEATURES

- **Choice of 3-State ('590) and Open-Drain ('591) Outputs**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs**
  (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These devices each consist of an 8-bit counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{CCKEN}$, is low. When the counter increments to the all ones condition, ripple carry out, $\overline{RCO}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{RCO}$ of the first stage to the $\overline{CCKEN}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the $\overline{RCO}$ of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed the outputs which are enabled when the enable input, G, is taken low. This enables connection of this part to a system bus. The Q outputs of the '590 are 3-State and those for '591 are Open-drain.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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FUNCTION TABLE

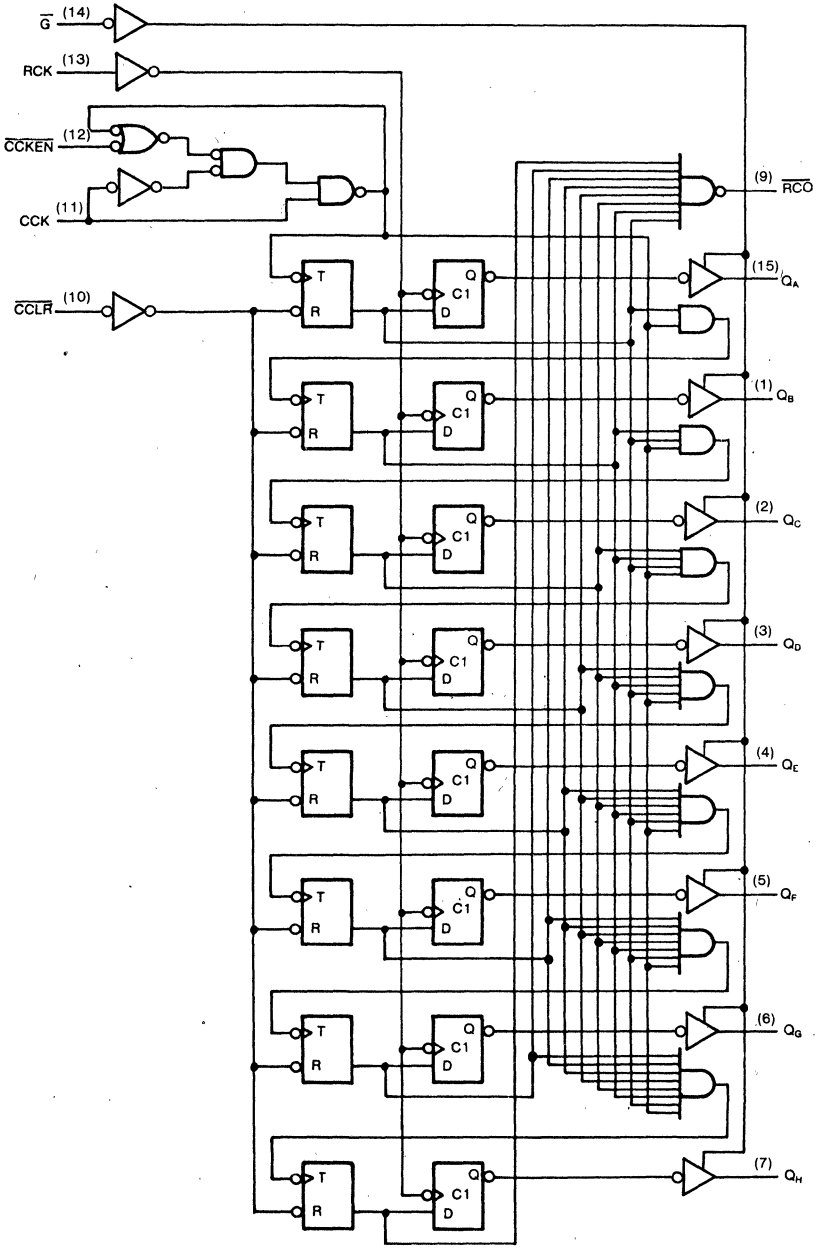
INPUTS					FUNCTION
$\overline{G}$	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q Outputs disable
L	X	X	X	X	Q Outputs enable
L	⌐	X	X	X	Counter data is stored into register
L	¬	X	X	X	Register state is not changed
L	X	L	X	X	Counter clear
L	X	H	L	⌐	Advance one count
L	X	H	L	¬	No count
L	X	H	H	X	No count

X: Don't care

$$\overline{RCO} = Q_A' \bullet Q_B' Q_C' \bullet Q_D' Q_E' \bullet Q_F' Q_G' \bullet Q_H'$$

($Q_A' \sim Q_H'$: Internal outputs of the counter)

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} +0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} +0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} +0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (All '590 Outputs and '591 $\overline{RCO}$ Outputs)	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS590

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}		35	25	20	20	ns
Maximum Propagation Delay, CCK↑ to $\overline{RCO}$		t_{PLH}	$C_L = 50pF$	24	32	40	48	ns
		t_{PHL}		24	32	40	48	
Maximum Propagation Delay, $\overline{CCLR}$↓ to $\overline{RCO}$		t_{PLH}		26	35	44	52	ns
Maximum Propagation Delay, RCK↑ to Q		t_{PLH}		16	21	26	31	ns
		t_{PHL}		16	21	26	31	
Maximum Output Enable Time, $\overline{G}$↓ to Q		t_{PZH}	$R_L = 1k\Omega$ $C_L = 50pF$	18	24	30	36	ns
		t_{PZL}		18	24	30	36	
Maximum Output Disable Time, $\overline{G}$↑ to Q		t_{PHZ}		18	24	30	36	ns
		t_{PLZ}		18	24	30	36	
Minimum Pulse Width	CCK or RCK High or Low	t_w		12	16	20	24	ns
	$\overline{CCLR}$ Low			12	16	20	24	
Minimum Setup Time	$\overline{CCKEN}$↓ before CCK↑	t_{su}		12	16	20	24	ns
	$\overline{CCLR}$↑ before CCK↑			12	16	20	24	
	CCK↑ to RCK↑††			24	32	40	48	
Maximum Input Capacitance		C_{IN}		5				pF
Maximum Output Capacitance		C_{OUT}	Output Disabled	10				pF
Power Dissipation Capacitance*		C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.
†† The RCK↑ to CCK↑ setup time ensures that the counter will see stable data from the register output.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS591

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}		35	25	20		20	ns
Maximum Propagation Delay, CCK↑ to $\overline{RCO}$		t_{PLH}	$C_L = 50pF$ $R_L = 1k\Omega$	24	32	40		48	ns
		t_{PHL}		24	32	40		48	
Maximum Propagation Delay, $\overline{CCLR}$↓ to $\overline{RCO}$		t_{PLH}		26	35	44		52	ns
Maximum Propagation Delay, RCK↑ to Q		t_{PLH}		27	37	46		55	ns
		t_{PHL}		16	21	26		31	
Maximum Output Enable Time, $\overline{G}$↓ to Q		t_{PZL}		18	24	30		36	ns
Maximum Output Disable Time, $\overline{G}$↑ to Q		t_{PLZ}		18	24	30		36	ns
Minimum Pulse Duration	CCK or RCK High or Low	t_w		12	16	20		24	ns
	$\overline{CCLR}$ Low			12	16	20		24	
Minimum Setup Time	$\overline{CCKEN}$↓ before CCK↑	t_{su}		12	16	20		24	ns
	$\overline{CCLR}$↑ before CCK↑			12	16	20		24	
	CCK↑ to RCK↑††			24	32	40		48	
Maximum Input Capacitance		C_{IN}		5					pF
Maximum Output Capacitance		C_{OUT}	Output Disabled						pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.
†† The clocks may be tied together, in which case the register state will be one clock pulse behind the counter.

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KS54HCTLS/KS74HCTLS 592/593

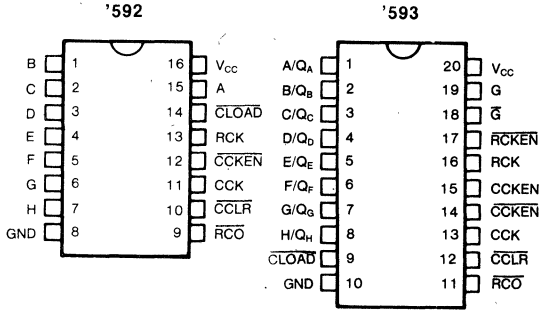
8-Bit Binary Counters with Input Registers

Preliminary Specifications

FEATURES

- **Parallel Register Inputs ('592)**
- **Parallel 3-State I/O: Register Inputs/Counter Outputs ('593)**
- **Counter Has Direct Overriding Load and Clear**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS



DESCRIPTION

The '592 and '593 both contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{CCKEN}$, is low. When the counter increments to the all ones condition, ripple carry out, $\overline{RCO}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{RCO}$ of the first stage to the $\overline{CCKEN}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the $\overline{RCO}$ of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, $\overline{CLOAD}$, input is taken low.

The '592 differs from the '593 in that the latter device has bidirectional input/output pins. The 3-state outputs of the counter can be enabled and are active when enable input, $\overline{G}$, is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The '593 also has a second clock enable pin, $\overline{CCKEN}$, which is active high and it also has an active low register clock enable, $\overline{RCKEN}$.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

INPUTS					FUNCTION
RCK	$\overline{CLOAD}$	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
X	L	H	X	X	Register data is loaded into counter
X	H	L	X	X	Counter clear
↑	H	H	X	X	The data of a thru H inputs is stored into register
↓	H	H	X	X	Register state is not changed
X	H	H	L	↑	Counter advances the count
X	H	H	L	↓	No count
X	H	H	H	X	No count

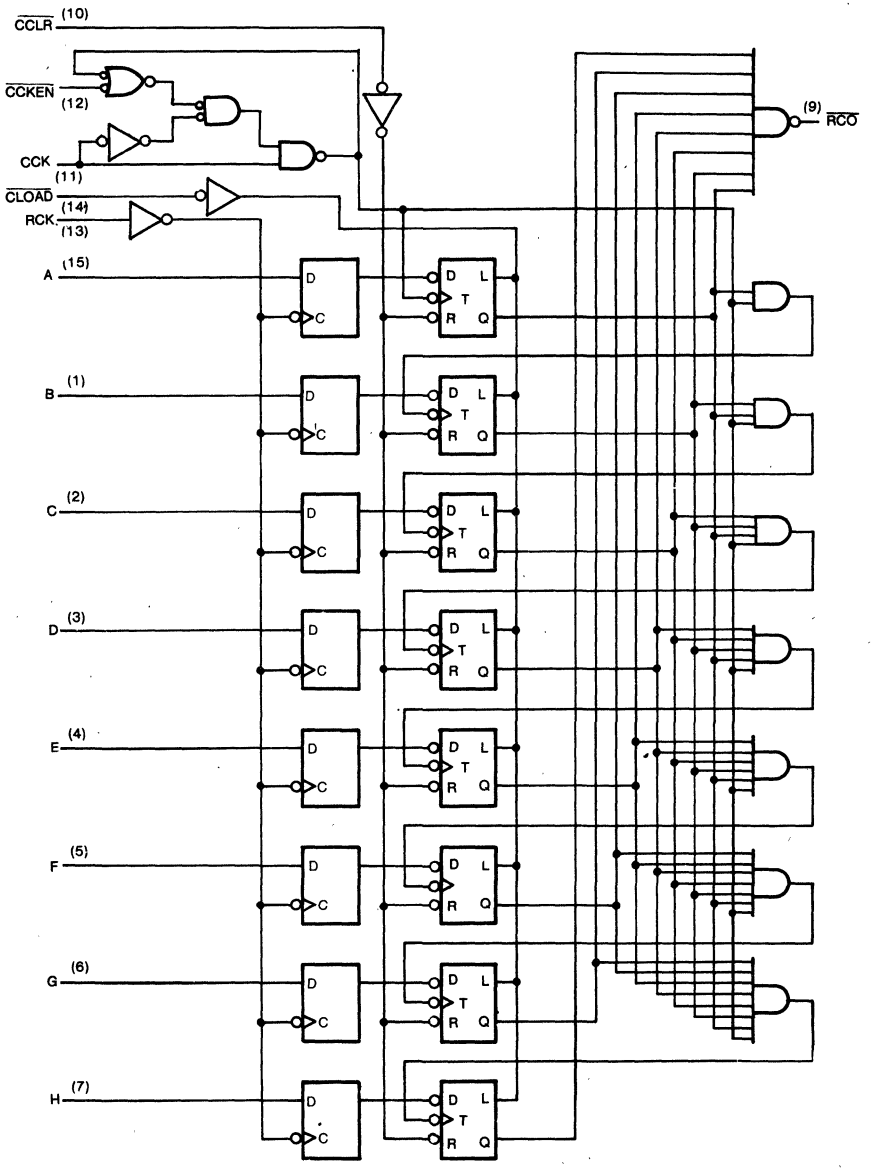
X: Don't care

$$\overline{RCO} = \overline{Q_A' \cdot Q_B' Q_C' \cdot Q_D' Q_E' \cdot Q_F' Q_G' \cdot Q_H'}$$

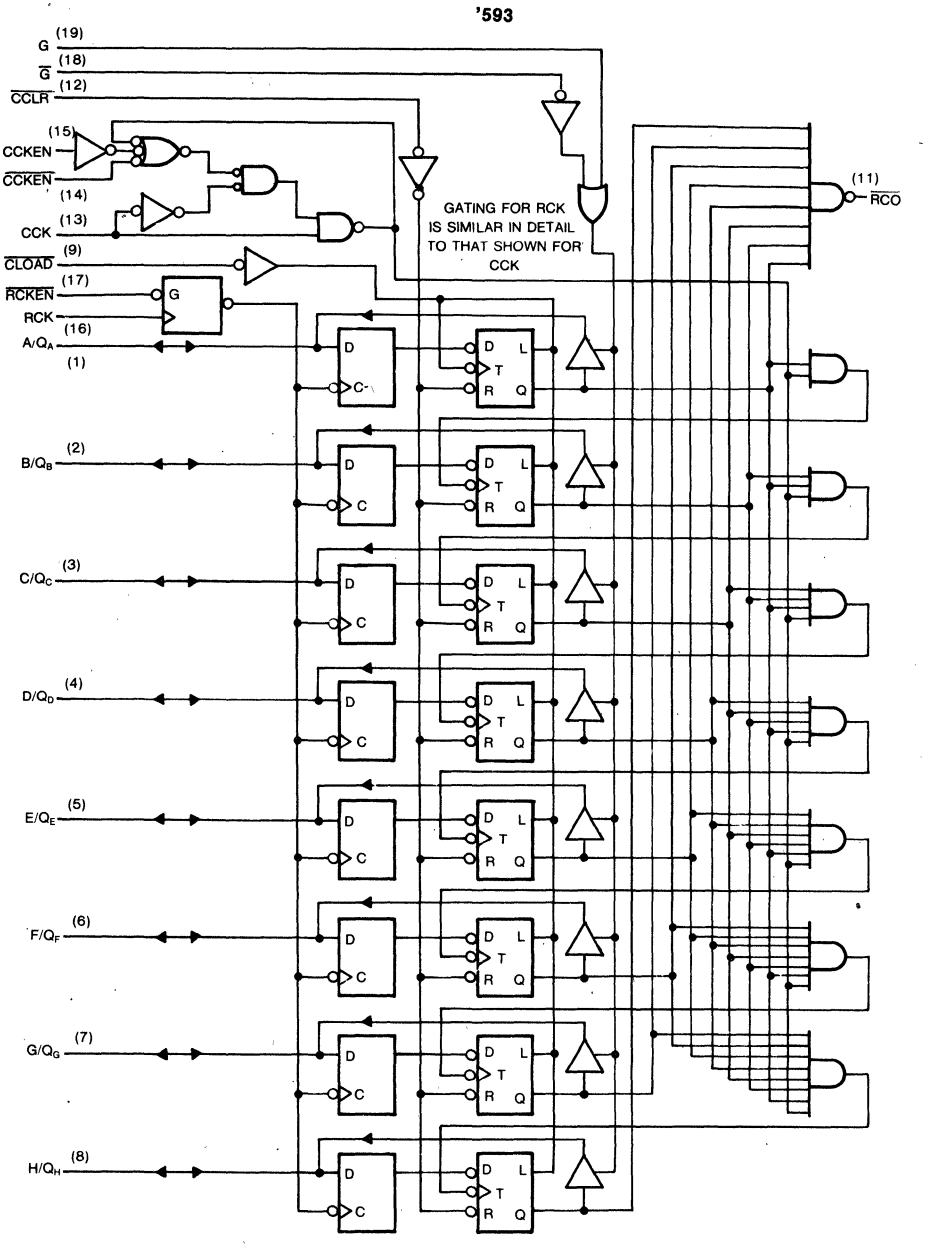
($Q_A' \sim Q_H'$: Internal outputs of the counter)

LOGIC DIAGRAMS

'592



LOGIC DIAGRAMS (Continued)



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), HCTLS592

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}		35	25		20	20	MHz
Maximum Propagation Delay, CCK↑ to $\overline{RCO}$		t_{PLH}	$C_L = 50pF$	24	32		40	48	ns
		t_{PHL}		24	32		40	48	
Maximum Propagation Delay, $\overline{CLOAD}$↓ to $\overline{RCO}$		t_{PLH}		24	32		40	48	ns
		t_{PHL}		24	32		40	48	
Maximum Propagation Delay, $\overline{CCLR}$↓ to $\overline{RCO}$		t_{PHL}		24	32		40	48	ns
Maximum Propagation Delay, RCK↑ to $\overline{RCO}$		t_{PLH}	$C_L = 50pF$ $\overline{CLOAD} = GND$	26	35		44	52	ns
		t_{PHL}		26	35		44	52	
Minimum Pulse Width	CCK or RCK High or Low	t_w		12	16		20	24	ns
	$\overline{CCLR}$ Low			12	16		20	24	
	$\overline{CLOAD}$ Low			12	16		20	24	
Minimum Setup Time	$\overline{CCKEN}$↓ before CCK↑	t_{su}		12	16		20	24	ns
	$\overline{CCLR}$↑ before CCK↑			12	16		20	24	
	RCK↑ before CCK↑††			24	32		40	48	
	Data A-H↑ before RCK↑			12	16		20	24	
Minimum Hold Time		t_h		−3	0		0	0	ns
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.
†† The RCK↑ to CCK↑ setup time ensures that the counter will see stable data from the register output.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS593

Characteristic		Symbol	Conditions†		$T_a=25°C$ $V_{CC}=5.0V$	KS74HCTLS $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54HCTLS $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$		Unit
					Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}			35	25		20	20	MHz
Maximum Propagation Delay, CCK↑ to Q		t_{PLH}	$C_L=50pF$		24	32		40	48	ns
			$C_L=150pF$		27	35		45	54	
		t_{PHL}	$C_L=50pF$		24	32		40	48	
			$C_L=150pF$		27	35		45	54	
Maximum Propagation Delay, CCK↑ to $\overline{RCO}$		t_{PLH}	$C_L=50pF$		24	32		40	48	ns
		t_{PHL}			24	32		40	48	
Maximum Propagation Delay, $\overline{CLOAD}$↓ to Q		t_{PLH}	$C_L=50pF$		24	32		40	48	ns
			$C_L=150pF$		27	35		45	54	
		t_{PHL}	$C_L=50pF$		24	32		40	48	
			$C_L=150pF$		27	35		45	54	
Maximum Propagation Delay, $\overline{CLOAD}$↓ to $\overline{RCO}$		t_{PLH}	$C_L=50pF$		24	32		40	48	ns
		t_{PHL}			24	32		40	48	
Maximum Propagation Delay, RCK↑ to $\overline{RCO}$		t_{PLH}	$C_L=50pF$		26	35		44	52	ns
		t_{PHL}	CLOAD=GND		26	35		44	52	
Maximum Propagation Delay, $\overline{CCLR}$↓ to Q		t_{PHL}	$C_L=50pF$		24	32		40	48	ns
			$C_L=150pF$		27	35		45	54	
Maximum Propagation Delay, $\overline{CCLR}$↓ to $\overline{RCO}$		t_{PLH}	$C_L=50pF$		24	32		40	48	ns
Maximum Enable Time, G↑ or $\overline{G}$↓ to Q		t_{PZL}	$R_L=1k\Omega$	$C_L=50pF$	21	28		39	42	ns
				$C_L=150pF$	24	31		44	48	
		t_{PZL}	$R_L=1k\Omega$	$C_L=50pF$	21	28		35	42	ns
				$C_L=150pF$	24	31		44	48	
Maximum Disable Time $\overline{G}$↓ or G↑ to Q		t_{PLH}	$R_L=1k\Omega$		24	28		35	42	ns
		t_{PLZ}	$C_L=50pF$		21	28		35	42	
Minimum Pulse Width	CCK or RCK High or Low	t_w			12	16		20	24	ns
	$\overline{CCLR}$ Low				12	16		20	24	
	$\overline{CLOAD}$ Low				12	16		20	24	
Minimum Setup Time	$\overline{CCKEN}$↓ before CCK↑	t_{su}			12	16		20	24	ns
	$\overline{RCKEN}$↓ to RCK↑					12		16	24	
	$\overline{CCLR}$↓ before CCK↑				12	16		20	24	
	RCK↑ before CCK↑††				24	32		40	48	
	Data A-H before RCK↑				12	16		20	24	
Hold Time		t_h			−3	0		0	0	ns
Maximum Input Capacitance		C_{IN}			5					pF
Maximum Output Capacitance		C_{OUT}	Output Disabled		10	10				pF
Power Dissipation Capacitance*		C_{PD}								pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

†† The RCK↑ to CCK↑ setup time ensures that the counter will see stable data from the register output.

FEATURES

- **8-Bit Serial-In, Parallel-Out Shift Registers With Storage**
- **Choice of 3-State ('595) or Open-Drain ('596) Parallel Outputs**
- **Shift Register Has Direct Clear**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

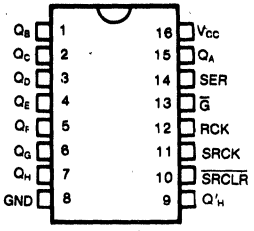
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('595) or open-drain ('596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

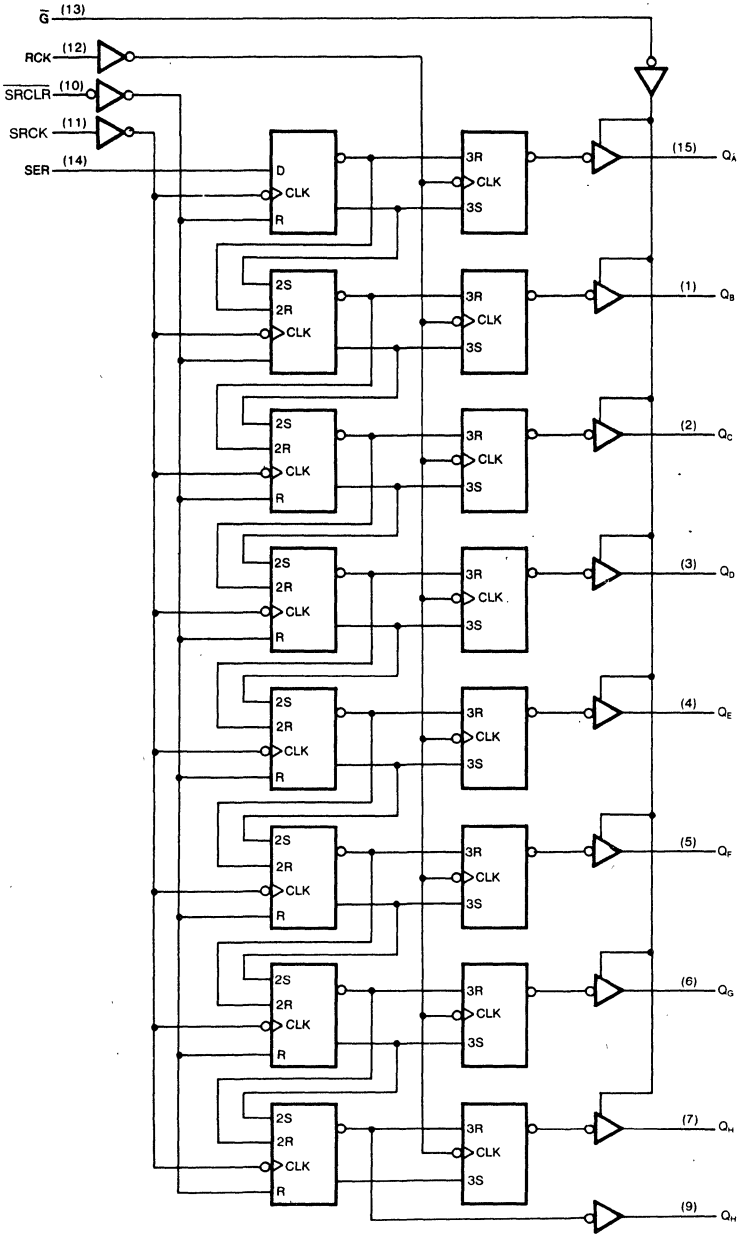


FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCK	$\overline{SRCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	Q_A thru Q_H outputs disable
X	X	X	X	L	Q_A thru Q_H outputs enable
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X	↓	H	X	X	State of S.R. is not changed.
X	X	X	↑	X	S.R. data is stored into storage register.
X	X	X	↓	X	Storage register state is not changed.

X: DON'T CARE

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (All '595 Outputs and '596 Q'_H Output)	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Output Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS595, HCTLS596

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits				
Maximum Propagation Delay, SRCK↑ to Q'_H	t_{PLH}	$C_L = 50pF$	15	18		25	30	ns
	t_{PHL}	$C_L = 50pF$	15	18		25	30	ns
Maximum Propagation Delay, RCK↑ to Q_A thru Q_H	t_{PLH}	$C_L = 50pF$	17	22		28	33	ns
		$C_L = 150pF$	20	25		33	39	
	t_{PHL}	$C_L = 50pF$	17	22		28	33	ns
		$C_L = 150pF$	20	25		33	39	
Maximum Output Enable Time, $\overline{G}$↓ to Q_A thru Q_H ('595 only)	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$	18	24		30	36	ns
		$R_L = 1k\Omega$, $C_L = 150pF$	21	27		35	42	
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$	18	24		30	36	ns
		$R_L = 1k\Omega$, $C_L = 150pF$	21	27		35	42	
Maximum Output Disable Time, $\overline{G}$↑ to Q_A thru Q_H ('595 only)	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	18	24		30	36	ns
			21	27		35	42	
	t_{PLZ}	$R_L = 1k\Omega$, $C_L = 50pF$	18	24		30	36	ns
			21	27		35	42	
Maximum Propagation Delay, $\overline{G}$↑ to Q_A thru Q_H ('596 only)	t_{PLH}	$C_L = 50pF$	18	24		30	36	ns
		$C_L = 150pF$	21	27		35	42	
Maximum Propagation Delay, $\overline{G}$↓ to Q_A thru Q_H ('596 only)	t_{PHL}	$C_L = 50pF$	18	24		30	36	ns
		$C_L = 150pF$	21	27		35	42	
Minimum Pulse Width — SRCK or RCK	t_w		12	16		20	24	ns
Minimum Pulse Width — $\overline{SRCLR}$ Low	t_w		12	16		20	24	ns
Minimum Setup Time — $\overline{SRCLR}$↑ to SRCK↑	t_{su}		12	16		20	24	ns
Minimum Setup Time — SER to SRCK↑	t_{su}		12	16		20	24	ns
Minimum Setup Time — SRCK↑ to RCK††	t_{su}		24	32		40	48	ns
Minimum Hold Time	t_h		−3	0		0	0	ns
Maximum Input Capacitance	C_{IN}		5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

†† This setup time ensures the register will see stable data from the register output.

FEATURES

- **8-Bit Parallel Storage Register Inputs**
- **shift Register has Direct Overiding Load and Clear**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

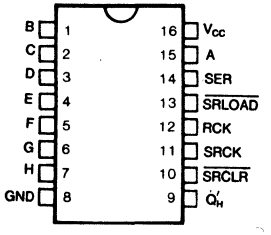
DESCRIPTION

The '597 consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

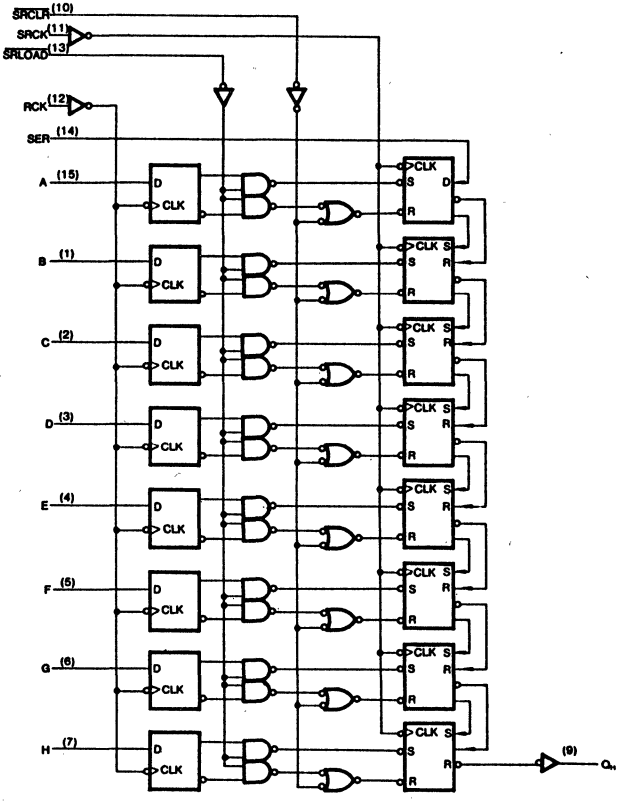
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCK	$\overline{SRCLR}$	$\overline{SRLOAD}$	RCK	
X	X	L	H	X	S.R. is cleared to "L"
X	X	H	J	X	Input register data is stored into S.R.
L	↓	H	H	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	↓	H	H	X	First stage of S.R. becomes "H". Other stages stores the data of previous stage, respectively.
X	X	X	X		State of S.R. is not changed.
X	X	X	X	↓	Input data on A~H line is stored into input register
X	X	X	X	⌐	Storage register state is not changed.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS597

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}		35	25		20	20	MHz
Maximum Propagation Delay, SRCK↑ to Q'_H		t_{PLH}	$C_L = 50pF$	15	18		25	30	ns
		t_{PHL}		15	18		25	30	
Maximum Propagation Delay, $\overline{SRLOAD}$↓ to Q'_H		t_{PLH}		18	24		30	36	ns
		t_{PHL}		18	24		30	36	
Maximum Propagation Delay, $\overline{SRCLR}$↓ to Q'_H		t_{PHL}		17	22		28	33	ns
Maximum Propagation Delay, RCK↑ to Q'_H		t_{PLH}	$C_L = 50pF$ $\overline{SLOAD}$=Low	21	29		35	42	ns
		t_{PHL}		21	29		35	42	
Minimum Pulse Width	RCK or SRCK High or Low	t_w		12	16		20	24	ns
	$\overline{SRCLR}$ or $\overline{SRLOAD}$ Low			12	16		20	24	
Minimum Setup Time	$\overline{SRCLR}$↑ before SRCK↑	t_{su}		12	16		20	24	ns
	RCK↑ before SRCK↑††			24	32		40	48	
	SER before SRCK↑			12	16		20	24	
	A thru H before RCK↑			12	16		20	24	
Minimum Hold Time		t_h		−3	0		0	0	ns
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

†† The RCK↑ before SRCK↑ setup time ensures that shift register will see stable data comming from the register output.

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

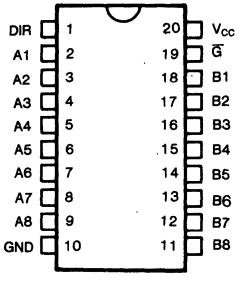
DESCRIPTION

These high-speed octal/bus transceivers are designed for asynchronous two-way communication between data buses. A direction control input (DIR) controls the flow direction of data. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The '643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus. The '640 transfers inverted data in both directions.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

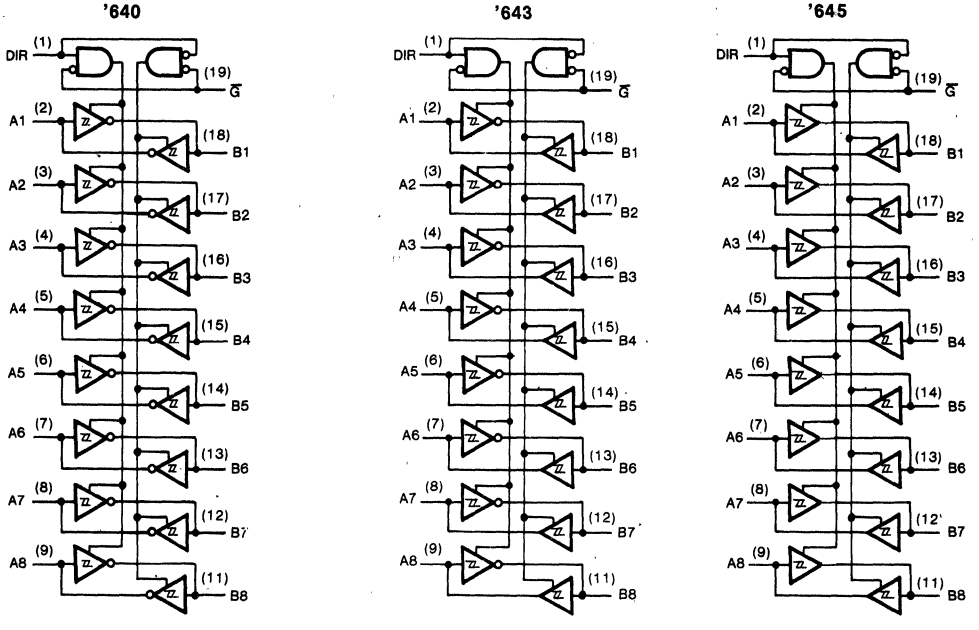
PIN CONFIGURATION



FUNCTION TABLE

Control Inputs		Operation		
$\overline{G}$	DIR	'640	'643	'645
L	L	Inverted data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A
L	H	Inverted data transmitted from Bus A to Bus B	Inverted data transmitted from Bus A to Bus B	Data transmitted from Bus A to Bus B
H	X	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)

LOGIC DIAGRAMS



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS640, HCTLS643, HCTLS645

Characteristic	Symbol	Conditions†		T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
				Typ	Guaranteed Limits		
Maximum Propagation Delay, A to B, or B to A	t_{PLH}	C_L=50pF C_L=150pF		9 12	12 15	16 21	19 25	ns
	t_{PHL}	C_L=50pF C_L=150pF		9 12	12 15	16 21	19 25	
Maximum Output Enable Time, $\overline{G}$ or DIR to A or B	t_{PZH}	R_L=1kΩ	C_L=50pF C_L=150pF	30 33	40 43	50 55	60 65	ns
	t_{PZL}		C_L=50pF C_L=150pF	30 33	40 43	50 55	60 65	
Maximum Output Disable Time, $\overline{G}$ or DIR to A or B	t_{PHZ}	R_L=1kΩ		20	27	34	40	ns
	t_{PLZ}	C_L=50pF		20	27	34	40	
Maximum Input Capacitance	C_{IN}			5				pF
Maximum Output Capacitance	C_{OUT}	Output disabled		10				pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{G}$=V_{CC} $\overline{G}$=GND		5 30				pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

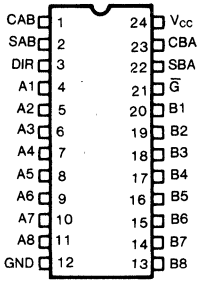
KS54HCTLS/KS74HCTLS 646/648

Octal 3-State Bus Transceivers with Registers

FEATURES

- 8 bi-directional data paths
- Transmits direct or stored data in either direction
- 24-pin 0.3″ slim DIP package
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74AHCT: −40°C to + 85°C
  KS54HACT: −55°C to + 125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



DESCRIPTION

The '646 and '648 are bi-directional bus transceivers with D-type flip-flops and control circuitry to facilitate high speed multiplexed data transmission. The '646 transmits true data and the '648 transmits inverted data.

Data can be transmitted directly from one port to the other in either direction. It also can be stored in the flip-flops from either or both ports for subsequent transmission to the opposite port. Six control inputs govern the data flow:

$\overline{G}$ (output enable) when high, all outputs are disabled, isolating the A and B ports. When low, one port is enabled at a time as determined by the DIR pin.

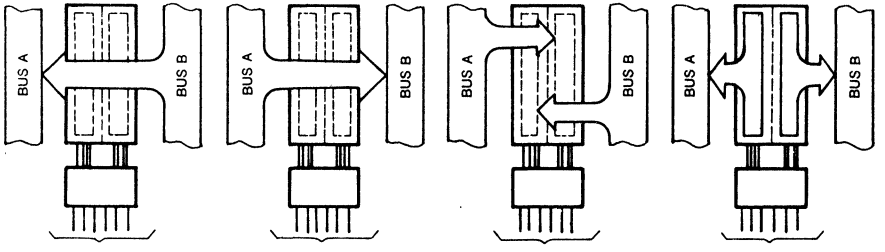
DIR (direction control) disables A or B outputs permitting the pins to be used as inputs thus determining the direction of a data flow. When DIR=high, data flows from A to B.

SAB,SBA (data source AB and BA) determines whether data transmitted is from the data inputs or the registers associated with those inputs.

CAB,CBA (Clock AB and BA) clocks data from the A inputs and the B inputs, respectively, into their associated registers. Since the clocks are not gated with the $\overline{G}$ and DIR pins, data at the A and B pins can be clocked into the flip-flops at any time.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

Real-Time transfer bus B to bus A

(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	X	X	L	X

Real-Time transfer bus A to bus B

(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Storage from A AND/OR B

(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	H
L	H	X	X	H	X

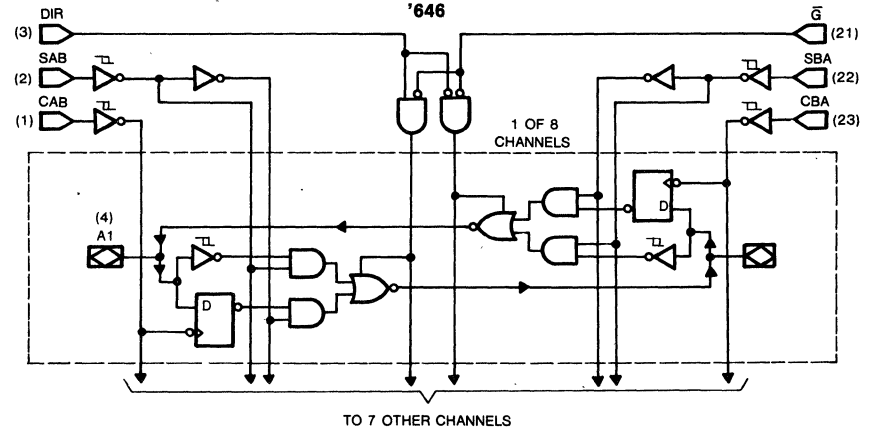
Transfer stored data to A AND/OR B

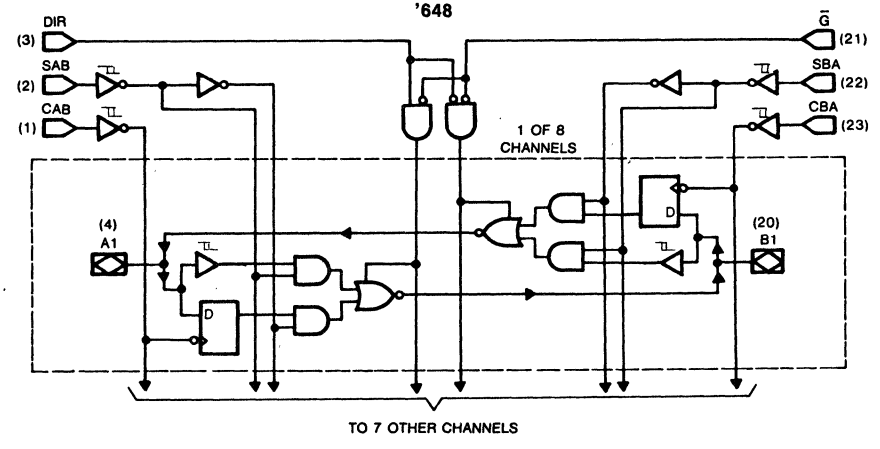
FUNCTION TABLE

Inputs						Data I/O*		Operation or Function	
$\bar{G}$	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	'646	'648
X	X	↑	X	X	X	input	input	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Not specified	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage	isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B data to A bus	Real-Time $\bar{B}$ data to A bus
L	L	X	H or L	X	H			Stored B data to A bus	Stored $\bar{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-Time A data to B bus	Real-Time $\bar{A}$ data to B bus
L	H	H or L	X	H	X			Stored A data to B bus	Stored $\bar{A}$ data to B bus

*The data output functions may be enabled or disabled by various signals at the $\bar{G}$ and DIR inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS646, HCTLS648

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Clock Frequency	f_{max}	C_L=50pF	40	30	25	20	MHz
Maximum Propagation Delay, A or B Input to B or A Output	t_{PHL}	C_L=50pF	14	19	24	29	ns
		C_L=150pF	17	22	29	35	
	t_{PHL}	C_L=50pF	14	19	24	29	
		C_L=150pF	17	22	29	35	
Maximum Propagation Delay, CBA or CAB Input to A or B Output	t_{PLH}	C_L=50pF	22	30	37	45	ns
		C_L=150pF	25	33	42	51	
	t_{PHL}	C_L=50pF	22	30	37	45	
		C_L=150pF	25	33	42	51	
Maximum Propagation Delay,†† SBA or SAB input to A or B Output (with A or B High)	t_{PLH}	C_L=50pF	26	35	44	53	ns
		C_L=150pF	29	38	49	59	
	t_{PHL}	C_L=50pF	26	35	44	53	
		C_L=150pF	29	38	49	59	
Maximum Propagation Delay, SBA or SAB Input to A or B Output (with A or B Low)	t_{PLH}	C_L=50pF	26	35	44	53	ns
		C_L=150pF	29	38	49	59	
	t_{PHL}	C_L=50pF	26	35	44	53	
		C_L=150pF	29	38	49	59	
Maximum Output Enable Time, $\overline{G}$ or DIR Input to A or B Output	t_{PZL}	R_L=1kΩ, C_L=50pF	33	45	56	67	ns
		R_L=1kΩ, C_L=150pF	36	48	61	73	
	t_{PZH}	R_L=1kΩ, C_L=50pF	33	45	56	67	
		R_L=1kΩ, C_L=150pF	36	48	61	73	
Maximum Output Disable Time, $\overline{G}$ or DIR Input to A or B Output	t_{PHZ}	R_L=1kΩ, C_L=50pF	26	35	44	53	ns
	t_{PLZ}		26	35	44	53	
Pulse Duration, Clocks High or Low	t_w		10	13	17	20	ns
Setup Time, A before CAB↑ or B before CBA↑	t_{su}		10	13	17	20	ns
Hold Time, A after CAB↑ or B after CBA↑	t_h		−3	0		0	ns
Maximum Input Capacitance	C_{IN}		5				pF
Maximum Output Capacitance	C_{OUT}	Output Disabled	10				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

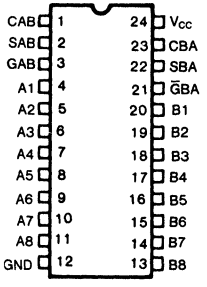
†† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Preliminary Specifications

FEATURES

- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of Time and Inverting Data Paths**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



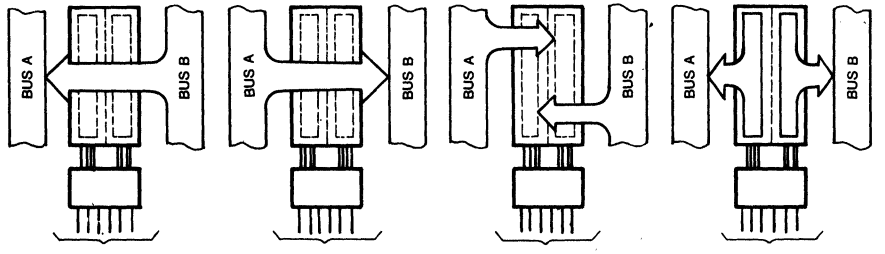
DESCRIPTION

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{G}$BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

Real-Time transfer bus B to bus A

(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	X	X	L	X

Real-Time transfer bus A to bus B

(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Storage from A AND/OR B

(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	H
L	H	X	X	H	X

Transfer stored data to A and/or B

FUNCTION TABLE

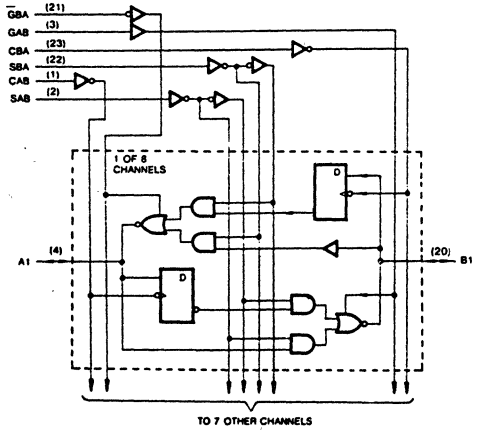
INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'651	'652
L	H	H or L	H or L	X	X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L	H	↑	↑	X	X				
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B	Store A Hold B
H	H	↑	↑	X**	X	Input	Output*	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X**	Output*	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to a Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

* The data output functions may be enabled or disabled by various signals at the GAB and $\overline{GBA}$ inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

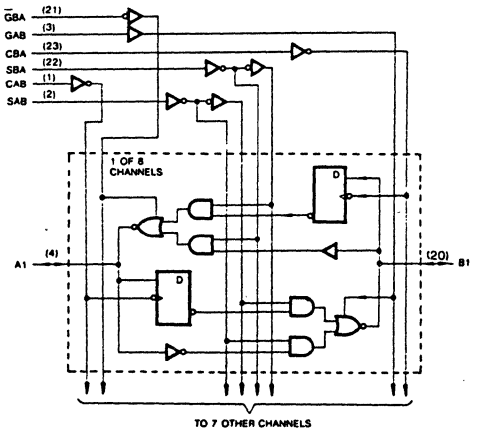
** Select control=L: clocks can occur simultaneously
Select control=H: clocks must be staggered in order to load both registers

LOGIC DIAGRAMS

'651



'652



5

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS651, HCTLS652

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits				
Maximum Clock Frequency	f_{max}	$C_L = 50pF$	40	30		25	20	MHz
Maximum Propagation Delay, A or B Input to B or A Ouput	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	14 17	19 22		24 29	29 35	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	14 17	19 22		21 26	20 26	
Maximum Propagation Delay, CBA or CAB Input to A or B Output	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	22 25	30 33		37 42	45 51	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	22 25	30 33		37 42	45 51	
Maximum Propagation Delay, SBA or SAB Input to A or B Output (with A or B High)	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	26 29	35 38		44 49	53 59	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	26 29	35 38		44 49	53 59	
Maximum Propagation Delay, SBA or SAB Input to A or B Output (with A or B Low)	t_{PLH}	$C_L = 50pF$ $C_L = 150pF$	26 29	35 38		44 49	53 59	ns
	t_{PHL}	$C_L = 50pF$ $C_L = 150pF$	26 29	35 38		44 49	53 59	
Maximum Output Enable Time, $\overline{G}$BA to A or GAB to B	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	33 39	45 48		56 61	67 73	ns
	t_{PZH}	$R_L = 1k\Omega$, $C_L = 50pF$ $R_L = 1k\Omega$, $C_L = 150pF$	33 39	45 48		56 61	67 73	
Maximum Output Disable Time, $\overline{G}$BA to A or GAB to B	t_{PHZ}	$R_L = 1k\Omega$	26	35		44	53	ns
	t_{PLZ}	$C_L = 50pF$	26	35		44	53	
Minimum Pulse Width Clocks High or Low	t_w		10	13		17	20	ns
Minimum Setup Time, A before CAB↑ or B before CBA↑	t_{su}		10	13		17	20	ns
Minimum Hold Time, A after CAB↑ or B after CBA↑	t_h		−3	0		0	0	ns
Maximum Input Capacitance	C_{IN}		5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10				pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

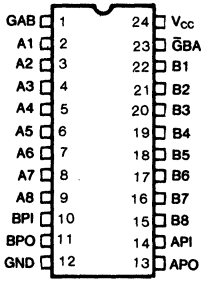
5

Preliminary Specifications

FEATURES

- **Bus Transceivers with Inverting Outputs ('658) or True Outputs ('659)**
- **Generates a Parity Bit for A Bus and B Bus**
- **Easily Cascadable**
- **Internal Active Pull-Ups and Pull-Downs**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus, or from the B Bus to the A Bus, depending on the levels at the direction control inputs, GAB and $\overline{G}BA$. These devices also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuits on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptiblity to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuits.

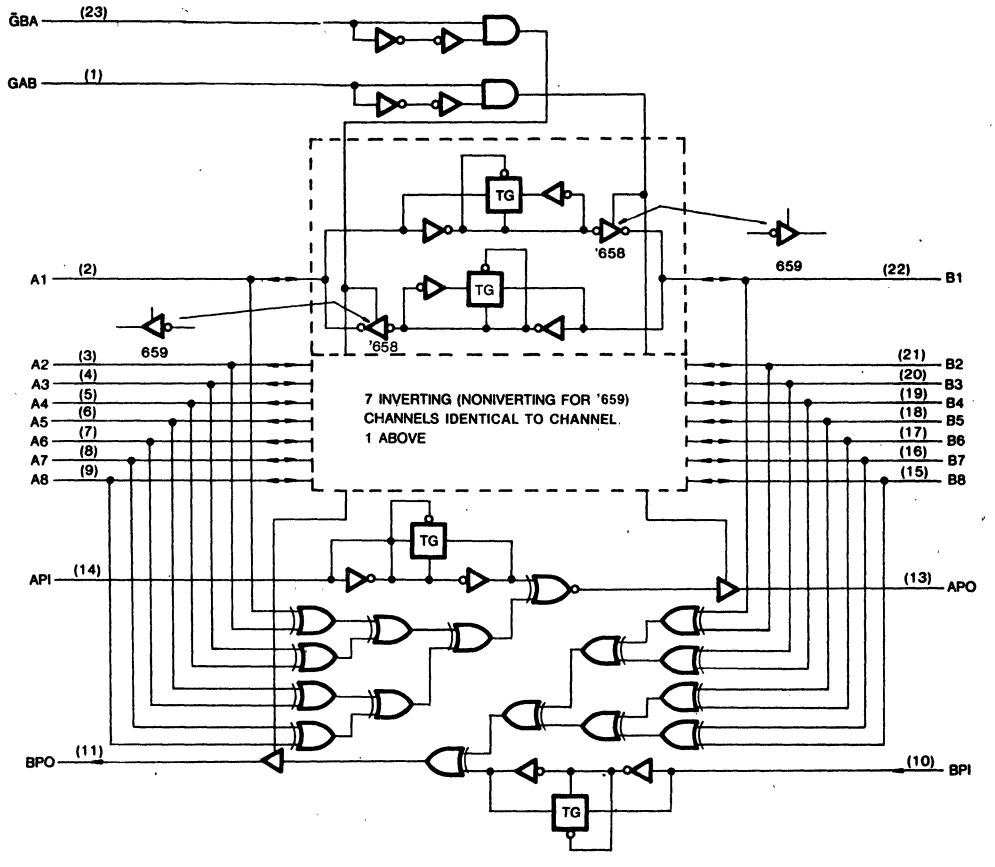
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

CONTROL INPUTS		NUMBER OF HIGH INPUTS ON A BUS AND API	NUMBER OF HIGH INPUTS ON B BUS AND BPI	OUTPUTS		OPERATION	
$\overline{G}BA$	GAB			APO	BPO	HCTLS658	HCTLS659
L	L	X	0, 2, 4, 6, 8	Z	H	B Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
H	H	0, 2, 4, 6, 8	X	H	Z	A Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	L	X	X	Z	Z	Isolation	Isolation
L	H	X	0, 2, 4, 6, 8		H	$\overline{B}$ Data to A Bus, $\overline{A}$ Data to B Bus	B Data to A Bus, A Data to B Bus
		X	1, 3, 5, 7, 9		L		
		0, 2, 4, 6, 8	X	H			
		1, 3, 5, 7, 9	X	L			

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O= −6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS658, HCTLS659

Characteristic	Symbol	Conditions†		T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%		KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V±10%		Unit
				Typ	Guaranteed Limits				
Maximum Propagation Delay, A or B to B or A	t_{PLH}	C_L=50pF		20	25		30	39	ns
		C_L=150pF		23	28		35	45	
	t_{PHL}	C_L=50pF		20	25		30	39	
		C_L=150pF		23	28		35	45	
Maximum Propagation Delay, A or B to B or A	t_{PLH}	C_L=50pF		24	32		40	48	ns
		C_L=150pF		27	35		45	54	
	t_{PHL}	C_L=50pF		24	32		40	48	
		C_L=150pF		27	35		45	54	
Maximum Propagation Delay A or B to APO or BPO	t_{PLH}	C_L=50pF		20	25		30	39	ns
		C_L=150pF		23	28		35	45	
	t_{PHL}	C_L=50pF		20	25		30	39	
		C_L=150pF		23	28		35	45	
Maximum Enable Time, GAB or $\overline{G}$BA to APO or BPO	t_{PZH}	R_L=1kΩ	C_L=50pF	20	25		30	39	ns
			C_L=150pF	23	28		35	45	
	t_{PZL}		C_L=50pF	20	25		30	39	
			C_L=150pF	23	28		35	45	
Maximum Disable Time, GAB or $\overline{G}$BA to APO or BPO	t_{PLZ}	R_L=1kΩ		20	25		30	39	ns
	t_{PHZ}	C_L=50pF		20	25		30	39	ns
Maximum Input Capacitance	C_{IN}			5					pF
Maximum Output Capacitance	C_{OUT}								pF
Power Dissipation Capacitance*	C_{PD}								pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

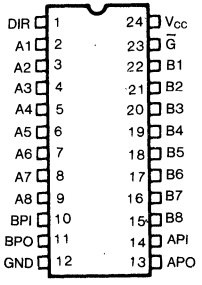
5

Preliminary Specifications

FEATURES

- **Bus Transceivers with Inverting Outputs ('664) or True Outputs ('665)**
- **Generates a Parity Bit for A Bus and B Bus**
- **Easily Cascadable**
- **Internal Active Pull-Ups and Pull-Downs**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input, $\overline{G}$ can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is tht when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry.

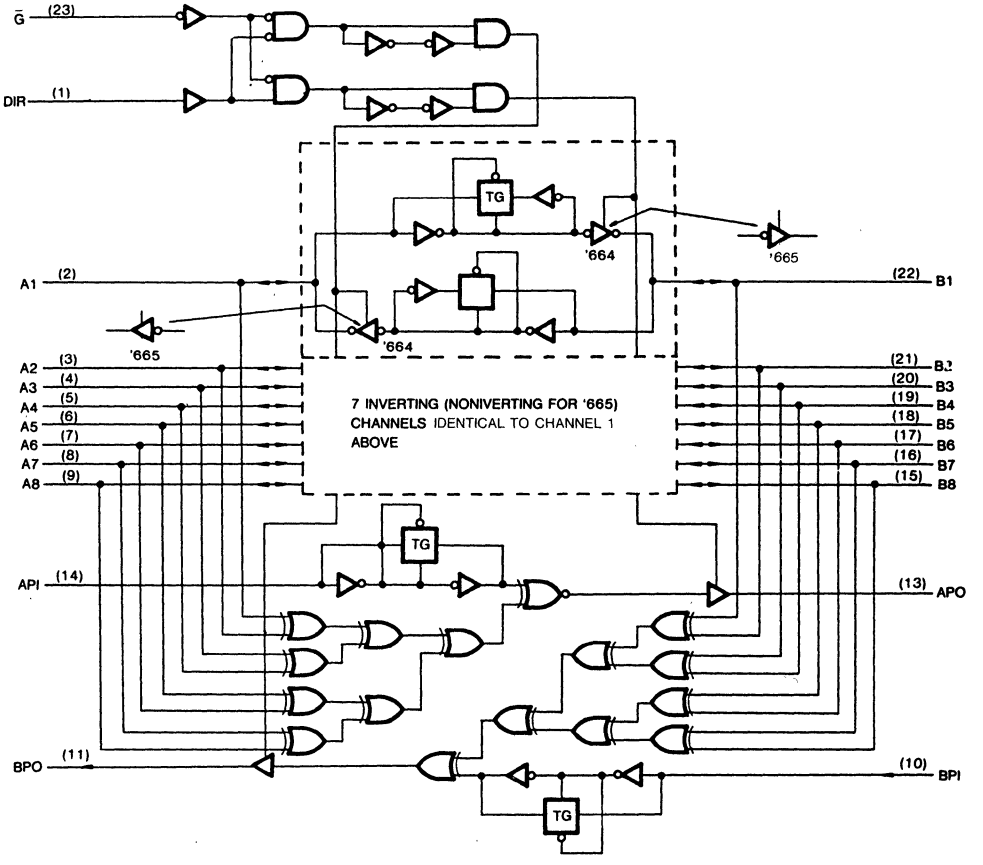
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLE

CONTROL INPUTS		NUMBER OF HIGH INPUTS ON A BUS AND API	NUMBER OF HIGH INPUTS ON B BUS AND BPI	OUTPUTS		OPERATION	
$\overline{G}$	DIR			APO	BPO	'664	'665
L	L	X	0, 2, 4, 6, 8	Z	H	$\overline{B}$ Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
L	H	0, 2, 4, 6, 8	X	H	Z	$\overline{A}$ Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	X	X	X	Z	Z	Isolation	Isolation

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS664/655

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Propagation Delay, A or B to B or A	t_{PLH}	$C_L = 50pF$		20	25	30		39	ns
		$C_L = 150pF$		23	28	35		45	
	t_{PHL}	$C_L = 50pF$		20	25	30		38	
		$C_L = 150pF$		23	28	35		36	
Maximum Propagation Delay, A or B to APO or BPO	t_{PLH}	$C_L = 50pF$		24	32	40		48	ns
		$C_L = 150pF$		27	35	45		54	
	t_{PHL}	$C_L = 50pF$		24	32	40		48	
		$C_L = 150pF$		27	35	45		54	
Maximum Propagation Delay, API or BPI to APO or BPO	t_{PLH}	$C_L = 50pF$		20	25	30		39	ns
		$C_L = 150pF$		23	28	35		45	
	t_{PHL}	$C_L = 50pF$		20	25	30		39	
		$C_L = 150pF$		23	28	35		45	
Maximum Output Enable Time, $\overline{G}$ to A or B	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	24	32	40		48	ns
			$C_L = 150pF$	27	35	45		54	
	t_{PZL}		$C_L = 50pF$	24	32	40		48	
			$C_L = 150pF$	27	35	45		54	
Maximum Output Delay Time, $\overline{G}$ to A or B	t_{PHZ}	$R_L = 1k\Omega$		24	32	40		48	ns
	t_{PLZ}	$C_L = 50pF$		24	22	40		50	
Maximum Output Enable Time DIR to A or B	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	24	32	40		48	ns
			$C_L = 150pF$	27	35	45		54	
	t_{PZH}		$C_L = 50pF$	24	32	40		48	
			$C_L = 150pF$	27	35	45		54	
Maximum Output Disable Time, DIR to A or B	t_{PHZ}	$R_L = 1k\Omega$		20	32	40		48	ns
	t_{HLZ}	$C_L = 50pF$		24	32	40		48	
Maximum Input Capacitance	C_{IN}			5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled		10					pF
Power Dissipation Capacitance*	C_{PD}								pF

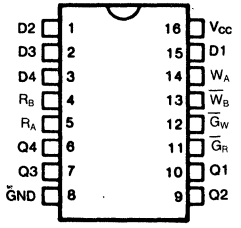
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

5

FEATURES

- **Separate Read/Write Addressing Permits Simultaneous Reading and Writing**
- **Expandable to 512 Words of N-bits**
- **For use as:**
  - **— Scratch pad memory**
  - **— Buffer storage between processors**
  - **— Bit storage in fast multiplication designs**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
  I_{OL} = 8 mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



FUNCTION TABLES

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES[a]
	$\bar{G}_W$	D_n	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

NOTE:

a. The Write Address (W_A and W_B) to the "Internal latches" must be stable while $\bar{G}_W$ is LOW for conventional operation.

DESCRIPTION

The '670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable Inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the write enable ($\bar{G}_W$) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\bar{G}_W$ is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when $\bar{G}_W$ is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs ($\overline{R_A}$ and R_B). The addrssed word appears at the four outputs when the read enable ($\bar{G}_R$) is LOW. Data outputs are in the HIGH impedance "off" state when the read enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull-up resistors to the outputs to increase the I_{OH} current available. Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

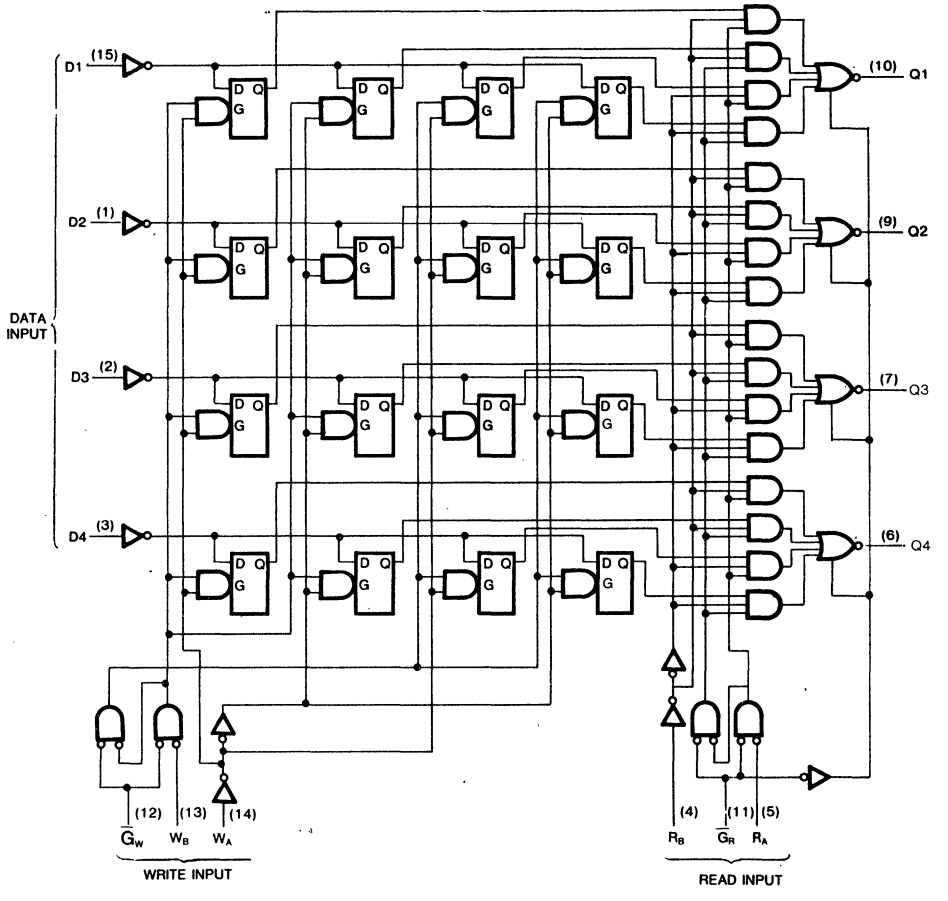
READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT Q_n
	$\bar{G}_R$	INTERNAL LATCHES[b]	
Read	L	L	L
	L	H	H
Disabled	H	H	(Z)

NOTE:

b. The selection of the "internal latches" by Read Address ($\overline{R_A}$ and R_B) are not constrained by $\bar{G}_W$ or $\bar{G}_R$ operation.

LOGIC DIAGRAM



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS • T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS670

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ		Guaranteed Limits		
Maximum Propagation Delay, R_A or R_B to Output	t_{PLH}	$C_L = 50pF$		20	32	40	48	ns
		$C_L = 150pF$		23	35	45	54	
	t_{PHL}	$C_L = 50pF$		20	32	40	48	
		$C_L = 150pF$		23	35	45	54	
Maximum Propagation Delay, $\overline{G}_W$ to Output	t_{PLH}	$C_L = 50pF$		27	36	45	59	ns
		$C_L = 150pF$		30	39	50	65	
	t_{PHL}	$C_L = 50pF$		27	36	45	59	
		$C_L = 150pF$		30	39	50	65	
Maximum Propagation Delay, Data to Output	t_{PLH}	$C_L = 50pF$		27	36	45	59	ns
		$C_L = 150pF$		30	39	50	65	
	t_{PHL}	$C_L = 50pF$		27	36	45	54	
		$C_L = 150pF$		30	39	50	60	
Maximum Output Enable Time, $\overline{G}_R$ to Output	t_{PZH}	$R_L = 1k\Omega$	$C_L = 50pF$	24	32	40	48	ns
			$C_L = 150pF$	27	35	45	54	
	t_{PZL}		$C_L = 50pF$	24	32	40	48	
			$C_L = 150pF$	27	35	45	54	
Maximum Output Disable Time, $\overline{G}_R$ to Output	t_{PHZ}	$R_L = 1k\Omega$		24	32	40	48	ns
	t_{PLZ}	$C_L = 150pF$		24	32	40	48	
Maximum Input Capacitance	C_{IN}			5				pF
Maximum Output Capacitance	C_{OUT}	Output disabled		10				pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

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Preliminary Specifications

FEATURES

- **'679: 12-bit to 4-bit comparator with enable**
- **'680: 12-bit to 4-bit comparator with latch**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges; KS74HCTLS: −40°C to +85°C KS54HCTLS: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

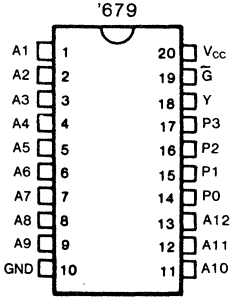
The '679 and '680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

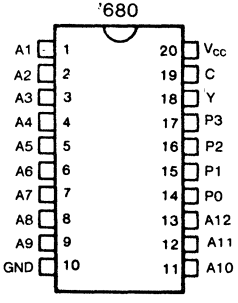
The '679 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs. The '680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

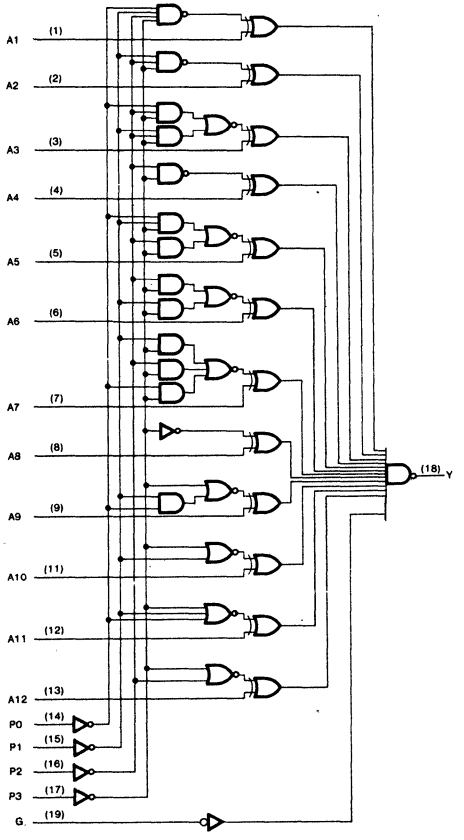
PIN CONFIGURATIONS



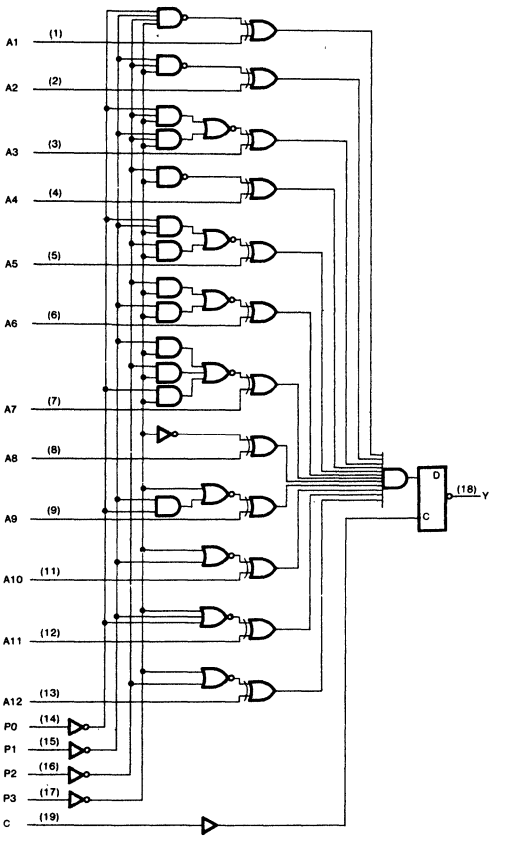


LOGIC DIAGRAMS

'679



'680



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FUNCTION TABLE

'679	'680	INPUTS COMMON TO '679 AND '680																OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L*
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	H	H	L	L*
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L*
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	All other combinations																H
H		'679: Any combination																H
	L	'680: Any combination																Latched

* These three rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for all combinations in which P=12, 13 and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P≥9 to P=9 ... 11/13 ... 15, P≥10 to P=10/11/14/15, and P≥11 to P=11/15.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS679

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, Any P to Y	t_{PLH}	C_L=50pF	24	32	40	48	ns
		C_L=150pF	27	35	45	54	
	t_{PHL}	C_L=50pF	27	32	40	48	
		C_L=150pF	30	35	45	54	
Maximum Propagation Delay, Any A to Y	t_{PLH}	C_L=50pF	21	28	35	42	ns
		C_L=150pF	24	31	40	48	
	t_{PHL}	C_L=50pF	21	28	35	42	
		C_L=150pF	24	31	40	48	
Maximum Propagation Delay, G to Y	t_{PLH}	C_L=50pF	18	24	30	36	ns
		C_L=150pF	21	27	35	42	
	t_{PHL}	C_L=50pF	18	24	30	36	
		C_L=150pF	21	27	35	42	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS680

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, Any P to Y	t_{PLH}	$C_L = 50pF$	27	36	45	54	ns
		$C_L = 150pF$	30	39	50	60	
	t_{PHL}	$C_L = 50pF$	27	32	40	48	
		$C_L = 150pF$	30	35	45	64	
Maximum Propagation Delay, Any A to Y	t_{PLH}	$C_L = 50pF$	24	32	40	48	ns
		$C_L = 150pF$	27	35	45	64	
	t_{PHL}	$C_L = 50pF$	24	32	40	48	
		$C_L = 150pF$	27	35	45	64	
Maximum Propagation Delay, C to Y	t_{PLH}	$C_L = 50pF$	19	26	32	38	ns
		$C_L = 150pF$	22	29	37	44	
	t_{PHL}	$C_L = 50pF$	19	26	32	38	
		$C_L = 150pF$	22	29	37	44	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Compares Two 8-Bit Words**
- **'682 has 20kΩ pull-up Resistors on the Q Inputs**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High drive current outputs:**
  (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

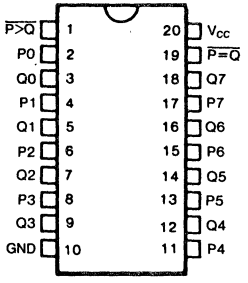
These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overline{P=Q}$ and $\overline{P>Q}$ outputs. The '682 features 20-kΩ pull-up termination resistors on the Q inputs for analog or switch data.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

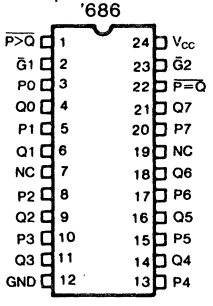
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS

'682 and '684



'686



NC—No internal connection

FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES			
P, Q	$\overline{G1}$	$\overline{G2}$	$\overline{P=Q}$	$\overline{P>Q}$
P=Q	L	X	L	H
P>Q	X	L	H	L
P<Q	X	X	H	H
P=Q	H	X	H	H
P>Q	X	H	H	H
X	H	H	H	H

NOTES: 1. The last 3 lines of the function table apply only to the device having enable inputs, i.e., '686.
2. The $\overline{P<Q}$ function can be generated by applying the $\overline{P=Q}$ and $\overline{P>Q}$ outputs to a 2-input NAND gate.

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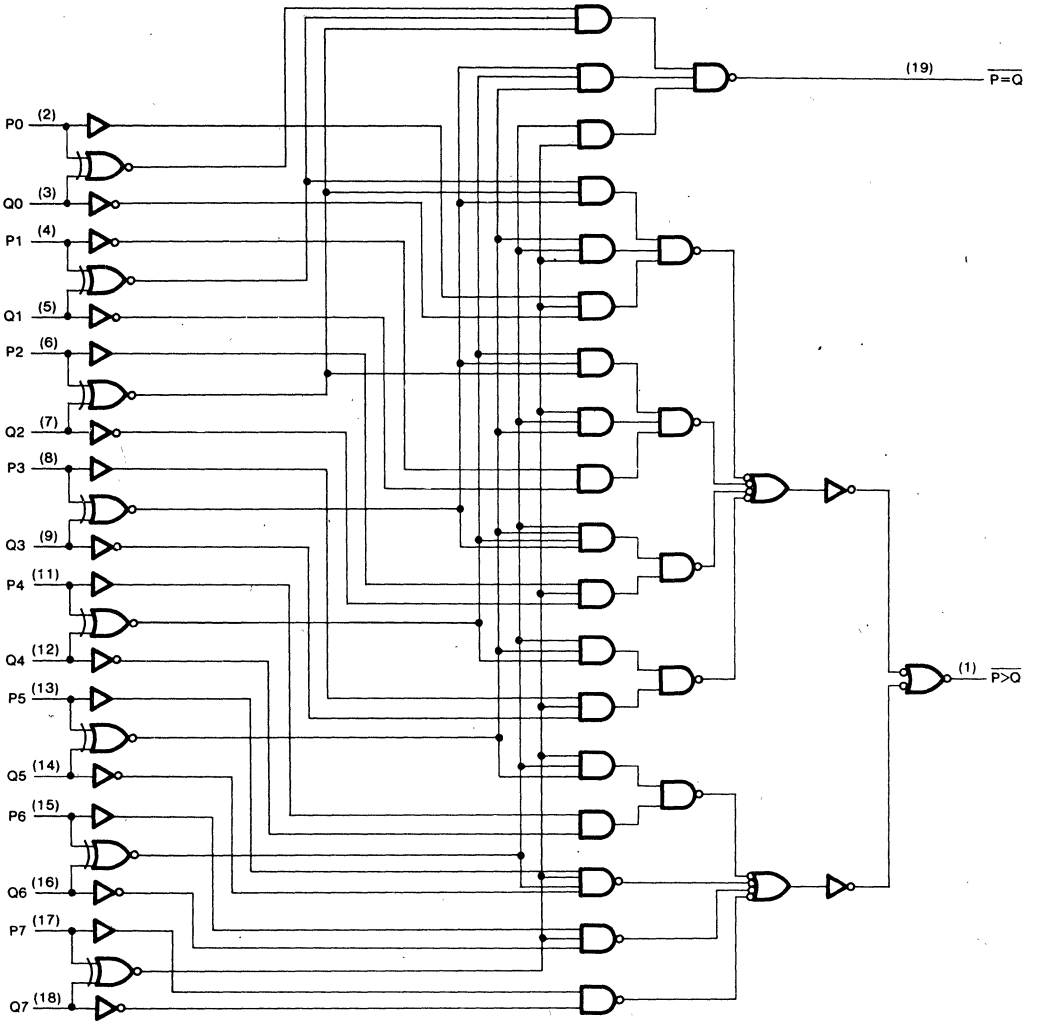
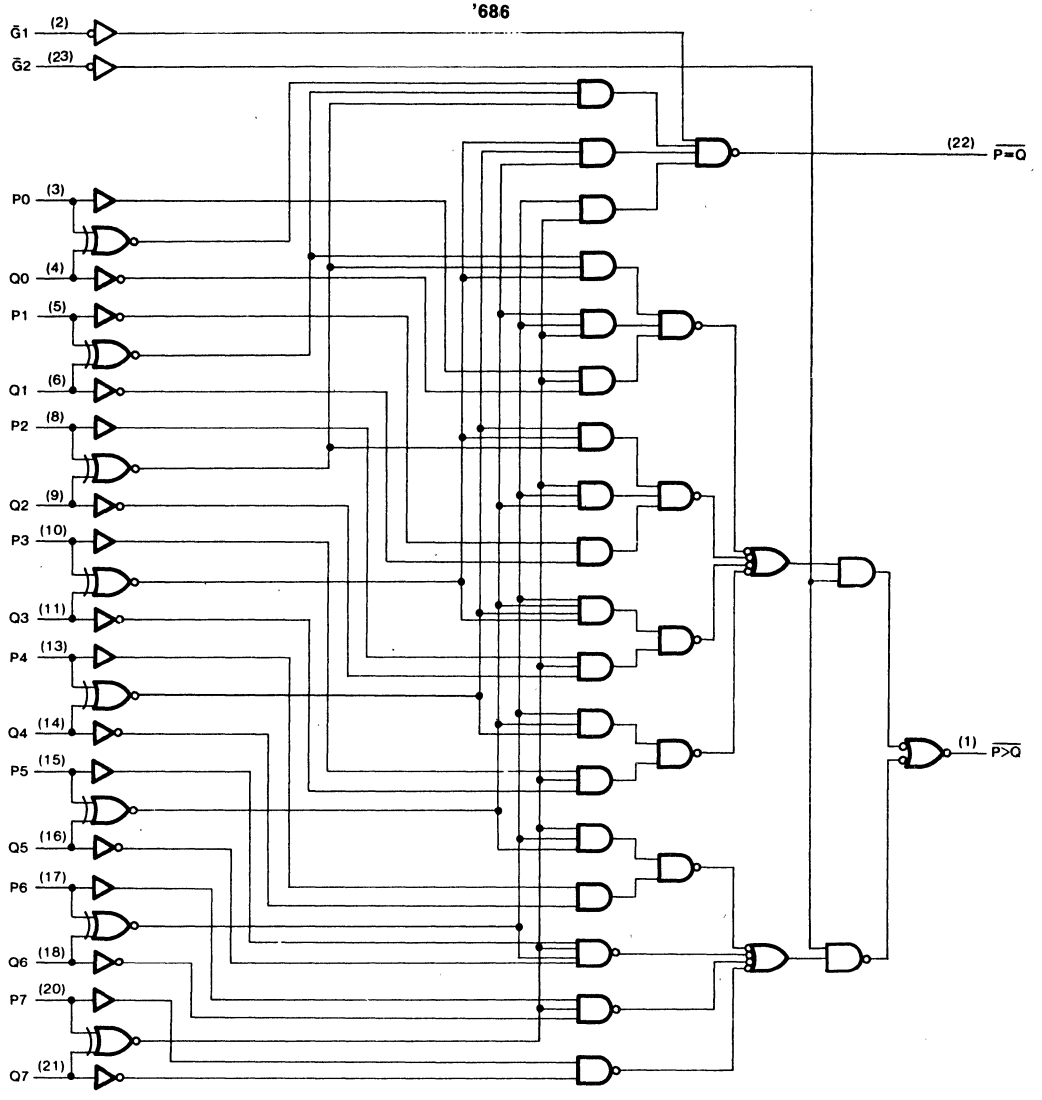
LOGIC DIAGRAMS

'682 or '684



LOGIC DIAGRAMS (continued)



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Parameter	Symbol	Test Conditions	T_A=25°C		KS74AHCT T_A=−40°C to +85°C	54AHCT T_A=−55°C to +125°C	Unit
			Typ		Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (Totem-pole Outputs)	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.93	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage (All Outputs)	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current, ('682 Q Inputs)		V_{CC}=Max V_{IN}=2.7V V_{IN}=0.4V		−0.2 −0.4	−0.2 −0.4	−0.2 −0.4	mA
Maximum Input Current (All other Inputs)	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	For '682: V_{IN}=GND (Q0-Q7) V_{IN}=V_{CC} or GND (all other inputs)		3.5	3.5	3.5	mA
		For '684 and '688 V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS682, HCTLS684, HCTLS686

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, P or Q to $\overline{P=Q}$	t_{PLH}	$C_L=50pF$	18	25	31	38	ns
		$C_L=150pF$	21	28	36	44	
	t_{PHL}	$C_L=50pF$	18	25	31	38	
		$C_L=150pF$	21	28	36	44	
Maximum Propagation Delay, P or Q to $\overline{P>Q}$	t_{PLH}	$C_L=50pF$	22	32	38	45	ns
		$C_L=150pF$	25	35	43	51	
	t_{PHL}	$C_L=50pF$	22	30	38	45	
		$C_L=150pF$	25	33	43	51	
Maximum Propagation Delay, $\overline{G1}$ to $\overline{P=Q}$ ('686 Only)	t_{PLH}	$C_L=50pF$	15	20	25	30	ns
		$C_L=150pF$	18	23	30	36	
	t_{PHL}	$C_L=50pF$	15	20	25	30	
		$C_L=150pF$	18	23	30	36	
Maximum Propagation Delay, $\overline{G2}$ to $\overline{P<Q}$ ('686 Only)	t_{PLH}	$C_L=50pF$	18	25	31	38	ns
		$C_L=150pF$	21	28	36	44	
	t_{PHL}	$C_L=50pF$	18	25	31	38	
		$C_L=150pF$	21	28	36	44	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

5

FEATURES

- **Compares Two 8-Bit Words**
- **Choice of Totem-pole ('688) and open-drain ('689) outputs ('688 is identical to '521)**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High drive current outputs:**
  (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

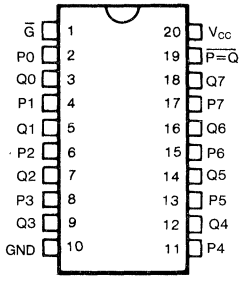
DESCRIPTION

These identity comparators perform comparisons of two 8-bit binary or BCD words. The output of '688 is totem-pole while '689's are open-drain.

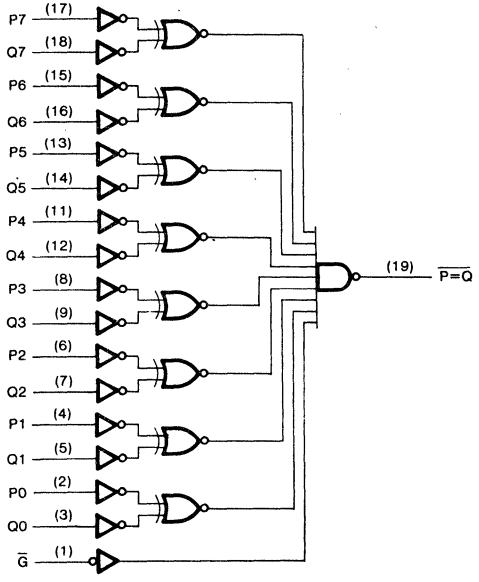
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM (Positive Logic)



FUNCTION TABLE

INPUTS		OUTPUT
DATA P.Q	ENABLE $\overline{G}$	$\overline{P=Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} +0.5V$) . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} +0.5V$) . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} +0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage ('688 only)	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current ('689 only)	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS688

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, P to $\overline{P=Q}$	t_{PLH}	$C_L = 50pF$	16	22	28	33	ns
		$C_L = 150pF$	19	25	33	39	
	t_{PHL}	$C_L = 50pF$	16	22	28	33	
		$C_L = 150pF$	19	25	33	39	
Maximum Propagation Delay, Q to $\overline{P=Q}$	t_{PLH}	$C_L = 50pF$	16	22	28	33	ns
		$C_L = 150pF$	19	25	33	39	
	t_{PHL}	$C_L = 50pF$	16	22	28	33	
		$C_L = 150pF$	19	25	33	39	
Maximum Propagation Delay, $\overline{G}$ to $\overline{P=Q}$	t_{PLH}	$C_L = 50pF$	15	20	25	30	ns
		$C_L = 150pF$	18	23	30	36	
	t_{PHL}	$C_L = 50pF$	15	20	25	30	
		$C_L = 150pF$	18	23	30	36	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS689

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay, P to $\overline{P=Q}$	t_{PLH}	$C_L = 50pF$	24	31	37	43	ns
		$C_L = 150pF$	27	34	42	49	
	t_{PHL}	$C_L = 50pF$	19	26	32	38	
		$C_L = 150pF$	22	29	37	44	
Maximum Propagation Delay, Q to $\overline{P=Q}$	t_{PLH}	$C_L = 50pF$	24	31	37	43	ns
		$C_L = 150pF$	27	34	42	49	
	t_{PHL}	$C_L = 50pF$	19	26	32	38	
		$C_L = 150pF$	22	29	37	44	
Maximum Propagation Delay, $\overline{G}$ to $\overline{P=Q}$	t_{PLH}	$C_L = 50pF$	23	29	35	41	ns
		$C_L = 150pF$	27	32	40	47	
	t_{PHL}	$C_L = 50pF$	18	24	30	36	
		$C_L = 150pF$	21	27	35	42	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

FEATURES

- **I/O port configuration enables output data back onto input bus**
- **Latch ('793) and and Register ('794) options**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

These are 8-bit latches/registers that allow temporary storage and retrieval of data on a bus. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in a '793 or '794, for verification and/or updating.

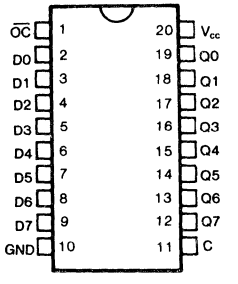
The data is loaded in the registers on the positive-edge of the clock (CLK) for the '794. The data is passed through the '793 when C is high, and it is latched when C goes low The output control ($\overline{OC}$) is used to enable data on the D0-D7 pins. when $\overline{OC}$ is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When $\overline{OC}$ is high, D0-D7 are inputs to the latches/registers configuring D as an input bus.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

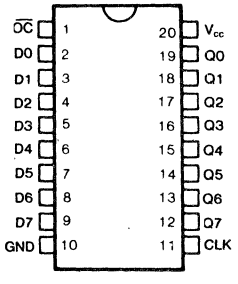
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS

'793



'794



FUNCTION TABLES

'793

C	$\overline{OC}$	Q	D
L	L	Q_O**	Output, Q
L	H	Q_O**	Input
H†	L	D*	Output, Q*
H	H	D	Input

* In this case the output of the latch feeds the input, and a "race" condition results.

** Q_O represents the previous "latched" state.

† This transition is not a normal mode of operation and may produce hazards.

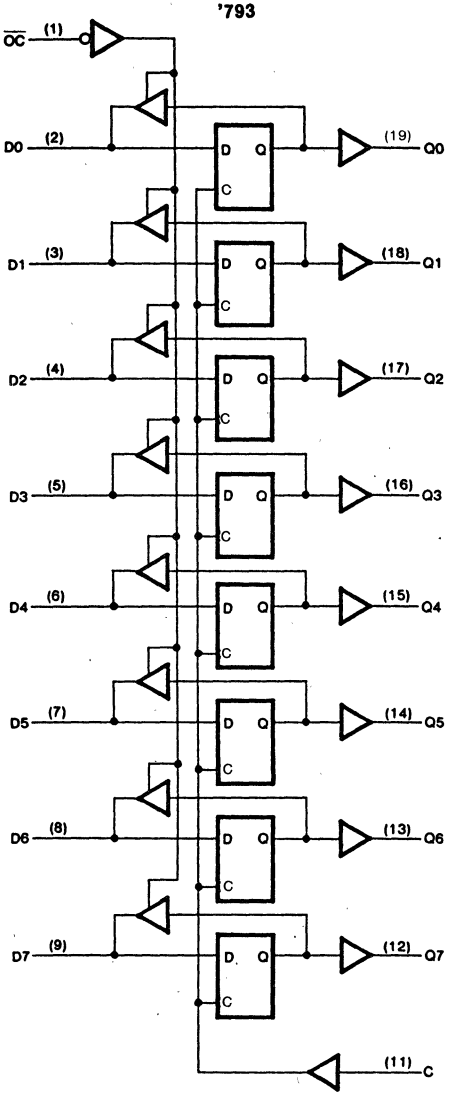
'794

CLK	$\overline{OC}$	Q	D
L or H or ↓	L	Q_O	Output, Q
L or H or ↓	H	Q_O	Input
↑	L	Q_O	Output, Q*
↑	H	D	Input

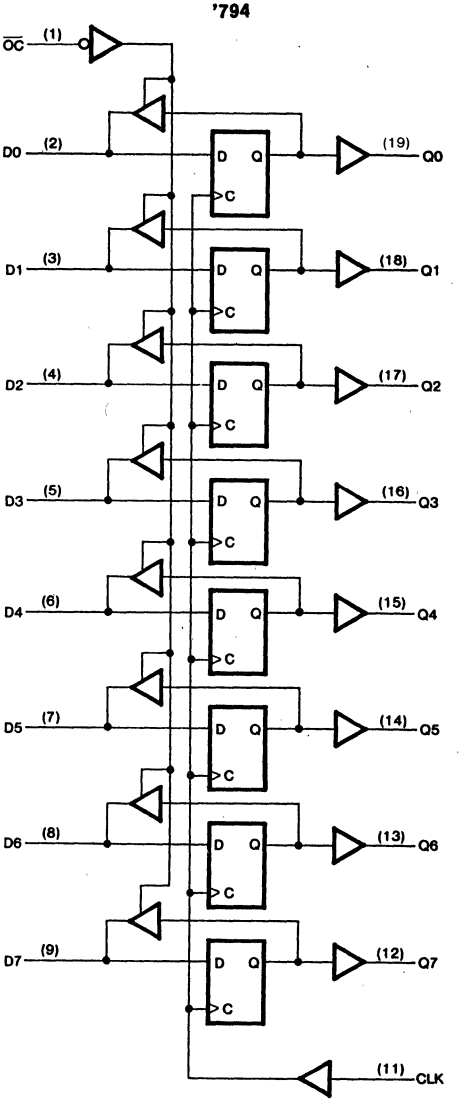
* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_O.

LOGIC DIAGRAMS

'793



'794



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS793, 794

Characteristic		Symbol	Conditions†	$T_a=25°C$ $V_{CC}=5.0V$	KS74HCTLS $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54HCTLS $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency ('794 only)		t_{max}	$C_L=50pF$	50	40		35	30	MHz
Maximum Propagation Delay, D to Any Q ('793 only)		t_{PLH}	$C_L=50pF$	14	18		23	27	ns
			$C_L=150pF$	17	21		28	33	
		t_{PHL}	$C_L=50pF$	14	18		23	27	
			$C_L=150pF$	17	21		28	33	
Maximum Propagation Delay, CLK/C to Any Q		t_{PLH}	$C_L=50pF$	15	20		25	30	ns
			$C_L=150pF$	18	23		30	36	
		t_{PHL}	$C_L=50pF$	15	20		25	30	
			$C_L=150pF$	18	23		30	36	
Maximum Enable Time, $\overline{OC}$ to D		t_{PZH}	$R_L=1k\Omega$ (C=Low for '793) $C_L=50pF$	15	20		25	30	ns
			$C_L=150pF$	18	23		30	36	
		t_{PZL}	$C_L=50pF$	15	20		25	30	
			$C_L=150pF$	18	23		30	36	
Maximum Disable Time, $\overline{OC}$ to D		t_{PHZ}	$R_L=1k\Omega$, $C_L=50pF$ (C=Low for '793)	15	20		25	30	ns
		t_{PLZ}		15	20		25	30	
Minimum Pulse Width, CLK/C High or low		t_w		10	15		18	20	ns
Minimum Setup Time	D before C↓ ('793)	t_{su}		8	10		13	15	ns
	D before CLK↑('794)			10	15		18	20	
Minimum Hold Time	D after C↓ ('793)	t_h		8	10		13	15	ns
	D after CLK↑ ('794)			−3	0		0	0	
Maximum Input Capacitance		C_{IN}		5					pF
Maximum Output Capacitance		C_{OUT}		10					pF
Power Dissipation Capacitance*		C_{PD}							ns

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS/KS74HCTLS 821/822

10-Bit Bus Interface Flip-Flops with 3-State Outputs

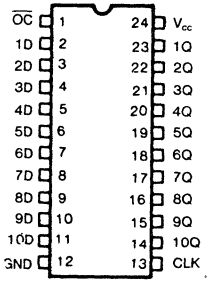
Preliminary Specifications

FEATURES

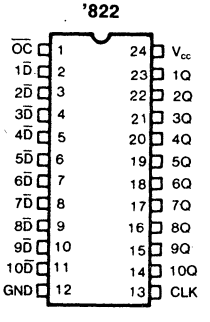
- **Functionally Equivalent to AMD's Am29821 and Am29822**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Power-Up High-Impedance State**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'821



'822



DESCRIPTION

These 10-bit bus-interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

All of the flip-flops are edge-triggered and D-type. On the positive transition of the clock the Q outputs on the '821 will be true, and on the '822 will be complementary to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

(Each Flip-Flop)

'821

Inputs			Output
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
L	H	X	Q_0
H	X	X	Z

'822

Inputs			Output
$\overline{OC}$	CLK	$\overline{D}$	Q
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
L	H	X	Q_0
H	X	X	Z

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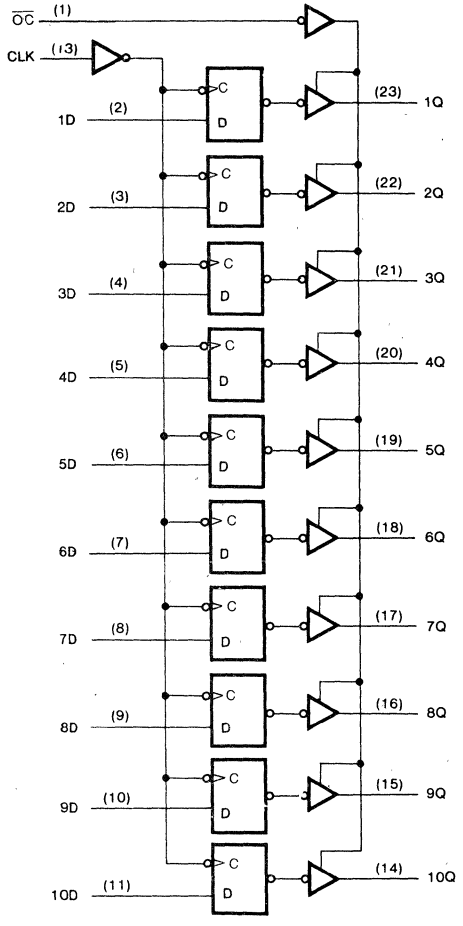
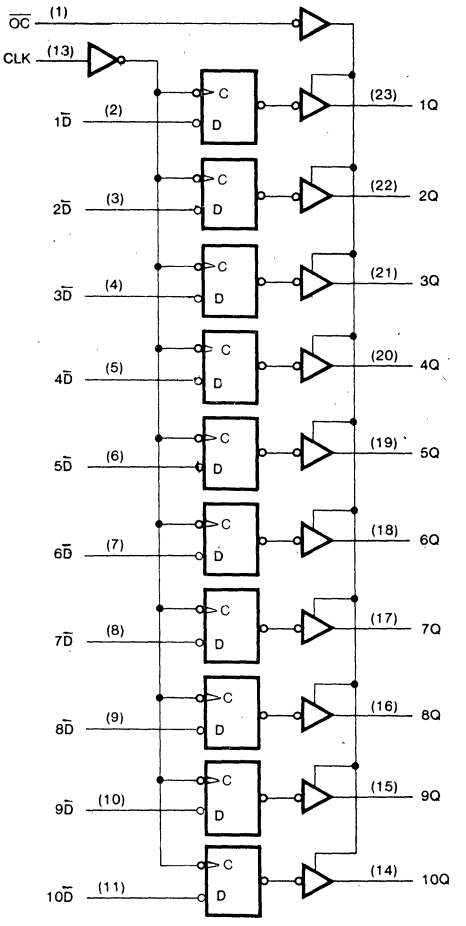
LOGIC DIAGRAMS

'821



'822



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} . . . . . −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS821, HCTLS822

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits				
Maximum Operating Frequency	f_{max}	$C_L = 50pF$	40	35		30	25	MHz
Maximum Propagation Delay, CLK to any Q	t_{PLH}	$C_L = 50pF$	15	20		25	30	ns
		$C_L = 150pF$	18	23		30	36	
	t_{PHL}	$C_L = 50pF$	15	20		25	30	
		$C_L = 150pF$	18	23		30	36	
Maximum Output Enable Time, $\overline{OC}$ to any Q	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$	18	24		30	36	ns
		$R_L = 1k\Omega$, $C_L = 150pF$	21	27		35	42	
	t_{PZL}	$R_L = 1k\Omega$, $C_L = 50pF$	18	24		30	36	
		$R_L = 1k\Omega$, $C_L = 150pF$	21	27		35	42	
Maximum Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	$R_L = 1k\Omega$, $C_L = 50pF$	18	24		30	36	ns
	t_{PLZ}		18	24		30	36	
Minimum Pulse Width, CLK High or Low	t_w		12	16		20	24	ns
Minimum Setup Time, Data before CLK↑	t_{su}		12	16		20	24	ns
Minimum Hold Time, Data after CLK↑	t_h		−3	0		0	0	ns
Maximum Input Capacitance	C_{IN}		5					pF
Maximum Output Capacitance	C_{OUT}	$\overline{OC} = V_{CC}$	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC} = V_{CC}$	5					pF
		$\overline{OC} = GND$	10					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS / KS74HCTLS 823/824

9-Bit Bus Interface Flip-Flops with 3-State Outputs

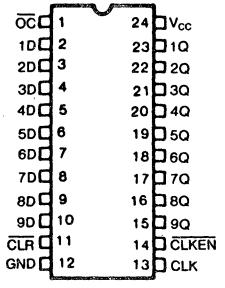
Preliminary Specifications

FEATURES

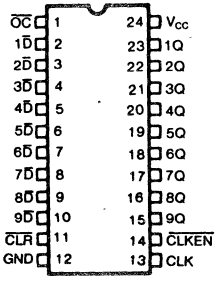
- **Functionally Equivalent to AMD's Am29823 and Am29824**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Power-Up High-Impedance State**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'823



'824



DESCRIPTION

These 9-bit bus interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable ($\overline{CLKEN}$) low, the D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The '823 has noninverting D inputs and the '824 has inverting D inputs. Taking the $\overline{CLR}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ($\overline{OC}$) can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

'823

INPUT					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'824

INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

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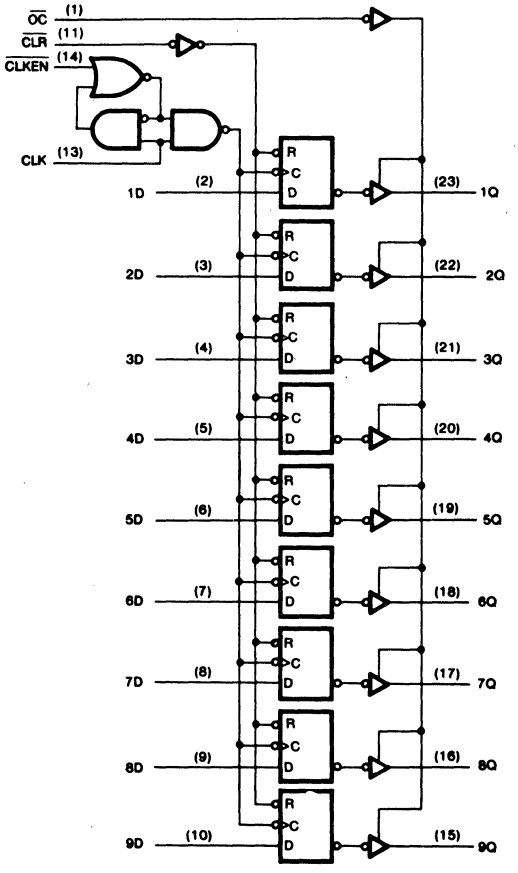
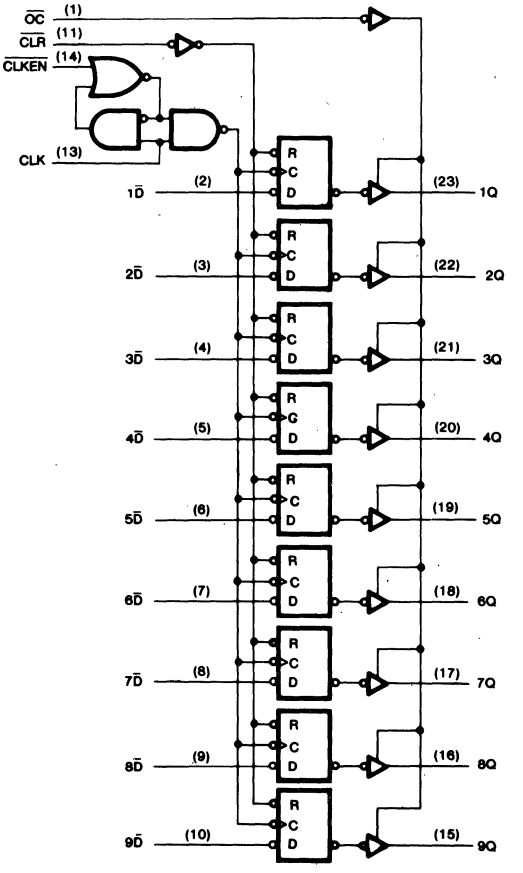
LOGIC DIAGRAMS

'823



'824



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5 to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS823, HCTLS824

Characteristic	Symbol	Conditions†	$T_A=25°C$ $V_{CC}=5.0V$	KS74HCTLS $T_A=-40°C$ to $+85°C$ $V_{CC}=5.0V\pm10\%$		KS54HCTLS $T_A=-55°C$ to $+125°C$ $V_{CC}=5.0V\pm10\%$		Unit
			Typ	Guaranteed Limits				
Maximum Operating Frequency	f_{max}	$C_L=50pF$	40	35		30	25	MHz
Maximum Propagation Delay, CLK to any Q	t_{PLH}	$C_L=50pF$	15	20		25	30	ns
		$C_L=150pF$	18	23		30	36	
	t_{PHL}	$C_L=50pF$	15	20		25	30	
		$C_L=150pF$	18	23		30	36	
Maximum Propagation Delay, CLR to Any Q	t_{PLH}	$C_L=50pF$	17	22		28	34	ns
		$C_L=150pF$	20	25		33	40	
Maximum Output Enable Time, $\overline{OC}$ to any Q	t_{PZL}	$R_L=1k\Omega$, $C_L=50pF$	18	24		30	36	ns
		$C_L=150pF$	21	27		35	42	
	t_{PZL}	$C_L=50pF$	18	24		30	36	
		$C_L=150pF$	21	27		35	42	
Maximum Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	$R_L=1k\Omega$	18	24		30	36	ns
	t_{PLZ}	$C_L=50pF$	18	24		30	36	
Minimum Pulse Width $\overline{CLR}$ Low	t_w		12	16		20	24	ns
Minimum Pulse Width CLK high or Low			12	16		20	24	
Minimum Setup Time Before CLK↑ $\overline{CLR}$ Inactive	t_{su}		12	16		20	24	ns
Minimum Setup Time Before CLK↑ Bata			12	16		20	24	
Minimum Setup Time Before CLK↑ $\overline{CLKEN}$ high or Low			12	16		20	24	
Minimum Hold Time, $\overline{CLKEN}$ or data after CLK↑	t_h		−3	0		0	0	ns
Maximum Input Capacitance	C_{IN}		5					pF
Maximum Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	OC=V_{CC}	5					pF
		OC=GND	30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD}\,V_{CC}^2\,f + I_{CC}\,V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

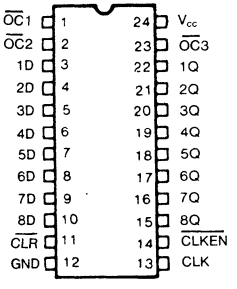
Preliminary Specifications

FEATURES

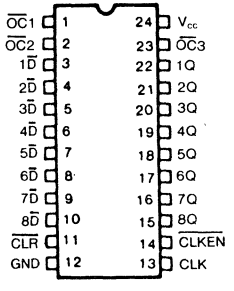
- **Functionally Equivalent to AMD's Am29825 and Am29826**
- **Improved I_{OH} Specifications**
- **Multiple Output Enables Allow Multiuser Control of the Interface**
- **Power-Up High-Impedance State**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'825



'826



DESCRIPTION

These 8-bit bus interface flip-flops leature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing multiuser buffer registers, I/O ports, bidirectional bus drivers and working registers.

With the clock enable ($\overline{CLKEN}$) low, all D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The '825 has non-inverting D inputs and the '826 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ inputs low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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FUNCTION TABLES

'825

Inputs					Output
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

* OC = H if any of OC1, OC2, or OC3 are high.
OC = L of OC1, OC2, and OC3 are low.

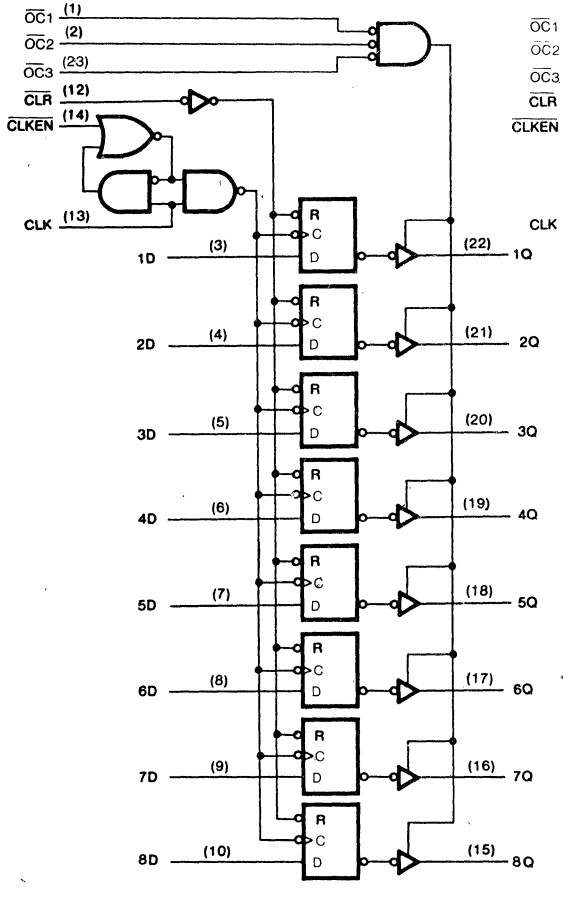
'826

Inputs					Output
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

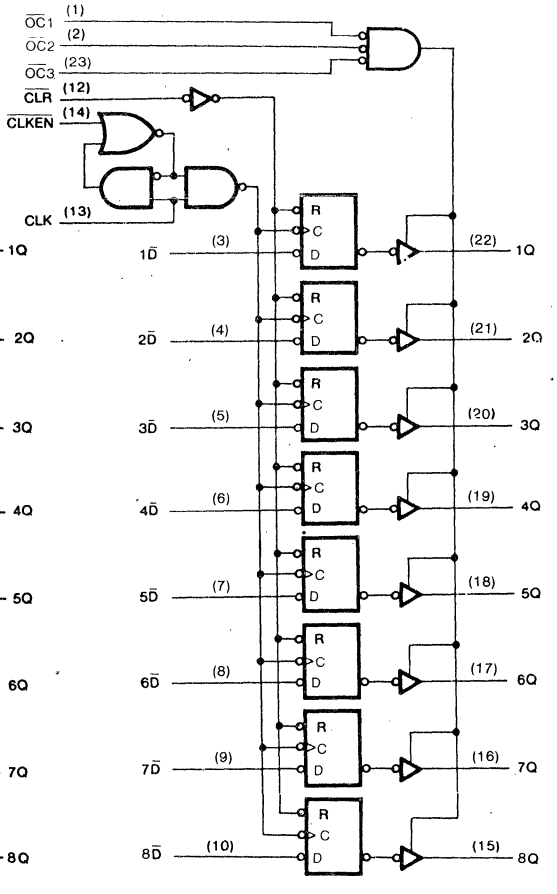
* OC = H if any of OC1, OC2, or OC3 are high.
OC = L of OC1, OC2, and OC3 are low.

LOGIC DIAGRAMS

'825



'826



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS825, HCTLS826

Characteristic		Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
					Typ	Guaranteed Limits				
Maximum Operating Frequency		f_{max}	$C_L = 50pF$		40	35		30		MHz
Maximum Propagation Delay, CLK to any Q		t_{PLH}	$C_L = 50pF$		15	20		25		ns
			$C_L = 150pF$		18	23		30		
		t_{PHL}	$C_L = 50pF$		15	20		25		
			$C_L = 150pF$		18	23		30		
Maximum Propagation Delay, $\overline{CLR}$ to Any Q		t_{PLH}	$C_L = 50pF$		17	22		28		ns
			$C_L = 150pF$		20	25		33		
Maximum Output Enable Time, $\overline{OC}$ to any Q		t_{PZL}	$R_L = 1k\Omega$	$C_L = 50pF$	18	24		30		ns
				$C_L = 150pF$	21	27		35		
		t_{PZL}	$R_L = 1k\Omega$	$C_L = 50pF$	18	24		30		
				$C_L = 150pF$	21	27		35		
Maximum Output Disable Time, $\overline{OC}$ to any Q		t_{PHZ}	$R_L = 1k\Omega$ $C_L = 50pF$		18	24		30		ns
		t_{PLZ}			18	24		30		
Minimum Pulse Width	$\overline{CLR}$ Low	t_w			12	16		20		ns
	CLK high or Low				12	16		20		
Minimum Setup Time Before CLK↑	$\overline{CLR}$ Inactive	t_{su}			12	16		20		ns
	Data				12	16		20		
	$\overline{CLKEN}$ high or Low				12	16		20		
Minimum Hold Time, $\overline{CLKEN}$ or data after CLK↑		t_h			−3	0		0		ns
Maximum Input Capacitance		C_{IN}			5					pF
Maximum Output Capacitance		C_{OUT}			10					pF
Power Dissipation Capacitance* (per stage)		C_{PD}			5 30					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

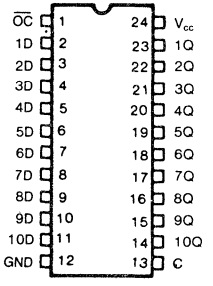
Preliminary Specifications

FEATURES

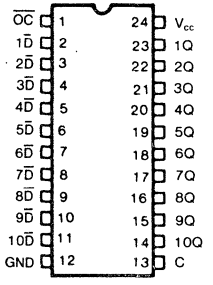
- **Bus-Structured Pinout**
- **Provides Extra Bus Driving Latches**
- **Necessary for Wider Address/Data Paths or Busses with Parity**
- **Power-Up High-Impedance State**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'841



'842



DESCRIPTION

These 10-bit bus interface latches feature three state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers. I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The '841 has noninverting data (D) inputs and the '842 has inverting ($\overline{D}$) inputs.

A buffered output control ($\overline{OC}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

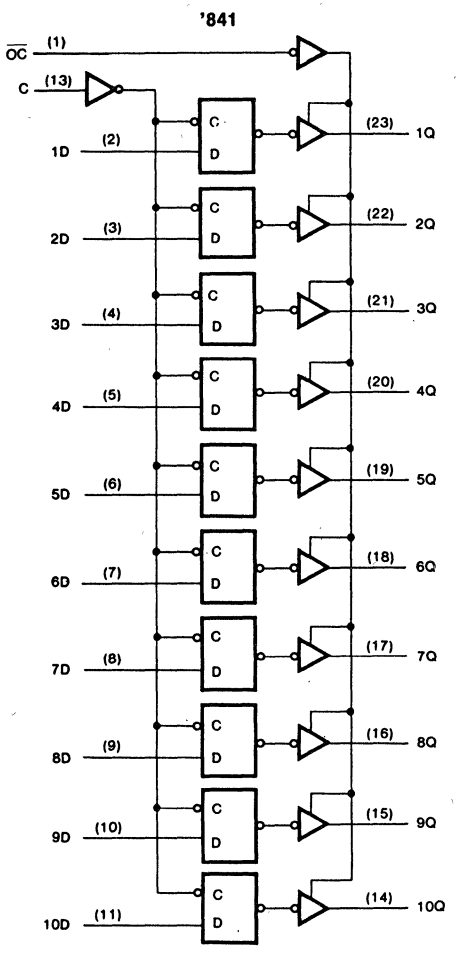
'841

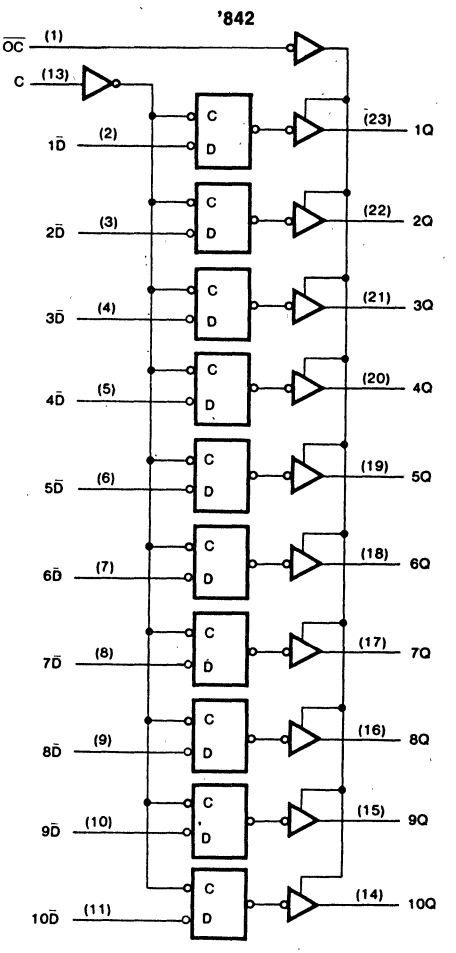
INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'842

INPUTS			OUTPUT
$\overline{OC}$	C	$\overline{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS841, HCTLS842

Characteristic	Symbol	Conditions†		$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Propagation Delay, Data to Q	t_{PLH}	C_L= 50pF		15	20	25		30	ns
		C_L=150pF		18	23	30		36	
	t_{PHL}	C_L=50pF		15	20	25		30	
		C_L=150pF		18	23	30		36	
Maximum Propagation Delay, C to any Q	t_{PLH}	C_L=50pF		21	28	35		42	ns
		C_L=150pF		24	31	40		48	
	t_{PHL}	C_L=50pF		21	28	35		42	
		C_L=150pF		24	31	40		48	
Maximum Output Enable Time, $\overline{OC}$ to any Q	t_{PZH}	R_L=1kΩ	C_L=50pF	18	24	30		36	ns
			C_L=150pF	21	27	35		42	
	t_{PZL}		C_L=50pF	18	24	30		36	
			C_L=150pF	21	27	35		42	
Maximum Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	R_L=1kΩ		18	24	30		36	ns
	t_{PLZ}	C_L=50pF		18	24	30		36	
Minimum Pulse Width, C High	t_w			15	20	25		30	ns
Minimum Setup Time, Data before C↓	t_{su}			12	16	20		24	ns
Minimum Hold Time, Data after C↓	t_h			6	8	10		12	ns
Maximum Input Capacitance	C_{IN}			5					pF
Maximum Output Capacitance	C_{OUT}			10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{OC}$=V_{CC}		5					pF
		$\overline{OC}$=GND		30					

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

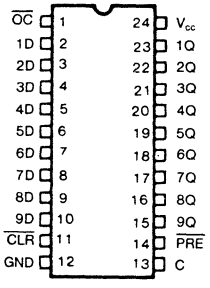
Preliminary Specifications

FEATURES

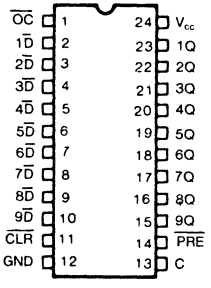
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Power-Up High Impedance**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'843



'844



DESCRIPTION

These 9-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

The nine latches are transparent D-type. The '843 has noninverting data (D) inputs and the '844 has inverting $\overline{D}$ inputs.

A buffered output control ($\overline{OC}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

'843

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

'844

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	$\overline{D}$	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	Q_0
X	X	H	X	X	Z

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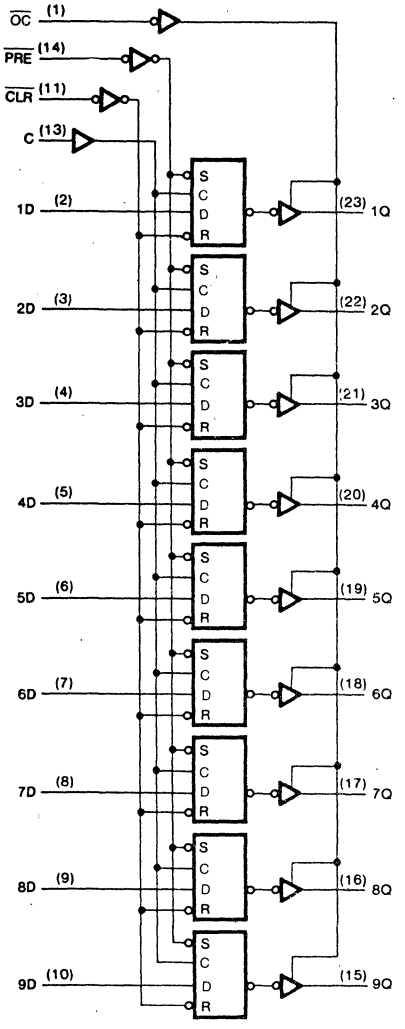
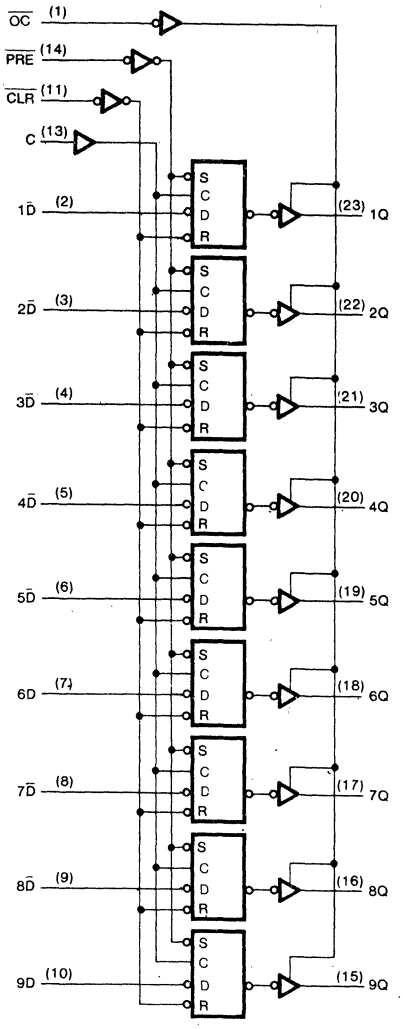
LOGIC DIAGRAMS

'843



'844



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS843, HCTLS844

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$ Typ	$T_a = 25°C$ $V_{CC} = 5.0V$ Guaranteed Limits	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
Maximum Propagation Delay, to	t_{PLH}	C_L= 50pF	18	24	30	36	ns
		C_L=150pF	21	27	35	42	
	t_{PHL}	C_L=50pF	18	24	30	36	
		C_L=150pF	21	27	35	42	
Maximum Propagation Delay, C to any Q	t_{PLH}	C_L=50pF	21	28	35	42	ns
		C_L=150pF	24	31	40	48	
	t_{PHL}	C_L=50pF	21	28	35	42	
		C_L=150pF	24	31	40	48	
Maximum Propagation Delay, $\overline{PRE}$ to Q	t_{PLH}	C_L=50pF	23	30	38	46	ns
		C_L=150pF	26	33	43	52	
Maximum Propagation Delay, $\overline{CLR}$ to Q	t_{PHL}	C_L=50pF	23	30	38	46	ns
		C_L=150pF	26	33	43	52	
Maximum Output Enable Time, $\overline{OC}$ to any Q	t_{PZH}	R_L=1kΩ, C_L=50pF	18	24	30	36	ns
		R_L=1kΩ, C_L=150pF	21	27	35	42	
	t_{PZL}	R_L=1kΩ, C_L=50pF	18	24	30	36	
		R_L=1kΩ, C_L=150pF	21	27	35	42	
Maximum Output Disable Time, $\overline{OC}$ to any Q	t_{PHZ}	R_L=1kΩ, C_L=50pF	18	24	30	36	ns
	t_{PLZ}		18	24	30	36	
Minimum Pulse Width, C High	t_w		15	20	25	30	ns
Minimum Setup Time, Data after C↓	t_{su}		12	16	20	24	ns
Minimum Hold Time, Data before C↓	t_h		6	8	10	12	ns
Maximum Input Capacitance	C_{IN}		5				pF
Maximum Output Capacitance	C_{OUT}		10				pF
Power Dissipation Capacitance (per stage)	C_{PD}	$\overline{OC}$=V_{CC}	5				pF
		$\overline{OC}$=GND	30				

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

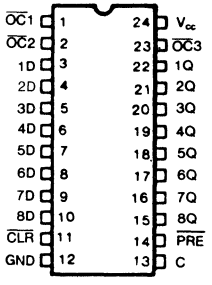
Preliminary Specifications

FEATURE

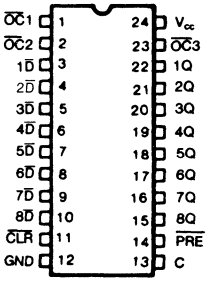
- **3-state buffer-type outputs drive bus-lines directly**
- **Bus-structured pinout**
- **Provides extra bus driving latches necessary for wider address/data paths or buses with parity**
- **Low power consumption characteristic of CMOS devices**
- **3-state outputs with high drive current (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface**
- **Direct interface capability with TTL, NMOS and CMOS devices**
- **Wide operating volage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS : −40°C to +85°C
  KS54HCTLS : −55°C to 125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATIONS

'845



'846



DESCRIPTION

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The '845 has noninverting data(D) inputs. The '846 has inverting D inputs. Since $\overline{CLR}$ and $\overline{PRE}$ are independent of the clock, taking the $\overline{CLR}$ input low will cause the eight Q outputs to go low. Taking the $\overline{PRE}$ input low will cause the eight Q outputs to go high. When both $\overline{PRE}$ and $\overline{CLR}$ are taken low, the outputs will follow the preset condition.

The buffered output control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impendance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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FUNCTION TABLE

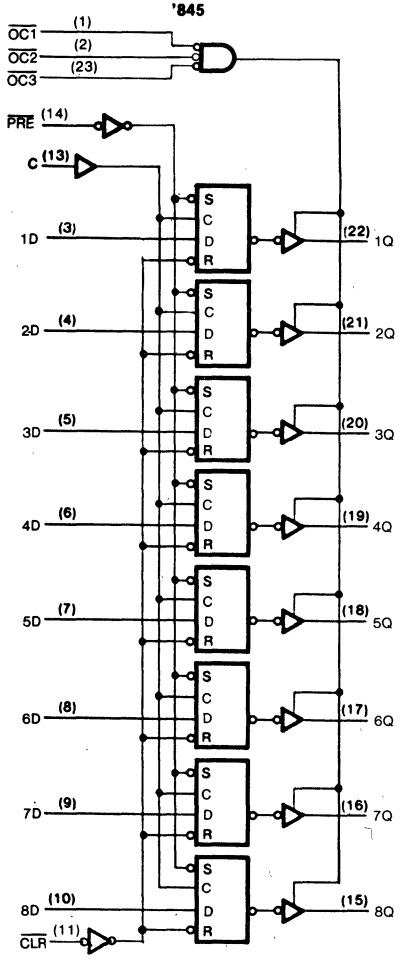
'845

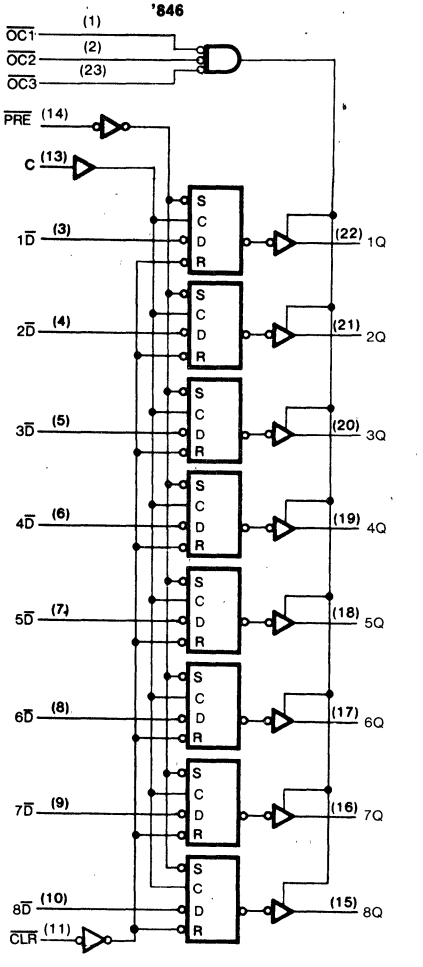
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

'846

INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	$\overline{D}$	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

LOGIC DIAGRAMS





Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCLTS: −40°C to +85°C
KS54HCLTS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS845

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Propagation Delay Clk to Q	t_{PLH}		23	30	38	46	ns
	t_{PHL}		23	30	38	46	
Propagation Delay D to Q	t_{PLH}		18	24	30	36	ns
	t_{PHL}		18	24	30	36	
Propagation Delay $\overline{CLR}$ to Q	t_{PLH}		27	36	45	54	ns
	t_{PHL}		27	36	45	54	
Propagation Delay $\overline{PRE}$ to Q	t_{PLH}		27	36	45	54	ns
	t_{PHL}		27	36	45	54	
Propagation Delay $\overline{OC}$ to Q	t_{PZH}		23	30	38	46	ns
	t_{PZL}		23	30	38	46	
Propagation Delay $\overline{OC}$ to Q	t_{PHZ}		16	21	26	31	ns
	t_{PLZ}		16	21	26	31	
Input Capacitance	C_{IN}		5				pF
Power dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS846

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Propagation Delay Clk to Q	t_{PLH}		25	34	42	65	ns
	t_{PHL}		25	34	42	65	
Propagation Delay $\overline{D}$ to Q	t_{PLH}		20	27	34	40	ns
	t_{PHL}		20	27	34	40	
Propagation Delay $\overline{CLR}$ to Q	t_{PLH}		26	35	44	53	ns
	t_{PHL}		26	35	44	53	
Propagation Delay $\overline{PRE}$ to Q	t_{PLH}		26	35	44	52	ns
	t_{PHL}		26	35	44	52	
Propagation Delay $\overline{OC}$ to Q	t_{PZH}		19	26	32	38	ns
	t_{PZL}		19	26	32	38	
Propagation Delay $\overline{OC}$ to Q	t_{PHZ}		14	19	24	30	ns
	t_{PLZ}		14	19	24	30	
Input Capacitance	C_{IN}		5				pF
Power dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- **Modified input structure allows voltages up to 15V**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High drive current outputs:**
  I_{OL} = 8mA @ V_{OL} = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

The '4049 and '4050 have a modified input protection structure that enable them to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0-15V logic can be converted to 0-5V logic when using a 5V supply. The modified input protection has no diode connected to V_{CC}, thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition the '4049 and '4050 can be used as simple buffers or inverters without level translation.

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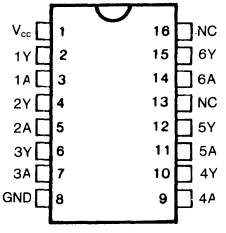
PIN CONFIGURATION

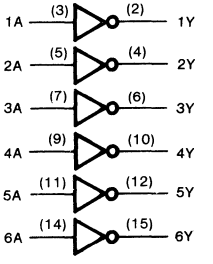


FUNCTION TABLE

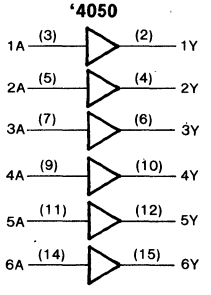
INPUT A	OUTPUT Y	
	'4049	'4050
H	L	H
L	H	L

LOGIC DIAGRAMS

'4049



'4050



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > +15.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND V_{IN}=15V		±0.1	±1.0 ±10.0	±1.0 ±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS4049, HCTLS4050

Characteristic	Symbol	Conditions†	T_a = 25°C V_{CC} = 5.0V		KS74AHCTLS T_a = −40°C to +85°C V_{CC} = 5.0V ± 10%	KS54HCTLS T_a = −55°C to +125°C V_{CC} = 5.0V ± 10%	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay	t_{PLH}	C_L=50pF	13	17	21	26	ns
	t_{PHL}		13	17	21	26	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}	(per gate)					pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

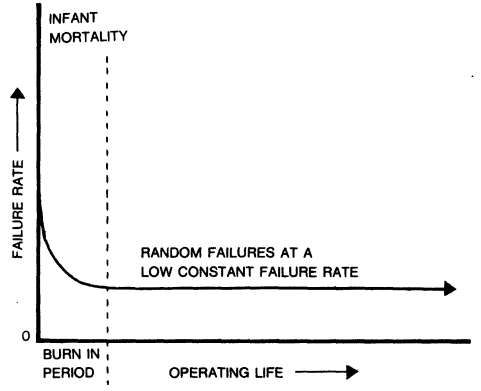
ENHANCEMENT PROGRAMS 6

SAMSUNG's A+ Program

The SST A+ Program has been designed to offer the customer an alternative to standard off-the-shelf plastic encapsulated CMOS circuits. The A+ Program will significantly reduce incoming inspection requirements as well as early device failures (infant mortality). These results are achieved by a tightened AQL inspection plan and a burn-in of each unit for 160 +8, −0 hours at 125°C or equivalent conditions established from a time/temperature regression curve.

The AQL Plan. Acceptable Quality Levels (AQL) are a measure of the quality of outgoing CMOS circuits. These levels are established by the manufacturer to show the process percent defective being produced and to ensure that the customer is receiving material that meets his requirements. The SST A+ Program has tightened these AQL levels to a point at which incoming inspection by the customer is no longer a necessity. A+ product quality is monitored significantly more closely than standard product; those lots which fail the AQL level are 100% reworked before resubmission to the AQL gate.

The Reliability Plan. Reliability is the statistical probability that a product will give satisfactory performance for a specified period of time when used under specified conditions. A typical rate curve is shown below:



Reliability theory assumes that devices fail according to the above curve. When a group of devices is manufactured a small portion of the units will be inherently weaker than the average. These weak units will *probably* fail during the first few hours of operation—hence the term "infant mortality." If the units are burned-in however, thereby allowing the weak units to fail, there is a much lower probability that those finally put into system use will fail.

The SST A+ Flow. In order to achieve an extremely high quality unit and reduce infant mortality failures the following flow has been established:

Process Flow

	DESCRIPTION
	WAFER FABRICATION CMOS PROCESS CV PLOTS OXIDE AND NITRIDE THICKNESS MEASUREMENTS OPTICAL INSPECTIONS SEM ANALYSIS
	ENCAPSULATION NITTO HC10 TYPE 2 EPOXY MOLDING COMPOUND ULTRA PURE FOR CMOS APPLICATIONS
	POST MOLD BAKE 6 HOURS AT 175 DEG. C. CURES PLASTIC STRESSES ALL WIRE BONDS AND DIE
	O/S FUNCTIONAL ELECTRICAL 100% TESTING OPENS/SHORTS AND INTERMITTENTS REMOVE
	HIGH TEMPERATURE BURN-IN 160 HOURS AT 125 DEG. C. OR EQUIVALENT CONDITIONS ESTABLISHED FROM A TIME/ TEMPERATURE REGRESSION CURVE. 0.96 eV
	FULL FUNCTIONAL AND PARAMETRIC ELECTRICAL TESTING 100% ELECTRICAL TESTING AC, DC 88 DEG, C.
	THERMAL SHOCK MONITOR −65 DEG. C. TO + 125 DEG. C. LIQUID TO LIQUID 5 CYCLES- SAMPLES SELECTED AT RANDOM
	TIGHT AQL SAMPLING PLAN ELECTRICAL−0.05% AQL AT 88 DEG. C. MECHANICAL−0.01% AQL CRITICAL & MAJOR
	SHIP UNITS

NOTES

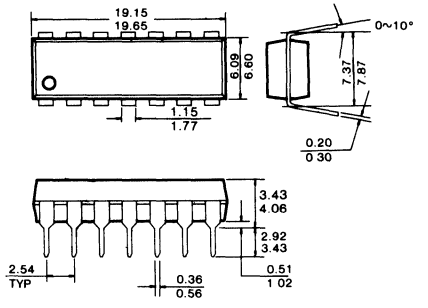
PACKAGE DIMENSIONS & ORDERING INFORMATION

7

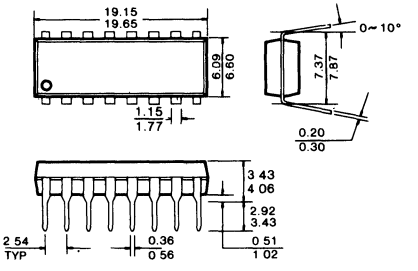
PACKAGE DIMENSIONS

1. PLASTIC PACKAGES

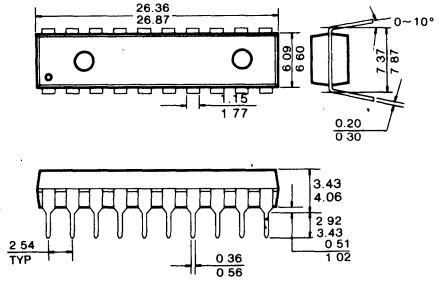
14-Pin Plastic DIP Units: mm



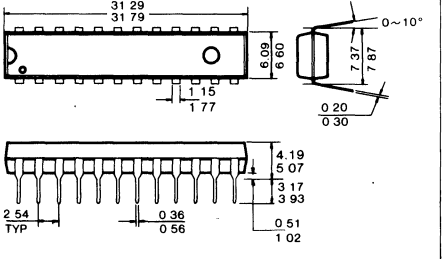
16-Pin Plastic DIP Units: mm



20-Pin Plastic DIP Units: mm



24-Pin Plastic DIP Units: mm



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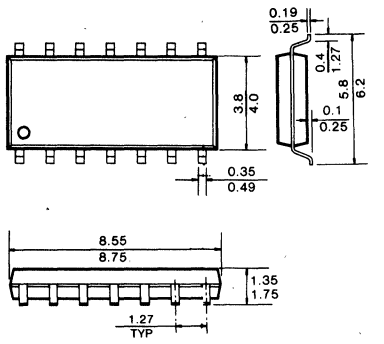
PACKAGE DIMENSIONS

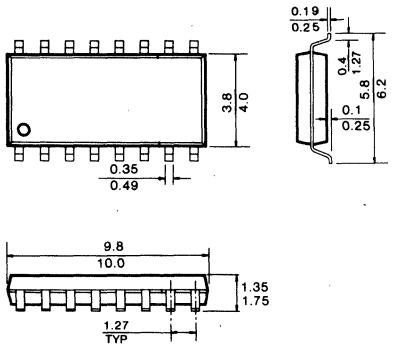
14-Pin SOP

Unit: mm



16-Pin SOP

Unit: mm



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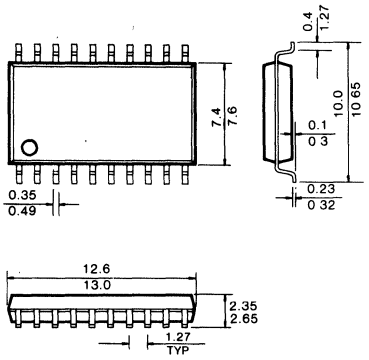
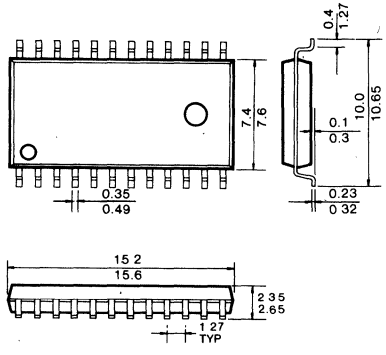
Unit: mm



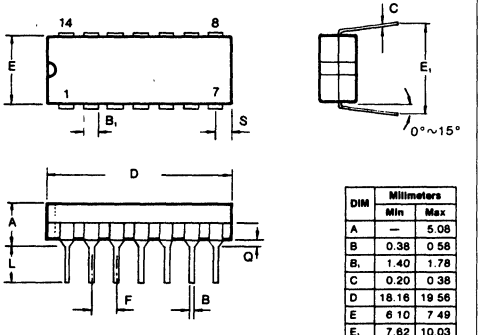
24-Pin SOP

Unit: mm



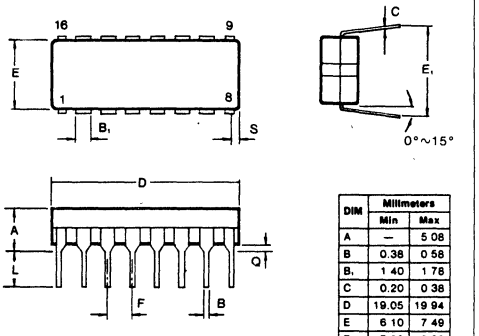
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



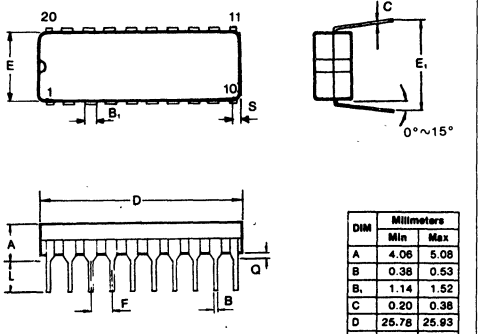
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0 58
B1	1.40	1.78
C	0.20	0 38
D	18.16	19 56
E	6 10	7 49
E1	7.62	10.03
F	2 54	
L	3.18	4.19
Q	0.51	1.02
S	1 91	2 29

16-Pin Ceramic DIP Units: mm



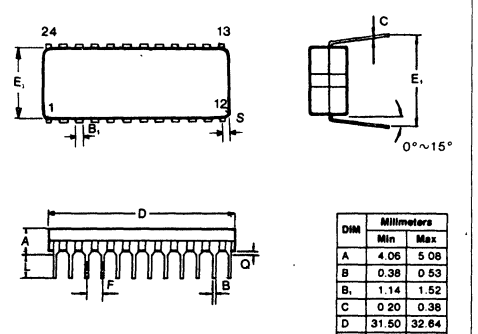
DIM	Millimeters	
	Min	Max
A	—	5 08
B	0.38	0 58
B1	1 40	1 78
C	0.20	0 38
D	19.05	19 94
E	6 10	7 49
E1	7 62	10 03
F	2 54	
L	3 18	4 19
Q	0.51	1 02
S	0 51	1 14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6 60
E1	7.77	7.98
F	2.54	
L	3.73	4 01
Q	0.38	0.89
S	0.51	1 14

24-Pin Ceramic DIP Units: mm

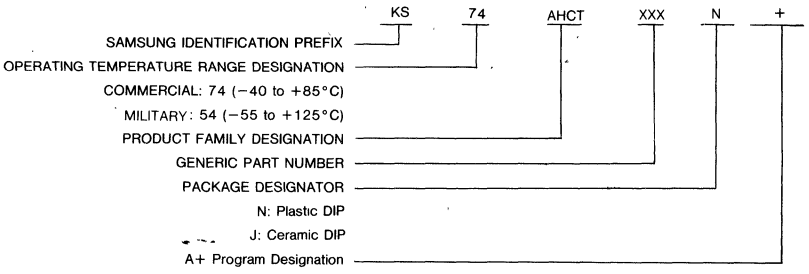


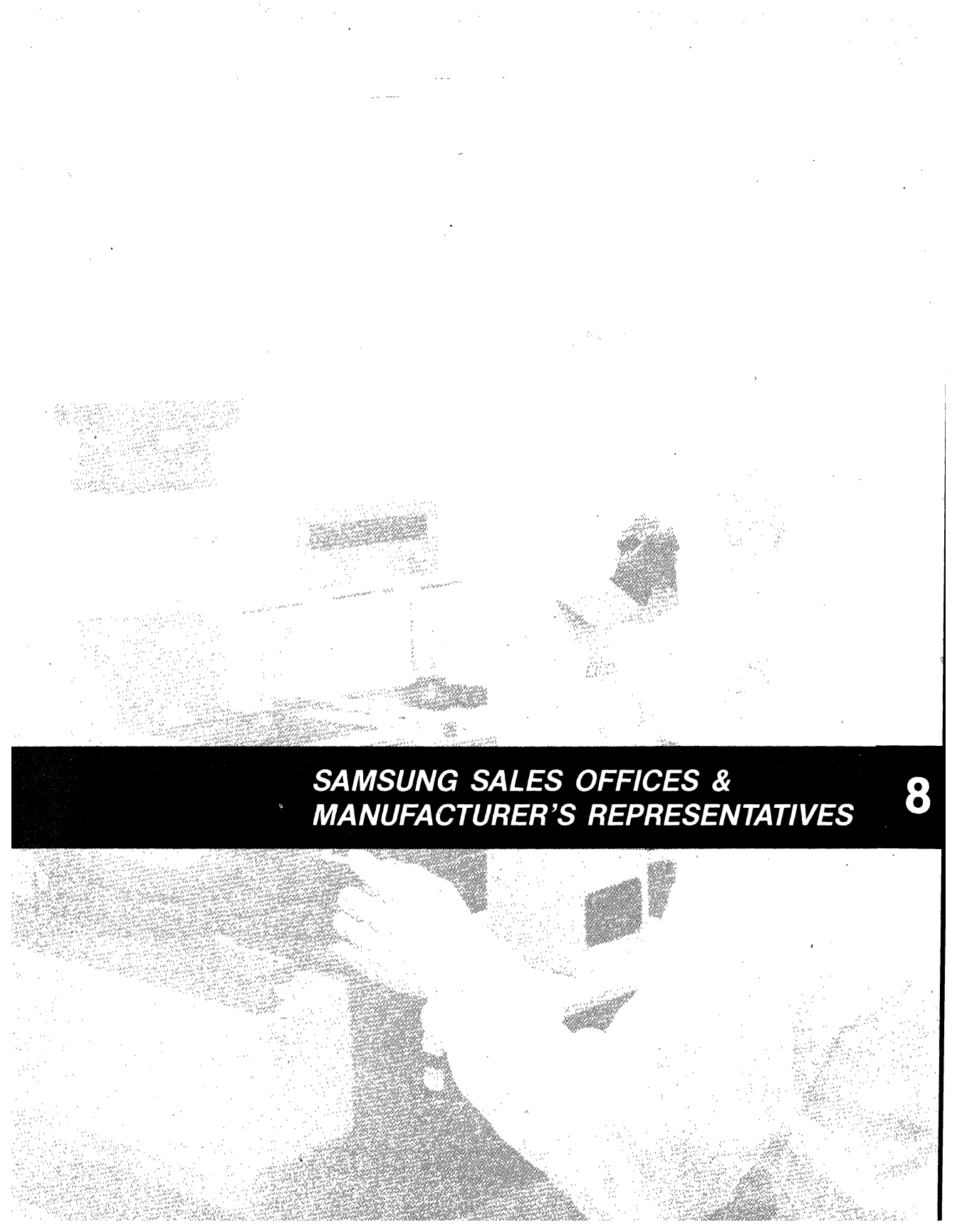
DIM	Millimeters	
	Min	Max
A	4.06	5 08
B	0.38	0 53
B1	1.14	1.52
C	0 20	0.38
D	31.50	32.64
E	7.24	7.75
E1	7 77	7.98
F	2 54	
L	3 73	4 01
Q	0 508	1 778
S	1.85	1 93

7

ORDERING INFORMATION

The ensure prompt and accurate processing of your order, please use the product code system as described in the following example.





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