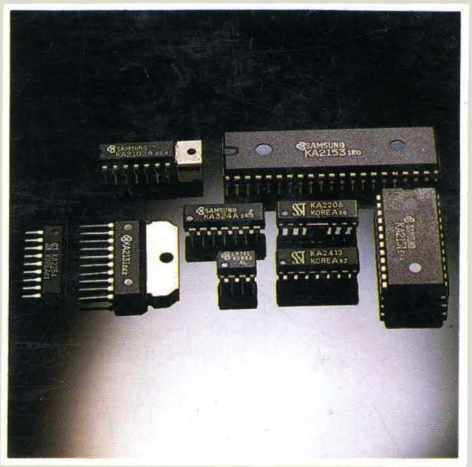
SAMSUNG

Linear IC Data Book



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SAMSUNG Linear IC Data Book 1986

III

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LINEAR IC DATA BOOK

AUDIO ICs
VIDEO ICs
TELEPHONE ICs
VOLTAGE REGULATOR
OPERATIONAL AMPLIFIER
COMPARATOR
TIMER
MISCELLANEOUS ICs

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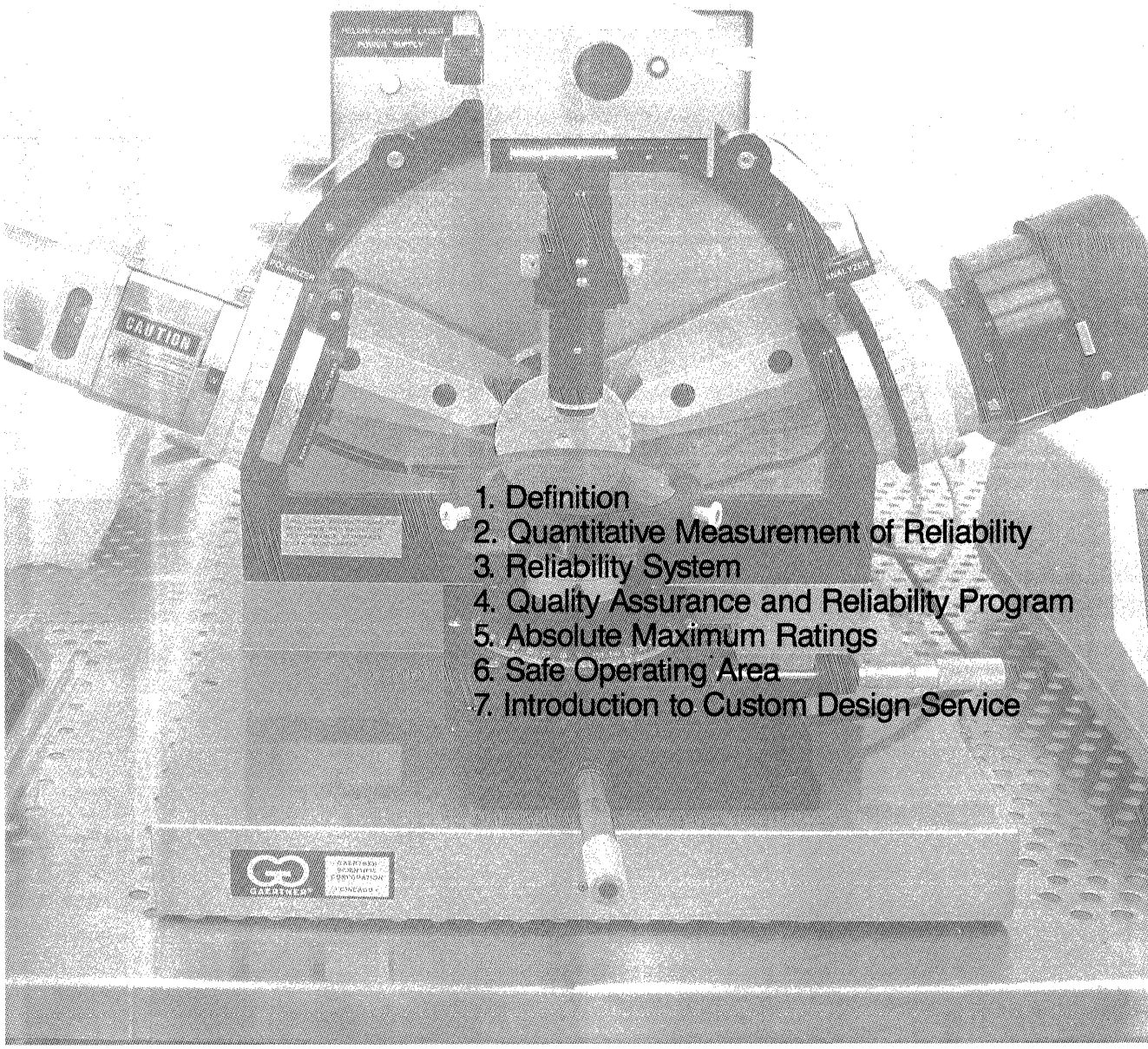
I. GENERAL INFORMATION



1. Definition
2. Quantitative Measurement of Reliability
3. Reliability System
4. Quality Assurance and Reliability Program
5. Absolute Maximum Ratings
6. Safe Operating Area
7. Introduction to Custom Design Service

1. DEFINITION

The definition of reliability assumes that the basic design of the device is adequate to provide the electrical performance required and to withstand the electrical, mechanical and thermal stresses it will encounter in the application for the intended life of the equipment. The reliability is also used to show the probability that a device will operate within specified limits for a given time period and set of operating conditions.

Reliability, in general, explained with "Mortality curve (or Bathtub curve)" This curve indicates three different failure periods: Early failure period, Inherent failure period, and Wear out failure period.

Consider a population of components from which a very large sample is taken and placed in operation at time T=0. The population will initially show a high failure rate and decrease rather rapidly. This period is called the "Early failure period. The early failure can be eliminate by proper design, control of fabrication process and assembly process, or deliberate bum-in before shipment to customers.

At inherent failure period, the failure rate stabilizes at an approximately constant (general electronic component). But failure rate of semiconductor devices such as transistors, unlike general electronic components, decreases gradually with time (see inherent failure period).

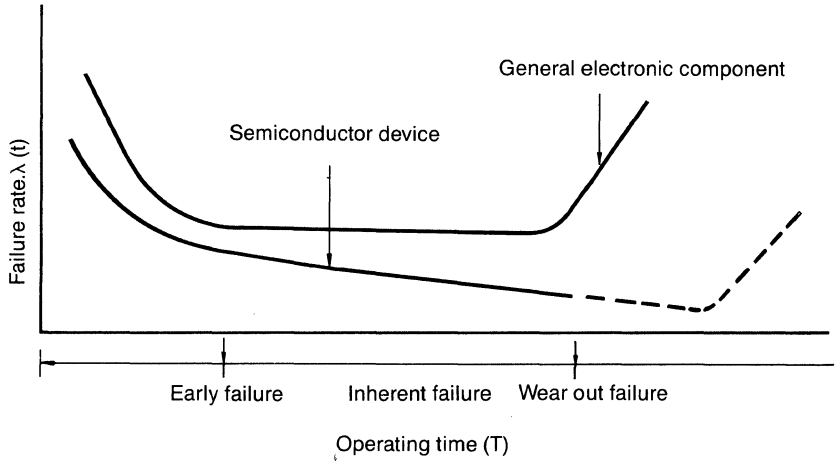


Fig 1. Mortality curve; Failure rate versus operating time.

2. QUANTITATIVE MEASUREMENT OF RELIABILITY

As previously defined, reliability is the probability that a device will operate within specified limits for a given time period and set of operating conditions. To express the reliability of semiconductor devices quantitatively, failure rate (λ) and mean time between failure are used conventionally.

A failure rate, λ, is the probability of failure per unit of time for the components still loperating, usually given in percent per 1000 operating hours (%/1000 hours) or quantity failure per hours.

$$\lambda = \frac{\text{number of failures}}{\text{total accumulated operation hours}} = \frac{r(t)}{N.t}$$

N: Quantity used or tested
t: Operating hours
r(t): Quantity failed after hours

Since cumulative failure rate of semiconductor device is small, FIT (10^{-9} failed/hour) is used reliability system.

3. RELIABILITY SYSTEM

From the stage of development to after sales service, assurance system is outlined in fig. 2, 3 by considering preproduction. The qualification test for the new product, significance test for the engineering change, in process quality control, batch acceptance test, periodical reliability test and customer service are performed under a consolidate system.

3.1 Quality assurance during development

Through the design review, qualification of material and piece parts, evaluation test for the trial product and preproduction, the new products are qualified as shown below.

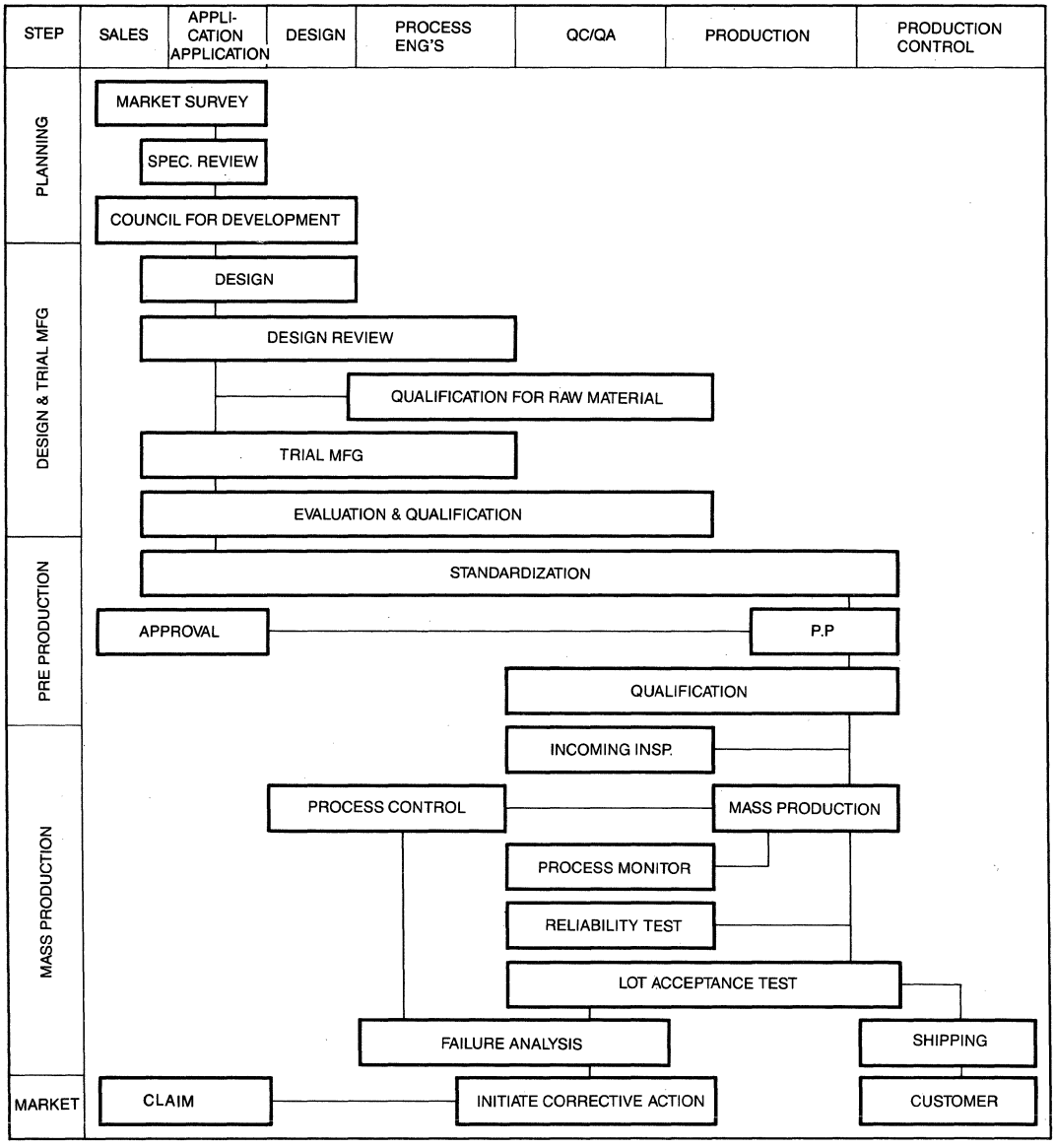


Fig 2.

3.2 Quality assurance during manufacturing

To maintain high quality and reliability aimed at design, the inprocess quality control, PRT (process reliability test) for lot acceptance and periodical DRT (device reliability test) are performed as follow.

MIL STD Method 750B, MIL STD 202E and MIL STD 883 are referenced for these test.

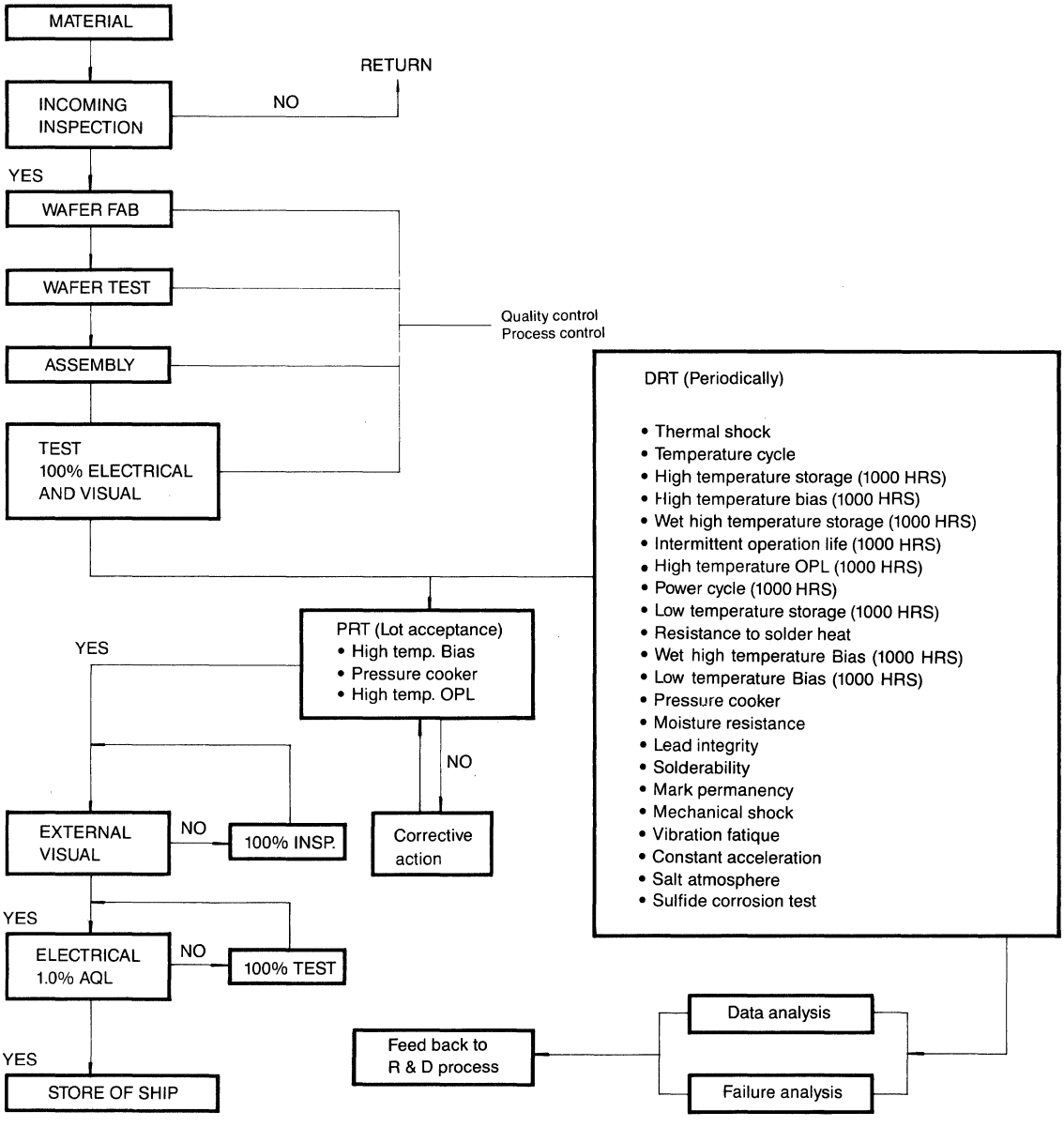


Fig 3. Quality assurance system during manufacturing.

4. QUALITY ASSURANCE AND RELIABILITY PROGRAM

4.1 Purpose

This program is applied for qualification approval test (for new products and process evaluation products), quality conformance test (for mass products) and sampling method.

4.2 Reliability test plan

1) Reliability test plan is shown at table 1.
2) For technical research project, these test items will be combined and modified.

4.3 Reliability test schedules

The procedure of reliability test will be performed separately as follows.

4.3.1 Quality approval test.
4.3.2 Quality conformance test.
4.3.3 Quality conformance test consists of process reliability test (PRT), device reliability test (DRT) and products test (out going test).

4.4 Selection of samples

4.4.1 Quality approval test
1) Sampling plan is listed at table 1 for each product type. (Discrete, LIC, Digital IC).
2) These plans are from MIL-STD-19500E.
3) After sampling, reliability test will be performed with table 1 and it is considered for test prupose, device characteristics.
4) The samples that are rejected in initial test will be excluded in reliability test.

4.4.2 Quality conformance test
1) Sampling plan is listed at table 1 for each product type.
2) These plans are from MIL-STD-19500E.
3) After sampling, reliability test will be performed with table 1 for each product type and it is considered for the test purpose, device characteristics.
4) The samples that are rejected in intial test will be exculed in reliability test.

4.5 Reliability test time

4.5.1 Test frequency is performed at every lot, 6 month and 1 year as listed at following table 1.
4.5.2 Process reliability test (PRT) is normally performed at every lots. It is discontinuously performed at 2 run, (or 3 run, 5 run), if it is continueously accepted for 5 lots.
4.5.3 It is normal to performa quality approval test & device reliability test during 1000 HRS, and to perform process reliability test during 48HRS. Upper test frequency and time can be modified for especial test purpose by QA manager.

4.6 Reliability test method

Reliability test and test method is performed with reliability and individual spec of SST.
In case there is different condition between general reliability test spec and individual spec, individual spec will be applied firstly.

4.7 Acceptance criteria

4.7.1 Acceptance criteria is listed in individual spec of each device.
4.7.2 Failure criteria is shown in following contents about TR, L-IC, digital IC.

4.8 Lot disposition

4.8.1 Lot that is rejected for qualification approval test must not be gone out.
4.8.2 When lot is rejected in process reliability test, it should be issued "lot rejection notice" based on specification. We feed back abnomal point to process departments. Therefore, this problem shall be solved.

4.9 Quality approval & conformance test program for finished goods

TEST PERIOD: A — EVERY LOT
B — 3 MONTHS
C — 6 MONTHS
D — 1 YEAR

NO	GROUP 0	PERIOD
1	VISUAL INSPECTION	A
2	ELECTRICAL TEST	A
3	DIMENSION (MAJOR)	A
4	DIMENSION (ALL)	D
5	PACKING INSPECTION	A

NO	GROUP 1	PERIOD
6	OPERATING LIFE TEST	C
7	INTERMITTENT OPL	C
8	POWER CYCLE	C

NO	GROUP 2	PERIOD
9	HIGH TEMP OPL	A
10	HIGH TEMP REV. BIAS	A
11	LOW TEMP STORAGE	C
12	HIGH TEMP STORAGE	C

NO	GROUP 3	PERIOD
13	PRESSURE COOKER	A
14	THERMAL SHOCK	C
15	TEMP CYCLE	C
16	SOLDER HEATRESIST	C

NO	GROUP 5	PERIOD
21	LEAD INTEGRITY	D
22	SOLDERABILITY	C
23	MARK PERMANENCY	C
24	MECHANICAL SHOCK	C
25	VIBRATION FATIQUE	C
26	CONSTANT ACCELERATION	C
27	SALT ATMOSPHERE	B

TABLE 1.

NO	GROUP 4	PERIOD
17	WET HIGH TEMP STORAGE	C
18	WET HIGH TEMP OPL	C
19	WET HIGH TEMP INTEMITTENT OPL	C
20	MOISTURE RESISTANCE SULFIDE CORROSION TEST	C

NO	GROUP 6	PERIOD
28	SET AGING TEST	C
29	ESD	C
30	SULFIDE CORROSION TEST	C

4-10. Quality approval & conformance test for discrete

4.10.1 Test condition and acceptance

No.	Test Item	Test Condition	Corrective Test Method	Quality Approval			Quality Conformance			Note
				Sample Size	LTPD	Acceptance NBR	Sample Size	LTPD	Acceptance NBR	
1	Visual Inspection Critical Major Minor	Outgoing Visual Spec		 231 231 231	 1.0 1.5 2.0	 0 1 2	 231 231 231	 1.0 1.5 2.0	 0 1 2	
2	Electrical Test (DC/AC) Critical Major Minor	Outgoing Test Spec		 231 231 231	 1.0 1.5 2.0	 0 1 2	 231 231 231	 1.0 1.5 2.0	 0 1 2	
3	Dimension (Major)	VIS/MECH Criteria		15	15	0	15	15	0	
4	Dimension (All)	VIS/MECH Criteria		15	15	0	15	15	0	
5	Packing Inspection	Outgoing Packing Criteria		Each Lot			Each Lot			
6	Operating Life Test	T_a=25°C P_C=P_C (max) 1000 HRS		22	10	0	22	10	0	
7	Intermittent OPL for S/S Devices	T_a=25°C P_C=P_C (max) 2 min/2 min on/off 1000 HRS		22	10	0	22	10	0	
8	Power Cycle for Power Devices	T_a=25°C ΔT_j=100°C 45 Sec 90 Sec on/off 1000 HRS		22	10	0	22	10	0	
10	High Temperature Reverse Bias	T_a=T_j (max) V_{CB}=BV_{CBO}×0.8 1000 HRS		22	10	0	22	10	0	48 HR for process reliability test
11	Low Temperature Storage	T_a=−55°C 1000 HRS		22	10	0	22	10	0	
12	High Temperature Storage	T_a=T_j (max) 1000 HRS		22	10	0	22	10	0	
13	Pressure Cooker Test	T_a=121°C±2°C RH=100%, 15PSIG 168 HRS		22	10	0	22	10	0	48 HR for process reliability test
14	Liquid Thermal Shock Test	−55°C⇄125°C 5 min, <10 Sec, 5 min 100 Cycles	MIL-STD-750 1056	22	10	0	22	10	0	
15	Temperature Cycle	−65°C⇄25°C⇄150°C 10 min, 5 min, 10 min 100 Cycles	MIL-STD-202 107 MIL-STD-750 1051	22	10	0	22	10	0	

4.10.1 Test condition and acceptance (continued)

No.	Test Item	Test Condition	Corrective Test Method	Quality Approval			Quality Conformance			Note
				Sample Size	LTPD	Acceptance NBR	Sample Size	LTPD	Acceptance NBR	
16	Solder Heat Resist	T_a=260°C±5°C Time=10±1 Sec Once Without Flux	MIL-STD-202 210A, B MIL-STD-750 2031	22	10	0	22	10	0	
17	Wet High Temperature Storage	T_a=85°C, RH=85% 1000 HRS	MIL-STD-202 103	22	10	0	22	10	0	
18	Wet High Temperature Reverse Bias Test	T_a=85°C, RH=85% V_{CB}=BV_{CBO} X 0.8 1000 HRS		22	10	0	22	10	0	
21	Terminal Strength (Lead Fatique)	W=227g, 90 3 Times	MIL-STD-202, 211 MIL-STD-750 2036	22	10	0	22	10	0	
22	Solderability	Tsol = 230°C, 5 Sec Once with Flux	MIL-STD-202, 208 MIL-STD-750, 2026	22	10	0	22	10	0	
23	Marking Permanency	Rub Marking with Ten Shrokes of a Cotton Cloth Damped with Solvents		22	10	0	22	10	0	
24	Mechanical Shock	1500G, 0.5mS 3 Times, Each Direction of X, Y and Z Axis	MIL-STD-202, 213 MIL-STD-750, 2016	22	10	0	22	10	0	
25	Vibration (Variable Frequency)	100 ~ 2000 ~ 100Hz 20G 4 min, 4 Times, Each Direciton of X, Y and Z Axis	MIL-STD-750 2031	22	10	0	22	10	0	
26	Constant Acceleration	20000G X, Y, Z Axis 1 min for each Axis	MIL-STD-202 750	22	10	0	22	10	0	
27	Salt Atmosphere	T_a=35°C 25HRS	MIL-STD-202 101 MIL-STD-750 1042	22	10	0	22	10	0	
28	Set Aging			22	10	0	22	10	0	
29	Electro Static Discharge	R=150K C=200pF	DOD-HDBK-263 MIL-STD-883-3015	22	10	0	22	10	0	
30	Sulfide Corrosion Test	T_a=25±2°C Humidity=75% R/H SO2: 10±2 PPM Velocity: 0.006 ~ 0.007m/s	DIN 40046	22	10	0	22	10	0	

4.10.2 Failure criteria

Parameter	Symbol	Life End Limit		Unit	Remark
		Min	Max		
Collector Cut-off Current	I_{CBO}	—	USLX2	μA	Surface Instability
Emitter Cut-off Current	I_{CEO}	—	USLX2	μA	Surface Instability
DC Current Gain	h_{FE}	LSLX0.8	USLX1.2	—	Surface Instability
h_{FE} Variation Ratio	Δh_{FE}	−20	+20	%	±50% for Darington
Collector-Emitter Saturation Saturation Voltage	V_{CE} (sat)	—	USLX1.2	mV	Half Open, Resistance Increase Surface Instability
Base-Emitter Saturation Voltage	V_{BE} (sat)	—	USLX1.2	mV	Half Open, Resistance Increase Surface Instability
Thermal Resistance	ΔV_{BE}	—	USLX1.2	V	θ_{jc} Instability ASO Instability
Noise	N_V, N_F	—	USLX1.5	mV	Crystal Defect Surface Instability

Note 1) USL: Upper Specification Limit
2) LSL: Lower Specification Limit
3) Δh_{FE} = Initial Value/After Test Value

4-11. Quality approval & conformance test for linear IC

4.11.1 Test condition and acceptance

No.	Test Item	Test Condition	Corrective Test Method	Quality Approval			Quality Conformance			Note
				Sample Size	LTPD	Acceptance NBR	Sample Size	LTPD	Acceptance NBR	
1	Visual Inspection Critical Major Minor	Outgoing Visual Spec		 231 231 231	 1.0 1.5 2.0	 0 1 2	 231 231 231	 1.0 1.5 2.0	 0 1 2	
2	Electrical Test Critical Major Minor	Outgoing Test Spec		 231 231 231	 1.0 1.5 2.0	 0 1 2	 231 231 231	 1.0 1.5 2.0	 0 1 2	
3	Dimension (Major)	VIS/MECH Criterial		15	15	0	15	15	0	
4	Dimension (All)	VIS/MECH Criterial		15	15	0	15	15	0	
5	Packing Inspection	Outgoing Packing Criteria		Each Lot			Each Lot			
6	Operating Life Test	T_a=25°C V_{CC}=V_{CC} (max) 1000 HRS		22	10	0	22	10	0	
7	Intermittent OPL	T_a=25°C V_{CC}=V_{CC} (max) 2 min/2 min on/off		22	10	0	22	10	0	
9	High Temperature Operation Life Test	T_a=T_j (max) V_{CC}=V_{CC} (max) 1000 HRS	MIL-STD-883, 1005	22	10	0	22	10	0	48 HR for process reliability test
11	Low Temperature Storage	T_a=−55°C 1000 HRS		22	10	0	22	10	0	
12	High Temperature Storage	T_a=125°C 1000 HRS		22	10	0	22	10	0	
13	Pressure Cooker Test	T_a=121°C±2°C RH=100% 15PSIG 168 HRS		22	10	0	22	10	0	48 HR for process reliability test
14	Liquid Thermal Shock	−55°C⇄125°C 5 min, <10 Sec, 5 min 100 Cycles	MIL-STD-883 1056	22	10	0	22	10	0	
15	Temperature Cycle	−65°C⇄25°C⇄150°C 10 min, 5 min, 10 min 100 Cycles		22	10	0	22	10	0	
16	Solder Heat Resist	260°C±5°C 10±1 Sec Once without Flux		22	10	0	22	10	0	

4.11.1 Test condition and acceptance (continued)

No.	Test Item	Test Condition	Corrective Test Method	Quality Approval			Quality Conformance			Note
				Sample Size	LTPD	Acceptance NBR	Sample Size	LTPD	Acceptance NBR	
17	Wet High Temperature Storage	T_a=85°C, RH=85% 1000 HRS		22	10	0	22	10	0	
18	Wet High Temperature OPL	T_a=85°C, RH=85% V_{CC}=V_{CC} (Typ) 1000 HRS		22	10	0	22	10	0	
19	Moisture Resistance	90~98%/65°C 3 HRS 80~98%/25°C 3 HRS 90~98%/65°C 3 HRS	MIL-STD-883 1004	22	10	0	22	10	0	
21	Lead Integrity	1) Wire Lead 0.229±0.0144 kg for Three 90±5° Arcs on each Leads Bending Cycle: 2~5 Sec 2) Dial-in-lines	MIL-STD-883 2004	22	10	0	22	10	0	
22	Solderability	260°C ± 10°C Preconditioning 1 HRS.	MIL-STD-883 2003	22	10	0	22	10	0	
23	Marking Permanency	Rub Marking with Ten Stokes of a Cotton Cloth Damped with Solvents		22	10	0	22	10	0	
24	Mechanical Shock	Pulse Duration: 0.1~1m Sec Shock Pulse: 0.5~3KG	MIL-STD-883 2002	22	10	0	22	10	0	
25	Vibration Fatique	100~200~600Hz 20G, 4 min, 4 times X, Y, Z Axis	MIL-STD-883 3007A	22	10	0	22	10	0	
26	Constant Acceleration	20000G X, Y, Z Axis 1 min for each Axis	MIL-STD-883	22	10	0	22	10	0	
27	Salt Atmosphere	Nacl T_a=35°C, 24 HRS	MIL-STD-883 1009A	22	10	0	22	10	0	
28	Set Aging	—	—	22	10	0	22	10	0	
29	ESD	C=200pF R=1.5K	DOD-HBDK-263 MIL-STD-883	22	10	0	22	10	0	
30	Sulfide Corrosion Test	T_a=25±2°C Humidity: 75% R/H SO2: 10±2ppm Velocity: 0.006~0.007m/s	DIN 400 46	22	10	0	22	10	0	

4.11.2 Failure Criteria

Parameter	Symbol	Life End Limit		Unit	Remark
		Min	Max		
Output Drive Current (P-CH)					
1. Reference Voltage	V_{REF}	LSLX0.9	USLX1.1	V	
2. Quiescent Current Drain	I_D	LSLX0.8	USLX1.2	I	
	D_{VO}	LSLX0.8	LSLX1.2	V	
3. Load Regulation					
Operational Amplifier					
1. Input Offset Voltage	V	—	USLX1.2	V	
2. Voltage Gain (Closed Loop)	G_V	LSLX0.8	USLX1.2	G_V	
Audio Amplifier					
1. Quiescent Output VTG	V_O	LSLX0.9	USLX1.1	V	
2. Output Power (D=10%)	P_O	LSLX0.9	—	W	
3. Input Resistance Drain	Ri	LSLX0.8	—	R	
4. Quiescent Current Drain	I_D	—	USLX1.25 +100% Initial Value	I	
Distortion			USLX1.5	%	
Input Limiting VTG			USLX3	dBμ, mV	
Input Offset Current			USLX1.5	A	
Input Current			USLX1.3	A	
Input Bias Current			USLX1.3	I	
Maximum Output			USLX0.9	V	
Voltage Level		LSLX1.1			
Same Level Input Voltage Range		LSLX0.9	—	V	
Open/Short					
Gross/Fine Leak Visual Color Disterhance Marking Disterhance Soldering	Individual Spec				

Note: LSL: Lower Specification Limit
USL: Upper Specification Limit

4-12. Quality approval & conformance test for digital IC

4.12.1 Test condition and acceptance

No.	Test Item	Test Condition	Corrective Test Method	Quality Approval			Quality Conformance			Note
				Sample Size	LTPD	Acceptance NBR	Sample Size	LTPD	Acceptance NBR	
1	Visual Inspection Critical Major Minor	Outgoing Visual Spec		 231 231 231	 1.0 1.5 2.0	 0 1 2	 231 231 231	 1.0 1.5 2.0	 0 1 2	
2	Electrical Test Critical Major Minor	Outgoing Test Spec		 231 231 231	 1.0 1.5 2.0	 0 1 2	 231 231 231	 1.0 1.5 2.0	 0 1 2	
3	Dimension (Major)	VIS/MECH Criteria		15	15	0	15	15	15	
4	Dimension (All)	VIS/MECH Criteria		15	15	15	15	15	15	
5	Packing Inspection	Outgoing Packing Criteria		Each Lot			Each Lot			
6	Operating Life Test	T_a=25°C V_{CC}=V_{CC} (max) 1000 HRS	MIL-STD-883 1005	32	7	0	32	7	0	
9	High Temperature OPL	T_a=125°C Dynamic V_{CC}=V_{CC} (max) 1000 HRS	MIL-STD-883 1005	32	7	0	22	7	0	48 HRS for process reliability test
11	Low Temperature Storage	T_a=−55°C 1000 HRS		32	7	0	32	7	0	
12	High Temperature Storage	T_a=125°C 1000 HRS		22	10	0	22	10	0	
13	Pressure Cooker Test	T_a=121°C±2°C RH=100% 15 PSIG 168 HRS		22	10	0	22	10	0	48 HRS for process reliability test
14	Liquid Thermal Shock Test	−55°C⇄125°C 5 min, <10 Sec, 5 min 100 Cycles	MIL-STD-883 1011	22	10	0	22	10	0	
15	Temperature Cycle	−65°C⇄25°C⇄150°C 10 min, 5 min, 10 min 100 Cycles	MIL-STD-883 1010	22	10	0	22	10	0	
16	Solder Heat Resist	260°C±5°C 10±1 Sec Once without Flux		22	10	0	22	10	0	
17	Wet High Temp. Storage	T_a=85°C, RH=85% 1000 HRS		32	7	0	32	7	0	

4.12.1 Test condition and acceptance (continued)

No.	Test Item	Test Condition	Corrective Test Method	Quality Approval			Quality Conformance			Note
				Sample Size	LTPD	Acceptance NBR	Sample Size	LTPD	Acceptance NBR	
18	Wet High Temperature OPL	T_a=85°C, RH=85% V_{CC}=V_{CC} (TYP) 1000 HRS		32	7	0	32	7	0	
19	Moisture Resistance	90~98%/65°C 3 HRS 80~98%/25°C 8 HRS 90~98%/65°C 3 HRS	MIL-STD-883 1004	32	7	0	32	7	0	
21	Lead Integrity	1) Wire Lead 0.229±0.0144 kg for Three 90±5° Arcs on each Leads Bending Cycle: 2~5 Sec 2) Dial-in-lines	MIL-STD-883 2004	32	7	0	32	7	0	
22	Solderability	260°C ± 10°C Preconditioning 1 HRS.	MIL-STD-883 2003	22	10	0	22	10	0	
23	Marking Permanancy	Rub Marking with Ten Stokes of a Cotton Cloth Damped with Solvents		22	10	0	22	10	0	
24	Mechanical Shock	Pulse Duration: 0.1~1m Sec Shock Pulse: 0.5~3kg	MIL-STD-883 2002	32	7	0	32	7	0	
25	Vibration Fatique	20G-3 Axis Orientations f=20 to 2000 CPS for 4 Minute Cycle	MIL-STD-883 3007A	32	7	0	32	7	0	
26	Constant Acceleration	20000G X, Y, Z Axis 1 min for each Axis	MIL-STD-883 2001	32	7	0	32	7	0	
27	Salt Atmosphere	Nacl T_a=35°C, 24 HRS	MIL-STD-883 1009A	32	7	0	32	7	0	
28	Set Aging	—	—	32	7	0	32	7	0	
29	ESD	C=200pF R=1.5K	MIL-STD-883 3015 DOD-HDBK-263	32	7	0	32	7	0	
30	Sulfide Corrosion Test	T_a=25±2°C Humidity: 75% R/H SO_2: 10±2ppm Velocity: 0.006~0.007m/s	DIN 40046	32	7	0	32	7	0	

4.12.2 Failure Criteria

Parameter	Symbol	Life End Limit		Unit	Remark
		Min	Max		
Output Drive Current (P-CH)	I_{DP}	LSLX0.9	USLX1.1	A	
Output Drive Current (N-CH)	I_{DN}	LSLX0.9	USLX1.1	A	
Output High Voltage	V_{OH}	LSLX0.9	—		
Output Low Voltage	V_{OL}	—	USLX1.1	V	
Input Current	I_{IN}	—	USLX2.0	V	
Quiescent Current	I_L	—	USLX2.0	A	
Voltage Mrgin		0.05XUSL	0.95XUSL	A	
		+0.95XLSL	+0.05XLSL	V	
AC Characteristic Open/Short		LSLX0.9	USLX1.1	Sec	
Gross/Time Leak Visual Color Disterbance Soldering Marking Disterbance	Individual Spec				

Note: LSL: Lower Specification Limit
USL: Upper Specification Limit

5. ABSOLUTE MAXIMUM RATINGS

The electrical performance of a semiconductor device is usually expressed in terms of its characteristics and maximum ratings.

Maximum ratings give the values which cannot be exceeded without risk of damage to the device. Change in supply voltage and in the tolerances of other components in their circuit must also be taken into consideration. No single maximum rating should ever be exceeded, even when the device is operated well within the other maximum ratings. The inclusion of the word "admissible" in a title means that the associated curve defines the maximum ratings.

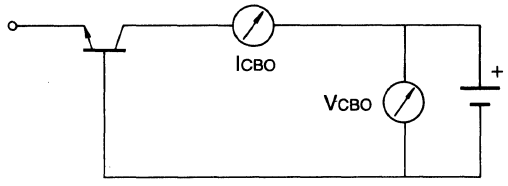
5.1 Voltage ratings

1) Diodes

- Peak reverse voltage (V_{RM})
  The peak value of the reverse voltage that may be applied. It is limited by the electron avalanche breakdown voltage.
- DC reverse voltage (V_R)
  The reverse voltage that may be applied continuously. Usually the reverse leakage current is specified as this voltage.

2) Transistors

- Collector-base voltage (V_{CBO})



The reverse voltage which may be applied vefore breakdown between collector and base, when the emitter is open circuited. This breakdown voltage is a characteristic of the transistor alone. Breakdown may be occur because of avalanche multiplication of the current (I_{CO}) that crosses the collector junction. As are sult of this multiplication. The current becomes $M \times I_{CC}$. in which Mis the factor by which the original current I_{CO} is multiplied by the avalanche effect.

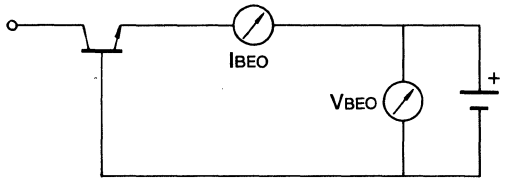
The avalanche multiplication factor depends on the voltage V_{CB} between collector and base. It is given by the following

$$M = \frac{1}{1 - (V_{CB}/B\ V_{CBO})^n}$$

V_{CB}: Voltage applied to the collector and base
BV_{CBO}: Electron avalanche breakdown voltage

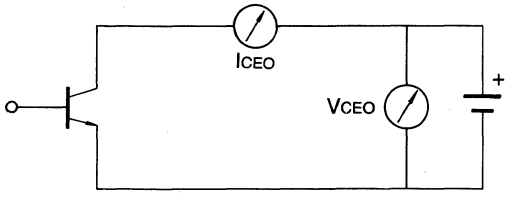
The parameter n is found to be in the range of about 2 to 10 experimentally.

- Emitter-base voltage (V_{EBO})



The reverse voltage which may be applied before breakdown between emitter and base, when the collector is open circuited.

• Collector-emitter voltage (V_{CEO})

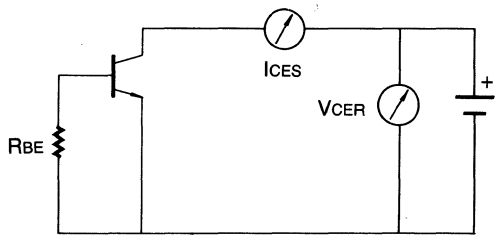


The reverse voltage which may be applied before breakdown between collector and emitter, when the base is open circuited. Determined by V_{CBO} and h_{FE}

$$V_{CEO} = V_{CBO} \cdot n\sqrt{\frac{1}{h_{FE}}}$$

The parameter n is determined experimentally.

• Collector-emitter voltage (V_{CER})

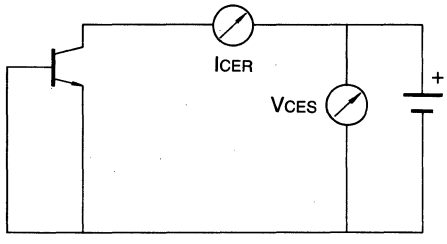


The reverse voltage which may be applied before breakdown between the collector and emitter when the resistor connected between base and emitter.
Determined V_{CBO} and R_{RE}.

$$V_{CER} = V_{CBO} \cdot n\sqrt{1 - \frac{I_{CBO}(rbb' + R_{BE})}{V_{TF}}}$$

V_{TF}: The forward threshold voltage between the base an emitter.

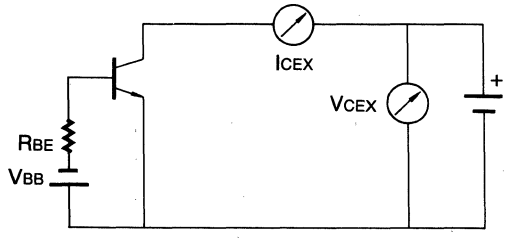
• Collector-emitter voltage (V_{CES})



The reverse boltage which may be applied before breakdown between the collector and emitter when the base and collector are shorted.

$$V_{CES} = V_{CBO} \cdot n\sqrt{1 - \frac{I_{CBO} \cdot rbb'}{V_{TF}}} \approx V_{CBO}$$

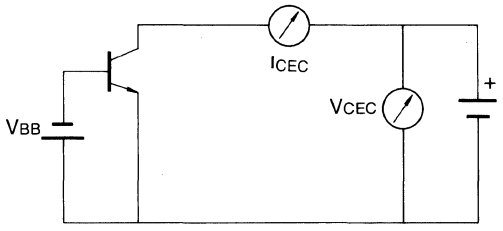
• Collector-emitter voltage (V_{CEX})



The reverse voltage which may be applied before breakdown the collector and emitter under the condition that the base-emitter is reverse biased through a resistor.

$$V_{CEX} = V_{CBO} \cdot n\sqrt{1 - \frac{I_{CBO}(rbb' + R_{BE})}{V_{TB} + V_{BB}}}$$

• Collector-emitter voltage (V_{CEC})

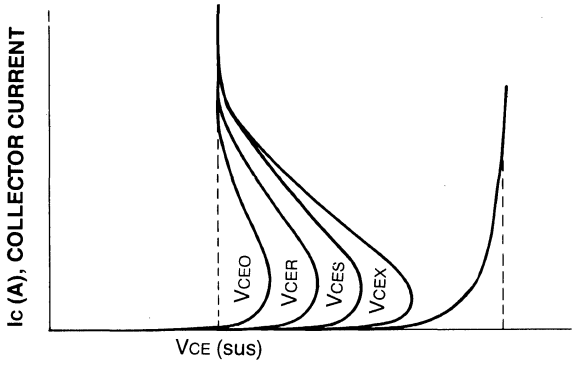


The reverse voltage which may be applied before breakdown the collector and emitter under the condition that the base-emitter is reverse biased without resistor.

$$V_{CEC} = V_{CBO} \cdot n \sqrt{1 - \frac{I_{CBO} \cdot rbb'}{V_{TF} + V_{BB}}} \approx V_{CEO}$$

Generally, this is expressed as V_{CEX}.

The relationship between these ratings is, generally, $V_{CBO} > V_{CEX} > V_{CER} > V_{CEO}$.



5.2 Current ratings

Current ratings mean the maximum current that can be passed through any terminal. The current is limited by the current handing capabiloty of the bonding wires. For current pulses, the limit is higher than for dc since the thermal capacitance of the wire prevents instantaneous heating.

1) Diodes

• Peak forward current (I_{FM})
Limited by the power rating. Current up to this value may be repeatly passed through the device.

• Average forward current (I_O)
The average value of the forward current, when a AC wave is rectified. DC current of this value may be passed continuously.

• Surge current (I_{FS})
The current that may be instantaneously within a specifried time.

2) Transistors

• Collector current (I_C)
This value means the maximum current that can be permitted at collector, and determined as follow:
— Under a condition of Tj less than Tj (max), breakdown or degradation of characteristics shall not occur when $I_C \leq I_C$ (max)
— The time that I_C max shall as rule be once for 5 minutes.
— In case of switching use, the current shall not be restricted to ½-⅓ of its peak value.
— The following values shall be used as rough indications for the lower limit of h_{FE}
Medium power use $h_{FE} = 10$
High power use $h_{FE} = 3$

• Base current (I_B)
Generally, the current is not determined. Base current at which breakdown will not occur are as follows.
Low power use $i_C \leq 1A$ . . . $I_B \leq I_C$
High power use $I_C \geq 1A$ . . . $I_B \frac{1}{2} I_C$

5.3 Temperature ratings

These temperatures are mainly determined by the materials of the semiconductor and package and assure that the failure rate will be under a certain value when the device are operated or stored at these temperatures.

Material	T_j Max	Remark
Ge	75- 90°C	
Si	100-150°C	
Planar-Si	150-200°C	Stabilized Surface Type

Relation of life time — Junction temperature can be determined as follow.

$$\text{Log } Lm = A + \frac{B}{T_J}$$

A, B: constant of transistor
Lm: average life time

5.4 Power rating

The indicated maximum admissible junction temperature must not be exceeded because this could changes or cause the destruction of the device. Since the user cannot measure this temperature, data sheets also reveal the maximum admissible power dissipation usually in the form of a derating curve.

1) Diodes
Generally, in case of diodes, the power rating is not specified. Since the major portion of the power dissipated in diodes is in a forward direction, the power rating will be inevitably determined by specified the forward current.

2) Transistors
The collector power dissipation P_C and the total power dissipation P_T is specified.

$$P_C = \frac{Tj\text{-}Ta}{Rth\ (j\text{-}a)}$$ free air

$$P_T = \frac{Tj\text{-}Ta}{Rth\ (j\text{-}c)}$$ with an infinitely heat sink.

Ta: Ambient temperature, normaly 25°C.
Tc: Case temperature, normaly 25°C.

Rth (j-a): thermal resistance between junction and ambient.
Rth (j-c): thermal resistance between junction and case.

5.5 Criterion of derating design

Derating Factor		Diode	Transistor	IC	Remark
Temperature	Junction temperature	below 110°C *(below T_j=60°C)	S/S below 125°C Power below 150°C	below 125°C	Ge: below 65°C
	Ambient temperature	T_a=0—45°C			
	Other	Power dissipation, Thermal condition T_j=Pd×Rth (j-a)+T_a			
Humidity	Relative humidity	RH=40-80%	RH=40-80%	RH=40-80%	
	Other	Generally, print circuit board must be coated against a water-drop, which formed by sudden drop of a temperature			
Voltage	Endurance voltage	below V_{CC} (max)×0.8 *V_{CC} (max)×0.5		according to catalogue spec.	
	Over load voltage	If the electrostiatic destruction is assumed, supply voltage must be protected to overload.			
Current	Average current	below I_C (max)×0.5 *below I_C (max)×0.25	below I_C (peak)×0.8	below I_C (max)×0.5 (especially power IC)	
	Peak current	below I_C (peak)×0.8	below I_C (peak)×0.8	below I_C (peak)×0.8	
Power	Average power	below Pd (max)×0.5 (especially zener diode)	below Pd (max)×0.5 (especially power transistor)	below Pd (max)×0.5 (especially power application)	
Pulse	SOA	Do not excess maximum rating			
	Surge	below I_F (surge)	below I_C (peak)	below I_c (peak)	

Note: 1. Exclude special using condition.
2. All derating factor must be satisfied simultaneously.
*For high reliability application.

6. SAFE OPERATING AREA

A number of factors such as secondary breakdown, power dissipation ability, voltage and current and voltage ratings, and ambient temperature critically affect the performance of power transistors in circuit applications. The factors define the safe operating areas (SOA) for the forward biased and reverse biased modes, within which each device can be safely operated without failure or degradation.

6.1 DC forward biased SOA

A transistor working in the active region is subjected to voltage and current at the same time and dissipates power. As shown Fig. 1, the four factors limiting the dc forward biased SOA of a particular power transistor are as follow.

(1) Collector current
(2) Thermal limit
(3) Secondary breakdown
(4) Open base breakdown voltage, V_{CEO} (sus)

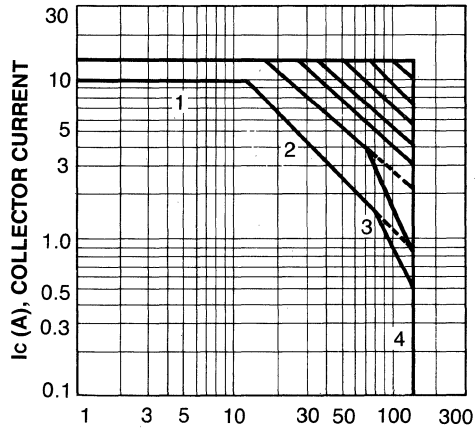


Fig. 4. Example of SOA

Current limit (I_C): region 1 of Fig. 4.
The region 1 is limited by the collector current rating.

Thermal limit: region 2 of Fig. 4.
The region 2 is limited by the maximum operating temperature and thermal resistance of transistor.
In Fig. 1, the case temperature T_C is constant (normaly 25°C); therefore the power limitation is

$$P_D = \frac{Tj\ (max) - 25°C}{Rth\ (j\text{-}c)}$$

Tj (max): maximum junction temperature
Rth (j-c): thermal resistance between junction and case.

Tj (max) is normally 150°C for plastic transistors. If power is applied in excess of this value, the transistor is not necessarily destroyed, but the mounting system of the die or the plastic can deteriorate. For power pulses, the limit is higher than for DC especially for short pulses due again to thermal capacitance.

Secondary breakdown limit ($I_{S/B}$) : region 3 of Fig. 4.
Theregion is limited by secondary breakdown capability. The higher operating voltage, current gathering occurs at the emitter periphery. Finally thermal runaway (hotspot), it is said to be the temperature at which semiconductors become intrinsic, may occur. There, the $I_{S/B}$ limit is specified at the point where junction reaches the melting point of the mounting solder.

Open base breakdown voltage (V_{CEO}) : region 4 of Fig. 4.

The voltage of collector-emitter must not excess the absolute maximum rating; not even a very short pulse is permissable. If voltage is applied in excess of this value, the transistor might be destory.

6.2 Measuring the SOA

Various proposal have been made for practices in measuring to determine the SOA; however, they can be summarized into the following three categories.

1) Over-the-hill method

The principle of the over-the-hill method is shown in Fig 2. The base bias condition is set to a desired one, and high voltage pulses are supplied across the collector and the emitter. Voltage and current waveforms are monitored at terminals A and B, until secondary breakdown occurs.

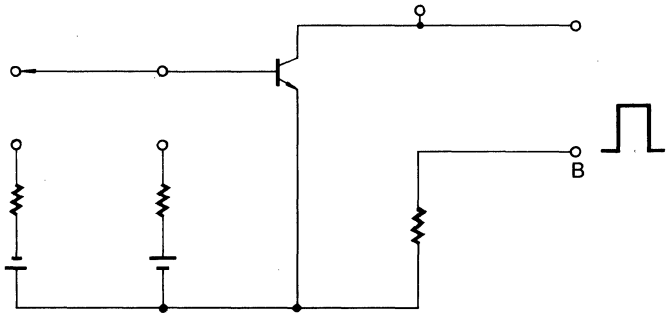


Fig. 5. Over-the-hill method

2) Latching medthod

The measurement setup is shown in Fig. 6. A fixed voltage is supplied across the collector and the emitter, and the base bias pulse condition is varied until secondary breakdown occurs.

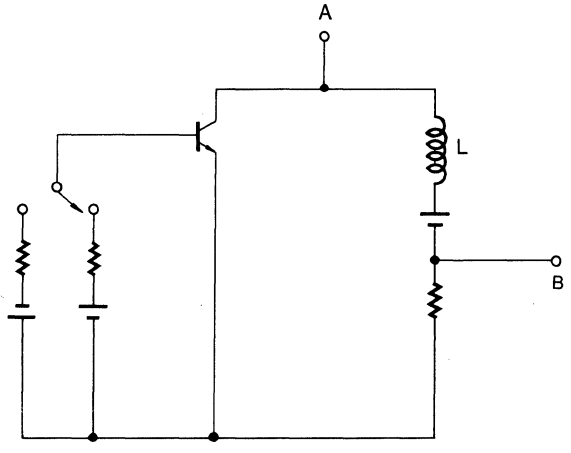


Fig. 6 Latching method

3) ΔV_{BE} method

The over-the-hill and the latching methods read the secondary breakdown directly. But ΔV_{BE} method measures the level at which the increase of junction temperature and hotspot occurs, as shown in Fig. 7. Variation in junction temperature can be determined from the thermal coefficient of ΔV_{BE} which is approximately $\Delta V_{BE}/\Delta T$=2mV/°C (at I_E=2mA). The transistor is driven by current pulses of the required condition and the temperature rise in the junction is measured by checking the emitter waveform (measurement of ΔV_{BE}, shown in Fig 7-b). The occurrence of a hotspot is checked by measuring the ΔV_{BE} level.

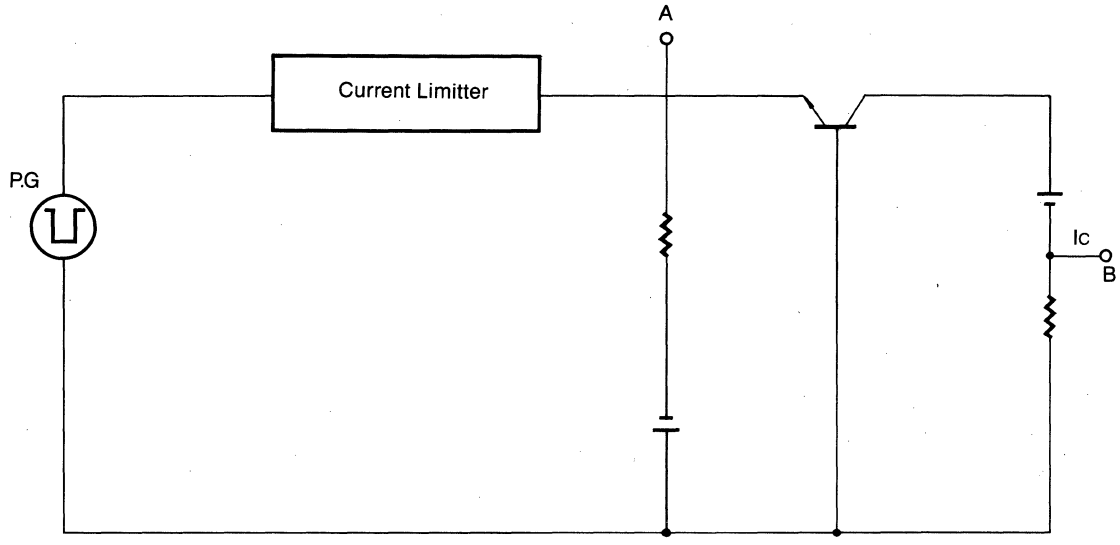


Fig. 7-a ΔV_{BE} measurement circuit

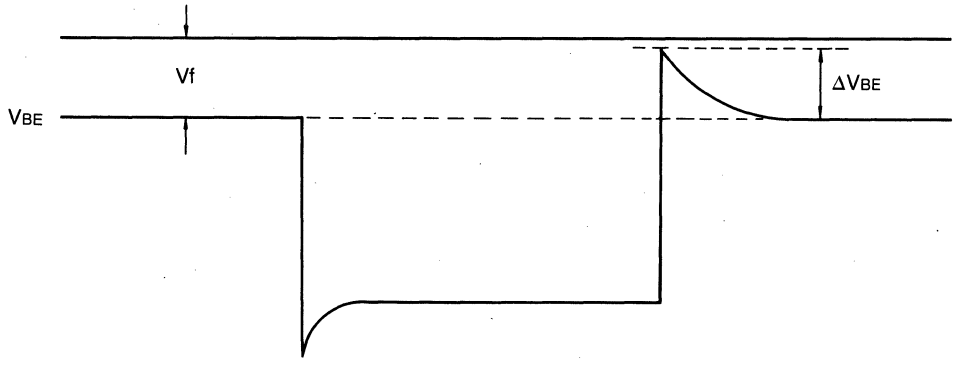
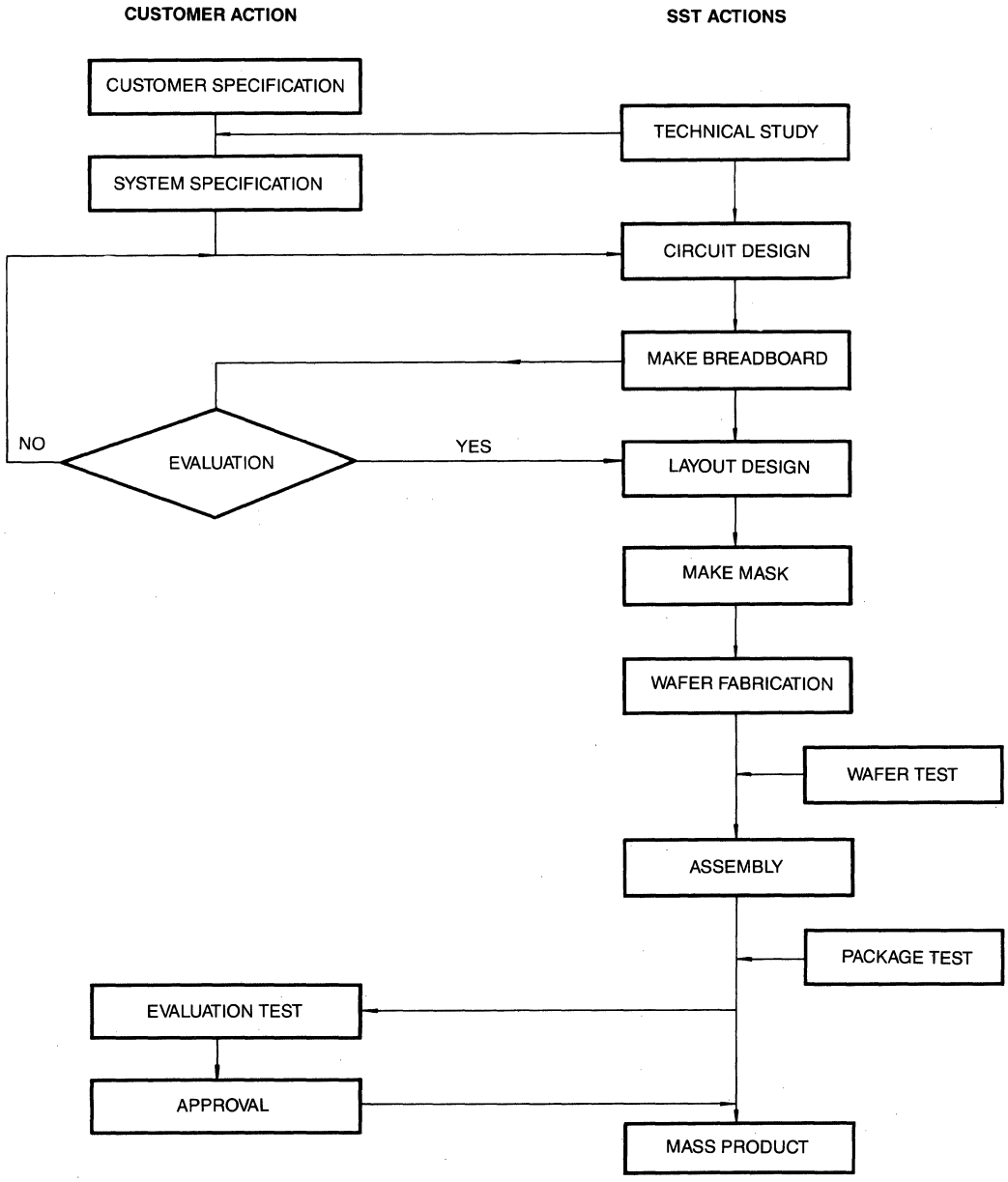


Fig. 7-b ΔV_{BE} wave form

7. INTRODUCTION TO CUSTOM DESIGN SERVICE

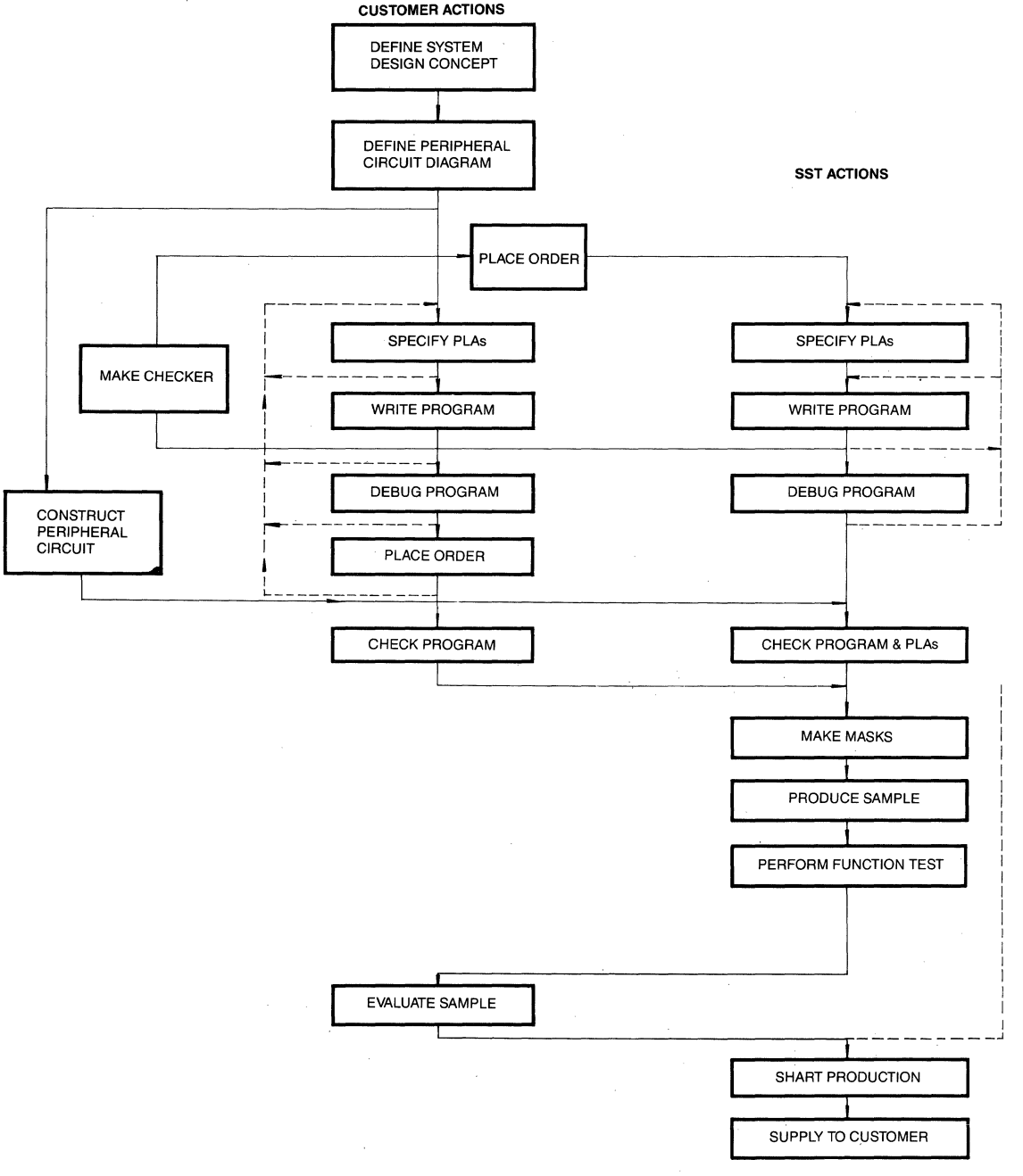
For many application, standard integrated circuits may be inappropriate from the standpoints of cost, size, power consumption or reliability. Moreover unique features demanded by proprietary products often require entirely new circuit configurations. SST will be ready to receive any customer's special order when customer needs some special IC of his own; for example, bipolar technology, C-MOS technology and 4 bit one chip micro computer.

7.1 Bipolar/C-MOS technology development sequence



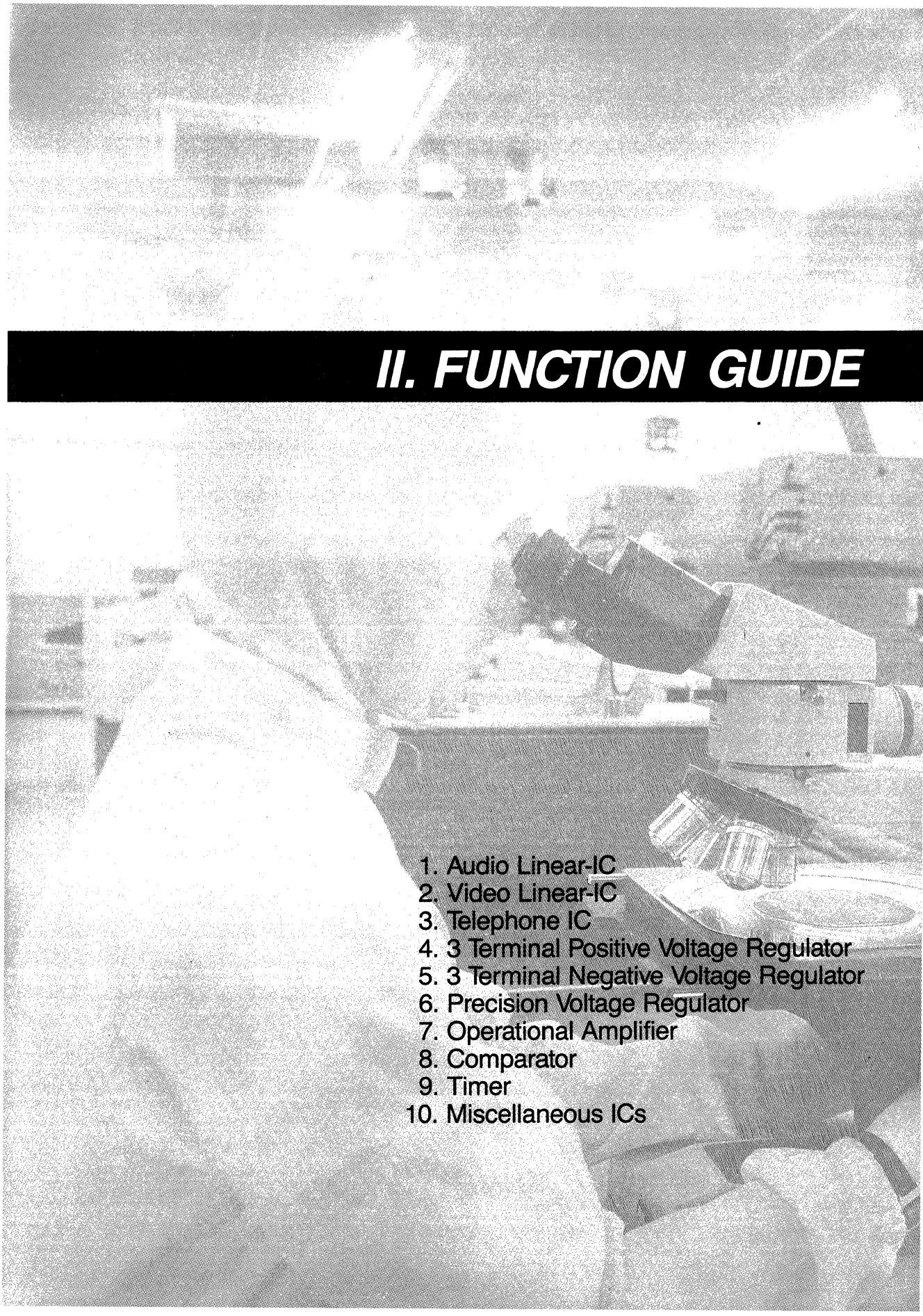
7.2 Development of a Product using the 4 bit one chip microcomputer

The SST 4 bit one chip microcomputer is a mask-programmed device intended for high-volume applications. The contents of the program memory (ROM) and various programmable logic arrays (PLAs) are fixed at the time of manufacture. Programs may be written by customer, by SST Semiconductors or by an independent consultant. The diagram below indicates the stages of a product development.



SYMBOLOGY

A_V	Voltage gain
B V_{CBO}	Collector-base breakdown voltage
B V_{CEO}	Collector-emitter breakdown voltage
B V_{EBO}	Emitter-base breakdown voltage
C_C.rbb≫	Collector-base time constant
Cob	Output capacitance
Cre	Reversew transfer capacitance
f	Frequency
f_T	Current-gain bandwidth product
G_{PE}	Power gain
h	Parameters of h (hybrid) matrix
hi	Input impedance
h_O	Output admittance
hr	Reverse voltage transfer ratio
h_{FE}	DC current gain
I_{AGC}	AGC current
I_B	Base current
I_C	Collector current
I_{CBO}	Collector-base cutoff current
I_{ECO}	Collector-emitter cutoff current
I_{CP}	Peak collector current
I_E	Emitter current
I_{EBO}	Emitter-base cutoff current
NF	Common source noise figure
NL	Common source noise level
P_C	Collector dissipation
P_D	Power dissipation
PW	Pulse width
R_{BE}	Resistance between base and emitter
Rg	Source resistance
R_L	Load resistance
Rth	Thermal resistance
t	Time
td	Delay tiem
tf	Fall time
toff	Turn-off time (ts+tf)
tr	Rise time
Ta	Ambient temperature
T_C	Case temperature
Tj	Junction temperature
Tstg	Storage temperature
V_{AGC}	AGC voltage
V_{BB}	Base supply voltage
V_{BE}	Base-emitter voltage
V_{BE} (sat)	Base-emitter saturationvoltage
V_{CB}	Collector-base voltage
V_{CBO}	Collector-base voltage (open emitter)
V_{CE}	Collector-emitter voltage
V_{CE} (sat)	Collector-emitter saturation voltage
V_{CEO}	Collector-emitter voltage (open base)
V_{EBO}	Emitter-base voltage (open collector)
V_{EE}	Emitter supply voltage



II. FUNCTION GUIDE

1. Audio Linear-IC
2. Video Linear-IC
3. Telephone IC
4. 3 Terminal Positive Voltage Regulator
5. 3 Terminal Negative Voltage Regulator
6. Precision Voltage Regulator
7. Operational Amplifier
8. Comparator
9. Timer
10. Miscellaneous ICs

2.1 Audio Application

A. FM Front End

Type	Package	Function			Use			Remark
		RF	OSC	MIXER	R/C	Car	Hi-Fi	
†KA2249	7 SIP	*	*	*	*			V_{CC}=1.8~7V
††KA22491	9 SIP	*	†	†	†			V_{CC}=1.6~6V

B. FM/AM RF IF and Detector System

Type	Package	Function						Use			Remark
		AM RF CONV	AM IF AMP	AM DET	FM IF AMP	FM DET	S/M	R/C	Car	Hi-Fi	
KA1241	14 DIP		*	*	*			*			V_{CC}=3.5~10V
KA2241	16 DIP		*	*	*	*	*	*			V_{CC}=3.5~10V
KA2243	16 DIP		*	*	*	*	*	*		*	V_{CC}=3.5~16V I_{CC}=15mA typ.
KA2244	9 SIP				*	*	*		*		3 Stage diff-amp
††KA22441	16 ZIP				*	*	*		*		V_{CC}=7.5~16V
†KA2245	7 SIP				*	*			*		V_{CC}=8~16V
†KA2247	16 DIP	*	*	*	*	*	*	*			V_{CC}=3~8V
††KA22471	16 DIP	*	*	*	*	*	*	*			V_{CC}=3~8V
†KA2248	16 DIP	*	*	*	*	*	*	*			V_{CC}=1.8V (min)

C. Audio Stereo Multiplex Decoder

Type	Package	PLL	Lamp Driver	VCO Stop	Sep. Cont.	Use			Remark
						R/C	Car	Hi-Fi	
KA2261	16 DIP	*	*	*	*	*	*		A_V=-1.4dB
††KA2262	16 ZIP	*	*	*	*		*		SNC/HCC
KA2263	9 SIP	*	*	*		*	*		A_V=0dB
††KA2263N	9 SIP	*	*	*		*	*		A_V=0dB
†KA2264	9 SIP	*	*	*		*			V_{CC}=1.8V (min)
††KA2265	16 DIP	*	*	*	*	*	*	*	VCO Non-Adjusting MPX

† New Product
†† Under development

D. Audio Power Amplifier

Type	Package	V_{CC} (V)	Output Power		Use			Remark
			R_L=4 ohm	R_L=8 ohm	R/C	Car	Hi-Fi	
KA2201/A/B	8 DIP	6		0.5W	*			V_{CC}=3~14V
KA2201N	8 DIP	9		1.2W				V_{CC}=3~14V
KA2206	12 DIP/F	9	2.3W×2		*			Dual Power Amp.
†KA22061	12 DIP/F	9	2.3W×2		*			Dual Power Amp.
†KA2209	8 DIP	3	120mW×2		*			V_{CC}=1.8V (min)
††KA2210	12 SIP H/S	13.2	5.5W×2			*		V_{CC}=10~16V
KA2212	9 SIP	6		0.5W	*			V_{CC}=3.5~14V
KA2213	14 DIP H/S	6	1W		*			Pre Amp. with ALC
††LM386	8 DIP	6		0.325W	*			V_{CC}=4~12V

E. Pre-Amplifier

Type	Package	Function	Use			Remark
			R/C	Car	Hi-Fi	
KA1222	8 SIP	Dual pre-amplifier	*			V_{CC}=2~6V
KA2220	9 SIP	Pre-amplifier with ALC	*			V_{CC}=3~15V
KA2221	8 SIP	Dual pre-amplifier		*	*	Voltage Regulator Included
KA2222	8 DIP	Dual pre-amplifier	*			V_{CC}=2~6V
†KA2223	16 DIP	5 Step graphic equalizer amp	*	*	*	V_{CC}=5~12V
KA2224	14 DIP	Dual pre-amplifier with ALC	*		*	V_{CC}=4~13V
†KA2225	16 DIP	Dual pre-amplifier with Mute	*			V_{CC}=1.8~6V
†KA2226	16 DIP	Dual pre-amplifier with ALC	*		*	Included ALC diode
†KA2227	16 DIP	Dual pre-amplifier with ALC	*		*	Included ALC diode

F. LED Level Meter Driver

Type	Package	Function	Remark
KA2281	16 DIP	5 Dot dual red/yellow/green LED driver	VU scale, input amplifier Reference voltage included
KA2283	16 DIP	5 Dot dual red/yellow/green LED driver	Log scale, input amplifier Reference voltage included
KA2284	9 SIP	5 Dot mono green LED driver	VU scale Reference voltage included

† New Product
†† Under Development

(Continued)

Type	Package	Function	Remark
KA2285	9 SIP	5 Dot mono red LED driver	VU scale Reference voltage included
KA2286	9 SIP	5 Dot mono red LED driver	Linear scale Reference voltage inclued
KA2287	9 SIP	5 Dot mono green LED driver	Linear scale Reference voltage included

2.2 Video Application (TV use)

Application	Type	Package	Circuit Function
Sound IF	KA2101	14 DIP	IF amp, IF limitter, IF detector, Electronic attenuator, Audio driver
Sound Multiplex SIF Sub System	††KA2105	9 SIP	IF amp, IF limiter, IF detector
Sound Multiplex SIF Sub System (Dual)	††KA2106	16 DIP	(IF amp, IF limiter, IF detector) x 2
Sound Multiplex SIF Sub System	††KA2268	28 DIP	SIF amp, IF limiter, IF detector, LED drive, Mode SW, Matrix, Electronic attenuator, V_{CO}.
Sound System	KA2102A	14 DIP H/S	KA2101+2.4W Audio power amp.
Sound Mute	†KA2103H/L	9 SIP	Hori sync detector, Integrator, Voltage controller, Comparator
Auto Power Off+Sound Mute	†KA2104	9 SIP	KA2103+Auto power off control
Vertical Deflection	KA2130A	10 SIP H/S	Vert osc/driver/output, Sawtooth generator
	†KA2132	12 DIP/F	Osc, Voltage regulator, Flyback generator, Sync circuit, Pre/Power amp, Ramp generator
	KA1170N	12 DIP/F	Synchronization circuit, oscillator and ramp generator, High power gain amplifier, Flyback generator, Voltage regulator
Vertical Output	†KA2131	10 SIP H/S	Driver, Output, Flyback generator, Pulse shaper
Horizontal Processor	KA1180P	16 DIP	Noise gated horizontal sync separator, Noise gate vertical sync separator, Horizontal oscillator with frequency range limiter, phase comparator between sync pulse and oscillator pulse (PLL), phase comparator between flyback and oscillator pulse (PLL), Loop gain and time constant switching (VCR), composite blanking and key pulse generator protection circuits, Output stage with high current capability.

† New Product
†† Under Development

(continued)

Application	Type	Package	Circuit Function
B/W TV Deflection	††KA2133	16 DIP H/S	Vert osc/driver/output, Sawtooth gen. Hori AFC/osc, Pre-driver
PAL Chroma Processor	KA2151	24 DIP	Chroma amp, DC chroma gain control, ACC peak detector, Burst amp, Killer detector, APC phase detector, DC uni-color control, ACC amp, Burst gate, PAL switch, Flip-Flop, Matrix circuit, Voltage controlled osc.
NTSC Chroma+Deflection+ Video System	KA2153	42 DIP	ACC amp/detector, Killer detector, Phase detector, CW osc, Demodulator, Sawtooth gen, APC detector, X-ray protection, Hori osc/drive, Vert osc/amp, Reverse amp.
PAL Chroma+Deflection+ Video System	††KA2154	42 DIP	ACC amp/detector, Killer detector, Phase detector, CW osc, Demodulator, Sawtooth gen, APC detector, X-ray protection, Hori osc/drive, Vert osc/amp, Reverse amp.
Infrared Preamplifier	†KA2181	8 SIP	AGC, Input separation stage, Output gain control amp.
	††KA2182/3	8 SIP	AGC, Input separation stage, Output gain control Low Voltage use amp.
CTV Video System FET Tuner NPN Tuner	 KA2911 †KA2916	 16 DIP 16 DIP	VIF amp, Limiter, Video detector, Video amp, Noise invert, AGC detector, IF AGC, RF AGC, AFT, Blocking protector
B/W Video System	KA2912	14 DIP H/S	VIF amp, Video detector, Noise canceller, IF, RF AGC, Video amp.
B/W TV VIF/SIF System	††KA2913	16 DIP	VIF amp, Limiter, Video detector, IF RF AGC, SIF amp, SIF Limiter, IF detector
CTV VIF/SIF System	††KA2914	24 DIP	VIF amp, Limiter, Video detector, Video AFT, IF, RF AGC, SIF amp, SIF Limiter, IF detector
VIF+SIF+Deflection System	††KA2915	28 DIP	VIF amp, Limiter, Video defector, Video AFT, IF, RF AGC, SIF amp, SIF limiter, SIF detector Sync separator, Hori osc/driver/AFC, Verf. OSC, Pre driver
Color TV Deflection Processor	KA2921	16 DIP	Sync separator, Noise blanking, Voltage regulator, Vert pre-driver/osc/amp, Hori osc/driver/AFC, X-ray protector, Integrator
Remocon Transmitter	††KS5803	20 DIP	Key in/output, Driver, Output control, OSC, DATA register, Controller

† New Product
†† Under Development

** Video Application (VTR use)

Application	Type	Package	Circuit Function
Write & Read Amplifier	†KA2984	28 DIP	Sync Tip Clamp, Dynamic emphasis (Nonlinear emphasis) Main Pre-Emphasis, White/Dark Clip, Frequency Modulator. Rec Buffer amplifier
Video Signal Processor	†KA2985	28 DIP	Sync Slicer, Video output amplifier REC MODE — Video AGC (Keyed+Peak to Peak DET Type) — Monitor Squelch for EE P B MODE — FM Limitter — FM Modulator — Dynamic De-Emphasis — Noise canceller — Chroma Mix amplifier — White Peak Clipper
Chroma Signal Processor	†KA2986 †KA2988	28 DIP	Automatic color, Burst Pre-emphasis circuits, converter, Automatic frequency controller for chroma signal, Sub converter, Voltage controlled oscillator ($160f_H$) 4 Phase $40f_H$ signal generator, Voltage controlled oscillator (f=3.579545MHz)
SERVO Controller	†KA2987	28 DIP	Divider for 30Hz Reference Signal Generation Drum speed controller (Linear servo system) Drum phase controller (Digital servo system) Capstan phase controller (Digital servo controller) Assembly recording controller

† New Product

2.3 Telephone ICs

Application	Type	Package	Circuit Function
Tone Ringer	KA2410 KA2411	8 DIP	* Adjustable warbling and 2 frequency tone * External triggering or ringer disable * Adjustable supply initiating voltage * Built-in hysteresis
Tone Ringer with Bridge Rectifier	††KA2418 ††KA2419	8 DIP	* Protect against over voltage * Low current consumption * Allow the parallel operation of 4 devices * Built-in hysteresis * External components are minimized * High output voltage — Non inverting output: KA2418 — Non/Inverting output: KA2419
One Chip Telephone	††KA2414	40 DIP	* Including DTMF generator, tone ringer, speech network and line voltage regulator * DTMF generator use low-cost ceramic generator * Speech network provides two-four wire conversion * I^2L technology provides low 1.4 volts operation
	††KA2417	40 DIP	* Provides all basic telephone station function in single IC * Including DTMF and line voltage regulator * Tone ringer drives piezo electronic transducer and satisfies ears-470 impedance signature requirement * Provides microprocessor interface port for automatic dialing features
DTMF	KS5808	16 DIP	* Direct telephone line operation * Standard 2 of 8 key board use * Tone output: Bipolar output * Mute output: N-CH open drain
	†KA2413	16 DIP	* Wide operating line voltage and current range * Short start up time * External components are minimized * Internal protection of all inputs

† New Product
†† Under Development

(Continued)

Application	Type	Package	Circuit Function
Pulse Dialer	KS5804	16 DIP	* Direct telephone line operation * On-Chip voltage regulator * Power up clear circuitry * 2 of 7 matrix or single contact keyboard * Pulse output: "1" true * Mute output: "0" true
	KS5805A/B	18 DIP	* KS5805A: Pin 2; Vref * KS5805B: Pin 2; Tone output * RC oscillator used as frequency reference * Pulse output: "0" true * Mute output: "0" true
Repertory Pulse Dialer	††KS5806	18 DIP	* 10 number at 16 digits memory * Redial function * Pacifier tone output * PABX pause key input * Uses the inexpensive form A-type Low memory retention current
Speech Network	KA2412A/B/C	14 DIP	* Transmit/Receiver amplifier * Side tone control * Mute function
Tone Decoder	†LM567C	8 DIP	* Touch tone decoding * Sequential tone decoding * Communication paging * High stable center frequency
FM IF Amplifier	†MC3361	16 DIP	* Small current dissipation (Typ. 3.5 mA: V_{CC} 4.0V) * Excellent input sensitivity * Minimum number of external parts required * Used to cordless telephone parts required * Work from 1.8V to 7.0V

† New Product
†† Under Development

2.4 3 Terminal Positive Voltage Regulator

Function	Type	Package	Features	Application
High output Current (I_O=1A)	MC78XXC series	TO-220	Maximum output current 1A External components are minimized internal protection circuit for output short Positive voltage regulator Variable appliction circuit	5V, 6V, 8V, 8.5V 11V, 12V, 15V, 18V and 24V fixed output voltage
Medium output current (I_O=500mA)	MC78MXXC series	TO-220	Maximum output current 500mA External components are minimized internal protection circuit for output short Positive voltage regulator Variable application circuit	5V, 6V, 8V, 10V 12V, 15V, 18V and 24V fixed output voltage

2.5 3 Terminal Negative Voltage Regulator

Function	Type	Package	Features	Application
High output Current (I_O=1A)	††MC79XXC series	TO-220	Output current in excess of 1A Internal thermal overload protection Internal short circuit current limiting	−2V, −5V, −5.2V −6V, −8V, −12V −15V, −18V, and −24V, fixed output voltage

2.6 Precision Voltage Regulator

Function	Type	Package	Features	Application
Adjustable Regulator	††LM723C	14 DIP	Positive or negative supply operation Series, shunt, switching or floating operation 0.01% line and load regulation Output current to 150mA without external pass transistor	Output voltage adjustable from 2 to 37V
33V Regulator	KA33V	TO-92		Electronic tuning system

† New Product
†† Under Development

2.7 Operational Amplifier

Function	Type	Package	Features	Application
OP AMP	LM741C	8 DIP	Internal frequency compensation Short circuit protection	Comparator, DC amp Multivibrator, Summing amp Integrator or differentiator Narrow band or BPF
Dual OP AMP	MC4558C	8 DIP	Internal frequency compensation Short circuit protection Low noise operation	Phone pre-amplifier Tape playback amplifier Schmitt trigger
	MC4558S MC1458S	9 SIP		
Dual OP AMP	††LM358/A	8 DIP	Internal frequency compensation for unit gain Large DC voltage gain Wide power supply range Low input biasing current	DC summing amplifier Power amplification RC active bandpass filter Compatible with all forms of logic
Quad	LM324C LM324/A	14 DIP	Internal frequency compensation Wide supply voltage range Single supply: DC 3V-30V Dual supply: DC+1.5V — +15V	Audio power booster DC amp. Multivibrator Switch, Comparator Schmitt trigger

2.8 Comparator

Function	Type	Package	Features	Application
Comparator	††LM311	8 DIP	Operates from single 5V supply Maximum input current: 250nA Maximum offset current: 50nA Differential input voltage range: +30V Power consumption: 135mW at +15V	Multivibrator output is compatible with DTL and TTL as well as MOS circuits voltage controlled oscillator
Dual Comparator	††LM393/A	8 DIP	High precision comparators Reduced V_{OS} drift over temperature Eliminates need for dual supply Allows sensing near ground Compatible with all forms of logic Power drain suitable for battery operation Low input biasing current: 25nA Low output saturation voltage 250mV at 4mA	Output voltage compatible with TTL, DTL, ECL and CMOS logic system Basic comparator Pulse generator MOS clock driver
Quad Comparator	††LM339/A	14 DIP	Wide single supply voltage range or dual supplies Very low supply current drain (0.8mA)-independent of supply voltage (2mW/Comparator at +5V DC) Low input biasing current: 25nA Input common-mode voltage range includes GND Low output saturation voltage 250mV at 4mA	Compatible with all forms of logic Bi-stable multivibrator One-shot multivibrator Time delay generator Square wave oscillator Pulse generator Limit comparator Crystal controlled oscillator

2.9 Timer

Function	Type	PKG	Features	Application
Timer	NE555C	8 DIP	Maximum operating frequency 500 KHz Adjustable duty cycle	Precision timing Pulse generator
Dual Timer	NE556C	14 DIP	TTL compatible Adjustable duty cycle	Sequential timing Time delay generation

2.10 Miscellaneous ICs

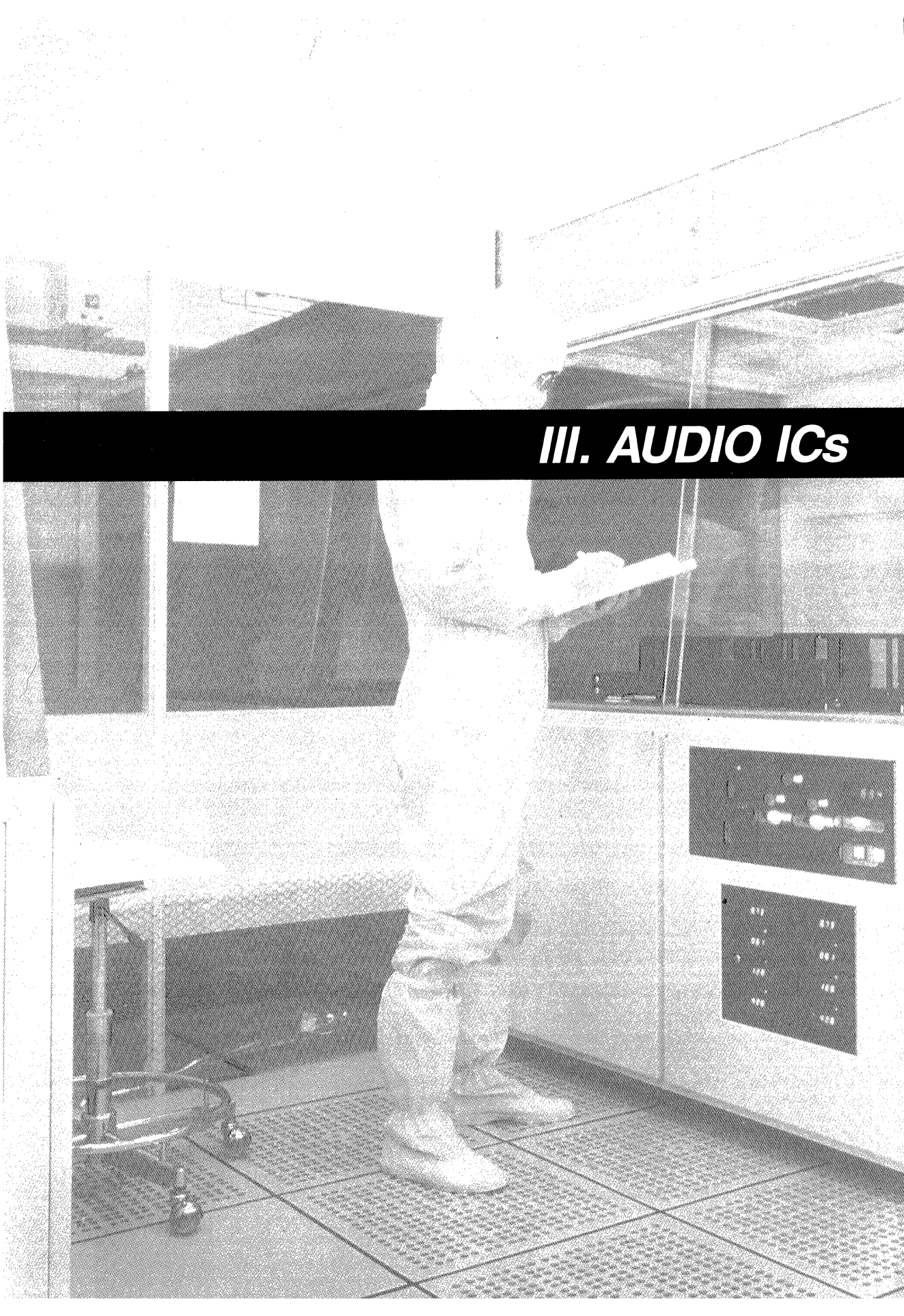
Function	Type	PKG	Features	Application
Toy Radio Control Actuator	KA2301	9 SIP	High gain amplifier, Peak detector Comparator with hysteresis Regulator motor driver	Exclusive custom design
	†KA2302	9 SIP		2 Function
	†KA2303	9 SIP		3 Function
DC Motor Speed Controller	KA2401	8 DIP	Stable voltage reference Reflection coefficient K=20 (Typ)	Medium voltage (6V)
	††KA2402	8 DIP	Stable current source	V_{CC}=1.8 ~ 8V
ADC	††KS7126	40 DIP	3-1/2 Digit LCD Driver	DMM
AD/DA Converter	††KSV3100A	40 DIP	8 Bit A/D+10 Bit D/A Converter 38.5MHz	Video signal processing for CATV converter
Earth Leakage Detector	KA2803	8 DIP	Low power consumption High noise immunity Few external components	Earth leakage detector
Zero Voltage Switch	†KA2804	8 DIP	Easy operation either through the AC line or a DC supply Supply voltage control External component are minimized Negative output current pulse up to 250mA (short circuit protection)	ON, OFF temperature control Time proportional temperature control
8-channel Source Driver	†KA2580A	18 DIP	TTL, CMOS, PMOS, NMOS compatible High output current ratings Internal transient suppression Efficient input/output pin structure	Low voltage LEDs and incandescent lamp
	††KA2588A	20 DIP	TTL, CMOS, PMOS, NMOS compatible High output current ratings Internal transient suppression Efficient input/output pin structure Separated logic and driver. Supply line.	Vacuum flourescent display driver Relay driver Interface between positive logic or negative logic and either negative or split-load supplies

† New Product †† Under Development

2.10 Miscellaneous ICs (continued)

Function	Type	PKG	Features	Application
Quad Line Driver	††MC1488	14 DIP	Current limited output ±10mA Typ. Power-off source impedance 300 ohms Min. Simple slew rate control with external capacitor Flexible operating supply range	Interface between data terminal and data communications equipment
Quad Line Receivers	††MC1489/A	14 DIP	Input resistance 3.0K to 7.0 kilohms Input signal range ±30 Volts Input threshold hysteresis built in response control a) Logic Threshold Shifting b) Input Noise Filtering	Interface between data terminal and data communications equipment

†† Under Development

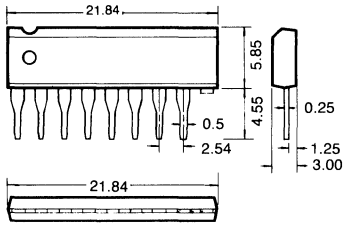


III. AUDIO ICs

DUAL LOW NOISE EQUALIZER AMPLIFIER

The KA1222 is a monolithic integrated circuit consisting of 2 channel pre-amplifier in 8 pin single in-line package.
Minimum operating voltage is 2.5 Volt, thus it is suitable for low voltage application.

8 Sip Unit: mm



FEATURES

- **Wide operating supply voltage range (2.5V ~ 6V).**
- **Low noise (V_{NI} =1.0μ Vrms: TYP).**
- **High channel separation.**
- **Good ripple rejection ratio.**
- **Minimum number of external parts required.**

SCHEMATIC DIAGRAM

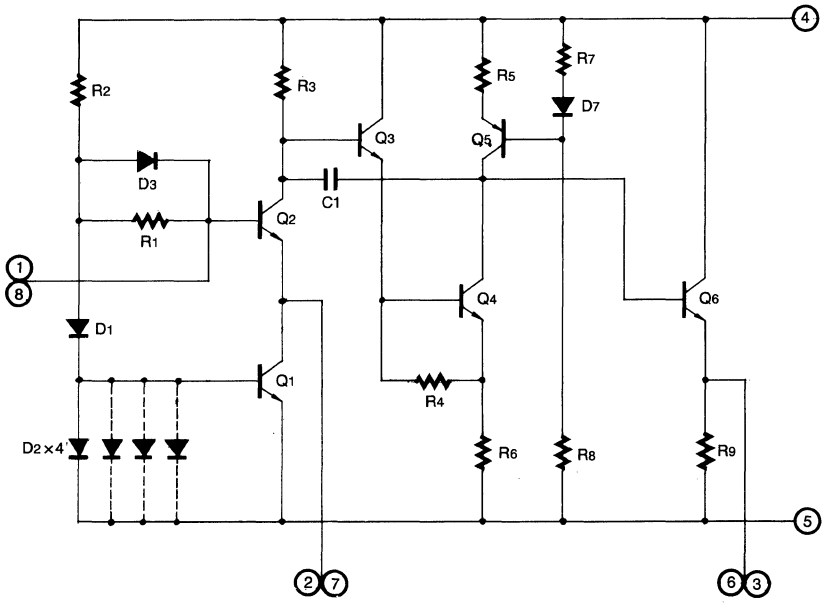


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.5	V
Power Dissipation	P_d	200	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 4V, R_L = 10KΩ, R_g = 600Ω, f = 1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		2.0	6.0	mA
Voltage Gain (Open Loop)	A_{VO}		65	80		dB
Voltage Gain (Closed Loop)	A_V	V_O = 0.2V	33	35	37	dB
Output Voltage	V_O	THD=1%	0.4	0.7		V
Total Harmonic Distortion	THD	V_O = 0.2V		0.1	0.3	%
Input Resistance	R_i			150		KΩ
Equivalent Input Noise Voltage	V_{NI}	R_g = 2.2KΩ BW (−3dB)=15Hz ~ 30KHz		1.0	2.0	μV
Cross Talk	CT	R_g = 2.2KΩ	50	65		dB

TEST CIRCUIT

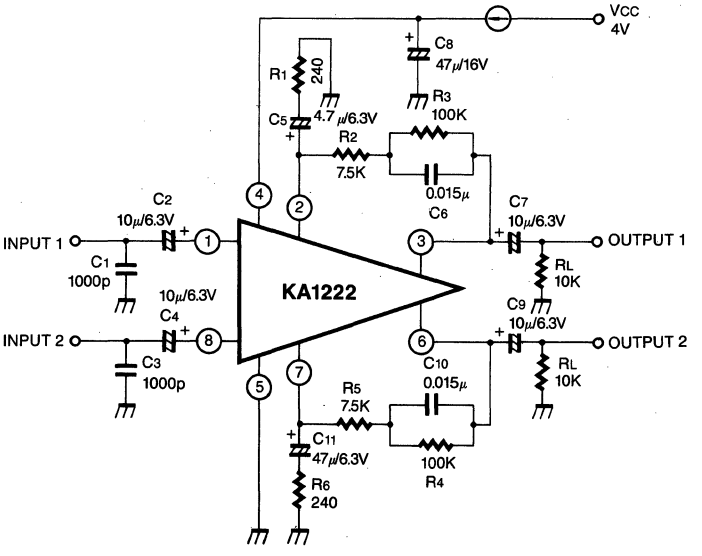
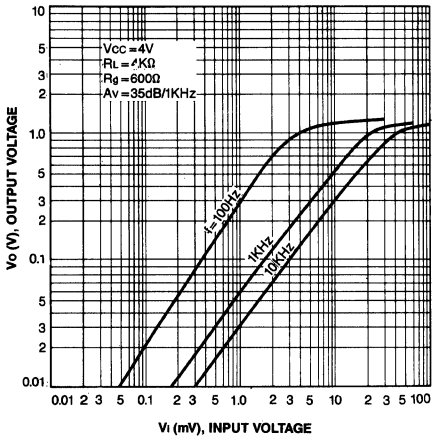
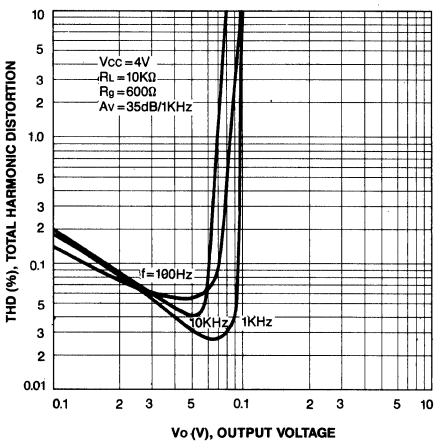


Fig. 2

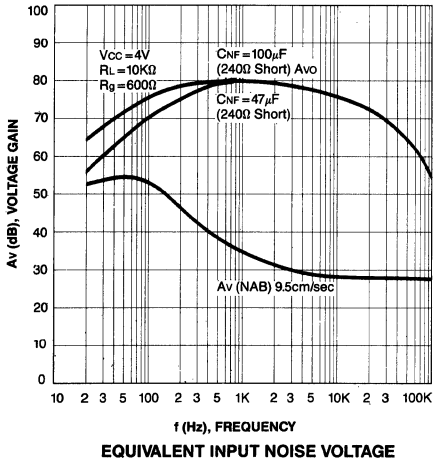
OUTPUT VOLTAGE-INPUT VOLTAGE



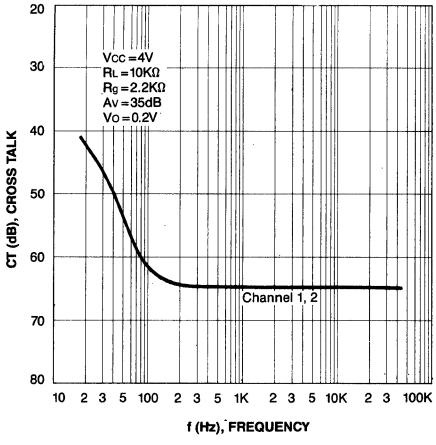
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



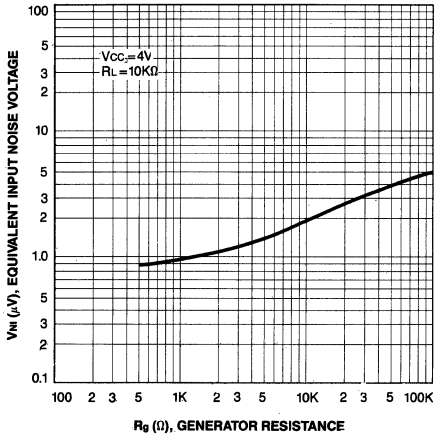
VOLTAGE GAIN-FREQUENCY



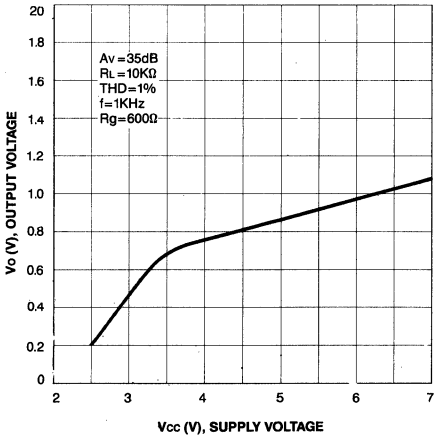
CROSS TALK-FREQUENCY



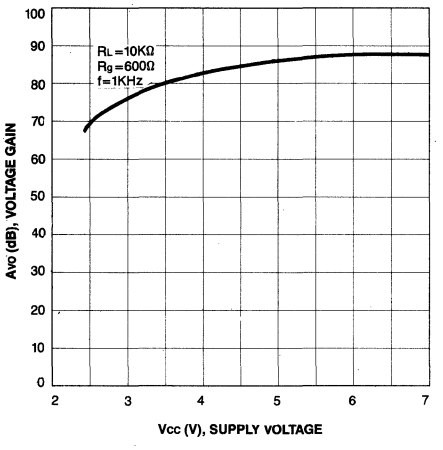
EQUIVALENT INPUT NOISE VOLTAGE -GENERATOR RESISTANCE



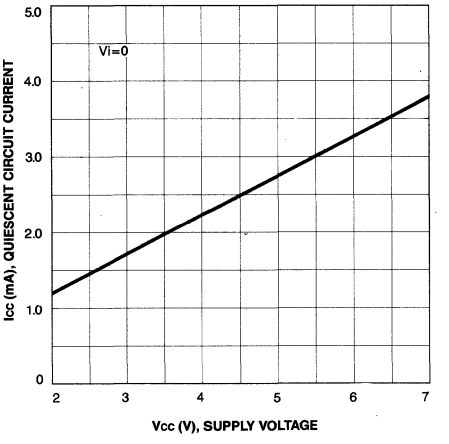
OUTPUT VOLTAGE-SUPPLY VOLTAGE



VOLTAGE GAIN-SUPPLY VOLTAGE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



TYPICAL APPLICATION CIRCUIT

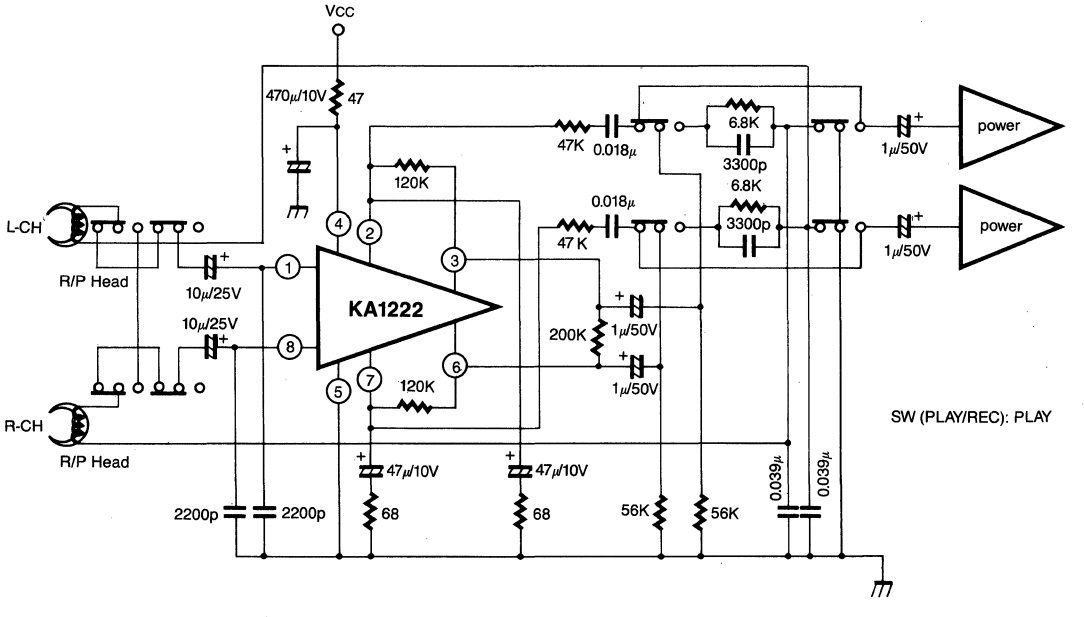
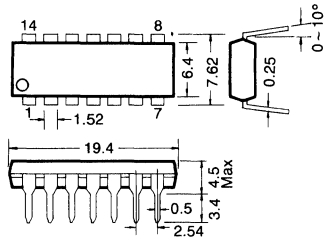


Fig. 3

AM/FM IF AMPLIFIER

The KA1241 is a monolithic integrated circuit consisting of four individual amplifiers and voltage regulator.

14 Dip Unit: mm



FEATURES

- **Suitable for AM/FM Radio.**
- **Wide operating supply voltage range (3.5V ~ 10V).**
- **Low power consumption.**
- **High AM AGC figure of merit.**
- **Good AMR characteristic.**
- **High amplifier gain.**

BLOCK DIAGRAM

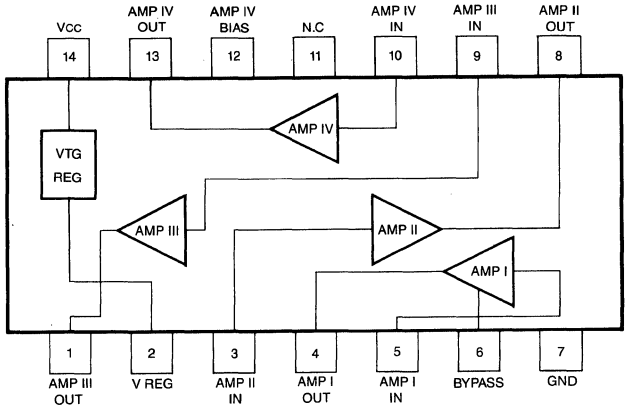


Fig. 1

TEST CIRCUIT

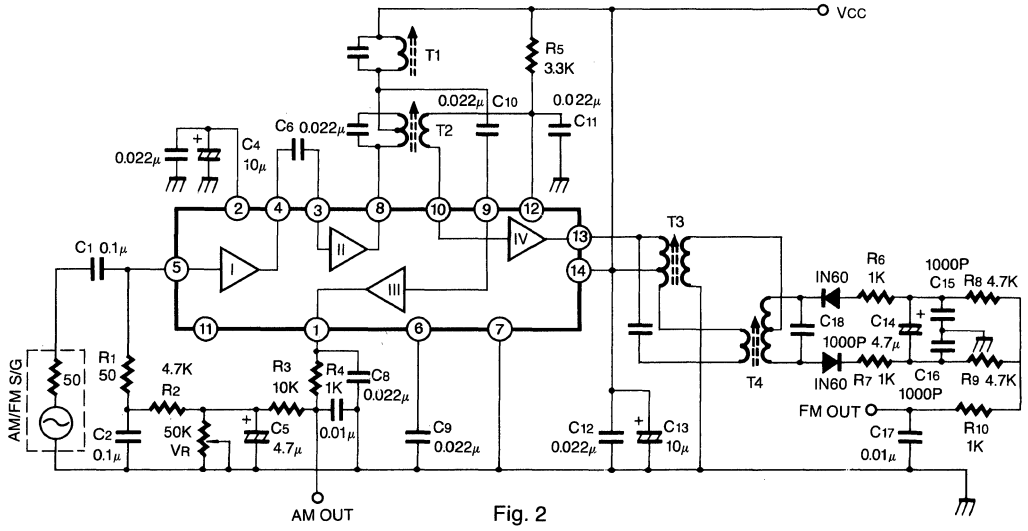


Fig. 2

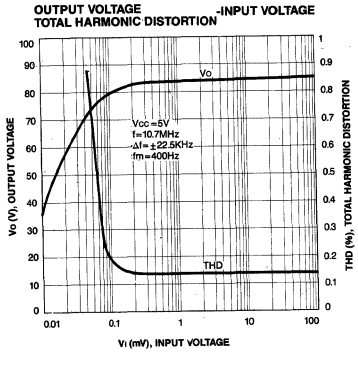
ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

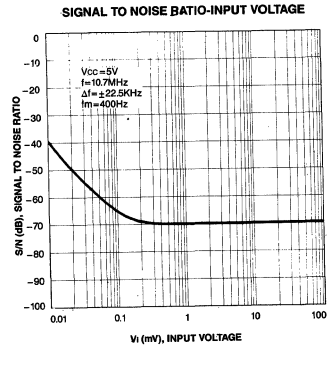
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C, V_{CC} = 5V)

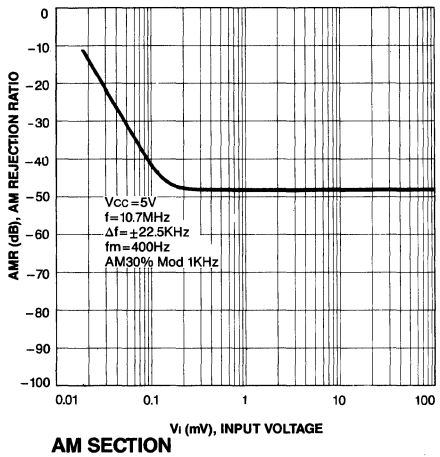
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Regulator Output Voltage	Vreg	Pin 2	2.7	3.0	3.3	V
FM Section (f=10.7MHz, Δf=±22.5KHZ, fm=400Hz)						
Quiescent Circuit Current	I_{CC}	V_i = 0		8	10	mA
Input Limiting Sensitivity	V_i (lim)	−3dB Point from V_O (V_i = 80dBμ)		40	46	dBμ
Detector Output	V_O	V_i = 80dBμ	60	90		mV
Total Harmonic Distortion	THD	V_i = 80dBμ		0.2	1.0	%
AM Rejection Ratio	AMR	V_i = 80dBμ AM: 30% Mod, 1KHz	40	50		dB
Signal to Noise Ratio	S/N	V_i = 80dBμ	60	70		dB
AM Seciton (f = 455KHz, fm = 400Hz, 30% Mod)						
Quiescent Circuit Current	I_{CC}	V_i = 0		8	10	mA
Max Sensitivity	V_i (sen)	V_O = 10mV		20	26	dBμ
Detector Output	V_O	V_i = 60dBμ	75	110		mV
Total Harmonic Distortion	THD1	V_i = 60dBμ		0.3	2.0	%
	THD2	V_i = 80dBμ		1.4	3.0	
Signal to Noise Ratio	S/N	V_i = 60dBμ	45	55		dB

FM SECTION

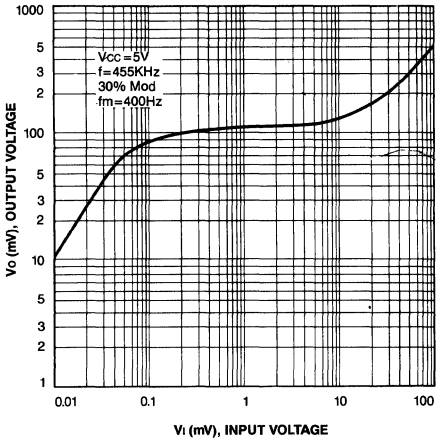




AM REJECTION RATIO-INPUT VOLTAGE

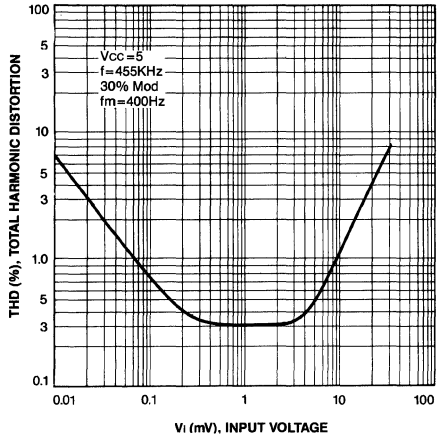


OUTPUT VOLTAGE-INPUT VOLTAGE

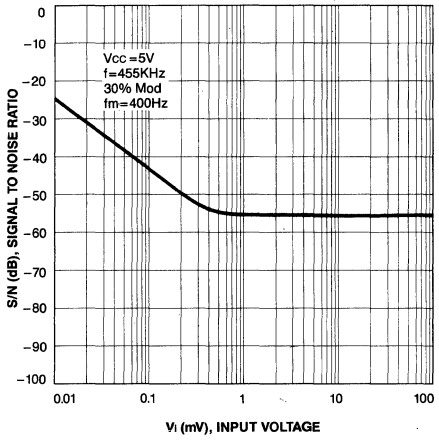


AM SECTION

TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



SIGNAL TO NOISE RATIO-INPUT VOLTAGE



TYPICAL APPLICATION CIRCUIT I

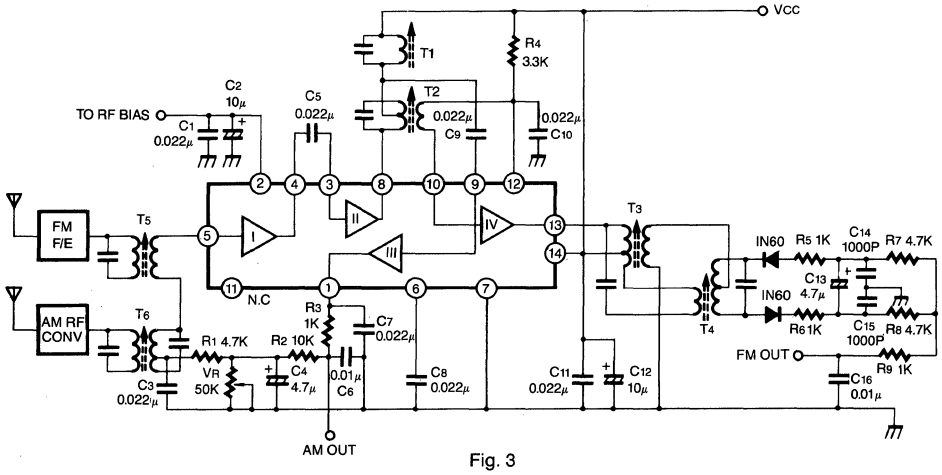


Fig. 3

APPLICATION CIRCUIT II

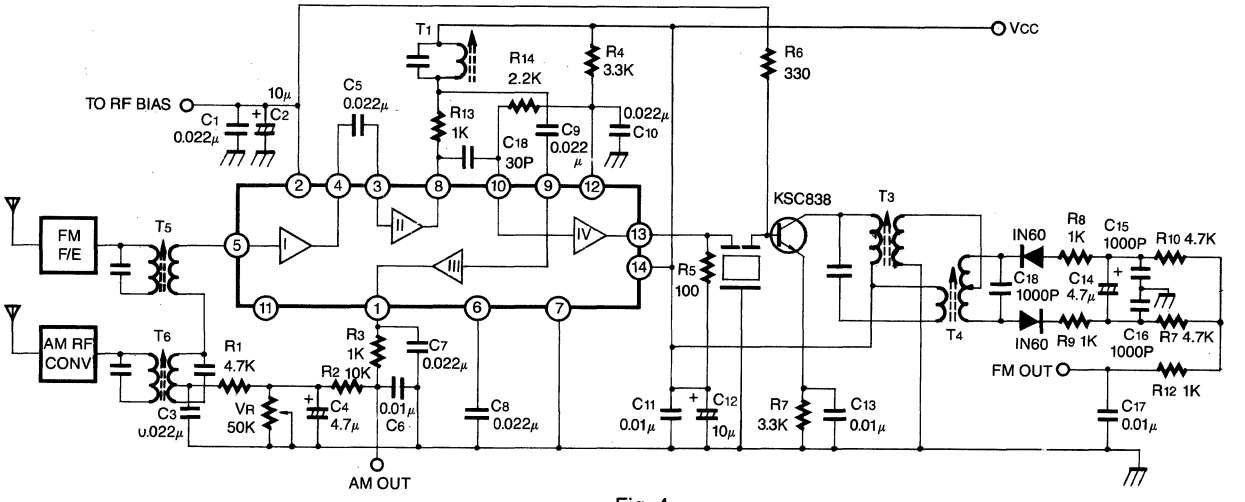
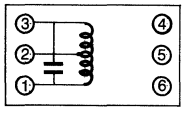


Fig. 4

COIL SPECIFICATIONS

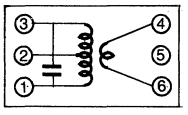
T1



C_o (pF)	f (KHz)	Q_o (%)	TURN		
			6-4	3-2	2-1
180	455	80	33	36	110

Seoul Jupa
SJ-015-472
0.07mmϕ UEW

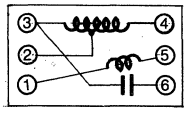
T2



C_o (pF)	f (MHz)	Q_o (%)	TURN		
			1-2	2-3	4-6
50	10.7	90	9	4	2

Seoul Jupa
SJ-015-239
0.1mmϕUEW

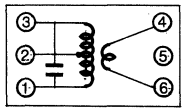
T3



C_o (pF)	f (MHz)	Q_o (%)	TURN		
			4-2	2-3	1-5
50	10.7	100	5½	7	5½

Seoul Jupa
SJ-015-474
0.1mmϕUEW

T4



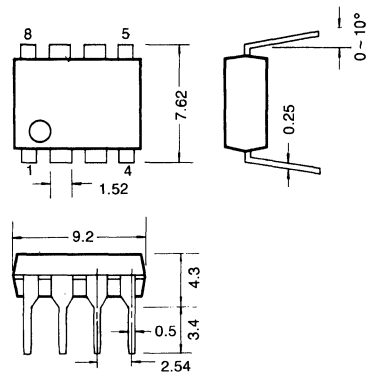
C_o (pF)	f (MHz)	Q_o (%)	TURN		
			4-6	1-2	2-3
30	10.7	110	1	8	8

Seoul Jupa
SJ-015-463
0.1mmϕUEW

0.5W AUDIO POWER AMPLIFIER

The KA2201 is a monolithic integrated audio amplifier in 8 lead dual in the plastic package, designed for audio frequency class B amplifier.

8 Dip Unit: mm



FEATURES

- **Wide operating supply voltage (3V ~ 14V).**
- **Medium output power.**
  P_O =0.5W at V_{CC} =6V, R_L =8Ω, THD=10%.
- **Low quiescent circuit aurrent (I_{CC} =3.5mA: Typ).**
- **Good ripple rejection.**
- **Minimum number of external parts required.**

SCHEMATIC DIAGRAM

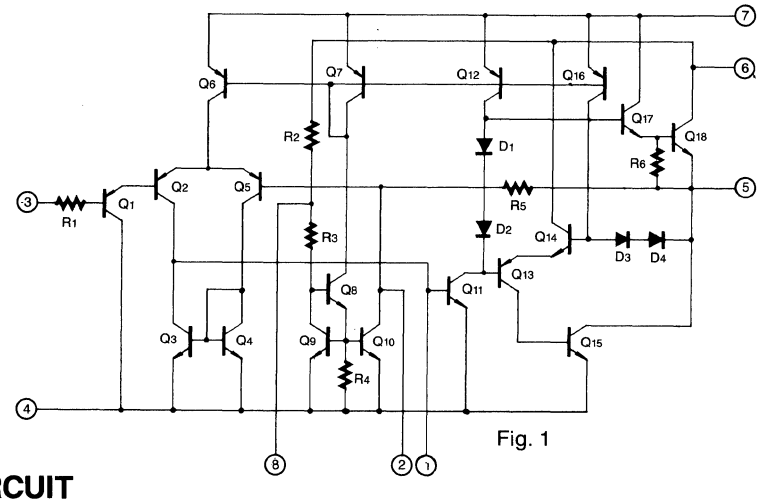


Fig. 1

TEST CIRCUIT

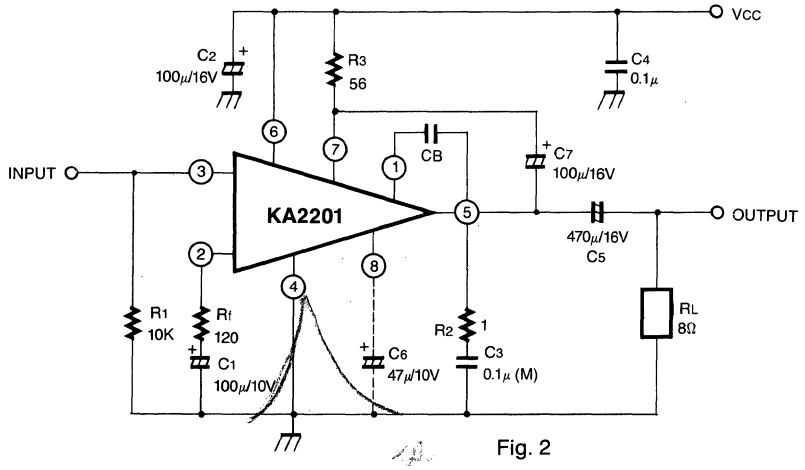


Fig. 2

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

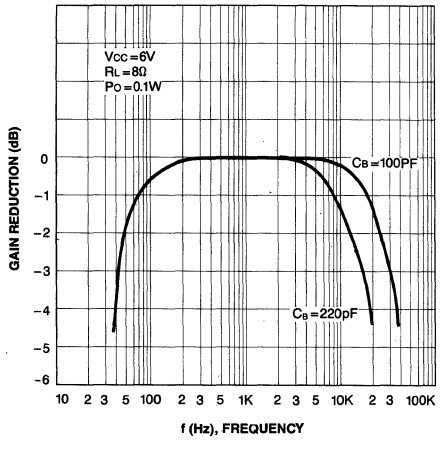
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	V
Output Peak Current	I_O	1.5	A
Power Dissipation	P_d	650	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

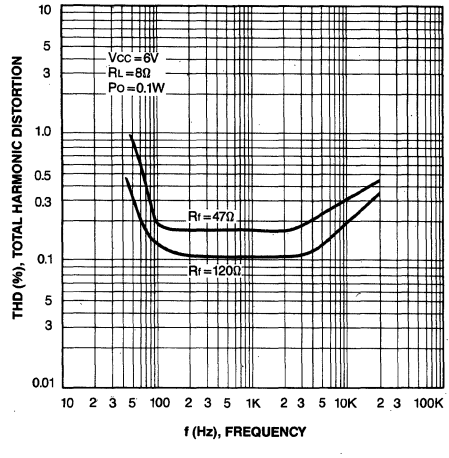
(T_a =25°C, V_{CC} =6V, f=1KHz, R_g =600Ω, R_f =120Ω, R_L =8Ω unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i =0		3.5	7.0	mA
Output Power	P_O	THD=10%	0.4	0.5		V
Total Harmonic Distortion	THD	P_O =100mW		0.3	1.0	%
Voltage Gain (Open Loop)	A_{VO}	Rf=0		75		dB
Voltage Gain (Closed Loop)	A_V	Rf=120Ω	33	36	39	dB
Input Resistance	R_i			5		MΩ
Output Noise Voltage	V_{NO}	R_g =10KΩ BW (−3dB)=50Hz ~ 20KHz		0.3	1.0	mV

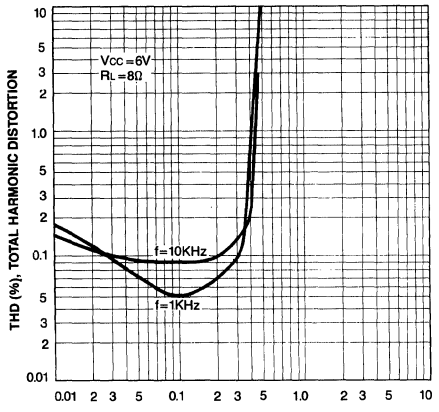
FREQUENCY RESPONSE



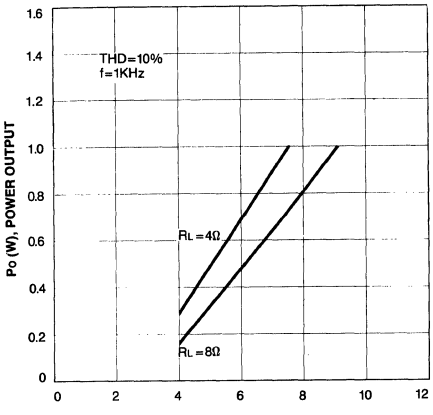
TOTAL HARMONIC DISTORTION-FREQUENCY



TOTAL HARMONIC DISTORTION-POWER OUTPUT

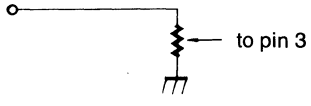


POWER OUTPUT-SUPPLY VOLTAGE



External Components (Refer to test circuit)

R_1: Input biasing resistor
Pin No. 3 is always to be grounded through R_1.
If need volume control, a VR ranging from several hundred ohm to several hundred Kilo-ohm can be used as following.



R_3, C_7: Bootstrap components
This components are used to boost the output power when positive half wave swing.
The capacitor C_7 is chosen enough largely, but not to make the output decreased.

C_1, Rf: Feedback components
The closed loop gain varies depending on this components (C1 and R_f), which are determined as follows.

$$C_1 = \frac{1}{2\pi f_L \cdot Rf} \qquad R_f = \frac{7K}{A_V} (\Omega)$$

where f_L: low cut-off frequency
A_V: the closed-loop gain

C_6: The ripple filter
This capacitor is used to get rid of the ripple to the first amplifier stage and is a factor to influence to the starting time.
The capacitance should be selected so that the above two factors is satisfied.

C_B: Compensation component
The higher cut-off frequency is set by C_B, which contributes to suppress the oscillation at the higher frequency range.

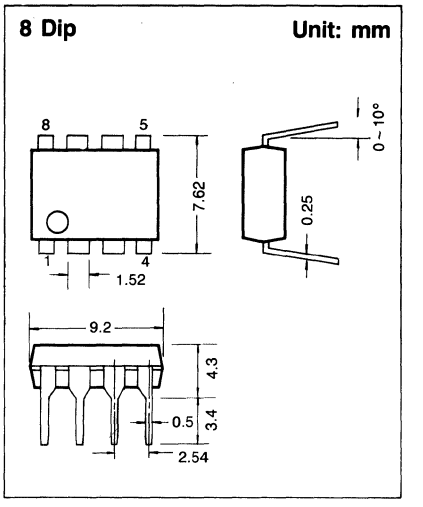
R_2, C_3: Oscillation suppression
The mylar capacitor is to be used for C3 to get a better characteristic for temperature and the frequency.

C_2: Ripple filter for power supply
The large capacitor is required to get an excellent ripple characteristic under the line operation but the small one can be used with the battery.

C_4: High frequency bypass filter in power supply line
It can be an effective method when occur some high frequency trouble in radio application

0.5W AUDIO POWER AMPLIFIER

The KA2201A is a monolithic integrated audio amplifier in 8 lead dual in line package, designed for audio frequency class B amplifier.



FEATURES

- **Wide operating supply voltage range (3.5V~14V).**
- **Medium output power.**
  P_O 0.5W at V_{CC} 6V, R_L =8Ω, THD=10% .
- **Low quiescent circuit current (I_{CC}=3.5mA: Typ).**
- **Good ripple rejection.**
- **Very low crossover distortion.**
- **Minimum number of external parts required.**

SCHEMATIC DIAGRAM

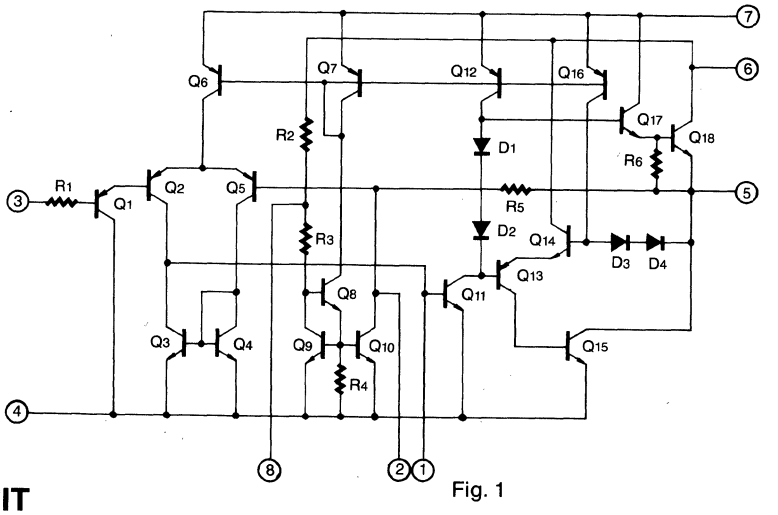


Fig. 1

TEST CIRCUIT

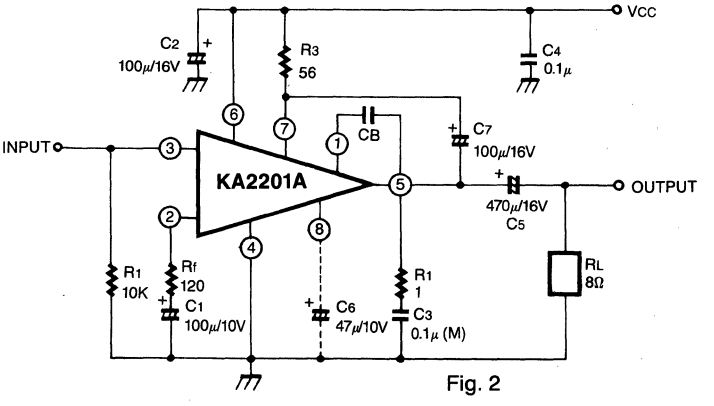


Fig. 2

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	V
Output Peak Current	I_O	1.5	A
Power Dissipation	P_d	650	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

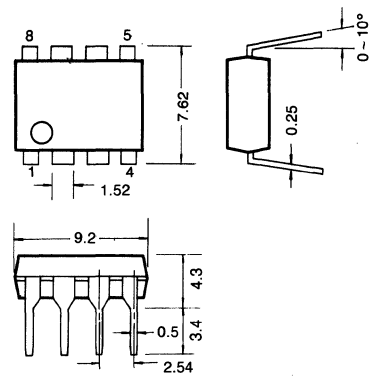
(T_a = 25°C, V_{CC} = 6V, f = 1KHz, R_g = 600Ω, R_f = 120Ω, R_L = 8Ω unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		3.5	7.0	mA
Output Power	P_O	THD = 10%	0.45	0.5		W
Total Harmonic Distortion	THD	P_O = 100mW		0.3	1.0	%
Voltage Gain (Open Loop)	A_{VO}	Rf = 0		75		dB
Voltage Gain (Closed Loop)	A_V	Rf = 120Ω	33	36	39	dB
Input Resistance	R_i			5		MΩ
Output Noise Voltage	V_{NO}	R_g = 10KΩ BW (−3dB) = 50Hz ~ 20KHz		0.3	1.0	mV

0.5W AUDIO POWER AMPLIFIER

The KA2201B is a monolithic integrated audio amplifier in 8 lead dual in the plastic package, designed for audio frequency class B amplifier.

8 Dip Unit: mm



FEATURES

- **Wide operating supply voltage (3V~14V).**
- **Medium output power.**
  P_O=0.5W at V_{CC}=6V, R_L=8Ω, THD=10%.
- **Low quiescent circuit aurrent (I_{CC}=3.5mA: Typ).**
- **Good ripple rejection.**
- **Minimum number of external parts required.**

SCHEMATIC DIAGRAM

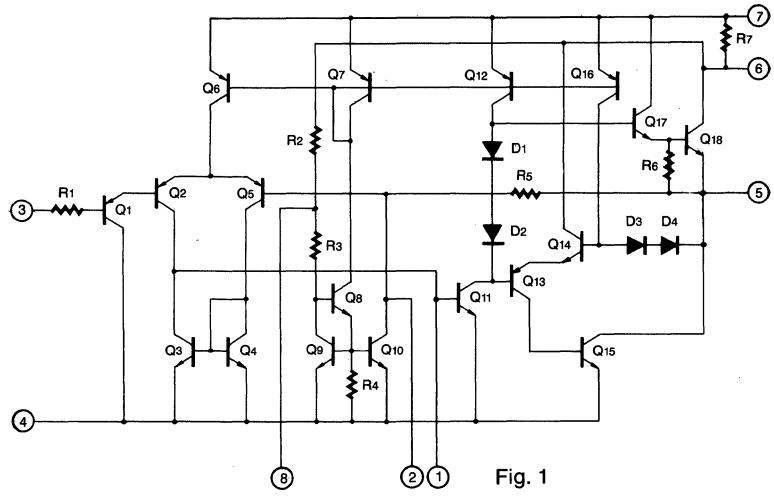


Fig. 1

TEST CIRCUIT

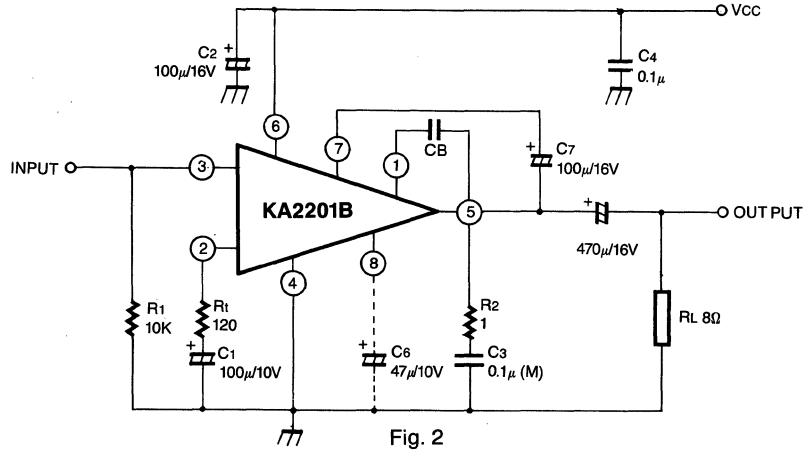


Fig. 2

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	V
Output Peak Current	I_O	1.5	A
Power Dissipation	Pd	650	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

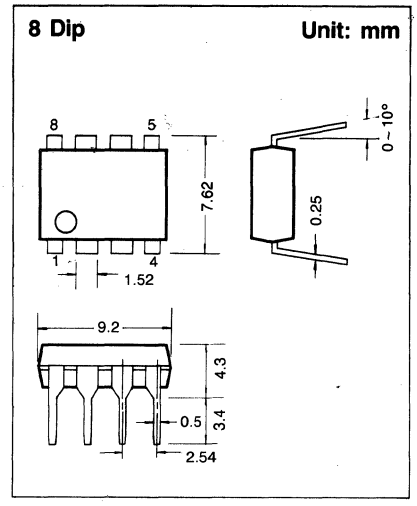
ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=6V, f=1KHz, Rg=600Ω, R_L=8Ω unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		3.5	7.0	mA
Output Power	P_O	THD=10%	0.4	0.5		W
Total Harmonic Distortion	THD	P_O=100mW		0.3	1.0	%
Voltage Gain (Open Loop)	A_{VO}	Rf=0		75		dB
Voltage Gain (Closed Loop)	A_V	Rf=120Ω	33	36	39	dB
Input Resistance	R_i			5		MΩ
Output Noise Voltage	V_{NO}	Rg=10KΩ BW (−3dB)=50Hz ~ 20KHz		0.3	1.0	mV

1.2W AUDIO POWER AMPLIFIER

The KA2201N is a monolithic integrated audio amplifier in 8 lead dual in the plastic package designed for audio frequency class B amplifier.



FEATURES

- **Wide operating supply voltage (3V ~ 16V)**
- **Medium output power**
  P_O =1.2W at V_{CC} =9V, R_L =8Ω, THD=10%
- **Low quiescent circuit current (I_{CC} =4mA: Typ)**
- **Good ripple rejection**
- **Minimum number of external parts required.**

SCHEMATIC DIAGRAM

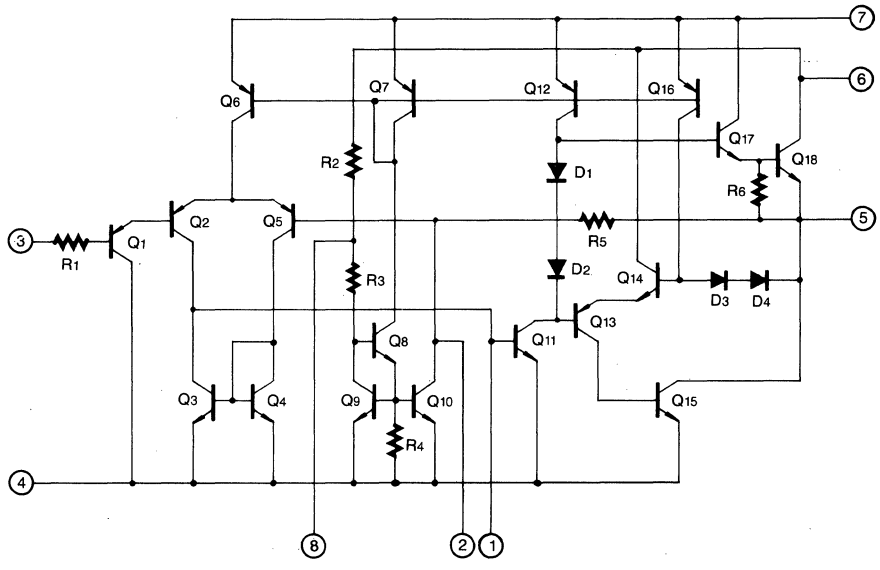


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Output Peak Current	I_O	1.5	A
Power Dissipation	P_d	1.25	W
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=9V, f=1KHz, R_g=600Ω, R_f=120Ω, R_L=8Ω unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		4	12	mA
Output Power	P_O	THD=10% V_{CC}=9V, R_L=4Ω V_{CC}=9V, R_L=8Ω V_{CC}=6V, R_L=4Ω V_{CC}=6V, R_L=8Ω V_{CC}=12V, R_L=8Ω	 0.9 0.4 	 1.6 1.2 0.75 0.5 2	 	 W W W W W
Total Harmonic Distortion	THD	P_O=500mW		0.3	1.0	%
Voltage Gain (Open Loop)	A_{VO}	R_f=0		75		dB
Voltage Gain (Closed Loop)	A_V	R_f=120Ω	33	36	39	dB
Input Resistance	R_i			5		MΩ
Output Noise Voltage	V_{NO}	R_g=10KΩ BW (−3dB)=50Hz ~ 20KHz		0.3	1.0	mV

TEST CIRCUIT

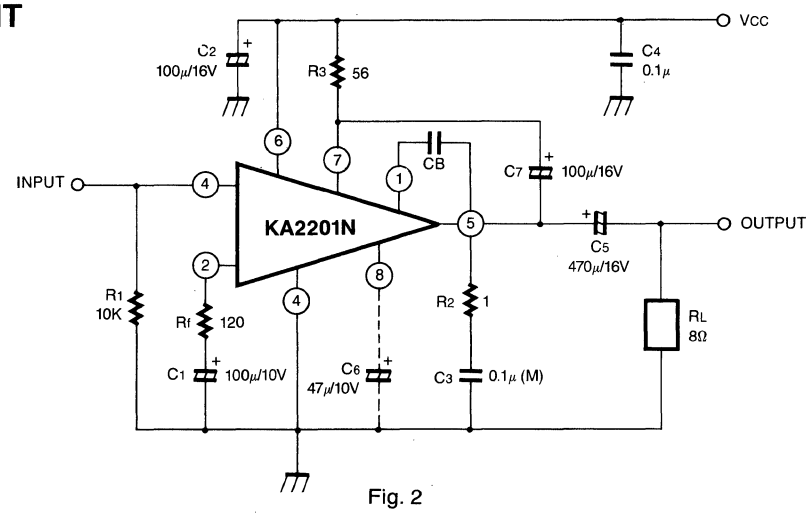
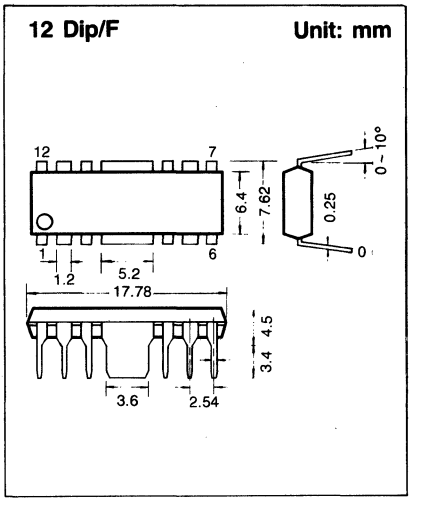


Fig. 2

2.3W DUAL AUDIO POWER AMPLIFIER

The KA2206 is a monolithic integrated circuit consisting of 2 channel power amplifier. It is suitable for stereo and bridge amplifier application of radio cassette tape recorder.



FEATURES

- **High output power**
  Stereo: P_O=2.3W (Typ) at V_{CC}=9V, R_L=4Ω.
  Bridge: P_O=4.7W (Typ) at V_{CC}=9V, R_L=8Ω.
- **Low switching distortion at high frequency.**
- **Small shock noise at the time of power on/off due to built-in muting circuit.**
- **Good ripple rejection due to built-in ripple filter.**
- **Good channel separation.**
- **Soft tone at the time of output saturation.**
- **Closed loop voltage gain fixed 45dB (Bridge: 51dB) but available with external resistor added.**
- **Minimum number of external parts required.**
- **Easy to design radiator fin.**

BLOCK DIAGRAM

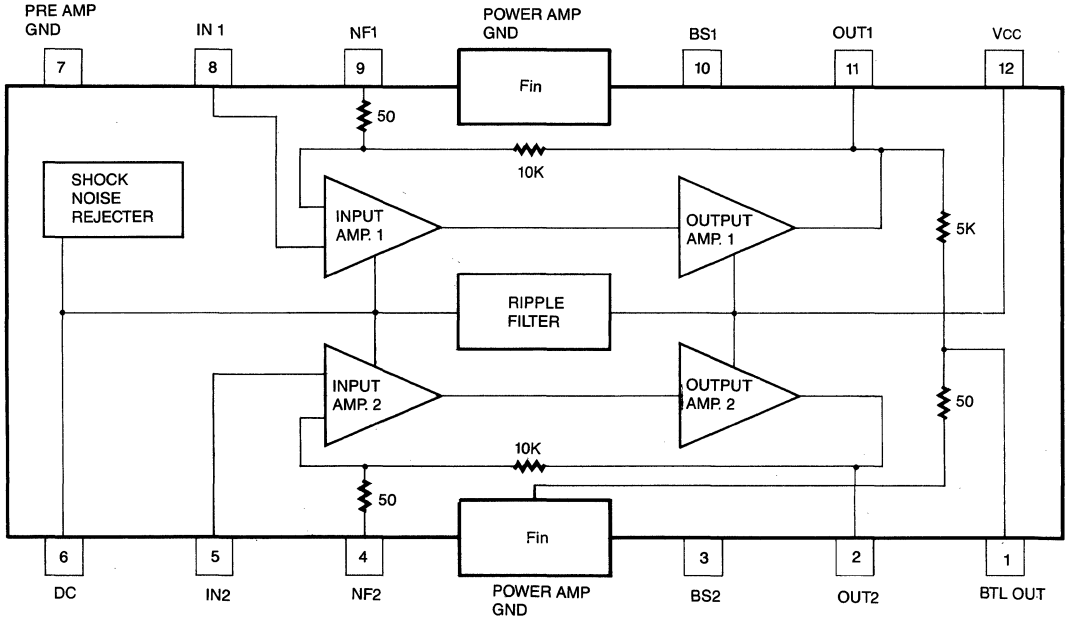


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Power Dissipation	P_d	4*	W
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

* Fin is soldering with PCB

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 9V, f=1KHz R_g =600Ω, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}				9	11	V
Quiescent Circuit Current	I_{CC}	V_i =0, Stereo			40	55	mA
Closed Loop Voltage Gain	A_V	Stereo	V_i = −45dBm	43	45	47	dB
		Bridge		49	51	53	dB
Channel Balance	CB	Stereo		−1	0	+1	dB
Output Power	P_O	Stereo	R_L =4Ω, THD=10%,	1.7	2.3		W
			R_L =8Ω, THD=10%		1.3		W
		Bridge	R_L =8Ω, THD=10%		4.7		W
Total Harmonic Distortion	THD	Stereo	P_O =250mW, R_L =4Ω		0.3	1.5	%
		Bridge			0.5		%
Input Resistance	R_i			21	30		KΩ
Ripple Rejection	RR	Stereo, R_g =0Ω, V_r = 150mV f=100Hz		40	46		dB
Output Noise Voltage	V_{NO}	Stereo, R_g =0Ω			0.3	1.0	mV
		Stereo, R_g =10KΩ			0.5	2.0	mV
Cross Talk	CT	Stereo, R_g =10KΩ, V_o =0dBm		40	55		dB

TYPICAL APPLICATION CIRCUIT: Stereo Amplifier

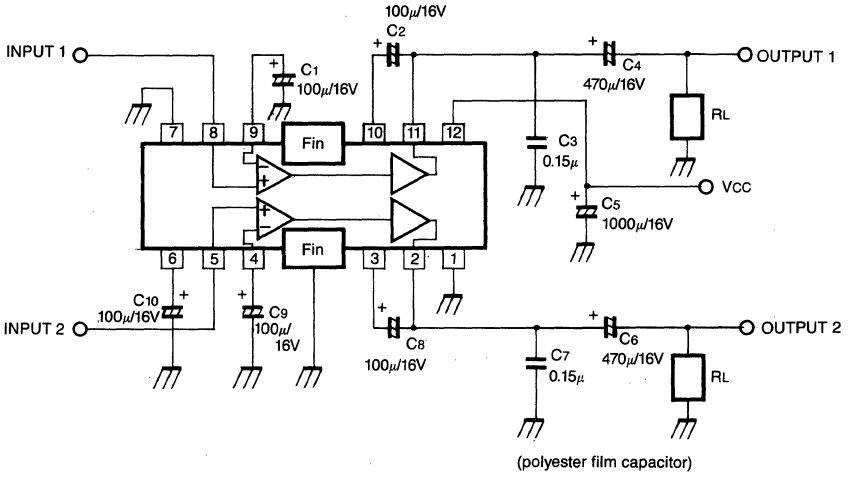


Fig. 2

TYPICAL APPLICATION CIRCUIT Bridge Amplifier

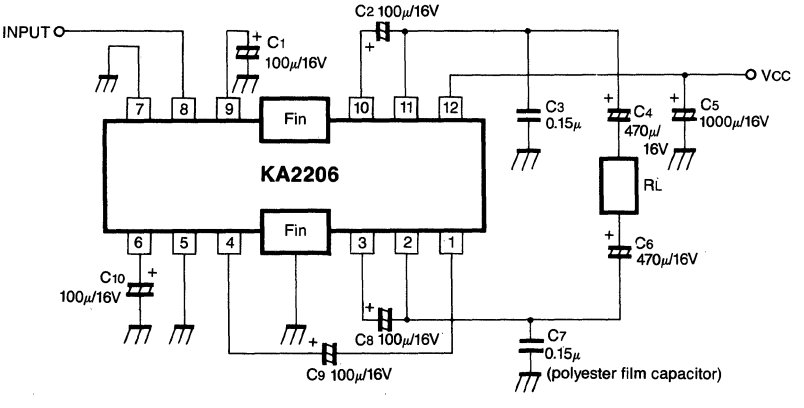
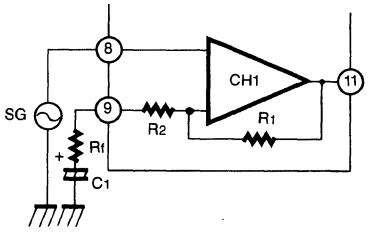


Fig. 3

VOLTAGE GAIN ADJUSTMENT

1. Stereo application



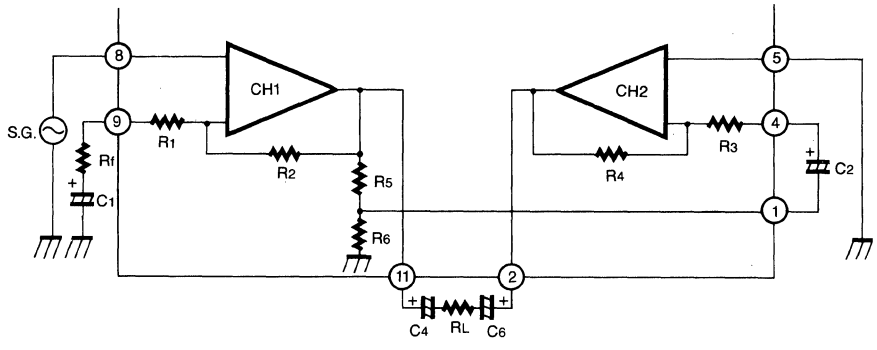
i) Fixed voltage gain
(Pin 9 connected GND directly)

$$Av = 20 \log \frac{R_1}{R_2} (dB)$$

ii) Variable voltage gain
(Rf and C_1 connected with pin 9)

$$Av = 20 \log \frac{R_1}{R_2 + R_f} (dB)$$

2. Bridge application



i) Fixed voltage gain (Pin 9 connected GND directly)

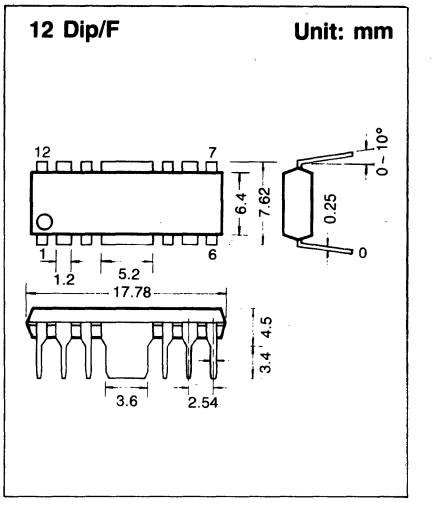
$$Av = 20 \log \frac{R_2}{R_1} + 6 (dB)$$

ii) Variable voltage gain (Rf and C_1 connected with pin 9)

$$Av = 20 \log \frac{R_2}{R_1 + R_f} + 6 (dB)$$

2.3W DUAL AUDIO POWER AMPLIFIER

The KA22061 is a monolithic integrated circuit consisting of 2 channel, power amplifier. It is suitable for stereo and bridge amplifier application of radio cassette tape recorder.



FEATURES

- **High output power**
  Stereo: P_O=2.3W (Typ) at V_{CC}=9V, R_L=4Ω.
  Bridge: P_O=4.7W (Typ) at V_{CC}=9V, R_L=8Ω.
- **Low switching distortion at high frequency.**
- **Small shock noise at the time of power on/off due to built-in muting circuit.**
- **Good ripple rejection due to built-in ripple filter.**
- **Good channel separation.**
- **Soft tone at the time of output saturation.**
- **Closed loop voltage gain fixed 45dB (Bridge: 51dB) but available with external resistor added.**
- **Minimum number of external parts required.**
- **Easy to design radiator fin.**

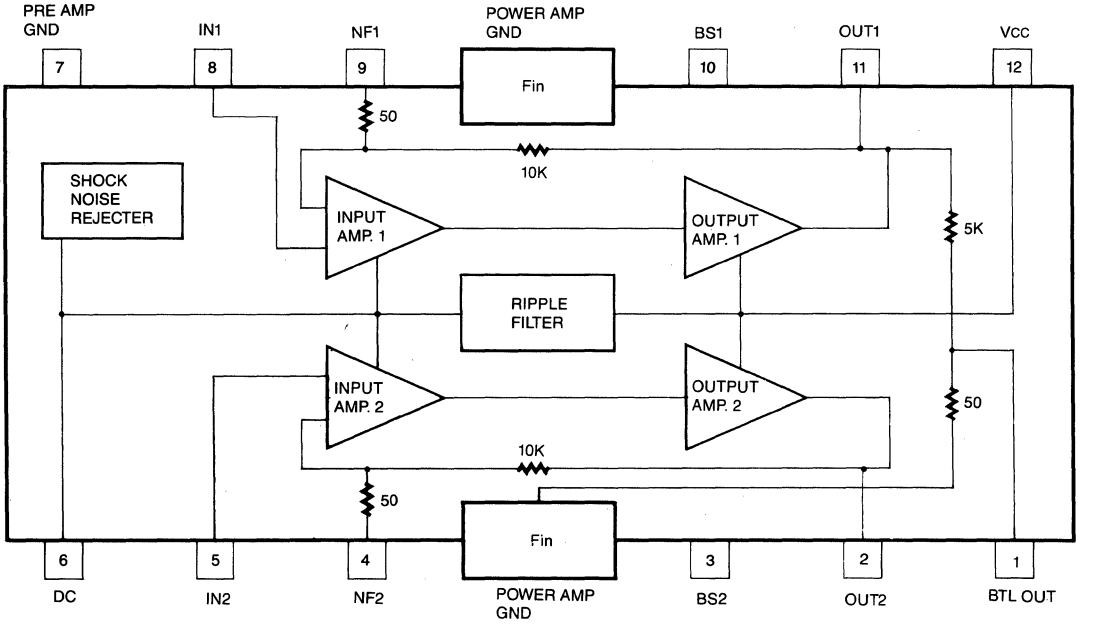


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Power Dissipation	Pd	4*	W
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

* Fin is soldering with PCB

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=9V, f=1KHz, Rg=600Ω, unless otherwise specified)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}				9	11	V
Quiescent Circuit Current	I_{CC}	V_i=0, Stereo			40	55	mA
Closed Loop Voltage Gain	A_V	Stereo	V_i=−45dBm	43	45	47	dB
		Bridge		49	51	53	dB
Channel Balance	CB	Stereo		−1	0	+1	dB
Output Power	P_O	Stereo	R_L=4Ω, THD=10%	1.7	2.3		W
			R_L=8Ω, THD=10%		1.3		W
		Bridge	R_L=8Ω, THD=10%		4.7		W
Total Harmonic Distortion	THD	Stereo	P_O=250mW, R_L=4Ω		0.3	1.5	%
		Bridge			0.5		%
Input Resistance	R_i			21	30		KΩ
Ripple Rejection	RR	Stereo, R_g=0Ω, V_r=150mV f=100Hz		40	46		dB
Output Noise Voltage	V_{NO}	Stereo, R_g=0Ω			0.3	1.0	mV
		Stereo, R_g=10KΩ			0.5	2.0	mV
Cross Talk	CT	Stereo, R_g=10KΩ, V_O=0dBm		40	55		dB

TYPICAL APPLICATION CIRCUIT: Stereo Amplifier

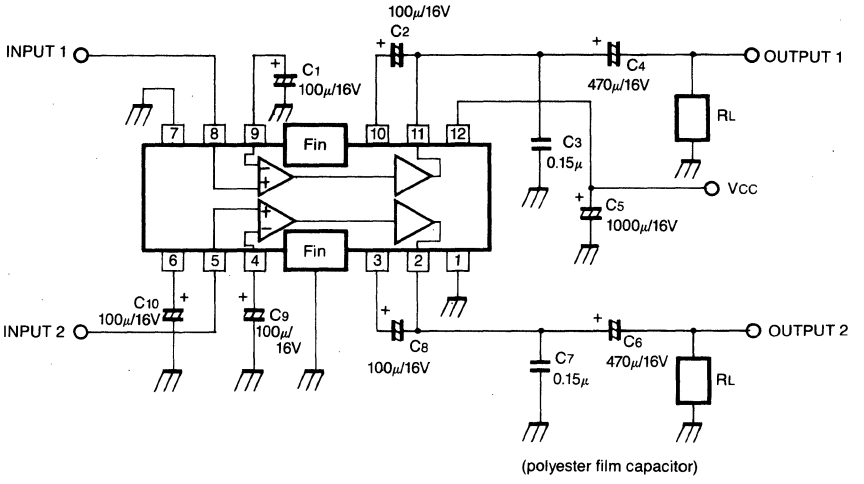


Fig. 2

TYPICAL APPLICATION CIRCUIT Bridge Amplifier

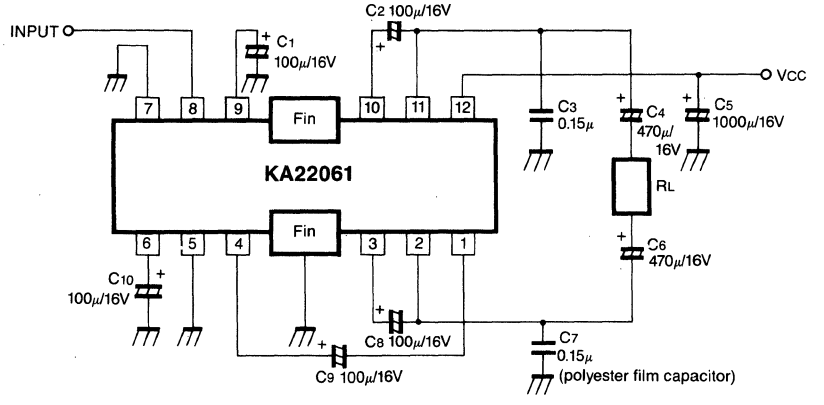
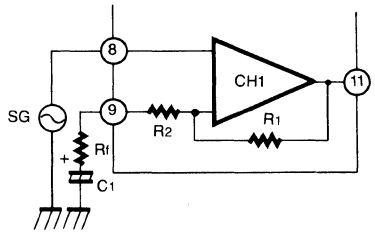


Fig. 3

VOLTAGE GAIN ADJUSTMENT

1. Stereo application



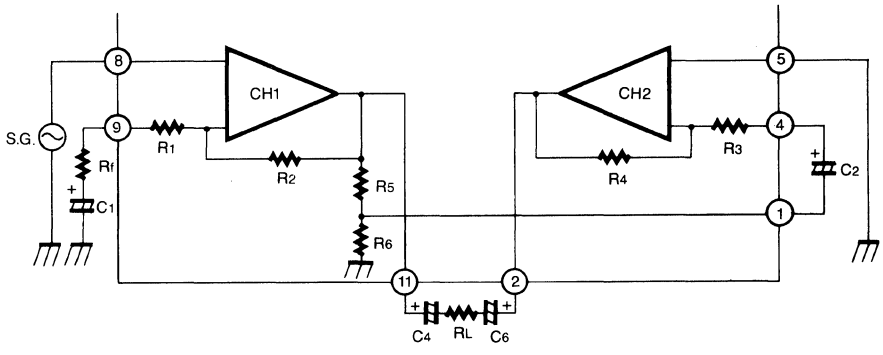
i) Fixed voltage gain
(Pin 9 connected GND directly)

$$Av = 20 \log \frac{R_1}{R_2} (dB)$$

ii) Variable voltage gain
(Rf and C_1 connected with pin 9)

$$Av = 20 \log \frac{R_1}{R_2 + Rf} (dB)$$

2. Bridge application



i) Fixed voltage gain (Pin 9 connected GND directly)

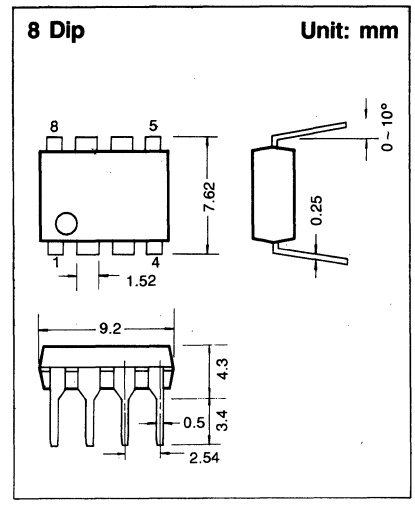
$$A_V = 20 \log \frac{R_2}{R_1} + 6 (dB)$$

ii) Variable voltage gain (Rf and C_1 connected with Pin 9)

$$A_V = 20 \log \frac{R_2}{R_1 + R_f} + 6 (dB)$$

DUAL LOW VOLTAGE POWER AMPLIFIER

The KA2209 is a monolithic integrated audio amplifier in 8 lead dual in the plastic package. It is designed for portable cassette players and radios.



FEATURES

- **Wide operating supply voltage: V_{CC}=1.8V~9V**
- **Low crossover distortion**
- **Low quiescent circuit current**
- **Bridge/stereo configuration**

BLOCK DIAGRAM

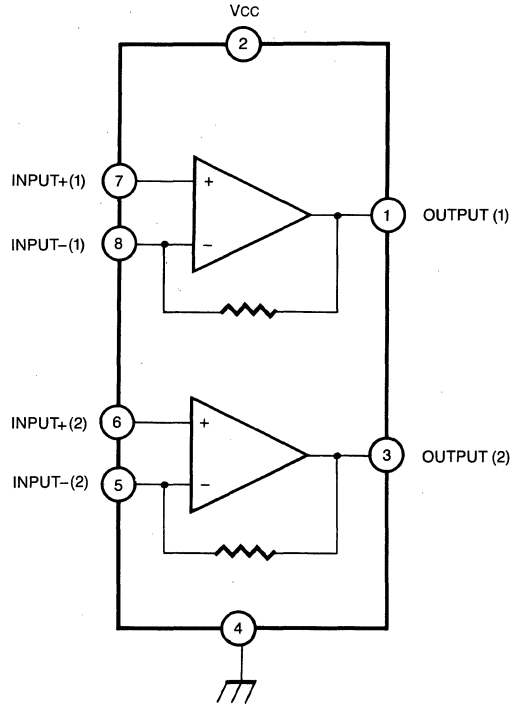


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Output Peak Current	I_O	1	V
Power Dissipation	P_d	1.4	W
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=6V, f=1KHz unless otherwise specified)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}			1.8		15	V
Quiescent Circuit Current	I_{CC}	V_i=0			9		mA
Closed Loop Voltage Gain	A_V	Stereo			44		dB
		Bridge			44		dB
Channel Balance	CB	Stereo		−1	0	1	dB
Output Power	P_O	Stereo	V_{CC}=6V, R_L=4Ω, THD=10%	0.4	0.65		W
			V_{CC}=3V, R_L=4Ω, THD=10%		0.11		W
		Bridge	V_{CC}=6V, R_L=8Ω, THD=10%	0.9	1.35		W
			V_{CC}=3V, R_L=4Ω, THD=10%		0.35		W
Total Harmonic Distortion	THD	Stereo, R_L=8Ω, P_O=0.2W			0.5		%
		Bridge, R_L=8Ω, P_o=0.5W			0.5		%
Ripple Rejection	RR	Stereo, f=100Hz, C_3=100μF		24	30		dB
Output Noise Voltage	V_{NO}	Stereo, 20Hz ~ 20KHz			0.5	2.0	mV
Cross Talk	CT	Stereo, f=1KHz			50		dB
Input Resistance	R_i			100			KΩ

TEST CIRCUIT 1: STEREO

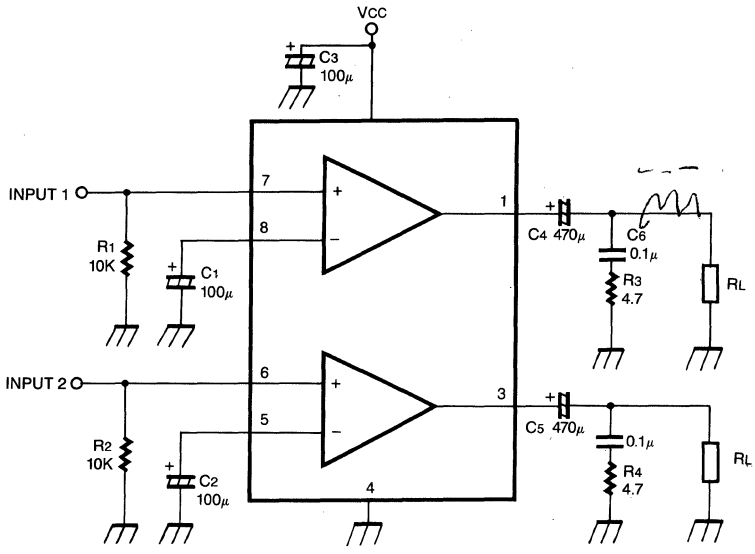


Fig. 2

TEST CIRCUIT 2: BRIDGE

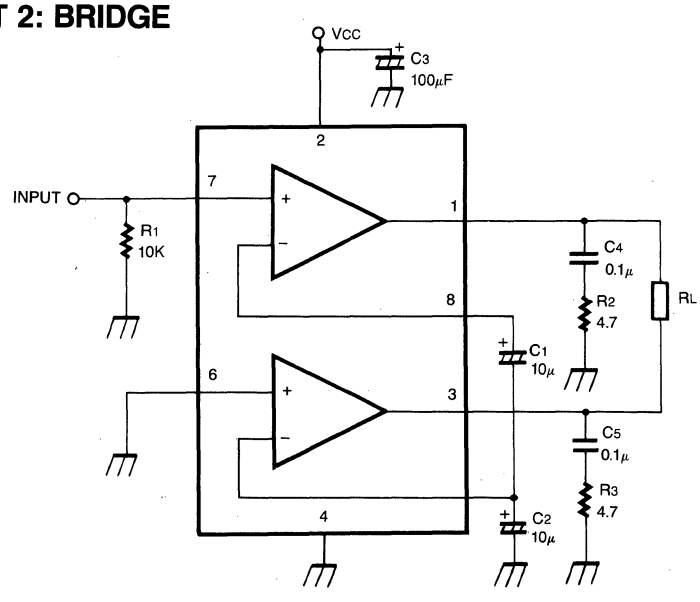
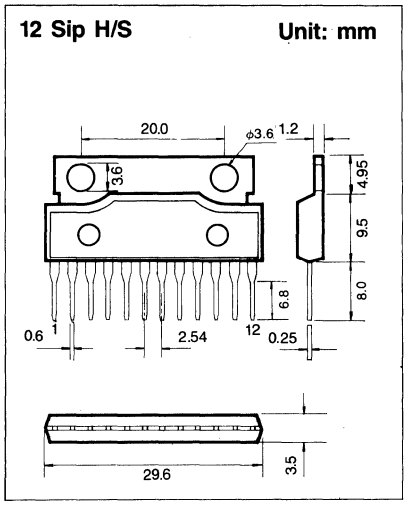


Fig. 3

5.5W DUAL POWER AMPLIFIER

The KA2210 is a monolithic integrated circuit consisting of 2 channel power amplifier. It is suitable for stereo and bridge amplifier application of car stereo.



FEATURES

- **2 channel amplifier: 5.5W×2 (typ).**
- **Minimum number of external parts required.**
- **Small shock noise at the time of power on/off and good starting balance.**
- **High ripple rejection ratio: 46dB (typ).**
- **Good channel separation.**
- **Small residual noise. (Rg=0)**
- **Included various kinds of protectors.**
- **Thermal protector.**
- **Surge and over-voltage protector.**
- **V_{CC} and output short protector.**

BLOCK DIAGRAM

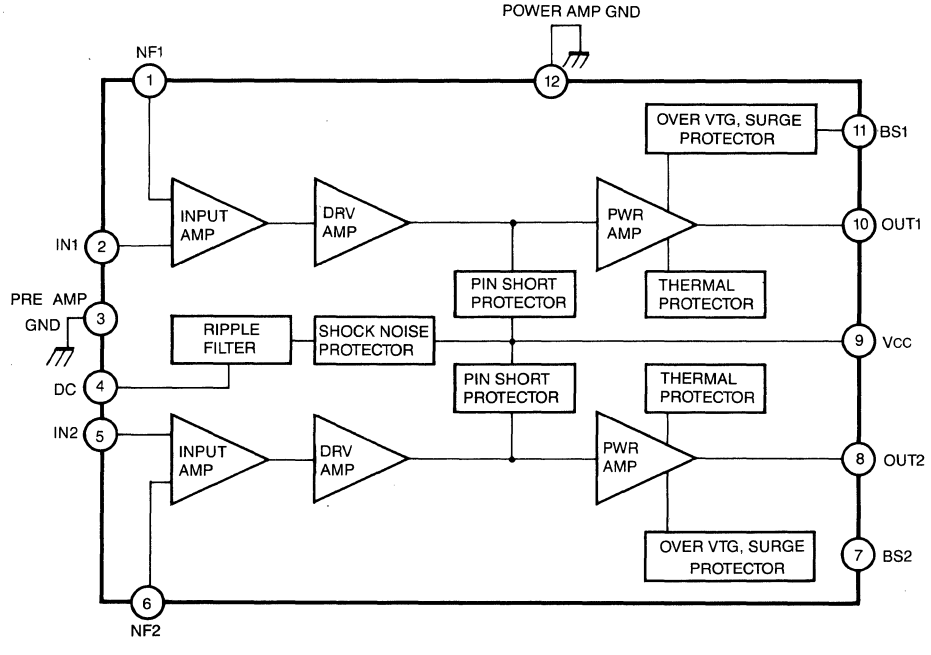


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Maximum Supply Voltage (Quiescent)	V_{CC} max 1	25	V
Maximum Supply Voltage (with Signal)	V_{CC} max 2	18	V
Surge Voltage ($t \leqq 0.2$ sec)	V_{CC} (Surge)	50	V
Maximum Output Current (1 Channel)	I_O peak	3.5	A
Power Dissipation	P_d max	15	W
Operating Temperature	Topr	−20 ~ +75	°C
Storage Temperature	Tstg	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =13.2V, R_L =4Ω, f=1KHz R_g =600Ω, 100×100×1.5mm³ Al H/S)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}		10	13.2	16	V
Quiescent Circuit Current	I_{CC}	V_i =0, Stereo		75	150	mA
Output Power	P_O	THD=10%	5.0	5.5		W
Voltage Gain	A_V		49.5	51.5	53.5	dB
Total Harmonic Distortion	THD	P_O =1W		0.15	1.0	%
Input Resistance	R_i			30		KΩ
Output Noise Voltage	V_{NO}	R_g =0		0.6	1.0	mV
		R_g =10KΩ		1.0	2.0	mV
Ripple Rejection Ratio	RR	R_g =0, V_r =200mV, f_r =100Hz		46		dB
Channel Separation	Sep	R_g =10KΩ, V_o =0 dBm	45	55		dB

TYPICAL APPLICATION CIRCUIT: STEREO

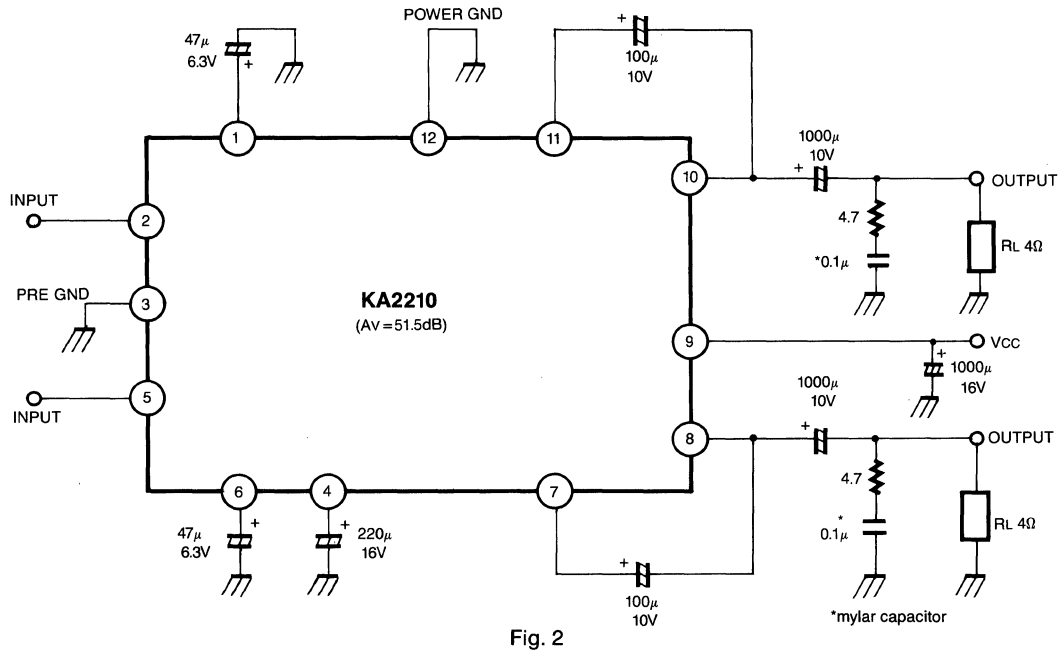


Fig. 2

APPLICATION CIRCUIT: BRIDGE

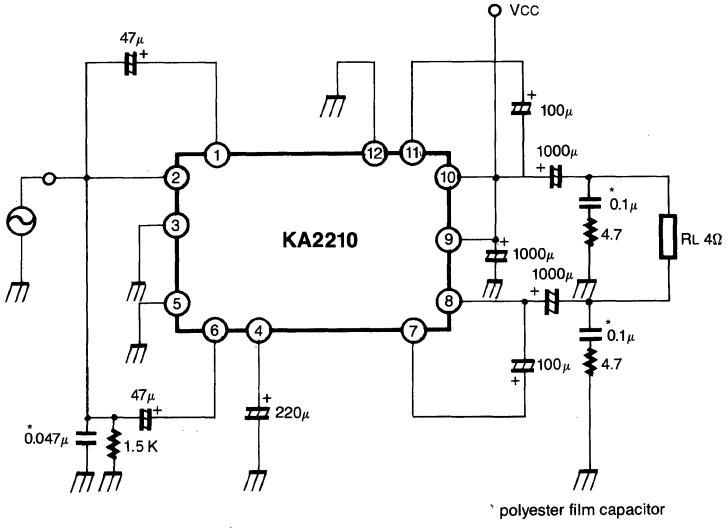
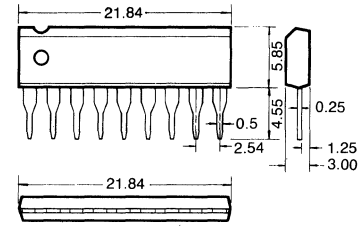


Fig. 3

0.5W AUDIO POWER AMPLIFIER

The KA2212 is a monolithic integrated audio power amplifier in 9 lead single in line plastic package, designed for audio frequency class B amplifier.

9 Sip Unit: mm



FEATURES

- **Suitable for portable radio, cassette tape recorder.**
- **Medium output power.**
  P_O=0.5W (Typ) at V_{CC}=6V, R_L=8Ω, THD=10%.
- **Wide operating supply voltage range (3.5V~14V).**
- **Low quiescent circuit current.**
- **Excellent thermal stability.**

SCHEMATIC DIAGRAM

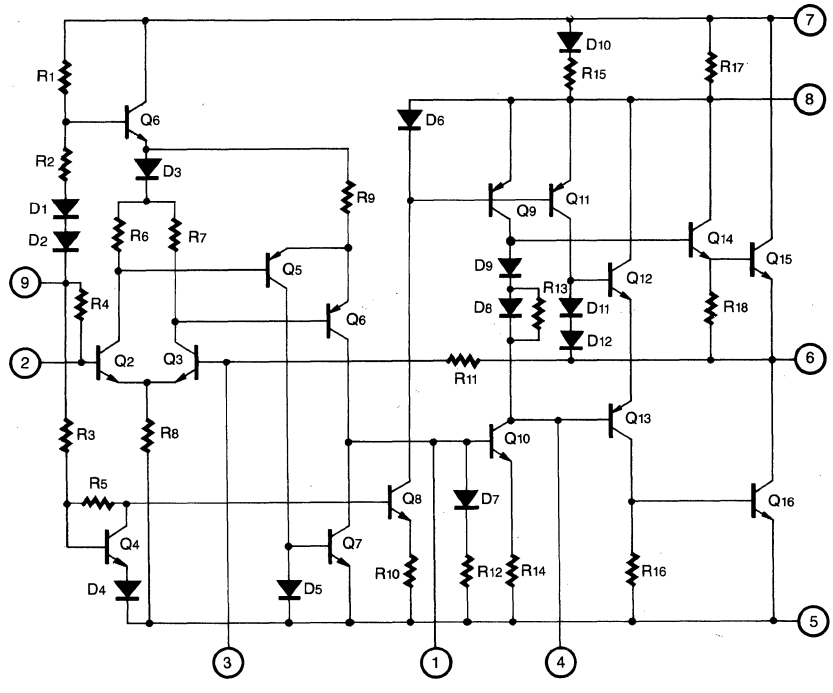


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	V
Power Dissipation	P_d	750	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 6V, R_L = 8Ω, R_g = 600Ω, Rf = 68Ω, f = 1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		14		mA
Voltage Gain (Open Loop)	A_{VO}	Rf=0Ω	60	75		dB
Voltage Gain (Closed Loop)	A_V	Rf=68Ω	47	50	52	dB
Output Power	P_O	THD=10%	0.45	0.5		W
Total Harmonic Distortion	THD	P_O=100mW		0.3	1.0	%
Input Resistance	R_i			15		KΩ
Output Noise Voltage	V_{NO}	Rg=10KΩ BW (−3dB)=50Hz ~ 20KHz		0.4	1.0	mV

TEST CIRCUIT

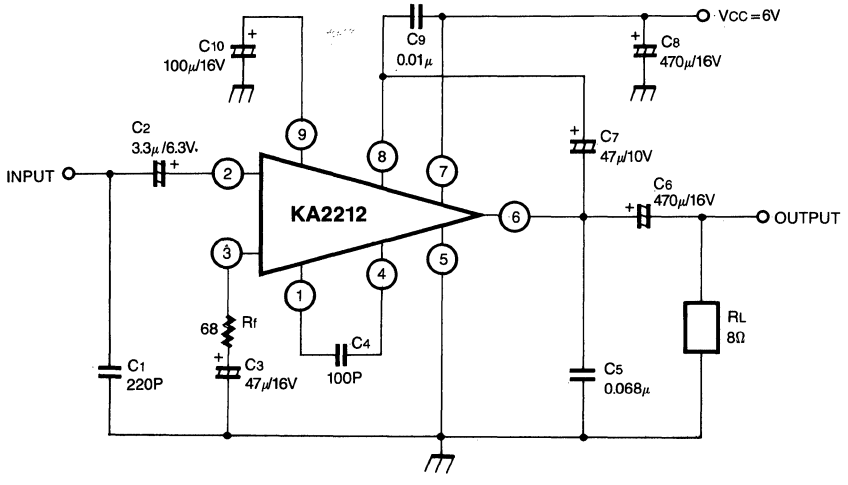
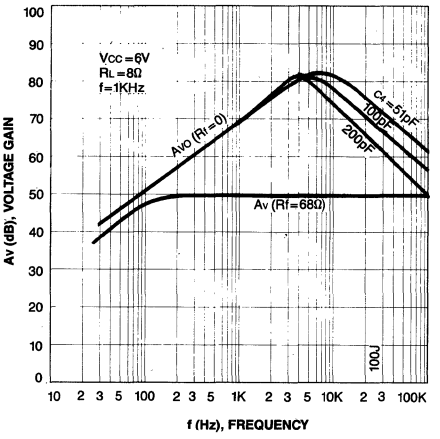
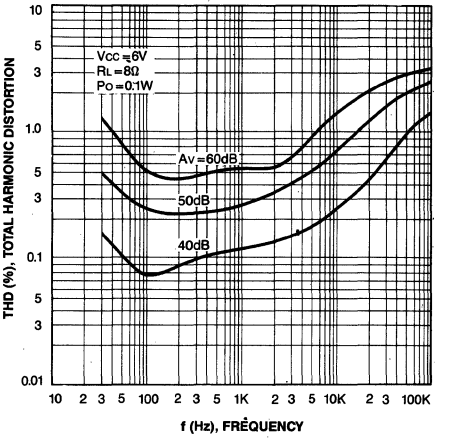


Fig. 2

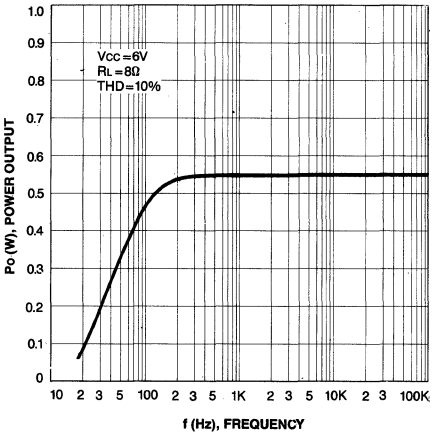
VOLTAGE GAIN-FREQUENCY



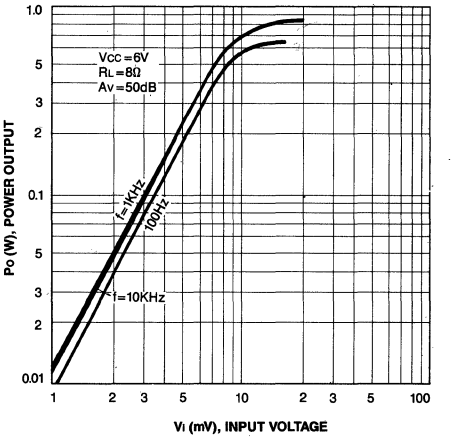
TOTAL HARMONIC DISTORTION-FREQUENCY



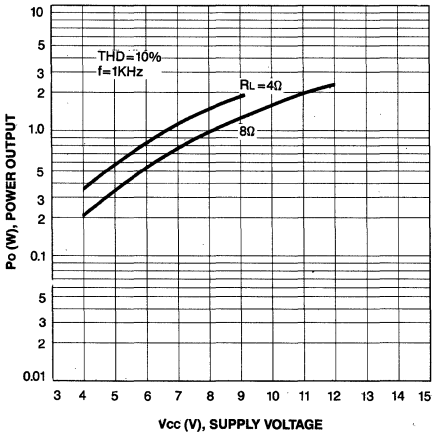
POWER OUTPUT-FREQUENCY



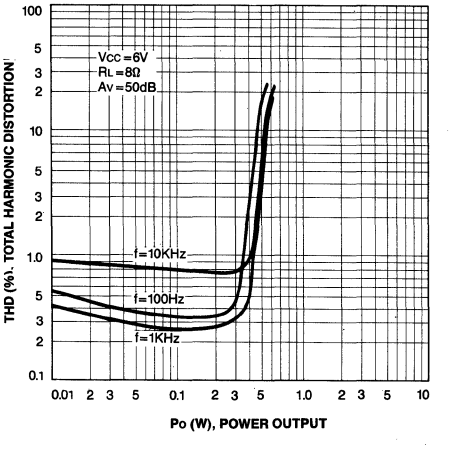
POWER OUTPUT-INPUT VOLTAGE



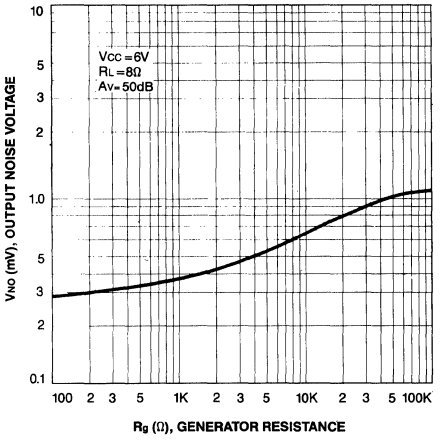
POWER OUTPUT-SUPPLY VOLTAGE



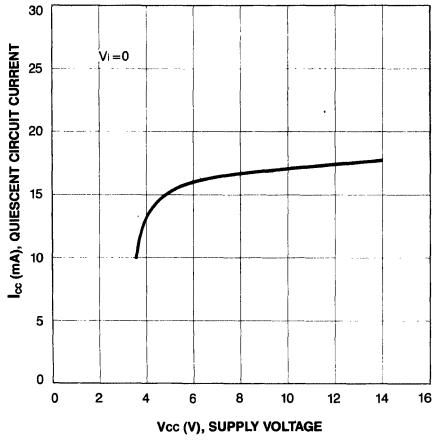
TOTAL HARMONIC DISTORTION-POWER OUTPUT



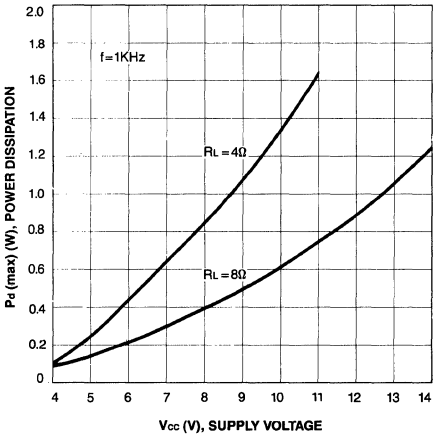
OUTPUT NOISE VOLTAGE-GENERATOR RESISTANCE



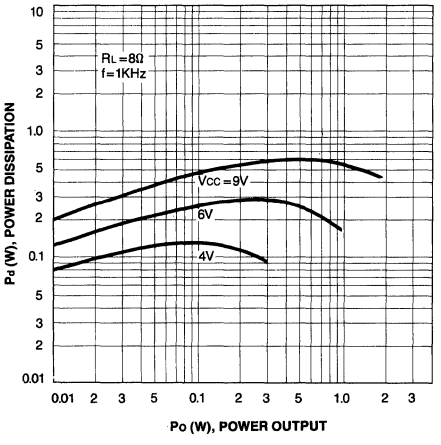
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



POWER DISSIPATION-SUPPLY VOLTAGE



POWER DISSIPATION-POWER OUTPUT



External Components (Refer to test circuit)

C_1: Noise filter

C_2: Input coupling capacitor
The recommended value for this capacitor is 3.3μF.
If made too small, low frequency characteristic is a change for the worse. Too large a capacitance value will in crease rise time when power is applied and may generate noise due to the charging current when the volume control is adjusted.

R_f, C_3: Feedback components
The variation of closed loop gain is depending on this component which are determined as follows.

$$C_3 = \frac{1}{2\pi f_L \cdot R_f} \qquad R_f = \frac{20K}{A_v}(dB)$$

Where f_L: low cut-off frequency
A_v: closed loop gain

C_4: Compensation capacitor
The high cut-off frequency is determined by C_4, which contributes to suppress the oscillation at the higher frequency range.

C_5, C_9: Oscillation supression
The mylar capacitor is be used for C_5 to get a better characteristic for temperature and the frequency.

C_6: Output coupling capacitor
It decides output power level of low frequency.

C_7: Bootstrap capacitor
In case of low value reduced rated output power and increased distortion at low frequency.

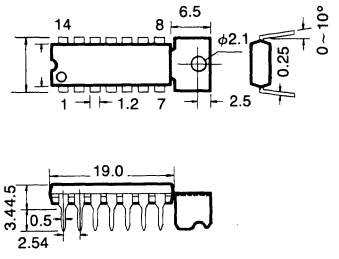
C_8: Ripple filter for power supply
The large value is required to get an excellent ripple characteristic under the line operation but the small one can be used with the battery.

C_{10}: Filter capacitor
Rejects power line hum.

ONE CHIP TAPE RECORDER SYSTEM

The KA2213 is a monolithic integrated circuit consisting of preamplifier, ALC circuit, power amplifier in 14 dual in line package with heat sink.

14 Dip H/S Unit: mm



FEATURES

- **Suitable for play and recording mono cassette tape recorder.**
- **Wide operating supply voltage range (4V ~ 12V).**
- **High gain preamplifier and power amplifier.**
- **Output power of power amplifier state P_O =1W at V_{CC} =6V, R_L =4Ω, THD= 10%.**
- **Soft tone quality at the time of output saturation.**
- **Wide ALC range and small variation in output voltage.**
- **Small shock noise at the time of power on/off due to built-in preventive circuit.**
- **Variable monitor capability due to recording amplifier consisting of preamplifier alone.**
- **Minimum number of external parts required.**

BLOCK DIAGRAM

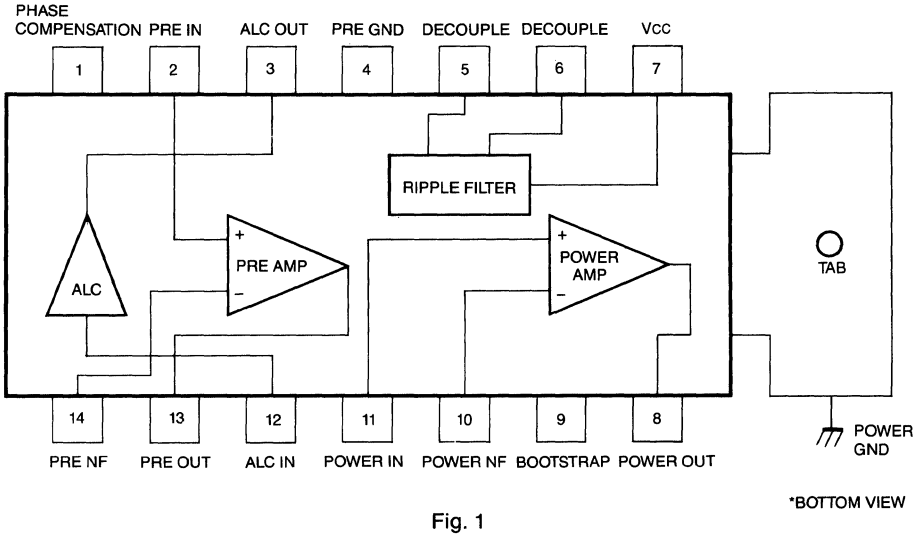


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	13	V
Power Dissipation	P_d	1.2	W
		2.25*	W
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

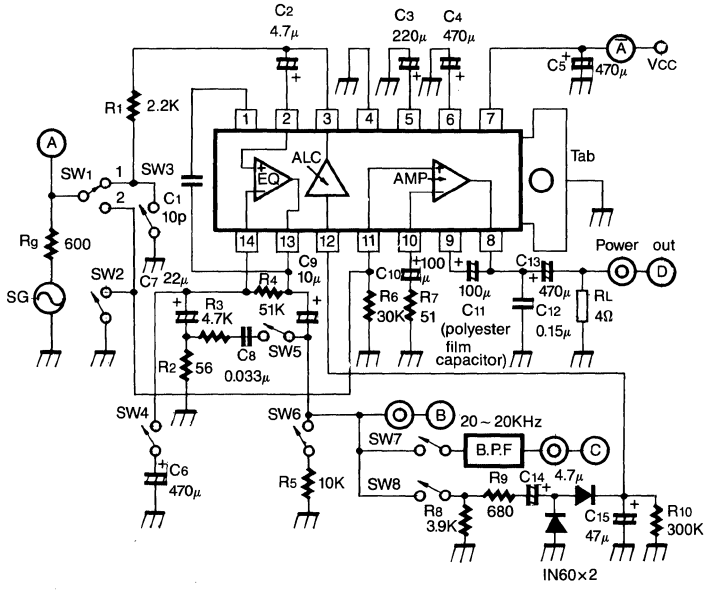
* Mounted and soldered on a 50mm x 50mm copper foil of PCB

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 6V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_{CC} = 6V, V_i = 0		18	30	mA
		V_{CC} = 9V, V_i = 0		23	40	mA
Preamplifier						
Voltage Gain (Open Loop)	A_{VO}	Open loop		85		dB
Voltage Gain (Closed Loop)	A_V	Closed loop, Play		40		dB
Output Voltage	V_O	THD=1%, Play	0.9	1.2		V
Input Resistance	R_i		21	30		KΩ
Equivalent Input Noise Voltage	V_{NI}	Play		1.0	2.0	μV
ALC Input Level	ALC	THD=1%, Play	−20	−12		dBm
Power Amplifier						
Voltage Gain (Closed Loop)	A_V	R_f = 51Ω	43	45	47	dB
Output Power	P_O	V_{CC} = 6V, R_L = 4Ω, THD=10%	0.7	1.0		W
		V_{CC} = 7.5V, R_L = 4Ω, THD=10%	1.0	1.5		W
		V_{CC} = 9V, R_L = 4Ω, THD=10%	1.7	2.2		W
Total Harmonic Distortion	THD	P_O = 250mW		0.3	1.5	%
Input Resistance	R_i			30		KΩ
Output Noise Voltage	V_{NO}	R_g = 10KΩ		0.6	1.8	mV
Ripple Rejection	RR	R_g = 0Ω, V_r = 150mV, f=100Hz	40	45		dB

TEST CIRCUIT



TEST CIRCUIT

Characteristic		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Test Point	Test Method
Power Amplifier	I_{CC}		on	on	off	on	on	off	off		Test circuit current
	A_V	2	off	off	off	on	on	off	off	A.D	$A_V = 20 \log V_O/V_i$ (dB)
	P_O	2	off	off	off	on	on	off	off	D	Test output voltage at THD = 10%
	THD	2	off	off	off	on	on	off	off	D	Test THD at output voltage V_O = 1V
	V_{NO}		on	off	off	on	on	off	off	D	Test output noise voltage
	RR		on	off	off	on	on	off	off	D	RR = 20 log V_{ro}/150 (dB) Test output ripple voltage (V_{ro})
Pre-Amplifier	A_{VO}	1	off	off	on	off	on	off	off	A.B	$A_{VO} = 20 \log V_O/V_i$ (dB)
	V_O	1	off	off	off	on	on	off	off	B	Test output voltage at THD = 1%
	V_{NI}		off	on	off	on	on	on	off	C	Convert output noise voltage at R_g = 2.2KΩ, $V_{NI} = V_{NO}/A_V$
	ALC Input level	1	off	off	off	off	off	off	on	A.B	Test input voltage at THD = 1%

TYPICAL APPLICATION CIRCUIT

1. Mono cassette tape recorder

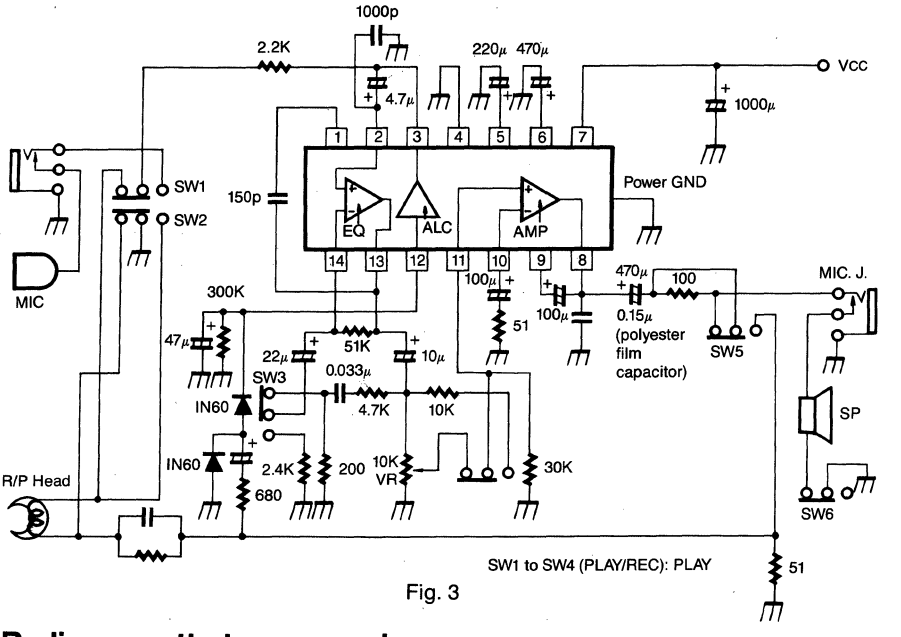


Fig. 3

2. Radio cassette tape recorder

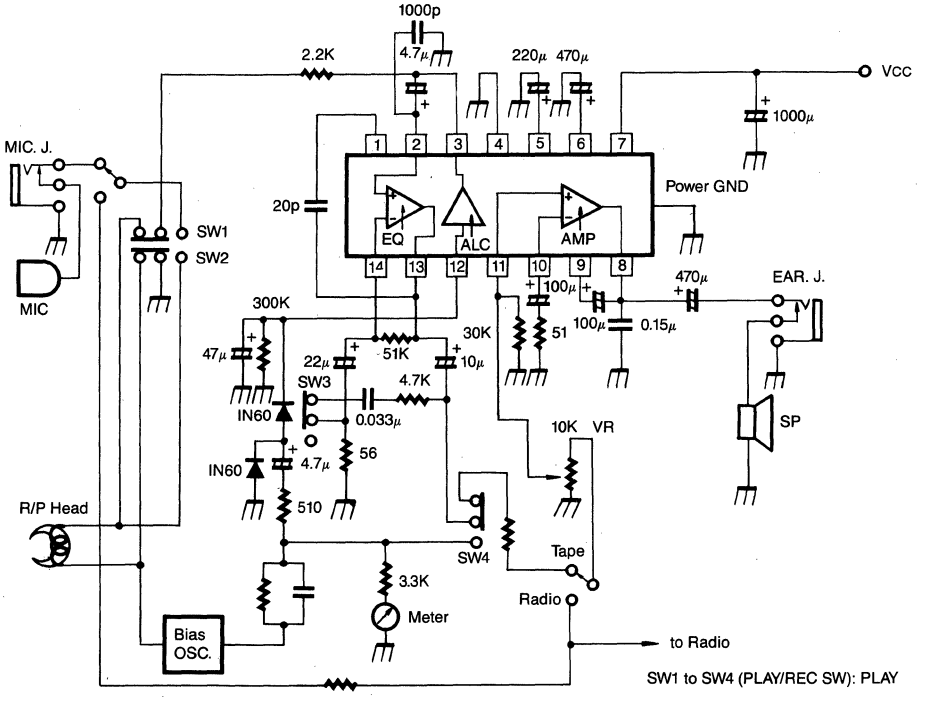


Fig. 4

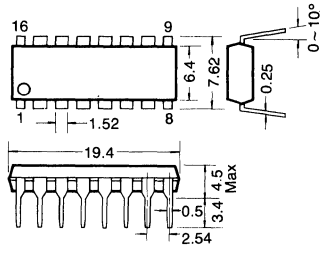
ONE CHIP TAPE RECORDER SYSTEM

The KA2213D is a monolithic intergrated circuit consisting of preamplifier, ALC circuit, power amplifier in 16 dual in line package.

FEATURES

- **Suitable for play and recording mono cassette tape recorder.**
- **Operating supply voltage range (4V ~ 9V).**
- **High gain pre-amplifier and power amplifier.**
- **Output power of power amplifier**
  P_O =0.8W (typ) at V_{CC} =6V, R_L = 8 Ω, THD= 10%.
- **Soft tone quality at the time of output saturation.**
- **Wide ALC range and small variation in output voltage.**
- **Small shock noise at the time of power switch on/off due to built-in preventive circuit.**
- **Variable monitor capability due to recording amplifier consisting of preamplifier alone.**
- **Minimum number of external parts required.**

16 Dip **Unit: mm**



BLOCK DIAGRAM

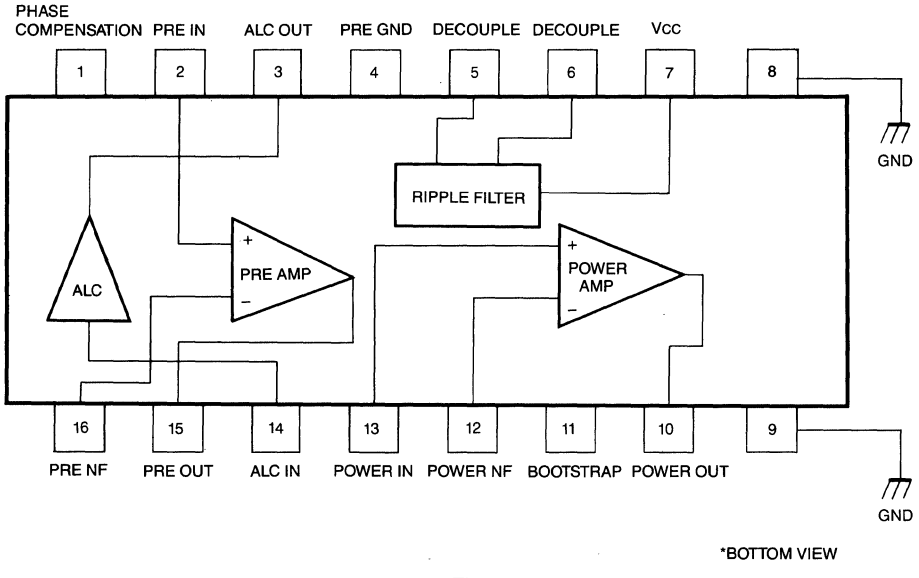


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Power Dissipation	P_d	900	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=6V, f=1KHz unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_{CC}=6V, V_i=0		18	30	mA
Preamplifier						
Voltage Gain (Open loop)	A_{VO}	Open Loop		85		dB
Voltage Gain (Closed Loop)	A_V	Closed Loop, Play		40		dB
Output Voltage	V_O	THD=1%, Play	0.9	1.2		V
Input Resistance	R_i		21	30		KΩ
Equivalent Input Noise Voltage	V_{NI}	Play		1.0	2.0	μV
ALC Input Level	ALC	THD=1%, Play	−20	−12		dBm
Power Amplifier						
Voltage Gain (Closed Loop)	A_V	R_f=51Ω	43	45	47	dB
Output Power	P_O	V_{CC}=6V, R_L=8Ω, THD=10%	0.4	0.5		W
Total Harmonic Distortion	THD	P_O=250mW		0.3	1.5	%
Input Resistance	R_i			30		KΩ
Output Noise Voltage	V_{NO}	R_g=10KΩ		0.6	1.8	mV
Ripple Rejection	RR	R_g=0, V_r=150mV, f=100Hz	40	45		dB

TEST CIRCUIT

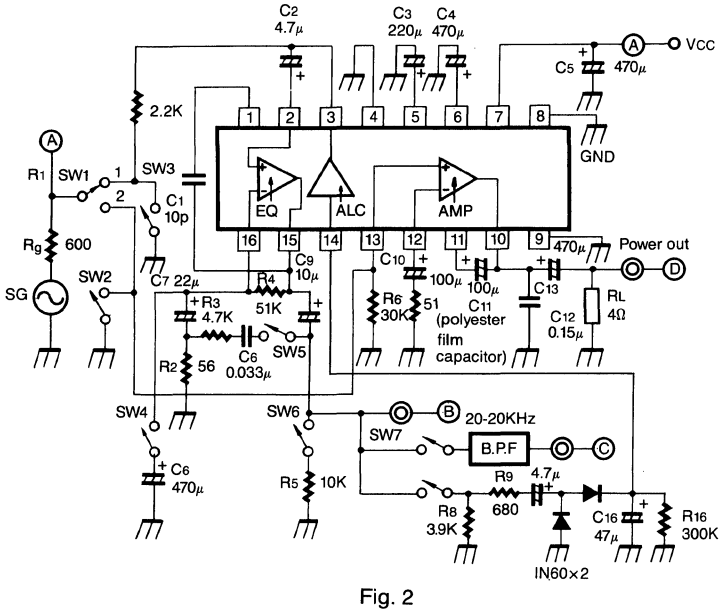


Fig. 2

TEST METHOD

Characteristic		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Test point	Test Method
Power Amplifier	I_{CC}		on	on	off	on	on	off	off		Test circuit current
	A_V	2	off	off	off	on	on	off	off	A.D	$A_V = 20 \log V_O/V_i$ (dB)
	P_O	2	off	off	off	on	on	off	off	D	Test output voltage at THD=10%
	THD	2	off	off	off	on	on	off	off	D	Test THD at output voltage $V_O = 1V$
	V_{NO}		on	off	off	on	on	off	off	D	Test output noise voltage
	RR		on	off	off	on	on	off	off	D	RR=20 log V_{ro}/150 (dB) Test output ripple voltage (V_{ro})
Pre-Amplifier	A_{VO}	1	off	off	on	off	on	off	off	A, B	$A_{VO} = 20 \log V_O/V_i$ (dB)
	V_O	1	off	off	off	on	on	off	off	B	Test output voltage at THD=1%
	V_{NI}		off	on	off	on	on	on	off	C	Convert output noise voltage at $R_g = 2.2K\Omega$, $V_{NI} = V_{NO}/A_V$
	ALC Input Level	1	off	off	off	off	off	off	on	A, B	Test input voltage at THD=1%

APPLICATION CIRCUIT 1: Straight Cassette

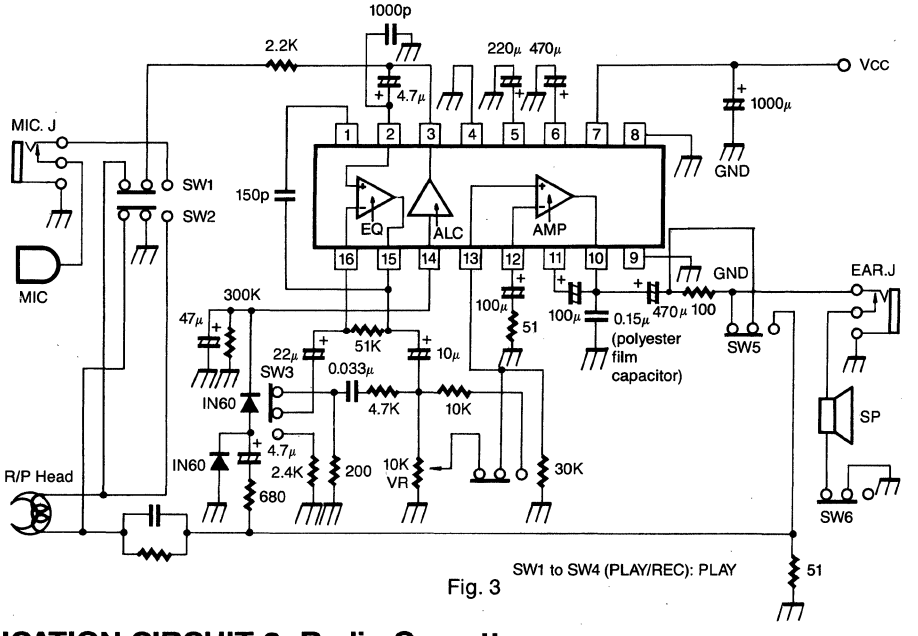


Fig. 3

APPLICATION CIRCUIT 2: Radio Cassette

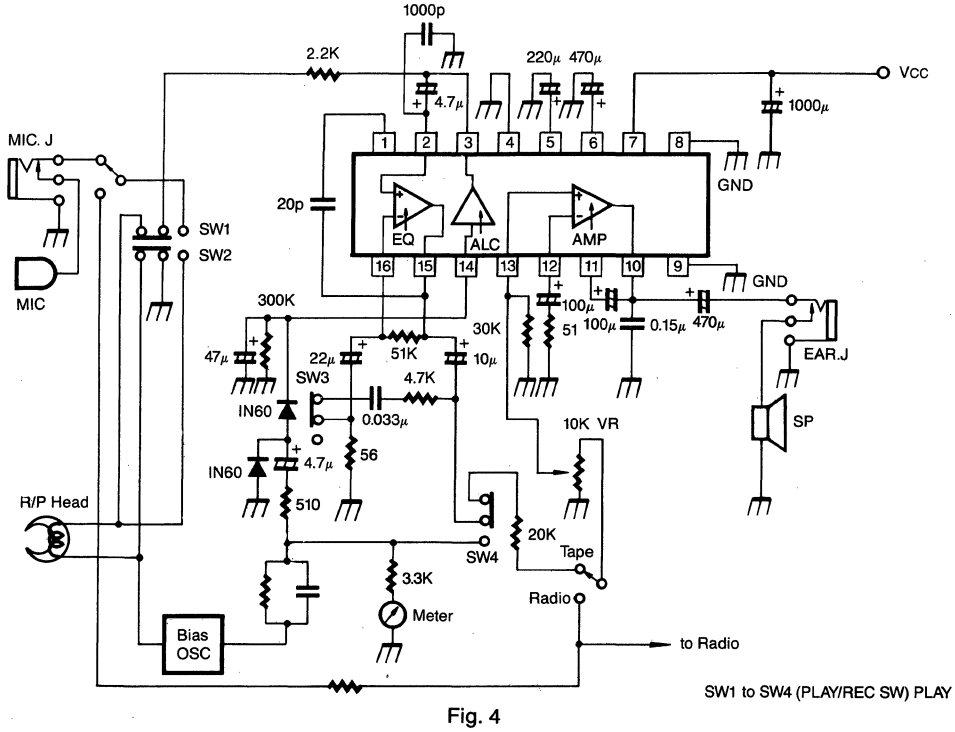
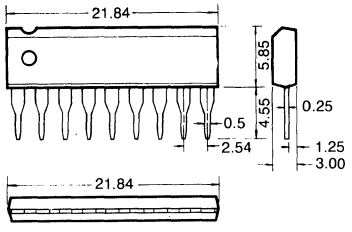


Fig. 4

EQUALIZER AMPLIFIER WITH ALC

The KA2220 is a monolithic integrated circuit consisting of a preamplifier and ALC circuit for cassette tape recorder.

9 Sip Unit: mm



FEATURES

- **Low noise amplifier.**
- **Wide operating supply voltage range (3.5V ~ 14V).**
- **High output voltage.**
- **Low distortion.**
- **Wide ALC range.**
- **KA2220 ST: Good ALC pair characteristic for stereo tape recorder.**

SCHEMATIC DIAGRAM

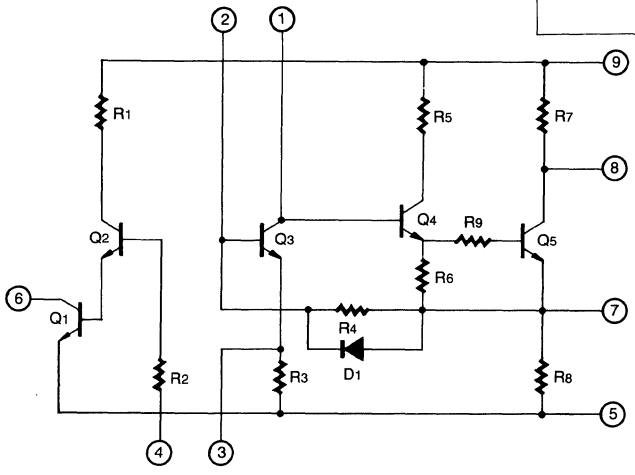


Fig. 1

TEST CIRCUIT

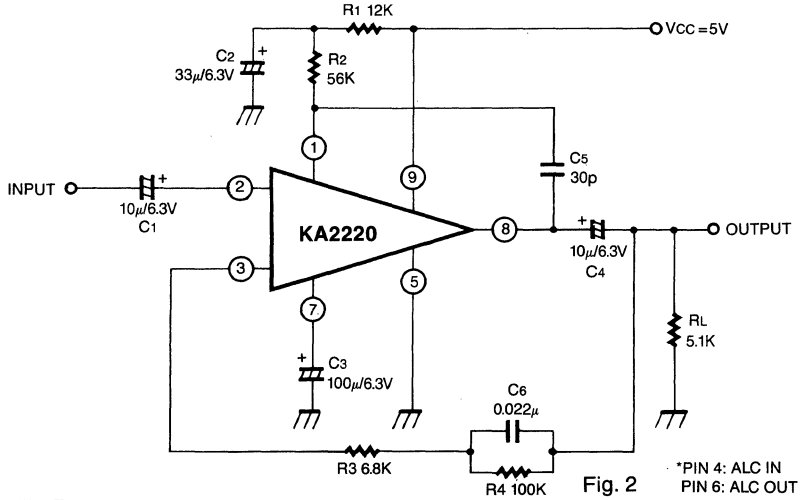


Fig. 2

*PIN 4: ALC IN
PIN 6: ALC OUT

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Power Dissipaiton	P_d	200	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 5V, R_L = 5.1KΩ, R_g = 600Ω, f = 1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0, ALC OFF		1.4	2.0	mA
Voltage Gain (Open Loop)	A_{VO}		66	69		dB
Voltage Gain (Closed Loop)	A_V	V_O =0.7Vrms	33	35	37	dB
Output Voltage	V_O	THD=1%	0.7	1.0		V
Total Harmonic Distortion	THD	V_O =0.2V		0.1		%
Input Resistance	R_i		60	100		KΩ
Equivalent Input Noise Voltage	V_{NI}	R_g =2.2KΩ, NAB BW (−3dB) = 15Hz ~ 30KHz		1.0		μV
ALC Transistor Saturation Voltage	V_{SAT}			75	100	mV

ALC GRADE BINNING TEST CIRCUIT

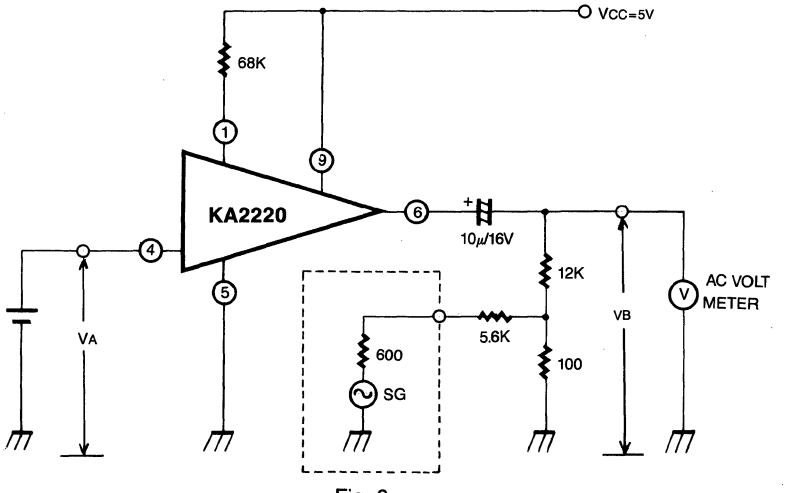


Fig. 3

Test condition: S.G output level should be adjusted to be 13.8mV of the AC voltmeter reading (V_B) when the D.U.T is not connected from the test circuit (V_{CC} =5V, V_A =1.16V, T_a =25°C)

ALC RANK is defined as ALC-G.R=20log V_{B2}/V_{B1}

where

V_{B1}: AC voltmeter reading when the D.U.T is not connected

V_{B2}: AC voltmeter reading whn the D.U.T is connected

ALC-G.R BINNING TABLE

Symbol	A_V (dB)		ALC Grade (dB)	
	Min	Max	Min	Max
KA2220 A	33	35	-16.0	-20.0
KA2220 B			-18.5	-22.5
KA2220 C			-21.0	-25.0
KA2220 D			-24.0	-28.0
KA2220 E			-27.0	-31.0
KA2220 F			-30.0	-34.0
KA2220 H	34	36	-16.0	-20.0
KA2220 J			-18.5	-22.5
KA2220 K			-21.0	-25.0
KA2220 L			-24.0	-28.0
KA2220 M			-27.0	-31.0
KA2220 N			-30.0	-34.0
KA2220 P	35	37	-16.0	-20.0
KA2220 R			-18.5	-22.5
KA2220 S			-21.0	-25.0
KA2220 T			-24.0	-28.0
KA2220 U			-27.0	-31.0
KA2220 V			-30.0	-34.0

External Components (Refer to test circuit)

C_1: Input coupling capacitor
The recommanded value is 10μF. If made too small, low frequency characteristic should be changed for the worse, too large a capacitance value will increase rising time when power is applied.

C_2: Ripple filter for power supply
The large value required to get an excellent ripple characteristic under the line operation, but sometime make smaller for starting time short.

C_3: Bypass capacitor
Short emitter resistor on AC and prevents AC signal from feedback to input.

C_4: Output coupling capacitor
C_4 is determined as follows.

$$C_4 = \frac{1}{2\pi \cdot f_L \cdot R_L}$$

f_L: low cut-off frequency
R_L: load resistance

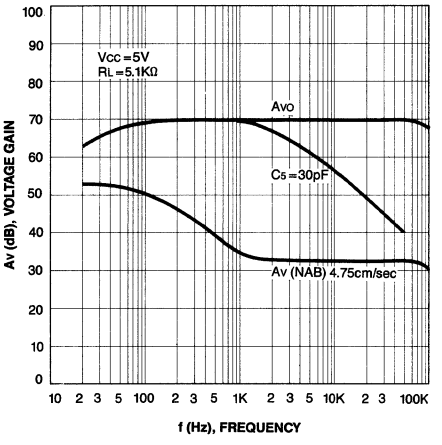
C_5: Phase compensation capacitor.
Prevents from high frequency oscillation by phase error when feedback deeply.

C_6, R_3, R_4: Equalizer network
Closed loop voltage gain determined by these components in relation to the internal resistance at pin 3.

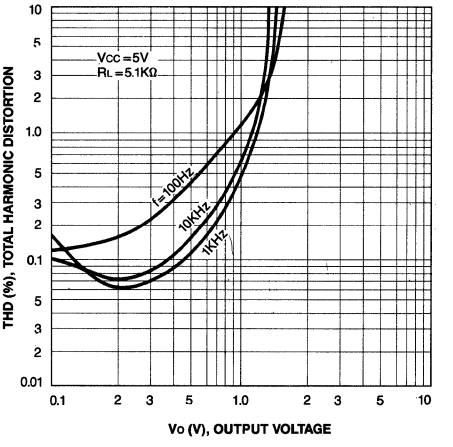
R_1: Filter resistance.

R_2: Collector resistor of first stage transistor of IC
Low voltage characteristic can be improved by adjusted this resistance.

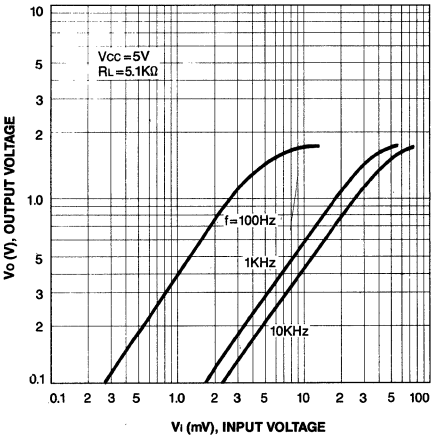
VOLTAGE GAIN-FREQUENCY



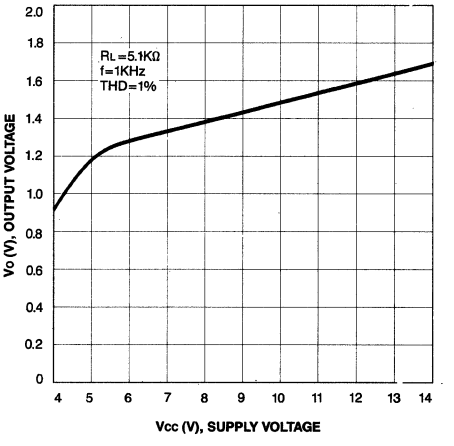
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



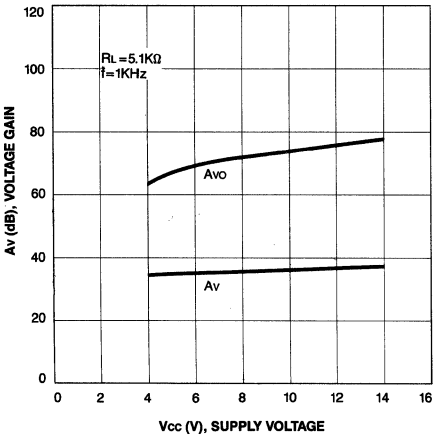
OUTPUT VOLTAGE-INPUT VOLTAGE



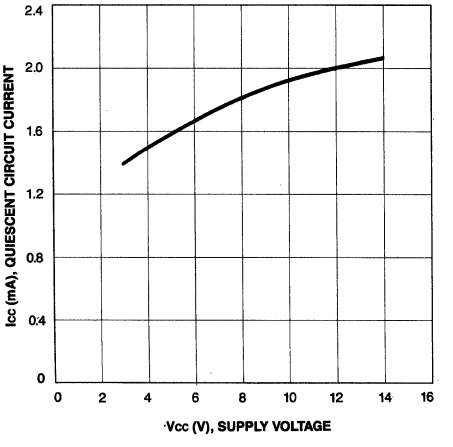
OUTPUT VOLTAGE-SUPPLY VOLTAGE



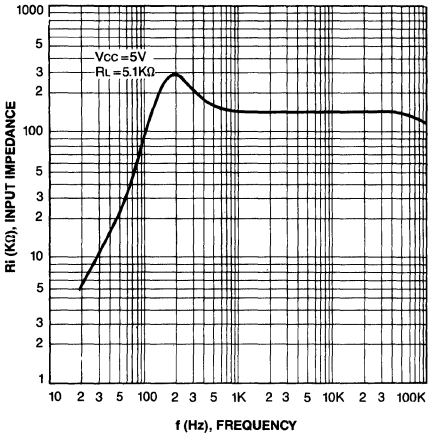
VOLTAGE GAIN-SUPPLY VOLTAGE



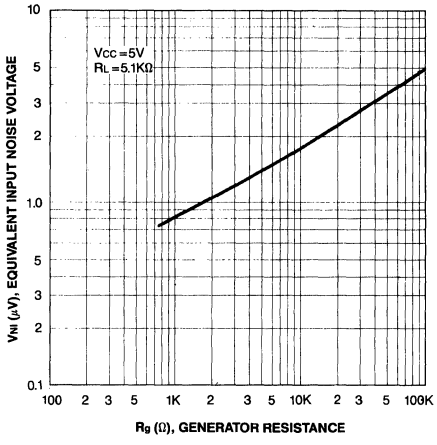
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



INPUT IMPEDANCE-FREQUENCY



EQUIVALENT INPUT NOISE VOLTAGE — GENERATOR RESISTANCE



TYPICAL APPLICATION CIRCUIT

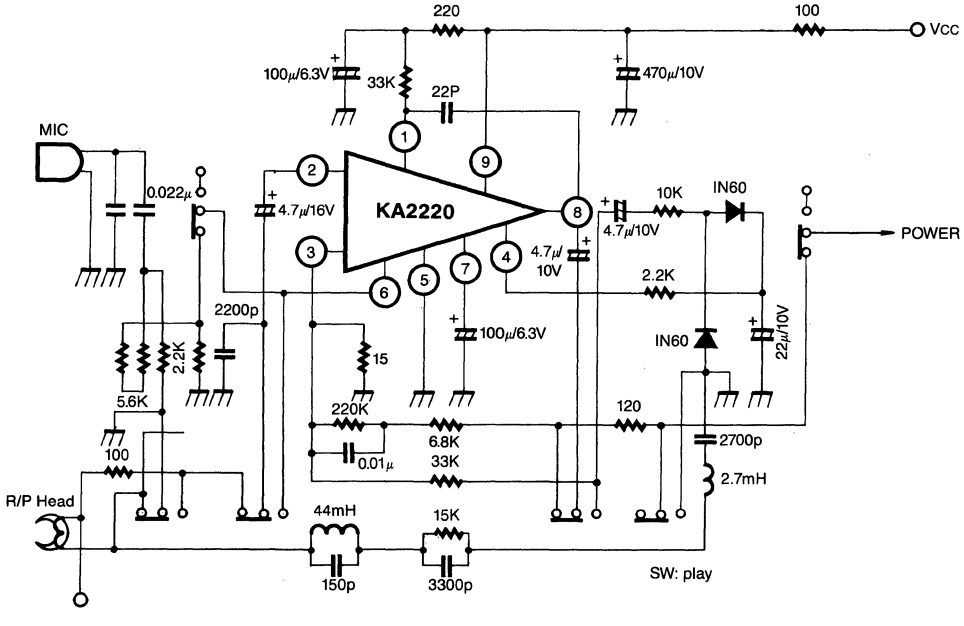
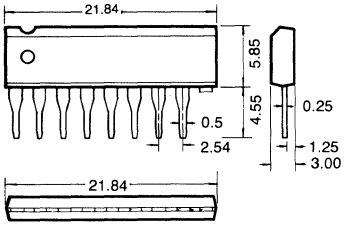


Fig. 4

DUAL LOW NOISE EQUALIZER AMPLIFIER

The KA2221 is a monolithic integrated circuit consisting of 2 channel low noise amplifiers and regulated power supply for car stereo.

8 Sip Unit: mm



FEATURES

- **Suitable for car stereo.**
- **Low noise amplifier.**
- **Voltage regulator included.**
- **Good ripple rejection.**
- **High channel separation (65dB Typ).**
- **Minimum number of external parts required.**

SCHEMATIC DIAGRAM

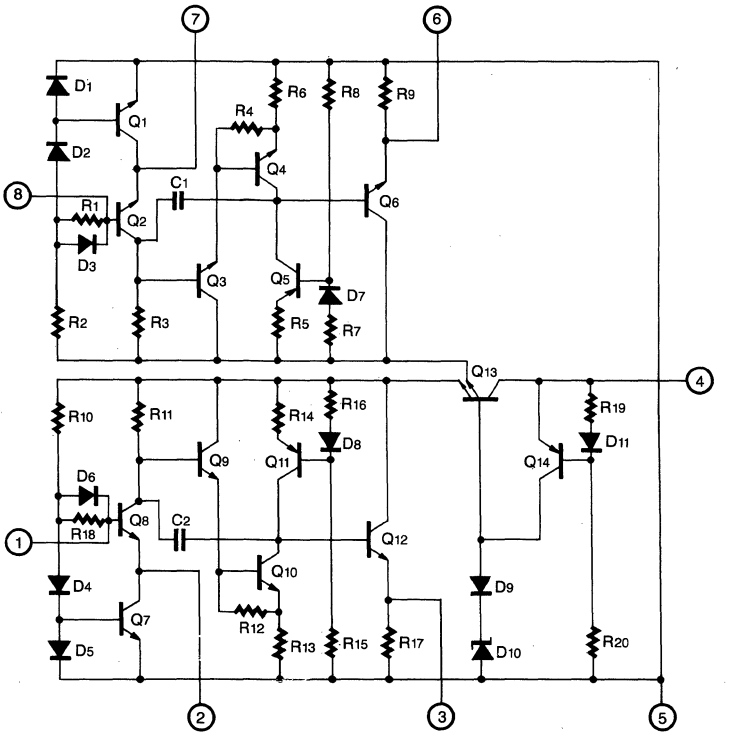


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Power Dissipation	P_d	200	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =250°C, V_{CC} =12V, R_L =10KΩ, f=1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		6.0	9.0	mA
Voltage Gain (Open Loop)	A_{VO}		65	80		dB
Voltage Gain (Closed Loop)	A_V	V_O =0.5Vrms	33	35	37	dB
Output Voltage	V_O	THD=1%	0.6	1.0		V
Total Harmonic Distortion	THD	V_O =0.5Vrms		0.1	0.3	%
Input Resistance	R_i			150		KΩ
Equivalent Input Noise Voltage	V_{NI}	R_g =2.2KΩ BW (−3dB) = 15Hz ~ 30KHz		1.0	2.0	μV
Cross Talk	CT	R_g = 2.2KΩ	50	65		dB

TEST CIRCUIT

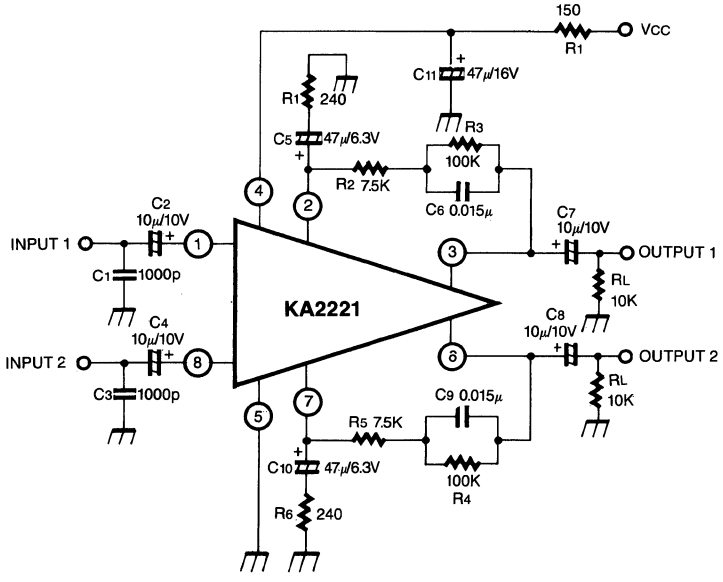
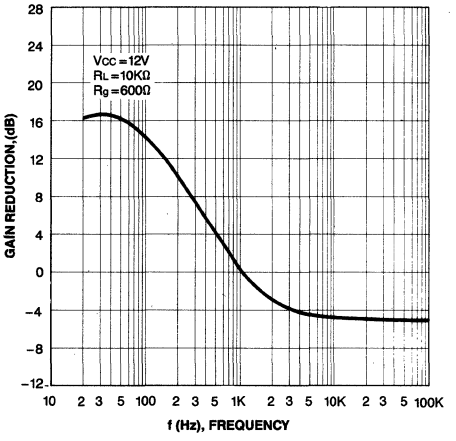
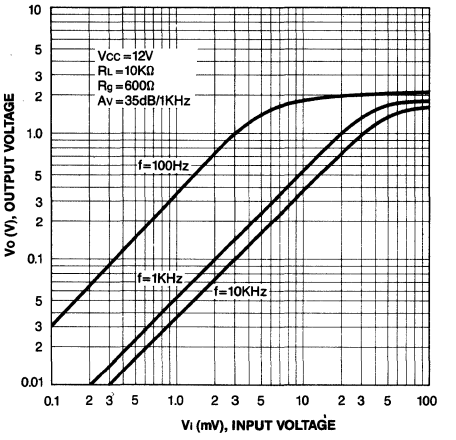


Fig. 2

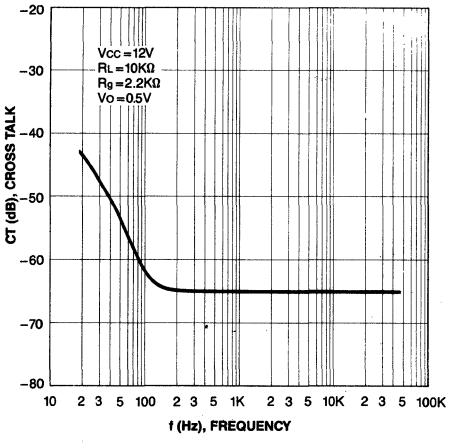
FREQUENCY RESPONSE



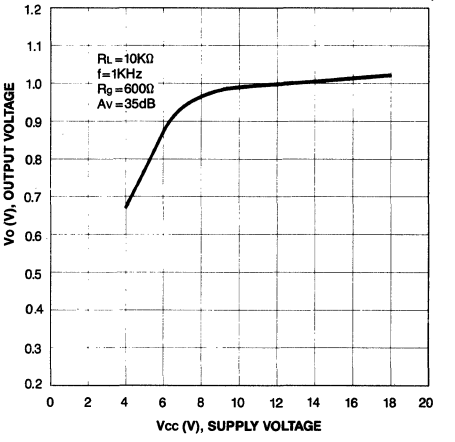
OUTPUT VOLTAGE-INPUT VOLTAGE



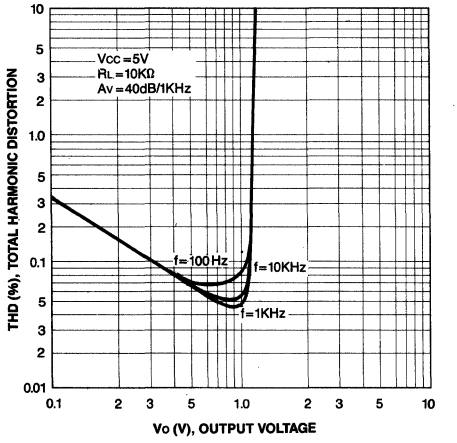
CROSS TALK-FREQUENCY



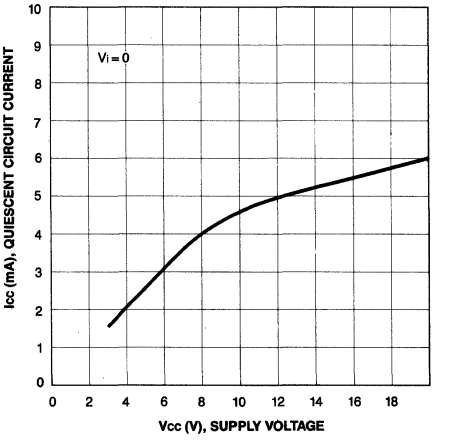
OUTPUT VOLTAGE-SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



External components (Refer to test circuit)

C_1 (C_3): Noise filter
These capacitors prevent from radio interference in the strong electric field. The recommanded value is 1000pF.

C_2 (C_4): Input coupling capacitor
The recommanded value is 10μF. If made too small, low frequency characteristic should be changed for the worse, too large value will increase rising time when power is applied.

C_5 (C_{10}): Negative feedback capacitor
The lower cut-off frequency depends on the value of these capacitors, and determined as follows.

$$C_5\ (C_{10}) = \frac{1}{2\pi f_L \cdot R_1\ (R_6)}$$

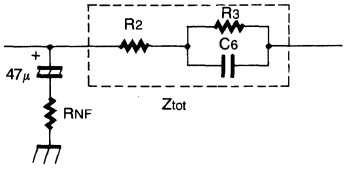
f_L: Low cut-off frequency
If the value of these capacitors are made larger, the starting time of amplifier is more delayed.

C_7 (C_8): Output coupling capacitor
The recommended value is 10μF.

R_2, R_3, C_6 (R_4, R_5, C_9): Equalizer network
The time constants of standard NAB characteristic are follow.

Tape speed	9.5cm/sec	4.75cm/sec
C_6 ($R_2 + R_3$) R_2, C_6	3180μsec 90μsec	1590μsec 120μsec

R_1 (R_6): Feedback component
The closed loop gain is determined approximately by the following relationship.

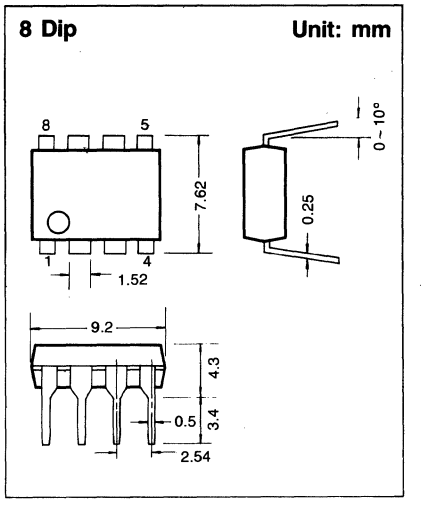


$$A_v = 20 \log \frac{Z_{tot}}{R_{NF}} (dB)$$

$$Z_{tot} = R_2 + R_3 // C_6$$

DUAL LOW NOISE EQUALIZER AMPLIFIER

The KA2222 is a monolithic integrated circuit cosisting of 2 channel preamplifier in 8 pin dual in line package.
Minimum operating voltage is 2.5 Volt, thus it is stuitable for low voltage application.



FEATURES

- **Suitable for mini cassette tape recorder.**
- **Low noise (V_{NI} =1.0μV: Typ).**
- **High channel separation.**
- **Good channel balance.**
- **Minimum number of external parts required.**

SCHEMATIC DIAGRAM

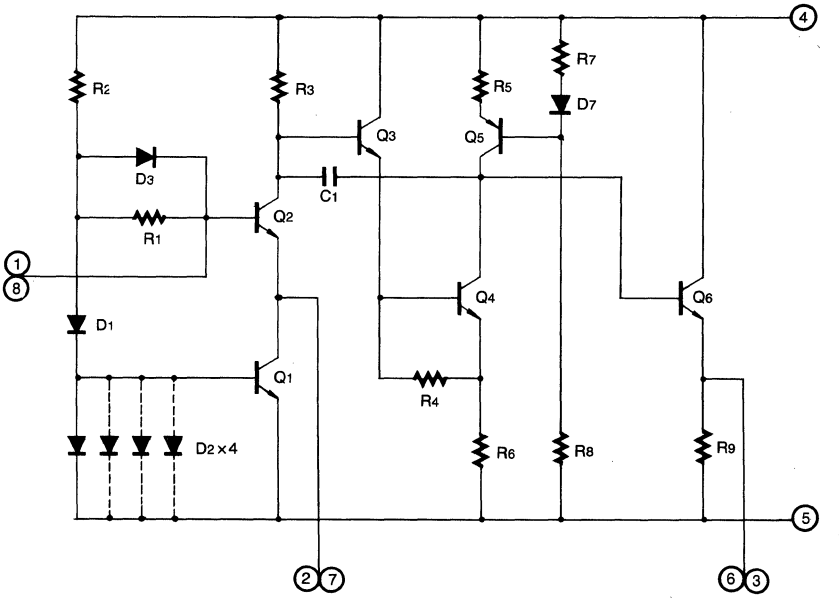


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.5	V
Power Dissipation	P_d	200	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 4V, R_L = 10KΩ, Rg = 600Ω, f = 1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		2.0	6.0	mA
Voltage Gain (Open Loop)	A_{VO}		65	80		dB
Voltage Gain (Closed Loop)	A_V	V_O = 0.2V	33	35	37	dB
Output Voltage	V_O	THD=1%	0.4	0.7		V
Total Harmonic Distortion	THD	V_O = 0.2V		0.1	0.3	%
Input Resistance	R_i			150		KΩ
Equivalent Input Noise Voltage	V_{NI}	R_g = 2.2KΩ BW (−3dB) = 15Hz ~ 30KHz		1.0	2.0	μV
Cross Talk	CT	R_g = 2.2KΩ	50	65		dB

TEST CIRCUIT

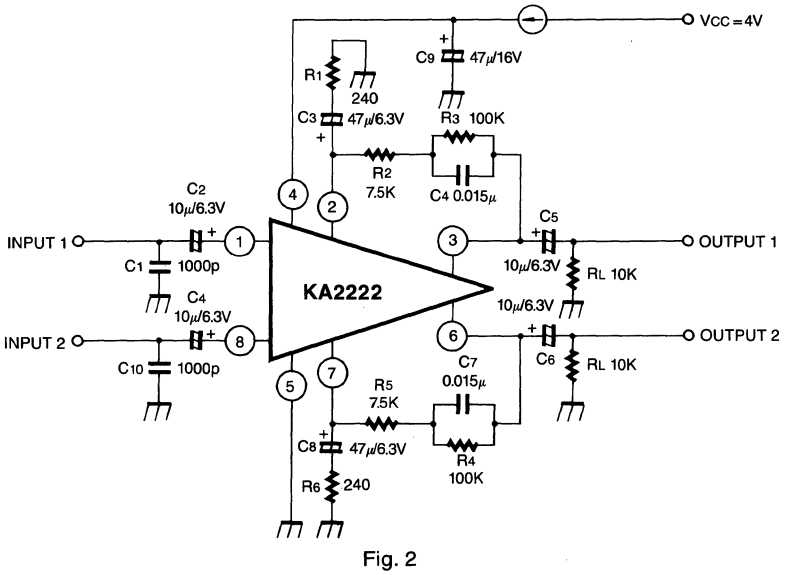
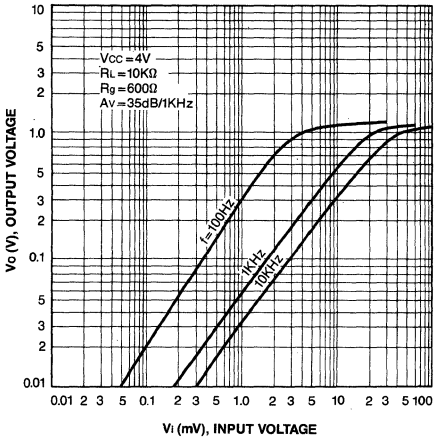
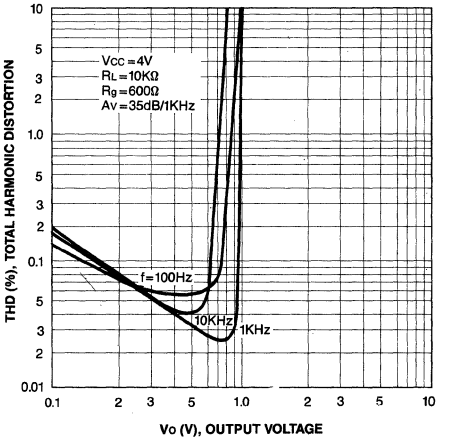


Fig. 2

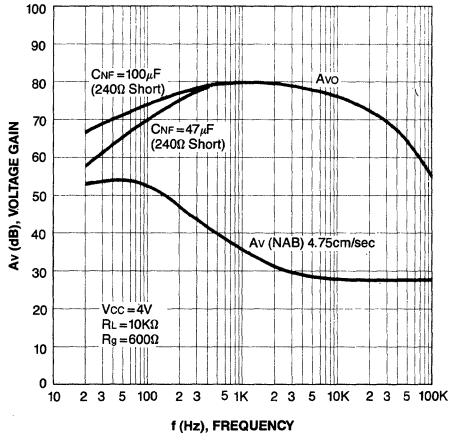
OUTPUT VOLTAGE-INPUT VOLTAGE



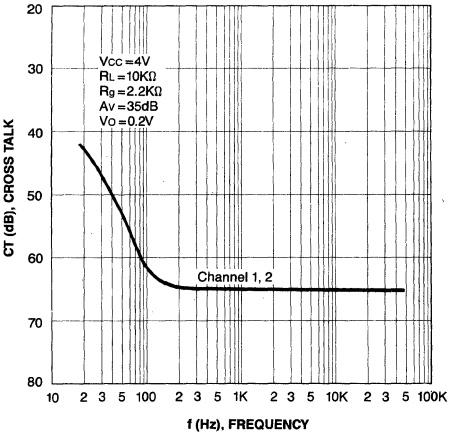
TOTAL HARMONIC DISTORTION -OUTPUT VOLTAGE



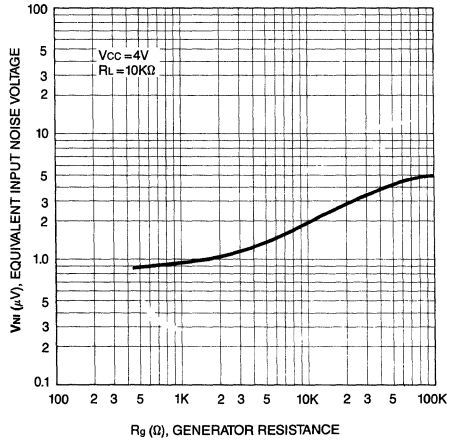
VOLTAGE GAIN-FREQUENCY



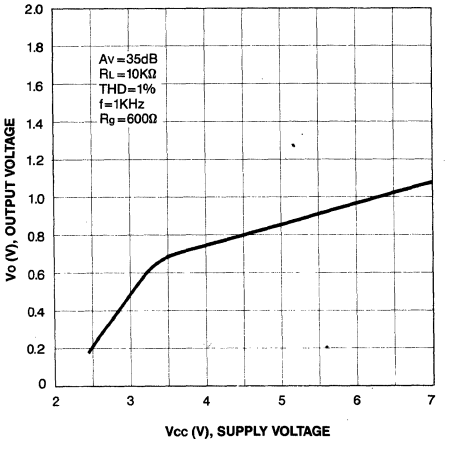
CROSS TALK-FREQUENCY



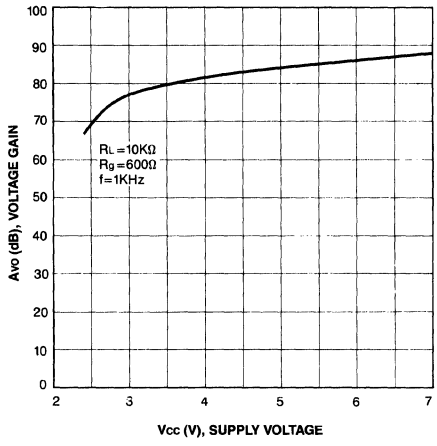
EQUIVALENT INPUT NOISE VOLTAGE -GENERATOR RESISTANCE



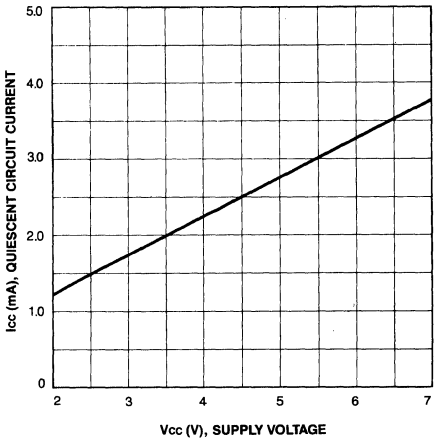
OUTPUT VOLTAGE-SUPPLY VOLTAGE



VOLTAGE GAIN-SUPPLY VOLTAGE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



TYPICAL APPLICATION CIRCUIT

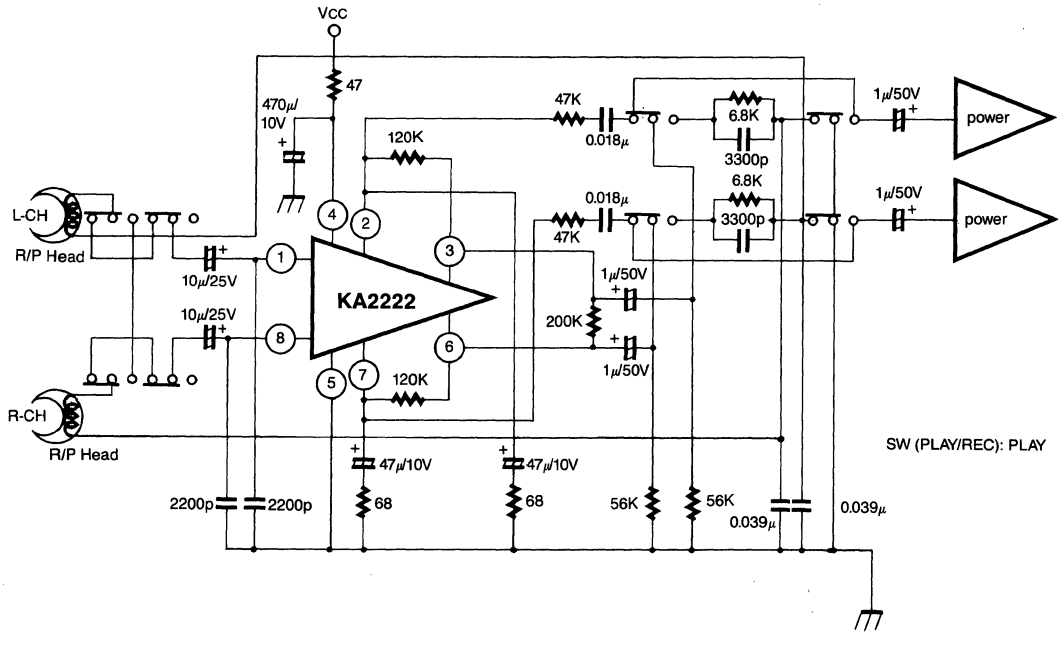


Fig. 3

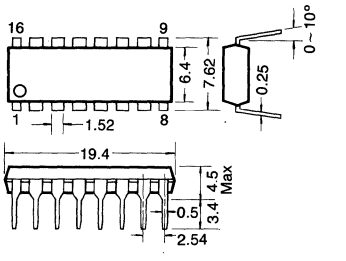
5CH GRAPHIC EQUALIZER AMPLIFIER

The KA2223 is a monolithic integrated circuit consisting of operational amplifier five resonant circuit with active filter, and it is suitable for radio-cassette tape recorder, car stereo or music center audio system.

FEATURES

- **Tone control with independent adjustment of each band through external capacitor.**
- **Gain control through external variable resistor.**
- **Increasing the bands by adding resonant circuit or using two KA2223 in series.**
- **Low noise (V_{NO} =7μV: Typ. Flat).**
- **Low distortion (THD=0.02% Typ. f=1KHz Flat).**
- **Large allowable input (V_i = 2.3V: Typ, V_{CC} =9V, f=1KHz Flat).**

16 Dip **Unit: mm**



SCHEMATIC DIAGRAM

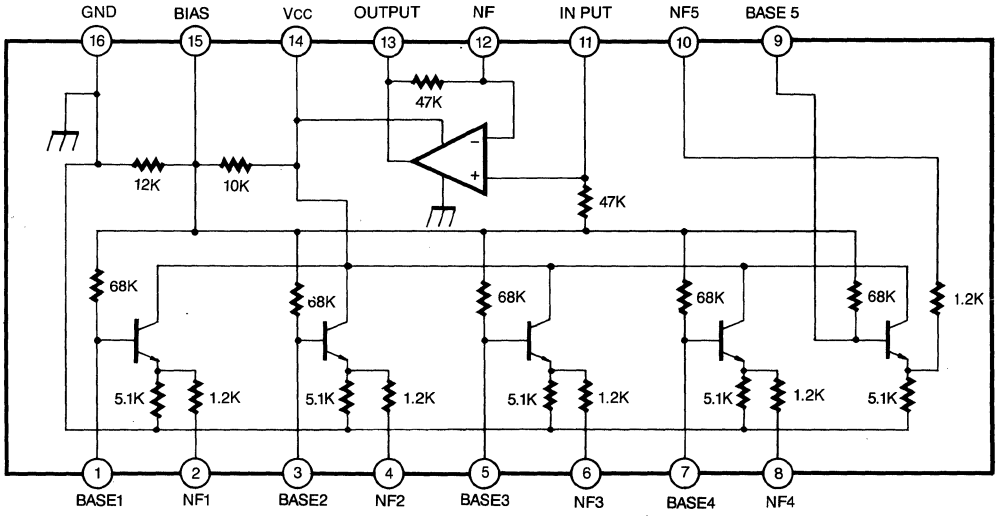


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Output Current	I_O	50	mA
Power Dissipation	P_d	700	mW
Operating Temperature	Topr	−20 ~ +75	°C
Storage Temperature	Tstg	−55 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=9V)

Characteristic		Symbol	Test		Min	Typ	Max	Unit
			f(Hz)	Condition				
Quiescent Circuit Current		I_{CC}		V_i=0	3.0	5.2	8.0	mA
Voltage Gain	Flat	A_V (Flat)	1K		−3.8	−0.8	2.2	dB
	Boost	A_V (Boost)	108		7.2	9.7	11.2	dB
			343		7.2	9.7	11.2	dB
			1.08K	V_i=−10dBm	7.2	9.7	11.2	dB
			3.43K		7.2	9.7	11.2	dB
			10.8K		7.2	9.7	11.2	dB
	Cut	A_V (Cut)	108		−12.8	−11.3	−8.8	dB
			343		−12.8	−11.3	−8.8	dB
			1.08K	V_i=−10dBm	−12.8	−11.3	−8.8	dB
			3.43K		−12.8	−11.3	−8.8	dB
			10.8K		−12.8	−11.3	−8.8	dB
Total Harmonic Distortion		THD	1K	V_i=1V		0.02	0.1	%
Output Noise Voltage		V_{NO}	Input Short BW: 10Hz ~ 30KHz (Flat)			7.0	30	μV

APPLICATION CIRCUIT 1

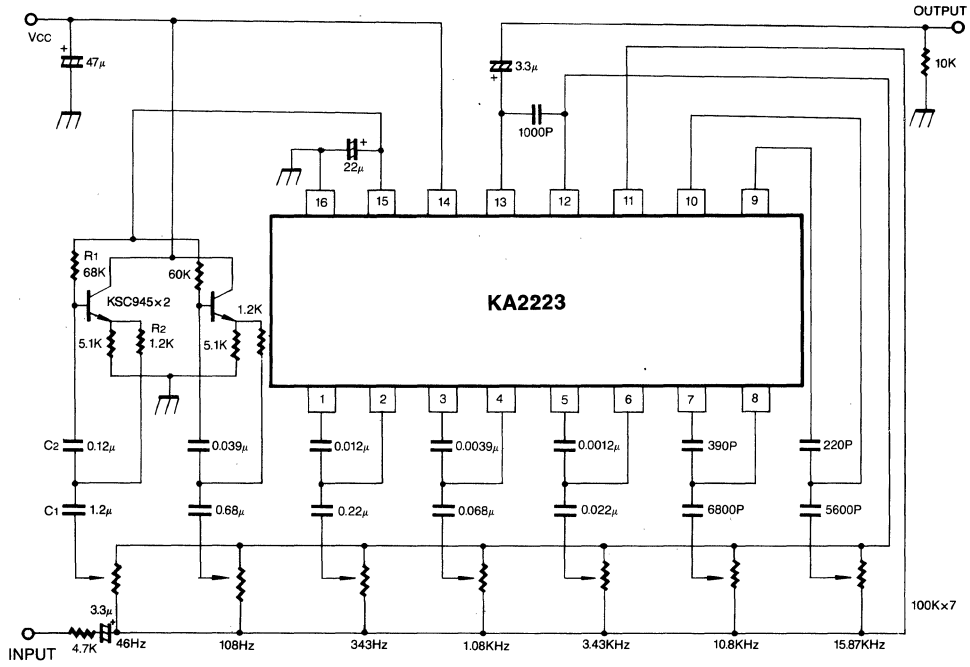


Fig. 3

$$\text{Resonant frequency } fp = \frac{1}{2\pi\sqrt{R_1 \cdot R_2 \cdot C_1 \cdot C_2}}$$

APPLICATION CIRCUIT 2

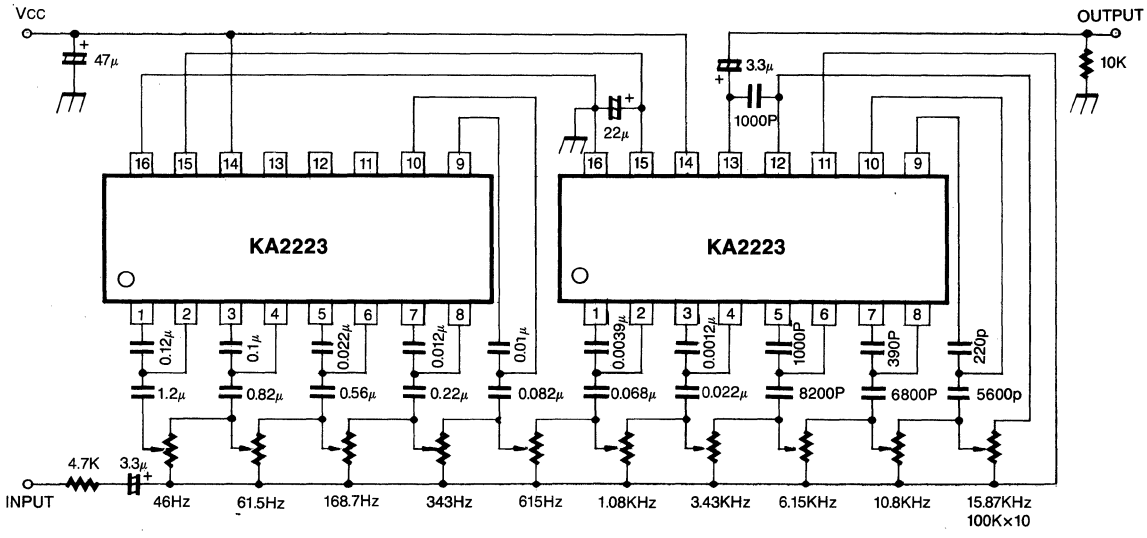


Fig. 4

TYPICAL APPLICATION CIRCUIT

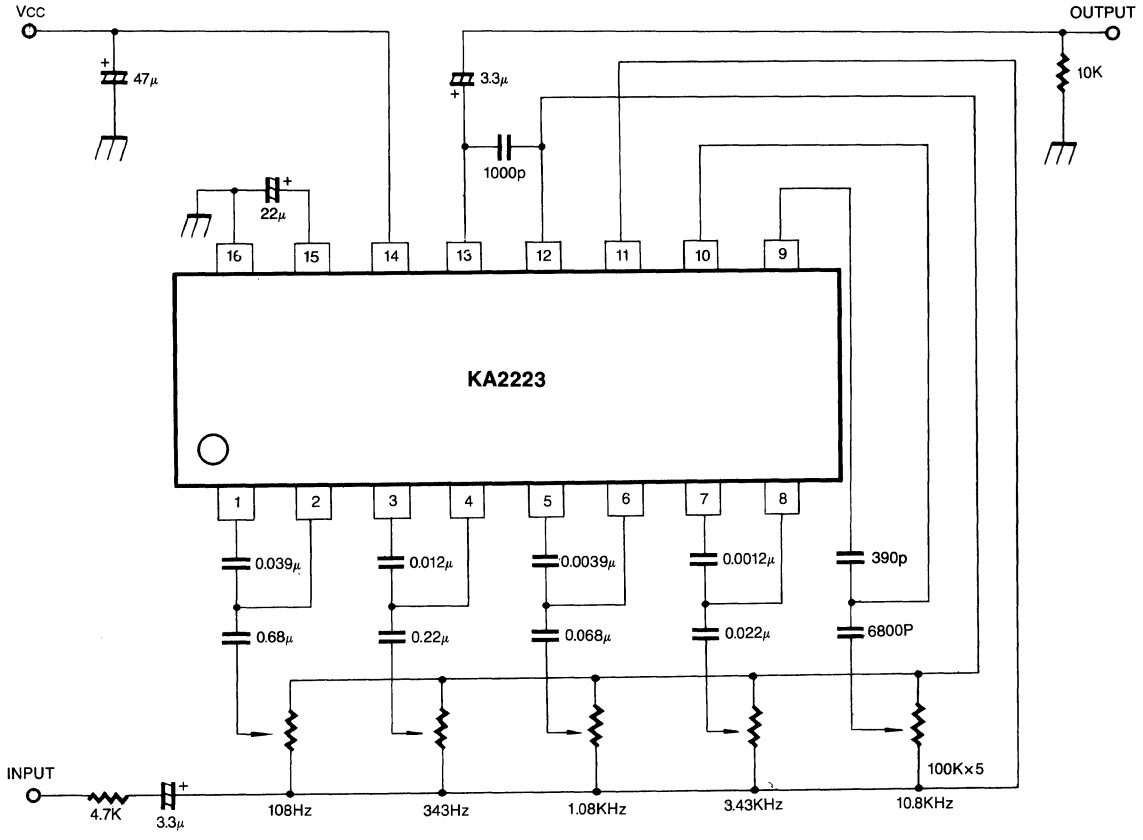
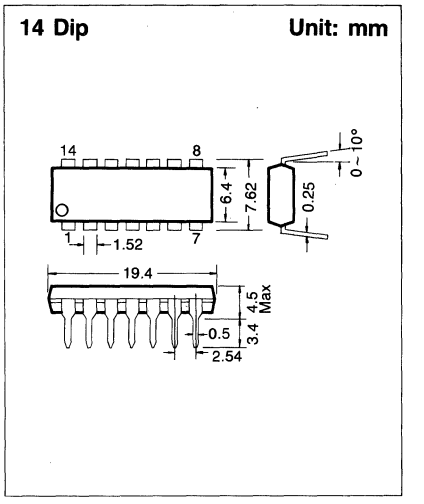


Fig. 2

DUAL EQUALIZER AMPLIFIER WITH ALC

The KA2224 is a monolithic integrated circuit consisting of dual equalizer amplifier with ALC, and it is suitable for stereo radio cassette.



FEATURES

- **Dual equalizer amplifier with built-in ALC circuit.**
- **Recording amp available because of high gain characteristic (Variable monitor possible).**
- **Good channel separation (Sep=50dB Typ).**
- **Quick stabilization after power on.**
- **Capable of direct meter driving and ALC transistor.**
- **Good ALC response balance between channels.**
- **Wide operating supply voltage range (4V ~ 13V).**

BLOCK DIAGRAM

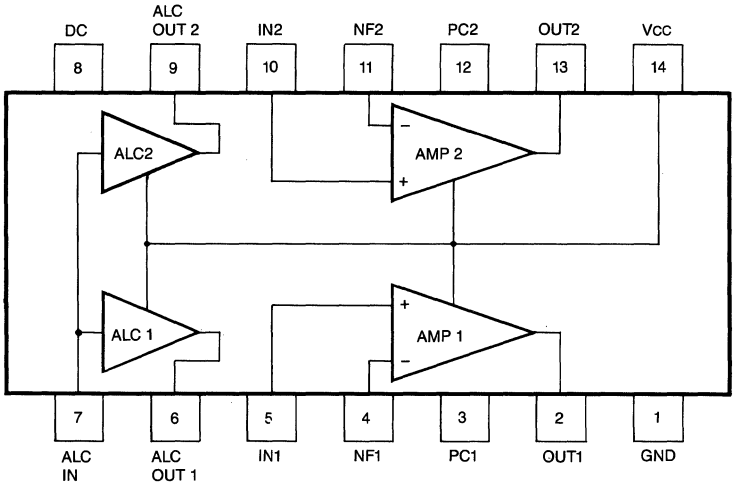


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	V
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C
ALC TR Maximum Current		3.5	mA

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 5V, R_L = 10KΩ: play, R_L = 680Ω: Recording)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current	I_{CC}	V_i = 0		4.5	10	mA
Voltage Gain (Open Loop)	A_{VO}			85		dB
Voltage Gain (Closed Loop)	A_{V1}	Play		40		dB
	A_{V2}	Record		58		dB
Output Voltage	V_O	THD = 1%, Play	0.9	1.2		V
Total Harmonic Distortion	THD	V_O = 0.5V, Play		0.1	1.0	%
Input Resistance	R_i		21	30		KΩ
Equivalent Input Noise Voltage	V_{NI}	BW (−3dB) = 20Hz ~ 20KHz		1.0	2.0	μV
Cross Talk	CT	Rg = 2.2KΩ	40	50		dB
ALC Range		V_i = −60dBm, Record	35	45		dB
ALC Balance		V_i = −20dBm, Record		0	2.0	dB
ALC Distortion		V_i = −20dBm, Record		0.5	2.0	%

TESR CIRCUIT

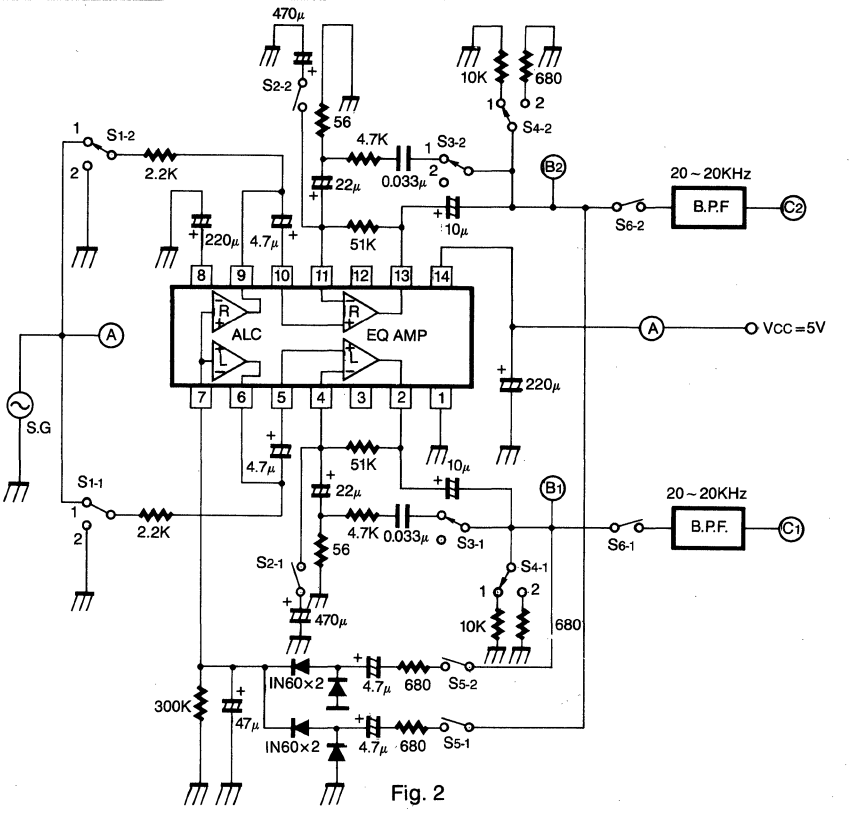


Fig. 2

TEST METHOD

Characteristic	S1	S2	S3	S4	S5	S6	Test Point	Test Method
I_{CC}	2	off	off	1	off	off		
A_{VO}	1	on	off	1	off	off	A, B	$A_{VO}=20\log V_O/V_i$ (dB) with Input voltage V_i, output voltage at V_O
A_V	1	off	on	1	off	off	A, B	$A_V=20\log V_O/V_i$ (dB)
V_O	1	off	on	1	off	off	B	Measure output voltage V_O at THD=1%
THD	1	off	on	1	off	off	B	Measure distortion factor at $V_O=0.5V$
CT	S1-1 S1-2 1 2 2 1	off	on	1	off	off	B	Measure crosstalk of amp 1,2 at output voltage $V_O=0$ dBm
V_{NI}	2	off	on	1	off	on	C	Convert output noise voltage at 1KHz gain when $R_g=2.2K\Omega$
ALC Range	1	off	off	2	on	off	B	Input voltage range from when input voltage $V_i=-60$dBm until output voltage V_O goes up 3 dB.
ALC Balance	1	off	off	2	on	off	B	Output voltage V_O level difference of amp 1, 2 when input voltage $V_i=-20$dBm is applied.
ALC Distortion	1	off	off	2	on	off	B	Measure distortion factor when input voltage $V_i=-20$dBm is applied.

TYPICAL APPLICATION CIRCUIT

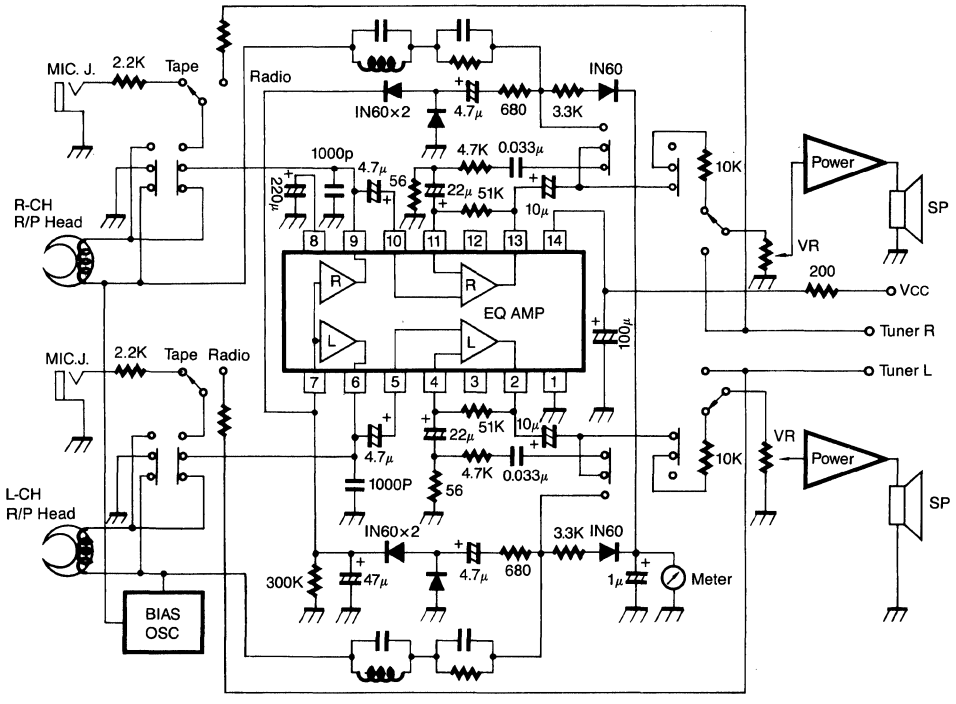


Fig.3

GENERAL OPERATING CONSIDERATIONS

1. Closed loop voltage gain

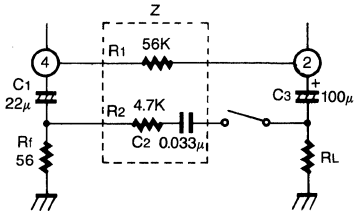


Fig. 4

SW on: play
off: record

A. Playback amplifier

$$Av = 20 \log \frac{Z}{Rf} \text{ (dB) at f=1KHz, Av=42dB (Typ)} \quad Z = R_1 // (R_2 + C_2)$$

B. Recording amplifier

$$Av = 20 \log \frac{R_1}{Rf} \text{ (dB) at f=1KHz, Av=58dB (Typ)}$$

2. ALC circuit

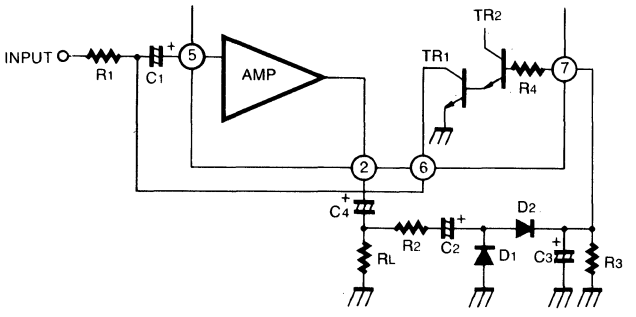


Fig. 5

The ALC circuit is consist of TR_1, TR_2 and some external components. The output level of amplifier is rectified by external circuits. Since this DC level is applied to the ALC input terminal (Pin 7), the impedance between collector and emitter of TR1 is available to change its value, therefore pre-amplifier input level can be controlled.

3. Oscillation suppression

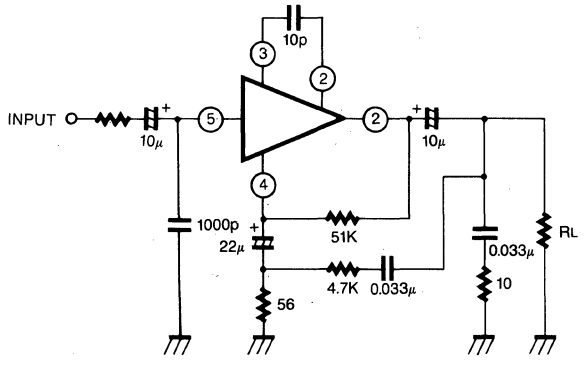
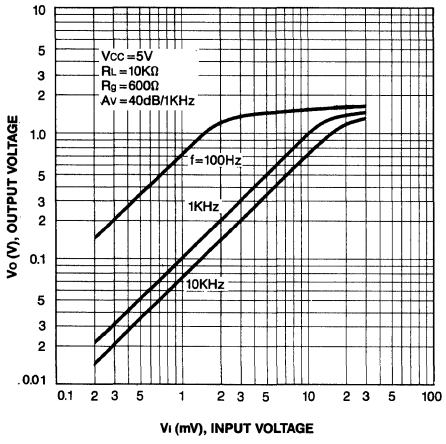


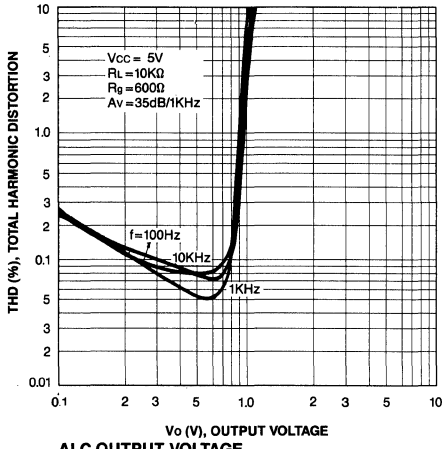
Fig. 6

If the closed loop gain of amplifier is designed lower than 40dB, the circuit should be compensated by connecting of 10pF between pin 3 and pin 2, and of 0.033μF (mylar)+10Ω to the load end.

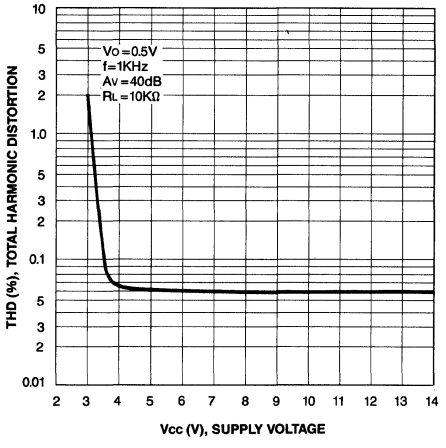
OUTPUT VOLTAGE-INPUT VOLTAGE



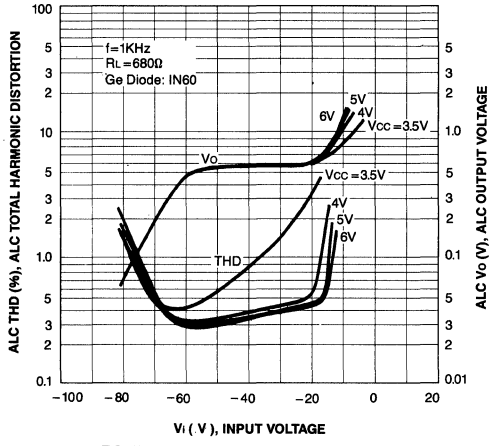
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



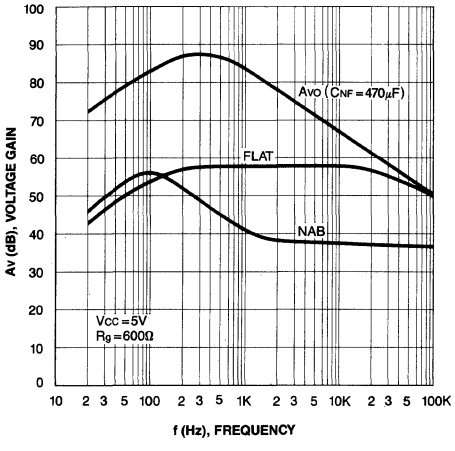
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



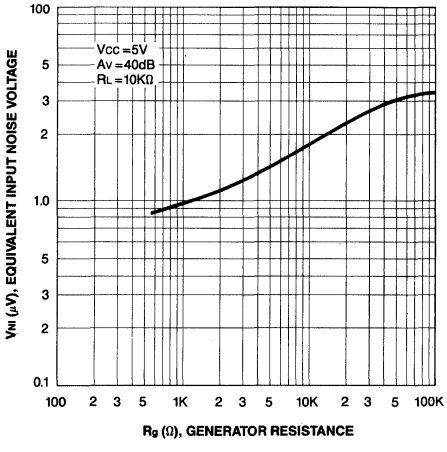
ALC OUTPUT VOLTAGE
ALC TOTAL HARMONIC DISTORTION —INPUT VOLTAGE



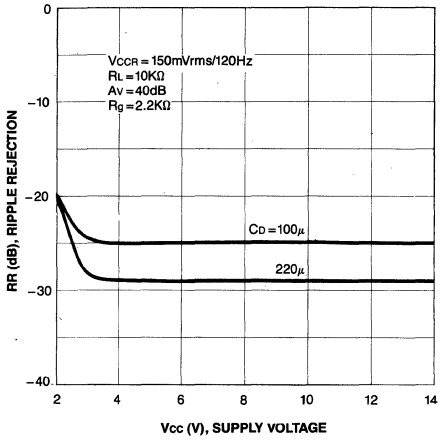
VOLTAGE GAIN-FREQUENCY



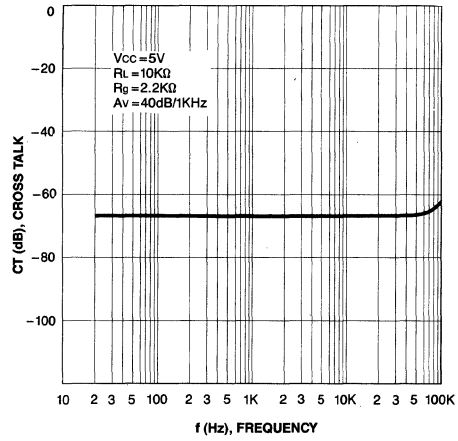
EQUIVALENT INPUT NOISE VOLTAGE
-GENERATOR RESISTANCE



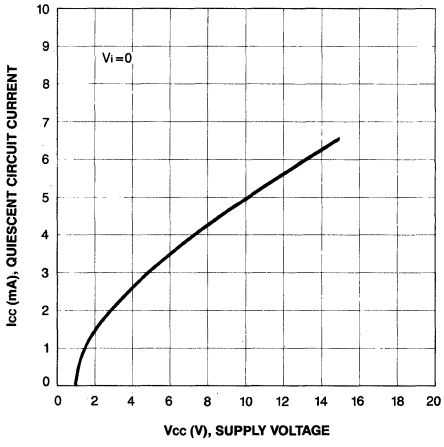
RIPPLE REJECTION-SUPPLY VOLTAGE



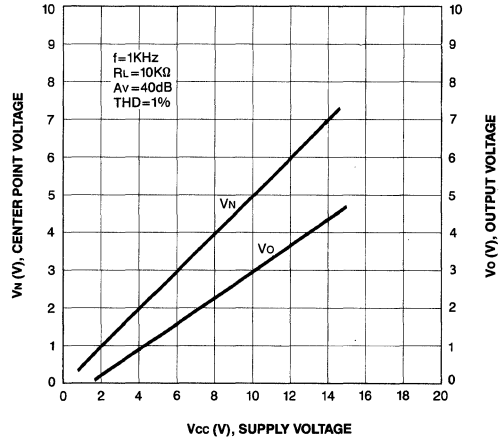
CROSS TALK-FREQUENCY



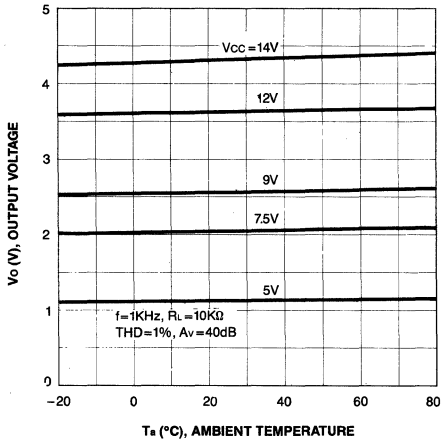
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



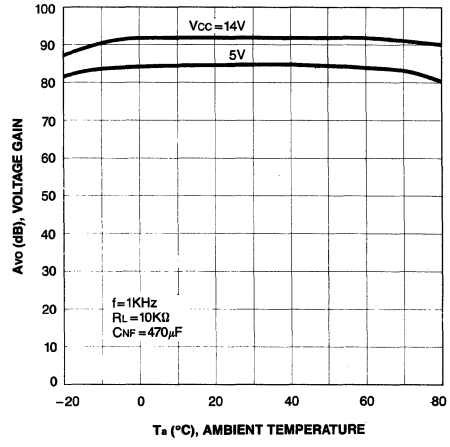
CENTER POINT VOLTAGE,-SUPPLY VOLTAGE
OUTPUT VOLTAGE-SUPPLY VOLTAGE



OUTPUT VOLTAGE-AMBIENT TEMPERATURE



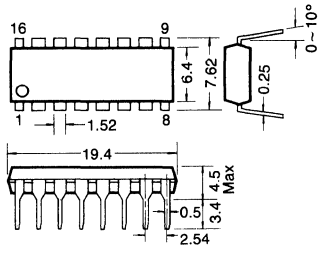
VOLTAGE GAIN-AMBIENT TEMPERATURE



DUAL PREAMPLIFIER FOR 3V USING

The KA2225 is a monolithic integrated circuit consisting of dual equalizer amplifier, and it is suitable for 3V stereo radio cassette.

16 Dip Unit: mm



FEATURES

- **High open loop gain: 85dB (typ) (V_{CC}=3V, f=1kHz).**
- **Non-necessary the input coupling capacitors.**
- **Operating supply voltage range: V_{CC}=1.6V~5V.**
- **Good channel seperation: 60dB (typ).**

BLOCK DIAGRAM

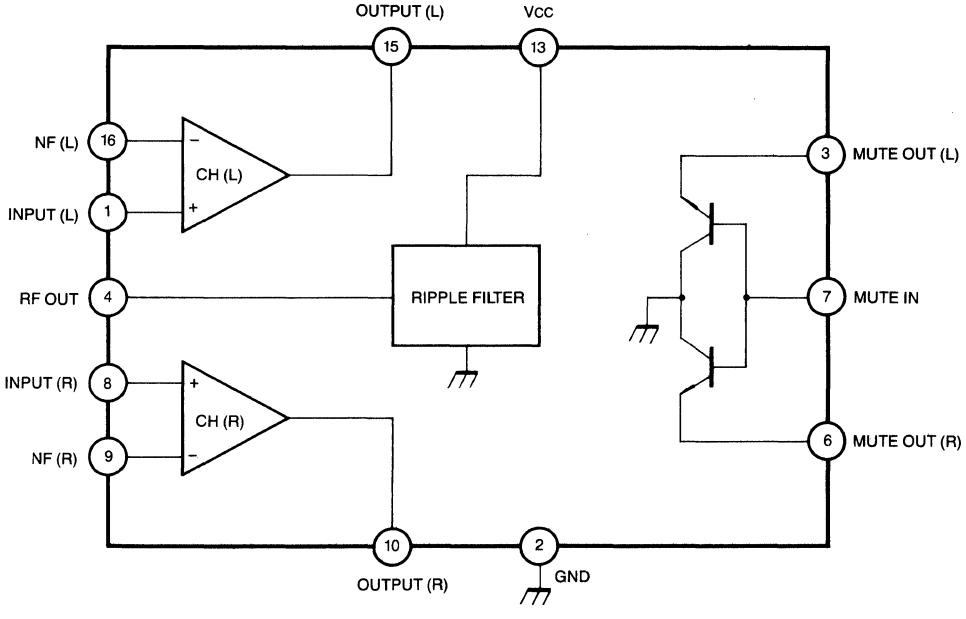


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7	V
Power Dissipation	P_d	750	mW
Operating Temperature	Topr	−25 ~ +75	°C
Storage Temperature	Tstg	−40 ~ +75	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =3V, f=1KHz)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i =0		2	3.4	mA
Voltage Gain	Open Loop	A_{VO}		70	85		dB
	Closed Loop	A_V			40		dB
Output Voltage		V_O	THD=1%	0.5	0.8		V
Total Harmonic Distortion		THD	V_O =0.1V,		0.07	0.5	%
Output Noise Voltage		V_{NO}	R_g =2.2KΩ, A_V =40dB BW=50Hz ~ 20KHz		0.14	0.22	mV
Cross Talk		CT	R_g =600Ω, V_O = −10dBv		60		dB
Muting Attenuation		ATT	V_{MUTE} =1V		43		dB
Input Resistance		R_i		20	30		KΩ

TEST CIRCUIT

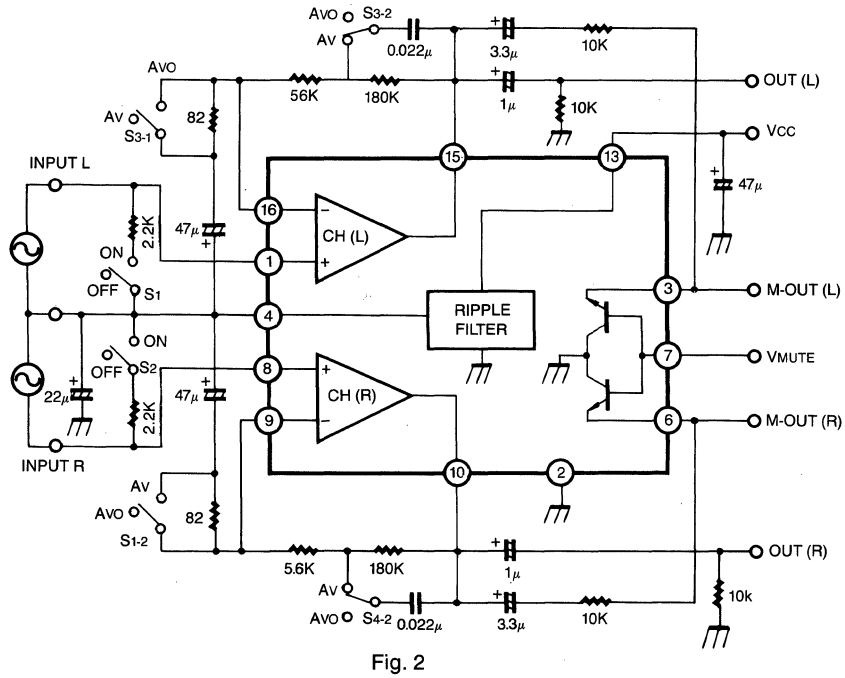


Fig. 2

APPLICATION CIRCUIT

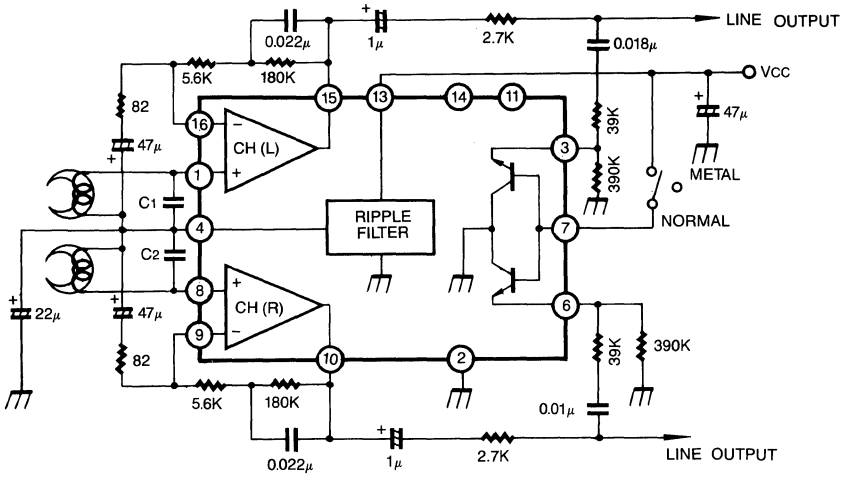


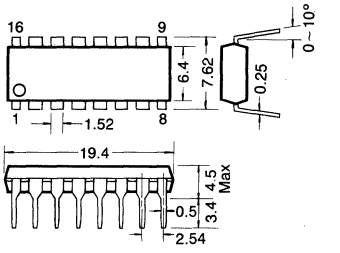
Fig. 3

- Capacitor C_1 and C_2 may be required for preventing a instability caused by the pattern layout or interference of external high frequency singal.

DUAL EQUALIZER AMPLIFIER WITH ALC

The KA2226 is a monolithic integrated circuit consisting of dual equalizer amplifier with ALC, and it is suitable for stereo radio cassettes.

16 Dip Unit: mm



FEATURES

- **Dual equalizer amplifier with ALC circuit.**
- **High open loop voltage gain: 85dB (typ).**
- **Recording amplifier available because of high open loop voltage gain.**
- **Non-necessary any diode or transistor for ALC.**
- **Good channel separation: 60dB (typ).**
- **Good ALC response balance between channels.**
- **Wide operating supply voltage range: V_{CC} =3V ~ 13V.**

BLOCK DIAGRAM

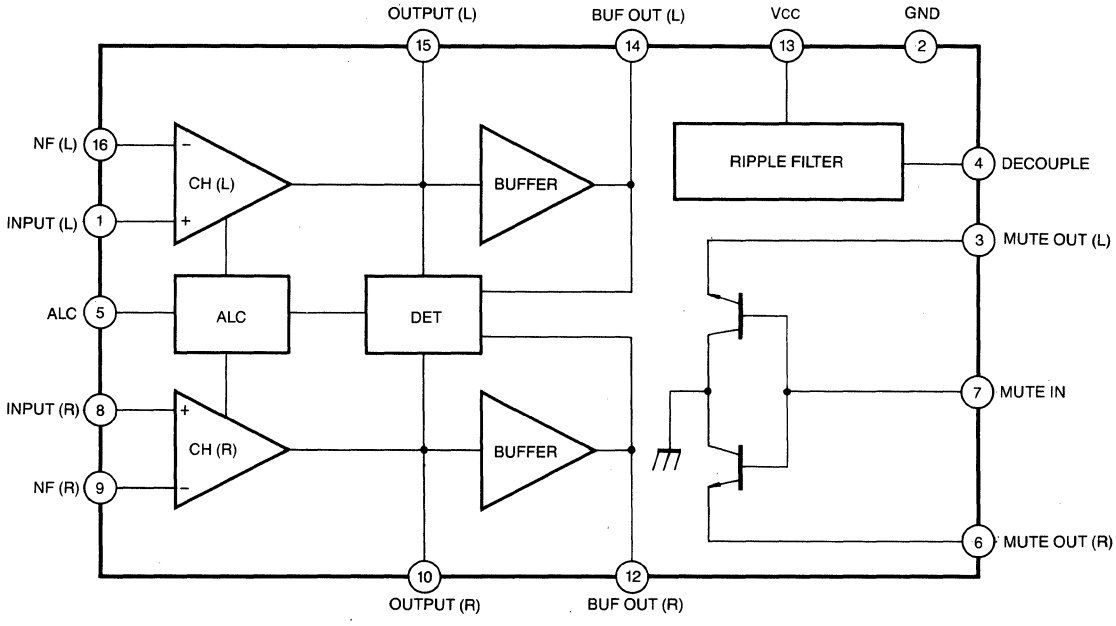


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	V
Power Dissipation	P_d	750	W
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 5V, R_L = 10KΩ (play), f = 1KHz unless otherwise specified)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i = 0		4.8	10	mA
Voltage Gain	Open Loop	A_{VO}			85		dB
	Closed Loop	A_{V1}/A_{V2}			40/58		dB
	Play/Record						
Output Voltage		V_O	THD=1%, Play	0.8	1.0		V
Total Harmonic Distortion		THD	V_O =0.5V, Play		0.1	1.0	%
Input Resistance		R_i		20	30		KΩ
Equivalent Input Noise Voltage		V_{NI}	BW (−3dB)=30Hz ~ 20KHz		1.4	2.2	μV
Cross Talk		CT	R_g =2.2KΩ, V_O = −10dBv		60		dB
ALC Range			V_i = −60dBm, Record	35	45		dB
ALC Balance			V_i = −20dBm, Record		0	2.0	dB
ALC Distortion			V_i = −20dBm, Record		0.5	2.0	%
ALC Voltage		V_O (ALC)	V_i = −20dBm, Record R_g =2.2KΩ		0.5		V
Muting Attenuation		ATT			50		dB

TEST CIRCUIT

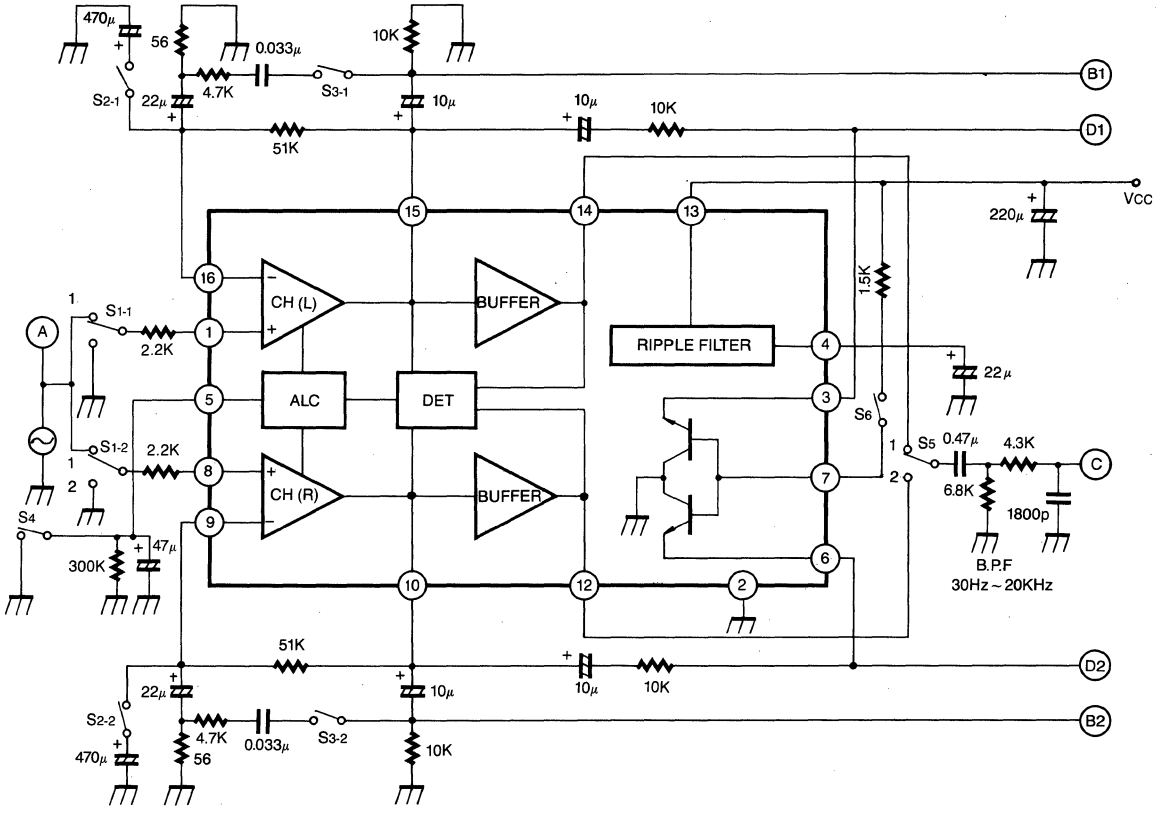


Fig. 2

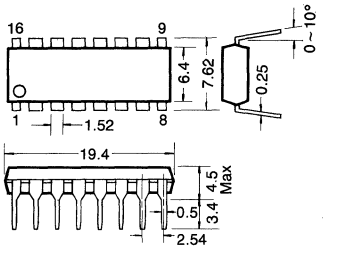
TEST METHOD

Characteristic	S1	S2	S3	S4	S5	S6	Test Point	Test Method
I_{CC}	2	off	off	on	off	off		
A_{VO}	1	on	off	on	off	off	A,B	$A_{VO}=20\log V_O/V_i$(dB) with Input Voltage V_i, Output Voltage at V_O
A_V	1	off	on	on	off	off	A,B	$A_V=20\log V_O/V_i$(dB)
V_O	1	off	on	on	off	off	B	Measure Output Voltage V_O at THD=1%
THD	1	off	on	on	off	off	B	Measure Distortion Factor at $V_O=0.5V$
CT	SI-1 SI-2 1 2 2 1	off	on	on	off	off	B	Measure Crosstalk of AMP L, R at Output Voltage $V_O=0$dBm
V_{NI}	2	off	on	on	R L 2 1	off	C	Convert Output Noise Voltage at 1KHz Gain When $R_g=2.2K\Omega$
ALC Range	1	off	off	off	2 1	off	C	Input Voltage Range from When Input Voltage $V_i=-60$dBm Until Output Voltage V_O Goes Up 3dB
ALC Balance	1	off	off	off	2 1	off	C	Output Voltage V_O Level Difference of AMP L, R When Input Voltage $V_i=-20$dBm is Applied
ALC Distortion	1	off	off	off	2 1	off	C	Measure Distortion Factor When Input Voltage $V_i=-20$dBm is Applied
Muting Attenuation	1	off	on	on	off	on	D	ATT=20 log V_O (M)/V_O

DUAL EQUALIZER AMPLIFIER WITH ALC FOR CAR

The KA2227 is a monolithic integrated circuit consisting of 2 channel low noise dual equalizer amplifiers with ALC, muting circuit, and regulated power supply for car stereo.

16 Dip Unit: mm



FEATURES

- **Suitable for car stereo.**
- **Dual equalizer amplifier with ALC circuit.**
- **High open loop voltage gain: 85dB (typ).**
- **Recording amplifier available because of high open loop voltage gain.**
- **Non-necessary any diode or transistor for ALC.**
- **Good channel separation: 60dB (typ).**
- **Good ALC response balance between channels.**
- **Wide operating supply voltage range: V_{CC} =6V ~ 18V.**
- **Good muting attenuation: 50dB (typ).**

BLOCK DIAGRAM

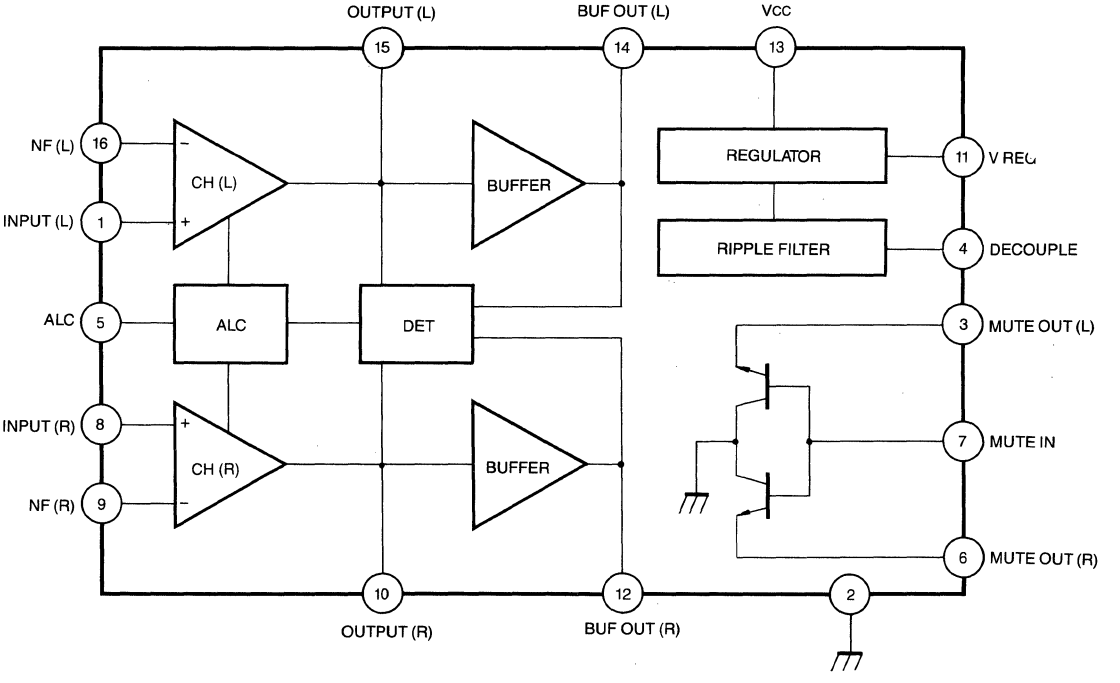


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Power Dissipation	P_d	750	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	-40 ~ +125	°C

* Mounted and soldered on a 50mm×50mm copper foil of PCB

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=9V, R_L=10KΩ (play), unless otherwise specified)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i=0		6.0	10	mA
Voltage Gain	Open Loop	A_{VO}			85		
	Closed Loop	A_{V1}/A_{V2}			40/58		dB
	Play/Record						
Output Voltage		V_O	THD=1%, Play	0.8	2.0		V
Total Harmonic Distortion		THD	V_O=0.5V, Play		0.1	1.0	%
Input Resistance		R_i		20	30		KΩ
Equivalent Input Noise Voltage		V_{N1}	BW (−3dB)=30Hz ~ 20KHz		1.4	2.2	μV
Cross Talk		CT	R_g=2.2KΩ, V_O=10dBv		60		dB
ALC Range			V_i=−60dBm, Record	35	45		dB
ALC Balance			V_i=−20dBm, Record		0	2.0	dB
ALC Distortion			V_i=−20dBm, Record		0.5	2.0	%
ALC Voltage		V_O(ALC)	V_i=−20dBm, Record R_g=2.2KΩ		0.5		V
Muting Attenuation		ATT			50		dB

TEST CIRCUIT

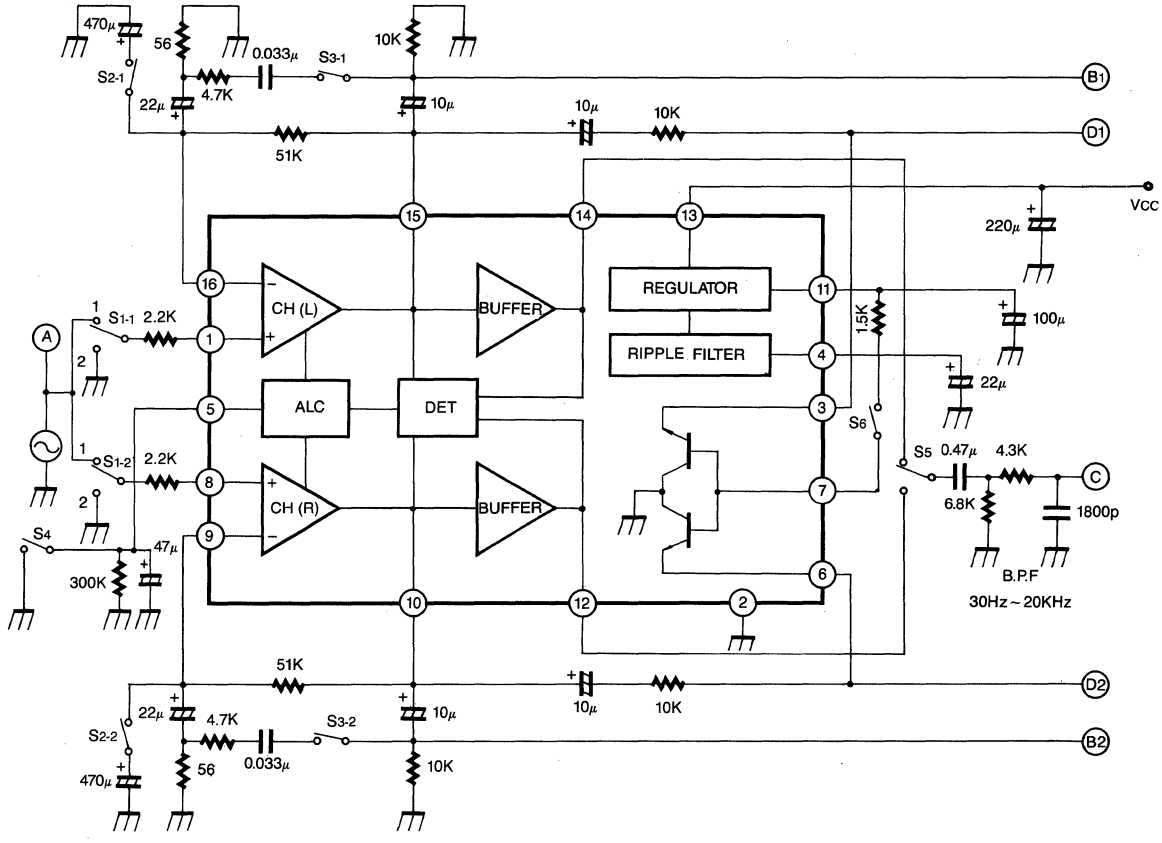


Fig. 2

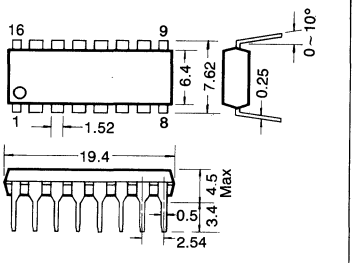
TEST METHOD

Characteristic	S1	S2	S3	S4	S5	S6	Test Point	Test Method
I_{CC}	2	off	off	on	off	off		
A_{VO}	1	on	off	on	off	off	A,B	$A_{VO}=20\log V_O/V_i$(dB) with Input Voltage V_i, Output Voltage at V_O
A_V	1	off	on	on	off	off	A,B	$A_V=20\log V_O/V_i$(dB)
V_O	1	off	on	on	off	off	B	Measure Output Voltage V_O at THD=1%
THD	1	off	on	on	off	off	B	Measure Distortion Factor at $V_O=0.5V$
CT	SI-1 SI-2 1 2 2 1	off	on	on	off	off	B	Measure Crosstalk of AMP L, R at Output Voltage $V_O=0dBm$
V_{NI}	2	off	on	on	R L 2 1	off	C	Convert Output Noise Voltage at 1KHz Gain When $R_g=2.2K\Omega$
ALC Range	1	off	off	off	2 1	off	C	Input Voltage Range from When Input Voltage $V_i=-60dBm$ Until Output Voltage V_O Goes Up 3dB
ALC Balance	1	off	off	off	2 1	off	C	Output Voltage V_O Level Difference of AMP L, R When Input Voltage $V_i=-20dBm$ is Applied
ALC Distortion	1	off	off	off	2 1	off	C	Measure Distortion Factor When Input Voltage $V_i=-20dBm$ is Applied
Muting Attenuation	1	off	on	on	off	on	D	ATT=20 log V_O (M)/V_O

AM/FM IF SYSTEM

The KA2241 is a monolithic integrated circuit consisting of four individual amplifiers and voltage regulator.

16 Dip Unit: mm



FEATURES

- **Suitable for AM/FM Radio.**
- **Wide operating supply voltage range (3.5V ~ 10V).**
- **Low power dissipation.**
- **High AM AGC figure of merit.**
- **High dynamic AMR-FM radio detection.**
- **High amplifier gain.**
- **AM/FM signal meter driver circuit included.**

BLOCK DIAGRAM

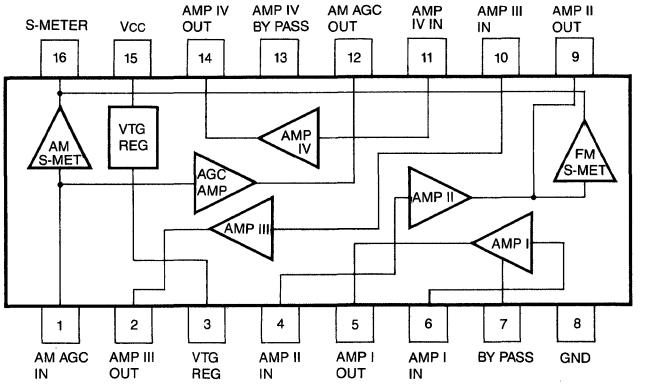


Fig. 1

TEST CIRCUIT

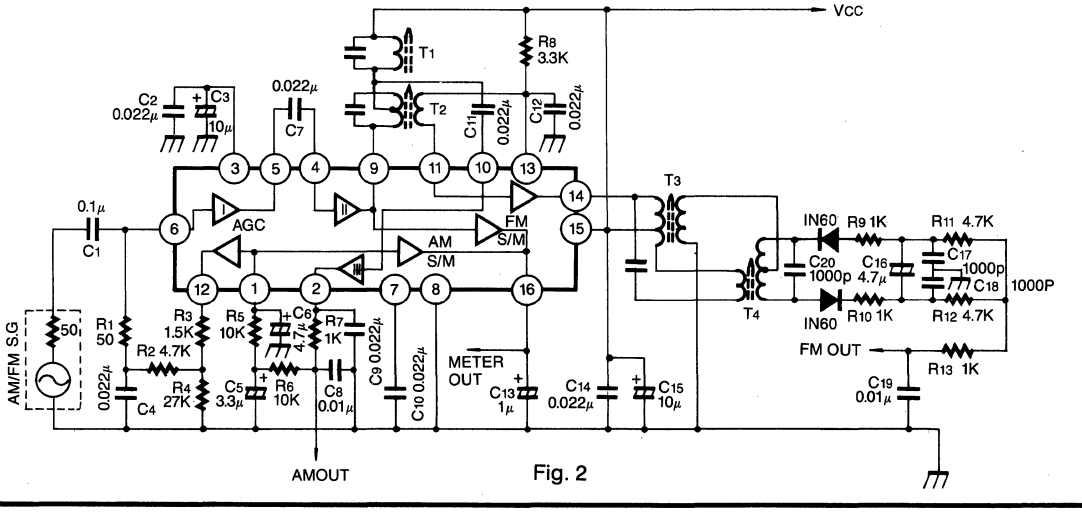


Fig. 2

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 5V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Regulator Output Voltage	Vreg	V_i = 0	2.7	3.0	3.3	V
FM Section (f=10.7MHz, Δf=±22.5KHz, fm=400Hz)						
Quiescent Circuit Current	I_{CC}	V_i = 0		8	10	mA
Input Limiting Sensitivity	V_i (lim)	−3dB Point from V_O (V_i = 80dBμ)		40	46	dBμ
Detector Output	V_O	V_i = 80dBμ	60	90		mV
Total Harmonic Distortion	THD	V_i = 80dBμ		0.2	1.0	%
AM Rejection Ratio	AMR	V_i = 80dBμ, AM: 30% Mod, 1KHz	40	50		dB
Signal to Noise Ratio	S/N	V_i = 80dBμ	60	70		dB
Meter Output Voltage	V_M	V_i = 0dBμ		0		V
		V_i = 80dBμ		0.8		
AM Section (f = 455KHz, fm = 400Hz, 30% Mod)						
Quiescent Circuit Current	I_{CC}	V_i = 0		8	10	mA
Max Sensitivity	V_i (sen)	V_O = 10mV		20	26	dBμ
Detector Output	V_O	V_i = 60dBμ	75	110		mV
Total Harmonic Distortion	THD1	V_i = 60dBμ		0.3	2.0	%
	THD2	V_i = 80dBμ		1.4	3.0	
Signal to Noise Ratio	S/N	V_i = 60dBμ	45	55		dB
Meter Output Voltage	V_M	V_i = 0dBμ		0		V
		V_i = 80dBμ		0.65		

TYPICAL APPLICATION CIRCUIT

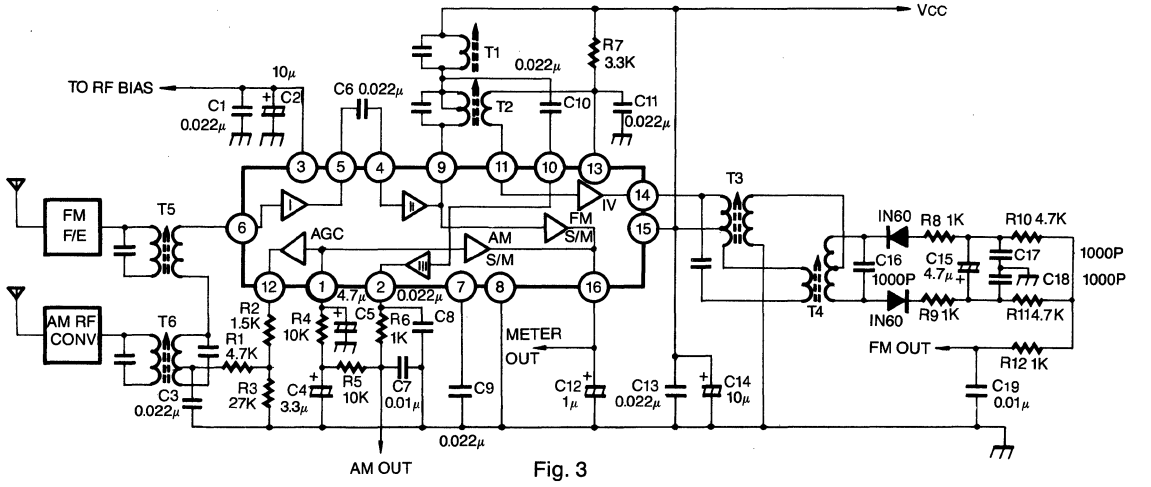
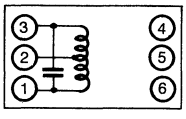


Fig. 3

COIL SPCIFICATION

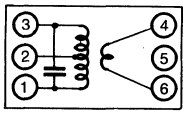
1. T1



C_o (pF)	f (KHz)	Q_o (%)	TURNS		
			6-4	3-2	2-1
180	455	80	33	36	110

Seoul Jupa
SJ-015-472
0.07mmϕ UEW

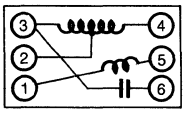
2. T2



C_o (pF)	f (MHz)	Q_o (%)	TURNS		
			1-2	2-3	4-6
50	10.7	90	9	4	2

Seoul Jupa
SJ-015-239
0.1mmϕ UEW

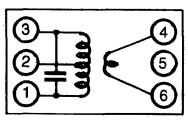
3. T3



C_o (pF)	f (MHz)	Q_o (%)	TURNS		
			4-2	2-3	1-5
50	10.7	100	5½	7	5½

Seoul Jupa
SJ-015-474
0.1mmϕ UEW

4. T4

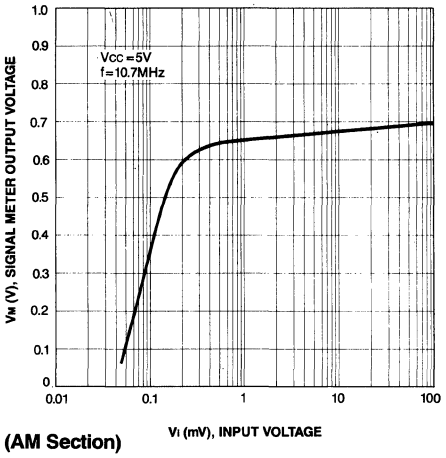


C_o (pF)	f (MHz)	Q_o (%)	TURNS		
			4-6	1-2	2-3
30	10.7	110	1	8	8

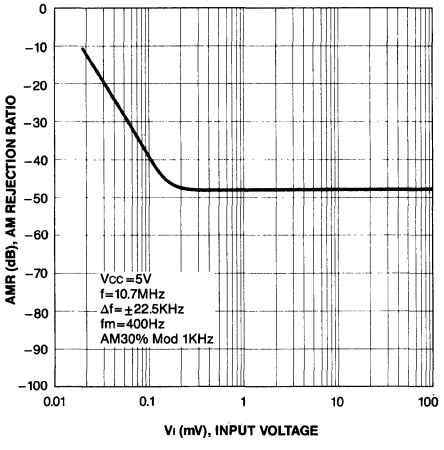
Seoul Jupa
SJ-015-463
0.1mmϕ UEW

(FM Section)

SIGNAL METER OUTPUT VOLTAGE-INPUT VOLTAGE

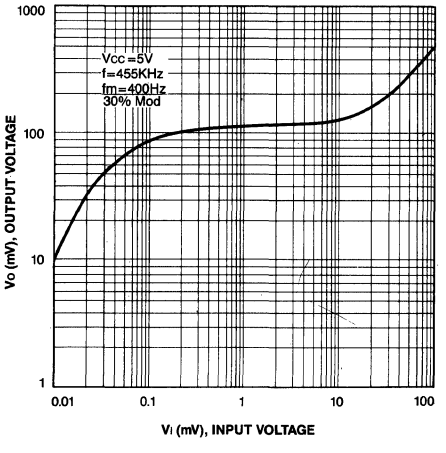


AM REJECTION RATIO-INPUT VOLTAGE

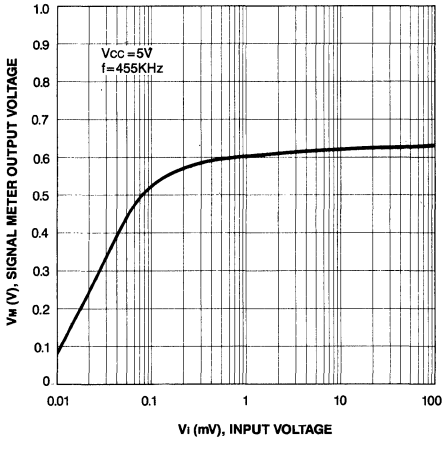


(AM Section)

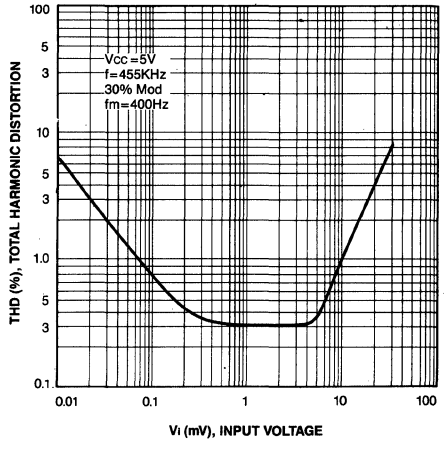
OUTPUT VOLTAGE-INPUT VOLTAGE



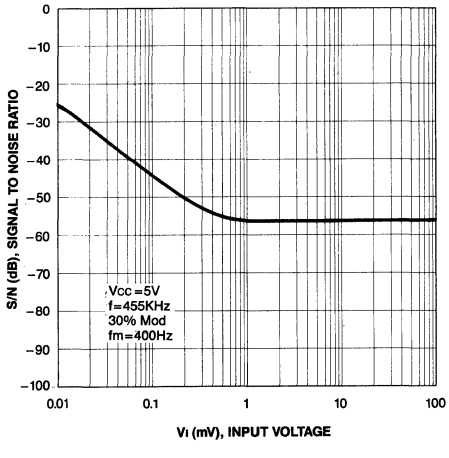
SIGNAL METER OUTPUT VOLTAGE-INPUT VOLTAGE



TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



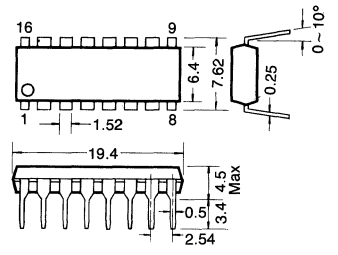
SIGNAL TO NOISE RATIO-INPUT VOLTAGE



AM/FM IF SYSTEM

The KA2243/N is a monolithic integrated circuit developed for the radio cassette tape recorder included AM/FM IF amplifier and detector.

16 Dip Unit: mm



FUNCTIONS

- AM Section
  IF amplifier with AGC detector.
  Signal meter driver circuit.
  Voltage regulator for RF external circuit.
- FM Section
  IF amplifier.
  Quadrature detector.
  Post amplifier.
  Signal meter driver circuit.

FEATURES

- **Suitable for radio cassette and home stereo.**
- **Wide operating supply voltage range. (3.0V ~ 14V).**
- **Low quiescent circuit current.**
- **AM section.**
  Simplified input circuit IFT (Ceramic filter type).
  RF AGC available.
- **FM section.**
  High limiting sensitivity (33dBμ, Typ).
  Low residual noise (−45dB at V_i = −10dBμ).
  Small side peak of detuned output voltage.

TEST CIRCUIT

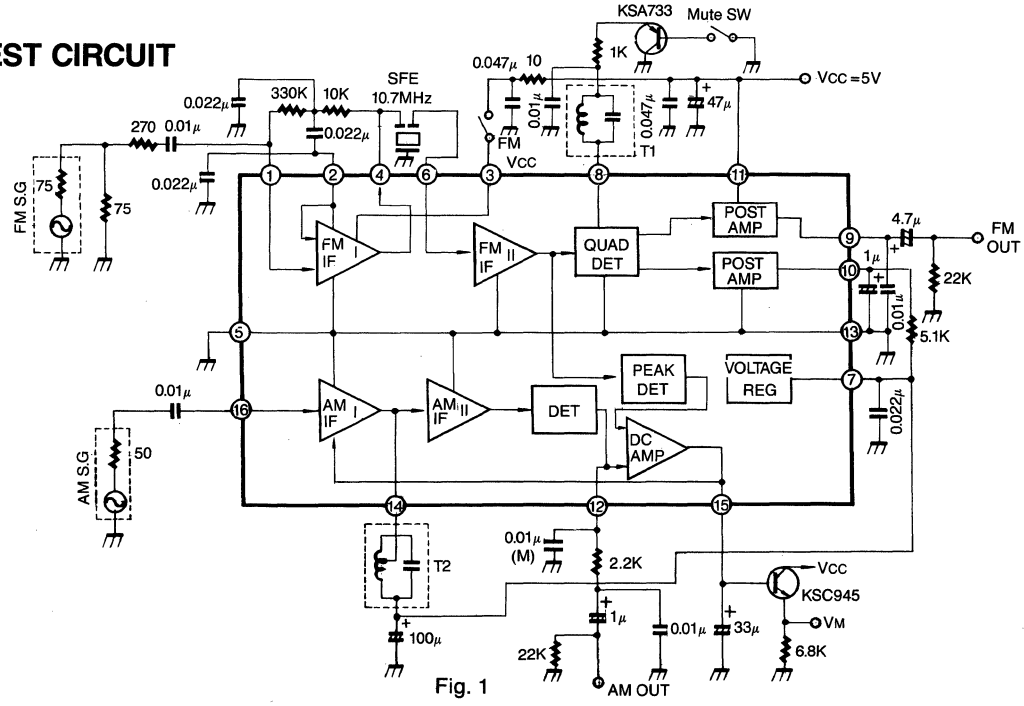


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

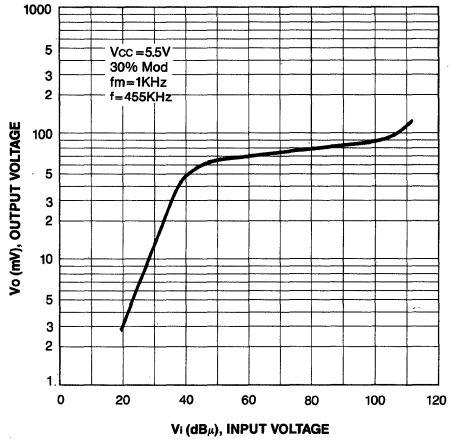
ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 5.5V, unless otherwise specified)

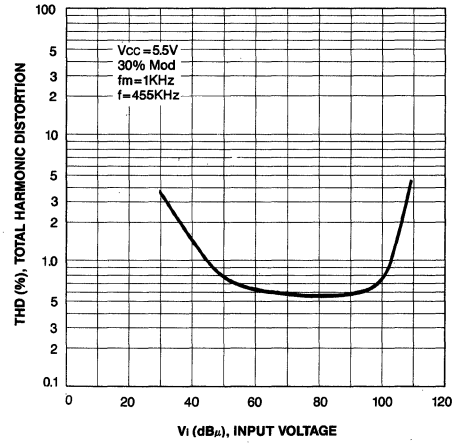
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
FM Section (f = 10.7MHz, fm = 1KHz, Δf = ± 75KHz)						
Quiescent Circuit Current	I_{CC}	V_i = 0	7	11	16.5	mA
Input Limiting Sensitivity	V_i (lim)	V_O (V_i = 100dBμ) − 3dB		33	38	dBμ
Detector Output	V_O	V_i = 100dBμ	180	245	310	mV
Total Harmonic Distortion	THD	V_i = 100dBμ		0.3	1.0	%
AM Rejection Ratio	AMR	V_i = 100dBμ	50	60		dB
Signal to Noise Ratio	S/N	V_i = 100dBμ	72	83		dB
Signal Meter Output	V_M	V_i = 100dBμ	1.05	1.5	2.05	V
Residual Noise	V_N	V_O (AF) (V_i = 100dBμ) :V_O (AF) (V_i = −10dBμ)		45		dB
Muting Attenuation	M (att)	V_i = 37dBμ, Mute SW on		35		dB
AM Section (f=455KHz, fm=1KHz, 30% Mod)						
Quiescent Circuit Current	I_{CC}	V_i = 0		8		mA
Maximum Sensitivity	V_i (sen)	V_O (AF) = 10mV		29		dBμ
Dector Output	V_O	V_i = 74dBμ	45	65	85	mV
Total Harmonic Distortion	THD	V_i = 74dBμ		0.3	2.0	%
		V_i = 100dBμ		0.7	3.5	%
Signal to Noise Ratio	S/N	V_i = 74dBμ	45	55		dBμ
Signal Meter Output	V_M	V_i = 100dBμ	1.2	1.4	1.6	V
Input Impedance (Pin 16)	R_i	Pin 16 0.8 − 0.9V_{DC}	1.45	2.12	2.8	KΩ

(AM Section)

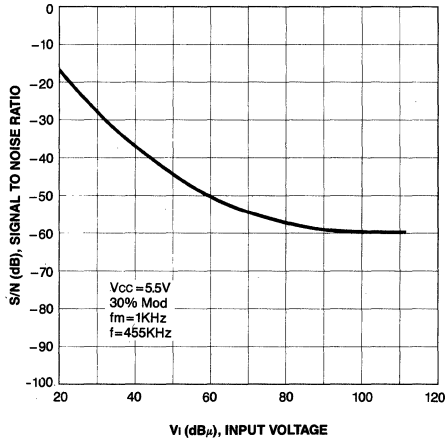
OUTPUT VOLTAGE-INPUT VOLTAGE



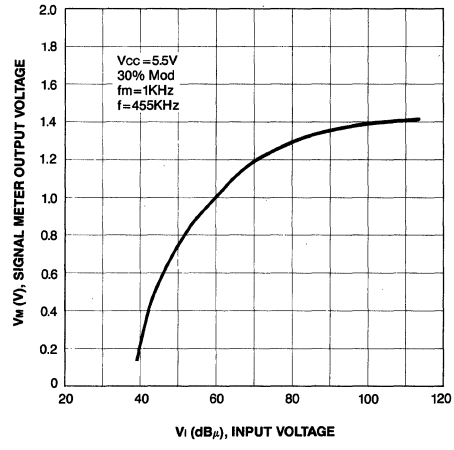
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



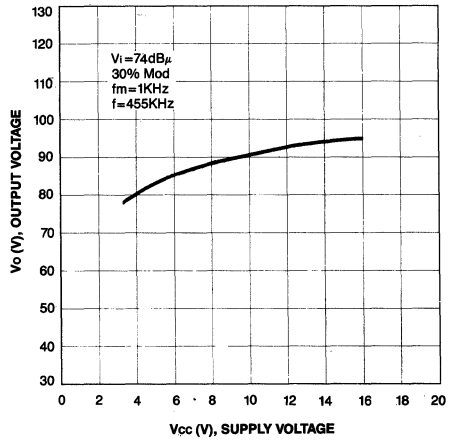
SIGNAL TO NOISE RATIO-INPUT VOLTAGE



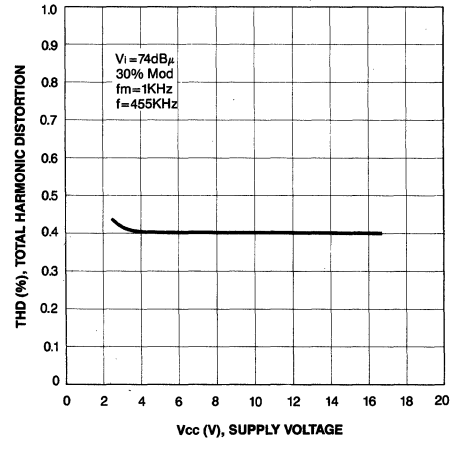
SIGNAL METER OUTPUT VOLTAGE-INPUT VOLTAGE



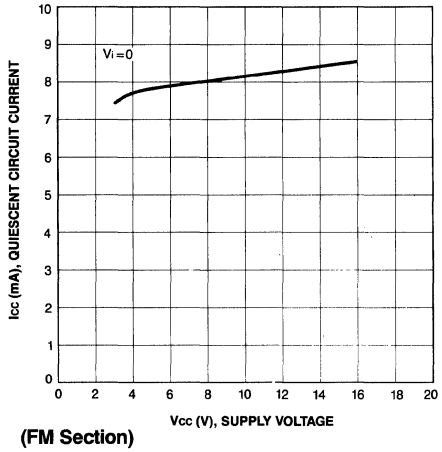
OUTPUT VOLTAGE-SUPPLY VOLTAGE



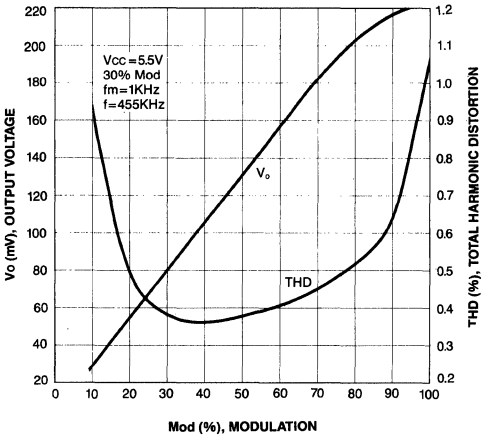
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE

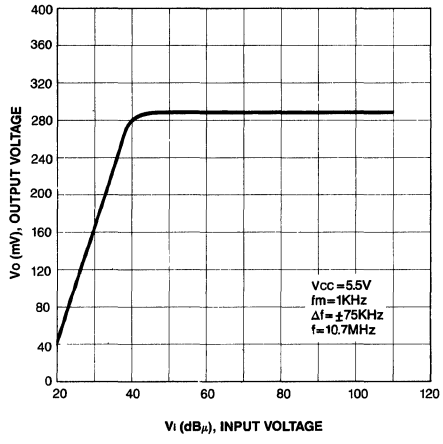


OUTPUT VOLTAGE — MODULATION
TOTAL HARMONIC DISTORTION

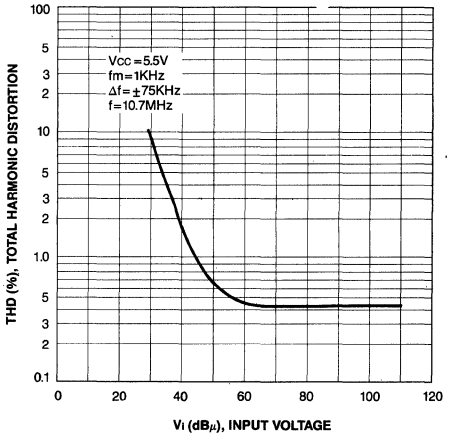


(FM Section)

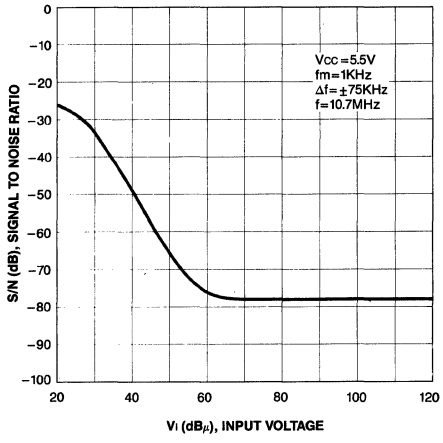
OUTPUT VOLTAGE-INPUT VOLTAGE



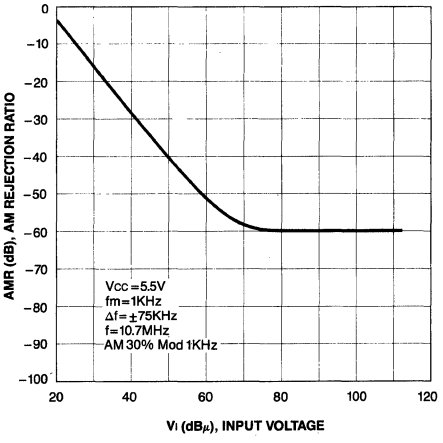
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



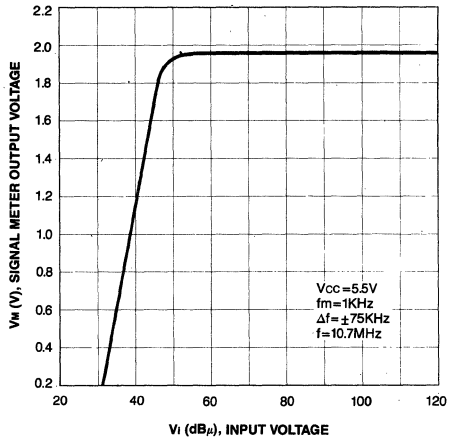
SIGNAL TO NOISE RATIO-INPUT VOLTAGE



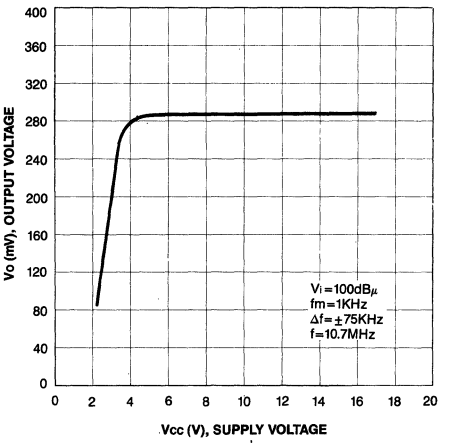
AM REJECTION RATIO-INPUT VOLTAGE



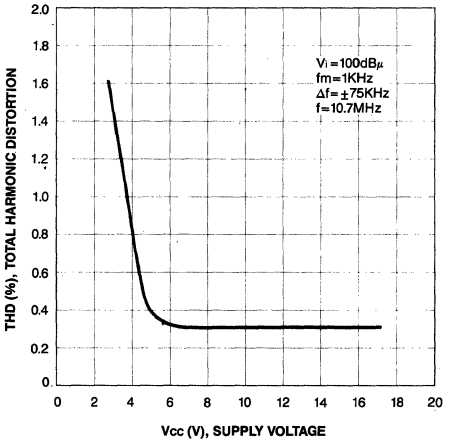
SIGNAL METER OUTPUT VOLTAGE-INPUT VOLTAGE



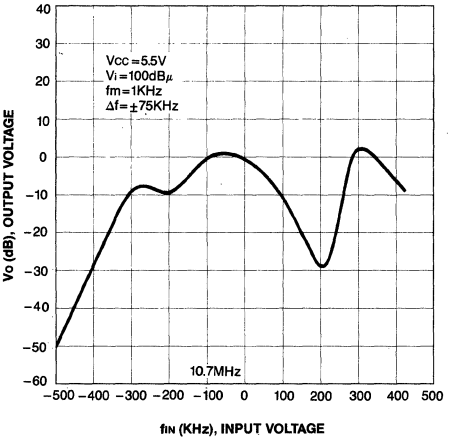
OUTPUT VOLTAGE-SUPPLY VOLTAGE



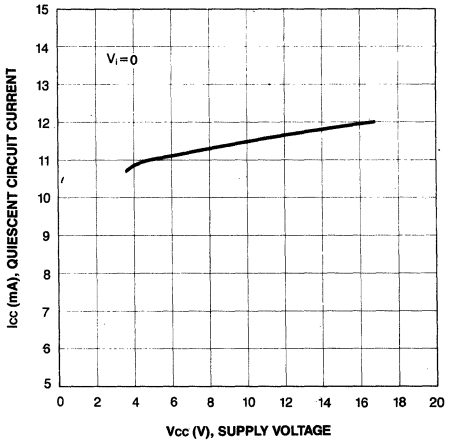
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



OUTPUT VOLTAGE-INPUT FREQUENCY



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



TYPICAL APPLICATION CIRCUIT

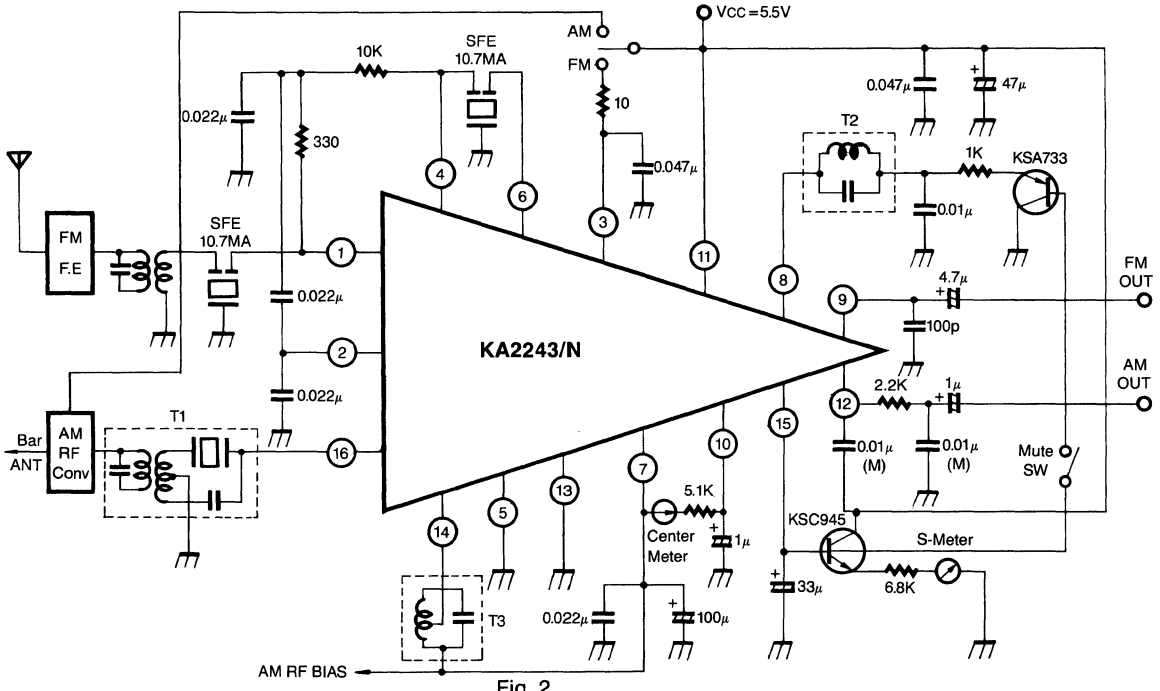
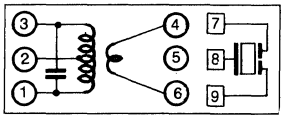


Fig. 2

COIL SPECIFICATION

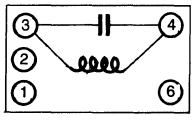
1. T1



C_o (pF)	f (KHz)	Q_o (%)	TURNS		
			4-6	3-2	2-1
180	455	105	6	93	55

Seoul Jupa
SJ-015-552
0.06mmϕ UEW

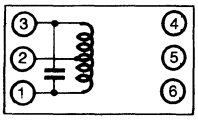
2. T2



C_o (pF)	f (MHz)	Q_o (%)	TURNS		
			3-4		
82	10.7	65	9		

Seoul Jupa
SJ-59JG-043
0.07mmϕ UEW

3. T3



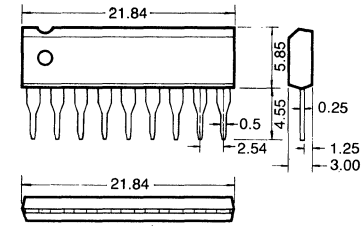
C_o (pF)	f (KHz)	Q_o (%)	TURNS		
			1-2	2-3	
180	455	120	51	92	

Seoul Jupa
SJ-015-521
0.07mmϕ UEW

FM IF AMPLIFIER

The KA2244 is a monolithic integrated circuit consisting of FM IF amplifier, detector, muting circuit and signal meter driver. It is suitable for car radio.

9 Sip Unit: mm



FUNCTIONS

- 3 stage IF amplifiers.
- Peak detector.
- Muting circuit.
- Signal meter driving circuit.

FEATURES

- **Suitable for FM car radio.**
- **Wide operating supply voltage range (8V ~ 16V).**
- **High recorved output voltage (V_o=500mV typ).**
- **Variable muting level.**
- **Muting off by pin 4 open.**
- **Simplified single coil tuning.**
- **Low distortion (THD=0.1%; Typ).**
- **Minimum number of external parts required.**

TYPICAL APPLICATION CIRCUIT

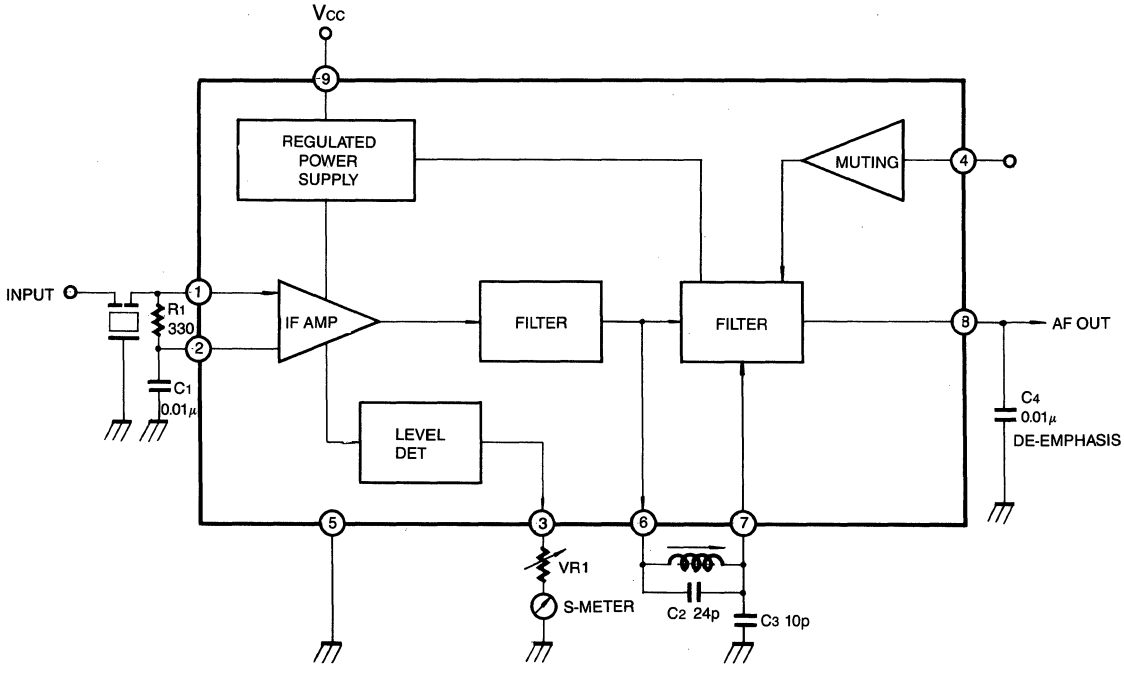


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Input Voltage	V_i	0.7	Vrms
Power Dissipation	P_d	500	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 12V, f = 10.7MHz, fm = 400Hz)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	V_i=0	10	14	18	mA
Input Limiting Sensitivity		V_i (lim)	−3dB point from V_O (V_i=80dBμ, Δf=±75KHz)		50	55	dBμ
AM Rejection Ratio		AMR	FM: Δf=±75KHz dev AM: 30% Mod, fm=1KHz V_i=80dBμ		50		dB
Detector Output Voltage		V_O	Δf=±75KHz dev V_i=80dBμ	300	500	700	mV
Total Harmonic Distortion		THD	Δf=±22.5KHz dev V_i=80dBμ		0.1		%
Signal to Noise Ratio		S/N	Δf=±75KHz dev V_i=80dBμ		75		dB
Muting Attenuation		M (att)	Δf=±75KHz dev V_i=80dBμ		70		dB
Meter Driver Voltage		V_3 (max)	V_i=110dBμ		4.0		V
Input Impedance	Resistance	Rip	f=10.7MHz 1 PIN-GND		5		KΩ
	Capacitance	Cip			4.5		pF
Output Impedance	Resistance	Rop	f=10.7MHz 6 PIN-GND		1.3		KΩ
	Capacitance	Cop			4		pF
Output Resistance		R_O	f=400Hz 8 PIN-GND		7.7		KΩ

TEST CIRCUIT

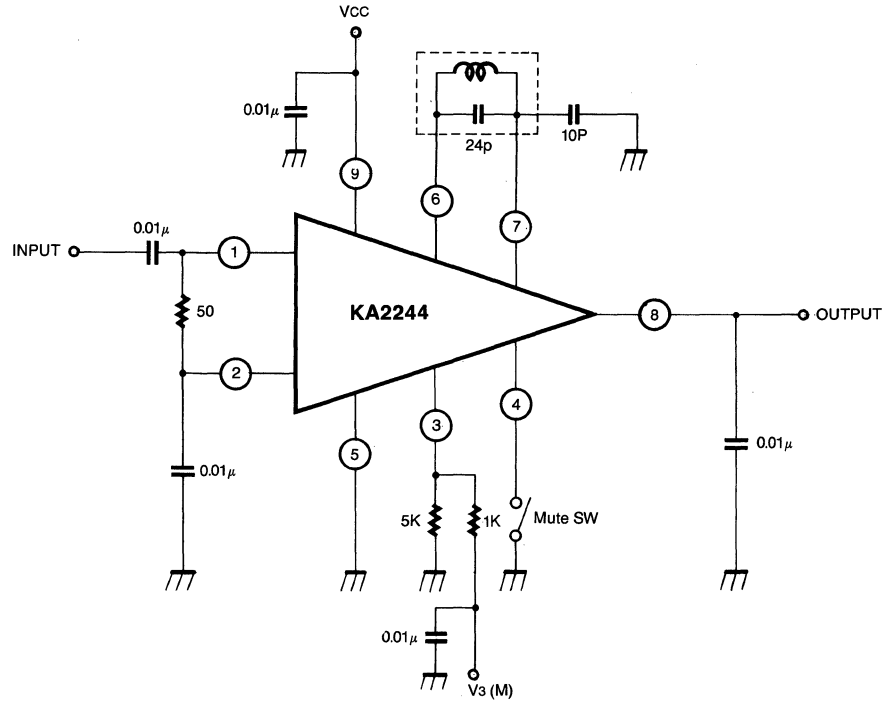
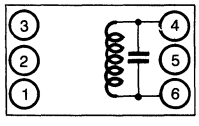


Fig. 2

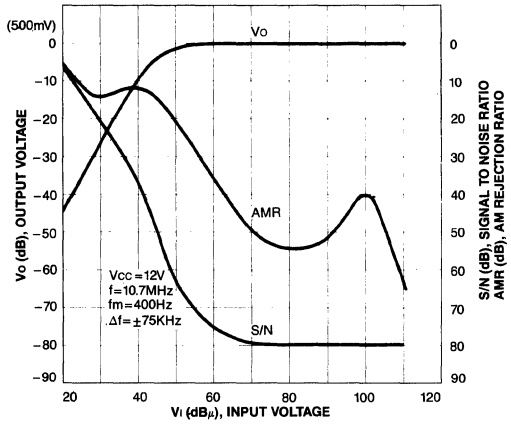
COIL SPECIFICATION



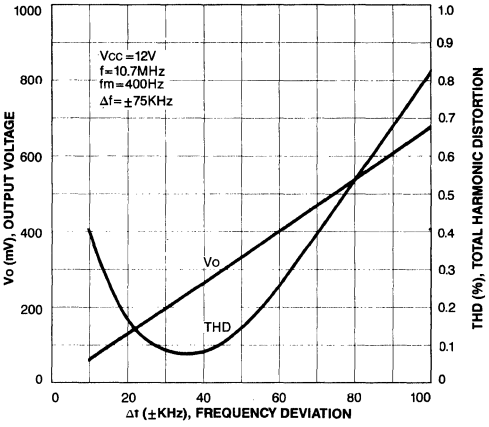
C_O (pF)	f (MHz)	Q_O (%)	TURNS		
			4-6		
27	10.7	150	18		

Seoul Jupa SJ-59JG-045 0.1mmϕ UEW

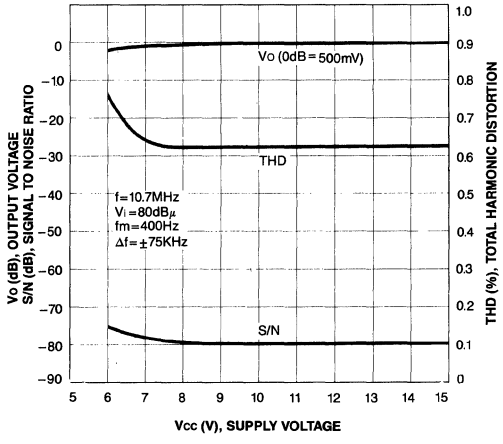
OUTPUT VOLTAGE
SIGNAL TO NOISE RATIO — INPUT VOLTAGE
AM REJECTION RATIO



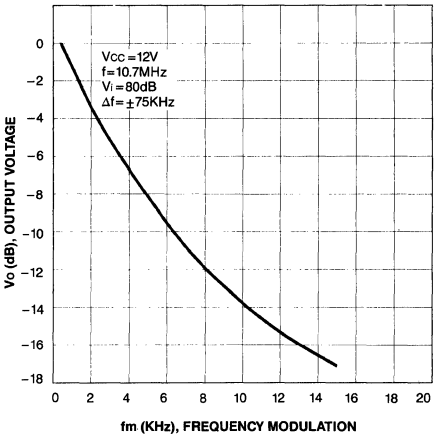
OUTPUT VOLTAGE , TOTAL HARMONIC DISTORTION
—FREQUENCY DEVIATION



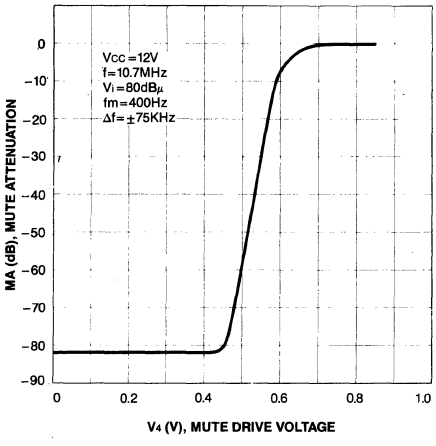
OUTPUT VOLTAGE
TOTAL HARMONIC DISTORTION —SUPPLY VOLTAGE
SIGNAL TO NOISE RATIO



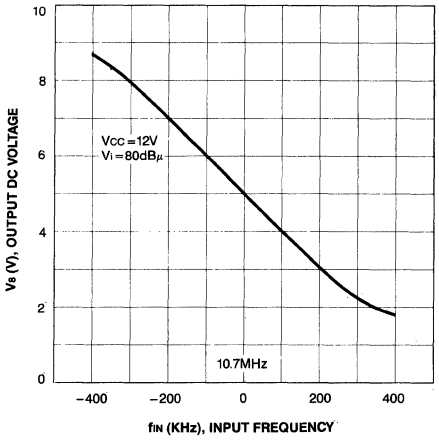
OUTPUT VOLTAGE-FREQUENCY MODULATION



MUTE ATTENUATION-MUTE DRIVE VOLTAGE



OUTPUT DC VOLTAGE-INPUT FREQUENCY

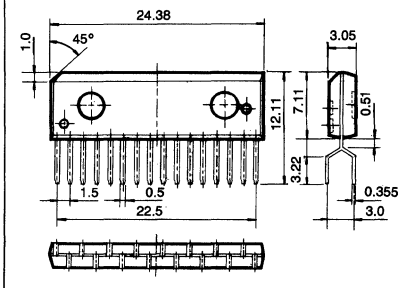


FM IF FOR CAR STEREO

The KA22441 is a monolithic integrated circuit consisting of FM IF amplifier, suitable for use in car stereo and music centers.

It features practically all of the functions for use a FM tuner, including AGC output, AFC output, level meter output in a single package.

16 ZIP



FUNCTIONS

- FM IF amplifier.
- Quadrature detector.
- AFC output.
- AGC output.
- Level meter output.
- Muting for weak signal.
- Muting for detuned condition.

FEATURES

- **Soft muting function.**
- **Variable muting maximum attenuation.**
- **Variable muting attack input signal.**
- **Variable muting slope with respect to input signal level.**
- **Level meter output.**
- **AFC output.**
- **AGC output.**
- **High sensitivity (V_i (lim)=25dBμ: Typ).**
- **High output level.**
- **Good S/N ratio (78dB: Typ).**
- **Low distortion (0.05%: Typ).**
- **Wide operating supply voltage range (6V ~ 14V).**

BLOCK DIAGRAM

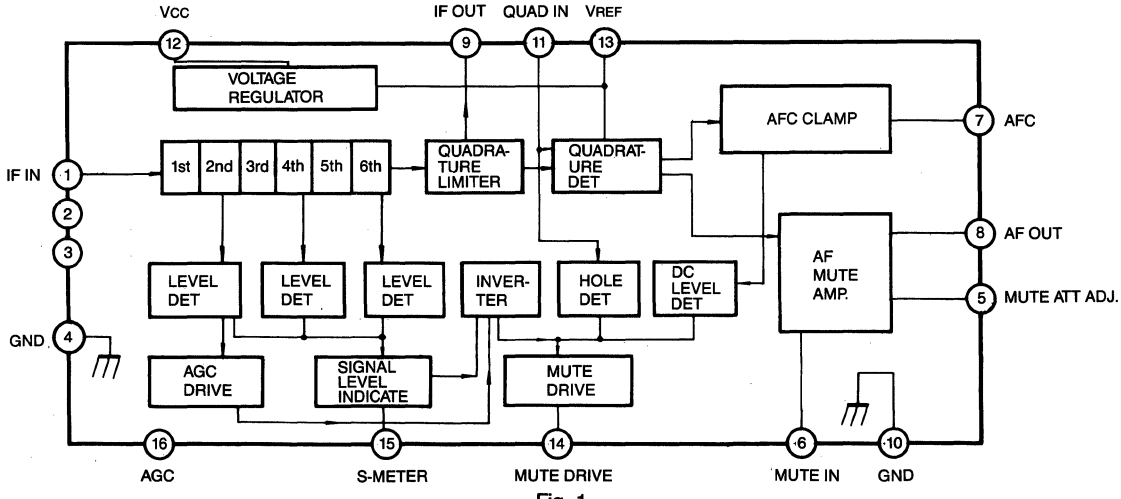


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	Pd	640	mW
Operating Temperature	Topr	−20 ~ +75	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =8V, f=±75KHz, V_i =100dBμ, fm=400Hz)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		6	8	14	V
Circuit Current	I_{CC}	V_i =0	15	21	27	mA
Input Limiting Sensitivity	V_i (lim)	V_O (V_i =100dBμ) −3dB		25	29	dBμ
Detector Output Level	V_O		200	260	320	mV
Total Harmonic Distortion	THD			0.05	0.2	%
Signal to Noise Ratio	S/N		70	78		dB
AM Rejection Ratio	AMR		50	63		dB
Signal Meter Output Level	V_M	V_i =0	0	0.1	0.3	V
		V_i =100dBμ	4.5	5.3	6.0	
AGC Output Level	$V_{(AGC)}$	V_i =0	3.5	4.1	4.5	V
		V_i =100dBμ	0	0.02	0.3	
Muting Sensitivity	M (sen)	V_{14} =2V	22	26	32	dBμ
Muting Attenuation	$M_{(att)}$	V_6 =2V	10	15	20	dB
		V_6 =5V	24	28	32	
Muting Bandwidth	$M_{(BW)}$	V_{14} = 2V	140	210	370	KHz

TEST CIRCUIT

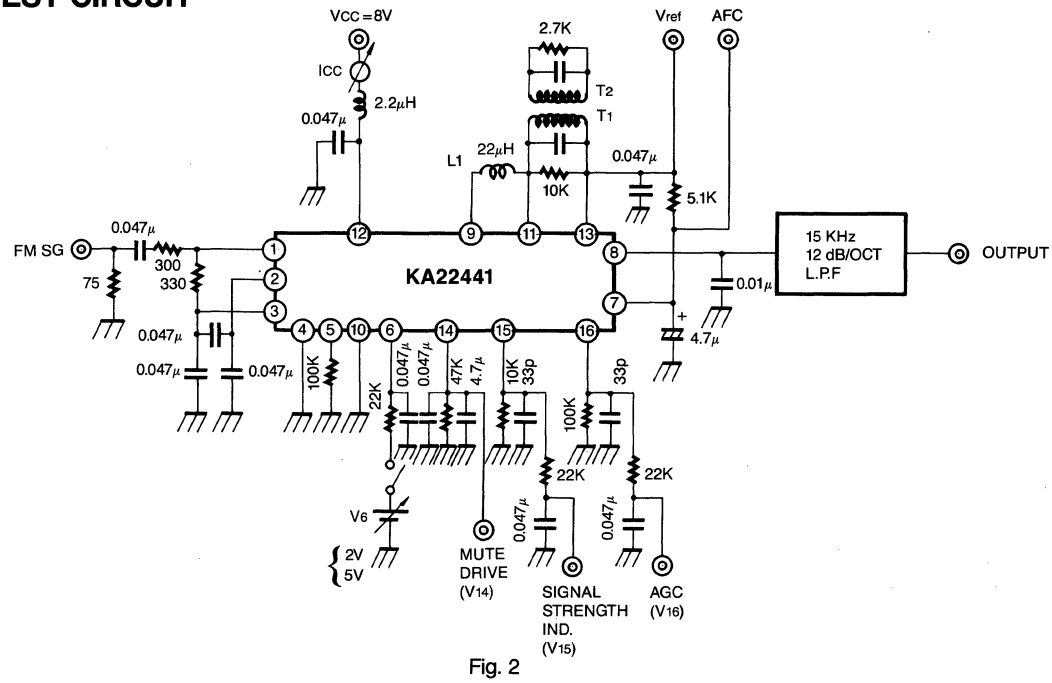


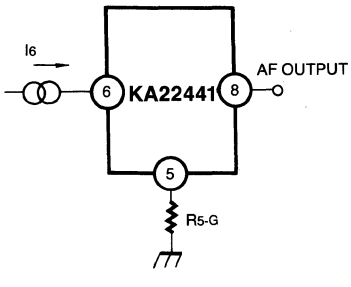
Fig. 2

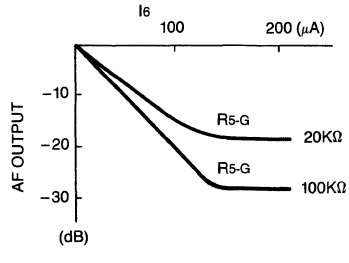
ON MUTING CHARACTERISTIC

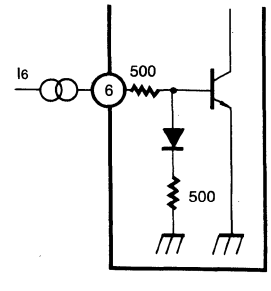
The muting operation in the KA22441 is performed by an AF pre-amplifier, the gain of which varies continuously with control current, and a muting drive circuit which supplies the control current.

The gain of the AF preamplifier decreases with the increased gain control current applied to the pin 6. However, the gain does not decrease further when the control current reaches approximately 120μA or higher. The lower limit of the gain under this condition depends upon a resistor connected between the pin 5 and GND, and the higher the resistance the lower the gain (the higher the attenuation).

Thus the maximum muting attenuation will be set by connecting the resistor between the pin 5 and GND.







Since the muting control input pin 6 is connected to the base of the emitter-grounded transistor (through a protection resistor of 500Ω in series), the voltage between pin 6 and GND is about 0.6V when the control current is applied.

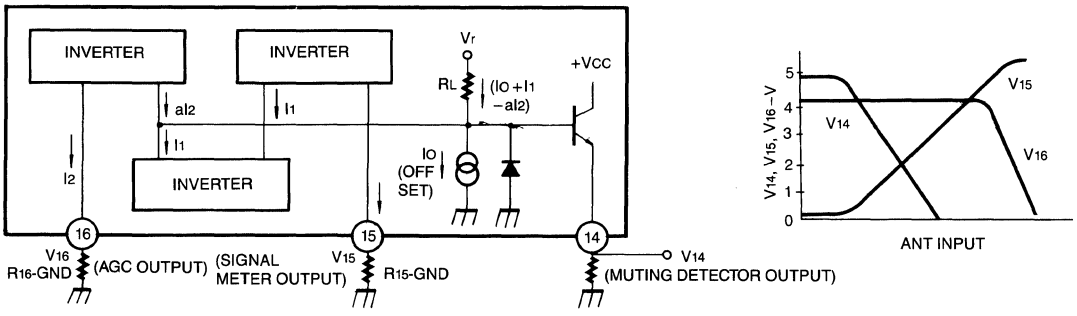
In actuality, the muting operation is accomplished by applying a voltage drive type muting drive output (pin 14) to the pin 6 through a high resistance (to 20KΩ).

The muting drive output is composed of three output devices:

1) Hole detector output which develops a voltage when C/N (carrier-to-noise ratio) lowers under weak signal input conditions.
2) A reversed output of the signal strength indicating output (output at pin 15)
3) A bandwidth limited muting drive output which develops a voltage when the AFC output becomes higher than $\pm V_{BE}$ during tuning-off operation.

All these outputs are led to an OR circuit and the processed output is developed at pin 14. Of the above muting drive outputs, descriptions on the hole detector output and the bandwidth limited muting drive output will be omitted, since they are the same as those used in conventional quadrature detector ICs.

The inverted output of the signal strength indication output is obtained as illustrated below.



By referring to the illustration, V_{14} is given by the formula: $V_{14} = V_r - (I_O + I_1 - aI_2) R_L - V_{BE}$.

Conditions are: $V_r = 4.9V$, $I_0 \cong 0.2mA$, $a \cong 2$, $R_L = 22K\Omega$, $V_{BE} \cong 0.6V$, $I_1 = V_{15}/R_{15}$-G, $I_2 = V_{16}/R_{16}$-G, where V_{16} is a constant equ al to 4.1V (typ.) for medium or lower signal input levels, where the muting drive output is required. Since the V_{15} increases proportionally to the increase of the input signal strength, I_1 will also increase. Therefore the V_{14} will decrease with the increased signal strength. Thus the required muting drive output can be obtained by selecting proper values of R_{15}-G and R_{16}-G.

For example, the muting drive output moves toward strong input signal level if the R_{16}-G is decreased, or the muting drive output becomes zero due to the offset current I_0 under a weak signal input condition, if the R_{16}-G is increased to infinity (namely pin 16 is opened). However the muting drive output caused by a hole detector still exists in this case. Increasing R_{15}-G makes the slope of the curve for the muting drive output vs. antenna signal input decrease, or decreasing the R_{15}-G increases the slope of the curve. Furthermore, varying the value of a resistor connected between the muting drive output (pin 14) and the muting control input (pin 6) changes the value of the muting control current required to obtain the same muting drive output, accordingly a slope of curve for muting attenuation vs. antenna signal input level is also changed. These characteristics investigated by using an actual receiver are shown on the curves below.

The general method to adjust the muting circuit of the KA22441 is: to set the signal input level required to actuate the muting circuit with the R_{16}-G, to adjust the slope of the curve for the muting attenuation vs. antenna signal input with the R_{15}-G, and the adjust the maximum muting attenuation (determined by setting the noise level at no signal). The slope of the curve for the muting attenuation vs. antenna signal input level can also be adjusted by the resistor connected between the pins 14 and 6 in addition to R_{15}-G, however, selecting a resistor too high does not allow the muting control current flowing into pin 6 to reach 120μA even though the maximum muting drive output (V_{14}) is applied, namely the muting attenuation does not reach its maximum value. Accordingly a recommended value of the resistor between pins 14 and 6 in about 22KΩ.

APPLICATION CIRCUIT

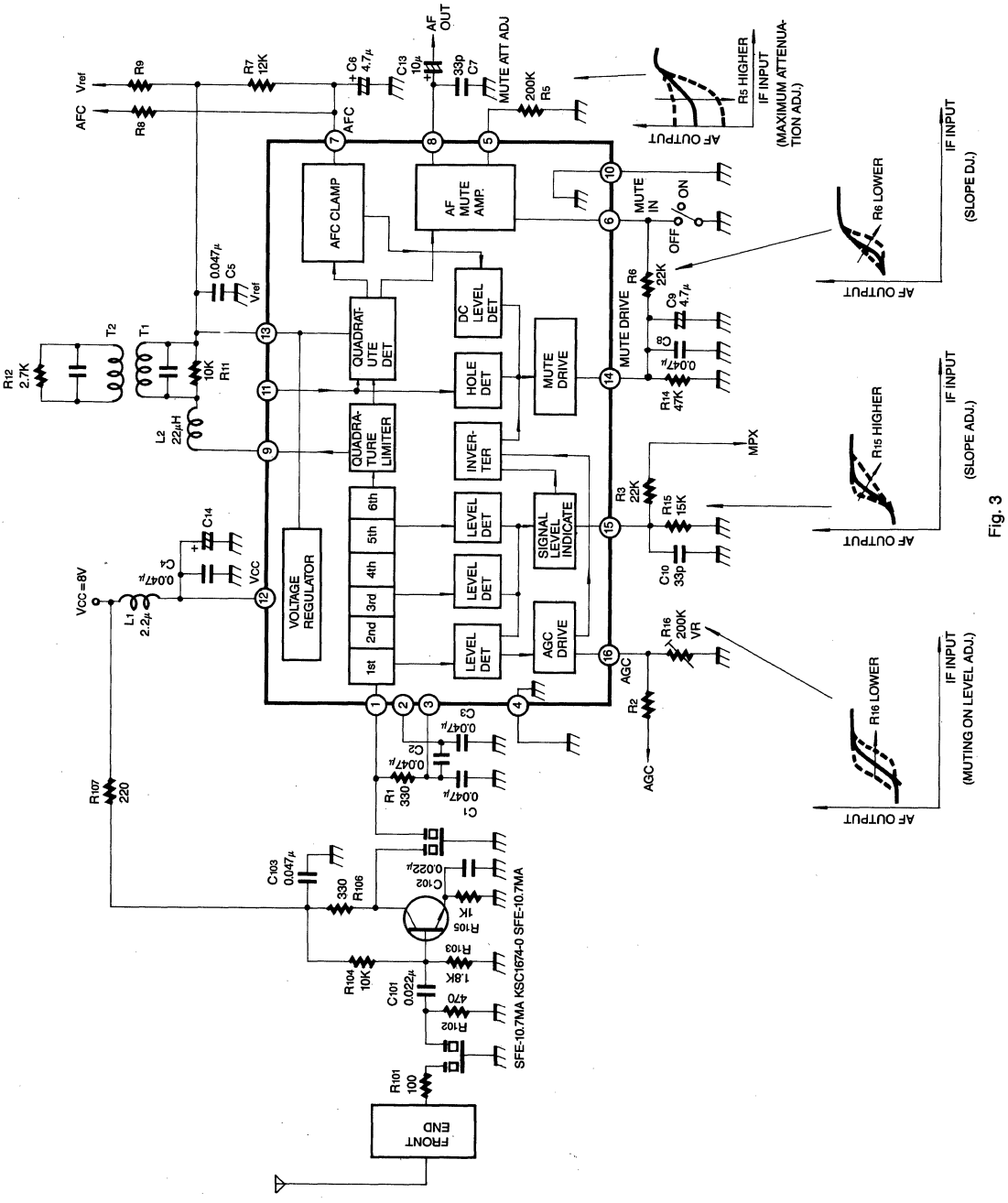
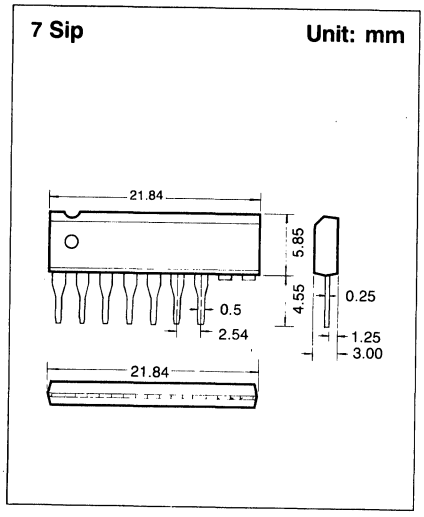


Fig. 3

FM IF AMPLIFIER

The KA2245 is a monolithic integrated circuit consisting of FM IF amplifier, detector.
It is suitable for car radio.



FUNCTIONS

- 3 stage IF amplifiers.
- Peak detector.

FEATURES

- **Suitable for FM car radio.**
- **Wide operating supply voltage range (8V ~ 15V).**
- **High recorved output voltage (V_o =500mV typ).**
- **Excellent AM rejection: AMR=50dB (typ).**
- **High sensitivity: V_i (lim)=50dBμV (typ).**
- **Simplified single coil tuning.**
- **Low distortion (THD=0.1%: typ).**
- **Minimum number of external parts required.**

BLOCK DIAGRAM

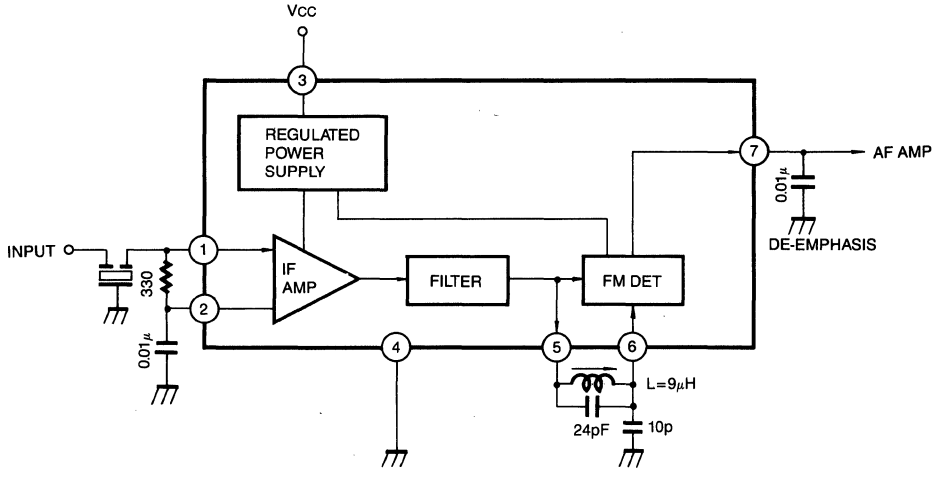


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

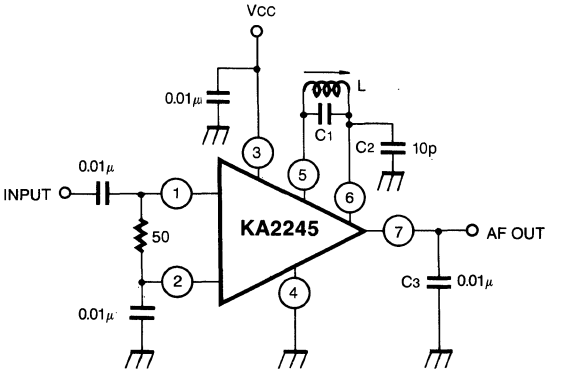
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Inut Voltage	V_i	0.7	V_{RMS}
Power Dissipation	P_d	500	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

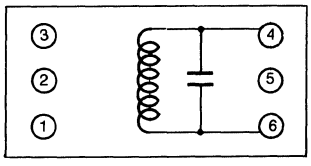
(T_a = 25°C, V_{CC} = 12V, f = 10.7MHz, fm = 400Hz)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	V_i = 0	8	12	14	mA
Input Limiting Sensitivity		V_i (lim)	−3dB point from V_O V_i = 80dBμ, Δf = ±75KHz		50	55	dBμ
AM-Rejection Ratio		AMR	FM: Δf = ±75KHz dev AM: 30% Mod V_i = 80dBμ		50		dB
Detector Output Voltage		V_O	Δf = ±75KHz dev V_i = 80dBμV	300	500	700	mV
Total Harmonic Distortion		THD	Δf = ±22.5KHz dev V_i = 80dBμV		0.1		%
Signal to Noise Ratio		S/N	Δf = ±75KHz dev V_i = 80dBμV		60		dB
Input Impedance	Resistance	R_P	f = 10.7MHz 1PIN-GND		5		KΩ
	Capacitance	C_{iP}			4.5		pF
Output Impedance	Resistance	R_{OP}	f = 10.7MHz 5 PIN-GND		1.3		KΩ
	Capacitance	C_{OP}			4		pF
Output Resistance		R_O	f = 400Hz 7 PIN-GND		7.7		KΩ

TEST CIRCUIT



COIL SPECIFICATION



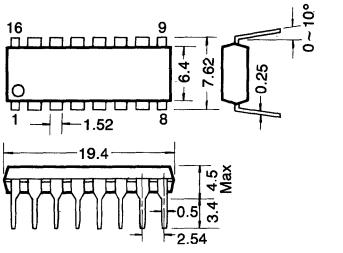
C_O (pF)	f (MHz)	Q_O (%)	TURNS		
			4-6		
27	10.7	150	18		

Seoul Jupa SJ-59 JG-045 0.1mmϕ UEW

AM TUNER SYSTEM

The KA2246 is a monolithic integrated circuit designed for high class receiver, which has all functions of AM tuner.

16 Dip Unit: mm



FUNCTIONS

- RF amplifier
- Mixer
- IF amplifier
- Detector
- AGC
- Signal meter driving circuit

FEATURES

- **Suitable for Hi-Fi AM tuner.**
- **High AGC figure of merit (75dB, Typ).**
- **Good usable sensitivity (20dBμ, Typ).**
- **Low distortion**
  THD=0.4% (Typ) at V_i=100dBμ, 30% modulation.
  THD=0.8% (Typ) at V_i=74dBμ, 90% modulation.
- **Good signal meter output characteristic.**

TYPICAL APPLICATION CIRCUIT

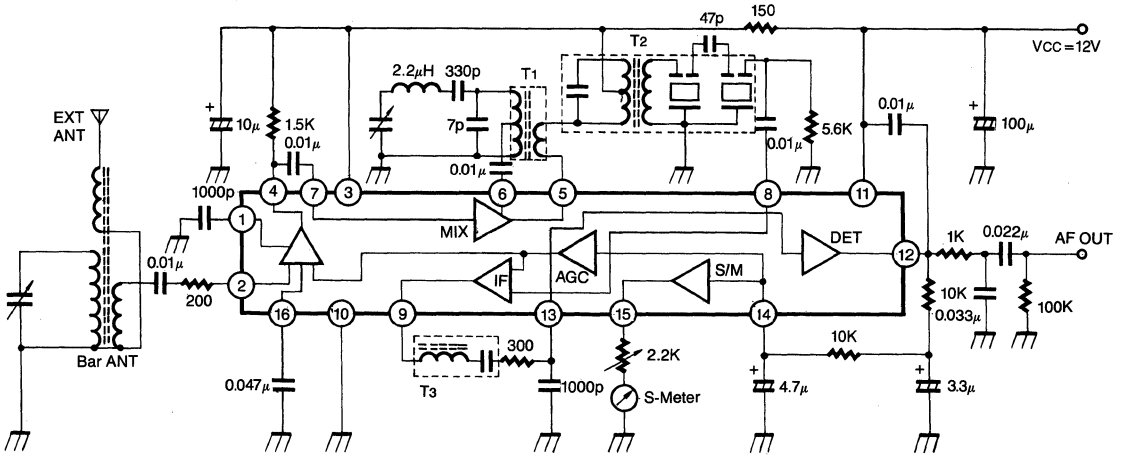


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

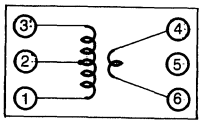
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_d	450	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12V, f = 1MHz, fm = 400Hz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		14.5	25	mA
Detector Output Voltage	V_O	V_i =74dBμ, 30% Mod	150	212	300	mV
Signal to Noise Ratio	S/N	V_i =74dBμ, 30% Mod	47	53		dB
		V_i =34dBμ, 30% Mod	29	33.5		dB
Total Harmonic Distortion	THD	V_i = 74dBμ, 90% Mod		0.8		%
		V_i =100dBμ, 30%		0.4	1.0	%
AGC		− 10dB point from output voltage with V_i =100dBμ	65	75		dB
Signal Meter Current	I_M	V_i =100dBμ, 30% Mod		240		μA

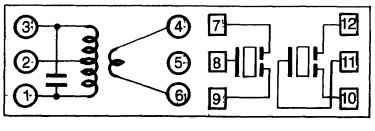
1. T1



C_o (pF)	f (MHz)	Q_o (%)	TURNS		
			4-6	1-2	2-3
	1.4	80	7	3	55

Seoul Jupa
SJ-015-150
0.08mmϕ UEW

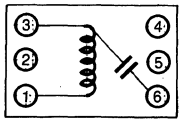
2. T2



C_o (pF)	f (KHz)	Q_o (%)	TURNS		
			4-6	1-2	2-3
180	455	105	6	55	93

Seoul Jupa
SJ-032-212B
0.07mmϕ UEW

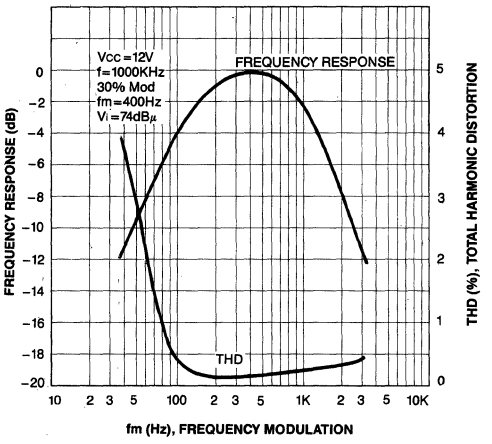
3. T3



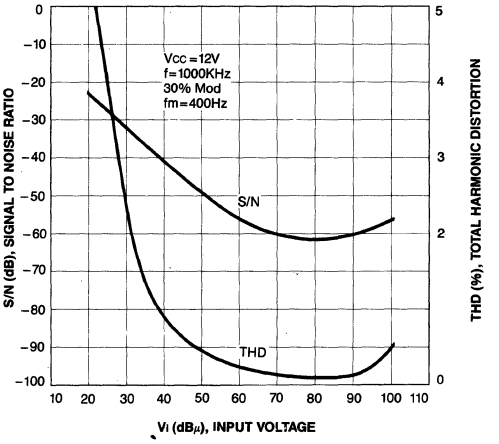
C_o (pF)	f (KHz)	Q_o (%)	TURNS		
			1-3		
8	455	120	140		

Seoul Jupa
SJ-59JG-042
0.07mmϕ UEW

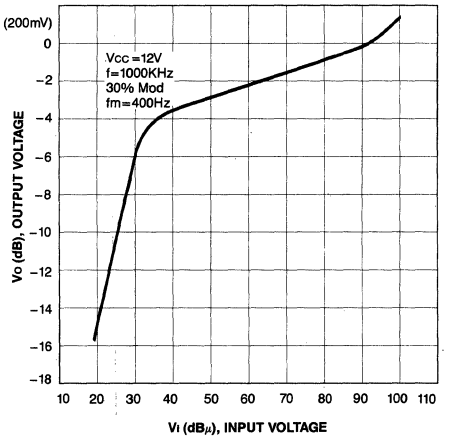
FREQUENCY RESPONSE
TOTAL HARMONIC DISTORTION-
FREQUENCY MODULATION



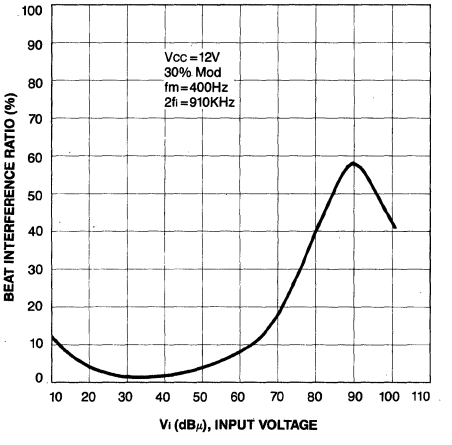
TOTAL HARMONIC DISTORTION
SIGNAL TO NOISE RATIO —INPUT VOLTAGE



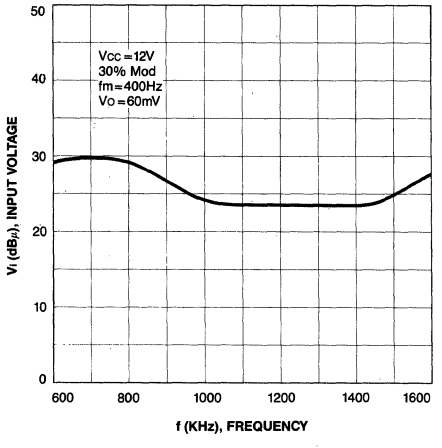
OUTPUT VOLTAGE-INPUT VOLTAGE



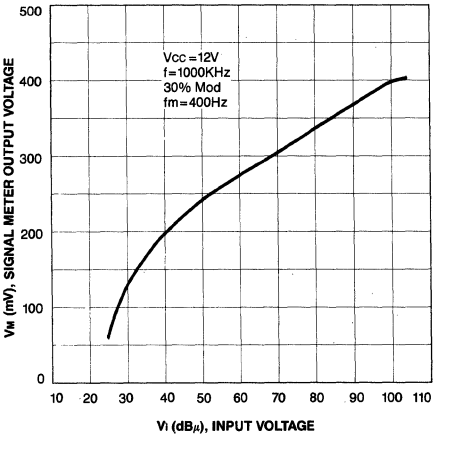
BEAT INTERFERENCE RATIO-INPUT VOLTAGE



INPUT VOLTAGE-FREQUENCY



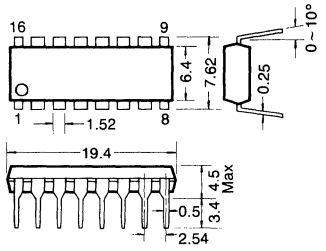
SIGNAL METER OUTPUT VOLTAGE-INPUT VOLTAGE



FM IF/AM TUNER SYSTEM

The KA2247 is a monolithic integrated circuit developed for the radio cassette tape recorder.

16 Dip Unit: mm



FUNCTIONS

- AM SECTION: RF amplifier, Mixer, OSC with ALC IF amplifier, Detector, AGC, Tuning indicator.
- FM SECTION: IF amplifier, Quadrature detector, AF preamplifier, Tuning indicator.

FEATURES

- **Minimum number of external parts required.**
- **Very good S/N: FM (81dB), AM (53dB).**
- **AM oscillator circuit with ALC: Oscillation output voltage of pin 16.**
  MW 130mV
  SW 70mV ~ 90mV
  (7MHz) ~ (24MHz)
- **Excellent AM whistle performance: Whistle 1% at V_i = 100dB.**
- **Built in tuning indicator.**
- **Built in AM/FM function switch.**
- **Operating voltage range: V_{CC} = 3V ~ 8V.**

BLOCK DIAGRAM

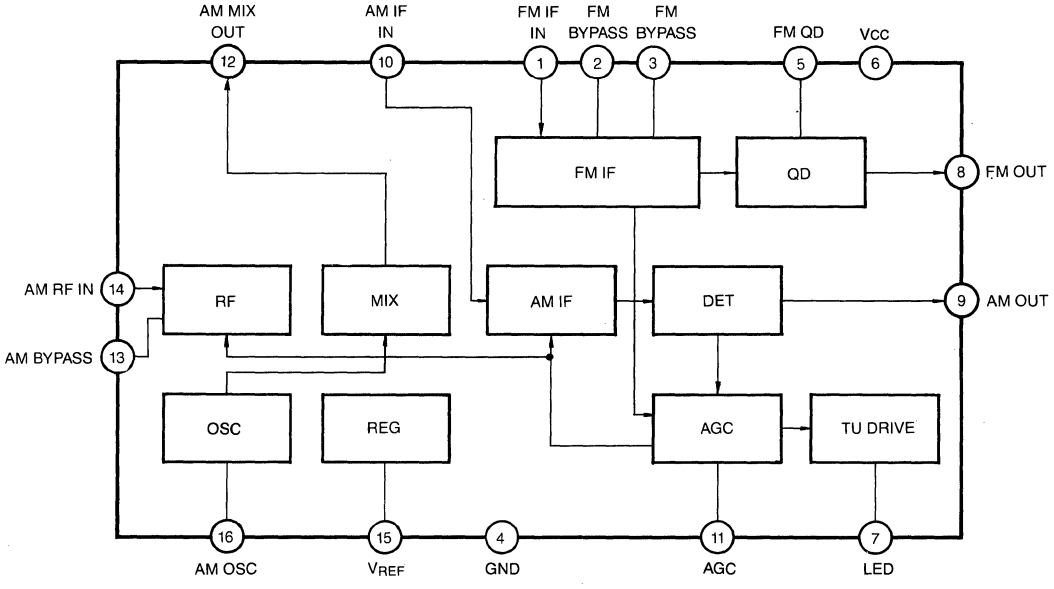


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Circuit Current	I_{CC}	30	mA
Input Current (pin 7)	I_7	20	mA
Output Current (pin 15)	I_{15}	0.1	mA
Power Dissipation	P_D	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=4.5V)

FM Section (f=10.7MHz, Δf=±75KHz, fm=400Hz)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		8.5	12.0	mA
Input Limiting	V_i (lim)	V_O (V_i=80dBμ) −3dB		35	42	dBμ
Detector Output	V_O	V_i=80dBμ	183	260	367	mV
Total Harmonic Distortion	THD 1	V_i=80dBμ		0.55	1.2	%
	THD 2	V_i=80dBμ, Δf=±22.5KHz		0.05		
AM Rejection Ratio	AMR	V_i=80dBμ, AM: fm=1KHz, 30% Mod		60		dB
Signal to Noise Ratio	S/N 1	V_i=80dB μ	77	81		dB
	S/N 2	V_i=80dB μ, Δf=±22.5KHz		71		
Tuning Indication Voltage	V_L	I_L=1mA		39	49	dBμ

AM Section (f=1MHz, fm=400Hz, 30% Mod)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		7.5	10.5	mA
Detector Output	V_O 1	V_i=23dBμ	17.3	31	55	mV
Detector Output	V_O 2	V_i=60dBμ	87	122	174	mV
Total Harmonic Distortion	THD 1	V_i=60dBμ		0.45	1.3	%
	THD 2	V_i=100dBμ		1.5	3.0	
Signal to Noise Ratio	S/N 1	V_i=23dBμ	18.0	21.5		dB
	S/N 2	V_i=60dBμ	48	53		
Tuning Indication Voltage	V_L	I_L=1mA	22	30	38	dBμ
Oscillation Output Voltage	V_{OSC}	f=24MHz	60	86	120	mV

TEST CIRCUIT

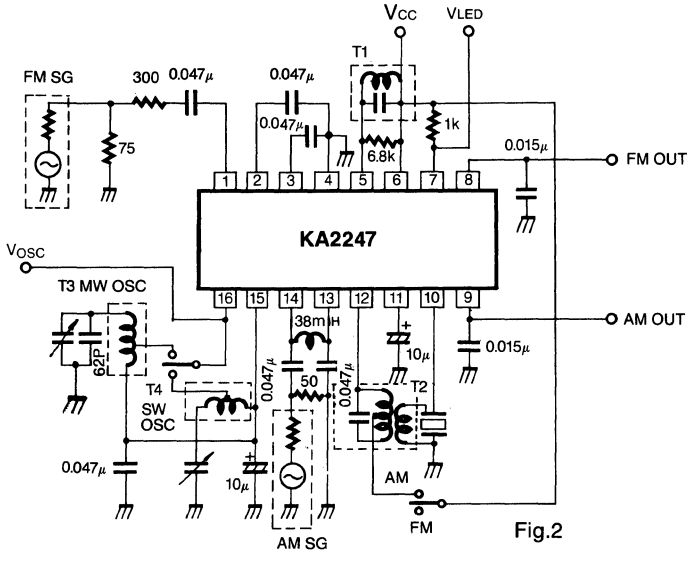
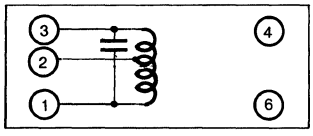


Fig.2

COIL SPECIFICATION

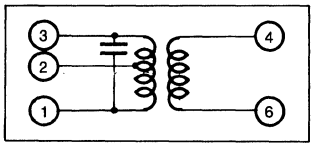
T1 FM IF (DET)



C_o (PF)	f (MHz)	Q_o	TURNS
1-3		1-3	1-3
56	10.7	95	12

Seoul Jupa
0.12mmϕ UEW

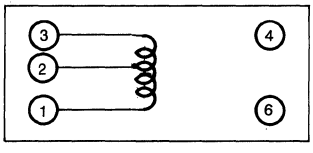
T2 AM IFT (MIX OUT)



C_o (PF)	f (KHz)	Q_o	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	110	90	62	8

Seoul Jupa
0.07mmϕ UEW

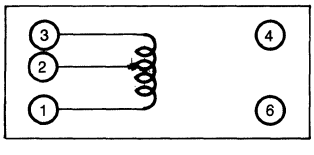
T3 (MW OSC)



f (KHz)	L (μH)	Q_o	TURNS	
	1-3	1-3	1-2	2-3
796	140	140	32	32

Seoul Jupa
0.07mmϕ UEW

T4 (SW OSC)



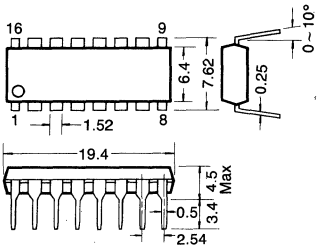
L (μH)	Q_o	TURNS	
1-3	1-3	1-2	2-3
12	80	12	12

Seoul Jupa
0.1mmϕ UEW

FM IF/AM TUNER SYSTEM

The KA22471 is a monolithic integrated circuit developed for the radio cassette tape recorder.

16 Dip Unit: mm



FUNCTIONS

- AM SECTION: Converter, IF amplifier, Detector, Tuning indicator.
- FM SECTION: IF amplifier, Quadrature detector Tuning indicator.

FEATURES

- **Low quiescent circuit current.**
  AM: 7mA (typ) FM: 10mA (typ)
- **Minimum number of external parts required.**
- **Built in AM/FM function switch.**
- **Tuning indicator: direct LED driving capability (V_{LAMP} = 10mA$_{(MAX)}$).**
- **One terminal AM/FM detector output.**
- **Advanced performance at high input signal.**
- **Operation voltage range: V_{CC} = 3V ~ 8V.**

BLOCK DIAGRAM

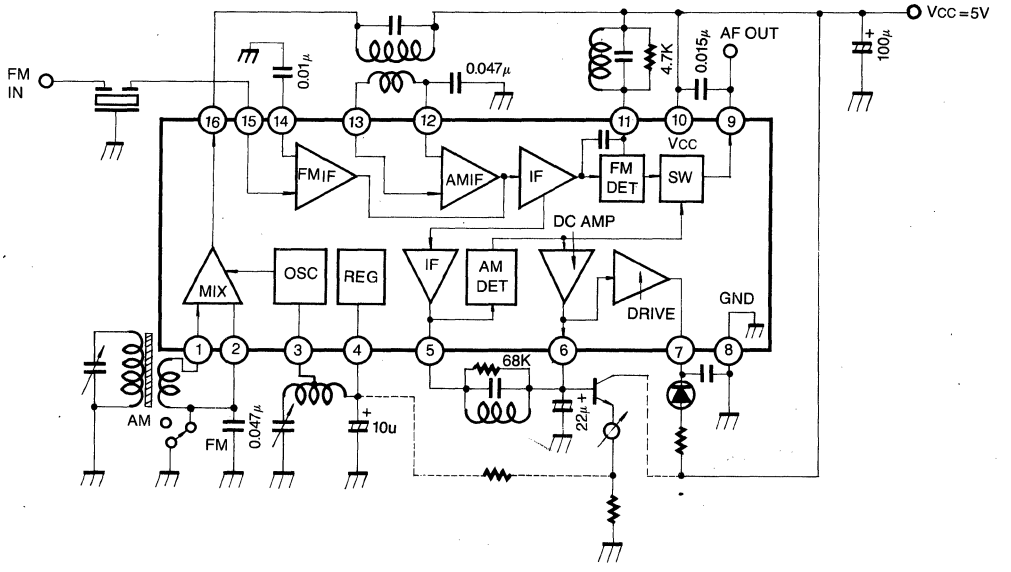


Fig. 1

Note: The dot line denotes a tuning meter application.

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 5V, unless otherwise specified)

FM Section (f=10.7MHz, fm=400Hz, Δf= ±22.5KHz)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		10	15	mA
Input Limiting Sensitivity	V_i (lim)	V_O (V_i=80dBμ)−3dB		40	46	dBμ
Detector Output	V_O	V_i = 66dBμ, R_{DUMP} = 4.7KΩ	57	85	114	mV
Total Harmonic Distortion	THD	V_i = 80dBμ		0.05		%
AM Rejection Ratio	AMR	V_i=80dBμ, AM: fm=1KHz, 30% Mod		38		dB
Signal to Noise Ratio	S/N	V_i = 80dBμ		65		dB
Signal Meter Output	V_M	V_i = 100dBμ	1.6	1.75	1.9	V
Tuning Indication Voltage	V_L	I_L = 1mA		46	52	dBμ

AM Section (f=1MHz, 30% Mod, fm=400Hz)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		7	10	mA
Voltage Gain	A_V	V_i = 26dBμ	20	30	60	mV
Detector Output	V_O	V_i = 60dBμ	65	95	125	mV
Total Harmonic Distortion	THD	V_i = 60dBμ		1.0		%
Signal to Noise Ratio	S/N	V_i = 60dBμ		47		dB
Signal Meter Output	V_M	V_i = 100dBμ	1.6	1.75	1.9	V
Tuning Indication Voltage	V_L			32		dBμ
Oscillator Stop Voltage	V_{stop}	R_{DUMP} = ∞		1.5		V

TEST CIRCUIT

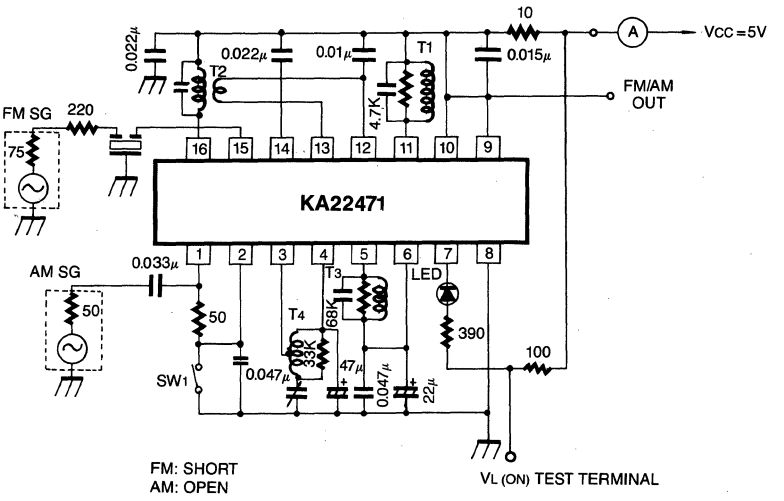
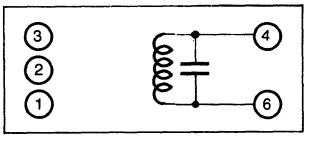


Fig. 2

COIL SPECIFICATION

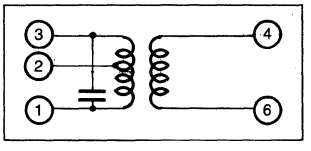
T1 FM IF (DET)



C_O (pF)	f (MHz)	Q_O	TURNS
4-6		4-6	4-6
47	10.7	150	14

Seoul Jupa
0.12mmϕ UEW

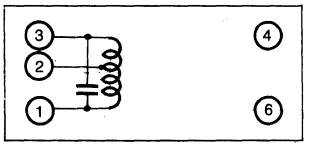
T2 AM IFT (MIX OUT)



C_O (PF)	f (KHz)	Q_O	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	110	90	62	8

Seoul Jupa
0.07mmϕ UEW

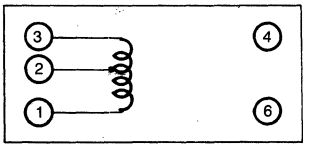
T3 AM IFT (DET)



C_O (pF)	f (KHz)	Q_O	TURNS
1-3		1-3	1-3
180	455	110	152

Seoul Jupa
0.07mmϕ UEW

T4 (MW OSC)



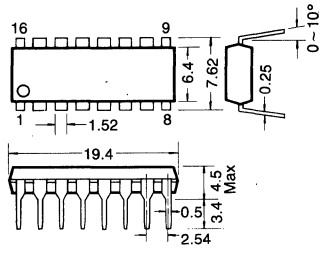
f (KHz)	L (μH)	Q_O	TURNS	
	1-3	1-3	1-2	2-3
796	288	120	13	75

Seoul Jupa
0.08mmϕ UEW

3V FM IF/AM TUNER SYSTEM

The KA2248 is a monolithic integrated circuit developed for the headphone stereo.

16 Dip Unit: mm



FUNCTIONS

- AM SECTION: Converter, IF amplifier, Detector, Tuning indicator
- FM SECTION: IF amplifier, Quadrature detector, Tuning indicator

FEATURES

- **Low quiescent current: AM; I_{CC}=3mA (typ), V_{CC}=3V**
  FM; I_{CC}=8mA (typ), V_{CC}=3V
- **Wide operating voltage range: V_{CC}=1.8V~6V.**
- **Built in AM/FM function switch.**
- **Tuning indicator: direct LED driving capability: 10mA (MAX).**
- **One terminal AM/FM detector output.**
- **Minimum number of external parts required.**

BLOCK DIAGRAM

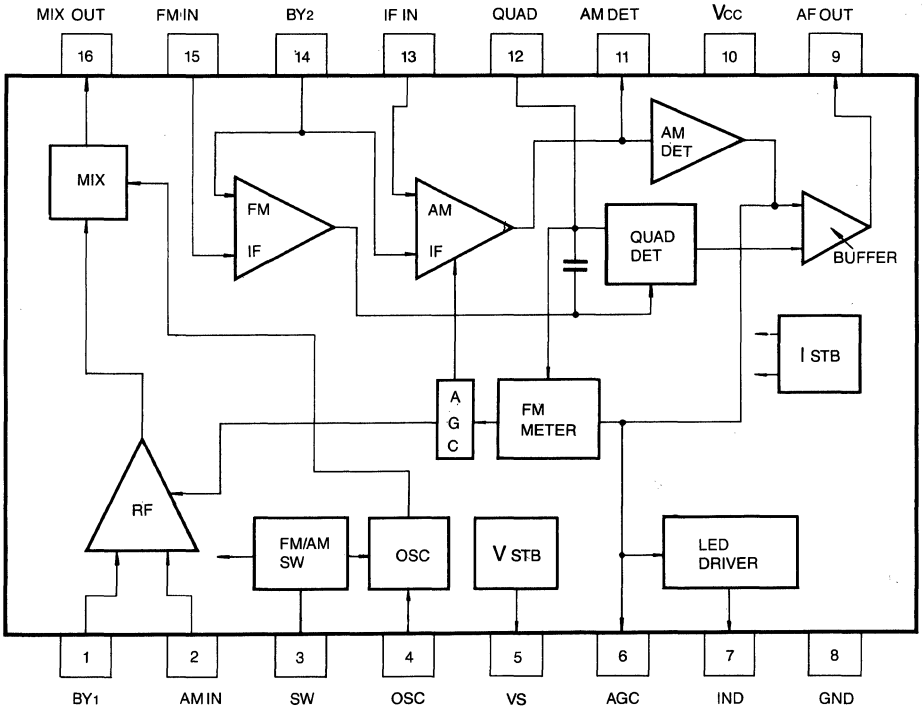


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	6	V
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =3V, unless otherwise specified)

* **FM Section** (f=10.7MHz, fm=1KHz, Δf=22.5KHz)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i =0		8	13	mA
Input Limiting Voltage	V_i (lim)	V_i =86dBμ		46	52	dBμ
Detector Voltage	V_o	V_i =86dBμ	60	85	120	mV
Signal to Noise Ratio	S/N	V_i =86dBμ	50	65		dB
Total Harmonic Distortion	THD	V_i =86dBμ		0.1	1.0	%
AM Rejection Ratio	AMR	V_i =86dBμ	30	45		dB
Tuning Indication Voltage	V_L	I_L =1mA		50	58	dBμ
Output Resistance	R_O	f=1KHz		0.7		KΩ

* **AM Section** (f=1MHz, fm=1KHz, 30% Mod)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Current	I_{CC}	V_i =0		3	7	mA
Voltage Gain	A_V	V_i =26dBμ	20	35	65	mV
Detector Voltage	V_O	V_i =60dBμ	40	60	85	mV
Signal to Noise Ratio	S/N	V_i =60dBμ	35	45		dB
Total Harmonic Distortion	THD	V_i =60dBμ		1.0	3.5	%
Oscillator Stop Voltage	Vstop			1.2		V
Output Resistance	R_O	f=1KHz		8.3		KΩ
Tuning Indication Voltage	V_L	I_L =1mA		26	40	dBμ

TEST CIRCUIT

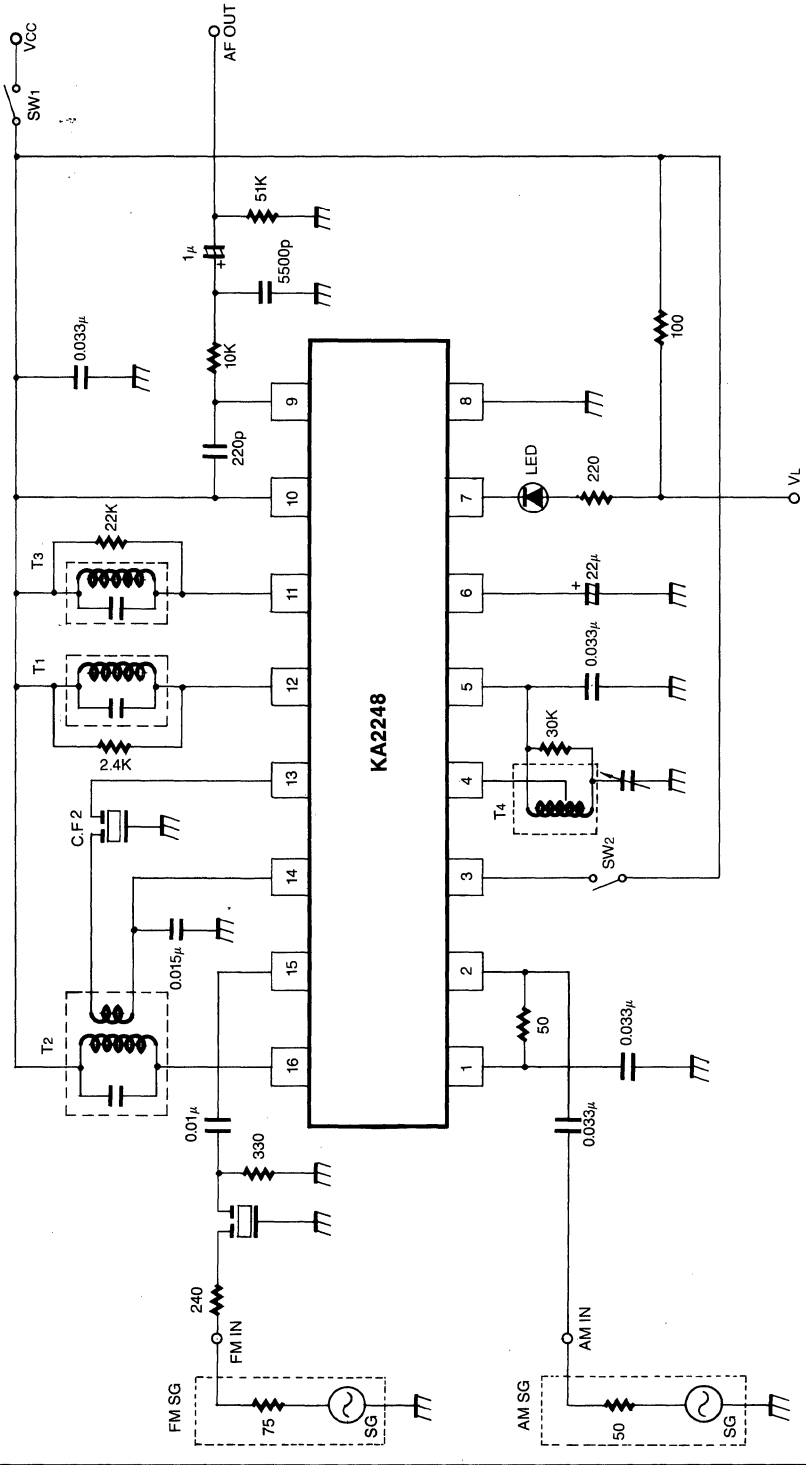
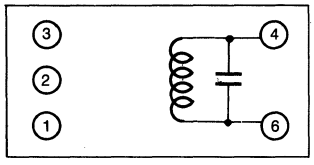


Fig. 2

COIL SPECIFICATION

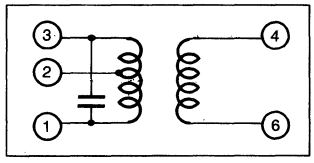
T1 FM IF (DET)



C_o (pF)	f (MHz)	Q_o	TURNS
4-6		4-6	4-6
100	10.7	150	14

Seoul Jupa
0.12mmϕ UEW

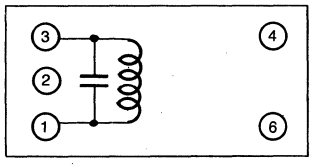
T2 AM IFT (MIX OUT)



C_o (PF)	f (KHz)	Q_o	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	110	90	62	8

Seoul Jupa
0.07mmϕ UEW

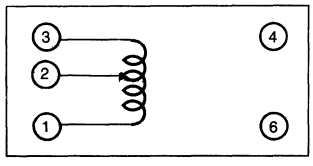
T3 AM IFT (DET)



C_o (pF)	f (KHz)	Q_o	TURNS
1-3		1-3	1-3
180	455	110	152

Seoul Jupa
0.07mmϕ UEW

T4 (MW OSC)



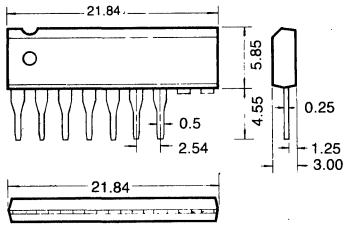
f (KHz)	L (μH)	Q_o	TURNS	
	1-3	1-3	1-2	2-3
796	288	120	13	75

Seoul Jupa
0.08mmϕ UEW

FM FRONT END FOR PORTABLE RADIO

The KA2249 is a monolithic integrated circuit designed for FM front end of the portable radio.

7 Sip Unit: mm



FEATURES

- **High frequency amplifier frequency converter local oscillator.**
- **Wide operating voltage: V_{CC}=2V ~ 7V.**
- **Low current consumption: typ. 2mA (V_{CC}=4V).**

SCHEMATIC DIAGRAM

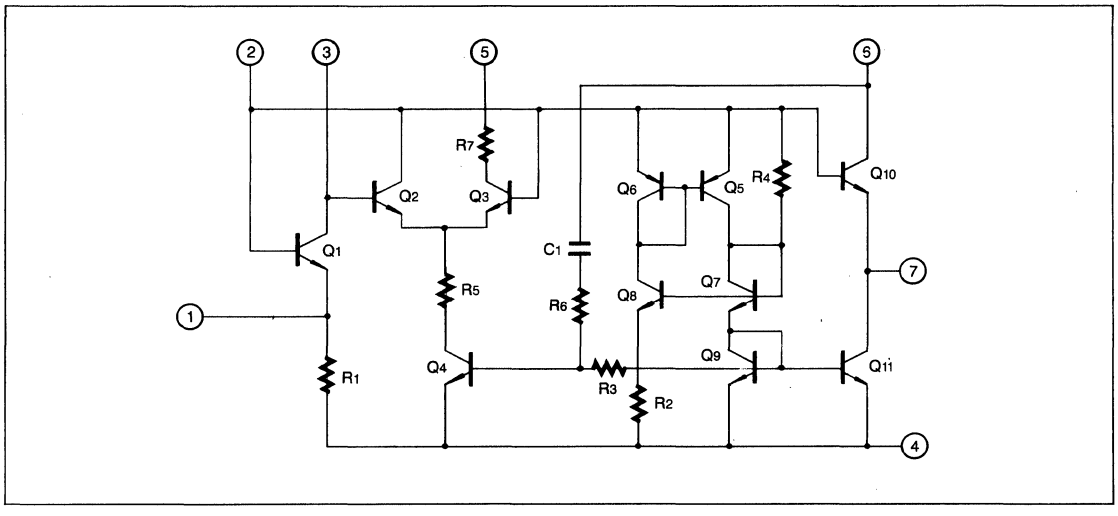


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7	V
	V (3 ~ 4)	14	V
Terminal Voltage	V (5 ~ 4)	14	V
	V (6 ~ 4)	14	V
Power Dissipation (T_a =75°C)	P_d	30	mW
Operating Temperature	Topr	− 20 ~ + 75	°C
Storage Temperature	Tstg	− 55 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 4V)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Circuit Current	I_{CC}	without signal	1.4		3.0	mA	2
Output Voltage	V_O	V_i =70dB, 106MHz	30.5		68.5	mV	3
Oscillation Voltage	V_{OSC}	V_{CC} =2V	130			mV	3

TEST CIRCUIT 1

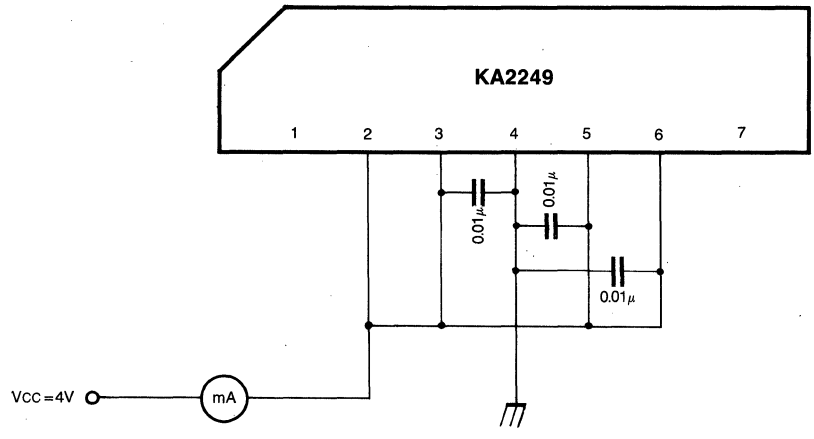


Fig. 2

TEST CIRCUIT 2 (V_o, V_{osc})

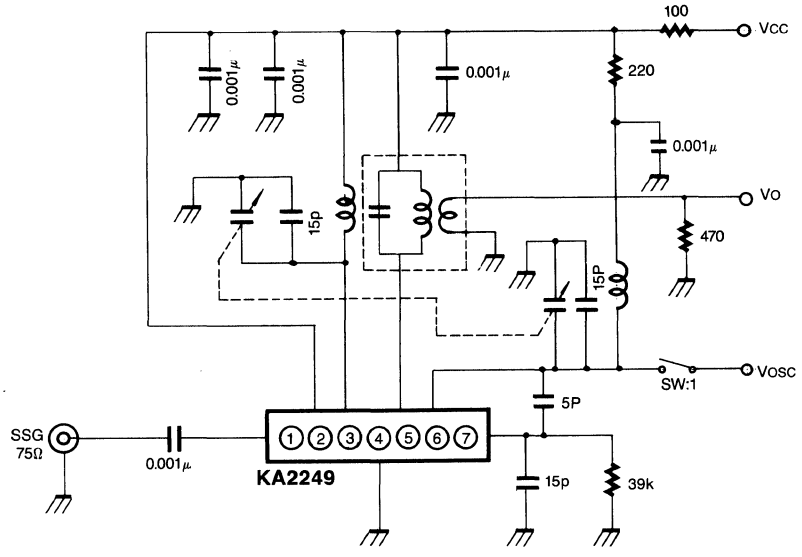
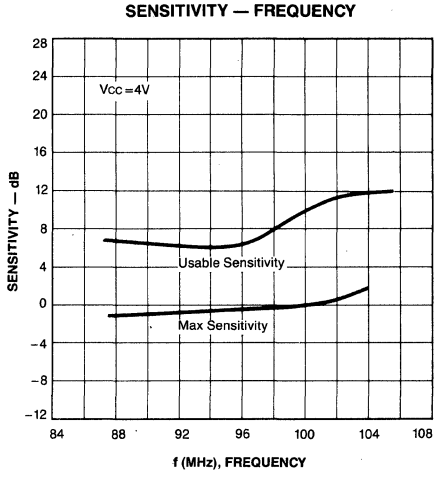
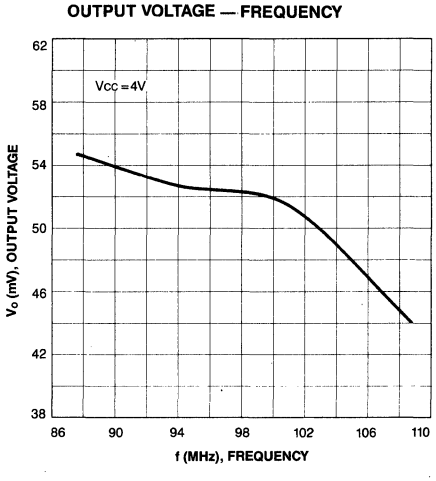
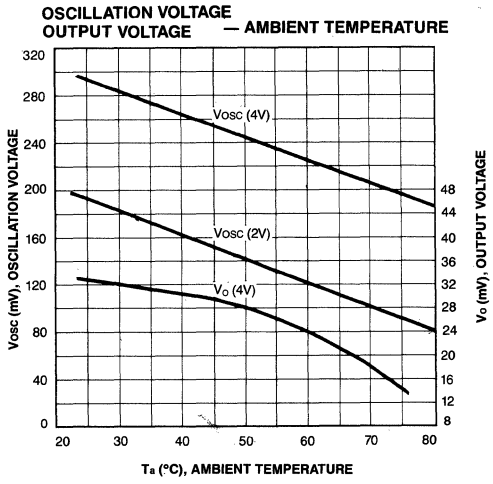
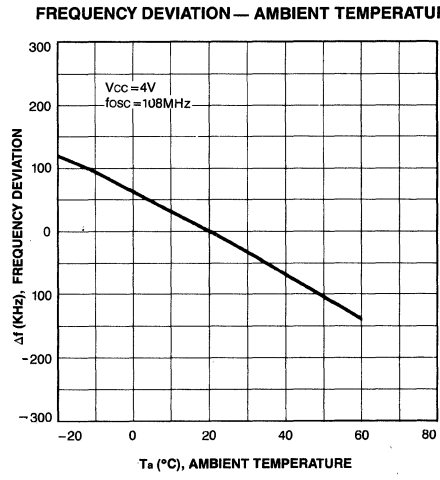


Fig. 3









APPLICATION CIRCUIT

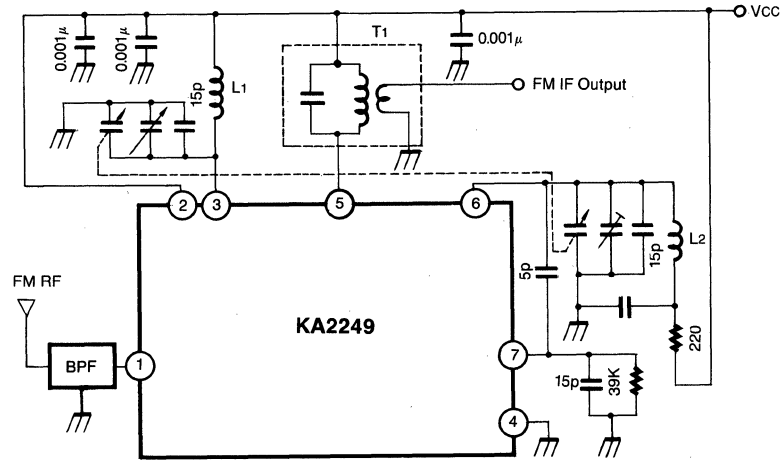
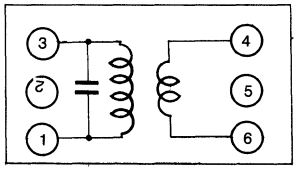


Fig. 4

COIL SPECIFICATION

T1 FM IFT



C_o (pF)	f (MHz)	Q_o (%)	TURNS		
			1-3	4-6	
56	10.7	95	12	2	

Seoul Jupa
SJ-015-382
0.1mmϕ UEW

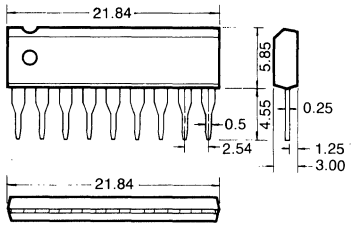
FM FRONT END

The KA22491 is a monolithic integrated circuit designed for FM front end application, which is suitable for portable radio and radio cassette.

This IC contains RF amplifier, MIX, local oscillator and varicap for AFC.

This IC simplify the design of FM front end circuit.

9 Sip Unit: mm



FEATURES

- **Wide operating supply voltage range: V_{CC}=1.8V~6V.**
- **Excellent supply voltage dependance of local oscillator: Oscillation stop V_{CC}=1.5V (Typ).**
- **Varicap for AFC.**

BLOCK DIAGRAM

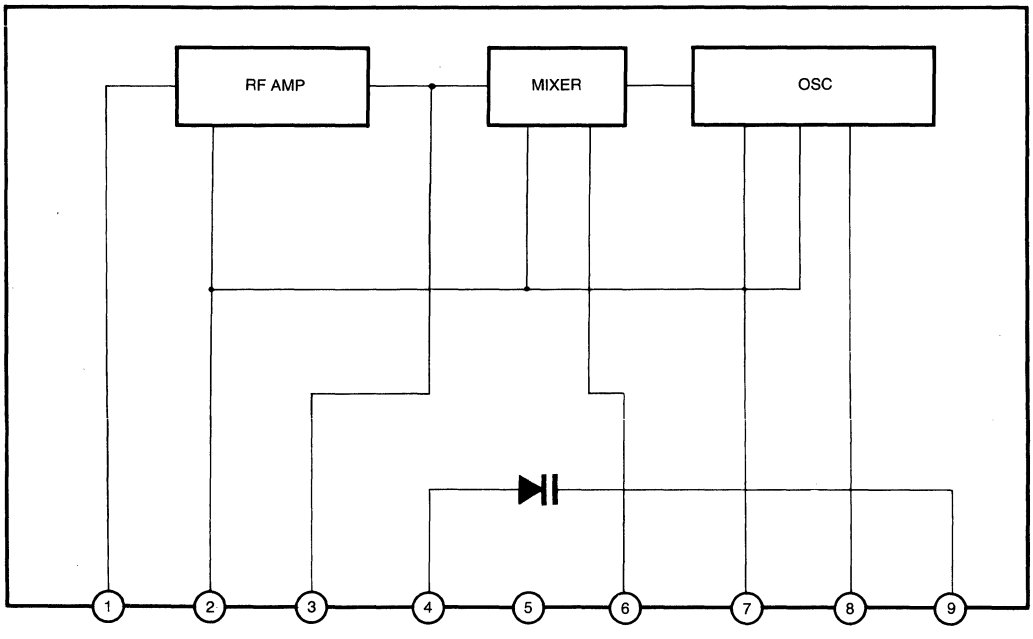


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7	V
Power Dissipation	Pd	100	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=4V, f=98MHz, f_{OSC}=108.7MHz, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current	I_{CC}	V_i=0		3	5	mA
Output Voltage	V_O	V_i=100dBμ	100	125	160	mV
Local Oscillation Voltage	V_{OSC}	V_{CC}=2V	180	300		mV
Conversion Gain	A_V			45		dB
Input Impedance	R_i			2		KΩ

these specifications are subject to change without notice.

TEST CIRCUIT

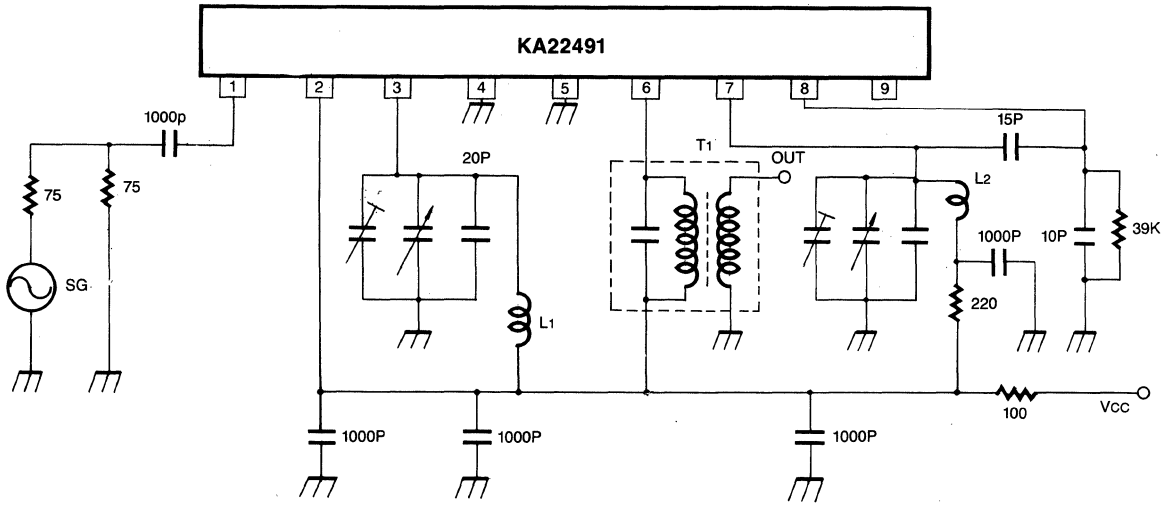


Fig. 2

APPLICATION CIRCUIT

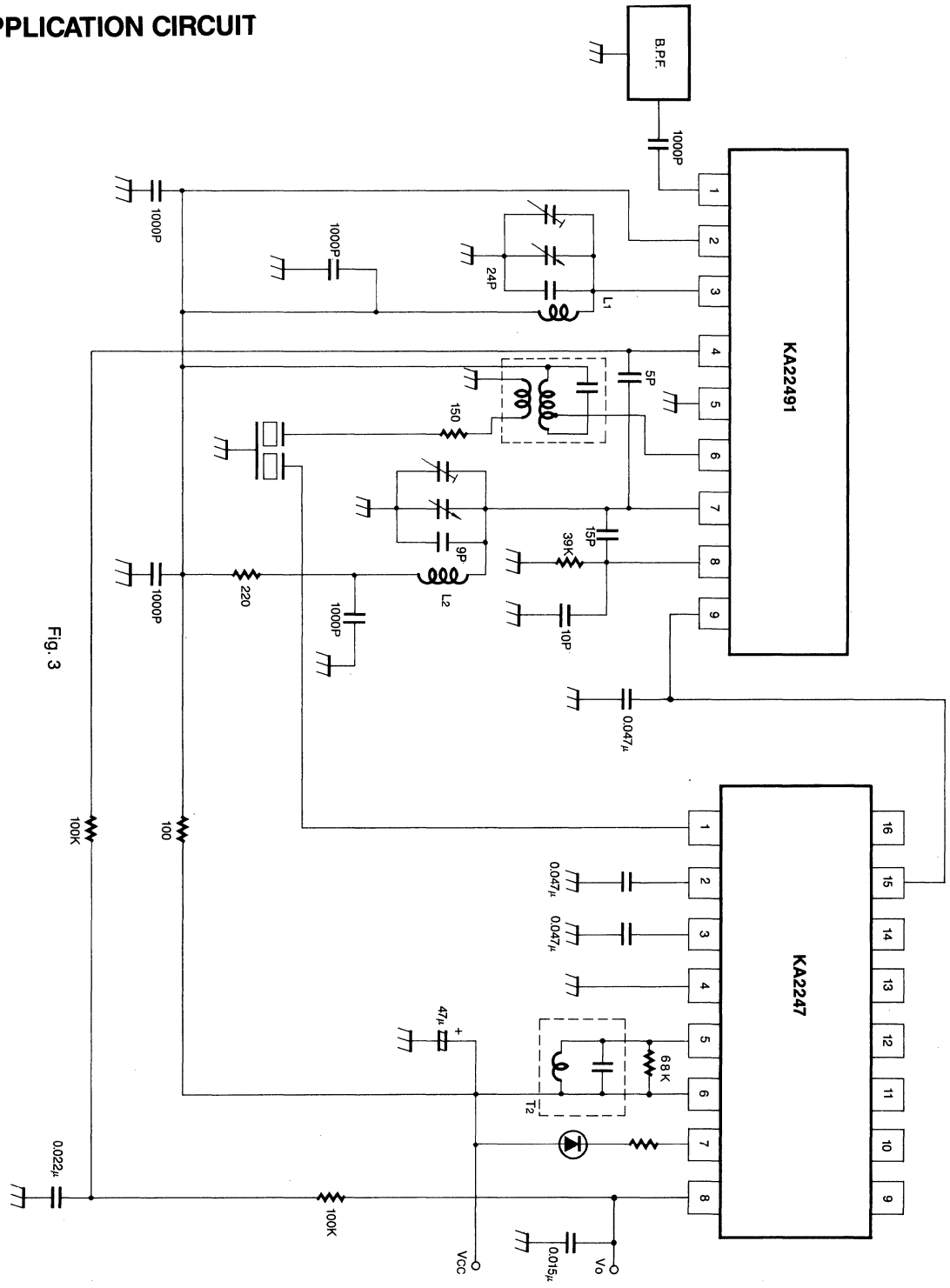
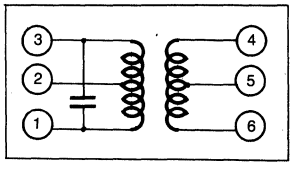


Fig. 3

COIL SPECIFICATION

	DIAMETER (ϕ)	WIRE	TURNS
L1 (RF COIL)	5.5mm	0.8mm	5
L2 (OSC COIL)	5.5mm	0.8mm	6

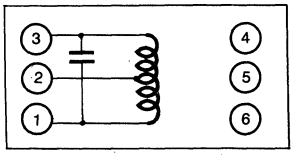
T1 (FM IF)



C_O (pF)	f (MHz)	Q_O (%)	TURNS		
			1-3	4-6	
56	10.7	95	12	2	

Seoul Jupa SJ-015-382 0.1mmϕ UEW

T2 (FM DET)



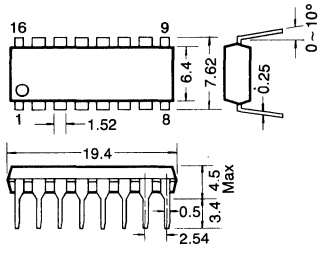
C_O (pF)	f (MHz)	Q_O (%)	TURNS		
			1-3		
56	10.7	95	12		

Seoul Jupa 0.1mmϕ UEW

FM STEREO MULTIPLEX DECODER

The KA2261 is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator. It was designed for use in car stereo, cassette recorder and other equipment.

16 Dip Unit: mm



FEATURES

- **A PLL is used for high multiplexing performance.**
- **Wide operating supply voltage range (3V ~ 16V).**
- **Low quiescent circuit current (I_{CC} = 8.5mA Typ).**
- **High SCA rejection ratio.**
- **High channel separation (45dB Typ) and can be controlled by external resistor.**
- **Built-in VCO disable and monaural muting circuits.**
- **Built-in stereo indicator lamp drive circuit.**

TYPICAL APPLICATION CIRCUIT

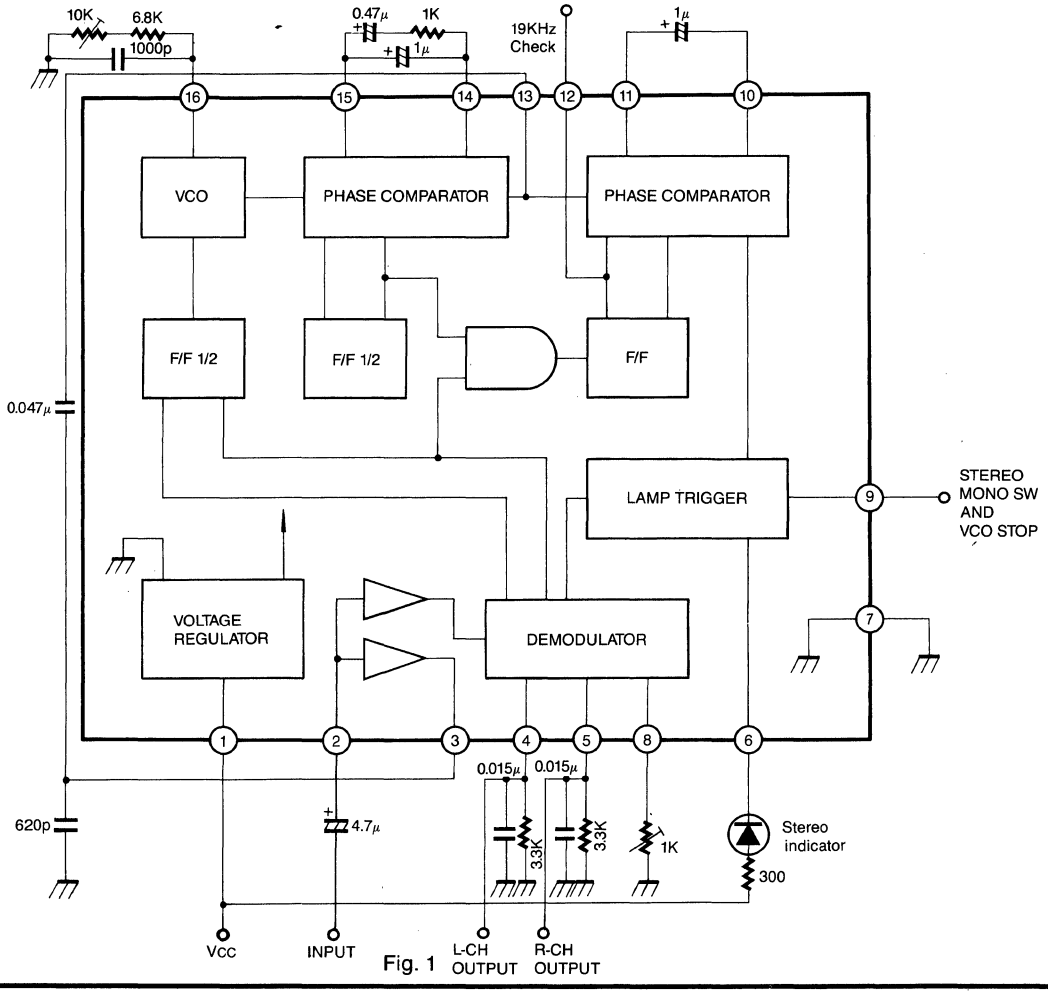


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lamp Current	I_L	40	mA
Power Dissipation	P_d	400	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temeprature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =6V, f=1KHz, R_L =3.3KΩ, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	V_i=o		8.5	12	mA
Channel Separation		Sep	V_i=100mV, L+R=90% P=10%, f=1KHz	35	45		dB
Total Harmonic Distortion	Mono	THD 1	V_i=100mV		0.2		%
	Stereo	THD 2	L+R=90mV, P=10mV		0.7		%
Output Voltage		V_O	V_i=100mV, f=1KHz	66	85	115	mV
Channel Balance		CB	V_i=100mV, f=1KHz		0.5	1.5	dB
Lamp on Level		V_L(on)	L+R=90%, P=10%		65		mV
Lamp Hystersis		HY			3.5	6.0	dB
Maximum Input Level		V_i (max)	THD=2%		450		mV
SCA Rejection Ratio		SCA R_{ej}	L+R=90%, P=10%		70		dB
Signal-to-Noise Ratio		S/N	V_i=100mV, f=1KHz		75		dB
Carrier Leak		CL	V_i=100mV, L+R=90% P=10%		32		dB
Capture Range		CR	V_i=100mV, L+R=90% P=10%		±3		%
Input Impedance		R_i		15	20		KΩ

TEST CIRCUIT

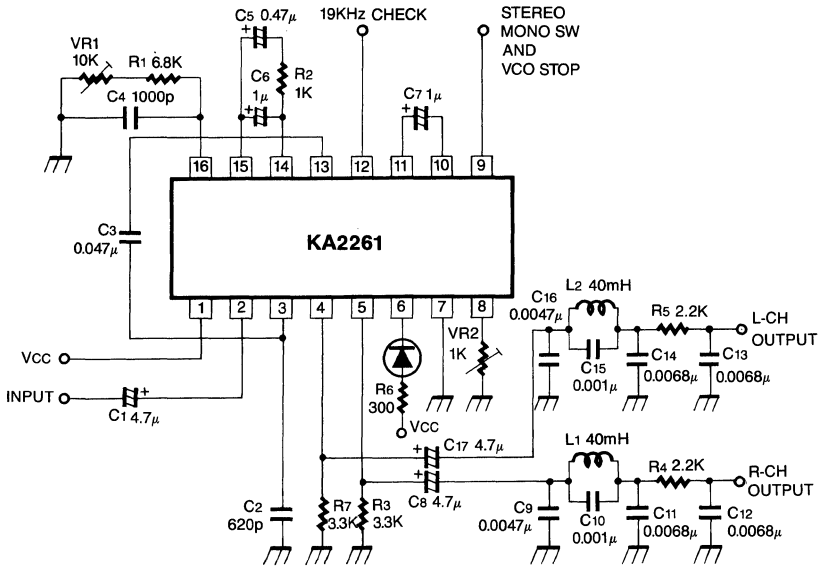
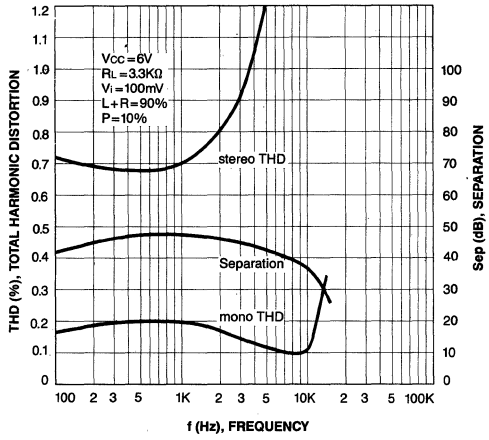
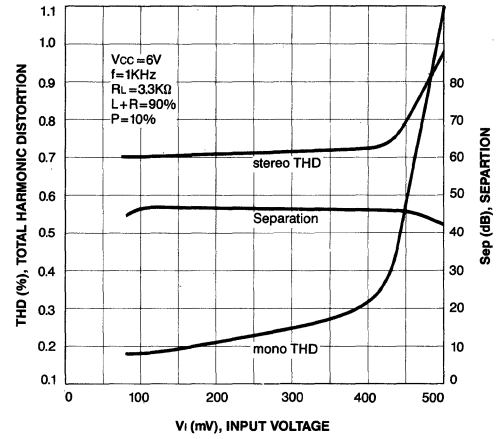


Fig. 2

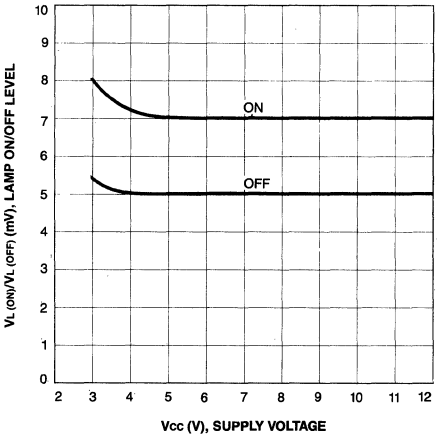
SEPARATION —FREQUENCY
TOTAL HARMONIC DISTORTION



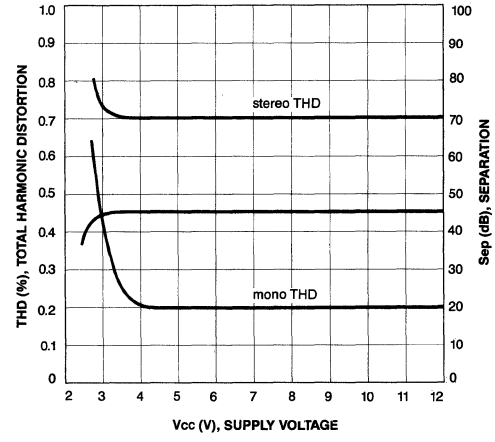
SEPARATION — INPUT VOLTAGE
TOTAL HARMONIC DISTORTION



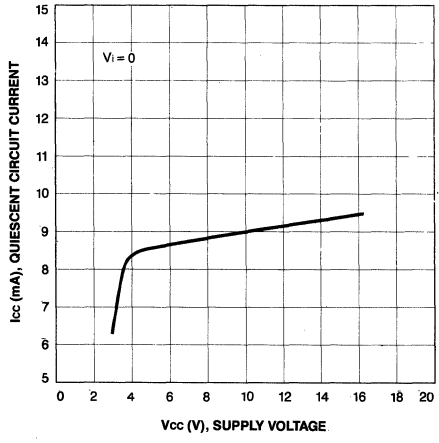
LAMP ON/OFF LEVEL-SUPPLY VOLTAGE



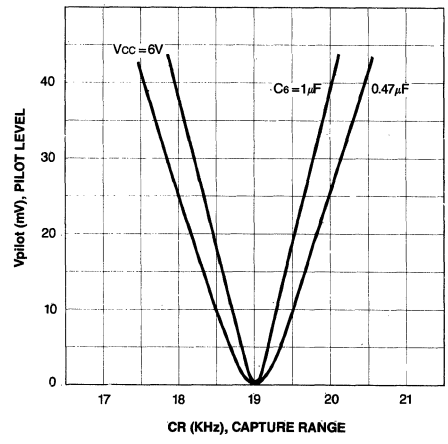
SEPARATION — SUPPLY VOLTAGE
TOTAL HARMONIC DISTORTION



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE

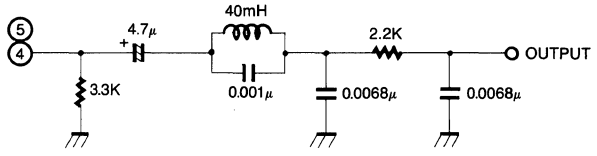


CAPTURE RANGE



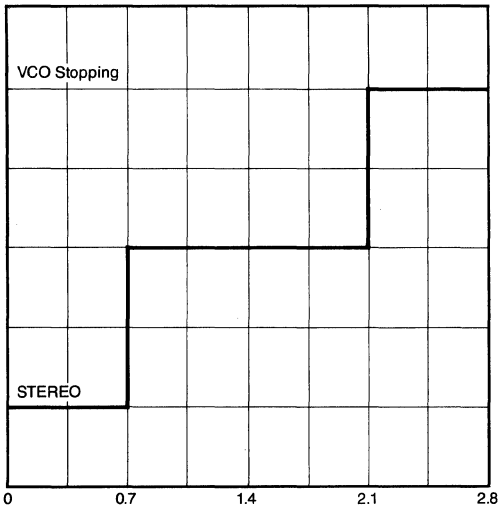
External Components (Refer to test circuit)

1. Input coupling capacitor (Pin 2)
   The recommended value is 4.7μF. If smaller values than 4.7μF are used low frequency separation will be worsen, and if larger values are used the DC operating point will require time for stabilization.
2. Demodulator output (Pin 4, 5)
   These components provide R and L channel output load circuits. The recommended circuits are follows:



3. Separation control (Pin 8)
   This component is a variable resistor used to adjust the out signal separation.
4. Low pass filter (Pin 10, 11)
   This capacitor is used to filter the 19KHz signal detected by the phase comparator. The recommended value is 1μF. If made too small, the lamp may light improvely when a large mono input signal or external noise received, too large a capacitance value will take more time to switch between mono and stereo modes.
5. Preamplifier output capacitor (Pin 3, 13)
   This capacitor coupled preamplified with phase comparator. The recommanded value is 0.047μF.
6. Phase compensation capacitor (Pin 3, GND)
   This capacitor is prepared in order to compensate the phase advanced.
7. Loop filter (Pin 14, 15)
   This is the low pass filter for the PLL, which is determined the capture range. The recommended value is follow:
   $V_i \leq 250mV$ $C_{14\text{-}15} = 0.47\mu F$
   $V_i \geq 250mV$ $C_{14\text{-}15} = 1\mu F$
8. Control of Pin 9
   Function of pin 9 is a change-over of stereo/mono and VCO stopping.

SCHEMATIC DIAGRAM of PIN 9 CONTROL



V9 (V), SUPPLY VOLTAGE to PIN 9

9. VCO network (Pin 16)
   Since the VCO has a negative temperature coefficient, the RC network compensate by using a poly styrene capacitor and a resistor.

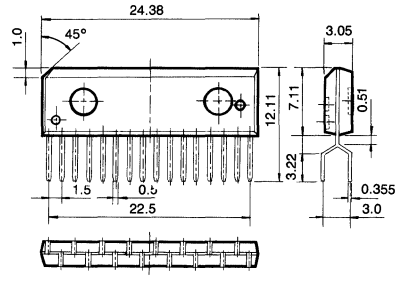
FM STEREO MULTIPLEX DECODER FOR CAR STEREO

KA2262 is a multiplex for FM car stereo, and it has the following 2 functions through its utilization of the IF meter output voltage, etc.

1. Stereo noise control (SNC) under which the noise particular on the FM stereo unit in the weak electric field is reduced smoothly.
2. High-cut control (HCC) under which the high frequency is smoothly attenuated.

   In addition, KA2262 can be, due to its low distortion factor, an IC for multiplex stereo demodulator which is appropriate for the car component stereo unit.

16 ZIP



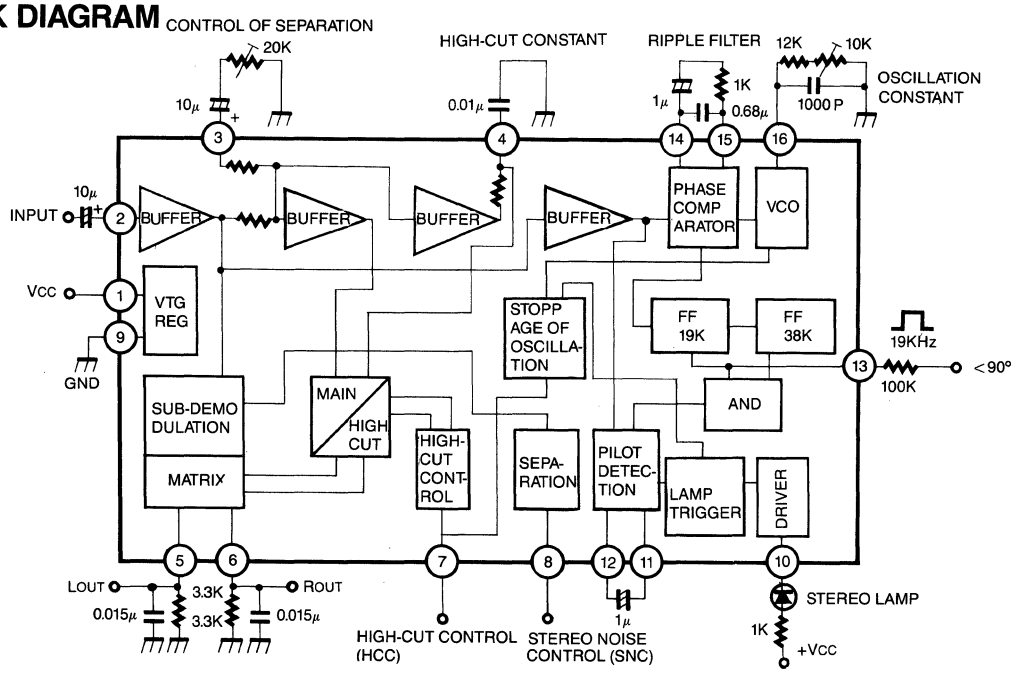
FUNCTIONS

- Stereo noise control (SNC Terminal).
- High-cut control (HCC Terminal).
- Stereo/Monaural automatic conversion.
- Stoppage of VCO oscillation.
- With separation control terminal.

FEATURES

- **Low distortion (0.05%: Typ).**
- **Good ripple rejection (35dB: Typ).**
- **Wide operating supply voltage range (6.5V ~ 14V).**
- **The space factor is advantageous because of the single-end package.**
- **High channel separation (50dB: Typ).**

BLOCK DIAGRAM



Note: There exists a possibility of change on the VCO Oscillation Constant.

Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

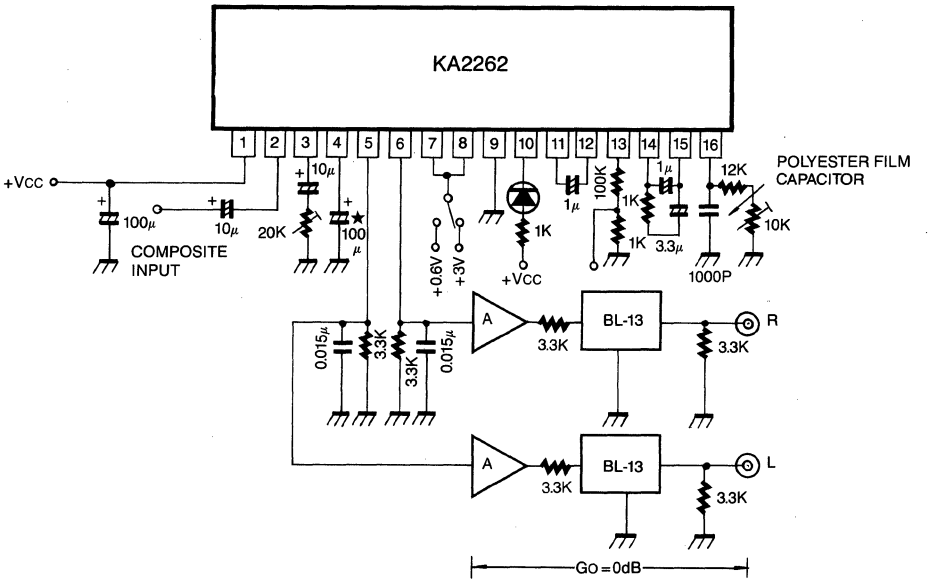
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lamp Current	I_L	40	mA
Power Dissipation	Pd ($T_a \leqq 45°C$)	520	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =10V, f=1KHz, R_L =3.3KΩ, unless otherwise specified)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	V_i =0		21	27	mA
Channel Separation		Sep	V_i =300mV, L+R=90%, P=10%	40	50		dB
Total Harmonic Distortion	Mono	THD1	V_i =300mV		0.05	0.2	%
	Stereo	THD2	V_i =300mV, L+R=90%, P=10%		0.05	0.2	%
Output Voltage		V_O	V_i =300mV, Sub	140	200	280	mV
Channel Balance		CB	V_i =300mV		0.5	1.5	dB
Lamp on Level		V_L (on)	L+R=90%, P=10%	60	85	120	mV
Lamp Hysteresis		HY			3	6	dB
Maximum Input Level		V_I (max)	L+R=90%, P=10%, THD=1%	700	800		mV
SCA Rejection Ratio		SCA Rej	L+R=90%, P=10%		80		dB
Signal-to-Noise Ratio		S/N	V_i =300mV		70	78	dB
Ripple Rejection		RR			35		dB
Capture Range		CR	P=30mV		±3		%
Input Impedance		Ri			20		KΩ
SNC Output Attenuation		$SNC_{(ATT)}$	V_8 =0.6V, L−R=90%, P=10%	−8.5	−3.0	−0.3	dB
SNC Output Voltage		SNC V_O	V_8 =0.1V, L−R=90%, P=10%			5	mV
HCC Output Attenuation		$HCC_{(ATT)}$ 1	V_7 =0.6V, L+R=90%, P=10%	−15.0	−6.0	−0.5	dB
		$HCC_{(ATT)}$ 2	V_7 =1V, L+R=90%, P=10%	−2.0		0	dB

TEST CIRCUIT



★:100μF connected between pin 4 and GND is for measurement of SNC output voltage, HCC output voltage.

Fig. 2

SNC (STEREO NOISE CONTROL) AND HCC (HIGH-CUT CONTROL)

In order to ameliorate the signal-to noise (S/N) ratio in the weak electric field, both SNC and HCC Terminals are installed in KA2262. When the SNC Terminal is controlled, the noise particular on the stereo reception in the weak electric field can be decreased.

By using the HCC Terminal, the FM noise at the high-frequency level can be reduced, resulting in the effective improvement of S/N ratio. (Refer to Fig. 4)

As shown in Fig. 4 the deterioration of S/N ratio is larger by approx. 21.7dB in the stereo mode than in the Monaural mode, as far as the weak electric field is concerned.

In general, the noise is considerably harsh (offensive) to the ear if the S/N ratio is lower than 30 ~ 40dB. So, the Areas "A", "B" and "C" have, in this study, been prepared, as shown in Fig. 4, according to the intensity of electric field on a provisional criteria of 30 ~ 40dB (S/N ratio).

The procedures of setting SNC and HCC are described below on the presumption of SNC operation in Area "A" and of HCC operation in Area "B".

Regarding the Area "C", a light level of muting is made at the IF stage.

1. SNC (Stereo Noise Control)

The S/N ratio of stereo reception is worse by 21.7dB in comparison with the monaural reception. However, such S/N ratio can be ameliorated if the separation of stereo reception is changed. The effect of S/N-ratio amelioration can become significant when the separation is less than approx. 20dB. The relationships between this separation and the degree of S/N improvement are shown in Fig. 5.

Under the SNC utilized in KA2262, the S/N ratio improvement is accomplished in the weak electric field by the alteration of separation mentioned above. In details, the separation of stereo reception is controlled by changing the demodulation level of this sub-signal.

If the level output of signal meter in IF stage is utilized as the source of control signal, the S/N ratio can be made lower than approx. 40dB in the Area "A" shown in Fig. 4.

In the case of an idealistic S/N-ratio improvement, a gradual conversion should be made from stereo mode to monaural mode so that the S/N ratio may be constant from the point of stereo S/N ratio, 40dB, to that of monaural S/N ratio, 40dB. The procedures of setting control level will be described later.

In Fig. 6, are shown the relationships between the voltage applied to Pin 8 (SNC Terminal) of KA2262 and the characteristics of separation (SNC characteristics).

Since Pin 8 is positioned at the base of common-collector PNP transistor, the unit is set in the stereo mode if Pin 8 is open. In contrast, it is set in the monaural mode when Pin 8 is grounded.

The control through the use of SNC Terminal is available only when the stereo indicator lights on by the locking to the pilot signal.

Since the SNC control current is less large, the constant of outer circuit can be set at a large amount, resulting in no influence on the meter output circuit of IF stage. Thus, the designing work of this circuit can easily be made.

2. Design of Outer Circuit for SNC Characteristics (Setting Characteristics through Drawing)

The SNC characteristics can be set in order to change the separation smoothly from stereo mode to monaural mode in Area A shown in Fig. 4. The following procedures are preferable for such a setting.

Relationships between separation and improvement of S/N ratio ..... Fig. 5

Relationships between voltage applied to SNC terminal and separation characteristics ..... Fig. 6

If both the "graph" showing the relationships between signal meter output (in IF stage) and antenna input and the "graph" which shows the relationships between antenna input and S/N ratio improvement characteristics are obtained by using Figs. 5 and 6, the relationships between antenna input and S/N ratio improvement characteristics can be obtained through the preparation of drawing.

Also, the characteristics of SNC-terminal application voltage can adversely be obtained from the S/N characteristics which is desirable for the user.

An example of drawing preparation is shown in Fig. 8. In order to simplify the recognition, all of "SNC characteristics", "IF meter characteristics" and "stereo S/N-ratio characteristics" are similarized each other with straight lines.

The example of preparation is as follows:

The stereo S/N-ratio improvement characteristics are obtained from the SNC characteristics. In the chart diagram, (a) of the 2nd sector is a base SNC characteristics. Through the projection to the 3rd sector from (a), the separation is 20dB at Point "1" while the level of S/N-ratio improvement is 1dB there at.

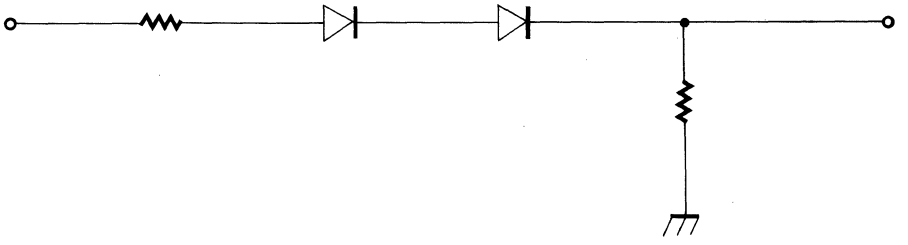
When projection is made from the 1st sector to the 4th sector, the point where S/N ratio is improved by 1dB from the line of stereo S/N ratio in the 4th sector corresponds with Point 1.

Similarly, Point 2 on SNC characteristics in the 2nd sector correspoinds with Point 2 in the 4th sector as well as Point 3 in the 2nd sector with Point 3 in the 4th sector. Thus, the individual S/N-ratio improvement characteristics can be obtained.

Similarly to the above, the characteristics (b) of 2nd sector is projected like Characteristics (b) of 4th sector, while the Characteristics (c) or 2nd sector is projected like Characteristics (c) of 4th sector. Thus, the drawing of improvement characteristics can be prepared.

As a result of preparation of drawing, the S/N-ratio improvement characteristics of Fig. (b) in the 4th sector is idealistic. However, the SNC characteristics corresponding therewith becomes the characteristics shown with Fig. (b) of 2nd sector. It is difficult to realize such characteristics.

From the viewpoint of practical characteristics, the one like Fig. (c) seems to be appropriate. The SNC characteristics shown in Fig. (c) are obtained by the use of both the shifting operation made by 2 diodes and 1/2 bleeder.



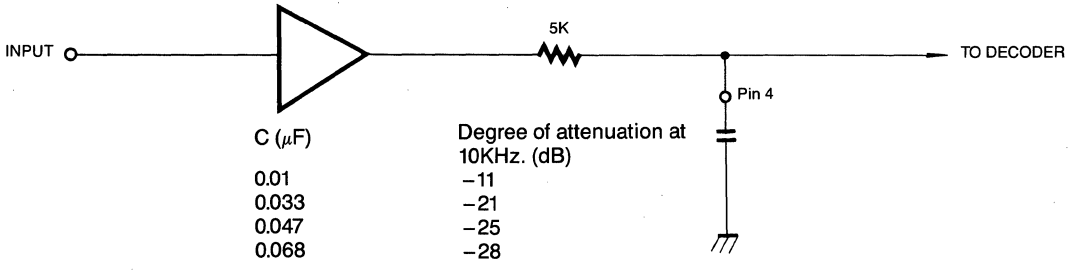
3. HCC (High-cut Control)

In Area B where the S/N ratio is lower than 40dB even in the monaural mode, the S/N ratio can be improved from the acoustic standpoint if the level of high frequency (at about 7 KHz) is lowered.

When the signal meter output voltage of IF stage is given to the HCC Terminal (Pin 7) of KA2262, a smooth high-level attenuation (high-cut control) can be made according to the meter's voltage.

In Fig. 9, are shown the frequency characteristics (monaural) of MPX output caused from the voltage applied to Pin 7. The frequency characteristics obtained when 100% high cut is made can freely be set by the 4-pin outer capacitor.

The equivalent circuit at this stage is determined by the time constant of "5KΩ" and "C", as shown in the following diagram. By the approx. amount by C, the degree of attenuation at 10KHz. is as follows:



C (μF)	Degree of attenuation at 10KHz. (dB)
0.01	−11
0.033	−21
0.047	−25
0.068	−28

The relationships (HCC characteristics) between Pin 7 applied voltage and high-cut rate (%) are shown in Fig. 10

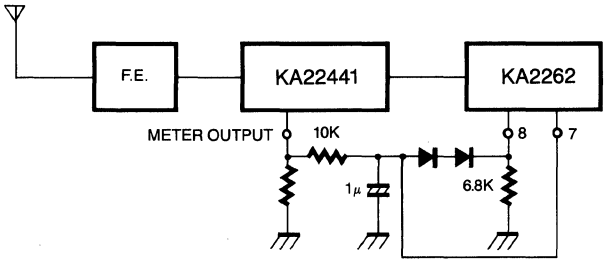
When the characteristics of IF meter output voltage and the S/N-ratio characteristics of Area B (shown in Fig. 4) are obtained in addition to Fig. 10, the characteristics of S/N-ratio improvement which is implemented by HCC can be drawn.

The output of meter of IF amplifier IC used for quadrature detection is usually the one shown in Fig. 4. (Fig. 3 shows the data of KA22441). Thus, the HCC characteristics (Fig. 10) are set so that the Area B may be ameliorated when the output mentioned above is directly connected with the HCC Terminal (Pin 7) of KA2262.

Being very small similarly to the control current of Pin 8, such control current of Pin 7 gives no influence to the output of meter.

4. SNC/HCC Connection Circuit when they are connected with IF Stage

In Fig. 3, is shown an example of S/N-ratio characteristics caused from the antenna input when SNC and HCC are connected with the IF stage through the outer circuit shown below.



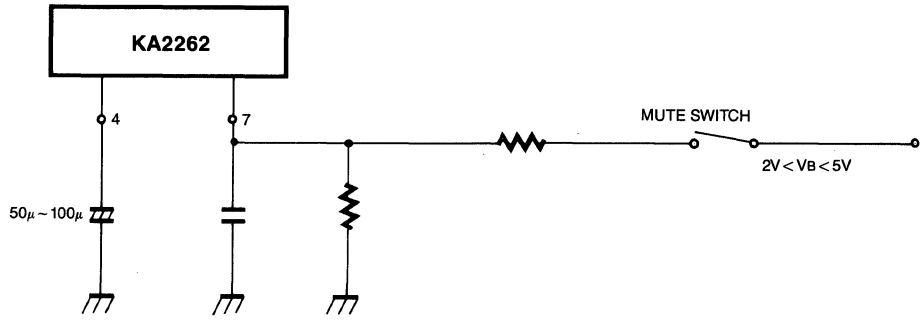
5. Improvement of S/N Ratio in Area C shown in Fig. 3

In Area C shown in Fig. 3, the S/N ratio is further worsened. Its improvement should be performed by the IF muting. The KA22441 can be enumerated as an IC which can vary this IF muting linearly. The S/N-ratio improvement effect of KA2262 can further be enhanced if KA2262 is used together with KA22441.

6. Use of HCC Terminal for the Muting Function

In the event that the removal of high-frequency noise is not required when HCC Terminal is used for a home-enjoyed stereo unit, etc., the muting can be accomplished by approx. 37dB if this HCC function is utilized for the muting function.

If the time constant is applied on the control of Pin 7, the "Fade In" and "Fade Out" operations can be performed on the muting. The muting can be performed without offensiveness to the ear as alien factors such as shock noise, etc. are removed thereby.



7. Stop Method of VCO

When a voltage higher than 7V is applied to the HCC Terminal (Pin 7), the oscillation of VCO can be discontinued, resulting in the Monaural Mode. At this stage, both SNC and HCC are in the OFF status.

The relationships between the incoming current and Pin 7 applied voltage are shown in Fig. 11.

8. Separation Control Terminal

The control of separation is implemented by controlling the level of main signal.

The range of separation of the controilable input compost signal (Sub-signal/main signal ratio) is approx. the one shown in the following formula.

$$m = \frac{\text{Sub-signal level}}{\text{Main signal level}} \qquad 0.7 > m > 1.25 \text{ (At peak level)}$$

AN EXAMPLE OF S/N IMPROVEMENT IN WEAK ELECTRIC FIELD MADE BY KA2262 SYSTEM

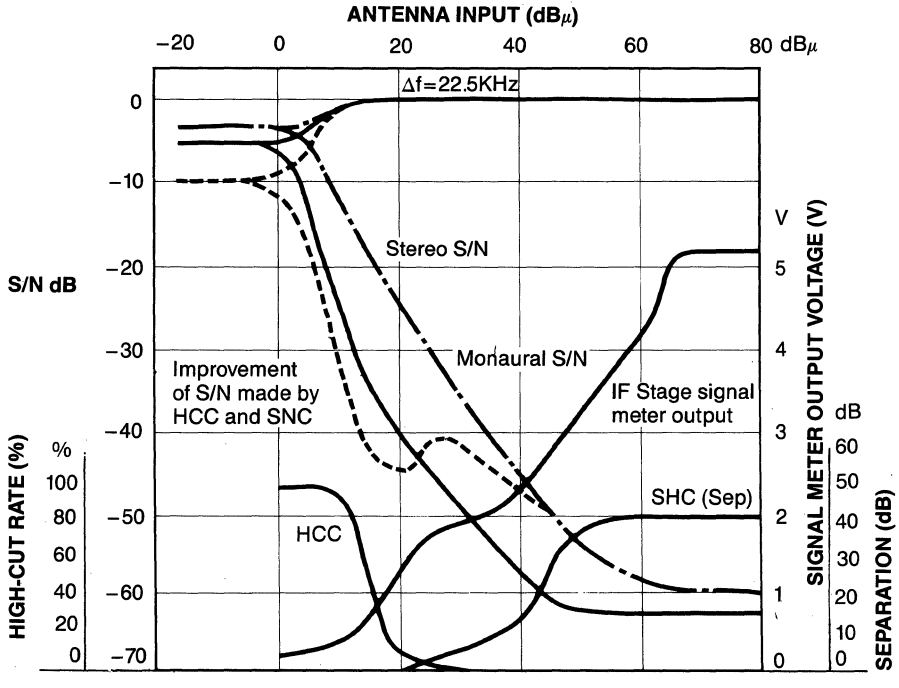


Fig. 3

CHART DIAGRAM USED FOR OBTAINING STEREO CHARACTERISTICS FROM SNC CHARACTERISTICS

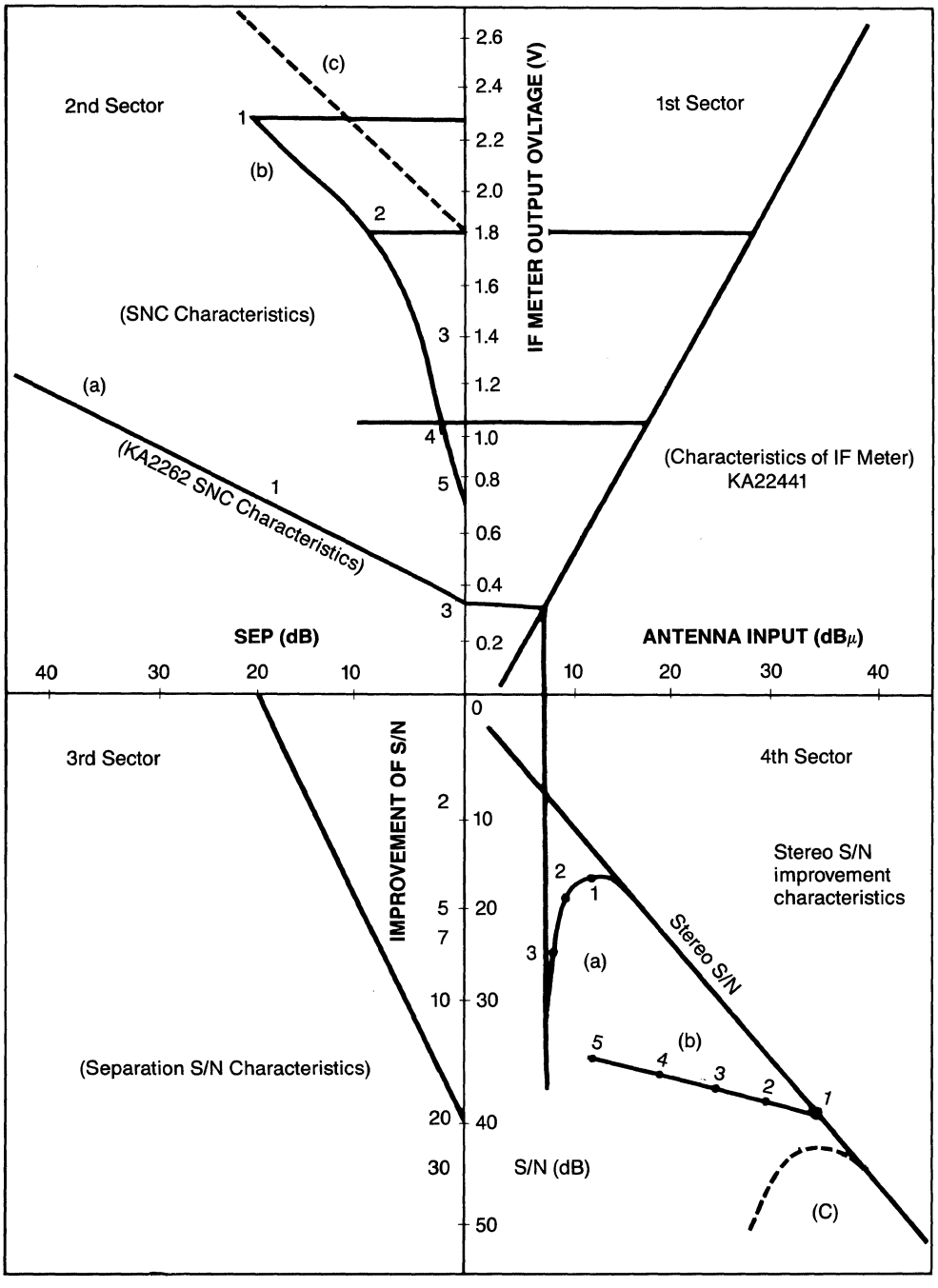


Fig. 8

WORKING AREA OF SNC AND HCC

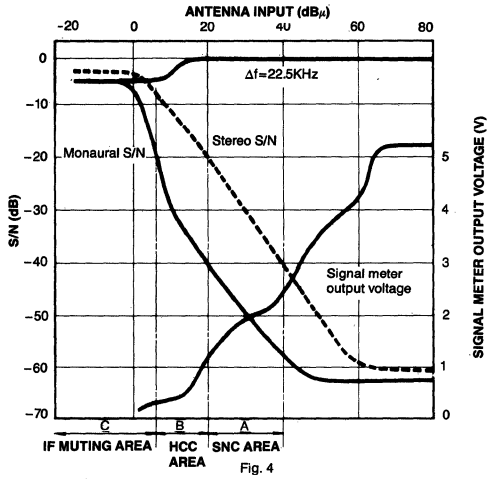


Fig. 4

RELATIONSHIPS BETWEEN SEPARATION AND S/N IMPROVEMENT

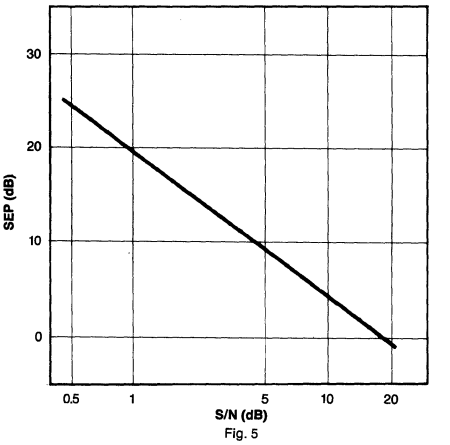
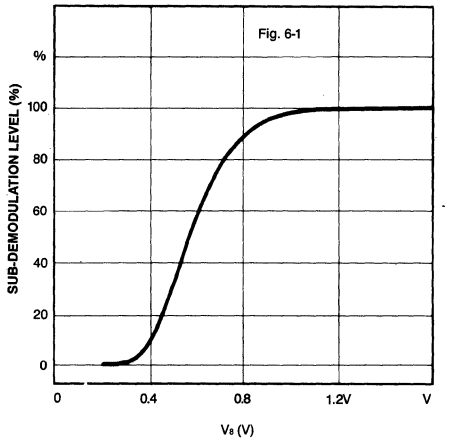


Fig. 5

SNC CHARACTERISTICS (SUB-LEVEL)



KA2262 SNC CHARACTERISTICS

SNC CHARACTERISTICS (SEPARATION)

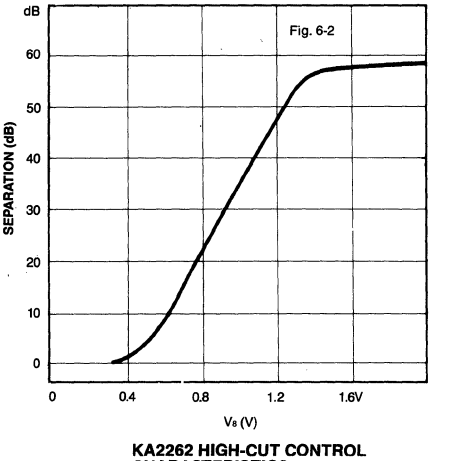


Fig. 6

SNC/HCC CONTROL PIN CURRENT

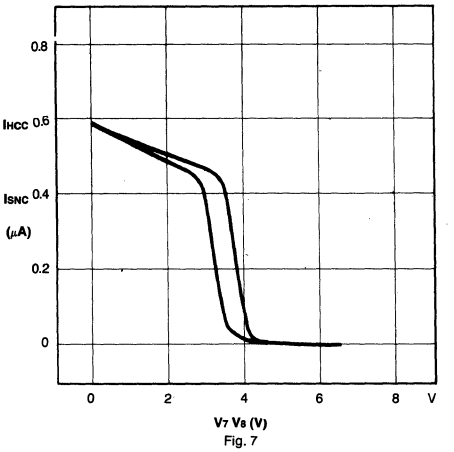


Fig. 7

KA2262 HIGH-CUT CONTROL CHARACTERISTICS

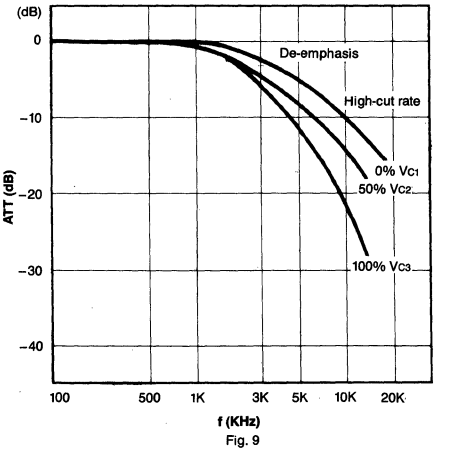


Fig. 9

KA2262 HCC CHARACTERISTICS

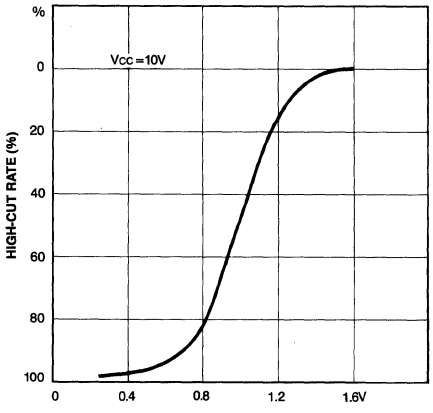


Fig. 10

CHARACTERISTICS OF CURRENT AT VCO STOP FUNCTION CONTROL TERMINAL

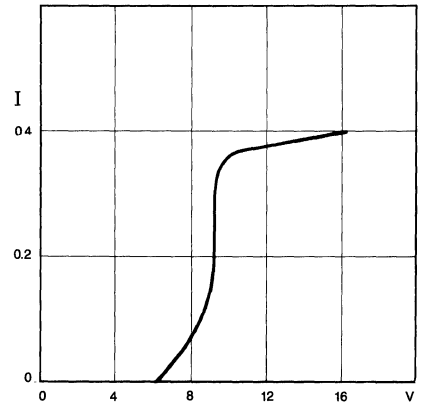
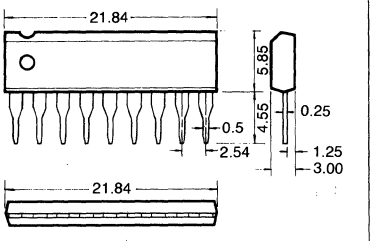


Fig. 11

FM STEREO MULTIPLEX DECODER

The KA2263 is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator. It was designed for use in car stereo, cassette recorder and other equipment.

9 Sip Unit: mm



FEATURES

- **Wide operating supply voltage range (3V ~ 12V).**
- **High pilot lamp ON sensitivity.**
  V_L (on)=9mV (Typ).
- **Built-in stereo indicator lamp drive circuit.**
  Maximum lamp current: 30mA (continuous).
- **High channel separation: Sep=45dB (Typ).**
- **Low distortion**
  THD=0.08% (Typ) at V_i=200mV.
- **VCO stop and stereo lamp turn off are simultaneously operated by connected pin 7 to V_{CC}.**
- **Minimum number of external parts required.**

TYPICAL APPLICATION CIRCUIT

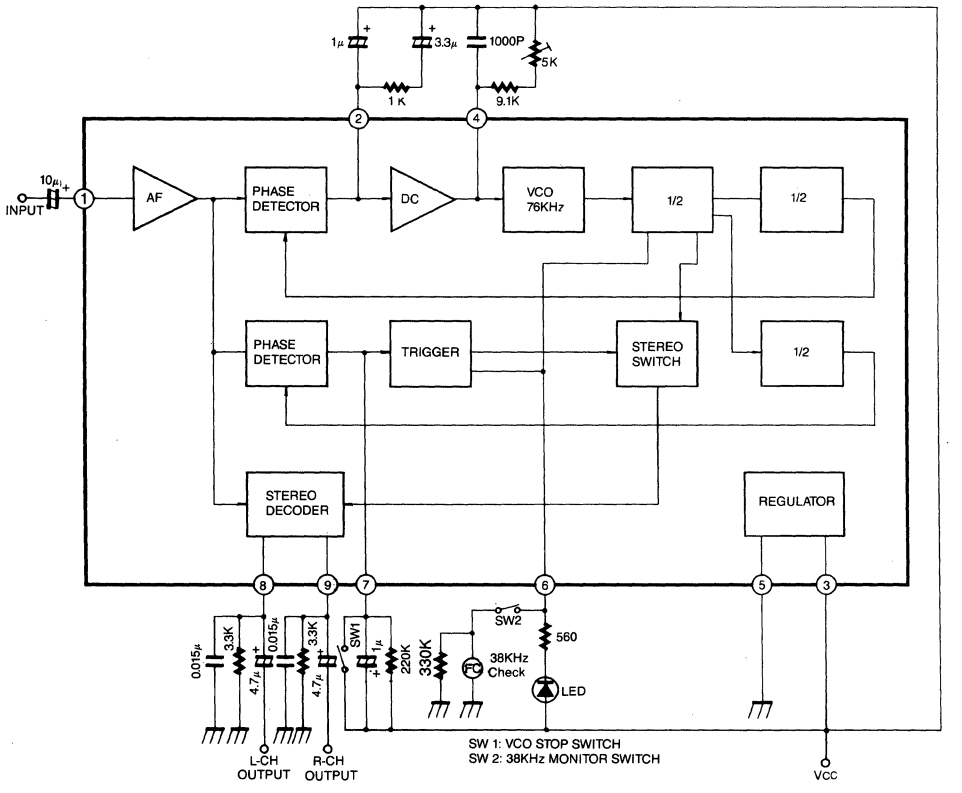


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	V
Lamp Voltage	V_{LAMP}	16	V
Lamp Current	I_L (continuous)	30	mA
	I_L (peak)	50	mA
Power Dissipation	P_d	500	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temeprature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =8V, f=1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	V_i =0		11	18	mA
Input Impedance		R_i			33		KΩ
Maximum Input Level		V_i (max)	L+R=90%, P=10%, THD=1%		550		mV
Channel Separation		Sep	L+R=180mV P=20mV	36	45		dB
Total Harmonic Distortion	Mono	THD 1	V_i =200mV		0.08	0.3	%
	Stereo	THD 2	L+R=180mV P=20mV		0.08		%
Voltage Gain		A_V	V_i =200mV	−2.0	0	+2.0	dB
Channel Balance		C.B	V_i =200mV		0	1.5	dB
Lamp ON Level		V_L (on)	Pilot only		9	15	mV
Lamp OFF Level		V_L (off)	Pilot only	2	6		mV
Lamp Hysteresis		HY			3		mV
Carrier Leak	19KHz	CL	L+R=180mV		34		dB
	38KHz		P=20mV		42		dB

TEST CIRCUIT

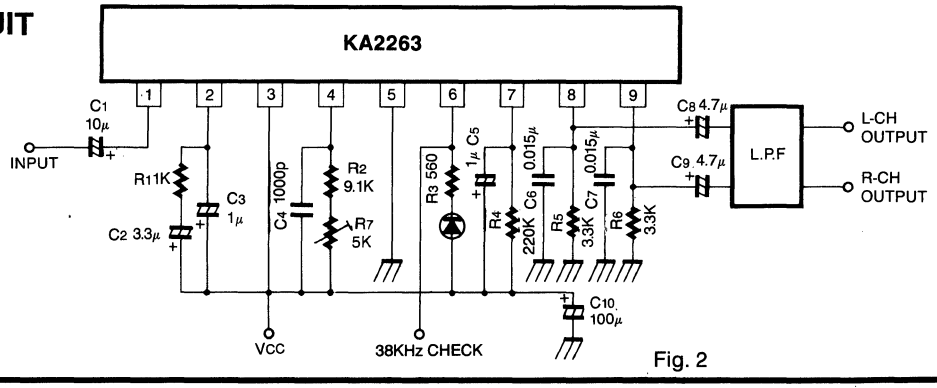
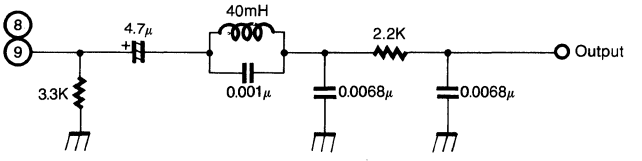
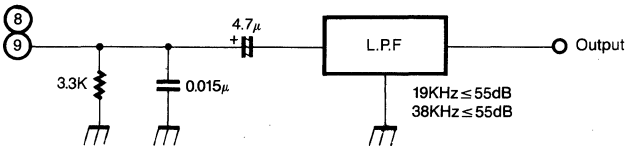


Fig. 2

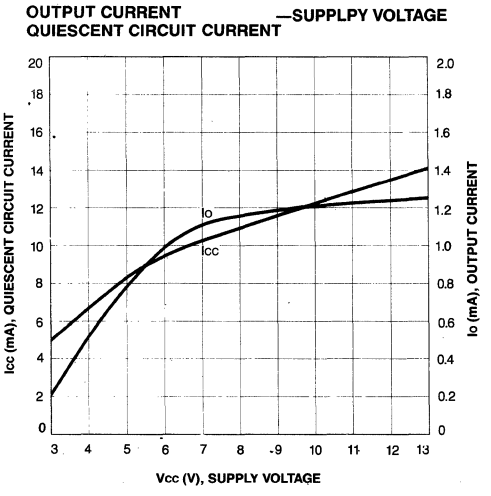
External Components (Refer to test circuit)

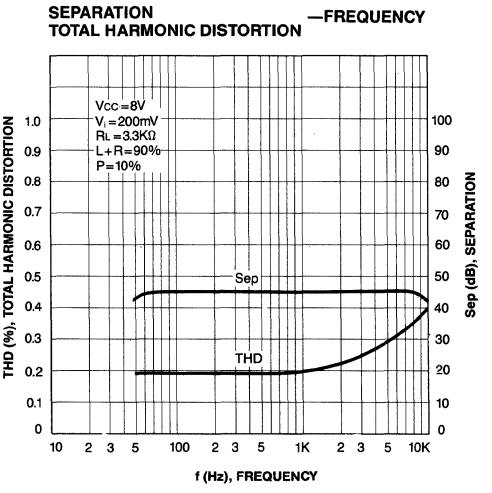
1. Input coupling capacitor (C_1)
   The recommended value is 10μF. If smaller vlaues than 10μF are used low frequency separation will worsen, and if larger values are used pop noise occured high.
2. Low pass filter (C_2, C_3, R_1)
   This is the low pass filter for the PLL, which is determined the capture range and THD at low frequency.
3. VCO network (C_4, R_2, R_7)
   The VCO free running frequency is adjusted by connecting a frequency counter to monitor the 38KHz output pin 6.
4. Decoder output (Pin 8, 9)
   These components provide R and L channel output load circuits. The recommended circuits are follow.



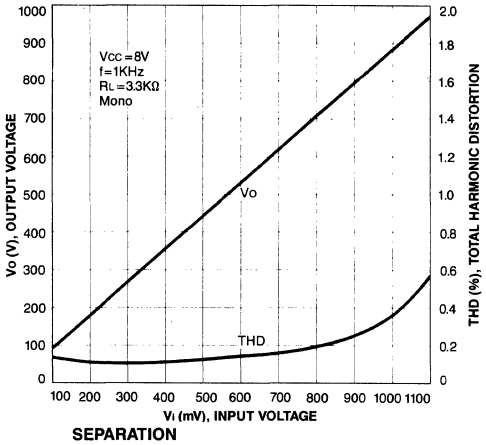


5. Lamp sensitivity control (R_4)
   Lamp on level can be controlled by this resistor.

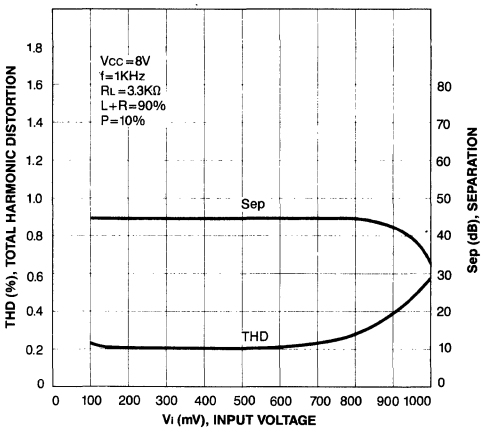




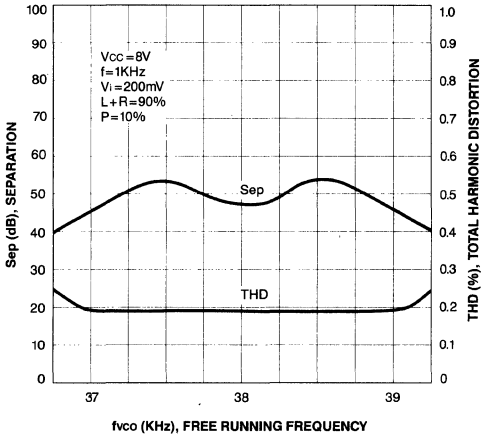
OUTPUT VOLTAGE TOTAL HARMONIC DISTORTION —INPUT VOLTAGE



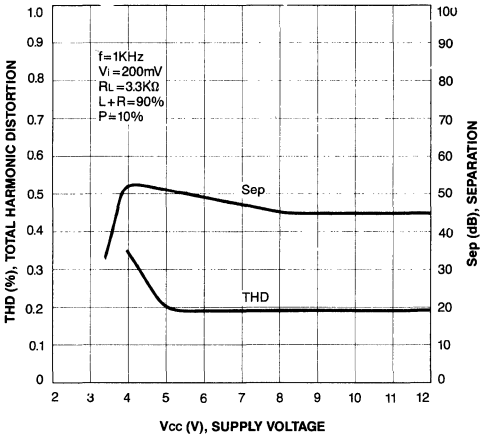
SEPARATION TOTAL HARMONIC DISTORTION —INPUT VOLTAGE



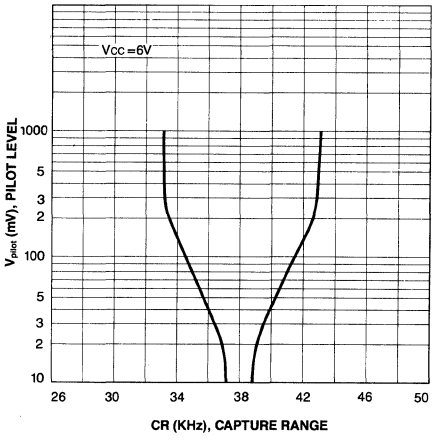
SEPARATION TOTAL HARMONIC DISTORTION —FREE RUNNING FREQUENCY



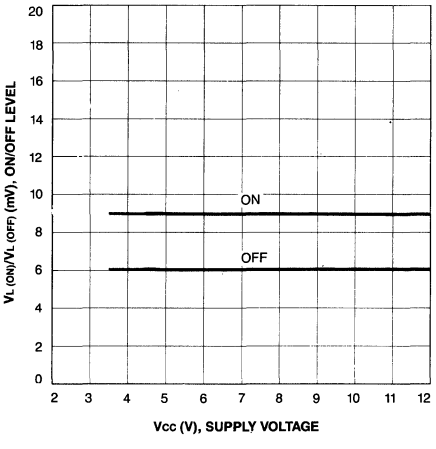
SEPARATION TOTAL HARMONIC DISTORTION --SUPPLY VOLTAGE



CAPTURE RANGE



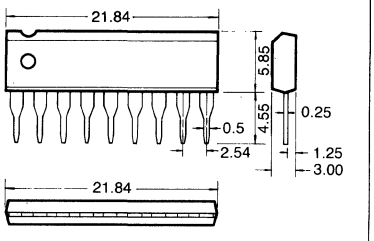
LAMP ON/OFF LEVEL-SUPPLY VOLTAGE



FM STEREO MULTIPLEX DECODER

The KA2263N is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator. It was designed for use in car stereo, cassette recorder and other equipment.

9 Sip Unit: mm



FEATURES

- **Wide operating supply voltage range (3V ~ 12V).**
- **High pilot lamp ON sensitivity.**
  V_L (on)=9mV (Typ).
- **Built-in stereo indicator lamp drive circuit.**
  Maximum lamp current: 30mA (continuous)
- **High channel separation: Sep=45dB (Typ).**
- **Low distortion**
  THD=0.08% (Typ) at V_i = 200mV.
- **VCO stop and stereo lamp turn off are simultaneously operated by connected pin 7 to V_{CC}.**
- **Minimum number of external parts required.**

TYPICAL APPLICATION CIRCUIT

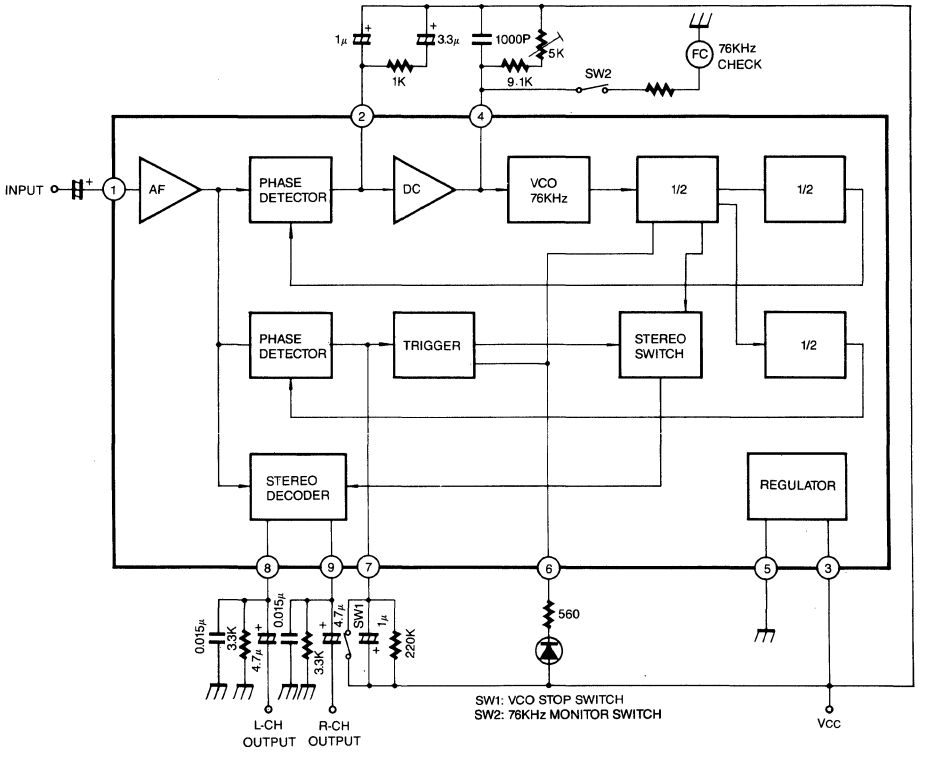


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

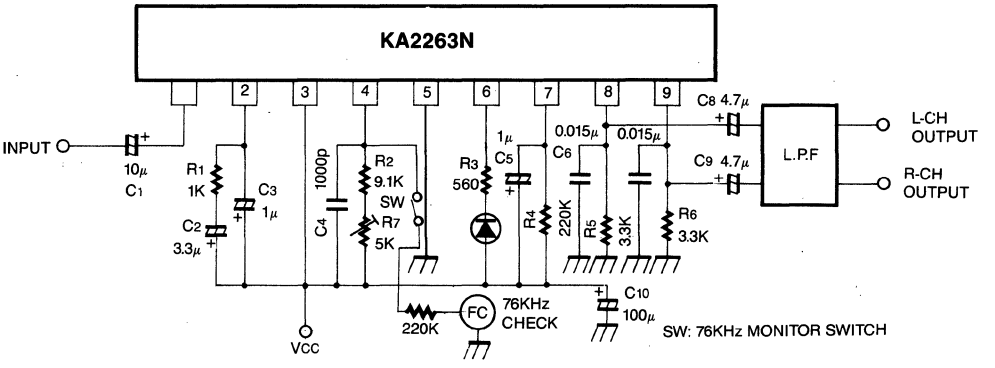
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	V
Lamp Voltage	V_{LAMP}	16	V
Lamp Current	I_{LAMP} (continuous)	30	mA
	I_{LAMP} (peak)	50	mA
Power Dissipation	P_d	500	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =8V, f=1KHz)

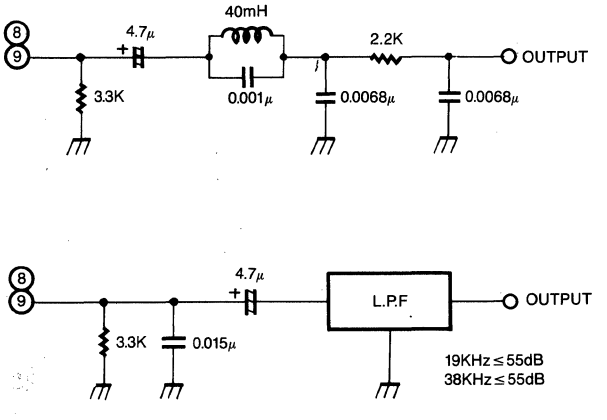
Characteristic		Symbol	Test Condition		Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i =0			11	18	mA
Input Impedance		R_{in}				33		KΩ
Maximum Input Level		V_i (max)	L+R=90%, P=10%, THD=1%			550		mV
Channel Separation		Sep	L+R=180mV, P=20mV		36	45		dB
THD	Mono	THD 1	V_i =200mV			0.08	0.3	%
	Stereo	THD 2	L+R=180mV, P=20mV			0.08		%
Voltage Gain		A_V	V_i =200mV		−2.0	0	+2.0	dB
Channel Balance		C.B.	V_i =200mV			0	1.5	dB
Lamp Level	On	V_L (on)	Pilot only			9	15	mV
	Off	V_L (off)	Pilot only		2	6		mV
Lamp Hysterisis		HY				3		mV
Carrier Leak	19KHz	C.L.	L+R=180mV P=200mV			34		dB
	38KHz					42		
SCA Rejection		SCA_{Rej}	P=20mV, L+R=160mV SCA=20mV f_{SCA} =67KHz			70		dB
S/N		S/N	V_i =200mV f=1KHz, R_g =620Ω			74		dB
Pin 8, Pin 9 Output Current		I_{out}	R_L =3.3KΩ	V_{CC} =3.0V		0.2	0.4	mA
				V_{CC} =8.0V		1.2	1.8	
				V_{CC} =12V		1.4	2.1	

TEST CIRCUIT



External Components (Refer to test circuit)

1. Input coupling capaciter (C_1)
   The recommended value is 10μF. If smaller vlaues than 10μF are used low frequency separation will worsen, and if larger values are used pop noise occured high.
2. Low pass filter (C_2, C_3, R_1)
   This is the low pass filter for the PLL, which is determined the capture range and THD at low frequency.
3. VCO network (C_4, R_2, R_7)
   The VCO free running frequency is adjusted by conneting a frequency counter to monitor the 76KHz output pin 4.
4. Decoder output (Pin 8, 9)
   These components provide R and L channel output load circuits. The recommended circuits are follow.

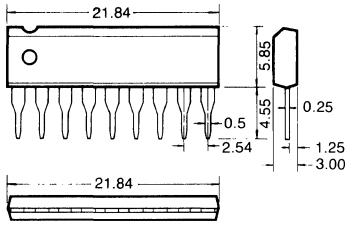


5. Lamp sensitivity control (R_4)
   Lamp on level can be controlled by this resistor.

FM STEREO MULTIPLEX DECODER

The KA2264 is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator. It is designed for use in 3V radio cassette recorder.

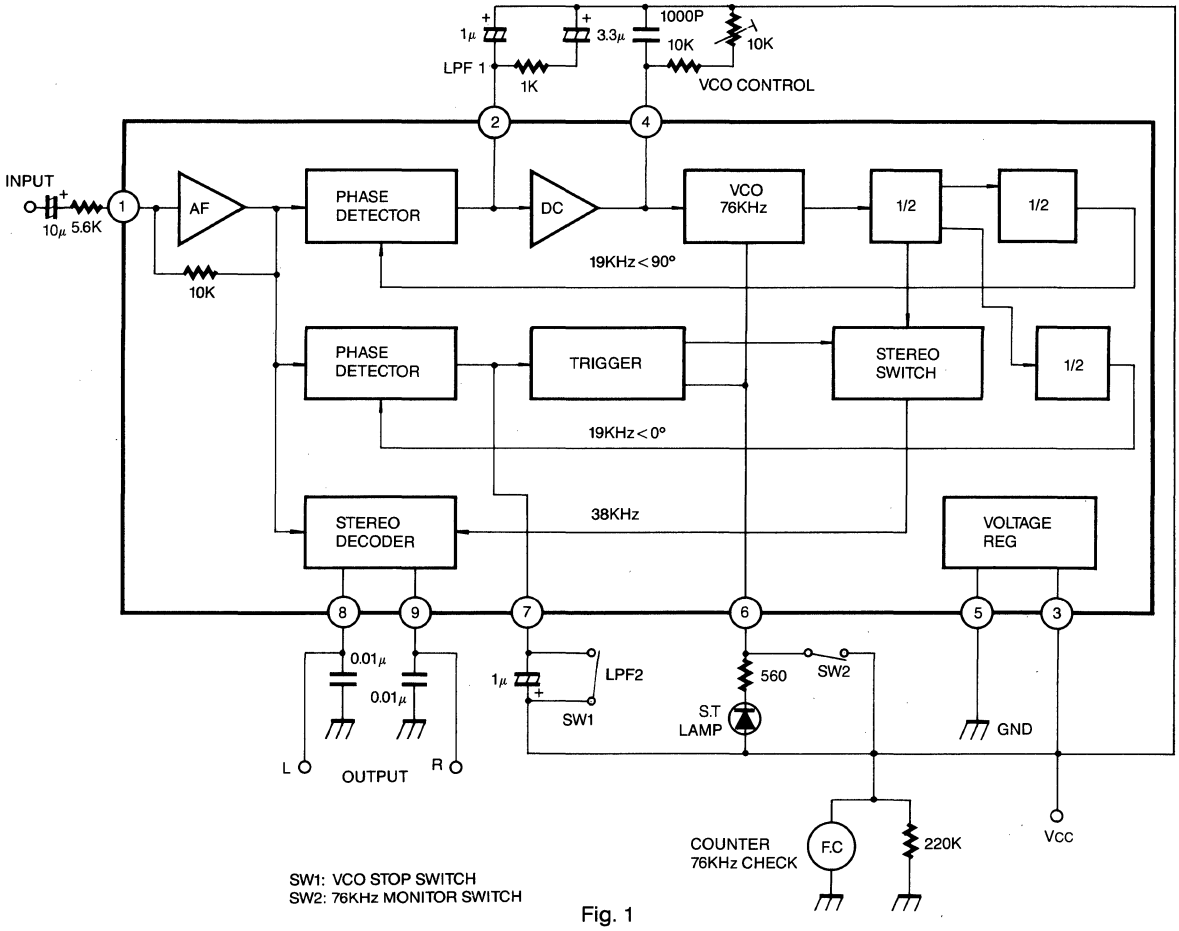
9 Sip Unit: mm



FEATURES

- **Low voltage operation: V_{CC} =1.8V ~ 5V.**
- **Excellent space-factor: 9 SIP.**
- **Minimum number of external parts required.**
- **Easy monitoring of VCO free running frequency is available at pin 6.**
- **High pilot sensitivity: V_L (on)=9mV (typ).**
- **Led drive current: max lamp current=8mA.**
- **VCO stop and stereo lamp turn-off are simultaneously operated by connecting pin 7 to V_{CC}.**

BLOCK DIAGRAM



SW1: VCO STOP SWITCH
SW2: 76KHz MONITOR SWITCH

Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

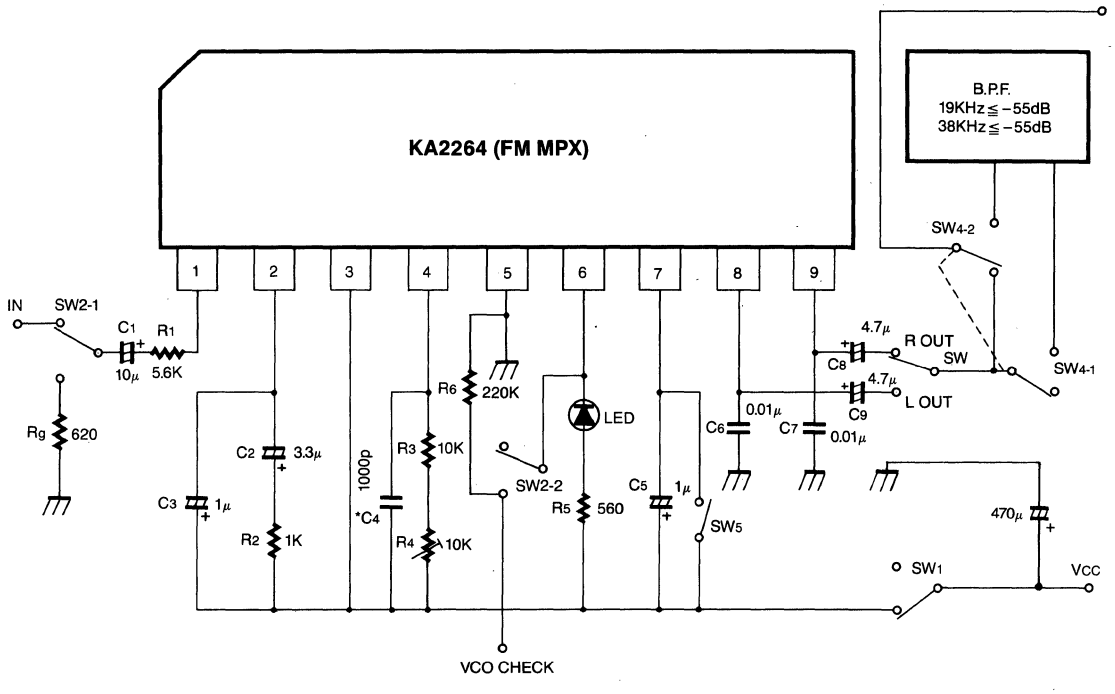
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	6	V
Lamp Voltage	V_{LAMP}	8	V
Lamp Current	I_{LAMP}	8	mA
Power Dissipation	P_d	500	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 3V, f = 1KHz, unless otherwise specified)

Characteristic		Symbol	Test Condition		Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i = 0			4.5	8.0	mA
Input Resistance		R_i				10		KΩ
Output Resistance		R_o			4.0	5.0	6.0	KΩ
Maximum Input Level		V_i (max) Stereo	L+R=90%, P=10% f=1KHz, THD=5%			400		mV
Channel Separation		Sep	L+R=180mV P=20mV	f=100Hz		35		dB
				f = 1KHz	30	35		
				f = 10KHz		35		
Total Harmonic Distortion	Mono	THD 1	V_i = 200mV			0.4	1.0	%
	Stereo	THD 2	L+R=180mV, P=20mV			0.5		
Voltage Gain		A_V	V_i = 200mV		−6.5	−5.0	−3.5	dB
Channel Balance		CB	V_i = 200mV			0	1.5	dB
Lamp Level	ON	V_L (on)	Pilot only			9	15	mV
	OFF	V_L (off)			2	6		
Lamp Hysterisis		HY				3		mV
Capture Range		CR	P=20mV			±3		%
Carrier Leak	19KHz	CL	P=20mV			31		dB
	38KHz		L+R=180mV			60		
SCA Rejection		SCA_{Rej}	P=20mV L+R=160mV SCA=20mV f_{SCA}=67KHz			80		dB
Signal to Noise Ratio		S/N	V_i=200mV R_g=620Ω			82		dB

TEST CIRCUIT



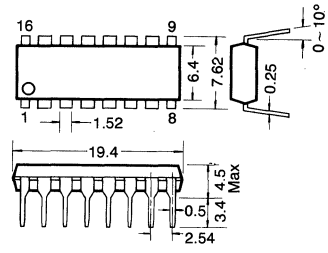
*POLYESTER CONDENSER

Fig. 2

NON-ADJUSTING FM STEREO MULTIPLEX DECODER

The KA2265 is a monolithic integrated circuit consisting of a non-adjusting FM stereo demodulator with a phase locked loop. It is designed for use in home stereo, portable Hi-Fi.

16 Dip Unit: mm



FEATURES

Non-adjusting VCO: adjustment of free-running frequency unnecessary.

- **Excellent temperature characteristics of VCO: ±50°C→±0.1% (typ).**
- **Excellent stereo high frequency distortion. (f=10KHz: 0.06% (typ)).**
- **Excellent distortion: f=1KHz, V_i=300mV, mono: 0.025% (typ). stereo: 0.02% (typ).**
- **High S/N: 91dB (typ) (mono V_i=300mV, LPF). 92dB (typ) (mono V_i=300mV, IHF BPF).**
- **High gain: about 8.5dB.**
- **Wide dynamic range: mono 800mV (f=1KHz, THD=1%).**
- **Good ripple rejection: 34dB (typ).**
- **Operating voltage range: V_{CC} = 6.5V ~ 14V .**

BLOCK DIAGRAM

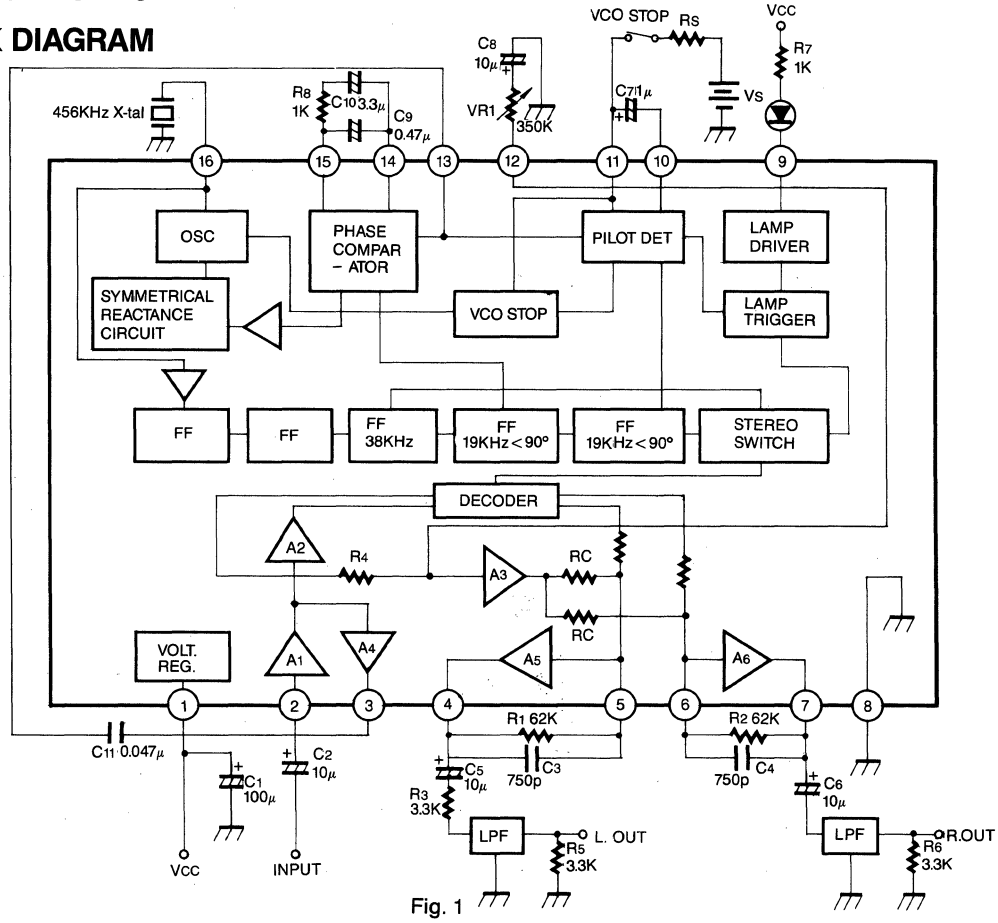


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	16	V
Lamp Current	I_L	30	mA
Power Dissipation	P_d	480	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

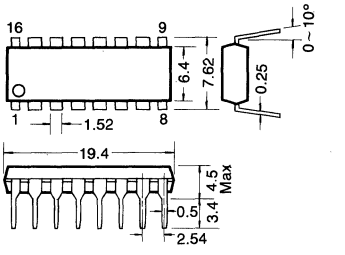
(V_{CC} = 12V, f = 1KHz, T_a = 25°C, unless otherwise specified)

Characteristic		Symbol	Test Condition		Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i=0			18.5	28	mA
Channel Separation		S_{eP}	P=30mV, L+R=270mV	f=100Hz		45		dB
				f=1KHz	40	55		
				f=10KHz		42		
Total Harmonic Distortion	Stereo	THD 1	P=30mV L+R=270mV	f=100Hz		0.025	0.15	%
				f=1KHz		0.02		
				f=10KHz		0.06	0.15	
	Mono	THD 2	V_i=300mV			0.025	0.15	
Output Voltage		V_O	V_i=300mV		500	730	1000	mV
Channel Balance		CB	V_i=300mV			0	1	dB
Lamp ON Level		V_L (on)			4	8	17	mV
Lamp Hysteresis		HY				3		dB
Capture Range		CR	P=30mV			+0.8 −1.2		%
Signal to Noise Ratio		S/N	V_i=300mV R_g=5.1KΩ		80	91		dB
Input Impedance		R_i				20		KΩ
Maximum Input Level		Vi (max)	Mono, THD=1%		700	800		mV
Carrier Leak		CL	P=30mV, L+R=270mV			31		dB
VCO Stop Voltage		VCO_{stop}			5.5		V_{CC}-3	V
Ripple Rejection		RR				34		dB

5 DOT DUAL LED LEVEL METER DRIVER

The KA2281 is a monolithic integrated circuit consisting of 2 channel LED level meter driver which was design for use in stereo radio cassette tape recorder and home stereo.

16 Dip Unit: mm



FEATURES

- **Suitable for AC level (−16, −11, −6, −3, 0dB)×2.**
- **Capable of driving red/green/yeollow LEDs.**
- **Externally adjustable gain of input amplifier.**
- **Wide operating supply voltage range (5V ~ 14V).**
- **10 dot dual output combinated with KA2283.**
- **Applicable to 10 dot mono output.**
- **High input impedance.**
- **Minimum number of external parts required.**

TYPICAL APPLICATION CIRCUIT

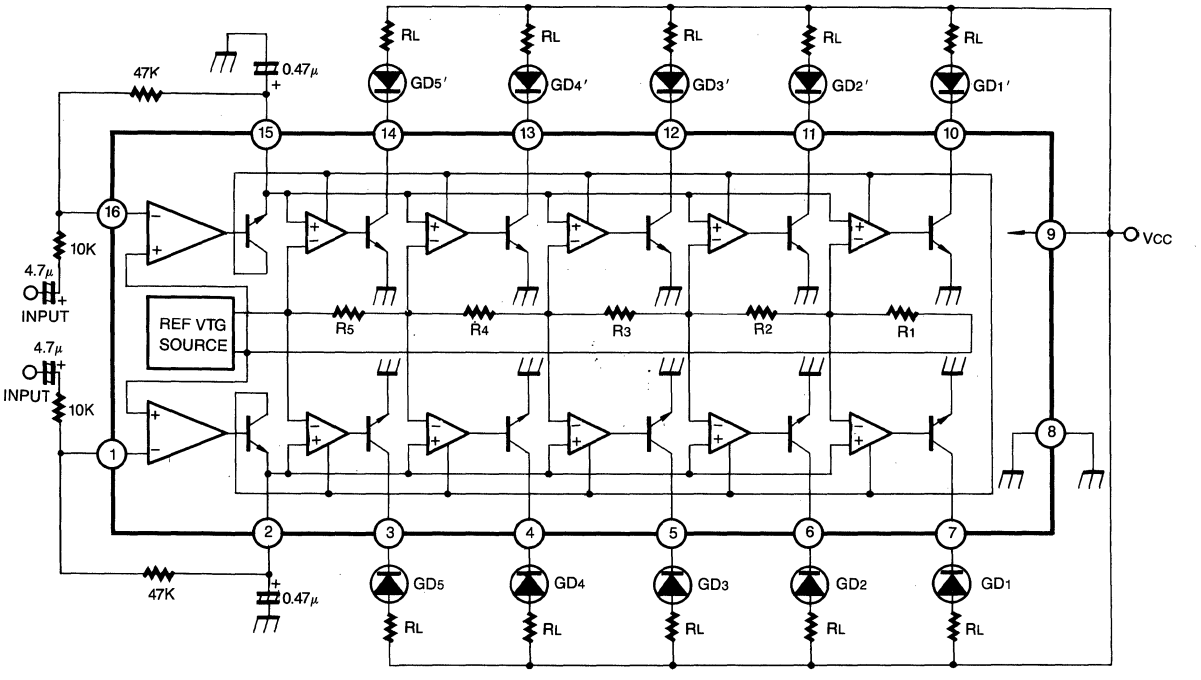


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
D Terminal Output Current	I_D	30	mA
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=12V, f=1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		4		mA
D Terminal ON Voltage	V_{OL}	I_O=20mA		1.5		V
D Terminal Leakage Current	I_O (off)	V_i=0			50	μA
Voltage Gain (Closed Loop)	A_V			13.4		dB
Comparator ON Level	GD_5 GD_5'	A_V=13.4dB	−1	−0	−1	dB
	GD_4 GD_4'		−4	−3	−2	
	GD_3 GD_3'		−7.5	−6	−4.5	
	GD_2 GD_2'		−13	−11	−9	
	GD_1 GD_1'		−19	−16	−13	
LED ON Level Difference	$\Delta GD_{1\text{-}5}$	$GD_{1\text{-}5}$-$GD'_{1\text{-}5}$ A_V=13.4dB	−1	0	1	dB
Input Impedance of Amp	R_i			200		KΩ

* Definition of 0dB; when the value of Input voltage is 218mVrms

TYPICAL APPLICATIONS

1. 5 dot dual application

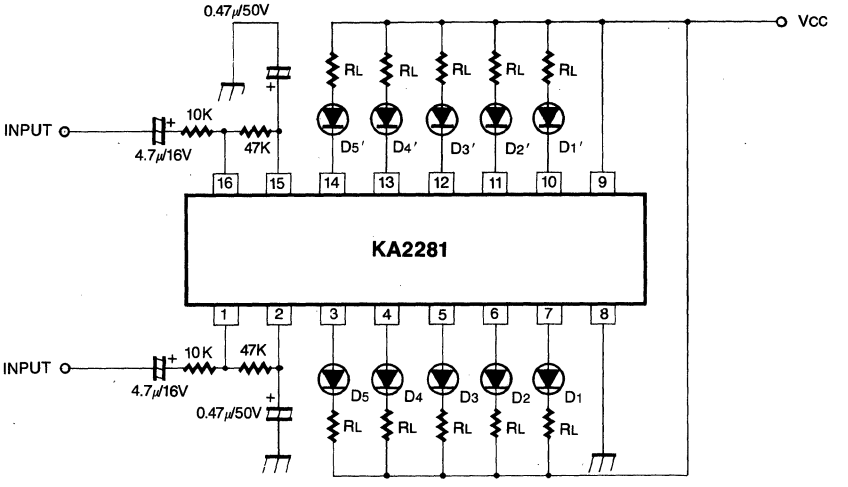


Fig. 2

2. 10 dot mono application

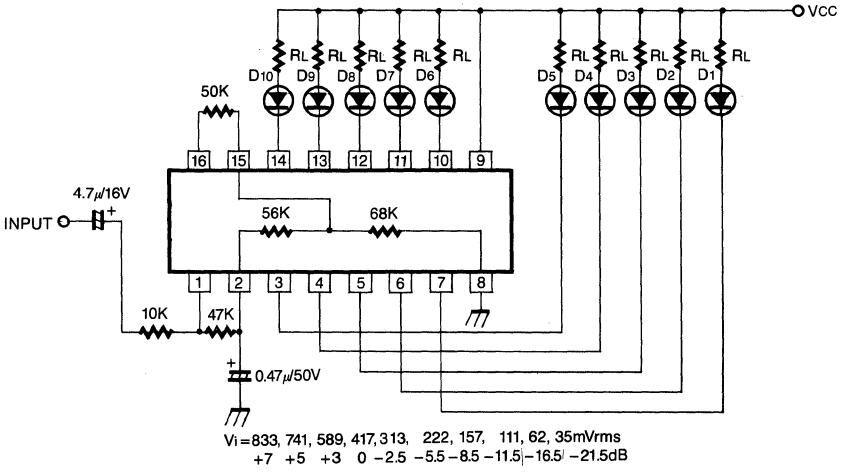
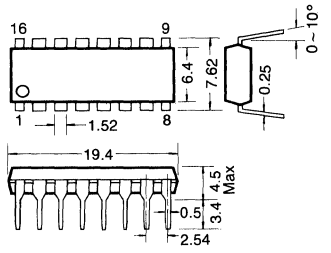


Fig. 3

5 DOT DUAL LED LEVEL METER DRIVER

The KA2283 is a monolithic integrated circuit consisting of 2 channel LED level meter driver which was designed for use in stereo radio cassette tape recorder and home stereo.

16 Dip Unit: mm



FEATURES

- **Suitable for AC level meter driver.**
- **Comparator level (−8, −6, −4, −2, 0dB)×2.**
- **Capable of driving red/green/yellow LEDs.**
- **Externally adjustable gain of input amp.**
- **Wide operating supply voltage range (5V ~ 14V).**
- **10 dot dual output combinated with KA2281.**
- **Applicable to 10 dot mono output.**
- **High input inpedance.**
- **Minimum number of external parts required.**

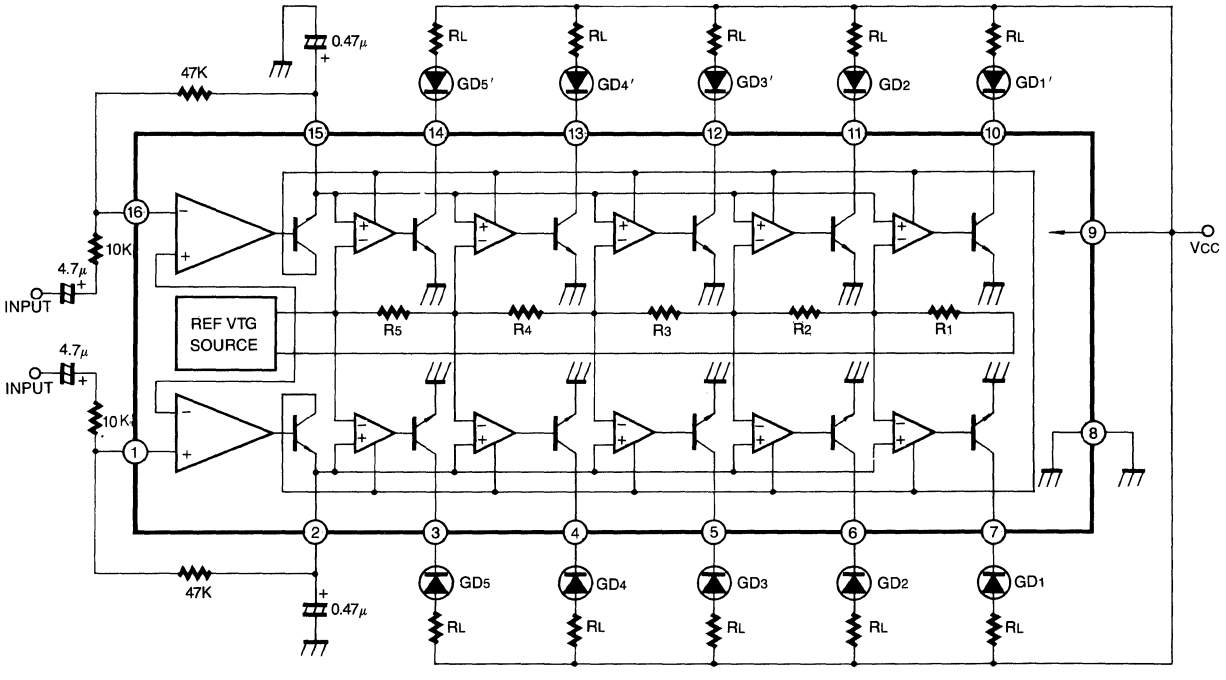


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
D Terminal Output Current	I_D	30	mA
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =12V, f=1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i =0		4		mA
D Terminal ON Voltage	V_{OL}	I_O =20mA		1.5		V
D Terminal Leakage Current	I_O (off)	V_i =0			50	μA
Voltage Gain (Closed Loop)	A_V			13.4		dB
Comparator ON Level	GD_5 GD_5'	A_V =13.4dB	−1	0	1	dB
	GD_4 GD_4'		−3	−2	−1	
	GD_3 GD_3'		−5	−4	−3	
	GD_2 GD_2'		−7	−6	−5	
	GD_1 GD_1'		−9	−8	−7	
LED ON Level Difference	$\Delta GD_{1\text{-}5}$	$GD_{1\text{-}5}$-$GD'_{1\text{-}5}$ A_V = 13.4dB	−1	0	1	dB
Input Impedance of Amp	R_i			200		KΩ

* Definition of 0dB; when the value of Input voltage is 218mVrms

APPLICATION CIRCUIT

1. 5 dot dual application

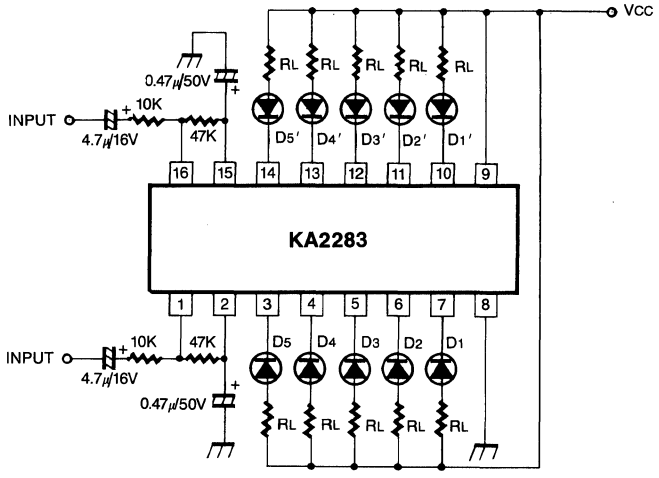
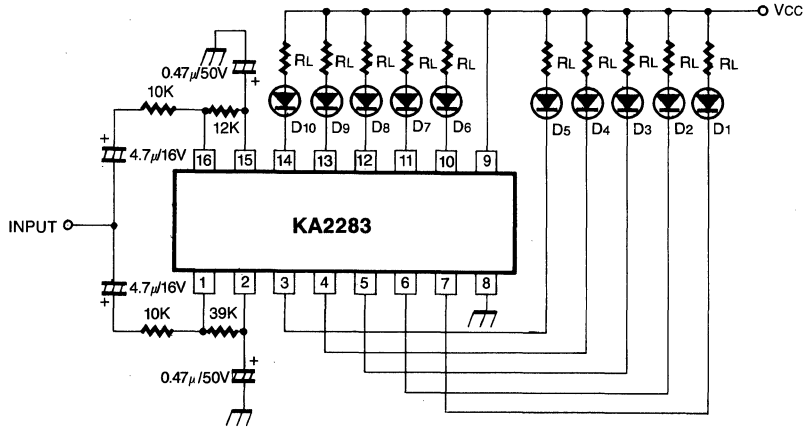


Fig. 2

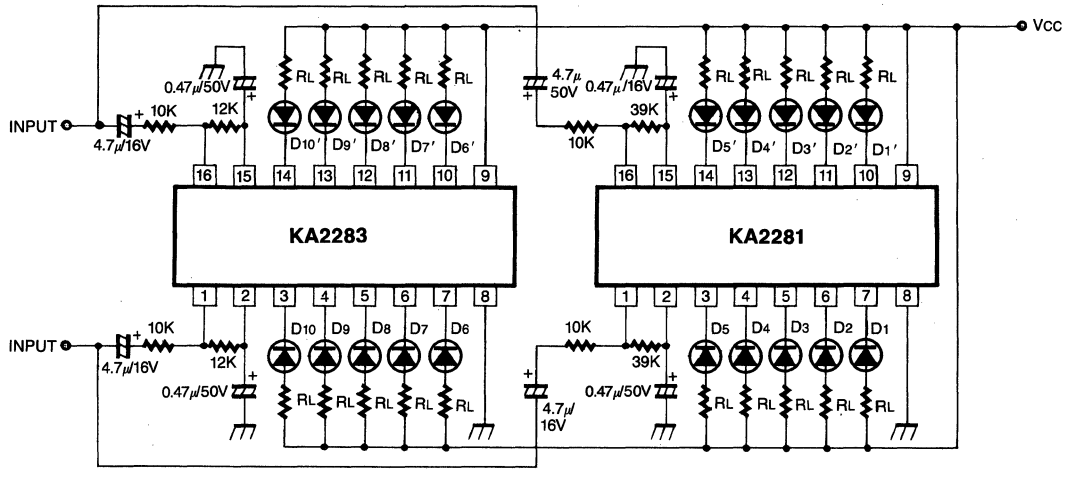
2. 10 dot mono application



Vi = 822, 653, 519, 412, 327, 260, 206, 163, 129, 102mVrms
+6, +4, +2, 0, −2, −4, −6, −8, −10, −12dB

Fig. 3

3. 10 dot dual application with KA2281

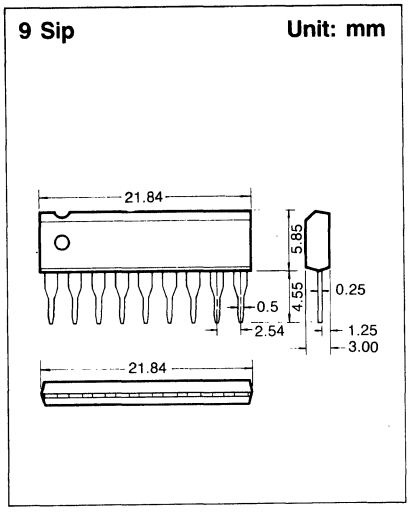


Vi =830, 660, 524, 417, 331, 263, 184, 130, 73, 41mVrms
+6, +4, +2, 0. −2, −4, −7, −10, −15, −20dB

Fig. 4

5 DOT LED VU LEVEL METER DRIVER

The KA2284/KA2285 are a monolithic integrated circuit designed for 5 dot LED level meter driver built-in rectifying amplifier, it is suitable for AC/DC level meter such as VU meter or signal meter.



FEATURES

- **High gain rectifying amplifier included (A_v=26dB).**
- **Low radiation noise when LED turns on.**
- **Logarithmic indicator for 5 dot LED of bar type. (−10, −5, 0, 3, 6dB)**
- **Constant current output. KA2284: I_o=15mA Typ. KA2285: I_o=7mA Typ.**
- **Wide operating supply voltage range (3.5V ~ 16V).**
- **Minimum number of external parts required.**

BLOCK DIAGRAM

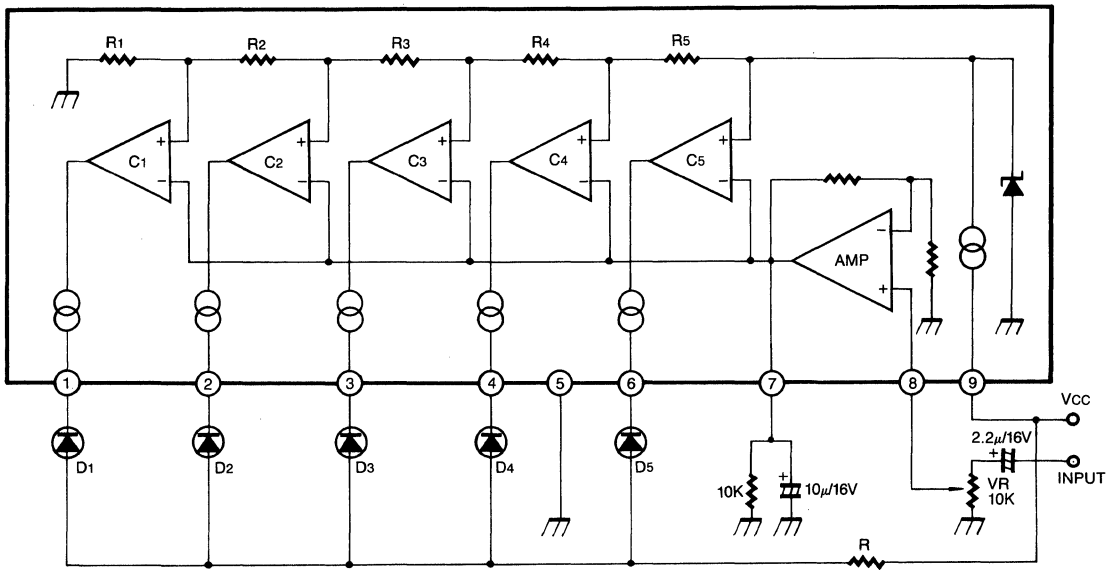


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Amp Input Voltage	$V_{8\text{-}5}$	−0.5 ~ V_{CC}	V
Pin 7 Voltage	$V_{7\text{-}5}$	6	V
D Terminal Output Voltage	V_D	18	V
Circuit Current	I_{CC}	12	mA
C Terminal Output Current	I_D	20	mA
Power Dissipation	P_d	1100	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

−11mW/°C is decreased at higher temperature than T_a =25°C.

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =6V, f=1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i =0V		6	8.5	mA
D Output Current	KA2284	I_O	V_i =0.15V	11	15	18.5	mA
	KA2285			5	7	9.5	
Input Bias Current		I_8		−1		0	μA
Amp Gain		A_V	V_i =0.1V	24	26	28	dB
Comparator ON Level		GD_1		−12	−10	−8	dB
		GD_2		−6	−5	−4	
		GD_3			0		
		GD_4		2.5	3	3.5	
		GD_5		5	6	7	

*Definition of 0dB; input voltage level when GD_3 turn ON.

TYPICAL APPLICATION CIRCUIT

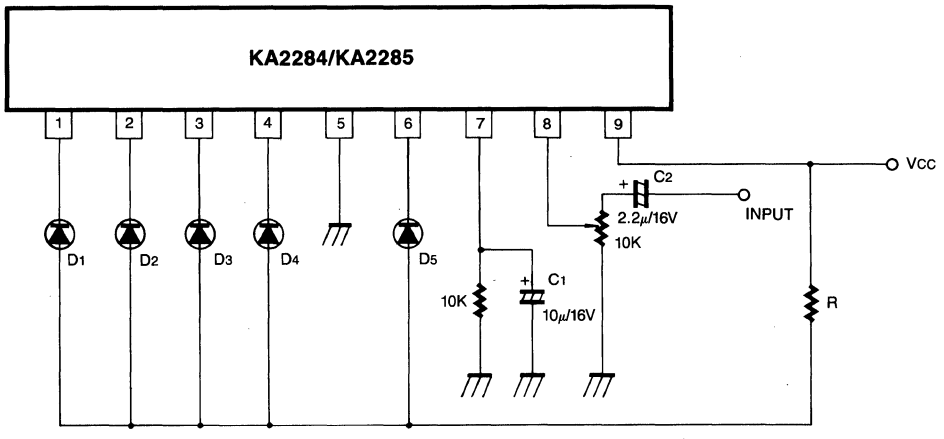


Fig. 2

C2: AC in, 2.2μ is used
DC in, 2.2μ is shorted

The recommended value of R at T_a (max)=60°C

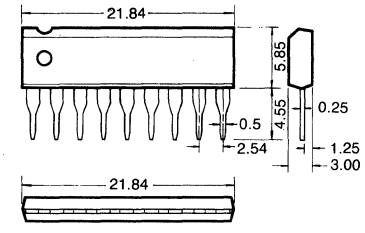
V_{CC} (V)	8 ~ 12	10 ~ 14	12 ~ 16
R (Ω)	47	68	91

By changing the time constant C_1 and C_2, the response time, attack and release time, may be varied. In case of above application conditions, power dissipation may be operated at higher level than absolute maximum ratings.
The wattage of R is to be determined by the total LED current and R value recommended by R table.

5 DOT LED LINEAR LEVEL METER DRIVER

The KA2286/KA2287 are a monolithic integrated circuit designed for 5 dot LED level meter driver built-in rectifying amplifier, it is suitable for AC/DC level meter such as VU meter or signal meter.

9 Sip Unit: mm



FEATURES

- **High gain rectifying amplifier included (A_V=26dB).**
- **Low radiation noise when LED turns on.**
- **Linear indicator for 5 dot LED of bar type. (0.33, 0.67, 1, 1.33, 1.67)**
- **Constant current output. KA2286: I_o=7mA Typ. KA2287: I_o=15mA Typ.**
- **Wide operating supply voltage range (3.5V ~ 16V).**
- **Minimum number of external parts required.**

BLOCK DIAGRAM

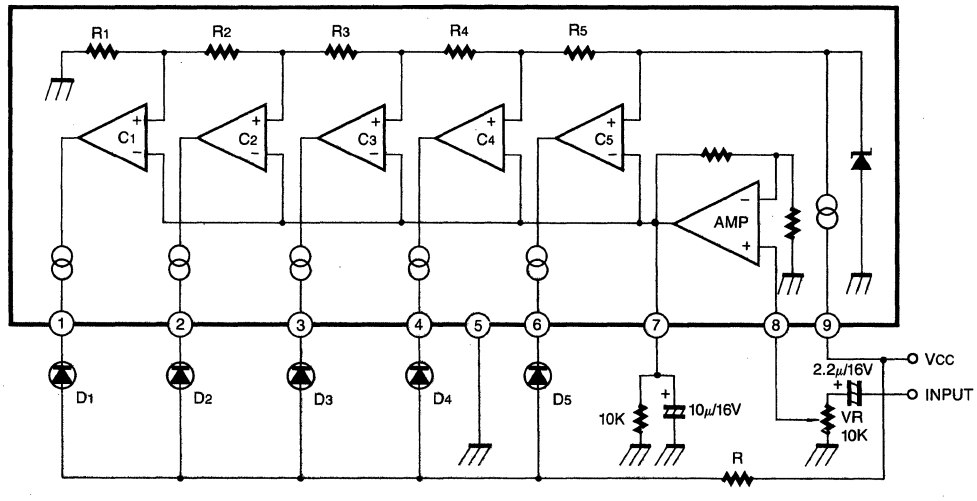


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Amp Input Voltage	$V_{8\text{-}5}$	−0.5 ~ V_{CC}	V
Pin 7 Voltage	$V_{7\text{-}5}$	6	V
D Terminal Output Voltage	V_D	18	V
Circuit Current	I_{CC}	12	mA
C Terminal Output Current	I_D	20	mA
Power Dissipation	P_d	1100	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

−11mW/°C is decreased at higher temperature than T_a = 25°C.

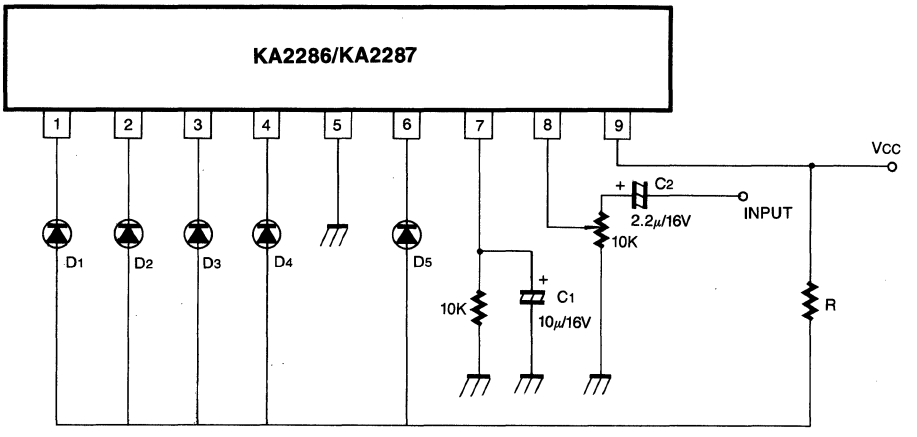
ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 6V, f = 1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	V_i = 0V		6	8.5	mA
D Output Current	KA2286	I_O	V_i = 0.15V	5	7	9.5	mA
	KA2287			11	15	18.5	
Input Bias Current		I_8		−1		0	μA
Amp Gain		A_V	V_i = 0.1V	24	26	28	dB
Comparator On Level		GD_1		0.28	0.33	0.40	V_3
		GD_2		0.59	0.67	0.75	
		GD_3			1		
		GD_4		1.25	1.33	1.42	
		GD_5		1.48	1.67	1.87	

*Definition of 1; pin 3 voltage when GD_3 turn on.

TYPICAL APPLICATION CIRCUIT



C2: AC in, 2.2μ is used
DC in, 2.2μ is shorted

Fig. 2

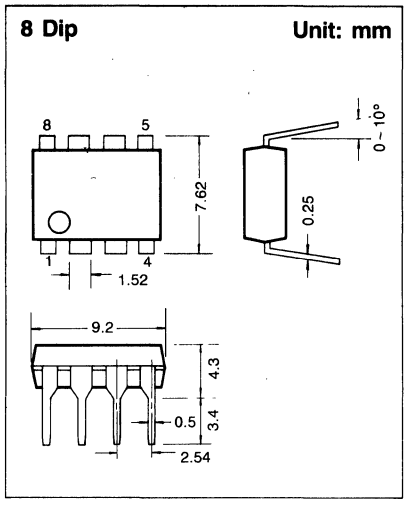
The recommended value of R at T_a (max)=60°C.

V_{CC} (V)	8 ~ 12	10 ~ 14	12 ~ 16
R (Ω)	47	68	91

By changing the time constant C_1 and C_2, the response time, attack and release time, may be varied. In case of above application conditions, power dissipation may be operated at higher level than absolute maximum ratings.
The wattage of R is to be determined by the total LED current and R value recommended by R table.

DC MOTOR SPEED CONTROLLER

The KA2401 is a monolithic integrated circuit designed for DC motor speed controllers.



FEATURES

- **Suitable for DC motor speed controllers of cassette tape recorder and radio cassette.**
- **Excellent stability of each characteristics against ambient temperature.**
- **Low quiescent current (0.8mA; Typ).**
- **Low reference voltage.**
- **Wide operating supply voltage range (4V ~ 12V).**

EQUIVALENT CIRCUIT BLOCK DIAGRAM

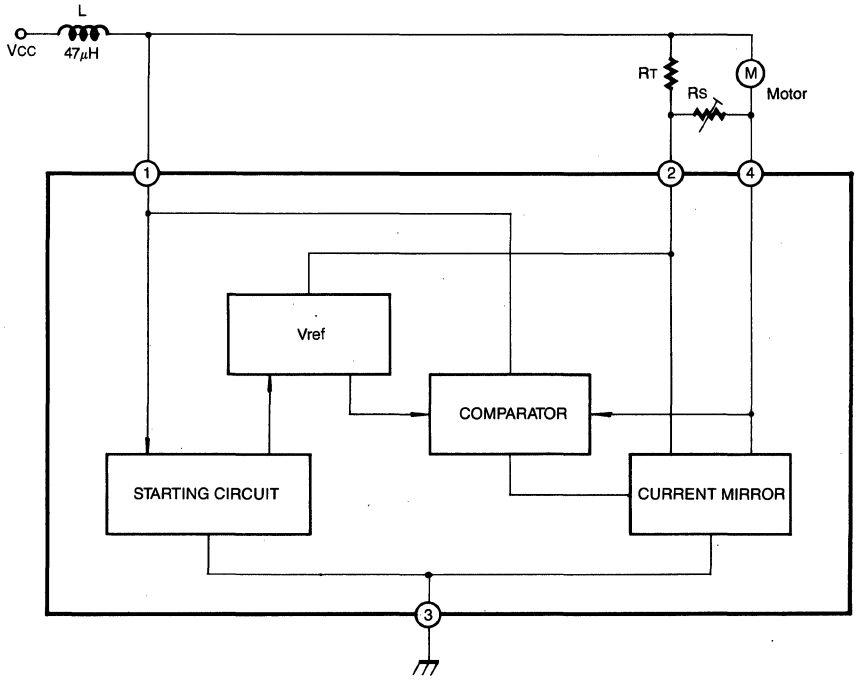


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Circuit Current	I_4	*2	A
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

*t < 5 sec

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =6V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Reference Voltage	Vref	I_4 =10mA	1.10	1.27	1.40	V	2
Quiescent Current	Id	Rm=180Ω	0.5	0.8	1.2	mA	5
Reflection-Coefficient	K	Rm_1 =44Ω, Rm_2 =33Ω	18	20	22		3
Saturation Voltage	V_4 (sat)	V_{CC} =4.2V, Rm=4.4Ω		1.5	20	V	4
Voltage Characteristic	$\frac{\Delta K}{K}/\Delta V_{CC}$	I_4 = 100mA, V_{CC} = 4 ~ 12V		0.4		%/V	3
	$\frac{\Delta Vref}{Vref}/\Delta V_{CC}$	I_4 =100mA, V_{CC} =4 ~ 12V		0.06		%/V	2
Current Characteristic	$\frac{\Delta K}{K}/\Delta I_4$	I_4 =30 ~ 200mA		−0.02		%/mA	3
	$\frac{\Delta Vref}{Vref}/\Delta I_4$	I_4 =30 ~ 200mA		−0.02		%/mA	2
Temperature Characteristic	$\frac{\Delta K}{K}/\Delta T_a$	I_4 =100mA T_a =−20 ~ +75°C		0.01		%/°C	3
	$\frac{\Delta Vref}{Vref}/\Delta T_a$	I_4 =100mA T_a =−20 ~ +75°C		0.01		%/°C	2

TEST CIRCUIT 1

Reference Voltage

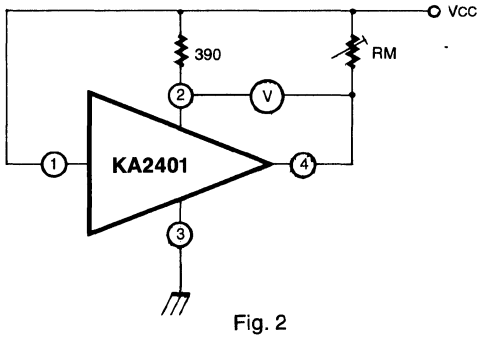


Fig. 2

$$Vref, \frac{\Delta Vref}{Vref}/\Delta Vcc, \frac{\Delta Vref}{Vref}/\Delta I4, \frac{\Delta Vref}{Vref}/\Delta Ta$$

TEST CIRCUIT 2

Reflection Coefficient

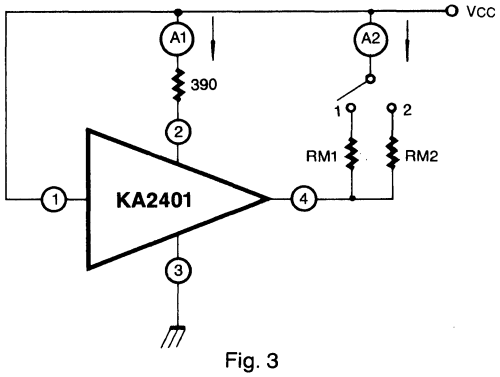


Fig. 3

$$K, \frac{\Delta K}{K}/\Delta Vcc, \frac{\Delta K}{K}/\Delta I4, \frac{\Delta K}{K}/\Delta Ta$$

$$K = \frac{I4\ (SW\ 2) - I4\ (SW\ 1)}{I2\ (SW\ 2) - I2\ (SW\ 1)}$$

TEST CIRCUIT 3

Saturation Voltage

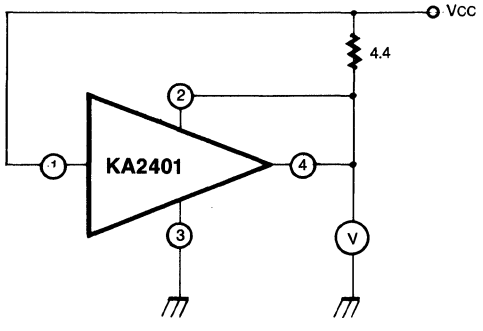
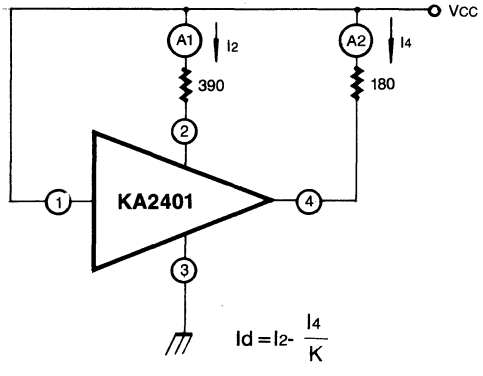


Fig. 4

TEST CIRCUIT 4

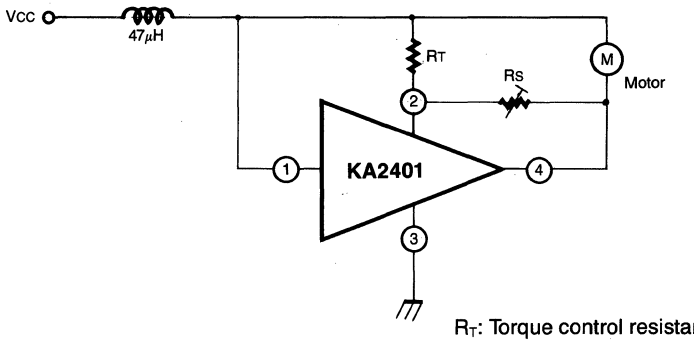
Quiescent Current



$$Id = I2 - \frac{I4}{K}$$

Fig. 5

TYPICAL APPLICATION



R_T: Torque control resistance
R_S: Speed control resistance

Fig. 6

BASIC EQUATION

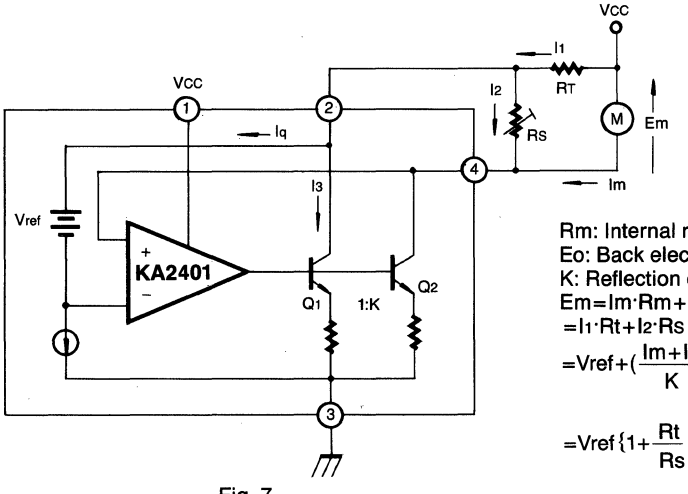


Fig. 7

Rm: Internal resistance of the motor
Eo: Back electronic force
K: Reflection coefficient

$Em = Im \cdot Rm + Eo$

$= I_1 \cdot Rt + I_2 \cdot Rs$

$= Vref + \left(\frac{Im + I_2}{K} + Iq + \frac{Vref}{Rs}\right) \cdot Rt$

$= Vref\left\{1 + \frac{Rt}{Rs}\left(1 + \frac{1}{K}\right)\right\} + Rt \cdot Iq + \frac{Rt}{K} Im$

If, $Rm = \frac{Rt}{K}$ then

$Eo = Vref\left\{1 + \frac{Rt}{Rs}\left(1 + \frac{1}{K}\right)\right\} + Rt \cdot Iq$

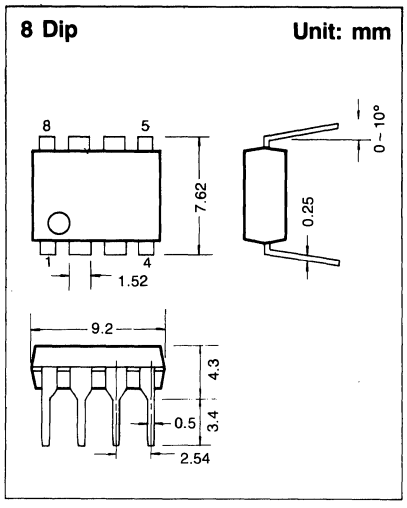
LOW-VOLTAGE DC MOTOR SPEED CONTROLLER

USE

- Speed control or generel-purpose low-voltage compect DC motor for microcassette tape recorder, radio cassette, and the equivelent

FEATURES

- **Wide operating voltage range (1.8V ~ 8V).**
- **Capable of making the applicable set compact because of minimum number of external parts required and compact package.**
- **Easy to adjust speed.**
- **Built-in stable low reference power meeting the requirements for 2 speeds.**
- **Vref=0.2V (KA2402), 0.5V (KA2403).**



EQUIVALENT CIRCUIT BLOCK DIAGRAM

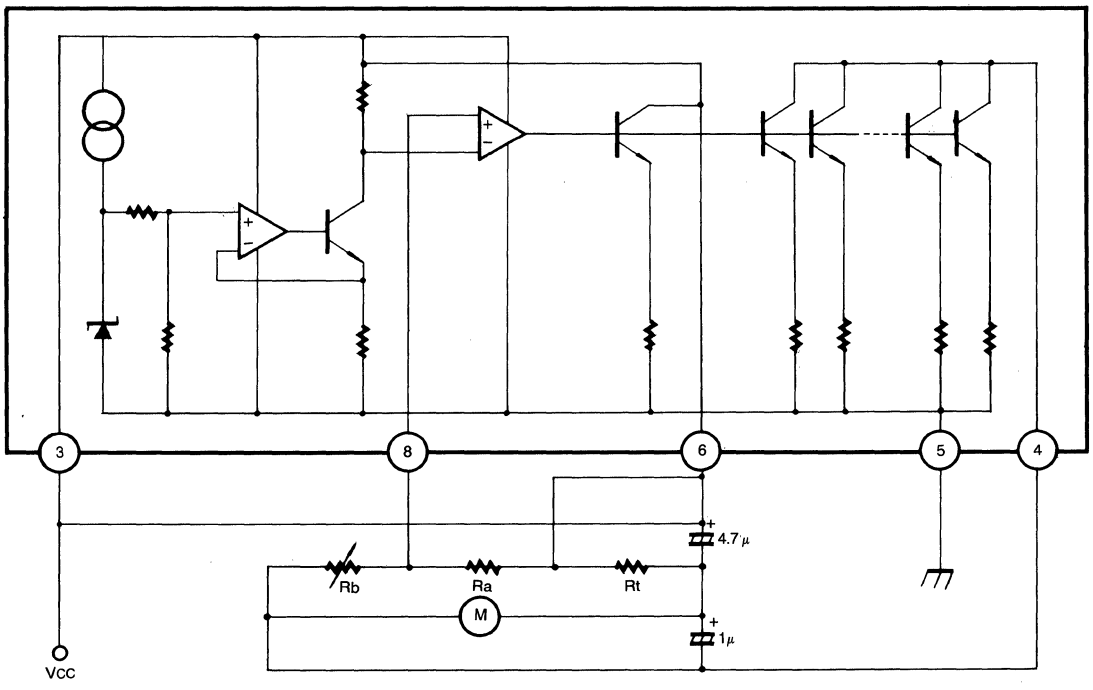


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_A =25°C)

Characteristic	Symbol	Value	Unit
Maximum Supply Voltage	V_{CC}	10	V
Maximum Motor Current	I_M	700	mA
Power Dissipation	P_D	600	mW
Operating Temperature	Topr	−20 ~ +80	°C
Storage Temperature	Tstg	−40 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS (T_A =25°C)

Supply Voltage	V_{CC}	1.8 ~ 8	V
Operating Temperature	Topr	− 20 ~ + 60	°C

ELECTRICAL CHARACTERISTICS (T_A =25°)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Reference Voltage	KA2402	Vref	V_{CC} =3V, I_m =100mA	0.18	0.2	0.22	V
	KA2403			0.44	0.49	0.54	
Circuit Current		I_{CC}	V_{CC} =3V, I_m =100mA		2.4	6.0	mA
Shunt Ratio		K	V_{CC} =3V, I_m =50mA I_m=100mA	45	50	55	
Saturation Voltage		V (sat)	V_{CC} = 3V, I_m = 100mA		0.13	0.3	V
Voltage Characteristic of Reference Voltage		$\frac{\Delta Vref}{Vref}/\Delta V_{CC}$	I_m =100mA V_{CC} =1.8 ~ 8V		0.1		%/V
Voltage Characteristic of Shunt Ratio		$\frac{\Delta K}{K}/\Delta V_{CC}$	I_m =50, 150mA V_{CC} = 1.8 ~ 8V		0.3		%/V
Current Characteristic of Reference Voltage		$\frac{\Delta Vref}{Vref}/\Delta I_m$	V_{CC} =3V I_m =20-200mA		0.005		%/mA
Current Characteristic of Shunt Ratio		$\frac{\Delta K}{K}/\Delta I_m$	V_{CC} =3V, I_m =20, 50mA ~170, 200mA		− 0.07		%/mA
Temperature Characteristic of Reference Voltage		$\frac{\Delta Vref}{Vref}/\Delta T_a$	V_{CC} =3V, I_m =100mA T_A =−20 ~ +80°C		− 0.008		%/°C
Temperature Characteristic of Shunt Ratio		$\frac{\Delta K}{K}/\Delta T_a$	V_{CC} =3V, I_m =50, 150mA T_A =−20 ~ +80°C		0.02		%/°C

TEST CIRCUIT

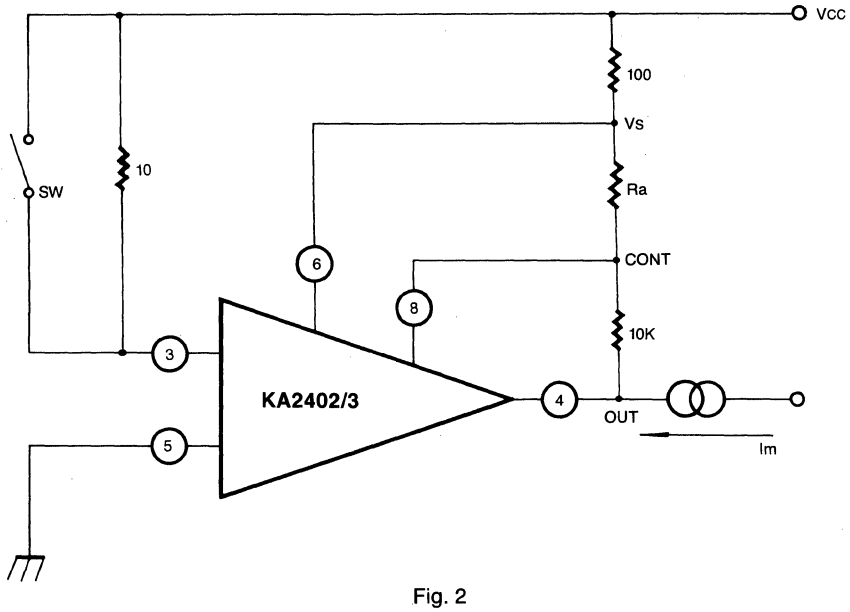


Fig. 2

TEST METHOD

1. V_{ref} : With SW turned on, measure the voltage developed across Ra.
2. I_{CC} : With SW turned off, measure I_{CC} for the voltage developed across resistor 10.00 ohm.
3. K : With SW turned on, measure current I_{50} flowing through resistor 100 ohm at I_m=50mA and current I_{150} flowing through resistor 100 ohm at I_m=150mA, and obtain K by use of the following equation.

$$K = \frac{100mA}{(I_{150} - I_{50})\ (mA)}$$

4. V (sat) : With SW turned on, set V_{CC}=V_S=CONT=3V and feed I_m=100mA, and measure the voltage developed across pins 4 and 5.

Application Circuit 1

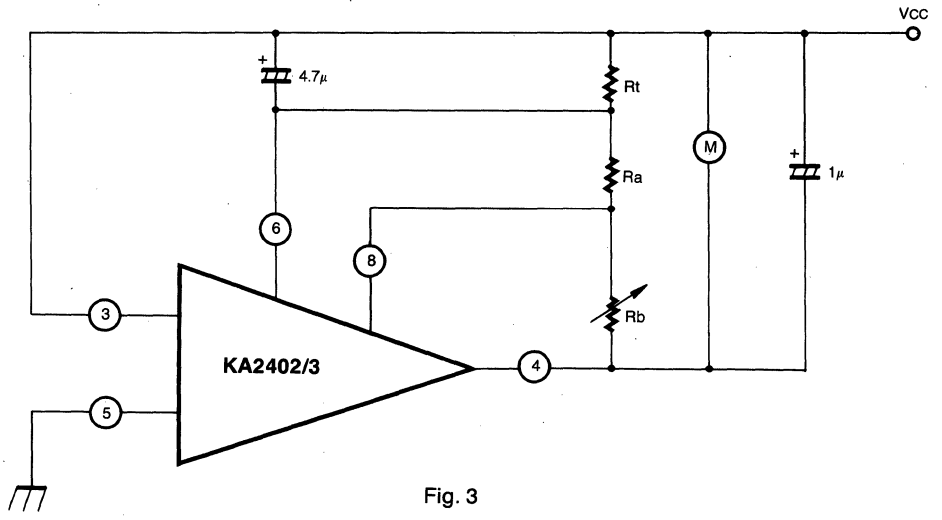
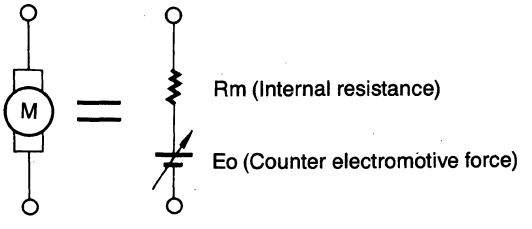


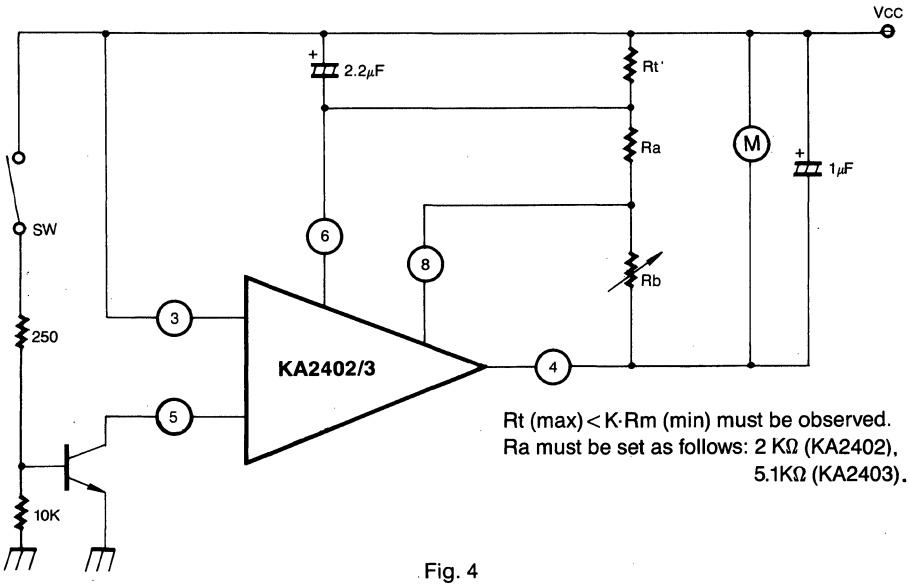
Fig. 3

Unless Rt (max) < K·Rm (min), the operation become unstable.
Ra must be set as follows: 2KΩ (KA2402), 5.1KΩ (KA2403).
Rm=Motor DC current



The values of the electrolytic capacitors depend on the type of the motor to be used.

Application Circuit 2: with stop circuit



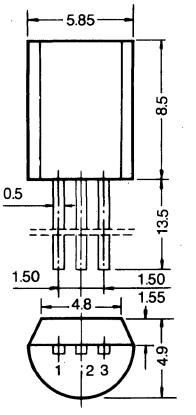
Rt (max) < K·Rm (min) must be observed.
Ra must be set as follows: 2 KΩ (KA2402),
5.1KΩ (KA2403).

Fig. 4

DC MOTOR SPEED CONTROLLER

The KA2404 is a monolithic integrated circuit designed for DC motor speed controllers.

TO-92L Unit: mm



1. Input 2. GND 3. Output

FEATURES

- **Suitable for DC motor speed controllers of cassette tape recorder and radio cassette.**
- **Excellent stability of each characteristics against ambient temperature.**
- **High output current.**
- **Low quiescent current (1.3mA: typ).**
- **Low reference vlotage.**
- **Wide operating supply voltage range (4V ~ 12V).**

EQUIVALENT CIRCUIT BLOCK DIAGRAM

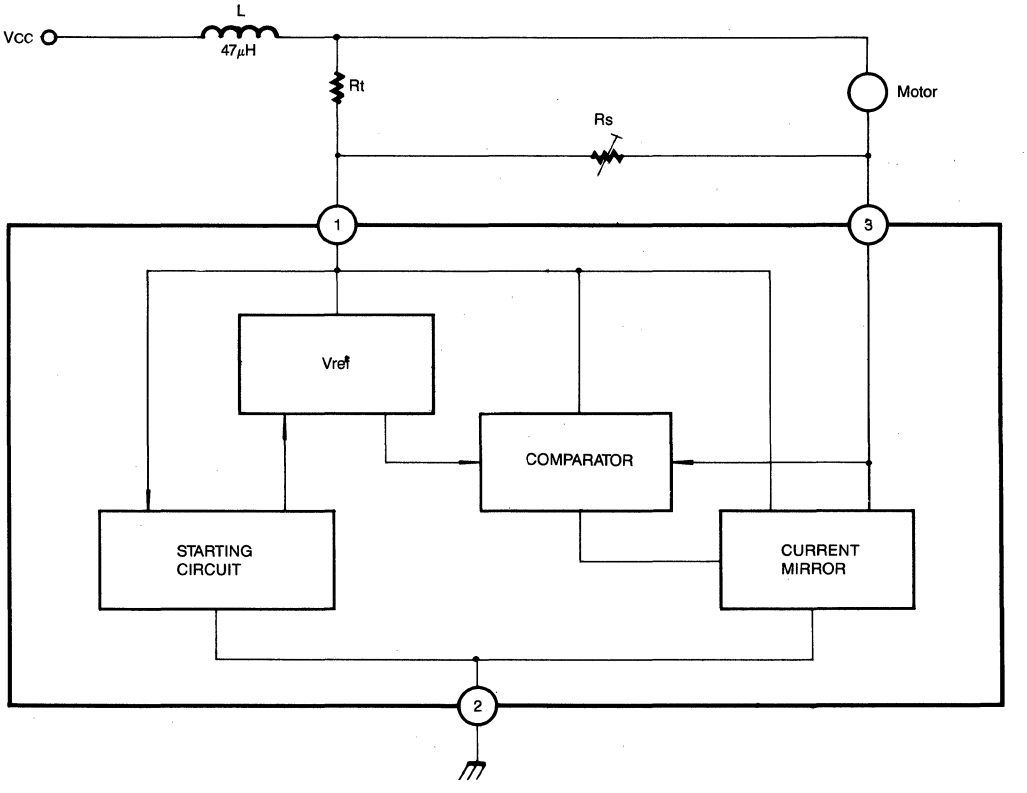


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Circuit Current	I_3	*2	A
Power Dissipation	P_d	800	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

* t<5 sec

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=9V unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Reference Voltage	Vref	I_3=10mA	1.10	1.27	1.40	V	2
Quiescent Current	Id	Rm=180Ω	0.8	1.3	1.8	mA	4
Reflection Coefficient	K	Rm_1=44Ω Rm_2=33Ω	16	18	20		3
Voltage Characteristic	$\frac{\Delta K}{K} / \Delta V_{CC}$	I_3=100mA V_{CC}=4 ~ 12V		0.4		%/V	3
	$\frac{\Delta Vref}{Vref} / \Delta V_{CC}$	I_3=100mA V_{CC}=4 ~ 12V		0.06		%/V	2
Current Characteristics	$\frac{\Delta K}{K} / \Delta I_3$	I_3=30 ~ 200mA		−0.02		%/mA	3
	$\frac{\Delta Vref}{Vref} / \Delta I_3$	I_3=30 ~ 200mA		−0.02		%/mA	2
Temperature Characteristics	$\frac{\Delta K}{K} / \Delta T_a$	I_3=100mA T_a=20 ~ +75°C		0.01		%/°C	3
	$\frac{\Delta Vref}{Vref} / \Delta T_a$	I_3=100mA T_a=−20 ~ +75°C		0.01		%/°C	2

TEST CIRCUIT 1

Reference Voltage

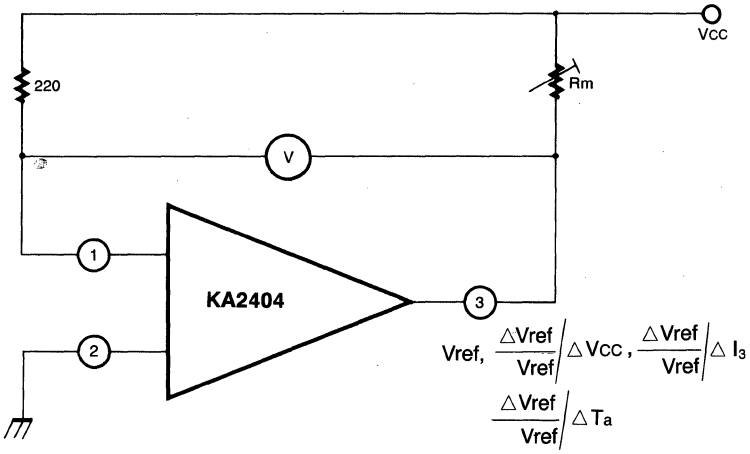


Fig. 2

TEST CIRCUIT 2

Reflection Coefficient

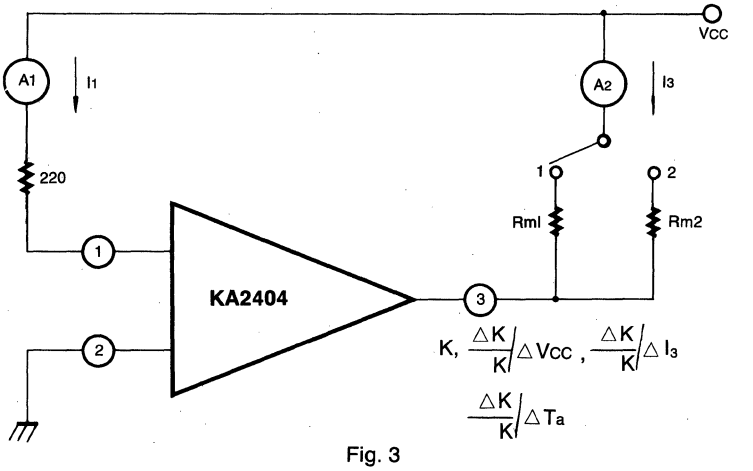


Fig. 3

$$K = \frac{I_3\ (SW\ 2) - (SW\ 1)}{I_1\ (SW\ 2) - (SW\ 1)}$$

TEST CIRCUIT 3

Quiescent Current

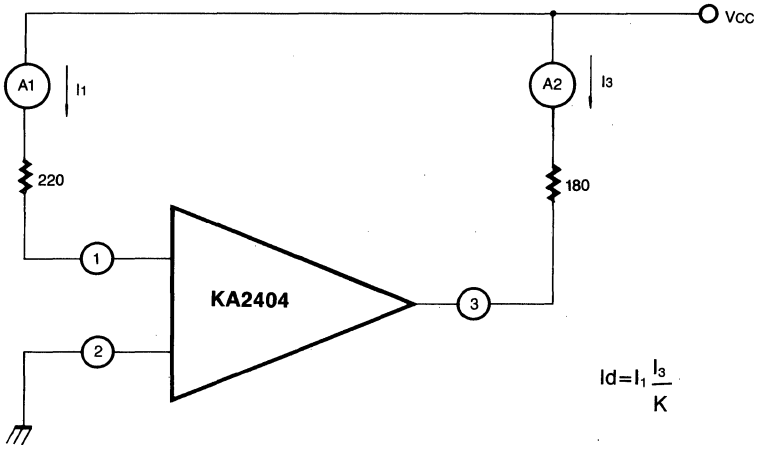


Fig. 4

TYPICAL APPLICATION

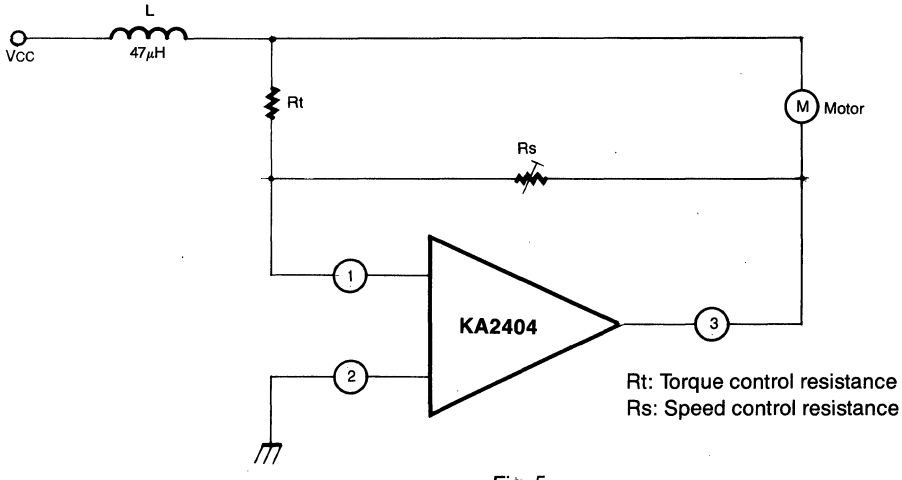
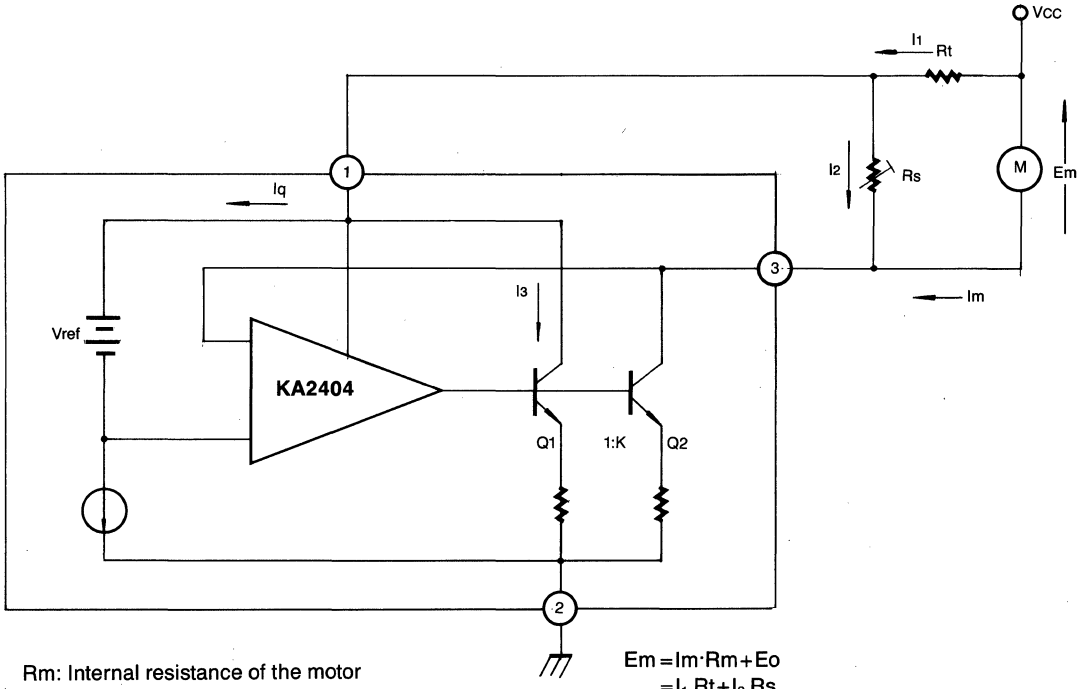


Fig. 5

BASIC EQUATION



Rm: Internal resistance of the motor
Eo: Back electronic force
K: Reflection coefficient

$$Em = Im \cdot Rm + Eo$$
$$= I_1\, Rt + I_2\, Rs$$
$$= Vref + \left(\frac{Im + I_2}{K} + Iq + \frac{Vref}{Rs}\right) \cdot Rt$$
$$= Vref\left(1 + \frac{Rt}{Rs}\left(1 + \frac{1}{K}\right)\right) + Rt \cdot Iq + \frac{Rt}{K} Im$$

Fig. 6

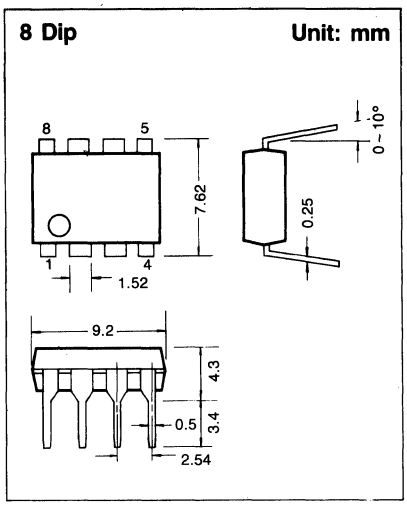
If. $Rm = \frac{Rt}{K}$ then

$$Eo = Vref\left(1 + \frac{Rt}{Rs}\left(1 + \frac{1}{K}\right)\right) + Rt \cdot Iq$$

Low Voltage Audio Power Amplifier

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low,but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.



FEATURES

- **Battery operation.**
- **Minimum external parts.**
- **Wide supply voltage range 4V ~ 12V or 5V ~ 18V.**
- **Low quiescent current drain 4mA.**
- **Voltage gains from 20 to 200.**
- **Ground referenced input.**
- **Self-centering output quiescent voltage.**
- **Low distortion.**
- **Eight pin dual-in-line package.**

SCHEMATIC AND CONNECTION DIAGRAMS

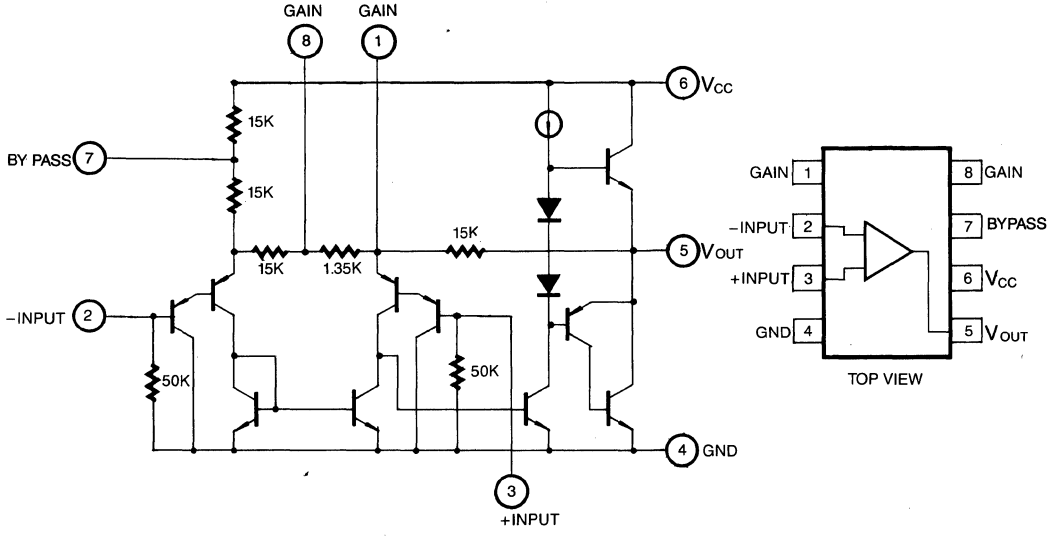


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Power Dissipation	P_d	660	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =6V, f= 1KHz, R_L =8Ω, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i =0		4	8	mA
Output Power	P_O	THD=10%	250	325		mW
Total Harmonic Distortion	THD	P_O =125mW		0.2		%
Bandwidth	BW	Pins 1 and 8 Open		72		kHz
Voltage Gain (Closed Loop)	A_V	10μF from Pin 1 to 8		46		dB
Input Resistance	R_i			50		kΩ
Input Bias Current	I_{BIAS}	Pins 2 and 3 Open		250		nA

TYPICAL APPLICATION

Amplifier with Gain=50

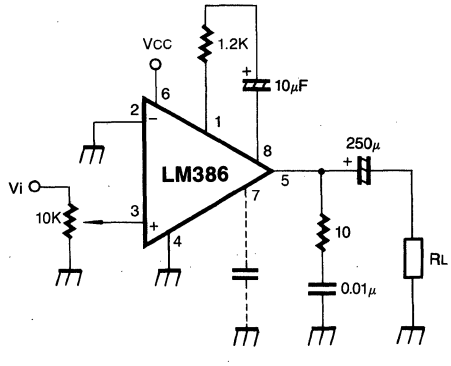


Fig. 2

Low Distortion Power Wienbridge Oscillator

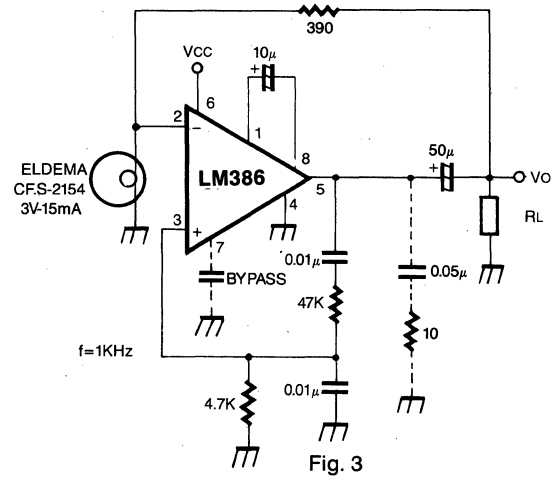


Fig. 3

Amplifier with Bass Boost

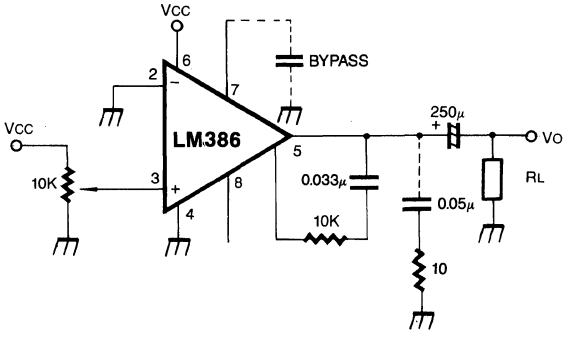


Fig. 4

Square Wave Oscillator

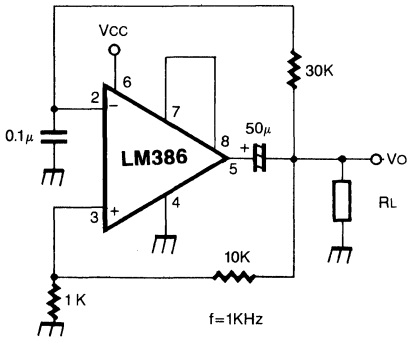
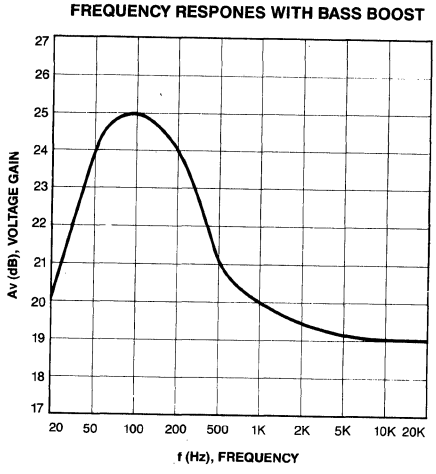


Fig. 5



AM Radio Power Amplifier

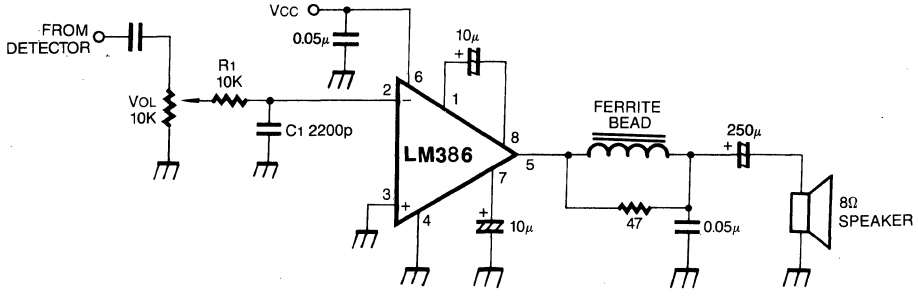
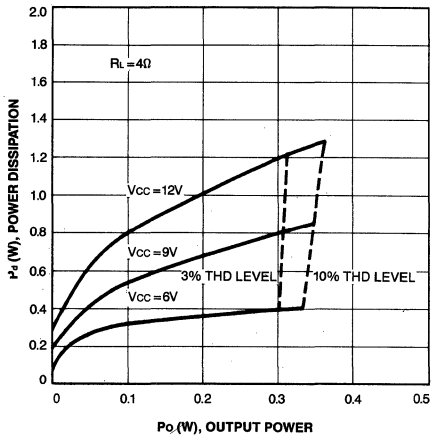
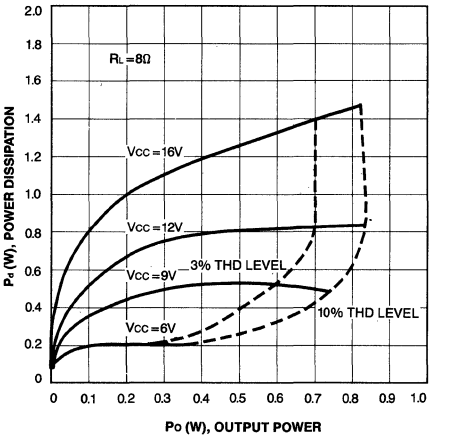


Fig. 6

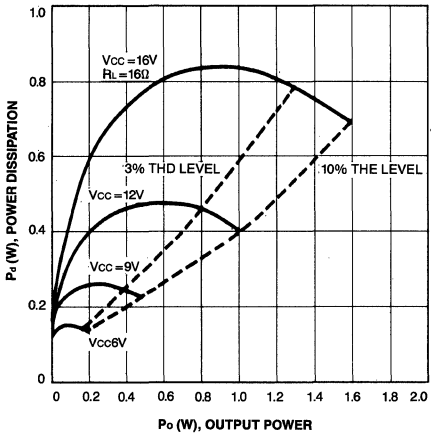
POWER DISSIPATION-OUTPUT POWER



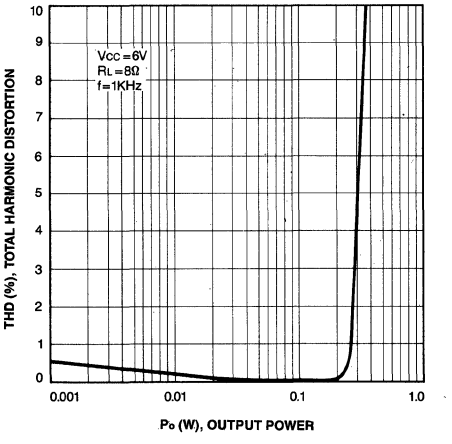
POWER DISSIPATION-OUTPUT POWER



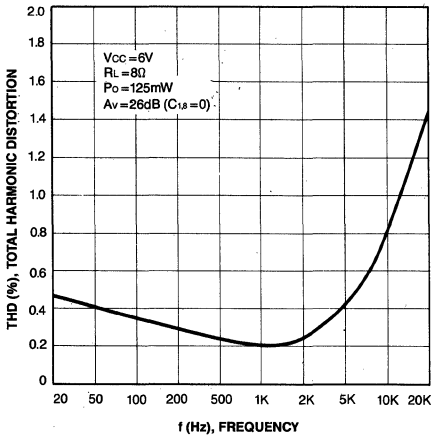
POWER DISSIPATION-OUTPUT POWER



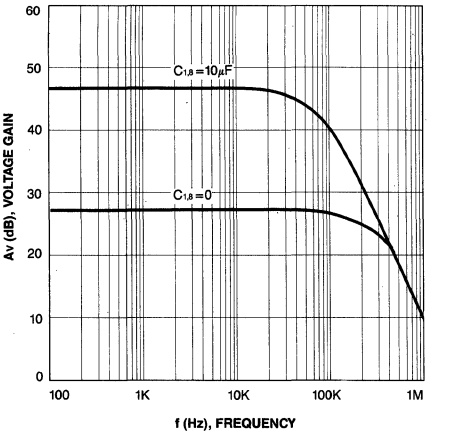
TOTAL HARMONIC DISTORTION-OUTPUT POWER



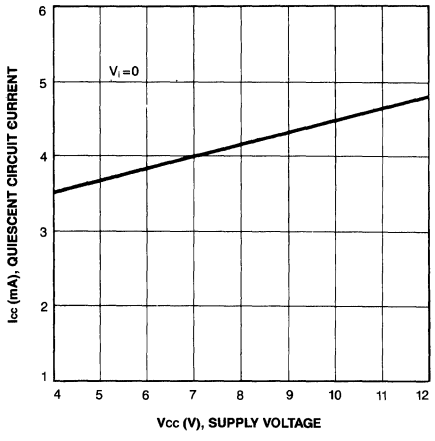
TOTAL HARMONIC DISTORTION-FREQUENCY



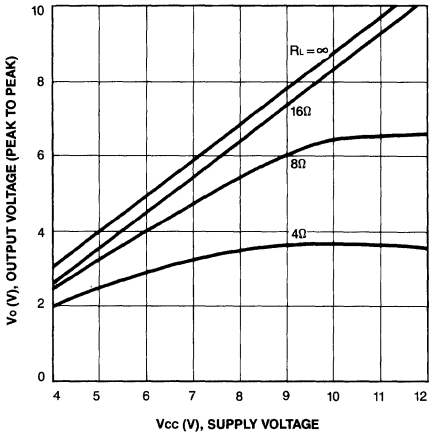
VOLTAGE GAIN—FREQUENCY



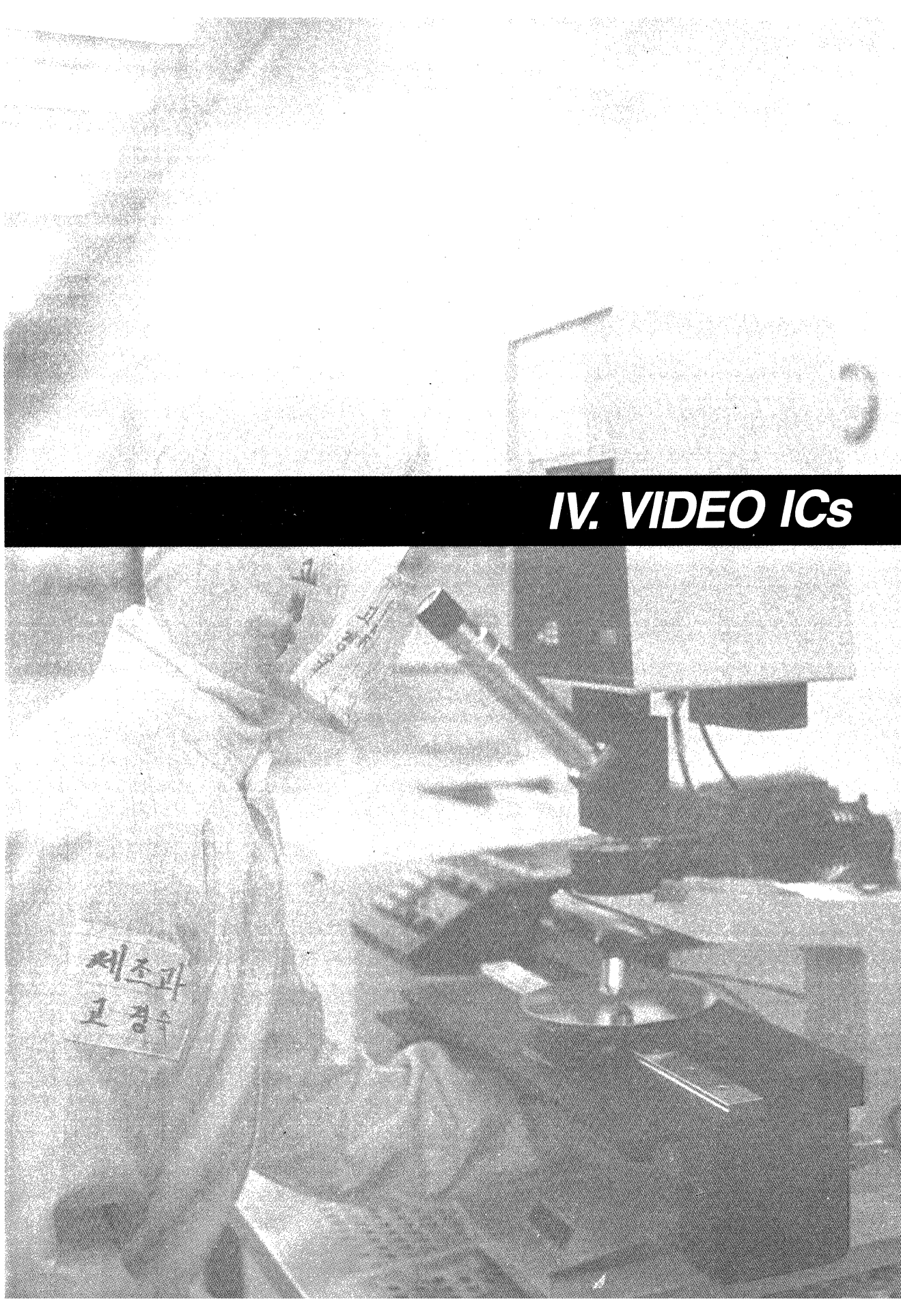
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING-SUPPLY VOLTAGE



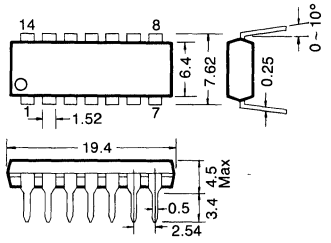
IV. VIDEO ICs



TV SOUND IF AMPLIFIER

The KA2101 is a monolithic integrated circuit for TV sound 1F amplifier. It contains a IF amplifier, IF limiting, detection, electronic attenuation, audio amplifier and audio driver capabilities.

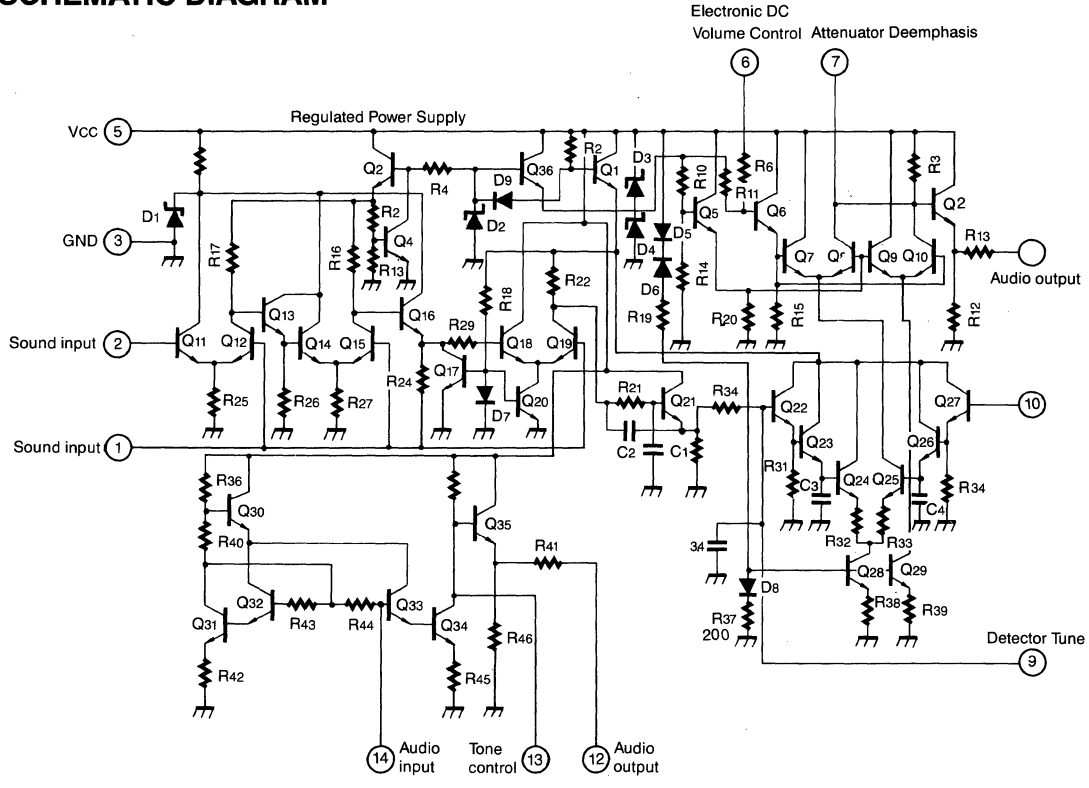
14 Dip **Unit: mm**



FEATURES

- **Electronic attenuator replaces conventional DC volume.**
- **Differential peak detector requires one single tuned coil.**
- **Internal zener diode regulated supply.**
- **High stability.**
- **Excellent AM rejection at 4.5 MHz, 5.5 MHz, 6.0 MHz, 6.5 MHz.**
- **Low harmonic distortion.**
- **High sensitivity 200μV limiting at 4.5 MHz.**
- **Audio driver capability 6.0 mA_{P-P}.**
- **Undistorted audio output voltage 7 V_{P-P}.**
- **Minimum undesirable output signal at maximum attenuation.**

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Input Signal Voltage (Pin 1, Pin 2)	V_{in}	±3	V
Power Supply Current (Pin 5)	I_5 (max)	50	mA
Total Power Dissipation	P_d	625	mW
Derate Above T_a =25°C		5.0	mW/°C
Operating Temperature	Topr	−20 ~ +75	°C
Storage Temperature	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS (T_a =25°C, V_{CC} =24V)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Regulated Voltag (Pin 5)		V_5		10.3	11.5	12.2	V	
DC Supply Current (Pin 5)		I_5	V_{CC} =9V R_S =0	10	13	24	mA	
Quiescent Output Vtg (Pin 12)		V_{12}		4.5	5.1	5.8	V	—
AM Rejection*		AMR	V_{in} = 10mV f_o =4.5MHz, Δf= ±25KHz	40	55	—	dB	4
Input Limiting Threshold Voltage		V_i (lim)	f_o =4.5MHz, Δf= ±25KHz	—	200	400	μVrms	4
Recovered Audio Output Voltage		V_o (AF)	V_{in} =10mV f_o =4.5MHz, Δf= ±25KHz	0.5	0.90	—	Vrms	4
Output Distortion		THD	V_{in} = 10mVrms	—	0.9	2	%	4
Input Resistance (Pin 1 & 2)		R_i (IF)	f=4.5MHz	—	17	—	KΩ	
Input Capacitance (Pin 1 & 2)		C_i (IF)	f = 4.5MHz	—	4	—	pF	
Output Resistance (Pin 9 & GND)		R_o (IF)	f=4.5MHz	—	3.25	—	KΩ	
Output Capacitance (Pin 9 & GND)		C_o (IF)	f = 4.5MHz	—	7.5	—	pF	
Output Resistance,	Pin 7	R_o		—	7.5	—	KΩ	
	Pin 8			—	250	—	Ω	
Volume Reduction Range			DC Volume Control = ∞	60	—	—	dB	4
Maximum Undesirable Signal (Note 1)				—	0.02	1	mVrms	4
Audio Amplifier Voltage Gain		A (AF)	V_{in} = 0.1Vrms, f = 400Hz	17.5	20.5	—	dB	5
Total Harmonic Distortion (Pin 12)		THD	V_o =20Vrms, f=400Hz	—	1.5	—	%	5
Output Voltage (Pin 12)			THD=5%, f=400Hz	2	3.4	—	Vrms	5
Input Resistance (Pin 14 & GND)		R_i (AF)	f=400Hz	—	70	—	KΩ	
Output Resistance (Pin 12 & GND)		R_o (AF)	f = 400Hz	—	270	—	Ω	

* 100% FM, 30% AM

Note 1. Undesirable signal is measured at pin 8 when volume control is set for minimum output.

TYPICAL APPLICATION CIRCUIT

A. 1.5 Watts Output

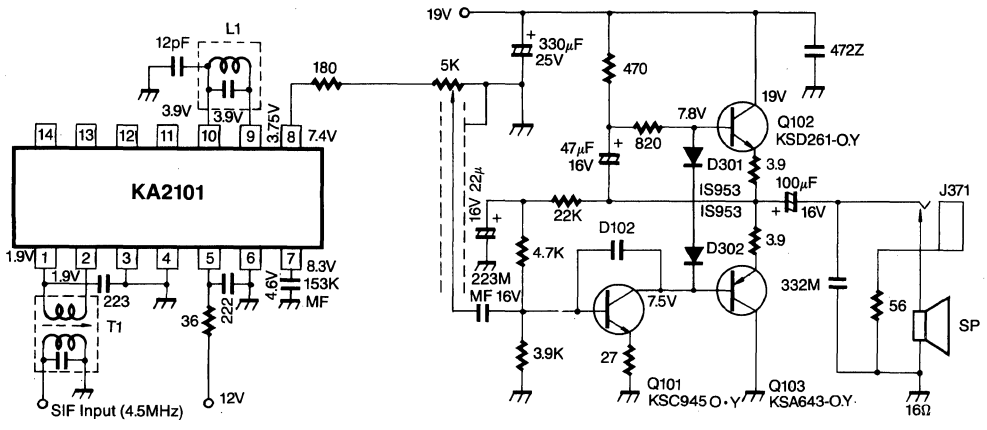


Fig. 2

B. 0.8 Watts Output

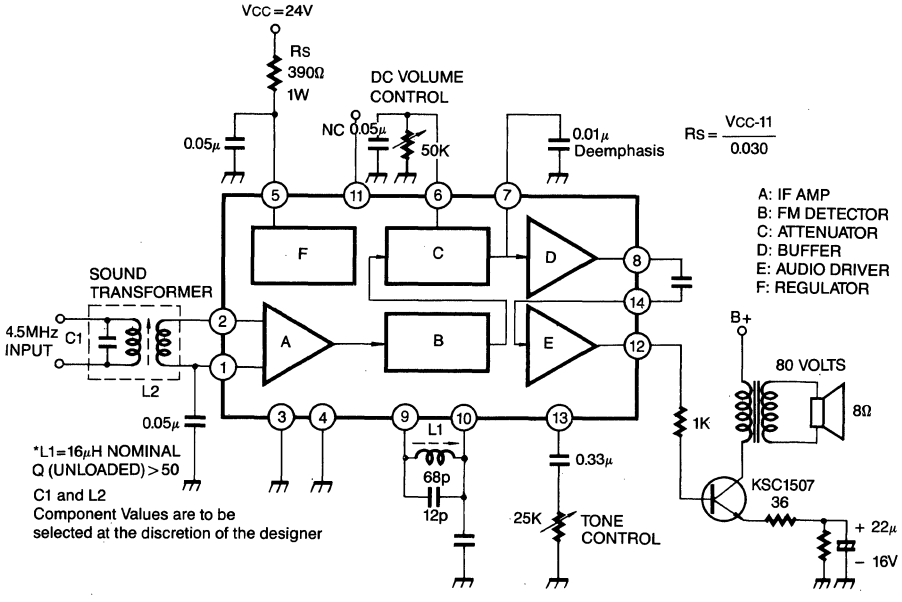


Fig. 3

TEST CIRCUIT 1

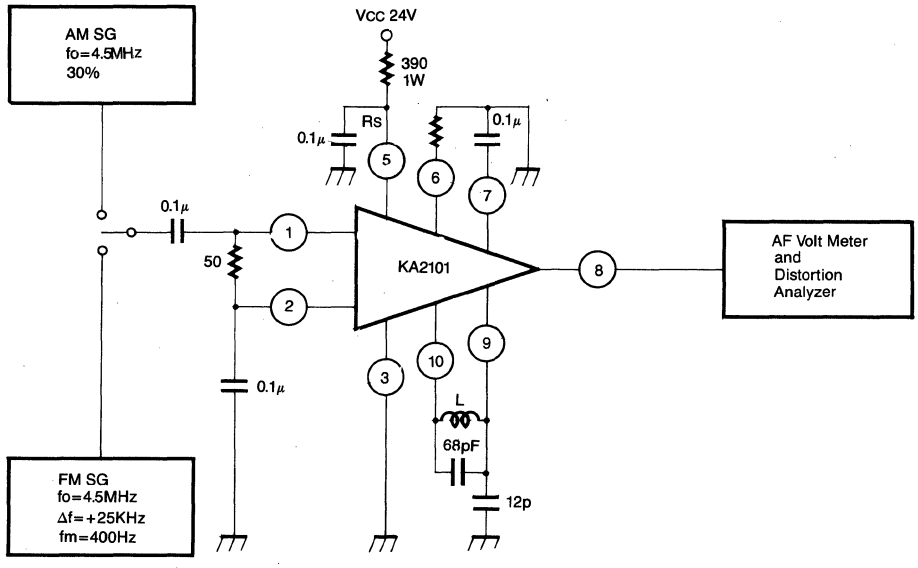


Fig. 5

TEST CIRCUIT 2

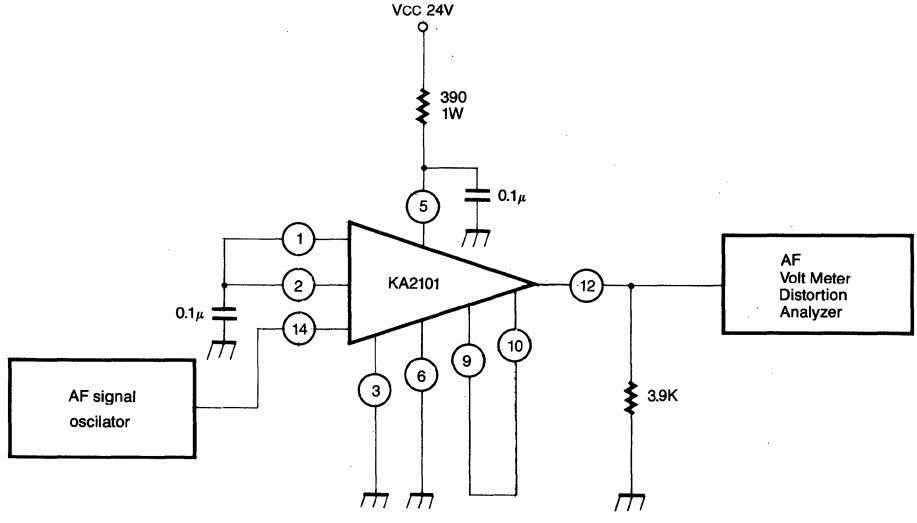
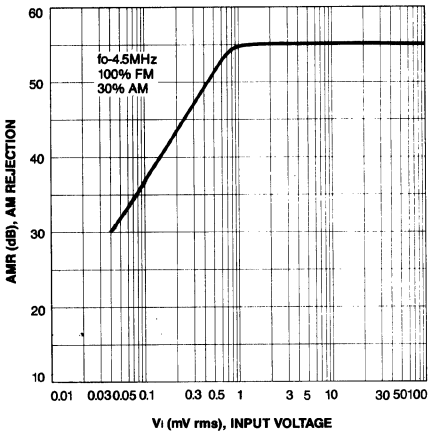
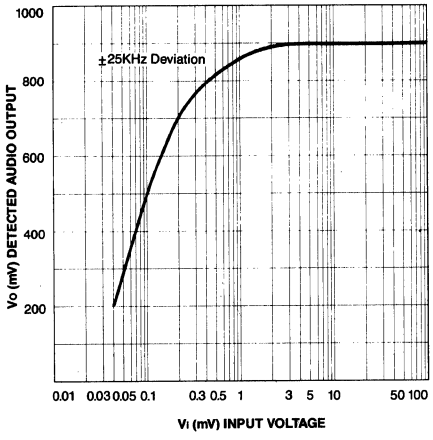


Fig. 4

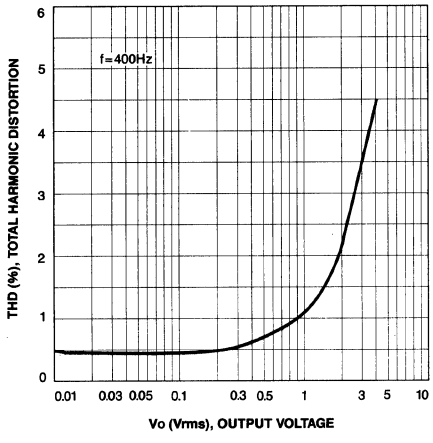
AM REJECTION



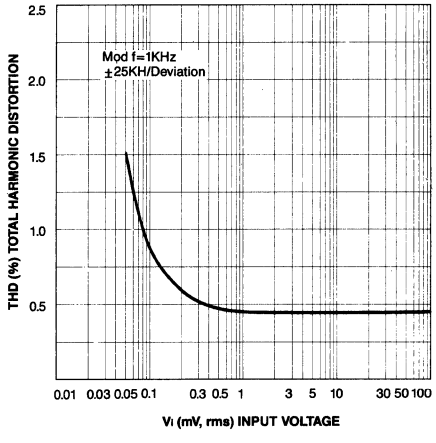
DETECTED AUDIO OUTPUT



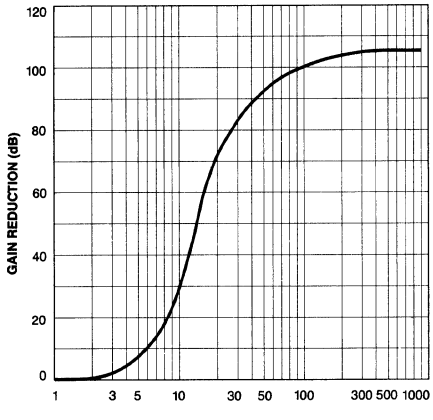
AUDIO AMPLIFIER THD



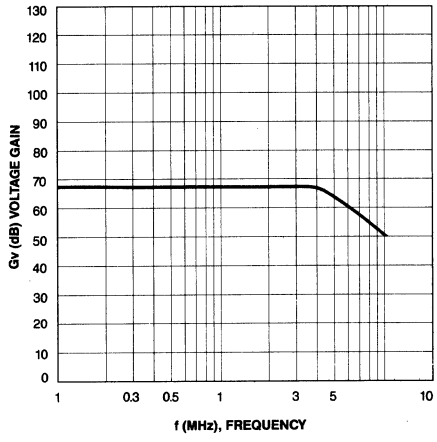
IF AMPLIFIER AND DETECTOR THD



GAIN REDUCTION OF ATTENUATOR



IF FREQUENCY RESPONSE

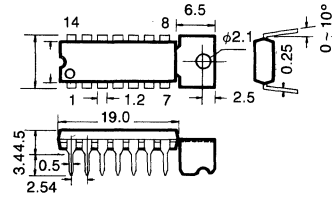


TY SOUND SYSTEM

The KA2102A is a silicon monolithic integrated circuit designed for SIF and audio section in television receivers. This IC has all functions including sound IF amplifier, FM detector, DC volume control circuit, audio output amplifier with 2.4 Watts output power and voltage regulator. This IC is encapsulated in 14 pin dual in-line package with heat tab.

- Wide power supply range, 9V ~ 18V
  2.4 Watt, at V_{CC} = 18V, R_L = 8Ω (For 17" TV)
  1.2 Watt, at V_{CC} = 12V, R_L = 8Ω (For 12" TV)
- Linear volume control
- Low harmonic distortion
- Differential peak detector
- Enough attenuation (Typ, 80dB) by squelch circuit

14 Dip H.S **Unit: mm**



TYPICAL APPLICATION CIRCUIT

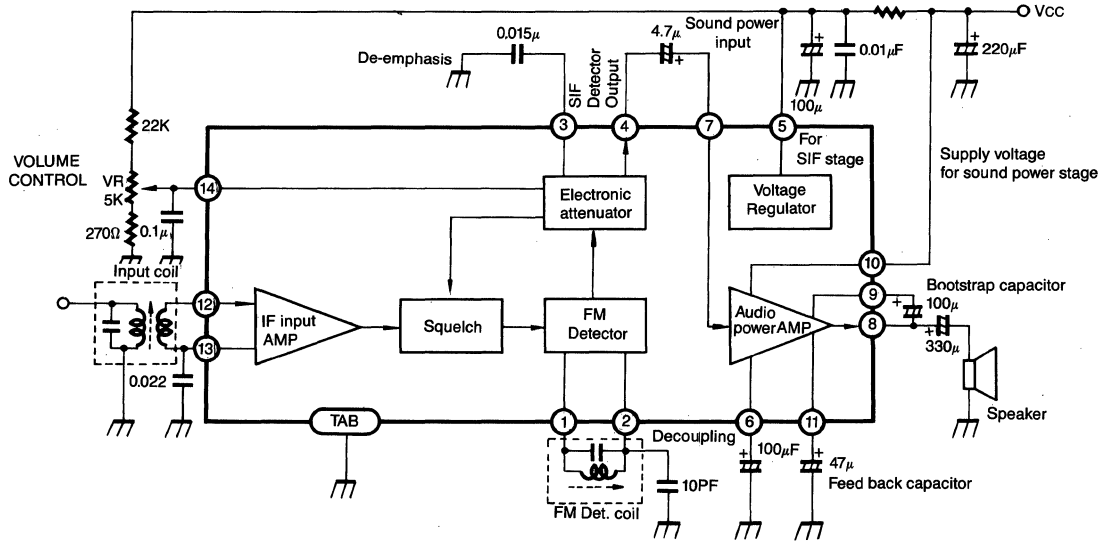


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage (Pin 10)	V_{10}	20	V
Supply Current (Pin 10)	I_{10}	1	A
Supply Current (Pin 5)	I_5	100	mA
Input Signal Voltage	V_i	3	V_{p-p}
Power Dissipation	P_{d1}	0.8 (T_a=75°C) free air	W
Power Dissipation	P_{d2}	1.4*	W
Operating Temperature	Topr	−20 ~ +75	°C
Storage Temperature	Tstg	−40 ~ +150	°C

* Printed Circuit Copper Area 50×50mm^2

ELECTRICAL CHARACTERISTICS (T_a=25°C)

1. IF STAGE (V_{CC}=12V, R_B=100Ω, V_{14}≧1.3V, fo=4.5MHz, fm=400Hz, f=±25KHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Pin 5 Voltage	V_{5A}		7.5	8.0	8.5	V
Pin 5 Voltage	V_{5B}	V_{CC}=18V, R_B=330Ω	7.5	8.0	8.5	V
Pin 10 Current	I_{10A}	No Input Signal	14	19	24	mA
Pin 10 Current	I_{10B}	V_{CC}=18V, R_B=330Ω No Input Signal	16	28	35	mA
IF Limiting Voltage	V_i (lim)	V_{OAF} (V_i=10mVrms). −3dB	—	200	400	μVrms
Detector Output Voltage	V_{OAF}	V_i=10mVrms	300	360	—	mVrms
Detector Distortion	THD_1	V_i=10mVrms	—	0.7	—	%
AM Rejection	AMR	AM Mod 30% fm=400Hz V_i=10mVrms	−40	−50	—	dB
Maximum Attenuation	ATTmax	V_{14}	−60	−80	—	dB

2. SOUND POWER STAGE (V_{CC}=12V, R_B=100Ω, R_L=8Ω, f=400Hz, R_G=600Ω)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Sound Stage Voltage Gain	G_{VAF}	V_i=30mVrms	33	37	41	dB
Sound Output Power	PoA	THD=10%	0.9	1.2	—	W
Sound Output Power	PoB	V_{CC}=18V, R_B=330Ω THD=10%	2.0	2.4	—	W
Sound Output Distortion	THD_{2A}	Po=0.5W	—	0.6	2.0	%
Sound Output Distortion	THD_{2B}	V_{CC}=18V, R_B=330Ω P_o=0.5W	—	0.5	2.0	%
Over All Sound Output Distortion (IF + Sound Power Stage)	THD_3	P_o=0.5W V_i=10mVrms	—	1.5	4.0	%

3. TYPICAL DATA

Characteristic	Symbol	Test Conditions	Value	Unit
Pin 10 Current	I_{10}	THD_{2A}=10%	200-210	mA
Pin 10 Current	I_{10}	THD_{2B}=10%	270-280	mA
Sound Output Power	PoA	THD=3%	1.1	W
Sound Output Power	PoB	V_{CC}=18V, R_B=330Ω THD=3%	2.0	W
Sound Stage Band Width	BW	-3dB	50~50K	Hz

TEST CIRCUIT

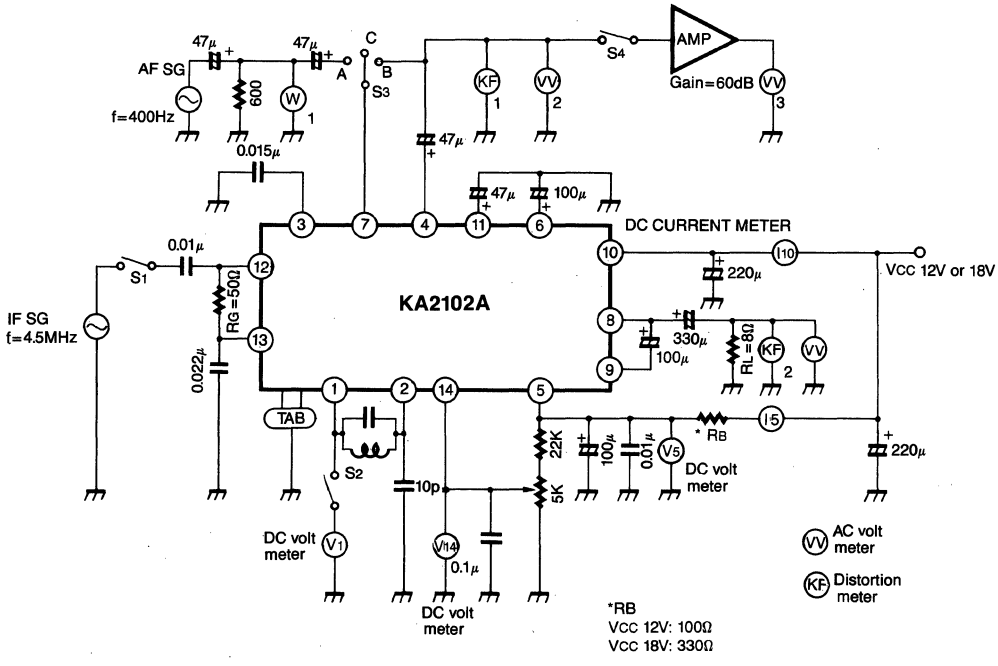
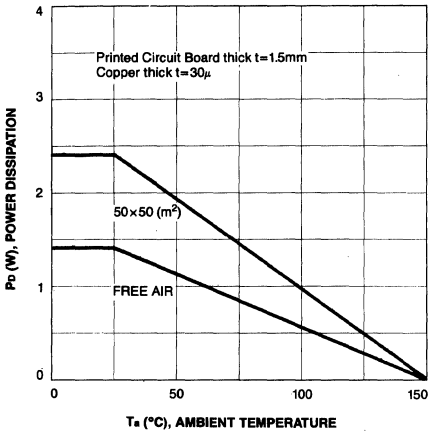
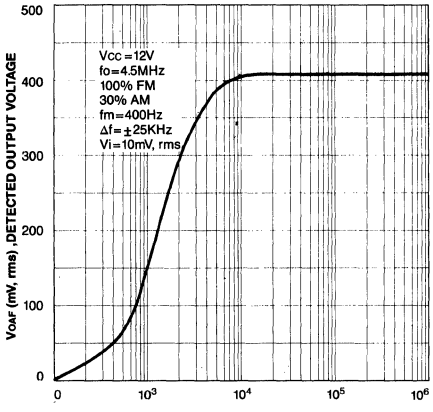


Fig. 2

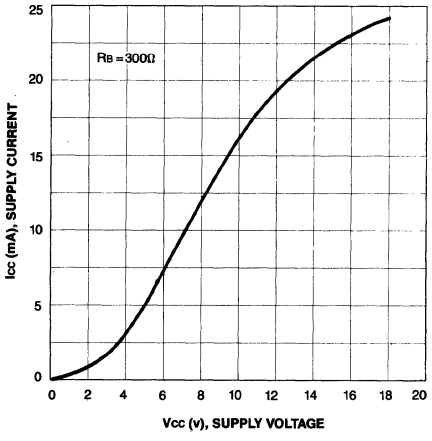
POWER DISSIPATION



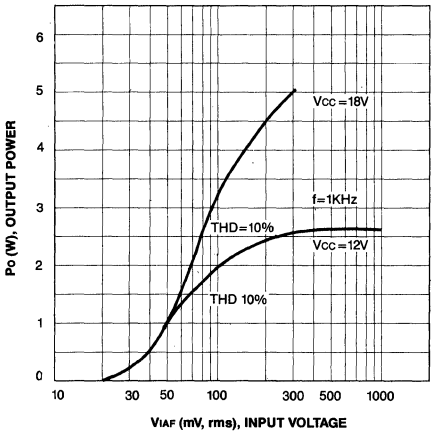
DETECTED OUTPUT VOLTAGE



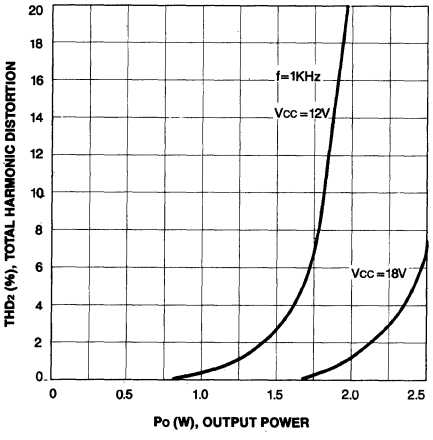
SUPPLY CURRENT



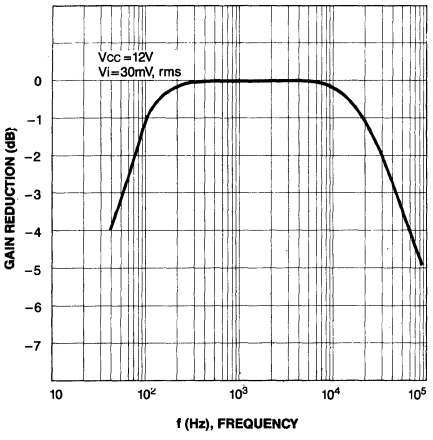
OUTPUT POWER (AUDIO AMPLIFIER)



TOTAL HARMONIC DISTORTION



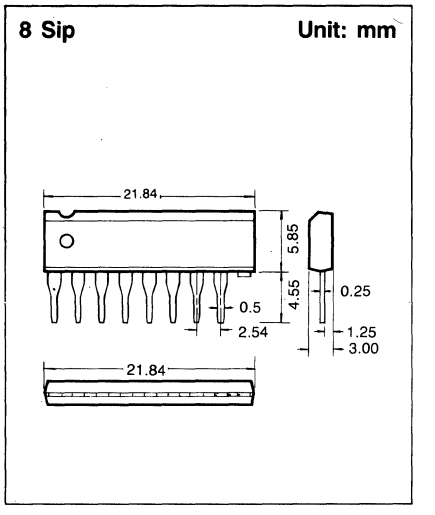
FREQUENCY RESPONSE (AUDIO AMPLIFIER)



SOUND MUTE SYSTEM FOR TV

The KA2103L is a monolithic integrated circuit designed for noise sound muting in television receiver.

This IC has all functions including horizontal synchronizing detector, comparator and open collector output terminal.



FEATURES

- **Wide operating voltage range.**
- **Small shock noise at the time of power on/off.**
- **Good noise sound muting characteristic.**
- **Capable of being connected to the other IC directed.**
- **Collector open output.**
- **Minimum number of external parts required.**

BLOCK DIAGRAM

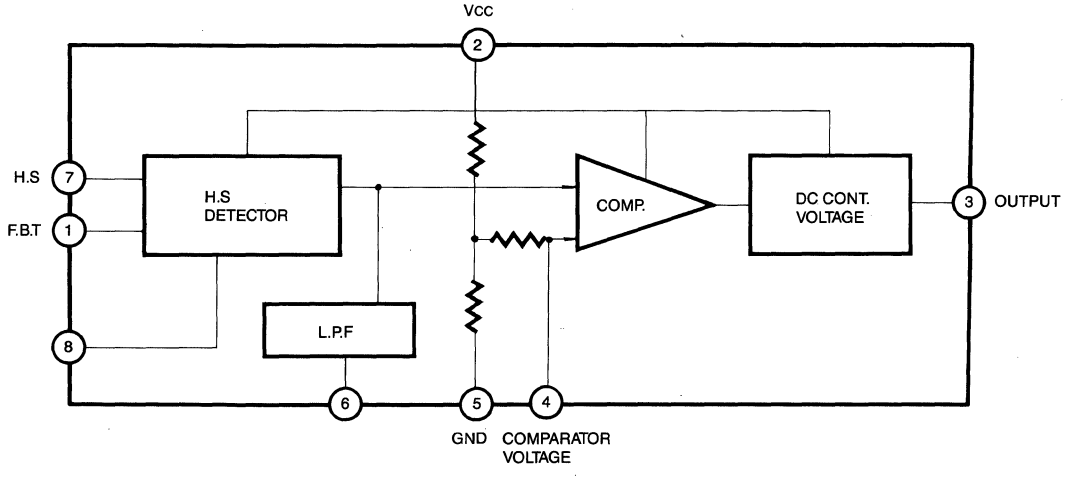


Fig. 1

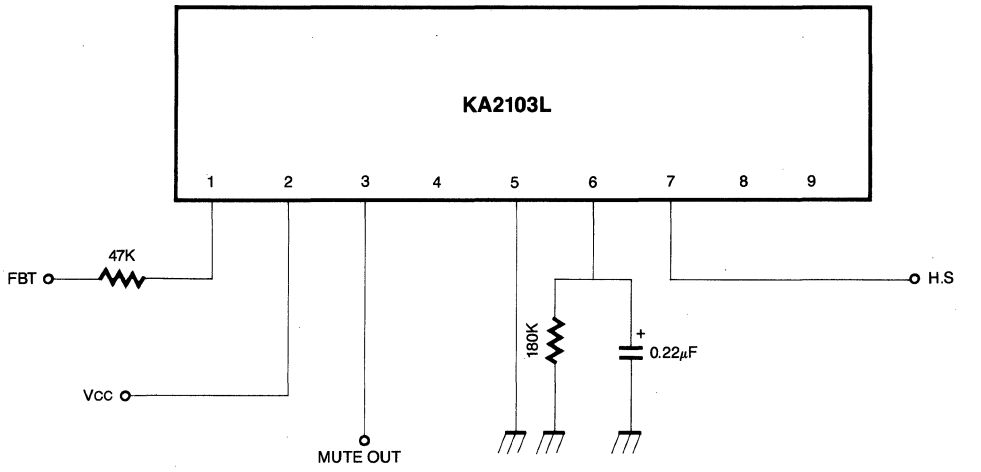
ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Comparator Differance	$V_{COMP.}$	6	V
Power Dissipation	Pd	80	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS (T_a =25°C, V_{CC} =12V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}		3.5	5.0	9.0	mA
Input Threshold Voltage	V (HS)		7.7	8.0	8.3	V
Input Threshold Voltage	V (FBT)		3.7	4.0	4.3	V
Output Saturation Voltage	$V_{(SAT)}$		—	0.33	0.7	V
L.P.F Output Current	I_O1		0.5	0.8	1.5	mA
Comparator Voltage Settling Range	BV_A		2	3	8	V
Comparator Voltage Settling Range	BV_B		7	9	11	V

TYPICAL APPLICATION CIRCUIT



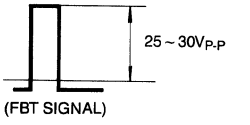
Note

F.B.T : Fly back transformer (C.R.T. Heater line)
(Television set F.B.T voltage=25 ~ 30V_{P-P})

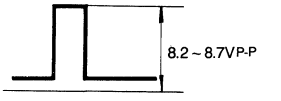
V_{CC}: D.C 12V

Mute Out : Sound IC Audio signal input
(Active: High)

H.S : Horizontal Sync (KA2153 Pin=37)
(Television set H.S voltage=8.2 ~ 8.7V_P)



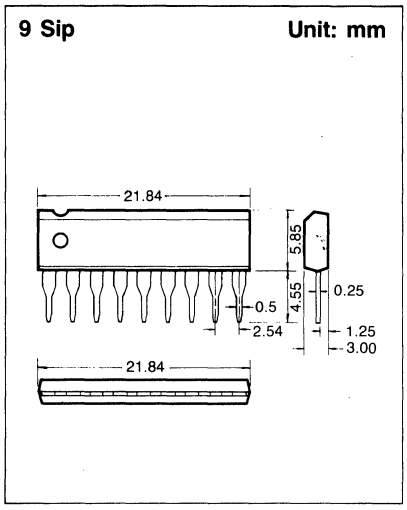
(FBT SIGNAL)



(H.S SIGNAL)

AUTO POWER OFF AND SOUND MUTE SYSTEM FOR TV

The KA2104 is a monolithic integrated circuit designed for noise sound muting and auto power off when channel without broadcasting selected or broadcasting ended.



FUNCTIONS

— Horizontal Synchronizing State Detector.
— Comparator.
— Open Collector Output.
— Auto Power off control.

FEATURES

- **Wide Operating Voltage Range.**
- **Good noise sound muting characteristic.**
  –Pin 9: open collector out.
- **Usable for all kind of TV system.**
- **Adjustable auto power off time.**
- **Minimum number of external parts required.**

BLOCK DIAGRAM

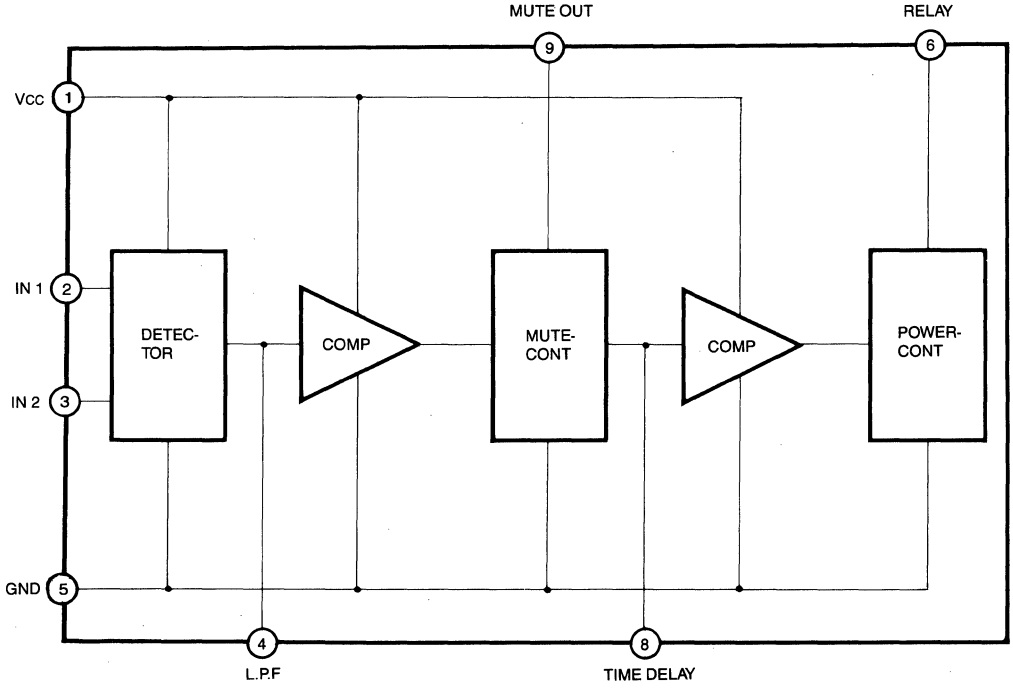


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Comparator Difference	V_{COMP}	6	Vpeak
Power Dissipation	Pd	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =12V, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_{CC} =12V	5.0	7.0	9.0	mA
Input Thereshold Voltage	Vth1 (p2)	Vpin3=5V	7.5	8.0	8.5	Vpeak
	Vth2 (p3)	Vpin2=9V	3.5	4.0	4.5	Vpeak
Output Saturation Voltage	Vsat1 (p6)	Vpin2=9V, Vpin3=5V	—	0.5	1.0	V
	Vsat2 (p9)	Vpin2, 3=0V	—	0.3	0.5	V
L.P.F Output Current	I (L.P.F)	R_L =150kΩ	50	80	100	μA
Time Delay Output Current	I (T.D)	R_L =150kΩ	50	80	100	μA

TEST CIRCUIT

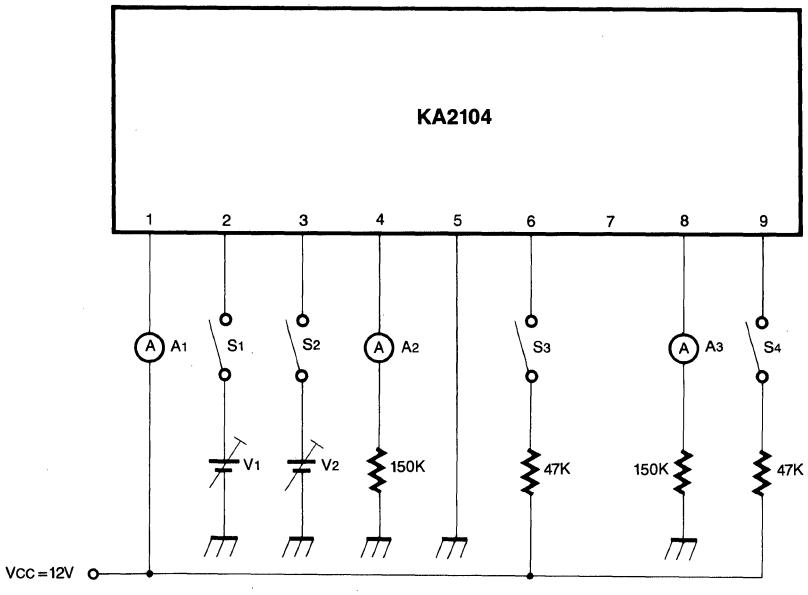
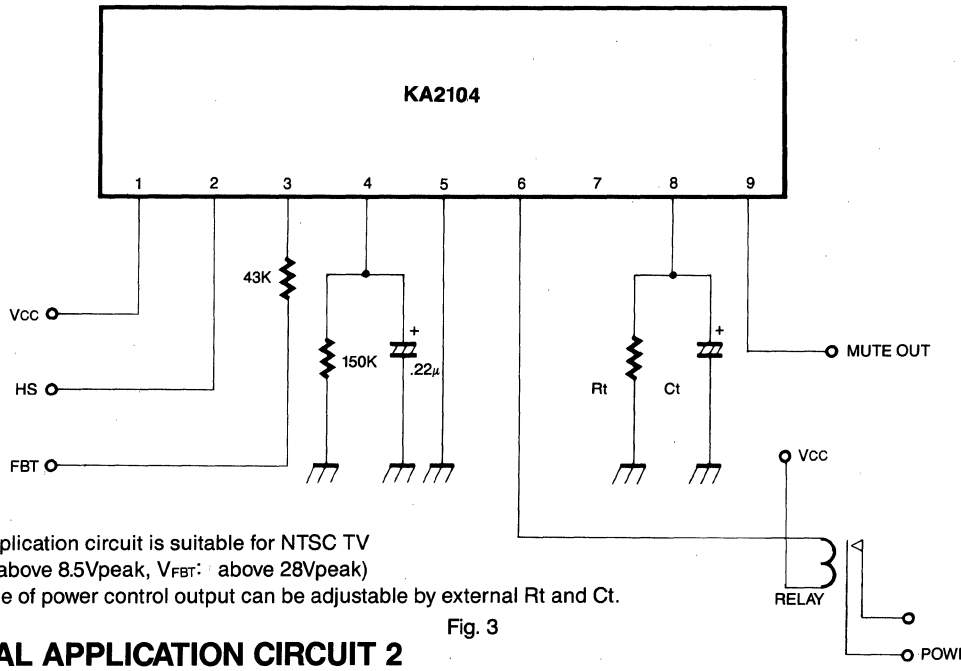


Fig. 2

TEST METHOD

Item	S1	S2	S3	S4	V1	V2	Test Point	Test Method
I_{CC}	×	×	×	×	—	—	Pin 1	Read A1
V_{th1} (Pin 2)	ON	ON	×	×	adjust	5V	V_I 2	At Pin 4 High
V_{th2} (Pin 3)	ON	On	×	×	9V	adjust	V_I 3	At Pin 4 High
V_{sat1} (Pin 6)	ON	ON	ON	×	9V	5V	Pin 6	Read Pin 6 Vtg.
V_{sat2} (Pin 9)	ON	ON	×	ON	9V	5V	Pin 9	Read Pin 9 Vtg.
I_{LPF}	ON	ON	×	×	9V	5V	Pin 4	Read A2
ITD	ON	On	×	×	9V	5V	Pin 8	Read A3

TYPICAL APPLICATION CIRCUIT 1

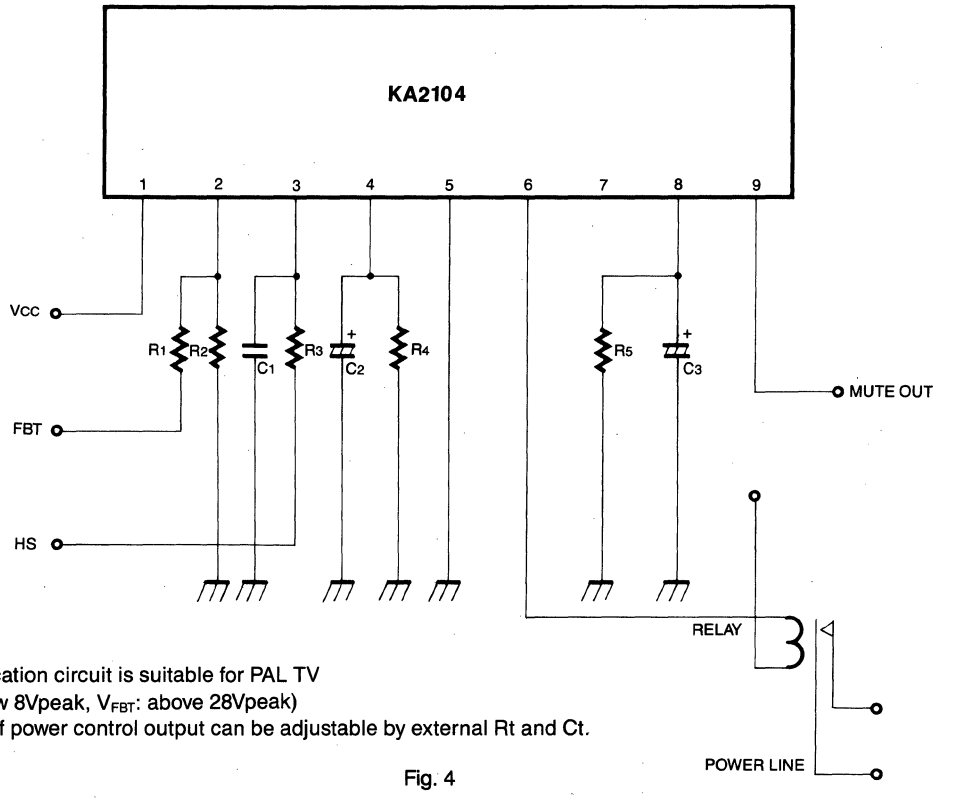


***Note**

1. This application circuit is suitable for NTSC TV
   ($V_{H.S}$: above 8.5Vpeak, V_{FBT}: above 28Vpeak)
2. The time of power control output can be adjustable by external Rt and Ct.

Fig. 3

TYPICAL APPLICATION CIRCUIT 2



***Note**

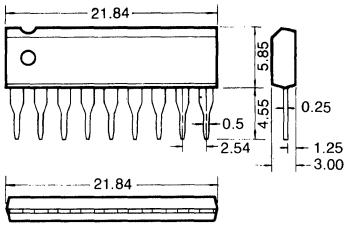
1. This application circuit is suitable for PAL TV
   ($V_{H.S}$: below 8Vpeak, V_{FBT}: above 28Vpeak)
2. The time of power control output can be adjustable by external Rt and Ct.

Fig. 4

LIMITER AMPLIFIER AND DETECTOR FOR A TV SIF

The KA2105 contans a limiting amplifier and an FM detector in a single-in-line plastic package. This device is especially recommended as a sound multiplex SIF subsystem requiring few external components and only one tuning adjustment for the 4.5 MHz tank circuit.

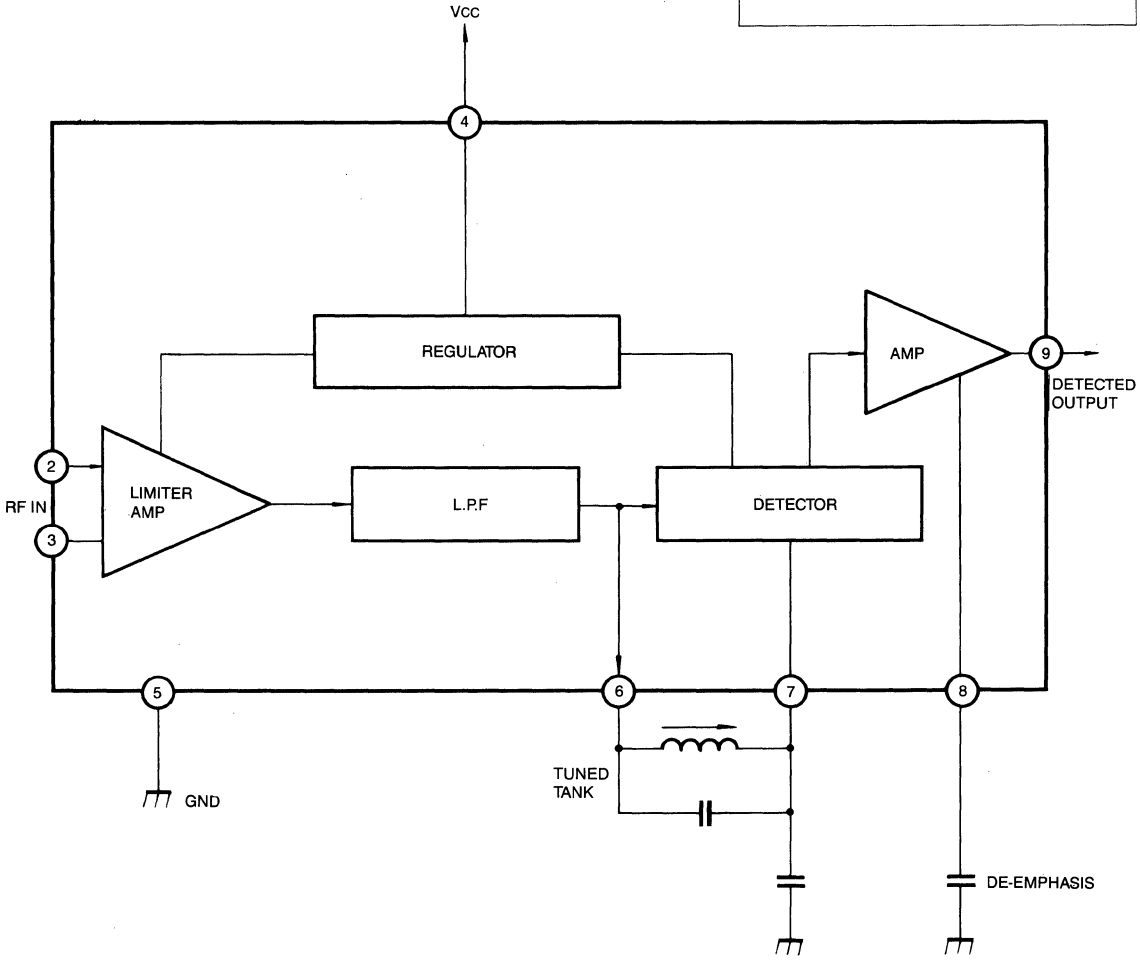
9 Sip Unit: mm



FEATURES

- **Detector with single tuned coil**
- **Excellent a rejection ratio; 50dB (Typ.)**
- **Wide supply voltage range; V_{CC} = 8-15V**
- **Minimum numbers of external parts requires.**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

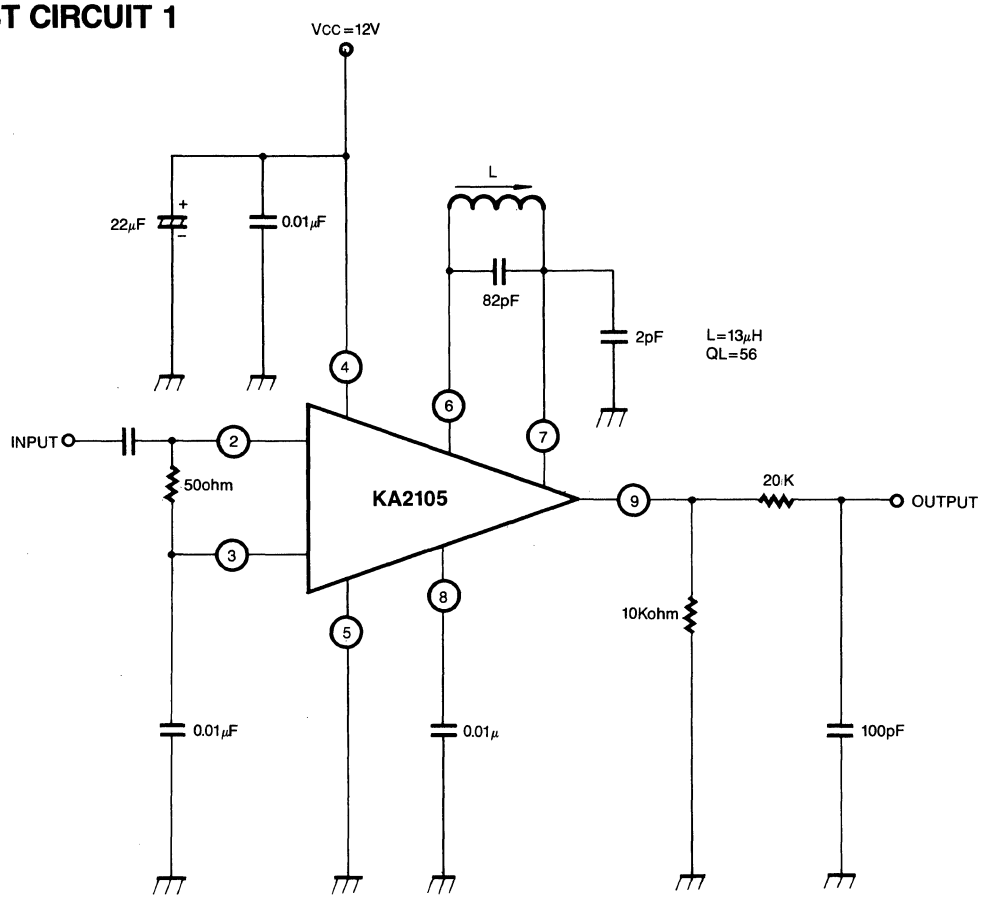
Characteristic	Symbol	Value	Unit
Supply Voltage	V_4	15	V
Input Voltage	V_2	0.7	V_{rms}
Power Dissipation (Note)	PD	625	mW
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

Note: Depated above T_a = 25°C

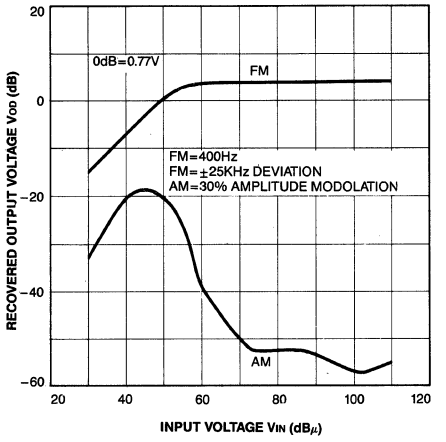
ELECTRICAL CHARACTERISTICS (T_a = 25°C, V_{CC} = 12V)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	—	8	—	15	V
Supply Current		I_{CC}	—	—	—	25	mA
Output Terminal Voltage		V_9	V_{IN} =0	—	5	—	V
Detected Output Voltage		V_{DD}	F=4.5MHz, FM=400Hz+25KHz	0.8	—	1.6	V_{rms}
Total Harmonic Distortion		THD	V_{IN} =100MV				
Limiting Sensitivity		V_{IN} (I_{IN})	−3dB 0 the Max, Output	—	—	500	μVrms
AM Rejection Ratio		AMR	V_{IN} =100MV_{rms}, FM 25KHz, 400Hz AM M=0.3, 400Hz	—	50	—	dB
Input Impedance	Parallel Input Resistance	RIP	F=4.5MHz	—	17	—	KΩ
	Parallel Input Capacitance	CIP	F = 4.5MHz	—	4	—	PF
Output Impedance	Parallel Output Resistance	ROP	F=4.5MHz	—	2	—	KΩ
	Parallel Output Capacitance	COP	F = 4.5MHz	—	3	—	PF

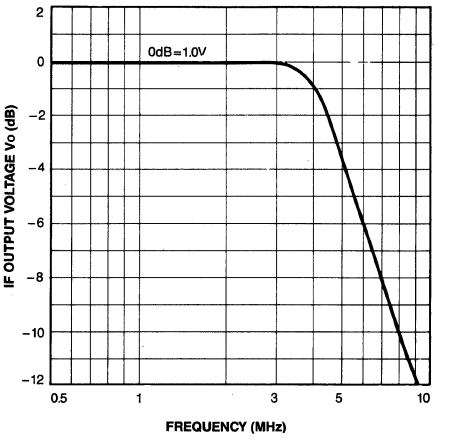
TEST CIRCUIT 1



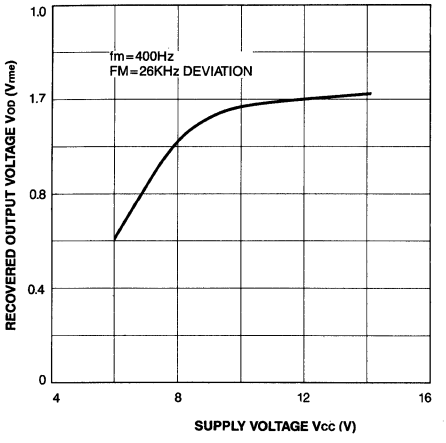
V_{OD}—V_{IN}



V_O—f



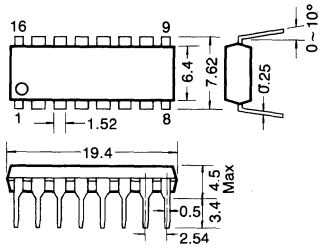
V_{OD}—V_{CC}



DUAL SOUND MULTIPLEX FOR A TV SIF

The KA2106 contain a dual limiting amplifier and FM detector in 16 dual-in-line flastic package. This device is especially recommended as dual sound multiplex SIF subsystem requiring few external components and each one tuning adjustment for the 4.5 MHz tank circuit.

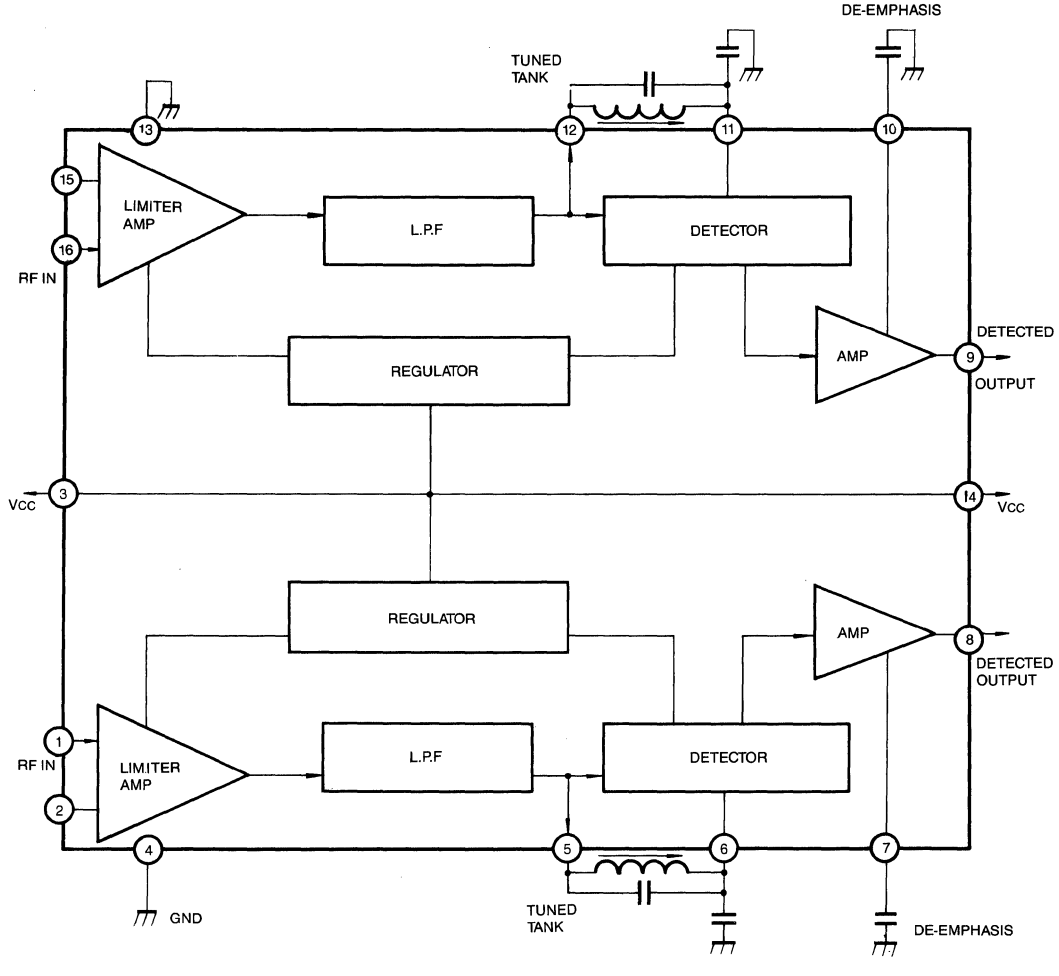
16 Dip Unit: mm



FEATURES

- **Detector with single tuned coil**
- **Excellent a rejection ratio; 50dB (Typ.)**
- **Wide supply voltage range; V_{CC}=8-15V**
- **Minimum numbers of external parts requires.**

BLOCKDIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

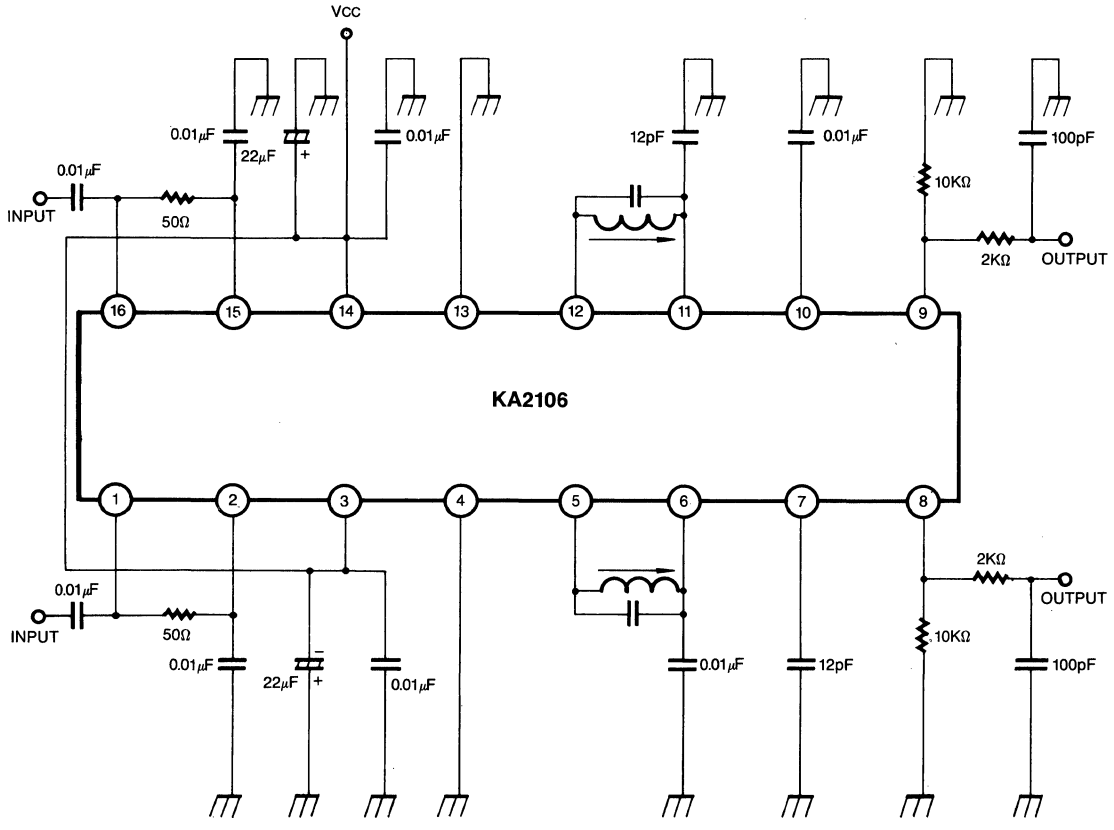
Characteristic	Symbol	Value	Unit
Supply Voltage	V_3, V_{14}	15	V
Input Voltage	V_1, V_{16}	0.7	V_{rms}
Power Dissipation (Note)	Pd	1,250	mW
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

Note: Depated above T_a = 25°C

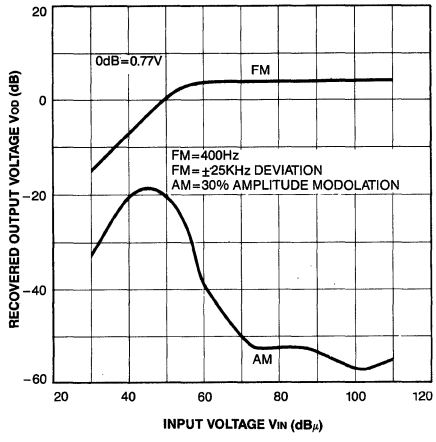
ELECTRICAL CHARACTERISTICS (T_a = 25°C, V_{CC} = 12V)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	—	8	—	15	V
Supply Current		I_{CC}	—	—	—	50	mA
Output Terminal Voltage		V_8	V_{IN} = 0	—	5	—	V
		V_9					
Detected Output Voltage		V_{DD}	F=4.5MHz, FM=400Hz+25KHz, V_{IN} = 100MV	0.8	—	1.6	V_{rms}
Total Harmonic Distortion		THD					
Limiting Sensitivity		V_{IN} (I_{IN})	− 3dB 0 the Max, Output	—	—	500	μV_{rms}
AM Rejection Ratio		AMR	V_{IN} = 100MV_{rms}, FM 25KHz, 400Hz AM M-0.3, 400Hz	—	50	—	dB
Input Impedance	Parallel Input Resistance	RIP	F = 4.5MHz	—	17	—	KΩ
	Parallel Input Capacitance	CIP	F = 4.5MHz	—	4	—	PF
Output Impedance	Parallel Output Capacitance	COP	F=4.5MHz	—	3	—	PF

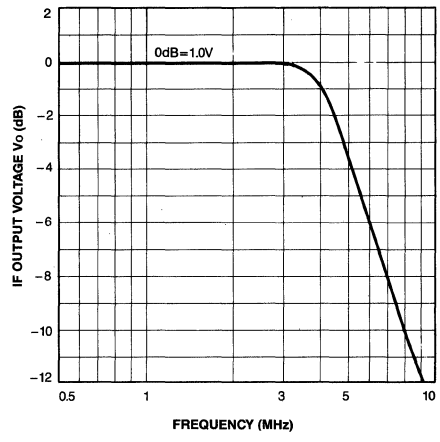
TEST CIRCUIT



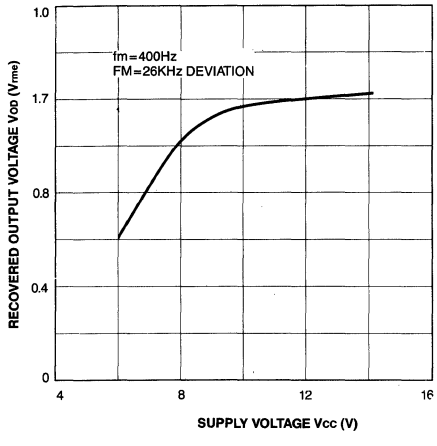
V_{OD}—V_{IN}



V_O—f



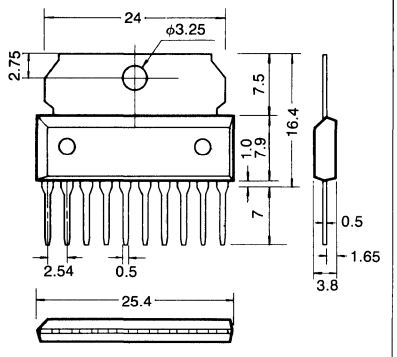
V_{OD}—V_{CC}



TV VERTICAL DEFLECTION SYSTEM

The KA2130A is a monolithic integrated circuit for use in vertical deflection circuit of monochrome and small-sized color television receivers. It oscillates vertical signal synchronizing with vertical synchronization signal and outputs the vertical deflection current with the single chip.

10 Sip H/S Unit: mm



FUNCTIONS

- Vertical synchronization circuit.
- Vertical oscillation circuit.
- Vertical saw-tooth shaper.
- Vertical-output circuit.
- Clamping circuit for blanking pulse.
- Temperature compensating circuit.

FEATURES

- **Less number of external components.**
- **Wide range of operational voltage (9V ~ 18 volts).**
- **Freely adjustable pull-in range.**
- **Adjustable blanking pulse-width.**
- **Large output current-capacity (2 A_{P-P}).**
- **Built-in adjusting circuit for flyback time.**
- **Easy mounting on printed circuit board.**

TYPICAL APPLICATION CIRCUIT

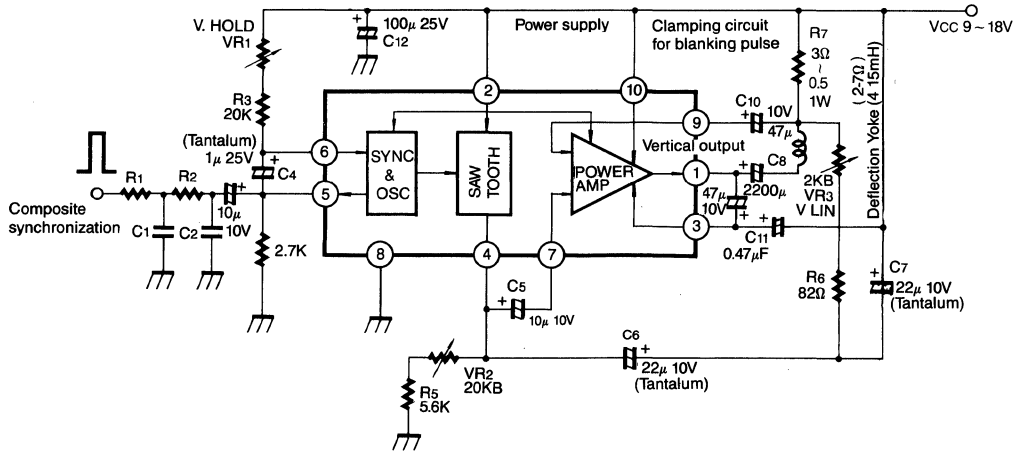


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Output Current	I_{p-p}	2	Ap-p
Power Dissipation	P_{d1}	1.5 (T_a=+75°C) With aluminum heatsink	W
Power Dissipation	P_{d2}	2.15 (T_a=+75°C) With aluminium heatsink (31.6×31.6×1mm t)	W
Operating Temperature	Topr	−20 ~ +75	°C
Storage Temperature	Tstg	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=12V, T_a=25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Circuit Current	I_{CC}	No input signal and no load condition	15	30	46	mA	2
Output Terminal Voltage	V_N	No inupt signal and no load condition	5.6	6.0	6.4	V	2
Vertical Oscillation Frequency	f_V	Synchronization signal voltage applied at terminal 5 is 1.3 V_{p-p}	—	50/60	—	Hz	2
Free-running Frequency	f_{VO}	Oscillation capacitor, 1μF (Tantalum) resistor, 38.1KΩ	53	60	67	Hz	2
Pull-in Range	f_P	With specified integration circuit, applied voltage of synchronization signal is 1.3 V_{p-p} at terminal 5	−10	−12	—	Hz	2
Drift of Free-running Frequency vs. Power Supply Voltage	Δf_{VO}	Frequency drift from standard frequency (f_{VO} 60 Hz at V_{CC} = 12V) vs. power supply voltage (V_{CC} = 12 ± 2V)	—	—	±1.0	Hz	2
Deviation of Pull-in Range vs. Power Supply Voltage	Δf_P	Deviation from the range for pull in (at V_{CC}=12V) vs. power supply voltage (V_{CC}=12±2V)	—	—	±3.0	Hz	2
Output Saturation Voltage	Vsat	Output current: 0.7A	—	1.3	1.6	V	2
Output Pulse Width of Terminal 4	T_O	Oscillation capacitor, 1μF (Tantalum) resistor, 38.1KΩ	300	420	600	μsec	2

TEST CIRCUIT

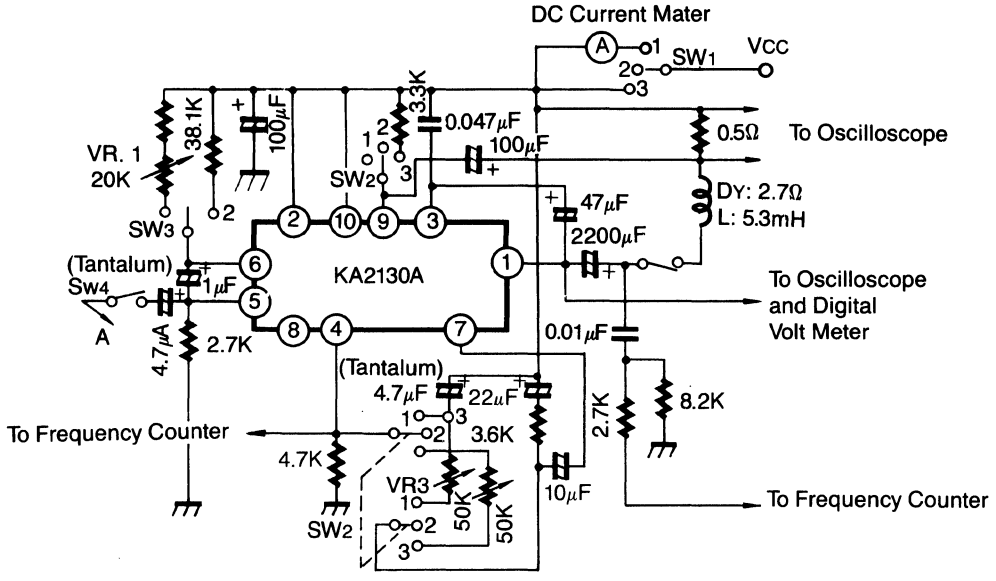


Fig. 2

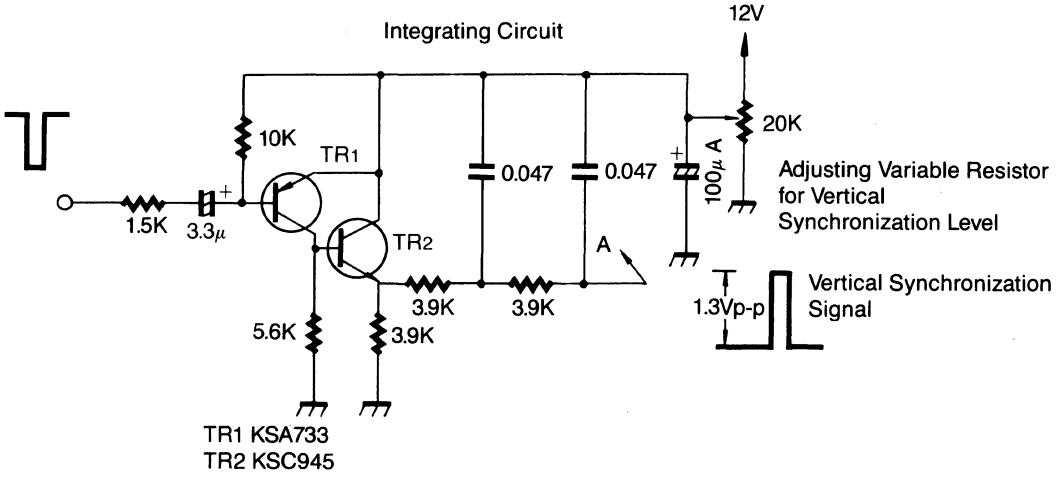
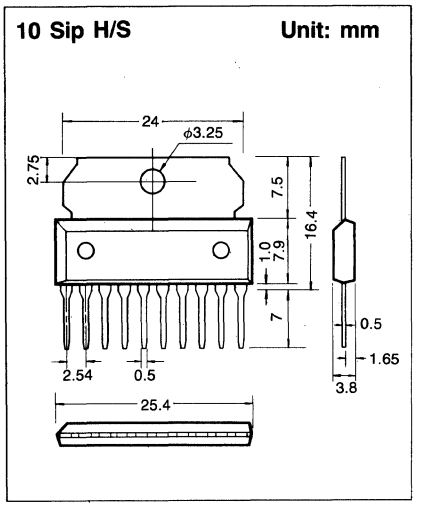


Fig. 3

TV VERTICAL OUTPUT CIRCUIT

The KA2131 is a monolithic integrated circuit designed for vertical output stage in color television receivers.



FUNCTIONS

- Driver stage.
- Output stage.
- Flyback generator.
- Pulse shaper.

FEATURES

- **Low power consumption, direct deflection coil driving capability (Flyback voltage two times as high as supply voltage is supplied during flyback period only).**
- **High breakdown voltage: 60V.**

BLOCK DIAGRAM

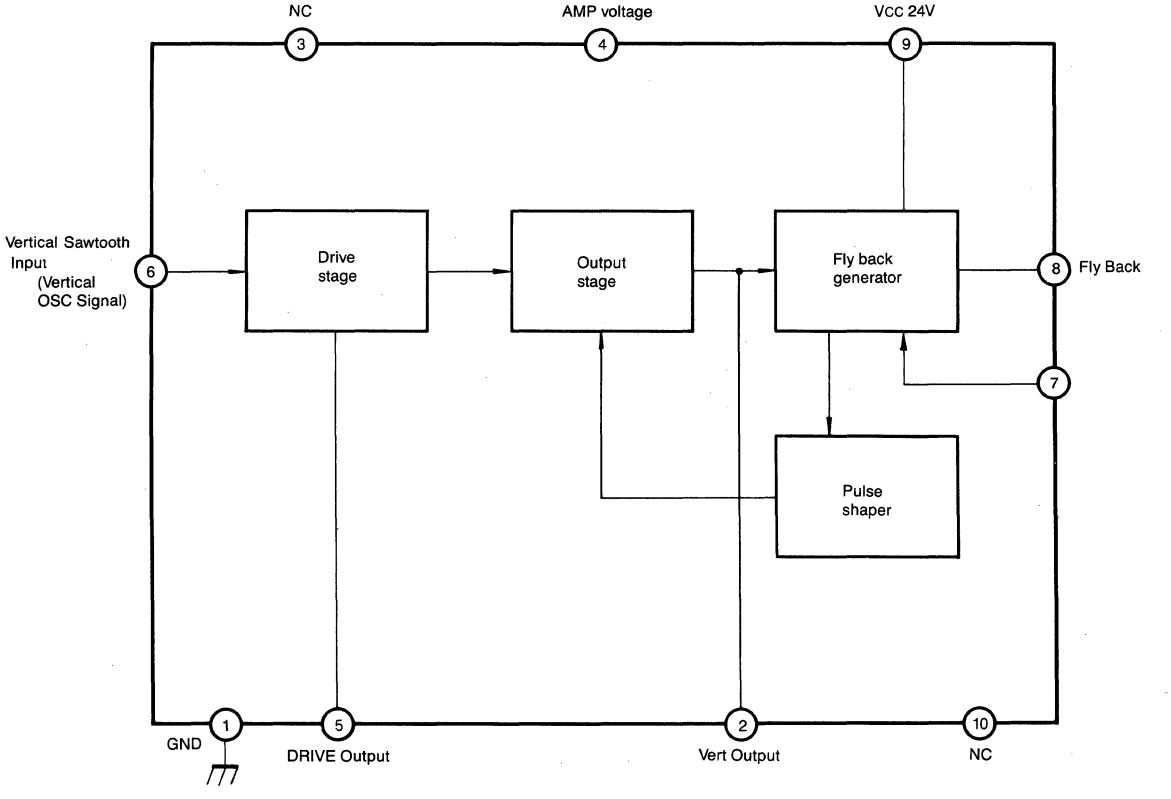
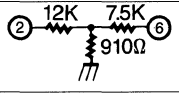


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	27.6	V
Circuit Voltage	V_4	60	V
	V_6	2.5	V
	V_7	1.3	V
Supply Current	I_{CC}	250	mA
Circuit Currnt	I_2	−500 ~ +500	mA_{p-p}
	I_8	−500 ~ +500	mA_{p-p}
Operating Temperature	Topr	−20 ~ +150	°C
Storage Temperature	Tstg	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=24V, T_a=25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Deflection Current	Iyp-p	SW:2	860	930	1000	mA_{p-p}
Deflection Current Linearity	Δly (+)	SW: 1	25	—	75	mA_{p-p}
	Δly (−)	SW:1	22	—	85	mA_{p-p}
Deflection Current vs. Operating Temperature	$\Delta Iy/T_a$	T_a=−20 ~ +70°C	−1.5	—	1.5	%
Center Voltage	V_{MID}	SW: 1	12.1	12.6	13.1	V
Flyback Pulse Amplitude	V(FBP)	SW: 1	47			V
Flyback Pulse Width	t_{FBP}	SW: 1	850	920	980	μsec
Quiescent Circuit Current	I_{CC}	V_4=24V, V_9=24V, V_7=0V 	7	13	22	mA
Output TR Saturation Voltage	V_{4-2}	V_4=V_9=24V, pin_{2-1}=56Ω, V_6=0.3V, V_7=0V	—	2.7	3.7	V
	V_2	V_4=V_9=24V, pin_{2-4}=56Ω, V_6=13V, V_7=0V	—	0.6	1.0	V
Saturation Voltage	V_8	V_9=24V, $Rpin_{9-8}$=1.2KΩ, V_7=0V	—	—	0.5	V
Thermal Resistance	Rth (j-c)		—	—	12	°C/W

TYPICAL APPLICATION CIRCUIT

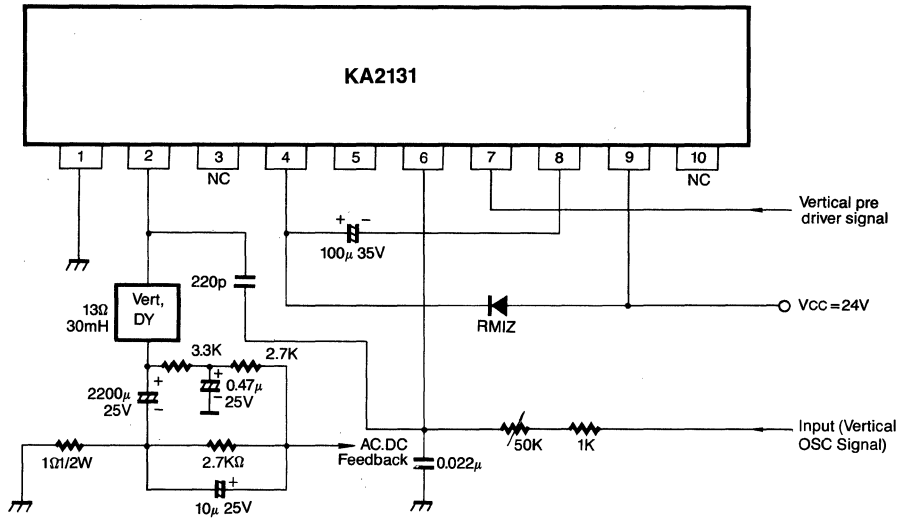


Fig. 2

TEST CIRCUIT

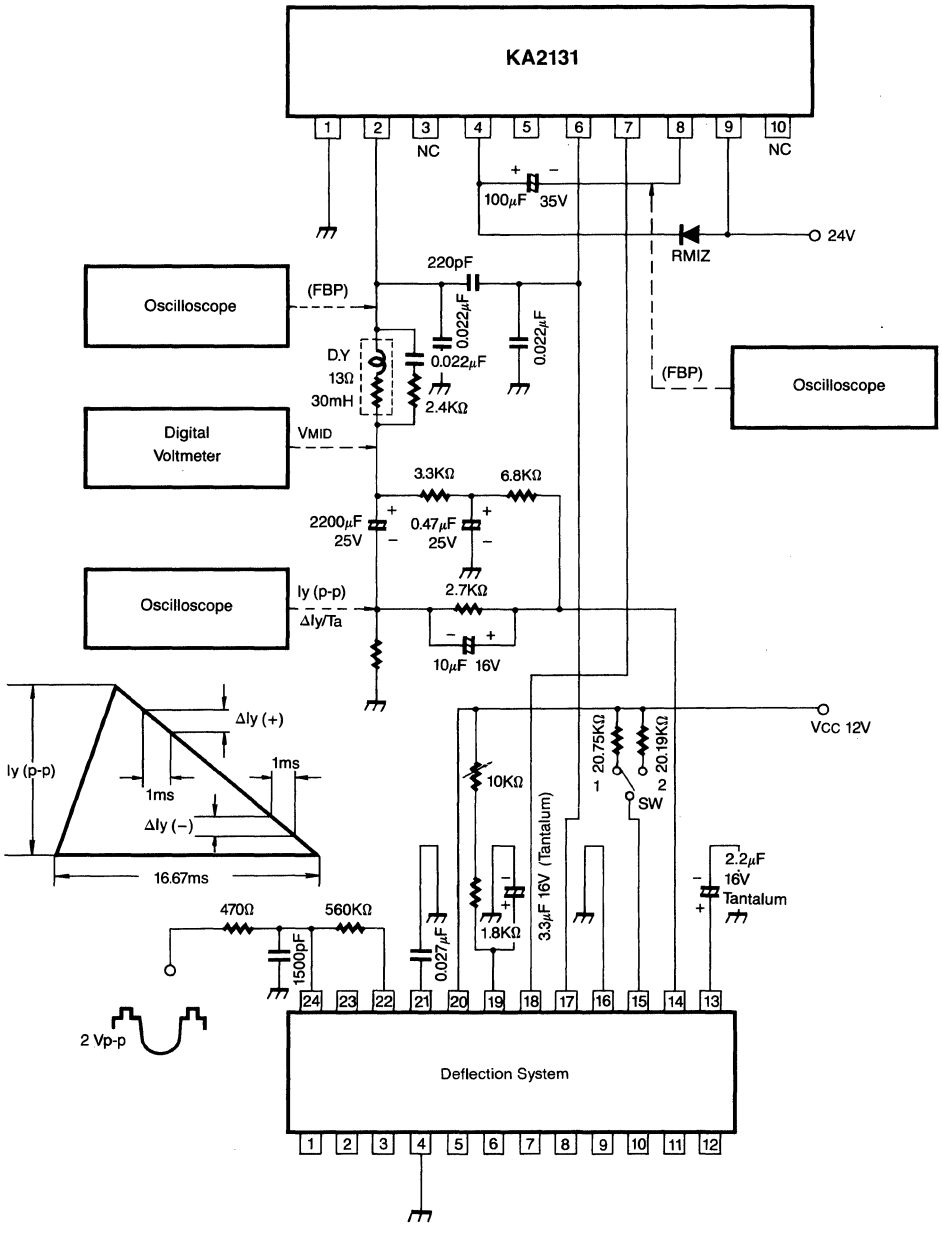
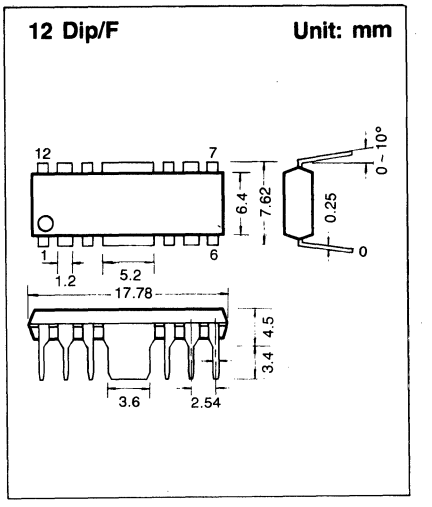


Fig. 3

TV VERTICAL DEFLECTION SYSTEM

The KA2132 is a monolithic integrated circuit containing all stages for the vertical deflection of television receivers, Monitor.



FUNCTIONS

- Linear sawtooth generator
- Geometric "S" correction circuit
- Flyback booster
- Output amplifier

FEATURES

- **Wide range of operational voltage (11V ~ 27V).**
- **Minimum number of external parts required**
- **High break down voltage: 60V**

TYPICAL APPLICATION CIRCUIT

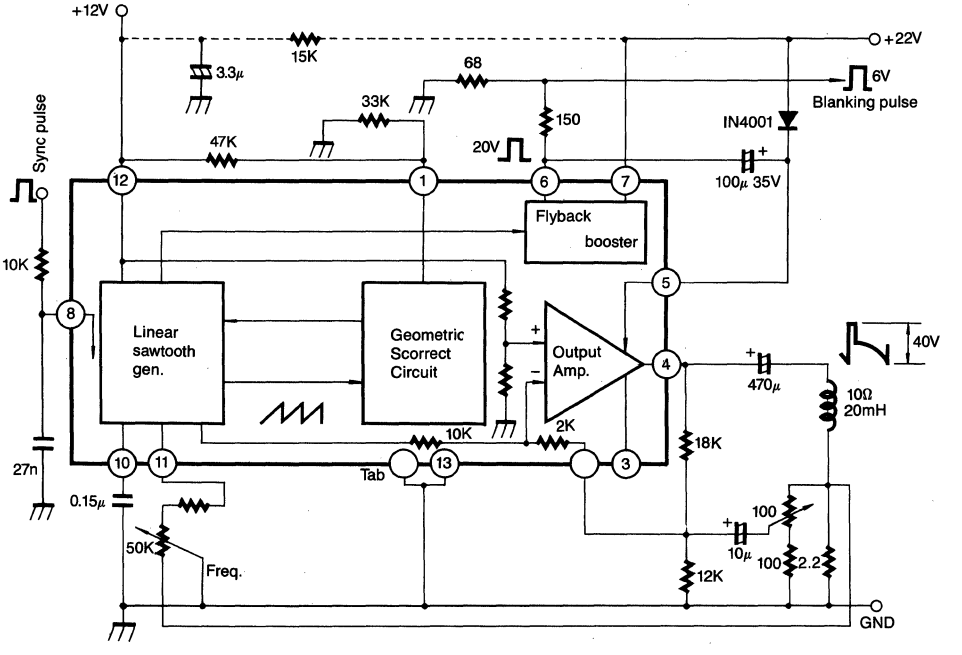


Fig. 1

RECOMMENDED OPERATING CONDITIONS (T_a =25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Supply Voltages	V_7		—	22	—	V	3
	V_{12}		—	12	—	V	3
Amplitude of Positive Sync Pulse	V_8		—	8	—	V	3
Ambient Operating Temperature Range	T_a		0		60	°C	3
Termal Resistance of the copper-clad area soldered to the cooling tabs.	Rths		—	15		°C/W	3

TEST CIRCUIT 1

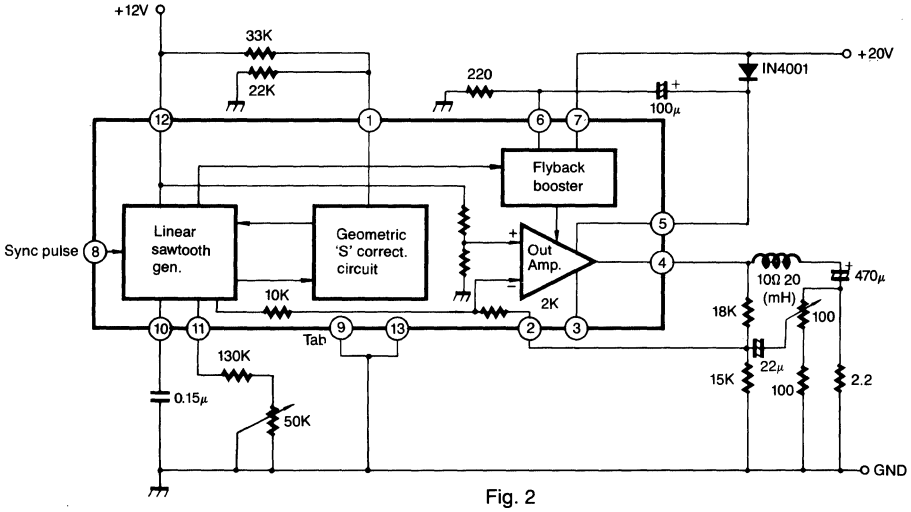


Fig. 2

TEST CIRCUIT 2

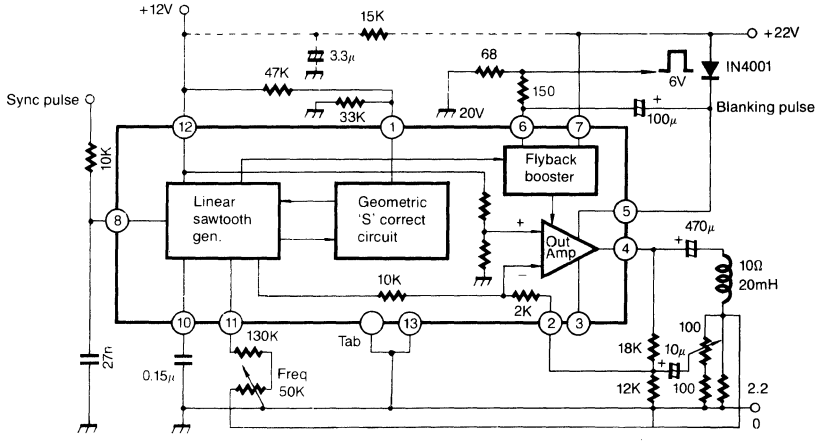


Fig. 3

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{12}	22	V
Operated with Flyback Booster	V_5	27[1]	V
	V_7	30	V
Input Voltage	V_8	−6	V
Input Current	I_8	2	mA
Output Current	$I_{4p\text{-}p}$	1	A
Flyback Current	I_6	0.5	A
Current Consumption	I_7+1_5	300	mA
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	−25 ~ +100	°C

1) during flyback pulse: 58V

ELECTRICAL CHARACTERISTICS (T_a=25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Current Consumption	I_5+I_7		—	140	—	mA	2
	I_{12}		—	12	—	mA	2
Adjustment Range of Deflection Current	I_{4pp}		0.4	—	0.9	A	2
Flyback Duration	t_{fly}		—	1	—	msec	2
Input Impedance	r_8/13		—	10	—	KΩ	2
Frequency of the Sawtooth Generator	f_B	R11/13 > 50Ω	$\frac{1.6}{R_{11/13}\,C_{10/13}}$			—	2
Adjustment Range of Sawtooth Generator	f_B/f_B		—	10	—	%	2
DC Voltage at pin 11	V_{11}	C10/13=0.15μF, f_B=50Hz	—	9.7	—	V	2
DC Current at pin 11	$-I_{11}$		—	45	—	μA	2
Required Sync Pulse amplitude at pin 8							
with picture sync signal	V_8		1	—	10	V	2
with negative sync signal	V_8		−1.3	—	−6	V	2
Geometric Distortion related to standard picture tube and standard deflection unit 1)	ΔI/I		—	3	—	%	2

1) Tangent correction can be made adjustable by potentiometers. The curvature of the deflection current S-curve may be changed by a series resistor connected to pin 1. The DC voltage at pin 1 is responsible for the up/down correction. This voltage derives from the supply voltage V_{12} and the divider ratio of the voltage divider at pin 12 and pin 1. If fixed resistors are used a ratio of approximately 1.45 for $R_{12/1}$ to $R_{1/3}$ should be observed.

APPLICATION CIRCUIT 1

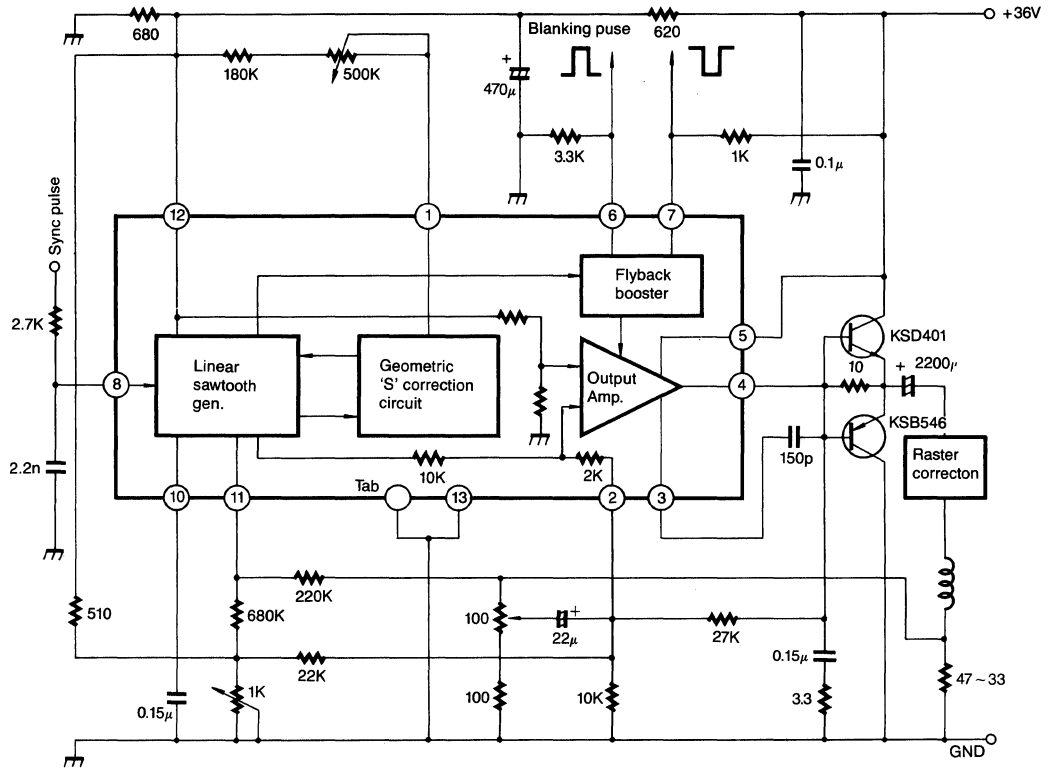


Fig. 4

Fig. 4: Application circuit for the KA2132 in color TV receivers. The geometric correction circuit is designed for picture tubes type 20 AX and must be modified for different types. The picture height is not influenced by the adjustment of the "Frequency" potentiometer. The duration of the blanking pulses is equal to the flyback duration and therefore depending on resistance and inductance on the deflection coil. The 150pF capacitator at pin 3 and pin 4 and also the Boucherot circuit 0.15μpoint at pin 4 and GND prevent any parasitic oscillation of the output amplifier. Dimensioning depends on the relation L/R of the vertical deflection coil. The higher this relation the more compensation (more capacitance and les resistance) is required. Both compensations are not required with usual black and white deflection coils.

APPLICATION CIRCUIT 2

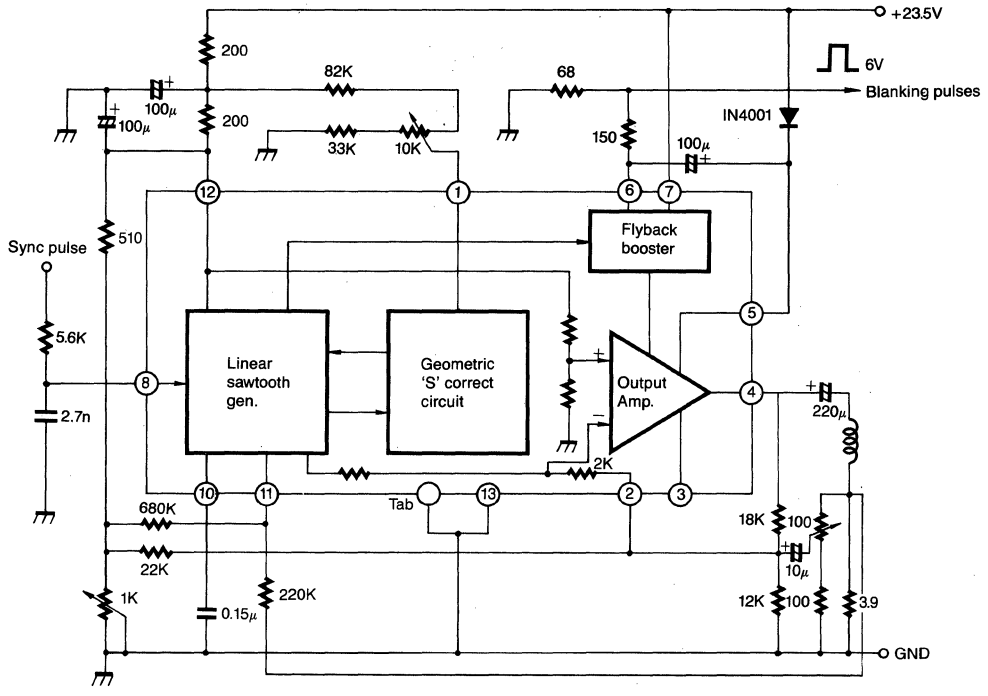


Fig. 5

Fig. 5: application circuit for the KA2132 in black and white TV receivers showing a more extended frequency adjustment circuit. this ensures a constant vertical deflection current during any adjustment of the "Frequency" potentiometer.

APPLICATION CIRCUIT 3

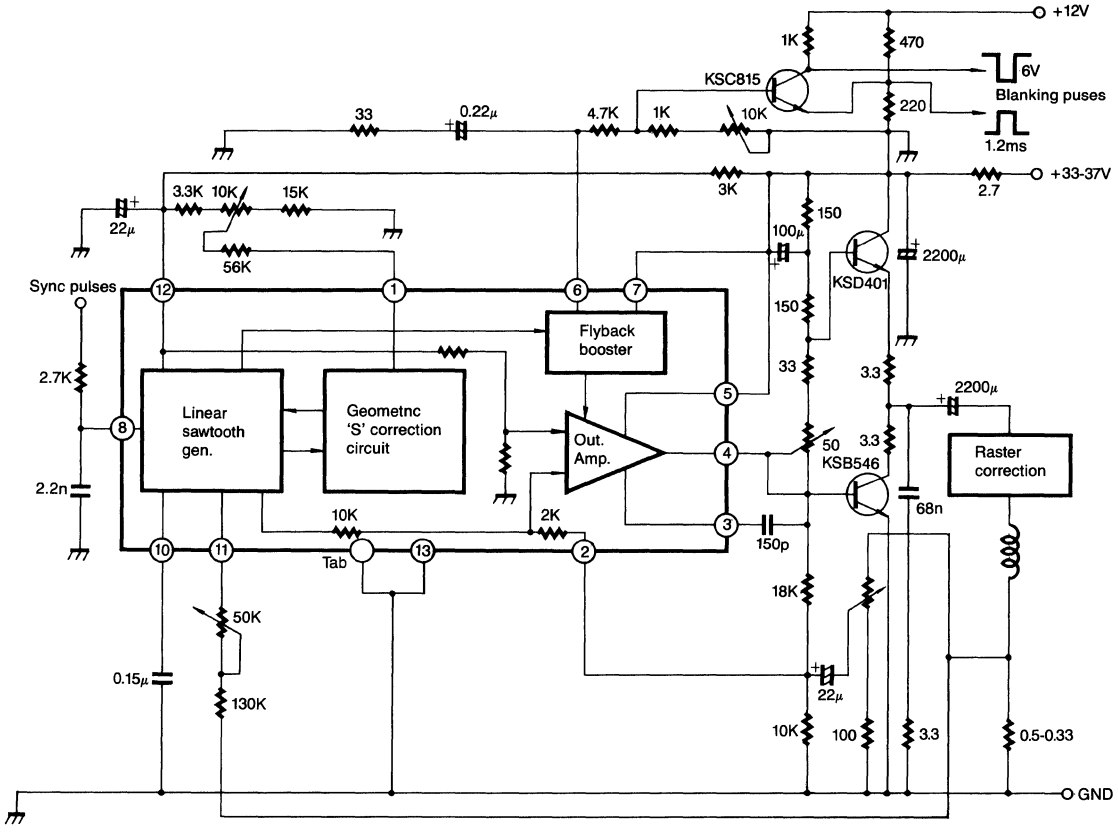


Fig. 6

Fig. 6: Application circuit for the KA2132 in CTV Receivers. The geometric correction circuit is designed for picture tubes type 20 AX and must be modified for different types. For the compensation network at pin 3 and the output the legend of Fig. 4 is also valid. A pulse shaper containing a transistor KSC815 is connected to pin 6. It ensures a constant duration of the blanking pulses (approx. 1.2 ms) independent of the flyback duration and the L/R ratio of the vertical deflection coil.

APPLICATION CIRCUIT 4

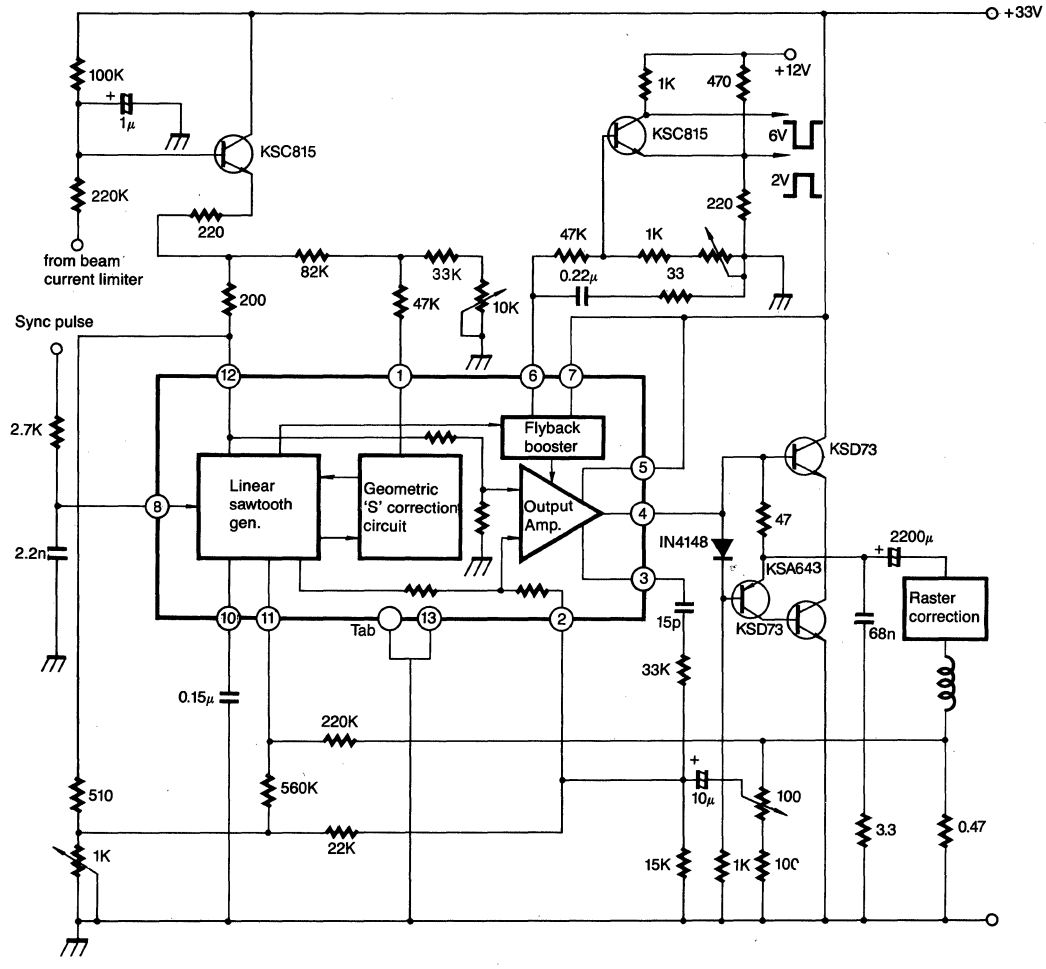


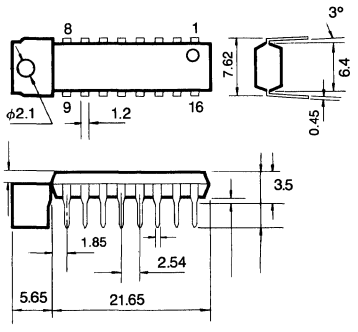
Fig. 7

Fig. 7: Application circuit for the KA2132 in color TV receivers. The geometric correction circuit is designed for in-line picture tubes and must be modified for different types. For the compensation network at pin 3 and at the output the legend of Fig. 4 is also valid. A pulse shaper as described in the legend of Fig. 6 is connected to pin 6. Adjustment of the "Frequency" potentiometer does not influence the picture height. Via a transistor KSC815 the beam current limiter influences the supply voltage of the sawtooth generator at pin 12 and subsequently the picture height. Higher beam current results in a lower hightension and enlarged picture (at constant deflection current). Reducing the oscillator amplitude via the supply voltage at pin 12 keeps constant the picture height.

I CHIP DEFLECTION SYSTEM

The KA2133 consists of vertical system including output function and a horizontal system including AFC function. It is for use in small size color TV, B/W TV receivers and monitor designed.

16 Dip H/S Unit: mm



FUNCTIONS

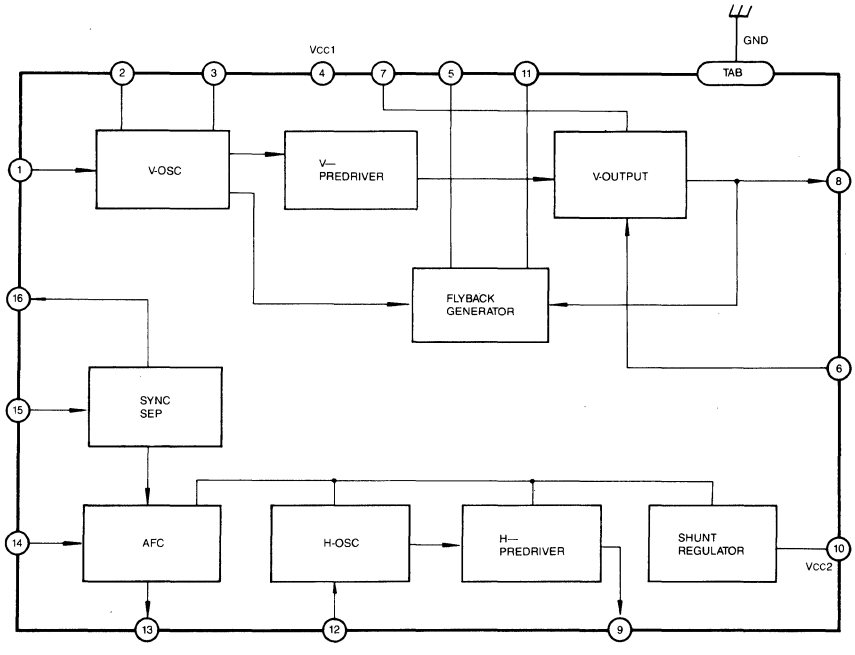
(Horizontal Section)
- SYNC separator
- Horizontal oscillator
- Horizontal predriver
- Horizontal AFC
- Shunt regulator (Typ.: 6.7V)

(Vertical Section)
- Vertical oscillator
- Vertical predriver
- Vertical output
- Flyback generator

FEATURES

- **Low power consumption, direct deflection coil driving capability (flyback voltage two times as high as supply voltage is supplied during flyback period only)**
- **Variable circuit of vertical retrace time on chip.**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Vertical Supply Voltage	V_{CC}	15	V
Horizontal Supply Current	I_{10}	30	mA
Vertical Output Current	I_8	−500 ~ +500	mA peak
Horizontal Output Current	I_9	−10 ~ +10	mA
Flyback Generator Output Current	I_5	−500 ~ +150	mA peak
Power Dissipation	P_d	1.2	W
Operation Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−40 ~ +150	°C

SUGGESTION CONDITION (T_a = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Vertical Supply Voltage	V_{CC}	9.6	12.0	14.4	V
Horizontal Supply Current	I_{10}	6.5	12	18	mA

ELECTRICAL CHARACTERISTICS

(V_{CC} =12V, I_{10} =12mA, T_a =25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Vertical Supply Current	I_{CC} (1)	SW_A =2	—	85	140	mA	1
Vertical Supply Current	I_{CC} (2)	No Input Signal SW_A =2	—	—	50	mA	1
Vertical Free Running Frequency	f_{VO}	SW_A =1	55	60	65	Hz	1
Vertical Free Running Frequency Operating Vertical Free Running	Δf_{RO} (V_{CC})	Δf_{VO} =1f_{VO} (14.4V)-f_{VO} (9.6V)1 SW_A =2	—	0.9	2	Hz	1
Frequency Operating Temperature	Δf_{VO} (T_a)	Δf_{VO} =1f_{VO} (−20°C)− f_{VO} (+75°C)1 SW_A =2	—	0.8	2	Hz	1
Vertical Output Center Voltage	V_{MID}	SW_A =2	5.3	5.8	6.3	V	1
Vertical Output Current	I_8	SW_A =2	450	500	550	mA_{p-p}	1
Horizontal Supply Pin Voltage	V_{10}	SW_B =2	6.2	6.7	7.2	V	1
Horizontal Free Running Frequency	f_{HO}	I_{10} =12mA SW_B =1	15.0	15.75	16.5	KHz	1
Horizontal Output Pulse Width	P_{WH}	f_{HO} =15.75KHz SW_B =2	20	25	30	us	1
Horizontal Output Current	I_9	SW_B =2	−10	−1.5	−2.0	mA	1

TEST CIRCUIT

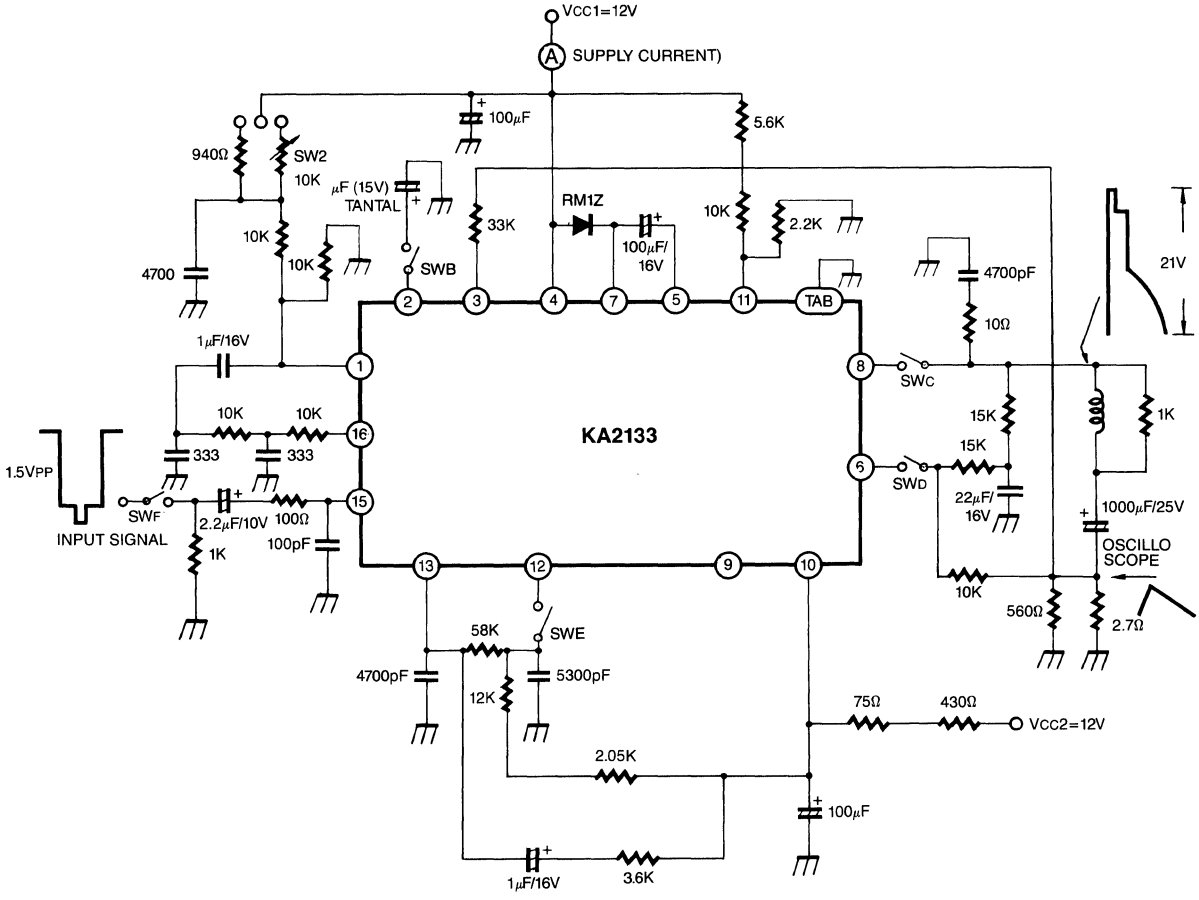


Fig. 2

TYPICAL APPLICATION CIRCUIT

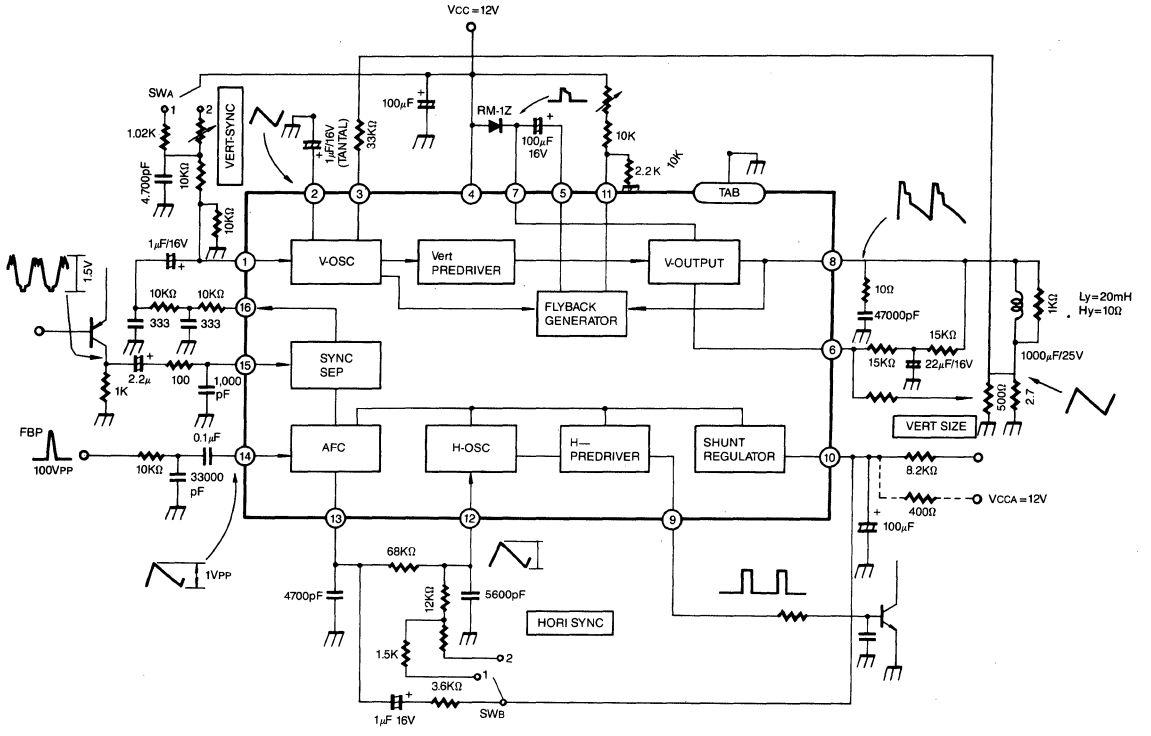
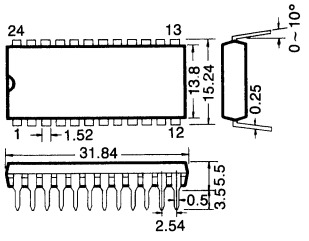


Fig. 3

CHROMINANCE SIGNAL PROCESSOR FOR PAL SYSTEM

The KA2151 is a silicon monolithic integrated circuit designed for chrominance signal processor in color television receivers. (PAL SYSTEM)

24 Dip Unit: mm



FUNCTION

- Chroma amplifier
- DC Uni-color control
- APC phase detector
- Matrix circuit
- DC chroma gain control
- Burst amplifier
- ACC peak detector
- Killer detector
- Voltage controlled oscilator
- PAL switch
- Flip flop

FEATURES

- **Having a whole color signal processing function.**
- **Minimum number of external parts required.**
- **In order to stabilize the operation of the phase detector in the APC circuit under poor receiving condition, DC feed back technique is provided.**
- **The VCO consists of a low pass RC circuit, so that there is no possibility of an undesirable parasitic oscillation.**
- **It needs no tank circuit and consequently no initial adjustment is required in the VCO circuit.**
- **As the reference signals reproduced in the VCO are fed internally without passing through a tuning circuit, adjustment is not needed.**
- **The ACC level is internally defined.**

BLOCK DIAGRAM

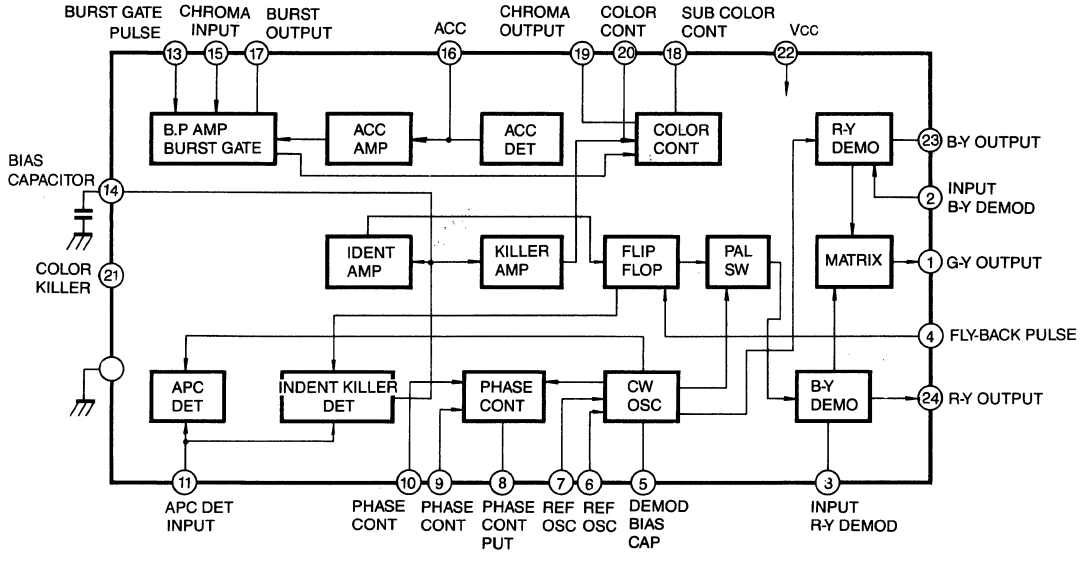


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Power Dissipation (T_a=65°C)	Pd	720	mW
Signal Level at Input Pin	Vin	5	V_{p-p}
Load Resistance at Demodulator	R_L	min 1.8	KΩ
Gate Pulse Input Voltage	Vp	±6	V
Thermal Resistance	R_{th}	108	°C/W
Flip-Flop Drive Pulse	e_f	±5	V
Operating Temperature	Topr	−20 ~ +65	°C
Storage Temperature	Tstg	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12V, T_a = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Supply Current	I_{CC}	S_1=2, S_2=1	34	46	65	mA	4
Maximum Chroma Output Voltage	V_C	S_1=1, S_2=1, S_3=1 e_{in}=100mV_{p-p} Pin 19	0.5	0.7	1.0	V_{p-p}	1
Burst Output Voltage	V_b		1.0	1.3	1.7	V_{p-p}	1
ACC Range	V_a	S_1=2, S_2=1, S_3=1 e_{in}=14mV_{p-p} Pin 17	0.7	—	—	V_{p-p}	1
Killed Chroma Output Voltage	V_k	S_1=1, S_2=1, S_3=2 V_{in}=100mV_{p-p} Pin 19	—	—	3	mV_{p-p}	1
Min Gain Chroma Output Voltage	V_s	S_1=1, S_2=3, S_3=1 V_{in}=100mV_{p-p} Pin 19	—	—	3	mV_{p-p}	1
Terminal Voltage 18	V_{18}	S_1=2, S_2=1, S_3=1	6.9	7.4	7.9	V	1
Color Control Voltage	V_{20}	S_1=1, S_2=1, S_3=1 V_{in}=100mV_{p-p} When V_C being reduced to half	—	8.3	—	V	1
Unicolor Control Characteristic	ΔV_{03}	S_1=3, S_2=1, S_3=1 V_{in}=100mV_{p-p} V_{18}=5.9 ~ 8.9V Signal Change of Pin 19	9	10	12	dB	1
Phase Shift by Unicolor Control	$\Delta\phi$	S_1=3, S_2=1, S_3=1 e_{in}=100mV_{p-p} 4.43MHz CW V_{18}=0V ~ 12V Phase shift of Pin 19	—	4	7	deg	1
APC Detector Output Balance	V_P	S_1=1, S_2=2, S_3=1 Difference in Voltage between Pin 9 and 10	−50	0	+50	mV	2

ELECTRICAL CHARACTERISTICS (T_a =25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
APC Pull-in Range	f_p	S_1=2, S_2=1, SΔ3=2 Adj. V_9-V_{10} for f_o ±10Hz S_1=1, S_2=1, S_3=2 Vary F_{11} & measure f_p	±240	±350	—	Hz	2
VCO Frequency Control Sensitivity	β	S_1=1, S_2=1, S_3=1 Measure V_9-V_{10} at Δf=100Hz	—	1.0	—	Hz/mV	2
Phase Detector Sensitivity	μ	S_1=1, S_2=2, S_3=1 Measure V_9-V_{10} at $\Delta\phi$=10°	—	−25	—	mV/deg	2
VCO Frequency Stability V_S V_{22}	f_{av}	S_1=2, S_2=1, S_3=1 V_{22}=12±1V	−20	0	+20	Hz	2
Temp-Stability of APC Detector	ΔV_{pt}	S_1=1, S_2=1, S_3=1 V_b=100mV_{p-p} T_a=0~60°C	−70	0	+70	mV	2
Burst Level for Killer & Ident	V_i	S_1=1, S_2=1, S_3=1 at V_{20}≧10V	30	80	150	mV_{p-p}	2
Demodulator DC Output Voltage	V_{ODC}	S_1=2, S_2=1, S_3=1	6.6	7.2	7.8	V	3
Temp. Coeffi, of Demodulator DC Output Voltage	$\frac{e\Delta V_{ODC}}{eT}$	T_a=−20~65°C	−3	0	+2	mV/°C	3
DC Voltage Difference between Any Demodulator Output Terminal	ΔV_{ODC}	S_1=2, S_2=1, S_3=1 Vtg Difference among Pin 1, 23 & 24	−0.3	0	+0.3	V	3
Temp. Coeffi, of Demodulator Output Voltage Differences	$\frac{e\Delta E_{ODC}}{eT}$	S_1=2, S_2=1, S_2=1 T_a=−20~65°C	−2	0	+2	mV/°C	3
Color Difference Output Voltage	V_{OB}	S_1=2, S_2=1, S_3=1 V_{CW}=0.2V_{p-p} 4.44MHz Pin 1, 23, & 24 (10KHz Beat)	—	2.4	—	V_{p-p}	3
	V_{OB}		—	1.45	—		
	V_{OG}		—	0.65	—		
Maximum Color Difference Output Voltage	V_{OM}B V_{OM}R V_{OM}G	S_1=1, S_2=1, S_3=1 e_{CW}=1.2V_{p-p} 4.44MHz Pin 1, 23 & 24 (10KHz Beat)	4.5 4.5 1.5	5.5 5.5 2.0	— — —	V_{p-p}	3
Relative Amplitude	B-Y/R-Y	S_1=3, S_2=1, S_3=2, V_{CW}=0.2V_{p-p} 4.44MHz (10KHz Beat)	—	1.65	—	—	3
	G-Y/R-Y		—	0.45	—		
Demodulator Phase	θ_{R-Y}	S_1=3, S_2=1, S_3=2 V_{CW}=0.2V_{p-p} 4.43MHz	83	90	97	deg	3
	θ_{R-Y}		222	236	250		
Residual Carrier	Vcar	S_1=1, S_2=2, S_3=1 4.43MHz	—	—	0.2	V_{p-p}	3
Demodulator Frequency Characteristics	f_D	S_1=1, S_2=2, S_3=1 V_{CW}=0.2V_{p-p} 4.44~7MHz 3dB band width	0.8	1.5	—	MHz	3

ELECTRICAL CHARACTERISTICS (T_a =25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Residual Harmonics	Vharm	S_1 =1, S_2 =2, S_3 =1 V_{CW} =1.2V_{p-p} 4.44MHz	—	—	2.2	V_{p-p}	3
Output DC Voltage Change by PAL switch	V_{SW}	S_1 =2, S_2 =1 V_{in} =0mV_{p-p} DC Deviation on each scanning	—	—	50	mV_{p-p}	4
Carrier Leak in B.P.	Vleak	S_1 =1, S_2 =2 V_{in} =0mV_{p-p}, Carrier Component Output of Pin 19	—	—	14	mV_{p-p}	4

TYPICAL APPLICATION CIRCUIT

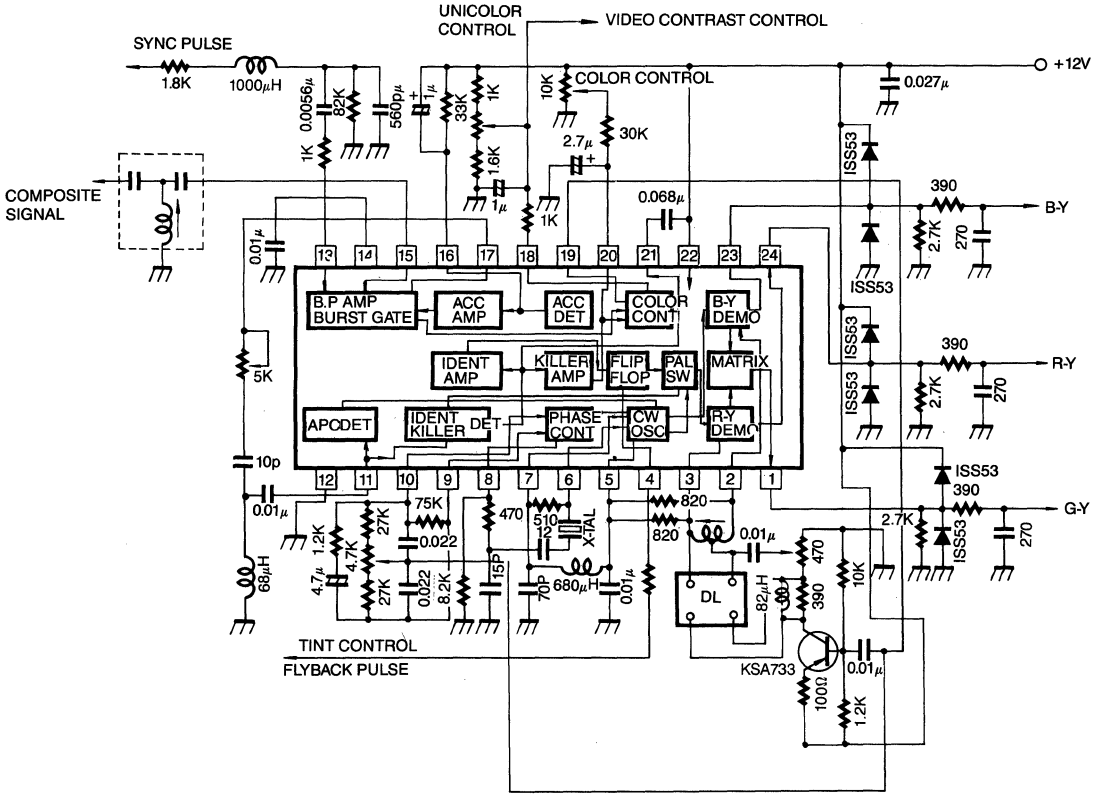


Fig. 2

TEST CIRCUIT 1

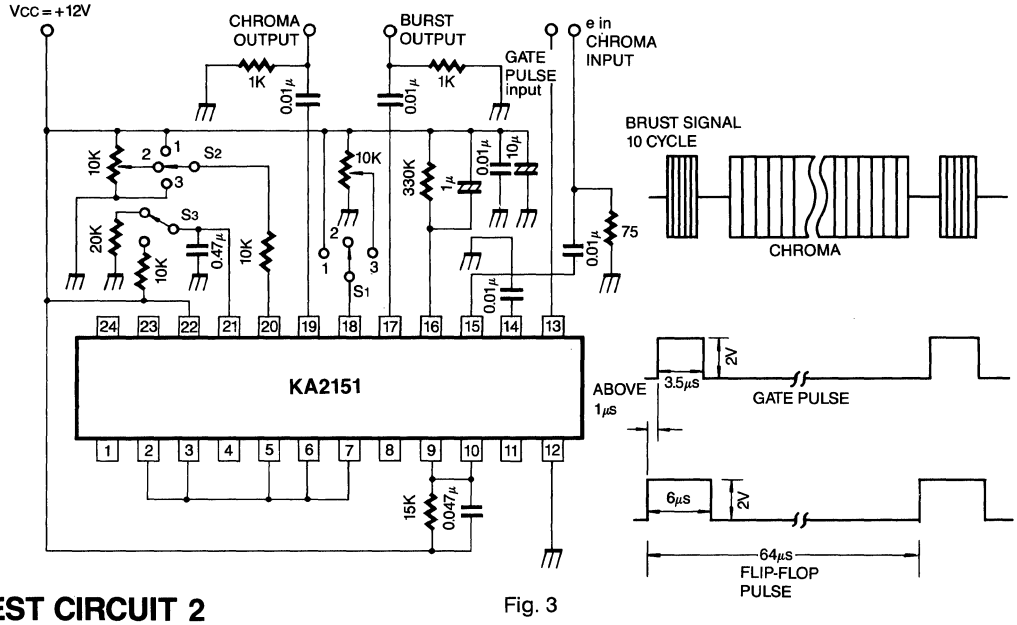


Fig. 3

TEST CIRCUIT 2

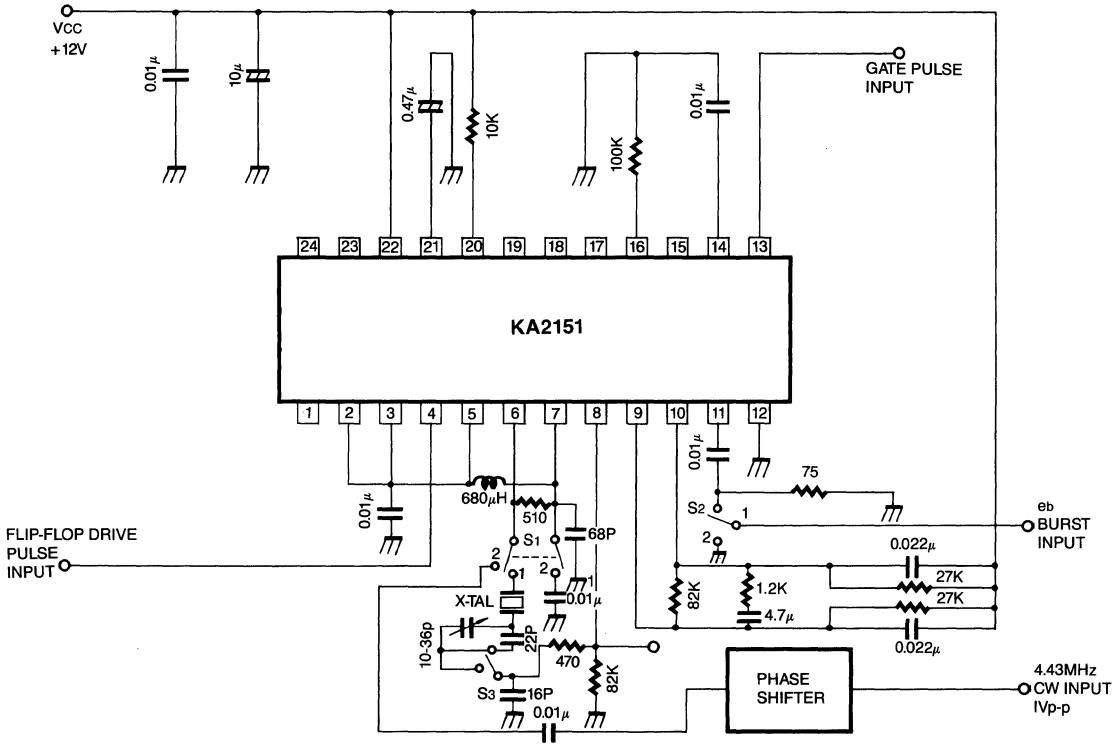


Fig. 4

TEST CIRCUIT 3

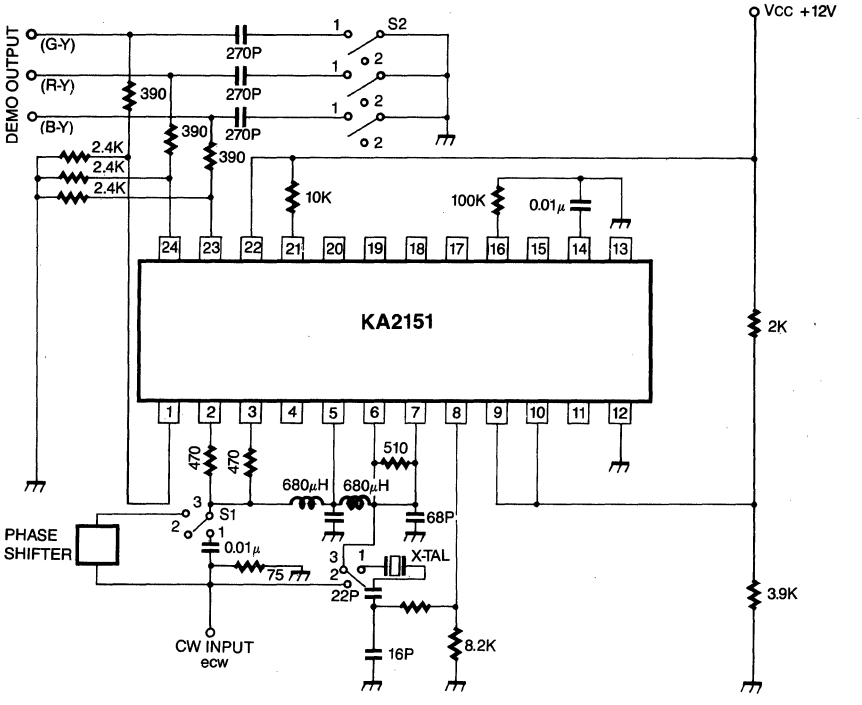


Fig. 5

TEST CIRCUIT 4

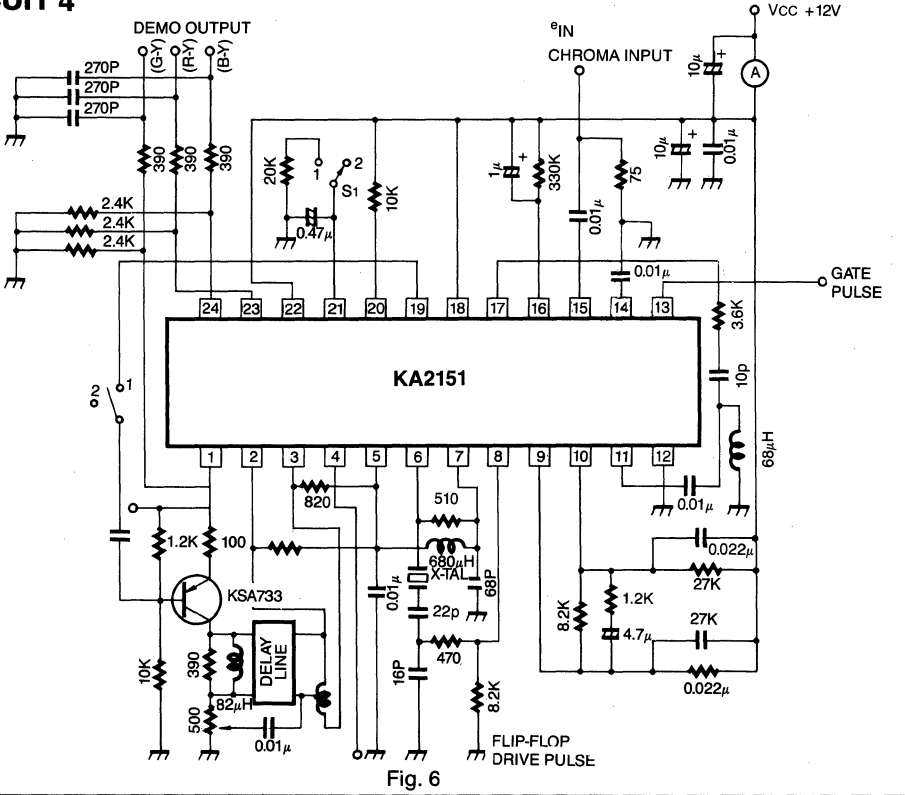
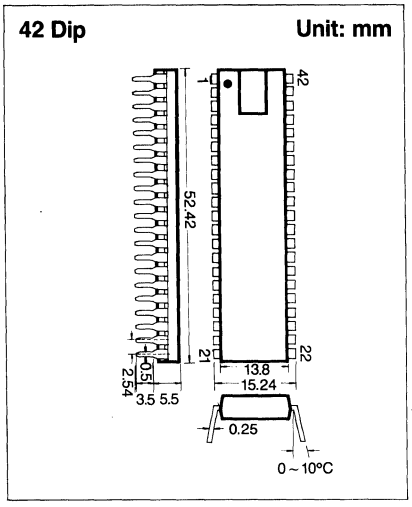


Fig. 6

VIDEO-CHROMA DEFLECTION SYSTEM FOR A COLOR TV (NTSC)

The KA2153 combines the video-chroma sub-system and the deflection combination on a single monolithic integrated circuit to provide a color television video-chroma deflection system.

This device includes a video amplifier, color demodulator that is designed to provide color differential output, and improved syncseparator, horizontal oscillator with saw tooth wave type AFC, horizontal pre-driver with X-ray protection circuit, and vertical oscillator, vertical pre-driver in a 42 leads dual in-line type plastic package.



FUNCTIONS

- Inverter-amplifier
- Contrast control
- Pedestal clamp
- Brightness control
- ACC-amplifier
- Tint control
- Uni-color control
- 3.58MHz V_{CO}
- APC
- Color-Killer
- Color demodulator
- Matrix circuit
- Sync-separator (H.V.sync in)
- $2f_H$ horizontal oscillator
- Flip-flop
- Stabilized horizontal V_{CC} by zener diode
- Horizontal pre driver
- Gate pulse generator
- Vertical sync input
- Vertical oscillator
- Ramp generator

FEATURES

Video-Chroma Section

- **Minimum numbers of external parts required.**
- **Stabilized with respect to variation of temperature and supply voltage.**
- **A few initial adjustment required.**

Deflection Section

- **Excellent temperature stability of horizontal oscillator.**
- **Exact 50% duty cycle output due to the 2-f_H oscillator and flip-flop circuit.**
- **Excellent interrace.**
- **Stable Sync separator with V/H input terminals.**

BLOCK DIAGRAM

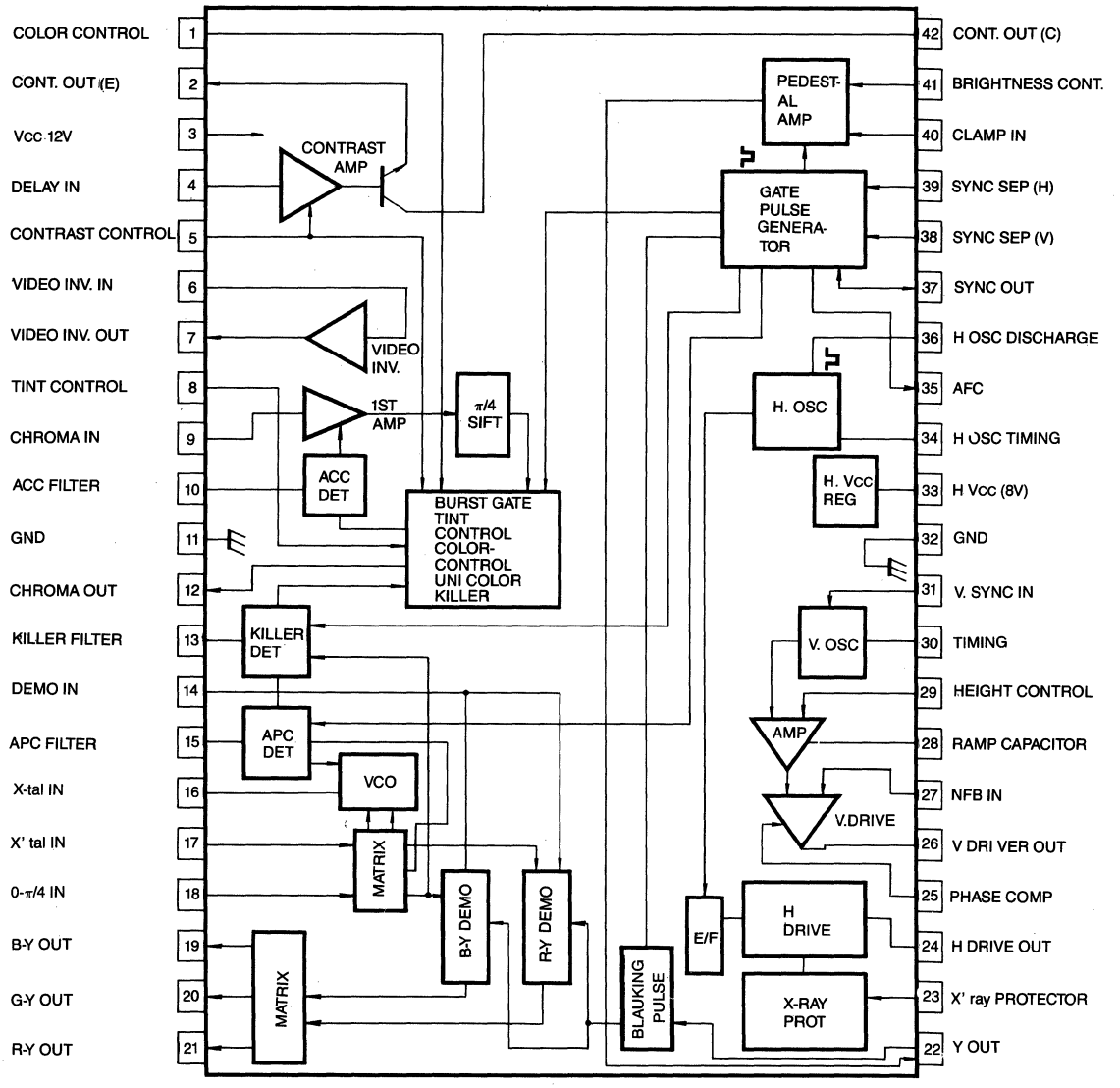


Fig. 1

MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_3 Max	15	V
Supply Current	I_{33} Max	40	mA
Input Signal Level	V_{in}	5	V_{p-p}
Demo. Min. Load Resistance	R_{LD}	1.8	KΩ
Horiz. Drive Peak Current	$-I_{24}$ Max	30	mA
Horiz. Drive Operating Current	$-I_{24}$	15	mA
Vert. Output Current	I_{26} Max	−5	mA
Syncseparator Input Level	V_{38} Max V_{39} Max	8	V_{p-p}
Term. 1 Max Operating Current	I_7	5	mA
Term. 2 Max Operating Current	I_2	4	mA
Power Dissipation (Note)	P_d	2.2	W
Operating Temperature	Topr	−20~65	°C
Storage Temperature	Tstg	−55~150	°C

Note: Derated above T_a =25°C in the proportion of 17.6mW/°C.

ELECTRICAL CHARACTERISTICS
VIDEO SECTION (Unless otherwise specified, V_3 =12V, T_a =25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
12V Supply Current	I_{CC3}	Measure term. 3 current	60	82	100	mA	1
Video Gain	V_{22}/V_6	V_6 =4.25V, V_6:4.0MHz, 1.0V_{p-p}, V_5 =10V, V_B =8.0V	2.0	3.5	5.0	dB	2
Contrast Gain Control Range	ΔG_V	V_6 =4.25V, V_6:500KHz, 1.0V_{p-p}, V_5: 5~10V 20 log (V_{22} (max)/V_{22} (min))	11.2	12.3	13.4	dB	2
Video Frequency Characteristics	ΔG_{vf}	V_6 =4.25V, V_5 =10V, V_B =8.0V V_6 =4.0MHz, 0.5MHz 1.0V_{p-p} 20 log (V_{22} (4MHz)/V_{22} (0.5MHz))	−3.5	−1.5	0.5	dB	2
DC Restoration Ratio	K	V_{41} =4.1V Change APL 10% to 90% Measure pedestal level change of term. 22	63	70	77	%	2
Maximum Video Output	V_V MAX.	Term. 5 open. change V_{40} DC voltage, measure 90% of voltage change at term. 22	5.0	7.5	—	V_{p-p}	2

ELECTRICAL CHARACTERISTICS
VIDEO SECTION (Unless otherwise specified, V_3 =12V, T_a =25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Video DC Output Therm. Co-effic.	$\delta V_{22}/\delta T$	V_6 =3.25V, V_{41} =4.1V T_a = −20 ~ +65°C	−2.5	0	2.5	mV/°C	2
Inverter Amplifier Gain	V_7/V_6	V_6 =4.25V, V_6: 4.0MHz, 1.0V_{p-p}, V_5 =10V, V_B =8.0V	2.2	3.5	4.6	dB	2
Inverter Amplifier Differential Gain	DG_R	V_6: 3.3 ~ 5.2V V_6: 3.58MHz, 100mV_{p-p}	—	2.5	10	%	2
Inverter Amplifier Differential Phase	DP_R	The same condition as above	—	3	5	deg	2
Inverter Amplifier Frequency Characteristics	ΔG_{Rf}	V_6 = 4.25V, V_5 = 10V, V_B = 8.0V, V_6: 4.0MHz, 500KHz, 1.0V_{p-p} 20 log (V_7 (4MHz)/V_7 (0.5MHz)	−3.5	−0.1	0.5	dB	2
Inverter Amplifier 3.58MHz Linearity	L_7	V_6 =4.0V, V_6 =3.58MHz	1.6	—	—	V_{p-p}	2

CHROMA SECTION
(Unless otherwise specified. Gate Pulse and Blanking Pulse of TEST CIRCUIT 2 is Applied)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Maximum Chroma Output	V_{CM}	V_1 =12V, V_5 =10V, V_8: open V_9: 120mV_{p-p} (B:C=1:1) V_G =8V, V_B =15V, measure term. 12	0.5	0.75	1.05	V_{p-p}	3
Burst Output	V_B	The same condition as above	0.45	0.70	0.95	V_{p-p}	3
ACC Characteristics (1)	V_a	V_1 =12V, V_5 =10V, V_8: open V_9 =15mV_{p-p} (B:C=1:1) Measure chroma amplitude term. 12	0.16	0.34	—	V_{p-p}	3
ACC Characteristics (2)	A	V_9 = 100mV_{p-p}, 300mV_{p-p} (B:C = 1:1) Chroma amplitude ratio at term. 12 $A = \frac{V_{12}\,(V_9 = 300mV_{p-p})}{V_{12}\,(V_9 = 100mV_{p-p})}$	—	1.0	1.3	—	3
Color Control Residual Signal	V_{CS}	V_1 = 0V, V_5 = 10V, V_8: open S_1: 1, S_2: 1, V_G = 8V, V_B =15V, V_9 =120mV_{p-p} (B:C=1:1)	—	—	3	mV_{p-p}	3

CHROMA SECTION
(Unless otherwise specified. Gate Pulse and Blanking Pulse of TEST CIRCUIT 2 is Applied)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Uni Color Control Gain Range	ΔV_{cu}	V_1 = 12.0V, V_5 = 5 ~ 10V, V_8: open, S_1: 1, S_2: 1, V_G = 8V, V_B = 15V V_9 = 120mV_{p-p} (B:C = 1:1)	7.5	8.5	9.5	dB	3
Uni Color Control Phase Range	$\Delta\Theta_{cu}$	The same as above. Burst chroma phase change at term. 12	—	4	10	deg	3
HUE Phase Control Range (1)	$\Delta\Theta_{bHI}$	V_1 = 12V, V_5 = 10V, V_8 = 0 ~ 12V, V_9 = 120mV_{p-p}, V_G = 8V, V_B = 15V Burst chroma phase change at term. 12 S_1:1, S_2:1	7.5	105	—	deg	3
HUE Phase Control Range (2)	$\Delta\Theta_{bH2}$	The same as above. Phase change from V_8 open	37	51	62	deg	3
Color Control Phase Change	$\Delta\Theta_{CC}$	V_1 = 0 ~ 12V, V_5: open, V_8: open V_9 = 120mV_{p-p} (B:C = 1:1) V_G = 8V, V_B = 15V, S_1:1, S_2:1	—	3	5	deg	3
Burst-Chroma Phase Difference	$\Delta\Theta_{bc}$	V_1: open The same as above	−8	0	8	deg	
APC Pull-in Range	f_p	V_{14} = 0.6V_{p-p} (Burst) Measure term. 16 frequency Difference between f_c and f_o when APC is out	±250	±350	—	Hz	3
Killer Sensitivity	V_{bk}	V_{14} Burst amplitude when V_1 = 2V S_1:1, S_2:2	18	29	45	mV_{p-p}	3
Residual Carrier of Demodulator Output	V_{car} R V_{car} G V_{car} B	V_{14}: AC GND 3.58MHz component at term. 19, 20 and 21. S_1:1, S_2: 2	—	—	300	mV_{p-p}	3
Color Difference Signal Output	V_{OR}	S_1:1, S_2:2 V_{14}:3.56954MHz, 0.2V_{p-p} CW: 3.579545MHz	1.45	1.85	2.3	V_{p-p}	3
	V_{OG}		0.49	0.62	0.77		
	V_{OB}		1.55	1.95	2.42		
Color Difference Signal Relative Output	R-Y/B-Y	The same as above	0.85	0.95	1.05	—	3
	G-Y/B-Y		0.25	0.31	0.38		
Color Difference Signal Maximum Output	V_{ORM}	S_1:1, S_2:2 V_{14}: 3.56945MHz, 1.2V_{p-p} CW: 3.579545MHz	4.5	5.5	—	V_{p-p}	3
	V_{OGM}		1.4	1.8	—		
	V_{OBM}		4.5	5.5	—		

CHROMA SECTION
(Unless otherwise specified. Gate Pulse and Blanking Pulse of TEST CIRCUIT 2 is Applied)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Relative Phase	Θ_{R-Y}	S_1:, S_2:2, V_{14}: Burst 0.6V_{p-p} Chroma 0.2V_{p-p}	100	107	112	deg	3
	Θ_{G-Y}		230	240	250		
Demodulator Band Width	f_{BR} f_{BG} f_{BB}	S_1:1, S_2:2 V_{14}:10KHz ~ 5MHz, 0.2V_{p-p} −3dB Frequency (0dB; 10KHz)	1.13	1.77	3.16	MHz	3
Blanking Operation Voltage	V_{Q22B}	S_1:1, S_2:2 V_{14}: Burst 0.6V_{p-p}, Chroma 0.2V_{p-p} Blanking pulse height when Demo. output is disappear	10.4	11.1	—	V	3
Demodulator Output DC Voltage	V_{OR} V_{OG} V_{OB}	S_1:1, S_2:2 V_{14}: AC GND	7.00	7.71	8.35	V	1
Demodulator Output Difference Voltage	$V_{O(R-G)}$ $V_{O(R-B)}$ $V_{O(B-G)}$	The same as above	−0.3	—	0.3	V	1
Demodulator DC Output Thermal Co-efficient	$\Delta V_{OR}\theta$ $\Delta V_{OG}\theta$ $\Delta V_{OB}\theta$	The same as above T_a=20°C ~ 65°C	−3	0	2	mV/°C	1
DC Output Voltage Difference Component Thermal Co-efficient	$\Delta V_{O(R-G)}\theta$ $\Delta V_{O(R-B)}\theta$ $\Delta V_{O(B-G)}\theta$	The same as above	−2	0	2	mV/°C	1
Color Control Terminal Voltage	V_i	Measure term. 1 open circuit voltage	5.4	6.0	6.52	V	1
Uni-color Control Terminal Voltage	V_5	Measure term. 5 open circuit voltage	6.9	7.5	8.02	V	1
HUE Control Terminal Voltage	V_8	Measure term. 8 open circuit voltage	5.4	6.0	6.52	V	1

HORIZONTAL SECTION

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Horizontal V_{CC}	V_{33}	V_B=20.3V	7.4	8.2	9.0	V	1
Recommendable Supply Current	I_{33}	—	22	26	30	mA	1
Horizontal Frequency	f_H	S_{39}:b, S_{38}:b, S_{35}: on, V_x=4V	15.069	15.569	16.069	KHz	4
f_H Thermal Drift	Δf_{HT}	The same as above T_a=−20~60°C	−70	80	230	Hz	4
AFC Clamping Voltage	V_{CL}	Measure term. 35 open Circuit Voltage S_1: on	3.71	4.20	4.75	V	1
AFC Input Current	I_{IN35}	S_1: on, S_5:2	2.2	3.62	5.1	mA	1
AFC Output Current	I_{O35}	S_1: on, S_5:1	2.4	3.99	5.6	mA	1
Horizontal Drive Saturation Voltage	V_{OL24}	S_1: on, S_3: on measure V_{24}	—	—	0.3	V	1
Horizontal Drive Output Duty Cycle	T_{O24}	S_{39}:b, S_{38}:b, S_{35}: open V_X=4V. $\frac{\text{H Level Period}}{\text{1 Cycle Period}} \times 100$ Measure V_{24} wave form	45	50	55	%	4
Oscillator Starting Voltage	V_{33} (min)	Minimum V_{33} when output Duty of term. 24 in 50%	—	—	4.0	V	4
Starting Supply Current	I_{33} (min)	V_{33}=4V, Measure I_{33}	5.5	8.8	11.5	mA	4
AFC Pull-in Range	$\Delta f_{H\ PULL}$	S_{38}:a, S_{35}:ON, S_{39}:a Changing V_x, measure Pull-in range	—	±600	—	Hz	4
AFC Hold-in Range	$\Delta f_{H\ HOLD}$	The same as pull-in range. Measure hold-in range.	—	±1000	—	Hz	4
X-ray Protector Voltage Sensitivity	V_{IN23}	Measure V_{23} when V_{24} Output becames L, level. T_a=25°C	0.50	0.88	1.10	V	4
X-ray Protector Current Sensitivity	I_{IN23}	Measure I_{23} when V_{24} Output becames L level. T_a=25°C	0.060	0.178	1.00	μA	4
X-ray Protector Operating Voltage	$V_{IN23\,\theta}$	The same as V_{IN23} T_a=−25~65°C	0.30	0.88	1.28	V	4
X-ray Protector Operating Current	$I_{IN23\,\theta}$	The same as I_{IN23} T_a=−20~65°C	0.03	0.178	2.0	μA	4

SYNC SEPARATOR

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Syncseparator Sensitivity (1)	I_{IN39}	Term. 38: open Measure I_{39} when V_{37} is L→H.	18.1	35.0	11.3	μA	4
Syncseparator Sensitivity (2)	I_{IN38}	Term. 39: open Measure I_{38} same as above	13.3	21.4	54.2	μA	4
Sync Output H Level	V_{OH37}	Term. 38: open	7.04	8.19	9.34	V	4
Sync Output L Level	V_{OL37}		0	1.5	2.4	V	4
Sync Clamp Voltage	V_{CL31}	Measure V_{31} at I_{31} = −1mA	−0.85	−0.63	−0.5	V	4

VERTICAL (Unless otherwise specified, V_{CC} =12V, T_a =25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Vert Freeruning Frequency	f_V	S_{31}: ON, measure term. 28	56	60	64	Hz	4
Retrace Time	T_r	Term. 28 output pulse	500	690	850	μs	4
f_V Pull-in Range	$\Delta f_{V\ PULL}$	S_{31}: ON/OFF, term. 39-VR S_{31}: OFF f_{OSC28} =60Hz S_{31}: ON measure f_{OSC28} $\Delta f_{V\ PULL} = f_{OSC}$ 28-60Hz	11.1	12.1	12.9	Hz	4
Ramp Maximum Voltage	V_{O28}	V_{30} = 6V, measure V_{28}	7.05	7.65	8.25	V	1
Ramp Maximum Current	I_{O28}	V_{30} =6V, measure I_{28}, S_6: ON	16.7	26.8	48.4	mA	1
Maximum Common Mode Input Voltage	V_{IH28}	S_{26}, S_{27}: ON, V_{30} =0V V_{28}: 6-12V, measure V_{28} when V_{27} is saturate.	11.9	—	—	V	4
Minimum Common Mode Input Voltage	V_{IL28}	V_{28}: 6-0V The same as above	—	2.86	3.7	V	4
Terminal 28 Input Current	I_{I28}	S_{26}, S_{27}: ON, V_{30} =0V. Measure I_{28} at V_{28} =6V	0.25	0.98	4.50	μA	4
Terminal 27 Input Current	I_{I27}	The same as above. Measure I_{27} at V_{28} =6V	0.18	0.94	6.21	μA	4
Maximum Vertical Output Voltage	V_{OH26}	S_{26}: OFF, S_{27}: ON, V_{30} =6V Measure V_{26}	5.6	6.3	7.2	V	4
Minimum Vertical Output Voltage	V_{OL26}	S_{26}, S_{27}: OFF, V_{30} =6V Measure V_{26}	—	—	0.3	V	4
Terminal 29 Bias Voltage	V_{29}	Measure V_{29} when I_{29} = − 0.2mA	3.7	3.9	4.1	V	4

TEST CIRCUIT 1 (DC)

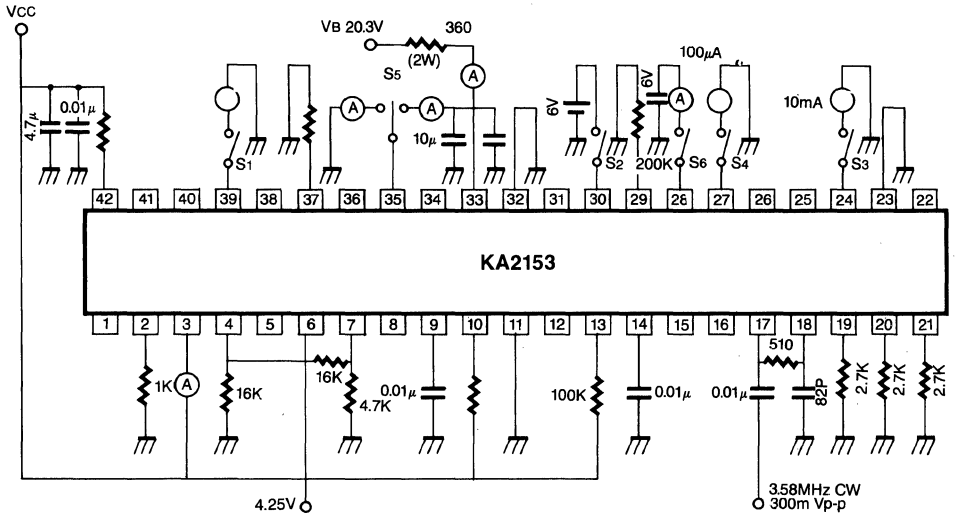


Fig. 2

TEST CIRCUIT 2 (Video)

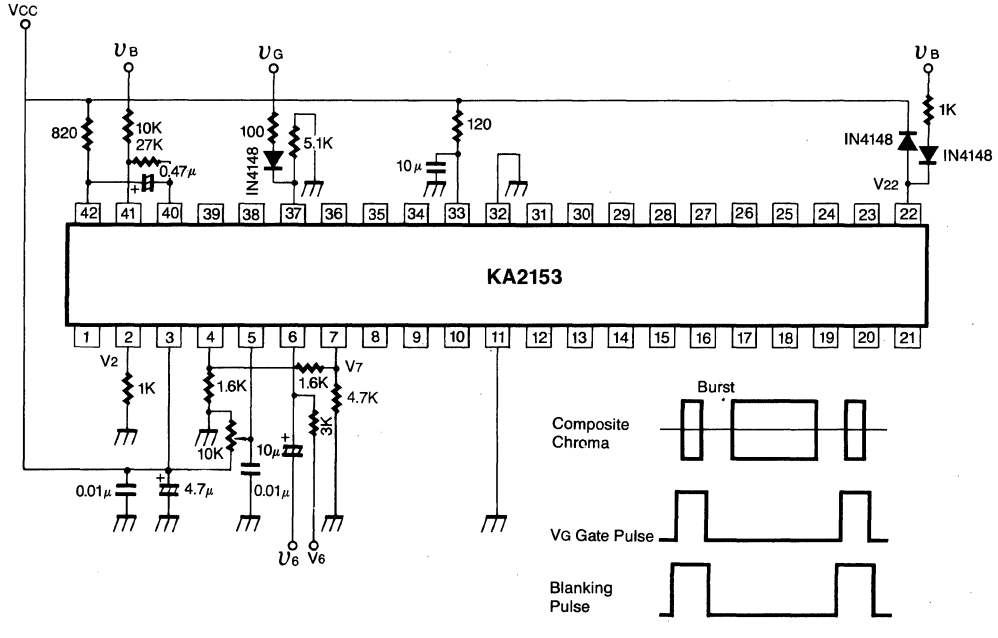


Fig. 3

TEST CIRCUIT 3 (Chroma OSC, Demo)

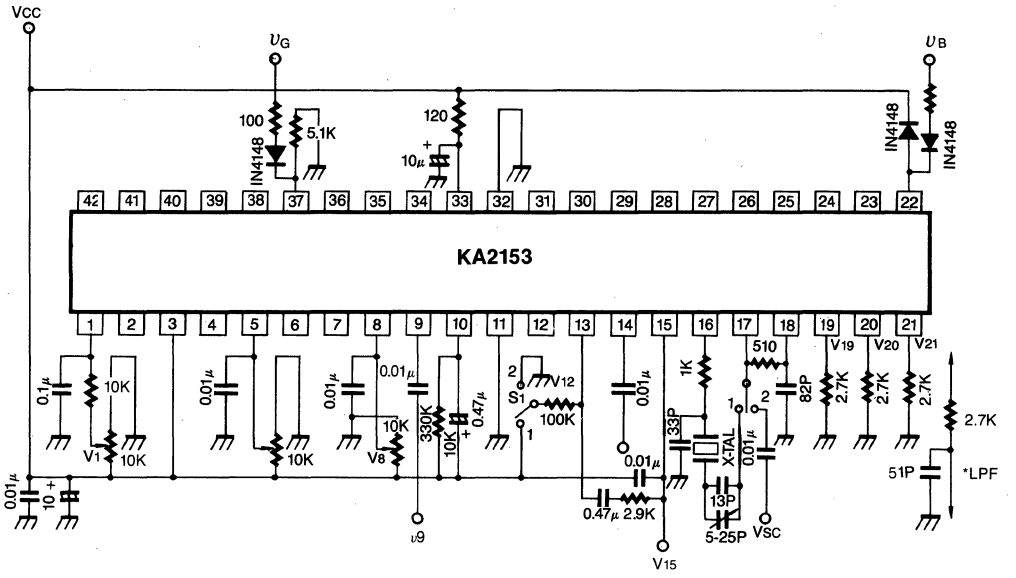
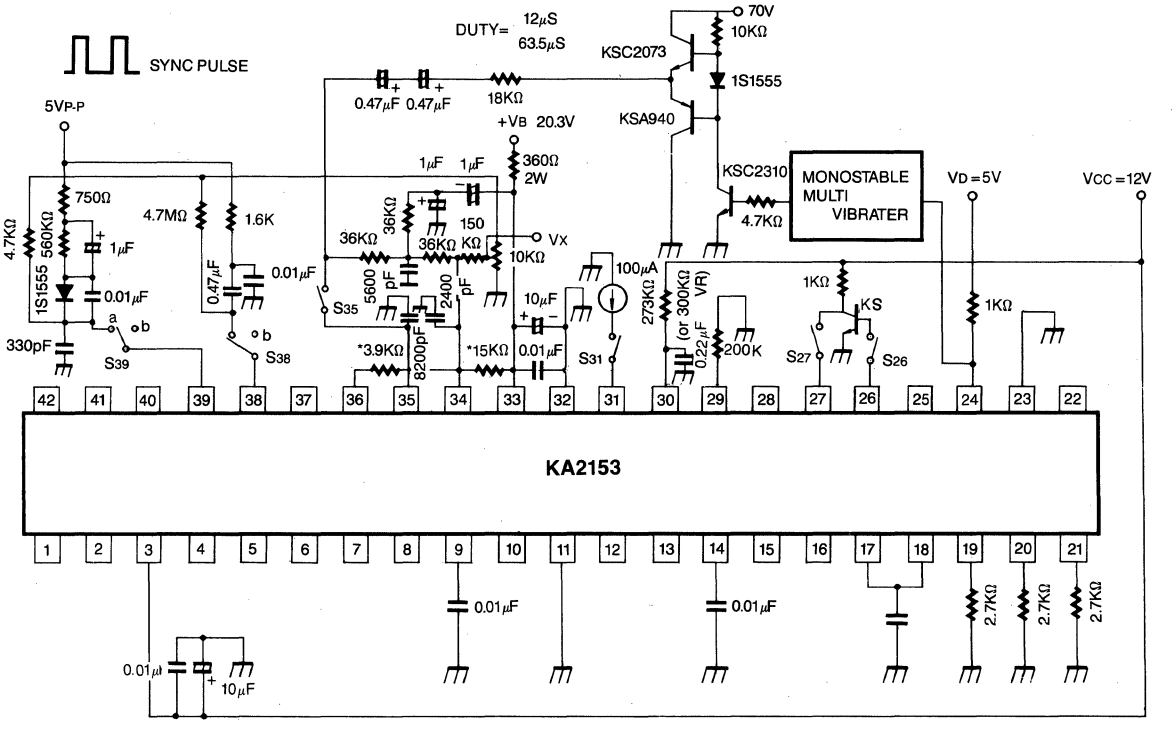
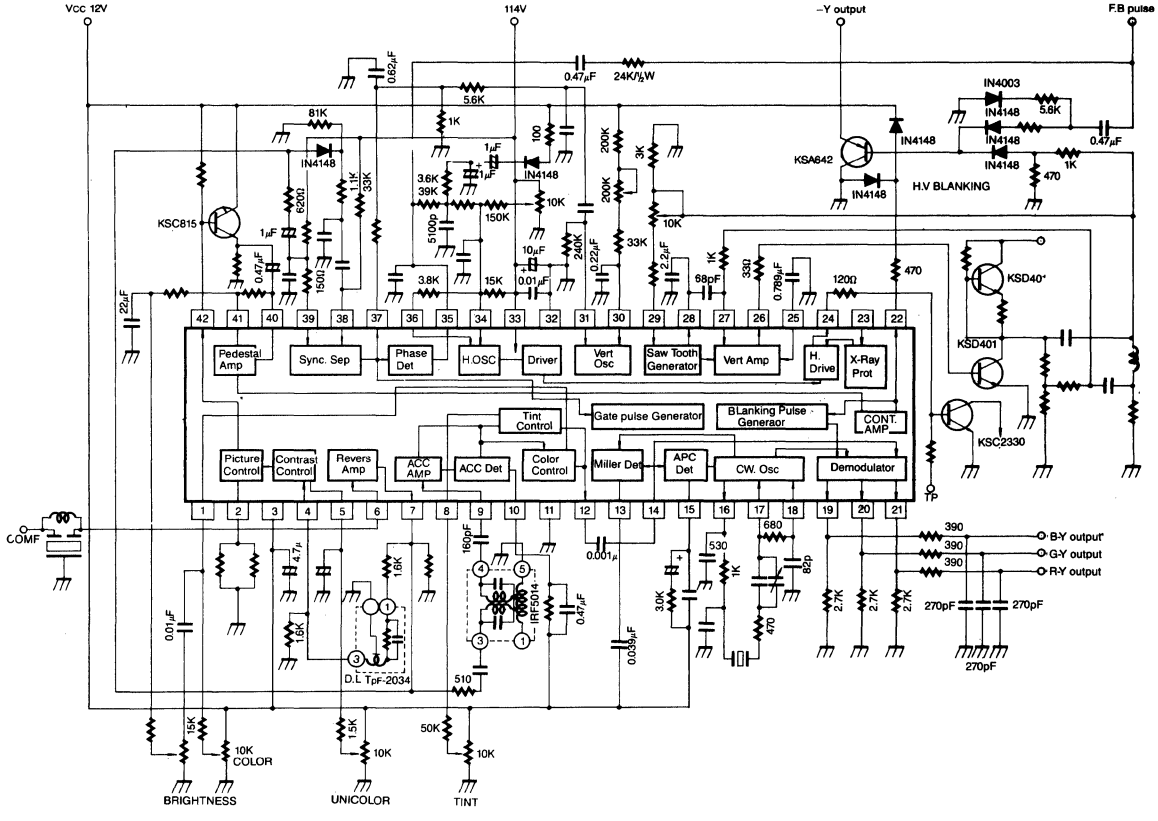


Fig. 4

CIRCUIT 4 (Horizontal, Vertical)



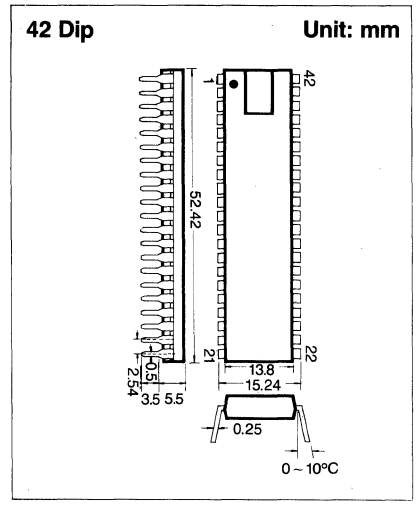
TYPICAL APPLICATION CIRCUIT



VIDEO-CHROMA-DEFLECTION SYSTEM FOR A COLOR TELEVISION (PAL/NTSC)

The KA2154 combines a PAL/NTSC Video-Chroma subsystem and a Deflection combination on a single monolithic integrated circuit to provide a PAL or PAL/NTSC color television.

This device includes a Video amplifier, PAL and NTSC color demodulator these are designed to provide color differential signal outputs, and improved Sync-separator, Horizontal oscillator with saw tooth wave type AFC, Horizontal pre-driver with X-ray protection circuit, Vertical oscillator and Vertical pre-driver in a 42 leads dual-in-line type plastic package.



FUNCTIONS

- Inverter-amplifier
- Contrast control
- Pedestal clamp
- Brightness control
- ACC-amplifier
- Tint control
- Uni-color control
- 3.58MHz VCO
- APC
- Color-Killer
- Color demodulator
- Matrix circuit
- Sync-separator (H.V. sync in)
- $2f_H$ horizontal oscillator
- Flip-flop
- Stabilized horizontal V_{CC} by zener diode
- Horizontal pre driver
- Gate pulse generator
- Vertical sync input
- Vertical oscillator
- Ramp generator

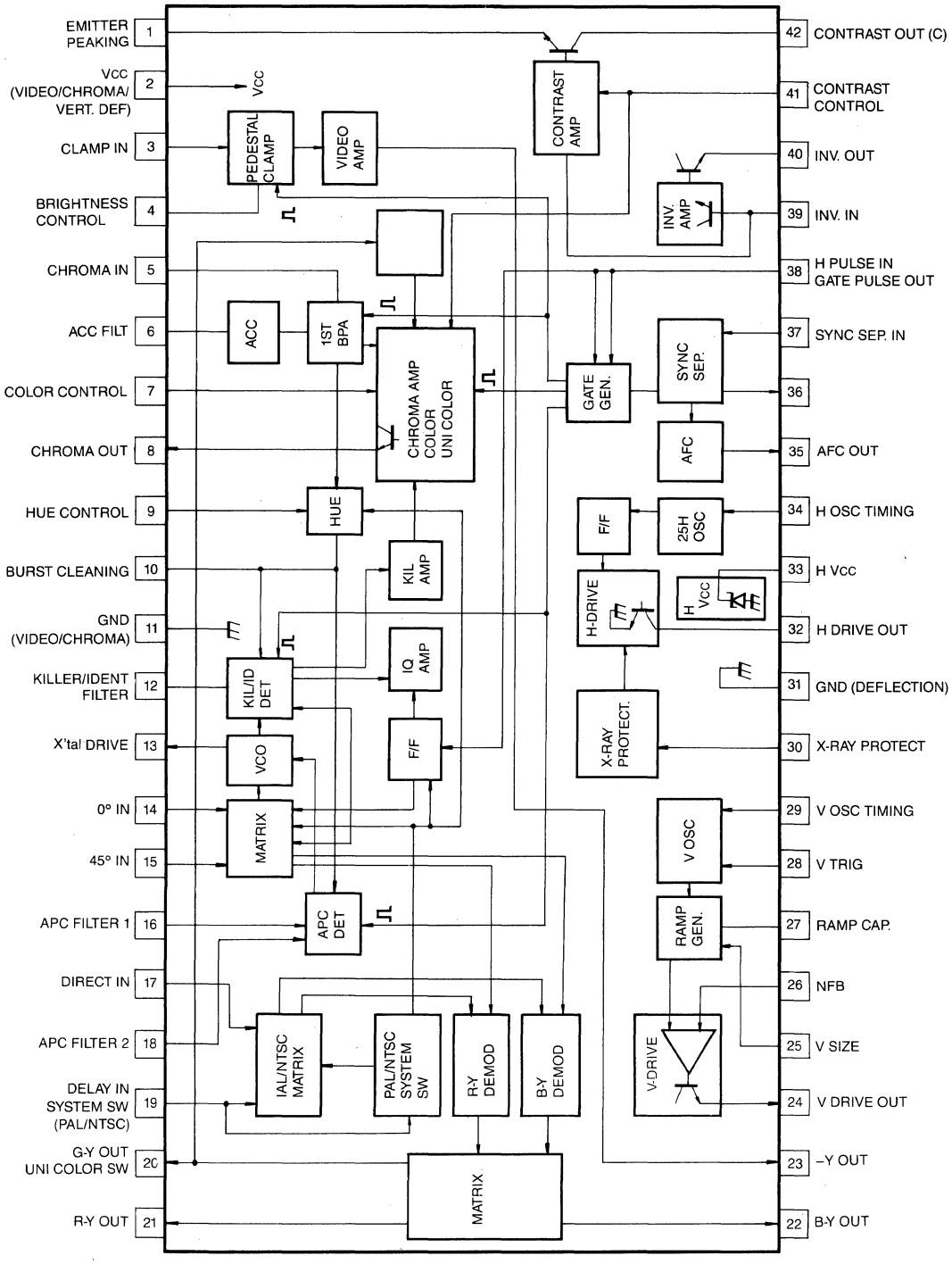
FEATURES

- **Video-Chroma Section**
- **Simple PAL/NTSC System Switch (Demodulator, Flip-flop, tint control for NTSC).**
- **Suitable to a Multi-CTV System: KA2154 PAL/NTSC Dual System Suitable to a Multi-CTV System: KA2154 SECAM Combination 3 or more System.**
- **Minimum Numbers of External Parts Required.**
- **Stabilized with Respect to Variation of Temperature and Supply Voltage.**
- **A Few Initial Adjustment Required.**

DEFLECTION SECTION

- Excellent Temperature Stability of Horizontal Oscillator.
- Exact 50% Duty Cycle Output Due to the $2\text{-}f_H$ Oscillator and Flip-Flop Circuit.
- Excellent Inter-race.

BLOCK DIAGRAM



MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbo	Value	Unit
Supply Voltage	V_{CC} Max	15	V
Horiz. Supply Current	I_{CC} Max	40	mA
Max. Input Signal Level	$IN_{3, 5, 14, 15, 17, 19, 28, 37, 39}$	5	V_{P-P}
Max. Control Terminal Voltage	$V_{4\ MAX}$, $V_{5\ MAX}$, $V_{7\ MAX}$, $V_{9\ MAX}$	V_{CC}	V
Term. 1 Max. Output Current	$I_{1\ MAX}$	4	mA
Term. 8 Max. Output Current	$I_{3\ MAX}$	10	mA
Term. 10 Max. Output Current	$I_{10\ MAX}$	4	mA
Term. 13 Max. Output Current	$I_{13\ MAX}$	4	mA
Min. Load Resistance	R_{LD}	1.8	KΩ
Term. 23 Max. Output Current	$I_{23\ MAX}$	4	mA
Vertical Stage Output Current	$I_{24\ MAX}$	20	mA
Term. 25 Max. Output Current	$I_{25\ MAX}$	4	mA
Term. 26 Max. Input Voltage	$V_{26\ MAX}$	V_{CC}	V
Term. 27 Max. Output Current	$I_{27\ MAX}$	20	mA
Term. 30 Max. Intput Current	$-I_{30\ MAX}$	1	mA
Horiz. Max. Sink Current	$-I_{32\ MAX}$	30	mA
Horiz. Ave. Sink Current	$-I_{32}$	15	mA
Term. 35 Max. Input Voltage	$V_{35\ MAX}$	V_{CC}	V
Term. 36 Max. Voltage	$V_{36\ MAX}$	V_{CC}	V
Term. 38 Max. Intput Voltage	$V_{38\ MAX}$	5	V
Term. 40 Max. Output Current	$I_{40\ MAX}$	5	mA
Term. 42 Max. Sink Current	$-I_{42\ MAX}$	4	mA
Max. Power Dissipation	$P_{D\ MAX}$	2.2	W
Operating Temperature	Topr	−20 ~ 65	°C
Storage Temperature	Tstg	−55 ~ 150	°C

Note: Derated above T_a =25°C in the proportion of 17.6mW/°C.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_Z=12V, T_A=25°C)

Video Section (1)

Characteristic	Symbol	Test Pin	SW 36	SW 41	SW 4A	SW 4B	Test Condition	Specification Min.	Specification Typ.	Specification Max.	Unit	Test CCT
Recommendable Supply Voltage	V_{CC1}							10.8	12	13.2	V	
12V Supply Current	I_{CC1}	2						—	82	—	mA	1
Video Gain	G_V	23 39	Off	On	Off	On	V_C=10V, V_X=4.25V, V_Z=4.0V V_{39}; 500KHz 1V_{P-P} (Multi Burst) G_V=20 log (V_{23}/V_{39})	3	6	8	dB	2
Contrast Gain Control Range	ΔG_V	23	Off	Off	Off	Off	V_O=10V~2V, V_X=4.25V, V_Z=4.0V V_{39}; 500KHz 1V_{PP} (Multi Burst) ΔG_V=20 log ($V_{23\,MAX}/V_{23\,MIN}$)	40 (14)	—	—	dB	2
Video Frequency Characteristics	ΔG_{VF}	23	Off	On	On	On	V_C=10V, V_X=4.25V, V_Z=4.0V V_{39}; 500KHz, 4.0MHz 1V_{P-P} (Multi Burst) ΔG_{VF}=20 log ($V_{23\,4MHz}/V_{23\,500KHz}$	-3.5	-1.5	0.5	dB	2
DC Restoration Ratio	K	23	Off	On	On	On	V_C=10V, V_Z=4.0V V_X; Pedestal #39=3.25V V_{39}; 2.5V_{P-P} 10_{STEP} APL 10%~90% $K=(1-\frac{\Delta V_{23}\ pedestal}{V_{23}\ 100\%\ APL}\times 100$	63	70	77	%	2
Max. Video Output	$V_{23\,MAX}$	23	Off	Off	Off	On	V_X=4.25V, V_{39}; No Signal V_Z=2V~7V 10% to 90% of Variation	5.0	7.5	—	V_{P-P}	2
Video DC Output Term. Co-effici.	V_{23}/DT	23	Off	Off	Off	On	V_X=4.25V, V_Z=4.0V V_{39}; No Signal T_a=-20°C~65°C	-2.5	0	2.5	mV/°C	2
Inverter Amp. Gain	G_R	40	Off	Off	Off	Off	V_X=4.25V V_{39}; 500KHz, 1V_{P-P} G_R=20 log (V_{40}/V_{39})	2.2	3.5	4.6	dB	2
Inverter Amp. Differential	DG_R	40	Off	Off	Off	Off	V_X; 3.3~5.3V V_{39}; 3.58 MHz 100mV_{P-P} $DG_R=(V_{40\,MAX}/V_{40\,MIN}-1)\times 100$		2.5	10	%	2
Inverter Amp. Differential Phase	DP_R	40	Off	Off	Off	Off	V_X; 3.3~5.3V V_{39}; 3.58MHz, 100mV_{P-P} $DP_R=\phi_{40\,MAX}-\phi_{40\,MIN}$		3	5	deg	2

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_Z = 12V, T_A = 25°C)

Video Section (2)

Characteristic	Symbol	Test Pin	SW 36	SW 41	SW 4A	SW 4B	Test Condition	Specification Min.	Specification Typ.	Specification Max.	Unit	Test CCT
Inverter Amp. Frequency Characteristics	ΔG_{RF}	40	Off	Off	Off	Off	V_X = 4.25V V_{39} = 500KHz, 4MHz $1V_{P-P}$ ΔG_{RF} = 20 log ($V_{40\ 4MHz}/V_{40\ 500KHz}$)	– 3.5	– 0.1	0.5	dB	2
Inverter Amp. 3.58 MHz Linearity	V_{L39}	39 40	Off	Off	Off	Off	V_X = 4.25V Measure #39 input level at #40 maximum output.	1.6	—	—	V_{P-P}	2
Contrast Control Open Voltage	V_{41}	41	—	—	—	—		6.7	7.2	7.7	V	1
Color Control Open Voltage	V_7	7	—	—	—	—		5.5	6.0	6.5	V	1
Tint Control Open Voltage	V_9	9	—	—	—	—		5.5	6.0	6.5	V	1
Pedestral Amp. Gain	G_P	3 23	Off	On	On	On	V_X = 4.25V, V_Z = 4V V_{39} = 50KHz $1V_{P-P}$ (Multi Burst) G_P = 20 log (V_{23}/V_3)	11	12.6 (9.5)	14	dB	

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_C=10V, V_S=10V, SW_{36}; On SW_{10}; Off SW_{4A}; On SN_{4B}; On)

Chroma (1) PAL

Characteristic	Symbol	Test Pin	SN 41	SN 7	SN 9	SN 12	SW 15	SW 20	Test Condition	Specification Min.	Specification Typ.	Specification Max.	Unit	Test CCT
Max. Chroma Output Voltage	ϱ_{CUP}	8	On	On	Off	a	b	On	V_5: 120mV$_{P-P}$ (B:C=1:1)	0.5	0.75	1.05	V_{P-P}	3
Burst Output Voltage	ϱ_{bP}	10	On	On	Off	a	b	On	V_5: 120mV$_{P-P}$ (B:C=1:1)	0.45	0.70	0.95	V_{P-P}	3
ACC Characteristics (1)	ϱ_{aP}	8	On	On	Off	a	b	On	V_5: 15mV$_{P-P}$ (B:C = 1:1)	0.2	0.43	—	V_{P-P}	3
ACC Characteristics (2)	A_P	8	On	On	Off	a	b	On	V_5: 100mV$_{P-P}$, 300mV$_{P-P}$ (B:C=1:1) $A_P = \frac{V_8\ V_5=300mV_{P-P})}{V_8\ (V_5=100mV_{P-P})}$	—	1.0	1.3		3
Chroma Input Dynamic Range	ϱ_{CIP}	8	On	On	Off	a	b	On	V_5=100mV$_{P-P}$→800mV$_{P-P}$	500	600	—	mV$_{P-P}$	3
Uni Color Control Range (1) Uni Color Switch On	ΔC_{CU1P}	8	On	On	Off	a	b	On	V_C=4~10V, V_S=10V V_5=120mV$_{P-P}$ (B:C=1:1) $\Delta\varrho CU_P = 20 \log \frac{V_8\ (V_C=10V)}{V_8\ (V_C=4V)}$	40	—	—	dB	3
Uni Color Control Range (Ω) (Switch Off)	$\Delta\varrho_{CU2P}$	8	On	On	Off	a	b	Off	Same as above	—	0	—	dB	3
Uni Color Control Phase Sift	$\Delta\theta_{UP}$	8	On	On	Off	a	b	On	V_C=4V~10V, V_S=10V V_5=120mV$_{P-P}$ (B:C=1:1)	—	—	5	deg	3
Residual Color	ϱ_{CKP}	8	On	On	Off	a	b	On	V_C=10V, V_S=5V V_5=120mV$_{P-P}$ (B:C=1:1)	—	—	3	mV$_{P-P}$	3

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_C =10V, V_S =10V, SW_{36}; On SW_{10}; Off SW_{4A}; On SN_{4B}; On)

Chroma (2) PAL

Characteristic	Symbol	Test Pin	SN 41	SN 7	SN 9	SN 12	SW 15	SW 20	Test Condition	Specification Min.	Specification Typ.	Specification Max.	Unit	Test CCT
Color Control Phase Sift	$\Delta\theta_{ccp}$	8	On	On	Off	a	b	On	V_C=10V, V_S=2~10V V_5=120mV$_{P-P}$ (B:C=1:1)	—	3	—	deg	8
Burst-Chroma Phase Difference	$\Delta\theta_{bcp}$	8 10	On	On	Off	a	b	On		45	60	75	deg	3
Tint control Range	$\Delta\theta bH1_P$	10	On	On	On	a	b	On		—	0	—	deg	3
Tint Control Phase Distribution	$\Delta\theta bH2_P$	10	On	On	On	a	b	On		—	0	—	deg	3
Killer Det. Sensitivity	ϱ_{KP}	8 10	Off	On	Off	a	a	On		30	60	110	mV$_{P-P}$	3
Ident Det. Sensitivity	ϱ_{IP}	21 10	Off	On	Off	a	a	On		30	60	110	mV$_{P-P}$	3
APC Pull-in Range	f_{PP}	13	Off	Off	Off	a	a	On		±300	±500	—	Hz	3
Phase Det. Sensitivity	μ_P	16 18	Off	Off	Off	a	c	On		—	25	—	mV/deg	3
Control Sensitivity	β_P	13 16 18	Off	Off	Off	a	a	On		—	2.2	—	Hz/deg	3

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_C = 10V, V_S = 10V, SW_{36}; On SW_{10}; Off SW_{4A}; On SN_{4B}; On)

Chroma (3) PAL

Characteristic	Symbol	Test Pin	SN 41	SN 7	SN 9	SN 12	SW 15	SW 20	Test Condition	Specification Min.	Specification Typ.	Specification Max.	Unit	Test CCT
Color Differential Output Voltage	ϱCR_P ϱO_G ϱOB_P	21 20 22	On	On	Off	a	a	On	V_{17}, V_{19}; 100-V_{P-P} 4.443618 MHz CN: 4.033618MHz	1.34 — 2.3	1.7 — 3.0	2.1 — 3.8	V_{P-P}	3
Max. Color Differential Output Voltage	ϱCRM_P ϱCGM_P ϱCBM_P	21 20 22	On	On	Off	a	a	On	V_{17}, V19; 500mV_{P-P} 4.43618 MHz CN: 4,433618 MHz	3.8 — 3.8	5.5 — 5.5	— — —	V_{P-P}	3
Relative Amplitude	R-Y/B-Y_P G-Y/B-Y_P	21/22 20/22	On	On	Off	a	a	On	V_{17}: 200mV_{P-P} 4,443618 MHz CW: 4.433618 MHz	0.46 0.24	0.56 0.34	0.66 0.44	—	3
Relative Phase	θR-Y_P ϱG-Y_P	21/22 20/22	On	On	Off	a	a	On		80 220	90 230	100 240	deg	3
Residual Carrier	ϱ_{RC} R_P ϱ_{RC} G_P ϱ_{RC} B_P	21 20 22	On	On	Off	a	a	On		—	—	300	mV_{P-P}	3
Demodulator Bandwidth	fBR_P fBG_P fBB_P	21 20 22	On	On	Off	a	a	On	V_{17}: 200mV_{P-P} 10KHz ~ 5MHz	1.1	2.1	3.2	MHz	3
Demo. Output DC Voltage	ECR_P EOG_P ECB_P	21 20 22	Off	Off	Off	a	b	On		6.8	7.4	8.0	V	1
Demo. Output DC Voltage Difference	$E_{O\ (R-G)P}$ $E_{O\ (R-B)P}$ $E_{O\ (B-G)P}$	21 20 22	Off	Off	Off	a	b	On	V_{17}, V_{19}	−0.3	0	0.3	V	1
Demo. Output DC Voltage Therm. Co-effic	ΔEOR_{9P} ΔEOR_{9P} ΔEOB_9	21 20 22	Off	Off	Off	a	b	On	T_a = −20°C ~ +65°C	−3	0	2	mV/°C	1
Demo. Output Diffence Voltage Therm. Co-effic.	$\Delta E_{O\ (R-G)9P}$ $\Delta E_{O\ (R-B)9P}$ $\Delta E_{O\ (B-G)9P}$	21 20 22	Off	Off	Off	a	b	On	T_a = −20°C ~ +65°C	−2	0	2	mV/°C	1
System SW Threshold	V_{THS}	19	Off	Off	Off	a	b	On	V_{17}: 200mV_{P-P} 4.443618 MHz CN: 4.433618 MHz	2.4	3	3.6	V	3
DC Change by System SW	ΔE_{OR} ΔE_{OG} ΔE_{OB}	21 20 22	Off	Off	Off	a	b	On	V_{IN}: 220mV_{P-P} 4.43618 MHz	−100	0	100	mV	3

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_C =10V, V_S =10V, SW_{36}; On SW_{10}; Off SW_{4A}; On SW_{4B}; On)

Chroma (4) NTSC

Characteristic	Symbol	Test Pin	SN 41	SN 7	SN 9	SN 12	SW 15	SW 20	Test Condition	Specification Min.	Specification Typ.	Specification Max.	Unit	Test CCT
Max. Chroma Output Voltage	ϱCM_N	8	On	On	Off	a	b	On	V_5: 120mV$_{P-P}$ (B:C=1:1)	0.5	0.75	1.05	V_{P-P}	4
Burst Output Voltage	ϱB_N	10	On	On	Off	a	b	On	V_5: 120mV$_{P-P}$ (B:C=1:1)	0.45	0.70	0.95	V_{P-P}	4
ACC Characteristics (1)	ϱa_N	8	On	On	Off	a	b	On	V_5: 15mV$_{P-P}$ (B:C=1:1)	0.2	0.43	—	V_{P-P}	4
Acc Characteristics (2)	A_N	8	On	On	Off	a	b	On	V_5: 100mV$_{P-P}$, 300mV$_{P-P}$ (B:C=1:1) $A_P = \frac{V_8\ (V_5=300mV_{P-P})}{V_8\ (V_5=100mV_{P-P})}$	—	1.0	1.3		4
Chroma Input Dynamic Range	ϱCI_N	8	On	On	Off	a	b	On	V_5=100mV$_{P-P}$→800mV$_{P-P}$	500	600	—	mV$_{P-P}$	4
Uni Color Control Range (1) Uni Color SW On	$\Delta CCU1_N$	8	On	On	Off	a	b	On	V_C=4~10V, V_S=10V V_5=120mV$_{P-P}$ (B:C=1:1) $\Delta\varrho CU_P = 20\log\frac{V_5\ (V_C=10V)}{V_8\ (V_C=4V)}$	40	—	—	dB	4
Uni Color Control Range (2) (SW. Off)	$\Delta\varrho CU2_N$	8	On	On	Off	a	b	Off		—	0	—	dB	4
Uni Color Control Phase Shift	$\Delta\theta U_N$	8	On	On	Off	a	b	On	V_C=4V~10V, V_C=10V V_5=120mV$_{P-P}$ (B:C=1:1)	—	—	5	deg	4
Residual Color	ϱCK_N	3	On	On	Off	a	b	On	V_C=0V, V_S=0V V_5=120mV$_{P-P}$ (B:C=1:1)	—	—	3	mV$_{P-P}$	4

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_C =10V, V_S =10V, SW_{36}; On SW_{10}; Off SW_{4A}; On SW_{4B}; On)

Chroma (5) NTSC

Characteristic	Symbol	Test Pin	SN 41	SN 7	SN 9	SN 12	SW 15	SW 20	Test Condition	Specification Min.	Specification Typ.	Specification Max.	Unit	Test CCT
Color Control Phase Shift	$\Delta\theta CC_N$	8	On	On	Off	a	b	On	V_C=10V, V_S=2~10V V_5=120mV$_{P\text{-}P}$ (B:C=1:1)	—	3	—	deg	4
Burst-Chroma Phase Difference	$\Delta\theta bC_N$	8 10	On	On	Off	a	b	On		45	60	75	deg	4
Tint Control Range	$\Delta\theta bH1_4$	10	On	On	On	a	b	On	V_C=10V, V_T=2~10V V_5=120mV$_{P\text{-}P}$ (B:C=1:1)	75	95	110	deg	4
Tint Control Phase Distribution	$\Delta\theta bH2_N$	10	On	On	On	a	b	On	V_C=10V V_5=120mV$_{P\text{-}P}$ (B:C=1:1) V_7	37	47	62	deg	4
Killer Det Sensitivity	ϱK_N	8 10	Off	On	Off	a	a	On		15	30	75	mV$_{P\text{-}P}$	4
APC Pull-in Range	fP_N	13	Off	Off	Off	a	a	On		±300	±500	—	Hz	4
Phase Det. Sensitivity	μ_N	16 18	Off	Off	Off	a	c	On		—	25	—	mV/deg	4
Control Sensitivity	β_N	13 16 18	Off	Off	Off	a	a	On		—	2.2	—	Hz/mV	4

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_C=10V, V_S=10V, SW_{36}; On SW_{10}; Off SW_{4A}; On SW_{4B}; On)

Chroma (6) NTSC

Characteristic	Symbol	Test Pin	SN 41	SN 7	SN 9	SN 12	SW 15	SW 20	Test Condition	Specification Min.	Specification Typ.	Specification Max.	Unit	Test CCT
Color Control Output Voltage	Q_{OR_N} Q_{OG_N} Q_{OB_N}	21 20 22	On	On	Off	a	a	On	V_{17}: 100mV$_{P-P}$ 4.443618 MHz C_N: 4.433618 MHz	2.3 0.85 2.3	3.0 1.1 3.0	3.75 1.37 3.75	V_{P-P}	4
Max. Color Differential Output Voltage	Q_{CRM_N} Q_{CGM_N} Q_{CBM_N}	21 20 22	On	On	Off	a	a	On	V_{17}: 500mV$_{P-P}$ 4.443618 MHz C_N: 4.433618 MHz	4.5 1.4 4.5	5.5 1.8 5.5	— — —	V_{P-P}	4
Relative Amplitude	R-Y/B-Y$_N$ G-Y/B-Y$_N$	21/22 20/22	On	On	Off	a	a	On	V_{17}: 100mV$_{P-P}$ 4.443618 MHz CN: 4.433618 MHz	0.9 2.28	1.00 0.38	1.1 0.48	—	4
Relative Phase	S_{R-Y_N} S_{G-Y_N}	21/22 20/22	On	On	Off	a	a	On		— —	105 235	— —	deg	
Residual Carrier	Q_{rcR_N} Q_{rcG_N} Q_{rcB_N}	21 20 22	On	On	Off	a	a	On		—	—	300	mV$_{P-P}$	4
Demodurator Bandwidth	f_{BR_N} f_{BG_N} f_{BB_N}	21 20 22	On	On	Off	a	a	On	V_{17}: 100mV$_{P-P}$ 10KHz ~ 5MHz	1.1	2.1	3.2	MHz	4
Demo. Output DC Voltage	E_{OR_N} E_{OG_N} E_{OB_N}	21 20 22	Off	Off	Off	a	b	On	V_{17}:	6.8	7.4	8.0	V	1
Demo. Output DC Voltage Difference	$E_{O\ (R-G)_N}$ $E_{O\ (G-B)_N}$ $E_{O\ (B-G)_N}$	21 20 22	Off	Off	Off	a	b	On	V_{17}:	−0.3	0	0.3	V	
Demo. Output DC Voltage Therm. Co. effi.	$\Delta E_{OR_{9N}}$ $\Delta E_{OG_{9N}}$ $\Delta E_{OB_{9N}}$	21 20 22	Off	Off	Off	a	b	On	T_a = −20 ~ +65°C	−3	0	2	mV/°C	1
Demo. Output Diff. Voltage Therm. Co. effi.	$\Delta E_{O\ (R-G)_{9N}}$ $\Delta E_{O\ (R-B)_{9N}}$ $\Delta E_{O\ (B-G)_{9N}}$	21 20 22	Off	Off	Off	a	b	On	T_a = −20 ~ +65°C	−2	0	2	mV/°C	1

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, SW_{24}; SW_{27}, SW_{28}; Off SW_{29}; a)

Horizontal Section (1)

Characteristic	Symbol	Test Pin	SW 34	SW 35	SW 36	SW 37	SW 32	Test Condition	Specification Min.	Specification Typ.	Specification Max.	Unit	Test CCT
Horizontal Regulated Voltage	V_{33}	33	—	—	—	—			7.4	8.2	9.0	V	1
Recommendable Supply Current	I_{33}	33							22	26	30	mA	5
Horizontal Free Running Frequency	f_H	34	Off	Off	Off	b	2	V_H=4V	15.125	15.625	16.125	kHz	5
f_H Thermal Drift	Δf_{HT}	34	Off	Off	Off	b	a	V_H=4V T_a=−20°C ~ +60°C	−90	70	230	Hz	5
AFC Clamping Voltage	V_{CL}	35	—	—	—	—	a	SW_1: 1 SW_2: 1	6.0	6.6	7.2	V	1
AFC Sink Current	I_{IN35}	35	—	—	—	—	a	SW_1: 1 SW_2: b	2.7	3.7	5.0	mA	1
AFC Source Current	I_{O35}	35	—	—	—	—	a	SW_1: b SW_2: c	2.7	4.0	5.0	mA	1
Horiz. Drive Residual Voltage	V_{OL32}	32	Off	Off	Off	b	a	V_H=4V Saturation Voltage of #32	—	—	0.3	V	5
Horiz. Output Pulse Duty	T_{O32}	32	Off	Off	Off	b	a	V_H=4V T_{C32}=Duty cycle of H period.	45	50	55	%	5
Horiz. Osc. Starting Voltage	$V_{33START}$	33	Off	Off	Off	b	a	V_B: Variable Measure min V_B which provides Δ50% duty Output to #32	—	—	6.0	V	5
4V Supply Current	$I_{33START}$	33	Off	Off	Off	b	a	V_B=4V Measure I_{33}	4.6	6.7	8.8	MA	5
AFC Pull-in Range	Δf_{HPULL}	32 37	On	On	Off	a b	a	V_H: Variable Observe #32 and #37 wave form. S_{37} a→b, Measure the frequency difference.	—	±900	—	Hz	5
AFC Hold Range	Δf_{HHOLD}	32 37	On	On	Off	a b	a	Same as above	—	±1800	–	Hz	5

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, SW_{24}; SW_{27}, SW_{28}; Off SW_{29}; a)

Horizontal Section (2)

Characteristic	Symbol	Test Pin	SW 34	SW 35	SW 36	SW 37	SW 32	Test Condition	Specification Min.	Specification Typ.	Specification Max.	Unit	Test CCT
AFC Voltage Sensitivity	β_H	32	Off	Off	Off	b	a	V_A=4.5V, Set V_H so that f_H will be 15.75 KHz. Then, change V_A 4V+0.5V, Measure f_H difference.	—	1900	—	Hz/V	5
X-ray protector Voltage Sensitivity	V_{IN30}	30	Off	Off	Off	b	a	Apply variable DC voltage to #30 (V_{30}). Measure V_{30} and I_{30} when #32 output disappears.	0.7	0.88	1.1	V	5
X-ray protector Current Sensitivity	I_{IN30}	30	Off	Off	Off	b	a		0.05	0.18	1.0	μA	5
H. Drive Output Excess Voltage Protector Current Sens.	I_{IN32}	32	Off	Off	Off	b	b	Apply variable DC voltage to #32 through 1KΩ resistor. Measure V_{32} and I_{32} just before V_{32} goes down.	0.05	0.18	1.0	μA	5
Excess Voltage Protector Voltage Sens.	V_{IN32}	32	Off	Off	Off	b	b		7.1	8.6	9.5	V	5

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, SW_{24}; SW_{27}, SW_{28}; Off SW_{29}; a)

Vertical Section

Characteristic	Symbol	Test Pin	SW 36	SW 41	SW 4A	SW 4B	Test Condition	Specification Min.	Specification Typ.	Specification Max.	Unit	Test CCT
Vertical Frequency	f_V	27	Off	Off	Off	c		47	50	54.1	Hz	5
Retrace Time	T_R	27	Off	Off	Off	c	H period of #27 output pulse	450	690	850	μsec	5
f_V Pull-in Range	$\Delta f_{V\,PULL}$	27	Off	Off	On / Off	b	Set f_V to 50Hz at SW_{28} Off; $f_{OSC\,28}$ Measure f_V at SW_{28} On; $f_{OSC'\,28}$ $\Delta f_{V\,PULL} = f_{OSC28} - f_{OSC'28}$	9.0	10.0	11.0	Hz	5
Term. 27 Max. Output Voltage	V_{O27}	27	—	—	—	—	SW_{29}; On SW_4; Off	7.7	8.5	9.2	V	1
Term. 27 Max. Output Current	I_{O27}	27	—	—	—	—	SW_{29}; On SN_4; On	15	27	50	mA	1
Max. Common Mode Input Voltage	V_{IH26}	26	On	On	Off	a	$V_{27} = 6 \rightarrow 12V$	11.9	—	—	V	5
Min. Common Mode Output Voltage	V_{IL26}	26	On	On	Off	a	$V_{27} = 6 \rightarrow 0V$	—	2.8	3.7	V	5
Term. 27 Input Current	I_{I27}	27	On	On	Off	a	$V_{27} = 6V$	0.25	1.0	4.5	μA	5
Term. 26 Input Current	I_{I26}	26	On	On	Off	a	$V_{27} = 6V$	0.18	1.0	6.3	μA	5
Max. Drive Output Voltage	V_{OH24}	24	Off	On	Off	d		7.3	8.0	8.7	V	5
Min. Drive Output Voltage	V_{OL24}	24	Off	Off	Off	d		—	—	0.3	V	5
Term. 25 Bias Voltage	V_{25}	25	—	—	—	—	$I_{25} = -0.2mA$	3.7	3.9	4.1	V	5
f_V Thermal Drift	Δf_{VT}	27	Off	Off	Off	c	$T_a = -20°C \sim +60°C$	−1.0	—	2.0	Hz	5

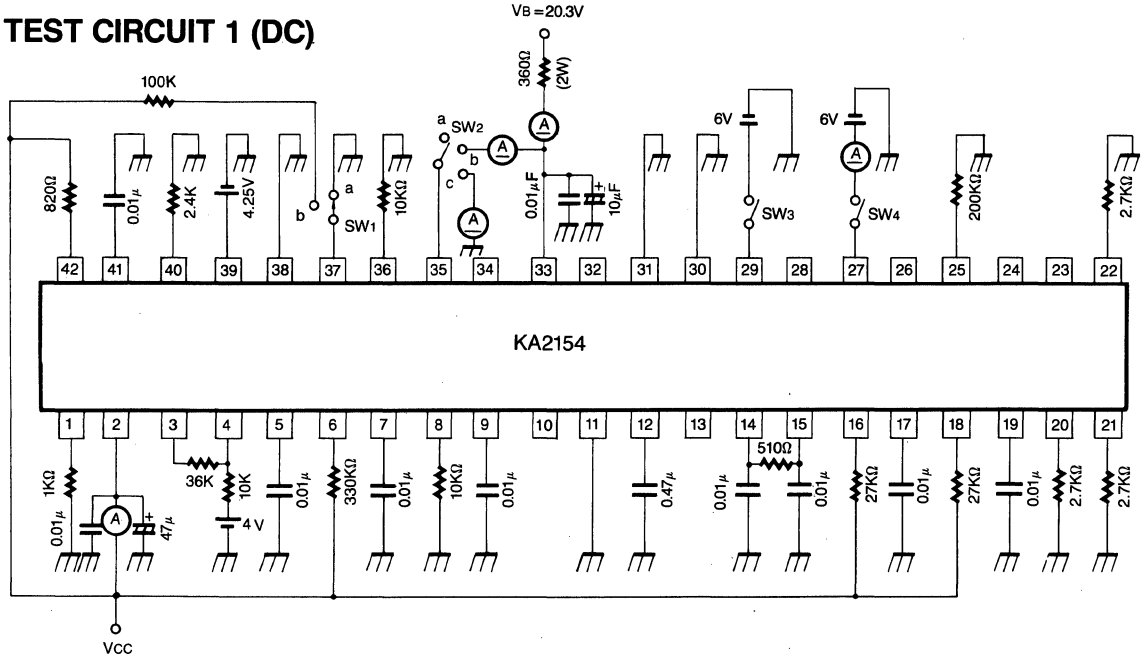
ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, SW_{24}; SW_{27}, SW_{28}; Off SW_{29}; a)

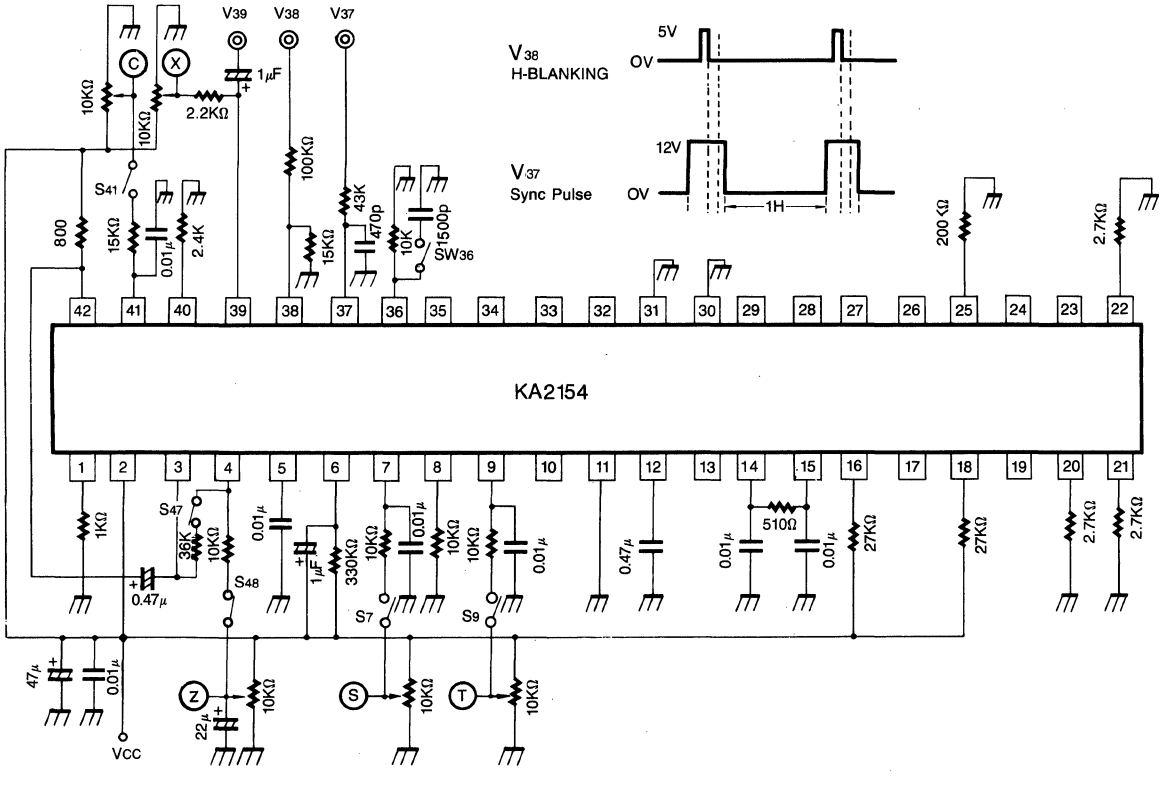
SYNC. Separator

Characteristic	Symbol	Test Pin	SW 36	SW 41	SW 4A	SW 4B	Test Condition	Specification Min.	Specification Typ.	Specification Max.	Unit	Test CCT
Sync. Separator Current Sensitivity	I_{IN37}	36 37	Off	Off	Off	c	Measure #37 input current when V_{36} goes L level to H.	18	35	113	μA	5
Sync. Output H Level	V_{OH36}	36	Off	Off	Off	c	V_S=2V Measure V_{36}	7.0	8.2	9.4	V	5
Sync. Outpout L Level	V_{OL36}	36	Off	Off	Off	b	Measure V_{36}	0	0.2	1.0	V	5
Gate Pulse H Level	V_{OH38}	38	Off	Off	Off	b	V_D=12V, V_{36}=5V Measure V_{38}	4.3	5	5.7	V	5
Gate Pulse L Level	V_{OL38}	38	Off	Off	Off	b	V_O=12V Measure V_{32}	—	1.6	—	V	5
H Pulse Threshold	V_{38ON}	38	Off	Off	Off	b	V_D: Variable 0→2V Measure V_D when V_{38} goes H to L.	0.7	1	1.5	V	5

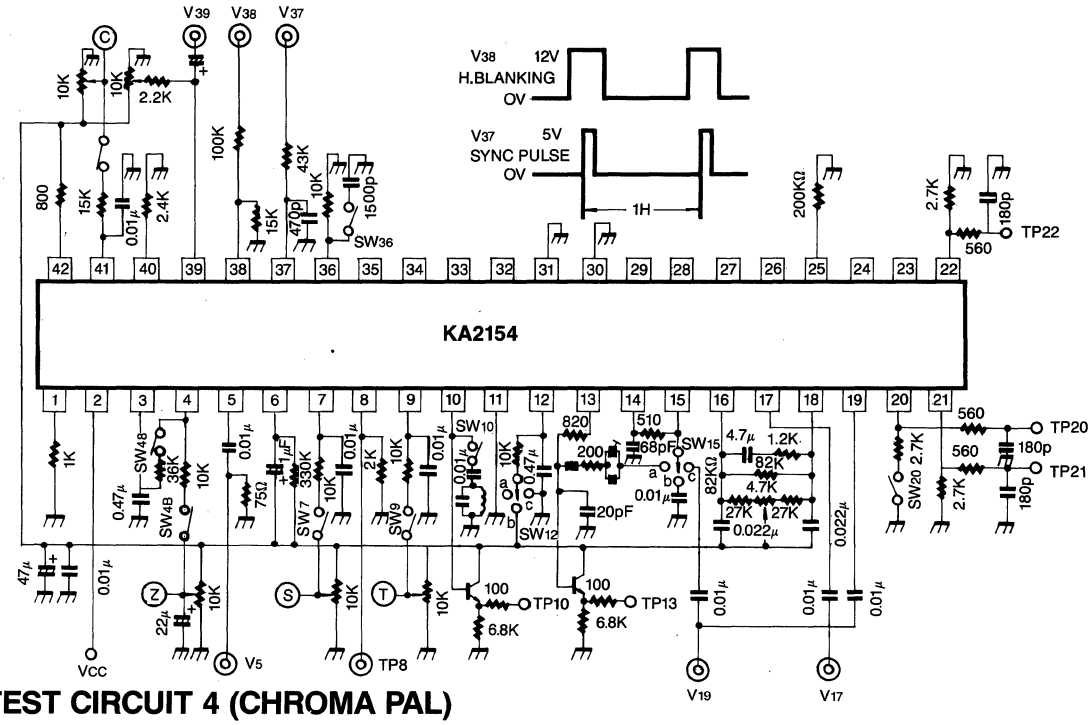
TEST CIRCUIT 1 (DC)



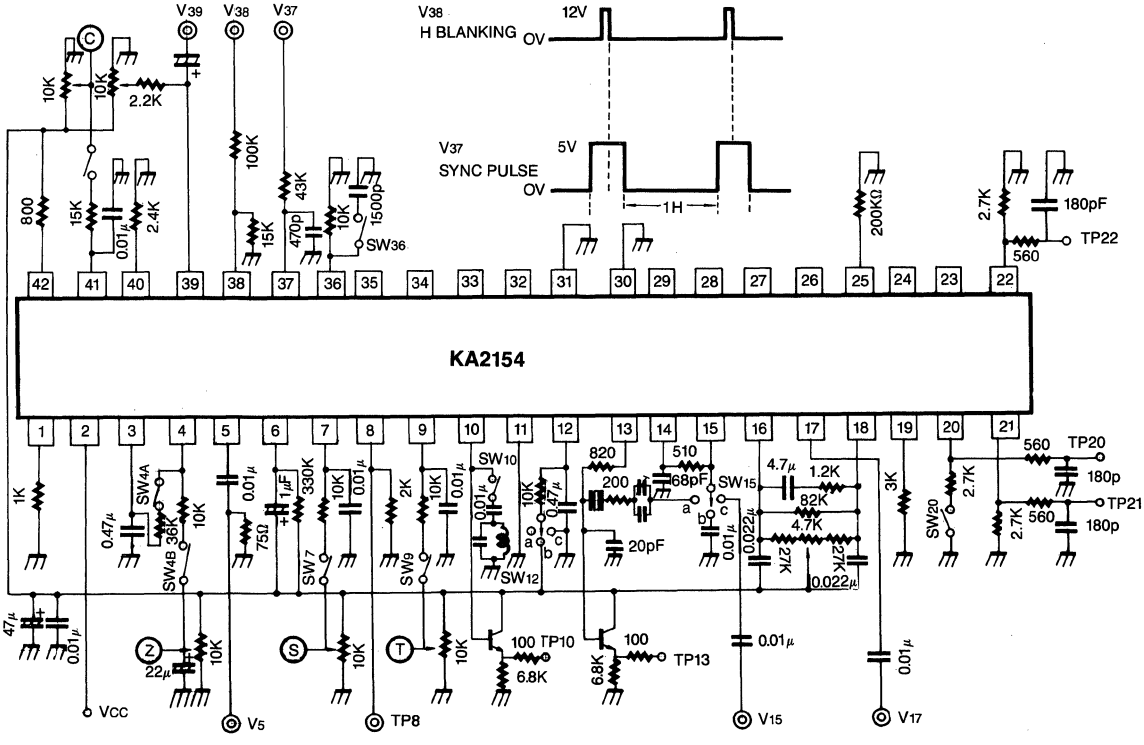
TEST CIRCUIT 2 (VIDEO)



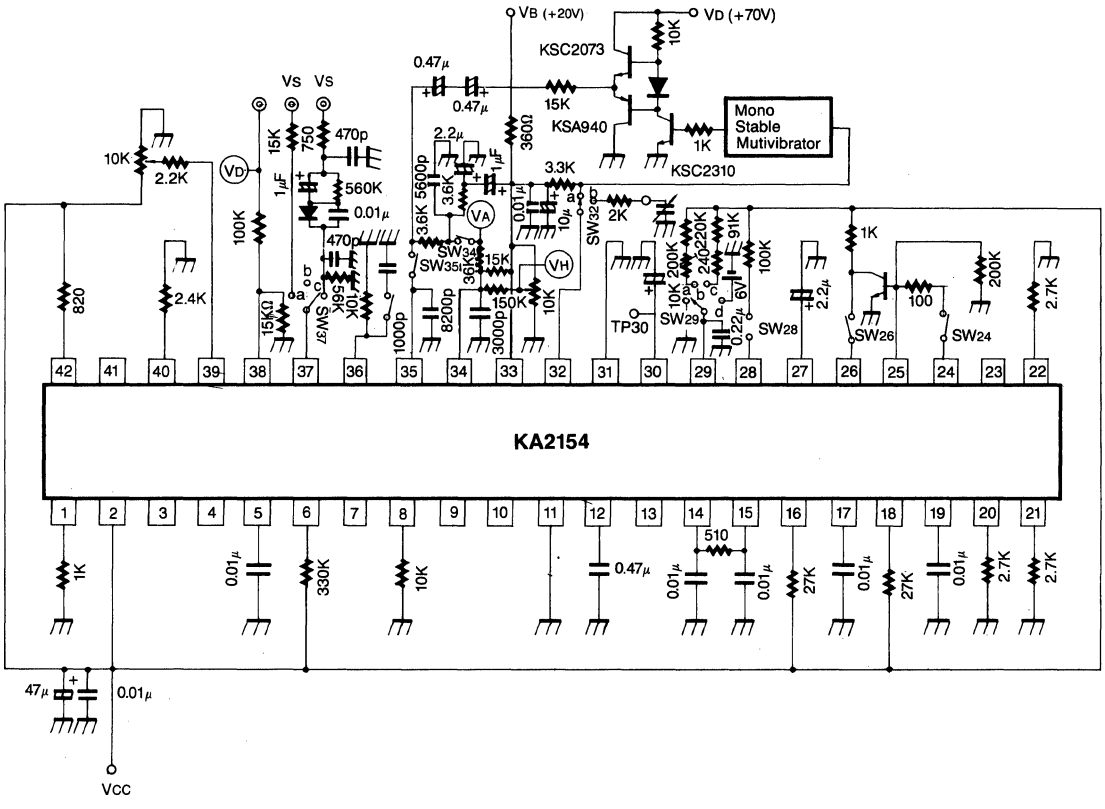
TEST CIRCUIT 3 (CHROMA PAL)



TEST CIRCUIT 4 (CHROMA PAL)



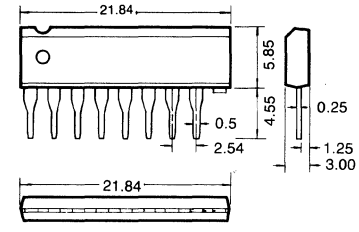
TEST CIRCUIT 5 (Deflection)



REMOTE CONTROL PREAMPLIFIER

The KA2181 is a silicon monolithic integrated circuit designed for a remote control preamplifier of infrared signals.
This device has features of low power, high sensitivity and wide supply voltage.

8 Sip Unit: mm



FUNCTIONS

- AMP • ABLC • LIMITTER & LEVEL SHIFT
- PEAK DET • SHAPING

FEATURES

- **Wide operation voltage** V_{CC} **=6 to 14.4V**
- **Low power consumption** I_{CC} **=2.5mA Typ.**
- **High input sensitivity** $50\mu V_{P-P}$ **Typ.**
- **Peak detector**
- **Small size package** **8 pin-SIP**
- **Minimum number of external parts required**
- **Designed for use with the KS5803 remote control transmitter IC.**

BLOCK DIAGRAM

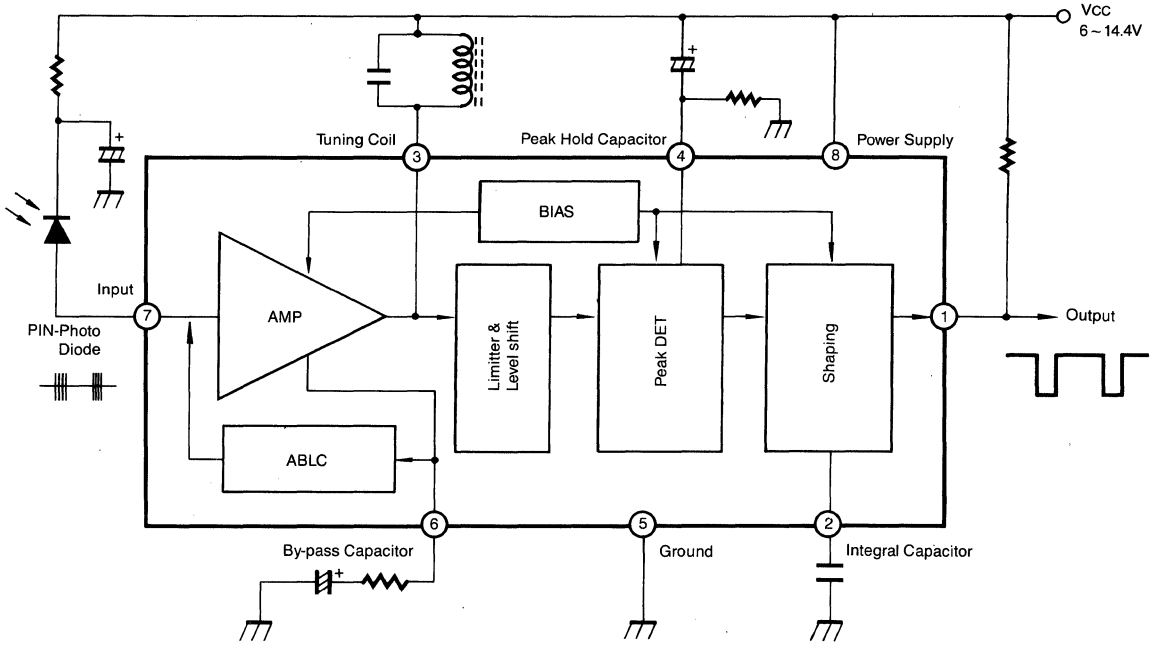


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Power Dissiation	P_d	270	mW
Operating Temperature	Topr	−20 to +75	°C
Storage Temperature	Tstg	−45 to +125	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	6.0	8.5	14.4	V
Input Frequency	f_{IN}	·30	—	50	KHz

ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=8.5V, F_{in}=40KHz)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{CC}		1.5	2.5	3.5	mA
Input Terminal Voltage	V_{IN} 1		2.1	2.6	3.1	V
Input Terminal Voltage	V_{IN} 2	I_{IN}=70μA	3.4	4.1	4.9	V
1st Stage Voltage Gain	A_{vL}	#7 ~ #3, V_{OUT}=500mV_{p-p}	—	60	—	dB
Detection Input Voltage	υ_{IN}		—	50	100	μV_{p-p}
Input Impedance	γ_{IN}		40	60	80	KΩ
Output Voltage	V_{OL}	I_{OL}=0.1mA, υ_{IN}=1mV_{p-p}	—	—	0.5	V
Output Leak Current	I_{OH}	V_{OH}=14.4V	—	—	2	μA
Noise		Input Open	Output Terminal is not fall			

TYPICAL APPLICATION CIRCUIT

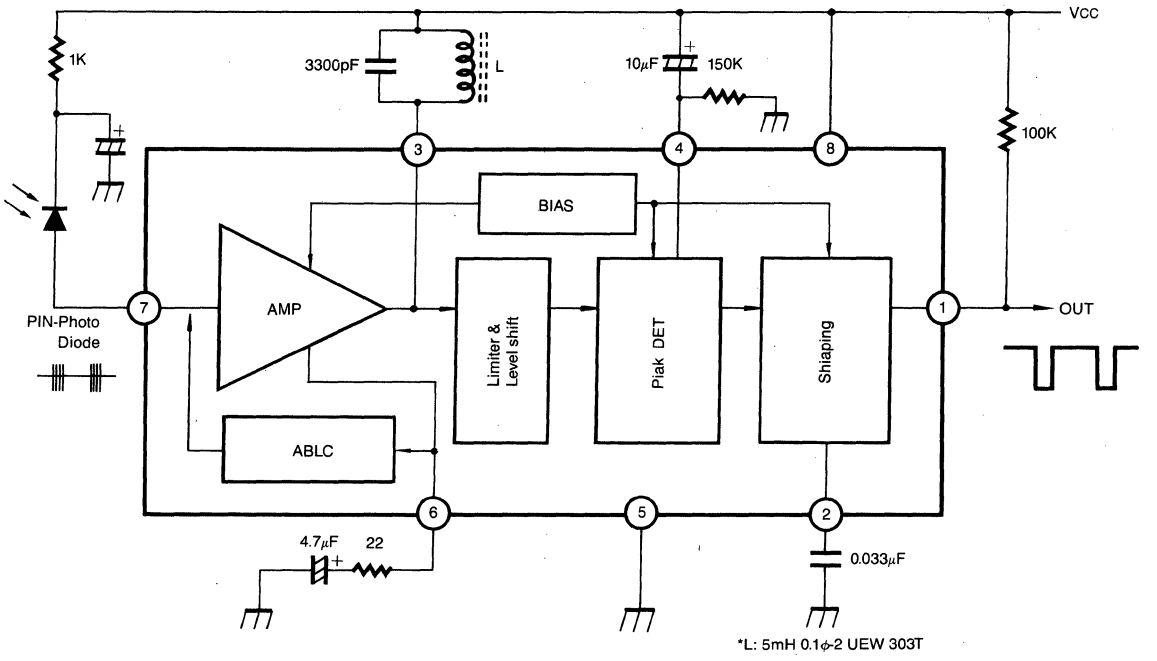


Fig. 2

TEST CIRCUIT

COIL 5mH 0.1φ-2 UEW 303T
C . . . 3300pF
R . . . 100K

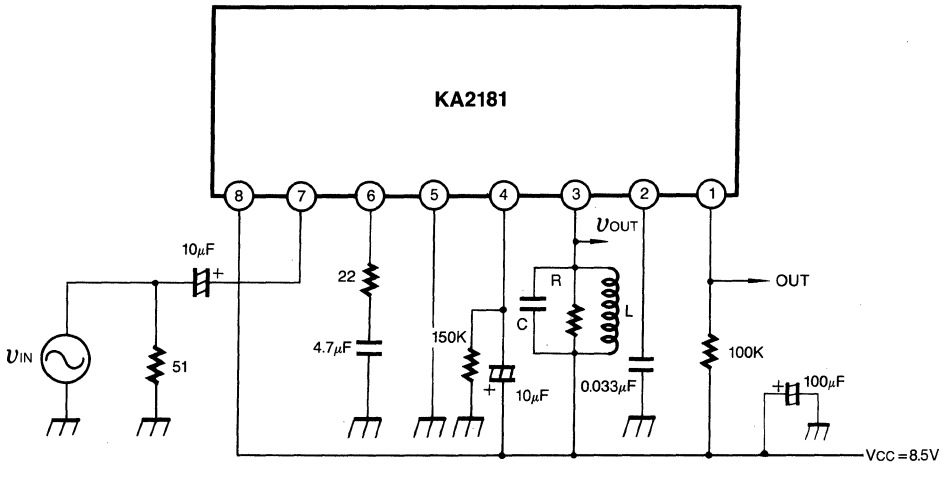


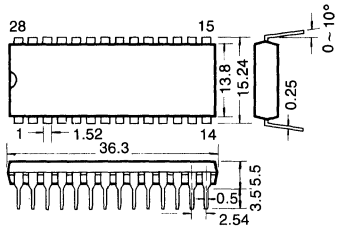
Fig. 3

TV MPX DEMODULATOR (KOREA TWO CARRIER SYSTEM)

The KA2268 is a integrated circuit for demodulating Korea two carrier TV-MPX broadcasts.

The use of PLL makes reed filters unnecessary. Uses include TV recievers, TV-MPX tuners etc. The KA2268 is suitable for the system with electronic attenuator.

28 Dip Unit: mm

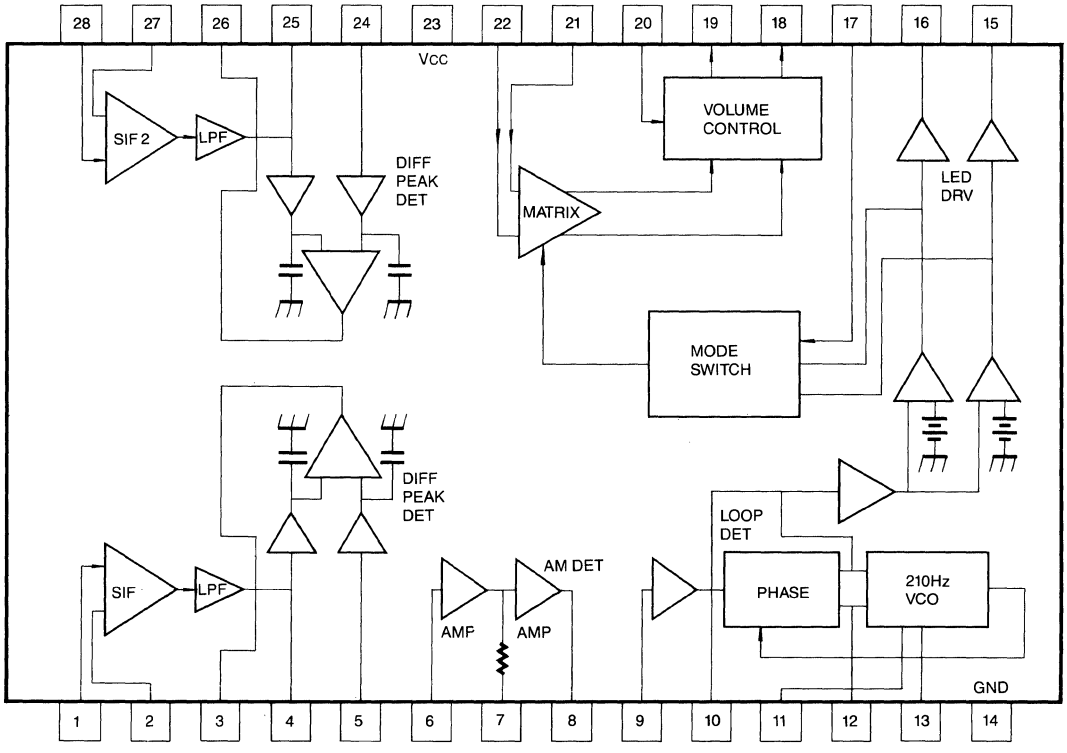


FUNCTION

- SIF limiter AMP.
- LPF.
- Matrix.
- Attenuator.
- Pilot Det.
- Mode SW.

FEATURES

- **Internal SIF amplifier and discriminators**
- **Internal electronic attenuator L/R Balance ±1dB (MAX)**



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Max Supply Voltage	V_{CC} max	15	V
Pin 15 Output Current	I_{15}	30	mA
Pin 16 Output Current	I_{16}	30	mA
Max Mode SW Voltage	V_{17}	$-0.3 \sim V_{CC}$	V
Max Volume Voltage	V_{20}	$-0.3 \sim V_{CC}$	V
Power Dissipation	Pd	1.5	W
Operating Temperature	Topr	$120 \sim 75$	°C
Storage Temperature	Tstg	$-40 \sim 125$	°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Characteristic	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Operating Voltage	V_{CC}			12		V
Circuit Current	I_{CC}	V_{CC} = 12V, V_I = 0			80	mA

SIF SECTION

(V_{CC} =12V, fm=400Hz, V_I =100dBu, T_a =25°C, Δf=±30KHz unless otherwise specified)

Characteristic	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Limiting Voltage	V_{lim} 1	f_O =4.5MHz, V_I =100dBu V_O =−3dB			400	μV
Input Limiting Voltage	V_{lim} 2	f_O = 4.724MHz, V_I = 100dBu, V_O = −3dB			400	μV
Det Output 1	V_{O1}	f_O =4.5MHz	0.8		1.5	V
Det Output 2	V_{O2}	f_O =4.724MHz	0.8		1.5	V
THD_1	THD_1	f_O =4.5MHz			2	%
THD_2	THD_2	f_O =4.724MHz			2	%
AMR_1	AMR_1	f_O =4.5MHz, AM=30%	35			dB
AMR_2	AMR_2	f_O =4.724MHz, AM=30%	35			dB
Input Impedance of Pin 28.1	Zin_{28}, Zin_1	f=4.5MHz		40		KΩ
Input Capacitance of Pin 28.1	C_{28}, C_1	f=4.5MHz		4.5		pF
Input Capacitance of Pin 24.5	C_{24}, C_5	f=4.5MHz	1.5	2.0	3.0	pF
Output Resistance of Det Output	Z_{26}, Z_3			1.2		KΩ
Crosstalk $SIF_1 \rightarrow SIF_2$	CT_1	SIF_1 f_O = 4.5m, fm=400 ~ 5K SIF_2 f_O =4.724m, Δf=0		55		dB
Crosstalk $SIF_2 \rightarrow SIF_1$	CT_2	SIF_1, f_O =4.5m, fm=400 ~ 5K SIF_2, f_O =4.724m, fm=400 ~ 5K		55		dB
Frequency Response of Detector	F_1	f_O =4.5MHz fm=40Hz ~ 55KHz	−6	0	1.5	dB
Frequency Response of Detector	F_2	f_O =4.724MHz fm=40Hz ~ 55KHz	−6	0	1.5	dB
Det Output Balance	C.B	SIF_1 =4.5m, SIF_2 =4.724m	−2	0	2	dB
Phase Difference of Det Output	Δφ	f_O =4.5MHz, fm=5KHz	−2	0	2	0

PILOT AMP AND DET

(V_{CC}=12V, f=55.125KHz, fm=150 or 276Hz, AM=50% unless otherwise specified)

Characteristic	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Resistance of Pin 6	Zin_6			30		KΩ
Max Pilot Input	VinPmax		20			mV
Det Gain	A_{VD}			36		dB
Det Output	V_{OD}	Vin=10mV		300		mVrms
Output Resistance of Pin 8	$Zout_8$			700		Ω

MODE CHANGE SWITCH CIRCUIT

Forced Mono Voltage	Vmono	SW=1		0	1.0	V
Main/Sub Supply Current	Im/s	SW=2	−0.2	0	0.2	mA
Sub/Sub Supply Voltage	Vs/s	SW=1	11	12		V

ELECTRONICS VOLUME CIRCUIT

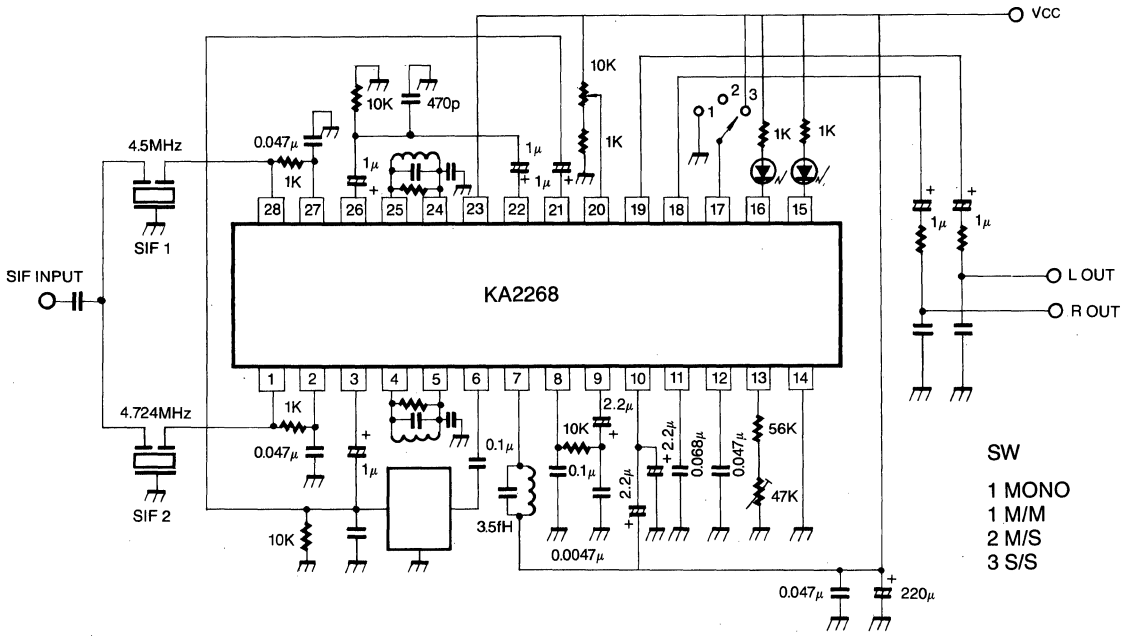
Output Impedance of Volume	Z_O (vr)			30		Ω
−3dB Pin Voltage	V_{20}		7.3	7.6	7.9	V
−20dB Pin Voltage	V_{20}		3.4	3.7	4.0	V
−60dB Pin Voltage	V_{20}			1.5		V
Channel Balance	C.B	$V_{20}=V_{CC}$	−1	0	1	dB

MATRIX CIRCUIT

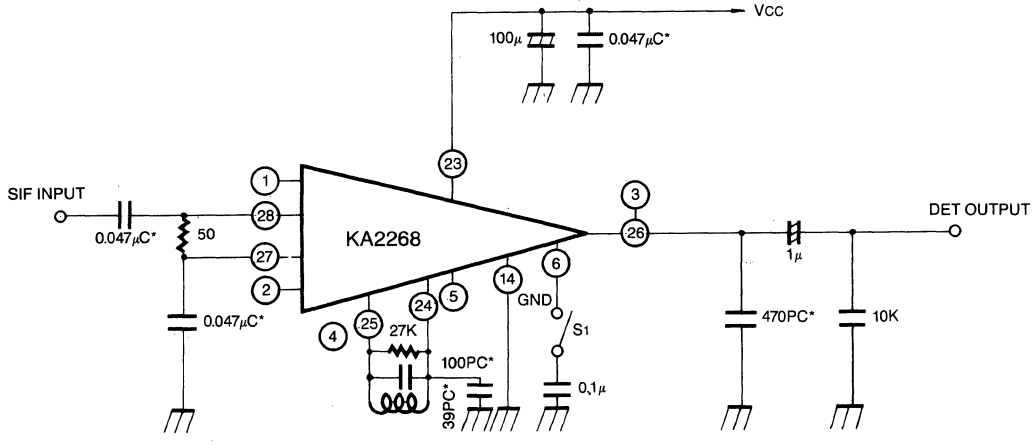
f=1KHz

Input Impedance of Matrix	$Zin_{(M)}$			10		KΩ
T.H.D in Main Mode	THD_M	V_I=50mVrms		0.3		%
T.H.D in Sub Mode	THD_S	V_i=50mVrms		0.3		%
T.H.D in Stereo Mode	THD_{ST}	V_I=50mVrms		0.3		%
Crosstalk (M→S)	$CT_{M\rightarrow S}$	V_I=50mVrms		55		dB
Crosstalk (S→M)	$CT_{S\rightarrow M}$	V_I=50mVrms		55		dB
Separation (L→R)	$SEP_{L\rightarrow R}$	V_I=50mVrms	35	40		dB
Separation (R→L)	$SEP_{R\rightarrow L}$	V_I=50mVrms	35	40		dB

TYPICAL APPLICATION CIRCUIT

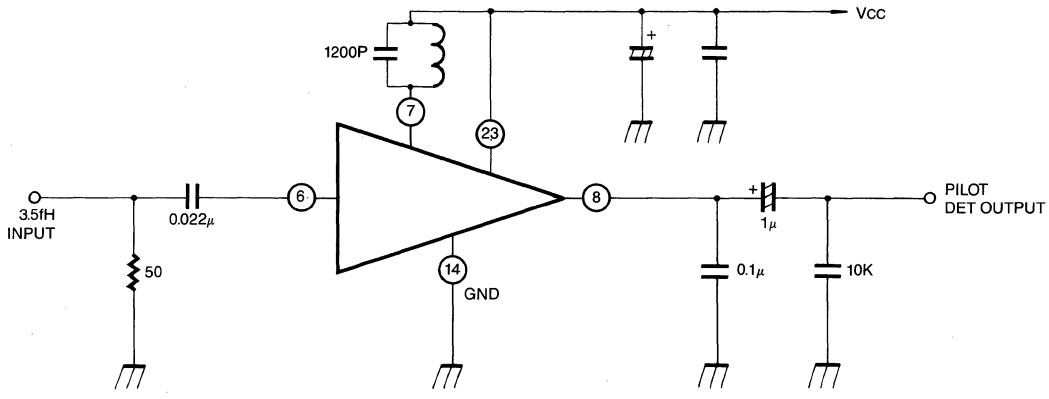


TEST CIRCUIT 1 SIF SECTION

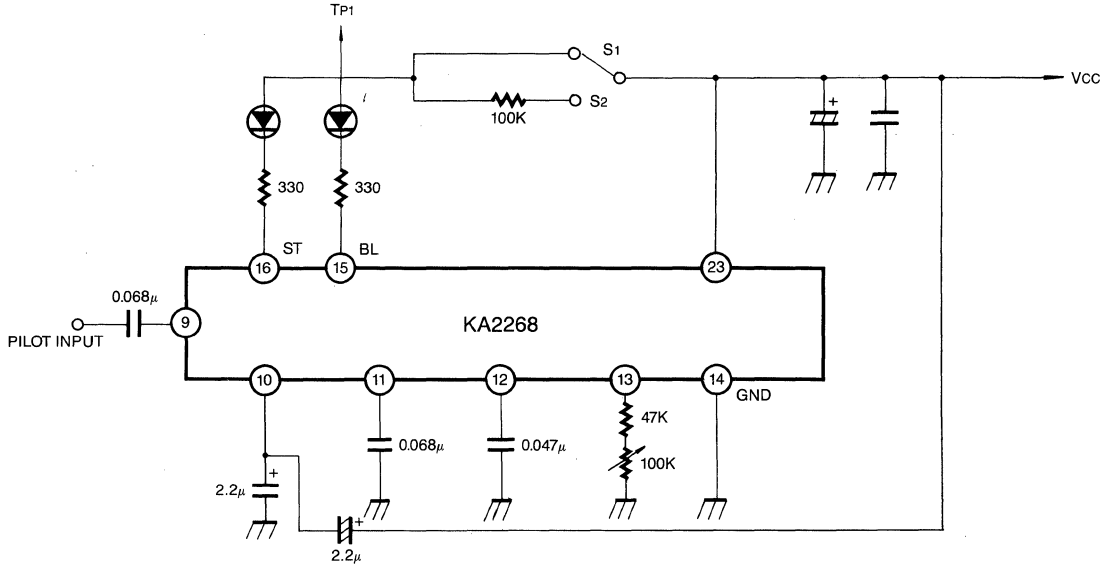


S1: PILOT IN NOISE BYPASS

TEST CIRCUIT 2 PILOT AMP/DET SECTION

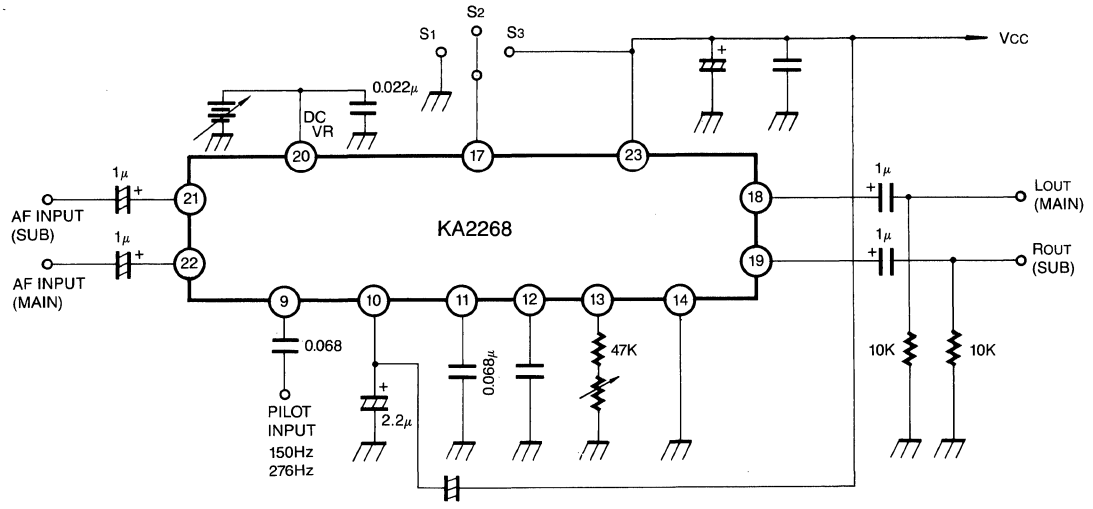


TEST CIRCUIT 3 PILOT PLL/INDICATOR SECTION

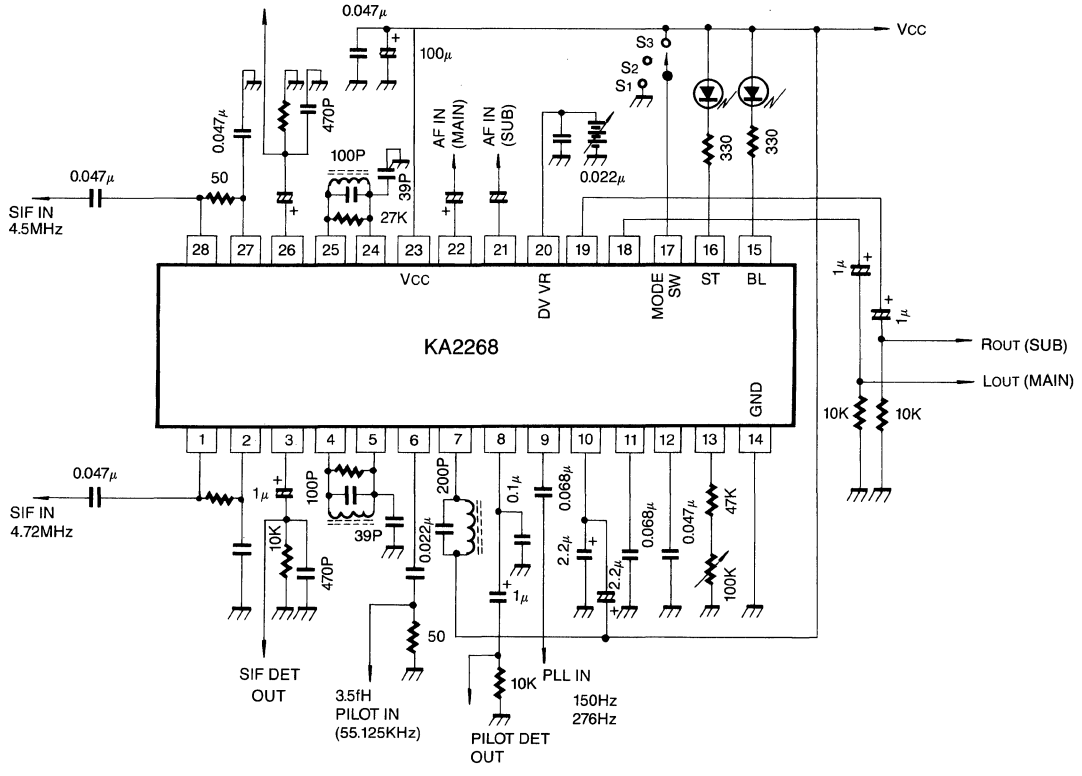


PIN 12: VCO FREQUENCY CHECK 210Hz ADJ

TEST CIRCUIT 4 MATRIX/DC VR/MODE SECTION



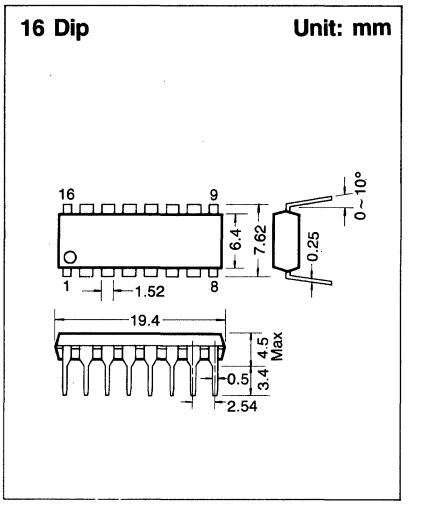
TEST CIRCUIT 5



VIDEO IF SYSTEM FOR COLOR TV

The KA2911, KA2916 is a silicon monolithic integrated circuit designed for VIF stage in color television receivers.

KA2911 for FET TUNER
KA2916 for NPN TUNER



FUNCTIONS

- Three controlld IF amplifier stages
- Video demodulator controlled by picture carrier
- Black noise and white noise inverter
- Peak AGC
- DC amplifier for RF AGC out
- Quadrature detector for AFT
- DC amplifier for AFT

FEATURES

- **High gain wide band IF amplifier**
- **Gain reduction with excellent stability**
- **Excellent DG/DP characteristics**
- **Excellent S/N characteristics due to delayed 3 stages AGC**
- **Negative video output signal**
- **Fast AGC action due to noise inverter and peak AGC**
- **Switch off the video part with VTR SW**
- **Dual differential AFT output**

BLACK DIAGRAM

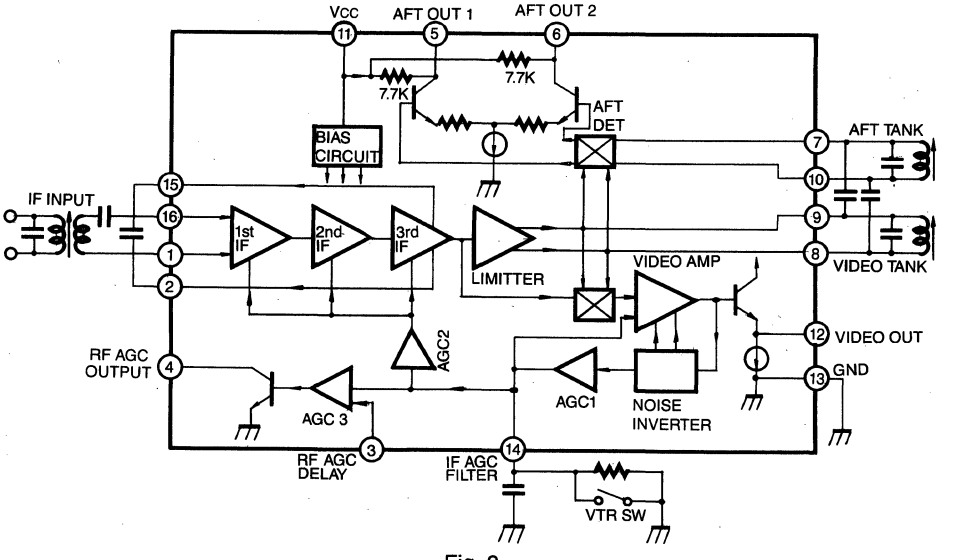


Fig. 2

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC} (Pin 11)	15	V
Open Loop Voltage	V_4 (Pin 4)	15	V
Video DC Output Current	I_{12} (Pin 12)	6	mA
Power Dissipation (Note)	P_d	1.4	W
Operating Temperature	Topr	−20 ~ +65	°C
Storage Temperature	Tstg	−55 ~ +150	°C

Note: Derated above T_a =25° in the proportion of 11.2mW

ELECTRICAL CHARACTERISTICS (T_a =25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Recommended Supply Voltage	V_{CC} (V_{11})		10.8	12.0	13.2	V	
Supply Current	I_{CC} (I_{11})	V_{CC} =12V	42	51	63	mA	1
Video DC Output Voltage	V_{12}	V_{CC} =12V	5.2	5.5	5.8	mA	1
AFT DC Output Voltage	V_5	V_{CC} =12V SW_1: ON, SW_2: ON	5.3	6.8	8.3	V	1
AFT Output Offset Voltage	V_5-V_6	V_{CC} =12V SW_1: ON, SW_2: ON	−1.5	0	1.5	V	1
RF AGC Residual Output Voltage	V_4 (sat)	V_{CC} =12V, SW_3:1, SW_4: 2 KA2916 SW_4: 1 KA2911	—	—	0.5	V	1
RF AGC Leak Current	I_4 (Leak)	V_{CC} =12V, SW_3: 1, SW_4: 2 KA2911 SW_4: 1 KA2916	—	—	1	μA	1
Video Sensitivity	v_I Pin (1-16)	V_{CC} =12V, V_{12} =0.8V_{p-p} f_o =45.75MHz AM: 30%	100	200	300	μVrms	2
AGC Range	ΔA (IF)	V_{CC} =12V, f_o =45.75MHz V_{14} = 11.5V→4.0V	60	64	—	dB	2
Sync Tip Level Voltage	V_{SYNC} (V_{12})	V_{CC} = 12V f_o =45.75MHz	2.3	2.5	2.7	V	2
Maximum IF Input Voltage	v_{IN} (Max)	V_{CC} =12V f_o =45.75MHz	100	120	—	mVrms	2
White Noise Threshold	V_{WTH} (V_{12})	V_{CC} =12V f_o =45.75MHz	5.8	6.2	6.6	V	2
White Noise Clamp Level	V_{WCL} (V_{12})	V_{CC} =12V f_o =45.75MHz	3.7	4.1	4.5	V	2
Black Noise Threshold	V_{BTH} (V_{12})	V_{CC} =12V f_o =45.75MHz	1.4	1.6	1.8	V	2
Black Noise Clamp Level	V_{BCL} (V_{12})	V_{CC} =12V f_o =45.75MHz	2.9	3.3	3.7	V	2
Video Frequency Response	F_{BW}	Input 45.75MHz Sweep generator	4.5	5.5	—	MHz	2

ELECTRICAL CHARACTERISTICS (T_a =25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Suppression of Carrier		SG=100mVrms SG_2, SG_3 OFF	40	50	—	dB	4
Suppression of and 2nd Carrier	I2nd	SG_1 =100mVrms SG_2, SG_3 OFF	40	50	—	dB	4
Suppression of Sound Carrier Color Subcarrier	I_{920}	SG_1 =100mVrms SG_2 =32mVrms SG_3 =32mVrms	33	38	—	dB	4
Differential Phase	DP		—	3.5	5	deg	3
Differential Gain	DG		—	7	10	dB	3
Input Impedance	R_{IN}	f_o =45.75MHz between Pin 16-1	3.0	4.5	6.0	KΩ	
	C_{IN}		—	2.0	5.0	pF	
AFT Sensitivity	$\Delta F/\Delta V_{5-6}$	f_o =45.75MHz	—	16	—	KHz/V	2
AFT Output Upper Voltage	V_5, V_6 (UPP)	f_o =45.75MHz	11.7	11.9	12.0	V	2
AFT Output Lower Voltage	V_5, V_6 (Low)	f_o =45.75MHz	1.8	2.3	2.8	V	2
Max Available Current	I_4 (max)	KA2911	0.3	—	—	mA	2
		KA2916	7	—	—	mA	

TYPICAL APPLICATION CIRCUIT

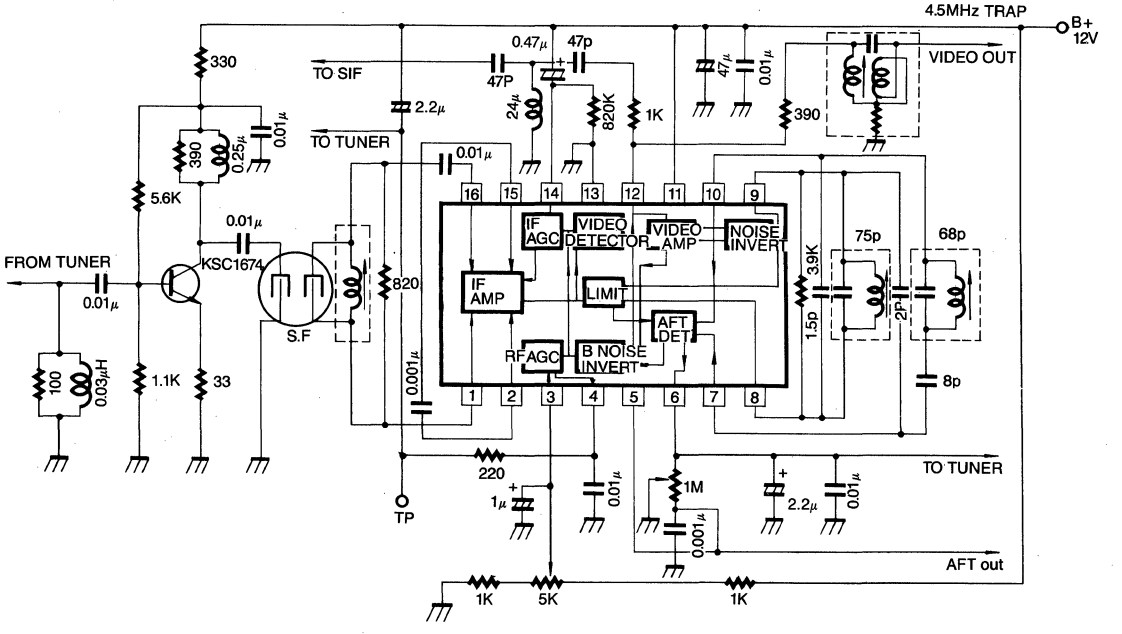


Fig. 2

TEST CIRCUIT 1 (DC Characteristics)

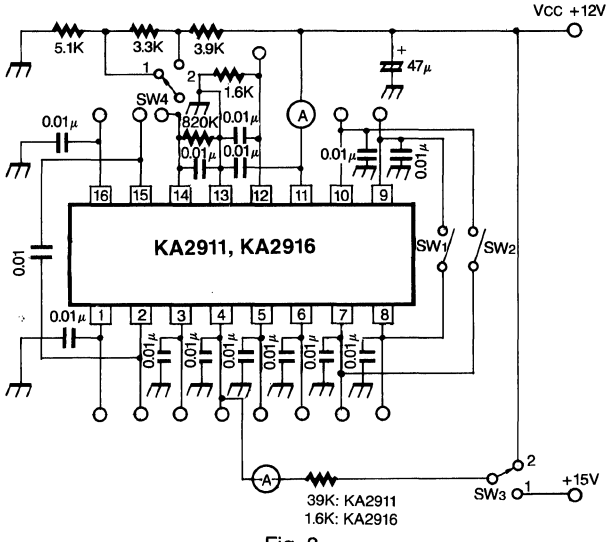


Fig. 3

TEST CIRCUIT 2 (Dynamic Characteristics)

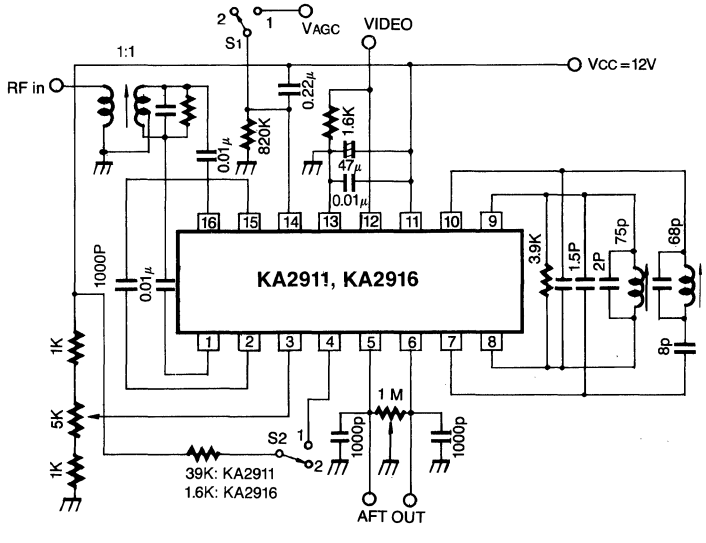


Fig. 4

TEST CIRCUIT 3 (DP, DG)

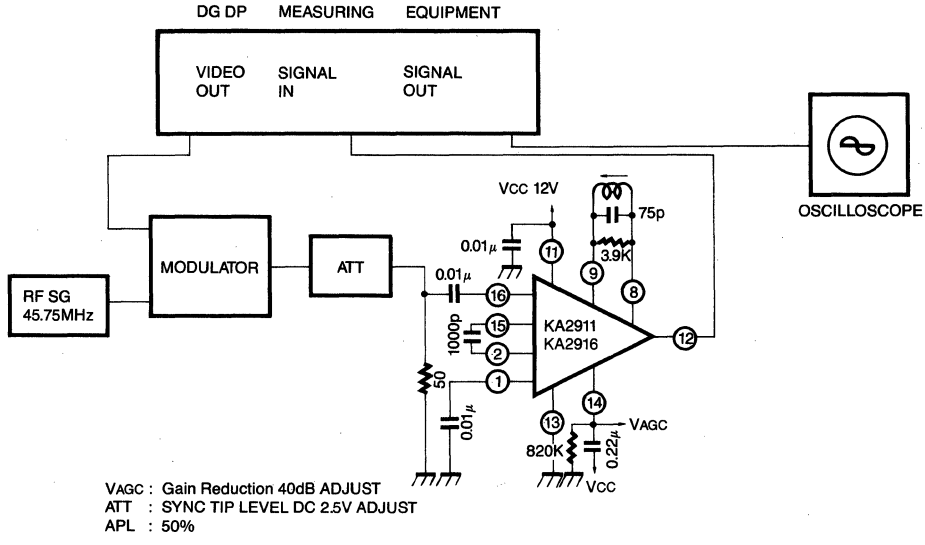


Fig. 4

TEST CIRCUIT 4 (Inter Modulation)

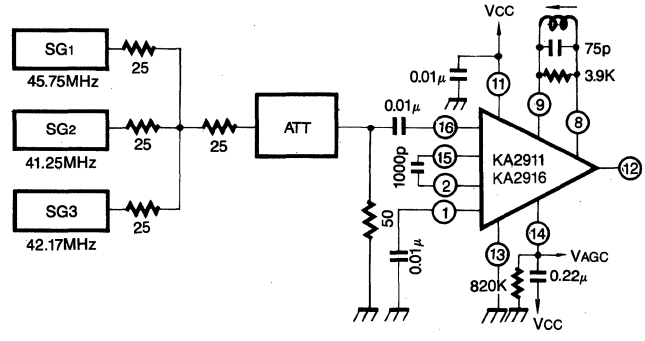
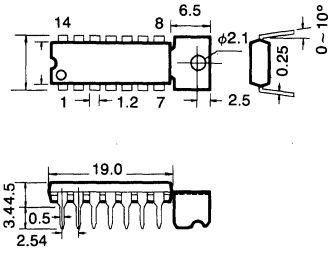


Fig. 5

VIDEO IF PROCESSOR FOR B/W TV

The KA2912 is a silicon monolithic integrated circuit designed for VIF section in B/W television receivers.
This IC has all functions including video IF amplifier, video low-level detector, RF AGC, IF AGC and noise canceller.
This IC is encapsulated in 14 pin dual in-line package with heat sink.

14 Dip H/S Unit: mm



FEATURES

- **High input sensitivity: Typ 30 dBμ.**
- **It can be used both of keyed type AGC and peak type AGC.**
- **It can be operated with the power supply voltage above 7V.**
- **Since the video detector has wide bandwidth, it's suitable for the sound carrier frequency of 4.5, 5.5, 6.0, 6.5 MHz.**
- **As input is differential mode, it can be used width saw filter.**
- **All function of VIF stage are provided by this single chip IC will realize reduction of assembly cost as well as reduction of number of external components.**

BLOCK DIAGRAM

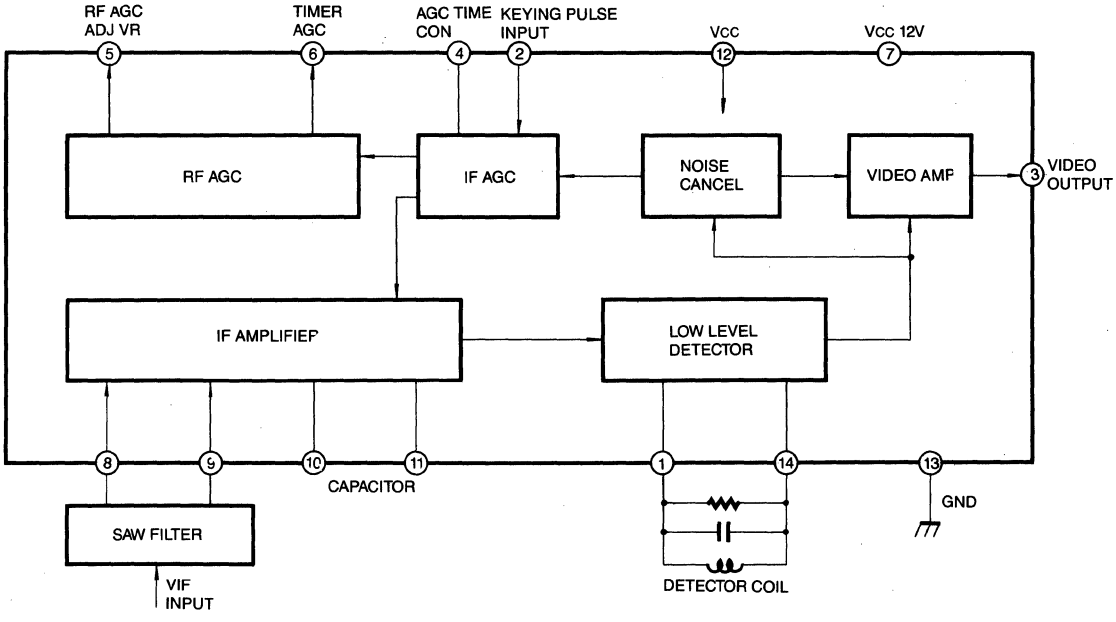


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC} (Pin 7)	15	V
Input Singnal Voltage	V_8, V_9	3	V_{p-p}
Power Dissipation	P_d	875 (T_a =75°C) free air	mW
Operating Temperature	Topr	−20 ~ +75	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS (T_a =25°C, V_{CC} =12V, f=45.75MHz, F_M =15.75KHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Total Supply Current	I_{CC}	I_7+I_{12}, R_A =150Ω	40	50	60	mA	1
Input Sensitivity	V_i	MOD=80%, V_o =1.4V_{p-p}	—	30	35	dBμ	1
Maximum Input Voltage	V_i (max)	MOD=80%−1dB Point	100	—	—	dBμ	1
Video Output Voltage	V_o	MOD=80%, V_i =3mVrms	1.0	1.4	1.7	V_{p-p}	1
Video Output DC Voltage	V_o	No Signal	3.3	3.8	4.3	V	1
Signal to Noise Ratio	S/N	MOD=80%−0% V_i =3mVrms	40	50	—	dB	1
RF AGC Voltage (High)	V_{6H}	V_5 =0V	8	9	11	V	1
RF AGC Voltage (Low)	V_{6L}	V_5 =7V	—	0	0.5	V	1
Differential Gain	D.G.	Stair step F_M =3.58MHz	—	—	10	%	1
Differential Phase	D.P.	Stair step F_M =3.58MHz	—	—	10	deg	1
Video Detector Band Width	BW	−3dB Point	5.5	—	—	MHz	1
Input Resistance	R_{in}		—	1.5	—	KΩ	1
Input Capacitance	C_{in}		—	3.3	—	pF	1

TYPICAL APPLICATION CIRCUIT

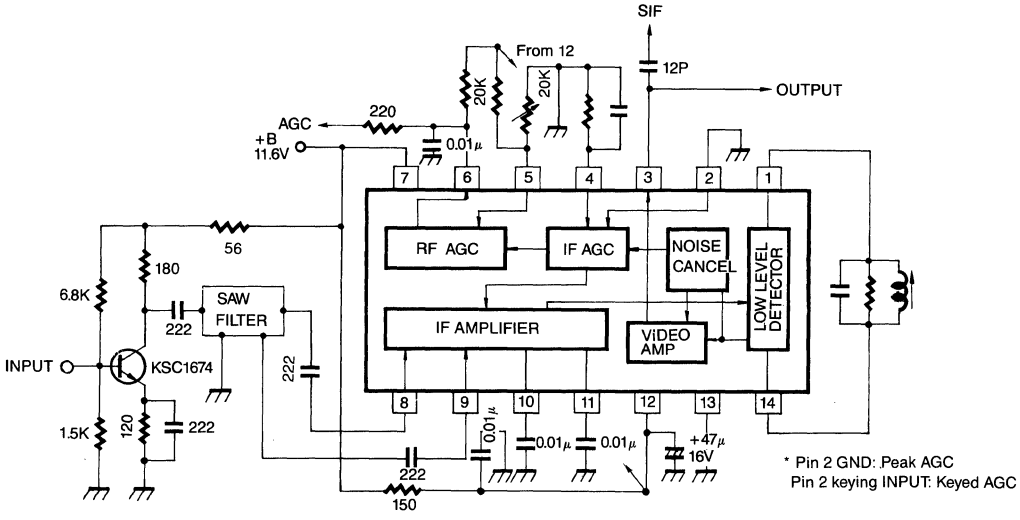


Fig. 2

TEST CIRCUIT

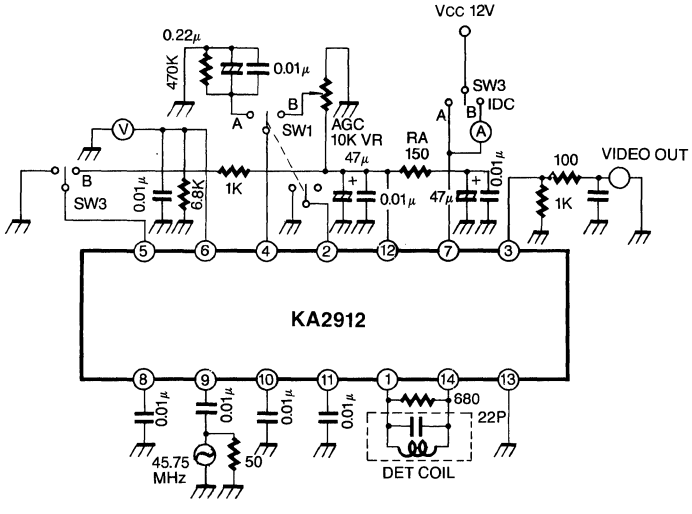
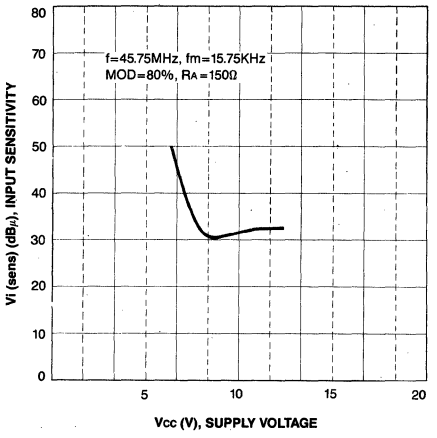
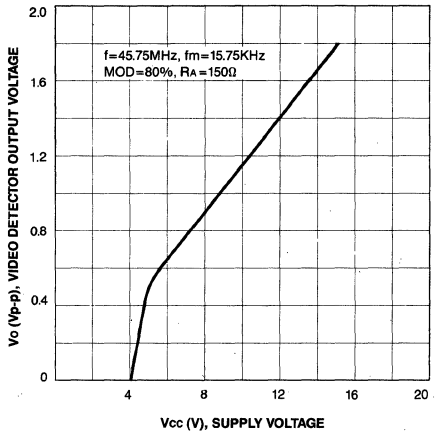


Fig. 3

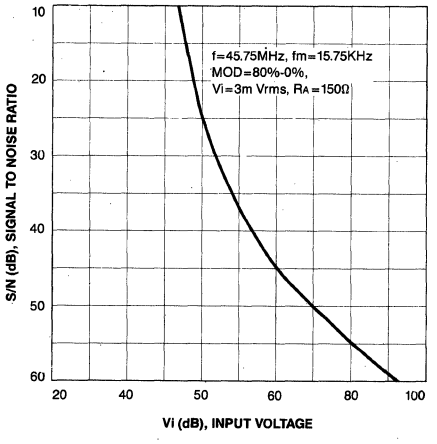
INPUT SENSITIVITY



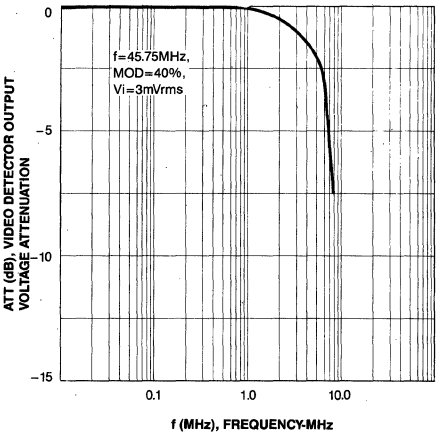
VIDEO DETECTOR OUTPUT VOLTAGE Vs SUPPLY VOLTAGE



S/N Vs INPUT VOLTAGE



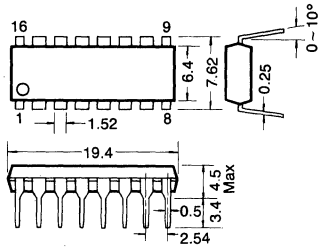
VIDEO DETECTOR OUTPUT VOLTAGE ATTENUATION Vs FREQUENCY



VIDEO AND SOUND IF AMPLIFIER FOR MONOCHROME TV RECEIVERS

The KA2913A is a silicon monolithic integrated circuit designed for VIF and SIF stage in B/W television receivers.

16 Dip Unit: mm



FUNCTION

VIF stage

- Three controlled IF amplifier stages
- Video demodulator controlled 3 picture carrier
- Black noise and write noise inverter peak AGC
- DC amplifier for RF AGC output

SIF stage

- Three controlled IF amplifier stages
- Quadrature detector

FEATURE

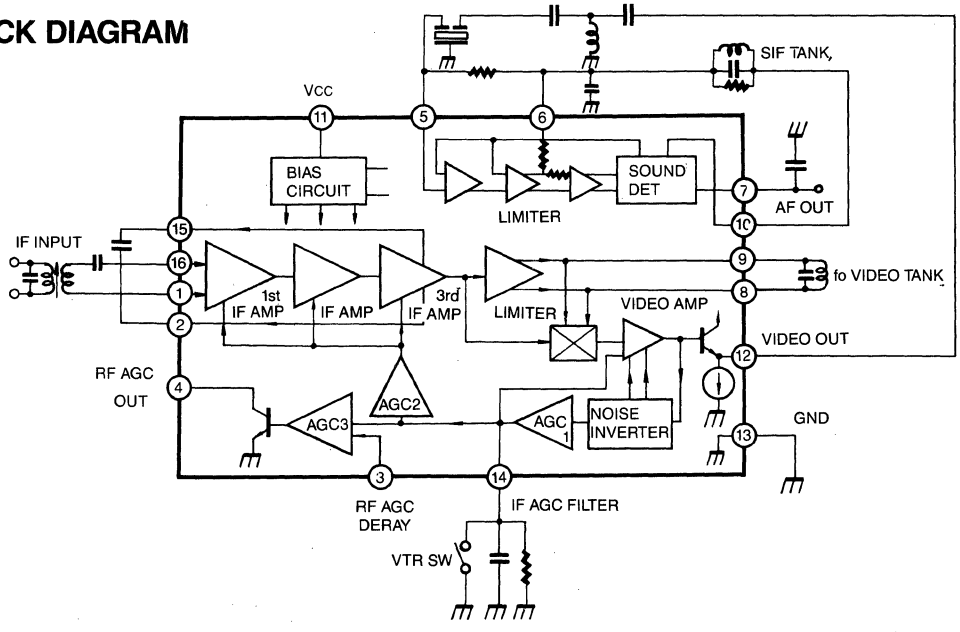
VIF stage

- **High gain, wide band IF amplifier: 50dB (Typ.) at 58MHz**
- **Gain reduction with excellent stability: 55dB (Typ.) at 58MHz**
- **Excellent DG/DP characteristics: DG 7% (Typ.), DP 3.5 deg. (Typ.)**
- **Excellent S/N characteristics due to delayed 3 stage AGC action.**
- **Fast AGC action due to noise inverter and peak AGC.**
- **Switch off the video part with VTR switch.**

SIF stage

- **Excellent limiter characteristics.**
- **Excellent AM rejection.**
- **Large undistorted audio output voltage with quadrature detector.**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage (Pin 11)	V_{CC}	15	V
Open Loop Voltage (Pin 4)	V_4	15	V
Video DC Output Current (Pin 12)	I_{12}	6	mA
Power Dissipation (Note)	P_d	1.4	W
Ambient Temperature	T_a	−20 ~ 65	°C
Storage Temperature	Tstg	−55 ~ 150	°C

Note: Derated above T_a =25°C in the proportion of 11.2 mW/°C.

ELECTRICAL CHARACTERISTICS
PIF Stage (T_a =25°C, V_{CC} =12V, f_p =45.75MHz, f_s =41.25MHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Recommended Supply Voltage	V_{CC} (V_{11})	—	10.8	12.0	13.2	V	—
Supply Current	I_{CC} (I_{11})	S_1: On, S_3: 2, S_5: 2, S_4: 1	35	50	65	mA	1
Video DC Output Voltage	V_{12}	S_1: Off, S_3: 2, S_5: 2, S_4: 1	5.2	5.5	5.8	V	1
Terminal Voltage 5	V_5	S_1: On, S_3: 2, S_5: 2, S_4: 1	3.5	4.4	5.3	V	1
Terminal Voltage 7	V_7	S_1: On, S_3: 2, S_5: 2, S_4: 1	4.6	6.0	7.2	V	1
RF AGC Residual Output Voltage	V_4 Sat	S_1: Off, S_3: 2, S_5: 2, S_4: 1	—	—	0.5	V	1
RF AGC Leak Current	I_4 Leak	S_1: Off, S_3: 1, S_5: 1, S_4: 2	—	—	1	μA	1
Video Sensitivity	v_1 Pin-16	(Note 1)	60	150	250	μV_{rms}	2
AGC Range	ΔA (IF)	(Note 2)	60	64	—	dB	2
SYNC TIP Level Voltage	V_{SYNC} (V_{12})	(Note 3)	2.3	2.5	2.7	V	2
Maximum IF Input Voltage	v_{IN} Max PIF	(Noite 4)	100	120	—	mV_{rms}	2
White Noise Threshold	V_W TH (V_{12})	(Note 5)	5.8	6.2	6.6	V	2
White Noise Clamp Level	V_{WCL} (V_{12})	(Note 5)	3.7	4.1	4.5	V	2
Black Noise Threshold	V_B TH (V_{12})	(Note 5)	1.4	1.6	1.8	V	2

ELECTRICAL CHARACTERISTICS
PIF Stage (T_a =25°C, V_{CC} =12V, f_p =45.75MHz, f_s =41.25MHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Black Noise Clamp Level	V_B CL (V_{12})	(Note 5)	2.9	3.3	3.7	V	2
Video Frequency Response	f_{BW}	(Note 6)	4.5	5.5	—	MHz	3
Suppression of Carrier	CL	(Note 7)	40	50	—	dB	4
Suppression of 2nd Carrier	I_{2nd}	(Note 8)	40	50	—	dB	4
Suppression of Sound Carrier/ Color Subcarrier	I_{920}	(Note 9)	33	38	—	dB	4
Differential Phase	DP	(Note 10)	—	3.5	5	deg	5
Differential Gain	DG	(Note 10)	—	7	10	%	5
VIF Input Impedance	R_{IN} (VIF)	(Note 11)	1.5	3.0	6.0	KΩ	6
	C_{IN} (VIF)		—	3.0	10.0	pF	
Max. Available Current	$I_{4\ MAX}$	(Note 12)	7	—	—	mA	1
RF AGC Delay Point Range	V_{IN} Delay	(Note 13)	5.0	7.0	9.0	V	2
Video Output Level	υ_{OUT}	(Note 14)	2.25	2.5	2.75	V	2

ELECTRICAL CHARACTERISTICS
SIF Stage (T_a =25°C, V_{CC} =12V, f_p =45.75MHz, f_s =41.25MHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
SIF Output Voltage	S_{OUT}	(Note 15)	200	400	600	mV_{rms}	3
Input Limiting Voltage	V_{IN} (Lim)	(Note 16)	—	200	400	μV_{rms}	8
AM Rejection Ratio	AMR	(Note 17) $R_L = \infty$, $R_D = \infty$	40	45	—	dB	8
Recovered Output Voltage	V_{OD}	(Note 18) $R_L = \infty$, $R_D = \infty$	0.5	0.75	—	V_{rms}	8
Total Harmonic Distortion	THD	(Note 18) $R_L = \infty$, $R_D = \infty$	—	1.0	2.0	%	8
Max. Audio Output Voltage	V_{OM}	(Note 19)	4.0	—	—	V_{P-P}	8
SIF Input Impedance	R_{IN} (SIF)		10	20	30	KΩ	7
	C_{IN} (SIF)		—	3	10	pF	
Audio Output Impedance	$R_{O\ (AF)}$	(Note 20)	10	15	20	KΩ	9

Note 1) V_{AGC} (TP14 EXT. Applying voltage)=11.5V
VIF in: f=45.75MHz 1kHz 30% AM modulation
Adjust VIF input level v_i so that the detected output of TP12C with high impedance probe will be $0.8V_{P\text{-}P}$ and measure the input level.

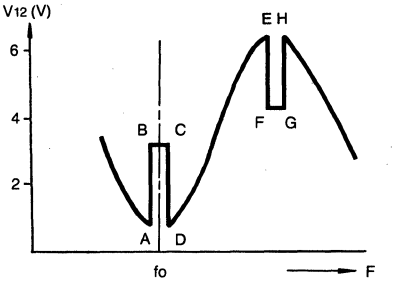
Note 2) V_{AGC}=4V
Measure pif input level V_i same as note 1

$$\Delta A = 20 \log \frac{v_i'}{v_i} (dB)$$

Note 3) VIF in: f=45.75MHz CW 15mVrms
Measure DC level of TP12A

Note 4) VIF in: f=45.75MHz APL100%, 87.5% AM modulation.
TP14: open
(1) Adjust VIF input level $50mV_{P\text{-}P}$ and measure the detected output level $v_O 1V_{p\text{-}p}$
(2) Then increase the input level so that the detected output level will be $1.1\times v_O 1V_{p\text{-}p}$ and measure the input level.

Note 5) V_{AGC}=8V
VIF in: f=45.75MHz±10MHz variable or sweep 15mVrms measure DC level of TP12A



AD; V_{BTH}
BC; V_{BCL}
EH; V_{WTH}
FG; V_{WCL}

Note 6) V_{AGC}=8V (GR×80dB)
SG_1: 45.75MHz CW
SG_2: 45.65-40MHz variable
(1) Setting output of SG_1 so that DC level of TP12A will be 4.0V
(2) Setting output of SG_2 (45.65MHz) so that AC level of TP12A will be $0.5V_{P\text{-}P}$
(3) Decreasing frequency of SG_2 until AC level of TP12A will be $0.35V_{P\text{-}P}$ (−3dB of $0.5V_{P\text{-}P}$) then read f_{SG2}=F
f_{BW}=45.75-F MHz

Note 7) SG_1: 45.75MHz, 1kHz 80% AM modulation 100mVrms
SG_2, SG_3; off
Setting V_{AGC} so that output AC level of TP12A will be $2.7V_{P\text{-}P}$
Measure CL of TP12A after setting to 0% AM of SG_1

Note 8) Measure I2nd of TP12A same as Note 9

Note 9) V_{AGC}=8V
SG_1: 45.75MHz (P: picture) 100mVrms
SG_2: 41.25MHz (S: sound) 32mVrms (−10dB of SG_1)
SG_3: 42.17MHz (C: chroma) 32mVrms (−10dB of SG_1)
(1) Setting V_{AGC}so that the output TIP level (lower) of TP12A will be 3.0V DC
(2) Measure the level difference (dB) between C-level and 920kHz level

Note 10) V_{AGC}=8V
VIF in: f=45.75MHz video signal (RAMP) 87.5% AM $100mV_{P\text{-}P}$
Setting ATT so that the SYNC TIP level of TP12A will be 2.5V DC measure DP and DG.

Note 11) V_{AGC}=5V f=45.75MHz
Measure R_{IN}, C_{IN}

Note 12) S_1: On, S_3: 2, S_5: 1 S_4: 2

Note 13) TP14: Open
VIF in: 45.75MHz CW 20mVrms
(1) Adjust the voltage of terminal 3 so that the voltage of terminal 4 will 6.0V DC
(2) Measure the terminal voltage 3

Note 14) TP14: Open
VIP in: 45.75MHz 100% APL 87.5% AM modulation signl amplitude 50mV_{P-P} measure detected output voltage (white peak to SYNC TIP)

Note 15) TP14: Open
SG_1: 45.75MHz CW 100mVrms
SG_2: 41.25MHz CW 25mVrms
Measure SIF (4.5MHz) output voltage at TP12A

Note 16) SIF IN: f=4.5MHz FM f_{MOD}=400Hz $\Delta f=\pm 25$kHz
(1) Adjust SIF input level 100mV_{P-P} and measure the detected output level υ_{OS}
(2) Then decrease the input level so that the detected output level will be 3dB down of υ_{OS} and measure the input level.

Note 17) SIF IN: f=4.5MHz FM: f_{MOD}=400Hz $\Delta f=\pm 25$kHz
AM 30%
Input level υ_{INS}=100dBμ

Note 18) SIF IN: f=4.5MHz FM: f_{MOD}=400Hz $\Delta f=\pm 25$kHz
Input level υ_{INS}=80dBμ

Note 19) SIF in: f=4.4-4.6MHz variable or sweep measure the output DC voltage change

Note 20) SIF IN: f=4.5mHz FM: f_{MOD}=400Hz $\Delta f=\pm 25$kHz
Input level υ_{INS}=80dBμ
(1) Measure the detected output voltage V_{OA} with $R_X=\infty$
(1) Then, adjust R_X so that the detected output voltage will be $\frac{V_{OA}}{2}$ and measure R_X.

1. DC TEST CIRCUIT

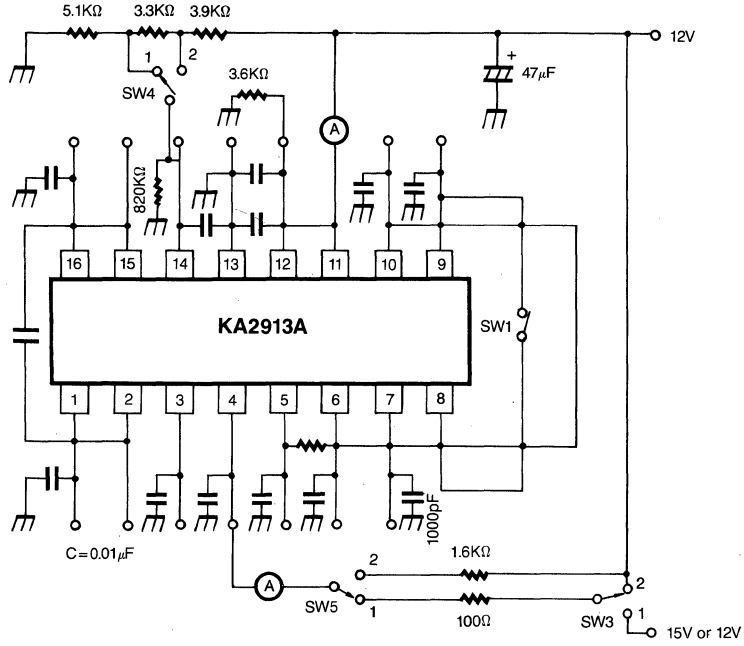


Fig. 1

2. AC TEST CIRCUIT

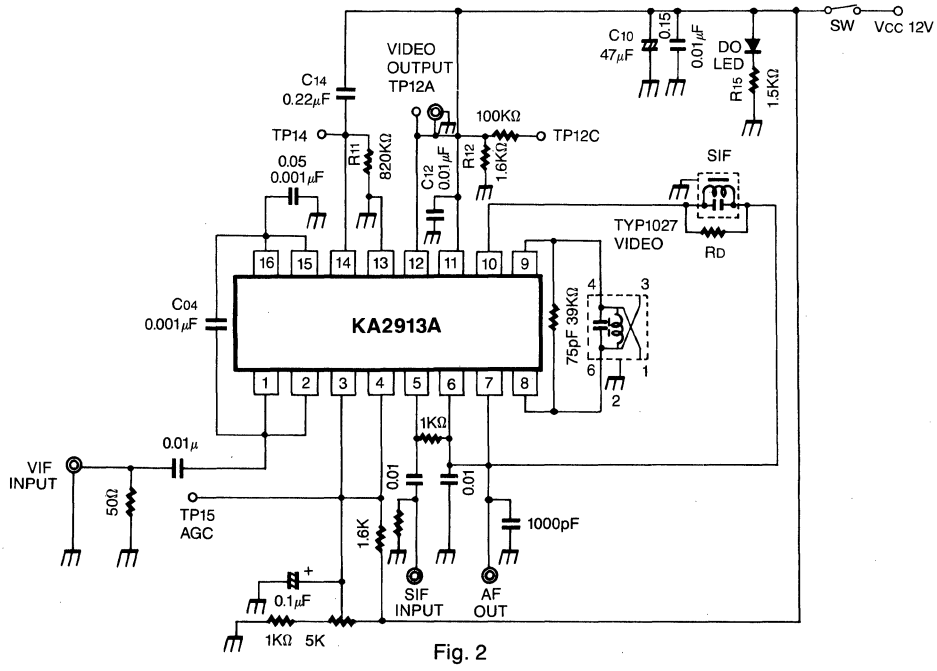


Fig. 2

3. VIDEO FREQUENCY RESPONSE & SIF OUTPUT VOLTAGE TEST CIRCUIT

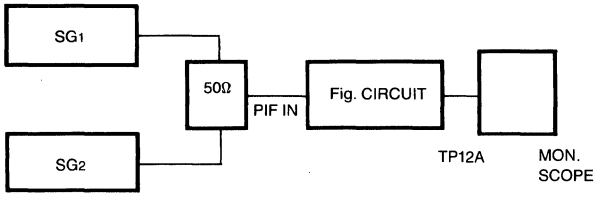


Fig. 3

4. INTER MODULATION TEST CIRCUIT

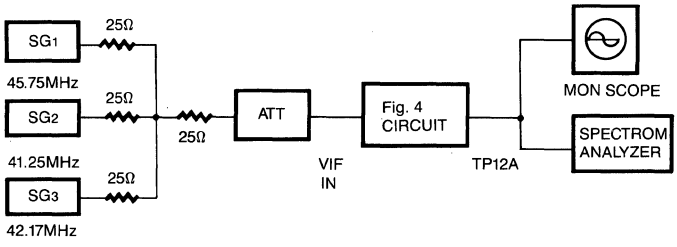
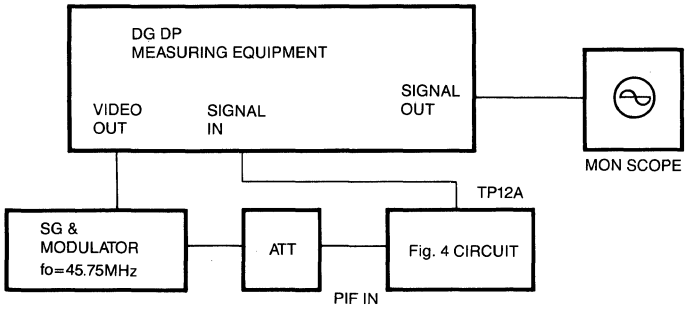


Fig. 4

5. DG, DP TEST CIRCUIT



APL: 50%
ATT: ADJUST SYNC TIP LEVEL TO DC2.5V

Fig. 5

6. INPUT IMPEDANCE TEST CIRCUIT

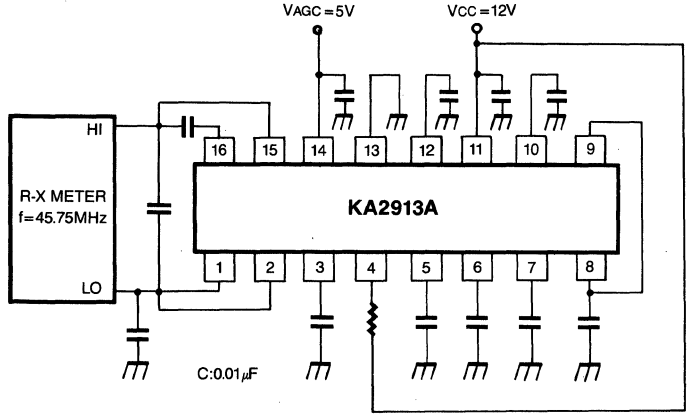


Fig. 6

7. SIF INPUT IMPEDANCE TEST CIRCUIT

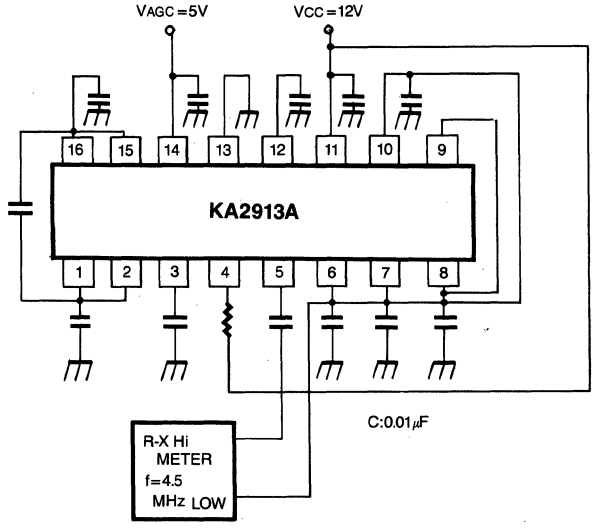


Fig. 7

8. V_{IN} (LIM), AMR, V_{OD}, THD, V_{OM} TEST CIRCUIT

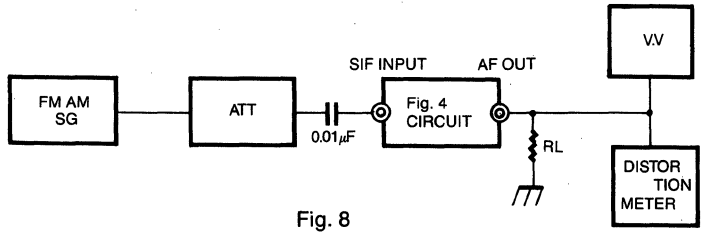


Fig. 8

9. AUDIO OUTPUT IMPEDANCE TEST CIRCUIT

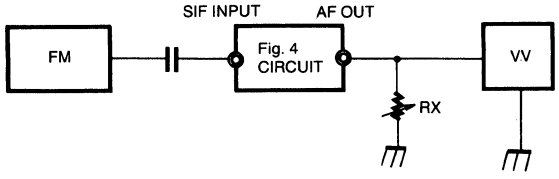
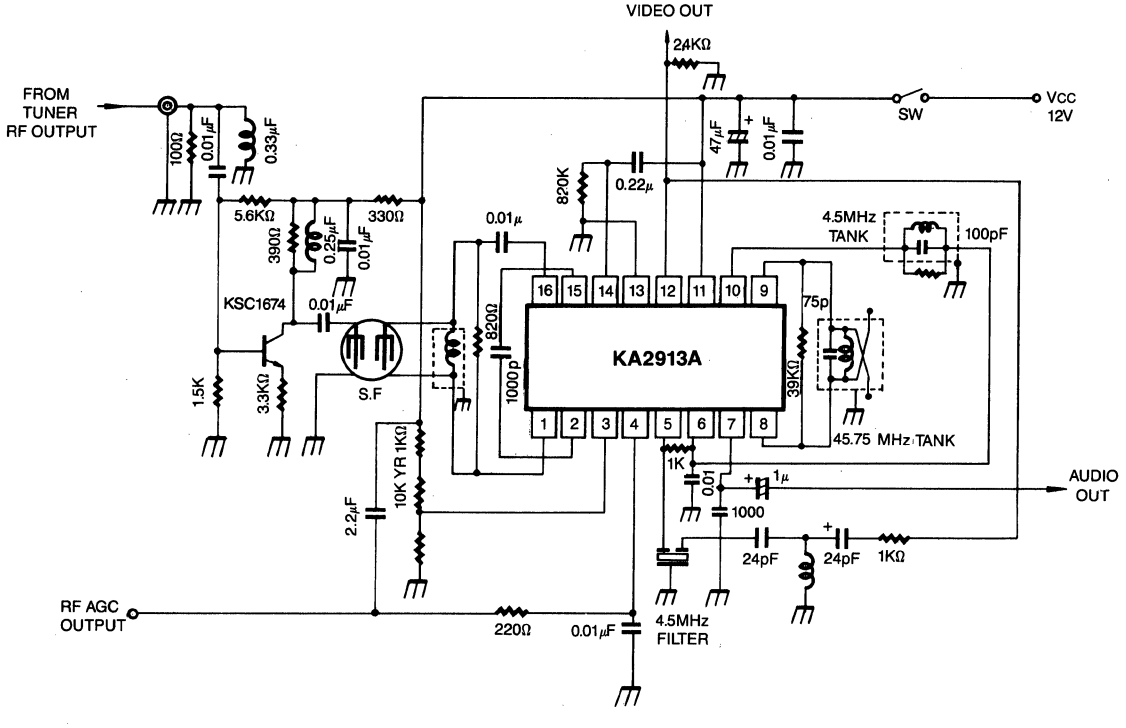


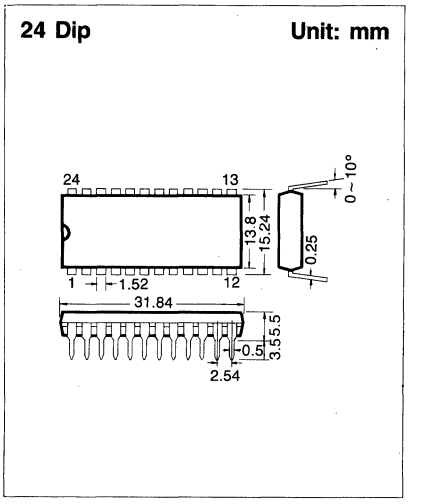
Fig. 9

TYPICAL APPLICATION CIRCUIT



VIDEO IF+SIF SYSTEM FOR COLOR TV

The KA2914A is a silicon monolithic intergrated circuit designed for VIF and SIF stage in color television receivers.



FUNCTIONS

VIF

- Three controlled IF amplifier stages
- Video demodulator controlled by picture carrier
- Black noise and white noise inverter
- Peak AGC
- DC amplipier for RF AGC out

SIF

- Three differential IF amplifier stages
- Phase detector
- DC controlled attenuator
- Audio amplifier stage with NFB terminal

FEATURES

- **PIF, SIF, ATT audio driver**
- **2 chip color TV system is possible with KA2153**

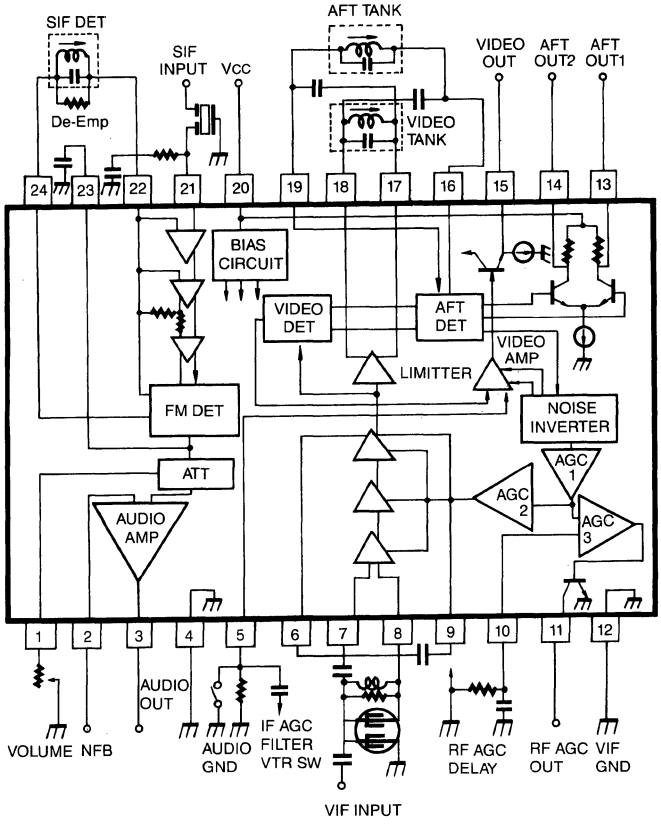
VIF

- **High gain, wide band IF amplifier**
- **AGC characteristics with excellent stability**
- **Excellent DG/DP characteristics**
- **Excellent S/N characteristics due to delayed 3 stages AGC action**
- **Negative video output signal**
- **Switch off the video part with VTR SW**

SIF

- **Excellent limitter characteristics**
- **Excellent attenuator characteristics**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Terminal 11 Open Voltage	V_{11}	15	V
Video DC Output Current	I_{15}	6	mA
Audio DC Output Current	I_3	3	mA
Terminal 2 Voltage	V_2	15	V
Power Dissipation (Note)	P_d	1.6	W
Operating Temperature	T_{opr}	−20 ~ 65	°C
Storage Temperature	T_{stg}	−55 ~ 150	°C

Note: Derated above T_a =25°C in the proportion of 12.8 mW/°C.

ELECTRICAL CHARACTERISTICS
PIF Section (T_a=25°C, V_{CC}=12V f_p=45.75MHz, f_s=41.25MHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Recommended Supply Voltage	V_{CC}	—	10.8	12.0	13.2	V	—
Supply Current	I_{CC}	—	50	72	95	mA	1
Video DC Output Voltage	V_{12}	SW_1: 1 SW_2: 2	5.2	5.5	5.8	V	1
AFT DC Output Voltage	V_{13}	SW_1: 1 SW_2: 2	5.3	6.8	8.3	V	1
	V_14	SW_1: 1 SW_2: 2	5.3	6.8	8.3	V	1
AFT DC Offset Voltage	ΔV_{13-14}	SW: 1 SW: 2	−1.5	0	1.5	V	1
RF AGC Residual Output Voltage	V_{11} (Sat)	SW_1: 1 SW_2: 2	—	—	0.5	V	1
RF AGC Leak Current	I_{11} Leak	SW_1: 2 SW_2: 1	—	—	1	uA	1
Video Sensitivity	υ_I Pin 7-8	(Note 1)	60	150	250	uV_{rms}	2
AGC Range	ΔA_{VIF}	(Note 2)	60	64	—	dB	2
SYNC TIP Level Voltage	V_{SYNC} (V_{15})	(Note 3)	2.3	2.5	2.7	V	2
Max. IF Input Voltage	υ_{IN} Max PIF	(Note 4)	100	120	—	mV_{rms}	2
White Noise Threshold Level	V_{WTH} (V_{15})	(Note 5)	5.8	6.2	6.6	V	2
White Noise Clamp Level	V_{WCL} (V_{15})	(Note 5)	3.7	4.1	4.5	V	2

ELECTRICAL CHARACTERISTICS
PIF Section (T_a =25°C, V_{CC} =12V, f_p =45.75MHz, f_s =41.25MHz)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Black Noise Clamp Level		V_{BTH} (V_{15})	(Note 5)	1.4	1.6	1.8	V	2
Black Noise Clamp Level		V_{BCL} (V_{15})	(Note 5)	2.9	3.3	3.7	V	2
Video Frequency Response		f_{BW}	(Note 6)	4.5	5.5	—	MHz	3
Suppression of Carrier		CL	(Note 7)	40	50	—	dB	4
Suppression of 2nd Carrier		I_{2nd}	(Note 8)	40	50	—	dB	4
920KHz Beat Level		I_{920}	(Note 9)	33	38	—	dB	4
Differential Phase		DP	(Note 10)	—	3.5	5	deg	5
Differential Gain		DG	(Note 10)	—	7	10	%	5
VIF Input Impedance		R_{IN} (VIF)	(Note 11)	1.5	3.0	6.0	KΩ	6
		C_{IN} (VIF)		—	3.0	10.0	pF	
AFT Sensitivity		$\Delta F/V_{13-14}$	(Note 12)	—	16	—	kHz/V	2
AFT Output Voltage	Upper	V_{13U} V_{14U}	(Note 13)	11.7	11.9	12.0	V	2
	Lower	V_{13L} V_{14L}	(Note 13)	1.8	2.3	2.8	V	2
RF AGC Max Available Current		I_4 Max	SW_1: 1 SW_2: 1	0.3	—	—	mA	1
RF AGC Delay Setting Range		V_{IN} Delay	(Note 14)	5	7	9	V	
AFT Band Width		ΔF_W	(Note 13)	1.4	—	—	MHz	2
Video Output Voltage		v_{OUT}	(Note 15)	2.25	2.50	2.75	V	2

ELECTRICAL CHARACTERISTICS
SIF Section (T_a=25°C, V_{CC}=12V, f_p=45.75MHz, f_s=41.25MHz)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
SIF Output Voltage		S_{OUT}	(Note 16)	200	400	600	mV_{rms}	3
Input Limitting Voltage		$v_{IN\,(LIM)}$	(Note 17) $R_D = \infty$	—	200	400	uV_{rms}	8
AM Rejection Ratio		AMR	SIF IN: f=4.5 MHz fm=400Hz, Δf=±25kHz AM 30%, V_{IN}=100dBu	40	45	—	dB	8
Recovered Output Voltage		V_{OD}	SIF IN: f=4.5MHz fm=400Hz, Δf=±25kHz V_{IN}=80dBu, R_D=12kΩ	0.5	0.75	—	V_{rms}	8
Total Harmonic Distortion		THD_{DET}	SIF IN: f=4.5MHz fm=400Hz, Δf=±25kHz V_{IN}=80dBu	—	1.0	—	%	8
Max. Audio Output Voltage		V_{OM}	SIF IN: f=4.4—4.6MHz	4.0	—	—	V_{p-p}	8
SIF Input Impedance		$R_{IN\,(SIF)}$	f=4.5MHz	10	20	30	KΩ	7
		$C_{IN\,(SIF)}$		—	3	—	pF	
DET Output Impedance		R_O (DET)	(Note 18)	10	15	20	KΩ	9
DC Voltage	Terminal 21	V_{21}	SW_1: 1 SW_2: 2	4.8	6.0	7.2	V	1
	Terminal 23	V_{23}		3.5	4.4	5.3	V	
	Terminal 1	V_1		6.0	6.7	7.4	V	
Max. Attenuation		ATT Max	(Note 19)	60	—	—	dB	10
DC Volume Gain		G_{ATT} Min	R_A=0 G_{ATT} Min=20log $\frac{v_2}{v_{23}}$	4	6	8	dB	10
ATT Characteristics	1	V_1 (1)	*a	3.4	3.8	4.2	V	10
	2	V_1 (2)	**b	4.5	4.9	5.3	V	10
Signal Leakage		V_{PT}	(Note 20)	—	1.0	3.0	mV_{rms}	11
AF AMP. Gain		V_V AF	(Note 21)	—	20	—	dB	13
AF AMP. Distortion		THD AF	P_{23A}=1V_{pp}, 400Hz SW_3: On ATT: −26dB Setting	—	1.5	—	%	12
AF AMP. Max. Output Voltage		v_{OAF} Max	(Note 21) THD_{AF} 5%	1.5	2.0	—	V_{rms}	13
AF Output DC Voltage		V_3	SW_1: 1 SW_2: 2	6.7	7.7	8.8	V	1

*a Read the 400Hz component of V_{AI} at P_2 with R_A=0, set R_A so that $V_{AI'}$=1/2 V_{AI} (−6dB), then read DC voltage of terminal 1 (V_1).

**b Read the 400Hz component of V_{AI} at P_2 with R_A=0. Set R_A so that $V_{AI'}$=3.16×10^{-3} V_{AI} (−50dB) then read DC voltage of terminal 1 (V1).

TEST CIRCUIT

1. DC Characteristic

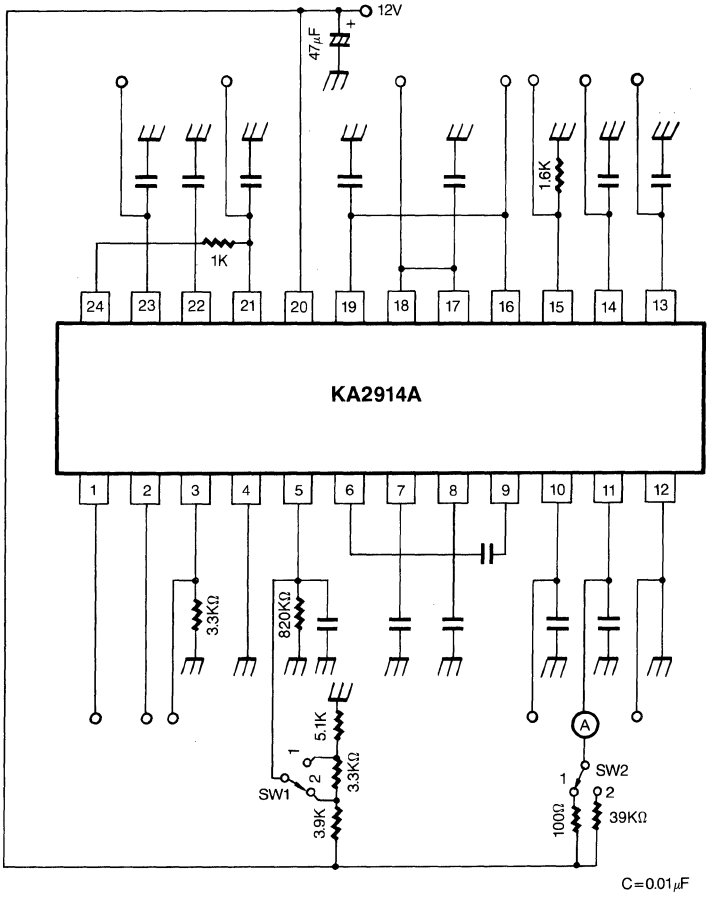


Fig. 1

2. AC Characteristic

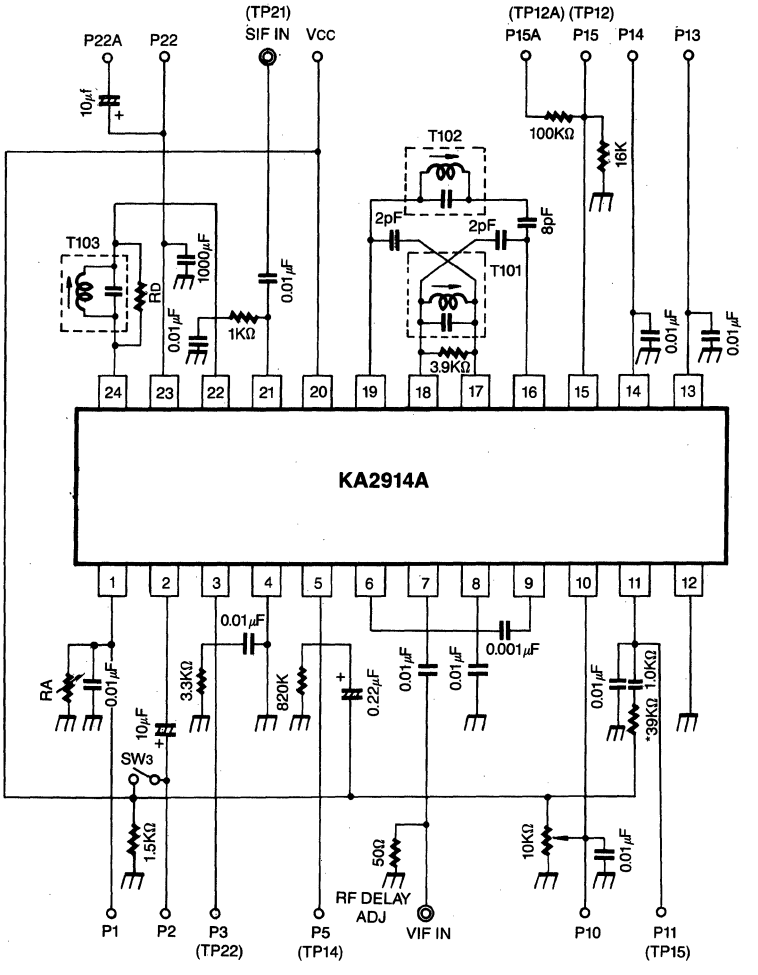


Fig. 2

3. Video Frequency Response and SIF Output Voltage

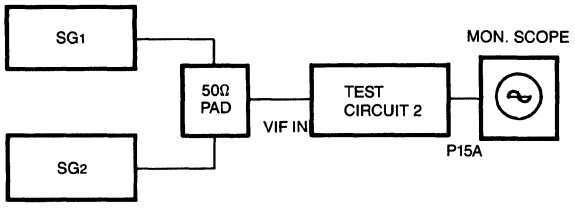


Fig. 3

4. Inter Modulation

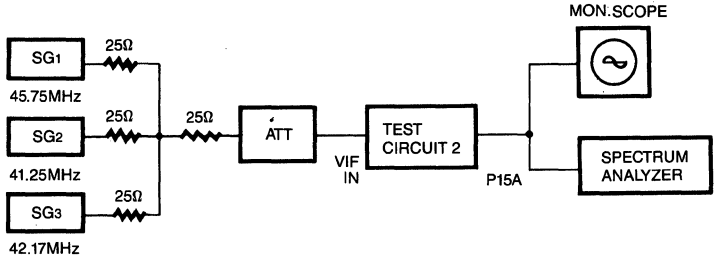
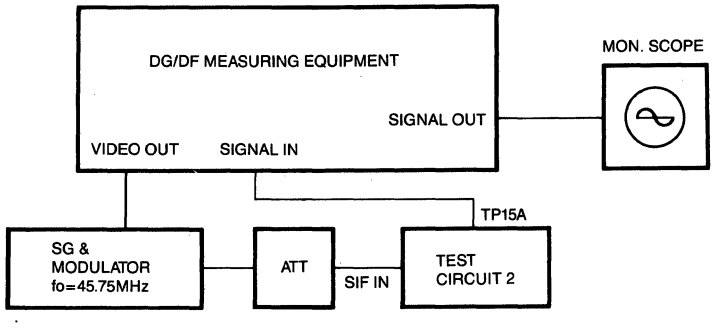


Fig. 4

5. DC, DP



APL=50%
ATT: ADJUST SYNC TIP LEVEL TO DC 25V

Fig. 5

6. VIF Input Impedance

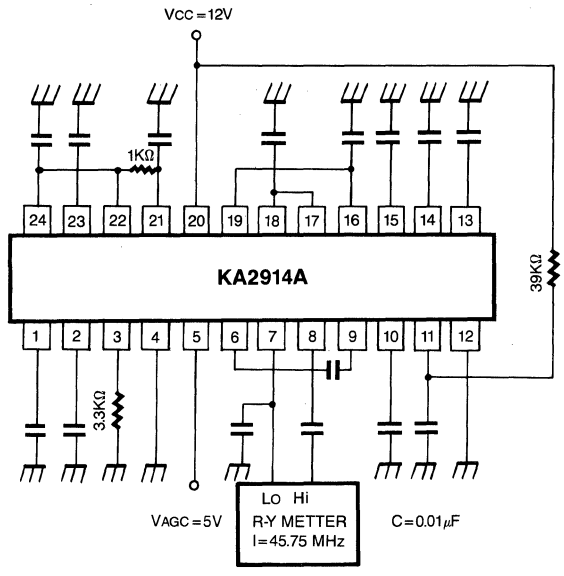


Fig. 6

7. SIF Input Impedance

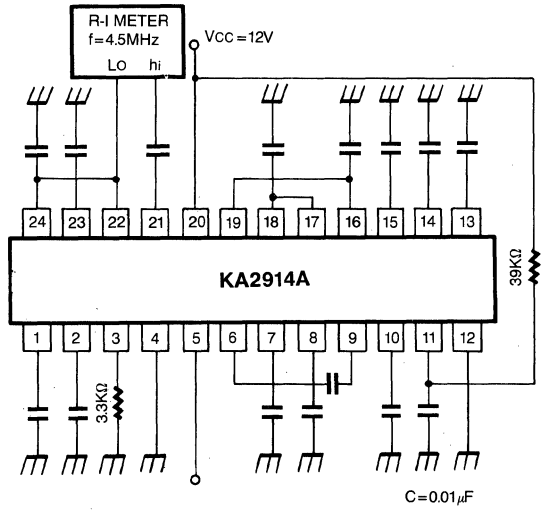


Fig. 7

8. $V_{IN\ (LIM)}$, AMR, V_{OD}, THD, V_{OM}

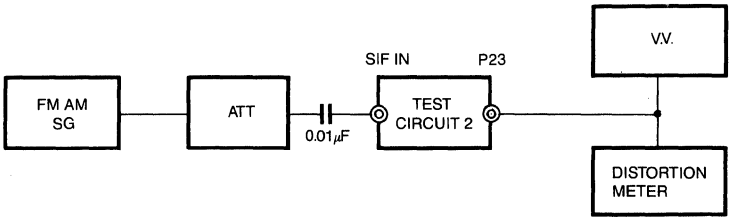


Fig. 8

9. Audio Output Impedance

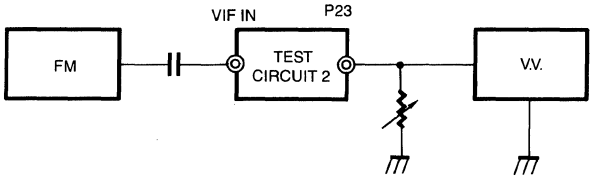


Fig. 9

10. ATT MAX., ATT MIN, $V_{1\ (1)}$, $V_{1\ (2)}$

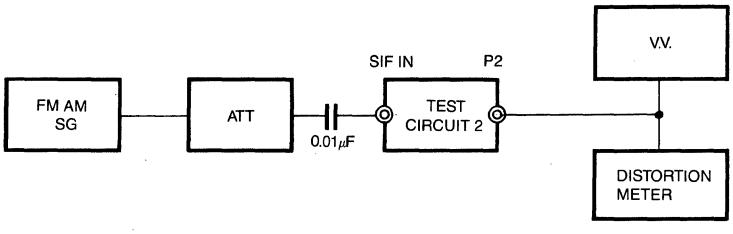


Fig. 10

11. v_{PT}

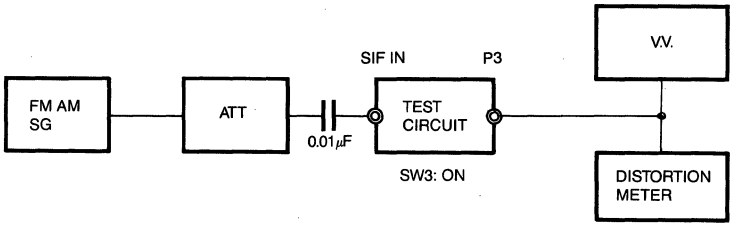


Fig. 11

12. THD_{AF}

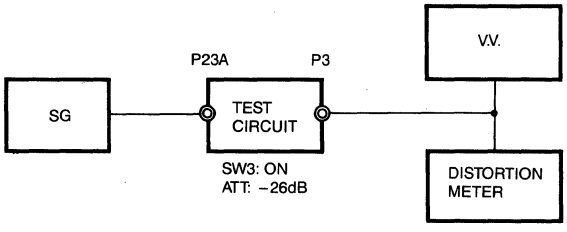


Fig. 12

13. G_V AF, v_{OAF} MAX

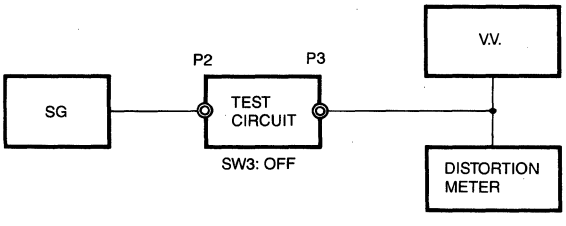


Fig. 13

TEST CONDITION

Note 1) V_{AGC} (P5 EXT. Applying voltage)=11.5V
VIF in: f=45.75MHz 1kHz 30% AM modulation
Adjust VIF input level V_I so that the detected output of P15A with high impedance probe will be $0.8V_{P\text{-}P}$ and measure the input level.

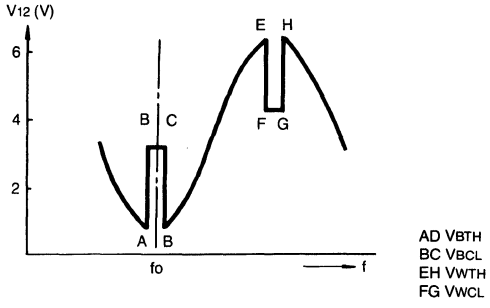
Note 2) V_{AGC}=4V
Measure VIF input level υ_i same as note 1

$$\Delta A = 20 \log \frac{V_I}{V_I} (dB)$$

Note 3) VIF IN: f=45.75MHz CW 15mVrms
Measure DC level of P15

Note 4) VIF IN: f=45.75MHZ APL 100%, 87.5% AM modulation.
P5: open
(1) Adjust VIF input level $50mV_{P\text{-}P}$ and measure the detected output level $0.1V_{P\text{-}P}$
(2) Then increase the input level so that the detected output level will be $1.1\times \upsilon_O 1V_{p\text{-}p}$ and measure the input level.

Note 5) V_{AGC}=8V
VIF in: f=45.75MHz±10MHz variable or sweep 15mVrms measure DC level of P15.



Note 6) V_{AGC}=8 (GR≈30dB)
SG_1: 45.75MHz CW
SG_2: 45.75~40MHz variable
(1) Setting output of SG_1 so that DC level of P15 will be 4.0V
(2) Setting output of SG_2 (45.75MHz) so that AC level of P15 will be $0.5V_{P\text{-}P}$
(3) Decreasing frequency of SG_2 until AC level of P15 will be $0.35V_{P\text{-}P}$ (−3dB of $0.5V_{P\text{-}P}$) then read f_{SG2}=F
f_{BW}=45.75-F MHz

Note 7) SG_1: 45.75MHz, 1kHz 80% AM modulation 100mVrms
SG_2, SG_3; off
Setting V_{AGC} so that output AC level of P15 will be $2.7V_{P-P}$
Measure CL of P15 after setting to 0% AM of SG_1

$$CL = 20 \log \frac{2.7}{U_{CR}\,(V_{P-P})} \text{ (dB)}$$

Note 8) Measure I_{2nd} of P15 same as note 7

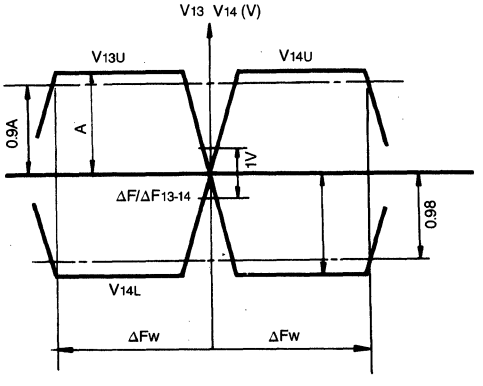
Note 9) V_{AGC} = 8V
SG_1: 45.75MHz (P: picture) 100mVrms
SG_2: 41.25MHz (S: sound) 32mVrms (−10dB of SG_1)
SG_3: 42.17MHz (C: chroma) 32mVrms (−10dB of SG_1)
(1) Setting V_{AGC} so that the output TIP level (lower) of P15 will be 3.0V DC
(2) Measure the level difference (dB) between C-level and 920kHz level

Note 10) V_{AGC} = 8V
VIF IN: f=45.75MHz video signal (RAMP) 87.5% AM $100mV_{p-p}$
Setting ATT so that the SYNC TIP level of P15 will be 2.5V DC measure DP and DG.

Note 11) V_{AGC} = 5V f=45.75MHz
Measure R_{IN} C_{IN}

Note 12) AFT sensitivity $\Delta F/\Delta (V_{13}\text{-}V_{14})$
(1) INT, AGC (P5 open)
(2) VIF input: 45.75MHz ± 1.0MHz, CW 15mVrms
(3) Read the frequency (f_1) of VIF when $V_{13}\text{-}V_{14} = -1V$
(4) Read the frequency (f_2) of VIF when $V_{13}\text{-}V_{14} = 1V$ then caluculate
$\Delta F/\Delta (V_{13}\text{-}V_{14}) = |f_1\text{-}f_2|$

Note 13) ΔF_W, V_{13U}, V_{13L}, V_{14L}, V_{14U}
(1) INT AGC (P5 open)
(2) VIF IN: 45.75MHz ± 10mHz CW 15mVrms
(3) 8_{PF} at PIN 16 should be shorted
(4) Read the frequency (f_1 or f_2) when the V_5 or V_6 reduced to 90% level of A or B with varying the frequency. Then band width is the difference from center frequency (f_0).



Note 14) P5: Open
VIF IN: 45.75MHz CW 20mVrms
(1) Adjust the voltage of terminal 3 so that the voltage of terminal 4 will be 6.0V DC
(2) Measure the terminal voltage 3

Note 15) P5: Open
VIF in: 45.75MHz 100% APL 87.5% AM modulation signal amplitude 50mV$_{P\text{-}p}$ measure detected output voltage (white peak to SYNC TIP)

Note 16) P5: Open
SG_1: 45.75MHz CW 100mVrms
SG_2: 41.25MHz CW 25mVrms
Measure SIF (4.5MHz) output voltage at P15

Note 17) SIP IN: f=4.5MHz FM f_{MOD}=400Hz Δf= ±25kHz,
(1) Adjust SIF input level 100mV$_{P\text{-}P}$ and measure the detected output level v_{OS}
(2) Then decrease the input level so that the detected output level will be 3dB down of V_{OS} and measure the input level

Note 18) Output impedance
(1) SIF IN: f=4.5MHz f=4.5MHz, f_{MOD}=400Hz, Δf=±25kHz, 80dBμ
(2) At P23 read the V_{01} at R_X=∞, then read the R_X when recovered output become $V_{01/2}$ with varying the R_X. The R_X is the output impedance.

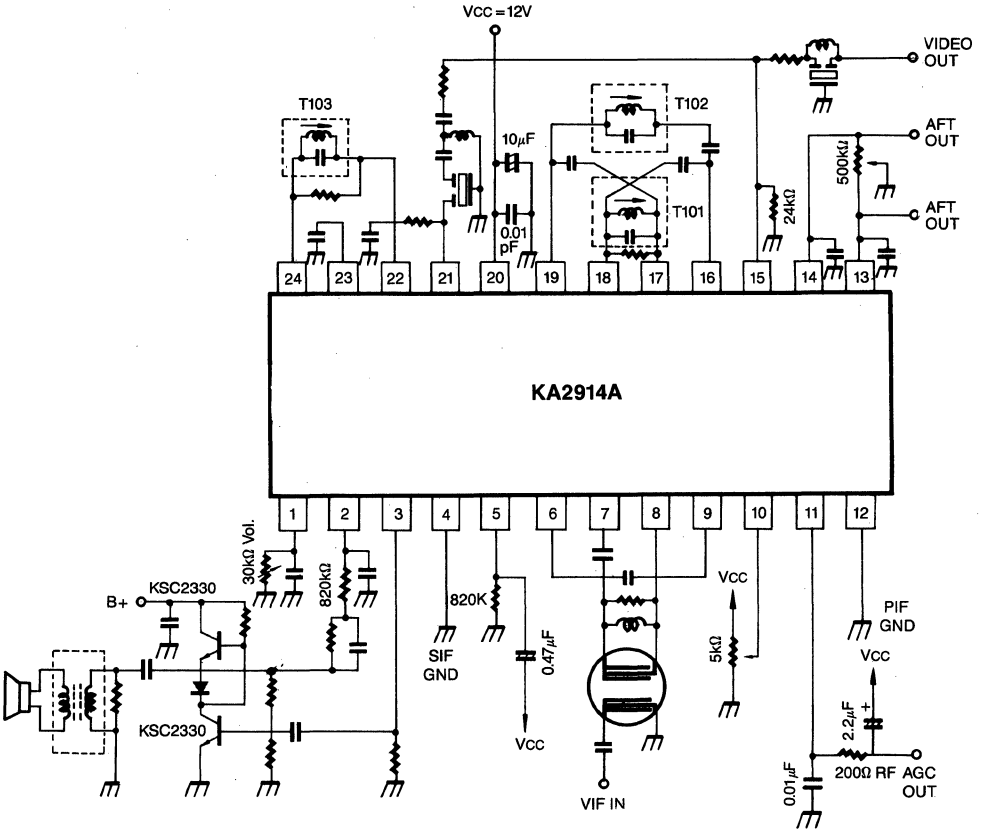
Note 19) ATT max
(1) SIF in: f=4.5MHz, f_{MOD}=400Hz, f=±25kHz, 80dBμ
(2) Read the 400Hz component of V_{AI} at P2 with R_A=0, then read $V_{AI'}$ with R_A= ∞

$$\text{ATT MAX} = 20 \log \frac{V_{A1}}{V_{A1'}}$$

Note 20) v_{PT}
(1) SIF IN: f=4.5MHz f_{MOD}=400Hz, Δf= ±25kHz, 80dBμ
(2) Read the 400Hz component at P3

Note 21) G_V AF
(1) Apply 400Hz 0.1Vrms signal to P2
(2) Read the output voltage at P3

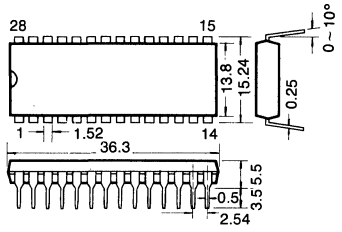
TYPICAL APPLICATION CIRCUIT



ONE CHIP B/W TV (IC FOR TV LARGE INTEGRATION)

The KA2915 is a monolithic integrated circuit containing all stages for the VIF, SIF and DEFLECTION, for television receivers.

28 Dip Unit: mm



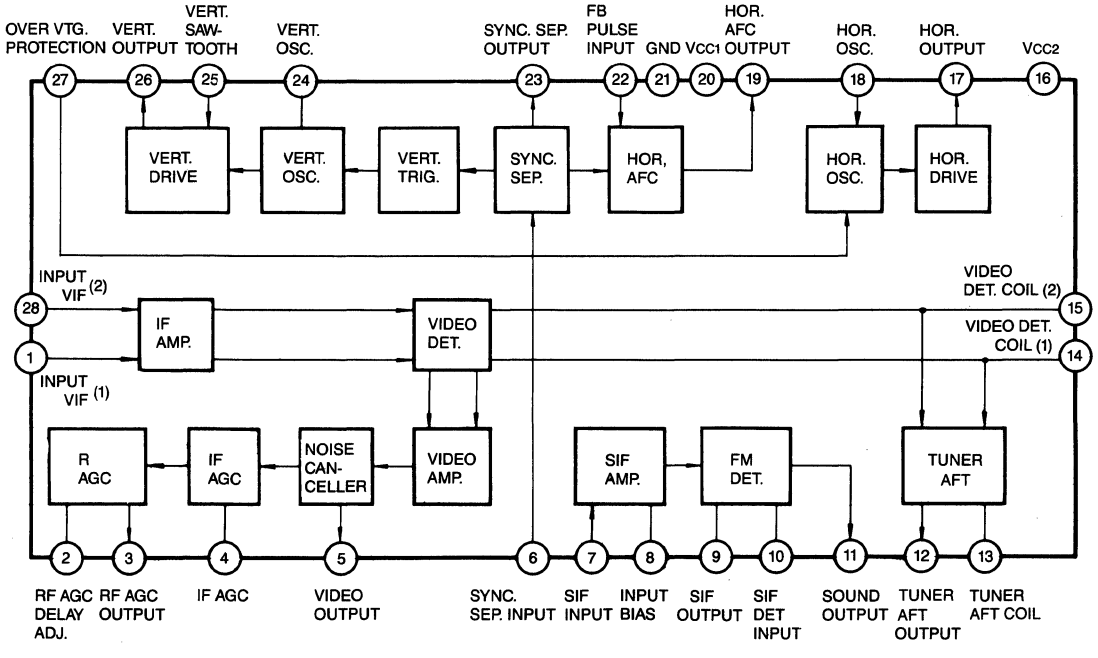
FUNCTIONS

- IF Amp.
- Video Amp.
- IF AGC
- Tuner AFT
- Sound DET. (FM DET.)
- Vertical trig.
- Vertical drive
- Horizontal drive
- Video DET. (AM DET.)
- Noise canceller
- RF AGC
- SIF Amp.
- Sync separation
- Vertical oscillation
- Horizontal oscillation
- Horizontal AFC

FEATURES

- **High integration technology makes possible integration of video if circuit, tuner AFC circuit, sound if circuit and deflection-jungle circuit on a single chip.**
- **Supply voltage range: 8~12V (Typ. 10V).**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value		Unit
Supply Voltage	V_{CC} (V20-21)	12		V
Supply Current	I20	85		mA
	I16	15		mA
Circuit Voltage	V2, 3, 4, 24-21	V20-21	0	V
	V8-21	5.5	0	V
	V13-21	4.2	0	V
	V17-21	V16-21	0	V
Circuit Current	I5, 6, 11, 23, 26	+0.3	−10	mA (peak)
	I19	+0.6	−0.6	mA (peak)
	I25	+10	0	mA (peak)
	I17	+10	−4	mA (peak)
Power Dissipation (T_a=70°C)	Pd	1100		mW
Operating Temperature	Topr	−20 ~ +70		°C
Storage Temperature	Tstg	−55 ~ +150		°C

ELECTRICAL CHARACTERISTICS ($V_{CC}1$=10V, V_{CC}=9.5V, T_a=25°C)

(Video Section)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Video Det. Output	V_O	m=87.5%	1.8	2.1	2.4	V_{p-p}
Input Sensitivity	V_S	V_O=−3dB	–	50	55	dBμ
Maximum Input	V_{MAX}	V_O>+0dB	105	110	—	dB
SN Rating	S/N	V_I=80dBμ	51	56	—	dB
Differential Gain	DG	m=87.5%	—	4	8	%
Differential Phase	DP	m=87.5%	—	3	6	deg
TV Freq. Characteristic	f_C	V_O=−3dB	4.5	6.0	8.0	MHz
Sync. Peak Voltage	V_P		1.9	2.3	2.7	V
Noise Inverter Output Level	V_{NT}		1.0	1.4	1.8	V
Noise Inverter Capture Level	V_{NI}		3.0	3.4	3.8	V
Sound IF Output	V_{SIF}	P/S=20dB	100	104	107	dBμ
Input Resistor	Ri1	f=45.75MHz	0.8	1.0	1.2	Kohm
Input Capacitor	Ci1	f=45.75MHz	3.0	3.4	3.8	pF
Output Resistor	R_O5	f=500kHz	30	50	150	ohm
RF AGC Gain	G_{RF} AGC	f=10kHz, V_4=5mV	36	42	48	dB
RF AGC Max. Voltage	V_3 (Max.)		8.2	8.8	9.4	V
RF AGC Min. Voltage	V_3 (Min.)		3.6	4.2	4.8	V
AFT Center Voltage	V_2		4.0	5.4	6.0	V

(Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
AFT Deffect SW Operating Voltage	V_{AFC} SW	R_S=10Kohm	0.5	2.6	3.0	V
AFT Maximum Output Voltage	V_{12} (Max.)		8.5	9.6	10.0	V
AFT Minimum Output Voltage	V_2 (Min.)		0	0.7	1.2	V
Selection Sensitivity	μ	R_L=68K//82K	30	50	90	mV/kHz

(Sound Section)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Sound Det. Output	V_O	f_O=4.5MHz, f_M=400Hz $\Delta f=\pm$25kHz, V_i=100mVrms	200	300	440	mVrms
Input Limit Voltage	V_i (lim)	f=4.5MHz, f_M=400Hz $\Delta f=\pm$25kHz	—	280	450	μV/rms
Total Harmonic Distortion	THD	f_O=4.5MHz, f_M=400Hz $\Delta f=\pm$25kHz, V_i=100mVrms		0.6	1.0	%
AM Rejection Ratio	AMR		43	55	—	dB
Input Impedance	R_i7	f=4.5MHz	6	20	100	KΩ
	C_i7		1.3	4.3	7.3	pF
Detector Input Impedance	R_{D9}	f=4.5MHz	2.0	3.0	4.0	KΩ
	C_{D9}		2.1	5.1	8.1	pF
	R_{D10}		50	200	—	KΩ
	C_{D10}		2.9	3.4	3.9	pF

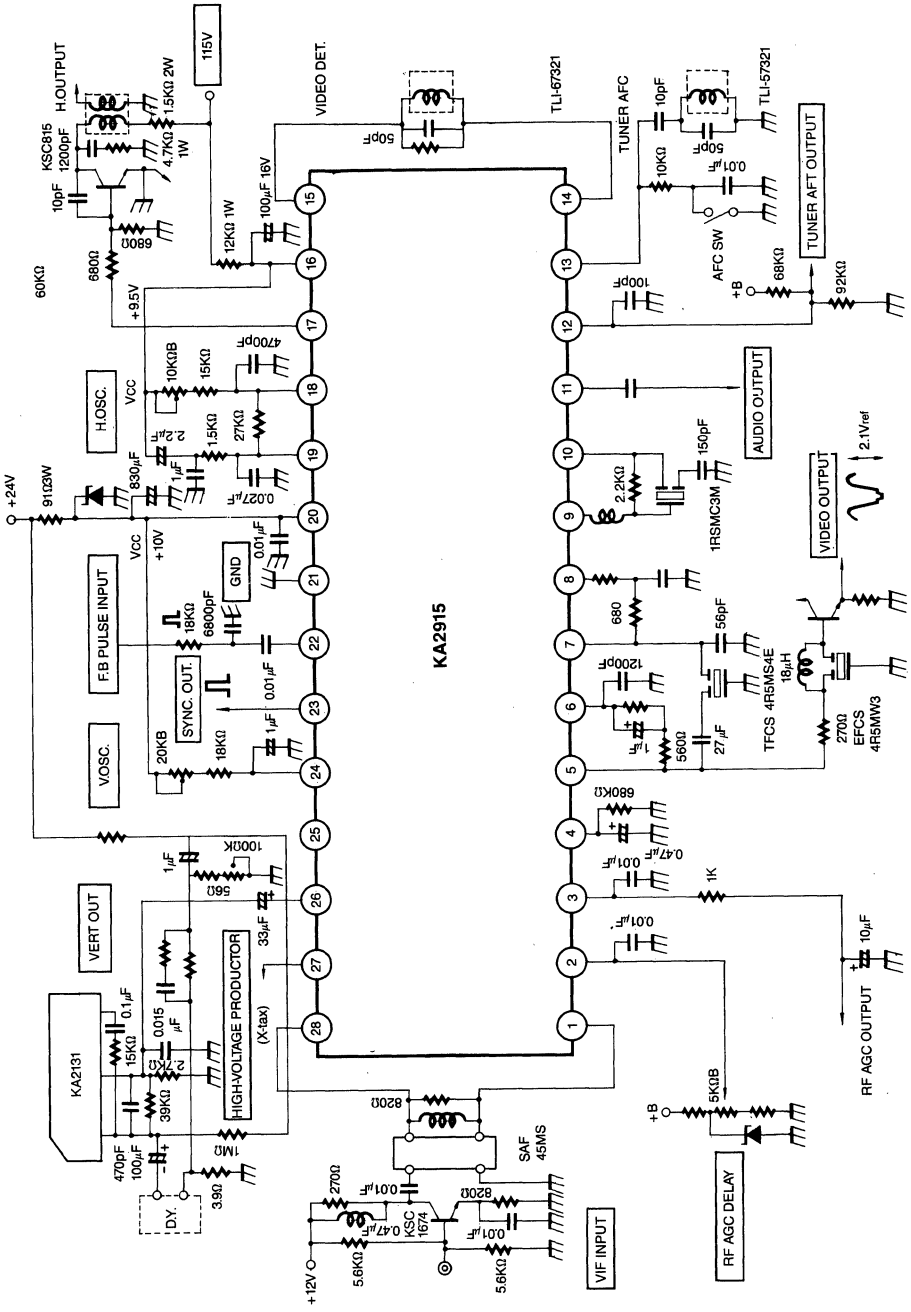
(Deflection Section)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Sync Sep. Hori. Pulse Width (1)	T_{SYNC1}	TV Input 2.5V_{P-P}, APL=50%, V_{CC1}=10V	4.8	5.1	5.4	μs
Sync Sep. Hori. Pulse Width (2)	T_{SYNC2}	TV Input 1.0V_{P-P}, APL=50% V_{CC1}=10V	4.9	5.2	5.5	μs
Hori. AFC Hori. Pulse Width (1)	T_{SYNC3}	TV Input 2.5V_{P-P}, APL=50% V_{CC}1=10V	4.8	5.1	5.4	μs
Hori. AFC Hori. Pulse Width (2)	T_{SYNC4}	TV Input 1.0V_{P-P}, APL=50% V_{CC1}=10V	4.9	5.2	5.5	μs
Vert. OSC. Start Supply Voltage	$V_{FVO.S}$	f_{VO}=50~70Hz Output=0.7V_{P-P}	—	—	6	V
Vert. Free Running Frequency	f_{VO}	$R_{OSC\,(V)}$=31.5KΩ	57	60	63	Hz

(Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Vert. OSC. Pulse Width	T_{VO}	$R_{OSC(V)}$=31.5Kohm	470	650	830	μs
Vert. OSC. Freq. Voltage Dependent	$\Delta f_{VO}/V_{CC}$	V_{CC1}=12V, 8V $\Delta f_{VO}/V_{CC}=f_{VO}$ (12V)-f_{VO} (8V)	0	1.0	1.3	Hz
Vert. Full in Range	f_{PV}	TV Input $2V_{P-P}$	—	44	48	Hz
Hori. OSC. Start Supply Voltage	$V_{FHO.S}$	f_{HO}=10~20kHz Output=$1V_{P-P}$ Pin 16 Voltage	—	—	5	V
Hori. OSC. Freq.	f_{HO}	$R_{OSC(H)}$=21KΩ	15.0	15.75	16.25	kHz
Hori. OSC. Pulse Width	T_{HO}	$R_{OSC(H)}$=21Ω	23	26	29	• μs
Hori. OSC. Freq. Voltage Dependent	f_{HO}/V_{CC}	V_{CC2}=10V, 8V $\Delta f_{HO}/V_{CC}=f_{HO(10V)}$-$f_{HO(8V)}$	0	50	100	Hz
Hori. OSC. Control Sensitivity	ß	ΔI_1 ±100μA Input Variable OSC. Freq. Variable	73	81	89	Hz/μA
Phase Det. Sensitivity	υP	TV Input $2V_{P-P}$, $R_{(U)}$=31.4KΩ, μ=V19×10	13.5	16.5	19.5	μA/μs
X-Ray Protector Operating Voltage	V_{27-21}		0.81	0.87	0.93	V
X-Ray Protector Input Resistor	R_{27}		16	19	22.5	KΩ

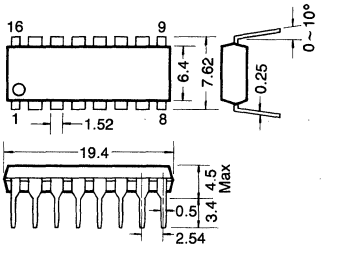
TYPICAL APPLICATION CIRCUIT BLOCK DIAGRAM



C/TV DEFLECTION COMBINATION

The KA2921 is a silicon monolithic integrated circuit disigned for deflection combination in color television receivers.

16 Dip Unit: mm



FUNCTIONS

(HORIZONTAL SECTION)
- Sync separator
- Saw tooth wave type AFC
- $2f_H$ Horizontal Oscillator
- Flip-Flop
- SCR type X-Ray protector
- Horizontal pre driver
- Internal zener diode regulated supply

(VERTICAL SECTION)
- Vertical oscillator
- Vertical sync amplifier
- Ramp wave shaper
- Vertical pre driver

FEATURES

HORIZONTAL SECTION
- **Excellent temperature stability of oscillator frequency**
- **Exact 50% duty cycle output due to 31.5KHz oscillator and flip flop**

VERTICAL SECTION
- **Excxellent interace**

BLOCK DIAGRAM

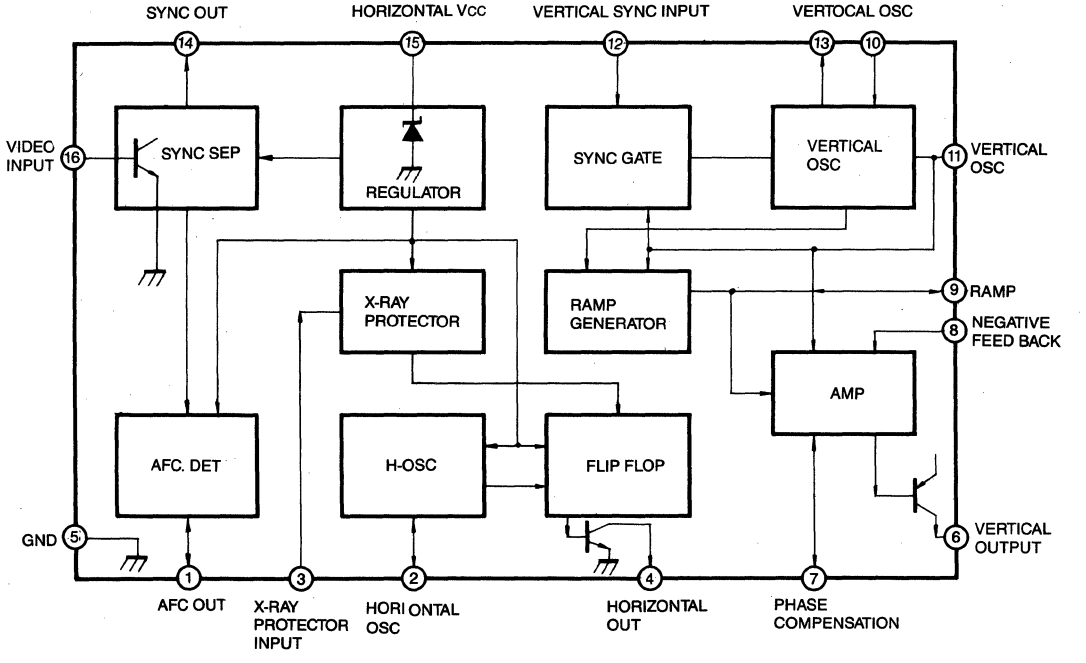


Fig. 2

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Horizontal Supply Current	I_{CC} (Pin 5)	40	mA
Horizontal Output Current	I_o (Pin 4)	60	mA
Horizontal Output Operating Current	I_o opr (Pin 4)	30	mA
Composite Signal Input Voltage	BV (Pin 16)	5	V_{p-p}
AFC Input Voltage	BV (Pin 1)	8	V_{p-p}
Vertical Supply Voltage	$V_{CC\ 11}$	15	V
Vertical Sync Input Voltage	BV_{12}	5	V_{p-p}
Vertical Output Current	I_{o7}	−5	mA
Power Dissipation (Note)	P_d	800	mW
Operating Temperature	Topr	−20 ~ +65	°C
Storage Temperature	Tstg	−55 ~ +150	°C

Note: Derated above T_a=25°C in the proportion of 6.4mW/°C

ELECTRICAL CHARACTERISTICS (T_a=25°C) HORIZONTAL STAGE (V_{CC}=19.7V)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Zener Regulating Voltage	V_{CC} (Pin 15)		8.9	9.8	10.9	V	1
Recommended Supply Current	I_{CC} (Pin 15)		20	25	30	mA	1
Sync Sep. Sensitivity	I_{IN} (Pin 16)		—	13	56	μA	3
Sync Tip Output Voltage	V_{OH} (Pin 14)		7.4	8.3	9.0	V	3
Sync Bottom Output Voltage	V_{OL} (Pin 14)		—	0.2	0.5	V	3
Sync Sep Delay Time (1)	t_{pdr}		—	—	100	nsec	4
Sync Sep Delay Time (2)	t_{pdf}		—	—	100	nsec	4
H-Free Run Frequency	f_H		15234	15734	16234	Hz	5
AFC Output Current	I_o (Pin 1)		2.15	3.08	4.42	mA	7

ELECTRICAL CHARACTERISTICS (T_a =25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
AFC Clamp Voltage	V_{CL} (Pin 1)		3.9	4.5	5.1	V	6
Horizontal Output Residual Output Voltage	V_{OL} (Pin 4)		—	0.08	0.3	V	8
Horizontal Output Pulse Width	to (Pin 4)		30.78	31.78	32.78	μsec	8
Sensitivity of Phase Detector	μ		—	0.16	—	V/sec	9
Sensitivity of Oscillator	β		—	1170	—	Hz/V	9
Frequency Pull-In Range	Δf_{PLL}		—	±600	—	Hz	9
Frequency Hold-In Range	Δf_{HOLD}			±1000		Hz	9
X-Ray Protector Sensitivity	V_{in} (Pin 3)		0.77	0.91	1.04	V	10
X-Ray Protector Input Impedance	R_{in} (Pin 3)		0.2	—	—	MΩ	—
Characteristic of Horizontal Free Run Frequency	Δf_{HT}	−20°C~60°C	0	−100	−350	Hz	5
Horizontal 8V Supply Current	I_{15} (Pin 15)		8.4	12.5	16	mA	2

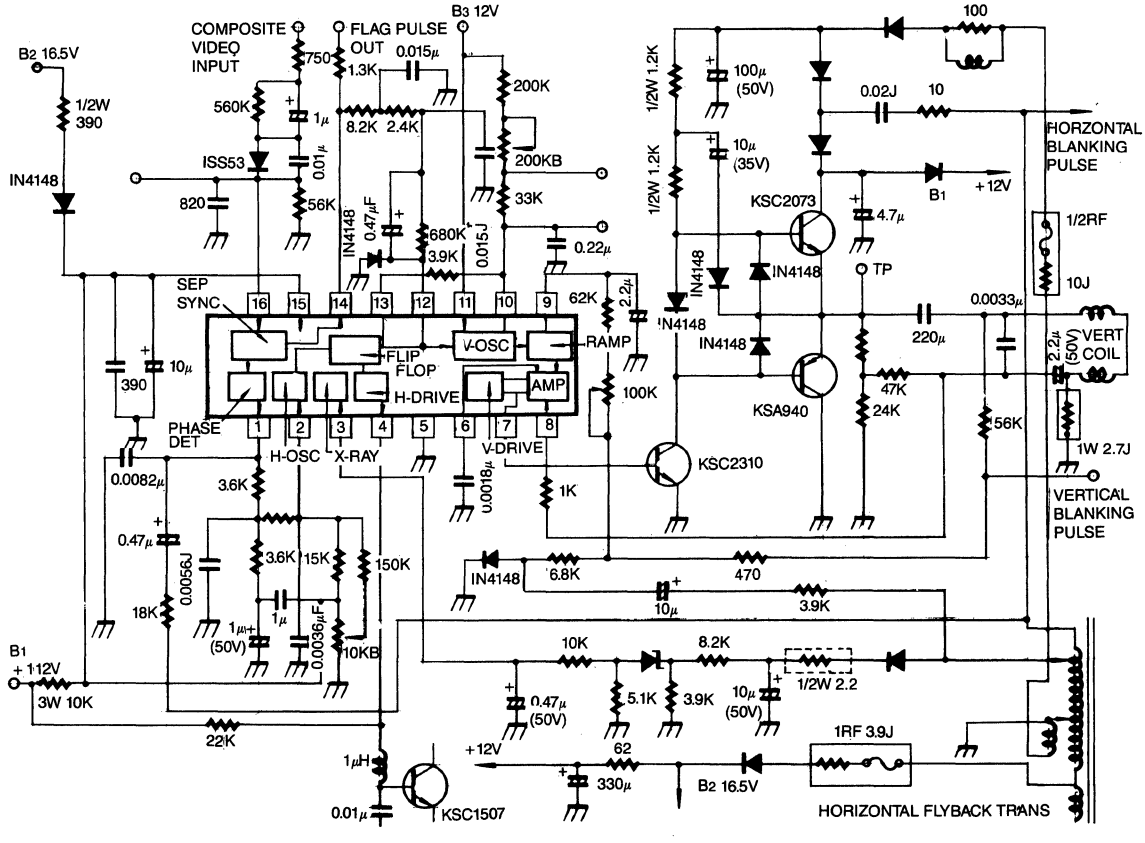
VERTICAL STAGE (V_{CC} =12V)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Recommended Supply Voltage	V_{CC}		10.8	12	13.2	V	—
Supply Current	I_{CC}		3.4	4.4	6.1	mA	11
Vertical Frequency	f_v		57.0	60.0	64.1	Hz	12
Vertical Pulse Width	t_r		847	891	933	μsec	13
Vertical Frequency Pull-In Range	Δf_{VPULL}		11.65	12.14	12.68	Hz	14
Vertical Sync Input Impendance	R_{in} (Pin 12)		400	500	600	Ω	—
Vertical Sync Operating Voltage	V_{in} (Pin 12)		0.64	0.72	0.80	V	15
Pin 9 (max) Output Voltage	V_o (Pin 9)		7.6	8.1	8.6	V	16
Pin 9 Output Current	I_o (Pin 9)		12.0	18.2	35.7	mA	17

VERTICAL STAGE (V_{CC}=12V)

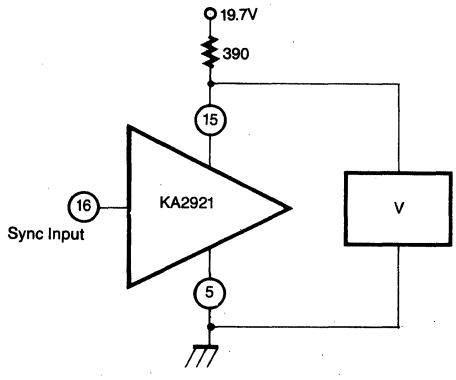
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Pin 8 Available Maximum Voltage	V_L (Pin 8)		—	2.86	3.7	V	18
Pin 9 Input Current	$I_{9\ LEAK}$ (Pin 9)		0.25	0.98	4.50	μA	19
Pin 8 Input Current	$I_{8\ LEAK}$ (Pin 8)		0.18	0.94	6.21	μA	20
Vertical Output Maximum Available Voltage	V_{OH} (Pin 7)		5.67	6.30	7.13	V	21
Vertical Output Maximum Voltage	V_{OL} (Pin 7)		—	—	0.3	V	22

TYPICAL APPLICATION CIRCUIT



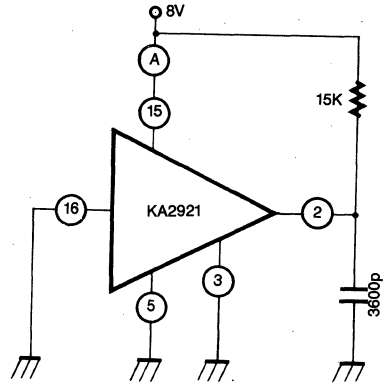
TEST CIRCUIT 1

(Zener Regulating voltage)



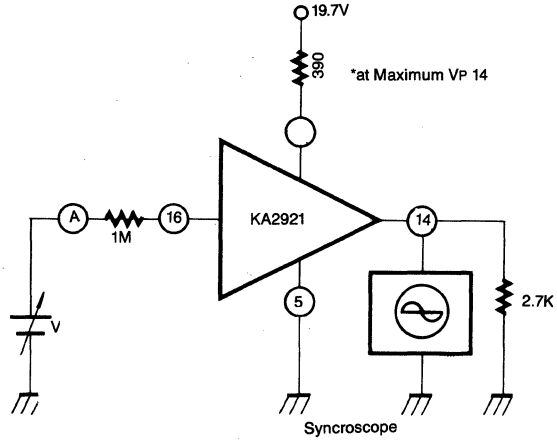
TEST CIRCUIT 2

(8V Supply Current)



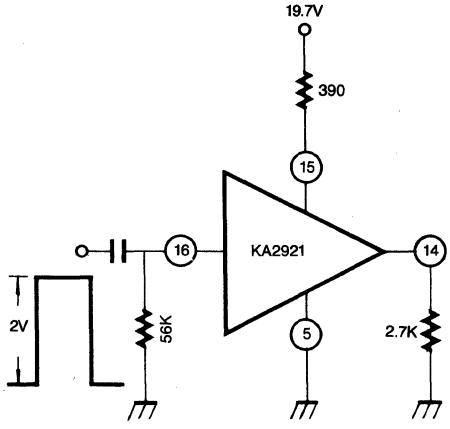
TEST CIRCUIT 3

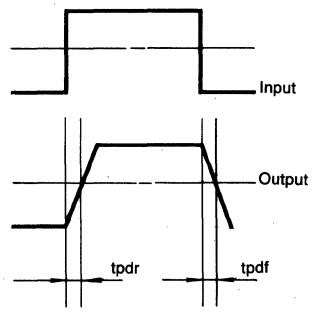
Sync. Sep. Sensitivity
Sync. Tip Output Voltage
Sync. Bottom Output Voltage



TEST CIRCUIT 4

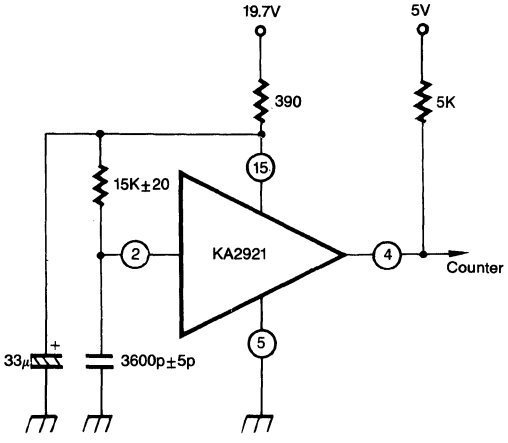
(Sync Sep Delay Time)





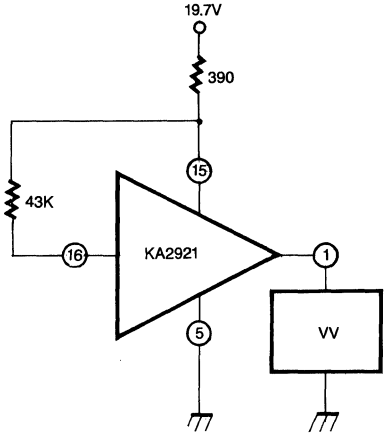
TEST CIRCUIT 5

(Horizontal Free Run Frequency)



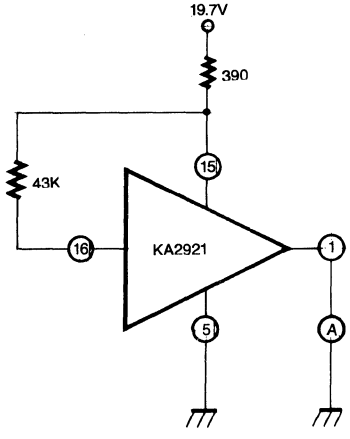
TEST CIRCUIT 6

(AFC Clamp Voltage)



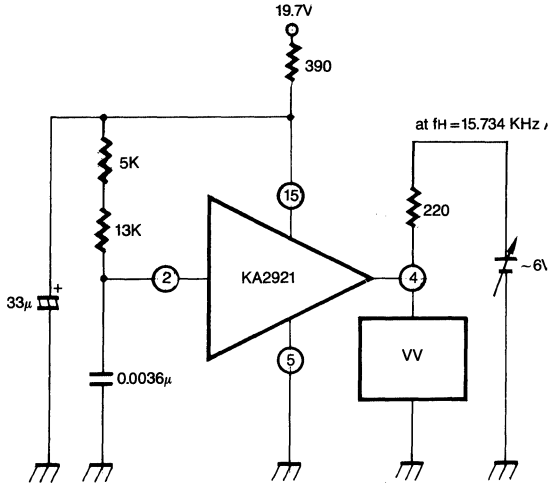
TEST CIRCUIT 7

AFC Output Current



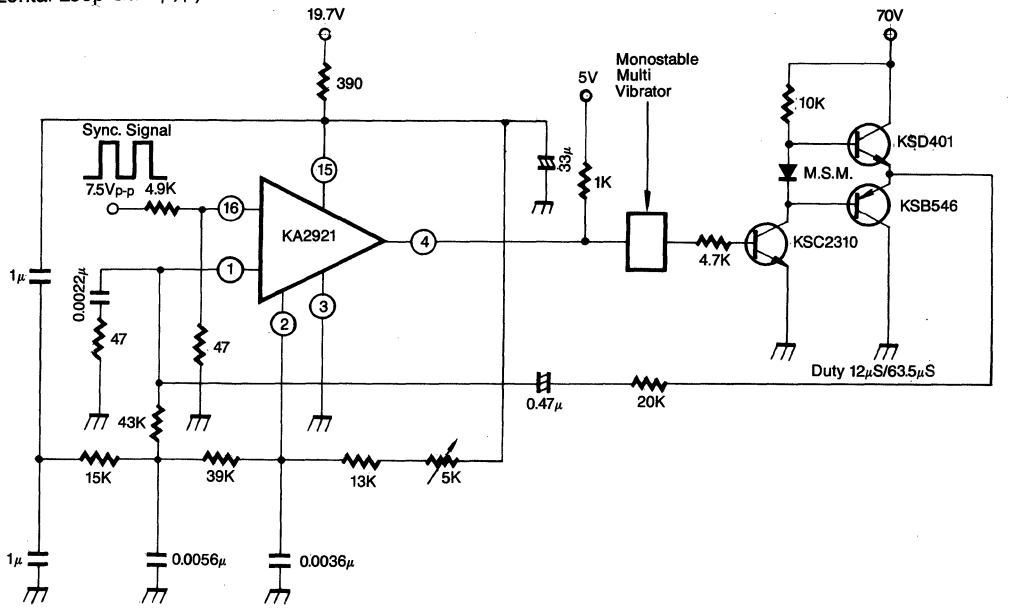
TEST CIRCUIT 8

Horizontal Output Residual Output Voltage
Horizontal Output Pulse Width



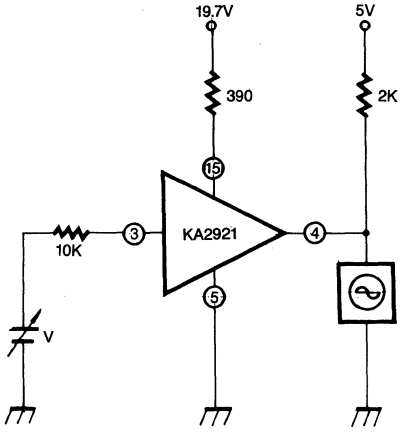
TEST CIRCUIT 9

(Horizontal Loop Gain μ, β)



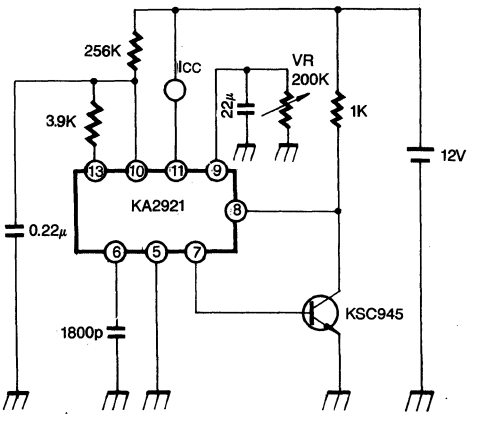
TEST CIRCUIT 10

(X-Ray Protector Sensitivity)



TEST CIRCUIT 11

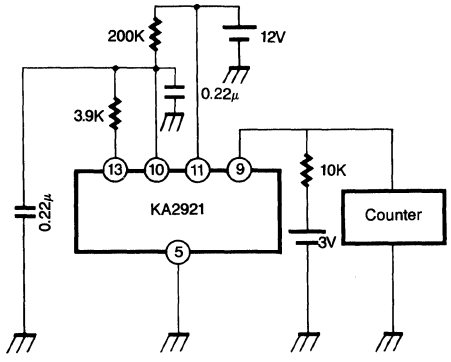
(Vertical Supply Current)



1.5Vp-p (Adjust Vpq) Vpp

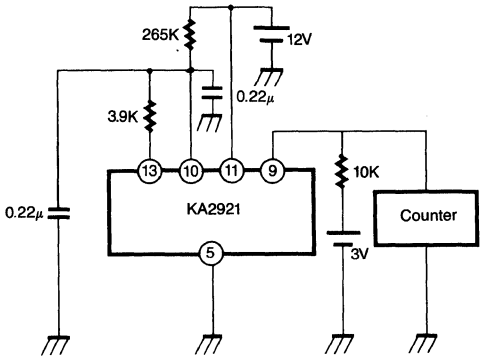
TEST CIRCUIT 12

(Vertical Frequency)



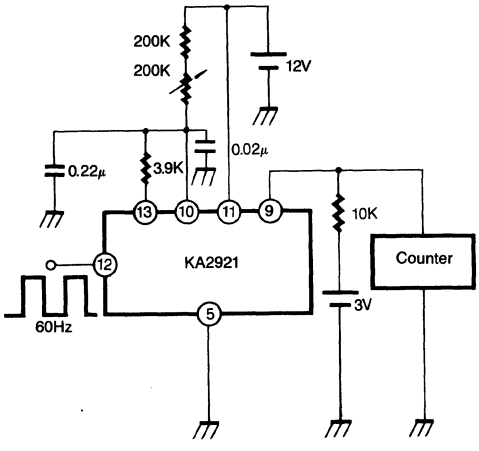
TEST CIRCUIT 13

(Vertical Pulse Width)



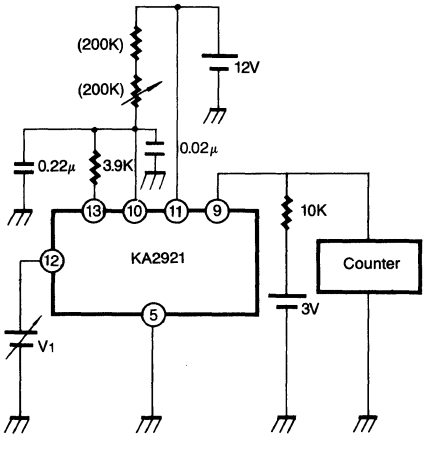
TEST CIRCUIT 14

(Vertical Frequency Pull-In Range)



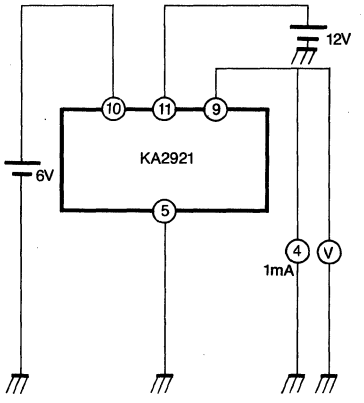
TEST CIRCUIT 15

(Vertical Sync Operating Voltage)



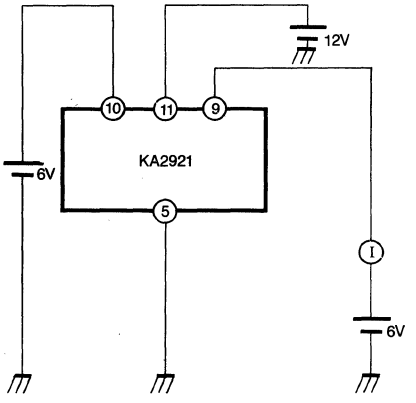
TEST CIRCUIT 16

(Pin 9 (Pin 8) Maximum Output Voltage)



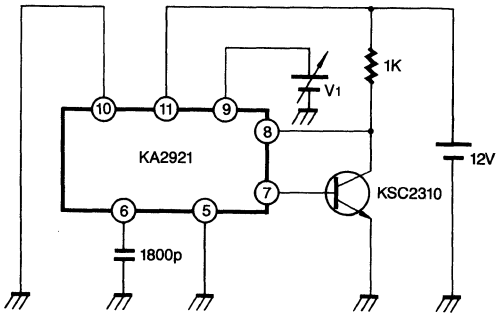
TEST CIRCUIT 17

(Pin 9 Output Current)



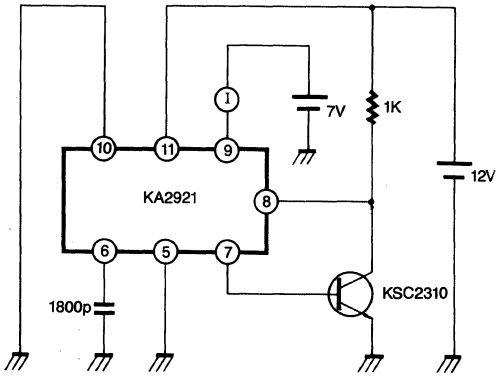
TEST CIRCUIT 18

(Pin 8 Available Minimum Voltage)



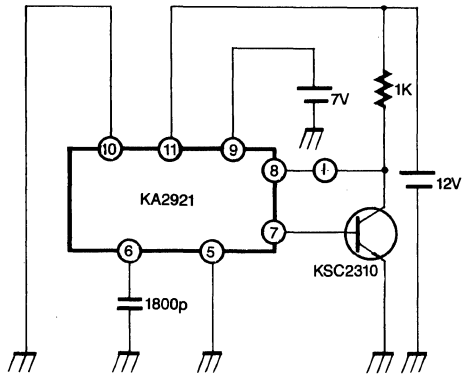
TEST CIRCUIT 19

(Pin 9 Input Current)



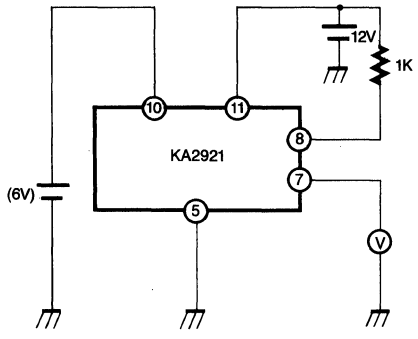
TEST CIRCUIT 20

(Pin 8 Input Current)



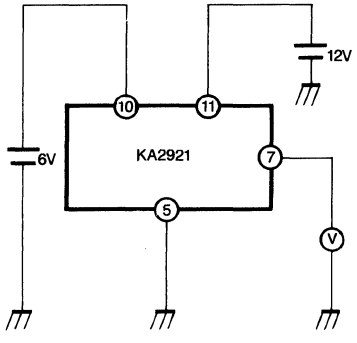
TEST CIRCUIT 21

(Vertical output Maximum Available Voltage)



TEST CIRCUIT 22

(Vertical Output Minimum Voltage)



WRITE AND READ AMPLIFIER

FUNCTION

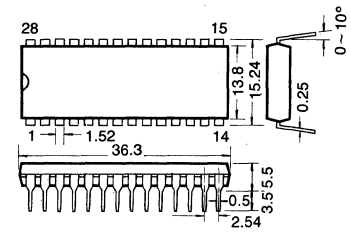
REC Mode

- Sync Tip clamp
- Dynamic emphasis (Nonlinear emphasis)
- Main Pre-Emphasis
- White/Dark clip
- Frequency monitor
- Rec buffer amplifier

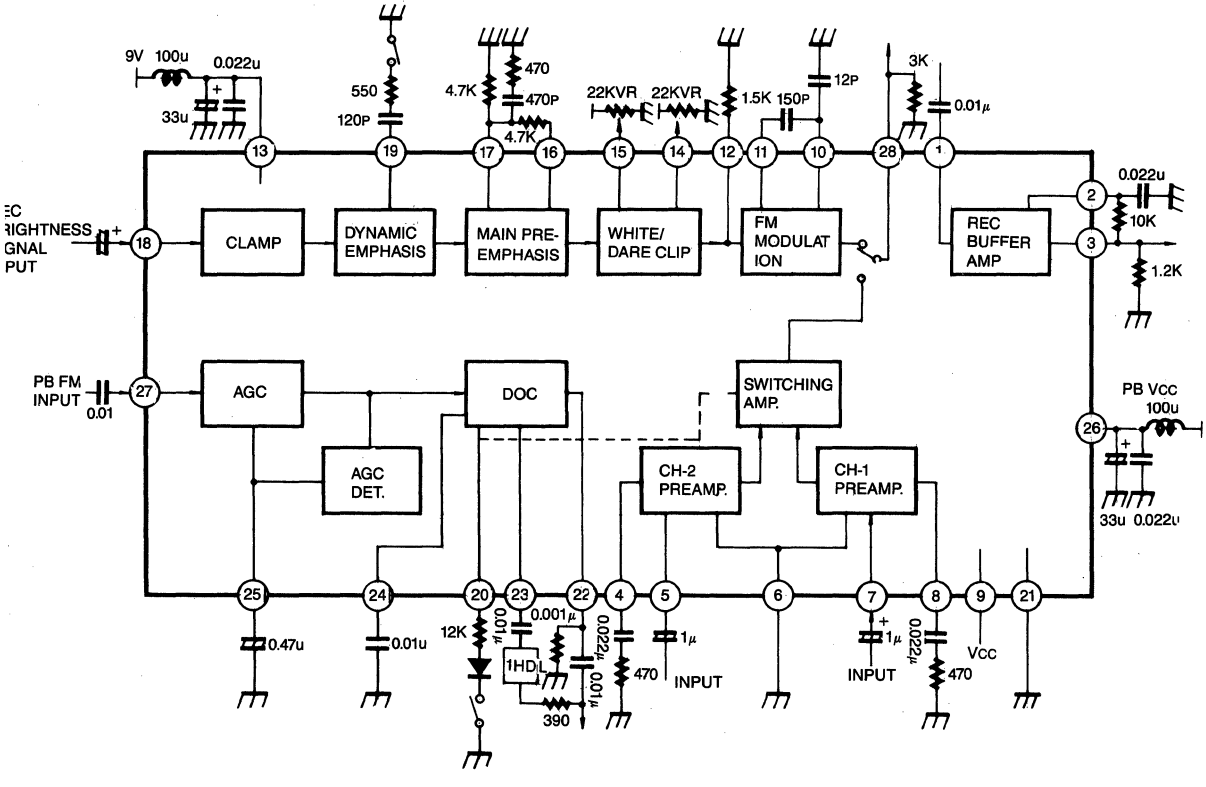
PB Mode

- Switching amplifier
- FM AGC
- DOC (Drop out compensator)

28 Dip Unit: mm



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Operating Voltage	V_{opr}	9±1	V
Power Dissipation	P_d	800* 675**	mW
Operating Temperature	T_{opr}	−10.75	°C
Storage Temperature	T_{stg}	−40~+125	°C

* Value at=65°C ** Value at=75°C

ELECTRICAL CHARACTERISTIC (T_a=25°C)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
PB Mode Supply Current		I_{CC} (PB)	PB Mode V_{CC}=9V inflow current of input 9 and 26	18.0	25.0	33.1	mA
Pre Amp Open Gain	CH1	GP_{01}	Sine wave input (0.53mV_{p-p} 10.6MHz) at pin 7; Output at pin 28	57.8	60.8	62.8	dB
	CH2	GP_{02}	Sine wave input (0.53mV_{p-p} 0.6MHz) at pin 5; Output at pin 28	57.8	60.8	62.8	
Pre Amp Open Gain Balance		ΔGP_O	GP_O1-GP_O2	−0.7	0	0.7	dB
Pre Amp Feeback Gain	CH1	GP_{F1}	Sine wave input (0.53mV_{p-p} 6MHz) at pin 7; Output at pin 28	55.2	58.2	61.2	dB
	CH2	GP_{F2}	Sine wave input (0.53mV_{p-p} 0.6MHz) at pin 5; Output at pin 28	55.2	58.2	61.2	
Pre Amp Open Gain Balance		ΔGP_F	GP_{F1}—GP_{F2}	−0.7	0	0.7	dB
Pre Amp Noise To Signal Ratio	CH1	S/N1	S/N Ratio at pin 28 between sine wave input (0.13mV_{p-p}. 0.6MHz) at pin 5 and zero signal input at pin (Noise BW=1MHz)	33.0	35.0	—	dB
	CH2	S/N2	S/N Ratio at pin 28 between sine Wave input (0.13mV_{p-p}. 0.6MHz) at Pin 7 and zero signal input at pin 7 (Noise BW=1 MHz)	33.0	35.0	—	
Pre Amp Channel Switch Offset Voltage		OS_p	DC Output voltage difference at pin 28 between CH1 ON all and CH2 ON	−1.00	0	1.00	V
Pre Amp Channel Switch Changeover Current		I_{SW}	Sine wave input (0.53mV_{p-p} 0.6MHz) at pin 7; Output at pin 20	90	120	150	μA

ELECTRICAL CHARACTERISTIC (continued)

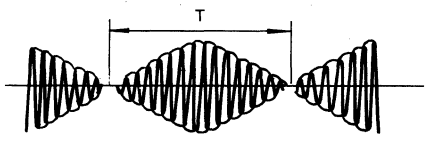
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
AGC Amp Gain	G_A	Sine wave input ($20mV_{p-p}$ 4MHz) at pin 27; Output at pin 22	19.2	20.7	22.2	dB
AGC Detective	V_D	Sine wave input ($0.5V_{p-p}$ 4MHz) at pin 27; DC voltage at pin 25	0.76	0.87	1.00	dB
AGC Control Characteristic	ΔV_{A1}	Pin 22 Output characteristic from $0.5V_{p-p}$ to $1V_{p-p}$ of pin 27 input (4MHz Sine wave)	0.0	0.3	1.0	dB
	ΔV_{A2}	Pin 22 Output characteristic from $0.5V_{p-p}$ to $1V_{p-p}$ of pin 27 input (4MHz Sine wave)	0.0	0.3	1.0	
Drop Output Detection Voltage	L_{DOC}	AM Modulation wave input at pin 27 (Note 1) e1 of pin 22; Output (Note) ($0dB=0.5V_{p-p}$)	−23.5	−20.5	−17.5	dB
Drop Output Recovery Hystersis	L_{HYS}	AM Modulation wave input at pin 27 (Note 1) el and e2 of pin; 22 output (Note 2) ($0\ dB=0.5V_{p-p}$) than e2/e1	3.2	5.7	8.2	dB
Drop Output Detective Pulse Output Voltage	L_{DP}	AM Modulation wave input at pin 27 (Note 1) output pulse (V) at pin 22 (Note 3)	0.6	0.7	0.8	V_{p-p}
DS Amp Gain	G_{DS}	Since wave input ($0.1V_{p-p}$ 4 MHz) at pin 23; Output at pin 22	12.2	13.2	14.2	dB
DS Amp Switch Output Offset	GS_{DS}	Difference between pin 22 DC Output at pin 27 Since wave input (0.5MHz 4 MHz) and pin 22 DC Potential at pin 27 No input signal	−70	0	70	mV
REC Mode Supply Current	I_{CC} (REC)	REC Mode, $V_{CC}=9V$; Inflow current of pin 13	16.5	22.0	27.5	mA
FM Mod Limitter Output Peak to Peak Voltage	V_{LIM}	Zero signal at pin 18 Output at pin 28 (Note 4)	1.0	1.2	1.4	V_{p-p}
REC Amp Gain	G_{RA}	Sine wave input ($0.15V_{p-p}$ 1MHz) at pin 1; Output at pin 3	17.3	19.3	21.3	dB

ELECTRICAL CHARACTERISTIC (continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Dynamic Emphasis Response Characteristic	DEM 1	Sine wave input ($0.7V_{p-p}$ 10KHz) at pin 18; Output at pin 16	−1.6	−1.0	−0.4	dB
	DEM 2	Sine wave input ($0.7V_{p-p}$ 3MHz) at pin 18; Output at pin 16 (DEM 1=0 dB)	1.8	2.8	3.8	
	DEM 3	Sine wave input ($0.22V_{p-p}$ 3 MHz) at pin 18; Output at pin 16 (DEM 1=0 dB)	4.1	5.3	6.5	
	DEM 4	Sine wave input ($0.07V_{p-p}$ 0.5MHz) at pin 18; Output at pin 16 (DEM 1=0 dB)	6.0	7.5	9.0	
Main Emphasis	GME	Sine wave input ($50mV_{p-p}$ 0.5MHz) at pin 18; Output at pin 16	23.5	25.5	27.5	dB
FM MOD Input Signal Voltage	V_{MOD}	Video signal input ($1\ V_{p-p}$) at pin 18 (Note 4) Output at pin 12	0.54	0.58	0.62	dB
White Clip Adjustment Voltage	V_{15A}	Video signal input ($1V_{p-p}$ at pin 18 (Note 4); pin 15 DC Voltage to give the white clip waveform of note 5 at pin 22	7.0	7.3	7.6	V
Dark Clip Adjustment Voltage	V_{14A}	Video signal input ($1V_{p-p}$) at 18 (Note 4) pin 15 DC Voltage to give the dark clip waveform of note 5 at pin 12	4.9	5.2	5.6	V
FM Mod Oscillation Frequency	f_{MOD}	Video input signal ($1V_{p-p}$) at pin 18 (Note 4) Output at pin 28 (by Spectrum analyzer) Oscillation frequency corresponding to sync tip	3.1	3.45	3.8	MHz
FM Mod V.F Conversion Linearity	L_{MOD}	Adjustment carrier set to 3.4MHz and deviation to 1MHz/V pin 28 frequences where pin 18 voltage is 5.2V, 6.2V and 7.2V $\frac{f6.2-(f7.2-f5.2)/2}{f7.2-f5.2} \times 100$	−5	0	5	%
FM Mod Secondary Distortion	H_{MOD}	Adjust pin 14 DC Voltage until pin 28; Output of 4MHz is produced; Ratio of 8MHz component to 4MHz basic wave at pin 28	—	−4.5	—	dB

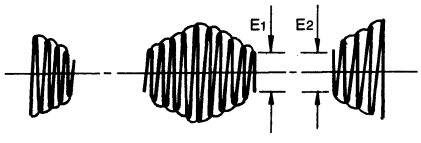
NOTE

1. AM Modulation Wave

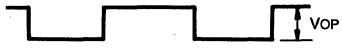


T=0.6mS 0.5V_{p-p} f=04MHz

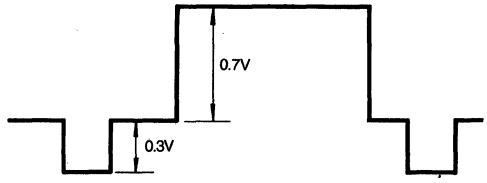
2. el e2



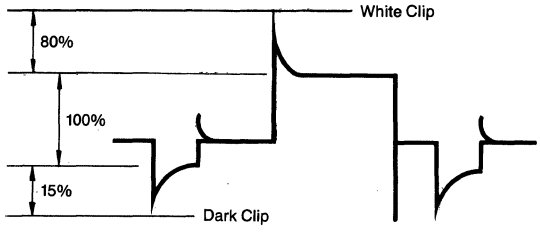
3. V_{DP}



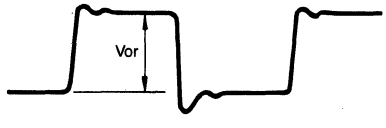
4. Video Signal



5. White Clip, Dark Clip



6. Limitter Output Amplitude



VIDEO SIGNAL PROCESSOR

FUNCTION

- Sync slicer
  Video output amplifier

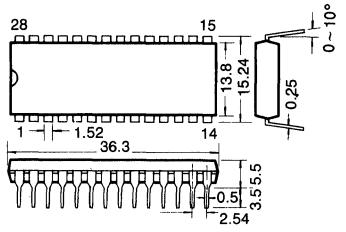
REC Mode

- **Video AGC (Keyed+Peak to Peak DET type)**
- **Monitor squelch for EE**

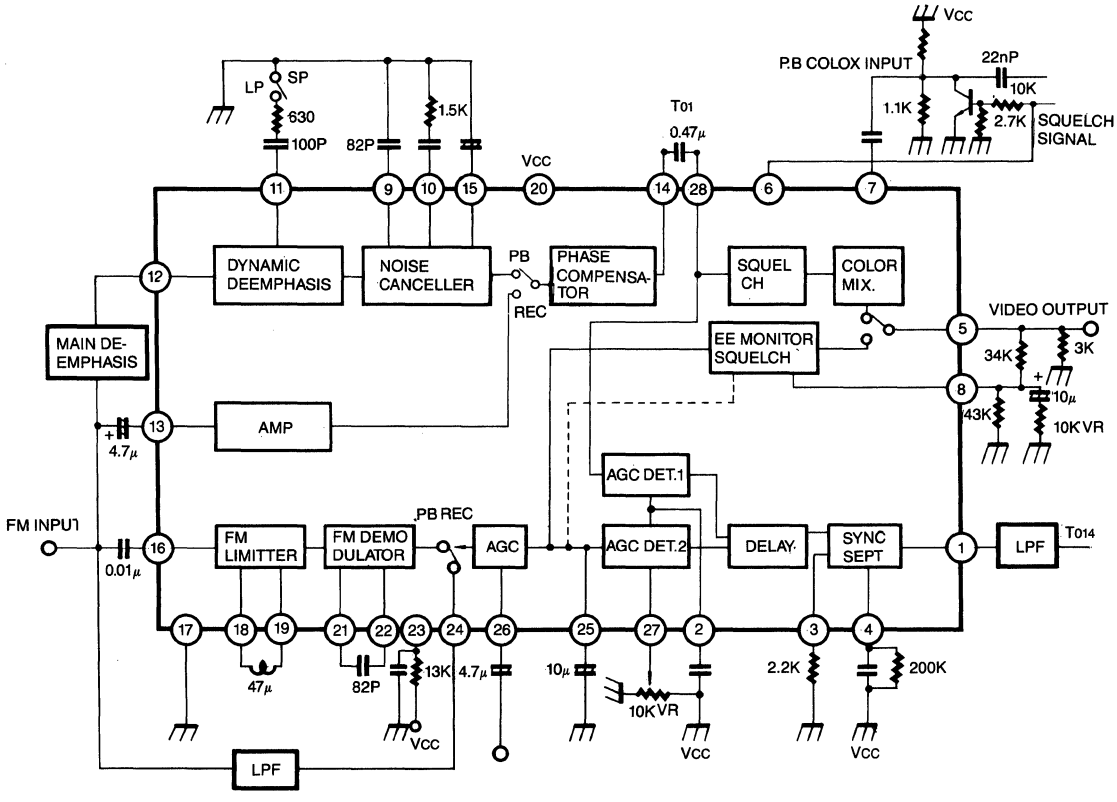
PB Mode

- FM Limitter
- FM Modulator
- Dynamic De-emphasis
- Noise canceller
- Chroma mix amplifier
- White peak clipper

28 Dip **Unit: mm**



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Operating Voltage	V_{opr}	9 ± 1	V
Power Dissipation	P_d	800* / 675**	mW
Operating Temperature	T_{opr}	−10.75	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

* Value at=65°C ** Value at=75°C

ELECTRICAL CHARACTERISTIC (V_{CC} = 9V, T_a = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
PB Mode Supply Current	I_{CC} (PB)	PB Mode V_{CC} = 9V inflow current of pin 20	18.0	25.0	33.1	mA
FM Demoulation Voltage	V_{DEM4}	Sine wave input (4MHz 50mV_{p-p}) at pin 16 DC voltage at pin 24	7.67	7.85	8.03	V
FM Demodulation Sensitivity	S_{DEM}	Sine wave input (3MHz and 5MHz, 50mV_{p-p}) at pin 16 DC voltage at pin 24 (V_{DEM} 3 and V_{DEM} 5 to each frequency) $S_{DEM} = \frac{V_{DEM5} - V_{DEM3}}{2}$	0.34	0.28	0.33	V
FM Demodulation Linearity	S_{DEM}	Sine wave inputs (3MHz 4MHz and 5MHz. 50mV_{p-p}) at pin 16 DC voltage at pin 24 $L_{DEM} = 100 \times \frac{V_{DEM4} - (V_{DEM5} - V_{DEM3})/2}{V_{DEM5} - V_{DEM3}}$	0.24	0.28	0.33	%
Carrier Leakage	C.L	Sine wave input (4MHz 0.5V_{p-p}) at pin 16 4MHz Component at pin 24 (0dB = 0.7 × S_{DEM})	—	−24	−20	V
DD. NC Main Amp Gain (Note 1)	G_{DN}	Sine wave input (0.5MHz 1V_{p-p}) at pin 12; Output at pin 14	−0.7	0	+0.7	dB
DD Limitter Gain	G_{DD}	Sine wave input (0.5MHz 10mV_{p-p}) at pin 11; Output at pin 9	—	−1	—	dB

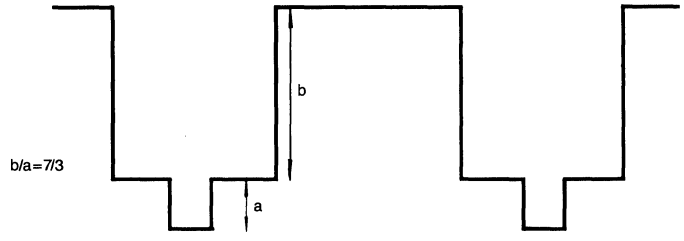
ELECTRICAL CHARACTERISTIC (continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
DD Response Characteristic	G_{D1}	Sine wave input (0.25MHz 0.7V_{p-p}) at pin 12; Output at pin 14	−2.1	−1.4	−0.7	dB
	G_{D2}	Sine wave input (2MHz 0.7V_{p-p}) at pin 12; Output at pin 14	−3.8	2.8	−1.8	
	G_{D3}	Sine wave input (0.25MHz 0.07V_{p-p}) at pin 12; Output at pin 14	−4.8	−3.8	−2.8	
	G_{D4}	Sine wave input (2MHz 0.07V_{p-p}) at pin 12; Output at pin 14	−7.0	−6.0	−5.0	
NC Response Characteristic	G_{N1}	Sine wave input (0.25MHz 0.7V_{p-p}) at pin 12; Output at pin 14	−1.0	−0.3	0.4	dB
	G_{N2}	Sine wave input (2MHz 0.7V_{p-p}) at pin 12; Output at pin 14	−2.9	−1.4	0.1	
	G_{N3}	Sine wave input (0.25MHz 0.07V_{p-p}) at pin 12; Output at pin 14	−3.9	−2.0	−1.0	
	G_{N4}	Sine wave input (2MHz 0.07V_{p-p}) at pin 12; Output at pin 14	−4.6	−3.1	−1.6	
PB Squelch Threshold Level	V_{SO}	Video signal input (1VV_{p-p}) at pin 28; Adjust until no output is produced at pin 5	1.5	2.2	3.0	V
PB Video Amp Gain	G_{PV}	Sine wave input (0.5MHz 1V_{p-p}) at pin 28; Output at pin 5	5.6	6.3	7.0	dB
PB Color Amp Gain	G_C	Sine wave input (0.5MHz 1V_{p-p}) at pin 7; Output at pin	15.0	16.0	17.0	dB
REC Mode Supply Current	I_{CC}(REC)	REC Mode, V_{CC} =9V; inflow current of pin 20	15.3	22.3	28.0	mA
AGC Control Characteristic	AGC−6	Video signal input (0.5V_{p-p}) at pin 26; Output at pin 14 (Referenced 1V_{p-p})	−7	−3	2	%
	AGC+6	Video signal input (2.0V_{p-p}) at pin 27; Output at pin 14 (Referenced 1V_{p-p})	−2	4	10	
	AGC_s6	Video signal input (Note 4) at pin 26; Output at pin 14 (Referenced 1V_{p-p})	−2	5	12	

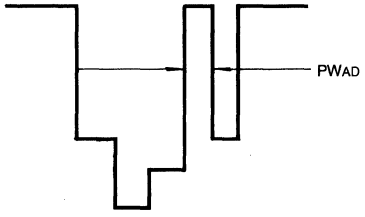
ELECTRICAL CHARACTERISTIC (continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
REC Video Amp Gain	G_{RVA}	Sine wave input (0.5MHz $0.3V_{p-p}$) at pin 13; Output at pin 14	8.9	9.6	10.3	dB
REC Video Amp Phase Characteristic	P_{com}	Sine wave input (2.45MHz $0.3VV_{p-p}$) at pin 13; Phase difference between pin 14 output and pin 13	8.9	9.6	10.3	dB
AGC Det Amp Gain	G_{AD}	Sine wave input (0.5MHz $1VV_{p-p}$) at pin 28; Output at pin 2	8.9	9.6	10.3	dB
AGC Det Amp Adding Pulse Width	PW_{AD}	Video signal amp ($1V_{p-p}$) at pin 28; Output PW pin 2 (Note 5)	—	5.3	—	dB
SYNC Slice Output Level	V_{SYNC}	Video signal inputs at pin 28 ($1V_{p-p}$) and at pin 1 ($0.5V_{p-p}$) (Note 3); Output at pin 3 (Note 6)	7.5	8.1	8.5	V_{p-p}
SYNC Slice Output Pulse Width	PW_{SYNC}		4.8	5.3	5.8	uS
Sync. Sep. Front Delay Time	T_{sync}	Video signal inputs at pin 28 ($1V_{p-p}$) and at pin 1 ($0.5V_{p-p}$) (Note 3); Output at pin 3 (Note 6)	—	2.0	—	μS
Sync. Sep. Threshold Level	TH_{sync}	Level without video level by lowering input level at pin 28	—	– 10	—	dB
EE Amp. Output Level Adjustment	V_{EE}	Pre-adjustment for AGC control: Supply video signal ($1V_{p-p}$) at pin 26 and adjust VR controlled to pin 8 to produce $2V_{p-p}$ Output at pin 5	2.0	4.5	9.0	dB
PB Video Amp. Dynamic Range	DR	Input at pin 28 when supplying V_a at pin 7 through 470KΩ at pin 7, Dynamic range at pin 5	—	3.0	—	V

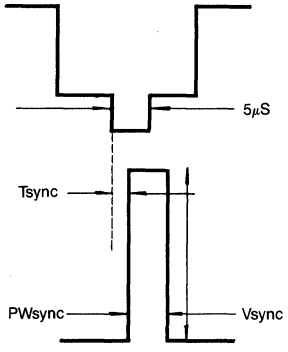
Note: 1. DD=Dynamic de-emphasis. NC=Noise canceller
2. Pre-adjustment for AGC control supply video signal of 1Vp-p at pin 27 to produce 1 Vp-p output
3. Video signal
4. a=0.15V
b=0.7V



5. PW AD



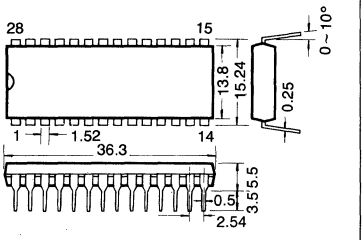
6. Async PWsync Tsync



CHROMA SIGNAL PROCESSOR

KA2986 is a chroma signal processer designed for the home video tape recorders (for NTSC & PAL)

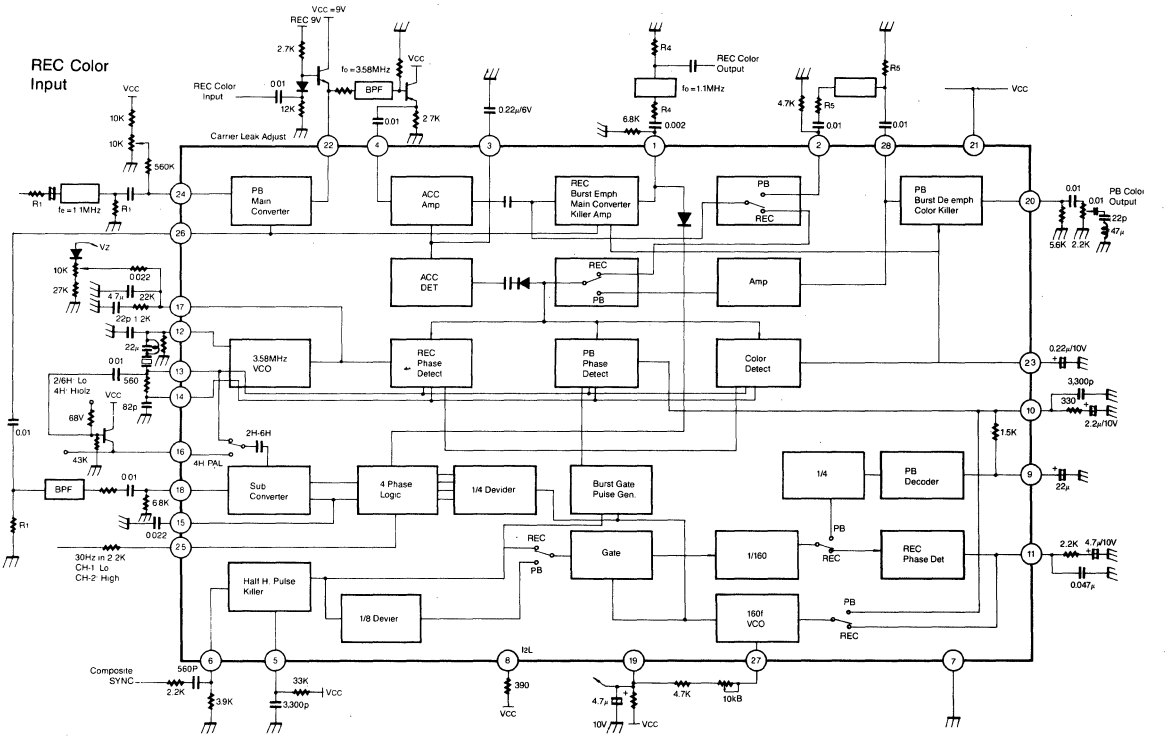
28 Dip **Unit: mm**



FUNCTION

- Automatic color
- Burst Pre-emphasis circuits
- Converter
- Automatic frequency controller for chroma signal
- Automatic phase controller for chroma signal
- Sub converter
- Voltage controlled oscillator (160fH)
- 4 Phase 40fH signal generator
- Voltage controlled oscillator (f=3.579545MHz)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Operating Voltage	V_{opr}	9±1	V
Power Dissipation	P_T	800* 675**	mW
Operating Temperature	T_{opr}	−10.75	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

* Value at=65°C ** Value at=75°C

ELECTRICAL CHARACTERISTIC (V_{CC}=9V, T_a=25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	Total REC Mode at pin 8, 19, 21 and 27	—	70	90	mA
Zener Voltage	V_{19}	820Ω connected to 9V	—	7.2	—	V
REC ACC Dynamic Range	V_{ACC}	With respect to input of 0.15V_{p-p}; input peak to peak voltage which varies output from −3dB to 3dB	15	150	450	mV_{p-p}
REC ACC secondary Harmonic		Input signal to pin 4= 0.15V_{p-p}; 33K connected to GND via pin 26; Output at pin 1 measured	—	−35	−30	dB
PB ACC Secondary Harmonic		Input signal at pin 4= 0.15V_{p-p}; Output at pin 2 measured	—	−43	−30	dB
REC Main Converter Carrier Leak Spurious		f=3.58 MHz	—	−30	−20	dB
		f=4.21 MHz	—	−28	−20	dB
PB Main Converter Conversion Gain		Input signal to pin 24=629KHz, 0.15V_{p-p}; Input signal to pin 26=4.21MHz 0.3V_{p-p}	4.5	6.0	7.5	dB
PB Main Converter Carrier Leak Spurious		f=4.21MHz	—	−32	−20	dB
		f=629KHz	—	−34	20	dB
Burst Emphasis	G_{KR}		5.0	6.0	7.0	dB
Burst Emphasis DC Offset Voltage			—	0	+100	mV
Burst De-emphasis	G_{KP}		—	4.7	—	dB
Burst De-emphasis DC Offset Voltage			—	0	+50	mV
Burst De-Emphasis Amp Gain		Chroma	9.5	11	12.5	dB

ELECTRICAL CHARACTERISTIC (continued)

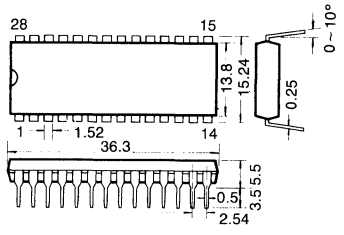
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Burst De-Emphasis Secondary Harmonic			—	-45	-30	dB
REC Killer Sensitivity			—	-43	-30	dB
Subconverter Carrier Leak	C_L	629KHz Internally	—	-40	-30	dB
Subconverter Spurious		629KHz Internally (4.21+0.629×3) MHz	—	-16	-13	dB
REC AFC Pull-in Range			75	—	—	KHz
VCO ($160f_H$) Control Sensitivity	ß		80	140	200	Hz/mV
REC AFC Phase Detective Sensitivity	μRS		50	100	—	mV/deg
REC AFC DC Loop Gain			9.0	14	—	KHz/deg
PB AFC Pull-in Range	f_{pp}		75	—	—	KHz
3.58 VCO Output Peak to Peak Voltage	V_{OSC}	Measured at pin 16	—	0.36	—	V
REC APC Pull-in Range	f_{PR}		300	—	—	Hz
REC APC Phase Detective Sensitivity	μRP		13	18	21	mV/deg
REC APC Control Sensitivity	ß		1.9	—	2.7	Hz/mV
Killer Threshold Voltage		Burst level at pin 4	—	8	—	mV
Injector Current		fr=160fH; Input current of pin 27 measured	—	0.32	—	mV

SERVO CONTOLLER

FUNCTION

- Divider for 30Hz reference signal
- Drum speed controller (Linear servo system)
- Drum phase controller (Digital servo controller)
- Capstan speed controller (Digital servo system)
- Capstan phase controller (Digital servo controller)
- Assembly recording controller

28 Dip Unit: mm



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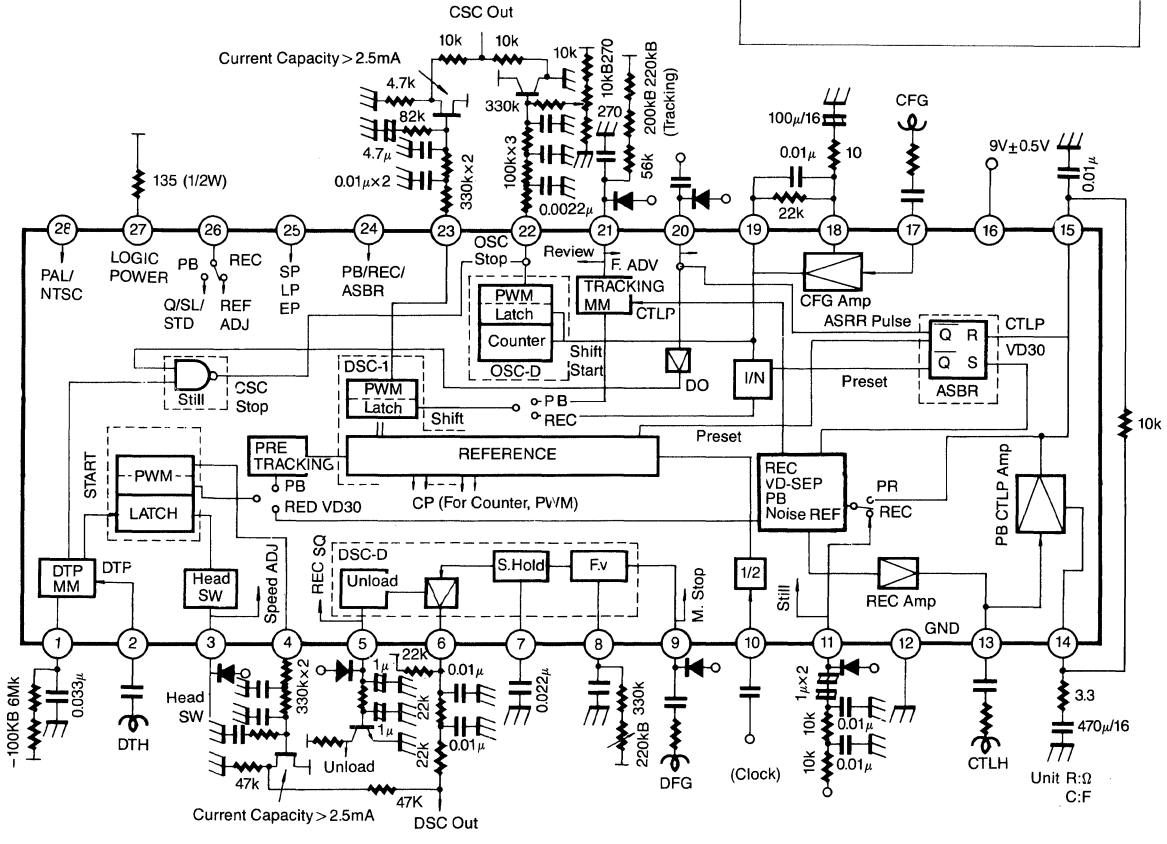


ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Operating Voltage	V_{opr}	9+1	V
Power Dissipation	P_T	800 (65°C) 675 (75°C)	mW
Operating Temperature	T_{opr}	−10~75	°C
Storage Temperature	T_{stg}	−40~125	°C

ELECTRICAL CHARACTERISTIC (T_a=25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current in Linear Portion	I_{CC}	PB Mode	16	24	32	mA
Supply Current in Logic Portion	I_{LOGIC}	(Note 1)	50	53	56	mA
DTP Signal Input Sensitivity	V_{TDP}	Normal operation at Pin 3 (Note 3)	—	0.4	0.9	V_P
Head SW Output Voltage	V3 (H)	No external applications at pin 3	3.5	4.2	4.9	V
	V3 (L)	No external applications at pin 3	—	0.1	0.4	V
Drum FG Signal Input Sensitivity	V_{DF6}	Normal operation at pin 8	—	0.1	—	V_{PP}
Clock Pulse (Chroma Sub Carrier) input Sensitivity	V_{fac}	Normal operation	—	0.03	0.1	V_{PP}
Vertical Sync Signal Input Sensitivity	V_{VD}	REC Mode normal operation at pin 13	—	0.6	0.9	V_P
REC Control Pulse Output Voltage	V_{13out} (H)	Vertical sync signal applied to pin 11 external applications	7.2	7.5	—	V
	V_{13out} (L)	Vertical sync signal applied to pin 11 external applications	—	—	0.4	V
PB Control Pulse Input Sensitivity	V_{13in}	Normal PB Mode normal operation at pin 21 1mS of Input pulse width	—	0.6	1.0	mV_{PP}
PB Control Pulse Amp Output Volage	V_{15out}	$1mV_{p-p}$ of input signal to pin 13	0.8	—	—	V_P
Capstan Frequency Generator Amp Gain	G_{CFG}	Input signal of 360Hz $0.5mV_{p-p}$ in the attached external applications (Note 4)	57	60	—	dB

ELECTRICAL CHARACTERISTIC (continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
ABSR Pulse (Reverse Pulse) Output Voltage	V_{20}(L)	ABSR Mode no external applications	—	0.4	0.8	V
STILL Mode Drop Out Signal Input Sensitivity	V_{DO}	STILL Mode normal operation at pin 22	—	0.3	0.7	V
PB REC ASBR Switching Voltage (Note 5)	V_{PB}		4.2	4.5	6.0	V
	R_{REC}		1.9	2.2	3.0	V
	V_{ASBR}		—	—	0.6	V
SP.LP.EP Switching Voltage (Note 6)	V_{EP}		4.2	4.5		V
	V_{SP}		1.9	2.2	2.5	V
	V_{LP}		—	—	0.5	V
Referential Frequency Fine Tuning Mode Switching Voltage (Note 7)	V	REC Mode	3.5	6.0	—	V
	V	REC Mode	2.0	3.0	4.0	V
	V	REC Mode	—	—	0.5	V
Quit Slow Standard Switching Voltage (Note 8)	V_D	PB Mode	5.5	6.0		V
	V_{SL}	PB Mode	2.0	3.0	4.0	V
	V_{STD}	PB Mode	—	—	0.5	V
PAL NTSC Switching Voltage	V_{PAL}		7.0	—	V_{CC} Note 9	V
	N_{NTSC}		—	0	5.0	V
Speed Adjust Mode Input Voltage	V_{ADJ}		7.0	—	V_{CC} Note 9	V
REC. SQ. Mode Switching Voltage	V_{SQ}		6.5	—	V_{CC}	V
Motor Stop Mode Input Voltage	V_{STOP}		7.0	—	V_{CC}	V
STILL Mode Input Voltage	V_{STILL}		7.0	—	V_{CC}	V
SEARCH Review Mode Input Voltage	V_{SEARCH}		7.0	—	V_{CC}	V
REVIEW. F. ADV. Mode Input Voltage	V_{REV}		7.0	—	V_{CC}	V
NTSC Referential Frequency Period (Note 10)	T_{N+}	REC Mode 6.0V At Pin 26	—	33.20	—	mS
	T_{N2}	REC Mode 3.0V At Pin 26	—	33.36	—	mS
	T_{N3}	REC Mode 0V At Pin 26	—	33.52	—	mS
	T_{PPB}	PB Normal Mode	—	33.36	—	mS
	T_{NS}	PB SEARCH Mode	—	32.65	—	mS
	T_{PR}	PB REVIEW Mode	—	34.36	—	mS

ELECTRICAL CHARACTERISTIC (continued)

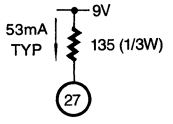
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
PAL Referential Frequency Period (Note 10)	T_{P1}	REC Mode 6.0V At Pin 26	—	47.35	—	mS
	T_{P2}	REC Mode 3.0V At Pin 26	—	47.58	—	mS
	T_{P3}	REC Mode 0V At Pin 26	—	47.81	—	mS
	T_{PPB}	PB Normal Mode	—	40.00	—	mS
	T_{PS}	PB SEARCH Mode	—	39.31	—	mS
	T_{PR}	PB REVIEW Mode	—	41.51	—	mS
REC Control Pulse Width	T_{CTLP}	REC Mode NTSC System VD signal applied to pin 11	—	21.8	—	mS
		REC Mode PAL System VD signal applied to pin 11	—	25.9	—	mS
Head Switch Pulse Width	T_{SW-L}	NTSC System REC Mode DPT signal applied to pin 2	—	16.68	—	mS
		PAL System REC Mode DTP signal applied to pin 2	—	20.00	—	mS
Conversion Gain in Drum Phase Control Portion	G_{CD}	NTSC System	—	66	—	V/mS
		PAL System	—	4.1	—	V/ms
Conversion Gain in Drum Speed Control	G_{DD}	120Hz of DFG Signal 22K of Load resistance at pin 6	—	(0.9)	—	V/Hz
Conversion Gain in Capstan Phase Control Portion (Note 12)	G_{CD}	SP Quick Mode	—	0.83	—	V/Hz
		SP Standard Mode	—	0.83	—	V/Hz
Conversion Gain in Capstan Speed Control Portion (Note 11, 12)	G_{CD}	SP Slow Mode	—	0.42	—	V/Hz
		LP Standard Mode	—	0.42	—	V/Hz
		EP Quick Mode	—	0.83	—	V/Hz
		EP Standard Mode	—	0.20	—	V/Hz
		EP Slow Mode	—	0.20	—	V/Hz
Conversion Gain in Capstan Phase Control Portion (Note 13)	G_{CD}	SP Standard Mode	—	0.51	—	V/Hz
		LP Standard Mode	—	0.26	—	V/Hz
		EP Standard	—	0.13	—	V/Hz

ELECTRICAL CHARACTERISTIC (continued)

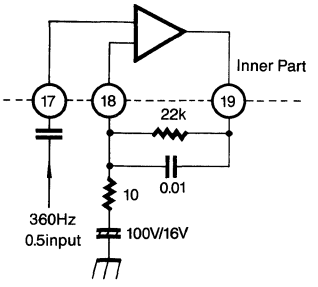
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Conversion Gain in Capstan Speed Control Portion (Note 12)	G_{CD}	SP Quick Mode CFG 1440Hz	—	13	—	mV/Hz
		SP Standard Mode CFG 720Hz	—	26	—	mV/Hz
		SP Slow Mode CFG 360Hz	—	26	—	mV/Hz
		LP Standard Mode CFG 360Hz	—	26	—	mV/Hz
		EP Quick Mode CFG 720Hz	—	26	—	mV/Hz
		EP Standard Mode CFG 240Hz	—	29	—	mV/Hz
		EP Slow Mode CFG 120Hz	—	29	—	mV/Hz
Conversion Gain in Capstan Speed Control Portion (Note 13)	G_{CD}	SP Standard Mode 504Hz	—	32	—	mV/Hz
		LP Standard Mode CPG 252Hz	—	32	—	mV/Hz
		EP Standard Mode 168Hz	—	36	—	mV/Hz
PB Lock Phase (Note 14, 15)	P_{PB}	SP Quick Mode	—	(0.6)	—	mS
		SP Standard Mode	—	(0.6)	—	mS
		SP Slow Mode	—	(0.6)	—	mS
		LP Standard Mode	—	(0.6)	—	mS
		EP Quick Mode	—	(0.6)	—	mS
		EP Standard Mode	—	(6.6)	—	mS
		EP Slow Mode	—	(5.6)	—	mS
PB Lock Phase (Note 14, 16)	P_{PB}	SP Quick Mode	—	(0.5)	—	mS
		SP Standard Mode	—	(0.5)	—	mS
		SP Slow Mode	—	(10.2)	—	mS
ASBR Phase Deferrence (Note 14)	P_{ASBR}	ASBR SP Mode NTSC System	—	(10.2)	—	mS

Note

1. 53mA Typ should be flowed into Pin 27 from power supply of 5V or more, via a resistance



2. Peak voltage at Pin 2 should be less than 5V
3. To prevent malfunction form being caused. The pulse having negative polarity should be clipped by a diode when using a bipolar drum track pulse
4. Test Circuit

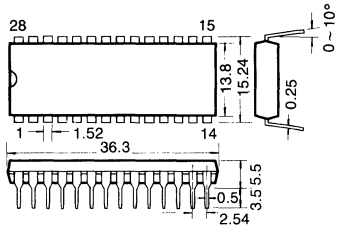


5. When the pin being open. Rec Mode will be selected
6. When the pin being open. LP Mode will be selected
7. When the pin being open. f-0.3% Operation Mode will be selected
8. When the pin being open. Stanard Mode will be selected
9. When V_{CC} =9V is applied the pin, the maximum input current will be current
   Pin 5 ..... 0.8mA
   Pin 3, 20 And 28 ..... 1.4mA
   Pin 9 And 11 ..... 3.7mA
   Pin 21 ..... 6.1mA
10. Clock frequency=3.579545 MHz (for NTSC System)
    Clock frequency=4.43361875 MHz (for PAL System)
11. The values shown are the once measured when the phase control output are disconnected thus, the gains smaller at the additional point
12. NTSC System. Output voltage should be measured via the filter
13. PAL System. Output voltage should be measured via the filter PAL
14. The values are for reference only: they via by the voltage-frequency characteristics in the motor
15. NTSC System
    Tracking MM Delay=16.7mS
16. PAL System
    Tracking MM Delay=20.0mS 4

CHROMA SIGNAL PROCESSOR

KA2988 is a chroma signal processor designed for the home video tape recorders. (for NTSC & PAL)

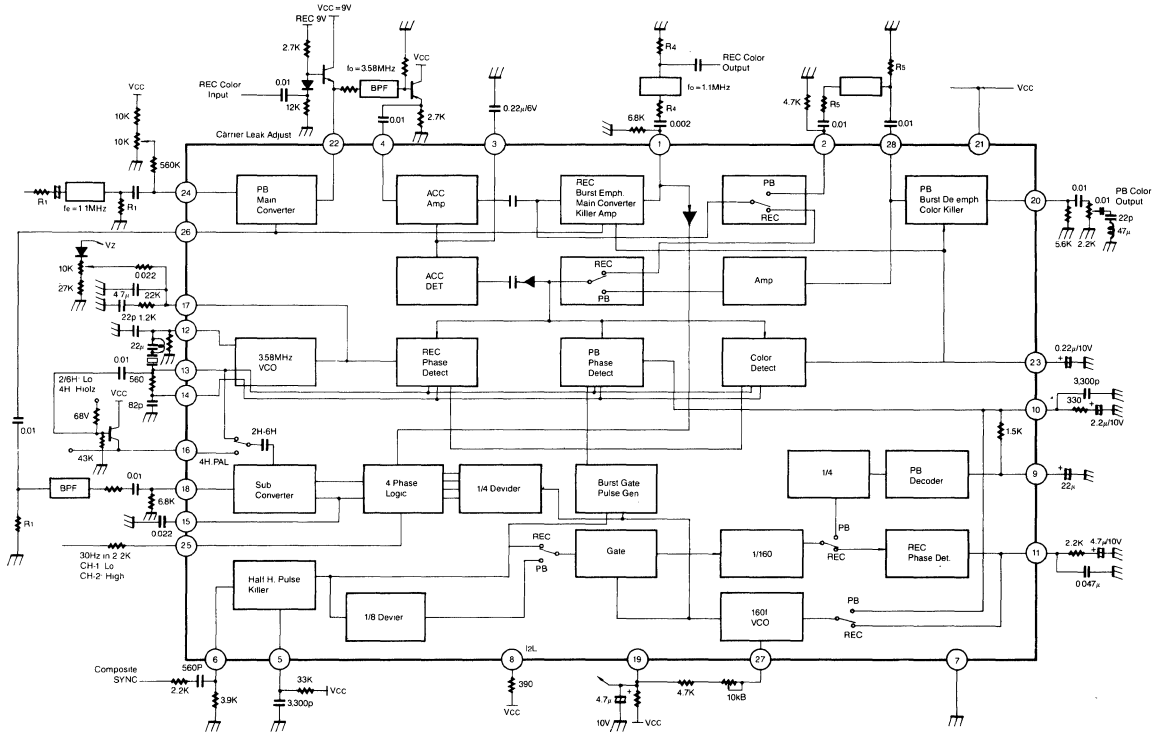
28 Dip **Unit: mm**



FUNCTION

- Automatic color controller
- Burst Pre/De-Emphasis circuits
- Converter
- Automatic frequency controllers for chroma signal
- Automatic phase controllers for chroma signal
- Sub Converter
- Voltage controlled oscillator (160fH)
- 4-Phase 40fH signal generator
- Voltage controlled oscillator (f=3.579545MHz)
- ID circuit

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Power Dissipation	P_D	800 (T_{OPR} = 65°C) 675 (T_{OPR} = 75°C)	mW
Operating Temperature	T_{opr}	−10 ~ +75	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C
Operating Supply Voltage	V_{opr}	9 ± 1	V

ELECTRICAL CHARACTERISTIC (T_a =25°C, V_{CC} =9V)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	V_{CC}	Total REC Mode at Pins 8, 19, 21, and 27	—	70	90	mA
Zener Voltage	V_{19}	820 Connected to 9V	—	7.2	—	V
REC ACC Dynamic Range	V_{ACC}	With Respect to Input of 0.15V_{p-p}; Input Peak to Peak Voltage which Varies Output from −3dB to +3dB	15	150	450	mV_{p-p}
REC ACC Secondary Harmonics		Input Signal to Pin 4= 0.15V_{p-p}; 33K Connected to GND Via Pin 26; Output at Pin 1 Measured	—	−35	−30	dB
PB ACC Secondary Harmonics		Input Signal at Pin 4 =0.15V_{p-p} Output at Pin 2 Measured	—	−43	−30	dB
REC Main Converter Carrier Leak Spurious		f=3.58MHz	—	−30	−20	dB
		f=4.21MHz	—	−28	−20	dB
PB Main Converter Conversion Gain		Input Signal to Pin 24 =629KHz, 0.15V_{p-p}; Input Signal to Pin 26 =4.21MHz, 0.3V_{p-p}	4.5	6.0	7.5	dB
PB Main Converter Carrier Leak Spurious		f=4.21MHz	—	−32	−20	dB
		f=629KHz	—	−34	−20	dB
Burst Emphasis	G_{KR}		5	6	7	dB
Burst Emphasis DC Offset Voltage			—	0	±100	mV
Burst De-Emphasis	G_{KP}		—	4.7	—	dB
Burst De-Emphasis DC Offset Voltage		—	—	0	±50	mV
Burst De-Emphasis AMP Gain		Chroma	9.5	11	12.5	dB

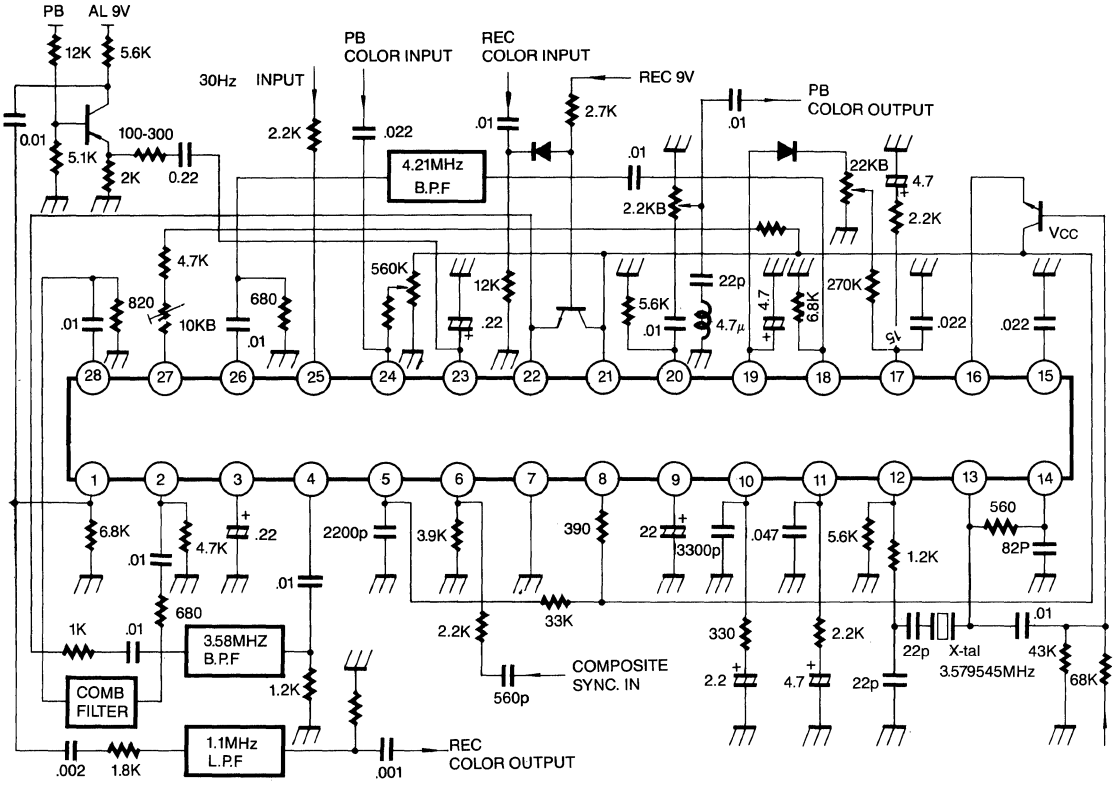
ELECTRICAL CHARACTERISTIC (continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Burst De-Emhasis Secondary Harmonics			—	−45	−30	dB
REC Killer Sensitivity			—	−46	−30	dB
PB Killer Sensitivity			—	−43	−30	dB
Subconverter Carrier Leak	C_L	629KHz Internally	—	−40	−30	dB
Subconverter Spurious		629KHz Internally; (4.21+0.629×3) KHz	—	−16	−13	dB
REC AFC Pull-In Range			75	—	—	KHz
VCO (160f_H) Control Sensitivity			80	140	200	Hz/mV
REC AFC Phase Detective Sensitivity	μRS		50	100	—	mV/DEG
REC AFC DC Loop Gain			9	14	—	KHz/DEG
PB AFC Pull-In Range	f_{PP}		75	—	—	KHz
3.58MHz VCO Output Peak-To-Peak Voltage	V_{OSC}	Measured at Pin 16	—	0.36	—	V
REC APC Pull-In Range	f_{PR}		300	—	—	Hz
REC APC Phase Detective Sensitivity	μRP		13	18	21	mV/DEG
REC APC Control Sensitivity	ß		1.9	—	2.7	Hz/mV
Killer Threshold Voltage		Burst Level at Pin 4 Measured	—	8	—	mV
Injector Current		f_r=160f_H; Input Current into Pin 27 Measured	—	0.32	—	mV
ID Input Threshold Voltage		Threshold at Pin 1 Measured (PB Only)	—	1.1	2.0	V_{DC}

PIN FUNCTIONS

No.		Comment
1	REC Color Output (REC) ID Input (PB)	
2	Buffer Amp Output (connected to 1HDL filter) (only PB)	
3	ACC Det Filter Terminal	DC IV
4	ACC Amp Input	
5	Mono-Multi Constant Terminal 1/2H Pulse Killer Circuit	
6	1/2 H Pulse Kill Circuit Input (Sync. Pulse)	
7	GND	
8	I^2L Injector Terminal	DC 0.8V
9	Freq. Discrimination Filter Terminal	DC 5V
10	APC PD Filter Terminal at PB	DC 5V PB
11	AFC PD Filter Terminal at REC	DC 5V REC
12	3.58 MHz V_{CO} Output	
13	3.58 MHz V_{CO} Input	
14	3.58 MHz V_{CO} Input	
15	4-Phase $40f_H$ Signal By-Pass	
16	3.58 MHz V_{CO} Output	
17	APC PD Filter Terminal at REC	DC 5V
18	Sub Conv. Output	
19	Zener Voltage Terminal	DC 7.2V
20	PS Color Output (only PB)	
21	V_{CC}	DC 9V
22	(REC) REC Color Signal Input (PB) Main Conv. Output (Connected to 3.58 MHz B.P.F.)	
23	Killer Det. Filter Terminal	DC 5V
24	Main Conv. Input (PB 629 KHz signal) (only PB)	
25	30 Hz Pulse Signal Input	
26	Main Conv. Input (Carrier for Freq. Conversion)	
27	160 f_H V_{CO} Control Current	DC 5V
28	(PB) Burst De-emphasis Kill Amp Input	

TYPICAL APPLICATION CIRCUIT



REMOTE CONTROL TRANSMITTER

The KS5803 is a CMOS LSI for infrared remote control transmitter function which is available for C/TV, VTR and TOY etc.

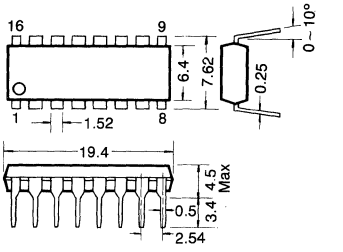
Originally the KS5803 is design to have 20 pin but pratically is indived two types.

One type (KS5803A) has 16 pins to transmit 736 commands. The other (KS5803B) has 20 pins to transmit 8960 commands.

These commands is made to a P.P.M system of 16 bit code, which transmit the code twice (invert in the second time) to prevent operation false code.

The KS5803 is design to be received with 4 bit CPU (DTS).

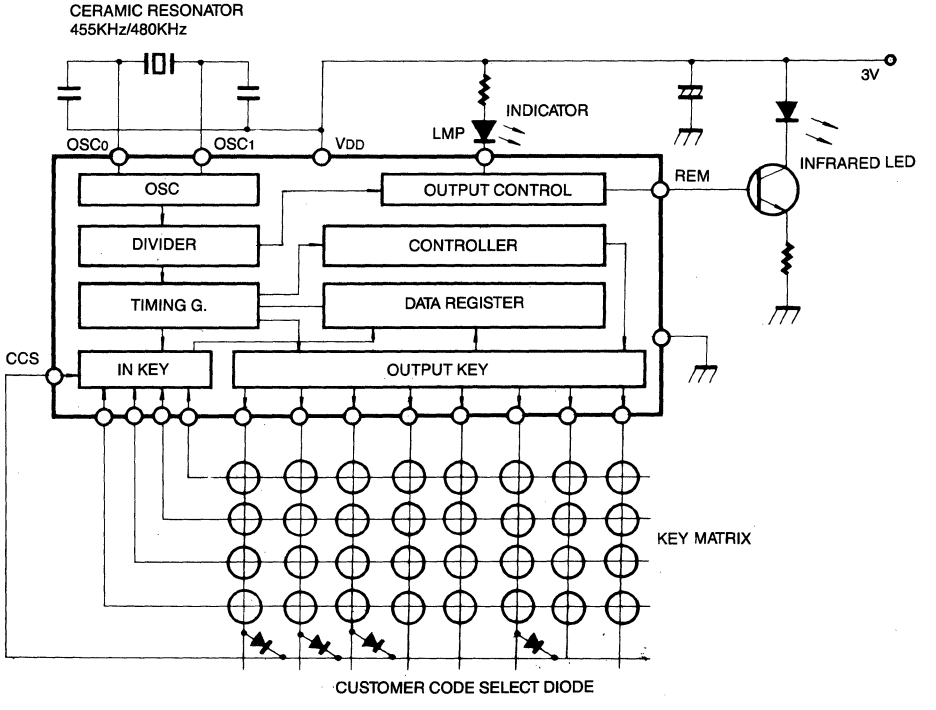
16 Dip Unit: mm



FEATURES

- **Low voltage operation: V_{DD} = 2.0 to 3.3V**
- **Low power consumption (CMOS): $I_{DD} < 1\mu A$ at standby mode**
- **32 function KEY and 3 dual action KEY (KS5803A is 20 function KEY)**
- **256 custom codes selected by external diode (KS5803A is 32 custom codes)**
- **16 bit pulse position modulated code**
- **High efficiency transmission: IR LED ON Duty 3%**
- **Indicator output**
- **Package KS5803A: 16 PIN DIP**
  Package KS5803B: 20 PIN DIP

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD} — V_{SS}	4.0	V
Input Voltage	V_{IN} — V_{SS}	−3.0 — V_{DD}	V
Output Current	I_{OH} (REM, LMP)	−15.0	mA
Power Dissipation	P_D	250	mW
Operating Temperature	T_{opt}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS

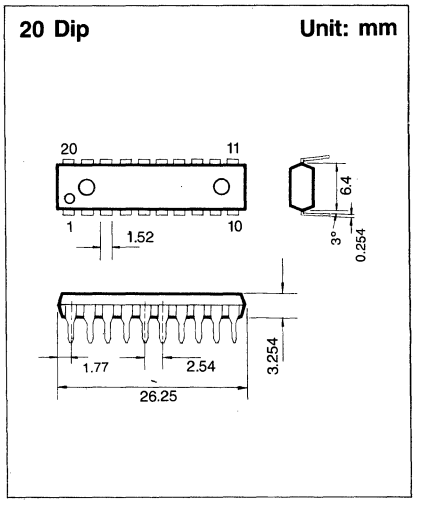
Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	2.0	3.0	3.3	V
Oscillation Frequency	f_{OSC}	400	455	500	kHz
Lamp Output Current	I_{OL} (LMP)		1		mA

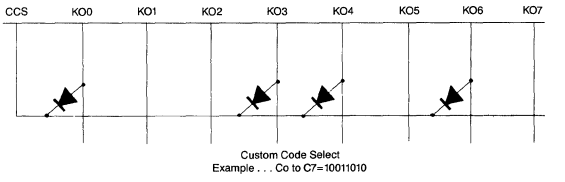
ELECTRICAL CHARACTERISTICS (T_a =25°C, V_{DD} =3.0V)

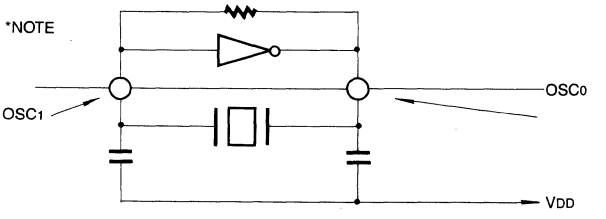
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD} (DP)	f_{OSC} =455KHz	—	0.1	1.0	mA
Supply Current	I_{DD} (ST)	f_{OSC} =STOP	—	—	1	uA
Input High Voltage	V_{IH} (KI)		0.7 VDD	—	VDD	V
Input Low Voltage	V_{IL} (KI)		0	—	0.3 VDD	V
Input Pull Down R	R (KI)		150	300	600	K
Output Current	I_{OH} (REM)	V_{OH} (REM)=1.5V	−5	—	—	mA
Output Low Voltage	V_{OL} (LMP)	I_{OL} =1.0mA	—	—	0.3	V

PIN FUNCTION

PIN (KS5803B)	PIN (KS5803A)	FUNCTION	
1	1	K10	Key Input 0
2	2	K11	Key Input 1 Internaly Pulldown
3	3	K12	Key Input 2 to V_{CC} by Resistor
4	4	K13	Key Input 3
5	5	REM	Remote Output
6	6	V_{DD}	Positive Supply . . . 2.0 to 3.3V
7	—	TEST	TEST Terminal . . . Normally Open
8	7	*OSC0	Oscillator Output Ceramic Resonator
9	8	*OSC1 (*NOTE)	Oscillator Input (400 to 500Hz)
10	9	LMP	Lamp Output . . . Indicator for Transmission
11	10	V_{CC}	Ground
12	—	Ko7	Key Output 7
13	11	Ko6	Key Output 6
14	12	Ko5	Key Output 5
15	13	Ko4	Key Output 4
16	—	Ko3	Key Output 3
17	14	Ko2	Key Output 2
18	—	Ko1	Key Output 1
19	15	Ko0	Key Output 0
20	16	CCS	Custom Code Select input Custom Code is selected by diode Connection to Key Output Ko0 to Ko7) This terminal is usually pull up to V_{DD} by internal Resistor.





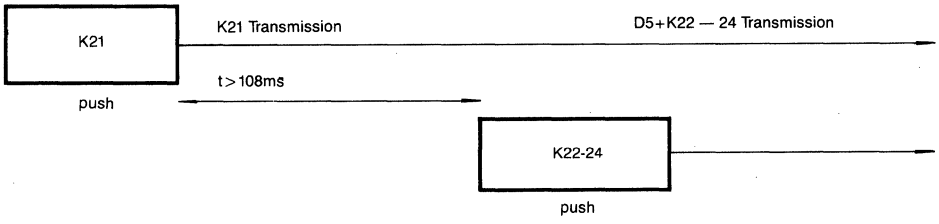


OPERATION OF DUAL ACTION KEY

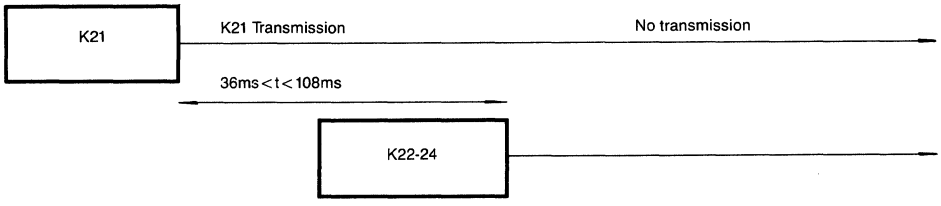
Keys (K21 to K24) are used for preventing failure caused by mistakes.
Example: Cassette Tape Recorder K21 . . . REC KEY
K22 . . . PLAY KEY

KEY	D0	D1	D2	D3	D4	D5	D6	D7
K21 + K22	1	0	1	0	1	1	0	0
K21 + K23	0	1	1	0	1	1	0	0
K21 + K24	1	1	1	0	1	1	0	0

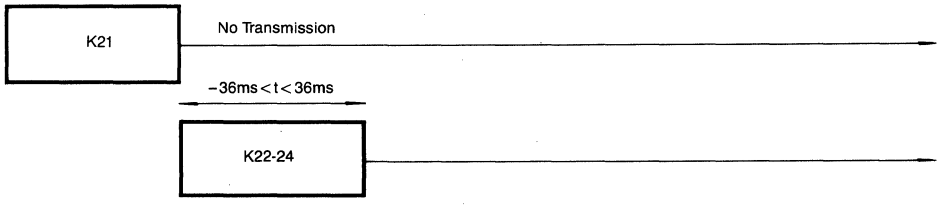
(a) Operation



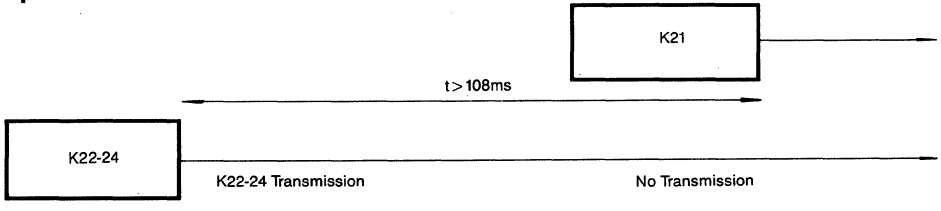
(b) No operation



(c) No operation



(d) No operation

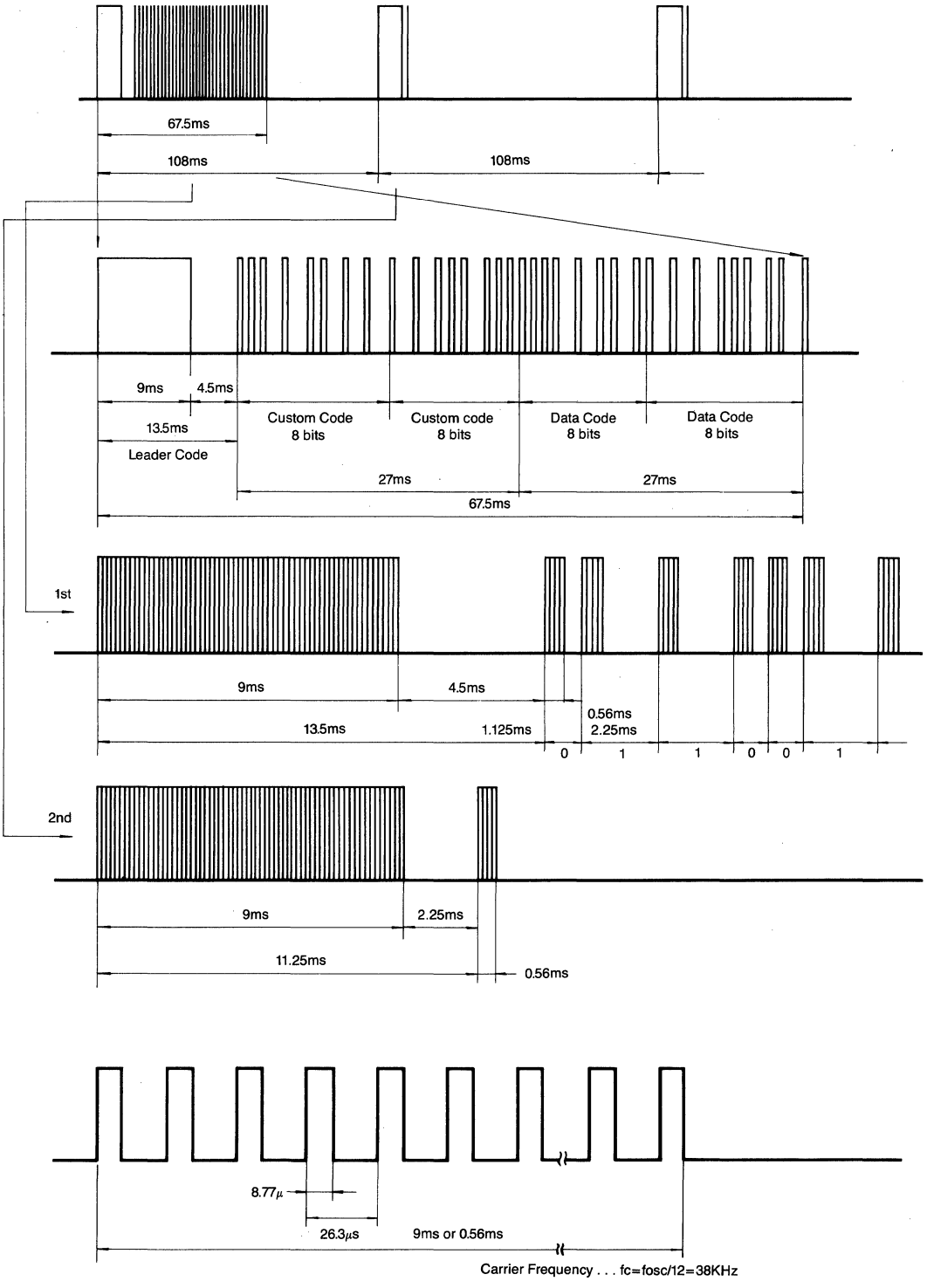


KEY DATA CODE

(Continued)

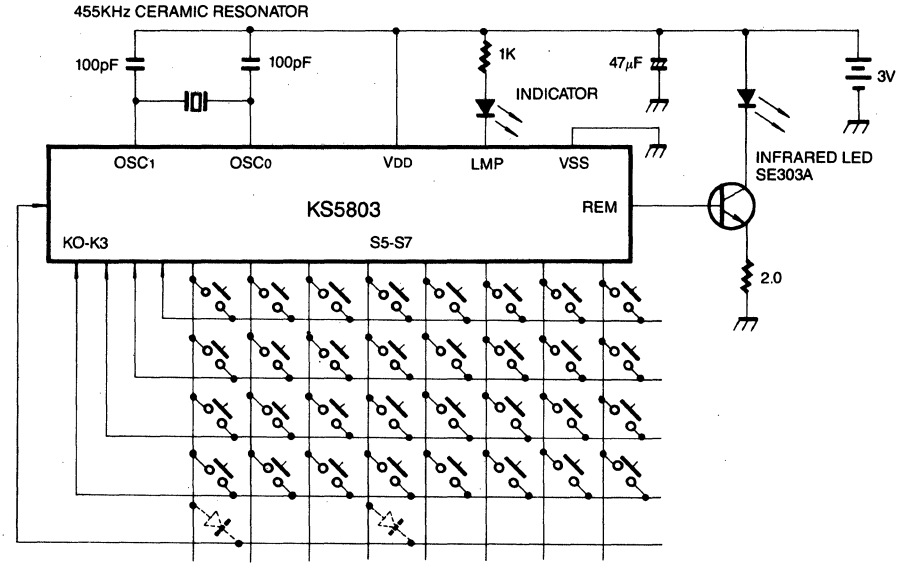
Key	Connection					Data Code								Notes
	K11	K12	K13	K14	K_O	D0	D1	D2	D3	D4	D5	D6	D7	
K 1	*				$K_0$0	0	0	0	0	0	0	0	0	
K 2		*				1	0	0	0	0	0	0	0	
K 3			*			0	1	0	0	0	0	0	0	
K 4				*		1	1	0	0	0	0	0	0	
K 5	*				$K_0$1	0	0	1	0	0	0	0	0	KS5803A is unable to use
K 6		*				1	0	1	0	0	0	0	0	
K 7			*			0	1	0	1	0	0	0	0	
K 8				*		1	1	1	0	0	0	0	0	
K 9	*				$K_0$2	0	0	0	1	0	0	0	0	
K10		*				1	0	0	1	0	0	0	0	
K11			*			0	1	0	1	0	0	0	0	
K12				*		1	1	0	1	0	0	0	0	
K13	*				$K_0$3	0	0	1	1	0	0	0	0	KS5803A is unable to use
K14		*				1	0	1	1	0	0	0	0	
K15			*			0	1	1	1	0	0	0	0	
K16				*		1	1	1	1	0	0	0	0	
K17	*				$K_0$4	0	0	0	0	1	0	0	0	
K18		*				1	0	0	0	1	0	0	0	
K19			*			0	1	0	0	1	0	0	0	
K20				*		1	1	0	0	1	0	0	0	
K21	*				$K_0$5	0	0	1	0	1	0	0	0	
K22		*				1	0	1	0	1	0	0	0	
K23			*			0	1	1	0	1	0	0	0	
K24				*		1	1	1	0	1	0	0	0	
K25	*				$K_0$2	0	0	0	1	1	0	0	0	
K26		*				1	0	0	1	1	0	0	0	
K27			*			0	1	0	1	1	0	0	0	
K28				*		1	1	0	1	1	0	0	0	
K29	*				$K_0$7	0	0	1	1	1	0	0	0	KS5803A is unable to use
K30		*				1	0	1	1	1	0	0	0	
K31			*			0	1	1	1	1	0	0	0	
K32				*		1	1	1	1	1	0	0	0	

REMOTE OUTPUT WAVEFORMS

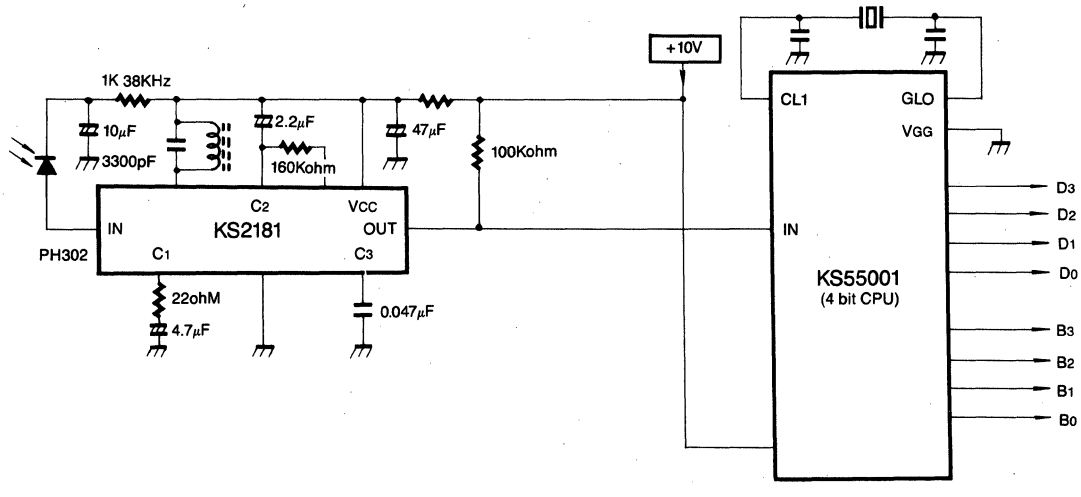


TYPICAL APPLICATION CIRCUIT

TX



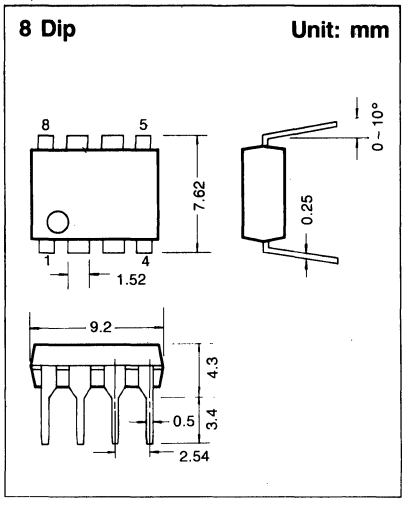
RX



V. TELEPHONE ICs

TONE RINGER

The KA2410/KA2411 is a bipolar integrated circuit designed for telephone bell replacement.



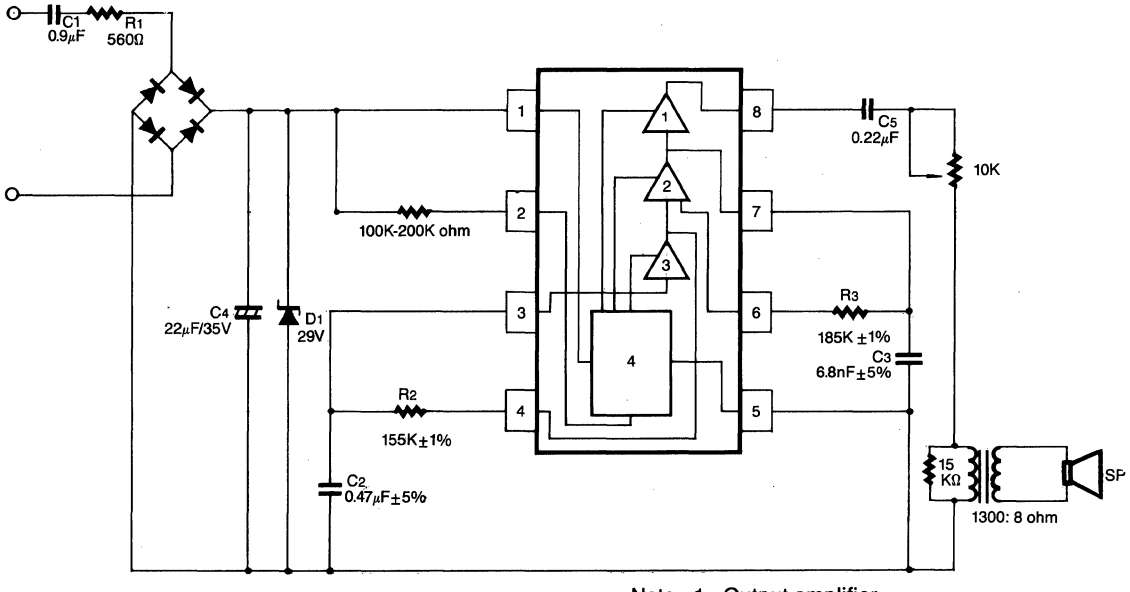
FUNCTIONS

- Two oscillators
- Output amplifier
- Power supply control circuit

FEATURES

- **Designed for telephone bell replacement**
- **Low current drain.**
- **Small size 'MINIDIP' package.**
- **Adjustable 2-frequency tone.**
- **Adjustable warbling rate.**
- **Built-in hysteresis prevents false triggering and rotary dial 'CHIRPS'**
- **Extension tone ringer modules**
- **Alarms or other alerting devices.**
- **External triggering or ringer disable (KA2410).**
- **Adjustable for reduced supply initiation current (KA2411)**

APPLICATION CIRCUIT 1 (KA2410)



Note: 1. Output amplifier
2. High frequency oscillator
3. Low frequency oscillator
4. Hysteresis regulator

Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	30	V
Power Dissipation	P_D	400	mW
Operating Temperature	T_{opr}	– 45 to 65	°C
Storage Temperature	T_{stg}	– 65 to 150	°C

ELECTRICAL CHARACTERISTICS (T_a =25°C)

(All voltage referenced to GND unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}				29.0	V
Initiation Supply Voltage	V_{SI}	See Fig. 2	17	19	21	V
Initiation Supply Current	I_{SI}	KA2411-6.8K-Pin 2 to GND	1.4	2.5	4.2	mA
Sustaining Voltage	V_{SUS}	See Fig. 2	9.7	11.5	13	V
Sustaining Current	I_{SUS}	No Load V_{CC}=V_{SUS}, See Fig. 2	0.7	1.4	2.5	MA
Trigger Voltage	V_{TR}	KA2410 Only V_{CC} =15V	8.5	9.5	10.5	V
Trigger Current	I_{TR}	KA2410 Only		20.0	1000	μA
Disable Voltage	V_{DIS}	KA2410 Only		0.4	0.8	V
Disable Current	I_{DIS}	KA2410 Only	– 40	– 50		μA
Output Voltage High	V_{OH}	V_{CC} =21V, I_8 =–15mA Pin 6=6V, Pin 7=GND	18.0	19.0	20.0	V
Output Voltage Low	V_{O1}	V_{CC} =21V, I_8 =15mA Pin 6=GND, Pin 7=6V	0.5	0.9	1.3	V
I_{IN} (Pin 3) I_{IN} (Pin 7)		Pin 3=6V, Pin 4=GND Pin 7=6V, Pin 6=GND	— —	— —	500 500	nA nA
High Frequency 1 High Frequency 2 Low Frequency	f_{H1} f_{H2} f_L	R_2 =185K, C_2 =6800pF R_2 =185K, C_2 =6800pF R_1 =155K, C_1 =0.47μF	472 615 9.3	508 635 10	543 679 10.7	Hz Hz Hz

• NOTE (see electrical characteristics sheet)

1. Initiation supply voltage (Vsi) is the supply voltage required to start the tone ringer oscillating.
2. Sustaining voltage (Vsus) is the supply voltage required to maintain oscillation.
3. Vtr and Itr are the conditions applied to trigger in to start oscillation for Vsus Vcc Vsi.
4. Vdis and Idis are the conditions applied to trigger in to inhibit oscillation for Vsi Vcc.
5. Trigger current must be limited to this value externally.

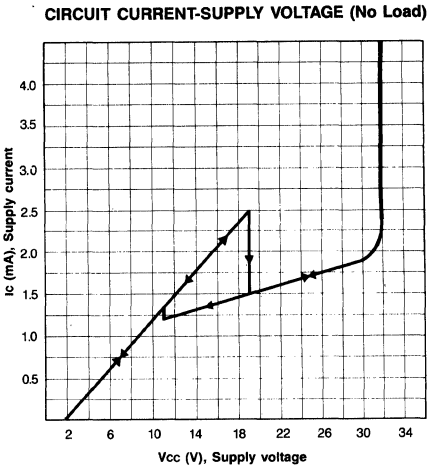


Fig. 2

APPLICATION NOTE

The application circuit illustrates the use of the KA2410/KA2411 devices in typical telephone or extension tone ringer application.

The AC ringer signal voltage appears across the TIP and RING inputs of the circuit and is attenuated by capacitor C_1 and resistor R_1.

C_1 also provides isolation from DC voltages (48V) on the exchange line.

After full waveform is filtered by capacitor C_4 to provide a DC supply for the tone ringer chip.

As this voltage exceeds the initiation voltage (V_{SI}) oscillation starts.

With the components shown, the output frequency chops between 516 (f_{h1}) and 630Hz (f_{h2}) at a 10Hz (f_L) rate.

The loudspeaker load is coupled through a 1300 to 8 transformer.

The output coupling capacitor C_5 is required with transformer coupled loads.

When driving a piezo-ceramic transducer type load, the coupling C_5 and transformer (1300: 8Ω) are not required. However, a current limiting resistor is required.

The low frequency oscillator oscillates at a rate (f_L) controlled by an extemal resistor (R_2) and capacitor (C_2).

The frequency can be determined using the relation $f_L = 1/1.384\ R_2.\ C_2$. The high frequency oscillates at a f_{h1}, f_{h2}, controlled by an external resistor (R_3) and capacitor (C_3). The frequency can be determined using the relation $f_{h1} = 1/1.54\ R_3.\ C_3$. $f_{h2} = 1/1.26\ R_3,\ C_3$.

Pin 2 of the KA2411 allows connection of an external resistor R_{SL}, which is used to program the slope of the supply current vs supply voltage characteristics (see Fig 4), and hence the supply current up to the initiation voltage (Vsi). This initiation voltage remains constant independent of R_{SL}.

The supply current drawn prior to triggering varies inversely with R_{SL}. decreasing for increasing value of resistance. Thus, increasing the value of R_{SL} will decrease the amount of AC ringing current required to trigger the device. As such, longer sucribser loops are possible since less voltage is dropped per unit length of loop wire due to the lower current level. R_{SL} can also be used to compensated for smaller AC coupling capacitors (C_5 on Fig 3) (higher impedance) to the line which can be used to alter the ringer equivalence number of a tone ringer circuit.

The graph in Fig. 4 illustrates the variation of supply current with supply voltage of the KA2411. Three curves are drawn to show the variation of initiation current with R_{SL}. Curve B ($R_{SL} = 6.8K$) shows the I-V characteristic for the KA2411 tone ringer. Curve A is a plot with $R_{SL} < 6.8K\Omega$ and shows an increase in the current drawn up to the initiation voltage Vsi. The I-V characteristic after initiation remains unchanged. Curve C illurates the effect of increasing RSL above 6.8K Initiation current decreases but again current after triggering is unchanged.

APPLICATION CIRCUIT (KA2411)

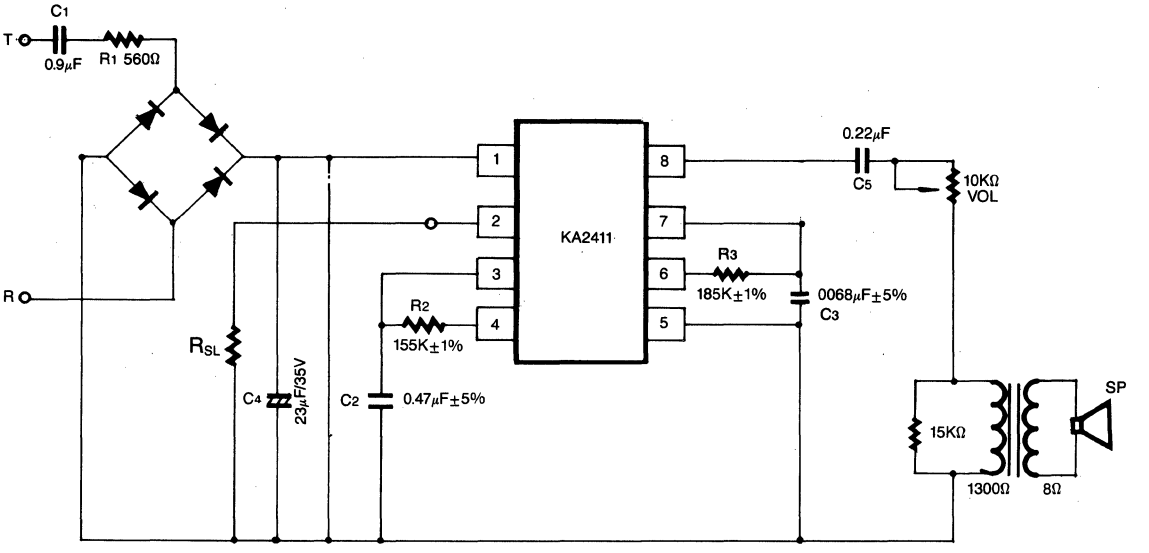


Fig. 3

LINEAR INTEGRATED CIRCUIT

KA2411 Supply Current (No Load) Vs. Supply Voltage

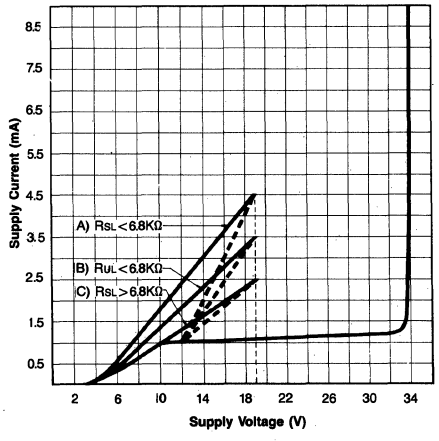


Fig. 4

EQUIVALENT CIRCUIT (Pin 2 Input)

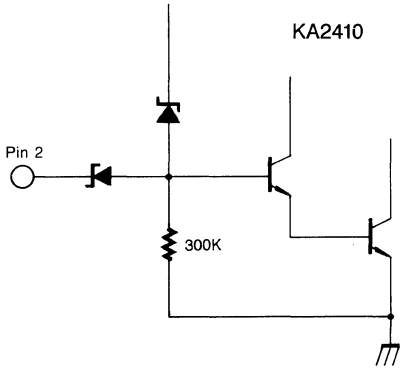


Fig. 5

INHIBITING OSCILLATION

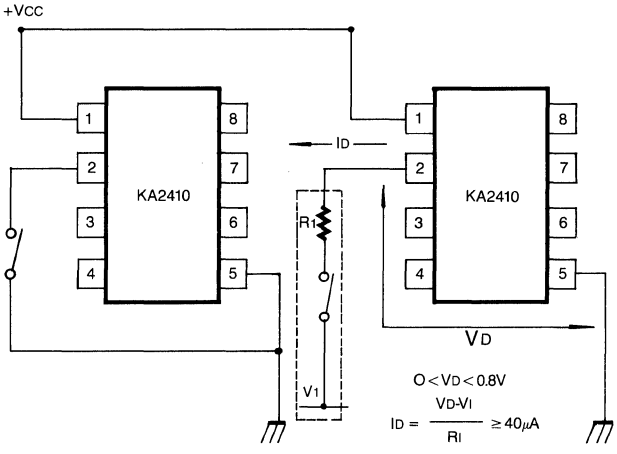


Fig. 6

PROGRAMMING THE KA2410 INITIATION SUPPLY VOLTAGE

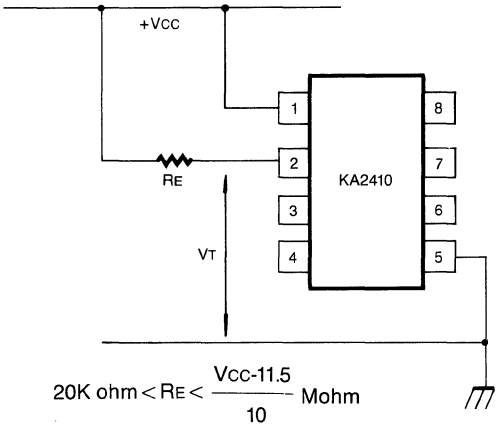


Fig. 7

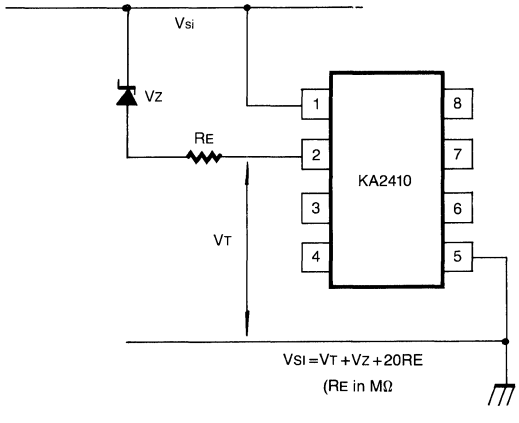


Fig. 8

TRIGGERING KA2410 FROM CMOS OR TTL LOGIC

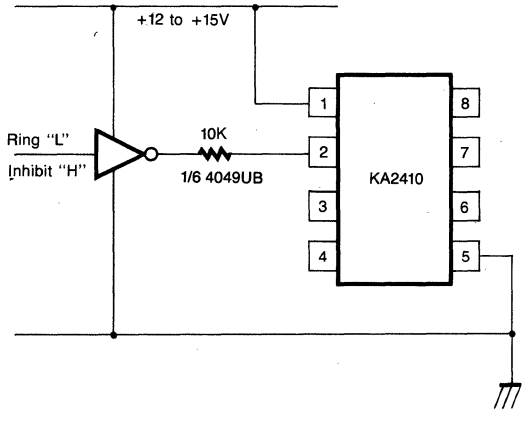


Fig. 9

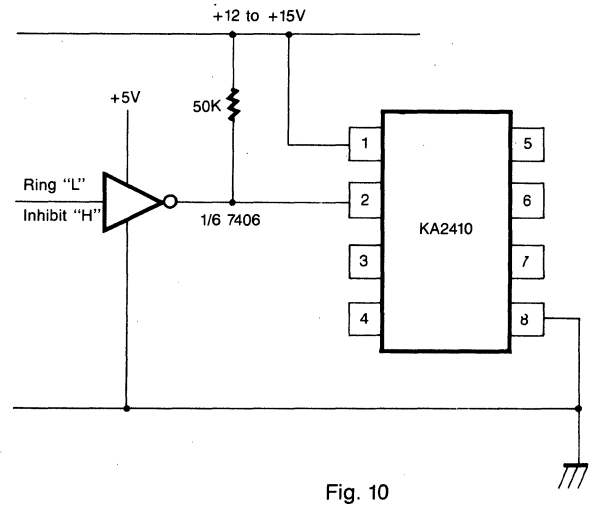
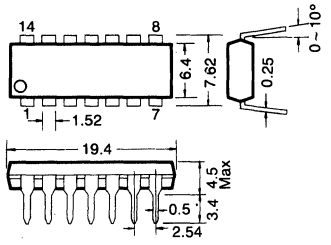


Fig. 10

TELEPHONE SPEECH CIRCUITS

The KA2412 A/B/C is designed for replacement of the hybrid circuit (2 ~ 4 wire interface) in conventional telephone.

14 Dip Unit: mm



FEATURES

- **Adjustable sending and receiving gain to compensate for line attenuation by sensing the line current.**
- **The same type of transducer can be used for both transmitter and receiver, usually a 350Ω dynamic type.**
- **Output impedance can be matched to the line, independent of transducer impedance.**
- **Minimum number of external parts required**
- **Parallel operation with pulse dialer IC (KS5804, KS5805A/B, KS5806) as well as DTMF IC (KA2413, KS5808)**
- **KA2412A: Pin 7 no connect**
  KA2412B: Pin 7 Mute input
  KA2412C: Pin 7 Mute input

BLOCK DIAGRAM

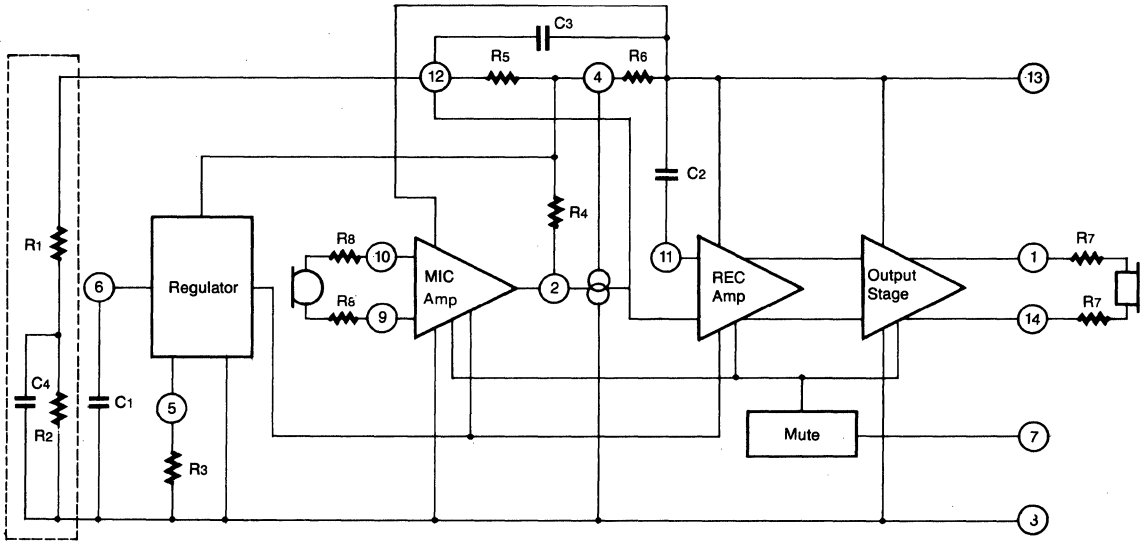


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Line Voltage (3 msec pulse duration)	V_L	22	V
Forword Line Current	I_{LF}	120	mA
Reverse Line Current	I_{LR}	−150	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a = −15°C ~ +45°C, f=300Hz ~ 3400Hz unless otherwise specified. Refer to the test circuit.)

Characteristic	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit
Line Voltage	V_L	Fig 2	I_L = 80mA I_L = 20mA I_L = 10mA	10.0 5.0 3.8		11.5 5.8 4.6	V
Sending Gain	G_S	Fig 3	T_a = 25°C, f=1KHz I_L = 10mA I_L = 20mA I_L = 60mA I_L = 80mA	 46.5 45.4 40.7 40.0		 50.5 49.5 44.0 43.0	dB
Sending Gain Variation V_S temp	ΔG_{ST}	Fig 3	−15°C < Tamb < +45°C			±1.0	dB
Sending Gain Flatness	ΔG_{SF}	Fig 3	G_S = 0dB at f=1KHz I_L = 10 ~ 80mA			±0.5	dB
Sending Distortion	THD_S	Fig 3	I_L = 10 ~ 15mA; V_{SO} = 0.7V_P I_L = 15 ~ 80mA; V_{SO} = 1V_P			2.0 2.0	% %
Sending Noise	V_{NS}		V_{MI} = 0, I_L = 60mA			−73	dB_{MP}
Microphone Amplifier Impedance	R_{IN} (MIC)			45.0		85.0	Ω
Maximum Sending Output	V_S (max)	Fig 3	I_L = 10 ~ 80mA V_{MI} = 1V_P			3.0	V_P
Receiving Gain	G_R	Fig 4	T_a = 25°C, f=1KHz I_L = 10mA I_L = 20mA I_L = 60mA I_L = 80mA	 −13.6 −13.6 −18.0 −19.0		 −10.0 −10.6 −15.0 −16.0	dB
Receiving Gain Variation V_S temp	ΔG_{RT}	Fig 4	−15°C < Tamb < 45°C			±1.0	dB
Receiving Gain Flatness	ΔG_{RF}	Fig 4	G_R = 0dB at f=1KHz I_L = 10 ~ 80mA			±0.5	dB

ELECTRICAL CHARACTERISTICS (Continued)

(T_a = −15°C ~ +45°C, f=300Hz ~ 3400Hz, unless otherwise specified)

Characteristic		Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit
Receiving Distortion		THD_R	Fig 4	I_L = 15 ~ 80mA V_{RO} = 500mV_P			2.0	%
Receiving Noise		V_{NR}	Fig 4	V_{RI} = 0V, I_L = 60mA Psophometric			100.0	μV
Receiving Amplifier Output Impedance		R_O (REC)	Fig 4			110		Ω
Side Tone		ST	Fig 5	f=1KHz, T_a = 25°C I_L = 20mA I_L = 60mA		7.0 0.0		dB
Return Loss		R_L	Fig 6	S2 in a S2 in b		14 14		dB
Mute Input Current (KA2412B)	Active	I_{MA}	Fig 2	I_C = 10 ~ 80mA	50			μA
	Disable	I_{MD}			—	—	0	μA
Mute Input Voltage (KA2412B)	Active	V_{MA}	Fig 2	I_C = 10 ~ 80mA	0.66			V
	Disable	V_{MD}					0.2	V
$\overline{\text{Mute}}$ Operating Current (KA2412C)			Fig 2	I_C = 10 ~ 80mA			−80	μA
$\overline{\text{Mute}}$ Operating Voltage (KA2412C)			Fig 2	I_C = 10 ~ 80mA			1	V
Extra Available Current when Muted at the Same DC Voltage		I_{DC}		(KA2412B/C) I_C = 20 ~ 100mA		10		mA

PIN DESCRIPTION

1. PIN 1, PIN 14 : Recevier output
2. PIN 2 : Line impedance adjust
3. PIN 3 : Ground
4. PIN 4 : DC regulator
5. PIN 5 : Bias
6. PIN 6 : AC loop opening
7. PIN 7 : Mute, $\overline{\text{Mute}}$, No connection, Pin 7 is specially designed for the mute function of a transmitter and in order to be heard a felicitous sound from a receiver when KS2412B/C is used for parallel operation with any DTMF IC. For example KA2412B and KA2412C can be used with KA2413 and KS5808 respectively.
8. PIN 8 : No connection
9. PIN 9, PIN 10 : Mic input
10. PIN 11 : Input receive Amp (−)
11. PIN 12 : Input receive Amp (+)
12. PIN 13 : V_{CC}

TEST CIRCUIT

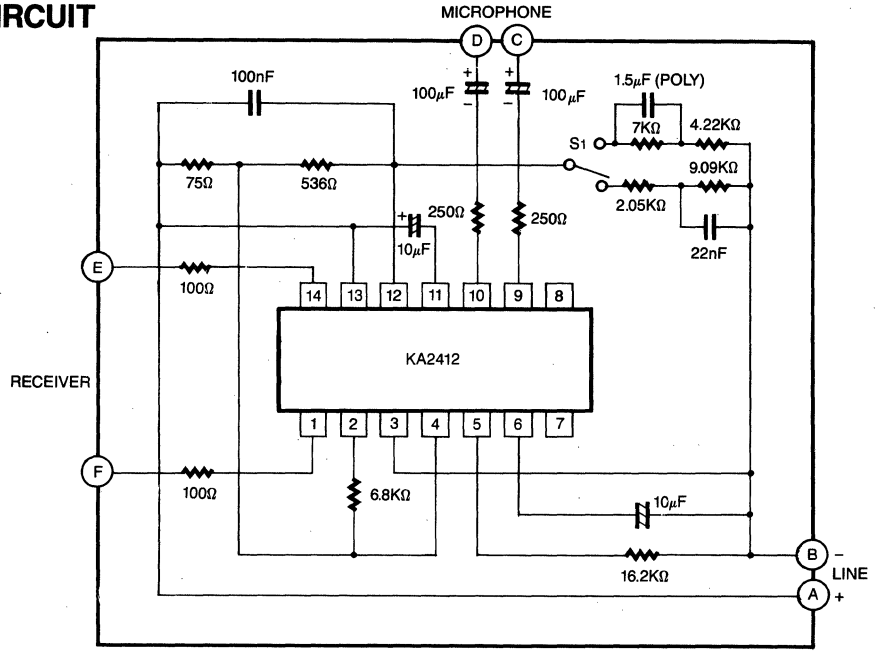


Fig. 2

Sending Gain

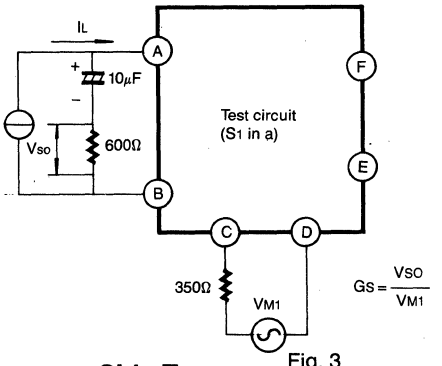


Fig. 3

Receiving Gain

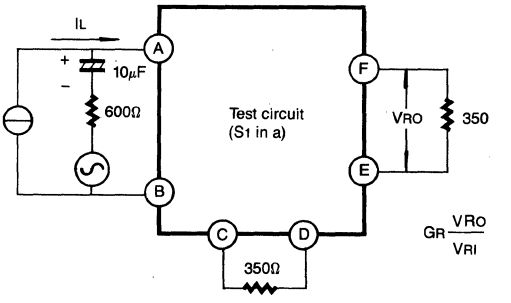


Fig. 4

Side Tone

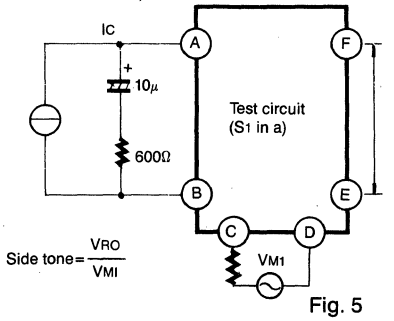


Fig. 5

Return Loss

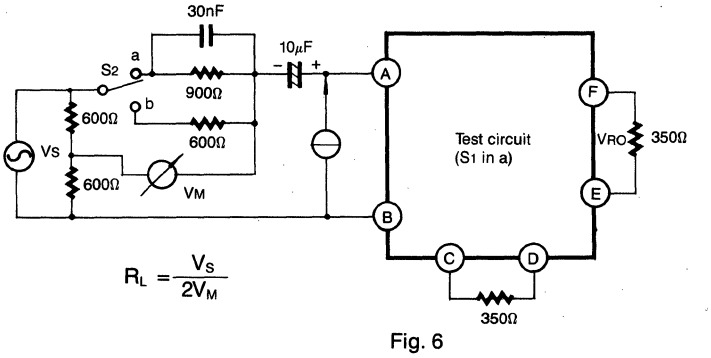


Fig. 6

APPLICATION INFOMRATION

The following table shows the recommended for the Fig 1. Different values can be used and notes are added in order to help designer.

Component	Recommended Value	Purpose	Note
R_1	2.05K	Balance network	In order to optimize the sidetone it is possible to change R_1 and R_2 values. In any case: $\frac{Z_B}{Z_L} = \frac{R_5}{R_6}$ where $Z_B = R_1 + R_2 // C_4$
R_2	9.09K		
R_3	16.2K	Bias resistor	Changing R_3 value, it is possible to shift the gain characteristics. The value can be chosen from 15K to 20K. The recommended value assures the maximum swing (See Fig. 9)
R_5	536	Bridge resistors	The ratio R_5/R_6 fixes the amount of the signal delivered to the line. (See Fig. 7)
R_6	75		
R_7, R_7'	100	Receiver impedance matching	R_7 and R_7' must be equal; 100Ω is a typical value for dynamic capsules
R_8, R_8'	250	Microphone impedance matching	R_8 and R_8' must be equal; 250Ω is a typical value for dynamic capsules. Furthermore, they determine a sending gain variation according to; $G_S = 20 \log \frac{R_X}{850}$ where $R_X = R_8 + R_8' + R_{MIC}$ (See Fig. 8)
C_1	10uF	AC loop opening	Ensures a high regulator impedance for AC signals (=20KΩ). This capacitor should not be higher than 10uF in order to have a short response time of the system.
C_2	1uF	DC decoupling for receiving input	
C_3	82nF	High frequency roll-of	C_3 determines the high frequency response of the circuit. It also acts as RF by pass.
C_4	22nF	Balance network	See note for R_1 and R_2

DESCRIPTION

1. Circuit Description:

The KA2412A, the KA2412B and the KA2412C are based on a bridge configuration. They contain a regulator block, a sending amplifier and a receiving amplifier. The regulator monitors the line current and adjusts the amplifier gain to compensate for the line length.

The transmit/receiver amplifiers are connected to the line via an external bridge to provide side tone attenuation. When the subscriber is talking, A controlled amount of the sending signal is allowed to reach the receiver to give a feedback to the subscriber. The phenomenon is caused by mismatching of the wheastone bridge and is called the signal of side tone.

The line current compensation ensures that when the subscriber is talking, the signal delivered to the line is increased in according to the line length. When he is hearing, the signal level on the receiver capsule is constant.

Gain variation over the operating temperature range is less than ±1dB. The impedance to the line can be adjusted; without any change in circuit parameters; by changing an external resistor (6.8KΩ at Pin 2).

The KA2412A/B/C works with the same type of transducers for both transmitter and receiver (typically 350 Ω Dynamic units). But the sending amplifiers can be matched to different transducers simply by varying external components. (see Fig 9, 10)

2. Two to four wires conversion

1) In the case of the traditional telephone set:

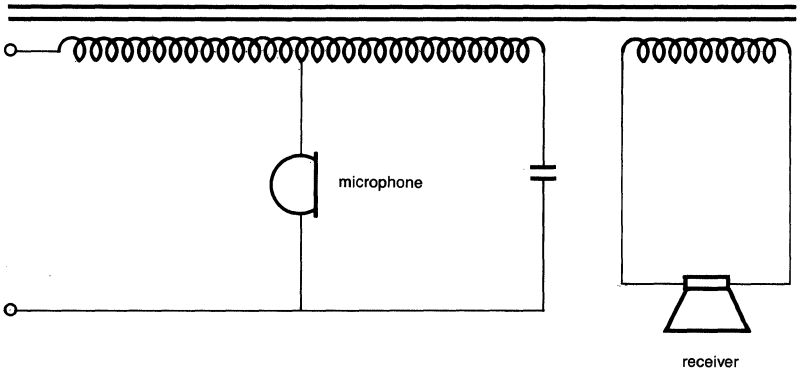


Fig. 10

A traditional speech circuit is equivalently equal to the circuit as described in Fig. 7. The microphone is composed of carbon powder. It converts the sound presure into the variation of resistance and so a AC signal is generated when the bias current flows through the microphone and a subscriber is talking. The current actuated by microphone does not affect receiver because it is compensated by the coil polarity.

But the incoming signal is transferred to receiver, so and this circuit is called 2 — 4 wires conversion, which is incoming 2 wires and Mic, Receivers 4 wires.

2) In the case of the KA2412 A/B/C:

KA2412 performs the two wires (Telephone line) to four wires (Microphone, Receiver) conversion by means of a wheastone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see Fig. 8)

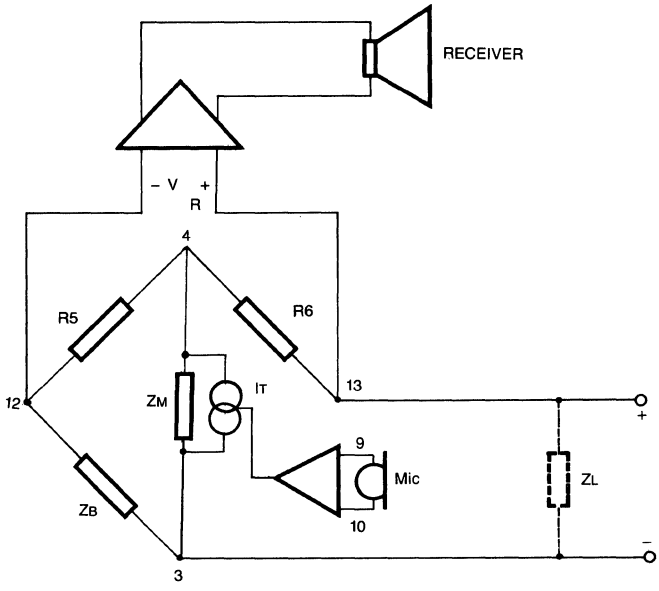


Fig. 11

For a perfect balancing of the bridge $\frac{Z_B}{Z_L} = \frac{R5}{R6}$

* In sending mode;

The AC signal from the microphone is sent to one diagonal of the bridge (pin 3 and pin 4). A small percentage of the signal power is lost on Z_B (being $Z_B >> Z_L$); the main part is sent to the line Via R6.

The impedance A_M is defined as $\frac{V_{4\text{-}3}}{I_{4\text{-}3}}$

$$V_R = \frac{(R6+Z_B)//(R5+Z_L)}{Z_M+(R6+Z_B)//(R5+Z_L)} \left(\frac{Z_L}{R6+Z_L} - \frac{Z_B}{R5+Z_B}\right) Z_M I_T$$

To reduce the receiving input signal,

$$\frac{Z_L}{R6+Z_L} = \frac{Z_B}{R5+Z_B} \rightarrow \frac{R6}{Z_L} = \frac{R5}{Z_B}$$

also, In order to reduce power loss in R5 & Z_B and to transfer the maximum power to the line via R6.

$R5+Z_B >> R6+Z_L$

$R6+Z_M = Z_L$

Then the line impedance Z_L grows from 600 ohm up to 900 ohm when the line length increases.
The voltage driven to the line is

$$V_L = \frac{Z_L}{R6+Z_M+Z_L} \times Z_{MIT}$$

In order to maximize sending Gain
$Z_L >> R6$

Therefore, in the case of the KA2412 test circuit:
$R6=75$, $Z_M=6.8K/11$, $Z_L=600$

$$V_L = \frac{Z_L}{Z_M+R6+Z_L} \times Z_M I_T = 286.82 I_T$$

* In receiving mode:
The AC signal coming from the line is sensed across the second diagonal of the whestone bridge (pin 11 and pin 13). After amplification it is applied to the receiver.

$$V_R = \frac{V_I}{Z_L+R_6+(R_5+Z_B)//Z_M} (R_6+R_5+Z_B)//Z_M \left(1-\frac{Z_B}{Z_B+R_5}\right)$$

$$= \frac{V_I}{Z_L+R_6+(R_5+Z_B)//Z_M} \left(R_6+\frac{Z_M R_5}{Z_M+R_5+R_6}\right)$$

To avoid the reflection
$Z_L=R_6+Z_M$, $10\,Z_M=R_5+Z_B$

Therefore

$$V_R = \frac{V_I}{2R_6+1.91\,Z_M}\left(R_6+\frac{Z_B}{11}\right)$$

In the case of the KA2412A/B/C test circuit
$Z_L=600\Omega$, $R_6=75\Omega$, $Z_M=6.8K\Omega/11=6.8\Omega$
$R_5=536\Omega$, $Z_B=6.076K\Omega$ ($f_{REF}=1KHz$)

$$\frac{V_R}{V_I}=0.093$$

3. Transducers interfacing.

The receiving output stage (pin 1 and pin 14) is particulary intended to drive dynamic capsules. (Low output impedance, Typically 100: high current capability, 3.0 mAp) when a dynamic capsule with Low impedance ($< 350\Omega$) is used, it is necessary to increase the receiving gain by decreasing R7 and R7'.

In sending mode, it is possible to adjust the input stage (pin 9 and pin 10) can be matched to different transducers simply by varying external components. (See Fig. 12 and Fig. 13)

1) When a microphone of carbon type is used, it is necessary to provide a perfect bias current because the resistance of carbon microphone is varied by the sound pressure. Therefore in order to convert the variaton of resistance into the voltage signal, A perfect bias current have to be supplied as described in Fig. 12

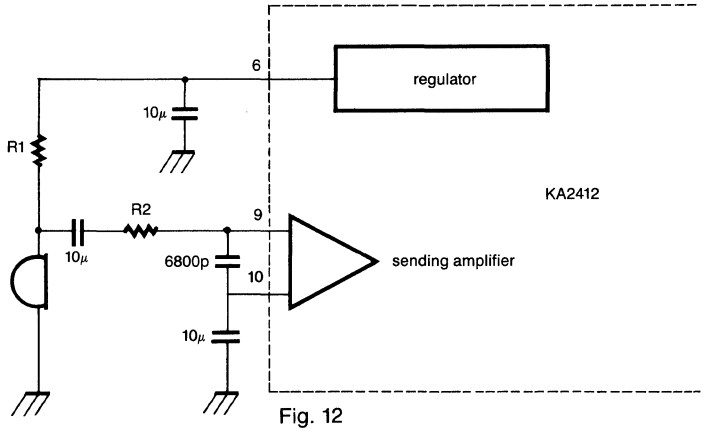


Fig. 12

2) When a microphone of condenser type is used; A perfect bias voltage have to be supplied. In this case, it can be designed as described in Fig. 12. But, in the case of other bias voltage needed, it is necessary to use a Buffer TR as described in Fig. 13.

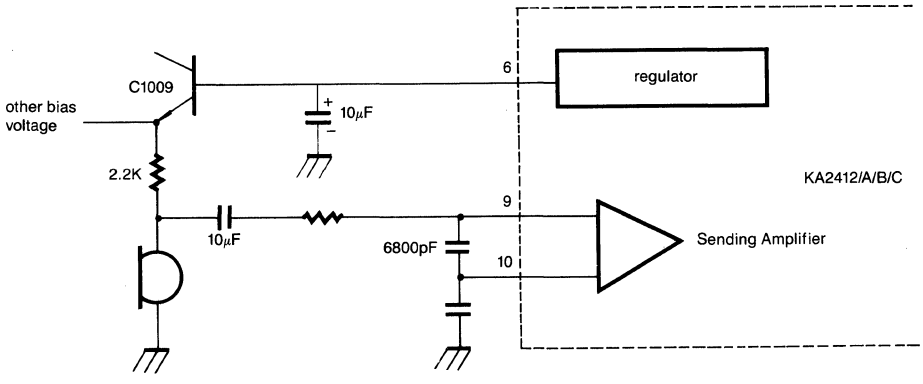


Fig. 13

4. Automatic Gain Control.

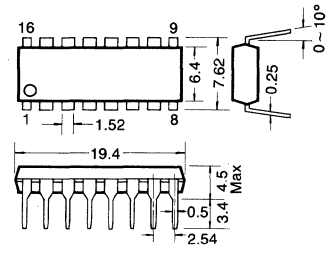
The KA2412 automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation.

Maximum gain is reached for a line current of range 10 — 20mA and minimum gain can also be reached for a line current of range 60 — 100mA.

DUAL TONE MULTI FREQUENCY GENERATOR

The KA2413 is a monolithic integrated DTMF generator designed for use in a telephone set in parallel with an electronic speech circuit. The DC characteristic to the line is set by the speech circuit.

16 Dip Unit: mm



FEATURES

- **Wide operating line voltage and current range**
- **Operates with a standard crystal at 3.58MHz**
- **Operates with a single contact or matrix key-board**
- **Levels from the high and low frequency group can be adjusted separately.**
- **No individual level adjustment is necessary for every circuit**
- **The signal levels are stabilized against variations in temperature and line voltage.**
- **Short start-up time**
- **All tones can be generated separately for testing.**
- **Easy PCB layout; all keyboard connections on one side of the chip**
- **Internal protection of all inputs**
- **Minimum number of external parts required.**

BLOCK DIAGRAM

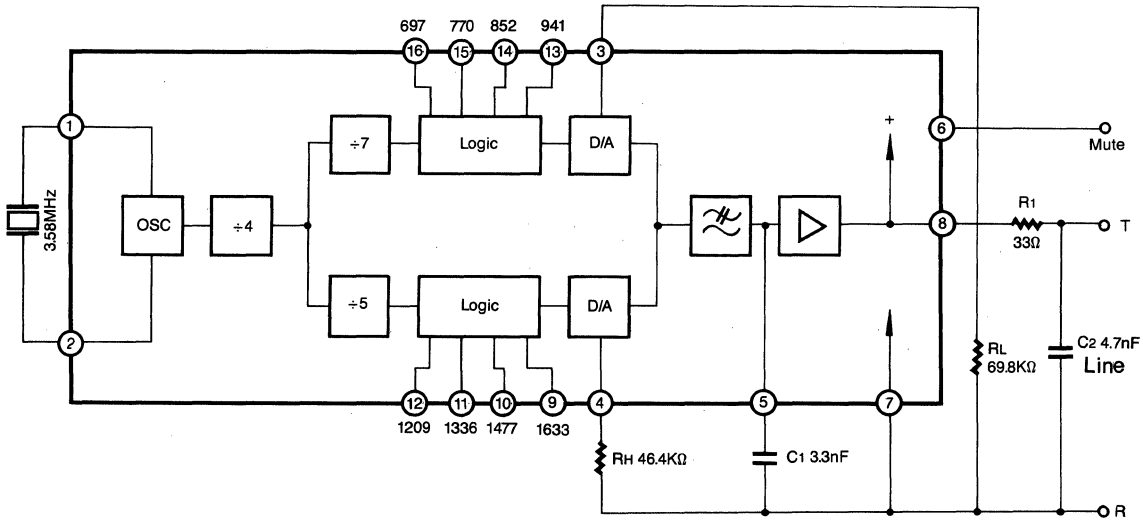


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Line Voltage (Peak) t_P=2 sec	V_L (peak)	20	V
Line Voltage (Peak) t_P=20m sec	V_L (peak)	22	V
Line Voltage (Conditions)	V_L (cont)	15	V
Power Dissipation	P_D	400	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS (T_a=25°C)

(T_a = −20°C ~ +50°C, V_L = 4.3 ~ 9V, unless otherwise specified)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Operating Line Voltage		V_L (opr)	Tone Generation 1.3 V_P Signal	4.3		9.0	V
Stand-By Line Voltage		V_L (std)	Stand-By 2.0 V_P Signal	4.3		9.0	V
Operating Line Current		I_L (opr)	V_L = 4.3V			10.0	mA
Stand-By Line Current		I_L (std)	No Key Pressed V_L = 4.3V			250	μA
Mute Current		I_M	One or More Keys Pressed	125.0			μA
Key Resistance		R_K	Key Circuit Closed			1.0	kΩ
Tone Output Frequency							
Low (Row)	f_1 = 697 Hz	Δf	f_{OSC} = 3.5795 MHz	−1.0	−0.32	+1.0	%
	f_2 = 770 Hz			−1.0	+0.02	+1.0	%
	f_3 = 852 Hz			−1.0	+0.03	+1.0	%
	f_4 = 941 Hz			−1.0	−0.11	+1.0	%
High (Column)	f_5 = 1209 Hz			−1.0	−0.03	+1.0	%
	f_6 = 1336 Hz			−1.0	−0.03	+1.0	%
	f_7 = 1477 Hz			−1.0	−0.68	+1.0	%
	f_8 = 1633 Hz			−1.0	−0.36	+1.0	%

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Signal level	High	V_H	R_H=46.4KΩ R_L=69.8KΩ	-11.0	-9.0	-7.0	dBm
	Low	V_L		-13.0	-11.0	-9.0	
	High	V_H	R_H=33.2KΩ R_L=48.7KΩ		-6.0		dBm
	Low	V_L			-8.0		
	High	V_H	R_H=26.1KΩ R_L=39.2KΩ		-4.0		dBm
	Low	V_L			-6.0		
Ratio Signal Level		V_H/V_L		1.0	2.0	3.0	dB
Impedance to Line		Z_L	Tone Generation or Stand-By	6.0 50.0			KΩ
Total Harmonic Distortion		THD	Tone Generation			-31.0	dBm
Output Noise		V_{NO}	Stand-By			-80.0	dBm
Harmonics			300 — 3400Hz			-33.0	dBm
			3.4 — 50KHz			-33.0	dBm
			≥50KHz			-80.0	dBm
Start-up Time		t_S	Output level within 1dB from final level		3	5	mS

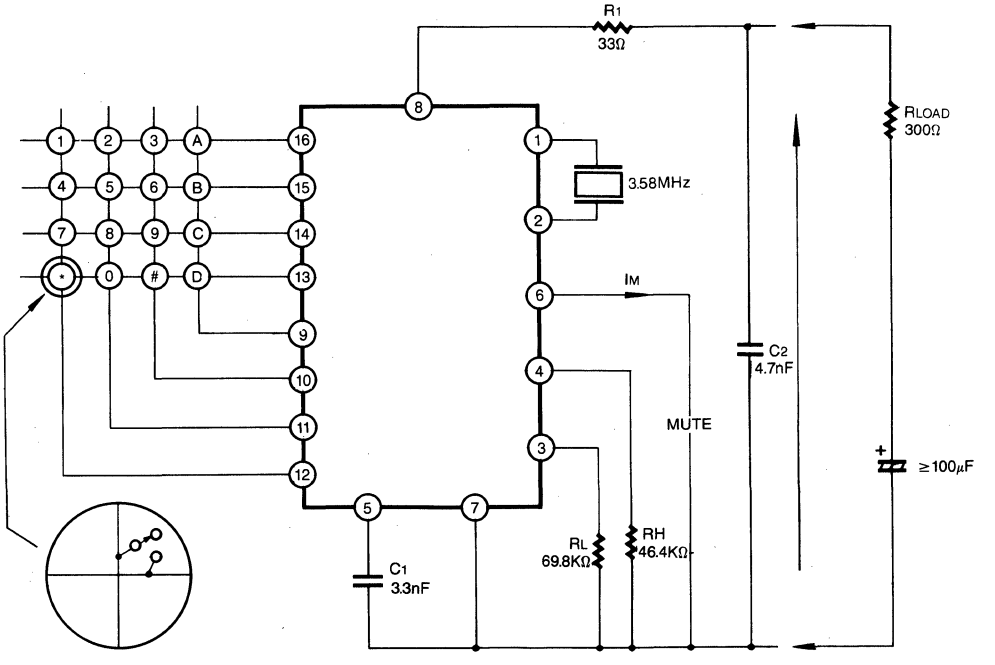


Fig. 2

- Component function:
  R1: Protecting resistor
  R_L: Signal Level (Low), R_H: Signal Level (High)
  C1: Low pass filter
  C2: Radio frequency suppresion (if used together with speech circuit with radio suppression built in, like KA2412 A/B/C, C2 is not necessary)
- To find suitable resistor values for R_H and R_L to get the desired tone levels the following formula can be used for a preliminary calculation.
  Note that in R_{Load} (f=1.4KHZ) and R_{Load} (f=800HZ) both the impedance of the line and the impedance of the speech circuit are include. V_H and V_L are the desired high and low frequency levels, in dBm

$$R_H = 56.2 \times R_{LOAD}\ (f=1.4KHz) \times 10^{-\frac{V_H}{20}}$$

$$R_L = 65.2 \times R_{LOAD}\ (f=800Hz) \times 10^{-\frac{V_L}{20}}$$

- The current consumption within KA2413 can be reduced with a resistor connected in parallel with C1. (see Fig. 3)
  If the current reduction is made too large, the output signal can be signal can be distorted by clipping.

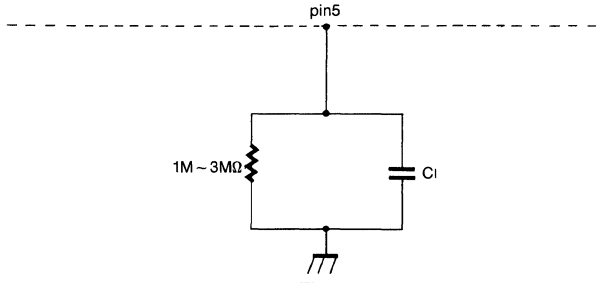


Fig. 3

- In application where a DTMF generator directly powered from the telephone line is wanted (the generator is not working in parallel with any kind of speech network),
  KA2413 can be used with a DC regulator as described in fig 4.
  These schematics give a DC regulator for the range 16 — 100mA.

DC regulator schematic

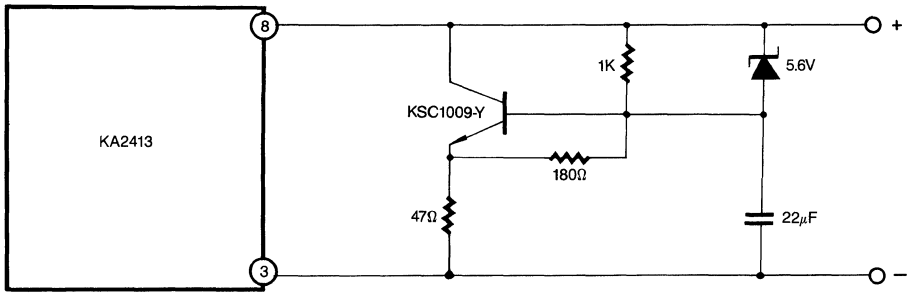


Fig. 4

KA2413 can also be controlled by a microprocessor (see Fig 5). The negative branch of the microprocessor voltage supply is connected to pin 7 of KA2413 and the inputs (8) are connected with resistors.

For tone-generating one input of the low group (pin 13 — 16) is connected to the positive voltage and one input of the high group (pin 9 — 12) is connected to the negative voltage, Then KA2413 is activated and the mute output is put in High state.

Microcomputer interface

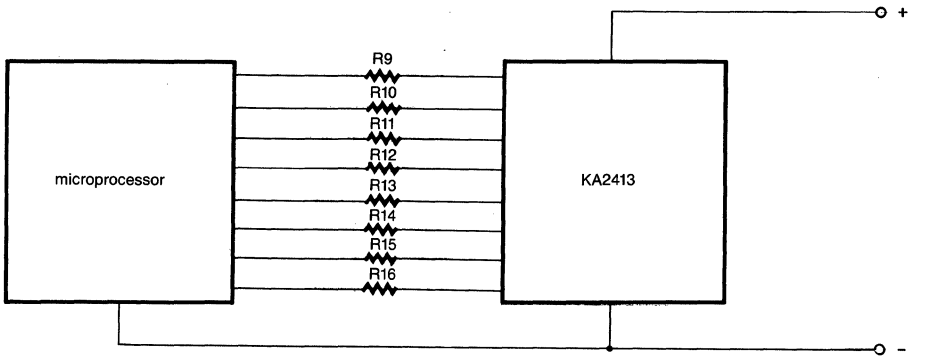


Fig. 5

1) R9, R10, R11, R12 (60K — 80K)
The resistors have two functions are:
— To raise the OFF/ON voltage
— To limit the current when the input levels are high. Too high current will interfere with the functions of the other three inputs (the resistors can be exchanged with diodes directly away from KA2413)

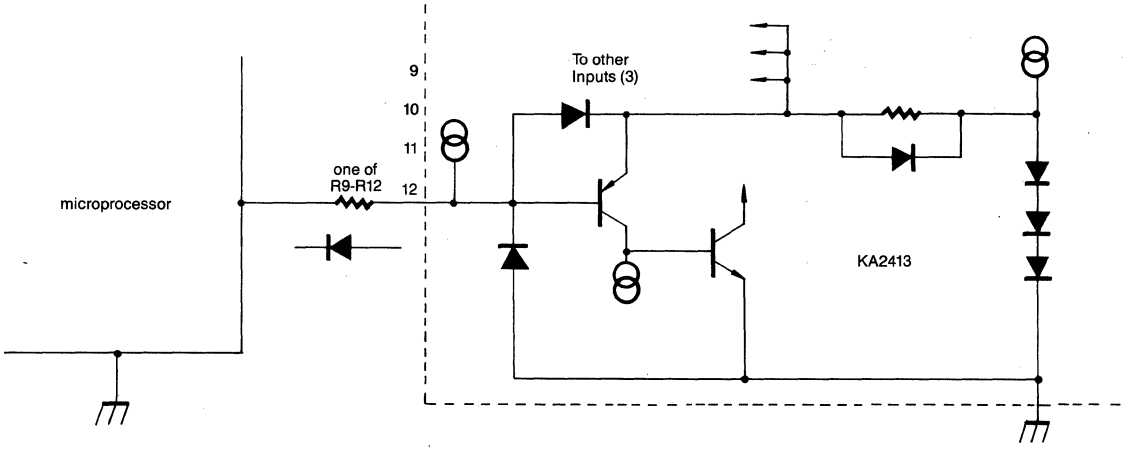


Fig. 6

2) R13, R14, R15, R16 (20K — 30K)
The two functions of the resistors are:
— To raise the OFF/ON voltage
— To limit the current when the input levels are high.

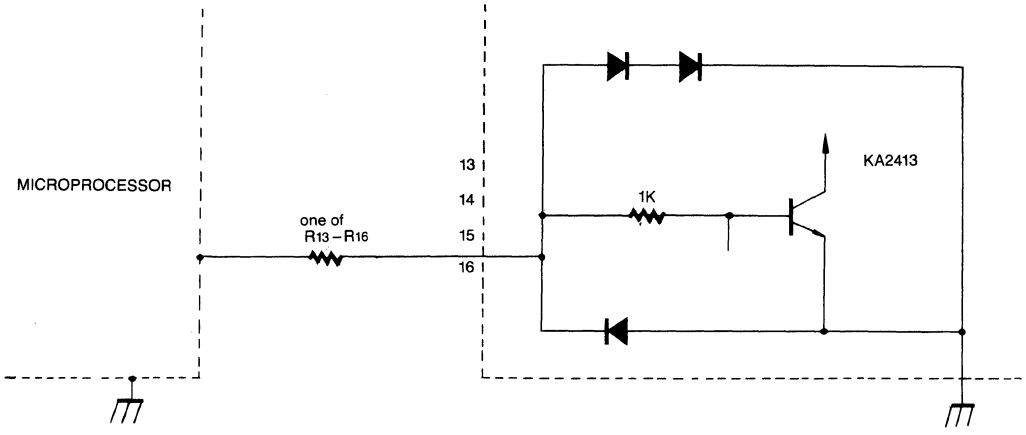
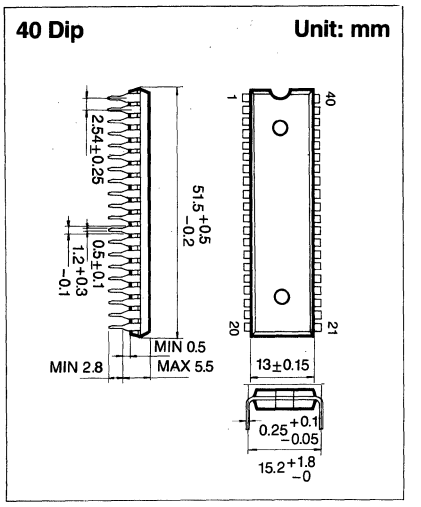


Fig. 7

ONE CHIP TELEPHONE

The KA2414/KA2417 electronic telephone circuits (ETC) Provide all the necessary elements of a tone dialing telephone in a single IC. The functional blocks of the ETC include the DTMF dialer, speech network, tone ringer, and DC line interface circuit (Fig. 1). The KA2417 also provides a microprocessor interface port that facilitates automatic dialing features.

Low voltage operation is a necessity for telephones in networks where parallel telephone connections are common. An electronic speech network operating in parallel with a conventional telephone may receive line voltage below 2.5 volts. DTMF dialers operate at similary low-line voltages when signaling through battery powered station carrier equipment. These low voltage requirements have been addressed by realizing the KA2414/KA2417 in a bipolar/I²L technology with appropriate circuit techniques. The resulting speech and dialer circuits maintain specified performance with instantaneous input voltage as low as 1.4 volts.



FEATURES

- **Provides all basic telephone station apparatus functions in a single IC, including DTMF dialer, tone ringer, speech network and line voltage regulator.**
- **DTMF generator uses Low-Cost ceramic resonator with accurate frequency synthesis technique.**
- **Tone ringer drives piezoelectric transducer and satisfies EIA RS-470 impedance signature requirements.**
- **Speech network provides two-four wire conversion with adjustable sidetone utilizing an electret transmitter.**
- **On-chip regulator insures stable operation over wide range of loop lengths.**
- **I²L technology provides low 1.4 volt operation and high static discharge immunity.**
- **KA2417 provides microprocessor interface port for automatic dialing features.**

BLOCK DIAGRAM

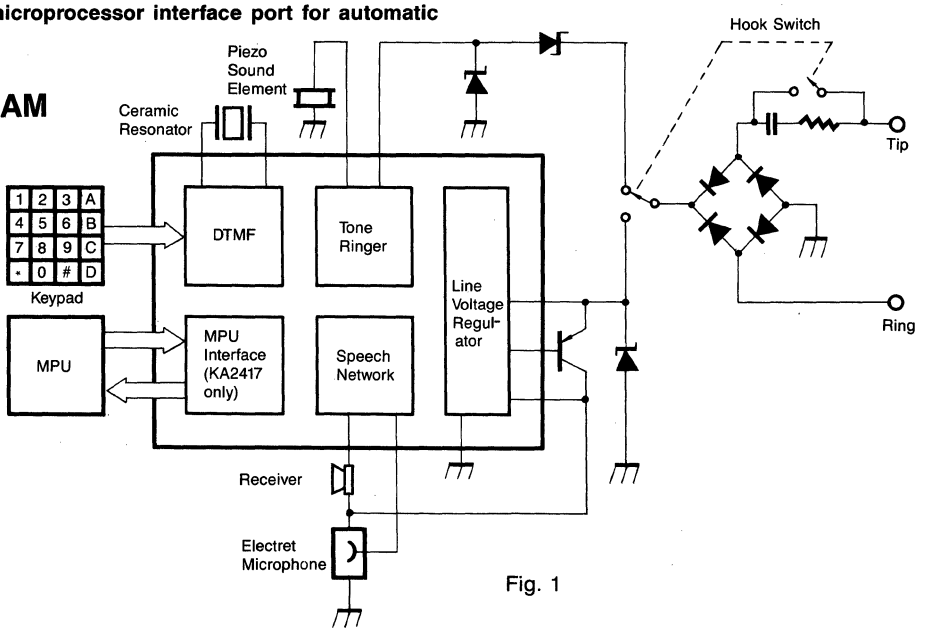


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
V⁺ Terminal Voltage (Pin 34)	V_{CC}	−1.0 ~ +20	V
VR Terminal Voltage (Pin 29)	VR	−1.0 ~ +2.0	V
RXO Terminal Voltage (Pin 27)	RXO	−1.0 ~ +2.0	V
TRS Terminal Voltage (Pin 37)	TRS	−1.0 ~ +35	V
TRO (with Tone Ringer Inactive) Terminal Voltage	TRO	−1.0 ~ +2.0	V
R_1-R_4 Terminal Current (Pins 1-4)	I_R	±100	mA
C_1-C_4 (Pins 5-8)	I_C	±100	mA
$\overline{CL}$, $\overline{TO}$, DD, I/O, A+ (KA2417 Only)		−1.0 ~ +12	V
Operating Ambient Temperature Range	T_{opr}	−20 ~ +60	°C
Stage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =5V Unless Otherwise Specified)

KEYPAD INTERFACE CIRCUIT

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Row Input Pullup Resistance m^{th} Row Terminal: m=1, 2, 3, 4	R_{RM}		4.0	8.0	11	KΩ
Column Input Pulldown Resistance n^{th} Column Terminal: n=1, 2, 3, 4	R_{CN}	V_I =1.0V	4.0	8.0	11	KΩ
Ratio of Row-to-Column Input Resistance $K_{MN}=\frac{R_{RM}}{R_{CN}}$ m=1, 2, 3, 4 / n=1, 2, 3, 4	K_{MN}		0.88	1.0	1.12	KΩ
Row Terminal Open Circuit Voltage	V_{ROC}		280	380	500	mV_{DC}
Row Threshold Voltage for m^{th} Row Terminal: m=1, 2, 3, 4	V_{RM}	Decrease from V_I =1.0V to 0.7V_{ROC}	0.7 V_{ROC}	—	—	V
Column Threshold Voltage for n^{th} Column Terminal: n=1, 2, 3, 4	V_{CN}	Increase from V_I =0V to 0.39V_{ROC}	—	—	0.39 V_{ROC}	V

*V_I: Input voltage of key board pins.

ELECTRICAL CHARACTERISTICS (Continued)

MICROPROCESSOR INTERFACE (KA2417 only)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Voltage Regulator Output A+ Rgulator	V_R/A+	V_{CC}=0.6V A+=2.4V	0.9	1.1	1.3	V
A+ Input Current Off-Hook	I_A (Off)	V_{CC}=1.4V, A+=5V	300	500	700	μA
A+ Input Current On-Hook	I_A (On)	V_{CC}=0.6V, A+=5V	4.0	6.0	9.0	MA
Input Resistance (DD, $\overline{TO}$, $\overline{CL}$)	R_{IN}	A+=5V	50	100	150	KΩ
Input Current (I/O)	I_{IN}	A+=5V, $V_{I/O}$=0.8V, V_{DD}=2V	—	80	200	μA
Input High Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	V_{IH}		2.0	—	A+	V
Input Low Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	V_{IL}		—	—	0.8	V
Output High Voltage (MS, DP, I/O)	V_{OH}	A+=5V	2.4	4.0	—	V
Output Low Voltage (MS, DP, I/O)	V_{OL}	A+=5V	—	0.1	0.4	V

LINE VOLTAGE REGULATOR

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Voltage Regulator Output	V_R	V_{CC}=1.7V	1.0	1.1	1.2	V
V+ Current in DTMF Mode	I_{DT}	V_{CC}=11.5V,R+=600Ω	8.0	12	14	mA
Change in I_{DT} with Change in V+ Voltage	ΔT_{DT}	V_{CC}=11.5~26V, R+=60Ω	—	0.8	2.0	mA
V+ Current in Speech Mode V+=1.7V V+=5.0V	I_{SP}		 3.5 8.0	 5.0 11	 7.0 15	 mA mA
Speech to DTMF Mode Current Difference	ΔI_{TR}	V+=11.5V R+=600Ω	−2.0	20	3.5	mA
LR Level Shift V+=5.0V, I_{LR}=10mA V+=18V, I_{LR}=110mA	ΔV_{LR}		 2.5 2.8	 2.9 3.3	 3.5 4.0	 V V
LC Terminal Resistance	R_{LC}		30	50	75	KΩ
Load Regulation	ΔV_R	V+=1.7v I_{BP}=0~150μA	−20	−6.0	20	mV_{AC}

ELECTRICAL CHARACTERISTICS (Continued)

SPEECH NETWORK

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
MIC Terminal Saturation Voltage	V_{MIC}	I_{MIC}=500μA, V_{MM}=0.8V	—	60	125	mV_{DC}
MIC Terminal Leakage Current	I_{MIC}	V_{MM}=2V, V_{MIC}=1V	—	0.0	5.0	μA
MM Terminal Input Resistance	R_{MM}	V_{MM}=5V	50	100	170	KΩ
TXO Terminal Bias	B_{TXO}	$B_{TXO}=V_{TXO}\div V_R$	0.46	0.53	0.62	—
TXI Terminal Input Bias Current	I_{TXI}	$I_{TXI}=(V_{TXO}-V_{TXI})\div 200K\Omega$	—	50	250	nA
TXO Terminal Positive Swing	$V_{TXO}(+)$	$I_{TXI}=-10\mu A$	—	25	60	mV_{DC}
TXO Terminal Negative Swing	$V_{TXO}(-)$	$I_{TXI}=10\mu A$		130	200	mV_{DC}
Transmit Amplifier Closed-Loop Gain	G_{TX}	V_I=3.0mV_{RMS}	16.5	19	20	V/V
Sidetone Amplifier Gain	G_{STA}	f=1.0KHz	0.41	0.45	0.55	V/V
STA Terminal Output Current	I_{STA}	V_{STA}=0.3V	50	100	250	μA
RXO Terminal Bias	B_{RXO}	$B_{RXO}=V_{RXO}\div V_R$	0.46	0.52	0.62	—
RXI Terminal Input Bias Current	I_{RXI}	$I_{RXI}=(V_{RXO}-V_{RXI})\div 100K\Omega$	—	100	400	nA
RXO Terminal Positive Swing	$V_{RXO}(+)$	$I_{RXI}=-10\mu A$ $V_{RXO}(+)=V_R-V_{RXO}$	—	1.0	20	mV_{DC}
RXO Terminal Negative Swing	$V_{RXO}(-)$	$I_{RXI}=+10\mu A$ $V_{RXO}(-)=V_{RXO}$	—	40	100	mV_{DC}
TXL Terminal Off Resistance	R_{TXL} (Off)	V_{TXL}=0.4V_{DC}	125	200	300	KΩ
TXL Terminal On Resistance	R_{TXL} (On)		—	20	100	Ω
RM Terminal Off Resistance	R_{RM} (Off)	V_{RM}=0.4V_{DC}	125	180	300	KΩ
RM Terminal On Resistance	R_{RM} (On)		410	570	770	Ω

DTMF GENERATOR (V_L=15V, R_L=600Ω)

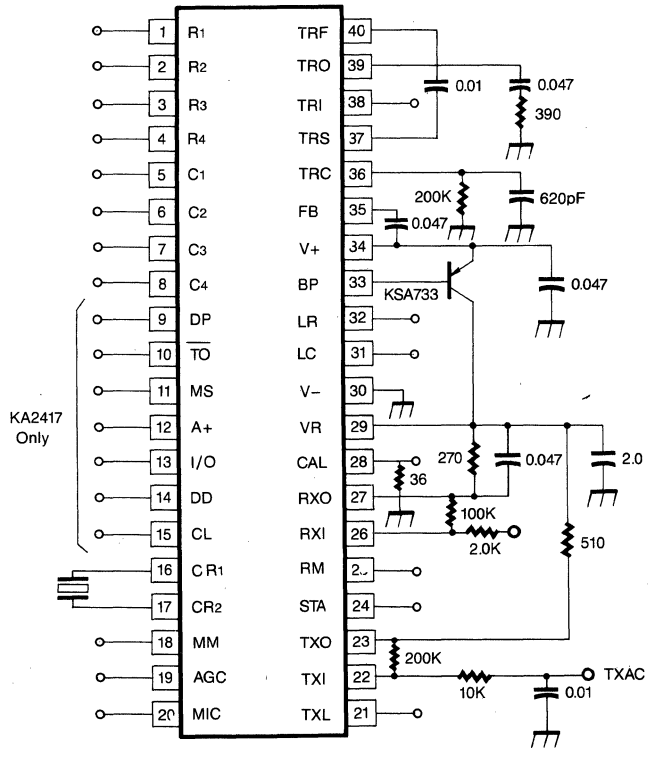
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Row Tone Frequency Row 1	f_{R1}		692.9	696.4	699.9	Hz
Row 2	f_{R2}	V_{CC}=15V	765.3	769.2	773.0	Hz
Row 3	f_{R3}	R+=600Ω	848.9	853.2	857.5	Hz
Row 4	f_{R4}		935.1	939.8	944.5	Hz
Column Tone Frequency Column 1	f_{C1}		1201.6	1207.7	1213.7	Hz
Column 2	f_{C2}	V_{CC}=15V	1330.2	1336.9	1343.6	Hz
Column 3	f_{C3}	R+=600Ω	1471.9	1479.3	1486.7	Hz
Column 4	f_{C4}		1625.2	1633.4	1641.5	Hz
Row Tone Amplitude	V_{ROW}	V_{CC}=15V, R+=600Ω	0.34	0.39	0.50	V_{RMS}
Column Tone Amplitude	V_{CO1}	V_{CC}=15V, R+=600Ω	0.43	0.48	0.62	V_{RMS}
Column Tone Pre-emphasis	dB_{CR}	V_{CC}=15V, R+=600Ω	0.5	1.8	3.0	dB
DTMF Distortion	THD		—	4.0	6.0	%
DTMF Output Resistance	R_O	V_{FB}=1.8~2.8V	1.0	2.5	3.0	KΩ

ELECTRICAL CHARACTERISTCS (Continued)

TONE RINGER (V_{TRI}=20V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
TRI Terminal Voltage	V_{TRI}	$I_{TRC}+I_{TRS}$=1.0mA	20	21.5	23	V_{DC}
TRS Terminal Input Current V_{TRS}=24V V_{TRS}=30V	I_{TRS}	V_{TRI}=20V	 70 0.4	 120 0.8	 170 1.5	 μA mA
TRF Threshold Voltage	V_{TRF}	V_{TRI}=20V	1.2	1.6	1.9	V_{DC}
TRF Threshold Hysteresis	ΔV_{TRF}	V_{TRI}=20V	100	200	400	mV_{DC}
TRF Filter Resistance	R_{TRF}	V_{TRF}=21V, R_{TRF}=1.0÷I_{TRA}	30	50	75	KΩ
High Tone Frequency Low Tone Frequency Warble Frequency	f_H f_L f_W		920 736 11.5	1000 800 12.5	1080 864 13.5	Hz Hz Hz
Tone Ringer Output Voltage	V_O (p-p)	V_{TRS}=22V, V_{TRI}=20V	18	20	22	V_{P-P}

TEST CIRCUIT



Notes:
1. *Selected ceramic resonator: 500KHz±0.2KHz
2. Capacitances in μF unless noted.
3. All resistances in ohms.

Fig. 2

PIN DESCRIPTION

(See Fig. 12 for external component identifications.)

Pin	Designation	Function
1-4	R1-R4	Keypad inputs for Rows 1 through 4. When open, internal 8.0 kΩ resistors pull up the row inputs to a regulated (= 0.5 volt) supply. In normal operation, a row and a column input are connected through a SPST switch by the telephone keypad. Row inputs can also be activated by a Logic "0" (< 250 mV) from a microprocessor port.
5-8	C1-C4	Keypad inputs for Columns 1 through 4. When open, internal 8.0 kΩ resistors pull down the column inputs to V– in normal operation, connecting any column input to any row input produces the respective row and column DTMF tones. In addition to being connected to a row input, column inputs can be activated by a Logic "1" (> 250 mV and < 1.0 volt).
9	DP*	Depressed Pushbutton (Output) — Normally low: A Logic "1" indicates one and only one, button of the DTMF keypad is depressed.
10	$\overline{TO}$*	Tone Output (Input) — When a Logic "1", disables the DTMF generator. Keypad is not disabled.
11	MS*	Mute/Single Tone (Output) — A Logic "1" indicates a row and/or column tone is being generated. A Logic "0" indicates tone generator is disabled.
12	A+ *	MPU Power Supply (input) — Enables pullups on the microprocessor section outputs. Additionally, this voltage will power the entire circuit (except Tone Ringer) in the absence of voltage at V+.
13	I/O*	Input/Output — Serial Input or Output data (determined by DD input) to or from the microprocessor for storing or retrieving telephone numbers. Guaranteed to be a Logic "1" on powerup if DD=Logic "0."
14	DD*	Data Direction (Input) — Determines direction of data flow through I/O pin. As a Logic "1," I/O is an input to the DTMF generator. As a Logic "0." I/O outputs keypad entires to the microprocessor.
15	$\overline{CL}$*	Clock (Input) — Serially shifts data in or out of I/O pin. Data is transferred on negative edge typically at 20 kHz.
16, 17	CR1, CR2	Ceramic Resonator oscillator input and feedback terminals, respectively. The DTMF dialer is intended to operate with a 500 kHz ceramic resonator from which row and column tones are synthesized.
28	CAL	Amplitude CALibration terminal for DTMF dialer. Resistor R14 from the CAL pin to V — controls the DTMF output signal level at Tip and Ring.
35	FB	Feed Back terminal for DTMF output. Capacitor C14 connected from FB to V+ provides ac feedback to reduce the output impedance to Tip and Ring when tone dialing.
29	VR	Voltage Regulator output terminal. VR is the output of a 1.1 volt voltage regulator which supplies power to the speech network amplifiers and DTMF generator during signaling. To improve regulator efficiency at low line current conditions, an external PNP pass-transistor T1 is used in the regulator circuit. Capacitor C9 frequency compensates the VR regulator to prevent oscillation.
33	BP	Base of a PNP Pass-transistor. Under long-loop conditions where low line voltages would cause VR to fall below 1.1 volts, BP drives the PNP transistor T1 into saturation, thereby minimizing the voltage drop across the pass transistor. At line voltages which maintain VR above. 1.1 volts, BP biases T1 in the linear region thereby regulating the VR voltage. Transistor T1 also couples the ac speech signals from the transmit amplifier to Tip and Ring at V_{CC}.

*KA2417 only

(continued)

PIN DESCRIPTION (Continued)

(See Fig. 12 for external component identifications.)

Pin	Designation	Function
34	V+	The more positive input to the regulator, speech, and DTMF sections connected to Tip and Ring through the polarity guard diode bridge.
30	V–	The dc common (more negative input) connected to Tip and Ring through the polarity guard bridge.
32	LR	DC Load Resistor, Resistor R4 from LR to V– determines the dc input resistance at Tip and Ring. This resistor is external not only to enable programming the dc resistance but also to avoid high on-chip power dissipation with short telephone lines. It acts as a shunt load conducting the excess dc line current. At low line voltages (< 3.0 volts), no current flows through LR.
31	LC	DC Load Capacitor. Capacitor C11 from LC to V– forms a low-pass filter which prevents the resistor at LR from loading ac speech and DTMF signals.
20	MIC	MiCrophone negative supply terminal. The dc current from the electret microphone is returned to V– through the MIC terminal which is connected to the collector of an on-chip NPN transistor. The base of this transistor is controlled either internally by the mute signal from the DTMF generator, or externally by the logic input pin MM.
18	MM	Microphone Mute. The MM pin provides a means to mute the microphone in response to a digital control signal. When this pin is connected to a Logic "1" (> 2.0 V) the microphone dc return path through the MIC terminal is disabled.
22	TXI	Transmit amplifier Input. TXI is the input to the transmit amplifier from an electret microphone. AC coupling capacitors allow the dc offset at TXI to be maintained approximately 0.6V above V– by feedback through resistor R11 from TXO.
21	TXL	Transmit Input Limiter. An internal variable resistance element at the TXL terminal controls the transmitter input level to prevent clipping with high signal levels. Coupling capacitors C4 and C5 prevent dc curent flow through TXL. The dynamic range of the transmit peak limiter is controlled by resistors R12 and R13.
23	TXO	Transmit Amplifier Output. The transmit amplifier output drives ac current through the voltage regulator pass-transistor T1 via resistor R10. The dc bias voltage at TXO is typically 0.6 volts above V–. The transmit amplifier gain is controlled by the R11/(R12+R13) ratio.
19	AGC	Automatic Gain Control low-pass filter terminal. Capacitor C3 connected between AGC and VR sets the attack and decay time of the transmit limiter circuit. This capacitor also aids in reducing clicks in the receiver due to hook-switch transients and DTMF on/off transients. In conjunction with internal resistors, C3 (1.0μF) forms a timer which mutes the receiver amplifier for approximately 20 milliseconds after the user goes off-hook or releases a DTMF Key.
27	RXO	Receiver Amplifier Output. This terminal is connected to the open-collector NPN output transistor of the receiver amplifier. DC bias current for the output device is sourced through the receiver from VR. The bias voltage at RXO is typically 0.6 volts above the V–. Capacitor C10 from RXO to VR provides frequency compensation for the receiver amplifier.
26	RXI	Receiver Amplifier Input. RXI is the input terminal of the receiver amplifier which is driven by ac signals from V+ and STA. Input coupling capacitor C8 allows RXI to be biased approximately 0.6 volts above the V– via feedback resistor R6.
25	RM	Receiver Amplifier Mute. A switched resistance at the RM terminal attenuates the receiver amplifier input signal produced by DTMF dialing tones at V+, RM also mutes clicks at the receiver which result from keypad or hook switch transitions. The ac resistance at RM is typically 540Ω in the mute mode and 200kΩ otherwide. Coupling capacitors C7 and C8 prevent dc current flow through RM.

* KA2417 only

(continued)

PIN DESCRIPTION (Continued)

(See Fig. 12 for external component dentifications.)

Pin	Designation	Function
24	STA	Side Tone Amplifier output STA is the output of the sidetone inverter amplifier whose input is driven by the transmit signal at TXO. The inverted transmit signal from STA subtracts from the receiver amplifier input current from V+, thus reducing the receiver sidetone level. Since the transmitted signal at V+ is phase shifted with respect to TXO by the reactive impedance of the phone line, the signal from STA must be similarly phase-shifted in order to provide adequate sidetone reduction. This phase relationship between the transmit signal at TXO and the sidetone cancellation signal from STA is controlled by R8, R9, and C6.
37	TRS	Tone Ringer Input Sense. TRS is the most positive input terminal of the tone ringer and the reference for the threshold detector.
38	TRI	Tone Ringer Input terminal. TRI is the positive supply voltage terminal for tone ringer circuitry. Current is supplied to TRI through resistor R2. When the average voltage across R2 exceeds an internal reference voltage (typically 1.6 volts) the tone ringer output is enabled.
40	TRF	Tone Ringer Input filter capacitor terminal. Capacitor C1 connected from TRF to TRS forms a low-pass filter. This filter averages the signal across resistor R2 and presents this dc voltage to the input of the threshold detector. Line voltage transients are rejected if the duration is insufficient to charge C1 to 1.6 volts.
36	TRC	Tone Ringer oscillator Capacitor and resistor terminal. The relaxation oscillator frequency f_O is set by resistor R3 and capacitor C13 connected from TRC to V−. Typically, $f_O = (R3C13 + 8.0\mu s)^{-1}$.
39	TRO	Tone Ringer Output terminal. The frequency of the square wave output signal at TRO alternates from $f_O/8$ to $f_O/10$ at a warble rate of $f_O/640$. Typical output frequencies are 1000 Hz and 800 Hz with a 12.5 Hz warble rate. TRO sources or sinks up to 20 mA to produce an output voltage swing of 18 volts peak-to-peak across the piezo transducer. Tone ringer volume control can be implemented by a variable resistor in series with the piezo transducer.

GENERAL CIRCUIT DESCRIPTION

LINE VOLTAGE REGULATOR

The DC line interface circuit (Fig 3) determines the DC input characteristic of the telephone. At low input voltage (less than 3 Volts) the ETC draws only the speech and dialer bias currents through the VR regulator. As input voltage increase, Q_1 conducts the excess DC line current through resistor R_4. The 1.5 Volt level shift prevents saturation of Q_2 with telephone line signals up to 2.0 Volts peak (+5.2 dBm). A constant current (dummy load) is switched off when the DTMF dialer is activated to reduce line current transients. Figure 4 inustrates the DC voltage/current characteristic of a KA2414/KA2417.

DC LINE INTERFACE BLOCK DIAGRAM

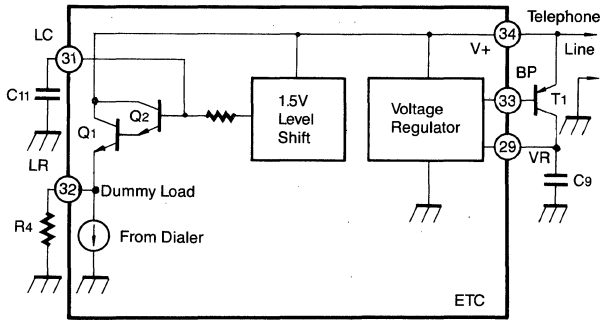


Fig. 3

DC V-I CHARACTERISTIC OF ETC

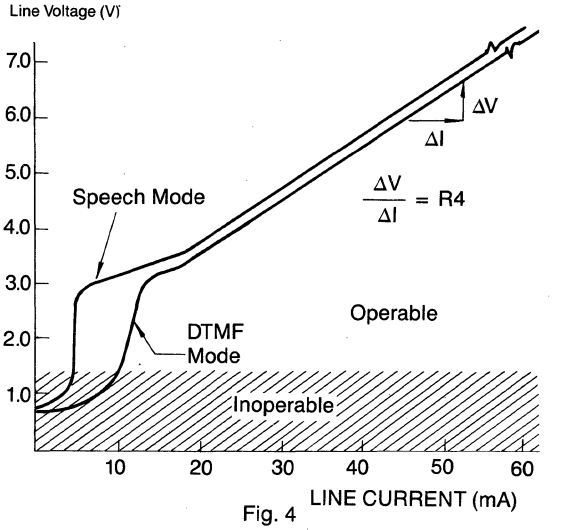


Fig. 4

SPEECH NETWORK

The speech network (Figure 5) provides the two-to-four wire interface between the telephone line and the instrument's transmitter and receiver. An electret microphone biased from VR drives the transmit amplifier. For very loud talkers, the peak limiter circuit reduces the transmit input level to maintain low distortion. The transmit amplifier output signal is inverted at the STA terminal and driven through an external R-C network to control the receiver sidetone level. The switched AC resistance at the RM terminal reduces receiver signal when dialing and suppresses clicks due to hook or keypad switch transitions. When transmitting, audio signal currents (i_{TXO} and i_{RXO}) flow through the voltage regulator pass transistor (T1) to drive the telephone line. This feature has two consequences: 1) in the transmitting mode the receiver sidetone current i_{RXO} contributes to the total signal on the line along with i_{TXO}: 2) The AC impedance of the telephone is determined by the receiver impedance and the voltage gain from the line to the receiver amplifier output.

SPEECH NETWORK BLOCK DIAGRAM

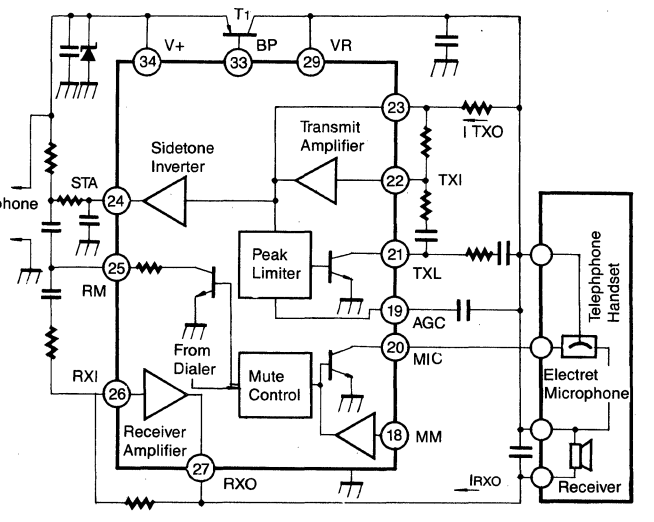


Fig. 5

DTMF DIALER

Keypad interface comparators activate the DTMF row and column tone generators (Figure 6) when a row and column input are connected through a SPST keypad. The keypad interface is designed to function with contact resistances up to 1.0 kΩ and leakage resistances as low as 150 kΩ. Single tones may be initiated by depressing two keys in the same row or column.

The programmable counters employ a novel design to produce non-integer frequency ratios. The various DTMF tones are synthesized with frequency division errors less than ±0.16% (Table 1). Consequently an inexpensive ceramic resonator can be used instead of a quartz crystal as the DTMF frequency reference. Total frequency error less than ±0.8% can be achieved with ±0.3% ceramic resonator. The row and column D/A converters produce 16-step approximations of sinusoidal waveforms. Feedback through terminal FB reduces the DTMF output impedance to approximately 2.0 kΩ to satisfy return loss specifications.

DTMF DIALER BLOCK DIAGRAM

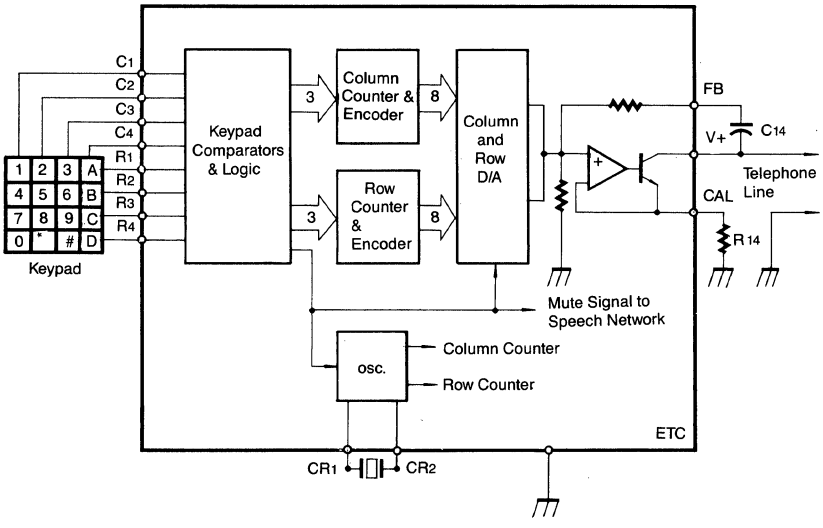


Fig. 6

TONE RINGER

The tone ringer (Figure 7) generates a warbling square wave output drive to a piezo sound element when the AC line voltage exceeds a predetermined threshold level. The threshold detector uses a current mode comparator to prevent on/off chatter when the output current reduces the voltage available at the ringer input. When the average current into the tone ringer exceeds the threshold level, the ringer output TRO commences driving the piezo transducer. This output current sourced from TRI increases the average current measured by the threshold detector. As a result, hysteresis is produced between the tone ringer on and off thresholds. The output frequency at TRO alternates between $f_o/8$ and $f_o/10$ at a warble rate of $f_o/640$, where f_o is the ringer oscillator frequency.

TONE RINGER BLOCK DIAGRAM

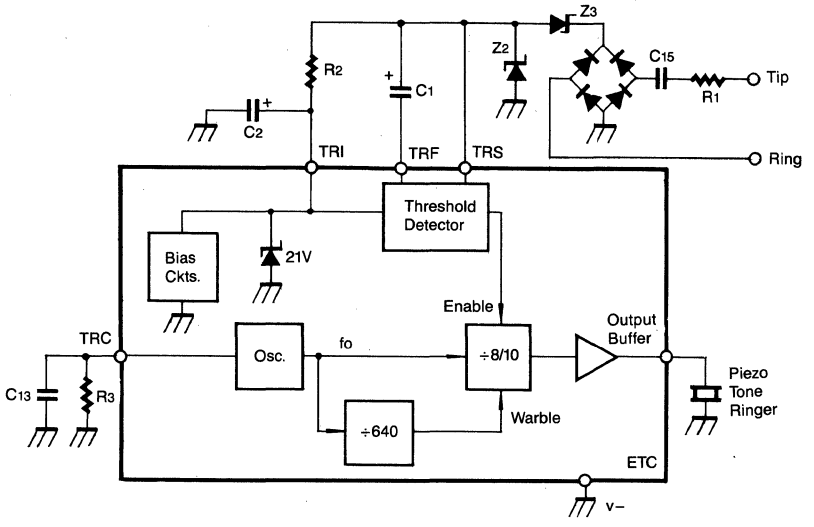


Fig. 7

MICROPROCESSOR INTERFACE (KA2417 ONLY)

The MPU interface connects the keypad and DTMF sections of the ETC to a microprocessor for storing and retrieving numbers to be dialed. Figure 8 shows the major blocks of the MPU interface section and the interconnections between the keypad interface, DTMF generator and microprocessor. Each button of a 12 or 16 number keypad is represented by a four-bit code (Figure 9). This four-bit code is used to load the programmable counters to generate the appropriate row and column tones. The code is transferred serially to or from the micdroprocessor when the shift register is clocked by the microprocessor. Data is transferred through the I/O terminal, and the direction of data flow is determined by the Data Direction (DD) input terminal. In the manual dialing mode, DD is a logic "0" and the four-bit code from the keypad is fed to the DTMF generator by the digital multiplexer and also output on the I/O terminal through the four-bit shift register. The data sequence on the I/O terminal is B3, B2, B1, B0 and is transferred on the negative edge of the clock input ($\overline{CL}$). In this mode the shift register load enable circuit cycles the register between the load and read modes such that multiple read cycles may be run for a single-key closure. Six complete clock cycles are required to output data from the ETC and reload the register for a second look.

In the automatic dialing mode, DD is a Logic "1" and the four-bit code is serially entered in the sequence B3, B2, B1, B0 into the four-bit shift register. Thus, only four clock cycles are required to transfer a number into the ETC. The keypad is disabled in this mode. A Logic "1" on the Tone Output ($\overline{TO}$) will disable tone outputs until valid data from the microprocessor is in place. Subsequently $\overline{TO}$ is switched to a Logie "0" to enable the DTMF generator. Figures 10 and 11 show the timing waveforms for the manual and automatic dialing modes and Table 2 specifies timing limitations.

The keypad decoder's exclusive OR circuit generates the DP and MS output signals. The DP output indicates (when at a Logic "1") that one, and only one, key is depressed, thereby indicating valid data is available to the MPU. The DP output can additionally be used to initiate a data transfer sequence to th microprocessor. The MS output (when at a Logic "1") indicates the DTMF generator is enabled and the speech network is muted.

Pin A+ is to be connected to a source of 2.5 to 10 volts (generally from the microprocessor circuit) to enable the pullup circuits on the microprocessor interface outputs (DP, MS, I/O). Additionally, this voltage will power the entire circuitry (except Tone Ringer) in the absence of voltage at V+. This permits use of the transmit and receive amplifiers, keypad interface, and DTMF generator for non-typical telephone functions.

MICROPROCESSOR INTERFACE BLOCK DIAGRAM (KA2417 ONLY)

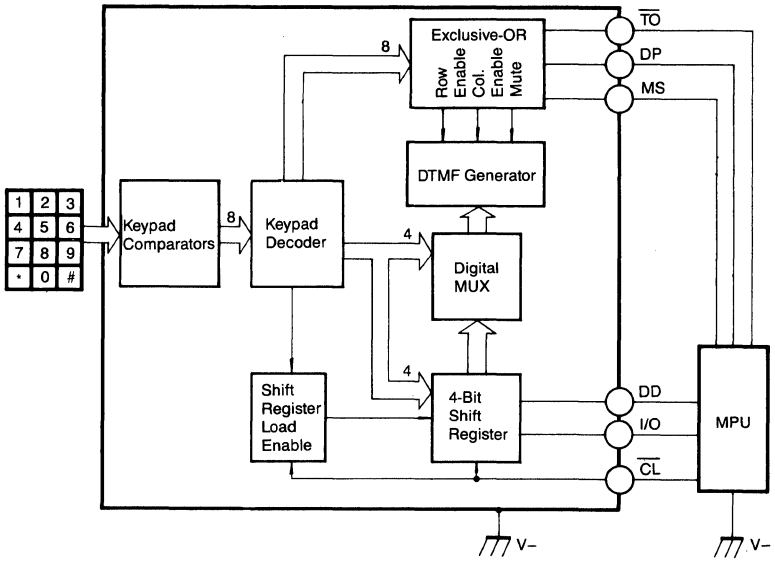
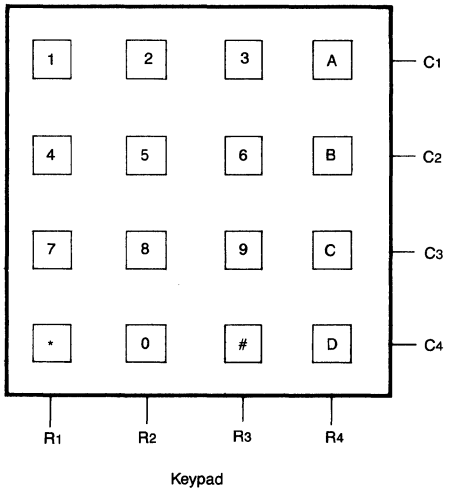


Fig. 8

MPU INTERFACE CODES



Key	Row	Column	Code (B3 ~ B0)
1	1	1	1111
2	1	2	0111
3	1	3	1011
4	2	1	1101
5	2	2	0101
6	2	3	1001
7	3	1	1110
8	3	2	0110
9	3	3	1010
0	4	2	0100
A	1	4	0011
B	2	4	0001
C	3	4	0010
D	4	4	0000
*	4	1	1100
#	4	3	1000

Fig. 9

OUTPUT DATA CYCLE FROM KA2417

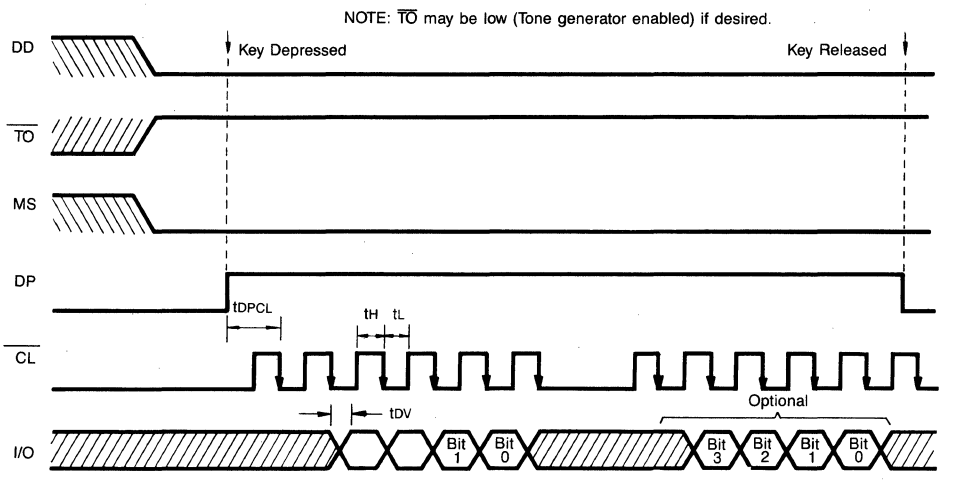


Fig. 10

INPUT DATA CYCLE TO KA2417

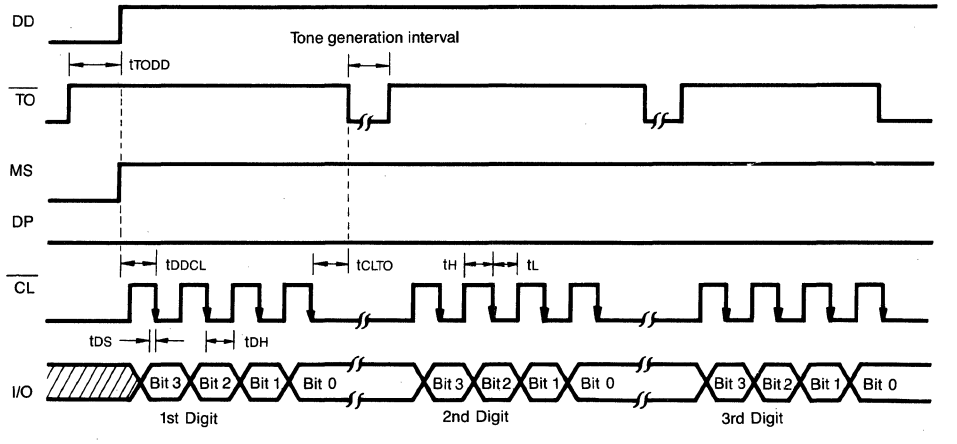


Fig. 11

TABLE 1 — FREQUENCY SYNTHESIZER ERRORS

	DTMF Standard (Hz)	Tone Output Frequency with 500KHz Oscillator	% Deviation from Standard
Row 1	697	696.4	−0.086
Row 2	770	769.2	−0.104
Row 3	852	853.2	+0.141
Row 4	941	939.8	−0.128
Column 1	1209	1207.7	−0.108
Column 2	1336	1336.9	+0.067
Column 3	1477	1479.3	+0.156
Column 4	1633	1634.0	+0.061

TABLE 2 — TIMING LIMITATIONS

Symbol	Parameter	Min	Typ	Max	Unit	Ref
f_{CL}	Clock Frequency	0	20	30	kHz	
t_H	Clock High Time	15	—	—	μs	Figs. 10, 11
t_L	Clock Low Time	15	—	—	μs	Figs. 10, 11
t_r, t_f	Clock, Rise, Fall Time	—	—	2.0	μs	
t_{DV}	Clock Transition to Data Valid	—	—	10	μs	Fig. 10
t_{DPCL}	Time from DP High to CL Low	20	—	—	μs	Fig. 10
t_{DDCL}	Time from DD High to CL Low	20	—	—	μs	Fig. 11
t_{DS}	Data Set-up Time	10	—	—	μs	Fig. 11
t_{DH}	Data Hold Time	10	—	—	μs	Fig. 11
t_{CLTO}	Time from CL Low to TO Low	10	—	—	μs	Fig. 11
t_{TODD}	Time from TO High to DD High	20	—	—	μs	Fig. 11

APPLICATIONS INFORMATION

Fig 12 specifies a typical application circuit for the KA2414 and KA2417.

Complete listing of external components are provided at the end of this section along with nominal component values.

The hook switch and polarity guard bridge configuration in Fig. 12 is one of several options. If two bridges are used, one for the tone ringer and the other for speech and dialer circuits, then the hook switch can be simplified. Component values should be varied to optimize telephone performance parameters for each application. The relationships between the application circuit components and certain telephone parameters are briefly described in the following:

On-Hook Input Impedance.

R1, C15, and Z3 are significant components for on-hook impedance. C15 dominates at low freguencies, R1 at high frequencies and Z3 provides the non-linearity required for 2.5v and 10v impedance signature tests. C15 must generally be ®1.0μF to satisfy 5.0HZ impedance specifications.

Tone Ringer Output Frequencies

R3 and C13 control the frequency (fo) of a relaxation oscillator.

Typically fo= $(R3\,C13 + 8.0\mu S)^{-1}$. The output tone frequencies are fo/10 and fo/8. The warble rate is fo/640. The tone ringer will operate with fo from 1.0KHz to 10KHz. R3 should be limited to values between 150K and 300K.

Tone Ringer Input Threshold

After R1, C15, and Z3 are chosen to satisfy on-hook impedance specifications, R2 is chosen for the desired ring start threshold.

Increasing R2 reduces the ac input voltage required to activate the tone ringer output. R2 should be limited to values between 0.8K and 2.0KΩ.

Off-Hook DC Resistance

R4 conducts the dc line current in excess of the speech and dialer bias current. Increasing R4 increases the input resistance of the telephone for line currents above 10mA. R4 should be selected between 40Ω and 120Ω.

Off-Hook AC Impedance

The ac input impedance is equal to the receive amplifier load impedance (at RXO) divided by the receive amplifier gain (voltage gain from V+ to RXO). Increasing the impedance of the receiver increases the impedance of the telephone.

Increasing the gain of the receiver amplifier decreases the impedance of the telephone.

DTMF Output Amplitude

R14 controls the amplitude of the row and column DTMF tones. Decreasing R14 increases the level of tone amplitudes is internally fixed R14 should be greater than 20Ω to avoid excessive current in the DTMF output amplifier.

Transmit Output Level

R10 controls the maximum signal amplitude produced at V+ by the transmit amplifier. Decreasing R10 increases the transmit output signal at V+. R10 should be greater than 250Ω to limit current in the transmit amplifier output.

Transmit Gain

The gain from the microphone to the telephone line varies directly with R11. Increasing R11 increases the signal applied to R10 and the ac current driven through R10 to the telephone line. The closed loop-gain from the microphone to the TXO terminal should be greater than 10 to prevent transmit amplifier oscillations.

Note: Adjustments to transmit level and gain are complicated by the addition of receiver sidetone current to the transmit amplifier output current at V+. Normally the sidetone current from the receiver will increase the transmit signal (if the current in the receiver is in phase with in R10). Thus the transmit gain and sidetone levels cannot be adjusted independently.

Receiver Gain

Feedback resistor R6 adjusts the gain at the receiver amplifier. Increasing R6 increases the receiver amplifier gain.

Sidetone Level

Sidetone reduction is achieved by the cancellation of receiver amplifier input signals from R9 and R5. R8, R15, and C6 determine the phase of the sidetone balance signal in R9. The ac voltage at the junction of R8 and R9 should be 180° out of phase with the voltage at V+. R9 is selected such that the signal current in R9 is slightly greater than that in R5. This insures that the sidetone current in the receiver adds to the transmit amplifier output current.

Hook-Switch Click Suppression

When the telephone is switched to the off-hook condition C3 charges from 0 volts to a 300mV bias voltage.

During this time interval, receiver clicks are suppresed by a low impedance at the RM terminal. If this click suppression mechanism is desired during a rapid succession of hook switch transitions, than C3 must be quickly discharged when the telephone is on-hook. R16 and S3 provide rapid discharge path for C3 to reset the click suppression timer. R16 is selected to limit the discharge current in S3 to prevent damage to switch contacts.

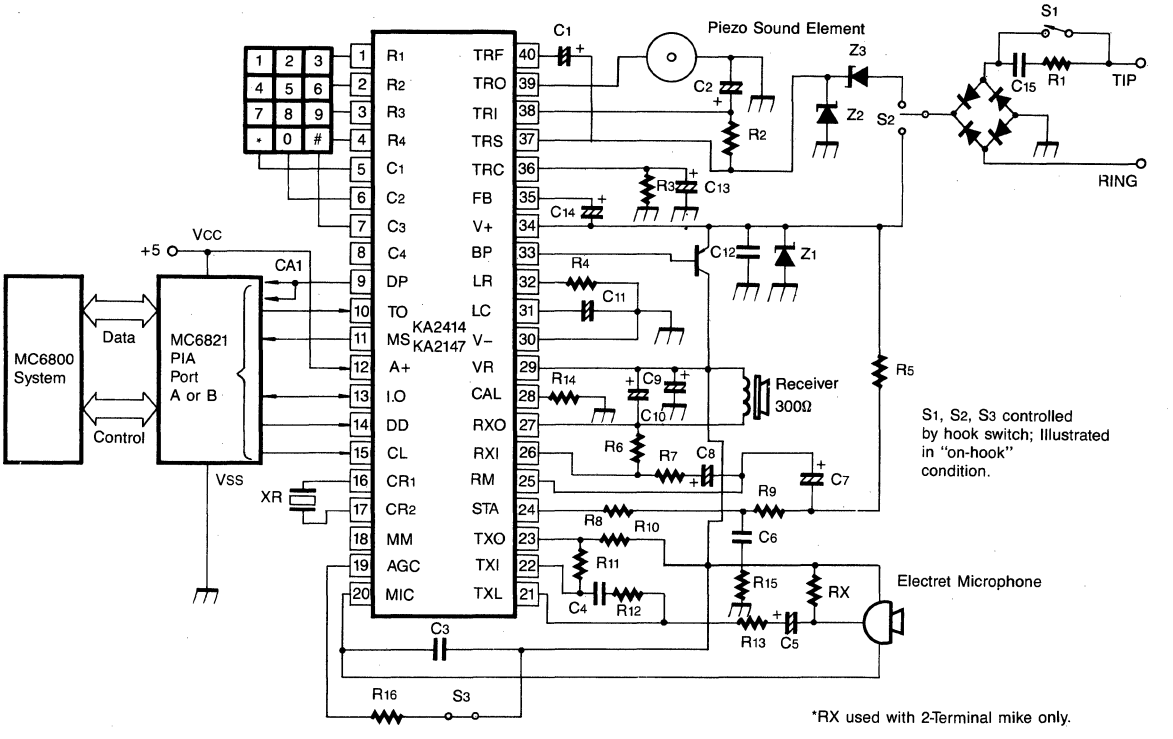
Microprocessor Interface (KA2417 only)

The six microprocessor interface lines (DP, $\overline{TO}$, MS, DD, I/O, and $\overline{CL}$) can be connected directly to a port, as shown in Fig 12. The DP line (Depressed Pushbutton) is also connected to an interrupt line to signal the microprocessor to begin a read data sequence when storing a number into memory. The KA2417 clock speed requirement is slow enough (typically 20KHZ) so that it is not necessary to divide down the processor's system clock, but rather a port output can be toggled. This facilitates synchronizing the clock and data transfer, eliminating the need for hardware to generate the clock.

The DD pin must be maintained at a logic "0" when the microprocessor section is not in use, so as to permit normal operation of the keypad.

When the microprocessor interface section is not in use, the supply voltage at pin 12 (A+) may be disconnected to conserve power. Normally the speech circuity is powered by the voltage supplied time, A+ powers only the active pullups on the three microprocessor outputs (DP, MS, and I/O). When the telephone is "on-hook", and V+ falls bellow 0.6 volts, power is then supplied to the telephone speech and dialer circuitry from A+. Powering the circuit from the A+ pin permits communication with a microprocessor, and/or use of the transmit and receiver amplifiers, while the telephone is "on-hook".

APPLICATION CIRCUIT



*pins 9 through 15 are for KA2417 only; corresponding pins on KA2414 should be connected to V−.

Fig. 12

EXTERNAL COMPONENTS

(Component labels referenced to Fig. 12)

Capacitors	Nominal Value	Description
C1	1.0μF, 10V	Tone ringer filter capacitor: integrates the voltage from current sense resistor R2 at the input of the threshold detector.
C2	4.7μF, 25V	Tone ringer input capacitor: filters the rectified tone ringer input signal to smooth the supply potential for oscillator and output buffer.
C3	1.0μF, 3.0V	Transmit limiter low-pass filter capacitor: controls attack and decay time of transmit peak limiter.
C4, C5	0.1μF	Transmit amplifier input capacitors: prevent dc current flow into TXL pin and attenuates low-frequency noise on microphone lead.
C6	0.05μF	Sidetone network capacitor: provides phase-shift in sidetone path to match that caused by telephone line reactance.
C7, C8	0.05μF	Receiver amplifier input capacitors: prevent dc current flow into RM terminal and attneuates low frequency noise on the telephone line.
C9	2.2μF, 3.0V	VR regulator capacitor: frequency compensates the VR regulator to prevent oscillation.
C10	0.01μF	Receiver amplifier output capacitor: frequency compensates the receiver amplifier to prevent oscillation.
C11	0.1μF	DC load filter capacitor: prevents the dc load circuit from attenuating ac signals on V+.
C12	0.01μF	Telephone line by pass capacitor: terminates telephone line for high frequency signals and prevents oscillation in the VR regulator.
C13	620pF	Tone ringer oscillator capacitor: determines clock frequency for tone and warble frequency synthesizers.
C14	0.1μF	DTMF output feed back capacitor: ac couples feed back around the DTMF output amplifier which reduces output impedance.
C15	1.0μF, 250Vac Non-Polarized	Tone ringer line capacitor; ac couples the tone ringer to the telepone lines; partially controls the on-hook input impedance of telephone.

EXTERNAL COMPONENTS (Continued)

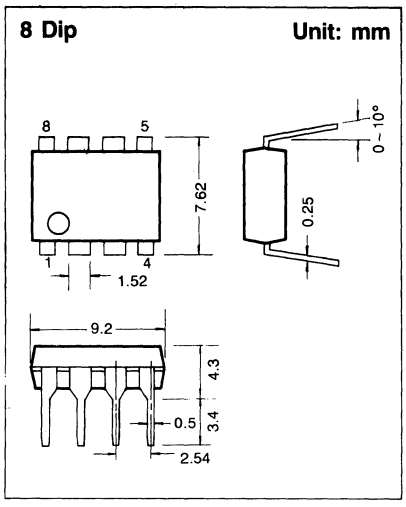
(Component labels referenced to Fig. 12)

Resistors	Nominal Value	Description
R1	6.8K	Tone ringer input resistor: limits current into the tone ringer frm transients on the telephone line and partially controls the on-hook impedance of the telephone.
R2	1.8K	Tone ringer current sense resistor: produces a voltage at the input of the threshold detector in proportion to the tone ringer input current.
R3	200K	Tone ringer oscillator resistor: determines the clock frequency for tone and warble frequency synthesizers.
R4	82, 1.0W	DC load resistor: conducts all dc line current in excess of the current required for speech or dialing circuits; controls the off-hook dc resistance of the telephone.
R5, R7	150K, 56K	Receiver amplifier input resistors: couple ac input signals from the telephone line to the receiver amplifier; signal in R5 subtracts from that in R9 to reduce sidetone in receiver.
R6	200K	Receiver amplifier feedback resistor: controls the gain of the receiver amplifier.
R8, R9	1.5K, 30K	Sidetone network resistors: drive receiver amplifier input with the inverted output signal from the transmitter; phase of signal in R9 should be opposite that in R5.
R10	270	Transmit amplifier load resistor: converts output voltage of transmit amplifier into a current that drives the telephone line; controls the maximum transmit level.
R11	200K	Transmit amplifier feedback resistor: controls the gain of the transmit amplifier.
R12, R13	4.7K, 4.7K	Transmit amplifier input resistors: couple signal from microphone to transmit amplifier; control the dynamic range of the transmit peak limiter.
R14	36	DTMF calibration resistor: controls the output amplitude of the DTMF dialer.
R16	100	Hook switch click suppression current limit resistor (optional): limits current when S3 discharges C3 after switching to the on-hook condition.
Rx	3.0K	Microphone bias resistor: sources current from VR to power a 2-terminal electret microphone; RX is not used with 3-terminal microphones.

Semiconductors	Electret Mic	Receiver
B1= MDA101A, or equivalent, or 4-IN4005 T1=KSA733 or equivalent Z1=18V, 1.5W, IN5931A Z2=30V, 1.5W, IN5936A Z3=4.7V, 1/2W, IN750 XR — CRM 500A TOKO Resonators Piezo — PBL5030BC TOKO Buzzer or equivalent	2 Terminal, Primo EM-95 (use Rx) or equivalent 3 Terminal, Primo O7A 181P (Remove Rx) or equivalent	Prime Model DH-34 (300Ω) or equivalent

TONE RINGER WITH BRIDGE DIODE

The KA2418/KA2419 is a monolithic integrated circuit designed to replace the mechanical bell in telephone sets, in connection with an electro acoustical converter. The supply voltage is obtained from the AC ring signal and the circuit is designed so that noise on the line or variation of the ringing signal cannot affect correct operation of the device.



FUNCTIONS

- Two oscillators
- Output amplifier
- Power supply control circuit.

FEATURES

- **Low current consumption, in order to allow the parallel operation of 4 devices.**
- **On-chip diode bridge and transient protection**
- **Little external circuitry**
- **Tone and switching frequencies adjustable by external components**
- **Integrated voltage and current hysteresis**
- **Activation voltage adjustable (KA2418)**
- **Include inverting output (KA2419)**

BLOCK DIAGRAM

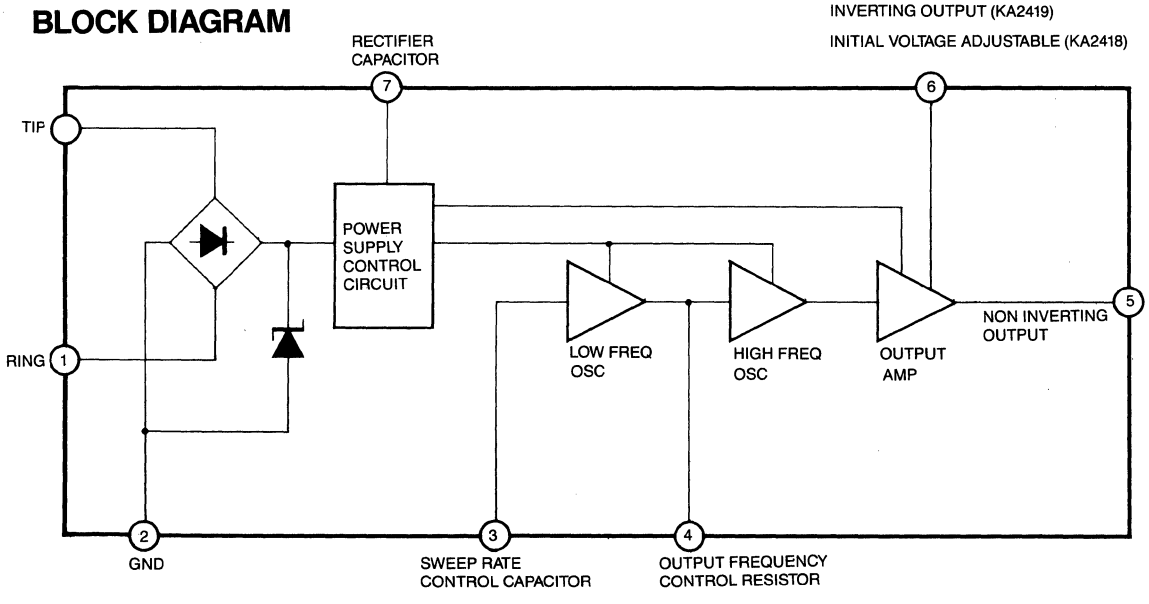


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Calling Voltage (f=50Hz) Continuous	V_{AB}	90	Vrms
Calling Voltage (f=50Hz) 5 Sec ON/10 Sec OFF	V_{AB}	110	Vrms
Supply Current	I_{CC}	22	mA
Operating Temeprature	T_{OP}	−20 ~ +70	°C
Storage and Junction Temeprature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

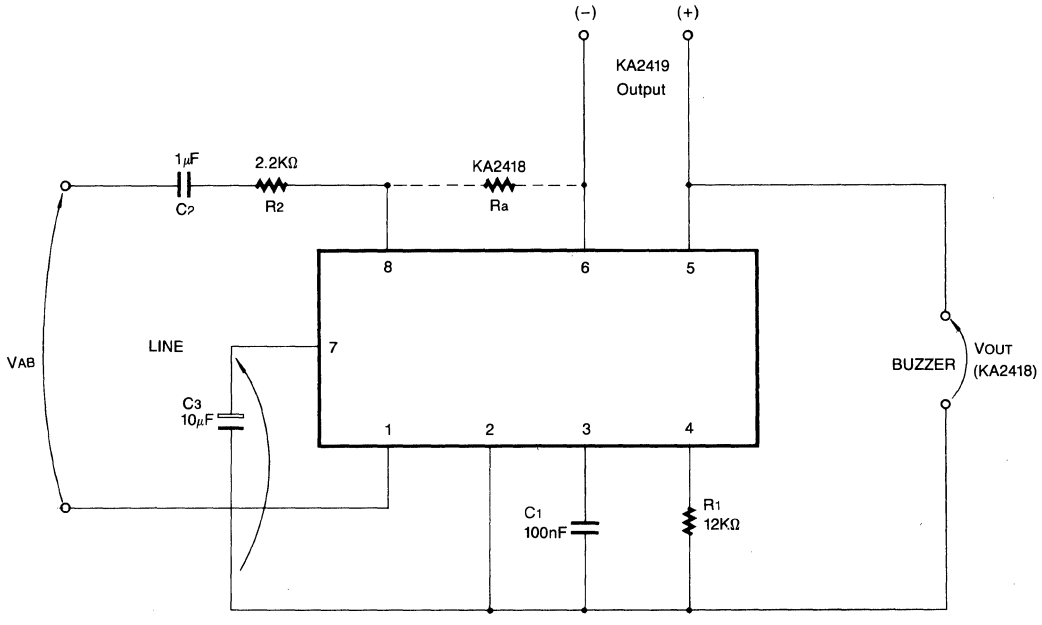
(T_a = 25°C unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{CC}				26	V
Current Consumption without Load	I_B	V_S = 8.8 to 26V		1.5	1.8	mA
Activiation Voltage	V_{ON}		12.2		13	V
Activiation Voltage Range	V_{ONR}	KA2418 only, R_A = 1kΩ	8		10	V
Sustaining Voltage	V_{OFF}		8		8.8	V
Differential Resistance in Off Condition	R_D		6.4			kΩ
Output Voltage Swing 1	$V_{OUT\,1}$			V_{CC} −3		V
Output Voltage Swing 2	$V_{OUT\,2}$	KA2419 only		2((V_{CC}−3)		V
Short Circuit Current	I_{OUT}			35		mA

AC OPERATION

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Output Frequencies		V_{CC} = 26V, R_1 = 14kΩ				
$f_{OUT\,1}$		V_{CC} = 0V		1,900		Hz
$f_{OUT\,2}$		V_{CC} = 6V		1,300		Hz
$f_{OUT\,1}$ Range		R_1 = 27kΩ to 1.7kΩ	0.1		15	KHz
Sweep Frequency		R_1 = 14kΩ, C_1 = 100nF		10		Hz

TEST AND APPLICATION CIRCUIT



$$f_1 = \frac{2.67 \cdot 10^4}{R_1\ (K\Omega)} \qquad f_2 = \frac{5}{7} f_1 \qquad f_{sweep} = \frac{1000}{C_1\ (nF)}$$

Fig. 2

DESCRIPTION

The KA2418/9 tone ringer derive its power supply by rectifying the AC ringing signal. It uses this power to activate two tone generators. The two tone frequencies generated are switched by an internal oscillator in a fast sequence and made audible across an output amplifier in the loudspeaker; both tone frequencies and the switching frequency can be externally adjusted.

The device can drive either directly a piezo ceramic converter (buzzer) or small loudspeaker. In case of using a loudspeaker, a transformer is needed.

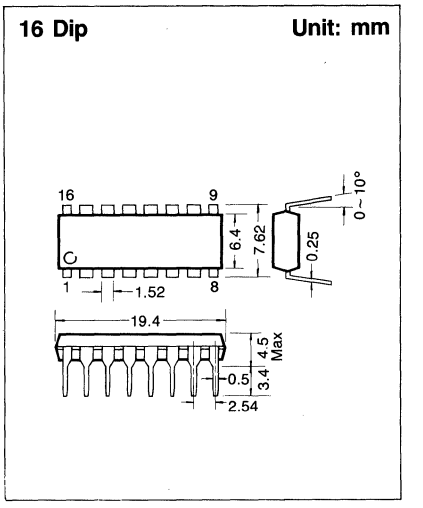
An internal shunt voltage Regulator provides DC voltage to output stage, low frequency oscillator, an High frequency oscillator. To protect the IC from telephone line transients, a zener Diode is included.

EXTERNAL COMPONENTS (refer to test circuit)

R_1 : Output Frequency control resistor
C_1 : Sweep Rate control capacitor
R_2 : Line input resistor. R_2affects the tone ringer input impedance. It also influences ringing threshold voltage and limits current from line transients.
C_2 : Line input capacitor. C_2 AC couples the tone ringer to the telephone line and controls ringer input impedance at low frequencies.
C_3 : Ringer supply capacitor, C_3 filters supply voltage for the tone generating circuits.
R_a : Activation voltage adjustable resistor (KA2418 ONLY)

TELEPHONE PULSE DIALER

The KS5804 consists of C-MOS circuit and keyboard input into pules signal outputs simulating a rotary telephone dial.



FUNCTIONS

- Pulse output
- $\overline{\text{Mute}}$ output
- On-hook/test
- Power up clear circuitry

FEATURES

- **Designed to operate directly from the telephone line**
- **Low voltage, low power operation**
- **Uses either a standard 2-of-7 matrix keyboard with positive common or the inexpensive Form A-type keyboard.**
- **Uses ceramic resonator as frequency reference for accurate timing**
- **Make/Break ratio can be selected**
- **Redial with either * or # input**
- **Provision for rapid testing**
- **On-chip voltage regulator with pin 2 connected GND**

TEST CIRCUIT

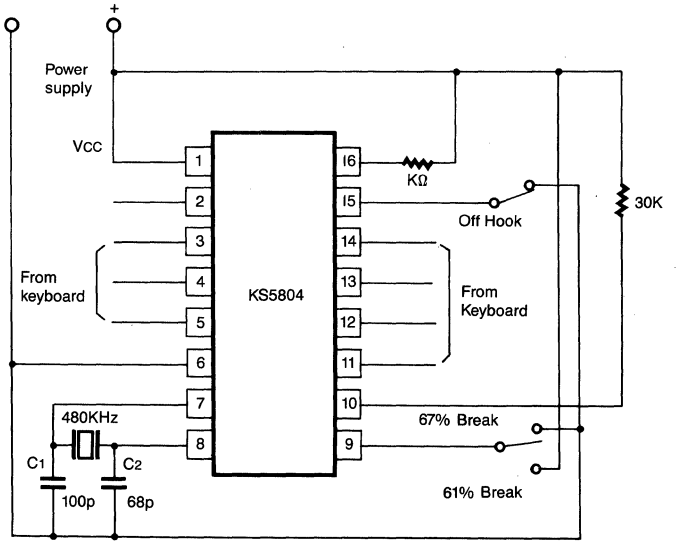


Fig. 1

PIN CONNECTION

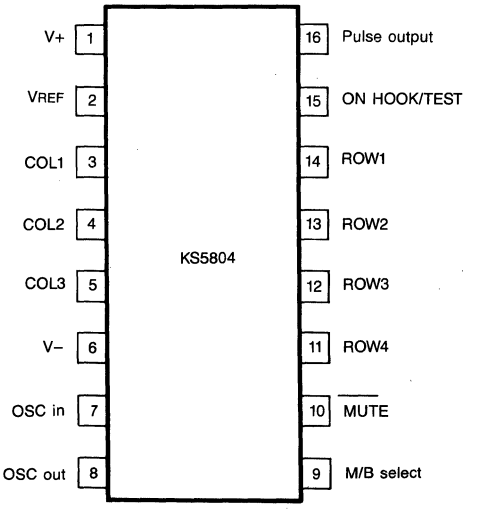


Fig. 2

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	6	V
Power Dissipation	P_D	500	mW
Operating Temperature	Topr	−30 ~ +60	°C
Storage Temperature	Tstg	−55 ~ +85	°C

ELECTRICAL CHARACTERISTICS

(−30°C < T_a < 60°C)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Voltage		V_{CC}	Pin 2 floating	2.3		5.5	V
Keyboard Contact Resistance		R_{KI}				1.0	KΩ
Keyboard Capacitance		C_{KI}				30.0	pF
Input Voltage		K_{IH}	2 of 7 Input mode	0.8V_{CC}		V_{CC}	V
		K_{IL}		V−		0.2V_{CC}	
Keyboard Pull-up Resistance		K_{IRU}	V_{CC} = 5.5V		4.0		KΩ
Mute Sink Current		I_M	V_{CC} = 2.5V, V_O = 0.5V	500.			μA
Pulse Sink Current		I_P	V_{CC} = 2.5V, V_O = 0.5V	1.0	4.0		mA
Magnitude of V_{CC}-V_{REF}		V_{REF}	I_{SUPPLY} = 150μA	1.2	2.2	3.2	V
Memory Retention Current		I_{MR}	All outputs unloaded On-Hook mode		0.7		μA
DC Operation Current		I_{OP}	All outputs unloaded Off-Hook mode		100.	150.	μA
Keyboard Pull-down Resistance		K_{IRO}	V_{IN} = 4.8V		100.0		KΩ
Mute and Pulse Leakage		I_{LKG}			0.001	1.0	μA
Oscillator Frequency		F_{OSC}			480		KHz
Keyboard Debounce Time		t_{DB}			10		m_{SEC}
Time for Valid Key Entry		t_{KD}		40			m_{SEC}
Oscillator Start-up Time		T_{OS}			6		m_{SEC}
Pulse Rate		P_R			10		PPS
Break Time	Pin 9 tied to V_{CC}	t_B			61		m_{SEC}
	Pin 9 tied to V−	t_B			67		m_{SEC}
Interdigital Pause		t_{IDP}			800		m_{SEC}

Notes 1) Typical values are exact with a nominal 480KHz frequence reference.
(except for oscillator start-up time)
2) Ceramic resonator should have the following equivalent values, R < 20Ω, R_A ≥ 70KΩ, C_O ≤ 500pF.

PIN DESCRIPTION

1. V_{CC} (Pin 1)

This is the positive supply input to the part and is measured relative to V– (Pin 6). The voltage on this pin must be maintained within 2.5V — 5.5V using either the on-chip reference circuitry or an external form of regulation.

2. V_{REF} (Pin 2)

The V_{REF} output provides a negative reference voltage relative to the V+ supply. Its magnitude is a function of the internal parameters which define the minimum operating voltage of each part. In a typical application, the V_{REF} PIN is simply tied to V–, as shown in Figure 6. The internal circuit with its associated I-V characteristic is shown in Figure 3.

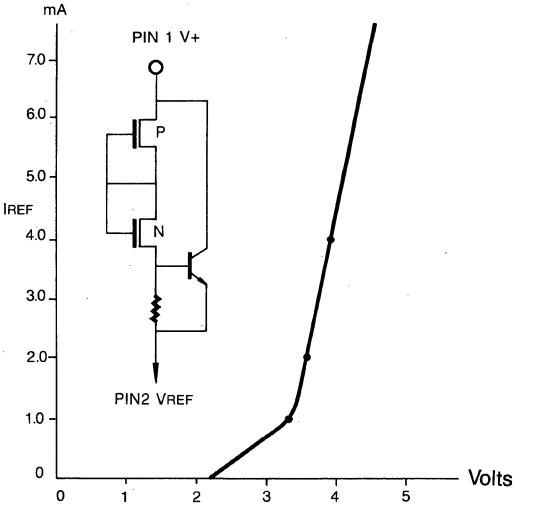


Fig. 3

3. Keyboard Input (Pins 3, 4, 5, 11, 12, 13, 14)

The KS5804 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 matrix keyboard with positive common or the inexpensive form A keyboard to be used, as shown in Figure 4. A valid key entry is defined by either a single row being connected to a single column or V+ being presented to both a single row and column simultaneously. When in the On-Hook mode, the row and column inputs are always held high. When Off-Hook, the key-board and oscillator are completely static until initial valid key input is sensed. The input must remain valid continuously for 10msec of debounce time to be accepted.

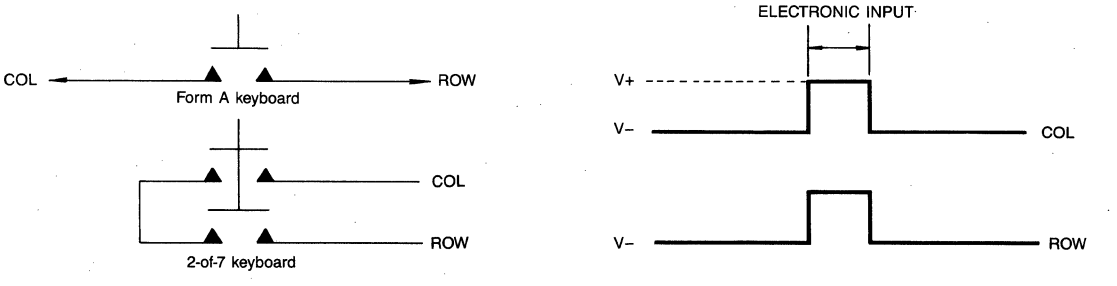


Fig. 4

4. V^- (Pin 6)

This pin is the negative supply pin input and is connected to the common port in the general applications.

5. Oscillator In/Out (Pin 7,8)

The KS5804 contains an on-chip inverter with sufficient gain to provide oscillation when working with a low-cost 480KHz ceramic resonator (anti-resonant mode). In addition to the resonator, two external capacitors are required. Suggested equivalent values for the resonator are given in the timing specification section. These value will insure proper oscillator operation in the specified voltage range. The KS5804 may be driven externally with a 480KHz signal on pin 7.

6. Make/Break Select (Pin 9)

The Make/Break ratio may be selected by connecting the pin either the V_{CC} or V– supply. Table indicates two typical ratios from which the user can choose.

Input to Make/Break Pin	Pulse Output	
	MAKE	BREAK
V_{CC} (Pin 1)	39%	61%
V– (Pin 6)	33%	67%

7. $\overline{\text{Mute}}$ Output (Pin 10)

The Mute output consists of an open-drain N-channel transistor. It provides the logic necessary to mute the receiver while the telephone line is being pulsed.

A typical way to interface this output is shown in the application diagram in Figure 6. The timing characteristic of the mute output is shown in Fig 5.

8. On-Hook/Test (Pin 15)

The "Test" or "On-Hook" input of the KS5804 has a 100KΩ pull-up to the positive supply. A V_{CC} input or allowing the pin to float sets the circuit in its On-Hook or test mode, while a V- input sets it in the Off-Hook or normal mode.

When Off-Hook, the KS5804 can accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled by opening the feedback loop and the circuit stands by for additional inputs.

Switching the KS5804 On-Hook while it is outpulsing causes the remaining digits to be outpulsed at 100 × the normal rate (M/B ratio is then 50/50). Rapidly testing the device is possible by this feature which is also an effecient method by which the circuitry is reset. When the outpulsing in this mode which can take up to 300msec is completed, the circuit is deactivated and will require only a little current necessary to sustain the memory and Power-Up-Clear detect circuitry. (refer to the electrical specifications)

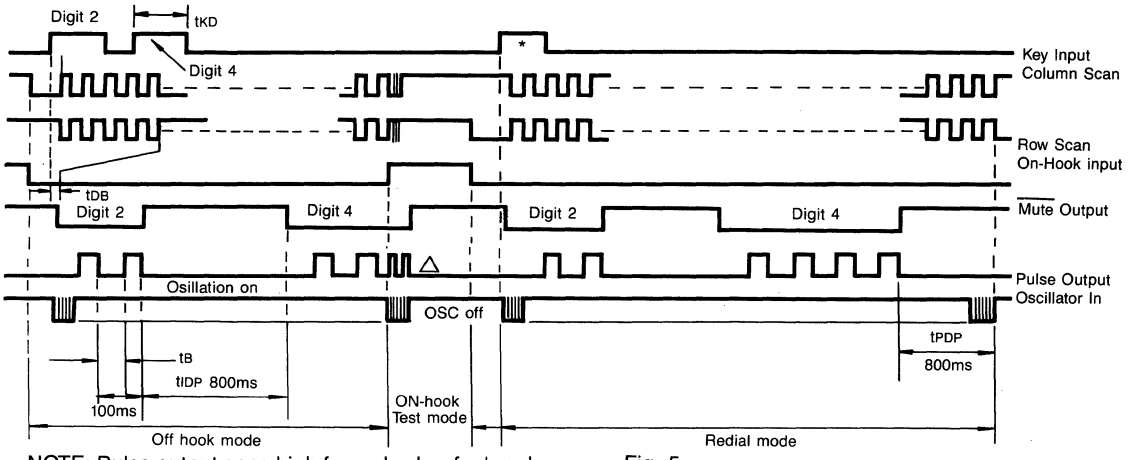
Upon returning Off-Hook, if the first key input is either * or #, the latest number sequence stored on chip will be outpulsed.

Any other valid key inputs will clear the memory and outpulse the new number sequence.

9. Pulse Output (Pin 16)

The pulse output is an open-drain N-channel transistor. This output provides the logic necessary to pulse the telephone line with the correct Make/Break pulse rate, and interdigital pause timings. The timing characteristics of the pulse output are shown in Fig. 5.

TIMING CHARACTERISTICS



NOTE: Pulse output goes high for make, low for break. Fig. 5

APPLICATION CIRCUIT

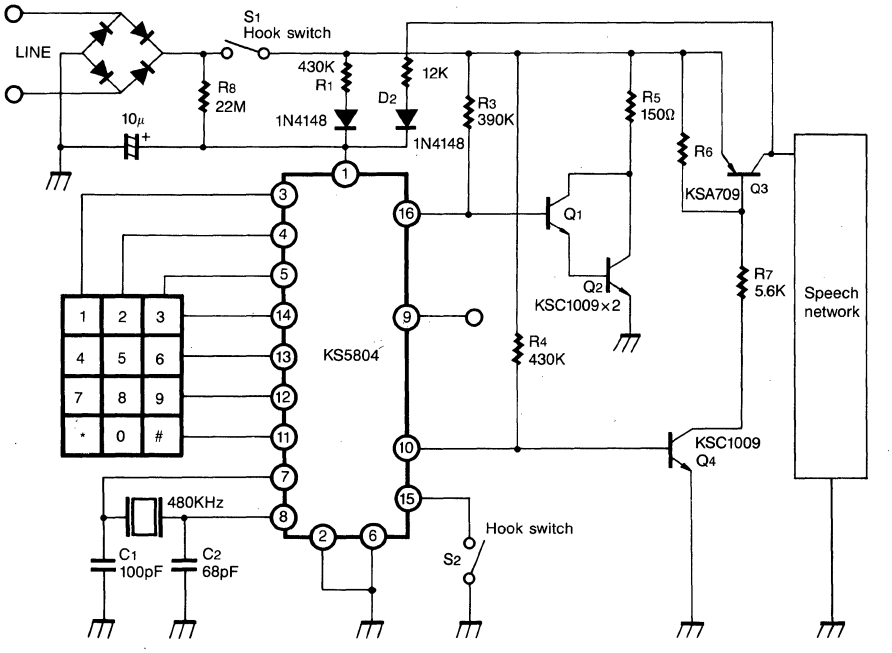


Fig. 6

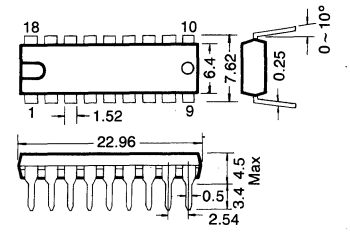
APPLICATION NOTE

The application circuit shows one method witch can be used to interface the pulse dialer with the telephone line.
In the application, the pulse dialer circuitry is in paralell with the speech network.
A current source of some type is desired to present a high impedance to the telephone line while guaranteeing sufficient current to the power the KS5804 ($\geq 150\mu A$).
When in the OFF-HOOK mode, the current is sourced by the collector Q_3 (KSA709), R_1 and R_2 from telephone line.
When ON-HOOK Mode, S_1 and S_2 are open, the memory retention current is only sourced by the resistor R_1 (22 MΩ).
A large value resistor, R_1, allows a small amount of current to maintain the memory on the KS5804.
If the redial function is unnecessary, the resistor R_1 have to needn't connect.
When in the OFF-HOOK mode, S_1 is closed and ON-HOOK pin 15 ties V-(GND).
As soon as the MUTE output pin 10 is high (voltage between base and emitter of transistor Q_4), transistor Q_4 turn on and this holds speech network on until outpulsing begins.
The speech network is connected through transistor Q_3 to the telephone line.
The MUTE Output pin 10 switches low before (60msec when pin 9 tied to V_{CC} pin 1 or 67msec when pin 9 tied to V-pin 6) pulse output pin 16 is beginning outpulse.
When MUTE switches low, the speech network is removed from the line and the first break occurs.
thus, the pops caused by breaking the line are isolated from the receiver.
When pulse output pin 16 is low, it flows to very low pulse sink current.
When pulse output pin 16 is high (voltage between base and emitter of transistor Q_1), it flows to base current of transistor Q_1.
If your application is difficult to connect S_2, it is necessary only one of transistor, request information on our KS5804 pplication circuit designer.

TELEPHONE PULSE DIALER

The KS5805A/B is a monolithic C-MOS integrated circuit and provides all the features required for implementing a pulse dialer with redial.

18 Dip Unit: mm



FUNCTIONS

- Mute output logic "0"
- $\overline{\text{Pulse}}$ output logic
- RC oscillation for reference frequency
- Designed to operate directly from the telephone line
- Used CMOS technology for low voltage, low current
- Power up clear circuitry
- KS5805A pin 2: V_{REF}
- KS5805B pin 2: Tone out

FEATURES

- **Uses either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard**
- **Make/Break ratio can be selected**
- **Redial with * or #**
- **Continuous $\overline{\text{MUTE}}$**
- **Tone signal output or on-chip reference Voltage by bonding option on chip**
- **10 pps/20 pps can be selected**

TEST CIRCUIT

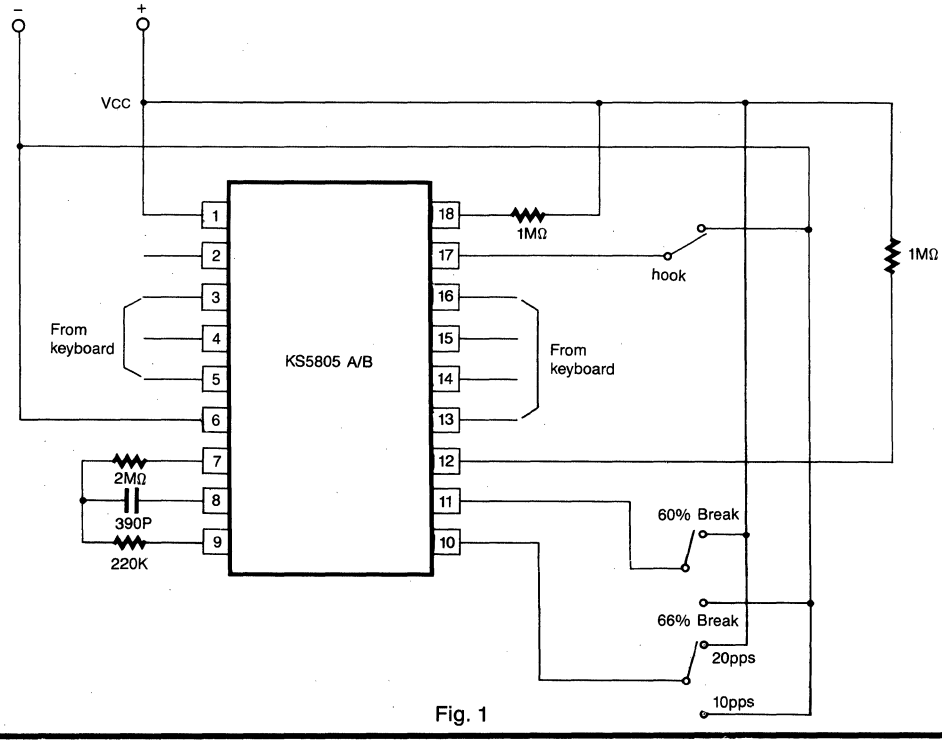


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	6.2	V
Voltage on Any Pin	V_{IN}	V_{CC} + 0.3, V_{SS} − 0.3	V
Power Dissipation	P_D	500.0	mW
Operating Temperature	Topr	−30 ~ +60	°C
Storage Temperature	Tstg	−55 ~ +85	°C

DC ELECTRICAL CHARACTERISTICS

(T_a=25°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}		2.5		6.0	V	
Key Contact Resistance	R_{KI}				1	KΩ	1
Keyboard Capacitance	C_{KI}				30	pF	
Key Input Voltage	K_{IH}	2 of 7 input mode	0.8V +		V +	V	1
	K_{IL}		V−		0.2V+		
Key Pull-Up Resistance	K_{IRU}	V+=6.0V		100		KΩ	
Key Pull-Down Resistance	K_{IRD}	V_{IN}=4.8V		4.0		KΩ	
Mute Sink Current	I_M	V+=2.5V V_O=0.5V	500			μA	2
Pulse Output Sink Current	I_P	V + =2.5V V_O=0.5V	1.0			mA	3
Tone Output Sink Current	I_{TL}	V+=2.5V V_O=0.5V	250			μA	4
Tone Output Source Current	I_{TH}	V+=2.5V V_O=0.5V	250			μA	4
Memory Retention Current	I_{MR}	All outputs under no load		0.7		μA	6
Operating Current	I_{OP}	All outputs under no load		100	150	μA	
Mute or Pulse Off Leakage	I_{LKG}	V+=6.0V V_O=6.0V		0.001	1.0	μA	2,3
V_{REF} Output Source Current	I_{REF}	V_{CC}-V_{REF}=6.0V	1.0	7.0		mA	5

Note 1) Applies to key input pin. (R_1-R_4, C_1-C_3)
2) Applies to $\overline{\text{MUTE}}$ output in.
3) Applies to $\overline{\text{PULSE}}$ output pin.
4) Applies to TONE pin (KS5805B)
5) Applies to V_{REF} pin (KS5805A)
6) Current necessary for memory to be maintained. All outputs unloaded.

* Typical values are to be used as a design aid are not subject to production testing.

AC ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Oscillator Frequency	F_{OSC}		4		KHz	1
Key Input Debounce Time	T_{DB}		10		ms	3.4
Key Down Time for Valid Entry	T_{KD}	40			ms	4.5
Key Down Time During Two-Key Roll Over	t_{KR}	5			ms	4
Oscillator Star-Up Time (V+ = 2.5V)	t_{OS}		1		ms	
Mute Valid After Last Outpules	t_{MO}		5		ms	3.4
Pulse Output Pulse Rate	P_R		10		PPS	2
On-Hook Time Required to Clear Memory	t_{OH}	300			ms	4
Pre-Digital Pause	T_{PDP}		800		ms	3.4
Inter-Digital Pause	T_{IDP}		800		ms	3.4
Frequency Stability V_{CC} = 2.5 – 3.5V	Δf		±4		%	
Frequency Stability V_{CC} = 3.5 ~ 6.0V	Δf		±4		%	
Tone Output Frequency	F_{TONE}		1		KHz	4.6

Note: 1) R_S = 2MΩ, R = 220KΩ, C = 390pF.
2) If pin 10 is tied to V_{CC}, the pulse output pulse rate will be 20pps.
3) If the 20pps option is selected, the time will be 1/2 these shown.
4) These times are directly proportional to the oscillator frequency.
5) Debounce plus oscillator start-up time ≤ 40ms.
6) If the 20pps option is selected, the tone output frequency will be 2KHz.

PIN CONNECTIONS

Pin 1: V_{CC}
Pin 2: V_{ref} (KS5805A)/Pacifier tone (KS5805B)
Pin 3: $\overline{\text{Column 1}}$
Pin 4: $\overline{\text{Column 2}}$
Pin 5: $\overline{\text{Column 3}}$
Pin 6: GND
Pin 7: RC Oscillator
Pin 8: RC Oscillator
Pin 9: RC Oscillator
Pin 10: 10/20pps Select
Pin 11: Make/Break Select
Pin 12: $\overline{\text{Mute}}$ Output
Pin 13: $\overline{\text{ROW 4}}$
Pin 14: $\overline{\text{ROW 3}}$
Pin 15: $\overline{\text{ROW 2}}$
Pin 16: ROW 1
Pin 17: On-Hook/Test
Pin 18: $\overline{\text{Pulse}}$ Output

TIMING CHARACTERISTICS

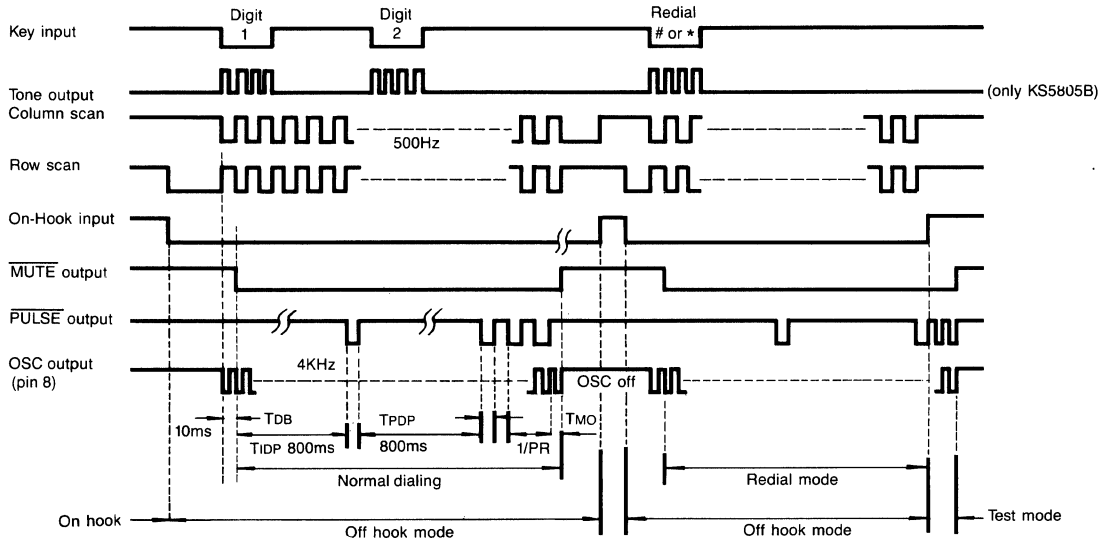


Fig. 2

PIN DESCRIPTIONS

1. V_{CC} (Pin 1)

This is the positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150μA current source. This voltage must be regulated to less than 6.0 volts using on external form or regulation.

2. Tone signal output/V_{REF} (Pin 2)

Tone signal out pin is CMOS comperementaly output and drive on external bipolar transistor. This pin generates a tone signal when a key is depressed as its recognition. Tone signal frequency is 1KHz when 10pps pulse rate is selected. (the frequency is 2KHz when 20pps pules rate is selected). Only the pin 2 of KS5805A is V_{REF} (on-chip reference voltage).

3. Keyboard inputs (Pin 3, 4, 5, 13, 14, 15, 16,)

The KS5805A/B incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used.

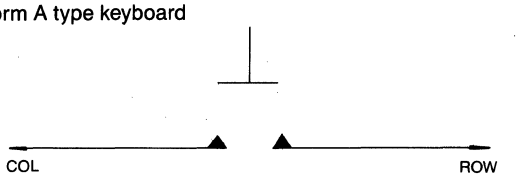
A valied key entry is defined by either a single row being connected to a single column or GND being simutaneously presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high and no keyboard inputs are accepted.

When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is varied. The input must remain valid continuously for 10msec of debounce time to be accepted.

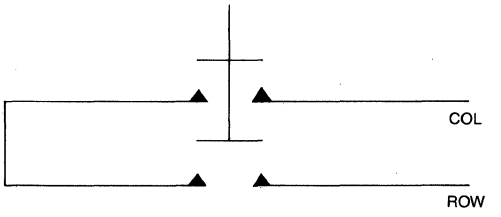
4. GND (Pin 6)

This is the negative supply pin and is connected to the common part in the general applications.

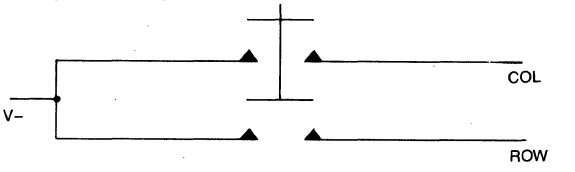
• Form A type keyboard



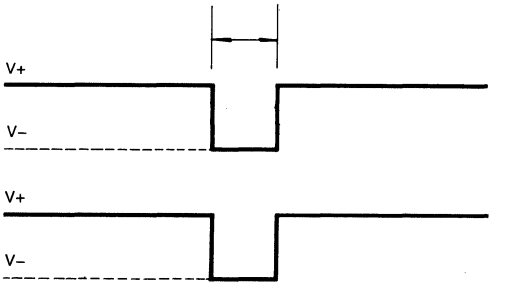
• 2 of 7 keyboard



• 2 of 7 keyboard (negative common)



• Electronic input



5. OSCILIATOR (Pins 7, 8, 9)

The KS5805A/B contains on-chip inverters to provide an oscillator which will operate with a minimum of external components.

Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K=R_S/R$ equal to 10.

The oscillator period is given by:

$$T=RC\ (1.386 + (3.5KC_S/C-(2K/(K+1)\ \ln\ (K/(1.5K+0.5))$$

Where C_S is the stray capacitance on Pin 7.

Accuracy and stability will be enhanced with this capacitance minimized.

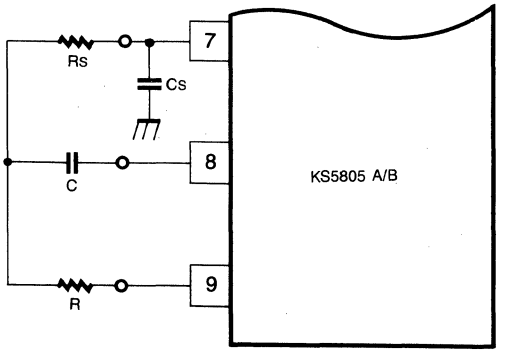


Fig. 4

6. 20/10 pps (Pin 10)

Connecting this pin to GND (pin 6) will select an output pulse rate of 10pps.

Connecting the pin V_{CC} (pin 1) will select an output pulse rate of 20pps.

7. MAKE/BREAK (Pin 11)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connecting V_{CC} or GND to this pin as shown in the following table.

Input	Make	Break
V+ (Pin 1)	34%	66%
V– (Pin 6)	40%	60%

8. $\overline{\text{MUTE}}$ OUTPUT (Pin 12)

The mute output is an open-drain N-channel transistor designed to drive an external bipolar transistor.

This circuitry is usually used mute the receiver during outpulsing. As shown in Fig. 2 the KS5805 $\overline{\text{mute}}$ output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break.

The dealy from the end of the last break until the $\overline{\text{mute}}$ output turns off is mute overlap and is specified as t_{MO}.

9. ON-HOOK/TEST (Pin 17)

The "ON-HOOK" or test input of the KS5805A/B has a 100KΩ pull-up to the positive supply. A V_{CC} input or allowing the pin to float sets the circuit in its on-hook or test mode while a V_{GND} input sets it in the off-hook or normal mode. When off-hook, the KS5805A/B will accept key inputs and outputs the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the KS5805A/B to on-hook while it is outpulsing causes the remaining digits to be outpulsed at 100x the normal rate (M/B ratio is then 50/50).

This features provides a mean of rapidly testing the device and is also on efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300msec, is completed, the circuit is deactived and will require only the current necessary to sustain the memory and power-up-clear detect circuitry (refer to the electrical specificontions).

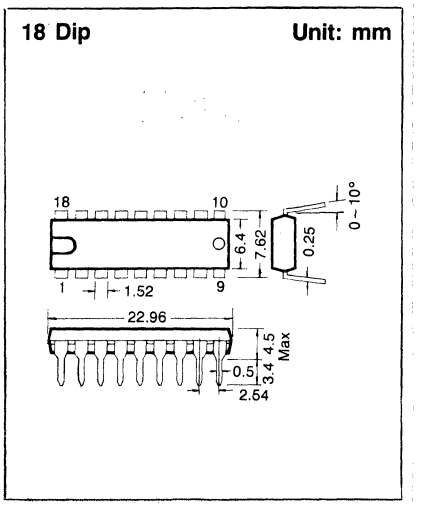
Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

10. $\overline{\text{PULSE}}$ OUTPUT (Pin 18)

The $\overline{\text{pulse}}$ output is an open drain N-channel transistor designed to drive on external bipolar transistor. These transistor would normally be used to pulse the telephone line by disconnecting and connecting the network. The KS5805A/B pulse output is an open circuit during make and pulls to the GND supply during break.

TEN NUMBER REPERTORY DIALER WITH PACIFIER TONE

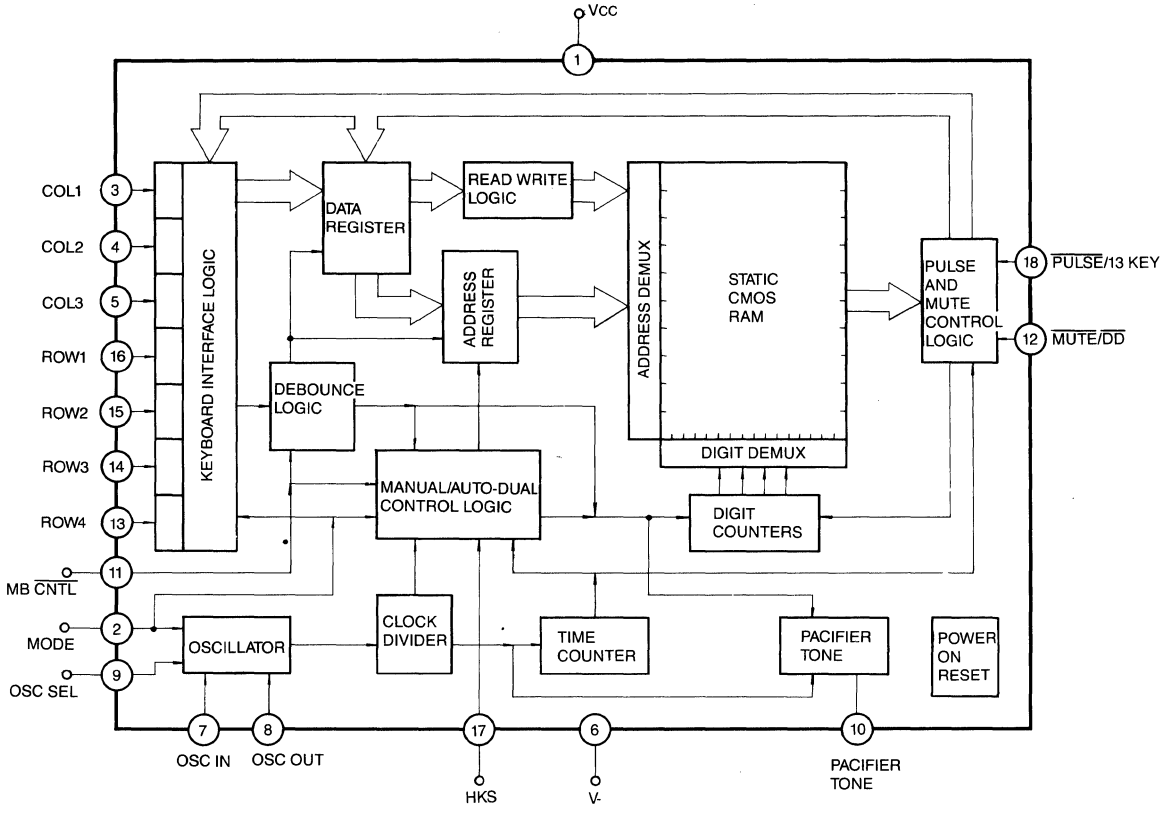
The KS5806 is a monolithic integrated ten-number repertory dialer manufactured using CMOS process. The circuit accepts keyboard inputs and provides the pulse and mute logic levels required for loop disconnent signaling.



FEATURES

- **Low-voltage (2 to 10V) and lowpower operation**
- **Low memory retention current of 1μ**
- **Auto-dials Ten 16 digit-numbers including Last Number Dialed (LND)**
- **Pacifier Tone Output**
- **Oscillator Selectable in pulse mode (RC or ceramic resonator)**
- **Stand-alone pulse dialer**
- **PABX pause key input**
- **Last number dialed memory**
- **Last number dialed may be copied into any one of nine other locations.**
- **Make/Break ratio is pin selectable in pulse mode**
- **Uses either the inexpensive Form-A type keyboard or the standard 2-of-7 matrix keyboard with common V–**
- **Optional use of 13th key input to control repertory functions in tone mode**
- **Power up circuit initializes RAM and logic**

BLOCK DIAGRAM



DESCRIPTION

The KS5806 is a ten-number repertory dialer manufactured using silicon Gate CMOS process. Pin 2, the "Mode select" input determines whether signaling will be pulse or tone. The interpretation of several inputs and outputs is dependent upon the mode selected.

In the pulse mode the time base for the circuit is selectable between a ceramic resonator and RC oscillator. In tone mode the circuit can only use the RC oscillator. An on chip RAM is capable of storing ten 16-digit telephone numbers including the last number dialed.

When used in a PABX system, a pause (# key) may be stored in the number sequence. The repertory dialer will recognize this pause when automatically dialing and stop until another key input is received.

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Caracteristic	Symbol	Value	Unit
DC Supply Voltage V^+	V_{CC}	10.5	V
Maximum Power Dissipation (25°C)	P_D	500	mW
Maximum Voltage on Any Pin	V_{IN}	V_{CC} +0.3, V_{SS} −0.3	V
Operating Temperature	T_{opr}	−30 ~ 60	°C
Storage Temperature	T_{stg}	−55 ~ 125	°C

DC ELECTRICAL CHARACTERISTICS

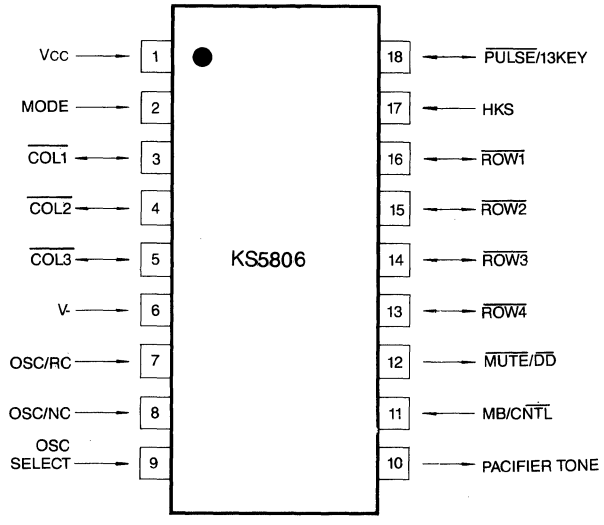
(T_a =25°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage	V_{CC}		2.0		10.0	V
Operating Current (Tone)	I_{OP}	V_{CC} =2.5V		50	100	μA
Operating Current (Pulse)	I_{OP}	V_{CC} =2.5V		100	200	μA
Standby Current (V_{CC} =2.5V)	I_{SB}	No load		1.0	2.0	μA
Memory Retention Current	I_{MR}			0.3	1.0	μA
Memory Retention Voltage	V_{MR}		1.5	1.3		V
Mute Sink Current	I_{ML}	V_{CC} =2.5V, V_O =0.5V	0.5	2.0		mA
Pulse Sink Current	I_P	V_{CC} =2.5V, V_O =0.5V	1.0	4.0		mA
Pacifier Tone Source/Sink	I_{PT}	Source V_O =2.0V	200	500		μA
Mute and Pulse Leakage	I_{LKG}	V_O =10V		0.001	1.0	μA
Key Contact Resistance	R_{KI}				1.0	KΩ
Keyboard Capacitance	C_{KI}				30	pF
"O" Logic Level	K_{IL}		V−		0.2V+	V
"I" Logic Level	K_{IH}		0.8V+		V+	V
Keyboard Pull Up	K_{RU}			100		KΩ
Keyboard Pull Down	K_{RD}			1.0		KΩ
CNT Pull Up (Pin 11)	R_{CNT}	Tone mode only		100		KΩ

AC ELECTRICAL CHARACTERISTICS (T_a =25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator (Cer. Res)	F_{CR}		480		KHz
Oscillator (RC)	F_{RC}		8	16	KHz
Oscillator Stability	ΔF_{RC}	−3		+3	%
Debounce Time	T_{DB}		32		mS
Valid Key Down Time	T_{KD}	40			mS
Oscillator Start Up Time	T_{OS}			8	mS
Key Rollover OVLP Time	T_{ROL}	4			mS
Pulse Rate	P_R		10		PRS
Break Time (Pin 11 V+/V−)	T_B		940		mS
Predigital Pause Time	T_{PDP}		170		mS
Mute Overlap Time	T_{MOL}		2		mS
Tone Rate	T_R		5		TPS
Pacifier Tone Burst Time	T_{PT}		28		mS
Pacifier Tone Frequency	F_{PT}		500		Hz
Interdigital Pause Time	T_{IDP}		940		mS

PIN CONNECTION



PIN DESCRIPTION

1. V_{CC} (Pin 1)

Pin 1 is the positive supply input to the part and is measured relative to GND (pin 6). The voltage on this pin should not exceed 10 Volts. On chip Zener diodes will provides protection from supply transients in most applications. A low voltage detect circuit will perform a power up initialization whenever the supply voltage at this pin falls below a level necessary to guarantee proper circuit operation.

2. Mode (Pin 2)

The KS5806 will function in either tone or pulse mode, dependent upon the logic level presented to pin 2. For pulse mode operation, this pin must be tied to GND (pin 6). For tone mode, it should be tied to V_{CC} (pin 1). The interpretation of pins 7,8,11,12, and 18 are dependent upon the mode selected.

3. Keyboard Inputs (Pins 3, 4, 5, 13, 14, 15, 16)

The KS5806 incorporates a keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single-contact (Form A) keyboard to be used, as shown in Fig. 1.

A valid key entry is defined by either a single row being connected to a single column or V — being simultareously presented to both a single row and column.

In the tone mode, the KS5806 features a bidirectional keyboard scheme. As the KS5806 passively monitors the key inputs (using the scan provided by the tone dialer), they are debounced, decoded, and stored in the on chip LND (Last Number Dialed) buffer. The keyboard inputs in tone mode are normally high impedance allowing the tone chip to scan the keyboard lines and begin signaling immediately upon detecting a key entry. A command key entry disables the tone chip and scanning is then controlled by the repertory dialer until the key is released. In tone mode auto-dialing is performed by the KS5806 which simulates key contact closures. The tone generator accepts these inputs as valid keyboard information and generates the proper DTMF frequencies.

In the pulse mode, the KS5806 keyboard inputs are static until an initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is valid. Keyboard bounce is ignored for 32 ms after the initial key down is detected. A key input is accepted if it is valid after this initial debounce time. This scheme guarantees any valid key input to be recognized in less than 40 ms after the initial key closure.

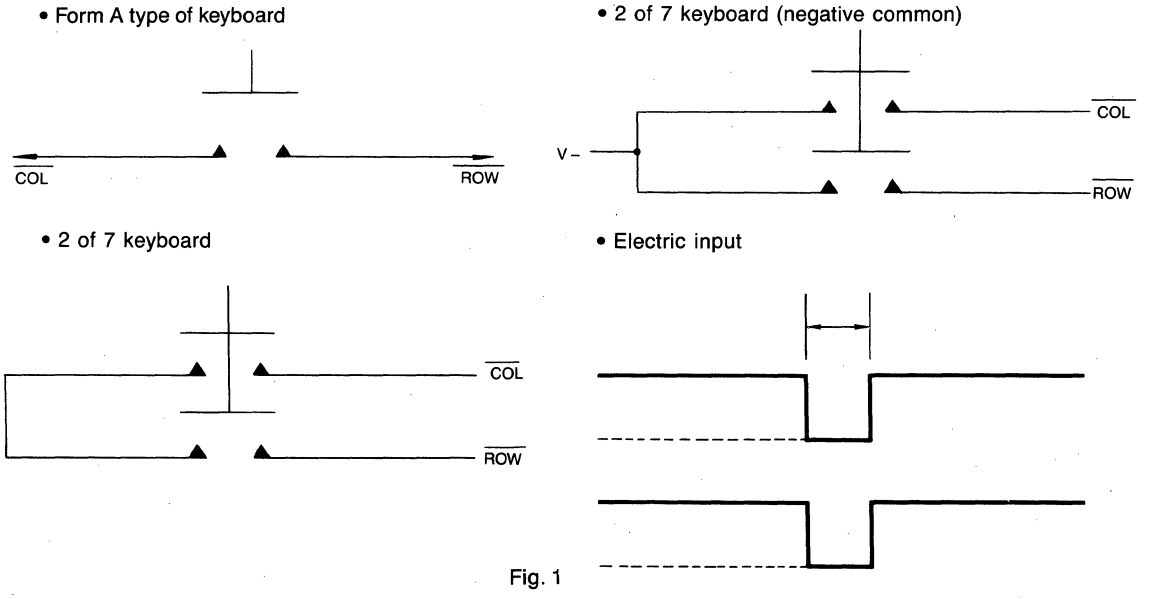


Fig. 1

4. GND (Pin 6)

This is the negative supply pin and is connected to the common part in the general applications.

5. Oscillator. (Pin 7 and Pin 8)

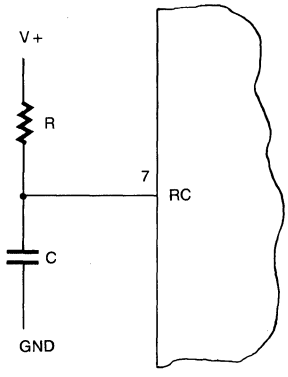
The RC oscillator (Figure 2a) requires a resistor and capacitor to provide the frequency reference for the KS5806. The resistor should be connected from Pin 7 (Osc/RC) to Pin 1 (V+) and the capacitor from Pin 7 to Pin 6 (V−). Pin 8 should be connected to V+ for normal operation. The nominal frequency for standard operation is 8kHz. This provides for a tone rate of 100ms on and 100ms off and pulse rate of 10pps. The frequency of oscillation is approximated by the equation.

$$F_{OSC} = 1/(1.45\ RC).$$

The value suggested for the capacitor (C) should be 410pF or lower and resistor (R) may be adjusted for the desired signalling rate. 10PPS and 5TPS operation is achieved by selecting a 390 pF capacitor and a 220K Ohm resistor.

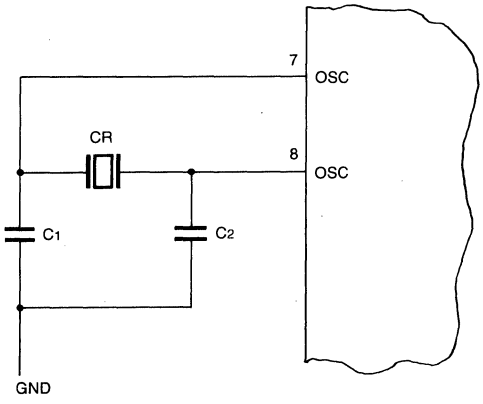
A more accurate and constant frequency reference in pulse mode is obtained using a 480 kHz ceramic resonator as shown in Figure 2b. The ceramic resonator is connected in parallel with an on-chip inverter. Two external capacitors to ground are also required.

a, RC OSC



NOMINAL FREQUENCY 8KHz

b, CERAMIC RESONATOR



FREQUENCY 480 KHz

Fig. 2

6. Oscillator Select. (Pin 9)

This pin determines the mode of oscillation used by the repertory dialer when in pulse mode. The ceramic resonator is chosen by tying this pin to Pin 1 (V+). The RC oscillator is chosen by tying this pin to Pin 6 (V−).

In tone mode this input must be tied either high or low but it will not affect the mode of oscillation which is always RC. The timing of the repertory dialer is independent of the tone chip which uses a 3.5795 MHz crystal as its frequency reference.

7. Pacifier Tone (Pin 10)

The pacifier tone consists of a burst of a 500 Hz square wave. The burst is initiated with the acceptance of a valid key input (following the debounce time) and terminates after 28ms or with the release of the key, whichever comes first. The output is high impedance when not active.

8. MB/$\overline{\text{CNTL}}$ (Pin 11)

The level on pin 16 determines the control key inputs required to implement the repertory dialer function. In the 13 key tone mode, Pin 9 can be used to "control" the repertory dialer functions of the phone with a momentary SPST switch to the negative supply connected to this input. This feature allows the basic keyboard to operate the same as in a standard telephone and only the closure of the 13th key will initiate a repertory dialer function. The * and # key inputs will be accepted as normal DTMF inputs (however they will not be stored in the LND buffer). In 12 key mode this pin should be connected to the positive supply (V+).

In pulse mode, the make/break ratio may be selected by connecting this pin to either the V+ or V– supply. Table 1 indicates the two ratios available.

9. $\overline{\text{Mute}}$/$\overline{\text{Dialer Disable}}$ (Pin 12)

Pin 12 is the output of an open drain N-channel transistor. In the tone mode, it is used to provide the tone dialer with a Dialer Disable signal which inhibits the generation of tones during command key entries. The timing characteristics in tone mode are shown in Figure 3a.

In the pulse mode, Pin 12 is the $\overline{\text{Mute}}$ output. It provides the logic necessary to mute the receiver while the telephone line is being pulsed. Figure 3b shows the timing characteristics of the $\overline{\text{Mute}}$ output.

MB Input	% Break	% Make
V^+	60	40
V^-	68	32

10. HKS (Pin 17)

The HKS (hook switch) input determines how the repertory dialer will handle key entries. When in the off-hook state (pin tied to V–) signalling is enabled and all entries will be stored in the LND buffer. A control key input in this state initiates the AUTO-DIAL function.

In the on-hook state (Pin 17 tied to V+), the dialer stores key information in the LND buffer as they are entered but will not pulse out or allow the DTMF generator to tone. A control key input is interpreted as a STORE command causing the information present in the LND buffer to be copied into the indicated location.

A hook switch transition terminates all dialer operations immediately and initializes all counters and latches. The dialer is then ready to accept a key entry which will be stored over previous data in the LND buffer.

11. $\overline{\text{Pulse}}$/13Key (Pin 18)

In the tone mode, a V+ level at Pin 18 allows the KS5806 to accept inputs from a control key (n.o. SPST) connected from $\overline{\text{CNTL}}$ (Pin 9) to V–. It is used to initiate all repertory functions. This is referred to as 13 key tone mode. With Pin 18 tied to V–, the KS5806 is set in the 12-key tone mode and the * and # keys are used in control functions. Pulse mode defaults to 12 key mode. Both 12 and 13 key tone modes are discussed in more detail in the Operations section of this data sheet.

In the pulse mode, Pin 18 is the $\overline{\text{Pulse}}$ output. It consists of an open drain N-channel transistor and provides the necessary timing for make, break, interdigital delay, and pulse rate to meet dialer specifications worldwide. The timing characteristics of the Pulse $\overline{\text{output}}$ are shown in Figure 3b.

General Operation

During normal dialing, each digit is stored in the LND (Last Number Dialed) buffer, location 0. The telephone number dialed can be left in this temporary LND buffer for later use or it can be copied into any of the other nine permanent memory locations (1-9).

The wrap-around feature of the buffer allows more than 16 digits to be dialed. Entries following the sixteenth input will be stored beginning with the first buffer location replacing the information originally stored there. Any number of digits may be entered and dialed correctly. In pulse mode, the user should not get more than 15 entries ahead of the digit being pulsed.

Keys entered while auto-dialing in pulse mode will be ignored and not affect the number dialed. In tone mode, if a key is entered while auto-dialing it will interfere with the keyboard outputs generated by the KS5806. The key entry is detected and auto-dialing is interrupted until the key is released. The keyboard entry generates a DTMF signal if valid.

The KS5806 repertory dialer will not store either a * or # entry in the buffer but will allow the tone generator to signal these digits as described below.

12. KEY OPERATION

Normal Dialing

In pulse mode digits 0-9 will result in the pulsing of that digit at the standard rate of 10 pps. If the RC oscillator is utilized this rate can be varied achieving a pulse rate of up to 20pps. The * and # keys enable the repertory functions listed below.

In tone mode operation, digits 0-9 causes the generation of respective DTMF signal. In order to tone a * or # key it must be entered twice. The second entry will generate the desired DTMF tone, although it will not be stored in memory.

Storage

Telephone numbers may be entered into the LND buffer while either on-hook or off-hook. However, the KS5806 must be in the on-hook mode for a number to be copied into a permanent memory location. The LND is copied by entering the key sequence **, followed by the address (1-9) of the desired memory location. This operation requires 300 ms before going off hook or initiating another store and does not change the data in the LND buffer. Information present in the LND buffer when new data is entered is replaced and cannot be recalled.

The storage operation may be performed with the telephone off-hook. If requires the addition of an additional switch providing an excellent "Scratchpad Memory". Numbers may be entered and copied without signalling the line making use of line current rather than battery current. Scratchapd memory is useful whenever the user has a need to record a telephone number such as when calling information.

Automatic Dialing

The automatic dialing function is implemented by going off-hook and entering a *, followed by the address (1-9) of the desired telephone number. Dialing will begin with the release of the address key and can be interrupted by initiating a new redial command or with a transition on the HKS pin. The LND buffer will contain the information last entered. A key sequence of * 0 will cause the last number entered to be redialed. More than one number sequence may be automatically dialed from memory without returning on-hook.

Pause/Continue Entries

The KS5806 has a feature which allows an indefinite pause to be programmed into the first 15 digits of a number sequence by entering a # key at the point in the sequence where a pause is desired. As the number is automatically dialed, the circuit will stop dialing when the pause is encountered. Any key entry, except for a * key, will cause the KS5806 to continue dialing the remainder of the number. If more than one pause was originally programmed into the number sequence, a corresponding number of continue commands must be made in order for the number to be completely dialed.

The continue input will not be recognized until one IDP period following the signalling of the digit preceeding the pause. This is approximately 940 ms in pulse mode and 100 ms in tone mode.

13. KEY MODE OPERATION

Normal Dialing

An additional mode of operation (tone mode only) is the ability to use the entire keyboard for normal signalling such that when any key is depressed once, including * or #, the proper DTMF signal is generated. This feature is activated by connecting Pin 16 to V+. The repertory dialer functions are then initiated by an extra control key (n.o. SPST) connected from Pin 9 (MB/$\overline{CNTL}$) to V−. This key will be referred to as "C"

Storage

The information in the LND buffer may be "copied" or stored into one of the nine permanent memory locations when the input to HKS is high. The control sequence for this function is C-N. The information will be copied yet leave the LND buffer information intact.

Automatic Dialing

Information stored in any of 10 memory locations may be autodialed by entering C-N when the input to HKS (Pin 17) is low. Autodialing may be initiated immediately following a hookswitch transition, manual key entries, or after the completion of a previous auto-dial number.

Pause/Continue

An indefinite pause may be inserted into the number sequence with a C # entry. This feature is quite useful when dialing through a PABX. When a number sequence with a pause is autodialed, signalling will stop when the pause is reached and will continue only when a valid key input is detected.

TONE MODE TIMING

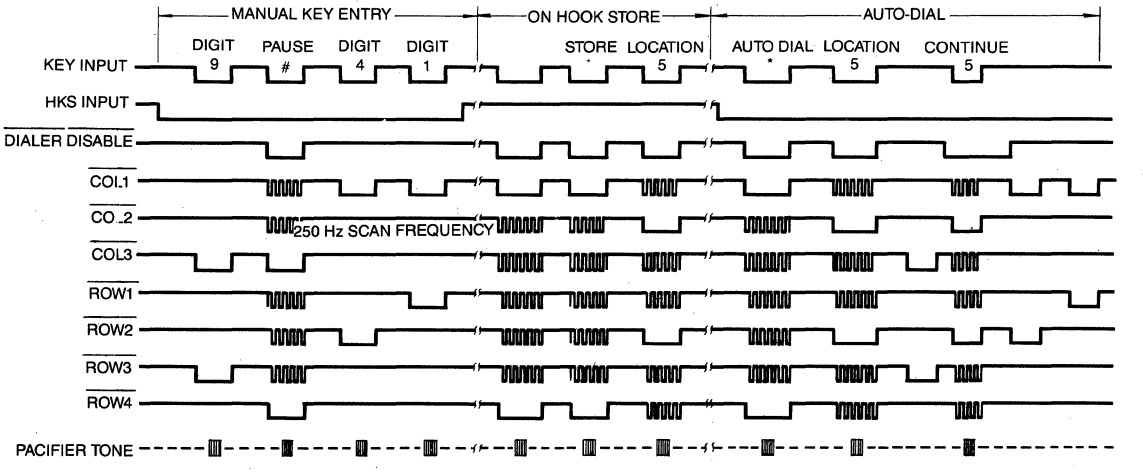


Fig. 3a

PULSE MODE TIMING

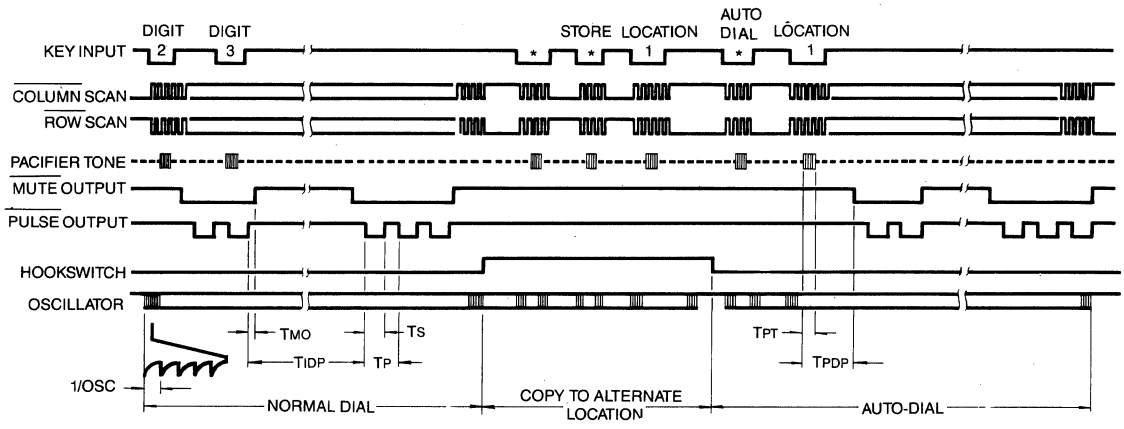
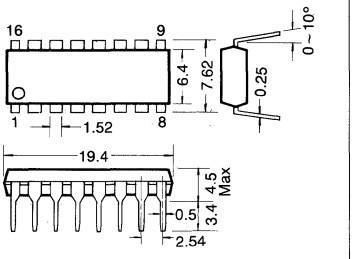


Fig 3b

DUAL TONE MULTI FREQUENCY DIALER

The KS5808 is a monolithic integrated circuit fabricated using C-MOS process and is designed specifically for integrated tone dialer applications.

16 Dip Unit: mm



FUNCTIONS

- Fixed supply operation
- Negative-true keyboard input
- Tone disable input
- Stable-output level

FEATURES

- **Minimum number of external parts required.**
- **High accuracy tones.**
- **Digital divider logic, resistive ladder network and CMOS operational amplifier on single chip.**
- **Uses inexpensive 3.579545 MHz television color burst crystal.**
- **Invalid key entry can result in either single tone or no tone.**
- **Tone disable allows any key down output to function from keyboard input without generating tones.**

BLOCK DIAGRAM

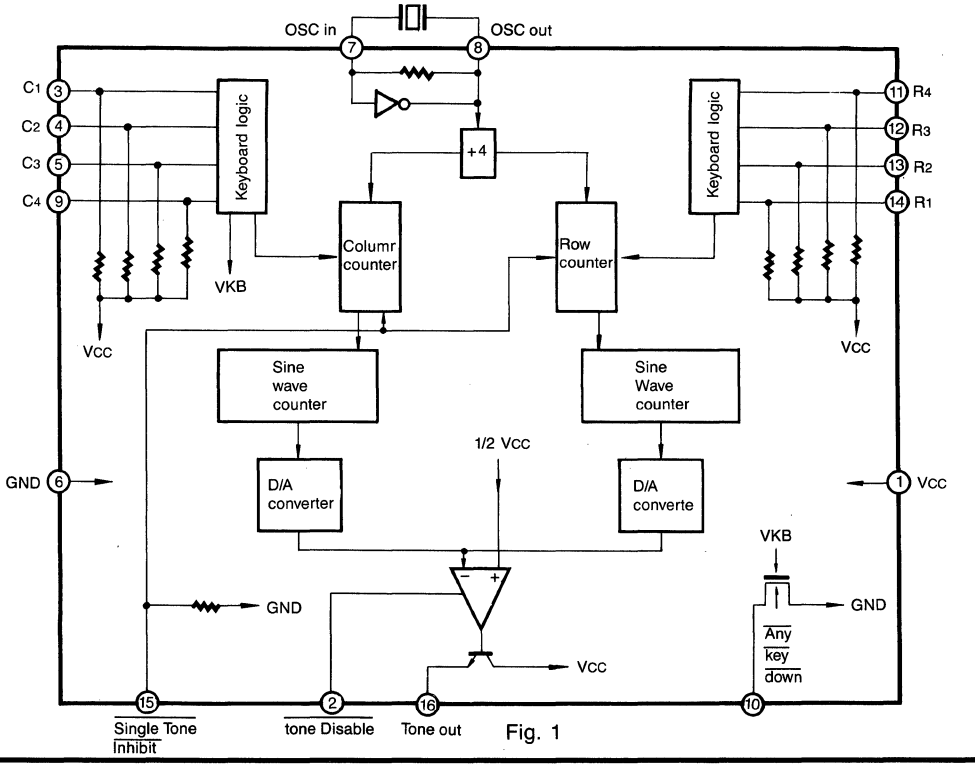


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10.5	V
Any Input Relative to V_{CC} (Except Pin 10)	V_N	0.3	V
Any Input Relative to GND (Except Pin 10)	V_N	−0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	Topr	−30 ~ +60	°C
Storage Temperature	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(−30°C < T_a < 60°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		3		10	V
Input "0"	V_{IL}		0		$0.3V_{CC}$	V
Input "1"	V_{IH}		$0.7V_{CC}$		V_{CC}	V
Input Pull-Up Resister	R_I		20		100	KΩ
$\overline{\text{Tone Disable}}$	T_D	Note 4	0		$0.3V_{CC}$	V
Tone Output	V_{OUT}	Note 1	−10		−7	dBm
Preemphasis, High Band			2.4	2.7	3	dB
Output Distortion, Measured in Terms of Total Out-of-Band Power Relative to RMS sum of Row and Column fundamental Power		Note 2			−20	dB
Rise Time	T_{RISE}	Note 3		2.8	5	m_{SEC}
$\overline{\text{Any Key Down}}$ Sink Current to GND	I_{AKD}	At V_{OUT} = 0.5V	500			uA
$\overline{\text{ADK}}$ Off Leakage Current	I_{AKDO}	At V_{OUT} = 5V			2	uA
Supply Current Operating	I_{SO}	At V_{CC} = 3.5V Note 6			2	mA
Supply Current Standby	I_{SST}	At V_{CC} = 10V Note 5			200	uA
Tone Output-No Key Down	NKD				−80	dBm

Note: 1. Single-tone, low-group. Any V_{CC} between 3.4V and 3.6V, odBm=0.775V, R_{LOAD} = 10K see test circuit Fig 2.
2. Any dual-tone. Any V_{CC}: Any V_{CC} between 3.4V to 10.0V. Any dual-tone.
3. Time from a valid keystroke with no bounce to allow the waveform to go from min to 90% of the final magnitude of either frequency. Crystal parameters defined as R_S = 100Ω L=96mH, C=0.02pF, and C_h = 5pF, $V_{CC} \geqq 3.4V$, f=3.57954MHz±0.02%.
4. Only tones will be disabled when $\overline{\text{TD}}$ is taken to logical "0" other chip functions may activate. Pill-up resistor on $\overline{\text{TD}}$ input will meet same spec as other inputs. Logic 0=GND
5. Stand-by condition is defined as no keys activated, $\overline{\text{TD}}$=Logical 1, $\overline{\text{Single Tone Inhibit}}$=Logical 0.
6. One key depressed only. Outputs unloaded.

PIN CONNECTIONS

PIN 1: Supply Voltage V_{CC}
PIN 2: $\overline{\text{Tone Disable}}$ Input
PIN 3: $\overline{\text{Column Input}}$ C_1
PIN 4: $\overline{\text{Column Input}}$ C_2
PIN 5: $\overline{\text{Column Input}}$ C_3
PIN 6: GND
PIN 7: OSC IN
PIN 8: OSC OUT
PIN 9: $\overline{\text{Column Input}}$ C_4
PIN 10: $\overline{\text{Any Key Down}}$
PIN 11: $\overline{\text{Row Input}}$ R_4
PIN 12: $\overline{\text{Row Input}}$ R_3
PIN 13: $\overline{\text{Row Input}}$ R_2
PIN 14: $\overline{\text{Row Input}}$ R_1
PIN 15: $\overline{\text{Single Tone in Hibit}}$
PIN 16: Tone Output

Tone Output Test Circuit

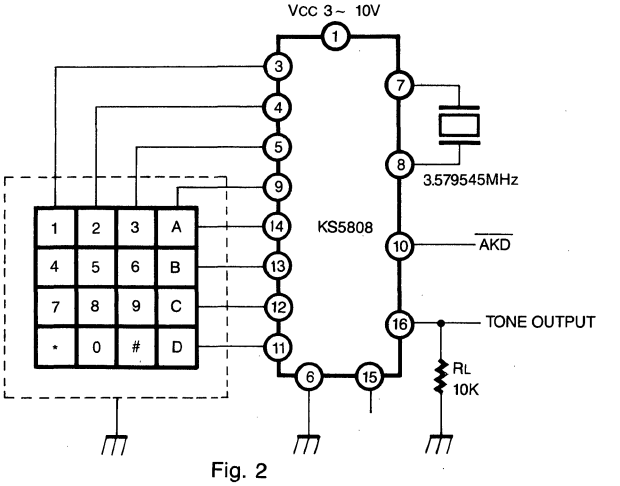


Fig. 2

FUNCTION DESCRIPTION

1. Oscillator

The network contains an on-board inverter with sufficient loop gain to provide oscillation when used with a low cost television color-burst crystal. The inverter's input is osc in (pin 7) and output is osc out (pin 8). The circuit is designed to work with a crystal cut to 3.579545MHz to give the frequencies in table 1. The oscillator is disabled whenever a keyboard input is not sensed.

Table 1: Standard DTMF and output frequencies of the KS5808

Item / Key	f	Standard DTMF Hz	Tone Output Frequency using 3.57954MHz Crystal Hz	Deviation from Standard %
ROW	f1	697	701.3	+0.62
	f2	770	771.4	+0.19
	f3	852	857.2	+0.61
	f4	941	935.1	−0.63
COL	f5	1209	1215.9	+0.57
	f6	1336	1331.7	−0.32
	f7	1477	1471.9	−0.35
	f8	1633	1645.0	+0.73

Most crystals don't vary more than 0.02%. Any crystal frequency deviation from 3.5795MHz will be reflected in the tone output frequency.

2. Output Waveform

The row and column output waveforms are shown in Figure 3. These waveforms are digitally synthesized using on-chip D/A converters. Distortion measurement of these unfiltered waveforms will show a typical distortion of 7% or less. The on-chip operational amplifier of the KS5808 mixes the row and column tones together to result in a dual-tone waveform.

Spectral analysis of this waveform will show that typically all harmonic and intermodulation distortion components will be-30dB down when referenced to the strongest fundamental (column tone). Figures 6 and 7 show a typical dual tone waveform and its spectral analysis.

Typical Sinewave Output

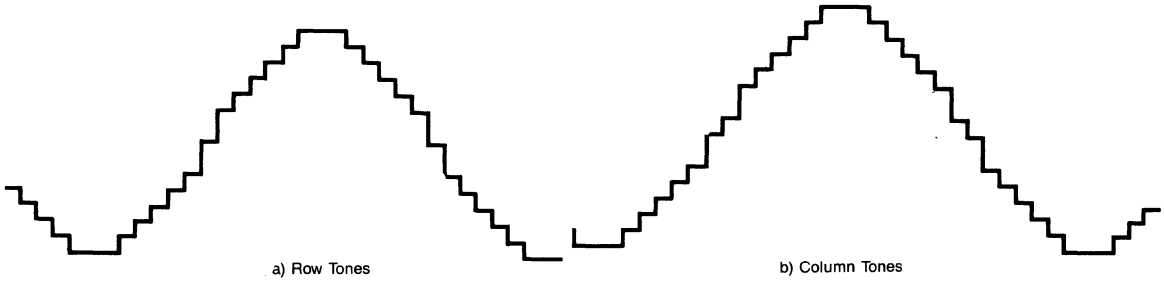


Fig. 3

3. Output Tone Level

The output tone level of the KS5808 is proportional to the applied DC supply voltage. Operation will normally be with a requlated supply. This results in enhanced temperature stability, since the supply voltage may be made temperature stable.

4. Keyboard Configuration

Each keyboard input is standard CMOS with a pull-up resistor to V_{CC}. These inputs may be controlled by a keyboard or electronic means. Open collector TTL or standard CMOS (operated off same supply as the KS5808) may be used for electronic control.

The switch contacts used in the keyboards may be void of precious metals, due to the CMOS network's ability to recognize resistance up to 1KΩ as a valid key closure.

2 of 8 DTMF keyboard

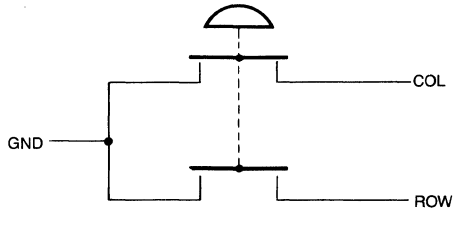


Fig. 4

Electronic Pulses

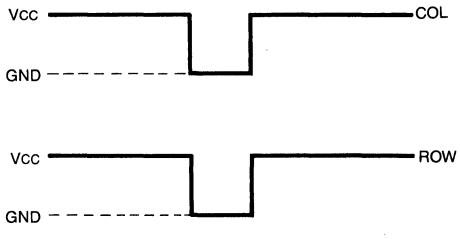


Fig. 5

PIN DESCRIPTIONS

1. Row and Column Input (Pin 3, 4, 5, 9, 11, 12, 13, 14)

With single tone inhibit at V_{CC} connection of GND to a single column will cause the generation of that column tone. Connection of GND to more than one column will result in no tones being generated. The application of GND to only a row pin or pins has no effect on the circuit. There must always be at least one column connected to GND for row tones to be generated. If a single row tone is desired, it mey be generated by tying any two column pins and the desired row pin to GND. Dual tones will be generated if a single row pin and a single column pin are connected to GND.

2. $\overline{\text{Any Key Down}}$ Output (Pin10)

The any key down output is used for electronic control of receiver and/or transmitter switching and other desired functions. It switches to GND when a keyboard button is pushed and is open circuited when not. The AKD output switches regardless of the tone disable and single tone inhibit inputs.

3. $\overline{\text{Tone Disable}}$ Input (Pin 2)

The tone disable input is used to defeat tone generation when the keyboard is used for other functions besides DTMF signaing. It has a pull-up to V_{CC} and when tied to GND tones are inhibited. All other chip functions operate ncrmally.

4. $\overline{\text{Single Tone}}$ Inhibit Input (Pin 15)

The single tone inhibit input is used to inhibit the generation of other than dual tones. It has a pull-down to GND and when floating or tied to GND, any input situation that would normally result in a single tone will now result in a single tone will now result in no tone, with all other chip functions operating normally.

When forced to V_{CC} single or dual tones may be generated as described in the paragraph under row and column inputs.

5. Tone Output (Pin 16)

The tone output pin is connected internally in the KS5808 to the emitter of an NPN transistor whose collector is tied to V_{CC}. The input to this transistor is the on-chip operational ampifier which mixes the row and column tones together and provides output level regulation.

POWER DISSIPATION VERSUS TEMPERATURE

Typical Dual Tone Waveform
(ROW 1, Column 1)

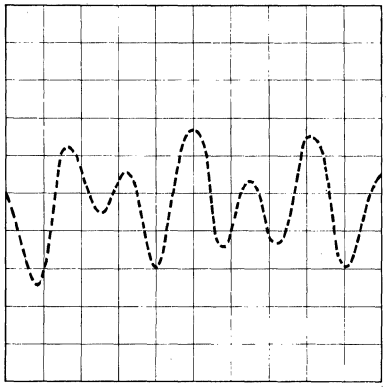


Fig. 6

Spectral Analysis of Waveform
(Vert: 10dB/Div, Hori: 1KHz/Div)

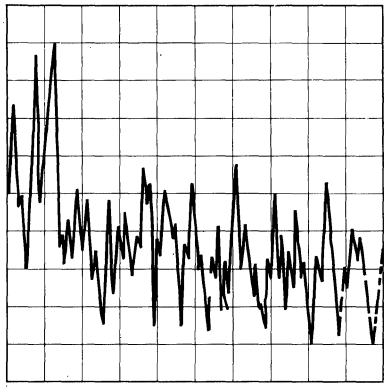


Fig. 7

POWER DISSIPATION VERSUS TEMPERATURE

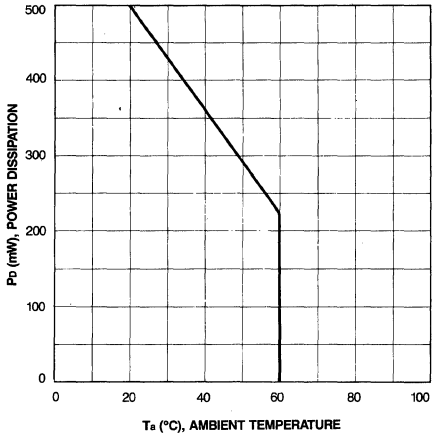
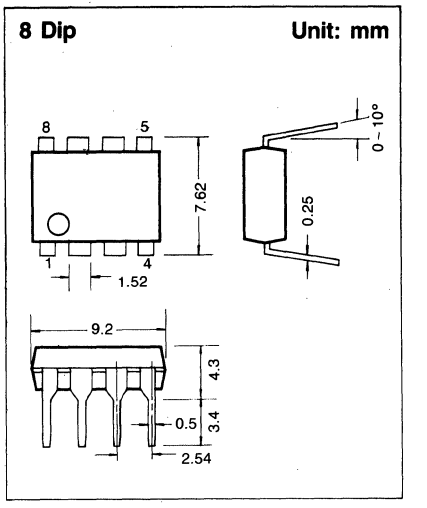


Fig. 8

OPERATING CYCLE VS BANDWIDTH

TONE DECODER

The LM567C is a monolithic phase locked loop system designed to provide a saturated transistor switch to GND, when an input signal is present within the passband. External components are used to independently set center frequency bandwidth and output delay.



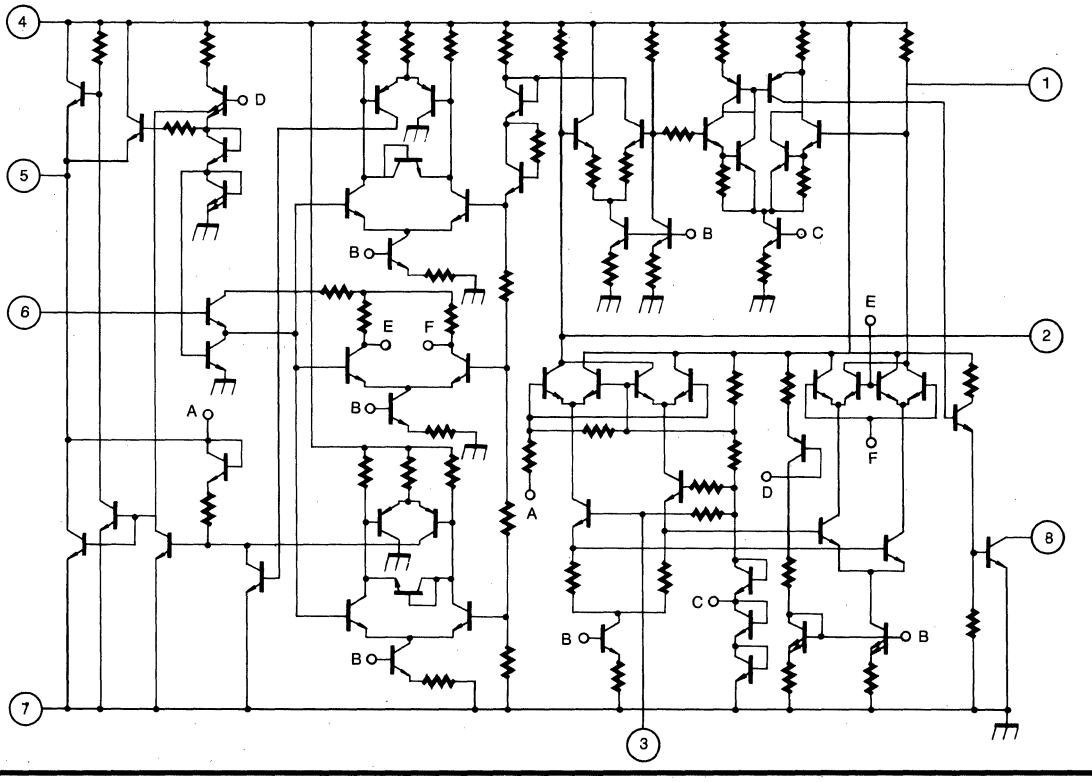
FEATURES

- **Wide frequency range (0.01Hz — 500kHz).**
- **Bandwidth adjustable from 0 to 14%**
- **Logic compatible output with 100mA current sinking capability.**
- **Inherent immunity to false signals.**
- **High rejection of out-of-band signals and noise.**
- **Frequency range adjustable over 20:1 range by an external resistor.**

APPLICATIONS

- Touch Tone Decoder
- Wireless Intercom.
- Communications paging decorders.
- Frequency monitoring and control.
- Ultrasonic controls (remote TV etc.)
- Carrier current remote controls.
- Precision oscillator.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{CC}	10	V
Input Voltage	V_{IN}	−10 ~ V_{CC} +0.5	V
Output Voltage	V_O	15	v
Power Dissipation	Pd	300	mW
Operating Temperature	Topr	0 ~ +70	°C
Storage Temperature	Tstg	−65 ~ +150	°C

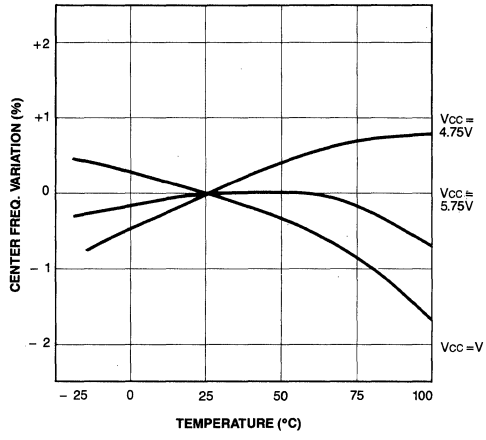
ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V, T_a=25°C)

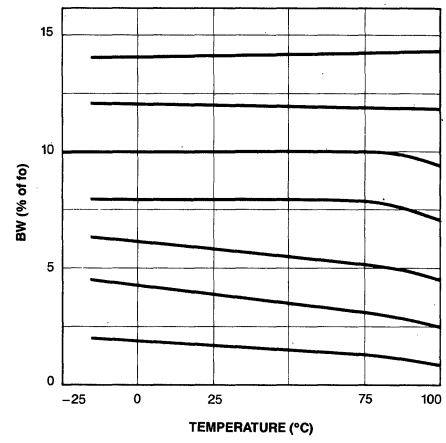
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage Range	V_{CC}		4.75	5.0	9.0	V
Supply Current Quiescent	I_{CC}-1	R_L=20K		7	10	mA
Supply Current Activated	I_{CC}-2	R_L=20K		12	15	mA
Quiescent Power Dissipation	P_{QD}			35		mW
Highest Center Frequency	H_{FO}	R_L=20K	100	500		KHz
Center Frequency Stability		0°C to 70°C		35±60		ppm/°C
Center Frequency Shift With Supply Voltage	F_{OV}			0.7	2	%/V
Largest Detection Bandwidth	B.W		10	14	18	% of fo
Largest Detection B.W Skew	B.Ws			2	3	% of fo
Largest Detection Bandwidth Variation With Supply Voltage	B.Wv	4.75 ~ 6.75V		±1	±5	%/V
Largest Detection Bandwidth Variation With Temperature	B.Wt			±0.1	±0.5	%/°C
Input Resistance	R_{IN}			20	25	Kohm
Smallest Detectable Input Voltage	V_{IN}-1	I_L=100mA, fi=fo		20	25	mVrms
Largest No Output Input Voltage	V_{IN}-2		10	15		mVrms
Greatest Simultaneous Outband Signal To Inband Signal Ratio	S1/Sd	R_L=20k V_{IN}=300mV_{RMS} fi=fo=100KHz		+6		dB
Minimum Input Signal to Wideband Noise Ratio	S2/Sd	fi_1=140KHz fi_2=60KHz		−6		dB
Fastest On-Off Cycling Rate	F_{OUT}	R_L=20K		fo/20		
Output Leakage Current	I_{CO}	V_{IN}=25mV_{RMS}		0.01	25	μA
Output Saturaton Voltage	V_{SAT}-1	I_L=30mA		0.2	0.4	V
	V_{SAT}-2	I_L=100mA		0.6	1.0	V
Output Fall Time	T_F	R_L=50		30		nS
Output Rise Time	T_R	R_L=50		150		nS

TYPICAL CHARACTERISTICS

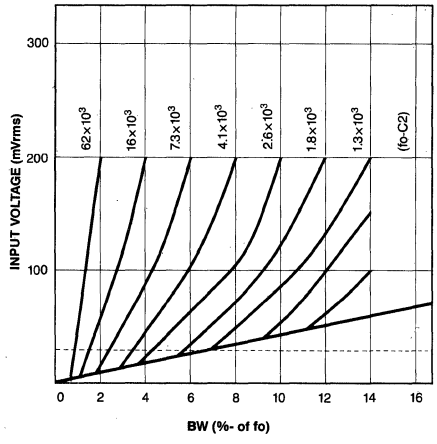
CENTER FREQ. VS TEMPERATURE



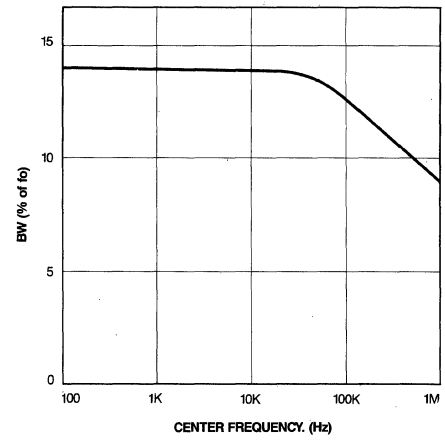
TYP. BW VS TEMPERATURE



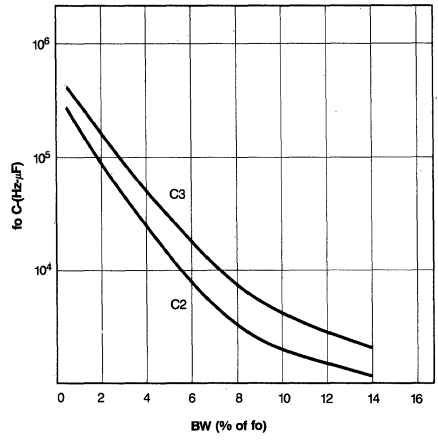
BW VS INPUT VOLTAGE.



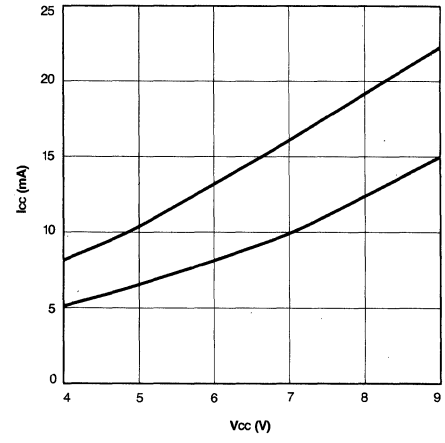
BW VS CENTER FREQENCY



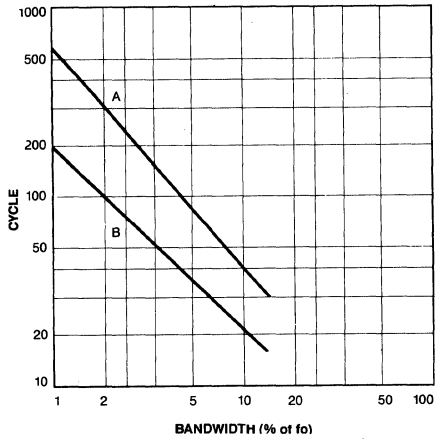
BW (C2, C3 CHARCT.)



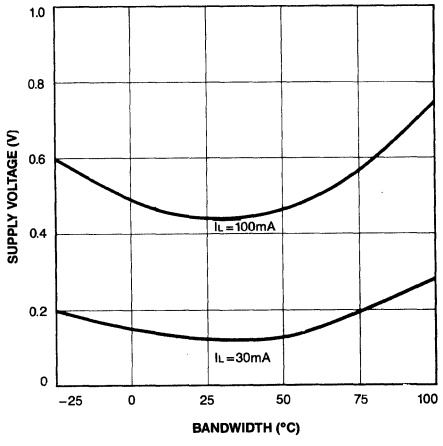
CURRENT DRAIN VS. VCC



OPERATING CYCLE VS BANDWIDTH



OUTPUT SATURATION VOLTAGE VS AMBIENT TEMPERATURE



BLOCK DIAGRAM

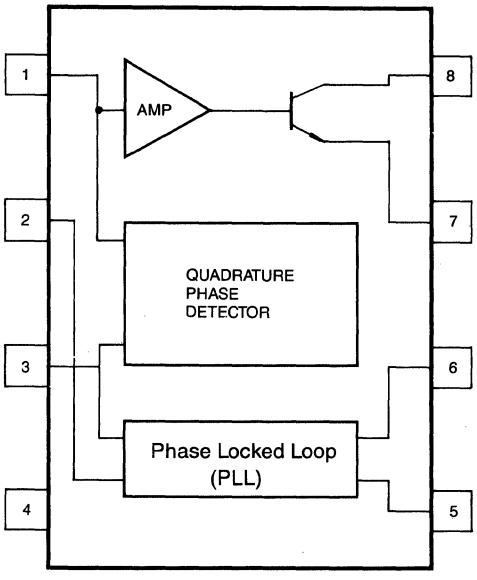
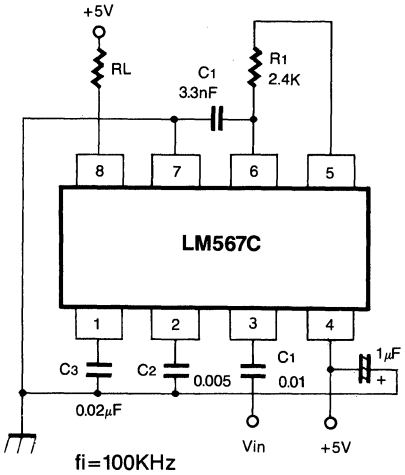


Fig. 2

AC TEST CIRCUIT



fi=100KHz
Note: Adjust for fo=100KHz

Fig. 3

PIN CONNECTIONS

Pin 1: Output Filter
Pin 2: Loop Filter
Pin 3: Input
Pin 4: Vcc
Pin 5: Timing Resistor
Pin 6: Timing Capacitor
Pin 7: GND
Pin 8: Output

APPLICATION NOTE

Center frequency is given bv:

$$fo = \frac{1}{R1 \cdot C1}$$

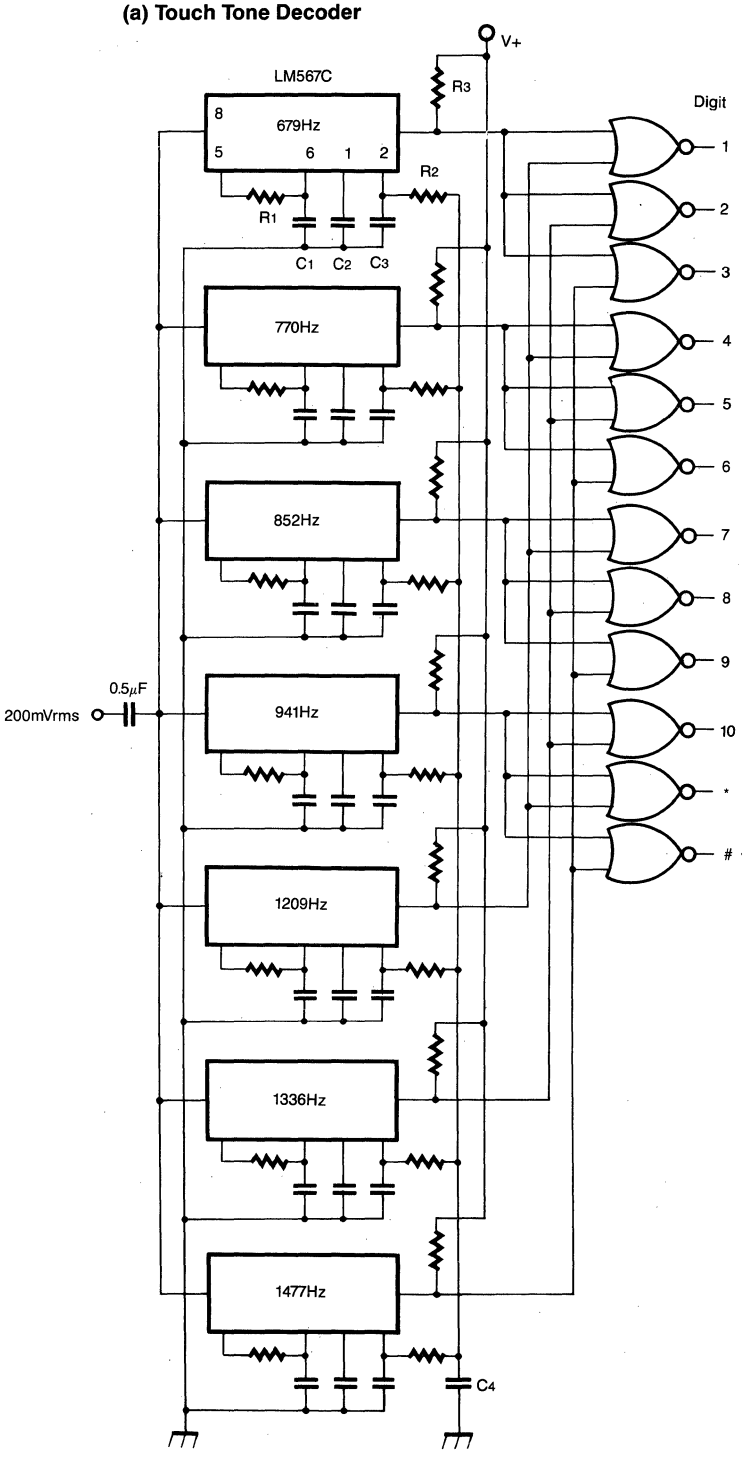
Bandwidth BW is given by:

$$BW \approx 1070 \sqrt{\frac{V_i}{fo\ C_2}} (\%)$$

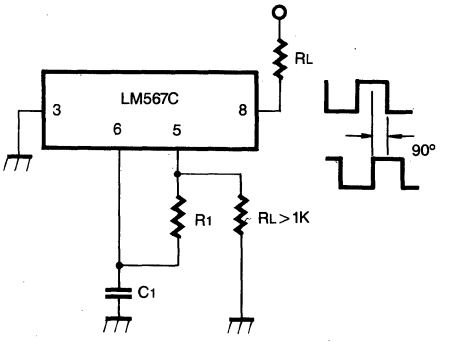
Where Vi ≤ 200mVrms
C2: uF μF

APPLICATION CIRCUIT

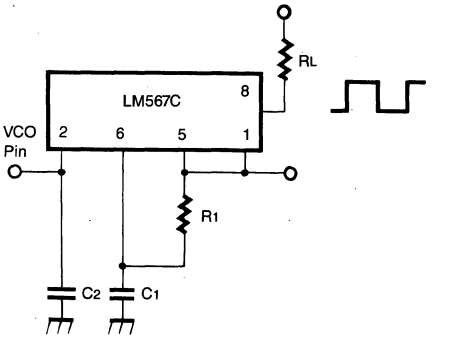
(a) Touch Tone Decoder



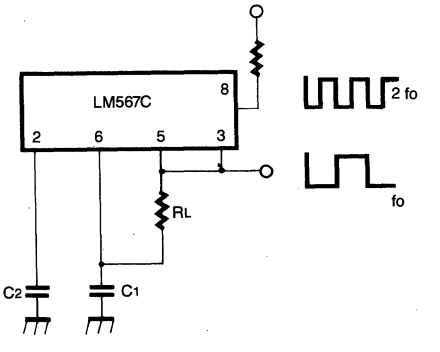
(b) 2-Phase Oscillator



(c) Variable Oscillator



(d) Frequency Doubler



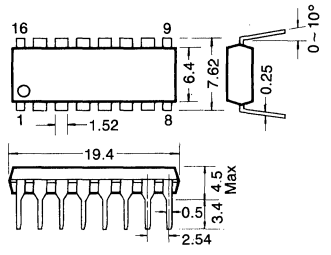
R1 = 6.8K to 15K
R2 = 4.7K
R3 = 20K

C1 = 0.1μF
C2 = 1μF
C3 = 2.2μF
C4 = 200μF

LOW POWER NARROW BAND FM IF

The MC3361 is designed for use in FM dual conversion communication equipment. It contains a complete narrow band FM demodulation system operable to less than 2V supply voltage.

16 Dip Unit: mm



FEATURES

- **Includes: Oscillator, Mixer, Limiting Amp, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch**
- **Stable operation with wide supply voltage (1.8V to 7.0V)**
- **Low drain current (4.0mA Typ. at V_{CC}=4.0V)**
- **Excellent Input Sensitivity (−3dB limiting, 2.0μVrms Typ.)**
- **Minimum number of external parts required.**

BLOCK DIAGRAM

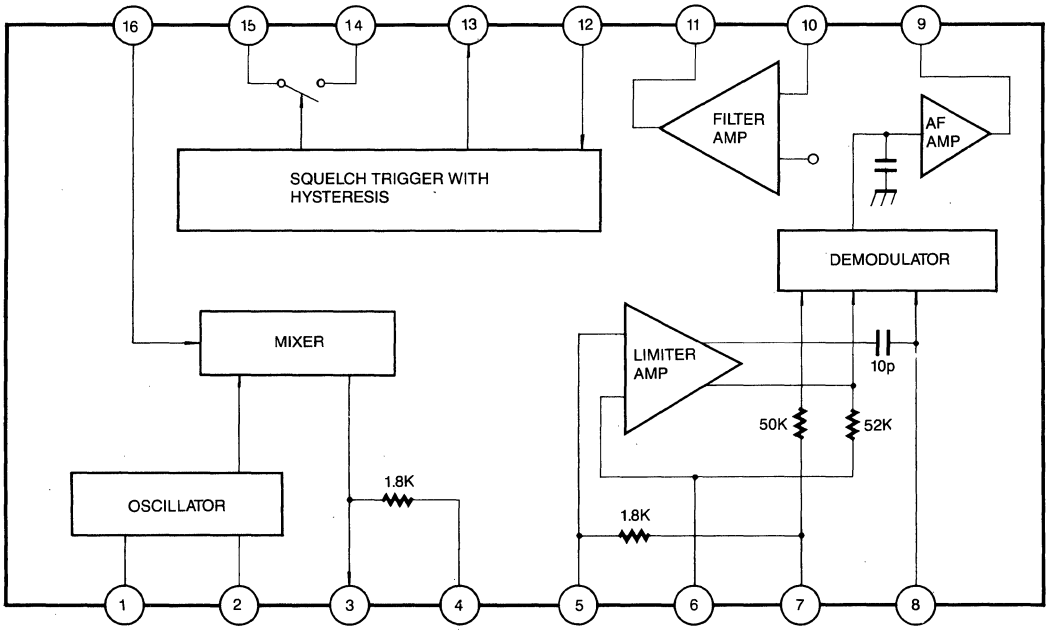


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Detector Input Voltage	—	1.0	V_{P-P}
Input Voltage ($V_{CC} \geq 4.0V$)	V_{16}	1.0	Vrms
Mute Function	V_{14}	−0.5 ~ +5.0	Vpeak
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} =4.0V, f=3KHz, f_{mod} =1KHz, T_a =25°C, Unless Otherwise Specified)

Characteristic	Symbol	Test Condition	Spec			Unit
			Min	Typ	Max	
Circuit Current	I_{CC}	Squelch Off Squelch On		4.0 6.0		mA
Input Limiting Voltage	$V_{IN}L$	−3dB Limiting		2.0		μV
Detector Output Voltage	V_7			2.0		V
Detector Output Impedance	Z_{OD}			400		ohm
Recodered Audio Output Voltage	V_O	V_{IN} =10mV	100	150		mVrms
Filter Gain	A_{VF}	f = 10KHz, V_{IN} = 5mV	40	48		dB
Filter Output Voltage	V_{OF}			1.5		V
Trigger Hysteresis	V_{TH}			50		mV
Mute Function Low	R_{OL}			10		ohm
Mute Function High	R_{OH}			10		Mohm
Scan Function Low	V_{14L}	Mute Off (V_{12} = 2V)			0.5	V
Scan Function High	V_{14H}	Mute On (V_{12} =GND)	3.0			V
Mixer Conversion Gain	A_{VM}			24		dB
Mixer Input Resistance	R_I			3.3		Kohm
Mixer Input Capacitance	C_I			2.2		pF

PIN CONNECTIONS

Pin 1: Oscillator
Pin 2: Oscillator
Pin 3: Mixer Output
Pin 4: Vcc
Pin 5: Limiter Input
Pin 6: Decoupling
Pin 7: Limiter Output
Pin 8: Quad Coil
Pin 9: Recovered Audio
Pin 10: Filter Input
Pin 11: Filter Output
Pin 12: Squelch In
Pin 13: Scan Control
Pin 14: Mute
Pin 15: GND
Pin 16: Mixer Input

TEST CIRCUIT

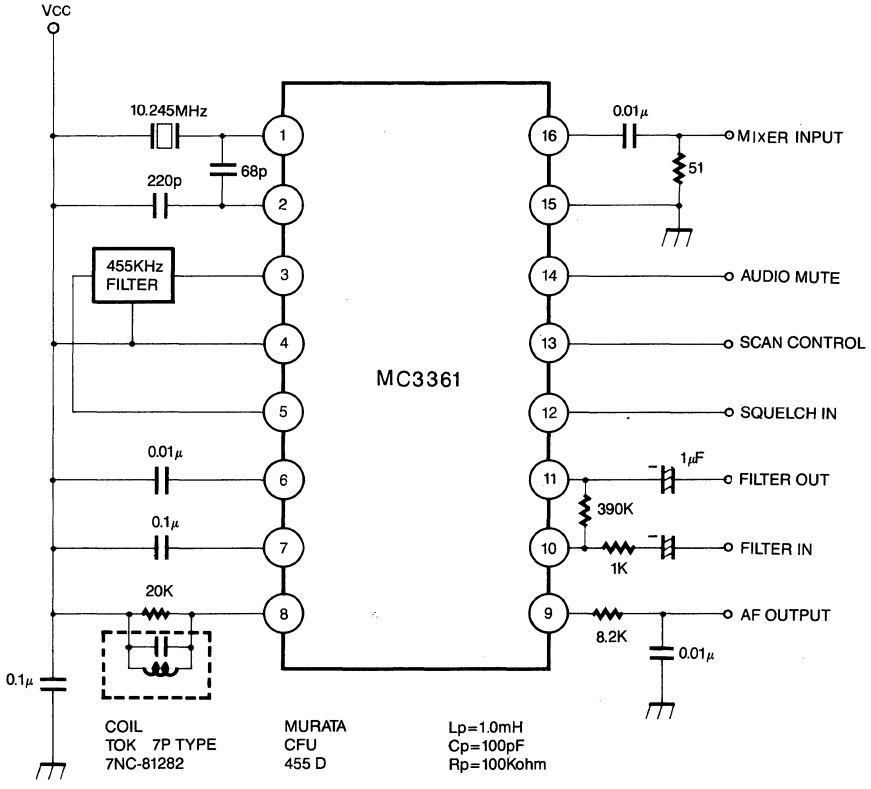


Fig. 2

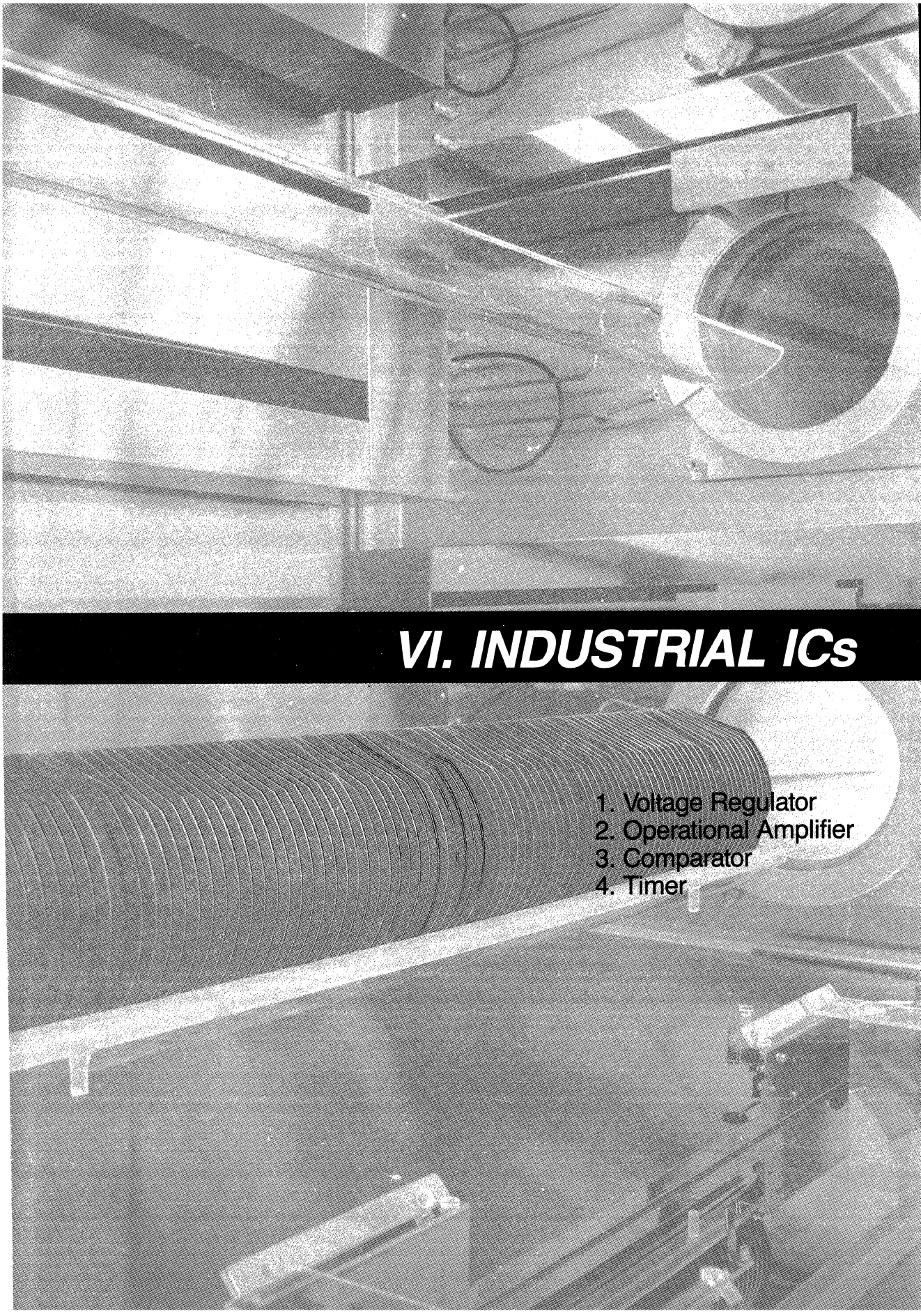
CIRCUIT DESCRIPTION (see block diagram)

The MC3361 functions include an oscillator, mixer, FM IF limiting amplifier, FM demodulator, OP-AMP, scan control and mute switch.

The mixer combines the crystal controlled oscillator to convert the input frequency from 10.7MHz to an intermediate frequency of 455KHz, where, after external bandpass filtering, most of the amplification is done. A conventional quadrature detector is used to demodulate the FM signal. The Q of the quad coil, which is determined by the external resistor placed across it, has multiple affects on the audio output. Increasing the Q increases output level because of nonlinearities in the tank phase characteristic.

After detection and de-emphasis, the audio output at pin 9 is partially filtered, then buffered by an emitter follower. The signal still requires volume control and further amplification before driving loudspeaker.

The op amp inverting input (pin 10) which is internally referenced to 0.7V, receives DC bias from the output of pin 11 through the external feedback network. It is normally utilized as either a bandpass filter to extract a specific frequency from th audio output, such as a ring or dial-tone, or as a highpass filter to detect noise due to no input at the mixer. This information is applied to pin 12. An external positive bias to pin 12 sets up the squelch trigger circuit such that pin 13 is low and the audio mute (pin 14) is open circuit. If pin 12 is pulled down to 0.7V by the noise or tone detector, pin 13 will rise to approximately 0.5Vdc and pin 14 is internally short circuited to ground. There is 50mV of hysteresis at pin 12 which effectively prevents jitter. Audio muting is accomplished by connecting pin 14 to a high-impedance ground-reference point in the audio path between pin 9 and the audio amplifier.



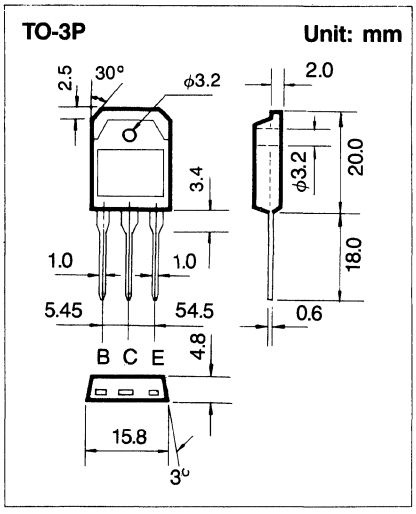
VI. INDUSTRIAL ICs

1. Voltage Regulator
2. Operational Amplifier
3. Comparator
4. Timer

E-TERMINAL POSITIVE VOLTAGE REGULATOR

The LM323 is a three-terminal positive regulator with a preset 5V output and a load driving capability of 3 Amps.

New circuit design and processing techniques are used to provide the high output current without sacrificing the regulation characteristics of lower current devices.



FEATURES

- **3 Amp output current**
- **Internal current and thermal limiting**
- **0.01Ω typical output impedance**
- **7.5 minimum input voltage**

SCHEMATIC DIAGRAM

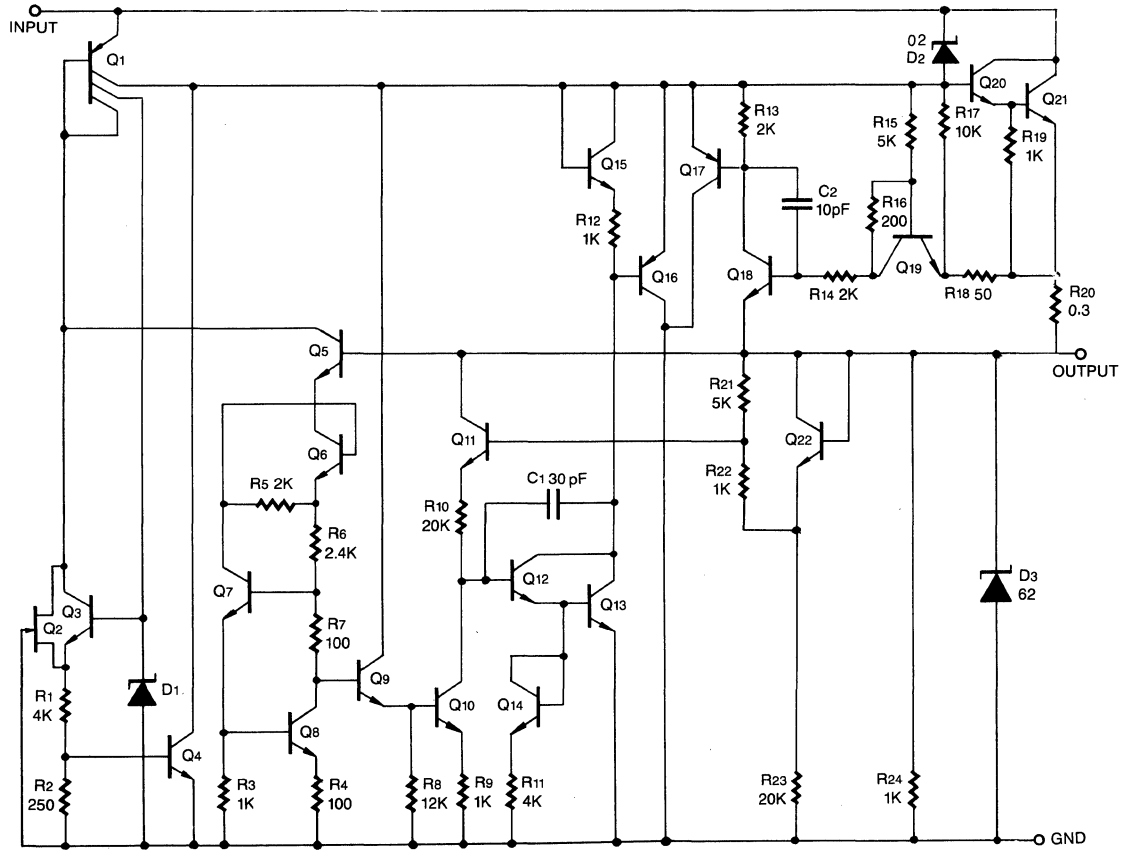


Fig. 1

ABSOLUTE MAXIMUM RATINGS

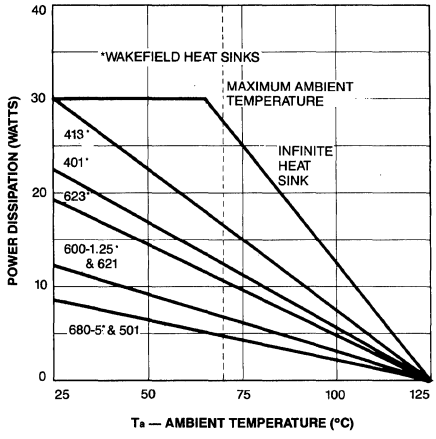
Characteristic	Symbol	Value	Unit
Input Voltage	V_C	20	V
Operating Junction Temperature	T_{opr}	0 ~ +125	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

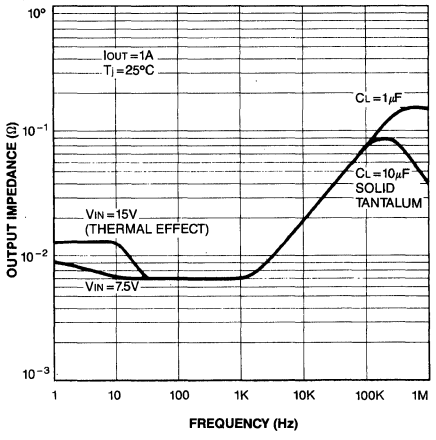
(0°C ≤ T_J ≤ 125°C unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage	V_O	T_J = 25°C V_{IN} = 7.5V, I_{OUT} = 0	4.8	5	5.2V	
		7.5V ≤ V_{IN} ≤ 15V 0 ≤ I_{OUT} ≤ 3A, P ≤ 30W	4.75		5.25	V
Line Regulation	ΔV_O	T_J = 25°C 7.5V ≤ V_{IN} ≤ 15V		5	25	mV
Load Regulation	ΔV_O	T_J25°C, V_{IN} ≤ 15V 0 ≤ I_{OUT} ≤ 3A		25	100	mV
Quiescent Current	I_D	7.5V ≤ V_{IN} ≤ 15V 0 ≤ I_{OUT} ≤ 3A		12	20	mA
Output Noise Voltage	E_N	T_J = 25°C, 10Hz ≤ f ≤ 100KHz		40		μV_{RMS}
Short Circuit Current	I_{SC}	T_J = 25°C, V_{IN} = 15V		3	4.5	A
		T_J = 25°C, V_{IN} = 7.5V		4	5	A
Thermal Resistance Junction to Case	Q_{J-C}			3		°C/W

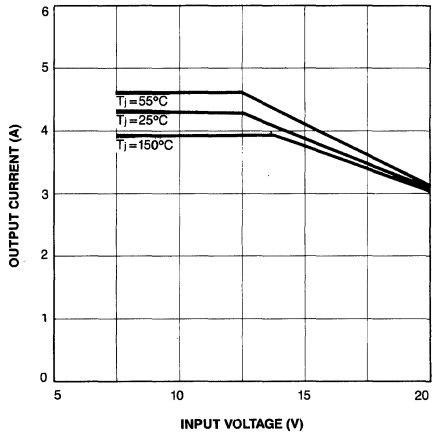
MAXIMUM AVERAGE POWER DISSIPATION



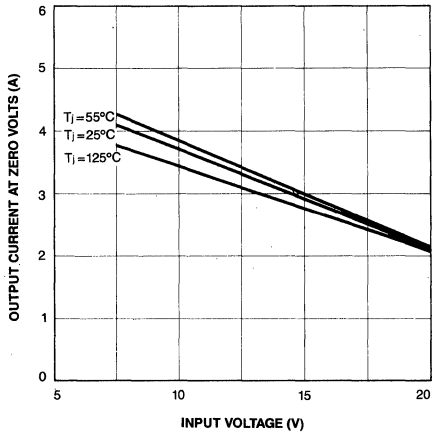
OUTPUT IMPEDANCE



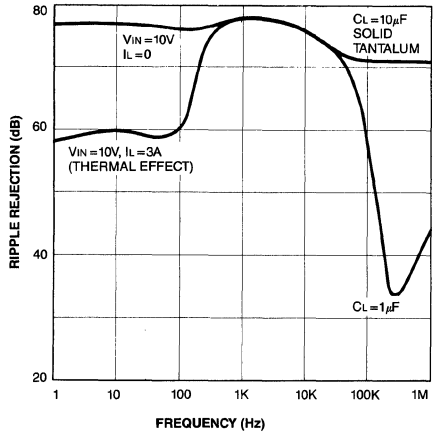
PEAK AVAILABLE OUTPUT CURRENT



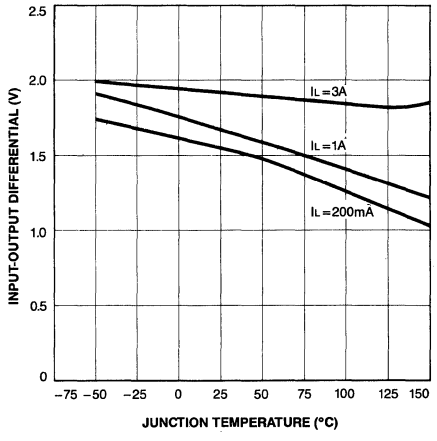
SHORT CIRCUIT CURRENT



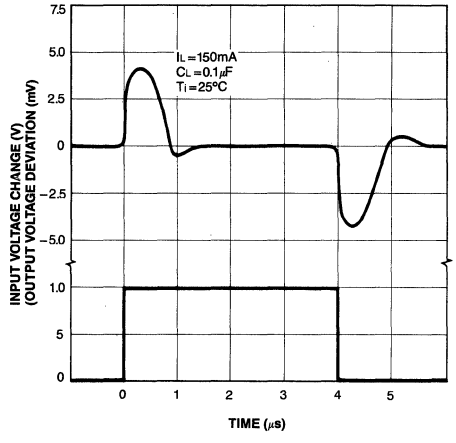
RIPPLE REJECTION



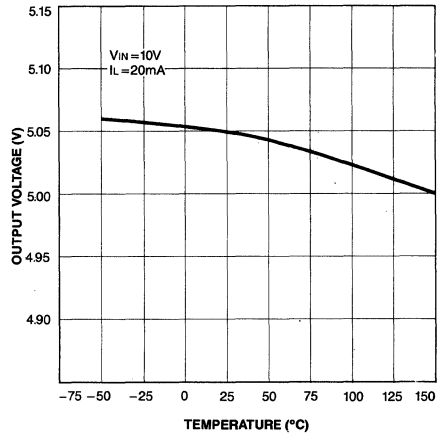
DROPOUT VOLTAGE



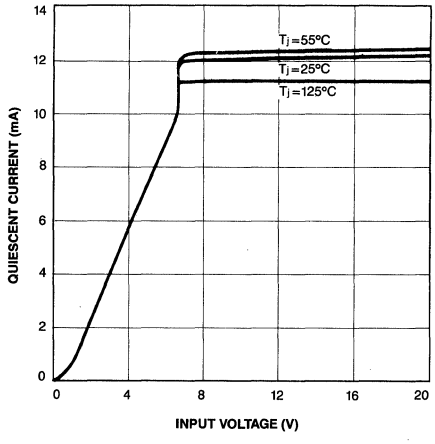
LINE TRANSIENT RESPONSE



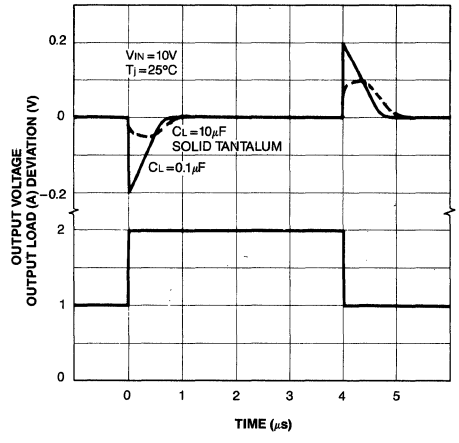
OUTPUT VOLTAGE



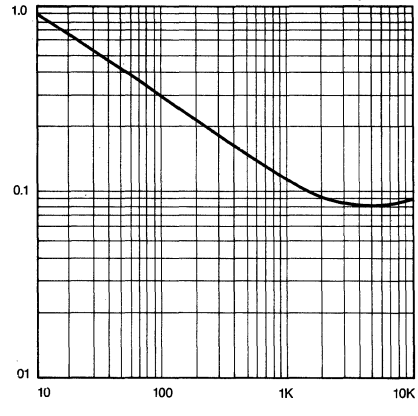
QUIESCENT CURRENT



LOAD TRANSIENT RESPONSE



OUTPUT NOISE VOLTAGE



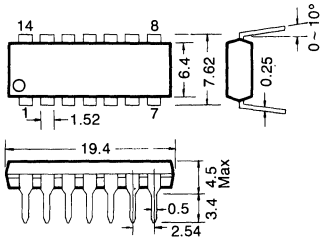
PRECISION VOLTAGE REGULATOR

The LM723C is a monolithic integrated circuit voltage regulator featuring high ripple rejection, excellent input and load regulation, excellent temperature stability, and low standby crrent.

FEATURES

- **Positive or Negative Supply Operation.**
- **0.01% line and load regulation**
- **Output voltage adjustable from 2 to 37 volts.**
- **Output current to 150mA without external pass transistor**

14 Dip **Unit: mm**



SCHEMATIC DIAGRAM

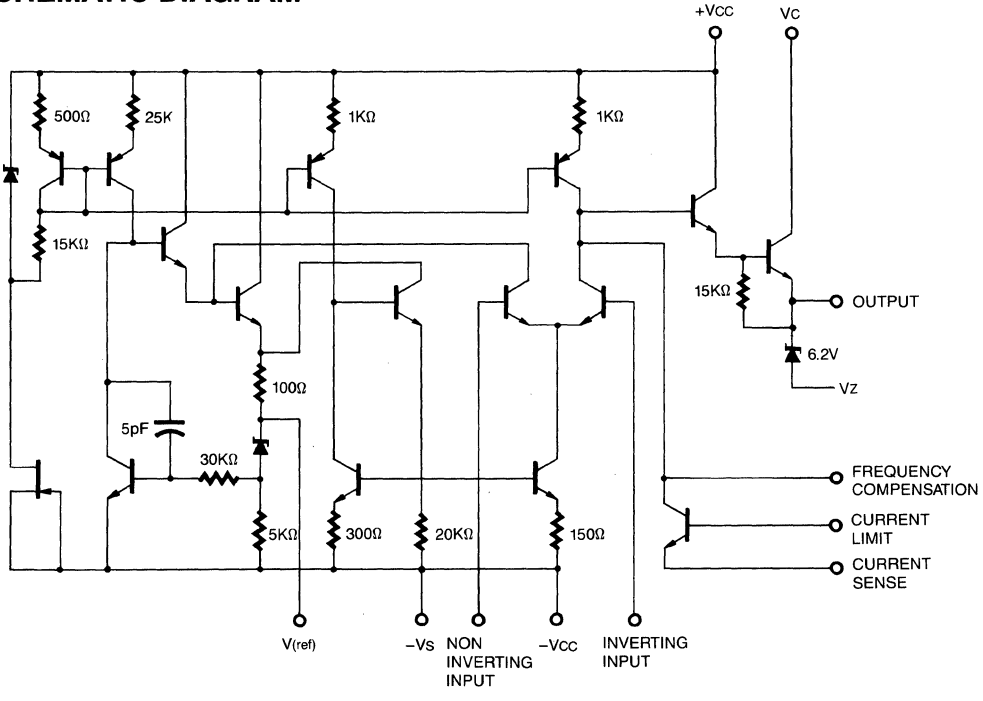
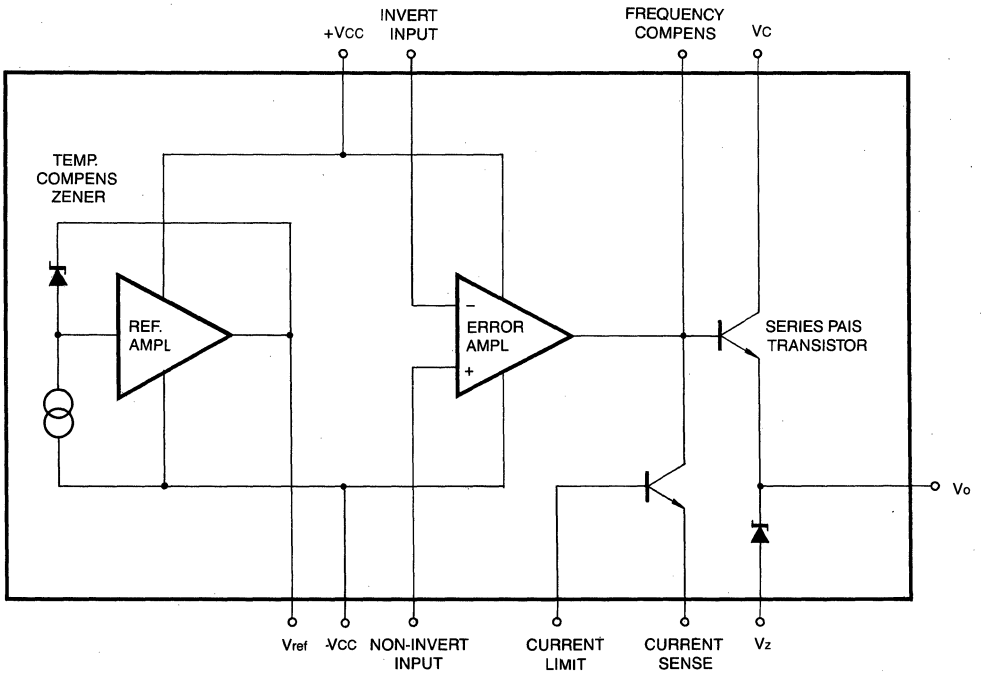


Fig. 1

ABSOLUTE MAXIMUM RATINGS ($T_a = 25°C$)

Characteristic	Symbol	Value	Unit
Pulse Voltage from V_+ to V_-	V_{in} (P)	50	V
Continuous from V_+ to V_-	V_{in}	40	V
Input-Output Voltage Differential	V_{in}-V_d	40	V
Maximum Output Current	I_L	150	mA
Current from V_{ref}	I_{ref}	15	mA
Current from V_z	I_Z	25	mA
Differential Input Voltage	V_{id}	±5.0	V
Voltage Between Non-Inverting-Input and V	V_{IE}	8.0	V
Power Dissipation and Thermal	P_d	1.25	W
Characteristics Plastic Package (T_a=25°C)			
Operating Temperature	T_{opr}	0~+70	°C
Storage Temperature	T_{stg}	−65~150	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, $T_a = 25°C$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	$\frac{\Delta V_o}{\Delta V_i}$	$V_i = 12$ to 15V $V_i = 12$ to 40V		0.01 0.1	0.1 0.5	%
		$V_i = 12$ to 15V $0°C \leq T_a \leq 70°C$			0.3	
Load Regulation	$\frac{\Delta V_o}{V_o}$	$I_o = 1$ to 50mA		0.03	0.2	%
		$0°C \leq T_a \leq 70°C$ $I_o = 1$ to 10mA			0.6	
Reference Voltage	V_{ref}	$I_{ref} = 160\mu A$	6.8	7.15	7.5	V
Ripple Rejection	SVR	f=100Hz to 10KHz $C_{ref} = 0$ $C_{ref} = 5\mu F$		 74 86		 dB dB
Output Voltage Drift	$\triangle V_o / \triangle T$				150	$\frac{ppm}{°C}$
Short Circuit Current Limiting	I_{sc}	$R_{sc} = 10\Omega$, $V_o = 0$		65		mA
Input Voltage Range	V_i		9.5		40	V
Output Voltage Range	V_o		2		37	V
Voltage Drop	V_i-V_o		3		38	V
Quiescent Drain Current	I_d	$I_o = 0$ $V_i = 30V$		2.3	4	mA
Long Term Stability				0.1		$\frac{\%}{1000hrs}$
Output Noise Voltage	^eN	BW = 100Hz to 10KHz $C_{ref} = 0$ $C_{ref} = 5\mu F$		 20 2.5		 μV μV
Output Zener Voltage	V_z	$I_z = 1mA$	6.9		7.7	V

Table 1 — Resistor values (KΩ) for standard output voltage

Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10%			Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10%		
		R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3	3, 6	4.12	3.01	1.8	0.5	1.2	−6*	5	3.57	2.43	1.2	0.5	0.75
+5	3, 6	2.15	4.99	0.75	0.5	2.2	−9	5	3.48	5.36	1.2	0.5	2
+6	3, 6	1.15	6.04	0.5	0.5	2.7	−12	5	3.57	8.45	1.2	0.5	3.3
+9	4, 6	1.87	7.15	0.75	1	2.7	−15	5	3.65	11.5	1.2	0.5	4.3
+12	4, 6	4.87	7.15	2	2	3	−28	5	3.57	24.3	1.2	0.5	10
+15	4, 6	7.87	7.15	3.3	1	3							
+28	4, 6	21	7.15	5.6	1	2							

Note: *V_{CC} must be connected to a +3V or greater supply.

Table II — Formulae for intermediate output voltages

Outputs from +2 to +7 volts Fig. 3 $V_o = [V_{ref} \times \frac{R_2}{R_1 + R_2}]$	Foldback Current Limiting $I_{KNEE} = [\frac{V_o R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts Fig. 4, 6 $V_o = [V_{ref} \times \frac{R_1 + R_2}{R_2}]$	Output from −6 to −250 volts Fig. 5 $V_o = [\frac{V_{ref}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	

APPLICATION INFORMATION

Basic low voltage regulator (V_o = 2 to 7V)

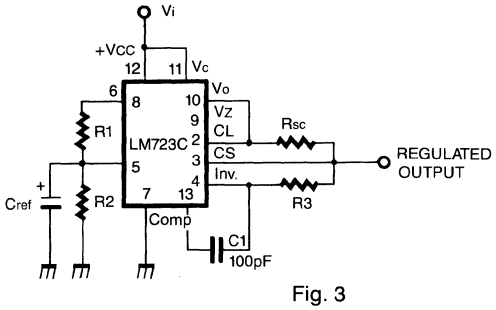


Fig. 3

Note: R3=R1 • R2 (R1+R2) for minimum temperature drift.
R3 may be eliminated for minimum component count.

Typical performance

Regulated Output Voltage	5V
Line Regulation (ΔV_i = 3V)	0.5mV
Load Regulation (ΔI_o = 50mA)	1.5mV

Basic high voltage regulator (V_o = 7 to 37V)

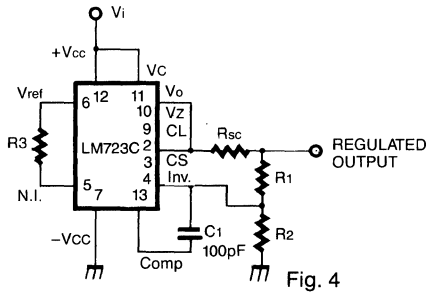


Fig. 4

Note: R1•R2/(R1+R2)for minimum temperature drift.
R3 may be eliminated for minimum component count.

Typical performance

Regulated Output Voltage	15V
Line Regulation (ΔV_i = 3V)	1.5mV
Load Regulation (ΔI_o = 50mA)	4.5mV

Negative voltage regulator

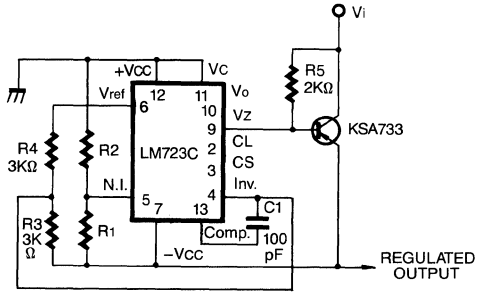


Fig. 5

Positive voltage regulator
(Extenal NPN Pass Transistor)

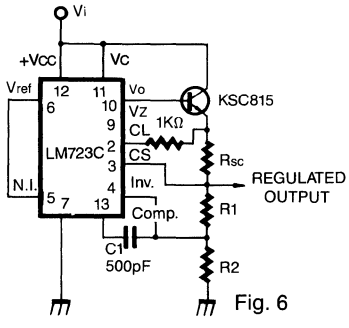


Fig. 6

Typical performance

Regulated output Voltage	-15V
Line Regulation (ΔV_i = 3V)	1mV
Load Regulation (ΔI_o = 100mA)	2mV

Typical performance

Regulated Output Voltage	+15V
Line Regulation (ΔV_i = 3V)	1.5mV
Load Regulation (ΔI_o = 1A)	15mV

Maximum output current vs. voltage drop

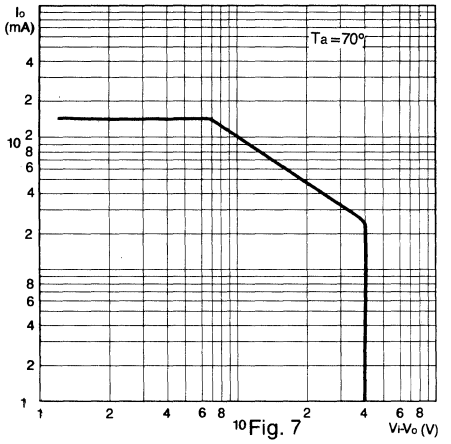


Fig. 7

Current limiting characteristics

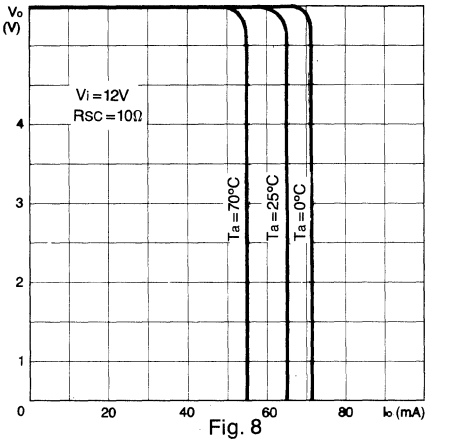


Fig. 8

Current limiting characteristics vs. junction temperature

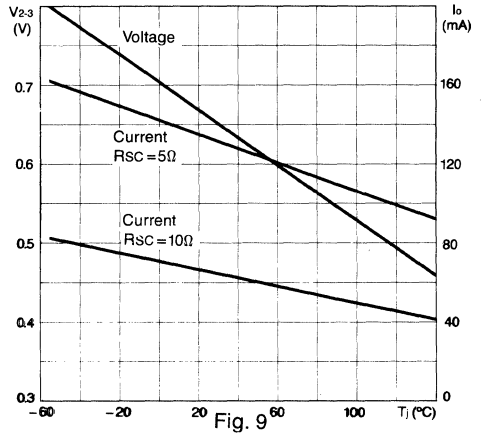


Fig. 9

Load regulation characteristics without current limiting

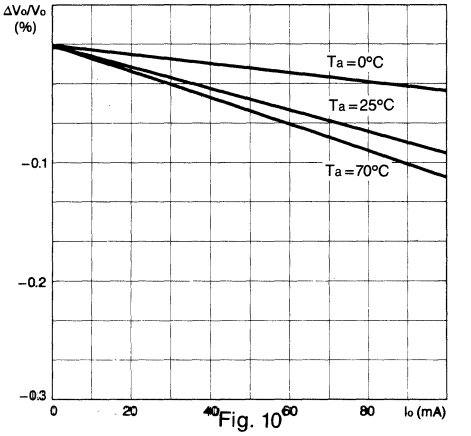


Fig. 10

Load regulation characteristics with current limiting

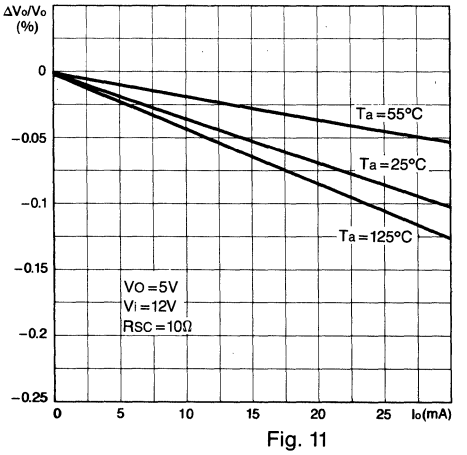


Fig. 11

Load regulation characteristic with current limiting

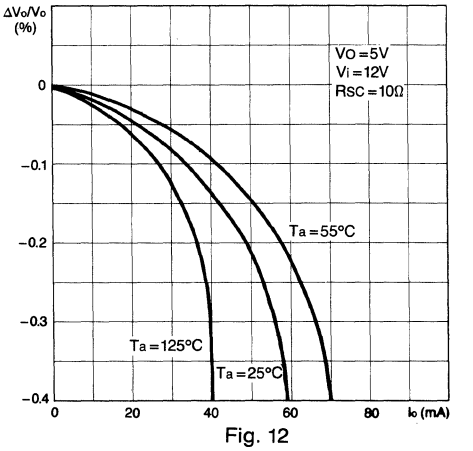


Fig. 12

Line regulation — voltage drop

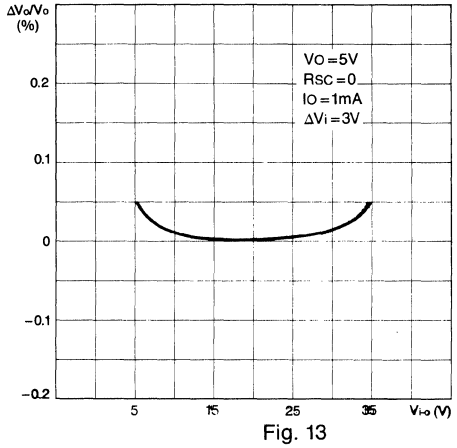


Fig. 13

Load regulation — voltage drop

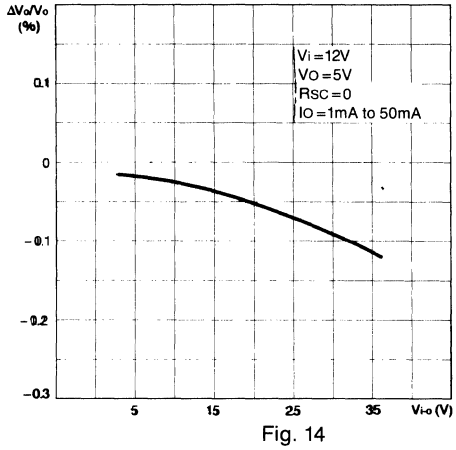


Fig. 14

Quiescent drain current vs. input voltage

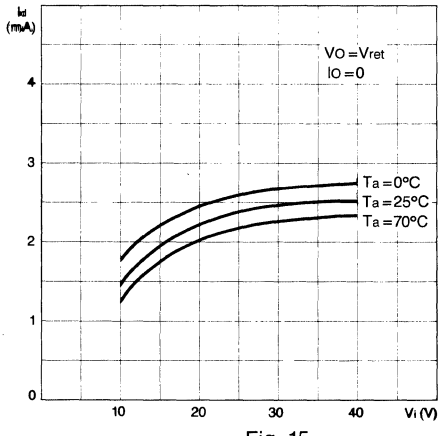


Fig. 15

Line transient response

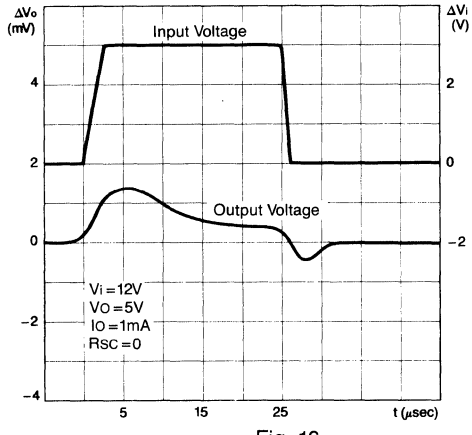


Fig. 16

Load transient response

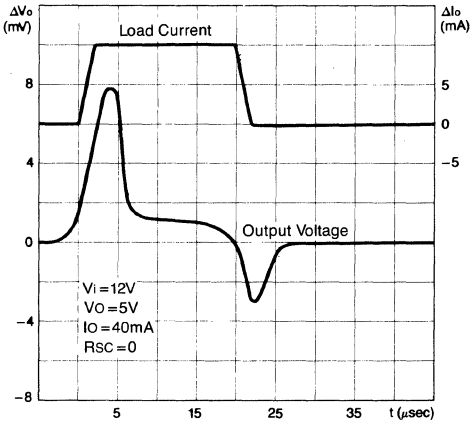


Fig. 17

Output impedance vs. frequency

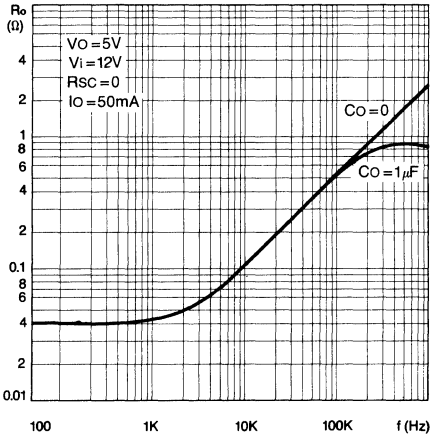
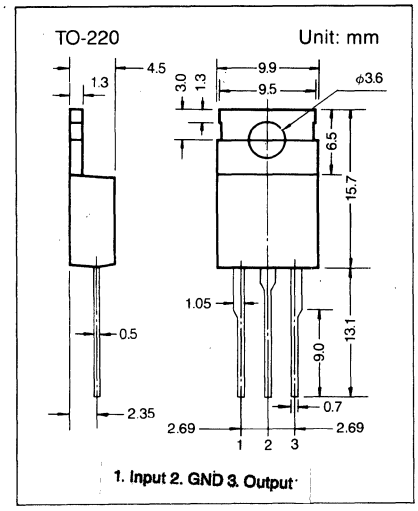


Fig. 18

3-TERMINAL 1A POSITIVE VOLTAGE REGULATOR

The MC78XXC series of three-terminal positive regulators is available in TO-220 package and with several fixed output voltages, making it useful in a wide range of applications. These Regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



FEATURES

- **Output Current up to 1.5A**
- **Output Voltages of 5; 6; 8; 12; 15; 18; 20; 24V**
- **Thermal Overload Protection**
- **Short circuit protection**
- **Output Transistor SOA Protection**

SCHEMATIC DIAGRAM

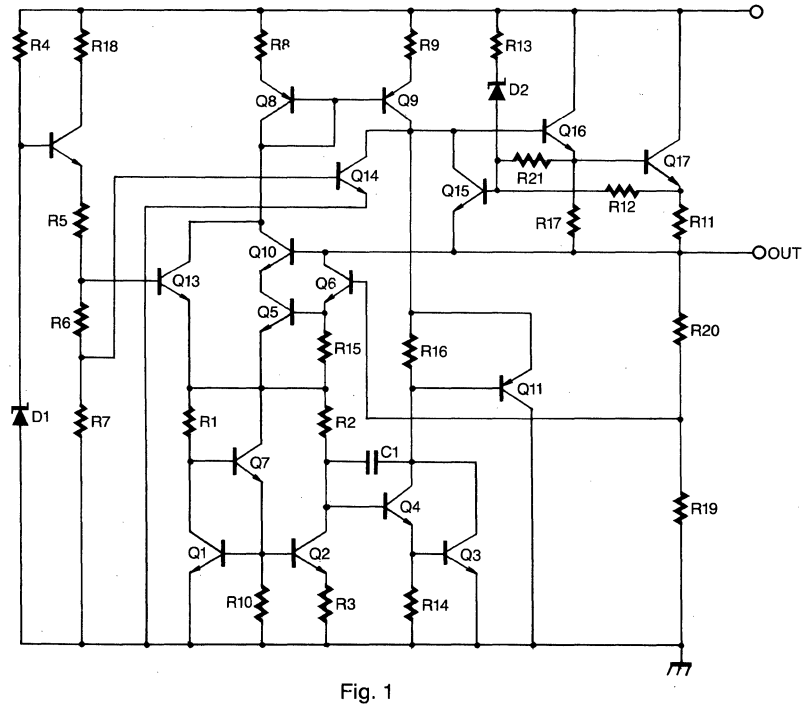


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (for V_o=5 to 18V)	V_i	35	V
(for V_o=20, 24V)	V_i	40	V
Thermal Resistance Junciton-Case	Q_{j-c}	5	°C/W
Thermal Resistance Junction-Air	Q_{j-c}	65	°C/W
Operating Temperature	T_{opr}	0 ~ +150	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

C8

BLOCK DIAGRAM

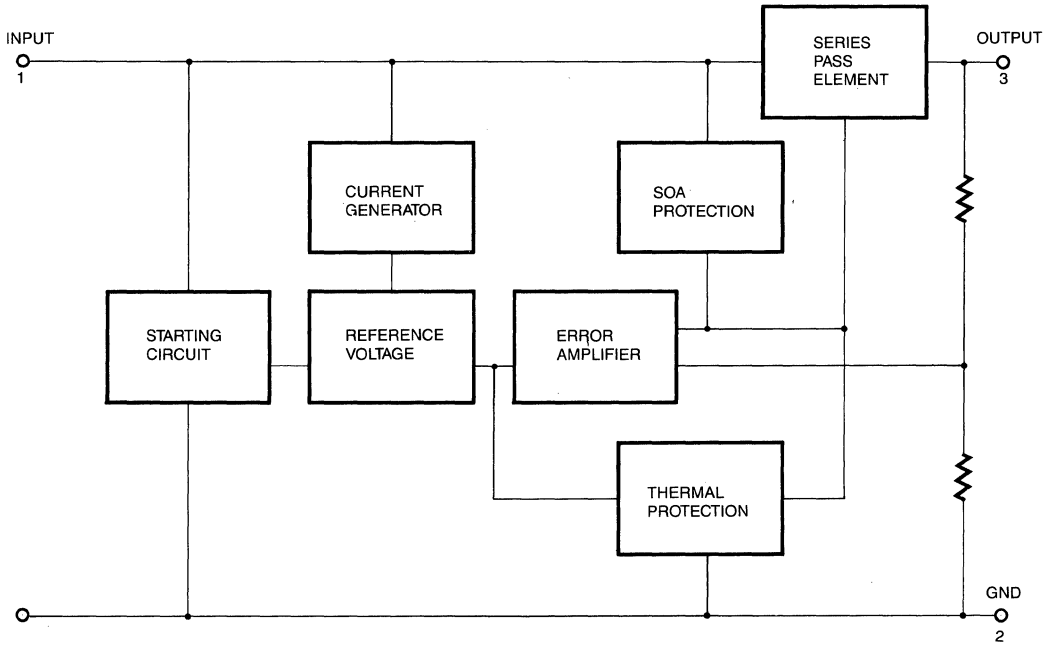


Fig. 2

ELECTRICAL CHARACTERISTICS MC7805C

(Refer to the test circuits, T_j=0 to 125°C, I_o=500mA, V_i=10V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	4.8	5	5.2	V
		I_o=5mA to 1A, P_o<15W, V_i=8 to 20V	4.75	5	5.35	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=7 to 25V		3	50	mV
		T_j=25°C, V_i=8 to 12V		1	25	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			100	mV
		T_j=25°C, I_o=250 to 750mA			25	
Quiescent Current	I_d	T_j=25°C			6	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=8 to 25V			1.3	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		-1.1		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		40		μV
Supply Voltage Rejection	SVR	f=120Hz, V_i=8 to 18V	62			dB
Dropout Voltage	V_d	T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		17		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_j=25°C		750		mA
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

ELECTRICAL CHARACTERISTICS MC7806C

(Refer to the test circuits, T_j=0 to 125°C, I_o=500mA, V_i=11V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_o	T_j=25°C	5.75	6	6.25	V
		I_o=5mA to 1A, $P_o \leq$ 15W, V_i=8 to 21V	5.7	6	6.3	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=8 to 25V			120	mV
		T_j=25°C, V_i=9 to 13V			60	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			120	mV
		T_j=25°C, I_o=250 to 750mA			60	
Quiescent Current	I_d	T_j=25°C			8	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=8 to 25V			1.3	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		−0.8		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		45		μV
Supply Voltage Rejection	SVR	f=120Hz, V_i=9 to 19V	59			dB
Dropout Voltage	V_d	I_o=1A		2		V
Output Resistance	R_o	f=1KHz		19		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_j=25°C		550		mA
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

ELECTRICAL CHARACTERISTICS MC7808C

(Refer to the test circuits, T_j=0 to 125°C, I_o=500mA, V_i=14V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_o	T_j=25°C	7.7	8	8.3	V
		I_o=5mA to 1A, P_o<15W, V_i=5 to 25V	7.6	8	8.4	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=10.5 to 25V			160	mV
		T_j=25°C, V_i=11 to 17V			80	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			160	mV
		T_j=25°C, I_o=250 to 750mA			80	
Quiescent Current	I_d	T_j=25°C			8	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=10.5 to 25V			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		-0.8		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		52		μV
Supply Voltage Rejection	SVR	f=120Hz, V_i=11.5 to 21.5V	56			dB
Dropout Voltage	V_d	I_o=1A		2		V
Output Resistance	R_o	f=1KHz		16		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_j=25°C		450		mA
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

ELECTRICAL CHARACTERISTICS MC7812C

(Refer to the test circuits, T_j=0 to 125°C, I_o=500mA, V_i=14V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Output Voltage	V_o	T_j=25°C		11.5	12	12.5	V
		I_o=5mA to 1A P_o<15W V_i=14.5 to 27V		11.4	12	12.6	
Line Regulation	$\triangle V_o$	T_j=25°C	V_i=14.5 to 30V			240	mV
			V_i=16 to 22V			120	
Load Regulation	$\triangle V_o$	T_j=25°C I_o=5mA to 1.5A				240	mV
		T_j=25°C I_o=250 to 750mA				120	
Quiescent Current	I_d	T_j=25°C				8	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A				0.5	mA
		V_i=14.5 to 30V				1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA			−1		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz T_j=25°C			75		μV
Supply Voltage Rejection	SVR	f=120Hz V_i=15 to 25V		65			dB
Dropout Voltage	V_d	I_o=1A			2		V
Output Resistance	R_o	f=1KHz		55	18		mΩ
Short Circuit Current	I_{sc}	V_i=35V T_j=25°C			350		mA
Short Circuit Peak Current	I_{scp}	T_j=25°C			2.2		A

ELECTRICAL CHARACTERISTICS MC7815C

(Refer to the test circuits, T_j=0 to 125°C, I_o=500mA, V_i=23V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_o	T_j=25°C	14.4	15	15.6	V
		I_o=5mA to 1A P_o<15W, V_i=17.5 to 30V	14.25	15	15.75	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=17.5 to 30V			300	mV
		T_j=25°C, V_i=20 to 26V			150	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			300	mV
		T_j=25°C, I_o=250 to 750mA			150	
Quiescent Current	I_d	T_j=25°C			8	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=17.5 to 30V			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		-1		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		90		μV
Supply Voltage Rejection	SVR	f=120Hz	54			dB
Dropout Voltage	V_d	I_o=1A		2		V
Output Resistance	R_o	f=1KHz		19		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_j=25°C		230		mA
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.1		A

ELECTRICAL CHARACTERISTICS MC7818C

(Refer to the test circuits, T_j=0 to 125°C, I_o=500mA, V_i=26V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_o	T_j=25°C	17.3	18	18.7	V
		I_o=5mA to 1A P_o<15W, V_i=21 to 33V	17.1	18	18.9	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=21 to 33V			360	mV
		T_j=25°C, V_i=24 to 30V			180	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			360	mV
		T_j=25°C, I_o=250 to 750mA			180	
Quiescent Current	I_d	T_j=25°C			8	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=21 to 33V			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		−1		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		110		μV
Supply Voltage Rejection	SVR	f=120Hz	53			dB
Dropout Voltage	V_d	I_o=1A		2		V
Output Resistance	R_o	f=1KHz		22		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_j=25°C		200		mA
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.1		A

ELECTRICAL CHARACTERISTICS MC7820C

(Refer to the test circuits, T_j=0 to 125°C, I_o=500mA, V_i=28V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_o	T_j=25°C	19.2	20	20.8	V
		I_o=5mA to 1A|P_o<15W, V_i=23 to 35V	19	20	21	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=22.5 to 35V			400	mV
		T_j=25°C, V_i=26 to 32V			200	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			400	mV
		T_j=25°C, I_o=250 to 750mA			200	
Quiescent Current	I_d	T_j=25°C			8	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=23 to 35V			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		-1		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		150		μV
Supply Voltage Rejection	SVR	f=120Hz	52			dB
Dropout Voltage	V_d	I_o=1A		2		V
Output Resistance	R_o	f=1KHz		24		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_j=25°C		180		mA
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.1		A

ELECTRICAL CHARACTERISTICS MC7824C

(Refer to the test circuits, T_j=0 to 125°C, I_o=500mA, V_i=33V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_o	T_j=25°C	23	24	25	V
		I_o=5mA to 1A P_o<15W, V_i=27 to 38V	22.8	24	25.2	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=27 to 38V			480	mV
		T_j=25°C, V_i=30 to 36V			240	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			480	mV
		T_j=25°C, I_o=250 to 750mA			240	
Quiescent Current	I_d	T_j=25°C			8	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=27 to 38V			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		-1.5		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		170		μV
Supply Voltage Rejection	SVR	f=120Hz	50			dB
Dropout Voltage	V_d	I_o=1A		2		V
Output Resistance	R_o	f=1KHz		28		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_j=25°C		150		mA
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.1		A

ELECTRICAL CHARACTERISTICS MC7805AC

(Refer to the test circuits, T_j=0 to 125°C, I_o=1A, V_i=10V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	4.9	5	5.1	V
		I_o=5mA to 1A, $P_o \leq$15W V_i=7.5 to 20V	4.8	5	5.2	
*Line Regulation	ΔV_o	V_i=7.5 to 25V, I_o=500mA		7	50	mV
		V_i=8 to 12V		10	50	
		T_j=25°C, V_i=7.3 to 25V		7	50	
		T_j=25°C, V_i=8 to 12V		2	25	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A		25	100	mV
		I_o=5mA to 1A		25	100	
		I_o=250 to 750mA		8	50	
Quiescent Current	I_d	T_j=25°C		4.3	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=8 to 25V, I_o=500mA			0.8	
		V_i=7.5 to 20V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$			−1.1		mV/°C
Output Noise Voltage	^eN	f=10Hz to 100KHz T_a=25°C		10		μV V_o
Supply Voltage Rejection	SVR	f=120Hz, I_o=500mA V_i=8 to 18V		68		dB
Dropout Voltage	V_d	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		17		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		0.2		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7806AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=11V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C		5.88	6	6.12	V
		I_o=5mA to 1A, $P_o \leq$15W V_i=8.6 to 21V		5.76	6	6.24	
*Line Regulation	ΔV_o	V_i=8.6 to 25V, I_o=500mA			9	60	mV
		V_i=9 to 13V			11	60	
		T_j=25°C	V_i=8.3 to 21V		9	60	
			V_i=9 to 13V		3	30	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A			43	100	mV
		I_o=5mA to 1A			43	100	
		I_o=250 to 750mA			16	50	
Quiescent Current	I_d	T_j=25°C			4.3	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A				0.5	mA
		V_i=9 to 25V, I_o=500mA				0.8	
		V_i=8.6 to 21V, T_j=25°C				0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$				−0.8		mV/°C
Output Noise Voltage	^eN	f=10Hz to 100KHz T_a=25°C			10		μV V_o
Supply Voltage Rejection	SVR	f=120Hz, I_o=500mA V_i=9 to 19V			65		dB
Dropout Voltage	V_d	I_o=1A, T_j=25°C			2		V
Output Resistance	R_o	f=1KHz			17		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C			0.2		A
Short Circuit Peak Current	I_{scp}	T_j=25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7808AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=14V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	7.84	8	0.16	V
		I_o=5mA to 1A, $P_o \leq$ 15W V_i=10.6 to 23V	7.7	8	8.3	
*Line Regulation	ΔV_o	V_i=10.6 to 25V, I_o=50mA		12	80	mV
		V_i=11 to 17V		15	80	
		T_j=25°C, V_i=10.4 to 23V		12	80	
		T_j=25°C, V_i=11 to 17V		5	40	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A		45	100	mV
		I_o=5mA to 1A		45	100	
		I_o=250 to 750mA		16	50	
Quiescent Current	I_d	T_j=25°C		4.3	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=11 to 25V, I_o=500mA			0.8	
		V_i=10.6 to 23V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$			-0.8		mV/°C
Output Noise Voltage	^eN	f=10Hz to 100KHz T_a=25°C		10		$\frac{\mu V}{V_o}$
Supply Voltage Rejection	SVR	f=120Hz, I_o=500mA V_i=11.5 to 21.5V		62		dB
Dropout Voltage	V_d	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		18		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		0.2		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7812AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=19V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	11.75	12	12.25	V
		I_o=5mA to 1A, $P_o \leq$15W, V_i=14.8 to 27V	11.5	12	12.5	
*Line Regulation	ΔV_o	V_i=14.8 to 30V, I_o=50mA		13	120	mV
		V_i=16 to 22V		16	120	
		T_j=25°C, V_i=14.5 to 27V		13	120	
		T_j=25°C, V_i=16 to 22V		6	60	
*Load Regulation	ΔV_o	T_j=25°C, I_o=5mA to 1.5A		46	100	mV
		I_o=5mA to 1A		46	100	
		I_o=250 to 750mA		17	50	
Quiescent Current	I_d	T_j=25°C		4.4	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=15 to 30V, I_o=500mA			0.8	
		V_i=14.8 to 27V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$			−1		mV/°C
Output Noise Voltage	^eN	f=10Hz to 100KHz, T_a=25°C		10		$\frac{\mu V}{V_o}$
Supply Voltage Rejection	SVR	f=120Hz, I_o=500mA, V_i=15 to 25V		60		dB
Dropout Voltage	V_d	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		18		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		0.2		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7815AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=23V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	14.7	15	15.3	V
		I_o=5mA to 1A, $P_o \leq$ 15W V_i=17.7 to 30V	14.4	15	15.6	
*Line Regulation	ΔV_o	V_i=17.9 to 30V, I_o=500mA		13	150	mV
		V_i=20 to 26V		16	150	
		T_j=25°C, V_i=17.5 to 30V		13	150	
		T_j=25°C, V_i=20 to 26V		6	75	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A		52	100	mV
		I_o=5mA to 1A		52	100	
		I_o=250 to 750mA		20	50	
Quiescent Current	I_d	T_j=25°C		4.4	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=17.5 to 30V, I_o=500mA			0.8	
		V_i=17.5 to 30V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$			−1		mV/°C
Output Noise Voltage	^eN	f=10Hz to 100KHz T_a=25°C		10		$\frac{\mu V}{V_o}$
Supply Voltage Rejection	SVR	f=120Hz, I_o=500mA V_i=18.5 to 28.5V		58		dB
Dropout Voltage	V_d	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		19		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		0.2		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7818AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=27V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	17.64	18	18.36	V
		I_o=5mA to 1A, $P_o \leq$15W V_i=21 to 33V	17.3	18	18.7	
*Line Regulation	ΔV_o	V_i=21 to 33V, I_o=500mA		25	180	mV
		V_i=24 to 30V		28	180	
		T_j=25°C, V_i=20.6 to 33V		25	180	
		T_j=25°C, V_i=24 to 30V		10	90	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A		55	100	mV
		I_o=5mA to 1A		55	100	
		I_o=250 to 750mA		22	50	
Quiescent Current	I_d	T_j=25°C		4.5	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=21 to 33V, I_o=500mA			0.8	
		V_i=21 to 33V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$			−1		mV/°C
Output Noise Voltage	^eN	f=10Hz to 100KHz T_a=25°C		10		$\frac{\mu V}{V_o}$
Supply Voltage Rejection	SVR	f=120Hz, I_o=500mA V_i=22 to 32V		57		dB
Dropout Voltage	V_d	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		19		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		0.2		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7824AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=33V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	23.5	24	24.5	V
		I_o=5mA to 1A, $P_o \leq$15W V_i=27.3 to 38V	23	24	25	
*Line Regulation	ΔV_o	V_i=27 to 33V, I_o=500mA		31	240	mV
		V_i=30 to 36V		35	240	
		T_j=25°C, V_i=26.7 to 38V		31	240	
		T_j=25°C, V_i=30 to 36V		14	120	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A		60	100	mV
		I_o=5mA to 1A		60	100	
		I_o=250 to 750mA		25	50	
Quiescent Current	I_d	T_j=25°C		4.6	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=27.3 to 38V, I_o=500mA			0.8	
		V_i=27.3 to 38V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$			−1.5		mV/°C
Output Noise Voltage	^eN	f=10Hz to 100KHz T_a=25°C		10		$\frac{\mu V}{V_o}$
Supply Voltage Rejection	SVR	f=120Hz, I_o=500mA V_i=28 to 38V		54		dB
Dropout Voltage	V_d	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		20		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		0.2		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TEST CIRCUIT

DC parameters

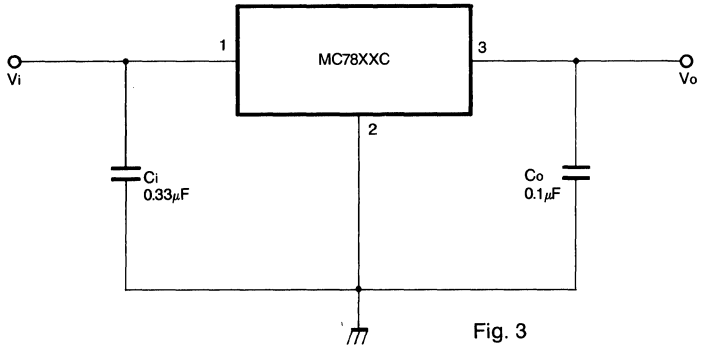


Fig. 3

Lord regulation

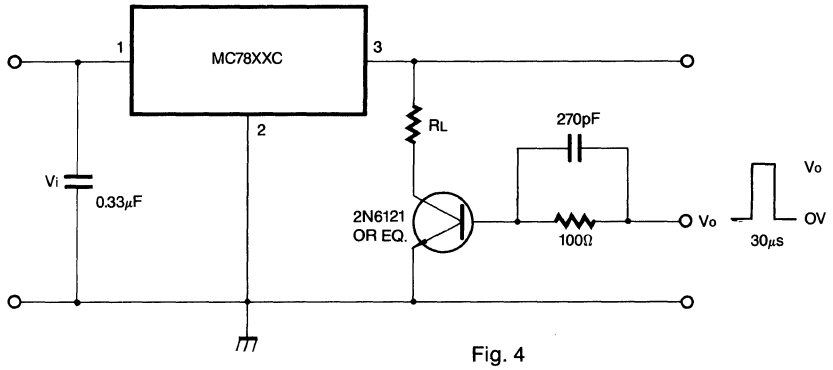


Fig. 4

Ripple rejection

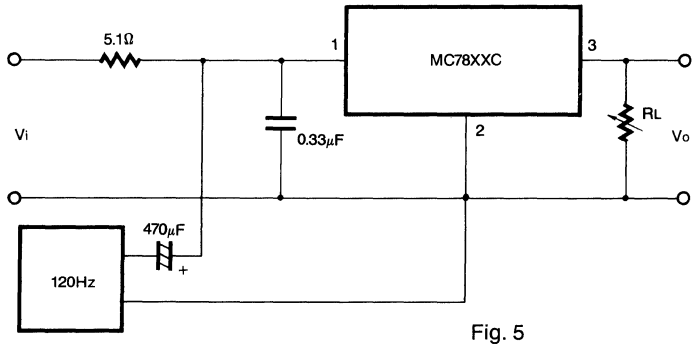


Fig. 5

APPLICATION CIRCUIT

Fixed output regulator

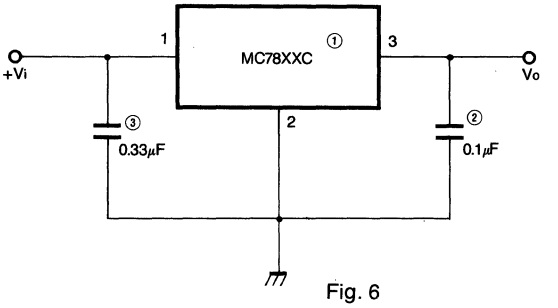


Fig. 6

Constant current regulator

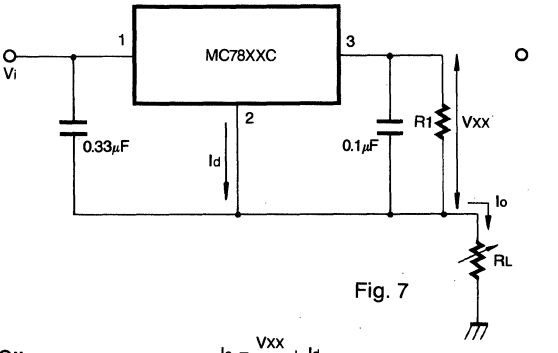


Fig. 7

$$I_O = \frac{V_{XX}}{R_1} + I_d$$

Notes:
(1) To specify an output voltage, substitute voltage value for "XXC."
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Circuit for increasing output voltage

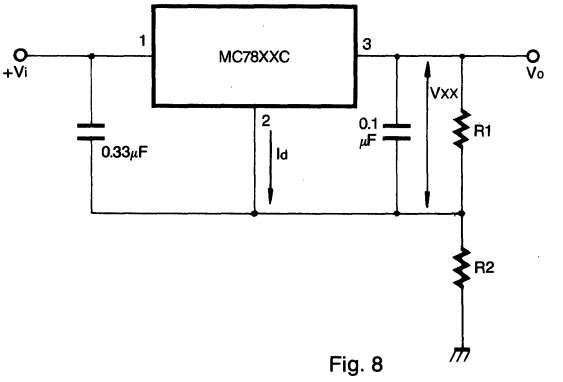


Fig. 8

Adjustable output regulator (7 to 30V)

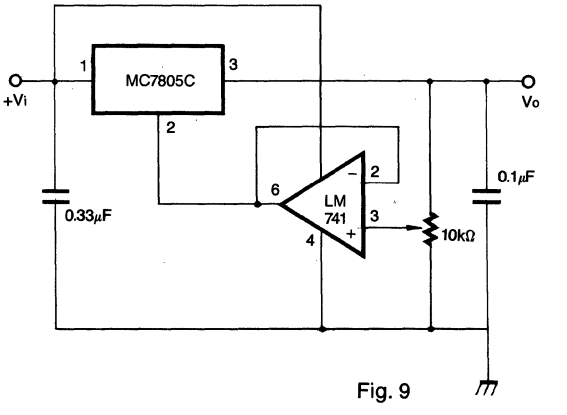


Fig. 9

$I_{R1} \geqslant 5I_d$
$V_O = V_{XX}(1+R_2/R_1)+I_d R_2$

APPLICATION CIRCUIT (continued)

0.5 to 10V regulator

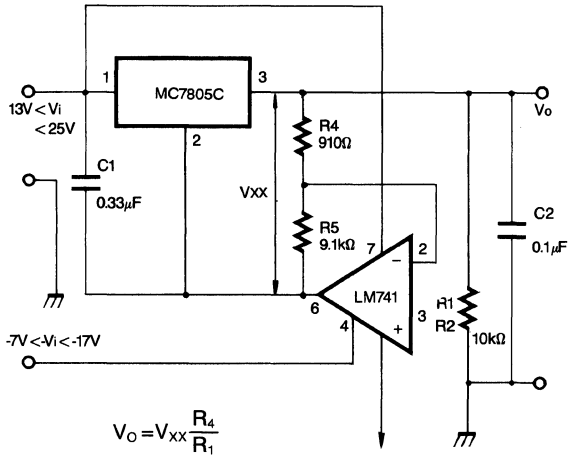


Fig. 10

High current voltage regulator

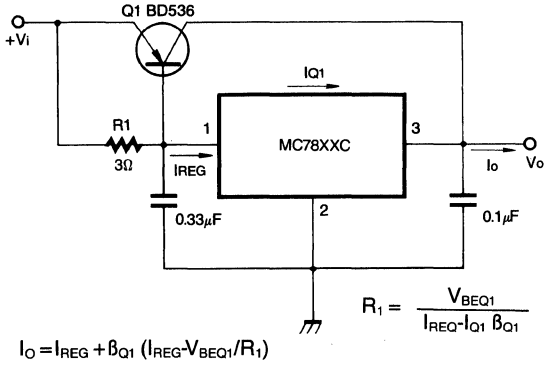


Fig. 11

High output current with short circuit protection

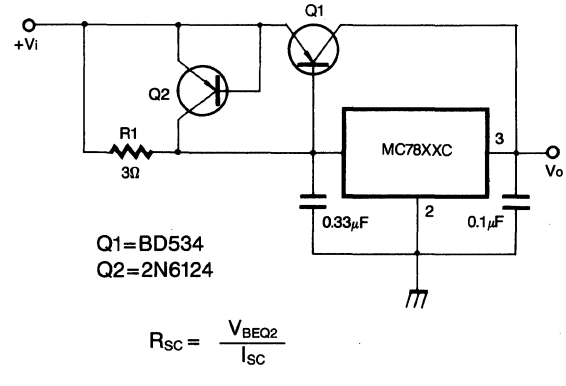


Fig. 12

Tracking voltage regulator

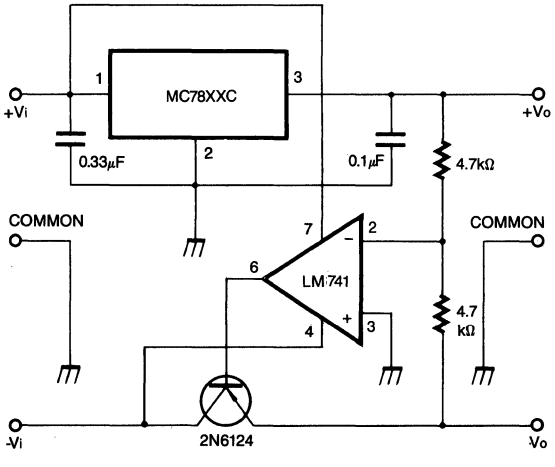


Fig. 13

APPLICATION CIRCUIT (continued)

Split power supply (± 15V — 1A)

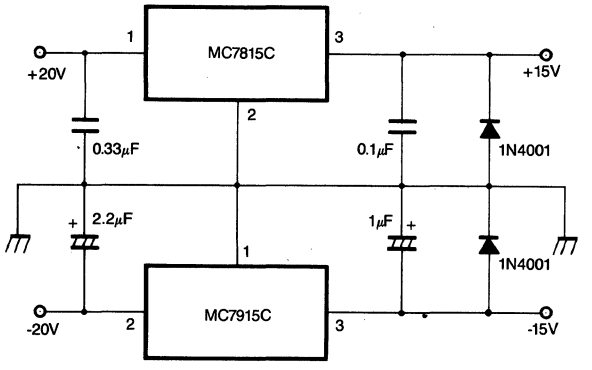


Fig. 14

Negative output voltage circuit

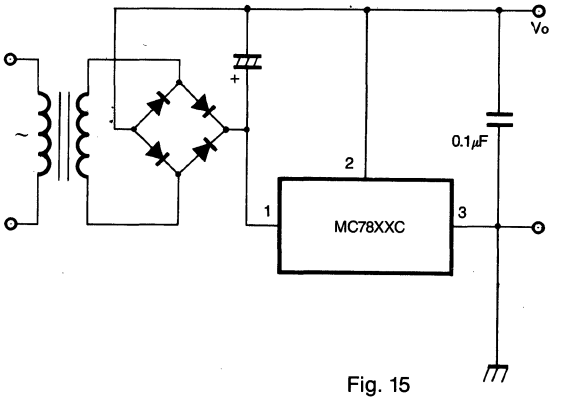


Fig. 15

Switching regulator

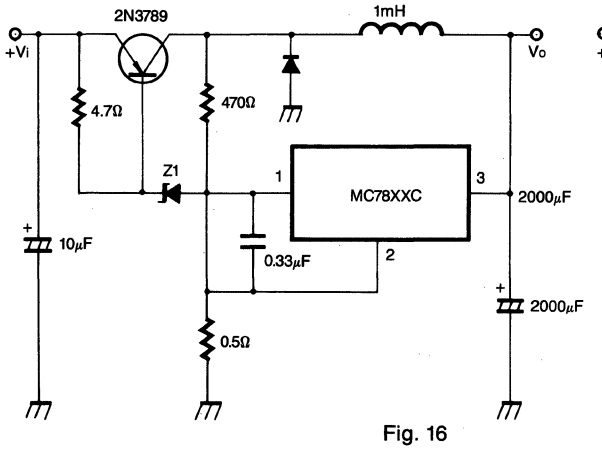
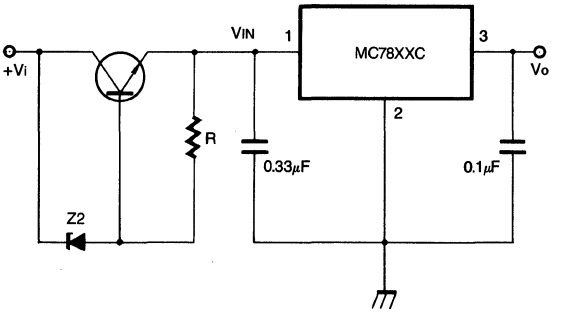


Fig. 16

High input voltage circuit



$V_{IN} = V_i - (V_Z + V_{BE})$

Fig. 17

APPLICATION CIRCUIT (continued)

High input voltage circuit

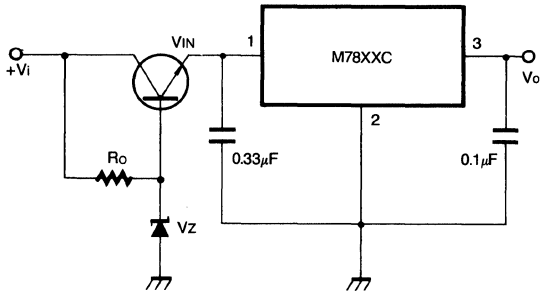


Fig. 18

$V_{IN} = V_Z - V_{BE}$

High output voltage regulator

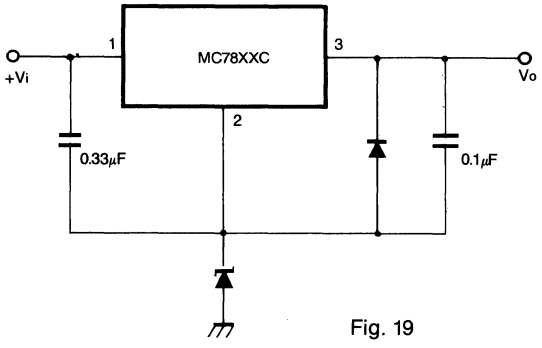
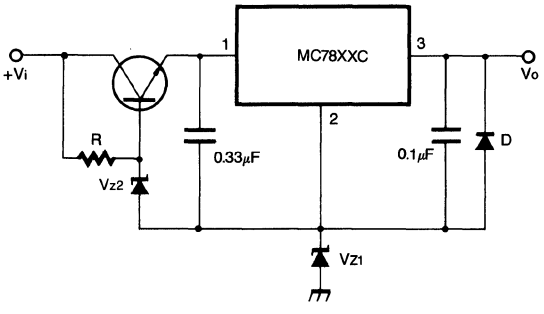


Fig. 19

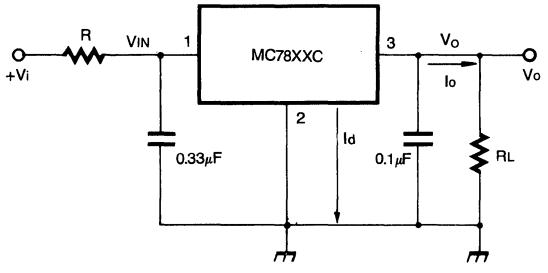
High input and output voltage



$V_O = V_{XX} + V_{Z1}$

Fig. 20

Reducing power dissipation with dropping resitor



$$R = \frac{V_{i\,(min)} - V_{XX} - V_{DROP\,(max)}}{I_{O\,(max)} + I_{O\,(max)}}$$

Fig. 21

APPLICATION CIRCUIT (continued)

Remote shuntdown

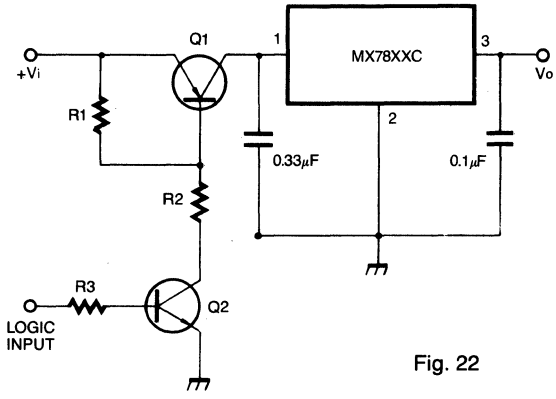


Fig. 22

Power AM modulator
(unity voltage gain, $I_O \leqslant 1A$)

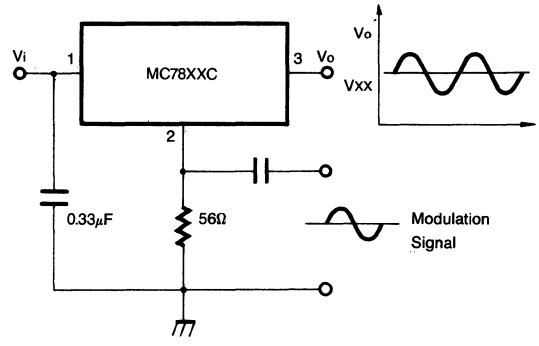


Fig. 23

Note: The circuit performs well up to 100 KHz.

Adjustable output voltage with temperature compensation

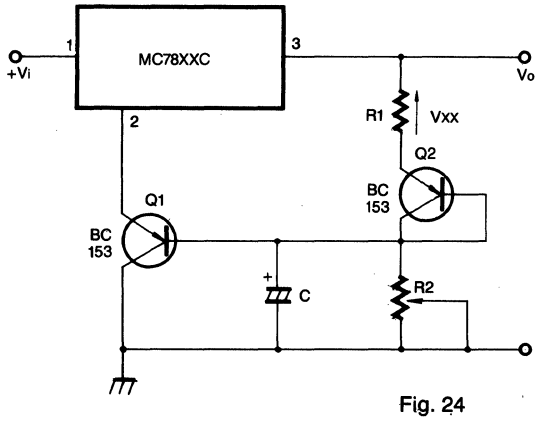


Fig. 24

Note: Q2 is connected as a diode in order to compensate the variation of the Q1 V_{BE} with the temperature. C allows a slow rise-time of the V_O

$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

APPLICATION CIRCUIT (continued)

Light controllers (V_O min=V_{XX} +V_{BE})

(a)

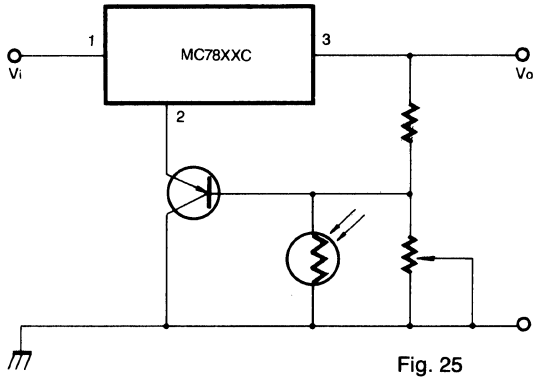
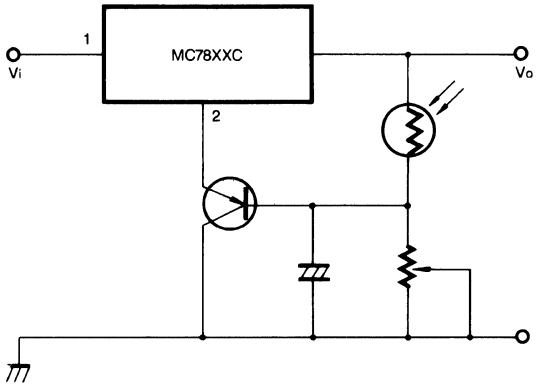


Fig. 25

V_O falls when the light goes up

(b)



V_O rises when the light goes up

Protection against input short-circuit with high capacitane loads

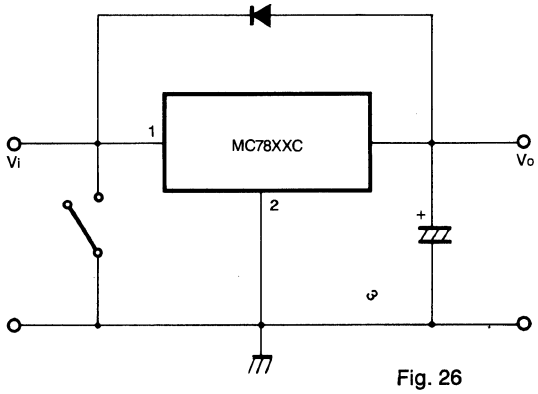
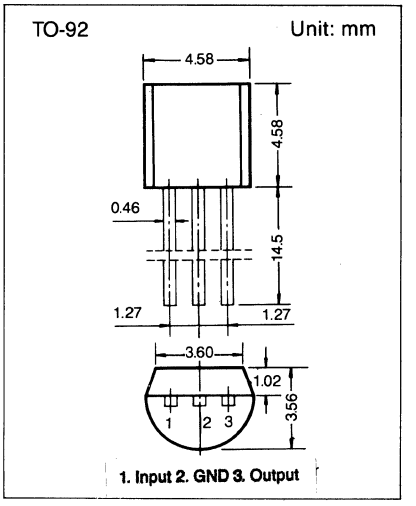


Fig. 26

Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 26) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the transistor may be destroyed. The external diode by-passes the current from the IC to ground.

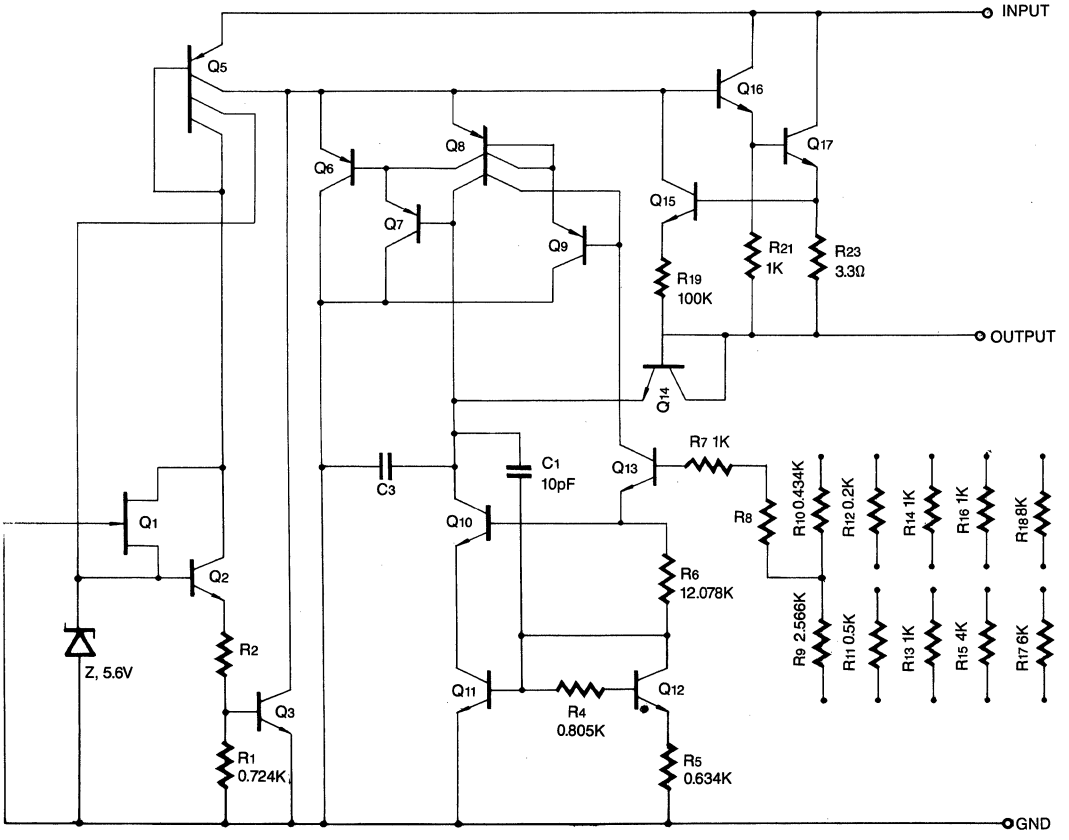
3-TERMINAL POSITIVE VOLTAGE REGULATORS

These regulators employ internal current-limiting and thermal-shutdown, making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 100mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high-current voltage regulators. The MC78LXXC used as a Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnitude, along with lower quiescent current and lower noise.



FEATURE

- **Output current up to 100mA.**
- **No external components.**
- **Internal thermal overload protection.**
- **Internal short circuit current limiting.**
- **Available in JEDEC TO-92.**
- **Output voltages of 5V, 6.2V, 8.2V, 9V, 12, 15V.**
- **Output voltage tolerances of ±5% over the temperature range.**



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage	V_I	35	V
Operating Junction Temperature Range	Topr	0 ~ +125	°C
Storage Temperature Range	Tstg	−65 ~ +150	°C

MC78L05AC (Note 2)
ELECTRICAL CHARACTERISTICS

V_{IN} =10V, I_{OUT} =40mA, 0°C≤Tj≤125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	Tj=25°C		4.8	5.0	5.2	V
Line Regulation		ΔV_O	Tj=25°C	7V≤V_{IN}≤20V		55	150	mV
				8V≤V_{IN}≤20V		45	100	mV
Load Regulation		ΔV_O	Tj=25°C	1mA≤I_{OUT}≤100mA		11	60	mV
				1mA≤I_{OUT}≤40mA		5.0	30	mV
Output Voltage		V_O	7V≤V_{IN}≤20V	1mA≤I_{OUT}≤40mA	4.75		5.25	V
			7V≤V_{IN}≤V_{max} (Note 3)	1mA≤I_{OUT}≤70mA	4.75		5.25	V
Quiescent Current		I_D				2.0	5.5	mA
Quiescent Current Change	with line	ΔI_D	8V≤V_{IN}≤20V				1.5	mA
	with load	ΔI_D	1mA≤I_{OUT}≤40mA				0.1	mA
Output Noise Voltage		^eN	T_a = 25°C, 10Hz≤f≤100kHz			40		μV
Temperature Coefficient of V_{OUT}		$\frac{V_O}{T}$	I_{OUT} =5mA			−0.65		mV/°C
Ripple Rejection		SVR	f = 120Hz, 8V≤V_{IN}≤18V, Tj = 25°C		41	49		dB
Dropout Voltage		V_D	Tj=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	Tj=25°C			140		mA

MC78L62AC ELECTRICAL CHARACTERISTICS

V_{IN} =12V, I_{OUT} =40mA, 0°C≤Tj≤125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	Tj=25°C		5.95	6.2	6.45	V
Line Regulation		ΔV_O	Tj=25°C	9V≤V_{IN}≤20V		65	175	mV
				9V≤V_{IN}≤20V		55	125	mV
Load Regulation		ΔV_O	Tj=25°C	1mA≤I_{OUT}≤100mA		13	80	mV
				1mA≤I_{OUT}≤40mA		6.0	40	mV
Output Voltage		V_O	8.5V≤V_{IN}≤20V	1mA≤I_{OUT}≤40mA	5.90		6.5	V
			8.5V≤V_{IN}≤V_{max} (Note 3)	1mA≤I_{OUT}≤70mA	5.90		6.5	V
Quiescent Current		I_D				2.0	5.5	mA
Quiescent Current Change	with line	ΔI_D	8V≤V_{IN}≤20V				1.5	mA
	with load	ΔI_D	1mA≤I_{OUT}≤40mA				0.1	mA
Output Noise Voltage		^eN	T_a=25°C, 10Hz≤f≤100kHz			50		μV
Temperature Coefficient of V_{OUT}		$\frac{V_O}{T}$	I_{OUT}=5mA			-0.75		mV/°C
Ripple Rejection		SVR	f=120Hz, 8V≤V_{IN}≤20V, Tj=25°C		40	46		dB
Dropout Voltage		V_D	Tj=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	Tj=25°C			140		mA

MC78L82AC ELECTRICAL CHARACTERISTICS

V_{IN} =14V, I_{OUT} =40mA, 0°C≤Tj≤125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	Tj=25°C		7.87	8.2	8.53	V
Line Regulation		ΔV_O	Tj=25°C	11V≤V_{IN}≤23V		80	175	mV
				12V≤V_{IN}≤23V		70	125	mV
Load Regulation		ΔV_O	Tj=25°C	1mA≤I_{OUT}≤100mA		15	80	mV
				1mA≤I_{OUT}≤40mA		8.0	40	mV
Output Voltage		V_O	11V≤V_{IN}≤23V	1mA≤I_{OUT}≤40mA	7.8		8.5	V
			11V≤V_{IN}≤V_{max} (Note 3)	1mA≤I_{OUT}≤70mA	7.8		8.6	V
Quiescent Current		I_D					1.5	mA
Quiescent Current Change	with line	ΔI_D	12V≤V_{IN}≤23V				1.5	mA
	with load	ΔI_D	1mA≤I_{OUT}≤40mA				0.1	mA
Output Noise Voltage		^eN	T_a=25°C, 10Hz≤f≤100kHz			60		μV
Temperature Coefficient of V_{OUT}		$\frac{V_O}{T}$	I_{OUT}=5mA			-0.8		mV/°C
Ripple Rejection		SVR	f=120Hz, 12V≤V_{IN}≤22V, Tj=25°C		39	45		dB
Dropout Voltage		V_D	Tj=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	Tj=25°C			140		mA

MC78L09AC ELECTRICAL CHARACTERISTICS

V_{IN}=15V, I_{OUT}=40mA, 0°C≤Tj≤125°C, C_{IN}=0.33μF, C_{OUT}=0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	Tj=25°C		8.64	9.0	9.36	V
Line Regulation		ΔV_O	Tj=25°C	11.5V≤V_{IN}≤24V		90	200	mV
				13V≤V_{IN}≤24V		100	150	mV
Load Regulation		ΔV_O	Tj=25°C	1mA≤I_{OUT}≤100mA		20	90	mV
				1mA≤I_{OUT}≤40mA		10	40	mV
Output Voltage		V_O	11.5V≤V_{IN}≤24V	1mA≤I_{OUT}≤40mA	8.55		9.45	V
			11.5V≤V_{IN}≤V_{max} (Note 3)	1mA≤I_{OUT}≤70mA	8.55		9.45	V
Quiescent Current		I_D				2.1	5.5	mA
Quiescent Current Change	with line	ΔI_D	11.5V≤V_{IN}≤24V				1.5	mA
	with load	ΔI_D	1mA≤I_{OUT}≤40mA				0.1	mA
Output Noise Voltage		^eN	T_a=25°C, 10Hz≤f≤100kHz			70		μV
Temperature Coefficient of V_{OUT}		$\frac{V_O}{T}$	I_{OUT}=5mA			−0.9		mV/°C
Ripple Rejection		SVR	f=120Hz, 15V≤V_{IN}≤25V, Tj=25°C		38	44		dB
Dropout Voltage		V_D	Tj=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	Tj=25°C			140		mA

MC78L12AC ELECTRICAL CHARACTERISTICS

V_{IN}=15V, I_{OUT}=40mA, 0°C≤Tj≤125°C, C_{IN}=0.33μF, C_{OUT}=0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	Tj=25°C		11.5	12	12.5	V
Line Regulation		ΔV_O	Tj=25°C	14.5V≤V_{IN}≤27V		120	250	mV
				16V≤V_{IN}≤27V		100	200	mV
Load Regulation		ΔV_O	Tj=25°C	1mA≤I_{OUT}≤100mA		20	100	mV
				1mA≤I_{OUT}≤40mA		10	50	mV
Output Voltage		V_O	14.5V≤V_{IN}≤27V	1mA≤I_{OUT}≤40mA		10	50	V
			14.5V≤V_{IN}≤V_{max} (Note 3)	1mA≤I_{OUT}≤70mA	11.4		12.6	V
Quiescent Current		I_D				2.1	5.5	mA
Quiescent Current Change	with line	ΔI_D	16V≤V_{IN}≤27V				1.5	mA
	with load	ΔI_D	1mA≤I_{OUT}≤40mA				0.1	mA
Output Noise Voltage		^eN	T_a=25°C, 10Hz≤f≤100kHz			80		μV
Temperature Coefficient of V_{OUT}		$\frac{V_O}{T}$	I_{OUT}=5mA			−1.0		mV/°C
Ripple Rejection		SVR	f=120Hz, 15V≤V_{IN}≤25V, Tj=25°C		37	42		dB
Dropout Voltage		V_D	Tj=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	Tj=25°C			140		mA

MC78L15AC
ELECTRICAL CHARACTERISTICS

V_{IN} =23V, I_{OUT} =40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

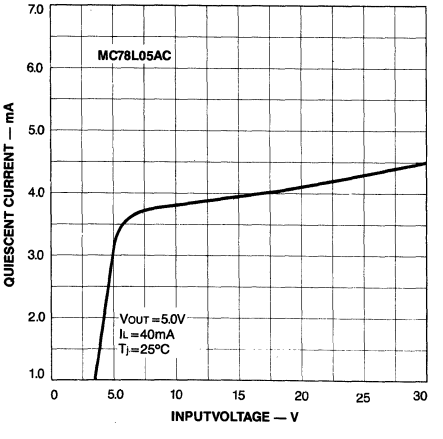
Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	Tj=25°C		14.4	15	15.6	V
Line Regulation		ΔV_O	Tj=25°C	17.5V ≤ V_{IN} ≤ 30V		130	300	mV
				20V ≤ V_{IN} ≤ 30V		110	250	mV
Load Regulation		ΔV_O	Tj=25°C	1mA ≤ I_{OUT} ≤ 100mA		25	150	mV
				1mA ≤ I_{OUT} ≤ 40mA		12	75	mV
Output Voltage		V_O	17.5V ≤ V_{IN} ≤ 30V	1mA ≤ I_{OUT} ≤ 40mA	14.25		15.75	V
			17.5V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	14.25		15.75	V
Quiescent Current		I_D				2.2	5.5	mA
Quiescent Current Change	with line	ΔI_D	20V ≤ V_{IN} ≤ 30V				1.5	mA
	with load	ΔI_D	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		^eN	T_a = 25°C, 10Hz ≤ f ≤ 100kHz			90		μV
Temperature Coefficient of V_{OUT}		$\frac{V_O}{T}$	I_{OUT} =5mA			-1.3		mV/°C
Ripple Rejection		SVR	f = 120Hz, 18.5V ≤ V_{IN} ≤ 28.5V, Tj = 25°C		34	39		dB
Dropout Voltage		V_D	Tj=25°C			1.7		dB
Peak Output/Short-Circuit Current		I_{SC}	Tj=25°C			140		mA

Notes

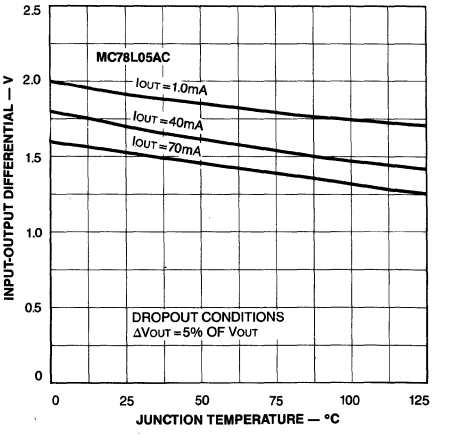
1. The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The date above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.
2. Power dissipation ≤ 75W.

TYPICAL PERFORMANCE CURVES

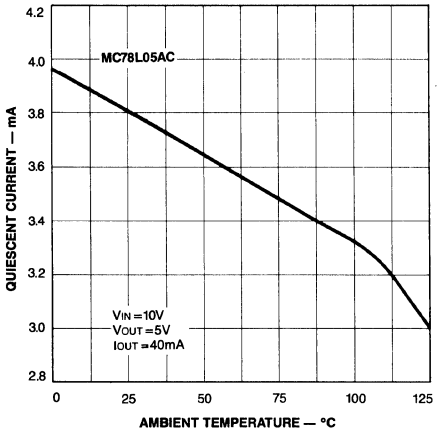
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



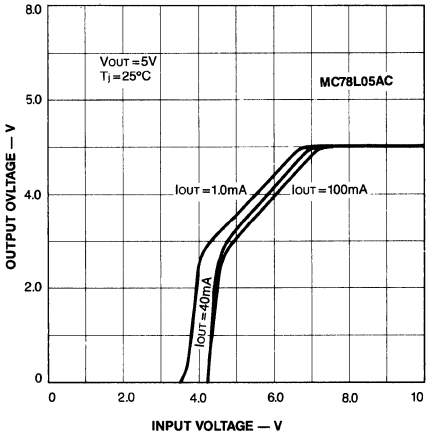
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



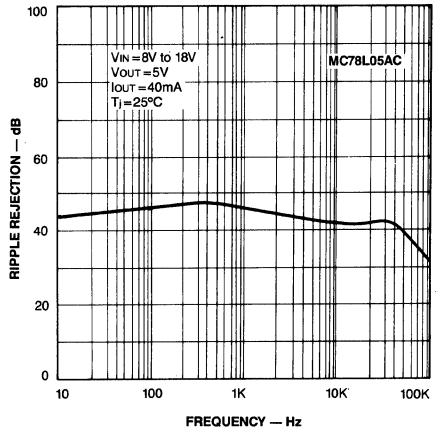
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



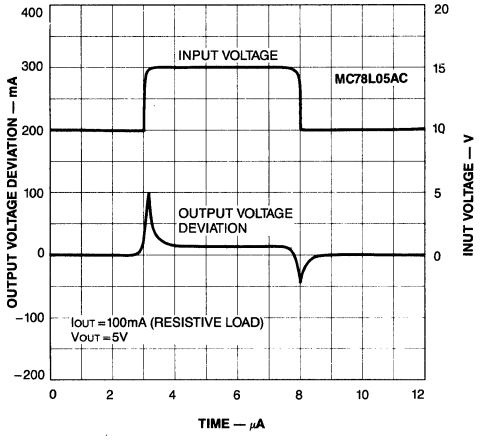
DROPOUT CHARACTERISTICS



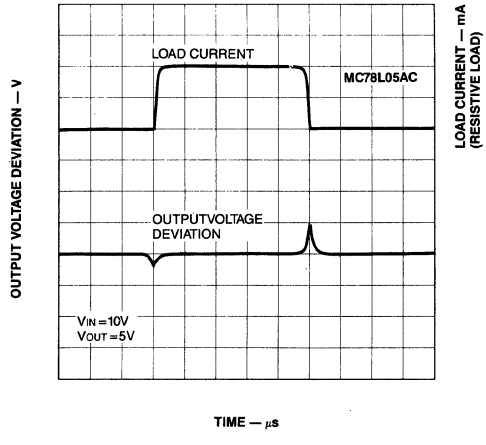
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



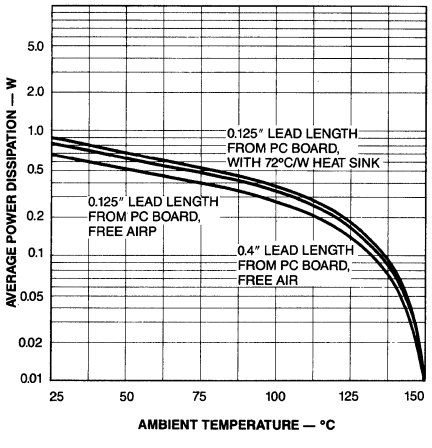
LINE TRANSIENT RESPONSE



LOAD-TRANSIENT RESPONSE



TO-92 WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



Design Considerations

The MC78L series regulators have thermal overload protection from excessive power, internal short-circuit protection which limits each circuit's maximum current, and output transistor safe-area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (125°C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Thermal Considerations

The TO-92 molded package manufactured by SST is capable of unusually high power dissipation due to the lead frame design. However, its thermal capabilities are generally overlooked because of a lack of understanding of the thermal paths from the semiconductor junction to ambient temperature. While thermal resistance is normally specified for the device mounted 1cm above an infinite heat sink, very little has been mentioned of the options available to improve on the conservatively rated thermal capability.

An explanation of the thermal paths of the TO-92 will allow the designer to determine the thermal stress he is applying in any given application.

The TO-92 Package

The TO-92 package thermal paths are complex. In addition to the path through the molding compound to ambient temperature, there is another path through the pins, in parallel with the case path, to ambient temperature, as shown in Figure 1.

The total thermal resistance in this model is then:

$$\theta_{JA} = \frac{(\theta_{JC} + \theta_{CA})(\theta_{JL} + \theta_{LA})}{\theta_{JC} + \theta_{CA} + \theta_{JL} + \theta_{LA}}$$

Where: θ_{JC} = thermal resistance of the case between the regulator die and a point on the case directly above the die location.
θ_{CA} = thermal resistance between the case and air at ambient temperature.
θ_{JL} = thermal resistance from transistor die through the collector lead to a point 1/16 inch below the regulator case.
θ_{LA} = total thermal resistance of the collector-base-emitter pins to ambient temperature.
θ_{JA} = junction to ambient thermal resistance.

TO-92 THERMAL EQUIVALENT CIRCUIT

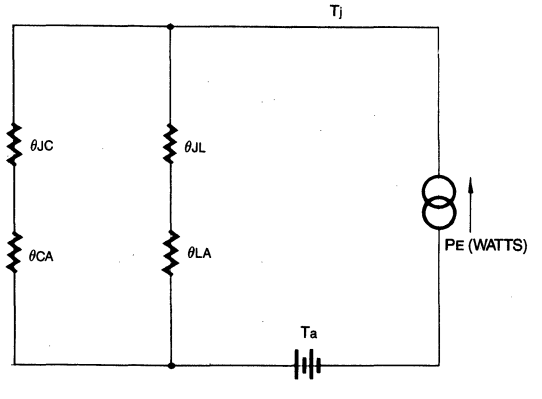


Fig. 1

TO-92 THERMAL EQUIVALENT CIRCUIT (PIN AT OTHER THAN AMBIENT TEMPERATURE)

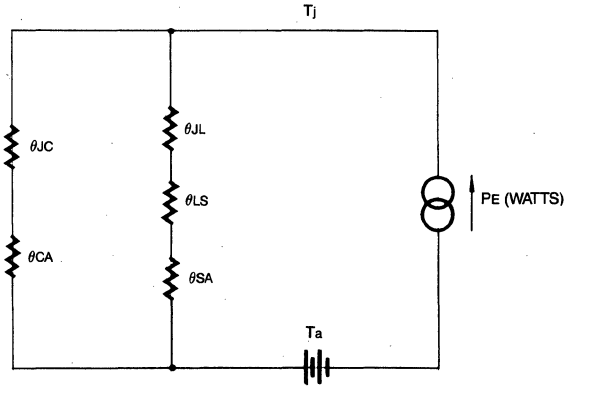


Fig. 2

Methods of Heat Sinking

With two external thermal resistances in each leg of a parallel network available to the circuit designer as variables, he can choose the method of heat sinking most applicable to his particular situation. To demonstrate, consider the effect of placing a small 72°C/W flag type heat sink, such as the Staver F1-7D-2, on the 78LXX molded case. The heat sink effectively replaces the θ_{CA} (Figure 2) and the new thermal resistance, θ'_{JA} =145°C/W (assuming, 125 inch lead length)

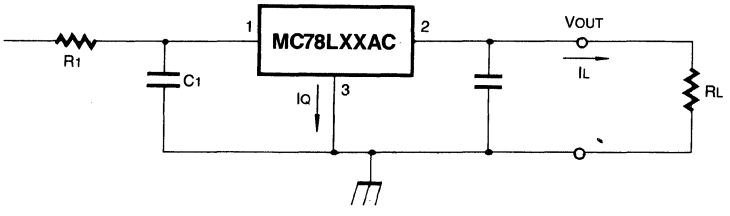
The net change of 15°C/W increases the allowable power dissipation to 0.86W with an inserted cost of 1-2 cents. A still further decrease in θ_{JA} could be achieved by using a heat sink rated at 46°C/W, such as the Staver FS-7A. Also, if the case sinking does not provide an adequate reduction in total θ_{JA}, the other external thermal resistance, θ_{LA}, may be reduced by shortening the lead length from package base to mounting medium. However, one point must be kept in mind. The lead thermal path includes a thermal resistance, θ_{SA}, from the pins at the mounting point to ambient, that is, the mounting medium, θ_{LA} is then equal to $\theta_{LS} + \theta_{SA}$. The new model is shown in Figure 2.

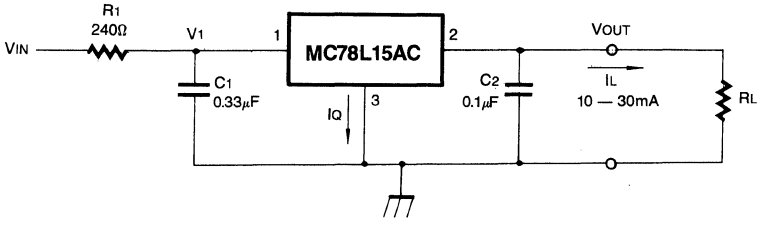
In the case of a socket, θ_{SA} could be as high as 270°C/W, thus causing a net increase in θ_{JA} and a consequent decrease in the maximum dissipation capability. Shortening the lead length may return the net θ_{JA} to the original value, but pin sinking would not be accomplished.

In those cases where the regulator is inserted into a copper clad printed circuit board, it is advantageous to have a maximum area of copper at the entry points of the pins. While it would be desirable to rigorously define the effect of PC board copper, the real world variables are too great to allow anything more than a few general observations.

The best analogy for PC board copper is to compare it with parallel resistors. Beyond some point, additional resistors are not significantly effective; beyond some point, additional copper area is not effective.

HIGH DISSIPATION APPLICATIONS





When it is necessary to operate a MC78LXXAC regulator with a large input-output differential voltage, the addition of series resistor R1 will extend the output current range of the device by sharing the total power dissipation between R1 and the regulator.

$$R1 \cong \frac{V_{IN\,(Min)} - V_{OUT} - 2.0V}{I_{L\,(Max)} + I_Q}$$

Where I_Q is the regulator quiescent current.

Regulator power dissipation at maximum input voltage and maximum load current is now

$$P_{D\,(Max)} = (V_1 - V_{OUT})\, I_{L\,(Max)} + V_1\, I_Q$$

where

$$V_1 = V_{IN\,(Max)} - (I_{L\,(Max)} + I_Q)\, R1$$

The presence of R1 will affect load regulation according to the equation:

load regulation (at constant V_{IN})
=load regulation (at constant V1)
+(line regulation, mV per V)
×(R1)×(ΔIL).

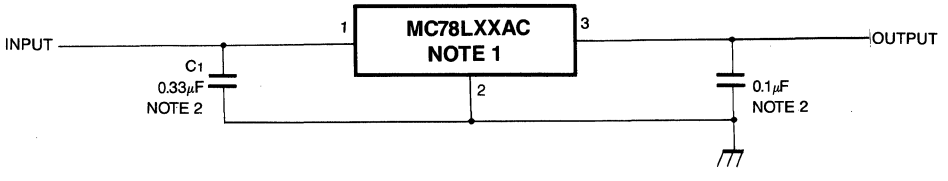
As an example, consider a 15V regulator with a supply voltage of 30 ±5V, required to supply a maximum load current of 30mA. I_Q is 4.3mA, and minimum load current is to be 10mA.

$$R_1 = \frac{(25\text{-}15\text{-}2)\ V}{(30+4.3)\ mA} = \frac{8V}{34.3mA} \cong 240\Omega$$

V1=35-(30+4.3).24=35-8.2=26.8V

$P_{D\,(Max)}$ =(26.8-15) 30+26.8 (4.3)
=354+115
=470mW, which permit operation up to 70°C in most applications.
Line regulation of this circuit is typically 110mV for an input range of 25 ~ 35V at a constant load current; i.e. 11mV/V

Load regulation =constant V_1 load regulation (typically 10mV, 10 ~ 30mA I_L)
+(11mV/V)×0.24×20mA (typically 53mV)
=63mV for a load current change of 20mA at a constant V_{IN} of 30V.

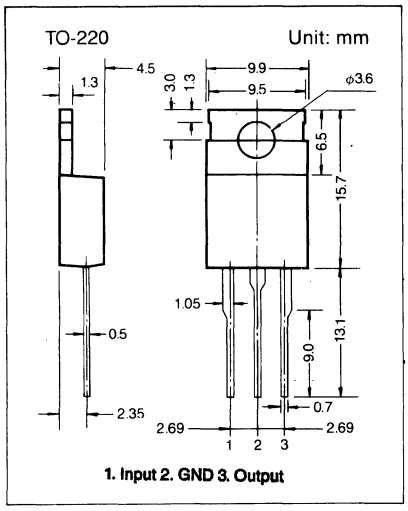


Notes

1. To specify an output voltage, substitute voltage value for "00".
2. Bypass Capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulator.

3-TERMINAL 0.5A POSITIVE VOLTAGE REGULATORS

The MC78MXXC series of three-terminal positive regulators is available TO-220 package with several fixed output voltages, making it useful in a wide range of applications. These reglators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they candeliver over 0.5A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



1. Input 2. GND 3. Output

FEATURES

- **Output Current up to 0.5A**
- **Output Voltages of 5; 6; 8; 10; 12; 15; 18; 20; 24V**
- **Thermal Overload Protection**
- **Short Circuit Protection**
- **Output Transistor SOA Protection**

BLOCK DIAGRAM

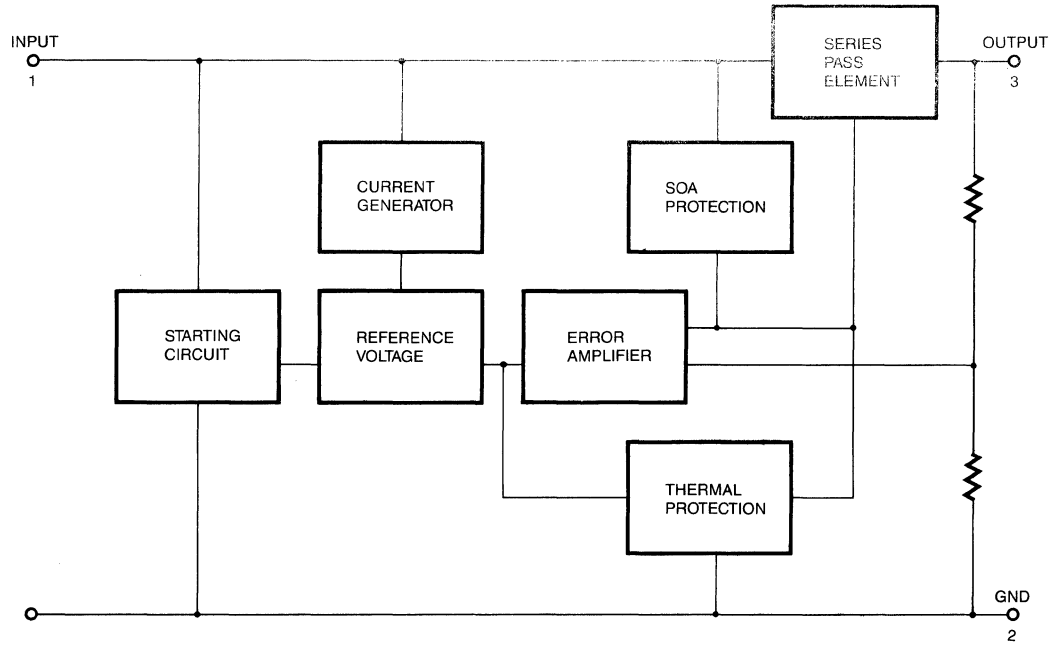


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
DC Input Voltage (for V_o = 5 to 18V)	V_i	35	V
(for V_o = 20, 24V)	V_i	40	V
Thermal Resistance Junction-Case	$Q_{j\text{-}c}$	5	°C/W
Junction-Air	$Q_{j\text{-}a}$	70	°C/W
Operating Junction Temperature	T_{opr}	0 ~ + 150	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

SCHEMATIC DIAGRAM

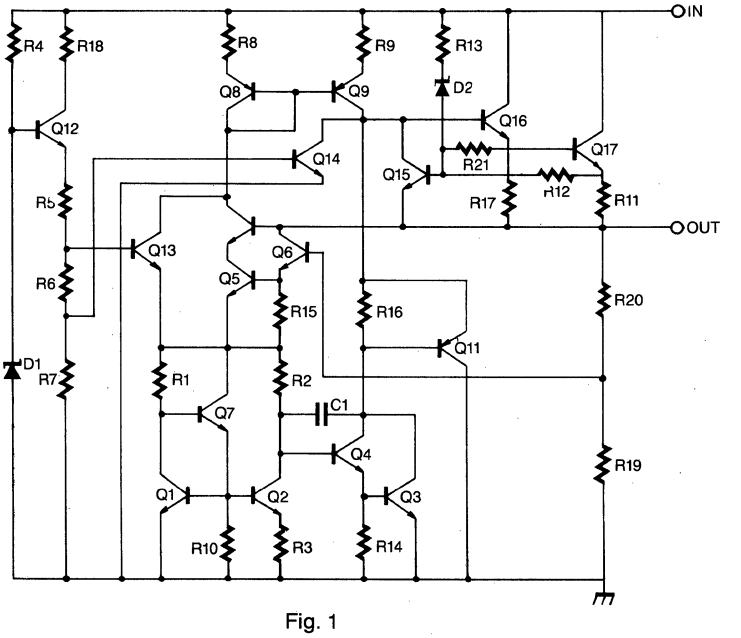


Fig. 1

ELECTRICAL CHARACTERISTICS MC78M05C

(Refer to the test circuits, T_j=25°C, I_o=350mA, V_i=10V, unless otherwise specified, C_i=0.33μF, C_o=0.1μF)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o		4.8	5	5.2	V
		I_o=5 to 350mA, V_i=7 to 20V	4.75	5	5.25	
Line Regulation	$\triangle V_o$	I_o=200mA, V_i=7 to 25V			100	mV
		I_o=200mA, V_i=8 to 25V			50	
Load Regulation	$\triangle V_o$	I_o=5mA to 0.5A			100	mV
		I_o=5mA to 200mA			50	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 350mA			0.5	mA
		I_o=200mA, V_i=8 to 25V			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA, T_j=0 to 125°C		-0.5		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz		40		μV
Supply Voltage Rejection	SVR	f=120Hz I_o=300mA, V_i=8 to 18V	62			dB
Dropout Voltage	V_d			2		V
Short Circuit Current	I_{sc}	V_i=35V		300		mA
Short Circuit Peak Current	I_{scp}			700		mA

ELECTRICAL CHARACTERISTICS MC78M06C

(Refer to the test circuits, T_j=25°C, I_o=350mA, V_i=11V unless otherwise specified, G_i=0.33μF, C_o=0.1μF)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o		5.75	6	6.25	V
		I_o=5 to 350mA, V_i=8 to 21V	5.7	6	6.3	
Line Regulation	$\triangle V_o$	I_o=200mA, V_i=8 to 25V			100	mV
		I_o=200mA, V_i=9 to 25V			50	
Load Regulation	$\triangle V_o$	I_o=5mA to 0.5A			120	mV
		I_o=5mA to 200mA			60	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 350mA			0.5	mA
		I_o=200mA, V_i=9 to 25V			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA, T_j=0 to 125°C		−0.5		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz		45		μV
Supply Voltage Rejection	SVR	f=120Hz I_o=300mA, V_i=9 to 19V	59			dB
Dropout Voltage	V_d			2		V
Short Circuit Current	I_{sc}	V_i=35V		270		mA
Short Circuit Peak Current	I_{scp}			700		mA

ELECTRICAL CHARACTERISTICS MC78M08C

(Refer to the test circuits, T_j=25°C, I_o=350mA, V_i=14V, unless otherwise specified, C_i=0.33μF, C_o=0.1μF)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o		7.7	8	8.3	V
		I_o=5 to 350mA V_i=10.5 to 23V	7.6	8	8.4	
Line Regulation	$\triangle V_o$	I_o=200mA, V_i=10.5 to 25V			100	mV
		I_o=200mA, V_i=11 to 25V			50	
Load Regulation	$\triangle V_o$	I_o=5mA to 0.5A			160	mV
		I_o=5mA to 200mA			80	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 350mA			0.5	mA
		I_o=200mA V_i=10.5 to 25V			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA T_j=0 to 125°C		−0.5		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz		52		μV
Supply Voltage Rejection	SVR	f=120Hz I_o=300mA V_i=11.5 to 21.5V	56			dB
Dropout Voltage	V_d			2		V
Short Circuit Current	I_{sc}	V_i=35V		250		mA
Short Circuit Peak Current	I_{scp}			700		mA

ELECTRICAL CHARACTERISTICS KA78M15C

(Refer to the test circuits, T_j=25°C, I_o=350mA, V_i=23V unless otherwise specified, C_i=0.33μF, C_o=0.1μF)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o		14.4	15	15.6	V
		I_o=5 to 350mA V_i=17.5 to 30V	14.25	15	15.75	
Line Regulation	$\triangle V_o$	I_o=200mA, V_i=17.5 to 30V			100	mV
		I_o=200mA, V_i=20 to 30V			50	
Load Regulation	$\triangle V_o$	I_o=5mA to 0.5A			300	mV
		I_o=5mA to 200mA			150	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 350mA			0.5	mA
		I_o=200mA V_i=17.5 to 30V			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA T_j=0 to 125°C		-1		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz		90		μV
Supply Voltage Rejection	SVR	f=120Hz I_o=300mA V_i=18.5 to 28.5V	54			dB
Dropout Voltage	V_d			2		V
Short Circuit Current	I_{sc}	V_i=35V		240		mA
Short Circuit Peak Current	I_{scp}			700		mA

ELECTRICAL CHARACTERISTICS KA78M18C

(Refer to the test circuits, T_j=25°C, I_o=350mA, V_i=26V, unless otherwise specified, C_i=0.33μF, C_o=0.1μF)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o		17.3	18	18.7	V
		I_o=5 to 350mA, V_i=20.5 to 33V	17.1	18	18.9	
Line Regulation	$\triangle V_o$	I_o=200mA, V_i=21 to 33V			100	mV
		I_o=200mA, V_i=24 to 33V			50	
Load Regulation	$\triangle V_o$	I_o=5mA to 0.5A			360	mV
		I_o=5mA to 200mA			180	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 350mA			0.5	mA
		I_o=200mA, V_i=21 to 33V			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA, T_j=0 to 125°C		−1.1		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz		100		μV
Supply Voltage Rejection	SVR	f=120Hz I_o=300mA, V_i=22 to 32V	53			dB
Dropout Voltage	V_d			2		V
Short Circuit Current	I_{sc}	V_i=35V		240		mA
Short Circuit Peak Current	I_{scp}			700		mA

ELECTRICAL CHARACTERISTICS KA78M20C

(Refer to the test circuits, T_j=25°C, I_o=350mA, V_i=29V, unless otherwise specified, C_i=0.33μF, C_o=0.1μF)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o		19.2	20	20.8	V
		I_o=5 to 350mA, V_i=23 to 35V	19	20	21	
Line Regulation	$\triangle V_o$	I_o=200mA, V_i=23 to 35V			100	mV
		I_o=200mA, V_i=24 to 35V			50	
Load Regulation	$\triangle V_o$	I_o=5mA to 0.5A			400	mV
		I_o=5mA to 200mA			200	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 350mA			0.5	mA
		I_o=200mA, V_i=23 to 35V			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA, T_j=0 to 125°C		−1.1		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz		110		μV
Supply Voltage Rejection	SVR	f=120Hz I_o=300mA, V_i=24 to 34V	53			dB
Dropout Voltage	V_d			2		V
Short Circuit Current	I_{sc}	V_i=35V		240		mA
Short Circuit Peak Current	I_{scp}			700		mA

ELECTRICAL CHARACTERISTICS KA78M24C

(Refer to the test circuits, T_j=25°C, I_o=350mA, V_i=33V, unless otherwise specified, C_i=0.33μF, C_o=0.1μF)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	
Output Voltage	V_o		23	24	25	V
		I_o=5 to 350mA, V_i=27 to 38V	22.8	24	25.2	
Line Regulation	$\triangle V_o$	I_o=200mA, V_i=27 to 38V			100	mV
		I_o=200mA, V_i=28 to 38V			50	
Load Regulation	$\triangle V_o$	I_o=5mA to 0.5A			480	mV
		I_o=5mA to 200mA			240	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 350mA			0.5	mA
		I_o=200mA, V_i=27 to 38V			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA, T_j=0 to 125°C		-1.2		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz		170		μV
Supply Voltage Rejection	SVR	f=120Hz I_o=300mA, V_i=28 to 38V	50			dB
Dropout Voltage	V_d			2		V
Short Circuit Current	I_{sc}	V_i=35V		240		mA
Short Circuit Peak Current	I_{scp}			700		mA

APPLICATION CIRCUIT

Fixed output regulator

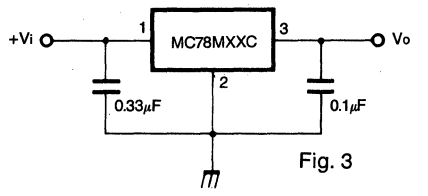


Fig. 3

Costant current regulator

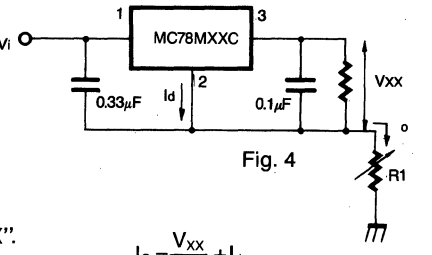


Fig. 4

$$I_O = \frac{V_{XX}}{R_1} + I_d$$

Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Circuit for increasing output voltage

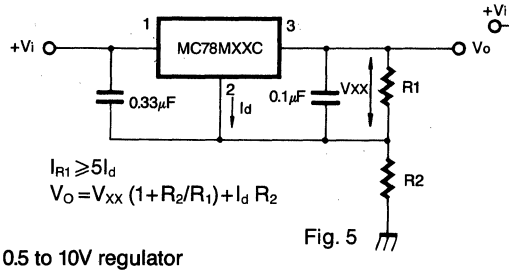


Fig. 5

Adjustable output regulator (7 to 30V)

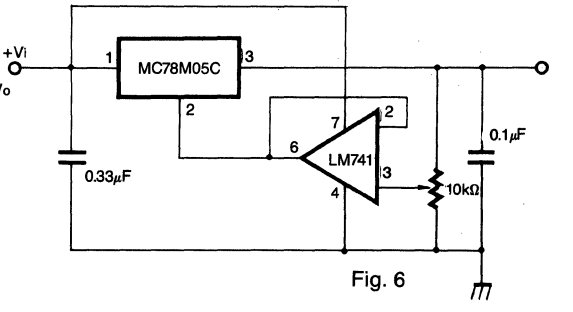


Fig. 6

0.5 to 10V regulator

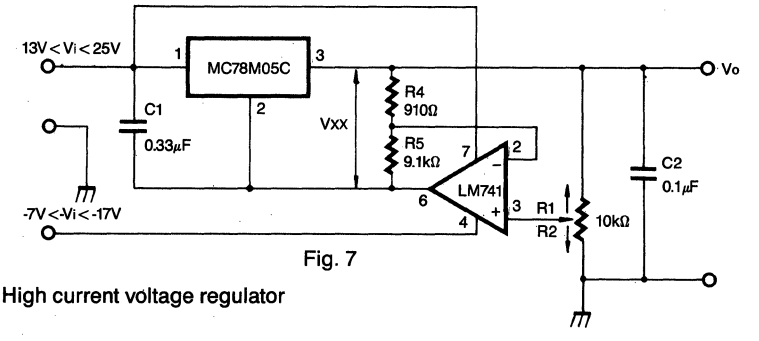


Fig. 7

$$V_O = V_{XX}\frac{R_4}{R_1}$$

High current voltage regulator

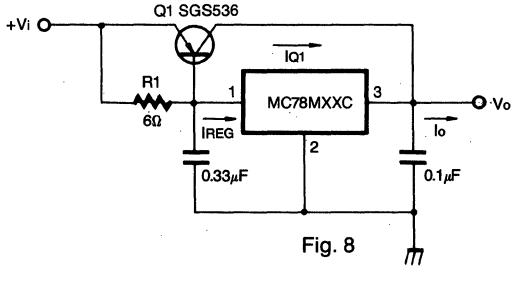


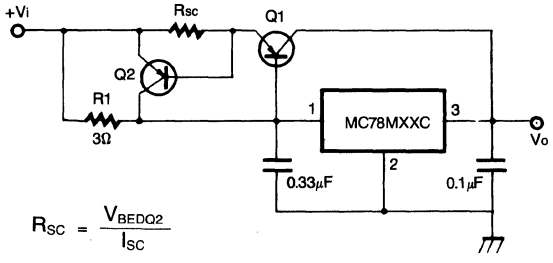
Fig. 8

$$R_1 = \frac{V_{BEQ1}}{I_{REQ} - \frac{I_{Q1}}{\beta_{Q1}}}$$

$$I_O = I_{REG} + \beta_{Q1}\left(I_{REG} - \frac{V_{BEQ1}}{R_{R1}}\right)$$

APPLICATION CIRCUIT (continued)

High output current with short circuit protection



$$R_{SC} = \frac{V_{BEDQ2}}{I_{SC}}$$

Fig. 12

Tracking voltage regulator

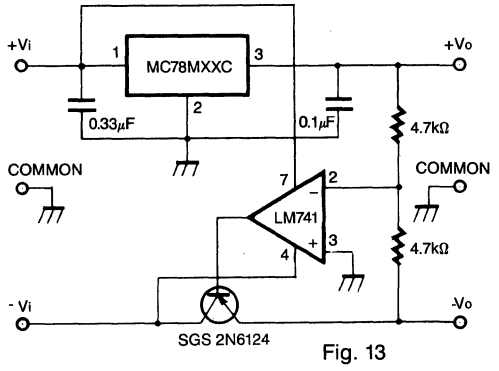
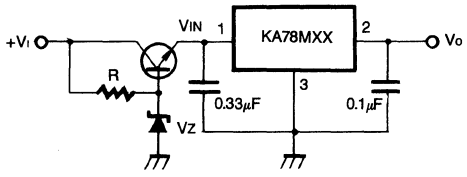


Fig. 13

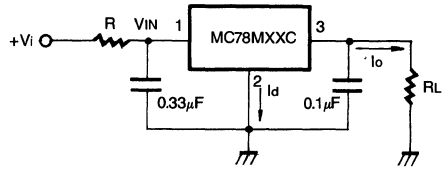
High input voltage circuit



$$V_{IN} = V_Z - V_{BE}$$

Fig. 14

Reducing power dissipation with dropping resistor



$$R = \frac{V_i(min) - V_{XX} - V_{DROP}(max)}{I_O(max) + I_d(max)}$$

Fig. 15

Power AM modultor (unity voltage gain, $I_o \leqslant 0.5$)

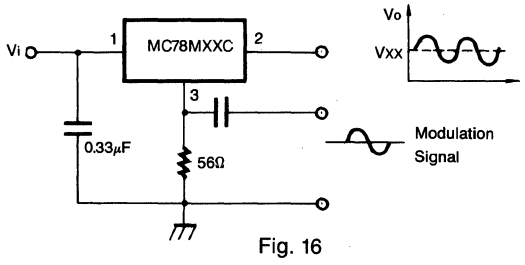


Fig. 16

Note: The circuit performs well up to 100 KHz.

Adjustable output voltage with temperature compensation

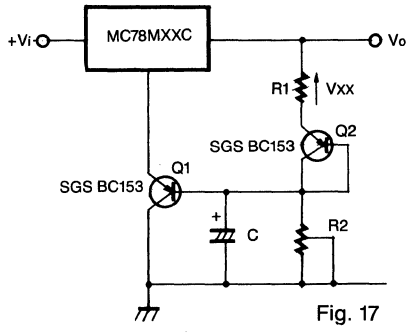


Fig. 17

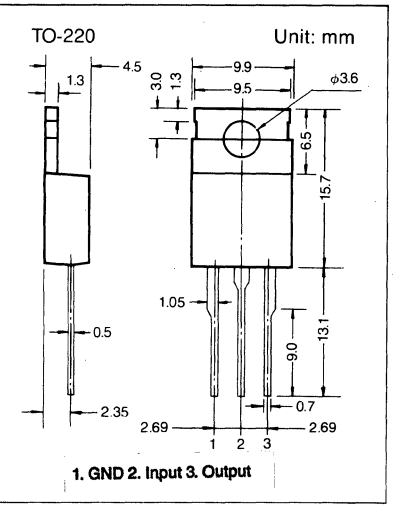
Note: Q2 is connected as a diode in order to compensate the variation of the Q1 V_{BE} with the temperature. C allows a slow rise-time of the Vo

$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

3-TERMINAL NEGATIVE VOLTAGE REGULATOR

The MC79XXC series of three-terminal negative regulators is available in TO-220 package and with several output voltages. They can provides local on-card regulation, eliminating the distribution problems associated with single point regulation; furthermore, having the same voltage options as the MC78XXC positive standard series, they are particularly suited for split power supplies. In addition, the −5.2V is also available for ECL system.

If adequate heat sinking is provided, the MC79XXC series can deliver an output current in excess of 1.5A. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



FEATURES

- **Output Current up to 1.5A**
- **Output Voltages of −2; −5; −5.2; −6; −8; −12; −15; −18; −20; −24V**
- **Thermal Overload Protection**
- **Short Circuit Protection**
- **Output Transistor SOA Protection**

SCHEMATIC DIAGRAM

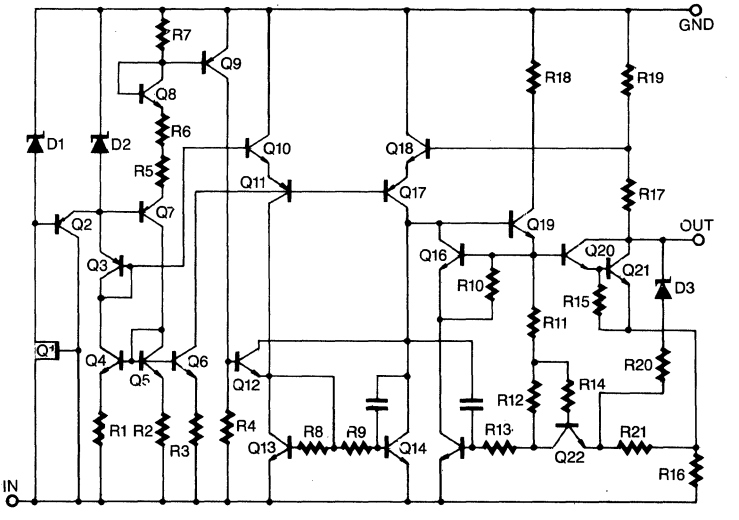


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (for V_o=5 to 18V)	V_i	−35	V
(for V_o=20 to −24V)	V_i	−40	V
Thermal Resistance Junction-Case	Q_{j-c}	5	°C/W
Junction-Air	Q_{j-a}	65	°C/W
Operating Junction Temperature	T_{opr}	0 ~ +150	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS MC7902C

(C_I=2.2μF, T_j=0 to 125°C, I_o=500mA, V_i=−10V, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C		−1.92	−2	−2.08	V
		I_o=5mA to 1A P_o<15W V_i=−7 to −20V		−1.9		−2.1	
Line Regulation	$\triangle V_o$	T_j=25°C	V_i=−7 to −25V			40	mV
			V_i=−8 to −12V			20	
Load Regulation	$\triangle V_o$	T_j=25°C I_o=5mA to 1.5A			70	120	mV
		T_j=25°C I_o=250 to 750mA			20	60	
Quiescent Current	I_d	T_j=25°C				2	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A				0.5	mA
		V_i=−7 to −25V				1.3	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA			−0.4		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz T_j=25°C			40		μV
Supply Voltage Rejection	SVR	f=120Hz $\triangle V_i$=10V		54	60		dB
Dropout Voltage	V_{i-o}	T_j=25°C I_o=1A $\triangle V_o$=100mV			2		V
Short Circuit Current	I_{sc}				2.2		A
Short Circuit Peak Current	I_{scp}	T_j=25°C			2.5		A

ELECTRICAL CHARACTERISTICS MC7905C

(C_I=2.2μF, T_j=0 to 125°C, I_o=500mA, V_i=−10V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	−4.8	−5	−5.2	V
		I_o=5mA to 1A, P_o<15W, V_i=−8 to −20V	−4.75	−5	−5.25	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=−7 to −25V			100	mV
		T_j=25°C, V_i=−8 to −12V			50	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			100	mV
		T_j=25°C, I_o=250 to 750mA			50	
Quiescent Current	I_d	T_j=25°C			2	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=−8 to −25V			1.3	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		−0.4		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		100		μV
Supply Voltage Rejection	SVR	f=120Hz, $\triangle V_i$=10V	54	60		dB
Dropout Voltage	V_{i-o}	T_j=25°C, I_o=1A, $\triangle V_o$=100mV		2		V
Short Circuit Current	I_{sc}			2.1		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.5		A

ELECTRICAL CHARACTERISTICS MC7906C

(C_I=2.2μF, T_j=0 to 125°C, I_o=500mA, V_i=−11V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	−5.75	−6	−6.25	V
		I_o=5mA to 1A, P_o<15W, V_i=−9 to −21V	−5.7		−6.3	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=−9 to −13V			120	mV
		T_j=25°C, V_i=−9 to −13V			60	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			120	mV
		T_j=25°C, I_o=250 to 750mA			60	
Quiescent Current	I_d	T_j=25°C			2	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=−9 to −25V			1.3	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		−0.5		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		130		μV
Supply Voltage Rejection	SVR	f=120Hz, $\triangle V_i$=10V	54	60		dB
Dropout Voltage	V_d	T_j=25°C, I_o=1A, $\triangle V_o$=100mV		1.5		V
Short Circuit Current	I_{sc}			1.8		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.5		A

ELECTRICAL CHARACTERISTICS MC7908C

(C_I=2.2μF, T_j=0 to 125°C, I_o=500mA, V_i=−14V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	−7.7	−8	−8.3	V
		I_o=5mA to 1A, P_o<15W, V_i=−11.5 to −23V	−7.6	−8	−8.4	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=−10.5 to −25V			160	mV
		T_j=25°C, V_i=−11 to −17V			80	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			160	mV
		T_j=25°C, I_o=250 to 750mA			80	
Quiescent Current	I_d	T_j=25°C			2	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=−11.5 to −25V			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		−0.6		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		175		μV
Supply Voltage Rejection	SVR	f=120Hz, $\triangle V_i$=10V	54	60		dB
Dropout Voltage	V_{i-o}	T_j=25°C, I_o=1A, $\triangle V_o$=100mV		1.1		V
Short Circuit Current	I_{sc}			1.5		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.5		A

ELECTRICAL CHARACTERISTICS MC7912C

(C_I =2.2μF, T_j =0 to 125°C, I_o =500mA, V_i = −19V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j =25°C	−11.5	−12	−12.5	V
		I_o =5mA to 1A, P_o <15W, V_i = −15.5 to −27V	−11.4	−12	−12.6	
Line Regulation	$\triangle V_o$	T_j =25°C, V_i = −14.5 to −30V			240	mV
		T_j =25°C, V_i = −16 to −22V			120	
Load Regulation	$\triangle V_o$	T_j =25°C, I_o =5mA to 1.5A			240	mV
		T_j =25°C, I_o =250 to 750mA			120	
Quiescent Current	I_d	T_j =25°C			3	mA
Quiescent Current Change	$\triangle I_d$	I_o =5mA to 1A			0.5	mA
		V_i = −15 to −30V			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o =5mA		−0.8		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j =25°C		200		μV
Supply Voltage Rejection	SVR	f=120Hz, $\triangle V_i$ =10V	54	60		dB
Dropout Voltage	V_{i-o}	T_j =25°C, I_o =1A, $\triangle V_o$ =100mV		1.1		V
Short Circuit Current	I_{sc}			1.5		A
Short Circuit Peak Current	I_{scp}	T_j =25°C		2.5		A

ELECTRICAL CHARACTERISTICS MC7915C

(C_I=2.2μF, T_j=0 to 125°C, I_o=500mA, V_i=−23V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	−14.4	−15	−15.6	V
		I_o=5mA to 1A, P_o<15W, V_i=−18 to −30V	−14.3	−15	−15.7	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=−17.5 to −30V			300	mV
		T_j=25°C, V_i=−20 to −26V			150	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			300	mV
		T_j=25°C, I_o=250 to 750mA			150	
Quiescent Current	I_d	T_j=25°C			3	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=−18.5 to −30V			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		−0.9		mV/°C
Output Noise Voltage	e_N	B=10Hz to 100KHz, T_j=25°C		250		μV
Supply Voltage Rejection	SVR	f=120Hz, $\triangle V_i$=10V	54	60		dB
Dropout Voltage	V_{i-o}	T_j=25°C, I_o=1A, $\triangle V_o$=100mV		1.1		V
Short Circuit Current	I_{sc}			1.3		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

ELECTRICAL CHARACTERISTICS MC7918C

(C_I=2.2μF, T_j=0 to 125°C, I_o=500mA, V_i=−27V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	−17.3	−18	−18.7	V
		I_o=5mA to 1A, P_o<15W, V_i=−22.5 to −33V	−17.1	−18	−18.9	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=−21 to −33V			360	mV
		T_j=25°C, V_i=−24 to −30V			180	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			360	mV
		T_j=25°C, I_o=250 to 750mA			180	
Quiescent Current	I_d	T_j=25°C			3	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=−22 to −33V			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		−1		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		300		μV
Supply Voltage Rejection	SVR	f=120Hz, $\triangle V_i$=10V	54	60		dB
Dropout Voltage	V_{i-o}	T_j=25°C, I_o=1A, $\triangle V_o$=100mV		1.1		V
Short Circuit Current	I_{sc}			1.1		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

ELECTRICAL CHARACTERISTICS MC7820C

(C_I=2.2μF, T_j=0 to 125°C, I_o=500mA, V_i=−29V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	−19.2	−20	−20.8	V
		I_o=5mA to 1A, P_o<15W, V_i=−24 to −35V	−19	−20	−21	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=−23 to −35V			400	mV
		T_j=25°C, V_i=−26 to −32V			200	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			400	mV
		T_j=25°C, I_o=250 to 750mA			200	
Quiescent Current	I_d	T_j=25°C			3	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=−24 to −35V			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		−1.1		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		350		μV
Supply Voltage Rejection	SVR	f=120Hz, $\triangle V_i$=10V	54	60		dB
Dropout Voltage	V_{i-o}	T_j=25°C, I_o=1A, $\triangle V_o$=100mV		1.1		V
Short Circuit Current	I_{sc}			0.9		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

ELECTRICAL CHARACTERISTICS MC7924C

(C_I=2.2μF, T_j=0 to 125°C, I_o=500mA, V_i=−33V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	−23	−24	−25	V
		I_o=5mA to 1A, P_o<15W, V_i=−27 to −38V	−22.8	−24	−25.2	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=−27 to −38V			480	mV
		T_j=25°C, V_i=−30 to −36V			240	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			480	mV
		T_j=25°C, I_o=250 to 750mA			240	
Quiescent Current	I_d	T_j=25°C			3	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=−27 to −38V			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		−1		mV/°C
Output Noise Voltage	e_N	B=10Hz to 100KHz, T_j=25°C		400		μV
Supply Voltage Rejection	SVR	f=120Hz, $\triangle V_i$=10V	54	60		dB
Dropout Voltage	V_{i-o}	T_j=25°C, I_o=1A, $\triangle V_o$=100mV		1.1		V
Short Circuit Current	I_{sc}			1.1		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.2		A

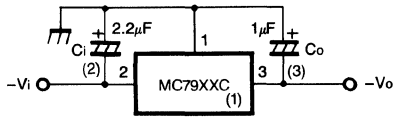
ELECTRICAL CHARACTERISTICS MC7952C

(C_I=2.2μF, T_j=0 to 125°C, I_o=500mA, V_i=−10V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	−5	−5.2	−5.4	V
		I_o=5mA to 1A, P_o<15W, V_i=−9 to −21V	−4.95	−5.2	−5.45	
Line Regulation	$\triangle V_o$	T_j=25°C, V_i=−8 to −25V			105	mV
		T_j=25°C, V_i=−9 to −13V			52	
Load Regulation	$\triangle V_o$	T_j=25°C, I_o=5mA to 1.5A			105	mV
		T_j=25°C, I_o=250 to 750mA			52	
Quiescent Current	I_d	T_j=25°C			2	mA
Quiescent Current Change	$\triangle I_d$	I_o=5mA to 1A			0.5	mA
		V_i=−9 to −25V			1.3	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o=5mA		−0.5		mV/°C
Output Noise Voltage	^eN	B=10Hz to 100KHz, T_j=25°C		125		μV
Supply Voltage Rejection	SVR	f=120Hz, $\triangle V_i$=10V	54	60		dB
Dropout Voltage	V_{i-o}	T_j=25°C, I_o=1A, $\triangle V_o$=100mV		1.8		V
Short Circuit Current	I_{sc}			2		A
Short Circuit Peak Current	I_{scp}	T_j=25°C		2.5		A

APPLICATION INFORMATION

Fig. 1 — Fixed output regulator



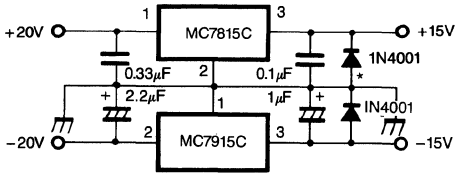
Notes:

(1) To specify an output voltage, substitute voltage value for "XXC".

(2) Required for stability. For value given, capacitor must be solid tantalum. If aluminium electrolitics are used, at least ten times value shown should be selected. Ci is required if regulator is located an appreciable distance from power supply filter.

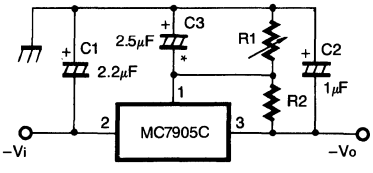
(3) To improve transient response. If large capacitors are used, a high current diode from input to output (1N4001 or similar) should be introduced to protect the device from momentary input short circuit.

Fig. 2 — Split power supply (±15V/1A)



* Against potential latch-up problems.

Fig. 3 — Circuit for increasing output voltage



$V_o = V_{XX} \cdot R1 + R1/R2$

$V_{XX}/R2 > 3\ I_d$

* C3 optional for improved transient response and ripple rejection.

Fig. 4 — High current negative regulator (−5V/4A with 5A current limiting)

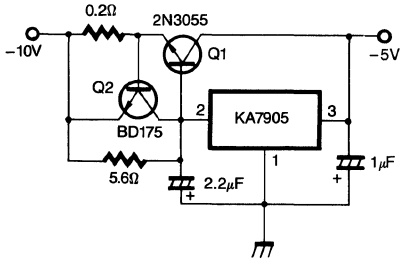
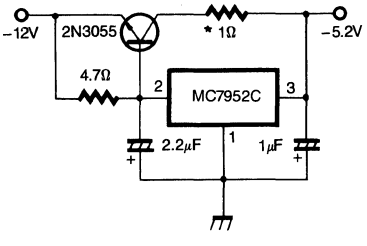


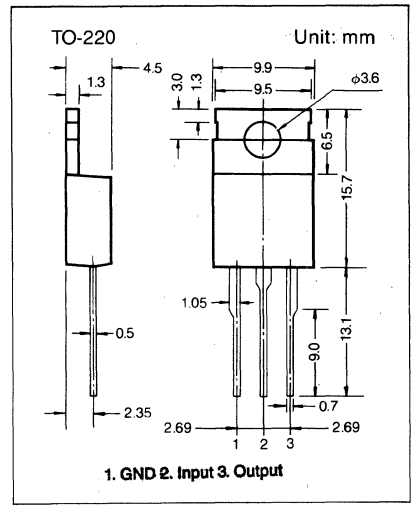
Fig. 5 — Typical ECL system power supply (−5.2V/4A)



* Optional dropping resistor to reduce the power dissipated in the boost transistor.

3-TERMINAL 0.5A NEGATIVE VOLTAGE REGULATOR

The MC79MXX series of 3-Terminal medium current negative voltage regulators are monolithic integrated circuits designed as fixed voltage regulators. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 500mA output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.



FEATURES

- **Output current in excess of 0.5A**
- **Internal thermal-overload protection**
- **Internal short circuit current limiting**
- **Output transistor safe-area compensation**
- **Available in jedec TO-220 and TO-39 packages**
- **Output voltages of −5V, −8V, −12V, and −15V**

SCHEMATHIC DIAGRAM

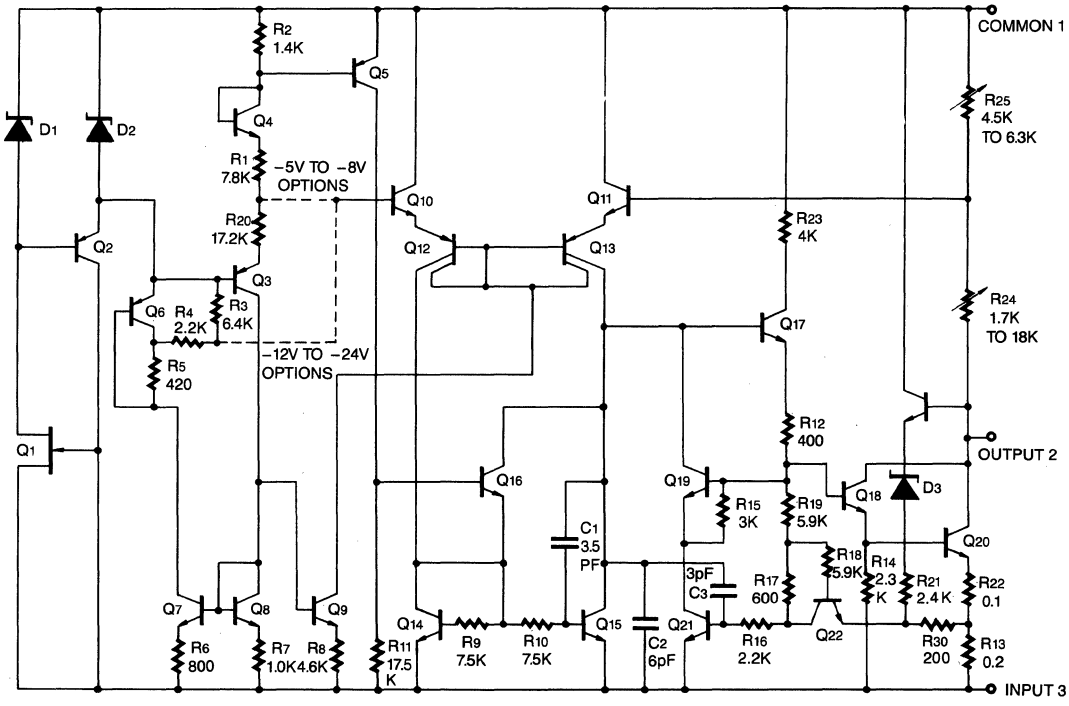


Fig. 1

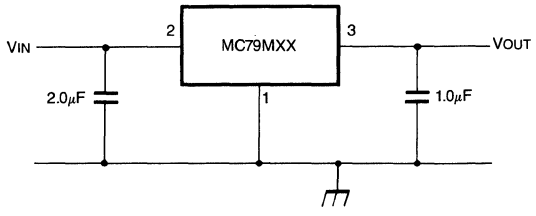
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (for −5 to −15V)	V_I	−35	V
(for −24V)	V_I	−40	V
Thermal Resistance			
Junction-Case	$\theta_{J\text{-}C}$	5	°C/W
Junction-Air	$\theta_{J\text{-}A}$	65	°C/W
Operating Junction Temperature	T_{OPR}	0~+125	°C
Storage Temperature	T_{STG}	−65~+150	°C

TYPICAL APPLICATION

Bypass capacitors are recommended for stable operation of the MC79MXXC series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.
The bypass capacitors, (2μF on the input, 1μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fixed Output Regulator



ELECTRICAL CHARACTERISTICS

(I_{OUT}=350mA, T_J=0 to (25°C, C_{IN}=2μF, C_{OUT}=1μF unless otherwise specified)

Output Voltage			**-5**			**-8**			**Unit**
Input Voltage (Unless Otherwise Specified)			**10**			**-14**			
Characteristic	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
Output Voltage	V_O	T_J=25	-5.2	-5.0	-4.8	-8.3	-8.0	-7.7	V
		I_O=5mA to 350mA $P_O \leq$ 4W	-5.25 (V_I= -7 to -25V)		-4.75	-8.4 (V_I= -10.5 to -25V)		-7.6	
Line Regulation	ΔV_O	T_J=25		7.0 (V_I= -7 to -18V)	50		8.0 (V_I= -10.5 to -25V)	80	mV
				3.0 (V_I= -8 to -18V)	30		4.0 V_I= -11 to -21V)	50	
Load Regulation	ΔV_O	T_J=25 I_O=5mA to 500mA		75	100		90	160	mV
		T_J=25 I_O=5mA to 350mA		50			60		
Quiescent Current	I_D	T_J=25	1	2		1	2		mA
Quiescent Current Change	ΔI_D	I_O=5mA to 350mA			0.4			0.4	mA
					0.4 (V_I=(-8 to -25V)			0.4 (V_I= -10.5 to -25V)	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	I_O=5mA		0.4			0.4		mV/°C
Output Noise Voltage	e_N	T_J=25 B=10Hz to 100KHz		125			200		μV
Supply Voltage Rejection	SVR	f=120Hz I_{OUT}=100mA	50 (V_I= -8 to -18V)			50 (V_I= -11.5 to -21.5V)			dB
Drop Output Voltage	V_{I-O}	T_J=25°C		1.1			1.1		V
Short Circuit Current	I_{SC}	T_J=25, V_I=-30V		140			140		mA
Output Peak Current	I_{SCP}	T_J=25		650			650		mA

ELECTRICAL CHARACTERISTICS

(I_{OUT} =350mA, T_J =0 to (25°C, C_{IN} =2μF, C_{OUT} =1μF unless otherwise specified)

Output Voltage			**-12**			**-15**			**Unit**
Input Voltage (Unless Otherwise Specified)			**-19**			**-23**			
Characteristic	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
Output Voltage	V_O	T_J =25	-12.5	12	-11.5	-15.6	15	-14.6	V
		I_O =5mA to 350mA $P_D \leq$ 4W	-12.6 (V_I = -14.5 to -30V)		-11.4	-15.75 (V_I = -17.5 to -30V)		-14.25	
Line Regulation	ΔV_O	T_J = 25		5.0 (V_I = -14.5 to -30V)	50		7.0 (V_I = -17.5 to -30V)	50	mV
				5.0 (V_I = -15 to -25V)	50		7.0 (V_I = -18 to -28V)	50	
Load Regulation	ΔV_O	T_J = 25 I_O =5mA to 1.5A		65	240		60	240	mV
		T_J = 25 I_O =250mA to 750mA		45			45		
Quiescent Current	I_D	T_J =25		1.5	3.0		1.5	3.0	
Quiescent Current Change	ΔI_D	I_O =5mA to 350mA			0.4			0.4	mA
					0.4 V_I =(-14.5 to -30V)			0.4 (V_I = -17.5 to -30V)	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	I_O = 5mA		0.8			1.0		mV/°C
Output Noise Voltage	e_N	T_J = 25 B = 10Hz to 100KHz		300			375		μV
Supply Voltage Rejection	SVR	f = 120Hz I_{OUT} = 100mA	50 (V_I = -15 to -25V)			50 (V_I = -1-.5 to -28.5V)			dB
Drop Output Voltage	V_{I-O}	T_J = 25°C		1.1			1.1		V
Short Circuit Current	I_{SC}	T_J =25, V_I =-30V		140			140		mA
Output Peak Current	I_{SCP}	T_J =25		650			650		mA

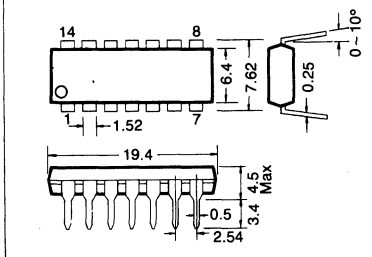
QUAD OPERATIONAL AMPLIFIER

The LM324/LM324A is a monolithic integrated circuit, consists of four independent amplifiers, high gain internally frequency compensated specifically to operate from a single power supply over a wide range of voltage.

Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single power supply systems.

14 Dip Unit: mm



FEATURES

- **No frequency compensation required.**
- **Differential input voltage range equal to the power supply voltage.**
- **Input common mode voltage range includes ground.**
- **Large output voltage swing** **0 V_{DC} to V_{CC}-1.5V_{DC}.**
- **Wide power supply voltage;**
  - **singly supply** **3 V_{DC} to 30 V_{DC}.**
  - **dual supply** **±1.5 V_{DC} to ±15 V_{DC}.**

SCHEMATIC DIAGRAM

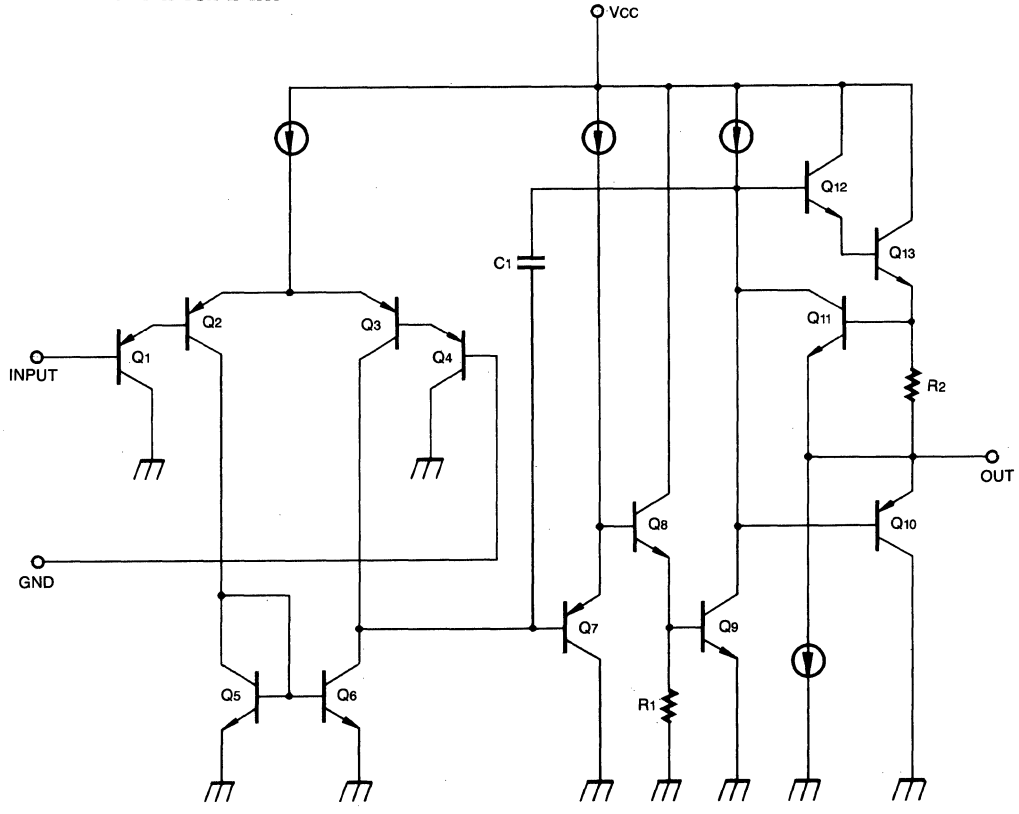


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage KA741C	V_{CC}	32 or ±16	V
Differential Input Voltage	V_{ID}	32	V
Input Voltage	V_I	−0.3~26	V
Power Dissipation	P_D	570	mW
Operating Temperature	T_{opr}	0~70	°C
Storage Temperature	T_{stg}	−65~150	°C

ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=5V)

Characteristic	Symbol	Test Conditions	LM324			LM324A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_o=1.4V, R_s=0		±2	±7		2	3	mV
Input Offset Current	I_{IO}	V_o=1.4V, R_s=0		±5	±50		5	30	nA
Input Bias Current	I_B	V_o=1.4V, R_s=0		45	250		45	100	nA
Input Common Mode Voltage Voltage Range	V_{ICM}		0		V_{CC}-1.5	0		V_{CC}-1.5	V
Supply Current		R_L= , V_{CC}=30V		1.5	3		1.5	3	mA
Large Signal Voltage Gain	A_v	V_{CC}=15V, R_L≥2KΩ	88	100		88	100		dB
Output Voltage Swing	V_{OUT}	R_L=2KΩ	0		V_{CC}-1.5	0		V_{CC}-1.5	V
Common Mode Rejection Ratio	CMR		65	70		65	85		dB
Power Supply Rejection Ratio	SVR		65	100		65	100		dB
Channel Separation	Sep	f=1KHz~20KHz		120			120		dB
Output Current (Source)	I_o (source)	V_{IN+}=1V, V_{IN-}=0V, V_{CC}=15V	20	40		20	40		mA
Output Current (Sink)	I_o (sink)	V_{IN+}=0V, V_{IN-}=1V, V_{CC}=15V	10	20		10	20		mA
		V_{IN+}=0V, V_{IN-}=1V, V_{CC}=200mV	12	50		12	50		μA

BLOCK DIAGRAM

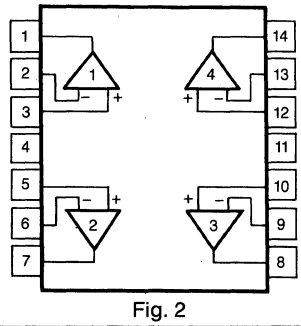


Fig. 2

PIN Connections

1. Out 1
2. − IN 1
3. + IN 1
4. Vcc
5. + IN 2
6. − IN 2
7. Out 2
8. Out 3
9. − IN 3
10. + IN 3
11. GND
12. + IN 4
13. − IN 4
14. Out 4

APPLICATION NOTE

The LM324 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger the V_{CC} without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3V_{DC}$ (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case noninverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

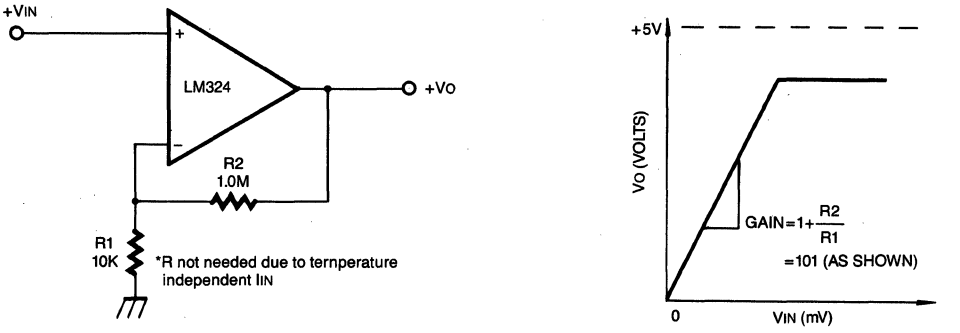
The bias network of the LM324 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

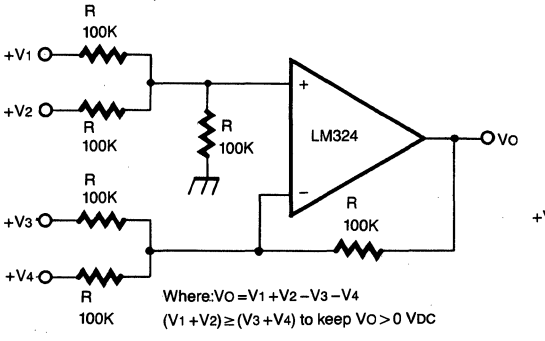
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. in general, introducing a pseudo-ground (a bias voltage reference of $V_{CC}/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

TYPICAL SINGLE-SUPPLY APPLICATIONS (V_{CC} = 5.0V_{DC})

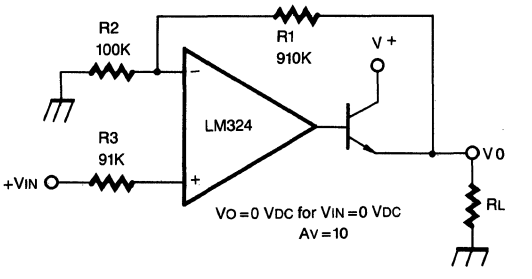
Non-Inverting DC Gain (0V Input=0V Output)



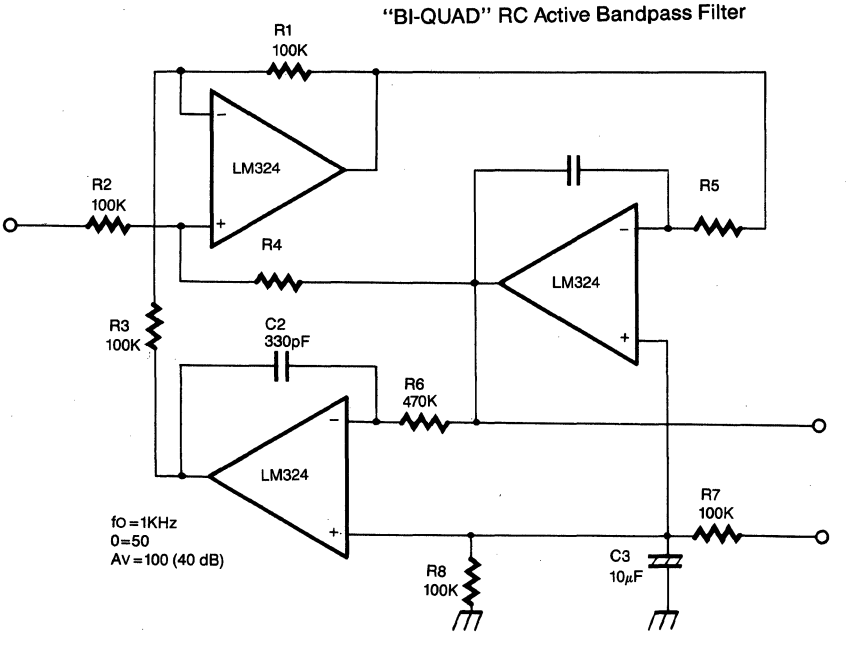
DC Summing Amplifier
(VIN'S ≥ 0 VDC AND VO ≥ 0 VDC)



Power Amplifier

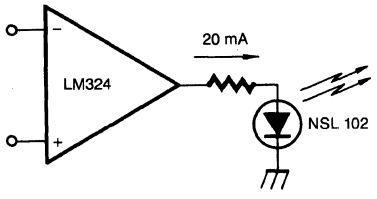


"BI-QUAD" RC Active Bandpass Filter

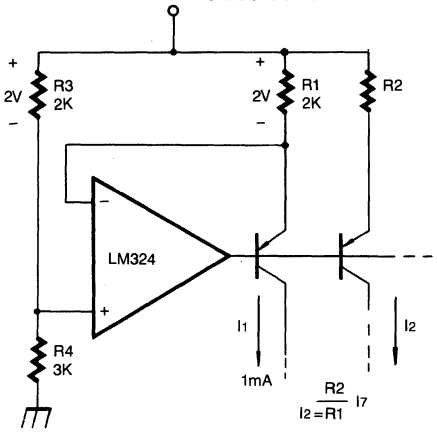


TYPICAL SINGLE-SUPPLY APPLICATIONS
(Continued (V_{CC} = 5.0V_{DC})

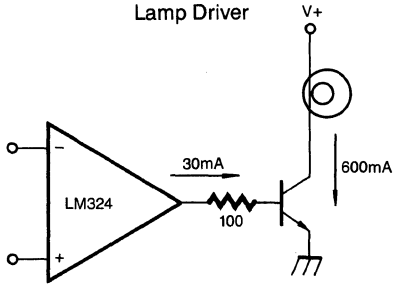
LED Driver



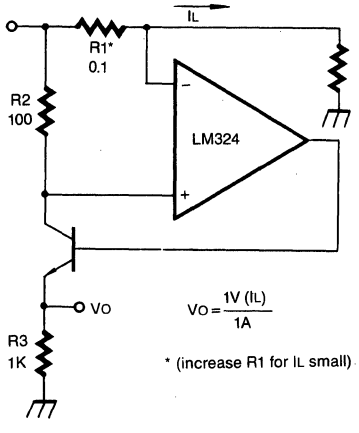
Fixed Current Sources



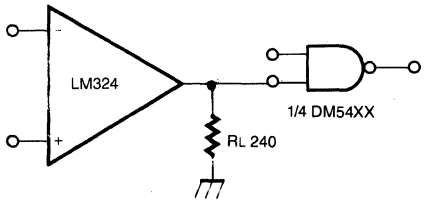
Lamp Driver



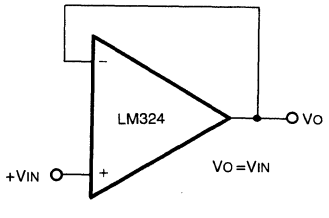
Current Monitor



Driving TTL

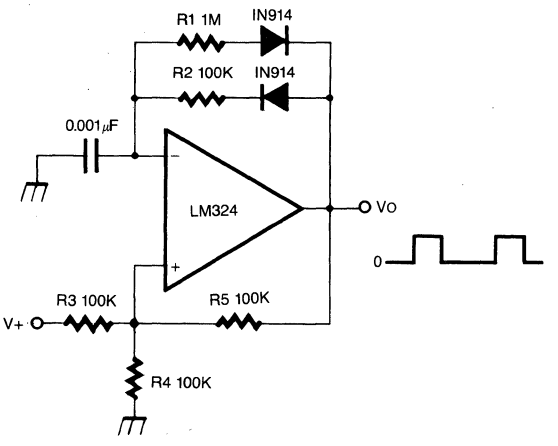


Voltage Follower

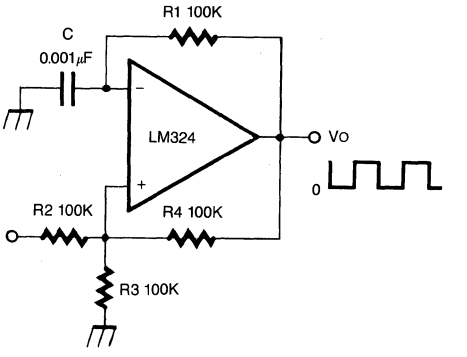


TYPICAL SINGLE-SUPPLY APPLICATIONS

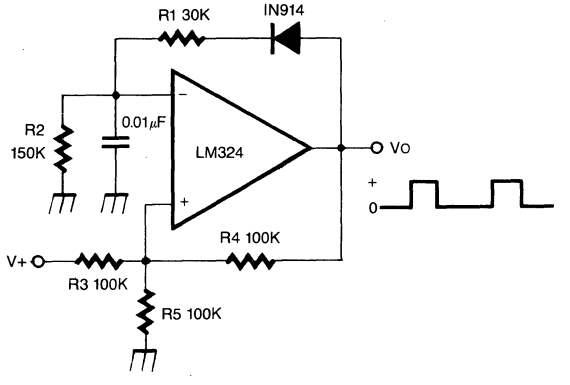
Pulse Generator



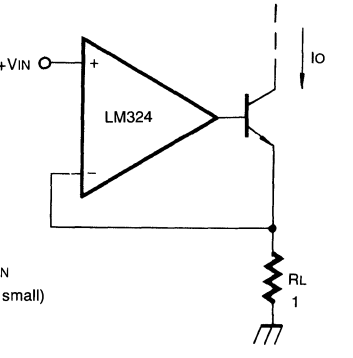
Squarewave Oscillator



Pulse Generator

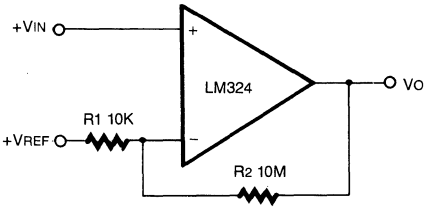


High Complifiance Current Sink

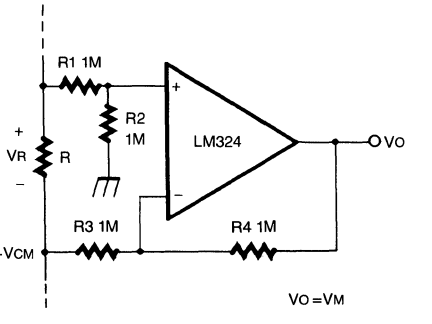


IO = 1 amp/volt VIN
(Increase RL for IO small)

Comparator with Hysteresis



Ground Referencing A Differential Input Signal

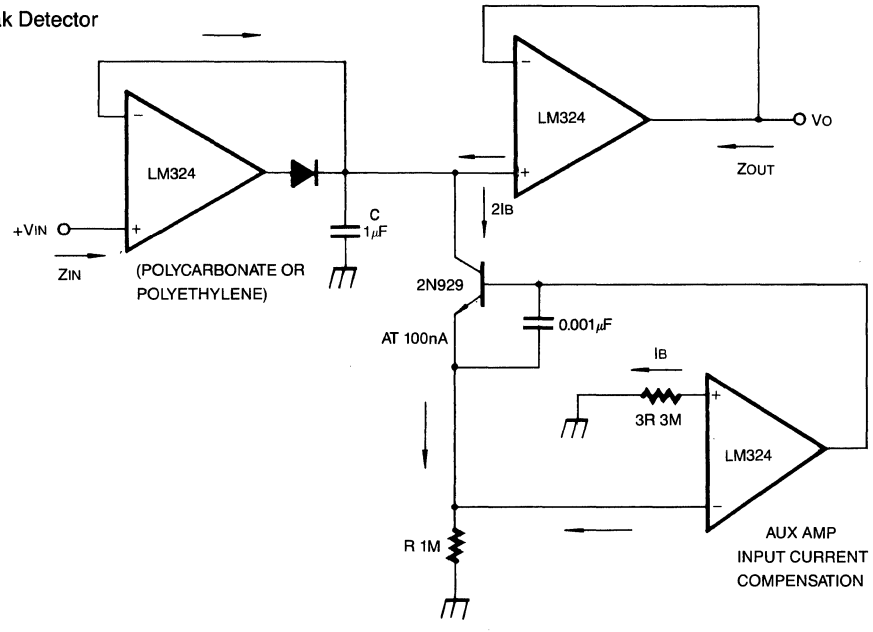


VO = VM

TYPICAL SINGLE-SUPPLY APPLICATIONS

(Continued V_{CC} = 5.0V_{DC})

Low Drift Peak Detector



Voltage Controlled Oscillator Circuit

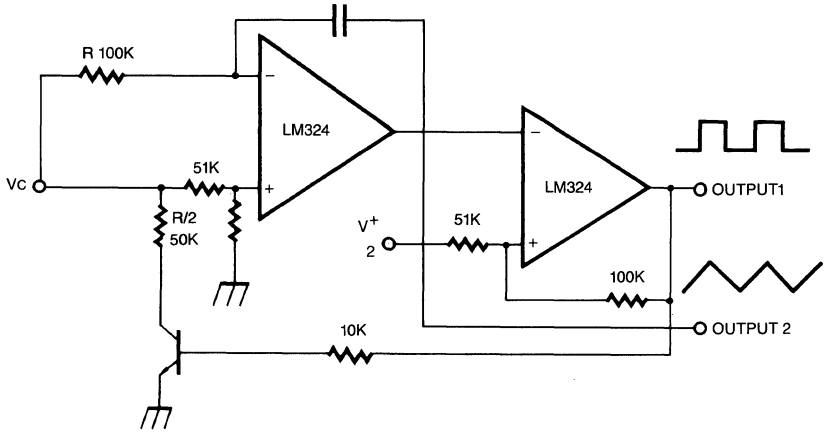
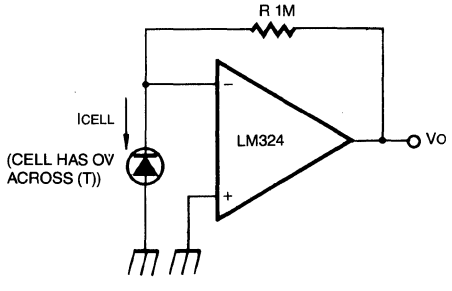
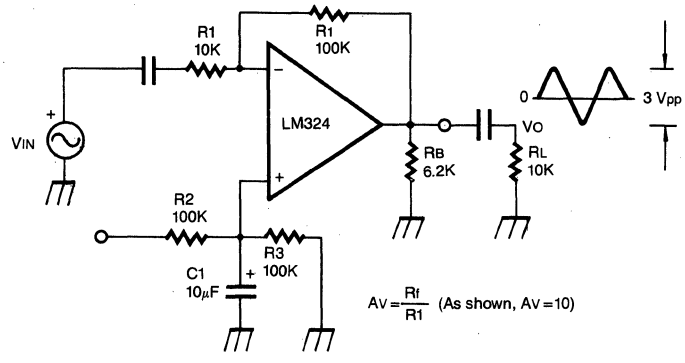


Photo Voltaic-Cell Amplifier



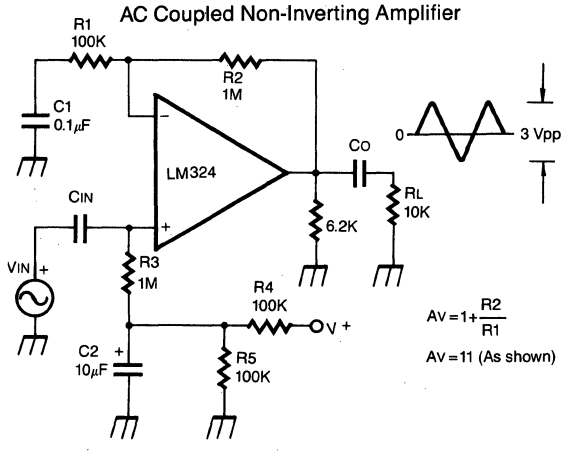
TYPICAL SINGLE-SUPPLY APPLICATIONS

AC Coupled Inverting Amplifier



$A_V = \frac{R_f}{R_1}$ (As shown, $A_V = 10$)

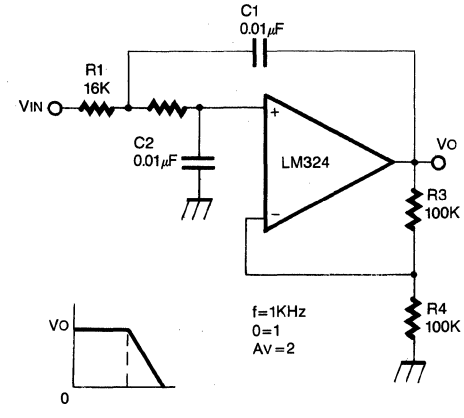
AC Coupled Non-Inverting Amplifier



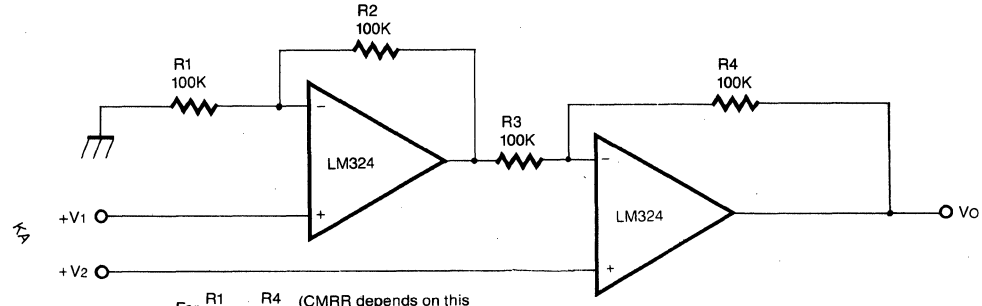
$A_V = 1 + \frac{R_2}{R_1}$

$A_V = 11$ (As shown)

DC Coupled Low-Pass RC Active Filter



High Input Z, DC Differential Amplifier

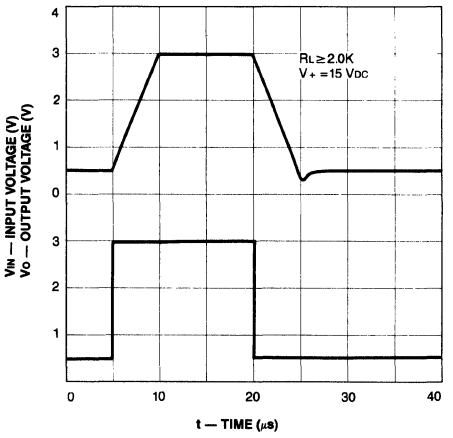


For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

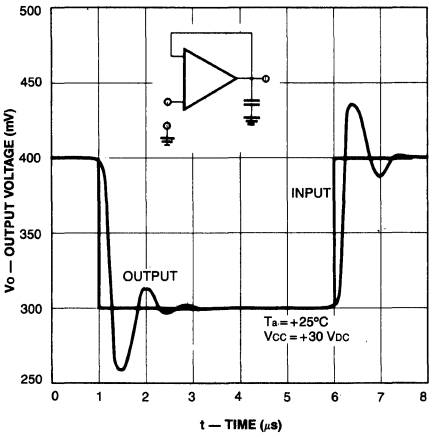
$V_O = 1 + \frac{R4}{R3} (V_2 - V_1)$

As shown: $V_O = 2 (V_2 - V_1)$

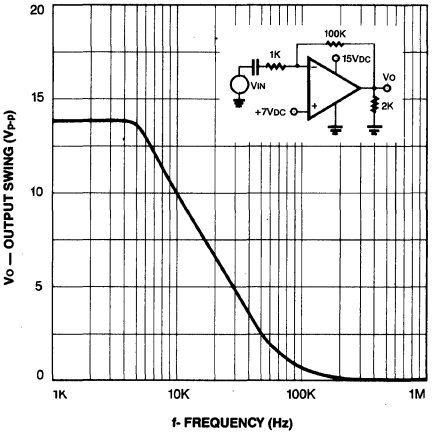
VOLTAGE FOLLOWER PULSE RESPONSE



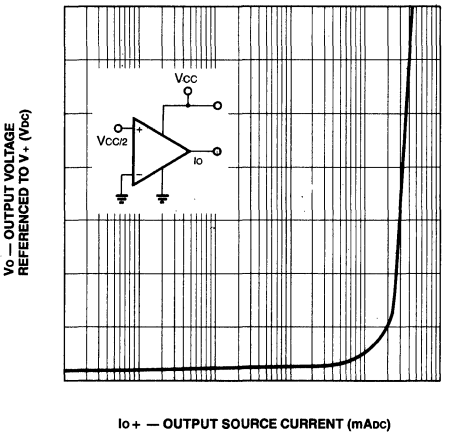
VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



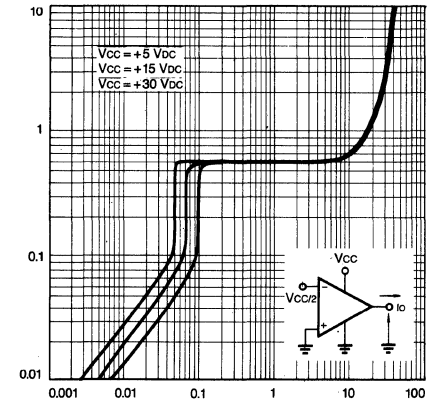
LARGE SIGNAL FREQUENCY RESPONSE



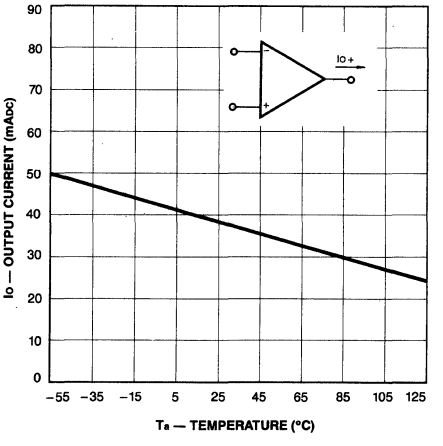
OUTPUT CHARACTERISTICS CURRENT SOURCING



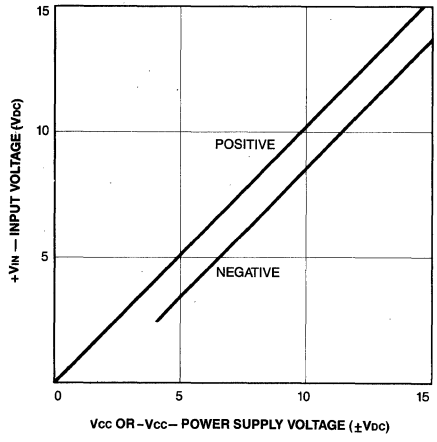
OUTPUT CHARACTERISTICS CURRENT SINKING



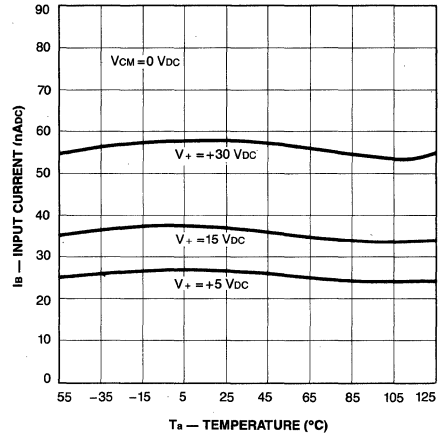
CURRENT LIMITING



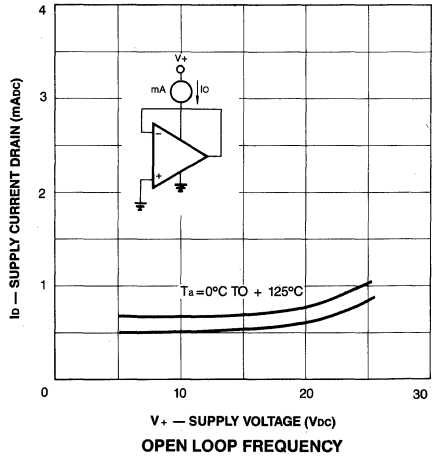
INPUT VOLTAGE RANGE



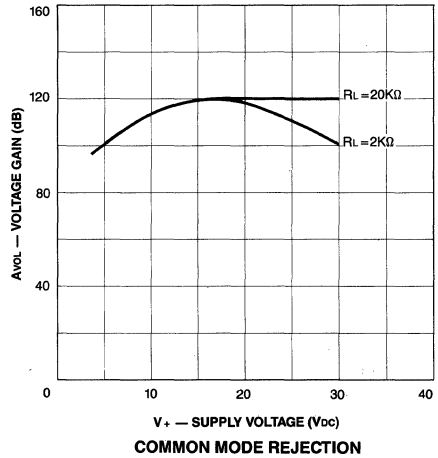
INPUT CURRENT



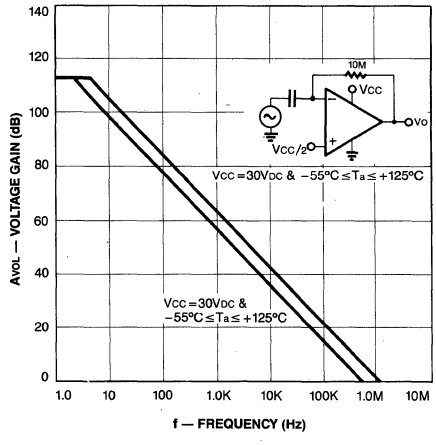
SUPPLY CURRENT



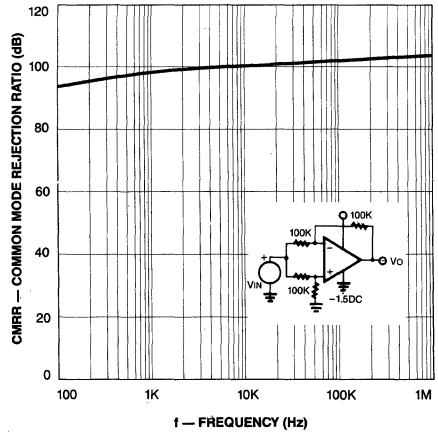
VOLTAGE GAIN



OPEN LOOP FREQUENCY RESPONSE



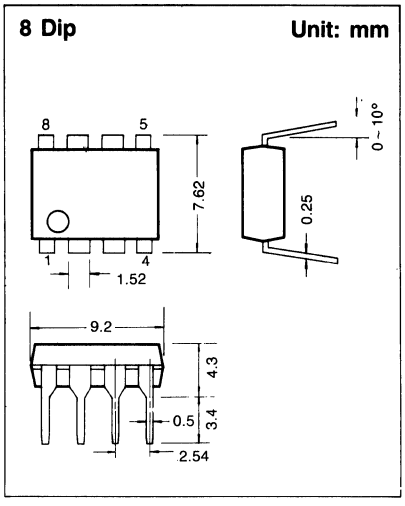
COMMON MODE REJECTION RATIO



DUAL OPERATIONAL AMPLIFIERS

The LM358/LM358A series consists of two independent, high-gain, frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages.

Operation from sprit supplies is also possible and the low supply current drain is independent of the magnitude of the supply voltage.
Applications include transducer amplifiers, D-C amplification blocks, and all the conventional OP amp circuits that now can be more easily implemented in single-supply-voltage systems.



FEATURES

- **No frequency compensation required.**
- **Differential input voltage range equal to the power supply voltage.**
- **Input common-mode voltage range includes ground.**
- **Range output voltage swing . . . 0 V_{dc} to V^+ −1.5V_{dc}**
- **Wide power supply voltage single supply or dual supply . . 3V_{dc} to 30 V_{dc}**

SCHEMATIC DIAGRAM (One section only)

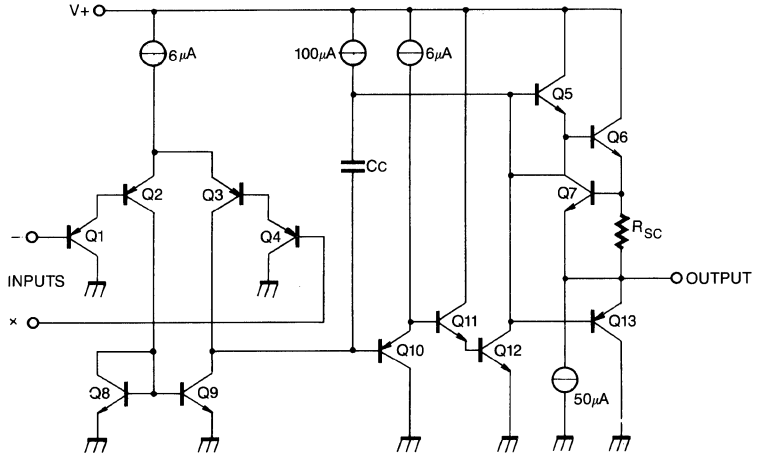


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	32	V
Differential Input Voltage	V_{ID}	C±32	V
Input Voltage	V_I	−0.3 ~ +32	V
Power Dissipation	P_d	650	mW
Operating Temeprature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

BLOCK DIAGRAM

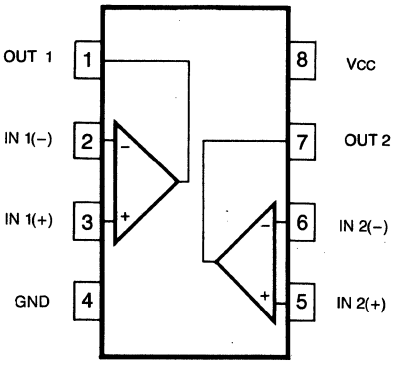


Fig. 2

ELECTRICAL CHARACTERISTICS

(V_{CC} =5V, T_a =0 to 70°C, unless therwise specified)

Characteristic	Symbol	Test Conditions		LM358 Min	LM358 Typ	LM358 Max	Unit
Supply Current	I_S	$R_L = \infty$	V_{CC} =30V		1	2	mA
					0.5	1.2	
Input Bias Current	I_b	T_a =25°C			45	250	nA
						500	
Input Offset Voltage	V_{os}	R_g =0 V_{CC} =5V to 30V	T_a =25C		±2	±7	mV
						±9	
Input Offset Voltage Drift	$\frac{\triangle V_{os}}{\triangle T}$	R_g =0			7		μV/°C
Input Offset Current	I_{OS}	T_a =25°C			±5	±50	nA
						±150	
Input Offset Current Drift	$\frac{\triangle I_{os}}{\triangle T}$				10		pA/°C
Output Short Circuit to Ground Current	I_{sc}	T_a =25°C*			40	60	mA
Large Signal Open Loop Voltage Gain	A_v	V_{CC} =15V $R_L \geqslant$ 2KΩ	T_a =25°C	88	100		dB
				83			
Input Common Mode Voltage Range	V_{LM}	V_{CC} =30V	T_a =25°C	0		V_{CC}-1.5	V
				0		V_{CC}-2	
Output Voltage Swing	V_o	T_a = 25°C	R_L = 2 KΩ			V_{CC}-1.5	V
			$R_L \geqq$10KΩ				
		V_{CC} =30V	R_L =2 KΩ	26			V
			$R_L \geqq$10 KΩ	27	28		
Output Saturation Voltage to Ground	$V_{o\,sat}$	$R_L \leqslant$ 10 KΩ			5	20	mV
Common Mode Rejection	CMR	T_a =25°C		65	70		dB
Supply Voltage Rejection	SVR	T_a =25°C		65	70		dB
Channel Separation	CS	f=1 KHz to 20KHz T_a =25°C (Input referred)			120		dB

ELECTRICAL CHARACTERISTICS

(V_{CC} =5V, T_a =0 to 70°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM358			Unit
				Min	Typ	Max	
Output Source Current	I_o^+	V_{CC} =15V V_i^+ =1V V_i^- =0V	T_a =25°C	20	40		mA
				10	20		
Output Sink Current	I_o^-	V_i^+ =0V V_i^- =1V V_o =200mV	T_a =25°C	12	50		μA
		V_i^- =1V V_i^+ =0V V_{CC} =15V	T_a =25°C	10	20		mA
				5	8		

* Short circuits from the output to positive supply voltage can cause excessive heating and eventual destruction. The maximum output current is 40 mA typ. independent of the magniture of V_{CC}.Destructive dissipation can result from simultaneous shorts on all amplifiers.

ELECTRICAL CHARACTERISTICS

(V_{CC} =5V, T_a =0 to 70°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM358A			Unit
				Min	Typ	Max	
Supply Current	I_S	$R_L = \infty$	V_{CC} =30V		1	2	mA
					0.5	1.2	
Input Bias Current	I_b	T_a =25°C			45	100	nA
						200	
Input Offset Voltage	V_{os}	R_g =0 V_s =5V to 30V	T_a =25C		±2	±3	mV
						±5	
Input Offset Voltage Drift	$\frac{\triangle V_{os}}{\triangle T}$	R_g =0			7	30	μV/°C
Input Offset Current	I_{OS}	T_a =25°C			±5	±30	nA
						±75	
Input Offset Current Drift	$\frac{\triangle I_{os}}{\triangle T}$				10	300	pA/°C
Output Short Circuit to Ground Current	I_{sc}	T_a =25°C *			40	60	mA
Large Signal Open Loop Voltage Gain		V_{CC} =15V $R_L \geqslant 2K\Omega$	T_a =25°C	88	100		dB
				83			
Input Common Mode Voltage Range		V_a =30V	T_a =25°C	0		V_{CC}-1.5	V
				0		V_{CC}-2	

ELECTRICAL CHARACTERISTICS

(V_{CC} =5V, T_a =0 to 70°C, unless therwise specified)

Characteristic	Symbol	Test Conditions		LM358A			Unit
				Min	Typ	Max	
Output Voltage Swing	V_o	T_a =25°C	R_L = 2 KΩ			V_{CC}-1.5	V
			R_L ≧10KΩ				
		V_{CC} =30V	R_L =2 KΩ	26			V
			R_L ≧10 KΩ	27	28		
Output Saturation Voltage to Ground	V_o sat	R_L ≦ 10 KΩ			5	20	mV
Common Mode Rejection	CMR	T_a =25°C		65	85		dB
Supply Voltage Rejection	SVR	T_a =25°C		65	100		dB
Channel Seperation	CS	f=1 KHz to 20KHz T_a =25°C (Input referred)			120		dB
Output Source Current	I_o^+	V_{CC} =15V V_i^+ =1V V_i^- =0V	T_a =25°C	20	40		mA
				10	20		
Output Sink Current	I_o^-	V_i^+ =0V V_i^- =1V V_o =200mV	T_a =25°C	12	50		μA
		V_i^- =1V V_i^+ =0V V_{CC} =15V	T_a =25°C	10	20		mA
				5	8		

* Short circuits from the output to positive supply voltage can cause excessive heating and eventual destruction. The maximum output current is 40 mA typ, independent of the magniture of V_{CC}. Destructive dissipation can result from simultaneous shorts on all amplifiers.

APPLICATION INFORMATION

Full wave rectifier

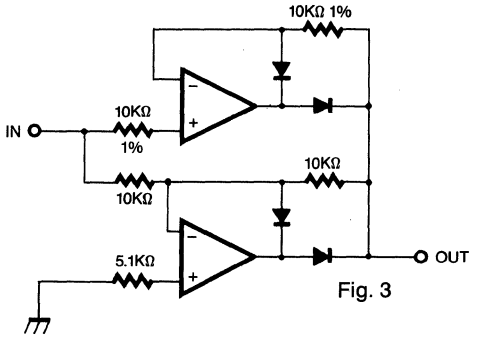


Fig. 3

Half wave rectifier

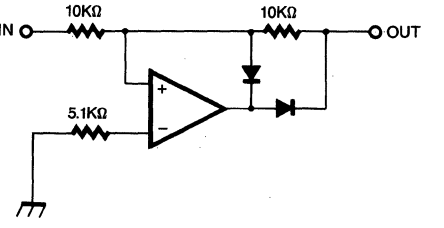


Fig. 4

Voltage reference

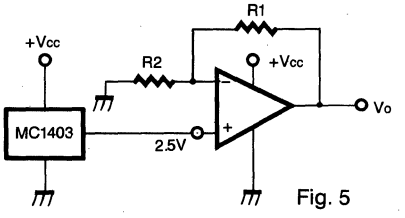


Fig. 5

$V_o = 2.5V\ (1+R1/R2)$

High-pass filter

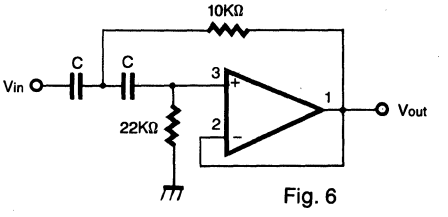


Fig. 6

$f_c = 100$ Hz with $C = 0.1\mu F$

Multiple feedback bandpass filter

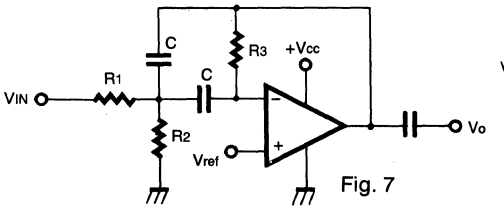


Fig. 7

Low-pass filter

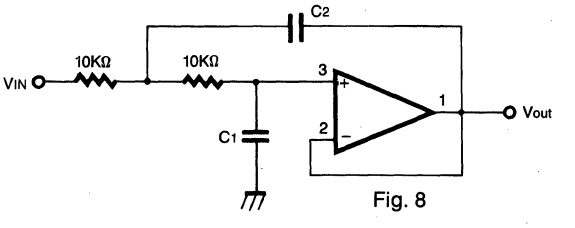


Fig. 8

$f_c = 3$KHz with C1=3.9nF and C2=6.8nF.

Given f_o = Center Frequency
A (f_o) = Gain at Center Frequency
Choose Value f_o, C
$R3 = Q/\pi\ f_oC$; $R1 = R3/2A$ (f_o); $R2 = R1 \cdot R3/(4Q^2\ R1-R3)$
For less than 10% error from operational amplifier
$Q_of_o/BW < 0.1$ Where f_o and BW are expressed in Hz. If source impedance varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

Supply current

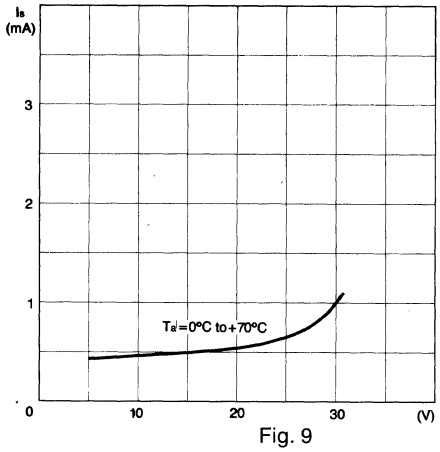


Fig. 9

Voltage gain

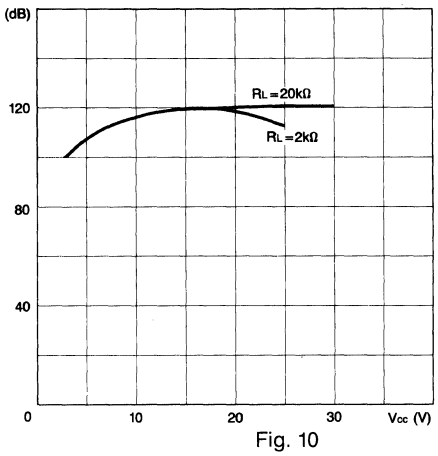


Fig. 10

Open loop frequency response

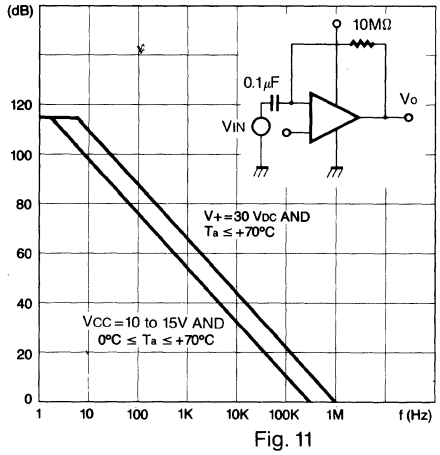


Fig. 11

Large signal frequency response

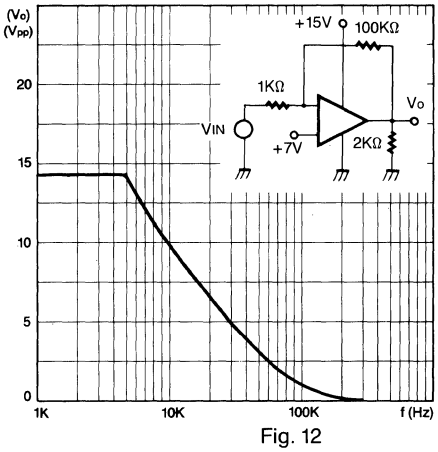


Fig. 12

Output characteristics (current sourcing)

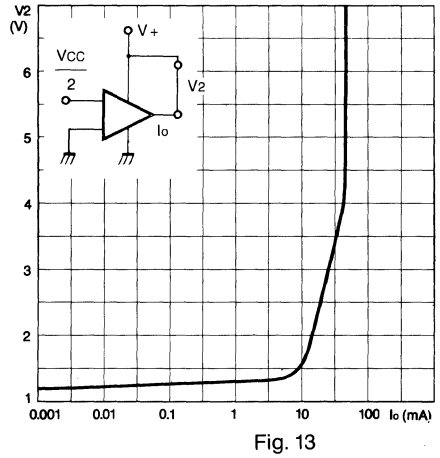


Fig. 13

Output characteristics (current sinking)

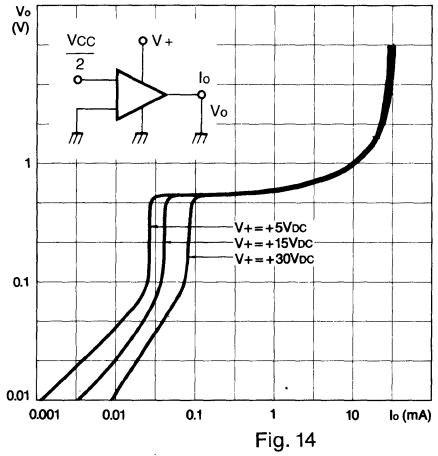


Fig. 14

Input voltage range

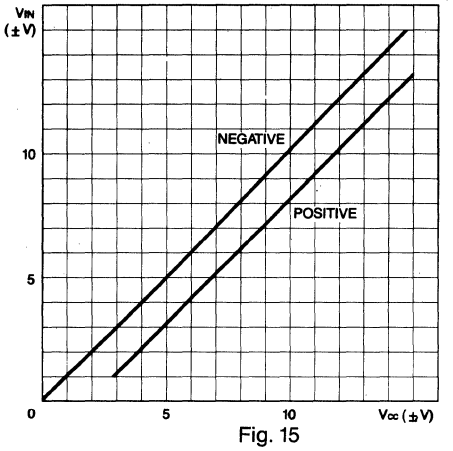


Fig. 15

Input current

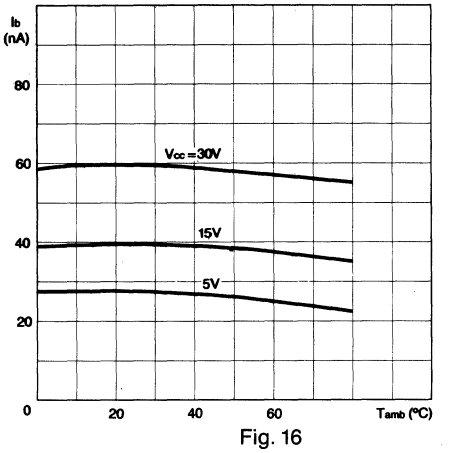


Fig. 16

Common mode rejection ratio

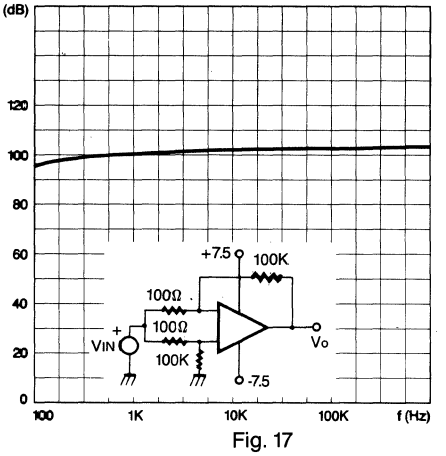
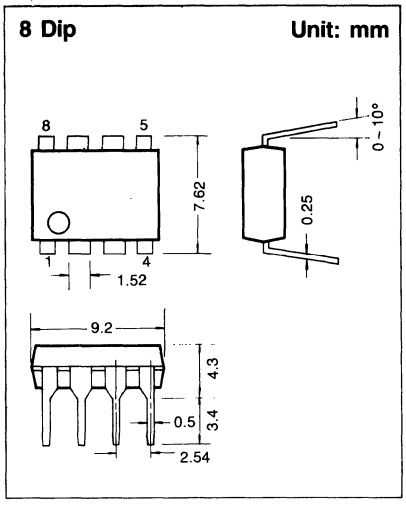


Fig. 17

GENERAL PURPOSE OPERATIONAL AMPLIFIER

The LM741C is a high performance operational amplifier with high open loop again.



FEATURES

- **Short circuit protection**
- **Excellent temperature stability**
- **Internal frequency compensation**
- **High input voltage range**
- **Direct replacement for μA 741**
- **Null of offset**

SCHEMATIC DIAGRAM

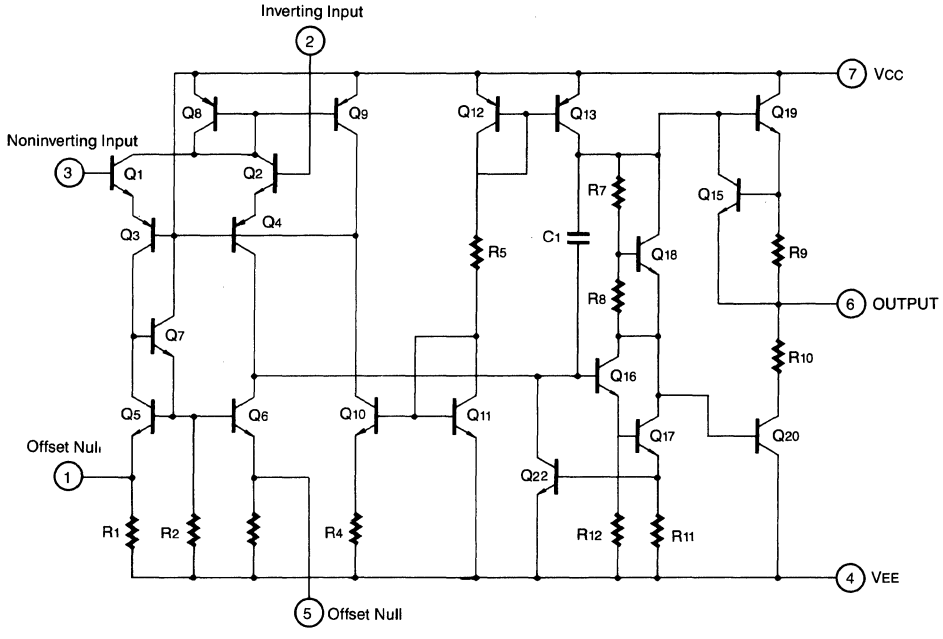


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

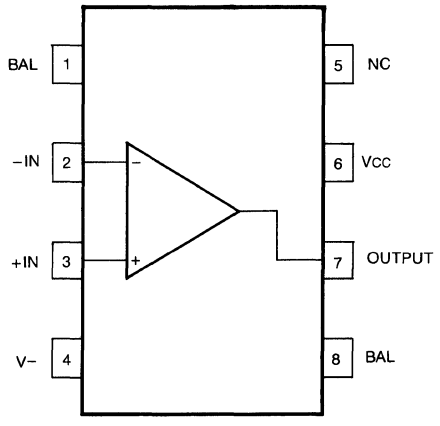
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	±18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage	V_I	±15	V
Power Dissipation	P_d	500	mW
Operating Temperature	Topr	0 ~ +70	°C
Storage Temperature	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C, V_{CC} = 15V, V_{EE} = −15V)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	$R_s \leq 10k\Omega$		2.0	6.0	mV
Input Offset Current	I_{IO}			20	200	nA
Input Bias Current	I_B			80	500	nA
Input Capacitance	C_i		0.3	2.0		MΩ
Offset Voltage Adjustment Range	—			±15		mV
Input Voltage Range	V_{ICM}		±12	±13		V
Common Mode Rejection Ratio	CMR	$R_s \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	SVR	$R_s \leq 10k\Omega$		30	150	μV/V
Large Signal Voltage Gain	A_v	$R_L \geq 2k\Omega$, V_{out} = ±10V	20	200		$\times 10^3$
Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$	±12	±14		V
		$R_L \geq 2k\Omega$	±10	±13		
Output Resistance	R_O		75		Ω	
Output Short Circuit Current	I_O			25		mA
Supply Current	I_{CC}			1.7	2.8	mA
Power Consumption	P_C			50	85	mW

ELECTRICAL CHARACTERISTICS ($0°C \leq T_a \leq 70°C$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}				7.5	mV
Input Offset Current	I_{IO}				300	nA
Input Bias Current	I_B			800	nA	
Large Signal Voltage Gain	A_v	$R_L \geq 2K\Omega$, Vout=±10V	83.5			dB
Output Voltage Swing	V_{OM}	$R_L \geq 2K\Omega$	±10	±13		V

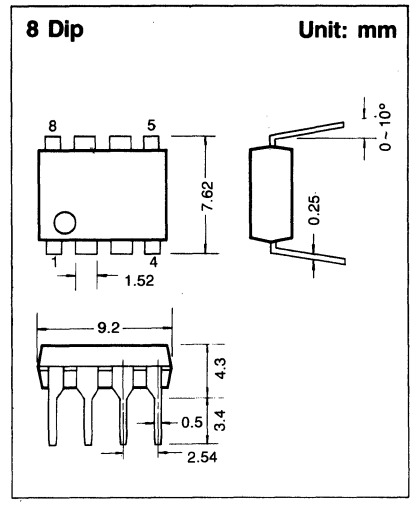


PIN CONNECTIONS

PIN 1: OFFSET NULL
PIN 2: -IN
PIN 3: +IN
PIN 4: V-
PIN 5: OFFSET NULL
PIN 6: OUTPUT
PIN 7: V_{CC}
PIN 8: NC

DUAL OPERATIONAL AMPLIFIER

The MC4558C is a monolithic integrated circuit designed for dual operational amplifier.



FUNCTIONS

- Internally frequency compensated.
- Short-circuit pretected.
- Low noise input transistors.

FEATURES

- **2MHz unity gain band width guaranteed.**
- **No frequency compensation required.**
- **No latch-up.**
- **Large common mode and differential voltage range.**
- **Parameter tracking over temperature range.**
- **Gain and phase match between amplifiers.**
- **Direct replacement for MC1458/MC1458C/MC4558C**

SCHEMATIC DIAGRAM

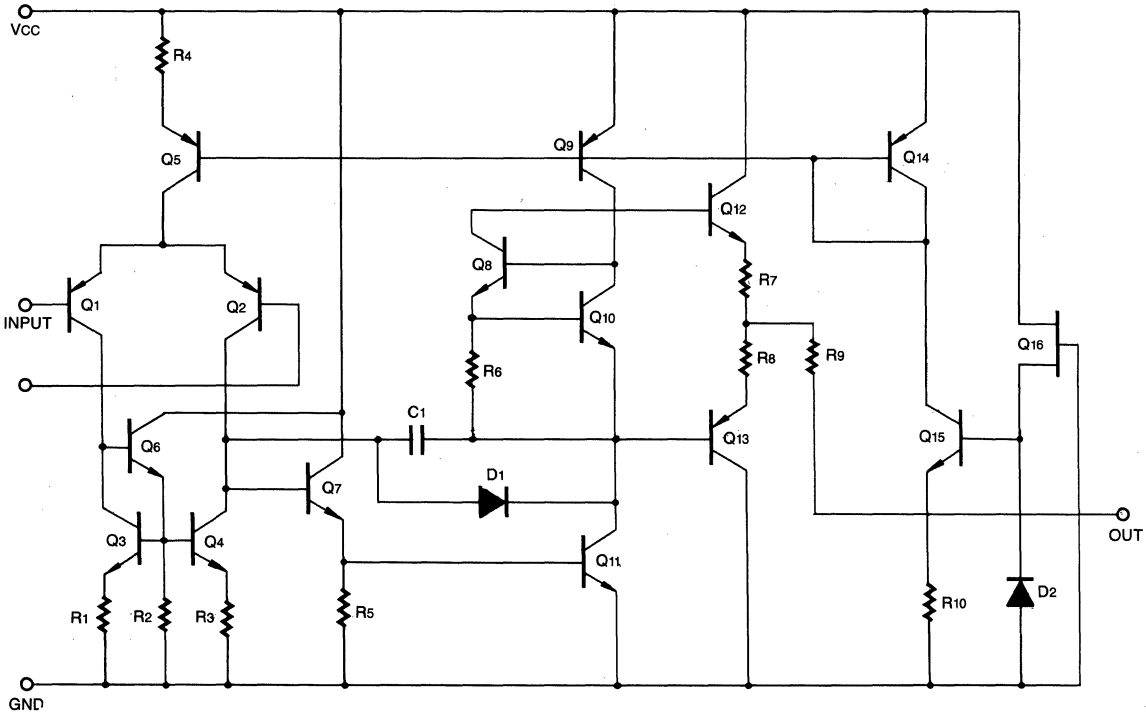


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	±18	V
Differential Input Voltage	V_{IO}	±30	V
Input Voltage	V_I	±15	V
Power Dissipation	P_D	400	mW
Operating Temperature	T_{opr}	0~70	°C
Storage Temperature	T_{stg}	−65~150	°C

ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=15V, V_{EE}=−15V)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 10k\Omega$	—	2.0	6	mV
Input Offset Current	V_{IO}		—	20	200	nA
Input Bias Current	I_B		—	80	500	nA
Input Resistance	R_I		0.3	2		MΩ
Large signal Voltage Again	A_V		20	200	—	V/mV
Output Voltage Swing	V_{OM}	$R_L \geq 10k$	±12	±14	—	V
		$R_L \geq 2k$	±10	±13	—	V
Input Voltage Range	V_{ICM}		±10	±13		V
Common Mode Rejection Ratio	CMR	$R_S \leq 10k$	70	90	—	dB
Supply Voltage Rejection Ratio	SVR	$R_S \leq 10k\Omega$	77	96	—	dB
Power Consumption	P_C			70	170	mW
Slew Rate		$R_L \geq 2k\Omega$		0.8		V/uS

BLOCK DIAGRAM

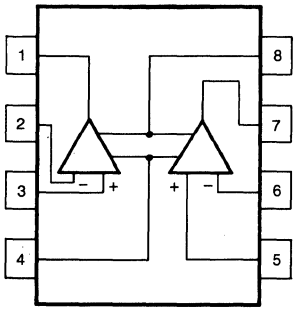


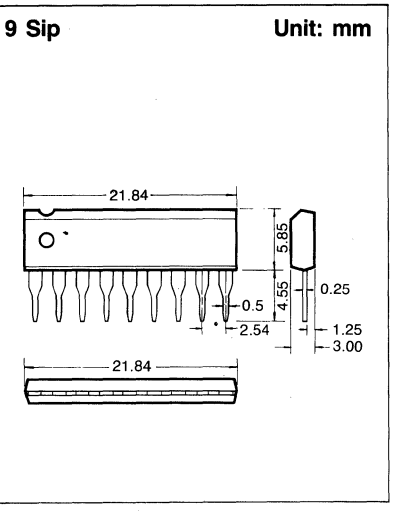
Fig. 2

PIN CONNECTIONS

PIN 1: OUT 1
PIN 2: IN 1 (−)
PIN 3: IN 1 (+)
PIN 4: V_{EE}
PIN 5: +IN 2(+)
PIN 6: −IN 2 (−)
PIN 7: OUT 2
PIN 8: V_{CC}

DUAL OPERATIONAL AMPLIFIER

The MC4558S is a monolithic integrated circuit designed for dual operational amplifier.



FUNCTIONS

- Internally frequency compensated.
- Short-circuit pretected.
- Low noise input transistors.

FEATURES

- **No frequency compensation required.**
- **No latch-up.**
- **Large common mode and differential voltage range.**
- **Parameter tracking over temperature range.**
- **Gain and phase match between amplifiers.**
- **Direct replacement for MC1458C.**

SCHEMATIC DIAGRAM

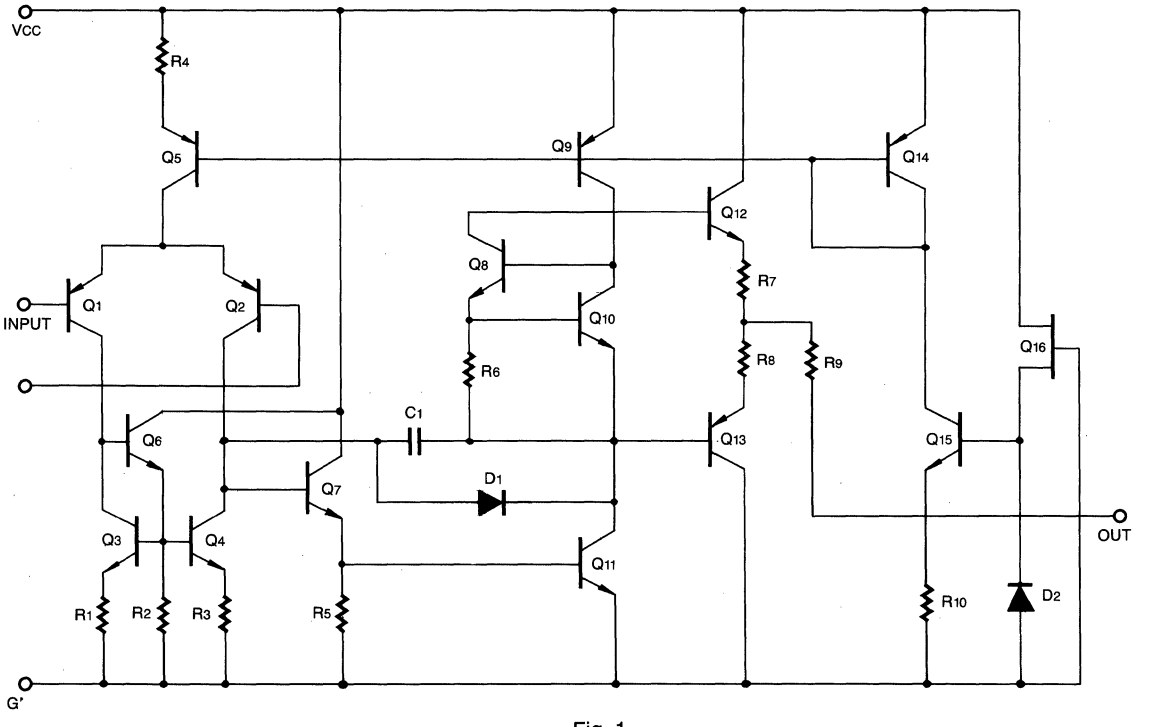


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_A =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	±18	V
Differential Input Voltage	V_{IO}	±30	V
Input Voltage	V_I	±15	V
Power Dissipation	P_D	400	mW
Operating Temperature	T_{opr}	0~70	°C
Storage Temperature	T_{stg}	−65~+150	°C

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CC} = 15V, V_{EE} = −15V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 10k$		2.0	6	mV
Input Offset Current	V_{IO}			20	200	nA
Input Bias Current	I_B			80	500	nA
Input Resistance	R_I		0.3	2		MΩ
Large Signal Voltage Gain	A_V		20	200		V/mV
Output Voltage Swing	V_{OM}	$R_L \geq 10k$	±12	±14		V
		$R_L \geq 2k$	±10	±13		V
Input Voltage Range	V_{ICM}		±10	±13		V
Common Mode Rejection Ratio	CMR	$R_S \leq 10k$	70	90		dB
Supply Voltage Rejection Ratio	SVR	$R_S \leq 10k$	77	96		dB
Power Consumption	P_C			70	240	mW
Slew Rate		$R_L \geq 2k$		0.8		V/uS

BLOCK DIAGRAM

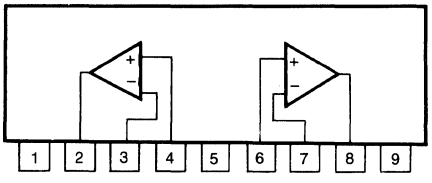
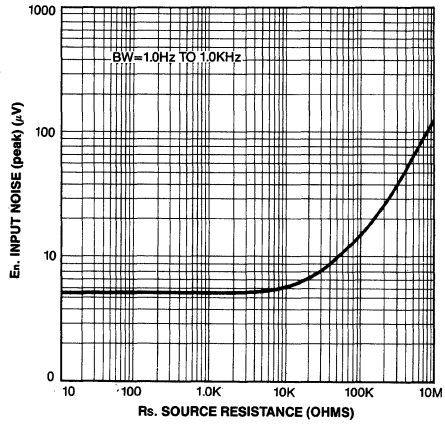


Fig. 2

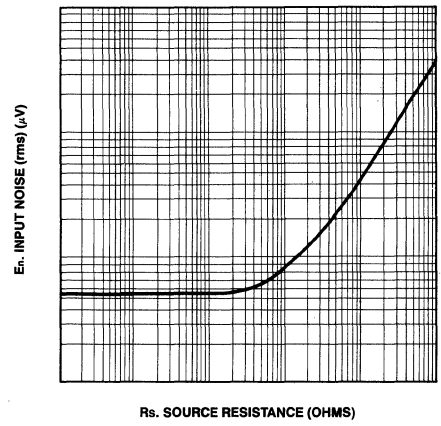
PIN CONNECTIONS

PIN 1: V_{CC}
PIN 2: OUT 1
PIN 3: IN 1 (−)
PIN 4: IN 1 (+)
PIN 5: V_{EE}
PIN 6: +IN 2(+)
PIN 7: −IN 2 (−)
PIN 8: OUT 2
PIN 9: V_{CC}

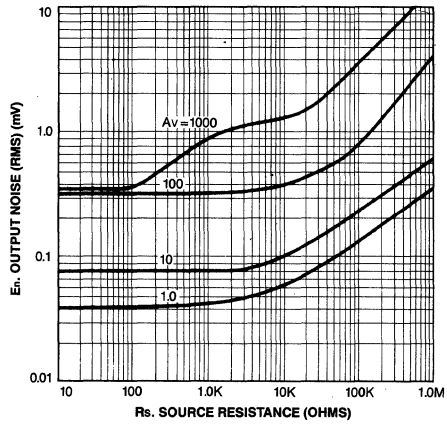
BURST NOISE VERSUS SOURCE RESISTANCE



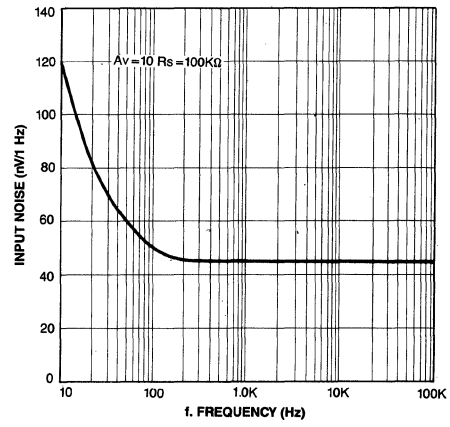
RMS NOISE VERSUS SOURCE RESISTANCE



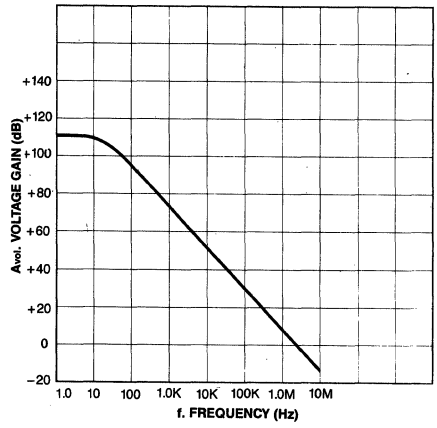
OUTPUT NOISE VERSUS SOURCE RESISTANCE



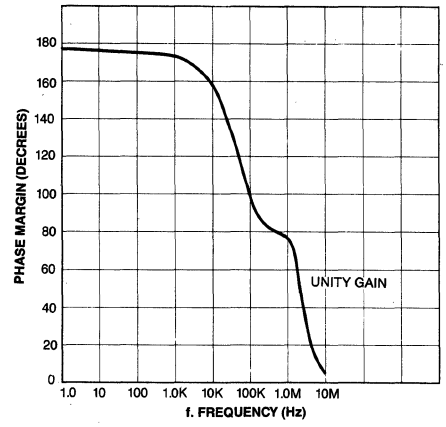
SPECTRAL NOISE DENSITY



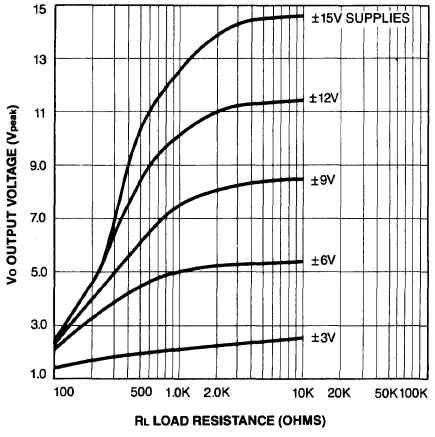
OPEN LOOP FREQUENCY RESPONSE



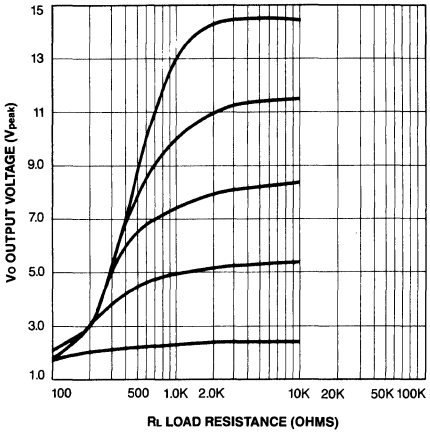
PHASE MARGIN VERSUS FREQUENCY



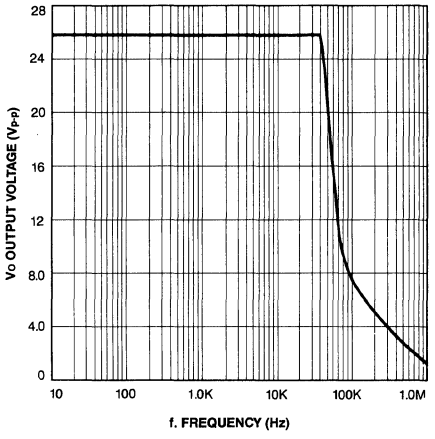
POSITIVE OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE



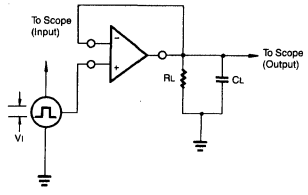
NEGATIVE OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE



POWER BANDWIDTH (LARGE SIGNAL SWING VERSUS FREQUENCY)

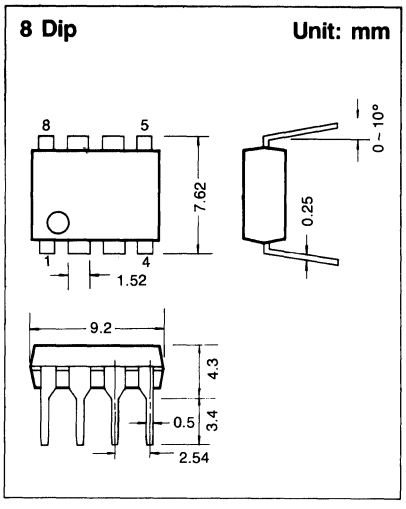


TRANSIENT RESPONSE TEST CIRCUIT



DESCRIPTION VOLTAGE COMPARATOR

The LM311 is monolithic, low input current Voltage Comparators.



FEATURE

- **Low input bias current: MAX: 205nA.**
- **Low input offset current MAX: 50nA.**
- **Differential Input Voltage ±30V.**
- **Power supply voltage single 5.0V supply to ±15V.**
- **Offset voltage null capability.**
- **Strobe capability.**

SCHEMATIC DIAGRAM

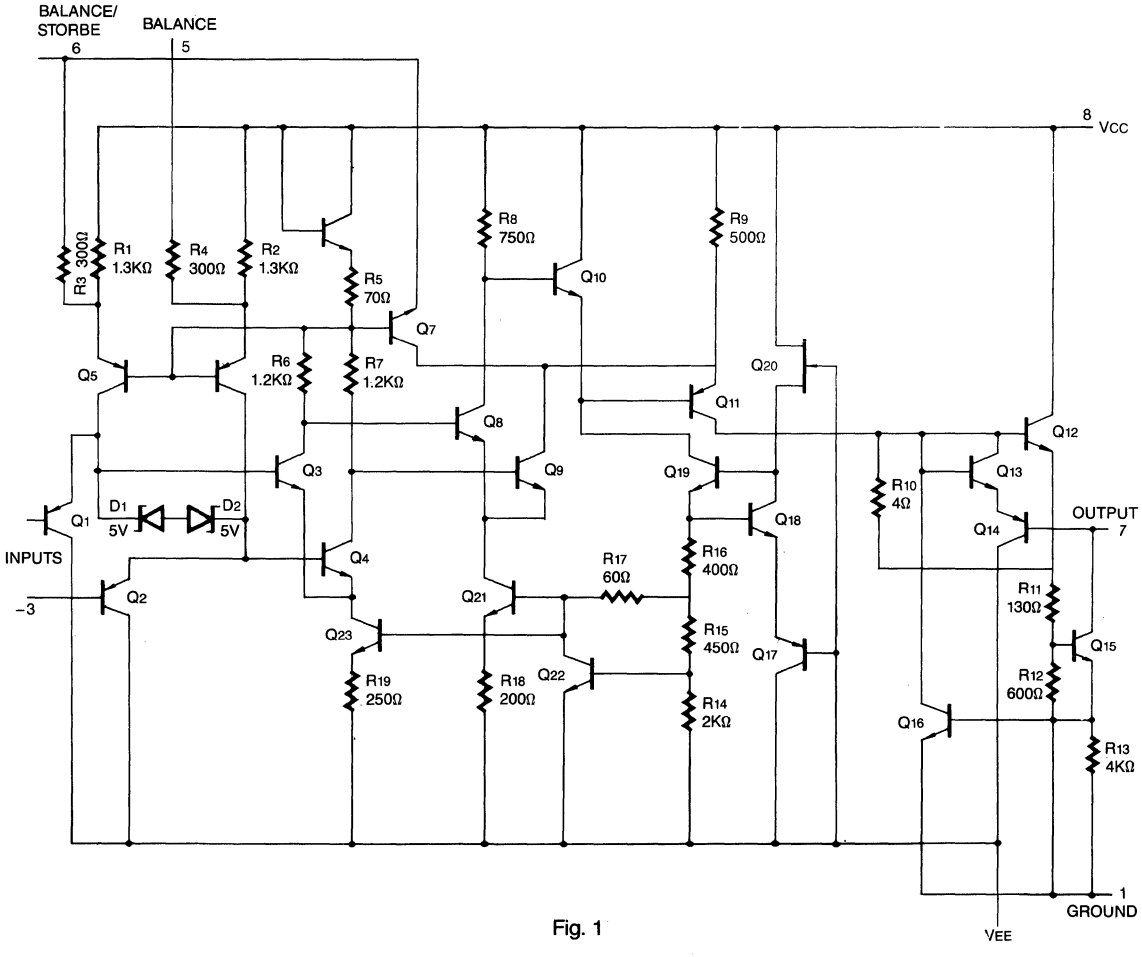


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage V+ and V− Terminals		36	V
Output to V_{EE}		40	V
Ground to V_{EE}		30	V
Differential Input Voltage		±30	V
Input Voltage (Note 1)		±15	V
Internal Power Dissipation (Note 2)		500	mW
Output Short-Circuit Duration		10	s
Operating Temperature Range		0 to +70	°C
Storage Temperature Range		−65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} =±15V, T_a =0°C to +70°C unless otherwise specified) (Note 3)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Input Offset Voltage (Note 4)	V_{IO}	T_a =25°C, $R_S \leq 50k\Omega$		2.0	7.5	mV
Input Offset Current (Note 4)	I_{IO}	T_a =25°C		6.0	50	nA
Input Bias Current	I_{IB}	T_a =25°C		100	250	nA
Voltage Gain	A_V	T_a =25°C	40	200		V/mV
Response Time (Note 5)	R_S	T_a =25°C		200		ns
Saturation Voltage	V_{SAT}	$V_{IN} \leq -10mV$, I_{OUT} =50mA T_a =25°C		0.75	1.5	V
Strobe On Current	I_S	T_a =25°C		3.0		mA
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, V_{OUT} =35V T_a =25°C		0.2	50	nA
Input Offset Voltage (Note 4)	V_{IO}	$R_S \leq 50k\Omega$			10	mV
Input Offset Current (Note 4)	I_{IO}				70	nA
Input Bias Current	I_{CB}				300	nA
Input Voltage Range	V_{COM}			±14		V
Saturation Voltage	V_{SAT}	V+ ≥4.5V, V− =0 $V_{IN} \leq -10mV$, $I_{SINK} \leq 8mA$		0.23	0.4	V
Positive Supply Current	I_{CC}	T_a =25°C		5.1	7.5	mA
Negative Supply Current	$-I_{CC}$	T_a =25°C		4.1	5.0	mA

Notes

3. The offset Voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the cutput within a voit of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.

ALLICATION EXAMPLE
(Switch Power Amplifier)

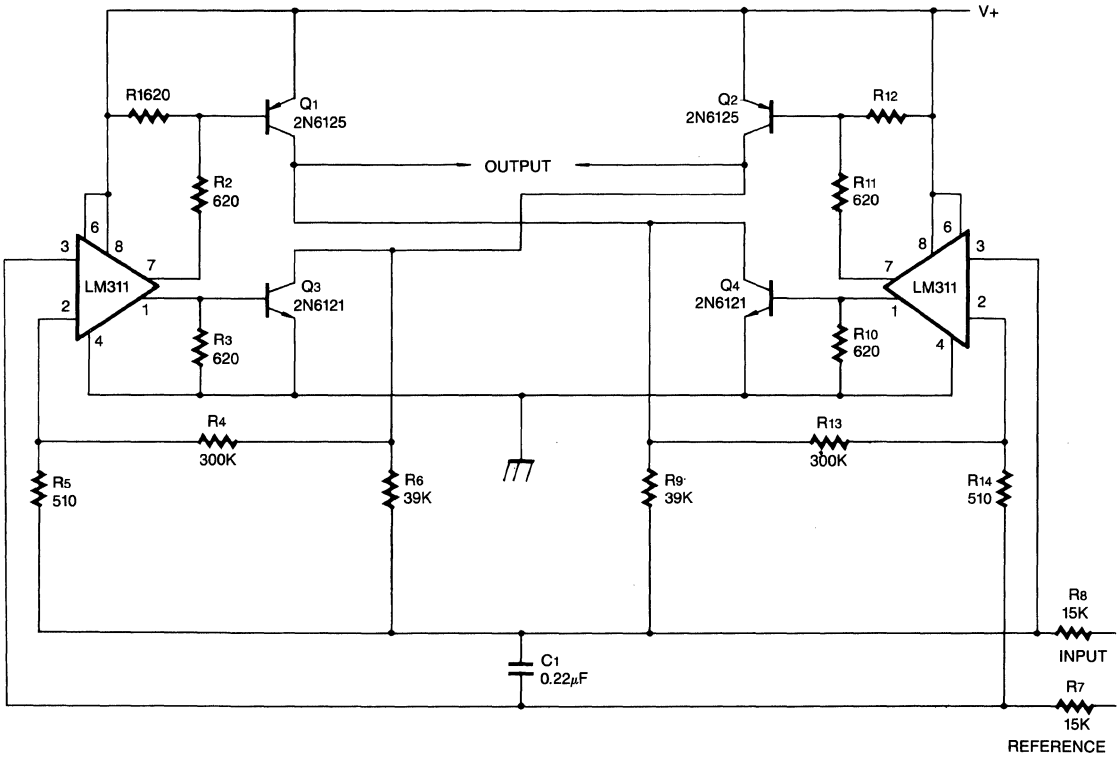
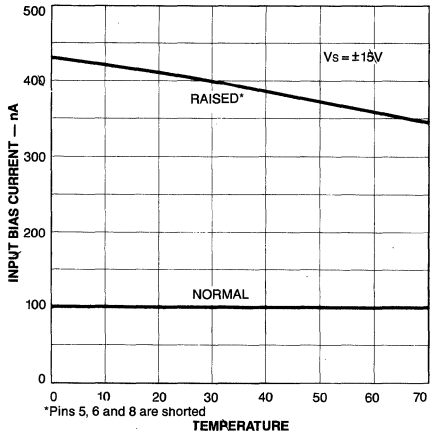
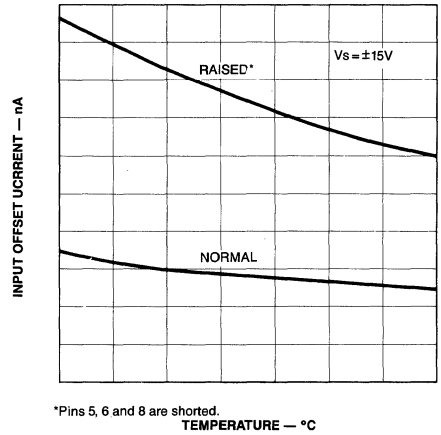


Fig. 2

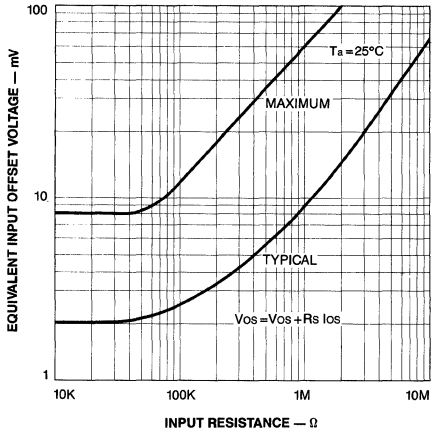
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



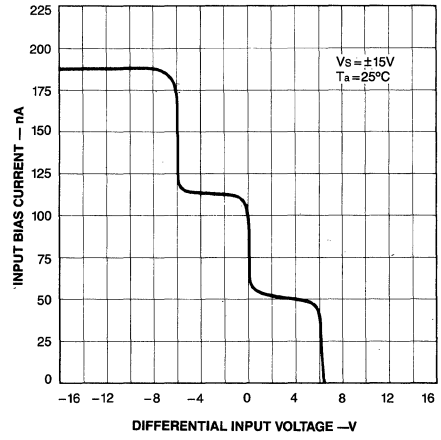
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



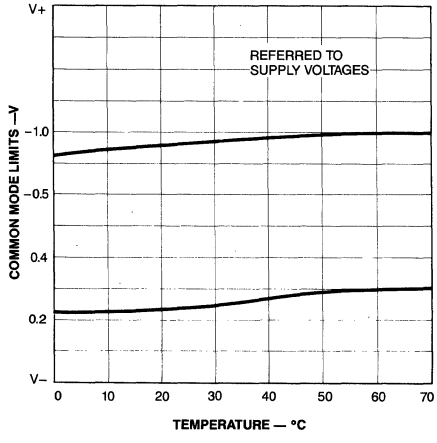
OFFSET VOLTAGE AS A FUNCTION OF INPUT RESISTANCE



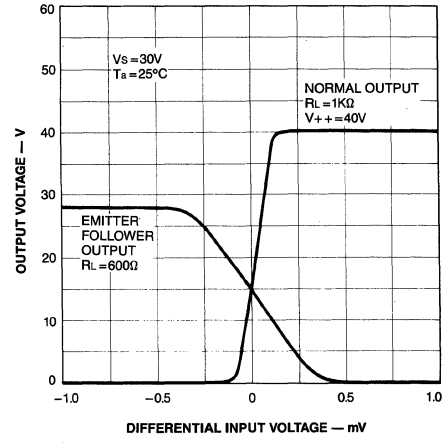
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



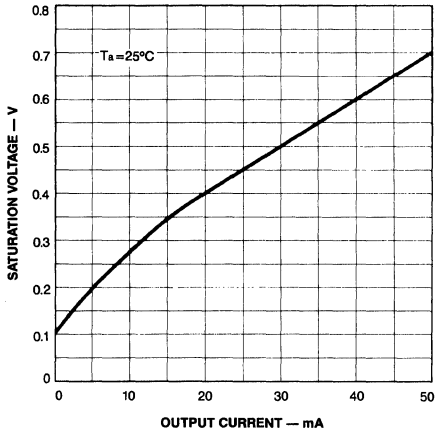
COMMON MODE LIMITS AS A FUNCTION OF TEMPERATURE



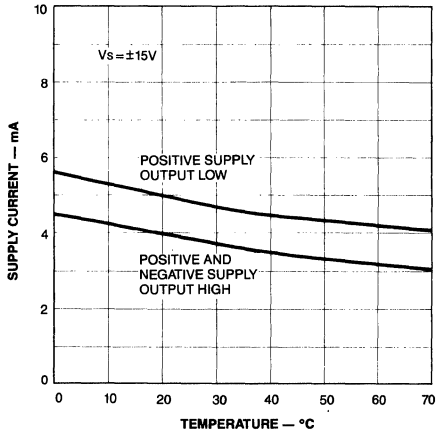
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



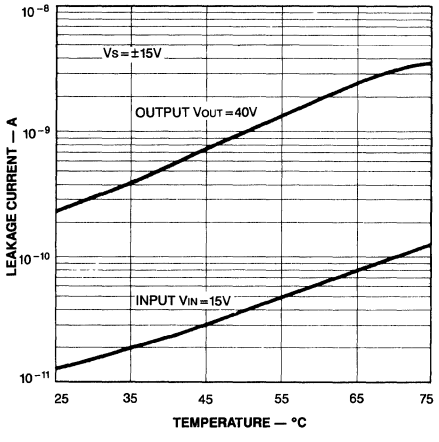
SATURATION VOLTAGE AS A FUNCTION OF CURRENT



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



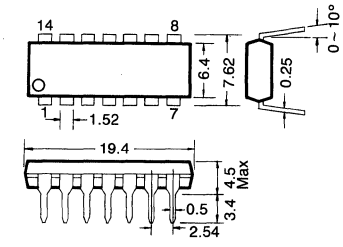
LEAKAGE CURRENTS AS A FUNCTION OF TEMPERATURE



QUAD DIFFERENTIAL COMPARATORS

The LM339/LM339A series consists of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages.

14 Dip Unit: mm



FEATURES

- **Single supply or dual supplies**
- **Wide range of supply voltages 2~36V**
- **Low supply current drain 800μA Typ.**
- **Open collector outputs for wired and connectors**
- **Low input bias current 25nA Typ.**
- **Low input offset current 5nA Typ.**
- **Low input offset voltage 2mV Typ.**
- **Common mode input voltage range includes ground.**
- **Low output saturation voltage**
- **Output compatible with TTL, DTL and MOS**

SCHEMATIC DIGRAM

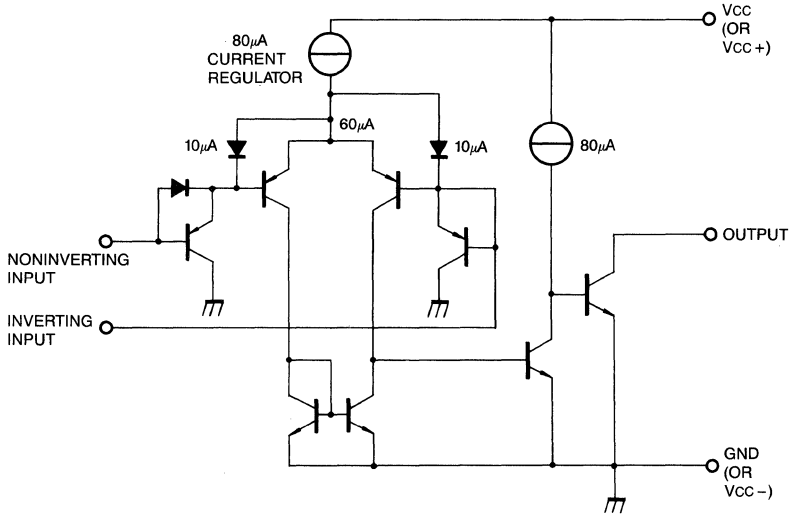


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	36	V
Differential Input Voltage	V_{IN}	±36	V
Output Current	I_O	20	mA
Power Dissipation	P_d	1.0	W
Operating Temeprature	T_{opr}	0~+70	°C
Storage Temperature	T_{stg}	−65~+150	°C

BLOACK DIAGRAM

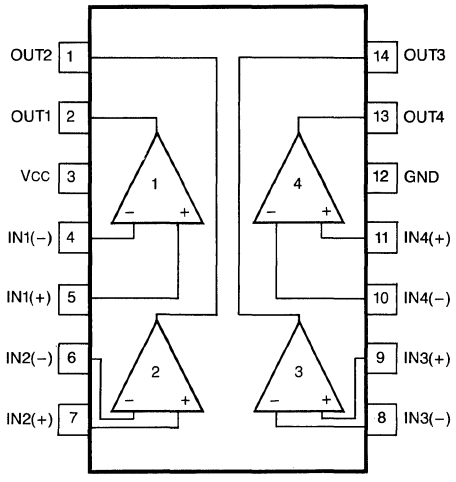


Fig. 2

ELECTRICAL CHARACTERISTICS

(VCC = 5V, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM339A			Unit
				Min	Typ	Max	
Supply Current	I_{CC}	No Load			0.8	2	mA
Input Offset Voltage	V_{IO}	V_{CC} = 5 ~ 30V V_O = 1.4V	25°C		±1	±2	mV
			Full range			±4	
Input Offset Current	I_{IO}	V_O = 1.4V	25°C		±5	±50	nA
			Full range			±150	
Input Bias Current	I_{IB}		25°C		25	250	nA
			Full range			400	
Common Mode Input Voltage Range	V_{ICR}	V_{CC} = 2 ~ 36V	25°C	0		V_{CC}-1.5	V
			Full range	0		V_{CC}-2	
Large Signal Voltage Gain	A_{VO}	V_{CC} = 15V R_L = 15KΩ		94	106		dB
High Level Output Current	I_{OH}	V_{ID} = 1V	V_{OH} = 50, 25°C		0.1		nA
			V_{OH} = 30V Full range			1	
Low Level Output Voltage	V_{OL}	V_{ID} = −1V I_{OL} = 4mA	25°C		150	400	mV
			Full range			700	
Low Level Output Current	I_{OL}	V_{ID} = −1V V_{OL} = 1.5V		6	16		mA

ELECTRICAL CHARACTERISTICS

(VCC =5V, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM339			Unit
				Min	Typ	Max	
Supply Current	I_{CC}	No Load			0.8	2	mA
Input Offset Voltage	V_{IO}	V_{CC} =5 ~ 30V V_O =1.4V	25°C		±2	±5	mV
			Full range			±9	
Input Offset Current	I_{IO}	V_O =1.4V	25°C		±5	±50	nA
			Full range			±150	
Input Bias Current	I_{IB}		25°C		25	250	nA
			Full range			400	
Common Mode Input Voltage Range	V_{ICR}	V_{CC} =2 ~ 36V	25°C	0		V_{CC}-1.5	V
			Full range	0		V_{CC}-2	
Large Signal Voltage Gain	A_{VO}	V_{CC} =15V R_L =15KΩ			106		dB
High Level Output Current	I_{OH}	V_{ID} = 1V	V_{OH} = 50, 25°C		0.1		nA
			V_{OH} =30V Full range			1	
Low Level Output Voltage	V_{OL}	V_{ID} = −1V I_{OL} =4mA	25°C		150	400	mV
			Full range			700	
Low Level Output Current	I_{OL}	V_{ID} = −1V V_{OL} =1.5V		6	16		mA

Driving C/MOS

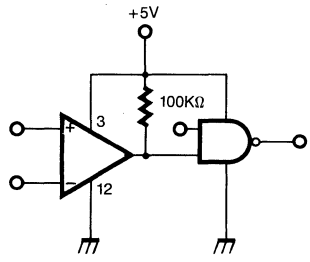


Fig. 6

Driving TTL

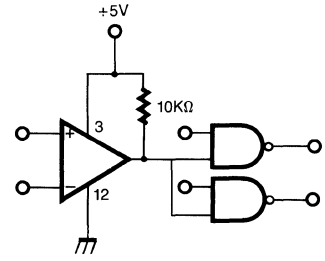


Fig. 7

AND gate

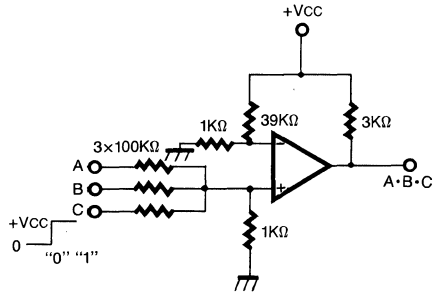


Fig. 8

OR gate

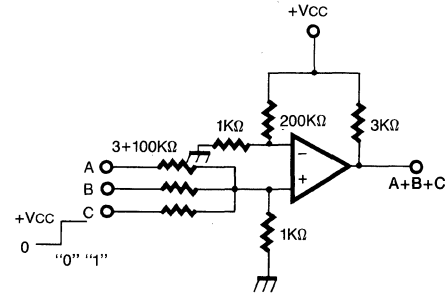


Fig. 9

Large fan-in AND gate

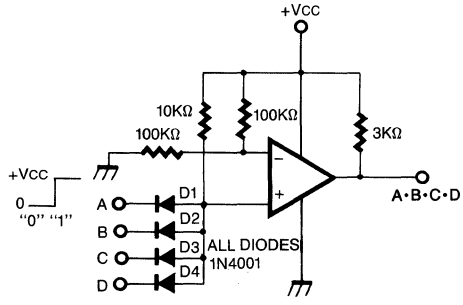


Fig. 10

Squarewave oscillator

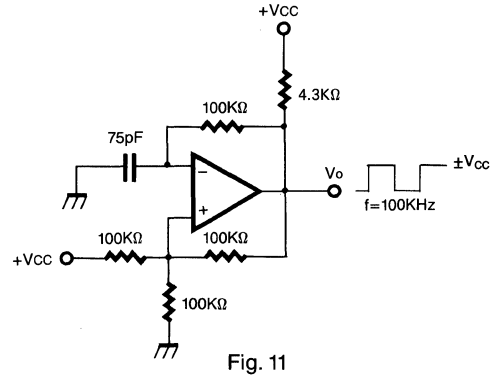


Fig. 11

SWITCHING CHARACTERISTICS

(T_a=25°C, V_{CC}=5V)

Characteristic	Symbol	Test Contions		Min.	Typ.	Max.	Unit
Response Time	T_r	R_L=5.1KΩ C_L=15pF	100mV input step with 5mV overdrive TTL level input		1.3		μS
					0.3		

APPLICATION INFORMATION

The LM339 includes four high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output is inadvertently allowed to capacitively couple to the inputs via stray capacitance. That occurs during the output voltage transitions, when the comparator changes state.

To minimize this problem, PC board layout should be designed to reduce stray input output coupling; reducing the input resistors to less than 10KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.

It is good design practice to ground all unused pins.

The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than −0.3V should not be used: an input clamping diode can be used as protection.

The output LM339 is the uncommitted collector of a NPN transistor with grounded emitter. This allows the device to be used like any open-collector gate providing the OR-wide facility.

The output sink current capability is approximately 16 mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltage will rise very rapidly.

Under this limit, the output saturation voltage is limited by the approximatively 60Ω r_{sat} of the output transistor.

Basic comparator

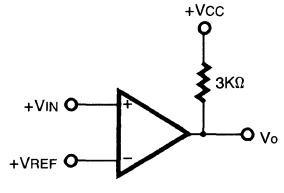


Fig. 3

Non-inverting comparator with Hysteresis

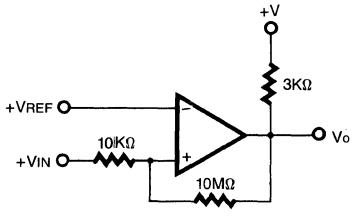


Fig. 4

Inverting comparator with Hysteresis

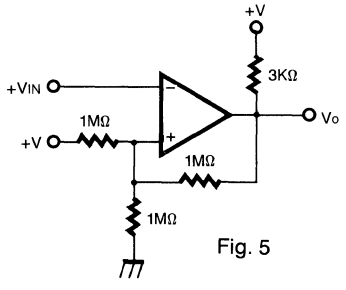


Fig. 5

ORing the outputs

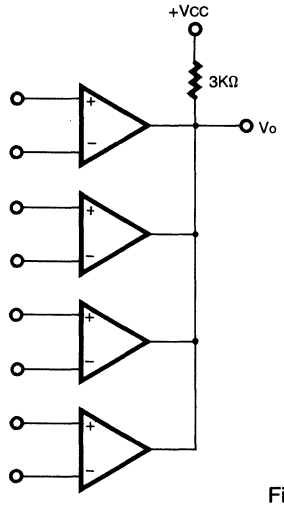


Fig. 12

Peak audio level display

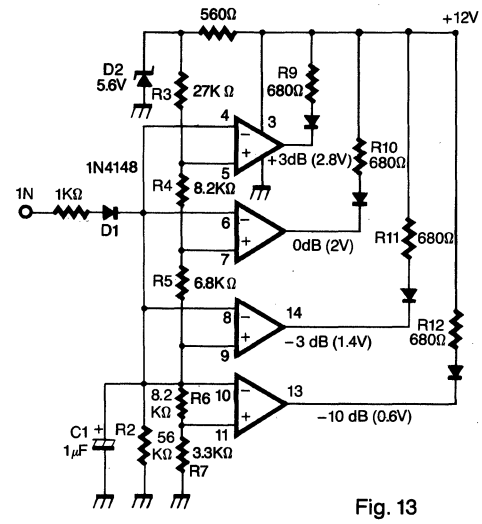


Fig. 13

Zero crossing detector (single supply)

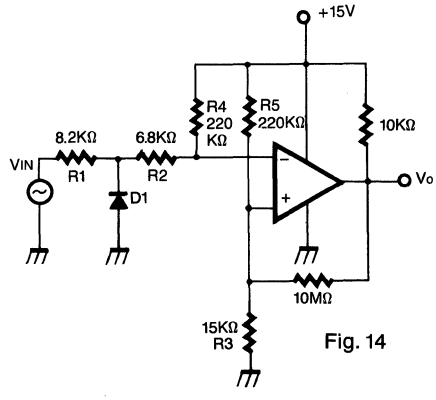


Fig. 14

Zero crossing detector (split supplies)

$V_{INmin} \approx 0.4V$ peak for 1% phase distortion ($\Delta\theta$)

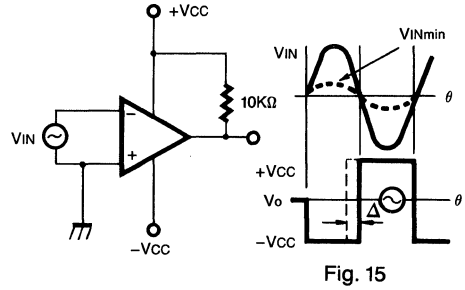


Fig. 15

D1 prevents input from going negative by more than 0.6V:

$R1+R2=R3$

$R3 \leqslant R5/10$ for smaller error in zero crossing

Fig. 16 — Supply current V_S supply voltage

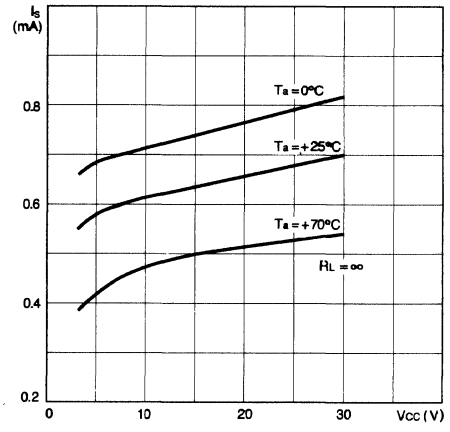


Fig. 17 — Input current V_S supply voltage

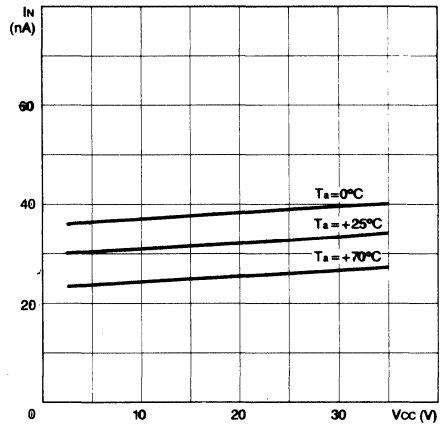


Fig. 18 — Output saturation voltage

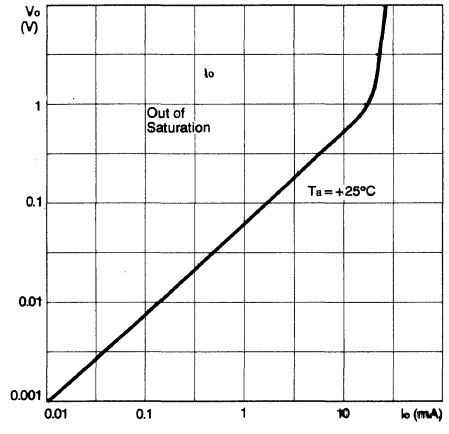


Fig. 19 — Response time

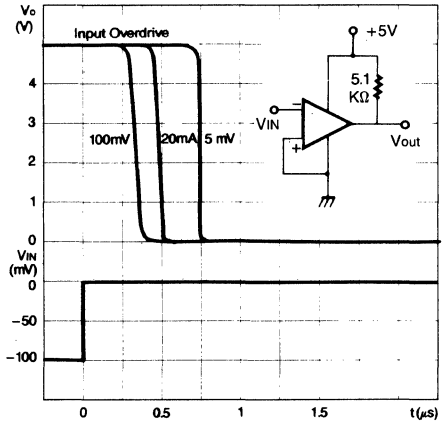
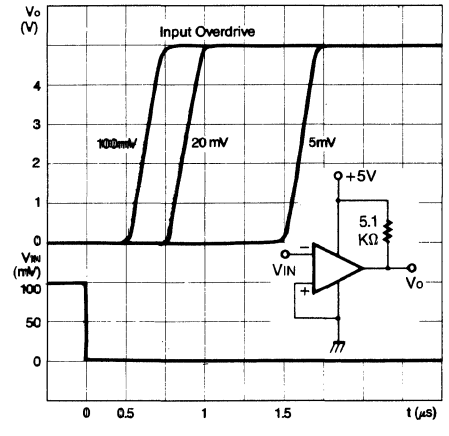
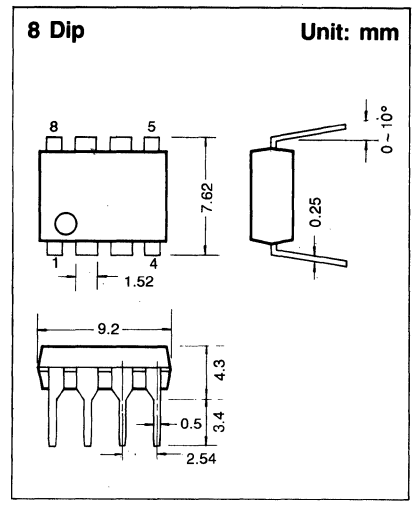


Fig. 20 — Response time



DUAL DIFFERENTIAL COMPARATOR

The LM393/LM393A consists of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages.



FEATURES

- **Single Supply Operation +2.0V to +36V**
- **Dual Supply Operation ±1.0V to ±18V**
- **Allow Comparison of Voltages Near Ground Potential**
- **Low Current Drain 400μA Typ**
- **Compatible with all Forms of Logic**
- **Low Input Bias Current 25nA Typ**
- **Low Input Offset Current ±5nA Typ**
- **Low Offset Voltage ±2mV**

SCHEMATIC DIAGRAM

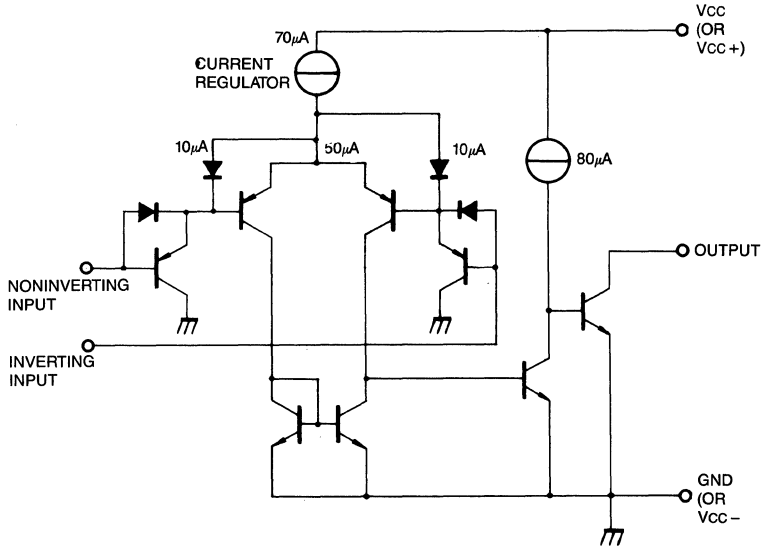


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	±36	V
Differential Input Voltage	V_{IN}	36	V
Output Current	I_O	20	mA
Power Dissipation	P_d	650	mW
Operating Temperature	T_{opr}	0 ~ 70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

BLOCK DIAGRAM

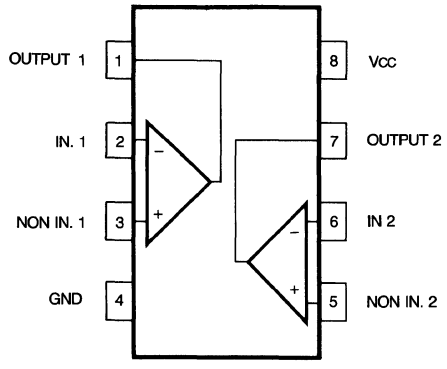


Fig. 2

ELECTRICAL CHARACTERISTICS

(V_{CC} =5V, T_a =25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM 393 Min	LM 393 Typ	LM 393 Max	Unit
Input Offset Voltage	V_{os}	At out. switch point $V_o \cong 1.4$; R_g =0			±2	±5	mV
		V_{REF} =1.4V	0°C ≤ T_a ≤ 70°C			±9	
Input Bias Current (1)	I_b	Output in linear range			25	250	nA
			0°C ≤ T_a ≤ 70°C			400	
Input Offset Current	I_{os}	≅			±5	±50	nA
			0°C ≤ T_a ≤ 70°C			±150	
Input Common-Mode Voltage Range (2)				0		V_{CC} −1.5	V
			0°C ≤ T_a ≤ 70°C	0		V_{CC} −2	
Supply Current	I_s	R_L = ∞			0.4	1	mA
Supply Current	I_s	V_{cc} =30V, R_L = ∞				2.5	mA
Voltage Gain	A_v	R_L ≥ 15KΩ, V_{CC} =15			106		dB
Large Signal Response Time		V_{IN} =TTL logic swing; V_{REF} =+1.4V; R_L =5.1KΩ V_{RL} =5V			300		ns
Response Time (3)	T_r	V_{RL} =5V; R_L =5.1V			1.3		μs
Output Sink Current	I_o	$V_{IN(-)}$ ≥ 1V; $V_{IN(+)}$ =0V; V_o ≤ 1.5V		6	16		mA
Output Saturation	V_{sat}	$V_{IN(-)}$ ≤ 1V $V_{IN(+)}$ =0V I_{sink} ≤ 4mA			150	400	mV
			0°C ≤ T_a ≤ 70°C			700	
Output Leakage	I_o leak	$V_{IN(+)}$ ≥ 1V $V_{IN(-)}$ =0V			0.1		μA
			0°C ≤ T_a ≤ 70°C			1	
Differential Input Voltage	V_{ID}	All V_{IN} ≥ 0V (or—V_{CC} if split supply is used)	0°C ≤ T_a ≤ 70°C			+ V_{CC}	V

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This conditions is not destructive providing the input current is limited to less than 50mA

(3) The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300 nsec can be obtained.

ELECTRICAL CHARACTERISTICS

(V_{CC}=5V, T_a=25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM 393A			Unit
				Min	Typ	Max	
Input Offset Voltage	V_{os}	At out. switch point $V_o \cong 1.4$; R_g=0			±1	±2	mV
		V_{REF}=1.4V	0°C≤T_a≤70°C			±4	
Input Bias Current (1)	I_b	Output in linear range			25	250	nA
			0°C≤T_a≤70°C			400	
Input Offset Current	I_{os}				±5	±50	nA
			0°C≤T_a≤70°C			±150	
Input Common-Mode Voltage Range (2)				0		V_{CC} – 1.5	V
			0°C≤T_a≤70°C	0		V_{CC} – 2	
Supply Current	I_s	R_L=			0.4	1	mA
Supply Current	I_s	V_{cc}=30V, R_L=				2.5	mA
Voltage Gain	G_V	R_L≥15KΩ, V_{CC}=15		94	106		dB
Large Signal Response Time		V_{IN}=TTL logic swing; V_{REF}=+1.4V; R_L=5.1KΩ V_{RL}=5V			300		ns
Response Time (3)	T_r	V_{RL}5V; R_L=5.1V			1.3		μs
Output Sink Current	I_o	$V_{IN(-)}$≥1V; $V_{IN(+)}$=0V; V_o≤1.5V		6	16		mA
Output Saturation	V_{sat}	$V_{IN(-)}$≤1V $V_{IN(+)}$=0V I_{sink}≤4mA			150	400	mV
			0°C≤T_a≤70°C			700	
Output Leakage	I_o leak	$V_{IN(+)}$≥1V $V_{IN(-)}$=0V	V_O=5V		0.1		μA
			0°C≤T_a≤70°C			1	
Differential Input Voltage	V_{ID}	All V_{IN}≥0V (or—V_{CC} if split supply is used)	0°C≤T_a≤70°C			+V_{CC}	V

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This conditions is not destructive providing the input current is limited to less than 50mA

(3) The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300 nsec can be obtained.

APPLICATION INFORMATION

The LM393 includes two high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output is inadvertently allowed to capacitively couple to the inputs via stray capacitance. That occurs during the output voltage transitions, when the comparator changes state.

To minimize this problem, PC board layout should be designed to reduce stray input-output coupling, reducing the input resistors to less than 10KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.

If is good design practice to ground all unused pins.

The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than −0.3V should not used: an input clamping diode can be used as protection.

The output of the LM393 is the uncommitted collector of a NPN transistor with grounded emitter. The allows the device to be used like any open-collector gate providing the OR-wide facility.

The output sink current capability is approximately 16mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltate will rise very rapidly.
Under this limit, the output saturation voltage is limited by the approximatively 60Ω r_{sat} of the output transistor.

Basic comparator

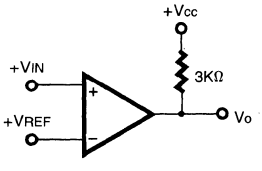


Fig. 3

Non-inverting comparator with Hysteresis

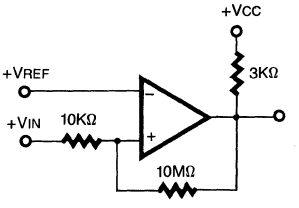


Fig. 4

Inverting comparator with Hysteresis

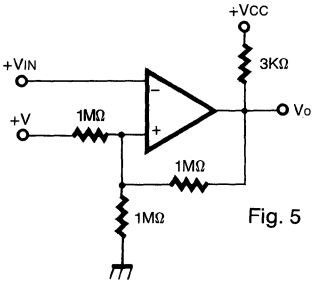


Fig. 5

Driving C-MOS

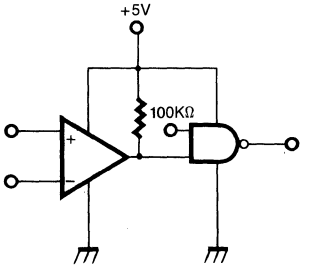


Fig. 6

Driving TTL

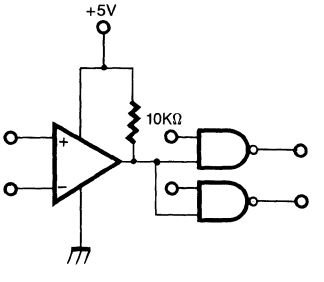


Fig. 7

APPLICATION INFORMATION (continued)

AND gate

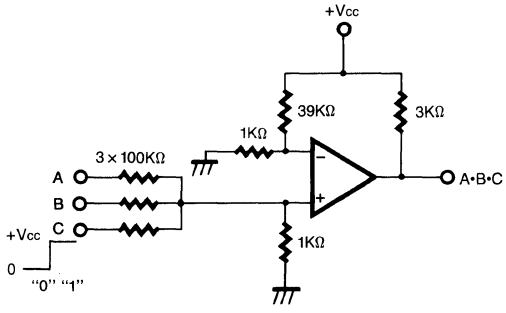


Fig. 8

OR gate

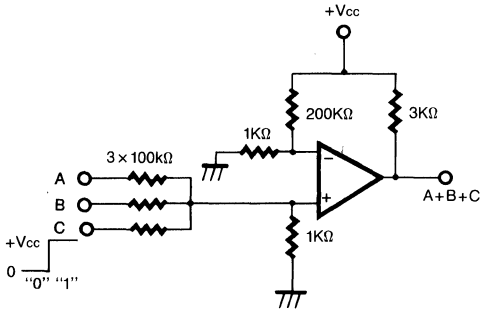


Fig. 9

Large fan-in AND gate

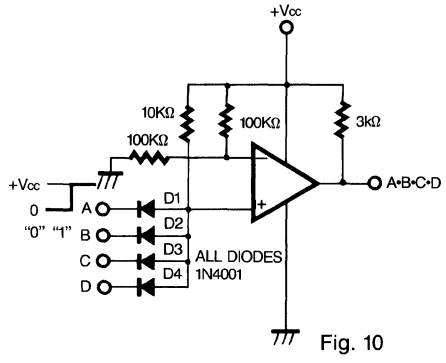


Fig. 10

Squarewave oscillator

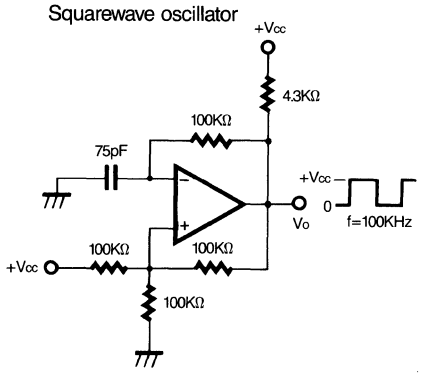


Fig. 11

Pulse generator

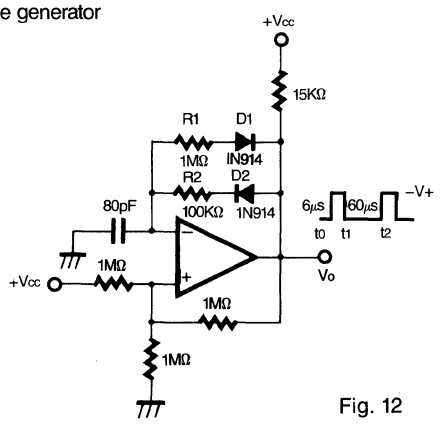


Fig. 12

One-shot multivibrator

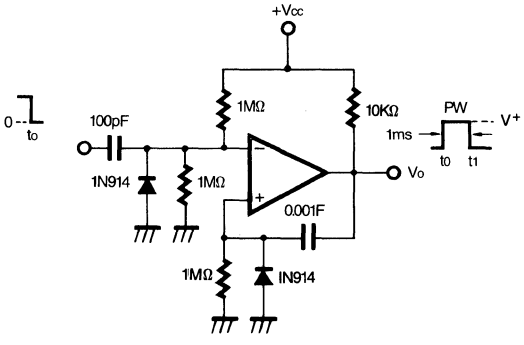
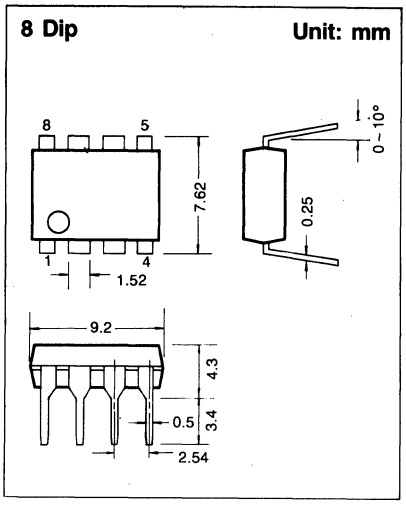


Fig. 13

TIMER

The NE555C is a monolithic integrated circuit and high stable device for generating accurate time delay or oscillation.



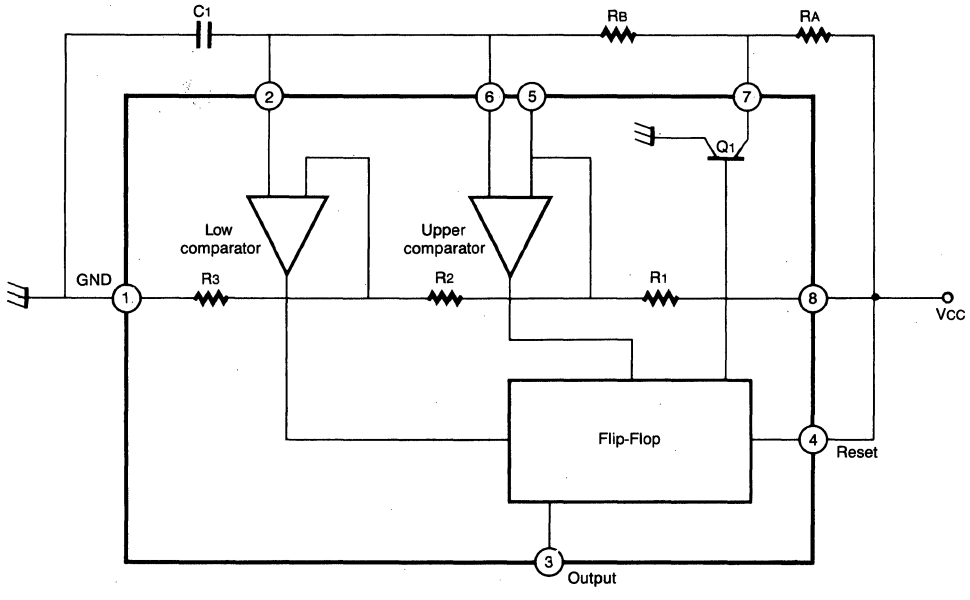
FEATURES

- **Turn off time less than 2μs**
- **Maximum operating frequency greater than 500KHz**
- **Timing from microsecond to hours**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **Temperature stability of 0.005% per °C**

APPLICATIONS

- Precision timing
- Time delay generation
- Pulse generation
- Pulse position modulation
- Sequential timing
- Missing pulse detector

APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_d	600	mW
Lead Temperature (soldering 10 sec)	T_{lead}	300	°C
Operating Temperature	Topr	0 ~ +70	°C
Storage Temperature	Tstg	−65 ~ +150	°C

DC ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=5 ~ 15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
Supply Current *1(low stable)	I_{CC}	V_{CC}=5V, R_L=		3	6	mA
		V_{CC}=15V, R_L=		10	15	mA
Timing Error (Monsotable)	MT_1					
*2Initial Accurary		R_A=1kΩ to 100kΩ		1.0	3.0	%
Drift with Temperature		C=0.1μF		50		ppm/°C
Drift with Supply Voltage				0.1	0.5	%/V
Timing Error (astable)	MT_2					
*2Initial Accurary		R_A=1k to 100kΩ		2.25		%
Drift with Temperature		C=0.1μF		150		ppm/°C
Drift with Supply Voltage				0.3		%/V
Control Voltage Level	V_C	V_{CC}=15V	9.0	10.0	11.0	V
		V_{CC}=5V	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	V_{CC}=15V		10.0		V
		V_{CC}=5V		3.33		V
*3Threshold Current	I_{TH}			0.1	0.25	μA
Trigger Voltage	V_T	V_{CC}=5	1.1	1.67	2.2	V
Trigger Current	I_T	V_T=0V		0.5	2.0	μA
Reset Voltage	V_R		0.4	0.7	1.0	V
Reset Current	I_R			0.1	0.4	mA

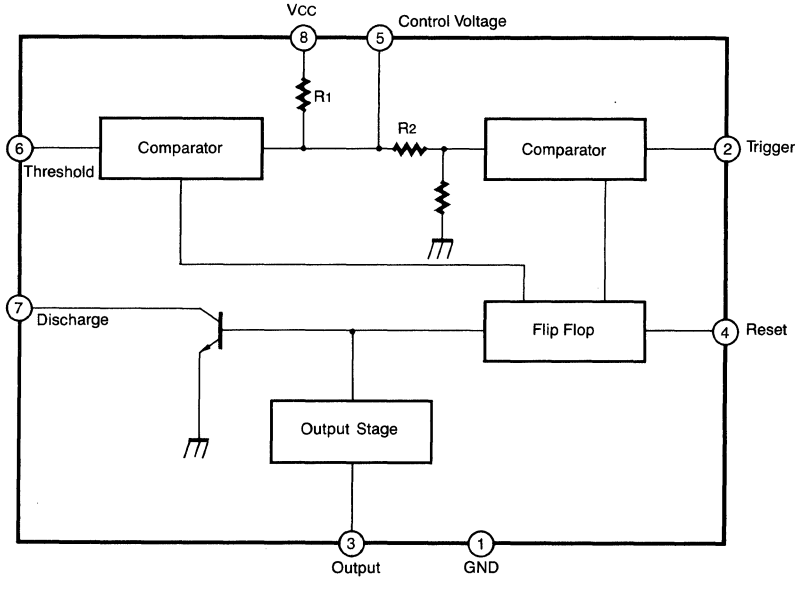
DC ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=5~15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage (low)	V_{OL}	V_{CC}=15V I_{sink}=10mA I_{sink}=50mA		0.1 0.4	0.25 0.75	V V
		V_{CC}= 5V I_{sink}=5mA		0.25	0.35	V
Output Voltage (high)	V_{OH}	V_{CC}=15V I_{source}=200mA I_{source}=100mA	 12.75	12.5 13.3		V V
		V_{CC}=5V I_{source}=100mA	2.75	3.3		V
Rise Time of Output	T_R			100		nsec
Fall Time of Output	T_F			100		nsec
Discharge Leakage Current				20	100	nA

Notes:

1. Supply current when output high typically 1mA less.
2. Tested at V_{CC}=5.0V and V_{CC}=15V
3. This will determine the maximum value of R_A+R_B, for 15V operation, the max total R=20MΩ, and for 5V operation the max total R=6.7MΩ.



APPLICATION NOTE

The application circuit shows astable mode.
The pin 6 (threshold) tied to the pin 2 (trigger) and pin 4 (reset) tied to V_{CC} (pin 8).
The external capacitor C_1 of pin 6 and pin 2 charges through R_A, R_B and discharges through R_B only.
In the internal circuit of the NE555C one input of upper comparator is the 2/3 V_{CC} ($^*R_1 = R_2 = R_3$), another input of it connected pin 6.
As soon as charging C_1 is higher than 2/3 V_{CC}, discharge transistor Q_1 turn on and C_1 discharges to collector of transistor Q_1.
Therefore flip-flop circuit is reset and output is low.
One input of lower comparator is the 1/3 V_{CC}, discharge transistor Q_1 turn off and C_1 charges through R_A and R_B.
Therefore flip-flop circuit is set and output is high.
So to say, when C_1 charges through R_A and R_B output is high and when C_1 discharges through R_B OUTPUT IS HIGH.
The charge time (output is high) T_1 is 0.693 $(R_A + R_B)$ C_1 and the discharge time (output is low) T_2 is 0.693 $(R_B\ C_1)$.

$$\left(l_n \frac{V_{CC}\text{-}1/3V_{CC}}{V_{CC}\text{-}2/3V_{CC}} = 0.693\right)$$

Thus the total period time T is given by
$T = T_1 + T_2 = 0.693\ (R_A + 2R_B).\ C_1$.
Then the frequency of astable mode is given by

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C_1}$$

The duty cycle is given by

$$D.C = \frac{T_2}{T_1} = \frac{R_B}{R_A + 2R_B}$$

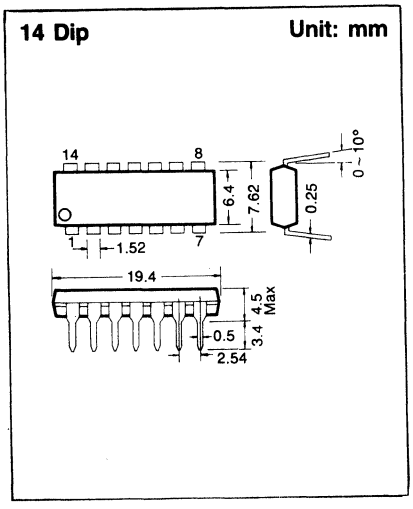
If you make use of the NE556C you can make two astable mode.
If you want another application note, request information on our timer IC application circuit designer.

DUAL TIMER

The NE556C dual monolithic timing circuit is a highly stable controller capable of producing accruate time delays or oscillaiton.

The NE556 is a dual NE555C. Timing is provided an external resistor and capacitor for each timing function.
The two times operate independently of each other sharing only V_{CC} and ground.

The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

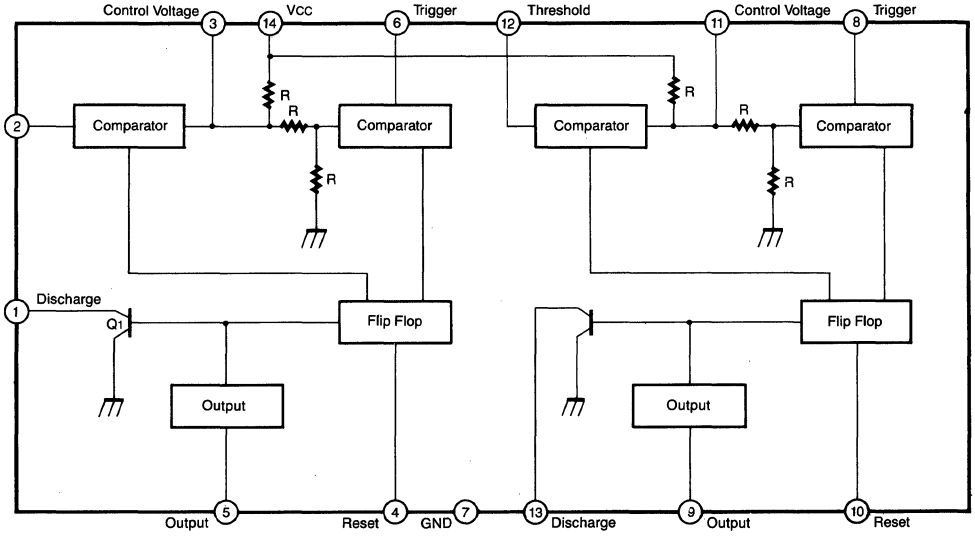


FEATURES

- **Direct replacement for NE556**
- **Replace two NE555C timers**
- **Operates in both astable and monostable modes**
- **High output current**
- **TTL compatible**
- **Timing from microsecond to hours**
- **Adjustable duty cycle**
- **Temperature stability of 0.05% per °C**

APPLICATIONS

- Precision timing
- Pulse shaping
- Pulse width modulation
- Frequency division
- Traffic light control
- Sequential timing
- Pulse generator
- Time delay generator
- Touch tone encoder
- Tone burst generator



ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	±16	V
Power Dissipation	P_d	6.00	mW
Lead Temperature (solding, 10 sec)	Tlead	+300	°C
Operating Temperature	Topr	0~+70	°C
Storage Temperature	Tstg	−65~+150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V to +15V, unless otherwise specified)

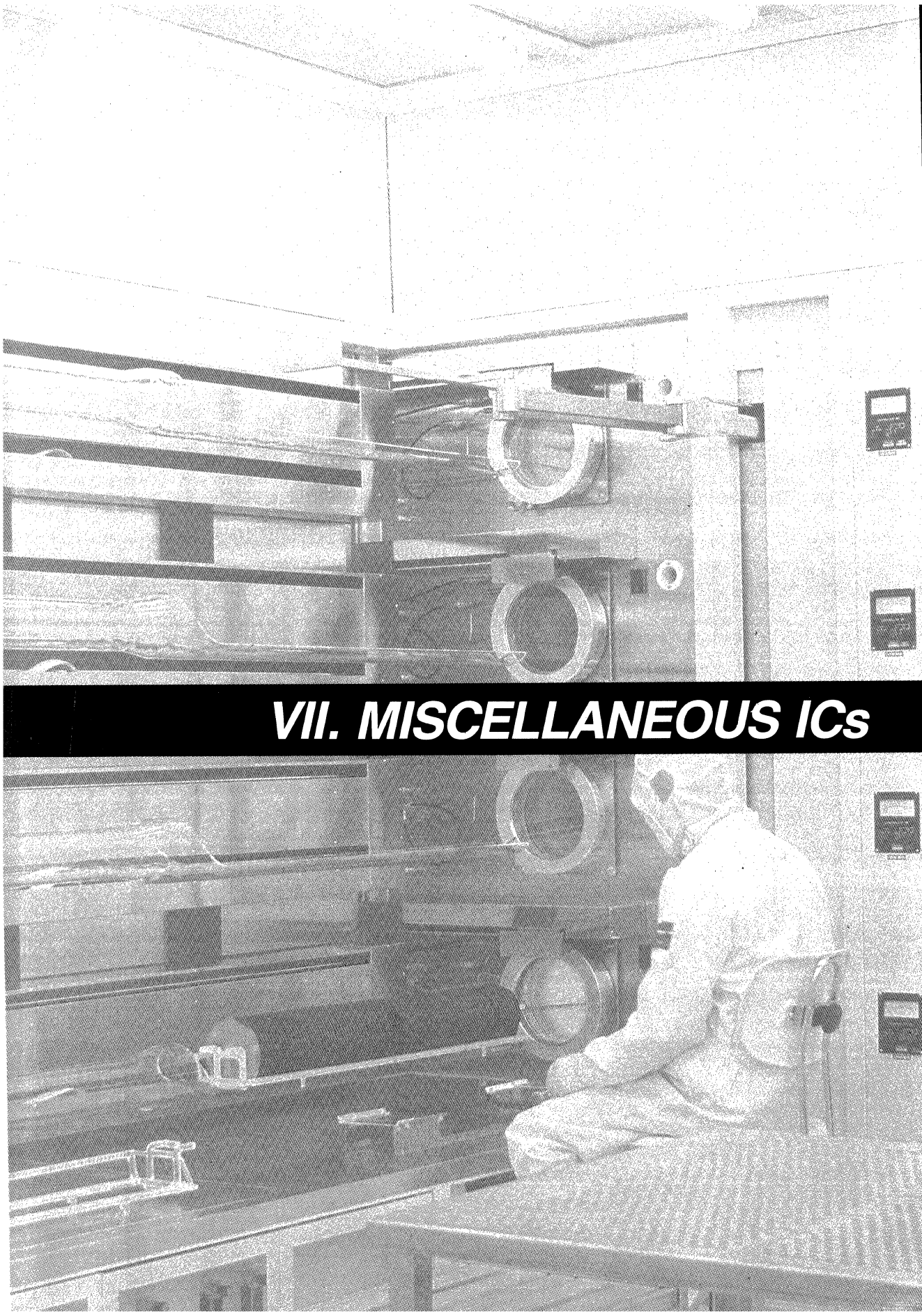
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
Supply Current[1] (low state)	I_{CC}	V_{CC}=5V, R_L=∞ V_{CC}=15V, R_L=∞		6 20	12 30	mA mA
Timing Error (monostable) Initial Accuracy[2] Drift with Temperature Drift with Supply Voltage	MT_1	R_A=2KΩ to 100KΩ C=0.1μF C=0.1μF		 0.75 50 0.1		 % % %/V
Control Voltage Level	V_C	V_{CC}=15V	9.0	10.0	11.0	V
		V_{CC}=5V	2.6	3.33	4.0	V
Treshold Voltage	V_{IH}	V_{CC}=15V		10.0		V
		V_{CC}=5V		3.33		V
Threshold Current[3]	I_{TH}			30	250	nA
Trigger Voltage	V_T	V_{CC}=15V	4.5	5.0	5.6	V
		V_{CC}=5V	1.1	1.67	2.2	V
Trigger Current	I_T	V_T=0V		0.5	2.0	μA
Reset Voltage[5]	V_R		0.4	0.7	1.0	V
Reset Current	I_R			0.1	0.6	mA
Output Voltage Low	V_{OL}	V_{CC}=15V I_{sink}=10mA I_{sink}=50mA I_{sink}=100mA I_{sink}=200mA V_{CC}=5V I_{sink}=8mA I_{sink}=5mA		 0.1 0.4 2.0 2.5 0.25 0.15	 0.25 0.75 2.75 0.35 0.25	 V V V V V V

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V to +15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage (high)	V_{OH}	V_{CC} = 15V				
		I_{source} = 200mA		12.5		V
		I_{source} = 100mA	12.75	13.3		V
		V_{CC} = 5V				
		I_{source} = 100mA	2.75	3.3		V
Rise Time of Output	T_R			100		nsec
Fall Time of Output	T_F			100		nsec
Discharge Leakage Current	I_D			20	100	nA
Matching Characteristics	M_{CH}					
Initial Accuracy[2]				1.0	2.0	%
Drift with Temperature				10		ppm/°C
Drift with Supply Voltage				0.2	0.5	%/V
Timing Error (astable)	MT_2	R_A, R_B = 1kΩ to 100kΩ				
Initial Accuracy[2]		C = 0.1μF		2.25		%
Drift with Temperature		V_{CC} = 15V		150		ppm/°C
Drift with Supply Voltage				0.3		%/V

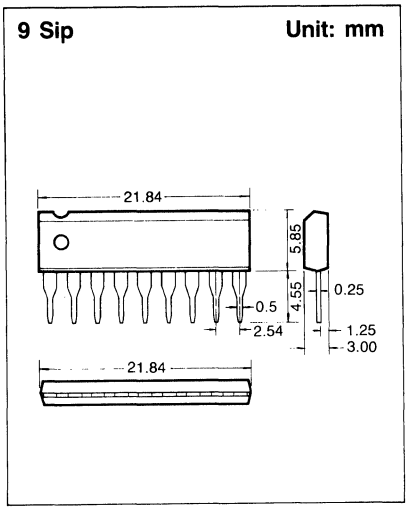
Notes:
1. Supply current when output high typically 1.0mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V
3. This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total R = 20MΩ, and for 5V operation the maximum total R = 6.6MΩ.
4. Matching characteristic refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high.



VII. MISCELLANEOUS ICs

TOY RADIO CONTROL ACTUATOR

The KA2302 is a monolithic integrated circuit designed for simple 2 function radio controlled car toy of which moving direction (forward, backward) is change whenever input singnal is diminished bellow a threshold level.



FEATURES

- **Includes**
  Amplifier, Detector, Comperator, Latch, Voltage Regulator, Actuator.
- **Wide power supply voltage range (2.5V ~ 10V).**
- **Capable of driving small DC motors in both directions**
- **Minimum number of external parts required.**

BLOCK DIAGRAM

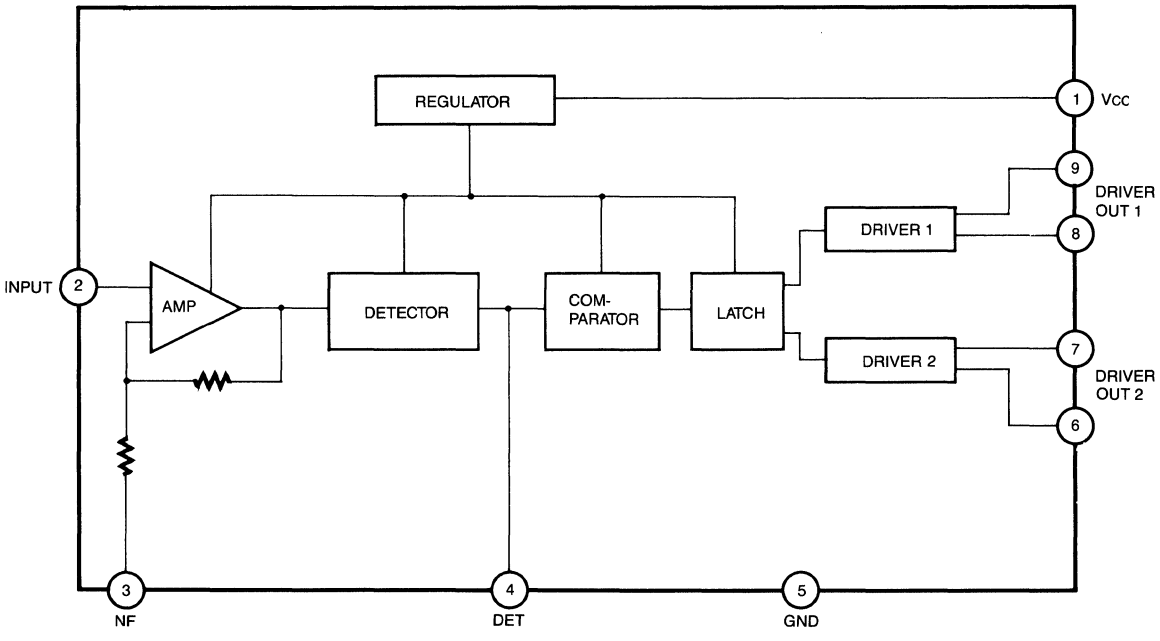


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	11	V
Output Current (Continuous)	I_O (Cont)	0.7	A
Output Current (Surge)	I_O (Surge)	1.2	A
Power Dissipation	P_d	500	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−45 ~ +125	°C

* Mounted and soldered on a 50mm×50mm copper foil of PCB

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 5V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current	I_{CC}	Without Load		40	50	mA
Input Impedance	R_i			10		KΩ
Output Saturation Voltage	V_{SAT}	I_O = 400mA		0.25	0.45	V
Output Sinking Current	I_{SINK}			10		mA
Sensitivity	V_i (sen)	f = 1KHz		3.5		mV
Comparator Hysterisis	HY			5		dB

TYPICAL APPLICATION CIRCUIT

1. Low Voltage Application Circuit

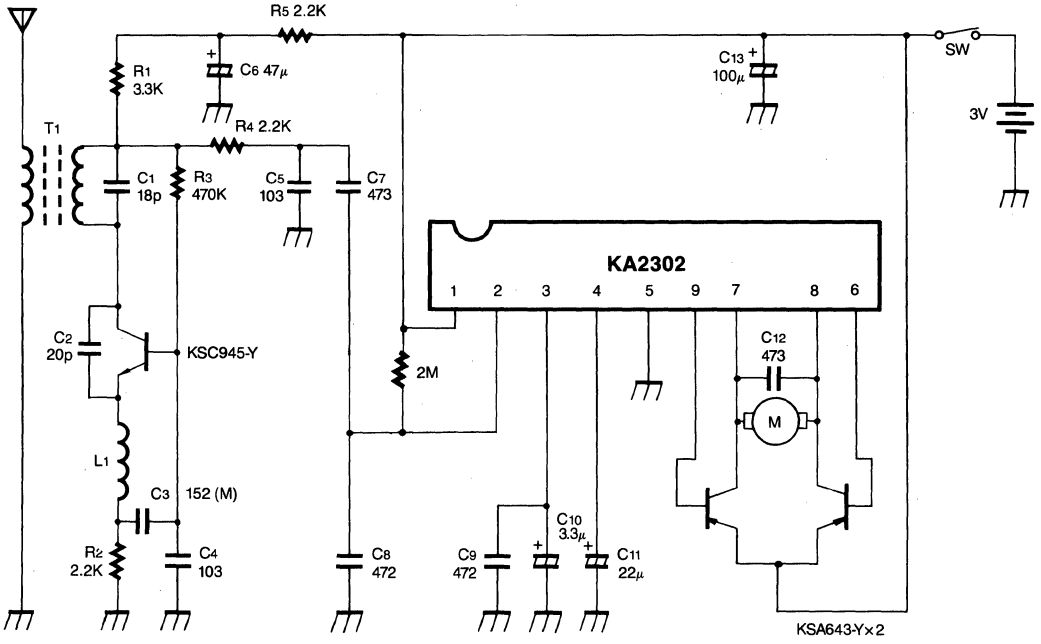


Fig. 2

2. High Voltage Application Circuit

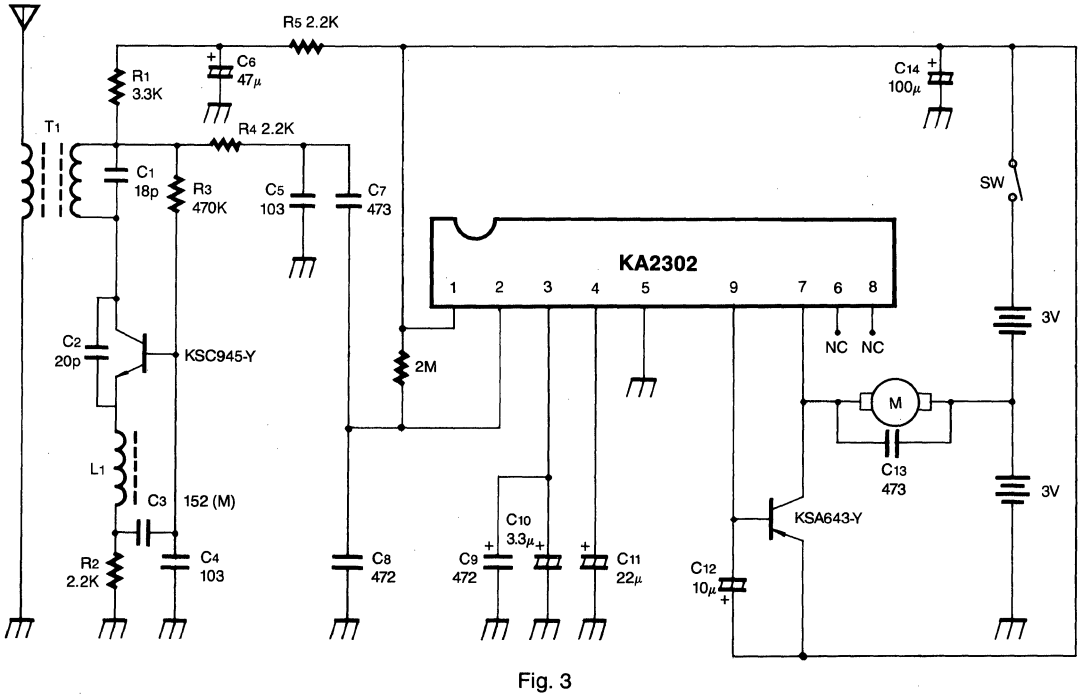
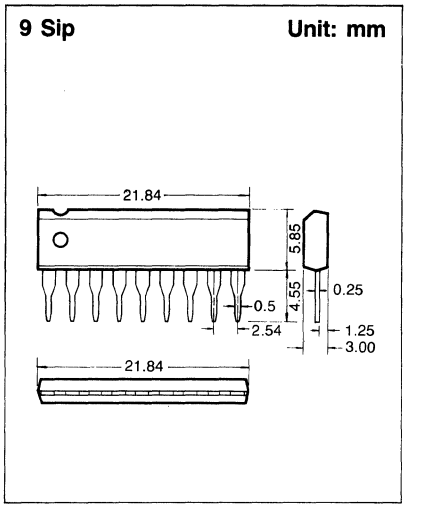


Fig. 3

TOY RADIO CONTROL ACTUATOR

The KA2303 is monolithic integrated circuit having 3 functions (Forward, stop, Backward) designed for radio controlled toy car and other equipment.



FEATURES

- **Includes**
  Amplifier, Detector, Comparator, Latch,Voltage Regulator, Actuator.
- **Wide power supply voltage range (2.5V ~ 10V)**
- **Very low quiescent circuit current (Stop: I_{CC} =5mA).**
- **Capable of driving small DC motors in both driections.**
- **Minimum number of external parts required.**

BLOCK DIAGRAM

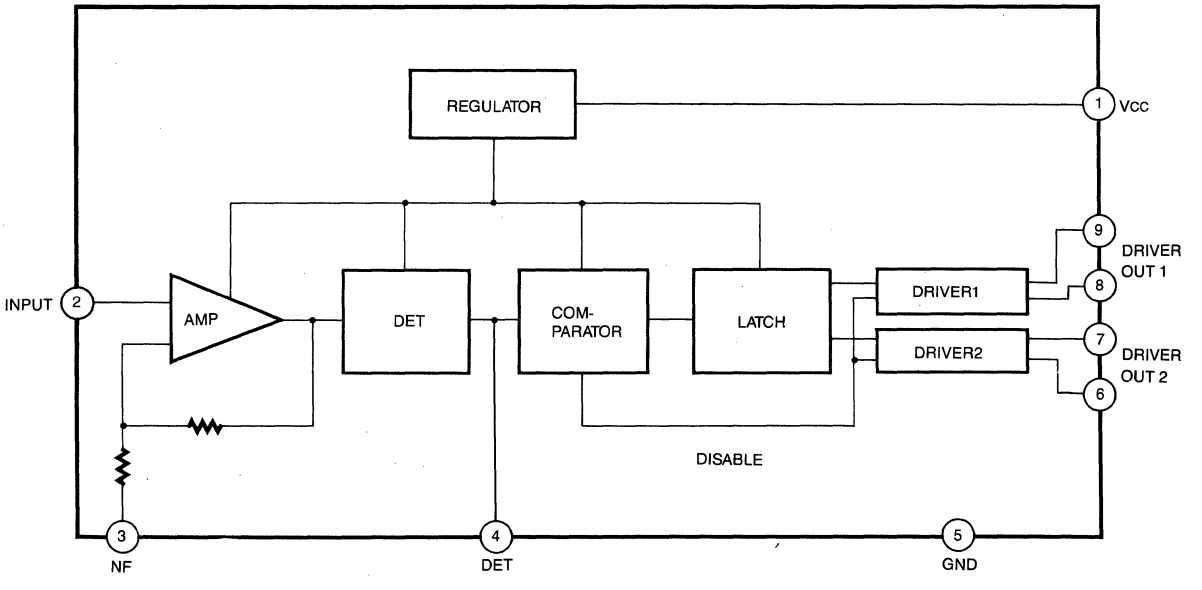


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	11	V
Output Current (Continuous)	I_O (cont)	0.7	A
Output Current (Surge)	I_O (surge)	1.2	A
Power Dissipation	P_o	500	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 5V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current	$I_{CC}1$	Without Load		40	50	mA
	$I_{CC}2$	Stop		5		mA
Input Impedance	R_i			10		KΩ
Output Sturation Voltage	V_{SAT}	I_O = 400mA		0.25	0.45	V
Output Sink Current	I_{SINK}			10		mA
Sensitivity	V_i (sen)	f=1KHz		3.5		mV
Comparator Hysterisis	HY			5		dB

TYPICAL APPLICATION CIRCUIT

1. Low Voltage Application Circuit

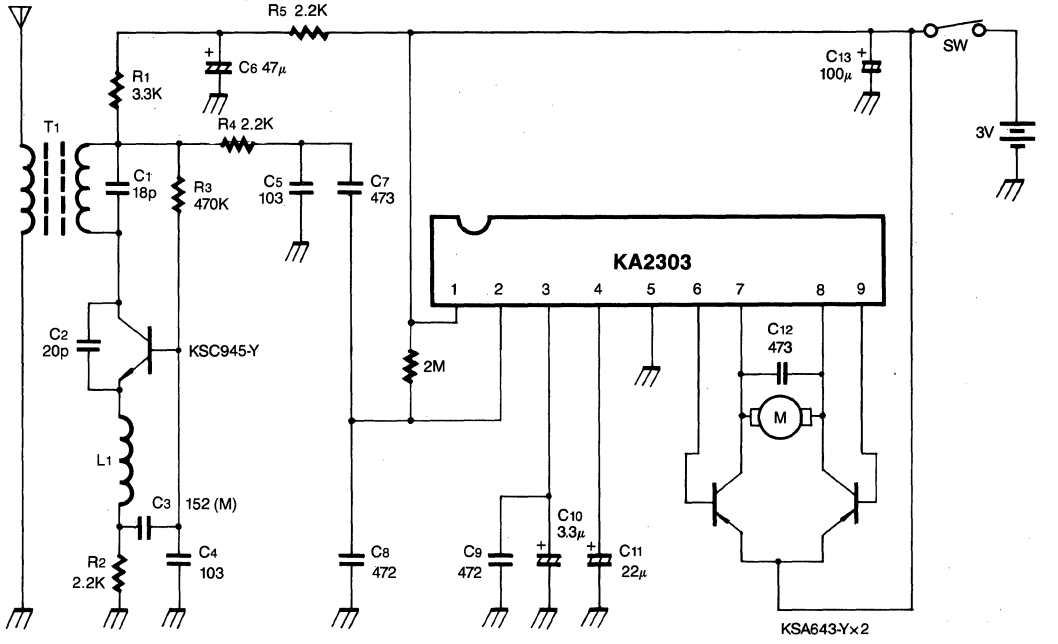


Fig. 2

2. High Voltage Application Circuit

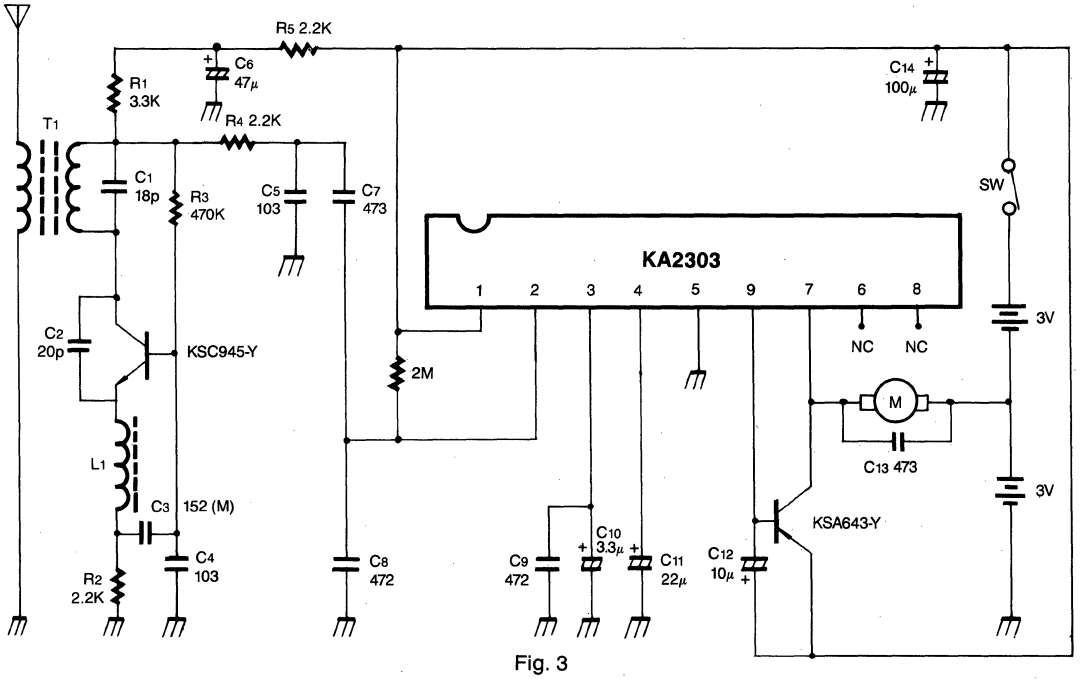


Fig. 3

8-CHANNEL SOURCE DRIVERS

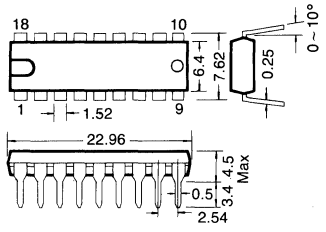
These integrated circuits, rated for operation with output voltages of up to 50V and designed to link NMOS logic with high-current inductive loads, will work with many combinations of logic-and load-voltage levels, meeting interface requirements beyond the capabilities of standard logic buffers.

KA2580A is a high current source driver used to switch the ground ends of loads that are directly connected to a negative supply. Typical loads are telephone relays, PIN diodes, and LEDs.

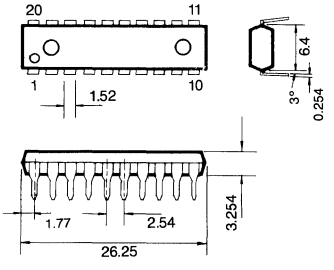
KA2588A is a high-current source driver similar to KA2580A, has separated logic and driver supply lines. Its eight drivers can serve as an interface between positive logic (TTL, CMOS, MOS) or negative logic (NMOS) and either negative or split-load supplies.

KA2580A is furnished in 18-pin with in-line plastic package; KA2588A is supplied in a 20-pin dual in-line plastic package. All input connections are on one side of the packages, output pins on the other, to simplify printed wiring board layout.

18 Dip **Unit: mm**



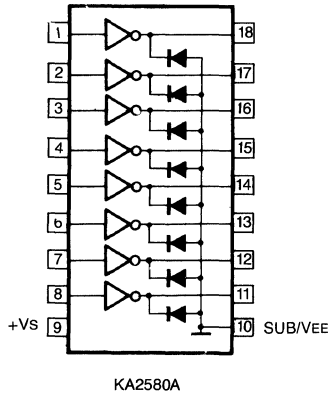
20 Dip **Unit: mm**



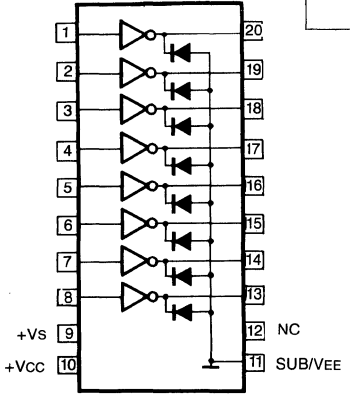
FEATURES

- **TTL, CMOS, PMOS, NMOS Compatible**
- **High Output Current Ratings**
- **Internal Transient Suppression**
- **Efficient Input/Output Pin Structure**

SCHEMATIC DIAGRAM



KA2580A



KA2588A

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C, for Any One Driver unless otherwise noted)

Characteristic	Symbol	Value	Unit
Output Voltage	V_{CE}	50	V
Supply Voltage (ref, sub)	V_S	50	V
Supply Voltage (ref, sub, KA2588A)	V_{CC}	50	V
Input Voltage (ref, Vs)	V_{IN}	−30	V
Total Current	$I_{CC}+I_S$	−500	mA
Substrate Current	I_{SUB}	3.0	A
Power Dissipation (single output)	Pd	1.0	W
(total Package)*		2.2	W
Operating Temperature	T_a	−20 ~ +85	°C
Storage Temperature	Tstg	−65 ~ +150	°C

* Derate at the rate of 18mW/°C above 25°C

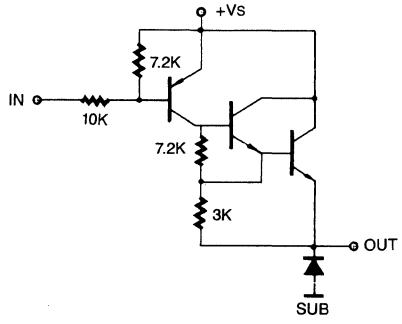
TYPICAL OPERATING VOLTAGE

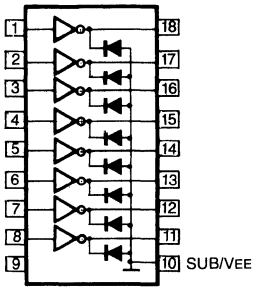
V_S	V_{INZ} (on)	V_{IN} (off)	V_{CC}	V_{CC} (max)	DVC Type
0V	−15V ~ −3.6V	−0.5V ~ 0V	NA	−50V	KA2580A
+5V	0V ~ +1.4V	+4.5V ~ +5V	NA ≤5V	−45V −45V	KA2580A KA2588A
+12V	0V ~ +8.4V	+11.5V ~ +12V	NA ≤12V	−38V −38V	KA2580A KA2588A
+15V	0V ~ +11.4V	+14.5V ~ +15V	NA ≤15V	−35V −35V	KA2580A KA2588A

Notes

1) For simplication, these devices are characterized to the above with specific voltages for inputs, logic supply (V_s), load supply (V_{ee}), and collector supply (V_{CC}).
2) Typical use of the KA2580A is with negative referenced logic. The more common application of the KA2588A is with positive referenced logic supplies.
3) In application, the devices are capable of operation over a wide range of logic and supply voltage levels.
4) The substrate must be tied to the most negative point in the external circuit to maintain isolation drivers and to provide for normal circuit operation.

PARTIAL SCHEMATIC





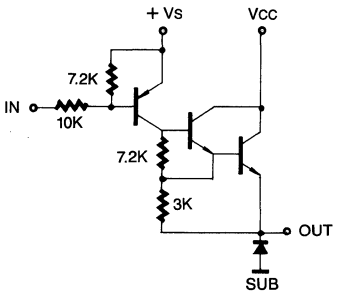
ELECTRICAL CHARACTERISTICS (T_a=25°C, V_S=0V, V_{EE}=−45V unless otherwise noted)

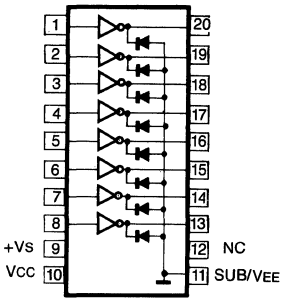
Characteristic	Symbol	Test Conditions	Min	Max	Unit
Output Leakage Current	I_{CEX}	V_{in}=−0.5V, V_{OUT}=V_{EE}=−50V		50	μA
		V_{IN}=−0.4V, V_{OUT}=V_{EE}=−50V T_a=70°C		100	μA
Output Sustaining Voltage (Note 1, 2)	V_{CE} (sus)	V_{IN}=−0.4V, I_{OUT}=−25mA	35		V
Output Saturation Voltage	V_{CE} (sat)	V_{IN}=−2.4V, I_{OUT}=−100mA		1.8	V
		V_{IN}=−3.0V, I_{OUT}=−225mA		1.9	V
		V_{IN}=−3.6V, I_{OUT}=−350mA		2.9	V
Input Current	I_{IN} (on)	V_{IN}=−3.6V, I_{OUT}=−350mA		−500	μA
		V_{IN}=−15V, I_{OUT}=−350mA		−2.1	mA
	I_{IN} (off)	I_{OUT}=−500μA, T_a=70°C (Note 3)	−50		μA
Input Voltage	V_{IN} (on)	I_{OUT}=−100mA, V_{CE}≤1.8V		−2.4	V
		I_{OUT}=−225mA, V_{CE}≤1.9V		−3.0	V
		I_{OUT}=350mA, V_{CE}≤2.0V		−3.6	V
	V_{IN} (off)	I_{OUT}=−500μA, T_a=70°C	−0.2		V
Clamp Diode Leakage Current	I_R	V_R=50V, T_a=70°C		50	μA
Clamp Diode Forward Voltage	Vf	If=350mA		2.0	V
Input Capacitance	C_{IN}			25	pF
Turn-On Delay	t_{PHL}	0.5 V_{IN} to 0.5 V_{OUT}		5.0	μS
Turn-Off Delay	t_{PLH}	0.5 V_{IN} to 0.5 V_{OUT}		5.0	μS

Notes

1) Pulsed test, tp≤300uS, duty cycle≤2%.
2) Negative current is defined as coming out of specified device pin.
3) The Iin (off) current limit guarantees against partial turn-on of the output.
4) The Vin (on) voltage limit guarantees a minimum output source per the specified conditions.
5) The substrate must always be tied to the most negative point and must be at least 4.0V below V_s.

PARTIAL SCHEMATIC





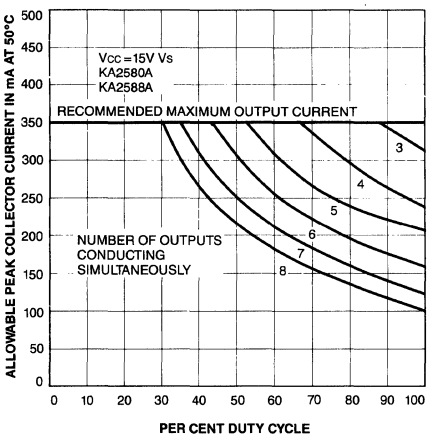
ELECTRICAL CHARACTERISTICS (T_a=25°C, V_S=5.0V, V_{EE}=−40V unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Output Leakage Current	I_{CEX}	$V_{IN} \geq 4.5V$, $V_{OUT}=V_{EE}=-45V$		50	μA
		$V_{IN} \geq 4.6V$, $V_{OUT}=V_{EE}=-45V$ T_a=70°C		100	μA
Output Sustaining Voltage (Note 1, 2)	V_{CE} (sus)	$V_{IN} \geq 4.6V$, $I_{OUT}=-25mA$	35		V
Output Saturation Voltage	V_{CE} (sat)	V_{IN}=2.6V, $I_{OUT}=-100mA$ Ref. V_{CC}		1.8	V
		V_{IN}=2.0V, $I_{OUT}=-225mA$ Ref. V_{CC}		1.9	V
		V_{IN}=1.4V, $I_{OUT}=-350mA$ Ref. V_{CC}		2.0	V
Input Current	I_{IN} (on)	V_{IN}=1.4V, $I_{OUT}=-350mA$		−500	μA
		V_S=15V, $V_{EE}=-30V$, V_{IN}=0V, $I_{OUT}=-350mA$		−2.1	mA
	I_{IN} (off)	$I_{OUT}=-500\mu A$, T_a=70°C (Note 3)	−50		μA
Input Voltage (Note 4)	V_{IN} (on)	$I_{OUT}=-100mA$, $V_{CE} \leq 1.8V$		2.6	V
		$I_{OUT}=-225mA$, $V_{CE} \leq 1.9V$		2.0	V
		$I_{OUT}=-350mA$, $V_{CE} \leq 2.0V$		1.4	V
	V_{IN} (off)	$I_{OUT}=-500\mu A$, T_A=70°C	4.8		V
Clamp Diode Leakage Current	I_R	V_R=50V, T_a=70°C		50	μA
Clamp Diode Forward Voltage	Vf	If=350mA		2.0	V
Input Capacitance	C_{IN}			25	pF
Turn-On Delay	t_{PHL}	0.5 V_{IN} to 0.5 Vout		5.0	μS
Turn-Off Delay	t_{PLH}	0.5 V_{IN} to 0.5 Vout		5.0	μS

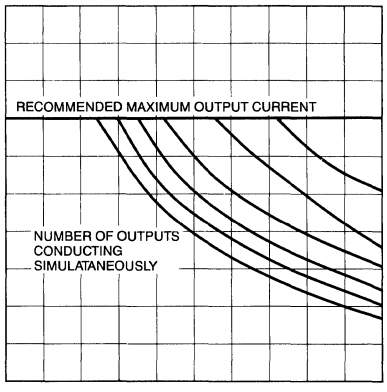
Notes

1) Pulsed test, tp ≤ 300uS, duty cycle ≤ 2%.
2) Negative current is defined as coming out of specified device pin.
3) The Iin (off) current limit guarantees against partial turn-on of the output.
4) The Vin (on) voltage limit guarantees a minimum output source per the specified conditions.
5) The substrate must always be tied to the most negative point and must be at least 4.0V below V_s.
6) V_{CC} must never be more positive than V_S.

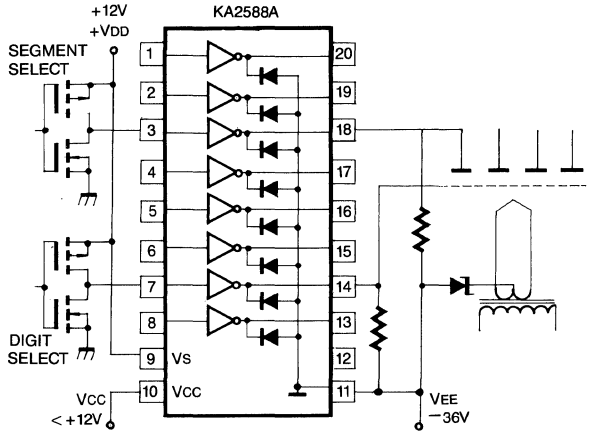
ALLOWABLE PEAK COLLECTOR CURRENT AT 50°C AS A FUNCTION OF DUTY CYCLE



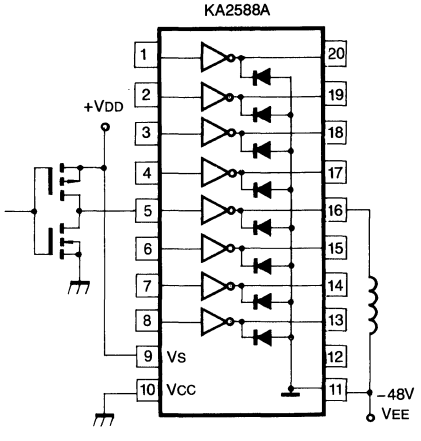
ALLOWABLE PEAK COLLECTOR CURRENT AT 70°C AS A FUNCTION OF DUTY CYCLE



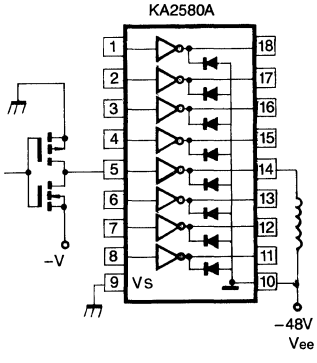
TYPICAL APPLICATIONS



Vacuum Fluorescent Display Driver (Split Supply)



Tlecommunicaiton Relay Driver (Positive Logic)

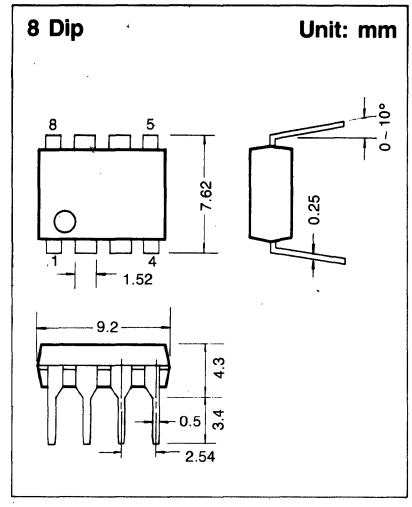


Telecommunication Relay Driver (Negative Logic)

LOW POWER CONSUMPTION EARTH LEAKAGE DETECTOR

The KA2803 is designed for use in earth leakage circuit interrupters, for operation directly off the AC line in breakers. The input of the differential amplifier is connected to the secondary coil of ZCT (Zero Current Transformer). The amplified output of differential amplifier is integrated at external capacitor to gain adequate time delay that is specified in KSC4613.

The level comparator generates high level when earth leakage current is greater than some level.



FUNCTIONS

- Differential amplifier
- Level camparator
- Latch circuit

FEATURES

- **Low power consumption (P_d=5mW, 100V/200V)**
- **Built-in voltage regulator**
- **High gain differential amplifier (V_T=13.5mV)**
- **1mA output current pulse to trigger SCR'S**
- **Low external part count, economic**
- **Mini-dip package (8 Dip), high packing density**
- **High noise immunity, large surge margin**
- **Super temperature characteristic of input sensitivity**
- **Wide operating temperature range (T_a=−25°C ~ +80°C)**

APPLICATION CIRCUIT

1. Full Wave Application Circuit

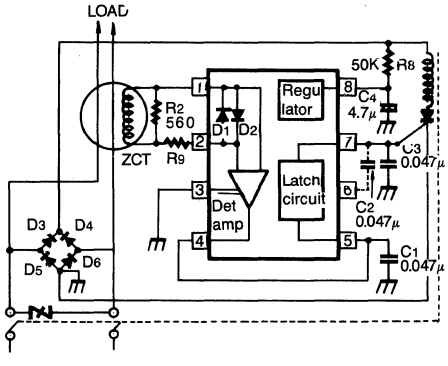


Fig. 1

2. Half Wave Application Circuit

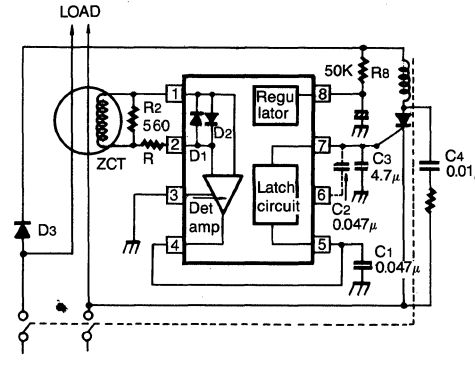


Fig. 2

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	20	V
Supply Current	I_S	8	mA
Power Dissipation (T_a =25°C)	P_d	300	mW
Operating Temperature	Topr	−25 ~ +80	°C
Storage Temperature	Tstge	−65 ~ +150	°C
Lead Temperature (soldering 10 sec)	Tlead	260	°C

ELECTRICAL CHARACTERISTICS (T_a =25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current 1	I_{S1}	V_{CC} =12V (−25°C) V_R-V_I =300mV (25°C) (80°C)		400	580 530 480	μA μA μA
Trip Voltage		V_{CC} =16V (−25°C ~ 80°C) V_R-V_I =X	10	13.5	17	mVrms
Differential Amplifier Output Current 1	I_{TDI}	V_{CC} =16V (25°C) V_R-V_I =30mV V_{OD} =1.2V	12		30	μA
Differential Amplifier Output Current 2	I_{TD2}	V_{CC} =16V (25°C) V_{OD} =0.6V V_R, V_1 short	17		37	μA
Output Current	I_O	V_{SC} = 1.4V V_{OS} =0.8V V_{CC} = 12V (−25°C) (+25°C) (+80°C)	 −200 −100 −75			 μA μA μA
Latch on Voltage	V_{scon}	V_{CC} = 16V (25°C)	0.7		1.4	V
Latch Input Current	I_{scon}	V_{CC} =12V (25°C)			5	μA
Output Low Current	I_{OSL}	V_{CC} =12V (−25 ~ 80°C) V_{OSL} =0.2V	200			μA
Diff. Input Clamp Voltage	V_{IDC}	I_{IDC} =100mA (−25 ~ 80°C)	0.4		2	V
Maximum Current Voltage	V_{SM}	I_{SM} =7mA (−25°C)	20		28	V
Supply Current 2	I_{S2}	V_R-V_I =X (25 ~ 80°C) V_{OS} =0.6			900	μA
Latch Off Supply Voltage	V_{soff}	V_{os} =high (25°C)	7.0			V
Response Time	T_{on}	V_{CC} =16V (25°C) V_R-V_I =0.3V	2		4	msec

APPLICATION NOTE

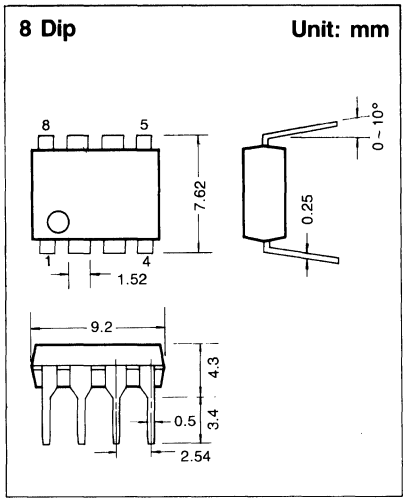
(refer to full wave application circuit Fig. 1)

The Fig 1 shows the KA2803 connected in a typical leakage current detector system.
The power is applied to the V_{CC} terminal (Pin 8) of the KA2803 directly from the power line.
The resistor R_S and capacitor C_S are chosen so that pin 8 voltage is at least 12V.
The value of C_S is recommended above 1μF at this time.
If the leakage current is at the load, it is detected by the zero current transformer (ZCT).
The output voltage signal of ZCT is amplified by the differential amplifier of the KA2803 internal circuit and appears as half-cycle sine wave signal referred to input signal at the output of the amplifier.
The amplifier closed loop gain is fixed about 1000 times with internal feedback resistor to compensate for zero current transformer (ZCT) Variations.
The resistor R_L should be selected so that the breaker satisfies the required sensing current.
The protection resistor R_P is not usually used put when the high current is injected at the breaker, this resistor should be used to protect the earth leakage detector IC the KA2803.
The range of R_P is from several hundred Ω to several kΩ.
The capacitor C_1 is for the noise canceller and standard value of C_1 is 0.047μF. Also the capacitor C_2 is noise canceller capacitance but it is not usually used.
When high noise is only appeared at this system 0.047μF capacitor may be connected between pin 6 and pin 7.
The amplified signal is finally appeared to the Pin 7 with pulse signal through the internal latch circuit of the KA2803.
This signal drivies the gate of the external SCR which energizes the trip coil which opens the circuit breaker.
The trip time of breaker is decided by the capacitor C_3 and the mechanism breaker.
This capacitor should be selected under 1μF for the required the trip time.
The full wave bridge supplies power to the KA2803 during both the positive and negative half-cycles of the line voltage.
This allows the hot and neutral lines to be interchanged.
If your application want the detail information, request it on our application circuit designer of KA2803.

LINEAR INTEGRATED CIRCUIT

The KA2804 is a TRIAC controller providing a complete solution for temperature controlled electric panel heaters, cookers, film processing baths etc.

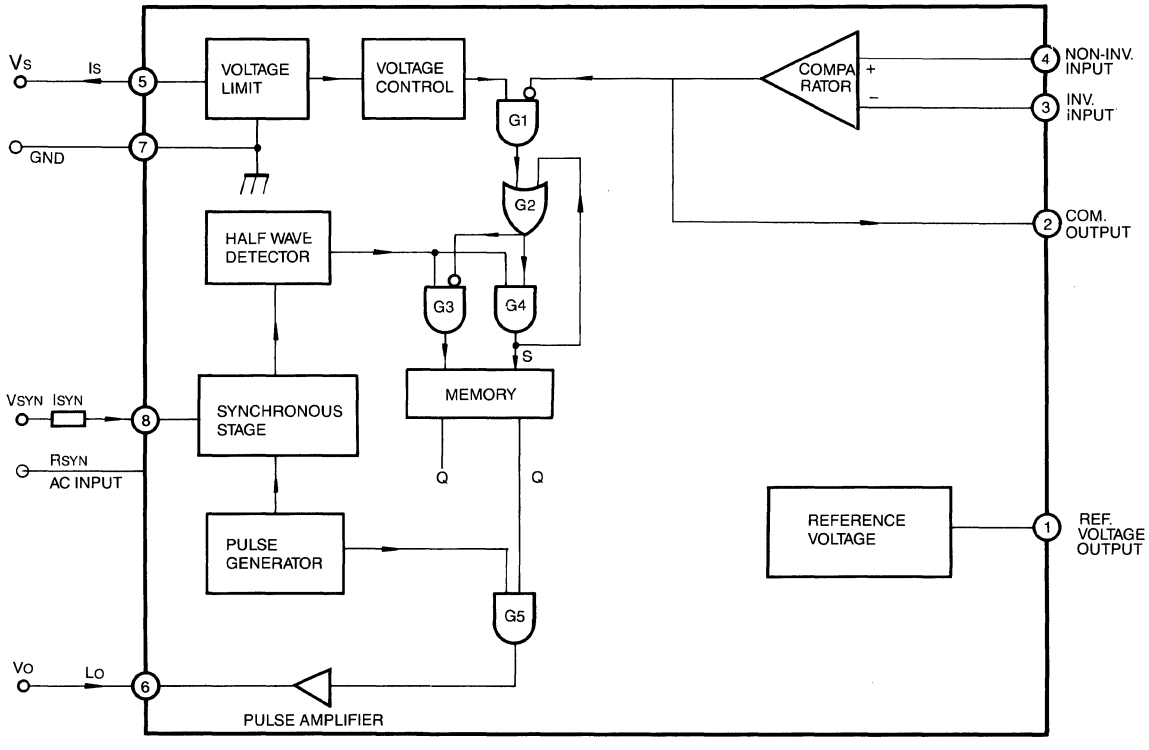
Switching occurs at the zero voltage point in order to minimise radio frequency interference. The device is suitable for mains-on-line operation and requires minimal components.



FEATURES

- **Easy operation either through the AC line or a DC supply.**
- **Supply voltage control.**
- **Very few external components.**
- **Symmetrical burst control — No DC current components in the load circuit.**
- **Negative output current pulse up to 250mA-short circuit protection.**
- **Reference voltage output.**

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Ratings	Symbol	Value	Unit
Supply Voltage	$-V_S$	8.2	V
Supply Current	$-I_S$	40 (average)	mA
Synchronous Current	I_{SYN}	5.0 (rms)	mA
Input Voltage	V_I	$\leqq \lvert V_S \rvert$	V
Junction Temperature	T_J	125	°C
Operating Ambient Temperature	T_{opr}	−20 to 70	°C
Storage Temperature	T_{stg}	−65 to 150	°C
Power Dissipation	P	350	mW

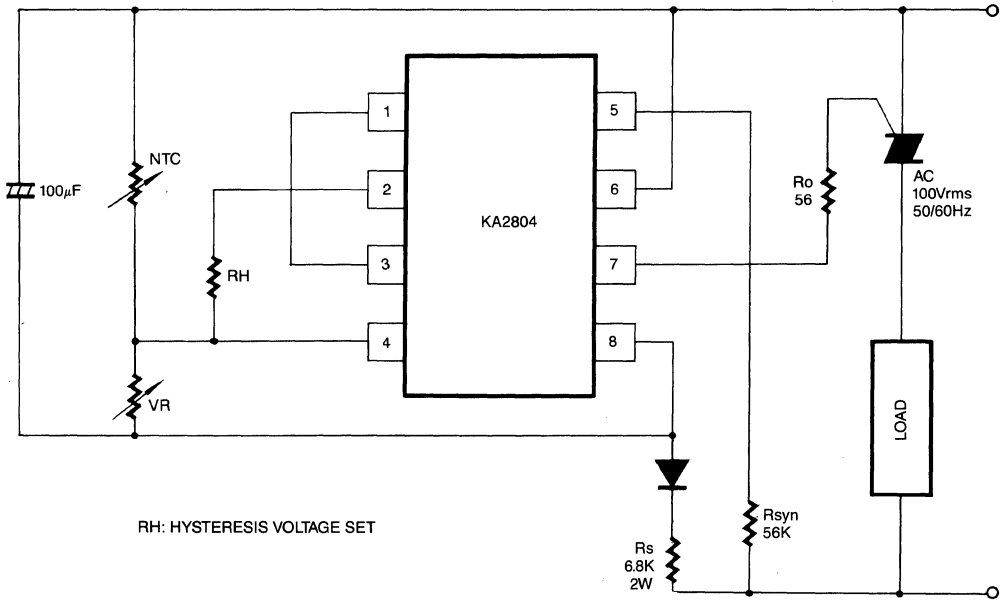
ELECTRICAL CHARACTERISTICS

(V_s=8.0V, V_{SYN}=100 to 115V_{rms}, T_a=25°C, f=50/60Hz)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current	$-I_S$	Pin 5, R_{SYN}=56K	—	2.0	2.5	mA
Supply Voltage 1	$-V_S$ 1	Pin 5, I_S=2.5mA R_{SYN}=56K	7.2	—	8.4	V
Supply Voltage 2	$-V_S$ 2	Pin 5, I_S=20mA R_{SYN}=56K	7.2	—	8.6	V
Synchronous Current	I_{SYN}	Pin 8	0.3	—	—	mA
Output Pulse Width	T_P	Pin 6, R_{SYN}=56K	—	200	—	μS
Output Voltage	V_O	Pin 6, $I_O \leqq$ 200mA	4.2	5.2	—	V
Output Current	I_O	Pin 6, $R_O \leqq$ 25	200	250	—	mA
Output Leakage Current	I_{LO}	Pin 6	—	—	2.0	μA
Input Offset Voltage	V_{IO}	Pin 3, 4	—	2.0	5.0	mV
Input Bias Current	I_I	Pin 3, 4	—	0.5	1.0	μA
Common Mode Input Voltage Range	$-V_{ICM}$	Pin 3, 4	0	—	5.7	V
Output Leakage Current	I_{LC}	Pin 2	—	—	0.2	μA
Reference Voltage	$-V_R$	Pin 1, $I_R \leqq$ 1uA	—	3.6	—	V

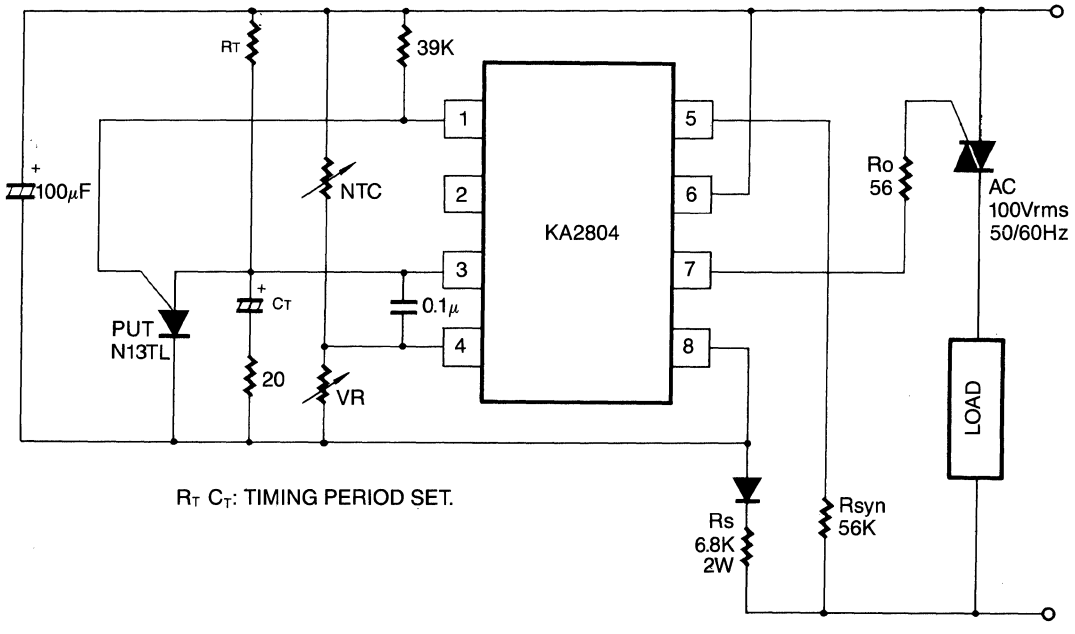
APPLICATIONS

ON-OFF TEMPERATURE CONTROL



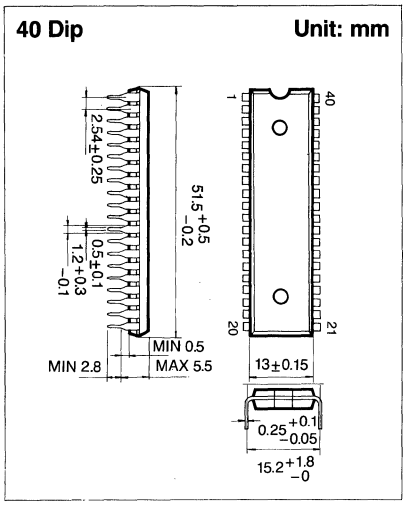
RH: HYSTERESIS VOLTAGE SET

TIME PROPORTIONAL TEMPERATURE CONTROL



R_T C_T: TIMING PERIOD SET.

3 1/2 DIGIT A/D CONVERTER



GENERAL DESCRIPTION

The single chip CMOS KS7126 incorporates all the active devices for a 3 1/2 digit analog-to-digital converter to directly drive an LCD display. The internal oscillator, voltage reference and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution-0.05%-indicating meter requires only a display, four resistors, four capacitors and 9V battery.

The KS7126 dual slope conversion technique rejects interference signal when the integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 40Hz line frequency signals are present. With an auto-zero error less than 10μV, zero drift less than 1μV/°C, input bias current of 10pA max and rollover error of less than one count, the KS7126 brings exceptional value to the portable battery powered field.

In addition, the differential input and reference allows the measurement on load cells, strain gauges and other bridge type transducers. The low power KS7126 can be used as a plug-in replacement for existing 7106 based systems by changing only the values of seven passive components.

FEATURES

- **Long Battery Life: 800 Hours Typical**
- **Auto-Zero Cycle**
- **Guaranteed Zero Reading With Zero Input**
- **Low Noise: 15μVp-p**
- **High Resolution (0.05%) and Wide Dynamic Range (72dB)**
- **Low Input Leakage Current: 1pA Typical, 10pA Maximum**
- **Direct LCD Display Drive-No External Components**
- **Precision Null Detection With True Polarity at Zero**
- **High Impedance Differential Input**
- **Convenient 9V Battery Operation With Low Power Dissipation: 500μW Typical, 900μW Maximum**
- **Internal Clock Circuit**
- **Drop-In Replacement for TSC7126, ICL7126**

TYPICAL APPLICATIONS

- Thermometry
- Bridge Readouts (Strain Gauges, Load Cells, Null Detectors)
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid/flow Rate/Viscosity/Level
- Digital Scales
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Photometers

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Analog Input Voltage (Either Input) (1)	V_{IN}	$V_{CC} \sim V_{EE}$	V
Reference Input Voltage (Either Input)	V_{REF}	$V_{CC} \sim V_{EE}$	V
Clock Input	V_{CL}	Text $\sim V_{CC}$	V
Power Dissipation	Pd	800	mW
Operating Temperature	T_a	0 ~ +70	°C
Storage Temperature	Tstg	−65 ~ +160	°C
Lead Temperature (Soldering, 60 Sec)	TI	300	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mW	−000.0	+000.0	+000.0	Digital Reading
Zero Reading Drift	V_{IN} = 0, 0°C < T_a < 70°C		0.2	1	μV/°C
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999 1000	1000	Digital Reading
Linearity (Max. deviation from best straight line fit)	Full Scale = 200mV or Full Scale = 2.000V	−1	+0.2	+1	Counts
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN}$ = 200.0mV	−1	+0.2	+1	Counts
Noise (Pk-Pk value not exceed 95% of time)	V_{IN} = 0V		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Common Mode Rejection Ratio (4)	V_{CM} = +1V, V_{IN} = 0V Full Scale = 200.0mV		50	μV/V	
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0 < T_a < 70°C (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
Temp. Coeff. of Common (with respect to positive supply)	250KΩ between Common and positive supply		80		ppm/°C
Analog Common Voltage (with respect to positive supply)	250KΩ between Common and positive supply	2.4	2.8	3.2	V
Pk-Pk Segment Drive Voltage (Note 5)	$V_{CC} \sim V_{EE}$ = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	$V_{CC} \sim V_{EE}$ = 9V	4	5	6	V

Notes

1) Input voltages may exceed the supply voltages provided the input current is limited to +100μA.
2) Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3) Unless otherwise noted, specifications apply T_a=25°C, f_{CLOCK}=16KHz and are tested in the circuit of Figure 1.
4) Refer to "Differential Input" discussion on page 7.
5) Backplane drive is in phase with segment drive for 'off' segment, 180 out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6) During auto-zero phase, current is 10~20μA higher, 48KHz oscillator, Figure 2, increases current by 8μA (Typ.)

TYPICAL OPERATING CIRCUITS

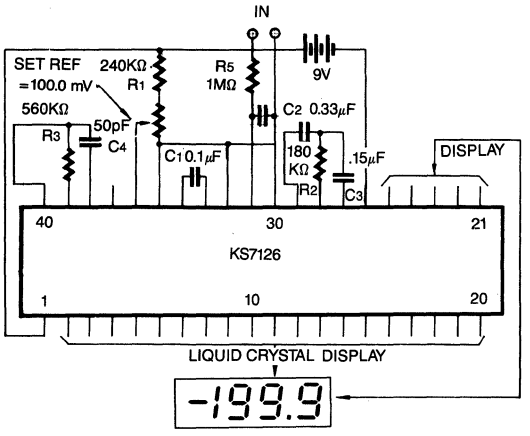


Figure 1: KS7126 Clock Frequency 16 KHz (1 reading/sec.)

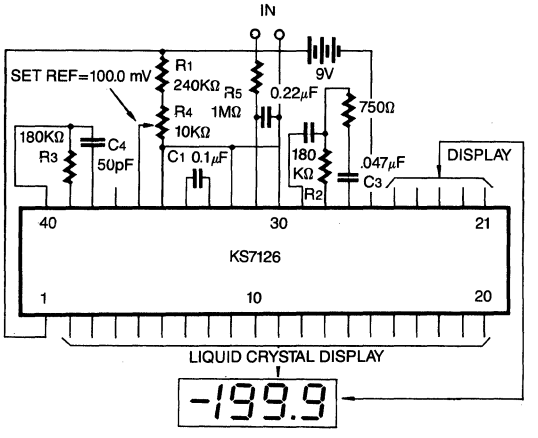
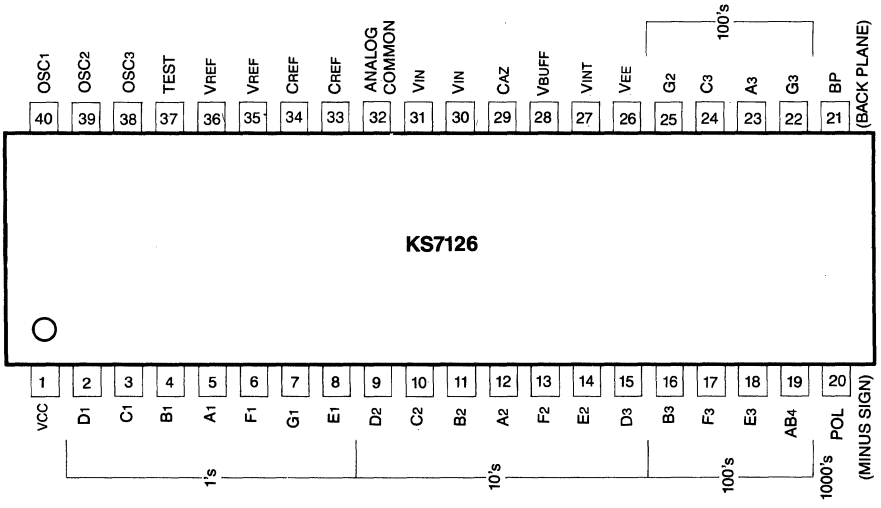


Figure 2: KS7126 Clock Frequency 48 KHz (3 readings/sec.)

PIN CONFIGURATION



PIN DESCRIPTION

Pin Number	Name	Description
1	V_{CC}	Positive supply voltage.
2	D_1	Activates the D section of the units display.
3	C_1	Activates the C section of the units display.
4	B_1	Activates the B section of the units display.
5	A_1	Activates the A section of the units display.
6	F_1	Activates the F section of the units display.
7	G_1	Activates the G section of the units display.
8	E_1	Activates the E section of the units display.
9	D_2	Activates the D section ofthe units display.
10	C_2	Actatives the C section of the tens display.
11	B_2	Activates the B section of the tens display.
12	A_2	Activates the A section of the tens display.
13	F_2	Activates the F section of the tens display.
14	E_2	Activates the E section of the tens display.
15	D_3	Activates the D section of the hundreds display.
16	B_3	Activates the B section of the hundreds display.
17	F_3	Activates the F section of the hundreds display.
18	E_3	Activates the E section of the hundreds display.
19	AB_4	Activates both halves of the 1 in the thousands display.
20	POL	Activates the negative polarity display.
21	BP	Backplane drive output
22	G_3	Activates the G section of the hundreds display.
23	A_3	Activates the A section of the hundreds display.
24	C_3	Activates the C section ofthe hundreds display.
25	G_2	Activates the G section of the tens display.
26	V_{EE}	Negative power supply voltage.
27	Vint	The integrating capacitor should be selected to give maximum voltage swing that ensures component tolerance build up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 reading per second, a 0.047μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See INTEGRATING CAPACITOR section for additional details.
28	Vbuff	Integration resistor connection. Use a 180K for a 200mV full-scale range and a 180K for 2V full-scale range.
29	Caz	The size of the auto-zero capacitor influences the system noise. Use a 0.33μF capacitor for a 200mV full-scale, and 0.033μF capacitor for a 2V full-scale. See paragraph on AUTO-ZERO CAPACITOR fo more details.

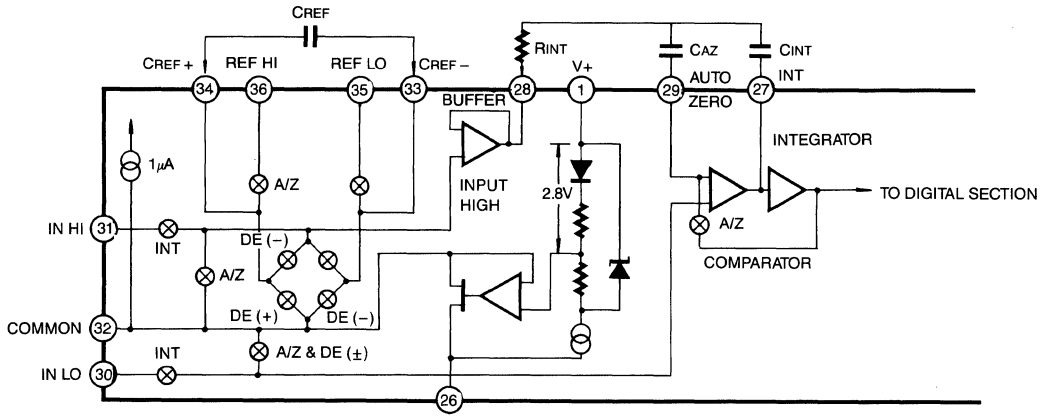
PIN DESCRIPTION (Continued)

Pin Number	Name	Description
30	Vin–	The low input is connected to this pin.
31	Vin+	The high input signal is connected to this pin.
32	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in sytem where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON on more details. It also acts as a reference voltage source.
33	Cref–	See pin 34
34	Cref+	A 0.1μF capacitor is used in most applications. If a large common mode voltage exists (for example the Vin pin is not at analog common), and a 200mV scale is used, a 1.0μF is recommended and will hold the rollover error to 0.5 count.
35	Vref–	See pin 36.
36	Vref+	The analog input required to generate a full-scale output (1.999 counts). Place 100mV between pins 35 and 36 for 199.9mV full-scale. Place 1.000 volt between pins 35 and 36 for 2V full-scale. See paragraph on REFERENCE VOLTAGE.
37	Test	Lamp test. When pulled high (to V_{CC}) all segments will be turned ON and the display should read –1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	OSC_3	See pin 40.
39	OSC_2	See pin 40.
40	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48KHz clock (3 readings per second) connect pin 40 the junction of a 180K resistor an a 50pF capacitor. The 180K resistor is tied to pin 39 an the 50pF capacitor is tied to pin 38.

DETAILED DESCRIPTION

ANALOG SECTION

Fig. 3 shows the Block Diagram of the Analog Section for the KS7126. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).



Flg. 3 Analog Section of KS7126

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one Volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000(\frac{V_{IN}}{V_{REF}})$

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 Volts below the positive supply to 1.0 Volt above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 Volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its modes. If there gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparision to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (See component Value Section)

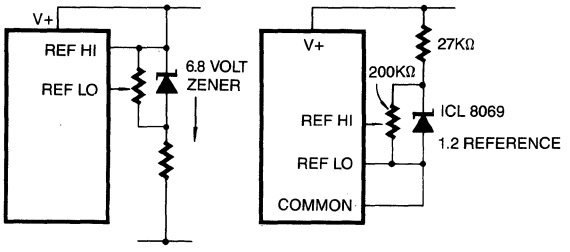


Fig. 4: Using an External Reference

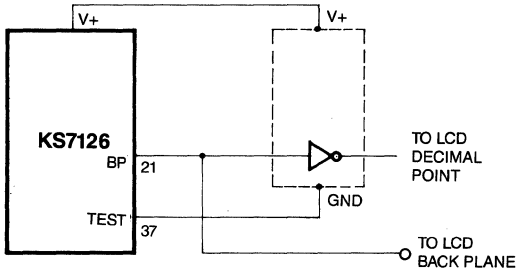


Figure 5: Simple Inverter for Fixed Decimal Point

Analog Common

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 Volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (<7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance (©15Ω), and a temperature coefficient typically less than 80 ppm/°C.

The limitations of the on-chip reference should be also recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2 to 8°C, typical for instruments, can give a scale factor error of a count or more. Also the common voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Fig. 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 100μA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage thus overriding the internal reference.

Test

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display Fig. 5 and Fig. 6 show such an application. No more than a 1mA load should be applied.

The second function is a "lamp test". When TEST is pulled high (to V_{CC}) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

CAUTION: In the lamp test mode, the segments have a constant D-C voltage (no square-wave) and may burn the LCD display if left in this mode for extended periods.

DIGITAL SECTION

Fig. 7 shows the digital section for the 7126. An internal digital ground is generated from a 6 volt zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive current when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

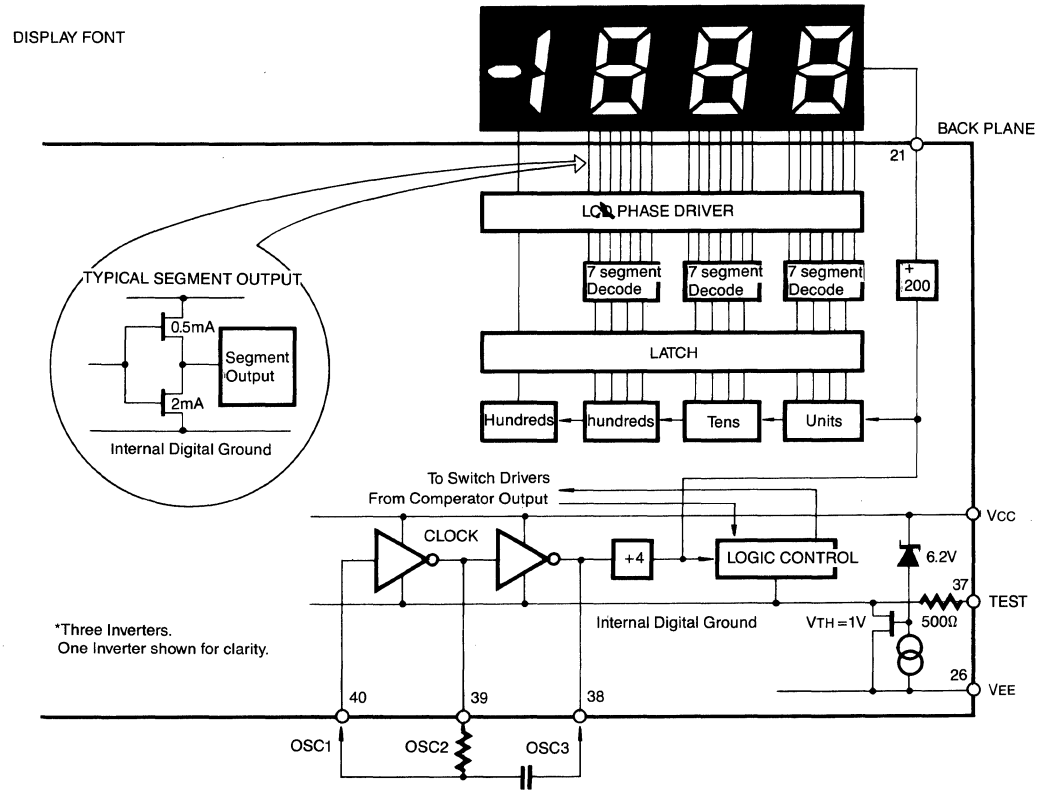


Fig. 7: Digital Section

System Timing

Fig. 8 shows the clocking arrangement used in the 7126. Three basic clocking arrangements can be used

1. An external oscillator connected to pin 40
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins

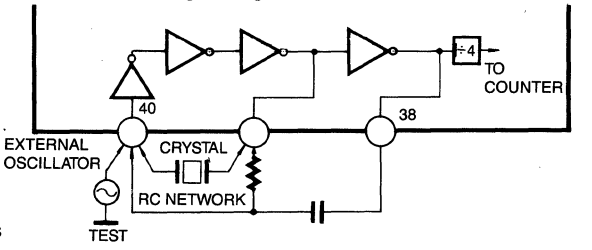


Fig. 8: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counts. It is then futher divided to form the three convert — cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto — zero (1000 to 3000 counts). For signals less than full scale, auto — zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (1,600 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 KHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequency of 60KHz, 48KHz, 33⅓KHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66⅔KHz, 50KHz, 40KHz, etc. would be suitable. Note that 40KHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz)

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6 μA of quiescent current. They can supply ~ 1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 Volt full scale, 1.8MΩ is near optimum and similarly 180KΩ for a 200.0mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integral swing (approx. 0.3 Volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 Volt full scale integrator swing is fine.For three readings/second (48KHz clock) nominal values for C_{INT} are 0.047μF, for 1/sec (16KHz) 0.15μF of course, it different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost. At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay.

3. Auto — Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.32μF capacitor is recommended. On the 2 Volt scale, a 0.033μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not analog COMMON) and a 200mV scale is used, a large value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

5. Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim \frac{45}{RC}$. For 48KHz clock (3 readings/second) R=18KΩ

TYPICAL APPLICATIONS

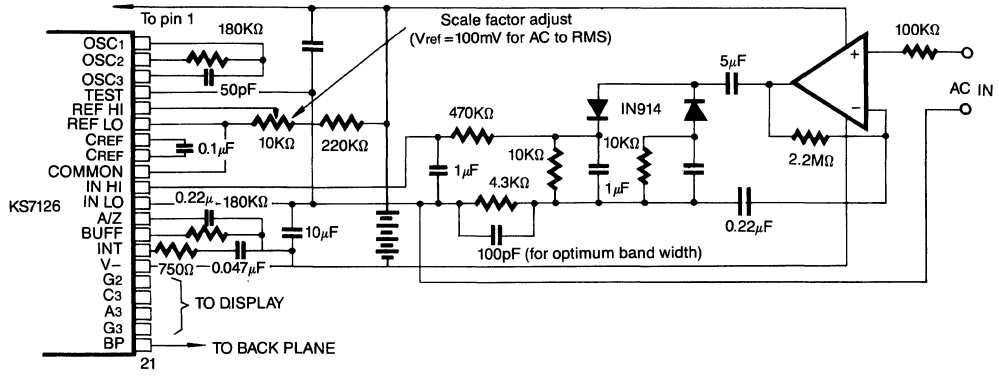


Figure 9: AC to DC Converter with KS7126. Test is Used as a Common Mode Reference Level to Ensure Compatibility with Most Op-amps.

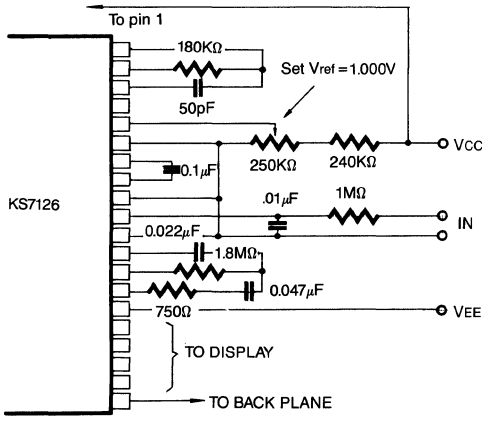


Figure 10: Recommended Values for 2.000V Full-Scale, Three Readings Per Second.

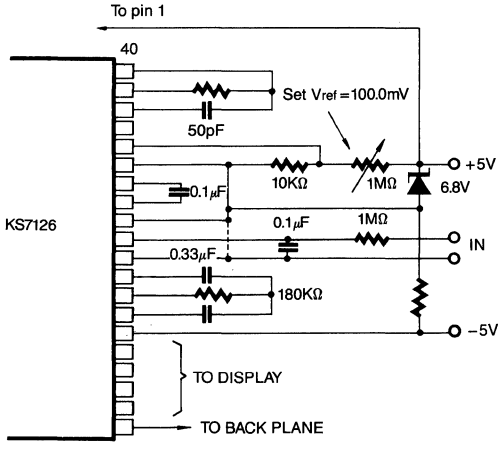


Figure 11: KS7126 with Zener Diode Reference.

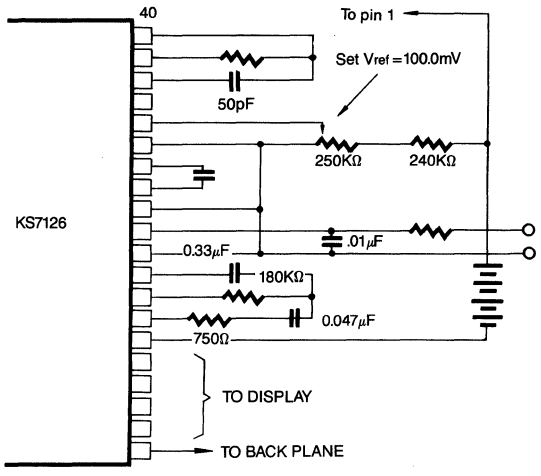


Figure 12: KS7126 Using the Internal Reference. 200.0mV Full-Scale, Three Readings Per Second, Floating Supply Voltage (9V Battery).

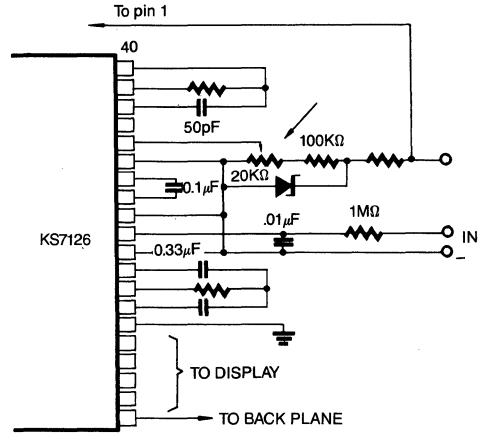
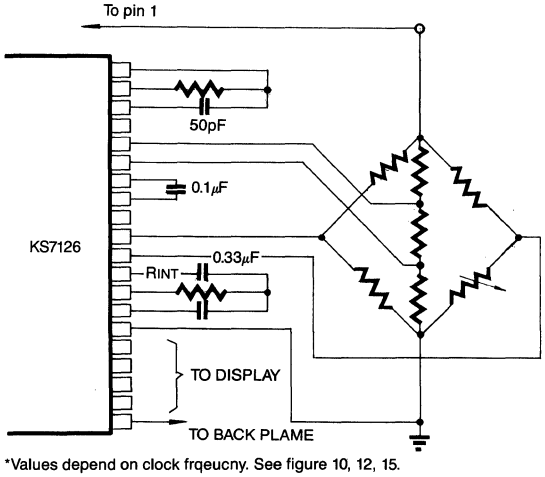


Figure 13: KS7126 Operated From Single +5V Supply. An External Reference Must Be Used.



*Values depend on clock frqeucny. See figure 10, 12, 15.

Figure 14: KS7126 Measuring Ratiometric Values of Quad Load Cell. The Resistor Values Within theBridge are Determined by the Desired Sensitivity.

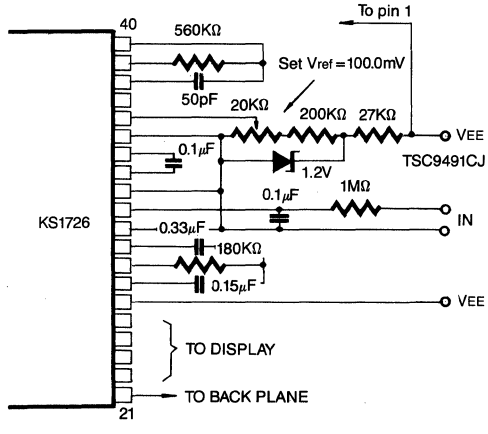


Figure 15: KS7126 with an External Band-Gap Reference (1.2V Typ) IN LO is tied to Common. Values Shown are for One Reading Per Second.

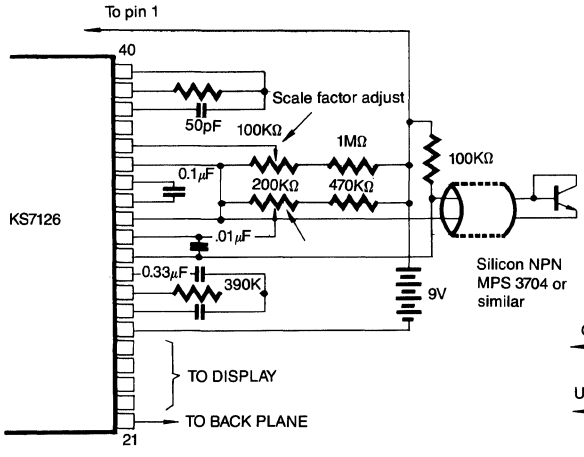


Figure 16: KS7126 Used as a Digital Centigrade Thermometer. A Silicon Diode-Connected Transistor Has a Temperature Coefficient of About 2mV/°C.

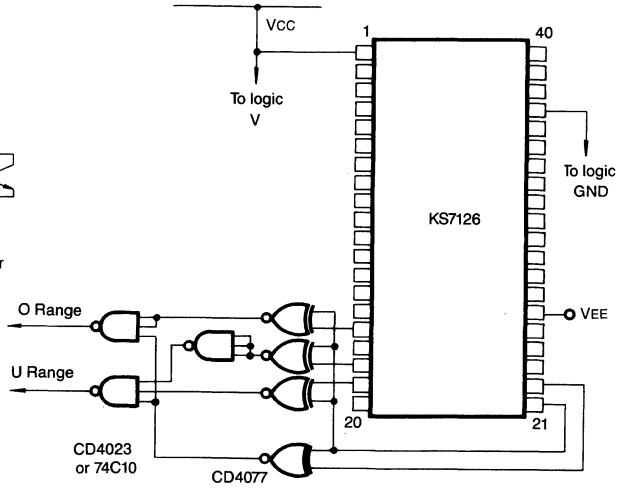


Figure 17: Circuit for Developing Underrange and Overrange Signals from KS7126 Outputs.

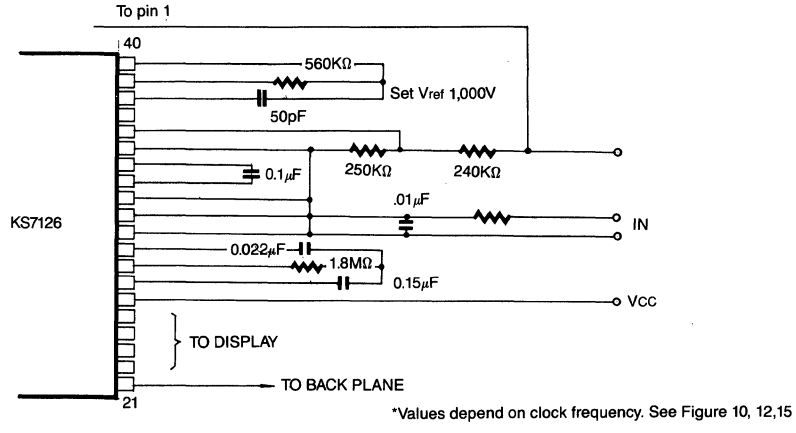
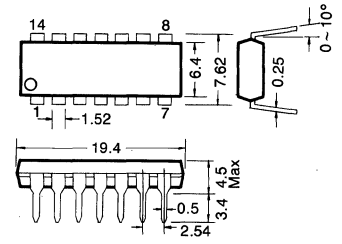


Figure 18: Recommended Component Values for 2.00V Full-Scale, One Reading Per Second.

QUAD LINE DRIVER

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

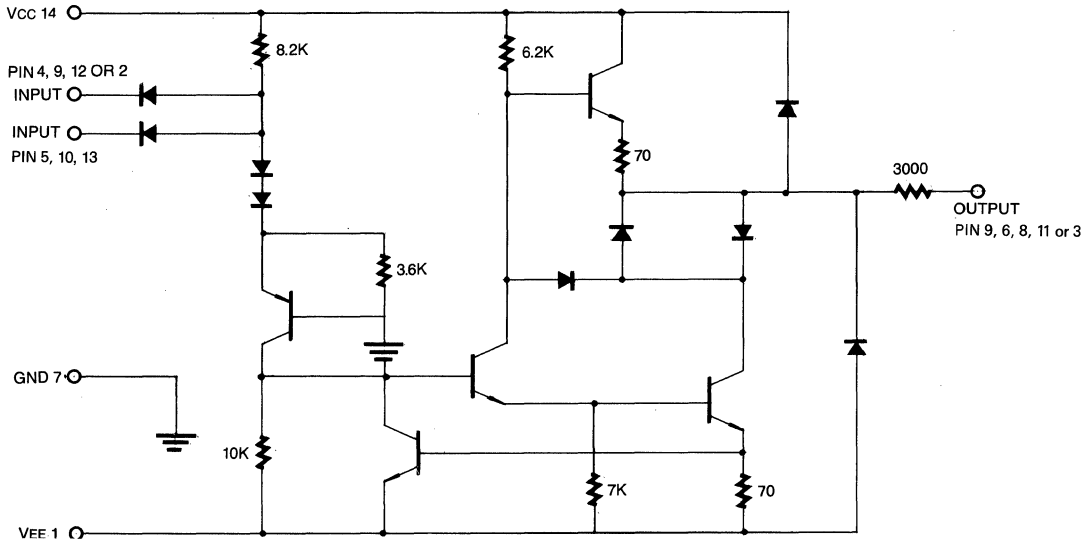
14 Dip Unit: mm



FEATURES

- **Current Limited Output:L ±10mA typ**
- **Power-Off Source Impedance: 300 Ohms min**
- **Simple Slew Rate Control with External Capacitor**
- **Flexible Operating Supply Range**

SCHEMATIC DIAGRAM (1/4 of Circuit Shown)



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 −15	V_{DC}
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	V_{DC}
Output Signal Voltage	V_O	±15	V_{DC}
Power Derating (Package Limitation, Ceramic and Plastic Dual-In-Line Package) Derate Above $T_a = +25°C$	P_D $1/R\theta_{JA}$	1000 6.7	mW mW/°C
Operating Temperature Range	T_a	0 to +75	°C
Storage Temperature Range	Tstg	−65 to +175	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 9.0±10%V, V_{EE} = −9±10%V, T_a = 0 ~ 75°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Input Current 1	I_{I1}	Low Logic State (V_{IL} = 0)		1.0	1.6	mA	1
Input Current 2	I_{I2}	High Logic State (V_{IH} = 5.0V)			10	μA	1
Output Voltage-High Logic State	V_{OH}	V_{IL} = 0.8V, R_L = 3.0KΩ V_{CC} = 9.0V, V_{EE} = −9.0V	6	7		V	2
		V_{IL} = 0.8V, R_L = 3.9KΩ V_{CC} = 13.2V, V_{EE} = −13.2V	9	10.5			
Output Voltage-Low Logic State	V_{OL}	V_{IH} = 1.9V, R_L = 3.0KΩ V_{CC} = 9.0V, V_{EE} = −9.0K	−6	−7		V	2
		V_{IH} = 1.9V, R_L = 3.9KΩ V_{CC} = 13.2V, V_{EE} = −13.2V	−9	−10.5			
Output Short Circuit Current	I_{OS+}	Positive	6	10	12	mA	3
Output Short Circuit Current	I_{OS-}	Negative	−6	−10	−12	mA	3
Output Resistance	R_O	V_{CC} = V_{EE} = 0, IV_O = ±2.0V	300			Ω	
Positive Supply Current (Ri=∞)	I_{CC}	V_{IH} = 1.9V, V_{CC} = +9.0V		15	20	mA	5
		V_{IL} = 0.8V, V_{CC} = +9.0V		4.5	6		
		V_{IH} = 1.9V, V_{CC} = +12V		9	25		
		V_{IL} = 0.8V, V_{CC} = +12V		5.5	7		
		V_{IH} = 1.9V, V_{CC} = +15V			34		
		V_{IL} = 0.8V, V_{CC} = +15V			12		
	I_{EE}	V_{IH} = 1.9V, V_{EE} = −9.0V		−13	−17	mA	5
		V_{IL} = 0.8V, V_{EE} = −9.0V			−500	μA	
		V_{IH} = 1.9V, V_{EE} = −12V		−18	−23	mA	
		V_{IL} = 0.8V, V_{EE} = −12V			−500	μA	
		V_{IH} = 1.9V, V_{EE} = −15V			−34	mA	
		V_{IL} = 0.8V, V_{EE} = −15V			−2.5	mA	
Power Consumption	P_C	V_{CC} = 9.0V, V_{EE} = −9.0V			333	mW	
		V_{CC} = 12V, V_{EE} = −12V			576		

* Maximum package power dissipation may be exceeded if all outputs are shorted simultaneously.

SWITCHING CHARACTERISTICS

(V_{CC} = 9.0±1%V, V_{EE} = −9±1%V, T_a = 0 ~ 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Propagation Delay Time	t_{PLH}	Z_i = 3.0K and 15pF		275	350	nS	6
Fall Time	t_{THL}	Z_i = 3.0K and 15pF		45	75	nS	
Rise Time	t_{TLH}	Z_i = 3.0K and 15pF		55	100	nS	

FIGURE 1 — INPUT CURRENT

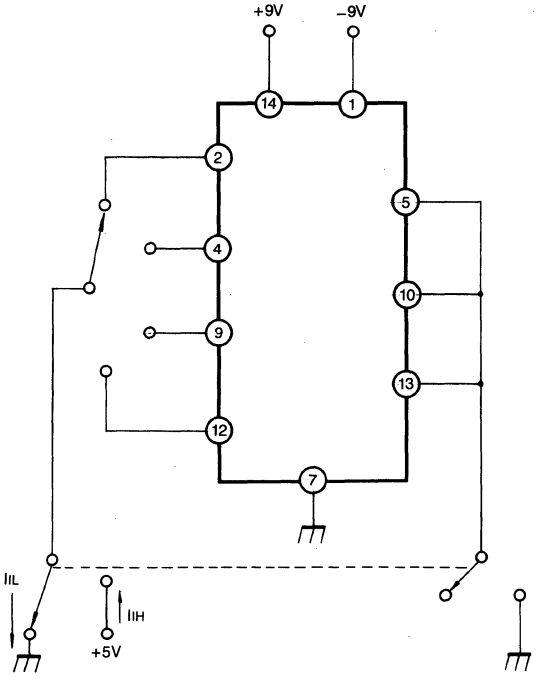


FIGURE 2 — OUTPUT VOLTAGE

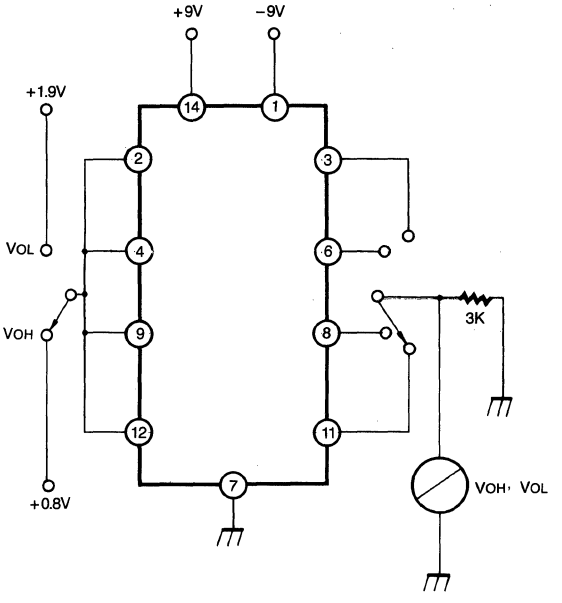


FIGURE 3 —
OUTPUT SHORT CIRCUIT CURRENT

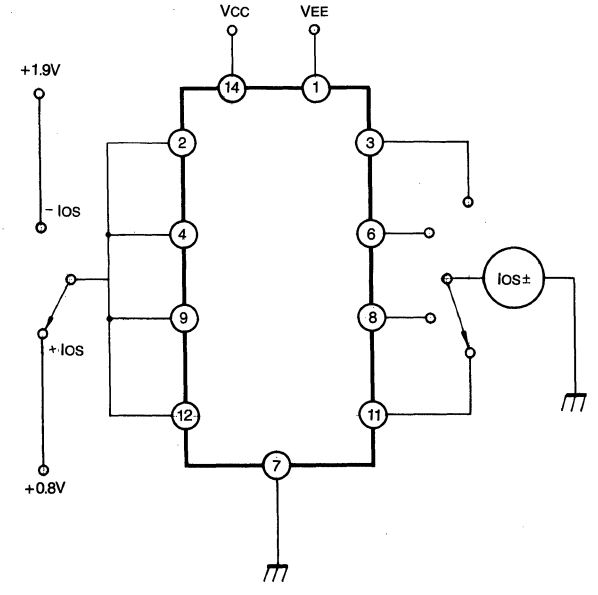


FIGURE 4 —
OUTPUT RESISTANCE (POWER OFF)

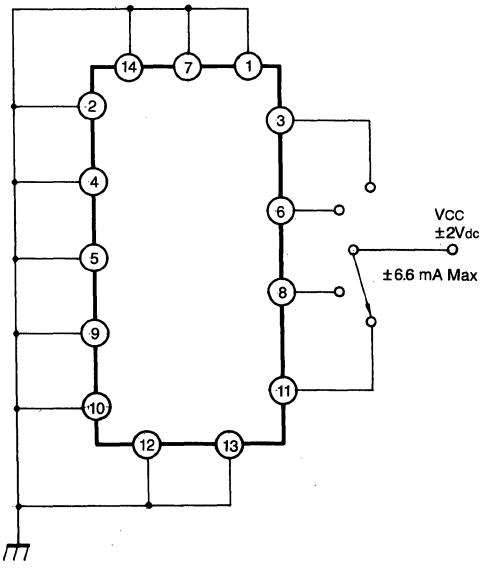


FIGURE 5 — POWER SURPPLY CURRENTS

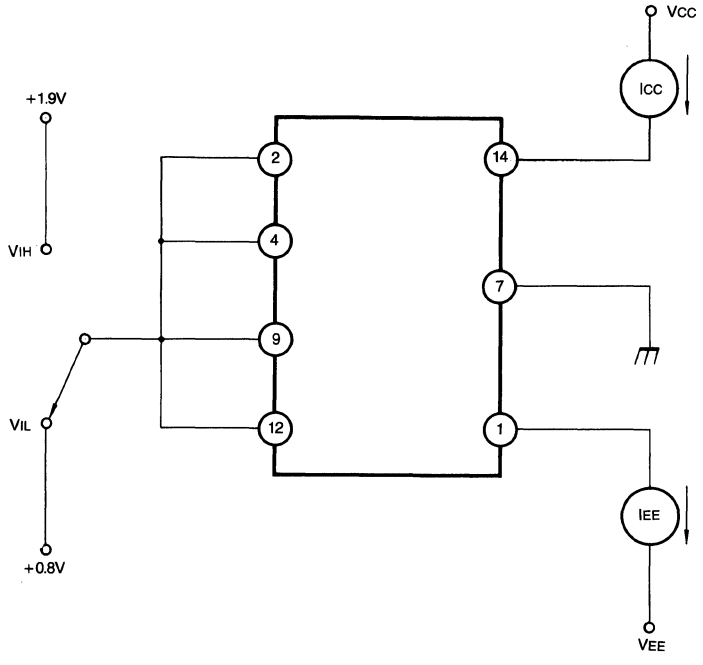
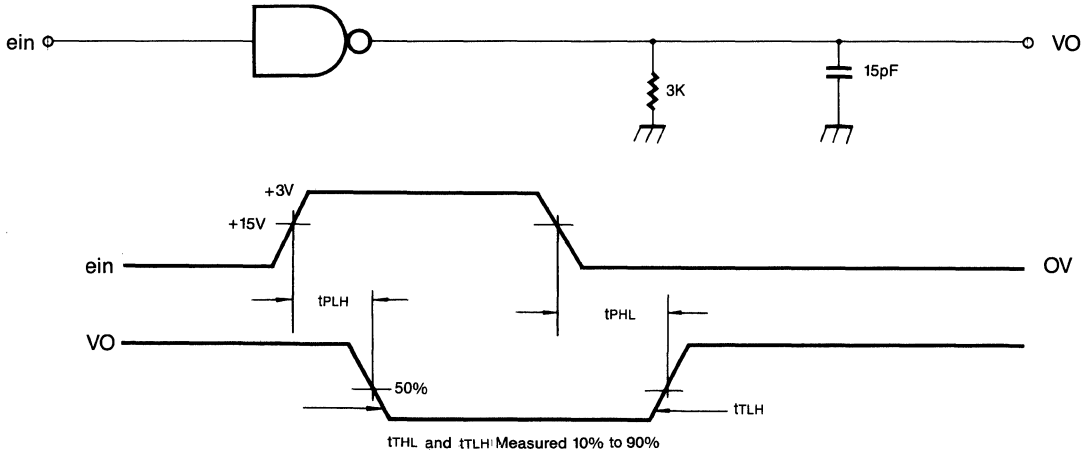


FIGURE 6 — SWITCHING RESPONSE



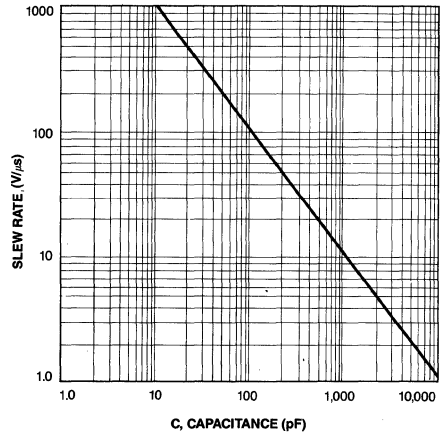
APPLICATION INFORMATION

The Electronic Industries Association (EIA) RS232C specification detail the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

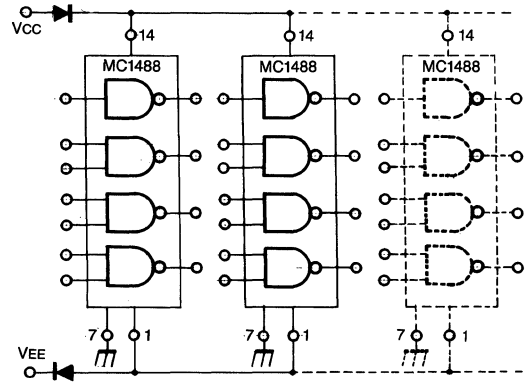
The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the

FIGURE 12 — SLEW RATE V_S CAPACITANCE FOR I_{SC} = 10mA



device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330-pF capacitor on each output will guarantee a worst case slew rate or 30 volts per microsecond.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geq 9.0$ V:$V_{EE} \leq -9.0$V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low



impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting — this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300mV above ground MOS input level limit.

2. Power-Supply Range — as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately −2.5 volts to the minimum specified the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

FIGURE 14 — MDTL/MTTL-TO-MOS TRANSLATOR

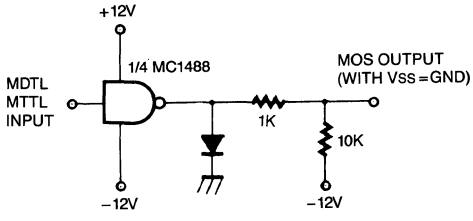


FIGURE 15 — LOGIC TRANSLATOR APPLICATIONS

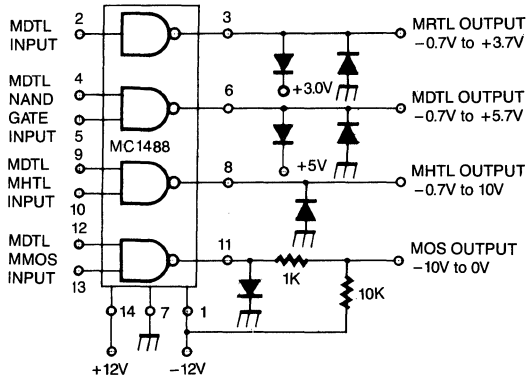


FIGURE 7 — TRANSFER CHARACTERISTICS
V_S POWER-SUPPLY VOLTAGE

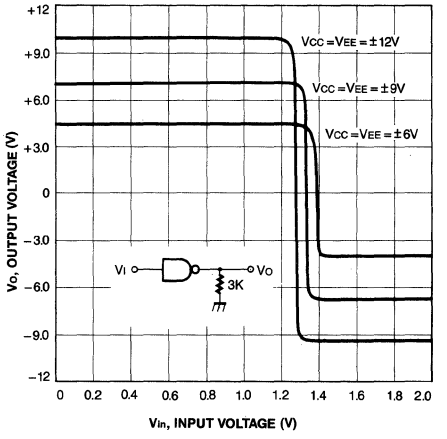


FIGURE 8 — SHORT CIRCUIT OUTPUT CURRENT
V_S TEMPERATURE

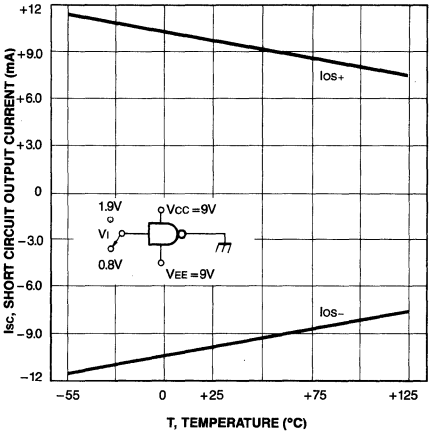


FIGURE 9 — OUTPUT SLEW RATE V_S LOAD CAPACITANCE

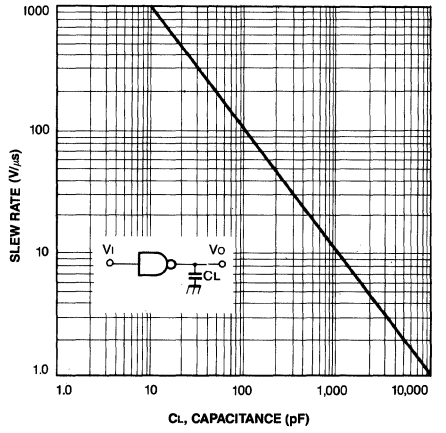


FIGURE 10 — OUTPUT VOLTAGE AND CURRENT LIMITING CHARACTERISTICS

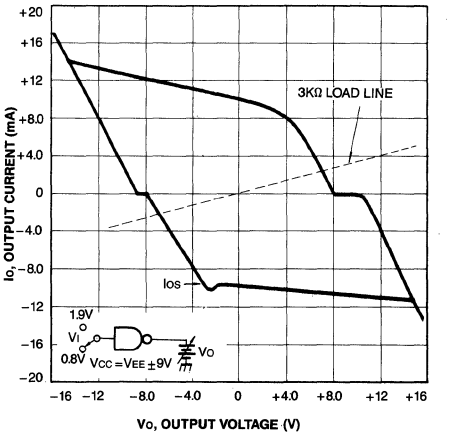
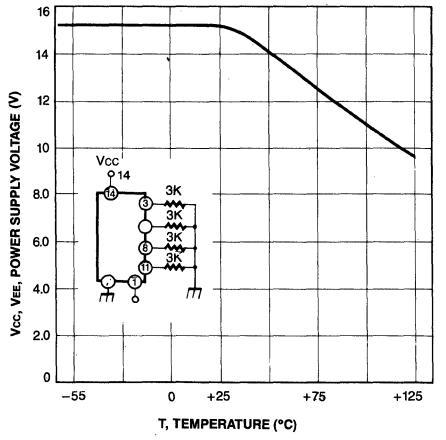


FIGURE 11 — MAXIMUM OPEATING TEMPERATURE
V_S POWER SUPPLY VOLTAGE



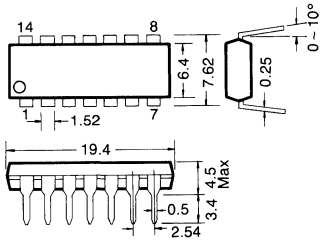
QUAD LINE RECEIVER

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

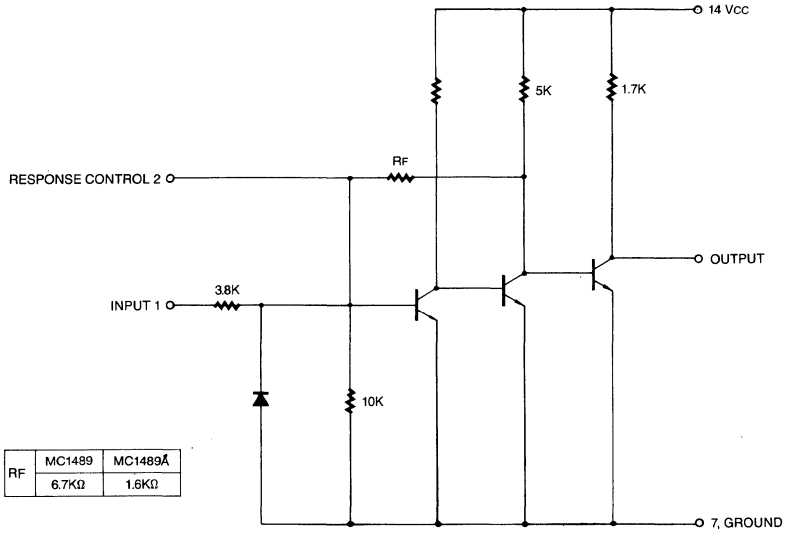
FEATURES

- **Input Resistance — 3.0K to 7.0 kilohms**
- **Input Signal Range — ±30 Volts**
- **Response Control**
  - **a) Logic Threshold Shifting**
  - **b) Input Noise Filtering**

14 Dip **Unit: mm**



SCHEMATIC DIAGRAM
(1/4 OF CIRCUIT SHOWN)



RF	MC1489	MC1489A
	6.7KΩ	1.6KΩ

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	V_{DC}
Input Voltage Range	V_{IR}	±30	V_{DC}
Output Load Current	I_L	20	mA
Power Dissipation Derate Above $T_a = +25°C$	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Temperature	T_a	0 to +75	°C
Storage Temperature	Tstg	−65 to +175	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0±10%V, T_a = 0 ~ 75°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Positive Input Current	I_{IH}	V_{IH} = 5V	3.6		8.3	mA
		V_{IH} = 3.0V	0.43			
Negative Input Current	I_{IL}	V_{IL} = − 25V	− 3.6		− 8.3	mA
		V_{IL} = − 3.0V	− 0.43			
Input Turn-On Thereshold Voltage MC1489 MC1489A	V_{IH}	T_a = 25°C, $V_{OL} \leq$ 0.45V	 1.0 1.75	 1.95	 1.5 2.25	V
Input Turn-Off Threshold Voltage	V_{IL}	T_a = 25°C, $V_{OH} \geq$ 2.5V, I_L = 0.5mA	0.75		1.25	V
Output Voltage High	V_{OH}	V_{IH} = 0.75V, I_L = −0.5mA	2.5	4.0	5.0	V
		Input Open, I_L = − 0.5mA	2.5	4.0	5.0	
Output Voltage Low	V_{OL}	V_{IL} = 3.0V, I_L = 10mA		0.2	0.45	V
Output Short Circuit Current	I_{OS}			− 3.0	− 4.0	mA
Power Supply Current	I_{CC}	All gates "on", I_{OUT} = 10mA, V_{IH} = 5.0V		16	26	mA
Power Consumption	P_C	V_{IH} = 5.0V		80	130	mW

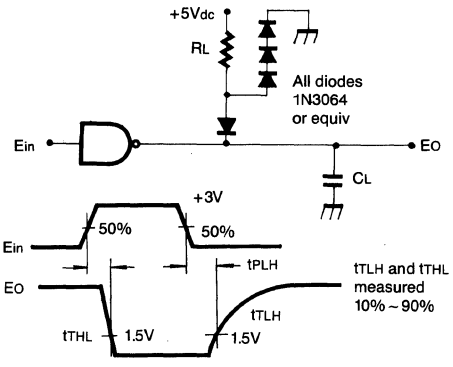
SWITCHING CHARACTERISTICS

(V_{CC} = 5.0±1%V, T_a = 25°C, See Fig. 1)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time	t_{PLH}	R_L = 3.9KΩ		25	85	nS
Rise Time	t_{TLH}	R_L = 3.9KΩ		120	175	nS
Propagation Delay Time	t_{PHL}	R_L = 390KΩ		25	50	nS
Fall Time	t_{THL}	R_L = 390KΩ		10	20	nS

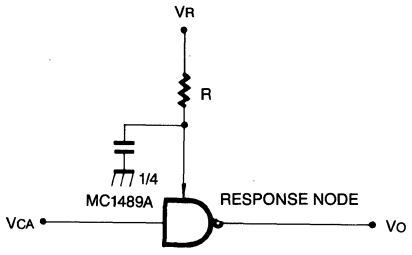
TEST CIRCUIT

Fig 1 — SWITCHING RESPONSE



CL=15pF=total parasitic capacitance, which includes probe and wiring capacitances

Fig 2 — RESPONSE CONTROL NODE



C, capacitor is for noise filtering
R, reistor is for threshold shifting

TYPICAL CHARACTERISTICS

(VCC=5.0 Vdc Ta=+25°C unless otherwise noted)

Fig. 8 — TYPICAL TURN-ON THRESHOLD V_S CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

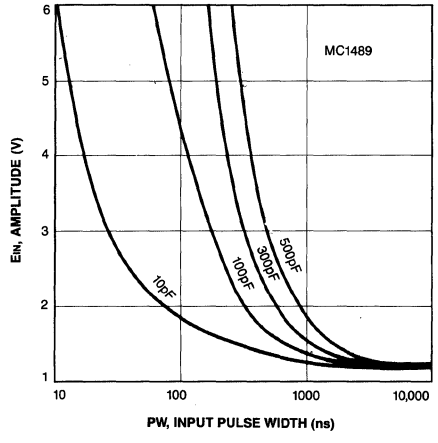
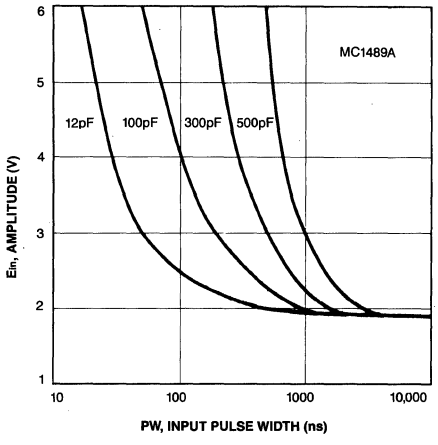


Fig. 9 — TYPICAL TURN-ON THRESHOLD V_S CAPACITANCE FROM RESPONSE CONTROL PIN TO GND



APPLICATION INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between −3.0 and −25 volts as a Logic "1" and inputs between +3.0 and +25 volts as a Logic "0". On some interchange leads, an open circuit of power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or Logic "1". For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for typical hysteresis of 250mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

Fig. 10 — TYPICAL TRANSLATOR APPLICATION — MOS TO DTL OR TTL

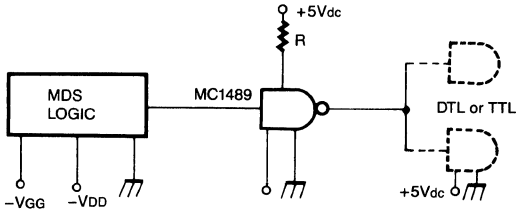


Fig. 11 — TYPICAL PARALLELING OF TWO MC1489/A RECEIVERS TO MEET RS-232C

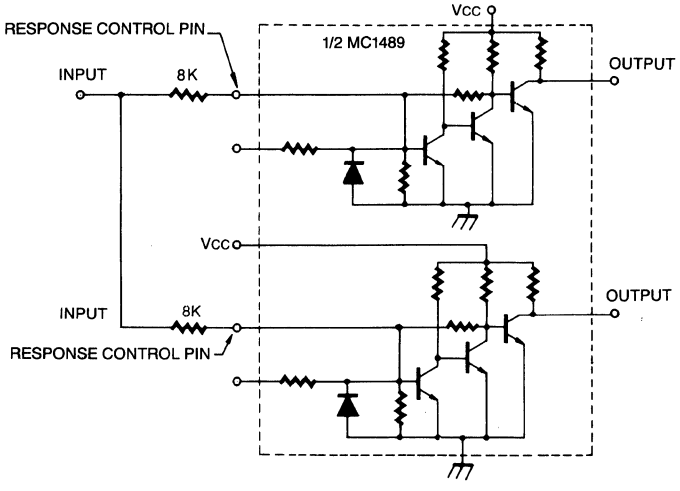


Fig. 3 — INPUT CURRENT

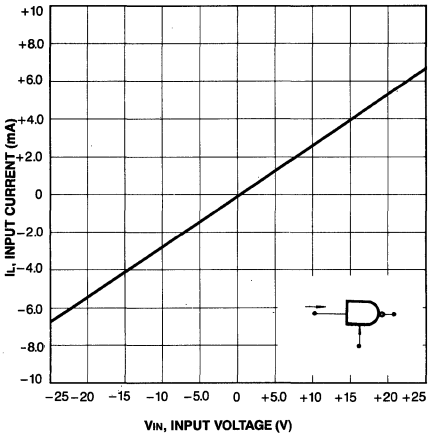


Fig. 4 — MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

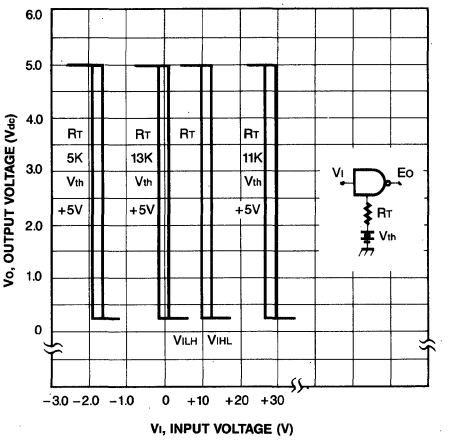


Fig. 5 — MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

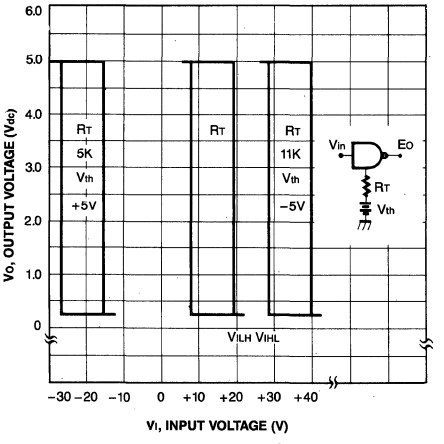


Fig. 6 — INPUT THRESHOLD VOLTAGE Vs. TEMPERATURE

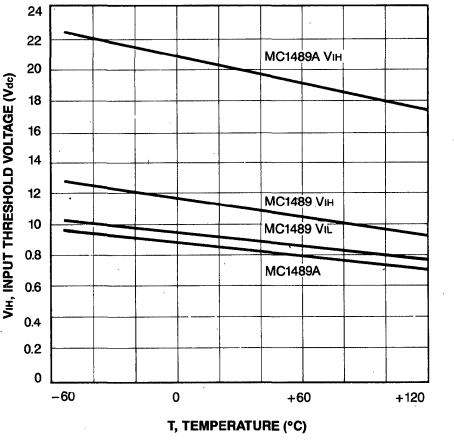
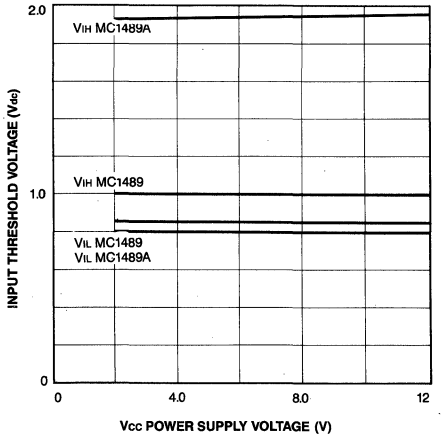


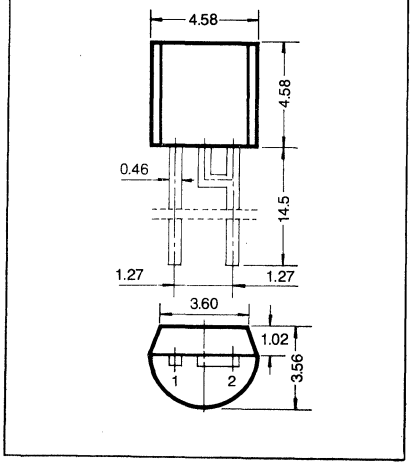
Fig. 7 — INPUT THRESHOLD Vs. POWER SUPPLY VOLTAGE



SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT VOLTAGE STABILIZAER FOR ELECTRONIC TUNER

The KA33V Is a monolithic integrated circuit voltage stabilizer especially designed as voltage supplier for varactor diode.

TO-92 Unit: mm



FEATURES

- **Low Temperature Coefficient**
- **Low Dynamic Resistance**
- **Typical Reference Voltage**

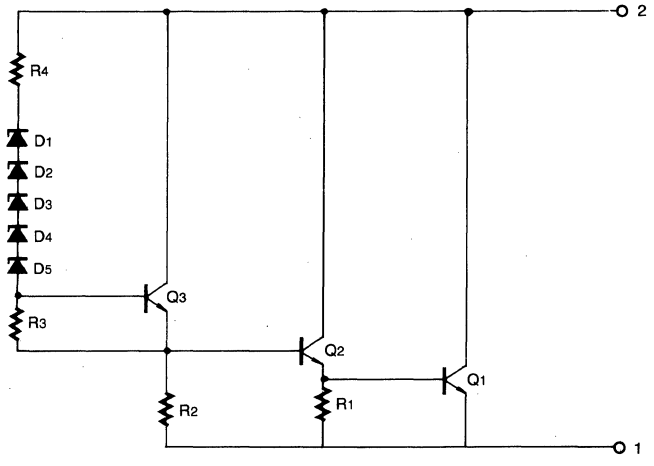
ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Rating	Unit
Zener Current	I_Z	10	mA
Power Dissipation	P_d	200	mW
Operating Ambient Temperature-Range	Topt	−20 ~ 75	°C
Storage Temperature Range	Tstg	−40 ~ 125	°C

ELECTRICAL CHARACTERISTICS (T_a =25°C)

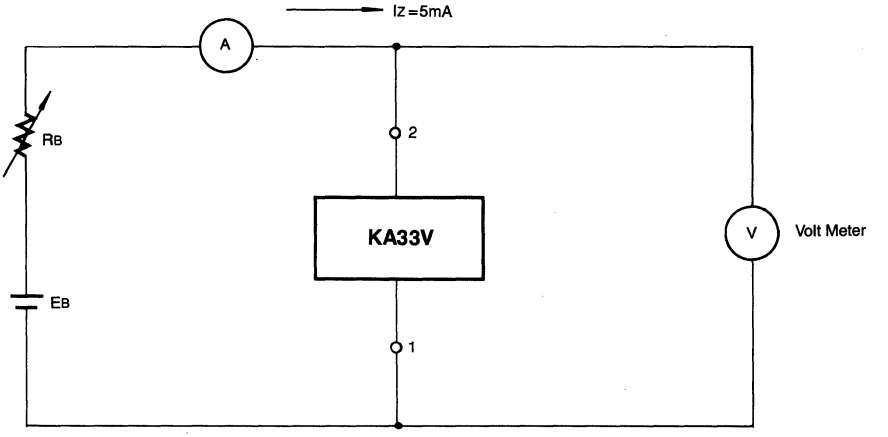
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Stabilizer Voltage	V_Z	I_Z=5mA	31		35	V
Stabilizer Voltage-Temperature Drift	$\Delta V_Z/T$	I_Z=5mA T_a=−20 to 75°C	−1	0	1	mV/°C
Dynamic Resistance	r_Z	I_Z=5mA, f=1KHz		10	25	

EQUIVALENT CIRCUIT

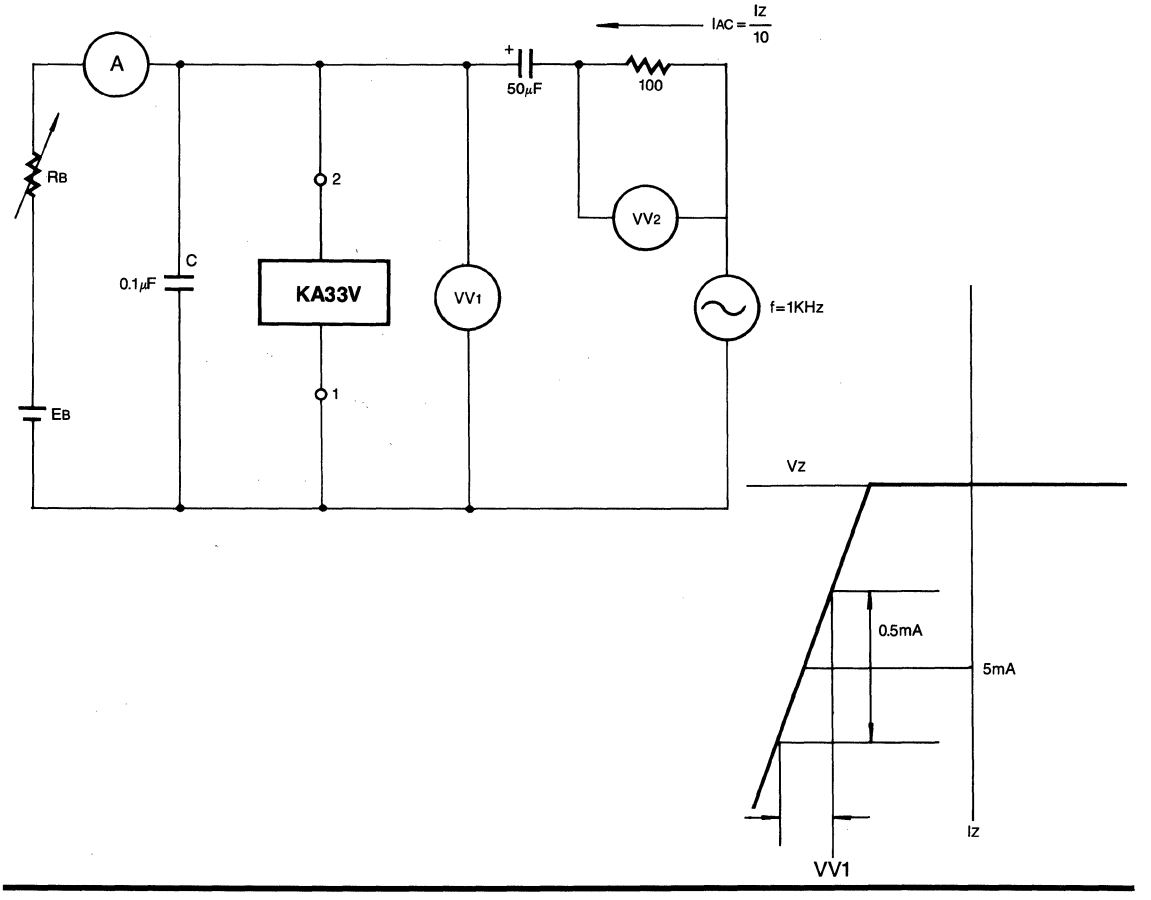


MEASURING CIRCUITS

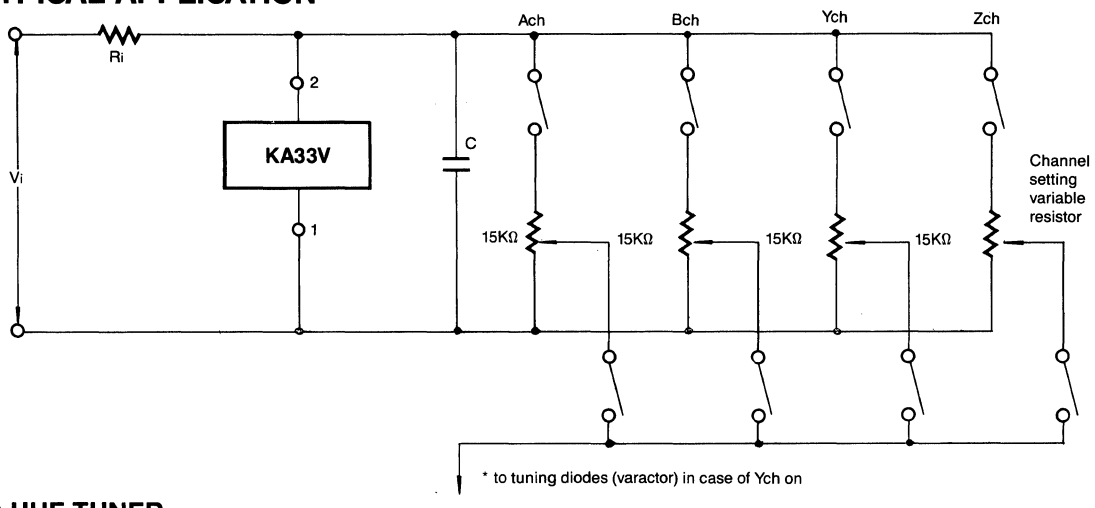
Measuring Circuit for Stabilized Voltage Vz



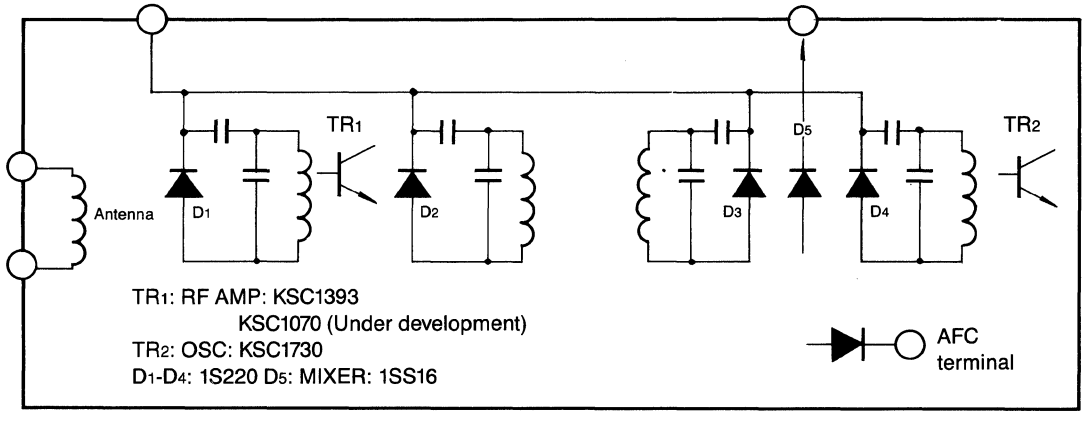
Measuring Circuit for Dynamic Resistance



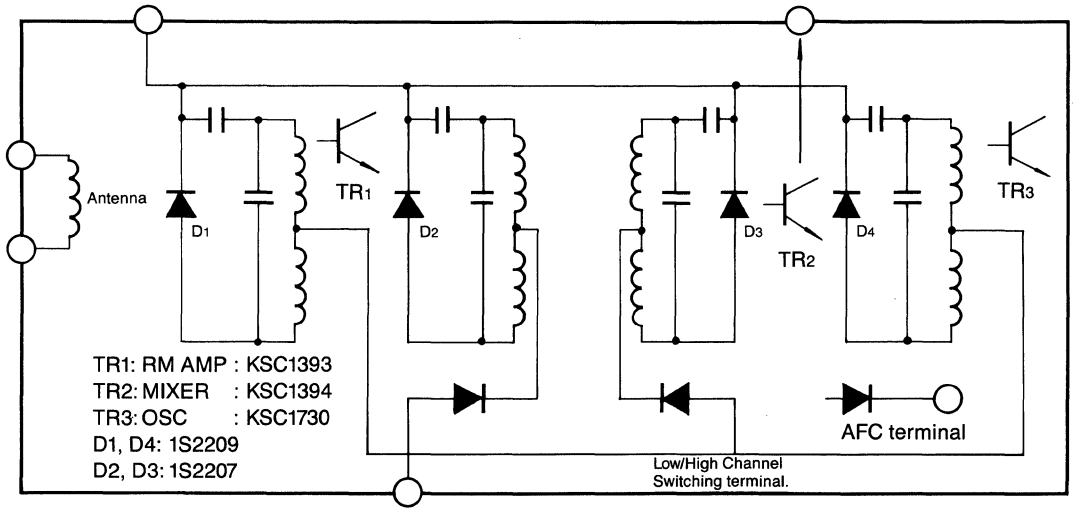
TYPICAL APPLICATION



(1) UHF TUNER

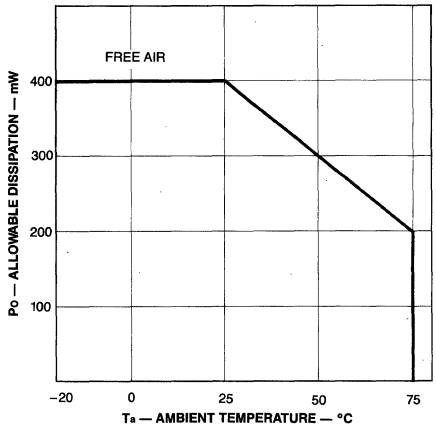


(2) VHF TUNER



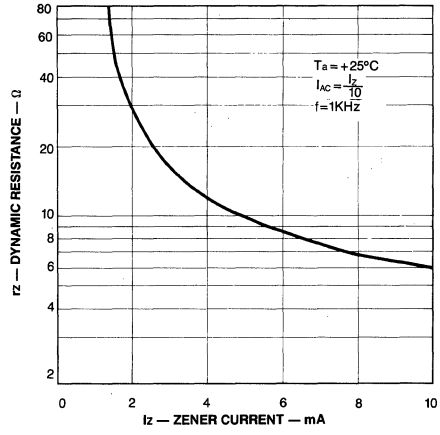
POWER-TEMPERATURE DERATING CURVE

ALLOWABLE DISSIPATION vs. AMBIENT TEMPERATURE

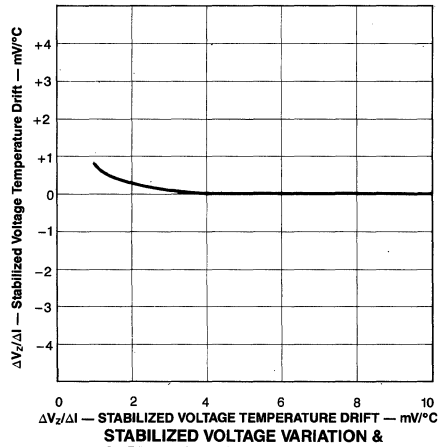


TYPICAL CHARACTERISTIC CURVES (Ta=25°C)

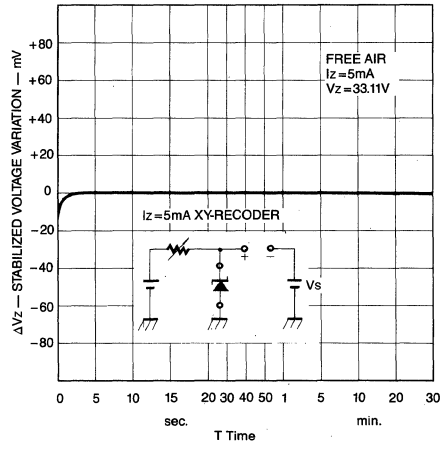
DYNAMIC RESISTANCE vs. ZENER CURRENT



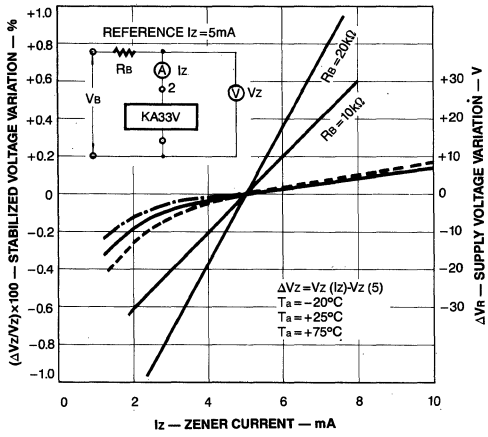
STABILIZED VOLTAGE TEMPERATURE DRIFT vs. ZENER CURRENT

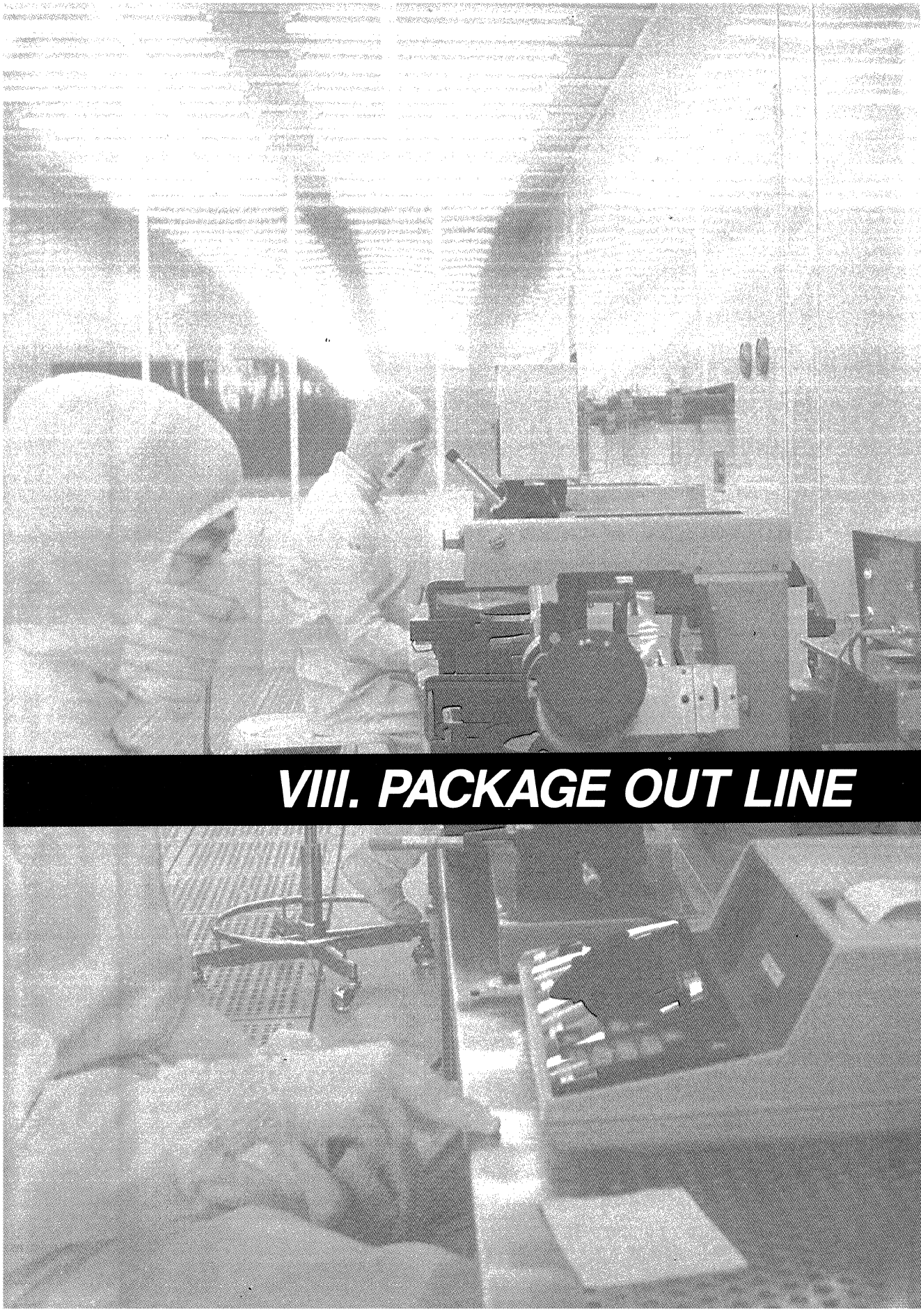


STABILIZED VOLTAGE VARIATION vs. TIME



STABILIZED VOLTAGE VARIATION & SUPPLY VOLTAGE VARIATION vs. ZENER CURRENT

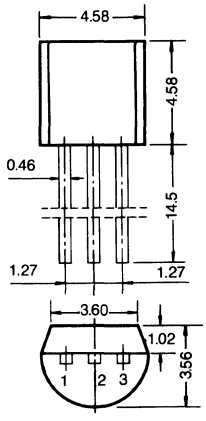




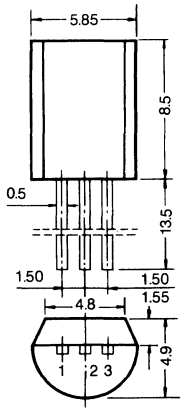
VIII. PACKAGE OUT LINE

PACKAGE OUT LINE

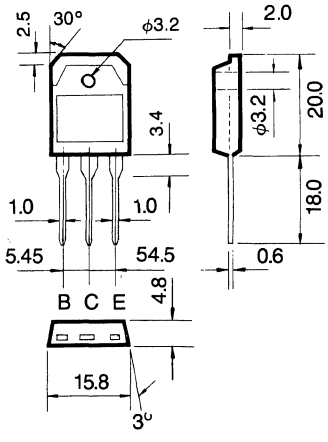
TO-92 Unit: mm



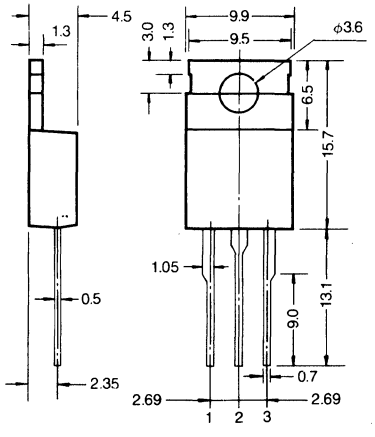
TO-92L Unit: mm



TO-3P **Unit: mm**



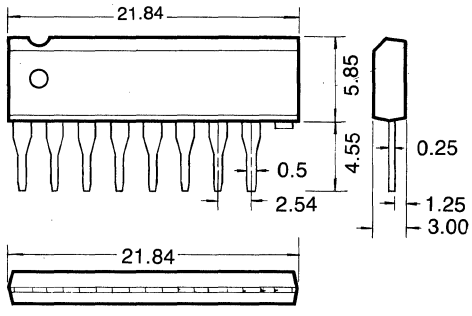
TO-220 Unit: mm



PACKAGE OUT LINE

8 Sip

Unit: mm



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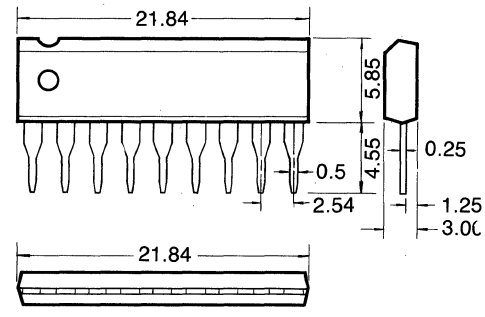
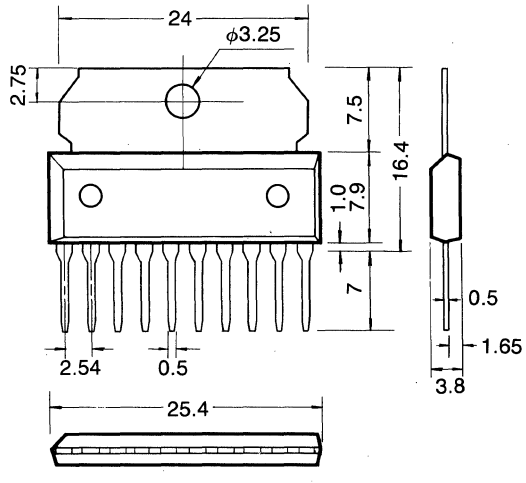


10 Sip H/S

Unit: mm



12 Sip H/S

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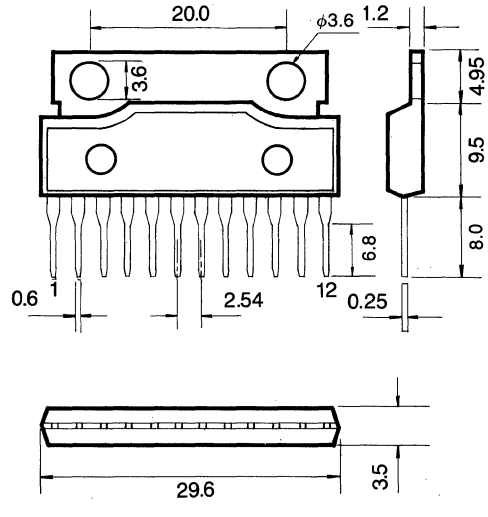

PACKAGE OUT LINE

8 Dip

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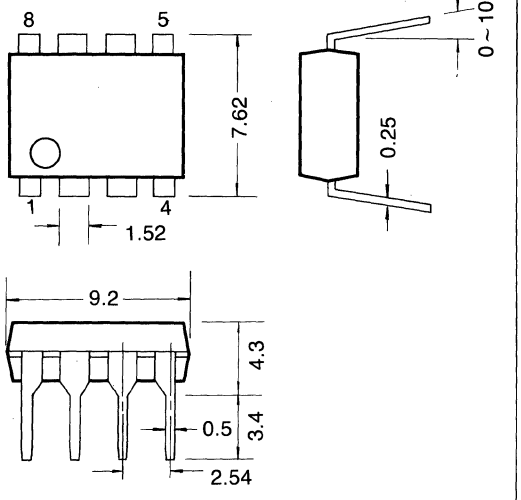

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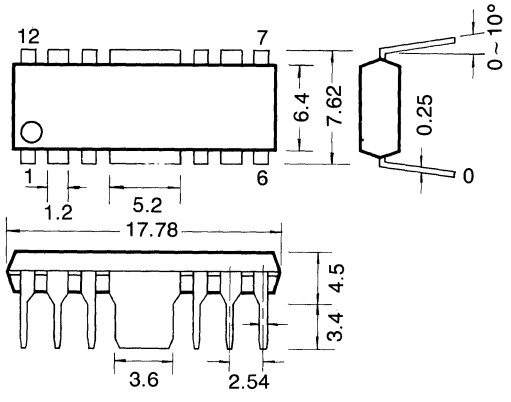

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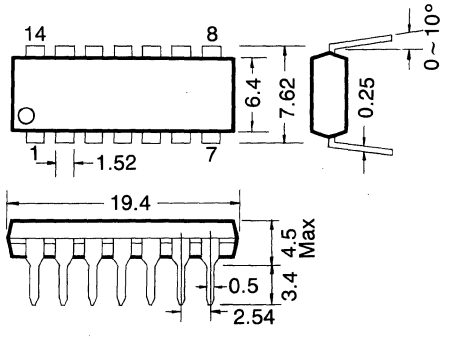

14 Dip H.S

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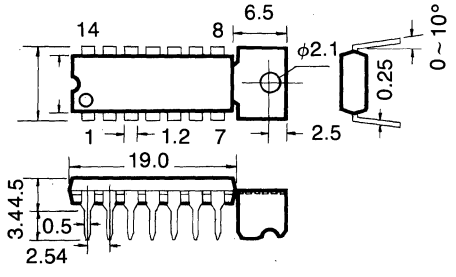
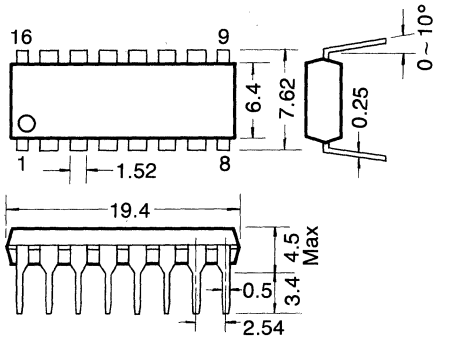


PACKAGE OUT LINE

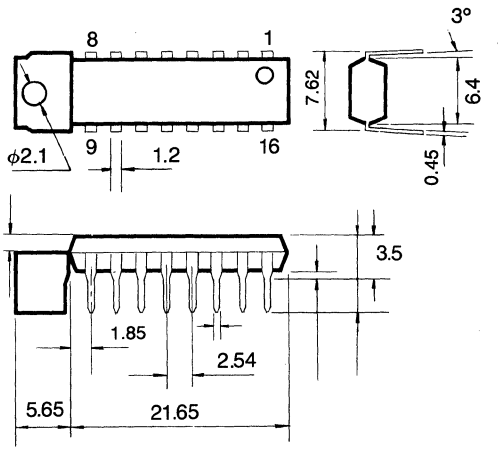
16 Dip

Unit: mm



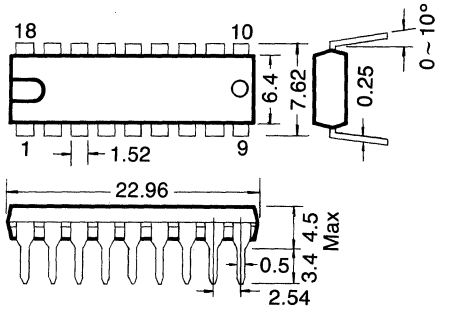
16 Dip H/S

Unit: mm



18 Dip

Unit: mm



20 Dip

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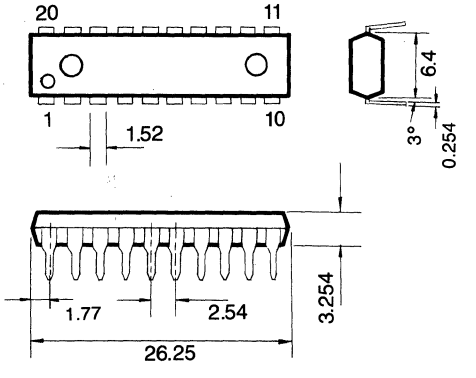
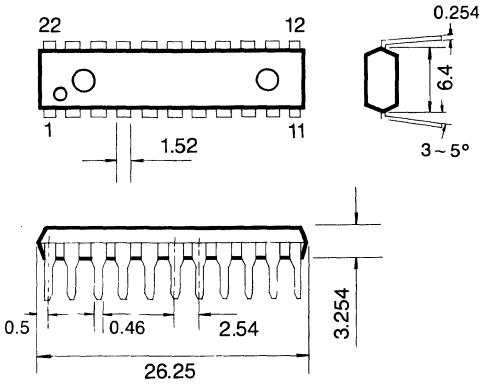


PACKAGE OUT LINE

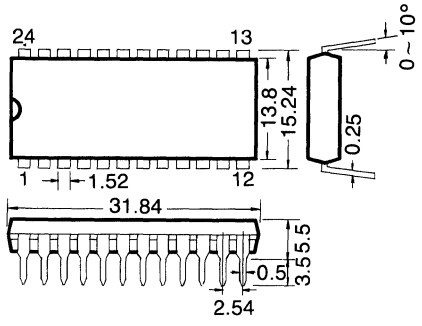
22 Dip

Unit: mm



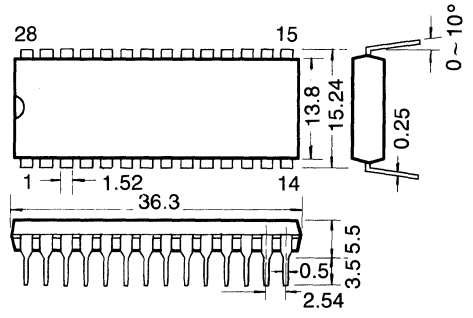
24 Dip

Unit: mm



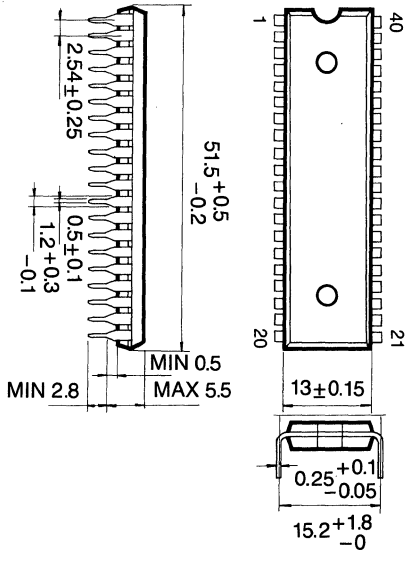
28 Dip

Unit: mm



40 Dip

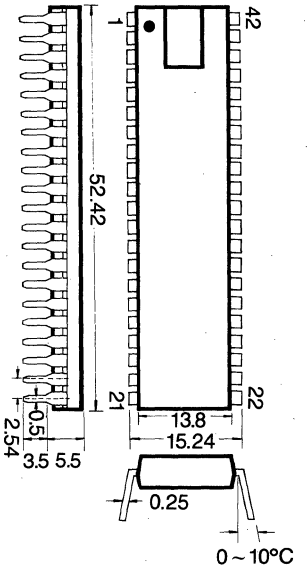
Unit: mm



PACKAGE OUT LINE

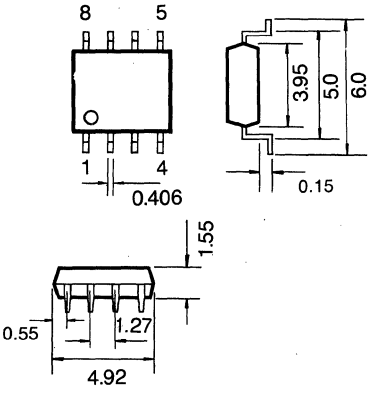
42 Dip

Unit: mm

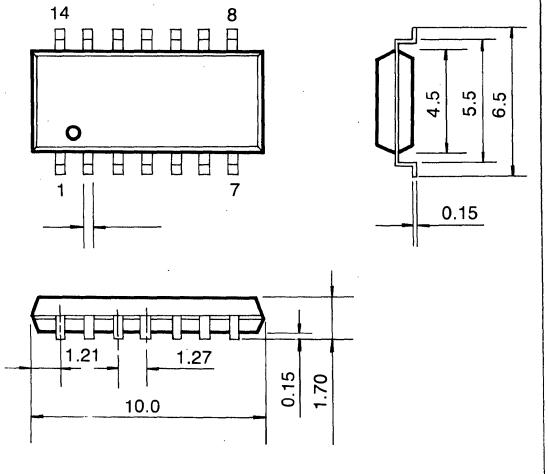


8 SOP

Unit: mm

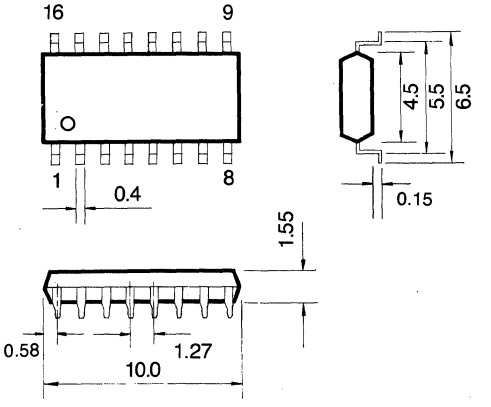


14 SOP



16 SOP

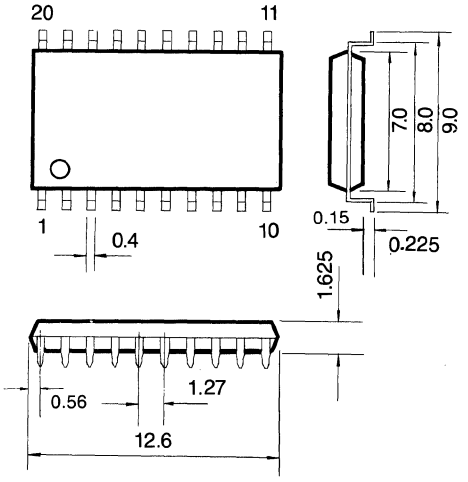
Unit: mm



PACKAGE OUT LINE

20 SOP

Unit: mm



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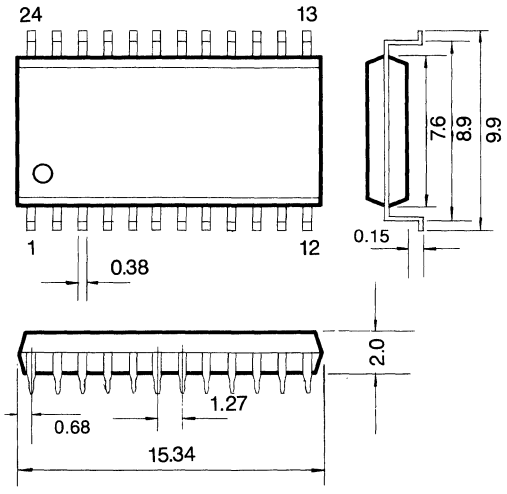
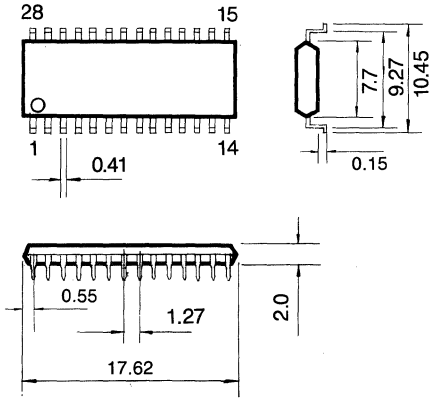
Unit: mm



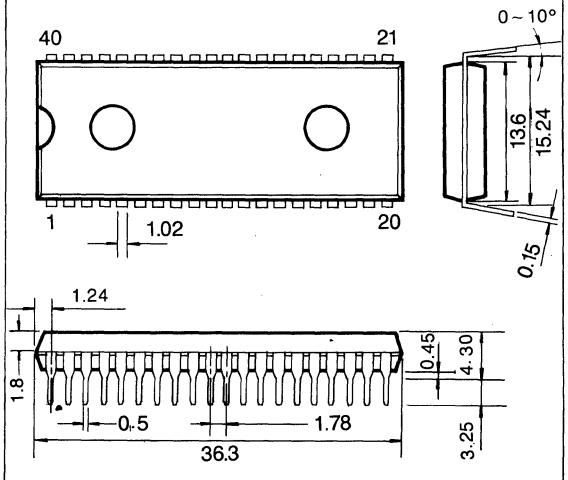
28 SOP

Unit: mm



40 SOP

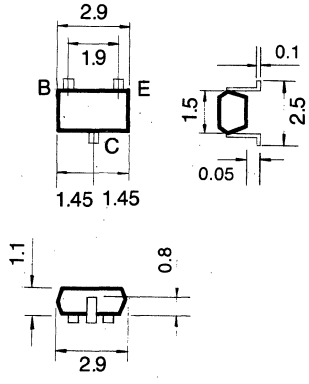
Unit: mm



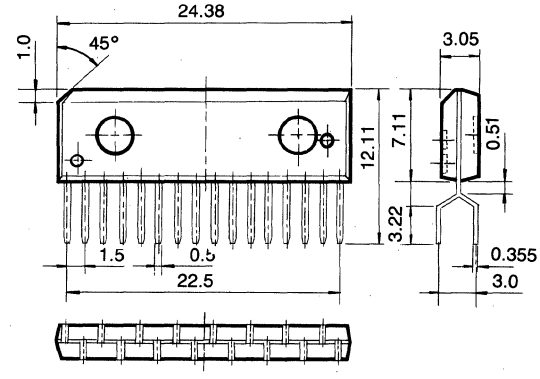
PACKAGE OUT LINE

SOT-23

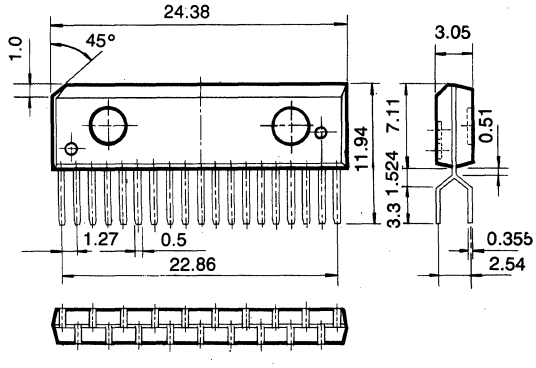
Unit: mm



16 ZIP



19 ZIP



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