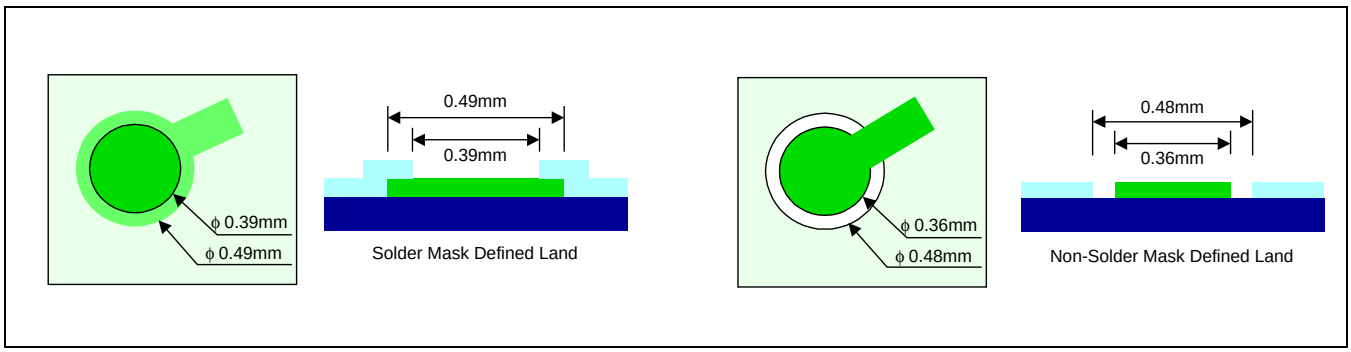
ROUTING GUIDE (PRELIMINARY)

1. LAND SIZE

It is of great importance to properly design the PCB land pad of FBGA package in terms of productivity of mass-produced board. It is better to match the size of PCB land pad with that of FBGA package. There are two methods for forming the land in PCB.

One is the solder mask defined method: The land copperplate is made bigger than its real size, and the solder mask is made in a desired size to determine the land area. Through this method, it is possible to accurately form the size of land, but relatively routing space is reduced because of large area of copperplate.

The other is the non-solder mask defined method: Land size is made smaller than the solder mask to form the land. The Land size is determined according to etching time generated in the course of producing PCB. This method is a little better for routing because of small area of copperplate, compared to the SMD method.



2. VIA HOLE

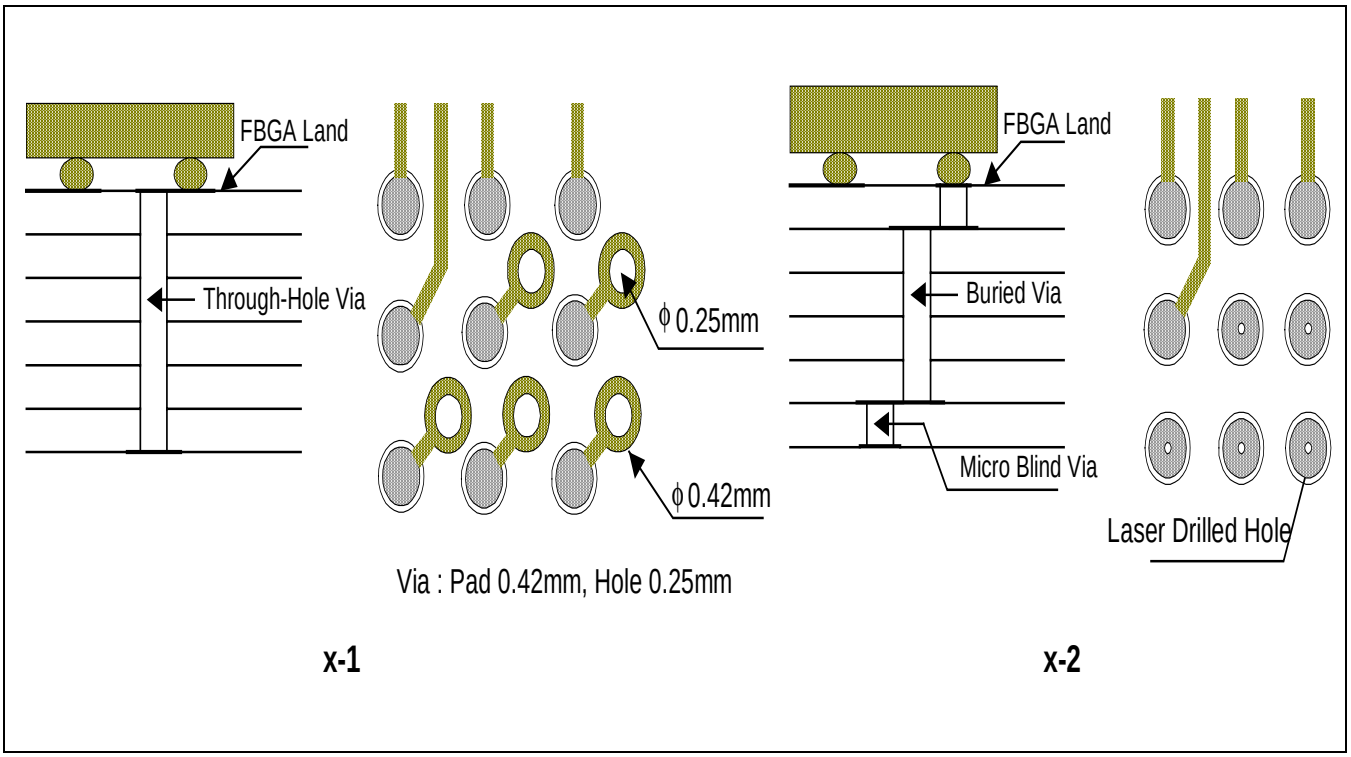
In multi-layered PCB, the via is the only method to enable electrical connection of signals between layers. Using the via properly facilitates the layout of parts. In case of highly integrated board, Via size becomes more important. It is because the small-sized via allows more routing space and the increased insertion rate of parts.

The through-hole via is the most frequently used type of via. However, it is not suitable for PCB routing and component layout since it occupies much area of PCB. In particular, if the through-hole via is used for FBGA package, the via hole matrix is formed on the opposite side of PCB, causing restriction in the layout of trace and component. (See Figure x-1)

If you want to facilitate routing on Board and increase the area of insertion for parts, it is more useful to use the following two via techniques.

Micro Blind Via: Possible to minimize the size of via by forming 'via' using very small-sized laser-drill (usually 4um). However, it is possible to connect one side of PCB only to the neighboring layer. When using the FBGA package, the user can get much space for routing, if the combination of PCB land and via is used (See Figure x-2). In addition, it facilitates both-side insertion because the via does not appear on the opposite side of PCB.

Buried Via: The via technique allowing connection from inner layer to inner layer of PCB, which is buried under the external surface of PCB. It is also used to interconnect Micro blind vias. (See Figure x-2)

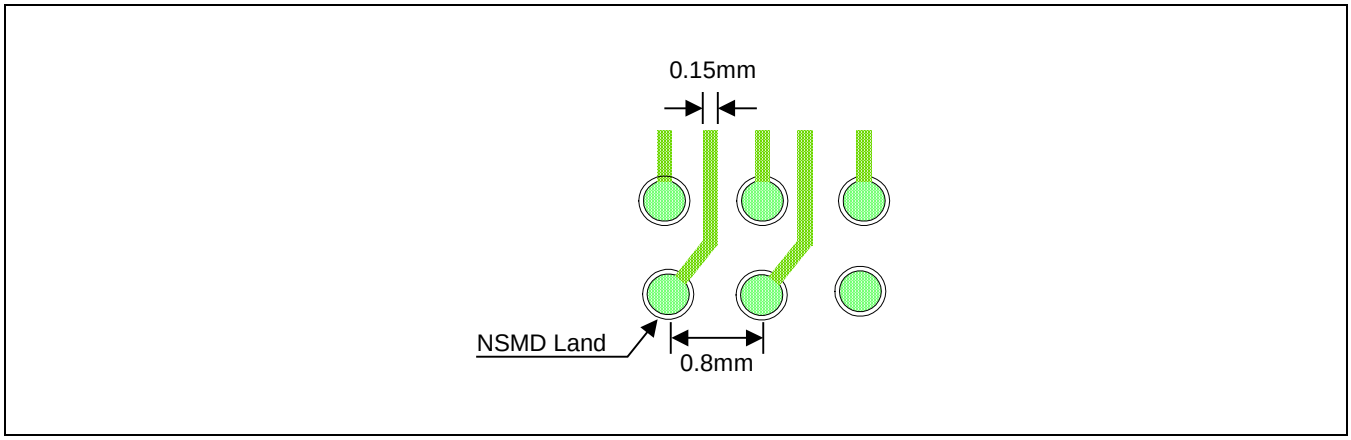


3. ROUTING GUIDE

3.1 TRACE WIDTH & CLEARANCE

This section describes how to perform routing while properly maintaining the width and interval of trace in FBGA package land.

It is required to extract many signal traces from narrow space and it is not easy for each trace to maintain desired characteristic impedance. Using too narrow trace might cause a problem in PCB manufacture and increase the costs of PCB manufacture. The following figure illustrates the width and interval of trace the user can observe when using the land pad as explained in the previous chapter. In normal case, we recommend the trace width of 0.1 ~ 0.15 mm.



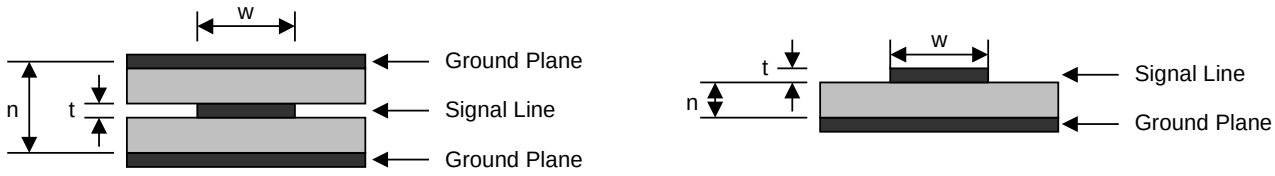
3.2 TRANSMISSION LINE IMPEDANCE

This section describes two transmission line impedance's that can be implemented on the PCB.

Strip line: The signal line is inserted between upper and lower layer power planes in order to implement transmission line. It is advantageous in that clean signals can be transmitted because the power plane has shield effects on both sides, but it must pass the via in order to connect to the element.

Microstrip line: The signal line is placed on the outer layer and ground plane is placed at the next neighboring layer. This is easier to implement than the Strip line.

The following example illustrates characteristic impedance of the two transmission lines.



Transmission line capacitance, Inductance, Z0 and TPD can be calculated with PCB size and material dielectric constant.

For Stripline

$$Z_0 = \frac{60}{\sqrt{\varepsilon_R}} \ln \frac{4h}{0.67\pi w\,(0.8 + \frac{t}{w})}\ \Omega$$

$$t_{PD} = 1.017\sqrt{\varepsilon_R}\ ns/ft$$

$$C_0 = 1000\,\frac{t_{PD}}{Z_0}\ pF/ft$$

$$L_0 = Z_0^2 C_0\ pH/ft$$

For Microstrip

$$Z_0 = \frac{87}{\sqrt{\varepsilon_R + 1.41}} \ln \frac{5.98h}{0.8w + t}\ \Omega$$

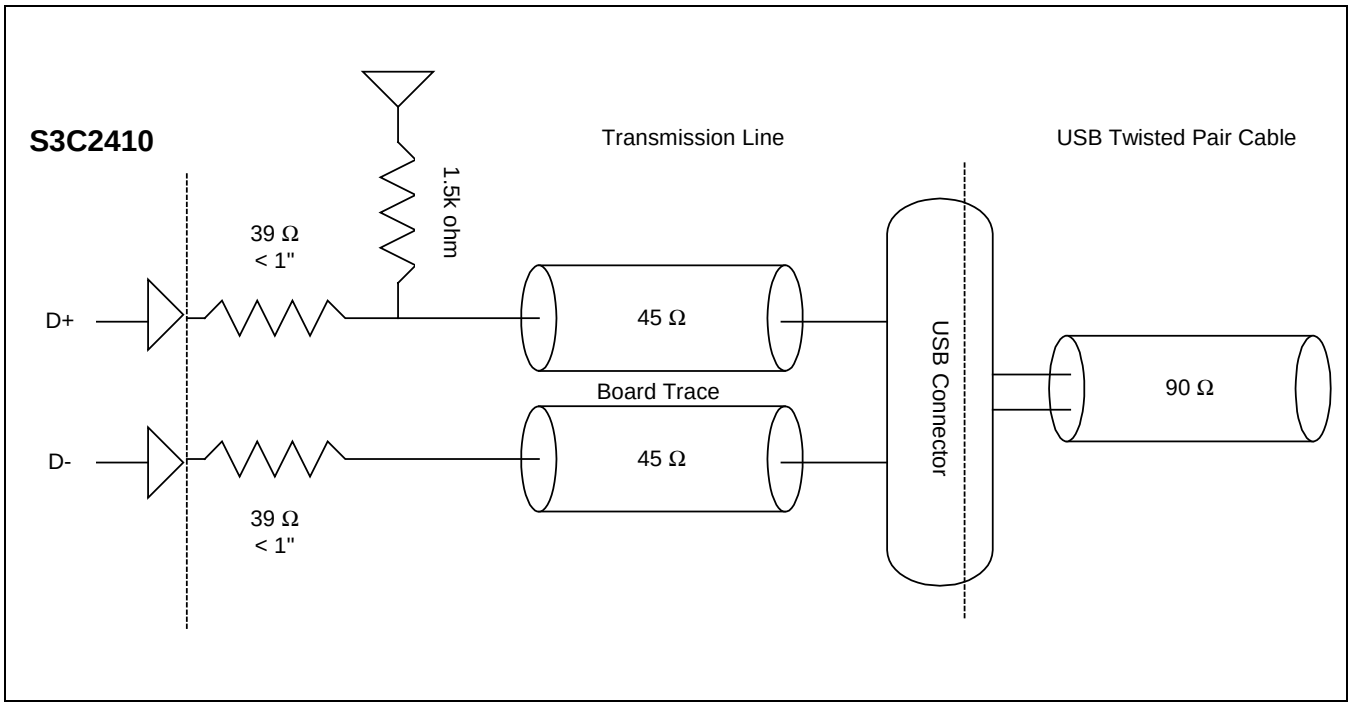
$$t_{PD} = 1.017\sqrt{0.457\varepsilon_R + 0.67}\ ns/ft$$

$$C_0 = 1000\,\frac{t_{PD}}{Z_0}\ pF/ft$$

$$L_0 = Z_0^2 C_0\ pH/ft$$

3.3 USB SIGNAL ROUTING

The following figure illustrates the recommended USB circuit.



— As USB signal is operated in differential mode and most of chip sets are composed of differential 90 ohm characteristic impedance, it is required to design the circuit with 90 ohm using the impedance calculator.

— As USB signal is bi-directional, it is required to perform parallel termination at the same impedance as characteristic impedance on both sides of Transmitter and Receiver.

— D+/D– Trace must be set to 45 Ohm Impedance and the length of Trace must be equal.

— To prevent cross-talk, D+/D– neighboring signals must be separated more than 2 times the USB D+/D– signal interval.

— If possible, impedance matching resistor and pull-up resistor must be placed closer to the S3C2410 D+/D– pin.

3.4 GUIDANCE NOTES FOR ROUTING

— All the SDRAM signals (nSCS, nSRAS, nSCAS, DQMn, SCKE, SCLK, ADDR and DATA) have to be similar in length. By our lab test result, this PCB routing method has enhanced the SDRAM I/O voltage margin up to 3.3V.

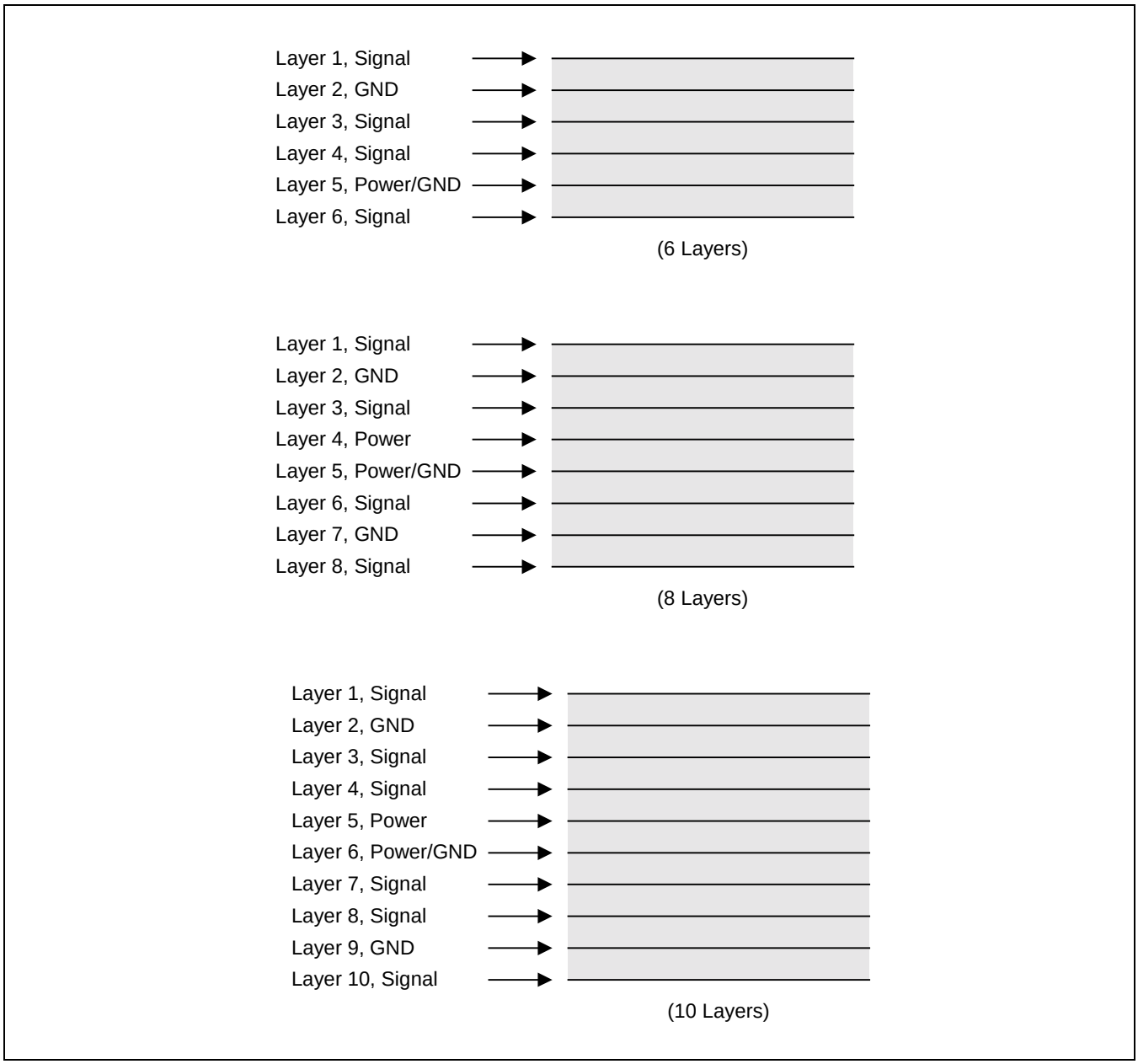
— SCLK0, SCLK1 are exactly the same signals. There are only two 16-bit SDRAM for 32-bit configuration. It is recommend to use all SCLKn signals. (For example, SCLK0 for one SDRAM, SCLK1 for the other SDRAM)

— Power signal (GND, 1.8V, 3.3V) must be reinforced as soon as possible. Also, the bypass capacitor has to be nearest to the power pads.

— All the memory signals are simulated at 35pF load. So, all capacitance including the board parasitic must be smaller than 35pF. The parasitic capacitance of the S3C2410 is typically 5pF.

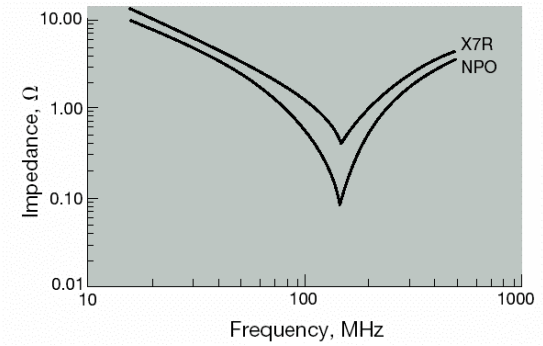
4. LAYER STACK-UP

To easily implement the impedance line, the PWR or GND plane must be placed in the layer adjacent to the signal line. The following examples illustrate the proper use of layers.



5. DECOUPLING CAP AND VIA HOLE LAYOUT

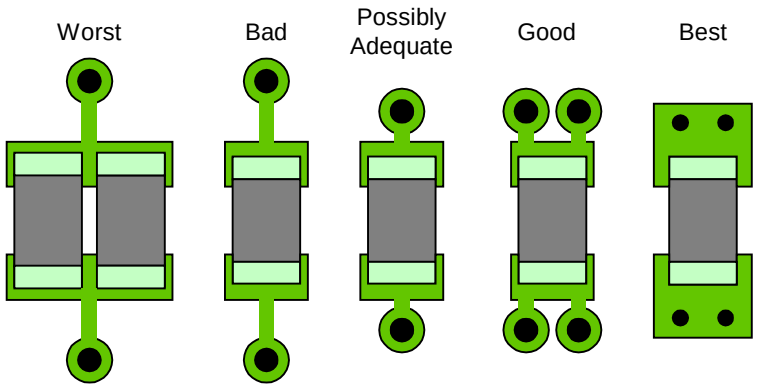
The decoupling capacitor of sufficient capacity must be placed in the high frequency switching device, for the supply of necessary power in the shortest distance. If dcap lacks capacity or supplied path impedance is too high, switching noise is generated and it becomes the source of radiation. Dcap must use a proper capacitor type according to the frequency. Since Dcap impedance is x= sqrt (r2+…) and parasitic inductance value can be dominant according to the frequency, be sure to use it in consideration of frequency bandwidth that acts as capacitor.



F = 1/(2×pi×sqrt(LC))

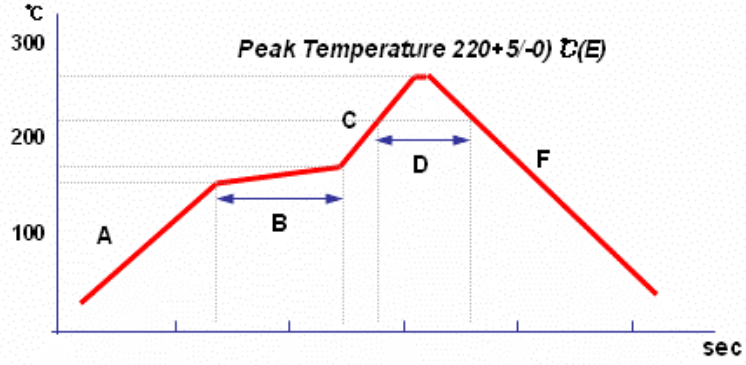
The Dcap must have enough capacity to supply power during the signal transition.

If possible, the decoupling capacitor must be basically placed closer to the power pin of a desired device. When using PCB pad, in addition, do not connect more than 2 decoupling capacitors to one via. The PWR/GND read trace used for decoupling capacitor installation must be routed short, if possible.



6. REFLOW PROFILE

❖ IR reflow Profile



IR re-flow profile for Pre-conditioning						
Peak Temp.	Heat-up(A)	Pre-heat(B)	Heat-up(C)	Maintain(D)	Re-flow peak(E)	Cooling down(F)
Max. 225'C	3'C/sec below	140~160'C 60~120sec	3'C/sec below	60~150sec (Over 183'C)	Max. 220(+5/-0)'C 10sec +/-3sec	6'C/sec

7. EMI REDUCTION

— Close coupling between conductors of a pair not only reduces EMI, but it helps to ensure noise coupled onto the conductors will do so equally as common mode noise which will then be rejected by the receiver.

— Imbalance minimization is the other important factor in reducing EMI.

— The basic rule to follow is: if any discontinuity must be introduced in proximity to differential lines, it should be introduced equally to both members of the pair.