S3 Incorporated

86C928

GUI Accelerator

86C928

GUI

ACCELERATOR

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S3 Incorporated
2880 San Tomas Expressway
Santa Clara, CA 95051-0981

NOTATIONAL CONVENTIONS

The following notational conventions are used in this data book:

Signal names are shown in all uppercase letters. For example, XD.

A bar over a signal name indicates an active low signal. For example, $\overline{OE}$.

n:m indicates a bit field from bit n to bit m. For example, 7:0 specifies bits 7 through 0, inclusive.

Use of the letter H indicates a hexadecimal number. For example, 7AH is a hexadecimal number.

When numerical modifiers such as K or M are used, they refer to binary rather than decimal form. Thus, for example, 1 KByte would be equivalent to 1024, not 1,000 bytes.

When NC is used to describe a pin, it indicates a No Connect.

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Section 1: Introduction

The S3 86C928 is an ultra-high performance graphical user interface (GUI) accelerator. It is specifically designed to speed up applications running under GUI environments such as Windows 3.0 and 3.1, X-Windows, OS/2 PM and AutoCad. It provides the fastest graphics accelerator performance available. The 86C928 is fully VGA compatible and fully backward compatible to CGA, HGC, and MDA, guaranteeing OEMs compatibility with low-end PC application software.

Some of the features provided are:

- Advanced architecture using pipelining, multiple FIFOs and a read-ahead cache
- Hardware acceleration of major 2-D graphics operations
- Direct connectivity to a 16-bit ISA bus, 32-bit 386DX/486 local bus or EISA bus
- Support for no-wait-state ISA and local bus cycles
- Internal and external hardware cursor support
- Optimized system interface, including display memory write posting capability
- Direct support for 0.5, 1, 2, 3 or 4 MBytes of VRAM
- DRAM can be used in place of VRAM for off-screen video memory
- Fast linear addressing by the CPU of up to 4 MBytes of display memory
- Fast direct image read/write by the CPU
- Direct interface to a wide range of video DACs, including those with serial input data (SID) support
- Support for resolutions up to 1600x1200x8, 1280x1024x16 and 1024x768x32
- High performance driver support and full compatibility with all S3 drivers
- Multimedia support via ability to genlock with external NTSC/PAL video
- Supplied in a 208-pin PQFP package using advanced sub-micron CMOS technology

1.1 BUS INTERFACES

When used on the motherboard, the 86C928 can directly connect to the 386DX/486 CPU bus. A 386/486 no-wait-state memory read/write cycle is provided for this configuration, resulting in very high performance in a PC environment. The 86C928 also contains a 32-bit EISA interface for use with add-in board graphics subsystems. The 86C928 further integrates a 16-bit ISA bus interface for add-in board graphics subsystems. This interface supports no-wait-state ISA memory cycles. The accelerator's high level of integration facilitates low-chip-count implementations for all supported bus system configurations as shown by the system block diagram in Figure 1-1.

1.2 VRAM SUPPORT

The 86C928 accelerator contains a complete VRAM interface. Thus, it is ideal for the highest performance graphics systems. Display memory configurations of 0.5, 1, or 2 MBytes are supported without additional external logic, and 3 or 4 MByte configurations are supported with the addition of a simple decoder.

1.3 RESOLUTIONS SUPPORTED

Table 1-1. Video Resolutions Supported

Resolution	1 MB VRAM	2 MBs VRAM	4 MBs VRAM
640x480x8	✔	✔	✔
640x480x16	✔	✔	✔
640x480x24	✔	✔	✔
640x480x32		✔	✔
800x600x4	✔	✔	✔
800x600x8	✔	✔	✔
800x600x16	✔	✔	✔
800x600x32		✔	✔
1024x768x4	✔	✔	✔
1024x768x8	✔	✔	✔
1024x768x16		✔	✔
1024x768x24			✔
1024x768x32			✔
1280x1024x4	✔	✔	✔
1280x1024x8		✔	✔
1280x1024x16			✔
1600x1200x4		✔	✔
1600x1200x8		✔ E	✔

Extended VGA text modes up to 132 columns by 43 rows are possible as well.

1.4 VIDEO DAC SUPPORT

Integrated support is provided for a wide range of video DACs. These range from inexpensive 8 bits-per-pixel (bpp) designs up to the newest 44-pin 16 and 24 bpp high-speed video DACs with SID and 64-bit pixel data input support.

1.5 ADVANCED ARCHITECTURE

Features such as Command and Display Memory FIFOs allow very fast execution of graphic operations such as "bitBLTs", line drawing, rectangle fills and window clipping. This makes common GUI operations such as opening and resizing of windows, menu management, dragging and scrolling virtually instantaneous. The chip also supports either an internal hardware cursor stored in off-screen video memory or an external video DAC cursor. This speeds up cursor and icon performance and eliminates the software overhead associated with their manipulation. Another advanced feature permits video memory to be mapped into the CPU's upper memory address space via a fast linear addressing scheme. A memory-mapped I/O port is also provided to speed CPU accesses to video memory.

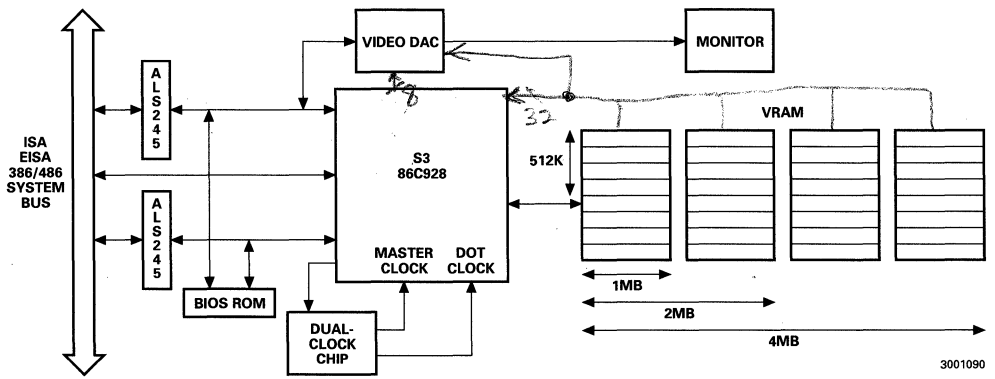

Figure 1-1. System Block Diagram

Section 2: Pins

2.1 PINOUT DIAGRAMS

The 86C928 comes in a 208 pin PQFP package. The ISA bus pinout is shown in Figure 2-1.

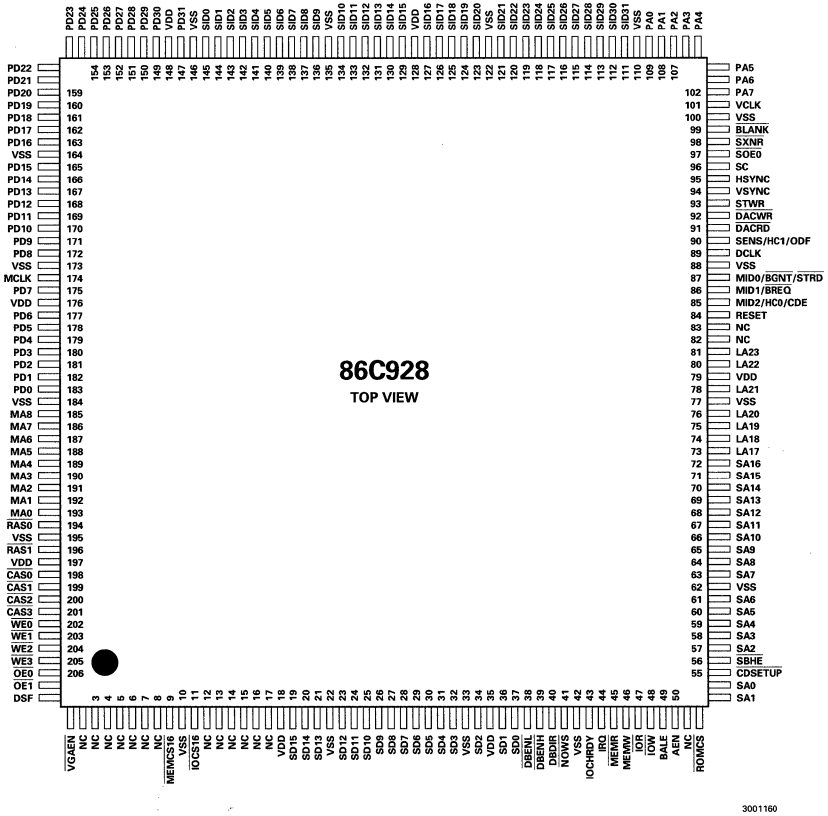

Figure 2-1. ISA Bus Configuration Pinout

The pinout for the EISA configuration of the 86C928 is shown in Figure 2-2.

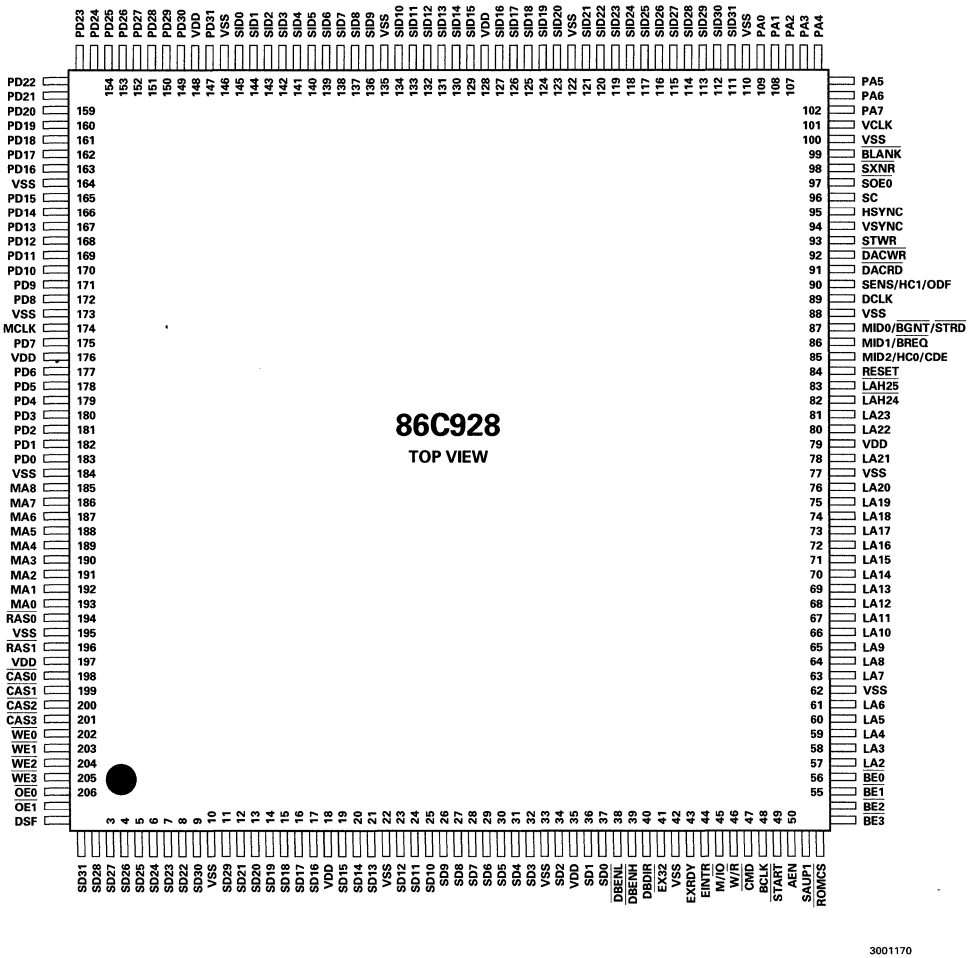

Figure 2-2. EISA Bus Configuration Pinout

The pinout for the local bus configuration of the 86C928 is shown in Figure 2-3.

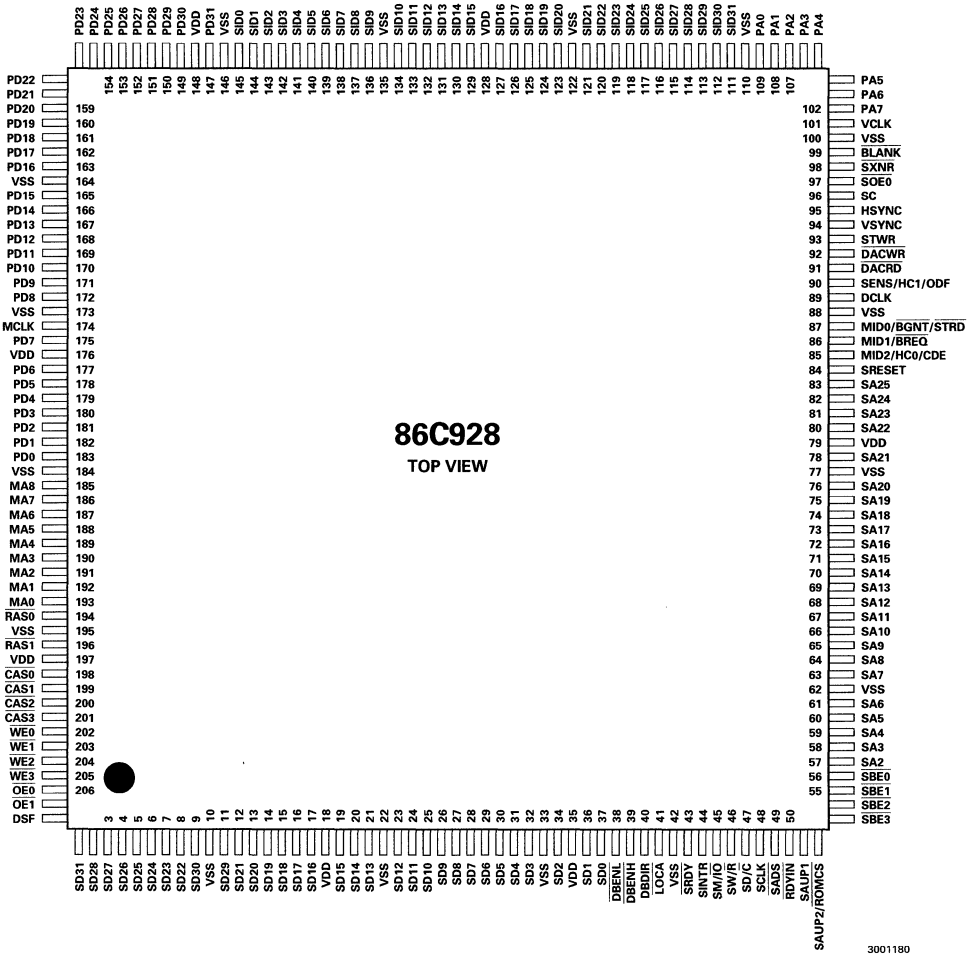

Figure 2-3. Local Bus Configuration Pinout

2.2 PIN DESCRIPTIONS

The following table provides a brief description of each pin on the 86C928 for its ISA, EISA and local bus configurations. The following definitions are used in these descriptions:

I - Input signal
O - Output signal
B - Bidirectional signal

Some pins have multiple names. This reflects the different functions performed by those pins depending on the bus configuration selected by power-on-strapping. The pin definitions and functions are given for each possible case.

Table 2-1. 86C928 Pin Descriptions

Symbol	Type	Pin Number(s)	Description
BUS INTERFACES			
Address and Data			
SD[15:0]	B	19-21, 23-32, 34, 36, 37	System Data Bus. (ISA) SD[7:0] also serve as the Video DAC Data Bus and as the General Input Port Data Bus. SD[11:8] act as the video DAC register select bits as well.
SD[31:0]		1, 9, 11, 2-8, 12-17, 19-21, 23-32, 34, 36, 37	System Data Bus. (EISA and Local Bus) SD[7:0] also serve as the Video DAC Data Bus and as the General Input Port Data Bus. SD[11:8] act as the video DAC register select bits as well.
LA[23:17]	I	81-80, 78, 76-73	Unlatched Address Bits. (ISA)
$\overline{\text{LAH[25:24]}}$		83, 82	System Upper Address Bits. (EISA)
SA[25:24]			System Address Bus Bits. (Local Bus)
SA[15:0]	I	71-63, 61-57, 53, 54	System Address Bus. (ISA)
LA[23:2]		81, 80, 78, 76-63, 61-57	System Address Bus. (EISA)
SA[23:2]			System Address Bus. (Local Bus)
$\overline{\text{SBHE}}$	I	56	High Data Byte Enable. (ISA)
$\overline{\text{BE[3:0]}}$		53-56	Data Byte Enables. (EISA)
$\overline{\text{SBE[3:0]}}$			Data Byte Enables. (Local Bus)
SAUP1	I	51	Upper Address Decode. (EISA)
SAUP[2:1]		52, 51	Upper Address Decodes. (Local Bus) SAUP2 also serves as a BIOS ROM Chip Select output

Table 2-1. 86C928 Pin Descriptions (Continued)

Symbol	Type	Pin Number(s)	Description
Bus Control			
AEN	I	50	Address Enable. (ISA, EISA) When asserted, this signal allows DMA transfers to occur.
$\overline{\text{RDYIN}}$			Local Bus Cycle End Acknowledge. (Local Bus) The 86C805 holds read data valid on the bus until this input is asserted.
$\overline{\text{IOW}}$	I	48	I/O Write. (ISA)
BCLK			Bus Clock. (EISA)
SCLK			System Clock. (Local Bus)
$\overline{\text{IOR}}$	I	47	I/O Read. (ISA)
$\overline{\text{CMD}}$			Bus Cycle Timing Control. (EISA)
SD/$\overline{\text{C}}$			Data/Control Cycle Indicator. (Local Bus)
IRQ	O	44	Interrupt Request. (ISA)
EINTR			Interrupt Request. (EISA)
SINTR			Interrupt Request. (Local Bus)
$\overline{\text{ENEID}}$	O	52	EISA ID. This signal is externally decoded using M/$\overline{\text{IO}}$. It is valid during I/O cycles. This pin can also serve as the BIOS ROM chip select ($\overline{\text{ROMCS}}$) during memory cycles. (EISA)
SAUP2	I		Upper Address Decode Bit 2. Also serves as a BIOS ROM Chip Select output ($\overline{\text{ROMCS}}$) (Local Bus)
IOCHRDY	O	43	Channel Ready. (ISA)
EXRDY			Wait State Request. (EISA)
$\overline{\text{SRDY}}$			Local Bus Cycle End. (Local Bus)
$\overline{\text{NOWS}}$	O	41	Zero Wait-State Cycle. (ISA)
$\overline{\text{EX32}}$			32-bit Slave Indicator. (EISA)
$\overline{\text{LOCA}}$			Local Bus Access Cycle Indicator. (Local Bus)
$\overline{\text{MEMR}}$	I	45	Memory Read. (ISA)
M/$\overline{\text{IO}}$			Memory/IO Cycle Indicator. (EISA)
SM/$\overline{\text{IO}}$			Memory/IO Cycle Indicator. (Local Bus)
RESET	I	84	Reset. (ISA, EISA)
SRESET			System Reset. (Local Bus)

Table 2-1. 86C928 Pin Descriptions (Continued)

Symbol	Type	Pin Number(s)	Description
BALE	I	49	Buffer Address Latch Enable. (ISA)
$\overline{START}$			Cycle Start Strobe. (EISA)
$\overline{SADS}$			System Address Strobe. (Local Bus)
$\overline{MEMW}$	I	46	Memory Write. (ISA)
W/$\overline{R}$			Write/Read Cycle Indicator. (EISA)
SW/$\overline{R}$			Write/Read Cycle Indicator. (Local Bus)
$\overline{CDSETUP}$	I	55	Card Setup. (ISA)
$\overline{VGAEN}$	I	1	Enable VGA I/O and memory access. (ISA)
$\overline{MEMCS16}$	O	9	Memory 16-bit Access. (ISA)
$\overline{IOCS16}$	O	11	I/O 16-bit Access. (ISA)
External Buffer and EPROM Control			
DBDIR	O	40	Data Buffer Direction Control. This signal is high for a data write and low for a data read.
$\overline{DBENH}$	O	39	Data Buffer High-Byte Enable. This active low signal enables external data buffers for data bits SD[31:8].
$\overline{DBENL}$	O	38	Data Buffer Low-Byte Enable. This active low signal enables an external data buffer for data bits SD[7:0].
$\overline{ROMCS}$	O	52	BIOS ROM Chip Select. Also can serve as the local bus upper address decode bit 2 (SAUP2) or the EISA bus ENEID signal.
CLOCK CONTROL			
MCLK	I	174	Master (Memory) Clock
DCLK	I	89	Dot Clock. This input is provided by the clock chip.
STWR	O	93	Clock Select Strobe. Also serves as the General Output Port Write Strobe.
PA[3:0]	O	106-109	Clock Select Bits. Also serve as pixel address bits to the video DAC.
DISPLAY MEMORY INTERFACE			
Address and Data			
PD[31:0]	B	147, 149-163, 165-172, 175, 177-183	Pixel Data Bus. PD[15-0] are also used as the system configuration strapping bits, providing system configuration and setup information upon power-on or reset.
SID[31:0]	I	111-121, 123-127, 129-134, 136-145	Serial Input Pixel Data Bus.
MA[8:0]	O	185-193	Memory Address Bus.

Table 2-1. 86C928 Pin Descriptions (Continued)

Symbol	Type	Pin Number(s)	Description
Memory Control			
RAS[1:0]	O	196, 194	Row Address Strobes for each 1 MByte memory bank.
CAS[3:0]	O	201-198	Column Address Strobes for each pixel data byte.
WE[3:0]	O	205-202	Write Enables for upper and lower pixel data nibbles.
OE[1:0]	O	207-206	Output Enables for each 2 MByte memory bank.
SOE0	O	97	Serial Pixel Select for the 1st MByte memory bank for configurations up to 2 MBytes. Externally decoded with SXNR to produce serial pixel selects for each MByte bank in configurations from 2 to 4 MBytes.
SXNR	O	98	Serial Pixel Select for the 2nd MByte memory bank for configurations up to 2 MBytes. Externally decoded with SOE0 to produce serial pixel selects for each MByte bank in configurations from 2 to 4 MBytes.
SC	O	96	Serial Pixel Data Clock.
DSF	O	208	Special VRAM Function Control.
VIDEO DAC INTERFACE			
Address and Data			
PA[7:0]	O	102-109	Video DAC Pixel Address Bus. These signals also serve as the General Output Port Data Bus. PA[3:0] also serve as the Clock Select Bits.
SD[7:0]	B	28-32, 34, 36, 37	Video DAC Data Bus. These signals also serve as the System Data Bus bits and as the General Input Port Data bus.
SD[11:8]	B	24-27	Video DAC Register Select. These signals also serve as System Data Bus bits.
Video DAC Control			
VCLK	O	101	Video/Pixel Clock
DACRD	O	91	Video DAC Read. This active low signal, when asserted, indicates a data read from the video DAC.
DACWR	O	92	Video DAC Write. This active low signal, when asserted, indicates a data write to the video DAC.
BLANK	O	99	Video Blank. Asserting this active low signal turns off the video output.
SENS	I	90	Video Level Sense. The video DAC asserts this active high signal when it detects the appropriate video voltage on the analog outputs. When bit 5 of the Extended DAC Control register (3?5H, Index 55H) is set to 1, this signal becomes the HC1 signal. If bit 5 of the Hardware Graphics Cursor Mode register (3?5H, Index 45H) is then set to 1, this becomes the ODF signal.
HSYNC	O	95	Horizontal Sync.
VSYNC	B	94	Vertical Sync.This is an input for genlock support.

Table 2-1. 86C928 Pin Descriptions (Continued)

Symbol	Type	Pin Number(s)	Description
MID2	I	85	Monitor ID Bit 2. This input from certain monitors is latched into bit 6 of the Subsystem Status register (42E8H, Read). This signal is normally pulled high externally. When bit 5 of the Extended DAC Control register (3?5H, Index 55H) is set to 1, this signal becomes the HC0 signal. If bit 5 of the Hardware Graphics Cursor Mode register (3?5H, Index 45H) is then set to 1, this becomes the CDE signal.
MID1	I	86	Monitor ID Bit 1. This input from certain monitors is latched into bit 5 of the Subsystem Status register (42E8H, Read). This signal is normally pulled high externally and is enabled when bit 1 of the System Configuration register (3?5H, Index 40H) is 0. If this bit is set to 1, then setting bit 2 of the Extended System Cont 1 register (3?5H, Index 50H) to 1 enables the BREQ function on this pin.
MID0	I	87	Monitor ID Bit 0. This input from certain monitors is latched into bit 4 of the Subsystem Status register (42E8H, Read). This signal is normally pulled high externally and is enabled when bit 1 of the System Configuration register (3?5H, Index 40H) is 0. If this bit is set to 1 and bit 5 of the Extended DAC Control register (3?5H, Index 55H) is set to 1, this becomes the STRD signal. When bit 1 of the System Configuration register (3?5H, Index 40H) is set to 1 and bit 2 of the Extended DAC Control register (3?5H, Index 55H) is cleared to 0, setting bit 2 of the Extended System Cont 1 register (3?5H, Index 50H) to 1 enables the BGNT function on this pin.
Extended Control for Brooktree Bt 484/485			
ODF	O	90	Odd Frame Control. The Bt484/485 requires this signal for proper operation. It is enabled by setting bit 5 of the Extended DAC Control register (3?5H, Index 55H) and bit 5 of the Hardware Graphics Cursor Mode Register (3?5H, Index 45) to 1.
CDE	O	85	Composite Display Enable. The Bt484/485 requires this signal in conjunction with the BLANK signal to determine whether the analog outputs are blanked or contain pixel or overscan data. It is enabled by setting bit 5 of the Extended DAC Control register (3?5H, Index 55H) and bit 5 of the Hardware Graphics Cursor Mode Register (3?5H, Index 45) to 1.

Table 2-1. 86C928 Pin Descriptions (Continued)

Symbol	Type	Pin Number(s)	Description
MISCELLANEOUS FUNCTIONS			
General I/O Port			
SD[7:0]	B	28-32, 34, 36, 37	General Input Port Data Bus. These signals also serve as System Data Bus bits and as the video DAC Data Bus.
PA[7:4]	O	102-105	General Output Port Data Bus. These signals also act as Pixel Address Bits to the video DAC.
$\overline{\text{STRD}}$	O	87	General Input Port Read Strobe. If the General Input Port is activated by setting bit 2 of the Extended DAC Control register (3?5H, Index 55H) to 1, bit 1 of the System Configuration register (3?5H, Index 40H) is set to 1 and this active low signal is asserted, a read of 3C8H brings in data from an external buffer via the low byte of the system data bus. If bit 2 of the Extended DAC Control register (3?5H, Index 55H) is then cleared to 0, the $\overline{\text{BGNT}}$ function can be enabled on this pin. If bit 1 of the System Configuration register (3?5H, Index 40H) is cleared to 0, this becomes the MID0 signal.
STWR	O	93	General Output Port Write Strobe. Write strobe for the General Output Port (General Output Port register (3?5H, Index 5CH)) and the Clock Select Strobe input to the clock chip.
Bus Master Control			
$\overline{\text{BREQ}}$	I	86	Bus Request from graphics co-processor. This function is enabled by setting bit 1 of the System Configuration register (3?5H, Index 40H) to 1 and setting bit 2 of the Extended System Cont 1 register (3?5H, Index 50H) to 1. Otherwise, this signal is MID1.
$\overline{\text{BGNT}}$	O	87	Bus Grant to graphics co-processor. Setting bit 1 of the System Configuration register (3?5H, Index 40H) to 1 and clearing bit 2 of the Extended DAC Control register (3?5H, Index 55H) to 0 sets up the pin for this function, which is then enabled by setting bit 2 of the Extended System Cont 1 register (3?5H, Index 50H) to 1. If bit 2 of the Extended DAC Control register (3?5H, Index 55H) is set to 1, this becomes the $\overline{\text{STRD}}$ signal. If bit 1 of the System Configuration register (3?5H, Index 40H) is cleared to 0, this becomes the MID0 signal. The bus will not be granted if the termination position programmed into the Bus Grant Termination register (3?5H, Index 5FH) and its extension (bit 7 of the Extended Horizontal Overflow register (3?5H, Index 5DH)) has been exceeded.

Table 2-1. 86C928 Pin Descriptions (Continued)

Symbol	Type	Pin Number(s)	Description
External Hardware Cursor Control			
HC1	O	90	Internal Hardware Cursor Bit 1. When bit 5 of the Extended DAC Control register (3?5H, Index 55H) is set to 1, this signal provides cursor control data to the video DAC. If bit 5 of the Hardware Graphics Cursor Mode Register (3?5H, Index 45H) is then set to 1, this become the ODF signal. If the external cursor is not enabled, this is the SENS signal.
HC0	O	85	Internal Hardware Cursor Bit 0. When bit 5 of the Extended DAC Control register (3?5H, Index 55H) is set to 1, this signal provides cursor control data to the video DAC. If bit 5 of the Hardware Graphics Cursor Mode Register (3?5H, Index 45H) is then set to 1, this become the CDE signal. If the external cursor is not enabled, this is the MID2 signal.
POWER AND GROUND			
V_{DD}	I	18, 35, 79, 128, 148, 176, 197	Power supply
V_{SS}	I	10, 22, 33, 42, 62, 77, 88, 100, 110, 122, 135, 146, 164, 173, 184, 195	Ground

2.3 PIN LISTS

Table 2-2 lists all 86C928 pins alphabetically. The pin number(s) corresponding to each pin name are given in the appropriate chip/bus interface type column. Table 2-3 lists all 86C928 pins in numerical order. The pin name corresponding to each pin number is given in the appropriate chip/bus interface column.

Table 2-2. Alphabetical Pin Listing

	PIN(S)		
Name	**ISA**	**EISA**	**Local Bus**
AEN	50	50	
BALE	49		
BCLK		48	
BE[3:0]		53-56	
BGNT	87	87	87
BLANK	99	99	99
BREQ	86	86	86
CAS[3:0]	201-198	201-198	201-198
CDE	85	85	85
CDSETUP	55		
CMD		47	
DACRD	91	91	91
DACWR	92	92	92
DBDIR	40	40	40
DBENH	39	39	39
DBENL	38	38	38
DCLK	89	89	89
DSF	208	208	208
EINTR		44	
ENEID		52	
EX32		41	
EXRDY		43	
HC0	85	85	85
HC1	90	90	90
HSYNC	95	95	95
IOCHRDY	43		
IOCS16	11		
IOR	47		
IOW	48		
IRQ	44		
LA[23:17]	81-80, 78, 76-73		
LA[23:2]		81, 80, 78, 76-63, 61-57	
LAH[25:24]		83, 82	
LOCA			41

Table 2-2. Alphabetical Pin Listing (Continued)

	PIN(S)		
Name	**ISA**	**EISA**	**Local Bus**
MA[8:0]	185-193	185-193	185-193
MCLK	174	174	174
MEMCS16	9		
$\overline{\text{MEMR}}$	45		
$\overline{\text{MEMW}}$	46		
MID0	87	87	87
MID1	86	86	86
MID2	85	85	85
M/$\overline{\text{IO}}$		45	
$\overline{\text{NOWS}}$	41		
$\overline{\text{ODF}}$	90	90	90
$\overline{\text{OE}}$[1:0]	207, 206	207, 206	207, 206
PA[7:0]	102-109	102-109	102-109
PD[31:0]	147, 149-163, 165-172, 175, 177-183	147, 149-163, 165-172, 175, 177-183	147, 149-163, 165-172, 175, 177-183
$\overline{\text{RAS}}$[1:0]	196, 194	196. 194	196, 194
$\overline{\text{RDYIN}}$			50
$\overline{\text{RESET}}$	84	84	
$\overline{\text{ROMCS}}$	52	52	52
SA[16:0]	72-63, 61-57, 53, 54		
SA[25:2]			83-80, 78, 76-63, 61-57
$\overline{\text{SADS}}$			49
SAUP1		51	
SAUP[2:1]			52, 51
$\overline{\text{SBE}}$[3:0]			53-56
$\overline{\text{SBHE}}$	56		
SC	96	96	96
SCLK			48
SD/$\overline{\text{C}}$			47
SD[15:0]	19-21, 23-32, 34, 36, 37		
SD[31:0]		1, 9, 11, 2-8, 12-17, 19-21, 23-32, 34, 36, 37	1, 9, 11, 2-8, 12-17, 19-21, 23-32, 34, 36, 37
SENS	90	90	90
SID[31:0]	111-121, 123-127, 129-134, 136-145	111-121, 123-127, 129-134, 136-145	111-121, 123-127, 129-134, 136-145
SINTR			44
SM/$\overline{\text{IO}}$			45

Table 2-2. Alphabetical Pin Listing (Continued)

	PIN(S)		
Name	**ISA**	**EISA**	**Local Bus**
START		49	
SOE0	97	97	97
SRDY			43
SRESET			84
STRD	87	87	87
STWR	93	93	93
SW/R			46
SXNR	98	98	98
VCLK	101	101	101
VDD	18, 35, 79, 128, 148, 176 197	18, 35, 79, 128, 148, 176 197	18, 35, 79, 128, 148, 176 197
VGAEN	1		
VSS	10, 22, 33, 42, 62, 77, 88, 100, 110, 122, 135, 146 164, 173, 184, 195	10, 22, 33, 42, 62, 77, 88 100, 110, 122, 135, 146 164, 173, 184, 195	10, 22, 33, 42, 62, 77, 88 100, 110, 122, 135, 146 164, 173, 184, 195
VSYNC	94	94	94
WE[3:0]	205-202	205-202	205-202
W/R		46	

Table 2-3. Numerical Pin Listing

Number	Name		
	ISA	**EISA**	**Local Bus**
1	$\overline{\text{VGAEN}}$	SD31	SD31
2	NC	SD28	SD28
3	NC	SD27	SD27
4	NC	SD26	SD26
5	NC	SD25	SD25
6	NC	SD24	SD24
7	NC	SD23	SD23
8	NC	SD22	SD22
9	$\overline{\text{MEMCS16}}$	SD30	SD30
10	V_{SS}	V_{SS}	V_{SS}
11	$\overline{\text{IOCS16}}$	SD29	SD29
12	NC	SD21	SD21
13	NC	SD20	SD20
14	NC	SD19	SD19
15	NC	SD18	SD18
16	NC	SD17	SD17
17	NC	SD16	SD16
18	V_{DD}	V_{DD}	V_{DD}
19	SD15	SD15	SD15
20	SD14	SD14	SD14
21	SD13	SD13	SD13
22	V_{SS}	V_{SS}	V_{SS}
23	SD12	SD12	SD12
24	SD11	SD11	SD11
25	SD10	SD10	SD10
26	SD9	SD9	SD9
27	SD8	SD8	SD8
28	SD7	SD7	SD7
29	SD6	SD6	SD6
30	SD5	SD5	SD5
31	SD4	SD4	SD4
32	SD3	SD3	SD3
33	V_{SS}	V_{SS}	V_{SS}
34	SD2	SD2	SD2
35	V_{DD}	V_{DD}	V_{DD}
36	SD1	SD1	SD1
37	SD0	SD0	SD0
38	$\overline{\text{DBENL}}$	$\overline{\text{DBENL}}$	$\overline{\text{DBENL}}$
39	$\overline{\text{DBENH}}$	$\overline{\text{DBENH}}$	$\overline{\text{DBENH}}$
40	DBDIR	DBDIR	DBDIR
41	$\overline{\text{NOWS}}$	$\overline{\text{EX32}}$	$\overline{\text{LOCA}}$
42	V_{SS}	V_{SS}	V_{SS}

Table 2-3. Numerical Pin Listing (Continued)

Number	Name ISA	EISA	Local Bus
43	IOCHRDY	EXRDY	$\overline{SRDY}$
44	IRQ	EINTR	SINTR
45	$\overline{MEMR}$	M/$\overline{IO}$	SM/$\overline{IO}$
46	MEMW	W/$\overline{R}$	SW/$\overline{R}$
47	$\overline{IOR}$	$\overline{CMD}$	SD/$\overline{C}$
48	$\overline{IOW}$	BCLK	SCLK
49	BALE	$\overline{START}$	$\overline{SADS}$
50	AEN	AEN	$\overline{RDYIN}$
51	NC	SAUP1	SAUP1
52	$\overline{ROMCS}$	$\overline{ENEID}$/$\overline{ROMCS}$	SAUP2/$\overline{ROMCS}$
53	SA1	$\overline{BE3}$	$\overline{SBE3}$
54	SA0	$\overline{BE2}$	$\overline{SBE2}$
55	$\overline{CDSETUP}$	$\overline{BE1}$	$\overline{SBE1}$
56	$\overline{SBHE}$	$\overline{BE0}$	$\overline{SBE0}$
57	SA2	LA2	SA2
58	SA3	LA3	SA3
59	SA4	LA4	SA4
60	SA5	LA5	SA5
61	SA6	LA6	SA6
62	V_{SS}	V_{SS}	V_{SS}
63	SA7	LA7	SA7
64	SA8	LA8	SA8
65	SA9	LA9	SA9
66	SA10	LA10	SA10
67	SA11	LA11	SA11
68	SA12	LA12	SA12
69	SA13	LA13	SA13
70	SA14	LA14	SA14
71	SA15	LA15	SA15
72	SA16	LA16	SA16
73	LA17	LA17	SD17
74	LA18	LA18	SA18
75	LA19	LA19	SA19
76	LA20	LA20	SA20
77	V_{SS}	V_{SS}	V_{SS}
78	LA21	LA21	SA21
79	V_{DD}	V_{DD}	V_{DD}
80	LA22	LA22	SA22
81	LA23	LA23	SA23
82	NC	$\overline{LAH24}$	SA24
83	NC	$\overline{LAH25}$	SA25
84	RESET	RESET	SRESET

Table 2-3. Numerical Pin Listing (Continued)

Number	Name ISA	EISA	Local Bus
85	MID2/HC0/CDE	MID2/HC0/CDE	MID2/HC0/CDE
86	MID1/BREQ	MID1/BREQ	MID1/BREQ
87	MID0/BGNT/STRD	MID0/BGNT/STRD	MID0/BGNT/STRD
88	Vss	Vss	Vss
89	DCLK	DCLK	DCLK
90	SENS/HC1/ODF	SENS/HC1/ODF	SENS/HC1/ODF
91	DACRD	DACRD	DACRD
92	DACWR	DACWR	DACWR
93	STWR	STWR	STWR
94	VSYNC	VSYNC	VSYNC
95	HSYNC	HSYNC	HSYNC
96	SC	SC	SC
97	SOE0	SOE0	SOE0
98	SXNR	SXNR	SXNR
99	BLANK	BLANK	BLANK
100	Vss	Vss	Vss
101	VCLK	VCLK	VCLK
102	PA7	PA7	PA7
103	PA6	PA6	PA6
104	PA5	PA5	PA5
105	PA4	PA4	PA4
106	PA3	PA3	PA3
107	PA2	PA2	PA2
108	PA1	PA1	PA1
109	PA0	PA0	PA0
110	Vss	Vss	Vss
111	SID31	SID31	SID31
112	SID30	SID30	SID30
113	SID29	SID29	SID29
114	SID28	SID28	SID28
115	SID27	SID27	SID27
116	SID26	SID26	SID26
117	SID25	SID25	SID25
118	SID24	SID24	SID24
119	SID23	SID23	SID23
120	SID22	SID22	SID22
121	SID21	SID21	SID21
122	Vss	Vss	Vss
123	SID20	SID20	SID20
124	SID19	SID19	SID19
125	SID18	SID18	SID18
126	SID17	SID17	SID17

Table 2-3. Numerical Pin Listing (Continued)

Number	Name ISA	EISA	Local Bus
127	SID16	SID16	SID16
128	VDD	VDD	VDD
129	SID15	SID15	SID15
130	SID14	SID14	SID14
131	SID13	SID13	SID13
132	SID12	SID12	SID12
133	SID11	SID11	SID11
134	SID10	SID10	SID10
135	VSS	VSS	VSS
136	SID9	SID9	SID9
137	SID8	SID8	SID8
138	SID7	SID7	SID7
139	SID6	SID6	SID6
140	SID5	SID5	SID5
141	SID4	SID4	SID4
142	SID3	SID3	SID3
143	SID2	SID2	SID2
144	SID1	SID1	SID1
145	SID0	SID0	SID0
146	VSS	VSS	VSS
147	PD31	PD31	PD31
148	VDD	VDD	VDD
149	PD30	PD30	PD30
150	PD29	PD29	PD29
151	PD28	PD28	PD28
152	PD27	PD27	PD27
153	PD26	PD26	PD26
154	PD25	PD25	PD25
155	PD24	PD24	PD24
156	PD23	PD23	PD23
157	PD22	PD22	PD22
158	PD21	PD21	PD21
159	PD20	PD20	PD20
160	PD19	PD19	PD19
161	PD18	PD18	PD18
162	PD17	PD17	PD17
163	PD16	PD16	PD16
164	VSS	VSS	VSS
165	PD15	PD15	PD15
166	PD14	PD14	PD14
167	PD13	PD13	PD13
168	PD12	PD12	PD12

Table 2-3. Numerical Pin Listing (Continued)

Number	Name ISA	EISA	Local Bus
169	PD11	PD11	PD11
170	PD10	PD10	PD10
171	PD9	PD9	PD9
172	PD8	PD8	PD8
173	VSS	VSS	VSS
174	MCLK	MCLK	MCLK
175	PD7	PD7	PD7
176	VDD	VDD	VDD
177	PD6	PD6	PD6
178	PD5	PD5	PD5
179	PD4	PD4	PD4
180	PD3	PD3	PD3
181	PD2	PD2	PD2
182	PD1	PD1	PD1
183	PD0	PD0	PD0
184	VSS	VSS	VSS
185	MA8	MA8	MA8
186	MA7	MA7	MA7
187	MA6	MA6	MA6
188	MA5	MA5	MA5
189	MA4	MA4	MA4
190	MA3	MA3	MA3
191	MA2	MA2	MA2
192	MA1	MA1	MA1
193	MA0	MA0	MA0
194	$\overline{\text{RAS0}}$	$\overline{\text{RAS0}}$	$\overline{\text{RAS0}}$
195	VSS	VSS	VSS
196	$\overline{\text{RAS1}}$	$\overline{\text{RAS1}}$	$\overline{\text{RAS1}}$
197	VDD	VDD	VDD
198	$\overline{\text{CAS0}}$	$\overline{\text{CAS0}}$	$\overline{\text{CAS0}}$
199	$\overline{\text{CAS1}}$	$\overline{\text{CAS1}}$	$\overline{\text{CAS1}}$
200	$\overline{\text{CAS2}}$	$\overline{\text{CAS2}}$	$\overline{\text{CAS2}}$
201	$\overline{\text{CAS3}}$	$\overline{\text{CAS3}}$	$\overline{\text{CAS3}}$
202	$\overline{\text{WE0}}$	$\overline{\text{WE0}}$	$\overline{\text{WE0}}$
203	$\overline{\text{WE1}}$	$\overline{\text{WE1}}$	$\overline{\text{WE1}}$
204	$\overline{\text{WE2}}$	$\overline{\text{WE2}}$	$\overline{\text{WE2}}$
205	$\overline{\text{WE3}}$	$\overline{\text{WE3}}$	$\overline{\text{WE3}}$
206	$\overline{\text{OE0}}$	$\overline{\text{OE0}}$	$\overline{\text{OE0}}$
207	$\overline{\text{OE1}}$	$\overline{\text{OE1}}$	$\overline{\text{OE1}}$
208	DSF	DSF	DSF

Section 3: Functional Description

This section describes the functional capabilities of the 86C928 that are beyond those provided by standard VGA controllers. Functions related to external hardware, such as video DAC and memory interfacing, are described in Section 12, Hardware Interface.

3.1 FUNCTIONAL BLOCKS

The 86C928 has 8 major functional blocks. These are depicted in Figure 3-1.

The Bus Interface Unit provides an interface to an ISA, a 386DX/486 local bus or an EISA bus. The Sequence Controller Unit generates display memory timing signals and display FIFO control signals, as well as the various clocks. The CRT Controller Unit generates the synchronization signals for the display monitor. The Memory Interface Unit generates display memory control and address signals.

There are two internal FIFO's: a display buffer and a data buffer for the enhanced (accelerated) commands.

The Attribute Controller Unit takes data from the display FIFO and formats it for screen display. The Data Manipulator/Graphics Controller Unit and Graphics Engine work together to produce acceleration of graphics commands, such as bitBLT's through and across the plane.

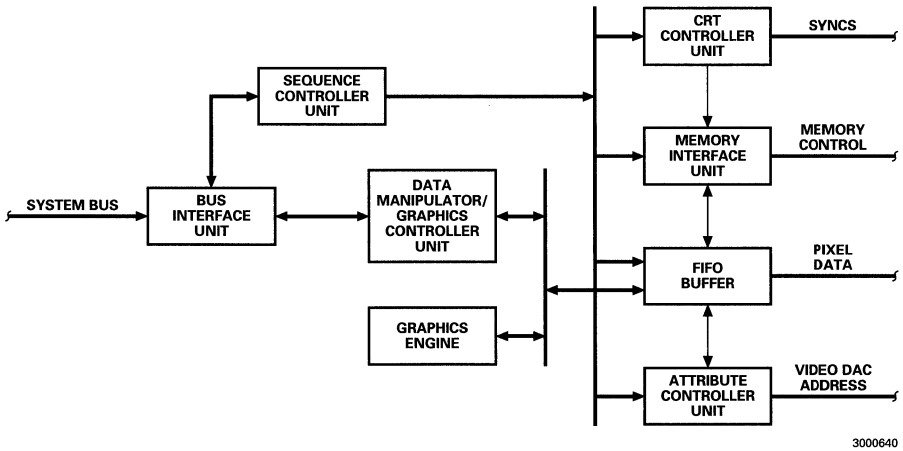

Figure 3-1. Functional Block Diagram

3.2 REGISTER ACCESS

In addition to all standard VGA and backward compatibility registers, the 86C928 contains several groups of registers providing advanced capabilities. These register groups must be unlocked before they can be accessed for reading or writing. This section explains how to unlock and relock each group.

Access to the S3 VGA Register group is gained by loading the bit pattern 01xx10xx (x = don't care) into Register Lock 1 (3?5H, Index 38H).

Access to the System Control and System Extension Register groups is gained by loading 101xxxxx into Register Lock 2 (3?5H, Index 39H).

Access to the Enhanced Graphic Command group is gained by setting bit 0 of the System Configuration register (3?5H, Index 40H) to 1. Note that the System Control Register group must be unlocked before this can be done.

Access to any register group can be re-locked by writing a bit pattern that changes any of the significant (non-don't care) bits.

3.3 VGA SETUP/ENABLE (ISA Only)

There are two standard methods of implementing VGA setup and configuration. One is the hardware method, where the $\overline{\text{VGAEN}}$ pin is strapped low to enable the video subsystem.

If $\overline{\text{VGAEN}}$ is strapped high, the software system setup method is used. Bit 4 of the Video Subsystem Access/Setup register (46E8H) is set to 1, bit 0 of the POS Mode Option Select register (102H) is set to 1 and then bit 3 of the 46E8H register is set to 1. This enables the video subsystem.

If bit 8 of configuration strapping (pin PD8) is 1, the 86C928 acts as a regular VGA for setup and bit 4 of the Video Subsystem Access/Setup register is used. If PD8 is set to 0, then bit 5 of the Video Subsystem Access/Setup register is used for setup.

3.4 MODE AND CURSOR SETUPS

The 86C928 supports all standard VGA and VESA-compliant extended VGA modes. In addition, it offers enhanced (accelerated) modes beyond these standards. This section explains the setup methods for the various modes and the hardware cursor.

3.4.1 VGA Mode Setup

The 86C928 powers up into a standard VGA mode determined by the BIOS. The mode can then be altered by programming the standard VGA registers. All standard VGA modes are supported and the 86C928 remains in VGA mode until the Enhanced functions are enabled.

The 86C928 also supports the following extended VGA modes without providing hardware acceleration. The 4 bits/pixel modes operate just like the VGA planar modes and the 8 bits/pixel modes operate just like the VGA packed pixel modes.

- 640x480x8
- 800x600x4
- 800x600x8
- 1024x768x4
- 1024x768x8

See standard VESA-compliant documentation for the setup steps for these modes.

132 character text mode is supported. Bit 5 of the Miscellaneous 1 register (3?5H, Index 3AH) is set to one while loading the character fonts. It is then reset to 0. Bit 6 of the Memory Configuration register (3?5H, Index 31H) is then set to 1 to enable the high speed text display font fetch (132 character) mode.

3.4.2 Backward Compatibility Modes Setup

The 86C928 is hardware compatible with CGA, MDA, and Hercules Graphics Card (HGC) standards which are based on the Motorola 6845 CRT controller. These standards are designed to run

on TTL (digital) monitors, however, the 86C928 uses analog displays for all modes. To emulate the 6845, the following additional setup is required before relinquishing control to 6845-based applications. This reconfiguration from VGA modes to corresponding CGA/MDA modes can be done with the aid of a BIOS call for 6845 emulation using INT 10. This procedure can be broken down into the following steps:

1. Character Generator Locking. The VGA BIOS reloads the character generator each time an alphanumeric mode is set whereas non-VGA modes (CGA, MDA, and Hercules) do not. Therefore the character table must be loaded onto plane 2 when the controller is still in the VGA mode.

2. Video DAC color compatibility. Non-VGA modes use 6-bit video output. Therefore, only the first 64 video DAC addresses need to be programmed and locked. Locking is done using bit 4 of the Backward Compatibility 2 register (3?5H, Index 33H).

3. Program default parameters. The 86C928 should be programmed for a 640 × 200 or 320 × 200 programming table for CGA, whereas MDA uses a 350-line programming table (Mode 7).

4. Set the S3 Registers for 6845 emulation by setting bit 3 of the Backward Compatibility 1 register (3?5H, Index 32H) to 1 to select non-VGA operation. Force high rate horizontal timing, then lock horizontal and vertical timing. These and other backward compatibility setup capabilities are provided by the Backward Compatibility 1 (3?5H, Index 32H), Backward Compatibility 2 (3?5H, Index 33H) and Backward Compatibility 3 (3?5H, Index 34H) registers.

At this point the 86C928 is hardware compatible with and can be programmed as a 6845. The program values will be inappropriate for VGA, but internal translation converts them to an equivalent value for analog monitors.

3.4.3 Enhanced Mode Setup

Enhanced mode provides a number of video modes. These are listed in the Introduction of this data book.

After the desired mode is selected, the Enhanced Graphic Command group is unlocked by setting bit 0 of the System Configuration register (3?5H, Index 40H) to 1. After that, bit 0 of the Advanced Function Control register (4AE8H) must be set to 1 to enable Advanced Display functions.

Several advanced capabilities are available when in Enhanced mode. Their setups are described next.

Enhanced mode registers are located at I/O addresses x2E8H, x6E8H, xAE8H and xEE8H (x = don't care). In order to prevent address conflicts with other I/O devices, they may be remapped to other I/O addresses by setting bit 4 of the Extended Mode register (3?5H, Index 43H) to 1. The new address becomes the original address XORed with 3A0H, resulting in the following I/O addresses: x148H, x548H, x948H and xD48H. The Video Subsystem Access/Setup Enable Register (46E8H) is not affected by the setting of bit 4 of the Extended Mode register. All 16 bits of the I/O address are decoded.

For improved performance, the Enhanced registers can be memory-mapped (MMIO). This function is enabled by setting bit 4 of the Extended Memory Control register (3?5H, Index 53H) or bit 5 of the Advanced Function Control register (4AE8H) to 1. Image transfers normally made by accessing I/O addresses E2E8H and E2EAH (the Pixel Data Transfer registers) are made instead by accessing any memory location in the 32-KByte address space from A0000H to A7FFFH. Accesses to the Enhanced command registers (write only) are made to particular locations in the A8000H to AFFFFH address range as shown in Table 3-1. The only exception is the Read Register Select register (BEE8H, Index 0FH), which cannot be accessed as a memory-mapped register.

Table 3-1. Memory-Mapped I/O Addresses for Enhanced Command Registers

I/O Address	Memory Address
8xE8H	A8xE8H
9xE8H	A9xE8H
AxE8H	AAxE8H
BxE8H	ABxE8H

The Enhanced modes normally share the display bitmap with the VGA graphics modes. Switching to a normal VGA graphics mode (using a BIOS clear screen command) destroys the Enhanced mode screen and vice versa. However, the 86C928 can be programmed to free up to 64 KBytes of memory in the off-screen area of the enhanced mode display for use by VGA text modes. Thus, it is possible to switch between a VGA text and the high resolution graphics modes without destroying the contents of display memory.

Simultaneous VGA text and Enhanced modes are enabled by setting bit 3 of the Miscellaneous 1 register (3?5H, Index 3AH) to 1. CPU and CRTC accesses are then directed to the top 32- or 64-KByte area of display memory depending on whether address bit 13 is 0 or 1 respectively.

Enhanced mode provides several sources of interrupts. Each of these sources can be independently enabled or disabled. This is done via the Subsystem Control register (42E8H, Write).

When in Enhanced mode, commands can be queued into a FIFO. This speeds writes since the CPU does not have to wait for a command to complete before issuing another command. This write posting capability is always enabled for Enhanced mode commands. Setting bit 3 of the System Configuration register (3?5H, Index 40H) to 1 enables the write posting capability during linear addressing and for the VGA modes.

3.4.4 Hardware Graphics Cursor Setup

Use of the 64x64 bits hardware graphics cursor is enabled by setting bit 0 of the Hardware Graphics Cursor Mode register (3?5H, Index 45H) to 1. This applies to all Enhanced modes. See Section 11.3.13 for more information.

Setting bit 5 of the Extended Video DAC Control register (3?5H, Index 55H) to 1 enables hardware cursor external operation mode. In this mode, the 86C928 provides the data required for the video DAC to control the cursor.

3.5 ENHANCED MODE FUNCTIONS

Enhanced Mode provides a level of performance far beyond what is possible with the VGA architecture. Hardware line drawing, BitBlt, rectangle fill, and image transfer between CPU memory and display memory are implemented. Also implemented are data manipulation functions, such as data extension, data source selection, and read/write bitplane control. Hardware clipping is supported by 4 registers (BEE8H, Indices 1-4) that define a rectangular clipping area. The use of these functions is explained in Section 11, Enhanced Mode Programming.

While in enhanced mode, the video memory bit map can be updated in two ways. One is to have the CPU write directly to memory. The other is to have the CPU issue commands to the Graphics Engine, which then controls pixel updating. The remainder of this section explains these two methods.

3.5.1 Direct Bit Map Accessing

When the CPU needs to do large block transfers to video memory, it can greatly speed this operation by directly accessing the video memory locations instead of reading or writing them through an I/O port. The 86C928 provides fast linear addressing of up to 4 MBytes of video memory. This requires that the CPU be operated in 386 protected mode.

The hardware busy flag, bit 9 of the Input/Output Status register (9AE8H), should be verified to be 0 (not busy) before fast linear addressing is enabled. Enabling is done by setting bit 4 of the Linear Address Window Control register (3?5H, Index 58H) or bit 4 of the Advanced Function Control register (4AE8H) to 1. Video memory can be mapped into the CPU memory address space

using the Linear Address Window Control (3?5H, Index 58H) and the Linear Address Window Position (3?5H, Index 59H and 5AH) registers.

The access window into memory can be restricted to 64 KBytes, allowing use of real mode. This is enabled by setting bit 3 of the Memory Configuration register (3?5H, Index 31H) to 1. A base address offset into display memory is then written into bits [3:0] of the CRT Register Lock register (3?5H, Index 35H) and into bits 2 and 3 of the Extended System Control 2 register (3?5H, Index 51H). (These latter extension bits enable access to up to 4 MBytes of video memory.) The offset is then added to the memory address if bit 0 of the Memory Configuration register (3?5H, Index 31H) is set to 1.

Direct bitmap accessing should not be enabled concurrently with memory-mapped I/O.

Bit 3 of the Memory Configuration register determines how the CPU memory access is translated into the display memory address. If this bit is set to 1, linear mapping is used. If it is set to 0, VGA mapping is used. VGA mapping depends on the VGA mode, which is still set even though the 86C928 is in Enhanced mode.

3.5.2 Read-Ahead Cache

The read-ahead cache function is enabled by setting bit 2 of the Linear Address Window Control (3?5H, Index 58H) register to 1. This causes extra data to be pre-fetched during video memory reads and cached. Subsequent reads of data in the cache (a cache hit) return data immediately. This function applies to linear addressing reads and VGA memory reads.

The amount of pre-fetch data returned is determined by the setting of bits 2-0 of the Extended Memory Control 2 (3?5H, Index 54H) register. The meaningful values are 1, 3 and 7 so that pre-fetched data is restricted to a full address boundary. The number represents the extra doublewords to be pre-fetched for linear addressing and VGA doubleword modes. It specifies the number of extra words to be pre-fetched for VGA word modes and the number of extra bytes to be pre-fetched for VGA byte modes.

Cache coherency is maintained through invalidation.

3.5.3 Bitmap Access Through the Graphics Engine

When updating pixels through the Graphics Engine, all CPU data moves through the Pixel Data Transfer register (E2E8H) for 16-bit transfers. This 16-bit register can be memory mapped as explained in section 3.4.3. The Pixel Data Transfer - Extension register (E2EAH) is also used for 32-bit transfers.

Each pixel is assigned a color index or true color value, which is translated via a programmable DAC before being displayed on a CRT. In addition, selected pixels can be masked off from being displayed by programming the DAC Mask register (03C6H).

Figure 3-2 is a flowchart for the process of updating the color of each pixel. The remainder of this section explains this flowchart.

Start at the block labeled 'New Color' in the middle of Figure 3-2. At this stage, a color has been determined that may or may not be used to update a pixel in the bitmap. How this color is determined will be covered later.

The first hurdle for the new color is the color compare process. If this is turned off (bit 8 of the Multifunction Control Miscellaneous (BEE8H, Index 0EH) register = 0), the new color is passed to the Write Mask register (AAE8H). If the plane to which the pixel update is directed has been masked off in this register, no update occurs. Otherwise, the new color is written to the bitmap.

If color compare is enabled (bit 8 of the Multifunction Control Miscellaneous register = 1), the new color (source) is compared to a color programmed into the Color Compare (B2E8H) register. The sense of the color comparison is determined by the SRC NE (source not equal) bit (bit 7) of the Multifunction Control Miscellaneous register. If this bit is 0, the new pixel color value is passed to the write mask only when the source color matches the color in the Color Compare register. If this bit is 1, the new pixel color value is passed to the write mask only when the source

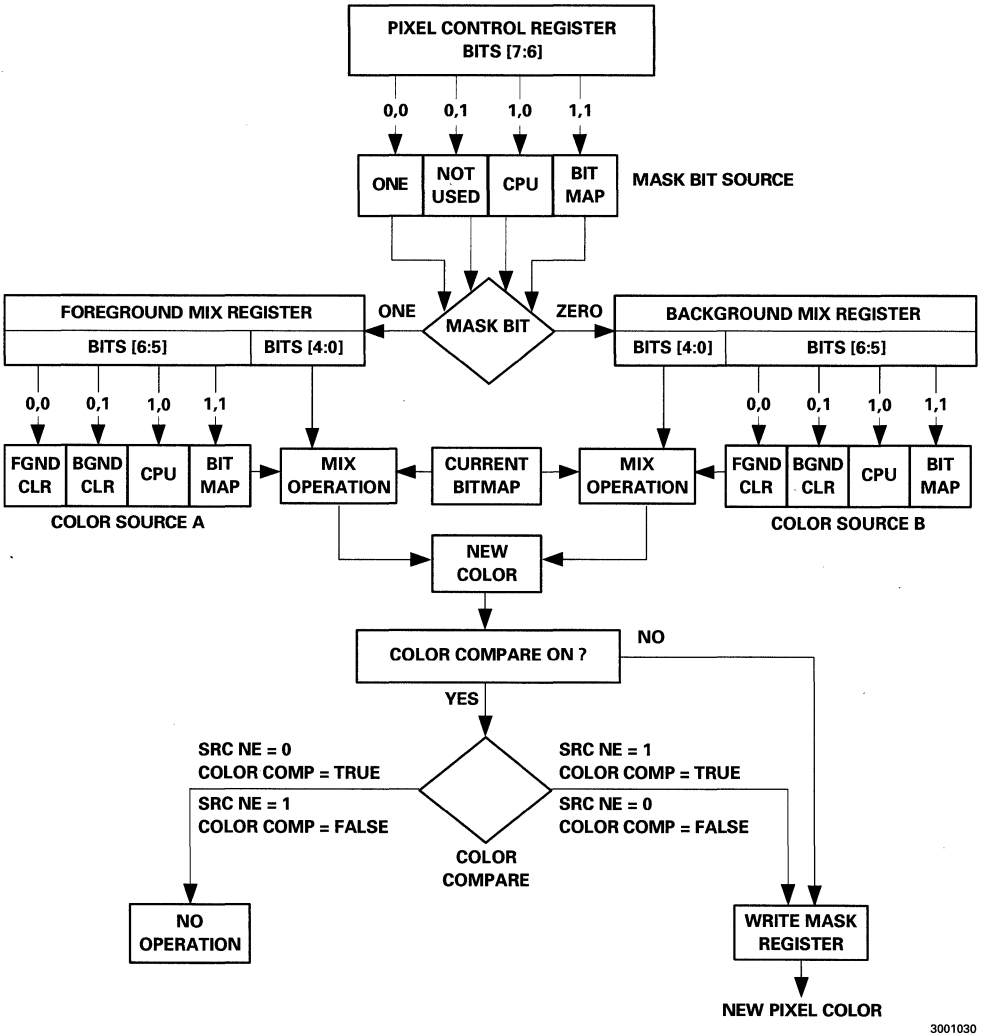

Figure 3-2. Pixel Update Flowchart

color does not match the color in the Color Compare register. If the new pixel color value is not passed to the write mask, no update occurs. Notice that the source color is used for the comparison, as opposed to the destination (bitmap) color used by the standard VGA color compare operation.

The new color is the result of a logical mix performed on a color source and the current color in the bitmap. For example, the color source could be XORed with the bitmap color. The new color can also be selected by operating on only the color source or the bitmap color, e.g., NOT color source. Both the color source and the logical mix operation are specified in either the Background Mix register (B6E8H) or the Foreground Mix register (BAE8H). Which of these two registers is used is determined by the settings of bits [7:6] of the Pixel Control register (BEE8H, Index A). Thus, the programmer can have two different pixel color index updating schemes specified at one time and choose one or the other by writing bits [7:6] of the Pixel Control register.

To set up the pixel color updating scheme, the programmer specifies one of four color sources by writing bits [6:5] of the Background Mix and Foreground Mix registers. The color sources are:

- Background Color register (A2E8H)
- Foreground Color register (A6E8H)
- CPU (via the Pixel Data Transfer register (E2E8H))
- Current bitmap color index

One of 16 logical operations is chosen by writing bits [4:0] of the Background Mix and Foreground Mix registers. Examples of logical operations are making the new pixel color index equal to the NOT of the current bitmap color index or making the new index equal to the XOR of the source and current bitmap indices.

When the logical operation and color source have been specified in the Background and Foreground Mix registers, bits [7:6] of the Pixel Control register are written to specify use of one or the other. If the resulting mask bit is a 'ONE', the Foreground Mix register is used. If the mask bit is a 'ZERO', the Background Mix register is used. There are three sources for the mask bit value:

- Always ONE (Foreground Mix register used)
- CPU (via the Pixel Data Transfer register (E2E8H))
- Bitmap

Setting bits [7:6] to 0,0 sets the mask bit to 'ONE'. All drawing updates to the video bitmap use the Foreground Mix register settings. This setup is used to draw solid lines, through-the-plane image transfers to video memory, and BitBLTs.

If bits [7:6] are set to 1,0, the mask bit source is the CPU. After the draw operation command is issued to the Command register port (9AE8), the mask bit is written into the Pixel Data register. A mask bit corresponding to every pixel drawn on the display must be provided via this register. If the mask bit is 'ONE', the Foreground Mix register is used. If the mask bit is 'ZERO', the Background Mix register is used. Note that if the color source is the CPU, the mask bit source cannot also be the CPU, and vice versa. This setup is used to transfer monochrome images such as fonts and icons to the screen.

If bits [7:6] are set to 11, the current bit map is selected as the mask bit source. The Read Mask register (AAE8H) is set up to indicate the active planes. When all bits of the read-enabled planes for a pixel are a 1, the mask bit 'ONE' is generated. If any one of the read-enabled planes is a 0, then a mask bit 'ZERO' is generated. If the mask bit is 'ONE', the Foreground Mix register is used. If the mask bit is 'ZERO', the Background Mix register is used. Note that if the color source is the bitmap, the mask bit source cannot also be the bitmap, and vice versa. This setting is used to bitBLT patterns and character images.

Section 4: CGA-Compatible Register Descriptions

In the following register descriptions, "U" stands for undefined or unused and "R" stands for reserved (write = 0, read = U).

See Appendix A for a table listing each register in this section and its page number.

Light Pen High Register (LPENH)

Read Only Address: 3D5H, Index 10H
Power-On Default: Undefined

15	14	13	12	11	10	9	8
U	U	Light Pen Strobe Address High					

Light Pen Low Register (LPENL)

Read Only Address: 3D5H, Index 11H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
Light Pen Strobe Address Low							

These registers contain the 14 memory address bits at the time the light pen strobe signal was detected in CGA and HGC modes.

These registers are not available in VGA mode.

The light pen is not actually connected to most systems, but the LP set/reset flag can be used to read the video memory addresses at the vertical retrace interval. The CPU can read the video memory address through this register. The screen mode and the video memory address have a known ratio at the vertical retrace interval. Therefore, the CPU can guess the screen mode (ex: low or high resolution, and text or graphics) from the light pen detect address at the vertical retrace.

The mode register is a write-only register, except in VGA mode. The CPU cannot read any screen mode information directly. Therefore the light pen detect address at the vertical retrace interval is used as a mode indicator indirectly in CGA and HGC modes.

CGA Mode Control Register (CGA_MODE)

Read/Write Address: 3D8H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	TEXT BLNK	HRES GRPH	DISP ENB	B/W MODE	GRPH MODE	HRES TEXT

Bit 0 HRES TEXT - High Resolution Text
0 = 40 x 25 alpha mode
1 = 80 x 25 alpha mode

Bit 1 GRPH MODE - Graphics Mode
0 = Alpha Mode
1 = Graphics Mode

Bit 2 B/W MODE - Black/White Mode
0 = Color enabled
1 = Color disabled. In 320 x 200 x 4 color mode, pixel bits represent:
00 = background
01 = cyan
10 = red
11 = white)

Bit 3 DISP ENB - Display Enable
0 = Screen Blank
1 = Video Enabled

Bit 4 HRES GRPH - High Resolution Graphics
0 = all other modes
1 = Enable 640 x 200 graphics mode

Bit 5 TEXT BLNK - Text Blinking
0 = Blinking disabled
1 = Blinking enabled

Bits 7–6 Reserved

CGA Color Select Register (CGA_COLOR)

Read/Write Address: 3D9H
Power-On Default: 00H

7	6	5	4	3	2	1	0
		SEL	SEL	BORDER/BKGR COLOR			
R	R	CSET	I-EN	I	R	G	B

In 640 x 200 (2 color) mode, pixel bit = 0 corresponds to black and pixel bit = 1 corresponds to the foreground color specified by bits 3-0 of this register.

Bit 0 BORDER/BKGR COLOR - Blue Border Select
0 = Blue not selected
1 = Select blue border in alpha mode, select blue background and border color in 320 × 200 graphics mode, select blue foreground color in 640 × 200 graphics mode.

Bit 1 BORDER/BKGR COLOR - Green Border Select
0 = Green not selected
1 = Select green border in alpha mode, select green background and border color in 320 × 200 graphics mode, select green foreground color in 640 × 200 graphics mode.

Bit 2 BORDER/BKGR COLOR - Red Border Select
0 = Red not selected
1 = Select red border in alpha mode, select red background and border color in 320 × 200 graphics mode, select red foreground color in 640 × 200 graphics mode.

Bit 3 BORDER/BKGR COLOR - Intensified Border
0 = No intensification
1 = Select intensified border in alpha mode, select intensified background and border color in 320 × 200 graphics mode, select intensified foreground color in 640 × 200 graphics mode.

Bit 4 SEL I-EN - Alternate Color Set
0 = Alternate color set not enabled
1 = Background color in alpha mode. Enable alternate (high intensity) color set in graphics mode.

Bit 5 SEL CSET - Select color set in 320x200 mode
0 = Pixel Bits
00 = Background determined by bits 3-0
01 = Green
10 = Red
11 = Yellow
1 = Pixel Bits
00 = Background determined by bits 3-0
01 = Cyan
10 = Violet
11 = White

Bits 7–6 Reserved

CGA Status Register (CGA_STAT)

Read Only Address: 3DAH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 1	= 1	= 1	= 1	VSY	= 1	LPF	$\overline{\text{DTM}}$

Bit 0 $\overline{\text{DTM}}$ - Border/Blanking Active
0 = Active display
1 = Border/Blanking Active

Bit 1 LPF - Light Pen Flag
0 = Light Pen Latch cleared
1 = Light Pen Latch triggered

Bit 2 = 1
0 = Light Pen switch closed (not available)
1 = Light Pen switch open

Bit 3 VSY - Vertical Sync Active
0 = Inactive Vertical Sync
1 = Active Vertical Sync

Bits 7–4 Reserved = 1

Clear Light Pen Flag Register (CLPEN)

Write Only Address: 3DBH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
Reset Light Pen Flag							

The CPU can control the light pen flag with I/O writes with any data to 3B9H or 3DCH to set, and 3BBH or 3DBH to reset. The CPU can guess the screen mode indirectly by reading the video memory address at the vertical retrace interval. When the light pen flag is set to 1, the video memory address at that time is stored in the Light Pen High and Low registers. The sequence to read the light pen detect address is:

1. Clear the light pen flag with an I/O write to 3BBH or 3DBH.
2. Wait for the vertical sync signal (VSY) to set.
3. Set light pen flag with an I/O write to 3B9H or 3DCH.
4. Read the light pen detect address.
5. Return to 1.

Set Light Pen Flag Register(SLPEN)

Write Only Address: 3DCH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
Set Light Pen Flag							

A write of anything to this register sets the light pen flag. See the description for the Reset Lightpen Flag register above.

Section 5: MDA- and HGC-Compatible Register Descriptions

In the following register descriptions, "U" stands for undefined or unused and "R" stands for reserved (write = 0, read = U). See Appendix A for a table listing each register in this section and its page number.

Light Pen High Register (LPENH)

Read Only Address: 3B5H, Index 10H
Power-On Default: Undefined

Refer to the description in Section 4.

Light Pen Low Register (LPENL)

Read Only Address: 3B5H, Index 11H
Power-On Default: Undefined

Refer to the description in Section 4.

MDA-Mode Control Register (MDA_MODE)

Read/Write Address: 3B8H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	TXT BLK	R	DSP ENB	R	R	R

Bits 2–0 Reserved

Bit 3 DSP ENB - Enable Display
0 = (screen blank)
1 = Video enabled

Bit 4 Reserved

Bit 5 TXT BLK - Text Blinking
0 = Blinking disabled
1 = Blinking enabled

Bits 7–6 Reserved

HGC- Mode Control Register (HGC_MODE)

Read/Write Address: 3B8H
Power-On Default: 00H

7	6	5	4	3	2	1	0
HGC PAGE	R	TXT BLK	R	DSP ENB	R	GRPPH MODE	R

Bit 0 Reserved

Bit 1 GRPH MODE - Graphics Mode
0 = 80 x 25 alpha mode enabled
1 = 720 x 348 graphics mode enabled

Bit 2 Reserved

Bit 3 DSP ENB - Enable Display
0 = (screen blank)
1 = Video enabled

Bit 4 Reserved

Bit 5 TXT BLK - Text Blinking
0 = Blinking disabled
1 = Blinking enabled

Bit 6 Reserved

Bit 7 HGC PAGE - Hercules Graphics Page
0 = graphics mode buffer displayed from B0000H (video page 0)
1 = graphics mode buffer displayed from B8000H (video page 1)

Set Light Pen Flag Register (HGC_SLPEN)

Write Only Address: 3B9H
Power-On Default: Undefined

Refer to the description in Section 4.

HGC Status Register (HGC_STS)

Read Only Address: 3BAH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
$\overline{VSY}$	= 1	= 1	= 1	V-DT	= 1	LPF	HSY

Bit 0 HSY - Horizontal Sync
0 = Active display
1 = Border/Blanking Active

Bit 1 LPF - Light Pen Flag
0 = Light Pen Flag off
1 = Light Pen Flag on

Bit 2 Reserved = 1

Bit 3 V-DT - Black/White Video
0 = B/W Video disabled
1 = B/W Video enabled

Bits 6–4 Reserved = 1

Bit 7 $\overline{VSY}$ - Vertical Sync Inactive
0 = Active Vertical Sync
1 = Inactive Vertical Sync

MDA Status Register (MDA_STS)

Read Only Address: 3BAH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 1	= 1	= 1	= 1	TEST	=1	= 1	HSY

Bit 0 HSY - Horizontal Sync
0 = Active display
1 = Border/Blanking Active

Bits 2–1 Reserved = 1

Bit 3 TEST
0 = B/W Video disabled
1 = B/W Video enabled

Bits 7–4 Reserved = 1

Clear Light Pen Flag Register (HGC_CLPEN)

Write Only Address: 3BBH
Power-On Default: Undefined

Refer to the description in Section 4.

HGC Configuration Register (CONFIG)

Write Only Address: 3BFH
Power-On Default: 00H

7	6	5	4	3	2	1	0
U	U	U	U	U	U	ENB PAGE	ENB GRPH

Bit 0 ENB PAGE - Enable Page
0 = Alpha mode is forced.
1 = Allows graphics mode.

Bit 1 ENB GRPH - Enable Graphics
0 = Bit 7 of Hercules Mode register can't be set, thus video memory occupies B0000H–B7FFFH, which allows the CGA to coexist.
1 = Bit 7 of Hercules Mode register can be set, allowing upper memory page access.

Section 6: VGA Standard Register Descriptions

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). A question mark in an address stands for a hexadecimal value of either 'B' or 'D'. If bit 0 of the Miscellaneous Output Register (3C2H, Write) is set to 1, the address is based at 3DxH for color emulation. If this bit is reset to 0, the address is based at 3BxH for monochrome emulation.

See Appendix A for a table listing each register in this section and its page number.

6.1 GENERAL REGISTERS

This section describes general input status and output control registers.

Miscellaneous Output Register (MISC)

Write Only — Address: 3C2H
Read Only — Address: 3CCH
Power-On Default: 00H

This register controls miscellaneous output signals. A hardware reset sets all bits to zero.

7	6	5	4	3	2	1	0
$\overline{\text{VSP}}$	$\overline{\text{HSP}}$	PGSL	= 0	CLK 1	SEL 0	ENB RAM	IOA SEL

Bit 0 IOA SEL - I/O Address Select
0 = Monochrome emulation. Address based at 3Bx.
1 = Color emulation. Address based at 3Dx.

Bit 1 ENB RAM - Enable RAM Access
0 = Disable access of the video memory from the CPU.
1 = Enable access of the video memory from the CPU.

Bit 3–2 Clock Select - These two bits select the video clock source
00 = Selects 25.175MHz clock for 640 horizontal pixels
01 = Selects 28.322MHz clock for 720 horizontal pixels
10 = Reserved
11 = Enable dot clock select bits in the Mode Control register (CR42), bits 3-0. This is an enhanced function.

Bit 4 Reserved = 0

Bit 5 PGSL - Page Select
0 = Select the low 64K page of memory.
1 = Select the high 64K page of memory.

Bit 6 $\overline{\text{HSP}}$ - Negative Horizontal Sync Pulse
0 = Select a positive horizontal retrace sync pulse.
1 = Select a negative horizontal retrace sync pulse.

Bit 7 $\overline{\text{VSP}}$ - Negative Vertical Sync Pulse
0 = Select a positive vertical retrace sync pulse.
1 = Select a negative vertical retrace sync pulse.

Bits 7-6 select the vertical size as shown in the following table;

Bit 6	Bit 7	Vertical size	Bit 6	Bit 7	Vertical Size
0	0	Reserved	1	0	350 lines
1	0	400 lines	1	1	480 lines

Feature Control Register (FCR_WT, FCR_AD)

Write Only Address: 3?AH
Read Only Address: 3CAH
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	VSSL	= 0	= 0	= 0

Bits 2–0 Reserved = 0

Bit 3 VSSL - Vertical Sync Select
0 = Enable normal vertical sync output to the monitor
1 = The 'vertical sync' output is the logical OR of 'vertical sync' and 'vertical display enable'.

Bits 7–4 Reserved = 0

Input Status 0 Register (STATUS_0)

Read Only Address: 3C2H
Power-On Default: Undefined

This register indicates the status of the VGA adapter.

7	6	5	4	3	2	1	0
CRT INTPE	= 0	= 0	MON SENS	= 0	= 0	= 0	= 0

Bits 3–0 Reserved = 0

Bit 4 MON SENS - Monitor Sense
0 = Selected sense switch off
1 = Selected sense switch on

Bits 6–5 Reserved = 0

Bit 7 CRT INTPE - CRT Interrupt
0 = Vertical retrace is occurring
1 = Vertical retrace is not occurring. Video is being displayed.

Input Status 1 Register (STATUS_1)

Read Only Address: 3?AH
Power-On Default: Undefined

This register indicates video sync timing and video wraparound.

7	6	5	4	3	2	1	0
= 0	= 0	TST-VDT 1	0	VSY	= 1	LPF	$\overline{\text{DTM}}$

Bit 0 $\overline{\text{DTM}}$ - Display Mode Inactive
0 = The display is in the display mode.
1 = The display is not in the display mode. Either the horizontal or vertical retrace period is active.

Bit 1 LPF - Light Pen Flag
0 = Light pen has not been triggered.
1 = Light pen has been triggered.

Bit 2 Reserved = 1

Bit 3 VSY - Vertical Sync
0 = Display is in the display mode.
1 = Display is in the vertical retrace mode.

Bits 5–4 TST-VDT - Test
Video Data Feedback 1,0. These bits are feedback video signals to do read back tests. These bits are selectively connected to two of the eight color outputs of the attribute controller. Bits 5 and 4 of the color plane enable register (AR12) control the multiplexer for this video output wrap wiring.

Bits 7–6 Reserved = 0

6.2 SEQUENCER REGISTERS

The sequencer registers are located at two-byte address spaces. These registers are accessed by first writing the data to the index register of the sequencer at I/O address 3C4H and then writing to or reading from the data register at 3C5H.

Sequencer Index Register (SEQX)

Read/Write Address: 3C4H
Power-On Default: Undefined

This register is loaded with a binary value that indexes the sequencer register for read/write data. This value is referred to as the "Index Number" of the SR register (SR0–4) in this document.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	SEQ ADDRESS		

Bits 2–0 SEQ ADDRESS - Sequencer Register Index
A binary value indexing the register where data is to be accessed.

Bits 7–3 Reserved = 0

Sequencer Data Register (SEQ_DATA)

Read/Write Address: 3C5H
Power-On Default: Undefined

This register is the data port for the sequencer register indexed by the Sequencer Index register (3C4H).

7	6	5	4	3	2	1	0
SEQ DATA							

Bit 7–0 SEQ DATA - Sequencer Register Data
Data to the sequencer register indexed by the sequencer address index.

Reset Register (RST_SYNC) (SR0)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	$\overline{\text{SYN}}$ RST	$\overline{\text{ASY}}$ RST

Bit 0 $\overline{\text{ASY}}$ RST - Asynchronous Reset
0 = Generate and hold the system in a reset condition.
1 = Release the reset if bit 0 is in the inactive state.

Bit 1 $\overline{\text{SYN}}$ RST - Synchronous Reset
0 = Generate and hold the system in a reset condition.
1 = Release the reset if bit 1 is in the inactive state.

Bits 7–2 Reserved = 0

Clocking Mode Register (CLK_MODE) (SR1)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 01H

This register controls the operation mode of dot clock and character clock.

7	6	5	4	3	2	1	0
= 0	= 0	SCRN OFF	SHF 4	DCK 1/2	SHF LD	= 0	$\overline{\text{9DC}}$

Bit 0 $\overline{\text{9DC}}$ - 9 Dot Clock Select
0 = Character clocks 9 dots wide are generated.
1 = Character clocks 8 dots wide are generated.

Bit 1 Reserved = 0

Bit 2 SHF LD - Shift Load
0 = Load the video serializer every character clock.
1 = Load the video serializers every other character clock.

Bit 3 DCK 1/2 - DCLK Divide
0 = Set the Dot Clock to the same frequency as the Master Clock.
1 = Divide the Master Clock by 2 to derive the Dot Clock.

Bit 4 SHF 4 - Shift 4
0 = Load the serializers every character clock cycle.
1 = Load the serializers every fourth character clock cycle.

Bit 5 SCRN OFF - Screen Off
0 = Screen is turned on.
1 = Screen is turned off.

Bit 7–6 Reserved = 0

Enable Write Plane Register (EN_WT_PL) (SR2)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 02H

This register selects write protection or write permission for CPU write access into video memory.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	EN.WT.PL.			

Bits 3–0 EN.WT.PL - Enable Write to a Plane
0 = Disables writing into the corresponding plane.
1 = Enables the CPU to write to the corresponding color plane.

Bits 7–4 Reserved = 0

Character Font Select Register (CH_FONT_SL) (SR3)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 03H

7	6	5	4	3	2	1	0
		SLA	SLB	SLA		SLB	
= 0	= 0	2	2	1	0	1	0

In text modes, bit 3 of the attribute byte normally turns the foreground intensity on or off. This bit can be redefined to be a switch between two character sets. The switch is enabled when there is a difference between the value of character font select A and character font select B bits. Memory Mode (SR4) register bit 1 = 1 (extended memory) enables all bits of this function; otherwise character fonts 0 and 4 are available. 256 KBytes of video memory support 8 character sets. This register is reset to 0 asynchronously during a system reset.

Bits 4, 1–0 SLB - Select Font B
This value selects the portion of plane 2 used to generate text character fonts when bit 3 of the attribute byte is a logical 1, according to the following table:

Bits 4,1,0	Font Table Location	Bits 4, 1,0	Font Table Location
000	First 8K of plane 2	100	Second 8K of plane 2
001	Third 8K of plane 2	101	Fourth 8K of plane 2
010	Fifth 8K of plane 2	110	Sixth 8K of plane 2
011	Seventh 8K of plane 2	111	Eighth 8K of plane 2

Bits 5, 3–2 SLA - Select Font B
This value selects the portion of plane 2 used to generate text character fonts when bit 3 of attribute byte is a logical 0, according to the same table as the character font select B.

Bits 7–6 Reserved = 0

Memory Mode Control Register (MEM_MODE) (SR4)

Read/Write Address: 3C5H, Index 04H
Power-On Default: 00H

This register controls CPU memory addressing mode.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	CHN 4M	O/E MODE	EXT MEM	= 0

Bit 0 Reserved = 0

Bit 1 EXT MEM - Extended Memory Access
0 = Memory access restricted to 16/32 KBytes.
1 = Allows complete memory access to 256 KBytes. Required for VGA.

Bit 2 O/E MODE - Odd/Even Addressing Mode
This bit affects only CPU write data accesses into video memory. Bit 3 of this register must be 0 for this bit to be effective.
0 = Enables the odd/even addressing mode. Even addresses access planes 0 and 2. Odd addresses access planes 1 and 3.
1 = Directs the system to use a sequential addressing mode.

Bit 3 CHN 4M - Chain 4 Mode
0 = Enables odd/even mode.
1 = Chain 4 Mode. This bit selects modulo 4 addressing for CPU access to display memory. A logical 1 directs the two lower order bits of the CPU address used to select the plane in video memory to be accessed as follows:

A1	A0	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

Bits 7–4 Reserved = 0

6.3 CRT CONTROLLER REGISTERS

The CRT controller registers are located at two locations in I/O address space. These registers are accessed by first writing to the index register of the CRT controller and then accessing the data register. The index register is located at I/O address 3?4H and the CRT Controller Data register is at 3?5H. Which address is used (3BX or 3DX) depends on bit 0 of the Miscellaneous Output register at 3C2H.

CRT Controller Index Register (CRTC_ADR) (CRX)

Read/Write Address: 3?4H
Power-On Default: 00H

This register is loaded with a binary value that indexes the CRT controller register where data is to be accessed. This value is referred to as the "Index Number" of the CR register (CR00–18). This register is also used as an index to the S3 VGA registers, the System Control Registers and the System Extension registers.

7	6	5	4	3	2	1	0
CRTC ADDRESS							

Bits 7–0 CRTC ADDRESS - CRTC Register Index
A binary value indexing the register where data is to be accessed.

CRT Controller Data Register (CRTC_DATA) (CRT)

Read/Write Address: 3?5H
Power-On Default: Undefined

This register is the data port for the CRT controller register indexed by the CRT Controller Address register.

7	6	5	4	3	2	1	0
CRTC DATA							

Bits 7–0 CRTC DATA - CRTC Register Data
Data to the CRT controller register indexed by the CRT controller address index.

Horizontal Total Register (H_TOTAL) (CR0)

Read/Write Address: 3?5H, Index 00H
Power-On Default: Undefined

This register defines the number of characters in the horizontal scan interval including retrace time.

7	6	5	4	3	2	1	0
HORIZONTAL TOTAL							

Bits 7–0 HORIZONTAL TOTAL.
The total number characters – 5. The value controls the period of the horizontal retrace output signal. An internal horizontal character clock inputs to the CRT Controller, and all horizontal and vertical timings are based upon this register. Comparators are used to compare register values with horizontal character values to provide horizontal timings.

Horizontal Display End Register (H_D_END) (CR1)

Read/Write Address: 3?5H, Index 01H
Power-On Default: Undefined

This register defines the number of characters to be displayed per horizontal line.

7	6	5	4	3	2	1	0
HORIZONTAL DISPLAY END							

Bits 7–0 HORIZONTAL DISPLAY END
A value one less than the total number of displayed characters.

Start Horizontal Blank Register (S_H_BLNK) (CR2)

Read/Write Address: 3?5H, Index 02H
Power-On Default: Undefined

This register determines where the horizontal blanking output signal becomes active in the horizontal timing.

7	6	5	4	3	2	1	0
START HORIZONTAL BLANK							

Bits 7–0 START HORIZONTAL BLANK
The horizontal blanking signal becomes active when the horizontal character counter reaches this value.

End Horizontal Blank Register (E_H_BLNK) (CR3)

Read/Write Address: 3?5H, Index 03H
Power-On Default: Undefined

This register determines the horizontal blanking output signal width and the display enable skew.

7	6	5	4	3	2	1	0
R	DSP-SKW 1	0	END HORIZONTAL BLANK				

Bits 4–0 END HORIZONTAL BLANK
A value equal to the six least-significant bits of the horizontal character counter value at which time the horizontal blanking signal becomes inactive (logical 0). To obtain a blanking signal of width W, the following algorithm is used: value of Start Horizontal Blank register + width of blanking signal in character clock units = 6-bit result to be programmed into the End Horizontal Blanking register. Bit number 5 is located in the End Horizontal Sync Position register (CR05 bit 7).

Bits 6–5 DSP-SKW - Display Skew
These two bits determine the amount of display enable skew. Display enable skew control provides sufficient time for the CRT Controller to access the display buffer to obtain a character and attribute code, access the character generator font, and then go through the Horizontal Pixel Panning register in the Attribute Controller. Each access requires the display enable signal to be skewed one character clock unit so the video output is synchronous with the horizontal and vertical retrace signals. The bit values and amount of skew are shown in the following table:
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 Reserved

Start Horizontal Sync Position Register (S_H_SY_P) (CR4)

Read/Write Address: 3?5H, Index 04H
Power-On Default: Undefined

This register is used to adjust the screen center horizontally, and to specify the character position at which the Horizontal Sync Pulse becomes active.

7	6	5	4	3	2	1	0
START HORIZONTAL SYNC POSITION							

Bits 7–0 START HORIZONTAL SYNC POSITION.
The value programmed is a binary count of the character position number at which the horizontal sync signal becomes active.

End Horizontal Sync Position Register (E_H_SY_P) (CR5)

Read/Write Address: 3?5H, Index 05H
Power-On Default: Undefined

This register specifies the character position at which the Horizontal Retrace Pulse becomes inactive (logical 0).

7	6	5	4	3	2	1	0
EHB b5	HOR-SKW 1	0	END HORIZONTAL SYNC POS				

Bits 4–0 END HORIZONTAL SYNC POS
A value equal to the five least significant bits of the horizontal character counter value at which time the horizontal sync signal becomes inactive(logical 0). To obtain a sync signal of width W, the following algorithm is used: Value of Horizontal Sync Position register + width of horizontal retrace signal in character clock units = 5-bit result to be programmed into the End Horizontal Sync register.

Bits 6–5 HOR-SKW - Horizontal Skew
These bits control the skew of the horizontal retrace signal. A binary 00 equals no horizontal retrace delay. For some modes, it is necessary to provide a horizontal retrace signal that takes up the entire blanking interval. Some internal timings are generated by the falling edge of the horizontal retrace signal. To guarantee the signals are latched properly, the retrace signal is started before the end of the display enable signal, and then skewed several character clock times to provide the proper screen centering.

Bit 7 EHB b5
End Horizontal Blanking bit 5.

Vertical Total Register (V_TOTAL) (CR6)

Read/Write Address: 3?5H, Index 06H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
VERTICAL TOTAL							

Bits 7–0 VERTICAL TOTAL
This is the low-order eight bits of a 10-bit register. The binary value represents the number of horizontal raster scans on the CRT screen – 2, including vertical retrace. The value in this register determines the period of the vertical retrace signal.

Bit 8 Is contained in the CRTC Overflow register, bit 0

Bit 9 Is contained in the CRTC Overflow register, bit 5.

CRTC Overflow Register (OVFL_REG) (CR7)

Read/Write Address: 3?5H, Index 07H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
VRS 9	VDE 9	VT 9	LCM 8	SVB 8	VRS 8	VDE 8	VT 8

The CRT controller overflow register contains the ninth bit (B8) and tenth bit (B9) of several other control registers. This register is used in conjunction with registers for which it supplies the ninth and tenth bits.

Bit 0 Bit 8 of the Vertical Total register

Bit 1 Bit 8 of the Vertical Display End register

Bit 2 Bit 8 of the Vertical Retrace Start register

Bit 3 Bit 8 of the Start Vertical Blank register

Bit 4 Bit 8 of the Line Compare register

Bit 5 Bit 9 of the Vertical Total register

Bit 6 Bit 9 of the Vertical Display End register

Bit 7 Bit 9 of the Vertical Retrace Start register

Preset Row Scan Register (P_R_SCAN) (CR8)

Read/Write Address: 3?5H, Index 08H
Power-On Default: Undefined

This register is used for the pixel scrolling and panning, and text formatting and vertical scrolling.

7	6	5	4	3	2	1	0
= 0	BYTE-PAN 1	0	PRE-SET ROW SCAN COUNT				

Bits 4–0 PRE-SET ROW SCAN COUNT
This value specifies the starting row scan count on the screen start. Each horizontal retrace increments the horizontal row scan counter. The horizontal row scan counter is cleared at maximum row scan count, which is programmed through register CR9. This register is used for software controlled vertical scrolling.

Bits 6–5 BYTE-PAN
These two bits control horizontal byte panning. The value of these two bits specifies the number of character clocks for horizontal panning scroll.

Bit 7 Reserved = 0

Maximum Scan Line Register (MAX_S_LN) (CR9)

Read/Write Address: 3?5H, Index 09H
Power-On Default: Undefined

This register specifies the number of scan lines per character row, having one scanning control bit and two overflow bits.

7	6	5	4	3	2	1	0
DBL SCN	LCM 9	SVB 9	MAX SCAN LINE				

Bits 4–0 MAX SCAN LINE
Number of scan lines per row minus one.

Bit 5 SVB 9
Bit 9 of the Start Vertical Blank Register (CR15)

Bit 6 LCM 9
Bit 9 of the Line Compare Register (CR18)

Bit 7 DBL SCN
0 = Normal operation
1 = Enables double scanning operation. Each line is displayed twice by repeating the row scan counter and video memory address. Vertical parameters in the CRT controller are not affected.

Cursor Start Scan Line Register (CSSL) (CRA)

Read/Write Address: 3?5H, Index 0AH
Power-On Default: Undefined

The cursor start register defines the row scan of a character line where the cursor is beginning.

7	6	5	4	3	2	1	0
= 0	= 0	CSR OFF	CSR CURSOR START SCAN LINE				

Bits 4–0 CSR CURSOR START SCAN LINE
The value in the register is one less than the starting cursor row scan. When the cursor start register is programmed with a value greater than the cursor end register, no cursor is generated.

Bit 5 CSR OFF
0 = Turns on the text cursor.
1 = Turns off the text cursor.

Bits 7–6 Reserved = 0

Cursor End Scan Line Register (CESL) (CRB)

Read/Write Address: 3?5H, Index 0BH
Power-On Default: Undefined

This register defines the row scan of a character line where the cursor is ending.

7	6	5	4	3	2	1	0
= 0	CSR-SKW 1	0	CURSOR END SCAN LINE				

Bits 4–0 CURSOR END SCAN LINE.
Last scan line number for the text cursor. If the value of cursor start scan line is greater than the value of cursor end line, then no cursor is generated.

Bits 6–5 CSR-SKW - Cursor Skew
These bits control the delay skew of the cursor signal. Cursor skew delays the text cursor by the selected number of clocks. For example, a skew of 1 moves the cursor

right one character position on the screen.
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 Reserved = 0

Start Address High Register (STA(H)) (CRC)

Read/Write Address: 3?5H, Index 0CH
Power-On Default: Undefined

15	14	13	12	11	10	9	8
DISPLAY START ADDRESS (HIGH)							

The start address is a 16-bit value. This value specifies the first address after a vertical retrace at which the display on the screen begins on each screen refresh. These are the high order start address bits.

Start Address Low Register (STA(L)) (CRD)

Read/Write Address: 3?5H, Index 0DH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS (LOW)							

Start address (low) contains the 8 low order bits of the address.

Cursor Location Address High Register (CLA(H)) (CRE)

Read/Write Address: 3?5H, Index 0EH
Power-On Default: Undefined

15	14	13	12	11	10	9	8
CURSOR LOCATION ADDRESS (HIGH)							

The cursor location address is a 16-bit value. This value specifies the cursor location address of the video memory where the text cursor is active. This register contains the high order bits of the address. This register is also used for the hardware cursor foreground color in Enhanced Mode.

Cursor Location Address Low Register (CLA(L)) (CRF)

Read/Write Address: 3?5H, Index 0FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
CURSOR LOCATION ADDRESS (LOW)							

Cursor location address (low) contains the 8 low order bits of the address. This register is also used for the hardware cursor background color in Enhanced Mode.

Vertical Retrace Start Register (VRS) (CR10)

Read/Write Address: 3?5H, Index 10H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
VERTICAL RETRACE START							

Bits 7–0 VERTICAL RETRACE START.
These are the low-order 8 bits of the vertical sync start position, programmed in horizontal scan lines. Bits 8 and 9 are in the Overflow register (CR7).

Vertical Retrace End Register (VRE) (CR11)

Read/Write Address: 3?5H, Index 11H
Power-On Default: 0xH

This register controls the vertical interrupt and CR0-7

7	6	5	4	3	2	1	0
LOCK R0-7	$\overline{\text{REF}}$ 3/5	DIS VINT	$\overline{\text{CLR}}$ VINT	VERTICAL RET END			

Bits 3–0 VERTICAL RET END
These bits determine the horizontal scan count value when the vertical sync signal output becomes inactive. The register is programmed in units of horizontal scan lines. To obtain a vertical sync signal of width W, the following algorithm is used: value of Vertical Sync Start register + width of vertical sync signal in horizontal scan units = 4-bit result to be programmed into the Vertical Retrace End register.

Bit 4 $\overline{\text{CLR}}$ VINT - Clear Vertical Retrace Interrupt
0 = Vertical retrace interrupt cleared.
1 = The flip-flop is able to catch the next interrupt request.

At the end of active vertical display time, a flip-flop is set for a vertical interrupt. The output of this flip-flop goes to the system interrupt controller. The CPU has to reset this flip-flop by writing a logical 0 to this bit while in the interrupt process, then set the bit to 1 to allow the flip-flop to catch the next interrupt request. Do not change the other bits in this register. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on.

Bit 5 DIS VINT - Disable Vertical Interrupt
0 = Vertical retrace interrupt enabled.
1 = Vertical interrupt disabled. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on.

Bit 6 REF $\overline{3}$/5 - Refresh Cycle Select
0 = Three DRAM refresh cycles generated per horizontal line
1 = Five DRAM refresh cycles generated per horizontal line. Selecting five refresh cycles allows use of the VGA chip with slow sweep rate displays (15.75KHz). This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on.

Bit 7 LOCK R0-7 - Lock Writes to CRT Controller Registers
0 = Writing to all CRT Controller registers enabled.
1 = Writing to all bits of the CRT Controller registers CR0–CR7 except bit 4 of CR7 (LCM8) disabled. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on.

Vertical Display End Register (VDE) (CR12)

Read/Write Address: 3?5H, Index 12H
Power-On Default: Undefined

The vertical display enable end register defines 8 bits of the 10-bit address of the scan line where the display on the screen ends. The ninth and the tenth bits are located in the Overflow register (CR7).

7	6	5	4	3	2	1	0
VERTICAL DISPLAY END							

Bit 7–0 VERTICAL DISPLAY END
This value specifies 8 low order bits of a 10-bit value. This register specifies which scan line ends the active video area of the screen. It is programmed with the total number of lines minus one.

Offset Register (SCREEN-OFFSET) (CR13)

Read/Write Address: 3?5H, Index 13H
Power-On Default: Undefined

This register specifies the logical line width of the screen. The starting memory address for the next display row is larger than the current row by two, four or eight times this amount.

7	6	5	4	3	2	1	0
LOGICAL SCREEN WIDTH							

Bits 7–0 LOGICAL SCREEN WIDTH
The register defines the width of the display buffer. The byte starting address of the next display row is the byte starting address of current row + k* (contents of this register) where k = 2 in byte mode, k = 4 in word mode and k = 8 in double word mode.

Underline Location Register (ULL) (CR14)

Read/Write Address: 3?5H, Index 14H
Power-On Default: Undefined

This register specifies the horizontal row scan position of underline and display buffer addressing modes.

7	6	5	4	3	2	1	0
= 0	DBWD MODE	CNT BY4	UNDER LINE LOCATION				

Bits 4–0 UNDER LINE LOCATION
This value specifies the horizontal row scan count of a character row on which an underline occurs. The value is one less than the scan line number desired.

Bit 5 CNT BY4
0 = The memory address counter depends on bit 3 of CR17 (count by 2).
1 = The memory address counter is incremented every four character clocks.

The CNT BY4 bit is used when double word addresses are used.

Bit 6 DBLWD MODE - Doubleword Mode
0 = The memory addresses are byte or word addresses.
1 = The memory addresses are double word addresses.

Bit 7 Reserved = 0

Start Vertical Blank Register (SVB) (CR15)

Read/Write Address: 3?5H, Index 15H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
START VERTICAL BLANK							

Bits 7–0 START VERTICAL BLANK.
These are low 8 bits of a 10-bit register.

Bit 8 Is in the Overflow register (CR7).

Bit 9 Is in the Maximum Scan Line register (CR9). The value of these 10 bits is one less than the horizontal scan line count at which the vertical blanking signal becomes active.

End Vertical Blank Register (EVB) (CR16)

Read/Write Address: 3?5H, Index 16H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
END VERTICAL BLANK							

Bits 7–0 END VERTICAL BLANK
This register specifies the horizontal scan count value when the vertical blank signal output becomes inactive. The register is programmed in units of horizontal scan lines.

To obtain a width of vertical blank signal W, the following algorithm is used: (Value of Start Vertical Blank register minus 1) + width of vertical blank signal in horizontal scan units = 8-bit result to be programmed into the End Vertical Blank register.

CRTC Mode Control Register (CRT_MD) (CR17)

Read/Write Address: 3?5H, Index 17H
Power-On Default: 00H

This register is a multifunction control register, with each bit defining a different specification.

7	6	5	4	3	2	1	0
$\overline{\text{RST}}$	BYTE MODE	$\overline{\text{ADW}}$ 16K	= 0	CNT BY2	VT X2	$\overline{\text{4BK}}$ HGC	$\overline{\text{2BK}}$ CGA

Bit 0 $\overline{\text{2BK}}$ CGA - Bank 2 Mode for CGA Emulation
0 = Row scan counter bit 0 is substituted for memory address bit 13 during active display time.
1 = Memory address bit 13 appears on the memory address output bit 13 signal of the CRT controller.

This bit allows memory mapping compatibility with the IBM CGA graphics mode.

Bit 1 $\overline{\text{4BK}}$ HGC - Bank 4 Mode for HGA Emulation
0 = Row scan counter bit 1 is substituted for memory address bit 14 during active display time.
1 = Memory address bit 14 appears on the memory address output bit 14 signal of the CRT controller.

The combination of this bit and bit 0 of this register allows compatibility with Hercules HGC graphics memory mapping.

Bit 2 VT X2 - Vertical Total Double Mode
0 = Horizontal retrace clock selected.
1 = Horizontal retrace clock divided by two selected.

This bit selects horizontal retrace clock or horizontal retrace clock divided by two as the clock that controls the vertical timing counter. If the vertical retrace counter is clocked with the horizontal retrace clock divided by 2, then the vertical resolution is double.

Bit 3 CNT BY2 - Count By 2 Mode
0 = Memory address counter is clocked with the character clock input, and byte mode addressing for the video memory is selected.
1 = Memory address counter is clocked by the character clock input divided by 2, and word mode addressing for the video memory is selected.

Bit 4 Reserved = 0

Bit 5 $\overline{\text{ADW}}$ 16K - Address Wrap
0 = When word mode is selected by bit 6 of this register, memory address counter bit 13 appears on the memory address output bit 0 signal of the CRT controller and the video memory address wraps around at 16 KBytes.
1 = When word mode is selected by bit 6 of this register, memory address counter bit 15 appears on the memory address output bit 0 signal of the CRT controller.

This bit is useful in implementing IBM CGA mode.

Bit 6 BYTE MODE
0 = Word mode shifts all memory address counter bits down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output.
1 = Byte address mode.

Bit 7 $\overline{\text{RST}}$ - Hardware Reset
0 = Vertical and horizontal retrace pulses cleared.
1 = Vertical retrace enabled.

This bit does not reset any other registers or outputs.

Line Compare Register (LCM) (CR18)

Read/Write Address: 3?5H, Index 18H
Power-On Default: Undefined

This register is used to implement a split screen function. When the vertical scan counter value is equal to the contents of this register, the memory address counter is cleared to 0. The linear address counter then sequentially addresses the display buffer starting at address 0. Each subsequent row address is determined by the addition of the Offset register contents.

7	6	5	4	3	2	1	0
LINE COMPARE POSITION							

Bit 7–0 LINE COMPARE POSITION
This register is the low-order 8 bits of the compare targets. Bit 8 of this register is in the Overflow register (bit 4 of CR7). Bit 9 is in the Maximum Scan Line register (bit 6 of CR9).

CPU Latch Data Register (GCCL) (CR22)

Read Only Address: 3?5H, Index 22H
Power-On Default: Undefined

This register is used to read the CPU latch in the Graphics Controller.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER CPU LATCH - N							

Bits 7–0 GRAPHICS CONTROLLER CPU LATCH - N
Bits 1-0 of GR4 select the latch number N (3-0) of the CPU Latch.

Attribute Index Register (ATC_F/I) (CR24)

Read Only Address: 3?5H, Index 24H, 26H
Power-On Default: Undefined

This register is used to read the value of the Attribute Controller Index register and its associated internal address flip-flop (AFF).

7	6	5	4	3	2	1	0
$\overline{AFF}$	= 0	ATTRIBUTE CONTROLLER INDEX					

Bits 5–0 ATTRIBUTE CONTROLLER INDEX
This value is the Attribute Controller Index Data at I/O port 3C0H.

Bit 6 Reserved = 0

Bit 7 $\overline{AFF}$
Inverted Internal Address flip-flop

6.4 GRAPHICS CONTROLLER REGISTERS

The graphics controller registers are located at a two byte I/O address space. These registers are accessed by first writing an index to the Graphics Address register (at 3CEH) and then accessing the Data register (at 3CFH).

Graphics Controller Index Register (GRC_ADR) (GRX)

Read/Write Address: 3CEH
Power-On Default: Undefined

This register is loaded with a binary index value that determines which graphics controller register will be accessed. This value is referred to as the "Index Number" of the GR register (GR0–6).

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	GR CONT ADDRESS			

Bits 3–0 GR CONT ADDRESS - Graphics Controller Register Index
A binary value indexing the register where data is to be accessed.

Bits 7–4 Reserved = 0

Graphics Controller Data Register (GRC_DATA) (GRD)

Read/Write Address: 3CFH
Power-On Default: Undefined

This register is the data port for the graphics controller register indexed by the Graphics Controller Index register.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER DATA							

Bit 7–0 GRAPHICS CONTROLLER DATA - Graphics Controller Register Data
Data to the Graphics Controller register indexed by the graphics controller address.

Set/Reset Data Register (SET/RST_DT) (GR0)

Read/Write Address: 3CFH, Index 00H
Power-On Default: Undefined

This register represents the value written to all 8 bits of the respective memory plane when the CPU executes a memory write in write modes 0 and 3.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	SET/RESET DATA			

Bits 3–0 SET/RESET DATA.
These bits become the color value for CPU memory write operations. In write mode 0, the set/reset data can be enabled on the corresponding bit of the Enable Set/Reset Data register. In write mode 3, there is no effect on the Enable Set/Reset Data register.

Bits 7–4 Reserved = 0

Enable Set/Reset Data Register (EN_S/R_DT) (GR1)

Read/Write Address: 3CFH, Index 01H
Power-On Default: Undefined

These bits enable the set/reset data, and affect write mode 0.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	ENB SET/RST DATA			

Bits 3–0 ENB SET/RST DATA
When each bit is a logical 1, the respective memory plane is written with the value of the Set/Reset Data register. A logical 0 disables the set/reset data in a plane, and that plane is written with the value of CPU write data.

Bits 7–4 Reserved = 0

Color Compare Register (COLOR-CMP) (GR2)

Read/Write Address: 3CFH, Index 02H
Power-On Default: Undefined

These bits represent a 4-bit color value to be compared. In read mode 1, the CPU executes a memory read, the read data is compared with this value and returns the results. This register works in conjunction with the Color Don't Care register.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	COLOR COMPARE DATA			

Bits 3–0 COLOR COMPARE DATA
This value becomes the reference color used to compare each pixel. Each of the 8-bit positions of the read data are compared across four planes and a logical 1 is returned in each bit position for which the colors match.

Bits 7–4 Reserved = 0

Raster Operation/Rotate Count Register (WT_ROP/RTC) (GR3)

Read/Write Address: 3CFH, Index 03H
Power-On Default: Undefined

This register selects a raster operation function and indicates the number of bits the CPU data will be rotated (right) on the video memory write operation.

7	6	5	4	3	2	1	0
			RST-OP				
= 0	= 0	= 0	1	0	ROTATE-COUNT		

Bits 2–0 ROTATE-COUNT
These bits define a binary encoded value of the number of positions to right-rotate data during a CPU memory write. To write non-rotated data, the CPU must preset a count of 0.

Bits 4–3 RST-OP - Raster Operation
The data written to memory can operate logically with the data already in the processor latches. This function is not available in write mode 1. The logical functions are defined as follows:
00 = No operation
01 = Logical AND with latched data
10 = Logical OR with latched data
11 = Logical XOR with latched data

The logical function specified by this register is applied to data being written to memory while in modes 0, 2 and 3.

Bits 7–5 Reserved = 0

Read Plane Select Register (RD_PL_SL) (GR4)

Read/Write Address: 3CFH, Index 04H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
						RD-PL-SL	
= 0	= 0	= 0	= 0	= 0	= 0	1	0

The contents of this register represent the memory plane from which the CPU reads data in read mode 0. This register has no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored. Four memory planes are selected as follows:

Bits 1–0 RD-PL-SL - Read Plan Select
The memory plane is selected as follows:
00 = Plane 0
01 = Plane 1
10 = Plane 2
11 = Plane 3

Bits 7–2 Reserved = 0

Graphics Controller Mode Register (GRP_MODE) (GR5)

Read/Write Address: 3CFH, Index 05H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
	SHF-MODE		O/E	RD		WRT-MD	
= 0	256	O/E	MAP	CMP	= 0	1	0

This register controls the mode of the Graphics Controller as follows:

Bit 1–0 WRT-MD - Write Mode
These bits select the CPU write mode into video memory. The function of each mode is defined as follows:

00 = Write Mode 0. Each of four video memory planes is written with the CPU data rotated by the number of counts in the rotate register. If the Set/Reset register is enabled for any of four planes, the corresponding plane is written with the data stored in the set/reset register. Raster operations and bit mask registers are effective.

01 = Write Mode 1. Each of four video memory planes is written with the data in the processor latches. These latches are loaded during previous CPU read operations. Raster operation, rotate count, set/reset data, enable set/reset data and bit mask registers are not effective.

10 = Write Mode 2. Memory planes 0-3 are filled with 8 bits of the value of CPU write data bits 0-3, respectively. For example, if write data bit 0 is a 1, eight 1's are written to memory plane 0. The data on the CPU data bus is treated as the color value. The Bit Mask register is effective as the Mask register. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A logical 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset, Enable Set/Reset and Rotate Count registers are ignored.

11 = Write Mode 3. Each of four video memory planes is written with 8 bits of the color value contained in the set/reset register for that plane. The Enable Set/Reset register is not effective. Rotated CPU write data is ANDed with the bit mask register to form an 8-bit value that performs the same function as the Bit Mask register in write modes 0 and 2. This write mode can be used to fill an area with a single color and pattern.

Bit 2 Reserved = 0

Bit 3 RD CMP - Read Compare

0 = The CPU reads data from the video memory planes. The plane is selected by the Read Plane Select register. This is called read mode 0.

1 = The CPU reads the results of the logical comparison between the data in four video memory planes selected by the contents of the Color Don't Care register and the contents of the Color Compare register. The result is a 1 for a match and 0 for a mismatch on each pixel. This is called read mode 1.

Bit 4 O/E MAP - Odd/Even Addressing
0 = Standard addressing.
1 = Odd/even addressing mode selected. Even CPU addresses access plane 0 and 2, while odd CPU addresses access plane 1 and 3. This option is useful for emulating the CGA compatible mode. The value of this bit should be the inverted value programmed in bit 2 of the Sequencer Memory Mode register (SR4). This bit affects reading of display memory by the CPU.

Bit 5 SHF-MODE - Shift Mode
0 = Normal shift mode.
1 = The video shift registers in the graphics section are directed to format the serial data stream with even-numbered bits from both planes on the even-numbered planes and odd-numbered bits from both planes on the odd planes.

Bit 6 SHF-MODE - Shift Mode
0 = Bit 5 in this register controls operation of the video shift registers.
1 = The shift registers are loaded in a manner that supports the 256 color mode.

Bit 7 Reserved = 0

Memory Map Mode Control Register (MISC_GM) (GR6)

Read/Write Address: 3CFH, Index 06H
Power-On Default: Undefined

This register controls the video memory addressing.

7	6	5	4	3	2	1	0
				MEM-MAP		CHN	$\overline{\text{TXT}}$
= 0	= 0	= 0	= 0	1	0	O/E	/GR

Bit 0 $\overline{\text{TXT}}$/GR - Text/Graphics Mode
0 = Text mode display addressing selected.
1 = Graphics mode display addressing selected. When set to graphics mode, the character generator address latches are disabled.

Bit 1 CHN O/E - Chain Odd/Even Planes
0 = A0 address bit unchanged.
1 = CPU address bit A0 is replaced by a higher order address bit. The content of A0 determines which memory plane is to be addressed. A0 = 0 selects planes 0 and 2, and A0 = 1 selects planes 1 and 3. This mode can be used to double the address space into video memory.

Bits 3–2 MEM-MAP - Memory Map Mode
These bits control the address mapping of video memory into the CPU address space. The bit functions are defined below.
00 = A0000H to BFFFFH (128 KBytes)
01 = A0000H to AFFFFH (64 KBytes)
10 = B0000H to B7FFFH (32 KBytes)
11 = B8000H to BFFFFH (32 KBytes)

Bits 7–4 Reserved = 0

Color Don't Care Register (CMP_DNTC) (GR7)

Read/Write Address: 3CFH, Index 07H
Power-On Default: Undefined

This register is effective in read mode 1, and controls whether the corresponding bit of the Color Compare Register is to be ignored or used for color comparison.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	COMPARE PLANE SEL			

Bits 3–0 COMPARE PLANE SEL - Compare Plane Select
0 = The corresponding color plane becomes a don't care plane when the CPU read from the video memory is performed in read mode 1.
1 = The corresponding color plane is used for color comparison with the data in the Color Compare register.

Bits 7–4 Reserved = 0

Bit Mask Register (BIT_MASK) (GR8)

Read/Write Address: 3CFH, Index 08H
Power-On Default: Undefined

Any bit programmed to 0 in this register will cause the corresponding bit in each of four memory planes to be immune to change. The data written into memory in this case is the data which was read in the previous cycle, and was stored in the processor latches. Any bit programmed to 1 allows unimpeded writes to the corresponding bits in the plane.

7	6	5	4	3	2	1	0
BIT MASK							

Bits 7–0 BIT MASK
A logical 0 means the corresponding bit of each plane in memory is set to the corresponding bit in the processor latches. A logical 1 means the corresponding bit of each plane in memory is set as specified by other conditions.

6.5 ATTRIBUTE CONTROLLER REGISTERS

The attribute controller registers are located at the same byte I/O address for writing address and data. An internal address flip-flop (AFF) controls the selection of either the attribute index or data registers. To initialize the address flip-flop (AFF), an I/O read is issued at address 3BAH or 3DAH. This presets the address flip-flop to select the index register. After the index register has been loaded by an I/O write to address 3C0H, AFF toggles and the next I/O write loads the data register. Every I/O write to address 3C0H toggles this address flip-flop. However, it does not toggle for I/O reads at address 3C0H or 3C1H. The Attribute Controller Index register is read at 3C0H, and the Attribute Controller Data register is read at address 3C1H.

Attribute Controller Index Register (ATR_AD)

Read/Write Address: 3C0H
Power-On Default: Undefined

This register is loaded with a binary index value that determines which attribute controller register will be accessed. This value is referred to as the "Index Number" of the AR register (AR0–14).

7	6	5	4	3	2	1	0
R	R	ENB PLT	ATTRIBUTE ADDRESS				

Bits 4–0 ATTRIBUTE ADDRESS
A binary value that points to the attribute controller register where data is to be written.

Bit 5 ENB PLT
0 = Video display access to the palette registers disabled. The Attribute Controller register can be accessed by the CPU.
1 = Display video using the palette registers enabled (normal display operation). The palette registers (AR0–ARF) cannot be accessed by the CPU.

Bits 7–6 Reserved

Attribute Controller Data Register (ATR_DATA)

Read/Write Address: R: 3C1H/W: 3COH
Power-On Default: Undefined

This register is the data port for the attribute controller register indexed by the Attribute Controller Index register.

7	6	5	4	3	2	1	0
ATTRIBUTE DATA							

Bits 7–0 ATTRIBUTE DATA.
Data to the attribute controller register indexed by the attribute controller address.

Palette Registers (PLT_REG) (AR00-0F)

Read/Write Address: 3C1H/3C0H, Index 00H-0FH
Power-On Default: Undefined

These are 16, 6-bit registers pointed to by the index and color code. They allow a dynamic mapping between the text attribute or graphics color input and the display color on the CRT screen.

7	6	5	4	3	2	1	0
		SECONDARY			PRIMARY		
= 0	= 0	SR	SG	SB	R	G	B

Bits 5–0 PALETTE COLOR.
The six bit display color, bits 5-0 are output as SR, SG/I, SB/V, R, G and B, respectively.

Bits 7–6 Reserved = 0

Attribute Mode Control Register (ATR_MODE) (AR10)

Read/Write
Power-On Default: 00H

Address: 3C1H/3C0H, Index 10H

The contents of this register controls the attribute mode of the display function.

7	6	5	4	3	2	1	0
SEL V54	256 CLR	TOP PAN	= 0	ENB BLNK	ENB LGC	MONO ATRB	$\overline{TX}$ /GR

Bit 0 $\overline{TX}$/GR - Text/Graphics Mode
0 = Selects text attribute control mode.
1 = Selects graphics control mode.

Bit 1 MONO ATRB - Monochrome Attributes
0 = Selects color display text attributes.
1 = Selects monochrome display text attributes.

Bit 2 ENB LGC - Enable Line Graphics
0 = The ninth dot is the same as the background.
1 = Special line graphics character codes enabled.

When this bit is set to 1, it forces the ninth dot of a line graphics character to be identical to the eighth dot of the character. The line graphics character codes are C0H through DFH. For other characters, the ninth dot is the same as the background.

Bit 3 ENB BLNK - Enable Blinking
0 = Selects the background intensity for the text attribute input.
1 = Selects blink attribute in text modes.

This bit must also be set to 1 for blinking graphics modes. The blinking counter is operated by the vertical retrace counter (VRTC) input. It divides the VRTC input by 32. The blinking rates are ON for 16 VRTC clocks and OFF for 16 VRTC clocks. In the graphics mode, when blink is activated, the most significant color bit (bit 3) for each dot is inverted alternately, thus allowing two different colors to be displayed for 16 VRTC clocks each.

When the cursor is displayed in the text mode, it is blinked at a rate of ON for 8 VRTC clocks and OFF for 8 VRTC clocks (period by 16 frames). The displayed characters are independently blinked at the rate of 32 frames as above.

Bit 4 Reserved = 0

Bit 5 TOP PAN - Top Panning Enable
0 = Line compare has no effect on the output of the pixel panning register.
1 = Forces the output of the pixel panning register to 0 after matching line compare until VSYNC occurs in the CRT controller. At the top of screen the output of the Pixel Panning register returns to its programmed value. This bit allows a top portion of a split screen to be panned.

Bit 6 256 CLR - 256 Color Mode
0 = 4 bits of video (translated to 6 bits by the palette) are output every internal dot-clock cycle.
1 = Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot-clock.

Bit 7 SEL V54 - Select V[5:4]
0 = Bits 5 and 4 of the video output are generated by internal palette registers.
1 = Bits 5 and 4 of video output are replaced by the Pixel Padding register (bits 1 and 0 of AR14).

Border Color Register (BDR_CLR) (AR11)

Read/Write Address: 3C1H/3C0H, Index 11H
Power-On Default: 00H

7	6	5	4	3	2	1	0
BORDER COLOR							

Bits 7–0 Border Color. This 8-bit register determines the border color displayed on the CRT screen. The border is an area around the screen display area.

Color Plane Enable Register (DISP_PLN) (AR12)

Read/Write Address: 3C1H/3C0H, Index 12H
Power-On Default: 00H

This register enables the respective video memory color plane 3–0 and selects video color outputs to be read back in the display status.

7	6	5	4	3	2	1	0
= 0	= 0	VDT-SEL 1	0	DISPLAY PLANE ENBL			

Bits 3–0 DISPLAY PLANE ENBL
A 0 in any of these bits forces the corresponding color plane bit to 0 before accessing the internal palette. A 1 in any of these bits enables the data on the corresponding color plane.

Bits 5–4 VDT-SEL
These bits select two of the eight bit color outputs to be available in the Input Status 1 register. The output color combinations available on the status bits are as follows:

D STS MUX		STS 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	Video 2	Video 0
0	1	Video 5	Video 4
1	0	Video 3	Video 1
1	1	Video 7	Video 6

Bits 7–6 Reserved = 0

Horizontal Pixel Panning Register (H_PX_PAN) (AR13)

Read/Write
Power-On Default: 00H

Address: 3C1H/3C0H, Index 13H

This register specifies the number of pixels to shift the display data horizontally to the left. Pixel panning is available in both text and graphics modes.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	NUMBER OF PAN SHIFT			

Bits 3–0 NUMBER OF PAN SHIFT
This register selects the number of pixels to shift the display data horizontally to the left. In the 9 pixels/character text mode, the output can be shifted a maximum shift of 8 pixels. In the 8 pixels/character text mode and all graphics modes, except 256 color mode, a maximum shift of 7 pixels is possible. In the 256 color mode, bit 0 of this register must be 0 resulting in only 4 panning positions per display byte. The panning is controlled as follows:

	Number of pixels shifted in		
Bits 3–0	**9 pixel/char.**	**8 pixel/char.**	**256 color mode**
0000	1	0	0
0001	2	1	–
0010	3	2	1
0011	4	3	–
0100	5	4	2
0101	6	5	–
0110	7	6	3
0111	8	7	–
1000	0	–	–

Bits 7–4 Reserved = 0

Pixel Padding Register (PX_PADD) (AR14)

Read/Write Address: 3C1H/3C0H, Index 14H
Power-On Default: 00H

This register specifies the high-order bits of video output when pixel padding is enabled and disabled in the 256 color mode.

7	6	5	4	3	2	1	0
				PIXEL PADDING			
= 0	= 0	= 0	= 0	V7	V6	V5	V4

Bits 1–0 PIXEL PADDING V5, V4
These bits are enabled with a logical 1 of bit 7 of AR10, and can be used in place of the V5 and V4 bits from the Palette registers to form the 8-bit digital color value output.

Bits 3–2 PIXEL PADDING V7, V6
In all modes except 256 color mode, these bits are the two high-order bits of the 8-bit digital color value output.

Bits 7–4 Reserved = 0

6.6 SETUP REGISTERS

This section describes the Video Subsystem Setup registers on the system board.

The I/O functions of the system board use POS information during the setup procedure. The I/O controllers on the system board are treated as a single device. Although the VGA is a part of the system board, POS treats it as a separate device. The Setup Enable register is used to place the system board or the Video Subsystem into setup. The Setup Enable register is read/write at I/O address 46E8H. The bit definitions are provided below.

Setup Option Select Register (SETUP_MD)

Read/Write Address: 102H (ISA)
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	= 0	V.S SLP

Bit 0 V.S. SLP - Video Subsystem Sleep Mode
When in setup mode (I/O address 46E8H, bit 4 equals 1 or bit 5 equals 0, depending on the strapping of the PD8 pin) the Video Subsystem responds to a single option select byte at I/O address 0102H and treats this bit as the Video Subsystem sleep bit.
0 = Video Subsystem does not respond to commands, addresses, or data on the data bus. If the Video Subsystem was set up and is generating video output when this bit is set to 0, the output is still generated.
1 = Video Subsystem responds to commands, addresses, or data on the data bus.

The Video Subsystem responds only to address 0102H when in the setup mode. No other addresses are valid at that time. The Video Subsystem ignores address 0102H when in the enabled mode (I/O address 46E8H, bit 4 equals 0 or bit 5 equals 1, depending on the strapping of the PD8 pin), and decodes normal I/O and memory addresses.

Bit 7–1 Reserved = 0

Note: When Video Subsystem is disabled, accesses to the video DAC registers are disabled. When the system is powered on, the power-on-self-test (POST) initializes and enables the Video Subsystem.

Video Subsystem Enable Register (SETUP_MD)

Write Only Address: 46E8H
Power-On Default: 00H

This register is effective for ISA configurations only.

7	6	5	4	3	2	1	0
= 0	= 0	V.S EN2	V.S EN1	V.S A.E	= 0	= 0	= 0

Bits 2–0 Reserved = 0

Bit 3 V.S. A.E - Video Subsystem Address Decoding
0 = Video I/O and memory address decoding disabled.
1 = The video I/O and memory address decoders are enabled.

Bit 4 V.S EN1 - Enable Video Subsystem 1
0 = The Video Subsystem is in operational mode.
1 = The Video Subsystem is placed in the setup mode. Bit 5 of this register is don't care.

Bit 5 V.S EN2 - Enable Video Subsystem 2
0 = Video Subsystem responds to commands, addresses and data on the data bus.
1 = If bit 4 of this register is a logical 0, the Video Subsystem is placed in the setup mode. If the ISA bus is selected and bit 8 of the Reset State Read register (Setup Sel) is turned off (= 0 through power-on strapping), this bit becomes effective and bit 4 of this register is disabled.

Bits 7–6 Reserved = 0

6.7 VIDEO DAC REGISTERS

Of all the video DAC registers described in this section, only the DAC Status Register (3C7H, Read Only) is physically located inside the 86C928. The others are located in the video DAC. The 86C928 decodes these addresses for video DAC data byte steering.

DAC Mask Register (DAC_AD_MK)

Read/Write Address: 3C6H
Power-On Default: Undefined

This register is the pixel read mask register to pixel select video output. The CPU can access this register at any time.

7	6	5	4	3	2	1	0
DAC ADDRESS MASK							

Bits 7–0 DAC ADDRESS MASK
The contents of this register are bit-wise logically ANDed with the pixel select video output (V7–V0). This register is initialized to FFH by BIOS during a video mode set.

DAC Read Index Register (DAC_RD_AD)

Write Only Address: 3C7H
Power-On Default: Undefined

This register contains the pointer to one of 256 palette data registers and is used when reading the color palette.

7	6	5	4	3	2	1	0
DAC READ ADDRESS							

Bits 7–0 DAC READ ADDRESS
Each time the color code is written to this register, it identifies that a read sequence will occur. A read sequence consists of three successive byte reads from the video DAC data register at I/O address 3C9H. The least significant 6 bits of each byte taken from the video DAC data register contain the corresponding color value, and the most significant 2 bits contain zeros. The order is red byte first, then green, and finally blue. The sequence of events for a read cycle is:

1. Write the color code to this register (Video DAC Read Index) at address 3C7H.
2. The contents of the location in the color look-up table pointed to by the color code are transferred to the video DAC data register at address 3C9H.
3. Three bytes are read back from the video DAC data register.
4. The contents of this register auto-increment by one.
5. Go to step 2.

If this register is written to during either a read or write cycle, a mode is initialized and the unfinished cycle is aborted. The effects of writing to the video DAC data register during a read cycle or reading from the video DAC data register during a write cycle are undefined and may change the look-up table contents.

DAC Status Register (DAC_STS)

Read Only Address: 3C7H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	DAC-STS	

Bits 1–0 DAC-STS - Video DAC Cycle Status
The last executing cycle was:
00 = Write Palette cycle
11 = Read Palette cycle

Reads from the Video DAC Write Index at address 3C8H or the DAC status register at address 3C7H do not interfere with read or write cycles and may take place at any time.

Bits 7–2 Reserved = 0

DAC Write Index Register (DAC_WR_AD)

Read/Write Address: 3C8H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
DAC WRITE ADDRESS/GIP READ DATA							

Bits 7–0 DAC WRITE ADDRESS/GIP READ DATA
This register contains the pointer to one of 256 palette data registers and is used during a palette load. Each time the color code is written to this register, it identifies that a write sequence will occur. A write sequence consists of three successive byte writes to the DAC data register at I/O address 3C9H. The least significant 6 bits of each byte are concatenated to form the value placed in the 18-bit data register. The order is red byte first, then green, and finally blue. Once the third byte has been written, the value in the data register is written to the location pointed to by the color code. The sequence of events for a write cycle is:

1. Write the color code to this register (DAC Write Index) at address 3C8H.
2. Three bytes are written to the DAC Data register at address 3C9H.
3. The contents of the DAC data register are transferred to the location in the color look-up table pointed to by the color code.
4. The DAC Write Index register auto-increments by 1.
5. Go to step 2.

If bit 2 of the Extended Video DAC Control register (3?5H, Index 55H) is set to 1 to enable the General I/O Port read function, a read of 3C8H retrieves data from an external input buffer.

Video DAC Data Register (DAC_DATA)

Read/Write Address: 3C9H
Power-On Default: Undefined

This register is a data port to read or write the contents of the location in the color look-up table pointed to by the DAC Read Index or the DAC Write Index registers.

7	6	5	4	3	2	1	0
DAC READ/WRITE DATA							

Bits 7–0 DAC READ/WRITE DATA
To prevent "snow flicker" on the screen, an application reading data from or writing data to the DAC Data register should ensure that the BLANK input to the video DAC is asserted. This can be accomplished either by restricting data transfers to retrace intervals, checking the Input Status 1 register to determine when retrace is occurring, or by using the screen-off bit in the Clocking Mode register of the sequencer.

Section 7: S3 VGA Register Descriptions

The 86C928 has additional registers to extend the functions of basic VGA. These registers are located in CRT Controller address space at locations not used by IBM. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 1 register (CR38) must be loaded with a binary unlock key pattern (see the register description). The registers will remain unlocked until the key pattern is reset by altering a significant bit.

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write =0, read = U). See Appendix A for a table listing each register in this section and its page number.

Chip ID/REV Register (CHIP-ID/REV) (CR30)

Read Only
Power-On Default: 90H

Address: 3?5H, Index 30H

7	6	5	4	3	2	1	0
CHIP ID				REVISION STATUS			

Bits 7–0 CHIP ID AND REVISION STATUS

Memory Configuration Register (MEM_CNFG) (CR31)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 31H

7	6	5	4	3	2	1	0
EXT BIOS	HST DFF	STRT-ADR 17	16	ENH MAP	VGA 16B	SCRN 2.PG	CPUA BASE

Bit 0 CPUA BASE - Enable Base Address Offset
0 = Address offset bits 3-0 of the CRT Register Lock register and bit 2 of the Extended System Control 2 register are disabled.
1 = Address offset bits 3-0 of the CRT Register Lock register and bit 2 of the Extended System Control 2 register are enabled for whole VGA display memory access by the CPU.

Bit 1 SCRN 2.PG - Two-Page Screen Image
0 = Normal Mode
1 = Enable 2K x 1K x 4 map image screen for 1024 × 768 or 800 x 600 screen resolution, or 2K x 512 x 8 map image screen for 640 x 480 screen resolution.

Bit 2 VGA 16B - VGA 16-bit Memory Bus Width
0 = 8-bit memory bus operation
1 = Enable 16-bit bus VGA memory read/writes

Bit 3 ENH MAP - Enhanced Memory Mapping
0 = Forces IBM VGA mapping for memory accesses.
1 = Forces Enhanced Mode mappings.

Bits 5–4 STRT-ADR 17, 16 - Start Address Bits 17-16
Bits 17-16 of start address, cursor location, and font access address registers

Note: Bit 2 of the Extended System Control 2 register (CR51) is bit 18 of the address and enables access to up to 2 MBytes of display memory.

Bit 6 HST DFF - High Speed Text Display Font Fetch Mode
0 = Normal Font Access Mode
1 = Enable Page Mode for Alpha Mode Font Access

Bit 7 EXT BIOS - External BIOS ROM Space (C6000H-C67FFH) Mapping
0 = External BIOS ROM space is not readable (default).
1 = External BIOS ROM space is readable.

Note: If power-on strapping bit PD3 = 1, the setting of this bit has no effect and all 32 KBytes of BIOS ROM are available.

Backward Compatibility 1 Register (BKWD_1) (CR32)

Read/Write Address: 3?5H, Index 32H
Power-On Default: 00H

7	6	5	4	3	2	1	0
SRO-TRI	VGA FXPG	EGA (R)	EGA (R)	BKWD MODE	FCHI CHCK	CH-CLK 1	0

Bits 1–0 CH-CLK - Character Clock Period
00 = Same as IBM VGA (8 or 9 dot clocks)
01 = 7 dots (used for 132 character mode)
10 = 9 dots
11 = Reserved

Bit 2 FCHI CHCK - Force Character Clock High
0 = Normal character clock
1 = Force character clock of horizontal timing to high rate (not 1/2 dot clock rate) for CGA and HGC emulations.

Bit 3 BKWD MODE - Backward Compatibility Modes
0 = VGA
1 = All other backward compatibility modes

Bits 5–4 Reserved

Bit 6 VGA FXPG - IBM VGA Memory Mapping
0 = Standard VGA screen page
1 = Fix VGA Screen Page with IBM VGA Memory Mapping using bits STA17-16 (bits 5-4 of the Memory Configuration register) and bit 0 of the Extended System Control 2 register as bit 18.

Bit 7 SRO-TRI Serial Out Tri-State
0 = Serial Out Tri-State disabled
1 = SC, SOE0 and SXNR pins are tri-stated

Backward Compatibility 2 Register (BKWD_2) (CR33)

Read/Write Address: 3?5H, Index 33H
Power-On Default: 00H

7	6	5	4	3	2	1	0
DISA FLKR	LOCK PLTW	BDR SEL	LOCK DACW	VDK= -DCK	R	DIS VDE	R

Bit 0 Reserved

Bit 1 DIS VDE - Disable VDE Protection
0 = VDE protection enabled
1 = Disables the write protect setting of the Vertical Retrace End register bit 7 on CRTC Overflow bits 6,1.

Bit 2 Reserved

Bit 3 VCLK = -DCLK.
0 = VCLK is inverted DCLK or DCLK/2
1 = VCLK is inverted DCLK only

Bit 4 LOCK DACW - Lock Video DAC Writes
1 = Disable writes to video DAC registers
0 = Enable writes to video DAC registers

Bit 5 BDR SEL - Blank/Border Select
0 = Blank comes earlier than display enable by including border area
1 = Blank signal will be same as active display enable timing

Bit 6 LOCK PLTW - Lock Palette/Overscan Registers
0 = Unlock Palette/Overscan registers
1 = Lock Palette/Overscan registers

Bit 7 DISA FLKR - Remove Flicker
0 = No effect
1 = Overrides the CGA Mode Control register video enable (bit 3). This eliminates flicker (CGA snow).

Backward Compatibility 3 Register (BKWD_3) (CR34)

Read/Write Address: 3?5H, Index 34H
Power-On Default: 00H

7	6	5	4	3	2	1	0
LOCK CKSL	R	LOCK 8/9D	ENB DTPC	R	R	R	R

Bits 3–0 Reserved.
These bits are set by VGA BIOS or the mode setup utility program.

Bit 4 ENB DTPC - Enable Data Transfer Position Control
Enables timing adjustment of the Data Transfer.
0 = Horizontal Total Position (CR0) register active
1 = Data Transfer Execute Position register (CR3B) active

Bit 5 LOCK 8/9D - Lock 8/9 Dots
0 = Bit 0 of the Clocking Mode register is unlocked.
1 = Bit 0 of the Clocking Mode register is locked.

When emulating EGA hardware, horizontal timing registers are programmed for an 8 dot character clock period (via bit 0 of the Clocking Mode register) and these registers are locked. Locking 8/9 dots prevents EGA software from modifying this bit.

Bit 6 Reserved

Bit 7 LOCK CKSL - Lock Clock Select
0 = Bits 3-2 of the Miscellaneous Output register (3C2H) are unlocked.
1 = Bits 3-2 of the Miscellaneous Output register (3C2H) are unlocked, This will force the video clock to a locked frequency by locking clock select to a fixed value.

CRT Register Lock Register (CRTR_LOCK) (CR35)

Read/Write Address: 3?5H, Index 35H
Power-On Default: 00H

7	6	5	4	3	2	1	0
		LOCK	LOCK	CPU-BASE-ADDRESS			
R	R	HTMG	VTMG	17	16	15	14

Bits 3–0 CPU-BASE-ADDRESS
CPU Base Address bits 17-14. These four bits define the CPU address base in 64 KByte units of display memory. These bits are added with CPU address bit 17 (MSB of video memory addressing) to bit 14 for display buffer accesses.

Note: Bit 2 of the Extended System Control 2 register (CR51) is bit 18 of the address and enables access to up to 2 MBytes of display memory.

Bit 4 LOCK VTMG - Lock Vertical Timing Registers
0 = Vertical timing registers are unlocked
1 = The following vertical timing registers are locked:

CR06
CR07 (bits 7,5,3,2,0)
CR09 (bit 5)
CR10
CR11 (bits 3-0)
CR15
CR16
Note: CR6,CR7 registers are also locked by bit 7 of the Vertical Retrace End register.

Bit 5 LOCK HTMG - Lock Horizontal Timing Registers
0 = Horizontal timing registers are unlocked
1 = The following horizontal timing registers are locked:

CR00
CR01
CR02
CR03
CR04
CR05
CR17 (bit 2)
Note: All these registers (except CR17(bit 2)) are also locked by bit 7 of the Vertical Retrace End register.

Bit 7-6 Reserved

Configuration1, 2 Registers (CONFG_REG1, CNFG_REG2) (CR36, 37)

Read Only Address: 3?5H, Indices 36H, 37H
Power-On Default: Depends on Strapping

These registers sample the reset state from PD bus pins [15:0].

Bits	Value	Function
System Bus Select		
1,0	00	EISA
	01	386DX/486 local bus
	11	ISA
VGA ROM Data Bus Width (ISA)		
2	0	16 bits
	1	8 bits
VGA BIOS ROM Enable (ISA)		
3	0	All accesses between C0000H-C7FFFH enabled except for accesses between C6000H-C67FFH, which are disabled
	1	All accesses between C0000H-C7FFFH enabled
Address Bit Range for MEMCS16 Decode (ISA) or SAUP2/ROMCS Select (Local Bus)		
4	0	LA[23:17], SA16 (ISA Bus) SAUP2 pin become ROMCS (Local Bus)
	1	LA[23:17] (ISA Bus) SAUP2 pin unchanged (Local Bus)
Display Memory Size (ISA, EISA, Local Bus)		
7-5	000	4 MBytes
	010	3 MBytes
	100	2 MBytes
	110	1 MByte
	111	0.5 MByte
VGA Subsystem Setup Select (ISA) or 86C805 Enable (Local Bus)		
8	0	Setup Bit is Bit 5 of the Video Subsystem Access/Setup register (46E8H) (ISA Bus) Disable 86C928 and use ISA/EISA adapter (Local Bus)
	1	Setup Bit is Bit 4 of the Video Subsystem Access/Setup register (46E8H) (ISA Bus) Enable 86C928. (Local Bus)
Reserved Bit (ISA, EISA, Local Bus)		
9		Always 1
Extended Monitor Identification (ISA, EISA, Local Bus)		
10	0 or 1	Extension of bits 15-13. See the ROM BIOS documentation.

Bits	Value	Function
No Wait State (ISA) or Local Bus Cycle Indicator		
11	0	NOWS disabled (ISA Bus) LOCA is a level signal (Local Bus)
11	1	NOWS enabled (ISA Bus) LOCA is a tri-state signal (Local Bus)
MEMCS16 Select (ISA) or LOCA for video DAC (Local Bus)		
12	0	MEMCS16 generated externally (ISA Bus) Disable LOCA and SRDY for video DAC accesses (Local Bus)
	1	86C928 generates MEMCS16 (ISA) Normal LOCA and SRDY for video DAC accesses (Local Bus)
Monitor Type Identification (ISA, EISA, Local Bus)		
15-13		See the ROM BIOS documentation.

Register Lock 1 Register (REG_LOCK1) (CR38)

Read/Write Address: 3?5H, Index 38
Power-On Default: 00H

Loading 01xx10xx into this register unlocks the S3 register set for read/writes. (x = don't care)

7	6	5	4	3	2	1	0
= 0	= 1			= 1	= 0		

Register Lock 2 Register (REG_LOCK2) (CR39)

Read/Write Address: 3?5H, Index 39
Power-On Default: 00H

Loading 101xxxxx unlocks the system control and system extension registers for reading/writing. (x = don't care)

7	6	5	4	3	2	1	0
= 1	= 0	= 1					

Miscellaneous 1 Register (MISC_1) (CR3A)

Read/Write
Address: 3B?H, Index 3AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
ENB M16	R	HST DFW	ENH 256	TOP MEM	ENB RFC	REF-CNT 1	REF-CNT 0

Bits 1–0 REF-CNT - Alternate Refresh Count Control
00 = Refresh Count 0
01 = Refresh Count 1
10 = Refresh Count 2
11 = Refresh Count 3

Bit 2 ENB RFC - Enable Alternate Refresh Count Control
0 = Alternate refresh count control (bits 1-0) is disabled
1 = Alternate refresh count control (bits 1-0) is enabled

Bit 3 TOP MEM - Top of Memory Access
0 = Top of memory access disabled
1 = CPU and CRTC accesses are forced into the top 32 or 64 KByte of video memory.

Bit 4 ENH 256 - 256 Color Enhanced Mode
0 = Attribute controller shift registers configured for 4-bit modes.
1 = Attribute controller shift register configured for 8-, 16- and 24-bit color enhanced modes.

Bit 5 HST DFW - High Speed Text Font Writing
0 = Disable high speed text font writing
1 = Enable high speed text font writing

Bit 6 Reserved = 0

Bit 7 ENB M16 - Enable $\overline{\text{MEMCS16}}$ Signal
0 = 8-bit system bus width (default)
1 = 16-bit system bus width

Data Transfer Execute Position Register (DT_EX_POS) (CR3B)

Read/Write Address: 3?5H, Index 3BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
DATA TRANSFER EXECUTE POSITION							

Bits 7–0 DATA TRANSFER EXECUTE POSITION. If bit 4 of the Backward Compatibility 3 register (3?5H, Index 34H) is set to 1, these bits specify the horizontal character position of data transfer execution for a VRAM configuration. The recommended value is halfway between the horizontal total (H_TOTAL, CR0) and the start horizontal sync position (S_H_SY_P, CR4).

Interlace Retrace Start Register (IL_RTSTART) (CR3C)

Read/Write Address: 3B?H, Index 3CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
INTERLACE RETRACE START POSITION							

Bits 7–0 INTERLACE RETRACE START POSITION
Specifies the value of the offset in terms of character clocks for Interlaced mode start/end in even/odd frames.

Section 8: System Control Register Descriptions

System Control registers are configuration registers, mode control registers, and hardware graphics cursor control registers. They are positioned in the same indexed register space as VGA S3 registers. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 2 register (CR39) must be loaded with a binary unlock key pattern (see the register description). The registers will remain unlocked until the key pattern is reset by changing a significant bit.

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). See Appendix A for a table listing each of the registers in this section and its page number.

System Configuration Register (SYS_CNFG) (CR40)

Read/Write Address: 3?5H, Index 40H
Power-On Default: A4H

7	6	5	4	3	2	1	0
RD-WAIT		DEC-WAIT		EWRT	WST	SIG	EN-A
1	0	1	0	POST	CTL	SEL	8514

Bit 0 EN-A 8514 - Enable Enhanced Register Access
0 = Enhanced register access disabled
1 = Enhanced register access enabled

Bit 1 SIG SEL - Signal Select
0 = MID0, MID1 signals active.
1 = MID0 signal becomes STRD if bit 2 of CR55 = 1. MID0 becomes $\overline{\text{BGNT}}$ and MID1 becomes $\overline{\text{BREQ}}$ if bit 2 of CR55 is 0.

Bit 2 WST CTL - Wait State Control
0 = No Wait State
1 = One Wait State (Default)

Bit 3 EWRT POST- Enable Fast Write Buffer (Write Posting Into FIFO)
0 = Disable fast write buffer (Default)
1 = Enable fast write buffer

Bits 5–4 DEC-WAIT - Decode Wait Control (386/486 Local Bus Only)
00 = 0 wait states
01 = 1 wait state
10 = 3 wait states (Default)
11 = 2 wait states

Bits 7–6 RD-WAIT - Read Wait Control
386/486 Local Bus Only
00 = 0 wait states
01 = 1 wait state
10 = 3 wait states (Default)
11 = 2 wait states

ISA Bus Only
00 = Enable $\overline{\text{NOWS}}$ signal
01 = Disable $\overline{\text{NOWS}}$ signal
10 = Disable $\overline{\text{NOWS}}$ signal (Default)
11 = Disable $\overline{\text{NOWS}}$ signal

BIOS Flag Register (BIOS_FLAG) (CR41)

Read/Write Address: 3?5H, Index 41H
Power-On Default: 00H

7	6	5	4	3	2	1	0
BIOS-FLAG-REGISTER-1							

Bits 7–0 BIOS-FLAG-REGISTER-1
Used by the BIOS. Users should not write to this register.

Mode Control Register (MODE_CTL) (CR42)

Read/Write Address: 3?5H, Index 42H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	INTL MODE	R	DOT-CLOCK-SELECT			

Bits 3–0 DOT-CLOCK-SELECT
These bits are set by the VGA BIOS or the mode setup utility program depending on the operational mode and monitor select/ID information in the Configuration Register 2 register, bits 14-12. These bits are effective when the VGA clock selects "11" in the Miscellaneous Output register and are strobed to the clock chip by the STWR signal.

[3:0] (HEX)	Freq (MHz)	Mode
0	25.175	VGA0
1	28.322	VGA1
2	40.000	VESA 800x600 @60Hz
3		Reserved
4	50.000	VESA 800x600 @72Hz, 640x480x16bpp @ 60 Hz
5	77.000	1024x768 @72Hz
6	36.000	VESA 800x600 @56Hz
7	44.889	1024x768 @43Hz - Interlaced
8		Reserved
9		Reserved
A	80.000	1280x1024 @46Hz -Interlaced
B	31.500	VESA 640x480 @72Hz
C	110.000	1280x1024 @60Hz
D	65.000	1024x768 @60Hz
E	75.000	1024x768 @70Hz, 640x480x24bpp @ 60 Hz
F		Reserved

Note: This table is an example, as the frequencies are dependent upon the clock synthesizer capabilites.See the *S3-Compatible Clock Generators* tech note.

Bit 4 Reserved

Bit 5 INTL MODE - Interlaced Mode
0 = Noninterlaced
1 = Interlaced

Bits 7–6 Reserved

Extended Mode Register (EXT_MODE) (CR43)

Read/Write Address: 3?5H, Index 43H
Power-On Default: 00H

7	6	5	4	3	2	1	0
HCTR X2	R	R	XEN	64K CLR	OLD LSW8	OLD RS2	DCK EDG

Bit 0 DCK EDG - Video Clock Edge Mode Select
0 = Normal (Rising Edge Only)
1 = Both Edges (Rising and Falling)

Bit 1 OLD RS2 - DAC Register Select Bit 2
This is an extension bit of RS[1:0] for video DAC addressing. This is disabled if bits 3-2 of the Extended Video DAC Control register (CR55) are not 0,0.

Bit 2 OLD LSW8 - Logical Screen Width Bit 8
This is an extension of the Offset (Screen Width) register (CR13). This is disabled if bits 5-4 of the Extended System Control 2 (CR51) are not 0,0.

Bit 3 64K CLR - 16-bit Color Mode
0 = Disable 16-bit color mode
1 = Enable 16-bit color mode

Bit 4 XEN - Translate Enable
0 = Use I/O port address X2E8H
1 = Enable I/O port at address X2E8H XOR 3A0H (X148H)

Bits 6–5 Reserved

Bit 7 HCTR X2 - Horizontal Counter Double Mode
0 = Disable horizontal counter double mode
1 = Enable horizontal counter double mode (horizontal CRT parameters are doubled)

Hardware Graphics Cursor Mode Register (HGC_MODE) (CR45)

Read/Write Address: 3?5H, Index 45H
Power-On Default: 00H

7	6	5	4	3	2	1	0
		ENB	HWGC	HWC-HSTR			HWGC
R	R	485	1280	X3W	X2W	R	ENB

Bit 0 HWGC ENB - Hardware Graphics Cursor Enable
0 = Hardware graphics cursor disabled in any mode
1 = Hardware graphics cursor enabled in Enhanced mode

Bit 1 Reserved

Bit 2 HWC-HSTR X2W - Hardware Cursor Horizontal Stretch 2
0 = Function disabled
1 = Stretch to twice width and use the Hardware Graphics Cursor Foreground and Background Stack registers (CR4A, CR4B), stack pointer 0-1.

Bit 3 HWC-HSTR X3W - Hardware Cursor Horizontal Stretch 3
0 = Function disabled
1 = Stretch to triple width and use the Hardware Graphics Cursor Foreground and Background Stack registers (CR4A, CR4B), stack pointer 0-2

Bit 4 HWGC 1280 - Hardware Cursor Right Storage
0 = Function disabled
1 = If 4 bits/pixel, 4 blocks of last 256 bytes in each 1 KByte line of HCS-STADR (size aligned; two LSBs must be 1,1) become the hardware graphics cursor storage area. If 8 bits/pixel, 2 blocks of last 512 bytes in each 2-KByte line of Hardware Graphics Cursor Start Address register (size aligned; two LSBs must be 1,1) become the hardware graphics cursor storage area.

Bit 5 ENB 485 - Cursor Control Enable for Brooktree Bt485 DAC
0 = HC[1:0] are unchanged
1 = HC1 becomes the ODF signal and HC0 becomes the CDE signal.

Note: This bit is effective only if bit 5 of the Extended Video DAC Control register (3?5H, Index 55) is set to 1.

Bits 7–6 Reserved

Hardware Graphics Cursor Origin-X Registers (HWGC_ ORGX(H)(L)) (CR46, CR47)

Read/Write Address: 3?5H, Index 46H, 47H
Power-On Default: 0000H

The high level three bits are written into CR46 and the low level byte is written into CR47.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	HWGC ORG X (H)			HWGC ORG X (L)							

Bits 10–0 HWGC ORG X(H) (L) - X-Coordinate of Cursor Left Side

Bits 15–11 Reserved

Hardware Graphics Cursor Origin-Y Registers (HWGC_ORGY(H)(L)) (CR48, CR49)

Read/Write Address: 3?5H, Index 48H, 49H
Power-On Default: Undefined

The high level three bits are written into CR48 and the low level byte is written into CR49.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	HWGC ORG Y (H)			HWGC ORG Y (L)							

Bits 10–0 HWGC ORG Y (H)(L) - Y-Coordinate of Cursor Upper Line
The cursor X, Y position is registered upon writing HWGC ORG Y (H).

Bits 15–11 Reserved

Hardware Graphics Cursor Foreground Stack Register (HWGC_FGSTK) (CR4A)

Read/Write Address: 3?5H, Index 4AH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TRUE COLOR FOREGROUND STACK (0-2)							

Bits 7–0 TRUE COLOR FOREGROUND STACK (0-2)

Three foreground color registers are stacked at this address. The stack pointer (common with CR4B) is reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). Each write to this register (CR4A) increments the stack pointer by 1, so three writes provide 24 bits of true color information. These registers are used when the hardware cursor horizontal stretch mode is turned on via either bit 2 or bit 3 of CR45.

Hardware Graphics Cursor Background Stack Register (HWGC_BGSTK) (CR4B)

Read/Write Address: 3?5H, Index 4BH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TRUE COLOR BACKGROUND STACK (0-2)							

Bits 7–0 TRUE COLOR BACKGROUND STACK (0-2)

Three background color registers are stacked at this address. The stack pointer (common with CR4A) is reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). Each write to this register (CR4B) increments the stack pointer by 1, so three writes provide 24 bits of true color information. These registers are used when the hardware cursor horizontal stretch mode is turned on via either bit 2 or bit 3 of CR45.

Hardware Graphics Cursor Storage Start Address Registers (HWGC_STA(H)(L) (CR4C, CR4D)

Read/Write Address: 3?5H, Index 4CH, 4DH
Power-On Default: Undefined

The high level four bits are written into CR4C and the low level byte is written into CR4D.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	HWGC STA(H)				HWGC STA(L)							

Bits 11–0 HWGC STA(H)(L) - Hardware Graphics Cursor Storage Start Address

Bits 15–12 Reserved

Hardware Graphics Cursor Pattern Display Start X-PXL-Position Register (HWGC_DX) (CR4E)

Read/Write Address: 3?5H, Index 4EH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HWGC PAT DISP START X-POS					

Bits 5–0 HWGC PAT DISP START X-POS - HWGC Pattern Display Start-X Pixel Position

Bits 7–6 Reserved

Hardware Graphics Cursor Pattern Disp Start Y-PXL-Position Register (HGC_DY) (CR4F)

Read/Write Address: 3?5H, Index 4FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HWGC PAT DISP START Y-POS					

Bits 5–0 HWGC PAT DISP START Y-POS - HWGC Pattern Display Start-Y Pixel Position

Bits 7–6 Reserved

Section 9: System Extension Register Descriptions

These registers provide extended system and memory control, external sync control and addressing window control. They are enabled in the same way as the System Control registers via the Register Lock 2 register (CR39).

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). See Appendix A for a table listing each of the registers in this section and its page number.

Extended System Cont 1 Register (EX_SCTL_1) (CR50)

Read/Write Address: 3?5H, Index 50H
Power-On Default: 00H

7	6	5	4	3	2	1	0
GE-SCR-W		PXL-LNGH		-LOCA	ENB		
1	0	1	0	-SRDY	BREQ	R	R

Bits 1–0 Reserved

Bit 2 ENB BREQ - Enable BREQ Function
0 = BREQ, BGNT functions disabled
1 = BREQ, BGNT functions enabled

Bit 3 DISABLE LOCA/SRDY - Disable LOCA/SRDY
0 = LOCA/SRDY signals enabled (Default)
1 = LOCA/SRDY signals disabled

Setting this bit to 1 disables the LOCA/SRDY signals on the 386/486 local bus for writing to the video DAC. This has the same effect as bit 12 of Configuration Register 2 (CR37).

Bits 5–4 PXL-LNGH - Pixel Length Select
These bits select the pixel length for Enhance Mode command execution through the Graphics Engine.
00 = 1 byte (Default). This corresponds to a pixel length status of 4 or 8 bits/pixel in bit 7 of the Subsystem Status register (42E8H).
01 = 2 bytes. 16 bits/pixel
10 = Reserved
11 = 4 bytes. 32 bits/pixel

Bits 7–6 GE-SCR-W - Graphics Engine Command Screen Pixel Width
00 = 1024/2048 (Default)
01 = 640
10 = 800
11 = 1280

Extended System Control 2 Register (EX_SCTL_2) (CR51)

Read/Write Address: 3?5H, Index 51H
Power-On Default: 00H

7	6	5	4	3	2	1	0
ENB ERW	DIS SPXF	LOG-SCR-W 9	8	CPU-BASE 19	18	DISP-ST-AD 19	18

Bits 1–0 DISP-ST-AD - Display Start Address Bits 19-18
These are extension bits of Memory Configuration register (CR31) bits 5-4 (Display Start Base Address).

Bits 3–2 CPU-BASE - CPU Base Address Bits 19-18
These are extension bits of CRT Register Lock register (CR35) bits 3-0 (CPU Base Address). They becomes bits 19-18 of the CPU base address, enabling access to up to 4 MBytes of display memory.

Bits 5–4 LOG-SCR-W - Logical Screen Width Bit [9:8]
These are two extension bits of the Offset register (CR13). If the value of these bits is not zero, bit 2 of the Extended Mode register (CR43) is disabled.

Bit 6 DIS SPXF - Disable Split Transfer
0 = Split transfers enabled
1 = Split transfers disabled

Bit 7 ENB ERW - Enable EPROM Write
0 = Disable flash memory write control to the BIOS ROM address
1 = Enable flash memory write control to the BIOS ROM address

Extended BIOS Flag 1 Register (EXT_BBFLG1) (CR52)

Read/Write Address: 3?5H, Index 52H
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-1							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-1
Used by the BIOS. Users should not write to this register.

Extended Memory Control 1 Register (EX_MCTL_1) (CR53)

Read/Write Address: 3?5H, Index 53H
Power-On Default: 00H

7	6	5	4	3	2	1	0
ENB NBLW	SWP NBL	PAR VRAM	ENB MMIO	ENBL-WRITE-PER-BIT MB3	MB2	MB1	MB0

Bits 3–0 ENBL-WRITE-PER-BIT MB3, MB2, MB1, MB0
Enable Write Per Bit Flags for each 1MB memory bank

Bit 4 ENB MMIO - Enable MMIO Access
The first 32-KByte MMIO area (A0000H-A7FFFH) is used for image transfers via E2E8H and E2EAH. The second 32-KByte MMIO area (A8000H-AFFFFH) is used for the enhanced command registers (from 82E8H to BEE8H).
0 = Disable (Default)
1 = Enable

Bit 5 PAR VRAM - Parallel VRAM Addressing
0 = Serial VRAM addessing mode
1 = Parallel VRAM addressing mode

Bit 6 SWP NBL
0 = No nibble swap
1 = Swap nibbles in each byte of a linear memory address read or write operation

Bit 7 ENB NBLW - Enable Nibble Write Control
0 = Disable nibble write control for the Graphics Engine
1 = Enable nibble write control for the Graphics Engine

If nibble write is to be enabled, this bit is set by software after memory testing.

Extended Memory Control 2 Register (EX_MCTL_2) (CR54)

Read/Write Address: 3?5H, Index 54H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R					RAC-EXT-PFTCH 2	1	0

Bits 2–0 RAC-EXT-PFTCH - Read Ahead-Cache Extra Prefetch Control
This specifies the extra pre-fetch number for read ahead-cache control. Only 1, 3 and 7 are meaningful values so that all pre-fetched data lies on a full address boundary. The programmed value specifies the number of doublewords to pre-fetch in linear addressing and VGA doubleword modes. The value is the number of words to pre-fetch in VGA word modes and the number of bytes to pre-fetch in VGA byte modes. A value of 0 causes no data to be pre-fetched, but a read-ahead cache overhead penalty is incurred. Disabling the read-ahead cache via bit 2 of the Linear Address Window Control (3?5H, Index 58H) is the preferable to setting a value of 0. Settings to values other than 1, 3 or 7 are automatically converted to the next lowest meaning value, e.g., a value of 4 is treated as a 3.

Bits 7–3 Reserved

Extended Video DAC Control Register (EX_DAC_CT) (CR55)

Read/Write Address: 3?5H, Index 55H
Power-On Default: 00H

7	6	5	4	3	2	1	0
DIS PAO	R	HWGC EXOP	$\overline{MS}$ /X11	ENB SID	ENB GIR	DAC-R-SEL 3	2

Bits 1–0 DAC-R-SEL - DAC Register Select Bits 3-2
These are two extension bits of the RS[1:0] signals for video DAC addressing. If the value of these bits is not zero, bit 1 of the Extended Mode register (CR43) is disabled.

Bit 2 ENB GIR - Enable General Input Port Read
0 = Video DAC reads enabled
1 = Video DAC reads disabled. $\overline{STRD}$ strobe for reading the General Input Port data is enabled for reading during the time $\overline{DACRD}$ is active.

Bit 3 ENB SID - Enable External SID Operation
0 = Disable external SID operation
1 = Enable external SID operation

Bit 4 $\overline{\text{MS}}$/X11 - Hardware Cursor MS/X11 Mode
This bit determines the functionality of the Cursor Display Control.
0 = MS-Windows mode (Default)
1 = X11-Windows mode

Bit 5 HWGC EXOP - Hardware Cursor External Operation Mode
0 = External hardware cursor mode disabled (normal)
1 = External hardware cursor mode enabled. The two bits of hardware graphics cursor data are output through the HC[1:0] pins for the video DAC, which uses this data to control the cursor. The SENS pin becomes HC1 and the MID2 pin becomes HC0.

Bit 6 Reserved

Bit 7 DIS PAO - Disable PA Output
0 = PA output enabled (normal)
1 = PA [7:0] and VCLK become tri-state off outputs

External Sync Control 1 Register (EX_SYNC_1) (CR56)

Read/Write Address: 3?5H, Index 56H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	DIS SYNC	PRST ODDF	ESYN -R/V	ENB PAL	ENB NTSC	RMT ON

Bit 0 RMT ON - Remote Mode Operation
0 = Remote Mode operation off
1 = Remote Mode operation on. The VSYNC pin becomes the input for GEN-LOCK operation.

Bit 1 ENB NTSC - NTSC Mode
This bit selects the H-counter special count mode.
0 = Normal H-COUNT (Default)
1 = NTSC H-COUNT = (113x8+6)xDCLK, HT(CR0)=113-4

Bit 2 ENB PAL - PAL Mode
This bit selects the H-counter special count mode.
0 = Normal H-COUNT (Default)
1 = PAL H-COUNT = (141x8+7)xDCLK, HT(CR0)=141-4

Bit 3 ESYN -R/V - External Sync Mode Select
0 = H/V reset Sync (Default)
1 = V Reset Sync with GEN-LOCK

If bit 0 (Remote Mode) is on, the falling edge of V-sync input signal resets the V (every other frame in the interlaced mode) or H/V counter.

Bit 4 PRST ODDF - Preset Frame Select (-EVEN/ODD)
If bit 3 selects the V Reset Sync with remote mode on, the starting frame after V-counter reset is selected by this bit.
0 = Even Frame (Default)
1 = Odd Frame

Bit 5 DIS SYNC - Disable SYNC Output
0 = Sync output enabled
1 = Sync output disabled. HSYNC, VSYNC, and $\overline{\text{BLANK}}$ become three-state off outputs.

Bits 7–6 Reserved.

External Sync Control 2 Register (EX_SYNC_2) (CR57)

Read/Write Address: 3?5H, Index 57H
Power-On Default: 00H

7	6	5	4	3	2	1	0
HSYN-RESET-ADJUST				VSYN-RESET-ADJUST			
3	2	1	0	3	2	1	0

Bits 3–0 VSYN-RESET-ADJUST
This specifies the vertical delay line number of the V-counter reset from the falling edge of VSYNC. The set value must be not equal zero in Remote mode.

Bits 7–4 HSYN-RESET-ADJUST
This specifies the horizontal delay character number of the H-counter reset from the falling edge of VSYNC after VSYNC Reset Adjust.

Linear Address Window Control Register (LAW_CTL) (CR58)

Read/Write Address: 3?5H, Index 58H
Power-On Default: 00H

7	6	5	4	3	2	1	0
RAS MCLK	SAM 256	LMT WPE	ENB LA	ISA LAD	ENB RAC	LAW-SIZE 1	0

Bits 1–0 LAW-SIZE - Linear Address Window Size
The size must be equal to or smaller than actual the existing memory size.
00 = 64 KBytes (Default)
01 = 1 MBytes
10 = 2 MBytes
11 = 4 MBytes

Bit 2 ENB RAC - Enable Read Ahead-CACHE
0 = Disable Read Ahead-CACHE (Default)
1 = Enable Read Ahead CACHE

Bit 3 ISA LAD - ISA Latch Address
0 = Unlatch Address during every ISA cycle on ISA (Default)
1 = Latch Address during every ISA cycle

Bit 4 ENB LA - Enable Linear Addressing
0 = Disable Linear Addressing (Default)
1 = Enable Linear Addressing

Bit 5 LMT WPE - Limit Entry Depth for Write-Post
0 = Normal Write-Post Entry Control 9 (Default)
1 = Limit Write-Post Entry Depth to avoid ISA bus time-out due to wait cycle limit.

Bit 6 SAM 256 - Serial Access Mode 256 Words Control
0 = SAM control is 512 words
1 = SAM control is 256 words

Bit 7 RAS 6-MCLK
0 = 7 MCLK cycles for the random read/write cycle time (t_{RC})
1 = 6 MCLK cycles for the random read/write cycle time (t_{RC})

Linear Address Window Position Registers (LAW_POS(X) (CR59-5A)

Read/Write Address: 3?5H, Index 59H-5AH
Power-On Default: 000AH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	LINEAR-ADDRESS-WINDOW-POSITION									

Bits 9–0 LINEAR-ADDRESS-WINDOW-POSITION
These registers specify the Linear Address Window Position in 26-bit CPU address space. The Linear Address Window resides on the 64KB, 1MB or 2MB memory boundaries (size aligned boundary). This scheme requires simple control logic and save gates. Some LSBs of this register (illustrated by "xx..xx" in the following table) are ignored because of the size aligned boundary scheme.

LAW Size	Linear Address Window Position Register Bit									
64KB	25	24	23	22	21	20	19	18	17	16
1MB	25	24	23	22	21	20	xx	xx	xx	xx
2MB	25	24	23	22	21	xx	xx	xx	xx	xx

Note: The bits 31-26 are compared externally and the 86C928 expects this result on the SAUP1 and SAUP2 signals. Bits 25-24 are ignored internally for ISA configurations.

Bits 15–10 Reserved

Extended BIOS Flag 2 Register (EXT_BFLG2) (CR5B)

Read/Write Address: 3?5H, Index 5BH
Power-On Default: 00H

15	14	13	12	11	10	9	8
EXT-BIOS-FLAG-REGISTER-2							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-2
Used by the BIOS. Users should not write to this register.

General Output Port Register (GOUT_PORT) (CR5C)

See Bit Descriptions Address: 3?5H, Index 5CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
GENERAL-OUT-PORT				CLOCK-SELECT-OUT			

Bits 3–0 CLOCK-SELECT-OUT (Read Only)
The value stored in these bits is determined as shown in the following table.

3C2H, Bits 3-2	CLOCK-SELECT-OUT
00	0000
01	0001
10	0010
11	Content of CR42 [3:0]

Bits 7–4 GENERAL-OUT-PORT (Read/Write)
These bits are user definable. See Section 12.7.

Extended Horizontal Overflow Register (EXT_H_OVF) (CR5D)

Read/Write Address: 3?5H, Index 5DH
Power-On Default: 00H

7	6	5	4	3	2	1	0
BGT 8	DXP 8	R	SHS 8	R	SHB 8	HDE 8	HT 8

Bit 0 HT 8 - Horizontal Total Bit 8

Bit 1 HDE 8 - Horizontal Display End Bit 8

Bit 2 SHB 8 - Start Horizontal Blank Bit 8

Bit 3 Reserved

Bit 4 SHS 8 - Start Horizontal Sync Position Bit 8

Bit 5 Reserved

Bit 6 DXP 8 - Data Transfer Position Bit 8

Bit 7 BGT 8 - Bus-Grant Terminate Position Bit 8

Extended Vertical Overflow Register (EXT_V_OVF) (CR5E)

Read/Write Address: 3?5H, Index 5EH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	LCM 10	R	VRS 10	R	SVB 10	VDE 10	VT 10

Bit 0 VT 10 - Vertical Total bit 10

Bit 1 VDE 10 - Vertical Display End Bit 10

Bit 2 SVB 10 - Start Vertical Blank Bit 10

Bit 3 Reserved

Bit 4 VRS 10 - Vertical Retrace Start Bit 10

Bit 5 Reserved

Bit 6 LCM 10 - Line Compare Position Bit 10

Bit 7 Reserved

Bus Grant Termination Position Register (BGNT_TPOS) (CR5F)

Read/Write Address: 3?5H, Index 5FH
Power-On Default: 00H

7	6	5	4	3	2	1	0
BGNT-TPOS							

Bits 7–0 BGNT_TPOS - Bus Grant Termination Position
This register specifies the termination position (in character clocks) during the horizontal scan time for the BGNT signal. This value is effective only if bit 2 of the Extended System Cont 1 register (CR50) is enabled.

Section 10: Enhanced Commands Register Descriptions

These registers support the 86C928 Enhanced drawing commands. Access to these registers is enabled via bit 0 of the System Configuration (3?5H, Index 40) register.

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). See Appendix A for a table listing each of the registers in this section and its page number.

Subsystem Status Register (SUBSYS_STAT)

Read Only Address: 42E8H
Power-On Default: 0000H

This read-only register provides information on interrupt status, monitor I.D. and the number of bits per pixel. See the Subsystem Control (42E8H, Write Only) register for details on enabling and clearing interrupts.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	PXL LNG	MONTR-ID 2	1	0	FIFO EMP	FIFO OVF	GE BSY	VSY INT

Bit 0 VSY INT - Vertical Sync Interrupt
0 = No interrupt
1 = Interrupt generated if enabled

Bit 1 GE BSY - Graphics Engine Busy Interrupt
0 = No interrupt
1 = Interrupt generated if enabled

Bit 2 FIFO OVF - FIFO Overflow Interrupt
0 = No interrupt
1 = Interrupt generated if enabled

Bit 3 FIFO EMP - FIFO Empty Interrupt
0 = No interrupt
1 = Interrupt generated if enabled

Bits 6–4 MONTR-ID - Monitor I.D.
010 = 8514/A color 16"
101 = VGA 8503 mono 12"
110 = VGA 8513 color 12"/8512 color 14"
111 = No monitor or other monitor

Bit 7 PXL LNG - Pixel Length (# of bit planes)
0 = 4-bit
1 = 8-bit

The number of bit planes status when bits 5-4 and 7-6 of the Extended System Control 1 register (CR50) are both 00 is derived from display memory size, memory configuration and screen resolution according to the following table. The actual number of bitplanes is the last number in the screen map column.

System Configuration bits 7-5	Memory Configuration bit 1	Advanced Function Control bit 2	Subsystem Status bit 7	Screen Map
Memory: 110 = 1 MByte 111 = 0.5 MByte	Pages: 0 = one 1 = two	Screen Resolution: 0 = 640x480 1 = 1024x768 or 800x600	Status: 0 = 4 bpp 1 = 8 bpp	
111	x	0	1	1024x512x8
111	x	1	0	1024x1024x4
110	0	x	1	1024x1024x8
110	1	0	1	2x1024x512x8 or 1024x512x16
110	1	1	0	2048x1024x4

Bits 15–8 Reserved

Subsystem Control Register (SUBSYS_CNTL)

Write Only Address: 42E8H
Power-On Default: 0000H

This register allows each of several interrupt sources to be enabled or disabled. Interrupt status (Subsystem Status (42E8H, Read Only) can be cleared. This register also controls the software reset of the graphics engine.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GE-RST				FIFO-ENB		GE	VSY					FIFO	FIFO	GEB	VSY
1	0	R	R	EMP	OVF	BSY	ENB	U	U	U	U	CLE	CLO	CLR	CLR

Bit 0 VSY CLR - Clear Vertical Sync Interrupt Status
0 = no change
1 = clear

Bit 1 GEB CLR - Clear Graphics Engine Busy Interrupt Status
0 = no change
1 = clear

Bit 2 FIFO CLO - Clear FIFO Overflow Interrupt Status
0 = no change
1 = clear

Bit 3 FIFO CLE - Clear FIFO Empty Interrupt Status
0 = no change
1 = clear

Bits 7–4 Undefined

Bit 8 VSY ENB - Vertical Sync Interrupt Enable
0 = Disable
1 = Enable

Bit 9 GE BSY- Graphics Engine Busy Interrupt Enable
0 = Disable
1 = Enable

Bit 10 FIFO-ENB OVF - FIFO Overflow Interrupt Enable
0 = Disable
1 = Enable

Bit 11 FIFO-ENB EMP - FIFO Empty Interrupt Enable
0 = Disable
1 = Enable

Bits 13–12 Reserved

Bits 15–14 GE-RST - Graphics Engine Software Reset
00 = no change
01 = Graphics Engine enabled
10 = reset
11 = reserved

Advanced Function Control Register (ADVFUNC_CNTL)

Read/Write Address: 4AE8H
Power-On Default: 0000H

This register enables or disables the enhanced display functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	U	U	U	U	U	WP	MIO	LA	R	SCRN SIZE	=1	ENB EHFC

Bit 0 ENB EHFC - Enable Enhanced Functions
0 = Enable VGA display functions
1 = Enable Enhanced display functions

Bit 1 Reserved = 1

Bit 2 SCRN SIZE - Screen Size (for enhanced modes only)
0 = 640x480
1 = 1024x768 or 800x600

Bit 3 Reserved

Bit 4 LA - Enable Linear Addressing
0 = Disable linear addressing
1 = Enable linear addressing

This bit is ORed with bit 4 of CR58 and is equivalent to it.

Bit 5 MIO - Enable Memory Mapped I/O (MMIO)
0 = Disable MMIO
1 = Enable MMIO

This bit is ORed with bit 4 of CR53 and is equivalent to it.

Bit 6 WP - Enable Write Posting Into FIFO
0 = Write posting disabled
1 = Write posting enabled

This bit is ORed with bit 3 of CR40 and is equivalent to it.

Bits 15–7 Undefined

Current Y-Position Register(CUR_Y)

Read/Write Address: 82E8H
Power-On Default: Undefined

Writing to this register defines the vertical screen coordinate at which the next pixel will be drawn. Reading it produces the current vertical coordinate.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	CURRENT Y-POSITION											

Bits 11–0 CURRENT Y-POSITION

Bits 15–12 Undefined

Current X-Position Register (CUR_X)

Read/Write Address: 86E8H
Power-On Default: Undefined

Writing to this register defines the horizontal screen coordinate at which the next pixel will be drawn. Reading it produces the current horizontal coordinate.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	CURRENT X-POSITION											

Bits 11–0 CURRENT X-POSITION

Bits 15–12 Undefined

Destination Y-Position/Axial Step Constant Register (DESTY_AXSTP)

Read/Write Address: 8AE8H
Power-On Default: Undefined

This register defines the destination Y position for BitBLTs or the axial step constant for line draws.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	DESTINATION Y-POSITION											

Bits 11–0 DESTINATION Y-POSITION
This setting applies only to BitBLTs and pattern fills.

Bits 15–12 Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	LINE PARAMETER AXIAL STEP CONSTANT													

Axial Step Constant = 2 * (min(|dx|,|dy|)) In other words, when drawing a line from point A to point B, determine the change in the X coordinate from A to B and the change in the Y coordinate from A to B. Take the smaller of the two changes and multiply its absolute value by 2.

Bits 13–0 LINE PARAMETER AXIAL STEP CONSTANT
This setting applies only to line draws.

Bits 15–14 Undefined

Destination X-Position/Diagonal Step Constant Register (DESTX_DIASTP)

Read/Write Address: 8EE8H
Power-On Default: Undefined

This register defines the destination X position for BitBLTs or the diagonal step constant for line draws.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	DESTINATION X-POSITION											

Bits 11–0 DESTINATION X-POSITION
This setting applies only to BitBLTs and pattern fills.

Bits 15–12 Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	LINE PARAMETER DIAGONAL STEP CONSTANT													

Diagonal Step Constant = 2 * [min(|dx|,|dy|) - max(|dx|,|dy|)] See the Destination Y-Position/Axial Step Constant (8AE8H) register for an explanation of the terms used in this equation.

Bits 13–0 LINE PARAMETER DIAGONAL STEP CONSTANT
This setting applies only to line draws.

Bits 15–14 Undefined

Line Error Term Read/Write Register (ERR_TERM)

Read/Write Address: 92E8H
Power-On Default: Undefined

This register specifies the initial error term for the line draw operation.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER/ERROR TERM													

Error Term = 2 * min(|dx|,|dy|) - max(|dx|,|dy| - 1 if the starting X < the ending X
Error Term = 2 * min(|dx|,|dy|) - max(|dx|,|dy| if the starting X ≥ the ending X
See the Destination Y-Position/Axial Step Constant (8AE8H) register for an explanation of the terms used in these equations.

Bits 13–0 LINE PARAMETER/ERROR TERM

Bits 15–14 Reserved

Major Axis Pixel Count Register (MAJ_AXIS_PCNT)

Read/Write Address: 96E8H
Power-On Default: Undefined

This register specifies the length (in pixels) of the major (longest) axis.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	RECTANGLE WIDTH/LINE PARAMETER MAX											

Bits 11–0 RECTANGLE WIDTH/LINE PARAMETER MAX
This parameter applies to BitBLTs, line draws and rectangle fills and pattern fills. Its value is the number of pixels along the major axis - 1.

Bits 15–12 Undefined

Graphics Processor Status Register (GP_STAT)

Read Only Address: 9AE8H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	U	AE	HDW BSY	RDT AVA	FIFO-STATUS							

Bits 7–0 FIFO-STATUS
00000000 = 8 FIFO slots available
00000001 = 7 FIFO slots available
00000011 = 6 FIFO slots available
00000111 = 5 FIFO slots available
00001111 = 4 FIFO slots available
00011111 = 3 FIFO slots available
00111111 = 2 FIFO slots available
01111111 = 1 FIFO slots available
11111111 = 0 FIFO slots available

Bit 8 RDT AVA - Read Data Available
0 = No read data is available in the Pixel Data Transfer (E2E8H) register.
1 = Read data is available in the Pixel Data Transfer (E2E8H) register.

Bit 9 HDW BSY - Hardware (Graphics Engine) Busy
0 = not busy
1 = busy - graphics command is executing

Bit 10 AE - All FIFO Slots Empty
0 = At least one FIFO slot is occupied
1 = All FIFO slots empty

Bits 15–11 Undefined

Drawing Command Register (CMD)

Write Only Address: 9AE8H
Power-On Default: Undefined

This register specifies the drawing command and a number of associated control parameters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD-TYPE			BYTE			BUS	WAIT	DRWG-DIR.			DRAW	DIR	LAST	PX	-RD
2	1	0	SWAP	= 0	R	SIZE	YES	2	1	0	YES	TYP	PXOF	MD	/WT

Bit 0 -RD /WT - Read/Write Data
0 = Read data from video memory
1 = Write data to video memory

Bit 1 PX MD - Pixel Mode
0 = Single pixel transferred at a time (through the plane mode)
1 = Multiple pixels transferred at a time (across the plane mode)

Bit 2 LAST PXOF - Last Pixel Off
0 = Last pixel of line or vector draw will be drawn
1 = Last pixel of line or vector draw will not be drawn

Bit 3 DIR TYP - Direction Type
0 = x-y (axial)
1 = Radial

Bit 4 DRAW YES
0 = Move the current position only - don't draw
1 = Draw pixel(s)

Bits 7–5 DRWG-DIR - Drawing Direction
In the following table, radial drawing angle is measured counterclockwise from the X axis. For axial line draws, the line is drawn from left to right or a +X and from right to left for a -X, down for a +Y and up for a -Y. X or Y maj specifies the longest axis.

7–5	Radial (bit 3 = 0)	x-y (Axial -bit 3 = 1)
000	0°	–Y,X maj,–X
001	45°	–Y,X maj,+X
010	90°	–Y,Y maj,–X
011	135°	–Y,Y maj,+X
100	180°	+Y,X maj,–X
101	225°	+Y,X maj,+X
110	270°	+Y,Y maj,–X
111	315°	+Y,Y maj,+X

Bit 8 WAIT YES
0 = Use Graphics Engine-based data
1 = Wait for data to be transferred to or from the CPU through the E2E8H port

Bit 9 BUS SIZE
0 = 8-bit
1 = 16-bit

This parameter applies only to the Pixel Data Transfer (E2E8H) register.

Bit 10 Reserved

Bit 11 Reserved = 0

Bit 12 BYTE SWAP
0 = High byte first, low byte second
1 = Low byte first, high byte second

Bits 15–13 CMD-TYPE - Command Type

000 = NOP. This is used to set up short stroke vector drawing without writing a pixel.
001 = Draw Line. If bit 3 of this register is cleared to 0, the axial step constant, diagonal step constant and error term are used to draw the line. If bit 3 is set to 1, the line will be drawn at the angle specified by bits 7-5 and with a length in pixels as specified by the Major Axis Pixel Count (96E8H) register.
010 = Rectangle Fill. The Major Axis Pixel Count register specifies the number of pixels in each horizontal line and the Minor Axis Pixel Count (BEE8H, Index 00H) register specifies the number of horizontal lines.
011 = Reserved
100 = Reserved
101 = Reserved
110 = BitBLT. This operation copies a rectangle from one part of video memory to another. It uses the Destination X and Y, the Current X and Y and the Major and Minor Pixel Count registers.
111 = Pattern Fill. Same as a BitBlt except that an 8x8 patterned rectangle is transferred repeatedly to the destination rectangle. The starting X coordinate of the source rectangle should always be on an 8 pixel boundary.

Short Stroke Vector Transfer Register (SHORT_STROKE)

Write Only Address: 9EE8H
Power-On Default: Undefined

This register defines two short stroke vectors. These are drawn one at a time based on the setting of the BYTE SWAP bit (bit 12) in the Command (9AE8H) register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRWG-DIR			DRW	PIXEL-LENGTH				DRWG-DIR.			DRW	PIXEL-LENGTH			
2	1	0	-MV	3	2	1	0	2	1	0	-MV	3	2	1	0

Bits 3–0 PIXEL-LENGTH
Value = # pixels - 1

Bit 4 DRW -MV - Draw/Move
0 = Move current position only - don't draw
1 = Draw pixel

Bits 7–5 DRWG-DIR.- Drawing Direction (measured counterclockwise from the X axis)
000 = 0°
001 = 45°
010 = 90°
011 = 135°
100 = 180°
101 = 225°
110 = 270°
110 = 315°

Bits 15–8 These bits duplicate bits 7-0 to define the second short stroke vector.

Background Color Register (BKGD_COLOR)

Read/Write Address: A2E8H
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for a detailed explanation of how and when this color value is used when writing a pixel to video memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BACKGROUND COLOR															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BACKGROUND COLOR															

Bits 31–0 BACKGROUND COLOR
In 32 bpp mode, the upper and lower doublewords are read or written sequentially,

depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Foreground Color Register (FRGD_COLOR)

Read/Write Address: A6E8H
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for a detailed explanation of how and when this color value is used when writing a pixel to video memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOREGROUND COLOR															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOREGROUND COLOR															

Bits 31–0 FOREGROUND COLOR
In 32 bpp mode, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Bitplane Write Mask Register (WRT_MASK)

Read/Write Address: AAE8H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT-PLANE WRITE MASK															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIT-PLANE WRITE MASK															

Bits 31–0 BIT-PLANE WRITE MASK
If bit i = 0, bitplane i is not updated.
If bit i = 1, bitplane i is updated.

Bits 31-0 control planes 31-0 respectively. In 32 bpp mode, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Bitplane Read Mask Register (RD_MASK)

Read/Write Address: AEE8H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT-PLANE READ MASK															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIT-PLANE READ MASK															

Bits 31–0 BIT-PLANE READ MASK
If bit i = 0, bitplane i is not used as a data source
If bit i = 1, bitplane i is used as a data source

Bit-plane read mask for BitBLT and image transfer functions. Bits 31-0 control planes 31-0 respectively. In 32 bpp mode, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Color Compare Register (COLOR_CMP)

Read/Write Address: B2E8H
Power-On Default: Undefined

This register contains the color value that is compared against the current bitmap color if the color compare option is turned on by setting bit 8 of the Pixel Control (BEE8H, Index 0EH) to 1. Bit 7 of the Pixel Control register determines whether a match or a non-match results in a pixel update.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMPARISON COLOR WITH SOURCE															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMPARISON COLOR WITH SOURCE															

Bits 31–0 COMPARISON COLOR WITH SOURCE
In 32 bpp mode, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Background and Foreground Mix Registers (BKGD_MIX, FRGD_MIX)

Read/Write Address: B6E8H (Background), BAE8H (Foreground)
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for a detailed explanation of how and when these registers are used when writing a pixel to video memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									CLR-SRC			MIX-TYPE			
U	U	U	U	U	U	U	U	= 0	1	0	R	3	2	1	0

Bits 3–0 MIX-TYPE
In the general case, a new color is defined. A logical operation such as AND or OR is then performed between it and the current bitmap color. If the bitplane to be written is enabled, the result of this logical "mix" is written to the bitmap as the new pixel color. The following table shows the mix types available (! = logical NOT).

0000	!current	1000	!current OR !new
0001	logical zero	1001	current OR !new
0010	logical one	1010	!current OR new
0011	leave current as is	1011	current OR new
0100	!new	1100	current AND new
0101	current XOR new	1101	!current AND new
0110	!current XOR new	1110	current AND !new
0111	new	1111	!current AND !new

Bit 4 Reserved

Bits 6–5 CLR-SRC
00 = Background Color (the register is the color source)
01 = Foreground Color (the register is the color source)
10 = CPU Data (the CPU is the color source)
11 = Video Memory (the video memory is the color source)

Bit 7 Reserved = 0

Bits 15–8 Undefined

Read Register Data Register (RD_REG_DT)

Read Only Address: BEE8H
Power-On Default: Undefined

A read of this register produces a read of the register specified by bits 2-0 of the Read Register Select (BEE8H, Index E) register. Each read of BEE8H causes bits 2-0 of the Read Register Select (BEE8H, Index E) register to increment by one. All the Multifunction Control (BEE8H, Indices 0H-EH) registers plus the Graphic Processor Status register (9AE8H) can thus be rapidly read by successive reads to BEE8H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Minor Axis Pixel Count Register (MIN_AXIS_PCNT)

Write Only Address: BEE8H, Index 0H
Power-On Default: Undefined

This register specifies the length of the minor (smallest) axis in pixels.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	RECTANGLE HEIGHT											

Bits 11–0 RECTANGLE HEIGHT
Value = # pixels in minor axis - 1

Bits 15–12 INDEX = 0H

Top Scissors (SCISSORS_T)

Write Only Address: BEE8H, Index 1H
Power-On Default: Undefined

This register specifies the top of the clipping rectangle. It is the lowest Y value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	CLIPPING TOP LIMIT											

Bits 11–0 CLIPPING TOP LIMIT

Bits 15–12 INDEX = 1H

Left Scissors (SCISSORS_L)

Write Only Address: BEE8H, Index 2H
Power-On Default: Undefined

This register specifies the left side of the clipping rectangle. It is the lowest X value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	CLIPPING LEFT LIMIT											

Bits 11–0 CLIPPING LEFT LIMIT

Bits 15–12 INDEX = 2H

Bottom Scissors (SCISSORS_B)

Write Only Address: BEE8H, Index 3H
Power-On Default: Undefined

This register specifies the bottom of the clipping rectangle. It is the highest Y value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	CLIPPING BOTTOM LIMIT											

Bits 11–0 CLIPPING BOTTOM LIMIT

Bits 15–12 INDEX = 3H

Right Scissors (SCISSORS_R)

Write Only Address: BEE8H, Index 4H
Power-On Default: Undefined

This register specifies the right side of the clipping rectangle. It is the highest Y value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	CLIPPING RIGHT LIMIT											

Bits 11–0 CLIPPING RIGHT LIMIT

Bits 15–12 INDEX = 4H

Pixel Control Register (PIX_CNTL)

Write Only Address: BEE8H, Index AH
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for an explanation of how and when bits 7-6 of this register are used when writing a pixel to video memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	0	DT-EX-SRC 1	0	R	R	R	PACK DATA	R	0

Bit 0 Reserved = 0

Bit 1 Reserved

Bit 2 PACK DATA
0 = Don't Pack Data (image read)
1 = Pack Data (image read)

This determines whether the data is compressed to 1 bit/pixel or remains unchanged (4, 8, 16 or 24 bits/pixel).

Bits 5–3 Reserved

Bits 7–6 DT-EX-SRC
00 = Foreground Mix register is always selected
01 = Reserved
10 = CPU Data determines Mix register selected
11 = Video Memory current value determines Mix register selected

Bits 11–8 Reserved = 0

Bits 15–12 INDEX = 0AH

Multifunction Control Miscellaneous Register (MULT_MISC)

Write Only Address: BEE8H, Index 0EH
Power-On Default: E000H

15	14	13	12	11	10	9	8	7	6	5	4	3 2	1 0
1	1	1	0	R	R	R	ENB CMP	SRC NEQ	SLW RM	EXT CLIP	RSF	SRC-BA 21 20	DEST-BA 21 20

Bits 1–0 DEST-BA 21 20 - Destination Base Address Bits 21-20
00 = First destination memory address is in the 1st MByte of display memory
01 = First destination memory address is in the 2nd MByte of display memory
10 = First destination memory address is in the 3rd MByte of display memory
11 = First destination memory address is in the 4th MByte of display memory

Bits 3–2 SRC-BA 21 20 - Source Base Address Bits 21-20
00 = First source memory address is in the 1st MByte of display memory
01 = First source memory address is in the 2nd MByte of display memory
10 = First source memory address is in the 3rd MByte of display memory
11 = First source memory address is in the 4th MByte of display memory

Bit 4 RSF - Register Select Flag
0 = Selects lower 16 bits for accesses to 32-bit registers in 32 bpp mode
1 = Selects upper 16 bits for accesses to 32-bit registers in 32 bpp mode

Bit 5 EXT CLIP - External Clipping
0 = Only pixels inside the clipping rectangle are drawn
1 = Only pixels outside the clipping rectangle are drawn

Bit 6 SLW RMW - Slow Read/Modify/Write Cycle
0 = Fast Read/Modify/Write Cycle
1 = Slow Read/Modify/Write Cycle

Bit 7 SRC NEQ - Source Not Equal
0 = Don't update current bitmap if the Color Compare (B2E8) register value is equal to the color value of the source bitmap
1 = Don't update current bitmap if the Color Compare (B2E8) register value is not equal to the color value of the source bitmap

This bit is only active if bit 8 is set to 1.

Bit 8 ENB CMP - Enable Color Compare
0 = Disable color comparison
1 = Enable color comparison

Bits 11–9 Reserved = 0

Bits 15–12 INDEX = 0EH

Read Register Select Register (READ_SEL)

Write Only Address: BEE8H, Index 0FH
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	R	R	R	R	R	R	R	R	R	READ-REG-SEL		

Bits 2–0 READ-REG-SEL - Read Register Select

When BEE8H is read, the value returned is determined by this read register index according to the following:
000 = BEE8H, Index 0H
001 = BEE8H, Index 1H
101 = BEE8H, Index 2H
011 = BEE8H, Index 3H
100 = BEE8H, Index 4H
101 = BEE8H, Index AH
110 = BEE8H, index EH
111 = 9AE8H (Bits 15-13 of the read data are forced to 0.)

The read register index increments by one with each reading of BEE8H.

Bits 15–3 Reserved

Pixel Data Transfer Register (PIX_TRANS)

Read/Write Address: E2E8H
Power-On Default: Undefined

All data to or from the Graphics Engine must pass through this register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMAGE READ/WRITE DATA															

Bits 15–0 IMAGE READ/WRITE DATA

Pixel Data Transfer - Extension Register (PIX_TRANS_EXT)

Read/Write Address: E2EAH
Power-On Default: Undefined

This register is an extension of E2E8H for 32-bit operations.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMAGE READ/WRITE DATA															

Bits 15–0 IMAGE READ/WRITE DATA

Section 11: Enhanced Mode Programming

This section provides programming examples of Enhanced Mode features provided by the 86C928.

11.1 NOTATIONAL CONVENTIONS

The REGMNEMONIC on the left hand side of the arrow is the register mnemonic of the I/O port being written into. Text following a ';' is a comment.

```
REGMNEMONIC ⇐ XXXXH                 ; Load a hexadecimal value into the register.
REGMNEMONIC ⇐ XXXXD                 ; Load a decimal value into the register.
REGMNEMONIC ⇐ XXXX                  ; Load a decimal value into the register
REGMNEMONIC ⇐ XXXXXXXXXXXXXXXXB ; Load a binary value into the register.
```

The programming examples often contain the following step:

wait for FIFO X empty

where X is some number between 1 and 8. This number equals the number of commands to follow that may need to be stored in the FIFO before execution. The number of empty FIFO entries is determined by reading bits [7:0] of the Graphics Processor Status (9AE8H, Read) register. These bits are interpreted as follows:

Bit i = 1 indicates all FIFO entries up to (i+1) are occupied. (FIFO entries are numbered 1-8.)
Bit i = 0 indicates FIFO entry (i+1) and all higher entries are empty.

Thus, if you need 4 empty FIFO slots, you must ensure that bit 4 is cleared to 0.

11.2 INITIAL SETUP

All examples assume the desired mode is selected. See Appendix A for the bit settings required for each mode. The video DAC must also be set up appropriately.

The Bitmap Access Through the Graphics Engine section of the Functional Description explains in detail how the colors, mixes and the data extensions are set for each example. These registers need not be set repeatedly before a series of draw commands if they use the same colors, mixes and data extension.

All bitmap updates are affected by the settings in the clipping registers (BEE8H, Indices 1-4) and the choice of internal or external clipping (BEE8H, Index E, bit 5). These must be set up so they include the area being drawn into.

If color compare is to be used, it must be enabled by setting bit 8 of the Multifunction Control Miscellaneous (BEE8H, Index 0EH) register to 1. Bit 7 of this register determines whether a TRUE or FALSE comparison allows the pixel update to continue. The comparison color is programmed into the Color Compare (B2E8) register.

All planes are enabled for writing unless explicitly set otherwise in an example. This is done via the Write Mask (AAE8H) register.

11.3 PROGRAMMING EXAMPLES

This section provides programming examples for the following Enhanced Mode drawing operations:

- Solid Line
- Textured Line
- Rectangle
- Image Transfer Write—Through the Plane
- Image Transfer Write—Across the Plane
- Image Transfer Read—Through the Plane
- Image Transfer Read—Across the Plane
- BitBLT—Through the Plane
- BitBLT—Across the Plane
- Pattern Fill—Through the Plane
- Pattern Fill—Across the Plane
- Short Stroke Vectors

In addition, an example of the setup and programming of the hardware cursor is provided.

A number of programming steps are repeated in multiple examples. They are explained in detail at their first occurrence. Therefore, readers are encouraged to work through the examples from first to last.

11.3.1 Solid Line

Draw a solid line using axial coordinates from x1,y1 to x2,y2 using the mix NEW and color index 2.

Setup:

Drawing a line using axial coordinates requires programming the axial step constant into the Destination Y-Position/Axial Step Constant (8AE8H) register (DESTY_AXSTP), the diagonal step constant into the Destination X-Position/Diagonal Step Constant (8EE8H) register (DESTX_DIASTP) and the error term into the Error Term (92E8H) register (ERR_TERM). Calculation of these three constants is based on the MAX and MIN parameters as calculated below.

MAX = maximum(ABS(x2–x1), ABS(y2–y1))
MIN = minimum(ABS(x2–x1), ABS(y2–y1))

where maximum means choose the largest of the two terms in parentheses and minimum means choose the smallest. ABS means take the absolute value of the expression.

Bits [7:5] of the Command (9AE8H) register (CMD) specify the drawing direction. Setting bit 7 to 1 means that the Y drawing direction is positive (y1 < y2). Clearing bit 7 to 0 means the Y drawing direction is negative (y1 > y2). Setting bit 6 to 1 means that X is the major (longer) axis (ABS(x2–x1) > ABS(y2–y1)). Clearing bit 6 to 0 means that Y is the major axis. Setting bit 5 to 1 means that the X drawing direction is positive
(x1 < x2). Clearing bit 5 to 0 means that the X drawing direction is negative (x1 > x2). These values replace the DDD sequence in the write to the CMD register shown in the pseudocode below.

The mix NEW represents a setting of 00111B in bits [4:0} of the Foreground Mix (BAE8H) register (FRGD_MIX). This overwrites the present bitmap color value with a new value.

The remainder of the setup is then:

```
Wait For FIFO 3 empty                ; Three commands to follow
FRGD_MIX ⇐ 0027H                     ; color source FRGD_COLOR, mix type is NEW
FRGD_COLOR ⇐ 0002H                   ; color index
MULTIFUNC_CNTL ⇐ A000H               ; Foreground Mix register provides color source and mix type
```

Drawing Operation:

```
Wait For FIFO 7 empty                ; 7 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
MAJ_AXIS_PCNT ⇐ MAX                  ; length in pixels of the major axis
DESTX_DIASTP ⇐ 2 * (MIX–MAX)         ; diagonal step constant
DESTY_AXSTP ⇐ 2 * MIN                ; axial step constant
If the X drawing direction is positive then
    ERR_TERM ⇐ 2 * MIN – MAX         ; error term
else if the X drawing direction is negative
    ERR_TERM ⇐ 2 * MIN – MAX – 1     ; error term
CMD ⇐ 00100000DDD10011B              ; Draw line command (bits [15:13]), Draw (as opposed to
                                     ; just move
                                     ; current position)(bit 4), draw multiple pixels (bit 1), write (bit 0).
```

11.3.2 Textured Line

Draw a textured line from x1,y1 to x2,y2 using the mix NEW for foreground mix, XOR for the background mix, foreground color index 2 and background color index 4. The 16-bit line texture/pattern (PATTERN) is 0011000011110011B. When the pattern bit is a 1, the pixel is written with foreground color and mix. When the bit is a 0, the pixel is written with background color and mix.

Setup:

The XOR mix corresponds to a setting of 00101B in bits [4:0] of the Background Mix (B6E8H) register (BKGD_MIX). See the Solid Line example for an explanation of other parameters and registers used in this example.

```
Wait For FIFO 5 empty                ; 5 commands to follow
FRGD_MIX ⇐ 0027H                     ; color source FRGD_COLOR, NEW mix type
FRGD_COLOR ⇐ 0002H                   ; color index
BKGD_MIX ⇐ 0005H                     ; color source BKGD_COLOR, XOR mix type
BKGD_COLOR ⇐ 0002H                   ; color index
MULTIFUNC_CNTL ⇐ A080H               ; mask data selecting mix register provided by CPU
```

Drawing Operation:

```
Wait For FIFO 7 empty                ; 7 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
MAJ_AXIS_PCNT ⇐ MAX                  ; length in pixels of major axis
DESTX_DIASTP ⇐ 2 * (MIX–MAX)         ; diagonal step constant
DESTY_AXSTP ⇐ 2 * MIN                ; axial step constant
If the X drawing direction is positive then
    ERR_TERM ⇐ 2 * MIN – MAX         ; error term
else if the X drawing direction is negative
    ERR_TERM ⇐ 2 * MIN – MAX – 1     ; error term
CMD ⇐ 00100011DDD10011B              ; Draw line (bits [15:13]), 16-bit bus (bit 9), wait for data from the
                                     ; Pixel Transfer register (bit 8), Draw (bit 4), Multi-pixel (bit 1),
                                     ; Write (bit 0),

COUNT (of PATTERN words) = (MAX + 1 + 15)/16
PIX_TRANS ⇐ 0011000011110011B        ; Output PATTERN to Pixel Transfer register COUNT times
```

An alternate faster method is:

```
COLOR_CMP ⇐ 0011000011110011B        ; This pattern is repeated an appropriate number of times to
                                     ; render the textured line.
```

11.3.3 Rectangle

Draw a rectangle with its top left corner at x1,y1, height = HEIGHT and width = WIDTH. Use the mix NEW and color index 2. The drawing direction (bits [7:5] in the write to the CMD register below) is set to X positive, X major and Y positive (111).

Setup:

```
Wait For FIFO 3 empty                ; 3 commands to follow
FRGD_MIX ⇐ 0027H                     ; color source FRGD_COLOR, NEW mix type
FRGD_COLOR ⇐ 0002H                   ; color index
MULTIFUNC_CNTL ⇐ A000H               ; Foreground Mix register specifies color source and mix type
```

Draw Operation:

```
Wait For FIFO 5 empty                ; 5 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 0100000011110011B              ; Draw rectangle (bits [15:13]), Draw (bit 4), Multi-pixel (bit 1),
                                     ; Write (bit 0)
```

Note

The rectangle can be defined by specifying any one of the four corners and setting bits [7:5] accordingly. Always select X as the major axis (bit 6 =1).

Corner	X direction (bit 5)	Y direction (bit 7)
top left	positive (1)	positive (1)
top right	negative (0)	positive (1)
bottom left	positive (1)	negative (0)
bottom right	negative (0)	negative (0)

11.3.4 Image Transfer Write—Through the Plane

A rectangular image is transferred from the CPU to the video memory through the planes. The image is stored as an array of pixels arranged in row major fashion, in which a byte represents a pixel of data. While transferring in word (16-bit transfer) mode, the number of bytes transferred per row must be even—a dummy byte is added at row end if the width is odd. This example use a mix type of NEW and x1,y1 is the top left corner of the rectangle on the display. The height and width of the rectangle (in pixels) are HEIGHT and WIDTH.

Setup:

```
Wait For FIFO 5 empty                ; 5 commands to follow
FRGD_MIX_REG ⇐ 0047H                 ; color source CPU, mix type NEW
MULTIFUNC_CNTL ⇐ A000H               ; Foreground Mix register is source for color source and mix type
```

Drawing Operation:

```
Wait For FIFO 2 empty                ; 2 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 01010011D0110001B              ; Draw rectangle (bits [15:13]), Swap ON (bit 12),
                                     ; 16-bit transfers (bit 9), Wait for CPU data (bit 8),
                                     ; Always X Major (bit 6) & X Positive (bit 5), Draw (bit 4),
                                     ; Write (bit 0)
```

COUNT (of image pixel data to transfer) = ((WIDTH +1)/2)*HEIGHT words.
PIX_TRANS ⇐ IMAGEDATA; Output image data to Pixel Transfer register for COUNT words.

Notes

In 4 bits/pixel mode, the image has to be packed so a single byte stores 2 pixels. The high nibble of a byte of data contains the *n*th pixel and the low nibble contains the (*n* + 1)th pixel in a row. The row width has to be a multiple of 4, and rows have to be padded with up to 3 pixels of dummy data at each row end. COUNT (of image pixel data to transfer) = ((WIDTH +3)/4)*HEIGHT words.

The command in the above example specified 16 bits/pixel. If it had specified 8 bits/pixel, then for 8-plane modes, COUNT = (WIDTH * HEIGHT) bytes. For 4-plane modes, COUNT = ((WIDTH + 1)/2 * HEIGHT) bytes. To output a byte, load the AL register with one byte and do OUT DX, AX.

11.3.5 Image Transfer Write—Across the Plane

A rectangular image is transferred from the CPU to the video memory across the plane. The monochrome bit image is stored as an array of pixels arranged in row major fashion. A byte represents data for 8 pixels in a row. While using 16-bit transfers, the number of data bits transferred per row must be a multiple of 16—dummy bits are added at the row end if the width is not a multiple of 16. This example uses a mix type of NEW, and x1,y1 is the top left corner of the rectangle on the display. The height and width of the rectangle (in pixels) are HEIGHT and WIDTH. The monochrome image is translated so that pixels corresponding to a 1 in the bit image are given color index 4 and pixels corresponding to a 0 in the bit image are given color index 0.

Setup:

```
Wait For FIFO 5 empty                ; 5 commands to follow
FRGD_MIX ⇐ 0027H                     ; foreground color source, mix type NEW
FRGD_COLOR ⇐ 0004H                   ; foreground color index 4
BKGD_MIX ⇐ 0007H                     ; background color source, mix type NEW
BKGD_COLOR ⇐ 0004H                   ; background color index 0
MULTIFUNC_CNTL ⇐ A080H               ; selection of mix register based on data from the CPU
```

Drawing Operation:

```
Wait For FIFO 5 empty                ; 5 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 01010011D0110011B              ; Draw rectangle (bits [15:13]), Swap ON (bit 12),
                                     ; 16-bit transfers (bit 9), Wait for CPU data (bit 8),
                                     ; Always X Major (bit 6) & X Positive (bit 5), Draw (bit 4),
                                     ; Multiple pixel (bit 1), Write (bit 0)

COUNT (of image pixel data to transfer) = ((WIDTH +15)/16)*HEIGHT words
PIX_TRANS ⇐ IMAGEDATA; Output image data to Pixel Transfer register for COUNT words
```

Note

With 8-bit transfers, the number of data bits transferred per row must be a multiple of 8, so COUNT = ((WIDTH +7)/8)*HEIGHT bytes. To write to a single plane, set the foreground mix to 'logical one' (0002H), the background mix to 'logical zero' (0001H), and the Write Mask register to select the desired (single) plane for updates.

11.3.6 Image Transfer Read—Through the Plane

A rectangular image is transferred from the video memory to the CPU. The image is read through the planes. The image is stored as an array of pixels arranged in row major fashion. A byte represents a pixel of data. While using 16-bit transfers, the number of bytes read per row must be even—a dummy byte is read at row end if the width is odd. For this example, x1,y1 is the top left corner of the rectangle on the display. The height and width of the rectangle (in pixels) are HEIGHT and WIDTH.

Setup:

```
Wait For FIFO 1 empty                ; 1 command to follow
MULTIFUNC_CNTL ⇐ A000H               ; Foreground Mix register is the source of color source and
                                     ; mix type
```

Draw Operation:

```
Wait For FIFO 5 empty                ; 5 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 01010011D0110000B              ; Draw rectangle (bits [15:13]), Swap ON (bit 12),
                                     ; 16-bit transfers (bit 9), Wait for CPU data (bit 8),
                                     ; Always X Major (bit 6) & X Positive (bit 5), Draw (bit 4),
                                     ; Read (bit 0)

Wait for Data Available              ; bit 8 of the Graphics Processor Status (9AE8H, Read)
                                     ; register = 1

COUNT (of Image pixel data to read) = ((WIDTH +1)/2)*HEIGHT words
IMAGEDATA ⇐ PIX_TRAN                 ; Input image data from Pixel Transfer register for COUNT words
```

Notes

In 4 bits/pixel mode, the image has to be packed so a single byte stores 2 pixels. The high nibble of a byte of data contains the *n*th pixel and the low nibble contains the (*n* + 1)th pixel in a row. The number of pixels read per row is a multiple of 4, and rows are padded with up to 3 pixels of dummy data at each row end. COUNT (of Image pixel data read) = ((WIDTH +3)/4)*HEIGHT words.

The command in the above example specified 16 bits/pixel. If it had specified 8 bits/pixel, then for 8-plane modes, COUNT = (WIDTH * HEIGHT) bytes. For 4-plane modes, COUNT = ((WIDTH + 1)/2 * HEIGHT) bytes. To output a byte, load the AL register with one byte and do OUT DX.

11.3.7 Image Transfer Read—Across the Plane

A rectangular monochrome image is transferred from the video memory to the CPU. Plane 0 is the source. The monochrome bit image is stored as an array of pixels arranged in row major fashion. A byte represents data for 8 pixels in a row. While using 16-bit transfers, the number of data bits read per row is a multiple of 16—dummy bits are read at row end if the width is not a multiple of 16. For this example, x1,y1 is the top left corner of the rectangle on the display. The height and width (in pixels) of the rectangle are HEIGHT and WIDTH.

Setup:

```
Wait For FIFO 2 empty                ; 2 commands to follow
MULTIFUNC_CNTL ⇐ A0C0H                ; data from video memory selects mix register
RD_MASK ⇐ 01H                        ; read from plane 0
```

Draw Operation:

```
Wait For FIFO 5 empty                ; 5 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 01010011D0110010B              ; Draw rectangle (bits [15:13]), Swap ON (bit 12),
                                     ; 16-bit transfers (bit 9), Wait for CPU data (bit 8),
                                     ; Always X Major (bit 6) & X Positive (bit 5), Draw (bit 4),
                                     ; Multi-pixel (bit 1), Read (bit 0)

Wait for Data Available              ; bit 8 of the Graphics Processor Status (9AE8H, Read)
                                     ; register = 1
```

COUNT (of image pixel data to transfer) = ((WIDTH +15)/16)*HEIGHT words.

```
IMAGEDATA ⇐ PIX_TRANS                ; Input image data from Pixel transfer register for COUNT words.
```

Note

With 8-bit transfers, the number of data bits transferred per row must be a multiple of 8, so COUNT = ((WIDTH +7)/8)*HEIGHT bytes. With more than 1 plane enabled for read, a '1' is read for the corresponding pixel if all planes enabled for reading are '1's. A '0' is read for the corresponding pixel if any one of the planes enabled for reading is a '0'.

11.3.8 BitBLT—Through the Plane

A source rectangular area in video memory is transferred to a specified destination in video memory. The pixels are written into the destination rectangle using the current foreground mix. Assume x1,y1 is the top left corner of the source rectangle in video memory and x2,y2 is the top left corner of the destination rectangle. The rectangles could be overlapping or disjoint. The height and width (in pixels) of the rectangle are HEIGHT and WIDTH.

Setup:

First, the values of the Srcx, Srcy, Destx and Desty must be determined.

Case 1: Source and destination rectangles do not overlap

For X Positive, Y Positive: Srcx = x1, Srcy = y1, Destx = x2, Desty = y2

Case 2: Source and destination rectangles overlap

```
If x1 > x2
    then if X Positive, Srcx = x1, Destx = x2
else
    Srcx = x1 – WIDTH –1, Desty = x2 – WIDTH –1          ; X Negative

If y1 > y2
    then if Y Positive, Srcy = y1, Desty = y2
else
    Srcy = y1 – HEIGHT –1, Desty = y2 – HEIGHT –1        ; Y Negative

Wait For FIFO 2 empty                ; 2 commands to follow
MULTIFUNC_CNTL ⇐ A000H               ; Foreground Mix register is source of color source and mix type
FRGD_MIX ⇐ 0067H                     ; color source is video memory, mix type is NEW
```

Draw Operation:

```
Wait For FIFO 7 empty                ; 7 commands to follow
CUR_X ⇐ Srcx                         ; set starting horizontal position
CUR_Y ⇐ Srcy                         ; set starting vertical position
DESTX_DIASTP ⇐ Destx                 ; set destination horizontal position
DESTY_AXSTP ⇐ Desty                  ; set destination vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 11000000D0D10011B              ; BitBLT (bits [15:13]), Always X Major (bit 6) , Draw (bit 4),
                                     ; Multi-pixel (bit 1), Write (bit 0)
```

11.3.9 BitBLT—Across the Plane

A source rectangular area in video memory is transferred to a specified destination in display memory. The bits corresponding to a single plane specified by setting the Read Mask register can be transferred. With more than 1 plane enabled for read, if all the bits in the planes enabled for read are '1's then a '1' is read. If a bit in any one of the planes enabled for read is a '0', then '0' is read. Assume x1,y1 is the top left corner of the source rectangle on the display, and x2,y2 is the top left corner of the destination rectangle. The image is read from plane 0 and written to plane 2. The rectangles could be overlapping or disjoint. The height and width (in pixels) of the rectangle are HEIGHT and WIDTH.

Setup:

First, the values of the Srcx, Srcy, Destx and Desty must be determined.

Case 1: Source and destination rectangles do not overlap

For X Positive, Y Positive: Srcx = x1, Srcy = y1, Destx = x2, Desty = y2

Case 2: Source and destination rectangles overlap

```
If x1 > x2
    then if X Positive, Srcx = x1, Destx = x2
else
    Srcx = x1 – WIDTH –1, Desty = x2 – WIDTH –1          ; X Negative

If y1 > y2
    then if Y Positive, Srcy = y1, Desty = y2
else
    Srcy = y1 – HEIGHT –1, Desty = y2 – HEIGHT –1        ; Y Negative
```

```
Wait For FIFO 5 empty                ; 5 commands to follow
MULTIFUNC_CNTL ⇐ A0C0H                ; data from video memory selects mix register
FRGD_MIX ⇐ 0002H                     ; Always 'logical 1'
BKGD_MIX ⇐ 0001H                     ; Always 'logical 0'
RD_MASK ⇐ 0001H                      ; Read from plane 0
WRT_MASK ⇐ 0004H                     ; Plane 2 enabled for write
```

Draw Operation:

```
Wait For FIFO 7 empty                ; 7 commands to follow
CUR_X ⇐ Srcx                         ; set starting horizontal position
CUR_Y ⇐ Srcy                         ; set starting vertical position
DESTX_DIASTP ⇐ Destx                 ; set destination horizontal position
DESTY_AXSTP ⇐ Desty                  ; set destination vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 11000000D0D10011B              ; BitBLT (bits [15:13]), Always X Major (bit 6) , Draw (bit 4),
                                     ; Multi-pixel (bit 1), Write (bit 0)
```

Note

It is possible to translate a monochrome image, e.g., text fonts, stored in a single plane in video memory into a 2-color image. This is accomplished by setting the mix registers differently and setting the desired background and foreground colors. If the source bit is a '1', then the corresponding pixel at the destination is colored with the foreground color index. The destination pixel is colored with the background color index if the corresponding source bit is a '0'. The setup for this is as follows:

```
FRGD_MIX ⇐ 0027H          ; color source foreground, mix type NEW
BKGD_MIX ⇐ 0007H          ; color source background, mix type NEW
FRGD_COLOR ⇐ 0004H        ; foreground color
BKGD_COLOR ⇐ 0001H        ; background color
```

11.3.10 PatBLT—Pattern Fill Through the Plane

An 8x8 pixel pattern is initially copied into video memory using an image transfer operation. This source pattern is then repeatedly copied to a destination rectangle of arbitrary size. Each copy is aligned to an 8-pixel boundary. The pixels are written into the destination rectangle using the current foreground mix. Assume x1,y1 is the top left corner of the source rectangle on the display and x2,y2 is the top left corner of the destination rectangle. The height and width (in pixels) of the rectangle are HEIGHT and WIDTH.

Setup:

```
Wait For FIFO 2 empty                ; 2 commands to follow
MULTIFUNC_CNTL ⇐ A000H               ; Foreground Mix register is source of color source and mix type
FRGD_MIX ⇐ 0067H                     ; color source is video memory, mix type is NEW
```

Draw Operation

```
Wait For FIFO 7 empty                ; 7 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
DESTX_DIASTP ⇐ x2                    ; set destination horizontal position
DESTY_AXSTP ⇐ y2                     ; set destination vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 11100000D0D10011B              ; Pattern Fill (bits [15:13]), Always X Major (bit 6) , Draw (bit 4),
                                     ; Multi-pixel (bit 1), Write (bit 0)
```

Note

The X coordinate of the source rectangle must be on an 8 pixel boundary (x=0, x=8, etc.). This pattern should be located in the non-displayed area of the bitmap. The source X destination patterns should be non-overlapping.

11.3.11 PatBLT—Pattern Fill Across the Plane

An 8x8 pixel pattern is initially copied into video memory using an image transfer operation. This source pattern is then transferred to a specified destination in video memory. The bits corresponding to a single plane specified by setting the Read Mask register can be transferred. With more than 1 plane enabled for read, if all the bits in the planes enabled for read are '1's, then a '1' is read. If a bit in any one of the planes enabled for read is a '0', then '0' is read. Assume x1,y1 is the top left corner of the source rectangle on the display, and x2,y2 is the top left corner of the destination rectangle. The image is read from plane 0 and written to plane 2. The height and width of the rectangle are HEIGHT and WIDTH.

Setup:

```
Wait For FIFO 5 empty                ; 5 commands to follow
MULTIFUNC_CNTL ⇐ A0C0H                ; data from video memory selects mix register
FRGD_MIX ⇐ 0002H                     ; Always 'logical 1'
BKGD_MIX ⇐ 0001H                     ; Always 'logical 0'
RD_MASK ⇐ 0001H                      ; Read from plane 0
WRT_MASK ⇐ 0004H                     ; Plane 2 enabled for write
```

Draw Operation:

```
Wait For FIFO 7 empty                ; 7 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
DESTX_DIASTP ⇐ x2                    ; set destination horizontal position
DESTY_AXSTP ⇐ y2                     ; set destination vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 11100000D0D10011B              ; Pattern Fill (bits [15:13]), Always X Major (bit 6) , Draw (bit 4),
                                     ; Multi-pixel (bit 1), Write (bit 0)
```

Notes

The X coordinate of the source rectangle must be on an 8 pixel boundary (x=0, x=8, etc.). This pattern should be located in the non-displayed area of the bitmap. The source X destination patterns should be non-overlapping.

To expand the source mono pattern into a 2-color pattern, set the foreground mix to 27H, the background mix to 7H and the foreground and background colors as desired. Also set the write mask to FFH.

11.3.12 Short Stroke Vectors

Using short stroke vectors, short lines up to 15 pixels in length can be drawn rapidly because it is not necessary to calculate and set the line constants. Such lines are constrained to one of the 8 directions at 45 degree increments starting at 0 degrees. The current point x1,y1 is set and a NOP command is issued to set all the desired drawing parameters without actually writing a pixel. For example, bit 2 (Last Pixel Off) would be set to 1 (OFF) for drawing connected lines until the last line is drawn. The short stroke vector parameters are then loaded in the Short Stroke Vector Transfer (9EE8H) register (SHORT_STROKE). Two vectors can be defined at a time, one in the low byte and one in the high byte. For the low byte, bits [7:5] define the direction, with bit 4 set to '1' for a draw operation or to '0' for a move current position operation. Bits [3:0] define the length of the short line. Let SSVD0, SSVD1, ...SSVDN–1 bytes be the short stroke vector data for N lines.

Setup:

```
Wait For FIFO 3 empty                ; 3 commands to follow
MULTIFUNC_CNTL ⇐ A000H               ; Foreground Mix register is source of color source and mix type
FRGD_MIX ⇐ 0027H                     ; use foreground color, mix type NEW
FRGD_COLOR ⇐ 0004H                   ; foreground color index 4
```

Draw Operation:

```
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
CMD ⇐ 00010010XXX11111B              ; NOP (bits [15:13]), Byte Swap (bit 12), 16-bit transfers (bit 9) ,
                                     ; Draw (bit 4), RadialDir (bit 3), LPixelOff (bit 2), Multi-pixel (bit 1),
                                     ; Write (bit 0)
```

```
While space available in the FIFO
   SHORT_STROKE ⇐ SSVD1 SHL 8 + SSVD0   ; SSVD1 shifted to high byte, SSVD0 in low byte
   SHORT_STROKE ⇐ SSVD3 SHL 8 + SSVD2   ; Byte swap turned on to read vectors out in
                                        ; correct order
                .
                .
                .
   SHORT_STROKE ⇐ SSVDN-1 SHL 8 + SSVDN-2
```

11.3.13 Programmable Hardware Cursor

A programmable cursor is supported which is compatible with the Microsoft Windows and X11 cursor definitions. The cursor is operational only in the S3 Enhanced Mode. The cursor size is 64 pixels wide by 64 pixels high, with the cursor pattern stored in an off-screen area of video memory. Two 2-bits-per-pixel images 64 bits wide by 64 bits high (512 bytes per image) define the cursor shape. The first bit image is an AND mask and the second bit image is an XOR mask. The following is the truth table for the cursor display logic.

AND Bit	XOR Bit	Displayed (Microsoft Windows)	Displayed (X11)
0	0	Cursor Background Color	Current Screen Pixel
0	1	Cursor Foreground Color	Current Screen Pixel
1	0	Current Screen Pixel	Cursor Background Color
1	1	NOT Current Screen Pixel	Cursor Foreground Color

The Cursor Location High register (3?5H, Index 0EH) is used to hold the hardware cursor foreground color when in Enhanced Mode. Similarly, Cursor Location Low (3?5H, index 0FH) is used to hold the hardware cursor background color. When using a true color mode (16- or 24 bits/pixel), the true color foreground and background colors are programmed into the Hardware Graphics Cursor Foreground Stack register (3?5H, Index 4AH) and the Hardware Graphics Cursor Background Stack register (3?5H, Index 4BH) respectively. Each of these is a stack of 3, 8-bit registers. The stack pointers are reset to 0 by reading the Hardware Graphics Cursor Mode register (3?5H, Index 45H). The color value is then programmed by 2 (16-bit) or 3 (24-bit) consecutive writes (low byte, second byte, third byte) to the appropriate (foreground or background) register.

Enabling/Disabling the Cursor

The hardware cursor is disabled when a VGA-compatible mode is in use. It can be enabled or disabled when in the Enhanced mode, as follows.

```
S3R9 ⇐ A0H                ; Unlock System Control registers
HGC-MODE BIT 0 ⇐ 1        ; Enable hardware cursor
HGC-MODE BIT 0 ⇐ 0        ; Disable hardware cursor
S3R9 ⇐ 0                  ; Lock System Control registers
```

Positioning the Cursor

The cursor can be positioned at any point on the display, with the X,Y coordinates ranging from 0 to 2047. This enables the full cursor images to be displayed on the screen and partial cursor images to be displayed at the right edge and the bottom edge of the screen. The cursor offset OX,OY has to be set to 0,0 for a 1024x768 resolution. If X is > (1024 – 64) or Y is > (768 – 64), then a partial cursor is visible at the right edge or top edge of the screen respectively. Note that if Y ≥ 768 then the cursor is not visible; it is residing in the off-screen area.

A partial cursor image can be displayed at the left edge or the top edge of the screen. To enable partial cursor display at the top edge of the screen, Y is set to 0 and the Y offset register is set to OY (range from 0 to 63). This displays the bottom 64–OY rows of the cursor image at the currently set X position and the top edge of the screen. Similarly, a partial cursor can be displayed at the left edge of the screen by setting X to 0 and the X offset register to OX (range from 0 to 63). This displays the right 64–OX columns of the cursor image at the currently set X and the left edge of the screen. The following pseudocode illustrates cursor positioning.

```
S3R9 ⇐ A0H                                  ; Unlock System Control registers
HWGC-CX(H) ⇐ MS 3 bits of X cursor position ; bits [10:8]
HWGC-CX(L) ⇐ LS 8 bits of X cursor position ; bits [7:0]
HWGC-CY(L) ⇐ LS 8 bits of Y cursor position ; bits [7:0]
HWGC-DX ⇐ Cursor Offset X position          ; bits [5:0]
HWGC-DY ⇐ Cursor Offset Y position          ; bits [5:0]
HWGC-CY(H) ⇐ MS 3 bits of Y cursor position ; bits [10:8]
S3R9 ⇐ 0                                    ; Lock System Control registers
```

Programming the Cursor Shape

The AND and the XOR images are 512 bytes each. The cursor image bitmaps are loaded into the display bitmap at some Y location (YI) in the off-screen area and start X is set at 0. This cursor pattern load is accomplished by performing an image transfer operation with the destination rectangle on the display set to 0,YI, the width set to 1024, and height set to 1 (2 if the 4 plane option is being used). The AND and XOR image bitmaps are transferred to the video memory via the Pixel Data Transfer (E2E8H) register. The image is loaded into the register as a sequence of AND image mask words followed by a word of the XOR image mask. This alternation is continued until the entire cursor pattern is loaded. The Hardware Graphics Cursor (3?5H, Indices 4CH and 4DH) registers are programmed to YI so the controller knows the start of the cursor definition in video memory. The X location is always assumed to be 0.

The AND_IMAGE is defined by the 256 words ANDword0, ANDword1,...ANDword255 and the XOR_IMAGE is defined by the 256 words XORword0, XORword1,...XORword255.

Setup:

```
S3R9 ⇐ A0H                                  ; Unlock System Control registers
HWGC-STA(H) ⇐ MS 4 bits of the cursor storage Y start = YI (bits [11:8])
HWGC-STA(L) ⇐ LS 8 bits of the cursor storage Y start = YI(bits [7:0])
S3R9 ⇐ 0                                    ; Lock System Control registers

Wait for FIFO 7 empty
MULTIFUNC_CNTL ⇐ A000H                      ; Foreground Mix register is source of color source and mix type
FRGD_MIX ⇐ 47H                              ; color source is CPU, mix type NEW
```

Draw Operation:

```
CUR_X ⇐ 0; set starting horizontal position
CUR_Y ⇐ Y1                                  ; set starting vertical position, which should be in the
                                            ; off-screen area
MAJ_AXIS_PCNT ⇐ (1024-1)                    ; rectangle width
MIN_AXIS_PCNT ⇐ (1-1)                       ; rectangle height
CMD ⇐ 0101001111010001B                     ; Rectangle Fill (bits [15:13]), Byte Swap (bit 12),
                                            ; 16-bit bus (bit 9), Draw (bit 4), Write (bit 0)
```

While FIFO space available
    PIX_TRANS ⇐ ANDword0, XORword0
    PIX_TRANS ⇐ ANDword1, XORword1
        .
        .
        .
    PIX_TRANS ⇐ ANDword255, XORword255

Notes

I/O operations to the registers used to program the cursor and set up Extended Mode are byte transactions. To write to these registers, an index is written at the I/O port 3?4H (? = D for color or B for monochrome) and the data is written to I/O port 3?5H.

If the cursor is not 64 bits by 64 bits, the given images should be padded to make the cursor image 64 bits by 64 bits. The padded area should be made transparent by padding the extra AND mask bits with '1's and the extra XOR bits by '0's.

For the 4-plane mode with 0.5 MByte memory option, the cursor pattern is stored in the off-screen video memory in a rectangle of width 1024 and height 2. For the 4-plane mode with 1 MByte memory option, the cursor pattern is stored in the off-screen video memory in a rectangle of width 2048 and height 1. In all cases the clipping rectangle should be set to include the cursor definition rectangle prior to loading the cursor image.

The cursor can be programmed to 64 bits by 64 bits in all modes, including the 16 and 24 bits/pixel true color modes. When a 2x or 3x zoom is selected by setting bit 2 or bit 3 respectively in the Hardware Graphics Cursor Mode (3?5H, Index 45H) register, the colors are automatically taken from the Hardware Graphics Cursor Foreground Stack (3?5H, Index 4A) and the Hardware Graphics Cursor Background Stack (3?5H, Index 4B).

Section 12: Hardware Interface

This section explains how the 86C928 interfaces to external devices. Discussed are interfaces to the CPU and I/O bus, BIOS ROM, video memory, video DAC, clock chip and co-processor. Hardware setup and initialization, the General I/O Port and genlocking are also described.

12.1 BUS INTERFACES

The 86C928 interfaces to an ISA, EISA or local bus. The EISA bus interface is described in the *86C805/86C928 EISA Bus Configuration Design Guide*. The 16-bit ISA interface is shown in Figure 12-1.

Data buffers are required to meet the drive specification of the ISA bus. Data buffer control signals DBENL, DBENH, and DBDIR are provided. DBDIR is driven low for reads and high for writes. DBENL is used to control the buffer for SD[7:0]. DBENH controls the buffer for SD[15:8]. Further descriptions of their use are given in Sections 12.3 and 12.5 on BIOS ROM and video DAC interfacing, respectively.

For some ISA systems, the control signal inputs from the ISA bus to the 86C928 must be buffered with a 74ALS244 and resistor terminated in order to prevent voltage undershoot from damaging the 86C928. Address decoding is provided entirely by the 86C928.

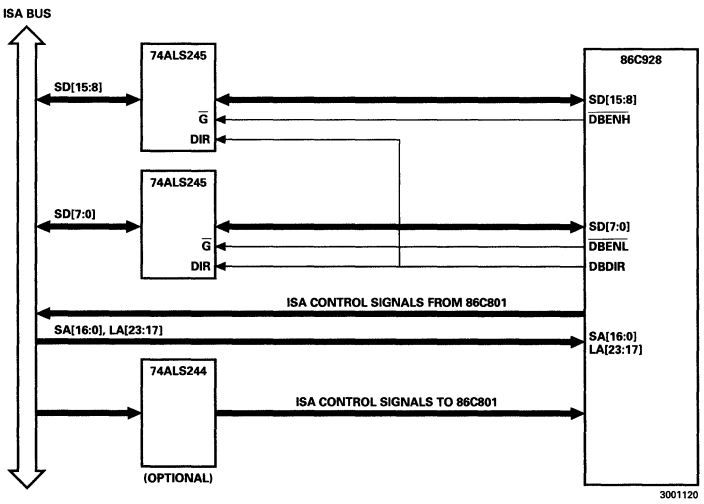

Figure 12-1. 86C928/ISA Bus Interface

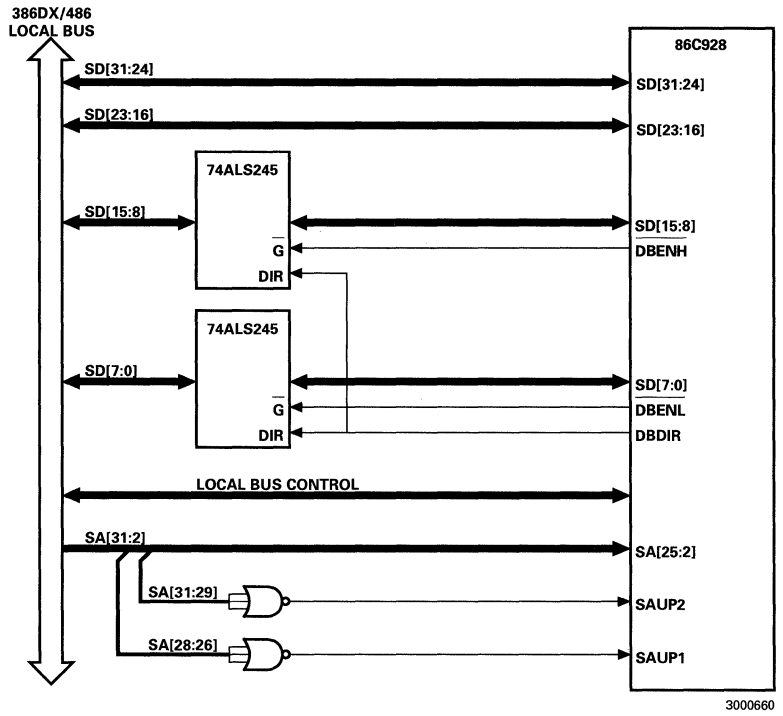

Figure 12-2. 86C928/Local Bus Interface

The 86C928 interfaces to a 386DX/486 local bus as shown in Figure 12-2. The only significant difference from the ISA interface is the generation of the SAUP1 and SAUP2 inputs. These signals are decodes of upper address bits [28:26] and [31:29] respectively and are driven high when all the bits are 0's. If separate video BIOS ROMs are implemented, power-on strapping bit PD4 is strapped to 0 and the SAUP2 input becomes the ROMCS output. A PLD is then required to decode SAUP1 from SA[31:26]. If both SAUP1 and SAUP2 are used, 2 NOR gates are sufficient as shown in Figure 12-2.

The local bus control inputs for the 86C928 do not require buffering. The upper data word can be optionally buffered in this configuration.

12.1.1 Bus Sizing

Except for video DAC accesses, the 86C928 ISA interface is always 16 bits for I/O cycles. The ISA interface is configurable to 8 or 16 bits for memory accesses, depending on the register bit settings described next.

At reset, memory cycles are always 8 bits wide for an ISA bus implementation. This is to provide compatibility with any monochrome cards which may be in the system. In the 8-bit case, MEMCS16 will always be tri-stated. The interface for video memory cycles may be changed to 16-bit by setting bit 7 of the Miscellaneous 1 register (3?5H, Index 3AH) to 1. In this case, MEMCS16 will be generated for memory cycles according to the strapping of system configuration bit PD12 at reset, as reflected by bit 12 of the Reset State

Read 2 register (3?5H, Index 37H). If this bit is pulled high on reset, MEMCS16 will be generated normally by the 86C928. If pulled low, MEMCS16 will be driven by inverted bit 7 of the Miscellaneous 1 register for use by an external decoder in systems with extremely fast MEMCS16 requirements. See the *86C801 ISA Bus Design Guide* for more information on MEMCS16 generation.

The 386DX/486 interface is always 32 bits for both memory and I/O cycles.

12.1.2 Local (386DX/486) Bus Active Signal (LOCA)

For the 86C928 interface to the local 386DX/486 bus, CPU accesses to the graphics memory or I/O space will be decoded by both the 86C928 and the ISA/EISA controller. In such cases, some method must be provided to prevent the bus controller from generating a bus cycle.

Some ISA/EISA controllers provide registers which allow portions of ISA memory or I/O space to be configured as local CPU space. Once programmed, accesses to this space will not generate ISA/EISA bus cycles. Many bus controllers do not provide such registers, so another method must be used to inhibit ISA/EISA cycles.

The 86C928 activates the LOCA pin whenever a local bus graphics access occurs. This signal is used to drive the "local bus active" pin provided by many chip sets, which inhibits generation of ISA/EISA cycles.

Two styles of LOCA signals can be generated by the 86C928. If system configuration bit PD11 is pulled high, this selects a tri-state LOCA signal. When this bit is puled low, a non-tri-state LOCA signal is generated.

Figure 12-3 shows the waveform for the tri-state version of LOCA. Once a valid graphics access has been decoded, the 86C928 drives LOCA low at the beginning of the first or second processor T2 cycle. This selection is programmable through bits 4 and 5 of the System Configuration register ((3?5H, Index 40H). If the decode wait is programmed to 00, LOCA will be available early in the first T2 cycle and no wait states will be induced. If the decode wait is programmed to 01, LOCA will be available early in the second T2 cycle. LOCA is held low until SRDY is generated, at which time it is driven high for one clock and then tri-stated during the first T2 of the next cycle. Three-stating LOCA allows more than one local bus peripheral to share the same "local bus active" pin on the ISA/EISA bus controller.

The non-tri-state version of LOCA is generated a short delay after the assertion of SADS. It remains low until T1 of the next cycle. The waveform for this signal is shown in Figure 12-4. This configuration works well if the 86C928 is the only device driving the "local bus active" signal.

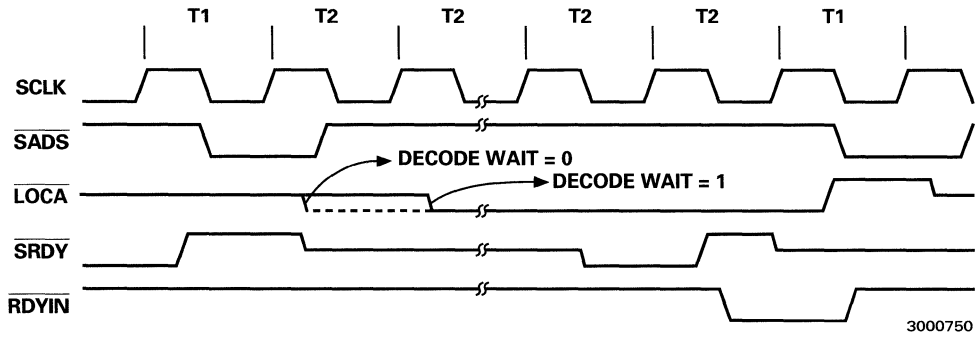

Figure 12-3. Tri-State LOCA Generation

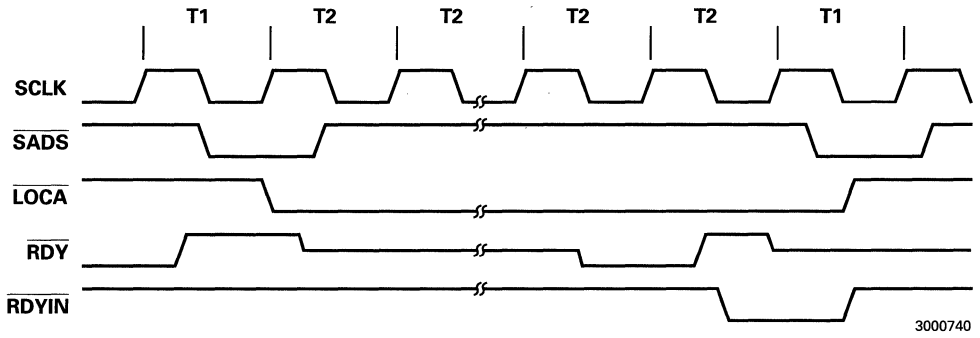

Figure 12-4. Early, Non-Tri-State LOCA Generation

If system configuration bit PD12 is tied low, LOCA and SRDY generation are suppressed for video DAC accesses. The 86C928 will generate write cycles to the local video DAC and the ISA/EISA controller will also generate cycles to an off-board video DAC (mirroring). Video DAC reads will always be from the local device. If PD12 is tied high, all video DAC accesses will be performed as local bus cycles.

12.1.3 RDY Generation

The 86C928 asserts its SRDY output to signal the end of a cycle. Some systems synchronize or otherwise delay this signal and then assert RDY to the processor. If this is done, this RDY signal should also be fed to the RDYIN input of the 86C928. The 86C928 holds read data active until RDYIN is asserted. If the SRDY signal is not intercepted, it should be fed to both the processor RDY input and the 86C928 RDYIN input.

12.1.4 Local Bus Clocking

The 86C928 expects a 1X SCLK like that used in a 486 system. Figure 12-5 shows one possible circuit for building such a 1X clock from the 386 2X clock. Since the 86C928 requires a clock during reset, any circuit used to generate a synchronized 1X clock must be free-running during RESET.

12.2 RESET AND INITIALIZATION

The RESET signal initializes the internal state machines and registers when it goes high. At the falling edge of RESET, the state of the pixel data bus, PD[15:0], is sampled and the data loaded into the Configuration 1 and 2 (3?5H, Indices 36H, 37H) registers. This data is used for system configuration, such as system bus selection, memory configuration, and operating modes.

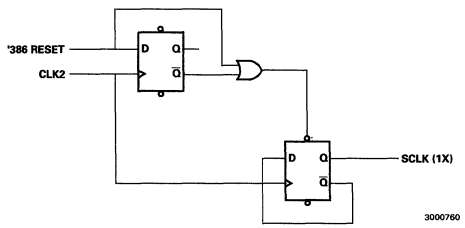

Figure 12-5. 1X Clock Generation

The definitions of bits PD[15:0] at the falling edge of RESET are shown in Table 12-1.

Table 12-1. Definition of PD[15:0] at the Falling Edge of RESET

Bit(s)	Value	Function
System Bus Select		
1,0	00	EISA
	01	386DX/486 local bus
	11	ISA
VGA ROM Data Bus Width (ISA)		
2	0	16 bits
	1	8 bits
VGA BIOS ROM Enable (ISA)		
3	0	All accesses between C0000H-C7FFFH are enabled except for accesses between C6000H-C67FFH, which are disabled.
	1	All accesses between C0000H-C7FFFH are enabled
Address Bit Range for $\overline{\text{MEMCS16}}$ Decode (ISA) or SAUP2/$\overline{\text{ROMCS}}$ Selection (Local Bus)		
4	0	LA[23:17], SA16 (ISA Bus) SAUP2 input pin becomes $\overline{\text{ROMCS}}$ output (Local Bus)
	1	LA[23:17] (ISA Bus) SAUP2 input pin unchanged (Local Bus)
Display Memory Size (ISA, EISA, Local Bus)		
7-5	000	4 MBytes
	010	3 MBytes
	100	2 MBytes
	110	1 MByte
	111	0.5 MByte
VGA Subsystem Setup Select (ISA) or Setup Select (Local Bus)		
8	0	VGA Subsystem Setup Bit is bit 5 of the Video Subsystem Access/Setup register (46E8H). (ISA) Disable 86C928 and use ISA/EISA adapter (Local Bus)
	1	VGA Subsystem Setup Bit is bit 4 of the Video Subsystem Access/Setup register (46E8H). (ISA) Enable 86C928 (Local Bus)
Reserved Bit (ISA, EISA, Local Bus)		
9		Always 1
Extended Monitor Identification (ISA, EISA, Local Bus)		
10	0 or 1	Extension of bits 15-13. See the ROM BIOS documentation.

Table 12-1. Definition of PD[15:0] at the Falling Edge of RESET (Continued)

Bit(s)	Value	Function
No Wait State (ISA) or LOCA type (Local Bus)		
11	0	NOWS disabled (ISA) LOCA is a level signal (Local Bus)
	1	NOWS enabled (ISA) LOCA is a tri-state signal (Local Bus)
MEMCS16 Select (ISA) or /LOCA and SRDY for video DAC (Local Bus)		
12	0	MEMCS16 generated externally (ISA) SHADOW ONLY No LOCA and SRDY for video DAC accesses (Local Bus)
	1	86C928 generates MEMCS16 (ISA) [redacted] MUST USE IN 'DUAL BUS' Normal LOCA and SRDY for video DAC accesses (Local Bus)
Monitor Type Identification (ISA, EISA, Local Bus)		
15-13		See the ROM BIOS documentation.

12.3 VGA BIOS ROM INTERFACE

The VGA BIOS ROM contains power-on initialization, mode setup, and video data read/write routines.

In the ISA bus case (Figure 12-6), the 86C928 maps the CPU memory address spaces for the VGA BIOS ROM into physical ROM addresses. The BIOS ROM chip enable signal ROMCS provides the EPROM chip enable and MEMR provides the output enable. The slow access time of the EPROMs requires the early enable provided by MEMR. For VGA BIOS ROM reads, the ROM data bus width can be selected as 8-bit or 16-bit through system configuration strapping of PD2. In the 8-bit ROM configuration, the 86C928 does not generate MEMCS16 for VGA BIOS ROM read cycles. Bus sizing is handled by the ISA bus. Data buffer control signals DBDIR, DBENL, DBENH, and the ROMCS chip enable signal are automatically generated.

In the 86C928 local bus case, the video BIOS can be part of the system ROM or it can be implemented separately as shown in Figure 12-7. To implement a separate video BIOS, the PD4 power-on strap must be pulled low. This causes pin 44 to become the ROMCS chip select output when the 86C928 is in the local bus mode. The ROMCS signal is active for valid BIOS addresses. The ROMs are connected through their own buffers to the ISA bus, and the ISA MEMR control signal qualifies the output enable. If 16-bit BIOS operation is required, the ROMCS signal may be used to drive the MEMCS16 line through an open collector buffer.

The VGA BIOS ROM uses the address range C0000H–C5FFFH and C6800H-C7FFFH for all standard and enhanced features.

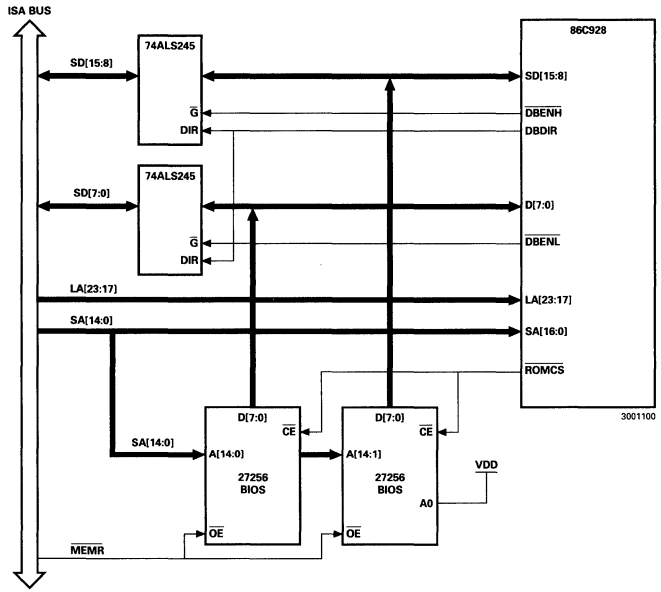

Figure 12-6. ROM BIOS Interface (ISA)

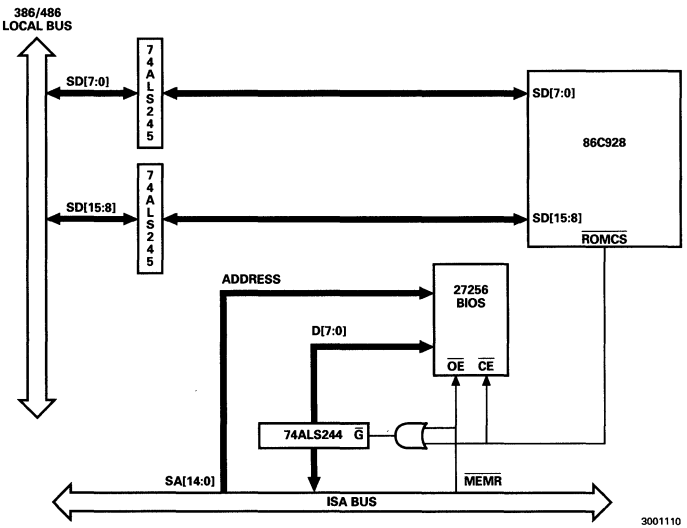

Figure 12-7. ROM BIOS Interface (Local Bus)

The CPU memory and ROM physical address mapping for the VGA BIOS ROM are shown in Table 12-2.

Table 12-2. ROM BIOS Address Mapping

ROM Address	Memory Location (HEX)	Capacity (KBytes)	Physical Address (HEX)
STD BIOS	C0000 – C5FFF C6800- C7FFF	4 × 6+6 = 30	0000 – 5FFF 6800- 7FFF
EXT BIOS	C0000 – C7FFF	32	6800 – 7FFF

Strapping of PD3 at reset determines whether only the standard or both the standard and extended range is selected. If bit 7 of the Memory Configuration Register (3?5H, Index 31H) is set to 1, then all 32 KBytes of BIOS ROM are available, regardless of strapping bit PD3. If bit 7 is reset to 0, PD3 determines the video BIOS address range.

12.4 VIDEO DAC/VIDEO DISPLAY INTERFACE

The 86C928 decodes all CPU accesses to the video DAC registers and provides all required control signals. The interface is shown in Figure 12-8. The *86C928 Local Bus Interface Design Guide* describes the interface to a video DAC that supports a serial input data port (SID) connection. A Technical Note lists all supported video DACs.

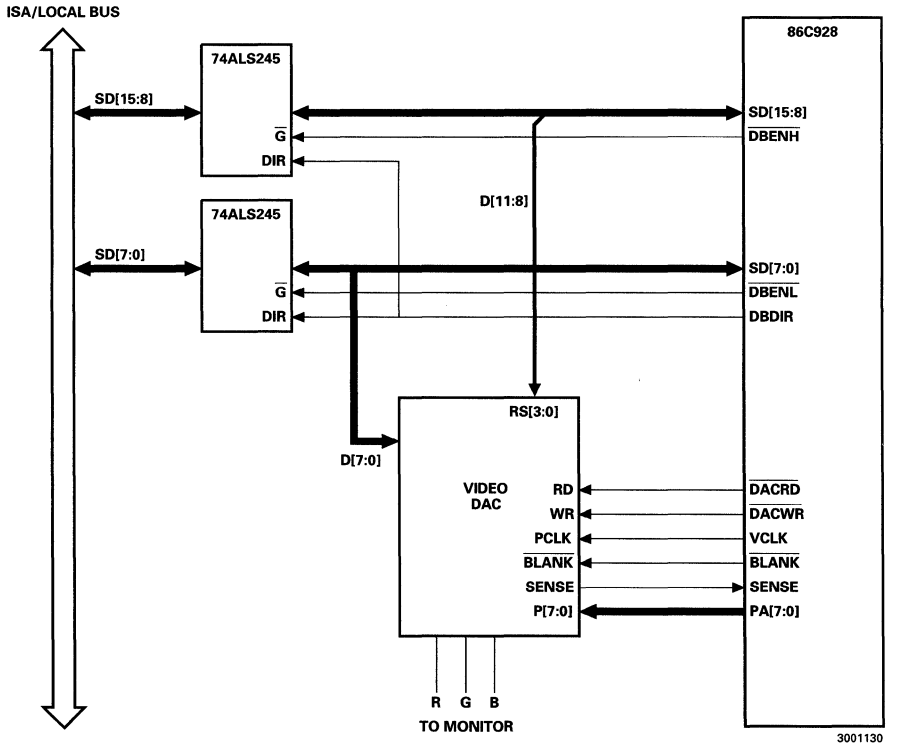

Figure 12-8. Video DAC Interface

When the video DAC is programmed for 16- or 24 bits/pixel operation, the pixel color data on PA[7:0] bypasses the color lookup table. In 16 bits/pixel mode, the pixel color data is latched either on two consecutive rising edges of VCLK or on both the rising and falling edge of a VCLK cycle. For 24 bits/pixel mode, the pixel color data is latched on 3 consecutive rising edges of VCLK.

The IBM 85XX series display monitors provide a 3-bit monitor ID for use by the ROM BIOS during initialization. These signals can be input to the 86C928 via the MID[2:0] pins. The monitor ID data is encoded as shown in Table 12-3.

Strapping of PD[10, 15:13] selects other monitors. See Section 12.2, Reset and Initialization.

Table 12-3. Monitor ID Encoding

MID[2-0]	Monitor Type
000	Not assigned
001	8604 MONO 15" or 19'
010	8514/A COLOR 16"
011	8515 COLOR 14"
100	Not assigned
101	VGA 8503 COLOR 12"
110	VGA 8513 COLOR 12" or VGA 8512 COLOR 14"
111	Not assigned

12.5 VIDEO MEMORY INTERFACE

The 86C928 provides direct support for 0.5-MByte, 1-MByte and 2-MByte VRAM configurations, as shown in Figure 12-9. Note that SOE0 selects the first megabyte and SXNR the second. The addition of a simple external decoder allows support for 3 or 4 MBytes of VRAM, as shown in Figure 12-10. The seemingly unusual decoding order is selected so that if only SOE0 is asserted, the first megabyte is selected and if only SXNR is asserted, the second megabyte is selected. This maintains consistency with the 2-MByte configuration.

Video memory size is set upon power-up reset by strapping the PD[7:5] pins appropriately. See Section 12.2, Reset and Initialization, for the correct settings.

Figure 12-11 depicts a very high performance configuration supporting high-end video DACs capable of handling 64-bit pixel data input. Bit 6 of the Extended Memory Control 1 register (3?5H, Index 53H) is the enable for parallel VRAM addressing. Some video DACs may support this configuration with the addition of an external 2 to 1 multiplexer strobed by the SXNR signal.

VRAMs must be either 256Kx4, 256Kx8 or 256Kx16. DRAM can be substituted for VRAM for use as off-screen video memory.

The *86C928 Local Bus Interface Design Guide* provides the details of a 4-MByte serial addressing VRAM implementation. A Technical Note lists recommended VRAMs.

12.6 CLOCK SELECT

Four clock select signals are provided, which allow selection of up to 16 DCLK (dot clock) frequencies. The 86C928 drives these signals onto the PA[3:0] lines, which in turn connect to the clock select pins on the clock chip. The clock chip then latches these signals on the falling edge of STWR. If the clock chip does not have a strobe input or if strobing causes jitter, the clock select data should be read from the General Output Port (GOP) external buffer, bits [3:0]. This data is fed to the clock chip when the buffer is strobed by STWR. See Figure 12-14 for a diagram depicting use of the external GOP buffer to interface to the clock chip.

At power-on reset, PA[3:0] are all zeros and STWR is asserted to latch them into the clock chip. This selects a 25.175 MHz clock (VGA mode 0). If bit 5 of the Clocking Mode register (3C5H, Index 01H) is set to 1, the screen display is turned off (blanked) and STWR is asserted only when the Mode Control register (3?5H, Index 42H - also called CR42) bits [3:0] and the Miscellaneous Output register (3C2H) bits [3:2] are written into. The values of these bits determine the value automatically written into the General Output Port register (3?5H, Index 5CH) bits [3:0] and then driven onto the PA[3:0] lines to be latched by STWR. This is shown in Table 12-4 and the timing is shown in Figure 12-12.

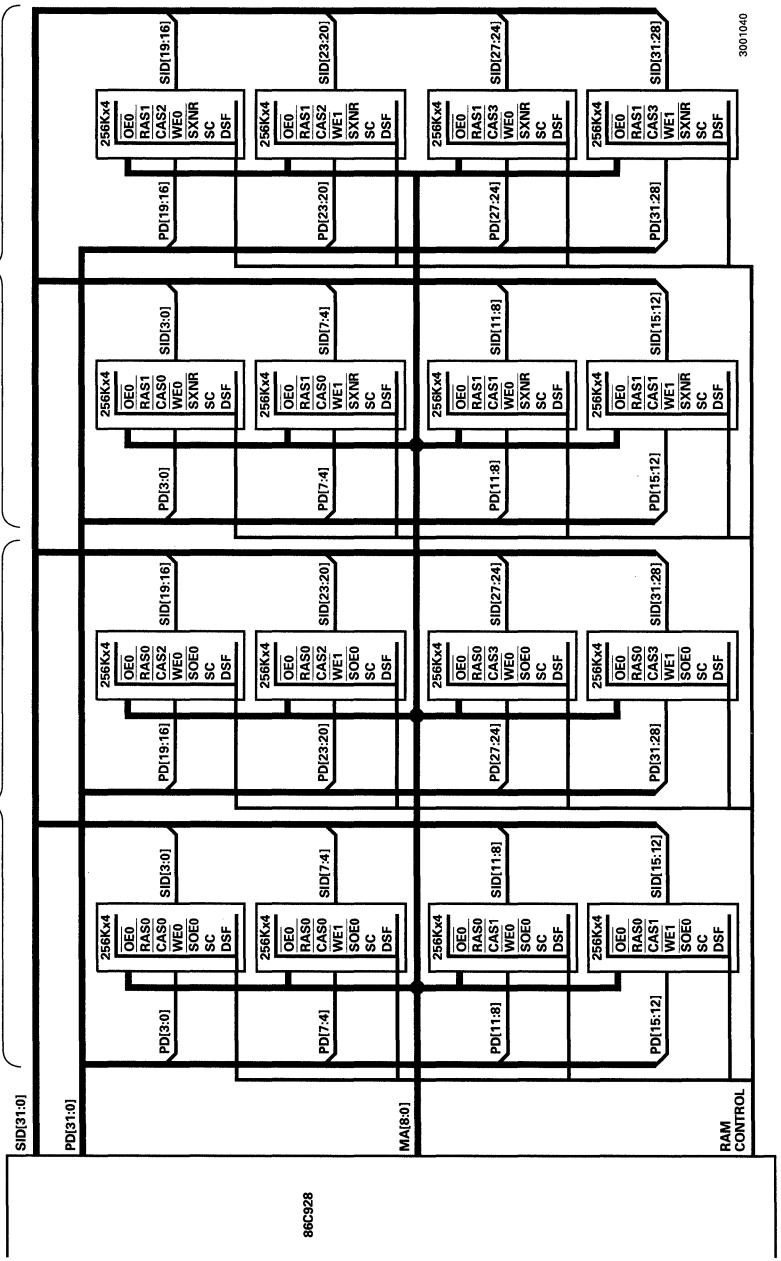

Figure 12-9. VRAM Interface (2MB, 256Kx4)

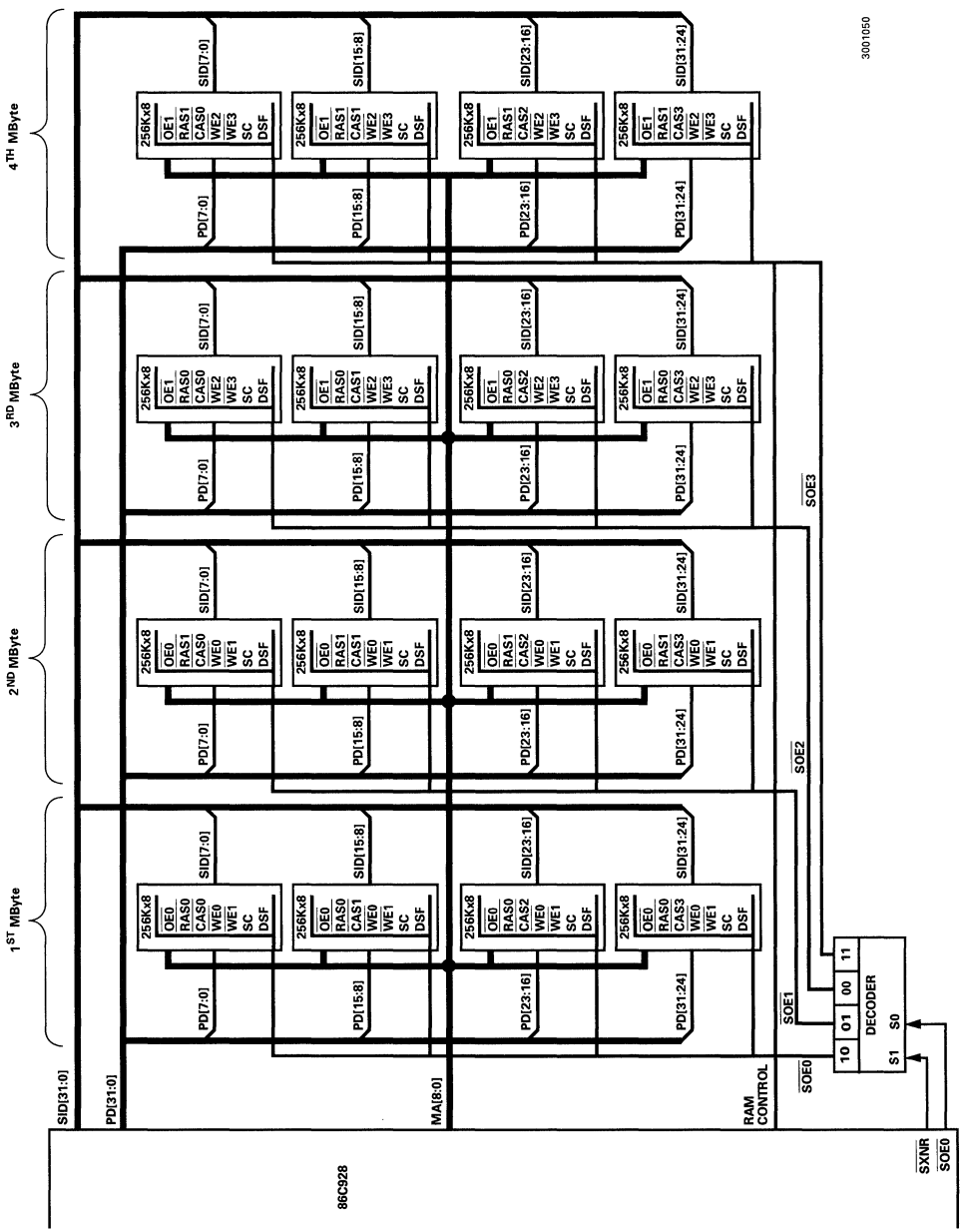

Figure 12-10. VRAM Interface (4MB, 256Kx8, Serial)

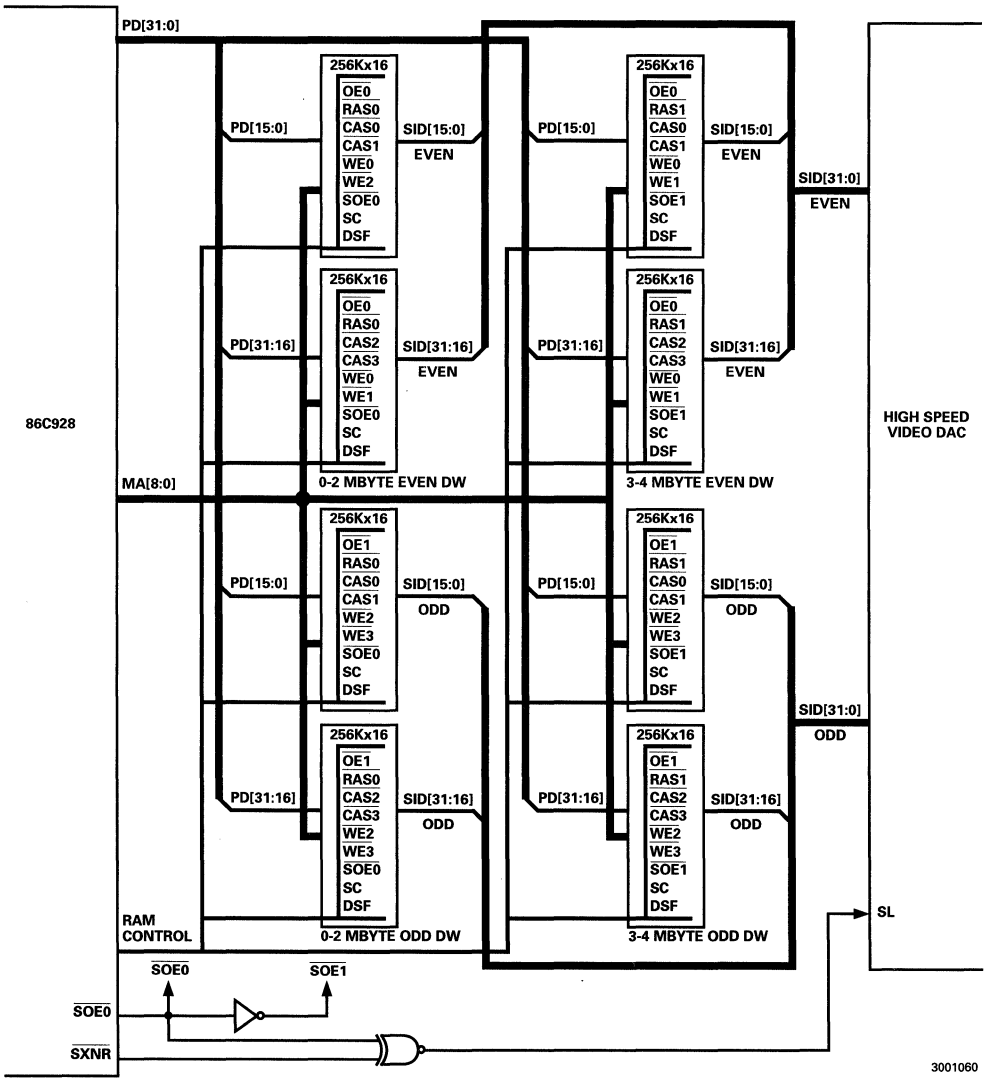

Figure 12-11. VRAM Interface (4MB, 256Kx16, Parallel)

Table 12-4. Dot Clock Select Values

3C2H, Bits [3:2]	PA[3:0]
00	0000
01	0001
10	0010
11	CR42, Bits [3:0]

The coding for these signals in this case is as shown in Table 12-5.

Table 12-5. Dot Clock Select Coding

PA[3:0] (HEX)	Freq (MHz)	Mode
0	25.175	VGA0
1	28.322	VGA1
2	40.000	VESA 800x600 @60Hz
3		Reserved
4	50.000	VESA 800x600 @72Hz 640x480x16bpp @ 60Hz
5	77.000	1024x768 @72Hz
6	36.000	VESA 800x600 @56Hz
7	44.889	1024x768 @43Hz - I
8		Reserved
9		Reserved
A	80.000	1280x1024 @46Hz - I
B	31.500	VESA 640x480 @72Hz
C	110.000	1280x1024 @60Hz
D	65.000	1024x768 @60Hz
E	75.000	1024x768 @70Hz 640x480x24bpp @ 60 Hz
F		Reserved

Note: In Table 12-5, I means interlaced. This table is an example, as the frequencies are dependent upon the clock synthesizer capabilites.See the *S3-Compatible Clock Generators* tech note.

If bit 5 of the Clocking Mode register (3C5H, Index 01H) is reset to 0, the screen display is turned on and STWR will be asserted once during every VSYNC interval as shown in Figure 12-13.

Having STWR asserted when the screen display is turned off is desirable because the clock chip only re-syncs its outputs when the latched PA[3:0] inputs have changed since the previous falling edge of STWR. This prevents screen jitter when the 86C928 selects the same clock value multiple times.

12.7 GENERAL I/O PORT

The 86C928 provides an 8-bit General Input Port and a 4-bit General Output Port. The block diagram showing how these are implemented is shown in Figure 12-14.

Bit 2 of the Extended DAC Control register (3?5H, Index 55H) and bit 1 of the System Configuration register (3?5H, Index 40H) are set to 1 to enable the General Input Port read function. The data to be read is held in an external buffer and is read via port 3C8H (the same as the DAC Write Index off-chip register). When STRD is asserted, this data is driven onto the SD[7:0] lines to the ISA/Local bus. The STRD assertion timing is identical to the DACRD timing.

The General Output Port register (3?5H, Index 5CH) bits [7:4] can be set to any value by a CPU write. The programmed values appear on PA[7:4] and are latched into the GOP external buffer whenever STWR is asserted. See Section 12.6 for a description of when STWR is asserted.

12.8 NTSC/PAL VIDEO INTERFACE

The 86C928 provides the capability to synchronize its video output with a remote video (NTSC, PAL or other PC video) signal. The first step is to enter remote mode by setting bit 0 of the External Sync Cont 1 (3?5H, Index 56H) register to 1. The VSYNC pin becomes an input to the 86C928. The falling edge of VSYNC resets the H/V counter to 0, corresponding to the top left corner of the display. The External Sync Cont 2 (3?5H, Index 57) is then programmed to match the falling edge of the VSYNC signal with the H/V counter reset. This technique works well with a remote video signal using the same dot clock oscillator as the 86C928.

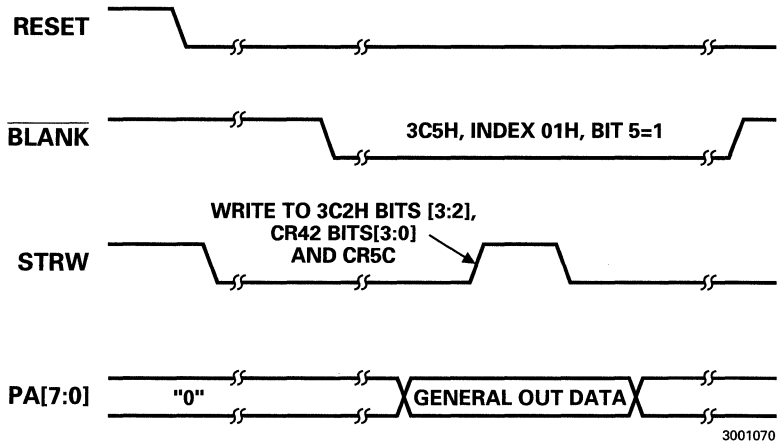

Figure 12-12. STWR Generation (Power On and Blanking)

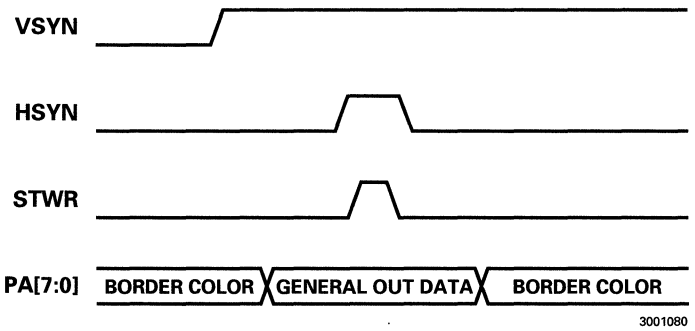

Figure 12-13. STWR Generation (Screen On)

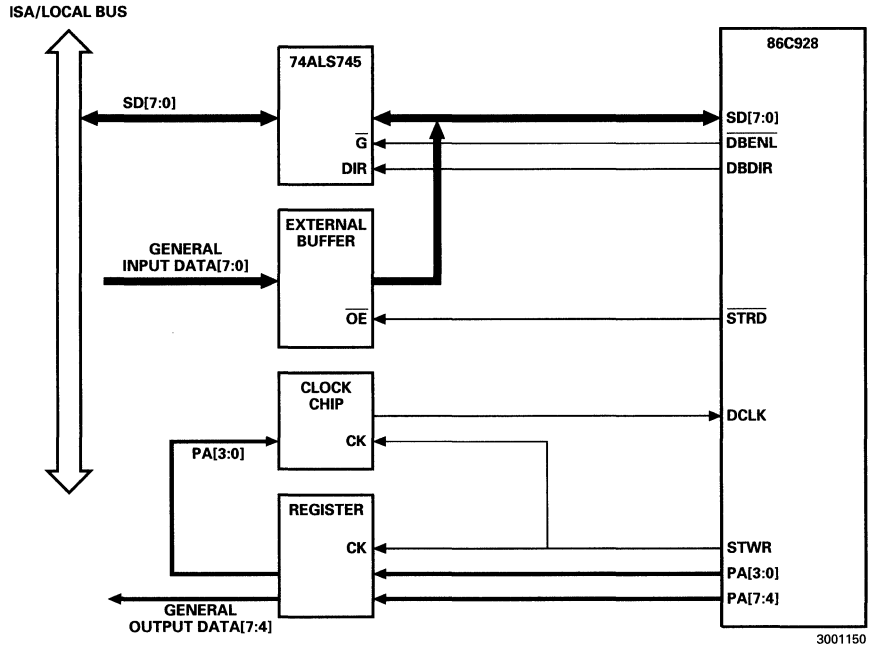

Figure 12-14. General I/O Port Configuration

12.9 CO-PROCESSOR INTERFACE

The 86C928 can share the pixel data bus and video memory with a co-processor. This function is enabled via bit 2 of the Extended System Cont 1 register (3?5H, Index 50H). The Bus Grant Termination Position register (3?5H, Index 5FH) and its extension bit (bit 7 of the Extended Horizontal Overflow egister (3?5H, Index 5DH) must be programmed with a value less than the horizontal scan period. Only between the start of the horizontal scan and this value can the 86C928 give up control of the pixel bus. This prevents conflict with 86C928 control fuctions such as VRAM refreshing that occur during the last part of the horizontal scan. The termination value programmed depends on how fast the co-processor can give up the bus. The greater the time this might take, the earlier in the horizontal scan the termination position must be.

The co-processor asserts the $\overline{\text{BREQ}}$ signal to the 86C928 to request the bus. If the bus grant termination position value has not been exceeded, the 86C928 grants control of the pixel bus to the co-processor by asserting $\overline{\text{BGNT}}$. At the terminal position, the 86C928 raises $\overline{\text{BGNT}}$ high. The co-processor must then raise $\overline{\text{BREQ}}$ high and give up the bus. The co-processor can then re-assert $\overline{\text{BREQ}}$ at any time. The termination position parameter is ignored in two cases. One is when bit 7 (Serial Out Tri-State Enable) of the Backward Compatibility 1 register (3?5H, Index 32H) is set to 1, such as when another processor is controlling video screen updating. The other is when bits [1:0] (the Alternate Refresh Count Control) of the Miscellaneous 1 register (3?5H, Index 3AH) are programmed to 00b, which means refresh interference is not a problem.

12.10 MULTIPLEXED PINS

Four pins on the 86C928 serve multiple purposes. Table 12-6 shows the register bit settings required to activate a particular function on each of these pins. In addition, the hardware must be designed to provide the desired signals. See the *86C928 Local Bus Interface Design Guide* and its accompanying schematic diagrams for an example of the required design.

Table 12-6. Bit Settings for Multiplexed Pins

Pin 90	Pin 85	Pin 86	Pin 87
SENS CR55, bit 5 = 0	MID2 CR55, bit 5 = 0	MID1 CR40, bit 1 = 0	MID0 CR40, bit 1 = 0
HC1 CR55, bit 5 = 1 CR45, bit 5 = 0	HC0 CR55, bit 5 = 1 CR45, bit 5 = 0	$\overline{\text{BREQ}}$ CR40, bit 1 = 1 CR50, bit 2 = 1	$\overline{\text{BGNT}}$ CR40, bit 1 = 1 CR55, bit 2 = 0 CR50, bit 2 = 1
ODF CR55, bit 5 = 1 CR45, bit 5 = 1	CDE CR55, bit 5 = 1 CR45, bit 5 = 1		$\overline{\text{STRD}}$ CR40, bit 1 = 1 CR55, bit 2 = 1

Section 13: Electrical Data

13.1 MAXIMUM RATINGS

Table 13-1. Absolute Maximum Ratings

Ambient temperature	0° C to 70° C
Storage temperature	-40° C to 125° C
DC Supply Voltage	-0.5V to 7.0V
I/O Pin Voltage with respect to VSS	-0.5V to VDD+0.5V

13.2 DC SPECIFICATIONS

Table 13-2. DC Specifications (VDD = 5V ± 5%)

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage		0.8	V
V_{IH}	Input High Voltage	2.0		V
V_{OL}	Output Low Voltage		V_{SS} + 0.4	V
V_{OH}	Output High Voltage	V_{DD} - 0.4		V
I_{OL1}	Output Low Current	4 (Note 1)		mA
I_{OH1}	Output High Current	-2		mA
I_{OL2}	Output Low Current	8 (Note 2)		mA
I_{OH2}	Output High Current	-4		mA
I_{OL3}	Output Low Current	24 (Note 3)		mA
I_{OH3}	Output High Current	-12		mA
I_{OZ}	Output Tri-state Current		1	µA
C_{IN}	Input Capacitance		5	pF
C_{OUT}	Output Capacitance		5	pF
I_{CC}	Power Supply Current	TBD		mA

Notes for Table 13-2

1. I_{OL1}, I_{OH1} for pins SD[15:0], $\overline{\text{DBENL}}$, SINTR, $\overline{\text{ROMCS}}$, HC[1:0], $\overline{\text{STRD}}$, $\overline{\text{STWR}}$, $\overline{\text{DACRD}}$, $\overline{\text{DACWR}}$, VSYNC, HSYNC, BLANK, PA[7:0], PD[31:0], MA[8:0], CAS[3:0], WE[3:0]

2. I_{OL2}, I_{OH2} for pins SD31, SD[28:16], $\overline{\text{DBENH}}$, DBDIR, $\overline{\text{SOE0}}$, $\overline{\text{SXNR}}$, DSF, SC, VCLK, $\overline{\text{RAS[1:0]}}$, $\overline{\text{OE[1:0]}}$
3. I_{OL3}, I_{OH3} for pins SD[30:29], $\overline{\text{LOCA}}$, $\overline{\text{SRDY}}$,

13.3 AC SPECIFICATIONS

Note: All timing units are in nanoseconds unless otherwise stated.

Table 13-3. Test Loads for AC Timing

Pin Name	Capacitive Load
SD[30:29] (ISA), $\overline{\text{SRDY}}$ (ISA), $\overline{\text{LOCA}}$ (ISA)	240pf
SD[31, 28:16] (ISA), SINTR, DSF, $\overline{\text{SRDY}}$ (Local Bus)	120pf
MA[8:0]	100pf
$\overline{\text{RAS[1:0]}}$, $\overline{\text{OE[1:0]}}$, SC	80pf
DBDIR	60pf
SD[31:0] (Local Bus), SD[15:0] (ISA), $\overline{\text{DBENH}}$, $\overline{\text{ROMCS}}$, HC[1:0], $\overline{\text{DACRD}}$, $\overline{\text{DACWR}}$, STWR, HSYNC, $\overline{\text{LOCA}}$ (Local Bus)	50pf
$\overline{\text{WE[3:0]}}$	40pf
$\overline{\text{DBENL}}$, $\overline{\text{BLANK}}$, VSYNC, PA[7:0], VCLK, PD[31:0]	30pf
$\overline{\text{CAS[3:0]}}$	25pf

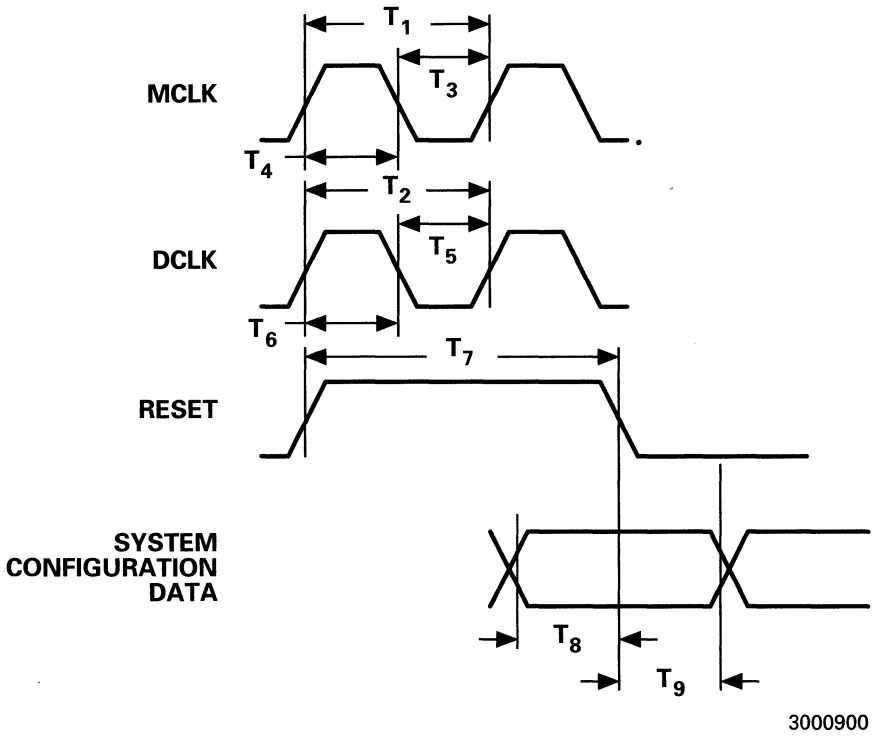

Figure 13-1. Clock And Reset Cycles

Table 13-4. Clock and Reset Timing

Symbol	Parameter	Min	Max
T_1	MCLK Period	20	
T_2	DCLK Period	9	
T_3	MCLK Low Time	8	
T_4	MCLK High Time	8	
T_5	DCLK Low Time	3	
T_6	DCLK High Time	3	
T_7	Reset High Time	400	
T_8	System Configuration Data Setup Time	20	
T_9	System Configuration Data Hold Time	10	

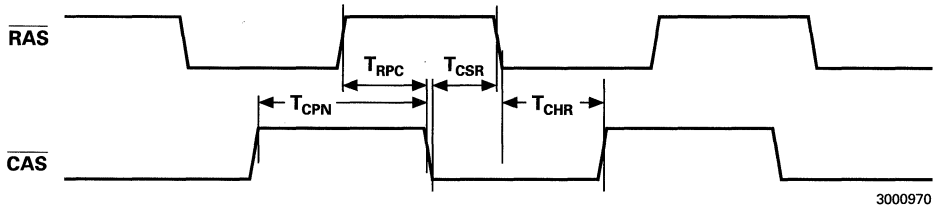

Figure 13-2. CAS Before RAS Refresh Cycle

Table 13-5. CAS Before RAS Refresh Cycle Timing

Sym.	Parameter	T-Value		MCLK 45MHz		MCLK 50MHz	
		Min	Max	Min	Max	Min	Max
TCPN	$\overline{CAS}$ Precharge Time	1		22		20	
TRPC	$\overline{RAS}$ High to $\overline{CAS}$ Low Precharge Time	1		22		20	
TCSR	$\overline{CAS}$ Before $\overline{RAS}$ Setup Time	1.5		33		30	
TCHR	$\overline{CAS}$ Before $\overline{RAS}$ Hold Time	3.5		77		70	

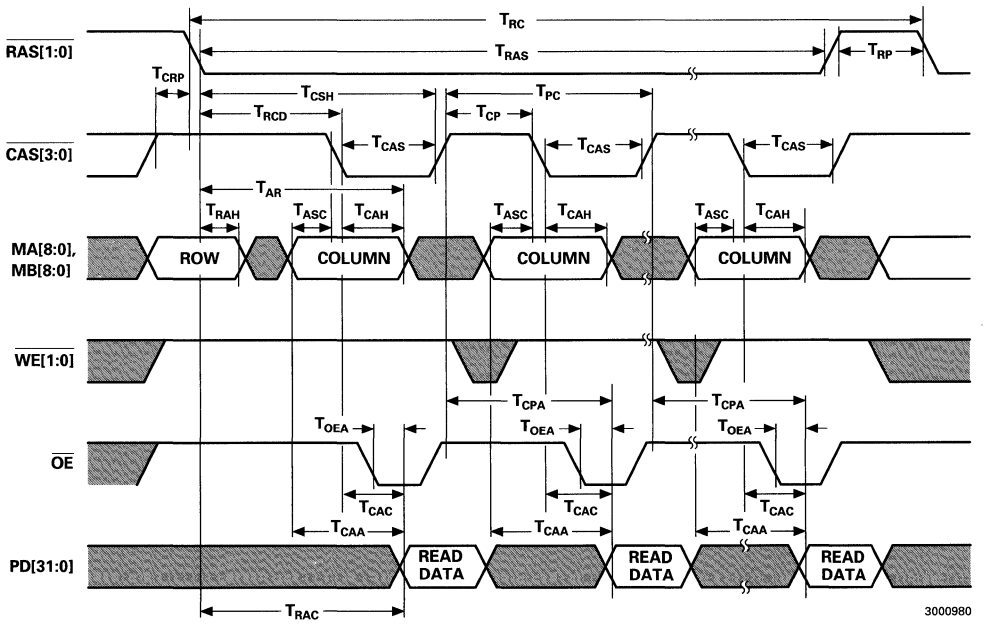

Figure 13-3. Video Memory Fast Page Mode Read Cycle

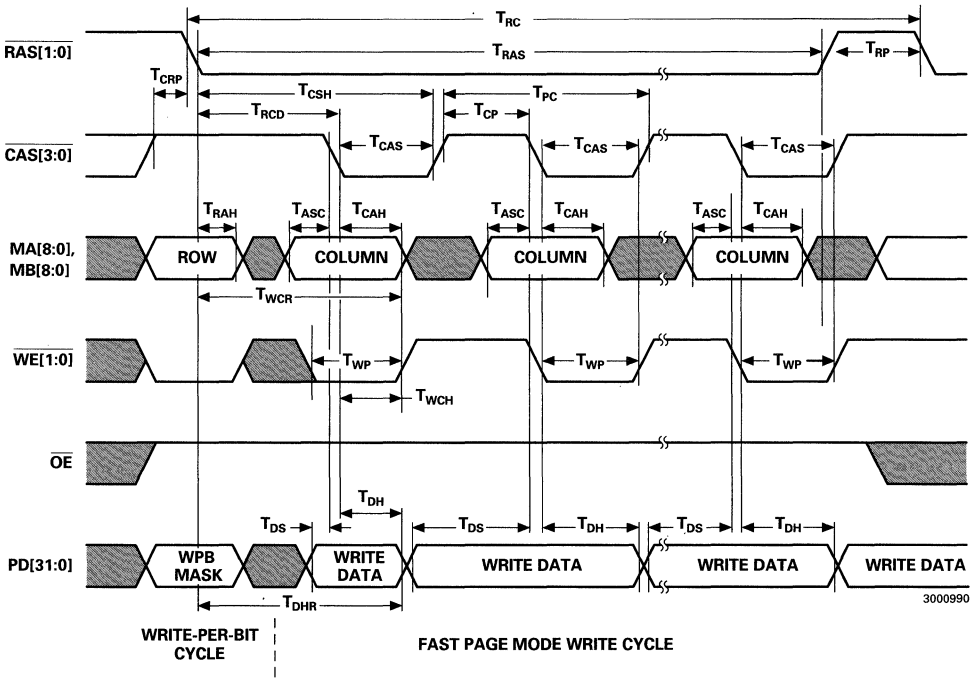

Figure 13-4. Video Memory Fast Page Mode Write Cycle

Table 13-6. Video Memory Fast Page Mode Read/Write Cycle Timing

Guaranteed Timings							
		T-Value		MCLK 45MHz		MCLK 50MHz	
Sym.	Parameter	Min	Max	Min	Max	Min	Max
TCAS	$\overline{CAS}$ Pulse Width	1		22		20	
TCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	1.5		33		30	
TCSH	$\overline{CAS}$ Hold Time	3.5		77		70	
TPC	CAS Cycle Time	2		45		40	
TCP	$\overline{CAS}$ Precharge Time	1		22		20	
TRP	$\overline{RAS}$ Precharge Time	2.5		55		50	
TRC	$\overline{RAS}$ Cycle Time	6,7		133,154		120,140	
TRAS	$\overline{RAS}$ Pulse Width	3.5		77		70	
TRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	2.5		55		50	
TRAH	Row Address Hold Time	1.5		33		30	
TAR	Column Address Hold From $\overline{RAS}$	3.5		77		70	
TASC	Column Address Setup Time	1		22		20	
TCAH	Column Address Hold Time	1		22		20	
TWCH	Write Command Hold Time	1		22		20	
TWCR	Write Command Hold Referenced to $\overline{RAS}$	3.5		77		70	
TWP	Write Command Pulse Width	1		22		20	
TDS	Data-in Setup Time	1		0		0	
TDH	Data-in Hold Time	1		22		20	
TDHR	Data Hold Referenced to $\overline{RAS}$	3.5		77		70	
Required Timings							
		T-Value		MCLK 45MHz		MCLK 50MHz	
Sym.	Parameter	Min	Max	Min	Max	Min	Max
TCPA	Data Access Time from $\overline{CAS}$ Precharge		2		44		40
TRAC	Data Access Time From $\overline{RAS}$		3.5		77		70
TCAC	Data Access Time from $\overline{CAS}$		1		22		20
TOEA	Data Access Time From $\overline{OE}$		1		22		20
TCAA	Data Access Time From Column Address		2		44		40

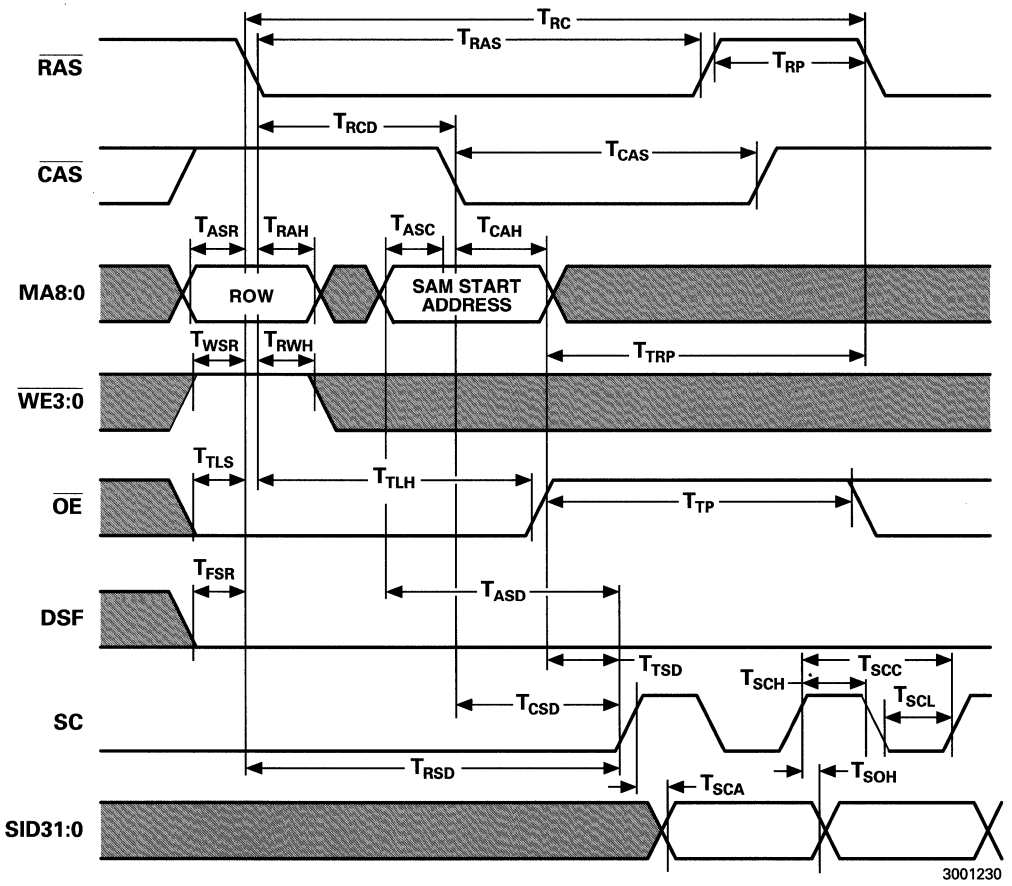

Figure 13-5. Read Transfer and Serial Output Cycle

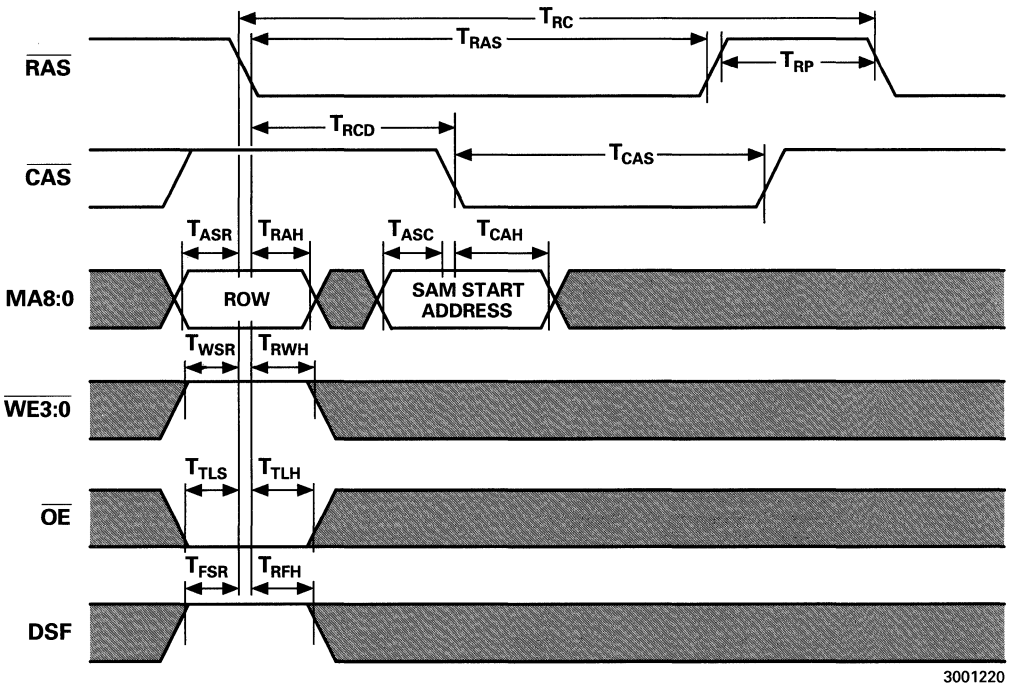

Figure 13-6. Split Read Transfer Cycle

Table 13-7. Read Transfer and Split Read Transfer Cycle Timing

Sym.	Parameter	Minimum T-Value (DCLKs)	
		6 Cycle $\overline{RAS}$	7 Cycle $\overline{RAS}$
TRP	$\overline{RAS}$ Precharge Time	2.5	3
TRAS	$\overline{RAS}$ Pulse Width	3.5	4
TTLS	$\overline{OE}$ High to $\overline{RAS}$ Setup	1	1
TTLH	$\overline{OE}$ High to $\overline{RAS}$ Hold	3	4
TFSR	DSF Setup to $\overline{RAS}$	1	1
TRFH	DSF Hold from $\overline{RAS}$	3	4
TWSR	Write Per Bit Setup	1	1
TRWH	Write Per Bit Hold	3	4
TRCD	$\overline{RAS}$ Low to $\overline{CAS}$ Low	2.5	3
TRC	Random Read/Write Cycle Time	6	7
TASR	Row Address Setup	1	1
TRAH	Row Address Hold	1.5	1.5
TASC	Column Address Setup	1	1
TCAH	Column Address Hold	1	1
TASD	Column Address to First SC Delay Time	4	4
TCSD	$\overline{CAS}$ to First SC Delay	2	2
TTSD	First SC Edge to $\overline{OE}$ Delay	2	2
TRSD	$\overline{RAS}$ to First SC Delay Time	9	9
TTRP	$\overline{OE}$ to $\overline{RAS}$ Precharge Time	3	2
TTP	$\overline{OE}$ Precharge Time	2	2

Table 13-8. Serial Output Cycle Timing

Sym.	Parameter	Value	
		Mininum	Unit
TSCH	SC High Time	1	DCLK
TSCC	SC Cycle Time	2	DCLK
TSCL	SC Low Time	1	DCLK
TSCA	Access Time from SC	25	ns
TSOH	Serial Output Hold from SC	5	ns

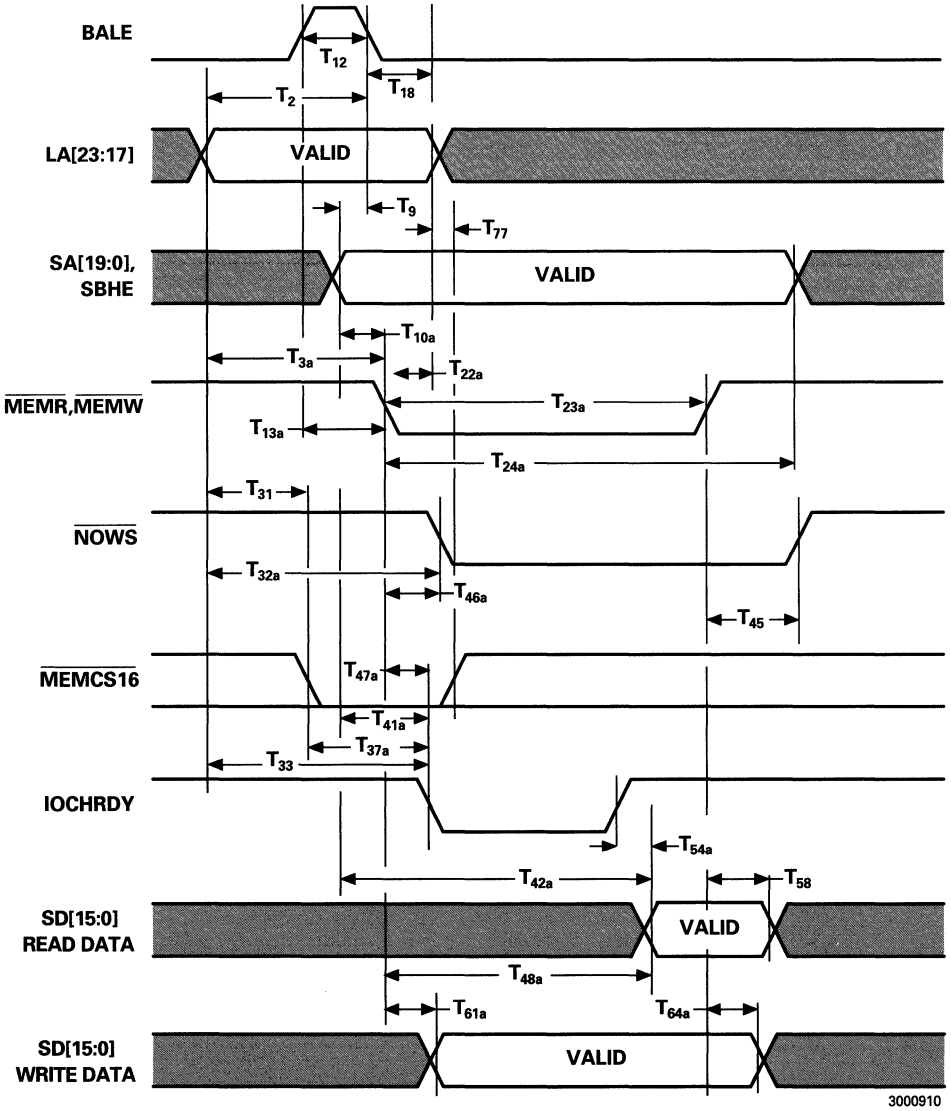

Figure 13-7. ISA Memory Read/Write Cycles

Table 13-9. ISA Memory Read/Write Cycles Timing

Symbol	Parameter	Req/ Guar	Min	Max	Notes
T_2	LA Valid before BALE Low	Req	77		Req = required for input
T_{3a}	LA Valid before $\overline{MEMR}$, $\overline{MEMW}$ Low	Req	79		
T_9	SA, $\overline{SBHE}$ Valid Before BALE Low	Req	19		
T_{10a}	SA, $\overline{SBHE}$ Valid Before $\overline{MEMR}$, $\overline{MEMW}$ Low	Req	21		
T_{12}	BALE High	Req	25		
T_{13a}	BALE High Before $\overline{MEMR}$, $\overline{MEMW}$ Low	Req	27		
T_{18}	BALE Low Before LA Invalid	Req	32		
T_{22a}	$\overline{MEMR}$, $\overline{MEMW}$ Low Before LA Invalid	Req	30		
T_{23a}	$\overline{MEMR}$, $\overline{MEMW}$ Low	Req	86		For 3 BCLK cycle, T_{23b} >150
T_{24a}	$\overline{MEMR}$, $\overline{MEMW}$ Low Before SA, $\overline{SBHE}$ valid	Req	99		For 3 BCLK cycle, T_{24b} >158
T_{31}	LA Valid to $\overline{MEMCS16}$ Low	Guar		22	Guar = guaranteed output
T_{32a}	LA Valid to $\overline{NOWS}$ Low	Guar	95		
T_{33}	LA Valid to IOCHRDY Low	Guar		99	
T_{37a}	BALE High to IOCHRDY Low	Guar		47	
T_{41a}	SA, $\overline{SBHE}$ Valid to IOCHRDY Low	Guar		40	
T_{42a}	SA, $\overline{SBHE}$ Valid to Read Data Valid	Guar		65	For 3 BCLK cycle, T_{42b} <350
T_{45}	$\overline{MEMR}$, $\overline{MEMW}$ High to $\overline{NOWS}$ Floated	Guar		22	
T_{46a}	$\overline{MEMR}$, $\overline{MEMW}$ Low to $\overline{NOWS}$ Low	Guar		18	
T_{47a}	$\overline{MEMR}$, $\overline{MEMW}$ Low to IOCHRDY Low	Guar		21	
T_{48a}	$\overline{MEMR}$ Low to Read Data Valid	Guar		45	For 3 BCLK cycle, T_{48b} <330
T_{54a}	IOCHRDY High to Read Data Valid	Guar		0	
T_{58}	$\overline{MEMR}$, $\overline{IOR}$ High to Read Data Invalid	Guar	14		
T_{61a}	$\overline{MEMW}$ Low to Write Data Valid	Req		25	
T_{64a}	$\overline{MEMW}$ High to Write Data Invalid	Req	16		
T_{77}	LA Invalid to $\overline{MEMCS16}$ Invalid	Guar	15		

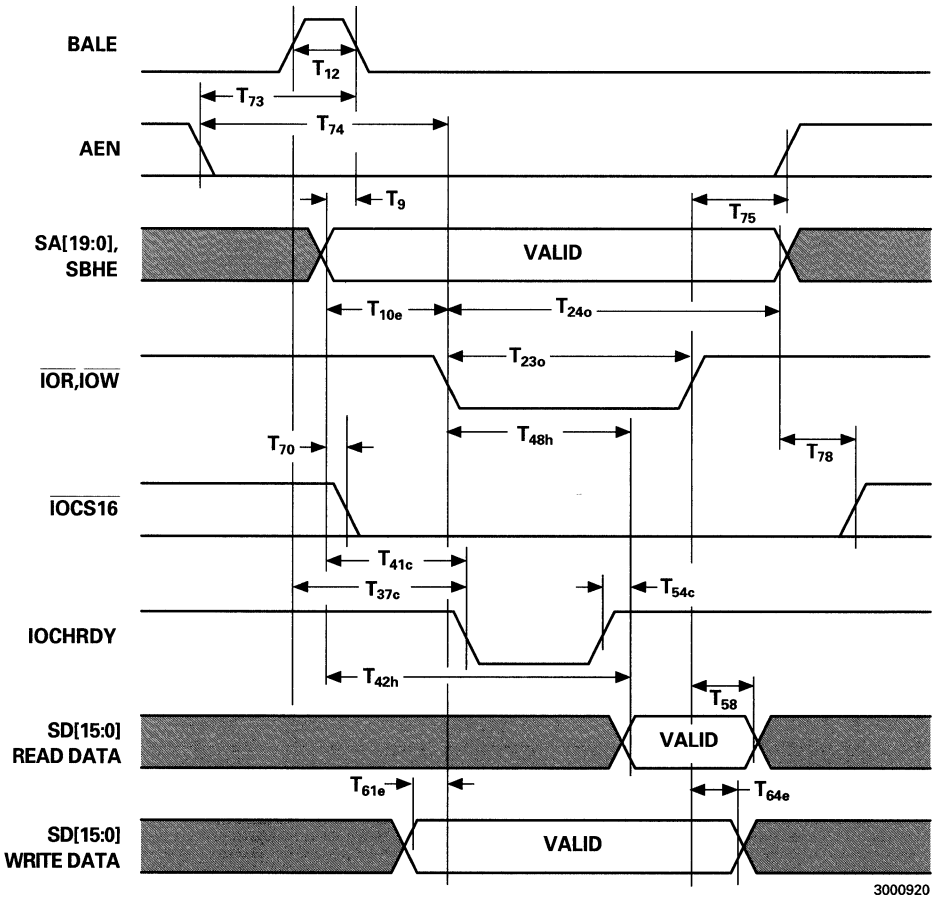

Figure 13-8. ISA I/O Read/Write Cycles

Table 13-10. ISA I/O Read/Write Cycles Timing

Symbol	Parameter	Req Guar	Min	Max	Notes
T_9	SA, $\overline{SBHE}$ Valid Before BALE Low	Req	19		Req = required for input
T_{10e}	SA, $\overline{SBHE}$ Valid before $\overline{IOR}$, $\overline{IOW}$ Low	Req	63		
T_{12}	BALE High	Req	25		
T_{23o}	$\overline{IOR}$, $\overline{IOW}$ Low	Req	106		
T_{24o}	$\overline{IOR}$, $\overline{IOW}$ Low Before SA, $\overline{SBHE}$ Invalid	Req	114		
T_{37c}	BALE High to IOCHRDY Low	Guar		99	Guar = guaranteed output
T_{41c}	SA, $\overline{SBHE}$ Valid to IOCHRDY Low	Guar		94	
T_{42h}	SA, $\overline{SBHE}$ Valid to Read Data Valid	Guar		240	
T_{48h}	$\overline{IOR}$ Low to Read Data Valid	Guar		230	
T_{54c}	IOCHRDY High to Read Data Valid	Guar		205	
T_{58}	$\overline{IOR}$ High to Read Data Invalid	Guar	10		
T_{61e}	$\overline{IOW}$ Low to Write Data Valid	Guar		25	
T_{64e}	$\overline{IOW}$ High to Write Data Invalid	Req	14		
T_{70}	SA, $\overline{SBHE}$ Valid before $\overline{IOCS16}$ Low	Guar		25	
T_{73}	AEN Valid Before BALE Low	Req	75		
T_{74}	AEN Valid Before $\overline{IOR}$, $\overline{IOW}$ Low	Req	122		
T_{75}	$\overline{IOR}$, $\overline{IOW}$ High Before AEN High	Req	8		
T_{78}	SA Invalid to $\overline{IOCS16}$ Invalid	Guar	21		

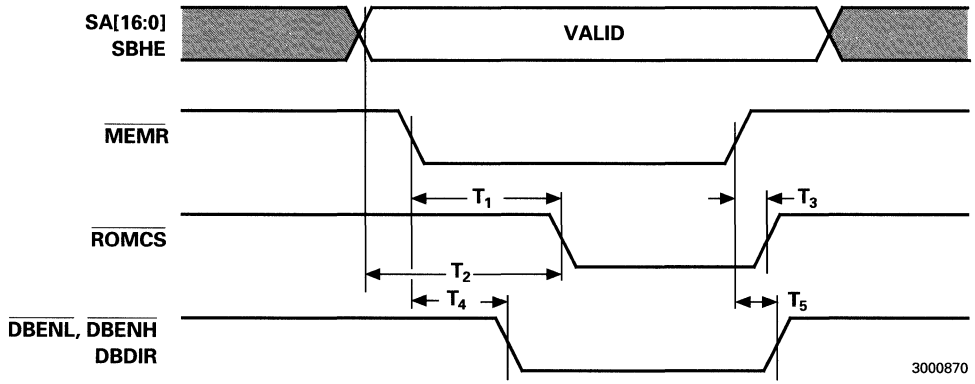

Figure 13-9. ISA BIOS Read Cycle

Table 13-11. ISA BIOS Read Cycle Timing

Symbol	Parameter	Min	Max
T_1	$\overline{\text{MEMR}}$ Low to $\overline{\text{ROMCS}}$ Low		36
T_2	SA[16:0] , $\overline{\text{SBHE}}$ Valid to $\overline{\text{ROMCS}}$ Low		54
T_3	$\overline{\text{MEMR}}$ High to $\overline{\text{ROMCS}}$ High	10	
T_4	$\overline{\text{MEMR}}$ Low to Data Buffer Enable Low		25
T_5	$\overline{\text{MEMR}}$ High to Data Buffer Enable High		25

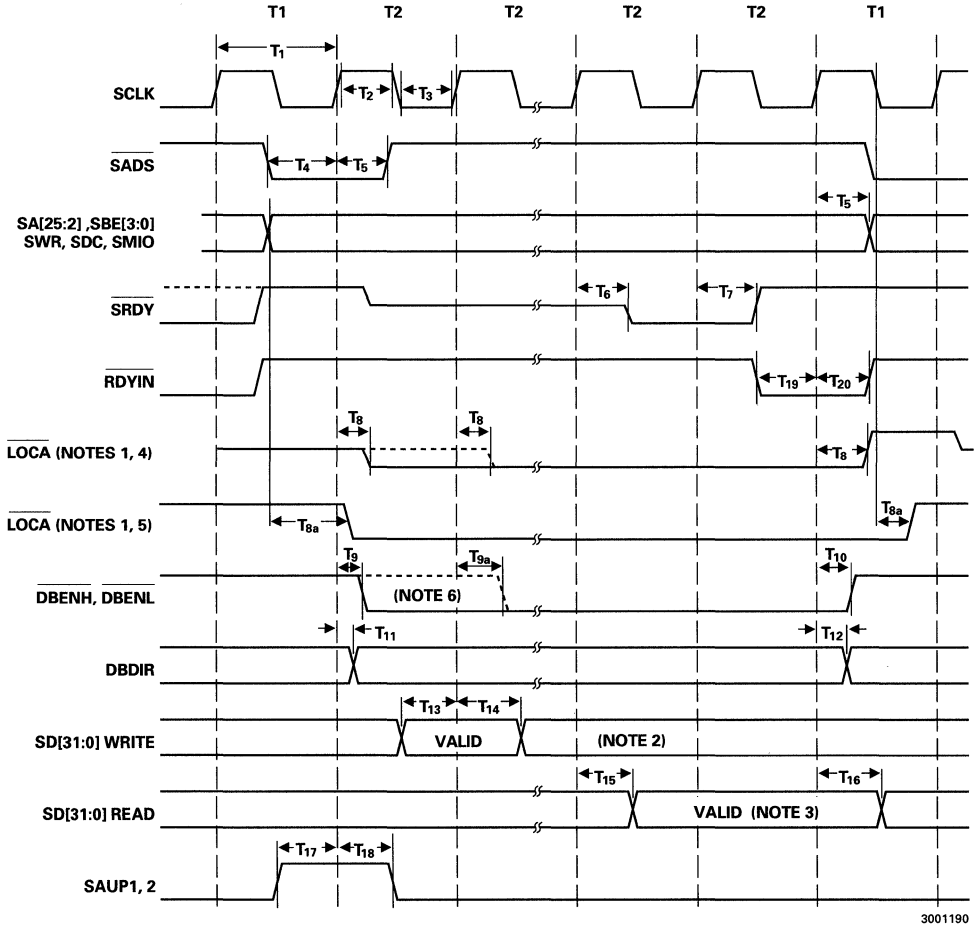

Figure 13-10. Local Bus AC Cycles

Notes for Figure 13-10

1. $\overline{\text{LOCA}}$ will be generated according to one of two waveforms selected through bit 11 of the power-on strapping pins. If bit 11 is strapped high, $\overline{\text{LOCA}}$ is tri-state until driven low after a period specified by the setting of "Decode Wait Control" (bits 5-4) of the System Configuration register (3?5H, Index 40). It is held low until $\overline{\text{SRDY}}$ is asserted, driven high for one clock, and then tri-stated. If bit 11 is strapped low, $\overline{\text{LOCA}}$ is never tri-stated and is held low as long as SA[19:0] and the control signals are valid.
2. Write data is latched into the 86C928 at the beginning of the first T2 cycle.
3. Read data is valid before the end of the T2 cycle indicated by $\overline{\text{SRDY}}$ until after the last T2 cycle (indicated by RDYIN).
4. The T-state in which $\overline{\text{LOCA}}$ goes active depends on the setting of "Decode Wait Control" (bits 5-4) of the System Configuration register (3?5H, Index 40). If these bits are programmed to a value of 00, then tri-state $\overline{\text{LOCA}}$ will be active in the first T2 cycle. If these bits are programmed to 01, then tri-state $\overline{\text{LOCA}}$ will be active in the second T2 cycle.
5. Parameter T_{8a} is measured from the latest of: $\overline{\text{SADS}}$ leading edge, SCLK going low, or address/status/SAUP[1:2] active for an 86C928 cycle.
6. The T-state in which $\overline{\text{DBENL/H}}$ goes active during read operations depends on the setting of "Decode Wait Control" (bits 5-4) of the System Configuration register (3?5H, Index 40). If these bits are programmed to a value of 00, then $\overline{\text{DBENL/H}}$ will go active in the first T2 cycle. If these bits are programmed to 01, then $\overline{\text{DBENL/H}}$ will go active in the second T2 cycle.

Table 13-12. Local Bus AC Cycles Timing

Symbol	Parameter	Req Guar	Min	Max	Notes
T_1	SCLK Period	Req	30/20*		Req = required for input
T_2	SCLK High Time	Req	11/7*		Measured at 2.0V
T_3	SCLK Low Time	Req	11/7*		Measured at 0.8V
T_4	SA, $\overline{SBE}$, $\overline{SWR}$, SDC, SMIO, $\overline{SADS}$ Setup	Req	8		
T_5	SA, $\overline{SBE}$, $\overline{SWR}$, SDC, SMIO, $\overline{SADS}$ Hold	Req	3		
T_6	$\overline{SRDY}$ Delay	Guar		15	Guar = guaranteed output
T_7	$\overline{SRDY}$ Hold	Guar	4		
T_8	$\overline{LOCA}$ Active Delay (Tri-state)	Guar		16	Tri-state $\overline{LOCA}$ selection
T_{8a}	$\overline{LOCA}$ Active Delay (Level)	Guar		20	Level $\overline{LOCA}$ selection
T_9	Data Buffer Enable Delay (Write Cycle)	Guar		15	Write cycle
T_{9a}	Data Buffer Enable Delay (Read Cycle)	Guar		20	Read cycle
T_{10}	Data Buffer Enable Hold	Guar	4	15	
T_{11}	Data Buffer Direction Delay	Guar		15	
T_{12}	Data Buffer Direction Hold	Guar	4		
T_{13}	Write Data Setup	Req	4		
T_{14}	Write Data Hold	Req	0		
T_{15}	Read Data Valid After Beginning of SRDY T-state	Guar		12	
T_{16}	Read Data Hold After end of $\overline{RDYIN}$ T-state	Guar	5	15	
T_{17}	SAUP1, SAUP2 Setup	Req	5		
T_{18}	SAUP1, SAUP2 Hold	Req	5		
T_{19}	$\overline{RDYIN}$ Setup	Req	7		
T_{20}	$\overline{RDYIN}$ Hold	Req	3		

* 33 MHz/50 MHz CPU clock speed

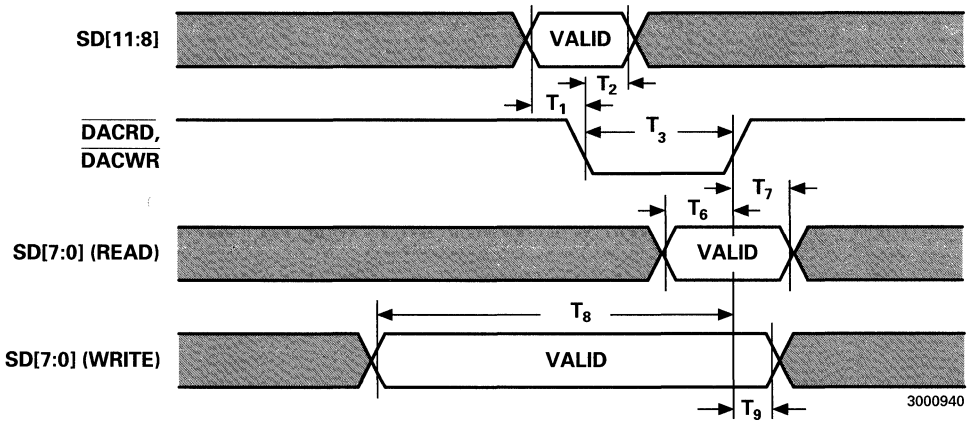

Figure 13-11. Video DAC Read/Write AC Cycles

Table 13-13. Video DAC AC Cycles Timing

Symbol	Parameter	Min	Unit
T_1	SD[10:8] Setup to $\overline{\text{DACRD}}$, $\overline{\text{DACWR}}$ Low	2	MCLK
T_2	SD[10:8] Hold from $\overline{\text{DACRD}}$, $\overline{\text{DACWR}}$ Low	2	MCLK
T_3	$\overline{\text{DACRD}}$, $\overline{\text{DACWR}}$ Low Time	4	MCLK
T_6	Read Data Valid Setup to $\overline{\text{DACRD}}$ High	2	MCLK
T_7	Read Data Valid Hold to $\overline{\text{DACRD}}$ High	2	MCLK
T_8	Write Data Valid Setup to $\overline{\text{DACWR}}$ High	2	MCLK
T_9	Write Data Valid Hold to $\overline{\text{DACWR}}$ High	2	MCLK

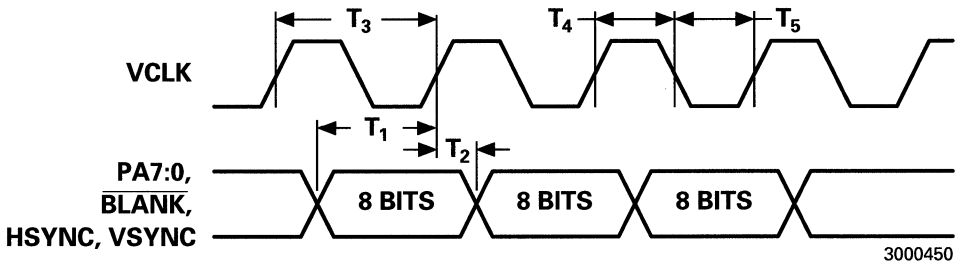

Figure 13-12. Video Timing - 4, 8, 24 Bits/Pixel Modes

Table 13-14. 4, 8 and 24 BPP Video AC Timing

Symbol	Parameter	Min	Unit
T_1	P[7:0], $\overline{\text{BLANK}}$, SYNC Setup Time	3	ns
T_2	PA[7:0], $\overline{\text{BLANK}}$, SYNC Hold Time	3	ns
T_3	VCLK Period	13.3	ns
T_4	VCLK High Time	5	ns
T_5	VCLK Low Time	5	ns

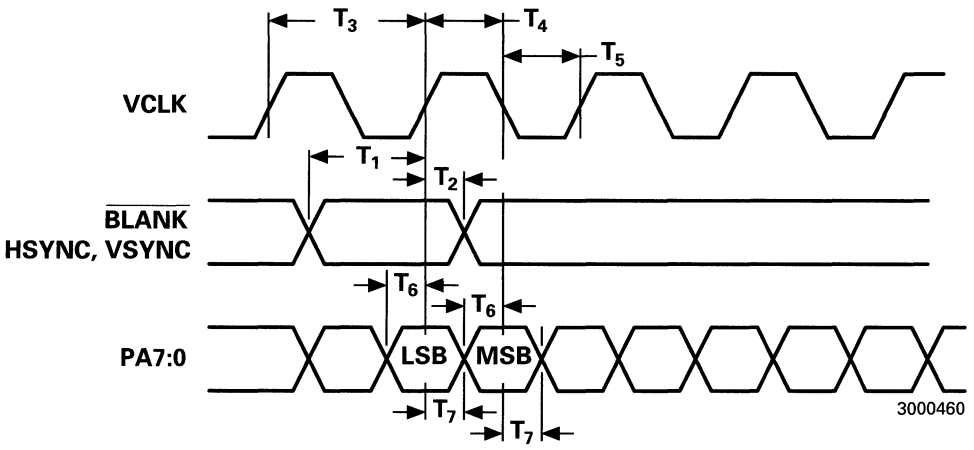

Figure 13-13. Video Timing - 16 Bits/Pixel Mode

Table 13-15. 16 BPP Video AC Timing

Symbol	Parameter	Min	Unit
T_1	$\overline{\text{BLANK}}$, SYNC Setup Time	3	ns
T_2	$\overline{\text{BLANK}}$, SYNC Hold Time	3	ns
T_3	VCLK Period	20	ns
T_4	VCLK High Time	8	ns
T_5	VCLK Low Time	8	ns
T_6	PA[7:0] Setup Time	1	ns
T_7	PA[7:0] Hold Time	7	ns

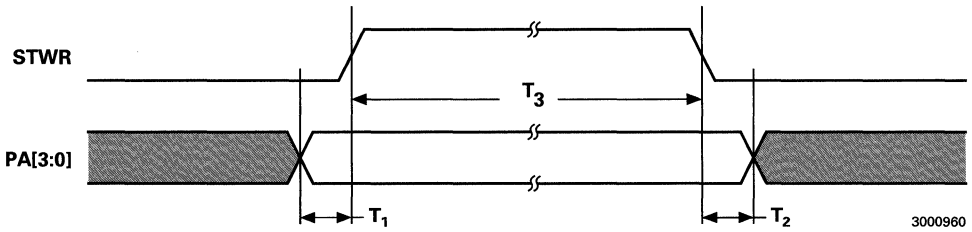

Figure 13-14. Clock Select Cycle

Table 13-16. Clock Select Cycle Timing

Symbol	Parameter	Min	Unit	Notes
T_1	Clock Select Lines Set-up Time	10	ns	
T_2	Clock Select Lines Hold Time	10	ns	
T_3	STWR Pulse Width	3	DCLK	For display off; if display is on, the minimum pulse width is 8 DCLKs.

Section 14: Mechanical Data

14.1 MECHANICAL DIMENSIONS

The mechanical dimensions for the 86C928 are given in Figure14-1.

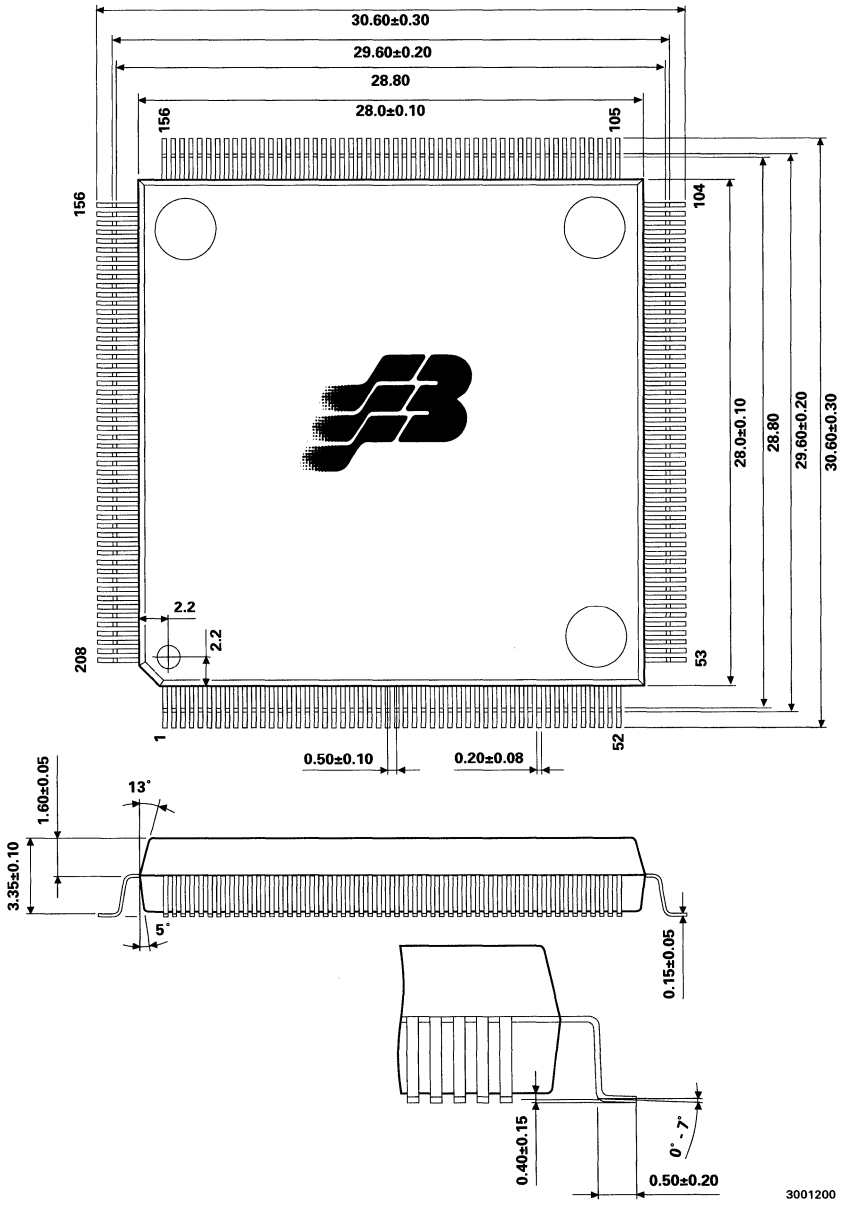

Figure 14-1. 86C928 Mechanical Dimensions

Appendix A: Register Reference

This Appendix contains tables listing all the registers in each of categories corresponding to Sections 4-10 of this data book.

- CGA-Compatible
- MDA- and HGC- Compatible
- VGA
- S3 VGA
- System Control
- System Extension
- Enhanced Commands

Within each table, registers are listed in order of increasing addresses/indices. Name, mnemonic, address, read/write status and page number of detailed description are provided for each register. All addresses and indices are hexadecimal values.

A.1 CGA-COMPATIBLE REGISTERS

Table A-1. CGA-Compatible Registers

I/O Address	Index	R/W	Name	Mnemonic	Description Page
3D5	10	R	Light Pen High	LPENH	4-1
3D5	11	R	Light Pen Low	LPENL	4-1
3D8	–	R/W	CGA Mode Control	CGA_MODE	4-2
3D9	–	R/W	CGA Color Select	CGA_COLOR	4-3
3DA	–	R	CGA Status	CGA_STAT	4-4
3DB	–	W	Reset Light Pen Flag	CLPEN	4-5
3DC	–	W	Set Light Pen Flag	SLPEN	4-5

A.2 MDA- AND HGC-COMPATIBLE REGISTERS

Table A-2. MDA- and HGC-Compatible Registers

I/O Address	Index	R/W	Name	Mnemonic	Description Page
3B5	10	R	Light Pen High	LPENH	5-1
3B5	11	R	Light Pen Low	LPENL	5-1
3B8	–	R/W	MDA-Mode Control	MDA_MODE	5-1
3B8	–	R/W	HGC-Mode Control	HGC_MODE	5-2
3B9	–	W	HGC-Set Light Pen Flag	HGC_SLPEN	5-3
3BA	–	R	HGC Status	HGC_STS	5-3
3BA	–	R	MDA Status	MDA_STS	5-4
3BB	–	W	Clear Light Pen Flag	HGC_CLPEN	5-4
3BF	–	R/W	HGC Configuration	CONFIG	5-4

A.3 VGA REGISTERS

The 86C928 is fully compatible with the VGA at the register level. The following table defines all VGA registers supported by this controller.

Table A-3. VGA Registers

I/O Address		Index	R/W	Name	Mnemonic	Description Page
Mono	Color					
General or External Registers						
3C2	3C2	–	W	Miscellaneous Output	MISC	6-1
3CC	3CC	–	R	Miscellaneous Output	MISC	6-1
3?A	3?A	–	W	Feature Control	FCR_WT	6-2
3CA	3CA	–	R	Feature Control	FCR_AD	6-2

Table A-3. VGA Registers (Continued)

I/O Address		Index	R/W	Name	Mnemonic	Description Page
Mono	Color					
3C2	3C2	–	R	Input Status 0	STATUS_0	6-3
3?A	3?A	–	R	Input Status 1	STATUS_1	6-3
Sequencer Registers						
3C4	3C4	–	R/W	Sequencer Index	SEQX	6-4
3C5	3C5	–	R/W	Sequencer Data	SEQ_DATA	6-4
3C5	3C5	00	R/W	Reset	RST_SYNC (SR0)	6-5
3C5	3C5	01	R/W	Clocking Mode	CLK_MODE (SR1)	6-5
3C5	3C5	02	R/W	Enable Write Plane	EN_WT_PL (SR2)	6-6
3C5	3C5	03	R/W	Character Font Select	CH_FONT_SL (SR3)	6-6
3C5	3C5	04	R/W	Memory Mode Control	MEM_MODE (SR4)	6-7
Controller Registers						
3B4	3D4	–	R/W	CRT Controller Index	CRTC_ADR (CRX)	6-8
3B5	3D5	–	R/W	CRT Controller Data	CRTC_DATA (CRT)	6-9
3B5	3D5	00	R/W	Horizontal Total	H_TOTAL (CR0)	6-9
3B5	3D5	01	R/W	Horizontal Display End	H_D_END (CR1)	6-9
3B5	3D5	02	R/W	Start Horizontal Blank	S_H_BLNK (CR2)	6-10
3B5	3D5	03	R/W	End Horizontal Blank	E_H_BLNK (CR3)	6-10
3B5	3D5	04	R/W	Start Horizontal Sync Position	S_H_SY_P (CR4)	6-11
3B5	3D5	05	R/W	End Horizontal Sync Position	E_H_SY_P (CR5)	6-11
3B5	3D5	06	R/W	Vertical Total	V_TOTAL (CR6)	6-12
3B5	3D5	07	R/W	CRTC Overflow	OVFL_REG (CR7)	6-12
3B5	3D5	08	R/W	Preset Row Scan	P_R_SCAN (CR8)	6-13
3B5	3D5	09	R/W	Maximum Scan Line	MAX_S_LN (CR9)	6-13
3B5	3D5	0A	R/W	Cursor Start Scan Line	CSSL (CRA)	6-14
3B5	3D5	0B	R/W	Cursor End Scan Line	CESL (CRB)	6-14
3B5	3D5	OC	R/W	Start Address High	STA(H) (CRC)	6-15
3B5	3D5	OD	R/W	Start Address Low	STA(L) (CRD)	6-15
3B5	3D5	OE	R/W	Cursor Location Address High (& Hardware Cursor Foreground Color in Enhanced Mode)	CLA(H) (CRE)	6-15
3B5	3D5	OF	R/W	Cursor Location Address Low (& Hardware Cursor Background Color in Enhanced Mode)	CLA(L) (CRF)	6-16
3B5	3D5	10	R/W	Vertical Retrace Start	VRS (CR10)	6-16
3B5	3D5	11	R/W	Vertical Retrace End	VRE (CR11)	6-16

Table A-3. VGA Registers (Continued)

I/O Address		Index	R/W	Name	Mnemonic	Description Page
Mono	Color					
3B5	3D5	12	R/W	Vertical Display End	VDE (CR12)	6-17
3B5	3D5	13	R/W	Offset	SCREEN_OFFSET (CR13)	6-18
3B5	3D5	14	R/W	Underline Location	ULL (CR14)	6-18
3B5	3D5	15	R/W	Start Vertical Blank	SVB (CR15)	6-19
3B5	3D5	16	R/W	End Vertical Blank	EVB (CR16)	6-19
3B5	3D5	17	R/W	CRTC Mode Control	CRT_MD (CR17)	6-20
3B5	3D5	18	R/W	Line Compare	LCM (CR18)	6-21
3B5	3D5	22	R	CPU Latch Data	GCCL (CR22)	6-22
3B5	3D5	24,26	R	Attribute Controller Flag/Index	ATC_F/I (CR24,26)	6-22
Graphics Controller Registers						
3CE	3CE	–	R/W	Graphics Controller Index	GRC_ADR (GRX)	6-23
3CF	3CF	–	R/W	Graphics Controller Data	GRC_DATA (GRD)	6-23
3CF	3CF	00	R/W	Set/Reset	SET/RST_DT (GR0)	6-24
3CF	3CF	01	R/W	Enable Set/Reset	EN_S/R_DT (GR1)	6-24
3CF	3CF	02	R/W	Color Compare	COLOR_CMP (GR2)	6-25
3CF	3CF	03	R/W	Raster Operation/Rotate Counter	WT_ROP/RTC (GR3)	6-25
3CF	3CF	04	R/W	Read Plane Select	RD_PL_SL (GR4)	6-26
3CF	3CF	05	R/W	Graphics Controller Mode	GRP_MODE (GR5)	6-27
3CF	3CF	06	R/W	Memory Map Mode Control	MISC_GM (GR6)	6-28
3CF	3CF	07	R/W	Color Don't Care	CMP_DNTC (GR7)	6-29
3CF	3CF	08	R/W	Bit Mask	BIT_MASK (GR8)	6-29
Attribute Registers						
3C0	3C0	–	R/W	Attribute Controller Index	ATR_AD	6-30
3C1/0	=	–	R/W	Attribute Controller Data	ATR_DATA	6-31
3C1/0	=	00–0F	R/W	Palette Register 00–15	PLT_REG (AR00–0F)	6-31
3C1/0	=	10	R/W	Attribute Mode Control	ATR_MODE (AR10)	6-32
3C1/0	=	11	R/W	Border Color	BDR_CLR (AR11)	6-33
3C1/0	=	12	R/W	Color Plane Enable	DISP_PLN (AR12)	6-33
3C1/0	=	13	R/W	Horizontal Pixel Panning	H_PX_PAN (AR13)	6-34
3C1/0	=	14	R/W	Pixel Padding	PX_PAD (AR14)	6-35
Setup Registers						
102	102	–	R/W	Setup Option Select	SETUP_OS	6-36
46E8	46E8	–	W	Video Subsystem Enable	SETUP_VSE	6-37

Table A-3. VGA Registers (Continued)

I/O Address		Index	R/W	Name	Mnemonic	Description Page
Mono	Color					
VIDEO DAC Registers						
3C6	3C6	–	R/W	DAC Mask	DAC_AD_MK	6-38
3C7	3C7	–	W	DAC Read Index	DAC_RD_AD)	6-38
3C7	3C7	–	R	DAC Status	DAC_STS	6-39
3C8	3C8	–	R/W	DAC Write Index	DAC_WR_AD	6-39
3C9	3C9	–	R/W	DAC Data	DAC_DATA	6-40

A.4 S3 VGA REGISTERS

The 86C928 has additional registers to extend the functions of basic VGA. These registers are located in CRT Controller address space at locations not used by IBM. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 1 register (CR38) must be loaded with a binary unlock key pattern (see the register description). The registers will remain unlocked until the key pattern is reset.

The additional VGA registers are described in the following table:

Table A-4. VGA S3 Registers

I/O Address		Index	R/W	Name	Mnemonic	Description Page
Mono	Color					
3B5	3D5	30	R	Chip ID/Rev Register	CHIP_ID/REV (CR30)	7-1
3B5	3D5	31	R/W	Memory Configuration	MEM_CNFG (CR31)	7-1
3B5	3D5	32	R/W	Backward Compatibility 1	BKWD_1 (CR32)	7-2
3B5	3D5	33	R/W	Backward Compatibility 2	BKWD_2 (CR33)	7-3
3B5	3D5	34	R/W	Backward Compatibility 3	BKWD_3 (CR34)	7-4
3B5	3D5	35	R/W	CRT Register Lock	CRTR_LOCK (CR35)	7-5
3B5	3D5	36	R	Configuration 1	CONFG_REG1 (CR36)	7-6
3B5	3D5	37	R	Configuration 2	CNFG_REG2 (CR37)	7-6
3B5	3D5	38	R/W	Register Lock 1	REG_LOCK1 (CR38)	7-7
3B5	3D5	39	R/W	Register Lock 2	REG_LOCK2 (CR39)	7-7
3B5	3D5	3A	R/W	Miscellaneous 1	MISC_1 (CR3A)	7-8
3B5	3D5	3B	R/W	Data Transfer Execute Position	(DT_EX_POS) (CR3B)	7-9
3B5	3D5	3C	R/W	Interlace Retrace Start	IL_RTSTART (CR3C)	7-9

A.5 SYSTEM CONTROL REGISTERS

System Control registers are configuration registers, mode control registers, and hardware graphics cursor control registers. They are positioned in the same indexed register space as VGA S3 registers. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 2 register (CR39) must be loaded with a binary unlock key pattern (see the register description). The registers will remain unlocked until the key pattern is reset.

The following table summarizes the System Control registers.

Table A-5. System Control Registers

I/O Address		Index	R/W	Name	Mnemonic	Description Page
Mono	Color					
3B5	3D5	40	R/W	System Configuration	SYS_CNFG (CR40)	8-1
3B5	3D5	41	R/W	BIOS Flag	BIOS_FLAG (CR41)	8-2
3B5	3D5	42	R/W	Mode Control	MODE_CTL (CR42)	8-3
3B5	3D5	43	R/W	Extended Mode	EXT_MODE (CR43)	8-4
3B5	3D5	45	R/W	Hardware Graphics Cursor Mode	HWGC_MODE (CR45	8-5
3B5	3D5	46–47	R/W	Hardware Graphics Cursor Origin-X	HWGC_ORGX (CR46-47)	8-6
3B5	3D5	48–49	R/W	Hardware Graphics Cursor Origin-Y	HWGC_ORGY (CR48-49)	8-6
3B5	3D5	4A	R/W	Hardware Graphics Cursor Foreground Stack	HWGC_FGSTK (CR4A)	8-6
3B5	3B5	4B	R/W	Hardware Graphics Cursor Background Stack	HWGC_BFSTK (CR4B)	8-7
3B5	3D5	4C–4D	R/W	Hardware Graphics Cursor Start Address	HWGC_STADR (CR4C-4D)	8-7
3B5	3D5	4E	R/W	Hardware Graphics Cursor Pattern Display Start X-Pixel Position	HWGC_DX (CR4E)	8-7
3B5	3D5	4F	R/W	Hardware Graphics Cursor Pattern Display Start Y-Pixel Position	HGC_DY (CR4F)	8-8

A.6 SYSTEM EXTENSION REGISTERS

These registers provide extended system and memory control, external sync control and addressing window control. They are enabled in the same way as the System Control registers via the Register Lock 2 register (CR39).

Table A-6. System Extension Registers

I/O Address	Index	R/W	Name	Mnemonic	Description Page
3?5	50	R/W	Extended System Cont 1	EX_SCTL_1 (CR50)	9-1
3?5	51	R/W	Extended System Cont 2	EX_SCTL_2 (CR51)	9-2
3?5	52	R/W	Extended BIOS Flag 1	EXT_BFLG1 (CR52)	9-3
3?5	53	R/W	Extended Memory Cont 1	EX_MCTL-1 (CR53)	9-3
3?5	54	R/W	Extended Memory Cont 2	EX_MCTL_2 (CR54)	9-4
3?5	55	R/W	Extended DAC Control	EX_DAC_CT (CR55)	9-4
3?5	56	R/W	External Sync Cont 1	EX_SYNC_1 (CR56)	9-5
3?5	57	R/W	External Sync Cont 2	EX_SYNC_2 (CR57	9-6
3?5	58	R/W	Linear Address Window Control	LAW_CTL (CR58)	9-6
3?5	59-5A	R/W	Linear Address Window Position	LAW_POS (CR59-5A)	9-7
3?5	5B	R/W	Extended BIOS Flag 2	EXT_BFLG2 (CR5B)	9-8
3?5	5C	R/W	General Out Port	GOUT_PORT (CR5C)	9-8
3?5	5D	R/W	Extended Horizontal Overflow	EXT_H_OVF (CR5D)	9-9
3?5	5E	R/W	Extended Vertical Overflow	EXT_V_OVF (CR5E)	9-9
3?5	5F	R/W	Bus Grant Termination Position	BGNT_TPOS	9-10

A.7 ENHANCED COMMANDS REGISTERS

This section lists the registers which support the 86C928 enhanced drawing functions. All of these registers are byte or word-addressed and are enabled only if bit 0 of the System Configuration register (CR40) is turned on.

Table A-7. Enhanced Commands Registers

I/O Address	Index	R/W	Name	Mnemonic	Description Page
42E8		R	Subsystem Status	SUBSYS_STAT	10-1
42E8		W	Subsystem Control	SUBSYS_CNTL	10-2
4AE8		R/W	Advanced Function Control	ADVFUNC_CNTL	10-4
82E8		R/W	Current Y Position	CUR_Y	10-5
86E8		R/W	Current X Position	CUR_X	10-5
8AE8		R/W	Destination Y Position/ Axial Step Constant	DESTY_AXSTP	10-5
8EE8		R/W	Destination X Position/ Diagonal Step Constant	DESTX_DIASTP	10-6
92E8		R/W	Error Term	ERR_TERM	10-7
96E8		R/W	Major Axis Pixel Count	MAJ_AXIS_PCNT	10-7
9AE8		R	Graphics Processor Status	GP_STAT	10-8
9AE8		W	Drawing Command	CMD	10-8
9EE8		W	Short Stroke Vector Transfer	SHORT_STROKE	10-11
A2E8		R/W	Background Color	BKGD_COLOR	10-11
A6E8		R/W	Foreground Color	FRGD_COLOR	10-12
AAE8		R/W	Write Mask	WRT_MASK	10-12
AEE8		R/W	Read Mask	RD_MASK	10-13
B2E8		R/W	Color Compare	COLOR_CMP	10-13
B6E8		W	Background Mix	BKGD_MIX	10-14
BAE8		W	Foreground Mix	FRGD_MIX	10-14
BEE8		R	Read Register Data	RD_REG_DT	10-15
BEE8	0	W	Minor Axis Pixel Count	MIN_AXIS_PCNT	10-15
BEE8	1	W	Top Scissors	SCISSORS_T	10-16
BEE8	2	W	Left Scissors	SCISSORS_L	10-16
BEE8	3	W	Bottom Scissors	SCISSORS_B	10-16
BEE8	4	W	Right Scissors	SCISSORS_R	10-17
BEE8	A	W	Pixel Control	PIX_CNTL	10-17
BEE8	E	W	Multifunction Control Miscellaneous	MULT_MISC	10-18
BEE8	F	W	Read Register Select	READ_SEL	10-19
E2E8		R/W	Pixel Data Transfer	PIX_TRANS	10-19
E2EA		R/W	Pixel Data Transfer-Extension	PIX_TRANS_EXT	10-20

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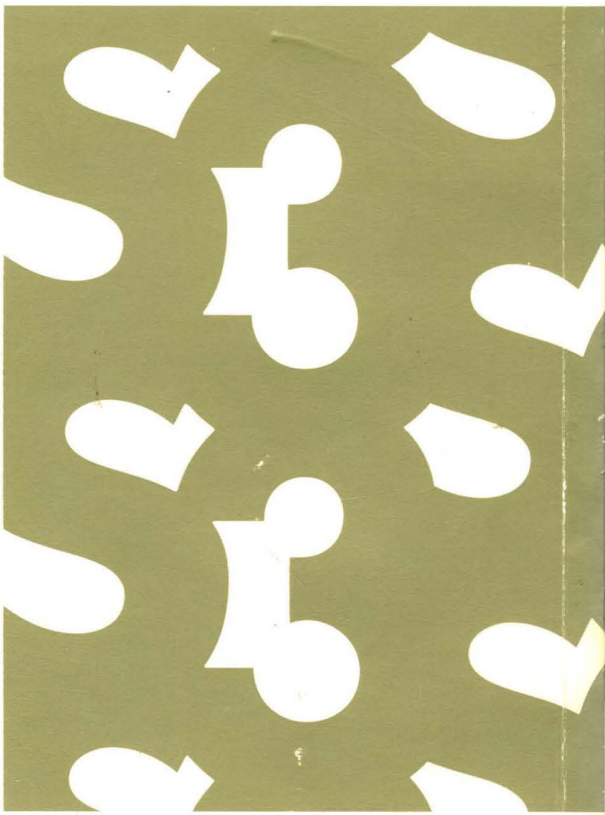

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