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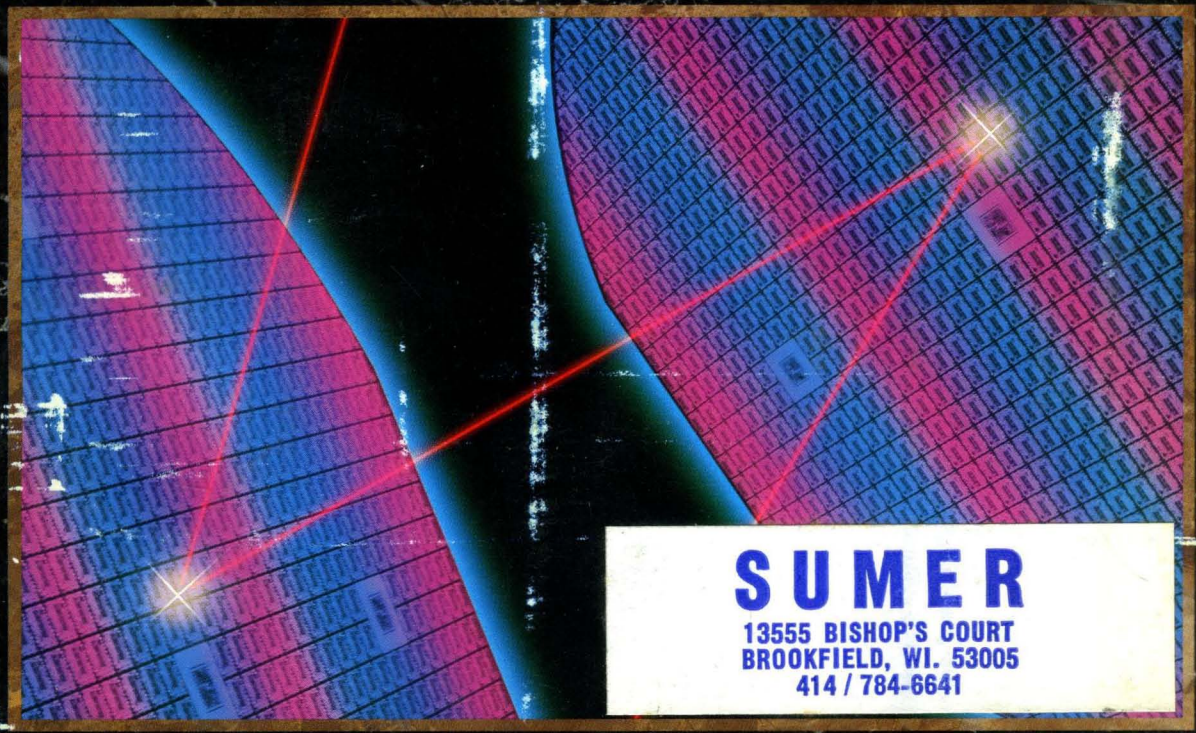
SSM AUDIO PRODUCTS

AUDIO HANDBOOK

VOLUME 1

INSIDE: Latest SSM Product Data
19 Application Notes



PMI®

SSM AUDIO PRODUCTS

AUDIO HANDBOOK

VOLUME 1

PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

TABLE OF CONTENTS

* Advance Information

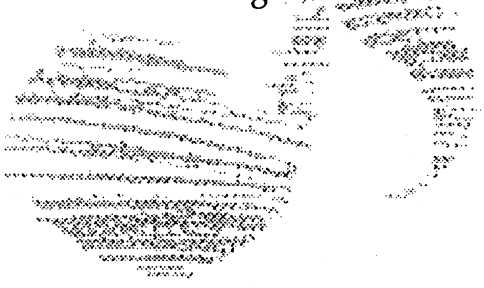
Application Notes - New 1989 and 1990 Publication

INTRODUCTION

We are proud to present Volume One of PMI's *Audio Handbook*. It represents a significant advance over previous SSM literature and is the result of extensive effort from numerous PMI employees. Inside you will find 26 data sheets and 19 application notes. The data sheets for the original 14 products have been completely rewritten and reformatted to be more concise and useful. Full data on seven new products released since the last SSM Product Guide is included, as is advance information on five new products which will be introduced soon.

The application notes were written to provide pragmatic solutions to real-world audio design problems. All were written by experienced systems designers, not IC designers. One note, the Morgan Compressor/Limiter (AN-135), was prepared by industry-renowned designer Michael Morgan who has spent many years developing state-of-the-art dynamic range processors.

Precision Monolithics, Inc., through its SSM Audio Products group, is committed to the ongoing development of high-performance ICs for applications in all ranges of audio equipment, including professional, consumer, automotive, medical, military, and industrial. Our goal is to provide integrated solutions resulting in higher performance, lower cost, improved quality, and hence greater overall value.



DEFINITIONS

Class A VCA – The standing (quiescent) current in the gain core transistors is the maximum output current the VCA can deliver without resulting in clipping or a large increase in distortion.

Class AB VCA – The gain core standing current is significantly less than the full output current.

Control Feedthrough, or Control Breakthrough – The amount of a control signal reaching the output of a VCA with no signal applied. Control feedthrough can be measured in terms of current, voltage, or dB.

Control Rejection – A ratio of an output signal to control voltage.

Decibels (db) – The decibel is a ratio of two quantities, and therefore is a relative rather than an absolute measurement. The mathematical formulas used to calculate dB are as follows:

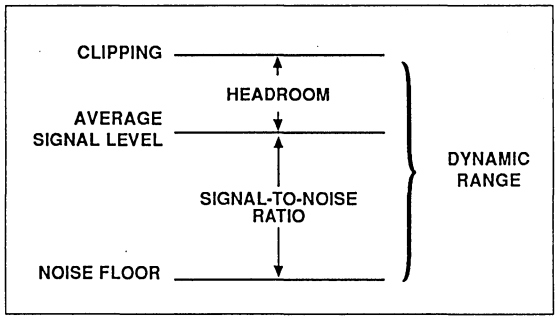
$dB_{watts} = 10 \log (P_1/P_0)$
$dB_{volts} = 20 \log (V_1/V_0)$

dB_{watts} provides a ratio for two power levels, P_1 and P_0. dB_{volts} is the calculation for two voltage levels, V_1 and V_0.

In some instances, however, dBs are expressed relative to a given reference level. Audio circuits may refer to one or more of the following relative dB types:

dBm: 0dB is referenced to 1mW
dBu: 0dBu is referenced to $0.775V_{RMS}$
dBV: 0dBV is referenced to $1V_{RMS}$
dBW: 0dBW is referenced to 1W
dB SPL: for sound pressure level
0dB SPL = 0.0002 dynes/cm^2
(threshold of hearing)

Dynamic Range – The magnitude, measured in dB, between clipping and the electronic noise floor of a device.



Dynamic Range Processor – A system whereby effective dynamic range is increased (such as noise reduction), or decreased (as with a compressor/limiter).

Equivalent Input Noise (EIN) – A measurement, in dBm, of noise at the output of a device with amplifier gain subtracted. The measurement is performed with a resistor connected across the input (usually 150Ω), the value of which must be specified. The theoretical minimum noise of a 150Ω resistor with 20Hz to 20kHz bandwidth at 15°C (59°F) is –131.9dBm.

Frequency Response – Indicates input-to-output frequency versus amplitude performance. A typical frequency response specification might be 20Hz to 40kHz, ±3dB. This means that amplitude will not vary more than 3dB at any frequency between 20Hz and 40kHz.

Headroom – The difference, measured in dB, between clip level and the average signal level.

Input Noise Voltage Density (e_n) – The RMS noise voltage in a 1Hz band centered on a specified frequency.

Intermodulation Distortion (SMPTE) – A peak voltage measurement of non-harmonic output frequencies caused by an electronic circuit, using 60Hz and 7kHz tones with a 4:1 ratio.

Noise Corner – The frequency below which the noise floor of an amplifier increases with input(s) shorted to ground.

Noise Figure – Related to EIN, the noise figure expresses in dB the incremental noise of a circuit over the theoretical minimum. For example, a circuit using a 150Ω source impedance with EIN of –129.5dB has a noise figure of 2.4dB.

Nominal, or Average, Signal Level – The average electronic line level of program material passing through an electronic device, measured in dB with respect to a given reference level.

Pink Noise – Filtered thermal noise to provide flat frequency response of 0dB over a 20Hz to 20kHz range. Equal noise power per octave.

Resonance – A sympathetic electrical vibration caused by reactive (capacitive or inductive) elements which causes peaking in the frequency response of a system.

Signal-to-Noise Ratio (SNR) – The difference, measured in dB, between the average signal level and the electronic noise floor. A statement of headroom should normally accompany the SNR.

Total Harmonic Distortion – A measurement, expressed as a percentage, of the RMS harmonic distortion components added to an audio signal by an electronic circuit.

White Noise – Unaltered thermal noise. Equal noise power per hertz over the frequency band.

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Audio Silicon Specialists™

SSM-2013
VOLTAGE-CONTROLLED AMPLIFIER

Precision Monolithics Inc.

FEATURES
- 0.01% THD Typ
- 0.03% IMD Typ
- 800kHz Unity-Gain Bandwidth
- 12dB Headroom (at Rating)
- 40dB Gain Capability
- 106dB Dynamic Range (17.5 Bits)
- Full Class A Performance
- Mute and Exponential Controls

APPLICATIONS
- Compressor/Limiters
- Noise Gates
- Automatic Gain Control
- Noise Reduction Systems
- Telephone Line Interfaces

ORDERING INFORMATION

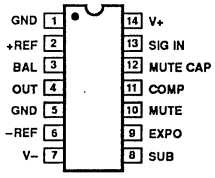
PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 14-PIN	
SSM2013P	–10°C to +55°C

GENERAL DESCRIPTION

The SSM-2013 is a high-performance monolithic Class A Voltage Controlled Amplifier. Operating with current mode inputs and outputs, the SSM-2013 is ideal when logarithmic control of gain is needed. The output current gain or attenuation is controlled by applying a control voltage to the EXPO pin 9. The amplifier offers wide bandwidth, easy signal summing and minimum external component count.

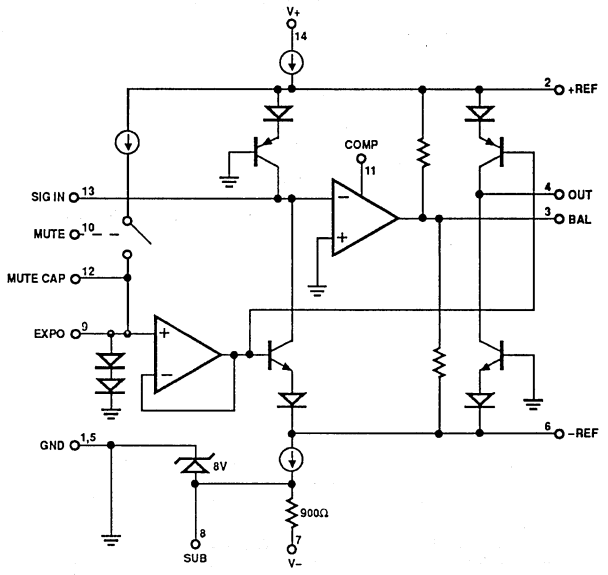
The SSM-2013 can operate with more than 12dB of headroom at the rated specifications or be configured for gains as high as 40dB. Inherently low control feedthrough and 2nd harmonic distortion make trimming unnecessary for most applications. An extremely wide control range of 110dB regulated by a flexible antilogarithmic control port make this VCA a versatile analog building block. With 800kHz bandwidth and 94dB S/N ratio at 0.01% THD, the SSM-2013 provides a useful solution for a variety of signal conditioning needs in applications ranging from professional audio to analog instrumentation, process controls and more.

PIN CONNECTIONS



14-PIN PLASTIC DIP (P-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 36V or ±18V
Junction Temperature ..... +150°C
Operating Temperature Range ..... –10°C to +55°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Current into any Pin 10mA
Lead Temperature Range (Soldering 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
14-Pin Plastic DIP (P)	90	47	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V and T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	SSM-2013 MIN	SSM-2013 TYP	SSM-2013 MAX	UNITS
Positive Supply Voltage Negative Supply Voltage (Note 1)		+12 –7.6	+15 –8.2	+18 –8.7	V
Positive Supply Current Negative Supply Current		5.4 6.0	8.7 8.7	10.4 11.0	mA
Negative Supply Bias Resistor (Pin 7 to Pin 8)		675	900	1170	Ω
Expo Input Bias	V_e = GND (Note 2)	–	1.0	3.2	µA
Expo Control Sensitivity	at Pin 9	–	–10	–	mV/dB
Mute Off (Logic Low)		0.0	–	1.0	V
Mute On (Logic High)		3.0	5	15	V
Mute Attenuation	(@ 1kHz, $V_{PIN\ 10}$ = +5V)	–	–90	–	dB
Current Gain	V_e = GND	0.90	1.0	1.1	
Current Output Offset	V_e = GND	–7.5	0	+7.5	µA
Output Leakage	V_e = +600mV	–50	0	+50	nA
Max Available Output Current	V_e = GND, 15k (pin 3 to –V)	±1.2	–	–	mA
Current Bandwidth (3dB)	V_e = GND	–	800	–	kHz
Signal Feedthrough	V_e = +1.2V	–	–90	–	dB
Signal to Noise (20Hz - 20kHz) (Notes 3, 4)	V_e = GND, No Signal	–	–94	92.5	dB
THD (Untrimmed) (Note 4)	V_e = GND, I_{IN} = 600µA_{p-p}	–	0.01	0.06	%
THD (Trimmed)	V_e = GND, I_{IN} = 600µA_{p-p}	–	0.004	–	%
IMD (Untrimmed) SMPTE (Note 4)	V_e = GND, I_{IN} = 600µA_{p-p}	–	0.03	0.12	%
IMD (Trimmed) SMPTE	V_e = GND, I_{IN} = 600µA_{p-p}	–	0.012	–	%

NOTES:
1. Measured at pin 8, pin 7 = –15V.
2. V_e is voltage on pin 9 (V_{EXPO}).
3. Referred to a 400µA_{p-p} input level.
4. Parameter is sample tested to max limit (0.4% AQL).

Specifications subject to change; consult latest data sheet.

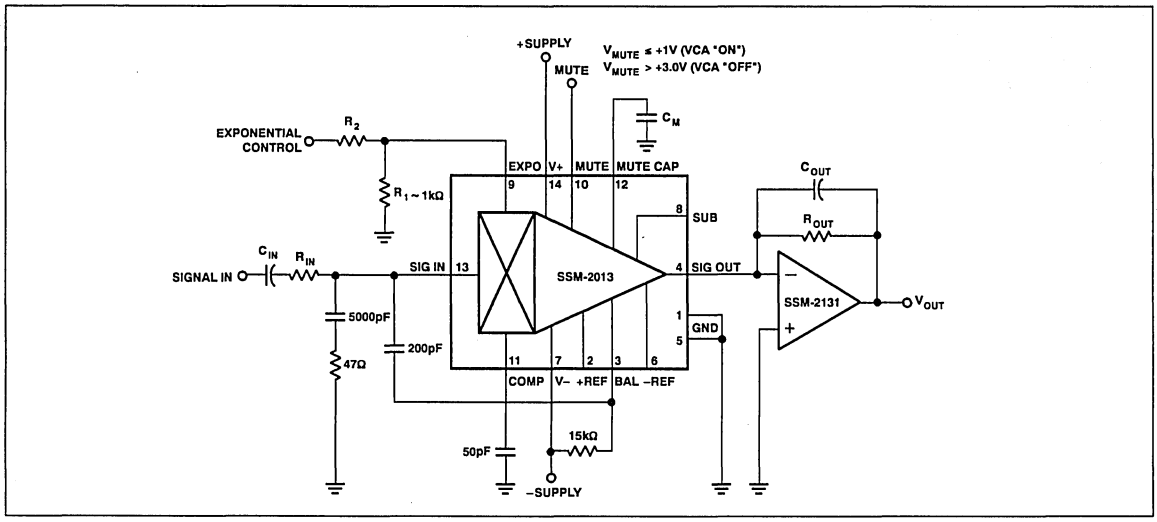


FIGURE 1: *Typical Connection*

THEORY OF OPERATION

The SSM-2013 is a current input/current output device. It is essentially a current mode amplifier where the output current/ input current transfer function is controlled by a control voltage applied at the EXPO pin (9). Current mode operation allows easy adaptation to various voltage ranges at the input, output and control port. As configured, it offers large attenuation plus moderate gain capability.

CHOOSING R_{IN}

Most applications use the typical connection of Figure 1. In this configuration, The SSM-2013 will accomodate input currents up to 1.2mA without significant distortion or clipping. To set the maximum operating current to 1.2mA, select R_{IN} to equal Vpeak/1.2mA.

As an example: For a $7V_{p-p}$ nominal signal level (±3.5V), select R_{IN} = 12kΩ. Here, I_{IN} operating is: 3.5V/12k = 300μA, which yields 12dB headroom from 1.2mA. In some applications such as broadcast equipment, 16 - 24dB headroom may be required.

Selecting ±300μA nominal operating current yields 12dB headroom. Figure 2 shows the IMD/THD (Intermodulation and Total Harmonic Distortion) characteristics of the SSM-2013 at this 300μA or 600μA peak-to-peak operating level.

Operation at higher input currents will increase distortion effects whereas operation at lower currents will improve distortion but decrease the S/N ratio. For examle, operation with 20dB headroom versus 12dB will improve the relative effects of IMD/THD shown in Figure 2 by 2.5 times. For 20dB headroom, use ±120μA nominal operating input current. At this level, the signal-to-noise ratio will be 86dB.

The SSM-2013 is capable of 40dB gain and as much as –95dB attenuation. Gain or attenuation levels are set by the EXPO control pin as described in the next section. Figure 2 shows how IMD/THD performance degrades with current gain and attenuation. Note also that distortion in the SSM-2013 is nearly all 2nd harmonic. From a sonic standpoint, this is much less objectionable than other types of distortion.

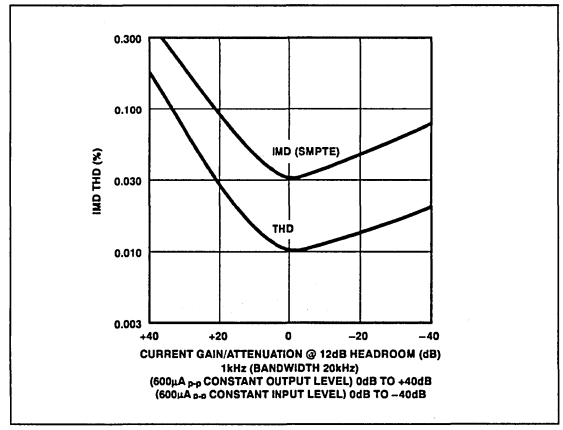


FIGURE 2

For best performance, choose C_{IN} and R_{IN} for a cutoff frequency below the audio band. C_{IN} will block DC offsets from previous stages.

OUTPUT SECTION

When establishing circuit gain or attenuation, it is important to consider the tradeoffs between gain/attenuation for the SSM-2013 versus the gain of the output amplifier/current to voltage

converter. Operating the SSM-2013 with current gain above 20 or 30dB increases distortion as shown in Figure 2. Gain in the output amplifier amplifies the VCA noise. This will directly increase the equivalent VCA noise floor by the amplifier gain. A compromise within these constraints will determine the best tradeoff between SSM-2013 current gain and the amplifier gain. Figure 3 shows how output noise increases as current gain increases.

CONTROL PIN EXPO

The control port EXPO (pin 9) is a high impedance input with an exponential control sensitivity of –1dB/10mV or –10mV/dB. The overall control range is +40dB to –95dB. This pin is easily adaptable to any control voltage range by selecting the R_1 and R_2

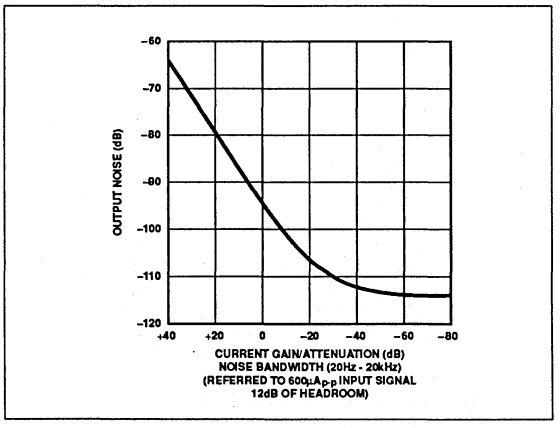


FIGURE 3

divider appropriately. Note the negative control relationship where positive voltages at pin 9 result in signal attenuation whereas negative voltages yield gain. The control pin is accurate to within ±1.5dB over a ±36dB range.

The transfer characteristics for the control pin is shown in Figure 4. Note the dotted line showing an optional improvement in gain accuracy. To achieve this improved transfer characteristic, refer to the circuit of Figure 5. As the recommended circuit for control summing applications, this technique offers a significant improvement in linearity over a wider control voltage range.

The control port sensitivity has a –3300ppm/°C temperature coefficient. To compensate for this drift, use a +3300ppm/°C tempsistor* in place of R_1 shown in Figure 1.

MUTING FUNCTION

The mute circuit turns the device on or off independent of the control pin EXPO. Muting is activated when the MUTE (pin 10) is raised above 3.0V and is compatible up to 15V. Muting is off when MUTE is below 1.0V.

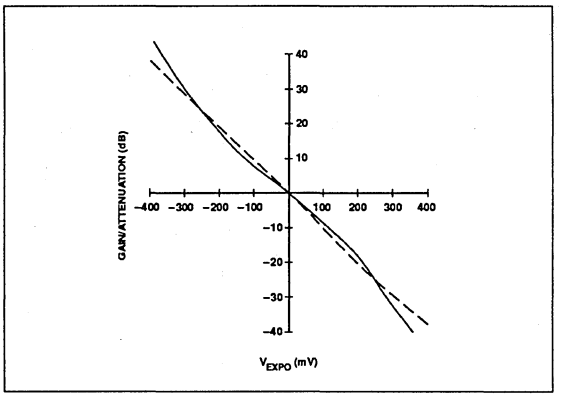


FIGURE 4: *Circuit Gain/Attenuation vs. V_{EXPO}*

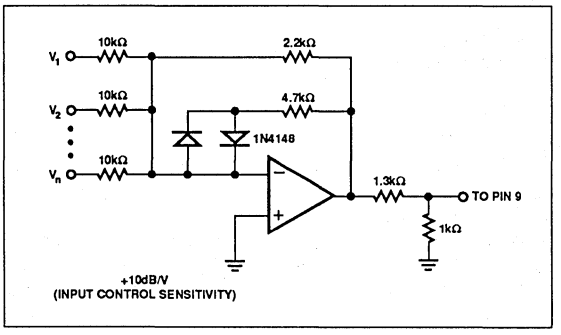


FIGURE 5: *Control Summer with Improved Linearity over Wider Control Range*

A selectable MUTE CAP connected between pin 12 and ground determines the controlled turn on/turn off rate. The recommended 1µF mute cap and internal 10kΩ impedance gives a 10ms time constant. This transition timing is considered quick without being too abrupt or "poppy."

To disable the muting function, simply ground pin 10.

APPLICATIONS INFORMATION

OUTPUT AMPLIFIER

Note the importance of including C_{OUT} in parallel with R_{OUT} to ensure stability under all signal and output loading conditions. A corner frequency of 300kHz for the R_{OUT}, C_{OUT} combination is sufficient, but a lower frequency may also be chosen to limit noise output the audio band. This, however will result in a slower transient response.

* RCD Components, Inc. Part Number LP1/4, 3301 Bedford Street, Manchester, NH U.S.A., (603) 669-0054, Telex 943512

CONTROL FEEDTHROUGH TRIMMING

Control feedthrough is defined as the portion of the control signal fed to the output in the absence of an input signal. A single shunt resistor across pins 2 and 6 will reduce both control feedthrough and noise (see Figure 6). Values from 3.3kΩ to 5.4kΩ offer an improvement in control feedthrough from 20dB to 10dB, respectively.

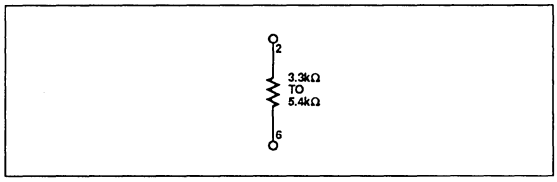


FIGURE 6

This trim will tradeoff an increase in THD by roughly 3 to 5 times. THD increases slightly more using a lower resistor value. With 3.3kΩ, the worst case is about 0.4% over gain and attenuation. By comparison, THD ranges from 0.05% to 0.1% with no shunt resistor.

TRIMMING DISTORTION

The SSM-2013 has very good distortion, offset and control feedthrough at unity current gain. For applications requiring over 10dB to 20dB gain, trimming allows the best overall distortion versus gain.

Distortion Trim Procedure for High Gain Applications:

1. Apply voltage at pin 9 corresponding to maximum current gain.
2. Set input level so output is just below clipping.
3. Adjust trimming per Figure 7 until distortion is at a minimum.

COMPENSATION

To compensate, connect a 50pF capacitor from pin 11 (COMP) to GND as shown in the typical connection.

ON-BOARD REFERENCE

An on-chip zener diode helps establish the –8V available at the SUB output (pin 8). This is a general purpose reference that can be used to introduce DC offsets.

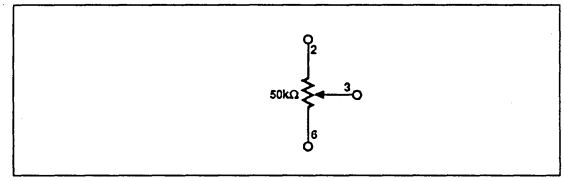


FIGURE 7

BREADBOARDING THE SSM-2013

A typical connection identical to Figure 1 and redrawn for breadboarding purposes is shown in Figure 8.

MEASURING NOISE

When measuring audio noise in the SSM-2013, bandwidth should be limited to 20kHz to 30kHz. This is due to the presence of broadband noise which is caused by a zero at 600kHz. The zero results from the 5000pF-47Ω network at the input. Beyond 30kHz, the noise floor increases at approximately 6dB per octave from 45kHz to 600kHz where it rolls off.

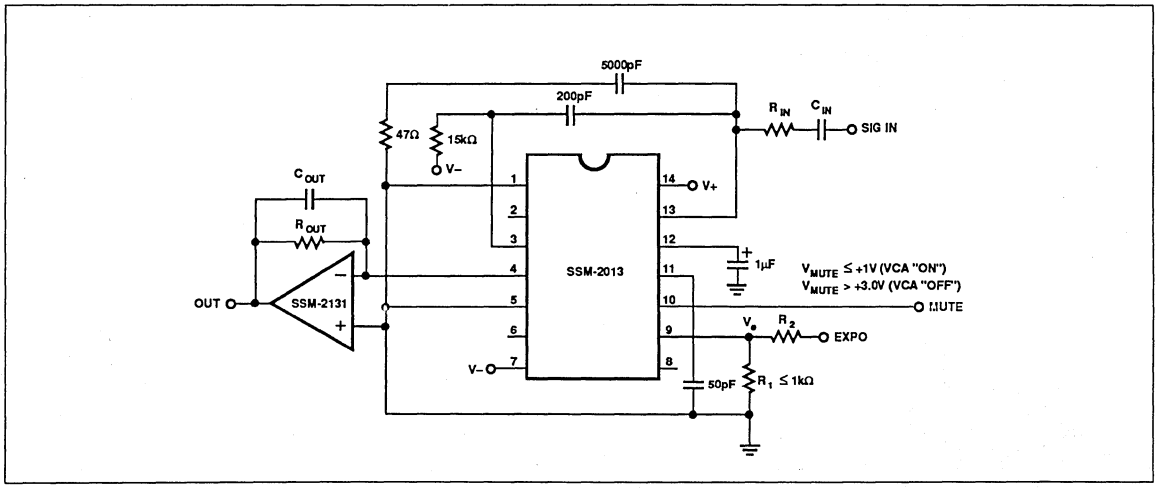


FIGURE 8: *Typical Connection for Breadboarding*

PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

SSM-2014

VOLTAGE-CONTROLLED AMPLIFIER/OVCE

FEATURES

- Wide Dynamic Range ..... 116dB (Class AB)
  ..... 104dB (Class A)
- 12MHz Effective Gain-Bandwidth Product
- 100dB Open-Loop Gain
- 0.01% THD Class A (Any Gain/Signal) @ = 10dBV$_{IN/OUT}$
- Minimum External Component Count
- No Trimming in Many Applications
- Low Cost

UNIQUE FEATURES

- Voltage Selectable Class A or AB Operation
- Low Distortion vs. Frequency
- No Active Components Needed
- Operates at ±15V
- Low Modulation Noise
- Complementary Current Outputs
- Combines Op Amp and VCA Features
- Fully Buffered Control Port
- High and Low (Balanced) Impedance Inputs

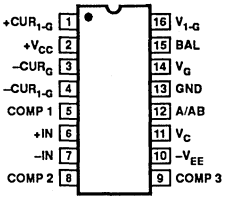
APPLICATIONS

- Voltage-Controlled Amplifiers
- Voltage-Controlled Preamplifiers
- Voltage-Controlled Panners
- Voltage-Controlled Equalizers
- Voltage-Controlled Oscillators
- Console Automation Systems
- Dynamics Processors
- Fader Automation

ORDERING INFORMATION

PACKAGE PLASTIC 16-PIN	OPERATING TEMPERATURE RANGE
SSM2014P	–10°C to +55°C

PIN CONNECTIONS

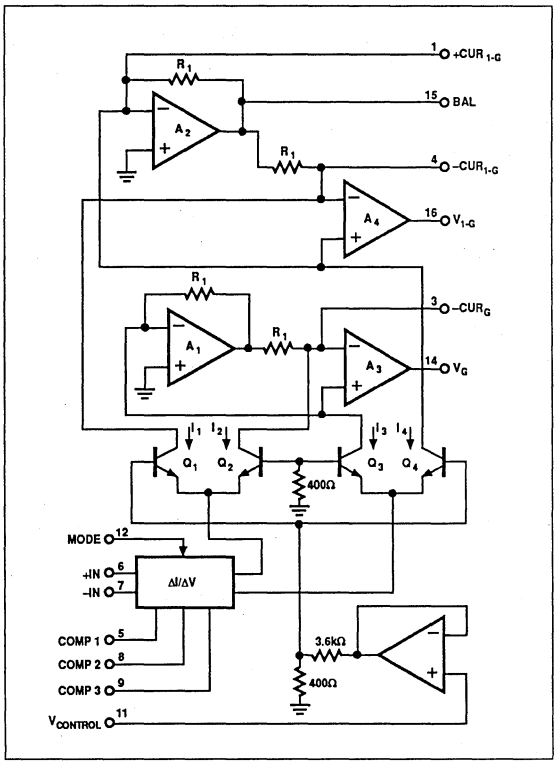


16-PIN PLASTIC DIP (P-Suffix)

DESCRIPTION

The SSM-2014 is an extremely flexible VCA building block that rivals the best monolithic VCAs while approaching the performance of modular devices. This versatile device acts as a VCA or OVCE (Operational Voltage-Controlled Element) and has inputs and outputs that can operate either in the current or voltage domain. To optimize performance at different signal levels, the SSM-2014 features programmable Class A or Class AB operation. This feature, along with the many configurations possible for operation make the SSM-2014 a unique and powerful signal processing tool. The device can be configured as a VCA or VCP (Voltage-Controlled Panner) and can replace a standard VCA and two or more operational amplifiers. Operation as a standard VCA provides up to 50dB gain and excellent specifications at any signal level. As a result, the SSM-2014 is an ideal choice for any system requiring remote or automatic control of gain or volume.

BLOCK DIAGRAM



Manufactured under the following U.S. Patents: 4,471,320 and 4, 560, 947. Other Patents pending. Mask work protected under the Semiconductor Chip Protection Act of 1983.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 36V or ±18V
Junction Temperature ..... +150°C
Operating Temperature Range ..... –10°C to +55°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Current Into Any Pin 10mA
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Plastic DIP (P)	90	47	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V and T_A = ±25°C, unless otherwise specified.

		SSM-2014			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT AMPLIFIER					
Bias Current		–	100	300	nA
Input Offset Current		–	15	30	nA
Input Offset Voltage		–	0.5	2	mV
Input Impedance		0.5	1	–	MΩ
Equivalent Input Noise	@ 1kHz	–	18	–	nV/√Hz
Common-Mode Range		–	+13, –13	–	V
Open-Loop Gain		75	100	–	V/mV
Effective Gain BW Product	VCA Configuration VCP Configuration	– –	12 .5	– –	MHz
Slew Rate	VCA Configuration	–	6	–	V/µs
Supply Current - Positive		–	7.5	9	mA
Supply Current - Negative		–	10	12	mA
OUTPUT AMPLIFIERS					
Offset Voltage		–	10	20	mV
Minimum Load Resistor	For Full Output Swing	10	9	–	kΩ
Output Voltage Swing		–	±13.5	–	V
Noise Residual	20kHz Bandwidth	–	8	–	µV
CONTROL PORT					
Bias Current		–	150	300	nA
Input Impedance		–	1	–	MΩ
Gain Constant	Ratio of Outputs	–	–30	–	mV/dB
Gain Constant Temperature Coefficient		–	–3300	–	ppm/°C
Gain Linearity		–	0.5	–	%
Control Feedthrough (Trimmed) Class A Class AB Intermediate	100Hz Sine Wave Applied to Control Port Causing –30dB to +20dB of Gain	 – – –	 2 0.5 1	 – – –	mV
Control Feedthrough (Untrimmed) Class A Class AB (Note 1) Intermediate (Note 1)	100Hz Sine Wave Applied to Control Port Causing –30dB to +20dB of Gain	 – – –	 25 5 15	 75 15 45	mV
Off Isolation	@ 1kHz	100	105	–	dB

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = \pm 25°C$, unless otherwise specified. *Continued*

PARAMETER	CONDITIONS	SSM-2014 MIN	TYP	MAX	UNITS
Channel Specifications					
Noise - Class A (Note 2)	$R_{PIN\ 12} = 33k\Omega$, 20kHz BW	–	–85	–81	dBV
Noise - Class AB (Note 2)	$R_{PIN\ 12} = 330k\Omega$, 20kHz BW	–	–95	–92	dBV
Noise - Intermediate (Note 2)	$R_{PIN\ 12} = 43k\Omega$, 20kHz BW	–	–88	–85	dBV
THD - A @ A_V = 0dB (Note 3)	$R_{PIN\ 12} = 33k\Omega$	–	0.005	0.02	%
THD - A @ $A_V = \pm 20dB$ (Note 3)	$R_{PIN\ 12} = 33k\Omega$	–	0.02	0.04	%
THD - AB @ A_V = 0dB (Note 3)	$R_{PIN\ 12} = 330k\Omega$	–	0.02	0.05	%
THD - AB @ $A_V = \pm 20dB$ (Note 3)	$R_{PIN\ 12} = 330k\Omega$	–	0.06	0.12	%
THD - Intermediate @ A_V = 0dB (Note 3)	$R_{PIN\ 12} = 43k\Omega$	–	0.01	0.03	%
THD - Intermediate @ $A_V = \pm 20dB$ (Note 3)	$R_{PIN\ 12} = 43k\Omega$	–	0.03	0.06	%

NOTES:
1. Symmetry trim only.
2. Parameter sample lot tested to maximum limits.
3. V_{IN} and/or V_{OUT} = +10dBV. Specifications may be subject to change without notice.

THEORY OF OPERATION

The simplified schematic shows that the SSM-2014 is fundamentally a controllable gain block that operates in the current or voltage mode. The outputs are the product of an input signal and a control signal. These outputs along with differential inputs, a control port, and selectable bias for Class A or AB operation give the SSM-2014 unparalleled flexibility. It is important to note, however, that actual implementation of any given function can only be realized by applying feedback as shown in the applications sections.

INPUT SECTION

For most applications, input signals should be coupled by a DC blocking capacitor to prevent errors from previous stages from affecting control feedthrough. The input section consists of an op amp with differential inputs and a gain-variable compensation scheme controlled by the gain control port. The variable compensation makes it possible to maintain a bandwidth in excess of 120kHz over the gain range of ±40dB.

The output of the op amp faces a current splitter with a variable bias point controlled by pin 12. This bias point establishes the quiescent current in the gain core which sets the class of operation (Class A, AB or INT). The class of operation selected affects the noise, distortion, and control feedthrough performance.

IMPORTANT NOTE

A current between 40 to 500µA must be sourced into pin 12 for proper operation of the device. Without such a current, the output signal will appear half-wave rectified.

SELECTING CLASS OF OPERATION

The class of operation is set by the current into pin 12. A resistor connected between pin 12 and V+ can be used to establish this current. Table 1 indicates the recommended resistor values and typical performance tradeoffs for various classes of operation.

Class A operation is preferred for its distortion performance, particularly at high signal levels and over gain and attenuation. Distortion in Class A is nearly pure second harmonic, which from a sonic standpoint, is much less objectionable than other types.

Class AB operation provides significantly better control feedthrough performance and lower noise which is important at low signal levels.

DYNAMICALLY SETTING CLASS OF OPERATION

In order to realize the virtues of both classes of operation, it is possible to use a level detector to sense the input signal and dynamically change the VCA from Class AB at lower signal levels to Class A for signals above this (sometimes referred to as "sliding bias"). Low signal levels are usually considered to be less than +4dBV. A time constant in the range of 10 to 25 milliseconds should be included in the level detector to both smooth the signal and to subjectively eliminate the resulting noise floor modulation and output offset shift. Both of these effects are small compared to the signal level at which the class of operation changes.

TABLE 1

CLASS	A	AB	INTERMEDIATE	CONDITION
R_{SET}	33kΩ	330kΩ	43kΩ	$V_S = \pm 15V$
Noise	–84dBV	–95dBV	–88dBV	20kHz Bandwidth
THD @ A_V = 0dB	0.005	0.02	0.010*	$+10dBV_{IN/OUT}$ @ 1kHz
THD @ $A_V = \pm 20dB$	0.02	0.06	0.030*	$+10dBV_{IN/OUT}$ @ 1kHz
THD Type	Pure 2nd	Mostly 3rd	2nd*	
Trimmed Control Feedthrough	2mV	500µV	1mV	–30dB ≤ Gain ≤ +20dB

* For intermediate operation near unity-gain, distortion will increase and become mostly third harmonic for levels above $+14dBV_{IN/OUT}$.

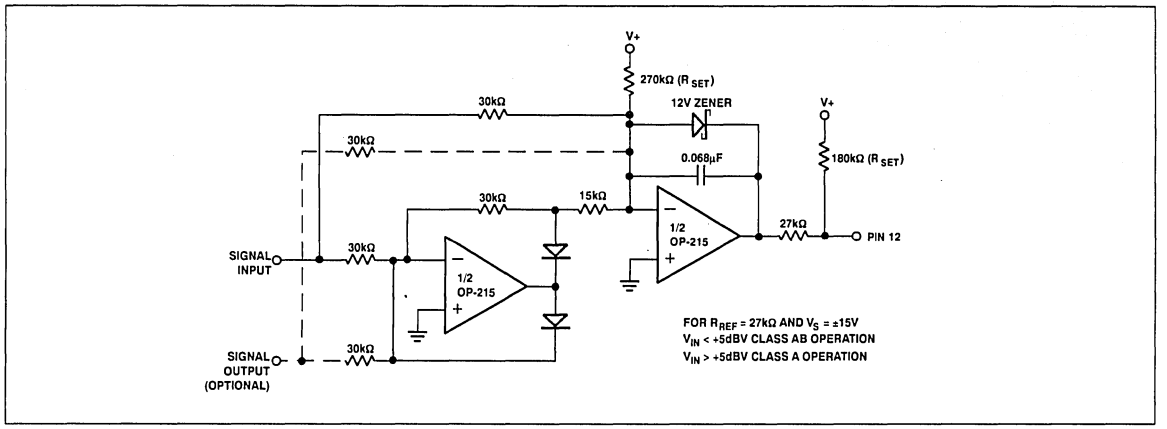


FIGURE 1: *SSM-2014 Operating Class Control Circuit (Sliding Bias)*

Figure 1 shows a typical level detector circuit which senses the input and/or output signal level and changes the SSM-2014 from Class AB to A when the signal exceeds +4dBV (R_{REF} = 270kΩ). Sensing the output signal is important in high-gain applications such as the voltage-controlled preamp. This circuit is a full-wave rectifier followed by an integrator which provides a fast, smooth transition. The 12V zener clamp diode in the feedback loop improves ripple rejection by maintaining the op amp output in its linear operating range. The output resistor network provides the program current into pin 12 for Class A or AB operation when the integrator output is high (+12V) or low (–0.6V) respectively. The program current is 500μA when the device operates in Class A (high) and 40μA when operating in Class AB (low).

CONTROL SECTION

The control sensitivity of the control port is –30mV/dB at pin 11. A simple resistor divider is ordinarily used to scale the control voltage source range to the desired voltage applied at the control port. This pin can draw as much as 300nA of bias current so the impedance of the divider to ground should be kept low. 10kΩ or less is recommended to keep gain error resulting from the voltage drop to a minimum. The graph of Figure 2 shows the control voltage transfer characteristic by plotting $V_{CONTROL}$ (at pin 11) vs. gain/attenuation over different temperatures.

When using the control pins, care must be taken to eliminate coupling to signal paths, particularly when using higher impedances.

The control port has a –3300ppm/°C temperature coefficient as do all dB/V VCAs. To compensate for this drift in automation systems, use a single tempsistor* with a +3300ppm/°C drift to replace the reference current set resistor in the system DAC. Temperature compensation can also be accomplished by using a tempsistor connected to the control pin to ground as part of the control input attenuator. This will improve tempco performance by five to ten times.

OUTPUT SECTION

The SSM-2014 has three current outputs and two voltage outputs. The current outputs can deliver at least 675μA signal current when operating on ±15V supplies. Feedback resistors for the internal or external current-to-voltage converter op amps should not be lower than 20kΩ with ±15V supplies. In normal operation, the current outputs are virtual grounds. The SSM-2014 block diagram shows that amplifiers A_1 and A_2 act as current mirrors that maintain the $+CUR_{1-G}$ to ground potential. Amplifiers A_3 and A_4 are used as current-to-voltage converters and maintain $-CUR_G$ and $-CUR_{1-G}$ at ground. If external op amps are used for this purpose, the on-board op amps can be disabled by connecting their outputs to the negative supply as shown in Figure 6. When used, the on-board op amps have current outputs and can sink in excess of 10mA and source a minimum of 1.5mA.

APPLICATIONS

The SSM-2014 can be used in a variety of ways. The most straightforward and perhaps the most often used configuration is that of a simple VCA. Here, the minimum VCA uses its own

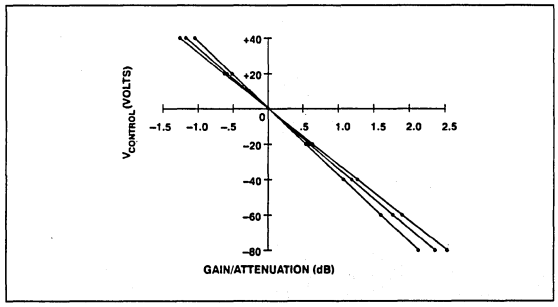


FIGURE 2: *$V_{CONTROL}$ at Pin 11 vs. Gain/Attenuation*

* RCD Components Inc., Manchester, N.H., TEL: (603) 669-0054 TLX: 943512

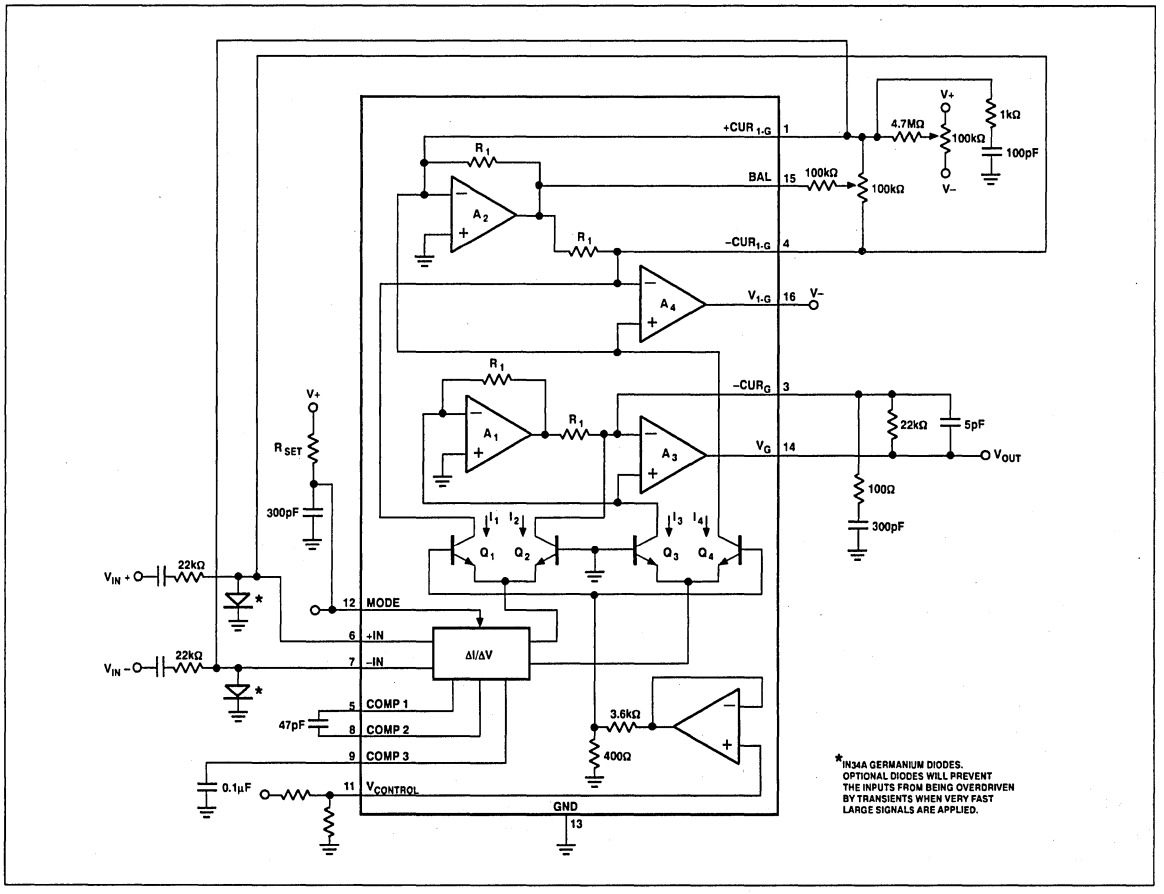


FIGURE 3a: *Simple VCA*

on-board op amps and using the configuration of Figures 3a and 3b, performs the basic VCA function of logarithmic voltage-controlled gain. In this application, the VCA is fixed in Class A or AB operation, whichever optimizes the tradeoff between noise and distortion.

Other functions are easily implemented using the SSM-2014 as an operational voltage-controlled element or "core" for other VCA configurations, including voltage-controlled panners and voltage-controlled preamplifiers. These applications will be described in the sections to follow.

SIMPLIFIED VCA OPERATION

The SSM-2014, when configured as a simple VCA, is a self-contained minimum component VCA with single-ended or differential inputs and a voltage output. The basic VCA configuration is shown in Figures 3a and 3b. Gain of up to 50dB is set by a voltage applied to the control pin. Current feedback from $+CUR_{1\text{-}G}$ to the –INPUT and $-CUR_{1\text{-}G}$ to the +INPUT creates differential virtual ground inputs. Input signals may be applied through blocking capacitors and 22kΩ resistors to pins 6 or 7

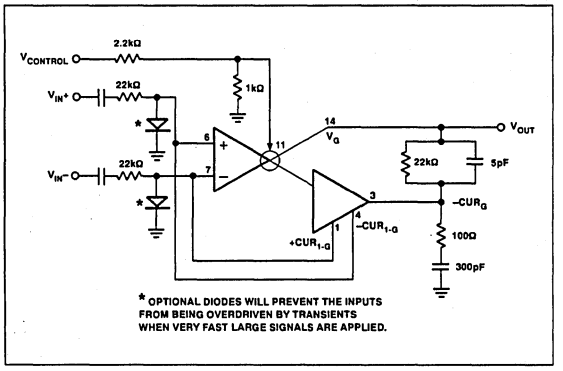


FIGURE 3b: *Block Diagram of Simple VCA*

(+IN and –IN). For single-ended inverting or noninverting operation, connect the unused input through 22kΩ to ground for best performance. Also, when large common-mode signals are present in differential operation, choose Class A operation.

Figure 4A shows typical distortion measurements using this circuit over gain and attenuation at 1kHz. (Figures 4b, 4c and 4d show THD vs. frequency for Class A and AB operation using +10dBV input.) These curves show THD at gain settings of +10dB, 0dB, and –10dB, respectively. Figure 4b is the worst case showing the amplifier near clipping.

The noise performance of the device with shorted inputs measured over a 20kHz bandwidth is seen in Figure 5. Three cases are shown: full Class A, Class AB, and Intermediate bias between the two extremes.

The tests for Figures 4a, 4c and 4d were made with a single-ended 1kHz source driving the input and/or output to a signal level of +10dBV regardless of gain or attenuation. This is 10dB below clipping.

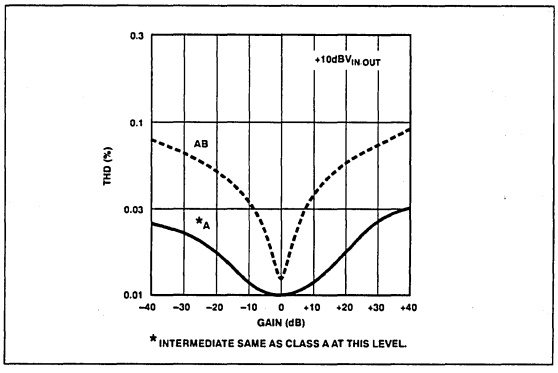


FIGURE 4a: *VCA THD Performance Curves*

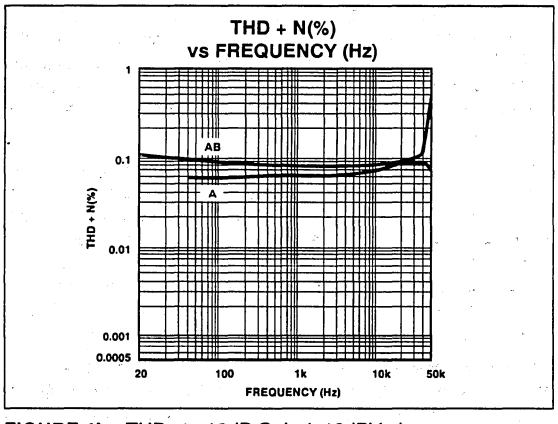


FIGURE 4b: *THD at +10dB Gain (+10dBV$_{IN}$)*

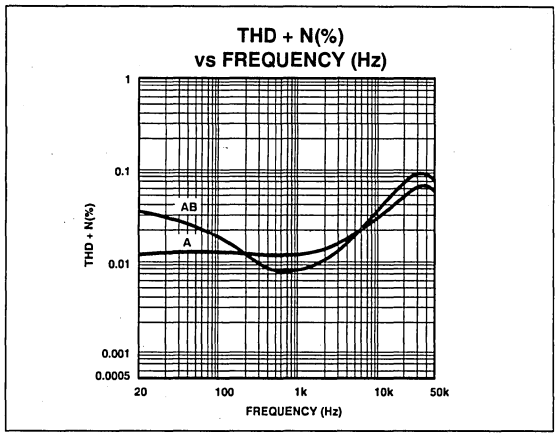


FIGURE 4c: *THD at 0dB Gain*

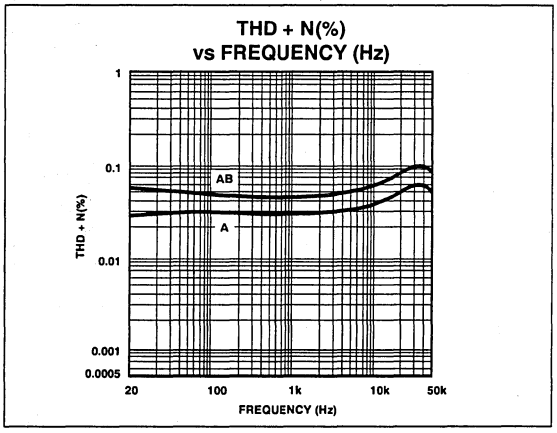


FIGURE 4d: *THD at –10dB Attenuation*

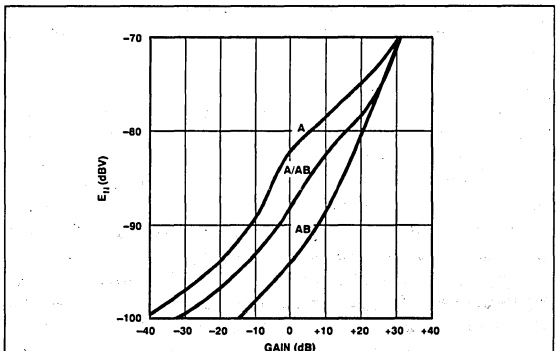


FIGURE 5: *VCA Noise vs. Gain (20kHz) Bandwidth*

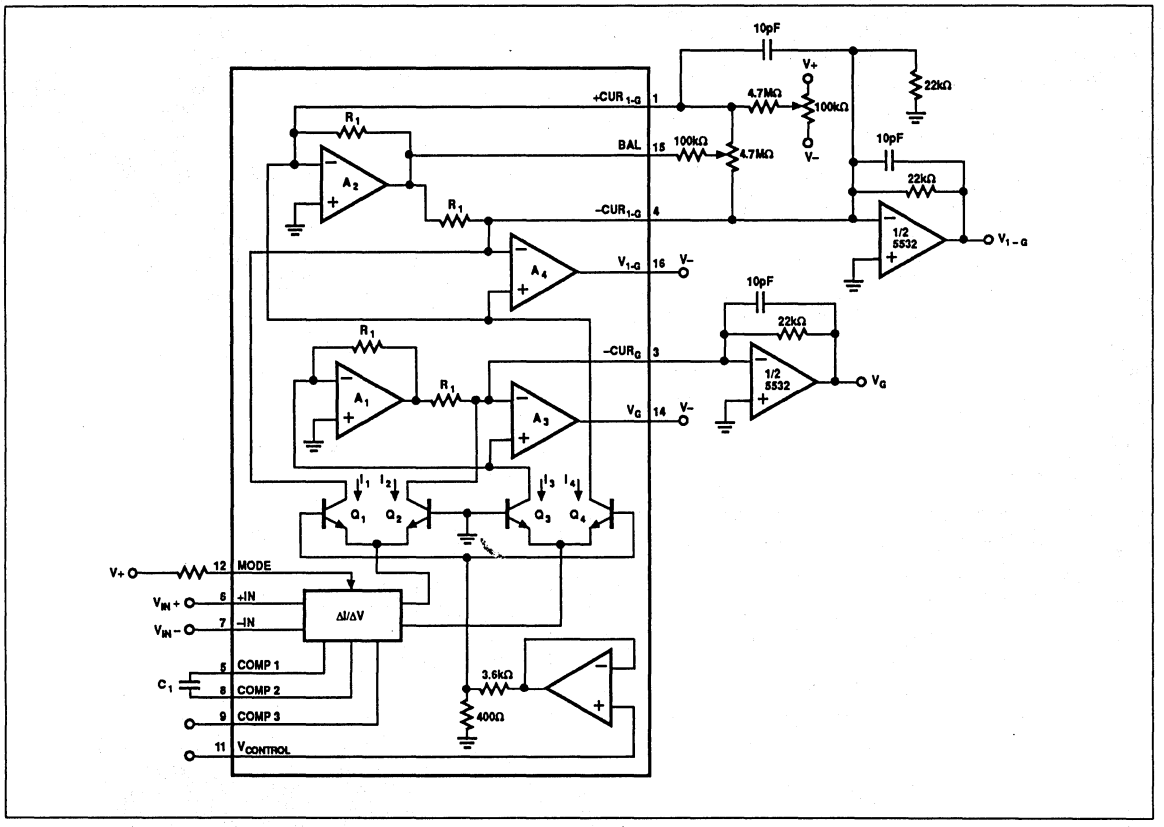


FIGURE 6: *Outboard OVCE*

COMPENSATION

To ensure stability when driving some distortion analyzers, it was found necessary to add a 300pF capacitor between pin 12 and GND in Figure 3a as shown. This is because high-gain preamp and AGC circuits in such measuring systems can cause ground loop problems which can lead to instability and false distortion readings. The output can drive capacitive loads of up to 100pF with little or no degradation in performance.

BASIC OVCE CONNECTIONS

Figure 6 shows the SSM-2014 as an operational voltage-controlled element with outboard current-to-voltage converter amplifiers. This diagram shows the SSM-2014 with uncommitted inputs and outputs and forms only the core of the application circuits to follow. Feedback is required to actually implement any given function. Note that Figure 6 uses an external 5532 op amp and has somewhat better output drive, distortion and noise performance. Pins 14 and 16 are tied to V– which disables the onboard op amps. The outputs used for feedback connections are now at the outputs of the external op amps and are now called V_G and $V_{1\text{-}G}$. Use of a 5532 is recommended since use of a TL072 would require that the SSM-2014 be somewhat overcompensated resulting in reduced bandwidth.

OVCE OPERATION

The complete SSM-2014 is a combination of a VCA structure and an operational amplifier. To simplify analysis, assume the op amp portion has infinite gain. (The finite gain limitations of the OVCE cause substantially the same problems as are found with conventional op amps and can be handled and appreciated in the same way.) This means we can apply the same rules used for the ideal op amp.

Since this device is intended for use only with negative feedback, the infinite gain assumption yields the usual contraint that in any closed-loop configuration, the voltage between the + and – inputs is zero. This is the same assumption that is typical of op amps where both inputs are forced to be at the same potential. In addition to this, we have the VCA constraint, that the ratio of the V_G and $V_{1\text{-}G}$ outputs are always e^{-aV_C}, where "a" is about 4 at room temperature, regardless of the configuration.

These two assumptions make calculation of the transfer characteristics simple for any configuration. Note that the VCA/VCP connections of Figures 7, 8, 9 and 12 resemble non-voltage-controlled functions implemented with op amps.

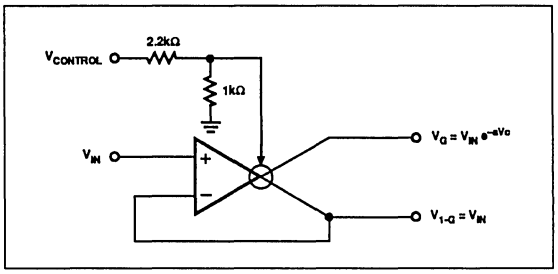


FIGURE 7: *Noninverting VCA*

VCA/VCP FEEDBACK CONNECTIONS

For the following examples, the core configuration of Figure 6 will be used. First, examine the feedback connection for the noninverting VCA of Figure 7. Here, the op amp assumption guarantees that the V_{1-G} output exactly follows the input, while the V_G output tracks the input with a gain of e^{-aV_C}. This means that this circuit simultaneously implements a voltage follower and a true exponential VCA.

Grounding the noninverting input and applying feedback as shown in Figure 8 yields the inverting VCA amplifier. Outputs are now $-V_{IN}$ and $-V_{IN}$ (e^{-aV_C}).

COMPENSATION

To ensure stability for VCA operation as described above, a capacitor greater than or equal to 220pF should be placed between pin 5 (COMP 1) and pin 8 (COMP 2). Pin 9 (COMP 3) should be left open.

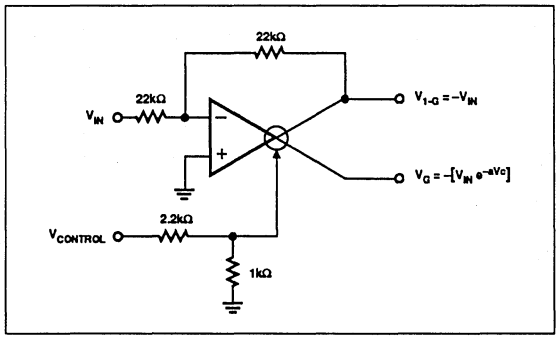


FIGURE 8: *Inverting VCA*

PANNING CIRCUIT

Figure 9 shows the SSM-2014 used as a voltage-controlled panning circuit. This is accomplished by feeding back signals from both the V_{1-G} and V_G outputs simultaneously. In this circuit, the signal at the inverting input is the average of the two outputs due to the balanced feedback (identical resistors). The assumption that the inputs are held to the same potential, therefore,

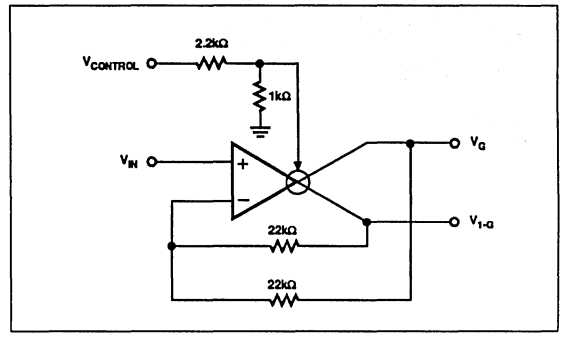


FIGURE 9: *SSM-2014 or OVCE as a Noninverting Voltage-Controlled "Panning" Circuit*

says that the average of the two outputs is always equal to the input. Because the ratio of the two outputs can be made to cover many orders of magnitude, it is possible to "pan" the input signal from the V_{1-G} output to the V_G output through the use of the control voltage. Setting V_C to zero is the "center" position, since the ratio is unity there. Positive control voltages will increase V_{1-G} and attenuate the V_G output. Conversely, setting V_C to negative voltages will increase V_G and attenuate V_{1-G}.

Noise and distortion performance are completely complementary where noise is lower and THD is higher in Class AB and the reverse for Class A. Figures 10 and 11 show the distortion and noise at the V_G or V_{OUT} (right) output only, where V_{1-G} and V_{OUT} (left) are symmetrical. Figure 11 shows noise vs. gain in Class AB bias only.

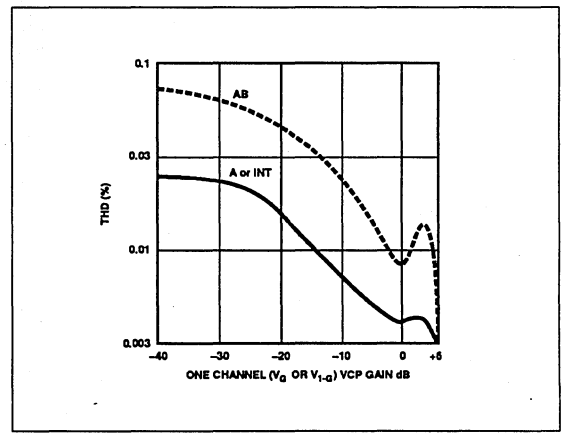


FIGURE 10: *VCP Typical THD Performance Curves (1kHz +10dB V_G/V_{1-G}) Noninverting*

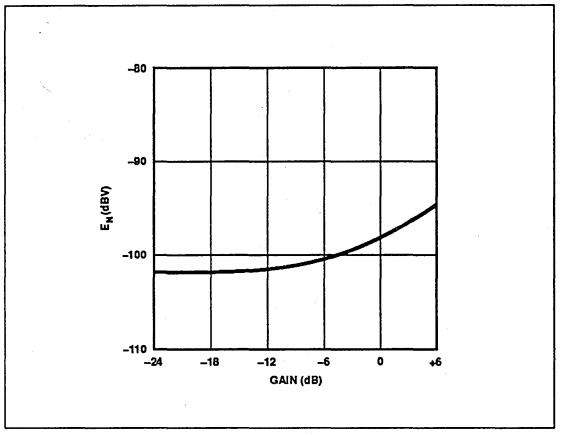


FIGURE 11: *Noise Performance of Circuit of Figure 10 (20kHz Bandwidth) Noninverting*

In Class AB operation at a maximum gain of unity, the variable compensation is not required and gain-bandwidth product is not of concern. Slew rate is 6V/μs for the inverting configuration and approximately 3V/μs for the noninverting connection (Figure 9). Control feedthrough for the voltage-controlled panner is 500μV_{p-p} with a 100Hz sine wave varying the gain from maximum to –40dB.

This panning circuit may be configured for inverting or noninverting operation in the same way that any operational amplifier circuit might be used. Grounding the +input and feeding the signal input through a resistor to the – input creates the inverting analogy to this example (Figure 12). The SSM-2014 is noteworthy for truly exceptional noise and distortion performance for the VCP, one of its unique uses.

COMPENSATION

For best stability when used in panning circuits, connect a capacitor greater than or equal to 330pF across pin 5 (COMP 1) and pin 8 (COMP 2) while grounding pin 3 (COMP 3).

VCA PREAMPLIFIER

A simple variation of the above VCA example is given in Figure 13 which shows the SSM-2014 configured as a full VCA preamp accepting both high and low impedance inputs simultaneously. Here, the feedback from the V_{1-G} output to the – input causes the V_{1-G} output to follow the input with a fixed gain, which is about 10 (20dB) inband. (Inband is the portion of the input signal at frequencies above the R_1, C_1 cutoff.) This behaves in exactly the same manner as the output of a noninverting operational amplifier. At the same time, however, the V_G output is voltage-controlled with a gain of e^{-aV_C} times the V_{1-G} output or $10e^{-aV_C}$ times the input inband signal.

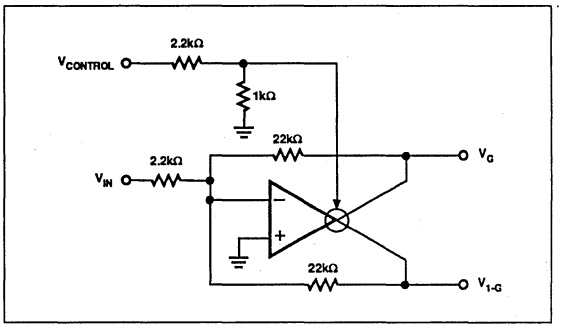


FIGURE 12: *VCA as an Inverting Voltage-Controlled "Panning" Circuit*

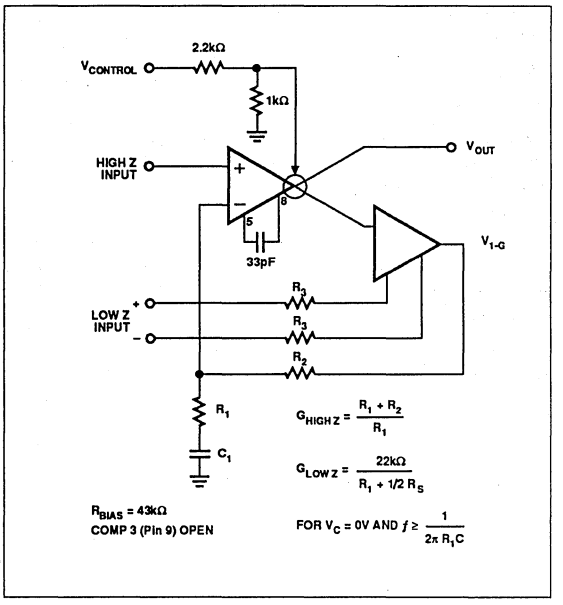


FIGURE 13: *Voltage-Controlled Preamplifier Accepts Both High and Balanced Low Impedance Inputs*

Performance curves for the VCA preamp are shown in Figures 14 and 15. Measurements for this data were taken with a signal applied to the high impedance input using the INT (Intermediate) bias setting. Performance in Class A or AB will vary from the INT setting in practically the same way as for the VCA. Distortion measurements were made by configuring the VCA to drive one or both outputs to +10dBV with a 1kHz sine wave applied. Auxiliary specifications are quite good for the device operating in this configuration. The effective gain-bandwidth product was measured to be 12MHz with an accompanying slew rate of about 10V/μs. The control feedthrough was measured at 3mV peak-to-peak, with a 100Hz sine wave varying gain from +40dB to 0dB. Tests were also conducted with a balanced 600Ω input using more than 70dB of gain which showed essentially the same noise and distortion.

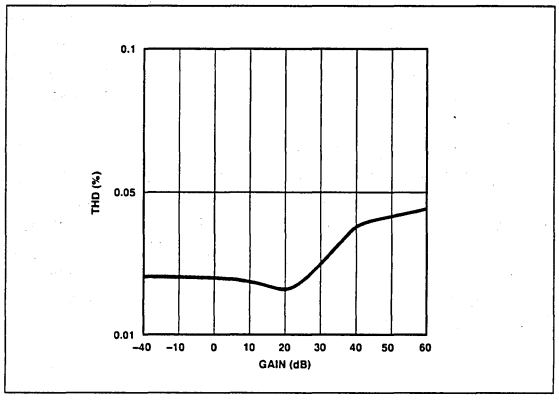


FIGURE 14: *Preamp THD Performance vs. Gain*

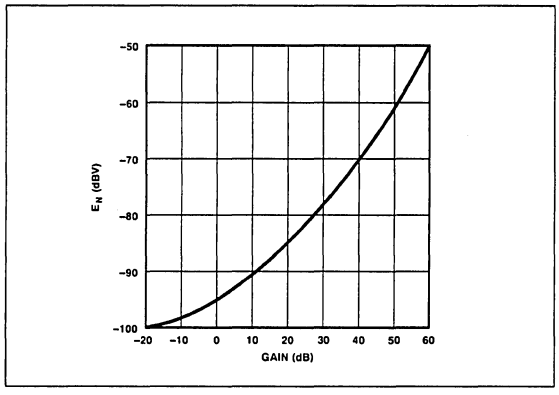


FIGURE 15: *Preamp Noise Performance vs. Gain (20kHz Bandwidth)*

AUTOMATIC GAIN CONTROL

An automatic gain control circuit can easily be implemented using the SSM-2014 and DAC-08 8-bit DAC. In this type of application, a DAC-08 could be digitally controlled to set the control voltage for the desired gain or attenuation with the SSM-2014 configured as a VCA or voltage-controlled preamplifier.

TRIMMING THE SSM-2014

Two TRIMPOTs™ are shown in each circuit. Figure 16 shows the basic scheme for trimming symmetry and offset. Both trims affect offset and control feedthrough while the symmetry trim also affects distortion. The waveform symmetry trim is mandatory for Class AB operation, but may not be required for less critical Class A-only operation. Offset trimming is needed when it is necessary to improve the untrimmed control feedthrough performance in either Class A or AB operation.

TRIM PROCEDURE

1. Symmetry trim – perform first if used. Apply a 1kHz sine wave at +10dBV with the amplifier set at unity gain.
2. Adjust symmetry trim to minimize distortion.
3. Ground input signal and apply a 100Hz sine wave to the control port. The sine wave should have its high and low peaks correspond to the highest gain and 30dB attenuation, respectively.
4. Adjust the offset trim to null control feedthrough.
5. Further reduction of control feedthrough can be achieved by a slight readjustment of the symmetry trim when in Class A operation. (This is not useful for Class AB.)
6. When a level detector switching scheme is used to select Class A and Class AB operation, choose the Class AB symmetry null point. This is the best choice since control feedthrough null points for Class A and Class AB operation do not exactly coincide.

As noted in the input section, the DC blocking capacitor in series with the input will prevent offsets of previous stages from affecting the control feedthrough performance.

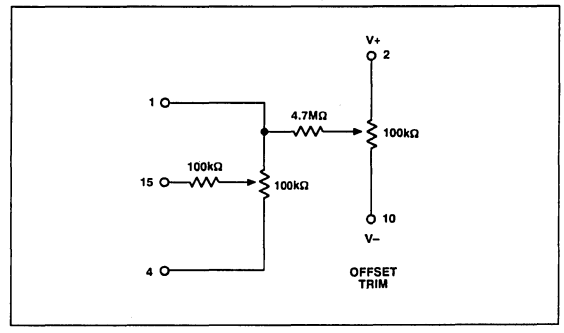


FIGURE 16: *Symmetry and Offset Trimming Scheme*

For many applications such as panning and equalizer circuits, control feedthrough trimming should not be required. Control settings for these circuits are usually established at setup and varied infrequently. In these types of circuits, audible control feedthrough can also be suppressed by inserting a 10 to 20ms time constant in the control signal path.

SELF-CONTAINED OVCE

Figure 17 shows a self-contained OVCE building block. It is used as the core element for VCAs and panning circuits in a similar fashion to the out-board OVCE element of Figure 6. Unlike Figure 6, however, this configuration utilizes the on-board op amps and needs only the SSM-2014 for the active electronics. This circuit tends to be more sensitive to oscillation than other configurations when prototyped on typical proto boards or even copper-clad vector boards. For this reason, use of the SSM-2014 evaluation board is recommended.

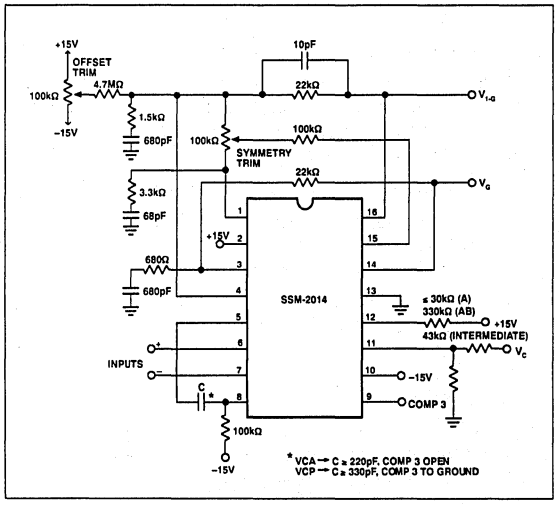


FIGURE 17: *Self-Contained OVCE*

FADER AUTOMATION SYSTEMS

The SSM-2014 lends itself well to fader automation applications. The circuit of Figures 3a and 3b is the most common where simple gain control would be used to amplify or attenuate signals in multi-channel systems. As an example, an SSM-2300 8-channel multiplexed sample-and-hold could be used along with a PM-7541 12-bit DAC to control the gain or attenuation of systems with a multiple of eight channels. Here, the DAC is used to set any given VCA control voltage port for gain or attenuation while the SSM-2300 captures and distributes the appropriate control voltage to the appropriate VCA in a time multiplexed system. With each channel updated by the time distributed SSM-2300 output, a real time fader automation system can be implemented.

DYNAMIC RANGE PROCESSORS

Similar to applications described for the SSM-2120, the SSM-2014 can be used in conjunction with the SSM-2110 level detector to implement virtually any dynamic range processing function. These may include noise reduction systems, compressor/limiters, noise gates, psychoacoustic enhancers and automatic microphone mixers.

SSM-2014 EVALUATION BOARD

An evaluation PCB for the SSM-2014 is available free of charge to qualified OEMs. It permits easy evaluation of the sliding bias control circuit (Figure 1), simple VCA (Figures 3a, 3b), outboard OVCE (Figure 6), and the self-contained OVCE (Figure 17). In order to avoid confusion, please use the PCB marked "Rev 3, 1/90" for proper reference to the appropriate circuits. Contact your local PMI sales office for details.

PMI

Audio Silicon Specialists™

SSM-2018
VOLTAGE-CONTROLLED AMPLIFIER/OVCE

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- Wide Dynamic Range ..... 118dB (Class AB Typ)
  ..... 108dB (Class A Typ)
- Improved THD and IMD over Gain, Attenuation, and Frequency
- Low Control Feedthrough ..... 500µV (Class AB Typ)
  ..... 2mV (Class A Typ)
- Buffered Control Port
- Accepts Low or High Impedance Inputs
- Extended Industrial Temperature Range –40°C to +85°C
- Few External Components
- Low Cost

APPLICATIONS

- Mix Console Fader Automation Systems
- Compressor/Limiters
- Noise Gates
- Noise Reduction Systems
- Telephone Line Interfaces
- Surround Sound Systems
- Automatic or Remote Volume Controllers
- Voltage-Controlled Equalizers
- Voltage-Controlled Panners

ORDERING INFORMATION

PACKAGE PLASTIC 16-PIN	OPERATING TEMPERATURE RANGE
SSM2018P	XIND*

* XIND = –40°C to +85°C

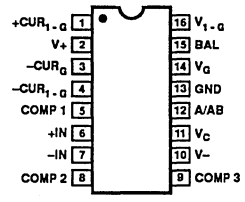
GENERAL DESCRIPTION

The SSM-2018 is a pin compatible upgrade to the SSM-2014, offering improved specifications while maintaining applications flexibility. Improvements include lower noise and lower distortion, particularly over gain and attenuation, with increased bandwidth. PMI's thin-film resistor capability results in fewer required external components than the SSM-2014.

Differential inputs and outputs are provided that permit voltage or current operation. An additional feature is the SSM-2018's programmable gain core, which allows Class A, AB, intermediate, or "sliding bias" operation. As a result, the SSM-2018 is an excellent choice for all common VCA applications, as well as Operational Voltage-Controlled Element (OVCE) functions such as voltage-controlled panners and equalizers.

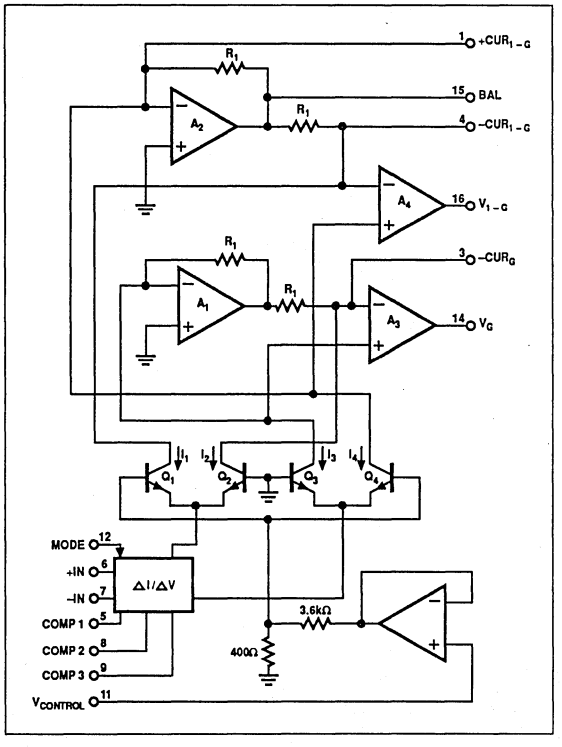
Combined with a PM-7524 DAC and SSM-2300 8-channel multiplexed sample-and-hold, the SSM-2018 enables the design of high performance fader automation systems with few components. The SSM-2018 and SSM-2110 can be used as the nucleus of a state-of-the-art dynamic range processor.

PIN CONNECTIONS



16-PIN PLASTIC DIP
(P-Suffix)

BLOCK DIAGRAM



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

PMI

Audio Silicon Specialists™

SSM-2024
QUAD CURRENT-CONTROLLED AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Four VCAs in One Package
- Ground Referenced Current Control Inputs
- 82dB S/N at 0.3 % THD
- Full Class A Operation
- –40dB Control Feedthrough (Untrimmed)
- Easy Signal Summing
- 6% Gain Matching

APPLICATIONS

- Electronic Musical Instruments
- Noise Gating
- Compressor/Limiters
- Signal Mixing
- Automatic Gain Control
- Voltage-Controlled Oscillators

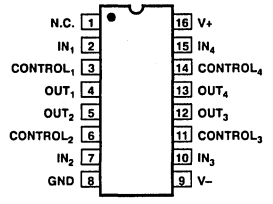
ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	
SSM2024P	–10°C to +50°C

GENERAL DESCRIPTION

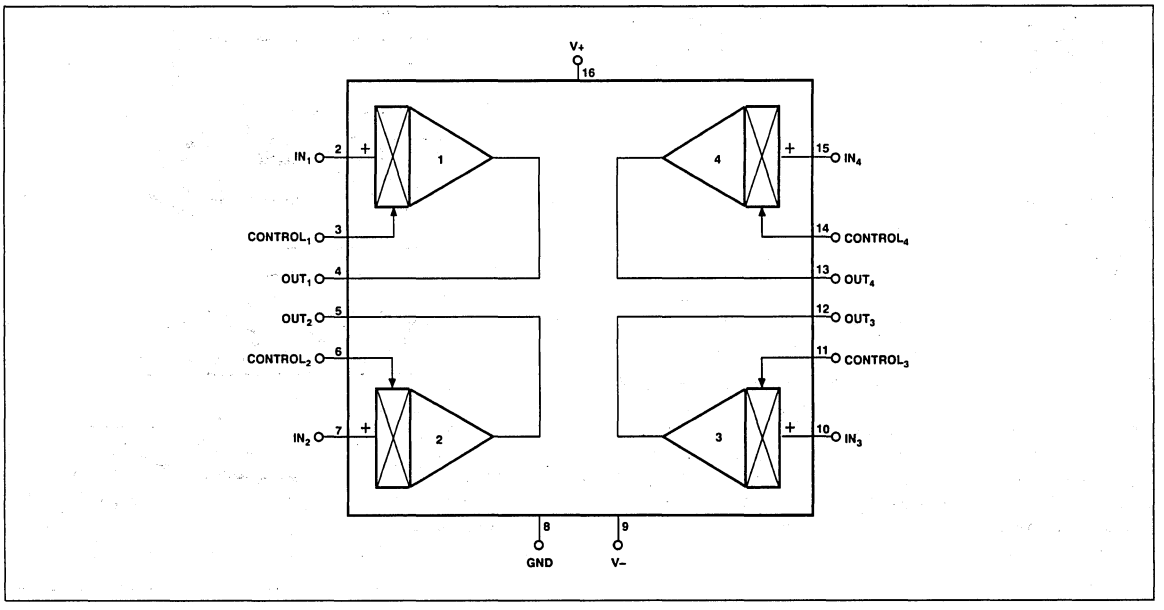
The SSM-2024 is a quad Class A noninverting current-controlled transconductance amplifier. Each of the four VCAs is completely independent and includes a ground referenced linear current gain control. These voltage-in/current-out amplifiers offer over 82dB S/N at 0.3% THD. Other features include low control voltage feedthrough and minimal external components for most applications. With four matched VCAs in a single IC, the SSM-2024 provides a convenient solution for applications requiring multiple amplifiers. The pinout groups the four outputs for easy signal summing for circuits such as four-channel mixers.

PIN CONNECTIONS



16-PIN PLASTIC DIP
(P-Suffix)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 36V or ±18V
Junction Temperature ..... +150°C
Operating Temperature Range ..... –10 to +50°C
Storage Temperature Range ..... –65 to +150°C
Maximum Current into Any Pin 10mA
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
14-Pin Plastic DIP (P)	90	47	°C/W

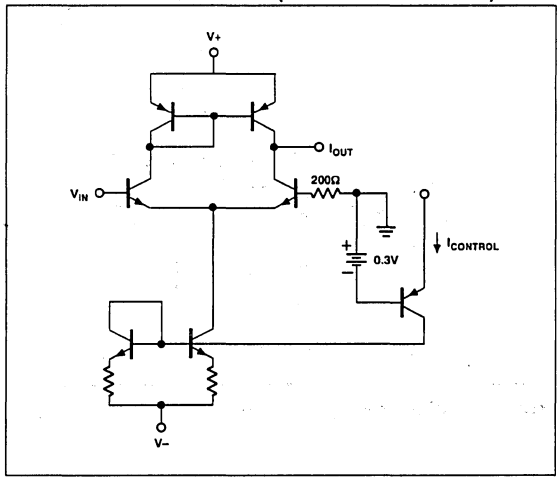
NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			SSM-2024			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Current	$+I_{SY}$	I_{CON} (1-4) = 0 V_S = ±15V I_{CON} (1-4) = 0 V_S = ±16.5V	0.95 1.05	1.40 1.55	1.85 2.05	mA
Negative Supply Current	$-I_{SY}$	I_{CON} (1-4) = 0 V_S = ±15V I_{CON} (1-4) = 0 V_S = ±16.5V	1.05 1.20	1.55 1.65	2.05 2.25	mA
Gain	G	I_{CON} (1-4) = ±500µA	3842	4085	4330	µmhos
Gain Matching	ΔG	I_{CON} (1-4) = ±500µA	–	–	±6	%
Input Offset Voltage	V_{OS}	V_{IN} = 0V I_{CON} (1-4) = ±500µA I_{CON} (1-4) = +250µA	–	±.4	±1.3	mV
Change in Offset Voltage	ΔV_{OS}	+2.5µA ≤ I_{CON} (1-4) ≤ +250µA +250nA ≤ I_{CON} (1-4) ≤ +250µA	– –	±100 ±250	±840 ±840	µV
Output Leakage	I_{OL}	I_{CON} (1-4) = 0	–	0.1	±5	nA
Control Rejection (Untrimmed)	CVR	I_{CON} (1-4) = 500µA V_{IN} (1-4) = 40mV_{p-p}	30	41.5	–	dB
Signal-to-Noise	S/N	V_{IN} (1-4) = 40mV_{p-p}	–	82	–	dB
Distortion	THD	V_{IN} (1-4) = 40mV_{p-p}	–	0.3	–	%
Threshold Input Control Voltage	V_{TCI}	I_{OUT} (1-4) = 0	+160	–	+220	mV

NOTE: Specifications subject to change; consult latest data sheet.

SIMPLIFIED SCHEMATIC (1 OF 4 AMPLIFIERS)



THEORY OF OPERATION

The SSM-2024 is a quad transconductance amplifier. Its voltage-in/current-out transfer functions are controlled by ground referenced linear current inputs. As shown in the simplified schematic, the control current is mirrored in the input stage current source. This sets the operating level for the input differential pair. The operating level established by $I_{CONTROL}$ will determine the slope of the I_{OUT}/V_{IN} transfer characteristic. Each independent device is configured as a noninverting transconductance amplifier and rated for ±15V operation.

SIGNAL INPUTS

The signal inputs offer the best offset and control rejection when shunted with 200Ω to ground. This resistor along with R_{IN} form the voltage divider to scale the input signal. Select R_{IN} to set the maximum operating level for the largest input signal.

This selection will determine the VCAs operating levels which have tradeoffs as shown in Figures 1 and 2. As the input signal level is increased, the effective signal-to-noise and control rejection will increase (improve). However, a larger input signal also means more THD.

The signal at the input of the device will be:

$$V_{IN}' = V_{IN}\left(\frac{200}{R_{IN} + 200}\right)$$

(where V_{IN} is the **applied** input). The circuit transconductance I_{OUT}/V_{IN}' is:

$$g_m = 8.17\ I_{CONTROL} = \frac{I_{OUT}}{V_{IN}'}$$

Therefore, the output current expressed as a function of the control current and the applied input signal is:

$$I_{OUT} = 8.17\ I_{CONTROL} = \left(\frac{200}{R_{IN} + 200}\right) V_{IN}$$

A graph of some typical operating levels is shown in Figure 3. Note this plot is for a general application where

$R_{IN} = R_{CONTROL} = 10k\Omega$

For output voltage vs. V_{IN} see the right axes of the graph using

$R_{OUT} = 10k\Omega$.

CONTROL INPUTS

Each control input is a low impedance, ground referenced linear current control input. When operated in its active region, input impedance is approximately 250Ω. When operating with an applied control voltage, connect a series resistor. Select R_{CON} so $V_{CONTROL}$ max/R_{CON} is no more than 500µA.

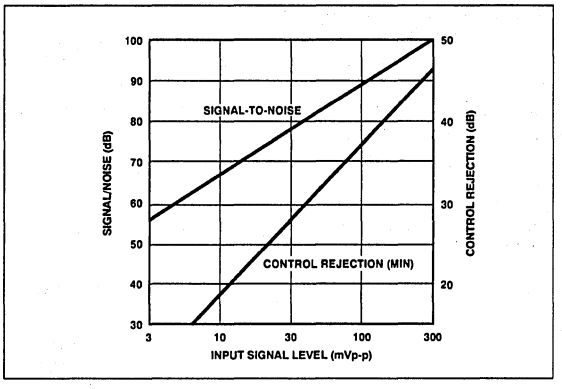


FIGURE 1

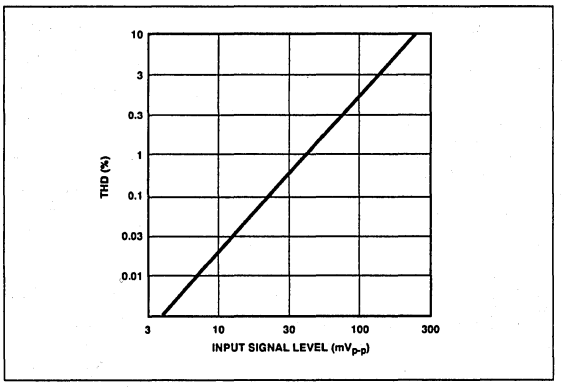


FIGURE 2

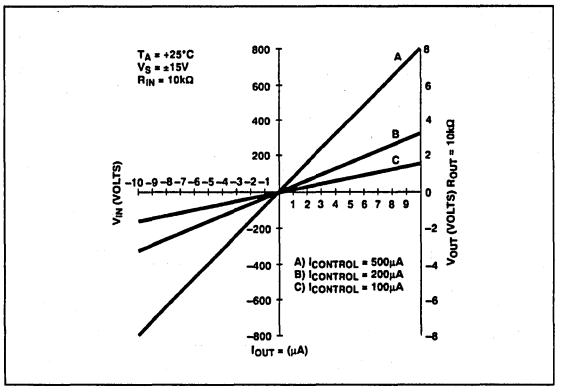


FIGURE 3: *SSM-2024* $g_m = I_{OUT}/V_{IN}$

The VCA will turn completely off as the control voltage drops below approximately 200mV. The control pin can go as low as V– with no adverse effects. Control voltages usually do not exceed 10V. It is possible to operate at higher voltages with current limiting. If the control pin is shorted directly to V+, however, the power dissipation rating of the package will be exceeded within 10 to 20 seconds.

OUTPUTS

The SSM-2024 is a current output device. Operating in the current mode as virtual grounds, the outputs have a voltage compliance of only about 500mV. For large output voltages an op amp is used as a current-to-voltage converter as shown in Figure 4. Selecting R_{OUT} will determine the output voltage range as

$$V_{OUT} = I_{OUT} (R_{OUT}).$$

The outputs can be used directly in many applications where voltage ranges are small, such as the exponential input of a voltage-controlled filter or other logarithmic-control voltage devices.

Outputs are conveniently located together at the center of the package for easy connections in signal summing applications.

DISTORTION

As shown in Figure 2, operation at higher signal levels will increase THD (Total Harmonic Distortion). For many applications such as control paths where a single input signal is being processed, distortion effects are minimal. This is because distortion only slightly alters the harmonic structure of a saw, pulse or triangle shaped waveform already rich in harmonics.

In the final VCA, however, where two or more signals are present, the effects of IMD (Intermodulation Distortion) become more significant. Intermodulation distortion is unwanted sideband signals produced by the circuit at frequencies that are the sums and differences of the harmonics present at the inputs.

In a Class A VCA, IMD will increase with increasing input signal level at the same rate as THD. For such applications, we recommend use of the SSM-2024 at signal levels corresponding to THD of no more than 0.3% (see Figure 2).

APPLICATIONS

The following examples were developed for musical instrument applications but also illustrate general methods of use. Applications for the SSM-2024 are numerous in programmable music systems. A waveform mixer following tone sources is shown in Figure 4. This type of mixer can be configured in several ways to allow the various waveforms and tone sources to be mixed under program control. Choice of mixer configurations depends on system philosophy and the number of tone and noise sources to be considered.

The SSM-2024 can also be used as the final VCA/volume and filter controls. This would make keyboard tracking and envelope sweep programmable.

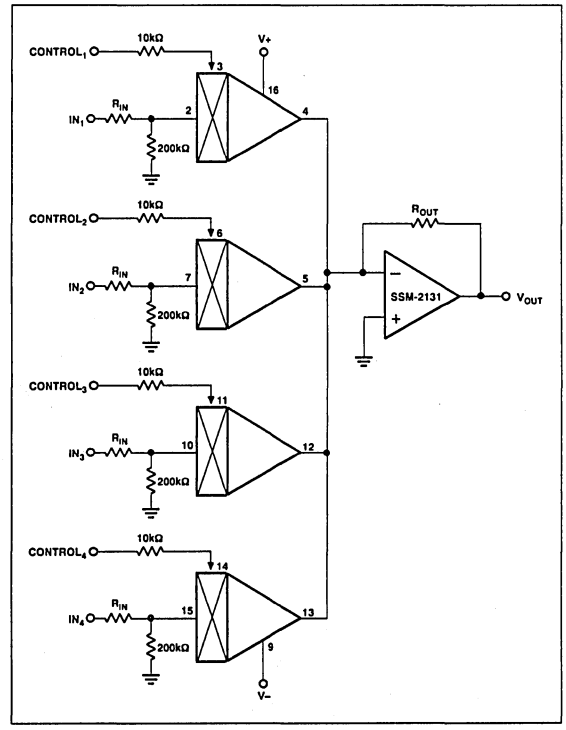


FIGURE 4: *Four-Channel Mixer (4–1)*

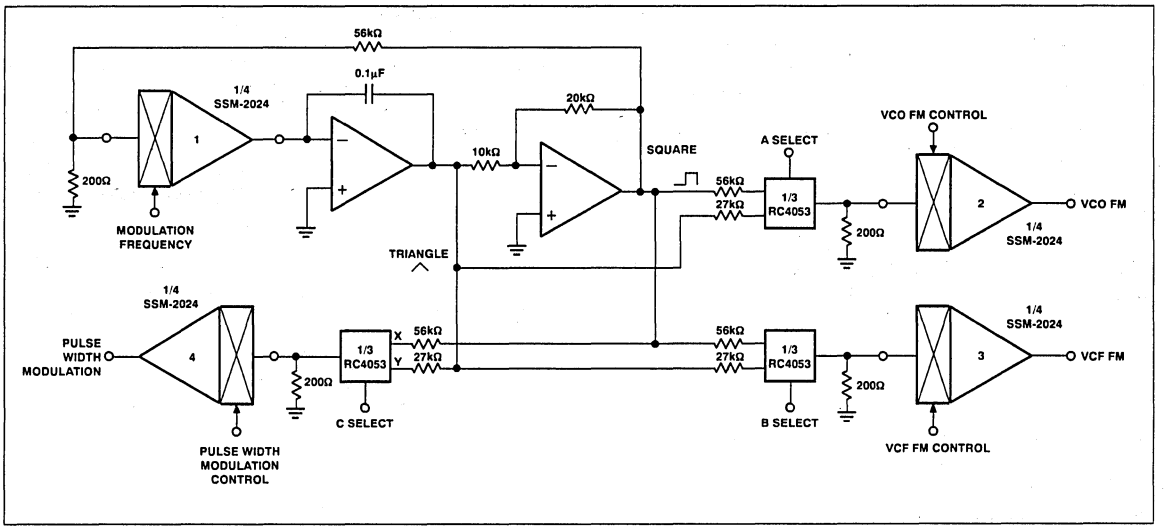


FIGURE 5: *Modulation Oscillator*

A practical modulation oscillator is shown in Figure 5. Here, the device is used in the circuit to control the oscillator frequency and the amount of modulation signal onto the modulation buses.

A VCA with programmable amplitude modulation control is shown in Figure 6. This circuit also exhibits direct interface to the SSM-2044 VCF without adding an op amp or offset adjustments.

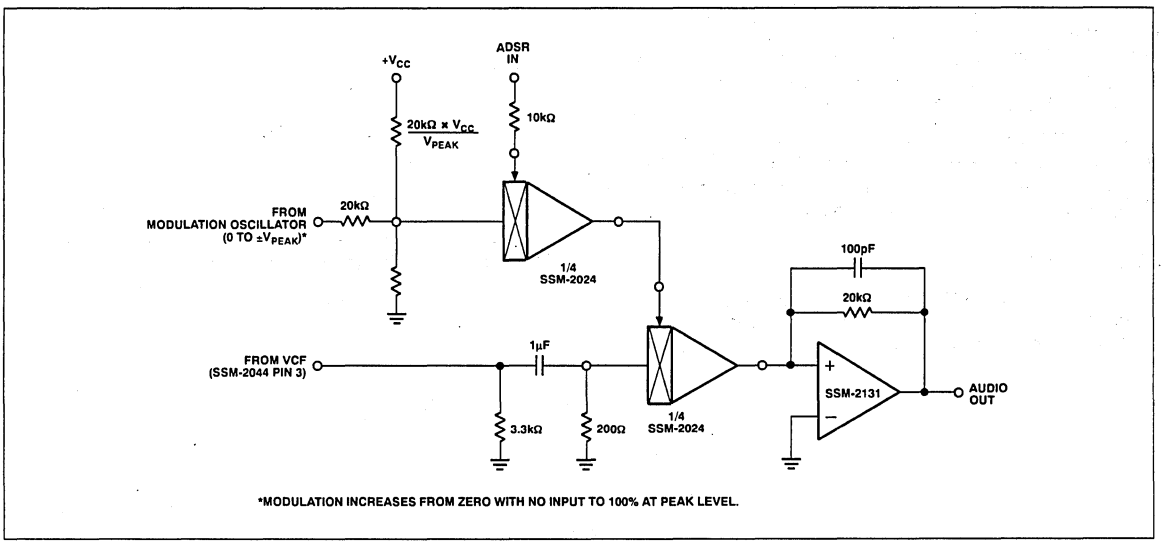


FIGURE 6: *VCA with Amplitude Modulation*

Two of the SSM-2024 channels can be used with the SSM-2220 dual PNP transistor in an exponential cross-fade circuit. Figure 7 shows how the PNP splits a common linear control current according to the bias of the PNP pair. Here, the voltage called "exponential cross-fade control" will determine the relative amount of the two signals at the inputs of the VCAs in the mix.

The transfer characteristic of this circuit is shown in Figure 8. This plot is normalized to the balance point where each VCA has equal current (250μA). This is plotted as the 0dB or unity-gain point. As the control voltage is swept positive or negative, the control current in each VCA is varied logarithmically. As the control voltage is increased, VCA B receives increased current as VCA A's current attenuates at a more rapid logarithmic rate. This applies inversely for decreasing control voltages. At the maximum positive or negative control voltages, VCA B or VCA A receives virtually all 500μA and is 6dB above the balance point.

To operate a single VCA with exponential control sensitivity, simply ground the collector of the unused PNP.

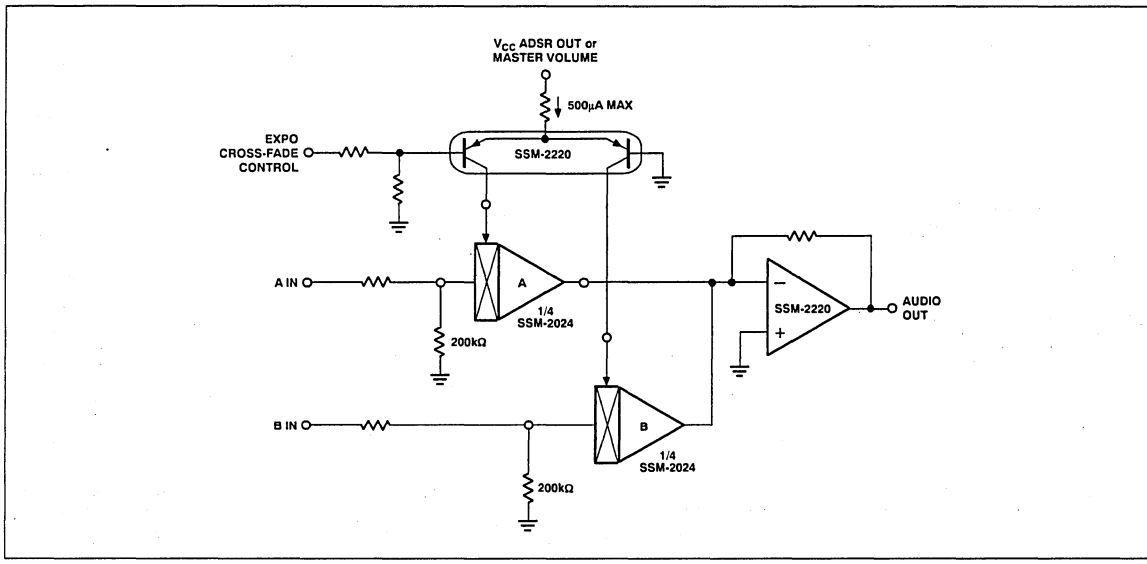


FIGURE 7: *Exponential Cross-Fade Controller*

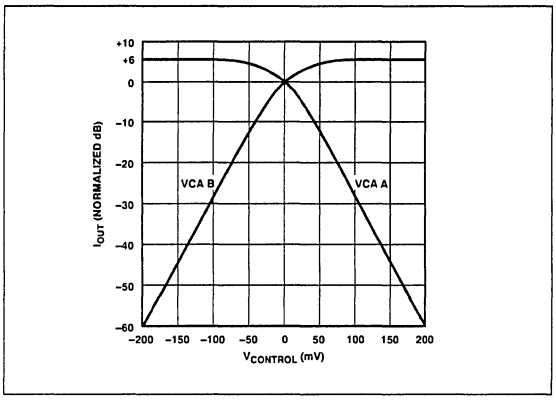


FIGURE 8: *Normalized Transfer Characteristic of a Exponential Cross-Fade Controller*

SSM-2120/SSM-2122

DYNAMIC RANGE PROCESSOR/DUAL VCA

FEATURES

- 0.01% THD at +10dBV In/Out
- 100dB VCA Dynamic Range
- Low VCA Control Feedthrough
- 100dB Level Detection Range
- Log/Antilog Control Paths
- Low External Component Count

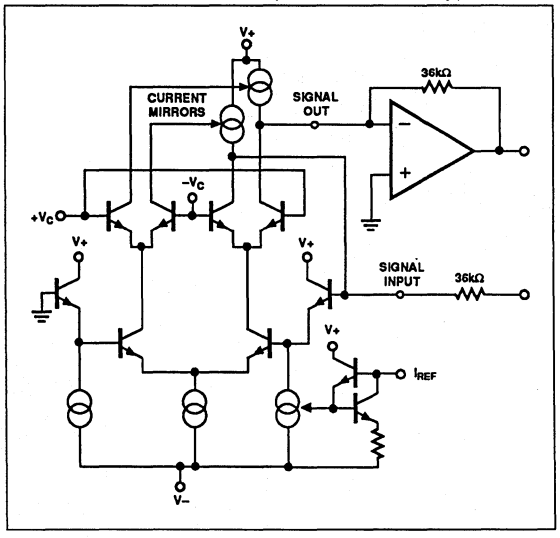
APPLICATIONS

- Compressors
- Expanders
- Limiters
- AGC Circuits
- Voltage-Controlled Filters
- Noise Reduction Systems
- Stereo Noise Gates

ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	PLASTIC 22-PIN	
SSM2122P	SSM2120P	–10°C to +50°C

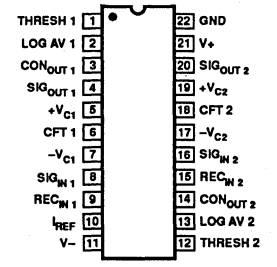
SIMPLIFIED SCHEMATIC (VCA Section Only)



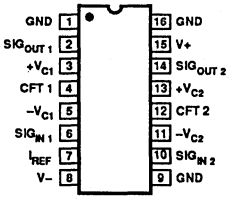
GENERAL DESCRIPTION

The SSM-2120 is a monolithic integrated circuit designed for the purpose of processing dynamic signals in various analog systems including audio. This "dynamic range processor" consists of two VCAs and two level detectors (the SSM-2122 consists of two VCAs only). These circuit blocks allow the user to logarithmically control the gain or attenuation of the signals presented to the level detectors depending on their magnitudes. This allows the compression, expansion or limiting of AC signals, some of the primary applications for the SSM-2120.

PIN CONNECTIONS



SSM-2120
22-PIN PLASTIC DIP
(P-Suffix)



SSM-2122
16-PIN PLASTIC DIP
(P-Suffix)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Operating Temperature Range ..... –10° to +55°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65° to +150°C
Maximum Current into Any Pin 10mA
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Plastic DIP (P)	86	10	°C/W
22-Pin Plastic DIP (P)	70	7	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, $I_{REF} = 200\mu A$, $A_V = 1$, unless otherwise noted.

		SSM-2120/SSM-2122			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY					
Supply Voltage Range		±5	–	±18	V
Positive Supply Current		–	8	10	mA
Negative Supply Current		–	6	8	mA
VCAs					
Max I_{SIGNAL} (In/Out)		±387	±400	±413	µA
Output Offset		–	±1	±2	µA
Control Feedthrough (Trimmed)	$R_{IN} = R_{OUT} = 36k\Omega$, $A_V \leq 0dB \leq -30dB$	–	750	–	µV
Gain Control Range	Unity-Gain	–100	–	+40	dB
Control Sensitivity		–	6	–	mV/dB
Gain Scale Factor Drift		–	–3300	–	ppm/°C
Frequency Response	Unity-Gain or Less	–	250	–	kHz
Off Isolation	At 1kHz	–	100	–	dB
Current Gain	$+V_C = -V_C = 0V$	–0.25	0	+0.25	dB
THD (Unity-Gain)	+10dBV IN/OUT	–	0.005	0.02	%
Noise (20kHz Bandwidth)	RE: 0dBV	–	–80	–	dB
LEVEL DETECTORS (SSM-2120 ONLY)					
Dynamic Range		100	110	–	dB
Input Current Range		0.03	–	3000	μA_{P-P}
Rectifier Input Bias Current		–	4	16	nA
Output Sensitivity (At LOG AV Pin)		–	3	–	mV/dB
Output Offset Voltage		–	±0.5	±2	mV
Frequency Response					
$I_{IN} = 1mA_{P-P}$		–	1000	–	
$I_{IN} = 10\mu A_{P-P}$		–	50	–	kHz
$I_{IN} = 1\mu A_{P-P}$		–	7.5	–	
CONTROL AMPLIFIERS (SSM-2120 ONLY)					
Input Bias Current		–	85	175	nA
Output Drive (Max Sink Current)		5.0	7.5	–	mA
Input Offset Voltage		–	±0.5	±2	mV

NOTE:
1. Specifications are subject to change; consult latest data sheet.

VOLTAGE-CONTROLLED AMPLIFIERS

The two voltage-controlled amplifiers are full Class A current in/current out devices with complementary dB/V gain control ports. The control sensitivities are +6mV/dB and –6mV/dB. A resistor divider (attenuator) is used to adapt the sensitivity of an external control voltage to the range of the control port. It is best to use 200Ω or less for the attenuator resistor to ground.

VCA INPUTS

The signal inputs behave as virtual grounds. The input current compliance range is determined by the current into the reference current pin.

REFERENCE PIN

The reference current determines the input and output current compliance range of the VCAs. The current into the reference pin is set by connecting a resistor to V+. The voltage at the reference pin is about two volts above V– and the current will be

$$I_{REF} = \frac{[(V+) - ((V-) + 2V)]}{R_{REF}}$$

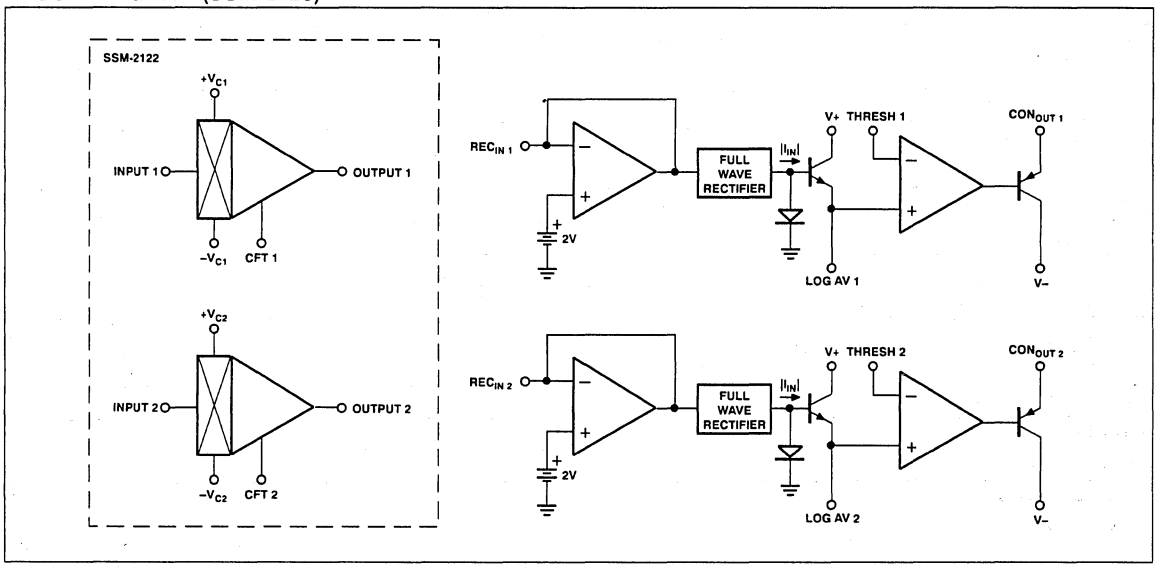
The current consumption of the VCAs will be directly proportional to I_{REF} which is nominally 200μA. The device will operate at lower current levels which will reduce the effective dynamic range of the VCAs. With a 200μA reference current, the input and output clip points will be ±400μA. In general:

$$I_{CLIP} = \pm 2I_{REF}$$

VCA OUTPUTS

The VCA outputs are designed to interface directly with the virtual ground inputs of external operational amplifiers configured as current-to-voltage converters. The outputs must operate at virtual ground because of the output stage's finite output impedance. The power supplies and selected compliance range determines the values of input and output resistors needed. As an example, with ±15V supplies and ±400μA maximum input and output current, choose $R_{IN} = R_{OUT} = 36k\Omega$ for an output compliance range of ±14.4 V. Note that the signal path through the VCA including the output current-to-voltage converter is noninverting.

BLOCK DIAGRAM (SSM-2120)



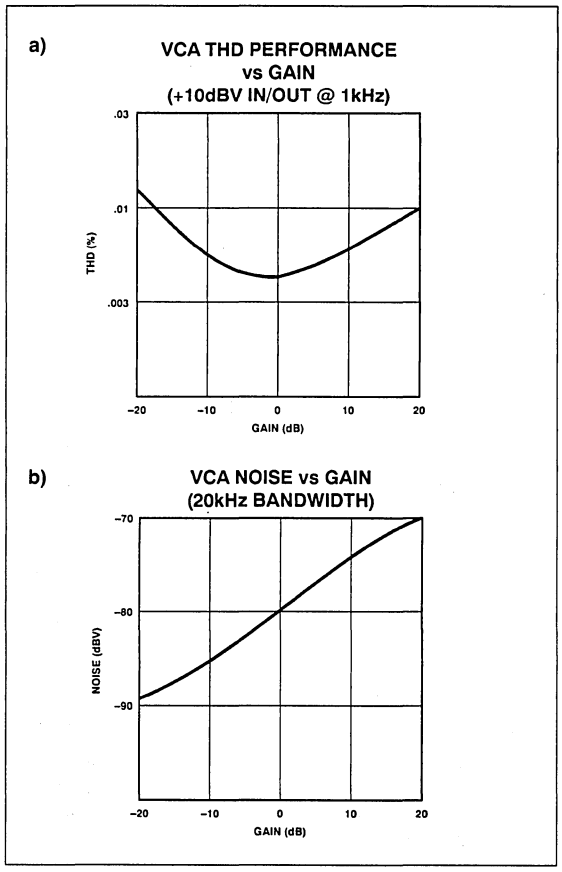


FIGURE 1

VCA PERFORMANCE

Figures 1a and 1b show the typical THD and noise performance of the VCAs over ±20dB gain/attenuation. Full Class A operation provides very low THD.

TRIMMING THE VCAs

The control feedthrough (CFT) pins are optional control feedthrough null points. CFT nulling is usually required in applications such as noise gating and downward expansion. If trimming is not used, leave the CFT pins open.

Trim Procedure

1) Apply a 100Hz sine wave to the control point attenuator. The signal peaks should correspond to the control voltages which induce the VCAs maximum intended gain and at least 30dB of attenuation.

2) Adjust the 50kΩ potentiometer for the minimum feedthrough.

(Trimmed control feedthrough is typically well under $1mV_{RMS}$ when the maximum gain is unity using 36kΩ input and output resistors.)

Applications such as compressor/limiters typically do not require control feedthrough trimming because the VCA operates at unity-gain unless the signal is large enough to initiate gain reduction. In this case the signal masks control feedthrough.

This trim is ineffective for voltage-controlled filter applications.

LEVEL DETECTION CIRCUITS

The SSM-2120 contains two independent level detection circuits. Each circuit contains a wide dynamic range full-wave rectifier, logging circuit and a unipolar drive amplifier. These circuits will accurately detect the input signal level over a 100dB range from 30nA to 3mA peak-to-peak.

LEVEL DETECTOR THEORY OF OPERATION

Referring to the level detector block diagram of Figure 2, the REC_{IN} input is an AC virtual ground. The next block implements the full-wave rectification of the input current. This current is then fed into a logging transistor (Q_1) whose pair transistor (Q_2) has a fixed collector current of I_{REF}. The LOG AV output is then:

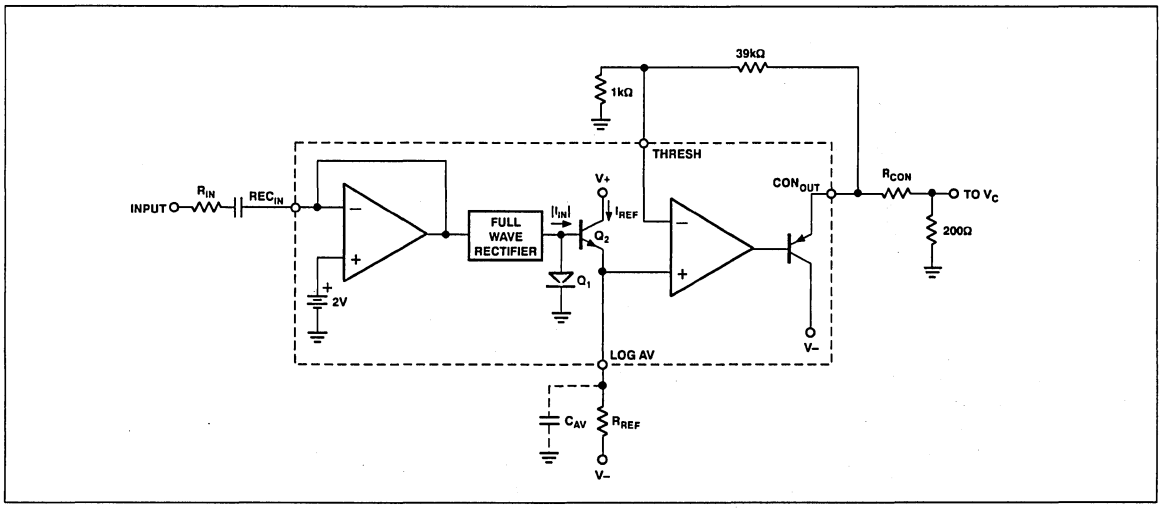


FIGURE 2: *Level Detector*

$$V_{LOG\,AV} = \frac{kT}{q}\ 1n\left(\frac{|I_{IN}|}{I_{REF}}\right)$$

With the use of the LOG AV capacitor the output is then the log of the average of the absolute value of I_{IN}.

(The unfiltered LOG AV output has broad flat plateaus with sharp negative spikes at the zero crossing. This reduces the "work" that the averaging capacitor must do, particularly at low frequencies.)

Note: It is natural to assume that with the addition of the averaging capacitor, the LOG AV output would become the **average of the log of the absolute value of I_{IN}**. However, since the capacitor forces an AC ground at the emitter of the output transistor, the capacitor charging currents are proportional to the **antilog** of the voltage at the base of the output transistor. Since the base voltage of the output transistor is the log of the absolute value of I_{IN}, the log and antilog terms cancel, so the capacitor becomes a linear integrator with a charging current directly proportional to the absolute value of the input current. This effectively inverts the order of the averaging and logging functions. The signal at the output therefore is the **log of the average of the absolute value of I_{IN}**.

USING DETECTOR PINS REC_{IN}, LOG_{AV}, THRESH AND CON_{OUT}

When applying signals to REC_{IN} (rectifier input) an input series resistor should be followed by a low leakage blocking capacitor since REC_{IN} has a DC voltage of approximately 2.1V above ground. Choose R_{IN} for a ±1.5mA peak signal. For ±15V operation this corresponds to a value of 10kΩ.

A 1.5MΩ value of R_{REF} from log average to –15V will establish a 10μA reference current in the logging transistor (Q_1). This will bias the transistor in the middle of the detector's dynamic current range in dB to optimize dynamic range and accuracy. The LOG AV outputs are buffered and amplified by unipolar drive op amps. The 39kΩ, 1kΩ resistor network at the THRESH pin provides a gain of 40.

An attenuator from the CON_{OUT} (control output) to the appropriate VCA control port establishes the control sensitivity. Use 200Ω for the attenuator resistor to ground and choose R_{CON} for the desired sensitivity. Care should be taken to minimize capacitive loads on the control outputs CON_{OUT}. If long lines or capacitive loads are present, it is best to connect the series resistor R_{CON} as closely to the CON_{OUT} pin as possible.

DYNAMIC LEVEL DETECTOR CHARACTERISTICS

Figures 3 and 4 show the dynamic performance of the level detector to a change in signal level. The input to the detector (not shown) is series of 500ms tone bursts at 1kHz in successive 10dBV steps. The tone bursts start at a level of –60dBV (with R_{IN} =10k) and return to –60dBV after each successive 10dB step. Tone bursts range from –60dBV to +10dBV. Figure 3 shows the logarithmic level detector output. The output of the detector is 3mV/dB at LOG AV and the amplifier gain is 40 which yields 120mV/dB. Thus, the output at CON_{OUT} is seen to increase by 1.2V for each 10dBV increase in input level.

DYNAMIC ATTACK AND DECAY RATES

Figure 4 shows the output levels overlayed using a storage scope. The attack rate is determined by the step size and the value of C_{AV}. The attack time to final value is a function of the step size increase. The chart of Figure 5 shows the values of total settling times to within 5, 3, 2 and 1dB of final value with C_{AV} = 10μF. When step sizes exceed 40dB, the increase in settling time for larger steps is negligible. To calculate the attack time to final value for any value of C_{AV}, simply multiply the value in the chart by C_{AV}/10μF.

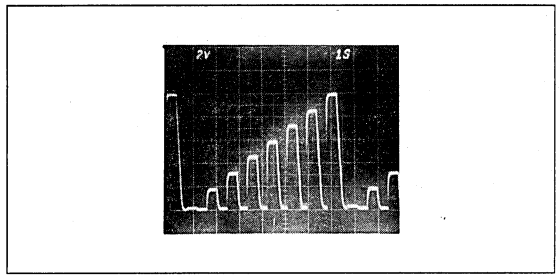


FIGURE 3: *Detector Output*

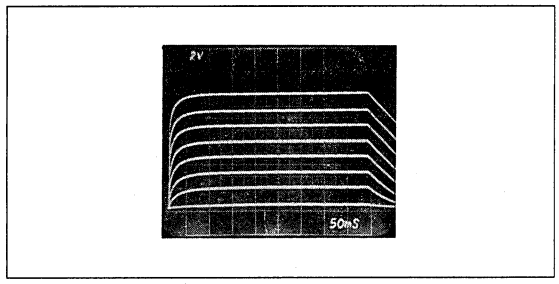


FIGURE 4: *Overlayed Detector Output*

The decay rates are linear ramps that are dependent on the current out of the LOG AV pin (set by R_{REF}) and the value of C_{AV}. The integration or decay time of the circuit is derived from the formula:

$$\text{Decrementation Rate (in dB/s)} = \frac{I_{REF} \times 333}{C_{AV}}$$

	5dB	3dB	2dB	1dB
10dB Step	11.28μs	21.46	30.19	46.09
20dB Step	16.65	26.83	35.56	51.46
30dB Step	18.15	28.33	37.06	52.96
40dB Step	18.61	27.79	37.52	53.42
50dB Step			(+144μs)	
60dB Step			(+46μs)	

FIGURE 5: *Settling Time (t_S) for C_{AV} = 10μF, $t_S' = t_S$ (C_{AV}/10μF)*

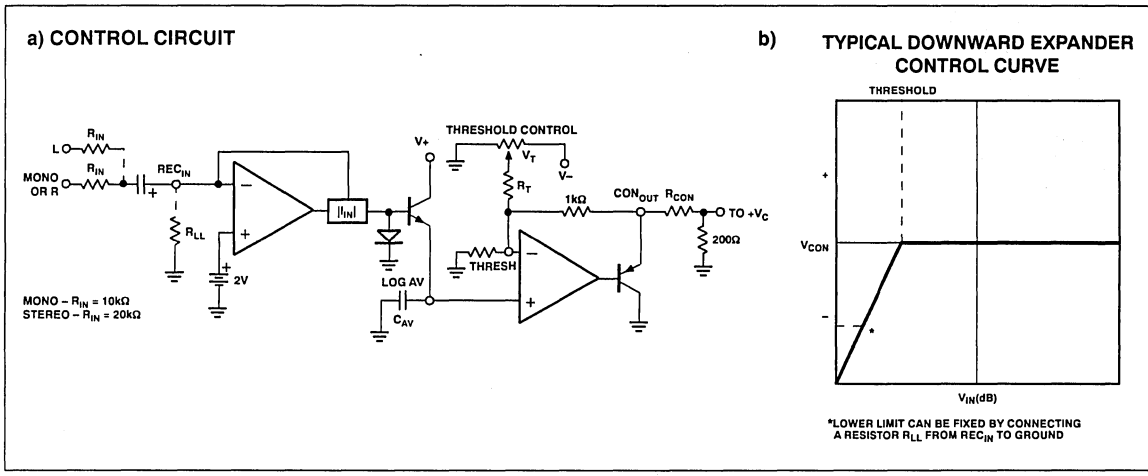


FIGURE 6: *Noise Gate/Downward Expander Control Circuit and Typical Response*

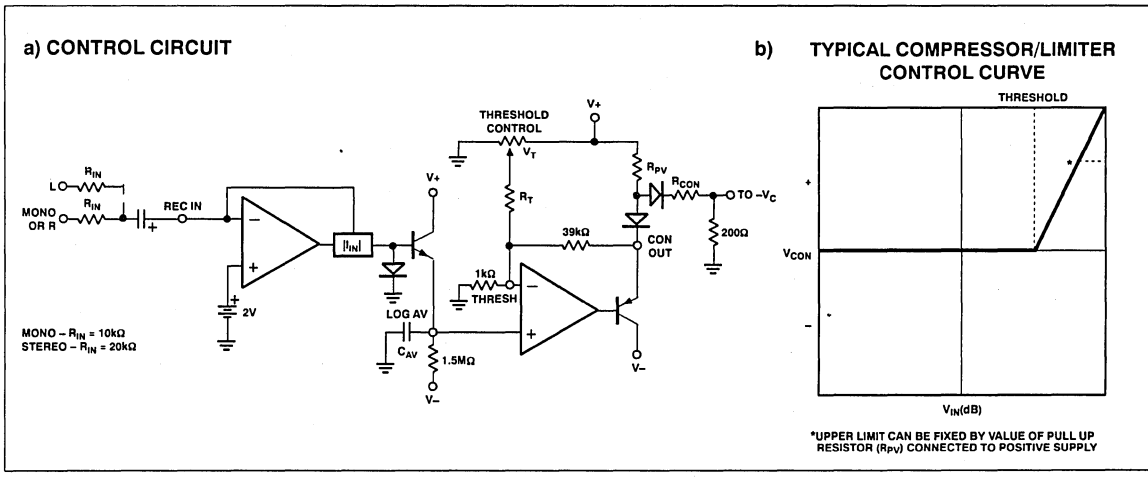


FIGURE 7: *Compressor/Limiter Control Circuit and Typical Response*

APPLICATIONS

The following applications for the SSM-2120 use both the VCAs and level detectors in conjunction to assimilate a variety of functions.

The first section describes the arrangement of the threshold control in each control circuit configuration. These control circuits form the foundation for the applications to follow which include the downward expander, compressor/limiter and compandor.

THRESHOLD CONTROL

Figure 6a shows the control circuit for a typical downward expander while Figure 6b shows a typical control curve. Here, the threshold potentiometer adjusts V_T to provide a negative unipolar control output. This is typically used in noise gate, downward expander, and dynamic filter applications. This potentiometer is used in all applications to control the signal level versus control voltage characteristics.

In the noise gate, downward expander and compressor/limiter applications, this potentiometer will establish the onset of the control action. The sensitivity of the control action depends on the value of R_T.

For a positive unipolar control output add two diodes as shown in Figure 7a. This is useful in compressor/limiter applications. Figure 7b shows a typical response.

Bipolar control outputs can be realized by adding a resistor from the op amp output to V+. This is useful in compandor circuits as

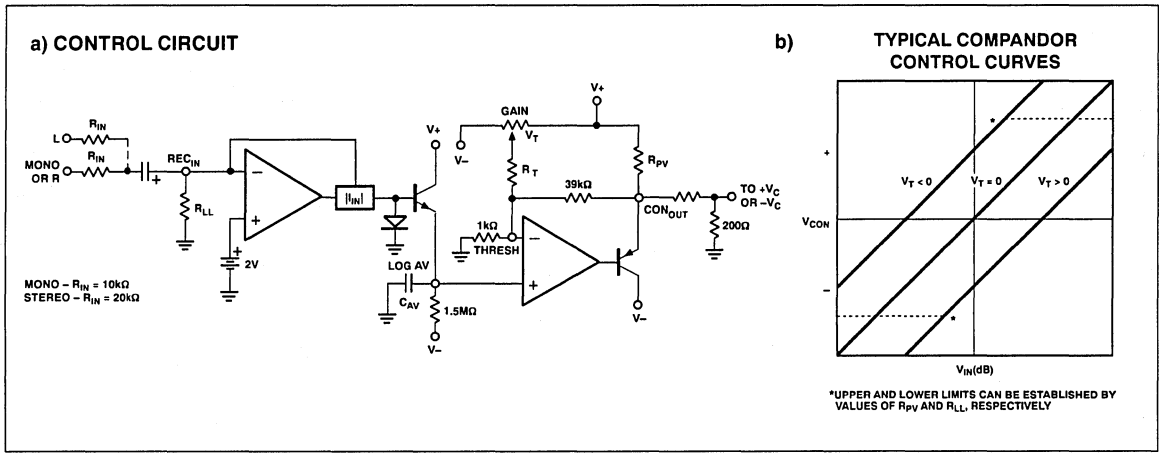


FIGURE 8: *Compandor Control Circuit and Typical Curves*

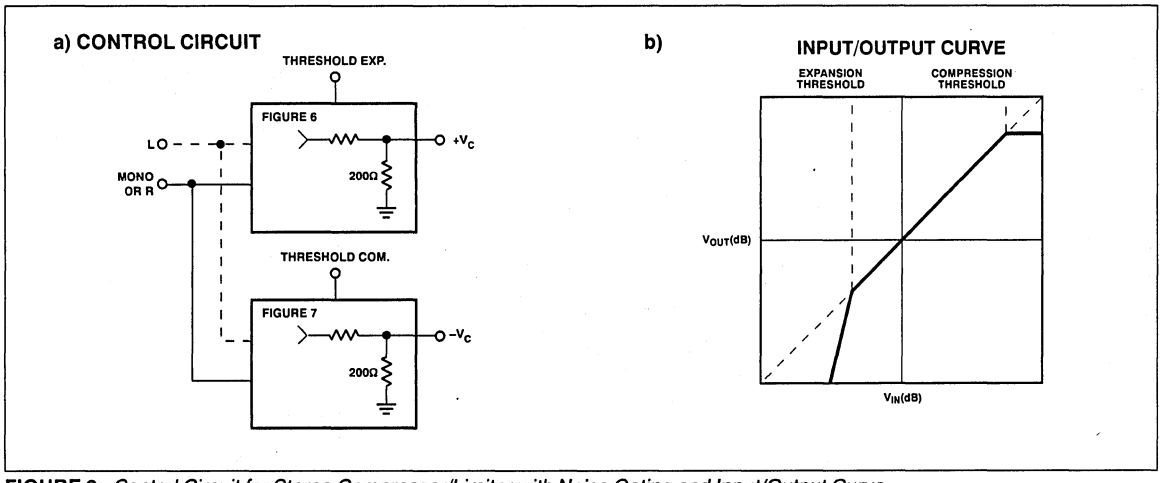


FIGURE 9: *Control Circuit for Stereo Compressor/Limiter with Noise Gating and Input/Output Curve*

shown in Figure 8a, with its response in Figure 8b. The value of the resistor R_{PV} will determine the maximum output from the control amplifier.

STEREO COMPRESSOR/LIMITER

The two control circuits of Figures 6 and 7 can be used in conjunction to produce composite control voltages. Figures 9a and 9b show this type of circuit and transfer function for a stereo compressor/limiter which also acts as a downward expander for noise gating. The output noise in the absence of a signal will be dependent on the noise of the current-to-voltage converter amplifier if the expansion ratio is high enough.

As discussed in the Threshold Control section, the use of the control circuit of Figure 5, including the R_{PV} to V+ and two diodes, yields positive unipolar control outputs.

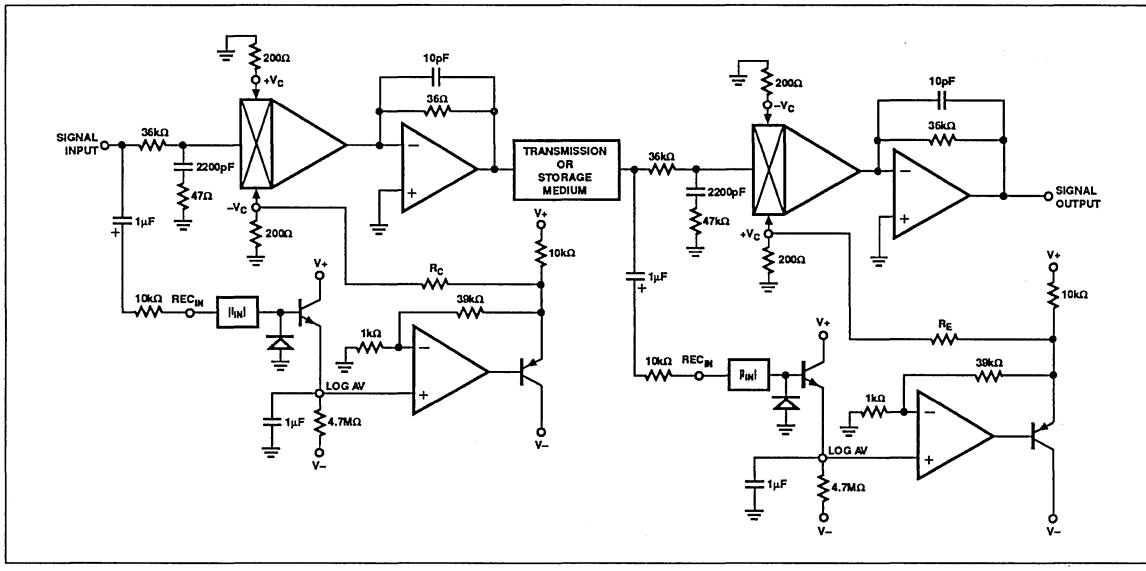


FIGURE 10: *Companding Noise Reduction System*

COMPANDING NOISE REDUCTION SYSTEM

A complete companding noise reduction system is shown in Figure 10. Normally, to obtain an overall gain of unity, the value of R_C is equal to R_E. The values of $R_{C/E}$ will determine the compression/expansion ratio.

Table 1 shows compression/expansion ratios ranging from 1.5:1 to full limiting with the corresponding values of $R_{C/E}$.

An example of a 2:1 compression/expansion ratio is plotted in Figure 11. Note that signal compression increases gain for low level signals and reduces gain for high levels while expansion does the reverse. The net result for the system is the same as the original input signal except that it has been compressed before being sent to a given medium and expanded after recovery. The compression/expansion ratio needed depends on the medium being used. As an extreme example, a household tape player would require a higher compression/expansion ratio than a professional stereo system.

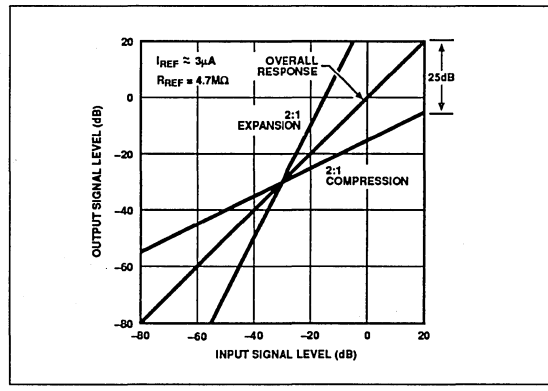


FIGURE 11: *Companding Noise Reduction with 2:1 Compression/Expansion Ratio*

TABLE 1

INPUT SIGNAL INCREASE (dB)	GAIN (REDUCTION OR INCREASE) (dB)	COMPRESSOR ONLY OUTPUT SIGNAL INCREASE (dB)	EXPANDER ONLY OUTPUT SIGNAL INCREASE (dB)	COMPRESSION/ EXPANSION RATIO	$R_{C/E}$ Ω	$\Delta V_{CONTROL}$ (mV/dB)
20	6.67	13.33	22.67	1.5:1	11,800	2.0
20	10.00	10.00	30.00	2:1	7,800	3.0
20	13.33	6.67	33.33	3:1	5,800	4.0
20	15.00	5.00	35.00	4:1	5,133	4.5
20	16.00	4.00	36.00	5:1	4,800	4.8
20	17.33	2.67	37.33	7.5:1	4,415	5.2
20	18.00	2.00	38.00	10:1	4,244	5.4
20	20.00	0	40.00	AGC*/Limiter	3,800	6.0

*AGC for Compression Only

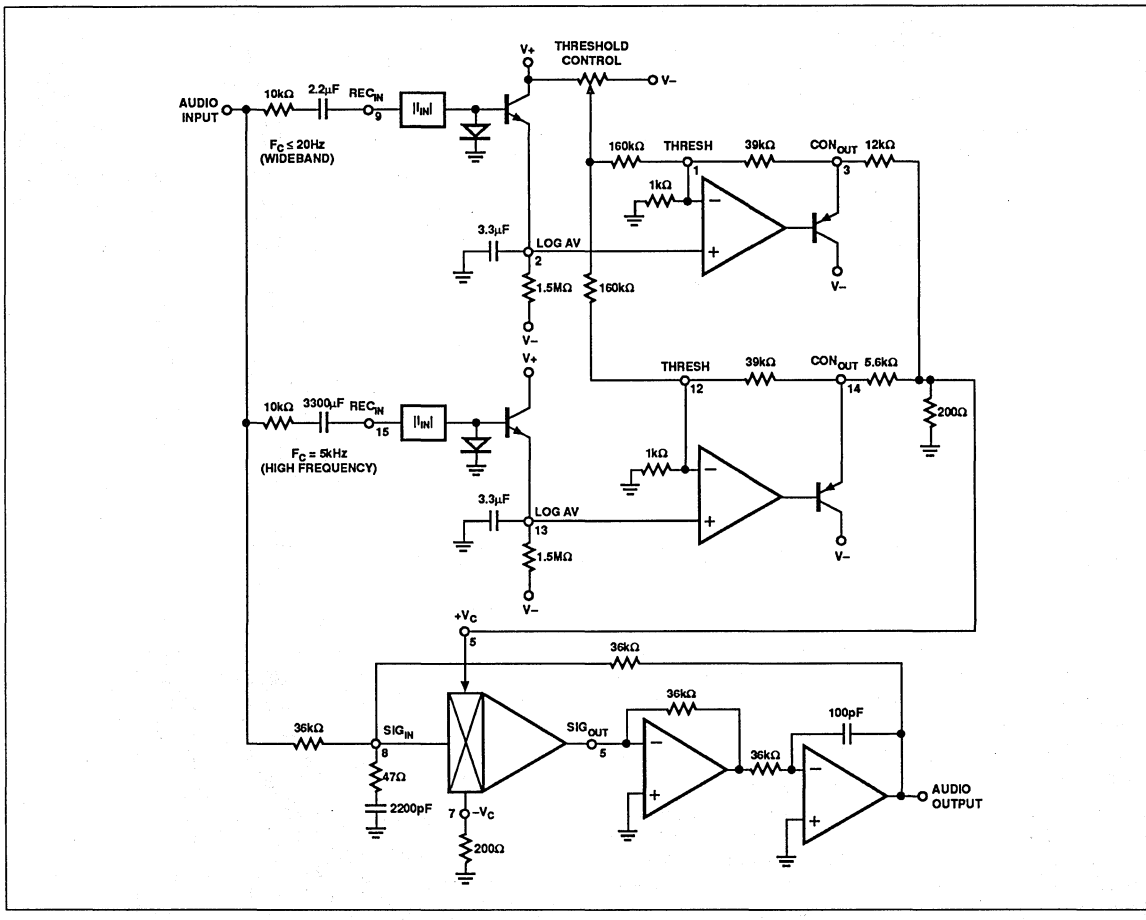
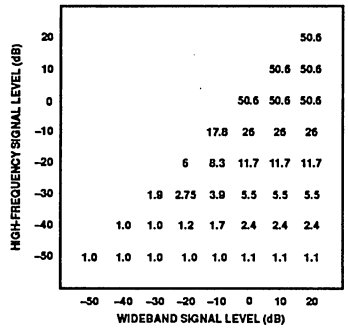


FIGURE 12: *Dynamic Noise Filter Circuit*

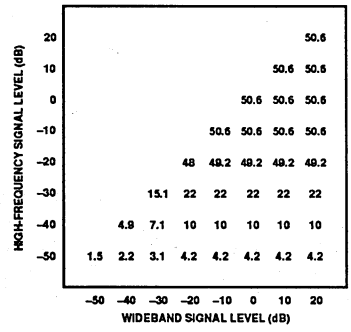
DYNAMIC FILTER

Figure 12 shows a control circuit for a dynamic filter capable of single ended (non-encode/decode) noise reduction. Such circuits usually suffer from a loss of high-frequency content at low signal levels because their control circuits detect the absolute amount of highs present in the signal. This circuit, however, measures wideband level as well as high-frequency band level to produce a composite control signal combined in a 1:2 ratio respectively. The upper detector senses wideband signals with a cutoff of 20Hz while the lower detector has a 5kHz cutoff to sense only high-frequency band signals. This approach allows very good noise masking with a minimum loss of "highs" when the signal level goes below the threshold.

a) V_{THRESH} at V+



b) V_{THRESH} Centered



c) V_{THRESH} at V–

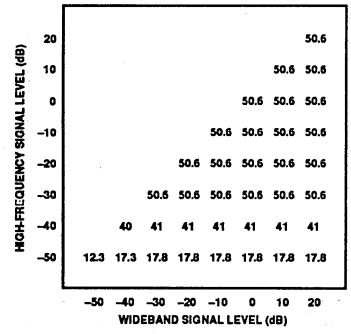


FIGURE 13: *3dB Filter Response*

Figures 13a-c show the filter's 3dB frequency response with the threshold potentiometer at V+, centered, and V–. Data was taken by applying a 300Hz signal to the wideband detector and a 20kHz signal to the high-frequency band detector simultaneously. These figures correspond to filter characteristics for 50dB, 70dB and 90dB dynamic range program source material, respectively. The system could thus treat signals from anything ranging from 1/4" magnetic tape to high-performance compact disc players.

Note that in Figure 13a the control circuit is designed so that the minimum cutoff frequency is about 1kHz. This results from the control circuit detecting the noise floor of the source material.

Dynamic filtering limits the signal bandwidth to less than 1kHz unless enough highs are detected in the signal to cover the noise floor in the mid- and high-frequency range. In this case the filter opens to pass more of the audio band as more highs are detected. The filter's bandwidth can extend to 50kHz with a nominal signal level at the input. At other signal levels with varying high-frequency content, the filter will close to the required bandwidth. Here, noise outside the band is removed while the perceived noise is masked by other signals within the band. Even in this system, however, a certain amount of mid- and high-frequency components will be lost, especially during transients at very low signal levels. This circuit does not address low frequency noise such as "hum" and "rumble."

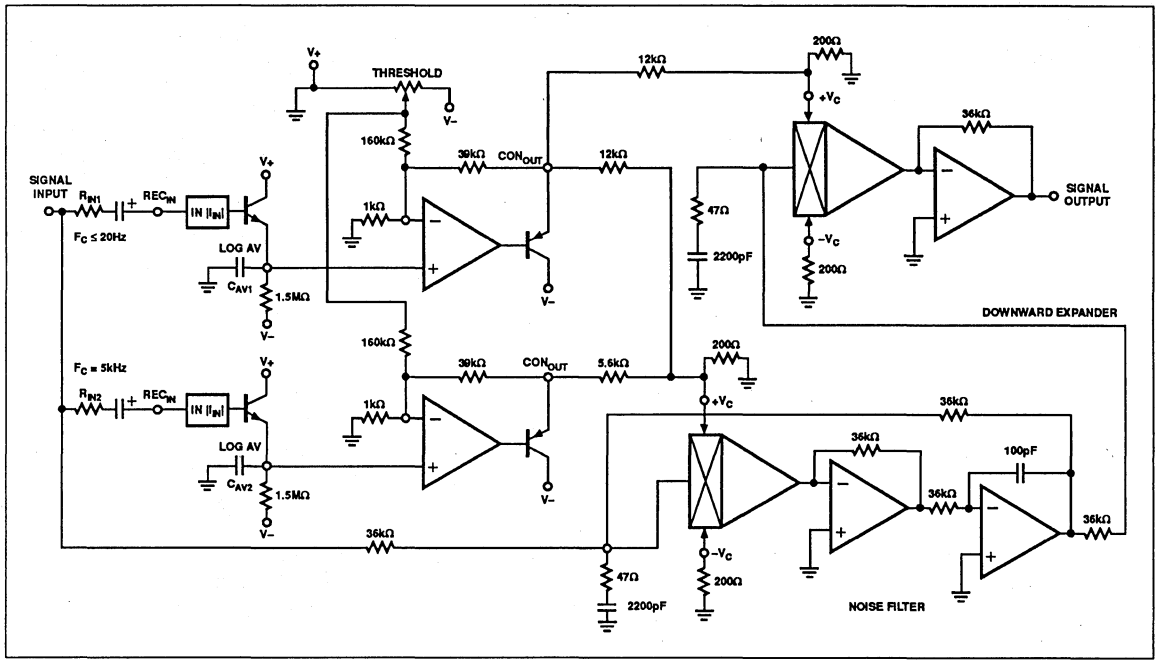


FIGURE 14: *Dynamic Filter with Downward Expander*

DYNAMIC FILTER WITH DOWNWARD EXPANDER

A composite single-ended noise reduction system can be realized by a combination of dynamic filtering and a downward expander. As shown in Figure 14, the output from the wideband detector can also be connected to the $+V_C$ control port of the second VCA which is connected in series with the sliding filter. This will act as a downward expander with a threshold that tracks that of the filter. Although both of these techniques are used for noise reduction, each alone will pass appreciable amounts of noise under some conditions. When used together, both contribute distinct advantages while compensating for each other's deficiencies.

Downward expansion uses a VCA controlled by the level detector. This section maintains dynamic range integrity for all levels above the user adjustable threshold level. As the input level decreases below the threshold, gain reduction occurs at an increasing rate (see Figure 15). This technique reduces audible noise in fade outs or low level signal passages by keeping the standing noise floor well below the program material.

This technique by itself is less effective for signals with predominantly low frequency content such as a bass solo where wideband frequency noise would be heard at full level. Also, since the level detector has a time constant for signal averaging, percussive material can modulate the noise floor causing a "pumping" or "breathing" effect.

The dynamic filter and downward expander techniques used together can be employed more subtly to achieve a given level of noise reduction than would be required if used individually. Up to 30dB of noise reduction can be realized while preserving the crisp highs with a minimum of transient side effects.

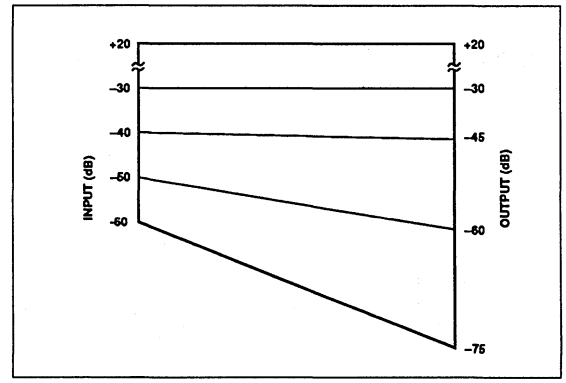


FIGURE 15: *Typical Downward Expander I/O Characteristics at –30dB Threshold Level (1:1.5 Ratio)*

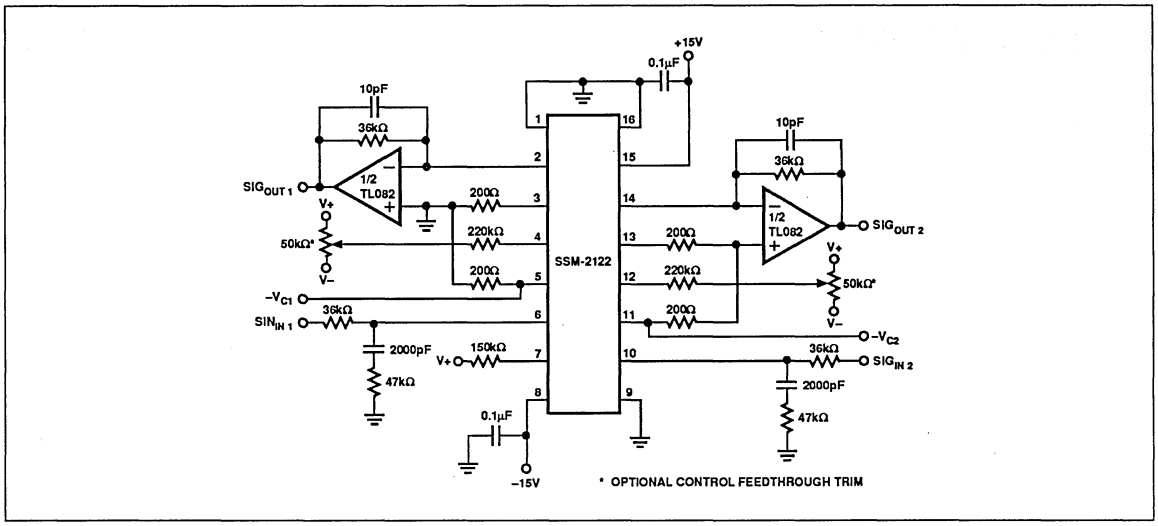


FIGURE 16: *SSM-2122 Basic Connection (Control Ports at 0V)*

FADER AUTOMATION

The SSM-2120 can be used in fader automation systems to serve two channels. The inverting control port is connected through an attenuator to the VCA control voltage source. The noninverting control port is connected to a control circuit (such as Figure 6) which senses the input signal level to the VCA. Above the threshold voltage, which can be set quite low (for example –60dBV), the VCA operates at its programmed gain. Below this threshold the VCA will downward expand at a rate determined by the $+V_C$ control port attenuator. By keeping the release time constant in the 10 to 25ms range, the modulation of the VCA standing noise floor (–80dB at unity-gain), can be kept inaudibly low.

The SSM-2300 8-channel multiplexed sample-and-hold IC makes an excellent controller for VCAs in automation systems.

Figure 16 shows the basic connection for the SSM-2122 operating as a unity-gain VCA with its noninverting control ports grounded and access to the inverting control ports. This is typical for fader automation applications. Since this device is a pinout option of the SSM-2120, the VCAs will behave exactly as described earlier in the VCA section.

The SSM-2122 can also be used with two or more op amps to implement complex voltage-controlled filter functions. Biquad and state-variable two-pole filters offering lowpass, bandpass and highpass outputs can be realized. Higher order filters can also be formed by connecting two or more such stages in series.

PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

SSM-2125

DOLBY* SURROUND PRO-LOGIC MATRIX DECODER

ADVANCE PRODUCT INFORMATION

FEATURES

- Noise Sequencer and Auto-Balance Circuits are Contained On-Chip
- Auto-Balance On/Off Control
- 3- or 4-Channel Pro-Logic Mode (Surround Channel Defeat)
- Selectable Center Channel Modes – Normal, Wide-band, Phantom, Off
- 3- or 4-Channel Noise Sequencer Option
- Selectable Noise Sequencer Time Interval
- Programmable Noise Generator Speaker Sequence
- Direct Path Bypass (Normal 2-Channel Stereo Mode)
- Wide Channel Separation (Any Channel to Another) .....35dB Typ
- Wide Dynamic Range .....100dB Typ
- Low Total Harmonic Distortion .....0.025% Typ
- Available in a 48-Pin Plastic DIP
- CMOS and TTL Compatible Control Logic

APPLICATIONS

- Direct View and Projection TV
- Integrated A/V Amplifiers
- Laserdisc and CD-V Players
- Video Cassette Recorders
- Stand-Alone Surround Decoders

GENERAL DESCRIPTION

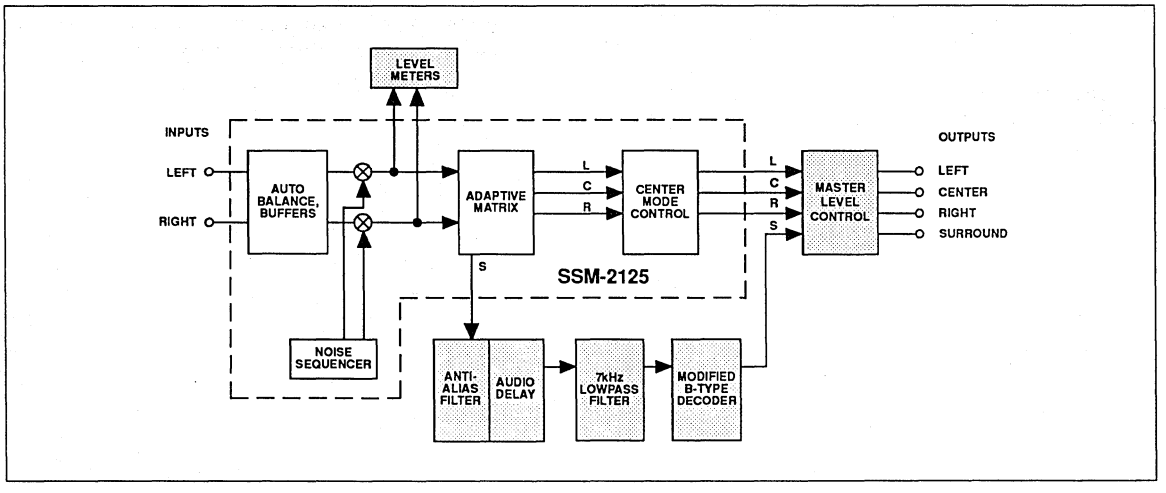
The SSM-2125 is a Dolby Surround Pro-Logic Decoder developed to provide multi-channel outputs from Dolby Surround encoded sources.

Over 2000 major films and an increasing amount of broadcast programming are available in Dolby Surround. Surround encoding is preserved in the stereo audio tracks of normal videodiscs, video cassettes, and television broadcasts, permitting the decoding to multi-channel audio in the home.

Major design considerations of the SSM-2125 are excellent audio performance and a high level of integration. In addition to the Adaptive Matrix and Center Mode Control, also included on-chip are the Automatic Balance Control and Noise Sequencer functions. A complete Pro-Logic system can be realized using the SSM-2125 and few external components. Using PMI's extensive experience in the design of professional audio integrated circuits, the SSM-2125 offers typical 100dB dynamic range and 0.025% THD. A direct path bypass mode allows normal stereo operation with high fidelity without the need for external switching or parallel signal paths.

The SSM-2125 is subject to final approval by Dolby Laboratories Licensing Corporation, and will be available only to licensees of Dolby Licensing Corporation, San Francisco, California from whom licensing and application information must be obtained.

BLOCK DIAGRAM, SHOWING PMI IMPLEMENTED SECTIONS



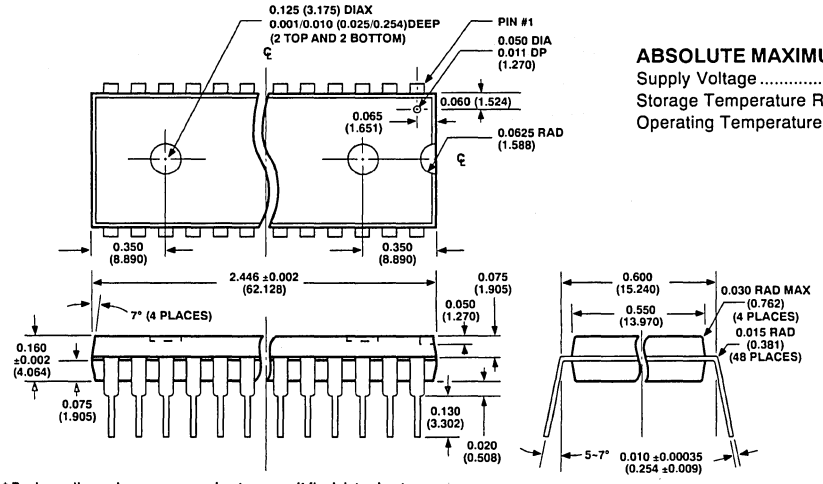
*Dolby Is a trademark of Dolby Laboratories Licensing Corporation, San Francisco, California

ELECTRICAL CHARACTERISTICS at: V_S = 12V; T_A = 25°C; V_{IN} = 1kHz at Dolby level.

		SSM-2125			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Channel Separation:					
Left	L Input	25	35	—	
Right	R Input	25	35	—	dB
Center	C Input	25	35	—	
Surround	S Input	25	35	—	
Total Harmonic Distortion:					
Left	L Channel	—	0.025	0.1	
Right	R Channel	—	0.025	0.1	%
Center	C Channel	—	0.025	0.1	
Surround	S Channel	—	0.025	0.1	
Signal-to-Noise Ratio:					
Left		80	85	—	
Right	R_S = 0, CCIR/ARM	80	85	—	dB
Center		80	85	—	
Surround		80	85	—	
Headroom:					
Left		16	18	—	
Right	V_{CC} = 9V, 1% THD	16	18	—	dB
Center		16	18	—	
Surround		16	18	—	
Auto Balance Range		±3	±4	—	dB
Noise Sequencing Channel Duration	C_{OSC} = 1µF	—	2	—	sec
Bypass Mode Dynamic Range		—	100	—	dB
Dolby Level (Input)	L, R		300		
	C,S		212		mV_{RMS}
(Output)	All Channels		300		

Specifications subject to change; consult latest data sheet.

PACKAGE DIAGRAM - 48-PIN PLASTIC DIP*



* Package dimensions are approximate; consult final data sheet

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 16V
Storage Temperature Range ..... −55°C to +125°C
Operating Temperature Range ..... −20°C to +80°C

This advance product information is based on proposed specifications. Final specifications may vary. Please contact local sales office or factory for final data sheet. © PMI 1990

PMI

Audio Silicon Specialists™

SSM-2015
LOW NOISE MICROPHONE PREAMPLIFIER

Precision Monolithics Inc.

FEATURES

- Ultra Low Voltage Noise ..... 1.3nV/√Hz
- Wide Bandwidth ..... 700kHz @ G = 100
- High Slew Rate 8V/µs
- Very Low Harmonic Distortion ..... 0.007% @ G = 100
- Excellent CMR 100dB
- True Differential "Instrumentation" Type Inputs
- Programmable Input Stage Optimizes e_n vs R_{IN}
- Low Cost

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 14-PIN	
SSM2015P	–10°C to +55°C

GENERAL DESCRIPTION

The SSM-2015 is an ultra-low noise audio preamplifier particularly suited to microphone preamplification. Gains from 10 to over 2000 can be selected with wide bandwidth and low distortion over the full gain range.

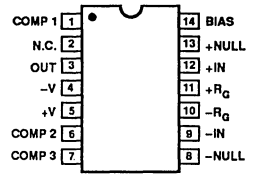
The very low voltage noise performance (1.3nV/√Hz) of the SSM-2015 is enhanced by a programmable input stage which allows overall noise to be optimized for source impedances of up to 4kΩ.

The SSM-2015's true differential inputs with high common-mode rejection provide easy interfacing to flotation transducers such as balanced microphone outputs, as well as single ended devices.

The SSM-2015 also offers high slew rate of about 8V/µs and full DC coupling without any crossover distortion.

This device is packaged in a 14-pin epoxy DIP and is guaranteed over the operating temperature range of –10°C to +55°C.

PIN CONNECTION



14-PIN PLASTIC DIP (P-Suffix)

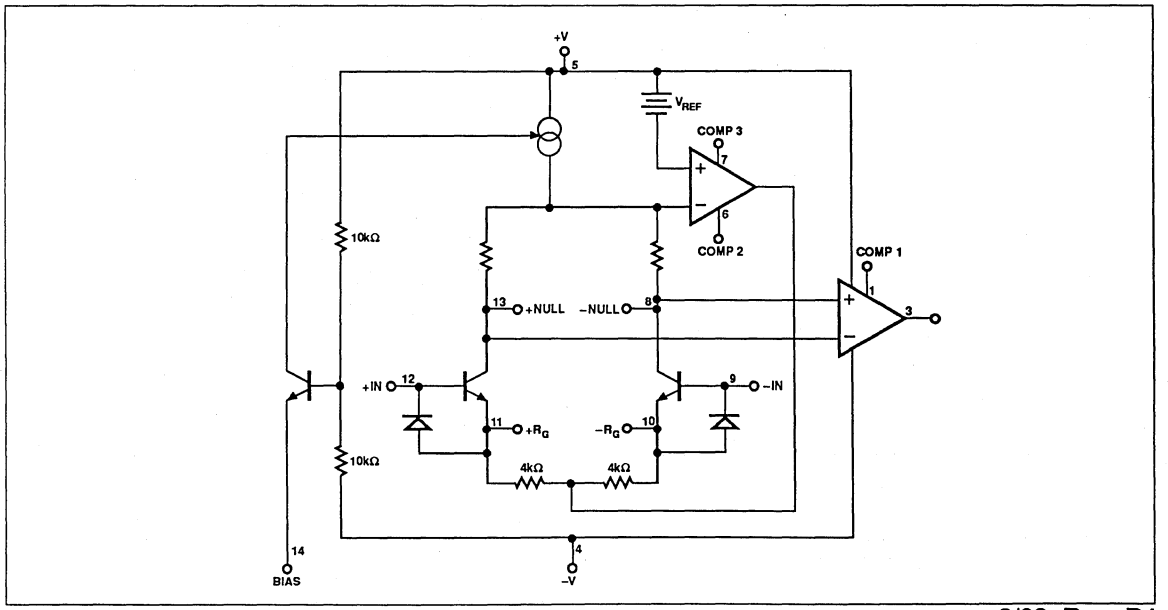
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Operating Temperature Range ..... –10°C to +55°C
Junction Temperature ..... +150C
Storage Temperature ..... –55°C to +125°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
14-Pin Plastic DIP (P)	76	33	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

BLOCK DIAGRAM



2/90, Rev. B1

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, R_{BIAS} = 33kΩ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2015 MIN	TYP	MAX	UNITS
Total Harmonic Distortion (Note 1)	THD	V_{OUT} = 7V RMS, R_L = 10kΩ				
		G = 1000				
		f = 1kHz	–	0.007	0.01	
		f = 10kΩ	–	0.015	0.02	
		G = 100				%
		f = = 1kHz	–	0.007	0.01	
		f = 10kHz	–	0.007	0.01	
		G = 10				
		f = 1kHz	–	0.01	0.015	
		f = 10kHz	–	0.01	0.015	
Input Referred Voltage Noise (Note 1)	E_n	Inputs Shorted to GND				
		20kHz Bandwidth				
		R_{BIAS} = 33KΩ				
		G = 1000	–	0.2	0.3	
		G = 100	–	0.3	0.5	
		G = 10	–	1.1	1.7	μV RMS
		R_{BIAS} = 150kΩ				
		G = 1000	–	0.28	0.45	
		G = 100	–	0.41	0.65	
		G = 10	–	1.1	1.7	
Input Current Noise (Note 1)	I_n	20kHz Bandwidth				
		R_{BIAS} = 33kΩ	–	250	380	
		R_{BIAS} = 68kΩ	–	200	300	pA RMS
		R_{BIAS} = 150kΩ	–	130	200	
Error From Gain Equation	ΔG	$R_1 = R_2$ = 10kΩ				
		G = 1000	–	0.1	0.3	
		G = 100	–	0.1	0.3	dB
		G = 10	–	0.2	0.8	
Input Offset Voltage	V_{OS}	$R_1 = R_2$ = 10kΩ				
		G = 1000	–	0.25	2	
		G = 100	–	0.3	7	mV
		G = 10	–	3	70	
Input Bias Current	I_B	V_{CM} = 0V				
		R_{BIAS} = 33kΩ	–	4.5	15	μA
		R_{BIAS} = 150kΩ	–	1	4	
Input Offset Current	I_{OS}	V_{CM} = 0V				
		R_{BIAS} = 33kΩ	–	0.5	2.5	μA
		R_{BIAS} = 150kΩ	–	0.15	0.7	
Common-Mode Rejection Ratio	CMRR	$R_1 = R_2$ = 10kΩ				
		G = 1000	90	100	–	
		G = 100	70	95	–	dB
		G = 10	60	75	–	
Power Supply Rejection Ratio	PSRR	V_S = ±12 to ±17V	–	100	–	dB
Common-Mode Voltage Range	CMVR		±4	±5.5	–	V
Common-Mode Input Impedance	R_{INCM}		–	50	–	MΩ
Differential-Mode Input Impedance	R_{IN}	G = 1000	–	0.5	–	
		G = 100	–	5	–	MΩ
		G = 10	–	20	–	
Output Voltage Swing	V_O	R_L = 2kΩ	±10.5	±12.5	–	V
Output Current (Note 2)	I_{OUT}	Source	15	25	–	mA
		Sink	8	14	–	
–3dB Bandwidth	GBW	G = 1000	–	150	–	
		G = 100	–	700	–	kHz
		G = 10	–	1000	–	
Slew Rate	SR		–	8	–	V/μs
Supply Current	I_{SY}		8	12	16	mA

NOTES:

1. Parameter is sample tested to maximum limits.
2. Output is protected from short circuits to ground or either supply.

Specifications subject to change; consult latest data sheet.

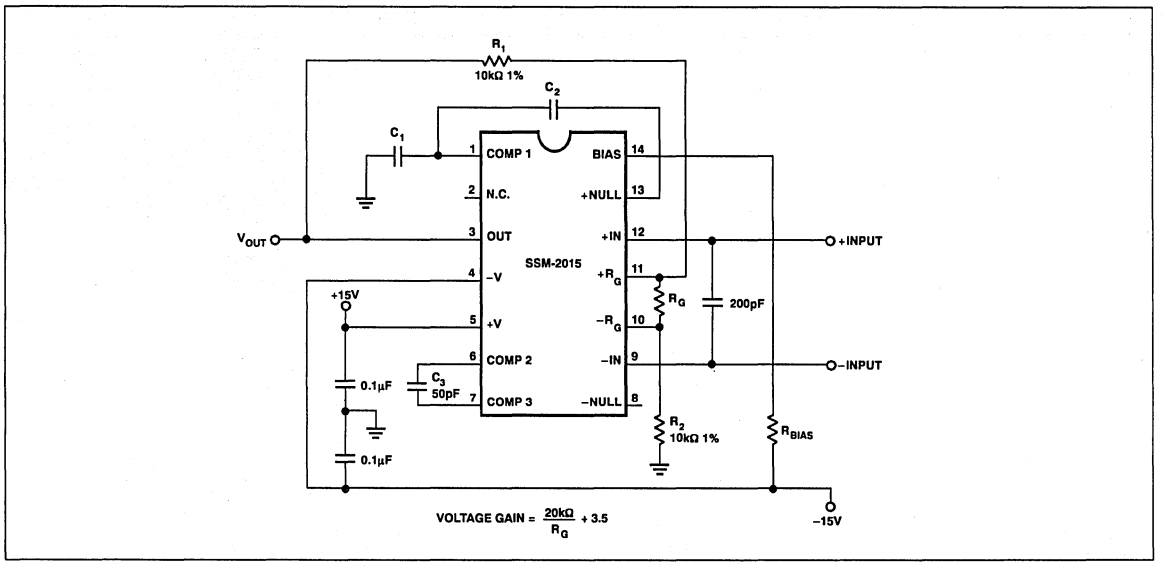


FIGURE 1: *Typical Application*

APPLICATIONS INFORMATION

PRINCIPLE OF OPERATION

Figure 1 shows a typical application for the SSM-2015. This device operates as a true differential amplifier with feedback returned directly to the emitters of the input stage transistors by R_1. This system produces both optimum noise and common-mode rejection while retaining a very high input impedance at both input terminals. An internal feedback loop maintains the input stage current at a value controlled by an external resistor (R_{BIAS}) from pin 14 to V–. This provides a programmability function which allows noise to be optimized for source impedances of up to 4kΩ.

GAIN SETTING

The nominal gain of the SSM-2015 is given by:

$$G \cong \frac{R_1 + R_2}{R_G} + \frac{R_1 + R_2}{8k\Omega} + 1$$

or

$$G = \frac{20k\Omega}{R_G} + 3.5 \quad \text{For } R_1,\ R_2 = 10k\Omega$$

R_1 and R_2 should be equal to 10kΩ for best results (see Figure 1). It is vital that good quality resistors be used in the gain setting network, since low quality types (notably carbon composition) can generate significant amounts of distortion and, under some conditions, low frequency noise. The SSM-2015 will function at gains down to 3.5, but the best performance is obtained at gains above 10. Table 1 gives R_G values for most commonly used gains.

TABLE 1: R_G Values for Commonly Used Gains

$$R_G = \frac{R_1 + R_2}{G - 3.5}$$

GAIN	R_G	ERROR
10	3kΩ	+0.14dB
50	430Ω	+0.002dB
100	200Ω	+0.3dB
500	39Ω	+0.28dB
1000	20Ω	+0.03dB

FREQUENCY COMPENSATION

Referring to Figure 1, C_3 (50pF) provides compensation for the input stage current regulator, while C_1 and C_2 compensate the overall amplifier. The latter two depend on the value of R_{BIAS} chosen. Table 2 shows the recommended values for C_1 and C_2 at various R_{BIAS} levels. These values are valid for all gain settings.

TABLE 2: Recommended Compensation Values

R_{BIAS}	C_1	C_2
27kΩ - 47kΩ	15pF	15pF
47kΩ - 68kΩ	15pF	10pF
68kΩ - 150kΩ	30pF	5pF

The SSM-2015 has a bandwidth of at least 70kHz under worst case conditions (G = 1000, R_{BIAS} = 150kΩ) and considerably greater at higher set currents and lower gains. This excellent performance is supplemented by a highly symmetric slew rate for optimum large signal audio performance. The SSM-2015 provides stable operation with load capacitances of up to 150pF; larger capacitances should be decoupled with a 100Ω resistor in series with the output (R_1 in Figure 1 should remain connected to pin 3).

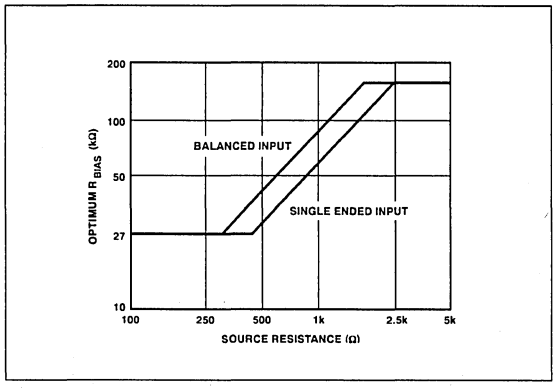


FIGURE 2: *Optimum R_{BIAS} vs. Source Resistance*

NOISE

The programmability of the SSM-2015 provides close to optimum performance for source impedances of up to 4kΩ, and is within 1dB of the theoretical minimum value between 500Ω and 2.5kΩ.

Figure 2 shows the recommended bias resistor (R_{BIAS}) versus source impedance, for balanced or single-ended inputs.

INPUTS

Although the SSM-2015 inputs are fully floating, care must be exercised to ensure that both inputs have a DC bias connection capable of maintaining them within the input common-mode range. The usual method of achieving this is to ground one side of the transducer as in Figure 3(a), but an alternative way is to float the transducer and use two resistors to set the bias point as in Figure 3(b). The value of these resistors can be up to 10kΩ, but they should be kept as small as possible to limit common-mode noise. Noise generated in the resistors themselves is negligible since it is attenuated by the transducer impedance. Balanced transducers give the best noise immunity, and interface directly as in Figure 3(c).

TRIMMING

The gain of the SSM-2015 can be easily trimmed by adjustment of R_G. However, two further trims may be desirable: Offset Voltage and Common-mode Rejection, although the SSM-2015 provides excellent untrimmed performance in both respects.

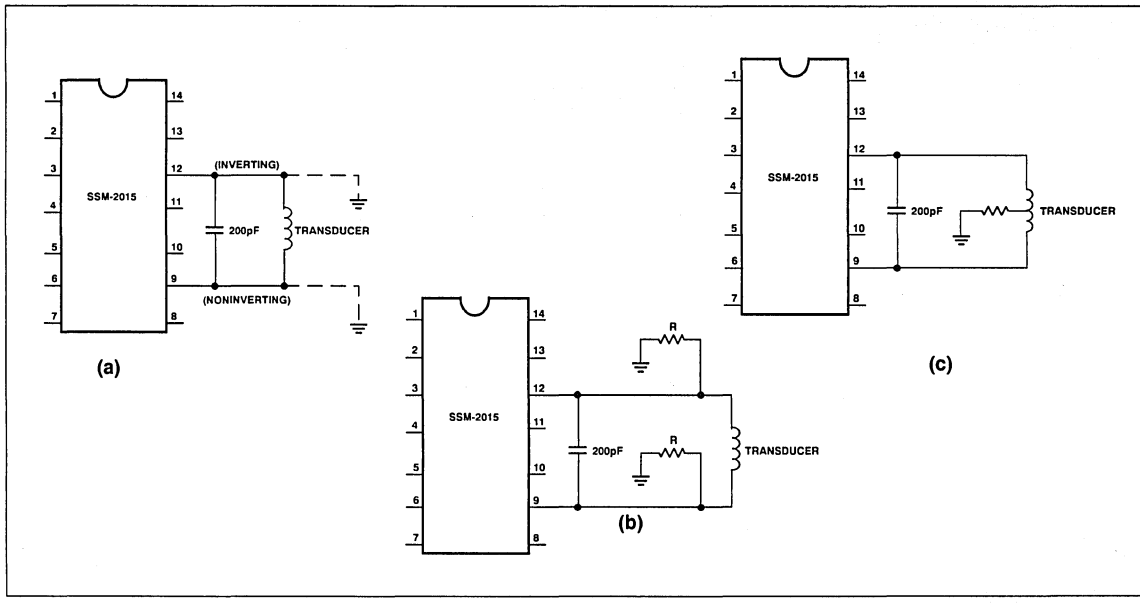


FIGURE 3: *Three Ways of Interfacing Transducers for High Noise Immunity*
(a) Single Ended (b) Pseudo Differential (c) True Differential

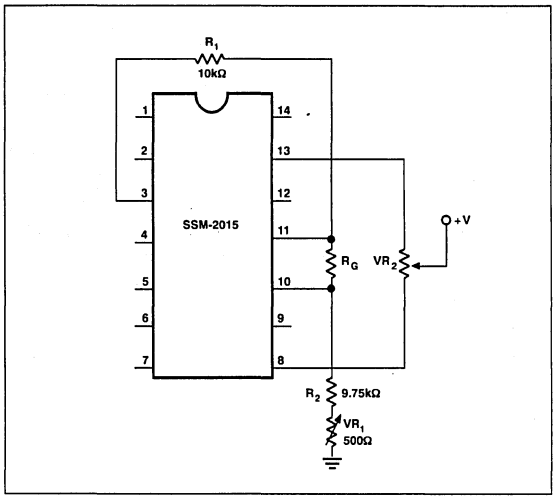


FIGURE 4: *Trimming the SSM-2015*

Figure 4 shows the trimming method for both parameters.

V_{R1} is the CMR trim and should be adjusted for minimum output with an $8V_{p-p}$ amplitude 60Hz Sine Wave common to both inputs.

V_{R2} is the offset voltage trim, and should be selected from Table 3. The offset trim should follow the CMR trim, since there is a small (non-reciprocal) interaction.

The offset trim can also be used to null out the gain control feedthrough. The output offset at low gains is determined by matching of the feedback resistors while at high gains it is determined by the matching of the input resistors. If the gain setting is changed rapidly, the output shift can cause an (audible) click or thump. To reduce or eliminate this, the offset at high gains is adjusted to be equal to the offset at low gains.

TABLE 3: Recommended Values for the Offset Voltage Trim

	R_{BIAS}		
	27kΩ - 47kΩ	**47kΩ - 68kΩ**	**68kΩ - 150kΩ**
$V_{R2'}$ G = 10	500kΩ	250kΩ	250kΩ
$V_{R2'}$ G = 100	500kΩ	100kΩ	100kΩ
$V_{R2'}$ G = 1000	250kΩ	100kΩ	50kΩ

PHANTOM POWER

A recommended circuit for phantom microphone powering is shown in Figure 5. Z_1 through Z_4 provide transient overvoltage protection for the SSM-2015 whenever microphones are plugged in and out.

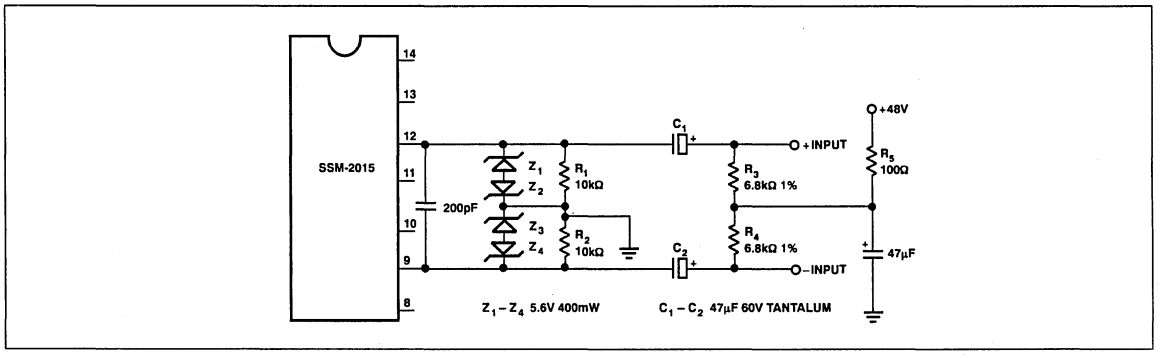


FIGURE 5: *SSM-2015 with Phantom Power*

PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

SSM-2016

ULTRA LOW NOISE DIFFERENTIAL AUDIO PREAMPLIFIER

FEATURES

- Ultra Low Voltage Noise ..... 800pV/$\sqrt{Hz}$ Typ
- High Slew Rate ..... 10V/μs Typ
- Very Low Harmonic Distortion ..... @ G = 1000 0.009% Typ
- Wide Bandwidth ..... @ G = 1000 650kHz Typ
- Very Wide Supply Voltage Range ..... ±9V to ±36V
- High Output Drive Capability ..... ±40mA Min
- High Common-Mode Rejection ..... 100dB Typ
- Low Cost

APPLICATIONS

- Low Noise High-Gain Microphone Preamplifier
- Bus Summing Amplifier
- Differential Line Receiver
- Low Noise Instrumentation Amplifier

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	
SSM2016P	–25°C to +55°C

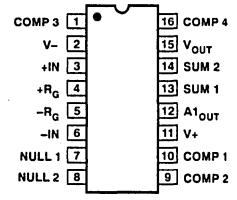
GENERAL DESCRIPTION

The SSM-2016 is an ultra low noise, low distortion differential audio preamplifier. The input referred noise of the SSM-2016 is about 800pV/$\sqrt{Hz}$ which will result in a noise figure of 1dB when operated with a 150Ω source impedance. This ensures that a large number of inputs can be paralleled without seriously degrading the signal-to-noise ratio. In addition, this device provides exceptionally low harmonic distortion of only 0.009% (G = 1000, f = 1kHz) Typ.

Fabricated on a high voltage process, the SSM-2016 is capable of operating from a wide supply voltage range of ±9V to ±36V. A

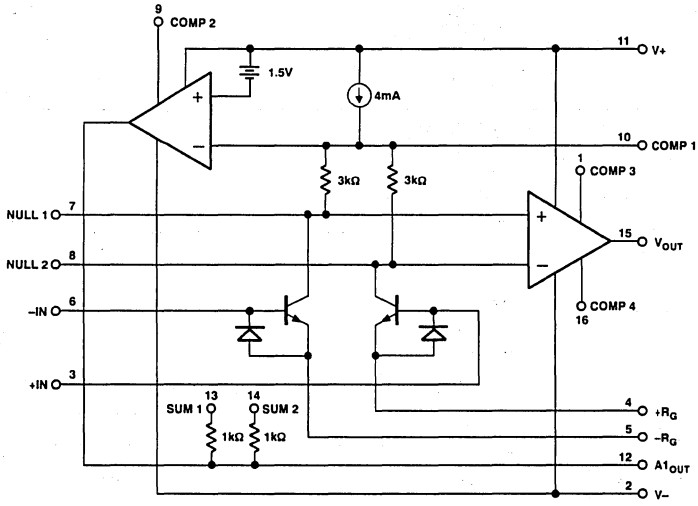
Continued

PIN CONNECTIONS



16-PIN PLASTIC DIP
(P-Suffix)

BLOCK DIAGRAM



The SSM-2016 has been granted mask work protection under the Semiconductor Chip Protection Act of 1983.

GENERAL DESCRIPTION *Continued*

The SSM-2016 can source or sink a minimum of 40mA allowing a jack-field to be driven directly.

At low gains, the SSM-2016 offers a bandwidth of about 1MHz and 650kHz at 60dB of gain. Slew rate is typically 10V/µs at all gains.

The SSM-2016 is packaged in a 16-pin epoxy DIP and performance and characteristics are guaranteed over the operating temperature range of –25°C to +55°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±38V
Recommended Supply
Voltage Range ..... ±9V to ±36V
Current Into Any Pin
(Except Pins 2, 11, and 15) 40mA
Lead Temperature (Soldering, 60 sec) ..... 300°C
Storage Temperature ..... –65°C to +150°C
Package Dissipation 2W
Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range ..... –25°C to 55°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Plastic DIP (P)	76	33	°C/W

NOTES:
1. Short-circuit duration is indefinite, provided dissipation limit is not exceeded.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm18V$, $R_1 = R_2 = 5k\Omega$, $R_3 = R_4 = 2k\Omega$, $T_A = +25°C$, unless otherwise noted.

			SSM-2016			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion	THD	$V_O = 10V_{RMS}$, $R_L = 2k\Omega$ G = 1000				%
		f = 1kHz	–	0.009	0.015	
		f = 10kHz	–	0.015	0.02	
		G = 100				
		f = 1kHz	–	0.003	0.005	
		f = 10kHz	–	0.005	0.007	
		G = 10				
		f = 1kHz	–	0.002	0.003	
		f = 10kHz	–	0.003	0.005	
		$V_O = 10V_{RMS}$, $R_L = 600k\Omega$, $V_S = \pm20V$ G = 1000				
		f = 1kHz	–	0.025	0.04	
		f = 10kHz	–	0.06	0.09	
		G = 100				
		f =1kHz	–	0.008	0.015	
		f = 10kHz	–	0.02	0.04	
		G = 10				
		f = 1kHz	–	0.005	0.008	
		f =10kHz	–	0.008	0.015	
Input Referred Voltage Noise (Note 1)	e_n	20kHz Bandwidth				μV_{RMS}
		G = 1000	–	0.11	0.16	
		G = 100	–	0.20	0.30	
		G = 10	–	0.80	1.2	
Input Current Noise (Note 1)	I_n	20 kHz Bandwidth	–	350	550	$pA/_{RMS}$
Slew Rate	SR		–	10	–	V/µs
–3dB Bandwidth (Note 2)	GBW	G = 1000	–	0.55	–	MHz
		G ≤ 100	–	1	–	
Input Offset Voltage	V_{OS}	G = 1000	–	0.5	2.5	mV
		G = 100	–	1.5	10	
		G = 10	–	5	8	
Input Bias Current	I_B	$V_{CM} = 0V$	–	9	25	µA
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	1.5	5.0	µA
Common-Mode Rejection Ratio	CMRR	G = 1000	96	100	–	dB
		G = 100	80.5	95	–	
		G = 10	64	75	–	
Power Supply Rejection Ratio	PSRR	$V_S = \pm9V$ to ±36V	90	100	–	dB
Common-Mode Voltage Range	CMVR		±7	±10	–	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 18V$, $R_1 = R_2 = 5k\Omega$, $R_3 = R_4 = 2k\Omega$, $T_A = +25°C$, unless otherwise noted.
Continued

PARAMETER	SYMBOL	CONDITIONS	SSM-2016 MIN	TYP	MAX	UNITS
Common-Mode Input Impedance	R_{INEM}		–	20	–	MΩ
Differential-Mode Input Impedance	R_{IN}	G = 1000	–	0.3	–	MΩ
		G = 100	–	3	–	
		G = 10	–	10	–	
Output Voltage Swing (Note 1)	V_O	$R_L = 2k\Omega$	±15	±17	–	V
		$R_L = 600\Omega$, $V_S = \pm 20V$	±15	±17	–	
Output Current (Note 3)	I_{OUT}	Source	40	70	–	mA
		Sink	40	70	–	
Supply Current	I_{SY}	$V_{CM} = 0V$	10	12	16	mA
Error From Gain Equation			–	0.1	0.3	dB

NOTES:
1. Sample tested.
2. Bandwidth will be slew-rate limited at high output levels.
3. Output is protected from short circuits to ground or either supply.

Specifications subject to change; consult latest data sheet.

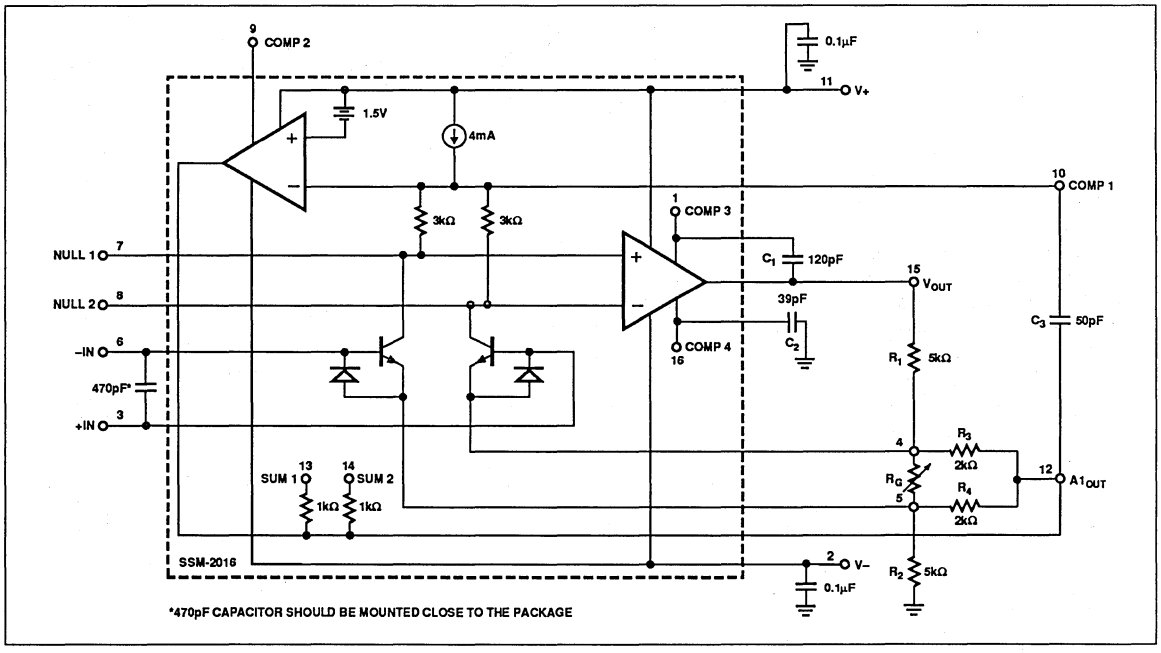


FIGURE 1: *Typical Preamplifier Amplification*

APPLICATIONS INFORMATION

PRINCIPLE OF OPERATION

The SSM-2016 operates as a true differential amplifier with feedback returned directly to the emitters of the input stage transistors by R_1 (See Figure 1). The differential pair is fed by a current source at the collectors and the required emitter current is supplied by a nulling (servo) amplifier through the external resistors R_3 and R_4 (Figure 1). This system produces both optimum noise and common-mode rejection while retaining a very high input impedance. The internal "servo" amplifier is used to control the input stage current independently of common-mode voltage and its output is accessible via pin 12.

GAIN SETTING

The nominal gain of the SSM-2016 is given by:

$$G = \frac{R_1 + R_2}{R_g} + \frac{R_1 + R_2}{R_3 + R_4} + 1$$

or

$$G = \frac{10k\Omega}{R_g} + 3.5 \text{ For } R_1 = R_2 = 5k\Omega, R_3 = R_4 = 2k\Omega$$

R_1 and R_2 should be equal to 5kΩ for best results. It is vital that good quality resistors be used in the gain setting network, since low quality types (notably carbon composition) can generate significant amounts of distortion and, under some conditions, low frequency noise.

The SSM-2016 is capable of operating at gains down to 3.5 at full performance. Gain range can be extended further by increasing R_3 and R_4 in Figure 1, but at the penalty of reduced common-mode input range. Gains below 2.5 are not practical unless the negative supply voltage is increased.

Note that tolerance of R_1 - R_4 directly affects the gain error and that good matching between R_1 - R_4 is essential to prevent degradation of the common-mode rejection performance.

The SSM-2016 provides internal 1kΩ resistors to replace R_3 and R_4 in applications where distortion is not too critical.

FREQUENCY COMPENSATION

The SSM-2016's internal "servo" amplifier is compensated by C_3, while C_1 and C_2 (see Figure 1) compensate the overall amplifier. The values shown maintain a very wide bandwidth with a good symmetrical slew rate. If desired, the bandwidth can be reduced by increasing the value of C_1.

NOISE PERFORMANCE

The SSM-2016's input referred noise is $0.11\mu V_{RMS}$ (20kHz bandwidth) at 60dB of gain, $0.2\mu V_{RMS}$ at 40dB, and $0.8\mu V_{RMS}$ at 20dB. The apparent increase at low gains is due to noise incurred in the feedback resistors and second stage becoming dominant. This noise is actually present at all times but becomes masked by input stage noise as the gain is increased.

The SSM-2016 is optimized for source impedances of 1kΩ or less and under these conditions, the noise performance is equal to the best discrete component designs. Considering that a "standard" microphone with impedance of 150Ω generates 1.6nV/$\sqrt{Hz}$ of thermal noise, the SSM-2016's 800pV/$\sqrt{Hz}$ of voltage noise or the corresponding noise figure of typically 1dB make the device virtually transparent to the user.

In applications where higher source impedances than 1kΩ are desired, the SSM-2015 preamplifier is recommended.

Another source of noise degradation is the chip's total power dissipation, since any increase in temperature will increase the noise. This effect is more pronounced at higher gains. As a result, the SSM-2016 uses a copper lead-frame package which greatly helps the power dissipation and the noise performance. The best noise performance of the SSM-2016 can be achieved at low supply voltages while driving light loads.

TOTAL HARMONIC DISTORTION

Figures 2 - 5 show the distortion behavior of SSM-2016. All measurements were taken at a $10V_{RMS}$ output to ensure a true "worst case" condition. No crossover distortion is observed at lower ouput levels. At 20dB of gain (Figure 2) total harmonic distortion (plus noise) is well below 0.01% at all audio frequencies. At 40dB of gain (Figure 3) some loading effects are evident, especially at higher frequencies, but the overall THD is still very low. The measurements at 60dB of gain (Figure 4) are a little misleading because the noise floor is at an equivalent level of 0.0085% at this gain. In fact, the real distortion components are not greatly increased from the 40dB case.

Figure 5 shows the intermodulation distortion performance of the SSM-2016. A basic SMPTE type test was performed with the main generator swept from 2.5kHz to 20kHz. The 60dB reading is once more mostly noise.

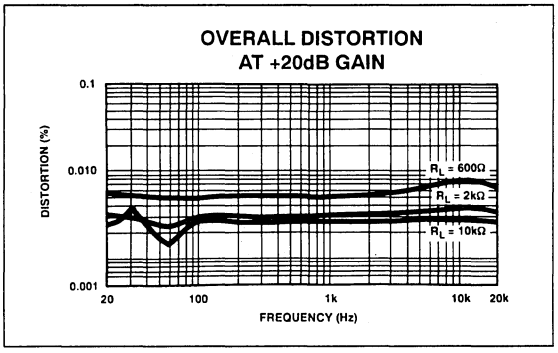


FIGURE 2

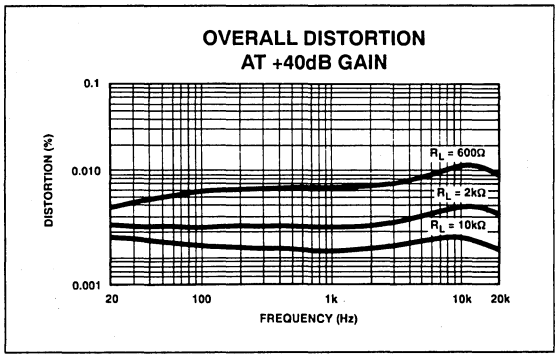


FIGURE 3

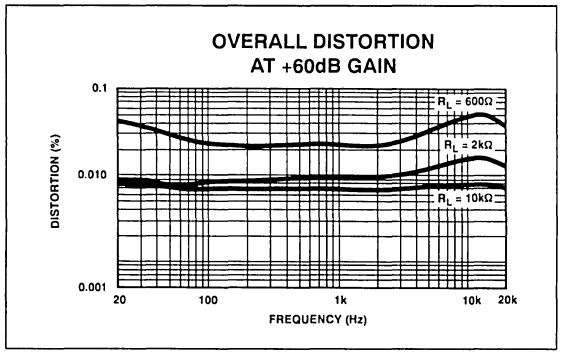


FIGURE 4

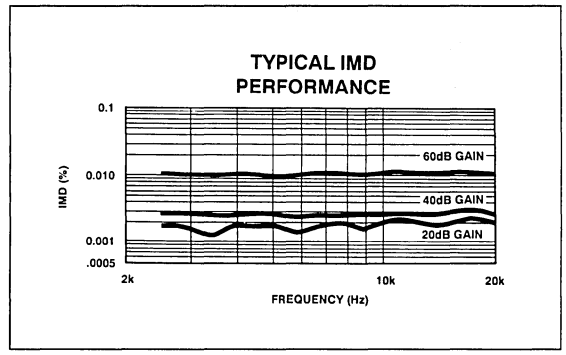


FIGURE 5

DRIVE CAPABILITY

Fabricated on a high voltage process, the SSM-2016 is capable of operating from ±9V to ±36V supplies. In addition, the powerful output stage is designed to drive a jack-field directly. The SSM-2016 is capable of driving a $10V_{RMS}$ sine wave into 600Ω load using ±18V supplies. However, ±20V or greater supplies are recommended to give a more comfortable headroom. A copper lead-frame DIP package is used to permit 1.5W of dissipation when driving heavy loads or operating from elevated supplies.

INPUTS

The SSM-2016 offers protection diodes across the base-emitter junctions of the input transistors. These prevent accidental avalanche breakdown which could seriously degrade noise performance. Additional clamp diodes are also provided to prevent the inputs from being forced too far beyond the supplies.

Although the SSM-2016's inputs are fully floating, care must be exercised to ensure that both inputs have a DC bias connection capable of maintaining them within the input common-mode range. The usual method of achieving this is to ground one side of the transducer as in Figure 6a, but an alternative way is to float the transducer and use two resistors to set the bias point as in figure 6b. The value of these resistors can be up to 10kΩ, but they should be kept as small as possible to limit common-mode pickup. Noise contribution by resistors themselves is negligible since it is attenuated by the transducer's impedance. Balanced transducers give the best noise immunity, and interface directly as in Figure 6c.

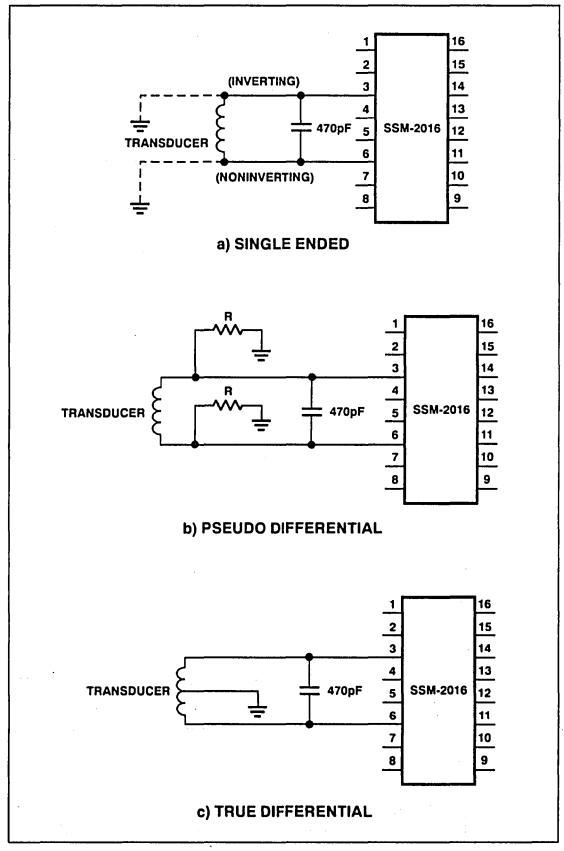


FIGURE 6: *Three Ways of Interfacing Transducers for High-Noise Immunity*

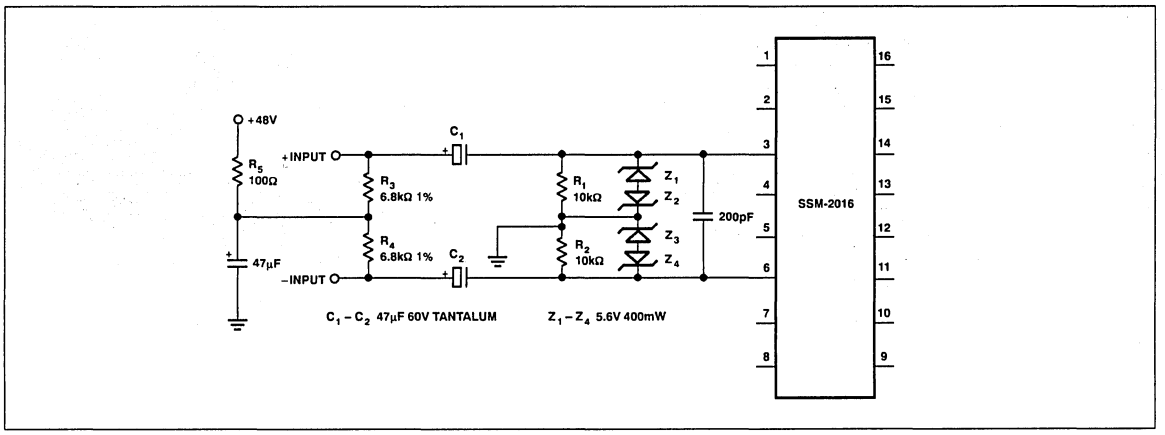


FIGURE 7: *SSM-2016 with Phantom Power*

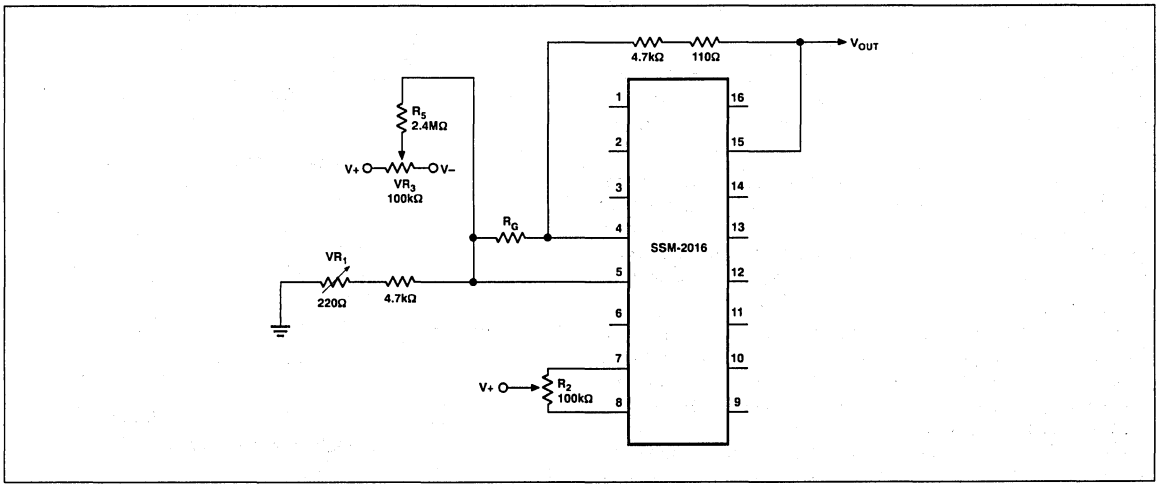


FIGURE 8: *Trimming Circuit*

PHANTOM POWERING

A typical phantom microphone powering circuit is shown in Figure 7. Z_1 through Z_4 provide transient overvoltage protection for the SSM-2016 whenever microphones are plugged in and out.

TRIMMING

The SSM-2016 accommodates four types of trimming: gain, high-gain offset, low-gain offset, and common-mode rejection. All four can be accomplished with the circuits shown in Figure 8.

Gain trim on the SSM-2016 is readily accomplished by adjusting R_G. VR_1 adjusts the common-mode rejection, VR_2 the high-gain offset, and VR_3 the low-gain offset. Common-mode rejection is best adjusted by applying an $8V_{p-p}$ 60Hz (50Hz in Europe) sine wave to both inputs and adjusting VR_1 for minimum output. Interaction is minimized by trimming the high-gain offset first, followed by the CMR and finally the low-gain offset. A two-pass trim is recommended for best results. Note that the overall gain has been reduced slightly to allow convenient values of resistors.

If the low-gain offset trim is not used, then gain control feedthrough can still be reduced by adjusting the high-gain offset to equal the low-gain offset by means of VR_2.

BUS SUMMING AMPLIFIER

In addition to its use as a microphone preamplifier, the SSM-2016 can be used as a very low noise summing amplifier. Such a circuit is particularly useful when many medium impedance outputs are summed together to produce a high effective noise gain.

The principle of the summing amplifier is to ground the SSM-2016 inputs. Under these conditions, pins 4 and 5 are AC virtual grounds sitting about 0.65V below ground. Any current injected into these points must flow through the feedback resistor (R_1) and hence are amplified to appear in the the output. Moreover, both positive (pin 5) and negative (pin 6) transfer characteristics are available simultaneously in contrast to the usual "inverting only" configuration.

To remove the 0.65V offset, the circuit of Figure 9 is recommended.

A_2 forms a "servo" amplifier feeding the SSM-2016's inputs. This places pins 4 and 5 at a true DC virtual ground. R_6 in conjunction with C_6 remove the voltage noise of A_2 and in fact just about any operational amplifier will work well here since it is removed from the signal path. If the DC offset at pins 4 and 5 is not too critical, then the servo loop can be replaced by the diode biasing scheme of Figure 9a. If AC coupling is used throughout, then pins 3 and 6 may be directly grounded.

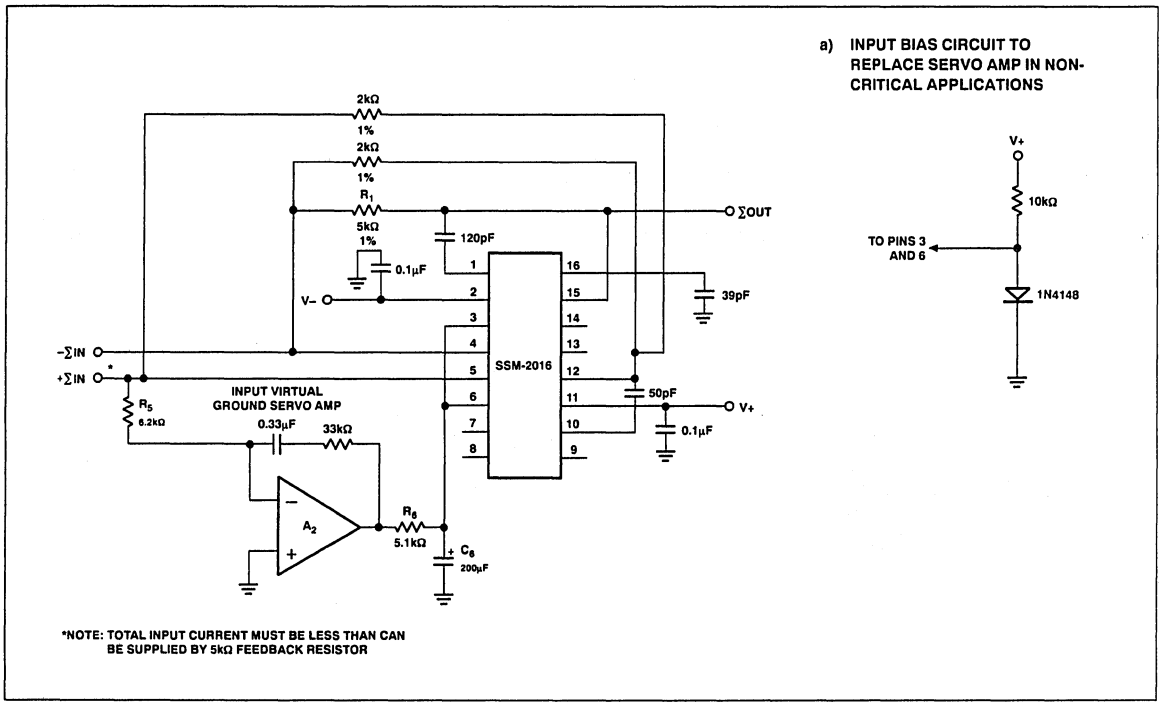


FIGURE 9: *Bus Summing Amplifier*

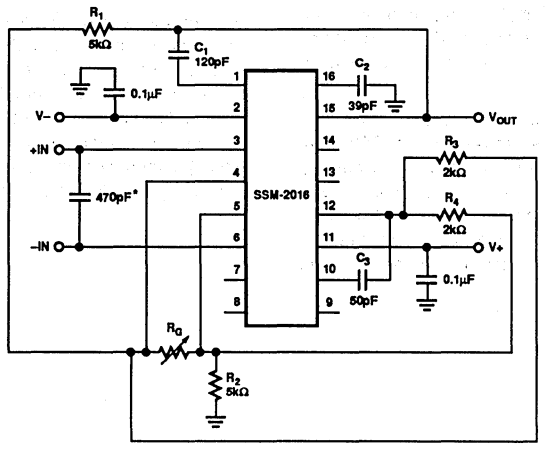


FIGURE 10: *Typical Connection for Breadboarding Purposes*

PMI

Audio Silicon Specialists™

SSM-2017
SELF-CONTAINED
AUDIO PREAMPLIFIER

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- Excellent Noise Performance ..... 750pv$\sqrt{Hz}$, or 1dB Noise Figure
- Ultra-Low THD ..... < 0.01% @ G = 1000 Over the Full Audio Band
- Wide Bandwidth ..... 250kHz @ G = 100
- High Slew Rate 10V/μs
- True Differential Inputs
- 8-Pin Mini-DIP with Only One External Component Required
- Very Low Cost
- Extended Industrial Temperature Range ..... –40°C to +85°C
- Gain Range of 0dB to Over 60dB
- Sub-Audio 1/f Noise Corner

APPLICATIONS

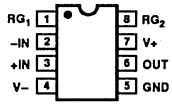
- Audio Mix Consoles
- Intercom/Paging Systems
- Two-Way Radio
- Sonar
- Digital Audio Systems

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	
SSM2017P	XIND*

*XIND = –40°C to +85°C

PIN CONNECTIONS



8-PIN
PLASTIC DIP
(P-Suffix)

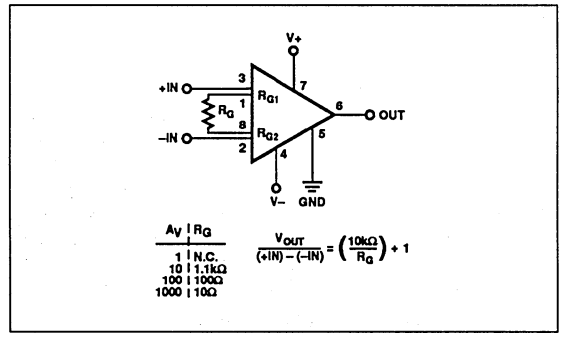
GENERAL DESCRIPTION

The SSM-2017 is PMI's latest generation audio preamplifier combining SSM preamplifier design expertise with advanced processing. The result is excellent audio performance from a self-contained 8-pin mini-DIP device, requiring only one external gain-set resistor or potentiometer. The SSM-2017 is further enhanced by its unity-gain stability.

Key specifications include ultra-low noise (1dB noise figure) and THD (<0.01% at G = 1000), complemented by wide bandwidth and high slew rate. The SSM-2017 can be operated by supply voltages from ±9V to ± 25V.

Applications for this low cost device include microphone preamplifiers and bus summing amplifiers in professional and consumer audio equipment, sonar, and other applications requiring a low-noise instrumentation amplifier with high gain capability.

TYPICAL APPLICATION



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

SSM-2402/SSM-2412

DUAL AUDIO ANALOG SWITCHES

FEATURES

- "Clickless" Bilateral Audio Switching
- Guaranteed "Break-Before-Make" Switching
- Low Distortion ..... 0.003% Typ
- Low Noise ..... 1nV/√Hz
- Superb OFF-Isolation ..... 120dB Typ
- Low ON-Resistance ..... 60Ω Typ
- Wide Signal Range:
  V_S = ±18V ..... 10V RMS
- Wide Power Supply Range ..... ±20V Max
- Available in Dice Form

ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 14-PIN	SOL 16-PIN	
SSM2402P	SSM2402S	XIND*
SSM2412P	SSM2412S	XIND*

*XIND = –40°C to +85°C

GENERAL DESCRIPTION

The SSM-2402/2412 are dual analog switches designed specifically for high-performance audio applications. Distortion and noise are negligible over the full audio operating range of 20Hz to 20kHz at signal levels of up to $10V_{RMS}$. The SSM-2402/2412 offer a monolithic integrated alternative to expensive and noisy relays or complex discrete JFET circuits. Unlike conventional general-purpose CMOS switches, the SSM-2402/2412 provide superb fidelity without audio "clicks" during switching.

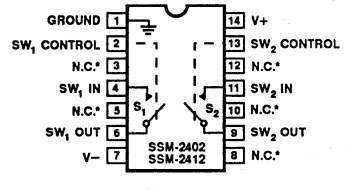
Conventional TTL or CMOS logic can be used to control the switch state. No external pull-up resistors are needed. A "T" configuration provides superb OFF-isolation and true bilateral operation. The analog inputs and outputs are protected against overload and overvoltage.

An important feature is the guaranteed "break-before-make" for all units, even IC-to-IC. In large systems with multiple switching channels, all separate switching units must open before any switch goes into the ON-state. With the SSM-2402/2412, you can be certain that multiple circuits will all break-before-make.

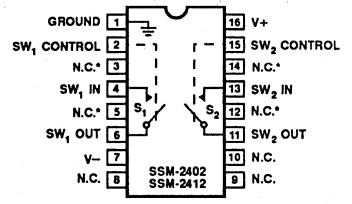
The SSM-2402/2412 represent a significant step forward in audio switching technology. Distortion and switching noise are significantly reduced in the new SSM-2402/2412 bipolar-JFET switches relative to CMOS switching technology. Based on a new circuit topology that optimizes audio performance, the SSM-2402/2412 make use of a proprietary bipolar-JFET process with thin-film resistor network capability. Nitride capacitors, which are very area efficient, are used for the proprietary ramp generator that controls the switch resistance transition. Very wide bandwidth amplifiers control the gate-to-source voltage over the full audio operating range for each switch. The ON-resistance is very constant with changes in signal amplitude and frequency, thus distortion is very low, less than 0.01% Max.

The SSM-2402 is the first analog switch truly optimized for high-performance audio applications. For broadcasting and other switching applications which require a faster switching time, we recommend the SSM-2412 – a dual analog switch with one-third of the switching time of the SSM-2402.

PIN CONNECTIONS



14-PIN PLASTIC DIP (P-Suffix)



16-PIN SOL (S-Suffix)

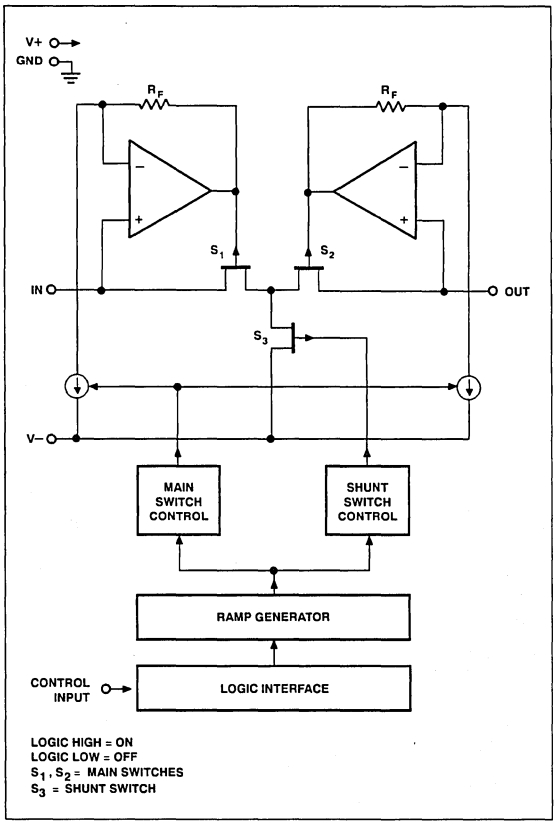
* GUARD PINS FOR INPUT/OUTPUT ISOLATION (GROUND FOR BEST PERFORMANCE)

CONTROL LOGIC

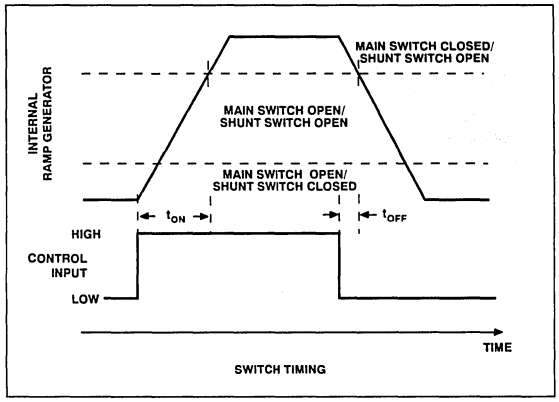
Logic In	Switch State
0	OFF
1	ON

Logic "0" ≤ 0.8V
Logic "1" ≥ 2.0V

FUNCTIONAL DIAGRAM



TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range ..... –40°C to +85°C
Operating Supply Voltage Range ..... ±20V
Analog Input Voltage Range
Continuous ..... V– +3.5V ≤ V_A ≤ V+ –3.5V
Maximum Current Through Switch 20mA
Logic Input Voltage Range ..... V+ Supply to –2V
V+ Supply to Ground ..... +36V
V– Supply to Ground ..... –20V
V_A to V– Supply ..... +36V

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±18V, R_L = OPEN, and –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

All specifications, tables, graphs, and application data apply to both the SSM-2402 and SSM-2412, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2402/2412 MIN	TYP	MAX	UNITS
Positive Supply Current	$+I_{SY}$	V_{IL} = 0.8V, 2.0V (Note 1)	–	6.0	7.5	mA
Negative Supply Current	$-I_{SY}$	V_{IL} = 0.8V, 2.0V (Note 1)	–	4.8	6.0	mA
Ground Current	I_{GND}	V_{IL} = 0.8V, 2.0V (Note 1)	–	0.6	1.5	mA
Digital Input High	V_{INH}	T_A = Full Temperature Range	2.0	–	–	V
Digital Input Low	V_{INL}	T_A = Full Temperature Range	–	–	0.8	V
Logic Input Current	I_{LOGIC}	V_{IN} = 0 to 15V (Note 2)	–	1.0	5.0	µA
Analog Voltage Range (Note 3)	V_{ANALOG}		–14.2	–	+14.2	V

ELECTRICAL CHARACTERISTICS at V_S = ±18V, R_L = OPEN, and –40°C ≤ T_A ≤ +85°C, unless otherwise noted. *Continued*

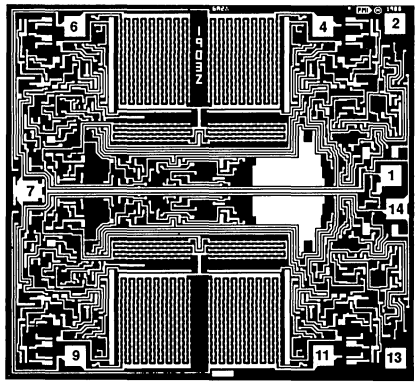
PARAMETER	SYMBOL	CONDITIONS		SSM-2402/2412 MIN	TYP	MAX	UNITS
Analog Current Range (Note 3)	I_{ANALOG}			–10	–	+10	mA
Overvoltage Input Current		$V_{IN} = \pm V_{SUPPLY}$		–	±40	–	mA
Switch ON Resistance	R_{ON}	–14.2 ≤ V_A ≤ +14.2V I_A = ±10mA, V_{IL} = 2.0V T_A = +25°C T_A = Full Temperature Range Tempco ($\Delta R_{ON}/\Delta T$)		– – –	60 – 0.2	85 115 –	Ω Ω Ω/°C
R_{ON} Match	$R_{ON}MATCH$	–14.2 ≤ V_A ≤ +14.2V I_A = ±10mA, V_{IL} = 2.0V		–	1	5	%
Switch ON Leakage Current	$I_{S(ON)}$	V_{IL} = 2.0V –14.2V ≤ V_A ≤ +14.2V V_A = 0V		– –	0.05 0.05	1.0 10.0	µA nA
Switch OFF Leakage Current	$I_{S(OFF)}$	V_{IL} = 0.8V –14.2V ≤ V_A ≤ +14.2V V_A = 0V		– –	0.05 0.05	1.0 10.0	µA nA
Turn-On Time (Note 4)	t_{ON}	V_A = +10V, R_L = 2kΩ T_A = +25°C, See Test Circuit	SSM-2402 SSM-2412	– –	10.0 3.5	– –	ms
Turn-Off Time (Note 5)	t_{OFF}	V_A = +10V, R_L = 2kΩ T_A = +25°C, See Test Circuit	SSM-2402 SSM-2412	– –	4.0 1.5	– –	ms
Break-Before-Make Time Delay (Note 6)	$t_{OFF} - t_{ON}$	T_A = +25°C	SSM-2402 SSM-2412	– –	6.0 2.0	– –	ms
Charge Injection	Q	T_A = +25°C	SSM-2402 SSM-2412	– –	50 150	– –	pC
ON-State Input Capacitance	$CS_{(ON)}$	V_A = 1V_{RMS} f = 5kHz, T_A = +25°C		–	12	–	pF
OFF-State Input Capacitance	$CS_{(OFF)}$	V_A = 1V_{RMS} f = 5kHz, T_A = +25°C		–	4	–	pF
OFF Isolation	$I_{SO(OFF)}$	V_A = 10V_{RMS}, 20Hz to 20kHz T_A = +25°C, See Test Circuit		–	120	–	dB
Channel-to-Channel Crosstalk	C_T	V_A = 10V_{RMS}, 20Hz to 20kHz T_A = +25°C		–	96	–	dB
Total Harmonic Distortion (Note 7)	THD	0 to 10V_{RMS}, 20Hz to 20kHz T_A = +25°C, R_L = 5kΩ		–	0.003	0.01	%
Spectral Noise Density	e_n	20Hz to 20kHz T_A = +25°C		–	1	–	nV/√Hz
Wideband Noise Density	$e_{n\ p\text{-}p}$	20Hz to 20kHz T_A = +25°C		–	0.2	–	$\mu V_{p\text{-}p}$

NOTES:

1. "V_{IL}" is the Logic Control Input.
2. Current tested at V_{IN} = 0V. This is the worst case condition.
3. Guaranteed by R_{ON} test condition.
4. Turn-ON Time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the final value.
5. Turn-OFF time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the initial value.
6. Switch is guaranteed by design to provide break-before-make operation.
7. THD guaranteed by design and dynamic R_{ON} testing.

DICE CHARACTERISTICS

SSM-2402/SSM-2412



DIE SIZE 0.105 x 0.097 inch, 10,185 sq. mils
(2.667 x 2.464 mm, 6.57 sq. mm)

1. GROUND
2. SWITCH $_1$ CONTROL
4. SWITCH$_1$ IN
6. SWITCH$_1$ OUT
7. V– SUPPLY
9. SWITCH$_2$ IN
11. SWITCH$_2$ OUT
13. SWITCH$_2$ CONTROL
14. V+ SUPPLY

For additional DICE information, refer to PMI's Data Book, Section 2.

WAFER TEST LIMITS at V_S = ±18V, R_L = OPEN, and T_A = +25°C.

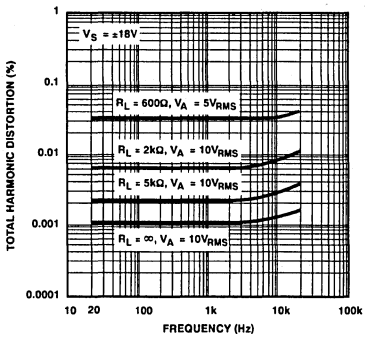
PARAMETER	SYMBOL	CONDITIONS (Note 1)	SSM-2402/2412 LIMIT	UNITS
Positive Supply Current	$+I_{SY}$	V_{IL} = 0.8V	7.5	mA MAX
Negative Supply Current	$-I_{SY}$	V_{IL} = 0.8V	6.0	mA MAX
Ground Current	I_{GND}	V_{IL} = 0.8V	1.5	mA MAX
Logic Input Current	I_{LOGIC}	V_{IN} = 0V (Note 2)	5.0	µA MAX
Switch ON Resistance	R_{ON}	$-14.2 \le V_A \le +14.2V$ I_A = ±10mA, V_{IL} = 2.0V	85	Ω MAX
R_{ON} Match Between Switches	R_{ON}MATCH	$-14.2V \le V_A \le +14.2V$ I_A = ±10mA, V_{IL} = 2.0V	5	% MAX
Switch ON Leakage Current	$I_{S(ON)}$	$-14.2V \le V_A \le +14.2V$ V_{IL} = 2.0V	1.0	µA MAX
Switch OFF Leakage Current	$I_{S(OFF)}$	$-14.2V \le V_A \le +14.2V$ V_{IL} = 0.8V	1.0	µA MAX

NOTES:
1. V_{IL} = Logic Control Input
   V_A = Applied Analog Input Voltage
   I_A = Applied Analog Input Current
2. Worst Case Condition

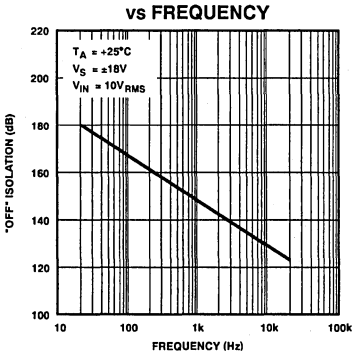
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

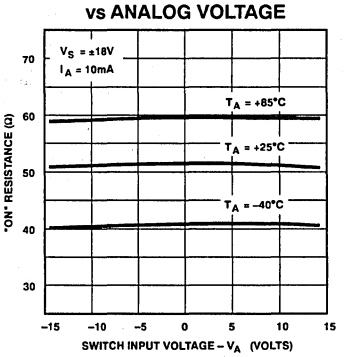
TOTAL HARMONIC DISTORTION vs FREQUENCY



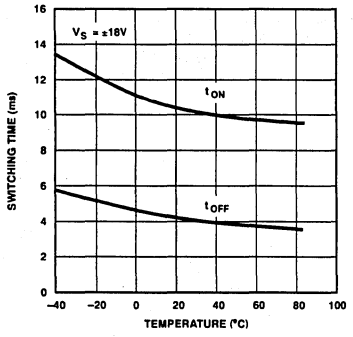
"OFF" ISOLATION vs FREQUENCY



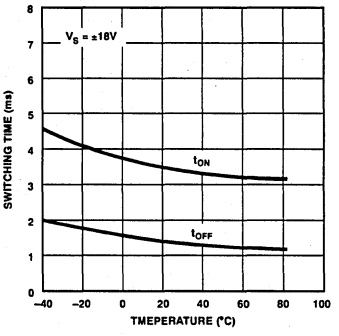
"ON" RESISTANCE vs ANALOG VOLTAGE



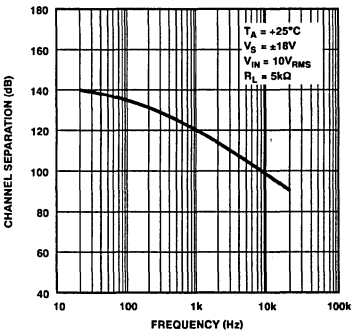
SSM-2402 SWITCHING TIME vs TEMPERATURE



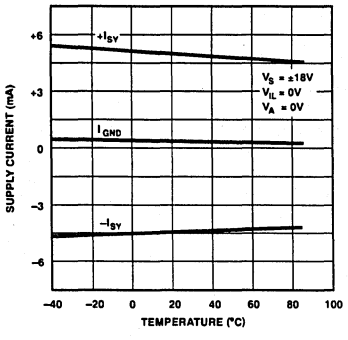
SSM-2412 SWITCHING TIME vs TEMPERATURE



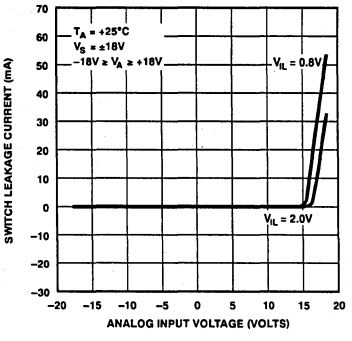
CHANNEL SEPARATION vs FREQUENCY



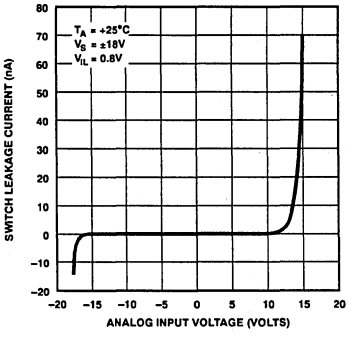
SUPPLY CURRENT vs TEMPERATURE



OVERVOLTAGE CHARACTERISTICS

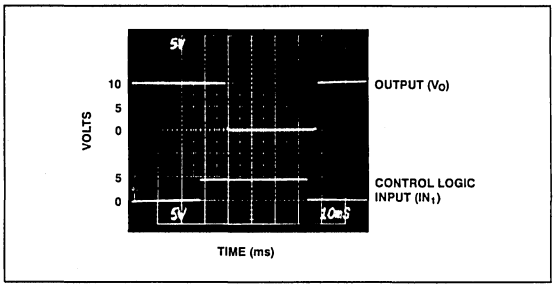


LEAKAGE CURRENT vs ANALOG VOLTAGE

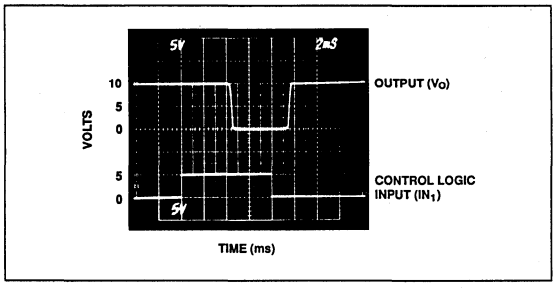


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

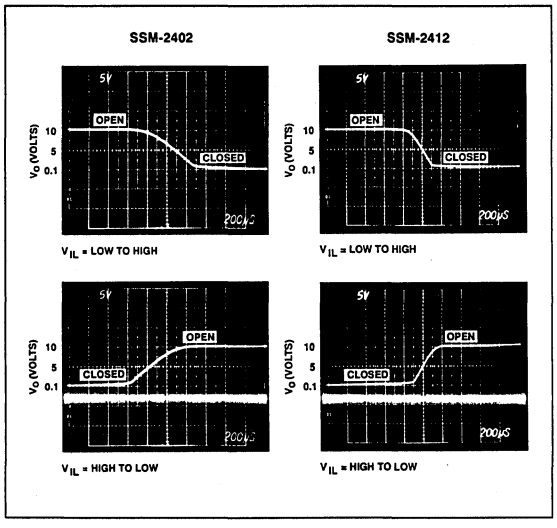
SSM-2402 T_{ON}/T_{OFF} SWITCHING RESPONSE



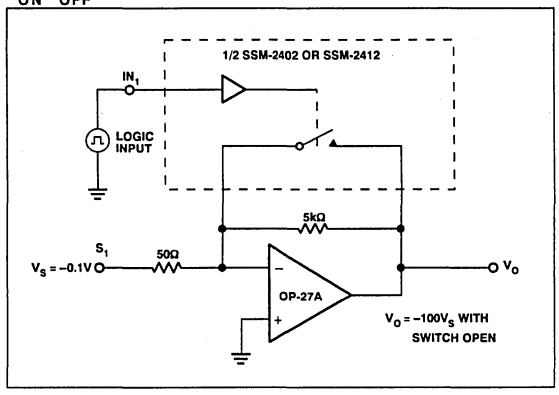
SSM-2412 T_{ON}/T_{OFF} SWITCHING RESPONSE



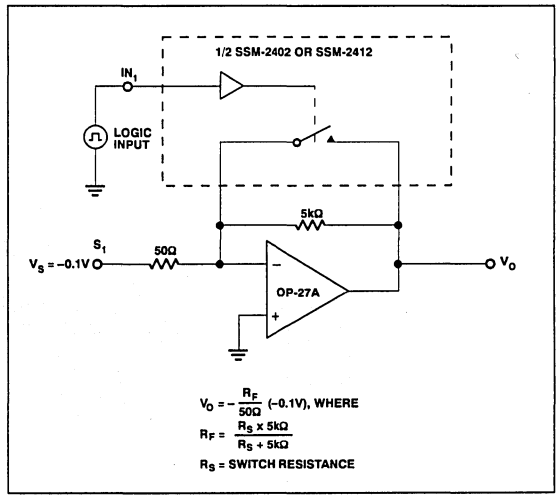
SWITCHING ON/OFF TRANSITION



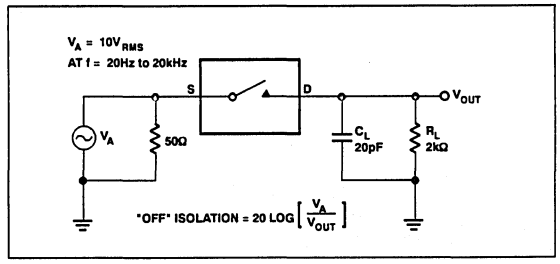
T_{ON}/T_{OFF} SWITCHING RESPONSE TEST CIRCUIT



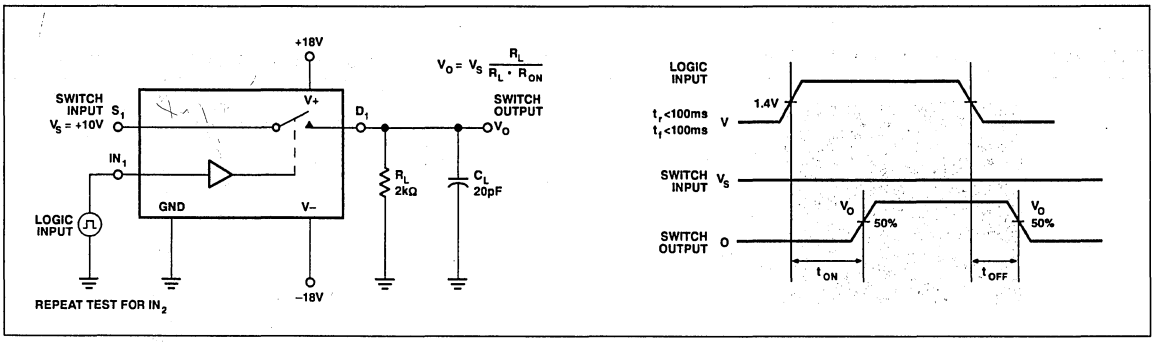
SWITCH ON/OFF TRANSITION TEST CIRCUIT



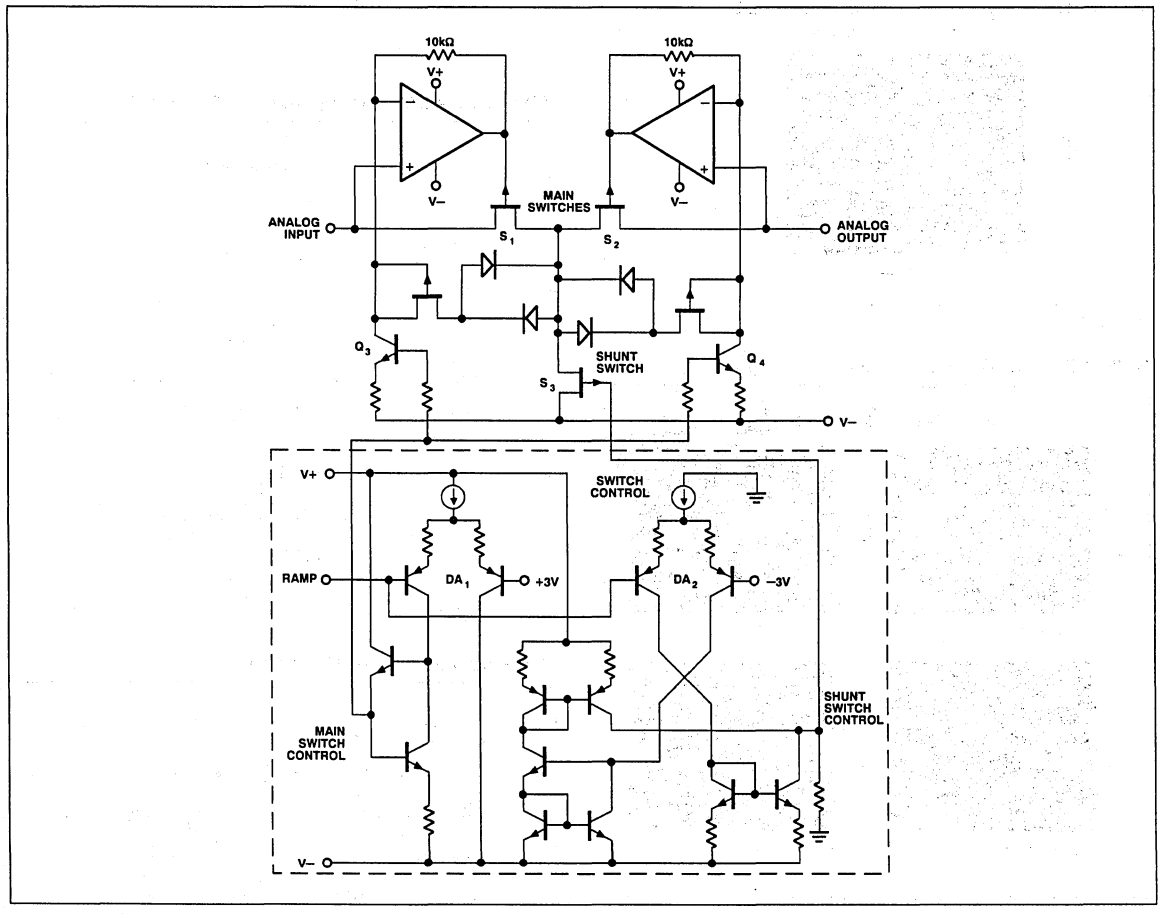
"OFF" ISOLATION TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT



SIMPLIFIED SCHEMATIC



APPLICATIONS INFORMATION

FUNCTIONAL SECTIONS

Each half of the SSM-2402/2412 are made up of three major functional blocks:

1. **"T" Switch**
   Consists of JFET switches S_1 and S_2 in series as the main switches and switch S_3 as a shunt.

2. **Ramp Generator**
   Generates a ramp voltage on command of the Control Input (see Figure 1). A LOW-to-HIGH TTL input at Control Input initiates a ramp that goes from approximately –7V to +7V in 12ms. Conversely, a HIGH-to-LOW TTL transition at Control Input will cause a downward ramp from approximately +7V to –7V in 12ms for the SSM-2402, and 4ms for the SSM-2412. The Ramp Generator also supplies the +3V and –3V reference levels for Switch Control.

3. **Switch Control**
   The ramp from the Ramp Generator section is applied to two differential amplifiers (DA_1 and DA_2) in the Switch Control block. (See Simplified Schematic). One amplifier is referenced to –3V and the other is referenced to +3V. Switch Control Outputs are:

   - **Main Switch Control** – Drives two 0.25mA current sources that control the inverting inputs of each op amp. When ON, the current sources cause a gate-to-source voltage of approximately 2.5V which is sufficient to turn off S_1 and S_2. When the current sources from Main Switch Control are OFF, each op amp acts as a unity-gain follower (V_{GS} = 0) and both switches (S_1 and S_2) will be ON.
   - **Shunt Switch Control** – Controls the Shunt Switch of the "T" configuration.

SWITCH OPERATION

Unlike conventional analog switches, the SSM-2402/2412 are designed to ramp on and off gradually over several milliseconds. The soft transition prevents popping or clicking in audio systems. Transients are minimized in active filters when the SSM-2402/2412 are used to switch component values.

To see how the SSM-2402/2412 switches work, first consider an OFF-to-ON transition. The Control Input is initially LOW and the Ramp Output is at approximately –7V. The Main Switch Control is HIGH which drives current sources Q_3 and Q_4 to 0.25mA each. These currents generate 2.5V gate-to-source back bias for each JFET switch (S_1 and S_2) which holds them OFF.

The Shunt Switch Control is negative which holds the shunt JFET S_3 ON. Undesired feedthrough signals in the series JFET switches S_1 and S_2 are shunted to the negative supply rail through S_3.

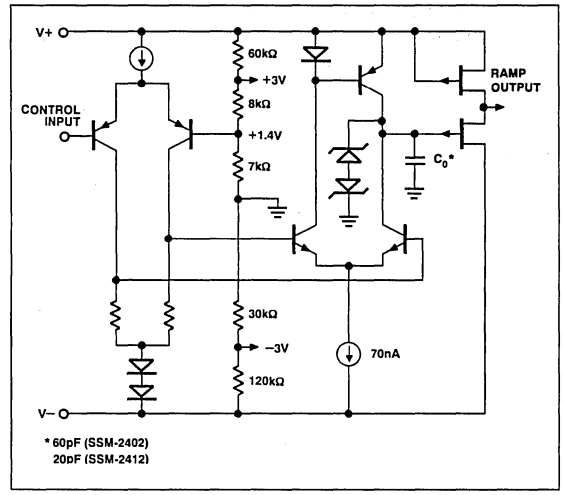


FIGURE 1: *Ramp Generator*

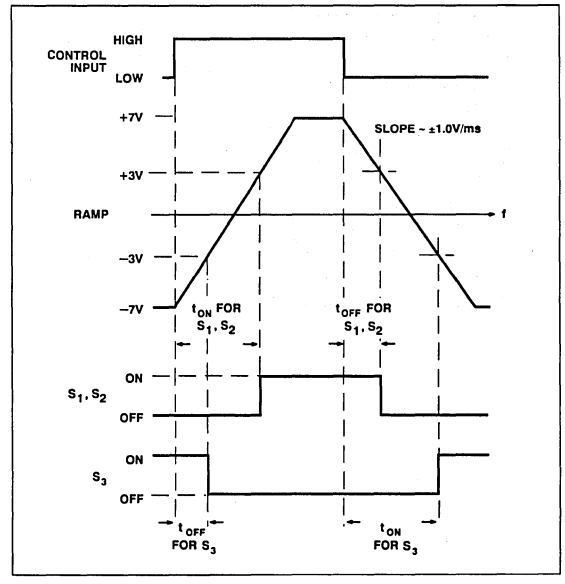


FIGURE 2: *Switch Control*

When the Control Input goes from LOW to HIGH, the Ramp Generator slews in the positive direction as shown in Figure 2. When the ramp goes more positive than –3V, the Shunt Switch Control is pulled positive by differential amplifier DA_2 which thereby puts shunt switch S_3 into the OFF state. Note that S_1 and S_2 are still OFF, so at this time all three switches in the "T" are OFF.

When the Ramp Output reaches +3V, and the drive for the Main Switch Control output is gated OFF by differential amplifier DA_1, current sources Q_3 and Q_4 go to the OFF state and the V_{GS} of each main switch goes to zero. The high-speed op amp followers provide essentially zero gate-to-source voltage over the full audio signal range; this in turn assures a constant low impedance in the ON state over the full audio signal range. Total time to turn on the SSM-2402 switch is approximately 10.0ms and 3.5ms for the SSM-2412.

In systems using a large number of separate switches, there are advantages to having faster switching into OFF state than into the ON state. Break-before-make can be maintained at the system level. To see how the SSM-2402/2412 guarantee break-before-make, consider the ON-to-OFF transition.

A Control Input LOW initiates the ON-to-OFF transition. The Ramp Generator integrates down from approximately +7V towards –7V. As the ramp goes through +3V, the comparator controlling the Main Switches (S_1 and S_2) goes HIGH and turns on current sources Q_3 and Q_4 which thereby puts S_1 and S_2 into the OFF state. At this time, all switches in the "T" are OFF. When the ramp integrates down to –3V, the Shunt Switch Control changes state and pulls shunt switch S_3 into the ON state. This completes the ON-to-OFF transistion; S_1 and S_2 are OFF, and S_3 is ON to shunt away any undesired feedthrough. Note though that the ON-to-OFF time for main switches S_1 and S_2 is only the time interval required for the ramp to go from +7V to +3V, about 4ms for the SSM-2402, and 1.5ms for the SSM-2412. The time to turn on is about 2.5 times as long as the time to turn off.

The SSM-2402/2412 are much more than simple single solid-state switches. The "T" configuration provides superb OFF-isolation through shunting of feedthrough via shunt switch S_3. Break-before-make is inherent in the design. The ramp provides a controlled gating action that softens the ON/OFF transitions. Distortion is minimized by holding zero gate-to-source voltage for the two main FET switches, S_1 and S_2, using the two op amp followers. Figure 3 shows a distortion comparison between the SSM-2402 and a typical CMOS switch. In summary, the SSM-2402/2412 are designed specifically for high-performance audio system usage.

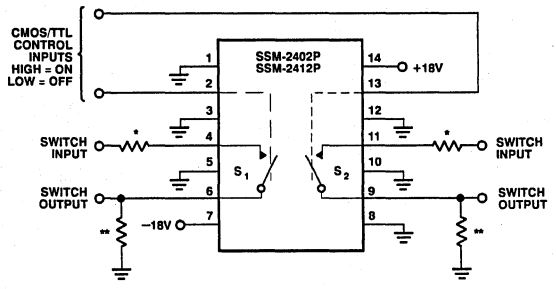
OVERVOLTAGE PROTECTION

The SSM-2402/2412 are designed to guarantee correct operation with inputs of up to ±14.2V with ±18V supplies. The switch input should never be forced to go beyond the supply rails. In the OFF condition, if the inputs exceeds +14.2V, there is a risk of turning the respective input pass FET "ON." When the input voltage rises to within 3.8V of the positive supply, the op amp follower saturates and will not be able to maintain the full 2.5V of back bias on the gate-to-source junction. Under this condition, current will flow from the input through the shunt FET to the negative supply. This current is substantial, but is limited by the FET I_{DSS}. Although this current will not damage the device, there is a danger of also turning on the output pass FET, especially if the output is close to the negative rail.

This risk of signal "breakthrough" for inputs above +14.2V can be eliminated by using a source resistor of 100-500Ω in series with the analog input to provide additional current limiting.

Near the negative supply, transistors Q_3 and Q_4 saturate and can no longer keep the switch OFF. Signal breakthrough cannot happen, but the danger here is latch-up via a path to V– through the shunt FET. Additional circuitry (not shown) has been incorporated to turn OFF the shunt FET under these conditions, and the potential for latch-up is thereby eliminated.

TYPICAL CONFIGURATION



* OPTIONAL INPUT RESISTORS
SEE SECTION ON OVERVOLTAGE PROTECTION

** OPTIONAL LOAD RESISTORS
LOWER VALUES WILL MINIMIZE "CLICKS" BUT WITH A $10V_{RMS}$ INPUT
IT IS RECOMMENDED THAT THEY BE GREATER THAN 2kΩ

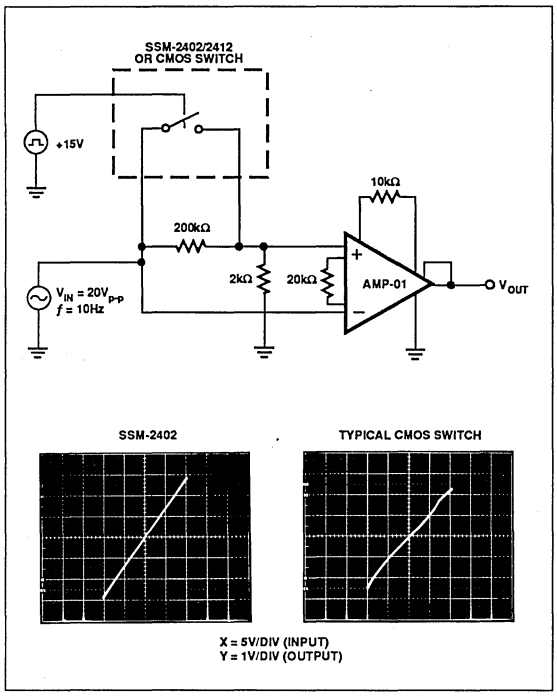


FIGURE 3: *Comparison of the SSM-2402 and Typical CMOS Switch for Distortion*

DIGITALLY-CONTROLLED ATTENUATOR

Figure 4 shows the usual approach to digitally-controlled attenuation. With S_1 closed, the signal passes unattenuated to the output. With S_1 open and S_2 closed, the signal is attenuated by R_1 and R_2. The advantage of this configuration is that the attenuator current does not have to flow through the switches. The disadvantage is that the output is undefined during the switching period, which can be several milliseconds.

The low distortion characteristics of the SSM-2402/2412 enable the alternate arrangement of Figure 5 to be used. Now only one switch is required to change between two gains, and there is always a signal path to the output. Values for R_2 will typically be in the low kilohm range.

For more gain steps and higher attenuation, the ladder arrangement of Figure 6 can be used. This enables a wide dynamic range to be achieved without the need for large value resistors, which would result in degradation of the noise performance.

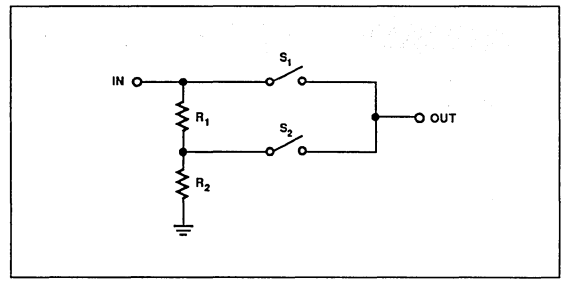


FIGURE 4

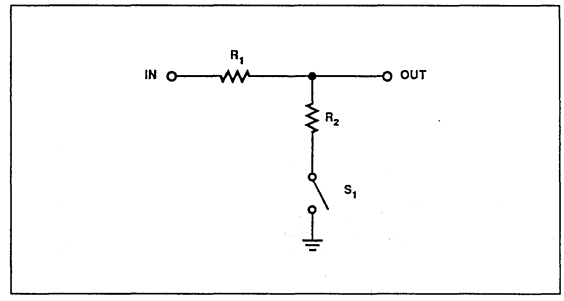


FIGURE 5

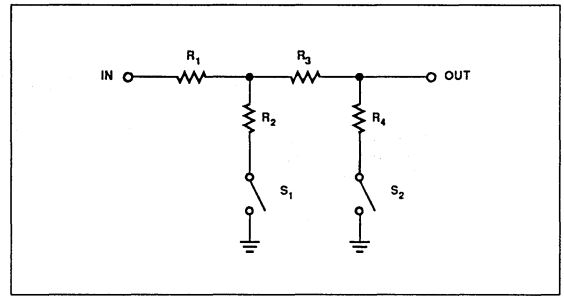


FIGURE 6

SSM-2141

HIGH COMMON-MODE REJECTION DIFFERENTIAL LINE RECEIVER

FEATURES

- **High Common-Mode Rejection**
  - **DC ..... 100dB Typ**
  - **60Hz ..... 100dB Typ**
  - **20kHz ..... 70dB Typ**
  - **40kHz ..... 62dB Typ**
- **Low Distortion ..... 0.001% Typ**
- **Fast Slew Rate ..... 9.5V/μs Typ**
- **Wide Bandwidth ..... 3MHz Typ**
- **Low Cost**
- **Complements SSM-2142 Differential Line Driver**

APPLICATIONS

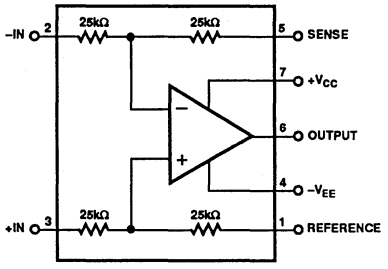
- **Line Receivers**
- **Summing Amplifiers**
- **Buffer Amplifiers – Drives 600Ω Load**

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	
SSM2141P	XIND*

*XIND = $-40°C \leq T_A \leq +85°C$

FUNCTIONAL DIAGRAM



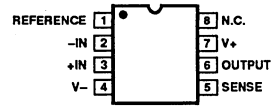
GENERAL DESCRIPTION

The SSM-2141 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of noise immunity and optimum common-mode rejection. The SSM-2141 typically achieves 100dB of common-mode rejection (CMR), whereas implementing an op amp with four off-the-shelf precision resistors will typically achieve only 40dB of CMR – inadequate for high-performance audio.

The SSM-2141 achieves low distortion performance by maintaining a large slew rate of 9.5V/μs and high open-loop gain. Distortion is less than 0.002% over the full audio bandwidth. The SSM-2141 complements the SSM-2142 balanced line driver. Together, these devices comprise a fully integrated solution for equivalent transformer balancing of audio signals without the problems of distortion, EMI fields, and high cost.

Additional applications for the SSM-2141 include summing signals, differential preamplifiers, and 600Ω low distortion buffer amplifiers.

PIN CONNECTIONS



8-PIN PLASTIC MINI-DIP (P-Suffix)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage (Note 1) ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P Package ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... +150°C
Operating Temperature Range ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	103	43	°C/W

NOTES:
1. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±18V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2141 MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}	V_{CM} = 0V	–1000	25	1000	µV
Gain Error		No Load, V_{IN} = ±10V, R_S = 0Ω	–	0.001	0.01	%
Input Voltage Range	IVR	(Note 1)	±10	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±10V	80	100	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	–	0.7	15	µV/V
Output Swing	V_O	R_L = 2kΩ	±13	±14.7	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted To Ground	+45/–15	–	–	mA
Small-Signal Bandwidth (–3dB)	BW	R_L = 2kΩ	–	3	–	MHz
Slew Rate	SR	R_L = 2kΩ	6	9.5	–	V/µs
Total Harmonic Distortion	THD	R_L = 100kΩ R_L = 600Ω	– –	0.001 0.01	– –	%
Capacitive Load Drive Capability	C_L	No Oscillation	–	300	–	pF
Supply Current	I_{SY}	No Load	–	2.5	3.5	mA

NOTE:
1. Input voltage range guaranteed by CMR test.

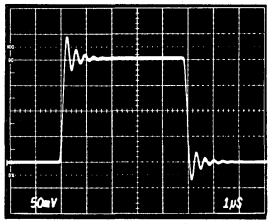
ELECTRICAL CHARACTERISTICS at V_S = ±18V, –40°C ≤ T_A ≤ +85°C.

PARAMETER	SYMBOL	CONDITIONS	SSM-2141 MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}	V_{CM} = 0V	–2500	200	2500	µV
Gain Error		No Load, V_{IN} = ±10V, R_S = 0Ω	–	0.002	0.02	%
Input Voltage Range	IVR	(Note 1)	±10	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±10V	75	90	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	–	1.0	20	µV/V
Output Swing	V_O	R_L = 2kΩ	±13	±14.7	–	V
Slew Rate	SR	R_L = 2kΩ	–	9.5	–	V/µs
Supply Current	I_{SY}	No Load	–	2.6	4.0	mA

NOTE:
1. Input voltage range guaranteed by CMR test.

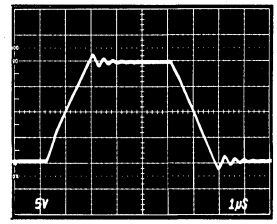
TYPICAL PERFORMANCE CHARACTERISTICS

SMALL-SIGNAL TRANSIENT RESPONSE



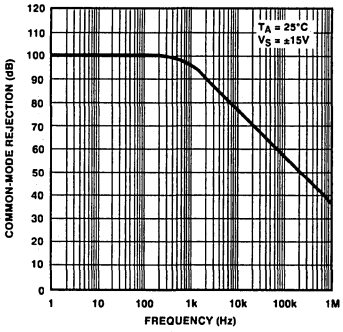
T_A = +25°C
V_S = ±15V

LARGE-SIGNAL TRANSIENT RESPONSE

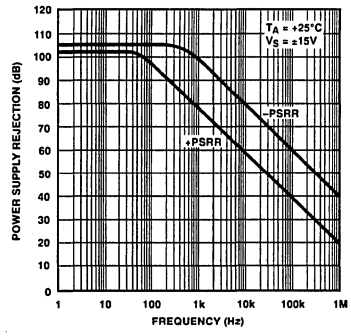


T_A = +25°C
V_S = ±15V

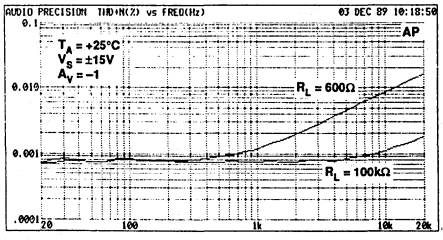
COMMON-MODE REJECTION vs FREQUENCY



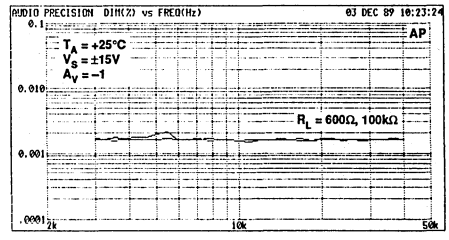
POWER SUPPLY REJECTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

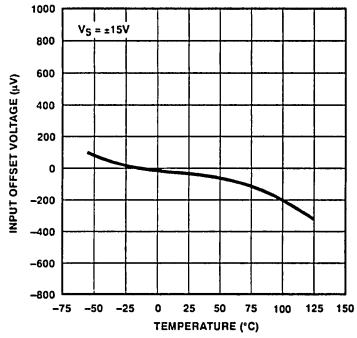


DYNAMIC INTERMODULATION DISTORTION vs FREQUENCY

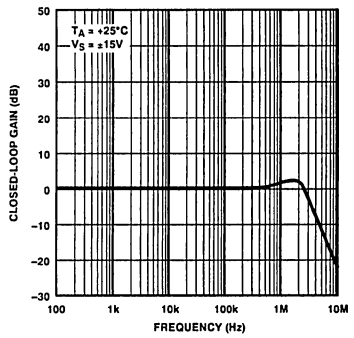


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

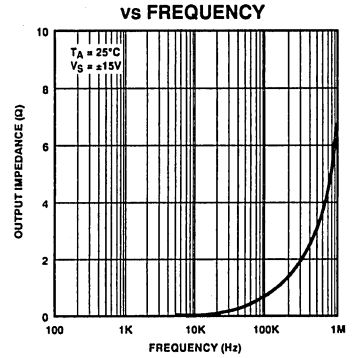
INPUT OFFSET VOLTAGE vs TEMPERATURE



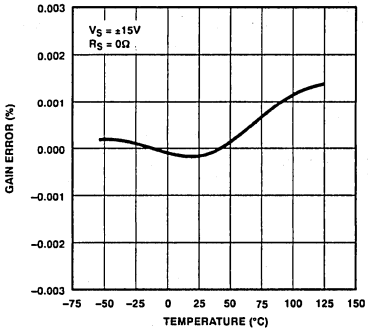
CLOSED-LOOP GAIN vs FREQUENCY



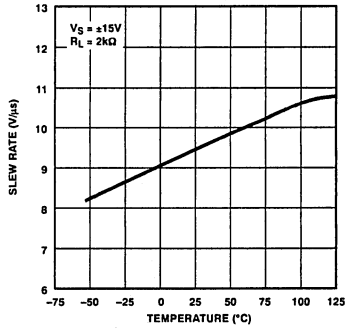
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



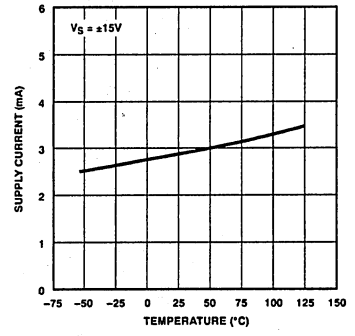
GAIN ERROR vs TEMPERATURE



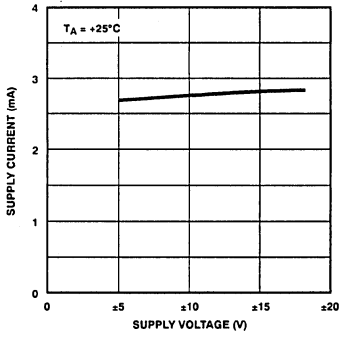
SLEW RATE vs TEMPERATURE



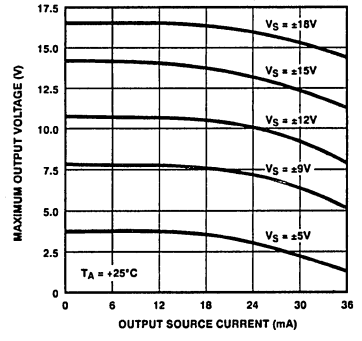
SUPPLY CURRENT vs TEMPERATURE



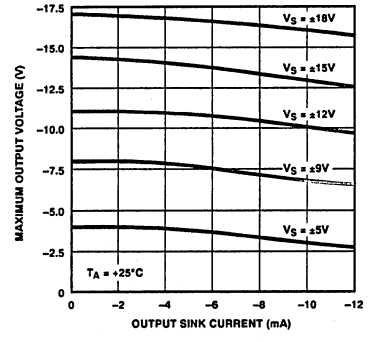
SUPPLY CURRENT vs SUPPY VOLTAGE



MAXIMUM OUTPUT VOLTAGE vs OUTPUT CURRENT (SOURCE)

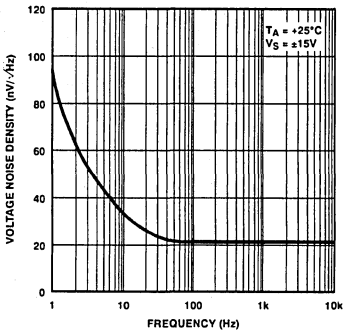


MAXIMUM OUTPUT VOLTAGE vs OUTPUT CURRENT (SINK)

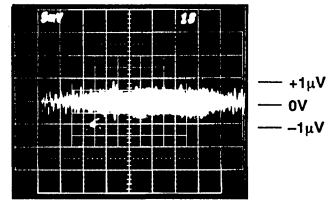


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

VOLTAGE NOISE DENSITY vs FREQUENCY

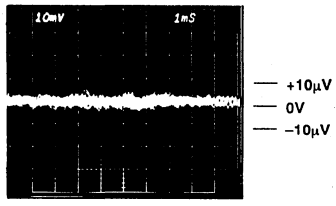


LOW FREQUENCY VOLTAGE NOISE



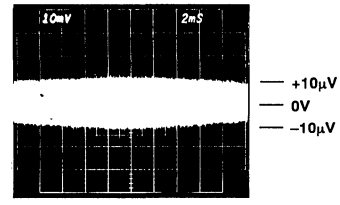
0.1 TO 10Hz PEAK-TO-PEAK NOISE

VOLTAGE NOISE FROM 0 TO 1kHz



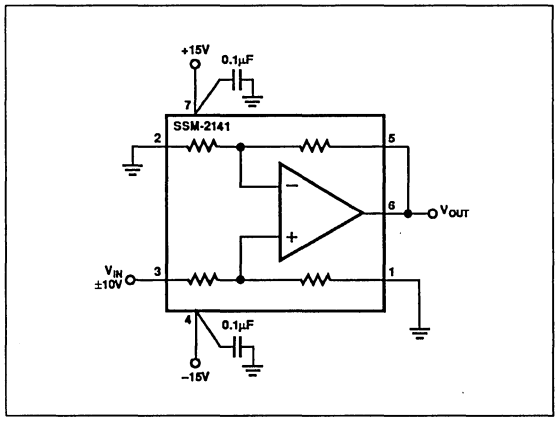
T_A = +25°C
V_S = ±15V
NOTE: EXTERNAL AMPLIFIER GAIN = 1000;
THEREFORE, VERTICAL SCALE = 10μV/DIV.

VOLTAGE NOISE FROM 0 TO 10kHz



T_A = +25°C
V_S = ±15V
NOTE: EXTERNAL AMPLIFIER GAIN = 1000;
THEREFORE, VERTICAL SCALE = 10μV/DIV.

SLEW RATE TEST CIRCUIT



APPLICATIONS INFORMATION

The SSM-2141 represents a versatile analog building block. In order to capitalize on fast settling time, high slew rate, and high CMR, proper decoupling and grounding techniques must be employed. For decoupling, place 0.1µF capacitor located within close proximity from each supply pin to ground.

MAINTAINING COMMON-MODE REJECTION

In order to achieve the full common-mode rejection capability of the SSM-2141, the source impedance must be carefully controlled. Slight imbalances of the source resistance will result in a degradation of DC CMR – even a 5Ω imbalance will degrade CMR by 20dB. Also, the matching of the reactive source impedance must be matched in order to preserve theCMRR over frequency.

APPLICATION CIRCUITS

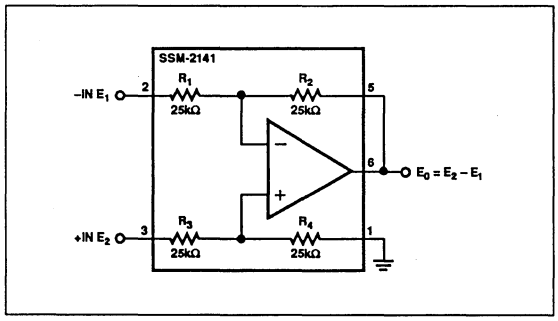


FIGURE 1: *Precision Difference Amplifier. Rejects Common-Mode Signal =* $\frac{[E_1 + E_2]}{2}$ *by 100dB*

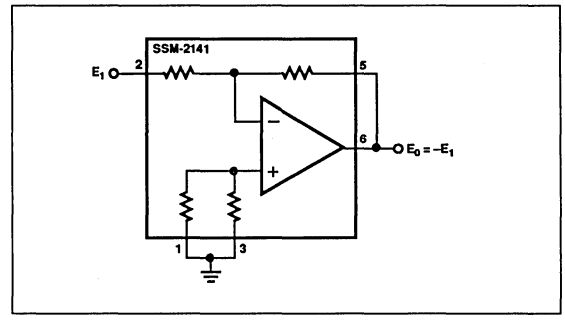


FIGURE 2: *Precision Unity-Gain Inverting Amplifier*

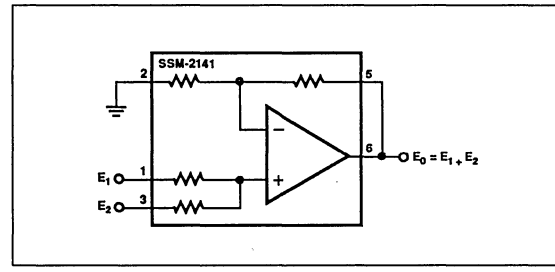


FIGURE 3: *Precision Summing Amplifier*

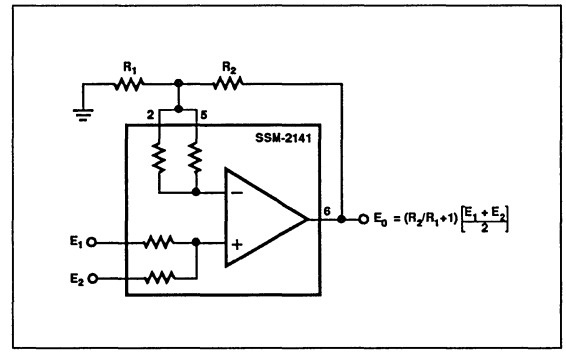


FIGURE 4: *Precision Summing Amplifier with Gain*

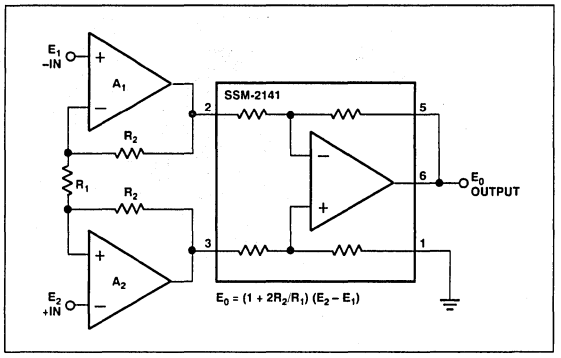


FIGURE 5: *Suitable instrumentation amplifier requirements can be addressed by using an input stage consisting of A_1, A_2, R_1 and R_2.*

PMI

Audio Silicon Specialists™

SSM-2142
BALANCED
LINE DRIVER

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- Transformer-Like Output
- Drives $10V_{RMS}$ into a 600Ω Load
- Low Gain Error (Differential or Single-Ended) ..... < 0.1%
- Low Supply Current (Quiescent) ..... 8mA Max
- High Slew Rate 15V/μs
- Short-Circuit Protected Outputs
- Space Saving 8-Pin Mini-DIP
- No External Components Required

APPLICATIONS

- Audio Mix Consoles
- Graphic and Parametric Equalizers
- Dynamic Range Processors
- Digital Effects Processors
- High Performance Hi-Fi
- Instrumentation Equipment

ORDERING INFORMATION

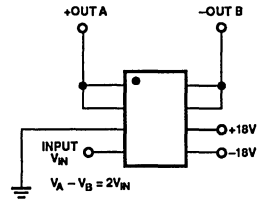
PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	
SSM2142P	XIND*

* XIND = −40°C to +85°C

GENERAL DESCRIPTION

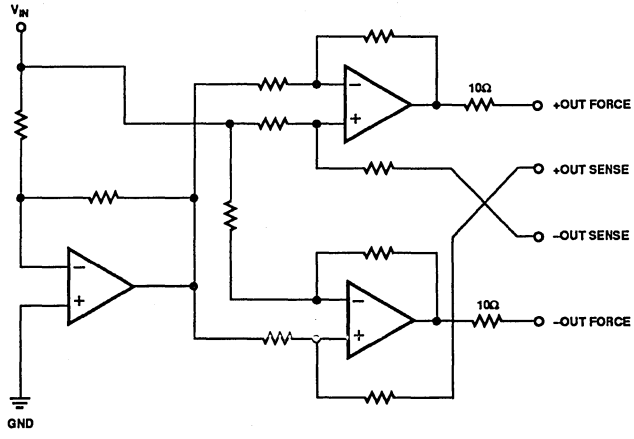
The SSM-2142 is a fully integrated processing block used to derive precision balanced outputs from a single-ended input in high performance audio systems. The output, which drives a 600Ω load from a $10V_{RMS}$ signal, functions very similar to transformer-based circuits. Low gain error and high slew rate further enhance the SSM-2142, making it the ideal output device in systems requiring balanced or differential outputs with high drive capability.

TYPICAL APPLICATION



8-PIN PLASTIC DIP
(P-Suffix)

BLOCK DIAGRAM



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

SSM-2131

ULTRA-LOW DISTORTION, HIGH-SPEED AUDIO OPERATIONAL AMPLIFIER

FEATURES

- **Low Distortion – DC to 40kHz, A_V = +10 ..... 0.01% Typ**
- **High Slew Rate ..... 40V/μs Min**
- **Gain-Bandwidth Product ..... 10MHz Typ**
- **High Gain ..... 200,000 Typ**
- **Common-Mode Rejection ..... 80dB Min**

APPLICATIONS

- **Power Amplifier Driver**
- **Active Filter Circuits**
- **Parametric Equalizers**
- **Graphic Equalizers**
- **Mixing Consoles**
- **Voltage Summers**
- **Active Crossover Networks**

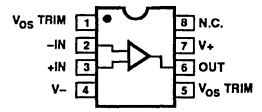
GENERAL DESCRIPTION

The SSM-2131 is a fast JFET input operational amplifier intended for use in audio applications. The SSM-2131 offers a symmetric 50V/μs slew rate for low distortion and is internally compensated for unity gain operation. Power supply current is less than 6.5mA. Unity-gain stability, a wide full-power bandwidth of 800kHz, and excellent ability to handle transient overloads make the SSM-2131 an ideal amplifier for use in high performance audio amplifier circuits.

The SSM-2131's common-mode rejection of 80dB minimum over a ±11 range is exceptional for a high-speed amplifier. High CMR, combined with a minimum 500V/mV gain into a 10kΩ load ensures excellent linearity in both noninverting and inverting gain configurations. This means that distortion will be very low over a wide range of circuit configurations. The low offset provided by the JFET input stage often eliminates the need for AC coupling or for external offset trimming.

The SSM-2131 conforms to the standard 741 pinout with nulling to V–. The SSM-2131 upgrades the performance of circuits using the AD544, AD611, AD711, and LF400 by direct replacement.

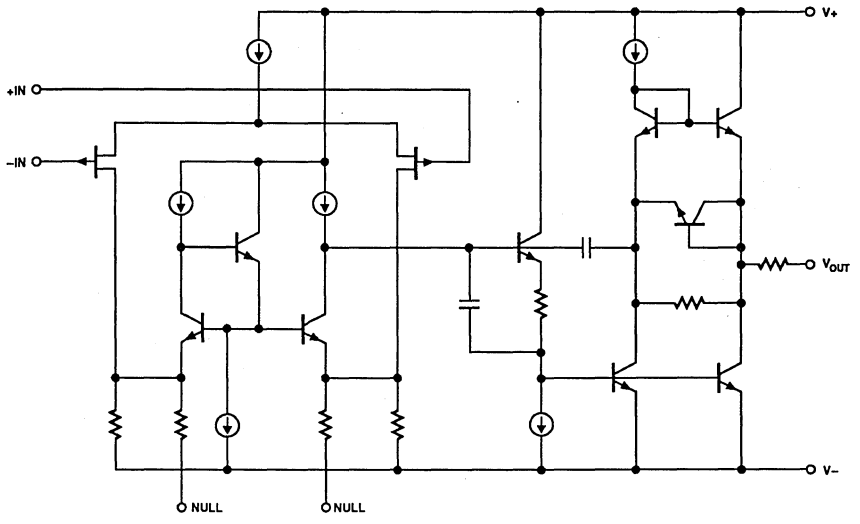
PIN CONNECTIONS



PLASTIC MINI-DIP (P-Suffix)

8-PIN SO (S-Suffix)

SIMPLIFIED SCHEMATIC



ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	SO 8-PIN	
SSM2131P	SSM2131S	XIND*

*XIND = –40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Input Voltage (Note 1) ..... ±20V
Differential Input Voltage (Note 1) 40V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +175°C
Operating Temperature Range ..... –40°C to +85°C
Junction Temperature ..... –65°C to +175°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2131 MIN	TYP	MAX	UNITS
Slew Rate	SR		40	50	–	V/µs
Gain-Bandwidth Product	GBW	f_O = 10kHz	–	10	–	MHz
Full-Power Bandwidth	BW_P	(Note 2)	600	800	–	kHz
Total Harmonic Distortion	THD	DC to 40kHz, R_L = 10kΩ, A_V = +10	–	0.01	–	%
Voltage Noise Density	e_n	f_O = 10Hz f_O = 1kHz	– –	38 13	– –	nV/√Hz
Current Noise Density	i_n	f_O = 1kHz	–	0.007	–	pA/√Hz
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ V_O = ±10V R_L = 2kΩ T_j = 25°C R_L = 1kΩ	500 200 100	900 260 170	– – –	V/mV
Output Voltage Swing	V_O	R_L = 1kΩ	±11.5	+12.5 –11.9	–	V
Offset Voltage	V_{OS}		–	1.5	6.0	mV
Input Bias Current	I_B	V_{CM} = 0V T_j = 25°C	–	130	250	pA
Input Offset Current	I_{OS}	V_{CM} = 0V T_j = 25°C	–	6	50	pA
Input Voltage Range	IVR	(Note 1)	±11.0	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	80	92	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	–	12	50	µV/V
Supply Current	I_{SY}	No Load V_O = 0V	–	5.1	6.5	mA
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+33 –28	±60	mA
Settling Time	t_s	10V Step 0.01% (Note 3)	–	0.9	1.2	µs
Overload Recovery Time	t_{OR}		–	700	–	ns

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SSM-2131 MIN	TYP	MAX	UNITS
Phase Margin	ϕ_O	0dB Gain	–	47	–	degrees
Gain Margin	A_{180}	180° Open-Loop Phase Shift	–	9	–	dB
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 4)	100	300	–	pF
Supply Voltage Range	V_S		±8	±15	±20	V

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.
3. Settling time is guaranteed but not tested.
4. Guaranteed but not tested.

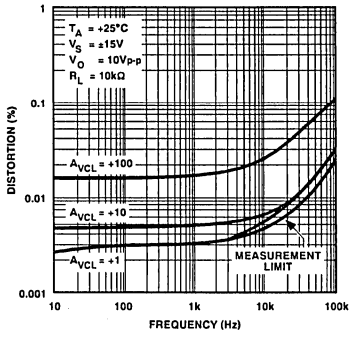
ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ 85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2131 MIN	TYP	MAX	UNITS
Slew Rate	SR	R_L = 2kΩ	40	50	–	V/µs
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ (Note 1) R_L = 2kΩ V_O = ±10V	200 100	500 160	– –	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±11.0	+12.3 –11.8	–	V
Offset Voltage	V_{OS}		–	2.0	7.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	8	–	µV/°C
Input Bias Current	I_B	(Note 1)	–	0.6	2.0	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.06	0.4	nA
Input Voltage Range	IVR	(Note 2)	±11.0	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	80	94	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	–	6	50	µV/V
Supply Current	I_{SY}	No Load V_O = 0V	–	5.1	6.5	mA
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±8	–	±60	mA

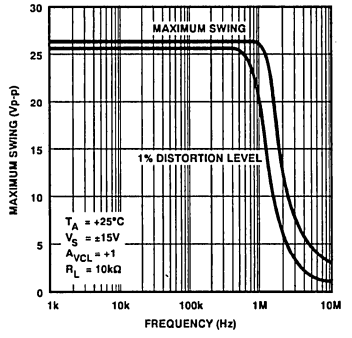
NOTES:
1. T_J = 85°C.
2. Guaranteed by CMR test.

TYPICAL PERFORMANCE CHARACTERISTICS

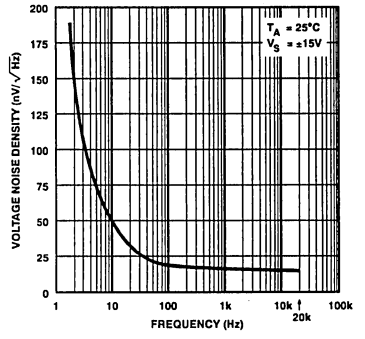
DISTORTION vs FREQUENCY



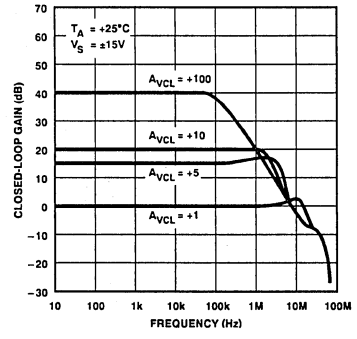
MAXIMUM OUTPUT SWING vs FREQUENCY



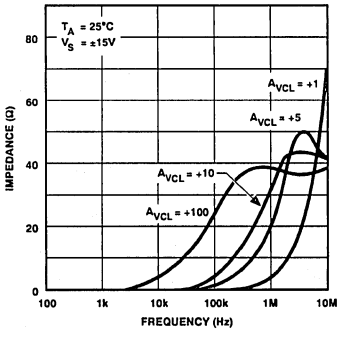
VOLTAGE NOISE DENSITY vs FREQUENCY



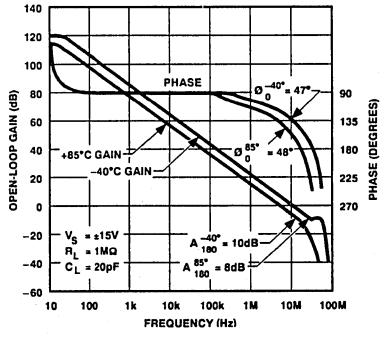
CLOSED-LOOP GAIN vs FREQUENCY



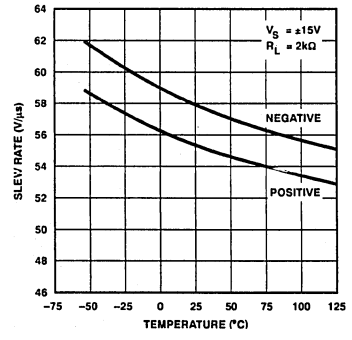
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



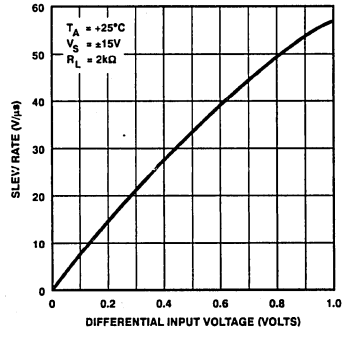
OPEN-LOOP GAIN, PHASE vs FREQUENCY



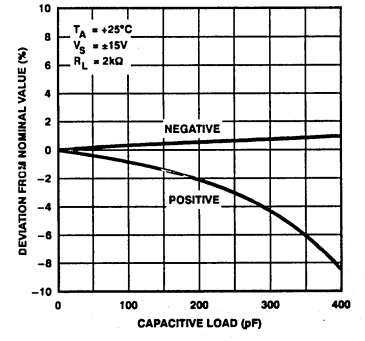
SLEW RATE vs TEMPERATURE



SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE

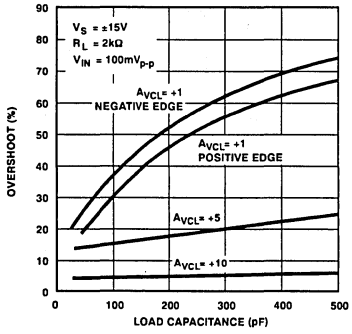


SLEW RATE vs CAPACITIVE LOAD

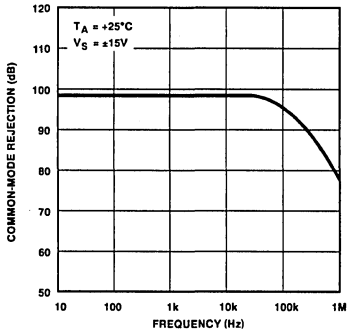


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

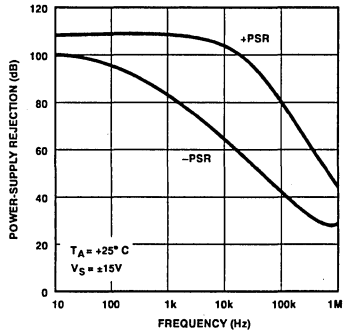
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



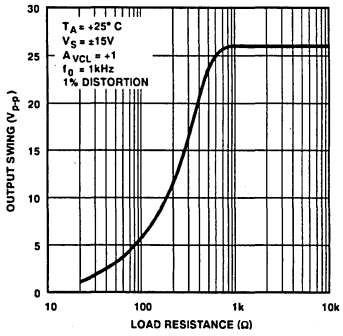
COMMON-MODE REJECTION vs FREQUENCY



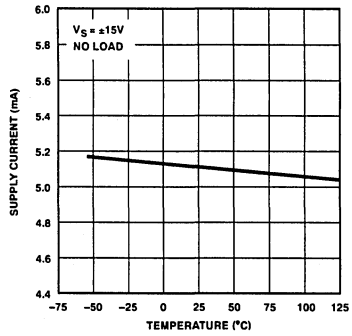
POWER-SUPPLY REJECTION vs FREQUENCY



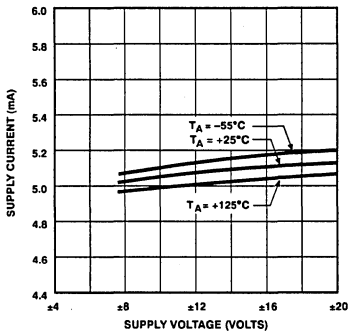
OUTPUT SWING vs LOAD RESISTANCE



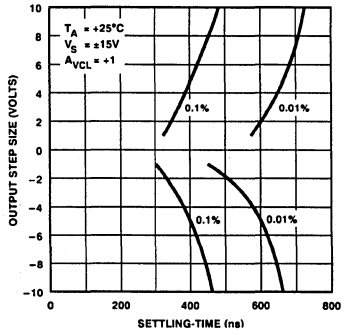
SUPPLY CURRENT vs TEMPERATURE



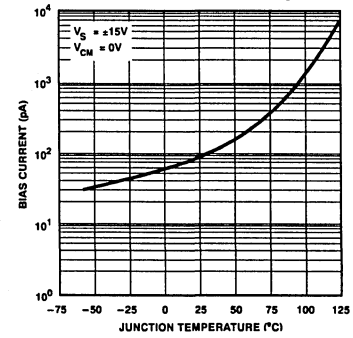
SUPPLY CURRENT vs SUPPLY VOLTAGE



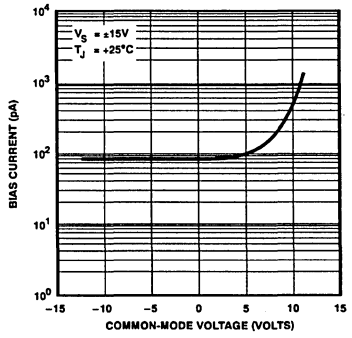
SETTLING-TIME vs STEP SIZE



BIAS CURRENT vs JUNCTION TEMPERATURE



BIAS CURRENT vs COMMON-MODE VOLTAGE



APPLICATIONS INFORMATION

The SSM-2131 combines speed with a high level of input precision usually found only with slower devices. Well-behaved AC performance in the form of clean transient response, symmetrical slew rates and a high degree of forgiveness to supply decoupling are the hallmarks of this amplifier. AC gain and phase response are quite independent of temperature or supply voltage. Figure 1 shows the SSM-2131's small-signal response. Even with 75pF loads, there is minimal ringing in the output waveform. Large-signal response is shown in Figure 2. This figure clearly shows the SSM-2131's exceptionally close matching between positive and negative slew rates. Slew rate symmetry decreases the DC offset a system encounters when processing high-frequency signals, and thus reduces the DC current necessary for load driving.

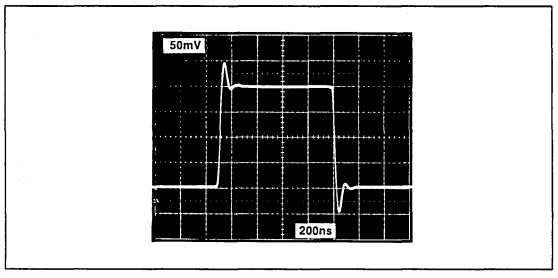


FIGURE 1: *Small-Signal Transient Response, Z_L = 2kΩ\|\|75pF*

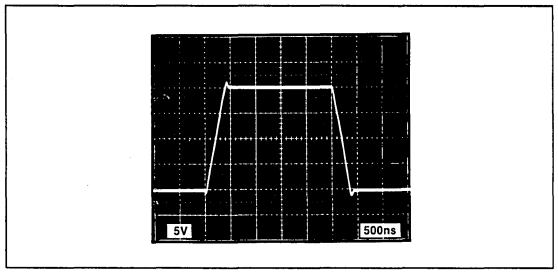


FIGURE 2: *Large-Signal Transient Response, Z_L = 2kΩ\|\|75pF*

As with most JFET-input amplifiers, the output of the SSM-2131 may undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion will not damage the amplifier, nor will it cause an internal latch-up.

Supply decoupling should be used to overcome inductance and resistance associated with supply lines to the amplifier.

For most applications, a 0.1μF to 0.01μF capacitor should be placed between each supply pin and ground.

OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted with a 10kΩ to 100kΩ potentiometer as shown in Figure 3. The potentiometer should be connected between pins 1 and 5 with its wiper connected to the V– supply.

Alternately, V_{OS} may be nulled by attaching the potentiometer wiper through a 1MΩ resistor to the positive supply rail.

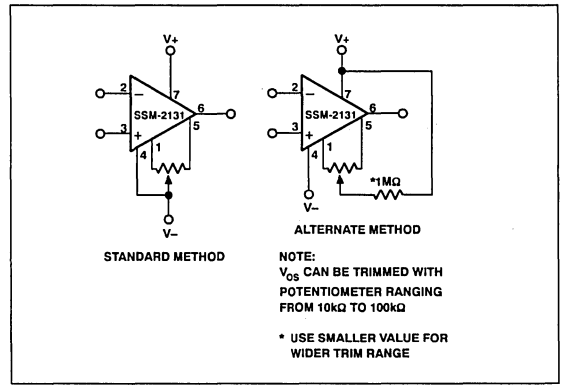


FIGURE 3: *Input Offset Voltage Nulling*

VOLTAGE SUMMING

Because of its extremely low input bias current and large unity-gain bandwidth, the SSM-2131 is ideal for use as a voltage summer or adder.

The following figures show both an inverting and noninverting voltage adder.

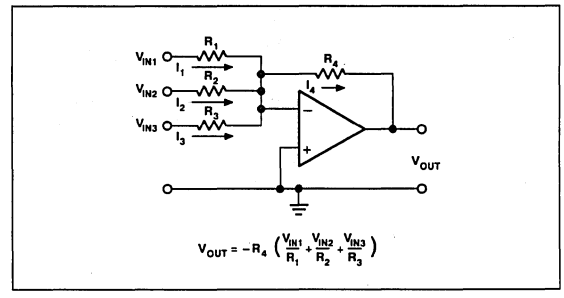


FIGURE 4: *Inverting Adder*

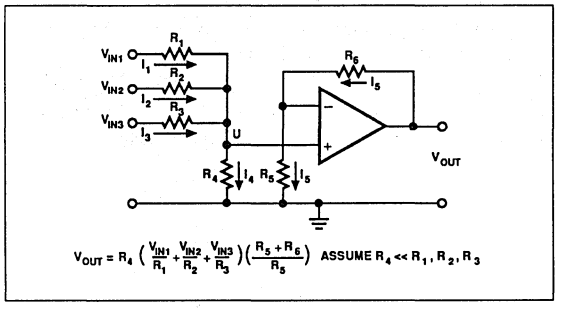


FIGURE 5: *Noninverting Adder*

CURRENT FEEDBACK AUDIO POWER AMPLIFIER

The SSM-2131 can be used as the input buffer in a current feedback audio power amplifier as shown in Figure 6. This design is capable of very good performance as shown in Figures 7, 8 and 9. At 1kHz and 50 watts output into an 8Ω load, the amplifier generates just 0.002% THD, and is flat to 1MHz. The slew rate for the overall amplifier is more than adequate at 300V/μs and is responsible for the very low dynamic intermodulation distortion (DIM-100) that was measured at just 0.0017% at 50 watts output into 8 ohms. The total amplifier idling current for all tests was approximately 300mA; the V+/V++ and V–/V— power supplies were both ±40V; and the gain was set to 24.0.

In a current feedback amplifier, a unity or low gain input buffer drives a low impedance network. Any differential current that flows in the collectors of the buffer (SSM-2131) output transistors is fed, via the two complementary Wilson current mirrors A and B, to a high impedance gain node where the high output voltage is generated.

This voltage is then buffered by a double emitter follower driver stage and fed to the complementary power MOSFET output stage. No RC compensation network to ground or output inductor is required at the output of this amplifier to make it stable. As the 100kHz square wave response shows, there's no evidence of any instability in the circuit. Capacitive load compensation can be provided by the components marked TBD on the amplifier schematic. These were not used in the test, however.

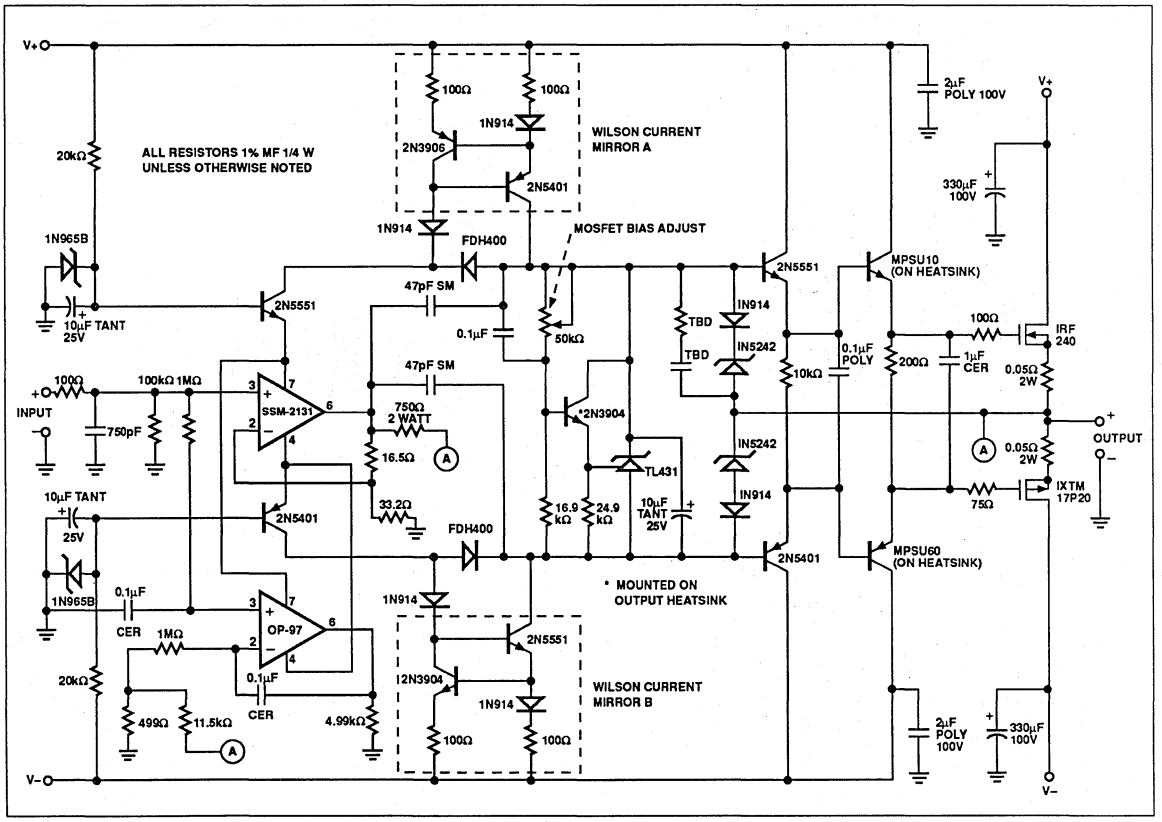


FIGURE 6: *Audio Power Amplifier Schematic*

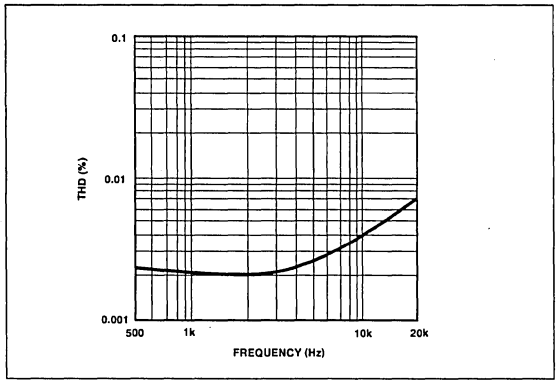


FIGURE 7: *THD vs. Frequency (at 50W into 8Ω)*

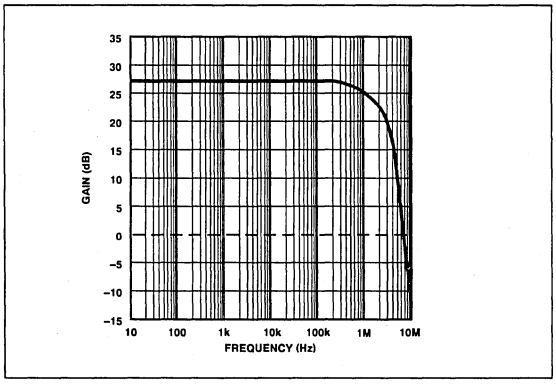


FIGURE 8: *Frequency Response*

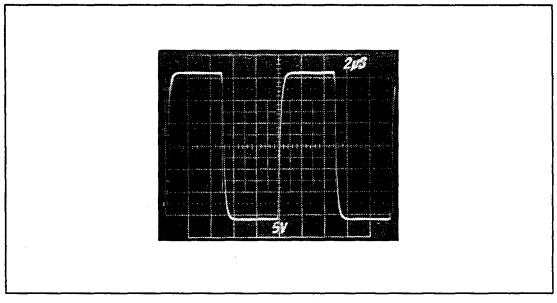


FIGURE 9: *100kHz Square Wave into 8Ω*

One problem that is commonly encountered with current feedback amplifiers is that the mismatch between the two current mirrors A and B forces a small bias current to appear at the input buffer's output terminal. This bias current (usually in the range of 1-100μA) is multiplied by the feedback resistor of 750Ω and generates an output offset that could be tens of millivolts in magnitude. Matched transistors could be used in the current mirrors, but these do not completely eliminate the output offset problem.

An inexpensive solution is to use a low power precision DC op amp, such as the OP-97, to control the amplifier's DC characteristics, thus overriding the DC offset due to mismatch in the current feedback loop. The OP-97 acts as a current output DC-servo amplifier that injects a compensating current into the emitters of the low voltage regulator transistors (that power the SSM-2131) to correct for current mirror mismatch. Since the OP-97 is set for an overall input-to-output gain of 24.0 as well, the DC output offset is equal to the OP-97's V_{OS} x 24.0, which is roughly 1 millivolt. Thus, any offset trimming can be completely eliminated. Together, the SSM-2131 and OP-97 provide a level of performance that exceeds most of the requirements for audio power amplifers. The driver circuit can handle several pairs of power MOSFETs in the output stage if required. This topology can be used in circuits that must deliver several hundreds of watts to a load by using higher voltage transistors in the driver stage. Operation with rail voltages in excess of ±100V is possible. If more gain is desired, the SSM-2131 input buffer can have its gain increased from the nominal value of 1.5 used in this example to as much as 10 before its bandwidth drops below that of the current feedback section.

DRIVING A HIGH-SPEED ADC

The SSM-2131's open-loop output resistance is approximately 50Ω. When feedback is applied around the amplifier, output resistance decreases in proportion to closed-loop gain divided by open-loop gain (A_{VCL}/A_{VOL}). Output impedance increases as open-loop gain rolls-off with frequency. High-speed analog-to-digital converters require low source impedances at high frequency. Output impedance at 1MHz is typically 5Ω for an SSM-2131 operating at unity-gain. If lower output impedances are required, an output buffer may be placed at the output of the SSM-2131.

HIGH-CURRENT OUTPUT BUFFER

The circuit in Figure 10 shows a high-current output stage for the SSM-2131 capable of driving a 75Ω load with low distortion. Output current is limited by R_1 and R_2. For good tracking between the output transistors Q_1, Q_2, and this biasing diodes D_1 and D_2, thermal contact must be maintained between the transistor and its associated diode. If good thermal contact is not maintained, R_1 and R_2 must be increased to 5-6Ω in order to prevent thermal runaway. Using 5Ω resistors, the circuit easily drives a 75Ω load (Figure 11). Output resistance is decreased and heavier loads may be driven by decreasing R_1 and R_2.

Base current and biasing for Q_1 and Q_2 are provided by two current sources, the SSM-2131 and the JFET. The 2kΩ potentiometer in the JFET current source should be trimmed for optimum transient performance. The case of the SSM-2210 should be connected to V–, and decoupled to ground with a 0.1μF capacitor. Compensation for the SSM-2131's input capacitance is provided by C_C. The circuit may be operated at any gain, in the usual op amp configurations.

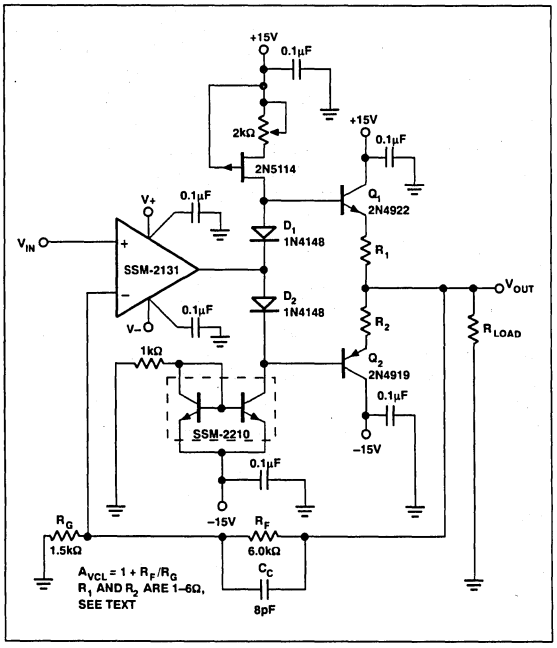


FIGURE 10: *High-Current Output Buffer*

DRIVING CAPACITIVE LOADS

Best performance will always be achieved by minimizing input and load capacitances around any high-speed amplifier. However, the SSM-2131 is guaranteed capable of driving a 100pF capacitive load over its full operating temperature range while

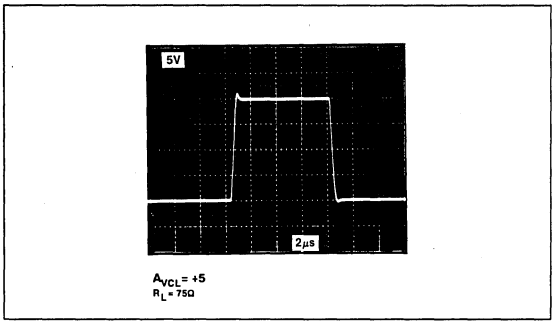


FIGURE 11: *Output Buffer Large-Signal Response*

operating at any gain including unity. Typically, an SSM-2131 will drive more than 250pF at any temperature. Supply decoupling does affect capacitive load driving ability. Extra care should be given to ensure good decoupling when driving capacitive loads; between 1μF and 10μF should be placed on each supply rail.

Large capacitive loads may be driven utilizing the circuit shown in Figure 12. R_1 and C_1 introduce a small amount of feedforward compensation around the amplifier to counteract the phase lag induced by the ouput impedance and load capacitance. At DC and low frequencies, R_1 is contained within the feedback loop. At higher frequencies, feedforward compensation becomes increasingly dominant, and R_1's effect on output impedance will become more noticeable.

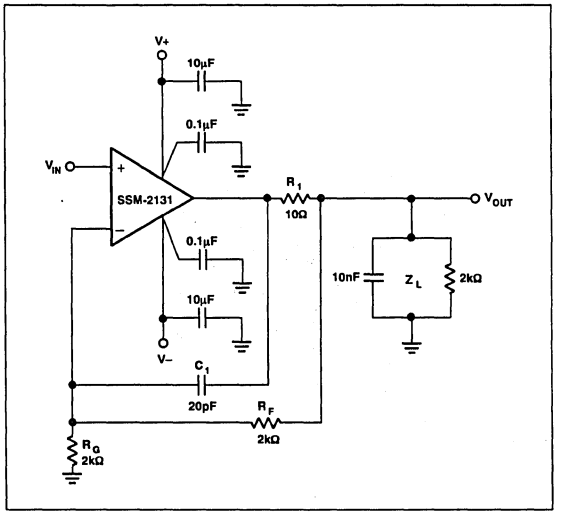


FIGURE 12: *Compensation for Large Capacitive Loads*

When driving very large capacitances, slew rate will be limited by the short-circuit current limit. Although the unloaded slew rate is insensitive to variations in temperature, the output current limit has a negative temperature coefficient, and is asymmetrical with regards to sourcing and sinking current. Therefore, slew rate into excessive capacities will decrease with increasing temperature, and will lose symmetry.

DAC OUTPUT AMPLIFIER

The SSM-2131 is an excellent choice for a DAC output amplifier, since its high speed and fast settling-time allow quick transitions between codes, even for full-scale changes in output level. The DAC output capacitance appears at the operational amplifier inputs, and must be compensated to ensure optimal settling speed. Compensation is achieved with capacitor C in Figure 13. C must be adjusted to account for the DAC's output capacitance, the op amp's input capacitance, and any stray capacitance at the inputs. With a bipolar DAC, an additional shunt resistor may be used to optimize response. This technique is described in PMI's application AN-24.

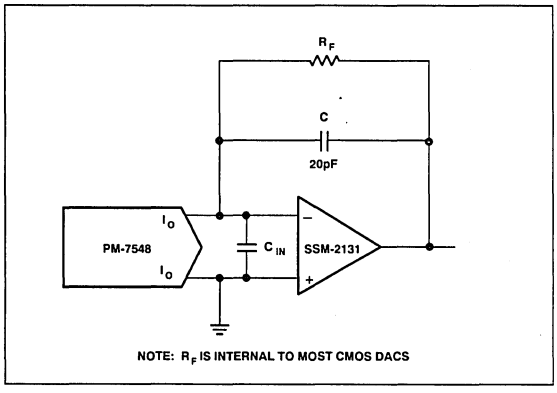


FIGURE 13: *DAC Output Amplifier Circuit*

Highest speed is achieved using bipolar DACs such as PMI's DAC-08, DAC-10 or DAC-312. The output capacitances of these converters are up to an order of magnitude lower than their CMOS counterparts, resulting in substantially faster settling-times. The high output impedance of bipolar DACs allows the output amplifier to operate in a true current-to-voltage mode, with a noise gain of unity, thereby retaining the amplifier's full bandwidth. Offset voltage has minimal effect on linearity with bipolar converters.

CMOS digital-to-analog converters have higher output capacitances and lower output resistances than bipolar DACs. This results in slower settling-times, higher sensitivity to offset voltages and a reduction in the output amplifier's bandwidth. These tradeoffs must be balanced against the CMOS DAC's advantages in terms of interfacing capability, power dissipation, accuracy levels and cost. Using the internal feedback resistor which is present on most CMOS converters, the gain applied to offset voltage varies between 4/3 and 2, depending upon output code. Contributions to linearity error will be as much as 2/3 V_{OS}. In a 10-volt 12-bit system, this may add up to an additional 1/5LSB DNL with the SSM-2131. Amplifier bandwidth is reduced by the same gain factor applied to offset voltage, however the SSM-2131's 10MHz gain-bandwidth product results in no reduction of the CMOS converter's multiplying bandwidth.

Individual DAC data sheets should be consulted for more complete descriptions of the converters and their circuit applications.

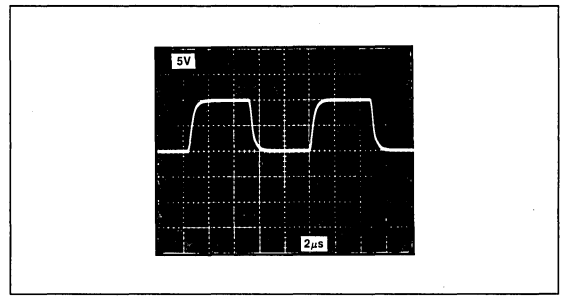


FIGURE 14: *DAC Output Amplifier Response (PM-7545 DAC)*

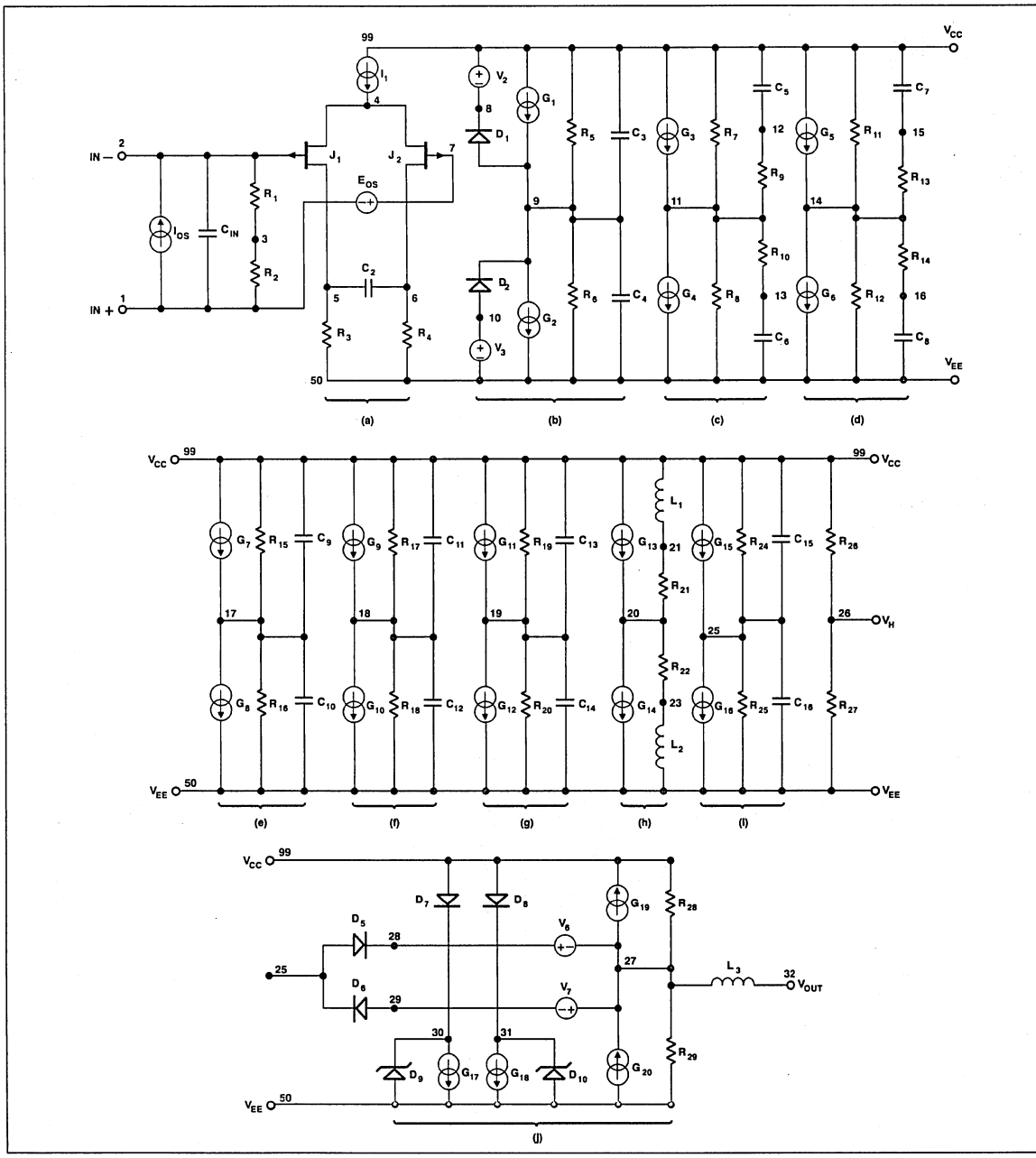
COMPUTER SIMULATIONS

The following pages show the SPICE macro-model for the SSM-2131 high-speed audio operational amplifier. This model was tested with, and is compatible with PSpice* and HSPICE**. The schematic and net-list are included here so that the model can easily be used. This model can accommodate multiple frequency poles and multiple zeroes, which is an advanced concept that results in more accurate AC and transient responses necessary for simulating the behavior of today's high-speed op amps. For example, 8 poles and 2 zeroes are required to sufficiently simulate the SSM-2131, which this advanced model can easily accommodate.

Throughout the SSM-2131 macro-model, RC networks produce the multiple poles and zeroes which simulate the SSM-2131's AC behavior. Each stage contains a pole or a pole-zero pair. The stages are separated from each other by voltage-controlled current sources so that the poles and zero locations do not interact. The only nonlinear elements in the entire model are two p-channel JFETs which comprise the input stage. Limiting the model to almost entirely linear circuit elements significantly reduces simulation time and simplifies model development.

*PSpice is a registered trademark of MicroSim Corporation.
**HSPICE is a tradmark of Meta-Software, Inc.

```
SSM-2131 MACRO-MODEL  © PMI 1989
*
* subckt SSM-2131  1  2 32  99  50
*
* INPUT STAGE & POLE AT 15.9 MHz
*
r1   1   3        5E11
r2   2   3        5E11
r3   5   50       707.36
r4   6   50       707.36
cin  1   2        5E-12
c2   5   6        7.08E-12
i1   99  4        1E-3
ios  1   2        4E-12
eos  7   1        poly(1) 20 26 1E-3 1
j1   5   2   4    jx
j2   6   7   4    jx
*
* SECOND STAGE & POLE AT 45 Hz
*
r5   9   99       176.84E6
r6   9   50       176.84E6
c3   9   99       20E-12
c4   9   50       20E-12
g1   99  9        poly(1) 5 6 3.96E-3 1.4137E-3
g2   9   50       poly(1) 6 5 3.96E-3 1.4137E-3
v2   99  8        2.5
v3   10  50       3.1
d1   9   8        dx
d2   10  9        dx
*
* POLE-ZERO PAIR AT 1.80 MHz/2.20 MHz
*
r7   11  99       1E6
r8   11  50       1E6
r9   11  12       4.5E6
r10  11  13       4.5E6
c5   12  99       16.1E-15
c6   13  50       16.1E-15
g3   99  11       9  26  1E-6
g4   11  50       26  9  1E-6
*
* POLE-ZERO PAIR AT 1.80 MHz/2.20 MHz
*
r11  14  99       1E6
r12  14  50       1E6
r13  14  15       4.5E6
r14  14  16       4.5E6
c7   15  99       16.1E-15
c8   16  50       16.1E-15
g5   99  14       11 26 1E-6
g6   14  50       26 11 1E-6
*
* POLE AT 53 MHz
*
r15  17  99       1E6
r16  17  50       1E6
c9   17  99       3E-15
c10  17  50       3E-15
g7   99  17       14 26 1E-6
g8   17  50       26 14 1E-6
*
* POLE  AT 53 MHz
*
r17  18  99       1E6
r18  18  50       1E6
c11  18  99       3E-15
c12  18  50       3E-15
g9   99  18       17 26 1E-6
g10  18  50       26 17 1E-6
*
* POLE AT 53 MHz
*
r19  19  99       1E6
r20  19  50       1E6
c13  19  99       3E-15
c14  19  50       3E-15
g11  99  19       18 26 1E-6
g12  19  50       26 18 1E-6
*
*COMMON-MODE GAIN NETWORK WITH ZERO AT 100 kHZ
*
r21  20  21       1E6
r22  20  23       1E6
l1   21  99       1.5915
l2   23  50       1.5915
g13  99  20       3  26 1E-11
g14  20  50       26  3 1E-11
*
*POLE AT 79.6 MHz
*
r24  25  99       1E6
r25  25  50       1E6
c15  25  99       2E-15
c16  25  50       2E-15
g15  99  25       19 26 1E-6
g16  25  50       26 19 1E-6
*
*OUTPUT STAGE
*
r26  26  99       111.1E3
r27  26  50       111.1E3
r28  27  99       90
r29  27  50       90
l3   27  32       2.5E-7
g17  30  50       25 27 11.1111E-3
g18  31  50       27 25 11.1111E-3
g19  27  99       99 25 11.1111E-3
g20  50  27       25 50 11.1111E-3
v6   28  27       0.7
v7   27  29       0.7
d5   25  28       dx
d6   29  25       dx
d7   99  30       dx
d8   99  31       dx
d9   50  30       dy
d10  50  31       dy
*
* MODELS USED
*
.model jx PJF(BETA=999.3E-6  VTO=-2.000  IS=4E-11)
.model dx    D(IS=1E-15)
.model dy    D(IS=1E-15 BV=50)
.ends SSM-2131
```


99
V_{CC}
I_1
4
V_2
8
D_1
G_1
R_5
C_3
G_3
R_7
C_5
12
R_9
R_{10}
13
C_6
G_5
R_{11}
C_7
15
R_{13}
R_{14}
16
C_8
G_6
R_{12}
14
11
9
2
IN –
1
IN +
J_1
J_2
7
E_{OS}
I_{OS}
C_{IN}
3
R_1
R_2
C_2
5
6
R_3
R_4
D_2
10
V_3
G_2
R_6
C_4
G_4
R_8
50
V_{EE}
(a)
(b)
(c)
(d)
L_1
L_2
G_7 R_{15} C_9
G_9 R_{17} C_{11}
G_{11} R_{19} C_{13}
G_{13} 21 R_{21}
G_{15} R_{24} C_{15} R_{26}
17
18
19
20
25
26
V_H
G_8 R_{16} C_{10}
G_{10} R_{18} C_{12}
G_{12} R_{20} C_{14}
G_{14} 23 R_{22}
G_{16} R_{25} C_{16} R_{27}
(e)
(f)
(g)
(h)
(i)
D_5
D_6
D_7
D_8
28
29
25
V_6
V_7
G_{19}
R_{28}
27
L_3
32
V_{OUT}
30
31
D_9
G_{17}
G_{18}
D_{10}
G_{20}
R_{29}
(j)

PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

SSM-2132

DUAL AUDIO OPERATIONAL AMPLIFIER

ADVANCE PRODUCT INFORMATION

FEATURES

- Low Input Noise Voltage ..... 6nV/$\sqrt{Hz}$
- High Slew Rate 15V/μs
- Low Supply Current (per Amplifier) 4mA
- High Output Drive ..... $10V_{RMS}$ into 600Ω
- Wide Gain Bandwidth Product ..... 16 MHz
- Extended Industrial Temperature Range ..... –40°C to +85°C
- Unity-Gain Stability
- Low Cost

APPLICATIONS

- Audio Mix Consoles
- Dynamic Range Processors
- Power Amplifiers
- Consumer Hi-Fi Equipment
- Graphic and Parametric Equalizers
- Audio Test and Measurement Equipment

ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	SO 8-PIN	
SSM2132P	SSM2132S	XIND*

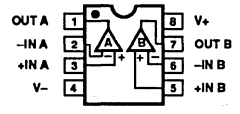
* XIND = –40°C to +85°C

GENERAL DESCRIPTION

The SSM-2132 is a high performance upgrade to the audio industry standard 5532 operational amplifier. All performance parameters have been optimized for high performance professional and consumer audio systems.

Low input noise, high output drive, excellent slew rate and bandwidth, and unity-gain stability are the key attributes of the SSM-2132. A further improvement is a 50 percent reduction in current consumption, resulting in cooler operation. Finally, the SSM-2132 is the only direct replacement to the 5532 that is available in an 8-pin SO package.

PIN CONNECTIONS



8-PIN PLASTIC DIP (P-Suffix)

8-PIN SO (S-Suffix)

This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

PMI

Audio Silicon Specialists™

SSM-2134

LOW NOISE AUDIO OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Very Low Input Noise Voltage..... 3.5nV/ $\sqrt{Hz}$ Typ
- Wide Small-Signal Bandwidth ..... 10MHz Typ
- High Current Drive Capability ($10V_{RMS}$ into 600Ω @ $V_S = \pm 18V$)
- High Slew Rate ..... 13V/μs Typ
- Wide Power Bandwidth ..... 200kHz Typ
- High Open-Loop Gain ..... 200V/mV Typ
- Extended Industrial Temperature Range..... –40°C to +85°C
- Direct Replacement for Industry Standard 5534AN

APPLICATIONS

- High Quality Audio Amplifiers
- Telephone Channel Amplifiers
- Active Filter Designs
- Microphone Preamplifiers
- Audio Line Drivers
- Low-Level Signal Detection
- Servo Control Systems

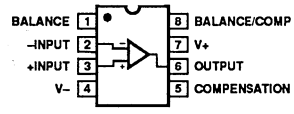
GENERAL DESCRIPTION

The SSM-2134 is a high performance low noise operational amplifier which offers exceptionally low voltage noise of 3.5nV/$\sqrt{Hz}$, outstanding output drive capability, and very high small-signal and power bandwidth. This makes the SSM-2134 an ideal choice for use in high quality and professional audio equipment, instrumentation, and control circuits.

The SSM-2134 is internally compensated for $A_V \geq 3$. However, the frequency response can be optimized with an external compensation capacitor to enable the SSM-2134 to operate at unity-gain or drive large capacitive loads.

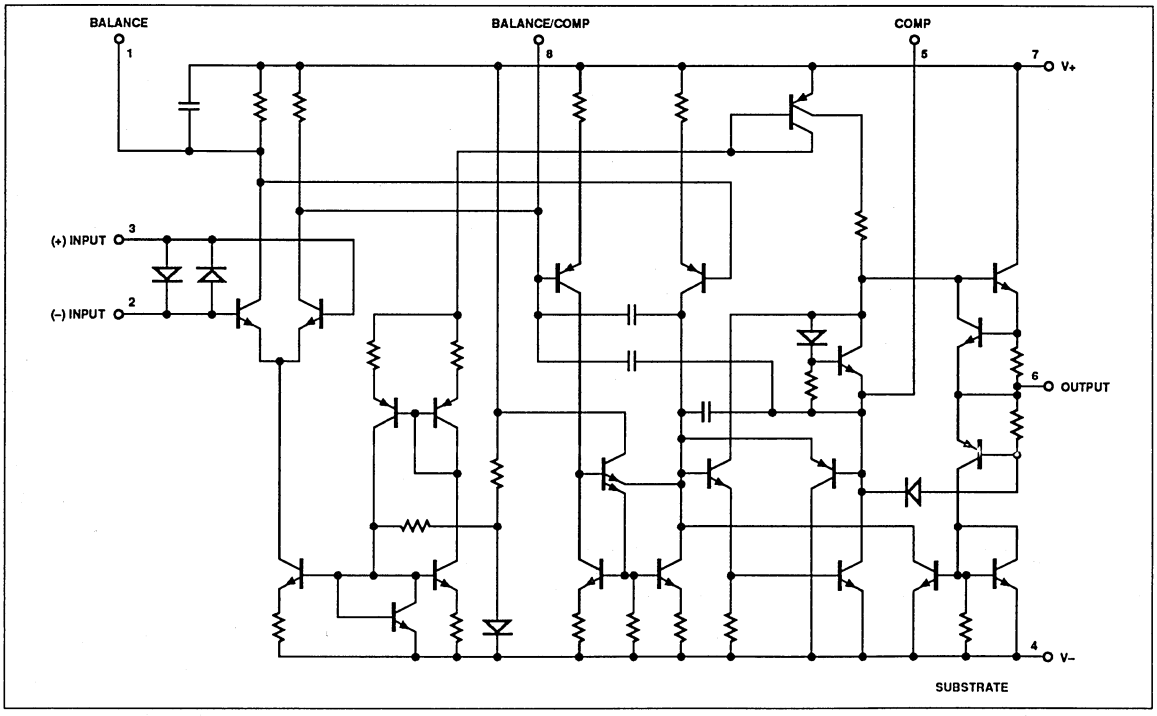
The SSM-2134 is offered in an 8-pin plastic DIP and its performance and characteristics are guaranteed over the extended industrial temperature range of –40°C to +85°C.

PIN CONNECTIONS



8-PIN
PLASTIC DIP
(P-Suffix)

SIMPLIFIED SCHEMATIC



ORDERING INFORMATION

PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
SSM2134P	XIND*

*XIND = –40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage (Note 1) ..... ±0.5V
Input Voltage (Note 2) ..... ±22V
Power Dissipation 300mW
Derate Above +24°C ..... 2.5mW/°C
Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature ..... –60°C to +150°C

NOTES:
1. The SSM-2134's inputs are protected by diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.6V, the input current should be limited to 10mA.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Output maybe shorted to ground at $V_S = \pm15V$, $T_A = +25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$ and $T_A = +25°C$, unless otherwise noted.

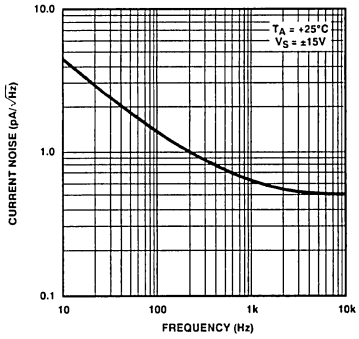
			SSM-2134P			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.3	2	mV
		$-40°C \le T_A \le +85°C$	–	0.4	3	
Input Offset Current	I_{OS}		–	15	300	nA
		$-40°C \le T_A \le +85°C$	–	25	400	
Input Bias Current	I_B		–	350	1500	nA
		$-40°C \le T_A \le +85°C$	–	500	2000	
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 600\Omega$, $V_O = \pm10V$	25	200	–	V/mV
		$R_L \ge 600\Omega$, $V_O = \pm10V$, $-40°C \le T_A \le +85°C$	15	150	–	
Supply Current	I_{SY}	No Load	–	4.5	6.5	mA
Output Voltage Swing	V_O	$V_S = \pm15V$, $R_L \ge 600\Omega$	±12	±13	–	V
		$V_S = \pm18V$, $R_L \ge 600\Omega$	±15	±16	–	
Output Short-Circuit Current	I_{SC}	(Note 1)	–	60	–	mA
Input Resistance-Differential-Mode	R_{IN}	(Note 2)	30	100	–	kΩ
Input Voltage Range	IVR		±12	±13	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm12V$	70	114	–	dB
Power Supply Rejection Ratio	PSRR		–	6	100	µV/V
Rise Time	t_r	$R_L \ge 600\Omega$, $C_C = 22pF$	–	20	–	ns
Overshoot	OS	$C_L = 100pF$	–	20	–	%
AC Gain		$C_C = 0$, $f_O = 10kHz$	–	6	–	V/mV
		$C_C = 22pF$, $f_O = 10kHz$	–	2.2	–	
Unity-Gain Bandwidth	GBW	$C_C = 22pF$, $C_L = 100$ p F	–	10	–	MHz
Slew Rate	SR	$C_C = 0$	–	13	–	V/µs
		$C_C = 22pF$	–	6	–	
Full Power Bandwidth	BW_P	$V_O = \pm10V$, $C_C = 22pF$	–	95	–	kHz
		$C_C = 0$	–	200	–	
Input Noise Voltage Density	e_n	$f_O = 30Hz$	–	5.5	7.0	$nV/\sqrt{Hz}$
		$f_O = 1kHz$	–	3.5	4.5	
Input Noise Current Density	i_n	$f_O = 30Hz$	–	2.5	–	$pA/\sqrt{Hz}$
		$f_O = 1kHz$	–	0.6	–	
Broadband Noise Figure	F_N	$R_S = 5k\Omega$, f = 10Hz to 20kHz	–	0.7	–	dB
Total Harmonic Distortion	THD	$V_{IN} = 3V_{RMS}$, $A_V = +1000$, $R_L = 2k\Omega$	–	0.025	–	%

NOTES:
1. Output may be shorted to ground at $V_S = \pm15V$, $T_A = +25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.
2. Guaranteed by design.

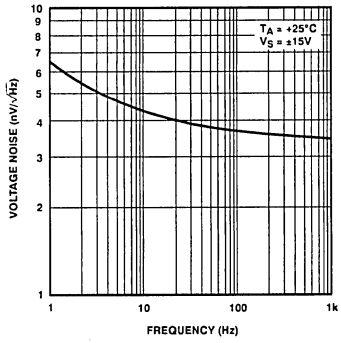
Specifications subject to change, Consult latest data sheet.

TYPICAL PERFORMANCE CHARACTERISTICS

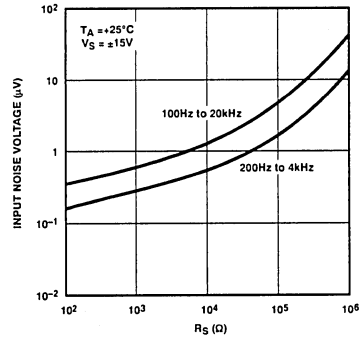
CURRENT NOISE DENSITY vs FREQUENCY



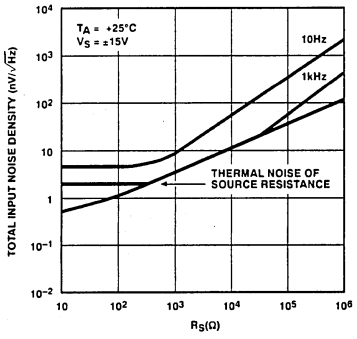
VOLTAGE NOISE DENSITY vs FREQUENCY



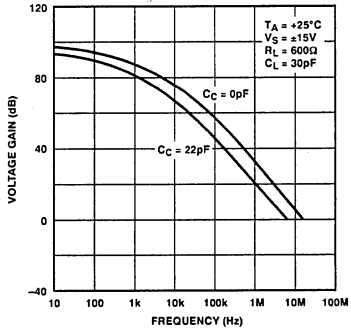
BROADBAND INPUT NOISE VOLTAGE



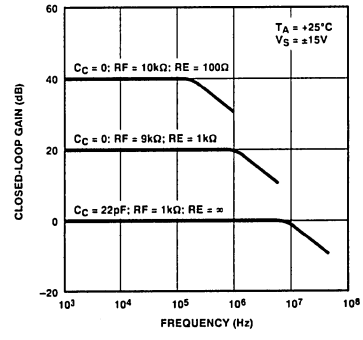
TOTAL INPUT NOISE DENSITY



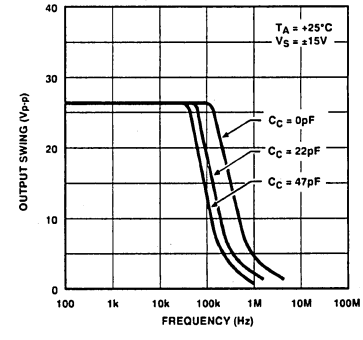
OPEN-LOOP GAIN vs FREQUENCY



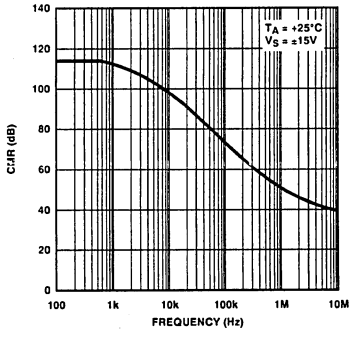
CLOSED-LOOP GAIN vs FREQUENCY



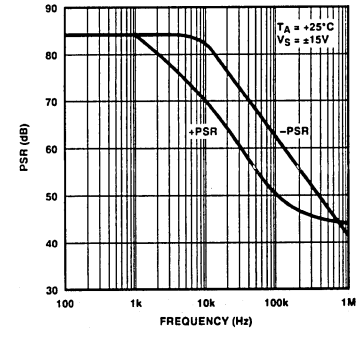
OUTPUT VOLTAGE SWING vs FREQUENCY



CMR vs FREQUENCY

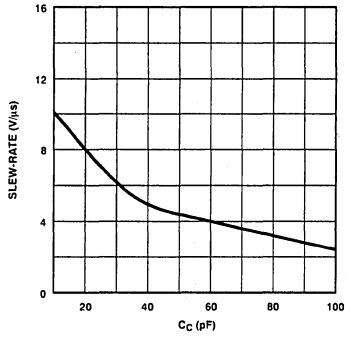


PSR vs FREQUENCY

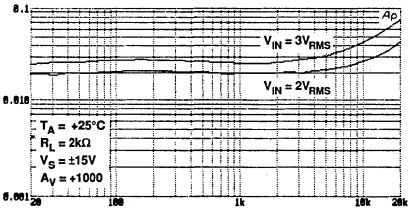


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

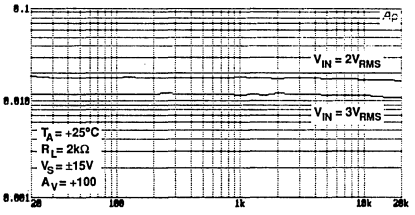
SLEW RATE vs COMPENSATION CAPACITOR



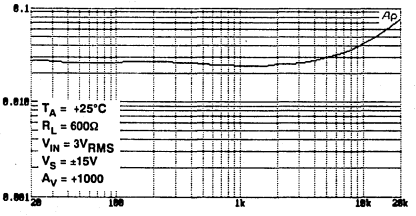
TOTAL HARMONIC DISTORTION vs FREQUENCY



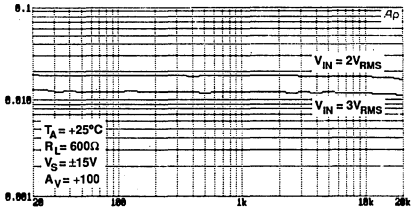
TOTAL HARMONIC DISTORTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

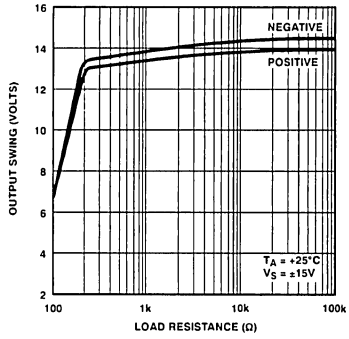


TOTAL HARMONIC DISTORTION vs FREQUENCY

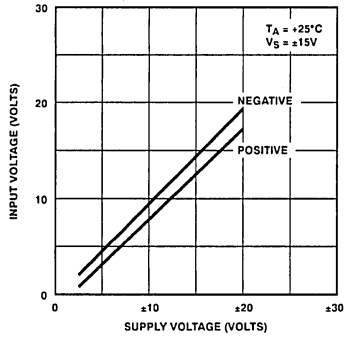


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

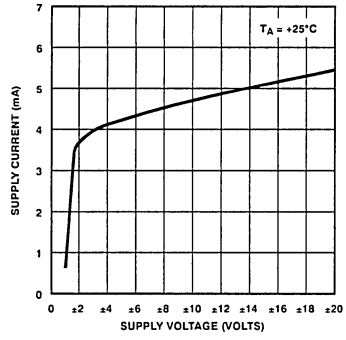
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



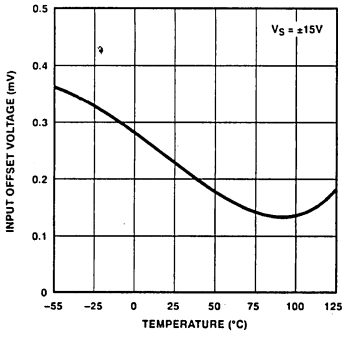
INPUT COMMON-MODE VOLTAGE vs SUPPLY VOLTAGE



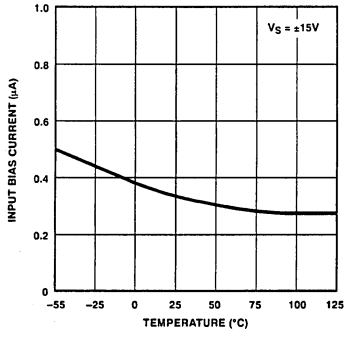
SUPPLY CURRENT vs SUPPLY VOLTAGE



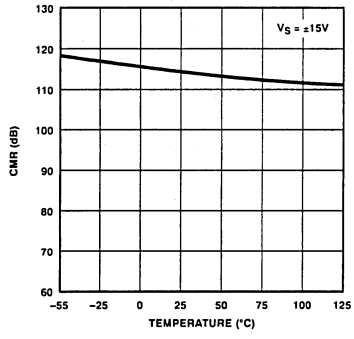
INPUT OFFSET VOLTAGE vs TEMPERATURE



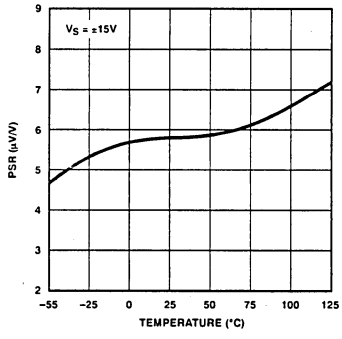
INPUT BIAS CURRENT vs TEMPERATURE



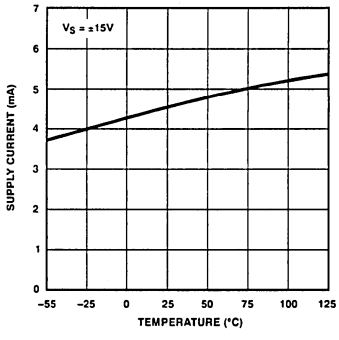
CMR vs TEMPERATURE



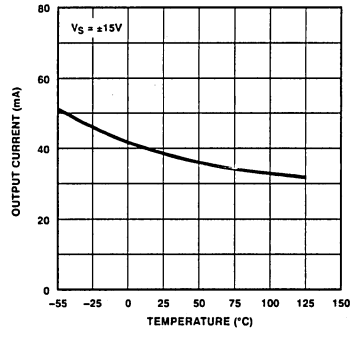
PSR vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE

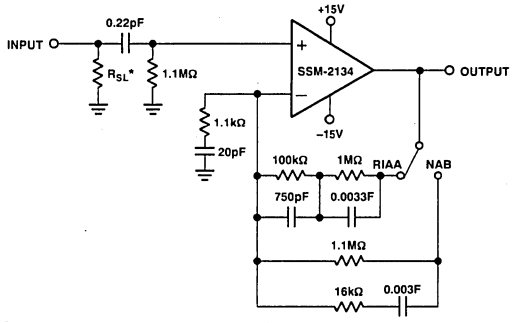


SHORT-CIRCUIT CURRENT vs TEMPERATURE

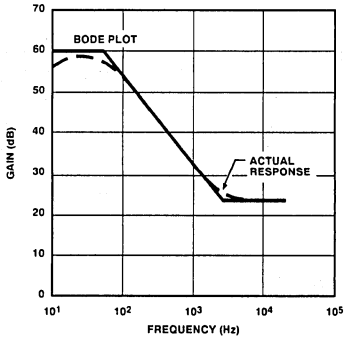


APPLICATIONS INFORMATION

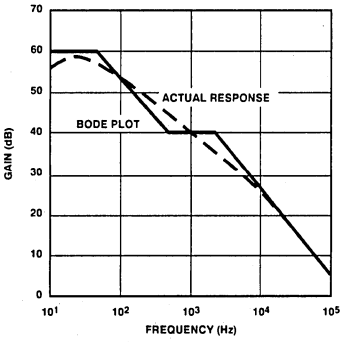
PREAMPLIFIER-RIAA/NAB COMPENSATION



*SELECT TO PROVIDE SPECIFIED TRANSDUCER LOADING
OUTPUT NOISE 0.8mV$_{RMS}$ (WITH INPUT SHORTED)



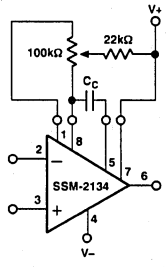
BODE PLOT OF RIAA EQUALIZATION AND THE RESPONSE REALIZED IN AN ACTUAL CIRCUIT USING THE SSM-2134



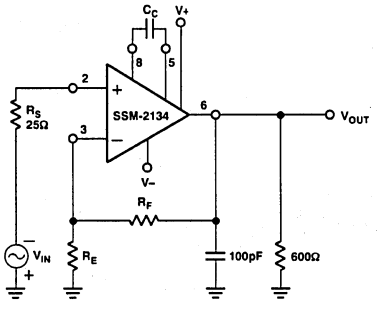
BODE PLOT OF NAB EQUALIZATION AND THE RESPONSE REALIZED IN THE ACTUAL CIRCUIT USING THE SSM-2134

TEST CIRCUIT

FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT



CLOSED-LOOP FREQUENCY RESPONSE



PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

SSM-2139

DUAL, LOW NOISE, HIGH-SPEED AUDIO OPERATIONAL AMPLIFIER ($A_{VCL} \geq 3$)

FEATURES

- Ultra-Low Voltage Noise ..... 3.2nV/√Hz
- High Slew Rate 11V/µs
- Excellent Gain Bandwidth Product 30MHz
- Low Supply Current (Both Amplifiers) 4mA
- Low Offset Voltage 500µV
- High Gain 1,700V/mV
- Compensated for Minimum Gain of 3
- Low Cost
- Industry Standard 8-Pin Plastic Dual Pinout

APPLICATIONS

- Microphone Preamplifiers
- Audio Line Drivers
- Active Filters
- Phono and Tape Head Preamplifiers
- Equalizers

ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	16-PIN SOL	
SSM2139P	SSM2139S	XIND*

* XIND = –40°C to +85°C

For availability on SOL package, contact your local sales office.

GENERAL DESCRIPTION

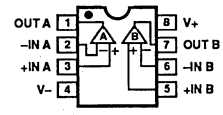
The SSM-2139 is a low noise, high-speed dual audio operational amplifier which has been internally compensated for gains equal to, or greater than three.

This monolithic bipolar op amp offers exceptional voltage noise performance of 3.2nV/√Hz (typical) with a guaranteed specification of only 5nV/√Hz MAX @ 1kHz.

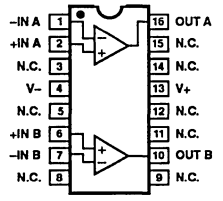
The high slew rate of 11V/µs and the gain-bandwidth product of 30MHz is achieved without compromising the power consumption of the device. The SSM-2139 draws only 4mA of supply current for both amplifiers.

Continued

PIN CONNECTIONS

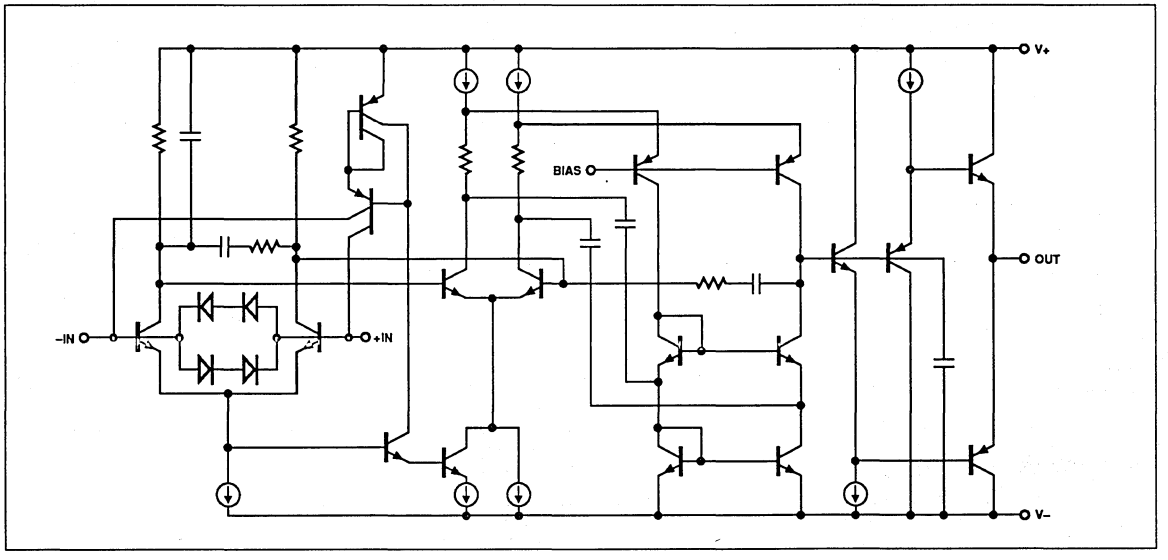


8-PIN
PLASTIC MINI-DIP
(P-Suffix)



16-PIN SOL
(S-Suffix)

SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



These characteristics make the SSM-2139 an ideal choice for use in high quality professional audio equipment, instrumentation, and control circuit applications.

The low offset voltage V_{OS} of 500μV MAX (20μV typical) and offset voltage drift of only 2.5μV/°C MAX assures system accuracy and eliminates the need for external V_{OS} adjustments.

The SSM-2139's outstanding open-loop gain of 1,700,000 and its exceptional gain linearity eliminate incorrectable system nonlinearities and provides superior performance in high closed-loop gain applications, such as preamplifiers.

The SSM-2139 is offered in an 8-pin plastic DIP and Small Outline (SO) package and its performance and characteristics are guaranteed over the extended industrial temperature range of –40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range ..... –65°C to +150C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
SSM-2139 (P, S) ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	96	37	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.
2. The SSM-2139 inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2139 MIN	TYP	MAX	UNITS
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	–	80	200	nV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	–	3.6	6.5	nV/√Hz
		f_O = 100Hz	–	3.2	5.5	
		f_O = 1kHz (Note 2)	–	3.2	5.0	
Input Noise Current Density	i_n	f_O = 10Hz	–	1.1	–	pA/√Hz
		f_O = 100Hz	–	0.7	–	
		f_O = 1kHz	–	0.6	–	
Slew Rate	SR		7	11	–	V/μs
Gain Bandwidth Product	GBW	f_O = 100kHz	–	30	–	MHz
Full Power Bandwidth	BWp	$V_O = 27V_{p-p}$, R_L = 2kΩ (Note 3)	–	130	–	kHz
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4	6.5	mA
Total Harmonic Distortion	THD	R_L = 2kΩ, $V_O = 3V_{RMS}$, f_O = 1kHz	–	0.002	–	%
Input Offset Voltage	V_{OS}		–	20	500	μV
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1	50	nA
Input Bias Current	I_B	V_{CM} = 0V	–	5	80	nA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V, R_L = 10kΩ	1000	1700	–	V/mV
		R_L = 2kΩ	500	900	–	
		R_L = 600Ω	–	900	–	
Output Voltage Swing	V_O	$R_L \geq$ 2kΩ	±12	±13.5	–	V
	V_O+	$R_L \geq$ 600Ω	–	+13	–	
	V_O–	$R_L \geq$ 600Ω	–	–10	–	
Common-Mode Rejection	CMR	V_{CM} = ±12V	94	115	–	dB

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SSM-2139 MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	105	120	–	dB
Input Voltage Range	IVR	(Note 4)	±12.0	±12.5	–	V
Output Short-Circuit Current	I_{SC}	Sink Source	– –	20 40	– –	mA
Input Resistance Common-Mode	R_{INCM}		–	20	–	GΩ
Input Resistance Differential-Mode	R_{IN}		–	0.4	–	MΩ
Input Capacitance	C_{IN}		–	3	–	pF
Channel Separation	CS	V_O = 20V_{p-p} f_O = 10Hz (Note 1)	125	175	–	dB

NOTES:
1. Guaranteed but not 100% tested.
2. Sample tested.
3. $BW_p = SR/2\pi V_{PEAK}$.
4. Guaranteed by CMR test.

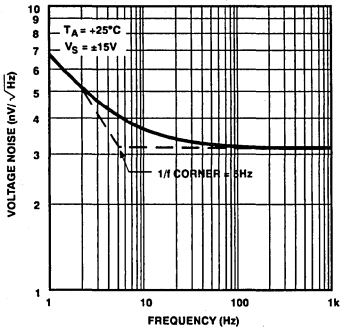
ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ 85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2139 MIN	TYP	MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.4	7.2	mA
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13	–	V
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10kΩ R_L = 2kΩ	500 250	1400 700	– –	V/mV
Input Offset Voltage	V_{OS}		–	45	700	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.4	2.5	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1.5	60	nA
Input Bias Current	I_B	V_{CM} = 0V	–	6	90	nA
Common-Mode Rejection	CMR	V_{CM} = ±12V	94	115	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 to ±18V	100	115	–	dB
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	V

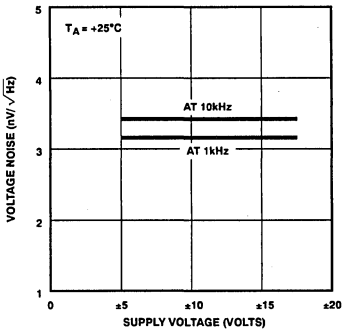
NOTES:
1. Guaranteed by CMR test.

TYPICAL PERFORMANCE CHARACTERISTICS

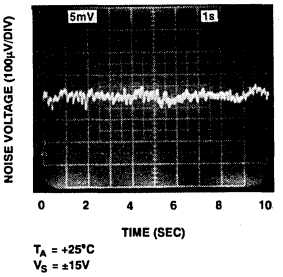
VOLTAGE NOISE DENSITY vs FREQUENCY



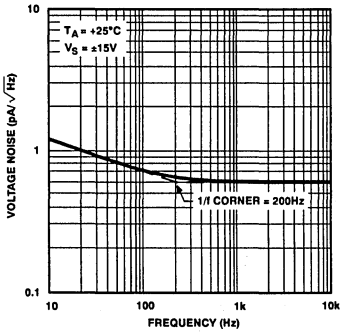
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



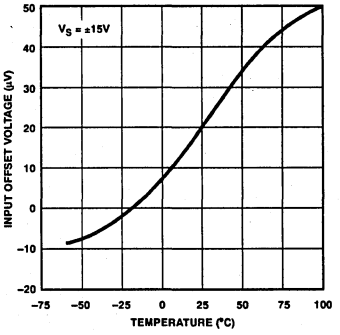
0.1Hz TO 10Hz NOISE



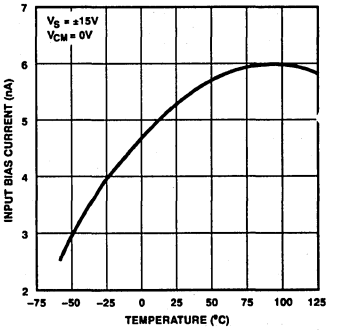
CURRENT NOISE DENSITY vs FREQUENCY



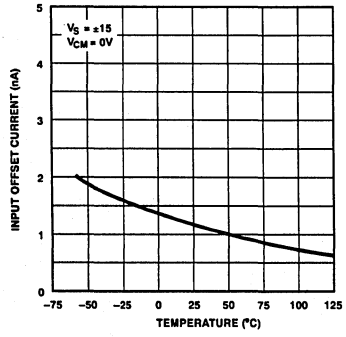
INPUT OFFSET VOLTAGE vs TEMPERATURE



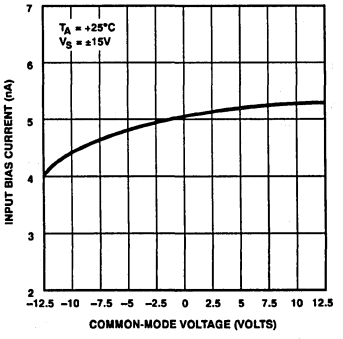
INPUT BIAS CURRENT vs TEMPERATURE



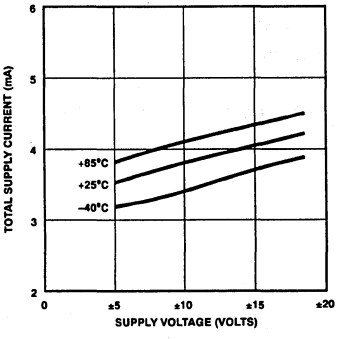
INPUT OFFSET CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

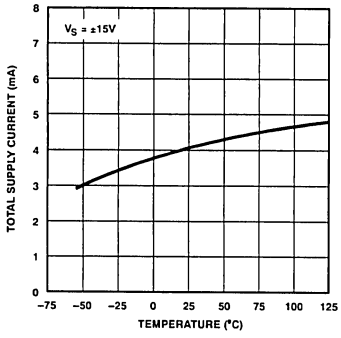


TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE

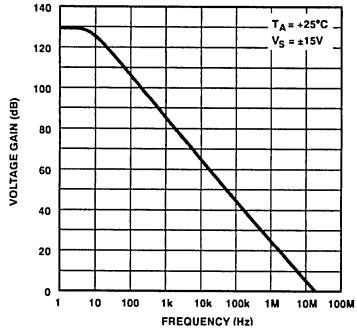


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

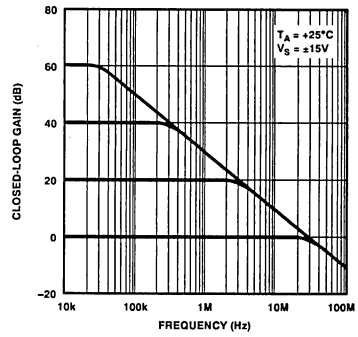
TOTAL SUPPLY CURRENT vs TEMPERATURE



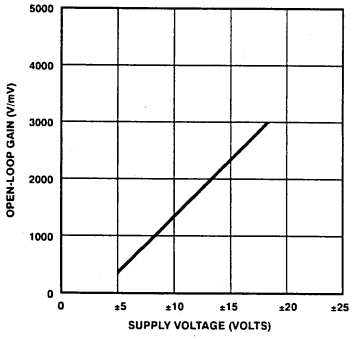
OPEN-LOOP GAIN vs FREQENCY



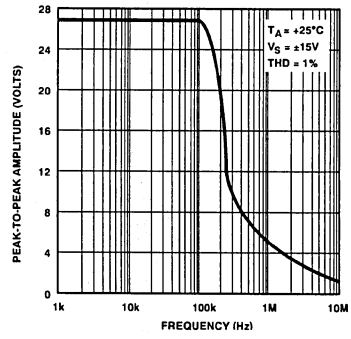
CLOSED-LOOP GAIN vs FREQUENCY



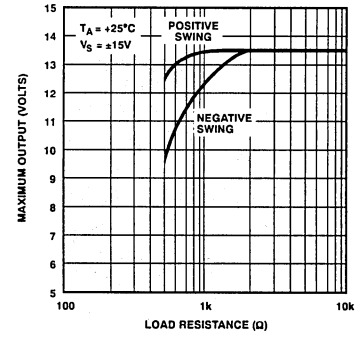
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



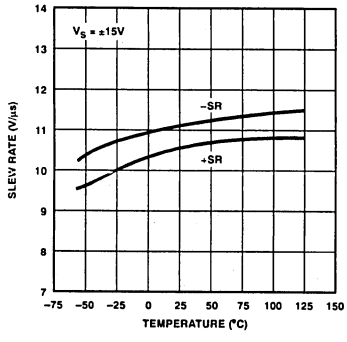
MAXIMUM OUTPUT SWING vs FREQUENCY



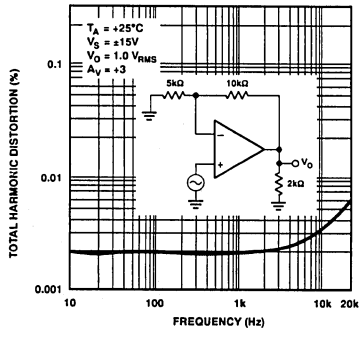
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



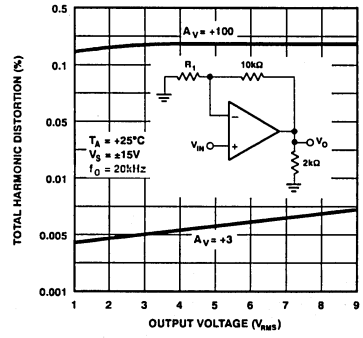
SLEW RATE vs TEMPERATURE



TOTAL HARMONIC DISTORTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE



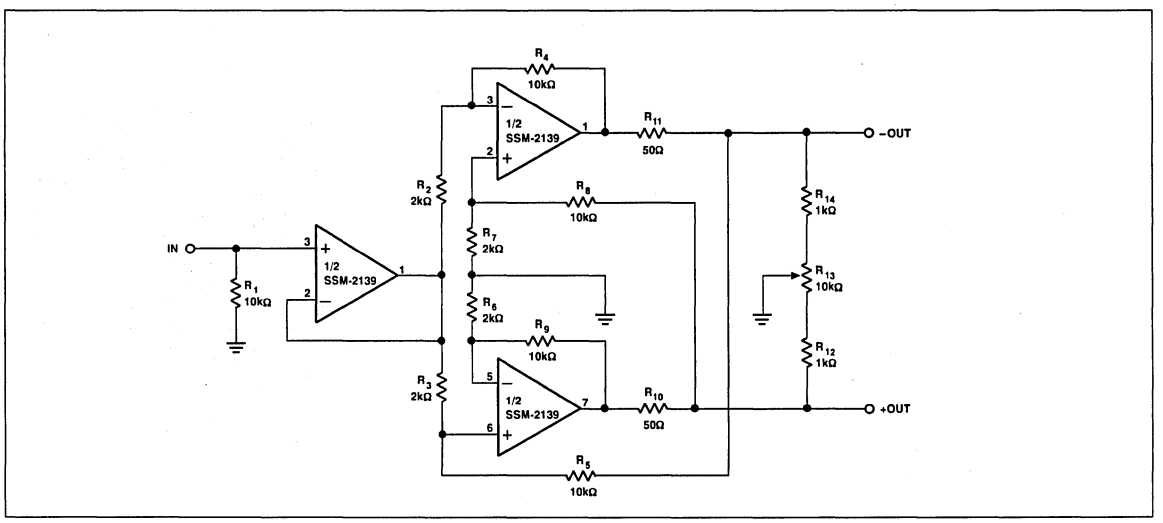


FIGURE 1: *High-Speed Differential Line Driver*

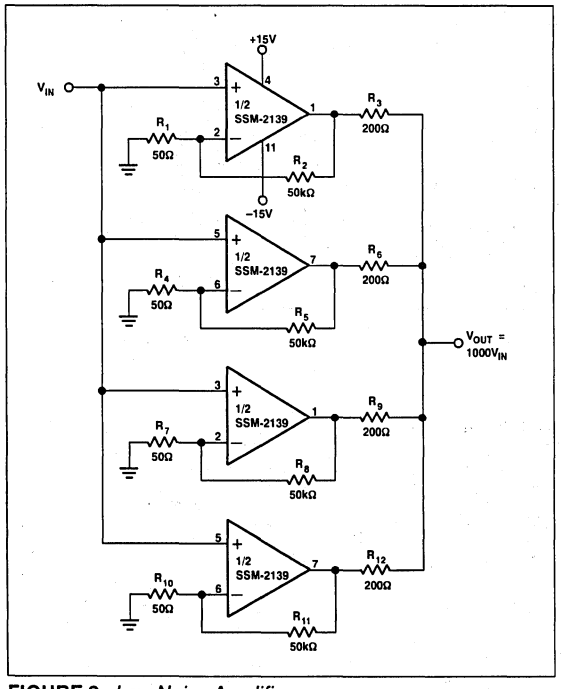


FIGURE 2: *Low Noise Amplifier*

APPLICATIONS INFORMATION

HIGH-SPEED DIFFERENTIAL LINE DRIVER

The circuit of Figure 1 is a unique approach to a line driver circuit widely used in professional audio applications. With ±18V supplies, the line driver can deliver a differential signal of 30Vp-p into a 1.5kΩ load. The output of the differential line driver looks exactly like a transformer. Either output can be shorted to ground without changing the circuit gain of 5, so the amplifier can easily be set for inverting, noninverting, or differential operation. The line driver can drive unbalanced loads, like a true transformer.

LOW NOISE AMPLIFIER

A simple method of reducing amplifier noise is by paralleling amplifiers as shown in Figure 2. Amplifier noise, depicted in Figure 3, is around $2nV/\sqrt{Hz}$ @ 1kHz (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 1000. The 200Ω resistors limit circulating currents and provide an effective output resistance of 50Ω.

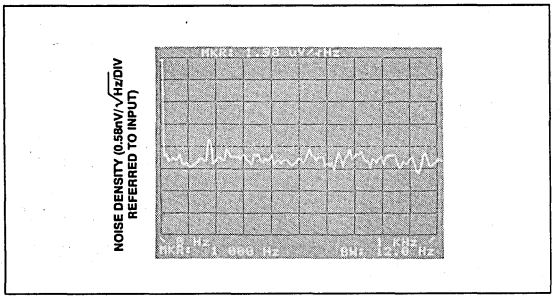


FIGURE 3: *Noise Density of Low Noise Amplifier, G = 1000*

VOLTAGE AND CURRENT NOISE

The SSM-2139 is a low noise, high-speed dual op amp, exhibiting a typical voltage noise of only 3.2nV/$\sqrt{Hz}$ @ 1kHz. The exceptionally low noise characteristics of the SSM-2139 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the SSM-2139 is gained at the expense of current noise performance, which is normal for low noise amplifiers.

To obtain the best noise performance in a circuit, it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calculated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 = (e_t)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_t = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 4 shows the relationship between total noise at 1kHz and source resistance. For R_S < 1kΩ, the total noise is dominated by the voltage noise of the SSM-2139. As R_S rises above 1kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the SSM-2139. When R_S exceeds 20kΩ, current noise of the SSM-2139 becomes the major contributor to total noise.

Figure 5 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 4 because current noise is inversely proportional to the square root of frequency. In Figure 5, current noise of the SSM-2139 dominates the total noise when R_S > 5kΩ.

From Figures 4 and 5, it can be seen that to reduce total noise, source resistance must be kept to a minimum.

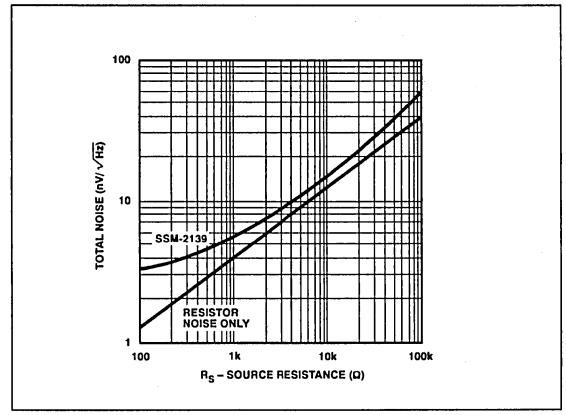


FIGURE 4: *Total Noise vs. Source Resistance (Including Resistor Noise) at 1kHz*

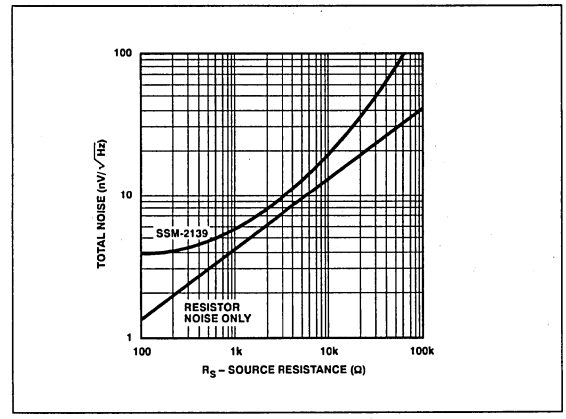


FIGURE 5: *Total Noise vs. Source Resistance (Including Resistor Noise) at 10Hz*

Figure 6 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S, the voltage noise of the SSM-2139 is the major contributor to peak-to-peak noise with current noise the major contributor as R_S increases.

For reference, typical source resistances of some signal sources are listed in Table 1.

For further information regarding noise calculations, see "Minimization of Noise in Op Amp Applications," Application Note AN-15.

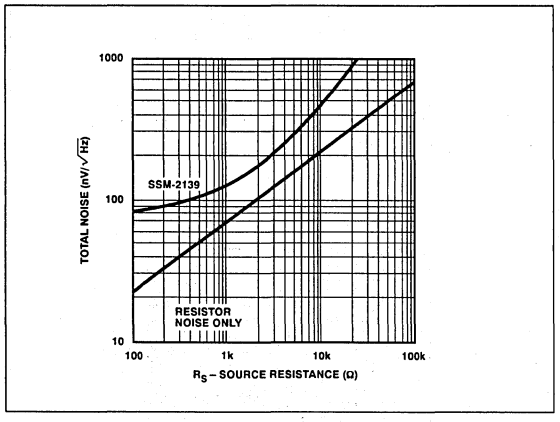


FIGURE 6: *Peak-to-Peak Noise (0.1Hz to 10Hz) vs. Source Resistance (Includes Resistor Noise)*

TABLE 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain Gauge	<500Ω	Typically used in low-frequency applications.
Magnetic Tapehead, Microphone	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. SSM-2139 I_B can be neglected.
Magnetic Phonograph Cartridge	<1500Ω	Similar need for low I_B in direct coupled applications. SSM-2139 will not introduce any self-magnetization problem.
Linear Variable Differential Transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

NOISE MEASUREMENTS – PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 7 is a test setup for measuring peak-to-peak voltage noise. To measure the 200nV peak-to-peak noise specification of the SSM-2139 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 2μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.

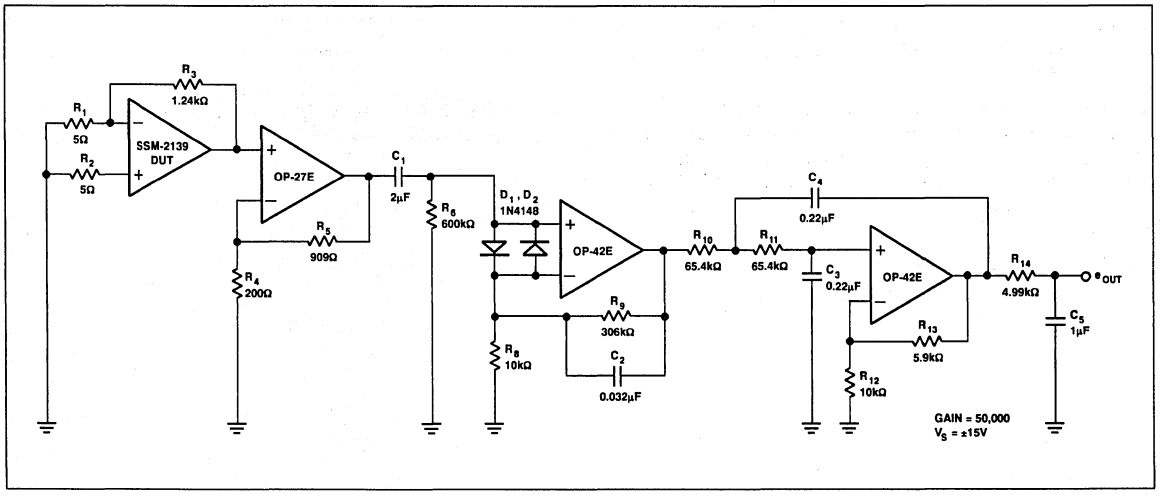


FIGURE 7: *Peak-to-Peak Voltage Noise Test Circuit (0.1Hz to 10Hz)*

3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
4. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 8, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts as a additional pole to eliminate noise contribution from the frequency band below 0.1Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimze output noise introduced via the amplifier supply pins.

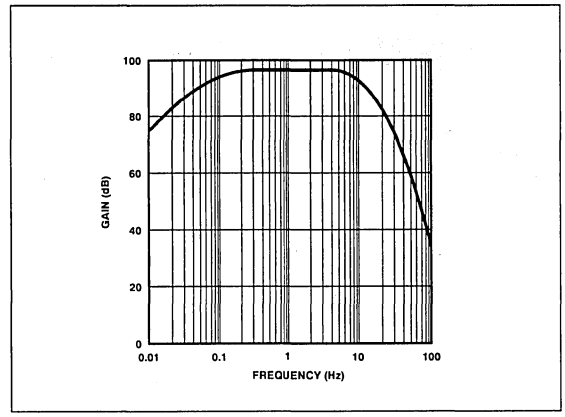
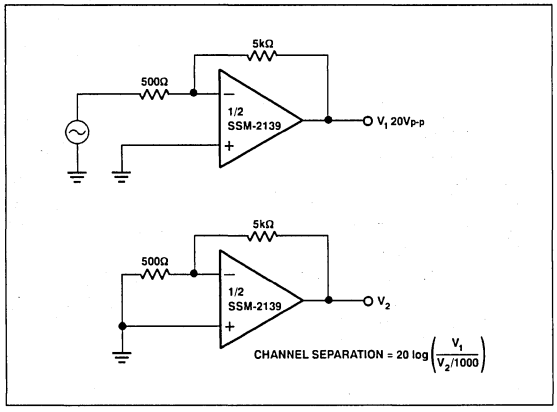


FIGURE 8: *0.1Hz to 10Hz Peak-to-Peak Voltage Noise Test Circuit Frequency Response*

CHANNEL SEPARATION TEST CIRCUIT



PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

SSM-2210

AUDIO DUAL MATCHED NPN TRANSISTOR

FEATURES

- **Very Low Voltage Noise ..... @ 100Hz, 1nV/√Hz MAX**
- **Excellent Current Gain Match ..... 0.5% TYP**
- **Tight V_{BE} Match (V_{OS}) ..... 200μV MAX**
- **Outstanding Offset Voltage Drift ..... 0.03μV/°C TYP**
- **High Gain-Bandwidth Product ..... 200MHz TYP**
- **Low Cost**
- **Direct Replacement For LM394BN/CN**

ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	SO 8-PIN	
SSM2210P	SSM2210S†	XIND*

* XIND = –40°C to +85°C

† For availability on SO package, contact your local sales office.

GENERAL DESCRIPTION

The SSM-2210 is a dual NPN matched transistor pair specifically designed to meet the requirements of ultra-low noise audio systems.

With its extremely low input base spreading resistance (rbb' is typically 28Ω), and high current gain (h_{FE} typically exceeds 600 @ I_C = 1mA), systems implementing the SSM-2210 can achieve outstanding signal-to-noise ratios. This will result in superior performance compared to systems incorporating commercially available monolithic amplifiers.

The equivalent input voltage noise of the SSM-2210 is typically only 0.8nV/√Hz over the entire audio bandwidth of 20Hz to 20KHz.

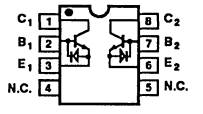
Excellent matching of the current gain (Δh_{FE}) to about 0.5% and low V_{OS} of less than 50μV (typical) make it ideal for symmetrically balanced designs which reduce high order amplifier harmonic distortion.

Stability of the matching parameters is guaranteed by protection diodes across the base-emitter junction. These diodes prevent degradation of Beta and matching characteristics due to reverse biasing of the base-emitter junction.

The SSM-2210 is also an ideal choice for accurate and reliable current biasing and mirroring circuits. Furthermore, since a current mirror's accuracy degrades exponentially with mismatches of V_{BE}'s between transistor pairs, the low V_{OS} of the SSM-2210 will preclude offset trimming in most circuit applications.

The SSM-2210 is offered in an 8-pin epoxy DIP and 8-pin SO, its performance and characteristics are guaranteed over the extended industrial temperature range of –40°C to +85°C.

PIN CONNECTIONS



8-PIN PLASTIC DIP (P-Suffix)

8-PIN SO (S-Suffix)

ABSOLUTE MAXIMUM RATINGS

Collector Current (I_C) 20mA
Emitter Current (I_E) 20mA
Collector-Collector Voltage (BV_{CC}) 40V
Collector-Base Voltage (BV_{CBO}) 40V
Collector-Emitter Voltage (BV_{CEO}) 40V
Emitter-Emitter Voltage (BV_{EE}) 40V
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature ..... –65°C to +125°C
Junction Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	110	50	°C/W
8-Pin SO (S)	160	44	°C/W

NOTE:

1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO packages.

ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2210 MIN	SSM-2210 TYP	SSM-2210 MAX	UNITS
Current Gain	h_{FE}	I_C = 1mA (Note 1) I_C = 10μA	300 200	605 550	– –	
Current Gain Match	Δh_{FE}	10μA ≤ I_C ≤ 1mA (Note 2)	–	0.5	5	%
Noise Voltage Density	e_n	I_C = 1mA, V_{CB} = 0 (Note 3) f_o = 10Hz f_o = 100Hz f_o = 1kHz f_o = 10kHz	 – – – –	 1.6 0.9 0.85 0.85	 2 1 1 1	nV/√Hz
Offset Voltage	V_{OS}	V_{CB} = 0 I_C = 1mA	–	10	200	μV
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ V_{MAX} (Note 4) 1μA ≤ I_C ≤ 1mA (Note 5)	–	10	50	μV
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0V 1μA ≤ I_C ≤ 1mA (Note 5)	–	5	70	μV
Breakdown Voltage	BV_{CEO}		40	–	–	V
Gain-Bandwidth Product	f_T	I_C = 10mA, V_{CE} = 10V	–	200	–	MHz
Collector-Base Leakage Current	I_{CBO}	V_{CB} = V_{MAX}	–	25	500	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = V_{MAX} (Notes 6, 7)	–	35	500	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = V_{MAX} (Notes 6, 7) V_{BE} = 0	–	35	500	pA
Input Bias Current	I_B	I_C = 10μA	–	–	50	nA
Input Offset Current	I_{OS}	I_C = 10μA	–	–	6.2	nA
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA I_B = 100μA	–	0.05	0.2	V
Output Capacitance	C_{OB}	V_{CB} = 15V, I_E = 0	–	23	–	pF
Bulk Resistance	r_{BE}	10μA ≤ I_C ≤ 10mA (Note 6)	–	0.3	1.6	Ω
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	–	35	–	pF

NOTES:

1. Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector currents.
2. Current Gain Match (Δh_{FE}) is defined as:

$$\Delta h_{FE} = \frac{100(\Delta I_B)(h_{FE}min)}{I_C}$$

3. Noise Voltage Density is guaranteed, but not 100% tested.
4. This is the maximum change in V_{OS} as V_{CB} is swept from 0V to 40V.
5. Measured at I_C = 10μA and guaranteed by design over the specified range of I_C.
6. Guaranteed by design.
7. I_{CC} and I_{CES} are verified by measurement of I_{CBO}.

ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

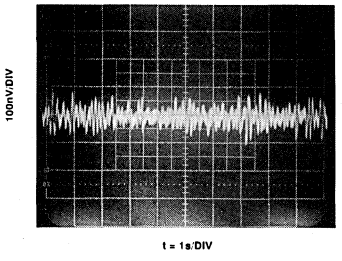
PARAMETER	SYMBOL	CONDITIONS	SSM-2210 MIN	TYP	MAX	UNITS
Current Gain	h_{FE}	I_C = 1mA (Note 1) I_C = 10µA	300 200	– –	– –	
Offset Voltage	V_{OS}	V_{CB} = 0 I_C = 1mA	–	–	220	µV
Average Offset Voltage Drift	TCV_{OS}	10µA ≤ I_C ≤ 1mA, 0 ≤ V_{CB} ≤ V_{MAX} (Note 2) V_{OS} Trimmed to Zero (Note 3)	– –	0.08 0.03	1 0.3	µV/°C
Input Bias Current	I_B	I_C = 10µA	–	–	50	nA
Input Offset Current	I_{OS}	I_C = 10µA	–	–	13	nA
Input Offset Current Drift	TCI_{OS}	I_C = 10µA (Note 4)	–	40	150	pA/°C
Collector-Base Leakage Current	I_{CBO}	V_{CB} = V_{MAX}	–	3	–	nA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = V_{MAX}, V_{BE} = 0	–	4	–	nA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = V_{MAX}	–	4	–	nA

NOTES:

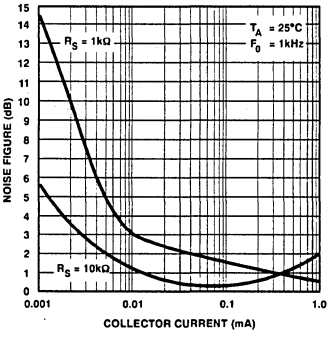
1. Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector current.
2. Guaranteed by V_{OS} test ($TCV_{OS} \approx \frac{V_{OS}}{T} \propto V_{BE}$), T = 298K for T_A = 25°C.
3. The initial zero offset voltage is established by adjusting the ratio of I_{C1} to I_{C2} at T_A = 25°C. This ratio must be held to 0.003% over the entire temperature range. Measurements are taken at the temperature extremes and 25°C.
4. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

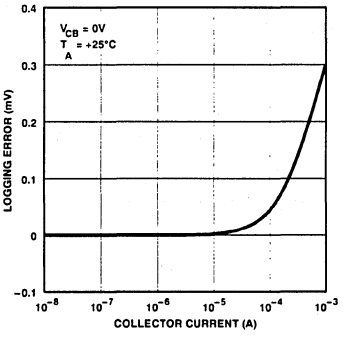
LOW FREQUENCY NOISE (0.1 Hz TO 10 Hz)



NOISE FIGURE vs COLLECTOR CURRENT

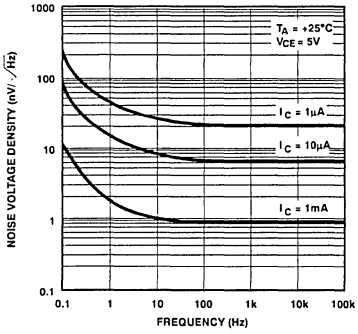


EMITTER-BASE LOG CONFORMITY

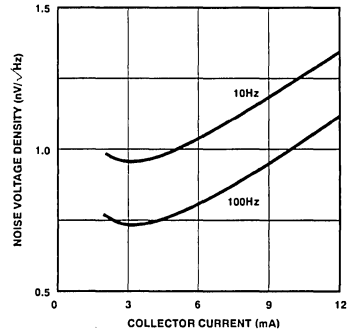


TYPICAL PERFORMANCE CHARACTERISTICS

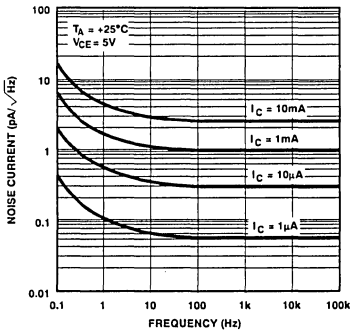
NOISE VOLTAGE DENSITY vs FREQUENCY



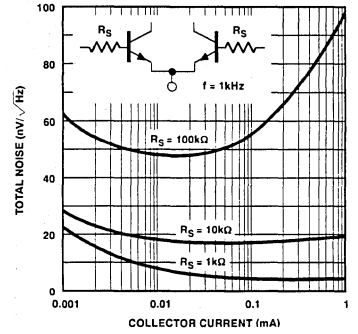
NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT



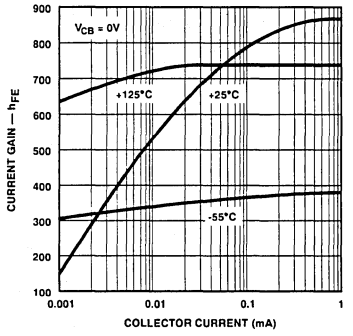
NOISE CURRENT DENSITY vs FREQUENCY



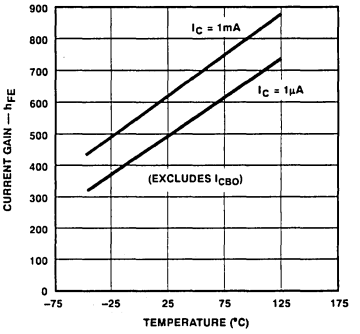
TOTAL NOISE vs COLLECTOR CURRENT



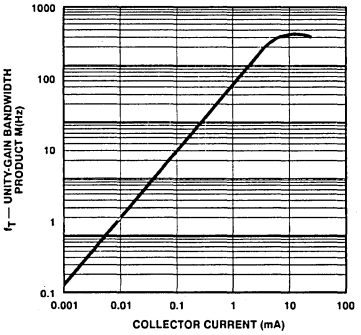
CURRENT GAIN vs COLLECTOR CURRENT



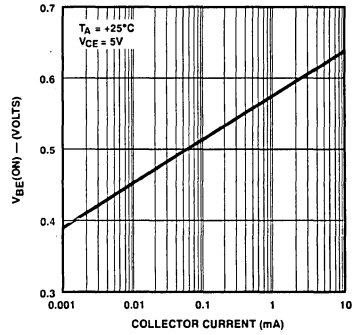
CURRENT GAIN vs TEMPERATURE



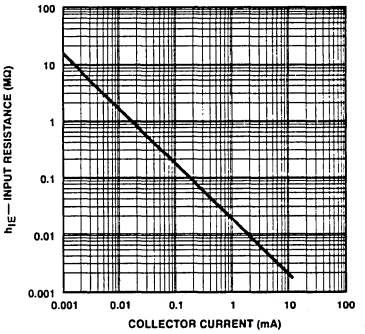
GAIN BANDWIDTH vs COLLECTOR CURRENT



BASE-EMITTER-ON-VOLTAGE vs COLLECTOR CURRENT

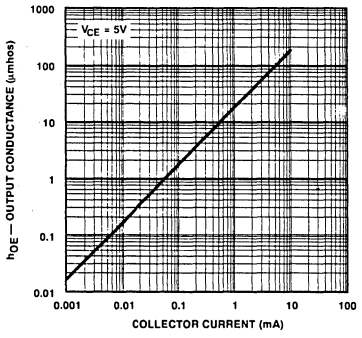


SMALL-SIGNAL INPUT RESISTANCE vs COLLECTOR CURRENT

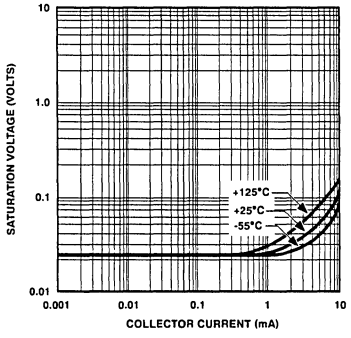


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

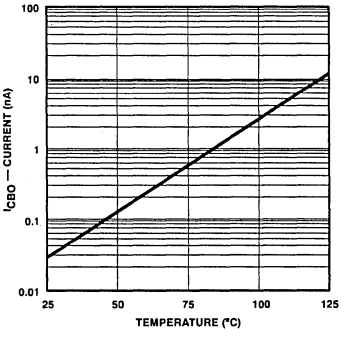
SMALL-SIGNAL OUTPUT CONDUCTANCE vs COLLECTOR CURRENT



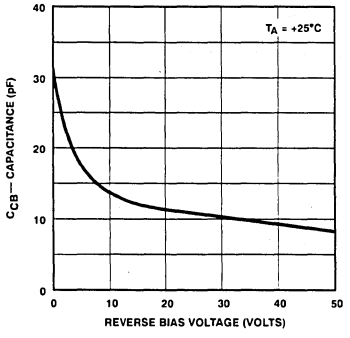
SATURATION VOLTAGE vs COLLECTOR CURRENT



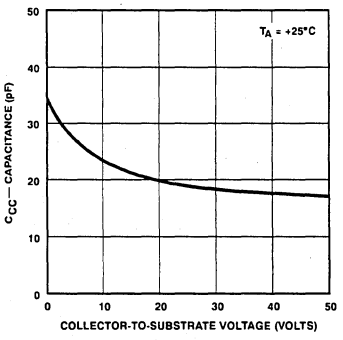
COLLECTOR-TO-BASE LEAKAGE vs TEMPERATURE



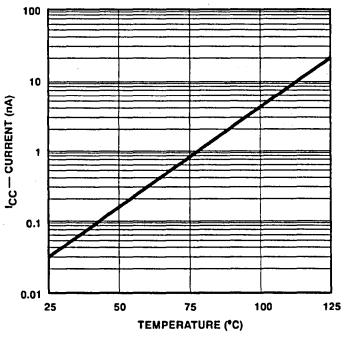
COLLECTOR-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE



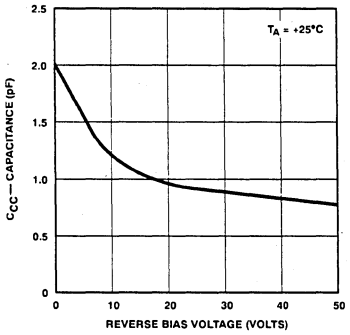
COLLECTOR-TO-COLLECTOR CAPACITANCE vs COLLECTOR-TO-SUBSTRATE VOLTAGE



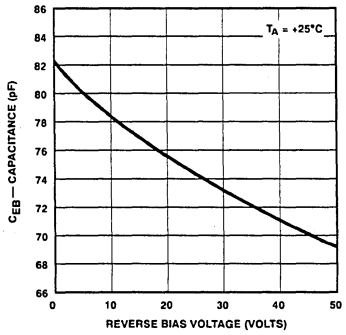
COLLECTOR-TO-COLLECTOR LEAKAGE vs TEMPERATURE



COLLECTOR-TO-COLLECTOR CAPACITANCE vs REVERSE BIAS VOLTAGE



EMITTER-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE



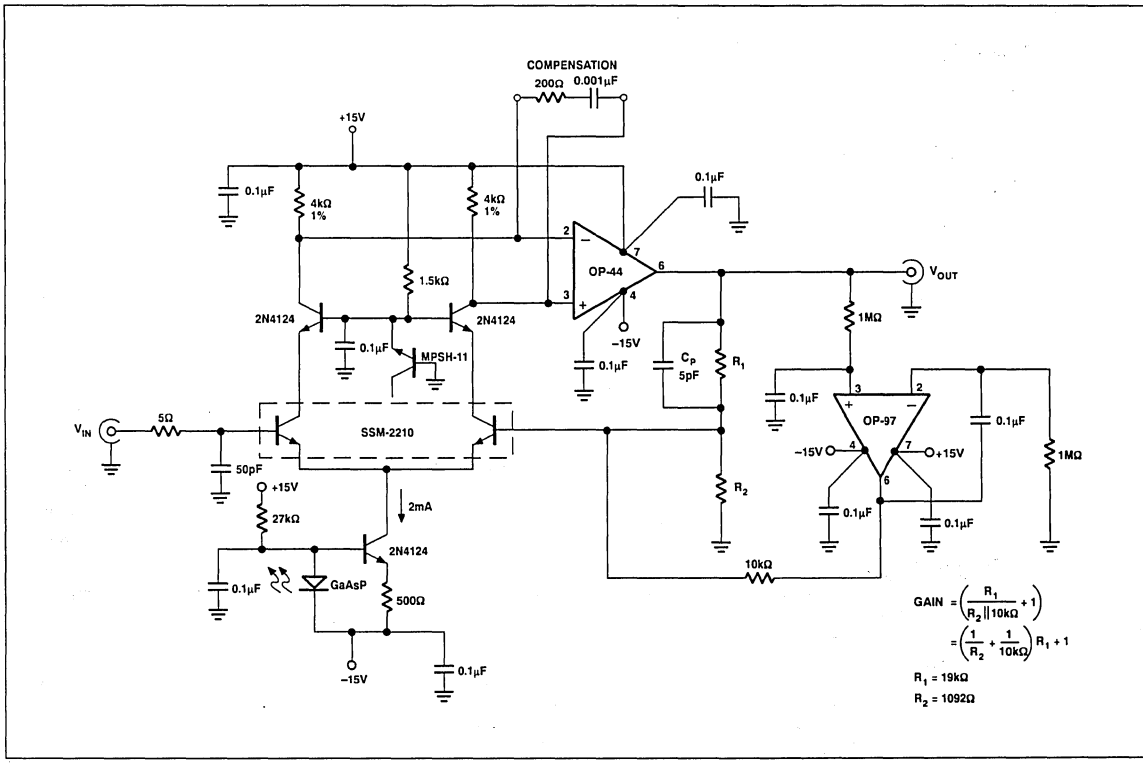


FIGURE 1: *A Low-Noise Wideband Amplifier*

A VERY LOW-NOISE, WIDEBAND AMPLIFIER

Figure 1 illustrates a low-noise, wide-band amplifier consisting of a high slew rate JFET amplifier, the OP-44, and a cascoded differential preamplifier using the SSM-2210 transistor pair. The SSM-2210 achieves extremely low input voltage noise performance ($e_n \sim 0.7nV/\sqrt{Hz}$) via a large geometry transistor design which minimizes the base-spreading resistance. This, however, results in relatively higher collector-to-base capacitance (C_{OB}) than ordinary small-signal transistors. For high gain stages, the Miller effect of C_{OB} will limit the voltage gain bandwidth; resorting to a cascode configuration reduces the Miller feedback capacitance, improving stability, bandwidth, and reducing distortion due to base-width modulation. Additionally, cascoding does not increase the noise figure of the overall amplifier system and reduces the high order harmonic distortion.

The circuit in Figure 1 balances the impedance symmetrically in the differential preamp. This serves to reject common-mode noise injected from the power supplies.

Although the SSM-2210's transistors are closely matched, an offset voltage error can still be created by imbalanced source impedances. Accordingly, a precision low-power amplifier (OP-97), configured as a noninverting integrator is implemented which servos-out the offset voltage to less than 100μV referred to the input of the amplifier.

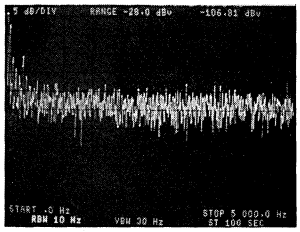


FIGURE 2: *Spectrum Analyzer Display of Wideband Amplifier Noise Spectral Density. $e_n \approx 1.7nV/\sqrt{Hz}$*

Figure 2 illustrates the composite amplifier's low voltage noise density of only $1.7nV/\sqrt{Hz}$ @ 1kHz. Figure 3 and Figure 4 show the excellent pulse response and an extremely low distortion of only 0.0015% over the audio bandwidth, respectively.

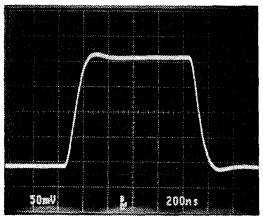


FIGURE 3: *Small-Signal Pulse Response*

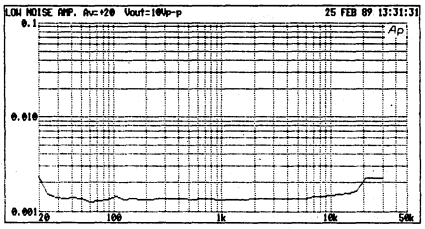


FIGURE 4: *Total Harmonic Distortion vs Frequency*

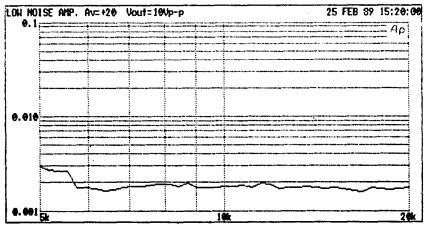


FIGURE 5: *D.I.M. vs Frequency*

A special test was performed to check for dynamic or transient intermodulation distortion. A square wave of 3.15kHz is mixed with a sine wave probe tone, and the resulting intermodulation distortion was found to be less than 0.002% (Figure 5). This is an impressively low value considering the amplifier's gain of 26dB. Interestingly, the GBW product of the composite amplifier was 63MHz which is much larger than that of the OP-44 by itself. This is made possible by the SSM-2210's cascoded preamplifier having a wide bandwidth and large signal gain.

The measured performance of this amplifier is summarized in Table 1.

TABLE 1: Measured Performance of the Low-Noise Wideband Amplifier

Slew-Rate	40V/μs
Gain-Bandwidth	63.6 MHz
Input Noise Voltage Density @ 1kHz	$1.7nV/\sqrt{Hz}$
Output Voltage Swing	±13V
Input Offset Voltage	10μV

500pV/√Hz AMPLIFIER

In situations where low output, low-impedance transducers are used, amplifiers must have very low voltage noise to maintain a good signal-to-noise ratio. The design presented in this application is an operational amplifier with only 500pV/√Hz of broadband noise. The front end uses SSM-2210 low-noise dual transistors to achieve this exceptional performance. The op amp has superb DC specifications compatible with high-precision transducer requirements, and AC specifications suitable for professional audio work.

PRINCIPLE OF OPERATION

The design configuration in Figure 6 uses an OP-27 op amp (already a low-noise design) preceded by an amplifier consisting of three parallel-connected SSM-2210 dual transistors. Base spreading resistance (rbb) generates thermal noise which is reduced by a factor of √3 when the input transistors are parallel connected. Schottky noise, the other major noise-generating mechanism, is minimized by using a relatively high collector current (1mA per device). High current ensures a low dynamic emitter resistance, but does increase the base current and its associated current noise. Higher current noise is relatively unimportant when low-impedance transducers are used.

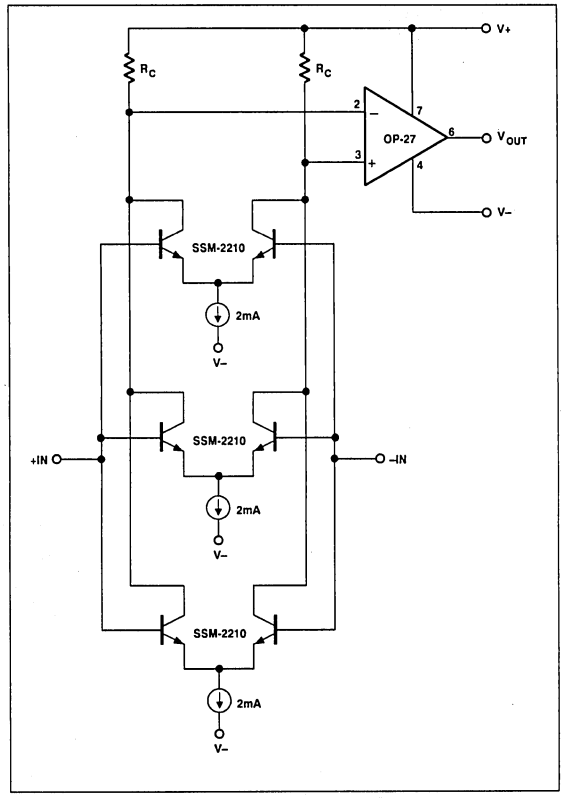


FIGURE 6: *Simplified Schematic*

CIRCUIT DESCRIPTION

The detailed circuit is shown in Figure 7. A total input-stage emitter current of 6mA is provided by Q_4. The transistor acts as a true current source to provide the highest possible common-mode rejection. R_1, R_2, and R_3 ensure that this current splits equally among the three input pairs. The constant current in Q_4 is set by using the forward voltage of a GaAsP light-emitting diode as a reference. The difference between this voltage and the base-emitter voltage of a silicon transistor is predictable and constant (to within a few percent) over the military temperature range. The voltage difference, approximately 1V, is impressed across the emitter resistor R_{12} which produces a temperature-stable emitter current.

R_6 and C_1 provide phase compensation for the amplifier and are sufficient to ensure stability at gains of ten and above.

R_7 is an input offset trim that provides approximately ±300μV trim range. The very low drift characteristics of the SSM-2210 make it possible to obtain drifts of less than 0.1μV/°C when the offset is nulled close to zero. If this trim is not required, the R_4, R_7, and R_8 network should be omitted and R_5/R_9 connected directly to V+.

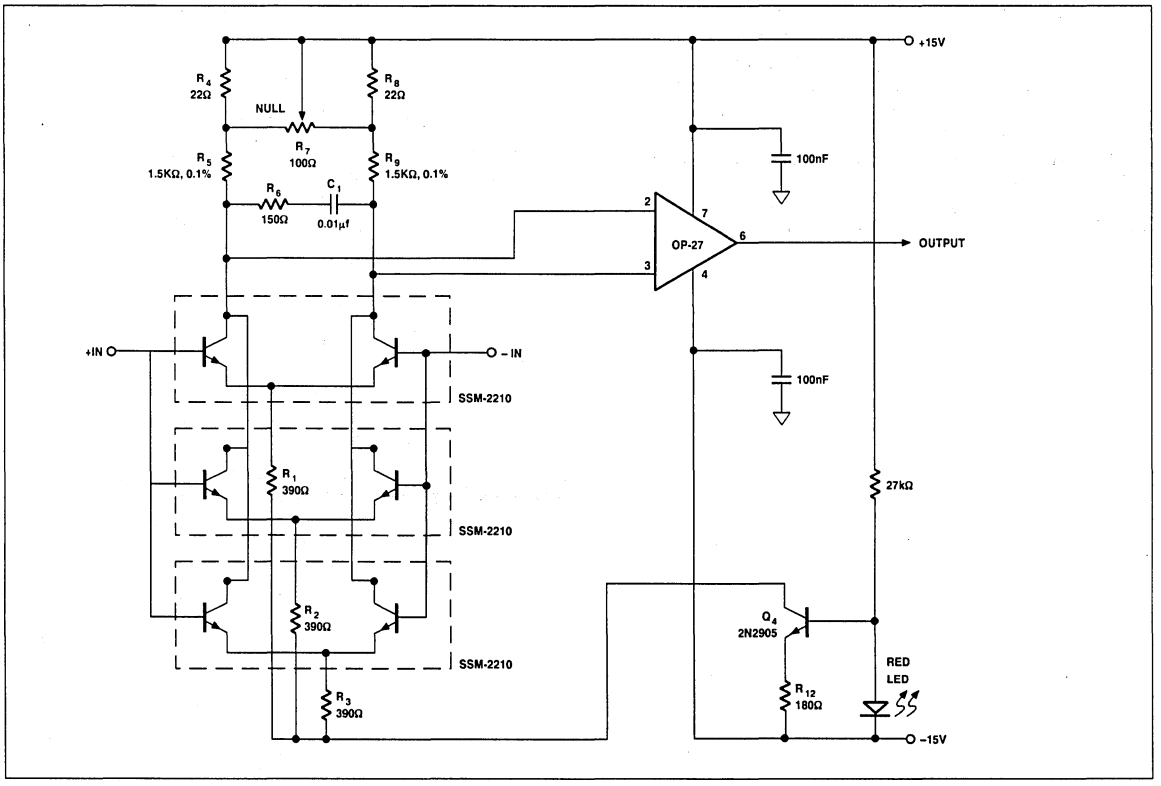


FIGURE 7: *Complete Amplifier Schematic*

AMPLIFIER PERFORMANCE

The measured performance of the op amp is summarized in Table 2. Figure 8 shows the broadband noise spectrum which is flat at about 500pV/√Hz. Figure 9 shows the low-frequency spectrum which illustrates the low 1/f noise corner at 1.5Hz. The low-frequency characteristic in the time domain from 0.1Hz to 10Hz is shown in Figure 10; peak-to-peak amplitude is less than 40nV.

TABLE 2: Measured Performance of the Op Amp

Input Noise Voltage Density at 1kHz		500pV/√Hz
Input Noise Voltage from 0.1Hz to 10Hz		$40nV_{p-p}$
Input Noise Current at 1kHz		1.5pA/√Hz
Gain-Bandwidth	G = 10	3MHz
	G = 100	600kHz
	G = 1000	150kHz
Slew Rate		2V/μs
Open-Loop Gain		3×10^7
Common-Mode Rejection		130dB
Input Bias Current		3μA
Supply Current		10mA
Nulled TCV_{OS}		0.1μV/°C Max
T.H.D. at 1kHz	G = 1000	0.002%

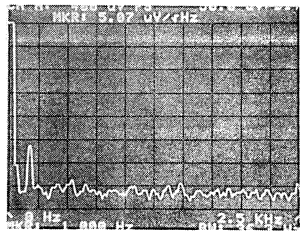


FIGURE 8: *Spectrum Analyzer Display – Broadband*

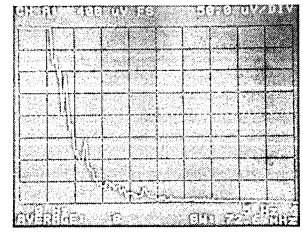


FIGURE 9: *Spectrum Analyzer Display – Low Frequency*

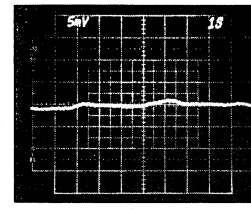


FIGURE 10: *Oscilloscope Display*

CONCLUSION

Using SSM-2210 matched transistor pairs operating at a high current level, it is possible to construct a high-performance, low-noise operational amplifier. The circuit uses a minimum of components and achieves performance levels exceeding monolithic amplifiers.

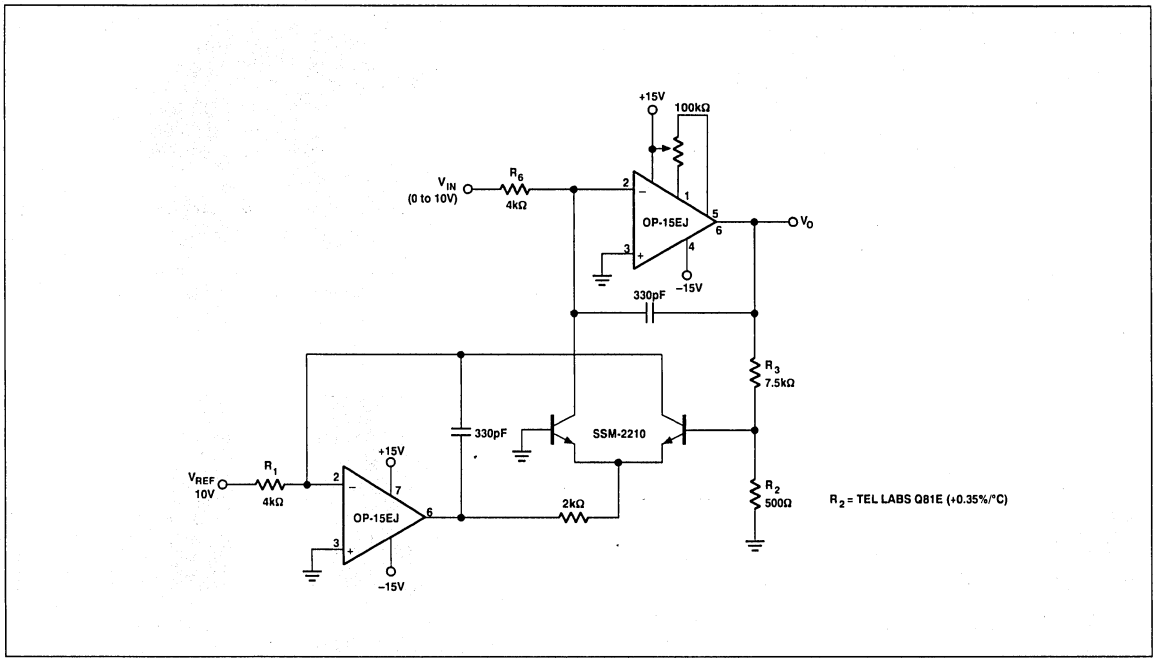


FIGURE 11: *Fast Logarithmic Amplifier*

FAST LOGARITHMIC AMPLIFIER

The circuit of Figure 11 is a modification of a standard logarithmic amplifier configuration. Running the SSM-2210 at 2.5mA per side (full-scale) allows a fast response with wide dynamic range. The circuit has a 7 decade current range, a 5 decade voltage range, and is capable of 2.5μs settling time to 1% with a 1 to 10V step.

The output follows the equation:

$$V_O = \frac{R_3 + R_2}{R_2} \frac{kT}{q} \ln \frac{V_{REF}}{V_{IN}}$$

To compensate for the temperature dependence of the kT/q term, a resistor with a positive 0.35%/°C temperature coefficient is chosen for R_2.

The output is inverted with respect to the input, and is nominally − 1V/decade using the component values indicated.

PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

SSM-2220

AUDIO DUAL MATCHED PNP TRANSISTOR

FEATURES

- Very Low Voltage Noise ..... @ 100Hz, 1nV/$\sqrt{Hz}$ Max
- High Gain Bandwidth ..... 190MHz Typ
- Excellent Gain ..... @ I_C = 1mA, 165 Typ
- Tight Gain Matching ..... 3% Max
- Outstanding Logarithmic Conformance .. r_{BE} = 0.3Ω Typ
- Low Offset Voltage ..... 200μV Max
- Low Cost

APPLICATIONS

- Microphone Preamplifiers
- Tape-Head Preamplifiers
- Current Sources and Mirrors
- Low Noise Precision Instrumentation
- Voltage Controlled Amplifiers/Multipliers

ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	SO 8-PIN†	
SSM2220P	SSM2220S	XIND*

* XIND = −40°C to +85°C

† For availability of SO package, contact your local sales office.

GENERAL DESCRIPTION

The SSM-2220 is a dual low noise matched PNP transistor which has been optimized for use in audio applications.

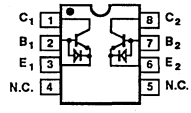
The ultra-low input voltage noise of the SSM-2220 is typically only 0.7nV/$\sqrt{Hz}$ over the entire audio bandwidth of 20Hz to 20kHz. The low noise, high bandwidth (190MHz), and Offset Voltage of (200μV Max) make the SSM-2220 an ideal choice for demanding low noise preamplifier applications.

The SSM-2220 also offers excellent matching of the current gain (Δh_{FE}) to about 0.5% which will help to reduce the high order amplifier harmonic distortion. In addition, to insure the long-term stability of the matching parameters, internal protection diodes across the base-emitter junction were used to clamp any reverse base-emitter junction potential. This prevents a base-emitter breakdown condition which can result in degradation of gain and matching performance due to excessive breakdown current.

Another feature of the SSM-2220 is its very low bulk resistance of 0.3Ω typically which assures accurate logarithmic conformance.

The SSM-2220 is offered in 8-pin plastic, dual-in-line, and SO and its performance and characteristics are guaranteed over the extended industrial temperature range of −40°C to +85°C.

PIN CONNECTIONS



8-PIN
PLASTIC DIP
(P-Suffix)

8-PIN
SO
(S-Suffix)

ABSOLUTE MAXIMUM RATINGS

Collector-Base Voltage (BV_{CBO}) 36V
Collector-Emitter Voltage (BV_{CEO}) 36V
Collector-Collector Voltage (BV_{CC}) 36V
Emitter-Emitter Voltage (BV_{EE}) 36V
Collector Current (I_C) 20mA
Emitter Current (I_E) 20mA
Operating Temperature Range
SSM-2220P ..... –40°C to +85°C
SSM-2220S ..... –40°C to +85°C
Operating Junction Temperature ..... –55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package; Θ_{JA} is specified for device soldered to printed circuit board for SO packages.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2220 MIN	TYP	MAX	UNITS
Current Gain (Note 1)	h_{FE}	V_{CB} = 0V, –36V I_C = 1mA I_C = 100µA I_C = 10µA	80 70 60	165 150 120	– – –	
Current Gain Matching (Note 2)	Δh_{FE}	I_C = 100µA, V_{CB} = 0V	–	0.5	6	%
Noise Voltage Density (Note 3)	e_N	I_C = 1mA, V_{CB} = 0V f_O = 10Hz f_O = 100Hz f_O = 1kHz f_O = 10kHz	– – – –	0.8 0.7 0.7 0.7	2 1 1 1	nV/√Hz
Offset Voltage (Note 4)	V_{OS}	V_{CB} = 0V, I_C = 100µA	–	40	200	µV
Offset Voltage Change vs. Collector Voltage	$\Delta V_{OS}/\Delta V_{CB}$	I_C = 100µA V_{CB1} = 0V V_{CB2} = –36V	–	11	200	µV
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0V I_{C1} = 10µA, I_{C2} = 1mA	–	12	75	µV
Offset Current	I_{OS}	I_C = 100µA, V_{CB} = 0V	–	6	45	nA
Collector-Base Leakage Current	I_{CBO}	V_{CB} = –36V = V_{MAX}	–	50	400	pA
Bulk Resistance	r_{BE}	V_{CB} = 0V, 10µA ≤ I_C ≤ 1mA	–	0.3	0.75	Ω
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA, I_B = 100µA	–	0.026	0.1	V

NOTES:
1. Current gain is measured at collector-base voltages (V_{CB}) swept from 0 to V_{MAX} at indicated collector current. Typicals are measured at V_{CB} = 0V.
2. Current gain matching (Δh_{FE}) is defined as:

$$\Delta h_{FE} = \frac{100(\Delta I_B)\, h_{FE}(MIN)}{I_C}.$$

3. Sample tested. Noise tested and specified as equivalent input voltage for each transistor.
4. Offset voltage is defined as:
$V_{OS} = V_{BE1} - V_{BE2}$,
where V_{OS} is the differential voltage for

$$I_{C2} = I_{C2} : V_{OS} = V_{BE1} - V_{BE2} = \frac{KT}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

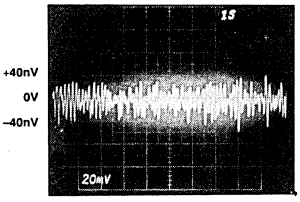
ELECTRICAL CHARACTERISTICS at $-40°C \le T_A \le +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2220 MIN	SSM-2220 TYP	SSM-2220 MAX	UNITS
Current Gain	h_{FE}	V_{CB} = 0V, –36V I_C = 1mA I_C = 100µA I_C = 10µA	60 50 40	120 105 90	– – –	
Offset Voltage	V_{OS}	I_C = 100µA, V_{CB} = 0V	–	30	265	µV
Offset Voltage Drift (Note 1)	TCV_{OS}	I_C = 100µA, V_{CB} = 0V	–	0.3	1.0	µV/°C
Offset Current	I_{OS}	I_C = 100µA, V_{CB} = 0V	–	10	200	nA
Breakdown Voltage	BV_{CEO}		36	–	–	V

NOTE:
1. Guaranteed by V_{OS} test ($TCV_{OS} = V_{OS}/T$ for $V_{OS} << V_{BE}$) where T = 298°K for T_A = 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

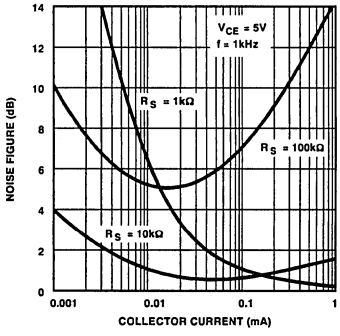
LOW FREQUENCY NOISE



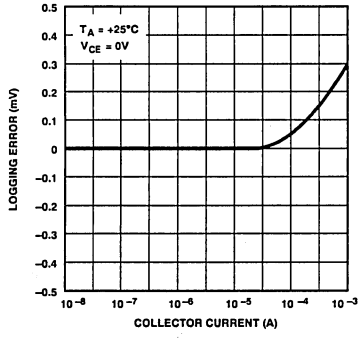
VERTICAL = 40nV/DIV
HORIZONTAL = 1s/DIV

V_{CE} = 5V
I_C = 1mA
T_A = +25°C

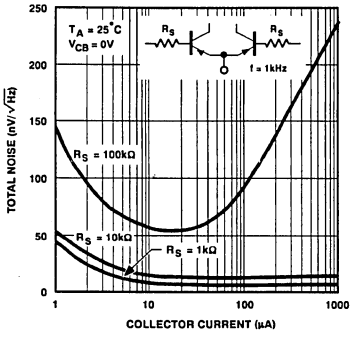
NOISE FIGURE vs COLLECTOR CURRENT



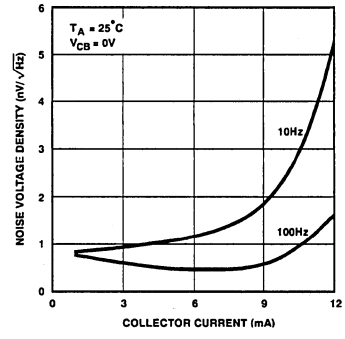
EMITTER-BASE LOG CONFORMITY



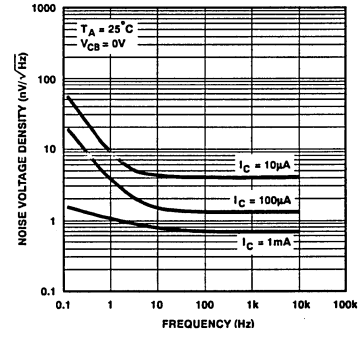
TOTAL NOISE vs COLLECTOR CURRENT



NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT

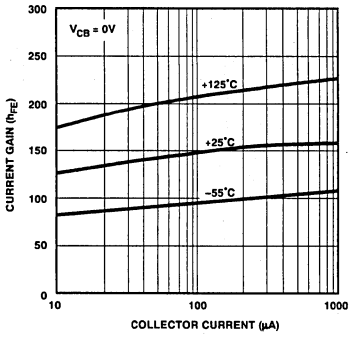


NOISE VOLTAGE DENSITY vs FREQUENCY

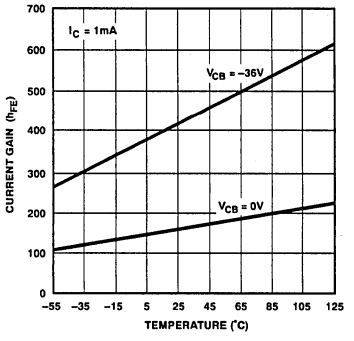


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

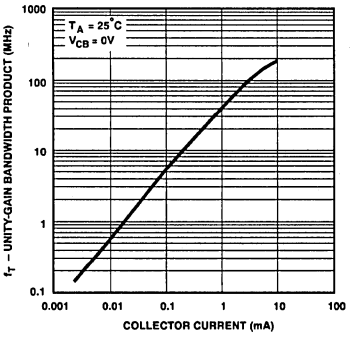
CURRENT GAIN vs COLLECTOR CURRENT



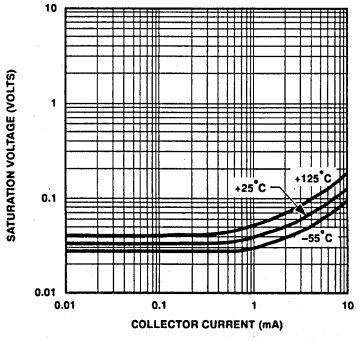
CURRENT GAIN vs TEMPERATURE



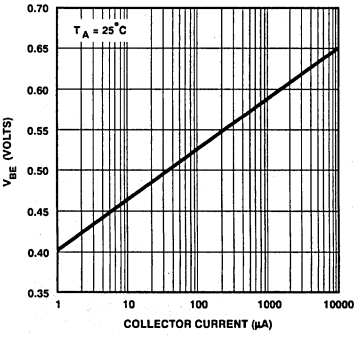
GAIN BANDWIDTH vs COLLECTOR CURRENT



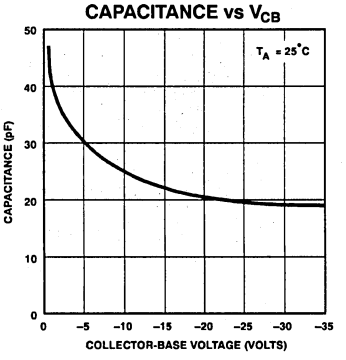
SATURATION VOLTAGE vs COLLECTOR CURRENT



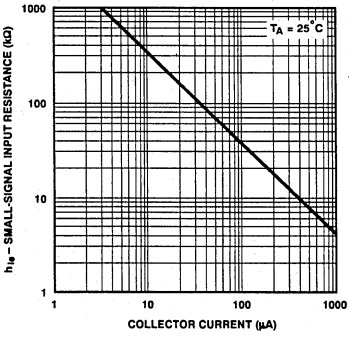
BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT



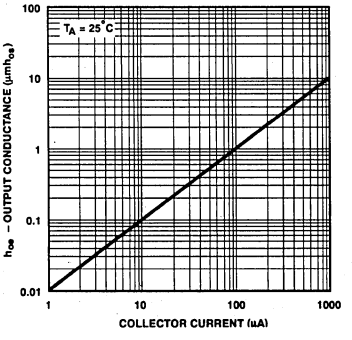
COLLECTOR-BASE CAPACITANCE vs V_{CB}



SMALL-SIGNAL INPUT RESISTANCE (h_{ie}) vs COLLECTOR CURRENT



SMALL-SIGNAL OUTPUT CONDUCTANCE (h_{oe}) vs COLLECTOR CURRENT



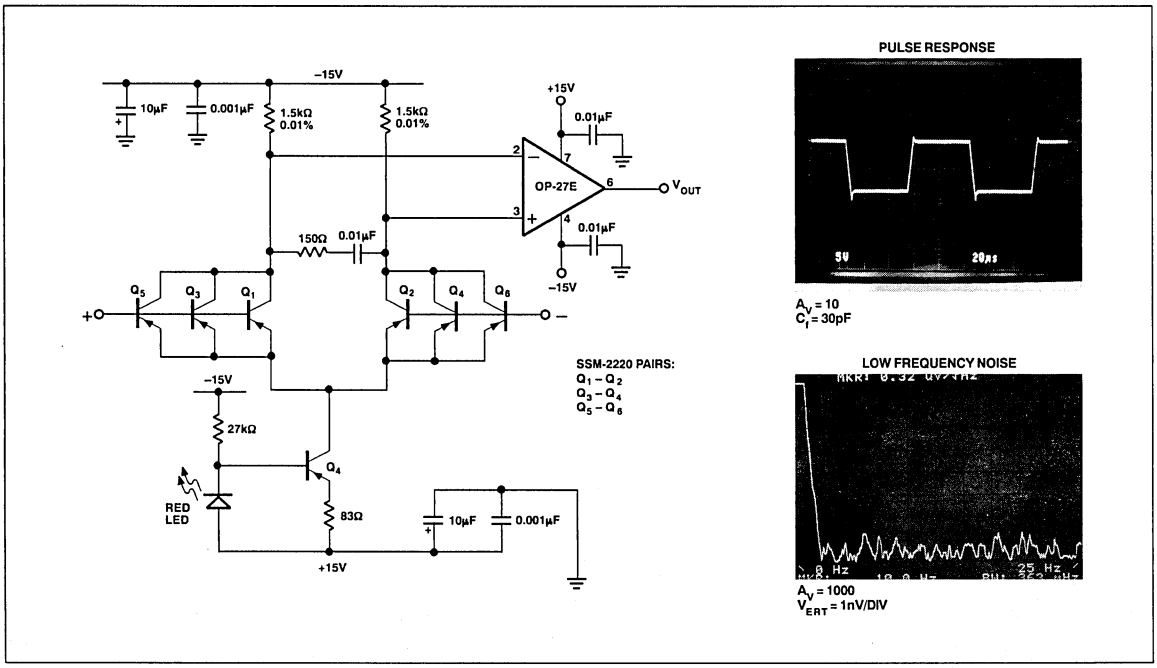


FIGURE 1a: *Super Low Noise Amplifier*

APPLICATIONS INFORMATION

SUPER LOW NOISE AMPLIFIER

The circuit in Figure 1a is a super low noise amplifier with equivalent input voltage noise of 0.32nV/$\sqrt{Hz}$. By paralleling SSM-2220 matched pairs, a further reduction of amplifier noise is attained by a reduction of the base spreading resistance by a factor of 3, and consequently the noise by $\sqrt{3}$. Additionally, the shot noise contribution is reduced by maintaining a high collector current (2mA/device) which reduces the dynamic emitter resistance and decreases voltage noise. The voltage noise is inversely proportional to the square root of the stage current, and current noise increases proportionally to the square root of the stage current. Accordingly, this amplifier capitalizes on voltage noise reduction techniques at the expense of increasing the current noise. However, high current noise is not usually important when dealing with low impedance sources.

This amplifier exhibits excellent full power AC performance, 0.08% THD into a 600Ω load, making it suitable for exacting audio applications (see Figure 1b).

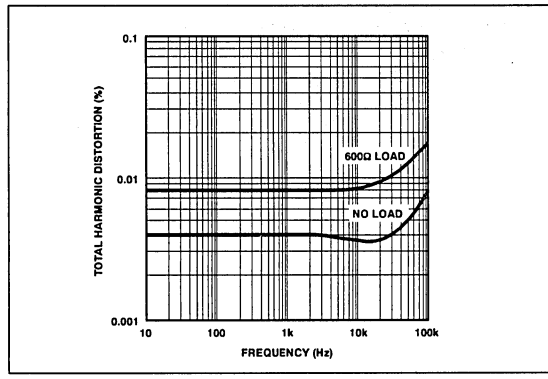


FIGURE 1b: *Super Low Noise Amplifier – Total Harmonic Distortion*

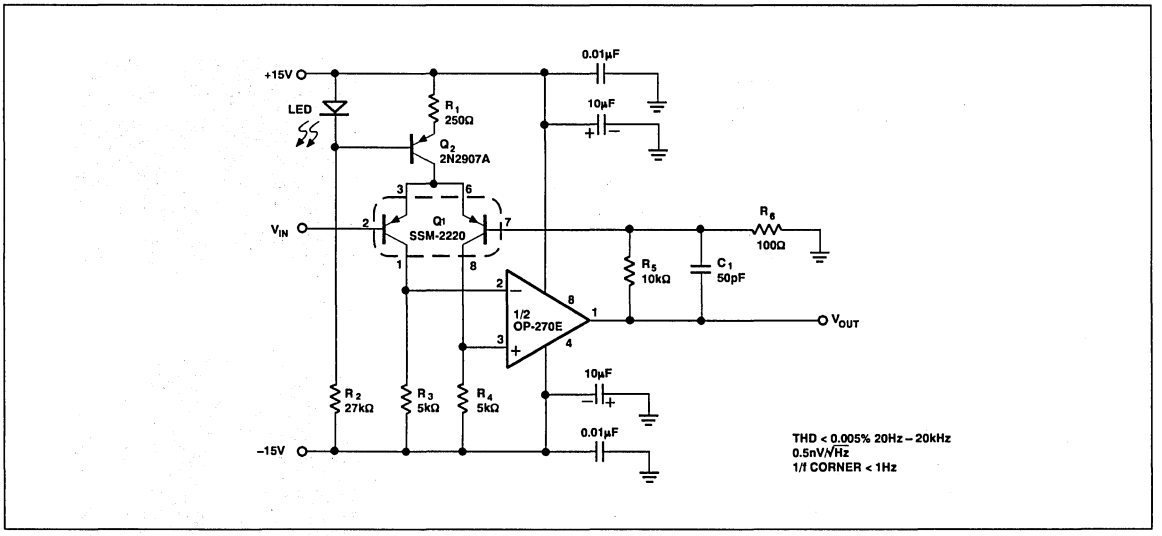


FIGURE 2: *Super Low Noise Amplifier*

LOW NOISE MICROPHONE PREAMPLIFIER

Figure 2 shows a microphone preamplifier that consists of a SSM-2220 and a low noise op amp. The input stage operates at a relatively high quiescent current of 2mA per side, which reduces the SSM-2220 transistor's voltage noise. The $1/f$ corner is less than 1Hz. Total harmonic distortion is under 0.005% for a $10V_{p\text{-}p}$ signal from 20Hz to 20kHz. The preamp gain is 100, but can be modified by varying R_5 or R_6 ($V_{OUT}/V_{IN} = R_5/R_6 + 1$).

A total input stage emitter current of 4mA is provided by Q_2. The constant current in Q_2 is set by using the forward voltage of a GaAsP LED as a reference. The difference between this voltage and the V_{BE} of a silicon transistor is predictable and constant (to a few percent) over a wide temperature range. The voltage difference, approximately 1V, is dropped across the 250Ω resistor which produces a temperature stabilized emitter current.

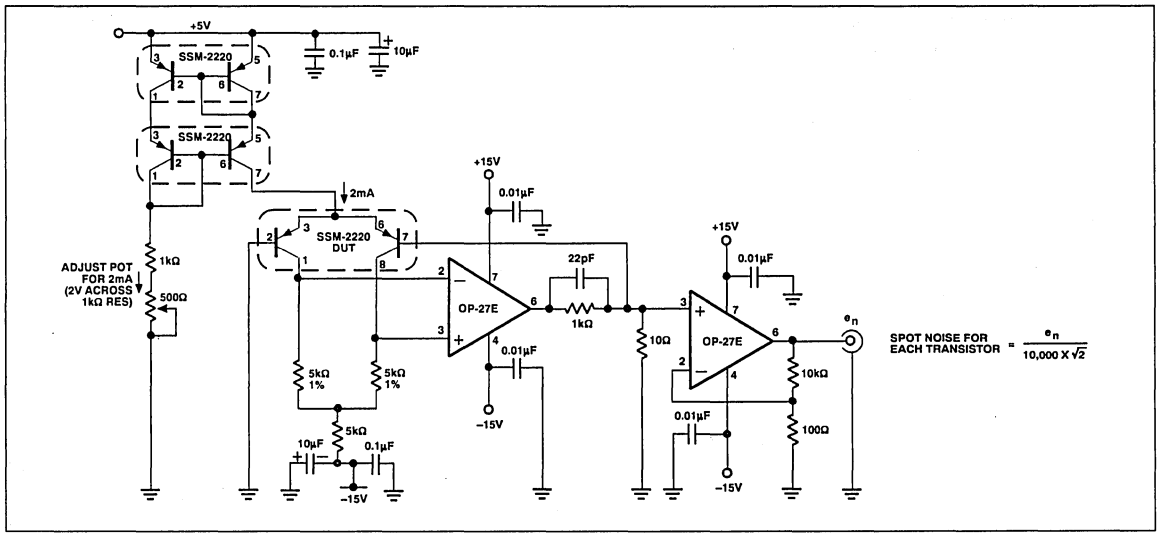


FIGURE 3: *SSM-2220 Voltage Noise Measurement Circuit*

SSM-2220 NOISE MEASUREMENT

All resistive components (Johnson noise, $e_n^2 = 4kTBR$, or $e_n = 0.13\sqrt{R}$ nV/$\sqrt{Hz}$, where R is in kΩ) and semiconductor junctions (Shot noise, caused by current flowing through a junction, produces voltage noise in series impedances such as transistor-collector load resistors, $I_n = 0.556\sqrt{I}$ pA/$\sqrt{Hz}$ where I is in µA) contribute to the system input noise.

Figure 3 illustrates a technique for measuring the equivalent input noise voltage of the SSM-2220. 1mA of stage current is used to bias each side of the differential pair. The 5kΩ collector resistors noise contribution is insignificant compared to the voltage noise of the SSM-2220. Since noise in the signal path is referred back to the input, this voltage noise is attenuated by the gain of the circuit. Consequently, the noise contribution of the collector load resistors is only 0.048nV/$\sqrt{Hz}$. This is considerably less than the typical 0.8nV/$\sqrt{Hz}$ input noise voltage of the SSM-2220 transistor.

The noise contribution of the OP-27 gain stages is also negligible due to the gain in the signal path. The op amp stages amplify the input referred noise of the transistors to increase the signal strength to allow the noise spectral density (e_{in} x 10000) to be measured with a spectrum analyzer. And, since we assume equal noise contributions from each transistor in the SSM-2220, the output is divided by $\sqrt{2}$ to determine a single transistor's input noise.

Air currents cause small temperature changes that can appear as low frequency noise. To eliminate this noise source, the measurement circuit must be thermally isolated. Effects of extraneous noise sources must also be eliminated by totally shielding the circuit.

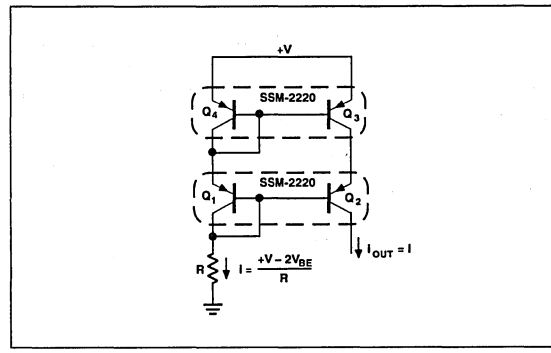


FIGURE 4: *Cascode Current Source*

CURRENT SOURCES

A fundamental requirement for accurate current mirrors and active load stages is matched transistor components. Due to the excellent V_{BE} matching (the voltage difference between V_{BE}'s required to equalize collector current) and gain matching, the SSM-2220 can be used to implement a variety of standard current mirrors that can source current into a load such as an amplifier stage. The advantages of current loads in amplifiers versus resistors is an increase of voltage gain due to higher impedances, larger signal range, and in many applications, a wider signal bandwidth.

Figure 4 illustrates a cascode current mirror consisting of two SSM-2220 transistor pairs.

The cascode current source has a common base transistor in series with the output which causes an increase in output impedance of the current source since V_{CE} stays relatively constant. High frequency characteristics are improved due to a reduction of Miller capacitance. The small-signal output impedance can be determined by consulting "h_{oe} vs. Collector Current" typical graph. Typical output impedance levels approach the performance of a perfect current source.

Considering a typical collector current of 100µA, we have:

$$ro_{Q3} = \frac{1}{1.0\mu MHOS} = 1M\Omega.$$

Q_2 and Q_3 are in series and operate at the same current level, so the total output impedance is:

$$R_O = h_{FE}\, ro_{Q3} \approx (160)(1M\Omega) = 160M\Omega.$$

CURRENT MATCHING

The objective of current source or mirror design is generation of currents that are either matched or must maintain a constant ratio. However, mismatch of base-emitter voltages cause output current errors. Consider the example of Figure 5. If the resistors and transistors are equal and the collector voltages are the same, the collector currents will match precisely. Investigating the current-matching errors resulting from a non-zero V_{OS}, we define ΔI_C as the current error between the two transistors.

Graph 5 describes the relationship of current matching errors versus offset voltage for a specified average current I_C. Note that since the relative error between the currents is exponentially proportional to the offset voltage, tight matching is required to design high accuracy current sources. For example, if the offset voltage is 5mV at 100µA collector current, the current matching error would be 20%. Additionally, temperature effects such as offset drift (3µV/°C per mV of V_{OS}) will degrade performance if Q_1 and Q_2 are not well matched.

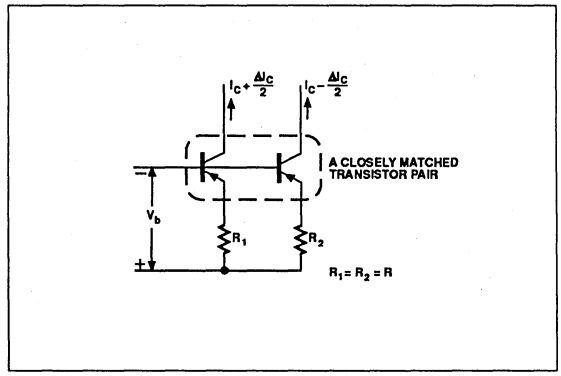


FIGURE 5a: *Current Matching Circuit*

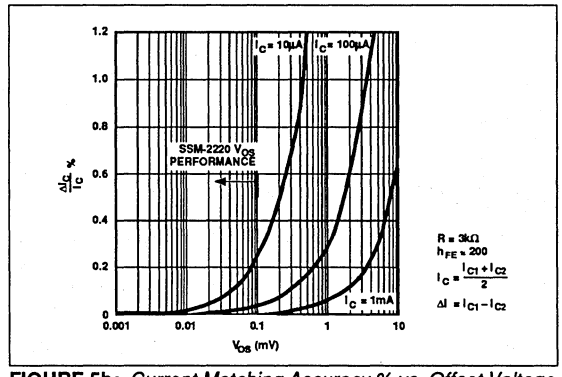


FIGURE 5b: *Current Matching Accuracy % vs. Offset Voltage*

SSM-2110
TRUE RMS-TO-DC CONVERTER

FEATURES

- Multiple Output Options (Absolute Value, RMS, Log RMS, Log Absolute Value, Average Absolute Value)
- Wide Dynamic Range 100dB
- Prebias Option for Fast Response at Low Signal Levels
- On-Chip Log Output Amplifier
- Optional Internal Log Output Temperature Compensation
- Low Drift Internal Voltage Reference
- Low Cost

APPLICATIONS

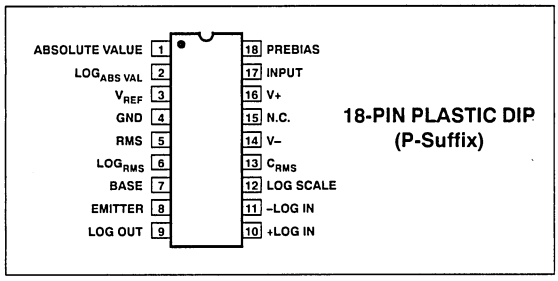
- Audio Dynamic Range Processors
- Audio Metering Systems
- Digital Multimeters
- Noise Testers
- Panel Meters
- Power Meters
- Process Control Systems

GENERAL DESCRIPTION

The SSM-2110 is a true RMS-to-DC converter designed to provide multiple linear and logarithmic output options. The linear outputs, true RMS and absolute value, can be obtained simultaneously with the absolute value output configurable to give a peak function. The logarithmic outputs can provide log RMS, log absolute value or log average absolute value. Full on-chip temperature compensation is available for each output option.

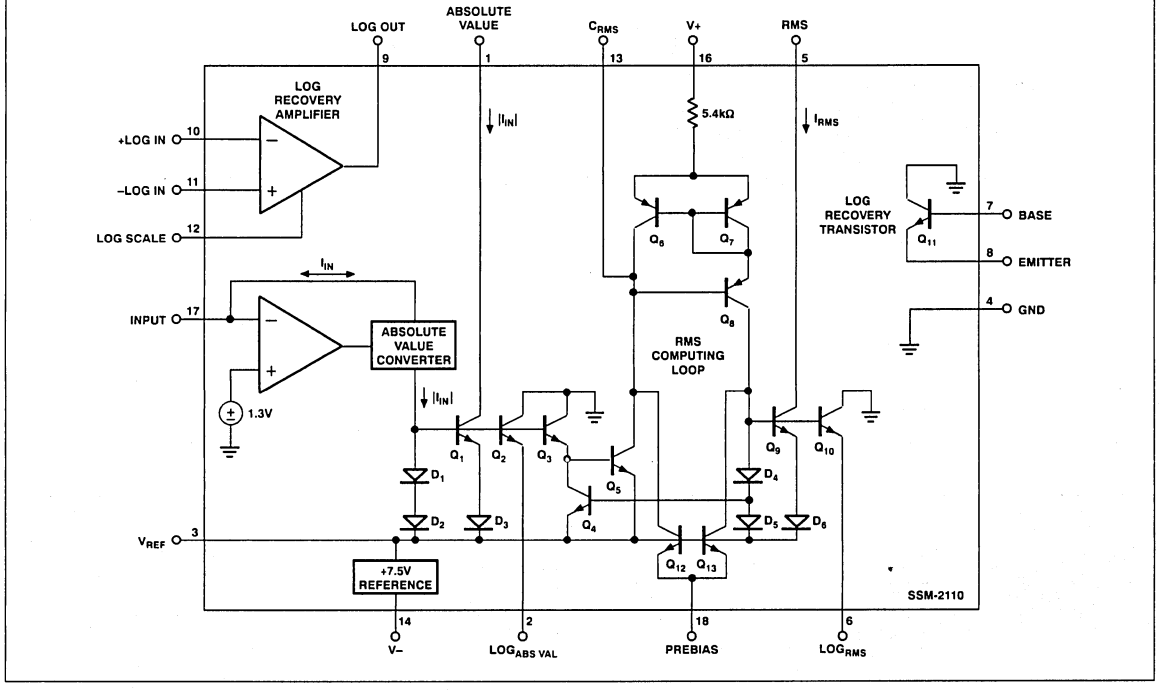
Continued

PIN CONNECTIONS



18-PIN PLASTIC DIP
(P-Suffix)

FUNCTIONAL DIAGRAM



The SSM-2110 has been granted mask work protection under the Semiconductor Chip Protection Act of 1983.

GENERAL DESCRIPTION *Continued*

The SSM-2110 has a dynamic range of 100dB. A unique on-chip prebias circuit enables the users to trade dynamic range at low signal levels for a faster response time. As a precision level detector, the SSM-2110 has applications in digital multimeters, panel meters, process control and audio systems.

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 18-PIN	
SSM2110P	–25°C to +75°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range
(Soldering, 60 sec) ..... +300°C
Junction Temperature ..... +150°C
Operating Temperature Range ..... –25°C to +75°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
18-Pin Plastic DIP (P)	75	33	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ and $R_{SCALE} = 4.7k\Omega$, unless otherwise noted.

			SSM-2110			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic Range	DR	$30nA_{p-p} \le I_{INp-p} \le 3mA_{p-p}$	100	110	–	dB
Unadjusted Gain		$I_{IN} = \pm 1mA$	0.95	1.0	1.05	
Error (Mean or RMS)			–	–	±0.5	dB
Output Offset Current	I_{OOS}	$I_{IN} = \pm 1mA$	–	5	15	nA
I_{OS} Shift	ΔI_{OOS}	$R_{PREBIAS} = 3M\Omega$	–	50	120	nA
Crest Factor @ $1mA_{RMS}$	CF	For 0.1dB Additional Error	–	2.5	–	
		For 0.5dB Additional Error	–	5	–	
		For 1.0dB Additional Error	–	8	–	
RMS Filter Time Constant	t_{CON}	$I_{RMS} > 10\mu A_{RMS}$		$11k\Omega \times C_{INT}$		
Frequency Response (Sine Wave)						
For 0.1dB Additional Error		$I_{IN} > 1mA_{RMS}$	–	400	–	
		$I_{IN} > 10\mu A_{RMS}$	–	10	–	
		$I_{IN} > 1\mu A_{RMS}$	–	2	–	
For 0.5dB Additional Error	BW	$I_{IN} > 1mA_{RMS}$	–	1000	–	kHz
		$I_{IN} > 10\mu A_{RMS}$	–	50	–	
		$I_{IN} > 1\mu A_{RMS}$	–	7.5	–	
–3dB Bandwidth		$I_{IN} > 1mA_{RMS}$	–	1500	–	
		$I_{IN} > 10\mu A_{RMS}$	–	300	–	
		$I_{IN} > 1\mu A_{RMS}$	–	50	–	
Log Amp Output Offset Current (Pin 9)	$I_{OOS\ -LOG}$		–	±3.3	±13	µA
Max Log Amp Output (Pin 9)	$I_{OUT\ -LOG}$		±250	±265	±288	µA
Log Scale Factor (Pin 2 or Pin 6)			–	+6	–	mV/dB
Log Mode Zero Crossing (Mean or RMS, Pin 9)		RMS In To Get Zero Out (See Figure 7)	–	10	–	µA
Log Amp Linearity (Pin 9)		$-240mV < V_{PIN\ 10} - V_{PIN\ 11} < +240mV$	–	0.1	0.25	dB
Log Output Tempco	T_C	$0°C < T_A < +70°C$	–	±75	–	ppm/°C
V_{REF} (Pin 3 to V–)			6.7	7.5	7.8	V

ELECTRICAL CHARACTERISTICS at V_S = ± 15V, T_A = +25°C and R_{SCALE} = 4.7kΩ, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SSM-2110 MIN	TYP	MAX	UNITS
Positive Supply Current	I_S+	I_{IN} = 0	480	–	920	µA
Negative Supply Current	I_S–		2.1	–	3.3	mA
Supply Voltage Range	V_S		±12	–	±18	V

Specifications subject to change; consult latest data sheet.

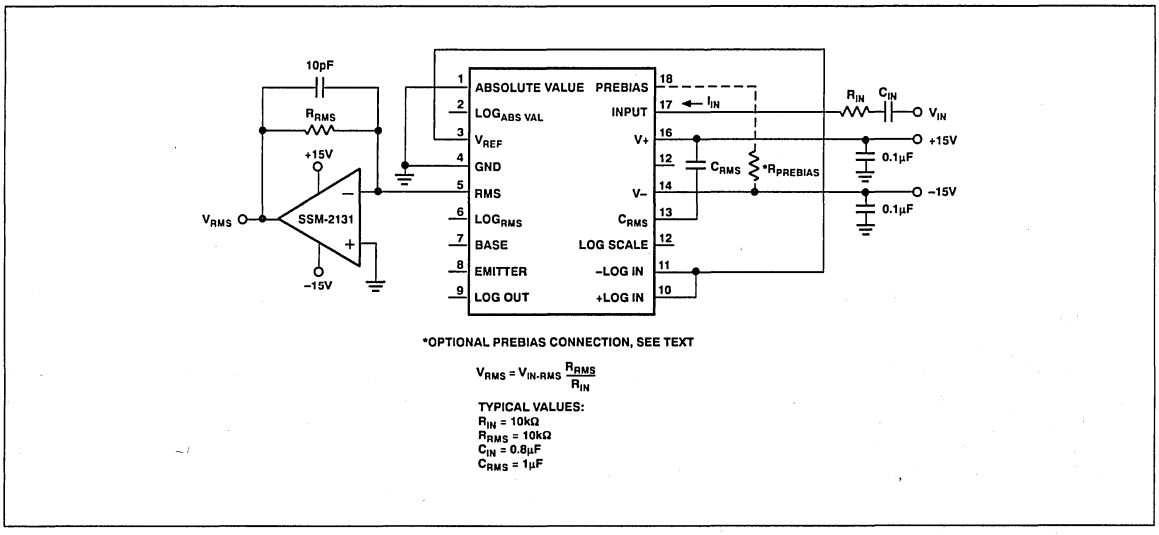


FIGURE 1: *RMS Output Circuit*

THE RMS COMPUTING LOOP

The RMS section of the SSM-2110 consists of an implicit RMS computing loop whose output follows the equation:

$$I_O = \frac{I_{IN}^2}{\overline{I_O}}$$

where $\overline{I_O}$ is the average of I_O

The time constant for averaging is determined by the value of the averaging cap C_{RMS} (on pin 13) and an internal resistor whose effective value is 10.8kΩ. A very low leakage capacitor must be used for C_{RMS} to prevent limiting the dynamic range.

Increasing the value of C_{RMS} will result in lower levels of ripple on the RMS Output at the expense of an increase in settling time for a step change in the input signal amplitude. This is a proportional relationship where increasing the value of C_{RMS} tenfold results in a tenfold increase in the settling time.

For the circuit in Figure 1, the peak-to-peak ripple approximately follows the equation:

$$V_{RIPPLE(p\text{-}p)} = \frac{2\sqrt{2} \times V_{RMS}}{4\pi f R_{INT} C_{RMS}} \times \frac{R_{RMS}}{R_{IN}}$$

where $R_{INT} \approx 10.8k\Omega$

The settling time of the SSM-2110 also depends on the frequency of the signal being processed. It takes approximately 100ms for a 300µA$_{p\text{-}p}$, 50Hz signal to settle within 0.1% when C_{RMS} = 1µF, and it takes 10ms for a 500Hz signal to settle within the same value. The general rule is a tenfold increase in frequency causes a tenfold reduction in settling time. The settling time also varies with the amplitude of the signal. The larger the signal level the faster the settling time.

INPUT

The INPUT (pin 17) is an AC virtual ground with approximately +1.3V DC offset voltage. The useful dynamic range of input current the device can process is 100dB (3mA$_{p-p}$ to 30nA$_{p-p}$). The input RC network is usually chosen to allow close to 20dB of headroom in order to process high crest factor signals and provide a DC block below a given frequency band. Since in every case the ratio of R_{OUT} (R_{AV} and R_{RMS}) to R_{IN} determines the overall gain of the circuit, R_{OUT} must also be considered when selecting the low frequency breakpoint. The maximum recommended values for R_{OUT} vary from 4kΩ to 10kΩ for the circuits in Figures 1, 3, 4, and 5.

Referring to the circuit in Figure 3, and assuming a gain of 1 is desired, R_{IN} should be set to 4kΩ (R_{RMS} and R_{AV} = 4kΩ). Based on this value of R_{IN}, C_{IN} should be 2μF to place the subsonic filter pole at 20Hz. If you wish to limit the lower frequency to something other than 20 Hz then C_{IN} should be changed accordingly. The low frequency pole is governed by the simple equation

$$f_{MIN} = 1/2\pi R_{IN} C_{IN}$$

C_{IN} should be a very low leakage capacitor to avoid impairing the dynamic range at low signal levels (many electrolytic types will not work).

The choice of R_{IN} = 10kΩ in Figure 1 is good for processing 0dBV reference signals. Given a nominal signal level of 0dBV (2.828V$_{p-p}$ = 1 V_{RMS}), this voltage across the 10kΩ input resistor gives a nominal input current of 283μA$_{p-p}$, which allows 20dB of headroom. The three other common choices for R_{IN} are 4kΩ, 5kΩ and 8kΩ, which provide 12dB, 14dB, and 18dB respectively.

The values of C_{IN}, R_{IN} and R_{OUT} can be changed accordingly to vary output levels to system requirements.

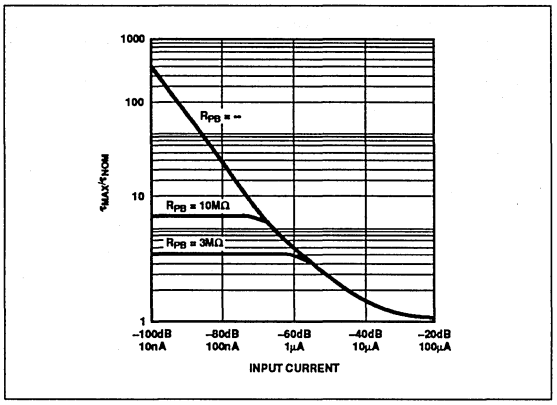


FIGURE 2: *Normalized Time Constant Relative to 1mA$_{RMS}$*

The PREBIAS pin (pin 18), can be used to increase the speed of the RMS computing loop at low signal levels at some expense to the dynamic range. Below a 10μA$_{RMS}$ input level, the time constant of the RMS loop will increase from its nominal value by a factor of 10 for every 20dB drop in level.

By use of the PREBIAS pin, one can ensure that the loop time constant will not increase above a chosen maximum as the signal level continues to decrease. The equation relating the maximum time constant increase to the value of $R_{PREBIAS}$ connected between pin 18 and V– is given by:

$$\frac{\tau_{MAX}}{\tau_{NOM}} = \frac{10\mu A \times R_{PREBIAS}}{6.8V} \quad \text{(See Figure 2)}$$

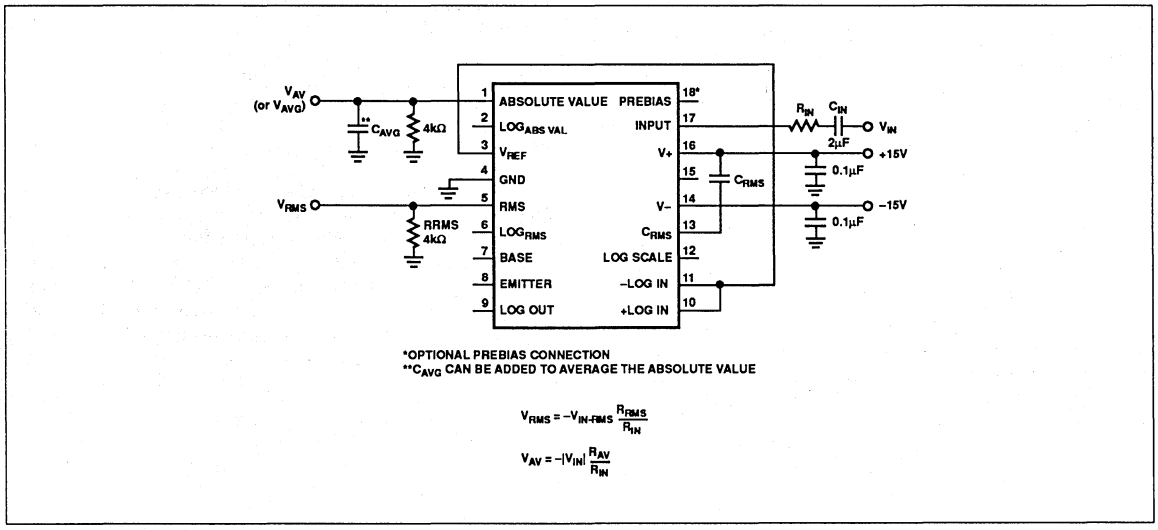


FIGURE 3: *Simple RMS/Absolute Value/Average Absolute Value Configuration*

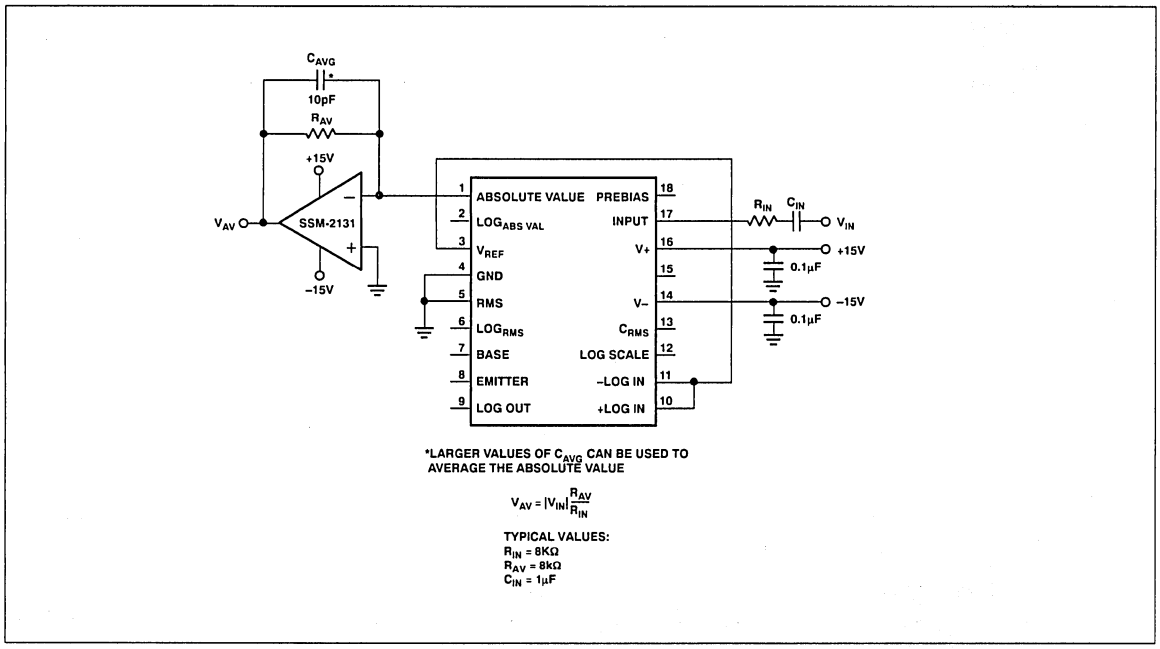


FIGURE 4: *Absolute Value and Average Absolute Value Output*

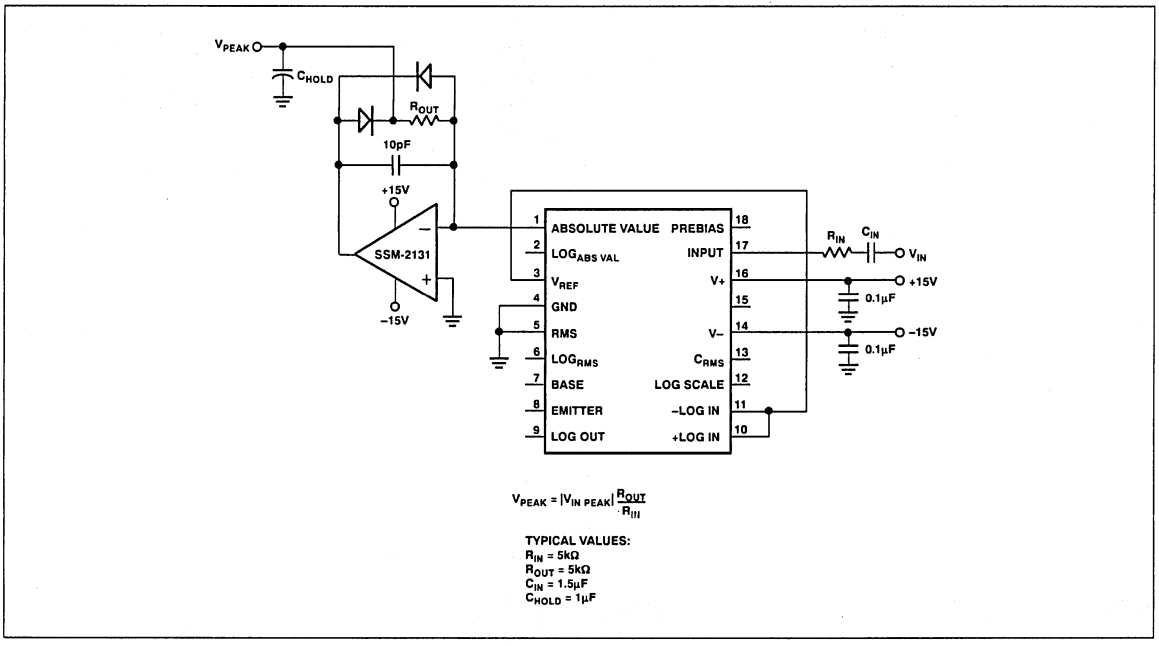


FIGURE 5: *Peak Voltage Output*

LINEAR OUTPUTS (ABSOLUTE VALUE AND RMS)

The instantaneous absolute value of the input signal appears as a current absolute value pin (pin 1). The true RMS value of the input signal similarly appears as a current into the RMS pin (pin 5). With ±15 volt supplies, the voltage compliance on these outputs is from +15 to –6 volts. For simple applications it is possible to convert these currents to negative output voltages by connecting a resistor in series with the pin(s) to ground (see Figure 3). For a maximum $3mA_{p-p}$ input signal, the resistor(s) value should be 4.0kΩ or less. To obtain an average of the absolute value output, capacitor C_{AVG} can be added in parallel with R_{AV}.

More commonly, a positive going voltage at low impedance is desired as an output. This can be accomplished by connecting a linear output pin to the virtual ground of an op amp configured as a current-to-voltage converter (see Figures 1 and 4). The scale factor for the conversion is determined by the value of R_{IN} and the feedback resistor (R_{RMS} or R_{AV}).

For the absolute value circuit in Figure 4, a maximum feedback resistor (R_{AV}) of 8kΩ allows maximum swing of the SSM-2131 output amplifier. Given a maximum output signal of $1.5mA_{PEAK}$ the SSM-2131 will be able to swing to +12V. If values larger than 8kΩ are used, then signal clipping may result.

For the RMS output circuit in Figure 1, the maximum feedback resistor (R_{RMS}) can be 10kΩ since the RMS level should never exceed 1.2mA.

A peak output can be implemented by using the circuit in Figure 5. The output scale factor is determined by R_{OUT}/R_{IN}. The decay time constant is equal to the product $R_{OUT}C_{HOLD}$. For this circuit, the feedback resistor (R_{OUT}) should be kept below 5kΩ.

A small capacitor (10pF) is usually added in parallel with the feedback resistor for stability particularly if a high slew rate JFET input op amp is used. In Figure 4, this capacitor (C_{AVG}) can be made large to obtain an average of the absolute value output. If the averaging circuit is implemented then R_{IN} can be increased to a maximum of 10kΩ since the 1.5mA peaks will no longer be present.

If the signal levels being processed are less than $3mA_{p-p}$ then the above mentioned feedback resistors can be increased accordingly.

The circuits in Figures 1 and 4 can be connected at the same time providing the user with multiple functions from a single SSM-2110. R_{IN}, R_{RMS} and R_{AV} should be set so that clipping does not occur.

The linear output pins must be kept within their voltage compliance range for proper device operations. An unused linear output must always be terminated, preferably to ground.

LOG OUTPUTS (LOG_{RMS} AND $LOG_{ABS\ VAL}$)

The log of the instantaneous absolute value and the log of true RMS of the input signal appears as voltages on pins 2 and 6 respectively. However, these outputs must be buffered, level shifted and, in many applications, temperature compensated in order to be made useful.

The log recovery transistor is an internal level shifting component which may be switched between the two log outputs. This will reference the log output(s) to the internal voltage regulator which is about 7.5V above the negative supply (see Figure 6).

Figures 6, 7, and 8 show the recommended connection between the log output transistor Q_2 or Q_{10}, and the log recovery transistor Q_{11}. Note that although the log recovery transistor can be switched between the two log outputs, only one log output can be recovered at a time. With the resistor values R_{REF1} and R_{REF2} shown, the output swing at the emitter of Q_{11} over the dynamic

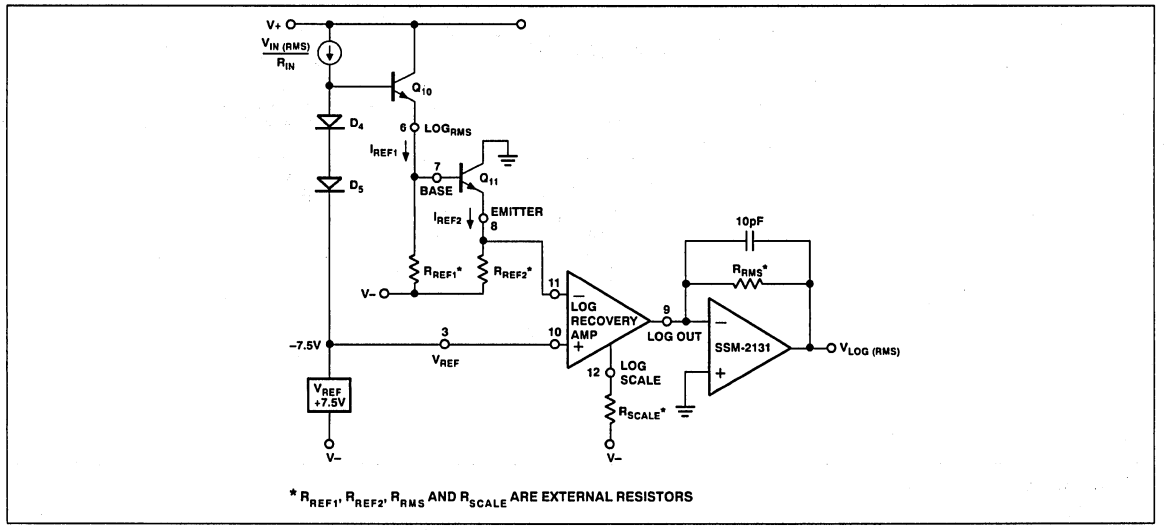


FIGURE 6: *Log Recovery Circuit*

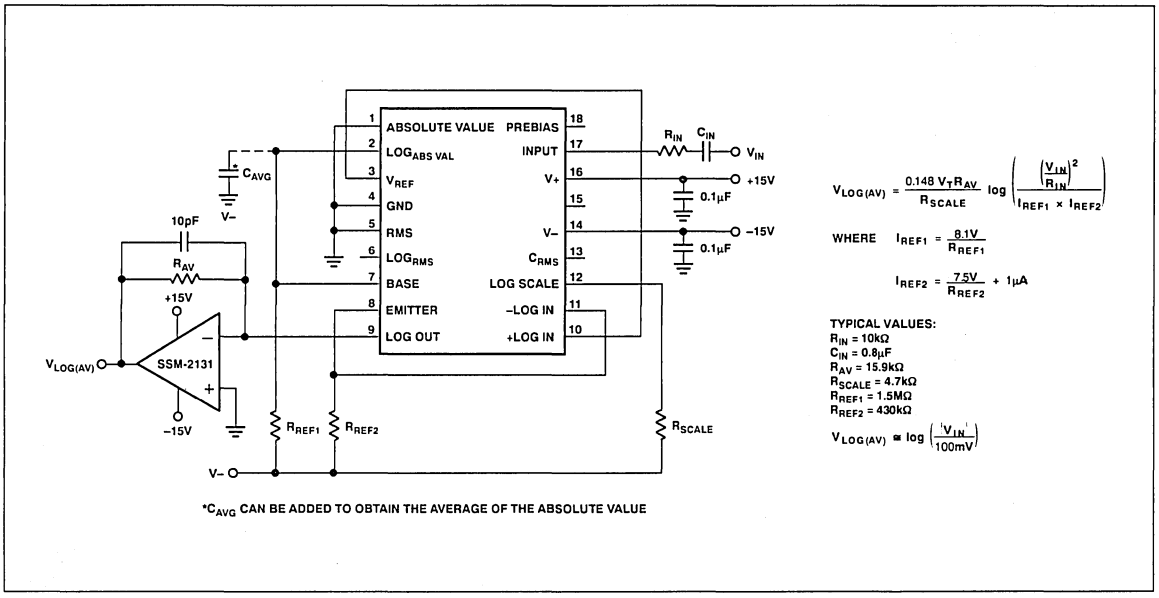


FIGURE 7: *Log of Absolute Value/Average Absolute Value*

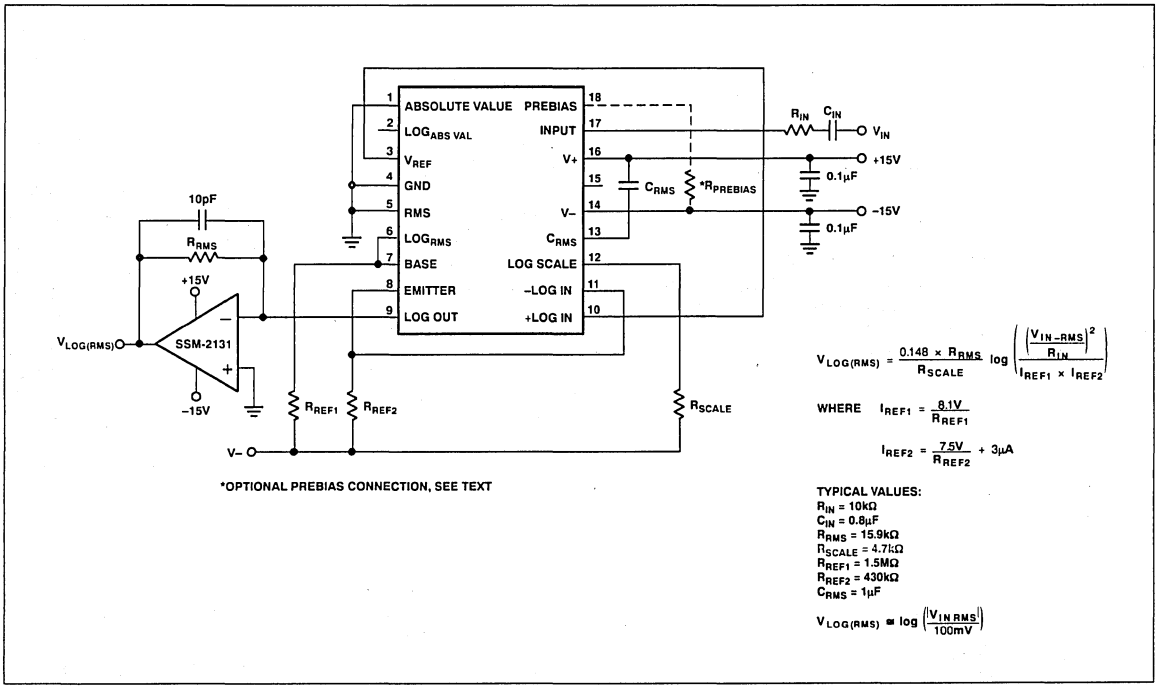


FIGURE 8: *Log of RMS*

range of the device will be roughly symmetrical about the internal negative voltage reference. Also, the output impedance will be low enough to drive the log amplifier's input(s) without introducing significant errors. The bias current into the pins of the log amplifier is typically less than 1μA but can be as high as 2μA. For this reason the current through the log recovery transistor Q_{11} should always be set higher than 5μA. The current I_{REF1} should not be set too high (above 50μA) because the base current of Q_{10} induces errors in the RMS computing loop. If higher reference currents are required then they should be taken care of by changing the current through Q_{11}. This can be done by changing R_{REF2}. The Log Recovery Amplifier Section explains this in more detail.

The output sensitivity at EMITTER (pin 8) is about +60mV for every 10dB of signal level increase at 25°C. This sensitivity has a temperature coefficient of +3300ppm/°C.

The log of absolute value output can be converted to a log of mean value by connecting a capacitor between $LOG_{ABS\ VAL}$ (pin 2) and V– (see Figure 7). Since this is an emitter follower output, the response to a large-signal level increase will be fast while the time constant of the output following a large-signal level decrease will be determined by the product of capacitor C_{AVG} and resistor R_{REF1}.

One might think that connecting a capacitor to the log output would produce the average of the log of the absolute value. However, since the capacitor enforces an AC ground at the emitter of the output transistor, the capacitor charging currents are proportional to the antilog of the signal at the base. Since the base voltage is the log of the absolute value, the log and the antilog terms cancel, and the capacitor is charged as a linear integrator with a current directly proportional to the absolute value of the input current. This effectively inverts the order of the averaging and logging operations. The signal at the output, therefore, is the log of the average of the absolute value of the input signal.

LOG RECOVERY AMPLIFIER (PINS 9,10, 11 AND 12)

The log recovery amplifier is a linearized voltage-to-current transconductor whose gain can be made proportional to absolute temperature. It is used to reference the log output(s) to ground and also to temperature compensate the V_T (KT/q) terms in the log output recovery transistors (Q_2/Q_{10} and Q_{11}).

One input of the log recovery amplifier is usually connected to EMITTER (the emitter of the log recovery transistor–pin 8) while the other is connected to V_{REF} (pin 3).

Figure 6 shows the internal and external connections used to obtain an output voltage equal to $V_{LOG(RMS)}$. The transfer characteristic of the log recovery transistors is given by the following equation:

$$\Delta V_{IN} = V_T \times \ln\left(\frac{(V_{IN(RMS)}/R_{IN})^2}{I_{REF1} \times I_{REF2}}\right)$$

where, $I_{REF1} \approx \left(\frac{8.1V}{R_{REF1}}\right)$

$$I_{REF2} \approx \left(\frac{7.5V}{R_{REF2}}\right) + 1\mu A$$

The transfer characteristic of the log recovery amplifier is given by the following equation:

$$I_{OUT} = \frac{64mV\ \Delta V_{IN}}{R_{SCALE}\ V_T}$$

Combining the two equations yields the overall transfer characteristic for the ouput voltage $V_{LOG(RMS)}$:

$$V_{LOG(RMS)} = \frac{0.148 \times R_{RMS}}{R_{SCALE}} \times \log\left(\frac{(V_{IN}/R_{IN})^2}{I_{REF1} \times I_{REF2}}\right)$$

where, $I_{REF1} \approx \left(\frac{8.1V}{R_{REF1}}\right)$

$$I_{REF2} \approx \left(\frac{7.5V}{R_{REF2}}\right) + 1\mu A$$

Ideally this voltage is completely independent of temperature. However, due to the temperature coefficient of several transistors internal to the SSM-2110, this is not entirely true. The temperature coefficient is approximately ±75ppm/°C.

With the values shown in Figures 7 and 8, this transfer function corresponds to an output change of 50mV/dB. The reference current is set to 10μA to provide the widest possible dynamic range. The following results can be expected for the circuit in Figure 8:

$V_{IN\ (RMS)}$	100μV	1mV	10mA	100mV	1V	10V
$I_{IN\ (RMS)}$	10nA	100nA	1μA	10μA	100μA	1mA
$V_{LOG\ OUT}$	–3V	–2V	–1V	0V	1V	2V

An R_{SCALE} value of approximately 4.7kΩ gives the best overall linearity and temperature compensation performance. This is an improvement of about a factor of 40 over the uncompensated drift. A 2kΩ resistor in series with a silicon diode can be connected from LOG SCALE (pin 12) to the negative supply to defeat the temperature compensation for certain applications such as compressor/limiters where the log drift will cancel the thermal gain drift of a VCA's dB/volt control port.

The maximum output current for both the compensated and uncompensated examples above is ±250μA. This output current is converted to a voltage with the circuits in Figures 7 and 8. For these circuits this corresponds to a maximum output voltage of ±3.975V. If R_{SCALE} is changed from the nominal value of 4.7kΩ the maximum output current will also change by the following equation:

$$I_{LOG\ OUT(MAX)} = \frac{1.18V}{R_{SCALE}}$$

If the log recovery amplifier is not used, +LOG IN (pin 10) and –LOG IN (pin 11) must be connected to V_{REF} (pin 3) for proper operation of the rest of the circuit.

It is possible to use one of the log configurations in Figure 7 or 8 in conjunction with the linear output circuits (Figures 1, 3, 4 and 5) but care must be taken in choosing the appropriate resistor values. This provides the user with substantial flexibility from a single device.

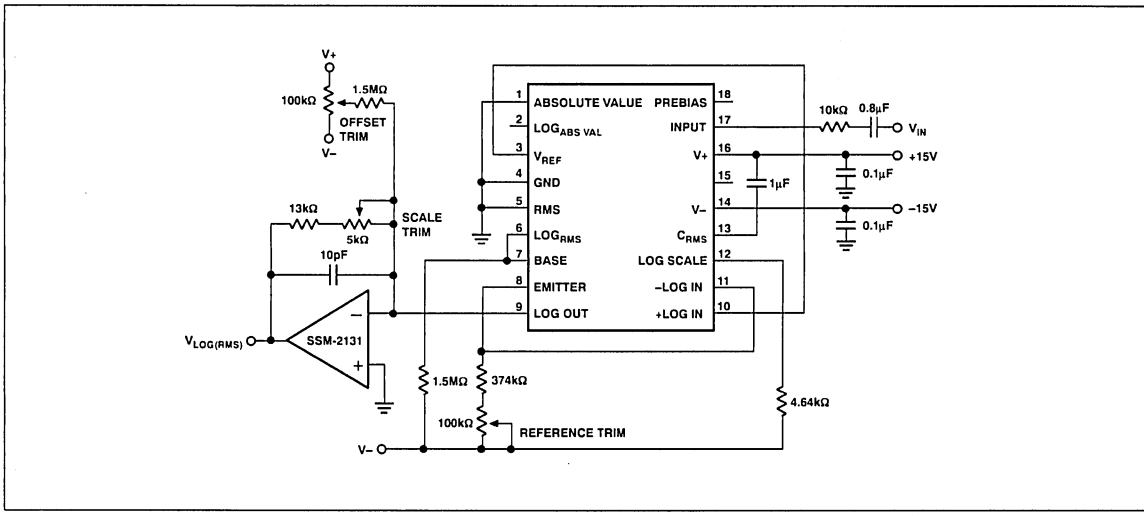


FIGURE 9: *Error Trimming*

ERROR TRIMMING

The offset, reference and scale factor trims (Figure 9) can be used to improve the overall accuracy of the device. The correct procedure for trimming out the various errors is as follows. First, +LOG IN (pin 10) and –LOG IN (pin 11) should be connected to V_{REF} (pin 3). The offset trim should be adjusted to achieve 0V at the $V_{LOG(RMS)}$ output. This nulls out any DC errors due to offsets in the log recovery amplifier. Second, reconnect the ±LOG IN pins as shown in Figure 9. Apply an input signal of $100mV_{RMS}$ ($10\mu A_{RMS}$). Adjust the reference trim to obtain 0V at the $V_{LOG(RMS)}$ output. This compensates for the input bias current of the log recovery amplifier and other errors. It sets the reference current to 10μA. Third, change the input signal to $1V_{RMS}$ ($100\mu A_{RMS}$). Adjust the scale trim to obtain 1.000V at the $V_{LOG(RMS)}$ output. This adjusts the scale factor to obtain 1V/20dB (50mV/dB). If other reference currents or scale factors are used then steps 2 and 3 will have to be changed accordingly.

This same procedure can be used for the log absolute value and log average absolute value configurations. If the log recovery amplifier is not used then the circuit in Figure 10 should be used to trim the offsets.

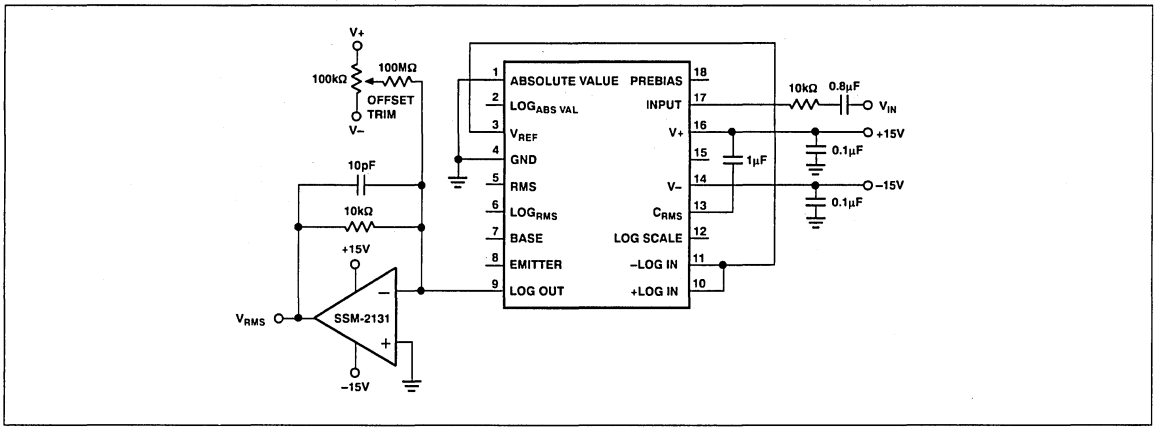
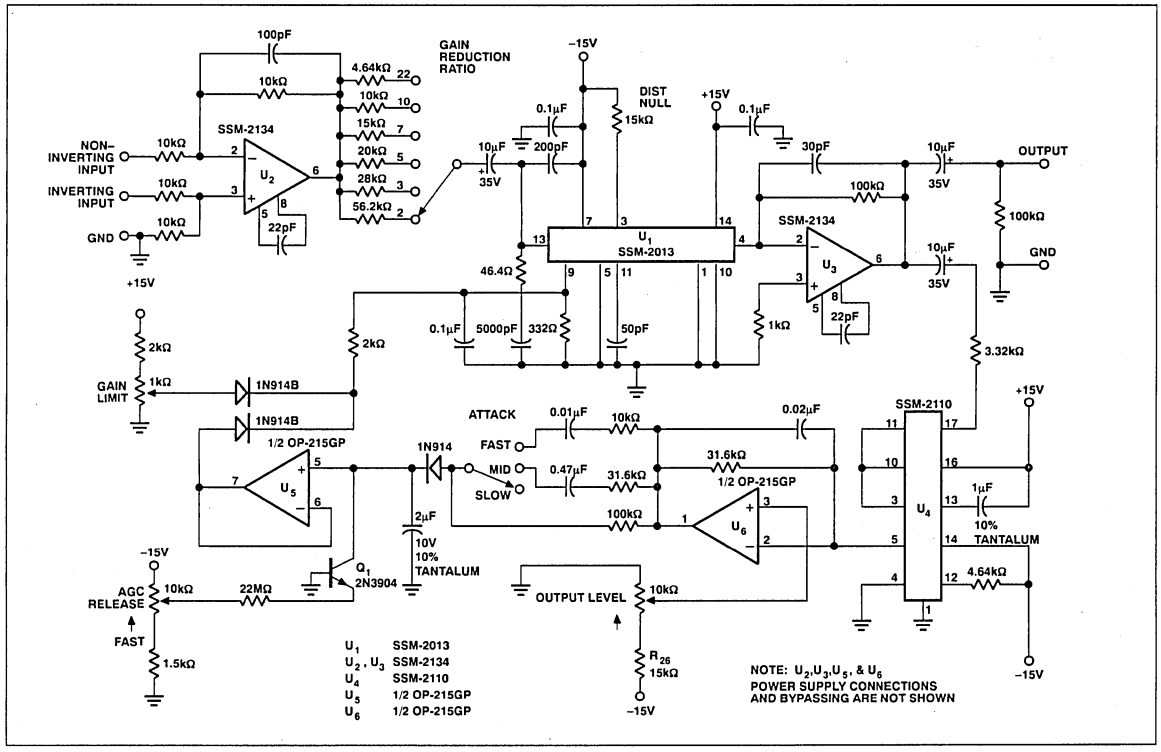


FIGURE 10: *Offset Trimming*

WAVEFORM	RMS	AVERAGE OF ABSOLUTE VALUE (A_{AV})	CREST FACTOR = $\frac{V_P}{RMS}$
V_P SINE WAVE	$\frac{V_P}{\sqrt{2}}$	$\frac{2 \cdot V_P}{\pi}$	$\sqrt{2} = 1.414$
V_P SQUARE WAVE	V_P	V_P	1
V_P TRIANGLE WAVE	$\frac{V_P}{\sqrt{3}}$	$\frac{V_P}{\sqrt{2}}$	$\sqrt{3} = 1.732$
$2V_P$ GAUSSIAN NOISE	RMS	$\sqrt{\frac{2}{\Pi}}$ x RMS	Typically varies from 1 to 6 depending on the characteristic of the noise. Theoretically, the crest factor is unlimited.

FIGURE11: *RMS, Average of Absolute Value and Crest Factors for Different Waveforms*



TYPICAL APPLICATIONS

AUTOMATIC GAIN CONTROL (AGC) AMPLIFIER

The automatic gain control amplifier shown below features selectable gain reduction compression ratios and time domain adjustable AGC attack and release. The design employs the SSM-2013 VCA, SSM-2110 true RMS-to-DC converter, two SSM-2134 low noise op amps and an OP-215 FET input op amp.

For additional information about this circuit, please see PMI application note AN-116.

PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

SSM-2044

4-POLE VOLTAGE-CONTROLLED FILTER/OSCILLATOR

FEATURES

- **Outstanding Frequency Control Range ...10,000 to 1 Min**
- **Stable Resonance Over Frequency Sweep**
- **Minimun External Parts Count**
- **High Control Rejection ...For 1000 to 1 Sweep 36dB Typ**
- **On-Chip Resonance Control**
- **Excellent Dynamic Range ..... 90dB Typ**
- **Gain Bandwidth..... 1MHz Typ**
- **Wide Supply Voltage Range ..... ±5V to ±18V**
- **Low Cost**

APPLICATIONS

- **Voltage Controlled Oscillators**
- **Anti-Aliasing and Reconstruction Filtering**
- **Medical Imaging and Ultra-Sound Systems**
- **Instrumentation and Sonar Systems**
- **Lower Noise Alternative to Switched-Capacitor Filters**

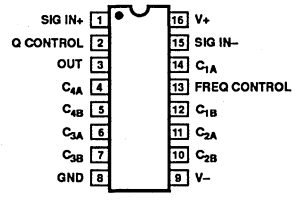
GENERAL DESCRIPTION

The SSM-2044 is a low cost 4-pole Voltage-Controlled Filter/Oscillator which has been designed as a –24/dB low-pass filter with a 10,000 to 1 variable cutoff frequency. The cutoff frequency is determined by a control voltage, making the device ideal for real-time analog filtering under microprocessor control.

A unique feature of the SSM-2044 is its on-chip resonance control, which can produce a low distortion sine wave for use in Voltage-Controlled Oscillator (VCO) applications.

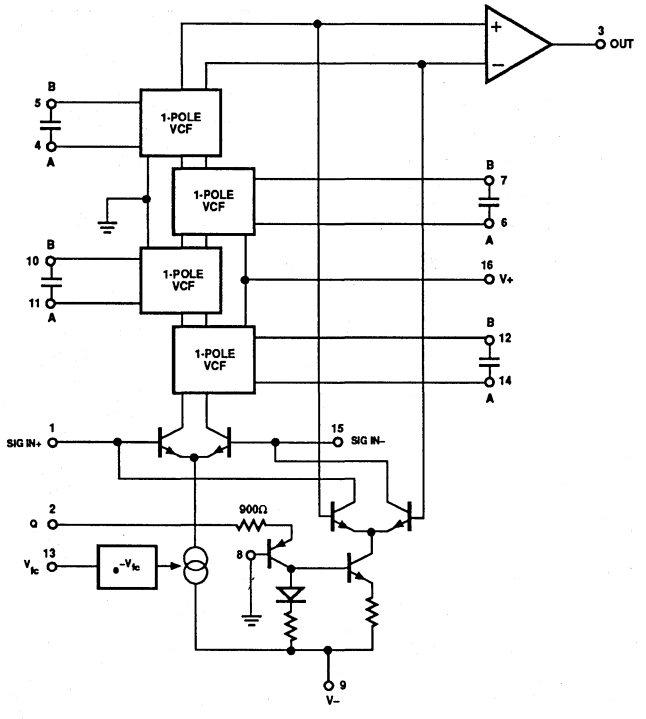
A novel filtering technique provides extended control range, low noise, and high control rejection of 36dB (Typ) for "pop"-free performance.

PIN CONNECTIONS



16-PIN PLASTIC DIP (P-Suffix)

BLOCK DIAGRAM



Manufactured under the following U. S. patent: 4,404,529

2/90, Rev. A1

The SSM-2044's dynamic range of 90dB (Typ) and gain bandwidth of 1MHz (Typ) make this device a good low noise alternative to switched-capacitor filters in a wide variety of applications, such as anti-aliasing and reconstruction filtering, medical/ultra-sound, instrumentation, and sonar systems.

The SSM-2044's performance and characteristics are guaranteed over the 0°C to +70°C temperature range and it is available in 16-pin epoxy DIP package.

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	
SSM2044P	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage ..... +18V
Negative Supply Voltage ..... –18V
Storage Temperature, P-Package ..... –55°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... +150C
Operating Temperature, P-Package ..... 0°C to +70°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Plastic DIP (P)	82	39	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted.

			SSM-2044			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Range	V+		+5	+15	+18	V
Negative Supply Range	V–		–5	–15	–18	V
Positive Supply Current	$I_{sy}+$	V_{fc} = 0V(Pin 13 to GND)	3.0	5.4	8.5	mA
Negative Supply Current	$I_{sy}-$	V_{fc} = 0V (Pin 13 to GND)	4.5	8.0	11.5	mA
Frequency Control Range			10,000:1	50,000:1	–	
Frequency Control Feedthrough		$\pm V_{IN}$ = 0V, –90mV ≤ V_{fc} ≤ +90mV	–	–36	–26	dB
Output Offset	I_O/I_{OMAX}	$\pm V_{IN} = V_{fc}$ = 0V	–	0.035	0.12	
Normalized Frequency	$f/f_{NOMINAL}$	Untrimmed	0.6	1	1.5	
Q Control Input Impedance	R_{INQC}	$V_{QC} \geq 0.7V$	675	900	1200	Ω
Q Current at Oscillation	I_{QOS}	–90mV ≤ V_{fc} ≤ +90mV	450	500	550	µA
Q Control Feedthrough			–	–30	–20	dB
Q Control Threshold Voltage	$V_{QC\ THRESHOLD}$		400	500	–	mV
Maximum Available Control Current	$I_{Q\ MAX}$	$V_{PIN\ 13}$ = –120mV	1.25	1.7	2.2	mA
Frequency Control Input Range	V_{fc}		–120	–	+180	mV
Maximum Output Signal Current	$I_{O\ MAX}$		±300	±400	±520	µA
Signal-to-Noise	S/N	Reference to $30mV_{P-P}$ (Pin 1 or 15)	–	70	–	dB
Gain Bandwidth			–	1	–	MHz

Specifications subject to change; consult latest data sheet.

APPLICATIONS INFORMATION

PRINCIPLE OF OPERATION

The SSM-2044 provides two major control functions controlled by two separate control input pins (pins 2 and 13). The voltage (V_{fC}) on the frequency control pin (pin 13) determines the cutoff frequency of the filter; the current (I_Q) sourced into the Q control (pin 2) determines the amount of the peaking in the filter frequency response by controlling the gain of the feedback amplifier.

Figure 1 shows the normalized amplitude vs. frequency for the SSM-2044 operating at a constant cutoff frequency for different Q or resonance settings. The overdamped curve is the response of the filter at minimum Q with a gradual rolloff approaching –24dB/octave at higher frequencies. As Q increases, the low frequency components are suppressed and the components near the cutoff frequency are emphasized. For all Q settings below oscillation, the final rolloff at high frequencies is –24dB/octave. At high Q settings, the filter will oscillate with a pure sinewave at the cutoff frequency. Oscillation will occur when the current into the Q control reaches approximately 500μA. (Figures 2 through 5 show the Square Wave resonance response vs. the Q-current.)

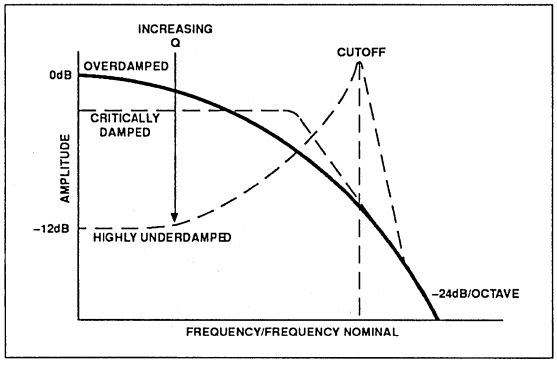


FIGURE 1: *Normalized Amplitude vs. Frequency Response*

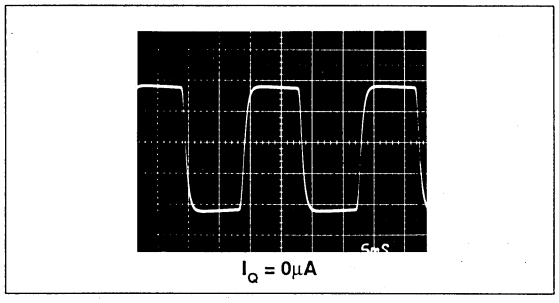


FIGURE 2

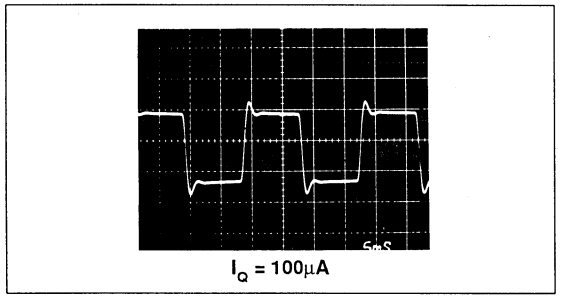


FIGURE 3

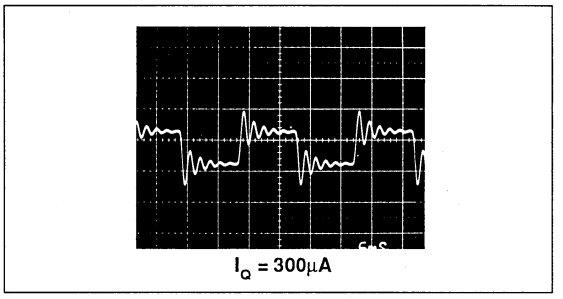


FIGURE 4

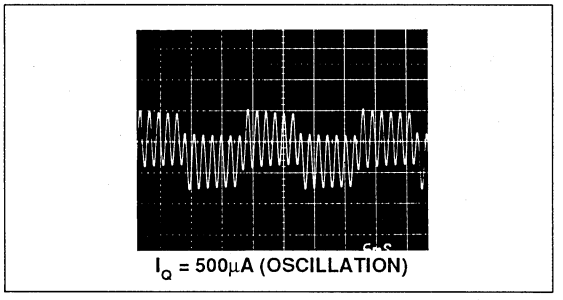


FIGURE 5

When Q = 0V, the feedback loop will be eliminated and the SSM-2044 will have a fourth-order transfer function with only one pole position. This will result in having all four poles on top of each other (see Figure 6).

As Q increases in the positive direction, the four poles of the SSM-2044 will be separated from each other and will travel in the direction shown in Figure 7. This will continue until the poles reach the imaginary axis. As previously stated, the oscillation will occur when the current into the Q control pin (pin 2) reaches approximately 500μA. This corresponds to +7.5V with the input resistors shown in Figure 11.

This oscillating waveform can be used as a tone source. The V/octave trim and the temperature compensation resistor (see Figure 11) are required in applications where the filter has to produce accurate musical intervals when in oscillation. If this is not necessary, the control op amp feedback network and the temperature compensation resistor can be replaced by 300kΩ and 1kΩ resistors respectively.

Figure 8 shows Q or resonance of a four-pole low-pass filter as a function of feedback or Q control current. The function changes very slowly with control current at the low end of the range but increases very rapidly as oscillation is approached. In applications where more precise control of the Q is desired, a "reverse-audio" taper pot can be connected to the Q control pin (pin 2) of the SSM-2044 (see Figure 9).

Combining the SSM-2044 with a "reverse-audio" taper pot will change the shape of the curve in Figure 8 to the one shown in Figure 10. By comparing the two graphs, it can be observed that when using the SSM-2044 by itself, the last 10 percent of the pot travel in the Q panel control will result in a 50 percent change in resonance. Using a "reverse-audio" taper pot in conjuction with the SSM-2044 will result in about 20 percent change in resonance for the same last 10 percent of pot travel.

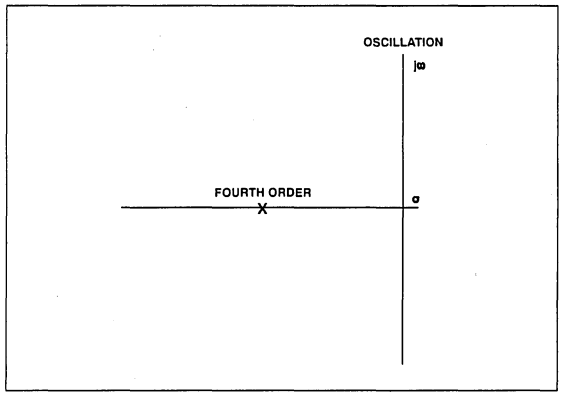


FIGURE 6: *Fourth-Order Transfer Function Q = 0V*

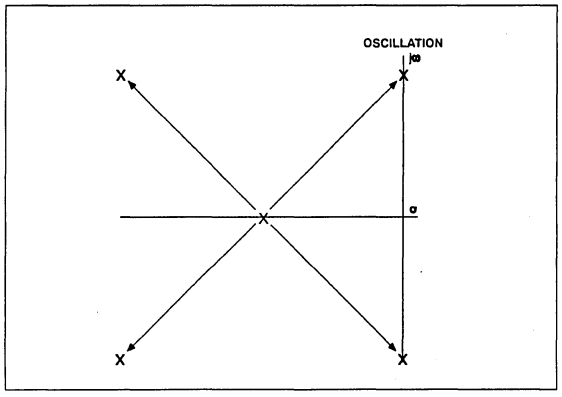


FIGURE 7: *Transfer Function as Q → Increasing*

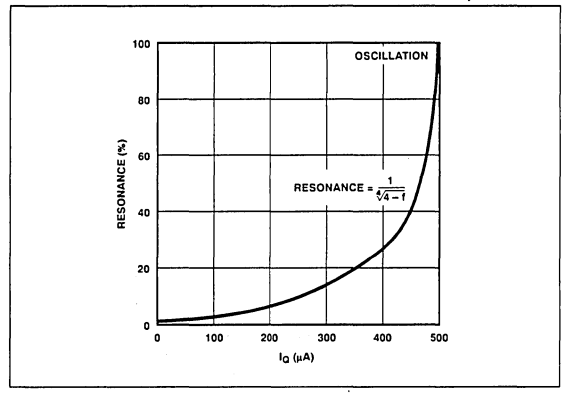


FIGURE 8: *Q-Control Transfer Curve*

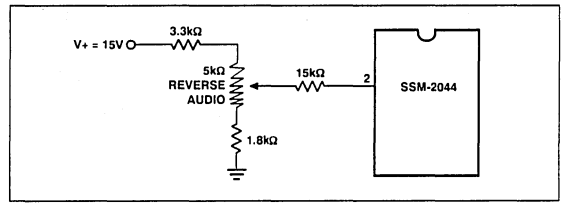


FIGURE 9: *"Reverse-Audio" Pot*

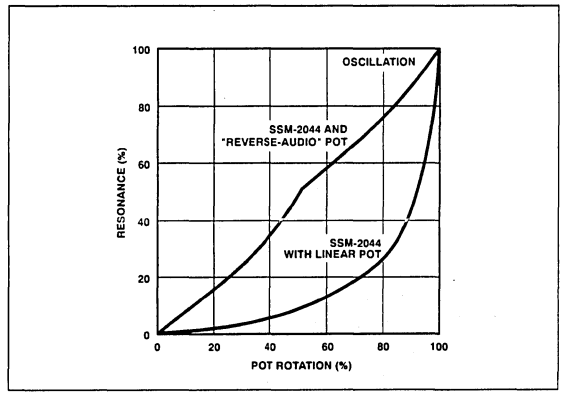


FIGURE 10: *SSM-2044 and "Reverse-Audio" Pot Transfer Curves*

In other words, the "reverse-audio" pot will help to reduce the Q panel control sensitivity before reaching oscillation.

TYPICAL CONNECTION

Figure 11 shows the typical connection of the SSM-2044 as a four-pole filter. The differential inputs will accept any signal(s) up to $\pm 18V_{p-p}$.

The control summer adds the voltages of various control sources such as f_c panel controls, transient generators, LFOs, etc. Any number of signals can be summed by applying them through resistors to the summing node of the op amp. The frequency offset adjust is required in polyphonic and programmable systems to make the filter(s) sound the same for identical input control voltages.

The frequency control pin (pin 13) should be terminated to ground through a resistor of 1kΩ or less. The combination of this resistor and the series resistor from pin 13 to a control voltage source form an attenuator that determines the frequency control scale factor which is about –18mV/octave at the pin. This attenuator will have a temperature drift of –3300PPM/°C. To offset this, a thermistor (in lieu of the 1kΩ resistor) with opposite drift characteristics should be connected from pin 13 to ground (for a possible thermistor source see Note 1). For best dynamic range, the control summer and the input attenuator should be designed so that the maximum swing at the SSM-2044's control pin corresponds to the extremes of the intended sweep range when the control summer is driven to the supplies. With the values shown in Figure 11, the voltage at the input pin will be ±90mV which corresponds to a 1000-to-1 sweep range for ±15V supplies.

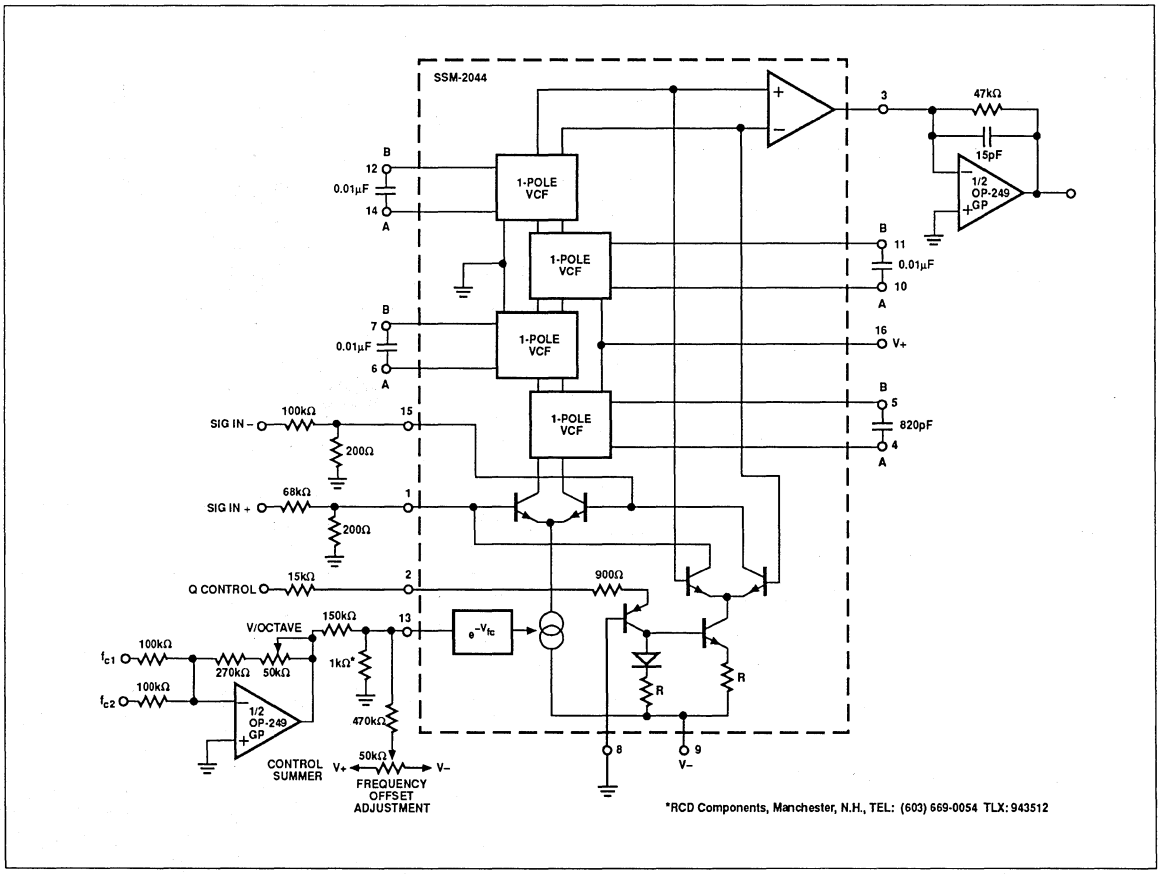


FIGURE11: *Typical Connection*

VOLTAGE CONTROLLED AMPLIFIER INTERFACE

Figure 12 shows the SSM-2044 is capable of driving a VCA's input without an intervening op amp. The 1µF capacitor provides a DC block so that the SSM-2044 offset will not affect the DC balance of the SSM-2024 VCA. With the connection shown in the Figure 12, an offset adjustment is not required to guarantee a worst case 30dB VCA control rejection.

The SSM-2024 Quad VCA is an excellent companion to the SSM-2044. The SSM-2024's channel specifications offer excellent performance in control mixers as well as a voicing VCA.

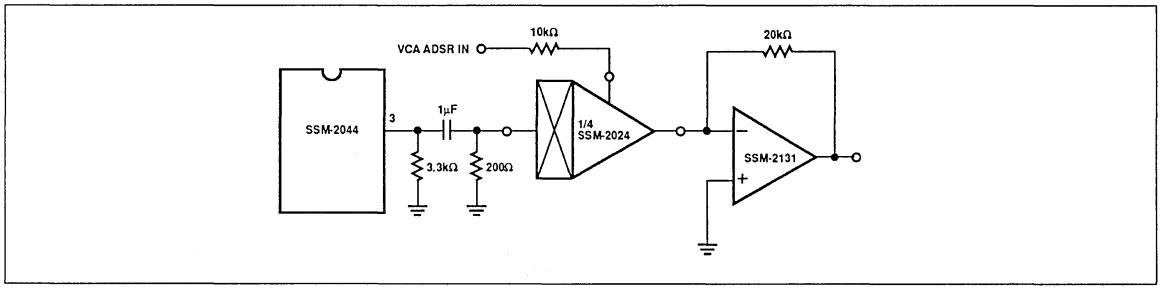


FIGURE 12: *VCA Interface*

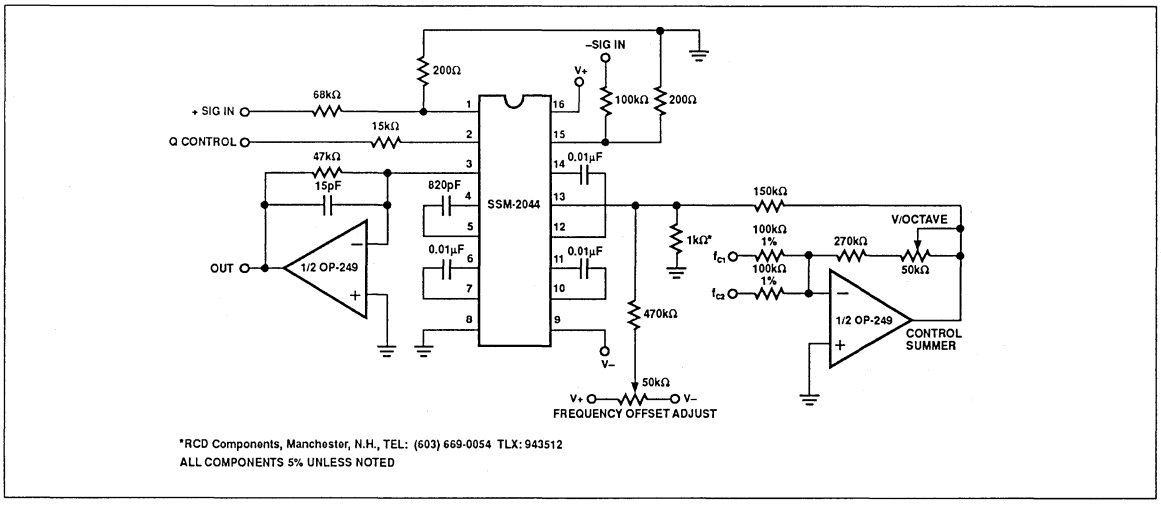


FIGURE 13: *Typical Connection for Breadboarding Purposes*

SSM-2045
VOLTAGE-CONTROLLED SIGNAL PROCESSOR

FEATURES

- 2-Pole and 4-Pole Low Pass Filter Outputs
- On-Chip Q Control, Mixer/VCA
- Low Offset
- Low Noise (80dB Below Nominal Signal Level)
- Low Control Feedthrough
- ±15 Volt Operation
- Separate Linear and Exponential Cross Fade Mixer Controls

APPLICATIONS

- Music Voicing Systems
- Audio Filtering
- Antialiasing Systems
- Voltage-Controlled Oscillators

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 18-PIN	
SSM2045P	0°C to +70°C

GENERAL DESCRIPTION

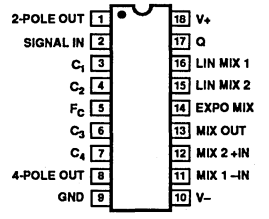
The SSM-2045 is a flexible, high performance building block which offers maximum options for active filter design. This monolithic device includes a voltage-controlled filter with 2-pole and 4-pole low pass outputs and an uncommitted mixer/VCA combination.

The filter section has exceptionally low noise, offset and control feedthrough delivering quality performance even in systems where the filter is not followed by a VCA. A voltage-controlled feedback amplifier gives built-in electronic Q control with a minimum amount of in-band loss at the oscillation point.

The mixer/VCA section can be connected to the filter input for waveform mixing or the outputs for mixing between the 2-pole and 4-pole responses. The two linear and exponential cross fade controls allow this circuit to be used both as a mixer and a VCA. This section has excellent offset, signal-to-noise and control feedthrough specifications. AC coupling between the filter and mixer/VCA is not required.

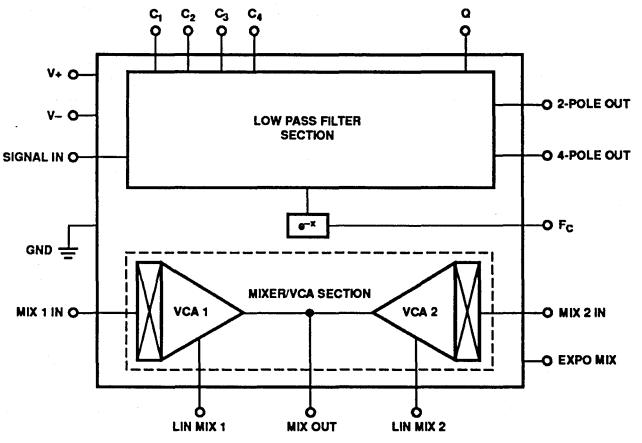
Continued

PIN CONNECTIONS



18-PIN PLASTIC DIP (P-Suffix)

BLOCK DIAGRAM



GENERAL DESCRIPTION *Continued*

Use in audio applications provides a "fat" open-loop type sound. Additional features such as a series voltage-controlled high pass filter can be designed using the VCF and onboard VCAs or by using the VCF with the SSM-2024.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage ..... +18V
Negative Supply Voltage ..... −18V
Storage Temp Range ..... −65° to +150°C
Lead Temp Range (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... +150°C
Operating Temp Range ..... 0°C to +70°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
18-Pin Plastic DIP (P)	70	30	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

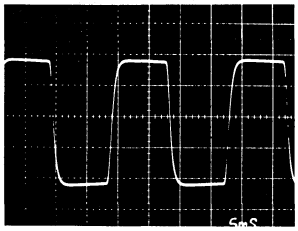
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

		SSM-2045			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FILTER SECTION					
Positive Supply Current		3.0	5.0	9.0	mA
Negative Supply Current	$V_{PIN\ 5}$ = GND, $I_{PIN\ 15-17}$ = 0 (Note 1)	5.0	6.5	7.1	mA
Output Offset (Pin 1)	$V_{PIN\ 5}$ = GND	−62.5	—	+62.5	mV
Output Offset (Pin 8)		−62.5	—	+62.5	mV
Change in Output Offset (Pin 1)	−90mV < $V_{PIN\ 5}$ < +90mV	−31.25	—	+31.25	mV
Change in Output Offset (Pin 8)	−90mV < $V_{PIN\ 5}$ < +90mV	−31.25	—	+31.25	mV
Signal Input Level (Pin 2)		—	150	300	mV_{p-p}
Signal Output (Pin 1, 8)		—	1	3	mV_{p-p}
Output Source Current (Pin 1,8)		5	10	15	mV
Output Sink Current (Pin 1, 8)		600	750	900	µA
Frequency Control Range		1000:1	5000:1	—	
F_C Input Bias Current (Pin 5)		—	1.0	2.5	µA
F_C Scale Factor Drift		—	−3300	—	ppm/°C
F_C Control Sensitivity (Pin 5)		−20	−19.3	−18.7	mV/OCTAVE
Q Current Required for Oscillation (Pin 17)		120	150	185	µA
Dynamic Range	$V_{PIN\ 5}$ = −90mV (Filter Wide Open)	—	92	—	dB
In Band Distortion (THD) ($4F_{IN} \leq F_C$)	At $150V_{p-p}$ IN	—	0.1	—	%
Max Distortion (THD) ($F_{IN} = F_C$)	At $150V_{p-p}$ IN	—	1.0	—	%
MIXER/VCA SECTION					
Output Offset Current	$V_{PIN\ 11} = V_{PIN\ 12} = V_{PIN\ 14}$ = GND $I_{PIN\ 15}$ = 500µA, $I_{PIN\ 16}$ = 0 or $I_{PIN\ 16}$ = 500µA, $I_{PIN\ 15}$ = 0	−12.5	—	+12.5	µA
Output Leakage	$I_{PIN\ 15} = I_{PIN\ 16} = 0$	−1	—	+1	nA
VCA Gain	$I_{PIN\ 15} = I_{PIN\ 16}$ = 500µA $I_{PIN\ 14}$ = GND	3842	4085	4330	µmhos
VCA Gain Matching		−0.5	—	+0.5	dB
Mix Expo Input Bias Current (Pin 14)	$I_{PIN\ 15}$ = 500µA, $I_{PIN\ 14}$ = GND	−50	—	−5	µA
Control Rejection (Untrimmed)	RE $40mV_{p-p}$ (Pin 11 or 12)	—	41.5	30	dB
Signal-to-Noise Ratio	RE $40mV_{p-p}$ (Pin 11 or 12)	—	82	—	dB
Distortion	$40mV_{p-p}$ (Pin 11 or 12)	—	0.3	—	%

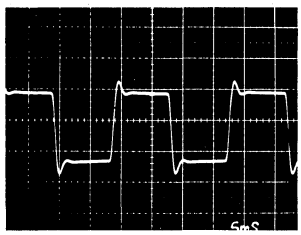
NOTE:
1. Resistor in series with pin 10 required for negative voltage supply voltage ≤ −6.8V.

Specifications subject to change; consult latest data sheet.

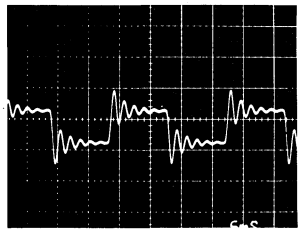
Q CONTROL CHARACTERISTICS



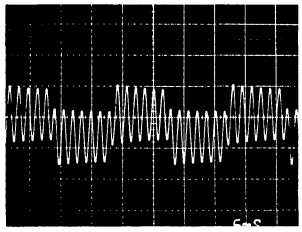
I_Q = 0μA



I_Q = 50μA

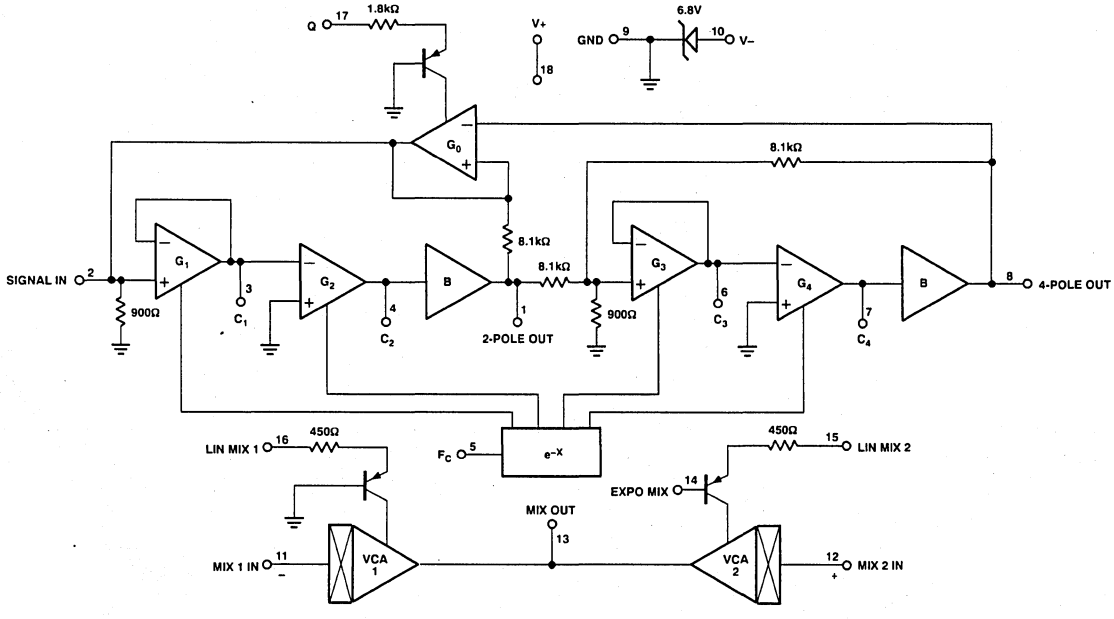


I_Q = 100μA



I_Q = 150μA (Oscillation)

FUNCTIONAL DIAGRAM



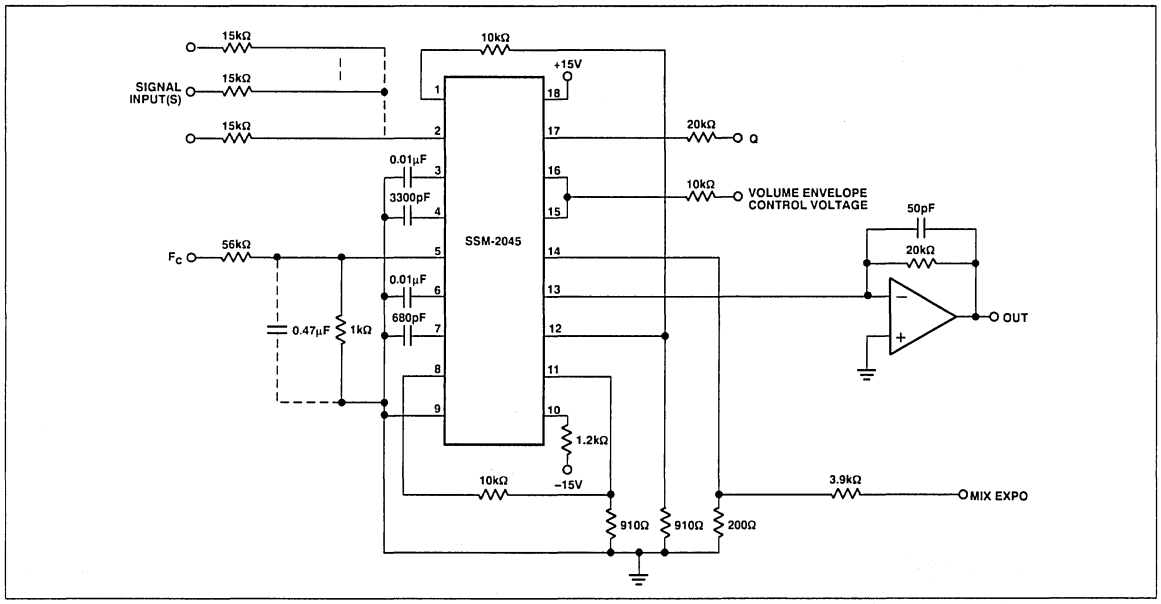


FIGURE 1: *SSM-2045 Typical Connection*

TYPICAL CONNECTION

Figure 1 shows a typical connection of the SSM-2045. The inputs of the Mixer/VCA are connected to the 2- and 4-pole outputs of the filter section. This allows the relative amount of the two low pass responses to be placed under program control via the expo mix control. The envelope is applied to the two linear mix controls. This determines the overall volume at the final output.

FILTER SECTION

The signal input has an input impedance of 900Ω and accepts a nominal input signal of 150mV$_{p-p}$. Higher signal levels can be used if the increased distortion is compatible with the desired sound. Signals can be summed at the input using a resistor network, the on-chip mixer/VCA or a multiple VCA IC such as the SSM-2024.

The frequency control input (pin 5) can vary the cutoff frequency over a 5000:1 range. Usually the sweep is restricted to 1000:1 which corresponds to ±90mV at the pin. With the input attenuator shown in Figure 1, the F_G control sensitivity is about −1 octave per volt. For best control rejection, a time constant of approximately 500µs should be established to limit rapid voltage changes either at the input pin or in the preceding control summer.

The frequency control pin (pin 5) should be terminated to ground through a resistor of ≤1kΩ. A series resistor from pin 5 to a control voltage source and the ground connected resistor form an input attenuator that determines the frequency control scale factor which is approximately −18mV/octave at the pin. This has a temperature drift of 3300ppm/°C. A tempsistor with similar drift to the ground connected ground resistor can minimize drift effect (see note).

The output can source more than the 10mA and sink approximately 750µA. Resistors can be connected from the outputs to the negative supply to increase sink current capability. The 2-pole output is inverted with respect to the 4-pole output.

The signal-to-noise ratio of the filter section is 84dB for 150m V$_{p-p}$ at the signal input pin which allows for more than 6dB of headroom. The worst case control feedthrough referred to this signal level is −32dB, 12dB better than conventional designs.

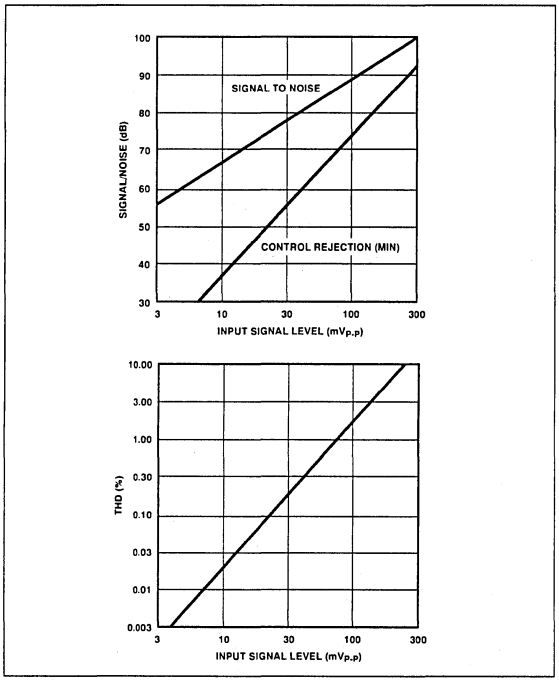
MIXER/VCA SECTION

This section is completely independent of the filter circuit allowing it to meet a variety of system requirements. First, it can be used as both a VCA and as a cross fade control between the 2-pole and 4-pole filter outputs. It can also be used in a similar manner as a volume contour VCA and to mix tone sources to the filter input. With most filters, placing the volume VCA before the filter would be unacceptable as the VCA as a follower is used to mask the filter background noise and control feedthrough. However, the filter specifications of the SSM-2045 will allow this configuration. For designs with more than two sources, a third oscillator or noise generator for example, the additional signals can be mixed or switched to the filter input using simple resistor summing, CMOS transmission gates or the SSM-2024.

The impedance from the signal inputs of the VCAs to ground should be approximately 910Ω for the best offset and control rejection performance. The overall performance of the VCAs with respect to signal-to-noise ratio, control rejection and distortion vs. input signal level is identical to the SSM-2024.

Note: RCD Components, Manchester, N.H. USA, Telephone: (603) 669-0054 TLX: 943512

MIXER/VCA PERFORMANCE



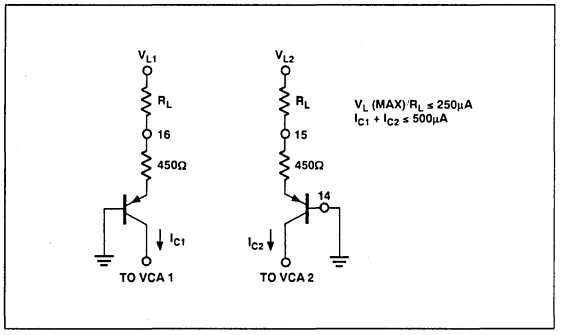


FIGURE 3

A series voltage-controlled high pass filter can also be made with this section (Figure 2a). Figure 2b shows a similar circuit using one section of the SSM-2024. The input signal level of these two circuits must be no more than 500mVp-p unless padded as shown. The output level can be set by scaling R_3 - R_5.

The controls of the Mixer/VCA section offer maximum flexibility as several control configurations and response characteristics are possible. Figure 3 shows both the VCA inputs connected for linear control. A VCA will be completely off when corresponding input control voltage is within 500mV of ground. The series resistor to linear control input should be chosen to give < 250µA at the maximum control voltage.

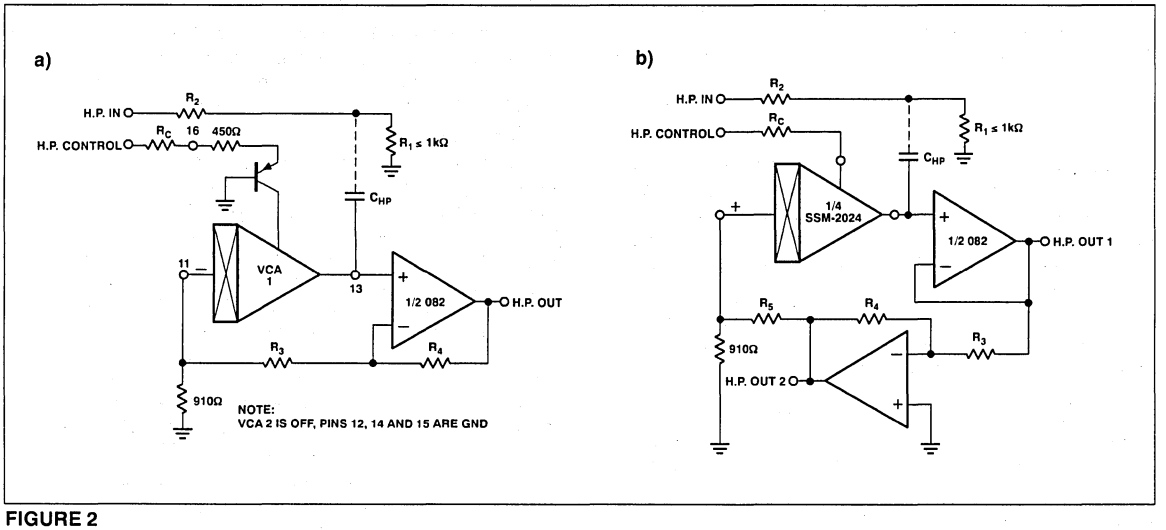


FIGURE 2

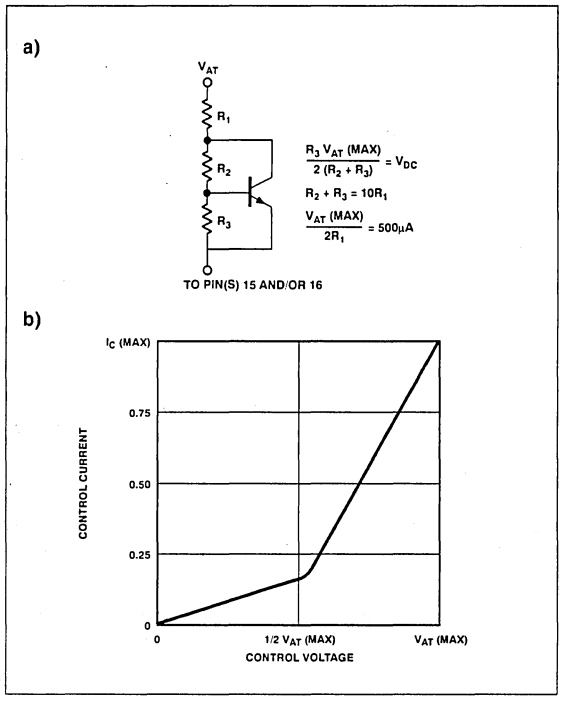


FIGURE 4

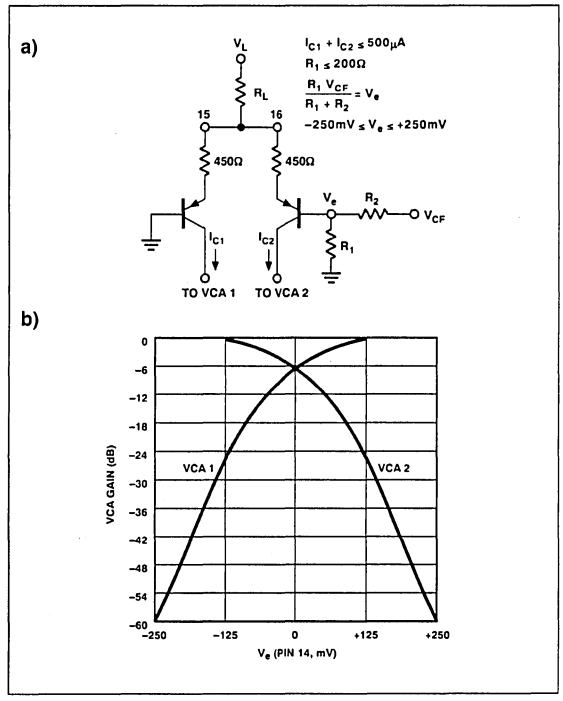


FIGURE 5

Figure 4a shows a circuit that can be added in series with a linear control input to give an audio taper control response. The network around the transistor is desired so the the impedance seen by the control voltage decreases by a factor of ten when the control voltage exceeds half its maximum value. At this point, the transistor turns on and almost all additional control passes through the transistor. Figure 4b shows the approximate control characteristic of the circuit.

The control for the combined linear and exponential cross-fade control is given in Figure 5a. This circuit splits a common linear control current between two VCAs according to the transfer characteristics of a differential input pair. An envelope generator can be applied to the common generator linear input to control overall volume contour while the relative amount of the two signals of the VCAs in the mix is determined by the voltage on pin 14. The characteristic of this control is shown in Figure 5b.

If cross-fade control is desired, a resistor can be connected to the common linear control from the positive supply to give a current of 500μA or less.

POWER SUPPLIES

The SSM-2045 is designed to give best overall performance when operated from ±15 volt supplies. Supply voltages down to ±5V can be accommodated with increasing degradation of some specifications, notably VCA offset and control feedthrough. The negative supply can be any value below –5V with no change in performance. A –5V supply can be connected directly to pin 10. For a negative supply voltage below –6.8V, a series resistor is used with a value determined by the following equation:

$R_{LIMIT} = (V_{ee} - 6.8)/7.1mA$ for $V_{ee} < -6.8V$

CALCULATING THE SSM-2045 FILTER RESPONSE CHARACTERISTIC

Example: Butterworth Rolloff Characteristic

Each 2-pole section in the SSM-2045 obeys the generalized 2-pole low pass transfer function:

$$\frac{V_{OUT}}{V_{IN}} = H(s) = \frac{H_\varnothing \omega_\varnothing^2}{s^2 + \alpha \omega_\varnothing s + \omega_\varnothing^2}$$

where $\omega_\varnothing 2\pi = f_{CUTOFF}$ and $\alpha \equiv \frac{1}{Q}$

Deriving for the SSM-2045 gives the following:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-g_m^2/(C_1\, 10\, C_2)}{S^2 + s\, g_m/C_1 + g_m^2/(C_1\, 10\, C_2)}$$

Comparing the generalized equation with the equation for the SSM-2045 we have:

$$H_\varnothing = -1,\ \omega_\varnothing = \frac{g_m}{\sqrt{C_1 10 C_2}} \text{ and } \alpha \equiv \frac{1}{Q} = \frac{\sqrt{C_1 10 C_2}}{C_1}$$

These last two equations allow calculation of the capacitor values for a desired transfer characteristic. Note that C_2 behaves as if it were 10 times its actual value. This is due to the gain of 10 in the second and fourth filter stages.

DESIGN EXAMPLE

The principle application of the SSM-2045 is a low pass filter with 2- and 4-pole outputs. If a Butterworth (maximally flat) rolloff characteristic with no feedback ($I_Q = 0$) is desired as the final 4-pole output, filter design tables would show:

$\omega_{\phi 1} = \omega_{\phi 2}$, $\alpha 1 = 1.85$ and $\alpha_2 = 0.765$

So the first 2-pole section would be overdampened and the second would be underdampened. Choosing $C_1 = 0.01\mu F$ we find:

$C_1 = 0.01\mu F$, $C_2 \approx 3300pF$, $C_3 \approx 0.024\mu F$, $C_4 \approx 1500pF$

This does produce a system with the correct response, however, performance under feedback is poor because of the high feedback gain required for oscillation. If $\omega_{\phi 1}$ is increased by approximately an octave and we recalculate:

$C_1 = 0.01\mu F$, $C_2 \approx 3300pF$, $C_3 \approx 0.01\mu F$, $C_4 \approx 680pF$

This yields a system with excellent sonic quality. The onset of oscillation with increasing feedback is smooth and well controlled. Also, the oscillation amplitude with a given feedback is nearly constant over the audio band as the frequency is swept.

TYPICAL APPLICATION

Figure 6 shows an application using two SSM-2045 Mixer/VCA sections which in addition to providing the basic dual VCA function, also positions the two sound sources in the left-right stereo image field under voltage control. Signal 1 and Signal 2 amplitude are the overall linear VCA gain control ports while the Signal 1 and Signal 2 Pan inputs control the relative amount of signals appearing in the two output channels. Note that each sound source can be both separately enveloped and positioned. Each half section works as described for the linear-exponential crossfade circuit shown in Figures 5a and 5b.

The Signal 1 and Signal 2 inputs can be connected to the outputs of the SSM-2045 filter sections in the two ICs. This scheme can easily be extended to any polyphonic music system having any multiple of two voices. In such a system, all the left and all the right current outputs can be connected together to the virtual ground inputs of the two op amp current-to-voltage converters. Note that since the left and right VCA inputs are inverted for each signal, one of the final outputs, either left or right, should be inverted to avoid phase cancellation.

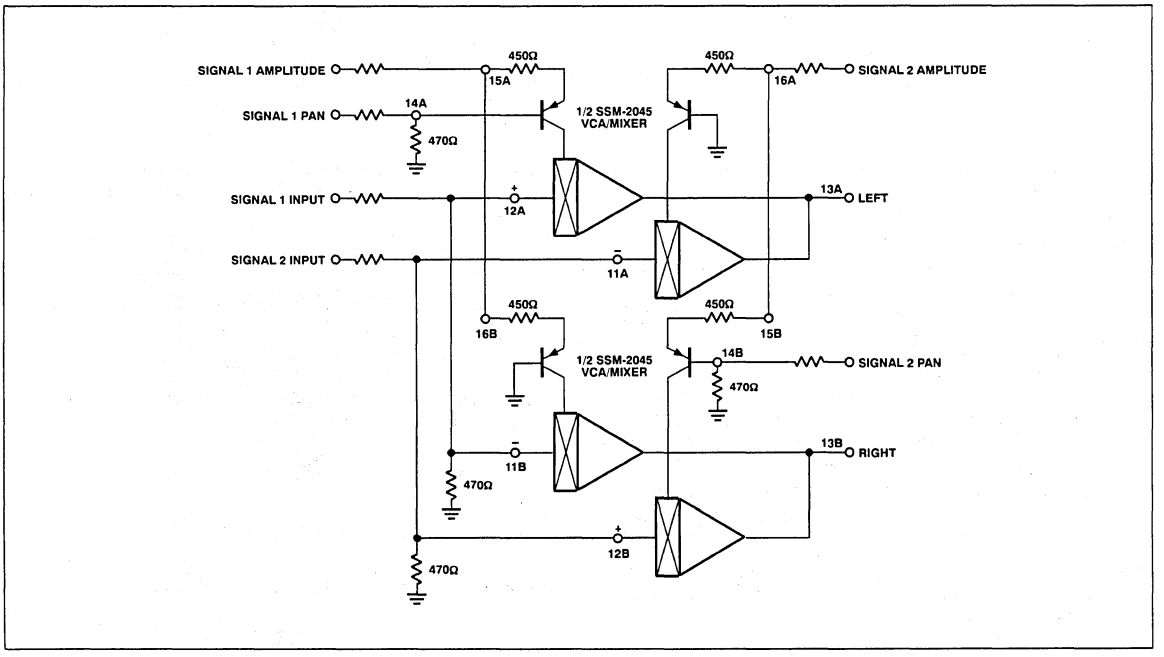


FIGURE 6: *Dual VCA/Stereo Panning Circuit*

PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

SSM-2047

VOLTAGE-CONTROLLED FILTER WITH TRIPLE VCAs

FEATURES

- 4 Pole Low-Pass Filter and On-Board Parallel Output VCAs
- 92dB VCF Dynamic Range
- Low Distortion VCF and VCAs
- Low Control Feedthrough
- Full Class A Signal Path
- dB/Volt Master Gain and Pan Controls

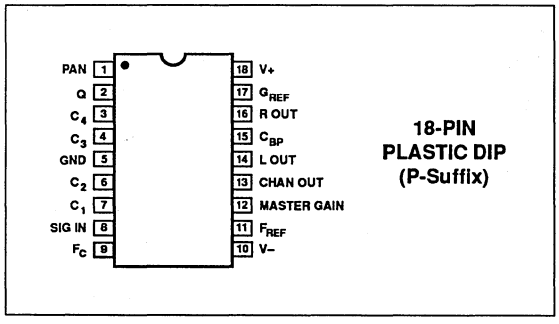
APPLICATIONS

- Digital Audio Systems
- Antialiasing and Reconstruction Filters
- Flight Simulators
- Sound Effects

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 18-PIN	
SSM2047P	0°C to +70°C

PIN CONNECTIONS



18-PIN
PLASTIC DIP
(P-Suffix)

GENERAL DESCRIPTION

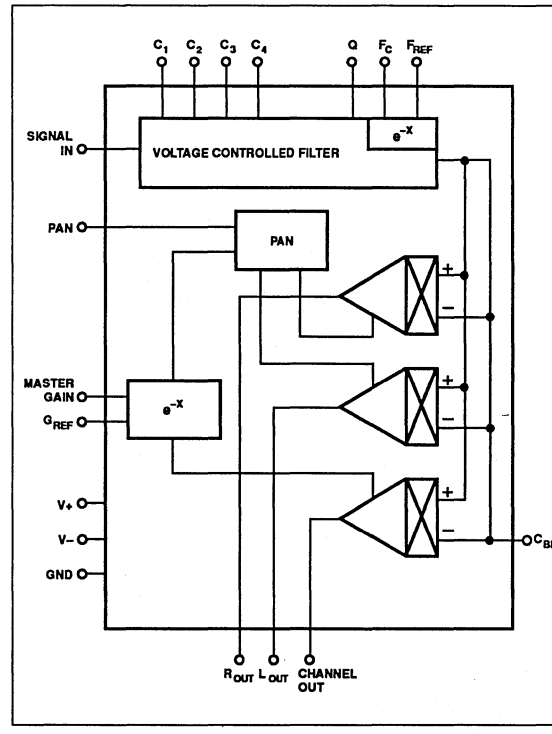
The SSM-2047 is a dedicated signal processing array designed to conform to the demands of state-of-the-art systems. Provided on-chip is a four pole low-pass voltage-controlled filter and three output VCAs which feature individual channel as well as mixable left and right independent outputs.

The filter section has been designed for low distortion, wide dynamic range and low offset. A voltage-controlled feedback amplifier gives built-in electronic Q (resonance) control with a minimum of in-band loss at the oscillation point.

The output VCAs are low control feedthrough, full Class A devices connected in parallel rather than in series for less noise and distortion build up.

The master gain and stereo pan pins have exponential (dB/volt) control characteristics. Unit-to-unit frequency and amplitude variability is reduced by external reference resistors.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage ..... +18V
Negative Supply Voltage ..... −18V
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... +150°C
Operating Temperature Range ..... 0°C to +70°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
18-Pin Plastic DIP (P)	70	30	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

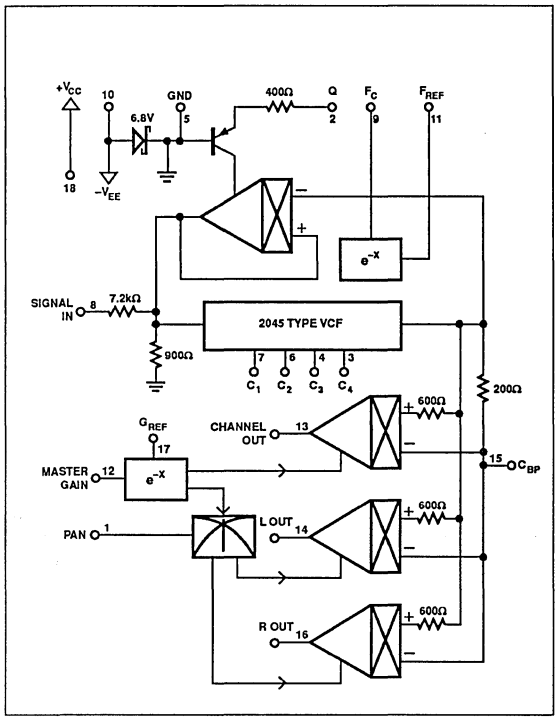
ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted.

		SSM-2047			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Current	$V_{PIN\ 9} = V_{PIN\ 12} = GND$	8.5	10.2	11.5	mA
Negative Supply Current	$V_{PIN\ 9} = V_{PIN\ 12} = GND$	6.5	8.15	9.8	mA
Filter Section @ $I_{F\ REF} = 10\mu A$ Signal Input Level (Pin 8)		–	1.35	2.7	V_{p-p}
Input Impedance (Pin 8)		6.56	7.2	9.84	kΩ
Output Offset (Pin 15)		–	+5	+15	mV
Frequency Control Feedthrough (Pin 15)	$-90mV \le V_{PIN\ 9} \le 90mV$ (Note 2)	–	−36	−28	dB
Frequency Control Range (Pin 9)		–	12	14	Octaves
Center Frequency Variability	$V_{PIN\ 9} = GND$	0.92	1.00	1.08	F/F nom
F_C Input Bias Current (Pin 9)	$V_{PIN\ 9} = GND$	–	1.25	2.5	µA
Frequency Control Sensitivity (Pin 9)		−20	−19.3	−18.7	mV/Octave
F_C Scale Factor Drift		–	−3300	–	ppm/°C
Q Current Required for Oscillation (Pin 2)		40	75	100	µA
Q Control Feedthrough (Pin 15)	$0 \le I_Q \le 60\mu A$ (Note 2)	–	−26	−16	dB
Dynamic Range (Clipping to Noise Floor)	$V_{PIN\ 9} = -90mV$	–	92	–	dB
In-Band Distortion $4F_{IN} < F_C$		–	0.1	–	%
Max Distortion $F_{IN} = F_C$		–	1.0	–	%
Output VCAs @ $I_{G\ REF} = 300\mu A$ Max VCA Gain (Pins 13, 14 and 16)	$V_{PIN\ 12} = 0V$ $V_{PIN\ 1} = +300mV$ or $-300mV$	2250	2450	2650	µmhos
Output Leakage (Pins 13, 14 and 16)	$V_{PIN\ 12} = +400mV$	−1	–	+1	nA
Left-Right Gain Matching (Pins 14, 16)	$V_{PIN\ 1} = V_{PIN\ 12} = GND$	−0.5	–	+0.5	dB
Gain Control Input Bias Current (Pin 12)	$V_{PIN\ 12} = 0V$	–	1.0	–	µA
Pan Control Input Bias Current (Pin 1)	$V_{PIN\ 1} = 0V$	–	0.5	–	µA
Control Feedthrough	(Note 2)	–	−41.5	−30	dB
Signal-to-Noise	(Note 2)	–	82	–	dB
Distortion	(Note 2)	–	0.3	–	%

NOTES:
1. Resistor in series with pin 10 required for $V - < -6.8V$. Due to internal zener diode between pin 10 and ground, negative supply voltages between −6V and −9V should be avoided.
2. These specifications are referred to a $1.8V_{p-p}$ signal into pin 8.

Specifications subject to change; consult latest data sheet.

FUNCTIONAL DIAGRAM



FILTER SECTION

The filter section of the SSM-2047 is similar in design and performance to that of the SSM-2045. The primary difference is a reduced output voltage swing since it is not brought out directly. This dictates different C_2 and C_4 than those used with the SSM-2045 (see Typical Connection Diagram).

The SSM-2047 has a 7.2kΩ input attenuator resistor internal to the device. The input (pin 8) referred clip point is approximately $2.7V_{p-p}$. The maximum input signal should be kept a few dB below this value. The frequency control (pin 9) should be terminated to ground through a resistor of 1kΩ or less. A series resistor from pin 9 to a control voltage source and the ground connected resistor form an input attenuator that determines the overall frequency control scale factor. The scale factor is approximately –19.3mV/octave at pin 9. This will have a temperature drift of –3300ppm/°C unless a tempsistor with opposite drift is used as the ground connected resistor (see note below).

The Q control has been designed to give only a 6dB in-band signal loss at the oscillation point. This slight loss will keep headroom nearly constant as Q is increased. The Q control input (pin 2) is the emitter of a grounded base PNP transistor through a 400Ω short-circuit protection resistor. The onset of sine wave oscillation will occur with about 75µA sourced into pin 2. An external series resistor is usually connected from pin 2 to the Q control voltage source.

OUTPUT VCAs

Three output VCAs are provided: channel and left-right stereo. These are connected in parallel rather than series for less noise and distortion build up. The inputs of the VCAs are internally connected to the filter output. Pin 15 has been provided for a capacitor which effectively acts as a DC block between the filter and the VCAs. This prevents any filter offset voltage from degrading the control rejection performance of the VCAs. The gain control (pin 12) controls the gain of all three VCAs. The control sensitivity is about –10dB/30mV at pin 12. A control attenuator is usually connected between pin 12 and the gain control source.

The pan control (pin 1) determines the relative amount of signal that will appear in the left-right stereo outputs. The sum of the signals in the two outputs is constant. The control sensitivity rapidly approaches –10dB/30mV away from center in the output being attenuated. Again, an external control attenuator is usually provided from the pan control voltage source to the pan pin. It may be desirable to remove the signal from the stereo mix when the channel output is in use. This can be accomplished with a switch on the channel jack connecting the positive supply to a resistor which goes to the control attenuator at the pan pin. The resistor's value should be chosen to give about +1.5V at pin 1 when it is connected to the supply.

The VCAs all have current outputs. This allows signal summing by simply connecting the appropriate outputs of multiple SSM-2047s to a single op amp current-to-voltage converter. The voltage compliance of the outputs is ±330mV. However, the output(s) can also be connected to a small resistor to ground.

GENERAL INFORMATION

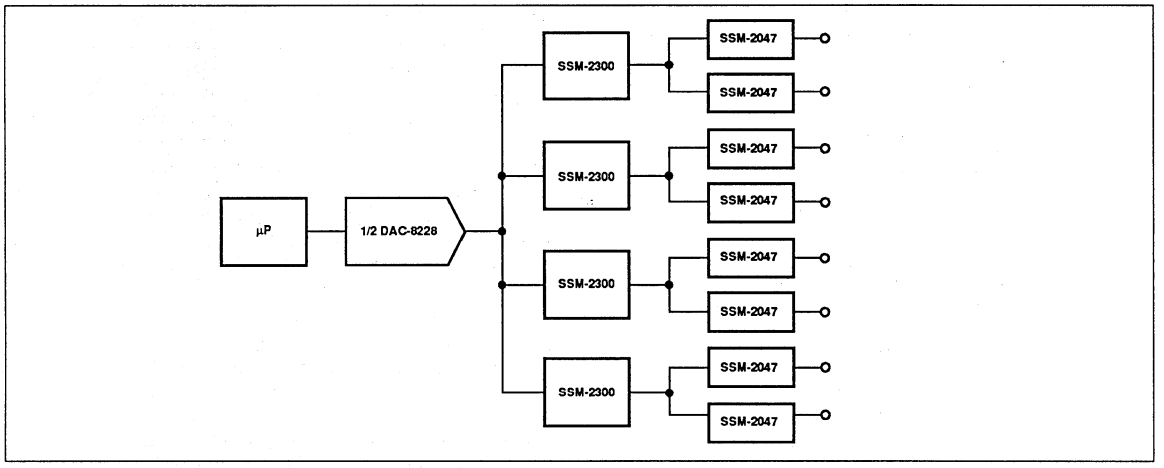
The SSM-2047 will operate with positive supply voltage in the range from +9 to +18 volts. Due to the internal zener diode connected between ground and pin 10, a resistor in series with pin 10 to the negative supply must be included for negative supplies below –6.8 volts. The resistor's value is determined by the equation:

$R_S = | 6.8 + V_{EE} | /9.8mA$ for $V_{EE} < -6.8V$

A –5 volt supply can be connected directly in pin 10. Negative supply voltages less than –6 volts or greater than –9 volts are recommended.

The SSM-2047 requires two external resistors to establish the filter center frequency and the maximum gain of the output VCAs. The voltage at pin 11, the filter reference current pin, is 2.5 volts above ground. The resistor between this pin and the negative supply or pin 10 should establish a 10µA current source. Pin 17's voltage is a few hundred millivolts below ground. The resistor between this pin and the negative supply or pin 10 will produce a current that determines the maximum gain of the ouput VCAs. This current should be no more than 300µA for optimum performance. If the negative supply is lower than the voltage on pin 10, connecting the resistors to V– will establish currents with greater accuracy. However, the supply should be well regulated and free of noise. If this is not the case, the resistors and the bypass capacitor should be connected to pin 10.

NOTE: RCD Components LP1/4, Manchester, NH U S A TEL: (603) 669-0054

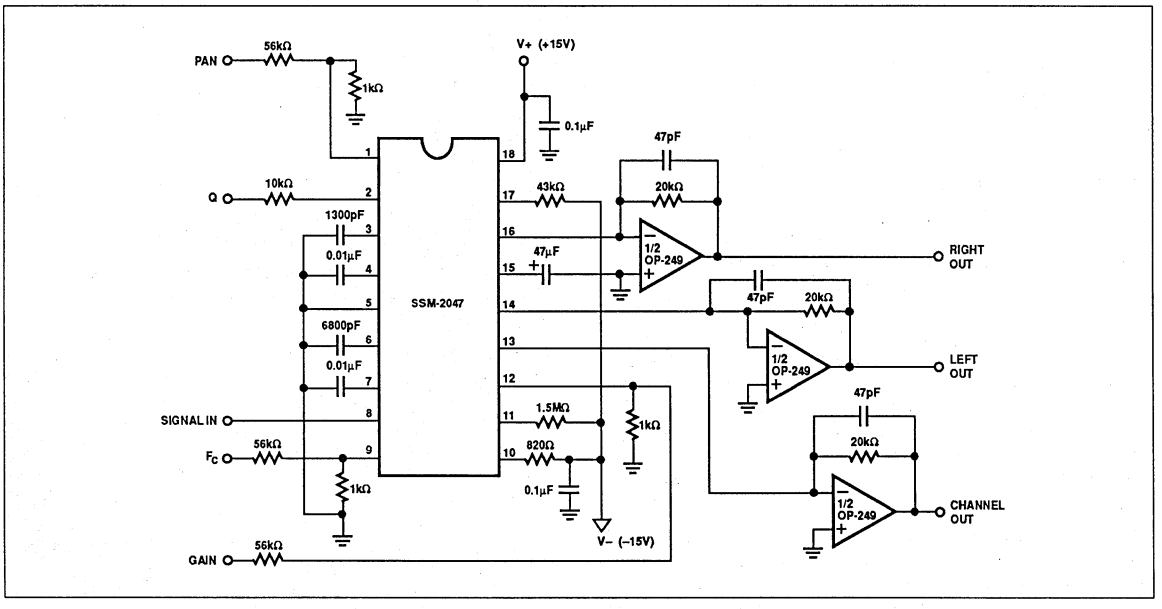


BLOCK DIAGRAM: 8-Channel System Using 8-Bit CMOS DAC, 8-Channel Demultiplexers, VCFs/VCAs.

TYPICAL CONNECTION OF THE SSM-2047

The figure below shows a typical connection of the SSM-2047 powered from ±15V supplies. The 43kΩ and 1.5MΩ resistors establish the 300µA and 10µA current references for VCA gain and filter center frequency respectively. Note that the negative supply should be well regulated and free of noise or the resistor values should be scaled and the connections moved to pin 10 with the bypass capacitor.

SSM-2407 TYPICAL CONNECTION



PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

SSM-2100
MONOLITHIC LOG/ANTILOG AMPLIFIER

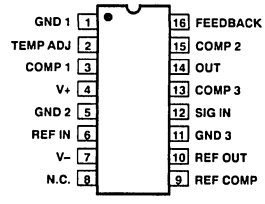
FEATURES
- Performs Log, Antilog, and Log Ratio Functions
- 50pA Input Bias Current (Trimmed)
- 4mV Input Offset Voltage
- On-Board Reference
- Temperature Stabilized
- 25ppm/°C Reference Drift
- 30ppm/°C Scale Factor Drift
- 0.25% Conformance
- 3-Decade Dynamic Range (Voltage Mode)
- 6-Decade Dynamic Range (Current Mode)
- Low Cost

APPLICATIONS
- Photodiode Preamplifier
- Absorption Measurement
- Low Sweep Generators
- High Resolution Data Acquisition
- Analog Computation Circuits
- Analog Compression/Expansion
- Linear-to-dB Conversion

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	
SSM2100P	–10°C to +55°C

PIN CONNECTIONS

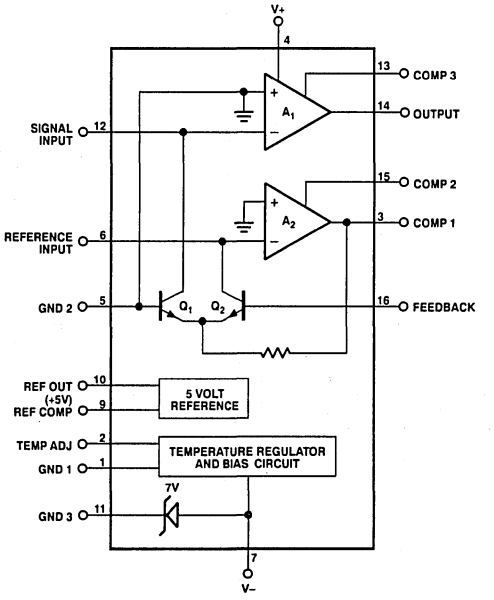


16-PIN PLASTIC DIP
(P-Suffix)

GENERAL DESCRIPTION

The SSM-2100 is a monolithic low-cost DC logarithmic amplifier capable of implementing log/antilog as well as log ratio transfer functions. This device offers a dynamic range of 6 decades of current and 3 decades of voltage. The circuit contains two precision operational amplifiers, a high conformance transistor pair and a precision bandgap voltage reference. An on-board substrate temperature regulator stabilizes both the scale factor and reference drift. A negative voltage reference is also available to facilitate external trimming.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 36V or ±18V
Junction Temperature ..... +150°C
Operating Temperature Range ..... –10°C to +55°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Current into Any Pin 10mA
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Plastic DIP (P)	82	39	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, R_{LIMIT} = 1.6kΩ, +5°C ≤ T_A ≤ +50°C, I_{REF} = 1mA, unless otherwise noted.

			SSM-2100			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conformity Error (Note 1)	V_{ERROR}	I_{IN} = 100nA to 100µA I_{IN} = 10nA to 1mA (Input Offset Trimmed)	– –	0.25 0.4	– –	%
Scale Factor	V_{SCALE}	Measured at Pin 16	65	70	75	mV/Decade
Scale Factor Temperature Drift	TCV_{SCALE}		–	30	–	ppm/°C
Input Offset Voltage (Note 2)	V_{IOS}		–	4	8	mV
Input Bias Current (Notes 1, 2)	I_B		–	500	2000	pA
Output Offset Voltage	V_{OOS}	$I_{IN} = I_{REF}$ = 1mA Scale Factor Set at 1V/Decade	–	30	70	mV
Power Supply Rejection Ratio (Note 3)	PSRR	+12V ≤ V+ ≤ +17V –12V ≥ V– ≥ –17V Scale Factor Set at 1V/Decade	– –	500 250	– –	µV/V
Output Voltage Swing	V_{OUT}	R_L ≥ 10kΩ R_L ≥ 2kΩ	–1 –0.2	– –	+10 +10	V
Reference Output Voltage	$+V_{REF}$	No Load	4.7	5.0	5.2	V
Reference Output Voltage Temperature Coefficient	TCV_{REF}		–	25	–	ppm/°C
Reference Output Current	I_{OUTREF}		5	–	–	mA
Reference Load Regulation		R_L ≥ 1kΩ	–	0.015	–	%/mA
Reference Supply Rejection	$PSRR_{REF}$	+12V ≤ V+ ≤ +17V	–	0.04	–	%/V
Voltage at Pin 7	$+V_{REF}$		6	7	8	V
Positive Supply Current	$+I_{SY}$	T_A = +25°C T_A = +50°C T_A = +5°C Heater Disabled	– – – –	35 20 50 5	– – – –	mA
Negative Supply Current	$-I_{SY}$		–	5	6.25	mA
Heater Start-up Current	I_{HTR}		–	80	120	mA
Regulated Chip Temperature	T_{REG}		53	60	75	°C

NOTES:
1. Guaranteed by design but not directly measured.
2. Applies to both signal and reference inputs.
3. Referred to output in log mode, or to input in antilog mode.
4. Specifications apply after a 50 second warmup period.

Specifications subject to change; consult latest data sheet.

GENERAL PRINCIPLE OF OPERATION

The SSM-2100 utilizes the predictable logarithmic relationship between the collector currents and differential input voltage of an NPN transistor pair, given by:

$$\text{delta } V_{IN} = kT/q \ \ln \ I_{C2}/I_{C1} \quad (1)$$

where: k = Boltzmann's constant (1.38×10^{-23}) J/°K)

q = charge of an electron (1.6×10^{-23} C)

T = absolute temperature (°K)

Deviation in the absolute temperature term is eliminated with the SSM-2100 design since the chip temperature is regulated at +60°C (333°K).

PRINCIPLE OF LOG OPERATION

The logging function is realized by placing the antilog element (transistor pair) in the feedback loop of the output converter amplifier (A_1) as shown in the block diagram. As shown in Figure 1, the loop is closed and the conversion is scaled with feedback resistors R_1 and R_2 from pin 16 to pin 14. The high-gain op amps (A_1 and A_2) have negligible input bias current. These force the collector currents of the high conformance transistor pair to be equal to the input current (pin 12) and the reference current (pin 6).

Referring to equation (1), the input current becomes I_{C1} and the reference current I_{C2}, while delta V_{IN} is V_{BASE} Q_2 or V_{16}, since the base of Q_1 is ground. Here, the output amplifier A_1 forces the base of Q_2 to be at the appropriate voltage governed by equation (1) and the collector currents of Q_1 and Q_2. With the reference current set at 1mA, the input current operates at less than or equal to 1mA. In the case of the inverting log amp, as the input current decreases, the V_{BE} of Q_1 decreases which increases V_{16} or V_{OUT} since the V_{BE} of Q_2 is fixed.

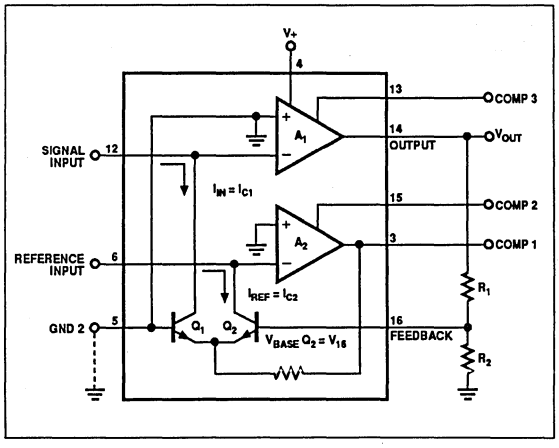


FIGURE 1: *Basic Principle of Operation*

NOTE: The output amplifier can only swing to approximately 1.5V below ground and sinks about 300µA. For this reason, they are used only with positive output voltages. For bipolar amplifier output, see Figure 7 in the Log Ratio section.

Equation (1) can be rewritten:

$$V_{16} = kT/q \ \ln \ (I_{REF}/I_{IN}) \quad (2)$$

converting to base 10:

$$V_{16} = 2.303 \ kT/q \ LOG_{10} \ (I_{REF}/I_{IN}) \quad (3)$$

Figure 1 shows the feedback which produces the output scale factor:

$$V_{OUT} = V_{16} \ (R_2/(R_1 + R_2)) \quad (4)$$

Substituting into equation 3 yields:

$$V_{OUT} = 2.303 \ kT/q \ (R_1 + R_2)/R_1 \ LOG_{10} \ (I_{REF}/I_{IN}) \quad (5)$$

Letting $\mathbf{K} = 2.303 \ kT/q \ (R_1 + R_2)/R_2$ (6)

or $\mathbf{K} = 0.066 \ (R_1 + R_2)/R_2$ (usually set to 1V/decade with R_2 = 470Ω)

For current-mode operation:

$$V_{OUT} = \mathbf{K} \ LOG_{10} \ (I_{REF}/I_{IN}) \quad (7)$$

For voltage-mode operation:

$$V_{OUT} = \mathbf{K} \ LOG_{10} \ (V_{REF}/V_{IN} \times R_{IN}/R_{REF}) \quad (8)$$

Since both op amp inputs rest at virtual ground, the reference and input currents can easily be generated by applied voltages through external resistors without generating excessive errors.

For the best results, the input and reference currents should be kept below 1mA.

A 5V reference has been included on chip for applications requiring a true log function (rather than a log ratio function).

INPUTS

As with all log amplifiers, the SSM-2100 has a limited dynamic range of 3 decades for voltage inputs. This is partially due to input offset voltage (trimmable) and various second order effects.

For the widest dynamic range, current-mode operation is recommended. The device can handle 5 decades of current input untrimmed and at least 6 decades when trimmed. Similarly, when operating in the log ratio mode, the device can handle 10 decades and 12 decades, respectively.

In order to ensure unconditional stability when operating with true current inputs, it is important to shunt the signal input to ground with a 10kΩ resistor and a 10nF capacitor in series.

NEGATIVE POWER SUPPLY CONSIDERATIONS

Because the negative power suppply is regulated at –7V, it is necessary to add a current limiting resistor (R_{LIMIT}) in series with pin 7. When using –15V for V–, a value of 1.6kΩ is recommended for R_{LIMIT}. This will keep the voltage at pin 7 very stable and useful for external trimming. Note that the negative power supply is internally regulated and needs no decoupling.

POSITIVE POWER SUPPLY CONSIDERATIONS

Because of the high gain of the temperature regulator circuit, generous positive supply decoupling should be used. The 0.2µF decoupling capacitor shown on the application circuits should be of ceramic type and mounted as close to pins 1 and 4 as possible. It should also be noted than pin 1 carries all the heater current and care should be taken when laying out ground lines to prevent this from causing errors.

TEMPERATURE CONTROL

The internal chip temperature is regulated at about 60°C if the temperature adjustment (pin 12) is not used. This on-board substrate temperature regulator stabilizes the scale factor and reduces drift of the reference.

The regulated chip temperature can be increased or decreased by the use of pin 2. To decrease the temperature by n°C, connect a resistor of the value 3.5n MΩ between pin 2 and 10. To increase the temperature by n°C, connect a resistor of the value 6/n MΩ between pins 2 and 7.

In some applications such as those requiring low power, the temperature regulator can be disabled entirely. This is accomplished by connecting a 100kΩ resistor between pins 2 and 4 (V+). In this case, the reference drift is about 70ppm/°C. The scale factor drift can be compensated by using a temperature compensating resistor* for R_2.

APPLICATIONS

The SSM-2100 can be connected for voltage or current logging functions. Figures 2a and 2b show the transfer characteristics of the inverting log amplifier for current and voltage mode operation.

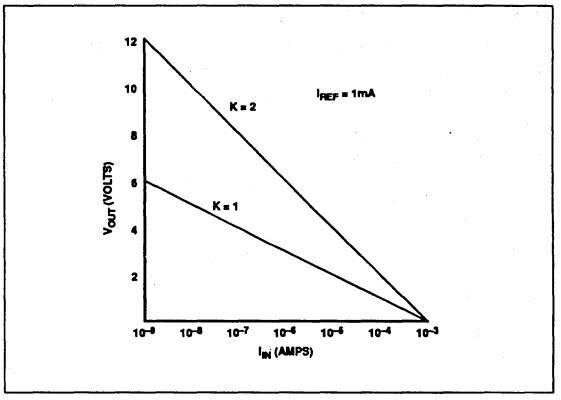


FIGURE 2a: *Inverting Log Amp with Current Input*

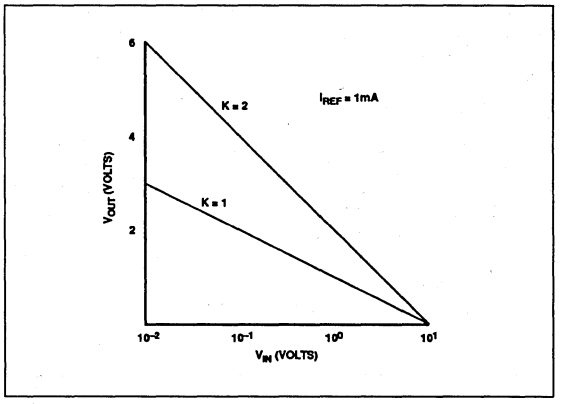


FIGURE 2b: *Inverting Log Amp with Voltage Input*

* RCD Components, Inc. Part Number LP1/4, 3301 Bedford Street, Manchester, NH U.S.A., (603) 669-0054, Telex 943512

INVERTING LOG AMPLIFIER

Figure 3 shows the SSM-2100 configured in the inverting log mode. Setting $I_{IN} = I_{REF}$ with $V_{IN} = 10V$, the output will be zero and increase by 1V/decade as I_{IN} is decreased. Whereas V_{IN} can be varied proportionally by varying R_{IN}, a 10V input optimizes the dynamic range with ±15V supplies.

To vary the scale factor, it is best to change R_1. To alter the output offset at a given input voltage, adjust R_{REF}. Phase compensation for the circuit is provided by C_1, C_2 and C_3. This scheme yields 30kHz small-signal bandwidth at 1mA input current, 8kHz at 1µA and approximately 1.6kHz at 100nA.

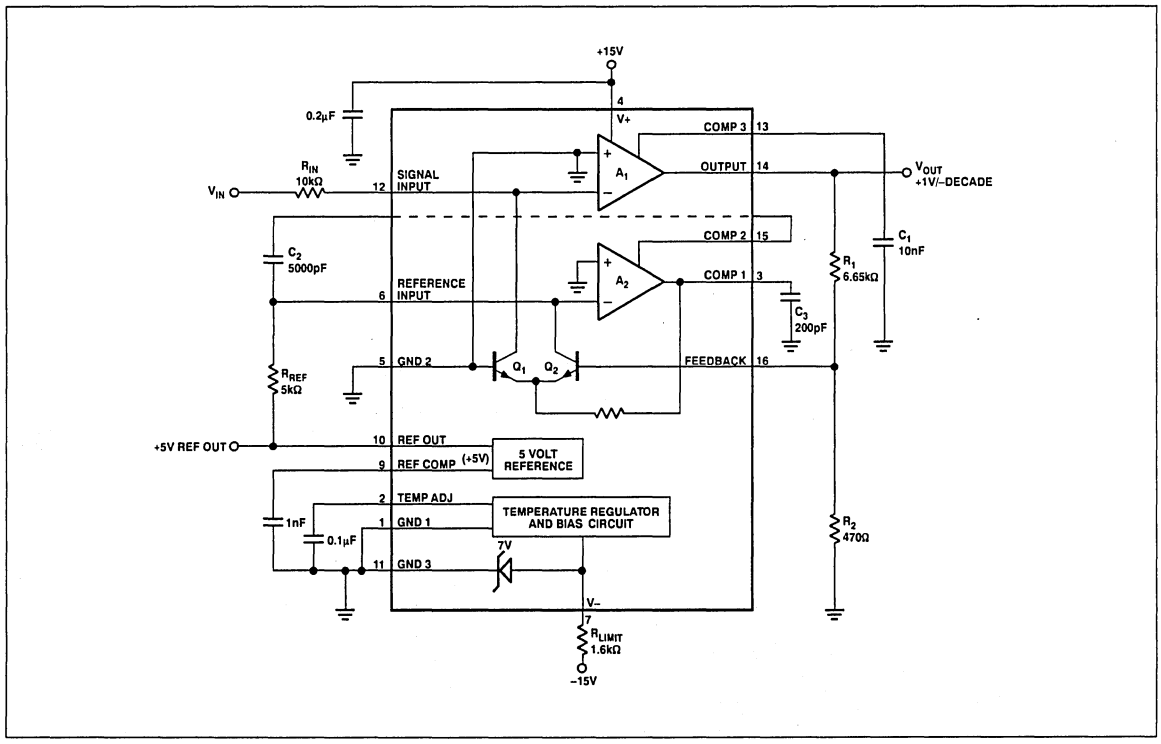


FIGURE 3: *Inverting Logarithmic Amplifier*

NONINVERTING LOG AMPLIFIER

Interchanging the signal and reference inputs yields a noninverting log amplifier as shown in Figure 4. In this configuration, the output crosses zero when the input is five decades below the full-scale value. This can be adjusted by varying R_3.

R_1 and R_2 can cause a slight inaccuracy because they add to the base resistance of Q_1 and Q_2. This can be minimized by keeping R_1 and R_2 as small as possible. It is recommended that $R_2 = 470\Omega$.

The small-signal bandwidth of this circuit is 5kHz with inputs currents from 1μA to 1mA. Over the full 5-decade input current range, the bandwidth is better than 2kHz.

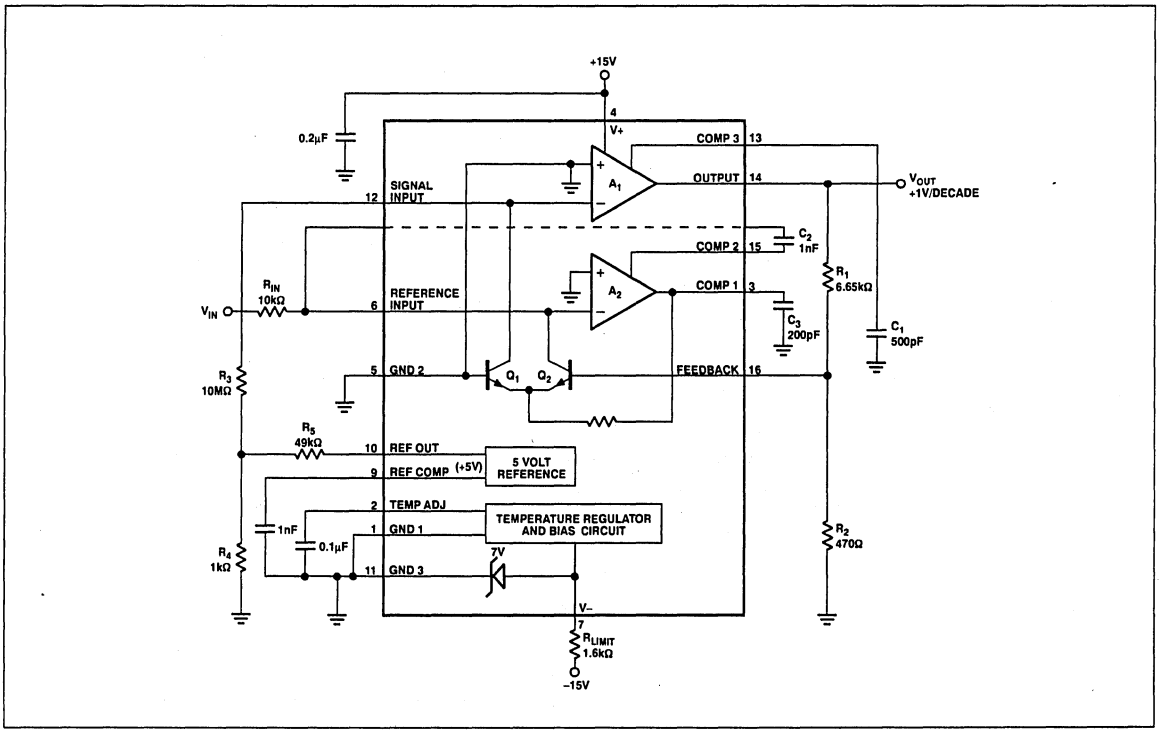


FIGURE 4: *Noninverting Logarithmic Amplifier*

ANTILOG AMPLIFIER

Figure 5 shows the configuration for the antilog amplifier. The input range for this circuit is zero to 10V which can be adjusted by R_1. The output scale factor is 1V/decade which can varied by adjusting R_{OUT}.

The transfer function is also derived from equation (1). In the antilog configuration, the current I_{C1} becomes I_{OUT} and V_{BASE} Q_2 or V_{16} is $V_{IN}(R_2/(R_1 + R_2))$. Equation (2) now becomes:

$$V_{IN}(R_2/(R_1 + R_2)) = kT/q \ \ln(I_{REF}/I_{OUT}) \quad (9)$$

or

$$I_{REF}/I_{OUT} = \exp[R_2/(R_1 + R_2) \ q/kT \ V_{IN}]$$

or

$$I_{REF} R_{OUT} = V_{OUT} \exp[R_2/(R_1 + R_2) \ q/kT \ V_{IN}]$$

Converting to base 10 and letting $K = 2.303 \ kT/q \ (R_1 + R_2)/R_2$ or $0.066(R_1 + R_2)/R_2$ (assuming T = +60°C or 333°K)

the final antilog transfer function becomes:

$$V_{OUT} = I_{REF} R_{OUT}/10^{[VIN \ R2/.066 \ (R1 + R2)]}$$

or

$$V_{OUT} = I_{REF} R_{OUT}/10^{[VIN/K]}$$

To set K = 1V/decade, $R_2/(R_1 + R_2) = 0.066$

If $R_2 = 470\Omega$, $R_1 = 6.65k\Omega$

The bandwidth of the antilog amplifier circuit is approximately 500kHz.

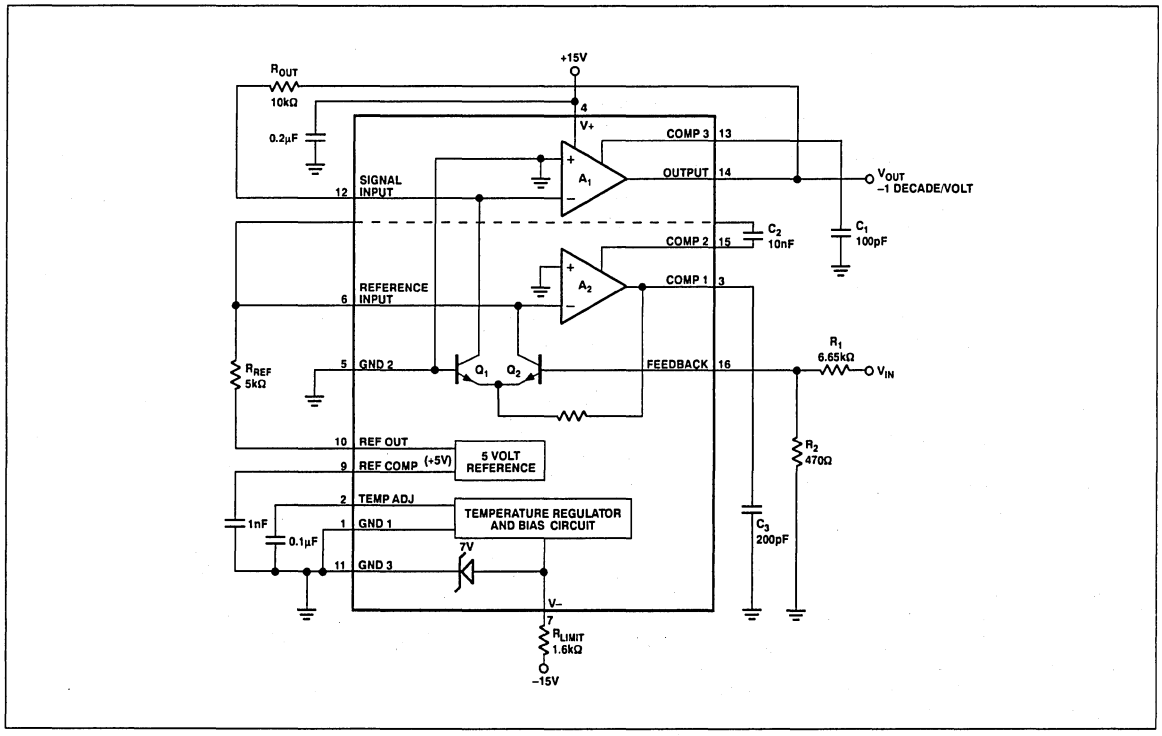


FIGURE 5: *Antilogarithmic Amplifier*

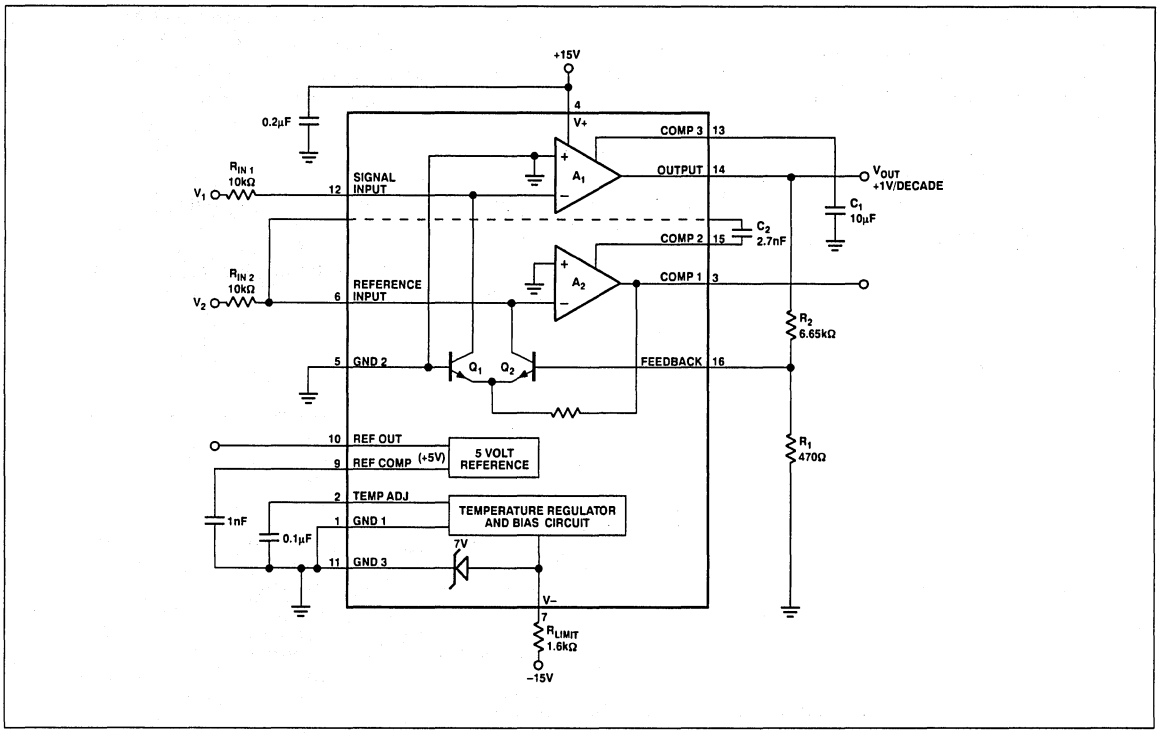


FIGURE 6: Log Ratio Amplifier, V_{OUT} = K LOG (V_2/V_1), K = 1V/Decade with Values Shown

LOG RATIO AMPLIFIER

The output of the log ratio amplifier is proportional to the ratio of its two input signals. The SSM-2100 is very well suited to this application because both the signal and reference inputs operate at true virtual ground. This eliminates the need for an external true current source as required by other types of log amplifiers.

The log ratio amplifier shown in Figure 6 has a dynamic range of 10^5 to 10^{-1} if the output buffer of Figure 7 is not used. This is because the output amplifier (A_1) can swing to a minimum of about 1.5V below ground and can only sink about 300µA maximum. Thus, the input current should not be more than one decade below the reference current.

For full four-quadrant operation, however, refer to the output buffer of Figure 7. The addition of this circuit will provide a ±5V output for reference/signal ratios from 10^5 to 10^{-5} for a full 10-decade range.

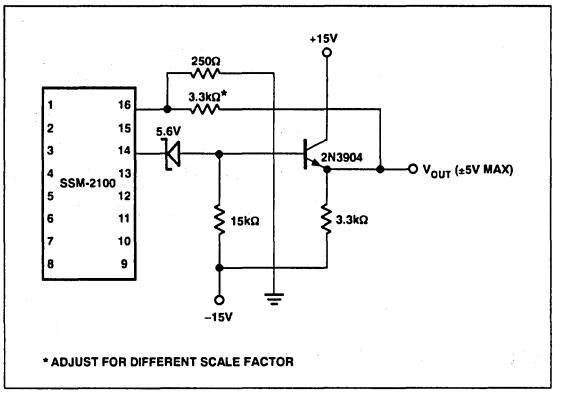


FIGURE 7: *Modification of Figure 6 for Four-Quadrant Operation*

TRIMMING THE SSM-2100

Figure 8 shows the general trimming technique for the log and log ratio applications shown in Figures 3, 4 and 6. The trim schemes for scale factor (R_1), input offset (R_x, R_y), and output offset (R_{REF}) factor are shown. For log ratio applications, the input offset trim can be duplicated for the reference input.

The scale factor trim scheme is identical in all applications. Simply replace R_1 with a 6.2kΩ resistor and 1kΩ potentiometer.

Input offset trimming removes errors from input bias current as well as amplifier offset. For optimum trim integrity, the use of the positive and negative reference voltages yields high rejection to variations in power supply voltages.

Output offset errors are essentially due to the mismatch between the base-emitter voltages of Q_1 and Q_2. The output offset adjustment (R_{REF}) scheme shown applies to the inverting log amp and the antilog amplifier. Output offset is adjusted in the noninverting log amplifier by changing R_5 in Figure 4. To adjust out the equivalent error in the log ratio amplifier, replace either of the 10kΩ input resistors with a 9kΩ resistor and 2kΩ potentiometer.

Unlike an operational amplifier, a log amp can not be trimmed with V_{IN} = 0 since the log of zero would theoretically produce an infinite output voltage.

LOG AMPLIFIER TRIM PROCEDURE

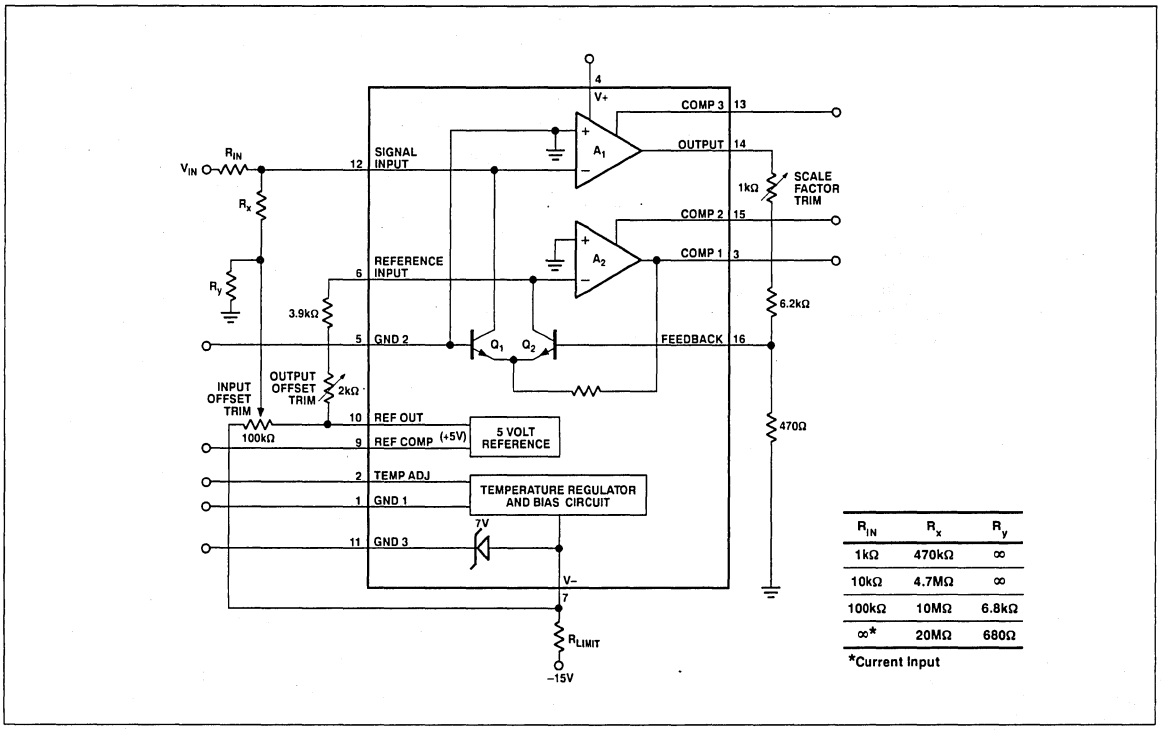
Log amp trim for K = 1:

1. Apply full-scale input voltage or current and adjust output offset for the proper output.
2. Apply an input signal one decade down from full-scale and adjust the scale factor for the desired output.
3. Finally, with the minimum input signal applied, adjust the input offset trim for the correct minimum scale output voltage or current.

ANTILOG AMPLIFIER TRIM PROCEDURE

Antilog trimming for K = 1:

1. Set full-scale by grounding V_{IN} and adjusting the output offset trim until V_{OUT} is 10V.
2. Apply 1V to V_{IN} and adjust the scale factor for 1V output.
3. Set the V_{IN} to the maximum value to be used and adjust input offset trim for the minimum desired output. Using K = 1, adjust for V_{OUT} of 0.1V with V_{IN} at 2V.



R_{IN}	R_x	R_y
1kΩ	470kΩ	∞
10kΩ	4.7MΩ	∞
100kΩ	10MΩ	6.8kΩ
∞*	20MΩ	680Ω

*Current Input

FIGURE 8: *Trimming the SSM-2100*

PMI

Audio Silicon Specialists™

Precision Monolithics Inc.

SSM-2300

8-CHANNEL MULTIPLEXED SAMPLE-AND-HOLD

FEATURES

- On-Chip 1:8 Demultiplexer, 8 Sample-and-Hold Capacitors and 8 Output Buffers
- Saves Space, Reduces System Cost
- Output Buffers Stable for $C_L \leq 500pF$
- Output Swing Includes Negative Supply
- TTL and CMOS Compatible Logic Inputs
- 5 to 18 Volts Total Supply Operation
- Low Cost

APPLICATIONS

- Automatic Test Equipment
- Process Control and Monitoring Systems
- Audio and Video Systems

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	
SSM2300P	–25°C to +75°C

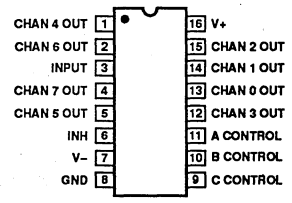
GENERAL DESCRIPTION

The SSM-2300 is an eight-channel CMOS multiplexed sample-and-hold device designed for voltage level distribution in µP controlled systems. On-chip functions include an 8-channel demultiplexer, 8 sample-and-hold capacitors and 8 output buffers. This function saves valuable board space and reduces system cost where multiple voltage levels are required.

The SSM-2300 can operate from single or dual supplies with both TTL and CMOS logic compatibility. Useful for adjusting amplifier offsets or VCA gains, one or more SSM-2300s can be used with a single DAC to provide multiple set points within a system. Applications are in ATE, audio and video, process control and monitoring systems.

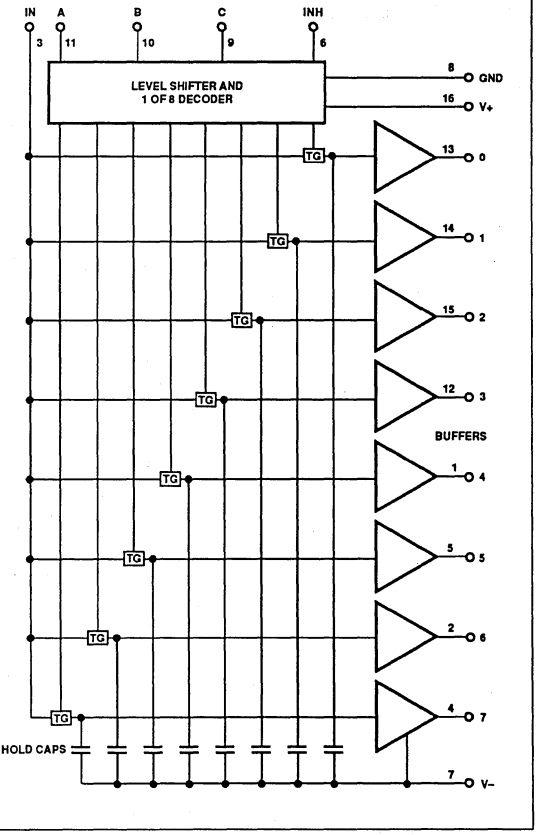
For improved performance and system upgrade, request the PMI SMP-08 data sheet.

PIN CONNECTIONS



16-PIN PLASTIC DIP (P-Suffix)

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Total Supply Range 18V
Positive Supply ($V+ - V_{GND}$) 18V
Negative Supply ($V- - V_{GND}$) ..... –10V
Storage Temperature Range
P Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... 150°C
Operating Temperature Range ..... –25°C to +75°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Plastic DIP (P)	82	39	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP.

ELECTRICAL CHARACTERISTICS at V+ = +15V, V– = GND, T_A = +25°C, unless otherwise noted.

			SSM-2300			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_S		2	4	8	mA
Positive Supply Voltage	V+	($V+ - V_{GND}$)	5	–	18	V
Negative Supply Voltage	V–	($V- - V_{GND}$)	–10	–	0	V
Logic High (A, B, C, INH)	V_{INH}	See Table 1	6	–	–	V
Logic Low (A, B, C, INH)	V_{INL}	See Table 1	–	–	0.8	V
Channel Select Time	t_{ON}		–	300	–	ns
Channel Deselect Time	t_{OFF}		–	300	–	ns
Inhibit Recovery Time	t_{INH}		–	150	–	ns
Buffer Offset	V_{OS}	$0 < V_{IN} < +13V$	–	8	50	mV
Hold Step	V_{HS}	$0 < V_{IN} < +13V$	–	4	8	mV
Acquisition Time	t_A	$0 < V_{IN} < +13V$	–	1	–	µs
Settling Time	t_S	$0 < V_{IN} < +13V$	–	2	–	µs
Droop Rate	dV_{CH}/dt	$0 < V_{IN} < +13V$	–	500	1500	mV/s
Output Source Current	I_{SOURCE}	$0 < V_{IN} < +13V$	1.2	–	–	mA
Output Sink Current	I_{SINK}	V_{OUT} = V– = GND	0.5	–	–	mA
Input/Output Voltage Range	V_{IN}	R_L = 10kΩ to GND	0	–	11	V
Maximum Output Capacitive Load	$C_{L\ MAX}$		–	500	–	pF

Specifications subject to change; consult latest data sheet.

SIGNAL INPUT (PIN 3)

The signal input should be driven by a low impedance voltage source such as the output of an operational amplifier. The op amp should have a high slew rate and fast settling time if the SSM-2300's fast acquisition time characteristics are desired. As with all CMOS devices, all input voltages should be kept within range of the supply rails (i.e., V– ≤ inputs ≤ V+) to avoid latch-up.

If single supply operation is desired, an op amp such as the OP-21, OP-80, or OP-90 with input and output voltage compliance including GND, can be used to drive pin 3. Split supplies, such as ±7.5V, can be used for the SSM-2300 and the above mentioned op amps.

If the op amp driving pin 3 is powered by dual supplies, the circuit shown in Figure 1 should be used to avoid latch-up due to negative transients during power-up. The addition of a small capacitor as shown may be useful in preventing a large false hold step.

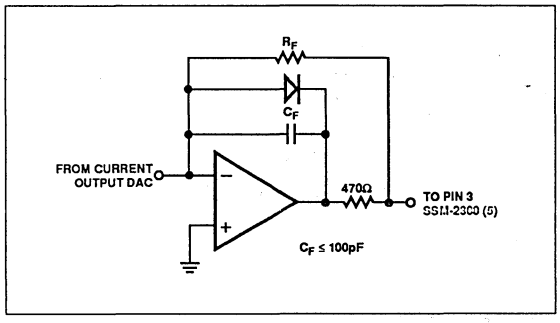


FIGURE 1: *DAC Interface Circuit (SSM-2300 Single Supply, Op Amp Driver Split Supply)*

LOGIC INPUTS (PINS 6, 9, 10 AND 11)

For V+ supplies up to +7.5 V, logic inputs can be driven by TTL or CMOS. For V+ (of the SSM-2300) from +7.5V to +12V, TTL outputs should add pull-up resistors to the +5V logic supply. For V+ of +12V or greater, CMOS logic should be used (see Table 1).

TABLE 1: Control Input Switch Points (Volts)

V+	GND	V–	V_{IH}	V_{IL}
5	0	–5	2.4	0.8
5	0	–10	2.4	0.8
3	0	–12	2	0.8
7.5	0	–7.5	3	0.8
15	0	0	6	0.8
12	0	0	5	0.8

If TTL is used to drive the logic inputs, the V+ supply should be designed to come up before the logic supply, or, current limiting (< 10mA) resistors should be connected in series with the inputs to avoid a potential latch-up condition. Open collector or 74C series logic avoid this problem because of their limited current sourcing capability.

TABLE 2: Channel Decoding

Pin 9 C	Pin 10 B	Pin 11 A	Pin 6 INH	CH	Pin
0	0	0	0	0	13
0	0	1	0	1	14
0	1	0	0	2	15
0	1	1	0	3	12
1	0	0	0	4	1
1	0	1	0	5	5
1	1	0	0	6	2
1	1	1	0	7	4
X	X	X	1	NONE	–

Table 2 shows the channel decoding for the SSM-2300 which is identical to that of 4051 type devices. When there is an address change, it is possible for two or more channels to momentarily be connected to the input at the same time. In order to avoid potential crosstalk problems, either the input signal should be kept at its previous level for 500ns after the address change (Figure 2a) or preferably INH (pin 6) should be exercised as in Figure 2b.

SUPPLIES (PINS 7, 8, AND 16)

The supply voltages V+ and V– establish the input and output voltage range which is :

V– ≤ inputs, outputs ≤ V+ – 2V

V+ and GND determine the control input logic levels and switch points (see Table 1).

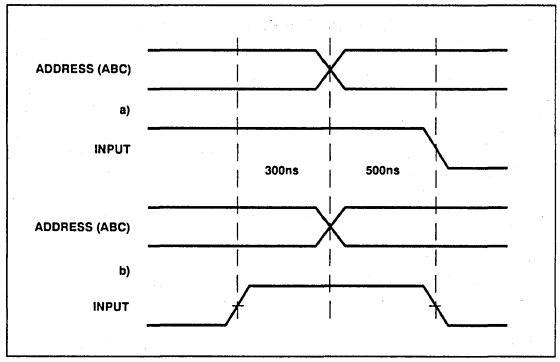


FIGURE 2: *Decode Timing*

The total supply range is 7 to 15V nominal and 5 to 18V absolute maximum, however, several specifications including acquisition time, offset, and output voltage compliance will degrade for a total supply less than 7V. The positive supply current is typically 4mA with the outputs unloaded. If split supplies are used, the negative supply should be bypassed (i.e., parallel 0.1 µF and 10µF capacitors to GND). The hold capacitors are connected to this supply pin and any noise on it will feed through to the outputs.

SUPPLY SEQUENCING

If TTL logic is used, the SSM-2300 V+ supply should be designed to come up before the logic supply; otherwise current limiting resistors should be connected in series with the logic inputs to prevent latch-up. Resistors should be chosen to limit current below 10mA.

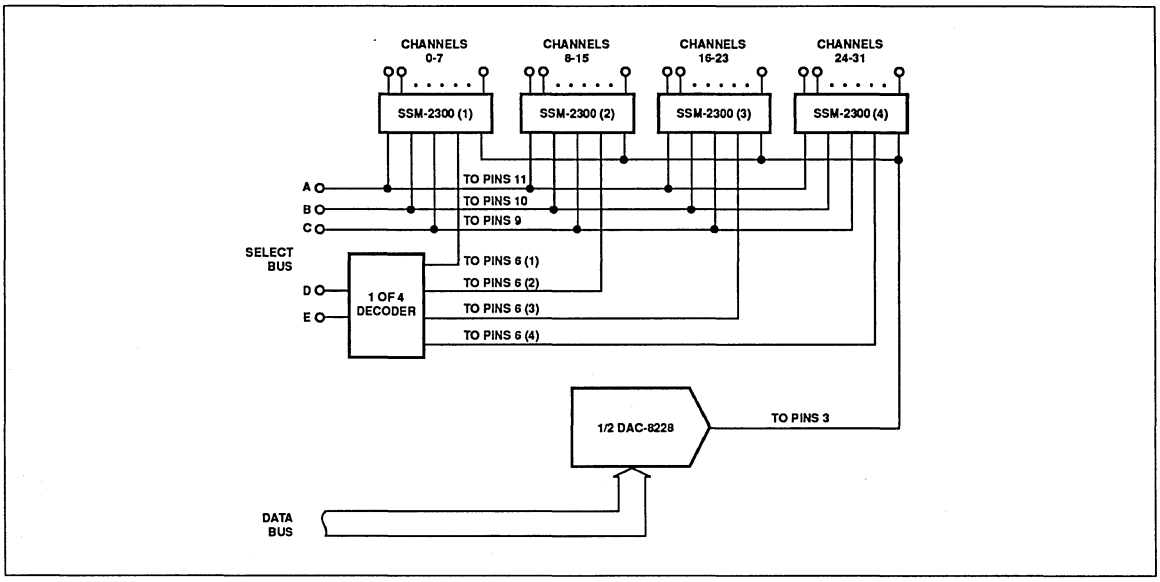
OUTPUT BUFFERS (PINS 1, 2, 3, 4, 5, 12, 13, 14, AND 15)

The buffer offset specification is ±50mV. This is approximately 1 LSB of an 8-bit DAC with a 10V full scale. The change in offset over the output range is typically 3mV. The hold step (the voltage shift when a channel is deselected) is about 4mV with little variation. The droop rate of a held channel is ±500mV/second typical and ±1500mV/second maximum (input and output(s) at opposite extremes of the voltage compliance range).

The buffers were designed primarily to drive loads connected to ground. The outputs can source more than 1.2mA each over the full voltage output range, but have limited current sinking capability near V–. In split supply operation, symmetrical output swing can be obtained by restricting the output range to 2V from either supply. The output impedance with the output sourcing current is approximately 0.1Ω. With the output sinking current, the impedance is approximately 1Ω.

The SSM-2300 buffers eliminate potential stability problems associated with external buffers as the outputs are stable with capacitive loads up to 500pF. However, the SSM-2300 buffer outputs are not short-circuit protected. Care should be taken to avoid shorting any of the outputs to the supplies or ground.

TYPICAL APPLICATION



GENERAL INFORMATION

HANDLING

By design consideration, the SSM-2300 gate inputs have a resistor/diode protection network. Inherent P-N junction diodes provide diode protection for all gate inputs and outputs. At the input and output interfaces, the diode networks of the SSM-2300 are protected from gate-oxide failure (70 - 100 volt limit) for static discharge or signal voltages up to 1,000 to 2,000 volts under most transient or low current conditions.

OPERATING

All unused inputs should be connected to either V+ or V– depending on the appropriate logic circuit. For connector-driven inputs which may temporarily become unterminated, a pull-up resistor to V+ or V– should be used with a value ranging from 0.2 to 1MΩ.

NOTE: Do not apply signals to the SSM-2300 with power off unless the input current's value is limited to less than 10mA.

APPLICATIONS

For signal frequencies near DC, almost any number of SSM-2300s can be connected in parallel; for example, in process control applications this allows a single DAC to service many control channels simultaneously (see Typical Application schematic). The 1μs acquisition time, the number of channels, and the address timing determines the maximum update rate. Sixteen channels of full band audio can be demultiplexed with a single DAC and two SSM-2300s.

Application Notes

AN-111
A BALANCED SUMMING AMPLIFIER

APPLICATION NOTE 111

The summing amplifier circuit shown in Figure 1 represents an excellent virtual ground summing amplifier using a balanced differential design that includes extremely low noise and wide bandwidth as featured by the SSM-2015. Any size audio mixing system can benefit from balanced virtual node mixing (summing). The low cost and exceptional performance of this design can be incorporated in any system with balanced or mixed balanced and unbalanced input sources.

IC_2, the PMI OP-41, serves as a DC servo-amplifier that is referenced to signal ground. The circuit functions as an integrator with a long time constant that retains the integrity of low frequency audio signals down to 5Hz, and keeps $e_{OUT} = 0V_{DC}$, ($\pm 10mV_{DC}$). The OP-41 is a FET input amplifier, with low input offset voltage (V_{OS}) and high input impedance. Although many low performance JFET/CMOS operational amplifiers can be employed, the summing output V_{DC} is a function of the servo's input offset voltage and its temperature coefficient ($\Delta V_{OS}/\Delta T$), which must be kept low for direct coupled summing applications.

In this design, the following facts predominate: $e_S = 0$, and $i_S = 0$. e_{IN} is the algebraic sum of the input(s) e_{IN1}, e_{IN2}, e_{IN3}, e_{INn} and etc. $e_{OUT} = [e_{IN1}(R_F/R_{IN1}) + e_{IN2}(R_F/R_{IN2}) + e_{IN3}(R_F/R_{IN3}) + e_{INn}(R_F/R_{INn})]$, etc. The input impedance therefore equals R_{IN1}, R_{IN2}, R_{IN3}, R_{INn}, etc. The overall gain of the circuit is set by R_F, and the gain of the individual channels can be adjusted independently by the values of R_{IN1}, R_{IN2}, R_{IN3}, R_{INn}, etc.

For individual source input(s), gain is $A_O = R_F/R_{IN}$.

The circuit configuration produces linear signal mixing at the summing nodes (IC_1 pins 10,11), whereas $e_S = 0$, therefore no interaction occurs between the source inputs. Owing to the fact that the SSM-2015 is a bipolar transistor device, the noise is low ($1.3nV/\sqrt{Hz}$). The commonly used values of 10kΩ for R_F and R_{IN} are optimal for both minimum noise and previous stage loading, eliminating the need for buffer amplifiers and their noise contribution.

The input common-mode rejection for the SSM-2015 is typically 100dB as a result of true differential input topology. The differential thermal noise and DC offset drift is nearly eliminated by the common substrate construction employed. To exploit the high CMR of the SSM-2015, all signal resistors should be matched resistor networks or should employ 0.5% or better resistor tolerances.

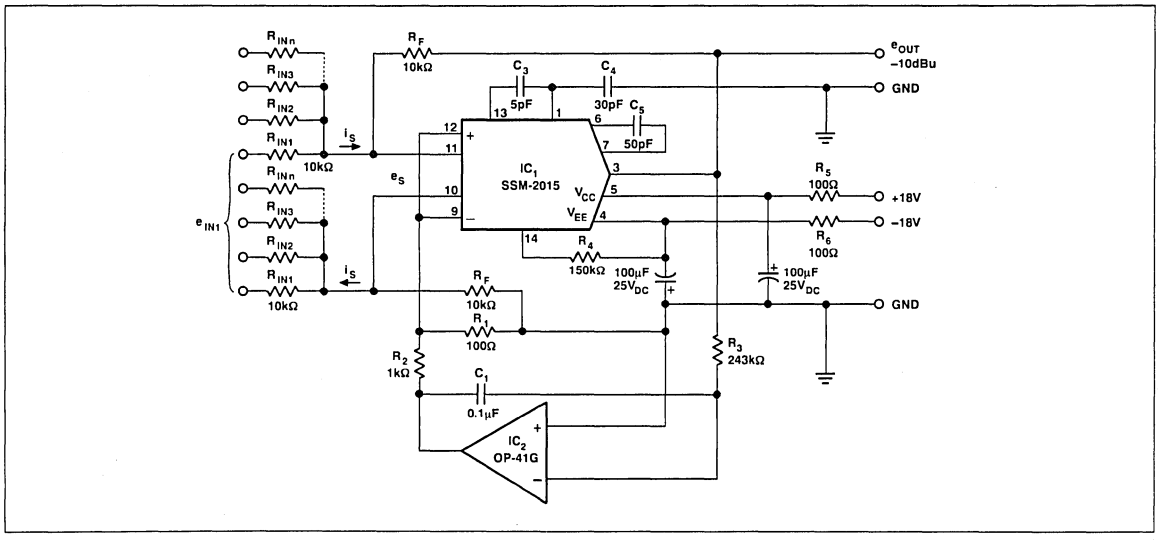


FIGURE 1

The output circuit topology of the SSM-2015 is complementary bipolar producing overall performance of 6V/μs slew rate, and is able to drive a 2kΩ unbalanced load. The circuit described can be directly coupled, eliminating coloration and distortion associated with coupling capacitors. The circuitry following this amplifier could be AC (capacitor) coupled if the DC servo IC_2 offset voltage of $\pm 10mV_{DC}$ is objectionable.

Audio performance challenges the best test equipment that might be used to measure high performance analog designs. For example: worst case THD for this circuit measures less than 0.008%, and IMD less than 0.02% over a band-width of 10Hz to 20kHz. See Table 1 for more performance details.

TABLE 1: Circuit Performance Specifications

Frequency Response (dB 20Hz to 20kHz)	±0.02
S/N Ratio @ +23dBu	103dB
TMD + Noise (@ +23dBu 20Hz to 20kHz)	0.008%
IMD (@ +23dBu SMPTE 60Hz & 4kHz, 4:1)	0.015%
CMRR (60Hz)	100dB
Slew Rate	6V/μs
Output Voltage (2kΩ load)	+23dBu or $11V_{RMS}$

AN-112
A BALANCED INPUT HIGH LEVEL AMPLIFIER

APPLICATION NOTE 112

The balanced amplifier in Figure 1 utilizing the SSM-2015 features adjustable gain and can accept nominal audio signals from –27.5dBu to +0dBu with more than 30dB of headroom. The input terminals can tolerate common-mode voltages of 30 volts peak-to-peak. Common-mode noise rejection is greater than 100dB at 1,000Hz, while the EIN (Equivalent Input Noise) is a low –124dBu.

The IC_1 amplifier circuit is gain adjustable, and the design utilizes a 12-position switch with 2.5dB steps. Other resistor values can be calculated to accommodate custom gain requirements.

IC_1 is PMI's SSM-2015 true differential input IC amplifier. Its input circuit utilizes two identical low noise bipolar transistors, with access to the emitters that provide the gain adjustment. R_G (R_{14} through R_{24}) sets the amplifier's gain using the equation:

$$\text{Gain} = 3.5 + \left(\frac{20 \times 10^3}{R_G}\right) \text{ for } R_8,\ R_{18} = 10.0\text{k}\Omega$$

The emitter feedback design exhibits both minimum noise and maximum common-mode rejection while retaining a very high input impedance. The output circuit topology is complementary bipolar producing 6V/μs slew rate, and is able to drive a 2kΩ unbalanced load. The circuit described can be directly coupled eliminating the distortion associated with coupling capacitors. Circuitry following this amplifier could be AC (capacitor) coupled if input normal-mode DC voltages are expected at the input of this circuit. Worst case THD measures less than 0.008%, and IMD less than 0.015%.

Input components C_1, C_2, R_1, and R_2 constitute a single pole low-pass filter that limits the input voltage slew rate, curbs interface transient intermodulation distortion, and keeps the amplifier from slewing. The input network has little effect on phase response within the pass band of 20Hz to 20kHz. To maintain high frequency common-mode performance, capacitors C_1 and C_2 should be matched for 1% tolerance.

For an output voltage of –10dBu, the balanced input amplifier circuit has an input sensitivity range of 0.0dBu to –27.5dBu. The common-mode voltage trim is included for maximizing application common-mode noise reduction and also allows the use of low cost components.

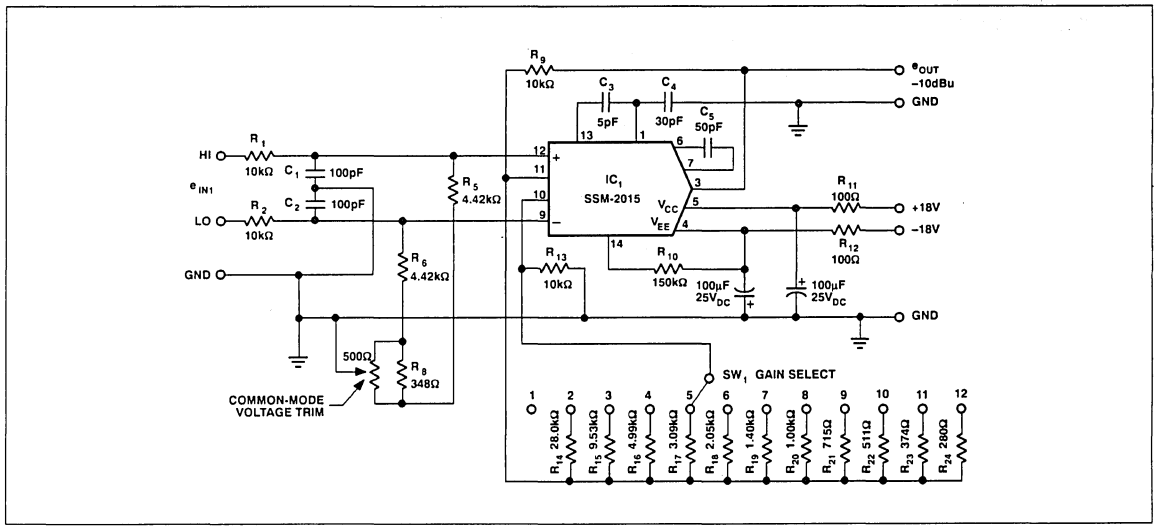


FIGURE 1

SW	G_{dB}	e_{IN}(dB)	R_G	VALUE (Ω)
1	10.0	0	R	ω
2	12.5	–2.5	R_{14}	28.0k
3	15.0	–5.0	R_{15}	9.53k
4	17.5	–7.5	R_{16}	4.99k
5	20.0	–10.0	R_{17}	3.09k
6	22.5	–12.5	R_{18}	2.05k
7	25.0	–15.0	R_{19}	1.40k
8	27.5	–17.5	R_{20}	1.00k
9	30.0	–20.0	R_{21}	715
10	32.5	–22.5	R_{22}	511
11	35.0	–25.0	R_{23}	374
12	37.5	–27.5	R_{24}	280

Specific gain can be calculated from the equation:

$$Gain_{dB} = 20 \log \left[3.5 + \left(\frac{20 \times 10^3}{R_G}\right)\right] \text{ for } R_8, R_{18} = 10.0k\Omega$$

TYPICAL APPLICATIONS

This design is ideal for use as the input amplifier in audio distribution amplifiers, for balanced input audio routing switchers, as the input buffer ahead of the A-to-D codec in digital recording and mixer equipment, or for the low noise high level input of mixing consoles.

TABLE 1: Circuit Performance Specifications

Frequency Response (dB 20Hz to 20kHz)	±0.1
S/N Ratio @ +23dBu	103dB
THD + Noise (20Hz to 20kHz) @ +23dBu	0.008%
IMD (SMPTE 60Hz & 4kHz, 4:1) @ +23dBu	0.015%
CMRR (60Hz)	100dB
Slew Rate	6V/μs
Output Voltage (2kΩ load)	+23dBu or $11V_{RMS}$

AN-113

AN UNBALANCED, VIRTUAL GROUND SUMMING AMPLIFIER

APPLICATION NOTE 113

The summing amplifier circuit shown in Figure 1 represents a splendid unbalanced virtual ground summing amplifier. The design utilizes the SSM-2134, PMI's superior version of the popular NE5534 bipolar operational amplifier. This low noise amplifier can now be implemented where most equipment manufacturers use FET input operational amplifiers. The circuit described features reduction in noise, temperature, and input impedance effects on static condition output voltages, and elimination of unity gain instability.

The SSM-2134 helps reduce wide-band noise figures by 3dB to 10dB, while improving the frequency and phase response performance. Only minimal value compensation (C_2) is required for the SSM-2134. In the feedback loop, C_1 improves stability while keeping the slew rate at 10V/μs and bandwidth greater than 100kHz.

In this circuit, note the following design facts: e_{OUT} is the algebraic sum of the input voltage(s) e_{IN1}, e_{IN2}, e_{IN3}, e_{INn} and etc. $e_{OUT} = (-) [e_{IN1} (R_F/R_{IN1}) + e_{IN2}(R_F/R_{IN2}) + e_{IN3}(R_F/R_{IN3}) + e_{INn}(R_F/R_{INn})]$, etc. The individual input impedance therefore equals R_{IN1}, R_{IN2}, R_{IN3}, R_{INn}, etc. The overall gain of the circuit is set by R_F, and the gain of the individual channels can be adjusted independently by the values of R_{IN1}, R_{IN2}, R_{IN3}, and R_{INn}.

For individual source input(s), voltage gain = R_F/R_{IN}.

The circuit configuration produces linear signal mixing at the summing node (common tie point C_1, R_F, R_{IN1}, R_{IN2}, R_{IN3}, and R_{INn}), whereas e_S = 0, there is no interaction between the source inputs. Owing to the fact that SSM-2134 is a bipolar device, noise is low (2.8nV/√Hz). The commonly used values of 10kΩ for R_F and R_{IN} are optimal for both minimum noise and previous stage loading, eliminating the need for buffer amplifiers and their noise contribution.

This design produces maximum amplifier bandwidth with unconditional circuit stability for both input and output impedance (reactive or not) variations.

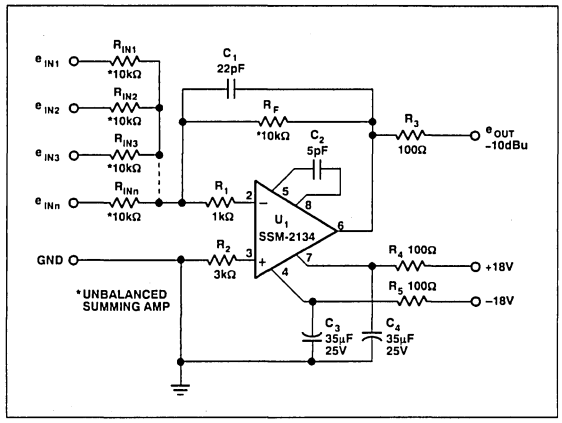


FIGURE 1

TABLE 1: Circuit Performance Specifications

Frequency Response (20Hz to 20kHz)	±0.02dB
S/N Ratio (@ +23dBu)	104dB
THD + Noise (@ +23dBu, 20Hz to 20kHz)	0.007%
IMD (SMPTE 60Hz and 4kHz, 4:1)	0.015%
Slew Rate	10V/μs
Output Voltage (2kΩ load)	+23.3dBu or 11.3V_{RMS}

PMI

Audio Silicon Specialists™

AN-114

A HIGH PERFORMANCE TRANSFORMER-COUPLED MICROPHONE PREAMPLIFIER

Precision Monolithics Inc.

APPLICATION NOTE 114

The SSM-2015 or SSM-2016 low noise differential amplifier is utilized in a transformer-coupled microphone preamplifier. The circuit shown in Figure 1 represents a microphone preamplifier with high performance, wide dynamic range, and ultra low noise. The design features a Jensen transformer-coupled preamplifier circuit with balanced/floating input, 1500Ω input loading, three step input attenuator, phantom microphone powering, and twelve amplifier gain choices. Although the design shown includes a twelve position gain selector, fixed gain applications can utilize the component value calculations and formula provided.

The design provides microphone input loading of 1500Ω. Input loading is capacitive reactive, and at higher input voltage frequencies, the low-pass network and transformer characteristics help attenuate unwanted normal-mode RF and ultrasonic voltages that might be present at the input terminals.

The input circuit contains a three position input attenuator used to optimize source levels versus amplifier headroom. As usual, it's a compromise of headroom and preamplifier signal-to-noise. The attenuation is 0dB, –10dB, and –20dB while maintaining an input impedance of 1500Ω.

A phantom microphone powering circuit is included for condenser microphones that require 24 to 48 volts DC power.

The common-mode voltage range is limited only by the transformer's primary-to-shield breakdown voltage. Common-mode rejection is a product of the primary-to-secondary isolation and provides detachment of the microphone wiring environment. Although the balanced single-pole low-pass filter at the input terminals provides protection from radio frequency interference, this network, along with the capacitive effect of the primary winding to the grounded shield, plus the phantom powering resistors present a circuit path for external RF voltages to enter the preamplifier's circuit ground. A carefully planned single point (power supply) grounding, and the true balanced and differential input topology of the SSM-2015/2016 amplifier will eliminate unwanted external noise signals.

The network composed of R_4 and C_6 at the transformer secondary serves two functions. It minimizes transformer rising secondary winding signal amplitude with rising input frequency and deters secondary ringing, while helping to prevent amplifier input slewing. The SSM-2015/2016 differential input improves transformer performance substantially as compared with the conventional unbalanced design.

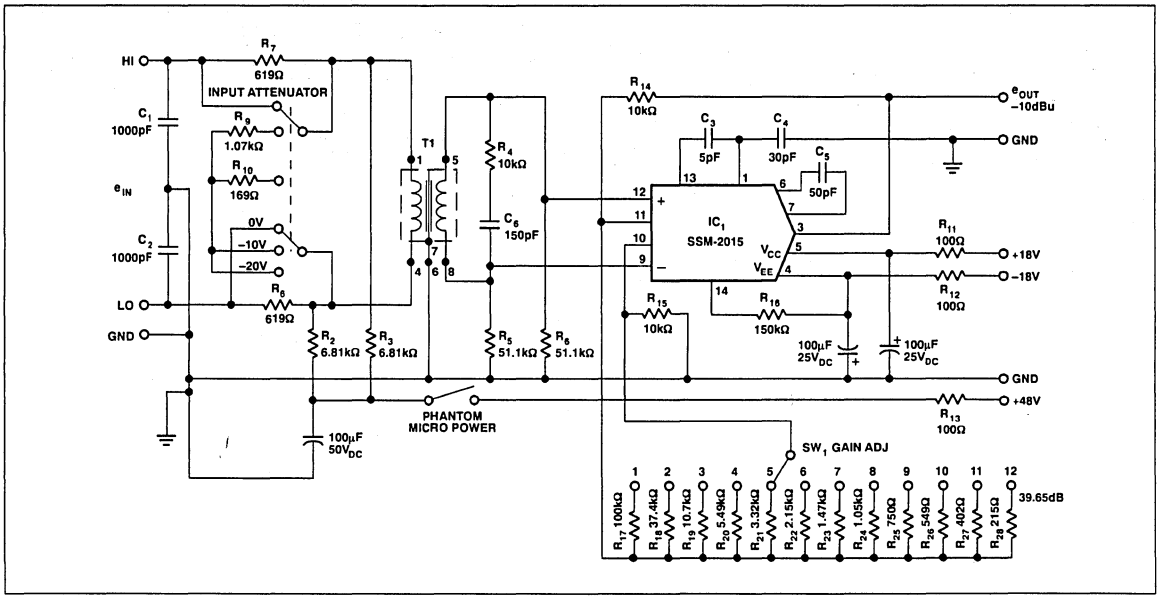


FIGURE 1

The circuit design incorporates a gain switch with twelve (12) calculated gain settings. The Jensen transformer, model JE-110K-HPC used in this application has a voltage gain of 17.9dB. For an output voltage of –10dBu, the microphone amplifier circuit has an input sensitivity range of –65dBu to –17.5dBu, with a typical output headroom of 33dB. The preamplifier circuit shown is gain adjustable from 9.6dB to 39.6dB in 2.5dB steps.

PMI's SSM-2015/2016 input circuit utilizes two identical low noise bipolar transistors, with access to the emitters, that provide the gain adjustment. The output circuit topology is complementary bipolar producing 6V/µs (2015) and 10V/µs (2016) slew rate into a 2kΩ unbalanced load.

R_G (R_{17} through R_{28}) sets the amplifier gain using the equation:

$$V_G = 3.5 + \left(\frac{20 \times 10^3}{R_G}\right)$$

for R_{14}, and R_{15} = 10.0kΩ.

SW	G_{dB}	*e_{IN}(dB)	R_G	VALUE (Ω)
1	9.6	–37.5	R_{17}	100k
2	12.1	–40.0	R_{18}	37.4k
3	14.6	–42.5	R_{19}	10.7k
4	17.1	–45.0	R_{20}	5.49k
5	19.6	–47.5	R_{21}	3.32k
6	22.1	–50.0	R_{22}	2.15k
7	24.6	–52.5	R_{23}	1.47k
8	27.1	–55.0	R_{24}	1.05k
9	29.6	–57.5	R_{25}	750
10	32.1	–60.0	R_{26}	549
11	34.6	–62.5	R_{27}	402
12	39.6	–65.0	R_{28}	215

*Input attenuator set to the 0dB position.

Unspecified overall circuit gain can be calculated from the equation:

$$G_{dB} = 20 \log\left[3.5 + \left(\frac{20 \times 10^3}{R_G}\right)\right] + 17.9$$

TYPICAL PERFORMANCE

Frequency response versus amplitude is ±0.2dB from 20 to 20,000Hz, and THD + noise is better than 0.03% over gain and frequency range described, with a typical EIN (Equivalent Input Noise) of –127dBu. See Table 1 for detailed performance specifications.

For applications where additional headroom is required, the SSM-2016 should be used. The SSM-2016 can be powered with up to ±36V_{DC} rails and drive 600Ω loads. If ±24V_{DC} rails are used, headroom increases to 35.7dB (typically), while the EIN remains at –127dB. As a consequence of the increased power supply voltage, the SSM-2016 package power dissipation will typically be 600mW with ±24V_{DC} rails (no signal), and will rise to 725mW with worst case signal conditions into 600Ω load.

For ±36V_{DC} power rails, although the headroom increases to 39.3dB, the SSM-2016 will dissipate 1.2 watts with no signal applied, and 1.5 watts worst case signal conditions into 600Ω load. Therefore IC package cooling should be taken into consideration. Please see the SSM-2016 data sheet for IC pin-out connections and recommended compensation capacitor values. All other circuit component values shown here apply.

The transformer-coupled microphone preamplifier circuit described above demonstrates robust, real-world usage refinements, along with most operational features required by equipment designers to deliver the highest performance. It will handle the most hostile microphone environments without distress to either the circuit or the user.

TABLE 1: Circuit Performance Specifications

Frequency Response (20Hz to 20kHz, –60dBu, 50dB gain)	±0.15dB
THD + Noise (20Hz to 20kHz, –60dBu, 50db gain)	0.045%
IMD (+23dBu, SMPTE 60Hz and 4kHz, 4:1)	0.05%
EIN (Equivalent Input Noise, 150Ω source)	–127dB
Input Impedance (20Hz to 5kHz)	1500Ω
Source Impedance	150Ω
CMR at 1kHz (common-mode rejection at 1kHz)	120dB
CMVR (common-mode voltage range)	±150V_{DC}
Slew Rate (overall circuit)	6V/µs
Gain Range (overall circuit)	17.5dB to 36dB
Output Voltage	
SSM-2015 (±18V_{DC}, 2kΩ load)	+23dBu or 11V_{RMS}
SSM-2016 (±24V_{DC}, 2kΩ load)	+25.7dBu or 15V_{RMS}
Output Headroom (SSM-2015, 2kΩ load, –10dBu nominal)	33dB

PMI

Audio Silicon Specialists™

AN-115

BALANCED LOW NOISE MICROPHONE PREAMPLIFIER DESIGN

Precision Monolithics Inc.

APPLICATION NOTE 115

The SSM-2015 differential amplifier is utilized in a transformerless, active-balanced input amplifier. The circuit shown in Figure 1 provides a microphone preamplifier design with excellent performance and low noise. The design features a transformerless preamplifier circuit with true-balanced input, 1500Ω input loading, phantom microphone powering, and high common-mode rejection. The design shown also includes a twelve position gain selector, or for fixed gain usage, component value calculations.

The design includes microphone input loading of 1500Ω, but the load resistor can be changed to accommodate other applications. Input loading is capacitive reactive at higher frequencies to attenuate unwanted RF and ultrasonic voltages at the input terminals.

The phantom microphone powering circuit provides power for condenser microphones that require 24 to 48 volts DC. The zener diodes CR_1, CR_2, CR_3, and CR_4 protect the input transistors of the SSM-2015 when connecting the microphone to the preamplifier circuit.

The common-mode voltage range is ±5.5 volts. Its common-mode rejection is optimized for most applications by the true-balanced and differential input topology of the SSM-2015. A balanced single pole low-pass filter at the input terminals provides protection for the circuit from radio frequency interference and prevents slewing of the SSM-2015 amplifier. The output circuit topology is complementary bipolar producing 6V/μs slew rate, and able to drive a 2kΩ unbalanced load.

The circuit design incorporates a gain switch with twelve (12) calculated gain settings. For an output voltage of –10dBu, the microphone amplifier circuit has an input sensitivity range of –65dBu to –27.5dBu, and an output headroom of 33dB. The overall circuit gain is adjustable from 27.5dB to 55dB in 2.5dB steps.

SW	G_{dB}	e_{IN}(dB)	R_G	VALUE (Ω)
1	27.5	–37.5	R_{15}	1.00k
2	30	–40	R_{16}	715
3	32.5	–42.5	R_{17}	511
4	35	–45	R_{18}	374
5	37.5	–47.5	R_{19}	280
6	40	–50	R_{20}	205
7	42.5	–52.5	R_{21}	154
8	45	–55	R_{22}	115
9	47.5	–57.5	R_{23}	86.6
10	50	–60	R_{24}	63.4
11	52.5	–62.5	R_{25}	47.5
12	55	–65	R_{26}	35.7

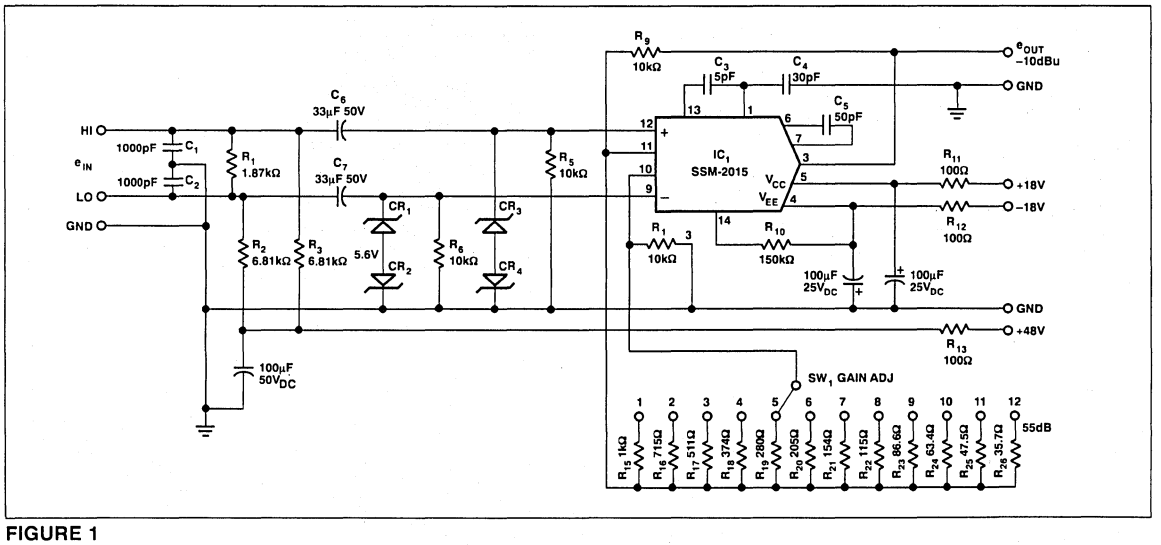


FIGURE 1

SSM-2015 input circuitry utilizes two identical low noise bipolar transistors, with access to the emitters that provide the gain adjustment. R_G (R_{15} through R_{26}) sets the amplifiers gain using the equation:

$$\text{Gain} = 3.5 + \left(\frac{20 \times 10^3}{R_G}\right) \quad \text{for } R_9 \text{ \& } R_{13} = 10.0\text{k}\Omega$$

Unspecified gain can be calculated from the equation:

$$\text{Gain}_{dB} = 20 \log \left[3.5 + \left(\frac{20 \times 10^3}{R_G}\right)\right]$$

The frequency response amplitude is ±0.1dB from 20 to 20,000Hz, and THD + noise of better than 0.03% over the gain range described with a typical EIN (Equivalent Input Noise) of –124dBu.

The transformerless microphone preamplifier circuit described above demonstrates real-world usage refinements and includes most operational features required by equipment designers.

TABLE 1: Circuit Performance Specifications

Frequency Response (20Hz to 20kHz)	±0.1dB
THD + Noise (@ +23dBu, 20Hz to 20kHz)	0.03%
IMD (@ +23dBu, SMPTE 60Hz & 4kHz, 4:1)	0.05%
EIN (Equivalent Input Noise, 150Ω source)	–124dB
CMR (Common-Mode Rejection at 1kHz)	105dB
Slew Rate	6V/μs
Output Voltage (2kΩ load) +23dBu or	$11V_{RMS}$
Output Headroom (2kΩ load, –10dBu nominal)	33dB

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AN-116

AGC AMPLIFIER DESIGN WITH ADJUSTABLE ATTACK AND RELEASE CONTROL

Precision Monolithics Inc.

APPLICATION NOTE 116

The automatic gain control (AGC) amplifier described below and shown in Figure 1, features selectable gain reduction compression ratios and time domain adjustable AGC attack and release. This design employs the SSM-2013 VCA , SSM-2110 precision level detector, two SSM-2134 low noise op amps, and an OP-215 FET input dual op amp.

The design features an inverting or noninverting input buffer amplifier, a voltage controlled amplifier with adjustable attack and recovery characteristics, driven by a true RMS level detector. Additionally, it provides selectable gain reduction compression, adjustable AGC output level, and maximum gain limit controls. Signal-to-noise ratio is better than 100dB and the RMS level detector allows the AGC amplifier to operate transparently throughout the audio spectrum. The gain recovery is linear and time adjustable, and has maximum gain limiting (gating) to preclude input source noise floor rise.

The input circuit includes a line level (–10dBu to 0dBu) buffer amplifier, that accepts inverting or noninverting inputs with greater than 10kΩ loading impedance. The buffer also isolates the input source from the compressor gain reduction ratio selector, and limits step function slewing voltage.

The six-position gain reduction selector that follows the input amplifier provides adjustable compression that smoothes the AGC action. Six GAIN REDUCTION slope ratios of 2 to 22 can be selected, thus reducing the irritating *"hole producing and pumping"* character of most AGC circuits. The SSM-2013 VCA is chosen for its predictable behavior and its high performance. The dynamic range exceeds 94dB over the frequency range 20Hz to 20kHz. Over this frequency range, the amplifier achieves typically less than 0.01% THD + noise, and 0.03% IMD.

The SSM-2110's precision rectifier circuit produces the true RMS output that comprises a level detector. It results in a consistent and precise AGC action that retains good signal dynamics while leveling the input signal. It responds to the audio signal power density in a manner similar to human hearing.

Following the precision RMS rectifier is the VCA control voltage conditioning circuits. Constructed around U_6 (OP-215), the FET-input amplifier forms an integrator while the other amplifier provides the VCA control port buffer. The AGC output level is set by the rectified signal voltage compared to the reference voltage from the OUTPUT LEVEL control.

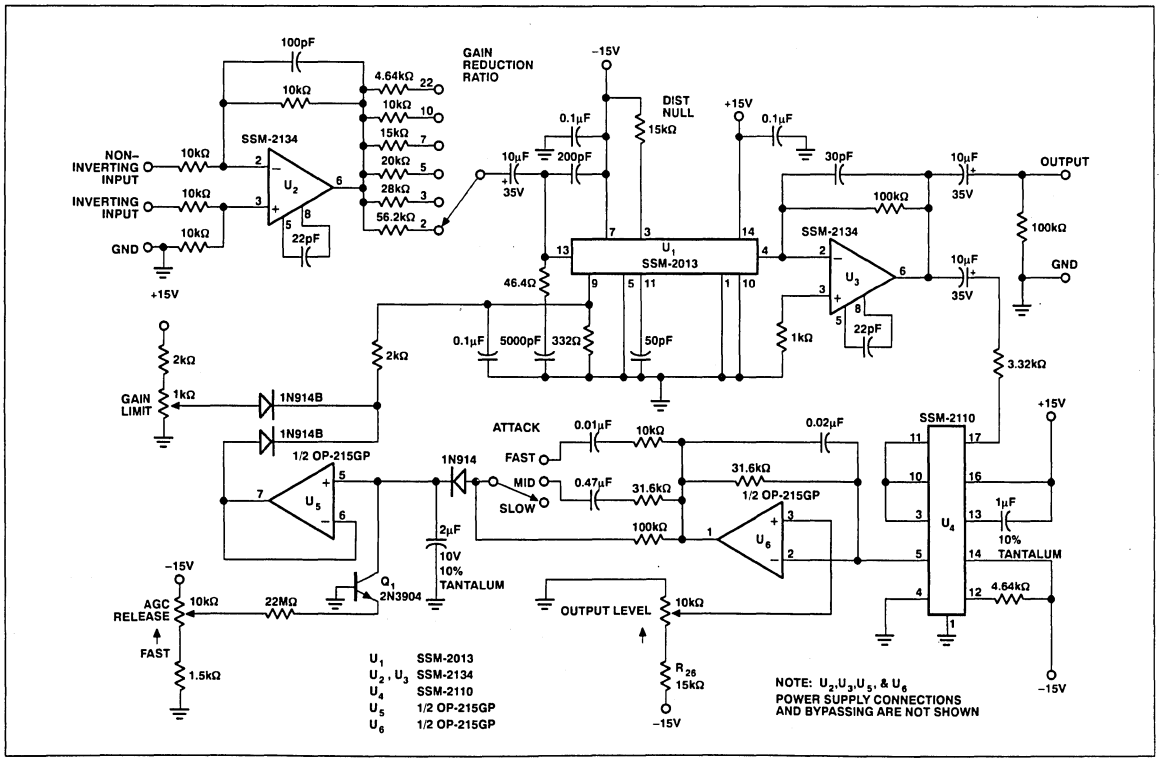

FIGURE 1

The AGC attack and compression response is altered by adjusting the integrator charging time constant or integrator wave shape current. The three-position ATTACK switch allows selection of fast, medium, and slow compression and AGC response. When the slow position is selected, an insignificant amount of compression will take place, while fast and medium combine compression with the AGC action. The AGC release rate is controlled by a constant current discharge of the integrator capacitor. The recovery time constant is linear and adjusted by changing the integrator discharge current supplied by Q_1 and regulated by the RELEASE rate control.

The SSM-2134 has been selected for its low noise and high performance characteristics. The AGC circuit described is of the feedback class, that is, the level detecting rectifier follows the voltage controlled amplifier stage. This class of AGC circuit combined with the complementary gain reduction compression, driven by RMS level detection, and adjustable attack and release AGC action, allows this circuit to be as unobtrusive or as conspicuous as desired.

The flexibility and high performance of this design, along with the simplicity and cost effectiveness, allows this design to be suitable for incorporating in mixing console designs, or in stand-alone products.

TABLE 1: Circuit Performance Specifications

Input Voltage Range (Nominal for 0dBu Out)	–26dBu to +10dBu (6mV to 2.45V_{RMS})
Rectifier Type	RMS
AGC Amplifier Class	Feedback
Attack Time	20 to 200ms
Recovery Time (6dB)	3 to 32 SEC
VCA Feedthrough (Trimmed)	–100dB
Gain Limit Range (Gain Reduction 22)	–26dBu to –12dBu
Frequency Response (20Hz to 20kHz)	±0.2dB
S/N Ratio (@ ±10dB Gain)	106dB
THD + Noise (@ +23dBu, 20Hz to 20kHz)	0.01%
IMD (@ + 23dBu, SMPTE 60Hz & 4kHz, 4:1)	0.02%
Output Voltage Slew Rate	6V/μs
Output Voltage (2kΩ Load)	+22dBu or 10V_{RMS}

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AN-121

HIGH PERFORMANCE STEREO ROUTING SWITCHER

Precision Monolithics Inc.

APPLICATION NOTE 121

The SSM-2402 Dual Audio Switch comprises the nucleus for this 16 channels-to-one high performance stereo audio routing switcher, which features negligible noise and low distortion over the frequency range of 20Hz to 20kHz. This performance is achieved even while driving 600Ω loads at signal levels up to +30dBu.

The SSM-2402 affords a much simplified electrical design and printed circuit board layout, along with reduced manufacturing cost, when compared with discrete JFET circuits of similar performance. The electrical performance of the design described is vastly superior to CMOS switch designs, which are more prone to failure resulting from electrical static discharge.

The switching control of the SSM-2402 may be activated by conventional mechanical switches or 5 volt TTL or CMOS logic circuits. The application shown utilizes a simple mechanical control switch for illustration purposes only. Many diverse X/Y control schemes, destination control, or computer controlled designs can be utilized.

The "T" configuration of the SSM-2402 switch provides excellent ON-OFF isolation. The SSM-2402 also features 7ms ramped turn on and 4ms ramped turn off for click-free switching. Additionally, the switch has a break-before-make switching sequence. Both features become significant in large audio switching systems where the audio path can pass through multiple switching elements. Such controlled switching is very important in large systems used in broadcast program switching or in production work.

The application circuit design also employs the SSM-2015 balanced input amplifier (Figure 1). The input impedance is high (≈100kΩ), balanced or unbalanced. The input circuit incorporates a single pole RFI filter with a cutoff frequency set at 145kHz. In addition, the input circuit attenuates the signal by 25dB and extends the common-mode input voltage range to ±98 volts peak, with common-mode rejection greater than 70dB from 20Hz to 20kHz. The SSM-2015 is set to produce a 15dB gain. The signal drive level into the SSM-2402 switch is then

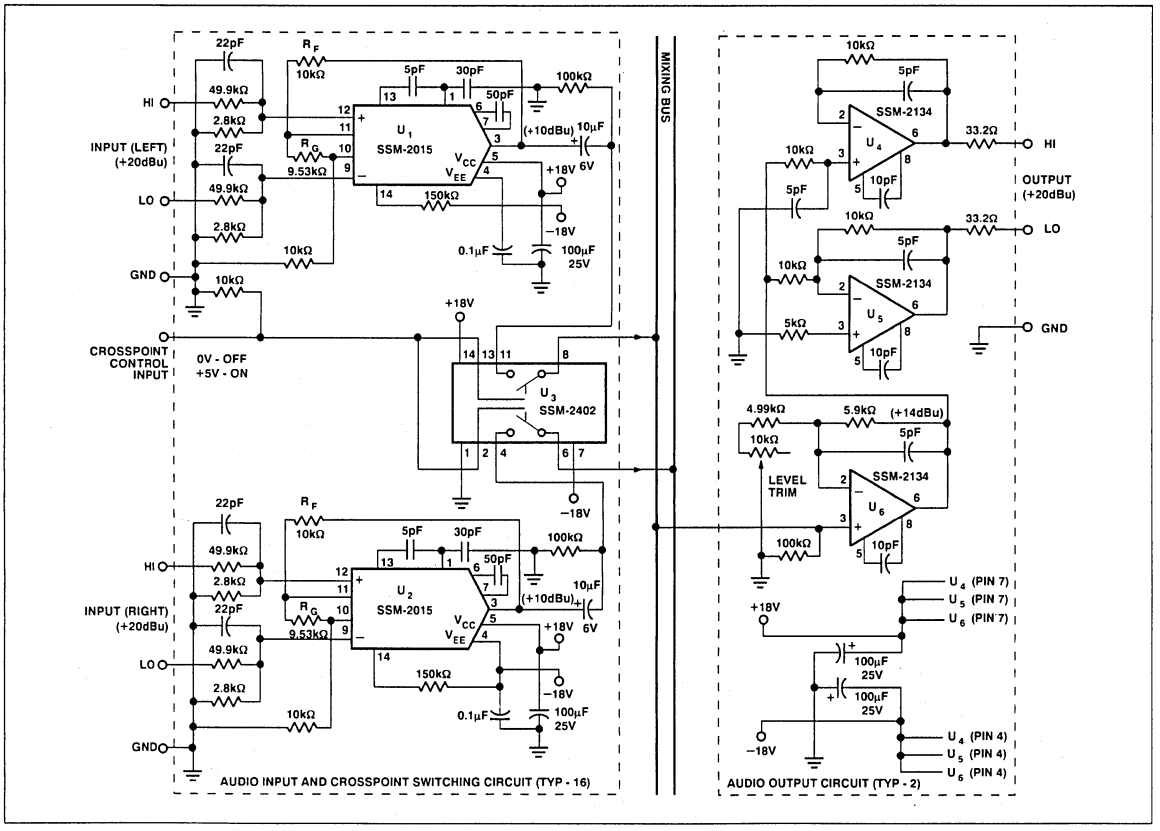

FIGURE 1: *Switcher Schematic*

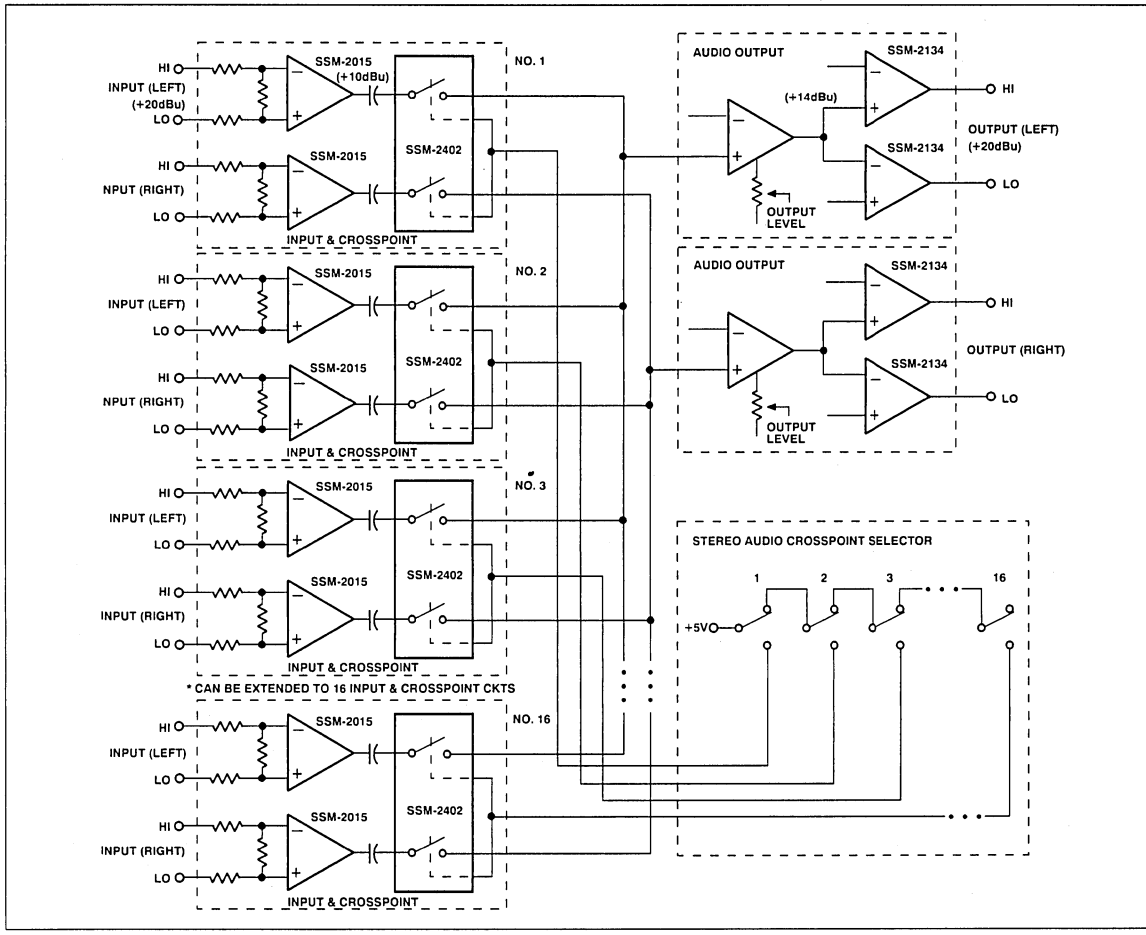

FIGURE 2: *Switcher Functional Block Diagram*

+10dBu with a +20dBu input level and +14dBu peak, well within ideal operating range. Good signal-to-noise is maintained, with generous head-room available by electing to use ±18VDC power supply voltages.

The routing switcher bus carries high level unbalanced audio, but is driven with low impedance sources. With the output impedance of the SSM-2015 at virtually 0Ω and the SSM-2402 switch ON, resistance is typically 60Ω. Bus-to-bus crosstalk is exceptionally low. For example, assuming 14pF coupling between buses and 20kHz signal, the crosstalk (isolation) exceeds 80dB. The 14pF would be representative for the 16 X 1 stereo design shown. Shielding of the buses with a printed circuit board ground plane and physically isolating the input and output circuits will reduce the crosstalk even further. The "T" configuration of the SSM-2402 switch virtually eliminates crosstalk between the various input signal sources.

The output amplifier incorporates a buffer amplifier that provides 4dB of gain (nominally), with adjustable output level trim control. The buffer also isolates the switching bus from the balanced output amplifier circuit. The balanced output is designed to drive 600Ω loads and utilizes two SSM-2134 IC amplifiers. The differential design increases drive capability, yet increases the heat dissipation surface area, and keeps IC package temperature well within safe operating limits, even when driving 600Ω loads. The SSM-2134 is recommended due to its low noise, wide frequency response, and output drive current capabilities.

Overall performance of the 16 X 1 stereo switcher is noteworthy. Input-to-output frequency response is flat to within 1dB over a 10Hz to 50kHz band. Total harmonic distortion plus noise is less than 0.03%, from 20Hz to 20kHz. SMPTE intermodulation distortion is less than 0.02%. The use of ±18VDC power supplies produces a +30dBm clip level, even when driving 600Ω loads.

TABLE 1: Circuit Performance Specifications

Max Input Level	+30dBu
Input Impedance, Unbalanced	100kΩ
Input Impedance, Balanced	200kΩ
Common-Mode Rejection (20Hz to 20kHz)	>70dB
Common-Mode Voltage Limit	±98V Peak
Max Output Level	+30dBu/dBm
Output Impedance	67Ω
Gain Control Range	±2dB
Output Voltage Slew Rate	6V/μs
Frequency Response (±0.05dB)	20Hz to 20kHz
Frequency Response (±0.5dB)	10Hz to 50kHz
THD + Noise (20Hz to 20kHz, +8dBu)	0.005%
THD + Noise (20Hz to 20kHz, +24dBu)	0.03%
IMD (SMPTE 60Hz & 4kHz, 4:1, +24dBu)	0.02%
Crosstalk (20Hz to 20kHz)	>80dB
S/N Ratio @ 0dB Gain	135dB

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AN-122

A BALANCED MUTE CIRCUIT FOR AUDIO MIXING CONSOLES

Precision Monolithics Inc.

APPLICATION NOTE 122

The SSM-2402 Dual Audio Switch enhances the performance and simplifies the design of balanced high level switching (Mute) circuits used in audio mixing consoles. The use of the SSM-2402 and SSM-2134 creates a design that has negligible transient noise (as a result of signal switching), and exceptionally low signal distortion over a wide dynamic range. The balanced high level voltage switch then drives a virtual ground summing bus through 10kΩ resistors. Also included is a design for a virtual ground summing amplifier.

The SSM-2402 is a monolithic dual audio switch that improves electrical performance and eases printed circuit board layout design. The design reduces manufacturing cost when compared with discrete JFET designs of similar performance. Electrical performance is measurably superior to CMOS switch designs, and will be less prone to failure from electrical static discharge.

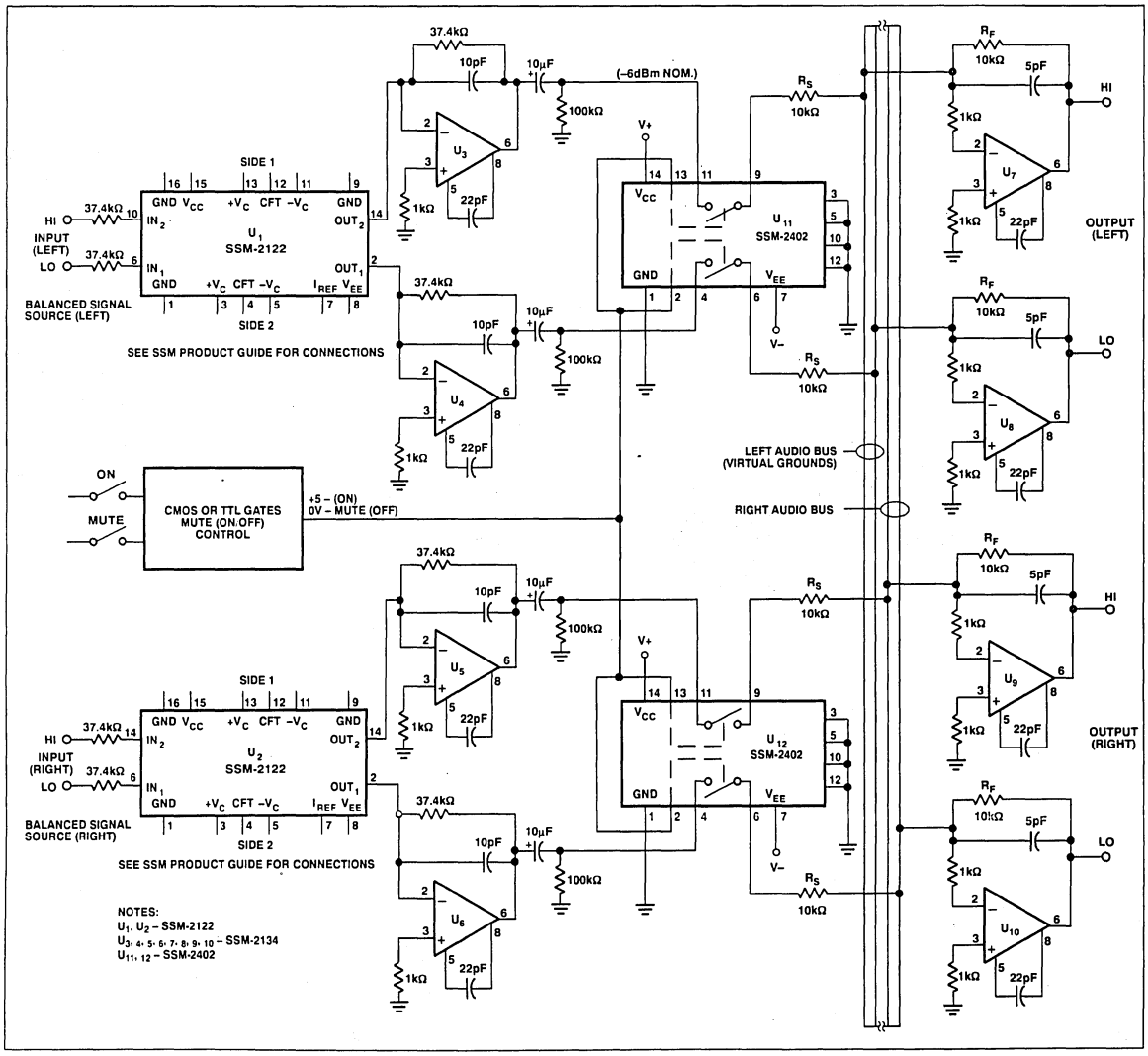

FIGURE 1: *Audio Mixer Channel Mute (On/Off) Circuit, a Balanced Design with High Level Bus Switching*

The "T" switch configuration of the SSM-2402 provides excellent ON-OFF isolation. The design shown further improves the ON-OFF isolation and left/right channel crosstalk figures by maintaining the common-mode rejection ratio of a fully balanced design. The switch features a 7ms ramped turn-on and 4ms ramped turn-off, and guaranteed break-before-make switching sequence for transient-free audio switching. The system performance is improved for large audio consoles that have multiple switches in the audio signal path.

The switch control ports are easily interfaced to conventional $5V_{DC}$ TTL or CMOS digital control circuits, further simplifying the control circuit design. Furthermore, product reliability and serviceability are improved by the simplified design. The application shown uses an elementary control circuit to functionally illustrate control voltage requirements. Customized logic gate control schemes or computer-controlled designs can easily be implemented.

The application circuit design employs dual audio switches driven by U_3, U_4, U_5 and U_6 inverting amplifiers. Their gain is controlled by two dual voltage controlled amplifier (VCA) elements U_1 and U_2. A simplified signal path is shown for application clarity. For additional design information of the SSM-2122 dual VCA, consult the data sheet.

The design shown in Figure 1 is signal phase noninverting, and incorporates a minimum number of components to minimize noise. The input signal source should be balanced to maximize separation and crosstalk isolation. PCB layout should also utilize equal inductance in each side of the signal path wiring, and include equal stray capacitance to ground and other signal paths to obtain maximum performance. The SSM-2122 VCA provides good gain tracking of the two audio channels, while maintaining accuracy in the balanced signal path.

U_{11} and U_{12} are utilized as high level switches so that other post-switching functions can be employed. A nominal drive level of 0dBu balanced (–6dBu unbalanced) is applied to the switch. This level is arbitrary, but will satisfy most signal-to-noise and headroom compromises. The output of amplifiers U_3, U_4, U_5, and U_6 are AC coupled prior to the switches to further minimize the switching transients caused by active component offset voltages. The balanced virtual ground mixing buses are current driven by R_S of 10kΩ. This value can affect overall system performance, and should be modified to suit the size of the mixing bus system. A greater number of input mixing channels will warrant lower bus drive current. Although the individual values of R_S and R_F can be altered, their values must be the same for a summing amplifier voltage gain of one (1).

TABLE 1: Circuit Performance Specifications

Max Input Level	+30dBu
Input Impedence, Balanced	75kΩ
Common-Mode Rejection (20Hz to 20kHz)	>70dB
Common-Mode Voltage Limit	±12V Peak
Max Output Level	+30dBu
Output Voltage Slew Rate	12V/μs
Frequency Response (±0.05dBu)	20Hz to 20kHz
Frequency Response (±0.5dBu)	10Hz to 50kHz
THD + Noise (20Hz to 20kHz, +8dBu)	0.005%
THD + Noise (20Hz to 20kHz, +24dBu)	0.03%
IMD (SMPTE 60Hz & 4kHz, 4:1, +24dBu)	0.02%
ON/MUTE Isolation (20Hz to 20kHz)	>85dB
S/N Ratio @ 0dB Gain	135dB

The active switches' ON resistances are typically 60Ω and are well matched. One should use 1% or better tolerance series resistor R_S (10kΩ) to minimize imbalance in the signal path. In the OFF state, the "T" configuration of the switch virtually eliminates leakage of the input source signal into the mixing bus(es). Greater than 100dB mute isolation at 1kHz can be obtained with prudent printed circuit board design since the SSM-2402 control inputs and switch terminals are separated by ground guards.

The use of $\pm 18V_{DC}$ power supplies allows a +30dBu (balanced) clipping level. All integrated circuit components mentioned will operate reliably at $\pm 18V_{DC}$, and noise contribution will be indiscernible, even in large mixing systems. The balanced input to balanced output frequency response is typically greater than 10Hz to 50kHz, within 1dB. Total harmonic distortion plus noise will measure less than 0.01%, from 20Hz to 20kHz at +30dBu, while SMPTE intermodulation distortion less than 0.02% under the same measurement conditions.

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AN-123

A CONSTANT POWER "PAN" CONTROL CIRCUIT FOR MICROPHONE AUDIO MIXING

Precision Monolithics Inc.

APPLICATION NOTE 123

The SSM-2134 permits the design of a constant power, transient-free "PAN" control circuit suitable for installation in the highest performance audio mixing consoles. The design incorporates unique and vital features. The PAN IN/OUT switch does not introduce transient type noise or interruptions in the audio when activated or deactivited, and when panning, an accurate constant power output is maintained between the sum of the two channels. The design allows "punching-in" and "punching-out" of the PAN circuit while mixing down or on-the-air, without transient clicks or holes in the mix.

The design utilizes conventional parts, e.g., a single SPST switch and a linear 10kΩ potentiometer. U_1 (SSM-2134) is used as a unity gain, inverting buffer with an input impedance of 37.4kΩ. The input source could be a VCA element or audio direct from the fader control. The values shown will allow a VCA, for example, the SSM-2013, to be used with only minor additions. The overall application circuit is noninverting from input to output.

The 15kΩ series input resistors R_S, plus the inverting input 15kΩ R_I in parallel with 5kΩ (1/2 of 10kΩ, with the PAN control in the center) forms an attenuator that has a 14dB loss. Rotating the PAN control in either direction decreases the attenuation to −11dB for one channel and maximum attenuation for the other.

$$\frac{1}{R_L} = \frac{1}{R_I} + \frac{1}{5k\Omega}, \qquad R_L = 3.75k\Omega$$

Attenuation is calculated as:

$$dB_{LOSS} = 20 \log \frac{R_L}{R_L + R_S} = 20 \log \frac{3.75k\Omega}{3.75k\Omega + 15k\Omega} = -14dB$$

Amplifier (U_2 & U_3) gain is:

$$dB_{GAIN} = 20 \log \frac{R_F}{R_I} = 20 \log \frac{75k\Omega}{15k\Omega} = +14dB$$

The frequency response is typically 10Hz to 50kHz, within 0.5dB. Total harmonic distortion plus noise will measure less than 0.007% from 20Hz to 20kHz, and SMPTE intermodulation distortion less than 0.01%. The amplifier clipping level is +24dBu with $\pm 18V_{DC}$ power supply rails. Headroom is nominally 30dB, and 27dB at full PAN for the operating channel.

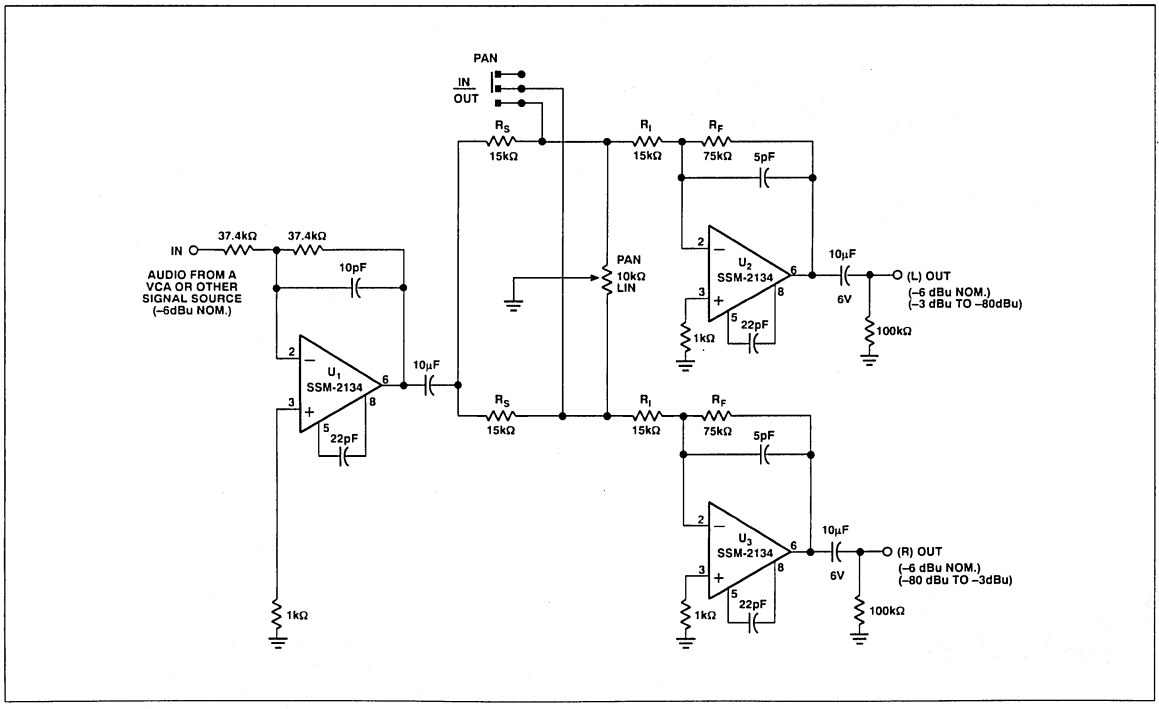

FIGURE 1: *Constant Power Type Control Circuit with Transient Free IN/OUT Switching*

TABLE 1: Circuit Performance Specifications

PAN Range, L ← C → R (L Out)	+3dB ← 0dB → –80dB
PAN Range, R ← C → L (R Out)	+3dB ← 0dB → –80dB
Max Input Level	+24dBu
Input Impedance, Balanced	37.4kΩ
Max Output Level (> 600Ω ±18V_{DC} PS)	+24dBu
Headroom	30dB
Output Voltage Slew Rate	<6V/μs
Frequency Response (±0.05dB)	20 Hz to 20kHz
Frequency Response (±0.5dB)	10 Hz to 50kHz
THD + Noise (20Hz to 20kHz, +8dBu)	0.005%
THD + Noise (20Hz to 20kHz, +24dBu)	0.03%
IMD (SMPTE 60Hz & 4kHz, 4:1, +24dBu)	0.02%
S/N Ratio	130dB

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AN-124

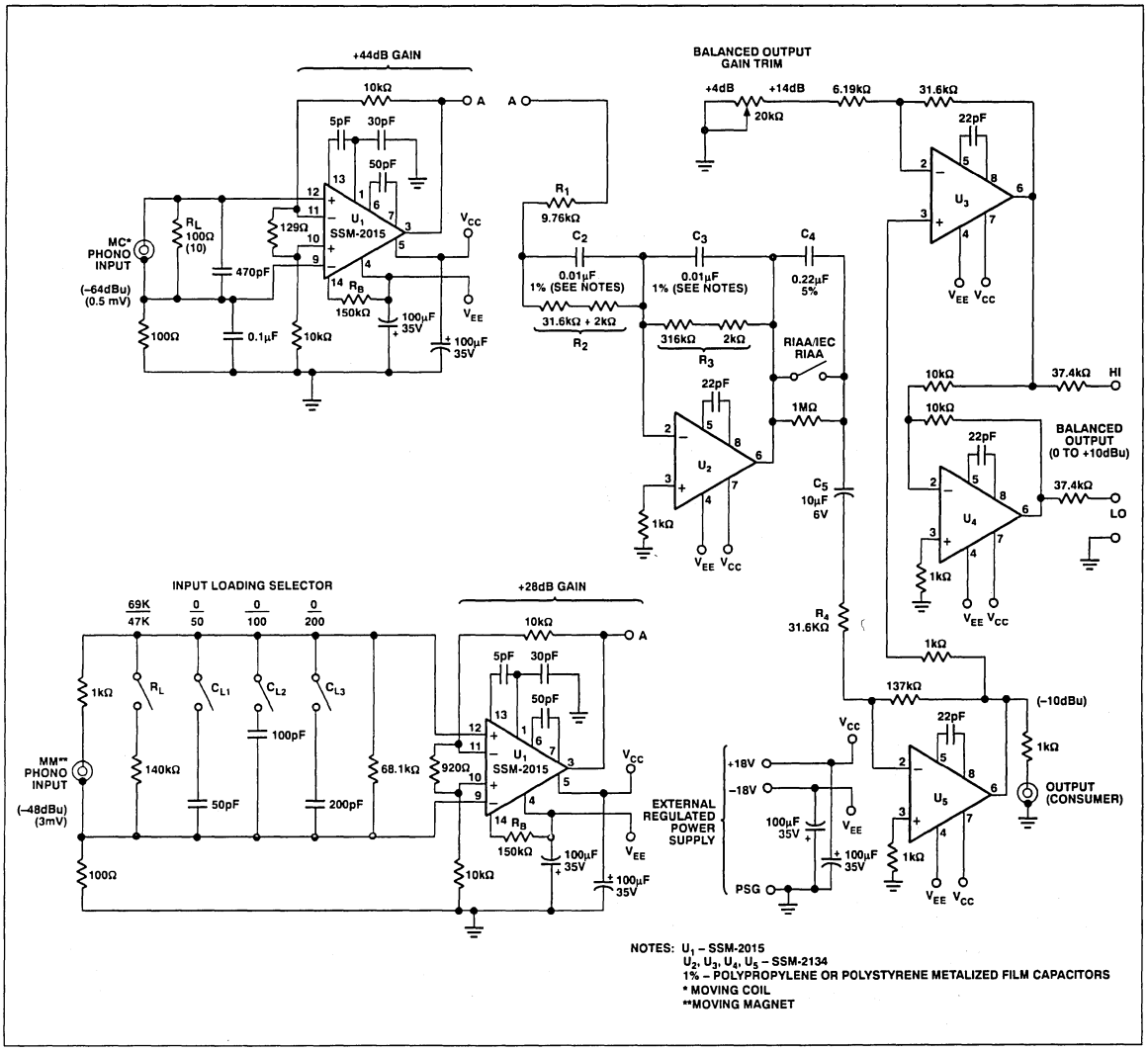
THREE HIGH ACCURACY RIAA/IEC MC AND MM PHONO PREAMPLIFIERS

Precision Monolithics Inc.

APPLICATION NOTE 124

Although the digital compact disk is rapidly supplanting the vinyl disk as the popular media method for professional and consumer audio entertainment, the electro-mechanical recording and reproduction of audio signals has many more years of life. The group of phono preamplifier application designs below will make the future years with vinyl more productive and pleasant. The applications employ solid engineering concepts, and dismiss "golden ear" discussions.

One design includes an input scheme for both moving coil (MC) and moving magnet (MM) – or variable reluctance – transducers. All designs employ extremely low noise circuit topologies, high accuracy active and passive RIAA (Recording Industries Association of America) equalization with selectable old RIAA or RIAA/IEC (International Electro-Technical Commission) curves. The applications incorporate both consumer and balanced output circuit configurations.



NOTES: U_1 – SSM-2015
U_2, U_3, U_4, U_5 – SSM-2134
1% – POLYPROPYLENE OR POLYSTYRENE METALIZED FILM CAPACITORS
* MOVING COIL
** MOVING MAGNET

FIGURE 1: *High Accuracy RIAA/IEC MC or MM Phono Preamplifier*

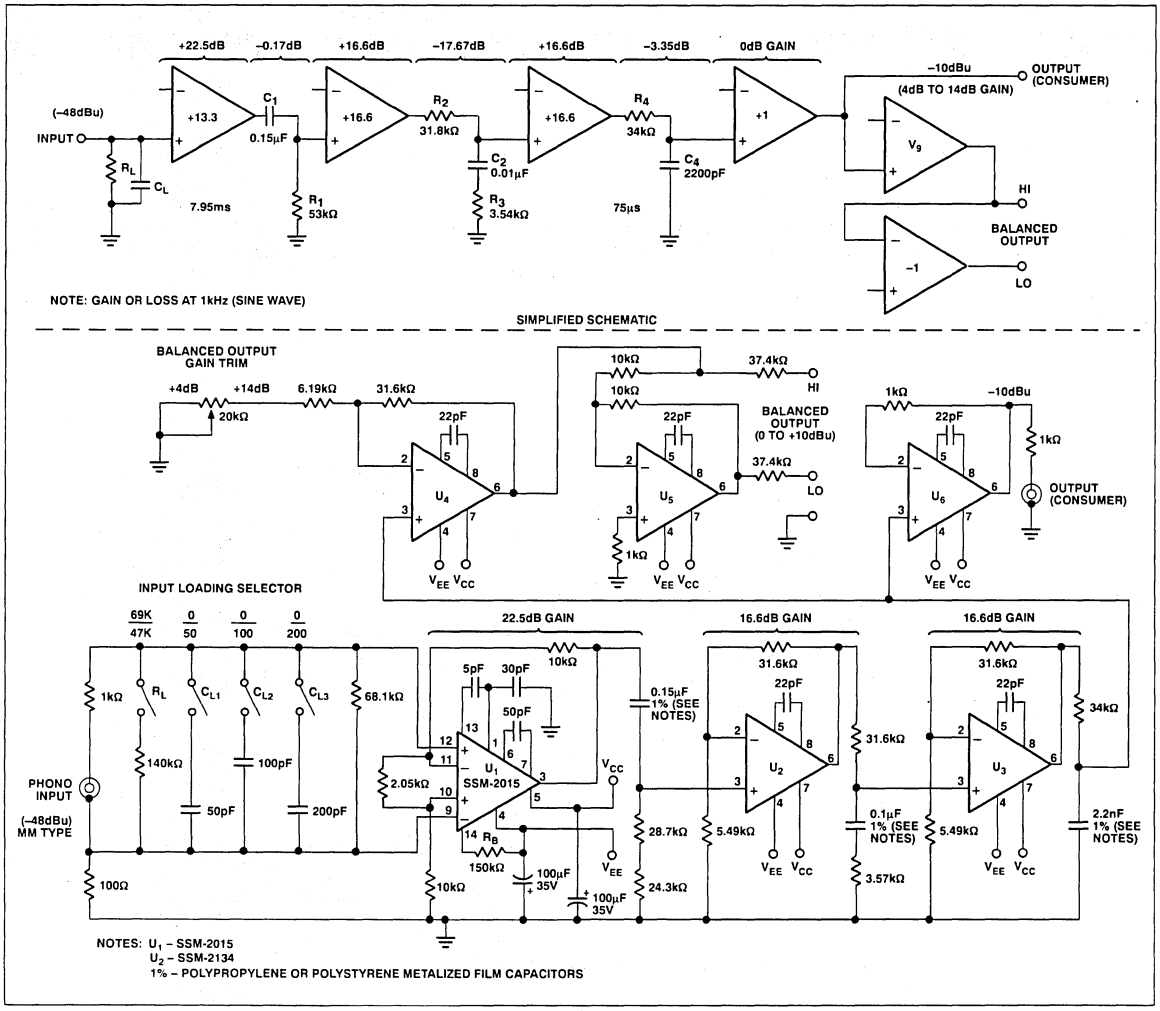


FIGURE 2: *Passive (Multi-Filter) RIAA/IEC Equalized Phono Preamplifier*

A HIGH ACCURACY DESIGN

In the High Accuracy RIAA/IEC Phono Preamplifier shown in Figure 1, both MC and MM transducer input configurations are presented. Both utilize the PMI SSM-2015 differential amplifier and take advantage of the high common-mode rejection it provides. The overall circuit structure *does not* incorporate any design compromises. It provides the lowest possible noise, adjustable MM input loading, highest accuracy RIAA filtering, and is completely devoid of transient and frequency dependent gain errors. The wide bandwidth stages minimize in-band phase shift, and provide exceptional phase and frequency response accuracy. This allows the RIAA/IEC filter to render the exact reciprocal of the recorded phase and frequency characteristics.

Referring to Figure 1, the MC input circuit has input loading (R_L) set at 100Ω. (Note: some MC transducers require 10Ω loading for maximum reproduction accuracy. For these, replace R_L with a 10Ω metal film resistor.) The input circuit gain is 44dB, and provides a -20dBu signal level at point A. 44dB gain should be adequate for most MC cartridges available. If U_1 gain requires adjusting, use the equation:

$$G_{dB} = 20 \log\left(3.5 + \frac{20 \times 10^3}{R_G}\right)$$

R_B sets the U_1 bias value and contributes to symmetrical amplifier slewing. The RIAA filter stage that follows U_1 stage(s) all but eliminates noise produced by the input amplifier.

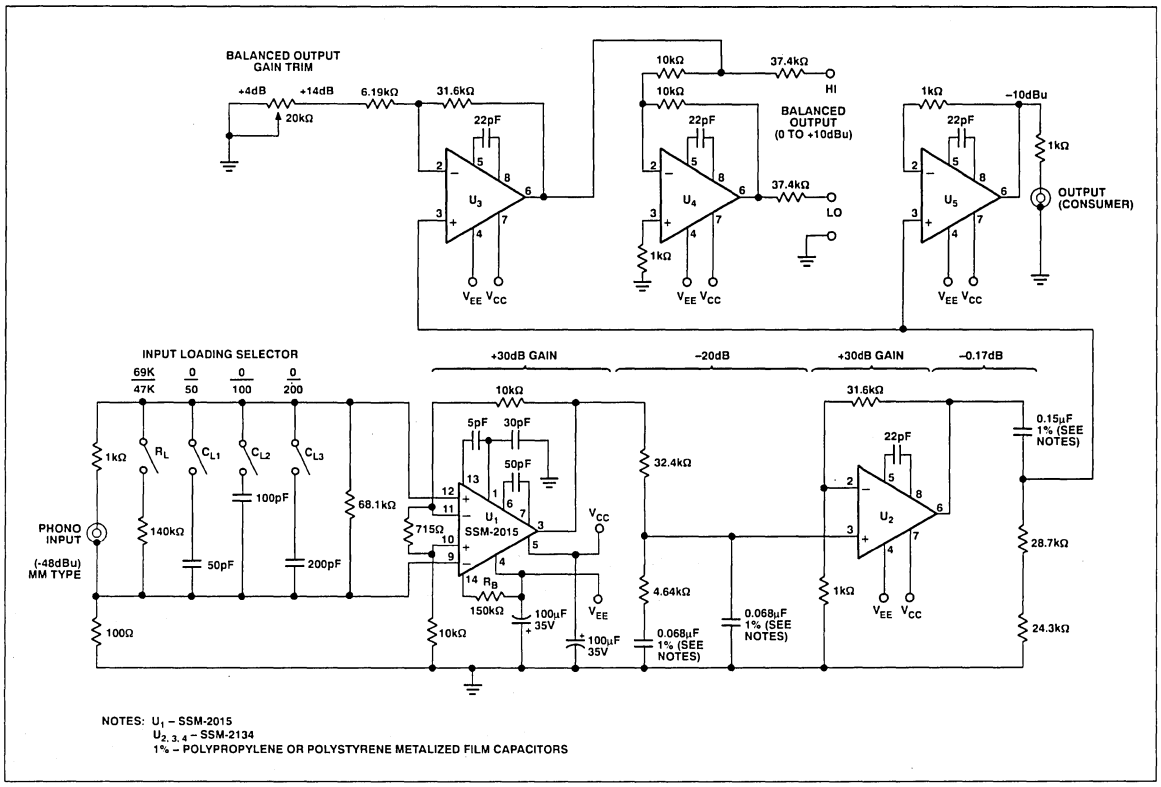


FIGURE 3: *Passive RIAA/IEC Equalized Phono Preamplifier*

The next stage contains the RIAA-RIAA/IEC equalization filter and is built around U_2, the SSM-2134 operational amplifier, and is an active feedback type filter. The overall gain of this circuit at 1,000Hz is –2.5dB. RIAA equalization requires a gain of 19.3dB at 20Hz, and attenuation of 19.6dB at 20,000Hz. The open-loop gain of U_2 is greater than 100dB at 20Hz, and 60dB at 20,000Hz, ensuring exceptional equalization accuracy.

Three filters make up the RIAA reproduction curve. The time constants are: 75µs, 318µs, and 3180µs, and a fourth time constant in the RIAA/IEC curve is 7960µs. The IEC filter was introduced to minimize warp and infrasonic signal interference while maintaining flat frequency response down to 40Hz.

- The 75µs filter is formed by resistors R_1 (9.76kΩ) and R_2 (31.8kΩ) in parallel with capacitor C_2 (0.01µF).
- The 318µs pre-emphasis filter is formed by R_2 (31.8kΩ) and C_2 (0.01µF).
- The 3180µs filter is formed by R_3 (318kΩ) and C_3 (0.01µF).
- The fourth pole, IEC 7960µs, a high pass filter is formed by R_4 (31.6kΩ) and C_4 (0.22µF), and provides 3dB attenuation at 20Hz rolling off at –6dB/octave thereafter.

Table 1 contains the complete RIAA and RIAA/IEC reproduction equalization characteristics. RIAA/IEC switching allows selection of either reproduction response curves. For the "audio purist," C_5 can be eliminated for a direct coupled design, thus reducing envelope and group delay distortions. All amplifier feedback circuits are direct coupled, and are referenced to circuit ground. The closed-loop gain is kept low to minimize input offset voltage, therefore only very small DC voltages can be expected at the output of the directly coupled version.

The high level amplifier, U_5, provides +12.7dB gain and feeds the unbalanced Consumer Output jack, with a nominal –10dBu level. U_5 is followed by balanced output buffer amplifier. The nominal output level is continuously adjustable from 0.0dBm to +10dBm at the balanced output terminals. The output source impedance is 75Ω, and will drive 600Ω loads to a maximum +30dBm clip point level. Table 2 shows circuit performance specifications.

TABLE 1: RIAA/IEC and RIAA Playback Characteristics

Frequency (Hz)	RIAA /IEC Relative Level (dB)	RIAA Relative Level (dB)
2.0	−0.2	
2.5	+1.8	
3.15	+3.7	
4.0	+5.7	
5.0	+7.6	
6.3	+9.4	
8.0	+11.2	
10.0	+12.8	
12.5	+14.1	
16.0	+15.4	
20.0	+16.3	+19.3
25.0	+16.8	+19.0
31.5	+17.0	+18.5
40.0	+16.8	+17.8
50.0	+16.3	+16.9
63.0	+15.4	+15.8
80.0	+14.2	+14.5
100	+12.9	+13.1
125	+11.5	+11.6
160	+9.7	+9.8
200	+8.2	+8.2
250	+6.7	+6.7
315	+5.2	+5.2
400	+3.8	+3.8
500	+2.6	+2.6
630	+0.8	+0.8
1,000	0.0	0.0
1,250	−0.8	−0.7
1,600	−1.6	−1.6
2,000	−2.6	−2.6
2,500	−3.7	−3.7
3,150	−5.0	−5.0
4,000	−6.6	−6.6
5,000	−8.2	−8.2
6,300	−10.0	−10.0
8,000	−11.9	−11.9
10,000	−13.7	−13.7
12,500	−15.6	−15.6
16,000	−17.7	−17.7
20,000	−19.6	−19.6

TABLE 2: High Accuracy Circuit Performance Specifications

MC Nominal Input Level	−64dBu (0.5mV)
MC Input Impedance	100Ω
MM Nominal Input Level	−48dBu (3.0mV)
MM Input Impedance, Resistive	69kΩ or 47kΩ
MM Input Impedance, Capacitive	50pF to 350pF
Common-Mode Rejection (20Hz to 20kHz)	>50dB
Common-Mode Voltage Limit	±10V Peak
Nominal Output Level, Balanced	+8dBu/dBm
Max Output Level, Balanced	+30dBu/dBm
Output Impedance, Balanced	70Ω
Gain Control Range, Balanced	0.0dBu to 10dBu/dBm
Nominal Output Level, Unbalanced	−10dBu
Max Output Level, Unbalanced	+24dBu
Output Impedance, Unbalanced	1,000Ω
Output Voltage Slew Rate	>6V/ μs
RIAA Reproduction Characteristics (20Hz to 20kHz)	±0.25dB
RIAA/IEC Reproduction Characteristic (2Hz to 20kHz)	±1.0dB
Wideband Frequency Response (±1.0dB)	0.0Hz to 70kHz
Signal-to-Noise Ratio (20Hz to 20kHz)	>90dB
THD + Noise (20Hz to 20kHz +8dBu, Any Output)	0.01%
IMD (SMPTE 60Hz & 4kHz, 4:1)	0.02%

A PASSIVE MULTI-FILTER DESIGN

The Passive Split Multi-Filter RIAA/IEC Preamplifier design, shown in Figure 2, is intended for moving magnet (MM) input phono transducers. The design has an extremely low noise circuit topology, high accuracy passive RIAA/IEC equalization filters, and both unbalanced consumer and balanced output circuits. The input configuration utilizes the SSM-2015. It provides the lowest possible noise, adjustable resistive and capacitive input loading, and high accuracy passive RIAA filtering totally devoid of transient and frequency dependent gain errors.

Referring to Figure 2, the following two stages contain the RIAA-RIAA/IEC passive equalization filters. All high pass and low pass filters are passive. The signal is amplified by U_2 and U_3 SSM-2134 op amps. The overall gain of the circuit at 1,000Hz is 38dB. RIAA equalization requires a gain of 19.3dB at 20Hz, and attenuation of 19.6dB at 20,000Hz. Open-loop gain of U_2 and U_3 is greater than 100dB at 20Hz, and 60dB at 20,000Hz. Closed-loop gain of U_1 is 22.5dB, and U_2, U_3 is 16.6dB, ensuring an extensive gain margin for phase accuracy. Refer to Table 3 for complete circuit specifications.

TABLE 3: Passive Multi-Filter Circuit Performance Specifications

MM Nominal Input Level	–48dBu (3.0mV)
MM Input Impedance, Resistive	69kΩ or 47kΩ
MM Input Impedance, Capacitive	50pF to 350pF
Common-Mode Rejection (20Hz to 20kHz)	> 50 dB
Common-Mode Voltage Limit	±10V Peak
Max Output Level, Balanced	+30dBu/dBm
Nominal Output Level, Balanced	+8dBu/dBm
Output Impedance, Balanced	70Ω
Gain Control Range, Balanced	0.0dBu to 10dBu/dBm
Nominal Output Level, Unbalanced	–10dBu
Max Output Level, Unbalanced	+24dBm
Output Impedance, Unbalanced	1,000Ω
Output Voltage Slew Rate	>6V/μs
RIAA Reproduction Characteristic (20Hz to 20kHz)	±0.25dB
RIAA/IEC Reproduction Characteristic (2Hz to 20kHz)	±0.5dB
Wideband Frequency Response (±1.0dB)	0.0Hz to 70kHz
Signal-to-Noise Ratio (20Hz to 20kHz)	>90dB
THD + Noise (20Hz to 20kHz +8dBu, Any Output)	0.01%
IMD (SMPTE 60Hz & 4kHz, 4:1)	0.02%

TABLE 4: Uncomplicated Passive Circuit Performance Specifications

MM Nominal Input Level	–48dBu (3.0mV)
MM Input Impedance, Resistive	69kΩ or 47kΩ
MM Input Impedance, Capacitive	50pF to 350pF
Common-Mode Rejection (20Hz to 20kHz)	> 50dB
Commom-Mode Voltage Limit	±10V Peak
Max Output Level, Balanced	+30dBu/dBm
Nominal Output Level, Balanced	+8dBu/dBm
Output Impedance, Balanced	70Ω
Gain Control Range, Balanced	0.0dBu to 10dBu/dBm
Nominal Output Level, Unbalanced	–10dBu
Max Output Level, Unbalanced	+24dBu
Output Impedance, Unbalanced	1,000Ω
Output Voltage Slew Rate	>6V/μs
RIAA Reproduction Characteristic (20Hz to 20kHz)	±0.5dB
RIAA/IEC Reproduction Characteristic (2Hz to 20kHz)	±1.0dB
Wideband Frequency Response (±1.0dB)	0.0Hz to 70kHz
Signal-to-Noise Ratio (20Hz to 20kHz)	>90dB
THD + Noise (20Hz to 20kHz, +8dBu, Any Output)	0.01%
IMD (SMPTE 60Hz & 4kHz, 4:1)	0.02%

AN ECONOMICAL APPROACH

An Uncomplicated Passive RIAA/IEC Preamplifier is shown in Figure 3. It is a low cost, practical design for a passively equalized RIAA/IEC phono preamplifier. The design shown is for moving magnet (MM) input. It also is an extremely low noise input circuit design, and includes both unbalanced consumer and balanced output circuit configurations. The input circuit also utilizes the SSM-2015, and provides adjustable resistive and capacitive input loading. Wide bandwidth stages minimize in-band phase shift, and provide exceptional phase and frequency response accuracy. Table 4 details circuit performance data.

SUMMARY

For a phono transducer cartridge to deliver the performance as intended, it should be loaded with proper resistance and capacitance. The MM input circuits have adjustable transducer loading. Most transducers currently available will be accommodated with resistive loading of 69kΩ or 47kΩ, and capacitive loading of a few pF (input wiring dependent) to 350pF, in 50pF steps.

If greater input common-mode noise rejection is required, it can be obtained in all input designs by increasing the value of the 100Ω resistor and 0.1μF capacitor connected between the input RCA jack shield connection and the main circuit ground point. The values shown satisfy most requirements for 1 meter cables supplied with the newer tone arms.

All circuits described are signal noninverting, and constructed with bipolar IC amplifiers for lowest noise. They are compensated for widest bandwidth and circuit stability.

To achieve optimum trouble-free performance, a few construction and manufacturing tips should be observed. For grounding to be truly effective, all grounded components must return to a single point. This technique is effective in minimizing ground current loops that can cause excessive noise, signal cross-talk, AC power line noise, and circuit instability, and permit external noise spikes to enter. The ground center should be as close to the input amplifier (U_1) as possible. All grounded components of U_2, U_3, U_4, U_5, the output jack grounds, and the power supply ground lead should be tied to the same U_1 ground point.

As long as the power supply leads are kept short, and adequately filtered and bypassed with polyester film capacitor at the regulators, there is no need for individual decoupling capacitors at U_2, U_3, U_4, and U_5. The power supply voltages should be regulated for $\pm 18V_{DC}$.

All signal filter components should be of the highest quality, i.e., metalized polypropylene or polystyrene film, 1% tolerance capacitors (except for C_5, 5% tolerance is OK) and metal film resistors, 1% or better tolerance.

AN-125
A TWO-CHANNEL DYNAMIC FILTER NOISE REDUCTION SYSTEM

APPLICATION NOTE 125

In this application, the SSM-2120 Dynamic Range Processor and SSM-2134 op amp are utilized in a dual-channel dynamic noise reduction circuit, where the input signal level and threshold control determine the corner frequency of a low-pass filter.

The SSM-2120 contains two class A VCAs (Voltage Controlled Amplifiers) that are used as the filter's control element, and two wide dynamic range full-wave rectifiers with control amplifiers. The VCA section or variable resistor is a current device con-

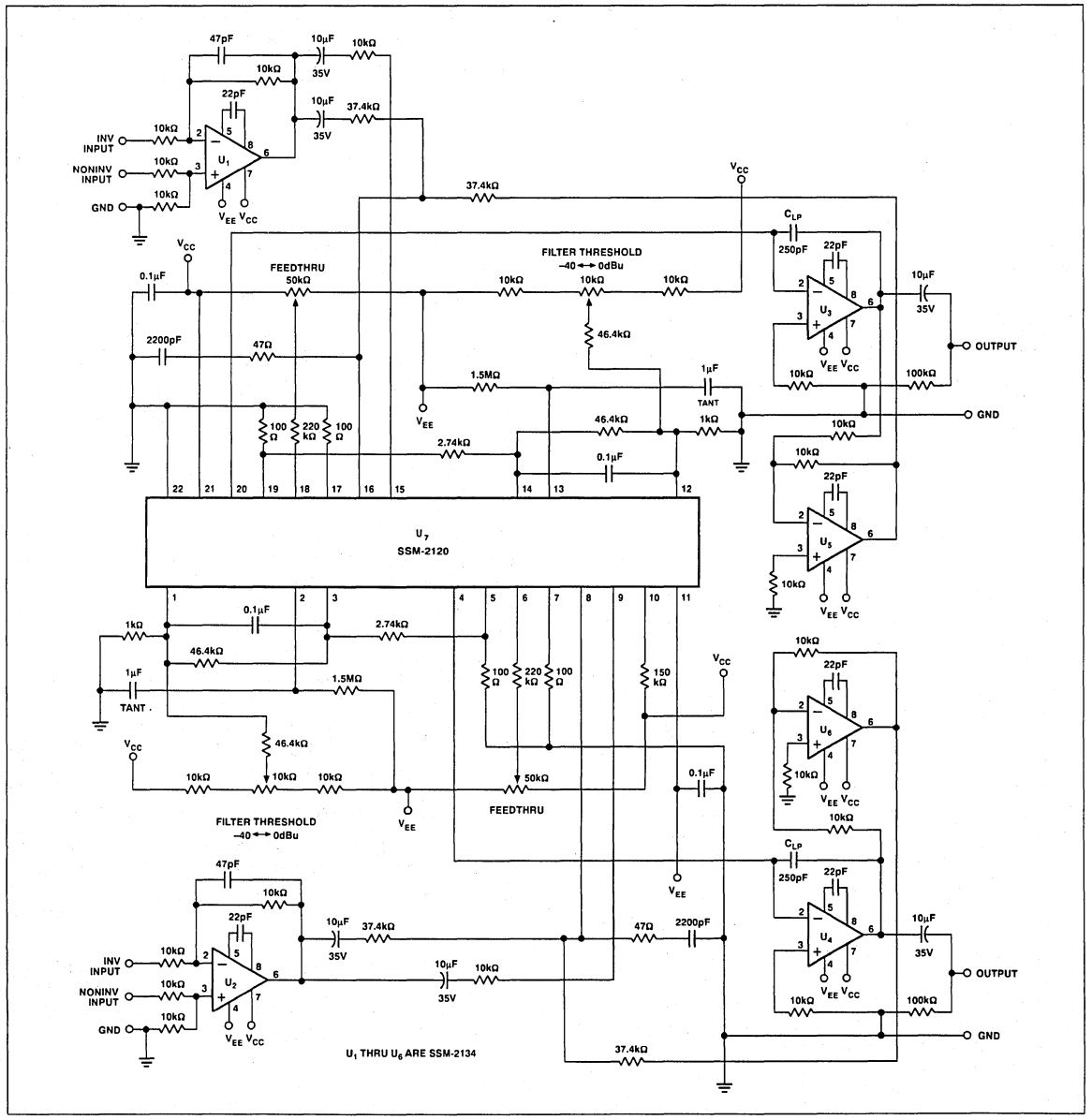


FIGURE 1: *Two-Channel Dynamic Filter Noise Reduction System*

trolled by the $+V_C$ voltage control ports. The VCAs are employed as variable resistor elements in a single pole low-pass filter operating in a virtual ground configuration. The level detecting rectifier is a full-wave averaging type with more than 100dB dynamic range, followed by a LOG amp converter. The part also contains two operational amplifiers with PNP output transistors used to drive the $+V_C$ ports.

U_1 and U_2 (SSM-2134) are input amplifiers and source-load isolating buffers. They provide a choice of noninverting, inverting, or balanced inputs. Unbalanced loading is 10kΩ and balanced loading is 20kΩ. U_1 and U_2 gain is set at 0dB, with a –10dBu nominal input signal recommended using $\pm 18V_{DC}$ power supply rails. This configuration will provide an overall circuit headroom of more than 30dB. In less critical applications, the feedthrough trim controls and 220kΩ resistors can be eliminated.

DETAIL CIRCUIT DESCRIPTION FOR U_7 (SSM-2120), AND U_3 & U_4

The rectifier circuit is configured to provide a negative control voltage referenced to ground. The LOG amplifier's bias is set by the 1.5MΩ resistor. The 1.5MΩ resistor also provides the discharge path for the 1μF rectifier averaging capacitor. The discharge time constant controls the low-pass filter's action toward a lower corner frequency. The LOG amplifier provides a constant current charging for the 1μF averaging capacitor. It results in an attack (return to flat response) time constant T_{C0} of approximately 6ms, and a low-pass filter activation T_{C1} of 350ms.

The internal op amp of U_7 has the gain V_G set at 47. The potentiometer at the inverting input provides the adjustable threshold to activate the filter. The threshold adjustment ranges from –40dBu to 0dBu of input signal level. The output from the op amp drive transistor supplies only a negative control voltage to the VCA ($+V_C$) control port(s). For example, with the filter threshold control adjusted to 0dB and a –10dBu signal applied to the input, f_{C1} is ≈4kHz; or with –20dBu applied, f_{C2} is ≈1.2kHz, both rolling off at 6dB/Octave. With the input signal level exceeding the filter threshold setting (0V VCA control voltage present), the overall circuit frequency response is 20Hz to 16kHz, at ±1dB.

The VCA audio input current is limited by the 37.4kΩ resistor. The VCAs operate as current devices whose outputs feed the virtual ground of an amplifier loop. The feedback capacitor around the amplifier loop sets up a single-pole low-pass filter. The SSM-2120 (U_7) inverts the signal current, therefore U_5 and U_6 are required to invert the output signal that is summed at the input(s) of U_7.

The design is an effective single-ended noise reduction circuit with low distortion and noise. When utilized on a noisy signal source, it will attenuate high frequency noise with inconspicuous operation.

TABLE 1: Circuit Performance Specifications

Nominal Input Voltage (–10dBu Out)	–10dBu
Headroom (–10dBu Out)	+30dBu
Input Voltage Range	–20dBu to +10dBu
Input Type/Impedance, Balanced	20kΩ
Input Type/Impedance, Unbalanced	10kΩ
Dynamic Noise Reduction Class	Dynamic Low-Pass
Filter Activate Time Constant (6dB)	350ms
Threshold Range (Level)	–40dBu to 0dBu
Filter Deactivate Time Constant	6ms
Signal Rectifier Type	Full Wave Averaging
Modulation Feedthrough, Trimmed	–100dB
Frequency Response (20Hz to 16kHz)	±1dB
Filter Type, Low-Pass	Single Pole, 6dB/Oct
Input 10dB Below Threshold Setting	f_{C1} = 3,800Hz
Input 20dB Below Threshold Setting	f_{C2} = 1,400Hz
Dynamic Range @ 0dB Gain (Ref. +22dBu)	106dB
THD + Noise (20Hz to 20kHz)	0.02%
IMD (SMPTE 60Hz & 4kHz, 4:1)	0.05%
Output Voltage (2kΩ Load)	+22dBu
Output Type	Unbalanced
Power Supply	$\pm 18V_{DC}$ Regulated

AN-127

AN UNBALANCED MUTE CIRCUIT FOR AUDIO MIXING CHANNELS

APPLICATION NOTE 127

This application note describes a dual channel unbalanced analog audio mute switch, for use in audio console mute circuits. The SSM-2402 dual audio switch, when used in the virtual ground configuration, truly enhances any audio mute design. The application, as shown in Figure 1, incorporates unbalanced stereo input buffers, dual stereo electronic virtual ground switches (with simplified control circuit), and virtual ground summing amplifiers.

THE AUDIO SWITCH AS IMPLEMENTED

The design utilizes the SSM-2402 (U_1 and U_2) dual audio switch in a virtual ground switching configuration. This method of operation improves linearity over a wide dynamic range. The SSM-2402 utilizes JFET switching, with internal wide bandwidth integrated amplifiers applied in a unique configuration. The result is low transient intermodulation distortion, low THD, and low IMD, while essentially eliminating all audio switching

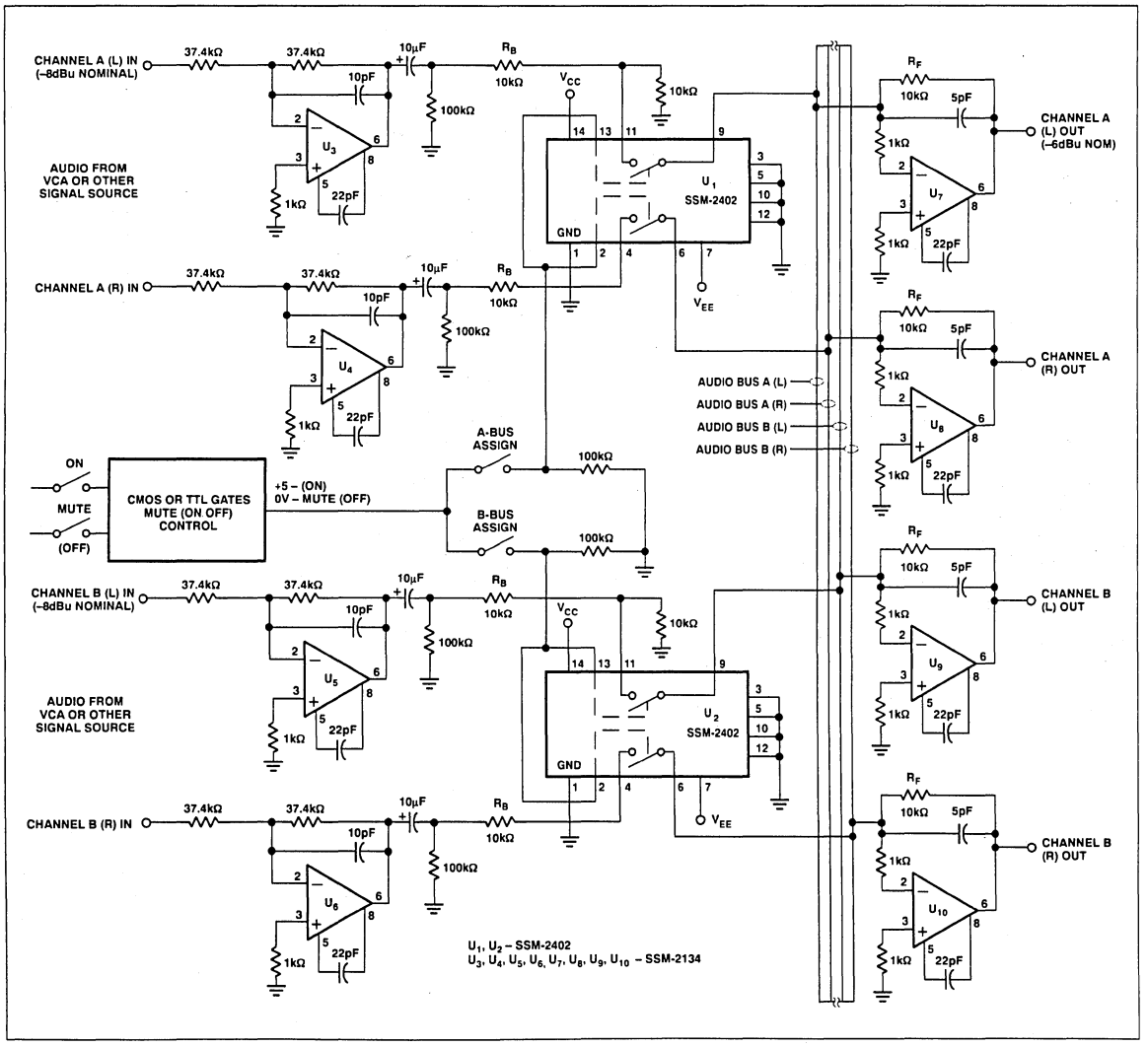


FIGURE 1: *Audio Mixer Channel Mute (On/Off) Circuit (Unbalanced Design with Virtual Ground Switching)*

transients. The SSM-2402 switch closed (ON) resistance is typically 60Ω in series with R_B (10kΩ). As shown in this mixing system, the tolerance of the 60Ω contributes to less channel imbalance than the 1% resistor tolerance, thus eliminating the need for level trim adjustments.

The SSM-2402 employs a "T" switching configuration that yields superior ON-OFF signal isolation. In the OFF state, the "T" configuration of the SSM-2402 virtually eliminates leakage of the input signal (down more than 100dB at 1kHz with guard pins 3, 5, 10 and 12 grounded) onto the mixing bus(es). The part also features a 7ms ramped turn ON and 4ms ramped turn OFF, for transient free audio switching even with signal applied. The switch also operates with a break-before-make switching sequence. These properties are significant when many remotely controlled electronic switches are connected in series and controlled by a single device, as in large audio systems managed by an automation computer.

CONTROL INTERFACE

In this application note, the bus assignment (selection) switches are shown functionally for clarity. The control ports of the SSM-2402 can easily be interfaced to conventional 5V TTL or CMOS logic control circuits. $+5V_{DC}$ (logic high) closes the switch (ON), and $0V_{DC}$ (logic low) opens the switch (OFF). The common interface levels improve the reliability and serviceability of any products it's designed into. Diverse logic gate control designs or computer controlled schemes can easily be implemented.

DRIVE REQUIREMENTS – THE INPUT CIRCUIT

The application employs two SSM-2402 dual audio switches in a four-bus configuration (two stereo buses) driven by U_3, U_4 and U_5, U_6 bipolar amplifiers. The buffer amplifiers are signal inverting, with their gain set to 0dB (A_V = 1). The input amplifiers also serve as source signal level clippers that prevent the input signal from exceeding the input range of the switches, thus preventing the switches from passing a distorted signal when overdriven in the open (OFF) state. A nominal input drive level of –10dBu is applied to the switch and will maximize the signal-to-noise ratio, and optimize headroom. The output of U_3, U_4, U_5, and U_6 are AC coupled to further minimize the switching transient noise caused by signal path DC voltages from previous origins.

The virtual ground mixing buses are current driven by R_B (10.0kΩ) resistors. Once again, this is a compromise value that can be changed to accommodate the extent of the mixing bus implemented. A greater number of input mixing channels will warrant a lower bus drive current. Although other values can be used, the resistance values of R_B and R_F should be the same.

As shown ($\pm 18V_{DC}$ power) R_B will apply approximately 1.7mA peak current to the mixing bus. This is well within SSM-2402 switching capabilities, as well as the SSM-2134 drive capabilities. The signal current is low enough to keep return ground currents low enough to prevent crosstalk as a result of the mechanical wiring constraints. Returning ground currents independently to the noninverting input of the summing amplifier is advised.

THE OUTPUT SUMMING AMPLIFIER

The design utilizes the SSM-2134, the PMI version of the popular NE5534 bipolar operational amplifier. The circuit features a significant reduction in summing amplifier noise, a decrease in temperature and bus impedance effects on the static output voltage as a result of using a bipolar amplifier. This design also balances the input circuit reflected source impedance of the bipolar IC amplifier, alleviating the unity-gain instability and eliminating the unbalanced input topology for inverting summing designs that could cause output offset.

The SSM-2134 has a noise voltage of 2.8nV/ $\sqrt{\text{Hz}}$, thus the noise floor is reduced by 3 to 10dB. Additionally, frequency and phase response performance have been improved. Only minimal compensation is required in the feedback loop of the SSM-2134 to maintain unconditional stability. The slew rate remains greater than 10V/μs, with bandwidth exceeding 50kHz.

SUMMARY

The design application shown in Figure 1 is signal noninverting, and utilizes a minimum number of noise generating elements. The circuit configuration produces linear signal mixing at the virtual ground summing node ($e_S = 0V_{AC}$), therefore, no reflected interaction occurs between the input sources. The signal input to any output frequency response is typically 10Hz to 50kHz, ±0.5dB. Total harmonic distortion plus noise will measure less than 0.01%, from 20Hz to 20kHz, SMPTE intermodulation distortion is less than 0.02%. With prudent printed circuit board design, a greater than 100dB mute isolation @ 1kHz can be obtained.

The application shown employs $\pm 18V_{DC}$ power supplies to produce a +24dBu audio output clip level. All SSM components will operate with equal reliability at $\pm 20V_{DC}$, producing approximately a 1dB increase in clip level. If the extra headroom is necessary, a $\pm 20V_{DC}$ power supply voltage is encouraged. The noise increase will be indiscernible, even in large mixing systems.

AN-128
A TWO-CHANNEL NOISE GATE

APPLICATION NOTE 128

This application applies the SSM-2120 as a dual-channel noise gate or adjustable threshold downward expander. A noise gate is a type of noise reduction system that fully attenuates a VCA when no audio signal is present. The SSM-2120 contains two class A VCAs (Voltage Controlled Amplifiers) and two wide dynamic range full-wave rectifiers and control amplifiers. The VCA section is a current amplifier device whose gain is controlled by two gain ports that have dB/V scaling. The VCAs are employed as wide bandwidth amplifiers with the current inputs and outputs operating in a virtual ground configuration. The rec-

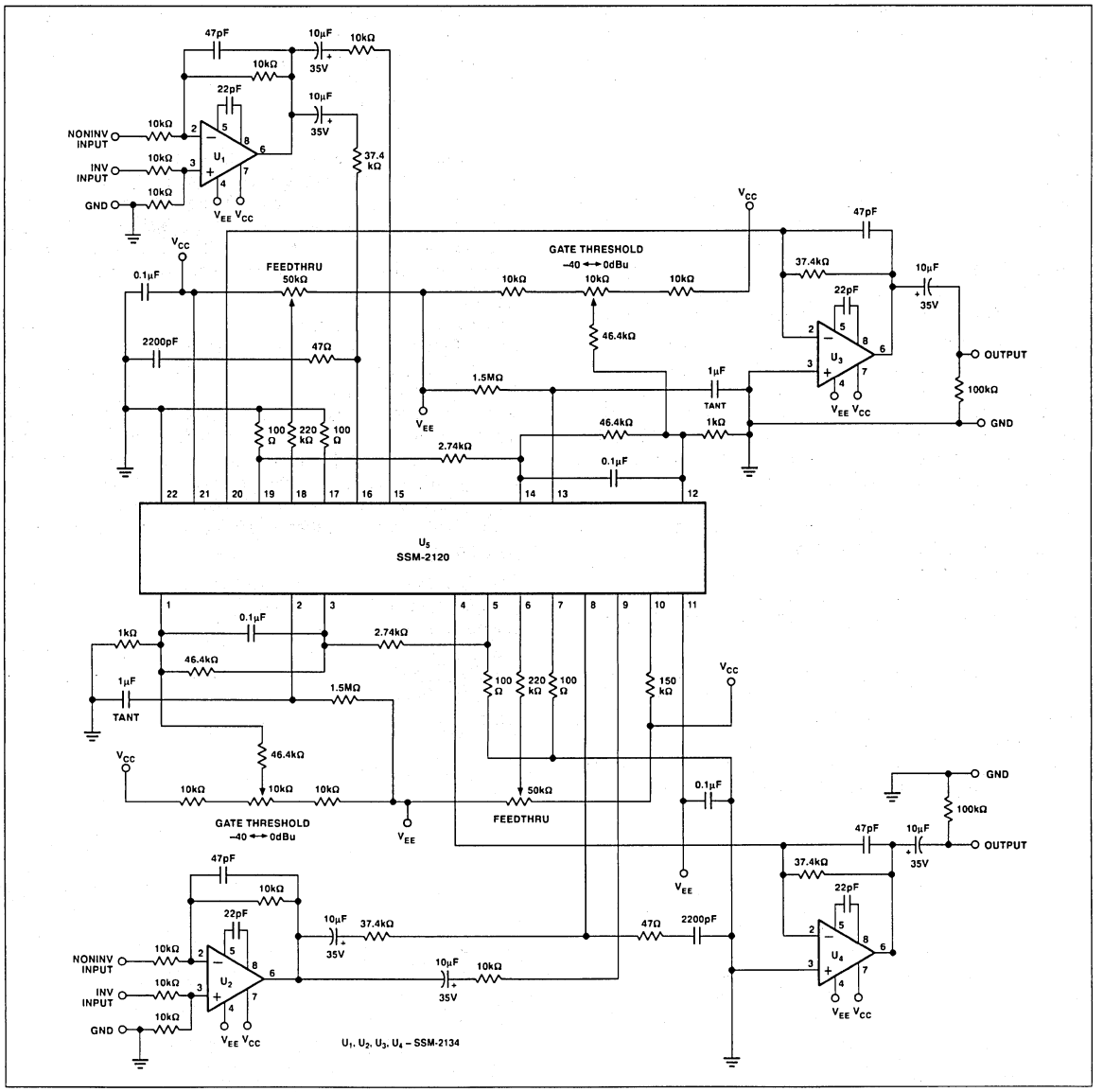


FIGURE 1: *Two-Channel Noise Gate*

tifiers are full-wave averaging type with 100dB dynamic range, followed by LOG converters. The part also contains two operational amplifiers with PNP output transistors connected in a common collector configuration.

Two SSM-2134s are used as input amplifiers, U_1 and U_2, to provide noninverting, inverting, or balanced inputs. Unbalanced loading is 10kΩ and balanced loading 20kΩ. U_1 and U_2 gain is set at 0dB, and with a –10dBu nominal input signal and $\pm 18V_{DC}$ power, will provide overall circuit headroom of 30dB. The VCA(s) could be DC coupled, although in this application they are AC coupled to reduce the dependence on trimming the side chain voltage modulation feedthrough. In critical applications the feedthrough trim controls and 220kΩ resistors should be added.

The SSM-2120's internal rectifier produces a negative DC voltage referenced to ground. The LOG amplifier bias is set by the 1.5MΩ resistor. The 1.5MΩ resistor also provides the discharge current path for the 1μF capacitor, that controls the gate's downward expansion time constant. The LOG amplifier provides a constant current capacitor charging value. It results in an attack (return 0dB gain) time constant T_C of approximately 6ms, and a downward expansion T_C of 350ms.

The internal op amp gain A_V is set at 47, with the inverting input also providing the reference voltage. The reference voltage range from the gate threshold control allows the gating to activate at any source signal level from –40dBu to 0dBu. The output from the op amp drive transistor supplies a negative control voltage to the VCA ($+V_C$) control port(s). The VCA(s) control ports have a sensitivity of 6mV/dB. As shown, the voltage divider provides a 2:1 downward expansion slope. Below the threshold level, the gain slope is $2dB_G/dB_{IN}$.

The VCAs are current output amplifiers that are designed to operate with virtual ground configurations such as U_3 and U_4. The VCA input current is supplied by the 37.4kΩ resistor and input voltage signal. The virtual ground amplifier feedback resistors are 37.4kΩ. With no VCA control voltage, the overall circuit voltage gain is 1 (0dB). Other non-gating gains can be attained by changing the output amplifiers feedback resistor value. The VCA input resistor should remain as shown for maximizing the performance of the VCA(s).

TABLE 1: Circuit Performance Specifications

Nominal Input Voltage (–10dBu Out)	–10dBu
Headroom (–10dBu Out)	+30dB
Input Type/Impedance, Balanced Unbalanced	20kΩ 10kΩ
Downward Expander Class	Feedthrough
Threshold Sense Time Constant (6dB)	350ms
Threshold Range (Level)	–40dBu to 0dBu
Gate Deactivate Time Constant	6ms
Signal Rectifier Type	Full-Wave Averaging
Modulation Feedthrough, Trimmed	< –60dBV
Gain Reduction Ratio, Downward Expansion	1 to 2 (–2dB/dB)
Frequency Response (20Hz to 20kHz)	±0.25dB
Dynamic Range	100dB
THD + Noise (20Hz to 20kHz)	0.02%
IMD (SMPTE 60Hz & 4kHz, 4:1)	0.05%
Output Voltage Slew Rate	6V/μs
Output Voltage (2kΩ Load)	+22dBu
Output Type	Unbalanced
Power Supply	$\pm$ 18V_{DC} Regulated

AN-129

A PRECISION SUM AND DIFFERENCE (AUDIO MATRIX) CIRCUIT

APPLICATION NOTE 129

When constructing an accurate sum and difference signal from stereo left and right sources, amplitude and phase (delay) errors can contribute substantial amounts of crosstalk in the reconstructed left and right audio channels. A minor 1dB difference, or 6° phase error, will result in only 25dB stereo channel separation. The design presented has essentially no phase or group delay in the sum or difference outputs as measured over the audio spectrum, 20Hz to 20kHz. This circuit utilizes matched (laser trimmed) resistor networks combined with high open-loop gain differential amplifiers to guarantee virtually no phase and amplitude error in the sum and difference channels.

Amplifiers U_3 and U_4 (SSM-2134) are utilized as input signal buffers that provide a low source impedance (0Ω) to the 10kΩ summing resistors that feed the virtual ground current summing

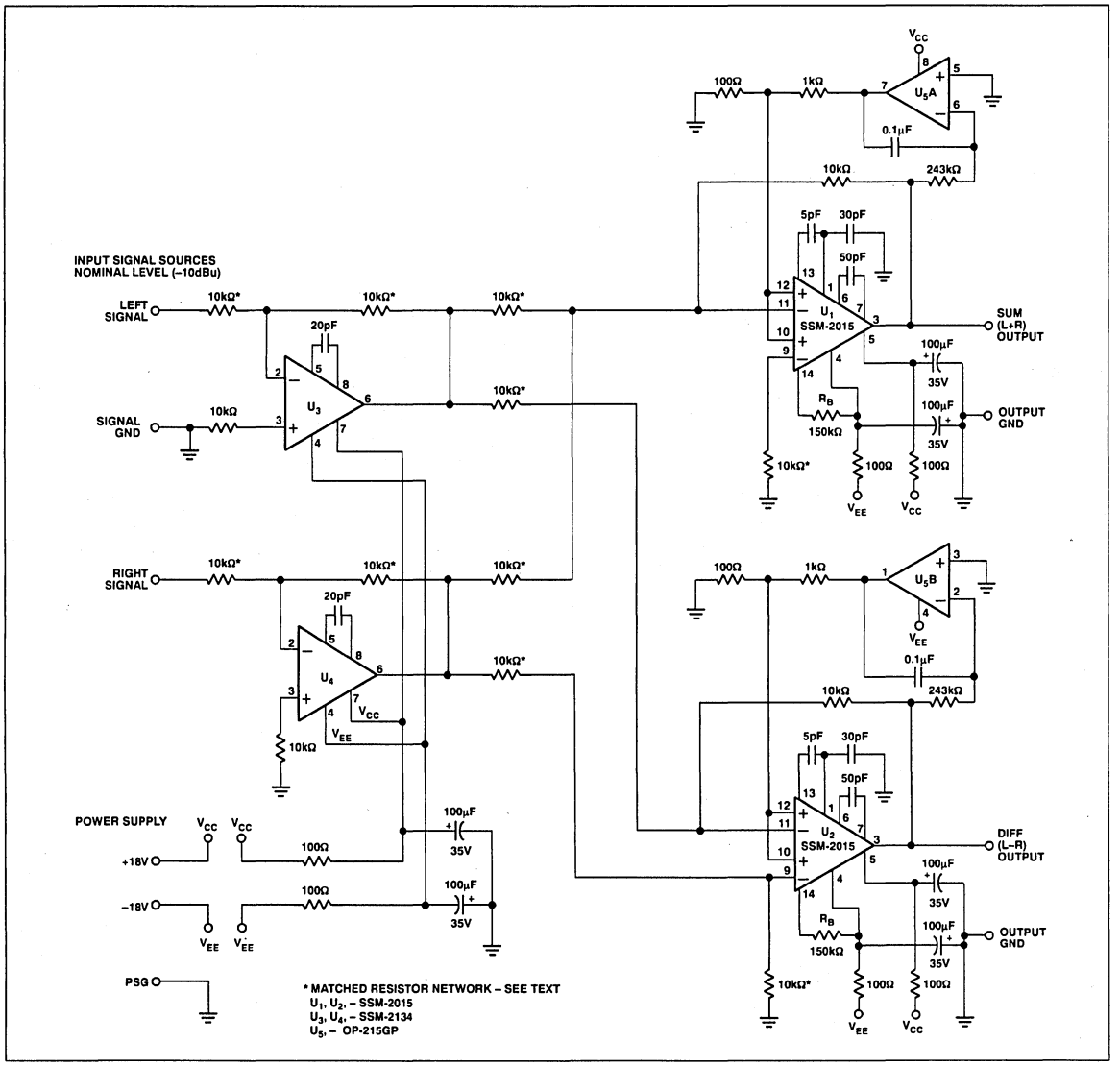


FIGURE 1: *Precision Sum and Difference (Audio Matrix) Circuit*

nodes of U_1 and U_2. The overall gain of the buffer circuit is 0dB. The buffer amplifiers, U_3 and U_4, are compensated for a frequency response that extends to 100kHz at +24dBu. The buffers are configured as inverting amplifiers for lowest phase and group delay effects.

U_1 and U_2 (SSM-2015) are true differential input, high performance bipolar amplifiers. The current summing inputs have been employed for sum and difference operations. All bipolar and JFET op amps exhibit considerable propagation time differences between inverting and noninverting inputs, which result in phase and group delay errors. The SSM-2015 was selected because this device has practically equal propagation time between inverting and noninverting inputs (typically less than 10ns differential). This important characteristic produces high accuracy L + R and L – R signals. Because U_1 and U_2 are ultra-low noise audio preamplifiers, they contribute little noise and distortion to output signals.

U_5 (OP-215GP) is a dual JFET amplifier, and is utilized as a long time constant integrator, or DC servo amplifier. The noninverting input is referenced to ground ($0V_{DC}$) and will hold the output terminals of U_1 and U_2 at $0V_{DC}$. Capacitor (AC) coupling is not recommended as it would allow formation of envelope and low frequency group delay distortion.

CONSTRUCTION REQUIREMENTS

All 10kΩ resistors need to be matched within 0.05% of each other, but can be 5% in value tolerance. The 0.1μF capacitor in the integrator circuit should be a metalized polyester film capacitor with 10% tolerance. The power supply rails are regulated at $\pm 18V_{DC}$.

TABLE 1: Circuit Performance Specifications

Frequency Response (± 0.02dB)	20Hz to 20kHz
Dynamic Range (20kHz Bandwidth)	104dB
THD + Noise (20Hz to 20kHz, +24dBu)	0.007%
IMD (SMPTE 60Hz & 4kHz, 4:1, +24dBu)	0.015%
Slew Rate	10V/μs
Nominal Signal Level	–10dBu
Maximum Output Voltage (2kΩ Load)	+23.3dBu or $11.3V_{RMS}$
Amplitude Accuracy	0.05%
Differential Error	<10ns

PMI

Audio Silicon Specialists™

AN-130

A TWO-BAND AUDIO COMPRESSOR/ LIMITER

Precision Monolithics Inc.

APPLICATION NOTE 130

The two-band audio compressor amplifier shown in Figure 1 features separate and adjustable signal compression ratios and threshold levels. This design employs the SSM-2120 Dynamic Range Processor, and SSM-2134 low noise op amps.

The design features: an inverting or noninverting input buffer amplifier; high-pass and low-pass filters; and a voltage-controlled amplifier driven by a log-average level detector with a full-wave rectifier. Additionally, there are fully adjustable gain reduction controls, and adjustable compression threshold level controls. Signal-to-noise ratio exceeds 100dB, while the level detector allows the compressor to operate transparently throughout the audio spectrum without interaction between high and low bands.

The circuit includes a line level input (–10dBu to 0dBu nominal) buffer amplifier, with inverting or noninverting inputs that have 10kΩ input impedance. The buffer also limits step-function slewing voltages from entering the next stage and isolates the input source from the high-pass and low-pass filter stages.

Both high-pass and low-pass filters are of the single-pole type. This filter class is utilized to eliminate combing effects in the stop bands, and to compensate for compressor artifacts when the two bands are summed back together in the output amplifier stage. Such artifacts include the compressor's effect on the amplitude of each independent band, and the filter's effect on the summing influence has been taken into account in the design.

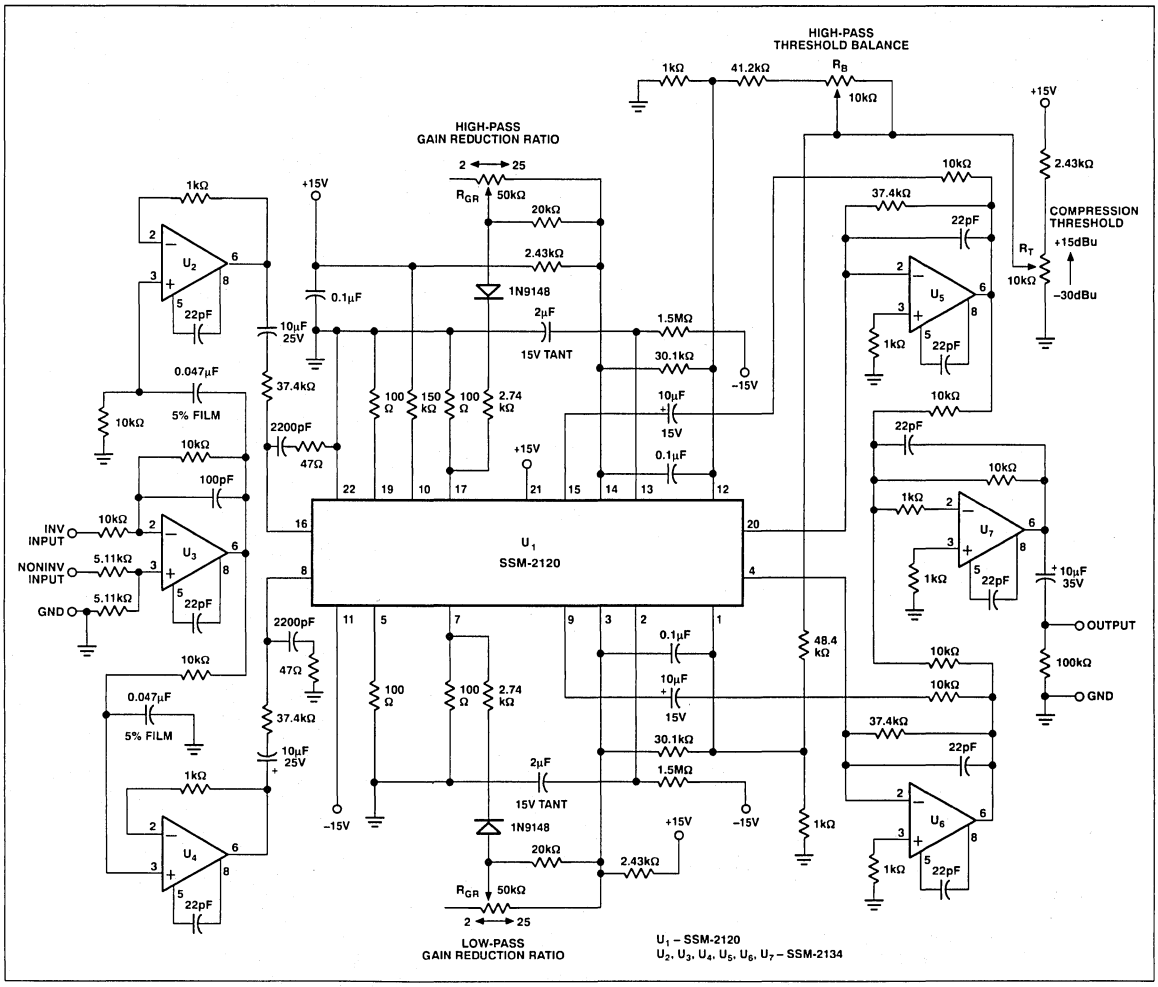


FIGURE 1: *Two-Band Audio Compressor*

Two continuously variable gain reduction controls (R_{GR}) in the VCA control circuit provide independent adjustment of compression gain slopes. The GAIN REDUCTION ratios are each adjustable from 2 to 25 for high-pass and low-pass bands. This range of adjustment provides mild compression to severe limiter/clipper action independently on each band. Thus the irritating "hole producing and pumping" character of single, wide-band compressor circuits can be reduced. The SSM-2120 provides a dynamic range of greater than 100dB over the frequency range of 20Hz to 20kHz with typically less than 0.02% THD + noise, and 0.05% IMD.

The COMPRESSION THRESHOLD control (R_T) allows the compressor to take effect from – 30dBu to +20dBu input levels. The SSM-2120's log-average precision rectifier is configured as a feedback-type level detctor. The design produces consistent and precise compression profile of the input signal with no threshold level or compression drift over time and temperature.

The SSM-2120's full-wave log-averaging rectifier and control amplifier form an integrator and buffer circuit that isolates the low impedance VCA control port from the integrator timing circuit. This circuit senses the VCA output level and modifies its compression profile by feeding the averaged VCA signal plus the compression threshold control signal back into the VCA control ports. The control R_B is used to balance the threshold amplitude between the two bands to pre-establish the compressor dynamics.

The small signal averaging time for the 2μF integration capacitor shown is 12ms. The attack time to 3dB of final value is about 6ms and is almost independent of signal level increase for level changes in excess of +10dB. The compression release rate is controlled by the 1.5MΩ discharge resistor in the integrator circuit. The recovery time constant is nearly linear since the discharge resistor returns to the $-15V_{DC}$ rail, and the rectifier produces a positive control voltage.

TABLE 1: Circuit Performance Specifications

Input Voltage Range (Nominal for 0dBu Out)	–10dBu to 0dBu 245mV to 755mV
Rectifier Type	Averaging
Compressor Amplifier Class	Feedback
Attack Time (+10dB or Greater Level Change)	6ms
Recovery Rate	1.67dB/ms
Feedthrough, Trimmed	–100dB
Gain Reduction Range	2 to 25
Frequency Response (20Hz to 20kHz)	0.2dB
Dynamic Range @ 0dB Gain	100dB
THD + Noise (20Hz to 20kHz)	0.02%
IMD (SMPTE 60Hz & 4kHz, 4:1)	0.05%
Output Voltage Slew Rate	6V/μs
Output Voltage (2kΩ Load)	+22dBu or $10V_{RMS}$

PMI

Audio Silicon Specialists™

AN-131

A TWO-CHANNEL VCA LEVEL (VOLUME) CONTROL CIRCUIT

Precision Monolithics Inc.

APPLICATION NOTE 131

The dual-channel voltage-controlled amplifier (VCA) level control circuit describes a useful application of the SSM-2122 dual VCA, SSM-2134 low noise op amp, and PMI's OP-215BP JFET/bipolar op amp. This circuit is very handy when extremely close gain matching of a stereo audio source is desired, such as in ON-AIR and production audio consoles.

The design features a balanced input buffer amplifier and VCA driven by a level shifting amplifier which is controlled by a single 10kΩ linear potentiometer. Additionally, there are fully adjustable and independent gain limit and maximum attenuation trim controls. The VCA circuit has a nominal attenuation range greater than 95dB and has input overdrive protection. The signal-to-noise ratio exceeds 100dB with a gain of 10dB, and headroom of 32dB. The amplitude varies less than ±0.1dB over the frequency range 20Hz to 20kHz. Typical THD and IMD are less than 0.005% and 0.02%, respectively.

As shown, the circuit includes two line-level inputs designed for a –10dBu input signal level. The SSM-2134 (U_2 and U_4) input buffer amplifiers can be connected for balanced or unbalanced inputs with inverting or noninverting inputs. The input loading impedance is 10kΩ unbalanced and 20kΩ balanced. The input buffer amplifier also limits step function slewing voltages from entering following stages. Other input levels can be accommodated by adjusting the feedback resistor R_{F2}. For example: for a nominal input level of 0dBu, R_{F2} should be changed to 3.16kΩ, or for a nominal input level of +10dBu, R_{F2} changed to 1kΩ to provide the optimal current drive to the VCA. C_F should also be changed to 68pF and 220pF respectively for both U_2 and U_3.

For other input levels, R_{F2} can be calculated:

$$R_{F2} = 10 \times 10^3 \times \text{EXP}\left(\frac{10 + \text{dBu}}{-20}\right)$$

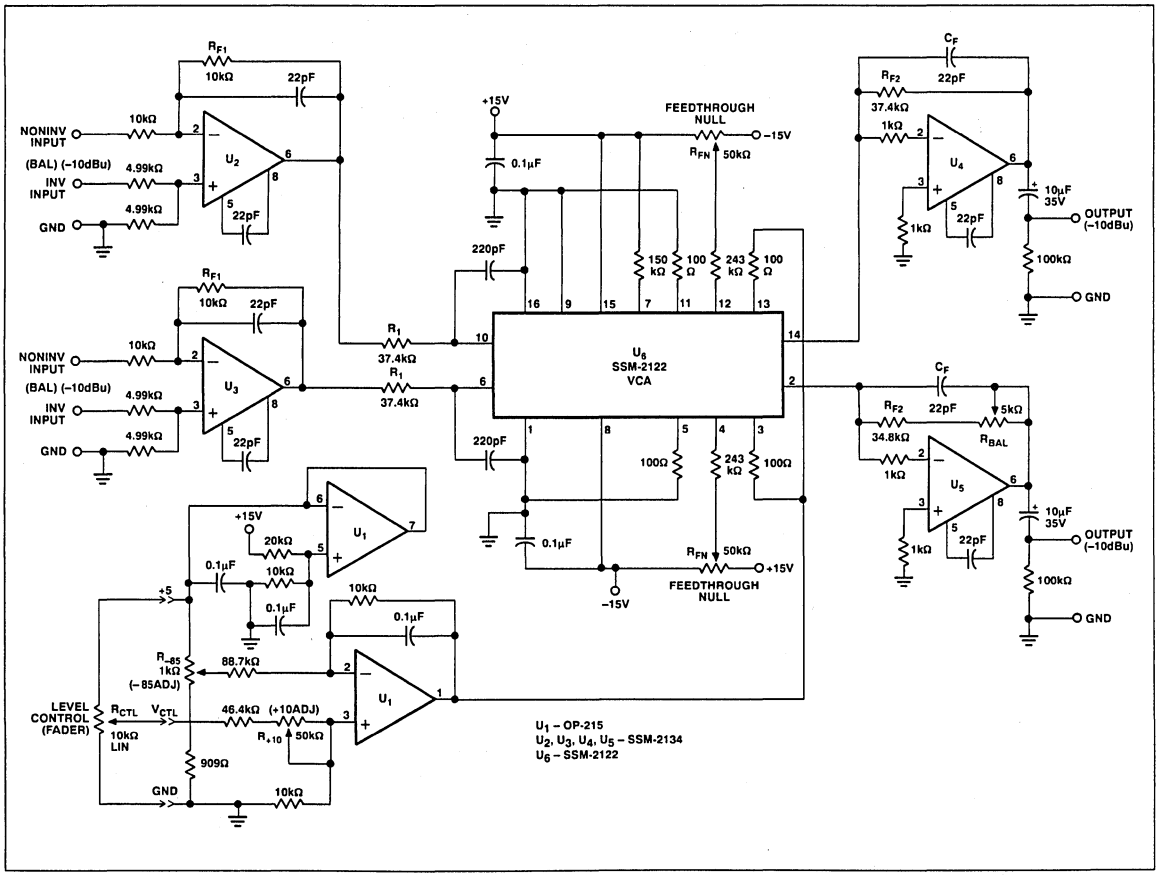


FIGURE 1: *Two-Channel VCA Level Control*

The SSM-2122 has a current-in and current-out structure. The input current is set by resistor R_1 and the virtual ground input of the SSM-2122. Similarly the transimpedance amplifier at the output converts the output current into a voltage. All devices in this design operate on $\pm 15V_{DC}$ power supply rails. The 37.4kΩ VCA input and output resistors optimize its dynamic range and minimize distortion. The SSM-2122 is a monolithic device, so the VCA gains remain uniform over a wide change in ambient temperature.

The SSM-2122 has two gain control ports that have a sensitivity of –6mV/dB. 0.0 volts at the gain control ports will yield 0dB overall gain; +60mV produces +10dB gain and –0.513V corresponds to a –85dB attenuation. The feedthrough trim null controls R_{FN} are not imperative for most applications. However, for very high performance requirements they will reduce attenuation control voltage feedthrough to less than 750μV. To adjust the null trim controls R_{FN}, inject a 100Hz sinewave into the control port through a 1kΩ resistor and a 100μF, 10V capacitor, and set the signal generator to 0.5 V_{RMS}. The control ports of U_6 are pins 3 and13. Adjust the level control R_{CTL} (fader) for 0dB gain, with the signal inputs shorted, then adjust R_{FN} for minium 100Hz signal at the outputs.

The output amplifier(s) U_4 and U_5 are virtual ground connected current-to-voltage converters. The 37.4kΩ feedback resistors set the circuit voltage gain to 0dB with zero volts applied to the VCA control ports. Variable resistor R_{BAL} is used to balance the signal path gain of the two audio circuits. With the circuit gain set to 0dB and a test signal applied to the inputs, R_{BAL} is adjusted for equal output levels.

The VCA provides 10dB of additional gain at maximum level setting (+60mV at the VCA control ports). The THD is extremely low within the characteristic gain range of +10dB to –20dB.

The VCA control circuit is designed around U_1, the high input impedance OP-215 dual op amp. One half of U_1 is used to develop the 5V reference voltage for the level control element.

This is a fail-safe design – with no voltage applied or an open connection at terminal V_{CTL}, the gain will descend to –85dB. Level control trimming is as follows: with the fader control set to minimum (0V), the trim control R_{-85} is adjusted for maximum attenuation of –85dB or $-0.513V_{DC}$ at pin 1 of U_1. Then with the fader set to its maximum (5V), trim control R_{+10} is adjusted for maximum circuit gain of +10dB or +60mV. Since there is no interaction when adjusting R_{+10} for +10dB gain, the setting for R_{-85} will remain unaffected. Other max-attenuation values can be used. R_{-85} has an attenuation range of –45dB(270mV) to –93dB (560mV).

TABLE 1: Circuit Performance Specifications

Input Voltage (Nominal for –10dBu Out)	-10dBu or $245mV_{RMS}$
Input Impedance, Unbalanced	10kΩ
Imput Impedance, Balanced	20kΩ
Headroom (Nominal for –10dBu In &Out)	32dB
Feedthrough, Trimmed	<750μV
Gain Control Range (Nominal)	+10dB to –85dB
Gain Control Voltage (+10dB to –85dB)	$5V_{DC}$ to $0V_{DC}$
Frequency Response (20Hz to 20kHz)	±0.1dB
S/N Ratio @ 10dB Gain	100dB
THD + Noise (20Hz to 20kHz, +22dBu)	0.005%
IMD (SMPTE 60Hz & 4kHz, 4:1, +22dBu)	0.02%
Output Voltage Slew Rate	6V/μs
Output Voltage (1kΩ Load)	+22dBu or $10V_{RMS}$
Output Impedance	<10Ω

AN-133

A HIGH-PERFORMANCE COMPANDOR FOR WIRELESS AUDIO SYSTEMS

Precision Monolithics Inc.

APPLICATION NOTE 133

Wireless audio systems are finding increasing use in live performances, as well as in communications equipment where mobility is required. Designing such systems present a difficult challenge: how to maintain adequate audio performance in view of power supply and current consumption limitations. To reduce transmission noise, the audio signal is usually compressed at

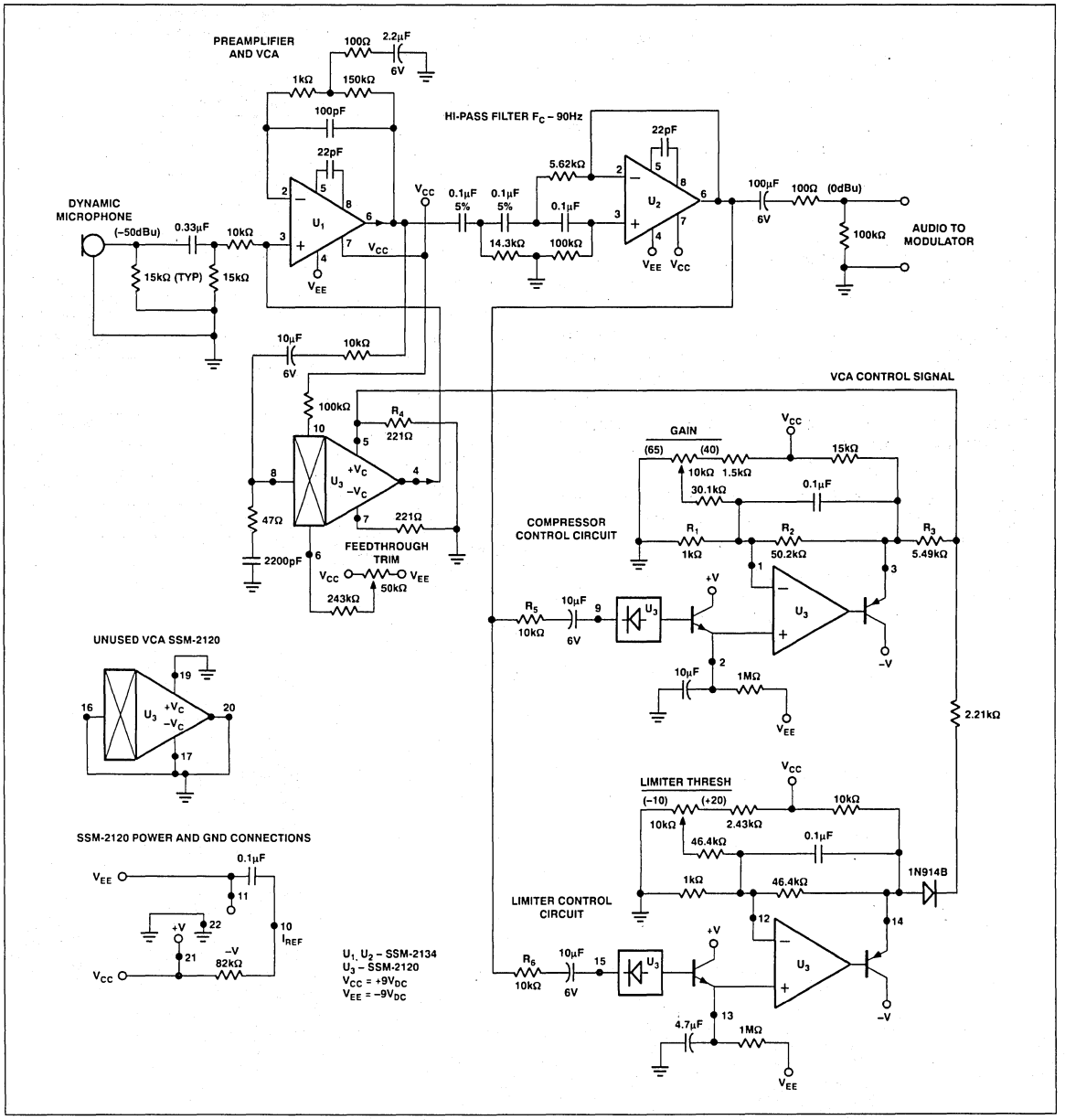


FIGURE 1: *Compressor-Limiter Circuit for Transmitter*

the transmitter and expanded at the receiver by using a telecommunications industry-standard compandor IC, which has marginal audio performance as measured by professional standards. This application note describes a companding system utilizing the SSM-2120 Dynamic Range Processor which permits considerable improvement over other techniques in terms of noise, distortion, feedthrough, and other key audio criteria.

Transmitters are battery powered, and hence pose the most severe constraints on supply voltages and current consumption. Receivers are often AC powered, so bipolar supplies are more easily accommodated. Since the SSM-2120 requires split supplies, a voltage doubler circuit is necessary for the transmitter. In some cases, this may be considered unfeasible. In this event, however, the SSM-2120 is still very useful in the receiver expander circuit to complement any compressed signal, and improve overall system performance. As a result, the compressor and expander sections of this application can be considered independent.

THE TRANSMITTER COMPRESSOR AND LIMITER CIRCUITS

COMPRESSOR

The design described is intended for $\pm 9V_{DC}$ battery operation, and includes a third order high-pass filter for the elimination of subsonic noise and low frequency pops that would cause compandor overload or mistracking.

Figure 1 shows the connection of the SSM-2120 (U_3) VCA_1, rectifier, and control amplifier as a compressor. The VCA is connected in the feedback loop of the preamplifier U_1 to control the gain. The compressor is designed for a 2:1 compression characteristic. If the input rises 6dB, the output level will rise only 3dB. The gain compression expression is:

$$\text{Gain}_{\text{reduction ratio}} = \frac{R_2 \cdot R_4}{R_1 \cdot R_3}$$

as long as the rectifier input currents are limited by R_5, R_6 (10kΩ) , and the rectifier has a ≈10μA reference current. The SSM-2120 rectifier and VCA have a dynamic range in excess of 100dB, resulting in exceptional tracking of the expander/compressor in the compandor system. High quality capacitors and resistors should be used to support the accuracy of the SSM-2120 elements. The small-signal averaging time for a 10μF integration capacitor is 25ms. The attack time to 3dB of final value is also about 26ms and is almost independent of signal level increases for level changes in excess of +10dB. The decay rate is 3ms per dB. The high-pass filter keeps frequencies below 90Hz from the input of the rectifier, reducing the low frequency distortion caused by the VCA control circuit.

DC and high-frequency feedback are provided for U_1 without sacrificing bandwidth or stability. The gain control is adjusted for 0dBu output with -50dBu applied to the microphone input terminals. The VCA is signal inverting. Its output current is summed, along with the microphone signal current, at the (virtual ground) noninverting input of preamplifier SSM-2134, U_1. The 10kΩ resistor at the input of the VCA limits the input current, while the 2200pF, 47Ω network provides frequency compensation for the VCA, keeping it stable.

The 100kΩ resistor from V_{CC} to pin 10 of U_3 establishes the operating current for the VCA. To minimize power supply current, all pins of the unused VCA should be returned to ground. The FEEDTHROUGH trim control is optional, and it can be used to minimize the VCA control voltage from feeding through to the output.

PROTECTION LIMITER

The limiter uses the second rectifier and control amplifier for separate and independent attack and decay times, along with a steeper gain reduction slope. The limiter threshold control sets the predetermined gain limiting point for high input signal levels. The gain reduction ratio is 4.6:1 as shown in Figure 1. Typically the onset of gain limiting should be set to +10dBu at the output.

As in the compressor control circuit, the rectifier input current is limited by R_6, 10kΩ, and the rectifier referenced to ≈10μA as well. Lower precision capacitors and resistors can be used here. Similar to the compressor, the attack time is much faster than the decay.

The VCA/Preamplifier was designed as a system. The VCA was put in the signal feedback loop of the preamplifier principally to prevent preamplifier overload, while keeping the overall noise low, and minimizing component count.

POWER SUPPLY

The application circuit requires two power supply voltages, $\pm 9V_{DC}$. The power consumption, for the circuit shown in Figure 1, is less than 15mA from each supply. The design described will operate properly with good dynamic range as the battery voltage begins to fall below the nominal $9V_{DC}$. It is assumed that two 9 volt batteries would be used, but for the smaller hand held wireless microphones a single 9 volt battery would be required. Figure 2 depicts a DC-to-DC converter that will supply the $-9V_{DC}$.

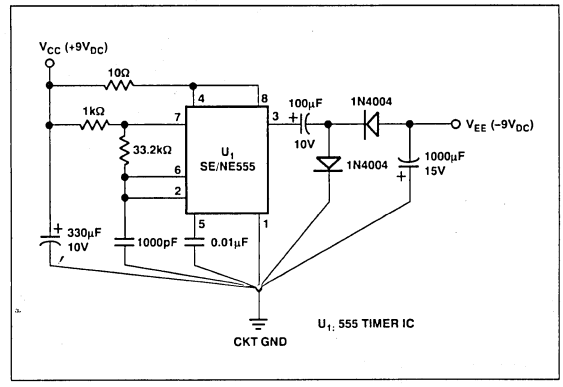


FIGURE 2: *DC-to-DC Converter for $+9V_{DC}$ to $-9V_{DC}$ at 15mA*

The converter circuit incorporates an astable oscillator running at 25kHz. It is followed by a capacitor-coupled level shifter and rectifier with a filter. A SE/NE555 timer is used in the "output sink" mode for maximum efficiency, and longest battery life.

THE RECEIVER EXPANDER SECTION

EXPANDER CONTROL

In Figure 3, the control connection of the SSM-2120 (U_3) VCA, rectifier, and control amplifier is shown. The control circuit connection to the VCA produces a 1:2 gain expansion curve. If the input rises 3dB, the output level will rise 6dB. The gain expansion ratio expression is:

$$\text{Gain}_{\text{expansion ratio}} = \frac{R_2 \cdot R_4}{R_1 \cdot R_3}$$

The rectifier input current is limited by a 10kΩ resistor connected to pin 9 of U_3, and the rectifier is biased at 10μA current through a 1.5MΩ resistor connected to V_{EE}. The SSM-2120 rectifier and VCA each have a 100dB dynamic range, resulting in accurate tracking of the compressor.

As with the compressor/limiter circuit, the small-signal averaging time for a 10μF integration capacitor is 26ms. The attack time to 3dB of final value is also about 26ms and is almost independent of signal level increases for level changes in excess of +10dB. The decay rate is 3ms per dB.

The control circuit gain values, as shown above, provide a control voltage to the VCA section $+V_C$ control port [U_3, pin 5(19)], which result in a 1:2 signal expansion characteristic. The LEVEL control sets the initial overall gain value, and is adjustable from –10dB to +20dB.

EXPANDER AUDIO

Input amplifier U_1 is a buffer between the input signal source (FM wireless receiver), the expander rectifier/control circuit, and the VCA audio signal input. If the signal source output impedance is below 100Ω, U_1 can be omitted. The nominal source signal level should be –10dBu. If signal gain or loss is required, U_1 gain structure should be modified to provide –10dBu to the VCA input current limiting resistor. The 37.4kΩ resistor ahead of the VCA input [pin 8,(16)] limits peak signal currents to avoid VCA distortion. The VCA signal input(s) are virtual ground current inputs. The 150kΩ resistor connected to V_{CC} and pin 10 of U_3 sets the VCA input/output current compliance range. A VCA input shunting capacitor shown from U_3 pin 8(16) to ground minimizes signal distortion and keeps the VCA stable by providing a high-frequency path to ground. The exact value is determined empirically. The output of the VCA feeds a virtual ground output amplifier, U_2. The overall audio path is signal noninverting, since the VCA is signal noninverting, and is combined with two inverting amplifiers U_1, and U_2.

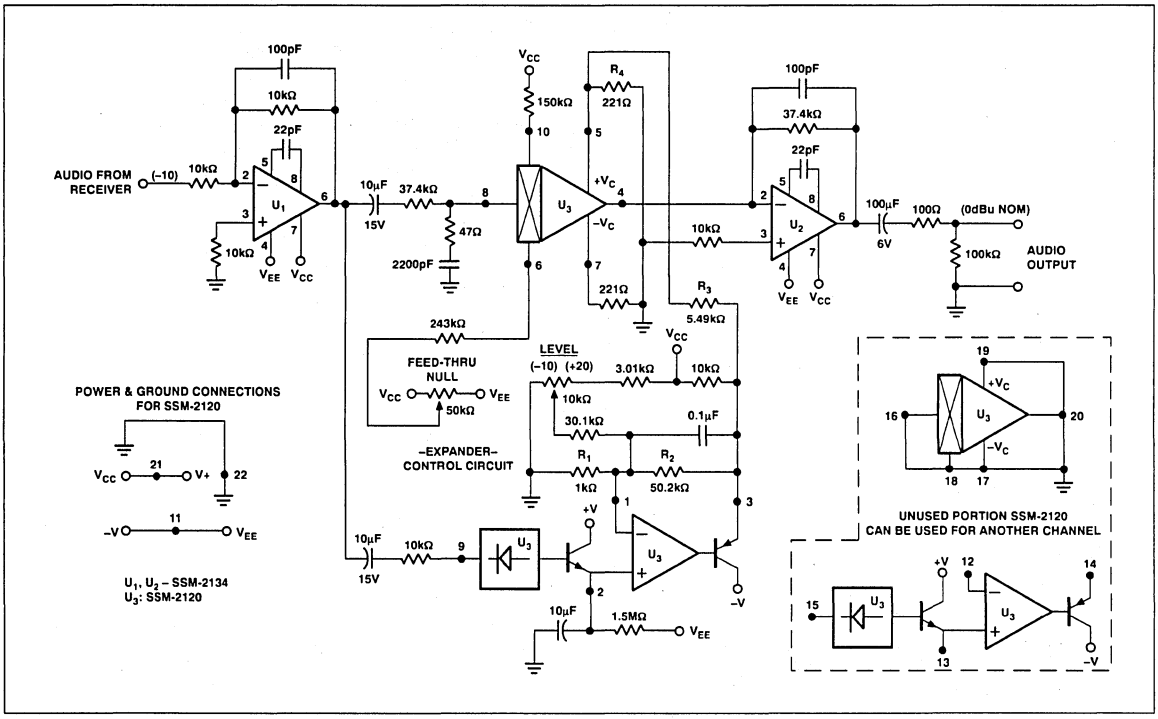


FIGURE 3: *Expander Circuit for Receiver Processor*

TABLE 1: Circuit Performance Specifications

Compressor/Limiter (Figure 1)	
Input Voltage Range (Nominal for 0dBu Out)	–65dBu to –40dBu
Compressor/Limiter Rectifier Type	Averaging
Compressor Amplifier Class	Feedback
Compressor Attack Time (to 3dB of Final Value)	26ms
Compressor Recovery Rate	3ms/dB
Feedthrough (Trimmed)	–70dBV
Compressor Gain Reduction Ratio	2:1
Limiter Attack Time (to 3dB of Final Value)	13ms
Limiter Recovery Rate	1.5ms/dB
Limiter Gain Reduction Ratio	4.6 to 1
High-Pass Filer, F_C	90Hz
High-Pass Filter Type	3rd Order Butterworth
Frequency Response (90Hz to 20kHz)	±0.5dB
S/N Ratio @ 0dB Gain	100dB
THD + Noise (% 1kHz to 20kHz)	0.05
IMD (% SMPTE 60Hz & 4kHz, 4:1)	0.05
Output Voltage Slew Rate	6V/µs
Power Supply, (Battery)	$\pm 9V_{DC}$
Output Voltage (2kΩ Load, $\pm 9V_{DC}$	+15dBu
Expander (Figure 3)	
Input Voltage Range (Nominal for 0dBu Out)	–10dBu
Expander Rectifier Type	Averaging
Expander Amplifier Class	Control Feed-Forward
Expander Attach Time (to 3dB of Final Value)	26ms
Expander Recovery Rate	3ms/dB
Feedthrough (Trimmed)	–70dBV
Gain Expander Ratio	1:2
Frequency Response (20Hz to 20kHz)	±1.0dB
S/N Ratio @ 0dB Gain (Dynamic Range)	100dB
THD + Noise (% 1kHz to 20kHz)	0.20%
IMD (% SMPTE 60Hz % 4kHz, 4:1)	0.25%
Output Voltage Slew Rate	6V/µs
Power Supply	$\pm 15V_{DC}$
Output Voltage (2kΩ Load)	+21dBu

AC coupling is not necessary but recommended. When the AC coupling is combined with feedthrough trimming, most of the unwanted sub-audible signals will be removed from the output signal. The unused portion of U_3 (SSM-2120) can be utilized in an identical second channel expander. The supply voltage should be held at ±15VDC to ±18VDC, to provide good dynamic range and circuit stability.

AN-134
AN AUTOMATIC MICROPHONE MIXER

APPLICATION NOTE 134

This application note describes an audio-signal activated microphone mixer, as shown, designed to accommodate eight input channels. The SSM-2120 Dynamic Range Processor is the nucleus of this design. The device includes two VCAs and two rectifier and control amplifier circuits. The application is designed for unattended microphone mixing functions, as would be used in a conference room that required sound reinforcement or conversation recording. The circuit provides automatic and transparent channel ON/OFF operation. The audio output automatically turns ON in less than 10ms and back OFF after 2 to 4 seconds of no audio. Each channel incorporates independent and automatic operation, with ON threshold sensitivity and level adjustment (trim) controls.

THE MICROPHONE PREAMPLIFIER CIRCUIT

For optimum circuit performance, the nominal output level from the microphone preamplifier or other audio source(s) should be –10dBu. The –10dBu level allows the SSM-2120 to provide the widest dynamic range and lowest noise, while optimizing the headroom of the automatic switch and the microphone preamplifier.

THE AUDIO SWITCH

Each audio signal is switched ON and OFF by a VCA (voltage controlled amplifier) element. By controlling the turn-ON and turn-OFF ramp time, the VCA produces transient-free switching. No distortion or "pops" are introduced using this technique. The turn-ON is ramped from a maximum of 90dB to 0dB attenuation in approximately 30ms. With the complete removal of the audio, the turn-OFF ramp of ≈100ms will begin after approximately three (3) seconds.

The VCA's input is a current input, virtual ground node. The design shown in Figure 1 assumes that $\pm 15V_{DC}$ will power the system. With this supply voltage, the 37.4kΩ input resistor(s) will keep the VCA operating at the optimum distortion and dynamic range. The 150kΩ resistor connected from V_{CC} ($+15V_{DC}$) to the reference current pin 10 of the 2120, sets the VCA bias operating point. The VCA's current output is then connected to a voltage by a transimpedance amplifier using a low noise SSM-2134 op amp. The VCA input(s) and output(s) are capacitively coupled to remove DC components from previous stages.

THE CONTROL CIRCUIT

The input signal is rectified and averaged before it is filtered by the integrator capacitor (10μF electrolytic). The small signal averaging time constant with this capacitor is approximately 60ms. The attack time is 30ms to 3dB of the final level, and is nearly independent of the magnitude of level increase. The discharge time is controlled by the 3.3MΩ resistor returned to V_{EE} ($-15V_{DC}$), which also sets the rectifier reference current.

The control circuit amplifier has a voltage gain of 217. The inverting input is used to set the ON/OFF threshold point too, and allows for the ON Threshold level adjustment. The ON Threshold range is adjustable from -40dBu to 0dBu as referenced to the input of the VCA element. The control port +Vc of the VCA is used so that a negative control voltage applied will produce an attenuation effect. R_4 (221Ω) and R_5 (4.64kΩ) attenuate the control voltage by a factor of 22, resulting in a maximum attenuation value of 90dB with no audio signal present.

To minimize the effect of ON/OFF control voltage appearing in the output signal of the VCA, the Feedthrough null control circuit is recommended. It provides an external method for balancing the internal VCA currents and component values.

THE OUTPUT SECTION

The design incorporates a virtual ground current summing bus, that is fed by the individual mixing channel level control(s) and 10.0kΩ resistor(s). The Level control(s) provides 21dB attenuation range (0dB to –21dB), and is designed to balance the different inputs, but not turn them off fully. The 100kΩ (linear taper) level control(s), for a linear rotation produces a logarithmic attenuation curve.

The virtual ground summing amplifier establishes half of the balanced output circuit, with another inverting amplifier completing the balanced output circuit. The circuit is able to drive 600Ω loads to +24dBm levels with low distortion and high reliability.

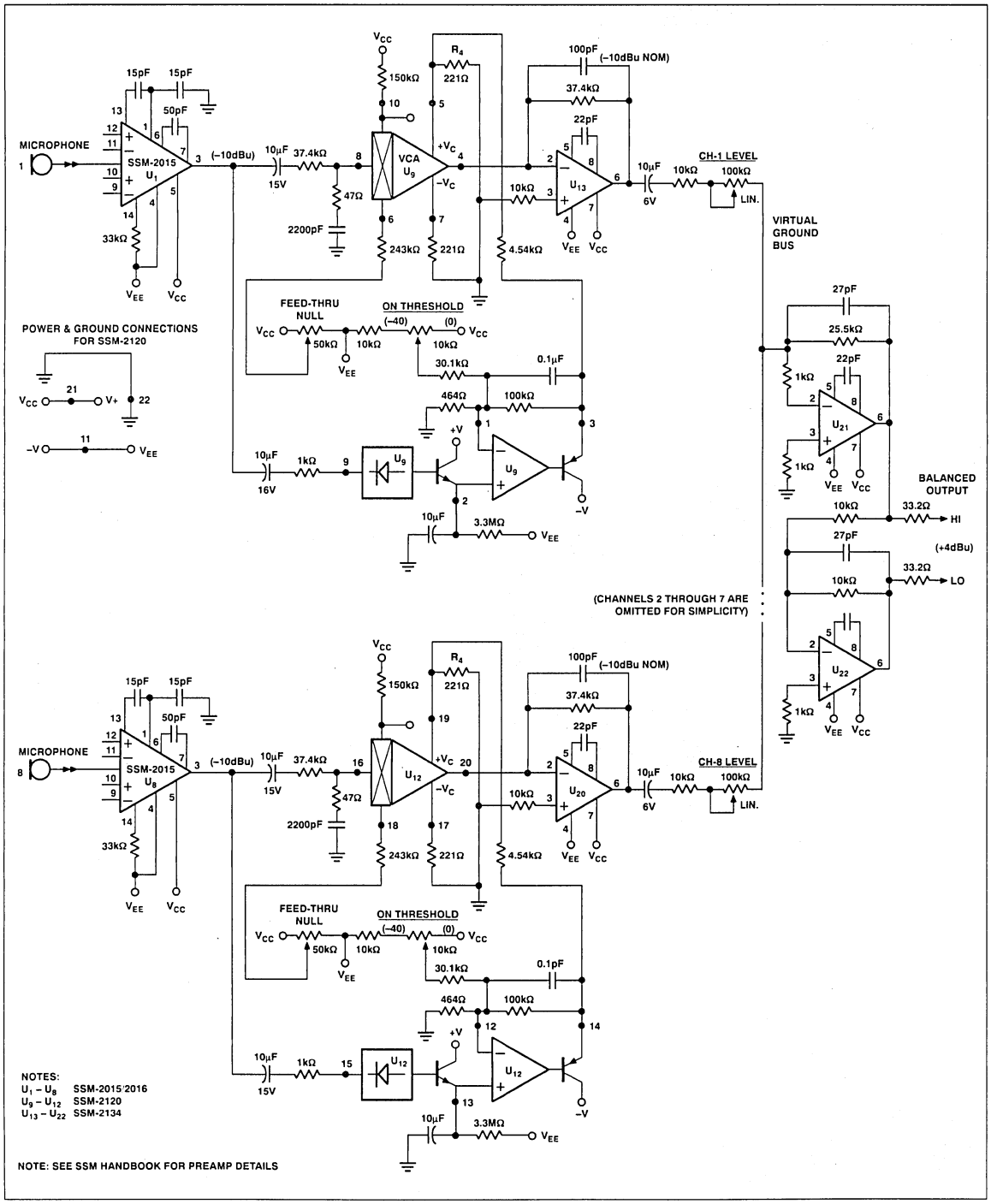


FIGURE 1: *Automatic Channel Activation Microphone Mixer Diagram Illustrates 8 Input Channels*

TABLE 1: Circuit Performance Specifications

Input Voltage, without Preamplifier, (for +4dBu Out)	–10dB
Input Impedance, Unbalanced	≈1kΩ
Headroom (Nominal for –10dBu In and Out)	32dB
Turn ON Time (to 3dB of Final Value)	30ms
Turn OFF Time (No Signal)	≈3sec
Turn OFF Ramp Time	100ms
Feedthrough (Trimmed)	>1mV
ON/OFF Threshold Range (Nominal)	0dBu to –40dBu
ON/OFF Gain Extent	0dB to –90dB
Frequency Response for ±0.1dB	20Hz to 20kHz
S/N Ratio @ 0dB Gain	110dB
THD + Noise (from 20Hz to 20kHz)	0.005%
IMD (SMPTE 60Hz and 4kHz, 4:1)	0.02%
Output Voltage Slew Rate	12V/μs
Rated Output Level (600Ω Load)	+24dBu
Output Impedance	68Ω
Output Type	Balanced
Power Supply Requirements	±15V_{DC} Regulated

AN-135
THE MORGAN COMPRESSOR/ LIMITER

APPLICATION NOTE 135

The following application was written by Michael Morgan, a consultant to PMI with extensive experience in the design of professional audio equipment, including high-performance dynamic range processors. While currently a freelance consultant, Mr. Morgan spent nine years at Valley International as a principal designer of their products.

This application note describes the configuration of a low cost, high quality compressor with variable attack time and ratio control using the SSM-2110 Level Detector and SSM-2014 VCA. The discussion begins with an overview of compressor/ limiter fundamentals, and is followed by a description of the unique attributes of the integrated circuits and their implications for the design engineer.

COMPRESSOR/LIMITER FUNDAMENTALS

The function of the audio compressor is, of course, to compress the dynamic range of the processed audio signal by altering the gain of its signal path in response to the relative level of the signal as compared to an arbitrary setpoint called the threshold, thus adding gain to low-level signals and reducing gain in the presence of high-level signals.

An audio compressor consists primarily of two functional sections, one of which derives a control signal by measuring and otherwise manipulating the audio signal to produce a voltage suitable for the second functional section, which is the gain control element. The gain control element is a device which can alter its attenuation, gain, or resistance in response to an external signal, such as a voltage or current.

The audio compressor differs from a similar device, called a limiter, in that a compressor exhibits a rotation point which is independent of its threshold setting. The rotation point is the locus on a graph of the compressor's transfer function at which the gain control element exhibits unity gain, and through which all lines derived from data describing the device's output level as a function of input level will pass. A limiter, in the purest sense, adds no gain and has no rotation point.

The compressor's ratio is defined as the increase in input level, in decibels, above the threshold which will result in an increase of output level equal to 1dB, and is a function of control circuitry gain. For example, each increase of 1dB in signal level above the threshold may cause a corresponding decrease in gain equal to 1dB, thus keeping the output level constant for a ratio of infinity:1, or it may cause a 1/2 dB decrease in gain, thus allowing the output level to rise at a ratio of 2:1. A compressor may have a very high ratio, and conversely, a limiter may have a very low ratio.

SHAPING THE RESPONSE

Figures 1a and 1b illustrate the transfer function of an ideal compressor as the ratio is varied with a fixed threshold, and as the threshold is varied with a fixed ratio, respectively. Note that in both cases, the rotation point is easily identified at 0dB. Note also that the compressor operates as a limiter when the threshold is equal to, or higher than, the rotation point. For this reason, the device described in this application note may be considered as a "compressor/limiter," but because it possesses a rotation point, we shall refer to the device as a compressor.

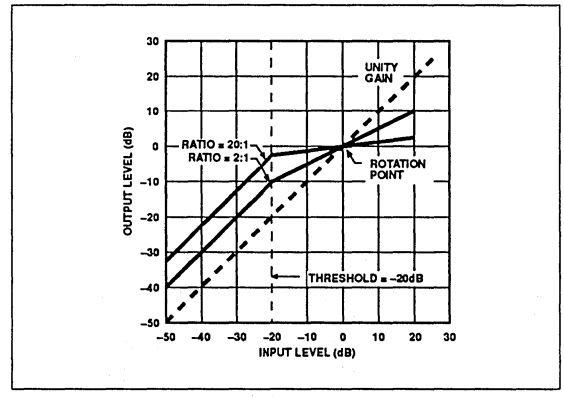


FIGURE 1a: *Output vs. Input Transfer Function of an Ideal Compressor*

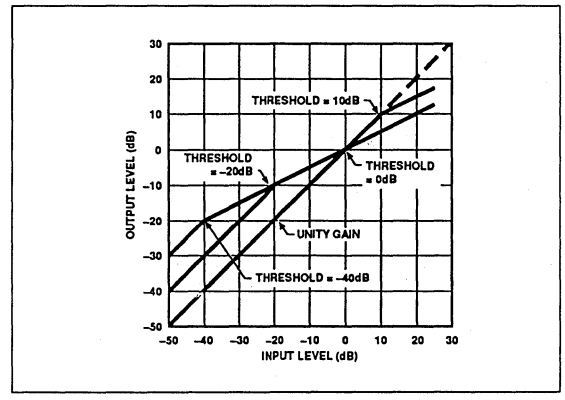


FIGURE 1b: *Output vs. Input Transfer Function of an Ideal Compressor Having a Fixed Ratio Showing the Effect of Threshold*

Audio compressors use two types of circuit topologies. In a feedback, or closed-loop configuration, the control signal is derived by measuring the output level of the gain control element. In a feedforward, or open-loop configuration, the control signal is derived by measuring the level of audio present at the input of the gain control device. Each topology has its typical advantages and disadvantages. The most common type of audio compressor uses the feedback topology. Among its advantages are: low parts cost; ease of configuration; ability to use simple, "linear" control circuitry and gain control elements. The disadvantages of the feedback topology are numerous: inability to realize continuously variable parameters accurately; heavy dependence upon circuit trimming to assure consistency in performance from unit to unit; tendency toward overshoot in either control signal or processed signal; virtual inability to configure circuitry for performing arbitrary dynamic functions, such as program control of release times, equalized sidechain functions, and interactive processing having more than one control function per gain control element.

The feedforward topology has long been considered by equipment designers to be the more versatile method of configuring audio dynamics processors. Among its advantages are: precise control of dynamics; ability to accurately and continuously vary processor parameters, such as ratio and attack-and-release time constants; easy circuit trimming for unit-to-unit consistency; possibility to realize arbitrary types of dynamics alteration; ease in configuration of interactive processing schemes using multiple control signals to operate a single gain control element; and relative freedom from control and signal overshoot. The disadvantages of feedforward topology have traditionally been: dependence upon relatively expensive and little understood logarithmic circuitry in configuration; difficulty in sourcing high-quality, low cost log/linear multipliers (dB/volt VCAs); dependence upon expensive log/RMS detection schemes to achieve the required accuracy for wide range of control.

By using integrated building blocks, feedforward control technology can be realized by equipment designers by virtue of their ease of application and low cost. These readily available integrated circuits deliver performance equal to or surpassing complicated discrete circuits, and are more cost effective for general use by equipment manufacturers.

THE SSM-2110 MONOLITHIC LEVEL DETECTOR

The SSM-2110 level detector IC represents a significant advancement in low cost, high quality converter circuitry. The device greatly simplifies the design of feedforward dynamic processors since it produces an accurate output that is proportional to the log of the absolute value of its input, and the log of the rms value of its input, in addition to the corresponding linear values. Such versatility is unique among detector/converter configurations.

VARIABLE TIME INTEGRATOR

In this application, the SSM-2110 is used in the design of a feedforward compressor. The log of the absolute value of the input signal is extracted, then integrated by a E/I x C circuit which corresponds roughly to an RC network in the linear domain (see Figure 2).

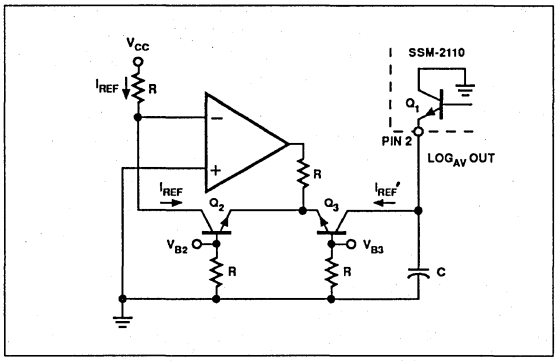


FIGURE 2: *Simplified Schematic of a Variable Time Constant Log of Average Integrator Using the SSM-2110*

The product of this operation is not, as one would expect, the average of the log of the absolute input value. During the integration process achieved by charging the integrator capacitor, C, the charging current is proportional to the antilog of the voltage appearing at the base of Q_1. Since the voltage at the base of Q_1 represents the log of the absolute value of the input, the log and anti-log terms cancel, thus leaving C to charge as a linear integrator with a current proportional to the absolute value of the input until the voltage across C approaches the voltage at the emitter of Q_1. In this manner, the order of the logging and averaging operations are reversed. This is a very important phenomenon which directly influences the audibility of the compression process, and will be discussed at length later.

The integration time of the circuit in Figure 2 is varied by changing the current through the collector of Q_3. This is accomplished by means of the multiplier circuit consisting of the operational amplifier, transistors Q_2 and Q_3, and their associated resistors.

Current I_{REF} is forced to flow through the collector of Q_2. The V_{be} of Q_2 is thus made to be proportional to the log of I_{REF} by virtue of the silicon transistor's intrinsic logarithmic property, idealized in the equation:

$V_{be} = kT/q \times \ln(I_c/I_s)$ where

k = Boltzman's constant (1.38×10^{-23}J/K)

T = Temperature in Kelvins

q = Charge on an electron (1.60×10^{-19}C)

I_c = Collector current

I_s = Reverse saturation current (extrapolated as $V_{be} \rightarrow 0$)

When transistors Q_2 and Q_3 are closely matched, V_{be} of Q_2, which appears also at Q_3's emitter, causes a current equal to I_c of Q_2 to flow through the collector of Q_3. This transistor collector current, I_{REF}, may be used to charge or discharge a capacitor, to cause a voltage drop across a resistor, or may be converted to a voltage at the output of an operational amplifier. The collector current of Q_3 may be varied by applying a voltage at the bases of Q_2 or Q_3, or both bases simultaneously. As a rule of thumb, at 25°C, each 60mV change in V_b will cause a corresponding ten-fold change in Q_3's I_c. By using the "shorthand" log relationship for gain in which a ten-fold change in voltage (or current) equals 20dB, we can say that the collector current of Q_3 can be made to vary antilogarithmically at a rate of 1 dB/3mV (20dB/60mV). In effect, the circuit generates a voltage at the emitter of Q_2 which corresponds to the log of the input current, I_{REF}, adds the control voltage, then generates a current at the collector of Q_3 which is proportional to the antilog of the sum. Thus the portion of the circuit formed by the operational amplifier, Q_2, Q_3, and their associated passive components form a two-quadrant multiplier whose output is a high compliance current sink.

A positive voltage applied to the base of Q_2 will cause a corresponding decrease in Q_3's collector current, while a positive voltage applied to the base of Q_3 has the opposite effect, causing an increase in I_c of Q_3. Both bases may be controlled by bipolar voltages, but I_{REF} must flow in the direction indicated by conventional current flow through the transistors (must be sourced from a voltage more positive than the noninverting input of the operational amplifier for NPN transistors).

In operation, varying the current which discharges C also causes a varying offset voltage at the collector of Q_3 which equals the change in V_b, and must be compensated for in order to derive a useful control voltage. Figure 3 shows the response to a +10 volt pulse input having a repetition frequency of approximately 4 pps and a duty cycle of 50%. Note that the X-axis corresponds also to increasing integration time (decreasing I_c of Q_3). The illustration is a composite of several sampled waveforms, thus, scalar references in the X-axis are valid only for each pulse.

As can be seen in Figure 3, in the log average detection mode, the response of the device to large level changes is relatively fast, while the last 50 to 100mV of change occurs at the characteristic integration time determined by the status of the charge on the capacitor, C, as it is discharged by the collector current of Q_3. As the voltage across C approaches the voltage at the emitter of Q_1, the transistor behaves less as an antilog element, and more as a linear resistance proportional to V_{be}/I_{REF}.

These attributes determine the detector circuit's response to complex waveforms, and directly affect the audibility of the compression process. Consider the following explanation: Humans respond to changes in audio signal level by perceiving volume as being proportional to the log of the acoustic power emitted by a source, thus the human listener perceives a source emitting 10 watts of "sound," (if the reader will permit such simplifications) to be roughly twice as loud as the same source emitting only 1 watt. This implies that one should be able to control audio levels logarithmically for a natural "sound" in the processed output. That is generally the case, but the principle does not extend, in a strict sense, to the control of a compressor.

If one accepts the premise that the most common uses of the audio compressor are to enhance the "loudness" of the processed material, or to "level" the apparent volume of the processed material, one should be aware of the effect of waveform complexity upon perceived loudness. A simple example is found in the case of a musician playing an instrument: when called upon to perform a solo, in order to "stand out" from the background music, the instrumentalist produces more complex sounds, in addition to producing sounds at a higher relative level. The increase in complexity provides a psychoacoustic "cue" which translates to the human listener as increased perceived loudness.

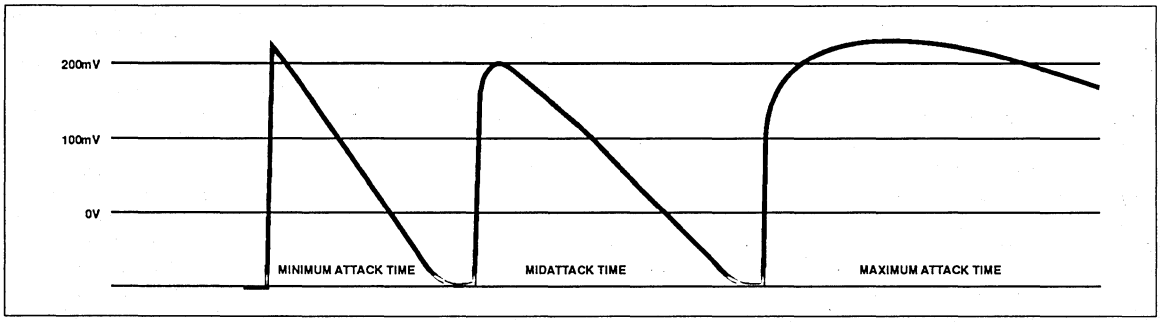


FIGURE 3: *Output Voltage Response of the Variable Time Constant Log of Average Integrator to a LF Square Wave Input*

During the compression process, if the detector circuitry produces a signal which calls for more gain reduction in response to the added harmonics in a sound which cause an increase in complexity, the gain control element will comply, thus making a solo instrumental exit the compressor at a lower level, foiling the intent of the performer. This is precisely what happens when using RMS detection – the detector circuit (correctly) assesses the increased complexity as an increase in sound energy, and calls for gain reduction.

The log averaging detector is relatively insensitive to increases in waveform complexity, and "ignores" the loudness cue thus provided. As a result, a complex waveform exits the compressor at a slightly higher level than it would if under the control of an rms detector. This rather unique "quirk" found in the log averaging process allows a solo instrumental or vocal to stand out in the processed signal, thus preserving the intent of the performer.

As a log averaging detector, the SSM-2110 exhibits remarkably little departure from an idealized log curve representing its input level throughout the entire range of the adjustable integration time, and offers superior performance to the equipment designer in this type of application. In addition, at higher input levels, the device does not compress the waveform at its output, thus under-reading the input value. In fact, the detector exhibits a gentle and quite predictable deviation from log conformity at high input current levels which results in the addition of a linear error term. This causes a slight over-reading of the input, and is quite useful for aficionados of "soft knee" limiting. It is unlikely that any real compressor design would require so wide a range of operation that this deviation might pose a problem (> 60 dB), but since the error term is so predictable and consistent, it can easily be corrected elsewhere in the control circuitry if necessary.

THE COMPRESSOR CONTROL CIRCUIT

Figure 4 illustrates a compressor control circuit incorporating the SSM-2110 as the detector element. Because the temperature compensation characteristics of the log recovery amplifier are not required in this application (control of a VCA having a complementary control sensitivity temperature coefficient) and to eliminate trimming of scale factor on a unit by unit basis, the log recovery amplifier is disabled by connecting its inputs to the IC's V_{REF} output. This step is necessary for proper operation of the IC when the log recovery amplifier is not used. The log recovery transistor is not used since offset is not a real concern in this circuit configuration.

The amplifier in the audio signal path, A_1, should be of a high quality, low noise type such as the SSM-2134. The remaining amplifiers may be general purpose types, preferably having FET input stages to minimize the effects of input bias currents on the accuracy of the multiplier circuits.

Amplifier A_2, and the SSM-2210 matched transistor pair Q_{1a}/Q_{1b} form the voltage-controlled current sink for the variable log averaging integrator. Amplifier A_4 boosts the output of the integrator to a usable level by increasing the nominal 6mV/dB scale factor of the signal at pin 2 to 1V/20dB, or 1V per decade. An offset corresponding to the change in voltage at pin 2 which results from varying the integration time is applied via R_{12}. Variable resistor VR_2 allows the adjustment of the compressor's rotation point, or that input level at which the output of A_4 will be 0V.

A pair of matching two-quadrant multipliers, which are configured using amplifiers A_6 and A_8 along with a four-transistor array Q_2 (MAT-04), allow adjustment of the compressor's ratio and adds sufficient gain as a function of both the threshold setting from VR_4 and A_9, and the ratio, as determined by VR_3 and A_5, to maintain the compressor's rotation point. Amplifier A_7 converts the current output of the ratio multiplier from Q_{2b} into a voltage which charges the holding capacitor C_8 via Q_{3a} to a voltage corresponding to the amount of gain reduction required of the VCA. Amplifier A_{12} converts the current output of the maintenance gain multiplier from Q_{2c} into a voltage corresponding to the quiescent gain required for the VCA to maintain the compressor rotation point, and adds or reduces gain at the VCA in response to the output gain control VR_7.

The release current sink is formed by amplifier A_{10}, and two sections of monolithic transistor array Q_3. Compensation for V_{be} of Q_{3a}, and for the quiescent change of voltage across C_8 caused by varying the release current through Q_{3c} are applied via R_{31} to A_7.

Amplifier A_9 and diode D_3 form a precision half-wave rectifier whose output is a positive voltage equal to the gain reduction signal. This point may also source a gain reduction indicator with intrinsic scaling of +1V = –20dB. Since metering is a matter of preference for the design engineer, no attempt has been made to include a gain reduction indicator as part of this circuit discussion.

Since it is possible for the inputs of both A_6 and A_8 to be negative voltages, it is wise to include germanium diodes D_1 and D_2 to prevent forward conduction of the internal base to emitter protective diodes in the MAT-04, thus eliminating the possibility of reverse leakage coupling between the multipliers. The existence of these diodes also prevents application of the MAT-04 as the charging transdiode Q_{3a}, since a voltage more negative than that across C_8 will frequently be present at the emitter of Q_{3a}.

Amplifier A_{13} outputs the algebraic sum of the various gain control signals for application to the compressor VCA section which will be described next.

Selection of the internal scale factor at 1V/decade, and inclusion of the –7.5V "math rail" are arbitrary choices made by the author in order to accommodate the use of the variable integrator, and to skew the control markings on the front panel controls, indicated by the enclosed names associated with those variable resistor potentiometers. Placing the rotation point, as determined by R_2, at the nominal operating line level, e.g., +4dB, etc., minimizes the effects of errors caused by the uncompensated temperature coefficient of the ratio multiplier, and any minor deviations in log conformity inherent in the detector circuitry or VCA sections of the compressor.

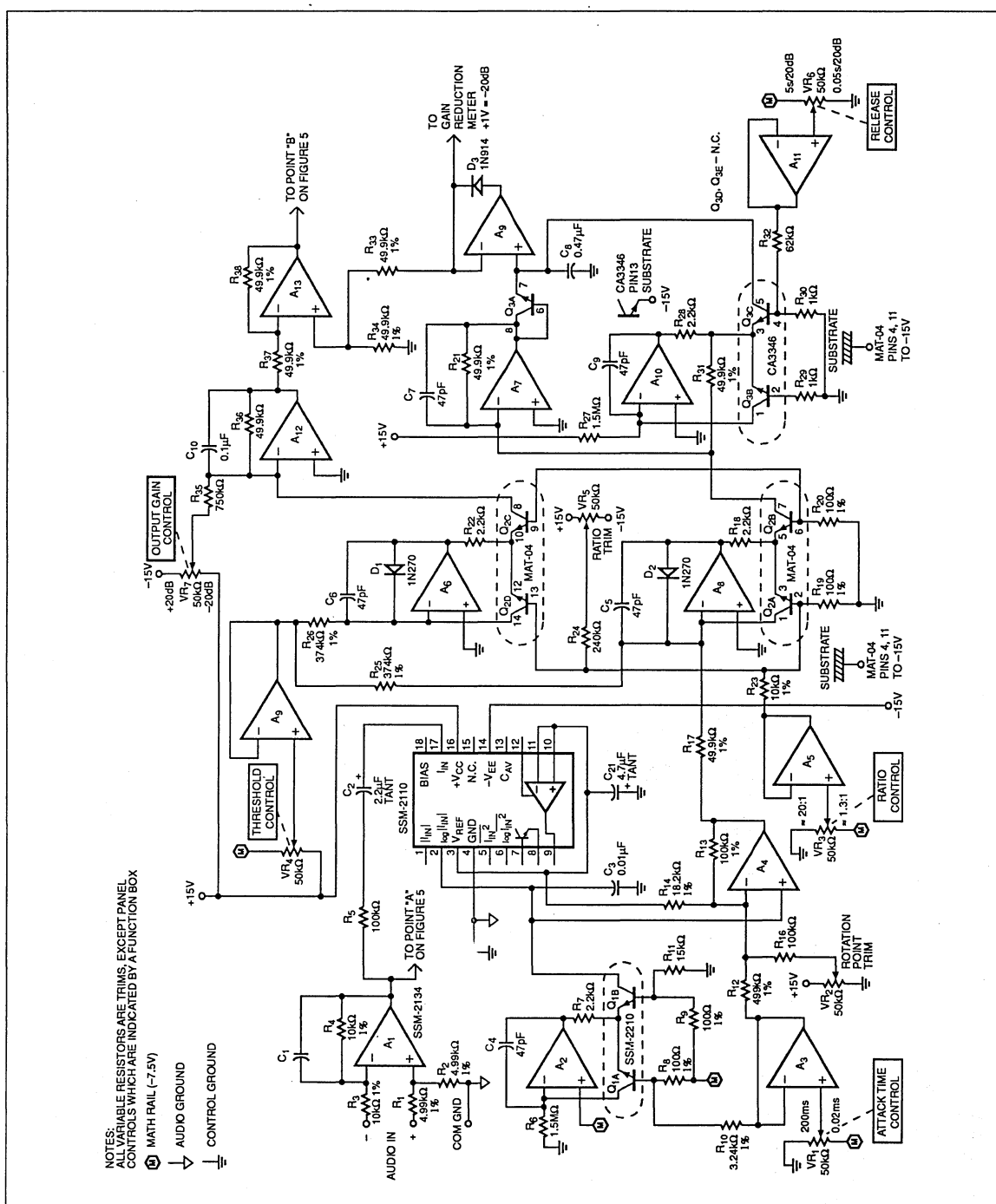


FIGURE 4: *Compressor Control Circuitry Schematic*

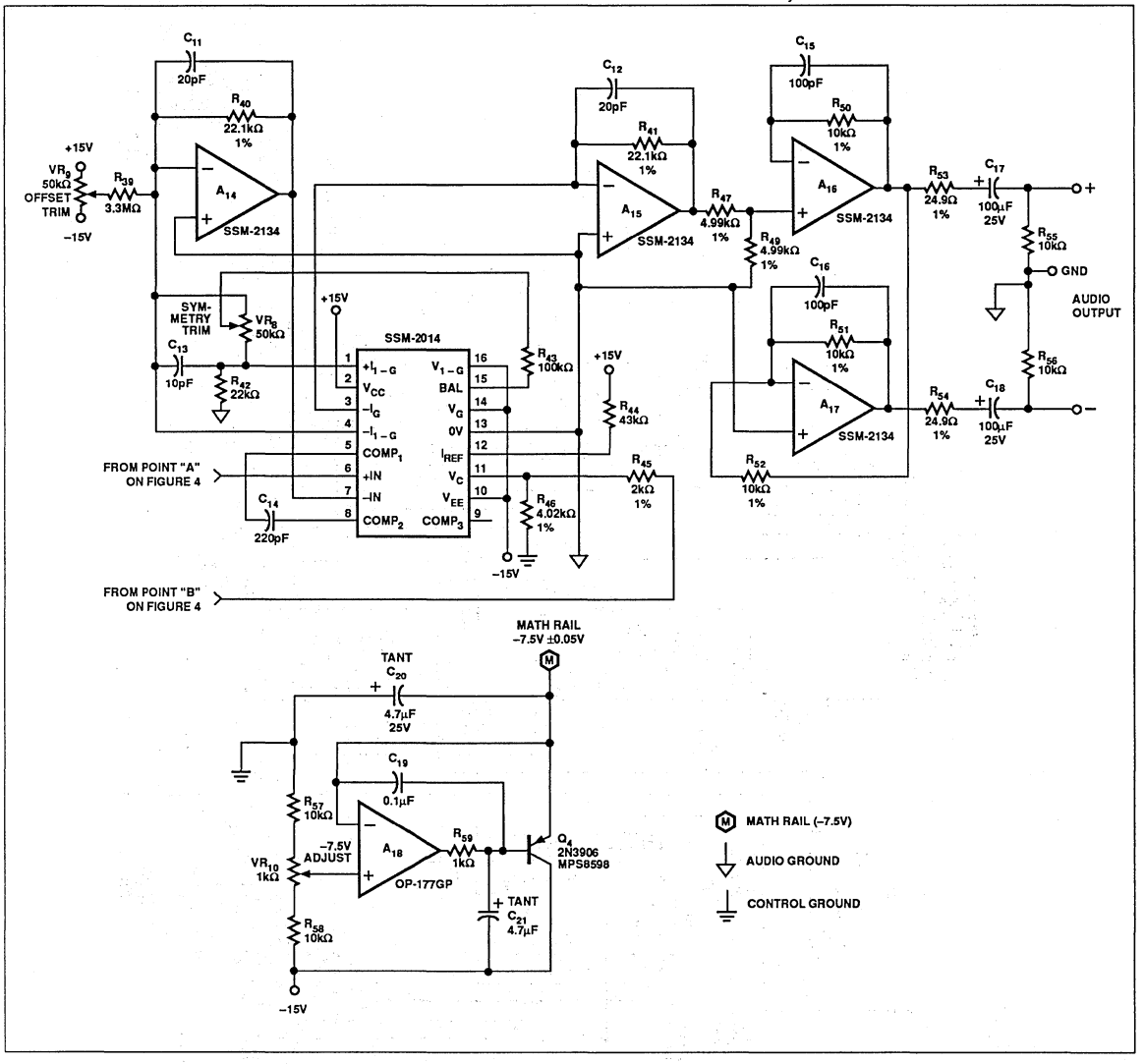


FIGURE 5: *VCA, Math Rail Regulator and Line Driver Schematic*

THE VCA SECTION

Figure 5 shows the VCA section of the compressor using the SSM-2014. The device is configured as an "outboard OVCE" in accordance with the literature supplied with the IC. Amplifiers A_{14}, A_{15}, A_{16}, and A_{17} should be high quality, low noise op amps such as the SSM-2134. A_{14} and A_{15} provide the necessary feedback and output buffers for this particular circuit. Resistive voltage divider R_{45}/R_{46} reduces the OVCE control port sensitivity to +1V/20dB attenuation to match the scale factor of the control circuitry. Variable resistor R_8 is adjusted for lowest distortion products, preferrably at unity gain with a high level input. R_9 is adjusted by applying a low frequency (<50Hz) signal at about $2V_{P-P}$ to pin 11, and setting for least low frequency output at A_{15} under a no-input signal or shorted-input condition. The stability of both these trims will be a welcomed surprise to the designer used to dealing with log/antilog VCAs.

A "quasi-balanced" line driver, consisting of A_{16}, A_{17}, and their associated passive components, completes the compressor

circuitry. The unit is capable of driving a 600Ω load at a sustained output level of +21dBm, and has a maximum output of +26dBm.

The SSM-2014 provides the designer a degree of flexibility in configuration which is not easily available using other VCA topologies. Chief among its attributes is the ability to select the operating bias current by applying current to a single port on the chip. This allows the user to select an operating point which is optimized for best noise performance vs. distortion for a given application.

In considering the normal operation of the compressor, the most common scenario is that the unit is used to "track" instruments or vocals. Of secondary, but no less important, concern is use for compressing mixed program material to enhance apparent loudness. In both applications, the trade-off between the residual noise floor and distortion at high-signal levels, both a function of operating bias, is somewhat arbitrary. Since it is likely that the dynamic distortion inherent in the compression process in normal operation would be at least equally as noticeable as moderate distortion at high-signal levels, the "intermediate" bias setting as described in the literature accompanying the device was chosen. This places the device bias at approximately 300μA, with a value of 43kΩ for R_{44}. As a result, the noise floor for the VCA circuit is –84dB (ref. $0.775V_{RMS}$) in a 20 kHz bandwidth at 0dB gain. The 1kHz THD+Noise measurements yielded figures consistent with the published data, and SMPTE IMD measurements disclosed worst-case distortion products in the 0.2% range, which is acceptable in all but the most critical applications. Should the designer wish to implement the sliding bias scheme, as described SSM-2014 data sheet, the output of the absolute value at pin 1 of the SSM-2110 (see Figure 4), or the rms computing loop (pin 5) may be used to drive a comparator with the appropriate time constants in order to switch to class A operation in the presence of high level inputs. In practice, this makes little difference in the transparency of the compressor in normal operation. Listening tests of the compressor demonstrated the smooth, precise control expected of the feedforward circuit topology. As the attack time (integration time) control is advanced from fast to slow settings, the low frequency content in mixed material becomes more solid and better defined, but the tendency to "squash" the lows is relatively absent at faster attack times as compared to other compressors having adjustable attack times with comparable settings.

The log averaging detector scheme really shines on vocals and horns, bringing a soloist "up-front" with moderate attack times. This is a noticeable difference when compared to any RMS-type compressor used for comparison in the listening tests.

ADJUSTING FOR BEST PERFORMANCE

As in any compressor or limiter whose ratio must be trimmed in its initial setup (see Figure 4, VR_5), the unit is sensitive to incorrect adjustment. One of the most distressing sounds which can be produced by a compressor is "over-compression," in which the control circuitry causes too much gain reduction at high ratios. For this reason, the compressor ratio trim should be set with the **Threshold** control at 0dB (0V at the wiper of VR_4), and with an input of +20dB, the trim should be adjusted so that with the **Attack**, **Release**, and **Output** gain controls centered, the maximum **Ratio** setting, fully clockwise, produces an output level equal to or slightly greater than the rotation point.

When laying out circuitry using the SSM-2014 and SSM-2110, care should be taken to keep traces to virtual grounds as short as possible, and a single point audio ground should be used. The control ground should connect to the audio ground at one point, pin 4 of the SSM-2110, and supply traces should be heavily decoupled with high quality capacitors. Traces carrying audio signal should be kept well away from control circuitry, and the detector IC and VCA should be located away from heat sources such as regulators or power supply transformers.

Since all parameter control is derived from DC levels produced by the front panel controls, high quality potentiometers need not be used. All the front panel control scales may be marked in equal intervals, and follow the antilog law, i.e., equal spacing per dB of gain or threshold setting, equal spacing per decade of attack and release times, etc. The sole exception is the ratio control, whose scale is skewed so that 2:1 appears near the middle of the control, as one normally would expect of a traditional feedback compressor.

The compressor control circuit described in this application note was configured using only four quad op amps in addition to the SSM-2110 and three matched transistor arrays. By providing the basic building blocks for an audio dynamic range processor in monolithic form, the SSM audio chip set greatly simplifies the implementation of an otherwise complex processor.

MEASURED PERFORMANCE:

SMPTE IMD @ Unity Gain, 0dBv in	0.009%
SMPTE IMD @ Unity Gain, +20dBv in	0.11%
SMPTE IMD @ 20dB Gain Reduction, 0dBv in	0.06%
SMPTE IMD @ 20dB Gain Reduction, +20dBv in	0.025%
Residual Noise and Hum @ Unity Gain, 20kHz BW	–84dBv
Maximum Output Level into 600Ω, Balanced	+21dBm
Maximum Input Level Before Clipping	+21dBv
Usable Dynamic Range, Unweighted in 20kHz BW	103dB
Threshold Range Ref. Rotation Point	–40 to +20dB
Useful Range of Rotation on Point Adj.	–10 to +4dBv
Nominal Attack (Integration) Time Range	0.02 to 200ms
Nominal Range of Ratio Adjustment	1.3:1 to 20:1
Range of Release Time Adjustment	0.05 to 5s/20dB
Range of Output Gain Adjustment	–20 to +20dB

NOTE: 0dBv refers to 0.775 V_{RMS}

PACKAGING AND ORDERING INFORMATION

PACKAGING

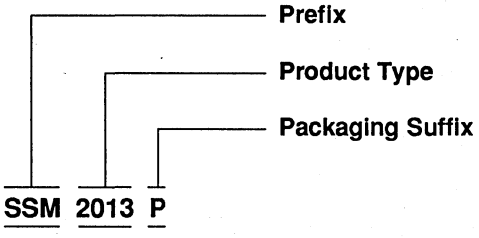
All PMI SSM Audio Products are offered in plastic DIP packages (P-suffix), and many new products are also available in a small outline surface mount package (S-suffix). Please refer to the individual data sheet for specific package options.

The 1990 PMI data book contains dimensions of the available packages.

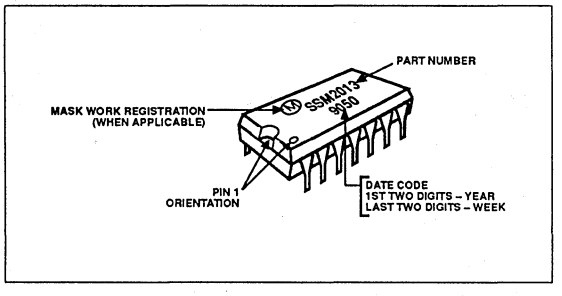
ORDERING

SSM Audio Products are available from over 400 PMI stocking distributor locations worldwide. Contact your local PMI Sales Office or representative for ordering information.

SSM PART NUMBERING SYSTEM



SSM DEVICE MARKING

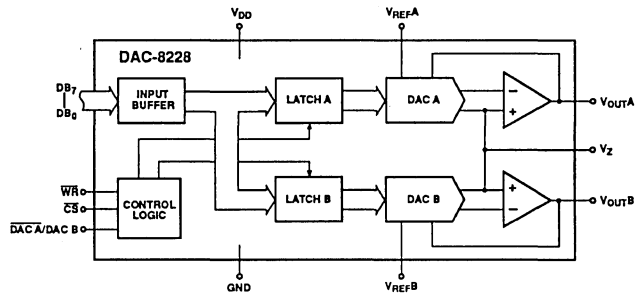


OTHER PMI PRODUCTS FOR AUDIO APPLICATIONS

Precision Monolithics Inc.

DIGITAL-TO-ANALOG CONVERTERS

Functional Diagram



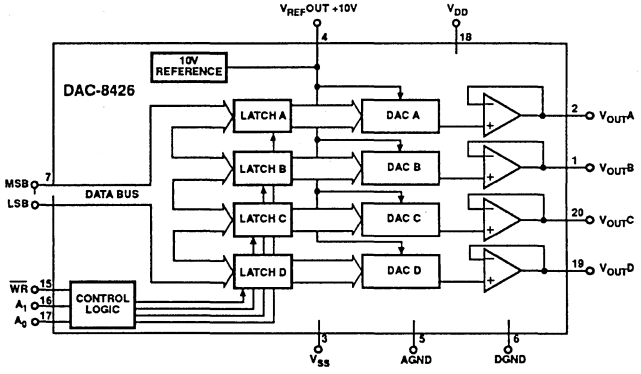
DAC-8228

Dual 8-Bit CMOS
D/A Converter with Voltage Output

Features

- Two 8-Bit DACs in a Single Chip
- Adjustment-Free Internal CMOS Amplifiers
- Fits AD/PM-7528 and AD/PM-7628 Sockets
- Single or Dual Supply Operation
- TTL Compatible Over Full V_{DD} Range
- 5µs Settling Time
- Fast Interface Timing . . . t_{WI} = 50ns
- Improved Resistance to ESD
- Available in Small Outline Package
- –40°C to +85°C for the Extended Industrial Temperature Range

Functional Diagram



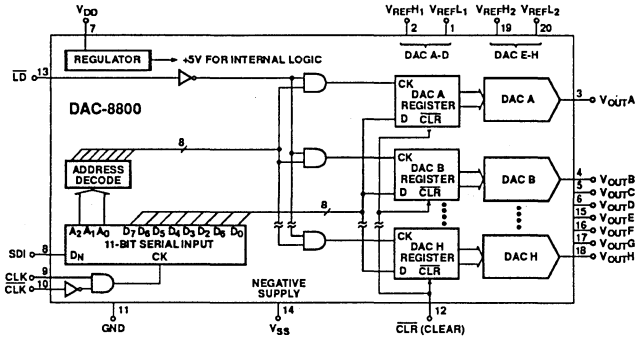
DAC-8426

Quad 8-Bit DAC
with 10 Volt Reference

Features

- Fits AD7226 Sockets
- ±1/2 LSB Maximum INL and DNL
- Space Saving 20-Pin 0.3" Wide DIP Package

Functional Diagram



DAC-8800

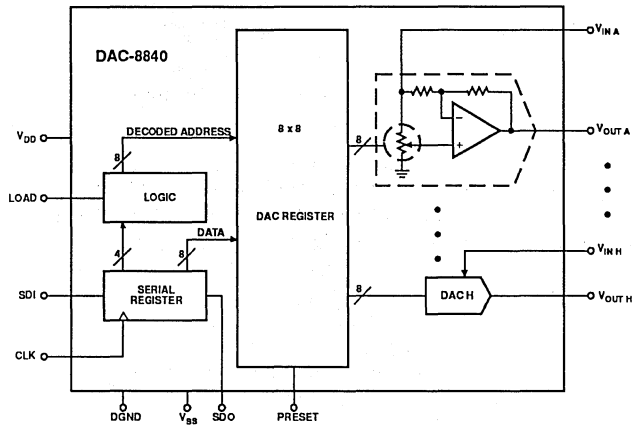
Octal 8-Bit CMOS TrimDAC™

Features

- Excellent for General Purpose Voltage Adjustment/Level Setting Applications
- ±1/2 LSB Relative Accuracy
- TTL Compatible, Serial Input
- 4µs Settling Time

DIGITAL-TO-ANALOG CONVERTERS

Functional Diagram



Advance Information

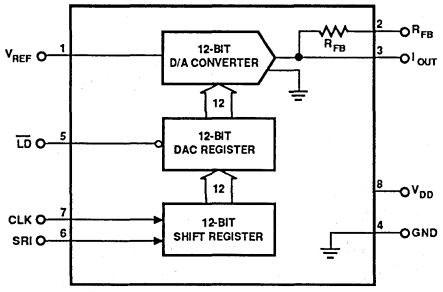
DAC-8840

8-BIT Octal
4-Quadrant, CMOS
Multiplying TrimDAC™

Features

- Replaces 8 Potentiometers
- 0.5% Total Harmonic Distortion
- 1MHz 4-Quadrant Multiplying Bandwidth
- No Signal Inversion
- Eight Individual Gain-Controlled Channels
- 3-Wire Serial Input
- Low Cost
- ±3 Volt Minimum Output Swing
- Mid-Scale Preset, V_{OUT} = 0V
- 24-Pin 0.3" DIP and SOL-24 Packages

Functional Diagram



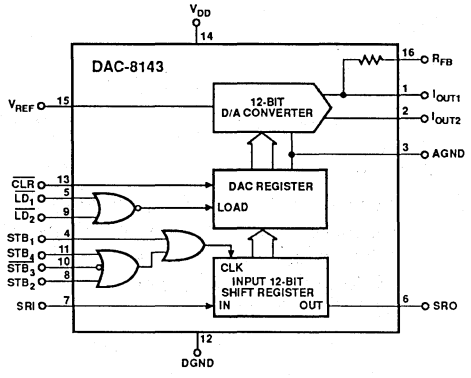
DAC-8043

12-Bit Serial Input
Multiplying CMOS D/A Converter
in an 8-Pin Mini-DIP

Features

- 12-Bit Accuracy in an 8-Pin Mini-DIP
- Fast Serial Data Input
- Low ±1/2 LSB Max INL and DNL
- Max Gain Error: ±1 LSB
- Low 5ppm/°C Max Tempco
- ESD Resistant
- Low Cost
- –40°C to +85°C for the Extended Industrial Temperature Range

Functional Diagram



DAC-8143

12-Bit Serial Daisy-Chain
CMOS D/A Converter

Features

- Fast, Flexible, Microprocessor Interfacing in Serially-Controlled Systems
- Buffered Digital Output-Pin for Daisy-Chaining Multiple DACs
- Minimizes Address-Decoding in Multiple DAC Systems – Three Wire Interface for Any Number of DACs
  - One Data Line
  - One CLK Line
  - One Load Line

DIGITAL-TO-ANALOG CONVERTER SELECTION GUIDE

DIGITAL-TO-ANALOG CONVERTER SELECTION GUIDE

PMI offers a complete line of digital-to-analog converters (DACs), all of which are guaranteed to be monotonic over their operating temperature ranges, and some which have become industry standards. The D/A converters have been arranged in the selector guide by resolution. 6-bit through 16-bit devices are sorted by number of D/A converters per package.

D/A CONVERTERS

Product	Resolution (Bits)	Settling Time	DACs/ Package	DAC Output	Power Dissipation (mW)	Digital Interface
*DAC-01	6	3µs	1	V	250	6-Bit
PM-7224	8	5µs	1	V	60	Latched 8-Bit
PM-7524	8	200ns	1	I	5	Latched 2-Digit BCD
DAC-08	8	135ns	1	I	136	8-Bit
DAC-108	8	20ns	1	I	136	8-Bit
DAC-888	8	400ns	1	I	190	Latched 8-Bit
*DAC-1408A	8	250ns	1	I	265	8-Bit
*DAC-1508A	8	250ns	1	I	265	8-Bit
DAC-20	8	150ns	1	I	194	2-Digit BCD
DAC-8228	8	5µs	2	V	165	Latched 8-Bit
DAC-8229	8	5µs	2	V	165	Latched 8-Bit
PM-7528	8	350ns	2	I	5	Latched 8-Bit
PM-7628	8	200ns	2	I	5	Latched 8-Bit
DAC-8408	8	250ns	4	I	5	8-Bit w/ Readback
PM-7226	8	5µs	4	V	250	Latched 8-Bit
DAC-8426	8	5µs	4	V	250	Latched 8-Bit
PM-7228	8	5µs	8	V	430	Latched 8-Bit
DAC-8800	8	2µs	8	V	25	Latched Serial
DAC-8840	8	4µs	8	V	150	Latched Serial

*Not recommended for new designs.

DIGITAL-TO-ANALOG CONVERTER SELECTION GUIDE

D/A CONVERTERS

Product	Resolution (Bits)	Settling Time	DACs/ Package	DAC Output	Power Dissipation (mW)	Digital Interface
PM-7533	10	600ns	1	I	30	10-Bit
*DAC-02	10 + Sign	2µs	1	V	350	10-Bit
*DAC-03	10 + Sign	2µs	1	V	350	10-Bit
*DAC-05	10 + Sign	2µs	1	V	350	10-Bit
DAC-06	10 + Sign	1.5µs	1	V	300	10-Bit
DAC-10	10	150ns	1	I	285	10-Bit
DAC-86	10	500ns	1	I	207	Chord + Step
DAC-88	10	500ns	1	I	262	Chord + Step, µ Law
DAC-89	10	500ns	1	I	263	Chord + Step, A Law
DAC-100	10	300ns	1	I	250	10-Bit
DAC-210	10 + Sign	1.5µs	1	V	315	10-Bit + Sign
DAC-401	10	2ns, 400MHz	1	V	450	Latched 10-Bit
DAC-8012	12	1µs	1	I	10	12-Bit w/ Readback
DAC-8043	12	1µs	1	I	10	Latched Serial Daisy
DAC-8143	12	1µs	1	I	10	Latched Serial Daisy
PM-7541	12	1µs	1	I	10	12-Bit
PM-7541A	12	1µs	1	I	10	12-Bit
PM-7542	12	1µs	1	I	10	Latched 4-Bit
PM-7543	12	1µs	1	I	10	Latched Serial
PM-7545	12	1µs	1	I	10	Latched 12-Bit
PM-7548	12	1µs	1	I	10	Latched 8-Bit
PM-7645	12	1µs	1	I	10	Latched 12-Bit
DAC-312	12	500ns	1	I	305	12-Bit
PM-562	12	1.5µs	1	I	465	12-Bit
DAC-8212	12	1µs	2	I	10	Latched 12-Bit
DAC-8221	12	1µs	2	I	10	Latched 12-Bit
DAC-8222	12	1µs	2	I	10	12-Bit Double-Buffered
DAC-8248	12	1µs	2	I	10	8-Bit Double-Buffered
DAC-8412	12	20µs	4	V	180	12-Bit w/ Readback
DAC-16†	16	650ns	1	V	200	16-Bit

* Not recommended for new designs.
† Advance information - check factory for availability.

OPERATIONAL AMPLIFIERS

Precision, Low Noise
OP-27, OP-270, OP-470

	OP-27 Single	OP-270 Dual	OP-470 Quad	
Extremely Low Noise (@ 1kHz)	3.8nV/√Hz	5nV/√Hz	5nV/√Hz	Max
Very Low Offset Voltage	25μV	75μV	400μV	Max
Slew Rate	2.8V/μs	2.4V/μs	2V/μs	Typ
Gain-Bandwidth	8MHz	5MHz	6MHz	Typ

The OP-27, OP-270 (dual), and OP-470 (quad) feature low noise with excellent DC performance. Each device is unity-gain stable. Supply current for the OP-270 and OP-470 is unusually low for low noise amplifiers, running at 2.25mA typically per amplifier. The excellent AC matching between amplifiers makes them ideal for matched gain stages, audio amplifiers, and active filters. The low offset, high CMR and PSR are especially useful in low noise instrumentation amplifiers.

Precision, Low Noise, Fast
OP-37, OP-271, OP-471

	OP-37 Single	OP-271 Dual	OP-471 Quad	
High Gain-Bandwidth	63MHz (A_{VCL}≥5)	5MHz	6MHz	Typ
Excellent Slew Rate	17V/μs	7V/μs	8V/μs	Typ
Low Noise (@ 1kHz)	3nV/√Hz	8nV/√Hz	7nV/√Hz	Typ
Low Offset Voltage	25μV	200μV	800μV	Max

The OP-37 has very good gain-bandwidth performance and is stable for gains of five and above. The OP-271 (dual) and OP-471 (quad) are unity-gain stable.

Wide Bandwidth, Low Noise, Precision
OP-61

High GBW (A_{VCL} ≥ 10)	200MHz	Typ
Low Voltage Noise	3.4nV/√Hz @ 1kHz	Typ
Low Offset Voltage	500μV	Max
High Slew Rate	45V/μs	Typ
Fast Settling	300ns to 0.01%	Typ
High Gain	475V/mV	Typ

The OP-61 offers an outstanding combination of high speed and low noise with DC precision to meet the demands of today's high performance equipment. A very high gain-bandwidth product of 200MHz (A_{VCL} ≥ 10) and a fast 45V/μs slew rate are achieved with only 7.5mA supply current.

The OP-61 is available in 8-pin plastic DIP and 8-pin small outline (SO) packages, with guaranteed operation over the –40°C to +85°C temperature range.

Also available in MIL temp and LCC packages.

OPERATIONAL AMPLIFIERS

Dual High-Speed JFET Input
OP-249

Fast Slew Rate	22V/μs	Typ
Fast Settling	900ns to 0.01%	Typ
Low Offset Voltage	300μV	Max
High Open-Loop Gain	1,000V/mV	Min
Low THD	0.002%	Typ

This high-precision dual features high slew rate, excellent DC performance and very low cost. Specifications include a maximum long term limit for input offset voltage, a first for JFET input amplifiers.

The OP-249 is available in an 8-pin plastic DIP with guaranteed operation over the –40°C to +85°C temperature range. Also available in military versions.

Matched Monolithic Quad NPN Transistor
MAT-04

Low Noise Voltage @ 100Hz, 1mA	2.5nV/$\sqrt{Hz}$	Max
High-Current Gain	400	Min
Gain-Bandwidth Product	300MHz	Typ
Excellent Log Conformance	r_{BE} = 0.6Ω	Max
Very Low Offset Voltage	200μV	Max
Matching Guaranteed for All Transistors		

The MAT-04 is a quad monolithic NPN transistor that offers excellent parametric matching for non-linear circuit applications. Performance characteristics of the MAT-04 include high gain of 400 (Min) over a wide range of collector current; low noise (2.5nV/$\sqrt{Hz}$ Max at 100Hz, I_{CZ} = 1mA); and excellent logarithmic conformance. The MAT-04 also features a low offset voltage of 200μV and tight current gain matching to within 2%.

The MAT-04 is an ideal choice in applications where low noise and high gain are required.

Other Products from PMI:

- High-Speed Operational Amplifiers
- Low Power/Micropower Operational Amplifiers
- High Accuracy Instrumentation Amplifiers
- High-Speed Buffers
- Data Conversion Products
- Voltage Comparators
- Precision Voltage References
- Analog Switches and Multiplexers
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HIGHLIGHTS FROM PMI'S 1990 DATA BOOK

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