5-Class Processor PCI System Controller with Power Management

FEATURES

- **Optimized three-chip PCI system controller for Intel Pentium® processor-based portable computers**
- **Supports all Pentium® and 5-class 3.3-V processors**
  - — Supports processor bus speeds of 50-, 60-, and 66-MHz
  - — Universal support for AMD® K5 and Cyrix® 6x86™ processors
  - — Supports both toggle and linear burst sequences
- **Supports SmartDock™ technology**
  - — Supports PCI hot-docking and secondary ISA bus in the docking station
  - — Enables desktop capabilities in a portable system
- **Supports distributed DMA to provide a direct memory access on the PCI Bus**
- **Supports level-1 write-back or write-through cache protocols**
- **Integrated 64-bit write-through level-2 cache controller**
  - — Supports cacheless configurations as well as cache sizes of 256 Kbytes to 1 Mbyte with 32-byte line size
  - — Supports synchronous burst, pipelined synchronous, and asynchronous 3.3-V SRAM
  - — Two less wait-states for read lead-off cycle with pipelining
- **State-of-the-art DRAM controller**
  - — 3.3- and 5-V DRAM support
  - — Supports up to 256 Mbytes of system memory in four banks of 64-bit DRAM or eight banks of 32-bit DRAM
  - — Supports 256 Kbit, 512 Kbit, 1 Mbit, 2 Mbit, 4 Mbit, and 16 Mbit DRAM
  - — Supports both symmetric and asymmetric DRAM
  - — Supports mixed FPM (fast page mode), EDO (extended data output), and Burst EDO DRAM
  - — Slow and self refresh support, including hidden, staggered, CAS-before-RAS refresh or RAS-only refresh
  - — 5-2-2-2 burst read cycles with 60-ns EDO DRAM at 66 MHz
  - — 5-3-3-3 page-hit and 10-3-3-3 page-miss burst-read cycles with 60-ns standard DRAM at 66 MHz
  - — Two less wait-states in the lead-off cycle for pipeline access
  - — Supports 2-1-1-1 burst write
  - — Supports read reordering and ROM shadowing
  - — Supports ROM shadowing
  - — Supports SMM RAM size from 32 Kbyte to 128 Kbyte with easy SMI code copying to SMM RAM in normal memory mode

(cont.)

OVERVIEW

A high-performance, highly integrated system controller for Microsoft® Windows® -compatible computers, the VESUVIUS-LS supports Intel's 3.3-V Pentium® processor and comparable 5-class processors. The PCI-based VESUVIUS-LS solution is optimized for portable systems with stringent form-factor and power consumption requirements.

VESUVIUS-LS consists of three chips: V1-LS, V2-LS, and V3-LS. A 0.5µm CMOS device, VESUVIUS-LS is available in a choice of PQFPand VQFP packages. For space-critical designs, VESUVIUS-LS is also available as a die product.

The V1-LS chip integratesthe following functions:

- — CPU bus to the PCI Bus interface controller and arbiter
- — L2 cache controller
- — DRAM controller
- — Power management controller

The V2-LS serves as a data path controller, providing a 32- or 64-bit data path between the CPU and the main memory; a 32-bit data path between the CPU bus and the PCI Local Bus, and a 32-bit data path between the PCI Local Bus and the main memory.

The V3-LS chip completes the VESUVIUS-LS solution by providing a bridge between the PCI and ISA buses; it has the logic to support master and slave cycles on both PCI and ISA buses.

The VESUVIUS-LS supports 3.3-V Pentium® and other 5-class processors with speeds up to 166 MHz. It connects the 5-class processor bus to the PCI Local Bus and provides a bridge between the PCI and ISA buses to support ISA bus peripherals.

(cont.)

FEATURES (cont.)

- **PCI Local Bus architecture**
  - — Supports 25- to 33-MHz PCI bus speeds
  - — Supports 3.3- or 5-V 32-bit PCI Local Bus
  - — Synchronous interface between the CPU bus and the PCI Bus
  - — PCI Local Bus revision 2.0 compliant
  - — Supports Mobile PCI specification
  - — Supports PCI burst cycles
  - — Supports up to five PCI masters and ten PCI loads
  - — Integrated PCI Bus arbiter with rotating priority
  - — PCI parity and system error support
  - — Eight-level write buffers for CPU-to-PCI writes
  - — PCI interrupt steering
  - — Intelligent power management through clock scaling
- **Best-in-class power and thermal management**
  - — Supports SMM (system management mode), SMI (system management interrupt), Stop Clock, and AutoHalt
  - — Flexible hybrid voltage implementation
  - — Optional thermal control with thermal clock throttling
  - — Supports wakeup control, interrupt-as-wakeup-source, and ring-input-as-wakeup source
  - — Supports 3.3-V processor bus, 3.3-V/5-V PCI and ISA buses, 3.3-V L2 cache controller, and 3.3-V/5-V DRAM subsystem
- **Docking station support**
  - — Proprietary hot-docking arbitration interface
  - — Distributed DMA support for DMA on the PCI Bus from secondary ISA in the dock
- **PCI-to-ISA bridge**
  - — 25- to 33-MHz operation on the PCI Bus
  - — Master and slave interface for the PCI and the ISA bus
  - — PCI-to-ISA and ISA-to-PCI Bus cycle translations
  - — Eight-bit BIOS ROM, FLASH EPROM support
- **Available in a choice of space-efficient VQFP or PQFP packages or die**
  - — **Option one:** 208-pin VQFP (V1-LS and V2-LS) and 176-pin VQFP (V3-LS) packages
  - — **Option two:** 208-pin PQFP (V1-LS, V2-LS, and V3-LS) packages
  - — **Option three:** Die (V1-LS and V2-LS) and 176-pin VQFP/208-pin PQFP (V3-LS)

OVERVIEW (cont.)

It takes full advantage of the 5-class processor performance by supporting CPU bus frequencies of up to 66 MHz.

An integrated, 64-bit, direct-mapped level-2 cache controller supports synchronous burst, pipelined synchronous, and asynchronous 3.3-V SRAM. Additionally, buffered write-through cache update schemes allow further performance gains.

By providing a sophisticated DRAM controller which supports leading-edge DRAM technology, the VESUVIUS-LS system solution has been optimized for a cacheless system configuration. The DRAM controller implements the logic required to use advanced, high-speed DRAM that reduces the performance overhead of level-2 cache miss cycles. It implements a synchronous interface between the CPU and PCI buses to exploit the maximum potential of the PCI bandwidth.

VESUVIUS-LS system solution offers superior power and thermal management. It also features a thermal control mechanism that uses CPU clock throttling to efficiently control the power consumption and heat dissipation associated with the processor. An innovative programming model simplifies BIOS development without compromising any of the power management features.

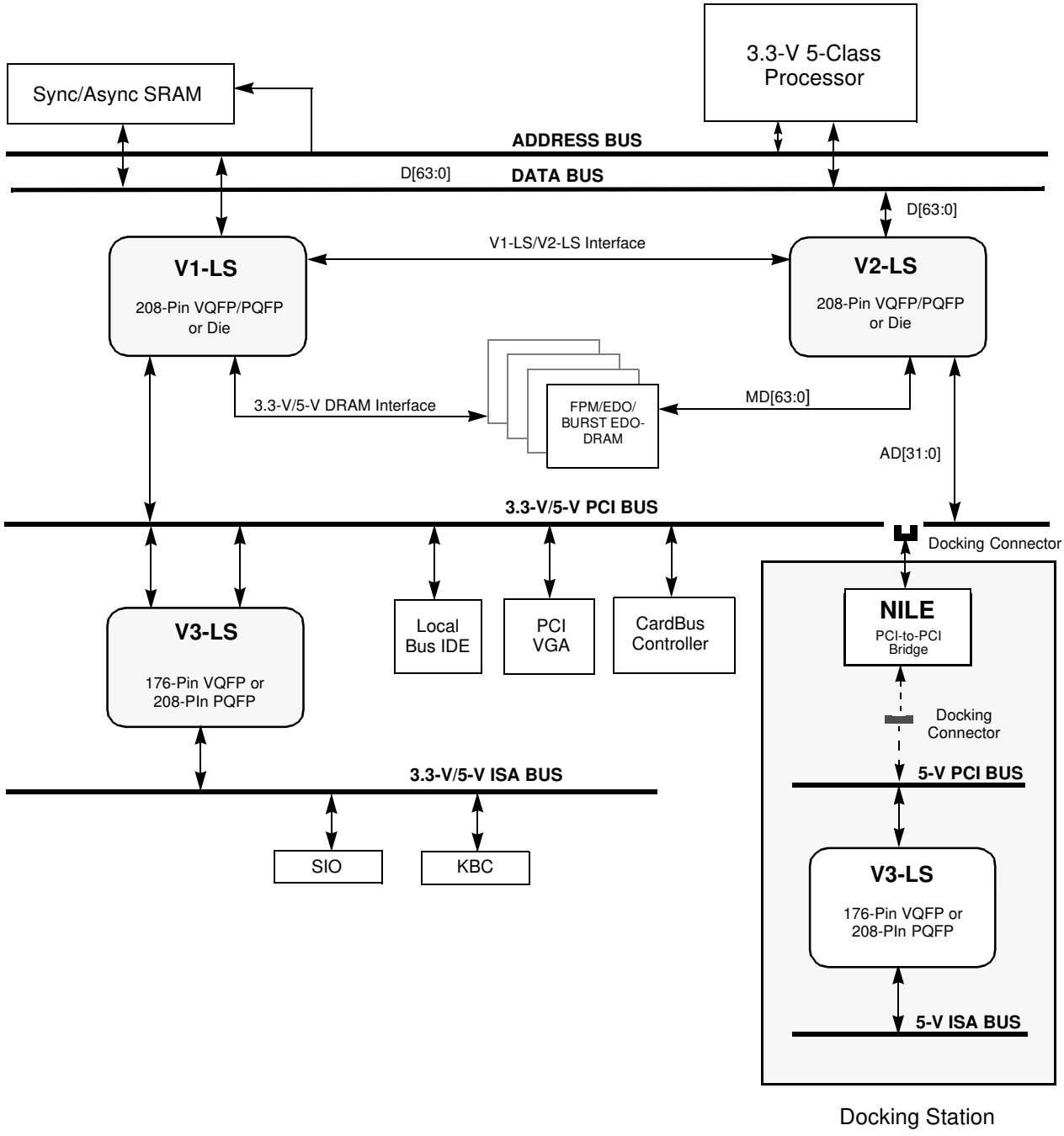
To enable a full-featured docking station design, VESUVIUS-LS portable system solution provides the necessary hooks to support PCI hot- and warm-docking. By supporting a secondary ISA bus in the PCI docking station, it allows both PCI and ISA slots in the docking station.

VESUVIUS-LS implements a Distributed DMA scheme to support ISA legacy devices in the PCI docking station. It can be programmed as positive decoding (primary V3-LS in the portable system) or subtractive decoding (secondary V3-LS in the dock).

VESUVIUS-LS comes with full technical and hardware support, including samples, evaluation boards, and design examples in OrCAD®.

System Block Diagram

Portable System With PCI Docking Station



SCOPE OF DOCUMENT

This document provides the system designer and programmer with comprehensive technical information about VESUVIUS-LS Pentium processor PCI system controller. **Information contained in this data book covers all silicon revisions up to and including Revision CC.** To assist both evaluation and system design, the material has been organized as follows:

- **VESUVIUS-LS Overview**
- **Section 1: V1-LS PT86C521 Data Book**
- **Section 2: V2-LS PT86C522 Data Book**
- **Section 3: V3-LS PT86C523 Data Book**
- **Appendixes**

PRODUCT INFORMATION

For information on product availability, pricing, and order status, contact your local National Semiconductor representative or the nearest sales office. A list of Direct Sales Offices can be found on the back cover of this document.

CONVENTIONS

This section lists conventions used in this document.

- For easy cross-referencing, the pin lists have been organized both numerically and alphabetically.
- ***Shading has been used to indicate changes in register information related to Revision BB and CC silicon***
- Signal groups that act together as a bus are shown with the individual numbered lines grouped in brackets and separated by a colon. For example, Power Control pins 0-3 are shown as PC[3:0]
- The word “assert” refers to driving a signal true or active.
- Hexadecimal numbers are suffixed with an ‘H’. For example, 00H.

ABBREVIATIONS

List of Abbreviations for Units of Measure

Units of Measure	Symbol Used
megahertz	MHz
kilobyte (1,024 bytes)	Kbyte
megabyte	Mbyte
microsecond	µs
nanosecond	ns

The use of ‘TBD’ indicates values that are to be determined; ‘n/a’ designates ‘not available’, and ‘NC’ indicates a pin that is ‘no connect’.

ACRONYMS

List of Acronyms

Acronym	Definition
APM	advanced power management
CAS	column address strobe
EDO	extended data output
FPM	fast page mode
P/A	primary activity
PCI	peripheral component interconnect
PM	power management
PMC	power management controller
PQFP	plastic quad-flat pack
RAS	row address strobe
RTC	real-time clock
R/W	read/write
S/A	secondary activity
SC	serial clock
SMI	system management interrupt
SMM	system management mode
STD	suspend-to-disk mode
STR	suspend-to-RAM mode

Table of Contents

SECTION 1: V1-LS PT86C521 DATA BOOK

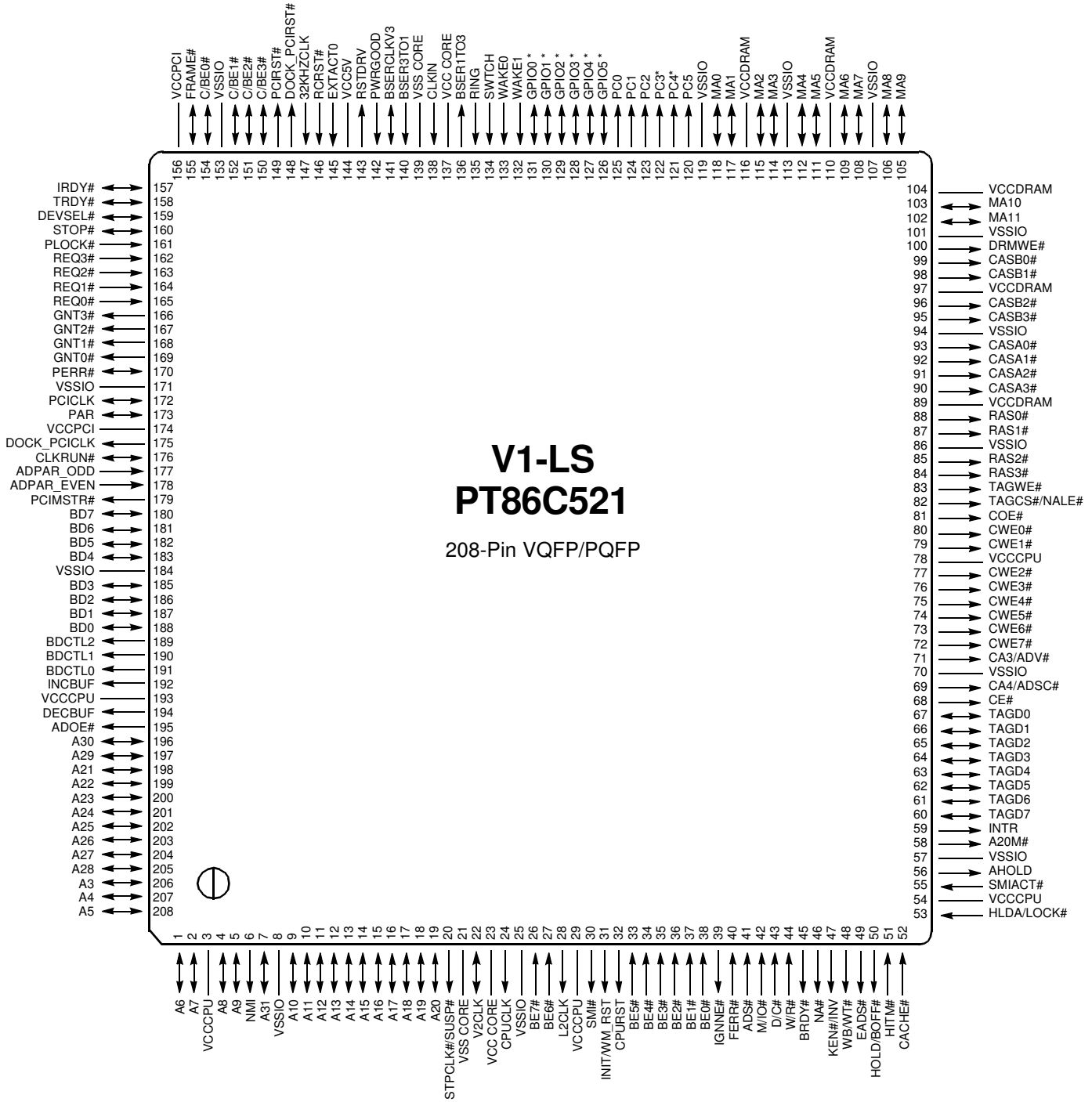
SECTION 2: V2-LS PT86C522 DATA BOOK

SECTION 3: V3-LS PT86C523 DATA BOOK

V1-LS PT86C521
Data Book

1. V1-LS PIN INFORMATION

1.1 Pin Diagram



NOTE: Multiplexed GPIO and PC signals are shown with an asterisk (*). Refer to Section 4.4.60 on page 1-193 for additional details on the multiplexing scheme.

1.2 Pin Cross Reference by Pin Numbe r

Table 1-1. Pin Assignment T able (Arranged by Pin Number)

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
1	A6	I/O	T	3.3-V	VCCCPU	CPU
2	A7	I/O	T	3.3-V	VCCCPU	CPU
3	VCCCPU	PWR		3.3-V	VCCCPU	POWER
4	A8	I/O	T	3.3-V	VCCCPU	CPU
5	A9	I/O	T	3.3-V	VCCCPU	CPU
6	NMI	O		3.3-V	VCCCPU	CPU
7	A31	I/O	T	3.3-V	VCCCPU	CPU
8	VSSIO	GND			VSSIO	GROUND
9	A10	I/O	T	3.3-V	VCCCPU	CPU
10	A11	I/O	T	3.3-V	VCCCPU	CPU
11	A12	I/O	T	3.3-V	VCCCPU	CPU
12	A13	I/O	T	3.3-V	VCCCPU	CPU
13	A14	I/O	T	3.3-V	VCCCPU	CPU
14	A15	I/O	T	3.3-V	VCCCPU	CPU
15	A16	I/O	T	3.3-V	VCCCPU	CPU
16	A17	I/O	T	3.3-V	VCCCPU	CPU
17	A18	I/O	T	3.3-V	VCCCPU	CPU
18	A19	I/O	T	3.3-V	VCCCPU	CPU
19	A20	I/O	T	3.3-V	VCCCPU	CPU
20	STPCLK#/SUSP#	O		3.3-V	VCCCPU	CPU
21	VSS CORE	GND			VSSC	GROUND
22	V2CLK	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
23	VCC CORE	PWR		3.3-V	VCC CORE	POWER
24	CPUCLK	O		3.3-V	VCCCPU	CPU
25	VSSIO	GND			VSSIO	GROUND
26	BE7#	I	T	3.3-V	VCCCPU	CPU
27	BE6#	I	T	3.3-V	VCCCPU	CPU
28	L2CLK	O		3.3-V	VCCCPU	L2 CACHE
29	VCCCPU	PWR		3.3-V	VCCCPU	POWER

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 1-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
30	SMI#	O		3.3-V	VCCCPU	CPU
31	INIT/WM_RST	O		3.3-V	VCCCPU	CPU
32	CPURST	O		3.3-V	VCCCPU	CPU
33	BE5#	I	T	3.3-V	VCCCPU	CPU
34	BE4#	I	T	3.3-V	VCCCPU	CPU
35	BE3#	I	T	3.3-V	VCCCPU	CPU
36	BE2#	I	T	3.3-V	VCCCPU	CPU
37	BE1#	I	T	3.3-V	VCCCPU	CPU
38	BE0#	I	T	3.3-V	VCCCPU	CPU
39	IGNNE#	O		3.3-V	VCCCPU	CPU
40	FERR#	I	T	3.3-V	VCCCPU	CPU
41	ADS#	I	T	3.3-V	VCCCPU	CPU
42	M/IO#	I	T	3.3-V	VCCCPU	CPU
43	D/C#	I	T	3.3-V	VCCCPU	CPU
44	W/R#	I	T	3.3-V	VCCCPU	CPU
45	BRDY#	O		3.3-V	VCCCPU	CPU
46	NA#	O		3.3-V	VCCCPU	CPU
47	KEN#/INV	O		3.3-V	VCCCPU	CPU
48	WB/WT#	O		3.3-V	VCCCPU	CPU
49	EADS#	O		3.3-V	VCCCPU	CPU
50	HOLD/BOFF#	O		3.3-V	VCCCPU	CPU
51	HITM#	I	T	3.3-V	VCCCPU	CPU
52	CACHE#	I	T	3.3-V	VCCCPU	CPU
53	HLDA/LOCK#	I	T	3.3-V	VCCCPU	CPU
54	VCCCPU	PWR		3.3-V	VCCCPU	POWER
55	SMIACT#	I	T	3.3-V	VCCCPU	CPU
56	AHOLD	O		3.3-V	VCCCPU	CPU
57	VSSIO	GND			VSSIO	GROUND
58	A20M#	O		3.3-V	VCCCPU	CPU
59	INTR	O		3.3-V	VCCCPU	CPU

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 1-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
60	TAGD7	I/O	T	3.3-V	VCCCPU	L2 CACHE
61	TAGD6	I/O	T	3.3-V	VCCCPU	L2 CACHE
62	TAGD5	I/O	T	3.3-V	VCCCPU	L2 CACHE
63	TAGD4	I/O	T	3.3-V	VCCCPU	L2 CACHE
64	TAGD3	I/O	T	3.3-V	VCCCPU	L2 CACHE
65	TAGD2	I/O	T	3.3-V	VCCCPU	L2 CACHE
66	TAGD1	I/O	T	3.3-V	VCCCPU	L2 CACHE
67	TAGD0	I/O	T	3.3-V	VCCCPU	L2 CACHE
68	CE#	O		3.3-V	VCCCPU	L2 CACHE
69	CA4/ADSC#	O		3.3-V	VCCCPU	L2 CACHE
70	VSSIO	GND			VSSIO	GROUND
71	CA3/ADV#	O		3.3-V	VCCCPU	L2 CACHE
72	CWE7#	O		3.3-V	VCCCPU	L2 CACHE
73	CWE6#	O		3.3-V	VCCCPU	L2 CACHE
74	CWE5#	O		3.3-V	VCCCPU	L2 CACHE
75	CWE4#	O		3.3-V	VCCCPU	L2 CACHE
76	CWE3#	O		3.3-V	VCCCPU	L2 CACHE
77	CWE2#	O		3.3-V	VCCCPU	L2 CACHE
78	VCCCPU	PWR		3.3-V	VCCCPU	POWER
79	CWE1#	O		3.3-V	VCCCPU	L2 CACHE
80	CWE0#	O		3.3-V	VCCCPU	L2 CACHE
81	COE#	O		3.3-V	VCCCPU	L2 CACHE
82	TAGCS#/NALE#	O		3.3-V	VCCCPU	L2 CACHE
83	TAGWE#	O		3.3-V	VCCCPU	L2 CACHE
84	RAS3#	O		3.3-V/5-V	VCCDRAM	DRAM
85	RAS2#	O		3.3-V/5-V	VCCDRAM	DRAM
86	VSSIO	GND			VSSIO	GROUND
87	RAS1#	O		3.3-V/5-V	VCCDRAM	DRAM
88	RAS0#	O		3.3-V/5-V	VCCDRAM	DRAM
89	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 1-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
90	CASA3#	O		3.3-V/5-V	VCCDRAM	DRAM
91	CASA2#	O		3.3-V/5-V	VCCDRAM	DRAM
92	CASA1#	O		3.3-V/5-V	VCCDRAM	DRAM
93	CASA0#	O		3.3-V/5-V	VCCDRAM	DRAM
94	VSSIO	GND			VSSIO	GROUND
95	CASB3#	O		3.3-V/5-V	VCCDRAM	DRAM
96	CASB2#	O		3.3-V/5-V	VCCDRAM	DRAM
97	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER
98	CASB1#	O		3.3-V/5-V	VCCDRAM	DRAM
99	CASB0#	O		3.3-V/5-V	VCCDRAM	DRAM
100	DRMWE#	O		3.3-V/5-V	VCCDRAM	DRAM
101	VSSIO	GND			VSSIO	GROUND
102	MA11	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
103	MA10	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
104	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER
105	MA9	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
106	MA8	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
107	VSSIO	GND			VSSIO	GROUND
108	MA7	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
109	MA6	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
110	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER
111	MA5	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
112	MA4	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
113	VSSIO	GND			VSSIO	GROUND
114	MA3	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
115	MA2	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
116	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER
117	MA1	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
118	MA0	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
119	VSSIO	GND			VSSIO	GROUND

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 1-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
120	PC5	O		5-V	VCC-5V	PMC
121	PC4*	O		5-V	VCC-5V	PMC
122	PC3*	O		5-V	VCC-5V	PMC
123	PC2	O		5-V	VCC-5V	PMC
124	PC1	O		5-V	VCC-5V	PMC
125	PC0	O		5-V	VCC-5V	PMC
126	GPIO5*	I/O	T	5-V	VCC-5V	PMC
127	GPIO4*	I/O	T	5-V	VCC-5V	PMC
128	GPIO3*	I/O	T	5-V	VCC-5V	PMC
129	GPIO2*	I/O	T	5-V	VCC-5V	PMC
130	GPIO1*	I/O	T	5-V	VCC-5V	PMC
131	GPIO0*	I/O	T	5-V	VCC-5V	PMC
132	WAKE1	I	T	5-V	VCC-5V	PMC
133	WAKE0	I	T	5-V	VCC-5V	PMC
134	SWTCH	I	T	5-V	VCC-5V	PMC
135	RING	I	T	5-V	VCC-5V	PMC
136	BSER1TO3	O		5-V	VCC-5V	V1-LS/V3-LS
137	VCC CORE	PWR		3.3-V	VCC CORE	POWER
138	CLKIN	I	C	5-V	VCC-5V	CLOCK
139	VSS CORE	GND			VSSC	GROUND
140	BSER3TO1	I	T	5-V	VCC-5V	V1-LS/V3-LS
141	BSERCLKV3	I/O	T	5-V	VCC-5V	V1-LS/V3-LS
142	PWRGOOD	I	T	5-V	VCC-5V	RESET
143	RSTDRV	O		5-V	VCC-5V	RESET
144	VCC5V	PWR		5-V	VCC-5V	POWER
145	EXTACT0	I	T	5-V	VCC-5V	PMC
146	RCRST#	I	T	5-V	VCC-5V	RESET
147	32KHZCLK	I	S	5-V	VCC-5V	CLOCK
148	DOCK_PCIRST#	O		3.3-V/5-V	VCCPCI	PCI
149	PCIRST#	O		3.3-V/5-V	VCCPCI	PCI

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 1-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
150	C/BE3#	I/O	T	3.3-V/5-V	VCCPCI	PCI
151	C/BE2#	I/O	T	3.3-V/5-V	VCCPCI	PCI
152	C/BE1#	I/O	T	3.3-V/5-V	VCCPCI	PCI
153	VSSIO	GND			VSSIO	GROUND
154	C/BE0#	I/O	T	3.3-V/5-V	VCCPCI	PCI
155	FRAME#	I/O	T	3.3-V/5-V	VCCPCI	PCI
156	VCCPCI	PWR			VCCPCI	POWER
157	IRDY#	I/O	T	3.3-V/5-V	VCCPCI	PCI
158	TRDY#	I/O	T	3.3-V/5-V	VCCPCI	PCI
159	DEVSEL#	I/O	T	3.3-V/5-V	VCCPCI	PCI
160	STOP#	I/O	T	3.3-V/5-V	VCCPCI	PCI
161	PLOCK#	I	T	3.3-V/5-V	VCCPCI	PCI
162	REQ3#	I	T	3.3-V/5-V	VCCPCI	PCI
163	REQ2#	I	T	3.3-V/5-V	VCCPCI	PCI
164	REQ1#	I	T	3.3-V/5-V	VCCPCI	PCI
165	REQ0#	I	T	3.3-V/5-V	VCCPCI	PCI
166	GNT3#	O		3.3-V/5-V	VCCPCI	PCI
167	GNT2#	O		3.3-V/5-V	VCCPCI	PCI
168	GNT1#	O		3.3-V/5-V	VCCPCI	PCI
169	GNT0#	O		3.3-V/5-V	VCCPCI	PCI
170	PERR#	I/O	T	3.3-V/5-V	VCCPCI	PCI
171	VSSIO	GND			VSSIO	GROUND
172	PCICLK	I/O	T	3.3-V/5-V	VCCPCI	PCI
173	PAR	I/O	T	3.3-V/5-V	VCCPCI	PCI
174	VCCPCI	PWR			VCCPCI	POWER
175	DOCK_PCICLK	O		3.3-V/5-V	VCCPCI	PCI
176	CLKRUN#	I/O	T	3.3-V/5-V	VCCPCI	PCI
177	ADPAR_ODD	I	T	3.3-V	VCCCPU	V1-LS/V2-LS
178	ADPAR_EVEN	I	T	3.3-V	VCCCPU	V1-LS/V2-LS
179	PCIMSTR#	O		3.3-V	VCCCPU	V1-LS/V2-LS

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 1-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
180	BD7	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
181	BD6	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
182	BD5	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
183	BD4	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
184	VSSIO	GND			VSSIO	GROUND
185	BD3	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
186	BD2	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
187	BD1	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
188	BD0	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
189	BDCTL2	O		3.3-V	VCCCPU	V1-LS/V2-LS
190	BDCTL1	O		3.3-V	VCCCPU	V1-LS/V2-LS
191	BDCTL0	O		3.3-V	VCCCPU	V1-LS/V2-LS
192	INCBUF	O		3.3-V	VCCCPU	V1-LS/V2-LS
193	VCCCPU	PWR		3.3-V	VCCCPU	POWER
194	DECBUF	O		3.3-V	VCCCPU	V1-LS/V2-LS
195	ADOE#	O		3.3-V	VCCCPU	V1-LS/V2-LS
196	A30	I/O	T	3.3-V	VCCCPU	CPU
197	A29	I/O	T	3.3-V	VCCCPU	CPU
198	A21	I/O	T	3.3-V	VCCCPU	CPU
199	A22	I/O	T	3.3-V	VCCCPU	CPU
200	A23	I/O	T	3.3-V	VCCCPU	CPU
201	A24	I/O	T	3.3-V	VCCCPU	CPU
202	A25	I/O	T	3.3-V	VCCCPU	CPU
203	A26	I/O	T	3.3-V	VCCCPU	CPU
204	A27	I/O	T	3.3-V	VCCCPU	CPU
205	A28	I/O	T	3.3-V	VCCCPU	CPU
206	A3	I/O	T	3.3-V	VCCCPU	CPU
207	A4	I/O	T	3.3-V	VCCCPU	CPU
208	A5	I/O	T	3.3-V	VCCCPU	CPU

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

1.3 Pin Cross Reference by Pin Name

Table 1-2. Pin Assignment Table (Arranged by Pin Name)

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
32KHZCLK	147	A30	196	BSER3TO1	140
A3	206	A31	7	C/BE0#	154
A4	207	ADOE#	195	C/BE1#	152
A5	208	ADPAR_EVEN	178	C/BE2#	151
A6	1	ADPAR_ODD	177	C/BE3#	150
A7	2	ADS#	41	CA3/ADV#	71
A8	4	AHOLD	56	CA4/ADSC#	69
A9	5	BD0	188	CACHE#	52
A10	9	BD1	187	CASA0#	93
A11	10	BD2	186	CASA1#	92
A12	11	BD3	185	CASA2#	91
A13	12	BD4	183	CASA3#	90
A14	13	BD5	182	CASB0#	99
A15	14	BD6	181	CASB1#	98
A16	15	BD7	180	CASB2#	96
A17	16	BDCTL0	191	CASB3#	95
A18	17	BDCTL1	190	CE#	68
A19	18	BDCTL2	189	CLKIN	138
A20	19	BE0#	38	CLKRUN#	176
A20M#	58	BE1#	37	COE#	81
A21	198	BE2#	36	CPUCLK	24
A22	199	BE3#	35	CPURST	32
A23	200	BE4#	34	CWE0#	80
A24	201	BE5#	33	CWE1#	79
A25	202	BE6#	27	CWE2#	77
A26	203	BE7#	26	CWE3#	76
A27	204	BRDY#	45	CWE4#	75
A28	205	BSERCLKV3	141	CWE5#	74
A29	197	BSER1TO3	136	CWE6#	73

Table 1-2. Pin Assignment Table (Arranged by Pin Name) *(cont.)*

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
CWE7#	72	M/IO#	42	RAS3#	84
D/C#	43	MA0	118	RCRST#	146
DECBUF	194	MA1	117	REQ0#	165
DEVSEL	159	MA2	115	REQ1#	164
DOCK_PCICLK	175	MA3	114	REQ2#	163
DOCK_PCIRST#	148	MA4	112	REQ3#	162
DRMWE#	100	MA5	111	RING	135
EADS#	49	MA6	109	RSTDRV	143
EXTACT0	145	MA7	108	SMI#	30
FERR#	40	MA8	106	SMIACT#	55
FRAME#	155	MA9	105	STOP#	160
GNT0#	169	MA10	103	STPCLK#/SUSP#	20
GNT1#	168	MA11	102	SWTCH	134
GNT2#	167	NA#	46	TAGCS#/NALE#	82
GNT3#	166	NMI	6	TAGD0	67
GPIO0*	131	PAR	173	TAGD1	66
GPIO1*	130	PC0	125	TAGD2	65
GPIO2*	129	PC1	124	TAGD3	64
GPIO3*	128	PC2	123	TAGD4	63
GPIO4*	127	PC3*	122	TAGD5	62
GPIO5*	126	PC4*	121	TAGD6	61
HITM#	51	PC5	120	TAGD7	60
HLDA/LOCK#	53	PCICLK	172	TAGWE#	83
HOLD/BOFF#	50	PCIMSTR#	179	TRDY#	158
IGNNE#	39	PCIRST#	149	V2CLK	22
INCBUF	192	PERR#	170	VCC5-V	144
INIT/WM_RST	31	PLOCK#	161	VCC CORE	23
INTR	59	PWRGOOD	142	VCC CORE	137
IRDY#	157	RAS0#	88	VCCCPU	3
KEN#/INV	47	RAS1#	87	VCCCPU	29
L2CLK	28	RAS2#	85	VCCCPU	54

Table 1-2. Pin Assignment Table (Arranged by Pin Name) *(cont.)*

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
VCCCPU	78	VSS CORE	139	VSSIO	113
VCCCPU	193	VSSIO	8	VSSIO	119
VCCDRAM	89	VSSIO	25	VSSIO	153
VCCDRAM	97	VSSIO	57	VSSIO	171
VCCDRAM	104	VSSIO	70	VSSIO	184
VCCDRAM	110	VSSIO	86	W/R#	44
VCCDRAM	116	VSSIO	94	WAKE0	133
VCCPCI	156	VSSIO	101	WAKE1	132
VCCPCI	174	VSSIO	107	WB/WT#	48
VSS CORE	21				

2. V1-LS DETAILED PIN DESCRIPTIONS

This chapter contains a detailed functional description of the pins on PT86C521. For ease of reference, the pins are arranged alphabetically within each of the following functional interface groups:

- CPU Interface (CPU)
- DRAM Interface (DRAM)
- L2 Cache Interface (L2 CACHE)
- PCI Interface (PCI)
- Power Management Interface (PMC)
- PT86C521 / V2-LS Interface (V1-LS / V2-LS)
- V1-LS / V3-LS Interface (V1-LS / V3-LS)
- Reset and Clock Interface (RESET / CLOCK)
- Power and Ground (POWER / GROUND)

The '#' symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. Signal names without the '#' symbol indicate that the signal is active, or asserted at the high voltage level.

The '/' symbol between signal names indicates that the signals are multiplexed or have dual functionality and use the same pin for all functions.

The following conventions have been used to describe the pin type: 'I' = input-only pins; 'O' = output-only pins; 'I/O' = bi-directional pins; 'PWR' = power pins, and 'GND' = ground pins. The pin type is defined relative to the V1-LS device.

For a list of pins arranged by pin number, refer to Section 1.2 on page 1-15. For a list of pins arranged by pin name, refer to Section 1.3 on page 1-22

2.1 CPU Interface

Pin Name	Type	Description
A20M#	O	**ADDRESS BIT 20 MASK#** : This output to the CPU indicates that the CPU should mask A20 in order to emulate the 8086 address wrap-around.
A[31:3]	I/O	**CPU ADDRESS LINES [31:3]** : These are address lines that together with the byte enable signals (BE[7:0]#) make the address bus and define the physical area of memory or I/O accessed; they are driven as outputs during bus master cycles.

2.1 CPU Interface *(cont.)*

Pin Name	Type	Description
ADS#	I	**ADDRESS STROBE#** : This input indicates the presence of a new valid bus cycle currently being driven by the CPU. ADS# is driven active in the first clock of a bus cycle and is driven inactive in the second or subsequent clocks of the cycle. ADS# is driven inactive when the bus is idle.
AHOLD	O	**ADDRESS HOLD** : This output is used in conjunction with EADS# for write-protecting a cacheable ROM region.
BE[7:0]#	I	**CPU BYTE ENABLE [7:0]** : The byte enable pins are used to determine which bytes must be written to memory, or which bytes were requested by the processor for the current cycle. They help define the physical area of the memory or I/O accessed. Byte enable pins are driven in the same clock as ADS#. They are driven with the same timing as the address lines A[31:3].
BRDY#	O	**BURST READY#:** This output to the Pentium processor indicates completion of the current cycle. BRDY# indicates that the V2-LS has presented valid data in response to a read, or that it has accepted the data from the Pentium processor in response to a write request.
CACHE#	I	**CACHE#:** This input from the Pentium processor indicates a CPU cacheable/burstable operation.
CPUCLK	O	**CPU CLOCK OUTPUT:** This will be the clock output from V1-LS to the CPU.
CPURST	O	**CPU RESET:** This output resets the CPU.
D/C#	I	**DATA_CODE#:** This cycle-definition input from the Pentium processor indicates whether the current cycle is a data or a code/special access. The D/C# pin is driven valid in the same clock as ADS# and the cycle address. It remains valid from the clock in which ADS# is asserted until the clock after the earlier of NA# or the last BRDY#.
EADS#	O	**EXTERNAL ADDRESS STROBE#:** This output to the Pentium processor indicates that a valid address has been driven onto the CPU address bus for internal cache snoop cycle.
FERR#	I	**FLOATING-POINT ERROR#:** This output pin from the Pentium processor is used for floating-point error reporting.
HITM#	I	**HITM#:** This input indicates that the snoop cycle hit a modified line in the level-1 cache inside the CPU such that V1-LS should suspend the master operation, allow the CPU to evict the modified line, and then restart the master cycle.

2.1 CPU Interface *(cont.)*

Pin Name	Type	Description
HLDA/LOCK#	I	**HOLD ACKNOWLEDGE:** This input from the Pentium processor indicates a Hold Acknowledge state. **LOCK#:** Indicates to the system that the current sequence of bus cycles should not be interrupted.**Note:** This pin applies to Revision CC only.
HOLD/BOFF#	O	**HOLD REQUEST:** This output to the Pentium processor indicates a Hold Request state. **BACK OFF#:** The back off input is used to force the Pentium processor off the bus in the next clock.**Note:** This pin applies to Revision CC only.
IGNNE#	O	**IGNORE NUMERIC ERROR#:** This pin indicates that a floating-point error should be ignored.
INIT/WM_RST	O	**INIT:** This Pentium processor initialization input forces the Pentium processor to begin execution in a known state. The INIT/WM_RST will typically be asserted when software reset commands are written to either Port 64 or 92, or a shutdown cycle is detected. **WM_RST:** Cyrix 6x86 processor initialization input forces the processor to begin execution in a known state.
INTR	O	**MASKABLE INTERRUPT:** This pin indicates a maskable interrupt request to the Pentium processor.
INV	O	See KEN#.
KEN#/INV	O	**CACHE ENABLE# :** This output to the Pentium processor indicates that the current cycle is cacheable. **INV:** This output pin indicates a request to invalidate the processor cache line during snoop cycles. If this function is not used, CPU's INV pin should either be pulled high or connected to W/R#.
M/IO#	I	**MEMORY_INPUT & OUTPUT#:** This cycle-definition signal is one of the main pins that define the bus cycle. It distinguishes a memory access from an I/O access. This signal is driven valid in the same clock as ADS# and the cycle address. It remains valid from the clock in which ADS# is asserted until the clock after earlier of NA# or the last BRDY#.
NA#	O	**NEXT ADDRESS #:** NA# indicates to the Pentium processor that V1-LS is ready to accept a new bus cycle. This signal is used for CPU's pipelining feature.

2.1 CPU Interface *(cont.)*

Pin Name	Type	Description
NMI	O	**NON-MASKABLE INTERRUPT:** This pin indicates that an external non-maskable interrupt has been generated.
SMI#	O	**SYSTEM MANAGEMENT INTERRUPT#:** This output triggers a system management interrupt and is used to invoke the SMM (system management mode).
SMIACT#	I	**SYSTEM MANAGEMENT INTERRUPT ACTIVE#:** This input from the Pentium processor indicates that the CPU is operating in SMM. Assertion of SMIACT# enables remapping of SMRAM to physical DRAM at 000A0000-000BFFFF region.
STPCLK#/SUSP#	O	**STOP CLOCK#:** This output indicates a stop clock request to Intel's Pentium and AMD's K5 processor. **SUSP#:** This output indicates a suspend request to Cyrix® 6x86 CPU.
SUSP#	O	See STPCLK#.
W/R#	I	**WRITE_READ#:** This is a cycle-definition input from the processor indicating whether the current cycle is a write or a read cycle. It is one of the primary bus cycle-definition pins. W/R# is driven valid in the same clock as ADS# and the cycle address. It remains valid from the clock in which ADS# is asserted until the clock after earlier of NA# or the last BRDY#.
WB/WT#	O	**WRITE-BACK_WRITE-THROUGH#:** This output to the processor allows a data cache line to be defined as write-back or write-through on a line-by-line basis.
WM_RST	O	See INIT.

2.2 DRAM Interface

Pin Name	Type	Description
CASA[3:0]# CASB[3:0]#	O	**COLUMN ADDRESS STROBES [3:0] GROUPS A AND B# :** In 64-bit bank mode, CASA[3:0]# corresponds to BE[3:0]# and CASB[3:0]# corresponds to BE[7:4]#. In 32-bit bank mode CASA[3:0]# outputs drive the CAS# inputs on DRAM bytes 3 to 0 in even banks (banks 0, 2, 4, 6) and CASB[3:0]# for odd banks (banks 1, 3, 5, 7).

2.2 DRAM Interface *(cont.)*

Pin Name	Type	Description
DRMWE#	O	**DRAM WRITE ENABLE# :** This output drives write-enable for all DRAM.
MA[11:0]	I/O	**MEMORY ADDRESSES [11:0] :** These outputs drive the MA lines for all DRAM. They are also used as RC-RESET configuration inputs during power up (on RCRST# rising edge).
RAS[3:0]#	O	**ROW ADDRESS STROBES [3:0]# :** These outputs drive the RAS# inputs on DRAM bank pairs 7/6, 5/4, 3/2, and 1/0 respectively.

2.3 L2 Cache Interface

Pin Name	Type	Description
ADSC#	O	See CA4.
ADV#	O	See CA3.
CA3/ADV#	O	**CACHE ADDRESS 3 :** Cache Data RAM address bits used for cache burst sequencing with asynchronous SRAM. **ADVANCE# :** This active-low output is used with synchronous SRAM to advance the internal SRAM burst counter, controlling burst accesses after the address is loaded.
CA4/ADSC#	O	**CACHE ADDRESS 4 :** Cache Data RAM address bits used for cache burst sequencing with asynchronous SRAM. **ADDRESS STATUS CONTROLLER# :** This active-low output is used with synchronous SRAM and interrupts any ongoing SRAM burst, causing a new address to be registered.
CE#	O	**CHIP ENABLE# :** Cache data RAM chip enable.
COE#	O	**CACHE OUTPUT ENABLE# :** Cache Data RAM output enable.
CWE[7:0]#	O	**CACHE WRITE ENABLE [7:0]# :** Cache data RAM byte write enables.
L2CLK	O	**L2 CLOCK:** This pin is a clock output to synchronous cache data RAM.
NALE#	O	See TAGCS#.

2.3 L2 Cache Interface *(cont.)*

Pin Name	Type	Description
TAGCS#/NALE#	O	**TAG RAM CHIP SELECT# :** TAG Data RAM chip select. **NEXT ADDRESS LATCH ENABLE# :** When using asynchronous SRAM, this output controls an external latch for the cache addresses necessary for pipelining.
TAGD[7:0]	I/O	**TAG RAM DATA BIT [7:0]:** These pins are used to compare addresses from the Pentium processor to determine L2 Cache cycles.
TAGWE#	O	**TAG RAM WRITE ENABLE# :** TAG Data RAM write enable.

2.4 PCI Interface

Pin Name	Type	Description
C/BE[3:0]#	I/O	**BUS COMMAND AND BYTE ENABLES [3:0]# :** Both command and byte enables are multiplexed on the same PCI pins. These pins define the Bus Command during the address phase and are used as Byte Enables during the data phase.
CLKRUN#	I/O	**CLOCK RUN#:** Used in the PCI mobile environment, this is a sustained tristate signal used by the central resource to request permission to stop or slow CLK.
DEVSEL#	I/O	**DEVICE SELECT#:** As an output it indicates whether V1-LS system memory is the target of the current address. As an input, V1-LS sees whether or not a PCI target exists.
DOCK_PCICLK	O	**PCI CLOCK FOR DOCKING STATION:** This signal is the PCI clock for the docking station. It provides timing for all transactions on the PCI bus in the docking station and is synchronous to PCICLK.
DOCK_PCIRST#	O	**PCI RESET FOR DOCKING STATION#:** This signal is the PCI reset for the docking station. When asserted, it resets all PCI devices in the docking station.
FRAME#	I/O	**FRAME#:** FRAME# is driven by the current initiator and indicates the start and duration of the transaction. FRAME# is deasserted to indicate that the initiator is ready to complete the final data phase. A transaction may consist of one or more data transfers between the current initiator and the currently-addressed target.

2.4 PCI Interface *(cont.)*

Pin Name	Type	Description
GNT[3:0]#	O	**PCI GRANT [3:0]# :** When the bus arbiter has granted access to the master requesting the ownership of the PCI bus, the master is notified using this point-to-point signal. Each PCI bus master has its own GNT#.
IRDY#	I/O	**INITIATOR READY# :** This indicates the bus master's state of readiness to complete the current data phase. During a write, IRDY# shows that valid data is present. During a read, it indicates the bus master's readiness to accept data. IRDY# is used in conjunction with TRDY#.
PAR	I/O	**PARITY :** This indicates that all PCI agents require parity generation.
PCICLK	I/O	**PCI CLOCK:** This pin provides timing for all transactions on the PCI bus.
PCIRST#	O	**PCI RESET:** When asserted, this pin resets all PCI devices.
PERR#	I/O	**PARITY ERROR#:** This signal indicates a data parity error. It may be pulsed active by any agent that detects an error condition.
PLOCK#	I	**PLOCK#:** This signal allows the master to lock the PCI bus and the arbiter does not grant the PCI bus to a new master until this signal has been deasserted.
REQ[3:0]#	I	**PCI REQUEST [3:0]#:** This signal indicates to the arbiter that this agent requests use of the bus. This is a point-to-point signal. Every PCI bus master has its own REQ#.
STOP#	I/O	**STOP#:** This signal facilitates either master-abort or target-abort cycles.
TRDY#	I/O	**TARGET READY#:** This indicates the ability of the target device to complete the current data phase of the bus transaction. During a read phase, TRDY# indicates that the valid data is present. During a write phase, it indicates that the device is ready to accept data.

2.5 Power Management Controller Interface

Pin Name	Type	Description
EXTACT0	I	**EXTERNAL ACTIVITY 0:** This pin indicates that there is a current external activity. This input can be unmasked to trigger a primary (P/A) or secondary activity (S/A). Refer to Registers PAM2 and SAM for more information. **NOTE:** EXTACT0 cannot be unmasked to wakeup from Suspend mode. Refer to Register WMC for more information.
GPIO0/ LED0	I/O	**GENERAL PURPOSE I/O 0:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register PINMUX, bit [1:0]. **LED 0:** LED indicator output 0.
GPIO1/ LED1	I/O	**GENERAL PURPOSE I/O 1:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register PINMUX, bits [3:2]. Refer to Section 4.4.60 on page 1-193 for additional details on the GPIO multiplexing scheme. **LED 1:** LED indicator output 1.
GPIO2/ DDMARETRY/ DPSLP_IRQPA	I/O	**GENERAL PURPOSE I/O 2:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register PINMUX, bit [5:4]. Refer to Section 4.4.60 on page 1-193 for additional details on the GPIO multiplexing scheme. **DDMARETRY:** During normal operation this input to V1-LS is used to define the Distributed DMA function between V1-LS and V3-LS devices. When high, it indicates that the V3-LS device is requesting V1-LS for ownership of the PCI bus. **DEEP SLEEP IRQ PRIMARY ACTIVITY:** Before entering Deep Sleep mode, the software will set this signal to DPSLP_IRQPA. During Deep Sleep mode, this pin acts as a wake-up source due to P/A on IRQs from V3-LS.
GPIO3/ SUPRESS_RESUME	I/O	**GENERAL PURPOSE I/O 3:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register PINMUX, bit [7:6]. Refer to Section 4.4.60 on page 1-193 for additional details on the GPIO multiplexing scheme. **SUPRESS RESUME:** This pin prevents a wake-up from Suspend mode regardless of the wake-up source. For example, when the system battery is running low, this pin will prevent the battery from further drain by not resuming from Suspend mode.

2.5 Power Management Controller Interface *(cont.)*

Pin Name	Type	Description
GPIO4 SUSPA#	I/O	**GENERAL PURPOSE I/O 4:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register PINMUX, bit [9:8]. Refer to Section 4.4.60 on page 1-193 for additional details on the GPIO multiplexing scheme. **SUSPEND ACKNOWLEDGE#:** This input from the Cyrix® 6x86 CPU indicates a suspend acknowledge state.
GPIO5 /THERM	I/O	**GENERAL PURPOSE I/O 5:** This pin can also be selected as a general purpose pin. Its function can be enabled by index register PINMUX, bit [11:10]. Refer to Section 4.4.60 on page 1-193 for additional details on the GPIO multiplexing scheme. **THERMAL SENSOR INPUT:** This input allows an external thermal sensor to feed thermal information back to the thermal throttler to regulate the control of heat generated by the CPU.
LED0	O	See GPIO0 and PC3.
LED1	O	See GPIO1 and PC4.
PC[2:0]	O	**POWER CONTROL [2:0]:** This output provides individual power control for any system component. PC[2:0] will default to high on power-up reset.
PC3/ LED0	O	**POWER CONTROL 3:** This output provides individual power control for any system component. PC3 will default to low on power-up reset. Refer to Section 4.4.60 on page 1-193 for additional details on the PC multiplexing scheme. **LED 0:** LED indicator output 0.
PC4/ LED1	O	**POWER CONTROL 4:** This output provides individual power control for any system component. PC4 will default to low on power-up reset. Refer to Section 4.4.60 on page 1-193 for additional details on the PC multiplexing scheme. **LED 1:** LED indicator output 1.
PC5	O	**POWER CONTROL 5:** This output provides individual power control for any system component. PC5 will default to low on power-up reset.
RING	I	**RING:** This input provides for a 'wake-up' call from a modem. RING can be unmasked to trigger a P/A (see Register PAM2). The number of RING to wake up from the Suspend mode is programmable in Register RCC. **Note:** RING cannot be unmasked to trigger a SMI.

2.5 Power Management Controller Interface *(cont.)*

Pin Name	Type	Description
SUSPA#	I	See GPIO1.
SWTCH	I	**SWITCH:** This input is used for power management functions and can be unmasked to trigger a P/A or a SMI. The wake mask of SWTCH is default-enabled. See Section 3.2.9.10 on page 1-76 for more details.
THERM	I	See GPIO5.
WAKE[1:0]	I	**WAKE [1:0]:** These pins request V1-LS to wake up or "resume" operation if the system was previously in Suspend mode. See Section 3.2.9.10 on page 1-76 for more details.

2.6 V1-LS / V2-LS Interface

Pin Name	Type	Description
ADOE#	O	**AD BUS OUTPUT ENABLE#:** When this signal is active V2-LS drives the PCI AD bus AD[31:0].
ADPAR_ODD	I	**ODD AD BUS PARITY:** This pin is an input from V2-LS to indicate odd PCI AD Bus parity.
ADPAR_EVEN	I	**EVEN AD BUS PARITY:** This pin is an input from V2-LS to indicate even PCI AD Bus parity.
BD[7:0]	I/O	**BURST DATA BUS [7:0]:** This 8-bit bus carries different information during various phases between V1-LS and V2-LS.
BDCTL[2:0]	O	**BUFFER DATA CONTROL [2:0]:** This pin indicates a data path control signal to V2-LS.
DECBUF	O	**DECREMENT WRITE BUFFER COUNTER:** This output is used to decrease the pointer on the eight-level write buffer.
INCBUF	O	**INCREMENT WRITE BUFFER COUNTER:** This output is used to increase the pointer on the eight-level write buffer.
PCIMSTR#	O	**PCI MASTER#:** This pin indicates to V2-LS that V1-LS is responding to a PCI master cycle.
V2CLK	I/O	**V2 CLOCK:** This pin is a clock for the interface between V1-LS and V2-LS.

2.7 V1-LS / V3-LS Interface

Pin Name	Type	Description
BSER1TO3	O	**SERIAL BUS:** This pin is the serial bus interface from V1-LS to V3-LS.
BSER3TO1	I	**SERIAL BUS:** This pin is the serial bus interface from V3-LS to V1-LS.
BSERCLKV3	O	**CLOCK:** This pin indicates a clock for the serial interface between V1-LS and V3-LS.
DDMARETRY		See Section 2.5 on page 1-32.

2.8 Reset and Clock Interface

Pin Name	Type	Description
32KHZCK	I	**CLOCK:** This pin indicates the clock source used for DRAM Refresh Controller and power management functions.
CLKIN	I	**CLOCK:** This pin indicates an input clock source to the CPU clock. CMOS level 50/50 duty cycle is recommended.
PWRGOOD	I	**POWER GOOD INPUT:** This input causes a complete system reset. It is driven by the PWRGOOD signal from the power supply or a reset switch. When transitioning from low to high on power-up, PWRGOOD indicates that the external VCC is stable.
RCRST#	I	**RC RESET#:** This input is used to reset V1-LS' power management controller upon initial system power-up. It should have a pull-up resistor tied to the same power source as V1-LS' VCC-5V.
RSTDRV	O	**AT BUS RESET OUTPUT:** This output provides a system reset.

2.9 Power and Ground

Pin Name	Type	Description
VCC5-V	PWR	**VCC5-V:** These are I/O power pins for VCC-5V power plane.
VCC CORE	PWR	**VCC CORE:** These are I/O power pins for VCC CORE power plane.
VCCCPU	PWR	**VCCCPU:** These are I/O power pins for VCCCPU power plane.
VCCDRAM	PWR	**VCCDRAM:** These are I/O power pins for VCCDRAM power plane.
VCCPCI	PWR	**VCCPCI:** These are I/O power pins for VCCPCI power plane.
VSS CORE	GND	**VSSC:** These are I/O ground pins.
VSSIO	GND	**VSSIO:** These are I/O ground pins.

3. V1-LS FUNCTIONAL DESCRIPTION

This chapter provides functional information and design guidelines on chip resources and interfaces of the V1-LS device. To fully understand the functionality of the V1-LS device, it is important to become familiar with the programming model of the VESUVIUS-LS platform. The BIOS will access the V1-LS device through a 16-bit access on Port 24H (index port) and Port 26H (data port). While the V3-LS device has its own register set, it is accessed through an 8-bit access on Port 24H and 26H. Registers discussed in this chapter are referred to by their abbreviated name. For a complete list of register names and their abbreviated names, refer toSection 4.1 on page 1-78.

3.1 Power Plane Structure

The VESUVIUS-LS platform offers a flexible power plane structure to support a wide variety of system configurations. The V1-LS device has five independent power planes:

- VCC CORE
- VCCCPU
- VCCDRAM
- VCCPCI
- VCC-5V

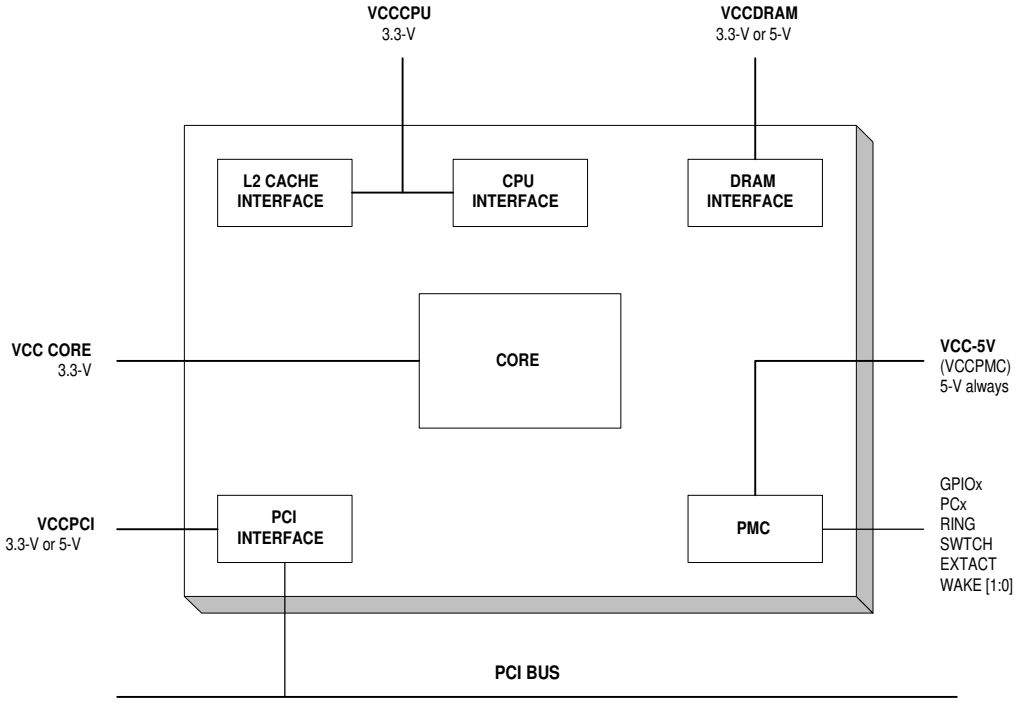


Figure 3-1. Power Plane Block Diagram

The V2-LS device has four power planes:

- VCC CORE
- VCCCPU
- VCCDRAM
- VCCPCI

Table 3-1 outlines the typical power plane usage for V1-LS and V2-LS**Power On Sequence:** If the I/O power plane is 5-V, then the 5-V power plane should be turned on first, followed by the 3.3-V planes. **Power Down Sequence:** 3.3-V planes should be turned off first, followed by the 5-V planes.

Table 3-1. Typical Power Plane Usage

Power Plane	V1-LS[1]	V2-LS
VCC CORE	always set to 3.3-V	always set to 3.3-V
VCCCPU	always set to 3.3-V	always set to 3.3-V
VCCDRAM	can be selected as 3.3-V or 5-V[2]	can be selected as 3.3-V or 5-V[1]
VCCPCI	can be selected as 3.3-V or 5-V[2]	can be selected as 3.3-V or 5-V[1]
VCC-5V	always set to 5-V	not applicable

1) During 5-V Suspend (STR) mode, though all V1-LS power planes must be kept on, all signals will be properly 'leakage-controlled.' Peripherals can be independently powered off during STR.

2) Example: Support for either 3.3-V or 5-V DRAM can be enabled simply by changing the setting for VCCDRAM.

3.1.1 Suspend-to-Disk (STD) or 0-V Suspend Mode

Figure 3-2 shows the typical design of a STD-capable portable system which can be woken up by a modem ring or RTC alarm (IRQ8). During STD all power planes of V1-LS, V2-LS, and V3-LS devices are powered off. Therefore, the RS232_RI# output from the PCMCIA controller and RS232 port or the IRQ8 from RTC are connected to an external microcontroller—typically H8 or 8051SL— through glue logic.

Figure 3-2 assumes that rising edge signals (IRQ8 and RI) are used so that the microcontroller can stay in a low-power state (around 1 µA) and wake up through its 'edge detect wakeup' feature. Both 3V_SUSP and 5V_SUSP are off, implying that RCRST# and PWRGOOD should be low. Refer to Section 3.2.9.4 on page 1-65 for a detailed discussion of the STD mode.

3.1.2 Suspend-To-RAM (STR) or 5-V/3.3-V-Suspend Mode

In the STR mode all V1-LS power planes must be kept on. It is important to note that while PC and GPIO signals are also driven, all other signals are properly leakage-controlled and devices like PCI VGA and PCI CardBus/PCMCIA controller can still be kept alive. Therefore, PCIRST# input of these PCI devices should not be asserted. This can be done by gating PCIRST# with a GPIO pin (set to high during Suspend mode) through an OR gate. On resume, the BIOS will toggle the GPIO pin back to low for normal operation. Refer to Section 3.2.9.4 on page 1-65for a detailed discussion of the STR mode.

NOTE: If used for GPIO functions, all GPIO signals should have an external pull-up or pull-down resistor. During the STR mode, RCRST# and PWRGOOD must be kept high.

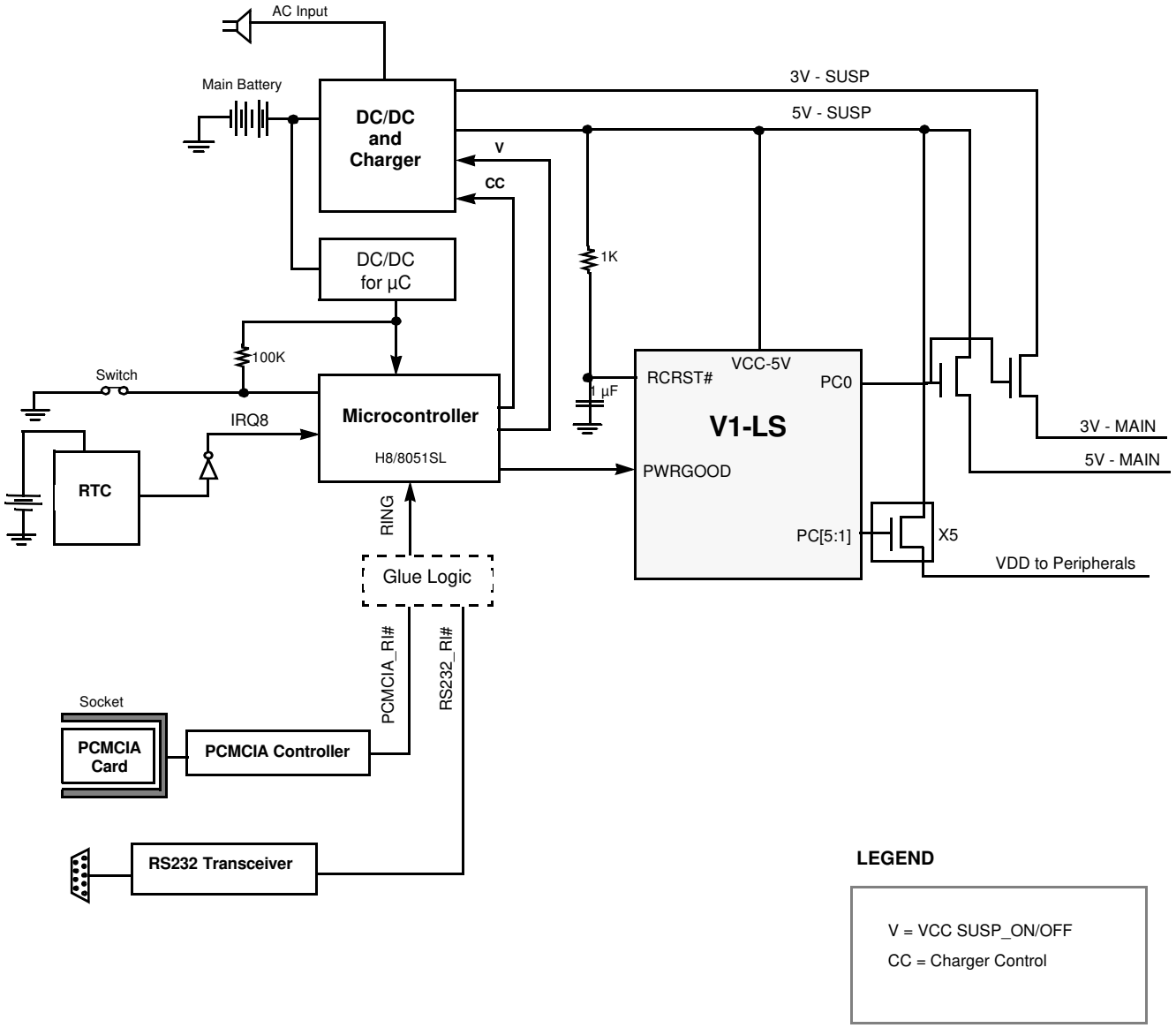


Figure 3-2. A Typical Portable Computer Design (With Zero-Volt Suspend)

3.2 Functional Blocks

The following functional blocks have been integrated into the V1-LS device. Refer to Figure 3-3 for a functional block diagram of the V1-LS device. This diagram also includes an alphabetical listing of pins in each functional group.

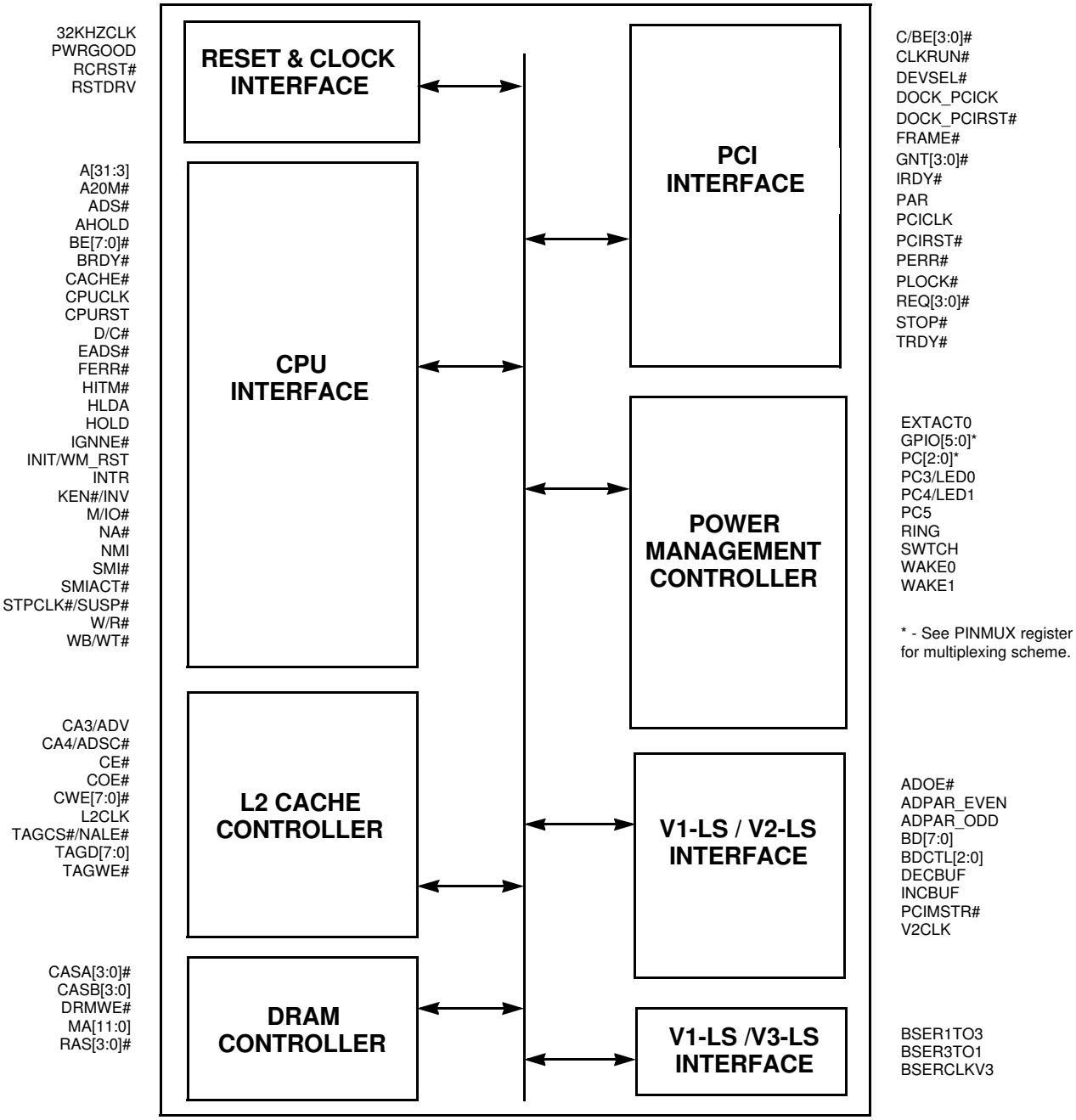


Figure 3-3. V1-LS Functional Block Diagram

3.2.1 Clock Interface

Refer to Figure 3-4 for a distribution of clocks in the V1-LS device. The CLKIN signal, an input to the V1-LS, is the clock source for the CPU/L2/DRAM/PCI subsystem. Since the CLKIN signal is a part of the VCC-5V plane, the PMC and power control interface voltage has a direct correlation with the choice of clock synthesizer or oscillator. Since the system logic of V1-LS and V2-LS uses both the rising and falling edges of the clock (derived from CLKIN), it is important to keep the CLKIN as close as possible to the 50/50 duty cycle. Therefore, CLKIN should use CMOS-level input with the threshold at VCC-5V and the synthesizer should generate an output with a worst case of 45/55 to 55/45 duty cycle, CMOS-level clock output.

The V1-LS also requires a 32-KHz input which is typically referred to as the power management clock. The 32KHZCLK is used as a debouncing clock for power management input signals like SWTCH, WAKE [1:0], EXTACT0, and RING. It is also used as a DRAM refresh clock source and as power management timers clock sources for Device Timers [5:0], Doze/Sleep/Suspend mode timers etc. Note that, the 32KHZCLK is usually connected to various devices like PCI VGA and RTC that can be independently powered on or off. Consequently, leakage could result if the 32KHz clock is not properly isolated between these devices. Since the 32KHz clock is used for power management functions, it also belongs to the VCC-5V plane and is typically set at 5-V.

Derived from CLKIN, the CPUCLK, L2CLK, and V2CLK are synchronous signals that are running at the same frequency. These signals can be stopped or restarted under certain conditions. The CPUCLK can be stopped in the Sleep, MoreStop, or Deep-Sleep mode and restarted when a primary activity (P/A) is detected. The L2CLK will stop when L2 is idle or when STPCLK# is asserted and there is no PCI Master cycle (snooping). All three clocks belong to the VCCCPU plane to minimize any potential clock skew which may otherwise result from the differences in the voltage of output buffers.

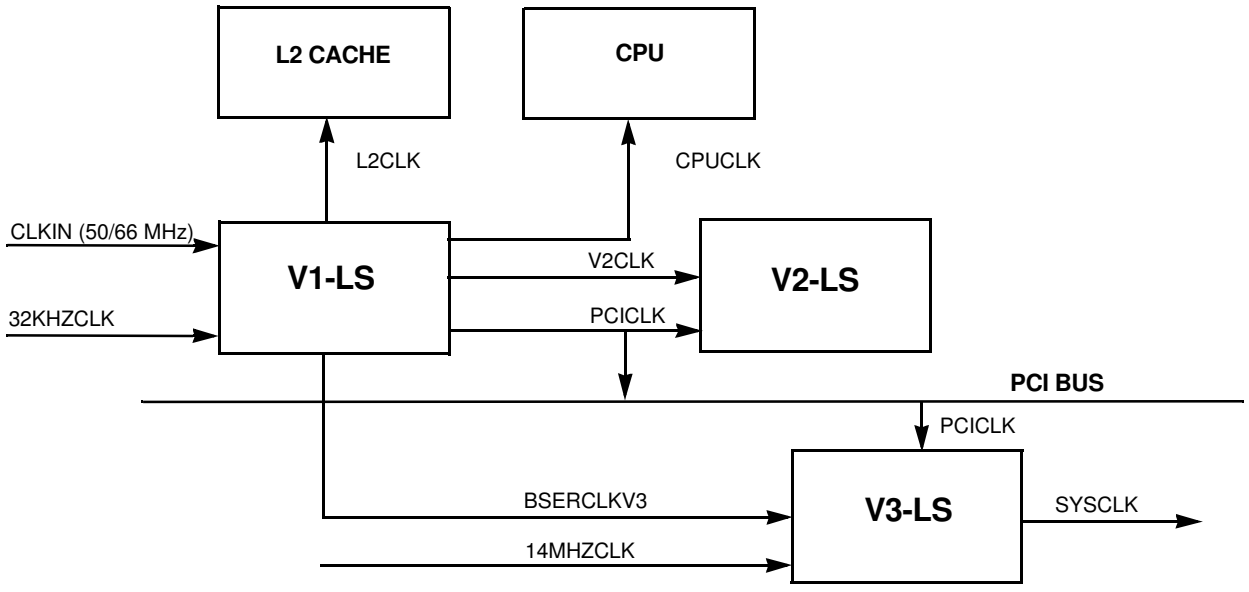


Figure 3-4. VESUVIUS-LS Clock Distribution

To ensure short rise and fall time, all three clocks use 24-mA output drivers. When laying out the printed circuit board, care must be taken to balance the trace length and loading to minimize the clock skew and clock distortion.

The PCICLK is also derived from CLKIN and runs at half the frequency of the CPUCLK. Therefore, both CPU/L2 and PCI subsystems are also running synchronously. The PCICLK belongs to the VCCPCI plane and is programmable as 3.3-V or 5-V. Clock buffering can be added if the buffer chip has a worst-case delay of 2 ns and a maximum difference of 0.5 ns among all buffered outputs. The VESUVIUS-LS also offers a proprietary PCI power management feature: If PCI idle cycles are detected for a predefined period of time, the PCICLK will be scaled (up to divided by 256) and substantially reduce the power of an idle PCI bus.

The BSERCLKV3 is the clock for BSER1TO3 and BSER3TO1 operation. The BSER3TO1 is a serialized signalling pin from V3-LS to V1-LS, indicating activities detected in V3-LS. The activities include, SMI events, P/A, secondary activities (S/A) resulting from IRQx, and V3-LS REQ#. The BSER1TO3 carries other system information from V1-LS to V3-LS, including V3-LS GNT# and IRQ13. The IRQ13 signal is also embedded because the coprocessor interface is located in V1-LS while the 8259s are located in V3-LS. All three burst signalling pins belong to the VCC-5V plane and are typically 5-V interface. In the Fully-On, Doze and Sleep mode, BSERCLKV3 will be running at the same frequency as the PCICLK to ensure minimal latency on SMI and IRQ events. However, during the Deep-Sleep mode, all clock sources (except 32KHz) are powered off and BSERCLKV3 will also stop. V3-LS will trigger V1-LS to restart the clock with a special protocol on the GPIO2 signal.

3.2.2 Reset Interface

The V1-LS device has two separate reset inputs: RCRST# and PWRGOOD. The RCRST# is the master reset of V1-LS and will reset all registers in V1-LS, V2-LS and V3-LS devices. Figure 3-5 illustrates the distribution of reset signals on VESUVIUS-LS. In a typical notebook design, the RCRST# signal should be connected to a resistor pulled up to the VCC-5V plane and a capacitor connected to ground. The time constant should be between 50 ms and 150 ms (typical value is 22 K to 68 K and 2.2 µF). If the system requires a hardware reset input, the RCRST# signal should be used.

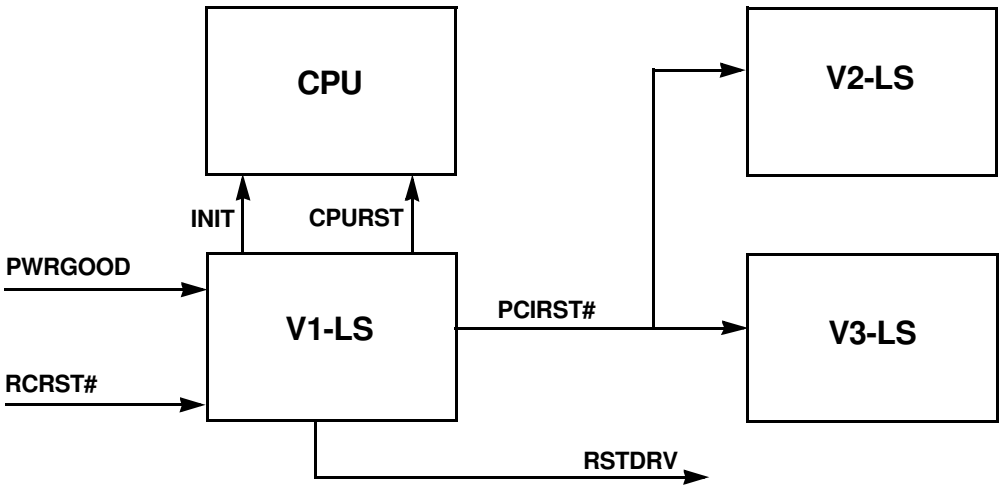


Figure 3-5. Distribution of Reset Signals

The PWRGOOD signal indicates that at least the VCC CORE and VCC-5V planes to V1-LS are powered on and in a stable condition. A low state on the PWRGOOD while the RCRST# is high and vice-versa, will trigger a reset pulse on CPURST, PCIRST#, and RSTDRV signals with a minimum pulse-width of 128 ms. For PC/AT compatibility, it is recommended that on power up, PWRGOOD should be asserted within 150 ms to 500 ms after all VCC planes have reached their regulation range. Depending on the power supply and DC/DC converter design, it may need some R, C time constant to delay the assertion of the PWRGOOD signal.

The INIT/WM_RST signal is generated under the following circumstances:

- A CPU shutdown special cycle is detected
- Keyboard reset command is written to Port 64H
- Fast reset command is written to Port 92H

3.2.3 Power-On Configuration

The VESUVIUS-LS platform incorporates a V1_POC register (V1 Power-On Register) to define any fundamental system configuration variables that must be set by hardware options. Bit [2:0] are defined as miscellaneous configuration bits (MISC_CFG [2:0]) that may be used in conjunction with the BIOS to control system variables or to detect system configurations (e.g. CPU type, CPUCLK clock speed, SRAM type, etc.) and are design-specific. Bit [5:3] are defined as Clock Skew Adjust [2:0] control bits. These bits allow the fine-tuning of internal-to-external clock skew to compensate for clock skews introduced by system design.

Register V1_POC is loaded by sampling the present value of MA[11:0] on RCRST# rising edge. In order to select the desired options for a particular system, each MA[11:0] pin should have either a pull-up or pull-down resistor connected. From the point of powering up the VESUVIUS-LS until the RCRST# rising edge, all MA lines will be tristated, therefore a weak pull-up or pull-down can easily set each MA pin to the intended high or low value. 100-K resistors are recommended. Once set, this register becomes read-only and will be sampled again only on the next RCRST# rising edge.

NOTE: Every MA pin must have either a pull-up or pull-down resistor. Any unused or reserved MA pins should be pulled-up or down according to the suggested default shown in the V1_POC register description. Since bit [11:6] are reserved, MA[11:6] should be pulled-down by 100-K resistors. Any unused MISC_CFG [2:0] should also be pulled down by a 100-K resistor.

3.2.4 CPU Interface

The VESUVIUS-LS fully supports Pentium®, K5 and 6x86 processors. It incorporates high-performance features including full pipelining support, eight-level deep write-buffers for both DRAM and PCI cycles, and read reordering on DRAM and PCI cycles.

3.2.4.1 Pentium Processor Toggle Burst Sequence and AMD/Cyrix Linear Burst Sequence

The VESUVIUS-LS supports both toggle burst sequence (Pentium processor) and linear burst sequence (K5 and 6x86 processors). This allows maximum performance for each processor in its corresponding operating frequency. The burst sequence is programmable by Register PROC bit 3, LINEARBURST.

3.2.4.2 Full CPU Address Pipelining Support (NA#)

The VESUVIUS-LS provides full address pipelining support. The pipelining option is programmable by Register PROC bit 2, PIPELINEEN.

If asynchronous data SRAM is used for L2, an external 16-bit address latch is required to latch the CPU address. Refer to Figure 3-6, and Figure 3-9 for more details.

Table 3-2. Toggle and Linear Burst Sequence

Burst Cycle First Address A[4:3]	Pentium Toggle Burst Sequence A[4:3]	K5 or 6x86 Linear Burst Sequence A[4:3]
00	00-01-10-11	00-01-10-11
01	01-00-11-10	01-10-11-00
10	10-11-00-01	10-11-00-01
11	11-10-01-00	11-00-01-10

3.2.4.3 High-Performance Eight-level Deep Write-Buffers With Read Reordering Support

The VESUVIUS-LS supports eight-level memory write-buffers. The write-buffers support (2-1-1-1) burst writes for CPU-to-DRAM and zero wait state CPU-to-PCI cycle at bus frequencies up to 66 MHz, vastly enhancing L2 write-miss and CPU-to-PCI performance. Since the write-buffers are deep enough to hold two back-to-back burst-write cycles, most L2 write-miss cycles complete in (2-1-1-1). Multiple CPU burst writes occurring in a short period of time are unlikely in a system with level-1 write-back CPU.

The VESUVIUS-LS also supports read reordering. Read reordering ensures that the CPU will not unnecessarily wait for the write-buffer to flush its content to the DRAM or PCI bus, resulting in loss of performance. In the VESUVIUS-LS platform, memory-reads (while the write-buffer is not empty) take priority and can interrupt the buffer dump to process the memory-read first. However, read reordering does not occur if the address read is still outstanding within the write buffer.

3.2.4.4 Cacheable Regions

The VESUVIUS-LS allows caching system memory which is directly controlled by the V1-LS DRAM controller into level-1 and level-2 cache. The DRAM banks and sizes programmed into the DRAM control registers imply the Top-of-Memory.

NOTE: For Revision AA and earlier revisions of VESUVIUS-LS silicon, the cacheability for L1 was limited by the memory size of the L2 cache. This limitation has been removed for silicon revision BB and beyond. By default, all memory accesses directed to on-board memory are cacheable by L1 cache.

The memory will be non-cacheable in the L1 cache:

- If the address is not within the local DRAM area: 00000000H to Top-Of-Memory.
- If the address is within one of the four programmable regions, PR [3:0], which is marked non-cacheable.
- If Register PROC bit 0, KENEN, is set to '0'.
- If during SMM, the address is within SMRAM and Register SMMC bit 1, KDISSMMRAM is set to '1.' The SMRAM address is programmable in 32-Kbyte granularity from 000D0000H-000EFFFFH by Register SMMC bit [11:4].

The VESUVIUS-LS system controller will always mark the lowest 4-Kbyte (00000000H-00000FFFH) region as non-cacheable for future proprietary features. Therefore, the lowest 64-Kbyte segment should not be used for L2 cache initialization.

The memory will be non-cacheable in the L2 cache:

- If the address is not within the local DRAM area: 00000000H to Top-Of-Memory.
- If the address is within one of the four programmable regions, PR [3:0], which is marked non-cacheable.
- If Register PROC (index 119H) bit 0, KENEN, is set to '0'.
- If any SMRAM within 000D0000H-000EFFFFH will not be cached in L2. During SMM, and if the address is within SMRAM, L2 will not respond to the cycle if it is L2 read-hit or miss. However, any write to L2 will be invalidated.
- If Register L2C (index 400H) bit 0, L2EN is set to '0'.

The memory address will be marked as write-through in L1 cache:

- If the address is within one of the four programmable regions, PR [3:0], which is marked write-through.
- If Register PROC bit 1, WTALWAYS# is set to '0'.
- If during SMM mode, i.e. SMIACT# is set to '0'.
- If the address is in the shadowed ROM range 000C0000H-000FFFFFH.

3.2.4.5 Special Programmable Regions

To allow greater system flexibility, the VESUVIUS-LS has four programmable regions: Register PR [3:0], that can be individually programmed as non-cacheable or treated as L1 write-through. The mode of each region is programmable in Register PRC. In a typical system configuration, these regions are not required since standard non-cacheable regions — non-shadowed ROM regions between 000C0000H-000FFFFFH — are automatically non-cached. The region sizes are programmable to 32 Kbytes, 64 Kbytes, 128 Kbytes, 256 Kbytes, 512 Kbytes, or 1 Mbyte.

3.2.4.6 Invalidate Write-Protected, Shadowed ROM Region in L1 Cache

When there is a write to a write-protected, shadowed ROM region (Register SHADWC, LMEMWRENn bit is set to '0') which has been cached in L1, that particular cache line must be invalidated in L1. To preserve coherency, the cached ROM region must be marked as write-through in L1 so that any write to it will become a CPU write cycle on the CPU bus. The VESUVIUS-LS will then invalidate the cached ROM line by asserting AHOLD (the VESUVIUS-LS drives out the same address) and then EADS# to the CPU.

To ensure L2 cache coherency, the L2 cache controller will not respond to any write to a write-protected, shadowed ROM region. For flash updating or flash disk operation, the corresponding LMEMWRENn bits in Register SHADWC should be set to '1' to enable a write to that region.

Snoop Filtering to Increase PCI Master Performance With L1 Cache

The VESUVIUS-LS provides a snoop filter (also known as snoop-line comparator) to compare the current memory address with the previous memory address, which will increase performance on PCI Master (V3-LS is also treated as PCI Master since it will generate REQ# for DMA/ISA Master cycle) operation with L1 cache. If the current memory address is in the same line as the previous one, snooping will be disabled and the DRAM cycle can be started earlier. Snooping is done only if the address is in the cacheable region.

3.2.4.7 STPCLK# and SUSP#/SUSPA# Support

The VESUVIUS-LS supports both Pentium/K5-style STPCLK# protocol and 6x86-style SUSP#/SUSPA# protocol. While operating in the STPCLK# protocol, the VESUVIUS-LS will look for the Stop Grant Bus Cycle (SGBC) to determine when the CPU has entered Stop Grant or Stop Clock state and decide

whether to keep the CPUCLK running or stop it to enter Stop Clock state. While operating in SUSP#/SUSPA# protocol, the VESUVIUS-LS will wait for SUSPA# from 6x86 to indicate that the CPU has entered a low-power state and the CPUCLK can then be kept running or stopped.

Since STPCLK# and SUSP# perform the same function, they share the same pin and do not require any multiplexing control. SUSPA# is multiplexed with GPIO1/LED1 pin functions and is selected by setting Register PINMUX bit [2:1] to '10'.

3.2.4.8 System Memory Map

Table 3-3. System Memory Map

Address Space	Address Range	Remarks
System DRAM	0 Mbyte – Top-of-Memory (max. 256 Mbyte)	
PCI Memory Space	Top-of-Memory – 256 Mbyte	
PCI Memory Space	256 – 479 Mbyte	10000000H – 1DF00000H
SMBASE	000D0000H–000EFFFFH (below 1 Mbyte)	See section on SMM
Upper ROM	(4 Gbytes – 32 Mbytes) to 4 Gbytes	

3.2.4.9 CPU Special Cycle

The V1-LS will always generate BRDY# to the processor when a special cycle is generated. However, for Shutdown and Halt special cycles, the V1-LS will broadcast these special cycles to the PCI bus and then generate a master-abort cycle to terminate the cycle.

3.2.5 Cache Controller

The V1-LS has an integrated L2 cache controller. It supports a direct-mapped, write-through scheme and can use 3.3-V asynchronous, synchronous burst or pipelined burst SRAM. Since V1-LS has an eight-level deep write-buffer, most L2 write-miss cycles will be completed in (2-1-1-1) up to 66 MHz, which provides the advantage of L2 write-back cache without the read-miss Dirty (castout) penalty. For systems that can only provide (3-1-1-1) L2 read-hit or write-hit at 60- or 66-Mhz with synchronous burst SRAM, the write-buffers will easily outperform them as long as the write-buffers are not full.

The L2 cache controller fully supports both non-pipelined and pipelined operations. For the pipelined mode, however, an external 16-bit latch is required when using asynchronous SRAM to latch the CPU address bus by NALE# signal from the V1-LS. Note that NALE# is multiplexed with TAGCS# signal.

3.2.5.1 L2 Cache Configurations

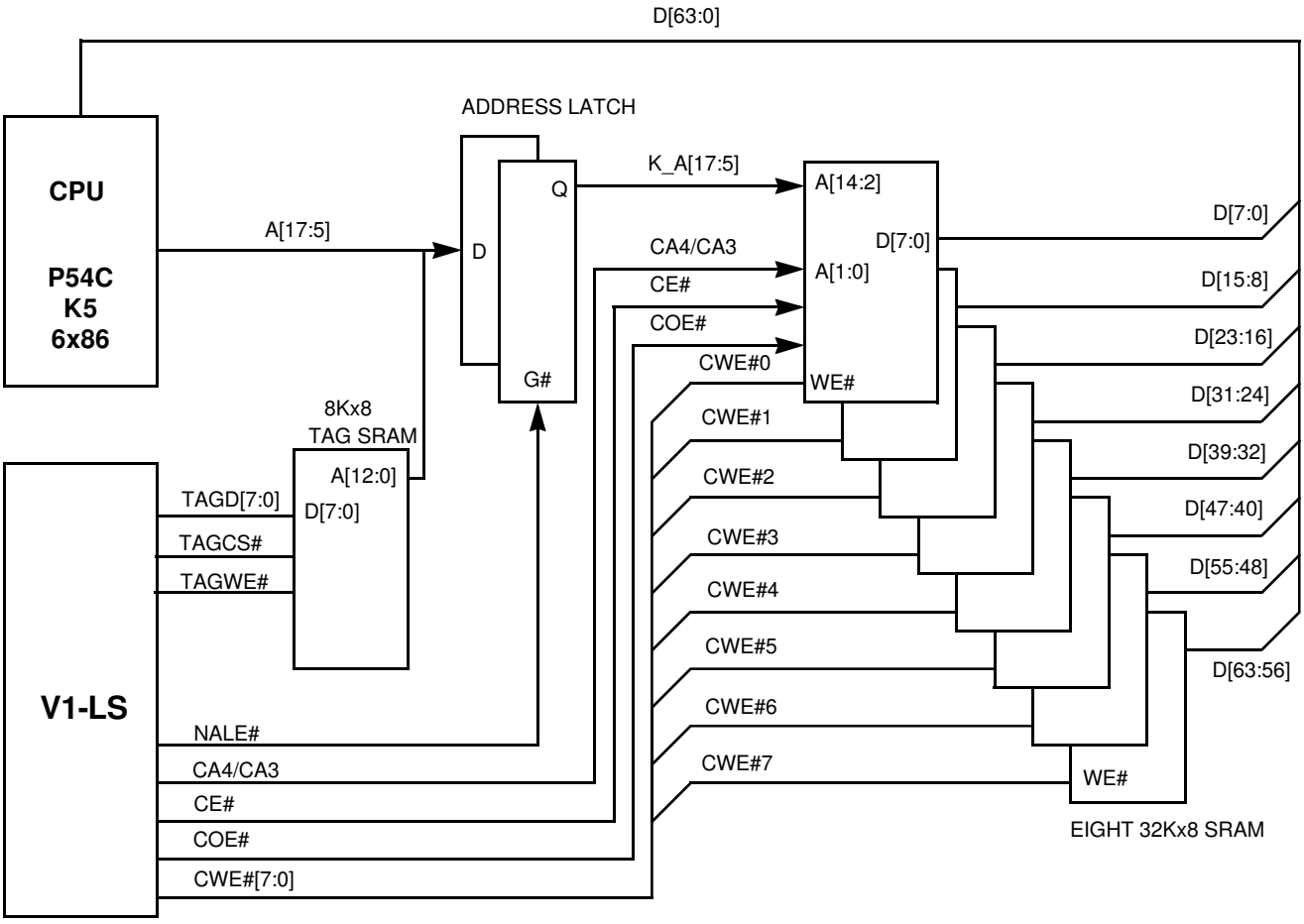
The VESUVIUS-LS supports both asynchronous and synchronous SRAM from 256 Kbyte, 512 Kbyte to 1 MByte size with 32-byte line size. All configurations are single-bank — with the exception of 512 Kbytes configuration — using two banks of 32 K x 36 synchronous SRAM (synchronous burst or pipelined burst). Refer to Table 3-4 for the cache configurations supported by V1-LS.

Table 3-4. Cache Configurations Supported

SRAM Size	SRAM Type[1]	# of Chips A-Bus Loading	D-Bus Loading	Address Latch Required for Pipeline	L2CLK Loading	L2 Cache Size	Figure
32K x 8	Async.	9	1	Yes	N.A.	256 Kbytes	Figure 3-6
32K x 16	Async.	5	1	Yes	N.A.	256 Kbytes	
32K x 36	Sync.	3	1	No	2	256 Kbytes	Figure 3-7
64K x 18	Sync.	5	1	No	4	512 Kbytes	
32K x 36	Sync.	5	2	No	4	512 Kbytes	Figure 3-8
128K x 8	Async.	9	1	Yes	N.A.	1 Mbyte	Figure 3-9

1 Sync. implies either synchronous burst or pipelined burst SRAM.

Note that for a robust system operation, there should be no more than two loads on CPU D-Bus data and five loads on CPU A-bus from the TAG SRAM and Data SRAM. If there are more than five address loads, an external buffer or latch will be required.



NOTE: TAGCS# and NALE# are multiplexed on a single pin. If NALE# function is used with asynchronous SRAM, the CS# of TAG SRAM should be connected to ground.

Figure 3-6. 256 Kbyte L2 Cache Using Eight 32 X 8 Asynchronous SRAM

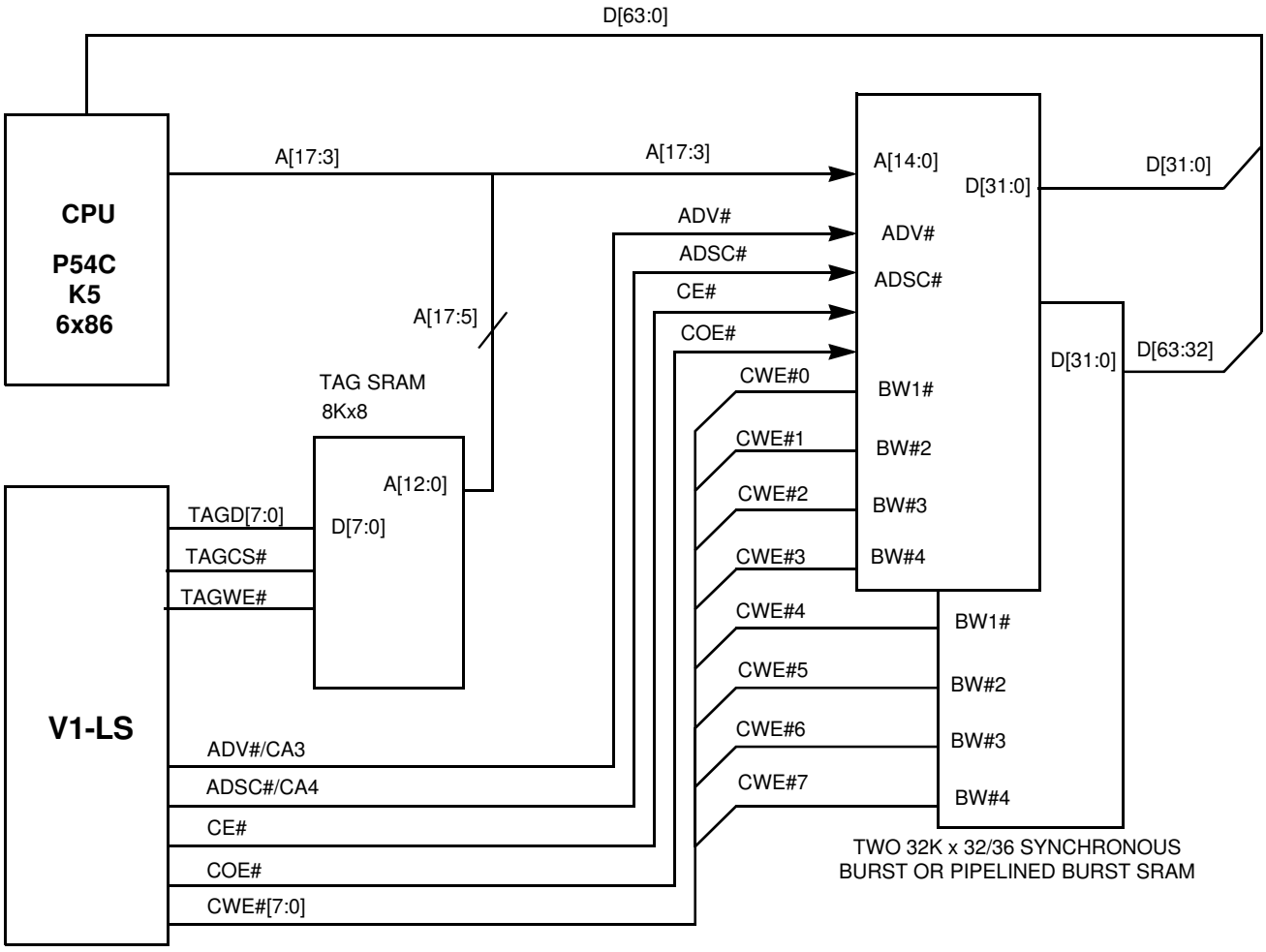


Figure 3-7. 256 Kbyte L2 Cache Using Two 32K X 32/36 Synchronous or Pipelined Burst SRAM

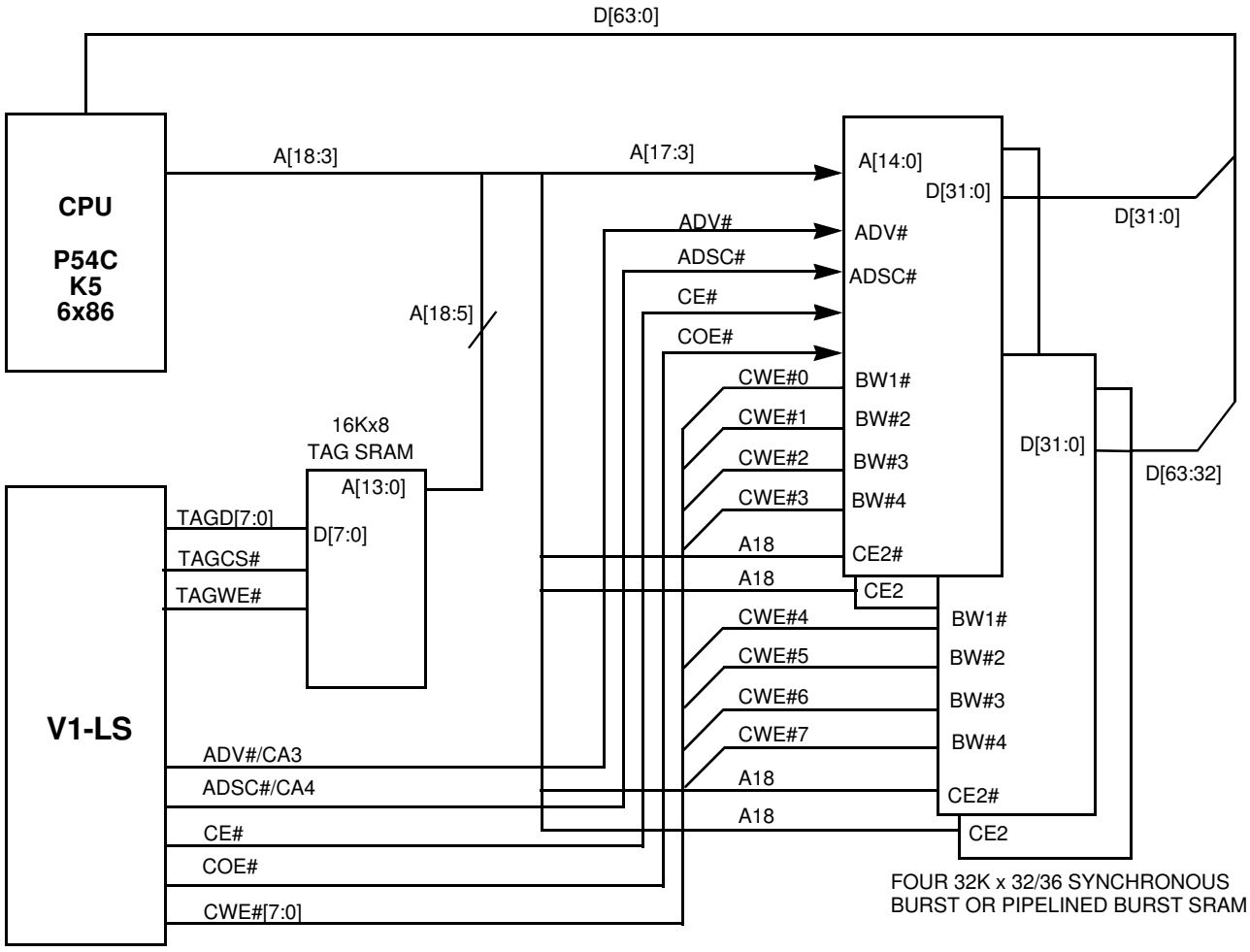
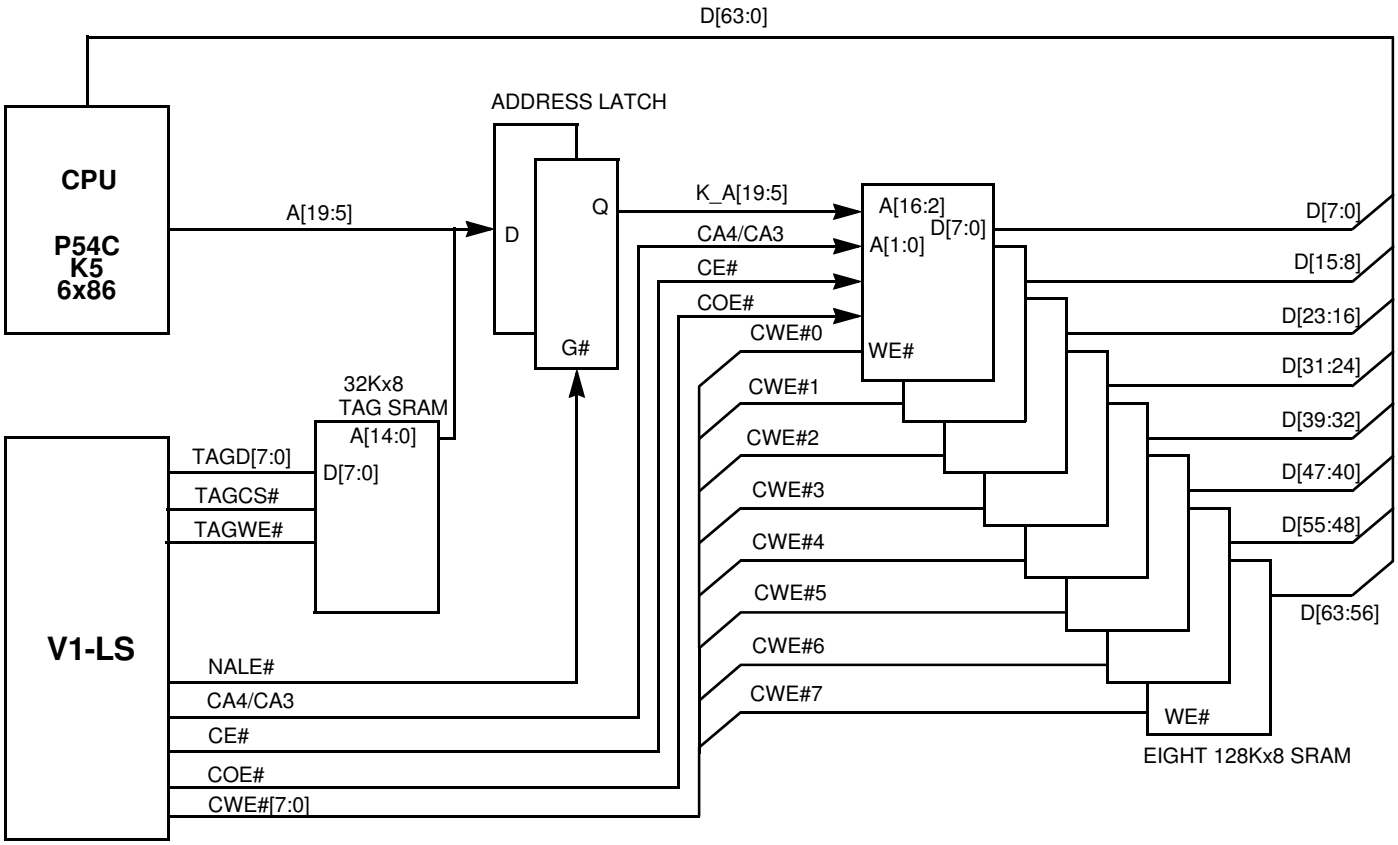


Figure 3-8. 512 Kbyte L2 Cache Using Four 32K X 32/36 Synchronous or Pipelined Burst SRAM



NOTE: TAGCS# and NALE# are multiplexed on a single pin. If NALE# function is used with asynchronous SRAM, the CS# of TAG SRAM should be connected to ground.

Figure 3-9. 1 Mbyte L2 Cache Using Eight 128K x 8 Asynchronous SRAM

3.2.5.2 TAG SRAM Size and Maximum Cacheable Region

The V1-LS has a a built-in TAG comparator which enables system designers to use low-cost Data SRAM as TAG RAM. This scheme enables 2-1-1-1 burst read or write up to 50 MHz. At 60- or 66-Mhz, 3-1-1-1 are supported.

Table 3-5. TAG SRAM Size and Maximum Cacheable Region

TAG RAM Size	L2 Cache Size	TAG SRAM Address Bus	TAG SRAM Data Bus	Maximum Cache-able Memory
8K x 8 or 32K x 8	256 Kbyte	A[17:5]	A[25:18]	64 Mbytes
16K x 8 or 32K x 8	512 Kbyte	A[18:5]	A[26:19]	128 Mbytes
32K x 8	1 Mbyte	A[19:5]	A[27:20]	256 Mbytes

3.2.5.3 TAG SRAM Speed Requirements and Hit/Miss Detection

Table 3-6 shows the TAG SRAM speed requirement for 2-x-x-x and 3-x-x-x burst cycles. It also shows the corresponding hit/miss detection point inside the VESUVIUS-LS to determine whether it is a L2 cache hit or miss cycle. The table is applicable to systems using either synchronous or asynchronous L2 data SRAM.

Table 3-6. TAG SRAM Speed Requirement and Hit/Miss Detection

Burst Performance (Lead Off Cycle)	Hit/Miss Detection Point	t_{AA} 50 MHz	t_{AA} 60 MHz	t_{AA} 66 MHz
(2-x-x-x)	t_{AA} + 9 ns	12 ns	5 ns	4 ns
(3-x-x-x)	t_{AA} + 9 ns	30 ns	15 ns	15 ns
(4-x-x-x)	t_{AA} + 9 ns	45 ns	30 ns	30 ns

3.2.5.4 Asynchronous Data SRAM Speed Requirements

Refer to Table 3-7 for the speed requirements of asynchronous data SRAM.

Table 3-7. Asynchronous Data SRAM Speed Requirement

Burst Performance	Timing Parameter	50 MHz	60 MHz	66 MHz
(3-2-2-2)	t_{AA} = Address access time	25 ns	15 ns	15 ns
	t_{OE} = OE# access time	8 ns	7 ns	7 ns
	t_{WP} = WE# pulse width	15 ns	12 ns	12 ns

NOTE: t_{AA} = TAG SRAM address access Time

3.2.5.5 Synchronous Burst Data SRAM Speed Requirements

Refer to Table 3-8 for the speed requirements of synchronous burst Data SRAM.

Table 3-8. Synchronous Burst Data SRAM Speed Requirements

Burst Performance	Timing Parameter	50 MHz	60 MHz	66 MHz
(x- 1-1-1)	t_{KQ} = Clock to output valid	10 ns	8 ns	7 ns
	t_{KC} = Clock cycle time	20 ns	16.7 ns	15 ns

3.2.5.6 Pipelined Burst Data SRAM Speed Requirement

Refer to Table 3-9 for the speed requirements of pipelined burst data SRAM.

Table 3-9. Pipelined Burst Data SRAM Speed Requirements

Burst Performance	Timing Parameter	50 MHz	60 MHz	66 MHz
(x- 1-1-1)	t_{KQ} = Clock to output valid	10 ns	8 ns	7 ns
	t_{KC} = Clock cycle time	20 ns	16.7 ns	15 ns

Pipelined SRAM supports zero wait-state writes (2-1-1-1). Thus the TAG speed must comply with this parameter.

3.2.5.7 TAGD[7:0] Mapping to CPU Address

Refer to Table 3-10 for the mapping of TAGD[7:0] to the CPU address. This information, though not required for typical system design, is provided for system debugging purposes.

Table 3-10. TAGD[7:0] Mapping to CPU Address

L2 Size	TAGD7	TAGD6	TAGD5	TAGD4	TAGD3	TAGD2	TAGD1	TAGD0
256 Kbytes	A25	A24	A23	A22	A21	A20	A19	A18
512 Kbytes	A26	A25	A24	A23	A22	A21	A20	A19
1 Mbyte	A27	A26	A25	A24	A23	A22	A21	A20

3.2.5.8 Invalidate or Write-Protect ROM Shadowed Region in L2 Cache

To ensure L2 cache coherency, the L2 cache controller will not:

- respond to any write to write-protected, shadowed ROM region.
- generate L2 cache hit cycle for reading shadowed ROM region by a non-CPU master .

In the above situations, the L2 cache controller will invalidate the cache line in L2.

For flash updating or flash disk operation, the corresponding LMEMWRENn bits in Register SHADWC should be set to ‘1’ to enable a write to that region.

3.2.5.9 L2 Cache Coherency With SMM

While in SMM, the L2 cache controller will monitor the SMIACT# pin and disable normal L2 activity. All read cycles from the CPU, while in SMM, will be marked write-through and will be fetched from the DRAM. All write cycles from the CPU will be passed to the DRAM and the corresponding index (for example, as defined by A[17:5]) to the TAG will be invalidated. Note that read misses will NOT be updated in the L2 during SMM.

3.2.5.10 L2 Cache Timing Options

To optimize system performance with specific SRAM speed grade, the cache read and write timings may be different. Thus, VESUVIUS-LS provides two independent sets of programmable timing options for read and write cycles. The read/write lead-off cycle timing is programmable to 2, 3, or 4 clocks. The read/write follow-on (subsequent burst) cycle timing is programmable to 1, 2, or 3 clocks. For details, refer to Register L2T.

Note that if Register PROC bit 2, PIPELINEEN is set to '1', the lead-off becomes follow-through time on a back-to-back L2 read or write hit cycle. Example: 4-2-2-2 back-to-back burst-read will become 2-2-2-2.

3.2.5.11 L1, L2, DRAM Cache Coherency Policy on CPU and PCI Master Cycles

Refer to Table 3-11 and Table 3-12 for more information.

Table 3-11. CPU-Initiated Cycles to Non-SMRAM Region

CPU Read/Write Cycle	L2 Hit/Miss	Description
Read	Miss	Read data from DRAM and write it to L2 cache
Read	Hit	Read data from L2 cache
Write	Miss	Write data to DRAM
Write	Hit	Write data to DRAM and L2 cache

Table 3-12. PCI Master Cycles

PCI Master Cycles	L1 Cache Line	L2 Cache Line	L1 Cache Operation	L2 Cache Operation	DRAM Operations
Read	Hit, Clean	Miss	Invalidate		PCI Master read from DRAM
Read	Hit, Clean	Hit	Invalidate	Invalidate	PCI Master read from DRAM
Read	Hit, Dirty	Miss	Castout, Invalidate		PCI Master read from DRAM
Read	Hit, Dirty	Hit	Castout, Invalidate	Invalidate	PCI Master read from DRAM
Read	Miss	Miss			PCI Master read from DRAM
Read	Miss	Hit		Invalidate	PCI Master read from DRAM
Write	Hit, Clean	Miss	Invalidate		PCI Master write data to DRAM
Write	Hit, Clean	Hit	Invalidate	Invalidate	PCI Master write data to DRAM
Write	Hit, Dirty	Miss	Castout, Invalidate		PCI Master write data to DRAM

Table 3-12. PCI Master Cycles *(cont.)*

PCI Master Cycles	L1 Cache Line	L2 Cache Line	L1 Cache Operation	L2 Cache Operation	DRAM Operations
Write	Hit, Dirty	Hit	Castout, Invalidate	Invalidate	PCI Master write data to DRAM
Write	Miss	Miss			PCI Master write data to DRAM
Write	Miss	Hit		Invalidate	PCI Master write data to DRAM

3.2.5.12 L2 Cache Auto-Sizing Procedure

Refer to Appendix C. for an example pseudo-code sequence of an algorithm for auto-sizing the L2 cache.

3.2.5.13 Power Management for L2 Cache

L2CLK will be stopped on all bus idle cycles.

For TAG SRAM, the TAGCS# will be deasserted in the following instances to save power, regardless of whether the data SRAM is synchronous or asynchronous:

- During non-L2 CPU memory cycles
- STPCLK# asserted while HOLD not asserted
- Deep-Sleep mode

3.2.6 DRAM Controller

The V1-LS incorporates a flexible DRAM controller that supports up to four 64-bit DRAM banks or eight 32-bit banks. Each 64-bit DRAM bank can be split into two 32-bit banks for finer granularity system upgrade, allowing memory expansion through a standard JEDEC 88-pin 32-bit DRAM memory card.

Additionally, the DRAM controller supports mixed 64- and 32-bit DRAM operation, thus providing unsurpassed flexibility to support virtually all possible DRAM configurations:

- 4 x 64-bit banks
- 3 x 64-bit banks and 2 x 32-bit banks
- 2 x 64-bit banks and 4 x 32-bit banks
- 1 x 64-bit bank and 6 x 32-bit banks
- 8 x 32-bit banks

Refer to Figure 3-10 for a typical 32-bit/64-bit DRAM configuration in the VESUVIUS-LS. RAS[3:0]# are connected to RAS# of the corresponding 64-bit bank, or 32-bit bank pair. In a 64-bit bank operation, CASA[3:0]# should be connected to the CAS[3:0]# (which corresponds to MD[31:0]) while CASB[3:0]# to CAS[7:4]# (corresponds to MD[63:32]). In a 32-bit bank operation, CASA[3:0]# should be connected to the CAS[3:0]# of the *even* banks (banks 0, 2, 4, 6) and CASB[3:0]# to CAS[7:4]# of the *odd* banks (banks 1, 3, 5, 7).

In addition to mixed 32/64-bit, the DRAM controller also supports mixed EDO, Burst EDO, FPM DRAM, and mixed asymmetric or symmetric DRAM without any limitation.

3.2.6.1 Programming Model for 64-bit and 32-bit DRAM Bank Configuration

Register DCONF2 (index 20FH) controls how a particular DRAM bank is configured. Bit [11:8] individually controls whether Bank 0/1, Bank 2/3, Bank 4/5 and Bank 6/7 will operate as one 64-bit bank or two 32-bit banks. Bit [7:0] individually enables/disables bank 7 to 0 as 32-bit bank. However, whenever bit [11:8] are set to enable 64-bit bank operation, the corresponding bit-pair in bit [7:0] will be overridden and ignored. For example, if DCONF2 bit 8 is set to '1', then bit [1:0] will be ignored and Bank 0/1 will operate as one 64-bit bank.

Additionally, if a bank is selected as a 64-bit bank, only the information programmed into the corresponding *even* bank registers (Registers B0C, B2C, B4C or B6C) is used and the corresponding *odd* bank information (Registers B1C, B3C, B5C or B7C) will be ignored and the DRAM bank SIZE will automatically *double* the programmed value in the even bank register. For example, if DCONF2 bit 8 is set to '1', Bank 0/1 will operate as one 64-bit bank, if B0C bit [11:0] are programmed as '100' or 16 Mbyte, the 64-bit bank size will be 32 Mbyte and the DRAM type will be 4 M (deep) x 64-bit (wide).

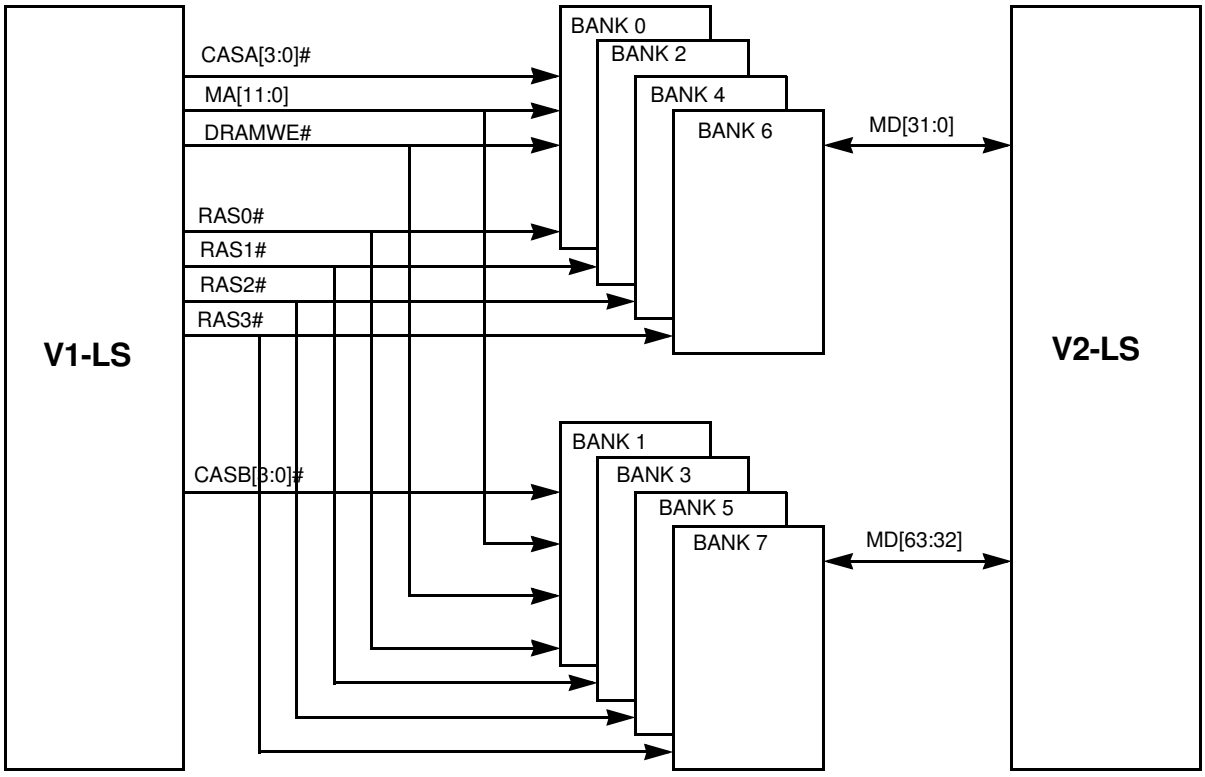


Figure 3-10. Typical 32-bit or 64-bit DRAM Configuration

3.2.6.2 Independently Programmable DRAM Timing Per 64-bit Bank or 32-bit Bank Pair

The V1-LS has a sophisticated programming model for DRAM timing control; it has an independent set of programmable DRAM timings per 64-bit bank or 32-bit bank pair (Registers B01TC, B23TC, B45TC and B67TC).

Programming the timing of a DRAM bank is an easy task; the BIOS simply needs to setup the RAS precharge time, RAS Address Hold time, CAS Address setup time, CAS precharge time, CAS Read pulse-width and CAS Write pulse-width of the DRAM used in 0.5T granularity and the DRAM controller will automatically generate optimized timing to meet the target DRAM specifications. Note, if external MA, RAS and CAS buffering is required, it should be considered when setting the timing parameters. Due to the advanced optimization of the DRAM controller to maximize system performance, the resulting waveform and burst sequence timing may not always be predictable from the programmed parameters.

3.2.6.3 Mixed FPM, EDO and Burst EDO DRAM Bank Support

The DRAM controller supports standard Fast Page Mode (FPM) DRAM, Extended Data Output (EDO) DRAM, and Burst EDO DRAM. An important use of this feature is that it allows the base system memory to use EDO to maximize performance while it can accept standard FPM memory expansion card or module, in either portable or desktop system. Register DCONF3 selects the DRAM type of each bank.

3.2.6.4 Mixed Symmetric and Asymmetric DRAM Bank Support

The DRAM controller also supports mixed symmetric and asymmetric DRAM banks with depths ranging from 256K, 512K, 1M, 2M, 4M, 8M to 16M. The MA mapping of the VESUVIUS-LS is arranged such that it will work with any available symmetric and asymmetric DRAM on the market. With the proper algorithm, the BIOS can determine the number of CAS address lines in the DRAM. The BIOS can then program the Column Address bits, or COLADRx[2:0] of the corresponding Register B0C to B7C, with the proper bank size, 32-bit/64-bit configuration information. The VESUVIUS-LS will then generate the proper MA for the DRAM cycle addressed to that particular bank. Note that symmetric and asymmetric DRAM can be mixed within the same 32-bit bank pair.

3.2.6.5 DRAM Memory Map

Refer to Table 3-13 and Table 3-14 for more information.

Table 3-13. 64-Bit DRAM Bank CPU A-Bus to MA Mapping

MA	8-bit Column Address		9-bit Column Address		10-bit Column Address		11-bit Column Address		12-bit Column Address	
	RAS	CAS	RAS	CAS	RAS	CAS	RAS	CAS	RAS	CAS
11	22	14	23	14	24	14	25	14	25	14
10	21	24	22	24	23	24	23	13	23	13
9	20	22	21	22	21	12	21	12	21	12
8	19	20	19	11	19	11	19	11	19	11
7	18	10	18	10	18	10	18	10	18	10
6	17	9	17	9	17	9	17	9	17	9
5	16	8	16	8	16	8	16	8	16	8
4	15	7	15	7	15	7	15	7	15	7
3	14	6	14	6	14	6	14	6	26	6
2	13	5	13	5	13	5	24	5	24	5
1	12	4	12	4	22	4	22	4	22	4
0	11	3	20	3	20	3	20	3	20	3

Table 3-14. 32-Bit DRAM Bank CPU A-Bus to MA Mapping

MA	8-bit Column Address		9-bit Column Address		10-bit Column Address		11-bit Column Address		12-bit Column Address	
	RAS	CAS	RAS	CAS	RAS	CAS	RAS	CAS	RAS	CAS
11	21	13	22	13	23	13	24	13	25	13
10	20	23	21	23	22	23	23	12	23	12
9	10	21	20	21	21	11	21	11	21	11
8	19	10	19	10	19	10	19	10	19	10
7	18	4	18	4	18	4	18	4	18	4
6	17	9	17	9	17	9	17	9	17	9
5	16	8	16	8	16	8	16	8	16	8
4	15	7	15	7	15	7	15	7	15	7
3	14	6	14	6	14	6	14	6	14	6
2	13	5	13	5	13	5	13	5	24	5
1	12	3	12	3	12	3	22	3	22	3
0	11	2	11	2	20	2	20	2	20	2

3.2.6.6 Shadow RAM Control

Register SHADRC controls the shadow RAM readability from 000C0000-000FFFFF in 16-Kbyte granularity while Register SHADWC controls the shadow RAM writability. The 16-Kbyte granularity supports the Plug and Play BIOS specification as recommended by various BIOS vendors. In the VESUVIUS-LS, Shadow RAM readability is tied to cacheability. It means that if Register SHADRC bit [1:0] are both set to '1', then 000C0000-000C7FFF will become a cacheable region.

3.2.6.7 Advanced DRAM Refresh Support

To support all possible DRAM types, the VESUVIUS-LS also provides versatile DRAM refresh support. Register DRFSHC controls the refresh scheme, RAS pulse-width and precharge time for refresh cycles and refresh period. The DRAM refresh clock source is based on 32KHz input clock which generates an internal refresh request once every 15 µs. However, some new DRAM require to be refreshed every 3.75 µs or 7.5 µs. If such options are selected through Register DRFSHC bit [7:5], the VESUVIUS-LS will generate a burst of 4 or 2 refreshes respectively every 15 µs.

3.2.7 System Management Mode (SMM)

The VESUVIUS-LS provides a flexible SMM interface for both software and hardware. It can generate SMI by up to 52 possible sources: external pins, power management events, timer time-out, and software-triggered events. To simplify polling of SMI events, the SMI trigger sources (and masks) are grouped. Refer to Section 3.2.9.6 on page 1-71for details on SMM as it relates to power management functions. The discussion on SMM in this section is limited to SMM as it relates to the CPU interface.

3.2.7.1 SMM Base and Remapping of SMRAM

The SMM base address in the VESUVIUS-LS is defined as 000D0000H-000EFFFFH. The physical memory space used for SMM memory is at 000A0000H-000BFFFFH in DRAM. The SMBASE and remapping options are programmable by Register SMMC bit [11:4].

It is suggested to use 000D0000H-000EFFFFH as the SMBASE and set SMRAM as non-cacheable; this not only eliminates the overhead on flushing L1 cache, it also eliminates potentially high overhead for eviction of all dirty lines on flushing L1 if it is operating in the write-back mode (even though WB/WT# pin is always low during SMIACT# low).

3.2.7.2 Relocating SMBASE and Initializing SMRAM

To simplify loading SMM handler and relocating SMBASE, the V1-LS device also supports remapping 0002000H-0003FFFFH to the SMRAM (at 000A0000H-000BFFFFH). The BIOS can set Register SMMC bit 2, EN23RMAB to '0' and set SMMC bit 14, LDSMIHLDER to '1'. It can then load the SMM handler by simply writing to 00020000H-0003FFFFH, thereby initialing the SMRAM at 000A0000H-000BFFFFH. Note that L1 and L2 cache must be disabled when remapping 2-3FFFF to A0000-BFFFF.

3.2.7.3 Other SMM Characteristics

- SMRAM accesses will always be marked as L1 WT, as specified by CPU specification.
- SMRAM will not be accessible by PCI masters. If a PCI master cycle access hit the memory range of SMRAM, V1-LS will not remap the address but will access the regular DRAM, even SMIACT# is still asserted low.

3.2.8 PCI Bus Interface and Arbiter

3.2.8.1 PCI configuration Address and Data Registers

The VESUVIUS-LS supports configuration type 1 with 64 bytes of configuration space (offset 00H-3FH). The PCI configuration address and data registers are located at the standard 0CF8H and 0CFCH respectively. Since some registers within these 64 bytes are reserved, any write to these areas is to be ignored and any read from these areas is to be returned with '0's, as recommended by *PCI Bus Specifications*.

3.2.8.2 PCI Master Arbitration Scheme

The V1-LS supports up to five PCI masters, one dedicated to the V3-LS PCI-ISA bridge, and remaining four REQ[3:0]# and GNT[3:0]# pairs for PCI masters. Since V3-LS represents ISA DMA and ISA Masters which do not support preempt mechanism, therefore, V3-LS has the highest priority in the arbitration. The VESUVIUS-LS supports rotating priority scheme for the other PCI masters since they have the same priority. Note that the arbiter will only grant to the requesting master after the write buffer has been emptied.

Since V3-LS REQ#/GNT# protocol is embedded into BSER1TO3 and BSER3TO1 protocol, there are only four pairs of REQ[3:0]# and GNT[3:0]# signals.

3.2.8.3 CPU-initiated PCI Bus Cycle Types

Refer to Table 3-15 for more information on CPU-initiated PCI bus cycles types.

Table 3-15. CPU-Initiated PCI Bus Cycle Types

M/IO#	D/C#	W/R#	CPU Bus Definition	C/BE[3:0]#	PCI Bus Definition
'0'	'0'	'0'	Interrupt Acknowledge	'0000'	Interrupt Acknowledge
'0'	'0'	'1'	Special Cycle*	'0001'	Special Cycle
'0'	'1'	'0'	I/O Read	'0010'	I/O Read
'0'	'1'	'1'	I/O Write	'0011'	I/O Write
'0'	'1'	'0'	I/O Read to CF8H or CFCH	'1010'	Configuration Write
'0'	'1'	'1'	I/O Write to CF8H or CFCH	'1011'	Configuration Write
'1'	X	'0'	Memory Read	'0110'	Memory Read
'1'	'1'	'1'	Memory Write	'0111'	Memory Write

* Only Shutdown and Halt special cycles are translated into PCI cycles; V1-LS will return BRDY# to CPU for other special cycles.

3.2.8.4 PCI interrupt Acknowledge Cycle

For PC AT compatibility, the processor will generate two INTA# cycles for each INTR assertion. The PCI interface only requires one PCI interrupt acknowledge cycle for each interrupt, thus, V1-LS will generate PCI interrupt acknowledge cycle only on the second CPU INTA# cycle.

3.2.8.5 Early AD[31:0] Assertion for PCI Configuration Access

As recommended by the*PCI Bus Specification 2.1*, during PCI configuration access, AD[31:0] (in address phrase) will be driven out one PCICLK before FRAME# is asserted. This provides enough precharge time for devices that resistively connect their IDSEL signals to the AD bus.

3.2.9 Power Management Controller (PMC)

The VESUVIUS-LS power management registers have evolved from the REDWOOD/FIR family and are engineered to be more programmer-friendly, while maintaining full flexibility and versatility. The key features of the VESUVIUS-LS PMC are:

- Advanced primary and secondary activity monitors.
- Support of Fully-On, Conserve, Doze, Sleep, Deep-Sleep and 0V-Suspend or Suspend-to-Disk modes.
- Three independently programmable power control registers for On/Doze, Sleep/Deep-Sleep and Suspend mode.
- Sophisticated CPU clock management by STPCLK# (or SUSP#/SUSPA#) throttling; independent throttler control for Conserve mode; Doze/Sleep/Deep-Sleep mode and THERM input.
- Generation of PMI from 14 different groups and up to 52 events.
- I/O trap and restart support.
- Six programmable range monitors, PRM[5:0], that can monitor any I/O or memory device on read, write or read/write accesses.

- Five external power management inputs, including SWTCH, RING, WAKE0/1, and EXTACT0. Each is independently selectable to be debounced or not, and triggers on either rising, falling or both rising and falling edges.
- Three mode (Doze, Sleep, Suspend) timers and six independent device timers .
- Device timers can be linked to any monitored device, PRM0/1 or EXTACT0 input.
- Flexible and easy-to-program BCD-encoded timer and prescalar select on all timers.
- Six GPIOs and six power control outputs.
- Two programmable LED indicator outputs.
- Effective PCI clock power management .

The VESUVIUS-LS PMC provides high flexibility and programmability to meet the system power management demands in an advanced portable system. The PMC employs both passive and active power management techniques to achieve power management in both Fully-On and power saving modes. The following discussion defines the usage of each power-saving mode and feature. It assumes that the reader is familiar with SMI# and STPCLK# operations of the CPU.

3.2.9.1 Activity Monitors

The concept of National Semiconductor's Power Management Controller deals with monitoring system activities in order to determine whether the system is idle or not. Various timers, including Doze Mode Timer (DZMT), Sleep Mode Timer (SLPMT), and Suspend Mode Timer (SPNDMT) are setup to determine the amount of time the system is idle in order to trigger mode timer time-out SMI to enter a progressively lower power state. To understand how activity monitors work, first we need to define primary and secondary activity.

3.2.9.2 Primary Activity (P/A)

A primary activity is defined as an 'important' system activity which indicates that the system is active and that the system resources are being accessed. If a primary activity is unmasked, it will trigger the activity monitor. If the system is already in either Doze, Sleep or Deep-Sleep mode, P/A brings the system back to Fully-On/Conserve mode. Also, P/A will reset all mode timers, i.e., DZMT, SLPMT and SPNDMT.

The V1-LS can monitor any of the following as primary activities. Each of these activities can be enabled/disabled by the corresponding mask bits in Register PAM1 and PAM2:

Primary Activity Mask 1 (Register PAM1)

P/A can be individually masked or triggered by accesses to VGA, primary or secondary IDE, FDD, KBC, Serial I/O 1 and 2, and parallel I/O. P/A can also be individually masked or triggered by any read, write, or both read and write accesses to PRM[5:0].

NOTE: HOLD can also be enabled as a primary activity because HOLD will represent any PCI Master, including ISA DMA or ISA Master requests, which will access system resources and requires the system to be in Fully-On / Conserve mode.

Primary Activity Mask 2 (Register PAM2)

P/A can be individually masked or triggered by a 'toggling' edge (triggered by either rising, falling or both rising and falling edges). See Register EDC, Edge Detect Control on EXTACT0, RING, SWTCH, WAKE0 or WAKE1.

Primary Activity Option Control (Register PAOC)

Any unmasked P/A can optionally be flagged in the activity flag Registers, AFR1 and AFR2. To enable flagging, Register PAOC bit 0, PAFLGEN, must be set to '1'. Registers PAM1 and PAM2 correspond — bit by bit — to AFR1 and AFR2 for easy BIOS implementation.

P/A also has an option to trigger SMI and is enabled by setting Register PAOC bit 1, SMI_MSK_PA to '0'. This is useful in SMI-driven mode change environment. Example: SMI_MSK_PA should not be masked if there is any BIOS housecleaning required when switching from Sleep mode back to Fully-On mode. Register PAOC bit 3, DISPACTVON should also be set to '1' to prevent automatic transition to On mode by hardware due to primary activity.

Register PAOC, bit 2, ENLTCH_PA_SMM, when set to '1' causes any primary activity detected within SMM to latch P/A until deassertion of SMIACT#. This primary activity will keep the timers reset and the system in On mode.

Register PAOC, bit 4, MSKSMI_PA, when set to '0' allows any unmasked SMI (except for an SMI caused by primary activity to prevent a recursive generation of SMI and P/A) to trigger primary activity. This is particularly useful when a SLPTO SMI causes a transition to Deep Sleep mode and a SPNDTO SMI is generated. Even if secondary activity is unmasked for SMI, it cannot revive clocks out of Deep Sleep mode. This bit allows SPNDTO SMI to trigger a P/A which will then cause a transition from Deep Sleep back to the Fully On mode.

Primary Activity Triggered by V3-LS (Register PAIRQM-1, PAIRQM-2 of V3-LS)

The VESUVIUS-LS platform allows any unmasked IRQs to trigger P/A. This enables 'any-key wakeup' from Deep-Sleep mode or 'Network-compliant Deep-Sleep mode', among other functions. The V3-LS Registers PAIRQM-1 and PAIRQM-2 are used to mask or unmask IRQ[15:3], IRQ1 and NMI to trigger a P/A.

P/A, S/A, SMI, and other power management information is passed through the BSER1TO3 from V1-LS to V3-LS and through BSER3TO1 from V3-LS to V1-LS. Therefore, V3-LS register PMCR (20H), bit 0 (BSEREN) must be set to'1' to enable communication between BSER1TO3 and BSER3TO1.

IMPORTANT: To trigger an SMI due to a PAIRQ, set Register PMCR bit 2, PMIPAENB to '1' in V3-LS device. This will allow the generation of both P/A and SMI due to an IRQ and the SMI source will only indicate V3-LS activity as the source (not primary activity as well). The BIOS should then reference Registers PMIIRQS-1 and PMIIRQ-2 in V3-LS device to find the particular source. Note that even if Register PAOC bit 1, SMI_MSK_PA in V1-LS is set to '0', it does not generate an SMI due to PAIRQs.

3.2.9.3 Secondary Activity (S/A)

A secondary activity or S/A is one that only requires a short service time during either Doze or Sleep modes. Refer to Figure 3-12 on page 1-69, where the system will temporarily go back to full speed (or conserve throttling speed if Conserve mode is enabled) to service the S/A while remaining in the state when S/A occurs, either Doze or Sleep mode. For example, the system should typically service IRQ0 in order to keep the system timer and to ensure any chained interrupt service routine (ISR) to IRQ0 to be serviced, e.g. scheduled faxing or tape backup. If the system doesn't require such a feature, it can mask IRQ0 from S/A. Another example: During Doze mode the 'lid-switch' toggles from open to close, triggering an SMI to power-off the LCD backlight in order to maximize battery life. Note that switching to and returning from "revive state" is not a mode change and will not trigger any PC[5:0] toggling.

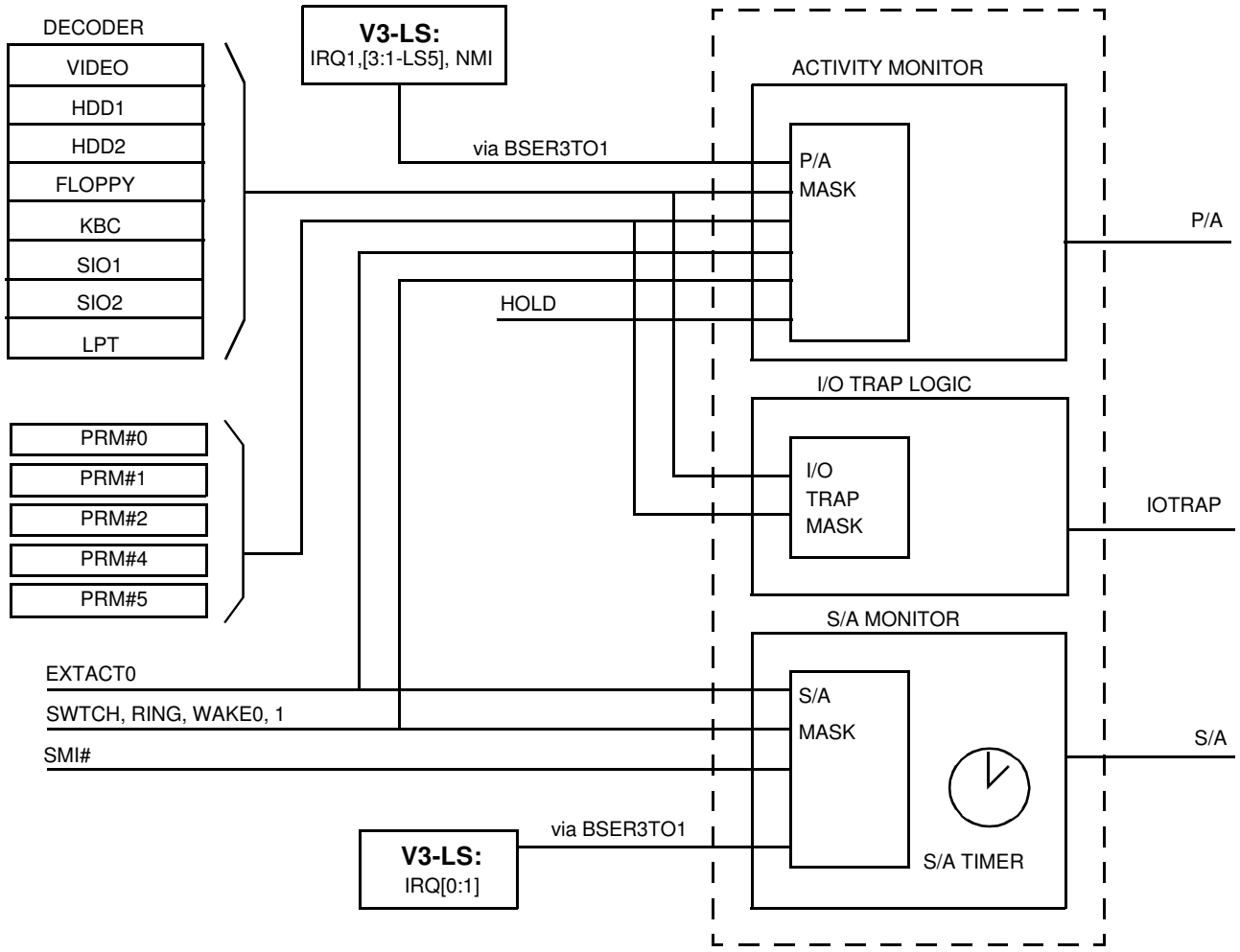


Figure 3-11. Generation of P/A, S/A, and I/O Trap

S/A cannot revive clocks from Deep Sleep mode. Since IRQ0 is not serviced, when the system wakes up from Deep-Sleep mode, a 'timing-correction' should be performed to read from RTC and update the DOS or operating system timer.

The V1-LS can monitor various secondary activities. They can be enabled/disabled by the corresponding mask bits in Register SAM :

Secondary Activity Mask (Register SAM)

S/A can be individually masked or triggered by a 'toggling' edge (triggered by either rising, falling or both rising and falling edges. See Register EDC, Edge Detect Control) on EXTACT0.

NOTE: SMI or HOLD assertion can also be unmasked to trigger S/A because SMI interrupt and PCI Master activity may only require a short period of service. This provides flexibility to different system environments. The decision to enable HOLD as P/A or S/A and SMI as S/A is system-specific and is up to the system designer.

Secondary Activity Triggered by V3-LS (Register PMCR of V3-LS)

The VESUVIUS-LS platform allows unmasked IRQ0 or IRQ1 to trigger a secondary activity. This offers a flexible option to update the system timer (IRQ0) and to service a keystroke (IRQ1) without returning to Fully-On/Conserve mode. The system designer has the choice of selecting whether a keystroke will wakeup the system (IRQ1 as P/A) or if it will only perform a screen update (IRQ1 as S/A) and wait until the key sequences to wake up the system by other P/A. Example `DIR C:<CR>` will access hard disk.

Secondary Activity Timer (Register SAT)

S/A will not reset any mode timers. However, S/A has its own timer, programmable by Register SAT. S/A timer determines the time to stay in 'revive state' before returning to either Doze or Sleep mode. The S/A timer provides a range from 100 µs to 79 ms and can be enabled or disabled. The S/A timer can be considered an 'additional time' timer.

Although typical S/A requires only a short service time, in some real-time or multitasking operating system environments, the service time may be extended due to the priority of other real-time events. The V1-LS provides various options to correctly time the S/A events.

S/A Triggered by SMI

If S/A is triggered by SMI events, SMIACT# deassertion (low-to-high edge) can be used to determine the end of the S/A event. Example: If the S/A timer is programmed to be 1 ms, the system will stay in 'revive state' until 1 ms after SMIACT# is deasserted.

For BIOS implementations that prefer to go to a power management mode which causes LessStop or MoreStop such as Sleep mode within SMM, it is recommended that Register SAT, bit 8, RST_SA_ON_SMI be used. Writing this bit high allows a one-time reset pulse to the SA on SMI latch. This terminates the secondary activity before the deassertion of SMIACT#, thus allowing STPCLK# to go low. Using this bit prevents unnecessary overhead in disabling and then enabling Register SAM, bit 0, SA_MSK_SMI.

S/A Triggered by HOLD

If a S/A is triggered by HOLD (PCI Master events), HLDA deassertion will be used to determine the end of the S/A event. Example: If the S/A timer is programmed to be 1 ms, the system will stay in 'revive state' until 1 ms after HLDA is deasserted.

S/A Triggered by IRQ0/1

If S/A is triggered by IRQ0/1, the corresponding ISR and IRR bits can be used to determine the end of S/A event. If S/A timer is programmed to be, e.g., 1 ms, the system will stay in 'revive state' until 1 ms after ISR and IRR are both cleared. Note that, since the interrupt service routine can execute EOI to clear ISR bit long before it executes IRET instruction, ISR and IRR bits can only be used as reference and S/A timer should be set to long enough time to complete the service routine, otherwise, undesirable nested interrupts may occur.

S/A Triggered by EXTACT0

If S/A is triggered by EXTACT0, the value programmed in the S/A timer will directly determine the amount of time the system will stay in 'revive state' before returning to either Doze or Sleep mode.

3.2.9.4 Power Management (PM) Modes

This section discusses the power management modes found in the VESUVIUS-LS system controller. Refer to Figure 3-12 on page 1-69 for a conceptual visualization of the VESUVIUS-LS power management modes.

Fully-On Mode

During the Fully-On mode the system is running at full-speed and all devices (except those powered-down by device timer time-out events) are powered-on.

Conserve Mode

This is a logical equivalent to the Fully-On mode. It is used in situations where prolonging the battery life is more critical than the need for full system performance. Example: running a word processing application on a portable computer during air travel. Once enabled, Conserve mode will logically replace the Fully-On mode. Register CON-CTRC enables and selects clock throttling ratio (see Section 3.2.9.5 on page 1-68 for additional details) during the Conserve mode.

Doze Mode

The first level of power conservation, this mode is typically entered when the system is idle. System idle is defined as the absence of P/A for a predefined time-out value (in range of seconds). Register DZMT selects the idle time before entering Doze mode. Register DS-CTRC is bit [4:0] enables and controls the clock throttling ratio during Doze mode. In VESUVIUS-LS, there are two ways to enter Doze mode. Each method can be selected by Register ISTM bit 6, SMI_MSK_DOZE_TO:

1) If SMI_MSK_DOZE_TO is set to '1', Doze mode can be entered automatically on DZMT time-out, without triggering SMI. This is used in situations where no PC[5:0] toggling is required. This allows entering Doze mode between keystrokes and returning to Fully-On / Conserve mode when keystroke or other P/A is detected.

2) If SMI_MSK_DOZE_TO is set to '0', then DZMT time-out will trigger a SMI. If PC[5:0] toggling is required, SMM handler should first write the new PC[5:0] state to Register ONDZ-PC, then write to Register PMM bit [2:0] to switch to Doze mode.

Note that both Fully-On and Doze modes share the same ONDZ-PC register. If Conserve mode is enabled and Doze mode is entered from Conserve, P/A will return the system to Conserve mode (or Conserve mode throttling for S/A) since it will logically replace Fully-On mode until it is disabled.

Sleep Mode

The second-level of power conservation, the Sleep mode is entered when the system is idle for a prolonged duration (defined as a range of minutes). Register SLPMT selects the idle time before entering Sleep mode. In VESUVIUS-LS, Sleep mode can be entered through SLPMT time-out SMI. Sleep mode can be entered through hardware time-out if SMI_MSK_SLPTO is set to '1. If PC[5:0] toggling is required, SMM handler should first write the new PC[5:0] state to Register SLP-PC, then write to Register PMM bit [2:0] to switch to Sleep mode.

The VESUVIUS-LS provides a high degree of programming flexibility to achieve different levels of power-savings in the Sleep mode. Also, there is a sub-mode called Deep-Sleep which provides the highest level of power-saving when compared with modes other than the Suspend mode. Refer to Table 3-16 on page 1-66 to find out about the options selected by Register DS-CTRC bit [7:5].

As shown in Figure 3-13, any unmasked S/A will temporarily put the system into 'revive state', overriding the MoreStop or LessStop and revive from Sleep mode until the S/A event or timer has expired.

Deep-Sleep Mode

This mode is entered the same way as the Sleep mode. On entering this sub-mode, STPCLK# is asserted continuously, PMC waits for Stop Grant bus cycle, stops the CPUCLK (CPU enters Stop Clock state) and then a clock-gate blocks the CLKIN from the internal logic. Register SPND_PC can be programmed to toggle PC output to either power-off or power-down CLKIN and other high speed clocks except 32 kHz (to keep the PMC running). On waking up from Deep-Sleep mode, the PC output (set high in Register ONMD_PC) will toggle to power-on CLKIN and other high speed clocks, wait for 20-30 ms stabilization time, and then the clock-gate will cleanly pass CLKIN to the internal logic. CPUCLK is then restarted, waits for the 'STPCLK Release Latency' (defined in DS-CTRC bit [10:8]), and then STPCLK# will be deasserted so that the CPU can service the P/A or SMI events. Refer to Register PAOC regarding the use of MSKSMI_PA bit to trigger a P/A due to an SMI to return to On mode from Deep Sleep mode.

Table 3-16. Register DS_CTRC bit[7:5] Selectable Options

DS-CTRC Bit [7:5]	Function
'000'	**Disable clock throttling in Sleep mode** .
'001'	**Enable clock throttling in Sleep mode:** The ratio is selected by DS-CRTC bit [2:0]
'010'	**Enable LessStop state (CPU in Stop Grant state) in Sleep mode:** STPCLK# will be asserted continuously, with CPUCLK running, until the system returns to Fully-On / Conserve mode by P/A.
'011'	**Enable MoreStop (CPU in Stop Clock state) in Sleep mode:** In this case, STPCLK# will be asserted continuously, with CPUCLK stopped, until the system returns to Fully-On / Conserve mode by P/A. DS-CTRC bit [10:8], STPCLK Release Latency, controls the time from CPUCLK restarted to STPCLK# deasserted to meet various CPU PLL stabilization specifications (1 µs to 2 ms).
'100'	**Enable Deep-Sleep mode:** Deep- Sleep mode is defined to provide a very low power state with very fast wakeup time.

If using the DISPACTVON bit (Register PAOC), make sure that it is low before entering Deep-Sleep mode; otherwise a P/A source cannot wakeup the system. The VESUVIUS-LS provides the capability to wakeup from Deep-Sleep mode by pressing any key since an IRQ is communicated through BSER3TO1 pin toggling. Any unmasked IRQs can trigger P/A to wake up from Deep-Sleep mode. Similarly, 'Network-compliance' is achieved due to the fast wakeup time possible from the network polling interrupt (around 30 ms).

As mentioned earlier, an S/A cannot revive the system out of Deep-Sleep mode. This is to maximize the power-savings since most devices are already in a static state (high frequency clock is stopped).

Suspend Mode

This mode offers the highest level of power saving. Suspend mode is activated (always through software) if the system is idle for an extended period after having entered the Sleep mode. Register SPNDMT selects the idle time before entering Suspend mode. There are two different implementations of the Suspend mode:

0V-Suspend or Suspend-to-Disk (STD)

The system and video memory, status, register dump, and shadowed register values are stored in the hard disk. A flag is setup in CMOS SRAM to indicate that a 0V-Suspend has previously occurred. Then the system (except the RTC and optionally, a microcontroller that monitors the keyboard and switch but-

ton activity) is totally shut-off. This mode does not require leakage control because all system devices, including V1-LS, are powered-off.

If the modem RING or RTC alarm IRQ8# is allowed to wake up a system in 0V-Suspend, an external microcontroller can be used to monitor the toggling of RI# from RS232 or PCMCIA and the assertion of IRQ8# since the V1-LS is powered off. The microcontroller will then resume the system by powering the DC/DC converter; the BIOS will check the CMOS SRAM flag to determine if a 0V-Suspend has occurred and perform the proper resume sequence. Refer to Figure 3-2 on page 1-39 for details.

Since the V1-LS is off, the 0V-Suspend and resume process relies on the external microcontroller. Therefore:

- Register WSS bit [10:8] will not indicate any wake source on resume from STD
- Register WMC bit [3:0] is not applicable to STD
- Register RCC bit [4:0] is not applicable to STD
- Register SPND-PC is not applicable to STD
- Register LC is not applicable to STD

5V-Suspend or Suspend-to-RAM (STR)

In this mode most devices (except V1-LS, VGA, RTC and optionally, the external microcontroller or PCMCIA controller) are powered off. Leakage control is required for all devices that are powered on during STR. V1-LS will keep the system DRAM refreshed while the VGA will keep the video memory refreshed. Register settings of devices that will be powered-off should be saved. For read-only registers, particularly for important ISA resources, the V3-LS provides an extensive set of shadow registers to enable the read-back process.

A flag is setup in CMOS SRAM to indicate that a STR has previously occurred. The BIOS will then write to Register SPND-PC to power-off the appropriate devices. In this mode, the system can wakeup directly from external PM inputs including SWTCH, RING, WAKE0 and WAKE1. If the RTC alarm IRQ8# will be allowed to wake up a system in STR state, one can utilize any unused wake sources or an external microcontroller to monitor the assertion of IRQ8#, then the microcontroller will assert any external wakeup source to resume the system. On resume, the BIOS will perform the proper resume sequence if the CMOS SRAM flag determines that a STR has occurred. In this mode, RCRST# and PWRGOOD must be kept high.

On resume, the BIOS should:

- Read Register WSS bit [10:8] to determine the wake source. If the wake source is an external microcontroller, the BIOS should interrogate the microcontroller on the source.
- Clear the wake source by writing Register WSS bit [10:8] to '111'.
- Execute resume sequence.

NOTE: All power planes of V1-LS must be kept on during the STR mode.

The following registers are reset during 5-V Suspend mode:

Table 3-17. Registers Reset During 5-V Suspend Mode

Index	Register Type	Registers Reset During 5-V Suspend
1XXH	Miscellaneous	110H-114H; 118H-119H, 11BH-11FH
2XXH	DRAM	None
3XXH	PMC	300H-304H; 310H (bit[4:0]); 311H; 314H-31DH; 320H-32DH; 335H-338H; 344H-34DH;
4XXH	L2 Cache	400H-402H
n.a.	PCI	All

3.2.9.5 CPU Clock Management (Using Clock Throttling)

Clock throttling, a technique that periodically modulates STPCLK# without stopping or scaling the clock to the CPU, has been used extensively in VESUVIUS-LS. This is because the minimum CPU bus frequency is 33 MHz and even if the CPU is allowed to run at that frequency continuously, it will still consume substantial power (and generate heat). In VESUVIUS-LS, the system designer can select both the clock throttling period (CTP) and clock throttling ratio or duty cycle (CTR) to fit various hardware and operating system requirements. For example, you may not want to select a CTP longer than the time slot in a multitasking operating system. CPU speed emulation — a by-product of clock throttling — is possible because the CPU performance will be scaled during STPCLK# throttling. Also, clock throttling can achieve substantial power-saving without the PLL stabilization penalty associated with Stop Clock state.

The VESUVIUS-LS has an independent CTR control during the following modes:

- Conserve mode, through Register CON-CTRC
- THERM input indicating overheat condition, through Register HR-CTRC
- Doze/Sleep mode, through Register DS-CTRC

Register CTPC selects the CTP from 800T to 409600T (where T=CPU bus frequency period) and the CTP is applicable to all CTRs. Example: If the CPU bus frequency is 66 MHz or T=15 ns, setting Register CTPC bit [2:0] to ‘100’ or 12800T will enable STPCLK# to throttle with the duty cycle programmed in the 192-µs period when triggered.

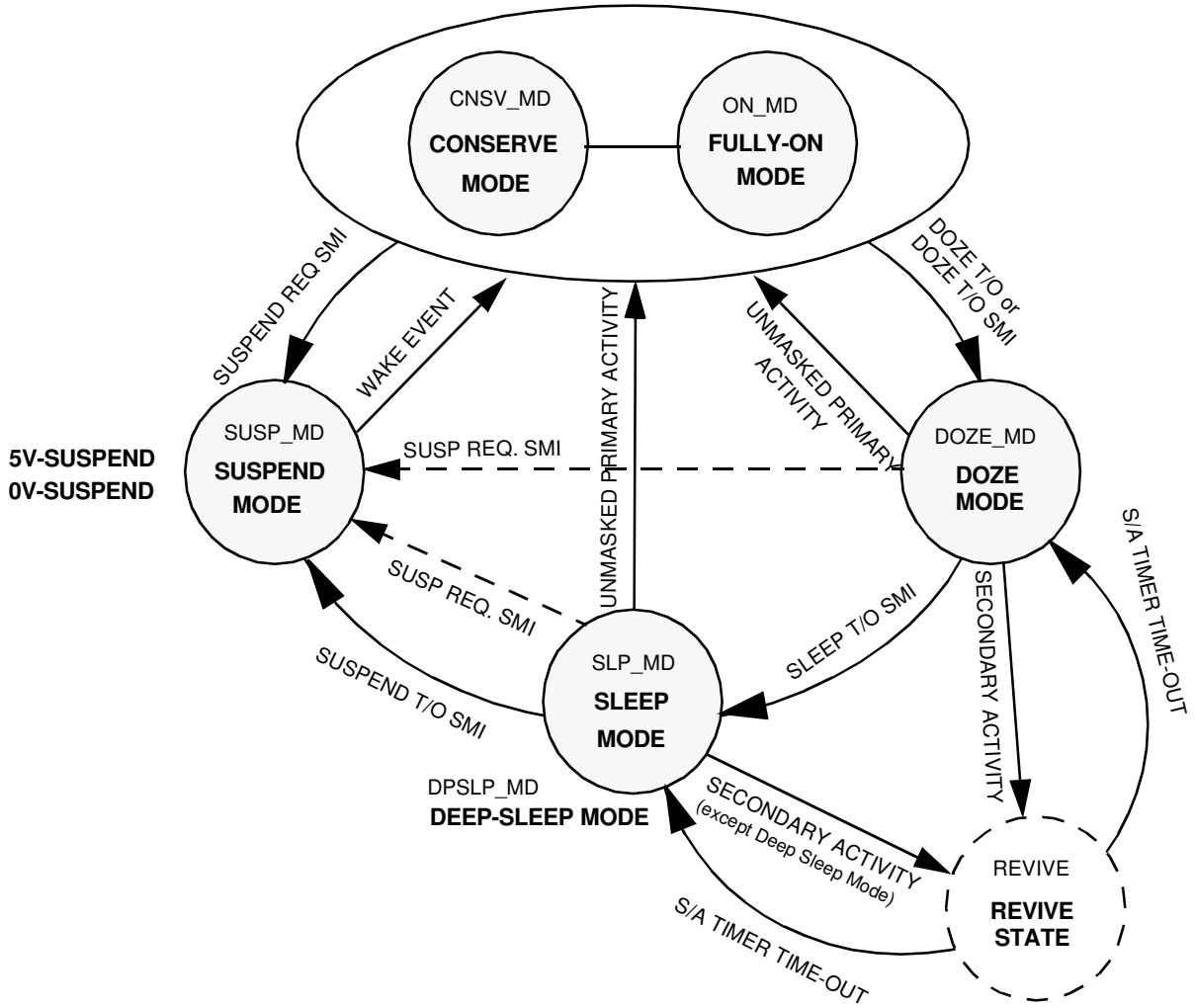


Figure 3-12. Conceptual Visualization of Power Management Mode s

Refer to Figure 3-13 for additional information. Each CTR is selectable as 5 percent or 10 to 90 percent in 10 percent steps. The percentage is defined as the time when the CPU is operating, or STPCLK# is deasserted. This gives independent and automatic control when switching between different modes. For example, if a user selects CON-CTRC=50%, HR-CTRC=5% and DS-CTRC=20%, once Conserve mode is enabled, STPCLK# will start throttling with 192 µs period and STPCLK# will be deasserted 50 percent of the time. If THERM — programmable as active-high or active-low in Register PINMUX bit [7:6] — is asserted indicating a CPU overheat condition, STPCLK# will change the throttling ratio to only 5 percent of the time deasserted.

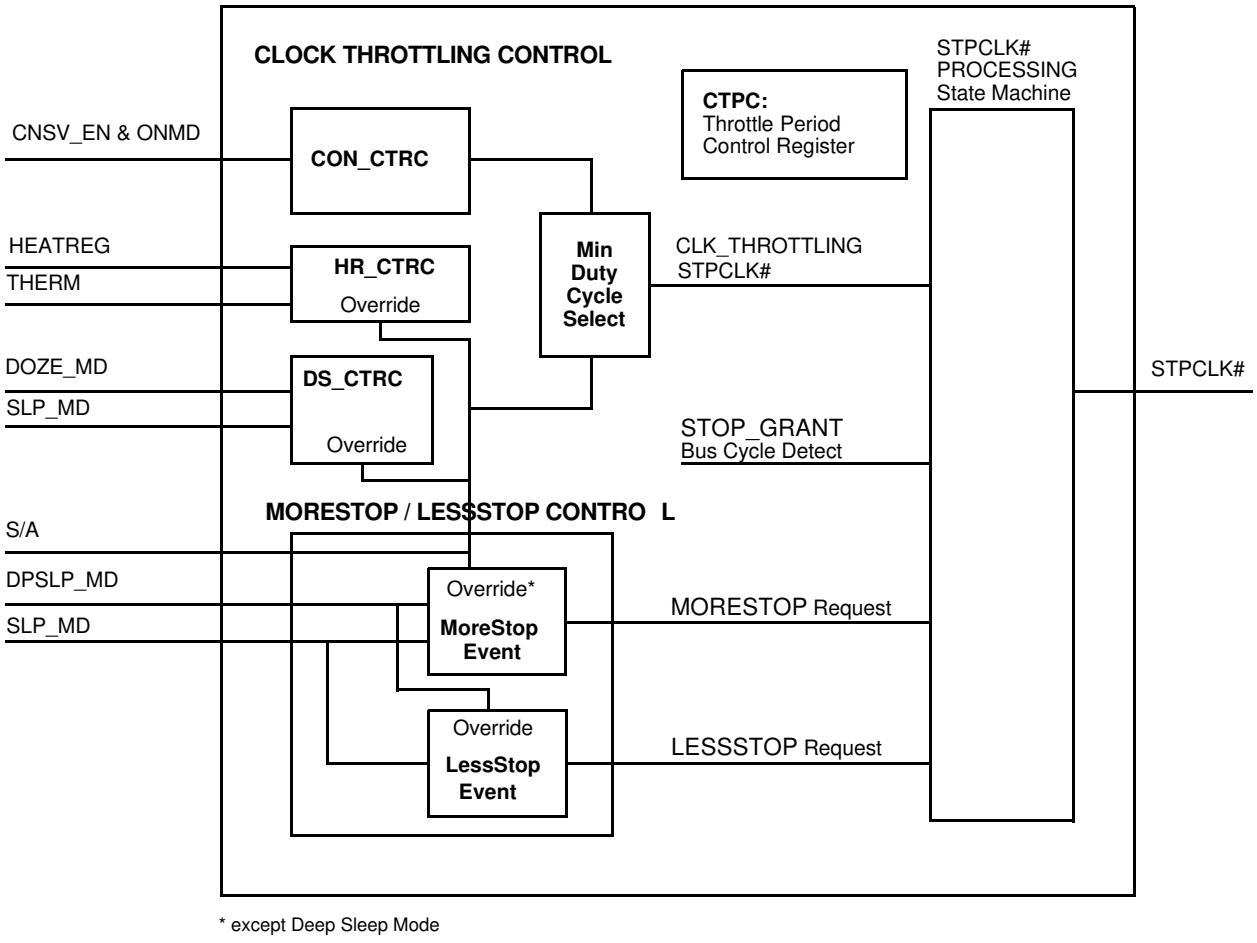


Figure 3-13. STPCLK# Generation in VESUVIUS-LS

On entering the Doze mode (with THERM input deasserted), the V1-LS will change the STPCLK# throttling ratio to 20 percent. To prevent the CPU from overheating due to incorrect parameters, the V1-LS is equipped with a “Minimum Duty Cycle Selector.” Therefore, if CON-CTRC=20%, and HR-CTRC=50%, asserting THERM will not change throttling ratio to 50 percent; the minimum duty cycle selector will choose 20 percent instead.

Note that S/A will override MoreStop, LessStop, HR-CTRC and DS-CTRC's STPCLK# assertion. This means that if the Conserve mode is not enabled, S/A will immediately deassert STPCLK# to process the S/A event. In the case of MORESTOP, STPCLK# will be deasserted after the PLL Restart Latency. However, if Conserve mode is enabled, S/A will revert to the throttling ratio defined in Register CON-CTRC.

Both Doze and Sleep mode enable throttling ratios defined by Register DS-CTRC bit [3:0]. Sleep mode provides options other than clock throttling, like LessStop, MoreStop or Deep-Sleep mode. Refer to Section 3.2.9.4 on page 1-65for details.

3.2.9.6 SMI Sources

The V1-LS can generate PMI, which triggers SMI#, from 14 different groups and up to 52 individual events. Table 3-18 shows the SMI sources defined in Register WSS bit [4:0] and the corresponding actions in the SMM handler. Refer toFigure 3-14 on page 1-72for a diagrammatic presentation of all the SMI sources. Due to the nature of different SMI groups, they are masked or unmasked through different mechanism.

Table 3-18. SMI Sources

Bit[4:0]	Source Group	Action in SMM Handler
00H	None	
01H	Primary Activity	Read AFR1, AFR2 to determine activity source, execute P/A handler, and then clear activity flag.
02H	I/O Trap	Read AFR1 to determine activity source, execute I/O Trap handler, and then clear activity flag.
03H	Device Timers time-out	Read AFR2 bit[13:8] to determine time-out source, execute device time-out handler, and then clear activity flag.
04H, 05H,- 06H	Doze, Sleep, or Suspend time-out	Read Register PMTS to confirm, execute PM mode switching handler, and then clears corresponding time-out status bit.
07H 08H	GP Timer Compare SWTCH Input Toggling	Execute GP Timer Time-out handler Execute SWTCH handler.
0AH, 0BH	WAKE0, 1 Input Toggling	Execute WAKE0, 1 handler.
0CH,	EXTACT0 Input Toggling	Execute EXTACT0 handler.
0EH	Rescheduled PMI	Recall SMI that has been previously rescheduled, and then execute appropriate SMM handler.
0FH	Software SMI	Execute APM-related handler (typical).
10H	V3-LS INT SMI	Read V3-LS Register PMIIRQS-1 and PMIIRQS-2 to determine IRQ source, execute SMM, and then clear activity flag.

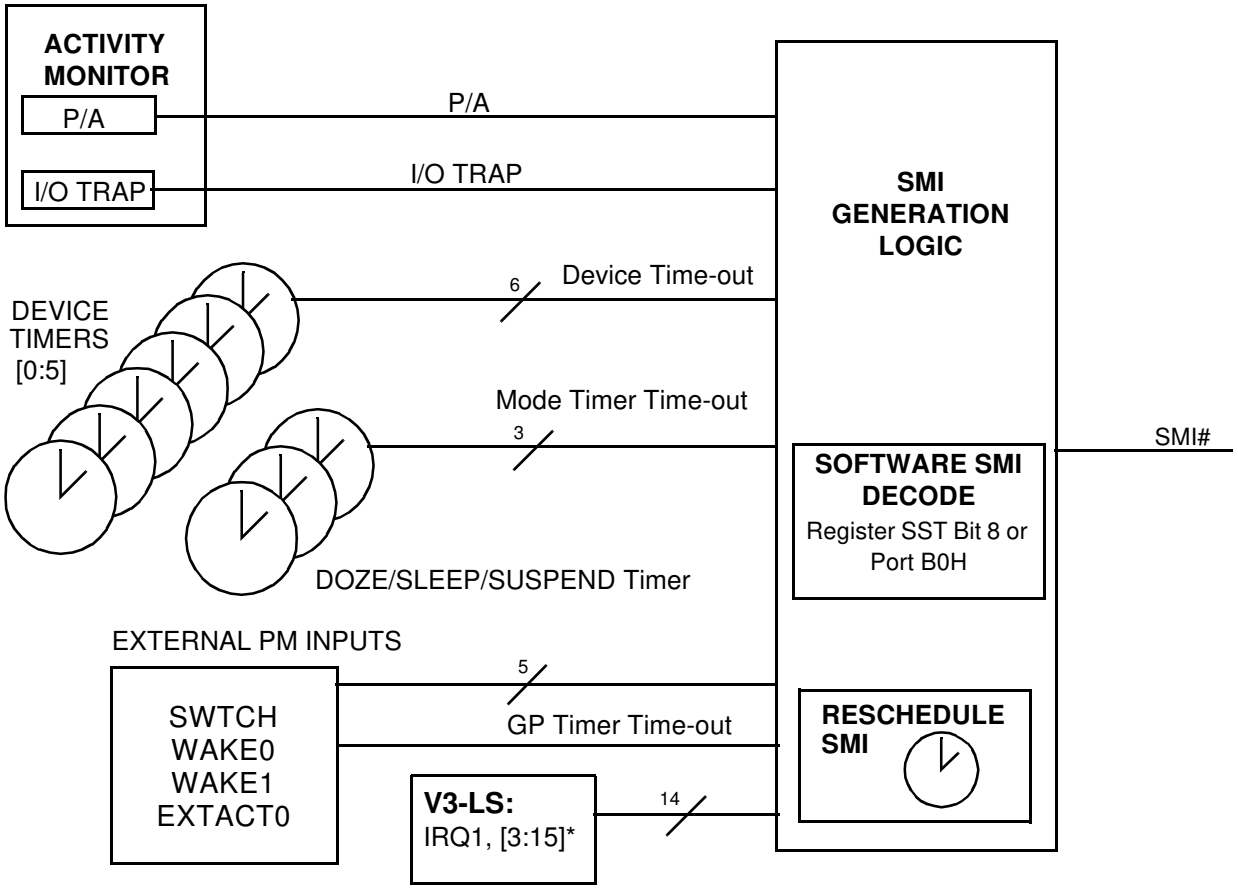


Figure 3-14. SMI# Generation in VESUVIUS-LS

SMI Triggered by P/A

P/A will trigger SMI if Register PAOC bit 1, SMI_MSK_PA is set to '0' and any unmasked P/A occurs. Individual P/A can be unmasked by Register PAM1, PAM2, and V3-LS Register PAIRQM-1 or PAIRQM-2.

SMI Triggered by I/O Trap

There is no group mask for an I/O Trap event. SMI will always be generated if the corresponding bit in Register IOTM is set to '0' and an access to that device occurs. Refer to Section 3.2.9.8 on page 1-74 for I/O Trap and Restart support in V1-LS.

SMI Triggered by Device Timers Time-out

Time-out of device Timer [5:0] will trigger SMI if the corresponding bit in Register ISTM bit [5:0] is unmasked. Refer to Section 3.2.9.4 on page 1-65 for using Device Timers in I/O Trap operation in V1-LS.

SMI Triggered by Doze, Sleep or Suspend Time-out

Doze, Sleep or Suspend time-out will trigger SMI if the corresponding bit in Register ISTM bit [6:8] is unmasked. See Section 3.2.9.4 on page 1-65for power management modes.

SMI Triggered by SWTCH, WAKE0, WAKE1, and EXTACT0 Toggling

Toggling of SWTCH, WAKE0/1, and EXTACT0 will trigger SMI if the appropriate bits in Register ESTM bit [4:0] are unmasked. Programmable in Register EDC (Edge Detection Control), power management input "toggling" can be selected to trigger either on rising, falling or both rising and falling edges. See Section 3.2.9.10 on page 1-76for more information on PM inputs.

Rescheduled SMI

If a SMI is triggered during a critical system operation, especially if it requires the system resources currently in use, that SMI should be rescheduled. Example: The system is updating the HDD while a 0V-Suspend request is issued. In this instance, the SMI should be rescheduled until all HDD operations are done. Typically, a flag will be setup to tell which SMI source is being rescheduled so that on Rescheduled SMI, the SMM handler can read the flag and determine the original SMI event. The rescheduling can range from 10 ms to 900 ms, selectable by Register SST bit [4:0]. In some situations, the same event may need to be rescheduled more than once.

Software SMI

Software SMI is mainly triggered by APM-idle call. V1-LS has two options for the APM BIOS to trigger a software SMI:

1) If a value of '1' is written to Register SST bit 8, this will trigger a software SMI.

2) If Register SST bit 9 is set to '1', a write to I/O port 0B0H will trigger a SMI.

When APM issues a call for low or very low power operation, the SMM handler then has a choice of putting the system into Doze, Sleep or Deep- Sleep mode with appropriate CTRs setup.

Nested SMI

The VESUVIUS-LS fully supports nested SMI. It is recommended that the SMM handler should check if there is any pending SMI before exiting SMM; this will save tremendous overhead on entering and exiting SMM. Multiple SMIs that occur simultaneously will be latched. To ensure that pending SMI will not be lost at the end of the current SMM handler, it should clear the SMI source by writing 1Fh to Register WSS bit [4:0], and then clear the corresponding activity flag in Register AFR1 or AFR2. The SMM handler can then detect any pending SMI by reading Register WSS bit [4:0]. The presence of a non-zero value indicates that a pending SMI exists and the SMM handler can then jump directly to the proper SMM handler to process it.

There are two simple rules for nested SMI:

1) On polling for nested SMI, the next SMI that pops up will be based on priority, but will not be in a chronological order.

2) SMI can be generated and nested in any sequence, except that the same SMI source cannot be nested itself before the SMM handler clears the SMI source and its activity flag.

3.2.9.7 Device Timer Time-out

The V1-LS has six device timers with time-out values ranging from 1 sec. to 90 min. in either 1 sec., 10 sec., 1 min., 10 min. steps. These device timers are independently programmable by Registers DDT0 to

DDT5. All monitored devices, including VGA, primary IDE, secondary IDE, FDD, KBC, serial I/O 1 and 2, parallel port, PRM0/1 and EXTACT0 can be linked to the device timers. Each timer can be linked to one or more devices, but each device can be linked to only one timer. The devices and timers are linked through the Registers DDTS1 to DDTS4 (Device Timer time-out Source). Note that EXTACT0 is used to monitor devices that are equipped with an output that indicates access to that device.

The VESUVIUS-LS also has a special device timer feature: the BIOS can setup a device timer without linking any device to it, which will then become a generic timer to trigger SMI. In the VESUVIUS-LS, the designer has up to seven generic timers, including six device timers and a doze timer (DZMT). If bit 8 of DZMT is set to '0' it will prevent a P/A from resetting the doze timer.

3.2.9.8 I/O Trap and Restart Support

I/O Trap and Restart, a special CPU feature, is usually used to trap an I/O access to a powered-off device. If the CPU accesses a device which has been powered-off, the V1-LS can generate an SMI to initiate an I/O Trap event if SMI# is asserted at least three CPUCLK before BRDY# is asserted (guaranteed by V1-LS). The SMM handler will power-on the device and instruct the CPU to restart the I/O cycle by writing a value 0FFH to offset 7F00H in SMRAM.

Devices that are powered-off during Fully-On, Doze or Sleep modes can result from either PC toggling during mode-switching or time-out of any of the six device timers triggering SMI to power-off the idle device(s). A device timer can be linked to one or more monitored devices and any access to the device(s) will reset the linked device timer if there is no activity on the linked device(s) for the preprogrammed period. A device timer time-out SMI (seeSection 3.2.9.6 on page 1-71) will be triggered and the SMM handler will then power-off or power-down the device(s).

Note that the I/O trapping address range can be different from the P/A monitoring range for the same device. Refer to Table 3-19 for the address ranges.

Table 3-19. I/O Trap and Primary Activity Address Ranges

Device	Primary Activity Address Range	I/O Trap Address Range
Hard Disk 1	1F0H-1F7H, 3F6H	1F0H-1F7H, 3F6-3F7H
Hard Disk 2	170H-177H, 376H	170H-177H, 376-377H
Floppy Disk Drive	3F2H, 3F4H, 3F5H	3F2H, 3F4H, 3F5H, 3F7H

Programming Example 1

Primary IDE, or Hard Disk 1 is linked to Device Timer 3. On device timer 3 time-out, SMI# is asserted, and the SMM handler will:

- Read Register WSS (Wake/SMI Source) to determine the SMI source. In this example, WSS bit [4:0], or SMISRC, will indicate 03H, or device timers time-out event. Then clear SMI source by writing 1FH to WSS bit [4:0].
- Read Register AFR2 to determine which Device Timer time-out. In this example, Register AFR2 bit 11, DEVTMRTO3, will be set indicating HD1 is timed out by Device Timer 3. Then clear Device Timer [3] time-out flag in Register AFR2.
- Set Register PAM1 bit 1 to mask PAM1 from triggering P/A.
- Clear Register IOTM bit 1 to enable I/O Trapping for HD1 address range (1F0-1F7, 3F6-3F7).

- Power-off HD1 through the appropriate PCx or GPIOx.
- If there is no other pending SMI request, then exit SMM.

Programming Example 2

On CPU accesses to HD1 which is powered-off when device timer 3 times out. The V1-LS will trigger SMI# to initiate the I/O Trap, and the SMM handler will:

- Read Register WSS to determine the SMI source. In this example, WSS bit [4:0] will indicate 02H, or I/O trap event. Then clear SMI source by writing 1FH to WSS bit [4:0].
- Read Register AFR1 to determine what device access triggers the I/O trapping. In this example, Register AFR1 bit 1, HD1_ACTV will be set indicating HD1 is accessed. Then clear HD1_ACTV flag in Register AFR1.
- Clear Register PAM1 bit 1 to enable PAM1 to trigger P/A.
- Set Register IOTM bit 1 to mask I/O Trapping for HD1 access.
- Power on HD1 through the appropriate PCx or GPIOx.
- Optionally, wait for 3 seconds for HD1 to spin-up to accept commands.
- If there is no other pending SMI request, then exit SMM.

3.2.9.9 Programmable Range Monitors (PRM)

The V1-LS has six PRMs, namely PRM[5:0]. PRM is defined primarily for activity detection and can be used to monitor any user-defined I/O or memory address ranges. It can also detect either read, write or both read and write access to trigger an event. The following describes how the PRM is programmed. PRM[5:0] are independently programmable:

Register PRM_CTRL1 bit [5:0] controls PRM[5:0] to monitor either memory or I/O.

Register PRM_CTRL1 bit[13:8] enables PRM[5:0].

Register PRM_CTRL2 bit [5:0] enables ‘write access’ to trigger PRM[5:0] event.

Register PRM_CTRL2 bit [13:8] enables ‘read access’ to trigger PRM[5:0] event.

The PRM address compare logic works like this: A ‘base address’ Register defines the base I/O or memory address range of the device. For an I/O device, PRMAx[15:0] will correspond to A[15:0]. For a memory device, PRMAx[14:0] corresponds to A[28:14] and PRMAx15 will be ignored. A ‘compare mask’ register is a bit mask defining which PRMAx[15:0] will be compared against the equivalent CPU address in the decoder.

Programming Example 1

If PRM0 is used to decode and monitor write-access to an audio device with address 0220-022F, then:

PRM_CTRL1 bit 0 = ’0’, bit 8 = ’1’

PRM_CTRL2 bit 0 = ’1’, bit 8 = ’0’

PRMA0 should be set to 0220h

PRMC0 should be set to FFF0h

Programming Example 2

If PRM1 is used to decode and monitor read/write access to two memory address blocks, one at 128 Mbyte and another at 129 Mbyte boundary, then:

PRM_CTRL1 bit 1 = '1', bit 9 = '1'

PRM_CTRL2 bit 1 = '1', bit 9 = '1'

PRMA1 should be set to 2000H

PRMC1 should be set to FF80H

3.2.9.10 Power Management (PM) Inputs

Power management inputs are defined as inputs involved with power management functions like triggering a P/A, S/A, SMI or wakeup event. The following five PM inputs are available in V1-LS: SWTCH, WAKE0, WAKE1, EXTACT0, and RING. The PM inputs have the following characteristics:

- All inputs can be unmasked to trigger P/A (see Register PAM2).
- Activities on unmasked inputs can be read through Register AFR2.
- All input pin status can be read through Register PMPS.
- All inputs can be unmasked to trigger SMI, except RING input (see Register ESTM).
- All inputs can be unmasked to wake up from suspend, except EXTACT0 (see Register WMC).
- All inputs have independent debounce control through Register DBC.
- All inputs have independent edge detect control through Register EDC.

Other Characteristics

- EXTACT0 can be unmasked to trigger S/A (see Register SAM).
- EXTACT0 can be linked to reset device timers (see Register DTTS4).
- The number of RING to wake up from suspend is programmable in Register RCC.
- The wake mask of SWTCH is default-disabled, all other wake masks are default-enabled.

THERM, dedicated for external thermal sensor input to trigger clock throttling with ratio defined in HRCTRC, is also a PM input although it doesn't perform any function other than preventing prolonged CPU overheat condition. Refer to Register PINMUX for more information.

Reading PM Input Pin Status

The V1-LS provides Register PMPS for SMM handler to read the pin status (except THERM) of all the PM inputs. This is necessary for any PM inputs programmed to trigger on both rising and falling edges. The BIOS needs to read the pin status to determine the proper action. Example: A lid switch is connected to EXTACT0 which generates a falling edge on closing the lid and a rising edge on opening it, and both will trigger SMI. The SMM handler will read the EXTACT0 status from Register PMPS. If it is '0', then it will turn off the LCD backlight and vice versa.

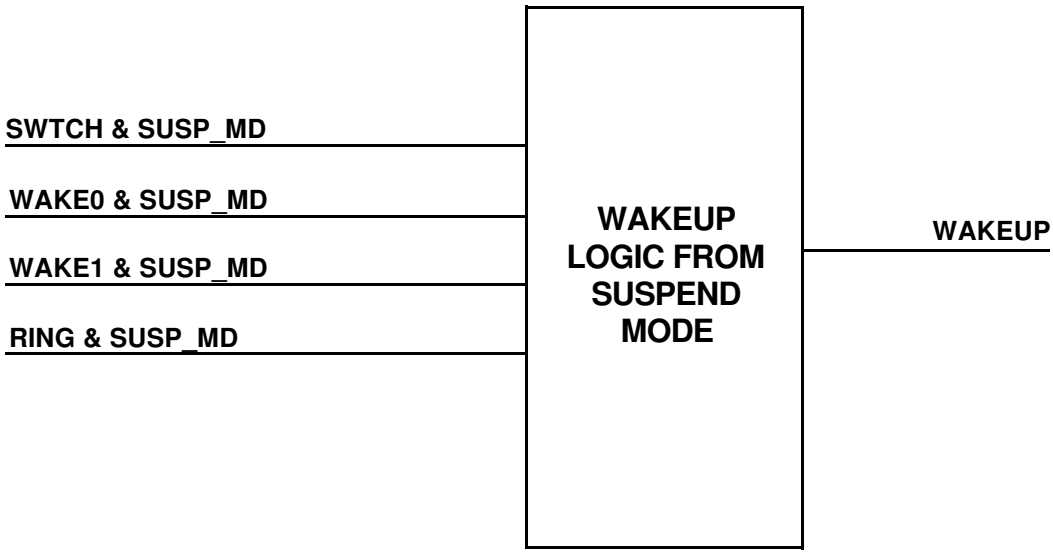


Figure 3-15. WAKE Sources in VESUVIUS-LS

3.2.9.11 PCICLK Power Management

The V1-LS has proprietary PCICLK power management control. Register PCIC bit [5:4] selects the number of PCICLKs that the PCI bus has idled (FRAME# and IRDY# deasserted). The idle count ranges from 0 (immediate) to 256 PCICLKs. When the idle condition is met, PCICLK will be divided down by the PCICLK divisor programmed in Register PCIC bit [1:0].

On CPU-initiated PCI bus cycle, PCICLK is returned to full speed immediately before FRAME# is being asserted and there is no performance loss. On PCI master cycle, V1-LS will detect REQ# assertion to return PCICLK to full speed. Slowing down the PCICLK will increase the latency in recognizing REQ# but does not cause a performance loss.

4. V1-LS REGISTER INFORMATION

This chapter describes the registers contained in the V1-LS device. The registers are divided into the following groups:

- Reset Sampling and Miscellaneous Registers
- DRAM Registers
- PMC Registers
- Level-2 Cache Registers
- PCI Configuration Registers

NOTE: Some registers discussed here may not be consecutively numbered ; registers reserved for future expansion are not shown in this chapter. Note that 16-bit access to Port 24H and 26H will be directed to V1-LS and not passed to the PCI bus. Access to V3-LS registers must be executed as an 8-bit access to Port 24H and 26H.

4.1 Register Summary Table

This table shows the index numbers and page cross-references to detailed register descriptions.

Index	Register Name	Abbreviation	Page
Reset Sampling and Miscellaneous Registers			
100H	Revision ID Register	V1_ID	1-81
101H	V1 Power On Register	V1_POC	1-82
110H	Programmable Region 1 Register	PR1	1-84
111H	Programmable Region 2 Register	PR2	1-85
112H	Programmable Region 3 Register	PR3	1-86
113H	Programmable Region 4 Register	PR4	1-87
114H	Programmable Region Control Register	PRC	1-88
118H	SMM Control Register	SMMC	1-90
119H	Processor Control Register	PROC	1-93
11AH	Write FIFO Control Register	WFIFOC	1-95
11BH	PCI Control Register	PCIC	1-96
11CH	Clock Skew Adjust Register	CSA	1-97
11DH	Bus Master and Snooping Control Register	SNOOPCTRL	1-98
11EH	Arbiter Control Register	ARBCTRL	1-99
11FH	Docking Control Register	DOCKC	1-100
DRAM Registers			
200H	Shadow RAM Read Enable Control Register	SHADRC	1-101
201H	Shadow RAM Write Enable Control Register	SHADWC	1-103
202H	Bank 0 Control Register	B0C	1-105
203H	Bank 1 Control Register	B1C	1-106
204H	Bank 0/1 Timing Control Register	B01TC	1-107
205H	Bank 2 Control Register	B2C	1-109
206H	Bank 3 Control Register	B3C	1-110
207H	Bank 2/3 Timing Control Register	B23TC	1-111
208H	Bank 4 Control Register	B4C	1-113
209H	Bank 5 Control Register	B5C	1-114
20AH	Bank 4/5 Control Register	B45TC	1-115
20BH	Bank 6 Control Register	B6C	1-117
20CH	Bank 7 Control Register	B7C	1-118
20DH	Bank 6/7 Timing Control Register	B67TC	1-119
20EH	DRAM Configuration Register 1	DCONF1	1-121
20FH	DRAM Configuration Register 2	DCONF2	1-122

4.2 Reset Sampling and Miscellaneous Registers

4.2.1 Revision ID Register (V1_ID)

Index: 100H

Bit	Description	Name	Reset State
0	V1-LS Mask ID [0]	V1LS_MSK_ID0	'0'
1	V1-LS Mask ID [1]	V1LS_MSK_ID1	'0'
2	V1-LS Mask ID [2]	V1LS_MSK_ID2	'0'
3	V1-LS Mask ID [3]	V1LS_MSK_ID3	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**V1-LS Mask ID [3:0]:** These bits indicate the metal-mask version of the V1-LS device. 3H = Revision AA 4H = Revision BB 5H = Revision CC
15:4	Reserved

4.2.2 V1 Power On Register (V1_POC)

Index: 101H

Bit	Description	Name	Default State
0	Miscellaneous Configuration Bit [0]	MISC_CFG0	PU/PD strap
1	Miscellaneous Configuration Bit [1]	MISC_CFG1	PU/PD strap
2	Miscellaneous Configuration Bit [2]	MISC_CFG2	PU/PD strap
3	Clock Skew Adjust [0]	CLK_SKW0	PU/PD strap
4	Clock Skew Adjust [1]	CLK_SKW1	PU/PD strap
5	Clock Skew Adjust [2]	CLK_SKW2	PU/PD strap
6	DRAM Power Plane Voltage	DRAM_VCC	PU/PD strap
7	PCI Power Plane Voltage	PCI_VCC	PU/PD strap
8	Snooping Scheme	SNOOP_CFG	PU/PD strap
9	Reserved		PU/PD strap
10	Tristate All Outputs	TRSTATE	PU/PD strap
11	Internal Clocks for Simulation	INT_CLK	PU/PD strap
12	Reserved		PD strap
13	Reserved		PD strap
14	Reserved		PD strap
15	Reserved		PD strap

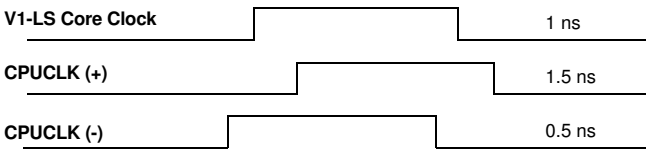
The V1 Power On register is loaded on the leading edge of the RCRESET pulse. This pulse should be triggered by power first being applied to the V1-LS device. At this time the present value of MA[11:0] will be loaded into the corresponding register bits. Once set, this register becomes read only. To select the desired options for a particular system, each MA pin should have either a pull-up or pull-down connected. From the point of powering up the V1-LS until slightly past the leading edge of RCRESET pulse, all MA pins will be floating. Therefore, the pull-up or pull-down will easily set each MA pin to the appropriate high or low value. It is recommended that 100 K resistors be used. Since MA pins do not have internal pull-downs, every MA pin should have either a pull-up or pull-down connected externally to ensure Power-On sampling.

NOTE: All reserved bits in this register must be pulled-down to ensure future compatibility.

IMPORTANT: Refer to Appendix F for special information related to silicon revision BB.

Bit	Description
2:0	**Miscellaneous Configuration Bit [2:0]:** These signals can be strapped to indicate miscellaneous system configuration. Example: In the case of Intel's Pentium or Cyrix's M1 processors, the user can define the bus-to-core frequency ratio to simplify the BIOS detection algorithm.

Bit	Description *(cont.)*
5:3	**Clock Skew Adjust:** These bits can be used to adjust the clock skew of CPUCLK, relative to V1-LS core clock. The following illustration shows how to interpret '+' and '-' delay.



Bit [2:0]	Delay (relative to V1 core clock)
'000'	0.0 ns (recommended default)
'001'	+0.55 ns
'010'	+1.10 ns
'011'	+1.65 ns
'100'	-2.20 ns
'101'	-1.65 ns
'110'	-1.10 ns
'111'	-0.55 ns

6	**DRAM Power Plane Voltage:** '0' = 3.3-V; '1' = 5-V. **NOTE:** This bit applies to Revision BB and later silicon revisions.
7	**PCI Power Plane Voltage:** '0' = 3.3-V; '1' = 5-V. **NOTE:** This bit applies to Revision BB and later silicon revisions.
8	**Snooping Scheme:** '0' = HOLD/HLDA; '1' = BOFF#/LOCK#. **NOTE:** This bit applies to Revision CC and later silicon revisions.
9	Reserved
10	**Tristate All Outputs:** When this bit is set to '0', it indicates a 'no tristate' condition; when set to '1', it indicates a 'tristate' condition.
11	**Use Internal Clocks for Simulation Purposes:** When this bit is set to '0', it disables the internal clock speedup. Setting this bit to '1' enables the internal clock speedup.
15:12	Reserved

4.2.3 Programmable Region 1 Register (PR1)

Index: 110H

Bit	Description	Name	Reset State
0	Programmable Region 1 Block Size [0]	PREG1S0	'0'
1	Programmable Region 1 Block Size [1]	PREG1S1	'0'
2	Programmable Region 1 Block Size [2]	PREG1S2	'0'
3	Programmable Region 1 Starting Address [15]	PREG1A15	'0'
4	Programmable Region 1 Starting Address [16]	PREG1A16	'0'
5	Programmable Region 1 Starting Address [17]	PREG1A17	'0'
6	Programmable Region 1 Starting Address [18]	PREG1A18	'0'
7	Programmable Region 1 Starting Address [19]	PREG1A19	'0'
8	Programmable Region 1 Starting Address [20]	PREG1A20	'0'
9	Programmable Region 1 Starting Address [21]	PREG1A21	'0'
10	Programmable Region 1 Starting Address [22]	PREG1A22	'0'
11	Programmable Region 1 Starting Address [23]	PREG1A23	'0'
12	Programmable Region 1 Starting Address [24]	PREG1A24	'0'
13	Programmable Region 1 Starting Address [25]	PREG1A25	'0'
14	Programmable Region 1 Starting Address [26]	PREG1A26	'0'
15	Programmable Region 1 Starting Address [27]	PREG1A27	'0'

Bit **Description**

2:0 **Programmable Region 1 Block Size [2:0]:** These bits indicate the block size of programmable region 1. The following table shows the block size corresponding to how bit [2:0] are set.

Bit [2:0]	Programmable Region 1 Block Size
'000'	32 Kbytes
'001'	64 Kbytes
'010'	128 Kbytes
'011'	256 Kbytes
'100'	512 Kbytes
'101'	1 Mbyte
'11X'	Reserved

15:3 **Programmable Region 1 Starting Address [27:15]:** The programmable region 1 starting address must be a multiple of the block size.

Example: If block size is 128 Kbytes, a starting address 0101 1111 01**0 0** is valid while address 0101 111 011**1 0** is not valid.

NOTE: A[31:28] are decoded as '0'.

4.2.4 Programmable Region 2 Register (PR2)

Index: 111H

Bit	Description	Name	Reset State
0	Programmable Region 2 Block Size [0]	PREG2S0	'0'
1	Programmable Region 2 Block Size [1]	PREG2S1	'0'
2	Programmable Region 2 Block Size [2]	PREG2S2	'0'
3	Programmable Region 2 Starting Address [15]	PREG2A15	'0'
4	Programmable Region 2 Starting Address [16]	PREG2A16	'0'
5	Programmable Region 2 Starting Address [17]	PREG2A17	'0'
6	Programmable Region 2 Starting Address [18]	PREG2A18	'0'
7	Programmable Region 2 Starting Address [19]	PREG2A19	'0'
8	Programmable Region 2 Starting Address [20]	PREG2A20	'0'
9	Programmable Region 2 Starting Address [21]	PREG2A21	'0'
10	Programmable Region 2 Starting Address [22]	PREG2A22	'0'
11	Programmable Region 2 Starting Address [23]	PREG2A23	'0'
12	Programmable Region 2 Starting Address [24]	PREG2A24	'0'
13	Programmable Region 2 Starting Address [25]	PREG2A25	'0'
14	Programmable Region 2 Starting Address [26]	PREG2A26	'0'
15	Programmable Region 2 Starting Address [27]	PREG2A27	'0'

Bit **Description**

2:0 **Programmable Region 2 Block Size [2:0]:** These bits indicate the block size of programmable region 2. The following table shows the block size corresponding to how bit [2:0] are set.

Bit [2:0]	Programmable Region 2 Block Size
'000'	32 Kbytes
'001'	64 Kbytes
'010'	128 Kbytes
'011'	256 Kbytes
'100'	512 Kbytes
'101'	1 Mbyte
'11X'	Reserved

15:3 **Programmable Region 2 Starting Address [27:15]:** The programmable region 2 starting address must be a multiple of the block size.

Example: If block size is 128 Kbytes, a starting address 0101 1111 010**0 0** is valid while address 0101 111 011**1 0** is not valid.

NOTE: A[31:28] are decoded as '0'.

4.2.5 Programmable Region 3 Register (PR3)

Index: 112H

Bit	Description	Name	Reset State
0	Programmable Region 3 Block Size [0]	PREG3S0	'0'
1	Programmable Region 3 Block Size [1]	PREG3S1	'0'
2	Programmable Region 3 Block Size [2]	PREG3S2	'0'
3	Programmable Region 3 Starting Address [15]	PREG3A15	'0'
4	Programmable Region 3 Starting Address [16]	PREG3A16	'0'
5	Programmable Region 3 Starting Address [17]	PREG3A17	'0'
6	Programmable Region 3 Starting Address [18]	PREG3A18	'0'
7	Programmable Region 3 Starting Address [19]	PREG3A19	'0'
8	Programmable Region 3 Starting Address [20]	PREG3A20	'0'
9	Programmable Region 3 Starting Address [21]	PREG3A21	'0'
10	Programmable Region 3 Starting Address [22]	PREG3A22	'0'
11	Programmable Region 3 Starting Address [23]	PREG3A23	'0'
12	Programmable Region 3 Starting Address [24]	PREG3A24	'0'
13	Programmable Region 3 Starting Address [25]	PREG3A25	'0'
14	Programmable Region 3 Starting Address [26]	PREG3A26	'0'
15	Programmable Region 3 Starting Address [27]	PREG3A27	'0'

Bit **Description**

2:0 **Programmable Region 3 Block Size [2:0]:** These bits indicate the block size of programmable region 3. The following table shows the block size corresponding to how bit [2:0] are set.

Bit [2:0]	Programmable Region 3 Block Size
'000'	32 Kbytes
'001'	64 Kbytes
'010'	128 Kbytes
'011'	256 Kbytes
'100'	512 Kbytes
'101'	1 Mbyte
'11X'	Reserved

15:3 **Programmable Region 3 Starting Address [27:15]:** The programmable region 3 starting address must be a multiple of the block size.

Example: If block size is 128 Kbytes, a starting address 0101 1111 01**0 0** is valid while address 0101 111 011**1 0** is not valid.

NOTE: A[31:28] are decoded as '0'.

4.2.6 Programmable Region 4 Register (PR4)

Index: 113H

Bit	Description	Name	Reset State
0	Programmable Region 4 Block Size [0]	PREG4S0	'0'
1	Programmable Region 4 Block Size [1]	PREG4S1	'0'
2	Programmable Region 4 Block Size [2]	PREG4S2	'0'
3	Programmable Region 4 Starting Address [15]	PREG4A15	'0'
4	Programmable Region 4 Starting Address [16]	PREG4A16	'0'
5	Programmable Region 4 Starting Address [17]	PREG4A17	'0'
6	Programmable Region 4 Starting Address [18]	PREG4A18	'0'
7	Programmable Region 4 Starting Address [19]	PREG4A19	'0'
8	Programmable Region 4 Starting Address [20]	PREG4A20	'0'
9	Programmable Region 4 Starting Address [21]	PREG4A21	'0'
10	Programmable Region 4 Starting Address [22]	PREG4A22	'0'
11	Programmable Region 4 Starting Address [23]	PREG4A23	'0'
12	Programmable Region 4 Starting Address [24]	PREG4A24	'0'
13	Programmable Region 4 Starting Address [25]	PREG4A25	'0'
14	Programmable Region 4 Starting Address [26]	PREG4A26	'0'
15	Programmable Region 4 Starting Address [27]	PREG4A27	'0'

Bit **Description**

2:0 **Programmable Region 4 Block Size [2:0]:** These bits indicate the block size of programmable region 4. The following table shows the block size corresponding to how bit [2:0] are set.

Bit [2:0]	Programmable Region 4 Block Size
'000'	32 Kbytes
'001'	64 Kbytes
'010'	128 Kbytes
'011'	256 Kbytes
'100'	512 Kbytes
'101'	1 Mbyte
'11X'	Reserved

15:3 **Programmable Region 4 Starting Address [27:15]:** The programmable region 4 starting address must be a multiple of the block size.

Example: If block size is 128 Kbytes, a starting address 0101 1111 01**0 0** is valid while address 0101 111 011**1 0** is not valid.

NOTE: A[31:28] are decoded as '0'.

4.2.7 Programmable Region Control Register (PRC)

Index: 114H

Bit	Description	Name	Reset State
0	Programmable Region 1 Select [0]	PRGREG1_SEL0	'0'
1	Programmable Region 1 Select [1]	PRGREG1_SEL1	'0'
2	Programmable Region 2 Select [0]	PRGREG2_SEL0	'0'
3	Programmable Region 2 Select [1]	PRGREG2_SEL1	'0'
4	Programmable Region 3 Select [0]	PRGREG3_SEL0	'0'
5	Programmable Region 3 Select [1]	PRGREG3_SEL1	'0'
6	Programmable Region 4 Select [0]	PRGREG4_SEL0	'0'
7	Programmable Region 4 Select [1]	PRGREG4_SEL1	'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

1:0 **Programmable Region 1 Select [1:0]:**

Bit [1:0]	Function
'00'	Disable
'01'	Write-through
'10'	Non-cacheable
'11'	Reserved

3:2 **Programmable Region 2 Select [1:0]:**

Bit [1:0]	Function
'00'	Disable
'01'	Write-through
'10'	Non-cacheable
'11'	Reserved

5:4 **Programmable Region 3 Select [1:0]:**

Bit [1:0]	Function
'00'	Disable
'01'	Write-through
'10'	Non-cacheable
'11'	Reserved

Bit	Description *(cont.)*
7:6	**Programmable Region 4 Select [1:0]:** **Bit [1:0]** — **Function** '00' — Disable '01' — Write-through '10' — Non-cacheable '11' — Reserved
15:8	Reserved

4.2.8 SMM Control Register (SMMC)

Index: 118H

Bit	Description	Name	Reset State
0	Reserved		'0'
1	SMRAM KEN Disable	KDISSMMRAM	'0'
2	Enable 0G+20000H	EN23RMAB	'0'
3	Reserved		'0'
4	SMM D0000H-D7FFFH Select [0]	SMM_DL_SEL0	'0'
5	SMM D0000H-D7FFFH Select [1]	SMM_DL_SEL1	'0'
6	SMM D8000H-DFFFFH Select [0]	SMM_DH_SEL0	'0'
7	SMM D8000H-DFFFFH Select [1]	SMM_DH_SEL1	'0'
8	SMM E0000H-E7FFFH Select [0]	SMM_EL_SEL0	'0'
9	SMM E0000H-E7FFFH Select [1]	SMM_EL_SEL1	'0'
10	SMM E8000H-EFFFFH Select [0]	SMM_EH_SEL0	'0'
11	SMM E8000H-EFFFFH Select [1]	SMM_EH_SEL1	'0'
12	Swap SMM 2/3 Mapping	SWAP_23_MAP	'0'
13	Swap SMM D/E Mapping	SWAP_DE_MAP	'0'
14	Load SMI Handler into SMM RAM	LDSMIHLDER	'0'
15	Lock SMRAM Access in Normal Mode	SMIHLDERLOCK	'0'

Bit	Description
0	Reserved
1	**SMRAM KEN Disable:** '1'= KEN# will be held inactive (high) when SMI is active.
2	**Enable 20000H-3FFFFH Remapped to A0000H-BFFFFH Physical Memory in SMM Mode:** '0' = enable, '1' = disable. This bit can be used to simplify the loading of SMI handler. BIOS must set this bit to '1' after the SMI handler is loaded. Refer to Section 3.2.7.2 on page 1-59 for more information. **NOTE:** This bit can only be used if both L1 and L2 are disabled.
3	Reserved
5:4	**SMM D0000H-D7FFFH Select [1:0]:** **Bit [1:0] — Function** '00' — 000D0000H-000D7FFFH is used as normal memory space. '01' — Reserved '10' — 000D0000H-000D7FFFH is used as SMM space. (Remap to 000A0000H-000A7FFFH in physical DRAM space.) '11' — Reserved **NOTE:** When programmed to '10', 000D0000H-000D7FFFH will be automatically set to non-cacheable.

Bit	Description *(cont.)*
7:6	**SMM D8000H-DFFFFH Select [1:0]:** **Bit [1:0]** — **Function** '00' — 000D8000H-000DFFFFH is used as normal memory space. '01' — Reserved '10' — 000D8000H-000DFFFFH is used as SMM space. (Remap to 000A8000H-000AFFFFH in physical DRAM space.) '11' — Reserved **NOTE:** When programmed to '10', 000D8000H-000DFFFFH will be automatically set to non-cacheable.
9:8	**SMM E0000H-E7FFFH Select [1:0]:** **Bit [1:0]** — **Function** '00' — 000E0000H-000E7FFFH is used as normal memory space. '01' — Reserved '10' — 000E0000H-000E7FFFH is used as SMM space. (Remap to 000B8000H-000BFFFFH in physical DRAM space.) '11' — Reserved **NOTE:** When programmed to '10', 000E0000H-000E7FFFH will be automatically set to non-cacheable.
11:10	**SMM E8000H-EFFFFH Select [1:0]:** **Bit [1:0]** — **Function** '00' — 000E8000H-000EFFFFH is used as normal memory space. '01' — Reserved '10' — 000E8000H-000EFFFFH is used as SMM space. (Remap to 000B8000H-000BFFFFH in physical DRAM space.) '11' — Reserved **NOTE:** When programmed to '10', 000E8000H-000EFFFFH will be automatically set to non-cacheable.
12	**Swap SMM 2/3 Mapping:** When set to '0', 00020000H–0002FFFFH region will be mapped to 000A0000H–000AFFFFH and 00030000H–0003FFFFH region will be mapped to 000B0000H–000BFFFFH. When set to '1', 00020000H–0002FFFFH region will be mapped to 000B0000H–000BFFFFH and 00030000H–0003FFFFH region will be mapped to 000A0000H–000AFFFFH. **NOTE:** This bit applies to Revision BB and later silicon revisions.
13	**Swap SMM D/E Mapping:** When set to '0', 000D0000H–000DFFFFH region will be mapped to 000A0000H–000AFFFFH and 000E0000H–000EFFFFH region will be mapped to 000B0000H–000BFFFFH. When set to '1', 000D0000H–000DFFFFH region will be mapped to 000B0000H–000BFFFFH and 000E0000H–000EFFFFH region will be mapped to 000A0000H–000AFFFFH. **NOTE:** This bit applies to Revision BB and later silicon revisions.

Bit	Description *(cont.)*
14	**Load SMI Handler into SMM RAM:** '1' = enable access to SMM RAM during normal cycle; '0' = disable access to SMM RAM during normal cycle. **NOTE:** SMI handler loading is directly achieved through A0000-BFFFF range.
15	**SMM RAM Access in Normal Mode Lock:** This bit provides an option to lock bit 14 in a disabled state, thereby prohibiting any further access to SMM RAM from normal mode. This bit can only be written once. Reading a '0' from this bit indicates that bit 14 is not locked. Reading a '1' from this bit indicates that bit 14 is locked to a disabled state.

4.2.9 Processor Control Register (PROC)

Index: 119H

Bit	Description	Name	Reset State
0	Cache Enable	KENEN	'0'
1	L1 Write-Back Enable	WB_ENABLE	'0'
2	Enable Processor Pipeline Mode	PIPELINEEN	'0'
3	Enable Linear Burst	LINEARBURST	'0'
4	Enable Combine of KEN# and INV Pins	EN_KEN_INV	'0'
5	Enable Write FIFO	WRFIFO_EN	'0'
6	INV is Asserted for Write Cycle Only	INV_ON_WR	'0'
7	Reserved		'0'
8	Disable FPU Error Clearing by F0H	DIS_FPUCLR_F0	'0'
9	Disable FPU Error Clearing by F1H	DIS_FPUCLR_F1	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**CACHE Enable:** When low, KEN# will be forced to an inactive state for all cycles. When high, KEN# will be asserted for all local memory cycles.
1	**L1 Write-Back Enable:** When low, WB_WT# will always be in write-through state. When high, WB_WT# will be in write-back state whenever it is possible.
2	**Enable Processor Pipeline Mode:** '0' = disable; '1' = enable.
3	**Enable Linear Burst:** '0' = toggle burst; '1' = linear burst. This bit should be set to the correct value before L1 and L2 cache is turned on.
4	**Enable Combination of KEN# and INV Pins:** When low, KEN# will only indicate cacheability of the cycle and CPU's INV input should be either pulled high or connected to W_R#. When high, KEN# and INV functionality will be combined into a single pin and KEN# should also be connected to CPU's INV pin.
5	**Enable Write FIFO:** '0' = disable; '1' = enable. When disabled, the write FIFO is forced to one level. When enabled, the write FIFO is forced to eight level.
6	**INV is Asserted for Write Cycle Only:** When '0', INV be asserted for both read and write cycles; when '1', INV will be asserted for write cycle only.
7	Reserved

Bit	Description *(cont.)*
8	**Disable FPU Error Clearing by Writing to I/O Port F0H:** Setting this bit to '0' will enable the clearing of FPU error by writing to I/O port F0H; setting it to '1' will disable it.
9	**Disable FPU Error Clearing by Writing to I/O Port F1H:** Setting this bit to '0' will enable the clearing of FPU error by writing to I/O port F1H; setting it to '1' will disable it.
15:10	Reserved

4.2.10 Write FIFO Control Register (WFIFOC)

Index: 11AH

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Reserved		'0'
2	Reserved		'0'
3	DRAM Read Reordering Enable	DRMRDREODEREN	'0'
4	PCI Read Reordering Enable	PCIRDREODEREN	'0'
5	PCI Write Buffering Select [0]	PCIWRBUFSEL0	'0'
6	PCI Write Buffering Select [1]	PCIWRBUFSEL1	'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'1'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
2:0	Reserved
3	**DRAM Read Reordering Enable:** '0' = disable; '1' = enable. When this bit is set and there is a pending DRAM write cycle, a DRAM read operation will be preceded by a DRAM write operation. **NOTE:** This bit applies to Revision BB and later silicon.
4	**PCI Read Reordering Enable:** '0' = disable; '1' = enable. When this bit is set and there is a pending DRAM write cycle, a PCI read operation will be preceded by a DRAM write operation. **NOTE:** A PCI read operation will never get reordered around a pending PCI write cycle. This bit applies to Revision BB and later silicon.
6:5	**PCI Write Buffering Select[1:0]:** **Bit [1:0] — Function** 00 — Disable 01 — Post-write PCI IO Write Cycle Only 10 — Post-write PCI Memory Write Cycle Only 11 — Post-write All PCI Write Cycles
15:7	Reserved

4.2.11 PCI Control Register (PCIC)

Index: 11BH

Bit	Description	Name	Reset State
0	Reserved		'0'
1	PCI Master-to-DRAM Burst Enable	PCI2DRM_BRST_EN	'0'
2	Reserved		'0'
3	Enable Optimized Address Transfer	ENOPT_ADDR_XFR	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	Reserved
1	**PCI Master-to-DRAM Burst Enable:** When this bit is set to '0', V1-LS will conduct a single PCI transfer only when the PCI Master is accessing the DRAM. When set to '1', V1-LS will attempt a burst to DRAM when PCI Master is accessing.
2	Reserved
3	**Enable Optimized Address Transfer Between V1-LS and V2-LS:** '0' = disable; '1' = enable. When enabled, the upper 24 bits of address are the same as the previous PCI address. By only allowing the transfer of the lower eight bits of address, a saving of at least one PCI clock is achieved.
15:4	Reserved

4.2.12 Clock Skew Adjust Register (CSA)

Index: 11CH

Bit	Description	Name	Reset State
0	L2CLK Skew Adjust [0]	L2CK_SKW_ADJ0	'0'
1	L2CLK Skew Adjust [1]	L2CK_SKW_ADJ1	'0'
2	L2CLK Skew Adjust [2]	L2CK_SKW_ADJ2	'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
2:0	**L2CLK Skew Adjust [2:0]:** These bits are used to adjust the clock skew of L2CLK relative to the V1-LS core clock

Bit [2:0]	Delay
'000'	0.0 ns
'001'	+0.55 ns
'010'	+1.10 ns
'011'	+1.65 ns
'100'	-2.20 ns
'101'	-1.65 ns
'110'	-1.10 ns
'111'	-0.55 ns

15:3	Reserved

4.2.13 Bus Master and Snooping Control Register (SNOOPCTRL)

Index: 11DH

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Reserved		'0'
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Early DRAM Cycle When PCI Master is Accessing DRAM	DISPCIM_ELY_DRM_CY	'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
12:0	Reserved
13	**Early DRAM Cycle When PCI Master is Accessing DRAM:** '0' = enable; '1' = disable.
15:14	Reserved

4.2.14 Arbiter Control Register (ARBCTRL)

Index: 11EH

Bit	Description	Name	Reset State
0	Disable Preemptability of PCI Request/Grant [0]	DIS_REQGNT0	'0'
1	Disable Preemptability of PCI Request/Grant [1]	DIS_REQGNT1	'0'
2	Disable Preemptability of PCI Request/Grant [2]	DIS_REQGNT2	'0'
3	Disable Preemptability of PCI Request/Grant [3]	DIS_REQGNT3	'0'
4	SIO Request/Grant Source [0]	SIOREQGNT0	'0'
5	SIO Request/Grant Source [1]	SIOREQGNT1	'0'
6	Enable REQ2# as FLOAT_REQ# and GNT2# as FLOAT_GNT#	FLOAT_REQ_GNT	'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Disable Preemptability of PCI Request/Grant 0:** '0' = preemptable; '1' = non-preemptable.
1	**Disable Preemptability of PCI Request/Grant 1:** '0' = preemptable; '1' = non-preemptable.
2	**Disable Preemptability of PCI Request/Grant 2:** '0' = preemptable; '1' = non-preemptable.
3	**Disable Preemptability of PCI Request/Grant 3:** '0' = preemptable; '1' = non-preemptable.
5:4	**SIO Request/Grant Source [1:0]:** These bits must be set to '01' for normal operation. **Bit [1:0]** — **SIO Request/Grant Source** '00' — None '01' — From BSER interface '10' — Reserved '11' — Reserved
6	**Enable REQ2# as FLOAT_REQ# and GNT2# as FLOAT_GNT#:** '0' = disable; '1' = enable.
15:7	Reserved

4.2.15 Docking Control Register (DOCKC)

Index: 11FH

Bit	Description	Name	Reset State
0	Tristate DOCK_PCIRST# and DOCK_PCICLK	TS_DOCK_SIGS	'0'
1	Reserved		'0'
2	Deassert DOCK_PCIRST#	DOCKRST_DASRT	'0'
3	Enable DOCK_PCICLK to Toggle	DOCK_CLK_EN	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	System Docked Indication	DOCKED	'0'

Bit	Description
0	**Tristate DOCK_PCIRST# and DOCK_PCICLK in Normal Operating Mode:** '0' = drive out DOCK_PCIRST# and DOCK_PCICLK; '1' = tristate DOCK_PCIRST# and DOCK_PCICLK.
1	Reserved
2	**Deassert DOCK_PCIRST#:** '0' = assert DOCK_PCIRST# in a low state; '1' = DOCK_PCIRST# will follow the state of PCIRST#.
3	**Enable DOCK_PCICLK to Toggle:** '0' = force DOCK_PCICLK low; '1' = DOCK_PCICLK will follow the state of PCICLK.
14:4	Reserved
15	**System Docked Indication:** This bit is used when the PCI floating method is used; it is set to '1' by SMI handler when the system is docked. This bit will be reset to '0' when it is previously set to '1' and FLOAT_REQ# is deasserted to indicate the completion of the undock procedure.

4.3 DRAM Registers

4.3.1 Shadow RAM Read Enable Control Register (SHADRC)

Index: 200H

Bit	Description	Name	Reset State
0	Local Memory Read Enable [0]	LMEMRDEN0	'0'
1	Local Memory Read Enable [1]	LMEMRDEN1	'0'
2	Local Memory Read Enable [2]	LMEMRDEN2	'0'
3	Local Memory Read Enable [3]	LMEMRDEN3	'0'
4	Local Memory Read Enable [4]	LMEMRDEN4	'0'
5	Local Memory Read Enable [5]	LMEMRDEN5	'0'
6	Local Memory Read Enable [6]	LMEMRDEN6	'0'
7	Local Memory Read Enable [7]	LMEMRDEN7	'0'
8	Local Memory Read Enable [8]	LMEMRDEN8	'0'
9	Local Memory Read Enable [9]	LMEMRDEN9	'0'
10	Local Memory Read Enable [10]	LMEMRDEN10	'0'
11	Local Memory Read Enable [11]	LMEMRDEN11	'0'
12	Local Memory Read Enable [12]	LMEMRDEN12	'0'
13	Local Memory Read Enable [13]	LMEMRDEN13	'0'
14	Local Memory Read Enable [14]	LMEMRDEN14	'0'
15	Local Memory Read Enable [15]	LMEMRDEN15	'0'

Bit	Description
0	**Local Memory C0000H-C3FFFH Read Enable:** '0' = disable; '1' = enable.
1	**Local Memory C4000H-C7FFFH Read Enable:** '0' = disable; '1' = enable.
2	**Local Memory C8000H-CBFFFH Read Enable:** '0' = disable; '1' = enable.
3	**Local Memory CC000H-CFFFFH Read Enable: '** 0' = disable; '1' = enable.
4	**Local Memory D0000H-D3FFFH Read Enable:** '0' = disable; '1' = enable.
5	**Local Memory D4000H-D7FFFH Read Enable:** '0' = disable; '1' = enable.
6	**Local Memory D8000H-DBFFFH Read Enable:** '0' = disable; '1' = enable.
7	**Local Memory DC000H-DFFFFH Read Enable:** '0' = disable; '1' = enable.
8	**Local Memory E0000H-E3FFFH Read Enable:** '0' = disable; '1' = enable.
9	**Local Memory E4000H-E7FFFH Read Enable:** '0' = disable; '1' = enable.
10	**Local Memory E8000H-EBFFFH Read Enable:** '0' = disable; '1' = enable.
11	**Local Memory EC000H-EFFFFH Read Enable:** '0' = disable; '1' = enable.

Bit	Description *(cont.)*
12	**Local Memory F0000H-F3FFFH Read Enable:** '0' = disable; '1' = enable.
13	**Local Memory F4000H-F7FFFH Read Enable:** '0' = disable; '1' = enable.
14	**Local Memory F8000H-FBFFFH Read Enable:** '0' = disable; '1' = enable.
15	**Local Memory FC000H-FFFFFH Read Enable:** '0' = disable; '1' = enable.

4.3.2 Shadow RAM Write Enable Control Register (SHADWC)

Index: 201H

Bit	Description	Name	Reset State
0	Local Memory Write Enable [0]	LMEMWREN0	'0'
1	Local Memory Write Enable [1]	LMEMWREN1	'0'
2	Local Memory Write Enable [2]	LMEMWREN2	'0'
3	Local Memory Write Enable [3]	LMEMWREN3	'0'
4	Local Memory Write Enable [4]	LMEMWREN4	'0'
5	Local Memory Write Enable [5]	LMEMWREN5	'0'
6	Local Memory Write Enable [6]	LMEMWREN6	'0'
7	Local Memory Write Enable [7]	LMEMWREN7	'0'
8	Local Memory Write Enable [8]	LMEMWREN8	'0'
9	Local Memory Write Enable [9]	LMEMWREN9	'0'
10	Local Memory Write Enable [10]	LMEMWREN10	'0'
11	Local Memory Write Enable [11]	LMEMWREN11	'0'
12	Local Memory Write Enable [12]	LMEMWREN12	'0'
13	Local Memory Write Enable [13]	LMEMWREN13	'0'
14	Local Memory Write Enable [14]	LMEMWREN14	'0'
15	Local Memory Write Enable [15]	LMEMWREN15	'0'

Bit	Description
0	**Local Memory C0000H-C3FFFH Write Enable:** '0' = disable; '1' = enable.
1	**Local Memory C4000H-C7FFFH Write Enable:** '0' = disable; '1' = enable.
2	**Local Memory C8000H-CBFFFH Write Enable:** '0' = disable; '1' = enable.
3	**Local Memory CC000H-CFFFFH Write Enable:** '0' = disable; '1' = enable.
4	**Local Memory D0000H-D3FFFH Write Enable:** '0' = disable; '1' = enable.
5	**Local Memory D4000H-D7FFFH Write Enable: '** 0' = disable; '1' = enable.
6	**Local Memory D8000H-DBFFFH Write Enable:** '0' = disable; '1' = enable.
7	**Local Memory DC000H-DFFFFH Write Enable:** '0' = disable; '1' = enable.
8	**Local Memory E0000H-E3FFFH Write Enable:** '0' = disable; '1' = enable.
9	**Local Memory E4000H-E7FFFH Write Enable:** '0' = disable; '1' = enable.
10	**Local Memory E8000H-EBFFFH Write Enable:** '0' = disable; '1' = enable.
11	**Local Memory EC000H-EFFFFH Write Enable:** '0' = disable; '1' = enable.
12	**Local Memory F0000H-F3FFFH Write Enable:** '0' = disable; '1' = enable.

Bit	Description *(cont.)*
13	**Local Memory F4000H-F7FFFH Write Enable:** '0' = disable; '1' = enable.
14	**Local Memory F8000H-FBFFFH Write Enable:** '0' = disable; '1' = enable.
15	**Local Memory FC000H-FFFFFH Write Enable:** '0' = disable; '1' = enable.

4.3.3 Bank 0 Control Register (B0C)

Index: 202H

Bit	Description	Name	Reset State
0	Bank 0 Starting Address [20]	B0A20	'0'
1	Bank 0 Starting Address [21]	B0A21	'0'
2	Bank 0 Starting Address [22]	B0A22	'0'
3	Bank 0 Starting Address [23]	B0A23	'0'
4	Bank 0 Starting Address [24]	B0A24	'0'
5	Bank 0 Starting Address [25]	B0A25	'0'
6	Bank 0 Starting Address [26]	B0A26	'0'
7	Bank 0 Starting Address [27]	B0A27	'0'
8	Reserved		'0'
9	Bank 0 DRAM Size [0]	B0S0	'0'
10	Bank 0 DRAM Size [1]	B0S1	'0'
11	Bank 0 DRAM Size [2]	B0S2	'0'
12	Column Address Bits for Bank 0 [0]	COLADR00	'0'
13	Column Address Bits for Bank 0 [1]	COLADR01	'0'
14	Column Address Bits for Bank 0 [2]	COLADR02	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 0 Starting Address [27:20]:** Starting address of bank 0.
8	Reserved
11:9	**Bank 0 DRAM Size [2:0]:** **Bit [2:0]** — **DRAM Bank Size** '000' — 1 Mbyte '001' — 2 Mbyte '010' — 4 Mbyte '011' — 8 Mbyte '100' — 16 Mbyte '101' — 32 Mbyte '110' — 64 Mbyte '111' — Reserved
14:12	**Number of Column Address Bits for Bank 0 [2:0]:** **Bit [2:0]** — **Column Address** '000' — 8 bits '001' — 9 bits '010' — 10 bits '011' — 11 bits '100' — 12 bits All others — Reserved
15	Reserved

4.3.4 Bank 1 Control Register (B1C)

Index: 203H

Bit	Description	Name	Reset State
0	Bank 1 Starting Address [20]	B1A20	'0'
1	Bank 1 Starting Address [21]	B1A21	'0'
2	Bank 1 Starting Address [22]	B1A22	'0'
3	Bank 1 Starting Address [23]	B1A23	'0'
4	Bank 1 Starting Address [24]	B1A24	'0'
5	Bank 1 Starting Address [25]	B1A25	'0'
6	Bank 1 Starting Address [26]	B1A26	'0'
7	Bank 1 Starting Address [27]	B1A27	'0'
8	Reserved		'0'
9	Bank 1 DRAM Size [0]	B1S0	'0'
10	Bank 1 DRAM Size [1]	B1S1	'0'
11	Bank 1 DRAM Size [2]	B1S2	'0'
12	Column Address Bits for Bank 1 [0]	COLADR10	'0'
13	Column Address Bits for Bank 1 [1]	COLADR11	'0'
14	Column Address Bits for Bank 1 [2]	COLADR12	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 1 Starting Address [27:20]:** Starting address of bank 1.
8	Reserved
11:9	**Bank 1 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12 **Number of Column Address Bits for Bank 1 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15 Reserved

4.3.5 Bank 0/1 Timing Control Register (B01TC)

Index: 204H

Bit	Description	Name	Reset State
0	Bank 0 and Bank 1 RAS Precharge Time [0]	B01_TRP0	'1'
1	Bank 0 and Bank 1 RAS Precharge Time [1]	B01_TRP1	'1'
2	Bank 0 and Bank 1 RAS Precharge Time [2]	B01_TRP2	'1'
3	Bank 0 and Bank 1 RAS Address Hold Time [0]	B01_TRAH0	'1'
4	Bank 0 and Bank 1 RAS Address Hold Time [1]	B01_TRAH1	'1'
5	Bank 0 and Bank 1 CAS Address Setup Time [0]	B01_TASC0	'1'
6	Bank 0 and Bank 1 CAS Address Setup Time [1]	B01_TASC1	'1'
7	Bank 0 and Bank 1 CAS Address Hold Time	B01_TCAH	'1'
8	Bank 0 and Bank 1 CAS Precharge Time	B01_TCP	'1'
9	Bank 0 and Bank 1 CAS Read Pulse Width [0]	B01_TCAS_RD0	'1'
10	Bank 0 and Bank 1 CAS Read Pulse Width [1]	B01_TCAS_RD1	'1'
11	Bank 0 and Bank 1 CAS Read Pulse Width [2]	B01_TCAS_RD2	'1'
12	Bank 0 and Bank 1 CAS Write Pulse Width [0]	B01_TCAS_WR0	'1'
13	Bank 0 and Bank 1 CAS Write Pulse Width [1]	B01_TCAS_WR1	'1'
14	Reserved		'1'
15	Reserved		'1'

Bit **Description**

2:0 **Bank 0 and Bank 1 RAS Precharge Time [2:0]:**

Bit [2:0]	Precharge Time
'000'	1.5T
'001'	2.0T
'010'	2.5T
'011'	3.0T
'100'	3.5T
'101'	4.0T
'110'	4.5T
'111'	5.0T

4:3 **Bank 0 and Bank 1 RAS Address Hold Time [1:0]:**

Bit [1:0]	Address Hold Time
'00'	0.5T
'01'	1.0T
'10'	1.5T
'11'	2.0T

6:5 **Bank 0 and Bank 1 CAS Address Setup Time [1:0]:**

Bit [1:0]	Address Setup Time
'00'	0.0T
'01'	0.5T
'10'	1.0T
'11'	1.5T

Bit	Description *(cont.)*
7	**Bank 0 and Bank 1 CAS Address Hold Time:** '0' = 0.5T; '1' = 1.0T.
8	**Bank 0 and Bank 1 CAS Precharge** : '0' = 0.5T; '1' = 1.0T.
11:9	**Bank 0 and Bank 1 CAS Read Pulse Width [2:0]:**

Bit [2:0]	Read Pulse Width
'000'	0.5T (EDO or Burst EDO only)
'001'	1.0T
'010'	1.5T
'011'	2.0T
'100'	2.5T
'101'	3.0T
'110'	3.5T
'111'	4.0T

13:12	**Bank 0 and Bank 1 CAS Write Pulse Width [1:0]:**

Bit [1:0]	Write Pulse Width
'00'	0.5T (EDO or Burst EDO only)
'01'	1.0T
'10'	1.5T
'11'	2.0T

15:14	Reserved

4.3.6 Bank 2 Control Register (B2C)

Index: 205H

Bit	Description	Name	Reset State
0	Bank 2 Starting Address [20]	B2A20	'0'
1	Bank 2 Starting Address [21]	B2A21	'0'
2	Bank 2 Starting Address [22]	B2A22	'0'
3	Bank 2 Starting Address [23]	B2A23	'0'
4	Bank 2 Starting Address [24]	B2A24	'0'
5	Bank 2 Starting Address [25]	B2A25	'0'
6	Bank 2 Starting Address [26]	B2A26	'0'
7	Bank 2 Starting Address [27]	B2A27	'0'
8	Reserved		'0'
9	Bank 2 DRAM Size [0]	B2S0	'0'
10	Bank 2 DRAM Size [1]	B2S1	'0'
11	Bank 2 DRAM Size [2]	B2S2	'0'
12	Column Address Bits for Bank 2 [0]	COLADR20	'0'
13	Column Address Bits for Bank 2 [1]	COLADR21	'0'
14	Column Address Bits for Bank 2 [2]	COLADR22	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 2 Starting Address [27:20]:** Starting address of bank 2.
8	Reserved
11:9	**Bank 2 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12	**Number of Column Address Bits for Bank 2 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15	Reserved

4.3.7 Bank 3 Control Register (B3C)

Index: 206H

Bit	Description	Name	Reset State
0	Bank 3 Starting Address [20]	B3A20	'0'
1	Bank 3 Starting Address [21]	B3A21	'0'
2	Bank 3 Starting Address [22]	B3A22	'0'
3	Bank 3 Starting Address [23]	B3A23	'0'
4	Bank 3 Starting Address [24]	B3A24	'0'
5	Bank 3 Starting Address [25]	B3A25	'0'
6	Bank 3 Starting Address [26]	B3A26	'0'
7	Bank 3 Starting Address [27]	B3A27	'0'
8	Reserved		'0'
9	Bank 3 DRAM Size [0]	B3S0	'0'
10	Bank 3 DRAM Size [1]	B3S1	'0'
11	Bank 3 DRAM Size [2]	B3S2	'0'
12	Column Address Bits for Bank 3 [0]	COLADR30	'0'
13	Column Address Bits for Bank 3 [1]	COLADR31	'0'
14	Column Address Bits for Bank 3 [2]	COLADR32	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 3 Starting Address [27:20]:** Starting address of bank 3.
8	Reserved
11:9	**Bank 3 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12	**Number of Column Address Bits for Bank 3 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15	Reserved

4.3.8 Bank 2/3 Timing Control Register (B23TC)

Index: 207H

Bit	Description	Name	Reset State
0	Bank 2 and Bank 3 RAS Precharge Time [0]	B23_TRP0	'1'
1	Bank 2 and Bank 3 RAS Precharge Time [1]	B23_TRP1	'1'
2	Bank 2 and Bank 3 RAS Precharge Time [2]	B23_TRP2	'1'
3	Bank 2 and Bank 3 RAS Address Hold Time [0]	B23_TRAH0	'1'
4	Bank 2 and Bank 3 RAS Address Hold Time [1]	B23_TRAH1	'1'
5	Bank 2 and Bank 3 CAS Address Setup Time [0]	B23_TASC0	'1'
6	Bank 2 and Bank 3 CAS Address Setup Time [1]	B23_TASC1	'1'
7	Bank 2 and Bank 3 CAS Address Hold Time	B23_TCAH	'1'
8	Bank 2 and Bank 3 CAS Precharge Time	B23_TCP	'1'
9	Bank 2 and Bank 3 CAS Read Pulse Width [0]	B23_TCAS_RD0	'1'
10	Bank 2 and Bank 3 CAS Read Pulse Width [1]	B23_TCAS_RD1	'1'
11	Bank 2 and Bank 3 CAS Read Pulse Width [2]	B23_TCAS_RD2	'1'
12	Bank 2 and Bank 3 CAS Write Pulse Width [0]	B23_TCAS_WR0	'1'
13	Bank 2 and Bank 3 CAS Write Pulse Width [1]	B23_TCAS_WR1	'1'
14	Reserved		'1'
15	Reserved		'1'

Bit **Description**

2:0 **Bank 2 and Bank 3 RAS Precharge Time [2:0]:**

Bit [2:0]	Precharge Time
'000'	1.5T
'001'	2.0T
'010'	2.5T
'011'	3.0T
'100'	3.5T
'101'	4.0T
'110'	4.5T
'111'	5.0T

4:3 **Bank 2 and Bank 3 RAS Address Hold Time [1:0]:**

Bit [1:0]	Address Hold Time
'00'	0.5T
'01'	1.0T
'10'	1.5T
'11'	2.0T

6:5 **Bank 2 and Bank 3 CAS Address Setup Time [1:0]:**

Bit [1:0]	Address Setup Time
'00'	0.0T
'01'	0.5T
'10'	1.0T
'11'	1.5T

Bit	Description *(cont.)*
7	**Bank 2 and Bank 3 CAS Address Hold Time:** '0' = 0.5T; '1' = 1.0T.
8	**Bank 2 and Bank 3 CAS Precharge:** '0' = 0.5T; '1' = 1.0T.
11:9	**Bank 2 and Bank 3 CAS Read Pulse Width [2:0]:**

Bit [2:0]	Read Pulse Width
'000'	0.5T (EDO or Burst EDO only)
'001'	1.0T
'010'	1.5T
'011'	2.0T
'100'	2.5T
'101'	3.0T
'110'	3.5T
'111'	4.0T

13:12	**Bank 2 and Bank 3 CAS Write Pulse Width [1:0]:**

Bit [1:0]	Write Pulse Width
'00'	0.5T (EDO or Burst EDO only)
'01'	1.0T
'10'	1.5T
'11'	2.0T

15:14	Reserved

4.3.9 Bank 4 Control Register (B4C)

Index: 208H

Bit	Description	Name	Reset State
0	Bank 4 Starting Address [20]	B4A20	'0'
1	Bank 4 Starting Address [21]	B4A21	'0'
2	Bank 4 Starting Address [22]	B4A22	'0'
3	Bank 4 Starting Address [23]	B4A23	'0'
4	Bank 4 Starting Address [24]	B4A24	'0'
5	Bank 4 Starting Address [25]	B4A25	'0'
6	Bank 4 Starting Address [26]	B4A26	'0'
7	Bank 4 Starting Address [27]	B4A27	'0'
8	Reserved		'0'
9	Bank 4 DRAM Size [0]	B4S0	'0'
10	Bank 4 DRAM Size [1]	B4S1	'0'
11	Bank 4 DRAM Size [2]	B4S2	'0'
12	Column Address Bits for Bank 4 [0]	COLADR40	'0'
13	Column Address Bits for Bank 4 [1]	COLADR41	'0'
14	Column Address Bits for Bank 4 [2]	COLADR42	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 4 Starting Address [27:20]:** Starting address of bank 4.
8	Reserved
11:9	**Bank 4 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12 **Number of Column Address Bits for Bank 4 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15 Reserved

4.3.10 Bank 5 Control Register (B5C)

Index: 209H

Bit	Description	Name	Reset State
0	Bank 5 Starting Address [20]	B5A20	'0'
1	Bank 5 Starting Address [21]	B5A21	'0'
2	Bank 5 Starting Address [22]	B5A22	'0'
3	Bank 5 Starting Address [23]	B5A23	'0'
4	Bank 5 Starting Address [24]	B5A24	'0'
5	Bank 5 Starting Address [25]	B5A25	'0'
6	Bank 5 Starting Address [26]	B5A26	'0'
7	Bank 5 Starting Address [27]	B5A27	'0'
8	Reserved		'0'
9	Bank 5 DRAM Size [0]	B5S0	'0'
10	Bank 5 DRAM Size [1]	B5S1	'0'
11	Bank 5 DRAM Size [2]	B5S2	'0'
12	Column Address Bits for Bank 5 [0]	COLADR50	'0'
13	Column Address Bits for Bank 5 [1]	COLADR51	'0'
14	Column Address Bits for Bank 5 [2]	COLADR52	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 5 Starting Address [27:20]:** Starting address of bank 5.
8	Reserved
11:9	**Bank 5 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12 **Number of Column Address Bits for Bank 5 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15 Reserved

4.3.11 Bank 4/5 Control Register (B45TC)

Index: 20AH

Bit	Description	Name	Reset State
0	Bank 4 and Bank 5 RAS Precharge Time [0]	B45_TRP0	'1'
1	Bank 4 and Bank 5 RAS Precharge Time [1]	B45_TRP1	'1'
2	Bank 4 and Bank 5 RAS Precharge Time [2]	B45_TRP2	'1'
3	Bank 4 and Bank 5 RAS Address Hold Time [0]	B45_TRAH0	'1'
4	Bank 4 and Bank 5 RAS Address Hold Time [1]	B45_TRAH1	'1'
5	Bank 4 and Bank 5 CAS Address Setup Time [0]	B45_TASC0	'1'
6	Bank 4 and Bank 5 CAS Address Setup Time [1]	B45_TASC1	'1'
7	Bank 4 and Bank 5 CAS Address Hold Time	B45_TCAH	'1'
8	Bank 4 and Bank 5 CAS Precharge Time	B45_TCP	'1'
9	Bank 4 and Bank 5 CAS Read Pulse Width [0]	B45_TCAS_RD0	'1'
10	Bank 4 and Bank 5 CAS Read Pulse Width [1]	B45_TCAS_RD1	'1'
11	Bank 4 and Bank 5 CAS Read Pulse Width [2]	B45_TCAS_RD2	'1'
12	Bank 4 and Bank 5 CAS Write Pulse Width [0]	B45_TCAS_WR0	'1'
13	Bank 4 and Bank 5 CAS Write Pulse Width [1]	B45_TCAS_WR1	'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
2:0	**Bank 4 and Bank 5 RAS Precharge Time [2:0]:**

Bit [2:0]	Precharge Time
'000'	1.5T
'001'	2.0T
'010'	2.5T
'011'	3.0T
'100'	3.5T
'101'	4.0T
'110'	4.5T
'111'	5.0T

4:3 **Bank 4 and Bank 5 RAS Address Hold Time [1:0]:**

Bit [1:0]	Address Hold Time
'00'	0.5T
'01'	1.0T
'10'	1.5T
'11'	2.0T

6:5 **Bank 4 and Bank 5 CAS Address Setup Time [1:0]:**

Bit [1:0]	Address Setup Time
'00'	0.0T
'01'	0.5T
'10'	1.0T
'11'	1.5T

Bit	Description *(cont.)*
7	**Bank 4 and Bank 5 CAS Address Hold Time:** '0' = 0.5T; '1' = 1.0T.
8	**Bank 4 and Bank 5 CAS precharge:** '0' = 0.5T; '1' = 1.0T.
11:9	**Bank 4 and Bank 5 CAS Read Pulse Width [2:0]:** **Bit [2:0]** — **Read Pulse Width** '000' — 0.5T (EDO or Burst EDO only) '001' — 1.0T '010' — 1.5T '011' — 2.0T '100' — 2.5T '101' — 3.0T '110' — 3.5T '111' — 4.0T
13:12	**Bank 4 and Bank 5 CAS Write Pulse Width [1:0]:** **Bit [1:0]** — **Write Pulse Width** '00' — 0.5T (EDO or Burst EDO only) '01' — 1.0T '10' — 1.5T '11' — 2.0T
15:14	Reserved

4.3.12 Bank 6 Control Register (B6C)

Index: 20BH

Bit	Description	Name	Reset State
0	Bank 6 Starting Address [20]	B6A20	'0'
1	Bank 6 Starting Address [21]	B6A21	'0'
2	Bank 6 Starting Address [22]	B6A22	'0'
3	Bank 6 Starting Address [23]	B6A23	'0'
4	Bank 6 Starting Address [24]	B6A24	'0'
5	Bank 6 Starting Address [25]	B6A25	'0'
6	Bank 6 Starting Address [26]	B6A26	'0'
7	Bank 6 Starting Address [27]	B6A27	'0'
8	Reserved		'0'
9	Bank 6 DRAM Size [0]	B6S0	'0'
10	Bank 6 DRAM Size [1]	B6S1	'0'
11	Bank 6 DRAM Size [2]	B6S2	'0'
12	Column Address Bits for Bank 6 [0]	COLADR60	'0'
13	Column Address Bits for Bank 6 [1]	COLADR61	'0'
14	Column Address Bits for Bank 6 [2]	COLADR62	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 6 Starting Address [27:20]:** Starting address of bank 6.
8	Reserved
11:9	**Bank 6 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12	**Number of Column Address Bits for Bank 6 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15	Reserved

4.3.13 Bank 7 Control Register (B7C)

Index: 20CH

Bit	Description	Name	Reset State
0	Bank 7 Starting Address [20]	B7A20	'0'
1	Bank 7 Starting Address [21]	B7A21	'0'
2	Bank 7 Starting Address [22]	B7A22	'0'
3	Bank 7 Starting Address [23]	B7A23	'0'
4	Bank 7 Starting Address [24]	B7A24	'0'
5	Bank 7 Starting Address [25]	B7A25	'0'
6	Bank 7 Starting Address [26]	B7A26	'0'
7	Bank 7 Starting Address [27]	B7A27	'0'
8	Reserved		'0'
9	Bank 7 DRAM Size [0]	B7S0	'0'
10	Bank 7 DRAM Size [1]	B7S1	'0'
11	Bank 7 DRAM Size [2]	B7S2	'0'
12	Column Address Bits for Bank 7 [0]	COLADR70	'0'
13	Column Address Bits for Bank 7 [1]	COLADR71	'0'
14	Column Address Bits for Bank 7 [2]	COLADR72	'0'
15	Reserved		'0'

Bit	Description
7:0	**Bank 7 Starting Address [27:20]:** Starting address of bank 7.
8	Reserved
11:9	**Bank 7 DRAM Size [2:0]:**

Bit [2:0]	DRAM Bank Size
'000'	1 Mbyte
'001'	2 Mbyte
'010'	4 Mbyte
'011'	8 Mbyte
'100'	16 Mbyte
'101'	32 Mbyte
'110'	64 Mbyte
'111'	Reserved

14:12	**Number of Column Address Bits for Bank 7 [2:0]:**

Bit [2:0]	Column Address
'000'	8 bits
'001'	9 bits
'010'	10 bits
'011'	11 bits
'100'	12 bits
All others	Reserved

15	Reserved

4.3.14 Bank 6/7 Timing Control Register (B67TC)

Index: 20DH

Bit	Description	Name	Reset State
0	Bank 6 and Bank 7 RAS Precharge Time [0]	B67_TRP0	'1'
1	Bank 6 and Bank 7 RAS Precharge Time [1]	B67_TRP1	'1'
2	Bank 6 and Bank 7 RAS Precharge Time [2]	B67_TRP2	'1'
3	Bank 6 and Bank 7 RAS Address Hold Time [0]	B67_TRAH0	'1'
4	Bank 6 and Bank 7 RAS Address Hold Time [1]	B67_TRAH1	'1'
5	Bank 6 and Bank 7 CAS Address Setup Time [0]	B67_TASC0	'1'
6	Bank 6 and Bank 7 CAS Address Setup Time [1]	B67_TASC1	'1'
7	Bank 6 and Bank 7 CAS Address Hold Time	B67_TCAH	'1'
8	Bank 6 and Bank 7 CAS Precharge Time	B67_TCP	'1'
9	Bank 6 and Bank 7 CAS Read Pulse Width [0]	B67_TCAS_RD0	'1'
10	Bank 6 and Bank 7 CAS Read Pulse Width [1]	B67_TCAS_RD1	'1'
11	Bank 6 and Bank 7 CAS Read Pulse Width [2]	B67_TCAS_RD2	'1'
12	Bank 6 and Bank 7 CAS Write Pulse Width [0]	B67_TCAS_WR0	'1'
13	Bank 6 and Bank 7 CAS Write Pulse Width [1]	B67_TCAS_WR1	'1'
14	Reserved		'1'
15	Reserved		'1'

Bit **Description**

2:0 **Bank 6 and Bank 7 RAS Precharge Time [2:0]:**

Bit [2:0]	Precharge Time
'000'	1.5T
'001'	2.0T
'010'	2.5T
'011'	3.0T
'100'	3.5T
'101'	4.0T
'110'	4.5T
'111'	5.0T

4:3 **Bank 6 and Bank 7 RAS Address Hold Time [1:0]:**

Bit [1:0]	Address Hold Time
'00'	0.5T
'01'	1.0T
'10'	1.5T
'11'	2.0T

6:5 **Bank 6 and Bank 7 CAS Address Setup Time [1:0]:**

Bit [1:0]	Address Setup Time
'00'	0.0T
'01'	0.5T
'10'	1.0T
'11'	1.5T

Bit	Description *(cont.)*
7	**Bank 6 and Bank 7 CAS Address Hold Time:** '0' = 0.5T; '1' = 1.0T.
8	**Bank 6 and Bank 7 CAS Precharge:** '0' = 0.5T; '1' = 1.0T.
11:9	**Bank 6 and Bank 7 CAS Read Pulse Width [2:0]:** **Bit [2:0]** — **Read Pulse Width** '000' — 0.5T (EDO or Burst EDOt only) '001' — 1.0T '010' — 1.5T '011' — 2.0T '100' — 2.5T '101' — 3.0T '110' — 3.5T '111' — 4.0T
13:12	**Bank 6 and Bank 7 CAS Write Pulse Width [1:0]:** **Bit [1:0]** — **Write Pulse Width** '00' — 0.5T (EDO or Burst EDO only) '01' — 1.0T '10' — 1.5T '11' — 2.0T
15:14	Reserved

4.3.15 DRAM Configuration Register 1(DCONF1)

Index: 20EH

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Reserved		'0'
2	Reserved		'0'
3	DRAM Inactive Time-out [0]	DRAM_INAT_TO0	'0'
4	DRAM Inactive Time-out [1]	DRAM_INAT_TO1	'0'
5	DRAM Inactive Time-out [2]	DRAM_INAT_TO2	'0'
6	DRAM Auto-Detect Mode [0]	DRAM_AUTODET0	'0'
7	DRAM Auto-Detect Mode [1]	DRAM_AUTODET1	'0'
8	Fast Cacheless Read Enable	FSTL2DISRDEN	'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit — **Description**

2:0 — Reserved

5:3 — **DRAM Inactive Time-out [2:0]:**

Bit [2:0]	Duration (T = CPU Bus Clock Frequency)
'000'	Never
'001'	8 T
'010'	32 T
'011'	128 T
'100'	512 T
'101'	Reserved
'110'	Reserved
'111'	Immediate

7:6 — **DRAM Auto-Detect Mode [1:0]:**

Bit [1:0]	Function
'00'	Normal mode
'01'	Setup for Auto-Detect. Set before auto-detect algorithm.
'10'	Reserved
'11'	Auto-Detect read mode

8 — **Fast Cacheless Read Enable:** '0' = fast cacheless read is disabled; '1' = fast cacheless read feature is enabled.

NOTE: L2 cache must be disabled and L2 read lead-off must be set to 2T.

15:9 — Reserved

4.3.16 DRAM Configuration Register 2 (DCONF2)

Index: 20FH

Bit	Description	Name	Reset State
0	Bank 0 Enable	BANK0_32EN	'1'
1	Bank 1 Enable	BANK1_32EN	'0'
2	Bank 2 Enable	BANK2_32EN	'0'
3	Bank 3 Enable	BANK3_32EN	'0'
4	Bank 4 Enable	BANK4_32EN	'0'
5	Bank 5 Enable	BANK5_32EN	'0'
6	Bank 6 Enable	BANK6_32EN	'0'
7	Bank 7 Enable	BANK7_32EN	'0'
8	Bank 0 and Bank 1 as a 64-bit Bank	BANK01_64EN	'0'
9	Bank 2 and Bank 3 as a 64-bit Bank	BANK23_64EN	'0'
10	Bank 4 and Bank 5 as a 64-bit Bank	BANK45_64EN	'0'
11	Bank 6 and Bank 7 as a 64-bit Bank	BANK67_64EN	'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Bank 0 Enable:** '0' = disable; '1' = enable. When enabled, bank 0 will operate as a 32-bit bank.
1	**Bank 1 Enable:** '0' = disable; '1' = enable. When enabled, bank 1 will operate as a 32-bit bank.
2	**Bank 2 Enable:** '0' = disable; '1' = enable. When enabled, bank 2 will operate as a 32-bit bank.
3	**Bank 3 Enable:** '0' = disable; '1' = enable. When enabled, bank 3 will operate as a 32-bit bank.
4	**Bank 4 Enable:** '0' = disable; '1' = enable . When enabled, bank 4 will operate as a 32-bit bank.
5	**Bank 5 Enable:** '0' = disable; '1' = enable . When enabled, bank 5 will operate as a 32-bit bank.
6	**Bank 6 Enable:** 0 = disable; '1' = enable. When enabled, bank 6 will operate as a 32-bit bank.
7	**Bank 7 Enable:** '0' = disable; '1' = enable. When enabled, bank 7 will operate as a 32-bit bank.

Bit	Description *(cont.)*
8	**Bank 0 and Bank 1 as a 64-bit Bank:** '0' = two 32-bit banks; '1' = one 64-bit bank. When enabled: (a) bank 0 and bank 1 will be used as a single 64-bit bank, (b) bit [1:0] above will be ignored, (c) all DRAM parameters will be from bank 0, and (d) the DRAM bank size programmed in bank 0 will be doubled.
9	**Bank 2 and Bank 3 as a 64-bit Bank:** '0' = two 32-bit banks; '1' = one 64-bit bank. When enabled: (a) bank 2 and bank 3 will be used as a single 64-bit bank, (b) bit [3:2] above will be ignored, (c) all DRAM parameters will be from bank 2, and (d) the DRAM bank size programmed in bank 2 will be doubled.
10	**Bank 4 and Bank 5 as a 64-bit Bank:** '0' = two 32-bit banks; '1' = one 64-bit bank. When enabled: (a) bank 4 and bank 5 will be used as a single 64-bit bank, (b) bit [5:4] above will be ignored, (c) all DRAM parameters will be from bank 4, and (d) the DRAM bank size programmed in bank 4 will be doubled.
11	**Bank 6 and Bank 7 as a 64-bit Bank:** '0' = two 32-bit banks; '1' = one 64-bit bank. When enabled: (a) bank 6 and bank 7 will be used as a single 64-bit bank, (b) bit [7:6] above will be ignored, (c) all DRAM parameters will be from bank 6, and (d) the DRAM bank size programmed in bank 6 will be doubled.
15:12	Reserved

4.3.17 DRAM Configuration Register 3 (DCONF3)

Index: 210H

Bit	Description	Name	Reset State
0	Bank 0 DRAM Type [0]	B0DRMTYPE0	'0'
1	Bank 0 DRAM Type [1]	B0DRMTYPE1	'0'
2	Bank 1 DRAM Type [0]	B1DRMTYPE0	'0'
3	Bank 1 DRAM Type [1]	B1DRMTYPE1	'0'
4	Bank 2 DRAM Type [0]	B2DRMTYPE0	'0'
5	Bank 2 DRAM Type [1]	B2DRMTYPE1	'0'
6	Bank 3 DRAM Type [0]	B3DRMTYPE0	'0'
7	Bank 3 DRAM Type [1]	B3DRMTYPE1	'0'
8	Bank 4 DRAM Type [0]	B4DRMTYPE0	'0'
9	Bank 4 DRAM Type [1]	B4DRMTYPE1	'0'
10	Bank 5 DRAM Type [0]	B5DRMTYPE0	'0'
11	Bank 5 DRAM Type [1]	B5DRMTYPE1	'0'
12	Bank 6 DRAM Type [0]	B6DRMTYPE0	'0'
13	Bank 6 DRAM Type [1]	B6DRMTYPE1	'0'
14	Bank 7 DRAM Type [0]	B7DRMTYPE0	'0'
15	Bank 7 DRAM Type [1]	B7DRMTYPE1	'0'

Bit	Description
1:0	**Bank 0 DRAM Type [1:0]:** **Bit [1:0]** — **DRAM Type** '00' — Standard '01' — EDO '10' — Burst EDO '11' — Reserved
3:2	**Bank 1 DRAM Type [1:0]:** **Bit [1:0]** — **DRAM Type** '00' — Standard '01' — EDO '10' — Burst EDO '11' — Reserved
5:4	**Bank 2 DRAM Type [1:0]:** **Bit [1:0]** — **DRAM Type** '00' — Standard '01' — EDO '10' — Burst EDO '11' — Reserved

Bit	Description *(cont.)*	
7:6	**Bank 3 DRAM Type [1:0]:**	
	Bit [1:0]	**DRAM Type**
	'00'	Standard
	'01'	EDO
	'10'	Burst EDO
	'11'	Reserved
9:8	**Bank 4 DRAM Type [1:0]:**	
	Bit [1:0]	**DRAM Type**
	'00'	Standard
	'01'	EDO
	'10'	Burst EDO
	'11'	Reserved
11:10	**Bank 5 DRAM Type [1:0]:**	
	Bit [1:0]	**DRAM Type**
	'00'	Standard
	'01'	EDO
	'10'	Burst EDO
	'11'	Reserved
13:12	**Bank 6 DRAM Type [1:0]:**	
	Bit [1:0]	**DRAM Type**
	'00'	Standard
	'01'	EDO
	'10'	Burst EDO
	'11'	Reserved
15:14	**Bank 7 DRAM Type [1:0]:**	
	Bit [1:0]	**DRAM Type**
	'00'	Standard
	'01'	EDO
	'10'	Burst EDO
	'11'	Reserved

4.3.18 DRAM Refresh Control Register (DRFSHC)

Index: 211H

Bit	Description	Name	Reset State
0	DRAM Refresh Scheme	DRAM_RF_NLYRF	'0'
1	RAS Precharge Time for Refresh Cycles [0]	RFRPRE0	'0'
2	RAS Precharge Time for Refresh Cycles [1]	RFRPRE1	'0'
3	RAS Pulse Width for Refresh Cycles [0]	RFRPW0	'0'
4	RAS Pulse Width for Refresh Cycles [1]	RFRPW1	'0'
5	Refresh Period [0]	REFRPRD0	'1'
6	Refresh Period [1]	REFRPRD1	'0'
7	Refresh Period [2]	REFRPRD2	'1'
8	Reserved		'0'
9	Reserved		'0'
10	Self-Refresh Enable	SLFREFEN	'0'
11	Reserved		'0'
12	Refresh Stagger Select [0]	REF_STAG_SEL0	'1'
13	Refresh Stagger Select [1]	REF_STAG_SEL1	'1'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**DRAM Refresh Scheme:** '0' = CAS-before-RAS refresh; '1' = RAS-only refresh.
2:1	**RAS Precharge Time for Refresh Cycles [1:0]:**

Bit [1:0]	RAS Precharge Time
'00'	5T
'01'	4T
'10'	3T
'11'	2T

Bit	Description
4:3	**RAS Pulse Width for Refresh Cycles [1:0]:**

Bit [1:0]	RAS Pulse Width Time
'00'	6T
'01'	5T
'10'	4T
'11'	3T

Bit	Description *(cont.)*
7:5	**Refresh Period:** These bits determine the refresh period for local DRAM. **Bit [2:0]** — **Refresh Period** '000' — 3.75 µs '001' — 7.5 µs '010' — 15 µs '011' — 30 µs '100' — 120 µs '101' — Stopped All Others — Reserved
9:8	Reserved
10	**Self-Refresh Enable:** When high, this bit enables self-refresh mode during Suspend Mode.
11	Reserved
13:12	**Refresh Stagger Select [1:0]:** **Bit [1:0]** — **Function** '00' — No staggering '01' — Reserved '10' — Stagger the active edge of RAS '11' — Stagger both edges of RAS
15:14	Reserved

4.3.19 Burst EDO Control Register (BEDOC)

Index: 212H

Bit	Description	Name	Reset State
0	Enable Burst EDO WCBR Configuration Cycle	ENWCBR_CONFIG	'0'
1	DRAM Bank Configuration Select [0]	BANK_CONGIG0	'0'
2	DRAM Bank Configuration Select [1]	BANK_CONGIG1	'0'
3	Trigger WCBR Configuration Cycle	TRIG_WCBR	
4	MA Setting During WCBR Cycle [0]	WCBR_MA0	'1'
5	MA Setting During WCBR Cycle [1]	WCBR_MA1	'0'
6	MA Setting During WCBR Cycle [2]	WCBR_MA2	'0'
7	MA Setting During WCBR Cycle [3]	WCBR_MA3	'0'
8	MA Setting During WCBR Cycle [4]	WCBR_MA4	'0'
9	MA Setting During WCBR Cycle [5]	WCBR_MA5	'1'
10	MA Setting During WCBR Cycle [6]	WCBR_MA6	'0'
11	MA Setting During WCBR Cycle [7]	WCBR_MA7	'0'
12	MA Setting During WCBR Cycle [8]	WCBR_MA8	'0'
13	MA Setting During WCBR Cycle [9]	WCBR_MA9	'0'
14	MA Setting During WCBR Cycle [10]	WCBR_MA10	'0'
15	MA Setting During WCBR Cycle [11]	WCBR_MA11	'0'

Bit — **Description**

0 — **Enable Burst EDO Write CAS-Before-RAS (WCBR) Configuration Cycle:** '0' = disable; '1' = enable.

2:1 — **DRAM Bank Configuration Select [1:0]:**

Bit [1:0]	DRAM Bank
'00'	Bank 0/1
'01'	Bank 2/3
'10'	Bank 4/5
'11'	Bank 6/7

NOTE: CASA[3:0]# and CASB[3:0]# are enabled, depending on the settings in Registers DCONF2 and DCONF3. Only banks set to burst EDO DRAM type will have CAS asserted.

3 — **Trigger WCBR Configuration Cycle:** A '0' to '1' transition generates a WCBR/refresh cycle. If bit 0 (ENWCBR_CONFIG) is set to '1', MA[11:0] is driven to the value programmed in bit [15:4] of this register and WE# is asserted during a CAS-before-RAS cycle. If bit 0 (ENWCBR_CONFIG) is set to '0', a normal refresh cycle is generated.

Bit	Description *(cont.)*
15:4	**MA Setting During WCBR Cycle [11:0]:** MA[0] and MA[11] are mapped to bits 4 and 15 respectively. DRAM vendors currently define MA[0] as selecting toggle mode (Pentium processor) versus linear burst mode. MA[11:1] must be 00000010000. Thus, for linear burst mode, the setting is 020H and for toggle mode, the setting is 021H.

4.4 Power Management Control Registers

4.4.1 Clock Control Register

Index: 300H

Bit	Description	Name	Reset State
0	PCI Clock Divisor During Idle [0]	PCI_IDLE_DIV0	'0'
1	PCI Clock Divisor During Idle [1]	PCI_IDLE_DIV1	'0'
2	Reserved		'0'
3	Reserved		'0'
4	PCI Idle Count [0]	PCI_IDLE_CNT0	'0'
5	PCI Idle Count [1]	PCI_IDLE_CNT1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Enable PCI Clock to Full Speed When PCI Request or Grant is Detected	MSTR_FULLSPD	'0'
9	Enable PCI Clock to Full Speed When PCI LOCK# is Detected	CKFUL_LOCKEN	'0'
10	Reserved		'0'
11	Enable CLKRUN# Method for PCI Clock Control	EN_CLKRUN	'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Enable Modular Clocking on V2 Clock	EN_MODCLKV2	'0'

Bit	Description
1:0	**PCI Clock Divisor During Idle [1:0]:** When PCI is detected to be idle, the PCI clock will be divided by the value programmed in this register. **Bit [1:0]** — **Divisor** '00' — 1 '01' — 2 '10' — 32 '11' — 256
3:2	Reserved
5:4	**PCI Idle Count [1:0]:** When PCI is idle, the PCI idle counter will start counting from zero. **Bit [1:0]** — **Idle Count (PCI Clocks)** '00' — Immediate '01' — 8 '10' — 32 '11' — 256
7:6	Reserved

Bit	Description *(cont.)*
8	**Enable PCI Clock to go Back to Full Speed When PCI Request or Grant is Detected:** '0' = disable; '1' = enable.
9	**Enable PCI Clock to go Back to Full Speed When PCI LOCK# is Detected:** '0' = disable; '1' = enable.
10	Reserved
11	**Enable CLKRUN# Method for PCI Clock Control:** '0' = use PicoPower's proprietary PCI clock control method; '1' = use PCI Mobile Design Guide's CLKRUN# pin method.
14:12	Reserved
15	**Enable Modular Clocking on V2 Clock:** '0' = disable; '1' = enable. When enabled, modular clocking for V2 clock will take effect every time the processor is in STOP GRANT state. Upon detection of DRAM refresh, PCI master request, etc. during STOP GRANT state, V2 clock will be restarted.

4.4.2 Clock Throttling Period Control Register (CTPC)

Index: 301H

Bit	Description	Name	Reset State
0	Clock Throttling Period Select [0]	CT_PERIOD0	'0'
1	Clock Throttling Period Select [1]	CT_PERIOD1	'0'
2	Clock Throttling Period Select [2]	CT_PERIOD2	'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
2:0	**Clock Throttling Period Select [2:0]:** Modulation period = CPU clock period× divisor. Modulation period is the period within which STPCLK# will throttle. **NOTE:** T = CPU bus frequency period.

Bit [2:0]	Modulation Period
'000'	800T
'001'	1600T
'010'	3200T
'011'	6400T
'100'	12800T
'101'	25600T
'110'	102400T
'111'	409600T

15:3	Reserved

4.4.3 Conserve Clock Throttling Ratio/Control Register (CON-CTRC)

Index: 302H

Bit	Description	Name	Reset State
0	Conserve Clock Throttling Ratio [0]	CONSERVE_CTR0	'0'
1	Conserve Clock Throttling Ratio [1]	CONSERVE_CTR1	'0'
2	Conserve Clock Throttling Ratio [2]	CONSERVE_CTR2	'0'
3	Conserve Clock Throttling Ratio [3]	CONSERVE_CTR3	'0'
4	Conserve Clock Throttling Enable	CONSERVE_ CTR_EN	'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Conserve Clock Throttling Ratio [3:0]:** The duty cycle shown below indicates the percentage that is being executed by the CPU. The accuracy of the duty cycle is within ±1.25%.

Bit [3:0]	Duty Cycle
'0000'	5 %
'0001'	10 %
'0010'	20 %
'0011'	30 %
'0100'	40 %
'0101'	50 %
'0110'	60 %
'0111'	70 %
'1000'	80 %
'1001'	90 %
All Others	Reserved

4 **Conserve Clock Throttling Enable:** '0' = disable; '1' = enable.

15:5 Reserved

4.4.4 Heat Regulator Clock Throttling Ratio / Control Register (HR-CTRC)

Index: 303H

Bit	Description	Name	Reset State
0	Heat Regulator Clock Throttling Ratio [0]	HR_CTR0	'0'
1	Heat Regulator Clock Throttling Ratio [1]	HR_CTR1	'0'
2	Heat Regulator Clock Throttling Ratio [2]	HR_CTR2	'0'
3	Heat Regulator Clock Throttling Ratio [3]	HR_CTR3	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	THERM Input Enable	THERM_EN	'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit — **Description**

3:0 — **Heat Regulator Clock Throttling Ratio [3:0]:** The duty cycle shown below indicates the percentage that is being executed by the CPU. The accuracy of the duty cycle is within ±1.25%

Bit [3:0]	Duty Cycle
'0000'	5 %
'0001'	10 %
'0010'	20 %
'0011'	30 %
'0100'	40 %
'0101'	50 %
'0110'	60 %
'0111'	70 %
'1000'	80 %
'1001'	90 %
All Others	Reserved

11:4 — Reserved

12 — **THERM Input Enable:** This bit uses the THERM input to indicate asystem or CPU overheat condition. When this bit is set high, an active level on the THERM input pin will force STPCLK# to throttle according to the setting of HR_CTRC Bit [3:0].

15:13 — Reserved

4.4.5 Doze/Sleep Mode Clock Throttling Ratio/Control Register (DS-CTRC)

Index: 304H

Bit	Description	Name	Reset State
0	Doze/Sleep Clock Throttling Ratio [0]	DS_CTR0	'0'
1	Doze/Sleep Clock Throttling Ratio [1]	DS_CTR1	'0'
2	Doze/Sleep Clock Throttling Ratio [2]	DS_CTR2	'0'
3	Doze/Sleep Clock Throttling Ratio [3]	DS_CTR3	'0'
4	Doze Mode Clock Throttling Enable	DOZE_CTR_EN	'0'
5	Sleep Mode Clock Throttling Enable [0]	SLP_CTR_EN0	'0'
6	Sleep Mode Clock Throttling Enable [1]	SLP_CTR_EN1	'0'
7	Sleep Mode Clock Throttling Enable [2]	SLP_CTR_EN2	'0'
8	STPCLK Release Latency [0]	STPCLK_LAT0	'0'
9	STPCLK Release Latency [1]	STPCLK_LAT1	'0'
10	STPCLK Release Latency [2]	STPCLK_LAT2	'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Doze/Sleep Clock Throttling Ratio [3:0]:** The duty cycle shown below indicates the percentage that is being executed by the CPU

Bit [3:0]	Duty Cycle
'0000'	5 %
'0001'	10 %
'0010'	20 %
'0011'	30 %
'0100'	40 %
'0101'	50 %
'0110'	60 %
'0111'	70 %
'1000'	80 %
'1001'	90 %
All Others	Reserved

4 **Doze Mode Clock Throttling Enable:** When set to '0', Doze mode will not enable clock throttling. When set to '1', Doze mode will enable clock throttling in the ratio set in DS_CTRC Bit [3:0]

Bit	Description *(cont.)*
7:5	**Sleep Mode Clock Throttling Enable [2:0] :** **Bit [2:0]** — **Function** '000' — Disable clock throttling in Sleep mode '001' — Enable clock throttling in ratio set in DS_CTRC Bit [3:0] in Sleep mode '010' — Enable LessStop mode (CPU Stop Grant state) in Sleep mode '011' — Enable MoreStop mode (CPU Stop Clock state) in Sleep mode '100' — Enable Deep_Sleep mode (MoreStop and high speed oscillator off; only 32 kHz is running.) **NOTE:** For Deep Sleep mode, if high speed oscillator is off, make sure that all devices can tolerate unstable oscillation when the clock oscillator is restarted. It is recommended that the power-down pin of the clock synthesizer chip be used to enable or disable the clock output so that its output clocks will always restart with stable frequency.
10:8	**STPCLK Release Latency (PLL Stabilization Delay) [2:0]:** This parameter defines the delay between restarting the CPU clock and deasserting STPCLK. This parameter applies only during Sleep mode when MoreStop is enabled, or when resuming from Deep Sleep mode. **Bit [2:0]** — **Delay** '000' — 0 s '001' — 1 µs '010' — 45 µs '011' — 1 ms '100' — 2 ms All Others — Reserved
15:11	Reserved

4.4.6 Wake/SMI Source Register (WSS)

Index: 310H

Bit	Description	Name	Reset State
0	System Management Interrupt Source [0]	SMISRC0	'0'
1	System Management Interrupt Source [1]	SMISRC1	'0'
2	System Management Interrupt Source [2]	SMISRC2	'0'
3	System Management Interrupt Source [3]	SMISRC3	'0'
4	System Management Interrupt Source [4]	SMISRC4	'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Wake-Up Source [0]	WAKEUP_SRC0	'0'
9	Wake-Up Source [1]	WAKEUP_SRC1	'0'
10	Wake-Up Source [2]	WAKEUP_SRC2	'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

4:0 **System Management Interrupt Source [4:0]:**

Bit [4:0]	Source
00H	None
01H	Primary Activity
02H	I/O trap
03H	Device Timers Time-out
04H	Doze Time-out
05H	Sleep Time-out
06H	Suspend Time-out
07H	GP Timer Compare
08H	SWTCH input toggling
09H	Reserved
0AH	WAKE0 input toggling
0BH	WAKE1 input toggling
0CH	EXTACT0 toggling
0DH	Reserved
0EH	Rescheduled SMI
0FH	Software SMI
10H	V3-LS INT SMI
1FH	Clear SMI source
All Others	Reserved

NOTE: These bits are read only; they should be cleared by writing a 1FH to bit [4:0]. To avoid losing any nested SMIs, the SMM handler should always clear the SMI group by writing a 1FH to bit [4:0] of WSS, then clear the corresponding flag in the Activity Registers (AFR1 and AFR2).

7:5 Reserved

Bit	Description *(cont.)*
10:8	**Wake-Up Source [2:0]:** **Bit [2:0]** — **Source** 0H — None 1H — RING 2H — SWTCH 3H — GP Timer Compare 4H — WAKE0 5H — WAKE1 6H — Reserved 7H — Clear Wake Source **NOTE:** These bits are read only; they should be cleared after reading by a write of 7H to bit [10:8].
15:11	Reserved

4.4.7 Power Management Timer Status Register (PMTS)

Index: 311H

Bit	Description	Name	Reset State
0	Doze Time-out Status	DOZE_TO	'0'
1	Sleep Time-out Status	SLEEP_TO	'0'
2	Suspend Time-out Status	SUSPEND_TO	'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Doze Time-out Status:** When high, this bit indicates that a doze Time-out has occurred. This bit will remain active until primary activity is detected, or until it is written low. Writing this bit high has no effect.
1	**Sleep Time-out Status:** When high, this bit indicates that a sleep Time-out has occurred. This bit will remain active until primary activity is detected, or until it is written low. Writing this bit high has no effect.
2	**Suspend Time-out Status:** When high, this bit indicates that a suspend Time-out has occurred. This bit will remain active until primary activity is detected, or until it is written low. Writing this bit high has no effect.
15:3	Reserved

4.4.8 Power Management Pin Status Register (PMPS)

Index: 312H

Bit	Description	Name	Reset State
0	WAKE0 Pin Status	WAKE0_ST	X
1	WAKE1 Pin Status	WAKE1_ST	X
2	EXTACT0 Pin Status	EXTACT0_ST	X
3	Reserved		'0'
4	RING Pin Status	RING_ST	X
5	SWTCH Pin Status	SWTCH_ST	X
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**WAKE0 Pin Status:** This bit reflects the status of WAKE0 input pin. This bit is read only.
1	**WAKE1 Pin Status:** This bit reflects the status of WAKE1 input pin. This bit is read only.
2	**EXTACT0 Pin Status:** This bit reflects the current status of EXTACT0 input pin. This bit is read only.
3	Reserved
4	**RING Pin Status:** This bit reflects the current status of RING input pin. This bit is read only.
5	**SWTCH Pin Status:** This bit reflects the current status of SWTCH input pin. This bit is read only.
15:6	Reserved

4.4.9 Wake Mask Control Register (WMC)

Index: 313H

Bit	Description	Name	Reset State
0	Mask WAKE0 From Resume	WMSK_WAKE0	'1'
1	Mask WAKE1 From Resume	WMSK_WAKE1	'1'
2	Mask SWTCH From Resume	WMSK_SWTCH	'0'
3	Mask RING From Resume	WMSK_RING	'1'
4	Mask GP Timer Compare From Resume	WMSK_GPTMR	'1'
5	Reserved		'1'
6	Reserved		'1'
7	Reserved		'1'
8	Reserved		'1'
9	Reserved		'1'
10	Reserved		'1'
11	Reserved		'1'
12	Reserved		'1'
13	Reserved		'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
0	**Mask WAKE0 from Resume:** When high, the WAKE0 input toggling will not trigger a wake-up from suspend mode; when low it will.
1	**Mask WAKE1 from Resume:** When high, the WAKE1 input toggling will not trigger a wake-up from suspend mode; when low it will.
2	**Mask SWTCH from Resume:** When high, the SWTCH input toggling will not trigger a wake-up from suspend mode; when low it will.
3	**Mask RING from Resume:** When high, the RING input toggling will not trigger a wake-up from suspend mode; when low it will.
4	**Mask GP Timer Compare from Resume:** When high, a compare on the GP Timer will not trigger a wake-up from suspend mode; when low it will.
15:5	Reserved

NOTE: WAKE0/1, SWTCH, and RNG toggling can be selected through EDC Register (index 354H).

4.4.10 Activity Flag Register 1 (AFR1)

Index: 314H

Bit	Description	Name	Reset State
0	Video Active	VID_ACTV	'0'
1	Hard Disk 1 Active	HD1_ACTV	'0'
2	Hard Disk 2 Active	HD2_ACTV	'0'
3	Floppy Disk Active	FLP_ACTV	'0'
4	Keyboard Active	KB_ACTV	'0'
5	Serial I/O 1 Active	SIO1_ACTV	'0'
6	Serial I/O 2 Active	SIO2_ACTV	'0'
7	Parallel I/O Active	PIO_ACTV	'0'
8	HOLD Active	HOLD_ACTV	'0'
9	Reserved		'0'
10	Programmable Range Monitor Active [0]	PROG_ACTV0	'0'
11	Programmable Range Monitor Active [1]	PROG_ACTV1	'0'
12	Programmable Range Monitor Active [2]	PROG_ACTV2	'0'
13	Programmable Range Monitor Active [3]	PROG_ACTV3	'0'
14	Programmable Range Monitor Active [4]	PROG_ACTV4	'0'
15	Programmable Range Monitor Active [5]	PROG_ACTV5	'0'

Bit	Description
0	**Video Active:** When video access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect
1	**Hard Disk 1 Active:** When hard disk 1 access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
2	**Hard Disk 2 Active:** When hard disk 2 access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
3	**Floppy Disk Active:** When floppy disk access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
4	**Keyboard Active:** When keyboard access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
5	**Serial I/O 1 Active:** When serial I/O 1 access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
6	**Serial I/O 2 Active:** When serial I/O 2 access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
7	**Parallel I/O Active:** When parallel I/O access is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.

Bit	Description *(cont.)*
8	**HOLD Active:** When HOLD is detected this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
9	Reserved
15:10	**Programmable Range Monitor Active [5:0]:** When programmable range [5:0] access is detected, the corresponding bits will be set high. Writing '0' to these bits will clear it; writing '1' will have no effect.

4.4.11 Activity Flag Register 2 (AFR2)

Index: 315H

Bit	Description	Name	Reset State
0	V3-LS Active	V3-LS_ACTV	'0'
1	Reserved		'0'
2	RING Active	RING_ACTV	'0'
3	SWTCH Active	SWTCH_ACTV	'0'
4	WAKE0 Active	WAKE0_ACTV	'0'
5	WAKE1 Active	WAKE1_ACTV	'0'
6	EXTACT0 Active	EXT0_ACTV	'0'
7	FLOAT_REQ# Active	FLOAT_REQ_ACTV	'0'
8	Device Timer [0] Time-out	DEV_TMRTO0	'0'
9	Device Timer [1] Time-out	DEV_TMRTO1	'0'
10	Device Timer [2] Time-out	DEV_TMRTO2	'0'
11	Device Timer [3] Time-out	DEV_TMRTO3	'0'
12	Device Timer [4] Time-out	DEV_TMRTO4	'0'
13	Device Timer [5] Time-out	DEV_TMRTO5	'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**V3-LS Active:** When unmasked PAIRQ from V3-LS is detected, this bit will be set high. Writing a '0' to this bit will clear it; writing a '1' will have no effect.
1	Reserved
2	**RING Active:** When RING toggling is detected, this bit will be set high. Writing a '0' to this bit will clear it; writing a '1' will have no effect.
3	**SWTCH Active:** When SWTCH toggling is detected, this bit will be set high. Writing a '0' to this bit will clear it; writing a '1' will have no effect.
4	**WAKE0 Active:** When WAKE0 toggling is detected, this bit will be set high. Writing a '0' to this bit will clear it; writing a '1' will have no effect.
5	**WAKE1 Active:** When WAKE1 toggling is detected, this bit will be set high. Writing a '0' to this bit will clear it; writing a '1' will have no effect.
6	**EXTACT0 Active:** When EXTACT0 toggling is detected, this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.
7	**FLOAT_REQ# Active:** When FLOAT_REQ# is detected, this bit will be set high. Writing '0' to this bit will clear it; writing '1' will have no effect.

Bit	Description *(cont.)*
13:8	**Device Timer [5:0] Time-out:** When the device timer [5:0] time-out occurs, these bits will be set high. These bits remain high until a reset of timer occurs or until it is written low. Writing this bit high has no effect.
15:14	Reserved

NOTE: EXTACT0, WAKE0/1, SWTCH, and RING toggling is selectable by EDC Register.

4.4.12 I/O Trap SMI Mask Register (IOTM)

Index: 316H

Bit	Description	Name	Reset State
0	Video On	VID_ON	'1'
1	Hard Disk 1 On	HD1 _ON	'1'
2	Hard Disk 2 On	HD2_ON	'1'
3	Floppy On	FLP _ON	'1'
4	Keyboard On	KBD_ON	'1'
5	Serial I/O 1 On	SIO1 _ON	'1'
6	Serial I/O 2 On	SIO2_ON	'1'
7	Parallel I/O On	PIO _ON	'1'
8	Reserved		'1'
9	Reserved		'1'
10	Programmable Range Device On [0]	PROG_ON0	'1'
11	Programmable Range Device On [1]	PROG_ON1	'1'
12	Programmable Range Device On [2]	PROG_ON2	'1'
13	Programmable Range Device On [3]	PROG_ON3	'1'
14	Programmable Range Device On [4]	PROG_ON4	'1'
15	Programmable Range Device On [5]	PROG_ON5	'1'

Bit	Description
0	**Video On:** When high, no SMI will be generated upon video access. When low, video is assumed to be off and SMI will be generated upon video access (A0000H-BFFFFH)
1	**Hard Disk 1 On:** When high, no SMI will be generated upon hard disk 1 access. When low, hard disk 1 is assumed to be off and SMI will be generated upon hard disk 1 access (1F0H-1F7H, 3F6H-3F7H).
2	**Hard Disk 2 On:** When high, no SMI will be generated upon hard disk 2 access. When low, hard disk 2 is assumed to be off and SMI will be generated upon hard disk 2 access(170H-177H, 376H-377H).
3	**Floppy On:** When high, no SMI will be generated upon floppy disk access. When low, floppy is assumed to be off and SMI will be generated upon floppy disk access (3F2H, 3F4H, 3F5H, 3F7H).
4	**Keyboard On:** When high, no SMI will be generated upon keyboard access. When low, keyboard is assumed to be off and SMI will be generated upon keyboard access (60H, 64H).
5	**Serial I/O 1 On:** When high, no SMI will be generated upon serial I/O 1 access. When low, serial I/O 1 is assumed to be off and SMI will be generated upon serial I/O 1 access (3F8H-3FFH, 3E8H-3EFH).

Bit	Description *(cont.)*
6	**Serial I/O 2 On:** When high, no SMI will be generated upon serial I/O 2 access. When low, serial I/O 2 is assumed to be off and SMI will be generated upon serial I/O 2 access (2F8H-2FFH, 2E8H-2EFH).
7	**Parallel I/O On:** When high, no SMI will be generated upon parallel I/O access. When low, parallel I/O is assumed to be off and SMI will be generated upon parallel I/O access (3BCH-3BFH, 378H-37FH, 278H-27FH).
9:8	Reserved
15:10	**Programmable Range Device On [5:0]:** When high, programmable range [5:0] device is on and no SMI will be generated. When low, programmable range [5:0] device is off and SMI will be generated when there is any access to the programmable range [5:0] device.

NOTE: There is no group mask for I/O trap event; SMI will always be generated if the corresponding bit is set to '0' and an access to that device occurs.

4.4.13 External SMI Trigger Mask Register (ESTM)

Index: 317H

Bit	Description	Name	Reset State
0	Mask WAKE0 From SMI	SMI_MSK_WAKE0	'1'
1	Mask WAKE1 From SMI	SMI_MSK_WAKE1	'1'
2	Mask SWTCH From SMI	SMI_MSK_SWTCH	'1'
3	Mask EXTACT0 From SMI	SMI_MSK_EXTACT0	'1'
4	Reserved		'1'
5	Reserved		'1'
6	Reserved		'1'
7	Reserved		'1'
8	Reserved		'1'
9	Reserved		'1'
10	Reserved		'1'
11	Reserved		'1'
12	Reserved		'1'
13	Reserved		'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
0	**Mask WAKE0 From SMI:** When high, the programmed edge of WAKE0 toggling will not trigger a SMI; when low, it will.
1	**Mask WAKE1 From SMI:** When high, the programmed edge of WAKE1 toggling will not trigger a SMI; when low, it will.
2	**Mask SWTCH From SMI:** When high, the programmed edge of SWTCH toggling will not trigger a SMI but put the system into Standby mode.
3	**Mask EXTACT0 From SMI:** When high, the programmed edge of EXTACT0 toggling will not trigger a SMI; when low, it will.
15:4	Reserved

NOTE: WAKE0, WAKE1, SWTCH, EXTACT0 toggling is selectable by EDC Register.

4.4.14 Internal SMI Trigger Mask Register (ISTM)

Index: 318H

Bit	Description	Name	Reset State
0	Mask Device Timer 0 Time-out from SMI	SMI_MSK_DEVTMR0TO	'1'
1	Mask Device Timer 1 Time-out from SMI	SMI_MSK_DEVTMR1TO	'1'
2	Mask Device Timer 2 Time-out from SMI	SMI_MSK_DEVTMR2TO	'1'
3	Mask Device Timer 3 Time-out from SMI	SMI_MSK_DEVTMR3TO	'1'
4	Mask Device Timer 4 Time-out from SMI	SMI_MSK_DEVTMR4TO	'1'
5	Mask Device Timer 5 Time-out from SMI	SMI_MSK_DEVTMR5TO	'1'
6	Mask Doze Time-out from SMI	SMI_MSK_DOZE_TO	'1'
7	Mask Sleep Time-out from SMI	SMI_MSK_SLEEP_TO	'1'
8	Mask Suspend Time-out From SMI	SMI_MSK_SPND_TO	'1'
9	Mask GP Timer Compare From SMI	SMI_MSK_GPTMR	'1'
10	Reserved		'1'
11	Reserved		'1'
12	Reserved		'1'
13	Reserved		'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
0	**Mask Device Timer 0 Time-out from SMI:** When high, device timer 0 time-out will not trigger a SMI; when low, it will.
1	**Mask Device Timer 1 Time-out from SMI:** When high, device timer 1 time-out will not trigger a SMI; when low, it will.
2	**Mask Device Timer 2 Time-out from SMI:** When high, device timer 2 time-out will not trigger a SMI; when low, it will.
3	**Mask Device Timer 3 Time-out from SMI:** When high, device timer 3 time-out will not trigger a SMI; when low, it will.
4	**Mask Device Timer 4 Time-out from SMI:** When high, device timer 4 time-out will not trigger a SMI; when low, it will.
5	**Mask Device Timer 5 Time-out from SMI:** When high, device timer 5 time-out will not trigger a SMI; when low, it will.
6	**Mask Doze Time-out from SMI:** When high, Doze time-out will not trigger a SMI. Instead the power management controller will change state directly from fully-on to Doze mode. When low, Doze time-out will trigger a SMI and no automatic mode transition.

Bit	Description *(cont.)*
7	**Mask Sleep Time-out from SMI:** When high, sleep time-out will not trigger a SMI; when low, it will. When high, the power management controller will change the state directly from Doze to Sleep mode. When low, sleep time-out will trigger a SMI and no automatic mode transition will occur.
8	**Mask Suspend Time-out from SMI:** When high, Suspend mode time-out will not trigger a SMI; when low, it will.
9	**Mask GP Timer Compare from SMI:** When high, a compare on the GP Timer/Counter will not trigger a SMI; when low, it will.
15:10	Reserved

NOTE: Primary Activity can also trigger SMM and its mask bit is located at Register PAOC bit 1.

4.4.15 Software SMI Trigger Register (SST)

Index: 319H

Bit	Description	Name	Reset State
0	Reschedule SMI Select [0]	RSMI_SEL0	'0'
1	Reschedule SMI Select [1]	RSMI_SEL1	'0'
2	Reschedule SMI Select [2]	RSMI_SEL2	'0'
3	Reschedule SMI Select [3]	RSMI_SEL3	'0'
4	Reschedule SMI Prescalar	RSMI_PRESCALAR	'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Soft SMI Immediate	SFTSMI_TRIG	'0'
9	Enable Soft SMI on I/O Write to B0H	SFTSMI_B0	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**Reschedule SMI Select [3:0]:** **Bit [3:0]** — **Value** 0H — Disable 1H — 1 2H — 2 3H — 3 4H — 4 5H — 5 6H — 6 7H — 7 8H — 8 9H — 9 All Others — Reserved
4	**Reschedule SMI Prescalar:** '0' = 10 ms; '1' = 100 ms.
7:5	Reserved
8	**Soft SMI Immediate:** Setting this bit to '1' will trigger a SMI. The value read from this bit has no meaning.
9	**Enable Soft SMI on I/O Write to B0H:** When high, a write to port B0H will trigger a SMI; when low, a write to port B0H will not trigger a SMI.
15:10	Reserved

4.4.16 Primary Activity Option Control register (PAOC)

Index: 31AH

Bit	Description	Name	Reset State
0	Primary Activity Flag Enable	PAFLGEN	'0'
1	Mask Primary Activity From SMI	SMI_MSK_PA	'1'
2	Enable P/A to be Latched in SMM Mode	ENLTCH_PA_SMM	'0'
3	Disable Primary Activity On	DISPACTVON	'0'
4	Mask SMI From Primary Activity	MSKSMI_PA	'1'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Primary Activity Flag Enable:** '0' = disable; '1' = enable. When enabled, primary activity will be flagged (Refer to register AFR1 and AFR2 for additional information) during Doze or Sleep mode. When disabled, no flagging occurs. If SMI is used, this bit should be enabled to specify exact P/A source.
1	**Mask Primary Activity From SMI:** When high, primary activity will not trigger a SMI; when low, it will.
2	**Enable Primary Activity to be Latched in SMM Mode:** '0' = disable; '1' = enable. This bit enables latching primary activity that occurs in SMM. The P/A is active until deassertion of SMIACT# and will keep in a reset state and the system in On/Conserve mode while active.
3	**Disable Primary Activity On:** This bit disables the power management controller from switching to 'on' mode upon detection of any unmasked condition of the primary idle detector.
4	**Mask SMI from Primary Activity:** When set low, this bit allows any unmasked SMI (except for SMI caused by a primary activity) to trigger a primary activity. **NOTE:** This primary activity does not reset timers. This bit applies to Revision BB and later silicon revisions.
15:5	Reserved

4.4.17 Primary Activity Mask Register 1 (PAM1)

Index: 31BH

Bit	Description	Name	Reset State
0	Primary Activity Mask Video Accesses	PAMSK_VID	'1'
1	Primary Activity Mask Hard Disk 1 Accesses	PAMSK_HD1	'1'
2	Primary Activity Mask Hard Disk 2 Accesses	PAMSK_HD2	'1'
3	Primary Activity Mask Floppy Accesses	PAMSK_FLP	'1'
4	Primary Activity Mask Keyboard Accesses	PAMSK_KBD	'1'
5	Primary Activity Mask Serial I/O 1 Accesses	PAMSK_SIO1	'1'
6	Primary Activity Mask Serial I/O 2 Accesses	PAMSK_SIO2	'1'
7	Primary Activity Mask Parallel I/O Accesses	PAMSK_PIO	'1'
8	Primary Activity Mask HOLD	PAMSK_HOLD	'1'
9	Reserved		'1'
10	Primary Activity Mask Programmable Range Accesses [0]	PAMSK_PROG0	'1'
11	Primary Activity Mask Programmable Range Accesses [1]	PAMSK_PROG1	'1'
12	Primary Activity Mask Programmable Range Accesses [2]	PAMSK_PROG2	'1'
13	Primary Activity Mask Programmable Range Accesses [3]	PAMSK_PROG3	'1'
14	Primary Activity Mask Programmable Range Access [4]	PAMSK_PROG4	'1'
15	Primary Activity Mask Programmable Range Accesses [5]	PAMSK_PROG5	'1'

Bit	Description
0	**Primary Activity Mask Video Accesses:** When high, video accesses will not trigger the primary idle detector. (A0000H-BFFFFH)
1	**Primary Activity Mask Hard Disk 1 Accesses:** When high, hard disk 1 accesses will not trigger the primary idle detector. (1F0H-1F7H, 3F6H)
2	**Primary Activity Mask Hard Disk 2 Accesses:** When high, hard disk 2 accesses will not trigger the primary idle detector. (170H-177H, 376H)
3	**Primary Activity Mask Floppy Accesses:** When high, floppy accesses will not trigger the primary idle detector. (3F2H, 3F4H, 3F5H)
4	**Primary Activity Mask Keyboard Accesses:** When high, keyboard accesses will not trigger the primary idle detector. (60H, 64H)
5	**Primary Activity Mask Serial I/O 1 Accesses:** When high, serial I/O 1 accesses will not trigger the primary idle detector. (3F8H-3FFH, 3E8H-3EFH)

Bit	Description *(cont.)*
6	**Primary Activity Mask Serial I/O 2 Accesses:** When high, serial I/O 2 accesses will not trigger the primary idle detector (2F8H-2FFH, 2E8H-2EFH).
7	**Primary Activity Mask Parallel I/O Accesses:** When high, parallel I/O accesses will not trigger the primary idle detector (3BCH-3BFH, 378H-37FH, 278H-27FH).
8	**Primary Activity Mask HOLD:** When high, HOLD active will not trigger the primary idle detector.
9	Reserved
15:10	**Primary Activity Mask Programmable Range [5:0] Accesses:** When high, programmable range [5:0] accesses will not trigger the primary idle detector.

4.4.18 Primary Activity Mask Register 2 (PAM2)

Index: 31CH

Bit	Description	Name	Reset State
0	Reserved		'1'
1	Reserved		'1'
2	Reserved		'1'
3	Reserved		'1'
4	Reserved		'1'
5	Reserved		'1'
6	Primary Activity Mask EXTACT0	PAMSK_EXT0	'1'
7	Reserved		'1'
8	Primary Activity Mask RING	PAMSK_RING	'1'
9	Primary Activity Mask WAKE0	PAMSK_WAKE0	'1'
10	Primary Activity Mask WAKE1	PAMSK_WAKE1	'1'
11	Primary Activity Mask SWTCH	PAMSK_SWTCH	'1'
12	Primary Activity Mask FLOAT_REQ#	PAMSK_FLOTREQ#	'1'
13	Reserved		'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
5:0	Reserved
6	**Primary Activity Mask EXTACT0:** When high, the programmed edge of EXTACT0 toggling will not trigger the primary idle detector; when low, it will.
7	Reserved
8	**Primary Activity Mask RING:** When high, the programmed edge of RING will not trigger the primary idle detector; when low, it will. **NOTE:** The ring counter does not apply in generating primary activity.
9	**Primary Activity Mask WAKE0:** When high, the programmed edge of WAKE0 will not trigger the primary idle detector. When low, it will.
10	**Primary Activity Mask WAKE1:** When high, the programmed edge of WAKE1 will not trigger the primary idle detector; when low, it will.
11	**Primary Activity Mask SWTCH:** When high, the programmed edge of SWTCH will not trigger the primary idle detector; when low, it will.
12	**Primary Activity Mask FLOAT_REQ#:** When high, FLOAT_REQ# active will not trigger the primary idle detector.
15:13	Reserved

4.4.19 Secondary Activity Mask Register (SAM)

Index: 31DH

Bit	Description	Name	Reset State
0	Mask SMI From Secondary Activity (S/A)	SA_MSK_SMI	'1'
1	Mask HOLD From Secondary Activity	SA_MSK_HOLD	'1'
2	Reserved		'1'
3	Reserved		'1'
4	Reserved		'1'
5	Reserved		'1'
6	Mask EXTACT0 From Secondary Activity	SA_MSK_EXT0	'1'
7	Reserved		'1'
8	Reserved		'1'
9	Reserved		'1'
10	Reserved		'1'
11	Reserved		'1'
12	Reserved		'1'
13	Reserved		'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
0	**Mask SMI From Secondary Activity:** When high, SMI will not trigger the secondary activity. When low, SMI will trigger the secondary activity and the duration of this activity will be determined by SMIACT#. **NOTE:** S/A can only revive out of Doze or Sleep mode.
1	**Mask HOLD From Secondary Activity:** When high, HOLD will not trigger the secondary activity. When low, HOLD will trigger the secondary activity and the SA duration will be determined by HLDA.
5:2	Reserved
6	**Mask EXTACT0 From Secondary Activity:** When high, EXTACT0 toggling will not trigger the secondary activity; when low, it will. **NOTE:** S/A can only revive out of Doze or Sleep mode.
15:7	Reserved

NOTE: EXTACT0 toggling is selectable by EDC Register for more information. Refer to SAT Register for more information.

4.4.20 RING Count Control Register (RCC)

Index: 31EH

Bit	Description	Name	Reset State
0	RINGS One's Digit [0]	RINGS1SEL0	'0'
1	RINGS One's Digit [1]	RINGS1SEL1	'0'
2	RINGS One's Digit [2]	RINGS1SEL2	'0'
3	RINGS One's Digit [3]	RINGS1SEL3	'0'
4	RINGS Ten's Digit	RINGS10SEL	'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **RINGS One's Digit [3:0]:** When these bits are set to 0H and bit 4, RINGS10SEL is set to '0', the ring counter will be reset:

Bit [3:0]	Value
0H	Disabled (Ring counter reset to '0')
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

4 **RINGS Ten's Digit:** '0' = 0; '1' = 1.

15:5 Reserved

4.4.21 Programmable Range Monitor Control Register 1 (PRM_CTRL1)

Index: 320H

Bit	Description	Name	Reset State
0	Programmable Range Monitor [0]	PRMMIO0	'0'
1	Programmable Range Monitor [1]	PRMMIO1	'0'
2	Programmable Range Monitor [2]	PRMMIO2	'0'
3	Programmable Range Monitor [3]	PRMMIO3	'0'
4	Programmable Range Monitor [4]	PRMMIO4	'0'
5	Programmable Range Monitor [5]	PRMMIO5	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Programmable Range Monitor Enable [0]	PRMEN0	'0'
9	Programmable Range Monitor Enable [1]	PRMEN1	'0'
10	Programmable Range Monitor Enable [2]	PRMEN2	'0'
11	Programmable Range Monitor Enable [3]	PRMEN3	'0'
12	Programmable Range Monitor Enable [4]	PRMEN4	'0'
13	Programmable Range Monitor Enable [5]	PRMEN5	'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
5:0	**Programmable Range Monitor [5:0] Memory or I/O Compare Enable:** When high, the monitor will select memory addresses, and when low, the monitor will select I/O addresses.
7:6	Reserved
13:8	**Programmable Range Monitor Enable [5:0]:** When high, the programmable range monitor will be enabled.
15:14	Reserved

4.4.22 Programmable Range Monitor Control Register 2 (PRM_CTRL2)

Index: 321H

Bit	Description	Name	Reset State
0	Programmable Range Monitor Write Enable [0]	PRMWREN0	'0'
1	Programmable Range Monitor Write Enable [1]	PRMWREN1	'0'
2	Programmable Range Monitor Write Enable [2]	PRMWREN2	'0'
3	Programmable Range Monitor Write Enable [3]	PRMWREN3	'0'
4	Programmable Range Monitor Write Enable [4]	PRMWREN4	'0'
5	Programmable Range Monitor Write Enable [5]	PRMWREN5	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Programmable Range Monitor Read Enable [0]	PRMRDEN0	'0'
9	Programmable Range Monitor Read Enable [1]	PRMRDEN1	'0'
10	Programmable Range Monitor Read Enable [2]	PRMRDEN2	'0'
11	Programmable Range Monitor Read Enable [3]	PRMRDEN3	'0'
12	Programmable Range Monitor Read Enable [4]	PRMRDEN4	'0'
13	Programmable Range Monitor Read Enable [5]	PRMRDEN5	'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
5:0	**Programmable Range Monitor [5:0] Write Enable:** When high, the monitor will select write cycles.
7:6	Reserved
13:8	**Programmable Range Monitor Read Enable [5:0]:** When high, the monitor will select read cycles.
15:14	Reserved

4.4.23 Programmable Range Monitor 0 Address Register (PRMA0)

Index: 322H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 0 Addresses [0]	PRMA00	'0'
1	Programmable Range Monitor 0 Addresses [1]	PRMA01	'0'
2	Programmable Range Monitor 0 Addresses [2]	PRMA02	'0'
3	Programmable Range Monitor 0 Addresses [3]	PRMA03	'0'
4	Programmable Range Monitor 0 Addresses [4]	PRMA04	'0'
5	Programmable Range Monitor 0 Addresses [5]	PRMA05	'0'
6	Programmable Range Monitor 0 Addresses [6]	PRMA06	'0'
7	Programmable Range Monitor 0 Addresses [7]	PRMA07	'0'
8	Programmable Range Monitor 0 Addresses [8]	PRMA08	'0'
9	Programmable Range Monitor 0 Addresses [9]	PRMA09	'0'
10	Programmable Range Monitor 0 Addresses [10]	PRMA010	'0'
11	Programmable Range Monitor 0 Addresses [11]	PRMA011	'0'
12	Programmable Range Monitor 0 Addresses [12]	PRMA012	'0'
13	Programmable Range Monitor 0 Addresses [13]	PRMA013	'0'
14	Programmable Range Monitor 0 Addresses [14]	PRMA014	'0'
15	Programmable Range Monitor 0 Addresses [15]	PRMA015	'0'

Bit	Description
15:0	**Programmable Range Monitor 0 Addresses [15:0]:** These bits represent the values to be compared against appropriate CPU addresses. For an I/O monitor the addresses monitored will be A[15:0], and for a memory monitor they will be A[31:16].

4.4.24 Programmable Range Monitor 0 Compare Register (PRMC0)

Index: 323H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 0 Compare Enable [0]	PRMCMP00	'0'
1	Programmable Range Monitor 0 Compare Enable [1]	PRMCMP01	'0'
2	Programmable Range Monitor 0 Compare Enable [2]	PRMCMP02	'0'
3	Programmable Range Monitor 0 Compare Enable [3]	PRMCMP03	'0'
4	Programmable Range Monitor 0 Compare Enable [4]	PRMCMP04	'0'
5	Programmable Range Monitor 0 Compare Enable [5]	PRMCMP05	'0'
6	Programmable Range Monitor 0 Compare Enable [6]	PRMCMP06	'0'
7	Programmable Range Monitor 0 Compare Enable [7]	PRMCMP07	'0'
8	Programmable Range Monitor 0 Compare Enable [8]	PRMCMP08	'0'
9	Programmable Range Monitor 0 Compare Enable [9]	PRMCMP09	'0'
10	Programmable Range Monitor 0 Compare Enable [10]	PRMCMP010	'0'
11	Programmable Range Monitor 0 Compare Enable [11]	PRMCMP011	'0'
12	Programmable Range Monitor 0 Compare Enable [12]	PRMCMP012	'0'
13	Programmable Range Monitor 0 Compare Enable [13]	PRMCMP013	'0'
14	Programmable Range Monitor 0 Compare Enable [14]	PRMCMP014	'0'
15	Programmable Range Monitor 0 Compare Enable [15]	PRMCMP015	'0'

Bit	Description
15:0	**Programmable Range Monitor 0 Compare Enable [15:0]:** These bits indicate which of the programmable range monitor addresses will be compared against the equivalent CPU address. For an I/O compare, they enable A[15:0], and for a memory compare, they enable A[31:16]. When high, the equivalent address will be compared; when low, it will be ignored.

4.4.25 Programmable Range Monitor 1 Address Register (PRMA1)

Index: 324H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 1 Addresses [0]	PRMA10	'0'
1	Programmable Range Monitor 1 Addresses [1]	PRMA11	'0'
2	Programmable Range Monitor 1 Addresses [2]	PRMA12	'0'
3	Programmable Range Monitor 1 Addresses [3]	PRMA13	'0'
4	Programmable Range Monitor 1 Addresses [4]	PRMA14	'0'
5	Programmable Range Monitor 1 Addresses [5]	PRMA15	'0'
6	Programmable Range Monitor 1 Addresses [6]	PRMA16	'0'
7	Programmable Range Monitor 1 Addresses [7]	PRMA17	'0'
8	Programmable Range Monitor 1 Addresses [8]	PRMA18	'0'
9	Programmable Range Monitor 1 Addresses [9]	PRMA19	'0'
10	Programmable Range Monitor 1 Addresses [10]	PRMA110	'0'
11	Programmable Range Monitor 1 Addresses [11]	PRMA111	'0'
12	Programmable Range Monitor 1 Addresses [12]	PRMA112	'0'
13	Programmable Range Monitor 1 Addresses [13]	PRMA113	'0'
14	Programmable Range Monitor 1 Addresses [14]	PRMA114	'0'
15	Programmable Range Monitor 1 Addresses [15]	PRMA115	'0'

Bit	Description
15:0	**Programmable Range Monitor 1 Addresses [15:0]:** These bits represent the values to be compared against appropriate CPU addresses. For an I/O monitor the addresses monitored will be A[15:0], and for a memory monitor they will be A[31:16].

4.4.26 Programmable Range Monitor 1 Compare Register (PRMC1)

Index: 325H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 1 Compare Enable [0]	PRMCMP10	'0'
1	Programmable Range Monitor 1 Compare Enable [1]	PRMCMP11	'0'
2	Programmable Range Monitor 1 Compare Enable [2]	PRMCMP12	'0'
3	Programmable Range Monitor 1 Compare Enable [3]	PRMCMP13	'0'
4	Programmable Range Monitor 1 Compare Enable [4]	PRMCMP14	'0'
5	Programmable Range Monitor 1 Compare Enable [5]	PRMCMP15	'0'
6	Programmable Range Monitor 1 Compare Enable [6]	PRMCMP16	'0'
7	Programmable Range Monitor 1 Compare Enable [7]	PRMCMP17	'0'
8	Programmable Range Monitor 1 Compare Enable [8]	PRMCMP18	'0'
9	Programmable Range Monitor 1 Compare Enable [9]	PRMCMP19	'0'
10	Programmable Range Monitor 1 Compare Enable [10]	PRMCMP110	'0'
11	Programmable Range Monitor 1 Compare Enable [11]	PRMCMP111	'0'
12	Programmable Range Monitor 1 Compare Enable [12]	PRMCMP112	'0'
13	Programmable Range Monitor 1 Compare Enable [13]	PRMCMP113	'0'
14	Programmable Range Monitor 1 Compare Enable [14]	PRMCMP114	'0'
15	Programmable Range Monitor 1 Compare Enable [15]	PRMCMP115	'0'

Bit	Description
15:0	**Programmable Range Monitor 1 Compare Enable [15:0]:** These bits indicate which of the programmable range monitor addresses will be compared against the equivalent CPU address. For an I/O compare, they enable A[15:0], and for a memory compare, they enable A[31:16]. When high, the equivalent address will be compared; when low, it will be ignored.

4.4.27 Programmable Range Monitor 2 Address Register (PRMA2)

Index: 326H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 2 Addresses [0]	PRMA20	'0'
1	Programmable Range Monitor 2 Addresses [1]	PRMA21	'0'
2	Programmable Range Monitor 2 Addresses [2]	PRMA22	'0'
3	Programmable Range Monitor 2 Addresses [3]	PRMA23	'0'
4	Programmable Range Monitor 2 Addresses [4]	PRMA24	'0'
5	Programmable Range Monitor 2 Addresses [5]	PRMA25	'0'
6	Programmable Range Monitor 2 Addresses [6]	PRMA26	'0'
7	Programmable Range Monitor 2 Addresses [7]	PRMA27	'0'
8	Programmable Range Monitor 2 Addresses [8]	PRMA28	'0'
9	Programmable Range Monitor 2 Addresses [9]	PRMA29	'0'
10	Programmable Range Monitor 2 Addresses [10]	PRMA210	'0'
11	Programmable Range Monitor 2 Addresses [11]	PRMA211	'0'
12	Programmable Range Monitor 2 Addresses [12]	PRMA212	'0'
13	Programmable Range Monitor 2 Addresses [13]	PRMA213	'0'
14	Programmable Range Monitor 2 Addresses [14]	PRMA214	'0'
15	Programmable Range Monitor 2 Addresses [15]	PRMA215	'0'

Bit	Description
15:0	**Programmable Range Monitor 2 Addresses [15:0]:** These bits represent the values to be compared against appropriate CPU addresses. For an I/O monitor, the addresses monitored will be A[15:0], and for a memory monitor they will be A[31:16].

4.4.28 Programmable Range Monitor 2 Compare Register (PRMC2)

Index: 327H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 2 Compare Enable [0]	PRMCMP20	'0'
1	Programmable Range Monitor 2 Compare Enable [1]	PRMCMP21	'0'
2	Programmable Range Monitor 2 Compare Enable [2]	PRMCMP22	'0'
3	Programmable Range Monitor 2 Compare Enable [3]	PRMCMP23	'0'
4	Programmable Range Monitor 2 Compare Enable [4]	PRMCMP24	'0'
5	Programmable Range Monitor 2 Compare Enable [5]	PRMCMP25	'0'
6	Programmable Range Monitor 2 Compare Enable [6]	PRMCMP26	'0'
7	Programmable Range Monitor 2 Compare Enable [7]	PRMCMP27	'0'
8	Programmable Range Monitor 2 Compare Enable [8]	PRMCMP28	'0'
9	Programmable Range Monitor 2 Compare Enable [9]	PRMCMP29	'0'
10	Programmable Range Monitor 2 Compare Enable [10]	PRMCMP210	'0'
11	Programmable Range Monitor 2 Compare Enable [11]	PRMCMP211	'0'
12	Programmable Range Monitor 2 Compare Enable [12]	PRMCMP212	'0'
13	Programmable Range Monitor 2 Compare Enable [13]	PRMCMP213	'0'
14	Programmable Range Monitor 2 Compare Enable [14]	PRMCMP214	'0'
15	Programmable Range Monitor 2 Compare Enable [15]	PRMCMP215	'0'

Bit	Description
15:0	**Programmable Range Monitor 2 Compare Enable [15:0]:** These bits indicate which of the programmable range monitor addresses will be compared against the equivalent CPU address. For an I/O compare, they enable A[15:0], and for a memory compare, they enable A[31:16]. When high, the equivalent address will be compared; when low, it will be ignored.

4.4.29 Programmable Range Monitor 3 Address Register (PRMA3)

Index: 328H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 3 Addresses [0]	PRMA30	'0'
1	Programmable Range Monitor 3 Addresses [1]	PRMA31	'0'
2	Programmable Range Monitor 3 Addresses [2]	PRMA32	'0'
3	Programmable Range Monitor 3 Addresses [3]	PRMA33	'0'
4	Programmable Range Monitor 3 Addresses [4]	PRMA34	'0'
5	Programmable Range Monitor 3 Addresses [5]	PRMA35	'0'
6	Programmable Range Monitor 3 Addresses [6]	PRMA36	'0'
7	Programmable Range Monitor 3 Addresses [7]	PRMA37	'0'
8	Programmable Range Monitor 3 Addresses [8]	PRMA38	'0'
9	Programmable Range Monitor 3 Addresses [9]	PRMA39	'0'
10	Programmable Range Monitor 3 Addresses [10]	PRMA310	'0'
11	Programmable Range Monitor 3 Addresses [11]	PRMA311	'0'
12	Programmable Range Monitor 3 Addresses [12]	PRMA312	'0'
13	Programmable Range Monitor 3 Addresses [13]	PRMA313	'0'
14	Programmable Range Monitor 3 Addresses [14]	PRMA314	'0'
15	Programmable Range Monitor 3 Addresses [15]	PRMA315	'0'

Bit	Description
15:0	**Programmable Range Monitor 3 Addresses [15:0]:** These bits represent the values to be compared against appropriate CPU addresses. For an I/O monitor, the addresses monitored will be A[15:0], and for a memory monitor they will be A[31:16].

4.4.30 Programmable Range Monitor 3 Compare Register (PRMC3)

Index: 329H

Bit	Description	Name	Reset State
0	Programmable Range Monitor 3 Compare Enable [0]	PRMCMP30	'0'
1	Programmable Range Monitor 3 Compare Enable [1]	PRMCMP31	'0'
2	Programmable Range Monitor 3 Compare Enable [2]	PRMCMP32	'0'
3	Programmable Range Monitor 3 Compare Enable [3]	PRMCMP33	'0'
4	Programmable Range Monitor 3 Compare Enable [4]	PRMCMP34	'0'
5	Programmable Range Monitor 3 Compare Enable [5]	PRMCMP35	'0'
6	Programmable Range Monitor 3 Compare Enable [6]	PRMCMP36	'0'
7	Programmable Range Monitor 3 Compare Enable [7]	PRMCMP37	'0'
8	Programmable Range Monitor 3 Compare Enable [8]	PRMCMP38	'0'
9	Programmable Range Monitor 3 Compare Enable [9]	PRMCMP39	'0'
10	Programmable Range Monitor 3 Compare Enable [10]	PRMCMP310	'0'
11	Programmable Range Monitor 3 Compare Enable [11]	PRMCMP311	'0'
12	Programmable Range Monitor 3 Compare Enable [12]	PRMCMP312	'0'
13	Programmable Range Monitor 3 Compare Enable [13]	PRMCMP313	'0'
14	Programmable Range Monitor 3 Compare Enable [14]	PRMCMP314	'0'
15	Programmable Range Monitor 3 Compare Enable [15]	PRMCMP315	'0'

Bit	Description
15:0	**Programmable Range Monitor 3 Compare Enable [15:0]:** These bits indicate which of the programmable range monitor addresses will be compared against the equivalent CPU address. For an I/O compare, they enable A[15:0], and for a memory compare, they enable A[31:16]. When high, the equivalent address will be compared; when low, it will be ignored.

4.4.31 Programmable Range Monitor 4 Address Register (PRMA4)

Index: 32AH

Bit	Description	Name	Reset State
0	Programmable Range Monitor 4 Addresses [0]	PRMA40	'0'
1	Programmable Range Monitor 4 Addresses [1]	PRMA41	'0'
2	Programmable Range Monitor 4 Addresses [2]	PRMA42	'0'
3	Programmable Range Monitor 4 Addresses [3]	PRMA43	'0'
4	Programmable Range Monitor 4 Addresses [4]	PRMA44	'0'
5	Programmable Range Monitor 4 Addresses [5]	PRMA45	'0'
6	Programmable Range Monitor 4 Addresses [6]	PRMA46	'0'
7	Programmable Range Monitor 4 Addresses [7]	PRMA47	'0'
8	Programmable Range Monitor 4 Addresses [8]	PRMA48	'0'
9	Programmable Range Monitor 4 Addresses [9]	PRMA49	'0'
10	Programmable Range Monitor 4 Addresses [10]	PRMA410	'0'
11	Programmable Range Monitor 4 Addresses [11]	PRMA411	'0'
12	Programmable Range Monitor 4 Addresses [12]	PRMA412	'0'
13	Programmable Range Monitor 4 Addresses [13]	PRMA413	'0'
14	Programmable Range Monitor 4 Addresses [14]	PRMA414	'0'
15	Programmable Range Monitor 4 Addresses [15]	PRMA415	'0'

Bit	Description
15:0	**Programmable Range Monitor 4 Addresses [15:0]:** These bits represent the values to be compared against appropriate CPU addresses. For an I/O monitor, the addresses monitored will be A[15:0], and for a memory monitor they will be A[19:4].

4.4.32 Programmable Range Monitor 4 Compare Register (PRMC4)

Index: 32BH

Bit	Description	Name	Reset State
0	Programmable Range Monitor 4 Compare Enable [0]	PRMCMP40	'0'
1	Programmable Range Monitor 4 Compare Enable [1]	PRMCMP41	'0'
2	Programmable Range Monitor 4 Compare Enable [2]	PRMCMP42	'0'
3	Programmable Range Monitor 4 Compare Enable [3]	PRMCMP43	'0'
4	Programmable Range Monitor 4 Compare Enable [4]	PRMCMP44	'0'
5	Programmable Range Monitor 4 Compare Enable [5]	PRMCMP45	'0'
6	Programmable Range Monitor 4 Compare Enable [6]	PRMCMP46	'0'
7	Programmable Range Monitor 4 Compare Enable [7]	PRMCMP47	'0'
8	Programmable Range Monitor 4 Compare Enable [8]	PRMCMP48	'0'
9	Programmable Range Monitor 4 Compare Enable [9]	PRMCMP49	'0'
10	Programmable Range Monitor 4 Compare Enable [10]	PRMCMP410	'0'
11	Programmable Range Monitor 4 Compare Enable [11]	PRMCMP411	'0'
12	Programmable Range Monitor 4 Compare Enable [12]	PRMCMP412	'0'
13	Programmable Range Monitor 4 Compare Enable [13]	PRMCMP413	'0'
14	Programmable Range Monitor 4 Compare Enable [14]	PRMCMP414	'0'
15	Programmable Range Monitor 4 Compare Enable [15]	PRMCMP415	'0'

Bit	Description
15:0	**Programmable Range Monitor 4 Compare Enable [15:0]:** These bits indicate which of the programmable range monitor addresses will be compared against the equivalent CPU address. For an I/O compare, they enable A[15:0], and for a memory compare, they enable A[19:4]. When high, the equivalent address will be compared; when low, it will be ignored.

4.4.33 Programmable Range Monitor 5 Address Register (PRMA5)

Index: 32CH

Bit	Description	Name	Reset State
0	Programmable Range Monitor 5 Addresses [0]	PRMA20	'0'
1	Programmable Range Monitor 5 Addresses [1]	PRMA21	'0'
2	Programmable Range Monitor 5 Addresses [2]	PRMA22	'0'
3	Programmable Range Monitor 5 Addresses [3]	PRMA23	'0'
4	Programmable Range Monitor 5 Addresses [4]	PRMA24	'0'
5	Programmable Range Monitor 5 Addresses [5]	PRMA25	'0'
6	Programmable Range Monitor 5 Addresses [6]	PRMA26	'0'
7	Programmable Range Monitor 5 Addresses [7]	PRMA27	'0'
8	Programmable Range Monitor 5 Addresses [8]	PRMA28	'0'
9	Programmable Range Monitor 5 Addresses [9]	PRMA29	'0'
10	Programmable Range Monitor 5 Addresses [10]	PRMA210	'0'
11	Programmable Range Monitor 5 Addresses [11]	PRMA211	'0'
12	Programmable Range Monitor 5 Addresses [12]	PRMA212	'0'
13	Programmable Range Monitor 5 Addresses [13]	PRMA213	'0'
14	Programmable Range Monitor 5 Addresses [14]	PRMA214	'0'
15	Programmable Range Monitor 5 Addresses [15]	PRMA215	'0'

Bit	Description
15:0	**Programmable Range Monitor 5 Addresses [15:0]:** These bits represent the values to be compared against appropriate CPU addresses. For an I/O monitor, the addresses monitored will be A[15:0], and for a memory monitor they will be A[19:4].

4.4.34 Programmable Range Monitor 5 Compare Register (PRMC5)

Index: 32DH

Bit	Description	Name	Reset State
0	Programmable Range Monitor 5 Compare Enable [0]	PRMCMP50	'0'
1	Programmable Range Monitor 5 Compare Enable [1]	PRMCMP51	'0'
2	Programmable Range Monitor 5 Compare Enable [2]	PRMCMP52	'0'
3	Programmable Range Monitor 5 Compare Enable [3]	PRMCMP53	'0'
4	Programmable Range Monitor 5 Compare Enable [4]	PRMCMP54	'0'
5	Programmable Range Monitor 5 Compare Enable [5]	PRMCMP55	'0'
6	Programmable Range Monitor 5 Compare Enable [6]	PRMCMP56	'0'
7	Programmable Range Monitor 5 Compare Enable [7]	PRMCMP57	'0'
8	Programmable Range Monitor 5 Compare Enable [8]	PRMCMP58	'0'
9	Programmable Range Monitor 5 Compare Enable [9]	PRMCMP59	'0'
10	Programmable Range Monitor 5 Compare Enable [10]	PRMCMP510	'0'
11	Programmable Range Monitor 5 Compare Enable [11]	PRMCMP511	'0'
12	Programmable Range Monitor 5 Compare Enable [12]	PRMCMP512	'0'
13	Programmable Range Monitor 5 Compare Enable [13]	PRMCMP513	'0'
14	Programmable Range Monitor 5 Compare Enable [14]	PRMCMP514	'0'
15	Programmable Range Monitor 5 Compare Enable [15]	PRMCMP515	'0'

Bit	Description
15:0	**Programmable Range Monitor 5 Compare Enable [15:0]:** These bits indicate which of the programmable range monitor addresses will be compared against the equivalent CPU address. For an I/O compare, they enable A[15:0], and for a memory compare, they enable A[19:4]. When high, the equivalent address will be compared; when low, it will be ignored.

4.4.35 Power Management Mode Register (PMM)

Index: 330H

Bit	Description	Name	Reset State
0	System Management Mode [0]	SM_MODE0	'0'
1	System Management Mode [1]	SM_MODE1	'0'
2	System Management Mode [2]	SM_MODE2	'0'
3	Resume	RESUME	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

2:0 **System Management Mode [2:0]:**

Bit [2:0]	Power Manangement State
0H	On
1H	Doze
2H	Sleep or Deep Sleep
3H	Suspend
All Others	Reserved

These bits are read and write. The system will enter the corresponding mode if a value of 0H-3H is written. A write of 4H-7H will have no effect on the power management mode.

3 **Resume:** When high, this bit indicates that the system has entered Suspend mode such that the previous system state must be restored. This bit should be written low upon resuming.

15:4 Reserved

4.4.36 On/Doze Mode Power Control Register (ONDZ-PC)

Index: 331H

Bit	Description	Name	Reset State
0	Power Control On/Doze Mode [0]	PCONDZ0	'1'
1	Power Control On/Doze Mode [1]	PCONDZ1	'1'
2	Power Control On/Doze Mode [2]	PCONDZ2	'1'
3	Power Control On/Doze Mode [3]	PCONDZ3	'0'
4	Power Control On/Doze Mode [4]	PCONDZ4	'0'
5	Power Control On/Doze Mode [5]	PCONDZ5	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
5:0	**Power Control On/Doze Mode [5:0]:** If any bit is high and On/Doze mode is active, the corresponding power control pin will be active.
15:6	Reserved

4.4.37 Sleep Mode Power Control Register (SLP-PC)

Index: 332H

Bit	Description	Name	Reset State
0	Power Control Sleep Mode [0]	PCSLP0	'1'
1	Power Control Sleep Mode [1]	PCSLP1	'1'
2	Power Control Sleep Mode [2]	PCSLP2	'1'
3	Power Control Sleep Mode [3]	PCSLP3	'0'
4	Power Control Sleep Mode [4]	PCSLP4	'0'
5	Power Control Sleep Mode [5]	PCSLP5	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
5:0	**Power Control Sleep Mode [5:0]:** If any bit is high and Sleep mode is active, the corresponding power control pin will be active.
15:6	Reserved

4.4.38 Suspend Mode Power Control Register (SPND-PC)

Index: 333H

Bit	Description	Name	Reset State
0	Power Control Suspend Mode [0]	PCSPND0	'1'
1	Power Control Suspend Mode [1]	PCSPND1	'1'
2	Power Control Suspend Mode [2]	PCSPND2	'1'
3	Power Control Suspend Mode [3]	PCSPND3	'0'
4	Power Control Suspend Mode [4]	PCSPND4	'0'
5	Power Control Suspend Mode [5]	PCSPND5	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
5:0	**Power Control Suspend Mode [5:0]:** If any bit is high and Suspend mode is active, the corresponding power control pin will be active.
15:6	Reserved

4.4.39 Doze Mode Timer Register (DZMT)

Index: 335H

Bit	Description	Name	Reset State
0	Doze Mode Timer One's Digit [0]	DZTMR1SEL0	'0'
1	Doze Mode Timer One's Digit [1]	DZTMR1SEL1	'0'
2	Doze Mode Timer One's Digit [2]	DZTMR1SEL2	'0'
3	Doze Mode Timer One's Digit [3]	DZTMR1SEL3	'0'
4	Doze Mode Timer Ten's Digit [0]	DZTMR10SEL0	'0'
5	Doze Mode Timer Ten's Digit [1]	DZTMR10SEL1	'0'
6	Doze Mode Timer Ten's Digit [2]	DZTMR10SEL2	'0'
7	Doze Mode Timer Clock Prescalar	DZTMR_PRESCALAR	'0'
8	Enable Doze Mode Timer to be Reset by Primary Activity	DZTMR_RSTPAEN	'1'
9	Doze Mode Timer Enable	DZTMR_EN	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**Doze Mode Timer One's Digit [3:0]:** When both one's and ten's digit are '0', the Doze mode timer will be disabled.

Bit [3:0]	One's Value
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

Bit	Description *(cont.)*
6:4	**Doze Mode Timer Ten's Digit [2:0]:** When both one's and ten's digit are '0', the Doze mode timer will be disabled.

Bit [3:0]	Ten's Value
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
All Others	Reserved

7	**Doze Mode Timer Clock Prescalar:** '0' = 100 ms; '1' = 1 s. **NOTE:** If 100 ms is used, the accuracy is within ± 100 ms. If 1s is used, the accuracy is within ± 1s.
8	**Enable Doze Mode Timer to be Reset by Primary Activity:** '0' = disable; '1' = enable.
9	**Doze Mode Timer Enable:** '0' = disable; '1' = enable.
15:10	Reserved

4.4.40 Sleep Mode Timer Register (SLPMT)

Index: 336H

Bit	Description	Name	Reset State
0	Sleep Mode Timer One's Digit [0]	SLPTMR1SEL0	'0'
1	Sleep Mode Timer One's Digit [1]	SLPTMR1SEL1	'0'
2	Sleep Mode Timer One's Digit [2]	SLPTMR1SEL2	'0'
3	Sleep Mode Timer One's Digit [3]	SLPTMR1SEL3	'0'
4	Sleep Mode Timer Ten's Digit [0]	SLPTMR10SEL0	'0'
5	Sleep Mode Timer Ten's Digit [1]	SLPTMR10SEL1	'0'
6	Sleep Mode Timer Ten's Digit [2]	SLPTMR10SEL2	'0'
7	Reserved		'0'
8	Reserved		'0'
9	Sleep Mode Timer Enable	SLPTMR_EN	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**Sleep Mode Timer One's Digit [3:0]:** When both one's and ten's digit are '0', the Sleep mode timer will be disabled.

Bit [3:0]	One's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

NOTE: The accuracy of the timer is within ± 1 min.

Bit	Description *(cont.)*
6:4	**Sleep Mode Timer Ten's Digit [2:0]:** When both one's and ten's digit are '0', the Sleep mode timer will be disabled.

Bit [3:0]	Ten's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
All Others	Reserved

8:7	Reserved
9	**Sleep Mode Timer Enable:** '0' = disable; '1' = enable.
15:10	Reserved

4.4.41 Suspend Mode Timer Register (SPNDMT)

Index: 337H

Bit	Description	Name	Reset State
0	Suspend Mode Timer One's Digit [0]	SPDTMR1SEL0	'0'
1	Suspend Mode Timer One's Digit [1]	SPDTMR1SEL1	'0'
2	Suspend Mode Timer One's Digit [2]	SPDTMR1SEL2	'0'
3	Suspend Mode Timer One's Digit [3]	SPDTMR1SEL3	'0'
4	Suspend Mode Timer Ten's Digit [0]	SPDTMR10SEL0	'0'
5	Suspend Mode Timer Ten's Digit [1]	SPDTMR10SEL1	'0'
6	Suspend Mode Timer Ten's Digit [2]	SPDTMR10SEL2	'0'
7	Reserved		'0'
8	Reserved		'0'
9	Suspend Mode Timer Enable	SPDTMR_EN	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Suspend Mode Timer One's Digit [3:0]:** When both one's and ten's digit are '0', the Suspend mode timer will be disabled.

Bit [3:0]	One's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

NOTE: The accuracy of the timer is within ± 1 min.

Bit	Description *(cont.)*
6:4	**Suspend Mode Timer Ten's Digit [2:0]:** When both one's and ten's digit are '0', the Suspend mode timer will be disabled.

Bit [3:0]	Ten's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
All Others	Reserved

NOTE: Tolerance is ± 3 minutes.

8:7	Reserved
9	**Suspend Mode Timer Enable:** '0' = disable; '1' = enable.
15:10	Reserved

4.4.42 Secondary Activity Timer Register (SAT)

Index: 338H

Bit	Description	Name	Reset State
0	Secondary Activity Timer One's Digit [0]	SATMR1SEL0	'0'
1	Secondary Activity Timer One's Digit [1]	SATMR1SEL1	'0'
2	Secondary Activity Timer One's Digit [2]	SATMR1SEL2	'0'
3	Secondary Activity Timer One's Digit [3]	SATMR1SEL3	'0'
4	Secondary Activity Timer Ten's Digit [0]	SATMR10SEL0	'0'
5	Secondary Activity Timer Ten's Digit [1]	SATMR10SEL1	'0'
6	Secondary Activity Timer Ten's Digit [2]	SATMR10SEL2	'0'
7	Secondary Activity Timer Clock Prescalar	SATMR_PRESCALAR	'0'
8	Reset Secondary Activity on SMI	RST_SA_ON_SMI	'0'
9	Secondary Activity Timer Enable	SATMR_EN	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**Secondary Activity Timer One's Digit [3:0]:** When both one's and ten's digit are '0', the secondary activity timer will be disabled. The timer is used to extend the revive time due to a S/A source.

Bit [3:0]	One's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

Bit	Description *(cont.)*
6:4	**Secondary Activity Timer Ten's Digit [2:0]:** When both one's and ten's digit are '0', the secondary activity timer will be disabled. The timer is used to extend the revive time due to a S/A source.

Bit [3:0]	Ten's Value
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
All Others	Reserved

7	**Secondary Activity Timer Clock Prescalar:** '0' = 100 µs; '1' = 1 ms. **NOTE:** If the 100-µs option is used, the accuracy of the timer is within ± 100 µs. If the 1-ms option is used, the accuracy of the timer is within ±1 ms.
8	**Reset Secondary Activity on SMI:** Writing a '1' to this bit will initiate a single pulse which resets secondary activity on SMI.
9	**Secondary Activity Timer Enable:** '0' = disable; '1' = enable.
15:10	Reserved

4.4.43 Power on Demand Primary Activity Timer Register (POD_PAT)

Index: 339H

Bit	Description	Name	Reset State
0	Primary Activity Timer One's Digit [0]	PATMR1SEL0	'0'
1	Primary Activity Timer One's Digit [1]	PATMR1SEL1	'0'
2	Primary Activity Timer One's Digit [2]	PATMR1SEL2	'0'
3	Primary Activity Timer One's Digit [3]	PATMR1SEL3	'0'
4	Primary Activity Timer Ten's Digit [0]	PATMR10SEL0	'0'
5	Primary Activity Timer Ten's Digit [1]	PATMR10SEL1	'0'
6	Primary Activity Timer Ten's Digit [2]	PATMR10SEL2	'0'
7	Primary Activity Timer Clock Prescalar	PATMR_PRESCALAR	'0'
8	Reserved		'0'
9	Primary Activity Timer Enable	PATMR_EN	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**Primary Activity Timer One's Digit [3:0]:** This timer is used to extend the time due to a P/A occurrence during which POD (Power on Demand) will be blocked. **NOTE:** This P/A will not affect the timers or power management modes.

Bit [3:0]	One's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

Bit	Description *(cont.)*
6:4	**Primary Activity Timer Ten's Digit [2:0]:** When both one's and ten's digit are '0', the primary activity timer will be disabled.

Bit [3:0]	Ten's Value (minutes)
0H	0
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
All Others	Reserved

Bit	Description *(cont.)*
7	**Primary Activity Timer Clock Prescalar:** '0' = 100 µs; '1' = 1 ms. **NOTE:** If the 100-µs option is used, the accuracy of the timer is within ± 100 µs. If the 1-ms option is used, the accuracy of the timer is within ±1 ms.
8	Reserved
9	**Primary Activity Timer Enable:** '0' = disable; '1' = enable.
15:10	Reserved

4.4.44 General Purpose Control Register (GPC)

Index: 340H

Bit	Description	Name	Reset State
0	General Purpose I/O Data [0]	GPIODATA0	'0'
1	General Purpose I/O Data [1]	GPIODATA1	'0'
2	General Purpose I/O Data [2]	GPIODATA2	'0'
3	General Purpose I/O Data [3]	GPIODATA3	'0'
4	General Purpose I/O Data [4]	GPIODATA4	'0'
5	General Purpose I/O Data [5]	GPIODATA5	'0'
6	Reserved		'0'
7	Reserved		'0'
8	General Purpose I/O Direction [0]	GPIODIR0	'0'
9	General Purpose I/O Direction [1]	GPIODIR1	'0'
10	General Purpose I/O Direction [2]	GPIODIR2	'0'
11	General Purpose I/O Direction [3]	GPIODIR3	'0'
12	General Purpose I/O Direction [4]	GPIODIR4	'0'
13	General Purpose I/O Direction [5]	GPIODIR5	'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
5:0	**General Purpose I/O Data [5:0]:** When the corresponding GPIODIR for each bit is low, a read of the bit returns the state of the GPIO pin and a write has no effect. When GPIODIR is high, a read returns the value last written and a write sets the GPIO output to the value written.
7:6	Reserved
13:8	**General Purpose I/O Direction [5:0]:** When low, GPIO is an input pin; when high, GPIO is an output pin.
15:14	Reserved

4.4.45 General Purpose Counter/Timer Control Register (GP_CNTMRC)

Index: 341H

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Reserved		'0'
2	Reserved		'0'
3	Reserved		'0'
4	GP Counter/Timer Clock Select	GPCT_CLKSEL	'0'
5	GP Counter/Timer Select [0]	GPCTSEL0	'0'
6	GP Counter/Timer Select [1]	GPCTSEL1	'0'
7	GP Counter/Timer Enable	GPCTEN	'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	Reserved
4	**General Purpose Counter/Timer Clock Select:** When low, a 1-Hz clock will be used to feed into the general purpose counter/timer. When high, a 32-kHz clock will be used to feed into the general purpose counter/timer.
6:5	**General Purpose Counter/Timer Select [1:0]:** When either counter is enabled, GPIO3 will be enabled as the counter clock. When the 1-s timer is enabled, a 1-Hz clock will be enabled. When the 1-min. timer is enabled, a 1-min. clock will be enabled.

Bit [1:0]	GPCT_CLKSEL = 0	GPCT_CLKSEL = 1
'00'	16-bit counter	16-bit counter
'01'	24-bit counter	24-bit counter
'10'	1-second timer	31.25-µs timer
'11'	1-minute timer	1.875-ms timer

7	**General Purpose Counter/Timer Enable:** When high, the general purpose counter/timer will be enabled; when low it will be disabled.
15:8	Reserved

4.4.46 General Purpose Counter/Timer Current Value Register (GP_CNTMR_VAL)

Index: 342H

Bit	Description	Name	Reset State
0	General Purpose Counter/Timer [0]	GPCT0	'0'
1	General Purpose Counter/Timer [1]	GPCT1	'0'
2	General Purpose Counter/Timer [2]	GPCT2	'0'
3	General Purpose Counter/Timer [3]	GPCT3	'0'
4	General Purpose Counter/Timer [4]	GPCT4	'0'
5	General Purpose Counter/Timer [5]	GPCT5	'0'
6	General Purpose Counter/Timer [6]	GPCT6	'0'
7	General Purpose Counter/Timer [7]	GPCT7	'0'
8	General Purpose Counter/Timer [8]	GPCT8	'0'
9	General Purpose Counter/Timer [9]	GPCT9	'0'
10	General Purpose Counter/Timer [10]	GPCT10	'0'
11	General Purpose Counter/Timer [11]	GPCT11	'0'
12	General Purpose Counter/Timer [12]	GPCT12	'0'
13	General Purpose Counter/Timer [13]	GPCT13	'0'
14	General Purpose Counter/Timer [14]	GPCT14	'0'
15	General Purpose Counter/Timer [15]	GPCT15	'0'

Bit	Description
15:0	**General Purpose Counter/Timer [15:0]:** Reading this register returns the lower byte of the current value of the general purpose counter/timer. When the 24-bit counter is enabled, these bits represent counter bits [23:8]; otherwise they represent counter/timer bits [15:0]. Any write to this register will reset the entire counter/timer.

4.4.47 General Purpose Counter/Timer Compare Register (GP_CNTMR_CMP)

Index: 343H

Bit	Description	Name	Reset State
0	General Purpose Counter/Timer Compare [0]	GPTMRCMP0	'0'
1	General Purpose Counter/Timer Compare [1]	GPTMRCMP1	'0'
2	General Purpose Counter/Timer Compare [2]	GPTMRCMP2	'0'
3	General Purpose Counter/Timer Compare [3]	GPTMRCMP3	'0'
4	General Purpose Counter/Timer Compare [4]	GPTMRCMP4	'0'
5	General Purpose Counter/Timer Compare [5]	GPTMRCMP5	'0'
6	General Purpose Counter/Timer Compare [6]	GPTMRCMP6	'0'
7	General Purpose Counter/Timer Compare [7]	GPTMRCMP7	'0'
8	General Purpose Counter/Timer Compare [8]	GPTMRCMP8	'0'
9	General Purpose Counter/Timer Compare [9]	GPTMRCMP9	'0'
10	General Purpose Counter/Timer Compare [10]	GPTMRCMP10	'0'
11	General Purpose Counter/Timer Compare [11]	GPTMRCMP11	'0'
12	General Purpose Counter/Timer Compare [12]	GPTMRCMP12	'0'
13	General Purpose Counter/Timer Compare [13]	GPTMRCMP13	'0'
14	General Purpose Counter/Timer Compare [14]	GPTMRCMP14	'0'
15	General Purpose Counter/Timer Compare [15]	GPTMRCMP15	'0'

Bit	Description
15:0	**General Purpose Counter/Timer Compare [15:0]:** These bits represent the compare value at which the general purpose counter/timer will trigger an interrupt if the corresponding SMI is unmasked. If a 24-bit counter is enabled, these bits represent compare value bits [23:8].

4.4.48 Device Timer 0 Time-out Register (DTT0)

Index: 344H

Bit	Description	Name	Reset State
0	Device Timer 0 Time-out Select [0]	DEVTMR0SEL0	'0'
1	Device Timer 0 Time-out Select [1]	DEVTMR0SEL1	'0'
2	Device Timer 0 Time-out Select [2]	DEVTMR0SEL2	'0'
3	Device Timer 0 Time-out Select [3]	DEVTMR0SEL3	'0'
4	Device Timer 0 Time-out Prescalar [0]	DEVTMR0PRES0	'0'
5	Device Timer 0 Time-out Prescalar [1]	DEVTMR0PRES1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Device Timer 0 Time-out Select [3:0]:**

Bit [3:0]	Time-out
0H	Disable
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

5:4 **Device Timer 0 Time-out Prescalar [1:0]:**

Bit [1:0]	Prescale	Accuracy
'00'	1 s	± 1 s
'01'	10 s	± 1 s
'10'	1 min.	± 10 s
'11'	10 min	± 1 min
All Others	Reserved	

15:6 Reserved

4.4.49 Device Timer 1 Time-out Register (DTT1)

Index: 345H

Bit	Description	Name	Reset State
0	Device Timer 1 Time-out Select [0]	DEVTMR1SEL0	'0'
1	Device Timer 1 Time-out Select [1]	DEVTMR1SEL1	'0'
2	Device Timer 1 Time-out Select [2]	DEVTMR1SEL2	'0'
3	Device Timer 1 Time-out Select [3]	DEVTMR1SEL3	'0'
4	Device Timer 1 Time-out Prescalar [0]	DEVTMR1PRES0	'0'
5	Device Timer 1 Time-out Prescalar [1]	DEVTMR1PRES1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Device Timer 1 Time-out Select [3:0]:**

Bit [3:0]	Time-out
0H	Disable
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

5:4 **Device Timer 1 Time-out Prescalar [1:0]:**

Bit [1:0]	Prescale	Accuracy
'00'	1 s	± 1 s
'01'	10 s	± 1 s
'10'	1 min.	± 10 s
'11'	10 min	± 1 min
All Others	Reserved	

15:6 Reserved

4.4.50 Device Timer 2 Time-out Register (DTT2)

Index: 346H

Bit	Description	Name	Reset State
0	Device Timer 2 Time-out Select [0]	DEVTMR2SEL0	'0'
1	Device Timer 2 Time-out Select [1]	DEVTMR2SEL1	'0'
2	Device Timer 2 Time-out Select [2]	DEVTMR2SEL2	'0'
3	Device Timer 2 Time-out Select [3]	DEVTMR2SEL3	'0'
4	Device Timer 2 Time-out Prescalar [0]	DEVTMR2PRES0	'0'
5	Device Timer 2 Time-out Prescalar [1]	DEVTMR2PRES1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Device Timer 2 Time-out Select [3:0]:**

Bit [3:0]	Time-out
0H	Disable
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

5:4 **Device Timer 2 Time-out Prescalar [1:0]:**

Bit [1:0]	Prescale	Accuracy
'00'	1 s	± 1 s
'01'	10 s	± 1 s
'10'	1 min.	± 10 s
'11'	10 min	± 1 min
All Others	Reserved	

15:6 Reserved

4.4.51 Device Timer 3 Time-out Register (DTT3)

Index: 347H

Bit	Description	Name	Reset State
0	Device Timer 3 Time-out Select [0]	DEVTMR3SEL0	'0'
1	Device Timer 3 Time-out Select [1]	DEVTMR3SEL1	'0'
2	Device Timer 3 Time-out Select [2]	DEVTMR3SEL2	'0'
3	Device Timer 3 Time-out Select [3]	DEVTMR3SEL3	'0'
4	Device Timer 3 Time-out Prescalar [0]	DEVTMR3PRES0	'0'
5	Device Timer 3 Time-out Prescalar [1]	DEVTMR3PRES1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Device Timer 3 Time-out Select [3:0]:**

Bit [3:0]	Time-out
0H	Disable
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

5:4 **Device Timer 3 Time-out Prescalar [1:0]:**

Bit [1:0]	Prescale	Accuracy
'00'	1 s	± 1 s
'01'	10 s	± 1 s
'10'	1 min.	± 10 s
'11'	10 min	± 1 min
All Others	Reserved	

15:6 Reserved

4.4.52 Device Timer 4 Time-out Register (DTT4)

Index: 348H

Bit	Description	Name	Reset State
0	Device Timer 4 Time-out Select [0]	DEVTMR4SEL0	'0'
1	Device Timer 4 Time-out Select [1]	DEVTMR4SEL1	'0'
2	Device Timer 4 Time-out Select [2]	DEVTMR4SEL2	'0'
3	Device Timer 4 Time-out Select [3]	DEVTMR4SEL3	'0'
4	Device Timer 4 Time-out Prescalar [0]	DEVTMR4PRES0	'0'
5	Device Timer 4 Time-out Prescalar [1]	DEVTMR4PRES1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Device Timer 4 Time-out Select [3:0]:**

Bit [3:0]	Time-out
0H	Disable
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

5:4 **Device Timer 4 Time-out Prescalar [1:0]:**

Bit [1:0]	Prescale	Accuracy
'00'	1 s	± 1 s
'01'	10 s	± 1 s
'10'	1 min.	± 10 s
'11'	10 min	± 1 min
All Others	Reserved	

15:6 Reserved

4.4.53 Device Timer 5 Time-out Register (DTT5)

Index: 349H

Bit	Description	Name	Reset State
0	Device Timer 5 Time-out Select [0]	DEVTMR5SEL0	'0'
1	Device Timer 5 Time-out Select [1]	DEVTMR5SEL1	'0'
2	Device Timer 5 Time-out Select [2]	DEVTMR5SEL2	'0'
3	Device Timer 5 Time-out Select [3]	DEVTMR5SEL3	'0'
4	Device Timer 5 Time-out Prescalar [0]	DEVTMR5PRES0	'0'
5	Device Timer 5 Time-out Prescalar [1]	DEVTMR5PRES1	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

3:0 **Device Timer 5 Time-out Select [3:0]:**

Bit [3:0]	Time-out
0H	Disable
1H	1
2H	2
3H	3
4H	4
5H	5
6H	6
7H	7
8H	8
9H	9
All Others	Reserved

5:4 **Device Timer 5 Time-out Prescalar [1:0]:**

Bit [1:0]	Prescale	Accuracy
'00'	1 s	± 1 s
'01'	10 s	± 1 s
'10'	1 min.	± 10 s
'11'	10 min.	± 1 min
All Others	Reserved	

15:6 Reserved

4.4.54 Device Timer Time-out Source Register 1 (DTTS1)

Index: 34AH

Bit	Description	Name	Reset State
0	Video Activity Device Timer Select [0]	VD_TMRSEL0	'0'
1	Video Activity Device Timer Select [1]	VD_TMRSEL1	'0'
2	Video Activity Device Timer Select [2]	VD_TMRSEL2	'0'
3	Hard Drive 1 Activity Device Timer Select [0]	HD1_TMRSEL0	'0'
4	Hard Drive 1 Activity Device Timer Select [1]	HD1_TMRSEL1	'0'
5	Hard Drive 1 Activity Device Timer Select [2]	HD1_TMRSEL2	'0'
6	Hard Drive 2 Activity Device Timer Select [0]	HD2_TMRSEL0	'0'
7	Hard Drive 2 Activity Device Timer Select [1]	HD2_TMRSEL1	'0'
8	Hard Drive 2 Activity Device Timer Select [2]	HD2_TMRSEL2	'0'
9	Floppy Activity Device Timer Select [0]	FD_TMRSEL0	'0'
10	Floppy Activity Device Timer Select [1]	FD_TMRSEL1	'0'
11	Floppy Activity Device Timer Select [2]	FD_TMRSEL2	'0'
12	Keyboard Activity Device Timer Select [0]	KB_TMRSEL0	'0'
13	Keyboard Activity Device Timer Select [1]	KB_TMRSEL1	'0'
14	Keyboard Activity Device Timer Select [2]	KB_TMRSEL2	'0'
15	Reserved		'0'

Bit **Description**

2:0 **Video Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by video activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

5:3 **Hard Drive 1 Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by hard drive 1 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

Bit	Description *(cont.)*
8:6	**Hard Drive 2 Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by hard drive 2 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

Bit	Description *(cont.)*
11:9	**Floppy Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by floppy activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

Bit	Description *(cont.)*
14:12	**Keyboard Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by keyboard activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

Bit	Description *(cont.)*
15	Reserved

4.4.55 Device Timer Time-out Source Register 2 (DTTS2)

Index: 34BH

Bit	Description	Name	Reset State
0	Serial Port 1 Activity Device Timer Select [0]	SIO1_TMRSEL0	'0'
1	Serial Port 1 Activity Device Timer Select [1]	SIO1_TMRSEL1	'0'
2	Serial Port 1 Activity Device Timer Select [2]	SIO1_TMRSEL2	'0'
3	Serial Port 2 Activity Device Timer Select [0]	SIO2_TMRSEL0	'0'
4	Serial Port 2 Activity Device Timer Select [1]	SIO2_TMRSEL1	'0'
5	Serial Port 2 Activity Device Timer Select [2]	SIO2_TMRSEL2	'0'
6	Parallel Port Activity Device Timer Select [0]	PIO_TMRSEL0	'0'
7	Parallel Port Activity Device Timer Select [1]	PIO_TMRSEL1	'0'
8	Parallel Port Activity Device Timer Select [2]	PIO_TMRSEL2	'0'
9	Programmable Range 0 Activity Timer Select [0]	P0_TMRSEL0	'0'
10	Programmable Range 0 Activity Timer Select [1]	P0_TMRSEL1	'0'
11	Programmable Range 0 Activity Timer Select [2]	P0_TMRSEL2	'0'
12	Programmable Range 1 Activity Timer Select [0]	P1_TMRSEL0	'0'
13	Programmable Range 1 Activity Timer Select [1]	P1_TMRSEL1	'0'
14	Programmable Range 1 Activity Timer Select [2]	P1_TMRSEL2	'0'
15	Reserved		'0'

Bit **Description**

2:0 **Serial Port 1 Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by serial port 1 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

5:3 **Serial Port 2 Activity Device Timer Time-out Select [2:0]:** These bits select which device timer time-out will be reset by serial port 2 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

Bit	Description *(cont.)*
8:6	**Parallel Port Activity Device Timer Select [2:0]:** These bits select which device timer time-out will be reset by parallel port activity. **Bit [2:0]** — **Timer** '000' — None '001' — 0 '010' — 1 '011' — 2 '100' — 3 '101' — 4 '110' — 5 '111' — Reserved
11:9	**Programmable Range 0 Activity Device Timer Select [2:0]:** These bits select which device timer time-out will be reset by programmable range 0 activity. **Bit [2:0]** — **Timer** '000' — None '001' — 0 '010' — 1 '011' — 2 '100' — 3 '101' — 4 '110' — 5 '111' — Reserved
14:12	**Programmable Range 1 Activity Timer Select [2:0]:** These bits select which device timer time-out will be reset by programmable range 1 activity. **Bit [2:0]** — **Timer** '000' — None '001' — 0 '010' — 1 '011' — 2 '100' — 3 '101' — 4 '110' — 5 '111' — Reserved
15	Reserved

4.4.56 Device Timer Time-out Source Register 3 (DTTS3)

Index: 34CH

Bit	Description	Name	Reset State
0	Programmable Range 2 Activity Timer Select [0]	P2_TMRSEL0	'0'
1	Programmable Range 2 Activity Timer Select [1]	P2_TMRSEL1	'0'
2	Programmable Range 2 Activity Timer Select [2]	P2_TMRSEL2	'0'
3	Programmable Range 3 Activity Timer Select [0]	P3_TMRSEL0	'0'
4	Programmable Range 3 Activity Timer Select [1]	P3_TMRSEL1	'0'
5	Programmable Range 3 Activity Timer Select [2]	P3_TMRSEL2	'0'
6	Programmable Range 4 Activity Timer Select [0]	P4_TMRSEL0	'0'
7	Programmable Range 4 Activity Timer Select [1]	P4_TMRSEL1	'0'
8	Programmable Range 4 Activity Timer Select [2]	P4_TMRSEL2	'0'
9	Programmable Range 5 Activity Timer Select [0]	P5_TMRSEL0	'0'
10	Programmable Range 5 Activity Timer Select [1]	P5_TMRSEL1	'0'
11	Programmable Range 5 Activity Timer Select [2]	P5_TMRSEL2	'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

2:0 **Programmable Range 2 Activity Timer Select [2:0]:** These bits select which device timer time-out will be reset by programmable range 2 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

5:3 **Programmable Range 3 Activity Timer Select [2:0]:** These bits select which device timer time-out will be reset by programmable range 3 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

Bit	Description *(cont.)*
8:6	**Programmable Range 4 Activity Timer Select [2:0]:** These bits select which device timer time-out will be reset by programmable range 4 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

Bit	Description *(cont.)*
11:9	**Programmable Range 5 Activity Timer Select [2:0]:** These bits select which device timer time-out will be reset by programmable range 5 activity.

Bit [2:0]	Timer
'000'	None
'001'	0
'010'	1
'011'	2
'100'	3
'101'	4
'110'	5
'111'	Reserved

Bit	Description *(cont.)*
15:12	Reserved

4.4.57 Device Timer Time-out Source Register 4 (DTTS4)

Index: 34DH

Bit	Description	Name	Reset State
0	EXTACT0 Device Timer Select [0]	EXT0_TMRSEL0	'0'
1	EXTACT0 Device Timer Select [1]	EXT0_TMRSEL1	'0'
2	EXTACT0 Device Timer Select [2]	EXT0_TMRSEL2	'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
2:0	**EXTACT0 Device Timer Select [2:0]:** These bits select which device timer time-out will be reset by EXTACT0 activity. **Bit [2:0]** / **Timer** '000' None '001' 0 '010' 1 '011' 2 '100' 3 '101' 4 '110' 5 '111' Reserved
15:3	Reserved

4.4.58 LED Indicator Control Register (LEDIC)

Index: 350H

Bit	Description	Name	Reset State
0	LED0 Flasher Enable	LED0FLSHEN	'0'
1	LED0 Flash Rate Selects [0]	FLSHRAT0	'0'
2	LED0 Flash Rate Selects [1]	FLSHRAT1	'0'
3	LED0 Flash Duration [0]	FLSHDUR0	'0'
4	LED0 Flash Duration [1]	FLSHDUR1	'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	LED1 Flasher Enable	LED1FSH	'0'
9	LED1 Flash Rate Selects [0]	LED1RAT0	'0'
10	LED1 Flash Rate Selects [1]	LED1RAT1	'0'
11	LED1 Flash Duration [0]	LED1DUR0	'0'
12	LED1 Flash Duration [1]	LED1DUR1	'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit — **Description**

0 — **LED0 Flasher Enable:** '1' = enable; '0' = disable.

2:1 — **LED0 Flash Rate Selects [2:0]:** These bits control the flash rate of the LED0 flasher output while LED0FLSH is high.

NOTE: When the flash rate is 2H, the flash duration cannot be set to 0H; when the flash rate is 3H, the flash duration cannot be set to 0H or 1H.

Bit [1:0]	LED Flash Rate
0H	0.5 Hz
1H	1 Hz
2H	2 Hz
3H	4 Hz

4:3 — **LED0 Flash Duration:** These bits control the duration of the flasher pulses while LED0FLSH is high.

Bit [1:0]	Flash Duration
0H	256 ms
1H	128 ms
2H	62.5 ms
3H	31.25 ms

NOTE: When the flash rate is 2H, the flash duration cannot be set to 0H; when the flash rate is 3H, the flash duration cannot be set to 0H or 1H.

7:5 — Reserved

Bit	Description *(cont.)*
8	**LED1 Flasher Enable:** '1' = enable; '0' = disable.
10:9	**LED1 Flash Rate Selects [1:0]:** These bits control the flash rate of the suspend LED flasher output while LED1FLSH is high. **Bit [1:0]** — **LED Flash Rate** 0H — 0.5 Hz 1H — 1 Hz 2H — 2 Hz 3H — 4 Hz
12:11	**LED1 Flash Duration:** These bits control the duration of the suspend flasher pulses while LED1FLSH is high. **Bit [1:0]** — **Flash Duration** 0H — 256 ms 1H — 128 ms 2H — 62.5 ms 3H — 31.25 ms **NOTE:** When the flash rate is 2H, the flash duration cannot be set to 0H; when the flash rate is 3H, the flash duration cannot be set to 0H or 1H.
15:13	Reserved

4.4.59 Leakage Control Register (LC)

Index: 351H

Bit	Description	Name	Reset State
0	Enable Input Leakage Control	EN_INPUT_LC	'0'
1	Enable Output Leakage Control	EN_OUTPUT_LC	'0'
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Enable Input Leakage Control During 5-V Suspend:** '0' = disable; '1' = enable.
1	**Enable Output Leakage Control During 5-V Suspend:** '0' = disable; '1' = enable.
15:2	Reserved

In V1-LS, when the system enters the STR mode, all signals (except DRAM, PCx, GPIOx, and PM inputs) are leakage-controlled. Leakage control implies:

(i) Input: Isolated from external node; internal node is driven to inactive state.

(ii) Output: Tristated.

(iii) I/O: Output buffer is tristated while input buffer is isolated from external and internal nodes driven to inactive state.

A floating input will not cause leakage current to a leakage-controlled input buffer.

4.4.60 Pin Multiplexing Control Register (PINMUX)

Index: 352H

Bit	Description	Name	Reset State
0	GPIO0 Function [0]	GPIO0_FUNC0	'0'
1	GPIO0 Function [1]	GPIO0_FUNC1	'0'
2	GPIO1 Function [0]	GPIO1_FUNC0	'0'
3	GPIO1 Function [1]	GPIO1_FUNC1	'0'
4	GPIO2 Function [0]	GPIO2_FUNC0	'0'
5	GPIO2 Function [1]	GPIO2_FUNC1	'0'
6	GPIO3 Function [0]	GPIO3_FUNC0	'0'
7	GPIO3 Function [1]	GPIO3_FUNC1	'0'
8	GPIO4 Function [0]	GPIO4_FUNC0	'0'
9	GPIO4 Function [1]	GPIO4_FUNC1	'0'
10	GPIO5 Function [0]	GPIO5_FUNC0	'0'
11	GPIO5 Function [1]	GPIO5_FUNC1	'0'
12	Reserved		'0'
13	PC3 Function	PC3_FUNC	'0'
14	PC4 Function	PC4_FUNC	'0'
15	PC5 Function	PC5_FUNC	'0'

Bit **Description**

1:0 **GPIO0 Function [1:0]:**

Bit [1:0]	Function
'00'	GPIO0
'01'	LED0 output
'10'	FLOAT_REQ# input (Rev. BB and later silicon)
'11'	Reserved

3:2 **GPIO1 Function [1:0]:**

Bit [1:0]	Function
'00'	GPIO1
'01'	LED1 output
'10'	FLOAT_GNT# output (Rev. BB and later silicon)
'11'	Reserved

5:4 **GPIO2 Function [1:0]:**

Bit [1:0]	Function
'00'	GPIO2
'01'	DDMA_RETRY input
'10'	DPSLP_IRQPA input
'11'	Reserved

Bit	Description *(cont.)*
7:6	**GPIO3 Function [1:0]:** **Bit [1:0]** — **Function** '00' — GPIO3 '01' — SUPPRESS_RESUME input '10' — Reserved '11' — Reserved
9:8	**GPIO4 Function [1:0]:** **Bit [1:0]** — **Function** '00' — GPIO4 '01' — Reserved '10' — SUSPA# input (Rev. BB and later silicon) '11' — Reserved
11:10	**GPIO5 Function [1:0]:** **Bit [1:0]** — **Function** '00' — GPIO5 '01' — Reserved '10' — THERM input active-high '11' — THERM input active-low
12	Reserved
13	**PC3 Function:** '0' = PC3; '1' = LED0 output.
14	**PC4 Function:** '0' = PC4; '1' = LED1 output.
15	**PC5 Function:** '0' = PC5; '1' = Reserved

4.4.61 Debounce Control Register (DBC)

Index: 353H

Bit	Description	Name	Reset State
0	SWTCH Debounce Select	SWTCH_DBSEL	'1'
1	WAKE0 Debounce Select	WAKE0_DBSEL	'1'
2	WAKE1 Debounce Select	WAKE1_DBSEL	'1'
3	RING Debounce Select	RING_DBSEL	'1'
4	EXTACT0 Debounce Select	EXT0_DBSEL	'1'
5	Reserved		'1'
6	Reserved		'1'
7	Reserved		'1'
8	Reserved		'1'
9	Reserved		'1'
10	Reserved		'1'
11	Reserved		'1'
12	Reserved		'1'
13	Reserved		'1'
14	Reserved		'1'
15	Reserved		'1'

Bit	Description
0	**SWTCH Debounce Select:** When low, debounce period will be 0 s. When high, debounce period will be 20 ms.
1	**WAKE0 Debounce Select:** When low, debounce period will be 0 s. When high, debounce period will be 20 ms.
2	**WAKE1 Debounce Select:** When low, debounce period will be 0 s. When high, debounce period will be 20 ms.
3	**RING Debounce Select:** When low, debounce period will be 0 s. When high, debounce period will be 20 ms.
4	**EXTACT0 Debounce Select:** When low, debounce period will be 0 s. When high, debounce period will be 20 ms.
15:5	Reserved

4.4.62 Edge Detect Control Register (EDC)

Index: 354H

Bit	Description	Name	Reset State
0	SWTCH Edge Detect [0]	SWTCHEGDT0	'0'
1	SWTCH Edge Detect [1]	SWTCHEGDT1	'1'
2	WAKE0 Edge Detect [0]	WAKE0EGDT0	'0'
3	WAKE0 Edge Detect [1]	WAKE0EGDT1	'1'
4	WAKE1 Edge Detect [0]	WAKE1EGDT0	'0'
5	WAKE1 Edge Detect [1]	WAKE1EGDT1	'1'
6	RING Edge Detect [0]	RINGEGDT0	'0'
7	RING Edge Detect [1]	RINGEGDT1	'1'
8	EXTACT0 Edge Detect [0]	EXTACT0EGDT0	'0'
9	EXTACT0 Edge Detect [1]	EXTACT0EGDT1	'1'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
1:0	**SWTCH Edge Detect [1:0]:**

Bit [1:0]	Edge Detect
'00'	Reserved
'01'	Falling
'10'	Rising
'11'	Rising and falling

Bit	Description
3:2	**WAKE0 Edge Detect [1:0]:**

Bit [1:0]	Edge Detect
'00'	Reserved
'01'	Falling
'10'	Rising
'11'	Rising and falling

Bit	Description
5:4	**WAKE1 Edge Detect [1:0]:**

Bit [1:0]	Edge Detect
'00'	Reserved
'01'	Falling
'10'	Rising
'11'	Rising and falling

Bit	Description *(cont.)*
7:6	**RING Edge Detect [1:0]:** **Bit [1:0]** — **Edge Detect** '00' — Reserved '01' — Falling '10' — Rising '11' — Reserved
9:8	**EXTACT0 Edge Detect [1:0]:** **Bit [1:0]** — **Edge Detect** '00' — Reserved '01' — Falling '10' — Rising '11' — Rising and falling
15:10	Reserved

NOTE: Edge Detect Register selects the edge that is detected as toggling to trigger either a primary activity, secondary activity, SMI or Wakeup events.

4.5 Level-2 Cache Registers

4.5.1 Level-2 Cache Configuration Register (L2C)

Index: 400H

Bit	Description	Name	Reset State
0	L2 Cache Enable	L2EN	'0'
1	L2 Cache Size Select [0]	L2SIZE0	'1'
2	L2 Cache Size Select [1]	L2SIZE1	'0'
3	L2 Cache Size Select [2]	L2SIZE2	'0'
4	L2 Cache Type [0]	L2TYPE0	'0'
5	L2 Cache Type [1]	L2TYPE1	'0'
6	Reserved		'0'
7	Enable Pipelined Burst SRAM	EN_PIPE_SRAM	'0'
8	Select NALE Mode	SEL_NALE	'0'
9	Enable TAG Initialization	EN_TAG_INIT	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit — **Description**

0 — **L2 Cache Enable:** '0' = disable; '1' = enable.

3:1 — **L2 Cache Size Select:**

Bit [2:0]	L2 Cache Size
'000'	128 Kbytes
'001'	256 Kbytes
'010'	512 Kbytes
'011'	1 Mbyte
All others	Reserved

5:4 — **L2 Cache Type [1:0]:**

Bit [2:0]	L2 Cache Type
'00'	Standard asynchronous
'01'	Standard synchronous (both sync burst and pipelined burst)
'10'	Reserved
'11'	Reserved

6 — Reserved

7 — **Enable Pipelined Burst SRAM:** '0' = disable; '1' = enable. This bit is effective only if bit [5:4] = 01H.

Bit	Description *(cont.)*
8	**Select NALE Mode:** '0' = TAGCS#/NALE# pin is in TAGCS# mode. '1' = TAGCS#/NALE# pin is in NALE# mode.
9	**Enable TAG Initialization:** '0' = disable; '1' = enable.
15:10	Reserved

4.5.2 Level-2 Cache Timing Register (L2T)

Index: 401H

Bit	Description	Name	Reset State
0	L2 Cache Read Leadoff [0]	L2RDLDOF0	'0'
1	L2 Cache Read Leadoff [1]	L2RDLDOF1	'0'
2	L2 Cache Read Follow-on [0]	L2RDFLWON0	'0'
3	L2 Cache Read Follow-on [1]	L2RDFLWON1	'0'
4	L2 Cache Write Leadoff [0]	L2WRLDOF0	'0'
5	L2 Cache Write Leadoff [1]	L2WRLDOF1	'0'
6	L2 Cache Write Follow-on [0]	L2WRFLWON0	'0'
7	L2 Cache Write Follow-on [1]	L2WRFLWON1	'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit **Description**

1:0 **L2 Cache Read Leadoff:**

Bit [1:0]	Cycle Time
'00'	2T
'01'	3T
'10'	4T
'11'	Reserved

3:2 **L2 Cache Read Follow-on:**

Bit [1:0]	Cycle Time
'00'	1T
'01'	Reserved
'10'	Reserved
'11'	Reserved

5:4 **L2 Cache Write Leadoff:**

Bit [1:0]	Cycle Time
'00'	2T
'01'	3T
'10'	4T
'11'	Reserved

Bit	Description *(cont.)*
7:6	**L2 Cache Write Follow-on:** **Bit [1:0]** — **Cycle Time** '00' — 1T '01' — Reserved '10' — Reserved '11' — Reserved
15:8	Reserved

4.5.3 Level-2 Cache Miscellaneous Register (L2M)

Index: 402H

Bit	Description	Name	Reset State
0	Dead Clock Enable	DEAD_CLK_EN	'0'
1	Disable Invalidation of ROM Address	DIS_INVD_ROM_ ADDR	'0'
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Advanced Synchronous Power Enhanced Cache Timing (ASPECT)	ASPECT	'0'
7	Disable Power Management on CE# only for 50-MHz Operation	DIS_CE_PM	'0'
8	Enable the Pipeline of Memory Read-Miss Cycle [0]	EN_PIPE_RDMISS0	'0'
9	Enable the Pipeline of Memory Read-Miss Cycle [1]	EN_PIPE_RDMISS1	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Dead Clock Enable:** When set to '0', there is no dead clock when there is a L2 read followed by a L2 write or vice versa. When '1', a dead clock will be inserted whenever there is a L2 read followed by a L2 write or vice versa.
1	**Disable Invalidation of ROM address:** '0' = enable; '1' = disable.
5:2	Reserved
6	**Advanced Synchronous Power Enhanced Cache Timing (ASPECT):** When enabled, clock to L2-cache will be turned off during bus idle condition. '0' = disable; '1' = enable.
7	**Disable Power Management on CE# only for 50-MHz Operation:** '0' = enable; '1' = disable.

Bit	Description *(cont.)*
9:8	**Enable the Pipeline of Memory Read-Miss Cycle [1:0]:** **Bit [1:0] — Mode** 'X0' (Rev. BB and later) — Disable Pipeline on Read-Miss Cycle '01' (Rev. BB and later) — Enable Pipeline on Read-Miss Cycle; 'NA' will be generated at the same time as the first BRDY#. '11' (Rev. BB and later) — Enable Pipeline on Read-Miss Cycle; 'NA' will be generated as soon as the internal read request is recognized.
15:10	Reserved

4.6 PCI Configuration Registers

NOTE: The following PCI registers are accessed through the PCI configuration space through I/O addresses 0CF8H and 0CFCH.

4.6.1 Vendor ID Register (VID)

Index: 00H

Bit	Description	Name	Reset State
0	Vendor ID Number [0]	VENDOR_ID0	'0'
1	Vendor ID Number [1]	VENDOR_ID1	'1'
2	Vendor ID Number [2]	VENDOR_ID2	'1'
3	Vendor ID Number [3]	VENDOR_ID3	'0'
4	Vendor ID Number [4]	VENDOR_ID4	'0'
5	Vendor ID Number [5]	VENDOR_ID5	'1'
6	Vendor ID Number [6]	VENDOR_ID6	'1'
7	Vendor ID Number [7]	VENDOR_ID7	'0'
8	Vendor ID Number [8]	VENDOR_ID8	'0'
9	Vendor ID Number [9]	VENDOR_ID9	'0'
10	Vendor ID Number [10]	VENDOR_ID10	'0'
11	Vendor ID Number [11]	VENDOR_ID11	'0'
12	Vendor ID Number [12]	VENDOR_ID12	'1'
13	Vendor ID Number [13]	VENDOR_ID13	'0'
14	Vendor ID Number [14]	VENDOR_ID14	'0'
15	Vendor ID Number [15]	VENDOR_ID15	'0'

Bit	Description
15:0	**Vendor ID Number [15:0]:** These bits are hardwired to 1066H.

4.6.2 Device ID Register (DID)

Index: 02H

Bit	Description	Name	Reset State
0	Device ID Number [0]	Device_ID0	'1'
1	Device ID Number [1]	Device_ID1	'0'
2	Device ID Number [2]	Device_ID2	'0'
3	Device ID Number [3]	Device_ID3	'0'
4	Device ID Number [4]	Device_ID4	'0'
5	Device ID Number [5]	Device_ID5	'0'
6	Device ID Number [6]	Device_ID6	'0'
7	Device ID Number [7]	Device_ID7	'0'
8	Device ID Number [8]	Device_ID8	'0'
9	Device ID Number [9]	Device_ID9	'0'
10	Device ID Number [10]	Device_ID10	'0'
11	Device ID Number [11]	Device_ID11	'0'
12	Device ID Number [12]	Device_ID12	'0'
13	Device ID Number [13]	Device_ID13	'0'
14	Device ID Number [14]	Device_ID14	'0'
15	Device ID Number [15]	Device_ID15	'0'

Bit	Description
15:0	**Device ID Number [15:0]:** These bits are hardwired. V1-LS = 0001H

4.6.3 Command Register (COMMD)

Index: 04H

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Memory Space Enable	MEM_RESPOND	'1'
2	Reserved		'1'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Parity Error Response	PARERR_REP	'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	Reserved
1	**Memory Space Enable:** When '0', PCI master access to main memory is disabled. When '1', PCI master access to main memory is enabled.
5:2	Reserved
6	**Parity Error Response:** When '1', V1-LS will assert PERR# when a PCI parity error is detected. When '0', V1-LS will not assert PERR# when a PCI parity error is detected.
15:7	Reserved

4.6.4 Status Register (STAT)

Index: 06H

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Reserved		'0'
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	DEVSEL Timing [0]	DEVSEL_TIM0	'0'
10	DEVSEL Timing [1]	DEVSEL_TIM1	'1'
11	Reserved		'0'
12	Receive Target Abort	REC_TAG_ABRT	'0'
13	Receive Master Abort	REC_MST_ABRT	'0'
14	Reserved		'0'
15	Detect Parity Error	DET_PAR_ERR	'0'

Bit	Description
8:0	Reserved
10:9	**DEVSEL Timing:** These bits indicate the slowest time that V1-LS will return DEVSEL#. These bits are hardwired to 'slow' timing.
11	Reserved
12	**Receive Target Abort:** Reading a '1' indicates receiving a target abort condition. This bit can be reset by writing a '1'.
13	**Receive Master Abort:** Reading a '1' indicates receiving a master abort condition (does not include master abort generated from a special cycle). This bit can be reset by writing a '1'.
14	Reserved
15	**Detect Parity Error:** When V1-LS detects a PCI parity error, this bit will be set to '1'. This bit can be reset by writing a '1'.

4.6.5 Revision ID Register (RID)

Index: 08H

Bit	Description	Name	Reset State
0	Revision ID Number [0]	REVISION_ID0	'0'
1	Revision ID Number [1]	REVISION_ID1	'0'
2	Revision ID Number [2]	REVISION_ID2	'0'
3	Revision ID Number [3]	REVISION_ID3	'0'
4	Revision ID Number [4]	REVISION_ID4	'0'
5	Revision ID Number [5]	REVISION_ID5	'0'
6	Revision ID Number [6]	REVISION_ID6	'0'
7	Revision ID Number [7]	REVISION_ID7	'0'

Bit	Description
7:0	**Revision ID Number [7:0]:** These bits are hardwired.

Bit [3:0]	Revision ID
3H	AA
4H	BB
5H	CC

4.6.6 Class Register (CLASS)

Index: 09H

Bit	Description	Name	Reset State
0	Class Code [0]	CLASS_CODE0	'0'
1	Class Code [1]	CLASS_CODE1	'0'
2	Class Code [2]	CLASS_CODE2	'0'
3	Class Code [3]	CLASS_CODE3	'0'
4	Class Code [4]	CLASS_CODE4	'0'
5	Class Code [5]	CLASS_CODE5	'0'
6	Class Code [6]	CLASS_CODE6	'0'
7	Class Code [7]	CLASS_CODE7	'0'
8	Class Code [8]	CLASS_CODE8	'0'
9	Class Code [9]	CLASS_CODE9	'0'
10	Class Code [10]	CLASS_CODE10	'0'
11	Class Code [11]	CLASS_CODE11	'0'
12	Class Code [12]	CLASS_CODE12	'0'
13	Class Code [13]	CLASS_CODE13	'0'
14	Class Code [14]	CLASS_CODE14	'0'
15	Class Code [15]	CLASS_CODE15	'0'
16	Class Code [16]	CLASS_CODE16	'0'
17	Class Code [17]	CLASS_CODE17	'1'
18	Class Code [18]	CLASS_CODE18	'1'
19	Class Code [19]	CLASS_CODE19	'0'
20	Class Code [20]	CLASS_CODE20	'0'
21	Class Code [21]	CLASS_CODE21	'0'
22	Class Code [22]	CLASS_CODE22	'0'
23	Class Code [23]	CLASS_CODE23	'0'

Bit	Description
23:0	**Class Code [23:0]:** These bits are hardwired to 060000H.

4.6.7 Latency Timer Register (LTMR)

Index: 0DH

Bit	Description	Name	Reset State
0	Latency Timer [0]	LAT_TIM0	'0'
1	Latency Timer [1]	LAT_TIM1	'0'
2	Latency Timer [2]	LAT_TIM2	'0'
3	Latency Timer [3]	LAT_TIM3	'0'
4	Latency Timer [4]	LAT_TIM4	'0'
5	Latency Timer [5]	LAT_TIM5	'0'
6	Latency Timer [6]	LAT_TIM6	'0'
7	Latency Timer [7]	LAT_TIM7	'0'

Bit	Description
7:0	**Latency Timer [7:0]:** These bits are hardwired to 00H.

5. V1-LS ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 5-1. Maximum Ratings

Condition	Maximum Rating
Ambient temperature	0^o - 70^o C
Storage temperature	-65^o to $+150^o$ C
Supply voltage to ground potential	3.135-V to 3.6-V (for 3-V design) 4.5-V to 5.5-V (for 5-V design)
Applied output voltage	-0.3 to V_{DD} + 0.3V
Applied input voltage	-0.3 to V_{DD} + 0.3V
Operating power dissipation	1 W

5.2 D.C. Characteristics 5.0 Volt

V_{DD} = 5-V ± 10% @ 50 MHz; T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Conditions
V_{DD}	Power supply voltage	4.75	5.25	V	Normal operation
V_{IL}	Input low voltage (TTL)	-0.5	0.8	V	
V_{ILC}	Input low voltage (CMOS)	-0.5	0.3 * V_{DD}	V	
V_{ILP}	Input low voltage (PCI)	-0.5	0.8	V	
V_{IH}	Input high voltage (TTL)	2.2	V_{DD} + 0.5	V	
V_{IHC}	Input high voltage (CMOS)	0.7 * V_{DD}	V_{DD} + 0.5	V	
V_{IHP}	Input high voltage (PCI)	2.0	V_{DD} + 0.5	V	
V_{OH}	Output high voltage (TTL)	3.7		V	
V_{OHC}	Output high voltage (CMOS)	V_{DD} - 0.2		V	
V_{OHP}	Output high voltage (PCI)	2.4		V	I_{OUT} = -2 mA
V_{OL}	Output low voltage (TTL)		0.4	V	
V_{OLC}	Output low voltage (CMOS)		0.2	V	
V_{OLP}	Output low voltage (PCI)		0.55	V	I_{OUT} = 6 mA
I_{CC}	Power supply current		300	mA	
I_L	Input leakage current		1.0	µA	
I_{OZ}	Tristate leakage current		10.0	µA	
C_{IN}	Input capacitance	5.0	10.0	pF	
C_{OUT}	Output capacitance	5.0	10.0	pF	

5.3 D.C. Characteristics 3.3 Volt

V_{DD} = 3.3-V ± 10% @ 50 MHz; T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Conditions
V_{DD}	Power supply voltage	3.135	3.6	V	Normal operation
V_{IL}	Input low voltage (TTL)	-0.3	0.8	V	
V_{ILC}	Input low voltage (CMOS)	-0.3	0.3 * V_{DD}	V	
V_{ILP}	Input low voltage (PCI)	-0.5	0.325 * V_{DD}	V	
V_{IH}	Input high voltage (TTL)	2.0	V_{DD} + 0.3	V	
V_{IHC}	Input high voltage (CMOS)	0.7 * V_{DD}	V_{DD} + 0.3	V	
V_{IHP}	Input high voltage (PCI)	0.475 * V_{DD}	V_{DD} + 0.5	V	
V_{OH}	Output high voltage (TTL)	2.4		V	
V_{OHC}	Output high voltage (CMOS)	V_{DD} - 0.2		V	
V_{OHP}	Output high voltage (PCI)	0.9 * V_{DD}		V	I_{OUT} = -500 µA
V_{OL}	Output low voltage (TTL)		0.4	V	
V_{OLC}	Output low voltage (CMOS)		0.2	V	
V_{OLP}	Output low voltage (PCI)		0.1 * V_{DD}	V	I_{OUT} = 1500 µA
I_{CC}	Power supply current		300	mA	
I_L	Input leakage current		1.0	µA	
I_{OZ}	Tristate leakage current		10.0	µA	
C_{IN}	Input capacitance	5.0	10.0	pF	
C_{OUT}	Output capacitance	5.0	10.0	pF	

5.4 A.C. Characteristics

Table 5-2. V1-LS AC Timing Parameters

Symbol	Parameter	Min	Max	Unit	Notes
PCI Timing					
t_{100a}	PCICLK to Signal Valid Delay - bussed signals	2	11	ns	1
t_{100b}	PCICLK to Signal Valid Delay - point to point	2	12	ns	1
t_{101}	Float to Active Delay	2		ns	1
t_{102}	Active to Float Delay		28	ns	1
t_{103a}	Input Set up Time to PCICLK - bussed signals	7		ns	
t_{103b}	Input Set up Time to PCICLK - point to point	12		ns	
t_{104}	Input Hold Time from PCICLK	0		ns	
CPU Timing					
t_{200h}	Hold Time: BE[7:0]#, D/C#, W/R#, CACHE#, A[31:3], LOCK#, ADS#, M/IO# to CPUCLK	1		ns	3
t_{200s}	Set Up time: BE[7:0]#, D/C#, W/R#, CACHE#, A[31:3], LOCK#, ADS#, M/IO# to CPUCLK		7	ns	3
t_{201h}	Hold Time: FERR#, SMIACT# to CPUCLK	1		ns	3
t_{201s}	Set Up Time: FERR#, SMIACT# to CPUCLK		6	ns	3
t_{202h}	Hold time: HLDA, HITM# to CPUCLK	1		ns	3
t_{202s}	Set Up Time: HLDA, HITM# to CPUCLK		8.0	ns	3
t_{203h}	Hold Time: D[63:0] to V2CLK	1.3		ns	3
t_{203s}	Set Up Time: D[63:0] to V2CLK		6	ns	3
t_{204}	CPUCLK to A[31:3], EADS# Valid Delay	2	8	ns	3
t_{205}	CPUCLK to INV, KEN#, NA#, WB/WT#, BRDY#, AHOLD, BOFF#, HOLD, A20M#, INTR, STPCLK#, INIT, NMI, SMI#, IGNNE# Valid Delay	2	9	ns	3
t_{206}	V2CLK to D[63:0] Valid Delay	2	11	ns	3
L2 Cache Timing					
t_{300}	CPUCLK to ADSC#, ADV# Valid Delay		11	ns	5

Table 5-2. V1-LS AC Timing Parameters *(cont.)*

Symbol	Parameter	Min	Max	Unit	Notes
t_{301}	CPUCLK to CWE[7:0]# Valid Delay		11	ns	2
t_{302}	CPUCLK to TAGD[7:0] Valid Delay	5	30	ns	4
t_{303}	CPUCLK to TAGWE# Valid Delay	2	13	ns	2
t_{304}	CPUCLK to COE# Valid Delay		9	ns	5
DRAM Timing					
t_{400}	CPUCLK to WE# Valid Delay		15	ns	6
t_{401}	CPUCLK to RAS#, CAS# Valid Delay (for both rising and falling edges)		10	ns	2
t_{402}	CPUCLK to MA Valid Delay		14	ns	6
t_{403}	V2CLK to MD Valid Delay (for both rising and falling edges)		14	ns	4
t_{404}	MD setup time to V2CLK		2	ns	4
t_{405}	V1-LS: BC[2:0], BD[7:0] output delay from V2CLK		9	ns	2
t_{406}	BD[7:0] setup time to V2CLK		3	ns	2
t_{407}	V2-LS: BD[7:0] output delay from V2CLK		9.5	ns	2
t_{408}	V2-LS: BD[7:0] setup time to V2CLK		5	ns	2
t_{409}	V1-LS: ADOE# output delay from PCICLK		8.5	ns	2

NOTES:

1) Minimum times are measured with 0 pF equivalent load; maximum times are measured with 50 pF equivalent load. Actual test capacitance may vary, but results should be correlated to these specifications.
2) Measured with 15 pF equivalent load.
3) Measured with 20 pF equivalent load.
4) Measured with 25 pF equivalent load.
5) Measured with 35 pF equivalent load.
6) Measured with 60 pF equivalent load.

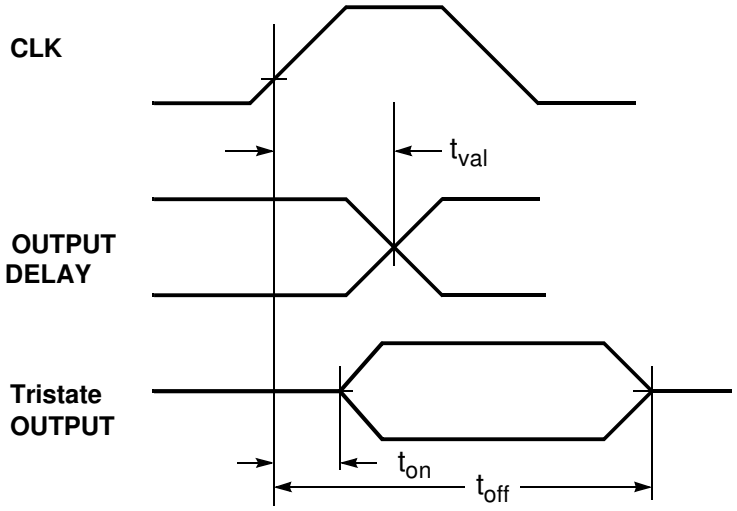


Figure 5-1. Output Timing Measurement Conditions

$t_{val} = t_{100a}, t_{100b}, t_{204}, t_{205}, t_{206}, t_{300} - t_{304}, t_{400} - t_{403}, t_{405}, t_{407}, t_{409}$

$t_{on} = t_{101}$

$t_{off} = t_{102}$

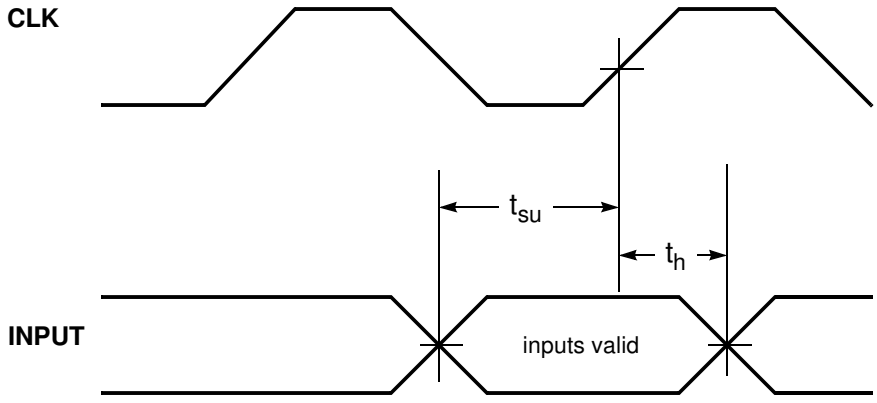


Figure 5-2. Input Timing Measurement Conditions

$t_{su} = t_{103a}, t_{103b}, t_{200s} - t_{203s}, t_{403}, t_{406}, t_{408}$

$t_h = t_{104}, t_{200h} - t_{203h}$

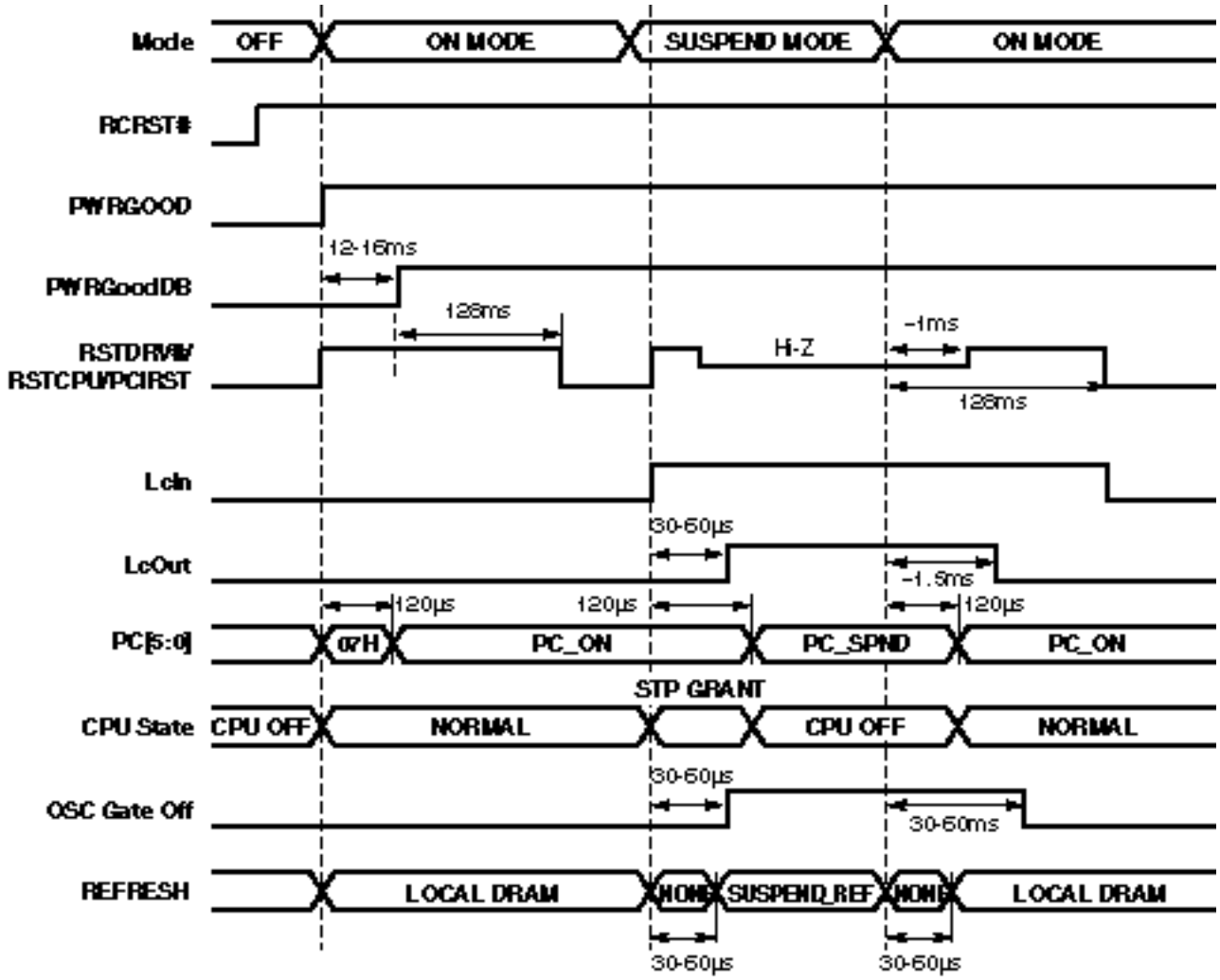


Figure 5-3. Power-On/5-V Suspend Timing Diagram

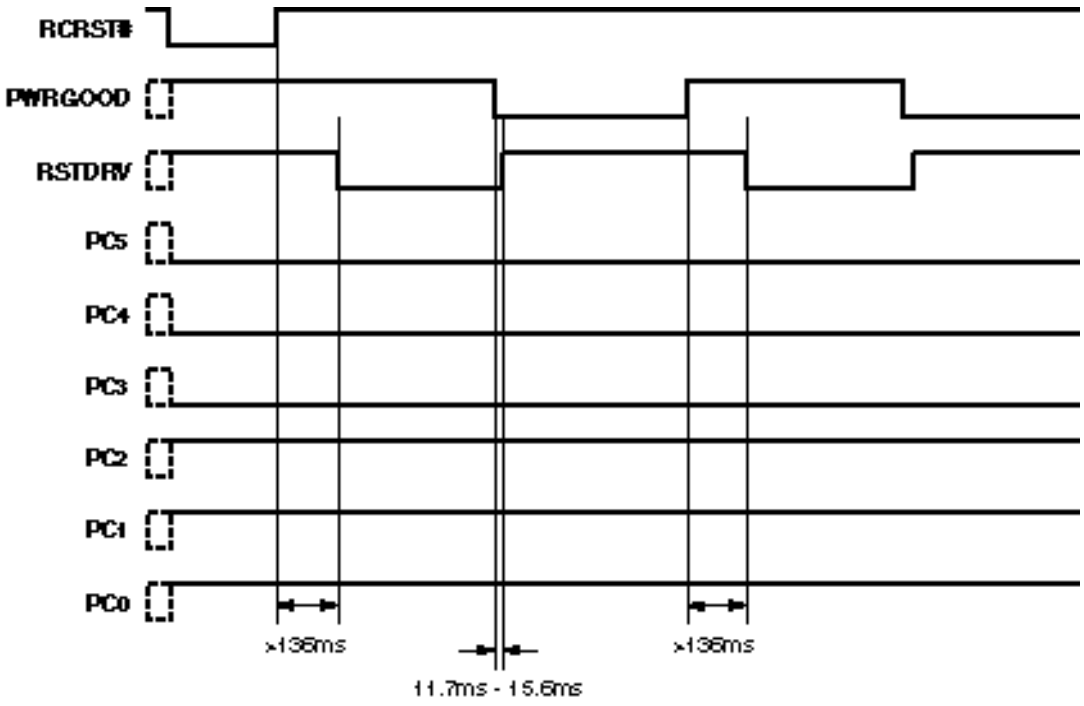


Figure 5-4. Reset Timing

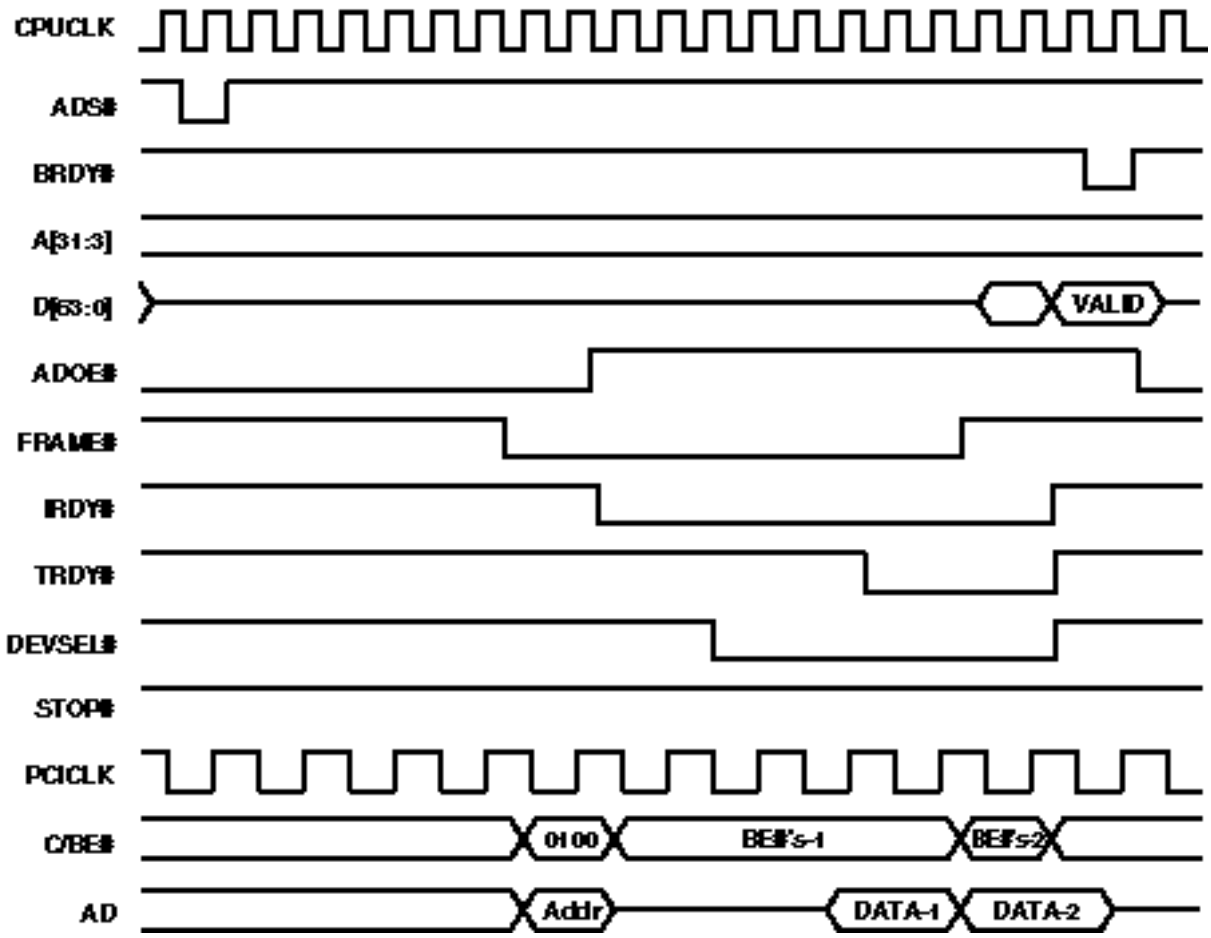


Figure 5-5. CPU-to-PCI Memory Burst Read Cycle

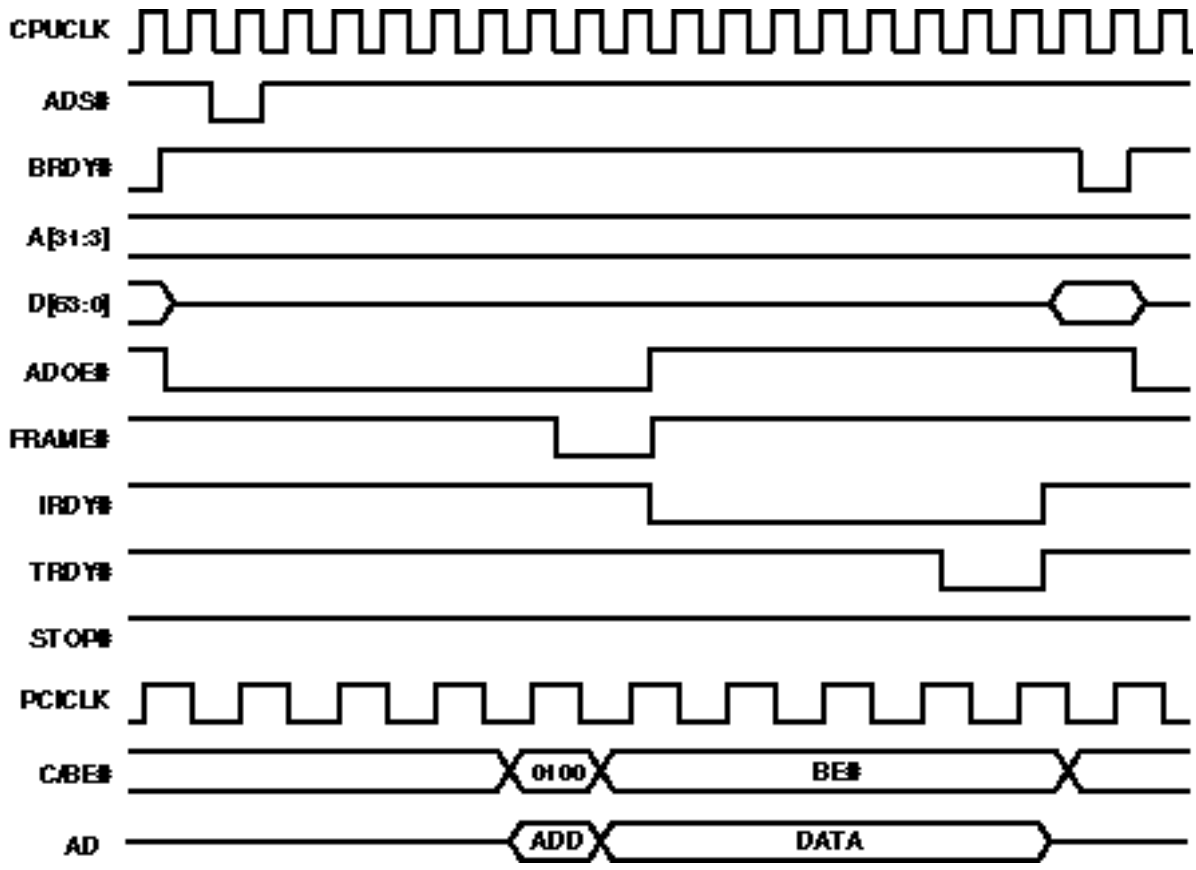


Figure 5-6. CPU-to-PCI Memory Read Cycle

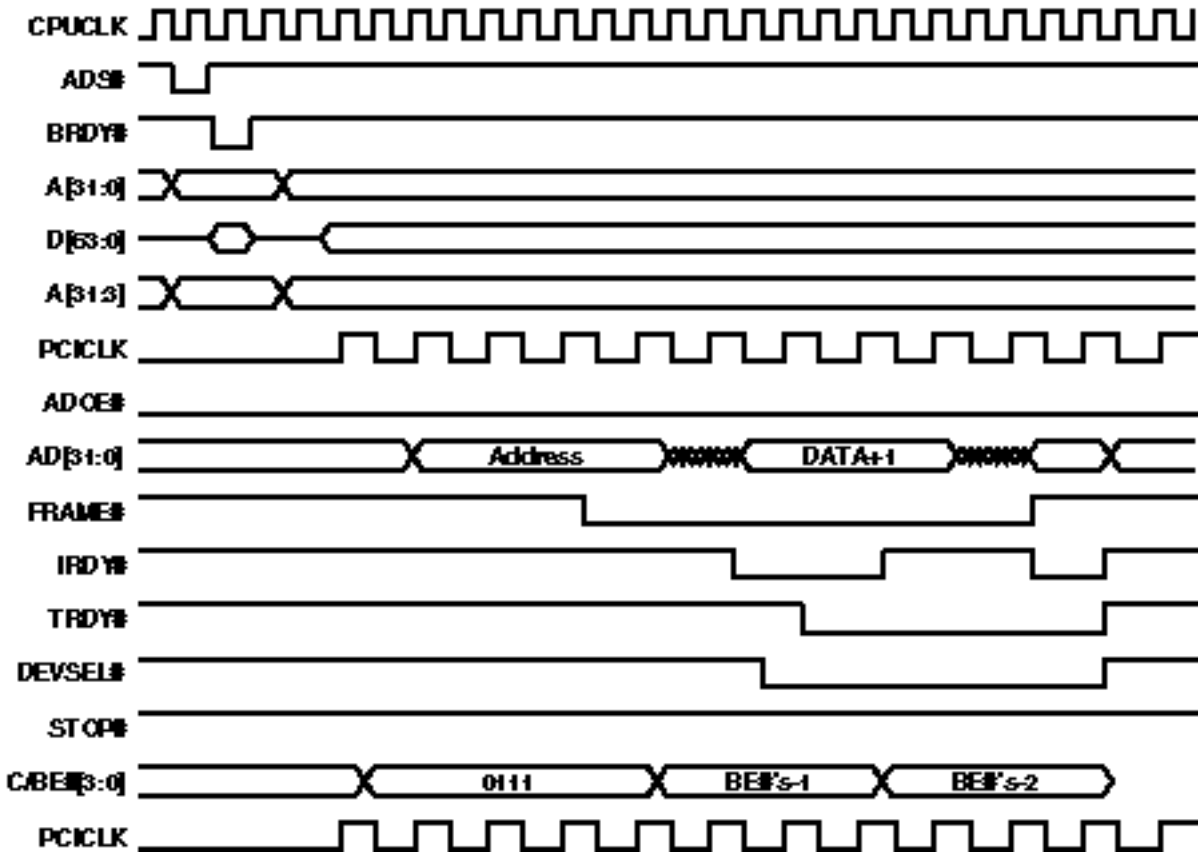


Figure 5-7. CPU-to-PCI Memory Write Cycle

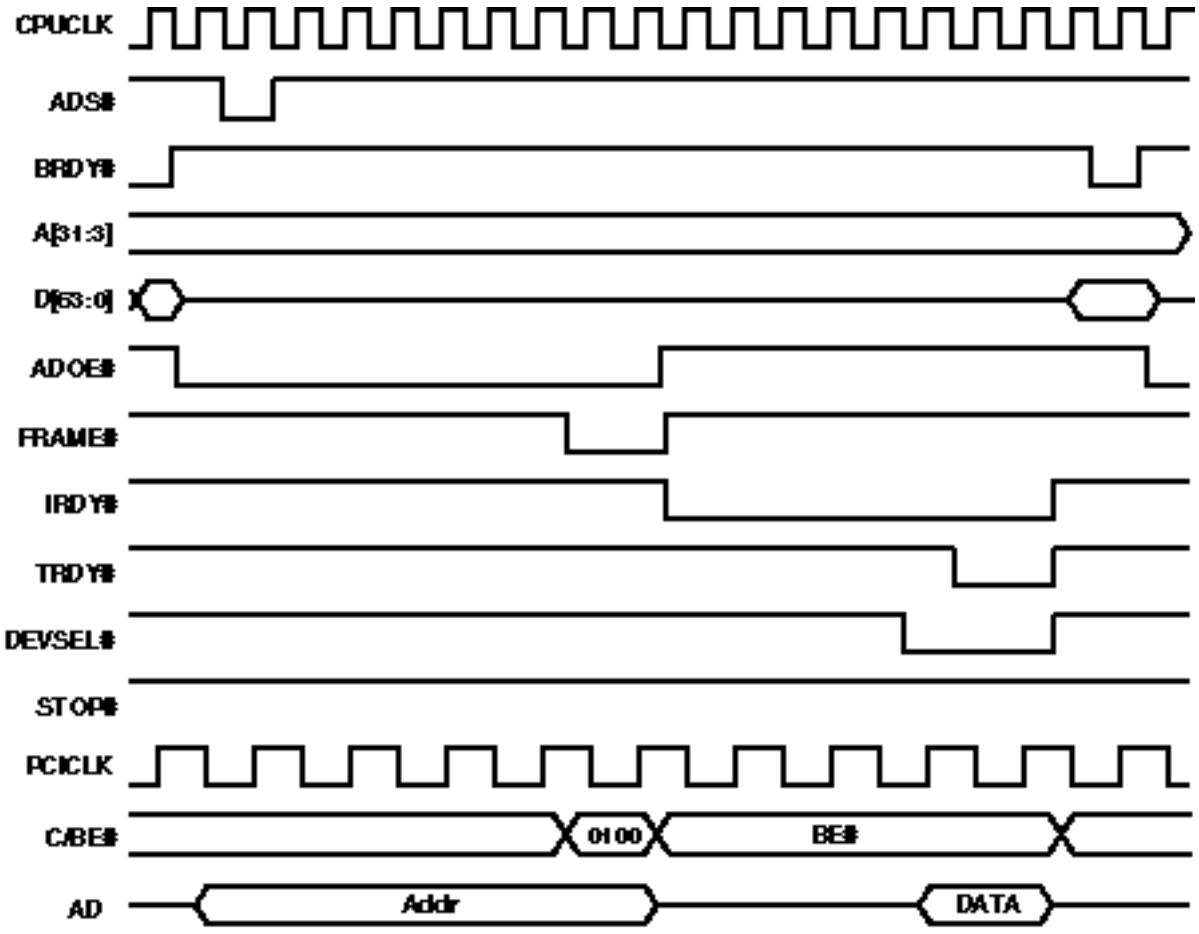


Figure 5-8. CPU-to-PCI I/O Read Cycle

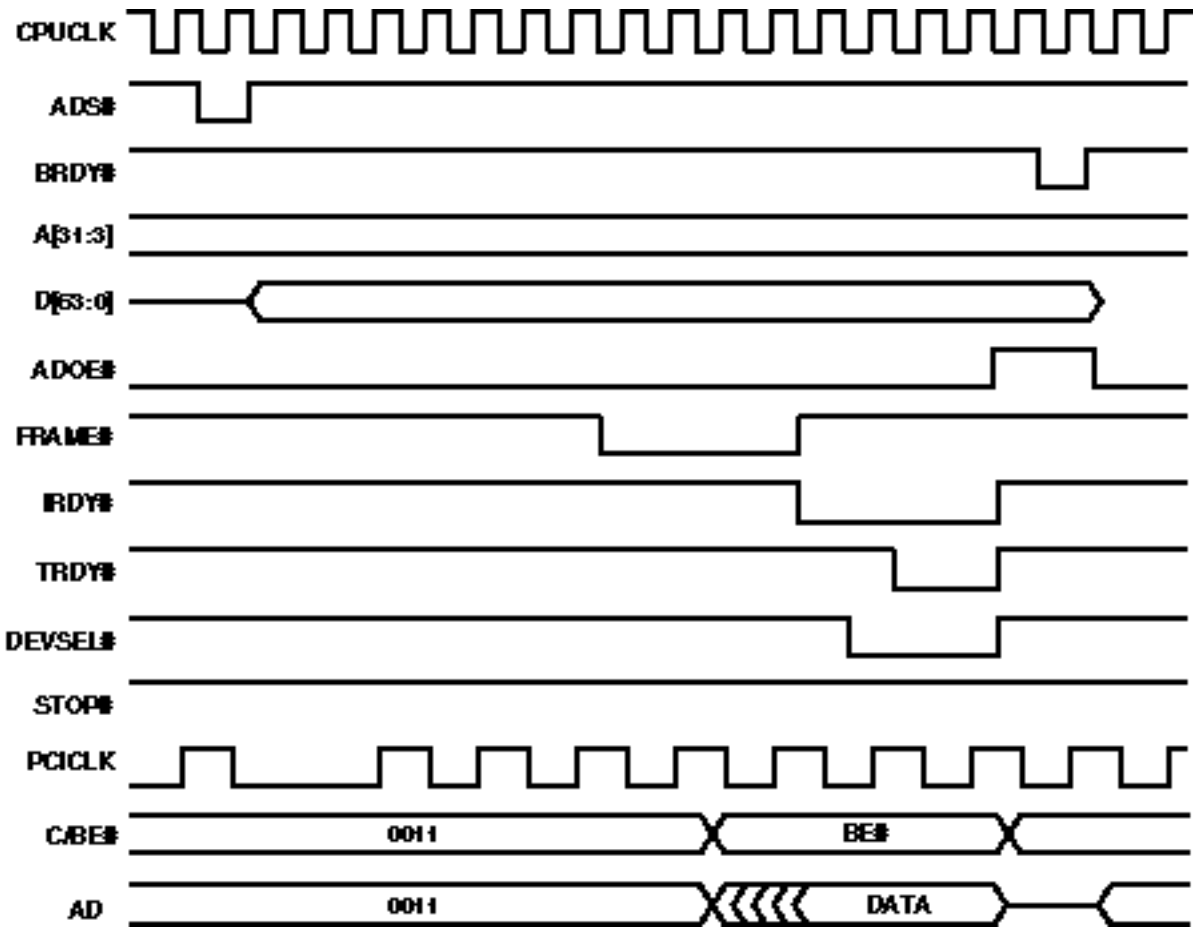


Figure 5-9. CPU-to-PCI I/O Write Cycle

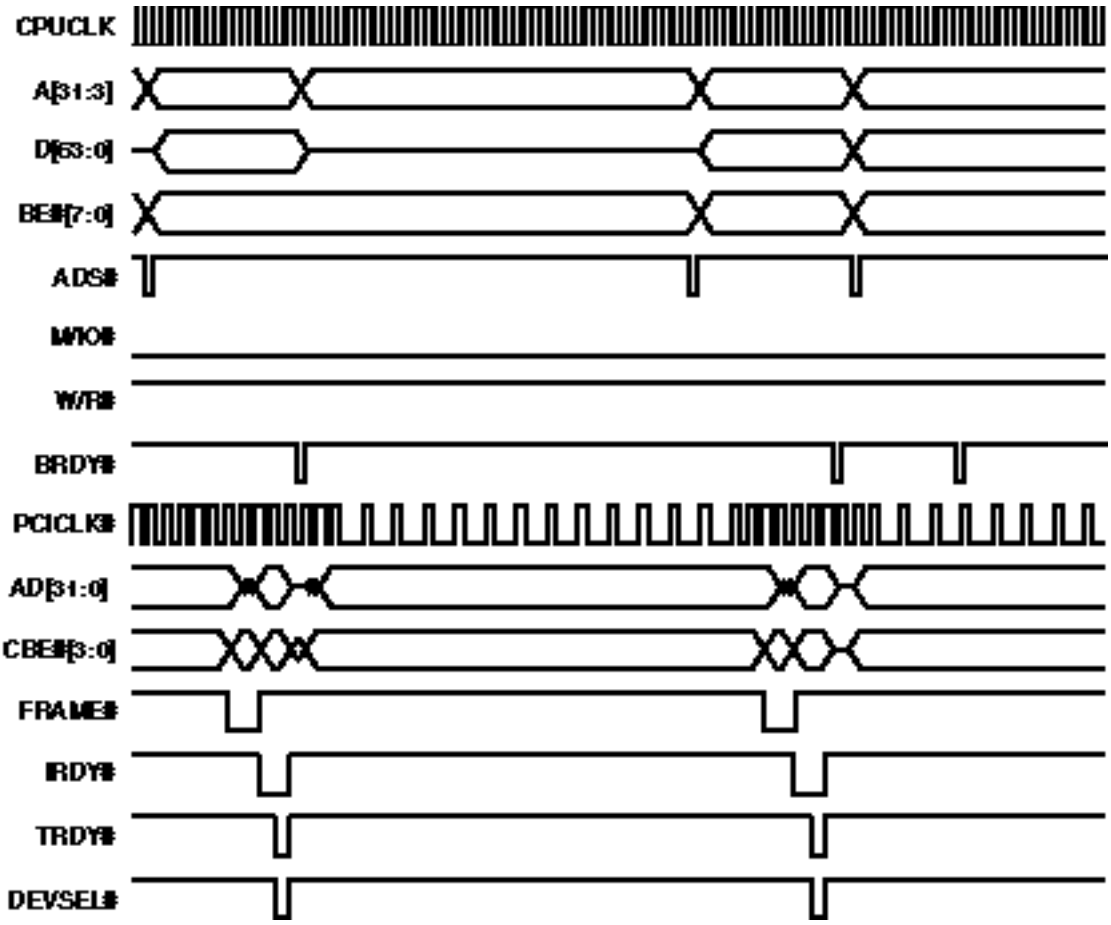


Figure 5-10. PicoPower PCICLK Control Scheme

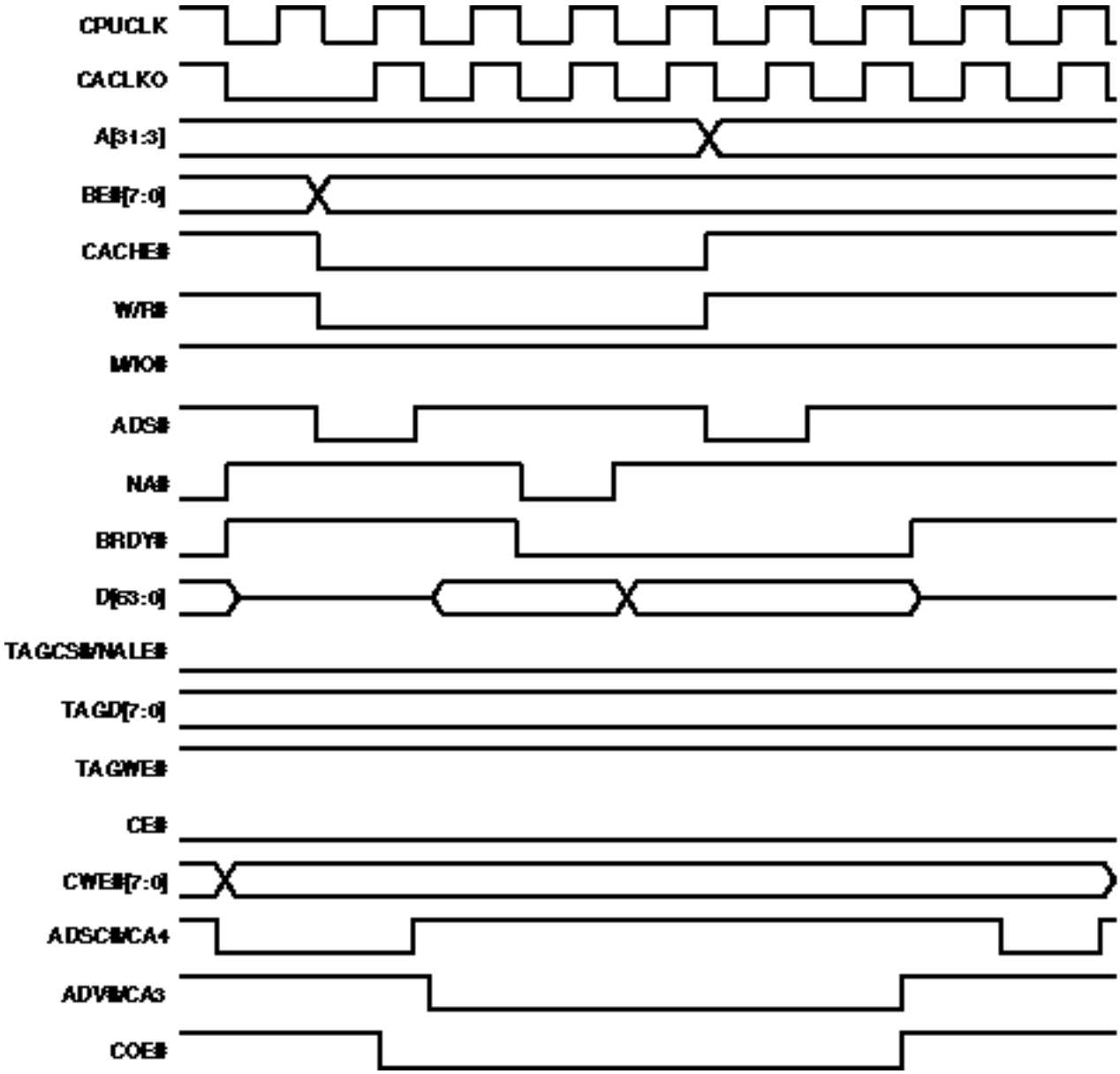


Figure 5-11. L2 Cache – Pipeline Synchronous, Single Read Hit

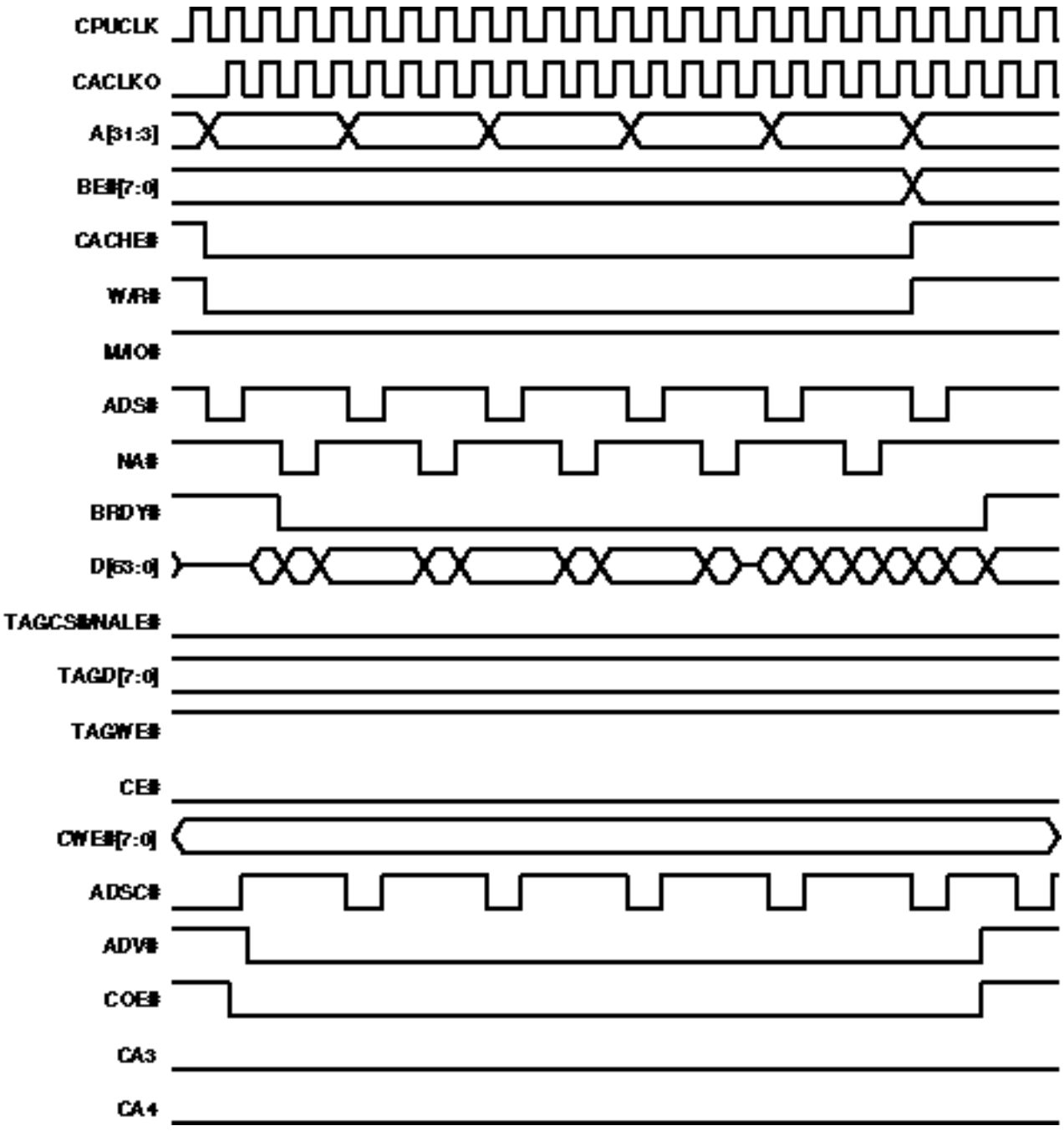


Figure 5-12. L2 Cache – Pipeline Synchronous, Multiple Read Hit

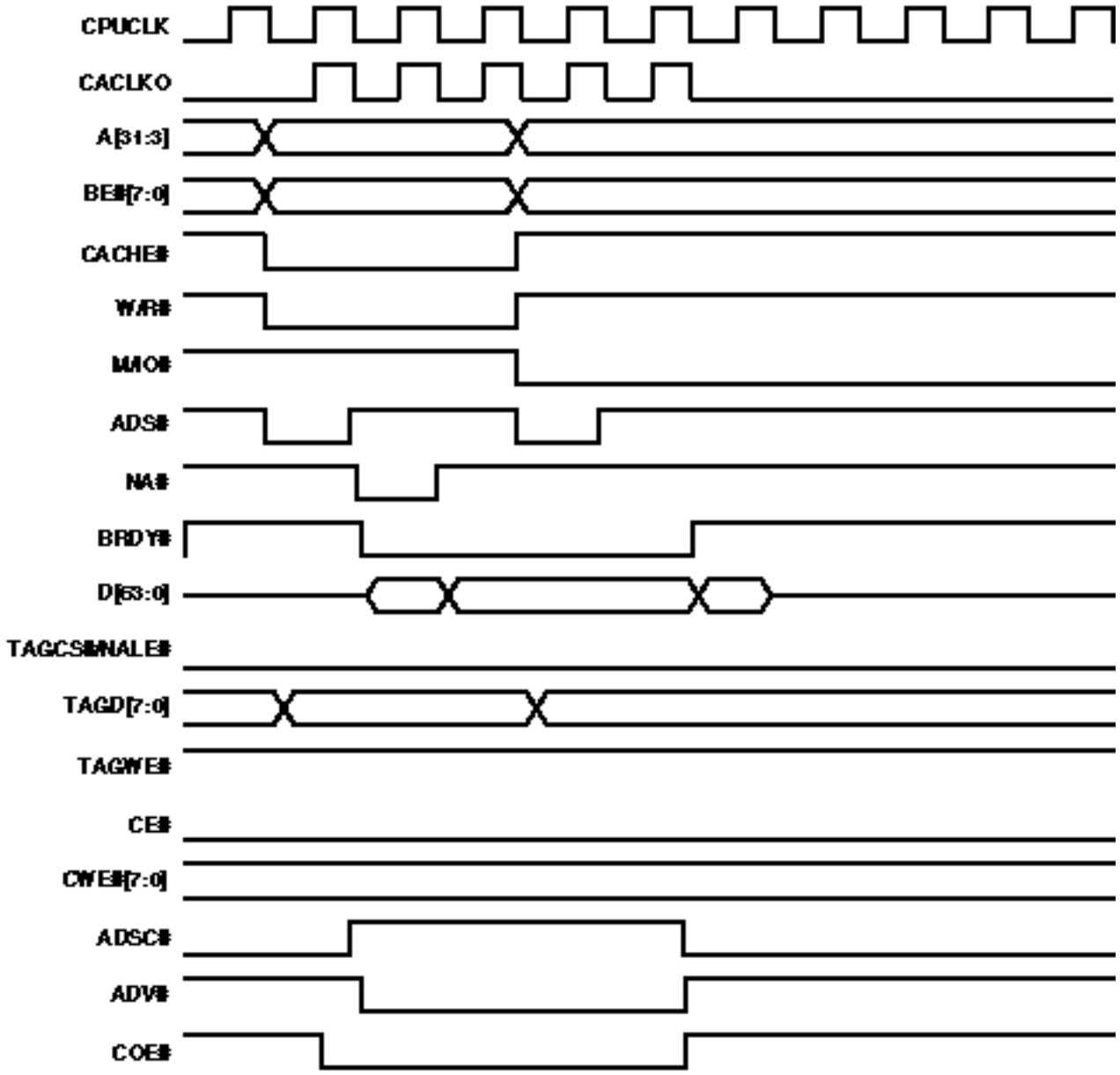


Figure 5-13. L2 Cache – Pipeline Synchronous Burst Read Hit

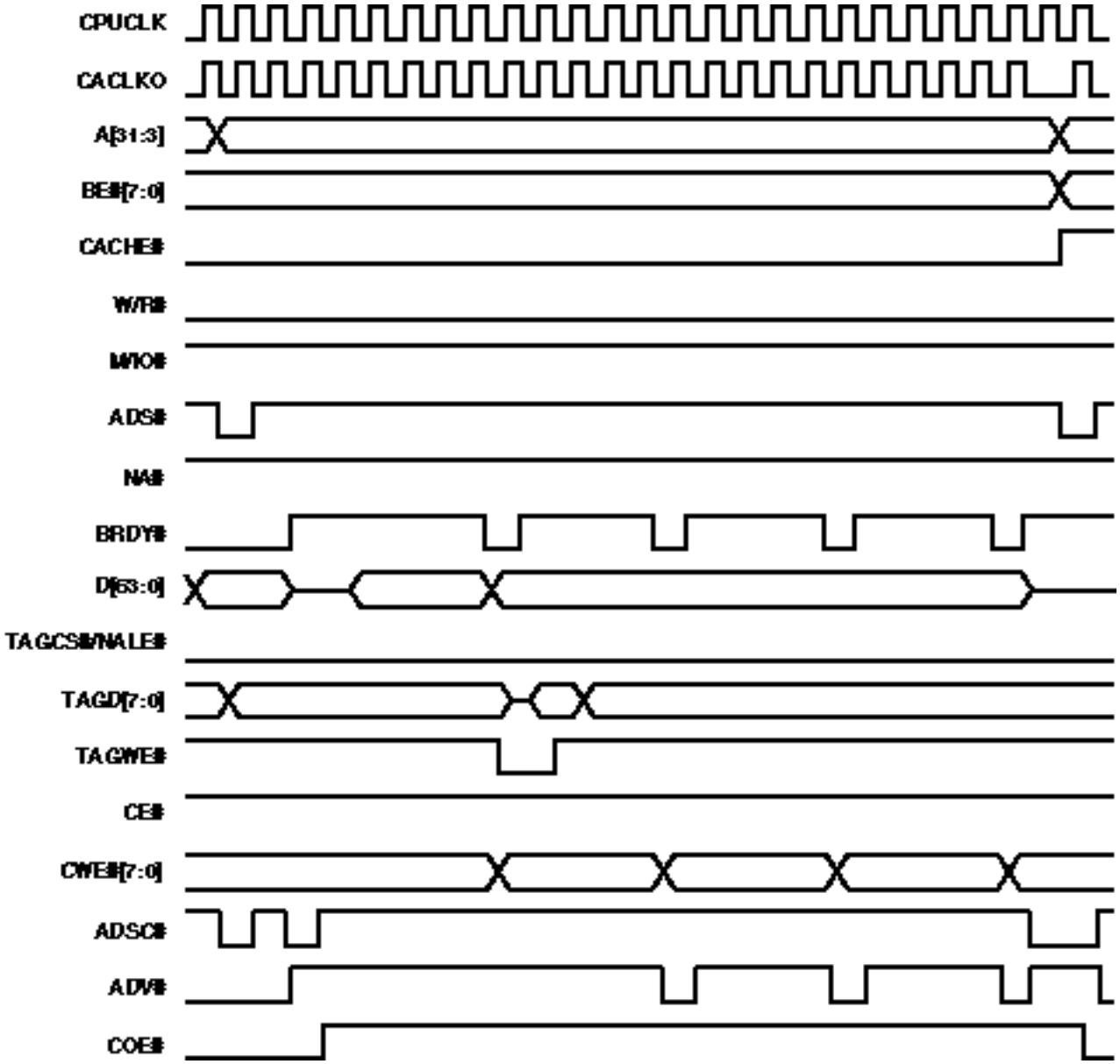


Figure 5-14. L2 Cache – Pipeline Synchronous Read Miss

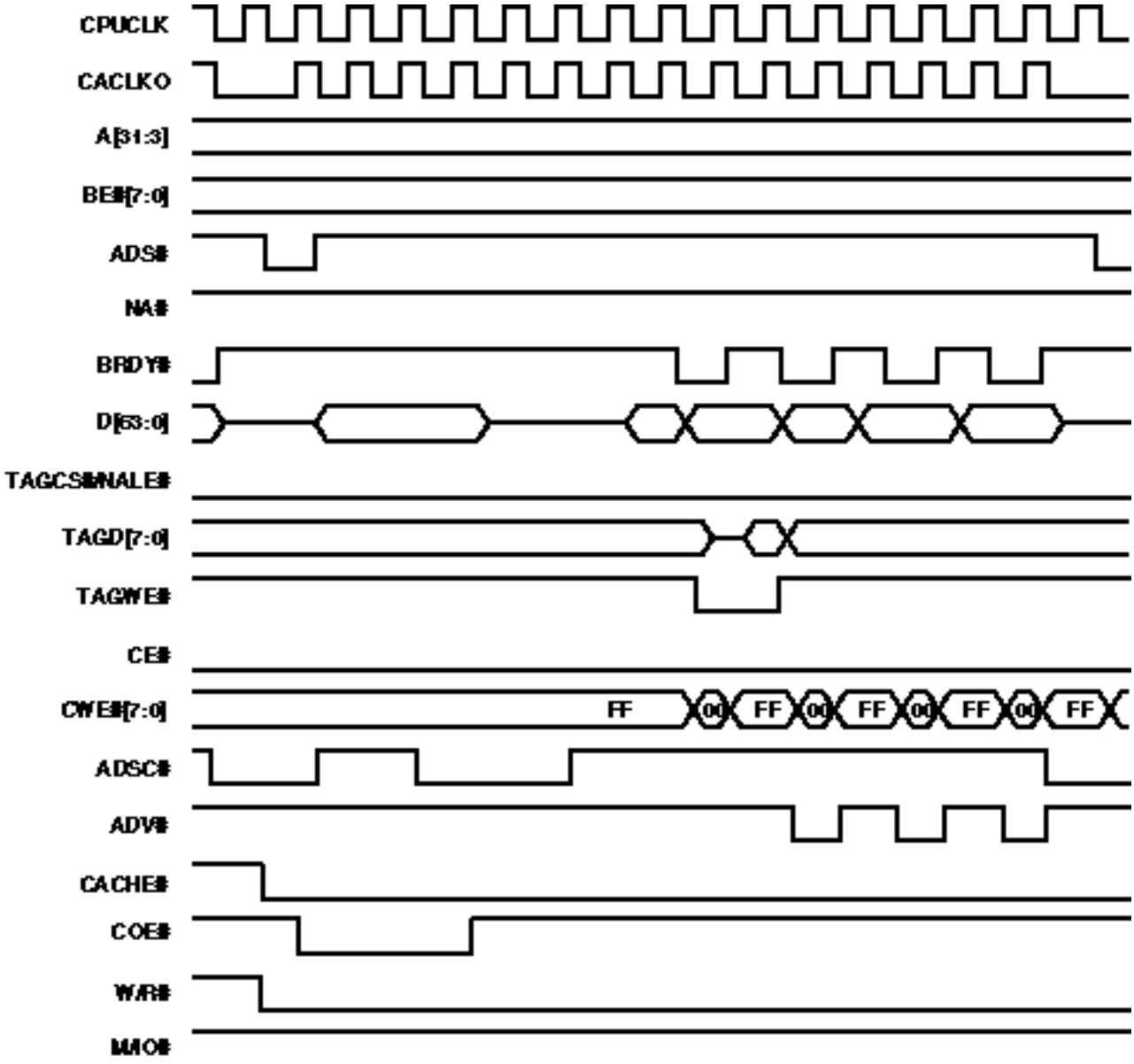


Figure 5-15. L2 Cache – Synchronous Burst Read Miss

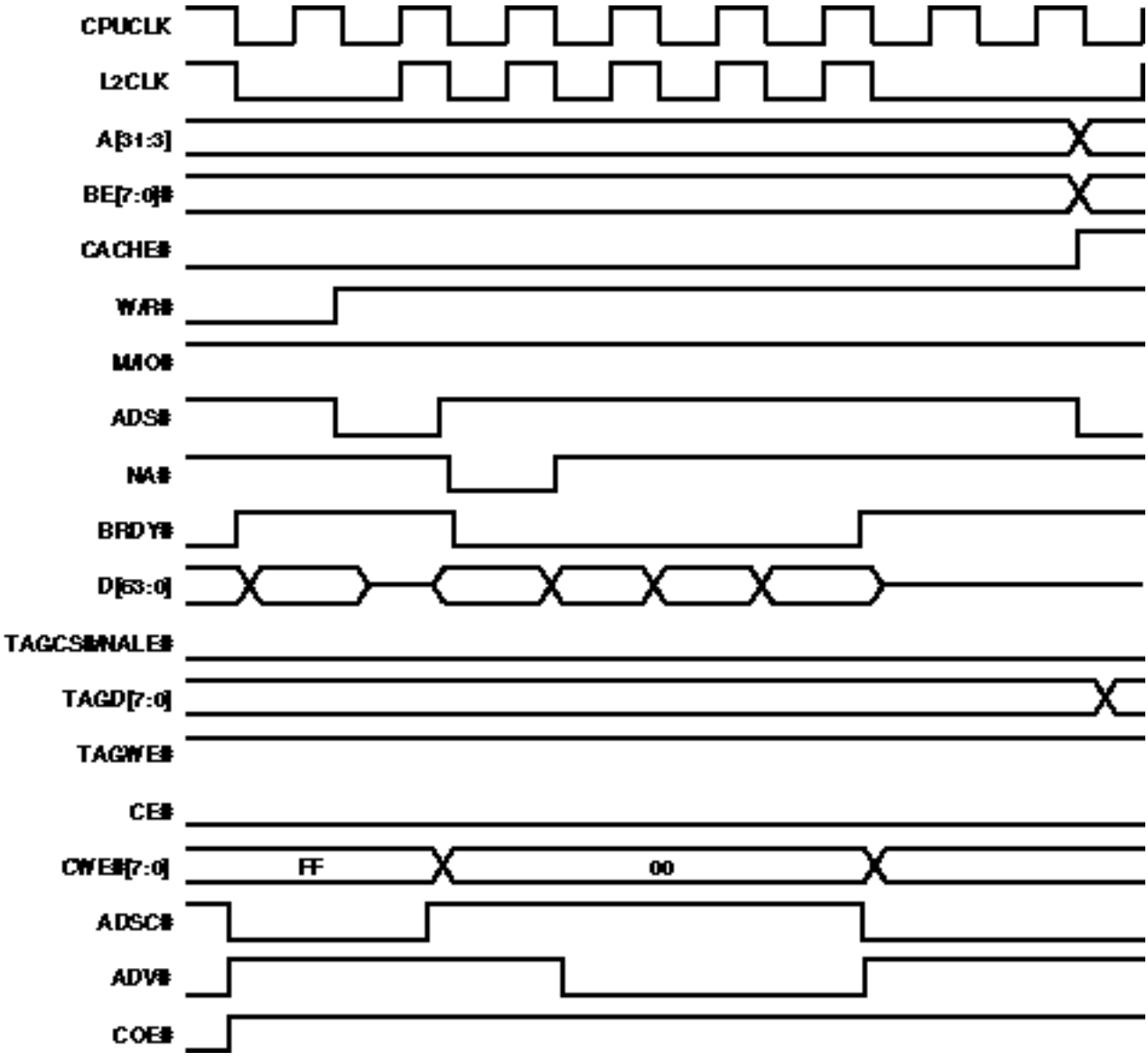


Figure 5-16. L2 Cache Write Burst Hit

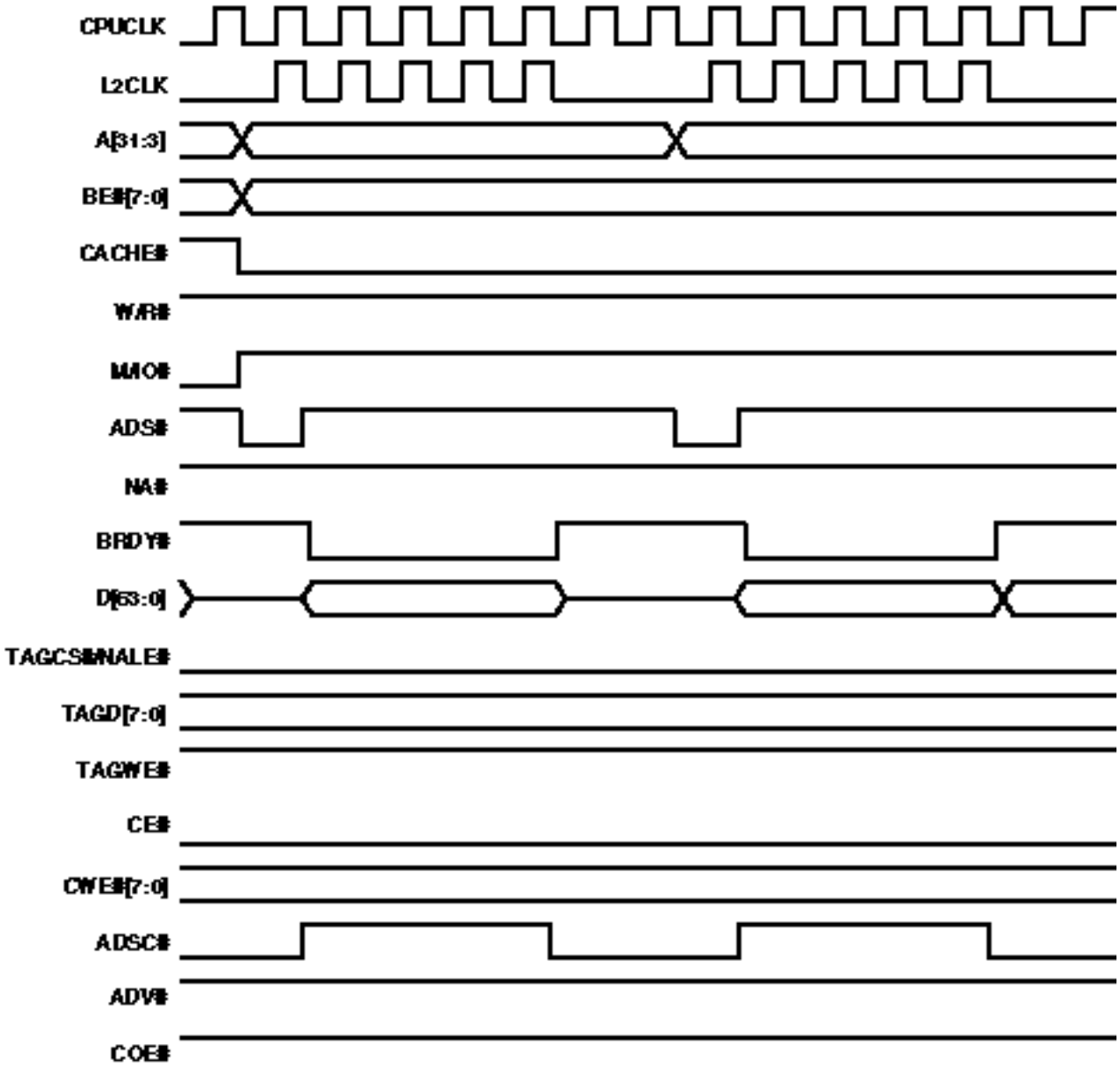


Figure 5-17. L2 Cache Write Burst Miss With Empty Write Buffer

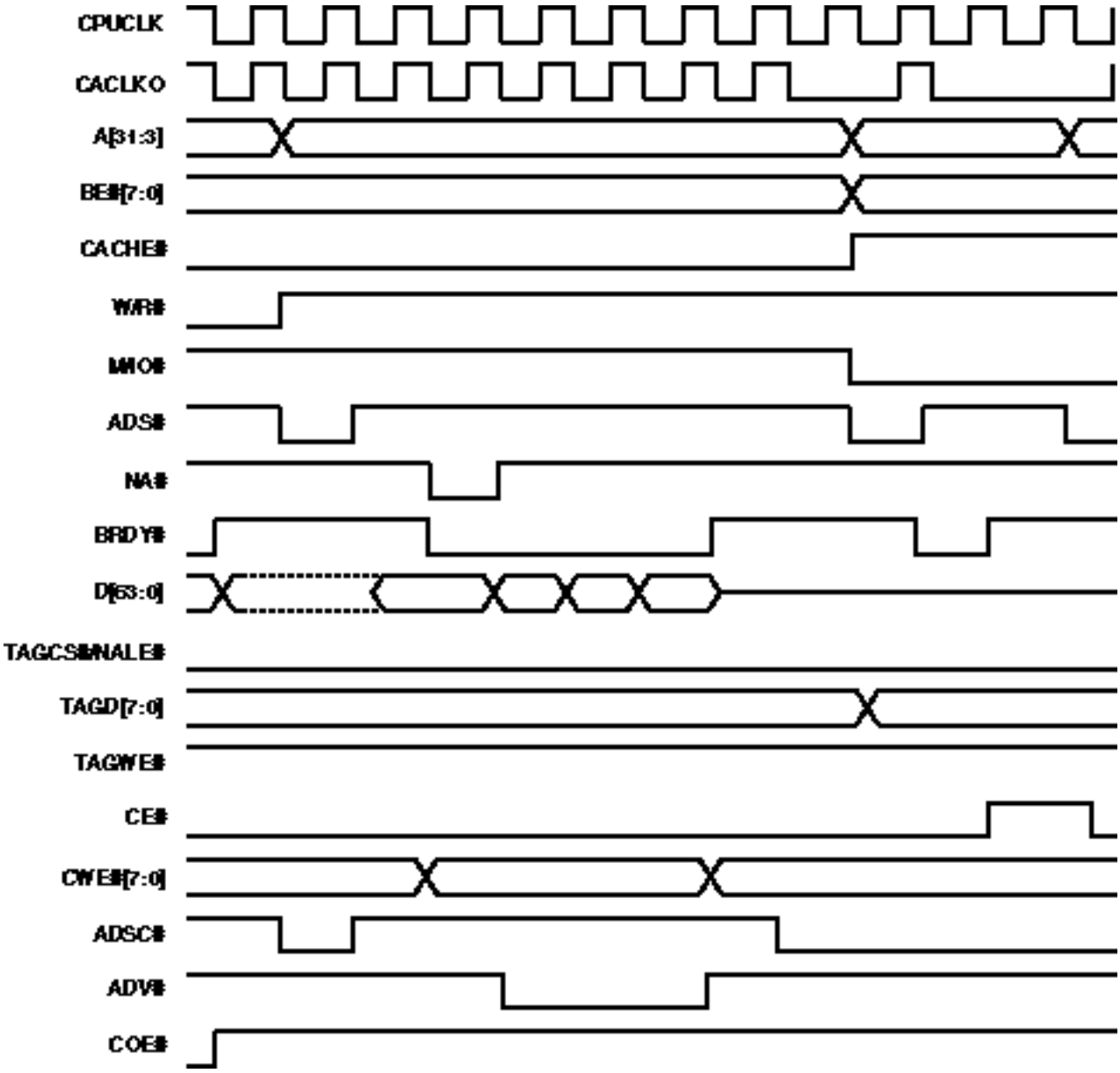


Figure 5-18. L2 Cache – Pipeline Synchronous, Write Burst Hit

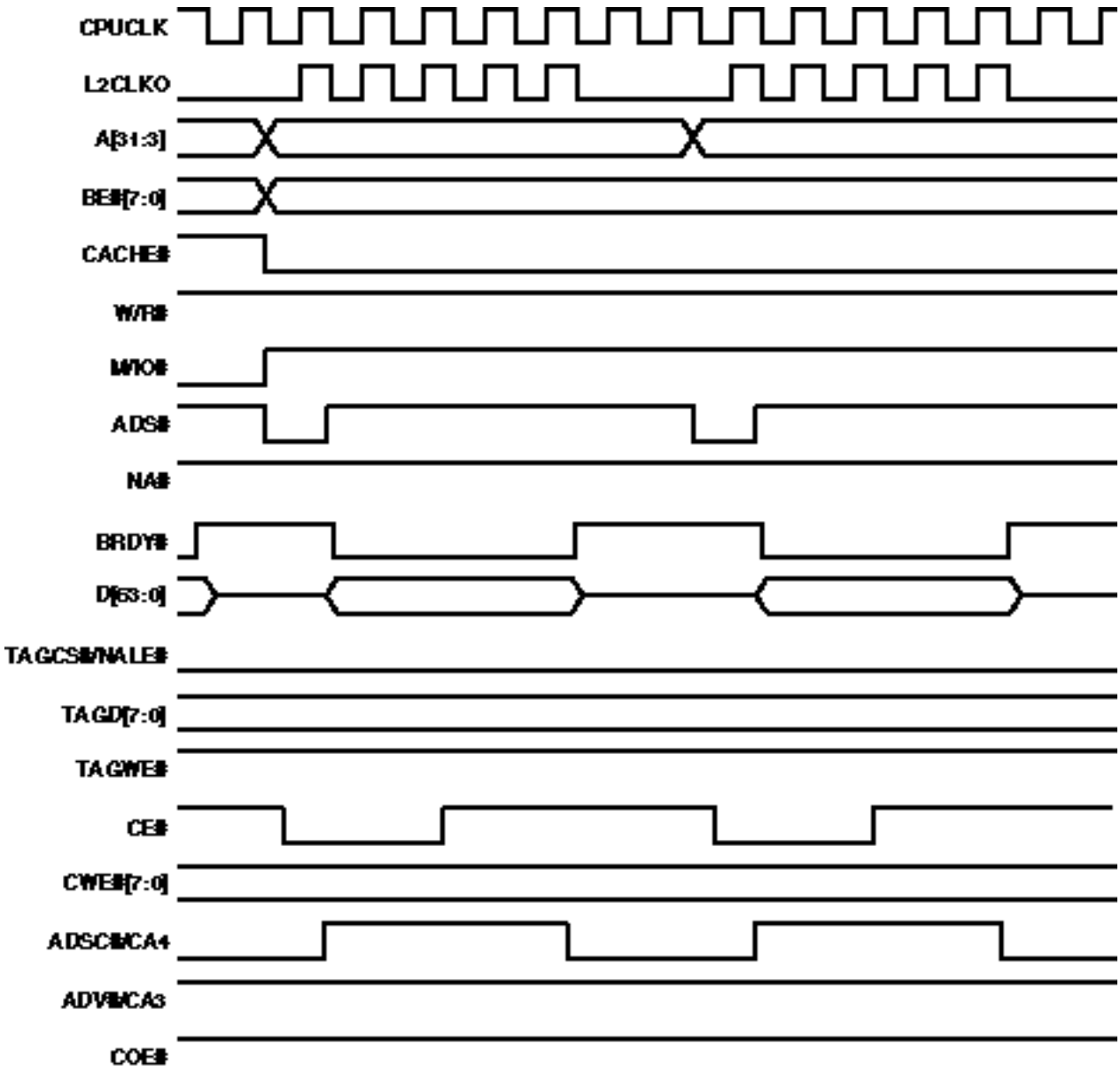


Figure 5-19. L2 Cache – Pipeline Synchronous, Burst Write Miss, Write Buffer Empty

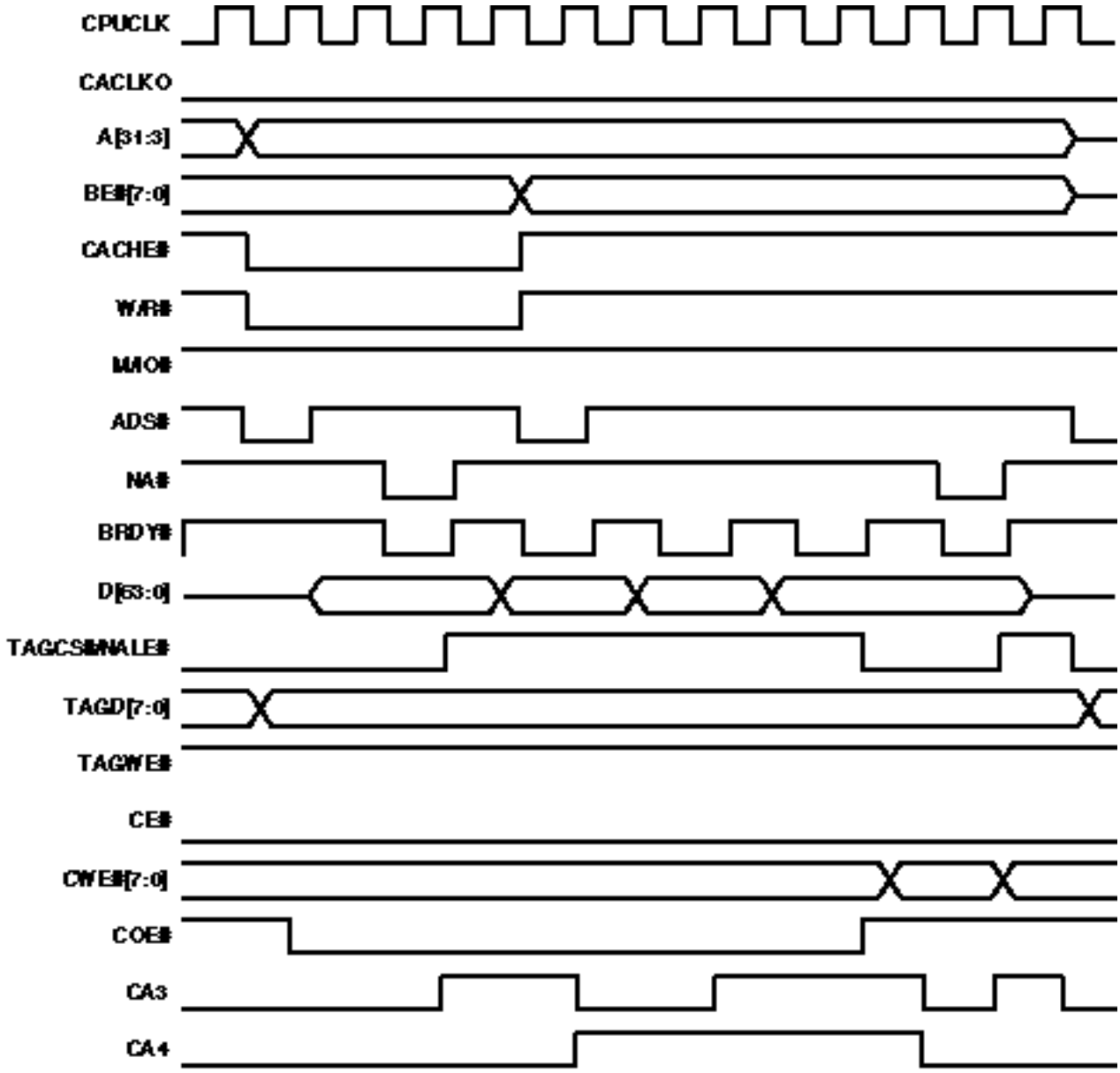


Figure 5-20. L2 Cache – Asynchronous, Burst Read 3-2-2-2 Hit

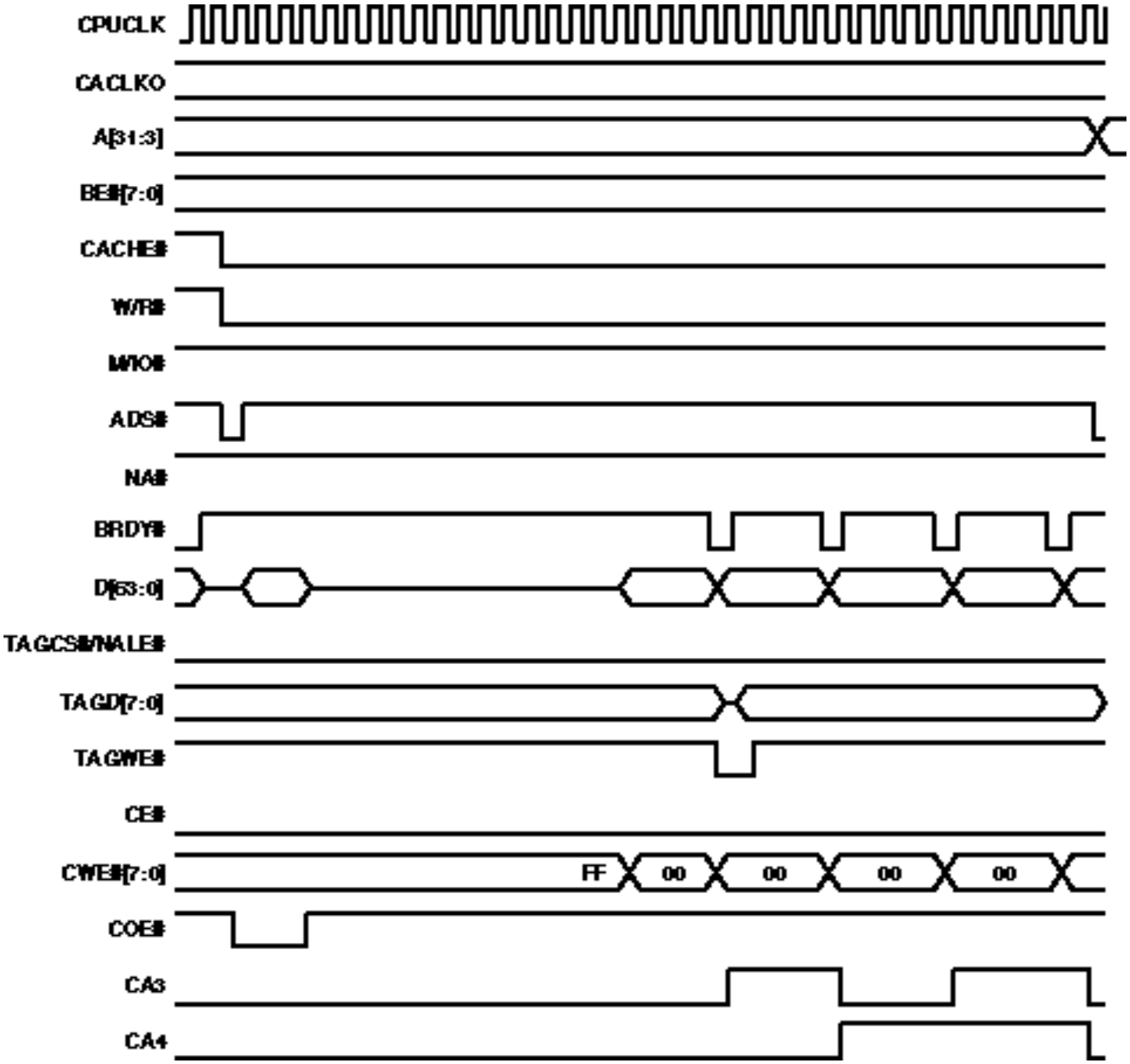


Figure 5-21. L2 Cache – Asynchronous, Burst Read Miss

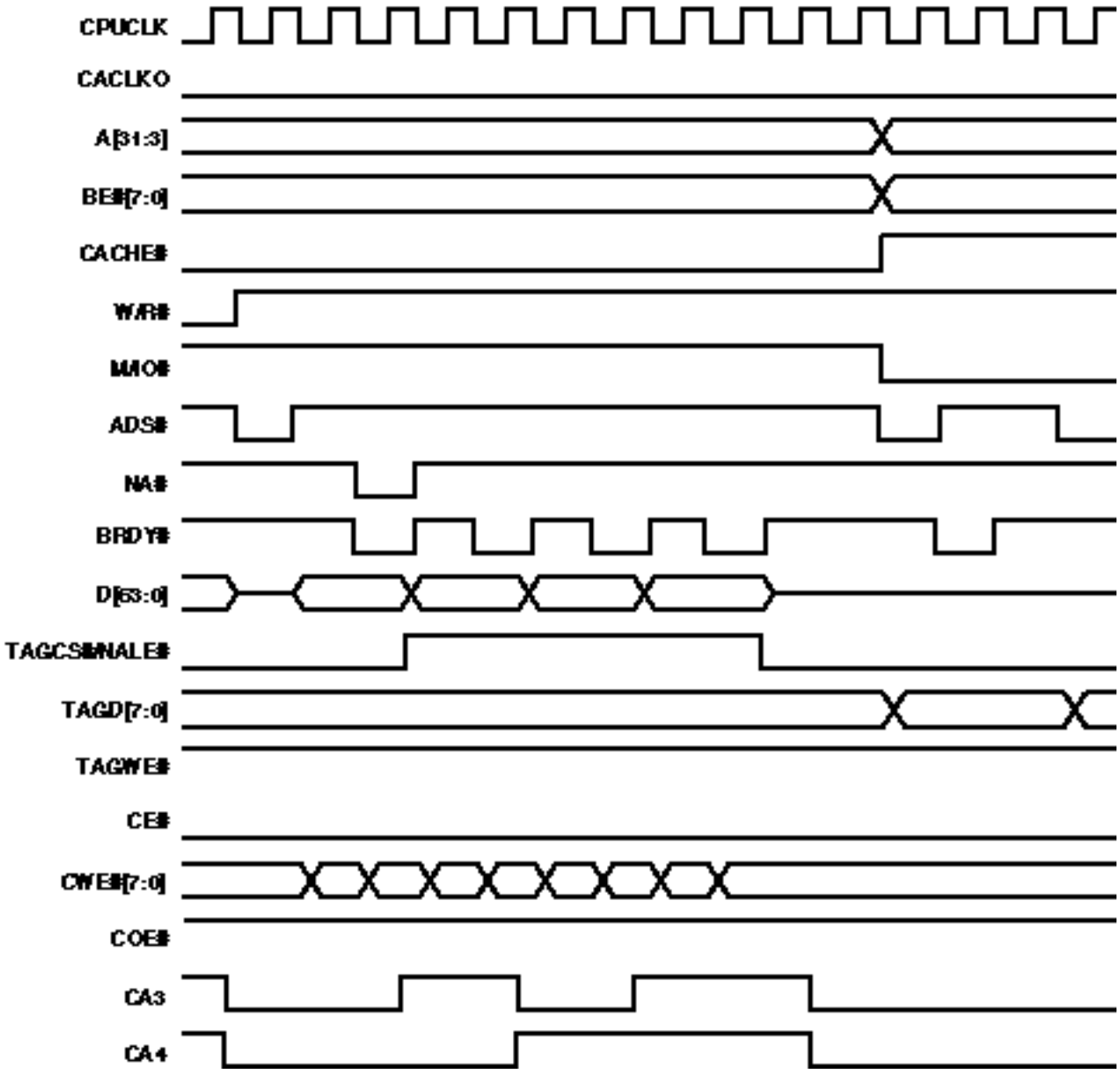


Figure 5-22. L2 Cache – Burst Write 3-2-2-2 Hit

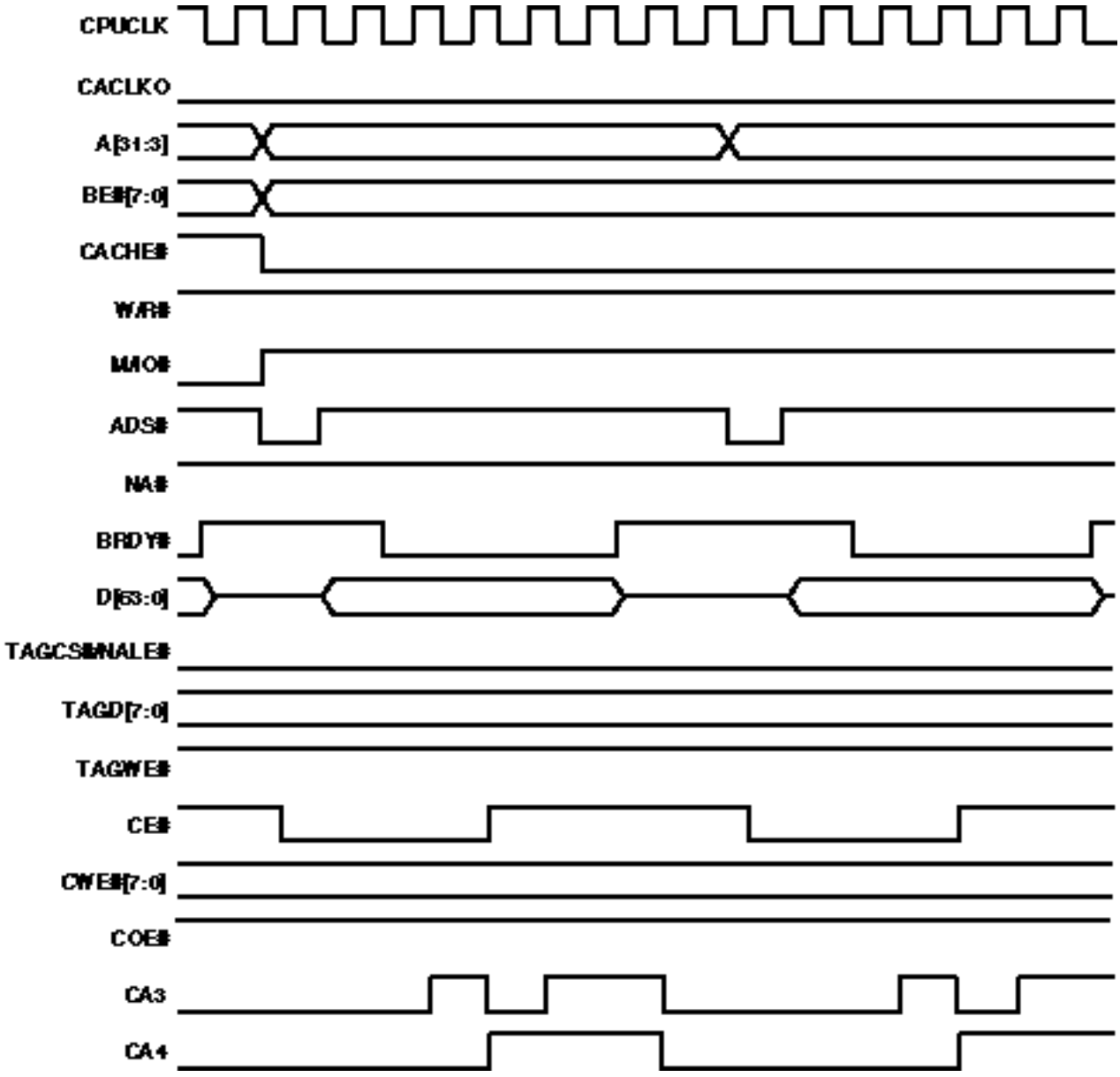


Figure 5-23. L2 Cache – Asynchronous, Burst Write Miss, Write Buffer Empty

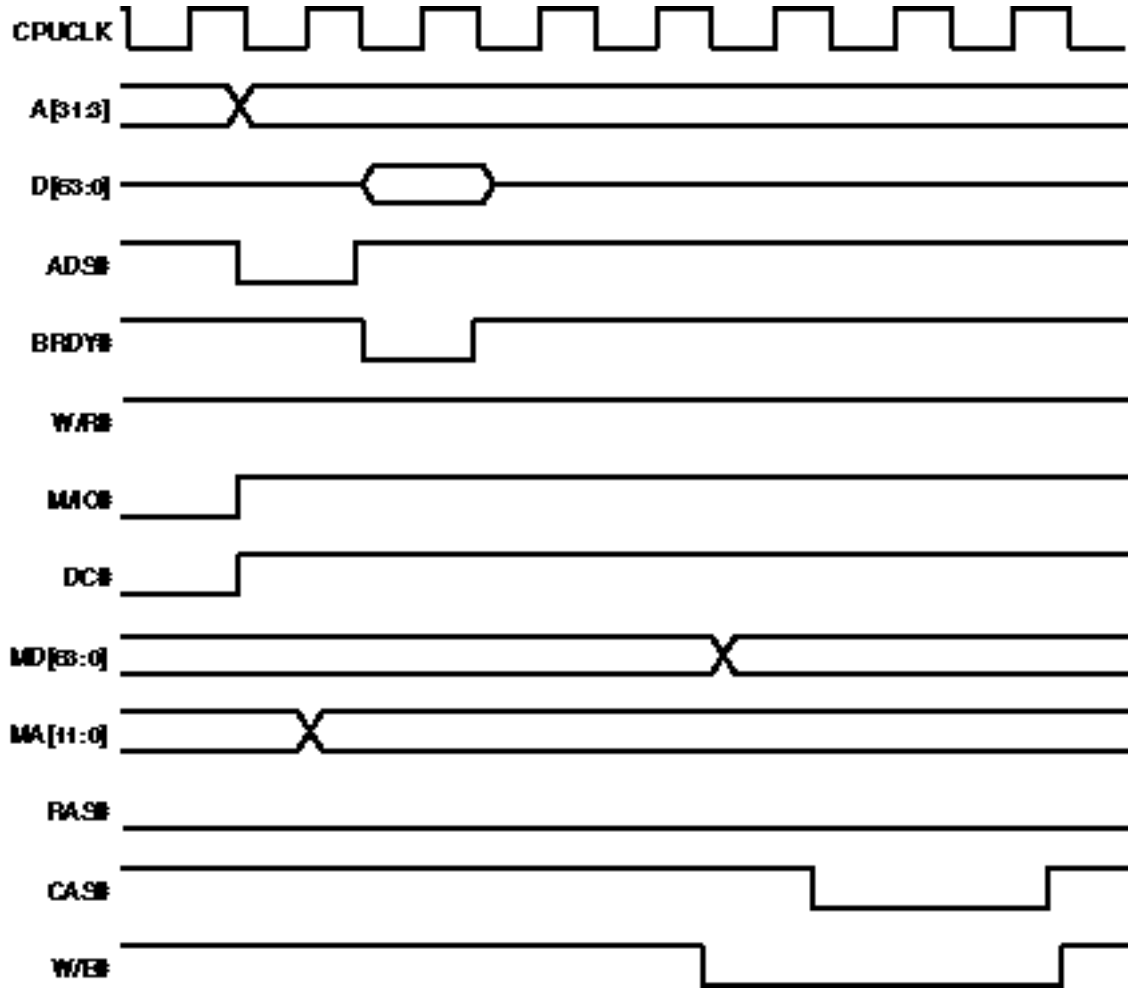


Figure 5-24. Fast Page Single Write – Page Hit

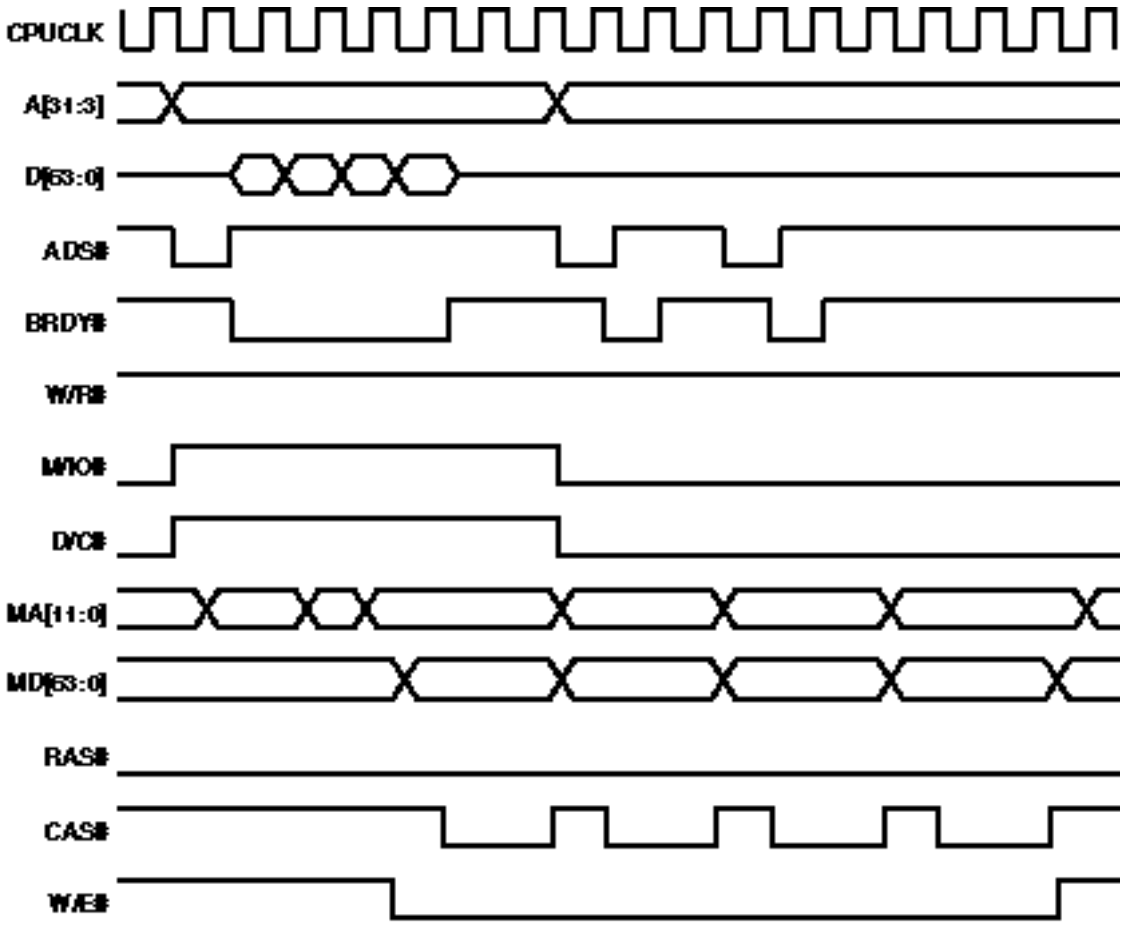


Figure 5-25. Fast Page Burst Write – Page Hit

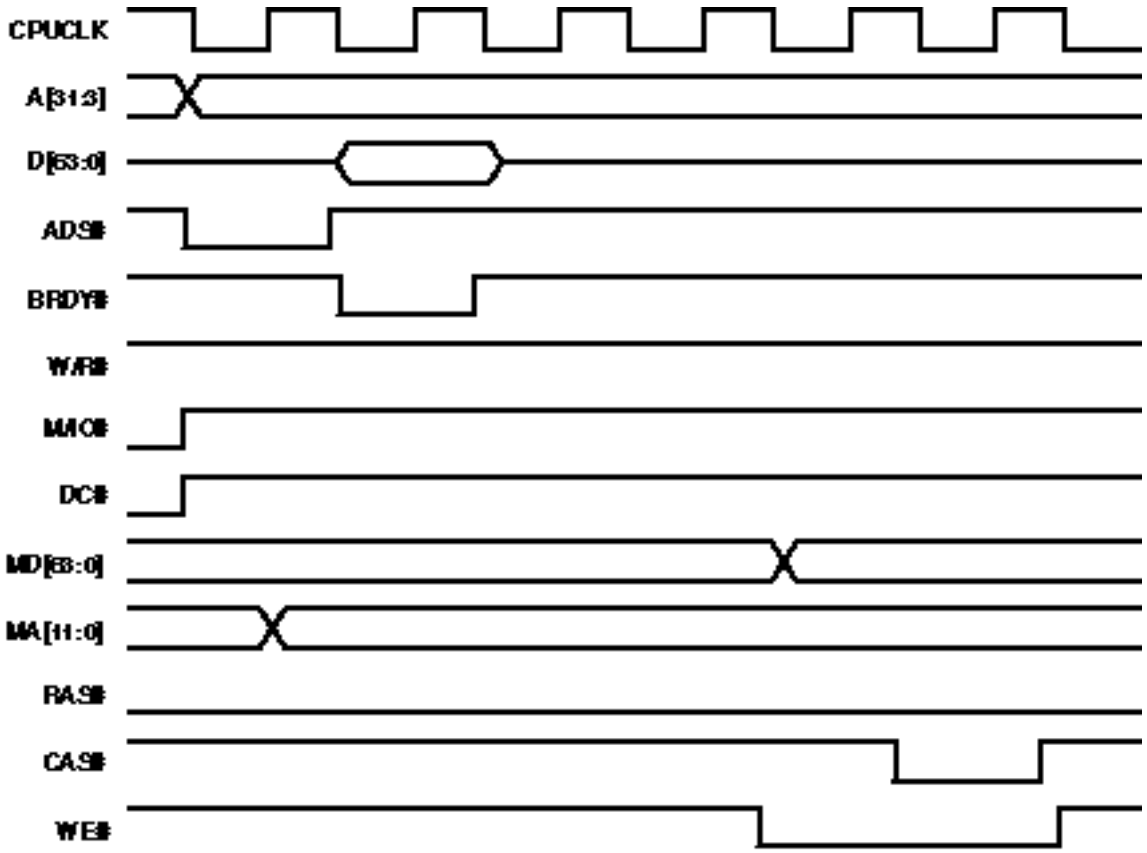


Figure 5-26. EDO Single Write – Page Hit

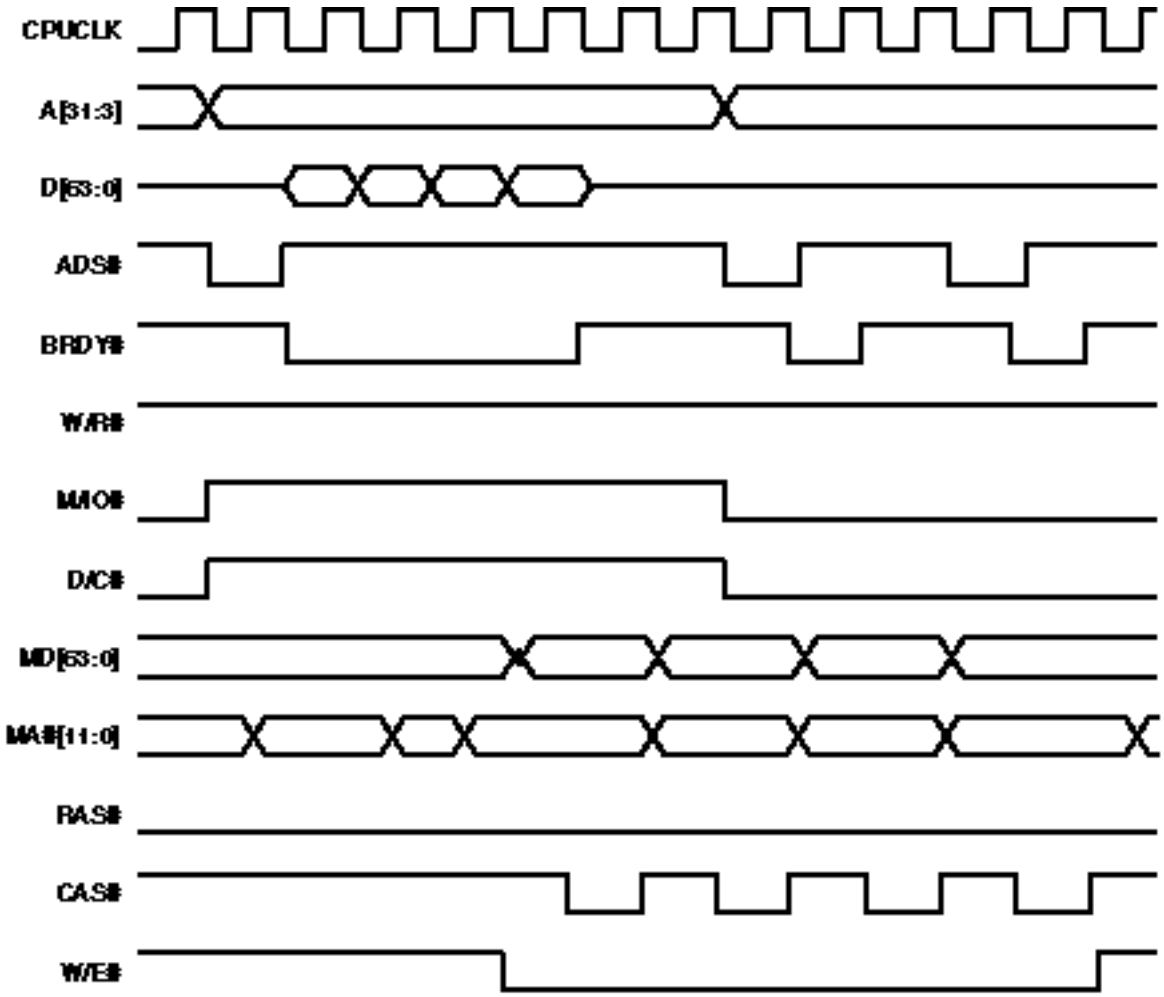


Figure 5-27. EDO Burst Write – Page Hit

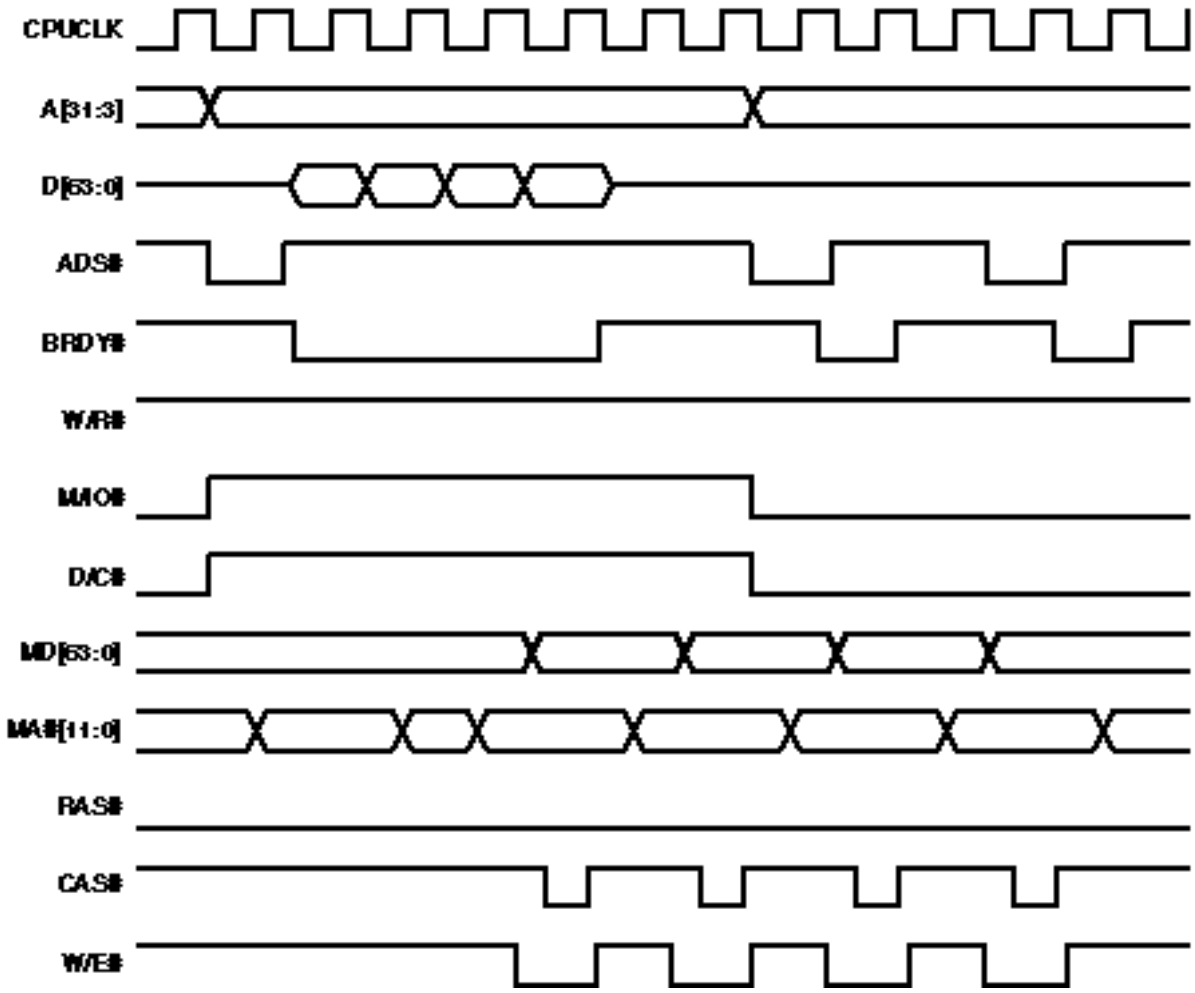


Figure 5-28. Burst EDO DRAM – Burst Write, Page Hit

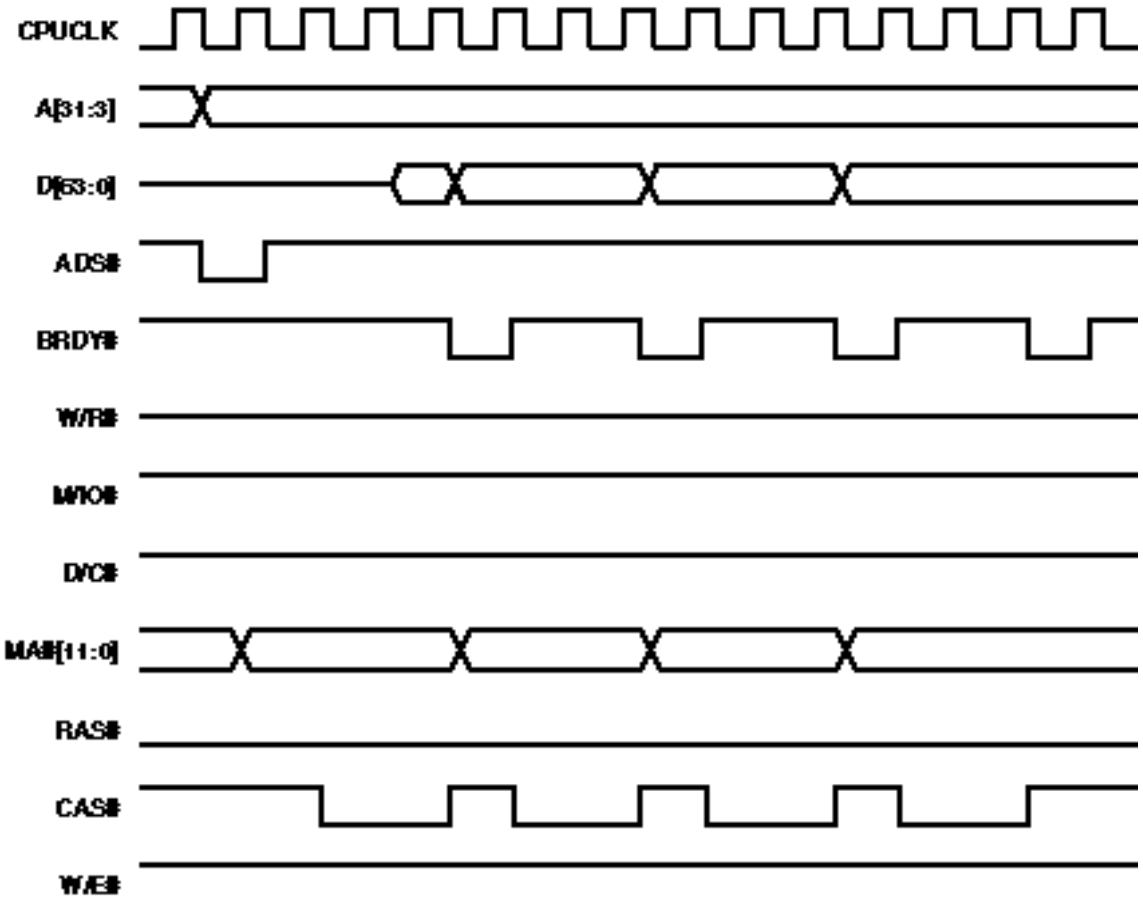


Figure 5-29. Fast Page Burst Read (5-3-3-3) – Page Hit (L2 cache disabled)

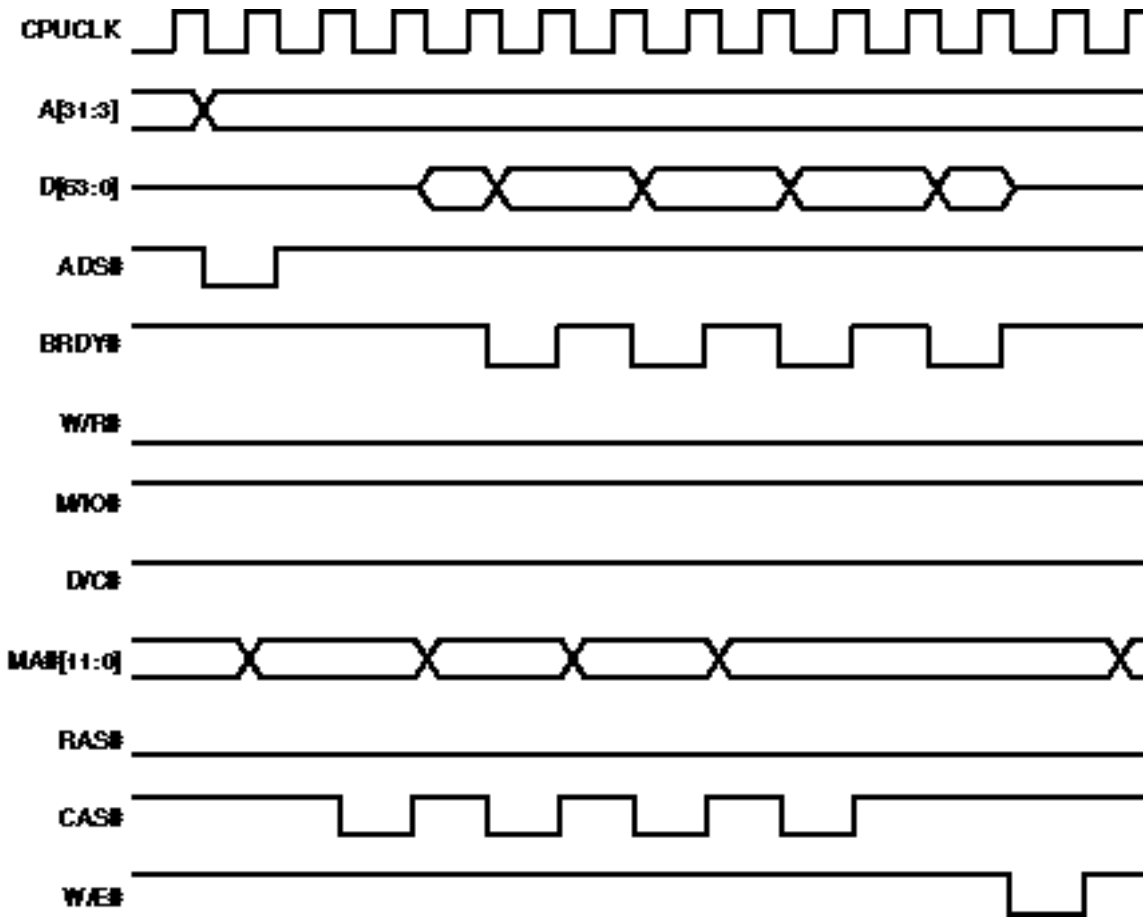


Figure 5-30. EDO Burst Read (5-2-2-2) – Page Hit (L2 cache disabled)

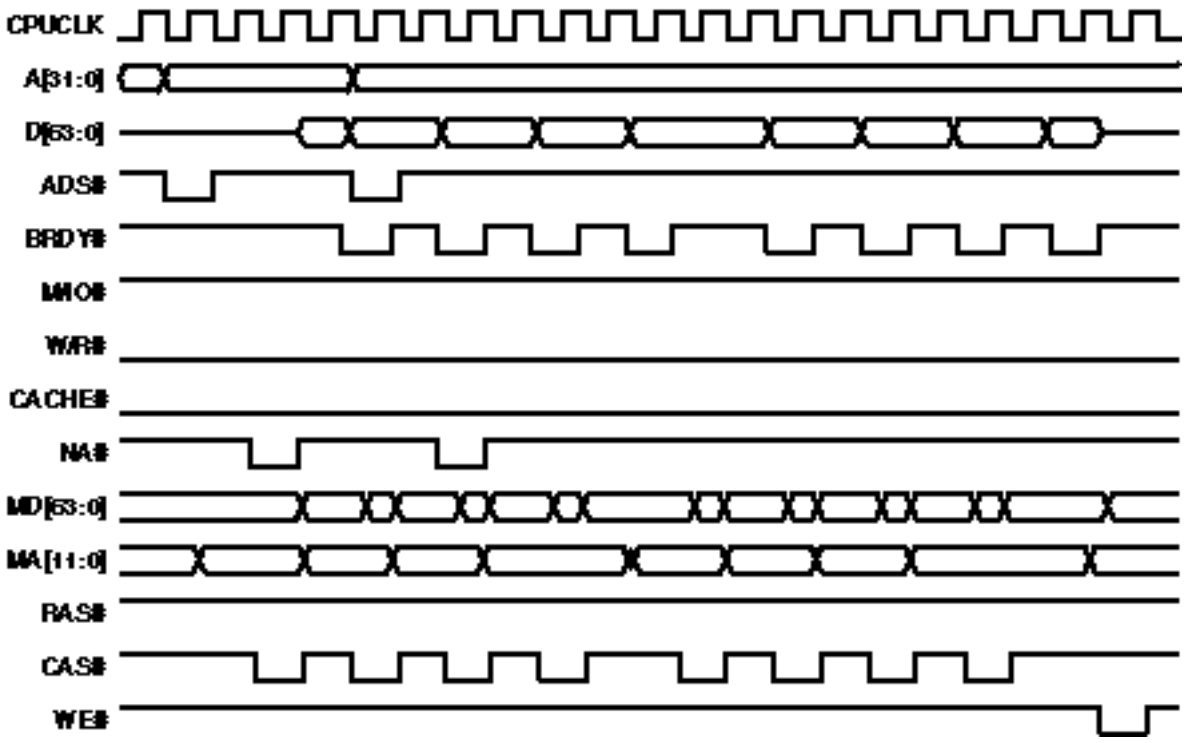


Figure 5-31. EDO Pipelined Burst Read (5-2-2-3-2-2-2)

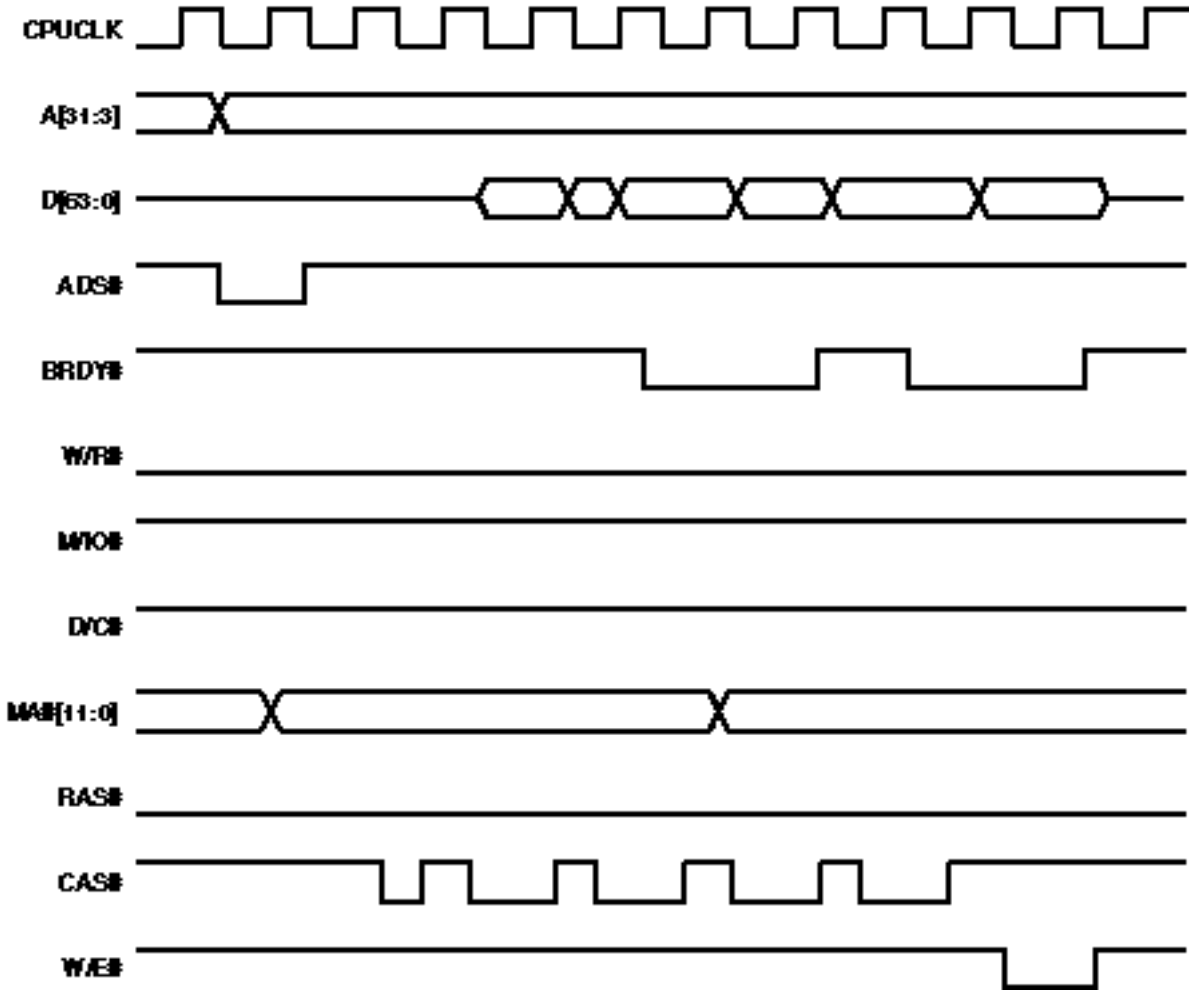


Figure 5-32. Burst EDO – Burst Read (6-1-2-1), Page Hit (L2 cache disabled)

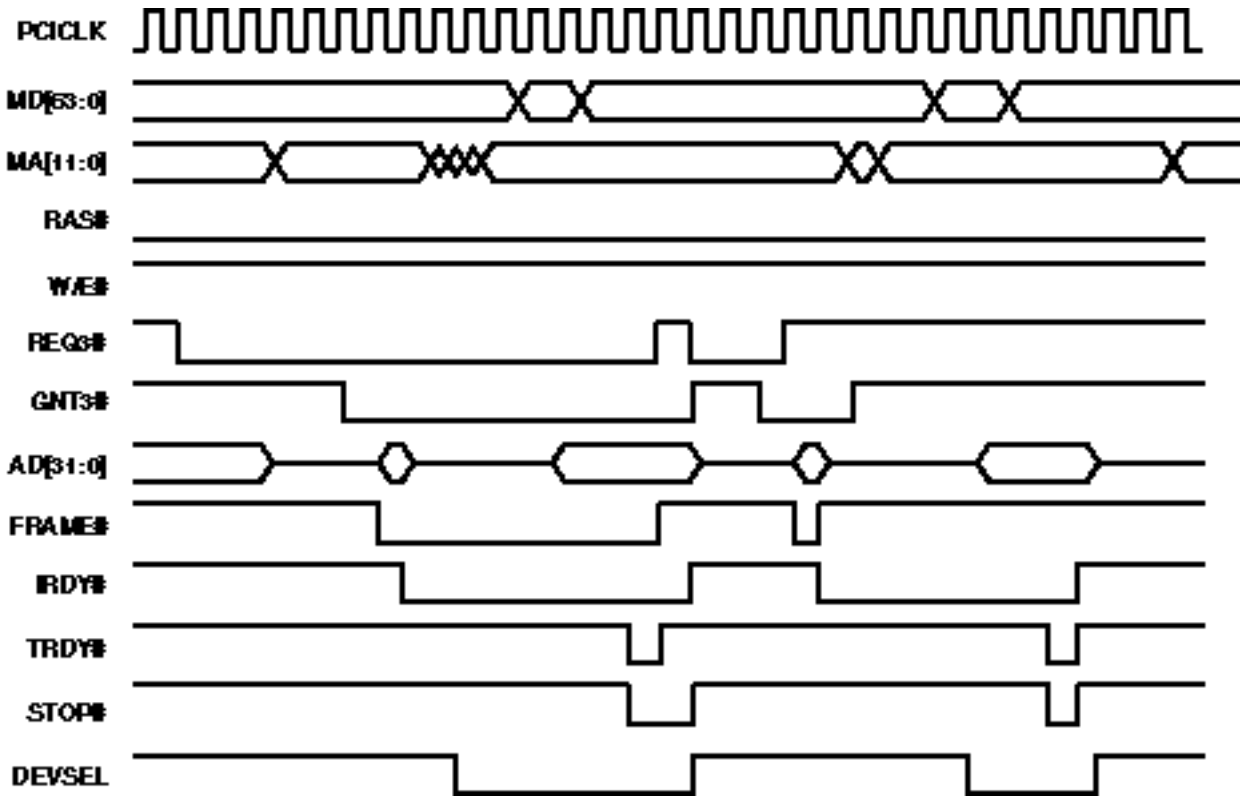


Figure 5-33. PCI Bus Master Read From 64-bit DRAM (no L1 cache hit)

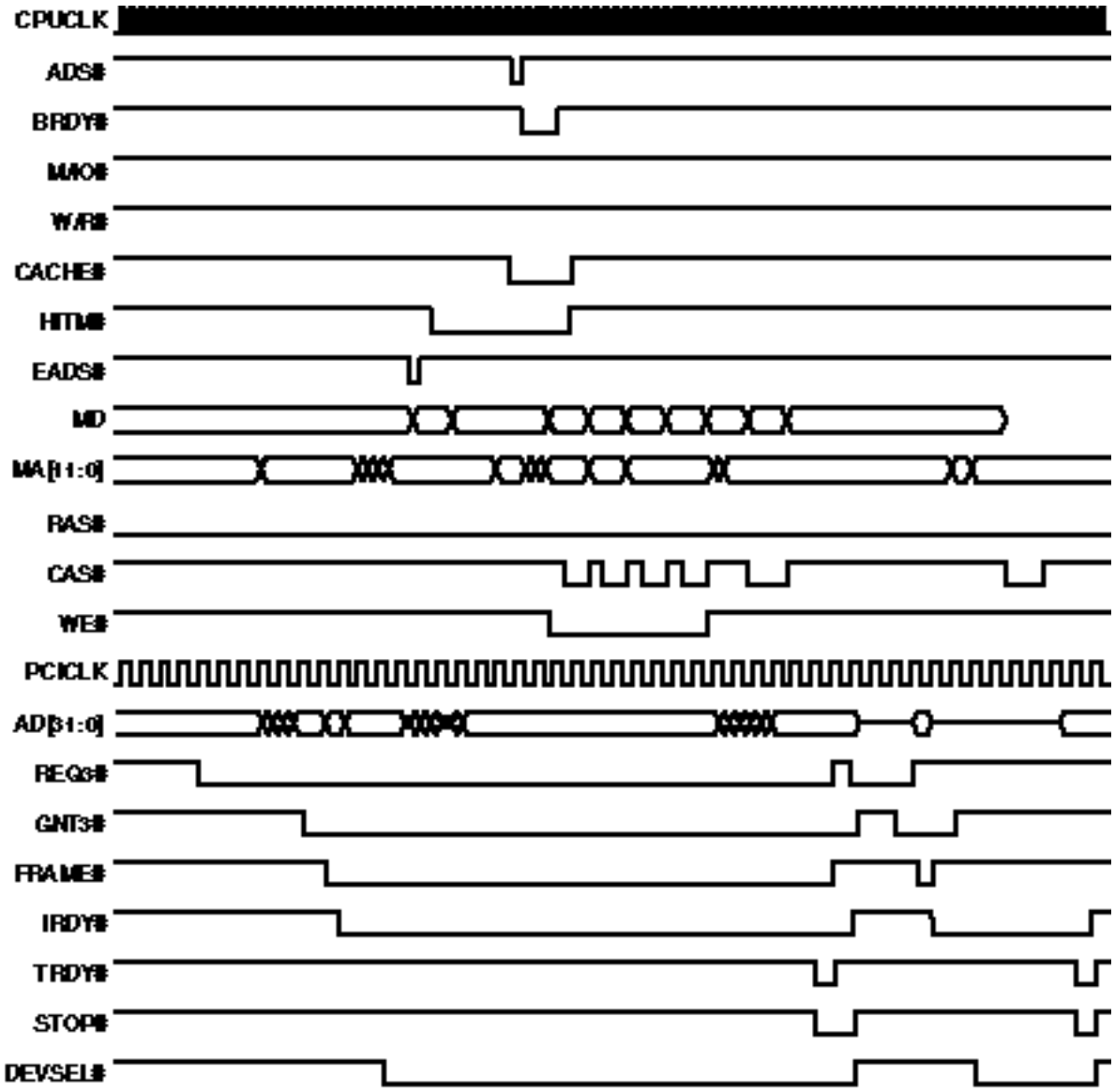


Figure 5-34. PCI Bus Master Read From 64-bit DRAM (L1 write-back)

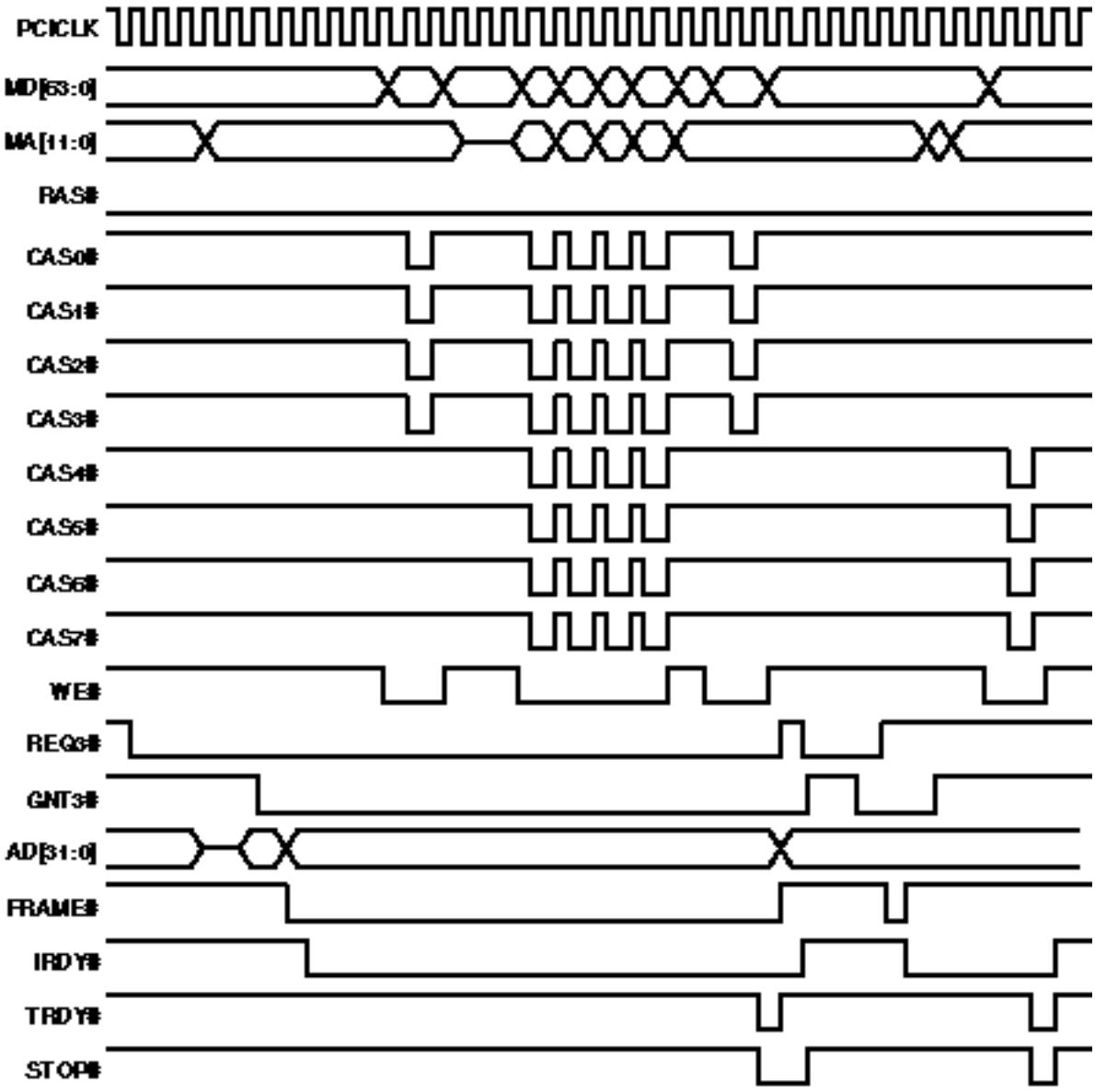


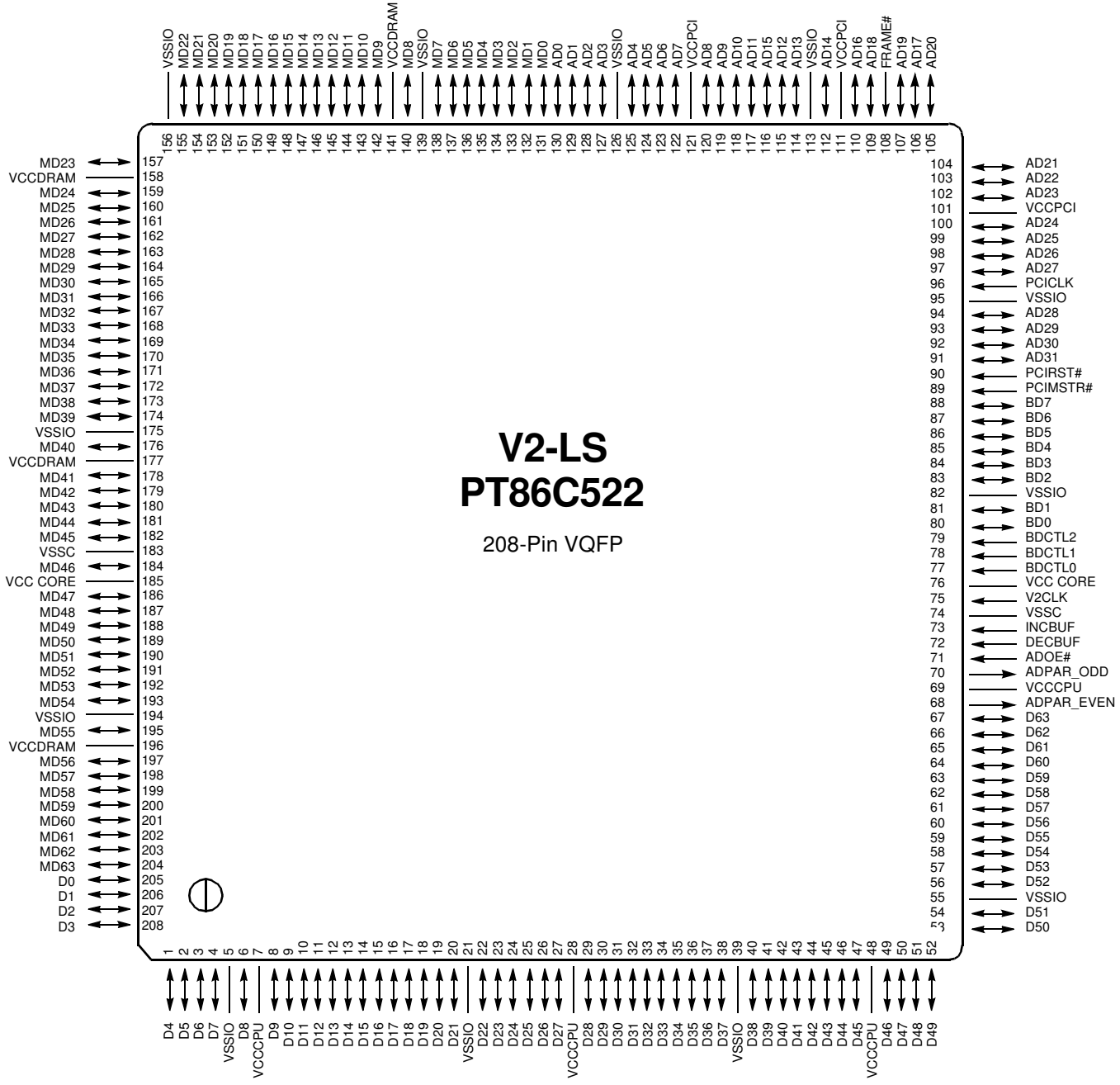
Figure 5-35. PCI Bus Master Write to 64-bit DRAM (L1 write-back)

V2-LS PT86C522
Data Book

V2-LS PT86C522

6. V2-LS PIN INFORMATION

6.1 Pin Diagram



6.2 Pin Cross Reference by Pin Number

Table 6-1. Pin Assignment Table (Arranged by Pin Number)

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
1	D4	I/O	T	3.3-V	VCCCPU	CPU
2	D5	I/O	T	3.3-V	VCCCPU	CPU
3	D6	I/O	T	3.3-V	VCCCPU	CPU
4	D7	I/O	T	3.3-V	VCCCPU	CPU
5	VSSIO	GND			VSSIO	GROUND
6	D8	I/O	T	3.3-V	VCCCPU	CPU
7	VCCCPU	PWR		3.3-V	VCCCPU	POWER
8	D9	I/O	T	3.3-V	VCCCPU	CPU
9	D10	I/O	T	3.3-V	VCCCPU	CPU
10	D11	I/O	T	3.3-V	VCCCPU	CPU
11	D12	I/O	T	3.3-V	VCCCPU	CPU
12	D13	I/O	T	3.3-V	VCCCPU	CPU
13	D14	I/O	T	3.3-V	VCCCPU	CPU
14	D15	I/O	T	3.3-V	VCCCPU	CPU
15	D16	I/O	T	3.3-V	VCCCPU	CPU
16	D17	I/O	T	3.3-V	VCCCPU	CPU
17	D18	I/O	T	3.3-V	VCCCPU	CPU
18	D19	I/O	T	3.3-V	VCCCPU	CPU
19	D20	I/O	T	3.3-V	VCCCPU	CPU
20	D21	I/O	T	3.3-V	VCCCPU	CPU
21	VSSIO	GND			VSSIO	GROUND
22	D22	I/O	T	3.3-V	VCCCPU	CPU
23	D23	I/O	T	3.3-V	VCCCPU	CPU
24	D24	I/O	T	3.3-V	VCCCPU	CPU
25	D25	I/O	T	3.3-V	VCCCPU	CPU
26	D26	I/O	T	3.3-V	VCCCPU	CPU
27	D27	I/O	T	3.3-V	VCCCPU	CPU
28	VCCCPU	PWR		3.3-V	VCCCPU	POWER
29	D28	I/O	T	3.3-V	VCCCPU	CPU

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 6-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
30	D29	I/O	T	3.3-V	VCCCPU	CPU
31	D30	I/O	T	3.3-V	VCCCPU	CPU
32	D31	I/O	T	3.3-V	VCCCPU	CPU
33	D32	I/O	T	3.3-V	VCCCPU	CPU
34	D33	I/O	T	3.3-V	VCCCPU	CPU
35	D34	I/O	T	3.3-V	VCCCPU	CPU
36	D35	I/O	T	3.3-V	VCCCPU	CPU
37	D36	I/O	T	3.3-V	VCCCPU	CPU
38	D37	I/O	T	3.3-V	VCCCPU	CPU
39	VSSIO	GND			VSSIO	GROUND
40	D38	I/O	T	3.3-V	VCCCPU	CPU
41	D39	I/O	T	3.3-V	VCCCPU	CPU
42	D40	I/O	T	3.3-V	VCCCPU	CPU
43	D41	I/O	T	3.3-V	VCCCPU	CPU
44	D42	I/O	T	3.3-V	VCCCPU	CPU
45	D43	I/O	T	3.3-V	VCCCPU	CPU
46	D44	I/O	T	3.3-V	VCCCPU	CPU
47	D45	I/O	T	3.3-V	VCCCPU	CPU
48	VCCCPU	PWR		3.3-V	VCCCPU	POWER
49	D46	I/O	T	3.3-V	VCCCPU	CPU
50	D47	I/O	T	3.3-V	VCCCPU	CPU
51	D48	I/O	T	3.3-V	VCCCPU	CPU
52	D49	I/O	T	3.3-V	VCCCPU	CPU
53	D50	I/O	T	3.3-V	VCCCPU	CPU
54	D51	I/O	T	3.3-V	VCCCPU	CPU
55	VSSIO	GND			VSSIO	GROUND
56	D52	I/O	T	3.3-V	VCCCPU	CPU
57	D53	I/O	T	3.3-V	VCCCPU	CPU
58	D54	I/O	T	3.3-V	VCCCPU	CPU
59	D55	I/O	T	3.3-V	VCCCPU	CPU

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 6-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
60	D56	I/O	T	3.3-V	VCCCPU	CPU
61	D57	I/O	T	3.3-V	VCCCPU	CPU
62	D58	I/O	T	3.3-V	VCCCPU	CPU
63	D59	I/O	T	3.3-V	VCCCPU	CPU
64	D60	I/O	T	3.3-V	VCCCPU	CPU
65	D61	I/O	T	3.3-V	VCCCPU	CPU
66	D62	I/O	T	3.3-V	VCCCPU	CPU
67	D63	I/O	T	3.3-V	VCCCPU	CPU
68	ADPAR_EVEN	O		3.3-V	VCCCPU	V1-LS/V2-LS
69	VCCCPU	PWR		3.3-V	VCCCPU	POWER
70	ADPAR_ODD	O		3.3-V	VCCCPU	V1-LS/V2-LS
71	ADOE#	I	T	3.3-V	VCCCPU	V1-LS/V2-LS
72	DECBUF	I	T	3.3-V	VCCCPU	V1-LS/V2-LS
73	INCBUF	I	T	3.3-V	VCCCPU	V1-LS/V2-LS
74	VSSC	GND			VSSC	GROUND
75	V2CLK	I	T	3.3-V	VCCCPU	V1-LS/V2-LS
76	VCC CORE	GND		3.3-V	VCCC	POWER
77	BDCTL0	I	T	3.3-V	VCCCPU	V1-LS/V2-LS
78	BDCTL1	I	T	3.3-V	VCCCPU	V1-LS/V2-LS
79	BDCTL2	I	T	3.3-V	VCCCPU	V1-LS/V2-LS
80	BD0	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
81	BD1	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
82	VSSIO	GND			VSSIO	GROUND
83	BD2	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
84	BD3	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
85	BD4	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
86	BD5	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
87	BD6	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
88	BD7	I/O	T	3.3-V	VCCCPU	V1-LS/V2-LS
89	PCIMSTR#	I	T	3.3-V	VCCCPU	V1-LS/V2-LS

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 6-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
90	PCIRST#	I	T	3.3-V/5-V	VCCPCI	PCI
91	AD31	I/O	T	3.3-V/5-V	VCCPCI	PCI
92	AD30	I/O	T	3.3-V/5-V	VCCPCI	PCI
93	AD29	I/O	T	3.3-V/5-V	VCCPCI	PCI
94	AD28	I/O	T	3.3-V/5-V	VCCPCI	PCI
95	VSSIO	GND			VSSIO	GROUND
96	PCICLK	I	C	3.3-V/5-V	VCCPCI	PCI
97	AD27	I/O	T	3.3-V/5-V	VCCPCI	PCI
98	AD26	I/O	T	3.3-V/5-V	VCCPCI	PCI
99	AD25	I/O	T	3.3-V/5-V	VCCPCI	PCI
100	AD24	I/O	T	3.3-V/5-V	VCCPCI	PCI
101	VCCPCI	PWR		3.3-V/5-V	VCCPCI	POWER
102	AD23	I/O	T	3.3-V/5-V	VCCPCI	PCI
103	AD22	I/O	T	3.3-V/5-V	VCCPCI	PCI
104	AD21	I/O	T	3.3-V/5-V	VCCPCI	PCI
105	AD20	I/O	T	3.3-V/5-V	VCCPCI	PCI
106	AD17	I/O	T	3.3-V/5-V	VCCPCI	PCI
107	AD19	I/O	T	3.3-V/5-V	VCCPCI	PCI
108	FRAME#	I	T	3.3-V/5-V	VCCPCI	PCI
109	AD18	I/O	T	3.3-V/5-V	VCCPCI	PCI
110	AD16	I/O	T	3.3-V/5-V	VCCPCI	PCI
111	VCCPCI	PWR		3.3-V/5-V	VCCPCI	POWER
112	AD14	I/O	T	3.3-V/5-V	VCCPCI	PCI
113	VSSIO	GND			VSSIO	GROUND
114	AD13	I/O	T	3.3-V/5-V	VCCPCI	PCI
115	AD12	I/O	T	3.3-V/5-V	VCCPCI	PCI
116	AD15	I/O	T	3.3-V/5-V	VCCCPU	PCI
117	AD11	I/O	T	3.3-V/5-V	VCCPCI	PCI
118	AD10	I/O	T	3.3-V/5-V	VCCPCI	PCI
119	AD9	I/O	T	3.3-V/5-V	VCCPCI	PCI

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 6-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
120	AD8	I/O	T	3.3-V/5-V	VCCPCI	PCI
121	VCCPCI	PWR		3.3-V/5-V	VCCPCI	POWER
122	AD7	I/O	T	3.3-V/5-V	VCCPCI	PCI
123	AD6	I/O	T	3.3-V/5-V	VCCPCI	PCI
124	AD5	I/O	T	3.3-V/5-V	VCCPCI	PCI
125	AD4	I/O	T	3.3-V/5-V	VCCPCI	PCI
126	VSSIO	GND			VSSIO	GROUND
127	AD3	I/O	T	3.3-V/5-V	VCCPCI	PCI
128	AD2	I/O	T	3.3-V/5-V	VCCPCI	PCI
129	AD1	I/O	T	3.3-V/5-V	VCCPCI	PCI
130	AD0	I/O	T	3.3-V/5-V	VCCPCI	PCI
131	MD0	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
132	MD1	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
133	MD2	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
134	MD3	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
135	MD4	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
136	MD5	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
137	MD6	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
138	MD7	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
139	VSSIO	GND			VSSIO	GROUND
140	MD8	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
141	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER
142	MD9	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
143	MD10	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
144	MD11	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
145	MD12	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
146	MD13	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
147	MD14	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
148	MD15	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
149	MD16	I/O	T	3.3-V/5-V	VCCDRAM	DRAM

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 6-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
150	MD17	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
151	MD18	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
152	MD19	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
153	MD20	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
154	MD21	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
155	MD22	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
156	VSSIO	GND			VSSIO	GROUND
157	MD23	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
158	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER
159	MD24	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
160	MD25	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
161	MD26	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
162	MD27	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
163	MD28	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
164	MD29	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
165	MD30	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
166	MD31	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
167	MD32	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
168	MD33	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
169	MD34	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
170	MD35	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
171	MD36	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
172	MD37	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
173	MD38	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
174	MD39	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
175	VSSIO	GND			VSSIO	GROUND
176	MD40	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
177	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER
178	MD41	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
179	MD42	I/O	T	3.3-V/5-V	VCCDRAM	DRAM

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 6-1. Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
180	MD43	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
181	MD44	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
182	MD45	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
183	VSSC	GND			VSSC	GROUND
184	MD46	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
185	VCC CORE	PWR		3.3-V	VCCC	POWER
186	MD47	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
187	MD48	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
188	MD49	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
189	MD50	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
190	MD51	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
191	MD52	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
192	MD53	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
193	MD54	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
194	VSSIO	GND			VSSIO	GROUND
195	MD55	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
196	VCCDRAM	PWR		3.3-V/5-V	VCCDRAM	POWER
197	MD56	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
198	MD57	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
199	MD58	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
200	MD59	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
201	MD60	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
202	MD61	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
203	MD62	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
204	MD63	I/O	T	3.3-V/5-V	VCCDRAM	DRAM
205	D0	I/O	T	3.3-V	VCCCPU	CPU
206	D1	I/O	T	3.3-V	VCCCPU	CPU
207	D2	I/O	T	3.3-V	VCCCPU	CPU
208	D3	I/O	T	3.3-V	VCCCPU	CPU

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

6.3 Pin Cross Reference by Pin Name

Table 6-2. Pin Assignment Table (Arranged by Pin Name)

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
AD0	130	AD29	93	D12	11
AD1	129	AD30	92	D13	12
AD2	128	AD31	91	D14	13
AD3	127	ADOE#	71	D15	14
AD4	125	ADPAR_EVEN	68	D16	15
AD5	124	ADPAR_ODD	70	D17	16
AD6	123	BD0	80	D18	17
AD7	122	BD1	81	D19	18
AD8	120	BD2	83	D20	19
AD9	119	BD3	84	D21	20
AD10	118	BD4	85	D22	22
AD11	117	BD5	86	D23	23
AD12	115	BD6	87	D24	24
AD13	114	BD7	88	D25	25
AD14	112	BDCTL0	77	D26	26
AD15	116	BDCTL1	78	D27	27
AD16	110	BDCTL2	79	D28	29
AD17	106	D0	205	D29	30
AD18	109	D1	206	D30	31
AD19	107	D2	207	D31	32
AD20	105	D3	208	D32	33
AD21	104	D4	1	D33	34
AD22	103	D5	2	D34	35
AD23	102	D6	3	D35	36
AD24	100	D7	4	D36	37
AD25	99	D8	6	D37	38
AD26	98	D9	8	D38	40
AD27	97	D10	9	D39	41
AD28	94	D11	10	D40	42

Table 6-2. Pin Assignment Table (Arranged by Pin Name)

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
D41	43	MD5	136	MD36	171
D42	44	MD6	137	MD37	172
D43	45	MD7	138	MD38	173
D44	46	MD8	140	MD39	174
D45	47	MD9	142	MD40	176
D46	49	MD10	143	MD41	178
D47	50	MD11	144	MD42	179
D48	51	MD12	145	MD43	180
D49	52	MD13	146	MD44	181
D50	53	MD14	147	MD45	182
D51	54	MD15	148	MD46	184
D52	56	MD16	149	MD47	186
D53	57	MD17	150	MD48	187
D54	58	MD18	151	MD49	188
D55	59	MD19	152	MD50	189
D56	60	MD20	153	MD51	190
D57	61	MD21	154	MD52	191
D58	62	MD22	155	MD53	192
D59	63	MD23	157	MD54	193
D60	64	MD24	159	MD55	195
D61	65	MD25	160	MD56	197
D62	66	MD26	161	MD57	198
D63	67	MD27	162	MD58	199
DECBUF	72	MD28	163	MD59	200
FRAME#	108	MD29	164	MD60	201
INCBUF	73	MD30	165	MD61	202
MD0	131	MD31	166	MD62	203
MD1	132	MD32	167	MD63	204
MD2	133	MD33	168	PCICLK	96
MD3	134	MD34	169	PCIMSTR#	89
MD4	135	MD35	170	PCIRST#	90

Table 6-2. Pin Assignment Table (Arranged by Pin Name)

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
V2CLK	75	VCCDRAM	141	VSSIO	55
VCC CORE	76	VCCPCI	101	VSSIO	82
VCC CORE	185	VCCPCI	121	VSSIO	95
VCCCPU	7	VCCPCI	111	VSSIO	139
VCCCPU	28	VSSC	74	VSSIO	156
VCCCPU	48	VSSC	183	VSSIO	175
VCCCPU	69	VSSIO	5	VSSIO	194
VCCDRAM	158	VSSIO	21	VSSIO	113
VCCDRAM	177	VSSIO	39	VSSIO	126
VCCDRAM	196				

7. V2-LS DETAILED PIN DESCRIPTIONS

This chapter contains a detailed functional description of the pins on PT86C522. For ease of reference, the pins have been arranged alphabetically within each of the following eight functional interface groups:

- CPU Interface (CPU)
- DRAM Interface (DRAM)
- PCI Interface (PCI)
- V1-LS / V2-LS Interface (V1-LS / V2-LS)
- Power and Ground (POWER / GROUND)

The '#' symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. Signal names without the # symbol indicate that the signal is active, or asserted at the high voltage level.

The '/' symbol between signal names indicates that the signals are multiplexed and use the same pin for all functions.

The following conventions have been used to describe the pin type: 'I' = input-only pins; 'O' = output-only pins; 'I/O' = bi-directional pins; 'PWR' = power pins, and 'GND' = ground pins. The pin type is defined relative to the Vesuvius-LS platform.

For a list of pins arranged by pin number, refer to Table 6-1 on page 2-266. For a list of pins arranged by pin name, refer to Table 6-2 on page 2-273.

7.1 CPU Interface

Pin Name	Type	Description
D[63:0]	I/O	**CPU DATA BUS D[63:0]:** These are the upper and lower bits of the 64-bit Pentium processor data bus.

7.2 DRAM Interface

Pin Name	Type	Description
MD[63:0]	I/O	**DRAM DATA BUS:** These pins are dedicated DRAM array data pins. These pins are inputs during DRAM read cycles and outputs during DRAM write cycles.

7.3 PCI Interface

Pin Name	Type	Description
AD[31:0]	I/O	**ADDRESS/DATA MULTIPLEXED [31:0]:** These signals are multiplexed on the same pins. Each transaction is initiated by a 32-bit physical address phase which is followed by one or more data phases. These bus transactions support both read and write bursts. AD[31:0] are also used as IDSELs in the Configuration Cycle.
FRAME#	I	**FRAME#:** FRAME# is driven by the current initiator and indicates the start and duration of the transaction. FRAME# is deasserted to indicate that the initiator is ready to complete the final data phase. A transaction may consist of one or more data transfers between the current initiator and the currently-addresses target.
PCICLK	I	**PCI CLOCK INPUT:** This is a clock generated by V1-LS and is derived from LCLK and delayed by 1/2+ clock cycle or is the inversion of LCLK.
PCIRST#	I	**PCI RESET#:** This signal is the PCI reset signal.

7.4 V1-LS/V2-LS Interface

Pin Name	Type	Description
ADOE#	I	**AD BUS OUTPUT ENABLE#:** When this signal is active, V2-LS drives the PCI AD bus AD[31:0].
ADPAR_EVEN	O	**AD BUS PARITY EVEN:** This signal indicates the PCI AD Bus parity when V2-LS samples PCI AD Bus.
ADPAR_ODD	O	**AD BUS PARITY ODD:** Output to V1-LS to indicate PCI AD Bus parity.
BD[7:0]	I/O	**BURST DATA BUS [7:0]:** This 8-bit bus carries different information during various phases.
BDCTL[2:0]	I	**BUFFER DATA CONTROL [2:0]:** These pins indicate datapath control signals from V1-LS.
DECBUF	I	**DECREMENT WRITE BUFFER COUNTER:** This input is used to decrease the pointer on the 8 level write buffer.
INCBUF	I	**INCREMENT WRITE BUFFER COUNTER:** This input is used to increase the pointer on the 8 level write buffer.

7.4 V1-LS/V2-LS Interface *(cont.)*

Pin Name	Type	Description
PCIMSTR#	I	**PCI MASTER#:** This output from V1-LS indicates that Vesuvius-LS is responding to a PCI master cycle.
V2CLK	I	**V2 CLOCK:** Clock for the interface between V1-LS and V2-LS.

7.5 Power and Ground

Pin Name	Type	Description
VCCCPU	PWR	**VCCCPU:** These are I/O power pins for VCCCPU power plane.
VCC CORE	PWR	**VCC CORE:** These are I/O power pins for VCC CORE power plane.
VCCPCI	PWR	**VCCPCI:** These are I/O power pins for VCCPCI power plane.
VCCDRAM	PWR	**VCCDRAM:** These are I/O power pins for VCCDRAM power plane.
VSSIO	GND	**VSSIO:** These are I/O ground pins.
VSSC	GND	**VSSC:** These are I/O ground pins.

8. V2-LS FUNCTIONAL DESCRIPTION

Refer to Chapter 3 in Section I (V1-LS PT86C521 data book) for functional description on V2-LS.

8.1 Functional Block Diagram

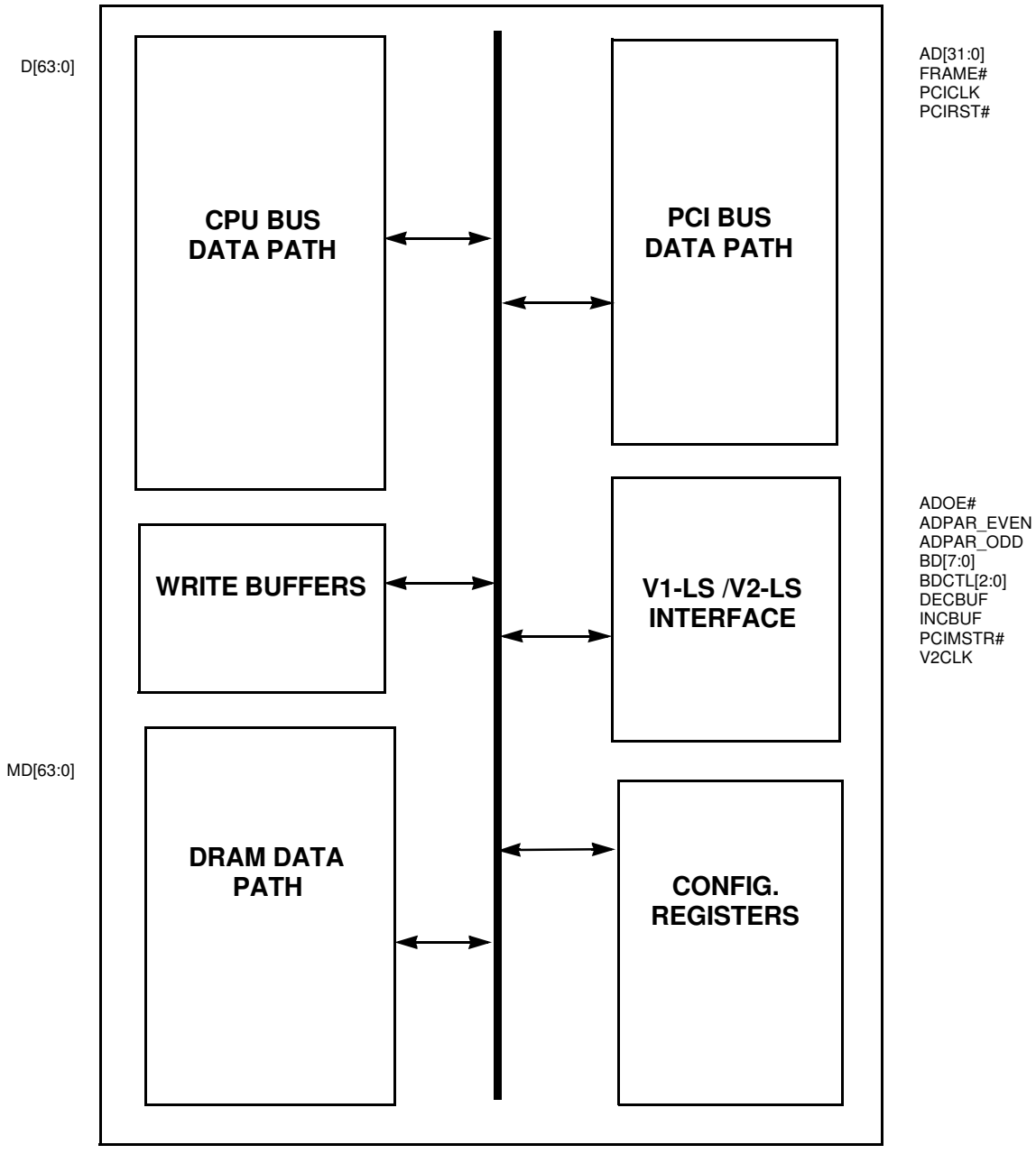


Figure 8-1. V2-LS Functional Block Diagram

9. V2-LS REGISTER INFORMATION

This chapter describes the registers contained in the V2-LS device. The registers are divided into the following groups:

- Version ID Register
- Configuration Register

9.1 Register Summary Table

This table shows the index numbers and page cross-references to detailed register descriptions.

Index	Register Name	Abbreviation	Page
108H	Version ID Register	V2LS VID	2-281
109H	Configuration Register	V2LS INC	2-282
10AH	Miscellaneous Status Register	V2S	2-283

9.2 Version ID Register (V2LS VID)

Index: 108H

Bit	Description	Name	Reset State
0	V2-LS Version ID Number [0]	V2LS_E_ID0	'0'
1	V2-LS Version ID Number [1]	V2LS_E_ID1	'0'
2	V2-LS Version ID Number [2]	V2LS_E_ID2	'0'
3	V2-LS Version ID Number [3]	V2LS_E_ID3	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	V2-LS Version ID Number [0]	V2LS_O_ID0	'0'
9	V2-LS Version ID Number [1]	V2LS_O_ID1	'0'
10	V2-LS Version ID Number [2]	V2LS_O_ID2	'0'
11	V2-LS Version ID Number [3]	V2LS_O_ID3	'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
3:0	**V2-LS Version ID Number [3:0]:** These bits indicate the version ID for V2-LS. 3H = Rev. AA 4H = Rev. BB
7:4	Reserved
11:8	**V2LS Version ID Number [3:0]:** 3H = Rev. AA 4H = Rev. BB
15:12	Reserved

9.3 Configuration Register (V2LS INC)

Index: 109H

Bit	Description	Name	Reset State
0	Enable Fast PCI Master Address Transfer	ENFSTPCIM_ XFR_E	'0'
1	Reserved		'0'
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Enable V2-LS Process Monitor	ENPROCMON_E	'0'
8	Enable Fast PCI Master Address Transfer	ENFSTPCIM_ XFR_O	'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Enable V2-LS Process Monitor	ENPROCMON_O	'0'

Bit	Description
0	**Enable Fast PCI Master Address Transfer:** '0'= disable; '1'= enable.
6:1	Reserved
7	**Enable V2-LS Process Monitor:** Setting this bit to '1' enables the V2-LS process monitor to propagate from ADOE# to ADPAR_EVEN for process monitor; setting it to '0' disables it.
8	**Enable Fast PCI Master Address Transfer for the Odd V2 Chip:** '0'= disable; '1'= enable.
14:9	Reserved
15	**Enable V2-LS Process Monitor:** Setting this bit to '1' enables the V2-LS process monitor to propagate from ADOE# to ADPAR_ODD; setting it to '0' disables it.

9.4 V2 Miscellaneous Status Register (V2S)

Index: 10AH

Bit	Description	Name	Reset State
0	DRAM Power Plane Voltage (Even)	DRAM_5V_E	PU/PD
1	PCI Power Plane Voltage (Even)	PCI_5V_E	PU/PD
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'
8	DRAM Power Plane Voltage (Odd)	DRAM_5V_O	PU/PD
9	PCI Power Plane Voltage (Odd)	PCI_5V_E	PU/PD
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**DRAM Power Plane Voltage (Even):** '0' = 3.3V; '1' = 5V. The DRAM voltage plane is set by a weak pull-up/pull-down resistor on ADPAR_EVEN. **NOTE:** This bit applies to Revision BB and later silicon.
1	**PCI Power Plane Voltage (Even):** '0' = 3.3V; '1' = 5V. The PCI voltage plane is set by a weak pull-up/pull-down resistor on ADPAR_ODD. **NOTE:** This bit applies to Revision BB and later silicon.
7:2	Reserved
8	**DRAM Power Plane Voltage (Odd):** '0' = 3.3V; '1' = 5V. The DRAM voltage plane is set by a weak pull-up/pull-down resistor on ADPAR_EVEN. **NOTE:** This bit applies to Revision BB and later silicon.
9	**PCI Power Plane Voltage (Odd):** '0' = 3.3V; '1' = 5V. The PCI voltage plane is set by a weak pull-up/pull-down resistor on ADPAR_ODD. **NOTE:** This bit applies to Revision BB and later silicon.
15:10	Reserved

10. V2-LS ELECTRICAL SPECIFICATIONS

10.1 Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 10-1. Maximum Ratings

Condition	Maximum Rating
Ambient temperature	0^o - 70^o C
Storage temperature	-65^o to $+150^o$ C
Supply voltage toground potential	3.135-V to 3.6-V (for 3-V design) 4.5-V to 5.5-V (for 5V design)
Applied output voltage	-0.3 to V_{DD} + 0.3V
Applied input voltage	-0.3 to V_{DD} + 0.3V
Operating power dissipation	1 W

10.2 DC Characteristics 5.0 Volt

Refer to Section 5.2 on page 1-225 for 5.0-V DC characteristics.

10.3 DC Characteristics 3.3 Volt

Refer to Section 5.3 on page 1-226 for 3.3-V DC characteristics.

10.4 AC Characteristics

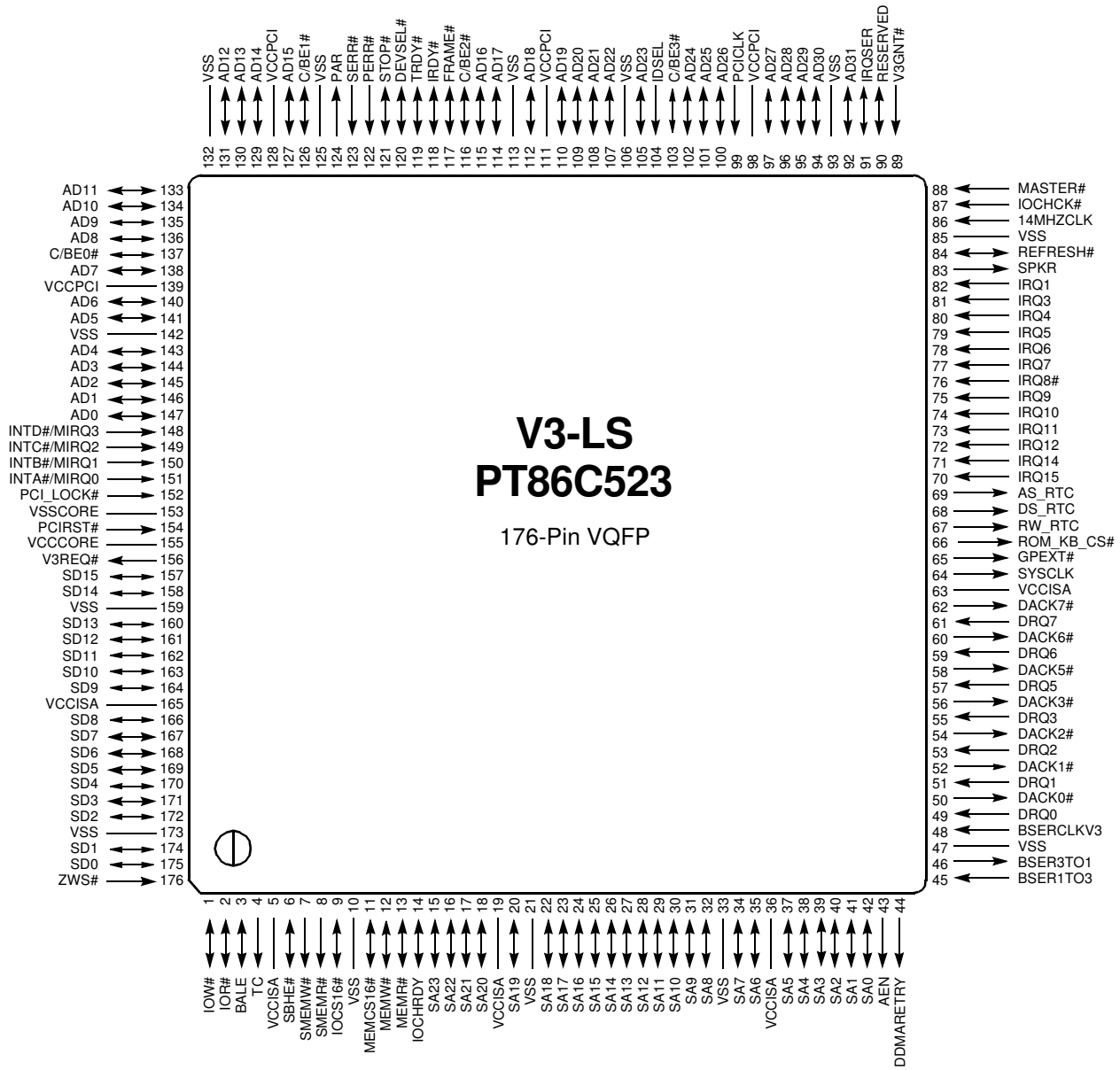
Refer to Section 5.4 on page 1-227 for AC characteristics.

V3-LS PT86C523
Data Book

V3-LS PT86C523

11. V3-LS PIN INFORMATION

11.1 176-Pin VQFP Pin Diagram



11.2 Pin Cross Reference by Pin Number (176-Pin VQFP)

Table 11-1. 176-Pin VQFP Pin Assignment Table (Arranged by Pin Number)

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
1	IOW#	I/O	T	3.3-V/5-V	VCCISA	ISA
2	IOR#	I/O	T	3.3-V/5-V	VCCISA	ISA
3	BALE	I/O	T	3.3-V/5-V	VCCISA	ISA
4	TC	O		3.3-V/5-V	VCCISA	ISA
5	VCCISA	PWR		3.3-V/5-V	VCCISA	POWER
6	SBHE#	I/O	T	3.3-V/5-V	VCCISA	ISA
7	SMEMW#	O		3.3-V/5-V	VCCISA	ISA
8	SMEMR#	O		3.3-V/5-V	VCCISA	ISA
9	IOCS16#	I/O	T	3.3-V/5-V	VCCISA	ISA
10	VSS	GND			VSSIO	GROUND
11	MEMCS16#	I/O	T	3.3-V/5-V	VCCISA	ISA
12	MEMW#	I/O	T	3.3-V/5-V	VCCISA	ISA
13	MEMR#	I/O	T	3.3-V/5-V	VCCISA	ISA
14	IOCHRDY	I/O	T	3.3-V/5-V	VCCISA	ISA
15	SA23	I/O	T	3.3-V/5-V	VCCISA	ISA
16	SA22	I/O	T	3.3-V/5-V	VCCISA	ISA
17	SA21	I/O	T	3.3-V/5-V	VCCISA	ISA
18	SA20	I/O	T	3.3-V/5-V	VCCISA	ISA
19	VCCISA	PWR		3.3-V/5-V	VCCISA	POWER
20	SA19	I/O	T	3.3-V/5-V	VCCISA	ISA
21	VSS	GND			VSSIO	GROUND
22	SA18	I/O	T	3.3-V/5-V	VCCISA	ISA
23	SA17	I/O	T	3.3-V/5-V	VCCISA	ISA
24	SA16	I/O	T	3.3-V/5-V	VCCISA	ISA
25	SA15	I/O	T	3.3-V/5-V	VCCISA	ISA
26	SA14	I/O	T	3.3-V/5-V	VCCISA	ISA
27	SA13	I/O	T	3.3-V/5-V	VCCISA	ISA
28	SA12	I/O	T	3.3-V/5-V	VCCISA	ISA
29	SA11	I/O	T	3.3-V/5-V	VCCISA	ISA

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 11-1. 176-Pin VQFP Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
30	SA10	I/O	T	3.3-V/5-V	VCCISA	ISA
31	SA9	I/O	T	3.3-V/5-V	VCCISA	ISA
32	SA8	I/O	T	3.3-V/5-V	VCCISA	ISA
33	VSS	GND			VSSIO	GROUND
34	SA7	I/O	T	3.3-V/5-V	VCCISA	ISA
35	SA6	I/O	T	3.3-V/5-V	VCCISA	ISA
36	VCCISA	PWR		3.3-V/5-V	VCCISA	POWER
37	SA5	I/O	T	3.3-V/5-V	VCCISA	ISA
38	SA4	I/O	T	3.3-V/5-V	VCCISA	ISA
39	SA3	I/O	T	3.3-V/5-V	VCCISA	ISA
40	SA2	I/O	T	3.3-V/5-V	VCCISA	ISA
41	SA1	I/O	T	3.3-V/5-V	VCCISA	ISA
42	SA0	I/O	T	3.3-V/5-V	VCCISA	ISA
43	AEN	O		3.3-V/5-V	VCCISA	ISA
44	DDMARETRY	O		3.3-V/5-V	VCCISA	ISA
45	BSER1TO3	I	T	3.3-V/5-V	VCCISA	ISA
46	BSER3TO1	O		3.3-V/5-V	VCCISA	ISA
47	VSS	GND			VSSIO	GROUND
48	BSERCLKV3	I	T	3.3-V/5-V	VCCISA	ISA
49	DRQ0	I	T	3.3-V/5-V	VCCISA	ISA
50	DACK0#	O		3.3-V/5-V	VCCISA	ISA
51	DRQ1	I	T	3.3-V/5-V	VCCISA	ISA
52	DACK1#	O		3.3-V/5-V	VCCISA	ISA
53	DRQ2	I	T	3.3-V/5-V	VCCISA	ISA
54	DACK2#	O		3.3-V/5-V	VCCISA	ISA
55	DRQ3	I	T	3.3-V/5-V	VCCISA	ISA
56	DACK3#	O		3.3-V/5-V	VCCISA	ISA
57	DRQ5	I	T	3.3-V/5-V	VCCISA	ISA
58	DACK5#	O		3.3-V/5-V	VCCISA	ISA
59	DRQ6	I	T	3.3-V/5-V	VCCISA	ISA

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 11-1. 176-Pin VQFP Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
60	DACK6#	O		3.3-V/5-V	VCCISA	ISA
61	DRQ7	I	T	3.3-V/5-V	VCCISA	ISA
62	DACK7#	O		3.3-V/5-V	VCCISA	ISA
63	VCCISA	PWR		3.3-V/5-V	VCCISA	POWER
64	SYSCLK	O		3.3-V/5-V	VCCISA	ISA
65	GPEXT#	O		3.3-V/5-V	VCCISA	ISA
66	ROM_KB_CS#	O		3.3-V/5-V	VCCISA	ISA
67	RW_RTC	O		3.3-V/5-V	VCCISA	ISA
68	DS_RTC	O		3.3-V/5-V	VCCISA	ISA
69	AS_RTC	O		3.3-V/5-V	VCCISA	ISA
70	IRQ15	I	S	3.3-V/5-V	VCCISA	ISA
71	IRQ14	I	S	3.3-V/5-V	VCCISA	ISA
72	IRQ12	I	S	3.3-V/5-V	VCCISA	ISA
73	IRQ11	I	S	3.3-V/5-V	VCCISA	ISA
74	IRQ10	I	S	3.3-V/5-V	VCCISA	ISA
75	IRQ9	I	S	3.3-V/5-V	VCCISA	ISA
76	IRQ8#	I	S	3.3-V/5-V	VCCISA	ISA
77	IRQ7	I	S	3.3-V/5-V	VCCISA	ISA
78	IRQ6	I	S	3.3-V/5-V	VCCISA	ISA
79	IRQ5	I	S	3.3-V/5-V	VCCISA	ISA
80	IRQ4	I	S	3.3-V/5-V	VCCISA	ISA
81	IRQ3	I	S	3.3-V/5-V	VCCISA	ISA
82	IRQ1	I	S	3.3-V/5-V	VCCISA	ISA
83	SPKR	O		3.3-V/5-V	VCCISA	ISA
84	REFRESH#	I/O	T	3.3-V/5-V	VCCISA	ISA
85	VSS	GND			VSSIO	GROUND
86	14MHZCLK	I	T	3.3-V/5-V	VCCISA	ISA
87	IOCHCK#	I	S	3.3-V/5-V	VCCISA	ISA
88	MASTER#	I	T	3.3-V/5-V	VCCISA	ISA
89	V3GNT#	I	T	3/3-V/5-V	VCCPCI	PCI

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 11-1. 176-Pin VQFP Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
90	RESERVED	I/O	T	3.3-V/5-V	VCCPCI	PCI
91	IRQSER	I/O	T	3.3-V/5-V	VCCPCI	PCI
92	AD31	I/O	T	3.3-V/5-V	VCCPCI	PCI
93	VSS	GND			VSSIO	GROUND
94	AD30	I/O	T	3.3-V/5-V	VCCPCI	PCI
95	AD29	I/O	T	3.3-V/5-V	VCCPCI	PCI
96	AD28	I/O	T	3.3-V/5-V	VCCPCI	PCI
97	AD27	I/O	T	3.3-V/5-V	VCCPCI	PCI
98	VCCPCI	PWR		3.3-V/5-V	VCCPCI	POWER
99	PCICLK	I	T	3.3-V/5-V	VCCPCI	PCI
100	AD26	I/O	T	3.3-V/5-V	VCCPCI	PCI
101	AD25	I/O	T	3.3-V/5-V	VCCPCI	PCI
102	AD24	I/O	T	3.3-V/5-V	VCCPCI	PCI
103	C/BE3#	I/O	T	3.3-V/5-V	VCCPCI	PCI
104	IDSEL	I	T	3.3-V/5-V	VCCPCI	PCI
105	AD23	I/O	T	3.3-V/5-V	VCCPCI	PCI
106	VSS	GND			VSSIO	GROUND
107	AD22	I/O	T	3.3-V/5-V	VCCPCI	PCI
108	AD21	I/O	T	3.3-V/5-V	VCCPCI	PCI
109	AD20	I/O	T	3.3-V/5-V	VCCPCI	PCI
110	AD19	I/O	T	3.3-V/5-V	VCCPCI	PCI
111	VCCPCI	PWR		3.3-V/5-V	VCCPCI	POWER
112	AD18	I/O	T	3.3-V/5-V	VCCPCI	PCI
113	VSS	GND			VSSIO	GROUND
114	AD17	I/O	T	3.3-V/5-V	VCCPCI	PCI
115	AD16	I/O	T	3.3-V/5-V	VCCPCI	PCI
116	C/BE2#	I/O	T	3.3-V/5-V	VCCPCI	PCI
117	FRAME#	I/O	T	3.3-V/5-V	VCCPCI	PCI
118	IRDY#	I/O	T	3.3-V/5-V	VCCPCI	PCI
119	TRDY#	I/O	T	3.3-V/5-V	VCCPCI	PCI

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 11-1. 176-Pin VQFP Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
120	DEVSEL#	I/O	T	3.3-V/5-V	VCCPCI	PCI
121	STOP#	I/O	T	3.3-V/5-V	VCCPCI	PCI
122	PERR#	I	T	3.3-V/5-V	VCCPCI	PCI
123	SERR#	I	T	3.3-V/5-V	VCCPCI	PCI
124	PAR	O		3.3-V/5-V	VCCPCI	PCI
125	VSS	GND			VSSIO	GROUND
126	C/BE1#	I/O	T	3.3-V/5-V	VCCPCI	PCI
127	AD15	I/O	T	3.3-V/5-V	VCCPCI	PCI
128	VCCPCI	PWR		3.3-V/5-V	VCCPCI	POWER
129	AD14	I/O	T	3.3-V/5-V	VCCPCI	PCI
130	AD13	I/O	T	3.3-V/5-V	VCCPCI	PCI
131	AD12	I/O	T	3.3-V/5-V	VCCPCI	PCI
132	VSS	GND			VSSIO	GROUND
133	AD11	I/O	T	3.3-V/5-V	VCCPCI	PCI
134	AD10	I/O	T	3.3-V/5-V	VCCPCI	PCI
135	AD9	I/O	T	3.3-V/5-V	VCCPCI	PCI
136	AD8	I/O	T	3.3-V/5-V	VCCPCI	PCI
137	C/BE0#	I/O	T	3.3-V/5-V	VCCPCI	PCI
138	AD7	I/O	T	3.3-V/5-V	VCCPCI	PCI
139	VCCPCI	PWR		3.3-V/5-V	VCCPCI	POWER
140	AD6	I/O	T	3.3-V/5-V	VCCPCI	PCI
141	AD5	I/O	T	3.3-V/5-V	VCCPCI	PCI
142	VSS	GND			VSSIO	GROUND
143	AD4	I/O	T	3.3-V/5-V	VCCPCI	PCI
144	AD3	I/O	T	3.3-V/5-V	VCCPCI	PCI
145	AD2	I/O	T	3.3-V/5-V	VCCPCI	PCI
146	AD1	I/O	T	3.3-V/5-V	VCCPCI	PCI
147	AD0	I/O	T	3.3-V/5-V	VCCPCI	PCI
148	INTD#/MIRQ3	I	T	3.3-V/5-V	VCCPCI	PCI
149	INTC#/MIRQ2	I	T	3.3-V/5-V	VCCPCI	PCI

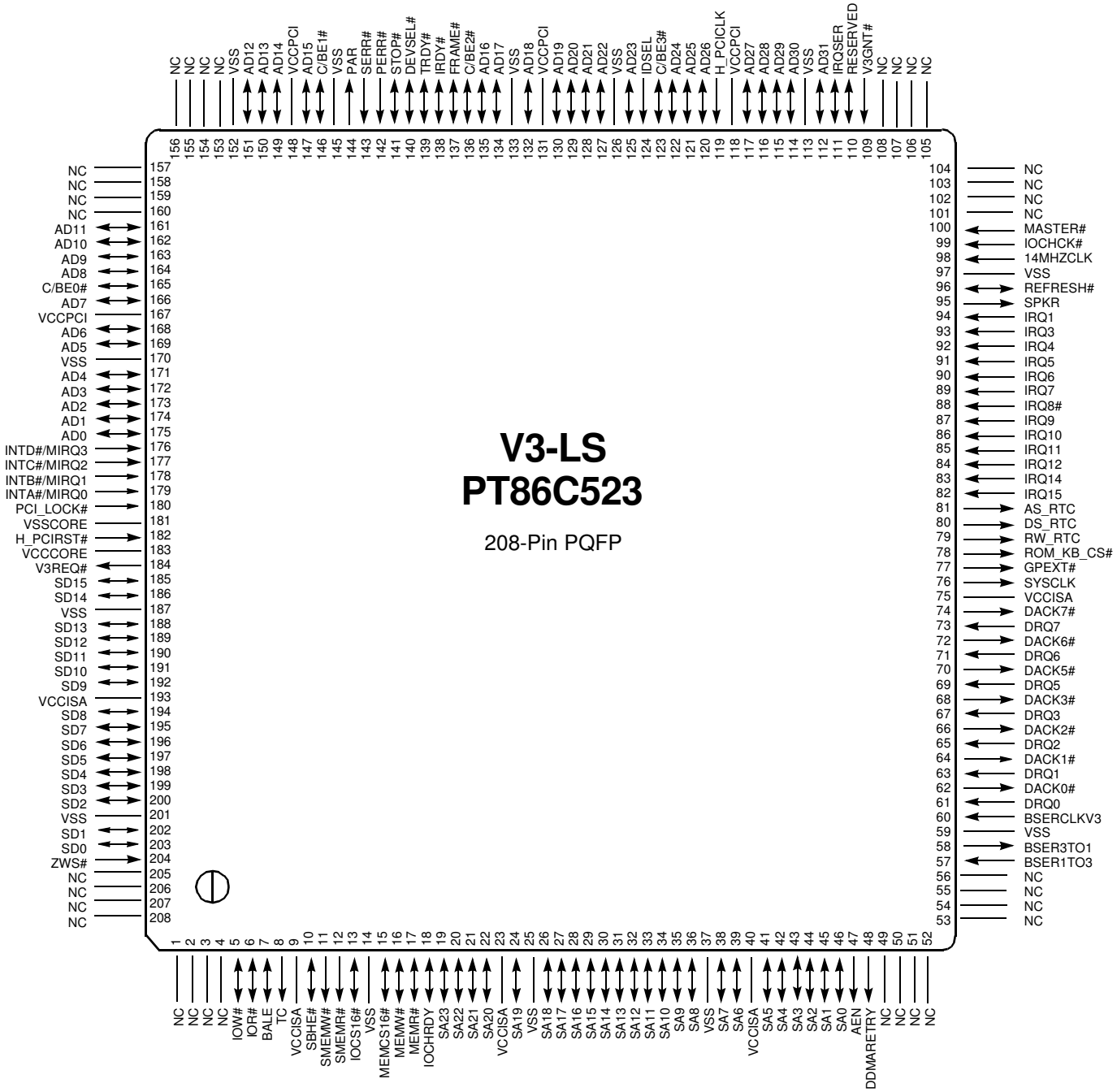
I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 11-1. 176-Pin VQFP Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
150	INTB#/MIRQ1	I	T	3.3-V/5-V	VCCPCI	PCI
151	INTA#/MIRQ0	I	T	3.3-V/5-V	VCCPCI	PCI
152	PCI_LOCK#	I	T	3.3-V/5-V	VCCPCI	PCI
153	VSSCORE	GND			VSSCORE	GROUND
154	PCIRST#	I	S	3.3-V/5-V	VCCPCI	PCI
155	VCCCORE	PWR		3.3-V/5-V	VCCCORE	POWER
156	V3REQ#	O		3.3-V	VCCPCI	PCI
157	SD15	I/O	T	3.3-V/5-V	VCCISA	ISA
158	SD14	I/O	T	3.3-V/5-V	VCCISA	ISA
159	VSS	GND			VSSIO	GROUND
160	SD13	I/O	T	3.3-V/5-V	VCCISA	ISA
161	SD12	I/O	T	3.3-V/5-V	VCCISA	ISA
162	SD11	I/O	T	3.3-V/5-V	VCCISA	ISA
163	SD10	I/O	T	3.3-V/5-V	VCCISA	ISA
164	SD9	I/O	T	3.3-V/5-V	VCCISA	ISA
165	VCCISA	PWR		3.3-V/5-V	VCCISA	POWER
166	SD8	I/O	T	3.3-V/5-V	VCCISA	ISA
167	SD7	I/O	T	3.3-V/5-V	VCCISA	ISA
168	SD6	I/O	T	3.3-V/5-V	VCCISA	ISA
169	SD5	I/O	T	3.3-V/5-V	VCCISA	ISA
170	SD4	I/O	T	3.3-V/5-V	VCCISA	ISA
171	SD3	I/O	T	3.3-V/5-V	VCCISA	ISA
172	SD2	I/O	T	3.3-V/5-V	VCCISA	ISA
173	VSS	GND			VSSIO	GROUND
174	SD1	I/O	T	3.3-V/5-V	VCCISA	ISA
175	SD0	I/O	T	3.3-V/5-V	VCCISA	ISA
176	ZWS#	I	T	3.3-V/5-V	VCCISA	ISA

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

11.3 208-Pin PQFP Pin Diagram



11.4 Pin Cross Reference by Pin Number (208-Pin PQFP)

Table 11-2. 208-Pin PQFP Pin Assignment Table (Arranged by Pin Number)

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
1	NC			3.3-V/5-V		
2	NC			3.3-V/5-V		
3	NC			3.3-V/5-V		
4	NC			3.3-V/5-V		
5	IOW#	I/O	T	3.3-V/5-V	VCCISA	ISA
6	IOR#	I/O	T	3.3-V/5-V	VCCISA	ISA
7	BALE	I/O	T	3.3-V/5-V	VCCISA	ISA
8	TC	O		3.3-V/5-V	VCCISA	ISA
9	VCCISA	PWR		3.3-V/5-V	VCCISA	POWER
10	SBHE#	I/O	T	3.3-V/5-V	VCCISA	ISA
11	SMEMW#	O		3.3-V/5-V	VCCISA	ISA
12	SMEMR#	O		3.3-V/5-V	VCCISA	ISA
13	IOCS16#	I/O	T	3.3-V/5-V	VCCISA	ISA
14	VSS	GND			VSSIO	GROUND
15	MEMCS16#	I/O	T	3.3-V/5-V	VCCISA	ISA
16	MEMW#	I/O	T	3.3-V/5-V	VCCISA	ISA
17	MEMR#	I/O	T	3.3-V/5-V	VCCISA	ISA
18	IOCHRDY	I/O	T	3.3-V/5-V	VCCISA	ISA
19	SA23	I/O	T	3.3-V/5-V	VCCISA	ISA
20	SA22	I/O	T	3.3-V/5-V	VCCISA	ISA
21	SA21	I/O	T	3.3-V/5-V	VCCISA	ISA
22	SA20	I/O	T	3.3-V/5-V	VCCISA	ISA
23	VCCISA	PWR		3.3-V/5-V	VCCISA	POWER
24	SA19	I/O	T	3.3-V/5-V	VCCISA	ISA
25	VSS	GND			VSSIO	GROUND
26	SA18	I/O	T	3.3-V/5-V	VCCISA	ISA
27	SA17	I/O	T	3.3-V/5-V	VCCISA	ISA
28	SA16	I/O	T	3.3-V/5-V	VCCISA	ISA
29	SA15	I/O	T	3.3-V/5-V	VCCISA	ISA

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 11-2. 208-Pin PQFP Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
30	SA14	I/O	T	3.3-V/5-V	VCCISA	ISA
31	SA13	I/O	T	3.3-V/5-V	VCCISA	ISA
32	SA12	I/O	T	3.3-V/5-V	VCCISA	ISA
33	SA11	I/O	T	3.3-V/5-V	VCCISA	ISA
34	SA10	I/O	T	3.3-V/5-V	VCCISA	ISA
35	SA9	I/O	T	3.3-V/5-V	VCCISA	ISA
36	SA8	I/O	T	3.3-V/5-V	VCCISA	ISA
37	VSS	GND			VSSIO	GROUND
38	SA7	I/O	T	3.3-V/5-V	VCCISA	ISA
39	SA6	I/O	T	3.3-V/5-V	VCCISA	ISA
40	VCCISA	PWR		3.3-V/5-V	VCCISA	POWER
41	SA5	I/O	T	3.3-V/5-V	VCCISA	ISA
42	SA4	I/O	T	3.3-V/5-V	VCCISA	ISA
43	SA3	I/O	T	3.3-V/5-V	VCCISA	ISA
44	SA2	I/O	T	3.3-V/5-V	VCCISA	ISA
45	SA1	I/O	T	3.3-V/5-V	VCCISA	ISA
46	SA0	I/O	T	3.3-V/5-V	VCCISA	ISA
47	AEN	O		3.3-V/5-V	VCCISA	ISA
48	DDMARETRY	O		3.3-V/5-V	VCCISA	ISA
49	NC			3.3-V/5-V		
50	NC			3.3-V/5-V		
51	NC			3.3-V/5-V		
52	NC			3.3-V/5-V		
53	NC			3.3-V/5-V		
54	NC			3.3-V/5-V		
55	NC			3.3-V/5-V		
56	NC			3.3-V/5-V		
57	BSER1TO3	I	T	3.3-V/5-V	VCCISA	ISA
58	BSER3TO1	O		3.3-V/5-V	VCCISA	ISA
59	VSS	GND			VSSIO	GROUND

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 11-2. 208-Pin PQFP Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
60	BSERCLKV3	I	T	3.3-V/5-V	VCCISA	ISA
61	DRQ0	I	T	3.3-V/5-V	VCCISA	ISA
62	DACK0#	O		3.3-V/5-V	VCCISA	ISA
63	DRQ1	I	T	3.3-V/5-V	VCCISA	ISA
64	DACK1#	O		3.3-V/5-V	VCCISA	ISA
65	DRQ2	I	T	3.3-V/5-V	VCCISA	ISA
66	DACK2#	O		3.3-V/5-V	VCCISA	ISA
67	DRQ3	I	T	3.3-V/5-V	VCCISA	ISA
68	DACK3#	O		3.3-V/5-V	VCCISA	ISA
69	DRQ5	I	T	3.3-V/5-V	VCCISA	ISA
70	DACK5#	O		3.3-V/5-V	VCCISA	ISA
71	DRQ6	I	T	3.3-V/5-V	VCCISA	ISA
72	DACK6#	O		3.3-V/5-V	VCCISA	ISA
73	DRQ7	I	T	3.3-V/5-V	VCCISA	ISA
74	DACK7#	O		3.3-V/5-V	VCCISA	ISA
75	VCCISA	PWR		3.3-V/5-V	VCCISA	POWER
76	SYSCLK	O		3.3-V/5-V	VCCISA	ISA
77	GPEXT#	O		3.3-V/5-V	VCCISA	ISA
78	ROM_KB_CS#	O		3.3-V/5-V	VCCISA	ISA
79	RW_RTC	O		3.3-V/5-V	VCCISA	ISA
80	DS_RTC	O		3.3-V/5-V	VCCISA	ISA
81	AS_RTC	O		3.3-V/5-V	VCCISA	ISA
82	IRQ15	I	S	3.3-V/5-V	VCCISA	ISA
83	IRQ14	I	S	3.3-V/5-V	VCCISA	ISA
84	IRQ12	I	S	3.3-V/5-V	VCCISA	ISA
85	IRQ11	I	S	3.3-V/5-V	VCCISA	ISA
86	IRQ10	I	S	3.3-V/5-V	VCCISA	ISA
87	IRQ9	I	S	3.3-V/5-V	VCCISA	ISA
88	IRQ8#	I	S	3.3-V/5-V	VCCISA	ISA
89	IRQ7	I	S	3.3-V/5-V	VCCISA	ISA

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 11-2. 208-Pin PQFP Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
90	IRQ6	I	S	3.3-V/5-V	VCCISA	ISA
91	IRQ5	I	S	3.3-V/5-V	VCCISA	ISA
92	IRQ4	I	S	3.3-V/5-V	VCCISA	ISA
93	IRQ3	I	S	3.3-V/5-V	VCCISA	ISA
94	IRQ1	I	S	3.3-V/5-V	VCCISA	ISA
95	SPKR	O		3.3-V/5-V	VCCISA	ISA
96	REFRESH#	I/O	T	3.3-V/5-V	VCCISA	ISA
97	VSS	GND			VSSIO	GROUND
98	14MHZCLK	I	T	3.3-V/5-V	VCCISA	ISA
99	IOCHCK#	I	S	3.3-V/5-V	VCCISA	ISA
100	MASTER#	I	T	3.3-V/5-V	VCCISA	ISA
101	NC			3.3-V		
102	NC			3.3-V		
103	NC			3.3-V		
104	NC			3.3-V		
105	NC			3.3-V		
106	NC			3.3-V		
107	NC			3.3-V		
108	NC			3.3-V		
109	V3GNT#	I/O	T	3.3-V/5-V	VCCPCI	PCI
110	RESERVED	I/O	T	3.3-V/5-V	VCCPCI	PCI
111	IRQSER	I/O	T	3.3-V/5-V	VCCPCI	PCI
112	AD31	I/O	T	3.3-V/5-V	VCCPCI	PCI
113	VSS	GND			VSSIO	GROUND
114	AD30	I/O	T	3.3-V/5-V	VCCPCI	PCI
115	AD29	I/O	T	3.3-V/5-V	VCCPCI	PCI
116	AD28	I/O	T	3.3-V/5-V	VCCPCI	PCI
117	AD27	I/O	T	3.3-V/5-V	VCCPCI	PCI
118	VCCPCI	PWR		3.3-V/5-V	VCCPCI	POWER
119	PCICLK	I	T	3.3-V/5-V	VCCPCI	PCI

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 11-2. 208-Pin PQFP Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
120	AD26	I/O	T	3.3-V/5-V	VCCPCI	PCI
121	AD25	I/O	T	3.3-V/5-V	VCCPCI	PCI
122	AD24	I/O	T	3.3-V/5-V	VCCPCI	PCI
123	C/BE3#	I/O	T	3.3-V/5-V	VCCPCI	PCI
124	IDSEL	I	T	3.3-V/5-V	VCCPCI	PCI
125	AD23	I/O	T	3.3-V/5-V	VCCPCI	PCI
126	VSS	GND			VSSIO	GROUND
127	AD22	I/O	T	3.3-V/5-V	VCCPCI	PCI
128	AD21	I/O	T	3.3-V/5-V	VCCPCI	PCI
129	AD20	I/O	T	3.3-V/5-V	VCCPCI	PCI
130	AD19	I/O	T	3.3-V/5-V	VCCPCI	PCI
131	VCCPCI	PWR		3.3-V/5-V	VCCPCI	POWER
132	AD18	I/O	T	3.3-V/5-V	VCCPCI	PCI
133	VSS	GND			VSSIO	GROUND
134	AD17	I/O	T	3.3-V/5-V	VCCPCI	PCI
135	AD16	I/O	T	3.3-V/5-V	VCCPCI	PCI
136	C/BE2#	I/O	T	3.3-V/5-V	VCCPCI	PCI
137	FRAME#	I/O	T	3.3-V/5-V	VCCPCI	PCI
138	IRDY#	I/O	T	3.3-V/5-V	VCCPCI	PCI
139	TRDY#	I/O	T	3.3-V/5-V	VCCPCI	PCI
140	DEVSEL#	I/O	T	3.3-V/5-V	VCCPCI	PCI
141	STOP#	I/O	T	3.3-V/5-V	VCCPCI	PCI
142	PERR#	I	T	3.3-V/5-V	VCCPCI	PCI
143	SERR#	I	T	3.3-V/5-V	VCCPCI	PCI
144	PAR	O		3.3-V/5-V	VCCPCI	PCI
145	VSS	GND			VSSIO	GROUND
146	C/BE1#	I/O	T	3.3-V/5-V	VCCPCI	PCI
147	AD15	I/O	T	3.3-V/5-V	VCCPCI	PCI
148	VCCPCI	PWR		3.3-V/5-V	VCCPCI	POWER
149	AD14	I/O	T	3.3-V/5-V	VCCPCI	PCI

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 11-2. 208-Pin PQFP Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
150	AD13	I/O	T	3.3-V/5-V	VCCPCI	PCI
151	AD12	I/O	T	3.3-V/5-V	VCCPCI	PCI
152	VSS	GND			VSSIO	GROUND
153	NC			3.3-V/5-V		
154	NC			3.3-V/5-V		
155	NC			3.3-V/5-V		
156	NC			3.3-V/5-V		
157	NC			3.3-V/5-V		
158	NC			3.3-V/5-V		
159	NC			3.3-V/5-V		
160	NC			3.3-V/5-V		
161	AD11	I/O	T	3.3-V/5-V	VCCPCI	PCI
162	AD10	I/O	T	3.3-V/5-V	VCCPCI	PCI
163	AD9	I/O	T	3.3-V/5-V	VCCPCI	PCI
164	AD8	I/O	T	3.3-V/5-V	VCCPCI	PCI
165	C/BE0#	I/O	T	3.3-V/5-V	VCCPCI	PCI
166	AD7	I/O	T	3.3-V/5-V	VCCPCI	PCI
167	VCCPCI	PWR		3.3-V/5-V	VCCPCI	POWER
168	AD6	I/O	T	3.3-V/5-V	VCCPCI	PCI
169	AD5	I/O	T	3.3-V/5-V	VCCPCI	PCI
170	VSS	GND			VSSIO	GROUND
171	AD4	I/O	T	3.3-V/5-V	VCCPCI	PCI
172	AD3	I/O	T	3.3-V/5-V	VCCPCI	PCI
173	AD2	I/O	T	3.3-V/5-V	VCCPCI	PCI
174	AD1	I/O	T	3.3-V/5-V	VCCPCI	PCI
175	AD0	I/O	T	3.3-V/5-V	VCCPCI	PCI
176	INTD#/MIRQ3	I	T	3.3-V/5-V	VCCPCI	PCI
177	INTC#/MIRQ2	I	T	3.3-V/5-V	VCCPCI	PCI
178	INTB#/MIRQ1	I	T	3.3-V/5-V	VCCPCI	PCI
179	INTA#/MIRQ0	I	T	3.3-V/5-V	VCCPCI	PCI

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

Table 11-2. 208-Pin PQFP Pin Assignment Table (Arranged by Pin Number) *(cont.)*

PIN NO.	PIN NAME	PIN TYPE	INPUT TYPE	VOLTAGE	POWER PLANE	GROUP
180	PCI_LOCK#	I	T	3.3-V/5-V	VCCPCI	PCI
181	VSSCORE	GND			VSSCORE	GROUND
182	PCIRST#	I	S	3.3-V/5-V	VCCPCI	PCI
183	VCCCORE	PWR		3.3-V	VCCCORE	POWER
184	V3REQ#	O		3.3-V/5-V	VCCPCI	PCI
185	SD15	I/O	T	3.3-V/5-V	VCCISA	ISA
186	SD14	I/O	T	3.3-V/5-V	VCCISA	ISA
187	VSS	GND			VSSIO	GROUND
188	SD13	I/O	T	3.3-V/5-V	VCCISA	ISA
189	SD12	I/O	T	3.3-V/5-V	VCCISA	ISA
190	SD11	I/O	T	3.3-V/5-V	VCCISA	ISA
191	SD10	I/O	T	3.3-V/5-V	VCCISA	ISA
192	SD9	I/O	T	3.3-V/5-V	VCCISA	ISA
193	VCCISA	PWR		3.3-V/5-V	VCCISA	POWER
194	SD8	I/O	T	3.3-V/5-V	VCCISA	ISA
194	SD7	I/O	T	3.3-V/5-V	VCCISA	ISA
196	SD6	I/O	T	3.3-V/5-V	VCCISA	ISA
197	SD5	I/O	T	3.3-V/5-V	VCCISA	ISA
198	SD4	I/O	T	3.3-V/5-V	VCCISA	ISA
199	SD3	I/O	T	3.3-V/5-V	VCCISA	ISA
200	SD2	I/O	T	3.3-V/5-V	VCCISA	ISA
201	VSS	GND			VSSIO	GROUND
202	SD1	I/O	T	3.3-V/5-V	VCCISA	ISA
203	SD0	I/O	T	3.3-V/5-V	VCCISA	ISA
204	ZWS#	I	T	3.3-V/5-V	VCCISA	ISA
205	NC			3.3-V/5-V		
206	NC			3.3-V/5-V		
207	NC			3.3-V/5-V		
208	NC			3.3-V/5-V		

I = Input-only; **O** = Output-only; **C** = CMOS-compatible; **S** = Schmitt-trigger; **T** = TTL-compatible input; **PWR** = Power; **GND** = Ground

11.5 Pin Cross Reference by Pin Name

Table 11-3. Pin Assignment Table (Arranged by Pin Name)

PIN NAME	PIN NO. (176-PIN)	PIN NO. (208-PIN)	PIN NAME	PIN NO. (176-PIN)	PIN NO. (208-PIN)
14MHZCLK	86	98	AD28	96	116
AD0	147	175	AD29	95	115
AD1	146	174	AD30	94	114
AD2	145	173	AD31	92	112
AD3	144	172	AEN	43	47
AD4	143	171	AS_RTC	69	81
AD5	141	169	BALE	3	7
AD6	140	168	BSERCLKV3	48	60
AD7	138	166	BSER1TO3	45	57
AD8	136	164	BSER3TO1	46	58
AD9	135	163	C/BE0#	137	165
AD10	134	162	C/BE1#	126	146
AD11	133	161	C/BE2#	116	136
AD12	131	151	C/BE3#	103	123
AD13	130	150	DACK0#	50	62
AD14	129	149	DACK1#	52	64
AD15	127	147	DACK2#	54	66
AD16	115	135	DACK3#	56	68
AD17	114	134	DACK5#	58	70
AD18	112	132	DACK6#	60	72
AD19	110	130	DACK7#	62	74
AD20	109	129	DDMARETRY	44	48
AD21	108	128	DEVSEL#	120	140
AD22	107	127	DRQ0	49	61
AD23	105	125	DRQ1	51	63
AD24	102	122	DRQ2	53	65
AD25	101	121	DRQ3	55	67
AD26	100	120	DRQ5	57	69
AD27	97	117	DRQ6	59	71

Table 11-3. Pin Assignment Table (Arranged by Pin Name) *(cont.)*

PIN NAME	PIN NO. (176-PIN)	PIN NO. (208-PIN)	PIN NAME	PIN NO. (176-PIN)	PIN NO. (208-PIN)
DRQ7	61	73	IRQSER	91	111
DS_RTC	68	80	MASTER#	88	100
FRAME#	117	137	MEMCS16#	11	15
GPEXT#	65	77	MEMR#	13	17
PCICLK	99	119	MEMW#	12	16
PCIRST#	154	182	NC		1
IDSEL	104	124	NC		2
INTA#/MIRQ0	151	179	NC		3
INTB#/MIRQ1	150	178	NC		4
INTC#/MIRQ2	149	177	NC		49
INTD#/MIRQ3	148	176	NC		50
IOCHCK#	87	99	NC		51
IOCHRDY	14	18	NC		52
IOCS16#	9	13	NC		53
IOR#	2	6	NC		54
IOW#	1	5	NC		55
IRDY#	118	138	NC		56
IRQ1	82	94	NC		101
IRQ3	81	93	NC		102
IRQ4	80	92	NC		103
IRQ5	79	91	NC		104
IRQ6	78	90	NC		105
IRQ7	77	89	NC		106
IRQ8#	76	88	NC		107
IRQ9	75	87	NC		108
IRQ10	74	86	NC		153
IRQ11	73	85	NC		154
IRQ12	72	84	NC		155
IRQ14	71	83	NC		156
IRQ15	70	82	NC		157

Table 11-3. Pin Assignment Table (Arranged by Pin Name) *(cont.)*

PIN NAME	PIN NO. (176-PIN)	PIN NO. (208-PIN)	PIN NAME	PIN NO. (176-PIN)	PIN NO. (208-PIN)
NC		158	SA16	24	28
NC		159	SA17	23	27
NC		160	SA18	22	26
NC		205	SA19	20	24
NC		206	SA20	18	22
NC		207	SA21	17	21
NC		208	SA22	16	20
PAR	124	144	SA23	15	19
PCI_LOCK#	152	180	SBHE#	6	10
PERR#	122	142	SD0	175	203
REFRESH#	84	96	SD1	174	202
RESERVED	90	110	SD2	172	200
ROM_KB_CS#	66	78	SD3	171	199
RW_RTC	67	79	SD4	170	198
SA0	42	46	SD5	169	197
SA1	41	45	SD6	168	196
SA2	40	44	SD7	167	195
SA3	39	43	SD8	166	194
SA4	38	42	SD9	164	192
SA5	37	41	SD10	163	191
SA6	35	39	SD11	162	190
SA7	34	38	SD12	161	189
SA8	32	36	SD13	160	188
SA9	31	35	SD14	158	186
SA10	30	34	SD15	157	185
SA11	29	33	SERR#	123	143
SA12	28	32	SMEMR#	8	12
SA13	27	31	SMEMW#	7	11
SA14	26	30	SPKR	83	95
SA15	25	29	STOP#	121	141

Table 11-3. Pin Assignment Table (Arranged by Pin Name) *(cont.)*

PIN NAME	PIN NO. (176-PIN)	PIN NO. (208-PIN)	PIN NAME	PIN NO. (176-PIN)	PIN NO. (208-PIN)
SYSCLK	64	76	VSS	10	14
TC	4	8	VSS	21	25
TRDY#	119	139	VSS	33	37
V3GNT#	89	109	VSS	47	59
V3REQ#	156	184	VSS	85	97
VCCCORE	155	183	VSS	93	113
VCCISA	5	9	VSS	106	126
VCCISA	19	23	VSS	113	133
VCCISA	36	40	VSS	125	145
VCCISA	63	75	VSS	132	152
VCCISA	165	193	VSS	142	170
VCCPCI	98	118	VSS	159	187
VCCPCI	111	131	VSS	173	201
VCCPCI	128	148	VSSCORE	153	181
VCCPCI	139	167	ZWS#	176	204

12. V3-LS DETAILED PIN DESCRIPTIONS

This chapter contains a detailed functional description of the pins on PT86C523. For ease of reference, the pins have been arranged alphabetically within each of the following functional interface groups:

- ISA Interface (ISA)
- PCI Interface (PCI)
- Power and Ground (POWER/GROUND)

The '#' symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. Signal names without the # symbol indicate that the signal is active, or asserted at the high voltage level.

The '/' symbol between signal names indicates that the signals are multiplexed and use the same pin for all functions.

The following conventions indicate the pin type: 'I' = input-only pins; 'O' = output-only pins; 'I/O' = bidirectional pins; 'PWR' = power pins; and 'GND' = ground pins. The pin type is defined relative to the Vesuvius platform.

For a list of pins arranged by pin number, refer to Table 11-2 on page 294 and Table 11-2 on page 294. For a list of pins arranged by pin name, refer to Table 11-3 on page 301.

12.1 ISA Interface

Pin Name	Type	Description
14MHZCLK	I	**CLOCK:** 14.318 MHz clock for the 8254 timer.
AEN	O	**ADDRESS ENABLE:** If AEN is driven high, it indicates that the DMA controller has taken control of the CPU address bus and the AT bus command lines.
AS_RTC	O	**RTC ADDRESS STROBE:** This output should be connected to the AS_RTC input of an 146818-type or equivalent RTC.
BALE	I/O	**BUFFERED ADDRESS LATCH ENABLE:** This output is driven to the AT bus where it indicates the presence of a valid address on the bus.
BSERCLKV3	I	**BUS SERIAL CLOCK:** Burst bus clock for serial system and power management bus.
BSER1TO3	I	**BUS SERIAL V1 TO V3:** Serialized system and power management information from V1-LS to V3-LS.
BSER3TO1	O	**BUS SERIAL V3 TO V1:** Serialized system and power management information from V3-LS to V1-LS.

12.1 ISA Interface *(cont.)*

Pin Name	Type	Description
DACK[7:5, 3:0]#	O	**DMA ACKNOWLEDGE [7:5, 3:0]#:** DACKn# asserted indicates that the corresponding DMA channel request “n” has been granted.
DDMARETRY	O	**DISTRIBUTED DMA RETRY:** When distributed-DMA is enabled, V3-LS activates this pin to retry V1-LS.
DRQ[7:5, 3:0]	I	**DMA REQUEST [7:5, 3:0]:** DRQn asserted indicates that a DMA device is requesting DMA service using Channel “n”.
DS_RTC	O	**RTC DATA STROBE :** This output should be connected to the DS_RTC input of an 146818-type or equivalent RTC.
GPEXT#	I/O	**GENERAL PURPOSE OUTPUT EXTENSION#:** The GPEXT# is pulsed (low) when register GPEXT_LB is being written. The value being written to GPEXT_LB and the value previously latched in GPEXT_HB will be driven onto SD[7:0] and SD[15:8] respectively to extend by up to 16 general purpose outputs. An external 8-bit or 16-bit flip-flop should be used to latch the SD-bus on the rising (trailing) edge of GPEXT#.
IOCHCK#	I	**I/O CHANNEL CHECK#:** This input indicates a parity error from some device on the AT bus.
IOCHRDY	I/O	**I/O CHANNEL READY:** When this input is driven low, it indicates that the device on the AT bus currently being accessed requires additional time to complete the cycle.
IOCS16#	I/O	I/**O CHIP SELECT 16#:** This input from the AT bus indicates that the current access is to a 16-bit I/O device.
IOR#	I/O	**I/O READ#:** This output to the AT bus indicates an I/O read cycle.
IOW#	I/O	**I/O WRITE#:** This output to the AT bus indicates an I/O write cycle.
IRQ[15,14,12:3,1]	I	**INTERRUPT REQUEST:** ISA bus interrupt requests.
MASTER#	I	**MASTER#:** This input from the AT bus indicates that a slot master has taken control of the AT bus.
MEMCS16#	I/O	**MEMORY CHIP SELECT 16-BIT#:** This input from the AT bus indicates that the current access is to a 16-bit memory device.
MEMR#	I/O	**MEMORY READ#:** This output to the AT bus indicates a Memory Read cycle to any valid AT bus address.
MEMW#	I/O	**MEMORY WRITE#:** This output to the AT bus indicates a Memory Write cycle to any valid AT bus address.

12.1 ISA Interface *(cont.)*

Pin Name	Type	Description
REFRESH#	I/O	**REFRESH#:** This output drives the AT bus to indicate a Memory Refresh cycle.
ROM_KB_CS#	I/O	**BIOS, KEYBOARD, AND CHIP SELECT#:** Combined system BIOS and keyboard chip select output.
RW_RTC	O	**RTC READ/WRITE:** This output should be connected to the RW_RTC input of an 146818-type or equivalent RTC.
SA[23:0]	I/O	**SLOT ADDRESS[23:0]:** These signals are decoded from AD[31:0] and BE[3:0]# of PCI bus. These signals will become inputs during ISA master cycles and outputs during all other cycles.
SBHE#	I/O	**SLOT BYTE HIGH ENABLE#:** This output to the AT bus indicates a data transfer on the high byte of the SD bus.
SD[15:0]	I/O	**SLOT DATA[15:0]** : These I/Os are the data read and write path for the AT bus.
SMEMR#	O	**SLOT MEMORY READ#:** This output to the AT bus indicates that a Memory Read cycle is within the lower 1 Mbyte address range.
SMEMW#	O	**SLOT MEMORY WRITE#:** This output to the AT bus indicates that a Memory Write cycle is within the lower 1 Mbyte address range.
SPKR	O	**SPEAKER:** Speaker data output.
SYSCLK	O	**SYSTEM CLOCK:** AT bus clock. It is derived from BSERCLKV3 and the divisor can be selected by bit [2:0] of Register ATCR-1.
TC	O	**TERMINAL COUNT:** This signal on the ISA bus indicates that a terminal count has reached for a given channel.
ZWS#	I	**ZERO WAIT STATE#:** This input from the AT bus indicates that the device currently being accessed can complete the cycle with a zero wait state.

12.2 PCI Interface

Pin Name	Type	Description
AD[31:0]	I/O	**ADDRESS/DATA MULTIPLEXED [31:0]:** These signals are multiplexed on the same pins. Each transaction is initiated by a 32-bit physical address phase which is followed by one or more data phases. These bus transactions support both read and write bursts.

12.2 PCI Interface *(cont.)*

Pin Name	Type	Description
C/BE[3:0]#	I/O	**COMMAND/BYTE ENABLES [3:0]#:** Both are multiplexed on the same pins. The pins define the Bus Command during the address phase. During the data phase, the pins are used as Byte Enables.
DEVSEL#	I/O	**DEVICE SELECT#:** As an output this signal, DEVSEL# indicates whether Vesuvius is the initiator or target of the current address. As an input, Vesuvius checks whether or not a PCI target exists.
FRAME#	I/O	**CYCLE FRAME#:** This signal is driven by the current initiator and indicates the start and duration of the transaction. FRAME# is deasserted to indicate that the initiator is ready to complete the final data phase. A transaction may consist of one or more data transfers between the current initiator and the currently-addresses target.
IDSEL	I	**ID SELECT:** ID Select for PCI interrupts.
INT[D:A]#/MIRQ[3:0]	I	**INTERRUPTS [D:A]#** / **MAPPABLE INTERRUPTS [3:0]:** These inputs from PCI devices are shareable, level sensitive (active low) interrupt request. They can be Mappable IRQ (MIRQ) ISA signals by changing registers PCI_INTM1 and PCI_INTM2.
IRDY#	I/O	**INITIATOR READY#:** This pin indicates whether or not the bus master is ready to complete the current data phase. During a write, IRDY# shows that valid data is present. During a read, it indicates the bus master's readiness to accept data. IRDY# is used in conjunction with TRDY#.
IRQSER		**SERIAL INTERRUPT** : This pin is reserved for serial interrupt service.
PAR	I/O	**PARITY:** All PCI agents require parity generation.
PCICLK	I	**PCI CLOCK:** 33/25 MHz clock for the PCI bus.
PCIRST#	I	**PCI RESET#:** V3-LS reset input.
PCI_LOCK#	I	**PCI LOCK#:** Used for locking ISA resources.
PERR#	I	**PARITY ERROR#:** This input indicates a data parity error. It may be pulsed active by any agent that detects an parity error condition.
SERR#	I	**SYSTEM ERROR#:** This input may be pulsed active by any agent that selects any system error condition.
V3GNT#	I	**V3 GRANT#:** This pin is used as a SIO grant for the V3-LS device.
V3REQ#	O	**V3 REQUEST#:** This pin is used as a SIO request for V3-LS.

12.2 PCI Interface *(cont.)*

Pin Name	Type	Description
STOP#	I/O	**STOP#:** This allows the master to stop the bus transaction to the current target device.
TRDY#	I/O	**TARGET READY#:** This indicates the ability of the target device to complete the current data phase of the bus transaction. During a read phase, TRDY# indicates that valid data is present. During a write phase, it indicates that the device is ready to accept data.

12.3 Power and Ground

Pin Name	Type	Description
VSS	GND	**VSS:** These are I/O ground pins.
VSSCORE	GND	**VSS CORE:** These are I/O ground pins.
VCCCORE	PWR	**VCC CORE:** These are I/O power pins for VCC CORE power plane.
VCCISA	PWR	**VCC ISA:** These are I/O power pins for VCCISA power plane.
VCCPCI	PWR	**VCC PCI:** These are I/O power pins for VCCPCI power plane.

13. V3-LS FUNCTIONAL DESCRIPTION

This section provides functional information and design guidelines on chip resources and interfaces of the V3-LS, a PCI-to-ISA bridge. To understand its functionality it is important to become familiar with the

13.1 Functional Block Diagram

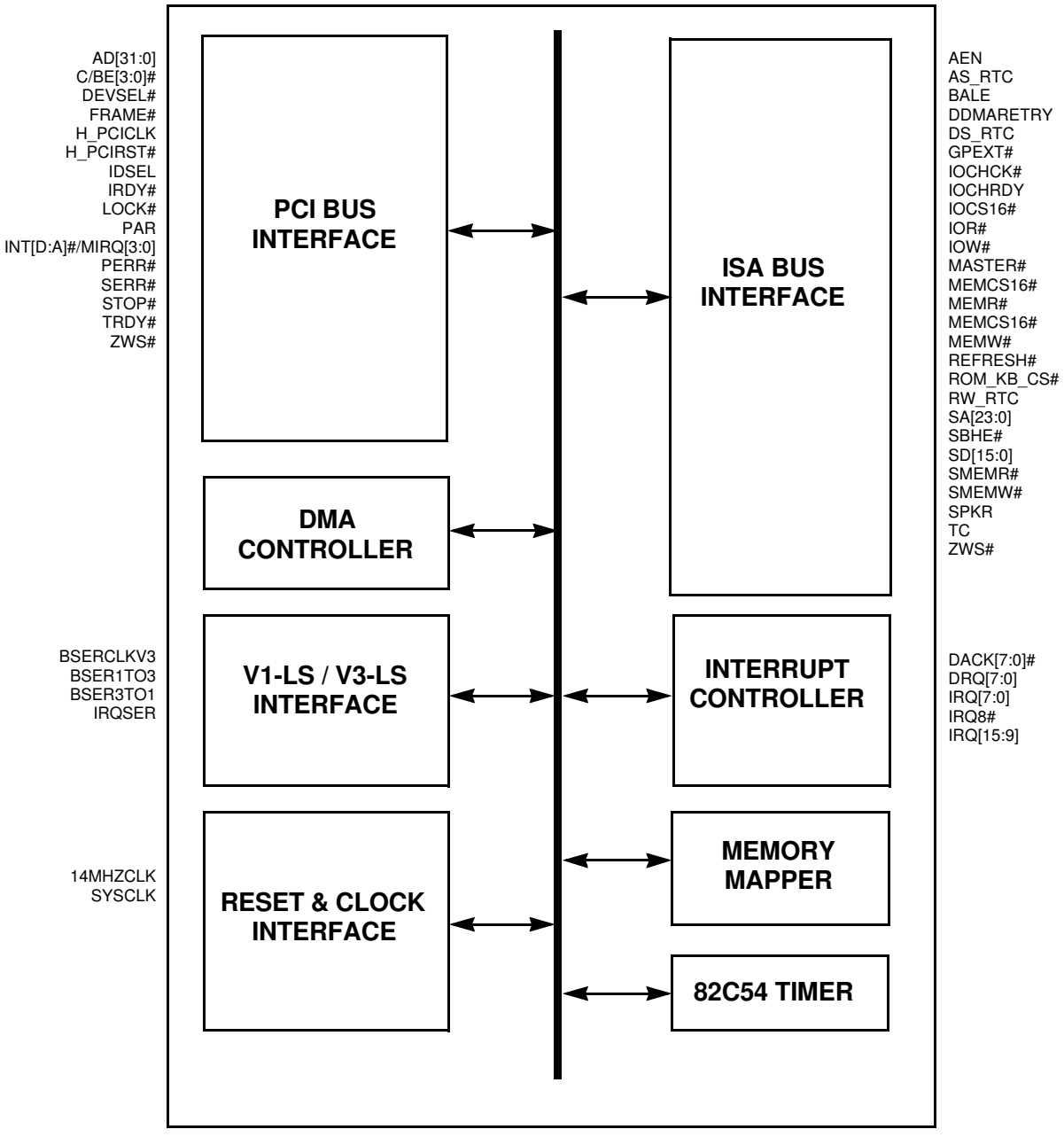


Figure 13-1. V3-LS Functional Block Diagram

programming model of the Vesuvius platform. The BIOS will access V3-LS through an 8-bit access on Port 24h (index port) and Port 26h (data port). Since the V3-LS index registers are only 8-bits wide, the registers are a maximum of 256 bytes (00H - FFH) wide.

13.2 Power Plane Structure

The Vesuvius platform offers a flexible power plane structure to support a wide variety of system configurations. V3-LS has three independent power planes which are divided into three groups: VCCPCI, VCCISA and VCCCORE. VCCPCI and VCCISA voltage planes can be selected to be either 5V or 3.3V. VCCCORE must be connected to 3.3V.

NOTE: All V3-LS power planes should be powered off during 5V Suspend (STR) since the I/O buffers are not leakage controlled.

13.2.1 Power-On Configuration

V3-LS incorporates a power-on configuration register to define several power-on functions, including the master/slave device definition. V3-LS is a master PCI-to-ISA bridge if the DDMARETRY signal is sampled low, or a slave PCI-to-ISA bridge if sampled high during power-on. The power-on register is loaded during PCIRST# using a 100K pull-up or pull-down resistor. The configuration can be viewed in index register 90H, bit 0.

Table 13-1. DDMA Retry Pin Function

Pin Name	176-pin VQFP	208-pin PQFP	Function
DDMARETRY	44	48	Pull-down to select Master PCI-to-ISA Pull-up t o select Slave PCI-to-ISA.
ROMKBCS#	66	78	5-V/3.3-V PCI bus select (SCS[1]) ‘1’ = 5-V; ‘0’ = 3.3-V
GPEXT#	65	77	Class Code/Device Selection (SCS[2]) See Register 02H on page 3-347 and Register 09H on page 3-351
Reserved	90	110	Stored as register bit SCS[3]

13.3 Functional Blocks

The following functional blocks have been integrated into the V3-LS device. Refer to Figure 13-1 on page 310 for a functional block diagram of the V3-LS device. This diagram includes an alphabetical listing of the pins included in each functional group.

13.3.1 Reset and Clock Interface

Refer to Figure 3-4 on page 41 in the V1-LS data book for a distribution of clocks in the VESUVIUS-LS device. As shown in this figure, there are three clock signals coming into the V3-LS: PCICLK, BSERCLKV3, and 14MHZCLK.

Refer to Figure 3-5 on page 42 in the V1-LS data book for a distribution of reset signals in the VESUVIUS-LS. As shown, the PCIRST# signal goes into both the V2-LS and the V3-LS.

13.3.1.1 AT BUS Clock Generation

V3-LS generates the AT Bus Clock by dividing down from the BSERCLKV3 to an approximate 8 MHz frequency. The appropriate divisor for the AT Bus Clock depends on the speed of the BSERCLKV3. The following table defines which divisor should be used for the corresponding CPU bus clock and BSERCLKV3 frequencies to achieve the approximate 8 MHz bus speed. The appropriate divisor must be selected through ATCR1, index register 01H bits [2:0].

Table 13-2. AT Bus Clock Divisors

CPU Bus Clock	BSERCLK	Divide by
50 Mhz	25 MHz	3
60 Mhz	30 MHz	4
66 Mhz	33 MHz	4

13.3.2 The V1-LS to V3-LS Interface

V1-LS and V3-LS devices communicate using two signals: BSER1TO3 and BSER3TO1. The operation of these signals is synchronized to the BSERCLKV3 clock signal.

BSER3TO1 is a serialized signal from V3-LS to V1-LS. It indicates V3 activities such as SMI events, primary activities and secondary activities resulting from interrupt requests (IRQs) or V3-LS ISA requests (REQ#). BSER1TO3 carries information from V1-LS to V3-LS, including the V3-LS grant (GNT#) and interrupt request 13 (IRQ13).

The burst serial interface is defined primarily to pass P/A, S/A, and other power management information between V1 and V3. Embedding the REQ#/GNT# protocol saves two pins on both V1-LS and V3-LS. The IRQ13 signal is also embedded because the coprocessor interface is in V1-LS, while the interrupt controllers are located in V3-LS. To use this interface BSEREN, index register 20H, bit 0 must be set to ‘1’.

13.3.3 PCI Bus Interface

The VESUVIUS supports configuration Type 0 with 64 bytes of configuration space (offset 00H-03FH). The PCI configuration address and data registers are located at the standard 0CF8H and 0CFCH locations. Since some registers within these 64 bytes are reserved, any write to these areas is to be ignored and any read from these areas is to be returned with all ‘0’s, as recommended by the PCI Local Bus Specification 2.1.

13.3.3.1 PCI Master Arbitration Scheme

The V1-LS supports up to five PCI masters, one of which is dedicated to the V3-LS’s PCI-to-ISA bridge, and the remaining four dedicated to REQ[3:0]# and GNT[3:0]# pairs for other PCI masters. Since V3-LS represents the ISA DMA and ISA Masters which do not support preemptive mechanisms, the V3-LS has the highest priority in the arbitration. The VESUVIUS supports a rotating priority scheme for the other PCI masters since they all have the same level of priority. Note that the arbiter will only grant to the requesting master after the write buffer has been emptied. Since the V3-LS REQ#/GNT# protocol is embedded in the BSER1TO3 and BSER3TO1 signals, there are only four pairs of REQ# and GNT# signals.

NOTE: For the SmartDock™ interface, REQ2#/GNT2# are redefined as FLOAT_REQ# and FLOAT_GNT# functions.

13.3.3.2 PCI-to-ISA Cycle Translation

V3-LS has three physical address spaces – Memory, Input/Output (I/O) and Configuration Address Spaces. A subtractive decoding scheme is implemented in V3-LS on power-up, and is used for ISA bus target, however, positive decoding is performed for interrupt acknowledge and PCI configuration cycles. V3-LS responds to INTA, I/O Read / Write, Memory Read / Write and Configuration Read / Write cycles.

V3-LS generates the PCI bus request for DMA or ISA master, and all ISA master and DMA cycle is translated by V3-LS into a PCI cycle. For ISA DMA to PCI Target devices, IOCHRDY will be used to extend the ISA commands until the PCI cycle is finished. PCI claims its cycle by using DEVSEL#. If no PCI agent claims the cycle, V3-LS will claim the pending cycle with subtractive DEVSEL#, perform the PCI to ISA transfer and return TRDY# when cycle is finished.

13.3.3.3 Interrupt Handling (INT[A:D]# and MIRQ[0:3])

V3-LS has an option to translate 'level sensitive' PCI interrupts into standard AT interrupts by using index register 12H, bits [3:0] to control the corresponding INT[A:D]# and MIRQ[0:3] signals. If a bit is set low, INTx# will be in PCI INTx# – level sensitive, active low – format. If a bit is set high, INTx# will be in Mappable IRQ (MIRQ) – ISA edge sensitive, active high – format. When using the MIRQ format, MIRQ [0:3] will be steered to any IRQs that are programmed in the corresponding PINTM1 and PINTM2 registers. This greatly enhances Plug and Play functionality, especially for systems which do not need all of the INT[A:D]# signals. For example, the PCI devices may use INT[A:B]# while Plug and Play ISA devices can be connected to MIRQ[2:3].

13.3.3.4 PCI Error Handling

There are three ways to generate a NMI. IOCHK# will generate a NMI for an ISA cycle. For PCI cycles, V3-LS will monitor the PERR# and SERR# signals and generate a NMI according to configuration setting for PCI cycle. This function can be enabled in Register ISA-BCR, index register 90h, bits [5:4]. When an NMI occurs, the BIOS can find out which pin trigger the NMI by reading index register 90H, bits [7:6].

13.3.4 ISA Bus Interface

Dual ISA

Although PCI is a popular docking bus, ISA bus support is still indespensible inside the docking station. To support the ISA bus, both notebook system and docking station will need to incorporate a PCI-to-ISA bridge (V3-LS). This will create two ISA buses running on one system, thus termed Dual ISA.

When docking with Dual ISA, the two buses need to be differentiated as a primary V3-LS and a secondary V3-LS (shown in Figure 13-2 on page 315). The major design differences in the primary and secondary V3-LS devices is shown in Table 13-3.

Table 13-3. ISA Bus Differences Between Primary and Secondary V3-LS

Major Differences	Primary V3-LS	Secondary V3-LS
DDMARETRY Signal	Pulled-down	Pulled-up
Decoding Scheme	Positive	Subtractive
DDMA	Master	Slave
IRQSER	Host	Source

13.3.5 Docking Interface

V3-LS is one component of the PicoPower SmartDock™ docking solution that incorporates several patent pending technologies. V3-LS's involvement in the docking solution is through its implementation of Serialized IRQ and Distributed DMA open standards. For complete information on docking or SmartDock, please reference the *SmartDock™ – The Hot-Docking Interface for VESUVIUS-LS* white paper and the NILE PCI-to-PCI Bridge Interface Controller Data Book. Both documents are available from your local National Semiconductor sales representative.

VESUVIUS-LS supports cold, warm and hot docking strategies. A block diagram of an integrated off-board (NILE in the docking station) docking design is shown in Figure 13-2 on page 315.

V3-LS supports legacy ISA IRQ[15:1] signals by incorporating the IRQSER standard. This implementation eliminates the false interrupts created by the standard docking glitches, since PCICLK is stopped such that any glitch on the IRQSER signal well be ignored during the docking process.

13.3.5.1 V3-LS Docking Operation

V1-LS sends a serial command through the BSER1TO3 pin to V3-LS asking V3-LS to keep the PCI bus and signals that go to the docking connector tristated. V1-LS also asks V3-LS not to request the PCI bus until further notice. Upon receiving the serial command, V3-LS completes the current cycle and does not start any new PCI cycles until V1-LS signals that it is ready. V3-LS keeps the PCI bus and signals that go to the docking station tristated, and acknowledges this to V1-LS with a serial command on BSER3TO1.

Once detecting an active FLOAT_REQ# the Power Management Control (PMC) Unit in V1-LS will put the system into Fully-On mode before asserting the FLOAT_GNT# signal.

13.3.5.2 Legacy DMA/IRQ on PCI-Bus

There are two major legacy DMA and IRQ requirements – PCI audio devices with Sound Blaster compatibility, and PCI Super I/O devices with FDC and Enhanced Capability Ports (ECP). The concern is how to select a particular DRQ channel when there is no DMA support on the PCI bus, and how to select a particular IRQ[15:1] channel when only INTA#, INTB#, INTC# and INTD# exist on the PCI bus.

The solution is to use Distributed DMA (DDMA) and Serialized IRQ (IRQSER). Each of these open standards are discussed in reference to the V3-LS in the following sections. For complete information please reference the respective standards.

To enable the DDMA function, index register 40H bit 0 must be set to '1'.

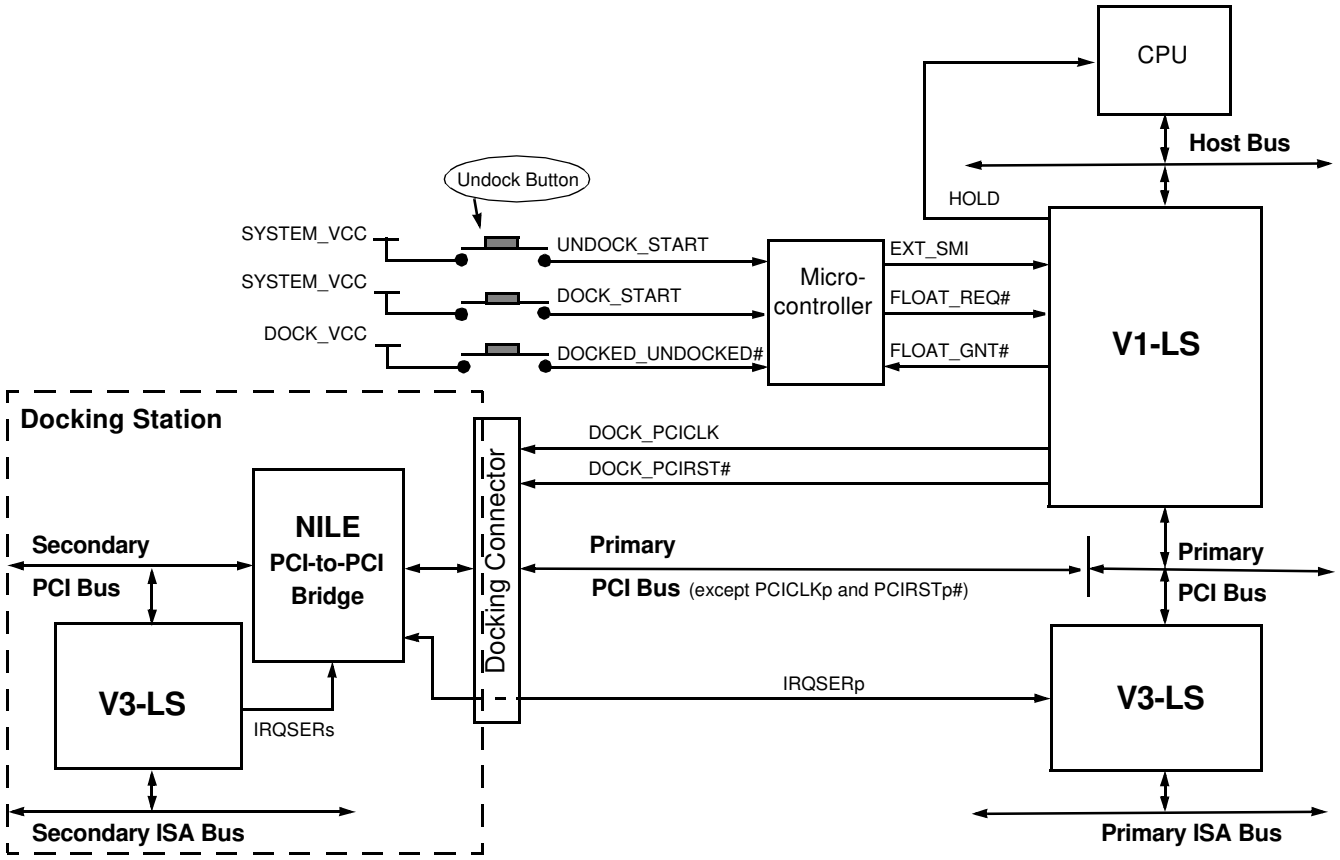


Figure 13-2. SmartDock ™ Block Diagram

13.3.5.3 Serialized IRQ (IRQSER) Support

IRQSER is a Wired-OR structure that simply replicates the state of each remote IRQ at the host controller and is only active to report the state transitions. Both high and low transitions must be reported, which means any IRQSER device that detects a transition on one of its IRQ[15:1] lines must issue a start cycle to update the host controller. A transfer, called an IRQSER cycle, consists of three frame types: one start frame, several IRQ / data frames and one stop frame, using the PCI clock as its clock source. To enable the IRQSER function, index register 13H needs to be programmed.

IRQSER Start Frame

There are two modes of operation for the IRQSER Start Frame – Quiet Mode and Idle Mode.

During Quiet (Active) Mode any device may initiate a Start Frame by driving IRQSER low for one clock After driving low for one clock, the IRQSER must immediately be tristated without at any time driving high. A Start Frame may not be initiated while the IRQSER is active and must be idle between Stop and Start Frames. IRQSER, on the other hand, is active between Start and Stop Frames. This allows the IRQSER to be idle when there is no IRQ or data transitions, which should be most of the time.

Once a Start Frame has been initiated, the host controller will take over by driving the IRQSER low in the next three clock cycles, and will continue driving the IRQSER low for a programmable period of three to seven clocks more. This makes a total low pulse width of four to eight clocks.

Any IRQSER device which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the host controller, unless the IRQSER is already in an IRQSER cycle and the IRQ/Data transition can be delivered in that IRQSER cycle.

During Idle (Continuous) Mode only the host controller can initiate the Start Frame to update IRQ/Data line information. All other IRQSER agents become passive and may not initiate a Start Frame. IRQSER will be driven low for four to eight clocks by the host controller. This mode has two functions. It can be used to stop or idle the IRQSER, or to allow the host controller to operate IRQSER in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An IRQSER mode transition can only occur during a Stop Frame. Upon reset, IRQSER bus is defaulted to Continuous Mode; therefore only the host controller can initiate the first Start Frame. The slave must continuously sample the Stop Frame pulse width to determine the next IRQSER cycle's mode.

IRQ/Data Input Detection

To assure that an IRQSER agent does not miss narrow IRQ/Data input pulses, it is recommended that IRQSER devices detect IRQ/Data input through a low level extender. IRQSER devices should detect any high to low transitions on an IRQ/Data input, and keep the transition latched until it has successfully been transmitted to the host through the IRQSER bus. On the other hand, short low to high pulses are considered glitches in the PC/AT system and can be ignored by IRQSER device.

IRQ/Data Frame

Once the Start Frame has been initiated, all IRQSER devices must watch for the rising edge of the Start Frame pulse and start counting IRQ/Data Frames from that point. Each IRQ/Data Frame is three clocks. This consists of a sample phase, recovery phase and a turn-around phase. During the sample phase, the IRQSER device must drive the IRQSER signal low, if an only if, its last detected IRQ/Data value was low. If the IRQ/Data value is high, IRQSER must be left tristated. During the recovery phase, the IRQSER device must drive the IRQSER high, if and only if, it had driven the IRQSER low during the previous sample phase. During the turn-around phase, all IRQSER devices must be tristated. All IRQSER devices must drive the IRQSER line low at the appropriate sample point if the associated IRQ/Data line is low, regardless of which device initiated the Start Frame.

The Sample Phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three minus one (e.g. THe IRQ5 sample clock is the sixth IRQ/Data Frame, (6 x 3) - 1 = 17th clock after the rising edge of Start Pulse. These values have been calculated in Table 13-4 on page 317.

At the end of each sample phase, the host controller will sample the state of the IRQSER line and replicate the status of the original IRQ/Data line at the input to the 8259 Interrupt Controller. Slot [22:18], INTA#, INTB#, INTC# and INTD# are optional. The required minimum IRQ/Data Frame is 17.

Table 13-4. IRQSER Sampling Periods

IRQ/Data Frame	Signal Sampled	Number of Clocks Past Start
1	IRQ0	2
2	IRQ1	5
3	SMI#	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47
17	IOCHCK#	50
18	INTA#	53
19	INTB#	56
20	INTC#	59
21	INTD#	62
32:22	Unassigned	95

Stop Cycle Frame

Once the IRQ/Data Frame has been completed, the host controller will terminate IRQSER activity by initiating a Stop Frame. Only the host controller can initiate the Stop Frame. A Stop Frame is indicated when the IRQSER is low for two or three clocks. If the Stop Frame's low time is two clocks, the next IRQSER cycle's sampled mode is the Quiet Mode. Any IRQSER device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks, the next IRQSER cycle's sampled mode is the Continuous Mode. Only the host controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

The IRQSER bus uses PCIRST# as its reset signal and follows the PCI bus reset mechanism. The IRQSER pin is tristated by all agents while PCIRST# is active. With reset, IRQSER slave and bridges are put into the Idle Mode. The host controller is responsible for starting the initial IRQSER cycle to connect system's IRQ/Data default values. The system then follows with the Continuous/Quiet Mode protocol (Stop Frame pulse width) for subsequent IRQSER cycles. It is host controller's responsibility to provide the default values to 8259's and other system logic before the first IRQSER cycle is performed. For IRQSER system suspend, insertion or removal application, the host controller should be programmed to Idle Mode first. This is to guarantee IRQSER bus is in Idle Mode before the system configuration changes.

13.3.6 Distributed DMA (DDMA) Support

DDMA is a Direct Memory Access open standard that supports legacy devices on the PCI bus. The standard defines that there is only one "Master DMAC" in a system, and that all slave DMA devices have a base register and a DRQ/IRQ definition. In this system, all slave devices positively decode the DMA I/O registers, PCI-to-PCI bridge and secondary PCI-to-ISA bridge. Each device in the system that has a legacy DMA programming model requirement, must have at least one compatible programming model bus master. This has the effect of breaking the two legacy 8237 DMA controllers into separate channels, existing in different devices. The method defined here allows the separation in the hardware architecture, and yet allows the OS and application base to still utilize two 8237-compatible DMA controllers.

13.3.6.1 DMA Master

Each DMA slave channel has a block of 16- and 8-bit registers, as defined in Table 13-5. The blocks are locatable anywhere in the legacy 64K I/O space by programming the DMA Slave Configuration Register, index register 44H - 5CH. As stated earlier, all DMA channels must have an identical programming model. The DMA Master will be programmed with the base address of each DMA slave by having a matching base address register for each channel.

Table 13-5. DMA Slave Channel Registers

Slave Address	R/W	Register Name
Base + 0	W	Base Address 0-7
Base + 0	R	Current Address 0-7
Base + 1	W	Base Address 8-15
Base + 1	R	Current Address 8-15
Base + 2	W	Base Address 16-23
Base + 2	R	Current Address 16-23
Base + 3	W	Base Address 24-31
Base + 3	R	Current Address 24-31
Base + 4	W	Base Word Count 0-7
Base +4	R	Current Word Count 0-7
Base + 5	W	Base Word Count 0-7
Base + 5	R	Current Word Count 0-7

Table 13-5. DMA Slave Channel Registers

Slave Address	R/W	Register Name
Base + 6	W	Base Word Count 0-7
Base + 6	R	Current Word Count 0-7
Base + 7	N/A	Reserved
Base + 8	W	Command
Base + 8	R	Status
Base + 9	W	Request
Base + A	N/A	Reserved
Base + B	W	Mode
Base + C	W	Reserved
Base + D	W	Master Clear
Base + E	N/A	Reserved
Base + F	R/W	Multi-Channel Mask

NOTE: All Reserved addresses must be decoded by the DMA Slave Channel for both write and read access.
Read access to a Reserved address must return all zeros.
Read access to a write only address is undefined.

13.3.6.2 DMA Master

It is the function of the DMA Master to translate I/O cycles to or from the legacy DMA controllers into I/O cycles to or from DMA Slave channels. V3-LS must translate all the PCI I/O reads and writes to the legacy DMA I/O addresses into DMA Slave I/O reads and writes. V3-LS is required to handle accesses to unassigned legacy DMA channels.

13.3.6.3 DDMA Operation

When the CPU attempts to read or write a legacy DMA register, a PCI I/O cycle will be initiated on the PCI bus with a legacy address. V3-LS will take control of this cycle by driving DEVSEL# active, driving its PCI REQ# pin active, and issuing a retry to terminate this cycle.

When granted the PCI bus, V3-LS will run up to four PCI I/O byte read/writes. The purpose of these read/writes is to return/send the individual channel read/write information. The DMA Slave device, which is either a secondary V3-LS or a PCI Sound Blaster, must only respond to the slave address assigned to it and not any legacy address.

At the end of the last read/write the primary V3-LS DMA Master will set an internal flag indicating completion, will drive the REQ pin inactive and wait for a retried PCI I/O read/write from the CPU.

The PCI I/O read/write will be retried. If it was a read, the primary V3-LS DMA Master will return the data. If it was a write, the primary V3-LS DMA Master will simply terminate the cycle. The primary V3-LS DMA Master will then reset the internal flag.

13.4 Power Management in V3-LS

There are power management features and detectors located in V3-LS, however, the power management controller is located in V1-LS. For a discussion of the VESUVIUS-LS power management abilities, please reference the V1-LS power management section.

13.5 Single 8-bit BIOS ROM

V3-LS provides for a single 8-bit BIOS ROM in order to save space and power. All necessary cycle conversions from 16 to 8-bit cycles are handled internally by the AT bus controller to provide the simplest possible ROM interface. VESUVIUS-LS support up to 256KB of ROM size which can be programmed by 32KB blocks. Please see index register 03H for more details on the programming.

V3-LS also provides the support for the Flash ROM through conditional control to the ROM_KB_CS# pin. The FLASHEN bit, index register 03H bit 6, enables a Flash ROM to be written by providing a valid ROM chip select for any memory write to the ROM address range. Normally ROM_KB_CS# would only be active on memory reads, and ROM_KB_CS# will only respond to memory reads when FLASHEN bit is low. With this implementation the MEMW# command can be directly connected to the program pin on the Flash ROM.

ROM_KB_CS# is a combination of KBCS# and ROMCE#, therefore ROMCE# will be disabled during DMA cycle. And also V3-LS will generate ROM_KB_CS# for system BIOS based on PCI address.

13.6 Back-to-Back I/O Delay

Computer systems built with newer generations of fast CPUs often have problems with older AT bus devices that expect to see significant delays between adjacent I/O cycles. For example, some AT bus devices and their associate software execute on I/O cycle followed by a several non-I/O instructions followed by another I/O cycle. In this context they require a certain delay between the two I/O cycles. This was reliably assured with previous generations of CPUs because the intervening instructions caused a sufficient delay by virtue of their relatively slower execution time. With the 586-class CPUs, however, many instructions execute much faster than previous generations of CPUs, such that the same AT bus hardware/software systems that ran fine with older CPUs may fail with 586-class CPUs. V3-LS provides an option to increase the minimum delay between I/O cycles from the nominal 1.5 AT bus clocks to 3.5, 5.5 or 7.5 AT bus clocks. The back to back I/O delay option is selected by index register 01H bits [5:4] for 16-bit I/O or bits [7:6] for 8-bit I/O cycles. The default value for the VESUVIUS-LS is the maximum, 7.5 bus clocks.

13.7 Hidden AT Bus Refresh

V3-LS implements only the hidden AT Bus refresh mechanism. The hidden refresh works by decoupling the AT bus from the CPU bus and local memory. Therefore, AT bus refresh cycles may occur simultaneously with CPU accesses to local memory. The result is that AT bus refresh cycles no longer tie up the CPU, since the accesses occur in parallel with normal CPU operation. This parallel operation provides a significant increase in system performance, and although the AT Bus refresh is hidden, its operation on the bus is still completely AT compatible, including the standard AT refresh counter and RAS-only refresh control logic.

13.8 General Purpose Extensions

Because portable computer systems never seem to have enough GPIOs, VESUVIUS provides an expansion option that allows up to 16 additional GPIOs. This allows for one or two external latches to be connected directly to the SD bus and to be gated by the GPEXT# output. This function can be enabled by registers index registers 06H and 07H.

A write to index register 06H will drive SD[7:0] to the value that corresponds to bits [7:0], and GPEXT# will be pulsed low so that SD[7:0] can be latched to an external 8- or 16-bit flip-flop on the rising (or falling) edge of GPEXT#. The byte contains information previously written to index 61H if the 16-bit output extensions are required. To enable this operation, the BIOS should first set up index register 07H, and then write to 06H.

A write to index register 06H will store an 8-bit value that corresponds to the upper 8-bit of a GPEXT# cycle. A write to index 60h will trigger GPEXT# such that index register 07H, bits [7:0] onto SD[15:8], allowing 16-bit general purpose output extensions.

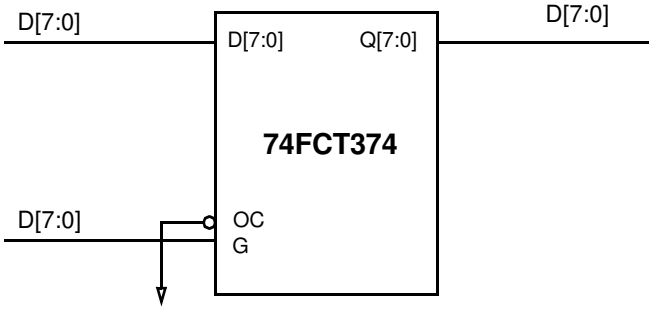


Figure 13-3. General Purpose Extension

14. V3-LS REGISTER INFORMATION

This chapter describes the registers contained in the V3-LS device. The registers are divided into the following groups:

- Revision ID Register
- AT Control Registers
- BIOS Control Registers
- GPEXT Register
- Interrupt Mapping Registers
- Power Management Registers
- 8254/8259/8237 Shadow Registers
- PCI Configuration Registers
- PCI-DMA Configuration Registers
- Standard AT Ports

As shown in the list above, there are different groups of registers inside V3-LS that are accessed through different mechanisms :

1. Access to V3-LS index registers must be executed as byte-wide I/O access to 26H
2. Access to V3-LS PCI Configuration space must be through I/O addresses 0CF8H, 0CFCH
3. Standard AT I/O ports must be accessed through their corresponding I/O addresses (000H-0FFH)

NOTE: Some registers discussed here may not be consecutively numbered. Registers reserved for future expansion are not shown in this chapter.

14.1 Register Summary Table

This table shows the index numbers and page cross-references to detailed register descriptions.

14.2 Revision ID Register (V3REV_ID)

Index: 00H

Bit	Description	Name	Reset State
0	V3-LS Mask ID	V3LS_MSK	X
1	V3-LS Mask ID	V3LS_MSK	X
2	V3-LS Mask ID	V3LS_MSK	X
3	V3-LS Mask ID	V3LS_MSK	X
4	V3-LS Revision ID	V3LS_REV	X
5	V3-LS Revision ID	V3LS_REV	X
6	V3-LS Revision ID	V3LS_REV	X
7	V3-LS Revision ID	V3LS_REV	X

Bit	Description
3:0	**V3-LS Mask ID Number [3:0]:** This indicates the metal-mask version of the V3-LS device.

Bit [2:0]	Mask ID
'0000'	A
'0001'	B
'0011'	C

Bit	Description
7:4	**V3-LS Revision ID Number [3:0]:** This indicates the revision of the V3-LS device.

Bit [2:0]	Revision ID
'0001'	A
'0010'	B
'0011'	C

14.3 AT Control Registers

14.3.1 AT Control Register 1 (ATCR1)

Index: 01H

Bit	Description	Name	Reset State
0	SYSCLK Divisor Select	SYSDIV	'0'
1	SYSCLK Divisor Select	SYSDIV	'0'
2	SYSCLK Divisor Select	SYSDIV	'1'
3	Reserved		'0'
4	Back-to-Back Delay for 16-bit I/O Cycle	B2BD16	'1'
5	Back-to-Back Delay for 16-bit I/O Cycle	B2BD16	'1'
6	Back-to-Back Delay for 8-bit I/O Cycle	B2BD8	'1'
7	Back-to-Back Delay for 8-bit I/O Cycle	B2BD8	'1'

Bit — **Description**

2:0 — **SYSCLK Divisor Select:**

Bit [2:0]	SYSCLK Rate
'000'	BSERCLK/2
'001'	BSERCLK/3
'010'	BSERCLK/4
'011'	BSERCLK/5
'100'	BSERCLK/6
'101'	Reserved
'110'	Reserved
'111'	14MHZCLK/2

3 — Reserved

5:4 — **Back-to-Back Delay for 16-bit I/O Cycle**

Bit [1:0]	I/O Spacing in SYSCLKs
'00'	0.5
'01'	1.5
'10'	2.5
'11'	3.5

NOTE: These bits apply to Revision BB silicon and beyond.

7:6 — **Back-to-Back Delay for 8-bit I/O Cycle:**

Bit [1:0]	I/O Spacing in SYSCLKs
'00'	0.5
'01'	2.5
'10'	4.5
'11'	6.5

NOTE: These bits apply to Revision BB silicon and beyond.

14.3.2 AT Control Register 2 (ATCR2)

Index: 02H

Bit	Description	Name	Reset State
0	AT Bus Refresh Enable	ATREFEN	'0'
1	Extended AT Address	EXTATADD	'0'
2	V3-LS Internal I/O Port Option	FSTV3IOEN	'0'
3	EISA Type CMOS RAM I/F Control Enable	EISA_CMO	'0'
4	Reserved		'0'
5	Reserved		'0'
6	External Keyboard Chip Select	EXTKBCS	'1'
7	Reserved		'0'

Bit	Description
0	**AT Bus Refresh Enable:** When low, AT Bus refresh function will be disabled.
1	**Extended AT Address:** When high, address bit AD[31:24] will be ignored for AT decoding logic and the ISA cycle will be generated with alias at 16 Mbyte memory boundary.
2	**V3-LS Internal I/O Port Option:** When low, all V3 I/O cycles are the same as normal AT 8-bit ISA I/O cycles; when high, access to the V3-LS internal I/O port will speed up and not propagate to the ISA bus. **NOTE:** This bit applies to Revision BB silicon and beyond.
3	**EISA Type CMOS RAM I/F Control Enable:** When low, ASRTC/DSRTC/RWRTC will be standard RTC interface control signals; when high, ASRTC/DSRTC/RWRTC will become EISA type CMOS RAM address strobe, data strobe, and output enable interface. **NOTE:** This bit applies to Revision BB silicon and beyond.
5:4	Reserved
6	**External Keyboard Chip Select:** When '1', ROM_KBCS# pin will decode I/O access 60/62/64/66 as keyboard ports; when '0', ROM_KBCS# pin will decode I/O access 60/64 as keyboard ports. **NOTE:** This bit applies to revision BB silicon and beyond.
7	Reserved

14.4 BIOS CS# Control Register (BCSC)

Index: 03H

Bit	Description	Name	Reset State
0	Enable ROMCS#	ENC0ROMCS	'0'
1	Enable ROMCS#	ENC8ROMCS	'0'
2	Enable ROMCS#	END0ROMCS	'0'
3	Enable ROMCS#	END8ROMCS	'0'
4	Enable ROMCS#	ENE0ROMCS	'0'
5	Enable ROMCS#	ENE8ROMCS	'0'
6	Flash Enable	FLASHEN	'0'
7	Reserved		'0'

Bit	Description
0	**Enable ROMCS#:** Enable ROMCS# for C0000H-C7FFFH area.
1	**Enable ROMCS#:** Enable ROMCS# for C8000H-CFFFFH area.
2	**Enable ROMCS#:** Enable ROMCS# for D0000H-D7FFFH area.
3	**Enable ROMCS#:** Enable ROMCS# for D8000H-DFFFFH area.
4	**Enable ROMCS#:** Enable ROMCS# for E0000H-E7FFFH area.
5	**Enable ROMCS#:** Enable ROMCS# for E8000H-EFFFFH area.
6	**Flash Enable:** When high, ROMCS# will be generated for memory write as well as memory read cycle. When low, ROMCS# will only be active for memory reads.
7	Reserved

NOTE: Accesses to FE000000H-FFFFFFFFH will always generate ROMCS#.
Accesses to 000F0000H-000FFFFFH will generate ROMCS# if the region is not shadowed.

14.5 Port 92 Control Regist er (P92CNTL)

Index: 05H

Bit	Description	Name	Reset State
0	Port 92 Enable	P92EN	'0'
1	Security Lock 1 Enable	SLOCK1EN	'0'
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'

Bit	Description
0	**Port 92 Enable:** '0' = Port 92 disabled, '1' = Port 92 enabled.
1	**Security Lock 1 Enable:** '0' = disable Port 92 bit 3, SCLOCK1 function; '1' = enable SCLOCK1 function.
7:2	Reserved

14.6 GPEXT Control Registers

14.6.1 GPEXT Low Byte Register (GPEXT_LB)

Index: 06H

Bit	Description	Name	Reset State
0	GPEXT Port Data [0]	GPEXT0	'0'
1	GPEXT Port Data [1]	GPEXT1	'0'
2	GPEXT Port Data [2]	GPEXT2	'0'
3	GPEXT Port Data [3]	GPEXT3	'0'
4	GPEXT Port Data [4]	GPEXT4	'0'
5	GPEXT Port Data [5]	GPEXT5	'0'
6	GPEXT Port Data [6]	GPEXT6	'0'
7	GPEXT Port Data [7]	GPEXT7	'0'

Bit	Description
7:0	**GPEXT Port Data [7:0]:** A write to this register will drive SD[7:0] to the value that corresponds to bit [7:0] and GPEXT# will be pulsed low so that SD[7:0] can be latched by an external 8- or 16-bit flip-flop on the rising edge (or trailing edge) of GPEXT#. The byte content, previously written to Index 07H, will also be driven onto SD[15:8] so that an extension up to 16 outputs is possible. Note that, since GPEXT# will not pulse on a write to Index 07H, if 16 output extension is required, the BIOS should first setup GPEXT_HB and then write to GPEXT_LB. A read to this register will return the value last written.

14.6.2 GPEXT High Byte Register (GPEXT_HB)

Index: 07H

Bit	Description	Name	Reset State
0	GPEXT Port Data [0]	GPEXT0	'0'
1	GPEXT Port Data [1]	GPEXT1	'0'
2	GPEXT Port Data [2]	GPEXT2	'0'
3	GPEXT Port Data [3]	GPEXT3	'0'
4	GPEXT Port Data [4]	GPEXT4	'0'
5	GPEXT Port Data [5]	GPEXT5	'0'
6	GPEXT Port Data [6]	GPEXT6	'0'
7	GPEXT Port Data [7]	GPEXT7	'0'

Bit	Description
7:0	**GPEXT Port Data [15:8]:** A write to this register will store an 8-bit value that corresponds to the upper 8-bit of a GPEXT# cycle. A write to Index 06H will trigger GPEXT# such that GPEXT_LB bit [7:0] will be driven onto SD[7:0] while GPEXT_HB bit [7:0] onto SD[15:8] allowing 16-bit general purpose output extension. Note that, GPEXT# will not pulse on a write to Index 07H. A read to this register will return the value last written.

14.6.3 Miscellaneous Configuration Register (MISC_CNFG)

Index: 08H

Bit	Description	Name	Reset State
0	BSER Arbitration Enable	BSER_ARBEN	'0'
1	DDMARETRY Enable#	DDMARETRYEN#	'0'
2	BSER Interrupt Enable	BSER_INTREN	'0'
3	DDMA Grant Enable	DDMA_GNTEN	'0'
4	Reserved		'0'
5	Timer Synchronous IOW# Fix Enable	TMR_SYNWR_EN	'0'
6	Reserved		'0'
7	Reserved		'0'

Bit	Description
0	**BSER Arbitration Enable:** If this bit is set to '0', BSER bus' REQ#/GNT# slot will be disabled and the V3-LS device will use SREQ#/SGNT# pair. If set to '1', the BSERBUS will be used for ISA DMA arbitration.
1	**DDMARETRY Enable#:** When this bit is set to '0', pin 44 (176-pin package) is defined as DDMA_RETRY. When set to '1', pin 44 (176-pin package) is defined as ISA_WAKE. **NOTE:** Pin 44 (176-pin package) is the same as pin 48 (208-pin package). This bit applies to Revision BB silicon and beyond.
2	**BSER Interrupt Enable:** '0' = BSER bus INTR slot is disabled; '1' = BSER bus INTR slot is enabled.
3	**DDMA Grant Enable:** '0' = V3 will use REQ#/GNT# pair for DDMA retry cycle; '1' = V3-LS will not. **NOTE:** BIOS needs to set this bit to '1' before V1 can work with V3-LS's DDMA_RETRY function. This bit applies to Revision BB silicon and beyond.
4	**Reserved**
5	**Timer Synchronous IOW# Fix Enable:** '0' = enable fix; '1' = disable fix.
6	**ISA Master I/O Command Synchronizer Disable:**
7:4	Reserved

14.7 Interrupt Mapping Registers

14.7.1 PCI Interrupt Mapping Register 1 (PCI_INTM1)

Index: 10H

Bit	Description	Name	Reset State
0	Map INTA# to IRQx [0]	MAP_INTA0	'0'
1	Map INTA# to IRQx [1]	MAP_INTA1	'0'
2	Map INTA# to IRQx [2]	MAP_INTA2	'0'
3	Map INTA# to IRQx [3]	MAP_INTA3	'0'
4	Map INTB# to IRQx [0]	MAP_INTB0	'0'
5	Map INTB# to IRQx [1]	MAP_INTB1	'0'
6	Map INTB# to IRQx [2]	MAP_INTB2	'0'
7	Map INTB# to IRQx [3]	MAP_INTB3	'0'

Bit	Description
3:0	**Map INTA# to IRQx[3:0]:**

0H	Disabled	8H	Reserved
1H	Reserved	9H	IRQ9
2H	Reserved	AH	IRQ10
3H	IRQ3	BH	IRQ11
4H	IRQ4	CH	IRQ12
5H	IRQ5	DH	Reserved
6H	IRQ6	EH	IRQ14
7H	IRQ7	FH	IRQ15

Bit	Description
7:4	**Map INTB# to IRQx [3:0]:**

0H	Disabled	8H	Reserved
1H	Reserved	9H	IRQ9
2H	Reserved	AH	IRQ10
3H	IRQ3	BH	IRQ11
4H	IRQ4	CH	IRQ12
5H	IRQ5	DH	Reserved
6H	IRQ6	EH	IRQ14
7H	IRQ7	FH	IRQ15

14.7.2 PCI Interrupt Mapping Register 2 (PCI_INTM2)

Index: 11H

Bit	Description	Name	Reset State
0	Map INTC# to IRQx [0]	MAP_INTC0	'0'
1	Map INTC# to IRQx [1]	MAP_INTC1	'0'
2	Map INTC# to IRQx [2]	MAP_INTC2	'0'
3	Map INTC# to IRQx [3]	MAP_INTC3	'0'
4	Map INTD# to IRQx [0]	MAP_INTD0	'0'
5	Map INTD# to IRQx [1]	MAP_INTD1	'0'
6	Map INTD# to IRQx [2]	MAP_INTD2	'0'
7	Map INTD# to IRQx [3]	MAP_INTD3	'0'

Bit	Description			
3:0	**Map INTC# to IRQx [3:0]:**			
	0H	Disabled	8H	Reserved
	1H	Reserved	9H	IRQ9
	2H	Reserved	AH	IRQ10
	3H	IRQ3	BH	IRQ11
	4H	IRQ4	CH	IRQ12
	5H	IRQ5	DH	Reserved
	6H	IRQ6	EH	IRQ14
	7H	IRQ7	FH	IRQ15
7:4	**Map INTD# to IRQx [3:0]:**			
	0H	Disabled	8H	Reserved
	1H	Reserved	9H	IRQ9
	2H	Reserved	AH	IRQ10
	3H	IRQ3	BH	IRQ11
	4H	IRQ4	CH	IRQ12
	5H	IRQ5	DH	Reserved
	6H	IRQ6	EH	IRQ14
	7H	IRQ7	FH	IRQ15

14.7.3 PCI INT# Configuration Register (PCI_INT_CFG)

Index: 12H

Bit	Description	Name	Reset State
0	Interrupt A / Mappable IRQ 0 Configuration	INTA_MIRQ0	'0'
1	Interrupt B / Mappable IRQ 1 Configuration	INTB_MIRQ1	'0'
2	Interrupt C / Mappable IRQ 2 Configuration	INTC_MIRQ2	'0'
3	Interrupt D / Mappable IRQ 3 Configuration	INTD_MIRQ3	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'

Bit	Description
0	**Interrupt A** / **Mappable IRQ 0 Configuration:** When set to '0', INTA#, the signal will go through a level-to-edge conversion. When set to '1', MIRQ0, the signal will bypass the level-to-edge conversion logic. In both cases, the input will be steered to the IRQx as programmed in PINTM1, bits [7:0].
1	**Interrupt B** / **Mappable IRQ 1 Configuration:** When set to '0', INTB#, the signal will go through a level-to-edge conversion. When set to '1', MIRQ1, the signal will bypass the level-to-edge conversion logic. In both cases, the input will be steered to the IRQx as programmed in PINTM1, bits [7:0]
2	**Interrupt C** / **Mappable IRQ2 Configuration:** When set to '0', INTC#, the signal will go through a level-to-edge conversion. When set to '1', MIRQ2, the signal will bypass the level-to-edge conversion logic. In both cases, the input will be steered to the IRQx as programmed in PINTM1, bits [7:0]
3	**Interrupt D** / **Mappable IRQ3 Configuration:** When set to '0', INTD#, the signal will go through a level-to-edge conversion. When set to '1', MIRQ3, the signal will bypass the level-to-edge conversion logic. In both cases, the input will be steered to the IRQx as programmed in PINTM1, bits [7:0]
7:4	Reserved

14.7.4 Serial IRQ Control Register (IRQSER_CNTL)

Index: 13H

Bit	Description	Name	Reset State
0	Serial IRQ Bus Enable	IRQSEREN	'0'
1	Host Poll	HOST_POLL	'0'
2	Start Cycle [0]	START_CYC0	'0'
3	Start Cycle [1]	START_CYC1	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Serial IRQ Mode	IRQSER_MODE	'0'
7	Reserved		'0'

Bit	Description
0	**Serial IRQ Bus Enable:** '0' = disabled; '1' = enabled.
1	**Host Poll:** Setting this bit to '1' performs a host polling. When in Idle Mode, only the host controller can initiate the Start Frame by IRQSER = '0', or host polling.
3:2	**Start Cycle [1:0]:** This indicates the length of 'START' state active-low: **Bit [1:0]** — **Number of Clocks** '00' — 4 '01' — 6 '10' — 8 '11' — 10
5:4	Reserved
6	**Serial IRQ Mode:** Setting this bit to '0' indicates a host; setting it to '1' indicates a source. Primary V3-LS is the host while the secondary V3-LS is the source.
7	Reserved

14.7.5 Serial IRQ Control Register 2 (IRQSER_CNTL2)

Index: 14H

Bit	Description	Name	Reset State
0	Serial IRQ Sampling Slot Length [0]	IRQSER_LEN0	'1'
1	Serial IRQ Sampling Slot Length [1]	IRQSER_LEN1	'1'
2	Serial IRQ Sampling Slot Length [2]	IRQSER_LEN2	'1'
3	Serial IRQ Sampling Slot Length [3]	IRQSER_LEN3	'1'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'

Bit	Description
3:0	**Serial IRQ Sampling Slot Length:** '1111' = 32 slots. **NOTE:** These bits apply to Revision BB silicon and beyond.
7:4	Reserved

14.8 Power Management Registers

14.8.1 Power Management Control Register (PMCR)

Index: 20H

Bit	Description	Name	Reset State
0	Burst Serial Bus Enable	BSEREN	'1'
1	Reserved		'0'
2	Primary Activity Enables PMI	PMIPAENB	'0'
3	IMR Disable	IMRDIS	'0'
4	Mask IRQ0 from SA	SAMSKIRQ0	'1'
5	Mask IRQ1 from SA	SAMSKIRQ1	'1'
6	SA Triggered by IRQ0	SAIRQ0ACT	'0'
7	SA Triggered by IRQ1	SAIRQ1ACT	'0'

Bit	Description
0	**Burst Serial Bus Enable:** '0' = disable, '1' = enable BSER1TO3 and BSER3TO1 serial bus for the passage of power management information between V1-LS and V3-LS.
1	Reserved
2	**Primary Activity Enables PMI:** When high, PA will trigger PMI; when low, will not
3	**IMR Disable:** When high, masked ISA IRQs will still trigger PA/SA/SMI, independent of 8259's IMR register value; when low, any ISA IRQs with the corresponding 8259's IMR bit set (masked) will not trigger PA/SA/SMI. **NOTE:** This bit applies to Revision BB silicon and beyond.
4	**Mask IRQ0 from SA:** When high, IRQ0 will not trigger a secondary activity. When low, it will.
5	**Mask IRQ1 from SA:** When high, IRQ1 will not trigger a secondary activity. When low, it will.
6	**SA Triggered by IRQ0:** When high, a secondary activity is triggered by IRQ0. Writing a '0' to this bit will clear it.
7	**SA Triggered by IRQ1:** When high, a secondary activity is triggered by IRQ1. Writing a '0' to this bit will clear it.

14.8.2 Primary Activity IRQ Mask Register 1 (PAIRQM1)

Index: 21H

Bit	Description	Name	Reset State
0	Reserved	Reserved	'1'
1	Mask IRQ1 from PA	PAMSKIRQ1	'1'
2	Mask NMI from PA	PAMSKNMI	'1'
3	Mask IRQ3 from PA	PAMSKIRQ3	'1'
4	Mask IRQ4 from PA	PAMSKIRQ4	'1'
5	Mask IRQ5 from PA	PAMSKIRQ5	'1'
6	Mask IRQ6 from PA	PAMSKIRQ6	'1'
7	Mask IRQ7 from PA	PAMSKIRQ7	'1'

Bit	Description
0	Reserved
1	**Mask IRQ1 from PA:** When high, IRQ1 will not trigger a primary activity. When low, it will.
2	**Mask NMI from PA:** When high, NMI will not trigger a primary activity. When low, it will.
3	**Mask IRQ3 from PA:** When high, IRQ3 will not trigger a primary activity. When low, it will.
4	**Mask IRQ4 from PA:** When high, IRQ4 will not trigger a primary activity. When low, it will.
5	**Mask IRQ5 from PA:** When high, IRQ5 will not trigger a primary activity. When low, it will.
6	**Mask IRQ6 from PA:** When high, IRQ6 will not trigger a primary activity. When low, it will.
7	**Mask IRQ7 from PA:** When high, IRQ7 will not trigger a primary activity. When low, it will.

14.8.3 Primary Activity IRQ Mask Register 2 (PAIRQM2)

Index: 22H

Bit	Description	Name	Reset State
0	Mask IRQ8 from PA	PAMSKIRQ8	'1'
1	Mask IRQ9 from PA	PAMSKIRQ9	'1'
2	Mask IRQ10 from PA	PAMSKIRQ10	'1'
3	Mask IRQ11 from PA	PAMSKIRQ11	'1'
4	Mask IRQ12 from PA	PAMSKIRQ12	'1'
5	Mask IRQ13 from PA	PAMSKIRQ13	'1'
6	Mask IRQ14 from PA	PAMSKIRQ14	'1'
7	Mask IRQ15 from PA	PAMSKIRQ15	'1'

Bit	Description
0	**Mask IRQ8 from PA:** When high, IRQ8 will not trigger a primary activity. When low, it will.
1	**Mask IRQ9 from PA:** When high, IRQ9 will not trigger a primary activity. When low, it will.
2	**Mask IRQ10 from PA:** When high, IRQ10 will not trigger a primary activity. When low, it will.
3	**Mask IRQ11 from PA:** When high, IRQ11 will not trigger a primary activity. When low, it will.
4	**Mask IRQ12 from PA:** When high, IRQ12 will not trigger a primary activity. When low, it will.
5	**Mask IRQ13 from PA:** When high, IRQ13 will not trigger a primary activity. When low, it will.
6	**Mask IRQ14 from PA:** When high, IRQ14 will not trigger a primary activity. When low, it will.
7	**Mask IRQ15 from PA:** When high, IRQ15 will not trigger a primary activity. When low, it will.

14.8.4 PMI Trigger IRQ Mask Register 1 (PMI_IRQM1)

Index: 23H

Bit	Description	Name	Reset State
0	Mask DDMA from PMI	IMSKDDMA	'1'
1	Mask IRQ1 from PMI	IMSKIRQ1	'1'
2	Reserved	Reserved	'1'
3	Mask IRQ3 from PMI	IMSKIRQ3	'1'
4	Mask IRQ4 from PMI	IMSKIRQ4	'1'
5	Mask IRQ5 from PMI	IMSKIRQ5	'1'
6	Mask IRQ6 from PMI	IMSKIRQ6	'1'
7	Mask IRQ7 from PMI	IMSKIRQ7	'1'

Bit	Description
0	**Mask DDMA from PMI:** When high, DDMA Slave Lock will not trigger a PMI. When low, it will.
1	**Mask IRQ1 from PMI:** When high, IRQ1 will not trigger a PMI. When low, it will.
2	Reserved
3	**Mask IRQ3 from PMI:** When high, IRQ3 will not trigger a PMI. When low, it will.
4	**Mask IRQ4 from PMI:** When high, IRQ4 will not trigger a PMI. When low, it will.
5	**Mask IRQ5 from PMI:** When high, IRQ5 will not trigger a PMI. When low, it will.
6	**Mask IRQ6 from PMI:** When high, IRQ6 will not trigger a PMI. When low, it will.
7	**Mask IRQ7 from PMI:** When high, IRQ7 will not trigger a PMI. When low, it will.

14.8.5 PMI Trigger IRQ Mask Register 2 (PMI_IRQM2)

Index: 24H

Bit	Description	Name	Reset State
0	Mask IRQ8 from PMI	IMSKIRQ8	'1'
1	Mask IRQ9 from PMI	IMSKIRQ9	'1'
2	Mask IRQ10 from PMI	IMSKIRQ10	'1'
3	Mask IRQ11 from PMI	IMSKIRQ11	'1'
4	Mask IRQ12 from PMI	IMSKIRQ12	'1'
5	Mask IRQ13 from PMI	IMSKIRQ13	'1'
6	Mask IRQ14 from PMI	IMSKIRQ14	'1'
7	Mask IRQ15 from PMI	IMSKIRQ15	'1'

Bit	Description
0	**Mask IRQ8 from PMI:** When high, IRQ8 will not trigger PMI. When low, it will.
1	**Mask IRQ9 from PMI:** When high, IRQ9 will not trigger PMI. When low, it will.
2	**Mask IRQ10 from PMI:** When high, IRQ10 will not trigger PMI. When low, it will.
3	**Mask IRQ11 from PMI:** When high, IRQ11 will not trigger PMI. When low, it will.
4	**Mask IRQ12 from PMI:** When high, IRQ12 will not trigger PMI. When low, it will.
5	**Mask IRQ13 from PMI:** When high, IRQ13 will not trigger PMI. When low, it will.
6	**Mask IRQ14 from PMI:** When high, IRQ14 will not trigger PMI. When low, it will.
7	**Mask IRQ15 from PMI:** When high, IRQ15 will not trigger PMI. When low, it will.

14.8.6 PMI Trigger Source Register 1 (PMI_IRQS1)

Index: 25H

Bit	Description	Name	Reset State
0	PMI Trigger Source DDMA Slave Lock	PMIDDMAACT	'0'
1	PMI Trigger Source IRQ1	PMIIRQ1ACT	'0'
2	Reserved		'0'
3	PMI Trigger Source IRQ3	PMIIRQ3ACT	'0'
4	PMI Trigger Source IRQ4	PMIIRQ4ACT	'0'
5	PMI Trigger Source IRQ5	PMIIRQ5ACT	'0'
6	PMI Trigger Source IRQ6	PMIIRQ6ACT	'0'
7	PMI Trigger Source IRQ7	PMIIRQ7ACT	'0'

Bit	Description
0	**PMI Trigger Source DDMA Slave Lock:** When high, PMI is triggered by DDMA Slave Lock. Writing '0' to this bit will clear it, writing '1' will have no effect.
1	**PMI Trigger Source IRQ1 Active:** When high, PMI is triggered by IRQ1. Writing '0' to this bit will clear it, writing '1' will have no effect.
2	Reserved
3	**PMI Trigger Source IRQ3 Active:** When high, PMI is triggered by IRQ3. Writing '0' to this bit will clear it, writing '1' will have no effect.
4	**PMI Trigger Source IRQ4 Active:** When high, PMI is triggered by IRQ4. Writing '0' to this bit will clear it, writing '1' will have no effect.
5	**PMI Trigger Source IRQ5 Active:** When high, PMI is triggered by IRQ5. Writing '0' to this bit will clear it, writing '1' will have no effect.
6	**PMI Trigger Source IRQ6 Active:** When high, PMI is triggered by IRQ6. Writing '0' to this bit will clear it, writing '1' will have no effect.
7	**PMI Trigger Source IRQ7 Active:** When high, PMI is triggered by IRQ7. Writing '0' to this bit will clear it, writing '1' will have no effect.

14.8.7 PMI Trigger Source Register 2 (PMI_IRQS2)

Index: 26H

Bit	Description	Name	Reset State
0	PMI Trigger Source IRQ8 Active	PMIIRQ8ACT	'0'
1	PMI Trigger Source IRQ9 Active	PMIIRQ9ACT	'0'
2	PMI Trigger Source IRQ10 Active	PMIIRQ10ACT	'0'
3	PMI Trigger Source IRQ11 Active	PMIIRQ11ACT	'0'
4	PMI Trigger Source IRQ12 Active	PMIIRQ12ACT	'0'
5	PMI Trigger Source IRQ13 Active	PMIIRQ13ACT	'0'
6	PMI Trigger Source IRQ14 Active	PMIIRQ14ACT	'0'
7	PMI Trigger Source IRQ15 Active	PMIIRQ15ACT	'0'

Bit	Description
0	**PMI Trigger Source IRQ8 Active:** When high, PMI is triggered by IRQ8. Writing '0' to this bit will clear it, writing '1' will have no effect.
1	**PMI Trigger Source IRQ9 Active:** When high, PMI is triggered by IRQ9. Writing '0' to this bit will clear it, writing '1' will have no effect.
2	**PMI Trigger Source IRQ10 Active:** When high, PMI is triggered by IRQ10. Writing '0' to this bit will clear it, writing '1' will have no effect.
3	**PMI Trigger Source IRQ11 Active:** When high, PMI is triggered by IRQ11. Writing '0' to this bit will clear it, writing '1' will have no effect.
4	**PMI Trigger Source IRQ12 Active:** When high, PMI is triggered by IRQ12. Writing '0' to this bit will clear it, writing '1' will have no effect.
5	**PMI Trigger Source IRQ13 Active:** When high, PMI is triggered by IRQ13. Writing '0' to this bit will clear it, writing '1' will have no effect.
6	**PMI Trigger Source IRQ14 Active:** When high, PMI is triggered by IRQ14. Writing '0' to this bit will clear it, writing '1' will have no effect.
7	**PMI Trigger Source IRQ15 Active:** When high, PMI is triggered by IRQ15. Writing '0' to this bit will clear it, writing '1' will have no effect.

14.9 8254/8237/8259 Shadow Registers

Index	AT I/O Port Address	Description	Default
30H	40H	8254 Counter 0 Initial Count Low Byte	XX
31H	40H	8254 Counter 0 Initial Count High Byte	XX
32H	41H	8254 Counter 1 Initial Count Low Byte	XX
33H	41H	8254 Counter 1 Initial Count High Byte	XX
34H	42H	8254 Counter 2 Initial Count Low Byte	XX
35H	42H	8254 Counter 2 Initial Count High Byte	XX
36H	43H	8254 Counter 0 Control Word	XX
37H	43H	8254 Counter 1 Control Word	XX
38H	43H	8254 Counter 2 Control Word	XX
39H	0BH	8237 DMA Controller Mode Register for Channel 0	XX
3AH	0BH	8237 DMA Controller Mode Register for Channel 1	XX
3BH	0BH	8237 DMA Controller Mode Register for Channel 2	XX
3CH	0BH	8237 DMA Controller Mode Register for Channel 3	XX
3DH	D6H	8237 DMA Controller Mode Register for Channel 4	XX
3EH	D6H	8237 DMA Controller Mode Register for Channel 5	XX
3FH	D6H	8237 DMA Controller Mode Register for Channel 6	XX
40H	D6H	8237 DMA Controller Mode Register for Channel 7	XX
41H	20H	8259 PIC 1 ICW 1	XX
42H	21H	8259 PIC 1 ICW 2	XX
43H	21H	8259 PIC 1 ICW 3	XX
44H	21H	8259 PIC 1 ICW 4	XX
45H	20H	8259 PIC 1 OCW 2	XX
46H	20H	8259 PIC 1 OCW 3	XX
47H	A0H	8259 PIC 2 ICW 1	XX
48H	A1H	8259 PIC 2 ICW 2	XX
49H	A1H	8259 PIC 2 ICW 3	XX
4AH	A1H	8259 PIC 2 ICW 4	XX
4BH	A0H	8259 PIC 2 OCW 2	XX
4CH	A0H	8259 PIC 2 OCW 3	XX
4DH	70H	RTC Index Register	XX
4EH		Reserved	XX
4FH	03F6H	Fixed Disk Register	XX
50H	01F1H	Hard Disk Write Precompression Register	XX
51H	08H	DMAC-1 Status Register	XX
52H	D0H	DMAC-2 Status Register	XX
53H	-	DMAC Mask Register	XX
54H	00H	CH0 Base Address Low Byte	XX
55H	00H	CH0 Base Address High Byte	XX
56H	01H	CH0 Base Count Low Byte	XX
57H	01H	CH0 Base Count High Byte	XX
58H	02H	CH1 Base Address Low Byte	XX
59H	02H	CH1 Base Address High Byte	XX
5AH	03H	CH1 Base Count Low Byte	XX
5BH	03H	CH1 Base Count High Byte	XX
5CH	04H	CH2 Base Address Low Byte	XX
5DH	04H	CH2 Base Address High Byte	XX

Index	AT I/O Port Address	Description	Default
5EH	05H	CH2 Base Count Low Byte	XX
5FH	05H	CH2 Base Count High Byte	XX
60H	06H	CH3 Base Address Low Byte	XX
61H	06H	CH3 Base Address High Byte	XX
62H	07H	CH3 Base Count Low Byte	XX
63H	07H	CH3 Base Count High Byte	XX
64H	C4H	CH5 Base Address Low Byte	XX
65H	C4H	CH5 Base Address High Byte	XX
66H	C6H	CH5 Base Count Low Byte	XX
67H	C6H	CH5 Base Count High Byte	XX
68H	C8H	CH6 Base Address Low Byte	XX
69H	C8H	CH6 Base Address High Byte	XX
6AH	CAH	CH6 Base Count Low Byte	XX
6BH	CAH	CH6 Base Count High Byte	XX
6CH	CCH	CH7 Base Address Low Byte	XX
6DH	CCH	CH7 Base Address High Byte	XX
6EH	CEH	CH7 Base Count Low Byte	XX
6FH	CEH	CH7 Base Count High Byte	XX
70H	08H	DMAC-0 Command Register	XX
71H	D0H	DMAC-1 Command Register	XX

NOTE: Shadow registers (SHAD30H to SHAD71H) are read-only registers.

14.10 PCI Configuration Registers

NOTE: The following PCI registers are accessed through the PCI configuration space through I/O addresses 0CF8H and 0CFCH. This should not be confused with the index registers of V3-LS which are accessed through I/O addresses 24H and 26H.

14.10.1 Vendor ID Register (VID)

Index: 00H

Bit	Description	Name	Reset State
0	Vendor ID Number	VID	'0'
1	Vendor ID Number	VID	'1'
2	Vendor ID Number	VID	'1'
3	Vendor ID Number	VID	'0'
4	Vendor ID Number	VID	'0'
5	Vendor ID Number	VID	'1'
6	Vendor ID Number	VID	'1'
7	Vendor ID Number	VID	'0'
8	Vendor ID Number	VID	'0'
9	Vendor ID Number	VID	'0'
10	Vendor ID Number	VID	'0'
11	Vendor ID Number	VID	'0'
12	Vendor ID Number	VID	'1'
13	Vendor ID Number	VID	'0'
14	Vendor ID Number	VID	'0'
15	Vendor ID Number	VID	'0'

Bit	Description
15:0	**Vendor ID Number:** These bits identify the manufacturer of the device, as specified in the PCI Local Bus Specification 2.1. For V3-LS, these bits are hard-wired to 1066H.

NOTE: This register is read-only.

14.10.2 Device ID Register (DID)

Index: 02H

Bit	Description	Name	Reset State
0	Device ID Number [0]	DID0	'0'
1	Device ID Number [1]	DID1	'1'
2	Device ID Number [2]	DID2	'0'
3	Device ID Number [3]	DID3	'0'
4	Device ID Number [4]	DID4	'0'
5	Device ID Number [5]	DID5	'0'
6	Device ID Number [6]	DID6	'0'
7	Device ID Number [7]	DID7	'0'
8	Device ID Number [8]	DID8	'0'
9	Device ID Number [9]	DID9	'0'
10	Device ID Number [10]	DID10	'0'
11	Device ID Number [11]	DID11	'0'
12	Device ID Number [12]	DID12	'0'
13	Device ID Number [13]	DID13	'0'
14	Device ID Number [14]	DID14	'0'
15	Device ID Number [15]	DID15	'0'

Bit	Description
15:0	**V3-LS Device ID Number [15:0]:** If Register 90H bit 2, SCS2 = '1', then the reset state is 0002H; if '0', then the reset state is 8002H. **NOTE:** These bits apply to Revision BB silicon and beyond.

14.10.3 Command Register (COMMD)

Index: 04H

Bit	Description	Name	Reset State
0	I/O Space Enable	IO_SPACE	'1'
1	Memory Space Enable	MEM_SPACE_EN	'1'
2	Bus Master Enable	BUS_MSTR_EN	'1'
3	Special Cycle Response	SPECIAL_CYCLE	'1'
4	Memory Write and Invalid Command Enable	MEMWR_INVCMD	'0'
5	VGA Palette Snoop Enable	PALETSNOOP	'0'
6	Parity Error Response	PAR_ERR_RESP	'0'
7	Address and Data Stepping Enable	ADD_DTA_STEP	'0'
8	SERR# Enable	SERR_EN	'0'
9	Fast Back-to-Back Cycle Enable	FAST_B2B_EN	'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**I/O Space Enable:** This bit is read only.
1	**Memory Space Enable:** This bit is read only.
2	**Bus Master Enable:** This bit is read only.
3	**Special Cycle Response:** This bit is read only.
4	**Memory Write and Invalid Command Enable:** This bit is read only
5	**VGA Palette Snoop Enable:** This bit is read only.
6	**Parity Error Response:** This bit is read-only.
7	**Address and Data Stepping Enable:** This bit is read only.
8	**SERR# Enable:** This bit is read-only.
9	**Fast Back-to-Back Cycle Enable When V3-LS is Bus Master:** This bit is read only.
15:10	Reserved

14.10.4 Status Register (STAT)

Index: 06H

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Reserved		'0'
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Fast Back-to Back Capable	FAST_B2B_CA	'0'
8	Data Parity	DATA_PARITY	'0'
9	DEVSEL Timing [0]	DEVT0	'1'
10	DEVSEL Timing [1]	DEVT1	'0'
11	Signaled Target Abort Flag	STA	'0'
12	Received Target Abort Flag	RAT	'0'
13	Signaled Master Abort Flag	SMA	'0'
14	Signaled SERR# Flag	SERRS	'0'
15	Signaled PERR# Flag	PERRS	'0'

Bit	Description
6:0	Reserved
7	**Fast Back-to-Back Capable:** This bit is read only. V3-LS does not support fast back-to-back cycle response.
8	**Data Parity:** This bit is read only.
10:9	**DEVSEL Timing [1:0]:** This bit is read only. If positive decoding occurs, V3-LS always uses medium DEVSEL timing.
11	**Signaled Target Abort Flag** : This bit is hard-wired to '0'.
12	**Received Target Abort Flag** : Writing '1' to this bit clears the flag
13	**Signaled Master Abort Flag** : This bit is hard-wired to '0'.
14	**Signaled SERR# Flag** : This bit is hard-wired to '0' and is read only. V3-LS will not assert SERR#.
15	**Signaled PERR# Flag** : This bit is hard-wired to '0' and is read only. V3-LS will not assert PERR#.

14.10.5 Revision ID Register 2 (REV_ID2)

Index: 08H

Bit	Description	Name	Reset State
0	Revision ID Number	RID	'0'
1	Revision ID Number	RID	'0'
2	Revision ID Number	RID	'0'
3	Revision ID Number	RID	'0'
4	Revision ID Number	RID	'0'
5	Revision ID Number	RID	'0'
6	Revision ID Number	RID	'0'
7	Revision ID Number	RID	'0'

Bit	Description
7:0	**Revision ID Number:** These bits indicate the revision of V3-LS and are hard-wired to 00H.

14.10.6 Class Code Register (CLASS)

Index: 09H

Bit	Description	Name	Reset State
0	Class Code [0]	CCD0	'0'
1	Class Code [1]	CCD1	'0'
2	Class Code [2]	CCD2	'0'
3	Class Code [3]	CCD3	'0'
4	Class Code [4]	CCD4	'0'
5	Class Code [5]	CCD5	'0'
6	Class Code [6]	CCD6	'0'
7	Class Code [7]	CCD7	'0'
8	Class Code [8]	CCD8	'0'
9	Class Code [9]	CCD9	'0'
10	Class Code [10]	CCD10	'0'
11	Class Code [11]	CCD11	'0'
12	Class Code [12]	CCD12	'0'
13	Class Code [13]	CCD13	'0'
14	Class Code [14]	CCD14	'0'
15	Class Code [15]	CCD15	'1'
16	Class Code [16]	CCD16	'0'
17	Class Code [17]	CCD17	'1'
18	Class Code [18]	CCD18	'1'
19	Class Code [19]	CCD19	'0'
20	Class Code [20]	CCD20	'0'
21	Class Code [21]	CCD21	'0'
22	Class Code [22]	CCD22	'0'
23	Class Code [23]	CCD23	'0'

Bit	Description
23:0	**Class Code:** If Register 90H bit 2, SCS2 = '1', then the reset state is 068000H; if '0', then the reset state is 060100H. **NOTE:** These bits apply to Revision BB silicon and beyond.

14.11 PCI-DMA Configuration Registers

14.11.1 Distributed DMA Control Register (DDMA_CTRL)

Index: 40H

Bit	Description	Name	Reset State
0	Distributed DMA Function Enable	DDMA_EN	'0'
1	Distributed DMA Mode	DDMA_MODE	'0'
2	Slave HD Distributed Access Enable	SLAVE_HD	'0'
3	Slave Floppy Distributed Access Enable	SLAVE_FLP	'0'
4	Sec. Slave HD Distributed Access Enable	SEC_SLAVE_HD	'0'
5	Sec. Slave Floppy Distributed Access Enable	SEC_SLAVE_FLP	'0'
6	Reserved		'0'
7	Reserved		'0'
8	Reserved		'0'
9	Reserved		'0'
10	Reserved		'0'
11	Reserved		'0'
12	Reserved		'0'
13	Reserved		'0'
14	Reserved		'0'
15	Reserved		'0'

Bit	Description
0	**Distributed DMA Function Enable:** '1' = enabled; '0' = disabled.
1	**Distributed DMA Mode:** If this bit is set to '0', it indicates master mode; when set to '1', it indicates slave mode. This bit is purely a BIOS function.
2	**Slave Hard Drive Port (3F7) Distributed Access Enable:** This bit is valid only when DDMA_MODE, bit 1 above, is set to master mode. A '0' indicates that the hard drive port is inside the notebook; a '1' indicates that hard disk port is inside the docking station. For more information, please refer to the 3F7H Application Note.
3	**Slave Floppy Drive Port (3F7) Distributed Access Enable:** This bit is valid only when DDMA_MODE, bit 1 above, is set to master mode. A '0' indicates the floppy drive port is inside the notebook; a '1' indicates that the floppy drive port is inside the docking station.
4	**Secondary Slave Hard Disk Distributed Access Enable:** This bit is only valid in master mode. '1' = secondary HD port (377) in secondary ISA; '0' = in primary ISA. **NOTE:** This bit applies to revision BB silicon and beyond.

Bit	Description *(cont.)*
5	**Secondary Slave Hard Disk Distributed Access Enable:** This bit is only valid in master mode. '1' = secondary floppy port (377) is in secondary ISA; '0' = secondary floppy port is in primary ISA. **NOTE:** This bit applies to revision BB silicon and beyond.
15:6	Reserved

14.11.2 Distributed DMA Status Register (DDMA_STAT)

Index: 42H

Bit	Description	Name	Reset State
0	DDMA Status	DDMA_BUSY	'0'
1	Reserved		'0'
2	Reserved		'0'
3	Reserved		'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'

Bit	Description
0	**DDMA Status:** The Distributed DMA controller sets this bit to '1' when the V3-LS device has not finished accessing the Distributed DMA channel. Writing a '1' clears this bit.
7:1	Reserved

14.11.3 Slave DMAC CH0 Base Register (DDMA_CH0)

Index: 44H

Bit	Description	Name	Reset State
0	Channel 0 Enable	CH0EN	'0'
1	Size [0]	SIZE0	'0'
2	Size [1]	SIZE1	'0'
3	Extended Address	EXTADD	'0'
4	Channel 0 Base Address [4]	CH0BASE4	'0'
5	Channel 0 Base Address [5]	CH0BASE5	'0'
6	Channel 0 Base Address [6]	CH0BASE6	'0'
7	Channel 0 Base Address [7]	CH0BASE7	'0'
8	Channel 0 Base Address [8]	CH0BASE8	'0'
9	Channel 0 Base Address [9]	CH0BASE9	'0'
10	Channel 0 Base Address [10]	CH0BASE10	'0'
11	Channel 0 Base Address [11]	CH0BASE11	'0'
12	Channel 0 Base Address [12]	CH0BASE12	'0'
13	Channel 0 Base Address [13]	CH0BASE13	'0'
14	Channel 0 Base Address [14]	CH0BASE14	'0'
15	Channel 0 Base Address [15]	CH0BASE15	'0'
31:16	Reserved		'0'

Bit	Description
0	**Channel 0 Enable:** '0' = disabled; '1' = enabled.
2:1	**Size [1:0]:** These bits are in 8-bit mode and are hardwired to '00'.
3	**Extended Address:** Hard-wired to '0'.
6:4	**Channel 0 Base Address [6:4]:** Hardwired to '0'.
15:7	**Channel 0 Base Address [15:7]:** This defines the base address of a block of I/O addresses (128-byte) for the Master DDMA controller to access the DMA channels distributed on the PCI or Secondary ISA buses.
31:16	Reserved: These bits are hard-wired to '0'.

14.11.4 Slave DMAC CH1 Base Register (DDMA_CH1)

Index: 48H

Bit	Description	Name	Reset State
0	Channel 1 Enable	CH1EN	'0'
1	Size [0]	SIZE0	'0'
2	Size [1]	SIZE1	'0'
3	Extended Address	EXTADD	'0'
4	Channel 1 Base Address [4]	CH1BASE4	'1'
5	Channel 1 Base Address [5]	CH1BASE5	'0'
6	Channel 1 Base Address [6]	CH1BASE6	'0'
7	Channel 1 Base Address [7]	CH1BASE7	'0'
8	Channel 1 Base Address [8]	CH1BASE8	'0'
9	Channel 1 Base Address [9]	CH1BASE9	'0'
10	Channel 1 Base Address [10]	CH1BASE10	'0'
11	Channel 1 Base Address [11]	CH1BASE11	'0'
12	Channel 1 Base Address [12]	CH1BASE12	'0'
13	Channel 1 Base Address [13]	CH1BASE13	'0'
14	Channel 1 Base Address [14]	CH1BASE14	'0'
15	Channel 1 Base Address [15]	CH1BASE15	'0'
31:16	Reserved		'0'

Bit	Description
0	**Channel 1 Enable:** '0' = disabled; '1' = enabled.
2:1	**Size [1:0]:** These bits are in 8-bit mode and are hardwired to '00'.
3	**Extended Address:** Hard-wired to '0'.
6:4	**Channel 1 Base Address [6:4]:** Hardwired to CH0BASE+001H.
15:7	**Channel 1 Base Address [15:7]:** This defines the base address of a block of I/O addresses (128-byte) for the Master DDMA controller to access the DMA channels distributed on the PCI or Secondary ISA buses.
31:16	Reserved: These bits are hardwired to '0'.

14.11.5 Slave DMAC CH2 Base Register (DDMA_CH2)

Index: 4CH

Bit	Description	Name	Reset State
0	Channel 2 Enable	CH2EN	'0'
1	Size [0]	SIZE0	'0'
2	Size [1]	SIZE1	'0'
3	Extended Address	EXTADD	'0'
4	Channel 2 Base Address [4]	CH2BASE4	'0'
5	Channel 2 Base Address [5]	CH2BASE5	'1'
6	Channel 2 Base Address [6]	CH2BASE6	'0'
7	Channel 2 Base Address [7]	CH2BASE7	'0'
8	Channel 2 Base Address [8]	CH2BASE8	'0'
9	Channel 2 Base Address [9]	CH2BASE9	'0'
10	Channel 2 Base Address [10]	CH2BASE10	'0'
11	Channel 2 Base Address [11]	CH2BASE11	'0'
12	Channel 2 Base Address [12]	CH2BASE12	'0'
13	Channel 2 Base Address [13]	CH2BASE13	'0'
14	Channel 2 Base Address [14]	CH2BASE14	'0'
15	Channel 2 Base Address [15]	CH2BASE15	'0'
31:16	Reserved		'0'

Bit	Description
0	**Channel 2 Enable:** '0' = disabled; '1' = enabled.
2:1	**Size [1:0]:** These bits are in 8-bit mode and are hardwired to '00'.
3	**Extended Address:** Hard-wired to '0'.
6:4	**Channel 2 Base Address [6:4]:** Hardwired to CH0BASE+002H.
15:7	**Channel 2 Base Address [15:7]:** This defines the base address of a block of I/O addresses (128-byte) for the Master DDMA controller to access the DMA channels distributed on the PCI or Secondary ISA buses.
31:16	Reserved: These bits are hardwired to '0'.

14.11.6 Slave DMAC CH3 Base Register (DDMA_CH3)

Index: 50H

Bit	Description	Name	Reset State
0	Channel 3 Enable	CH3EN	'0'
1	Size [0]	SIZE0	'0'
2	Size [1]	SIZE1	'0'
3	Extended Address	EXTADD	'0'
4	Channel 3 Base Address [4]	CH3BASE4	'1'
5	Channel 3 Base Address [5]	CH3BASE5	'1'
6	Channel 3 Base Address [6]	CH3BASE6	'0'
7	Channel 3 Base Address [7]	CH3BASE7	'0'
8	Channel 3 Base Address [8]	CH3BASE8	'0'
9	Channel 3 Base Address [9]	CH3BASE9	'0'
10	Channel 3 Base Address [10]	CH3BASE10	'0'
11	Channel 3 Base Address [11]	CH3BASE11	'0'
12	Channel 3 Base Address [12]	CH3BASE12	'0'
13	Channel 3 Base Address [13]	CH3BASE13	'0'
14	Channel 3 Base Address [14]	CH3BASE14	'0'
15	Channel 3 Base Address [15]	CH3BASE15	'0'
31:16	Reserved		'0'

Bit	Description
0	**Channel 3 Enable:** '0' = disabled; '1' = enabled.
2:1	**Size [1:0]:** These bits are in 8-bit mode and are hardwired to '00'.
3	**Extended Address:** Hard-wired to '0'.
6:4	**Channel 3 Base Address [6:4]:** Hardwired to CH0BASE+003.
15:7	**Channel 3 Base Address [15:7]:** This defines the base address of a block of I/O addresses (128-byte) for the Master DDMA controller to access the DMA channels distributed on the PCI or Secondary ISA buses.
31:16	Reserved: These bits are hardwired to '0'.

14.11.7 Slave DMAC CH5 Base Register (DDMA_CH5)

Index: 54H

Bit	Description	Name	Reset State
0	Channel 5 Enable	CH5EN	'0'
1	Size [0]	SIZE0	'1'
2	Size [1]	SIZE1	'0'
3	Extended Address	EXTADD	'0'
4	Channel 5 Base Address [4]	CH5BASE4	'1'
5	Channel 5 Base Address [5]	CH5BASE5	'0'
6	Channel 5 Base Address [6]	CH5BASE6	'1'
7	Channel 5 Base Address [7]	CH5BASE7	'0'
8	Channel 5 Base Address [8]	CH5BASE8	'0'
9	Channel 5 Base Address [9]	CH5BASE9	'0'
10	Channel 5 Base Address [10]	CH5BASE10	'0'
11	Channel 5 Base Address [11]	CH5BASE11	'0'
12	Channel 5 Base Address [12]	CH5BASE12	'0'
13	Channel 5 Base Address [13]	CH5BASE13	'0'
14	Channel 5 Base Address [14]	CH5BASE14	'0'
15	Channel 5 Base Address [15]	CH5BASE15	'0'
31:16	Reserved		'0'

Bit	Description
0	**Channel 5 Enable:** '0' = disabled; '1' = enabled.
2:1	**Size [1:0]:** These bits are in 16-bit mode and are hardwired to '01'.
3	**Extended Address:** Hard-wired to '0'.
6:4	**Channel 5 Base Address [6:4]:** Hardwired to CH0BASE+005.
15:7	**Channel 5 Base Address [15:7]:** This defines the base address of a block of I/O addresses (128-byte) for the Master DDMA controller to access the DMA channels distributed on the PCI or Secondary ISA buses.
31:16	Reserved: These bits are hardwired to '0'.

14.11.8 Slave DMAC CH6 Base Register (DDMA_CH6)

Index: 58H

Bit	Description	Name	Reset State
0	Channel 6 Enable	CH6EN	'0'
1	Size [0]	SIZE0	'1'
2	Size [1]	SIZE1	'0'
3	Extended Address	EXTADD	'0'
4	Channel 6 Base Address [4]	CH6BASE4	'0'
5	Channel 6 Base Address [5]	CH6BASE5	'1'
6	Channel 6 Base Address [6]	CH6BASE6	'1'
7	Channel 6 Base Address [7]	CH6BASE7	'0'
8	Channel 6 Base Address [8]	CH6BASE8	'0'
9	Channel 6 Base Address [9]	CH6BASE9	'0'
10	Channel 6 Base Address [10]	CH6BASE10	'0'
11	Channel 6 Base Address [11]	CH6BASE11	'0'
12	Channel 6 Base Address [12]	CH6BASE12	'0'
13	Channel 6 Base Address [13]	CH6BASE13	'0'
14	Channel 6 Base Address [14]	CH6BASE14	'0'
15	Channel 6 Base Address [15]	CH6BASE15	'0'
31:16	Reserved		'0'

Bit	Description
0	**Channel 6 Enable:** '0' = disabled; '1' = enabled.
2:1	**Size [1:0]:** These bits are in 16-bit mode and are hardwired to '01'.
3	**Extended Address:** Hard-wired to '0'.
6:4	**Channel 6 Base Address [6:4]:** Hardwired to CH0BASE+006.
15:7	**Channel 6 Base Address [15:7]:** This defines the base address of a block of I/O addresses (128-byte) for the Master DDMA controller to access the DMA channels distributed on the PCI or Secondary ISA buses.
31:16	Reserved: These bits are hardwired to '0'.

14.11.9 Slave DMAC CH7 Base Register (DDMA_CH7)

Index: 5CH

Bit	Description	Name	Reset State
0	Channel 7 Enable	CH7EN	'0'
1	Size [0]	SIZE0	'1'
2	Size [1]	SIZE1	'0'
3	Extended Address	EXTADD	'0'
4	Channel 7 Base Address [4]	CH7BASE4	'1'
5	Channel 7 Base Address [5]	CH7BASE5	'1'
6	Channel 7 Base Address [6]	CH7BASE6	'1'
7	Channel 7 Base Address [7]	CH7BASE7	'0'
8	Channel 7 Base Address [8]	CH7BASE8	'0'
9	Channel 7 Base Address [9]	CH7BASE9	'0'
10	Channel 7 Base Address [10]	CH7BASE10	'0'
11	Channel 7 Base Address [11]	CH7BASE11	'0'
12	Channel 7 Base Address [12]	CH7BASE12	'0'
13	Channel 7 Base Address [13]	CH7BASE13	'0'
14	Channel 7 Base Address [14]	CH7BASE14	'0'
15	Channel 7 Base Address [15]	CH7BASE15	'0'
31:16	Reserved		'0'

Bit	Description
0	**Channel 7 Enable:** '0' = disabled; '1' = enabled.
2:1	**Size [1:0]:** These bits are in 16-bit mode and are hard-wired to '01'.
3	**Extended 7 Address:** Hardwired to '0'.
6:4	**Channel 7 Base Address [6:4]:** Hardwired to CH0BASE +007
15:7	**Channel 7 Base Address [15: 7]:** This defines the base address of a block of I/O addresses (128-byte) for the Master DDMA controller to access the DMA channels distributed on the PCI or Secondary ISA buses.
31:16	Reserved: These bits are hardwired to '0'.

14.11.10 PCI-to-ISA Bridge Configuration Register (ISA_BCR)

Index: 90H

Bit	Description	Name	Reset State
0	System Configuration Setting [0]	SCS0	X
1	System Configuration Setting [1]	SCS1	X
2	System Configuration Setting [2]	SCS2	X
3	Reserved		X
4	Enable PERR# to Trigger NMI	PERRNMIEN	'0'
5	Enable SERR# to Trigger NMI	SERRNMIEN	'0'
6	PERR#/NMI Status Flag	PERRNMI	'0'
7	SERR#/NMI Status Flag	SERRNMI	'0'
8	LOCK# Input Enable	LOCKEN	'0'
9	Retry Enable	RETRYEN	'0'
10	Reserved		'0'
11	Reserved		'0'
12	ISA Bridge PCI Subtractive Decode Disable	PCI_SUB_DIS	SCS0
13	ISA Bridge PCI Positive Decode Enable	PCI_POS_EN	'0'
14	AD/SD/SA Bus Staggering Enable	AD_STAGEN	'0'
15	Reserved		'0'
16	Reserved		'0'
31:17	Reserved		'0'

Bit	Description
2:0	**System Configuration Setting [3:0]:** V3-LS can sample strapping information from pins on the rising edge of PCIRST# for power-on system configuration. Strobed in from V3-LS's pin at the end of PCI reset cycle. **NOTE:** See POWER-ON functional description for detail. These bits apply to Revision BB silicon and beyond.
3	Reserved
4	**Enable PERR# to Trigger NMI:** '1' = enabled; '0' = disabled.
5	**Enable SERR# to Trigger NMI:** '1' = enabled; '0' = disabled.
6	**PERR#/NMI Status Flag:** This bit indicates that PERR# has triggered NMI. Writing a '1' will clear this bit.
7	**SERR#/NMI Status Flag:** This bit indicates that SERR# has triggered NMI. Writing a '1' will clear this bit.
8	**Lock Input Enable:** Writing '0' to this bit will break the ISA/IDE lock condition.
9	**Retry Enable**: When set high, this bit will enable V3-LS to retry DMA/ISA master access while receiving Retry-Disconnect on the PCI bus.

Bit	Description *(cont.)*
10	Reserved
11	Reserved
12	**ISA Bridge PCI Subtractive Decode Disable:** Writing a '1' to this bit disables V3-LS subtractive decoding. The default value for this bit is derived from SCS[0].
13	**ISA Bridge PCI Positive Decode Enable:** '0' = disabled; '1' = enabled.
14	**AD/SD/SA Bus Staggering Enable:** '0' = disable AD/SD/SA bus staggering; '1' = enable AD/SD/SA bus staggering.
31:15	Reserved

14.11.11 ISA Memory Address Positive Decode (ISAMEM_PDECODE)

Index: 94H

Bit	Description	Name	Reset State
0	ISA Memory [F0000:FFFFF] Decode Enable	MEM_0F0000	'0'
1	ISA Memory [E8000:EFFFF] Decode Enable	MEM_0E8000	'0'
2	ISA Memory [E0000:E7FFF] Decode Enable	MEM_0E0000	'0'
3	ISA Memory [D8000:DFFFF] Decode Enable	MEM_0D8000	'0'
4	ISA Memory [D0000:D7FFF] Decode Enable	MEM_0D0000	'0'
5	ISA Memory [C8000:CFFFF] Decode Enable	MEM_0C8000	'0'
6	ISA Memory [C0000:C7FFF] Decode Enable	MEM_0C0000	'0'
7	ISA Memory [B0000:BFFFF] Decode Enable	MEM_0B0000	'0'
8	ISA Memory [A0000:AFFFF] Decode Enable	MEM_0A0000	'0'
31:9	Reserved		'0'

Bit	Description
0	**ISA Memory [F0000:FFFFF] Decode Enable:** '0' = Enable both 000F0000-000FFFFF and FFF0000-FFFFFFFF ranges.
1	**ISA Memory [E8000:EFFFF] Decode Enable:** '0' = Enable both 000E8000-000EFFFF and FFE8000-FFFEFFFF ranges.
2	**ISA Memory [E0000:E7FFF] Decode Enable:** '0' = Enable both 000E0000-000E7FFF and FFE0000-FFFE7FFF ranges.
3	**ISA Memory [D8000:DFFFF] Decode Enable:** '0' = Enable both 000D8000-000DFFFF and FFD8000-FFFDFFFF ranges.
4	**ISA Memory [D0000:D7FFF] Decode Enable:** '0' = Enable both 000D0000-000D7FFF and FFD0000-FFFD7FFF ranges.
5	**ISA Memory [C8000:CFFFF] Decode Enable:** '0' = Enable both 000C8000-000CFFFF and FFC8000-FFFCFFFF ranges.
6	**ISA Memory [C0000:C7FFF] Decode Enable:** '0' = Enable both 000C0000-000C7FFF and FFC0000-FFFC7FFF ranges.
7	**ISA Memory [B0000:BFFFF] Decode Enable:** '0' = Enable both 000B0000-000BFFFF and FFB0000-FFBFFFFF ranges.
8	**ISA Memory [A0000:AFFFF] Decode Enable:** '0' = Enable both 000A0000-000AFFFF and FFA0000-FFAFFFFF ranges.
31:9	Reserved

14.11.12 ISA I/O Address Positive Decoder (ISAIO_PDECODE)

Index: 98H

Bit	Description	Name	Reset State
0	Reserved		'0'
1	Reserved		'0'
2	Configuration (24/26H) Decode Enable	CONFIG	'0'
3	ISA System I/O	SYSIO	'0'
4	ISA COM-1 Decode Enable	COM1	'0'
5	ISA COM-2 Decode Enable	COM2	'0'
6	ISA COM-3 Decode Enable	COM3	'0'
7	ISA COM-4 Decode Enable	COM4	'0'
8	ISA LPT-1 Decode Enable	LPT1	'0'
9	ISA LPT-2 Decode Enable	LPT2	'0'
10	ISA LPT-3 Decode Enable	LPT3	'0'
11	ISA Primary IDE Decode Enable	HD1	'0'
12	ISA Secondary IDE Decode Enable	HD2	'0'
13	ISA Primary Floppy Decode Enable	FD1	'0'
14	ISA Secondary Floppy Decode Enable	FD2	'0'
15	Audio-0 Decode Enable	AUD0	'0'
16	Audio-1 Decode Enable	AUD1	'0'
17	Audio-2 Decode Enable	AUD2	'0'
18	Audio-3 Decode Enable	AUD3	'0'
19	Audio-4 Decode Enable	AUD4	'0'
20	Audio-5 Decode Enable	AUD5	'0'
21	PC NET	PC_NET	'0'
22	I/O Read 03F7	3F7READ	'0'
23	I/O Read 0377	377READ	'0'
31:24	Reserved		'0'

Bit	Description
0	Reserved
1	Reserved
2	**Configuration (24/26H) Decode Enable:** Address: 24, 26 - 8-bit cycle only.
3	**ISA System I/O:** Address: [00:FF], except 24 and 26.
4	**ISA COM-1 Decode Enable:** Address: 03F8:03FF
5	**ISA COM-2 Decode Enable:** Address: 02F8:02FF
6	**ISA COM-3 Decode Enable:** Address: 03E8:03EF
7	**ISA COM-4 Decode Enable:** Address: 02E8:02EF

Bit	Description *(cont.)*
8	**ISA LPT-1 Decode Enable:** Address: 0378:037F, 0778:077A
9	**ISA LPT-2 Decode Enable:** Address: 0278:027F, 678:67A
10	**ISA LPT-3 Decode Enable:** Address: 03BC:03BF, 7BC:7BE
11	**ISA Primary IDE Decode Enable:** Address: 01F0:01F7, 03F6 **NOTE:** This bit applies to revision BB silicon and beyond.
12	**ISA Secondary IDE Decode Enable:** Address: 0170:0177, 0376 **NOTE:** This bit applies to revision BB silicon and beyond.
13	**ISA Primary Floppy Decode Enable:** Address: 03F0: 03F5, 03F7(W) **NOTE:** This bit applies to revision BB silicon and beyond.
14	**ISA Secondary Floppy Decode Enable:** Address: 0370: 0375, 0377(W) **NOTE:** This bit applies to revision BB silicon and beyond.
15	**Audio-0 Decode Enable:** Address: 0201
16	**Audio-1 Decode Enable:** Address: 0220 – 022F
17	**Audio-2 Decode Enable:** Address: 0230 – 023F
18	**Audio-3 Decode Enable:** Address: 0240 – 024F
19	**Audio-4 Decode Enable:** Address: 0250 – 025F
20	**Audio-5 Decode Enable:** Address: 0388 – 038B
21	**PC NET:** Address: 0360:036F
22	**I/O Read 03F7** **NOTE:** This bit applies to revision BB silicon and beyond.
23	**I/O Read 0377** **NOTE:** This bit applies to revision BB silicon and beyond.
31:24	Reserved

14.11.13 I/O Configuration Address Register (IO_CNFG)

Index: 9CH

Bit	Description	Name	Reset State
0	Configuration Address Register Enable	CONFIGEN	'0'
1	Configuration Address Bit [0]	CFGA0	'0'
2	Configuration Address Bit [1]	CFGA1	'0'
3	Configuration Address Bit [2]	CFGA2	'0'
4	Configuration Address Bit [3]	CFGA3	'0'
5	Configuration Address Bit [4]	CFGA4	'0'
6	Configuration Address Bit [5]	CFGA5	'0'
7	Configuration Address Bit [6]	CFGA6	'0'
8	Configuration Address Bit [7]	CFGA7	'0'
9	Configuration Address Bit [8]	CFGA8	'0'
15:10	Reserved		'0'

Bit	Description
0	**Configuration Address Register Enable:** '0' = disabled; '1' = enabled.
9:1	**Configuration I/O Address Bits [8:0]:** These bits represent CPU address A[9:1].
15:10	Reserved

14.11.14 Programmable ISA I/O Address Decoder (ISAIO_DECODE)

Index: A0H

Bit	Description	Name	Reset State
0	ISA Range Decoder 1 Type	ISATYP1	'0'
1	ISA Range Decoder 1 Write Enable	ISAWREN1	'0'
2	ISA Range Decoder 1 Read Enable	ISARDEN1	'0'
3	ISA Range Decoder 2 Type	ISATYP2	'0'
4	ISA Range Decoder 2 Write Enable	ISAWREN2	'0'
5	ISA Range Decoder 2 Read Enable	ISARDEN2	'0'
6	ISA Range Decoder 3 Type	ISATYP3	'0'
7	ISA Range Decoder 3 Write Enable	ISAWREN3	'0'
8	ISA Range Decoder 3 Read Enable	ISARDEN3	'0'
9	ISA Range Decoder 4 Type	ISATYP4	'0'
10	ISA Range Decoder 4 Write Enable	ISAWREN4	'0'
11	ISA Range Decoder 4 Read Enable	ISARDEN4	'0'
12	ISA Range Decoder 5 Type	ISATYP5	'0'
13	ISA Range Decoder 5 Write Enable	ISAWREN5	'0'
14	ISA Range Decoder 5 Read Enable	ISARDEN5	'0'
15	ISA Range Decoder 6 Type	ISATYP6	'0'
16	ISA Range Decoder 6 Write Enable	ISAWREN6	'0'
17	ISA Range Decoder 6 Read Enable	ISARDEN6	'0'
31:18	Reserved		'0'

Bit	Description
0	**ISA Range Decoder 1 Type:** '0' = Memory; '1' = I/O.
1	**ISA Range Decoder 1 Write Enable:** '0' = disabled; '1' = enabled.
2	**ISA Range Decoder 1 Read Enable:** '0' = disabled; '1' = enabled.
3	**ISA Range Decoder 2 Type:** '0' = Memory; '1' = I/O.
4	**ISA Range Decoder 2 Write Enable:** '0' = disabled; '1' = enabled.
5	**ISA Range Decoder 2 Read Enable:** '0' = disabled; '1' = enabled.
6	**ISA Range Decoder 3 Type:** '0' = Memory; '1' = I/O.
7	**ISA Range Decoder 3 Write Enable:** '0' = disabled; '1' = enabled.
8	**ISA Range Decoder 3 Read Enable:** '0' = disabled; '1' = enabled.
9	**ISA Range Decoder 4 Type:** '0' = Memory; '1' = I/O.
10	**ISA Range Decoder 4 Write Enable:** '0' = disabled; '1' = enabled.

Bit	Description *(cont.)*
11	**ISA Range Decoder 4 Read Enable:** '0' = disabled; '1' = enabled.
12	**ISA Range Decoder 5 Type:** '0' = Memory; '1' = I/O.
13	**ISA Range Decoder 5 Write Enable:** '0' = disabled; '1' = enabled.
14	**ISA Range Decoder 5 Read Enable:** '0' = disabled; '1' = enabled.
15	**ISA Range Decoder 6 Type:** '0' = Memory; '1' = I/O.
16	**ISA Range Decoder 6 Write Enable:** '0' = disabled; '1' = enabled.
17	**ISA Range Decoder 6 Read Enable:** '0' = disabled; '1' = enabled.
31:18	Reserved

14.11.15 Programmable ISA Range Decoder Register 1 (ISAPR_DECODE1)

Index: A4H

Bit	Description	Name	Reset State
0	ISA Device Address [0]	ISA_A0	'0'
1	ISA Device Address [1]	ISA_A1	'0'
2	ISA Device Address [2]	ISA_A2	'0'
3	ISA Device Address [3]	ISA_A3	'0'
4	ISA Device Address [4]	ISA_A4	'0'
5	ISA Device Address [5]	ISA_A5	'0'
6	ISA Device Address [6]	ISA_A6	'0'
7	ISA Device Address [7]	ISA_A7	'0'
8	ISA Device Address [8]	ISA_A8	'0'
9	ISA Device Address [9]	ISA_A9	'0'
10	ISA Device Address [10]	ISA_A10	'0'
11	ISA Device Address [11]	ISA_A11	'0'
12	ISA Device Address [12]	ISA_A12	'0'
13	ISA Device Address [13]	ISA_A13	'0'
14	ISA Device Address [14]	ISA_A14	'0'
15	ISA Device Address [15]	ISA_A15	'0'
16	ISA Address Compare Enable [0]	ISA_CMP0	'0'
17	ISA Address Compare Enable [1]	ISA_CMP1	'0'
18	ISA Address Compare Enable [2]	ISA_CMP2	'0'
19	ISA Address Compare Enable [3]	ISA_CMP3	'0'
20	ISA Address Compare Enable [4]	ISA_CMP4	'0'
21	ISA Address Compare Enable [5]	ISA_CMP5	'0'
22	ISA Address Compare Enable [6]	ISA_CMP6	'0'
23	ISA Address Compare Enable [7]	ISA_CMP7	'0'
24	ISA Address Compare Enable [8]	ISA_CMP8	'0'
25	ISA Address Compare Enable [9]	ISA_CMP9	'0'
26	ISA Address Compare Enable [10]	ISA_CMP10	'0'
27	ISA Address Compare Enable [11]	ISA_CMP11	'0'
28	ISA Address Compare Enable [12]	ISA_CMP12	'0'
29	ISA Address Compare Enable [13]	ISA_CMP13	'0'
30	ISA Address Compare Enable [14]	ISA_CMP14	'0'
31	ISA Address Compare Enable [15]	ISA_CMP15	'0'

Bit	Description
15:0	**ISA Device Address [15:0]:** If the device type is an I/O, bit[15:0] = A[15:0]; if the device is memory, bit[15:0] = A[23:8].
31:16	**ISA Address Compare Enable [15:0]:**

14.11.16 Programmable ISA Range Decoder Register 2 (ISAPR_DECODE2)

Index: A8H

Bit	Description	Name	Reset State
0	ISA Device Address [0]	ISA_A0	'0'
1	ISA Device Address [1]	ISA_A1	'0'
2	ISA Device Address [2]	ISA_A2	'0'
3	ISA Device Address [3]	ISA_A3	'0'
4	ISA Device Address [4]	ISA_A4	'0'
5	ISA Device Address [5]	ISA_A5	'0'
6	ISA Device Address [6]	ISA_A6	'0'
7	ISA Device Address [7]	ISA_A7	'0'
8	ISA Device Address [8]	ISA_A8	'0'
9	ISA Device Address [9]	ISA_A9	'0'
10	ISA Device Address [10]	ISA_A10	'0'
11	ISA Device Address [11]	ISA_A11	'0'
12	ISA Device Address [12]	ISA_A12	'0'
13	ISA Device Address [13]	ISA_A13	'0'
14	ISA Device Address [14]	ISA_A14	'0'
15	ISA Device Address [15]	ISA_A15	'0'
16	ISA Address Compare Enable [0]	ISA_CMP0	'0'
17	ISA Address Compare Enable [1]	ISA_CMP1	'0'
18	ISA Address Compare Enable [2]	ISA_CMP2	'0'
19	ISA Address Compare Enable [3]	ISA_CMP3	'0'
20	ISA Address Compare Enable [4]	ISA_CMP4	'0'
21	ISA Address Compare Enable [5]	ISA_CMP5	'0'
22	ISA Address Compare Enable [6]	ISA_CMP6	'0'
23	ISA Address Compare Enable [7]	ISA_CMP7	'0'
24	ISA Address Compare Enable [8]	ISA_CMP8	'0'
25	ISA Address Compare Enable [9]	ISA_CMP9	'0'
26	ISA Address Compare Enable [10]	ISA_CMP10	'0'
27	ISA Address Compare Enable [11]	ISA_CMP11	'0'
28	ISA Address Compare Enable [12]	ISA_CMP12	'0'
29	ISA Address Compare Enable [13]	ISA_CMP13	'0'
30	ISA Address Compare Enable [14]	ISA_CMP14	'0'
31	ISA Address Compare Enable [15]	ISA_CMP15	'0'

Bit	Description
15:0	**ISA Device Address [15:0]:** If the device type is an I/O, bit[15:0] = A[15:0]; if the device is memory, bit[15:0] = A[23:8].
31:16	**ISA Address Compare Enable [15:0]:**

14.11.17 Programmable ISA Range Decoder Register 3 (ISAPR_DECODE3)

Index: ACH

Bit	Description	Name	Reset State
0	ISA Device Address [0]	ISA_A0	'0'
1	ISA Device Address [1]	ISA_A1	'0'
2	ISA Device Address [2]	ISA_A2	'0'
3	ISA Device Address [3]	ISA_A3	'0'
4	ISA Device Address [4]	ISA_A4	'0'
5	ISA Device Address [5]	ISA_A5	'0'
6	ISA Device Address [6]	ISA_A6	'0'
7	ISA Device Address [7]	ISA_A7	'0'
8	ISA Device Address [8]	ISA_A8	'0'
9	ISA Device Address [9]	ISA_A9	'0'
10	ISA Device Address [10]	ISA_A10	'0'
11	ISA Device Address [11]	ISA_A11	'0'
12	ISA Device Address [12]	ISA_A12	'0'
13	ISA Device Address [13]	ISA_A13	'0'
14	ISA Device Address [14]	ISA_A14	'0'
15	ISA Device Address [15]	ISA_A15	'0'
16	ISA Address Compare Enable [0]	ISA_CMP0	'0'
17	ISA Address Compare Enable [1]	ISA_CMP1	'0'
18	ISA Address Compare Enable [2]	ISA_CMP2	'0'
19	ISA Address Compare Enable [3]	ISA_CMP3	'0'
20	ISA Address Compare Enable [4]	ISA_CMP4	'0'
21	ISA Address Compare Enable [5]	ISA_CMP5	'0'
22	ISA Address Compare Enable [6]	ISA_CMP6	'0'
23	ISA Address Compare Enable [7]	ISA_CMP7	'0'
24	ISA Address Compare Enable [8]	ISA_CMP8	'0'
25	ISA Address Compare Enable [9]	ISA_CMP9	'0'
26	ISA Address Compare Enable [10]	ISA_CMP10	'0'
27	ISA Address Compare Enable [11]	ISA_CMP11	'0'
28	ISA Address Compare Enable [12]	ISA_CMP12	'0'
29	ISA Address Compare Enable [13]	ISA_CMP13	'0'
30	ISA Address Compare Enable [14]	ISA_CMP14	'0'
31	ISA Address Compare Enable [15]	ISA_CMP15	'0'

Bit	Description
15:0	**ISA Device Address [15:0]:** If the device type is an I/O, bit[15:0] = A[15:0]; if the device is memory, bit[15:0] = A[23:8].
31:16	**ISA Address Compare Enable [15:0]:**

14.11.18 Programmable ISA Range Decoder Register 4 (ISAPR_DECODE4)

Index: B0H

Bit	Description	Name	Reset State
0	ISA Device Address [0]	ISA_A0	'0'
1	ISA Device Address [1]	ISA_A1	'0'
2	ISA Device Address [2]	ISA_A2	'0'
3	ISA Device Address [3]	ISA_A3	'0'
4	ISA Device Address [4]	ISA_A4	'0'
5	ISA Device Address [5]	ISA_A5	'0'
6	ISA Device Address [6]	ISA_A6	'0'
7	ISA Device Address [7]	ISA_A7	'0'
8	ISA Device Address [8]	ISA_A8	'0'
9	ISA Device Address [9]	ISA_A9	'0'
10	ISA Device Address [10]	ISA_A10	'0'
11	ISA Device Address [11]	ISA_A11	'0'
12	ISA Device Address [12]	ISA_A12	'0'
13	ISA Device Address [13]	ISA_A13	'0'
14	ISA Device Address [14]	ISA_A14	'0'
15	ISA Device Address [15]	ISA_A15	'0'
16	ISA Address Compare Enable [0]	ISA_CMP0	'0'
17	ISA Address Compare Enable [1]	ISA_CMP1	'0'
18	ISA Address Compare Enable [2]	ISA_CMP2	'0'
19	ISA Address Compare Enable [3]	ISA_CMP3	'0'
20	ISA Address Compare Enable [4]	ISA_CMP4	'0'
21	ISA Address Compare Enable [5]	ISA_CMP5	'0'
22	ISA Address Compare Enable [6]	ISA_CMP6	'0'
23	ISA Address Compare Enable [7]	ISA_CMP7	'0'
24	ISA Address Compare Enable [8]	ISA_CMP8	'0'
25	ISA Address Compare Enable [9]	ISA_CMP9	'0'
26	ISA Address Compare Enable [10]	ISA_CMP10	'0'
27	ISA Address Compare Enable [11]	ISA_CMP11	'0'
28	ISA Address Compare Enable [12]	ISA_CMP12	'0'
29	ISA Address Compare Enable [13]	ISA_CMP13	'0'
30	ISA Address Compare Enable [14]	ISA_CMP14	'0'
31	ISA Address Compare Enable [15]	ISA_CMP15	'0'

Bit	Description
15:0	**ISA Device Address [15:0]:** If the device type is an I/O, bit[15:0] = A[15:0]; if the device is memory, bit[15:0] = A[23:8].
31:16	**ISA Address Compare Enable [15:0]:**

14.11.19 Programmable ISA Range Decoder Register 5 (ISAPR_DECODE5)

Index: B4H

Bit	Description	Name	Reset State
0	ISA Device Address [0]	ISA_A0	'0'
1	ISA Device Address [1]	ISA_A1	'0'
2	ISA Device Address [2]	ISA_A2	'0'
3	ISA Device Address [3]	ISA_A3	'0'
4	ISA Device Address [4]	ISA_A4	'0'
5	ISA Device Address [5]	ISA_A5	'0'
6	ISA Device Address [6]	ISA_A6	'0'
7	ISA Device Address [7]	ISA_A7	'0'
8	ISA Device Address [8]	ISA_A8	'0'
9	ISA Device Address [9]	ISA_A9	'0'
10	ISA Device Address [10]	ISA_A10	'0'
11	ISA Device Address [11]	ISA_A11	'0'
12	ISA Device Address [12]	ISA_A12	'0'
13	ISA Device Address [13]	ISA_A13	'0'
14	ISA Device Address [14]	ISA_A14	'0'
15	ISA Device Address [15]	ISA_A15	'0'
16	ISA Address Compare Enable [0]	ISA_CMP0	'0'
17	ISA Address Compare Enable [1]	ISA_CMP1	'0'
18	ISA Address Compare Enable [2]	ISA_CMP2	'0'
19	ISA Address Compare Enable [3]	ISA_CMP3	'0'
20	ISA Address Compare Enable [4]	ISA_CMP4	'0'
21	ISA Address Compare Enable [5]	ISA_CMP5	'0'
22	ISA Address Compare Enable [6]	ISA_CMP6	'0'
23	ISA Address Compare Enable [7]	ISA_CMP7	'0'
24	ISA Address Compare Enable [8]	ISA_CMP8	'0'
25	ISA Address Compare Enable [9]	ISA_CMP9	'0'
26	ISA Address Compare Enable [10]	ISA_CMP10	'0'
27	ISA Address Compare Enable [11]	ISA_CMP11	'0'
28	ISA Address Compare Enable [12]	ISA_CMP12	'0'
29	ISA Address Compare Enable [13]	ISA_CMP13	'0'
30	ISA Address Compare Enable [14]	ISA_CMP14	'0'
31	ISA Address Compare Enable [15]	ISA_CMP15	'0'

Bit	Description
15:0	**ISA Device Address [15:0]:** If the device type is an I/O, bit[15:0] = A[15:0]; if the device is memory, bit[15:0] = A[23:8].
31:16	**ISA Address Compare Enable [15:0]:**

14.11.20 Programmable ISA Range Decoder Register 6 (ISAPR_DECODE6)

Index: B8H

Bit	Description	Name	Reset State
0	ISA Device Address [0]	ISA_A0	'0'
1	ISA Device Address [1]	ISA_A1	'0'
2	ISA Device Address [2]	ISA_A2	'0'
3	ISA Device Address [3]	ISA_A3	'0'
4	ISA Device Address [4]	ISA_A4	'0'
5	ISA Device Address [5]	ISA_A5	'0'
6	ISA Device Address [6]	ISA_A6	'0'
7	ISA Device Address [7]	ISA_A7	'0'
8	ISA Device Address [8]	ISA_A8	'0'
9	ISA Device Address [9]	ISA_A9	'0'
10	ISA Device Address [10]	ISA_A10	'0'
11	ISA Device Address [11]	ISA_A11	'0'
12	ISA Device Address [12]	ISA_A12	'0'
13	ISA Device Address [13]	ISA_A13	'0'
14	ISA Device Address [14]	ISA_A14	'0'
15	ISA Device Address [15]	ISA_A15	'0'
16	ISA Address Compare Enable [0]	ISA_CMP0	'0'
17	ISA Address Compare Enable [1]	ISA_CMP1	'0'
18	ISA Address Compare Enable [2]	ISA_CMP2	'0'
19	ISA Address Compare Enable [3]	ISA_CMP3	'0'
20	ISA Address Compare Enable [4]	ISA_CMP4	'0'
21	ISA Address Compare Enable [5]	ISA_CMP5	'0'
22	ISA Address Compare Enable [6]	ISA_CMP6	'0'
23	ISA Address Compare Enable [7]	ISA_CMP7	'0'
24	ISA Address Compare Enable [8]	ISA_CMP8	'0'
25	ISA Address Compare Enable [9]	ISA_CMP9	'0'
26	ISA Address Compare Enable [10]	ISA_CMP10	'0'
27	ISA Address Compare Enable [11]	ISA_CMP11	'0'
28	ISA Address Compare Enable [12]	ISA_CMP12	'0'
29	ISA Address Compare Enable [13]	ISA_CMP13	'0'
30	ISA Address Compare Enable [14]	ISA_CMP14	'0'
31	ISA Address Compare Enable [15]	ISA_CMP15	'0'

Bit	Description
15:0	**ISA Device Address [15:0]:** If the device type is an I/O, bit[15:0] = A[15:0]; if the device is memory, bit[15:0] = A[23:8].
31:16	**ISA Address Compare Enable [15:0]:**

14.12 Standard AT Ports

Address	Name	Width
00-1F	DMAC-1	8-bit
20-3F	PIC-1	8-bit
40-5F	TIMER	8-bit
61	PORT B	8-bit
60,64	KEYBOARD	8-bit
70	CMOS INDEX and NMI ENABLE	8-bit
80-8F	DMA Page Register	8-bit
92	PORT 92	8-bit
A0-BF	PIC-2	8-bit
C0-DF	DMAC-2	8-bit
F0	COPROCESSOR	8-bit

These are IBM-AT standard registers. They are accessed through normal addressing scheme without indexing.

14.12.1 Port B

I/O Address 061H

Bit	Description	Name	Reset State
0	Timer 2 Enable	TMR2EN	'0'
1	Speaker Enable	SPKREN	'0'
2	Parity Disable	PARDIS	'0'
3	I/O Channel Check Disable	IOCHKDIS	'0'
4	Refresh Toggle	REFRTOGL	X
5	Timer 2 Output	TMR2OUT	X
6	I/O channel Check Error	IOCKERR	'0'
7	Parity Error	PARERR	'0'

Bit	Description
0	**Timer 2 Enable:** When high, Timer 2 in the 8254 will be enabled by making GATE input high. When low, it will be disabled. This bit is read/write-able.
1	**Speaker Enable:** When high, output of Timer 2 will be gated onto SPKR output. When low, the SPKR pin will be inactive. This bit is read/write-able.
2	**Parity Disable:** When high, parity check is disabled and inhibited from generating NMIs. When low, it is enabled. This bit is read/write-able.
3	**I/O Channel Check Disable:** When high, ISA signal IOCHK sampling is inhibited from generating NMIs. When low, NMI generation is enabled. This bit is read/write-able. **NOTE:** This bit applies to Revision BB silicon and beyond.
4	**Refresh Toggle:** This bit toggles on each AT refresh cycle. This bit is read only; writing to this bit has no effect.
5	**Timer 2 Output:** Reading this bit returns the status of Timer 2 output. This bit is read only. Writing to this bit has no effect.
6	**IO Channel Check Error:** When high, this bit indicates that an IOCHK error has occurred. When low, it indicates that no error has occurred.
7	**Parity Error:** When high, this bit indicates that a parity error has occurred. When low, it indicates that no error has occurred.

14.12.2 Port 70H

I/O Address 070H

Bit	Description	Name	Reset State
0	RTC Index	RTCINDX	X
1	RTC Index	RTCINDX	X
2	RTC Index	RTCINDX	X
3	RTC Index	RTCINDX	X
4	RTC Index	RTCINDX	X
5	RTC Index	RTCINDX	X
6	RTC Index	RTCINDX	X
7	NMI Mask	NMIDIS	X

Bit	Description
6:0	**RTC Index:** Writing these bits selects index value of RTC CMOS RAM. These seven bits are write-only and reside inside RTC chip. V3-LS will provide shadowing for these bits.
7	**NMI Mask:** When high, NMI output pin will be disabled.

14.12.3 Port 92H

I/O Address 092H

Bit	Description	Name	Reset State
0	Alternate Fast CPU Reset	FSTRST	'0'
1	Fast Gate A20	FGATEA20	'0'
2	Reserved		'0'
3	Security Lock 1	SLOCK1	'0'
4	Reserved		'0'
5	Reserved		'0'
6	Reserved		'0'
7	Reserved		'0'

Bit	Description
0	**Alternate Fast CPU Reset:** A low-to-high transition of this bit will trigger a CPU reset after 6.7 µs. Once set high, this bit will stay high until written low, but will not trigger reset again. This bit works in parallel with the keyboard controller reset and is read/write.
1	**Fast Gate A20:** When high, this bit has no effect on A20. When low, A20 will be forced low by asserting A20M# signal. This bit is read/write.
2	Reserved
3	**Security Lock 1:** When this bit is set high, RTC CMOS RAM index 38-3FH cannot be read or written. Once this bit is set high, it can only be cleared by the reset input of V3-GS device. SCLOCK1 function is disabled by default and is controlled by V3-GS register P92CNTL bit 1.
7:4	Reserved

15. V3-LS ELECTRICAL SPECIFICATIONS

15.1 Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 15-1. Maximum Ratings

Condition	Maximum Rating
Ambient temperature	0 - 70 ^{o}C
Storage temperature	-65 to +150 ^{o}C
Supply voltage to ground potential	3.0-V to 3.6-V (for 3-V design) 4.5-V to 5.5-V (for 5V design)
Applied output voltage	-0.3 to V_{DD} + 0.3
Applied input voltage	-0.3 to V_{DD} + 0.3
Operating power dissipation	1 W

15.2 DC Characteristics 5.0 Volt

Symbol	Parameter	MIN	MAX	Unit	Condition
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{DD}+0.5	V	
V_{OL}	Output Low Voltage	-	0.4	V	
V_{OH}	Output High Voltage	3.7	-	V	
I_L	Input Leakage Current		10	uA	
I_{OZ}	Tristate Leakage Current		10	uA	
C_{IN}	Input Capacitance		6	pF	Typical Value
C_{OUT}	Output capacitance		9	pF	Typical Value
I_{DD}	Power Supply Current		300	mA	

15.3 DC Characteristics 3.3 Volt

Symbol	Parameter	MIN	MAX	Unit	Condition
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{DD}+0.3	V	
V_{OL}	Output Low Voltage	-	0.2	V	
V_{OH}	Output High Voltage	2.4	-	V	
I_L	Input Leakage Current		10	uA	
I_{OZ}	Tristate Leakage Current		10	uA	
C_{IN}	Input Capacitance		6	pF	Typical Value
C_{OUT}	Output capacitance		9	pF	Typical Value
I_{DD}	Power Supply Current		300	mA	

15.4 AC Characteristics

Table 15-2. V3-LS AC Timing Parameters

Symbol	Parameter	Min	Max	Unit	Notes	Reference
ISA BUS TIMING						
t_{101}	BALE active from SYSCLK rising	8	24	ns		t_{val}
t_{102}	BALE inactive from SYSCLK rising	7	19	ns		t_{val}
t_{103}	MEMR# active from SYSCLK falling (8-bit)	5	13	ns		t_{val}
t_{104}	MEMR# inactive from SYSCLK rising (8-bit)	6	17	ns		t_{val}
t_{105}	SMEMR# active from SYSCLK falling (8-bit)	9	27	ns		t_{val}
t_{106}	SMEMR# inactive from SYSCLK rising (8-bit)	10	31	ns		t_{val}
t_{107}	MEMW# active from SYSCLK falling (8-bit)	5	13	ns		t_{val}
t_{108}	MEMW# inactive from SYSCLK rising (8-bit)	6	17	ns		t_{val}
t_{109}	SMEMW# active from SYSCLK falling (8-bit)	9	35	ns		t_{val}
t_{110}	SMEMW# inactive from SYSCLK rising (8-bit)	10	35	ns		t_{val}
t_{111}	MEMR# active from SYSCLK rising (16-bit)			ns		t_{val}
t_{112}	SMEMR# active from SYSCLK rising (16-bit)			ns		t_{val}
t_{113}	MEMW# active from SYSCLK rising (16-bit)			ns		t_{val}
t_{114}	SMEMW# active from SYSCLK rising (16-bit)			ns		t_{val}
t_{115}	IOR# active from SYSCLK falling	5	14	ns		t_{val}
t_{116}	IOR# inactive from SYSCLK rising	6	17	ns		t_{val}
t_{117}	IOW# active from SYSCLK falling	5	14	ns		t_{val}
t_{118}	IOW# inactive from SYSCLK rising	6	17	ns		t_{val}
t_{119}	ZWS# setup time to SYSCLK falling			ns		t_{su}
t_{120}	ZWS# hold time to SYSCLK falling			ns		t_{h}
t_{121}	IOCHRDY setup time to SYSCLK rising			ns		t_{su}
t_{122}	IOCHRDY hold time to SYSCLK rising	0		ns		t_{h}
t_{123}	SD write data setup time (MEMW cycle)			ns		t_{su}
t_{124}	SD write data hold time (MEMW cycle)	0		ns		t_{h}
t_{125}	SD write data setup time (IOW cycle)			ns		t_{su}
t_{126}	SD write data hold time (IOW cycle)	0		ns		t_{h}

Table 15-2. V3-LS AC Timing Parameters

Symbol	Parameter	Min	Max	Unit	Notes	Reference
t_{127}	MEM16# setup time to SYSCLK rising			ns		t_{su}
t_{128}	MEM16# hold time to SYSCLK rising	0		ns		t_h
t_{129}	IO16# setup time to SYSCLK rising			ns		t_{su}
t_{130}	IO16# hold time to SYSCLK rising	0		ns		t_h
t_{131}	16-bit memory command active time	2T		ns		t_{val}
t_{132}	16-bit I/O command active time	1.5T		ns		t_{val}
t_{133}	8-bit memory or I/O command active time	4.5T		ns		t_{val}
t_{134}	16-bit command off time	0.5T	3.5T	ns		t_{val}
t_{135}	8-bit command off time	0.5T	6.5T	ns		t_{val}
t_{136}	BALE falling to 8-bit command	0.5T		ns		t_{val}
t_{137}	BALE falling to 16-bit I/O command	0.5T		ns		t_{val}
t_{138}	BALE high period	0.5T		ns		t_{val}
t_{139}	SA hold time from command inactive			ns		t_h
t_{140}	SA[1:0] valid to BALE falling	0.5T		ns		t_{val}
REFRESH TIMING						
t_{201}	AEN active from SYSCLK	9	30	ns		t_{val}
t_{202}	AEN inactive from SYSCLK falling	11	33	ns		t_{val}
t_{203}	MEMR# active pulse width			ns		t_{val}
t_{204}	MEMR# active delay from SYSCLK rising	5	13	ns		t_{val}
t_{205}	MEMR# inactive delay from SYSCLK rising	5	15	ns		t_{val}
t_{206}	REFRESH# active pulse width			ns		t_{val}
t_{207}	REFRESH# active delay from SYSCLK rising			ns		t_{val}
t_{208}	REFRESH# inactive delay from SYSCLK rising	5	15	ns		t_{val}
t_{209}	IOCHRDY setup time to SYSCLK rising			ns		t_{su}
t_{210}	IOCHRDY hold time to SYSCLK rising			ns		t_h
DMA TIMING						
t_{301}	DACK# set up to IOR# command	1T		ns		t_{su}

Table 15-2. V3-LS AC Timing Parameters

Symbol	Parameter	Min	Max	Unit	Notes	Reference
t_{302}	DACK# setup to IOW# command	3T		ns		t_{su}
t_{303}	SA set up to command (MEMR#)	1T		ns		t_{su}
t_{304}	SA set up to command (MEMR#)	3T		ns		t_{su}
t_{305}	IOR# setup to MEMW#	2T		ns		t_{su}
t_{306}	MEMR# setup to IOW#	2T		ns		t_{su}
t_{307}	Read command hold time from write command inactive (MEMR#/IOR# rising edge)			ns		t_{val}
t_{308}	Adress hold time from command off	1T		ns		t_h
t_{309}	IOCHRDY from command	32	44	ns		
t_{310}	TC set up to command			ns		t_{su}
t_{311}	DACK# hold time from command off	1T	1T	ns		t_h
t_{312}	AEN hold from command off	7T	7T	ns		t_h
PCI TIMING						
t_{401}	FRAME# active from PCICLK			ns		t_{val}
t_{402}	FRAME# inactive from PCICLK	4	12	ns		t_{val}
t_{403}	IRDY# active from PCICLK			ns		t_{val}
t_{404}	IRDY# inactive from PCICLK	4	13	ns		t_{val}
t_{405}	TRDY# active from PCICLK	5	13	ns		t_{val}
t_{406}	TRDY# inactive from PCICLK	4	12	ns		t_{val}
t_{407}	DEVSEL# active from PCICLK			ns		t_{val}
t_{408}	DEVSEL# inactive from PCICLK	4	12	ns		t_{val}
t_{409}	STOP# active from PCICLK	5	13	ns		t_{val}
t_{410}	STOP# inactive from PCICLK	4	12	ns		t_{val}
BSER TIMING						
t_{501}	BSER3TO1 delay to BSERCLK	5	16	ns		t_{val}
t_{502}	BSER1TO3 set up to BSERCLK rising			ns		t_{su}

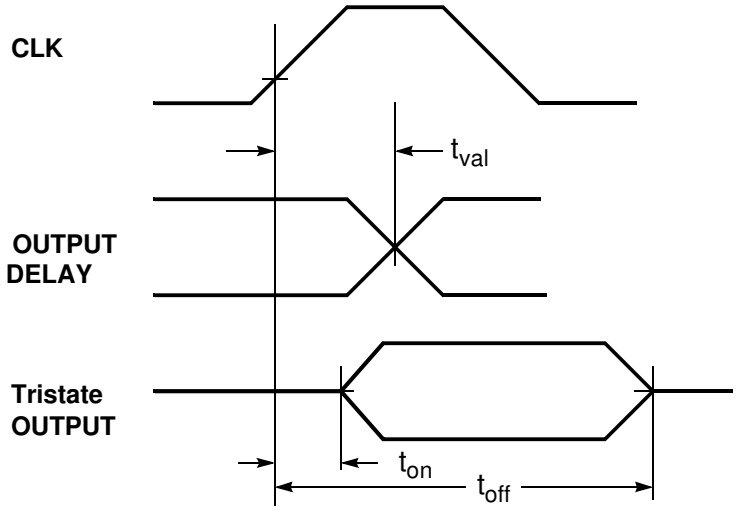


Figure 15-1. Output Timing Measurement Conditions

t_{val} – See 'Reference' column in Table 15-2

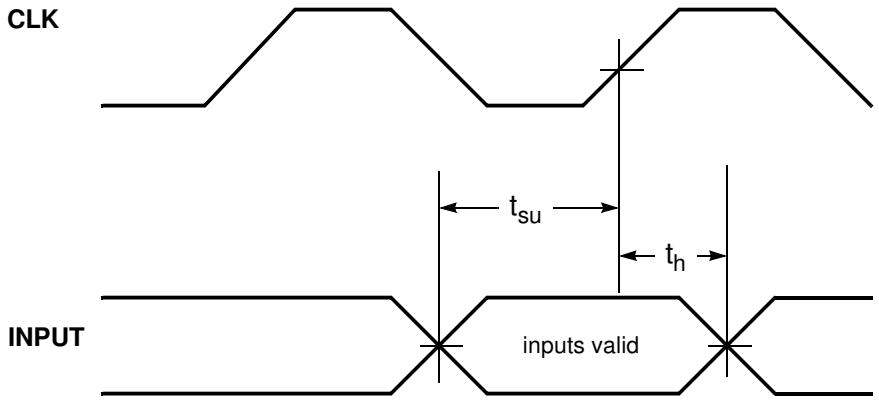


Figure 15-2. Input Timing Measurement Conditions

t_{su} – See 'Reference' column in Table 15-2

t_h – See 'Reference' column in Table 15-2

Appendices

Appendix A

Package Specifications

VESUVIUS-LS devices are available in a choice of flexible packaging alternatives. Please consult the following table for product packaging selection.

Device	Part No.	Pin Count	Package Type
V1-LS	PT86C521	208	VQFP[a]
		208	PQFP[b]
V2-LS	PT86C522	208	VQFP
		208	PQFP
V3-LS	PT86C523	176	VQFP
		208	PQFP

[a] very-tight-pitch quad flat pack
[b] plastic quad flat pack

Detailed package specifications for 208-pin VQFP, 208-pin PQFP, and 176-pin VQFP packages are shown on the following pages.

Refer to Appendix B for ordering information.

The following notes apply to the package diagrams in this section:

NOTES:
1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawings do not reflect exact package pin count.
3) Before beginning any new design with a device, please contact National Semiconductor for the latest package information.
4) Pin 1 identification may be either an ink dot or a dimple.
5) Ejector pin marks in molding are present on every package.
6) Package top dimensions can be smaller than bottom dimensions by 0.20 mm (0.008 in.)

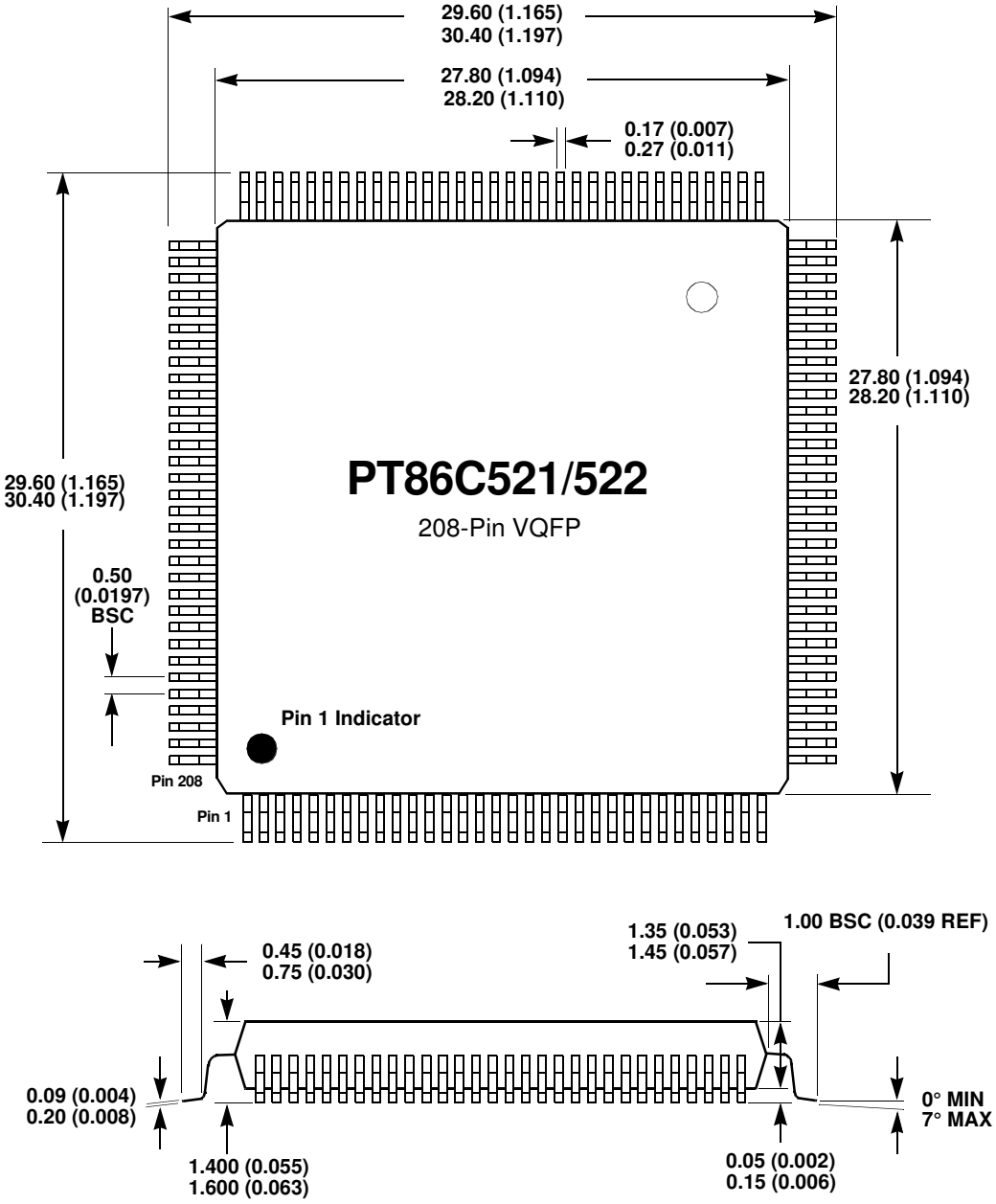


Figure A-1. 208-Pin VQFP Package Dimensions

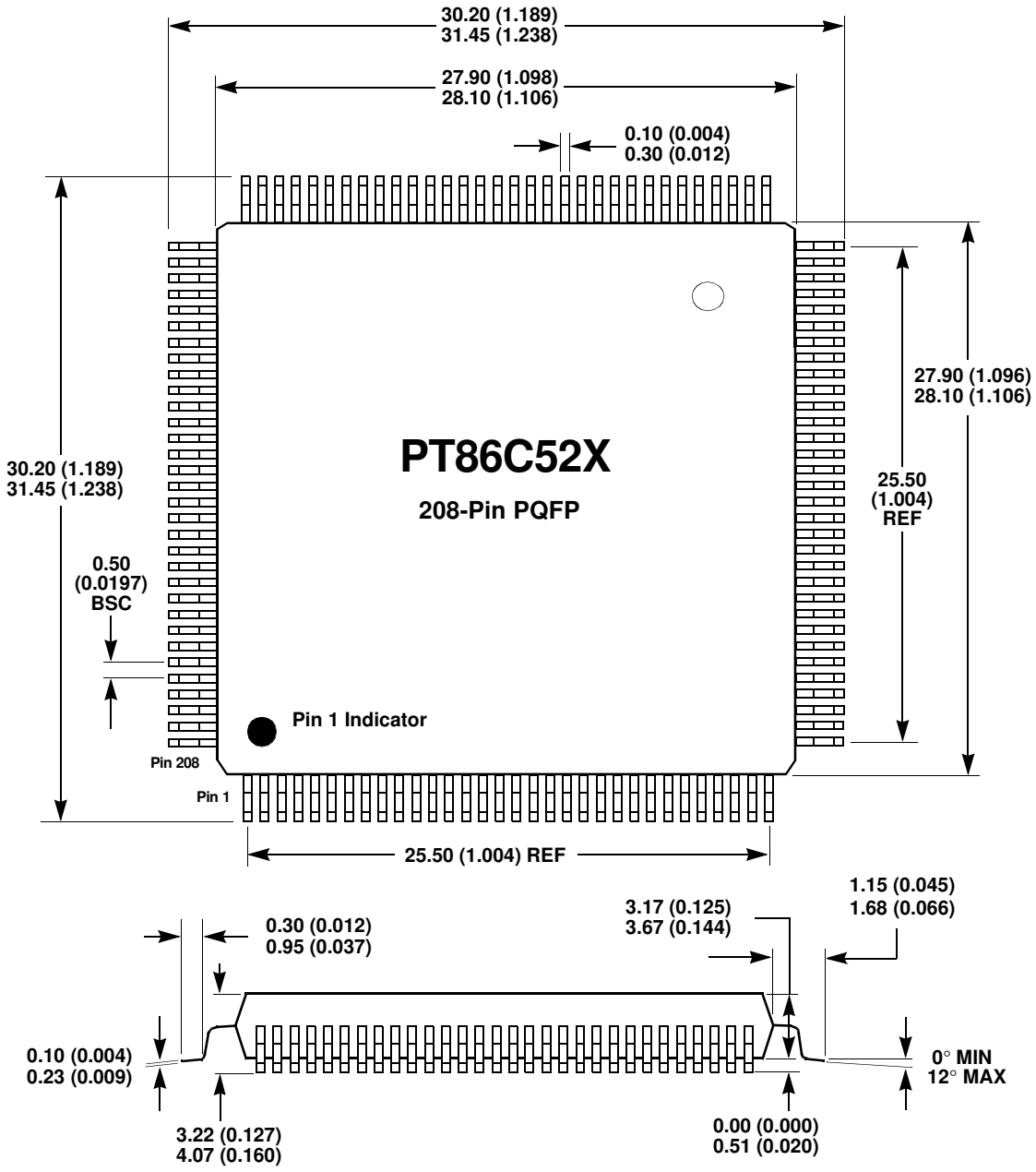


Figure A-2. 208-Pin PQFP Package Dimensions

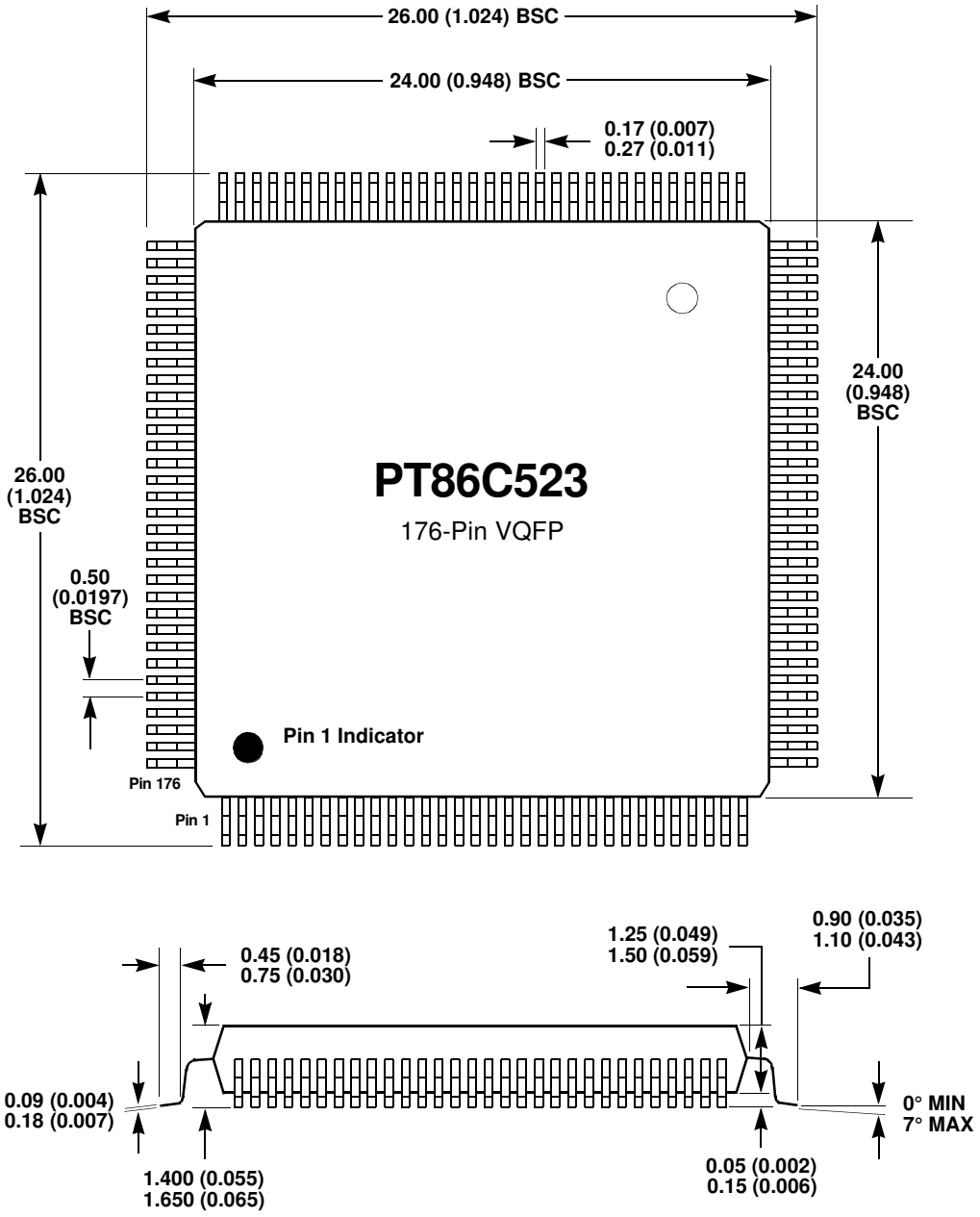
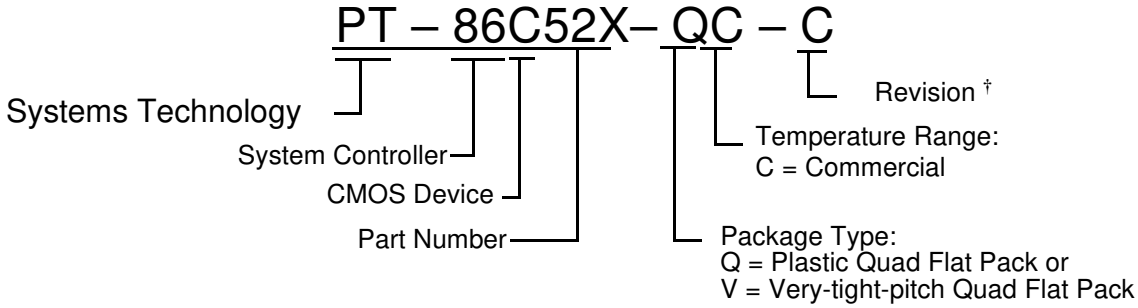


Figure A-3. 176-Pin VQFP Package Dimensions

Appendix B

Ordering Information Example

Contact the National Semiconductor sales office nearest you for the latest ordering and availability information. A list of National Semiconductor Direct Sales Offices can be found on the back cover of this document.



† Contact National Semiconductor Corporation for up-to-date information on revisions.

For V1-LS: X = 1
For V2-LS: X = 2
For V3-LS: X = 3

Appendix C

L2 Cache Auto-sizing: Sample Pseudo-Code Sequence

This sample pseudo-code sequence for cache sizing makes the following assumptions:

- **Memory:** at least 4 Mbytes
- **Cache:** standard synchronous
- **DRAM:** configured and tested

This example uses the 2- to 3-Mbyte area of memory to avoid any A20 Gate complications.

The following code goes through a process of turning on the L2 cache and writing a pattern such as 'AAH', and then turning off the L2 and writing another pattern such as '55H' (the pattern can be a byte, word, or double word length). When finished writing the patterns, a testing algorithm checks for either 'AAH' or '55H' in specific address locations, going from the 3-Mbyte boundary down to the 2-Mbyte boundary. When '55H' is detected, the cache size is determined to be the preceding cache size.

SEQUENCE

NOTE: Applicable register/bit settings are shown in parentheses.

1) Enable L1 cache and set to WB

2) Configure L2 cache to 128 Kbytes (Set index register 400H, bits [3:1] to '000')

3) Configure the cache to standard synchronous (Set index register 400H, bits [5:4] to '01')

4) Enable TAG initialization on L2 cache (Set index register 400H, bit 9 to '1')

5) Enable L2 cache (Set index register 400H, bit 0 to '1')

6) Write 'AAH' to addresses 208000H, 288000H, 2C8000H, and 2E8000H

7) Flush L1 cache

8) Read Memory from 200000H to 2FFFFFH to ensure a full L2 cache

9) Disable L2 cache (Set index register 400H, bit 0 to '1')

10) Disable TAG initialization on L2 cache (Set index register 400H, bit 9 to '0')

11) Write '55H' to addresses 208000H, 288000H, 2C8000H, and 2E8000H

12) Flush L1 cache

13) Load the cache-sizing algorithm — steps 14 and 15 — into L1 cache to ensure that there are no cache misses

14) Enable L2 cache (Set index register 400H, bit 0 to '1')

15) Test for cache size by reading the pattern in the following addresses in the order listed in Figure D-1. As long as 'AAH' is in the address, proceed to the next address. This step is illustrated with the help of a flow chart.

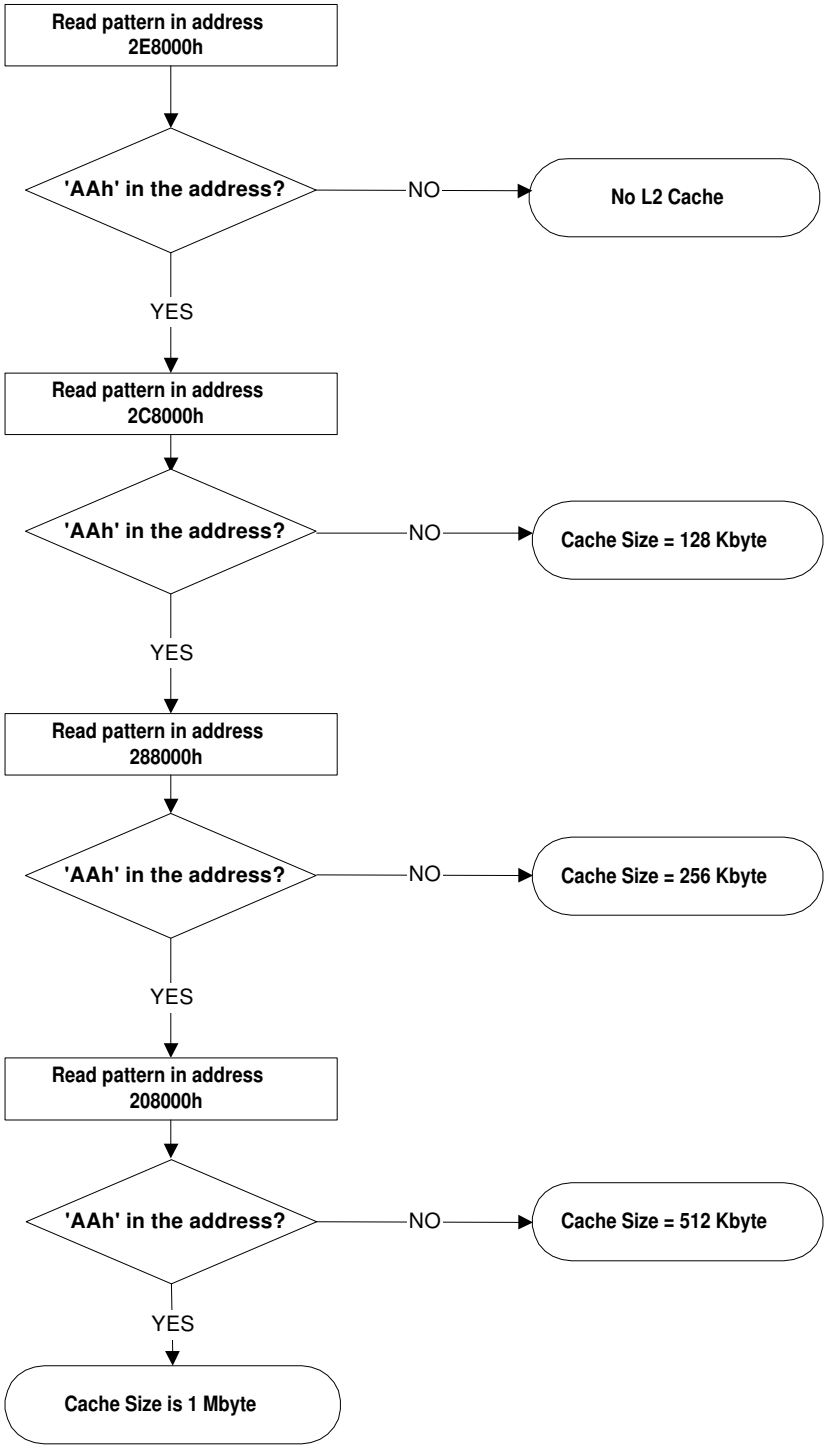


Figure D-4. Sequence for Testing Cache Size

16) Configure L2 cache to the correct size (Set index register 400H, bits [3:1] as appropriate)

17) Configure the cache to standard synchronous (Set index register 400H, bits [5:4] to '01')

18) Enable TAG initialization on L2 cache (Set index register 400H, bit 9 to '1')

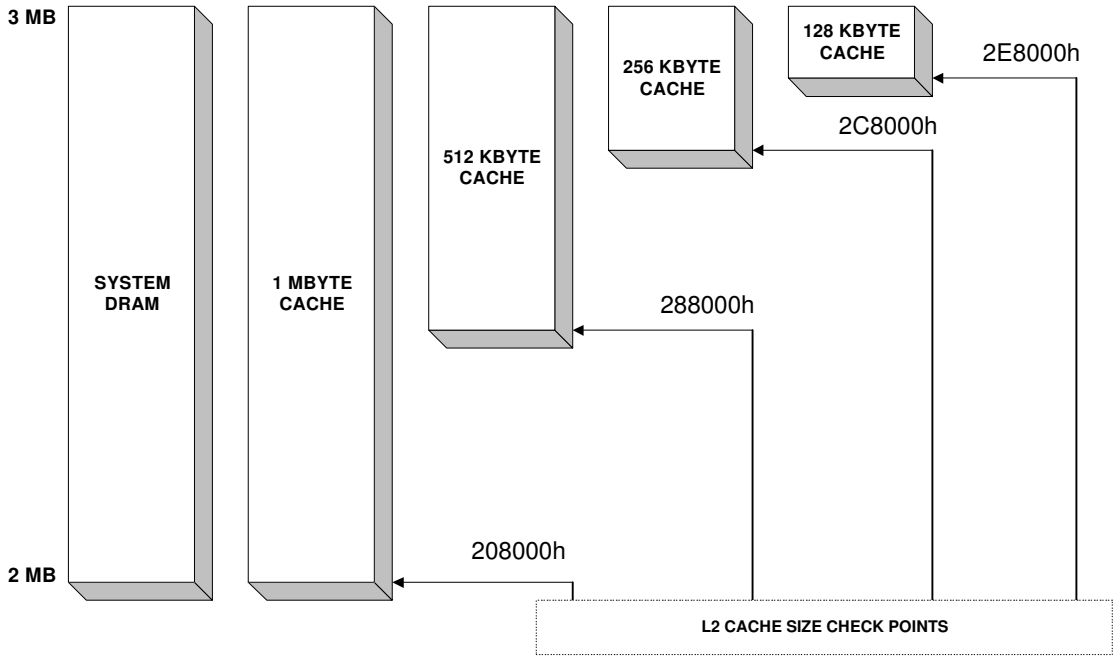
19) Enable L2 cache (Set index register 400H, bit 0 to '1')

20) Flush L1 cache

21) Read Memory from 200000H to 2FFFFFH to ensure cache coherency

22) Disable TAG initialization on L2 (Set index register 400H, bit 9 to '0')

23) Reconfigure L1 cache to WB



Appendix D

V1-LS Leakage Control Pin Status

LEGEND:
Hi-Z High impedance or tristate

Table E-1. V1-LS Leakage Control Pin Status

PIN NO.	PIN NAME	VOLTAGE	POWER PLANE	SUSPEND INPUT STATE	SUSPEND OUTPUT STATE
1	A6	3.3V	VCCCPU	low	Hi-Z
2	A7	3.3V	VCCCPU	low	Hi-Z
3	VCCCPU	3.3V	VCCCPU		
4	A8	3.3V	VCCCPU	low	Hi-Z
5	A9	3.3V	VCCCPU	low	Hi-Z
6	NMI	3.3V	VCCCPU		Hi-Z
7	A31	3.3V	VCCCPU	low	Hi-Z
8	VSSIO		VSSIO		
9	A10	3.3V	VCCCPU	low	Hi-Z
10	A11	3.3V	VCCCPU	low	Hi-Z
11	A12	3.3V	VCCCPU	low	Hi-Z
12	A13	3.3V	VCCCPU	low	Hi-Z
13	A14	3.3V	VCCCPU	low	Hi-Z
14	A15	3.3V	VCCCPU	low	Hi-Z
15	A16	3.3V	VCCCPU	low	Hi-Z
16	A17	3.3V	VCCCPU	low	Hi-Z
17	A18	3.3V	VCCCPU	low	Hi-Z
18	A19	3.3V	VCCCPU	low	Hi-Z
19	A20	3.3V	VCCCPU	low	Hi-Z
20	STPCLK#/SUSP#	3.3V	VCCCPU		Hi-Z

Table E-1. V1-LS Leakage Control Pin Status *(cont.)*

PIN NO.	PIN NAME	VOLTAGE	POWER PLANE	SUSPEND INPUT STATE	SUSPEND OUTPUT STATE
21	VSS CORE		VSSC		
22	V2CLK	3.3V	VCCCPU		low
23	VCC CORE	3.3V	VCCC		
24	CPUCLK	3.3V	VCCCPU		Hi-Z
25	VSSIO		VSSIO		
26	BE7#	3.3V	VCCCPU	high	
27	BE6#	3.3V	VCCCPU	high	
28	L2CLK	3.3V	VCCCPU		Hi-Z
29	VCCCPU		VCCCPU		
30	SMI#	3.3V	VCCCPU		Hi-Z
31	INIT/WM_RST	3.3V	VCCCPU		Hi-Z
32	CPURST	3.3V	VCCCPU		Hi-Z
33	BE5#	3.3V	VCCCPU	high	
34	BE4#	3.3V	VCCCPU	high	
35	BE3#	3.3V	VCCCPU	high	
36	BE2#	3.3V	VCCCPU	high	
37	BE1#	3.3V	VCCCPU	high	
38	BE0#	3.3V	VCCCPU	high	
39	IGNNE#	3.3V	VCCCPU		Hi-Z
40	FERR#	3.3V	VCCCPU	high	
41	ADS#	3.3V	VCCCPU	high	
42	M/IO#	3.3V	VCCCPU	low	
43	D/C#	3.3V	VCCCPU	high	
44	W/R#	3.3V	VCCCPU	high	
45	BRDY#	3.3V	VCCCPU		Hi-Z
46	NA#	3.3V	VCCCPU		Hi-Z
47	KEN#/INV	3.3V	VCCCPU		Hi-Z
48	WB/WT#	3.3V	VCCCPU		Hi-Z
49	EADS#	3.3V	VCCCPU		Hi-Z
50	HOLD/BOFF#	3.3V	VCCCPU		Hi-Z

Table E-1. V1-LS Leakage Control Pin Status *(cont.)*

PIN NO.	PIN NAME	VOLTAGE	POWER PLANE	SUSPEND INPUT STATE	SUSPEND OUTPUT STATE
51	HITM#	3.3V	VCCCPU	high	
52	CACHE#	3.3V	VCCCPU	high	
53	HLDA/LOCK#	3.3V	VCCCPU	low	
54	VCCCPU	3.3V	VCCCPU		
55	SMIACT#	3.3V	VCCCPU	high	
56	AHOLD	3.3V	VCCCPU		Hi-Z
57	VSSIO		VCCCPU		
58	A20M#	3.3V	VCCCPU		Hi-Z
59	INTR	3.3V	VCCCPU		Hi-Z
60	TAGD7	3.3V	VCCCPU		low
61	TAGD6	3.3V	VCCCPU		low
62	TAGD5	3.3V	VCCCPU		low
63	TAGD4	3.3V	VCCCPU		low
64	TAGD3	3.3V	VCCCPU		low
65	TAGD2	3.3V	VCCCPU		low
66	TAGD1	3.3V	VCCCPU		low
67	TAGD0	3.3V	VCCCPU		low
68	CE#	3.3V	VCCCPU		Hi-Z
69	CA4/ADSC#	3.3V	VCCCPU		Hi-Z
70	VSSIO		VCCCPU		
71	CA3/ADV#	3.3V	VCCCPU		Hi-Z
72	CWE7#	3.3V	VCCCPU		Hi-Z
73	CWE6#	3.3V	VCCCPU		Hi-Z
74	CWE5#	3.3V	VCCCPU		Hi-Z
75	CWE4#	3.3V	VCCCPU		Hi-Z
76	CWE3#	3.3V	VCCCPU		Hi-Z
77	CWE2#	3.3V	VCCCPU		Hi-Z
78	VCCCPU	3.3V	VCCCPU		
79	CWE1#	3.3V	VCCCPU		Hi-Z
80	CWE0#	3.3V	VCCCPU		Hi-Z

Table E-1. V1-LS Leakage Control Pin Status *(cont.)*

PIN NO.	PIN NAME	VOLTAGE	POWER PLANE	SUSPEND INPUT STATE	SUSPEND OUTPUT STATE
81	COE#	3.3V	VCCCPU		Hi-Z
82	TAGCS#/NALE#	3.3V	VCCCPU		Hi-Z
83	TAGWE#	3.3V	VCCCPU		Hi-Z
84	RAS3#	3.3V/5V	VCCDRAM		
85	RAS2#	3.3V/5V	VCCDRAM		
86	VSSIO	3.3V	VCCCPU		
87	RAS1#	3.3V/5V	VCCDRAM		
88	RAS0#	3.3V/5V	VCCDRAM		
89	VCCDRAM	3.3V/5V	VSSIO		
90	CASA3#	3.3V/5V	VCCDRAM		
91	CASA2#	3.3V/5V	VCCDRAM		
92	CASA1#	3.3V/5V	VCCDRAM		
93	CASA0#	3.3V/5V	VCCDRAM		
94	VSSIO	3.3V/5V	VCCDRAM		
95	CASB3#	3.3V/5V	VCCDRAM		
96	CASB2#	3.3V/5V	VCCDRAM		
97	VCCDRAM	3.3V/5V	VCCDRAM		
98	CASB1#	3.3V/5V	VCCDRAM		
99	CASB0#	3.3V/5V	VCCDRAM		
100	DRMWE#	3.3V/5V	VCCDRAM		
101	VSSIO	3.3V/5V	VCCDRAM		
102	MA11	3.3V/5V	VCCDRAM		
103	MA10	3.3V/5V	VCCDRAM		
104	VCCDRAM	3.3V/5V	VCCDRAM		
105	MA9	3.3V/5V	VCCDRAM		
106	MA8	3.3V/5V	VCCDRAM		
107	VSSIO	3.3V/5V	VCCDRAM		
108	MA7	3.3V/5V	VCCDRAM		
109	MA6	3.3V/5V	VCCDRAM		
110	VCCDRAM	3.3V/5V	VCCDRAM		

Table E-1. V1-LS Leakage Control Pin Status *(cont.)*

PIN NO.	PIN NAME	VOLTAGE	POWER PLANE	SUSPEND INPUT STATE	SUSPEND OUTPUT STATE
111	MA5	3.3V/5V	VCCDRAM		
112	MA4	3.3V/5V	VCCDRAM		
113	VSSIO		VSSIO		
114	MA3	3.3V/5V	VCCDRAM		
115	MA2	3.3V/5V	VCCDRAM		
116	VCCDRAM	3.3V/5V	VCCDRAM		
117	MA1	3.3V/5V	VCCDRAM		
118	MA0	3.3V/5V	VCCDRAM		
119	VSSIO		VSSIO		
120	PC5	5V	VCCDRAM		
121	PC4*	5V	VCCDRAM		
122	PC3*	5V	VCCDRAM		
123	PC2	5V	VCCDRAM		
124	PC1	5V	VCCDRAM		
125	PC0	5V	VSSIO		
126	GPIO5*	5V	VCCPMC		
127	GPIO4*	5V	VCCPMC		
128	GPIO3*	5V	VCCPMC		
129	GPIO2*	5V	VCCPMC		
130	GPIO1*	5V	VCCPMC	high (Cyrix)	
131	GPIO0*	5V	VCCPMC		
132	WAKE1	5V	VCCPMC		
133	WAKE0	5V	VCCPMC		
134	SWTCH	5V	VCCPMC		
135	RING	5V	VCCPMC		
136	BSER1TO3	5V	VCCPMC		low
137	VCC CORE	5V	VCCPMC		
138	CLKIN	5V	VCCPMC		
139	VSS CORE	5V	VCCPMC		
140	BSER3TO1	5V	VCCPMC	low	

Table E-1. V1-LS Leakage Control Pin Status *(cont.)*

PIN NO.	PIN NAME	VOLTAGE	POWER PLANE	SUSPEND INPUT STATE	SUSPEND OUTPUT STATE
141	BSERCLKV3	5V	VCCPMC		low
142	PWRGOOD	5V	VCCPMC		
143	RSTDRV	3.3V	VCCC		Hi-Z
144	VCC5-V	5V	VCCPMC		
145	EXTACT0	5V	VSSC		
146	RCRST#	5V	VCCPMC		
147	32KHZCLK	5V	VCCPMC		
148	DOCK_PCIRST#	5V	VCCPMC		Hi-Z
149	PCIRST#	5V	VCCPMC		Hi-Z
150	C/BE3#	5V	VCC5V	high	Hi-Z
151	C/BE2#	5V	VCCPMC	high	Hi-Z
152	C/BE1#	5V	VCCPMC	high	Hi-Z
153	VSSIO	5V	VCCPMC		
154	C/BE0#	3.3V/5V	VCCPCI	high	Hi-Z
155	FRAME#	3.3V/5V	VCCPCI	high	Hi-Z
156	VCCPCI	3.3V/5V	VCCPCI		
157	IRDY#	3.3V/5V	VCCPCI	high	Hi-Z
158	TRDY#	3.3V/5V	VCCPCI	high	Hi-Z
159	DEVSEL#	3.3V/5V	VSSIO	high	Hi-Z
160	STOP#	3.3V/5V	VCCPCI	high	Hi-Z
161	PLOCK#	3.3V/5V	VCCPCI	high	
162	REQ3#	3.3V/5V	VCCPCI	high	
163	REQ2#	3.3V/5V	VCCPCI	high	
164	REQ1#	3.3V/5V	VCCPCI	high	
165	REQ0#	3.3V/5V	VCCPCI	high	
166	GNT3#	3.3V/5V	VCCPCI		Hi-Z
167	GNT2#	3.3V/5V	VCCPCI		Hi-Z
168	GNT1#	3.3V/5V	VCCPCI		Hi-Z
169	GNT0#	3.3V/5V	VCCPCI		Hi-Z
170	PERR#	3.3V/5V	VCCPCI	high	Hi-Z

Table E-1. V1-LS Leakage Control Pin Status *(cont.)*

PIN NO.	PIN NAME	VOLTAGE	POWER PLANE	SUSPEND INPUT STATE	SUSPEND OUTPUT STATE
171	VSSIO	3.3V/5V	VCCPCI		
172	PCICLK	3.3V/5V	VCCPCI		low
173	PAR	3.3V/5V	VCCPCI	high	Hi-Z
174	VCCPCI	3.3V/5V	VCCPCI		
175	DOCK_PCICLK	3.3V/5V	VCCPCI		Hi-Z
176	CLKRUN#	3.3V/5V	VCCPCI	low	Hi-Z
177	ADPAR_ODD	3.3V/5V	VCCPCI	high	
178	ADPAR_EVEN	3.3V/5V	VCCPCI	high	
179	PCIMSTR#	3.3V/5V	VCCPCI		Hi-Z
180	BD7	3.3V	VSSIO	low	Hi-Z
181	BD6	3.3V/5V	VCCPCI	low	Hi-Z
182	BD5	3.3V/5V	VCCPCI	low	Hi-Z
183	BD4	3.3V/5V	VCCPCI	low	Hi-Z
184	VSSIO	3.3V/5V	VCCPCI		
185	BD3	3.3V/5V	VCCPCI	low	Hi-Z
186	BD2	3.3V	VCCCPU	low	Hi-Z
187	BD1	3.3V	VCCCPU	low	Hi-Z
188	BD0	3.3V	VCCCPU	low	Hi-Z
189	BDCTL2	3.3V	VCCCPU		Hi-Z
190	BDCTL1	3.3V	VCCCPU		Hi-Z
191	BDCTL0	3.3V	VCCCPU		Hi-Z
192	INCBUF	3.3V	VCCCPU		Hi-Z
193	VCCCPU		VSSIO		
194	DECBUF	3.3V	VCCCPU		Hi-Z
195	ADOE#	3.3V	VCCCPU		Hi-Z
196	A30	3.3V	VCCCPU	low	Hi-Z
197	A29	3.3V	VCCCPU	low	Hi-Z
198	A21	3.3V	VCCCPU	low	Hi-Z
199	A22	3.3V	VCCCPU	low	Hi-Z
200	A23	3.3V	VCCCPU	low	Hi-Z

Table E-1. V1-LS Leakage Control Pin Status *(cont.)*

PIN NO.	PIN NAME	VOLTAGE	POWER PLANE	SUSPEND INPUT STATE	SUSPEND OUTPUT STATE
201	A24	3.3V	VCCCPU	low	Hi-Z
202	A25	3.3V	VCCCPU	low	Hi-Z
203	A26	3.3V	VCCCPU	low	Hi-Z
204	A27	3.3V	VCCCPU	low	Hi-Z
205	A28	3.3V	VCCCPU	low	Hi-Z
206	A3	3.3V	VCCCPU	low	Hi-Z
207	A4	3.3V	VCCCPU	low	Hi-Z
208	A5	3.3V	VCCCPU	low	Hi-Z

Appendix E

Maintaining Similar Drive Characteristics (Rev. BB)

IMPORTANT: This application note only applies to Rev. BB of the VESUVIUS system controller.

To maintain similar drive characteristics, a special control signal has been implemented in the V1-LS, V2-LS, and V3-LS devices. A 100-K pull-up or pull-down resistor is required on the pins (listed in the table below) in addition to the strap options already defined in the VESUVIUS-LS design. These pins are sampled on power-on to control the drive current.

The following table shows how this implementation has been currently defined:

Table F-1. Power-On Sampling for Vesuvius Devices

Device	Pin No.	Pin Sampled on Power On	3-V	5-V
V1-LS PT86C521	109	MA6 = '0'	DRAM	
		MA6 = '1'		DRAM
	108	MA7 = '0'	PCI	
		MA7 = '1'		PCI
V2-LS PT86C522	68	ADPAR_EVEN = '0'	DRAM	
		ADPAR_EVEN = '1'		DRAM
	70	ADPAR_ODD = '0'	PCI	
		ADPAR_ODD = '1'		PCI
V3-LS PT86C523	78[1] / 66[2]	ROM_KB_CS# = '0'	PCI	
		ROM_KB_CS# = '1'		PCI

CAUTION: Device may be damaged if above implementation is not followed as shown.

Appendix F

Bulletin Board Service (BBS)

INTRODUCTION

PicoPower Bulletin Board Service (BBS) is primarily intended for one-way communication between Pico Power and its OEMs and end users.

PicoPower maintains strict access control to this bulletin board to minimize the possibility of distribution of pirated or virus-ridden software.

The software running on this bulletin board is Wildcat!™ IM, written by Mustang Software®, Inc.

TELEPHONE NUMBER AND COMMUNICATION PARAMETERS

The telephone number for the PicoPower BBS is **(408) 721-1654**. The communication parameters are:

- 8 data bits
- No parity
- 1 stop bit

The PicoPower BBS line supports up to a 14,400 baud rate. However, baud connections of 300 and 1200 bps are allowed, so long as such connections do not impede access for other users.

FIRST-TIME LOG ON

Upon connection with the bulletin board, the name and the password fields will display default entries for a 'New User' account. With this account the user can only download PicoPower product bulletins.

UPGRADED ACCESS

To access a BIOS image, schematics, application notes, errata reports, or utilities, an account upgrade is required. Please contact Sandy Hoang at (408) 721-5801 or through fax (408) 721-4785 for account upgrade. Allow at least one working day for the account upgrade to be effective.

INDEX OF ABBREVIATED REGISTER NAMES

This index is designed to help you find VESUVIUS-LS registers by their abbreviated name. It includes the registers for V1-LS, V2-LS, and V3-LS devices.