National Semiconductor

ADVANCE INFORMATION

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PC87560 — PCI System I/O

1.0 General Description

The PC87560 is a highly integrated IC that provides all of the system peripheral and power management functions (in conjunction with the PC87550 host controller) for a complete PCI based computer system. The functions include two Interrupt Controllers (8259), two DMA controllers (8237), System Timer (8254), and interfaces to an external Keyboard Controller, external ROM/FLASH ROM, and Real Time Clock for an AT compatible system. The system I/O functions include two serial ports (16550), one serial Infrared port, one Parallel port (IEEE 1284), Bus Mastering Fast IDE interface supporting two channels, Floppy Disk Controller (FDC), and OpenHCI Universal Serial Bus Controller (USB). Address re-mapping is provided for all internal functions to support Plug and Play capable systems. The PC87560 also provides additional I/O subsystem expansion via a 16-bit Fast Expansion Bus (FX Bus) giving the system designer additional I/O peripheral flexibility.

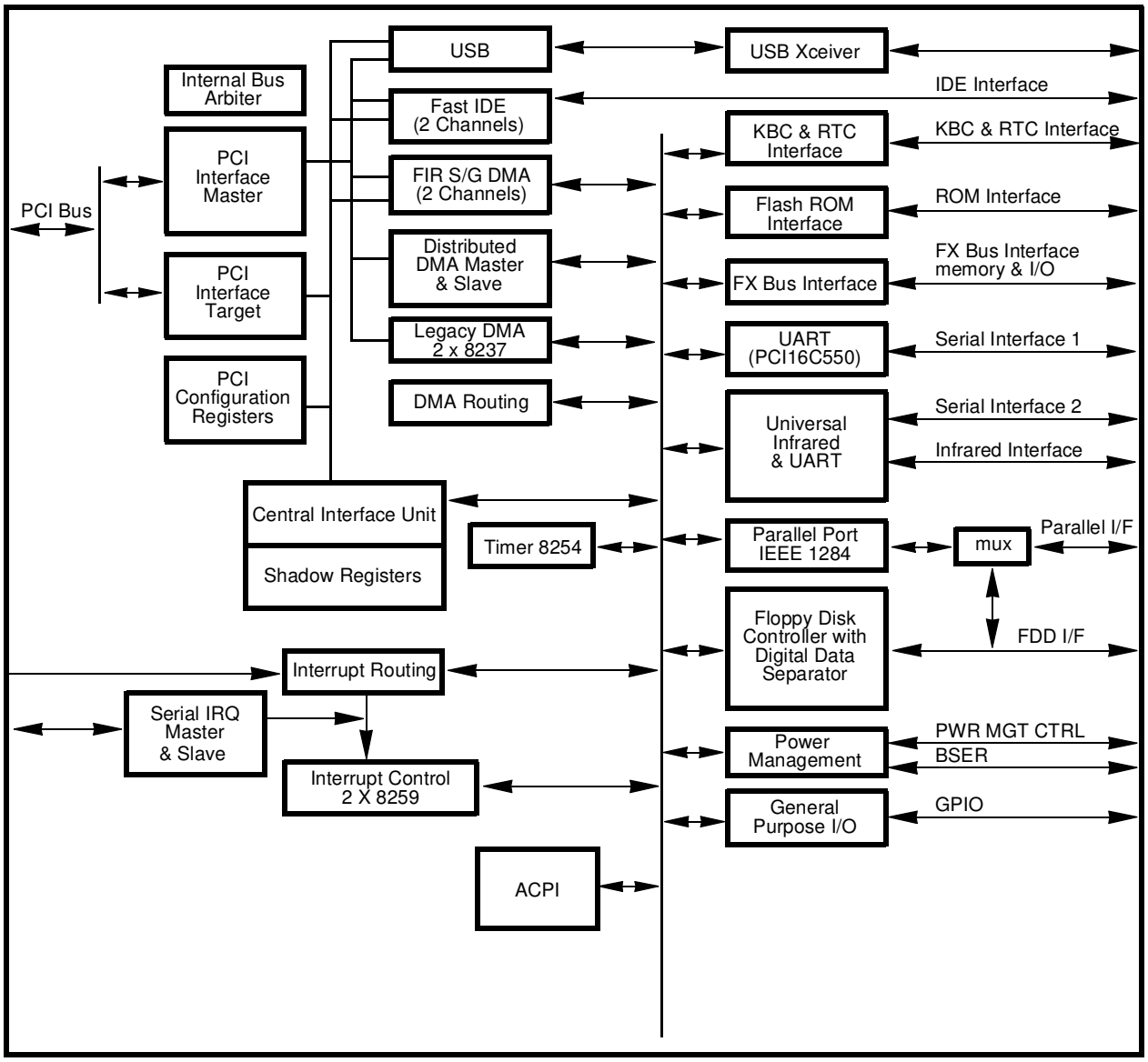
1.1 Features

- **PCI Interface**
  - PCI 2.1 Compliant
  - PCI Mobile Design Guide (revision 1.0 compliant)
  - 32-bit PCI Bus
  - Up to 33 MHz PCI Bus Frequency
  - Positive decoding when in notebook
  - Subtractive decoding when in dock
  - Internal functions fully remappable via PCI configuration registers
- **Enhanced IDE**
  - Programmable IDE access timing per channel/drive
  - 16 MBytes/sec maximum IDE data transfer rate
  - 2 IDE channels supported (primary and secondary)
  - Bus master support (SFF 8038 compliant)
  - Multi-tasking DMA engine for channel concurrency
  - 10 Double-Word write FIFOs per channel to sustain 16 MB/sec on IDE bus with burst of 8 Double-Words on the PCI Bus
  - ATAPI support (SFF 8022i compliant)
  - Supports ANSI ATA PIO Modes 0 through 4 and DMA modes 0 through 2
- **Universal Serial Bus (USB) Host Controller**
  - USB version 1.0 compliant
  - OpenHCI version 1.0a compliant
  - PCI Master DMA Scatter/Gather Channel
  - Two Root Hub Ports
  - Optimized List-Queue Manager for transfer scheduling and management
  - Dynamic re-scheduling of data transfers
  - Comprehensive Power Management support
  - Supports real-time device attaching/detaching
  - Supports transfer protocols for Full-speed (FS) and Low-Speed (LS) USB devices
  - Legacy Keyboard /Mouse Emulation
  - Integrated Transceivers
- **Legacy 8237 DMA Controller**
  - Seven 8237 compatible channels supported
  - Distributed DMA Master and Slave modes
  - 2 Double-Word Buffers for PCI Bus transfers
  - DMA Channel routing for Plug and Play
  - Support for preemption and re-arbitration per each PCI Bus transfer cycle
  - ISA Compatible, Type “A”, “B” and “F” timing supported
- **Floppy Disk Controller**
  - Software compatible with the DP8477, the 765A and the N82077
  - Perpendicular Recording drive support
  - Support of enhanced TDR
  - Tri-mode floppy support
  - 65% dynamic window margin
- **IEEE 1284 compatible Parallel Port**
  - All five modes supported: Compatible mode, Nibble mode, Byte mode, ECP,EPP 1.7 and 1.9.
  - One Legacy DMA channel supported
- **Floppy Interface multiplexed on Parallel Port**
- **Two Standard Serial Ports (16550 UART)**
  - Second serial port configurable as serial port or IR port
  - MIDI baud rate support
- **Infrared Communication Port**
  - IrDA (revision 1.0 compatible)
  - IrDA2 (revision 1.1 compatible)
  - 1.152Mb/sec and 4Mb/sec support
  - Sharp support
  - TV Remote Support
  - Programmable pulse width of 1.6 usec or 3/16 of bit time
  - Two independent DMA scatter/gather channels (one for receive and the other for transmit)
  - Two Legacy 8237 DMA channels support
  - Plug and Play dongle support
- **FX Bus (Non- Bus Master ISA Bus)**
  - Programmable timing for ISA compatible peripherals
  - 2 Programmable I/O range Chip selects
  - One Programmable Memory Range
  - One programmable, fragmented I/O window with Chip select for Sound Blaster compatibility
  - IORDY support
  - $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ support
  - DMA support (4 channels)
  - Interrupt support (3 channels)
- **ROM/FLASH ROM Interface**
  - Supports up to 256 KBytes of ROM
- **8254 Compatible Timer**
  - 3 Timer Channels
- **External Keyboard Controller Interface**
  - Interface to 8051 or PC87570 style keyboard controller
  - Keyboard Chip Select re-mappable anywhere in the 64Kbyte I/O range

Features Cont'd

- **External Real Time Clock Interface**
  - Support for DS1287 or MC146818 style RTCs
- **Interrupts**
  - Support for PCI native interrupts
  - Two 8259 interrupt controllers
  - Edge or level triggering individually programmable for each interrupt position
  - Interrupt routing for Plug and Play
  - PCIway Serial Interrupt support (both master and slave modes)
- **Mixed Voltage Support**
  - 5V and 3.3V operation
- **Power Management (ACPI/Slave Mode Support)**
  - Advanced Configuration and Power Interface (ACPI) support (revision 1.0 compliant)
  - Slave Mode: Power management control in the North-Bridge
  - FDC, SP1/2, IDE 1/2 and Parallel Port access monitors
  - 8 General Purpose I/Os for Power Management
  - 1 System event register monitoring IRQs 15-0 and NMI
  - CLKRUN# support
  - Full set of shadow registers
  - BSER (Burst Serial) interface to communicate power management activity to the PC87550 Host Bridge
- **Other**
  - Each internal peripheral can be individually disabled
  - Fast GateA20 and Fast Keyboard Reset support
  - PCI Bus and CPU reset control
  - Port 61 and Port 92 support
  - Numeric coprocessor error support (Port F0)
  - Back powering protection from printer, FDC and IDE
  - 316 BGA package

Block Diagram



2.0 Pin Description

2.1 PCI Interface

Pin	Name	Voltage (See Notes)	Type	Description
See Table 2.17	AD[31:0]	3/5V	I/O	Multiplexed **A**ddress and **D**ata**.** The direction of these pins are defined below: *Phase* — *Target* — *Bus Master* Address Phase — input — output Data Phase Read — output — input Write — input — output
G18 G19 G20 H17	C/BE[3:0]	3/5V	I/O	**C**ommand/**B**yte **E**nable are multiplexed Bus command and Byte enables.
D12	PAR	3/5V	I/O	**PAR**ity is even parity across AD[31:0] and C/BE[3:0]. PAR directionality follows the AD[31:0] directionality.
B11	FRAME#	3/5V	I/O	Cycle **FRAME** is driven by the initiator to indicate the beginning and duration of an access.
C12	TRDY#	3/5V	I/O	**T**arget **R**ea**DY** indicates that the target of the current data phase of the transaction is ready to be completed.
B12	IRDY#	3/5V	I/O	**I**nitiator **R**ea**DY** indicates that the initiator is ready to complete the current data phase of the transaction.
C11	STOP#	3/5V	I/O	**STOP** indicates that the current target is requesting the initiator to stop the current transaction.
A11	LOCK#	3/5V	I	**LOCK** indicates an atomic operation that may require multiple transactions to complete.
D11	DEVSEL#	3/5V	I/O	**DEV**ice **SEL**ect, when driven active low, this signal indicates the driving device has decoded its address as the target of the current access.
B14	IDSEL	3/5V	I	**I**nitialization **D**evice **SEL**ect is used as a chip select during configuration read and write transactions.
A13	PERR#	3/5V	I/O	**P**arity **ERR**or is used for reporting data parity errors during all PCI transactions except a Special Cycle. PERR# is an output when AD[31:0] and PAR are inputs and is an input when AD[31:0] and PAR are outputs.
A12	SERR#	3/5V	I/O	**S**ystem **ERR**or is used for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. When reporting address parity errors, SERR# is an output. As an input to the PC87560, any PCI device can pulse the SERR# to indicate a catastrophic error condition.
A14	PCICLK	3/5V	I	**PCI CL**oc**K.** The PCI clock input can be any frequency from 0-33MHz.
D13	PCIRST#	3/5V	O	**PCI R**e**S**e**T.** PCIRST# is used to reset PCI bus devices and is asserted following RESET_IN#. PCIRST# will be deasserted a minimum of 1ms after RESET_IN# is deasserted.

2.2 Arbitration Signals

Pin	Name	Voltage (See Notes)	Type	Description
C13	SIOGNT#	3/5V	I	PCI **S**ystem **I/O** Gra**NT.** This is signal is asserted from the host bridge allowing the PC87560 to become the PCI bus master.
B13	SIOREQ#	3/5V	O	PCI **S**ystem **I/O REQ**uest. This signal is asserted this signal to request the host controller to allow the PC87560 to become PCI bus Master.

2.3 PCI Interrupts

Pin	Name	Voltage (See Notes)	Type	Description
A9 D10 C10 B10	INTA#, INTB#, INTC#, INTD#	3/5V	I	PCI **INT**errupt Request **A**, **B**, **C** and **D**. These four active-low, share-able interrupt requests may be used by PCI devices to make an inter-rupt request.

2.4 IDE Interface

Pin	Name	Voltage (See Notes)	Type	Description
See Table 2.17	DD[15:0]	3/5VT	I/O	IDE **D**rive **D**ata Bus**.** When accessing the IDE drive, this is an 8- or 16-bit bi-direction data bus between the PC87560 chip and the drive. The lower 8 bits are used for non-data 8-bit transfers (such as regis-ters, ECC bytes).
W16, V16, U16	DA[2:0]	3/5V	O	IDE **D**rive **A**ddress. When accessing the IDE drive, these pins are the DA[2:0] pins used to access a register or data port in the drive.
V11	DIORDY	3/5VT	I	**D**rive **I/O** Channel **R**ea**DY.** When accessing the IDE drive, this signal is negated (low) to extend a Programmable I/O (PIO) disk transfer cycle of any register access (read or write) when the drive is not ready to respond to a data transfer request. When an IDE drive no longer desires to extend the cycle, DIORDY will be placed in TRI-STATE by the IDE drive(s) and pulled high by an external pull-up resistor.
U11	DIOR#	3/5V	O	**D**rive **I/O R**ead. This is the read strobe signal for both channels. When active low, DIOR# enables data from a register or the data port of the drive onto the IDE Drive data bus.
Y12	DIOW#	3/5V	O	**D**rive **I/O W**rite. This is the write strobe signal for both channels. The rising edge of DIOW# clocks data from the IDE Drive data bus into the register or the data port of the drive.
Y8	DRST#	3/5V	O	**D**rive **R**e**S**e**T.** This signal from the IDE Controller is asserted active low during power up or under software control. DRST# will remain active low as long as the PCI Reset signal (PCIRST#) is asserted low or as long as the drive reset bit in the IDE Controller is set to one. **NOTE:** This signal will be driven active low for a maximum of 2 msec. following the rising edge of RESET_IN#. It is the system designer's responsibility to guarantee that no accesses are made to any IDE drive device during this period of time, if the IDE drive devices use this signal as reset and the PC87560's PCIRST# is not used as the PCI Bus reset. In such a case the PC87560 cannot guarantee that a PCI Bus Cycle will not occur while DRST# remains active low. If the PC87560's PCIRST# is used as the PCI Bus reset, no accesses until DRST# is de-asserted high are guaranteed.

U9 V9	CH1_CS1#, CH1_CS3#	3/5V	O	**CH**annel **1 C**hip **S**elect **1** and **3.** CH1_CS1# is the chip select signal to select the Command Block Registers. CH1_CS3# is the chip select signal to select the Control Block Registers of channel 1.
V10 W10	CH2_CS1#, CH2_CS3#	3/5V	O	**CH**annel **2 C**hip **S**elect **1** and **3.** CH2_CS1# is the chip select signal to select the Command Block Registers. CH2_CS3# is the chip select signal to select the Control Block Registers of channel 2.
W9 Y10	CH1_INT CH2_INT	3/5VT	I	**CH**annel **1** and **CH**annel **2** Drive **INT**errupts. These signals are used to interrupt the host system. CH1_INT is asserted when the drive(s) on channel 1 have a pending interrupt. CH2_INT is asserted when the drive(s) on channel 2 have a pending interrupt.
Y9	CH1_ DMREQ	3/5VT	I	**CH**annel **1 DM**A **REQ**uest. This signal is used when the device is configured to use the pseudo DMA handshake mode or when using the internal DMA controller. When asserted, this signals the PC87560 that the selected drive on channel 1 is ready to transfer data.
Y11	CH2_ DMREQ	3/5VT	I	**CH**annel **2 DM**A **REQ**uest. This signal is used when the device is configured to use the pseudo DMA handshake mode or when using the internal DMA controller. When asserted, this signals the PC87560 that the selected drive on channel 2 is ready to transfer data.
U10	CH1_ DMACK#	3/5V	O	**CH**annel **1 DM**A **ACK**nowledge. This signal is used when the PC87560's IDE Controller is configured to use the pseudo DMA handshake mode or when using the internal DMA controller. This signal indicates to the selected drive on channel 1 that data has either been accepted, or that data is available.
W11	CH2_ DMACK#	3/5V	O	**CH**annel **2 DM**A **ACK**nowledge. This signal is used when the PC87560's IDE Controller is configured to use the pseudo DMA handshake mode or when using the internal DMA controller. This signal indicates to the selected drive on channel 2 that data has either been accepted, or that data is available.

2.5 FX Bus Interface

Pin	Name	Voltage (See Notes)	Type	Description
Y17	FXA[20]	3/5V	O	**FX A**ddress 20. This is the most significant address bit on the FX Bus. It will always be driven by the PC87560 and is never multiplexed with any data.
See Table 2.17	FXA[19:4]/ FXD[15:0]	3/5VT	I/O	**FX A**ddress19-4/FX **D**ata Bus 15-0. This is the multiplexed FX address/data bus. During FX Bus address phases, the appropriate address will be driven onto these pins by the PC87560. During FX Bus data phases, the PC87560 will drive out the appropriate data during write cycles and will TRI-STATE these signals during read cycles, thus acting as inputs.
R17, R18, R19, R29	FXA[3:0]	3/5VT	O	**FX A**ddress 3-0. These four signals are the least significant address bits on the FX Bus. They will always be driven by the PC87560 and are not multiplexed with data.
P20	FXASTB#	3/5V	O	**FX A**ddress **ST**ro**B**e. During the FX Bus address phase, the falling edge of FXASTB# is used to latch the address FXA[19:4] off of the multiplexed FXA[19:4]/FXD[15:0] pins.
N17	FXIOR#	3/5VT	O	**FX I/O R**ead. This is the FX bus I/O read strobe. The pulse width of this signal is programmable.
N18	FXIOW#	3/5VT	O	**FX I/O W**rite. This is the FX bus I/O write strobe. The pulse width of this signal is programmable.
M19	FXMEMR#	3/5V	O	**FX MEM**ory **R**ead. This is the FX bus Memory read strobe. This signal will strobe active for every memory read cycle on the FX Bus.
M20	FXMEMW#	3/5V	O	**FX MEM**ory **W**rite. This is the FX bus Memory write strobe. This signal will strobe active for every memory write cycle on the FX Bus

L17	FXSMEMR#	3/5V	O	**FX S**ystem **MEM**ory **R**ead. This is the FX bus System Memory read strobe. This signal will strobe active only for memory reads on the FX Bus with addresses below 1Meg.
L18	FXSMEMW#	3/5V	O	**FX S**ystem **MEM**ory **W**rite. This is the FX bus System Memory write strobe. This signal will strobe active only for memory writes on the FX Bus with address below 1Meg.
N19	FXIORDY	3/5VT	I/O	**FX I/O R**ea**DY**. When accessing the FX bus this signal may be negated low by the device being accessed to extend the FX bus transfer cycle.
N20	FXIOCS16#	3/5VT	I	**FX I/O C**hip **S**elect **16** Bit. This input signal is driven active low by 16-bit I/O devices when they are being addressed and this signal will be used by the PC87560's FX Bus Controller to appropriately steer data for I/O cycles.
M17	FXMEMCS16#	3/5VT	I	**FX MEM**ory **C**hip **S**elect **16** Bit. This input signal is driven active low by 16-bit memory devices when they are being addressed and this signal will be used by the PC87560's FX Bus Controller to appropriately steer data for memory cycles.
M18	BHE#	3/5V	O	**B**yte **H**igh **E**nable. This FX Bus signal is asserted low to indicate the high (odd) data byte is being transferred. Only 16-bit devices use this signal.
L20, K20, K19, K18	DRQ[3:0]	3/5VT	I	**D**MA **R**e**Q**uests **3-0.** These DMA request pins may be steered to any of the internal PC87560 8237 DMA Controllers' request inputs.
J18	DACK0#/ DOCKEN#	3/5VT	I/O	**D**MA **ACK**nowledge **0**/**DOCK EN**able. During normal operation this pin will act as the active-low DMA Acknowledge output signal associated with the DRQ[0] input. During a power-up reset this pin will become an input strapping option and is sampled on the rising edge of RESET_IN#. This I/O has a weak pull-down resistor, thus will default low unless an external pull-up resistor is used. If this pin is sampled low, the PC87560 will indicate that it is in a Docking Station (Its Function 1 Device ID will be 000Eh). If this pin is sampled high, then the PC87560 will indicate that it is in the Notebook Motherboard (Its Function 1 Device ID will be 0011h).
J19	DACK1#/ FENCFG	3/5VT	I/O	**D**MA **ACK**nowledge **1**/**F**unction **EN**able **C**on**F**i**G**uration. During normal operation this pin will act as the active-low DMA Acknowledge output signal associated with the DRQ[1] input. During a power-up reset this pin will become an input strapping option and is sampled on the rising edge of RESET_IN#. This I/O has a weak pull-down resistor, thus will default low unless an external pull-up resistor is used. If this pin is sampled low, all of the PC87560 functions are disabled. If this pin is sampled high, then the PC87560 functions will operate normally as defined.
J20	DACK2#/ FGA20EN	3/5VT	I/O	**D**MA **ACK**nowledge **2**/**F**ast **G**ate **A20 EN**able. During normal operation this pin will act as the active-low DMA Acknowledge output signal associated with the DRQ[2] input. During a power-up reset this pin will become an input strapping option and is sampled on the rising edge of RESET_IN#. This I/O has a weak pull-down resistor, thus will default low unless an external pull-up resistor is used. If this pin is sampled low, the Fast GateA20 and the Fast Keyboard Reset logic will be disabled. If this pin is sampled high, the Fast GateA20 and the Fast Keyboard Reset logic will be enabled.

K17	DACK3#/ SIRQMST	3/5VT	I/O	**D**MA **ACK**nowledge **3**/**S**eral **I**nterrupt **R**e**Q**uest **M**a**ST**er Mode Enabled. During normal operation this pin will act as the active-low DMA Acknowledge output signal associated with the DRQ[3] input. During a power-up reset this pin will become an input strapping option and is sampled on the rising edge of RESET_IN#. This I/O has a weak pull-down resistor, thus will default low unless an external pull-up resistor is used. If this pin is sampled low, the Serial Interrupt interface logic will be operate as a Slave. If this pin is sampled high, the Serial Interrupt interface logic will operate as the Master.
J17	TC/ MRTRYD#	3/5VT	I/O	**T**erminal **C**ount/**M**emory **R**e**TRY D**isable. During normal operation this pin will act as the Terminal Count (TC) of a compatible 8237 DMA Controller. During a power-up reset this pin will become an input strapping option and is sampled on the rising edge of RESET_IN#. This I/O has a weak pull-down resistor, thus will default low unless an external pull-up resistor is used. If it is sampled low, memory reads from the ROM BIOS will not be retried on the PCI Bus. If this pin is sampled high, memory reads from the ROM BIOS will be retried on the PCI Bus. NOTE: If the reads from the ROM BIOS are not retried, it would tend to violate the standard 16 PCI clock Target Initial Latency requirement. As long as the purpose of these read cycles is to perform a POST Code copy of the ROM image to memory, this will be compliant with the PCI Local Bus specification Revision 2.1.
H20, H19, H18	FXIRQ[2:0]	3/5VT	I	**FX** Bus **I**nterrupt **R**e**Q**uest **2-0.** These are general purpose interrupts that are internally routed (configurable) to the interrupt lines of the 8259s.
P17, P18	FXCS[1:0]#	3/5V	O	**FX C**hip **S**elect **0** and **1**. These two active-low signals are programmable I/O address range chip selects to select external devices on the FX bus.
P19	AUDIOCS#	3/5V	O	**AUDIO C**hip **S**elect. This active-low output chip select provides support for a compatible, fragmented Sound Blaster I/O map.

2.6 External KBC and RTC Interface

Pin	Name	Voltage (See Notes)	Type	Description
B8	KBCS#	3/5V	O	**K**ey**B**oard Controller **C**hip **S**elect. This pin is asserted during read or write accesses to the keyboard's programmable I/O locations.
C8	KBGA20	3/5VT	I	**K**ey**B**oard **GA**te**A20** input. Gate A20 from an external keyboard controller.
C9	KBINT	3/5VT	I	**K**ey**B**oard **INT**errupt. Keyboard interrupt request from an external keyboard controller.
D8	KBRST#	3/5VT	I	**K**ey**B**oard **R**e**S**e**T** input. Keyboard Reset from an external keyboard controller.
D9	MINT	3/5VT	I	**M**ouse **INT**errupt. Mouse interrupt request from an external keyboard controller.
A7	RTCALE/ PMCS#	3/5V	O	**R**eal **T**ime **C**lock **A**ddress **L**atch **E**nable or **P**ower **M**anagement **C**hip **S**elect. When this pin is programmed as the RTCALE pin, then this pin is asserted during an I/O write to port 70h. When this pin is configured as the PMCS# pin, then this pin is asserted during an I/O read/ write to addresses KBCBAR+2h, and KBCBAR+6h.
A8	RTCCS#	3/5V	O	**R**eal **T**ime **C**lock **C**hip **S**elect. This pin is asserted during I/O read or write accesses to the RTC location 71h. When VMKBC is selected (Function1, Reg. 5Ch, bit 4="1"), this pin is asserted during I/O read or write accesses to locations 70h and 71h.
J4	RTCINT#	3/5VT_PM	I	**R**eal **T**ime **C**lock **INT**errupt. Active-low Real Time Clock interrupt.

2.7 ROM Interface

Pin	Name	Voltage (See Notes)	Type	Description
L19	ROMCS#	3/5V	O	**ROM C**hip **S**elect. This signal will be active low any time there is a memory access to the (configurable) ROM BIOS memory range.

2.8 Universal Serial Bus Interface

Pin	Name	Voltage (See Notes)	Type	Description
L4	OC_SENSE1	3/5VT	I	USB Root Hub **O**ver-**C**urrent **SENSE** PORT **1** input. Used in conjunction with an external bus power regulator to indicate to the host controller when a bus overcurrent shutdown has occured.
M1	OC_SENSE2	3/5VT	I	USB Root Hub **O**ver-**C**urrent **SENSE** PORT **2** input. Used in conjunction with an external bus power regulator to indicate to the host controller when a bus overcurrent shutdown has occured.
K3 K2	PORT1D+, PORT1D-	3/5V_PM	I/O	USB Root Hub **PORT 1 D**ifferential Signal Pair.
L1 L2	PORT2D+, PORT2D-	3/5V_PM	I/O	USB Root Hub **PORT 2 D**ifferential Signal Pair.
M2	PWRCTL1#	3/5V	O	USB Root Hub **P**o**W**e**R** **C**on**T**ro**L** PORT **1** output. Used in conjunction with an external USB bus power regulator to enable or disable bus power.
M3	PWRCTL2#	3/5V	O	USB Root Hub **P**o**W**e**R** **C**on**T**ro**L** PORT **2** output. Used in conjunction with an external USB bus power regulator to enable or disable bus power.
K4	USB_ACT	3/5V_PM	O	**USB ACT**ivity. When active high this output indicates that there has been activity on the USB ports. This output is used to support ACPI wake-up via activity on the USB ports.

2.9 Floppy Disk Controller Interface

Pin	Name	Voltage (See Notes)	Type	Description
G3,G4	MSEN[1:0]	3/5VT	I	**M**edia **SEN**se **0** and **1**
D2,D3	DENSL[1:0]	3/5V	O	**DEN**sity **S**elect **0** and **1**
E3,E2	DS[1:0]#	3/5V	O	**D**rive **S**elect **0** and **1**
D1,E4	MTR[1:0]#	3/5V	O	**M**o**T**o**R S**elect **0** and **1**
E1	DIR#	3/5V	O	**DIR**ection
G2	INDEX#	3/5VT	I	**INDEX**
F4	STEP#	3/5V	O	**STEP**
F3	WDATA#	3/5V	O	**W**rite **DATA**
F2	WGATE#	3/5V	O	**W**rite **GATE**
M4	TRK0#	3/5VT	I	**TR**ac**K 0**
N1	WP#	3/5VT	I	**W**rite **P**rotect
N2	RDATA#	3/5VT	I	**R**ead **DATA**
F1	HDSEL#	3/5V	O	**H**ea**D SEL**ect
N3	DSKCHG#	3/5VT	I	**DiSK CH**an**G**e

2.10 Serial Port 1 and 2

Pin	Name	Voltage (See Notes)	Type	Description
Y6,U4	DCD[1:0]#	3/5VT	I	**D**ata **C**arrier **D**etect for Serial Port 1 and 2.
U7,W3	DSR[1:0]#	3/5VT	I	**D**ata **S**et **R**eady for Serial Port 1 and 2.
V7,Y3	SIN[1:0]	3/5VT	I	**S**erial Data **IN** for Serial Port 1 and 2.
W7,V4	RTS[1:0]#	3/5V	O	**R**eques**T** to **S**end for Serial Port 1 and 2.
Y7,W4	SOUT[1:0]	3/5V	O	**S**erial Data **OUT**put for Serial Port 1 and 2.
U8,Y4	CTS[1:0]#	3/5VT	I	**C**lear **T**o **S**end for Serial Port 1 and 2.
V8,U5	DTR[1:0]#	3/5V	O	**D**ata **T**erminal **R**eady for Serial Port 1 and 2.
W8,V5	RI[1:0]#	3/5VT	I	**R**ing **I**ndicator for Serial Port 1 and 2.

2.11 Serial Infrared Interface

Pin	Name	Voltage (See Notes)	Type	Description
W5	IRTX	3/5V	O	**I**nfra**R**ed **T**ransmit Data
Y5	IRRX	3/5VT	I	**I**nfra**R**ed **R**eceive Data
U6	IRSEL0/ IRRX2/ID[0]	3/5VT	I/O	**I**nfra**R**ed **SEL**ect 0 or **I**nfra**R**ed **R**eceive Data **2** or **ID0** for plug and play support
W6,V6	IRSEL[2:1]/ ID[2:1]	3/5VT	I/O	**I**nfra**R**ed **SEL**ect 2-1 or **ID[2:1]** for plug and play support

2.12 Parallel Port/Floppy Interface

Pin	Name	Voltage (See Notes)	Type	Description
P2	STB#/ WRITE#	3/5VT	O	Data **ST**ro**B**e in compatibility Parallel Port mode, **WRITE** strobe in ECP mode
P3	PD0/ INDEX#	3/5VT	I/O	**D**ata **0** in **P**arallel Port mode or **INDEX#** in floppy mode.
P4	PD1/TRK0#	3/5VT	I/O	**D**ata **1** in **P**arallel Port mode or **TR**ac**K 0** in floppy mode.
R1	PD2/WP#	3/5VT	I/O	**D**ata **2** in **P**arallel Port mode or **W**rite **P**rotect in floppy mode.
R2	PD3/ RDATA#	3/5VT	I/O	**D**ata **3** in **P**arallel Port mode or **R**ead **DATA** in floppy mode.
R3	PD4/ DSKCHG#	3/5VT	I/O	**D**ata **4** in **P**arallel Port mode or **DiSK CH**an**G**e in floppy mode.
R4	PD5/ MSEN0	3/5VT	I/O	**D**ata **5** in **P**arallel Port mode or **M**edia **SEN**se **0** in floppy mode.
T2	PD6/ DENSL1	3/5VT	I/O	**D**ata **6** in **P**arallel Port mode or **DEN**sity **S**e**L**ect**1** in floppy mode.
T1	PD7/MSEN1	3/5VT	I/O	**D**ata **7** in **P**arallel Port mode or **M**edia **SEN**se **1** in floppy mode.
T3	ACK#/DS1#	3/5VT	I/O	**ACK**nowledge in Parallel Port mode or **D**rive **S**elect **1** in floppy mode.
T4	BUSY#/ WAIT#/ MTR1#	3/5VT	I/O	**BUSY** in compatibility parallel port mode, **WAIT** in ECP mode and **M**o**T**o**R** Select **1** in floppy mode.
U1	PE/ WDATA#	3/5VT	I/O	**P**aper **E**nd in Parallel Port mode or **W**rite **DATA** in floppy mode.
U2	SLCT/ WGATE#	3/5VT	I/O	**S**e**L**e**CT** in parallel port mode or **W**rite **GATE** in floppy mode.

U3	SLIN#/ ASTB#/ STEP#	3/5V	O	**S**e**L**ect **IN**put in compatibility Parallel Port mode, **ST**ro**B**e in ECP mode and **STEP** in floppy mode.
V1	INIT#/DIR#	3/5V	O	**INIT**ialize in Parallel Port mode or **DIR**ection in floppy mode.
V2	ERR#/ HDSEL#	3/5VT	I/O	**ERR**or in Parallel Port mode or **H**ea**D SEL**ect in floppy mode.
V3	AFD#/ DSTRB#/ DENSL0	3/5V	O	**A**utomatic **F**ee**D** XT in compatibility Parallel Port mode, **D**ata**S-TR**o**B**e**#** in ECP mode and **DEN**sity **S**e**L**ect**0** in floppy mode.
N4	PNF	3/5VT	I	**P**rinter **N**ot **F**loppy. This input is disabled when the PNF Select bit (Bit 0 of the System I/O Configuration Register at offset 5Ch) is a zero. When this input is a zero and the PNF Select bit is a one, the FDC signals are multiplexed onto the Parallel Port/Floppy pins. When this input is a one and the PNF Select bit is a one, the Parallel Port signals are multiplexed onto the Parallel Port/Floppy pins.

Note: DENSL1 is a 14ma push-pull output

2.13 Power Management Interface

Pin	Name	Voltage (See Notes)	Type	Description
A10	CLKRUN#	3/5V	I/O	**CL**oc**K RUN** is used to request starting or stopping the PCI clock as well as indicating the clock status. The PC87560 can request the Central Resource, to start or maintain the interface clock by assertion of CLKRUN#. The Central Resource is responsible for maintaining CLKRUN# asserted, and for driving it high to the deasserted state. CLKRUN# defaults low (active) upon deassertion of reset. CLKRUN# is a sustained TRI-STATE I/O signal.
H3	SLPEN#	3/5V_PM	O	**SL**eep **EN**able. This signal indicates a request for the ACPI Embedded Controller to enter an ACPI sleep mode.
J3	EVENT1/ EX_PME_EC	3/5VT_PM	I/O	**EVENT 1** or **EX**ternal **P**ower **M**anagement **E**vent input from the **E**mbedded **C**ontroller. When power management is configured in slave mode, EVENT1 is an output and will be asserted whenever one of the system events occurs in the System Events 1 Register. This pin can be connected to the EXTACT0 pin of the PC87550 Host Controller. When this signal functions as EX_PME_EC, it operates as the ACPI External Power Management Event input signal from the Embedded Controller.
J1	SMI_SB	3V_PM	O	**S**ystem **M**anagement **I**nterrupt. This signal is asserted high whenever an I/O trap occurs, a system event occurred, an SMI occurred through the Serial Interrupt bus, or when an ACPI SMI is generated. SMI_SB is an active high output to a PCI Bus Host Controller and will remain asserted until software clears the condition causing the SMI.
D7	BSERCLK3	3/5VT	I	**B**urst **SER**ial **CL**oc**K**. This pin is the serial bus clock for the serial system and power management bus (BSER1TO3/BSER3TO1).
C7	BSER3TO1	3/5V	O	**B**urst **SER**ial **3TO1**. Communicates system and power management information from the PC87560 to the PC87550.
B7	BSER1TO3	3/5VT	I	**B**urst **SER**ial **1TO3**. Communicates system and power management information from the PC87550 to the PC87560.
H1	SUSPEND#	3/5VT_PM	I	**SUSPEND#**. This pin is asserted by the ACPI Embedded Controller to acknowledge entering an ACPI sleep state. When the Embedded Controller de-asserts this signal high, it indicates that the Embedded Controller is waking-up the system.

C3	GPIO0/AEN	3/5VT	I/O	**G**eneral **P**urpose **I/O 0** or FX Bus **A**ddress **EN**able. When this pin is configured as a General Purpose I/O, this pin is accessed through the General Purpose I/O register Bit 0. When this pin is configured as the AEN signal, it will function as the FX Bus Address ENable signal for FX Bus cycles.
B3	GPIO1/ID3	3/5VT	I/O	**G**eneral **P**urpose **I/O 1** or Infrared **ID3** input. When this pin is configured as a General Purpose I/O, this pin is accessed through the General Purpose I/O register Bit 1. When this pin is configured to operate as the ID3 pin, it will act as the ID3 Infrared input signal to the UIR module. NOTE: When configured as a General Purpose I/O, the value driven will continue to be driven to the UIR module as the ID3 Infrared input signal. It is the responsiblity of the hardware and software system design to avoid any conflicts between the configuration of this pin and the associated (if any) Infrared Driver software.
A3	GPIO2	3/5VT	I/O	**G**eneral **P**urpose **I/O 2**. This pin is accessed through the General Purpose I/O register Bit 2. It may be configured to operate as either a Totem-Pole driver (default) or as an Open-Drain driver (to support a bit-bang I^2C interface).
C4	GPIO3	3/5VT	I/O	**G**eneral **P**urpose **I/O 3**. This pin is accessed through the General Purpose I/O register Bit 3. It may be configured to operate as either a Totem-Pole driver (default) or as an Open-Drain driver (to support a bit-bang I^2C interface).
B4	GPIO4/ IDE_INT1	3/5VT	I/O	**G**eneral **P**urpose **I/O 4** or **IDE INT**errupt **1** output. When this pin is configured as a GP I/O pin, this pin is accessed through the General Purpose I/O register Bit 4. When configured as the IDE_INT1 pin, it will be the output of the IDE Channel 1 Interrupt Request.
A4	GPIO5/ IDE_INT2	3/5VT	I/O	**G**eneral **P**urpose **I/O 5** or **IDE INT**errupt **2** output. When this pin is configured as a GP I/O pin, this pin is accessed through the General Purpose I/O register Bit 5. When configured as the IDE_INT2 pin, it will be the output of the IDE Channel 2 Interrupt Request.
D5	GPIO6/ USB_INT	3/5VT	I/O	**G**eneral **P**urpose **I/O 6** or **USB INT**errupt output. When this pin is configured as a GP I/O pin, this pin is accessed through the General Purpose I/O register Bit 6. When this pin is configured as the USB_INT pin, it will be the output of the USB Host Controller's Interrupt Request.
J2	GPIO7/ EX_PME	3/5VT_PM	I/O	**G**eneral **P**urpose **I/O 7** or **EX**ternal **P**ower **M**anagement **E**vent input. When used as a General Purpose I/O pin, this pin is accessed through the General Purpose I/O register Bit 7. When this pin is configured as EX_PME, this input will signal an External Power Management Event to the ACPI logic.

2.14 CPU Interface and Miscellaneous

Pin	Name	Voltage (See Notes)	Type	Description
B5	FGA20	Open-Drain	O	**F**ast **G**ate **A20**. This signal with a pull-up resistor can be used to drive the CPU A20M# pin. If the USB Legacy Keyboard Support function is enabled, it will be the source for this output. Otherwise, if the Fast GateA20 strapping option is enabled this would be the source of this signal. If both the USB Legacy Keyboard Support function and the Fast Gate A20 strapping option are disabled, then the Keyboard GateA20 input (KBGA20) will drive this signal.
A5	CPURST	Open-Drain	O	**CPU R**e**S**e**T**. This signal with a pull-up resistor can be used to drive the CPU Reset signal of the CPU. The PC87560 releases CPURST during power-up (PWRGOOD negated). CPURST is driven inactive low a minimum of 2ms after RESET_IN# is driven inactive to allow the CPU's clock and VCC to stablize. CPURST is driven inactive low synchronously to the rising edge of PCICLK.
D6	CPUINIT	Open-Drain	O	**CPU INIT**ialization. This signal with a pull-up resistor can be used to drive the CPU's INIT pin during power-up (PWRGOOD negated) or when the PC87560 detects a shutdown special cycle on the PCI bus. CPUINIT will also be active if a soft reset is initiated via Port 92, or a snooped Fast Reset (if Fast Reset is enabled) or KBRST# is asserted (if Fast Reset is disabled).
H2	RESET_IN#	3/5VT_PM	I	**RESET IN**put. When de-asserted high, RESET_IN# is an indication to the PC87560 that power and PCICLK have been stable for at least 1ms, and can be driven asynchronously. When RESET_IN# is asserted low, the PC87560 resets all functions powered by VDD and asserts CPURST, CPUINIT and PCIRST#.
H4	PM_PWRGOOD	3/5VT_PM	I	**P**ower **M**anagement **P**o**W**e**R GOOD**. When PM_PWRGOOD is asserted high, it indicates that the VDD_PM power is on and valid. When PM_PWRGOOD is de-asserted low, it will reset all PC87560 functions that are powered by VDD_PM.
C5	CPUINT	Open-Drain	O	**CPU INT**errupt. This signal with a pull-up resistor can be used to drive the CPU INT pin.
C6	FERR#	3/5V	I	Numeric Coprocessor **ERR**or input from the CPU.
B6	IGNNE#	Open-Drain	O	**IGN**ore **N**umeric **E**rror. This signal wit ha pull-up resistor may be used to drive the CPU IGNNE pin.
B9	SINT	3/5V	I/O	**S**erial **INT**errupt I/O for Docking Interface
C2	SPKR	3/5V	O	**SP**ea**K**e**R** Output.
A6	NMI	Open-Drain	O	**N**on **M**askable **I**nterrupt. This signal with a pull-up resistor may be used to drive the CPU's NMI signal. This signal is active high when a PCI System Error occurs.
A2	TEST#	3/5VT	I	**TEST.** This input has a weak pull-up resistor and in normal operation should be a ***No Connect.***

2.15 Clocks

Pin	Name	Voltage (See Notes)	Type	Description
C1	14.318CLK	3/5VT	I	**14.318** Mhz **CL**oc**K** Oscillator Input
P1	48CLK	3/5VT	I	**48**Mhz **CL**oc**K** input For Super I/O Functions

2.16 Power and Ground

Pin	Name	Pin Type SEE NOTE 6	Description
L3	AVSS	USB GND	Analog Ground. This pin should be connected seperately to the system ground plane on a seperate trace from the digital VSS pins.
E7,E8,E10,E11,E13, E14,G5,G16,H5,H16, K5,K16,L5,L16,N5, N16,P5,P16,T7,T8, T10,T11,T13,T14	VDD	POWER (Note 6)	+5v or +3.3v power input. These VDD pins are used to provide power to the core and I/O buffers (except for the ACPI circuitry and I/Os).
G1	VDD_PM	POWER (Note 6)	+5v or +3.3v power input. This VDD_PM pin provides power to the ACPI circuitry and I/Os only.
K1	VREF	USB POWER	USB 3.3 volt, **V**oltage **REF**erence. 3.3 volts must be supplied to this pin from an external regulator if VDD=VDD_PM=3.3 volts. The USB_REG_EN bit (Bit 0 of the USB Regulator Control Register at ACPIBAR+1Fh) is used to select the PC87560's on-chip regulator. Following a PM_PWRGOOD transition, the PC87560's on-chip regulator will be disabled. **NOTE:** If an external regulator is used, it must be sequenced at the same time as VDD_PM. When the PC87560's on-chip regulator is used, a 10 microfarad capacitor should be connected externally to the VREF and AVSS pins to provide additional stability. No other device should be connected to this pin when the PC87560's on-chip regulator is enabled.
E5,E6,E9,E12,E15, E16,F5,F16,J5,J9, J10,J11,J12,J16,K9, K10,K11,K12,L9,L10, L11,L12,M5,M9,M10, M11,M12,M16,R5, R16,T5,T6,T9,T12, T15,T16	VSS	GND	Ground.

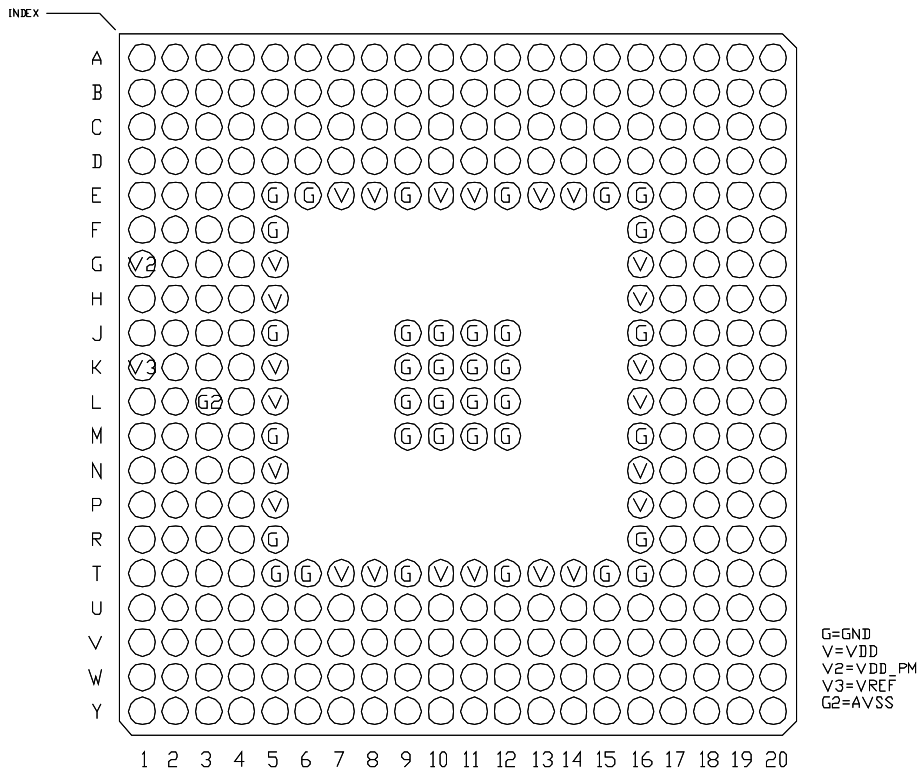
Notes:

1. A signal designated as 3/5V means that if the chip is powered by 3V (VDD=3.3V), then the I/O is 3V. If the chip is powered by 5V (VDD=5V), then the I/O is 5 volts.
2. A signal designated as 3/5VT means that if the chip is powered by 3V (VCC=3.3V), then the I/O is 3V with 5V tolerant inputs. If the chip is powered by 5V (VCC=5V), then the I/O is 5 volts.
3. Open-Drain indicates those output signals that will always be Open-Drain signals capable of driving the associated CPU signals directly.
4. A signal designated as 3/5V_PM means that this signal is powered by the ACPI power (VDD_PM). Furthermore, if the ACPI logic is powered by 3V (VDD_PM=3.3V), then the I/O is 3V. If the ACPI logic is powered by 5V (VDD_PM=5V), then the I/O is 5 volts.
5. A signal designated as 3/5VT_PM means that this signal is powered by the ACPI power (VDD_PM). Furthermore, if the ACPIlogic is powered by 3V (VDD_PM=3.3V), then the I/O is 3V with 5V tolerant inputs. If the ACPI logic is powered by 5V (VDD_PM=5V), then the I/O is 5 volts.
6. Both VDD and VDD_PM must be the same voltage (VDD=5V and VDD_PM=5V) or (VDD=3.3V and VDD_PM=3.3V). Furthermore VDD_PM may be powered by either 5V or 3.3V when VDD is not being powered, but VDD_PM must be present before VDD is applied.

2.17 Bus Pin List

Pin **(In Decending Bit Order)**	**Bus**
C14,D14,A15,B15,C15,D15,A16,B16,C16,D16,A17,B17,C17,A18,B18,D17,A19, C18,C19,C20,D18,D19,D20,E17,E18,E19,E20,F17,F18,F19,F20,G17	AD[31:0]
W12,V12,U12,Y13,W13,V13,U13,Y14,W14,V14,U14,Y15,W15,V15,U15,Y16	DD[15:0]
W17,V17,Y18,W18,V18,W20,U17V19,V20,U18,U19,U20,T17,T18,T19,T20	FXA[19:4]/FXD[15:0]

2.18 Connection Diagram



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3.0 DC Specifications

3.1 Absolute Maximum Ratings

(Notes 1 and 2)

Symbol	Characteristic	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		-0.5	7.0	V
V_I	Input Voltage		-0.5	V_{DD} + 0.5	V
V_O	Output Voltage		-0.5	V_{DD} + 0.5	V
T_{STG}	Storage Temperature		-65	+165	°C
P_D	Power Dissipation			1	W
T_L	Lead Temperature Soldering (10 seconds)			+260	°C

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

3.2 Recommended Operating Conditions

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
			4.75	5.0	5.25	V
T_A	Operating Temperature		0		+70	°C
	ESD Tolerance	C_{ZAP} = 100 pF R_{ZAP} = 1.5 kW (Note 1)	1500			V

Note 1: Value based on test complying with NSC SOP5-028 human body model ESD testing using the ETS-910 tester.

3.3 Pin Capacitance (Excluding PCI Bus Signal Pins)

$T_A = 25_i C$, f = 1 Mhz

Symbol	Characteristic	Min	Typ	Max	Unit
C_{IN}	Input Pin Capacitance		5	7	pF
C_{IN1}	Clock Input Capacitance		8	10	pF
C_{IO}	I/O Pin Capacitance		10	12	pF
C_O	Output Pin Capacitance		6	8	pF

3.4 Pin Capacitance For PCI Bus Signal Pins

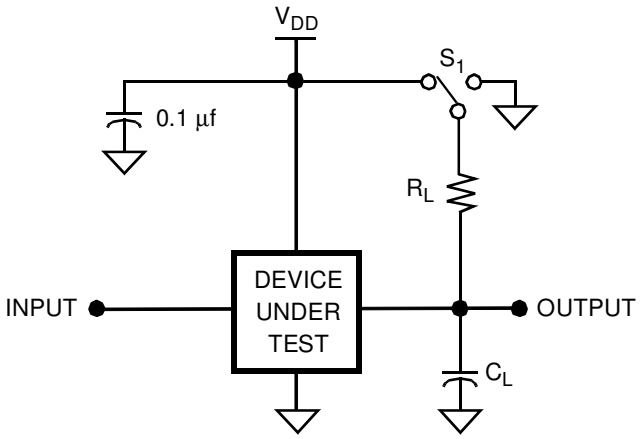
Symbol	Characteristic	Min	Typ	Max	Unit
$C_{P,IN}$	PCI Input Pin Capacitance			10	pF
$C_{P,CLK}$	PCI Clock Input Capacitance			12	pF
L_{PIN}	Pin Inductance			20	nH

4.0 AC Timing Specifications

4.1 AC Test Conditions

All test conditions are, T_A = 0 ^oC to 70 ^oC, V_{DD} = 5.0V +/- 5%, 3.0V to 3.6V

Load Circuit (Notes 1, 2, 3)



AC Testing Input/Output Waveform

Note 1: C_L = 100 pF, includes jig and scope capacitance.

Note 2: S_1 = Open for push-pull outputs. S_1 = V_{DD} for high impedance to active low and active low to high impedance measurements. S_1 = GND for high impedance to active high and active high to high impedance measurements. R_L = 1.0 kohm for

Note 3: For the FDC Open Drive Interface Pins S_1 = V_{DD} and R_L = 150ohms.

4.2 Clock Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{CH}	CLK High Pulse Width	11		ns	
t_{CL}	CLK Low Pulse Width	11		ns	
t_{CP}	CLK Period	30		ns	
t_{ICP}	Internal Clock Period	*Table 4.1*		ns	
t_{DRP}	Data Rate Period	*Table 4.1*		ns	

Table 6.1 — Nominal t_{ICP} , t_{DRP} Values

MFM Data Rate	t_{DRP}	t_{ICP}	Value	Units
1 Mbps	1000	3 x t_{CP}	125	ns
500 kbps	2000	3 x t_{CP}	125	ns
300 kbps	3333	3 x t_{CP}	208	ns
250 kbps	4000	6 x t_{CP}	250	ns

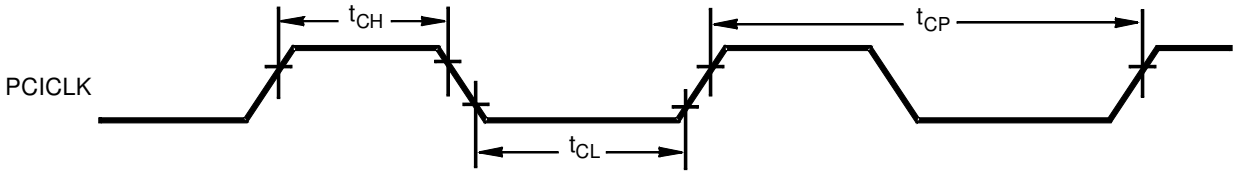


Figure 4.1 — CLK Timing

4.3 PCI Timing

Symbol	Parameter	Min	Max	Units	Notes
t_1	PCI Signals Input Setup Time to CLK	7		ns	
t_{1A}	Address Setup to CLK for Fast Decode			ns	
t_2	PCI Signals, CLK to Output Valid (bussed signals)	2	16	ns	
	CLK Slew Rate (Input)	1	4	V/ns	
	RST# Slew Rate (Output)	1	4	V/ns	
t_{ON}	Float to Active Delay	2		ns	
t_{OFF}	Active to Float Delay		28	ns	
t_H	Input Hold Time from CLK	2		ns	
t_{RST}	Reset Active Time After Power Stable	1		ms	
$t_{RST-CLK}$	Reset Active Time After CLK Stable	100		ms	
$t_{RST-OFF}$	Reset Active to Output Float Delay		40	ns	
t_{CR}	CLK to CLKRUN# Valid		17	ns	
t_{CR-SET}	CLKRUN# Input Setup Time to CLK		7	ns	

4.4 UART Timing

4.4.1 BAUD OUT TIMING

Symbol	Parameter	Min	Max	Units	Notes
N	Baud Divisor	1	65535	clocks	
t_{BHD}	Baud Output Positive Edge Delay		56	ns	Note 1
t_{BLD}	Baud Output Negative Edge Delay		56	ns	Note 1

Note 1: Conditions: CLK = 24 MHz/2, 100 pF load

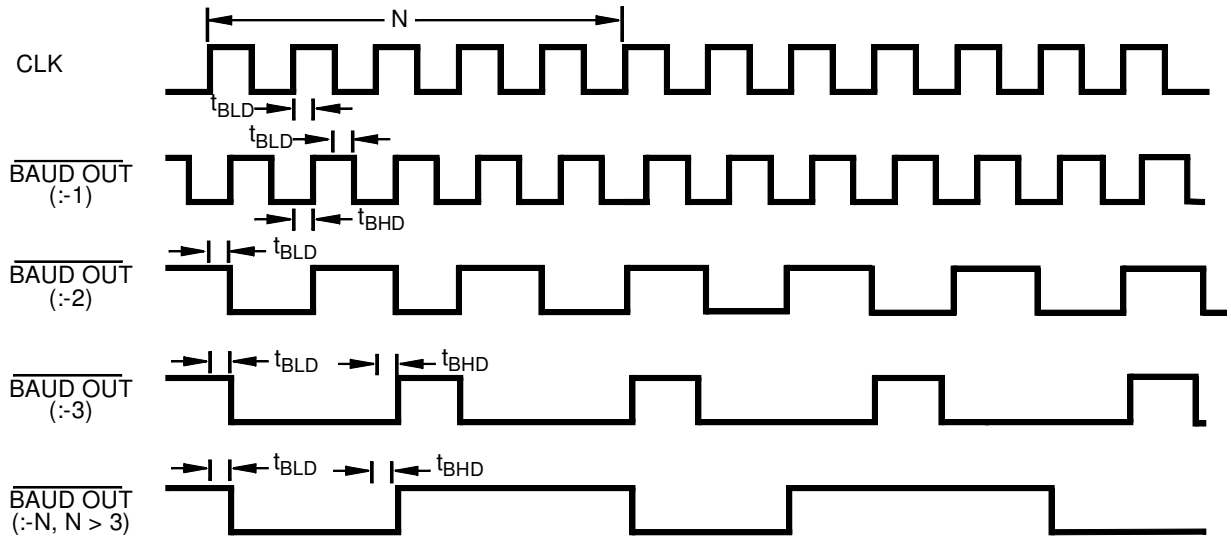


Figure 4.2 — Baud Out Timing

4.4.2 MODEM CONTROL TIMING

Symbol	Parameter	Min	Max	Units	Notes
t_{MDO}	Delay from WR# (WR MCR) to Output		40	ns	
t_{RIM}	Delay to Reset IRQ from RD# (RD MSR)		78	ns	
t_{SIM}	Delay to Set IRQ from MODEM Input		40	ns	

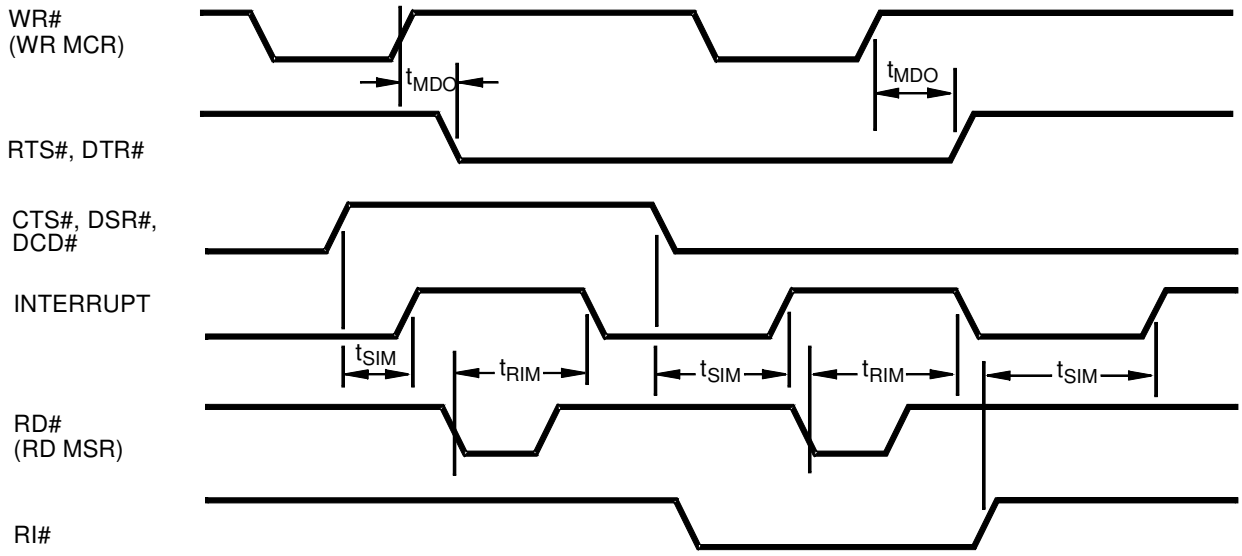


Figure 4.3 — MODEM Control Timing

4.5 Infrared Interface Timing

Symbol	Parameter		Min	Max	Units	Notes
t_{CMW}	Modulation Signal Pulse Width in Sharp-IR and Consumer-IR	Transmitter Receiver	t_{CWN}-30ns 500	t_{CWN}+30ns	ns	Note 1
t_{CMP}	Modulation Signal Period in Sharp-IR and Consumer-IR	Transmitter Receiver	t_{CPN}-30ns t_{MMIN}	t_{CPN}+30ns t_{MMAX}		Note 2 Note 3
t_{BT}	Single Bit Time in UART and Sharp-IR	Transmitter Receiver	t_{BTN}-30ns t_{BTN}-2%	t_{BTN}+30ns t_{BTN}+2%		Note 4
S_{DRT}	SIR Transmitter Data Rate Tolerance			+/- 0.87%		
t_{SJT}	SIR Receiver Edge JItter. Percent of Nominal Bit Duration			+/- 6.5%		
t_{SPW}	SIR Signal Pulse Width	Transmitter, variable	(3/16) x t_{BTN} - 25ns	(3/16) x t_{BTN} - 25ns		Note 4
		Transmitter, fixed	1.60	1.65	µs	
		Receiver	1		µs	
M_{DRT}	MIR Transmitter Data Rate Tolerance			+/- 0.1%		
t_{MJT}	MIR Receiver Edge Jitter. Percent of Nominal Bit Duration			+/- 2.9%		
t_{MPW}	MIR Signal Pulse Width	Transmitter Receiver	t_{MWN}-25ns 60	t_{MWN}+25ns	ns	Note 5
F_{DRT}	FIR Transmitter Data Rate Tolerance			+/- 0.01%		
t_{FJT}	FIR Receiver Edge Jitter. Percent of Nominal Bit Duration			+/- 4.0%		
t_{FPW}	FIR Signal Single Pulse Width	Transmitter Receiver	120 90	130 160	ns ns	
t_{FDPW}	FIR Signal Double Pulse Width	Transmitter Receiver	245 215	255 285	ns ns	

Note 1: t_{CWN} is the nominal pulse width of the modulation signal for Sharp-IR and Consumer-IR modes. It is determined by the MCPW[2:0] and TXHSC bits in the IRTXMC and RCCFG registers.

Note 2: t_{CPN} is the nominal period of the modulation signal for Sharp-IR and Consumer-IR modes. Iby the MCFR[4:0] and TXHSC bits in the IRTXMC and RCCFG registers.

Note 3: t_{MMIN} and t_{MMAX} define the time range within which the period of the incoming carrier signal has to fall in order for the signal to be accepted by the receiver. These time values are determined by the content of register IRRXDC and the setting of bit RXHSC in the RCCFG register.

Note 4: t_{BTN} is the nominal bit time in UART, Sharp-IR, SIR, and Consumer-IR modes. It is determined by setting the baud generator divisor register.

Note 5: t_{MWN} is the nominal pulse width for MIR mode. It is determined by the MPW[3:0] and MDRS bits in the MIR_PW and IRCR2 registers.

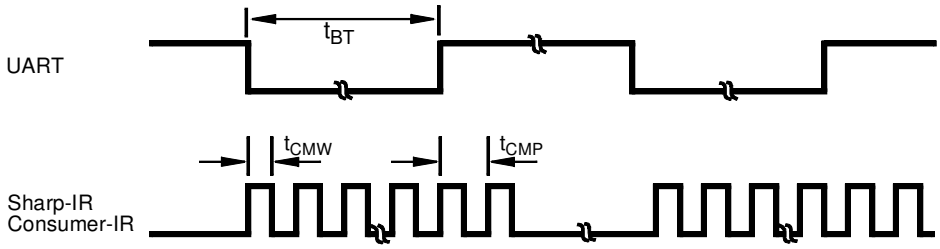


Figure 4.4 — UART, Sharp-IR, and Consumer-IR Timing

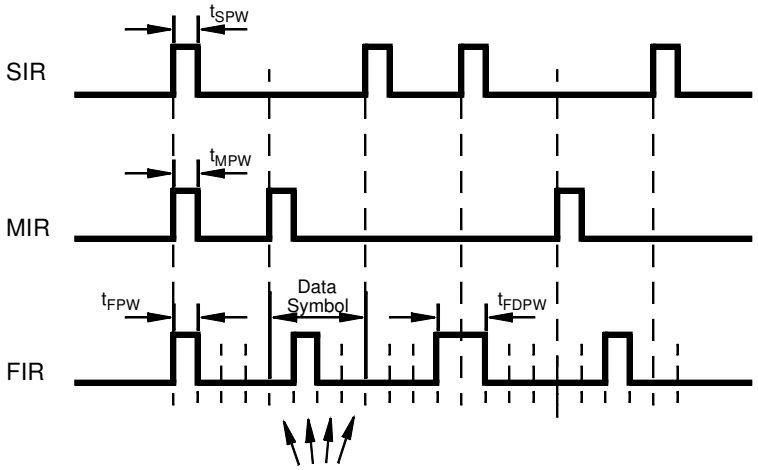


Figure 4.5 — SIR, MIR, and FIR Timing

4.6 Parallel Port Timing

Symbol	Parameter	Typ	Max	Units	Notes
t_{PDH}	Port Data Hold	500		ns	Note 1
t_{PDS}	Port Data Setup	500		ns	Note 1
t_{PI}	Port Interrupt		33	ns	
t_{SW}	STB# Width	500		ns	Note 1

Note 1: These times are system dependent and are therefore not tested.

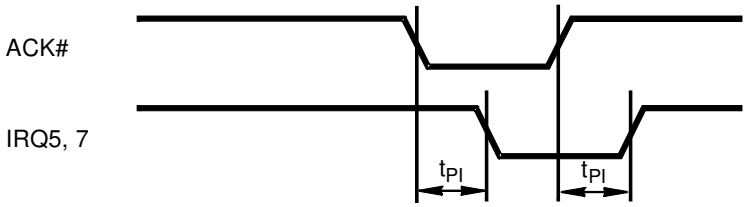


Figure 4.6 — Compatible Mode Parallel Port Interrupt Timing

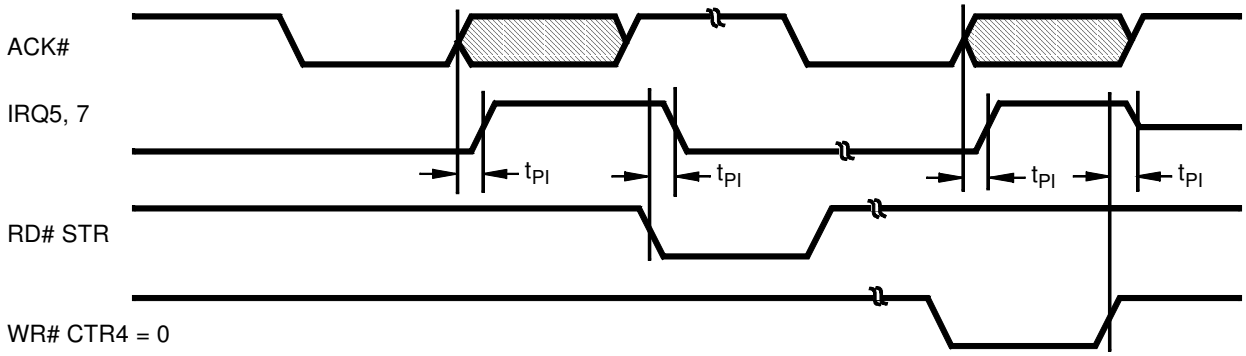


Figure 4.7 — Extended Mode Parallel Port Interrupt Timing

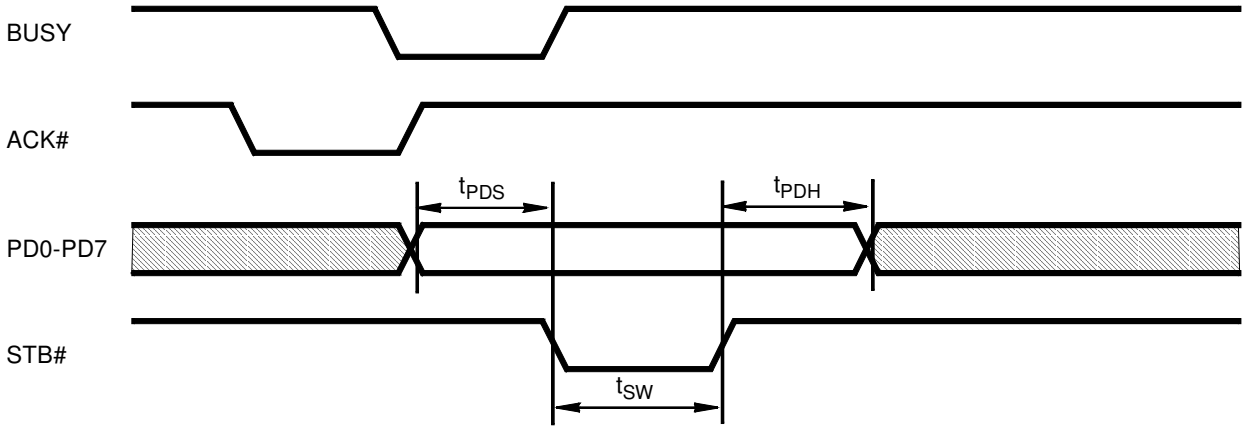


Figure 4.8 — Typical Parallel Port Data Exchange

4.7 Bserial Interface Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{BS-CLK}	BSER CLK Period (CPU clock / 2)	30	40	ns	
$t_{1to3-SET}$	BSER Interface (from PC87550 to PC87560) Input Set-up to BSER CLKBSER CLK Period (CPU clock / 2)	5		ns	
$t_{1to3-HLD}$	BSER CLK to BSER Interface (from PC87550 to PC87560) Output Valid				
$t_{3to1-SET}$	BSER Interface (from PC87560 to PC87550) Input Set-up to BSER CLK				
$t_{3to1-HLD}$	BSER CLK to BSER Interface (from PC87560 to PC87550) Output Valid	11	23	ns	

4.8 DMA Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{D1}	DACK# to FXIOR#	100		ns	
t_{D2}	DACK# to FXA/FXD = FFFFh	0		ns	
t_{D3}	DACK# to FXASTB#	60		ns	
t_{D4}	TC valid setup time to the rising edge of FXIOR# or FX-IOW#	400		ns	
t_{D5}	FXIOR# Width	720		ns	
t_{D6}	FXA/FXD turn off		12	ns	
t_{D7}	Read Data Setup	80		ns	
t_{D8}	Read Hold	0		ns	
t_{D9}	FXIOR# Inactive to DACK# Inactive	120		ns	
t_{D10}	TC valid hold time from the rising edge of FXIOR# or FXIOW#	60		ns	
t_{D11}	DRQ Removal Time	120		ns	Note 1
t_{D12}	DACK# to FXIOW#	360		ns	
t_{D13}	FXIOW# Width	480		ns	
t_{D14}	FXIOW# Inactive to DACK# Inactive	120		ns	
t_{D15}	Write Data Setup Time	400		ns	
t_{D16}	Write Data Hold Time	10		ns	
t_{D17}	Max Delay Between FXIORDY and FXIOR# in order to Insert Wait States		500	ns	
t_{D18}	Cycle Finish after Removal of FXIORDY	120		ns	
t_{D19}	Max Delay Between FXIORDY and FXIOW# in order to Insert Wait States		260	ns	

t_{D20}	AEN Valid to FXIOR# or FXIOW# active command strobe	100		ns	
t_{D21}	AEN Valid from FXIOR# or FXIOW# active command strobe	30		ns	

Note 1: In Demand Mode DRQ needs to be removed before this time so the next DMA cycle will not be generated.

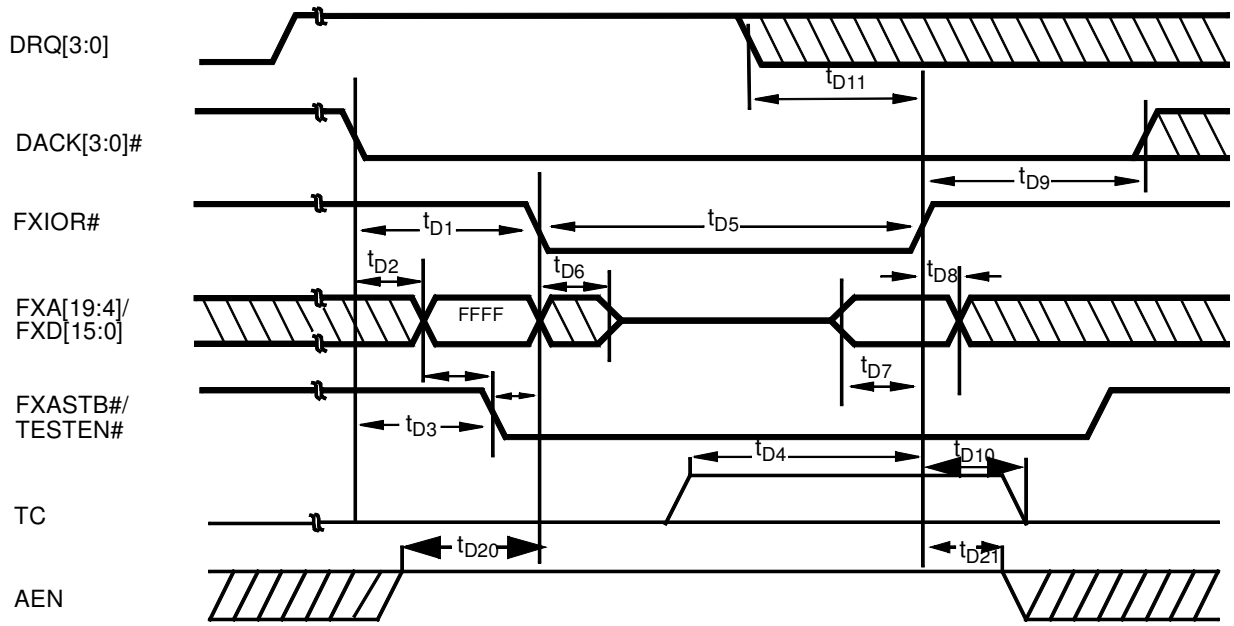


Figure 4.9 — DMA FX Bus Read Cycle

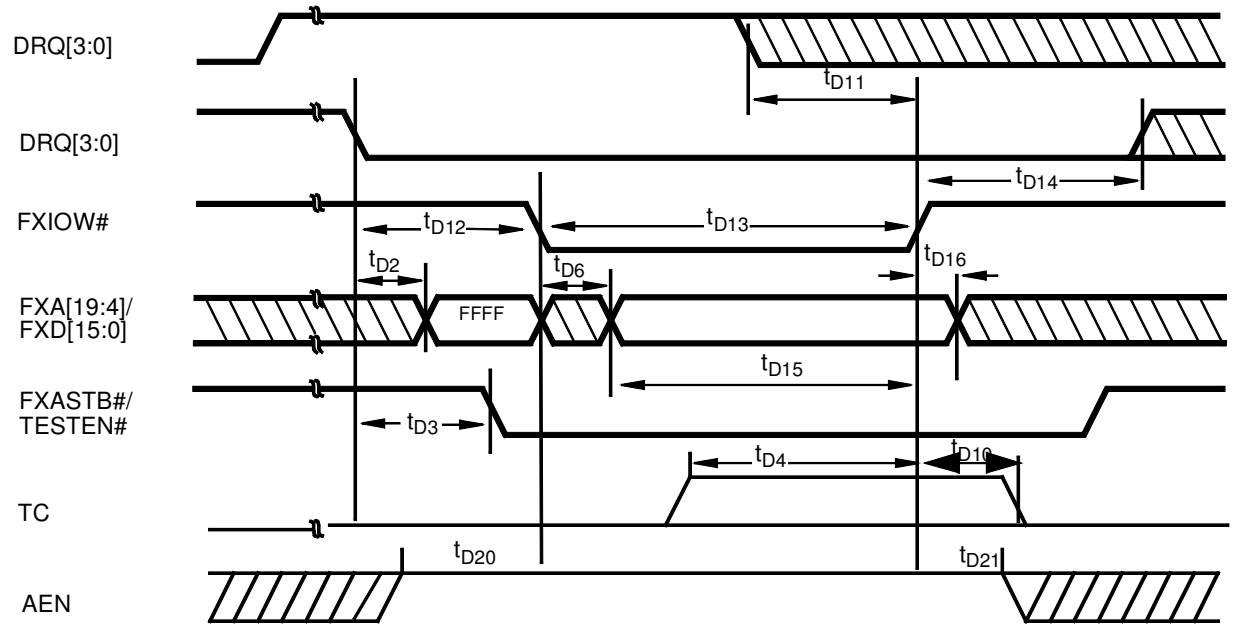


Figure 4.10 — DMA FX Bus Write Cycle

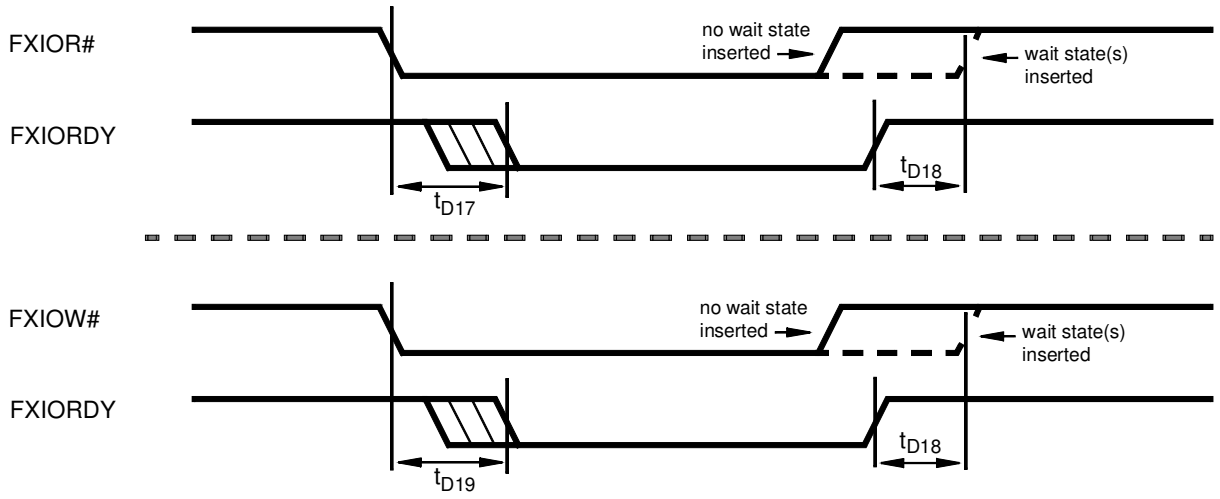


Figure 4.11 — DMA FX Bus Cycle Wait State Insertion

4.9 Fast External (FX) Bus Timing

Table 6.2 — FX Bus AC Timing Specification

#	Description	Min.	Max.
1	FXASTB# pulse width.	20 nsec	
2	FXA[19:4] setup time to the falling edge of FXASTB#	20 nsec	
3	FXA[19:4] hold time from the falling edge of FXASTB#	10 nsec	
4	FXA[20:0], BHE# setup time to the falling edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXS-MEMW#)	110 nsec	
5	FXCS[1:0]#, AUSIOCS#,KBCS#, ROMCS#, RTCCS# setup to the falling edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXS-MEMR# and/or FXSMEMW#)	60 nsec	
6	FXA[19:4]/FXD[15:0] TRI-STATE before the falling edge of the read command strobe (FXIOR#, FXMEMR# and/or FXSMEMR#)	0 nsec	
7	FXD[15:0] valid Write Data Out before the falling edge of the write command strobe (FXIOW#, FXMEMW# and/or FXSMEMR#)	20 nsec	
8	FXMEMCS16# setup to the memory command strobe (FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) to guarantee the proper cycle timing as well as proper data reading	0 nsec	
9	FXIOCS16# setup to the command strobe (FXIOR# or FXIOW#) to guarantee the proper cycle timing as well as proper data reading	-50 nsec	
10	8-bit Command Strobe (FXMEMR#, FXMEMW#, FXSMEMR# and/or FXS-MEMW#) pulse width. (NOTE: This is for the default timing of the FX Bus.)	520 nsec	
10	16-bit Command Strobe (FXMEMR#, FXMEMW#, FXSMEMR# and/or FXS-MEMW#) pulse width. (NOTE: This is for the default timing of the FX Bus.)	160 nsec	

Table 6.2 — FX Bus AC Timing Specification

#	Description	Min.	Max.
11	FXIORDY inactive low setup to the end of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) to insert additional wait states.	120 nsec	
12	Command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) active hold time from FXIORDY asserted active high	120 nsec	
13	Valid FXD[15:0] Read Data In setup time to the rising edge of the read command strobe (FXIOR#, FXMEMR# and/or FXSMEMR#).	100 nsec	
14	Valid FXD[15:0] Read Data In hold time from the rising edge of the read command strobe (FXIOR#, FXMEMR# and/or FXSMEMR#)	0 nsec	
15	FXMEMCS16#, FXIOCS16# valid hold time from the rising edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	0 nsec	
16	FXA[20, 3:0], BHE# hold time from the rising edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	20 nsec	
16	FXD[15:0] Write Data Out hold time from the rising edge of the write command strobe (FXIOW#, FXMEMW# and/or FXSMEMW#)	20 nsec	
16	FXASTB# inactive low hold time from the rising edge of the command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#)	20 nsec	
17	FXA[19:4]/FXD[15:0] TRI-STATE hold time following the rising edge of the read command strobe (FXIOR#, FXMEMR# and/or FXSMEMR#)	20 nsec	
18	Command strobe (FXIOR#, FXIOW#, FXMEMR#, FXMEMW#, FXSMEMR# and/or FXSMEMW#) going inactive to next active command strobe	170 nsec	
19	AEN Valid to FXIOR# or FXIOW# active command strobe	100 nsec	
20	AEN Valid from FXIOR# or FXIOW# active command strobe	30 nsec	

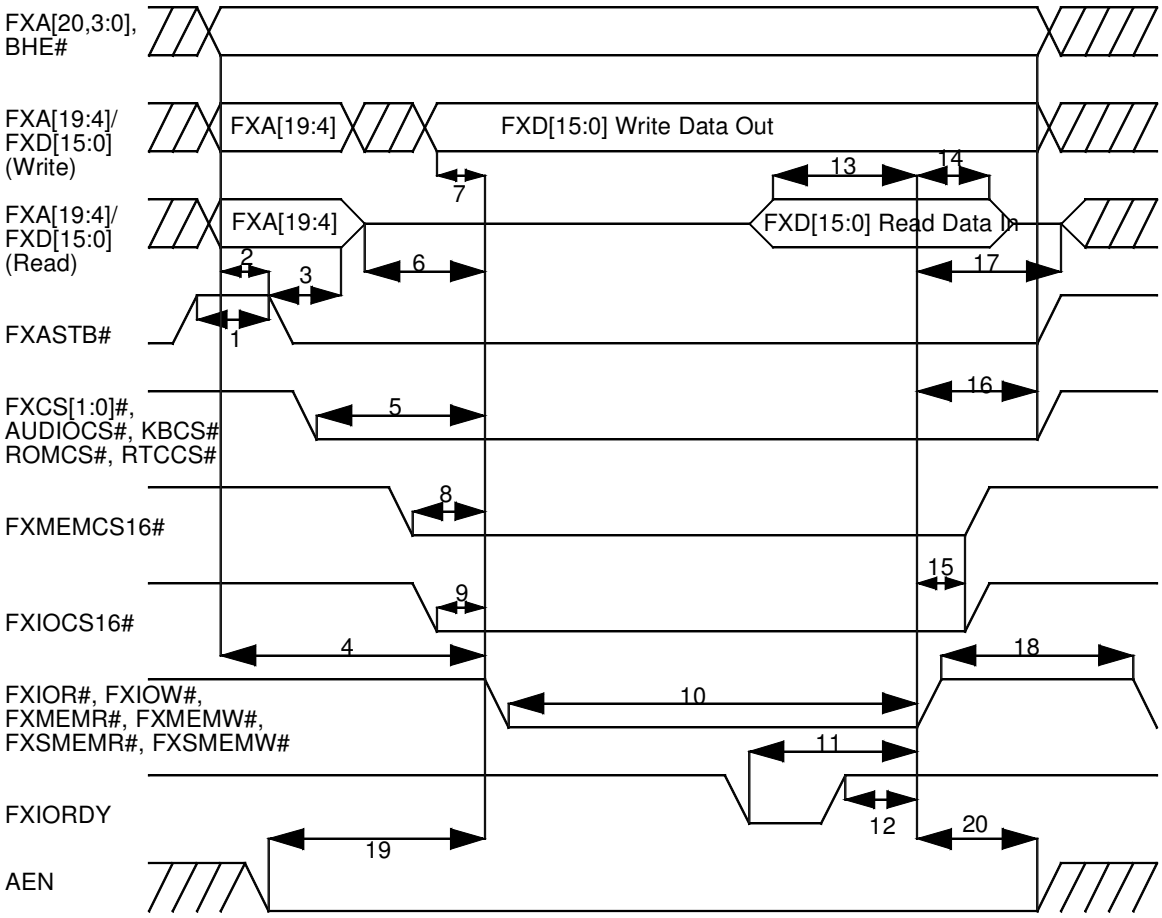


Figure 4.12 — FX Bus Timing

4.10 FDC Clock Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{ICP}	Internal Clock Period	*Table 1*		ns	
t_{DRP}	Data Rate Period	*Table 1*		ns	

Table 6.3 — Nominal t_{ICP} , t_{DRP} Values

MFM Data Rate	t_{DRP}	t_{ICP}	Value	Units
1 Mbps	1000	3 x t_{CP}	125	ns
500 kbps	2000	3 x t_{CP}	125	ns
300 kbps	3333	3 x t_{CP}	208	ns
250 kbps	4000	6 x t_{CP}	250	ns

4.11 FDC Write Data Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{HDH}	HDSEL# Hold from WGATE# Inactive	750			
t_{HDS}	HDSEL# Setup to WGATE# Active	100			
t_{WDW}	Write Data Pulse Width	*Table 3*			

Table 6.4 — Minimum t_{WDW} Values

Data Rates	t_{DRP}	t_{WDW}	t_{WDW} Value	Units
1 Mbps	1000	2 x t_{ICP}	250	ns
500 kbps	2000	2 x t_{ICP}	250	ns
300 kbps	3333	2 x t_{ICP}	375	ns
250 kbps	4000	2 x t_{ICP}	500	ns

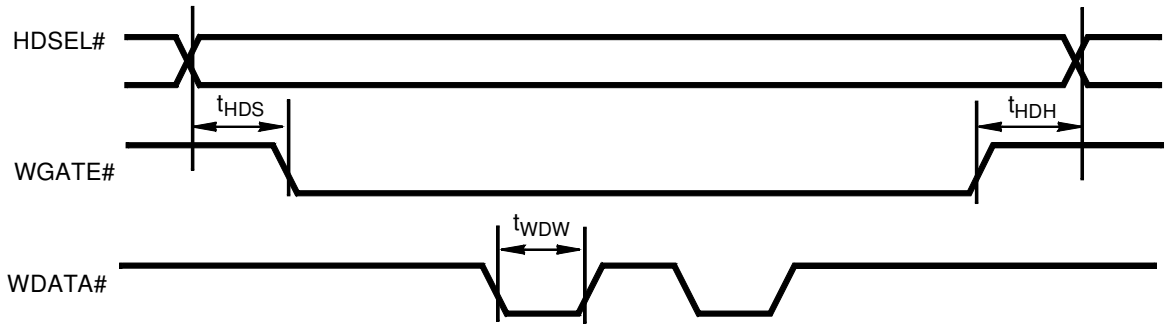


Figure 4.13 — Write Data Timing

4.12 FDC Read Data Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{RDW}	Read Data Pulse Width	50		ns	

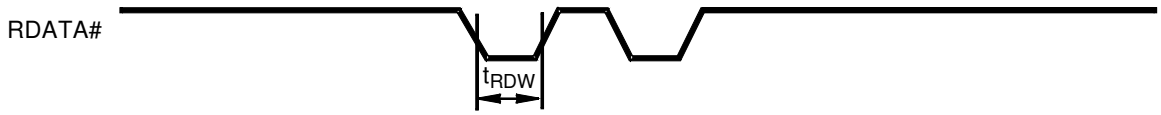


Figure 4.14 — Read Data Timing

4.13 FDC Drive Control Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{DRV}	DR0-3#, MTR0-3# from End of WR#		100	ns	
t_{DST}	DIR# Setup to STEP# Active	6			
t_{IW}	Index Pulse Width	100		ns	
t_{STD}	DIR# Hold from STEP# Inactive	t_{STR}		ms	
t_{STP}	STEP# Active High Pulse Width	8			
t_{STR}	STEP# Rate Time	1		ms	

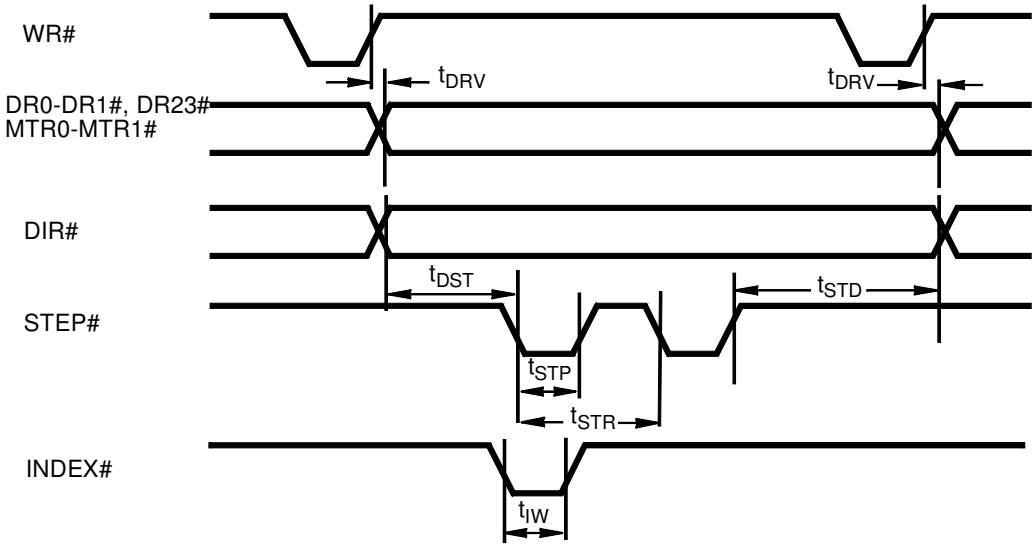


Figure 4.15 — Drive Control Timing

4.14 Reset Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{R-PCI}	RST# Active after PWRGOOD (to PCI Bus)	1		ms	
t_{R-CPU}	CPURST Active after PWRGOOD (to CPU)	2		ms	

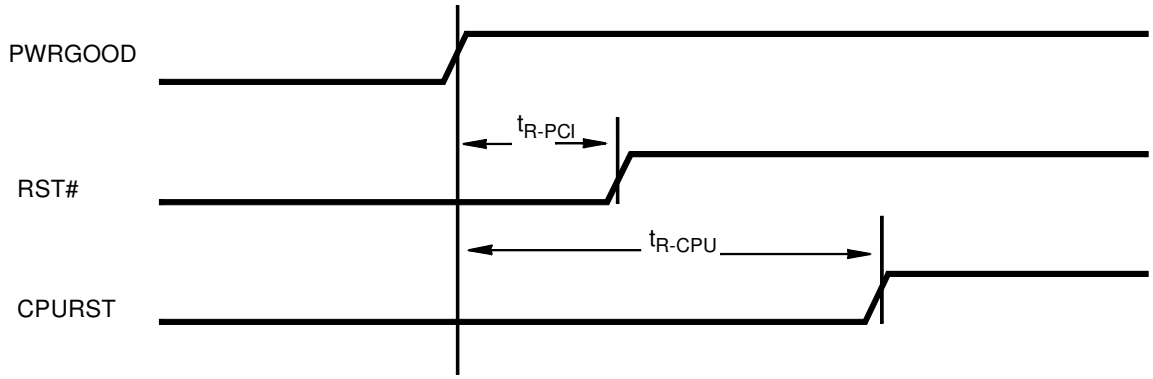


Figure 4.16 — Reset Timing

4.15 IDE Interface Timing for DMA Transfers

Symbol	Parameter	Min	Max	Units	Notes
t_{IDE_C}	IDE DMA DIOR# and DIOW# Access Cycle Time	120		ns	1
t_{IDE_CA}	IDE DIOR# and DIOW# Comand Strobe Active Time	70		ns	1
t_{IDE_CCH}	IDE CH1_DMACK# or CH2_DMACK# Hold Time from DIOR# or DIOW# Command Strobe rising	5		ns	
t_{IDE_CCS}	IDE CH1_DMACK# or CH2_DMACK# Setup Time to DIOR# or DIOW# Command Strobe falling	0		ns	
t_{IDE_CI}	IDE DIOR# and DIOW# Comand Strobe Inactive Time	25		ns	1
t_{IDE_CR}	IDE DIOR# or DIOW# Command Strobe active to CH1_DMREQ or CH2_DMREQ valid to indicate if another transfer cycle is to be performed		35	ns	
t_{IDE_RDH}	IDE Read Data Hold Time from DIOR# rising	5		ns	
t_{IDE_RDS}	IDE Read Data Setup Time to DIOR# rising	20		ns	
t_{IDE_RDZ}	IDE CH1_DMACK# or CH2_DMACK# inactive to Read Data TRI-STATE		25	ns	
t_{IDE_WDH}	IDE Write Data Hold Time from DIOW# rising	10		ns	
t_{IDE_WDS}	IDE Write Data Setup Time to DIOW# rising	20		ns	

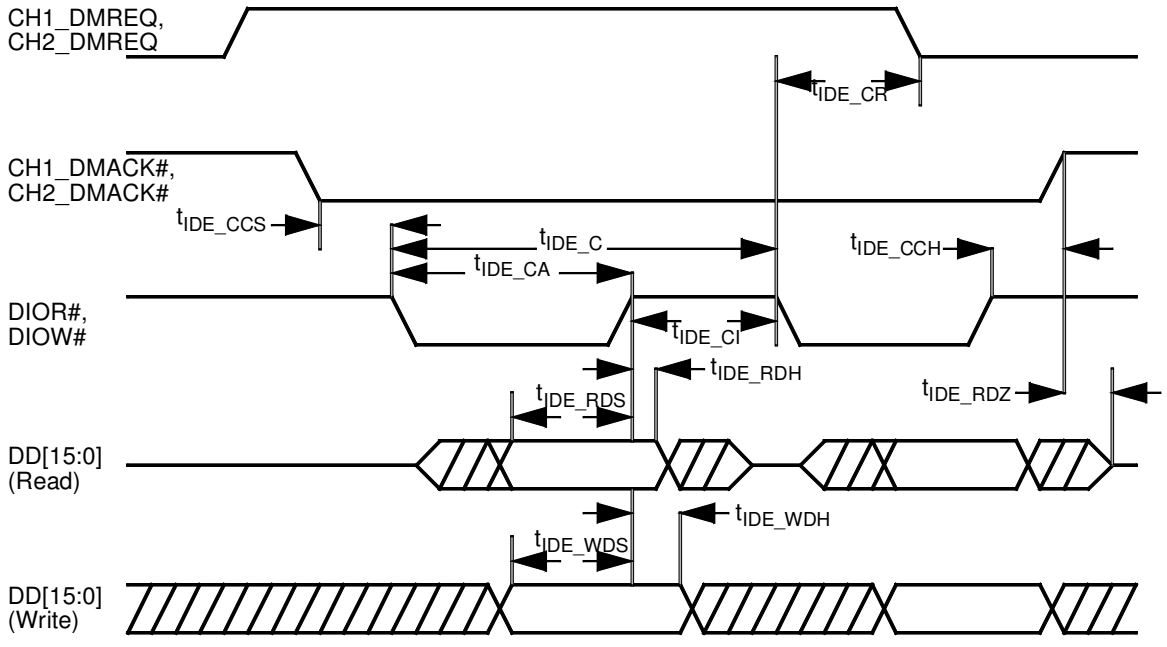


Figure 4.17 — IDE DMA Timing

NOTE 1: The IDE Command Strobe cycle time specification (t_{IDE_C}) is greater than the sum of the IDE Command Strobe active time specification (t_{IDE_CA}) and the IDE Command Strobe inactive time specification (t_{IDE_CI}). The PC87560 will guarantee each specificaion independant of the other two.

4.16 IDE Interface Timing for Programmed I/O (PIO) Transfers

Symbol	Parameter	Min	Max	Units	Notes
t_{IDE_ACH}	IDE DA[2:0] valid Hold Time from DIOR# and DIOW# Comand Strobe Active	5		ns	
t_{IDE_ACS}	IDE DA[2:0] valid Setup Time to DIOR# and DIOW# Comand Strobe Active	25		ns	
t_{IDE_C}	IDE DMA DIOR# and DIOW# Access Cycle Time	120		ns	1
t_{IDE_CA}	IDE DIOR# and DIOW# Comand Strobe Active Time	70		ns	1
t_{IDE_CI}	IDE DIOR# and DIOW# Comand Strobe Inactive Time	25		ns	1
t_{IDE_CIRY}	IDE DIOR# or DIOW# Command Strobe active to DIORDY valid to indicate if the cycle is to insert wait states		35	ns	
t_{IDE_PRDZ}	IDE DIOR# inactive to Read Data TRI-STATE		30	ns	
t_{IDE_RDH}	IDE Read Data Hold Time from DIOR# rising	5		ns	
t_{IDE_RDS}	IDE Read Data Setup Time to DIOR# rising	20		ns	
t_{IDE_RDRS}	IDE Read Data Setup Time to DIORDY rising	0		ns	
t_{IDE_WDH}	IDE Write Data Hold Time from DIOW# rising	10		ns	
t_{IDE_WDS}	IDE Write Data Setup Time to DIOW# rising	20		ns	

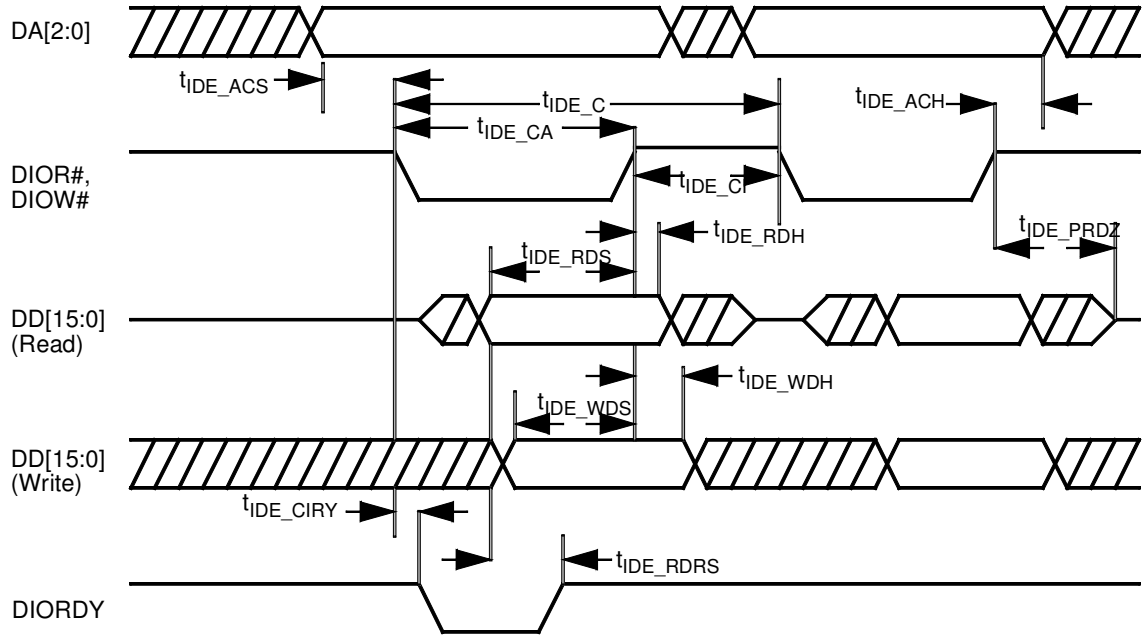


Figure 4.18 — IDE Programmed I/O (PIO) Timing

NOTE 1: The IDE Command Strobe cycle time specification (t_{IDE_C}) is greater than the sum of the IDE Command Strobe active time specification (t_{IDE_CA}) and the IDE Command Strobe inactive time specification (t_{IDE_CI}). The PC87560 will guarantee each specificaion independant of the other two.

5.0 Package Description

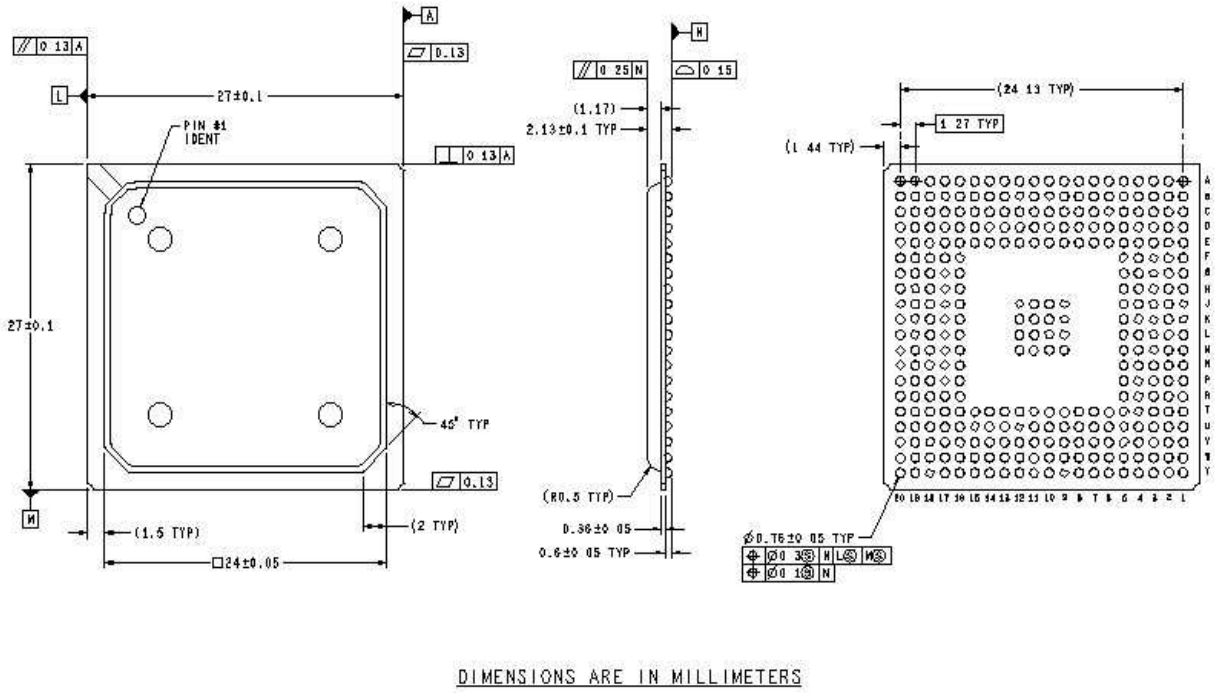


Figure 5.1 — 316 PBGA Package-NUBD316

6.0 Register Description

The PC87560 has both PCI configuration registers and non-configuration registers. The device has three configuration register sets, one for each function (that is, IDE Controller, I/O Peripherals and USB Controller). The non-configuration registers are accessed through the PCI bus and include all the standard I/O registers of devices such as DMA Controllers, Timers, Interrupt Controllers, Serial Ports, Parallel Port, Floppy Disk Controller, Power Management, and Advanced Configuration and Power Interface (ACPI) registers.

6.1 Configuration Registers

The PC87560 will acknowledge all PCI Bus Configuration cycles (by asserting DEVSEL# active low) when the IDSEL input is asserted high, address bits 1-0 of the Configuration cycle are both zeros and address bits 10-8 correspond to one of the three internal functions.

The configuration address format is as follows:

C/BE[3:0]# Byte Enable
AD[1:0] Configuration Cycle type
00b: PC87560 responds
01b: configuration cycle is forwarded to PCI bridge (PC87560 does not respond)
10b: **Reserved** (PC87560 does not respond)
11b: **Reserved** (PC87560 does not respond)
AD[7:2] 0-256 configuration registers
AD[10:8] 1-8 functions (only three supported)
000b: IDE Controller
001b: I/O Peripherals
010b: USB Controller
011b: **Reserved** (PC87560 does not respond)
100b: **Reserved** (PC87560 does not respond)
101b: **Reserved** (PC87560 does not respond)
110b: **Reserved** (PC87560 does not respond)
111b: **Reserved** (PC87560 does not respond)

The configuration registers can be accessed as byte, word(16 bits) or DWord (32 bits) quantities. In all of these accesses only byte enables are used, AD[1:0] is always 00b when accessing the configuration registers. All multi-byte fields use "little-endian" ordering (that is, lower addresses contain the least significant parts of the fields). Registers that are marked “**Reserved**” will be decoded and return zeros when read.
All bits defined as “**Reserved**” within PC87560’s PCI Configuration Registers will be read as zero and will be unaffected by writes, unless they specifically documented otherwise.

Table 6.1 — Function 000b (IDE) Configuration Registers

Reg. # (HEX)	R/W	Description
00-01	R	Vendor ID (100Bh)
02-03	R	Device ID (0002h)
04-05	R/W	Command Register (CMD)
06-07	R/W	Status Register (SR)
08	R	Rev ID (02h)
09	R/W	Programming Interface (PIF)
0A	R	Sub-Class Code (01h)
0B	R	Class code (01h)
0C	R/W	Cache Line Size
0D	R/W	Latency Timer
0E	R	Header Type (80h)
0F	R	**Reserved** (00h)
10-13	R/W	Base Address Register 0 (F0BAR0)

Table 6.1 — Function 000b (IDE) Configuration Registers

Reg. # (HEX)	R/W	Description
14-17	R/W	Base Address Register 1 (F0BAR1)
18-1B	R/W	Base Address Register 2 (F0BAR2)
1C-1F	R/W	Base Address Register 3 (F0BAR3)
20-23	R/W	Base Address Register 4 (F0BAR4)
24-3F	R	Reserved (all zeros)
40	R/W	IDE Control Register 1
41	R/W	IDE Control Register 2
42	R/W	IDE Control Register 3
43	R	Write Buffer Status
44	R/W	IDE Channel 1 Device 1 Data Read Timing Register
45	R/W	IDE Channel 1 Device 1 Data Write Timing Register
46-47	R	**Reserved** (0000h)
48	R/W	IDE Channel 1 Device 2 Data Read Timing Register
49	R/W	IDE Channel 1 Device 2 Data Write Timing Register
4A-4B	R	**Reserved** (0000h)
4C	R/W	IDE Channel 2 Device 1 Data Read Timing Register
4D	R/W	IDE Channel 2 Device 1 Data Write Timing Register
4E-4F	R	**Reserved** (0000h)
50	R/W	IDE Channel 2 Device 2 Data Read Timing Register
51	R/W	IDE Channel 2 Device 2 Data Write Timing Register
52-53	R	**Reserved** (0000h)
54	R/W	IDE Command and Control Block Timing Register
55	R/W	IDE Sector size
56-57		**Reserved** (0000h)
58		Channel 1 Drive 0 Device Control Register
59		Channel 1 Drive 0 Device Control Register
5A-5B		**Reserved** (0000h)
5C		Channel 2 Drive 0 Device Control Register
5D		Channel 1 Drive 0 Device Control Register
5E-FF		**Reserved** (all zeros)

Table 6.2 — Function 001b (I/O Peripherals) Configuration Registers

Reg. # (HEX)	R/W	Description
00-01	R	Vendor ID (100Bh)
02-03	R	Device ID (0011h or 000Eh, depending on the DACK0#/DOCKEN# strapping option)
04-05	R/W	Command Register (CMD)
06-07	R/W	Status Register (SR)
08	R	Rev ID (01h)
09	R/W	Programming Interface (PIF)
0A	R	Sub-Class Code (80h)
0B	R	Class code (06h)
0C	R/W	Cache Line Size
0D	R/W	Latency Timer
0E	R	Header Type (80h)
0F-3F	R	**Reserved** (all zeros)
40-43	R/W	FX Bus Region 0 Base Address Register
44-47	R/W	FX Bus Region 1 Base Address Register
48-4B	R/W	FX Bus Region 2 Base Address Register
4C-4F	R/W	Distributed DMA Remap Base Address Register
50-53	R/W	Fast Infrared (FIR) Scatter/Gather DMA Controller Base Address Register
54-57	R	**Reserved** (00000000h)
58-59	R/W	System Configuration Register
5A-5B	R/W	Function Enable Register For Decoding
5C	R/W	System I/O Configuration Register
5D	R/W	Special Function Enable Register
5E	R	Parallel Port Identification Register (PPDID)
5F	R/W	Parallel Port Mode Select Register
60	R	**Reserved** (00h)
61	R/W	DMA Routing Control Register 4
62	R/W	ROM Configuration Register
63	R/W	DMA Routing Control Register 1
64	R/W	DMA Routing Control Register 2
65	R/W	DMA Routing Control Register 3
66	R/W	DMA Channel Control Register
67-68	R/W	Interrupt Level/Edge triggering Control Register 1 and 2
69-71	R/W	Interrupt Routing Control Registers 1 - 9
72-73	R/W	Internal (FM Master Bus) Arbiter Control Register
74-75	R/W	FX Bus Region 2 Mask Register
76-77	R/W	FX Bus Timing Control
78	R/W	FX Bus Control Register
79	R/W	General Purpose I/O Configuration Register
7A	R/W	General Purpose I/O Direction Register
7B	R/W	Serial Interrupt Control Register
7C-7D	R/W	Serial Interrupt Enable Register

Table 6.2 — Function 001b (I/O Peripherals) Configuration Registers

Reg. # (HEX)	R/W	Description
7E	R/W	**Reserved Configuration Offset 7Eh Register** (01h)
7F	R/W	Audio Chip Select Control Register
80-83	R/W	FX Bus Memory Range Control Register 1
84-87	R/W	Keyboard Controller Base Address Register (KBCBAR)
88-8B	R/W	Advance Configuration and Power Interface Base Address Register (ACPIBAR)
8C-8F	R/W	Power Management Base Address Register (PMBAR0)
90-93	R/W	Floppy Disk Controller Base Address Register (FDCBAR)
94-97	R/W	Serial Port 1 Base Address Register (SP1BAR)
98-9B	R/W	Serial Port 2 Base Address Register (SP2BAR)
9C-9F	R/W	Parallel Port Base Address Register (PPBAR)
A0-FE		**Reserved.** (All zeros.)
FF		Output Internal Data Buses Control Register (Test Function ONLY)

Table 6.3 — Function 010b (USB) Configuration Registers

Reg. # (HEX)	R/W	Description
00-01	R	Vendor ID (100Bh)
02-03	R	Device ID (0012h)
04-05	R/W	Command Register (CMD)
06-07	R/W	Status Register (SR)
08	R	Rev ID (01h)
09	R/W	Programming Interface (PIF)
0A	R	Sub-Class Code (03h)
0B	R	Class code (0Ch)
0C	R/W	**Reserved** (00h)
0D	R/W	Latency Timer
0E	R	Header Type (80h)
0F	R	**Reserved** (00h)
10-13	R/W	Open HCI Base Address Register (OHCIBAR)
14-17	R/W	NSC USB Base Address Register (NUSBBAR)
18-3B	R	**Reserved** (all zeros)
3C	R/W	Interrupt Line Register
3D-FF	R	**Reserved** (all zeros)

6.1.1 VENDOR ID REGISTER

Configuration offset: 00h - 01h
Function: 000b, 001b and 010b
Attribute: Read only
Size: 16 bits
Default value: 100Bh

The Vendor ID Register contains the vendor identification number. This 16-bit register along with the Device ID Register uniquely identifies any PCI device. Writes to this register have no effect.

6.1.2 DEVICE ID REGISTER

6.1.2.1 Function 0 (IDE) Device ID

Configuration offset: 02h - 03h
Function: 000b
Attribute: Read only
Size: 16 bits
Default value: 0002h

The Device ID Register contains the National Semiconductor PCI device identification number for an IDE controller (0002h). Writes to this register have no effect.

6.1.2.2 Function 1 (I/O) Device ID

Configuration offset: 02h - 03h
Function: 001b
Attribute: Read only
Size: 16 bits
Default value: 0011h or 000Eh

The Device ID Register contains the National Semiconductor PCI device identification number for a PC87560 I/O peripheral. Writes to this register have no effect.

When the DACK0#/DOCKEN# strapping option is latched as a one, the PC87560 will respond to reads of this register with the value 0011h; indicating that it is in a NoteBook.

When the DACK0#/DOCKEN# strapping option is latched as a zero, the PC87560 will respond to reads of this register with the value 000Eh; indicating that it is in a Dock.

6.1.2.3 Function 2 (USB) Device ID

Configuration offset: 02h - 03h
Function: 010b
Attribute: Read only
Size: 16 bits
Default value: 0012h

The Device ID Register contains the National Semiconductor PCI device identification number for a PCI USB Host controller (0012h). Writes to this register have no effect.

6.1.3 COMMAND REGISTER

6.1.3.1 Function 0 (IDE) Command Register

Configuration offset: 04h - 05h
Function: 000b
Attribute: Read/Write
Size: 16 bits
Default value: 0005h

The command register provides coarse control over the IDE controller's ability to generate and respond to PCI cycles.

Bit 0: I/O Space. This bit is used to enable the device to respond to PCI I/O cycles.

0: Function 0 is disabled.
1: Function 1 is enabled (default value)

Bit 1: **Reserved.**

Bit 2: PCI Bus Master. Controls the device's ability to act as a master on the PCI bus.

0: Device cannot be PCI Bus master. This will disable all DMA operations even if internal IDE DMA is enabled.
1: Device can become a PCI Bus master. If this bit is set and internal IDE DMA is enabled then the device can become a PCI Bus master. (default value).

Bit 5-3: **Reserved.**

Bit 6: Parity Error (PERR#) response

0: Ignore parity error (default)
1: Respond to parity error

Bit 7: **Reserved.**

Bit 8: System Error (SERR#) response

0: Disable system error checking (default)
1: Enable system error checking

Bit 15-9: **Reserved.**

Bit 6 and Bit 8 of Function 0,1,2 Command Registers are logically ORed together to determine if PERR# and SERR# can be asserted.

6.1.3.2 Function 1 (I/O) Command Register

Configuration offset: 04h - 05h
Function: 001b
Attribute: Read/Write
Size: 16 bits
Default value: 000Fh

The command register provides coarse control over the PC87560 I/O Peripheral Function's ability to generate and respond to PCI cycles.

Bit 0: I/O Space. This bit is always 1, the PC87560 Function 1 devices will respond to PCI I/O cycles.

Bit 1: Memory Space. This bit is always 1, the PC87560 will respond to PCI Memory cycles.

Bit 2: PCI Bus Master. Controls the device's ability to act as a master on the PCI bus.

0: Device cannot be PCI Bus master. This will disable all Function 1 DMA operations even if internal Function 1 DMA is enabled.
1: Device can become a PCI Bus master. If this bit is set and internal Function 1 DMA is enabled then the device can become a PCI Bus master (default value).

Bit 3: Special Cycle Enable

0: Disable. The PC87560 ignores all PCI Special cycles
1: Enable. The PC87560 recognizes special cycles (Shutdown).

Bits 5-4: **Reserved.**

Bit 6: Parity Error (PERR#) response

0: Ignore parity error (default)
1: Respond to parity error

Bit 7: **Reserved.**

Bit 8: System Error (SERR#) response

0: Disable system error checking (default)
1: Enable system error checking

Bits 15-9: **Reserved.**

Bit 6 and Bit 8 of Function 0,1,2 Command Registers are logically ORed together to determine if PERR# and SERR# can be asserted.

6.1.3.3 Function 2 (USB) Command Register

Configuration offset: 04h - 05h
Function: 010b
Attribute: Read/Write
Size: 16 bits
Default value: 0000h

The command register provides coarse control over the PC87560 USB Host Controller Function's ability to generate and respond to PCI cycles.

Bit 0: I/O Space. This bit is reset to a zero, but may be written to a one to indicate support for I/O Space accesses.

Bit 1: Memory Space. This bit is reset to a zero, but may be written to a one to indicate support for Memory Space

accesses.

Bit 2: PCI Bus Master. Controls the USB Controllers ability to act as a master on the PCI Bus.

0: The PC87560's USB Host Controller cannot be PCI Bus master.
1: The PC87560's USB Host Controller can become a PCI Bus master.

Bits 5-3: Reserved.

Bit 6: Parity Error (PERR#) response

0: Ignore parity error (default)
1: Respond to parity error

Bit 7: Reserved.

Bit 8: System Error (SERR#) response

0: Disable system error checking (default)
1: Enable system error checking

Bits 15-9: Reserved.

Bit 6 and Bit 8 of Function 0,1,2 Command Registers are logically ORed together to determine if PERR# and SERR# can be asserted.

6.1.4 STATUS REGISTER (SR)

6.1.4.1 Function 0 (IDE) and Function 1 (I/O) Status Register

Configuration offset: 06h - 07h
Function: 000b and 001b
Attribute: Read/Write
Size: 16 bits
Default value: 0200h

The status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes to this register may cause bit(s) to be reset. A bit is reset to '0' whenever the register is written with a'1' in the corresponding bit location. Only one PCI Status register is implemented in the PC87560 for Function 0 and 1.

Bits 7-0: Reserved.

Bit 8: Data Parity Error Detected.

0: No parity error detected
1: Parity error detected

Bits 10-9: DEVSEL# timing. Always 01b, medium speed DEVSEL# assertion.

Bit 11: Signaled Target Abort

0: The device did not terminate a transaction with target abort.
1: The device has terminated a transaction with target abort.

Bit 12: Receive Target Abort

0: The device has not received a target abort.
1: The device has received a target abort when it was a master.

Bit 13: Received Master Abort

0: Transaction was not terminated with a master abort.
1: Transaction has been terminated with a master abort.

Bit 14: Signaled System Error (SERR#)

0: System error was not signaled
1: System error was signaled

Bit 15: Detected Parity Error (PERR#)

0: No parity error detected
1: Parity error detected

6.1.4.2 Function 2 (USB) Status Register

Configuration offset: 06h - 07h
Function: 010b

Attribute: Read/Write
Size: 16 bits
Default value: 0000h

The status register is used to record status information for PCI Bus related events. Reads to this register behave normally. Writes to this register may cause bit(s) to be reset. A bit is reset to zero whenever a one is written to the corresponding bit location.

Bits 7-0: Reserved.

Bit 8: Data Parity Error Detected.

0: No parity error detected
1: Parity error detected

Bits 10-9: DEVSEL# timing. Always 01b, medium speed DEVSEL# assertion.

Bit 11: Signaled Target Abort

0: The device did not terminate a transaction with target abort.
1: The device has terminated a transaction with target abort.

Bit 12: Receive Target Abort

0: The device has not received a target abort.
1: The device has received a target abort when it was a master.

Bit 13: Received Master Abort

0: Transaction was not terminated with a master abort.
1: Transaction has been terminated with a master abort.

Bit 14: Signaled System Error (SERR#)

0: System error was not signaled
1: System error was signaled

Bit 15: Detected Parity Error (PERR#)

0: No parity error detected
1: Parity error detected

6.1.5 REV ID REGISTER

6.1.5.1 Function 0 (IDE) Revision ID Register

Configuration offset: 08h
Function: 000b
Attribute: Read only
Size: 8 bits
Default value: 02h

This 8-bit register contains the revision number for the IDE Function in the PC87560.

6.1.5.2 Function 1 (I/O) Revision ID Register

Configuration offset: 08h
Function: 001b
Attribute: Read only
Size: 8 bits
Default value: 01h

This 8-bit register contains the revision number for the SIO Function in the PC87560. One may view this as the PC87560's generic revision number

6.1.5.3 Function 2 (USB) Revision ID Register

Configuration offset: 08h
Function: 010b
Attribute: Read only
Size: 8 bits
Default value: 01h

This 8-bit register contains the revision number (01h) for the USB Controller Function in the PC87560.

6.1.6 FUNCTION 0 (IDE) PROGRAMMING INTERFACE (PIF) REGISTER

Configuration offset: 09h
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: 8Ah

The Programming Interface byte of the Class Code register indicates whether the device supports legacy and/or native mode. There is a pair of bits per IDE channel in the Programming Interface register that indicate to the BIOS which mode(s) the device supports. Bits 0 and 1 of the Programming Interface register correspond to channel 1, bits 2 and 3 correspond to channel 2 (see Programming Interface Register description for details of each bit).

When the device is programmed in legacy mode, the device will respond to the following addresses:

Primary: 1F0h - 1F7h, 3F6h

Secondary:170h - 177h, 376h

When Channel 1 is in legacy mode, the Base Address Registers 0-1 are not used, and when Channel 2 is legacy mode Base Address Registers 2-3 are not used When in legacy mode, each channel can be disabled independently by software. To turn off a legacy channel, software writes a one to the mode bit of the Programming Interface register (bits 0 or 2). When a channel is in native mode, it will not respond to legacy addresses, but will claim addresses defined by the Base Address Register 0-1 for Channel 1 and Base Address Register 2-3 for Channel 2.

Bit 0: This bit determines what addresses Channel 1 responds to. The default value is 0.

0: Channel 1 responds to addresses 1F0h-1F7h and 3F6h. Base registers 0 and 1 (10h-17h) are not used -legacy mode.
1: Channel 1 responds to addresses programmed in base register 0 and 1 - native mode.

Bit 1: Always 1. Channel 1 has programmable selection of modes. Bit 0 determines which mode (default). This bit is read only.

Bit 2: This bit determines what addresses channel 2 responds to. The default value is 0.

0: Channel 2 responds to addresses 170-177h and 376h. Base registers 2 and 3 (18h-1Fh) are not used - legacy mode.
1: Channel 2 responds to addresses programmed in base register 2 and 3 - native mode.

Bit 3: Always 1. Channel 2 has programmable selection of modes. Bit 2 determines which mode (default). This bit is read only.

Bits 6-4: Reserved.

Bit 7: Always 1. Indicating that the device supports Master IDE.

6.1.7 FUNCTION 0 (IDE) SUB-CLASS CODE REGISTER

Configuration offset: 0Ah
Function: 000b
Attribute: Read only
Size: 8 bits
Default value: 01h

The device indicates to BIOS, that Function 0 is an IDE device by returning 01h in the Class code byte (indicating that it is a mass storage controller) and a 01h in the Sub-Class code byte (indicating that it is an IDE controller) of the Class Code register.

6.1.8 FUNCTION 0 (IDE) CLASS CODE REGISTER

Configuration offset: 0Bh
Function: 000b
Attribute: Read only
Size: 8 bits
Default value: 01h

Class code byte indicating that it is a mass storage controller.

6.1.9 FUNCTION 1 (I/O) PROGRAMMING INTERFACE (PIF) REGISTER

Configuration offset: 09h
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

TBD

6.1.10 FUNCTION 1 (I/O) SUB-CLASS CODE REGISTER

Configuration offset: 0Ah
Function: 001b
Attribute: Read only
Size: 8 bits
Default value: 80h

The Sub-class code indicated that the PC87560 is a SuperIO bridge device.

6.1.11 FUNCTION 1 (I/O) CLASS CODE REGISTER

Configuration offset: 0Bh
Function: 001b
Attribute: Read only
Size: 8 bits
Default value: 06h

The Class code indicates that the PC87560 is a bridge device.

6.1.12 FUNCTION 2 (USB) PROGRAMMING INTERFACE (PIF) REGISTERS

Configuration offset: 09h
Function: 010b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

TBD

6.1.13 FUNCTION 2 (USB) SUB-CLASS CODE REGISTER

Configuration offset: 0Ah
Function: 010b
Attribute: Read only
Size: 8 bits
Default value: 03h

The Sub-class code indicated that this function is an Universal Serial Bus Controller.

6.1.14 FUNCTION 2 (USB) CLASS CODE REGISTER

Configuration offset: 0Bh
Function: 010b
Attribute: Read only
Size: 8 bits
Default value: 0Ch

The Class code indicates that this function is a serial bus controller.

6.1.15 FUNCTION 0 (IDE) CACHE LINE SIZE REGISTER

Configuration offset: 0Ch
Function: 000b
Attribute: Read/write
Size: 8 bits
Default value: 00h

If the value 08h is written to this register, the PC87560 IDE Controller will perform PCI Memory Read Line and PCI Memory Write and Invalidate cycles whenever possible, when the IDE Controller becomes a PCI Bus master.

If any value other than 08h is in this register, the PC87560 IDE Controller will only use PCI Memory Read and PCI Memory Write cycles to perform IDE DMA transfers.

6.1.16 LATENCY TIMER REGISTERS

6.1.16.1 Function 0 & 1 (IDE & I/O) Latency Timer Register

Configuration offset: 0Dh
Function: 000b & 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

This register specifies, in units of PCI bus clocks, the value of an 8-bit Latency Timer for all of the PC87560 functions. It should be noted that it is only accessible via the Function 0 and Function 1 Configuration Offset 0Dh (that means that writes to Function 2 Configuration Offset 0Dh will not effect this register or the Latency Timer value used for any of the functions; that includes the Latency Timer value used for Function 2 itself.) Only PCI Master modules that can transfer more than two Double-Words will ever use this Latency Timer. In the PC87560, this means that the IDE Controller (Function 0), the FIR Scatter/Gather DMA (of Function 1) and USB Host Controller (Function 2) may all be effected by this Latency Timer. Once the Latency Timer times-out, an IDE, a FIR Scatter/Gather DMA, or USB controlled PCI transfer will be terminated on the earliest appropriate data phase.

6.1.16.2 Function 2 (USB) Latency Timer Register

Configuration offset: 0Dh
Function: 010b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

This register serves no function in the PC87560; it is suggested for consistency reasons that this register is always programmed to the same value as the Function 0 & 1 Latency Timer Register (that register will actually control the value used by the Latency Timer for all PC87560 PCI Bus Master transfers, including those of the USB Host Controller).

6.1.17 HEADER TYPE REGISTERS

Configuration offset: 0Eh
Function: 000b, 001b and 010b
Attribute: Read only
Size: 8 bits
Default value: 80h

The PC87560 is a multi-function device and uses header type 80 as defined in the PCI Specification.

6.1.18 FUNCTION 0 (IDE) BASE ADDRESS REGISTER 0 (F0BAR0)

Configuration offset: 10h - 13h
Function: 000b
Attribute: Read/Write
Size: 32 bits
Default value: FFFFFFF9h

Used for IDE Channel 1 data/command block accesses if Channel 1 is programmed to be in native mode. The device decodes 8 bytes of address space for data/command block accesses.

Bit 0: Always 1. Indicating that IDE Channel 1 data/command block accesses are mapped into PCI I/O space.

Bits 2-1: Always 00. Indicating that this base address register requires an 8-byte I/O address space.

Bits 31-3: The upper 29 bits of the base address are read/write bits that allow IDE Channel 1 data/command accesses to be located anywhere in the system I/O space and can be placed on any 8-byte boundary, with an 8-byte range.

6.1.19 FUNCTION 0 (IDE) BASE ADDRESS REGISTER 1 (F0BAR1)

Configuration offset: 14h - 17h
Function: 000b
Attribute: Read/Write
Size: 32 bits
Default value: FFFFFFFDh

Used for IDE Channel 1 control block accesses if Channel 1 is programmed to be in native mode. The device decodes 4 bytes of address space for control block accesses.

Bit 0: Always 1. Indicating that IDE Channel 1 control block accesses are mapped into PCI I/O space.

Bit 1: Always 0. Indicating that this base address register requires an 4-byte I/O address space.

Bits 31-2: The upper 30 bits of the base address are read/write bits that allow IDE Channel 1 control accesses to be located anywhere in the system I/O space and can be placed on any 4-byte boundary, with an 4-byte range.

6.1.20 FUNCTION 0 (IDE) BASE ADDRESS REGISTER 2 (F0BAR2)

Configuration offset: 18h - 1Bh
Function: 000b
Attribute: Read/Write
Size: 32 bits
Default value: FFFFFFF9h

Used for IDE Channel 2 data/command block accesses if Channel 2 is programmed to be in native mode. The device decodes 8 bytes of address space for data/command block accesses.

Bit 0: Always 1. Indicating that IDE Channel 2 data/command block accesses are mapped into PCI I/O space.

Bits 2-1: Always 00. Indicating that this base address register requires an 8-byte I/O address space.

Bits 31-3: The upper 29 bits of the base address are read/write bits that allow IDE Channel 2 data/command accesses to be located anywhere in the system I/O space and can be placed on any 8-byte boundary, with an 8-byte range.

6.1.21 FUNCTION 0 (IDE) BASE ADDRESS REGISTER 3 (F0BAR3)

Configuration offset: 1Ch - 1Fh
Function: 000b
Attribute: Read/Write
Size: 32 bits
Default value: FFFFFFFDh

Used for IDE Channel 2 control block accesses if Channel 2 is programmed to be in native mode. The device decodes 4 bytes of address space for control block accesses.

Bit 0: Always 1. Indicating that IDE Channel 2 control block accesses are mapped into PCI I/O space.

Bit 1: Always 0. Indicating that this base address register requires an 4-byte I/O address space.

Bits 31-2: The upper 30 bits of the base address are read/write bits that allow IDE Channel 2 control accesses to be

located anywhere in the system I/O space and can be placed on any 4-byte boundary, with an 4-byte range.

6.1.22 FUNCTION 0 (IDE) BASE ADDRESS REGISTER 4 (F0BAR4)

Configuration offset: 20h - 23h
Function: 000b
Attribute: Read/Write
Size: 32 bits
Default value: FFFFFFF1h

Used to address the Bus Master IDE control and status registers. The device decodes 16 bytes of address space for control block accesses.

Bit 0: Always 1. Indicating that the Bus Master IDE control and status registers are mapped into PCI I/O space.

Bits 3-1: Always 000. Indicating that this base address register requires a 16-byte I/O address space.

Bits 31-4: The upper 28 bits of the base address are read/write bits that allow the Bus Master IDE control and status registers to be located anywhere in the system I/O space and can be placed on any 16-byte boundary, with a 16-byte range.

6.1.23 FUNCTION 0 IDE CONTROL REGISTER 1

Configuration offset: 40h
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

The control register provide control of the IDE function.

Bit 0: **Reserved**. Always 0

Bit 1: 0: DRST# pin is 1

1:DRST# pin is 0

Bits 3-2: **Reserved.**

Bit 4: Channel 1 drive 1 IDE/ATAPI buffer mode

0: Normal IDE prefetch buffer mode (default)
1: ATAPI buffer mode (no prefetching)

Bit 5: Channel 1 drive 2 IDE/ATAPI buffer mode

0: Normal IDE prefetch buffer mode (default)
1: ATAPI buffer mode (no prefetching)

Bit 6: Channel 2 drive 1 IDE/ATAPI buffer mode

0: Normal IDE prefetch buffer mode (default)
1: ATAPI buffer mode (no prefetching)

Bit 7: Channel 2 drive 2 IDE/ATAPI buffer mode

0: Normal IDE prefetch buffer mode (default)
1: ATAPI buffer mode (no prefetching)

6.1.24 FUNCTION 0 IDE CONTROL REGISTER 2

Configuration offset: 41h
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

The control register provide control of the IDE function.

Bit 0: Channel 1 Interrupt.

0: Unmasked

1: Masked

Bit 1: Channel 2 Interrupt.

0: Unmasked

1: Masked

Bit 2: PCI Base Address Registers 2 and 3.

0: Enabled

1: Disabled

Bit 3: PCI Data Phase WATCHDOG Timer.

0: Disabled.

1: Enabled

Bit 4: Base Address Registers 10h and 14h Data Buffer Bypass.

0: All accesses mapped to Base Address Register 10h and 14h bypass the data buffers.

1: IDE device accesses (Control Register Bit 14=0) to offset 0 of the base address window register 10h and 14h are buffered.

Bit 5: Base Address Registers 18h and 1Ch Data Buffer Bypass.

0: All accesses mapped to Base Address Register 18h and 1Ch bypass the data buffers.

1: IDE device accesses (Control Register bit 15=0) to offset 0 of the base address window register 18h and 1Ch are buffered.

Bits 7-6: Reserved.

6.1.25 FUNCTION 0 IDE CONTROL REGISTER 3

Configuration offset: 42h
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

The control register provide control of the IDE function.

Bit 0: Channel 1 Pre-fetch Buffer.

0: Disabled

1: Enabled

Bit 1: Channel 2 Pre-fetch Buffer.

0: Disabled

1: Enabled

Bit 2: **Reserved.**

Bit 3: Number of PCI Master Wait States inserted during PCI Memory Bursts

0: One

1: Zero

Bit 4: Channel 1 Drive 1 IORDY or DMREQ/DMACK Handshake for Flow Control.

0: Channel 1 drive 1 IORDY handshaking for flow control

1: Channel 1 drive 1 DMREQ/DMACK handshaking for flow control

Bit 5: Channel 1 Drive 2 IORDY or DMREQ/DMACK Handshake for Flow Control.

0: Channel 1 drive 2 IORDY handshaking for flow control

1: Channel 1 drive 2 DMREQ/DMACK handshaking for flow control

Bit 6: Channel 2 Drive 1 IORDY or DMREQ/DMACK Handshake for Flow Control.

0: Channel 2 drive 1 IORDY handshaking for flow control

1: Channel 2 drive 1 DMREQ/DMACK handshaking for flow control

Bit 7: Channel 2 Drive 2 IORDY or DMREQ/DMACK Handshake for Flow Control.

0: Channel 2 drive 2 IORDY handshaking for flow control

1: Channel 2 drive 2 DMREQ/DMACK handshaking for flow control

6.1.26 FUNCTION 0 (IDE) WRITE BUFFER STATUS

Configuration offset: 43h
Function: 000b
Attribute: Read only
Size: 8 bits
Default value: 00h

This status information is used for power management. Before the software attempts to turn off power to the IDE drives it must ensure that the write buffer is empty.

Bit 0: Channel 1 Write Buffer Status.

0: Channel 1 write buffer empty

1: Channel 1 write buffer not empty

Bit 1: Channel 2 Write Buffer Status.

0: Channel 2 write buffer empty

1: Channel 2 write buffer not empty

Bits 7-2: Reserved.

6.1.27 FUNCTION 0 IDE CHANNEL 1 DEVICE 1 DATA READ TIMING REGISTER

Configuration offset: 44h
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: 85h

All reads from the IDE Channel 1 Device 1 data register (offset 0) are always 16 bits and use this timing registers.

Bits 3-0: Command active time (in PCI clock periods) for Channel 1 Device 1 read from data port.

Bits 7-4: Command recovery time (in PCI clock periods) for Channel 1 Device 1 read from data port.

6.1.28 FUNCTION 0 IDE CHANNEL 1 DEVICE 1 DATA WRITE TIMING REGISTER

Configuration offset: 45h
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: 85h

All writes to the IDE Channel 1 Device 1 data register (offset 0) are always 16 bits and use this timing registers.

Bits 3-0: Command active time (in PCI clock periods) for Channel 1 Device 1 write to data port.

Bits 7-4: Command recovery time (in PCI clock periods) for Channel 1 Device 1 write to data port.

6.1.29 FUNCTION 0 IDE CHANNEL 1 DEVICE 2 DATA READ TIMING REGISTER

Configuration offset: 48h
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: 85h

All reads from the IDE Channel 1 Device 2 data register (offset 0) are always 16 bits and use this timing registers.

Bits 3-0: Command active time (in PCI clock periods) for Channel 1 Device 2 read from data port.

Bits 7-4: Command recovery time (in PCI clock periods) for Channel 1 Device 2 read from data port.

6.1.30 FUNCTION 0 IDE CHANNEL 1 DEVICE 2 DATA WRITE TIMING REGISTER

Configuration offset: 49h
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: 85h

All writes to the IDE Channel 1 Device 2 data register (offset 0) are always 16 bits and use this timing registers.

Bits 3-0: Command active time (in PCI clock periods) for Channel 1 Device 2 write to data port.

Bits 7-4: Command recovery time (in PCI clock periods) for Channel 1 Device 2 write to data port.

6.1.31 FUNCTION 0 IDE CHANNEL 2 DEVICE 1 DATA READ TIMING REGISTER

Configuration offset: 4Ch
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: 85h

All reads from the IDE Channel 2 Device 1 data register (offset 0) are always 16 bits and use this timing registers.

Bits 3-0: Command active time (in PCI clock periods) for Channel 2 Device 1 read from data port.

Bits 7-4: Command recovery time (in PCI clock periods) for Channel 2 Device 1 read from data port.

6.1.32 FUNCTION 0 IDE CHANNEL 2 DEVICE 1 DATA WRITE TIMING REGISTER

Configuration offset: 4Dh
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: 85h

All writes to the IDE Channel 2 Device 1 data register (offset 0) are always 16 bits and use this timing registers.

Bits 3-0: Command active time (in PCI clock periods) for Channel 2 Device 1 write to data port.

Bits 7-4: Command recovery time (in PCI clock periods) for Channel 2 Device 1 write to data port.

6.1.33 FUNCTION 0 IDE CHANNEL 2 DEVICE 2 DATA READ TIMING REGISTER

Configuration offset: 50h
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: 85h

All reads from the IDE Channel 2 Device 2 data register (offset 0) are always 16 bits and use this timing registers.

Bits 3-0: Command active time (in PCI clock periods) for Channel 2 Device 2 read from data port.

Bits 7-4: Command recovery time (in PCI clock periods) for Channel 2 Device 2 read from data port.

6.1.34 FUNCTION 0 IDE CHANNEL 2 DEVICE 2 DATA WRITE TIMING REGISTER

Configuration offset: 51h
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: 85h

All writes to the IDE Channel 2 Device 2 data register (offset 0) are always 16 bits and use this timing registers.

Bits 3-0: Command active time (in PCI clock periods) for Channel 2 Device 2 write to data port.

Bits 7-4: Command recovery time (in PCI clock periods) for Channel 2 Device 2 write to data port.

6.1.35 FUNCTION 0 IDE COMMAND AND CONTROL BLOCK TIMING REGISTER

Configuration offset: 54h

Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: B7h
All IDE command and control block accesses are 8-bits and use this register to control their timing.

Bits 3-0: Command/Control active time (in PCI clock periods).

Bits 7-4: Command/Control recovery time (in PCI clock periods).

6.1.36 FUNCTION 0 IDE SECTOR SIZE

Configuration offset:55h
Function: 000b
Attribute: Read/Write
Size: 8 bits
Default value: EEh

Bits 3-0: Channel 1 sector size

1111: Not used

1110: 512 bytes

1100: 1024 bytes

1000: 2048 bytes

0000: 4096 bytes

Bits 7-4: Channel 2 sector size

1111: Not used

1110: 512 bytes

1100: 1024 bytes

1000: 2048 bytes

0000: 4096 bytes

6.1.37 FUNCTION 0 (IDE) CHANNEL 1 DRIVE 0 DEVICE CONTROL REGISTER

Configuration offset: 58h
Function: 000b
Attribute: Read Only
Size: 8 bits
Default value: xx

This register holds the data of the last write to the Channel 1 Drive 0 device Control Register.

6.1.38 FUNCTION 0 (IDE) CHANNEL 1 DRIVE 1 DEVICE CONTROL REGISTER

Configuration offset: 59h
Function: 000b
Attribute: Read Only
Size: 8 bits
Default value: xx

This register holds the data of the last write to the Channel 1 Drive 1 device Control Register.

6.1.39 FUNCTION 0 (IDE) CHANNEL 2 DRIVE 0 DEVICE CONTROL REGISTER

Configuration offset: 5Ch
Function: 000b
Attribute: Read Only
Size: 8 bits
Default value: xx

This register holds the data of the last write to the Channel 2 Drive 0 device Control Register.

6.1.40 FUNCTION 0 (IDE) CHANNEL 2 DRIVE 1 DEVICE CONTROL REGISTER

Configuration offset: 5Dh
Function: 000b
Attribute: Read Only
Size: 8 bits
Default value: xx

This register holds the data of the last write to the Channel 2 Drive 1 device Control Register.

6.1.41 FUNCTION 1 (I/O) FX BUS REGION 0 BASE ADDRESS REGISTER

Configuration offset: 40h-43h
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

This register serves as an address window for the FX bus Chip Select 0 (FXCS[0]#). PCI I/O accesses to this address window, if enabled, generate DEVSEL# and forward the cycle to the FX bus. The size of the window is programmable from 8 bytes to 64 bytes.

Bit 0: FX Bus Region 0 Address Window Enable.

0: Disabled
1: Enabled

Bits 2-1: Window size

Bit 2	Bit 1	Window size
0	0	8 bytes
0	1	16 bytes
1	0	32 bytes
1	1	64 bytes

Bits 31-3: FX Bus Window address. This corresponds to the PCI addresses AD[31:3]. Decoding of bits 5-3 are defined as follows:

Window size	Bit 5	Bit 4	Bit 3
8 bytes	decoded	decoded	decoded
16 bytes	decoded	decoded	not used
32 bytes	decoded	not used	not used
64 bytes	not used	not used	not used

6.1.42 FUNCTION 1 (I/O) FX BUS REGION 1 BASE ADDRESS REGISTER

Configuration offset: 44h-47h
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

This register serves as an address window for the FX bus Chip Select 1 (FXCS[1]#). PCI I/O accesses to this address window, if enabled, generate DEVSEL# and forward the cycle to the FX bus. The size of the window is programmable from 8 bytes to 64 bytes.

Bit 0: FX Bus Region 1 Address Window Enable.

0: Disabled
1: Enabled

Bits 2-1: Window size

Bit 2	Bit 1	Window size
0	0	8 bytes
0	1	16 bytes
1	0	32 bytes
1	1	64 bytes

Bits 31-3: FX Bus Window address. This corresponds to the PCI addresses AD[31:3]. Decoding of bits 5-3 are defined as follows:

Window size	Bit 5	Bit 4	Bit 3
8 bytes	decoded	decoded	decoded
16 bytes	decoded	decoded	not used
32 bytes	decoded	not used	not used
64 bytes	not used	not used	not used

6.1.43 FUNCTION 1 (I/O) FX BUS REGION 2 BASE ADDRESS REGISTER

Configuration offset: 48h-4Bh
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

This register serves as an address window for the FX bus. PCI I/O accesses to this address window, if enabled, generate DEVSEL# and forward the cycle to the FX bus. No FX bus chip selects are asserted during this cycle. The size of the window is programmable through the FX Bus Region 2 Mask Register (Function 1 configuration offset 74h-75h).

Bit 0: FX Bus Region 2 Address Window Enable.

0: Disabled
1: Enabled

Bits 31-1: FX Bus Region 2 Base address. This corresponds to the PCI addresses AD[31:1].

6.1.44 FUNCTION 1 (I/O) DISTRIBUTED DMA REMAP BASE ADDRESS REGISTER

Configuration offset: 4Ch - 4Fh
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

Bit 0: Global DMA Channel Remapping Enable

0: DMA remapping disabled. All accesses to DMA legacy addresses are forwarded to the internal Legacy 8237 DMA Controller.
1: DMA remapping enabled. Individual Legacy 8237 DMA channels can be remapped based upon the state of the bits in the DMA Channel Control Register (Function 1, configuration register offset 66h).

Bit 1: Distributed DMA Slave vs. Legacy DMA

If the Global DMA Channel Remapping bit is a one, this bit should always be a zero.

0: Distributed DMA Slave Mode disabled. The PC87560 DMA registers will be accessible only via their Legacy addresses. If Bit 0 of this register is a one, then the registers associated with channels that have corresponding zeros in the DMA Channel Control Register (Function 1, configuration register offset 66h) will be accessible via their Legacy I/O addresses. If Bit 0 of this register is a zero, then all of the PC87560 DMA resisters will be accessible via their Legacy I/O addresses.
1: Distributed DMA Slave Mode enabled. The PC87560 DMA registers will only be accessible via their remapped Distributed DMA I/O addresses. This bit and Bit 0 of this register should never both be one at the same time. When this bit is set to a one, the registers associated with the channels that have corresponding ones in the DMA CHannel Control Register (Function 1, configuration register offset 66h) will

be accessible via their Distributed DMA I/O addresses.

Bits 6-2: **Reserved.** Always zeros.

Bits 31-7: Base address of remapped legacy DMA registers. Corresponds to the PCI addresses AD[31:7]. The mapping format is as follows:

AD[31:7]	AD[6:4]	AD[3:0]
Base Address	Channel # (7-0)	Register # (Fh-0h)

6.1.45 FUNCTION 1 (I/O) FAST INFRARED (FIR) SCATTER/GATHER DMA CONTROLLER BASE ADDRESS REGISTER

Configuration offset: 50h - 53h
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

Bit 0: FIR DMA Controller Enable

0: Disabled

1: Enabled

Bit 1: FIR DMA loopback mode enable

0: Disabled

1: Enabled

Bits 5-2: Always 0000b, indicating that this base address register requires 64 bytes of I/O address space.

Bits 31-6: Base address for FIR DMA Controller. Corresponds to the PCI addresses AD[31:6].

6.1.46 FUNCTION 1 (I/O) SYSTEM CONFIGURATION REGISTER

Configuration offset: 58h-59h
Function: 001b
Attribute: Read/Write
Size: 16 bits
Default value: 0024h

Bit 0: Flash Address Shift Enable.

0: Disabled

1: Enabled

Bit 1: Flash Write enable.

0: The PC87560 MEMW# and SMEMW# signals will not be activated during write cycles to ROM address space.

1: The PC87560 MEMW# and SMEMW# signals will be activated during write cycles to ROM address space.

Bit 2: Lower 64KBytes (000E0000h-000EFFFFh, and aliases FFFE0000h-FFFEFFFFh & FFEE0000h-FFEEFFFFh) BIOS Memory Enable.

0: Disabled

1: Enabled

Bit 3: Coprocessor Error Enable

0: Disable coprocessor error reporting. When disabled, asserting FERR# will not generate a coprocessor error interrupt, and writing to Port F0h while FERR# is asserted will not cause IGNNE# to be asserted low.

1: Enable coprocessor error reporting. When enabled, asserting FERR# will generate a coprocessor error interrupt, and writing to Port F0h while FERR# is asserted will cause IGNNE# to be asserted low until FERR# is negated high.

Bit 4: Positive/subtractive decoding. All the PC87560 functions that are re-mappable or fixed always use positive decoding on the PCI bus. When a PCI cycle occurs, if the address matches any one of the re-mappable or fixed addresses, the device will claim the cycle by asserting DEVSEL# within the second to fourth PCI clock.

All PCI bus accesses outside the re-mappable and fixed address range can be configured to either respond to a PCI cycle after the 5th PCI clock by asserting DEVSEL# and generating TRDY# if no other device claims the cycle (subtractive decoding) or not to respond to such PCI cycles (no subtractive decoding, responding to positive decoded addresses only). If a PCI-ISA bridge is used (an ISA bridge uses subtractive decoding) then the device needs to be configured in positive decoding only not respond to addresses outside the remappable and fixed address range. When subtractive decoding is enabled, all subtractively decode PCI I/O accesses are forwarded to the FX bus. If it is a PCI I/O cycle and subtractive decoding is enabled, the FXIOR#/FXIOW# are used as the control signals on the FX bus without any FX bus chip selects enabled.

0: Positive decoding only. No subtractive decoding used for accesses outside the re-mappable and fixed range.

1: Subtractive decoding used for accesses outside the re-mappable and fixed range.

Bit 5: Shutdown Cycle Decode. When enabled, the PC87560 will generate a CPU reset through the CPUINIT pin when a Shutdown special cycle is decoded.

0: Shutdown cycle decode disabled

1: Shutdown cycle decode enabled

Bits 7-6: Reserved.

Bit 8: Reserved.

Bit 9: Reserved.

Bit 10: Reserved.

Bit 11: Reserved.

Bit 12: Fast Internal Legacy 8237 DMA Cycles.

0: Internal Legacy 8237 DMA cycles will run using Demand Mode and Type “F” timing mode.

1: Internal Legacy 8237 DMA cycles will run using their programmed transfer and timing modes.

Bit 13: CLKRUN# Enable.

0: Disable

1: Enable

Bit 14: Reserved.

Bit 15: PS2 Mouse Select.

0: Non-PS2 Mouse Mode. When configured in this mode, KBINT and MINT are input directly to the interrupt routing block without any latching.

1: PS2 Mouse Mode. When configured in PS2 mouse mode, KBINT and MINT are each latched when they transition from a low to high. The latch is cleared when a read to I/O port 60h is detected. The output of the latch goes to the interrupt routing block.

6.1.47 FUNCTION 1 (I/O) FUNCTION ENABLE REGISTER FOR DECODING

Configuration offset: 5Ah-5Bh
Function: 001b
Attribute: Read/Write
Size: 16 bits
Default value: FFBFh if FENCFG# pin is sampled high by the rising edge of RESET_IN#. 0000h if FENCFG# is sampled low by the rising edge of RESET_IN#.

This register is used to enable/disable individual functions such as Parallel Port, Serials Ports, Floppy Disk Controller, IDE channels, Port 92 and the "206" functions. When a function is disabled, the PC87560 will not respond to PCI accesses to that device (that is, no active DEVSEL#).

Bit 0: Floppy Disk Controller (FDC) Enable

0:Disabled
1:Enabled

Bit 1: Serial Port 1 Enable

0:Disabled
1:Enabled

Bit 2: IDE Channel 1 Enable

0:Disabled
1:Enabled

Bit 3: Serial Port 2 Enable

0:Disabled
1:Enabled

Bit 4: IDE Channel 2 Enable

0:Disabled
1:Enabled

Bit 5: Parallel Port Enable

0:Disabled
1:Enabled

Bit 6: **Reserved.**

Bit 7: Port 92 Enable

0:Disabled
1:Enabled

Bit 8: Real Time Clock Access Enable

0:Disabled
1:Enabled

Bit 9: 8259s and Port F0 Enable

0:Disabled
1:Enabled

Bit 10: 8254 Enable

0:Disabled
1:Enabled

Bit 11: Legacy 8237 DMA1 Enable

0:Disabled
1:Enabled

Bit 12: Legacy 8237 DMA2 Enable

0:disable
1:enable

Bit 13: Keyboard Controller Access Enable

0:Disabled
1:Enabled

Bit 14: Port 61 Enable

0:Disabled
1:Enabled

Bit 15: APM Registers Enable

0:Disabled
1:Enabled

6.1.48 FUNCTION 1 (I/O) SYSTEM I/O CONFIGURATION REGISTER

Configuration offset: 5Ch
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bit 0: PNF Select. If enabled, the Floppy Disk Controller (FDC) signals are multiplexed out onto the Parallel Port/ Floppy pins when the PNF pin is de-asserted low. If either this bit is a zero or the PNF pin is inactive low the Parallel Port signals will be multiplexed onto the Parallel Port/Floppy pins.

0: Disabled. The Parallel Port signals will be multiplexed onto the Parallel Port/Floppy pins.

1: Enabled. If the PNF input signal is a zero, the FDC signals will be multiplexed onto the Parallel Port/ Floppy pins. If the PNF input signal is a one, the Parallel Port signals will be multiplexed onto the Parallel Port/Floppy pins.

Bit 1: Enable Setting Lock from Port 92 Bit 3 bit.

0: When 0, setting Port 92 Bit 3 to a one has no effect. (Default value.)

1: When 1, setting Port 92 Bit 3 to a one enables CMOS locking of index 38h 3Fh.

Bit 2: Enable Setting Lock from P92 Bit 5 bit.

0: When 0, setting Port 92 Bit 5 to a one has no effect. (Default value.)

1: When 1, setting Port 92 Bit 5 to a one enables CMOS locking of index 19h.

Bit 3: Fast Infrared DMA Routing. The FIR's Scatter/Gather DMA request and acknowledge for the receive and transmit channels can be routed to either the Legacy 8237 DMA Controller or the FIR Scatter/Gather DMA Controller.

0: FIR DMA channels routed to the Legacy 8237 DMA Controller

1: FIR DMA channels routed to the FIR Scatter/Gather DMA Controller

Bit 4: 8051/VM Keyboard Controller select.

0: 8051 KBC.

1: VM KBC. When VM KBC is selected, then the RTCALE pin is configured to generate PMCS# output to the VM KBC. PMCS# is asserted during I/O read/writes to addresses KBCBAR+2h and KBCBAR+6h if KBC access enable is 1. RTCCS# is asserted during I/O read/writes to addresses 70h and 71h if RTC access enable = 1.

Bit 5: Baudrate Test Enable for Serial Port 1.

0: Disable

1: Enable (BAUD clock output on DTR[0]# pin)

Bit 6: UIR Enable Register Bank Selection

0:Bank selection disabled (Serial Port 2 in 16550 mode)

1: Bank selection enabled (Serial Port 2 in UIR mode)

Bit 7: KBCS# Address Range Select

This bit has no effect when KBC Access Enable bit (Bit 13 of Function 1 (I/O) Function Enable Register for Decoding) is a zero. In that case, KBCS# will never go active.

0: KBCS# is asserted for I/O read/writes to addresses KBCBAR+0h and KBCBAR+4h. (Default value.)

1: KBCS# is asserted for I/O read/writes to addresses KBCBAR+0h, KBCBAR+2h, KBCBAR+4h and KBCBAR+6h.

6.1.49 FUNCTION 1 (I/O) SPECIAL FUNCTION ENABLE REGISTER

Configuration offset: 5Dh
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bit 0: Floppy Disk Controller (FDC) Configuration Mode Enable.

0: Disabled. Access to the FDC Configuration Registers is disabled.

1: Enabled. Access to the FDC Configuration Registers is enabled. Also, when this bit transitions from a zero to a one, the FDC configuration index register will be initialized to 00h.

Bit 1: Enable BSER CPU Interrupt generation.

0: Disabled. The CPU Interrupt will be disabled from generating a BSER sequence due to the CPU Interrupt going active.

1: Enabled. The CPU Interrupt will generate a BSER sequence when the CPU Interrupt goes active.

Bits 7-2: Reserved.

6.1.50 FUNCTION 1 (I/O) PARALLEL PORT IDENTIFICATION REGISTER (PPDID)

Configuration offset: 5Eh
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 10h

Bit 3-0: Revision Level.

Bit 7-4: Device ID.

6.1.51 FUNCTION 1 (I/O) PARALLEL PORT MODE SELECT REGISTER

Configuration offset: 5Fh
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bits 2-0: Parallel Port Mode Selct. When the Parallel Port is enabled, the Parallel Port mode is selected as follows.

Bit 2	Bit 1	Bit 0	Description
0	0	0	Compatible Mode. In this mode the Parallel Port data pins are always in the output direction.
0	0	1	Extended mode. In this mode the Parallel Port data pins direction is controlled by the Parallel Port`s direction bit.
0	1	0	EPP 1.7 Mode.
0	1	1	EPP 1.9 Mode.
1	0	0	ECP Mode without embedded EPP support.
1	0	1	**Reserved.** Undefined results if this combination is selected.
1	1	0	**Reserved.** Undefined results if this combination is selected.
1	1	1	ECP Mode with EPP in mode 4.

Bits 7-3: Reserved.

6.1.52 FUNCTION 1 (I/O) DMA ROUTING CONTROL REGISTER 4

Configuration offset: 61h
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bits 3-0: DRQ[3] Routing. DRQ[3] from the FX Bus may be used to support either an 8-bit or a 16-bit DMA requester and therefore the PC87560 supports routing this signal to any of the Legacy 8237 DMA channels. DACK[3]# will be driven with the Legacy 8237 DMA Acknowledge signal corresponding to the channel selected for the DRQ[3]

NOTE: It is illegal for software to program more than one source to be routed to any single DMA channel. It is the responsiblity of the software to guarantee that this does not happen.

Bit 3	Bit 2	Bit 1	Bit 0	Description
0	x	x	x	DRQ[3] not routed to DMA channel
1	0	0	0	DRQ[3] routed to DMA channel 0
1	0	0	1	DRQ[3] routed to DMA channel 1
1	0	1	0	DRQ[3] routed to DMA channel 2
1	0	1	1	DRQ[3] routed to DMA channel 3
1	1	0	0	DRQ[3] not routed to DMA channel
1	1	0	1	DRQ[3] routed to DMA channel 5
1	1	1	0	DRQ[3] routed to DMA channel 6
1	1	1	1	DRQ[3] routed to DMA channel 7

Bits 7-4: **Reserved.** These bits must always be written as zeros for future compatiblity.

6.1.53 FUNCTION 1 (I/O) ROM CONFIGURATION REGISTER

Configuration offset: 62h
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

This register is used to select what PCI address range will generate ROMCS#. Refer to Table 4.17 - ROM Chip Select.

Bit 0: ROMCS# for addresses 000C0000h-000C3FFFh Enable.

0:Disabled
1:Enabled

Bit 1: ROMCS# for addresses 000C4000h-000C7FFFh Enable.

0:Disabled
1:Enabled

Bit 2: ROMCS# for addresses 000C8000h-000CBFFFh Enable.

0:Disabled
1:Enabled

Bit 3: ROMCS# for addresses 000CC000h-000CFFFFh Enable.

0:Disabled
1:Enabled

Bit 4: ROMCS# for addresses 000D0000h-000D3FFFh Enable.

0:Disabled
1:Enabled

Bit 5: ROMCS# for addresses 000D4000h-000D7FFFh Enable.

0:Disabled
1:Enabled

Bit 6: ROMCS# for addresses 000D8000h-000DBFFFh Enable.

0:Disabled
1:Enabled

Bit 7: ROMCS# for addresses 000DC000h-000DFFFFh Enable.

0:Disabled
1:Enabled

6.1.54 FUNCTION 1 (I/O) DMA ROUTING CONTROL REGISTER 1

Configuration offset: 63h
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 67h

Bits 2-0: Parallel Port DMA Routing. The parallel port is an 8-bit device and uses only 8-bit DMA channels as selected by these bits.

NOTE: It is illegal for software to program more than one source to be routed to any single DMA channel. It is the responsiblity of the software to guarantee that this does not happen.

Bit 2	Bit 1	Bit 0	Description
0	x	x	PP not routed to DMA channel
1	0	0	PP routed to DMA channel 0
1	0	1	PP routed to DMA channel 1
1	1	0	PP routed to DMA channel 2
1	1	1	PP routed to DMA channel 3

Bit 3: **Reserved.** This bit must always be written as a zero for future compatiblity.

Bits 6-4: Floppy Disk Controller (FDC) DMA Routing. The FDC is an 8-bit device and uses only 8-bit DMA channels as selected by these bits.

NOTE: It is illegal for software to program more than one source to be routed to any single DMA channel. It is the responsiblity of the software to guarantee that this does not happen.

Bit 6	Bit 5	Bit 4	Description
0	x	x	FDC not routed to DMA channel
1	0	0	FDC routed to DMA channel 0
1	0	1	FDC routed to DMA channel 1
1	1	0	FDC routed to DMA channel 2
1	1	1	FDC routed to DMA channel 3

Bit 7: **Reserved.** This bit must always be written as a zero for future compatiblity.

6.1.55 FUNCTION 1 (I/O) DMA ROUTING CONTROL REGISTER 2

Configuration offset: 64h
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bits 3-0: DRQ[0] Routing. DRQ[0] from the FX Bus may be used to support either an 8-bit or a 16-bit DMA requester and therefore the PC87560 supports routing this signal to any of the Legacy 8237 DMA channels. DACK[0]# will be driven with the Legacy 8237 DMA Acknowledge signal corresponding to the channel selected for DRQ[0].

NOTE: It is illegal for software to program more than one source to be routed to any single DMA channel.

It is the responsiblity of the software to guarantee that this does not happen.

Bit 3	Bit 2	Bit 1	Bit 0	Description
0	x	x	x	DRQ[0] not routed to DMA channel
1	0	0	0	DRQ[0] routed to DMA channel 0
1	0	0	1	DRQ[0] routed to DMA channel 1
1	0	1	0	DRQ[0] routed to DMA channel 2
1	0	1	1	DRQ[0] routed to DMA channel 3
1	1	0	0	DRQ[0] not routed to DMA channel
1	1	0	1	DRQ[0] routed to DMA channel 5
1	1	1	0	DRQ[0] routed to DMA channel 6
1	1	1	1	DRQ[0] routed to DMA channel 7

Bits 7-4: DRQ[1] Routing. DRQ[1] from the FX Bus may be used to support either an 8-bit or a 16-bit DMA requester and therefore the PC87560 supports routing this signal to any of the Legacy 8237 DMA channels. DACK[1]# will be driven with the Legacy 8237 DMA Acknowledge signal corresponding to the channel selected for DRQ[1].

NOTE: It is illegal for software to program more than one source to be routed to any single DMA channel. It is the responsiblity of the software to guarantee that this does not happen.

Bit 7	Bit 6	Bit 5	Bit 4	Description
0	x	x	x	DRQ[1] not routed to DMA channel
1	0	0	0	DRQ[1] routed to DMA channel 0
1	0	0	1	DRQ[1] routed to DMA channel 1
1	0	1	0	DRQ[1] routed to DMA channel 2
1	0	1	1	DRQ[1] routed to DMA channel 3
1	1	0	0	DRQ[1] not routed to DMA channel
1	1	0	1	DRQ[1] routed to DMA channel 5
1	1	1	0	DRQ[1] routed to DMA channel 6
1	1	1	1	DRQ[1] routed to DMA channel 7

6.1.56 FUNCTION 1 (I/O) DMA ROUTING CONTROL REGISTER 3

Configuration offset: 65h
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bits 3-0: DRQ[2] Routing. DRQ[2] from the FX Bus may be used to support either an 8-bit or a 16-bit DMA requester and therefore the PC87560 supports routing this signal to any of the Legacy 8237 DMA channels. DACK[2]# will be driven with the Legacy 8237 DMA Acknowledge signal corresponding to the channel selected for DRQ[2].

NOTE: It is illegal for software to program more than one source to be routed to any single DMA channel. It is the responsiblity of the software to guarantee that this does not happen.

Bit3	Bit2	Bit1	Bit0	Description
0	x	x	x	DRQ[2] not routed to DMA channel
1	0	0	0	DRQ[2] routed to DMA channel 0
1	0	0	1	DRQ[2] routed to DMA channel 1
1	0	1	0	DRQ[2] routed to DMA channel 2
1	0	1	1	DRQ[2] routed to DMA channel 3

Bit3	Bit2	Bit1	Bit0	Description
1	1	0	0	DRQ[2] not routed to DMA channel
1	1	0	1	DRQ[2] routed to DMA channel 5
1	1	1	0	DRQ[2] routed to DMA channel 6
1	1	1	1	DRQ[2] routed to DMA channel 7

Bits 5-4: FIR Transmit Channel DMA Routing. The FIR is an 8-bit device and uses only 8-bit DMA channels as selected by these bits. When the FIR is routed to the Legacy 8237 DMA Controller (System I/O Configuration Register Bit 3=0), then these bits select the DMA channel that the transmit channel connects to.

NOTE: It is illegal for software to program more than one source to be routed to any single DMA channel. It is the responsiblity of the software to guarantee that this does not happen.

Bit5	Bit4	Description
0	0	FIR Tx routed to DMA channel 0
0	1	FIR Tx routed to DMA channel 1
1	0	FIR Tx routed to DMA channel 2
1	1	FIR Tx routed to DMA channel 3

Bits 7-6: FIR Receive Channel DMA Routing. The FIR is an 8-bit device and uses only 8-bit DMA channels as selected by these bits. When the FIR is routed to the Legacy 8237 DMA Controller (System I/O Configuration Register bit 3=0), then these bits select the DMA channel that the receive channel connects to.

NOTE: It is illegal for software to program more than one source to be routed to any single DMA channel. It is the responsiblity of the software to guarantee that this does not happen.

Bit 7	Bit 6	Description
0	0	FIR Rx routed to DMA channel 0
0	1	FIR Rx routed to DMA channel 1
1	0	FIR Rx routed to DMA channel 2
1	1	FIR Rx routed to DMA channel 3

6.1.57 FUNCTION 1 (I/O) 8237 DMA CHANNEL CONTROL

Configuration offset: 66h
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

The individual channels on the Legacy 8237 DMA Controllers can be remapped if enabled. When the Global DMA Channel Remapping Enable bit (Bit 0 of the Function 1 (I/O) DMA Remap Base Address Register) is equal to a one, accesses to that channel are forwarded out on to the PCI bus by the Distributed DMA Remapper. This includes access to the channel's legacy registers, DMA page 1 and DMA page 2 registers.

When the Global DMA Channel Remapping Enable bit is a zero and the Distributed DMA Slave vs. Legacy DMA bit (Bit 1 of the Function 1 (I/O) DMA Remap Base Address Register) is set to a one, then the bits with ones in this register indicate which DIstributed DMA slave slices are to be supported by the PC87560 Legacy 8237 DMA Controller.

If both the Global DMA Channel Remapping Enable bit and the Distributed DMA vs. Legacy DMA bit are zero, the bits in this register have no effect.

Bit 0: Channel 0 Remap enable

0: disable
1: enable

Bit 1: Channel 1 Remap enable

0: disable
1: enable

Bit 2: Channel 2 Remap enable

0: disable
1: enable

Bit 3: Channel 3 Remap enable

0: disable
1: enable

Bit 4: Channel 5 Remap enable

0: disable
1: enable

Bit 5: Channel 6 Remap enable

0: disable
1: enable

Bit 6: Channel 7 Remap enable

0: disable
1: enable

Bit 7: **Reserved.**

6.1.58 FUNCTION 1 (I/O) INTERRUPT LEVEL/EDGE TRIGGERING CONTROL

Configuration offset: 67h - 68h
Function: 001b
Attribute: Read/Write
Size: 16 bits
Default value: 0000h

Each interrupt channel of the interrupt controller can be programmed to be either edge or level triggered. This feature works in conjunction with the global setting of edge/level sensitivity of each interrupt controller.

When the individual channel is set to be edge sensitive, then a low to high transition of the interrupt source will be recognized as an interrupt. The interrupt source request can remain high without generating another interrupt. If the individual channel is set to be level sensitive, then a low level on the interrupt source will cause an interrupt. The interrupt source request must be removed before the End Of Interrupt (EOI) command in order to prevent another interrupt to occur.

Bit 0: **Reserved.**

Bit 1: INT1 edge or level select

0: edge
1: level

Bit 2: **Reserved.**

Bit 3: INT3 edge or level select

0: edge
1: level

Bit 4: INT4 edge or level select

0: edge
1: level

Bit 5: INT5 edge or level select

0: edge
1: level

Bit 6: INT6 edge or level select

0: edge
1: level

Bit 7: INT7 edge or level select

0: edge
1: level

Bit 8: **Reserved.**

Bit 9: INT9 edge or level select

0: edge
1: level

Bit 10: INT10 edge or level select

0: edge
1: level

Bit 11: INT11 edge or level select

0: edge
1: level

Bit 12: INT12 edge or level select

0: edge
1: level

Bit 13: **Reserved.**

Bit 14: INT14 edge or level select

0: edge
1: level

Bit 15: INT15 edge or level select

0: edge
1: level

6.1.59 FUNCTION 1 (I/O) INTERRUPT ROUTING CONTROL REGISTER 1 (IRCR1)

Configuration offset: 69h
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 34h

Bits 3-0: Serial Port 1 (SP1) interrupt routing

Bit3	Bit2	Bit1	Bit0	Description
0	0	0	0	SP1 not routed to Interrupt controller
0	0	0	1	SP1 routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	SP1 routed to Interrupt channel 3
0	1	0	0	SP1 routed to Interrupt channel 4
0	1	0	1	SP1 routed to Interrupt channel 5
0	1	1	0	SP1 routed to Interrupt channel 6
0	1	1	1	SP1 routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	SP1 routed to Interrupt channel 9
1	0	1	0	SP1 routed to Interrupt channel 10
1	0	1	1	SP1 routed to Interrupt channel 11
1	1	0	0	SP1 routed to Interrupt channel 12
1	1	0	1	Reserved, undefined results if configured
1	1	1	0	SP1 routed to Interrupt channel 14
1	1	1	1	SP1 routed to Interrupt channel 15

Bits 7-4: Serial Port 2 (SP2) interrupt routing

Bit7	Bit6	Bit5	Bit4	Description
0	0	0	0	SP2 not routed to Interrupt controller
0	0	0	1	SP2 routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	SP2 routed to Interrupt channel 3
0	1	0	0	SP2 routed to Interrupt channel 4
0	1	0	1	SP2 routed to Interrupt channel 5
0	1	1	0	SP2 routed to Interrupt channel 6
0	1	1	1	SP2 routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	SP2 routed to Interrupt channel 9
1	0	1	0	SP2 routed to Interrupt channel 10
1	0	1	1	SP2 routed to Interrupt channel 11
1	1	0	0	SP2 routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	SP2 routed to Interrupt channel 14
1	1	1	1	SP2 routed to Interrupt channel 15

6.1.60 FUNCTION 1 (I/O) INTERRUPT ROUTING CONTROL REGISTER 2 (IRCR2)

Configuration offset: 6Ah
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 65h

Bits 3-0: Parallel Port (PP) interrupt routing. See also Printer Control Register 2.

Bit3	Bit2	Bit1	Bit0	Description
0	0	0	0	PP not routed to Interrupt controller
0	0	0	1	PP routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	PP routed to Interrupt channel 3
0	1	0	0	PP routed to Interrupt channel 4
0	1	0	1	PP routed to Interrupt channel 5
0	1	1	0	PP routed to Interrupt channel 6
0	1	1	1	PP routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	PP routed to Interrupt channel 9
1	0	1	0	PP routed to Interrupt channel 10
1	0	1	1	PP routed to Interrupt channel 11
1	1	0	0	PP routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	PP routed to Interrupt channel 14
1	1	1	1	PP routed to Interrupt channel 15

Bits 7-4: Floppy Disk Controller (FDC) interrupt routing

Bit7	Bit6	Bit5	Bit4	Description
0	0	0	0	FDC not routed to Interrupt controller
0	0	0	1	FDC routed to Interrupt channel 1
0	0	0	1	**Reserved**, undefined results if configured
0	0	0	1	FDC routed to Interrupt channel 3
0	1	0	0	FDC routed to Interrupt channel 4
0	1	0	1	FDC routed to Interrupt channel 5
0	1	1	0	FDC routed to Interrupt channel 6
0	1	1	1	FDC routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	FDC routed to Interrupt channel 9
1	0	1	0	FDC routed to Interrupt channel 10
1	0	1	1	FDC routed to Interrupt channel 11
1	1	0	0	FDC routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	FDC routed to Interrupt channel 14
1	1	1	1	FDC routed to Interrupt channel 15

6.1.61 FUNCTION 1 (I/O) INTERRUPT ROUTING CONTROL REGISTER 3 (IRCR3)

Configuration offset: 6Bh
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: FEh

Bits 3-0: IDE Channel1 (IDE1) interrupt routing

Bit3	Bit2	Bit1	Bit0	Description
0	0	0	0	IDE1 not routed to Interrupt controller
0	0	0	1	IDE1 routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	IDE1 routed to Interrupt channel 3
0	1	0	0	IDE1 routed to Interrupt channel 4
0	1	0	1	IDE1 routed to Interrupt channel 5
0	1	1	0	IDE1 routed to Interrupt channel 6
0	1	1	1	IDE1 routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	IDE1 routed to Interrupt channel 9
1	0	1	0	IDE1 routed to Interrupt channel 10
1	0	1	1	IDE1 routed to Interrupt channel 11
1	1	0	0	IDE1 routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	IDE1 routed to Interrupt channel 14
1	1	1	1	IDE1 routed to Interrupt channel 15

Bits 7-4: IDE Channel 2 (IDE2) interrupt routing

Bit7	Bit6	Bit5	Bit4	Description
0	0	0	0	IDE2 not routed to Interrupt controller
0	0	0	1	IDE2 routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	IDE2 routed to Interrupt channel 3
0	1	0	0	IDE2 routed to Interrupt channel 4
0	1	0	1	IDE2 routed to Interrupt channel 5
0	1	1	0	IDE2 routed to Interrupt channel 6
0	1	1	1	IDE2 routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	IDE2 routed to Interrupt channel 9
1	0	1	0	IDE2 routed to Interrupt channel 10
1	0	1	1	IDE2 routed to Interrupt channel 11
1	1	0	0	IDE2 routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	IDE2 routed to Interrupt channel 14
1	1	1	1	IDE2 routed to Interrupt channel 15

6.1.62 FUNCTION 1 (I/O) INTERRUPT ROUTING CONTROL REGISTER 4 (IRCR4)

Configuration offset: 6Ch
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bits 3-0: PCI INTA# routing

Bit3	Bit2	Bit1	Bit0	Description
0	0	0	0	INTA# not routed to Interrupt controller
0	0	0	1	INTA# routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	INTA# routed to Interrupt channel 3
0	1	0	0	INTA# routed to Interrupt channel 4
0	1	0	1	INTA# routed to Interrupt channel 5
0	1	1	0	INTA# routed to Interrupt channel 6
0	1	1	1	INTA# routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	INTA# routed to Interrupt channel 9
1	0	1	0	INTA# routed to Interrupt channel 10
1	0	1	1	INTA# routed to Interrupt channel 11
1	1	0	0	INTA# routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	INTA# routed to Interrupt channel 14
1	1	1	1	INTA# routed to Interrupt channel 15

Bits 7-4: PCI INTB# routing

Bit7	Bit6	Bit5	Bit4	Description
0	0	0	0	INTB# not routed to Interrupt controller
0	0	0	1	INTB# routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	INTB# routed to Interrupt channel 3
0	1	0	0	INTB# routed to Interrupt channel 4
0	1	0	1	INTB# routed to Interrupt channel 5
0	1	1	0	INTB# routed to Interrupt channel 6
0	1	1	1	INTB# routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	INTB# routed to Interrupt channel 9
1	0	1	0	INTB# routed to Interrupt channel 10
1	0	1	1	INTB# routed to Interrupt channel 11
1	1	0	0	INTB# routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	INTB# routed to Interrupt channel 14
1	1	1	1	INTB# routed to Interrupt channel 15

6.1.63 FUNCTION 1 (I/O) INTERRUPT ROUTING CONTROL REGISTER 5 (IRCR5)

Configuration offset: 6Dh
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bits 3-0: PCI INTC# routing

Bit3	Bit2	Bit1	Bit0	Description
0	0	0	0	INTC# not routed to Interrupt controller
0	0	0	1	INTC# routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	INTC# routed to Interrupt channel 3
0	1	0	0	INTC# routed to Interrupt channel 4
0	1	0	1	INTC# routed to Interrupt channel 5
0	1	1	0	INTC# routed to Interrupt channel 6
0	1	1	1	INTC# routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	INTC# routed to Interrupt channel 9
1	0	1	0	INTC# routed to Interrupt channel 10
1	0	1	1	INTC# routed to Interrupt channel 11
1	1	0	0	INTC# routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	INTC# routed to Interrupt channel 14
1	1	1	1	INTC# routed to Interrupt channel 15

Bits 7-4: PCI INTD# routing

Bit7	Bit6	Bit5	Bit4	Description
0	0	0	0	INTD# not routed to Interrupt controller
0	0	0	1	INTD# routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	INTD# routed to Interrupt channel 3
0	1	0	0	INTD# routed to Interrupt channel 4
0	1	0	1	INTD# routed to Interrupt channel 5
0	1	1	0	INTD# routed to Interrupt channel 6
0	1	1	1	INTD# routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	INTD# routed to Interrupt channel 9
1	0	1	0	INTD# routed to Interrupt channel 10
1	0	1	1	INTD# routed to Interrupt channel 11
1	1	0	0	INTD# routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	INTD# routed to Interrupt channel 14
1	1	1	1	INTD# routed to Interrupt channel 15

6.1.64 FUNCTION 1 (I/O) INTERRUPT ROUTING CONTROL REGISTER 6 (IRCR6)

Configuration offset: 6Eh
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: C1h

Bits 3-0: Keyboard Controller interrupt (KBINT) routing

Bit3	Bit2	Bit1	Bit0	Description
0	0	0	0	KBINT not routed to Interrupt controller
0	0	0	1	KBINT routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	KBINT routed to Interrupt channel 3
0	1	0	0	KBINT routed to Interrupt channel 4
0	1	0	1	KBINT routed to Interrupt channel 5
0	1	1	0	KBINT routed to Interrupt channel 6
0	1	1	1	KBINT routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	KBINT routed to Interrupt channel 9
1	0	1	0	KBINT routed to Interrupt channel 10
1	0	1	1	KBINT routed to Interrupt channel 11
1	1	0	0	KBINT routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	KBINT routed to Interrupt channel 14
1	1	1	1	KBINT routed to Interrupt channel 15

Bits 7-4: Mouse interrupt (MINT) routing

Bit7	Bit6	Bit5	Bit4	Description
0	0	0	0	MINT not routed to Interrupt controller
0	0	0	1	MINT routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	MINT routed to Interrupt channel 3
0	1	0	0	MINT routed to Interrupt channel 4
0	1	0	1	MINT routed to Interrupt channel 5
0	1	1	0	MINT routed to Interrupt channel 6
0	1	1	1	MINT routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	MINT routed to Interrupt channel 9
1	0	1	0	MINT routed to Interrupt channel 10
1	0	1	1	MINT routed to Interrupt channel 11
1	1	0	0	MINT routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	MINT routed to Interrupt channel 14
1	1	1	1	MINT routed to Interrupt channel 15

6.1.65 FUNCTION 1 (I/O) INTERRUPT ROUTING CONTROL REGISTER 7 (IRCR7)

Configuration offset: 6Fh
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bits 3-0: FX Bus IRQ 0 interrupt routing

Bit3	Bit2	Bit1	Bit0	Description
0	0	0	0	FXIRQ[0] not routed to Interrupt controller
0	0	0	1	FXIRQ[0] routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	FXIRQ[0] routed to Interrupt channel 3
0	1	0	0	FXIRQ[0] routed to Interrupt channel 4
0	1	0	1	FXIRQ[0] routed to Interrupt channel 5
0	1	1	0	FXIRQ[0] routed to Interrupt channel 6
0	1	1	1	FXIRQ[0] routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	FXIRQ[0] routed to Interrupt channel 9
1	0	1	0	FXIRQ[0] routed to Interrupt channel 10
1	0	1	1	FXIRQ[0] routed to Interrupt channel 11
1	1	0	0	FXIRQ[0] routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	FXIRQ[0] routed to Interrupt channel 14
1	1	1	1	FXIRQ[0] routed to Interrupt channel 15

Bits 7-4: FX Bus IRQ 1 interrupt routing

Bit7	Bit6	Bit5	Bit4	Description
0	0	0	0	FXIRQ[1] not routed to Interrupt controller
0	0	0	1	FXIRQ[1] routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	FXIRQ[1] routed to Interrupt channel 3
0	1	0	0	FXIRQ[1] routed to Interrupt channel 4
0	1	0	1	FXIRQ[1] routed to Interrupt channel 5
0	1	1	0	FXIRQ[1] routed to Interrupt channel 6
0	1	1	1	FXIRQ[1] routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	FXIRQ[1] routed to Interrupt channel 9
1	0	1	0	FXIRQ[1] routed to Interrupt channel 10
1	0	1	1	FXIRQ[1] routed to Interrupt channel 11
1	1	0	0	FXIRQ[1] routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	FXIRQ[1] routed to Interrupt channel 14
1	1	1	1	FXIRQ[1] routed to Interrupt channel 15

6.1.66 FUNCTION 1 (I/O) INTERRUPT ROUTING CONTROL REGISTER 8 (IRCR8)

Configuration offset: 70h
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bits 3-0: FX Bus IRQ 2 interrupt routing

Bit3	Bit2	Bit1	Bit0	Description
0	0	0	0	FXIRQ[2] not routed to Interrupt controller
0	0	0	1	FXIRQ[2] routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	FXIRQ[2] routed to Interrupt channel 3
0	1	0	0	FXIRQ[2] routed to Interrupt channel 4
0	1	0	1	FXIRQ[2] routed to Interrupt channel 5
0	1	1	0	FXIRQ[2] routed to Interrupt channel 6
0	1	1	1	FXIRQ[2] routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	FXIRQ[2] routed to Interrupt channel 9
1	0	1	0	FXIRQ[2] routed to Interrupt channel 10
1	0	1	1	FXIRQ[2] routed to Interrupt channel 11
1	1	0	0	FXIRQ[2] routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	FXIRQ[2] routed to Interrupt channel 14
1	1	1	1	FXIRQ[2] routed to Interrupt channel 15

Bits 7-4: USB Controller Interrupt Request routing

Bit7	Bit6	Bit5	Bit4	Description
0	0	0	0	USB_IRQ not routed to Interrupt controller
0	0	0	1	USB_IRQ routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	USB_IRQ routed to Interrupt channel 3
0	1	0	0	USB_IRQ routed to Interrupt channel 4
0	1	0	1	USB_IRQ routed to Interrupt channel 5
0	1	1	0	USB_IRQ routed to Interrupt channel 6
0	1	1	1	USB_IRQ routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	USB_IRQ routed to Interrupt channel 9
1	0	1	0	USB_IRQ routed to Interrupt channel 10
1	0	1	1	USB_IRQ routed to Interrupt channel 11
1	1	0	0	USB_IRQ routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	USB_IRQ routed to Interrupt channel 14
1	1	1	1	USB_IRQ routed to Interrupt channel 15

6.1.67 FUNCTION 1 (I/O) INTERRUPT ROUTING CONTROL REGISTER 9 (IRCR9)

Configuration offset: 71h
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bits 3-0: Advanced Configuration and Power Interface (ACPI) System Control Interrupt (SCI) interrupt routing

Bit3	Bit2	Bit1	Bit0	Description
0	0	0	0	ACPI_SCI not routed to Interrupt controller
0	0	0	1	ACPI_SCI routed to Interrupt channel 1
0	0	1	0	**Reserved**, undefined results if configured
0	0	1	1	ACPI_SCI routed to Interrupt channel 3
0	1	0	0	ACPI_SCI routed to Interrupt channel 4
0	1	0	1	ACPI_SCI routed to Interrupt channel 5
0	1	1	0	ACPI_SCI routed to Interrupt channel 6
0	1	1	1	ACPI_SCI routed to Interrupt channel 7
1	0	0	0	**Reserved**, undefined results if configured
1	0	0	1	ACPI_SCI routed to Interrupt channel 9
1	0	1	0	ACPI_SCI routed to Interrupt channel 10
1	0	1	1	ACPI_SCI routed to Interrupt channel 11
1	1	0	0	ACPI_SCI routed to Interrupt channel 12
1	1	0	1	**Reserved**, undefined results if configured
1	1	1	0	ACPI_SCI routed to Interrupt channel 14
1	1	1	1	ACPI_SCI routed to Interrupt channel 15

Bits 7-4: Reserved.

6.1.68 FUNCTION 1 INTERNAL (FM MASTER BUS) ARBITER CONTROL REGISTER

Configuration offset: 72h-73h
Function: 001b
Attribute: Read/Write
Size: 16 bits
Default value: 4C88h

This register configures the internal (FM Master Bus) arbiter. The internal arbiter is used to arbitrate between the USB, IDE, Legacy 8237 DMA, FIR Scatter/Gather DMA and the Distributed DMA masters. The sixteen bits of this register determine the order of priority of the five arbiting agents in fixed mode, or the current priority values in rotate mode. Each agent is allotted three bits for this purpose:

Bits 2-0: Assigns the priority level for agent 0 (DST_DMA).

Bits 5-3: Assigns the priority level for agent 1 (FIR_DMA).

Bits 8-6: Assigns the priority level for agent 2 (8237_DMA).

Bits 11-9: Assigns the priority level for agent 3 (IDE).

Bits 14-12: Assigns the priority level for agent 4 (USB).

Bit 15: Fixed Mode selected. This is a read only bit which is set equal to one when none of the bit triplets are equal to another.

Note that this register must not be written if there are active bus masters.

Fixed mode is selected when none of the bit triplets are equal to one another when written. The Priority of each agent remains as assigned. However, if any of these bit triplets are equal when they are written, Rotate mode is selected. In this case, the contents of this register is set to the default value of 4688h (0_100_011_010_001_000b). The chart below describes possible combinations and their outcome. Note that all of the possible decodes of these bits are not covered.

The algorithm employed in Rotate mode is simply this: After an agent has been granted and has surrendered control of the FM Master Bus, it is assigned the lowest priority (its priority bit triplet is reset to zero), acceding to the other agents requesting access to the FM Bus. The value of the priority bit triplets of lower priority agents increment when this occurs. This same algorithm is applied to all five agents, therefore the worst case condition, when all five requests are active from the start, still allows each agent every fifth access.

The value of each agent's bit triplet determines its priority level. There are only five possible agents, however their are eight unique combination of bit triplets; each combination of bit triplets is unique resulting in the possibility of eight different levels of priority, the greater the value in the bit triplet the higher the priority. This means that the value 111b is the highest priority and 000b is the lowest priority. The following table illustrates some examples of the possible fixed priority combinations, but the example only uses the five least signification bit triples (100b - 000b) for simplicity reasons. From this illustration, one should recognize the logical pattern used and thus be able to deduce any desired fixed priority setup.

agent4 [14:12]	**agent3 [11:9]**	**agent2 [8:6]**	**agent1 [5:3]**	**agent0 [2:0]**	**Priority** Highest				Lowest
Fixed Mode									
000b	001b	010b	011b	100b	agent 0	agent 1	agent 2	agent 3	agent 4
100b	011b	010b	001b	000b	agent 4	agent 3	agent 2	agent 1	agent 0
011b	010b	001b	000b	100b	agent 0	agent 4	agent 3	agent 2	agent 1
010b	001b	000b	100b	011b	agent 1	agent 0	agent 4	agent 3	agent 2
001b	000b	100b	011b	010b	agent 2	agent 1	agent 0	agent 4	agent 3
000b	100b	011b	010b	001b	agent 3	agent 2	agent 1	agent 0	agent 4

Rotate Mode (default)

100	011	010	001	000	agent4<->agent 3<->agent 2 <-> agent 1 <-> agent 0
[14:12] = [11:9]					
[14:12] =		[8:6]			
[14:12] =			[5:3]		
[14:12] =				[2:0]	
	[11:9] = [8:6]				
	[11:9] =		[5:3]		
	[11:9] =			[2:0]	
		[8:6] =	[5:3]		
		[8:6] =		[2:0]	
			[5:3] =	[2:0]	

This table gives the priority assigned when the Control Register is written with any of the values shown in the first column.

Bits 2-0: Assigns the priority level for agent 0.

Bits 5-3: Assigns the priority level for agent 1.

Bits 8-6: Assigns the priority level for agent 2.

Bits 11-9: Assigns the priority level for agent 3.

Bits 14-12: Assigns the priority level for agent 4.

The lower section of the table enables a Rotate mode, where an agent assumes the lowest priority level upon surrendering control of the FM Bus, and the lower priority agents' priorities are incremented. If any of the values shown in the bottom section of this table are written, the contents of this register are set to 0_100_011_010_001_000b, and rotate mode is assumed.

6.1.69 FUNCTION 1 (I/O) FX BUS REGION 2 MASK REGISTER

Configuration offset: 74h-75h
Function: 001b
Attribute: Read/Write
Size: 16 bits
Default value: 0000h

This register is used to define the address range for the FX Region 2 window.

Bit 0: **Reserved.**

Bits 15-1: Address mask. Corresponds to the PCI addresses AD[15:1]. The PCI address bits that have their corresponding mask bit set to 1 will not be used to decode the FX Bus I/O Region 2 address range.

6.1.70 FUNCTION 1 (I/O) FX BUS TIMING CONTROL REGISTER

Configuration offset: 76h-77h
Function: 001b
Attribute: Read/Write
Size: 16 bits
Default value: 0000h

Timing for FX Bus commands for standard I/O reads and writes can be programmed. DMA cycles on the FX Bus are fixed. Both the command active time and recovery time are programmable. FXIORDY is sampled at Command Active Time - 2 CLKs.

Bits 1-0: Command active time for region 0 (in PCI clocks).

Default value:
8-bit = 20 clocks

16-bit = 8 clocks

Bit 1	Bit 0	# of CLKs 16-bit mode	# of CLKs 8-bit mode
0	0	8	20
0	1	6	16
1	0	4	8
1	1	**Reserved.**	4

Bits 3-2: Recovery time for region 0

Default value:10 clocks

Bit 3	Bit 2	# of CLKs - 8/16-bit mode
0	0	10
0	1	8
1	0	6
1	1	4

Bits 5-4: Command active time for region 1

Default value:
8-bit = 20 clocks
16-bit = 8 clocks

Bit 5	Bit 4	# of CLKs - 16-bit mode	# of CLKs - 8-bit mode
0	0	8	20
0	1	6	16
1	0	4	8
1	1	**Reserved.**	4

Bits 7-6: Recovery time for region 1

Default value: 10 clocks

Bit 7	Bit 6	# of CLKs - 8/16-bit mode
0	0	10
0	1	8
1	0	6
1	1	4

Bits 9-8: Command time for region 2

Default value:
8-bit = 20 clocks
16-bit = 8 clocks

Bit 9	Bit 8	# of CLKs - 16-bit mode	# of CLKs - 8-bit mode
0	0	8	20
0	1	6	16
1	0	4	8
1	1	**Reserved.**	4

Bits 11-10: Recovery time for region 2

Default value:10 clocks

Bit 11	Bit 10	# of CLKs - 8/16-bit mode
0	0	10
0	1	8
1	0	6
1	1	4

Bits 13-12: Command time for all other regions

Default value:
8-bit = 20 clocks
16-bit = 8 clocks

Bit 13	Bit 12	# of CLKs - 16-bit mode	# of CLKs - 8-bit mode
0	0	8	20
0	1	6	16
1	0	4	8
1	1	**Reserved.**	4

Bits 15-14: Recovery time for all other regions

Default value:10 clocks

Bit 15	Bit 14	# of CLKs - 8/16-bit mode
0	0	10
0	1	8
1	0	6
1	1	4

6.1.71 FUNCTION 1 (I/O) FX BUS CONTROL REGISTER

Configuration offset: 78h
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

This register configures the FX peripherals for either 8- or 16- bits.

Bit 0: FX Bus Region 0 address range accesses are 8- or 16- bits on FX bus.

0: FXCS0 address range accesses are 8 bits (an active IOCS16# can override this programming dynamically on a cycle by cycle basis)
1: FXCS0 address range accesses are 16 bits.

Bit 1: FX Bus Region 1 address range accesses are 8- or 16- bits on FX bus.

0: FXCS1 address range accesses are 8 bits (an active IOCS16# can override this programming dynamically on a cycle by cycle basis)
1: FXCS1 address range accesses are 16 bits.

Bit 2: FX Bus Region 2 accesses are 8- or 16-bits on FX bus.

0: Accesses are 8 bits (an active IOCS16# can override this programming dynamically on a cycle by cycle basis)
1: Accesses are 16 bits.

Bit 3: All other regions (i.e, Subtractive decoding I/O cycles of FX bus, ROM, KBC and RTC accesses) are 8- or 16- bits.

0: Accesses are 8 bits (an active IOCS16# or MEMCS16# can override this programming dynamically on a cycle by cycle basis)
1: Accesses are 16 bits.

Bits 7-4: Reserved.

6.1.72 FUNCTION 1 (I/O) GENERAL PURPOSE I/O CONFIGURATION REGISTER

Configuration offset: 79h
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

This register is used to configure the General Purpose I/O pins.

Bit 0: GPIO0 or AEN pin select.

0: GPIO0
1: AEN - DMA Address ENable output signal.

Bit 1: GPIO1 or ID3 pin select.

0: GPIO1
1: ID3 - Infrared ID3 dongle input.

Bit 2: GPIO2 pin Open-Drain enable.

0: GPIO2 operates as a totem-pole driver
1: GPIO2 operates as a Open-Drain driver (bit-bang support for I^2C)

Bit 3: GPIO3 pin Open-Drain enable.

0: GPIO3 operates as a totem-pole driver
1: GPIO3 operates as a Open-Drain driver (bit-bang support for I^2C)

Bit 4: GPIO4 or IDE_INT1 pin select.

0: GPIO4
1: IDE_INT1 - IDE Channel 1 Internal Interrupt Request output.

Bit 5: GPIO5 or IDE_INT2 pin select.

0: GPIO5
1: IDE_INT2 - IDE Channel 2 Internal Interrupt Request output.

Bit 6: GPIO6 or USB_INT pin select.

0: GPIO6.

1: USB_INT - USB Host Controller Internal Interrupt Request output.

Bit 7: GPIO7 enable/disable.

When the Advance Configuration and Power Management (ACPI) Mode is enabled (Bits 1-0 of the ACPI Function Control Register, ACPIBAR+12h, equal 01b), the GPIO7/EX_PME pin will become the EX_PME input no matter what value resides in this bit.

0: GPIO7 enabled if ACPI Mode is disabled.
1: GPIO7 disabled.

Note: When the alternate function is selected, the direction of the associated GPI0 pin is set according to the alternate function description overriding what is configured in the General Purpose I/O Direction Register.

6.1.73 FUNCTION 1 (I/O) GENERAL PURPOSE I/O DIRECTION REGISTER

Configuration offset: 7Ah
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

This register is used to configure the direct of each General Purpose I/O pins as either input or output when they are configured as general purpose I/O through the General Purpose I/O configuration Register.

Bit 0: GPIO0 direction select

0: input
1: output

Bit 1: GPIO1 direction select

0: input
1: output

Bit 2: GPIO2 direction select

0: input
1: output

Bit 3: GPIO3 direction select

0: input
1: output

Bit 4: GPIO4 direction select

0: input
1: output

Bit 5: GPIO5 direction select

0: input
1: output

Bit 6: GPIO6 direction select

0: input
1: output

Bit 7: GPIO7 direction select

0: input
1: output

6.1.74 FUNCTION 1 (I/O) SERIAL INTERRUPT CONTROL REGISTER

Configuration offset: 7Bh
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Note: Programming of the serial interrupt controller when the controller is currently running can produce unexpected results. It is best to program the serial interrupt controller when it is not active (Bit 7 = 0).

Bits 1-0: Start Cycle length

Bit 1	Bit 0	Number of PCI Clocks
0	0	4 (Default)
0	1	6
1	0	8
1	1	**Reserved.**

Bits 5-2: SINT Sample Period

Bit5	Bit4	Bit3	Bit2	Sample Period
0	0	0	0	17 slots
0	0	0	1	18 slots
0	0	1	0	19 slots
0	0	1	1	20 slots
0	1	0	0	21 slots
0	1	0	1	22 slots
0	1	1	0	23 slots
0	1	1	1	24 slots
1	0	0	0	25 slots
1	0	0	1	26 slots
1	0	1	0	27 slots
1	0	1	1	28 slots
1	1	0	0	29 slots
1	1	0	1	30 slots
1	1	1	0	31 slots
1	1	1	1	32 slots

Bit 6: Quiet/Continuous Mode

0: Quiet
1: Continuous

Bit 7: Serial Interrupt enable

0: disabled
1: enabled

6.1.75 FUNCTION 1 (I/O) SERIAL INTERRUPT ENABLE REGISTER

Configuration offset: 7Ch-7Dh
Function: 001b
Attribute: Read/Write
Size: 16 bits
Default value: 0000h

Bit 0: Serial IRQ1 Enable

0: disable
1: enable

Bit 1: Serial SMI# Enable

0: disable

1: enable

Bit 2: Serial IRQ3 Enable

0: disable
1: enable

Bit 3: Serial IRQ4 Enable

0: disable
1: enable

Bit 4: Serial IRQ5 Enable

0: disable
1: enable

Bit 5: Serial IRQ6 Enable

0: disable
1: enable

Bit 6: Serial IRQ7 Enable

0: disable
1: enable

Bit 7: **Reserved.**

Bit 8: Serial IRQ9 Enable

0: disable
1: enable

Bit 9: Serial IRQ10 Enable

0: disable
1: enable

Bit 10: Serial IRQ11 Enable

0: disable
1: enable

Bit 11: Serial IRQ12 Enable

0: disable
1: enable

Bit 12: **Reserved.**

Bit 13: Serial IRQ14 Enable

0: disable
1: enable

Bit 14: Serial IRQ15 Enable

0: disable
1: enable

Bit 15: Serial IOCHK# Enable

0: disable
1: enable

6.1.76 FUNCTION 1 (I/O) RESERVED CONFIGURATION OFFSET 7EH REGISTER

Configuration offset: 7Eh
Function: 001b
Attribute: Bits 3-0 Read/Write;
Bits 7-4 Read Only
Size: 8 bits
Default value: 01h

This register has a default value of 01h and if any value other than this value is written to these bits, the PC87560 may not operate correct. The user must never write any value other than 01h to this register.

BIT	FUNCTION		
3:0		Command Active time	Recover Time
	0000b	2 clocks	3 clocks
	0001b	3 clocks	3 clocks (default)
	0010b	6 clocks	4 clocks
	0011b	8 clocks	6 clocks
	0100b - 1111b	4 clocks	6 clocks
7:4	**Reserved.**		

6.1.77 FUNCTION 1 (I/O) AUDIO CHIP SELECT ENABLE REGISTER

Configuration offset: 7Fh
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 0000h

This register supports a fragmented Sound Blaster compatible I/O address decode to generate the active-low Audio Chip Select (AUDIOCS#). The following is a quick synopsis of the I/O ranges associated with each bit:

Bit 0: 0201h
Bit 1: 0220h-022Fh
Bit 2: 0230h-023Fh
Bit 3: 0240h-024Fh
Bit 4: 0250h-025Fh
Bit 5: 0388h-038Fh

Bit 0: Audio Range 0 Enabled.

0: Disable. The AUDIOCS# will not be asserted for accesses to I/O address 0201h and the corresponding I/O access will not be performed on the FX Bus.
1: Enable. The AUSIOCS# will be asserted low for accesses to I/O address 0201h and the corresponding I/O access will be performed on the FX Bus.

Bit 1: Audio Range 1 Enabled.

0: Disable. The AUDIOCS# will not be asserted for accesses to I/O addresses 0220h-022Fh and the corresponding I/O access will not be performed on the FX Bus.
1: Enable. The AUSIOCS# will be asserted low for accesses to I/O addresses 0220h-022Fh and the corresponding I/O access will be performed on the FX Bus.

Bit 2: Audio Range 2 Enabled.

0: Disable. The AUDIOCS# will not be asserted for accesses to I/O addresses 0230h-023Fh and the corresponding I/O access will not be performed on the FX Bus.
1: Enable. The AUSIOCS# will be asserted low for accesses to I/O addresses 0230h-023Fh and the corresponding I/O access will be performed on the FX Bus.

Bit 3: Audio Range 3 Enabled.

0: Disable. The AUDIOCS# will not be asserted for accesses to I/O addresses 0240h-024Fh and the corresponding I/O access will not be performed on the FX Bus.
1: Enable. The AUSIOCS# will be asserted low for accesses to I/O addresses 0240h-024Fh and the corresponding I/O access will be performed on the FX Bus.

Bit 4: Audio Range 4 Enabled.

0: Disable. The AUDIOCS# will not be asserted for accesses to I/O addresses 0250h-025Fh and the corresponding I/O access will not be performed on the FX Bus.
1: Enable. The AUSIOCS# will be asserted low for accesses to I/O addresses 0250h-025Fh and the corresponding I/O access will be performed on the FX Bus.

Bit 5: Audio Range 5 Enabled.

0: Disable. The AUDIOCS# will not be asserted for accesses to I/O addresses 0388h-038Fh and the corresponding I/O access will not be performed on the FX Bus.
1: Enable. The AUSIOCS# will be asserted low for accesses to I/O addresses 0388h-038Fh and the corresponding I/O access will be performed on the FX Bus.

Bits 7-6: Reserved.

6.1.78 FUNCTION 1 (I/O) FX BUS MEMORY RANGE CONTROL REGISTER 1

Configuration offset: 80h - 83h
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

This register provides for support of a memory range on the FX Bus. The memory may be programmed to have a block size of between 4Kbytes and 2Mbytes. The base address will be at the multiple of the block size specified by this register Bits 20-12.

Bits 0: FX Bus Memory Block 1 Enable bit. When this bit is a one, the PC87560 will enable the programmed memory range for PCI Bus cycle accesses to the corresponding FX Bus memory range.**Bits 4-1:**

FX Bus Memory Block 1 Size Control bits. These bits determine the size of the FX Bus Memory Block 1 according to the following:

Bit4	Bit3	Bit2	Bit1	FX Bus Memory Block Size
0	0	0	0	4 Kbytes (Default)
0	0	0	1	8 Kbytes
0	0	1	0	16 Kbytes
0	0	1	1	32 Kbytes
0	1	0	0	64 Kbytes
0	1	0	1	128 Kbytes
0	1	1	0	256 Kbytes
0	1	1	1	512 Kbytes
1	0	0	0	1 Mbytes
1	0	0	1	2 Mbytes
1	0	1	0	**Reserved**, this combination will disable the memory range.
1	0	1	1	**Reserved**, this combination will disable the memory range.
1	1	0	0	**Reserved**, this combination will disable the memory range.
1	1	0	1	**Reserved**, this combination will disable the memory range.
1	1	1	0	**Reserved**, this combination will disable the memory range.
1	1	1	1	**Reserved**, this combination will disable the memory range.

Bits 11-0: Reserved. Always zeros.

Bits 20-12: FX Bus Memory Block 1 Base Address. These nine bits are compared to memory address 20-12 and if memory address bits 31-21 are all zeros and these bits match (while the FX Memory BLock 1 range is enabled), the memory access will be performed on the FX Bus.

Bits 23-21: Reserved. Always zeros.

Bits 25-24: FX Bus Memory Block 1 Recovery time bits.

Default value: 10 clocks

Bit 25	Bit 24	# of CLKs - 8/16-bit mode
0	0	10
0	1	8
1	0	6
1	1	4

Bits 27-26: FX Bus Memory Block 1 Command time bits.

Default value:
8-bit = 20 clocks
16-bit = 8 clocks

Bit 27	Bit 26	# of CLKs - 16-bit mode	# of CLKs - 8-bit mode
0	0	8	20
0	1	6	16
1	0	4	8
1	1	**Reserved.**	4

Bits 31-28: Reserved. Always zeros.

6.1.79 FUNCTION 1 (I/O) KEYBOARD CONTROLLER BASE ADDRESS REGISTER (KBCBAR)

Configuration offset: 84h - 87h
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: 00000060h

Used for Keyboard Controller I/O accesses. The PC87560PC87560 decodes 8 bytes of address space for the Keyboard Controller Chip Select (KBCS#). The default value decodes the I/O address range 0060h-0067h, but depends on the Keyboard Controller Access Enable bit for enabling and the KBCS# Address Range Select bit for specifically which of the addresses in this eight byte range will generate an active low KBCS#.

Note: The Keyboard Controller Access Enable bit is Bit 13 of the Function 1 (I/O) Function Enable Register For Decoding, configuration offset 5Ah-5Bh.

The KBCS# Address Range Select bit is Bit 7 of the Function 1 SIO Configuration Register, configuration offset 5Ch.

Bits 2-0: Always 000b. Indicating that this base address register requires an 8-byte I/O address space.

Bits 31-3: The upper 29 bits of the base address are read/write bits that allow Keyboard Controller accesses to be located anywhere in the system I/O space and can be placed on any 8-byte boundary, with an 8-byte range.

6.1.80 FUNCTION 1 (I/O) ADVANCED CONFIGURATION AND POWER INTERFACE BASE ADDRESS REGISTER (ACPIBAR)

Configuration offset: 88h - 8Bh
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

Bit 0: ACPI Register Block Enable.

0: Disable.
1: Enable.

Bits 4-1: **Reserved.** Always 0000b, indicating that the ACPI registers reside in a 32 byte range of I/O address space.

Bits 31-5: The upper 27 bits of the base address are read/write bits that allow ACPI Registers to be located anywhere in the system I/O space and can be placed on any 32-byte boundary.

6.1.81 FUNCTION 1 (I/O) POWER MANAGEMENT BASE ADDRESS REGISTER (PMBAR)

Configuration offset: 8Ch - 8Fh
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: FFFFFF01h

Used for power management register accesses. The device decodes 256 bytes of address space. The power management registers are 32-bit aligned.

Bit 0: Always 1. Indicating that the power management registers are mapped into PCI I/O space.

Bits 7-1: Always 0000000. Indicating that this base address register requires 256 bytes of I/O address space.

Bits 31-8: Base address the power management registers. Corresponds to the PCI addresses AD[31:8].

6.1.82 FUNCTION 1 (I/O) FLOPPY DISK CONTROLLER BASE ADDRESS REGISTER (FDCBAR)

Configuration offset: 90h - 93h
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: 000003F1h

Used for Floppy Disk Controller accesses. The device decodes 8 bytes of address space. The default value decodes I/O addresses 3F0h-3F7h. (excluding 3F6h)

Bit 0: Always 1. Indicating that Floppy Disk Controller accesses are mapped into PCI I/O space.

Bits 2-1: Always 00. Indicating that this base address register requires an 8-byte I/O address space.

Bits 31-3: The upper 29 bits of the base address are read/write bits that allow Floppy Disk Controller accesses to be located anywhere in the system I/O space and can be placed on any 8-byte boundary, with an 8-byte range.

6.1.83 FUNCTION 1 (I/O) SERIAL PORT 1 BASE ADDRESS REGISTER (SP1BAR)

Configuration offset: 94h - 97h
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: 000003F9h

Used for Serial Port 1 I/O accesses. The device decodes 8 bytes of address space. The default value decodes I/O addresses 3F8h-3FFh.

Bit 0: Always 1. Indicating that Serial Port 1 accesses are mapped into PCI I/O space.

Bits 2-1: Always 00. Indicating that this base address register requires an 8-byte I/O address space.

Bits 31-3: The upper 29 bits of the base address are read/write bits that allow Serial Port 1 acœsses to be located anywhere in the system I/O space and can be placed on any 8-byte boundary, with an 8-byte range.

6.1.84 FUNCTION 1 (I/O) SERIAL PORT 2 BASE ADDRESS REGISTER (SP2BAR)

Configuration offset: 98h - 9Bh
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: 000002F9h

Used for Serial Port 2 I/O accesses. The device decodes 8 bytes of address space. The default value decodes I/O addresses 2F8h-2FFh.

Bit 0: Always 1. Indicating that Serial Port 2 accesses are mapped into PCI I/O space.

Bits 2-1: Always 00. Indicating that this base address register requires an 8-byte I/O address space.

Bits 31-3: The upper 29 bits of the base address are read/write bits that allow Serial Port 2 acœsses to be located anywhere in the system I/O space and can be placed on any 8-byte boundary, with an 8-byte range.

6.1.85 FUNCTION 1 (I/O) PARALLEL PORT BASE ADDRESS REGISTER (PPBAR)

Configuration offset: 9Ch - 9Fh
Function: 001b
Attribute: Read/Write
Size: 32 bits
Default value: 00000379h

Used for Parallel Port accesses. The device decodes 16 bytes of I/O space. Eight bytes are at addresses PPBAR +(0h-7h) and another 8 bytes are at addresses PPBAR +(400h-407h). The default value decodes I/O addresses 378h-37Fh (LPT2) and 778h-77Fh.

Bit 0: Always 1. Indicating that Parallel accesses are mapped into PCI I/O space.

Bits 2-1: Always 00. Indicating that this base address register requires an 8-byte I/O address space.

Bits 31-3: The upper 29 bits of the base address are read/write bits that allow Parallel Portaccesses to be located anywhere in the system I/O space and can be placed on any 8-byte boundary, with two 8-byte ranges offset by 400h.

6.1.86 FUNCTION 1 (I/O) OUTPUT INTERNAL BUSES CONTROL REGISTER (TEST FUNCTION ONLY)

Configuration offset: FFh
Function: 001b
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bit 2-0: FXD[15:0] Driving Source Selection

Bit2	Bit1	Bit0	FXD[15:0] Driving Source
0	0	0	Normal Operation
0	0	1	Test Output sib_db[15:0]
0	1	0	Test Output sib_db[31:16]
0	1	1	Test Output fmt_db[15:0]
1	0	0	Test Output fmt_db[31:16]
1	0	1	Test Output fmm_db[15:0]
1	1	x	Test Output fmm_db[31:16]

Bit 3: Route Internal DMA Requests to DACK[3:0] pins, Enable bit.

. 0: Disable.
1: Enable.
DACK[0]# - Floppy Disk Controller DMA Request is multiplexed onto DACK[0]# output.
DACK[1]# - Parallel Port DMA Request is multiplexed onto DACK[1]# output.
DACK[2]# - Fast Infrared Transmit DMA Request is multiplexed onto DACK[2]# output.
DACK[3]# - Fast Infrared Receive DMA Request is multiplexed onto DACK[3]# output.

Bits 7-4: Reserved.

6.1.87 FUNCTION 2 (USB) OPEN HCI BASE ADDRESS REGISTER (OHCIBAR)

Configuration offset: 10h - 13h
Function: 010b
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

Used for the USB Host Controller's Open HCI register accesses. The USB Host Controller decodes 4 Kbytes of PCI Bus Memory address space. For a detailed discussion of the Open HCI registers and their functions, please refer to the Open Host Controller Interface Specification for USB (Release 1.0).

Bit 0: Always 0. Indicating that the Open HCI registers are mapped into PCI Bus Memory space.

Bits 11-1: Always 000_0000_0000b. Indicating that this base address register requires 4 Kbytes of Memory address space.

Bits 31-12: Base address the power management registers. Corresponds to the PCI addresses AD[31:12].

6.1.88 FUNCTION 2 (USB) NSC USB BASE ADDRESS REGISTER (NUSBBAR)

Configuration offset: 14h - 17h
Function: 010b
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

Used for the USB Host Controller's NSC USB register accesses. The USB Host Controller decodes 4 Kbytes of PCI Bus Memory address space.

Bit 0: Always 0. Indicating that the Open HCI registers are mapped into PCI Bus Memory space.

Bits 11-1: Always 000_0000_0000b. Indicating that this base address register requires 4 Kbytes of Memory address space.

Bits 31-12: Base address the power management registers. Corresponds to the PCI addresses AD[31:12].

6.1.89 FUNCTION 2 (USB) INTERRUPT LINE REGISTER

Configuration offset: 3Ch
Function: 010b
Attribute: Read/Write
Size: 8 bits
Default value: FFh

This register resets to FFh and thus indicates that the interrupt request being used is "unknown". Software may if it so desires write the appropriate value into this register, but this register never controls the steering of the USB interrupt request to the 8259 Programmable Interrupt Controllers (the steering of the USB interrupt request is controlled by Bits 7-4 of Function 1 Interrupt Routing Control Register 8 at Function 1 configuration offset 70h).

6.2 Standard I/O Registers

The table below shows all the I/O registers supported by the PC87560.

TABLE 6.4 — Standard I/O Registers

I/O Address (Fixed or Reset Value)	**Function**	**Comment**
0000h-000Fh	Legacy 8237 DMA Channels 3-0	Fixed address
0020h-0021h	8259 Interrupt Controller 1	Fixed address
0040h-0043h	8254 Timer	Fixed address
0060h[Notes 1, 2, 3 and 4]	Keyboard Controller Data Port	Re-mappable
0061h	Port 61	Fixed address
0062h, 0066h[Notes 1, 2, 3 and 4]	VM KBC Power Management Registers	Re-mappable
0064h[Notes 1, 2, 3 and 4]	Keyboard Controller Command Port	Re-mappable
0070h-0071h[Note 4]	RTC and lower 128 Bytes of CMOS RAM	Fixed address
0080h-008Fh	Legacy 8237 DMA Low Page Segment Address Registers	Fixed address
0092h	Port 92	Fixed address
00A0h-00A1h	8259 Interrupt Controller 2	Fixed address
00B2h	Advanced Power Management Control Register	Fixed Address
00B3h	Advanced Power Management Status Register	Fixed Address
00C0h-00DFh	8237 DMA 2 channels 5-7	Fixed address
00F0h	Port F0	Fixed address
0170h-0177h[Notes 2, 3 and 4]	IDE Channel 2 data and command registers	Re-mappable
01F0h-01F7h[Notes 2, 3 and 4]	IDE Channel 1 data and command registers	Re-mappable
02F8h-02FFh[Notes 1 and 2]	Serial Port 2	Re-mappable
0376h[Notes 2, 3 and 4]	IDE Channel 2 control register	Re-mappable
0378h-037Fh[Notes 1 and 2]	Parallel Port	Re-mappable
03F0h-03F7h[Notes 1 and 2]	FDC (except for 03F6h)	Re-mappable
03F6h[Notes 2, 3 and 4]	IDE Channel 1 control register	Re-mappable
03F8h-03FFh[Notes 1 and 2]	Serial Port 1	Re-mappable
040Bh	DMA Channels 3-0 Extended Mode Register	Fixed
0480h-048Fh	Legacy 8237 DMA High Page Segment Address Registers	Fixed
04D6h	DMA Channels 7-5 Extended Mode Register	Fixed
xxxxxxx0h-xxxxxxxFh[Note 2]	Enhanced DMA Controller Channel 1 (used for IDE)	Re-mappable
xxxxxxx0h-xxxxxxxFh[Note 2]	Enhanced DMA Controller Channel 2 (used for IDE)	Re-mappable
xxxxxxx0h-xxxxxxxFh	FX Bus Region 0	Re-mappable
xxxxxxx0h-xxxxxxxFh	FX Bus Region 1	Re-mappable
xxxxxxxxh	FX Bus Region 2	Re-mappable
xxxxxxx00h-xxxxxxxFFh	Power Management Registers	Re-mappable
CF9h	Reset Control Register	Fixed address
xxxxxx00h-xxxxxx3Fh	FIR Scatter/Gather DMA Controller Registers	Re-mappable
xxxxx000h-xxxxxFFFh	USB Controller Open Host Controller Interface Registers	Re-mappable
xxxxx000h-xxxxxFFFh	USB Controller NSC USB Interface Registers	Re-mappable

Notes:

1. The value shown in this table is the default address location.
2. A re-mappable device is re-mappable anywhere within the 4GBytes of I/O or memory space.
3. The value shown in this table is the default address location for legacy operation.
4. Only the I/O decoding is done on chip. The registers reside external to the PC87560.

6.2.1 LEGACY 8237 DMA CONTROLLER REGISTER

When the Legacy 8237 DMA Controller is programmed to operate in Legacy Mode or Distributed DMA Master Mode, its registers will be accessed through the following Legacy I/O addresses. Refer to Section 3.2.2 DISTRIBUTED DMA SLAVE MODE REGISTERS for information describing the I/O addresses via which the Legacy 8237 DMA Controller's register may be accessed in Distributed DMA Slave Mode.

One should note that the registers listed in this section and Section 3.2.2 DISTRIBUTED DMA SLAVE MODE REGISTERS are physically the same registers being accessed via different I/O address locations.

Legacy Mode is enabled when: The Global DMA Channel Remapping Enable bit equals 0 and the Distributed DMA Slave vs. Legacy DMA bit equals 0.

The Global DMA Channel Remapping Enable bit is Bit 0 of the Function 1 (I/O) DMA Remap Base Address Register at configuration offset 4Ch-4Fh.

The Distributed DMA Slave vs. Legacy DMA bit is Bit 1 of the Function 1 (I/O) DMA Remap Base Address Register at configuration offset 4Ch-4Fh.

Distributed DMA Master Mode is enabled when: The Global DMA Channel Remapping Enable bit equals 1. The state of the Distributed DMA Slave vs. Legacy DMA bit has no function when the Global DMA Channel Remapping Enable bit equals 1.

When operating in the Distributed DMA Master Mode, only those I/O addresses associated with channels that have been enabled to be remapped in the FUNCTION 1 (I/O) 8237 DMA CONTROL REGISTER will be remapped back out to external Distributed DMA Slave Slices. While those channels that have not been remapped will be allowed to access the Legacy 8237 DMA Controller Registers via their Legacy I/O address listed below in the following 3.2.1 subsections.

Distributed DMA Slave Mode is enabled when: The Global DMA Channel Remapping Enable bit equals 0 and the Distributed DMA Slave vs. Legacy DMA bit equals 1.

6.2.1.1 Legacy 8237 DMA Base and Current Address Registers 7-0

I/O Addresses: 0000h, 0002h, 0004h, 0006h,
00C0h, 00C4h, 00C8h and 00CCh
Attribute: The Base Address Registers are Write Only
The Current Address Registers are Read Only
Size: 8 bits
Default value: undefined

Legacy I/O Address	Read/ Write	Register Function
0000h	Write	DMA Channel 0, Base Address register
0002h	Write	DMA Channel 1, Base Address register
0004h	Write	DMA Channel 2, Base Address register
0006h	Write	DMA Channel 3, Base Address register
00C0h	Write	DMA Channel 4, Base Address register[NOTE]
00C4h	Write	DMA Channel 5, Base Address register
00C8h	Write	DMA Channel 6, Base Address register
00CCh	Write	DMA Channel 7, Base Address register
0000h	Read	DMA Channel 0, Current Address register
0002h	Read	DMA Channel 1, Current Address register
0004h	Read	DMA Channel 2, Current Address register
0006h	Read	DMA Channel 3, Current Address register
00C0h	Read	DMA Channel 4, Current Address register[NOTE]

Legacy I/O Address	Read/ Write	Register Function
00C4h	Read	DMA Channel 5, Current Address register
00C8h	Read	DMA Channel 6, Current Address register
00CCh	Read	DMA Channel 7, Current Address register

NOTE: This register controls no function in the PC87560, but must be supported due to Legacy compatibility reasons.

6.2.1.2 Legacy 8237 DMA Base and Current Word Count Registers 7-0

I/O Addresses: 0001h, 0003h, 0005h, 0007h,
00C2h, 00C6h, 00CAh and 00CEh
Attribute: The Base Word Count Registers are Write Only
The Current Word Count Registers are Read Only
Size: 8 bits
Default value: undefined

Legacy I/O Address	Read/ Write	Register Function
0001h	Write	DMA Channel 0, Base Word Count register
0003h	Write	DMA Channel 1, Base Word Count register
0005h	Write	DMA Channel 2, Base Word Count register
0007h	Write	DMA Channel 3, Base Word Count register
00C2h	Write	DMA Channel 4, Base Word Count register NOTE
00C6h	Write	DMA Channel 5, Base Word Count register
00CAh	Write	DMA Channel 6, Base Word Count register
00CEh	Write	DMA Channel 7, Base Word Count register
0001h	Read	DMA Channel 0, Current Word Count register
0003h	Read	DMA Channel 1, Current Word Count register
0005h	Read	DMA Channel 2, Current Word Count register
0007h	Read	DMA Channel 3, Current Word Count register
00C2h	Read	DMA Channel 4, Current Word Count register NOTE
00C6h	Read	DMA Channel 5, Current Word Count register
00CAh	Read	DMA Channel 6, Current Word Count register
00CEh	Read	DMA Channel 7, Current Word Count register

NOTE: This register controls no function in the PC87560, but must be supported due to Legacy compatibility reasons.

6.2.1.3 Legacy 8237 DMA Status Registers

I/O Address: 0008h (DMA Channels 3-0)
00D0h (DMA Channels 7-4)
Attribute: Read only
Size: 8 bits
Default value: xxxx0000b

Bit 0: Channel 0 (4) Terminal Count Status

Bit 1: Channel 1 (5) Terminal Count Status

Bit 2: Channel 2 (6) Terminal Count Status

Bit 3: Channel 3 (7) Terminal Count Status

Bit 4: Channel 0 (4) Request Status

Bit 5: Channel 1 (5) Request Status

Bit 6: Channel 2 (6) Request Status

Bit 7: Channel 3 (7) Request Status

6.2.1.4 Legacy 8237 DMA Command Registers

I/O Address: 0008h (DMA Channels 3-0)
00D0h (DMA Channels 7-4)
Attribute: Write only
Size: 8 bits
Default value: 00h

Bits 1-0: **Reserved.** Always 00b

Bit 2: Group Enable
0: Channels 3-0 (7-4) enabled
1: Channels 3-0 (7-4) disabled

Bit 3: **Reserved.** Always 0

Bit 4: Arbitration Priority
0: Channels 3-0 (7-4) enabled
1: Channels 3-0 (7-4) disabled

Bit 5: **Reserved.** Always 0

Bit 6: DMA Request (DREQ) Active Level
0: DREQ[3-0 (7-4)] are active high
1: DREQ[3-0 (7-4)] are active low

NOTE: For compatibility reasons this bit is supported, but it should always be written to zero for proper operation in the PC87560's system environment.

Bit 7: DMA Acknowledge (DACK) Active Level
0: DACK[3-0 (7-4)] are active low
1: DACK[3-0 (7-4)] are active high
NOTE: For compatibility reasons this bit is supported, but it should always be written to zero for proper operation in the PC87560's system environment.

6.2.1.5 Legacy 8237 DMA Soft Request Registers

I/O Address: 0009h (DMA Channels 3-0)
00D2h (DMA Channels 7-4)
Attribute: Write only
Size: 8 bits
Default value: 00h

Bits 0-1: Channel Select Bits

Bit 1	Bit 0	Description
0	0	DMA Channel 0 (4) selected
0	1	DMA Channel 1 (5) selected
1	0	DMA Channel 2 (6) selected
1	1	DMA Channel 3 (7) selected

Bit 2: Request bit
0: Clear request bit associated with the channel selected by bits 1-0 of this I/O write.
1: Set request bit associated with the channel selected by bits 1-0 of this I/O write.

Bits 7-3: **Reserved**.

6.2.1.6 Legacy 8237 DMA Write Single Mask Registers

I/O Address: 000Ah (DMA Channels 3-0)
00D4h (DMA Channels 7-4)
Attribute: Write only
Size: 8 bits
Default value: 04h

Bits 1-0: Channel Select Bits

Bit 1	Bit 0	Description
0	0	DMA Channel 0 (4) selected
0	1	DMA Channel 1 (5) selected
1	0	DMA Channel 2 (6) selected
1	1	DMA Channel 3 (7) selected

Bit 2: Mask bit

0: Clear mask bit associated with the channel selected by bits 1-0 of this I/O write.
1: Set mask bit associated with the channel selected by bits 1-0 of this I/O write.

NOTE: The mask bits effected by this I/O write are physically the same registers that are set by a Legacy 8237 DMA Master Clear Register I/O write cycle, cleared by a Legacy 8237 DMA Clear Mask Register I/O write cycle or written when writing to the DMA All Mask Bits Registers.

Bits 7-3: Reserved.

6.2.1.7 Legacy 8237 DMA Channel Mode Registers

I/O Address: 000Bh (DMA Channels 3-0)
00D6h (DMA Channels 7-4)
Attribute: Write only
Size: 8 bits
Default value: 00h

Bits 1-0: Channel Select Bits

Bit 1	Bit 0	Description
0	0	DMA Channel 0 (4) selected
0	1	DMA Channel 1 (5) selected
1	0	DMA Channel 2 (6) selected
1	1	DMA Channel 3 (7) selected

Bits 3-2: Transfer Type

Bit 3	Bit 2	Description
0	0	Verify Transfer
0	1	Memory Write Transfer
1	0	Memory Read Transfer
1	1	**Illegal**

Bit 4: Autoinitialize Enable

0: Autoinitialization disabled
1: Autoinitialization enabled

Bit 5: DMA Address Increment/Decrement

0: Address increments
1: Address decrements

Bits 7-6: Transfer Mode

Bit 7	Bit 6	Description
0	0	Demand Transfer Mode
0	1	Single Transfer Mode
1	0	Block Transfer Mode
1	1	Cascade Mode (This option is **illegal** in the PC87560 and will not be tested.)

6.2.1.8 DMA Channel Extended Mode Registers

I/O Address: 040Bh (DMA Channels 3-0)
04D6h (DMA Channels 7-5)
Attribute: Write only
Size: 8 bits
Default value: 00h

Bits 1-0: Channel Select Bits

Bit 1	Bit 0	Description
0	0	DMA Channel 0 selected
0	1	DMA Channel 1 (5) selected
1	0	DMA Channel 2 (6) selected
1	1	DMA Channel 3 (7) selected

Bits 3-2: DMA Cycle Timing Mode

Bit 3	Bit 2	Description
0	0	ISA Compatible timing
0	1	Type “A” Timing mode
1	0	Type “B” Timing mode
1	1	Type “F” Timing mode

Bits 7-4: Reserved.

NOTE: The Slave Distributed DMA registers do not provide support capabilities for these DMA Extended Mode Registers, so these two registers are accessible via these I/O addresses in all operating modes of the DMA Controller (that is these registers are accessible and functional in Legacy Mode, Distributed Master DMA Mode and Distributed Slave DMA Mode.) No other DMA Controller registers are accessible in their Legacy I/O space during Distributed Slave DMA Mode.

6.2.1.9 Legacy 8237 DMA Clear Byte Pointer Registers

I/O Address: 000Ch (DMA Channels 3-0)
00D8h (DMA Channels 7-4)
Attribute: Write only
Size: 8 bits
Default value: The Byte Pointer points to the low order byte.

This write only byte pointer register allows the current address and count internal byte pointer to be reset to the low order byte. There are two separate byte pointers, one for DMA Channels 3-0 and one for DMA Channels 7-4. The command is executed prior to accessing a current address or count register so that the register contents will be accessed in the proper sequence. The data value written during this command is ignored so any value causes the byte pointer reset operation. After a power on reset the internal byte pointer is reset to zero and thus points to the low order byte.

NOTE: Writing the Legacy 8237 DMA Master Clear Register(s) will also clear the associated byte pointer.

6.2.1.10 Legacy 8237 DMA Master Clear Registers

I/O Address: 000Dh (DMA Channels 3-0)
00DAh (DMA Channels 7-4)
Attribute: Write only
Size: 8 bits
Default value: undefined

This write only register causes the associated DMA Channels to go into a power on reset condition. The Command, Status, and Soft Request registers are cleared. The mask register bits are set to ones and the internal byte pointer is reset to zero for the associated DMA Channels. The data value written during this command is ignored so any value causes the master clear operation.

NOTE: The mask bits effected by this I/O write are physically the same registers that are cleared by a Legacy 8237 DMA Clear Mask Register I/O write cycle, written when writing the Legacy 8237 DMA Clear Write Single Mask Register cycle or written when writing to the DMA All Mask Bits Registers.

6.2.1.11 Legacy 8237 DMA TemporaryRegisters

I/O Address: 000Dh (DMA Channels 3-0)
00DAh (DMA Channels 7-4)
Attribute: Read only
Size: 8 bits
Default value: undefined

This read only register will provides the value of the Temporary memory-to-memory storage Register; however, sense the PC87560's Legacy 8237 DMA Controller does not support Memory-to-Memory transfers, a read of this register will always return the reset value of this register (which is 00h). This functionality is provide to be backwards compatible with the PC/AT.

6.2.1.12 Legacy 8237 DMA Clear Mask Registers

I/O Address: 000Eh (DMA Channels 3-0)
00DCh (DMA Channels 7-4)
Attribute: Write only
Size: 8 bits
Default value: undefined

This write only register causes the associated DMA Channels' mask register bits to be cleared to zeros. All four associated channels are unmasked and ready to sample the DREQ signals.

The data value written during this command is ignored so any value causes the mask clear operation.

NOTE: The mask bits effected by this I/O write are physically the same registers that are set by a Legacy 8237 DMA Master Clear Register I/O write cycle, written when writing the Legacy 8237 DMA Clear Write Single Mask Register cycle or written when writing to the DMA All Mask Bits Registers.

6.2.1.13 Legacy 8237 DMA All Mask Registers

I/O Address: 000Fh (DMA Channels 3-0)
00DEh (DMA Channels 7-4)
Attribute: Read/Write
Size: 8 bits
Default value: 0Fh

Bit 0: DMA Channel 0 (4) mask bit
0: Mask bit clear
1: Mask bit set

Bit 1: DMA Channel 1 (5) mask bit
0: Mask bit clear
1: Mask bit set

Bit 2: DMA Channel 2 (6) mask bit
0: Mask bit clear
1: Mask bit set

Bit 3: DMA Channel 3 (7) mask bit
0: Mask bit clear
1: Mask bit set

Bits 4-7: Reserved.

NOTE: The mask bits effected by this I/O write are physically the same registers that are cleared by a Legacy 8237 DMA Clear Mask Register I/O write cycle, set by a Legacy 8237 DMA Master Clear Register I/O write cycle or written when writing the Legacy 8237 DMA Clear Write Single Mask Register cycle.

6.2.1.14 Legacy 8237 DMA Low Page Segment Address Registers

I/O Addresses: 0080h-008Fh
Attribute: Read/Write
Size: 8 bits
Default value: Undefined

Legacy I/O Address	Register Function
0080h	Legacy Support (This register is writable and readable and may be used as a scratch pad register.)
0081h	DMA Channel 2 Low Page Segment Address Register
0082h	DMA Channel 3 Low Page Segment Address Register
0083h	DMA Channel 1 Low Page Segment Address Register
0084h	Legacy Support (This register is writable and readable and may be used as a scratch pad register.)
0085h	Legacy Support (This register is writable and readable and may be used as a scratch pad register.)
0086h	Legacy Support (This register is writable and readable and may be used as a scratch pad register.)
0087h	DMA Channel 0 Low Page Segment Address Register
0088h	Legacy Support (This register is writable and readable and may be used as a scratch pad register.)
0089h	DMA Channel 6 Low Page Segment Address Register
008Ah	DMA Channel 7 Low Page Segment Address Register
008Bh	DMA Channel 5 Low Page Segment Address Register
008Ch	Legacy Support (This register is writable and readable and may be used as a scratch pad register.)
008Dh	Legacy Support (This register is writable and readable and may be used as a scratch pad register.)
008Eh	Legacy Support (This register is writable and readable and may be used as a scratch pad register.)
008Fh	Legacy Support (This register is writable and readable and may be used as a scratch pad register.)

Seven of the sixteen Low Page Segment Address Registers are used to provide the address bits 23-16 (for DMA Channels 3-0) and address bits 23-17 (for DMA Channels 7-5), for their associated DMA transfer cycles.

The other nine 8-bit Low Page Segment Address Registers are provide for Legacy Support only and have no function other than providing nine bytes of scratch-pad register space.

6.2.1.15 Legacy 8237 DMA High Page Segment Address Registers

I/O Addresses: 0480h-048Fh
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Legacy I/O Address	Register Function
0480h	**Reserved.** (Always read as 00h.)
0481h	DMA Channel 2 High Page Segment Address Register
0482h	DMA Channel 3 High Page Segment Address Register
0483h	DMA Channel 1 High Page Segment Address Register
0484h	**Reserved.** (Always read as 00h.)
0485h	**Reserved.** (Always read as 00h.)
0486h	**Reserved.** (Always read as 00h.)

Legacy I/O Address	Register Function
0487h	DMA Channel 0 High Page Segment Address Register
0488h	**Reserved.** (Always read as 00h.)
0489h	DMA Channel 6 High Page Segment Address Register
048Ah	DMA Channel 7 High Page Segment Address Register
048Bh	DMA Channel 5 High Page Segment Address Register
048Ch	**Reserved.** (Always read as 00h.)
048Dh	**Reserved.** (Always read as 00h.)
048Eh	**Reserved.** (Always read as 00h.)
048Fh	**Reserved.** (Always read as 00h.)

The High Page Segment Address Registers are used to provide the address bits 31-24 for the DMA Channels 7-5 and 3-0, during their associated DMA transfer cycles.

Writes to a DMA Channel's Base Address Register or Low Page Segment Address Register will result in clearing that DMA Channel's High Page Segment Address Register to all zeros.

6.2.1.16 Distributed DMA Slave Mode Register

When the Legacy 8237 DMA Controller is programmed to operate in Distributed DMA Slave Mode, its registers will be accessed through the Distributed DMA I/O addresses listed in the table below. Refer to Section 3.2.1 LEGACY 8237 DMA CONTROLLER REGISTERS for information describing the I/O addresses via which the Legacy 8237 DMA Controller's register may be accessed in Legacy Mode or Distributed DMA Master Mode.

One should note that the registers listed in this section and Section 3.2.2 Section 3.2.1 LEGACY 8237 DMA CONTROLLER REGISTERS are physically the same registers being accessed via different I/O address locations.

Legacy Mode is enabled when: The Global DMA Channel Remapping Enable bit equals 0 and the Distributed DMA Slave vs. Legacy DMA bit equals 0.

The Global DMA Channel Remapping Enable bit is Bit 0 of the Function 1 (I/O) DMA Remap Base Address Register at configuration offset 4Ch-4Fh.

The Distributed DMA Slave vs. Legacy DMA bit is Bit 1 of the Function 1 (I/O) DMA Remap Base Address Register at configuration offset 4Ch-4Fh.

Distributed Master DMA Mode is enabled when: The Global DMA Channel Remapping Enable bit equals 1. The state of the Distributed DMA Slave vs. Legacy DMA bit has no function when the Global DMA Channel Remapping Enable bit equals 1.

Distributed Slave DMA Mode is enabled when: The Global DMA Channel Remapping Enable bit equals 0 and the Distributed DMA Slave vs. Legacy DMA bit equals 1.

When operating in the Distributed DMA Slave Mode, only those I/O addresses associated with channels that have been enabled to be remapped in the FUNCTION 1 (I/O) 8237 DMA CONTROL REGISTER will be supported. The following table has seven, sixteen byte ranges which are associated with the seven possible channels that may be supported.

DDBASE in the following Table stands for Distributed DMA Base address, which is equal to Bits 31-7 of the DMA Remap Base Address Register concatenated with seven zero bits ({31-7, 7'b000_0000}).

The Distributed DMA Base Address Register is a Function 1 configuration registers located at offset 4Ch-4Fh.

Distribute DMA I/O Address	DMA Channel	Read/Write	Register Function	Legacy I/O Address Locations
DDBASE+00h	0	Write	Base & Current Address register, Bits 7-0	0000h, Byte Pointer = 0
DDBASE+00h	0	Read	Current Address register, Bits 7-0	0000h, Byte Pointer = 0
DDBASE+01h	0	Write	Base & Current Address register, Bits 15-8	0000h, Byte Pointer = 1
DDBASE+01h	0	Read	Current Address register, Bits 15-8	0000h, Byte Pointer = 1
DDBASE+02h	0	Read/Write	Low Page Segment Address register	0087h
DDBASE+03h	0	Read/Write	High Page Segment Address register	0487h
DDBASE+04h	0	Write	Base & Current Word Count register, Bits 7-0	0001h, Byte Pointer = 0
DDBASE+04h	0	Read	Current Word Count register, Bits 7-0	0001h, Byte Pointer = 0
DDBASE+05h	0	Write	Base & Current Word Count register, Bits 15-8	0001h, Byte Pointer = 1
DDBASE+05h	0	Read	Current Word Count register, Bits 15-8	0001h, Byte Pointer = 1
DDBASE+06h	0	Read	**Reserved** (Always reads 00h)	
DDBASE+07h	0	Read	**Reserved** (Always reads 00h)	
DDBASE+08h	0	Write	DMA Channels 3-0, Command Register NOTE 1	0008h
DDBASE+08h	0	Read	DMA Channel 0 Status Register NOTE 2	0008h, Bits 4,0
DDBASE+09h	0	Write	DMA Channel 0 Request register NOTE3	0009h
DDBASE+09h	0	Read	**Reserved** (Always reads 00h)	
DDBASE+0Ah	0	Read	**Reserved** (Always reads 00h)	
DDBASE+0Bh	0	Write	DMA Channel 0 Mode register NOTE4	000Bh
DDBASE+0Bh	0	Read	**Reserved** (Always reads 00h)	
DDBASE+0Ch	0	Read	**Reserved** (Always reads 00h)	
DDBASE+0Dh	0	Write	DMA Channels 3-0, Master Clear NOTE 5	000Dh
DDBASE+0Dh	0	Read	**Reserved** (Always reads 00h)	
DDBASE+0Eh	0	Read	**Reserved** (Always reads 00h)	
DDBASE+0Fh	0	Read/Write	DMA Channel 0 Mask NOTE 6	000Fh, Bit 0
DDBASE+10h	1	Write	Base & Current Address register, Bits 7-0	0002h, Byte Pointer = 0
DDBASE+10h	1	Read	Current Address register, Bits 7-0	0002h, Byte Pointer = 0
DDBASE+11h	1	Write	Base & Current Address register, Bits 15-8	0002h, Byte Pointer = 1
DDBASE+11h	1	Read	Current Address register, Bits 15-8	0002h, Byte Pointer = 1
DDBASE+12h	1	Read/Write	Low Page Segment Address register	0083h
DDBASE+13h	1	Read/Write	High Page Segment Address register	0483h
DDBASE+14h	1	Write	Base & Current Word Count register, Bits 7-0	0003h, Byte Pointer = 0
DDBASE+14h	1	Read	Current Word Count register, Bits 7-0	0003h, Byte Pointer = 0

Distribute DMA I/O Address	DMA Channel	Read/Write	Register Function	Legacy I/O Address Locations
DDBASE+15h	1	Write	Base & Current Word Count register, Bits 15-8	0003h, Byte Pointer = 1
DDBASE+15h	1	Read	Current Word Count register, Bits 15-8	0003h, Byte Pointer = 1
DDBASE+16h	1	Read	**Reserved** (Always reads 00h)	
DDBASE+17h	1	Read	**Reserved** (Always reads 00h)	
DDBASE+18h	1	Write	DMA Channels 3-0, Command Register NOTE 1	0008h
DDBASE+18h	1	Read	DMA Channel 1 Status Register NOTE 2	0008h, Bits 5,1
DDBASE+19h	1	Write	DMA Channel 1 Request register NOTE3	0009h
DDBASE+19h	1	Read	**Reserved** (Always reads 00h)	
DDBASE+1Ah	1	Read	**Reserved** (Always reads 00h)	
DDBASE+1Bh	1	Write	DMA Channel 1 Mode register NOTE4	000Bh
DDBASE+1Bh	1	Read	**Reserved** (Always reads 00h)	
DDBASE+1Ch	1	Read	**Reserved** (Always reads 00h)	
DDBASE+1Dh	1	Write	DMA Channels 3-0, Master Clear NOTE 5	000Dh
DDBASE+1Dh	1	Read	**Reserved** (Always reads 00h)	
DDBASE+1Eh	1	Read	**Reserved** (Always reads 00h)	
DDBASE+1Fh	1	Read/Write	DMA Channel 1 Mask NOTE 6	000Fh, Bit 1
DDBASE+20h	2	Write	Base & Current Address register, Bits 7-0	0004h, Byte Pointer = 0
DDBASE+20h	2	Read	Current Address register, Bits 7-0	0004h, Byte Pointer = 0
DDBASE+21h	2	Write	Base & Current Address register, Bits 15-8	0004h, Byte Pointer = 1
DDBASE+21h	2	Read	Current Address register, Bits 15-8	0004h, Byte Pointer = 1
DDBASE+22h	2	Read/Write	Low Page Segment Address register	0081h
DDBASE+23h	2	Read/Write	High Page Segment Address register	0481h
DDBASE+24h	2	Write	Base & Current Word Count register, Bits 7-0	0005h, Byte Pointer = 0
DDBASE+24h	2	Read	Current Word Count register, Bits 7-0	0005h, Byte Pointer = 0
DDBASE+25h	2	Write	Base & Current Word Count register, Bits 15-8	0005h, Byte Pointer = 1
DDBASE+25h	2	Read	Current Word Count register, Bits 15-8	0005h, Byte Pointer = 1
DDBASE+26h	2	Read	**Reserved** (Always reads 00h)	
DDBASE+27h	2	Read	**Reserved** (Always reads 00h)	
DDBASE+28h	2	Write	DMA Channels 3-0, Command Register NOTE 1	0008h
DDBASE+28h	2	Read	DMA Channel 2 Status Register NOTE 2	0008h, Bits 6,2
DDBASE+29h	2	Write	DMA Channel 2 Request register NOTE3	0009h
DDBASE+29h	2	Read	**Reserved** (Always reads 00h)	
DDBASE+2Ah	2	Read	**Reserved** (Always reads 00h)	
DDBASE+2Bh	2	Write	DMA Channel 2 Mode register NOTE4	000Bh
DDBASE+2Bh	2	Read	**Reserved** (Always reads 00h)	
DDBASE+2Ch	2	Read	**Reserved** (Always reads 00h)	
DDBASE+2Dh	2	Write	DMA Channels 3-0, Master Clear NOTE 5	000Dh
DDBASE+2Dh	2	Read	**Reserved** (Always reads 00h)	

Distribute DMA I/O Address	DMA Channel	Read/Write	Register Function	Legacy I/O Address Locations
DDBASE+2Eh	2	Read	**Reserved** (Always reads 00h)	
DDBASE+2Fh	2	Read/Write	DMA Channel 2 Mask NOTE 6	000Fh, Bit 2
DDBASE+30h	3	Write	Base & Current Address register, Bits 7-0	0006h, Byte Pointer = 0
DDBASE+30h	3	Read	Current Address register, Bits 7-0	0006h, Byte Pointer = 0
DDBASE+31h	3	Write	Base & Current Address register, Bits 15-8	0006h, Byte Pointer = 1
DDBASE+31h	3	Read	Current Address register, Bits 15-8	0006h, Byte Pointer = 1
DDBASE+32h	3	Read/Write	Low Page Segment Address register	0082h
DDBASE+33h	3	Read/Write	High Page Segment Address register	0482h
DDBASE+34h	3	Write	Base & Current Word Count register, Bits 7-0	0007h, Byte Pointer = 0
DDBASE+34h	3	Read	Current Word Count register, Bits 7-0	0007h, Byte Pointer = 0
DDBASE+35h	3	Write	Base & Current Word Count register, Bits 15-8	0007h, Byte Pointer = 1
DDBASE+35h	3	Read	Current Word Count register, Bits 15-8	0007h, Byte Pointer = 1
DDBASE+36h	3	Read	**Reserved** (Always reads 00h)	
DDBASE+37h	3	Read	**Reserved** (Always reads 00h)	
DDBASE+38h	3	Write	DMA Channels 3-0, Command Register NOTE 1	0008h
DDBASE+38h	3	Read	DMA Channel 3 Status Register NOTE 2	0008h, Bits 7,3
DDBASE+39h	3	Write	DMA Channel 3 Request register NOTE3	0009h
DDBASE+39h	3	Read	**Reserved** (Always reads 00h)	
DDBASE+3Ah	3	Read	**Reserved** (Always reads 00h)	
DDBASE+3Bh	3	Write	DMA Channel 3 Mode register NOTE4	000Bh
DDBASE+3Bh	3	Read	**Reserved** (Always reads 00h)	
DDBASE+3Ch	3	Read	**Reserved** (Always reads 00h)	
DDBASE+3Dh	3	Write	DMA Channels 3-0, Master Clear NOTE 5	000Dh
DDBASE+3Dh	3	Read	**Reserved** (Always reads 00h)	
DDBASE+3Eh	3	Read	**Reserved** (Always reads 00h)	
DDBASE+3Fh	3	Read/Write	DMA Channel 3 Mask NOTE 6	000Fh, Bit 3
DDBASE+40h through DDBASE+4Fh			No Distributed DMA Slave Mode support	
DDBASE+50h	5	Write	Base & Current Address register, Bits 7-0	00C4h, Byte Pointer = 0
DDBASE+50h	5	Read	Current Address register, Bits 7-0	00C4h, Byte Pointer = 0
DDBASE+51h	5	Write	Base & Current Address register, Bits 15-8	00C4h, Byte Pointer = 1
DDBASE+51h	5	Read	Current Address register, Bits 15-8	00C4h, Byte Pointer = 1
DDBASE+52h	5	Read/Write	Low Page Segment Address register	008Bh
DDBASE+53h	5	Read/Write	High Page Segment Address register	048Bh

Distribute DMA I/O Address	DMA Channel	Read/Write	Register Function	Legacy I/O Address Locations
DDBASE+54h	5	Write	Base & Current Word Count register, Bits 7-0	00C6h, Byte Pointer = 0
DDBASE+54h	5	Read	Current Word Count register, Bits 7-0	00C6h, Byte Pointer = 0
DDBASE+55h	5	Write	Base & Current Word Count register, Bits 15-8	00C6h, Byte Pointer = 1
DDBASE+55h	5	Read	Current Word Count register, Bits 15-8	00C6h, Byte Pointer = 1
DDBASE+56h	5	Read	**Reserved** (Always reads 00h)	
DDBASE+57h	5	Read	**Reserved** (Always reads 00h)	
DDBASE+58h	5	Write	DMA Channels 3-0, Command Register NOTE 1	00D0h
DDBASE+58h	5	Read	DMA Channel 5 Status Register NOTE 2	00D0h, Bits 5,1
DDBASE+59h	5	Write	DMA Channel 5 Request register NOTE3	00D2h
DDBASE+59h	5	Read	**Reserved** (Always reads 00h)	
DDBASE+5Ah	5	Read	**Reserved** (Always reads 00h)	
DDBASE+5Bh	5	Write	DMA Channel 5 Mode register NOTE4	00D6h
DDBASE+5Bh	5	Read	**Reserved** (Always reads 00h)	
DDBASE+5Ch	5	Read	**Reserved** (Always reads 00h)	
DDBASE+5Dh	5	Write	DMA Channels 3-0, Master Clear NOTE 5	00DAh
DDBASE+5Dh	5	Read	**Reserved** (Always reads 00h)	
DDBASE+5Eh	5	Read	**Reserved** (Always reads 00h)	
DDBASE+5Fh	5	Read/Write	DMA Channel 5 Mask NOTE 6	00DEh, Bit 1
DDBASE+60h	6	Write	Base & Current Address register, Bits 7-0	00C8h, Byte Pointer = 0
DDBASE+60h	6	Read	Current Address register, Bits 7-0	00C8h, Byte Pointer = 0
DDBASE+61h	6	Write	Base & Current Address register, Bits 15-8	00C8h, Byte Pointer = 1
DDBASE+61h	6	Read	Current Address register, Bits 15-8	00C8h, Byte Pointer = 1
DDBASE+62h	6	Read/Write	Low Page Segment Address register	0089h
DDBASE+63h	6	Read/Write	High Page Segment Address register	0489h
DDBASE+64h	6	Write	Base & Current Word Count register, Bits 7-0	00CAh, Byte Pointer = 0
DDBASE+64h	6	Read	Current Word Count register, Bits 7-0	00CAh, Byte Pointer = 0
DDBASE+65h	6	Write	Base & Current Word Count register, Bits 15-8	00CAh, Byte Pointer = 1
DDBASE+65h	6	Read	Current Word Count register, Bits 15-8	00CAh, Byte Pointer = 1
DDBASE+66h	6	Read	**Reserved** (Always reads 00h)	
DDBASE+67h	6	Read	**Reserved** (Always reads 00h)	
DDBASE+68h	6	Write	DMA Channels 3-0, Command Register NOTE 1	00D0h
DDBASE+68h	6	Read	DMA Channel 6 Status Register NOTE 2	00D0h, Bits 6, 2
DDBASE+69h	6	Write	DMA Channel 6 Request register NOTE3	00D2h
DDBASE+69h	6	Read	**Reserved** (Always reads 00h)	
DDBASE+6Ah	6	Read	**Reserved** (Always reads 00h)	
DDBASE+6Bh	6	Write	DMA Channel 6 Mode register NOTE4	00D6h

Distribute DMA I/O Address	DMA Channel	Read/Write	Register Function	Legacy I/O Address Locations
DDBASE+6Bh	6	Read	**Reserved** (Always reads 00h)	
DDBASE+6Ch	6	Read	**Reserved** (Always reads 00h)	
DDBASE+6Dh	6	Write	DMA Channels 3-0, Master Clear NOTE 5	00DAh
DDBASE+6Dh	6	Read	**Reserved** (Always reads 00h)	
DDBASE+6Eh	6	Read	**Reserved** (Always reads 00h)	
DDBASE+6Fh	6	Read/Write	DMA Channel 6 Mask NOTE 6	00DEh, Bit 2
DDBASE+70h	7	Write	Base & Current Address register, Bits 7-0	00CCh, Byte Pointer = 0
DDBASE+70h	7	Read	Current Address register, Bits 7-0	00CCh, Byte Pointer = 0
DDBASE+71h	7	Write	Base & Current Address register, Bits 15-8	00CCh, Byte Pointer = 1
DDBASE+71h	7	Read	Current Address register, Bits 15-8	00CCh, Byte Pointer = 1
DDBASE+72h	7	Read/Write	Low Page Segment Address register	008Ah
DDBASE+73h	7	Read/Write	High Page Segment Address register	048Ah
DDBASE+74h	7	Write	Base & Current Word Count register, Bits 7-0	00CEh, Byte Pointer = 0
DDBASE+74h	7	Read	Current Word Count register, Bits 7-0	00CEh, Byte Pointer = 0
DDBASE+75h	7	Write	Base & Current Word Count register, Bits 15-8	00CEh, Byte Pointer = 1
DDBASE+75h	7	Read	Current Word Count register, Bits 15-8	00CEh, Byte Pointer = 1
DDBASE+76h	7	Read	**Reserved** (Always reads 00h)	
DDBASE+77h	7	Read	**Reserved** (Always reads 00h)	
DDBASE+78h	7	Write	DMA Channels 3-0, Command Register NOTE 1	00D0h
DDBASE+78h	7	Read	DMA Channel 7 Status Register NOTE 2	00D0h, Bits 7, 3
DDBASE+79h	7	Write	DMA Channel 7 Request register NOTE3	00D2h
DDBASE+79h	7	Read	**Reserved** (Always reads 00h)	
DDBASE+7Ah	7	Read	**Reserved** (Always reads 00h)	
DDBASE+7Bh	7	Write	DMA Channel 7 Mode register NOTE4	00D6h
DDBASE+7Bh	7	Read	**Reserved** (Always reads 00h)	
DDBASE+7Ch	7	Read	**Reserved** (Always reads 00h)	
DDBASE+7Dh	7	Write	DMA Channels 3-0, Master Clear NOTE 5	00DAh
DDBASE+7Dh	7	Read	**Reserved** (Always reads 00h)	
DDBASE+7Eh	7	Read	**Reserved** (Always reads 00h)	
DDBASE+7Fh	7	Read/Write	DMA Channel 7 Mask NOTE 6	00DEh, Bit 3

NOTE 1: When enabled, writes to DDBASE+08h, DDBASE+18h, DDBASE+28h and DDBASE+38h will all access the same physical register that is written at I/O address 0008h (DMA Channels 3-0, Command Register) when operating in Legacy Mode.

When enabled, writes to DDBASE+58h, DDBASE+68h and DDBASE+78h will all access the same physical register that is written at I/O address 00D0h (DMA Channels 7-4, Command Register) when operating in Legacy Mode.

NOTE 2: When being read the status bits of this channel must be duplicated such that bits 7-4 are all the same and reflect the Request Status of the channel, while bits 3-0 are all the same and reflect the Terminal Count Status of this Channel. It is the responsibility of the Distributed DMA Master to organize these bits appropriately.

NOTE 3: Only Bit 2 of this write contains any information and indicates whether or not the associated channel's Request Bit should be cleared to zero or set to a one.

NOTE 4: Bits 1-0 of this write are considered undefined, while the other six bits should be written to the associated channel's Mode Register control bits.

NOTE 5: When enabled, writes to DDBASE+0Dh, DDBASE+1Dh, DDBASE+2Dh and DDBASE+3Dh will all access the same physical register that is written at I/O address (DMA Channels 3-0, Master Clear) when operating in Legacy Mode.

When enabled, writes to DDBASE+5Dh, DDBASE+7Dh and DDBASE+7Dh will all access the same physical register that is written at I/O address (DMA Channels 7-4, Master Clear) when operating in Legacy Mode.

NOTE 6: Bit 0 of these read and writes indicates the status of the associated channels mask.

6.2.2 PROGRAMMABLE INTERRUPT CONTROLLERS (PIC) REGISTER DESCRIPTION

6.2.2.1 ICW1 - Initialization Command Word 1 (ICW1) Register

I/O Address: 0020h - Interrupt Controller 1
00A0h - Interrupt Controller 2
Attribute: Write only
Size: 8 bits
Default value: undefined

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence. Addresses 0020h and 00A0h are referred to as the base addresses of Interrupt Controller 1 and Interrupt Controller 2, respectively. An I/O write to the Interrupt Controller 1 and 2 base address with bit 4 equal to 1 is interpreted as ICW1. For AT compatible systems, three I/O writes to "base address +1" must follow the ICW1. The first write to "base address +1" performs ICW2, the second write performs ICW3, and the third write performs ICW4.

Bit 0: IC4 (ICW4 write required). This bit must be programmed to a 1.

Bit 1: SNGL (Single or cascade). This bit must be programmed to a 0.

0: Cascade mode

1: Single mode

Bit 2: ADI. This bit is ignored in the PC87560.

Bit 3: LTIM (Edge/level bank select). This bit is ignored in the PC87560. The Function 1 (I/O) Interrupt Level/Edge Triggering Control Register in the configuration registers controls each channel's edge/level triggering mechanism.

The Function 1 (I/O) Interrupt Level/Edge Triggering Control Register is located at configuration offset 67h-68h in the Function 1 configuration register space.

Bit 4: ICW/OCW select. This bit must be a 1 to select ICW1. After the fixed initialization sequence to ICW1, ICW2, ICW3 and ICW4, the controller base address is used to write to OCW2 and OCW3. Bit 4 is a 0 on writes to these registers. A 1 on this bit at any time will force the interrupt controller to interpret the write as an ICW1. The controller will then expect to see ICW2, ICW3, and ICW4.

Bits 7-5: ICW/OCW select. Always 000b.

6.2.2.2 ICW2 - Initialization Command Word 2 (ICW2) Register

I/O Address: 0021h - Interrupt Controller 1
00A1h - Interrupt Controller 2
Attribute: Write only
Size: 8 bits
Default value: undefined

Bits 2-0: Interrupt request level. When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt code representing the interrupt level to be serviced. This interrupt code is combined with bits [7:3] to form the complete interrupt vector driven onto the data bus during the second INTA# cycle. The code is as follows:

000b: IRQ0 (IRQ8 for ICU 2)

001b: IRQ1 (IRQ9 for ICU 2)

010b: IRQ2 (IRQ10 for ICU 2)

011b: IRQ3 (IRQ10 for ICU 2)

100b: IRQ4 (IRQ10 for ICU 2)

101b: IRQ5 (IRQ10 for ICU 2)

110b: IRQ6 (IRQ10 for ICU 2)

111: IRQ7 (IRQ15 for ICU 2)

Bits 7-3: Interrupt vector base address. Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.

6.2.2.3 ICW3 - Initialization Command Word 3 (ICW3) Register

I/O Address: 0021h - Interrupt Controller 1 - Master Unit
Attribute: Write only
Size: 8 bits

Default value: undefined

Bits 1-0: These bits must be programmed to 0.

Bit 2: Cascade interrupt controller IRQ connection. Bit 2 must always be programmed to a 1. This bit indicates that Interrupt Controller 2, the slave controller, is cascaded on interrupt request line two (IRQ2).

Bits 7-3: These bits must be programmed to 0.

6.2.2.4 ICW3 - Initialization Command Word 3 Register

I/O Address: 00A1h - Interrupt Controller 2 - Slave Unit
Attribute: Write only
Size: 8 bits
Default value: undefined

Bits 2-0: Slave identification code. The slave identification code must be programmed to 010b during the initialization sequence. The code stored in ICW3 is compared tothe incoming slave identification code broadcast by the master controller during interrupt acknowledge cycles.

Bits 7-3: These bits must be programmed to 0.

6.2.2.5 ICW4 - Initialization Command Word 4 Register

I/O Address: 0021h - Interrupt Controller 1
00A1h - Interrupt Controller 2
Attribute: Write only
Size: 8 bits
Default value: undefined

Both interrupt controllers must have ICW4 programmed as part of their initialization sequence.

Bit 0: Microprocessor mode. The Microprocessor Mode bit must be programmed to 1 to indicate that the interrupt controller is operating in an x86 based system. Never program this bit to 0.

Bit 1: AEO (automatic end of interrupt).

0: Normal End of Interrupt mode.

1: Automatic End of Interrupt mode.

Bit 2: Master/Slave in buffered mode. This bit should always be programmed to 0.

Bit 3: BUFM (buffered mode). This bit must be programmed to 0.

Bit 4: SFNM (special fully nested mode). SFNM should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.

Bits 7-5: These bits must be programmed to 0.

6.2.2.6 OCW1 - Operational Control Word 1 Register

I/O Address: 21h - Interrupt Controller 1
A1h - Interrupt Controller 2
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bits 7-0: Interrupt Request mask. When a one is written to any bit in this register, the corresponding IRQ(x) mask is set. When a zero is written to any bit in this register, the corresponding IRQ(x) mask bit is cleared, and interrupt requests will again be accepted by the controller. Note that masking IRQ2 in Interrupt Controller 1 will also mask the interrupt request from Interrupt Controller 2, which is physically cascaded to IRQ2.

6.2.2.7 OCW2 - Operational Control Word 2 Register

I/O Address: 20h - Interrupt Controller 1
A0h - Interrupt Controller 2
Attribute: Write only
Size: 8 bits
Default value: Undefined

Bits 2-0: Interrupt level select (L2, L1, L0). These bits determine the interrupt level which the Rotate on Specific Command or Set Priority Command is addressed to. If any of the other options are selected by Bits 7-5, these

three bits are don't cares.

Bit 2	Bit 1	Bit 0	Description
0	0	0	IRQ0(8)
0	0	1	IRQ1(9)
0	1	0	IRQ2(10)
0	1	1	IRQ3(11)
1	0	0	IRQ4(12)
1	0	1	IRQ5(13)
1	1	0	IRQ6(14)
1	1	1	IRQ7(15)

Bits 4-3: OCW2 select. When selecting OCW2, bits 3 and 4 must both be 0. If bit 4 is a 1, the interrupt controller interprets the write to this port as an ICW1. Therefore, always ensure that these bits are both 0 when writing to OCW2.

Bits 7-5: Rotate and EOI codes

Bit 7	Bit 6	Bit 5	Function
0	0	0	Rotate in auto EOI mode (clear)
0	0	1	Non-specific EOI command
0	1	0	No operation
0	1	1	Specific EOI command
1	0	0	Rotate in auto EOI mode (set)
1	0	1	Rotate on non-specific EOI command
1	1	0	Set priority command
1	1	1	Rotate on specific EOI command

6.2.2.8 OCW3 - Operational Control Word 3 Register

I/O Address: 0020h - Interrupt Controller 1
00A0h - Interrupt Controller 2
Attribute: Read/Write
Size: 8 bits
Default value: Undefined

Bits 1-0: Register read command

00: No action

01: No action

10: Read Interrupt Request Register (IRR)

11: Read In Service Register (ISR)

Bit 2: Poll mode command

Bits 4-3: OCW3 select. When selecting OCW3, Bit 3 must be a 1 and Bit 4 must be a 0. If Bit 4=1, the interrupt controller interprets the write to this port as an ICW1. There, always ensure that Bits [4:3]=01b when writing to OCW3.

Bit 5: ESMM (enable special mask mode)

Bit 6: SMM (special mask mode)

Bit 7: **Reserved.**

6.2.3 PROGRAMMABLE INTERVAL TIMER (PIT) REGISTER DESCRIPTION

6.2.3.1 PIT Status Byte Format Registers

I/O Address: 0040h - Counter 0
0041h - Counter 1
0042h - Counter 2
Attribute: Read only
Size: 8 bits
Default value: Bit 7 = 0, Bits 6-0 = undefined

Bit 0: Counter type status

Bits 3-1: Mode selection status

Bit 3	Bit 2	Bit 1	Mode
0	0	0	0
0	0	1	1
x	1	0	2
x	1	1	3
1	0	0	4
1	0	1	5

Bits 5-4: Read/Write selection status

Bit 5	Bit 4	Function
0	0	Counter latch command
0	1	R/W least significant byte (LSB)
1	0	R/W most significant byte (MSB)
1	1	R/W LSB then MSB

Bit 6: Counter register status

Bit 7: Counter Out pin status

6.2.3.2 Counter Access Ports Register

I/O Address: Counter 0, System Timer - 0040h
Counter 1, Refresh Request - 0041h
Counter 2, Speaker Tone - 0042h
Attribute: Read/Write
Size: 8 bits
Default value: undefined

Bits 7-0: Counter port bit (x). Each count I/O port address is used to program the 16 bit count register. The order of programming, either LSB only, MSB only, LSB then MSB, is defined with the Interval Counter Control Register at I/O port 43h. The counter I/O port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

6.2.3.3 Timer Control Word Register

I/O Address: 43h
Attribute: Write only
Size: 8 bits
Default value: undefined

Bit 0: Binary/BCD countdown select

0: binary

1: BCD (Binary Coded Decimal)

Bits 3-1: Counter mode select

Bit 3	Bit 2	Bit 1	Function
0	0	0	Out signal on end of count (=0) - mode 0
0	0	1	Hardware retriggerable one-shot 0 - mode 1
x	1	0	Rate generator (divide by n counter) - mode 2
x	1	1	Square wave output - mode 3
1	0	0	Software triggered strobe - mode 4
1	0	1	Hardware triggered strobe - mode 5

Bits 5-4: Read/Write Select

Bit 5	Bit 4	Function
0	0	Counter latch command
0	1	R/W least significant byte (LSB)
1	0	R/W most significant byte (MSB)
1	1	R/W LSB then MSB

Bits 7-6: Counter select

Bit 7	Bit 6	Function
0	0	Counter 0 select
0	1	Counter 1 select
1	0	Counter 2 select
1	1	Read back command

6.2.4 KEYBOARD CONTROLLER REGISTER DESCRIPTION

6.2.4.1 Keyboard Controller Data Register

I/O Address: KBCBAR+0h (Default I/O Address is 0060h, but it is remappable via the Keyboard Controller Base Address Register to anywhere in the 32-bit I/O address range.)
Attribute: Read/Write
Size: 8 bits
Default value: undefined

Read

When the PS87422 is configured in PS2 Mouse mode (System Configuration Register bit 15=1), KINT and MINT are both latched on a low to high transition. Reads to this address location clears the PC87560 internal PIC latches for keyboard and mouse interrupts. The data is ignored. This cycle is passed to the external keyboard controller.

Write

Write to address KBCBAR+0h with data bit 1 equal to a 0, and previous to this write to address KBCBAR+4h with data equal to D1h has occurred, the PC87560 output signal FA20 will asserted active. FA20 will remain active until either a write to address 92h bit 1 equal to a 1, or write to 64h data equal to D1h followed by a write to 60h with data bit 1 equal to a 1. The PC87560 will ignore writes to address 60h if a write to 64h data equal to D1h has not occurred previously. This cycle is passed to the external keyboard controller.

6.2.4.2 Keyboard Controller Command Register

I/O Address: KBCBAR+4h(Default I/O Address is 0064h, but it is remappable via the Keyboard Controller Base Address Register to anywhere in the 32-bit I/O address range.)

Attribute: Read/Write
Size: 8 bits
Default value: undefined

Read

This cycle is forwarded to the external keyboard controller and KBCS# is generated.

Write

Writes to address 64h with data equal to D1h allow writes to address 60h to occur. Write to address 64h data equal to FEh generates a "fast reset" (FRST# asserted). This cycle is passed to the external keyboard controller and KBCS# is generated.

6.2.5 PORT 61 REGISTER

I/O Address: 0061h
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bit 0: Timer Counter 2 Enable. This bit controls the GATE input to counter 2.

0: Counter 2 counting is disabled

1: Counter 2 counter is enabled

Bit 1: Speaker Data. (ANDed with counter 2 OUT to drive SPKR output.)

0: Speaker output (SPKR) disabled.

1: Speaker output (SPKR) enabled and will oscillate at the count 2 OUT frequency.

Bit 2: NMI Enable. When this bit is a 0, an NMI will be generated (if NMI is enabled through Port 70, Bit 7 must be a 0) if a 0 is detected on the SERR# input pin or if any one of the error bits (Bits 15-11) is set in the PCI Status Register. When this bit is a one, NMI is disabled and cleared.

Bit 3: IOCHK# NMI Enable. When this bit is 1, IOCHK# NMIs are disabled and cleared. When this bit is 0, IOCHK# NMIs are enabled. The IOCHK# signal is input to the PC87560 through the serial interrupt bus (SINT)

Bit 4: Refresh Cycle Toggle

Bit 5: Timer 2 OUT Status

Bit 6: IOCHK# NMI Source Status. This bit is set if a device asserts IOCHK# on an ISA bus and this information is passed to the 420 through the serial interrupt bus. This interrupt source is enable by setting Bit 3 to 0. To reset the interrupt, set Port 61 Bit 3 to 1. This bit is read only.

Bit 7: NMI Status. Bit 7 is set if a system board agent (PCI devices or main memory) detects a system board error and pulses the PCI SERR# line or if any one of the error bits (Bits 15-11) is set in the PCI Status Register. This interrupt source is enabled by setting Port 61 Bit 2 to 0. To reset the interrupt, set Port 61 Bit 2 to 1. This bit is read only.

6.2.6 PORT 70 REGISTER

I/O Address 0070h
Attribute: Read/Write
Size: 8 bits
Default value: xx

A write to this address generates RTCALE. A read or write to this address generates RTCCS# if System I/O Configuration Register Bit 4=1.

Bits 6-0: Real Time Clock (RTC) Index Address. Used by the Real Time Clock as an index address to indicate which internal RTC register (or CMOS RAM address) is to be accessed via the I/O address port 0071h. The PC87560 records a copy of these bits every time they are written, so that the PC87560 may support the CMOS Locking of RTC Indices of 19h and 38h-3Fh (enabled via Port 92 Register, Bits 5 and 3 respectively). When this I/O address is read, the value presented to the PCI Bus will be the value driven onto the FX Bus by the external RTC and will not be the internal PC87560 copy discussed here.

Bit 7: NMI Enable. Setting this bit to a 1 disables all NMI sources. Setting this bit to a 0 enables the NMI interrupt. Reset value is a 1.

6.2.7 REAL TIME CLOCK DATA REGISTER

I/O Address: 0071h
Attribute: Read/Write
Size: 8 bits
Default value: undefined

A read or write to this address generates RTCCS# and the cycle is forwarded to the FX Bus as long as that cycle is not a write to a Locked CMOS RAM location.

6.2.8 PORT 92 REGISTER

I/O Address: 92h
Attribute: Read/Write
Size: 8 bits
default value: 00h

Bit 0: Alternate Fast Reset. A one written into this bit field causes a soft reset (CPUINIT) pulse of 16 PCI clocks duration. Before another CPUINIT pulse can be generated, this bit must be written back to a zero. This signal is ORed with the output of the RESET snoop block.

Bit 1: Alternate Fast Gate A20. Writing a zero to this bit causes the FA20 signal to be driven low (assuming the snooping mechanism hasn't taken FA20 high and the USB Legacy Keyboard support is disabled). Writing a one to this bit causes the FA20 signal to be driven high. This signal is ORed with the output of the GATEA20 snoop block.

Bit 2: **Reserved.**

Bit 3: CMOS Lock Enable for RTC Index address 19h bit.

0: Data accesses to Port 71h with the RTC Index address set to 38h-3Fh, the PC87560 will generate an active low RTCCS# and will forward the access to the FX Bus. (Default value)

1: Data writes to Port 71h with the RTC Index address set to 38h-3Fh, the PC87560 will not generate an active low RTCCS# and will not forward the write cycle to the FX Bus; nonetheless any such PCI I/O Write will be acknowledged by the PC87560 as if it has completed. Once this bit is set to one, nothing can unlock it until a hardware reset is detected (RESET_IN# is 0). A read cycle from Port 71h during a lock to the RTC Index address 38h-3Fh does generate an active low RTCCS# and the read cycle is forwarded to the FX Bus. Thus reads from the RTC Index address 38h-3Fh are unaffected by this bit.

Bit 4: **Reserved.**

Bit 5: CMOS Lock Enable for Index 19h bit.

0: Data accesses to Port 71h with the RTC Index address set to 19h, the PC87560 will generate an active low RTCCS# and will forward the access to the FX Bus. (Default value)

1: Data writes to Port 71h with the RTC Index address set to 19h, the PC87560 will not generate an active low RTCCS# and will not forward the write cycle to the FX Bus; nonetheless any such PCI I/O Write will be acknowledged by the PC87560 as if it has completed. Once this bit is set to 1, nothing can unlock it until a hardware reset is detected (RESET_IN# is 0). A read cycle from Port 71h during a lock to the RTC Index address 19h does generate an active low RTCCS# and the read cycle is forwarded to the FX Bus. Thus reads from the RTC Index address 19h are unaffected by this bit.

Bits 7-6: **Reserved.**

6.2.9 ADVANCED POWER MANAGEMENT CONTROL PORT (APMC)

I/O Address: 00B2h
Attribute: Read/Write
Size: 8 bits
Default value: 00h

This register passes data (APM Commands) between the OS and the SMI handler. In addition, writes can generate a SMI. The PC87560 is not affected by the data in this register.

Bits 7-0: APM Control Port (APMC). Writes to this register store data in the APMC Register and Reads return the last data written. In addition, writes generate a SMI if Bit 23 and Bit 25 of the Global SMI I/O Trap Enable Register are both set to 1. Reads from this register do not generate an SMI.

6.2.10 ADVANCED POWER MANAGEMENT STATUS PORT (APMS)

I/O Address: 00B3h
Attribute: Read/Write
Size: 8 bits
Default value: 00h

This register passes status information between the OS and the SMI handler. The PC87560 is not affected by the data in this register.

Bits 7-0: APM Status Port (APMS). Writes store data in this register and reads return the last data written.

6.2.11 PORT F0 REGISTER

I/O Address: 00F0h
Attribute: Write only
Size: 8 bits
Default value: 00h

When coprocessor error reporting is enabled in the PC87560 (Coprocessor Error Enable bit 3=1 in the System Configuration Register), the PC87560 generates a numeric coprocessor interrupt when it receives an error signal (FERR# asserted) from the CPU's coprocessor. Writing to I/O address F0H, when FERR# is asserted, causes the PC87560 to assert IGNNE# and negate the coprocessor interrupt. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted, writing to I/O address F0H does not effect IGNNE#.

Figure 1.1 — Numeric Error

6.2.12 IDE CHANNEL 2 DATA AND COMMAND REGISTERS

I/O Address: 0170h - 0177h (programmable)
Attribute: Read/Write
Size: 8 bits
Default value: undefined

The PC87560 provides the control signals for the secondary IDE interface. See ANSI ATA Standard Rev. 3.2 for register definitions.

Secondary Data and Command Block Registers		
Address	**Read Function**	**Write Function**
0170h	Data (16 bits)	Data (16 bits)
0171h	Error register	Features
0172h	Sector count	Sector count
0173h	Sector number	Sector number

Secondary Data and Command Block Registers		
0174h	Cylinder low	Cylinder low
0175h	Cylinder high	Cylinder high
0176h	Drive/head	Drive/head
0177h	Status	Command

6.2.13 IDE CHANNEL 1 DATA AND COMMAND REGISTERS

I/O Address: 01F0h - 01F7h (programmable)
Attribute: Read/Write
Size: 8 bits
Default value: undefined

The PC87560 provides the control signals for the primary IDE interface. See ANSI ATA Standard Rev. 3.2 for register definitions.

Primary Data and Command Block Registers		
Address	**Read Function**	**Write Function**
01F0h	Data (16 bits)	Data (16 bits)
01F1h	Error register	Features
01F2h	Sector count	Sector count
01F3h	Sector number	Sector number
01F4h	Cylinder low	Cylinder low
01F5h	Cylinder high	Cylinder high
01F6h	Drive/head	Drive/head
01F7h	Status	Command

6.2.14 UART 2 REGISTERS

I/O Address: 02F8h-02FFh (programmable)
Attribute: Read/Write
Size: 8 bits
Default value: undefined

6.2.15 IDE CHANNEL 2 CONTROL REGISTER

I/O Address: 0376h (programmable)
Attribute: Read/Write
Size: 8 bits
Default value: undefined

The PC87560 provides the control signals for the secondary IDE interface. See ANSI ATA Standard Rev. 3.2 for register definitions.

Secondary Control Block Registers		
Address	**Read Function**	**Write Function**
0376h	Alternate Status	Device control

6.2.16 PARALLEL PORT REGISTERS

I/O Address: 0378h - 037Fh (programmable)
Attribute: Read/Write
Size: 8 bits
Default value: undefined

6.2.17 FLOPPY DISK CONTROLLER REGISTERS

I/O Address: 03F0h - 03F7h (programmable)
Attribute: Read/Write
Size: 8 bits
Default value: undefined

6.2.18 IDE CHANNEL 1 CONTROL REGISTERS

I/O Address: 03F6h (programmable)
Attribute: Read/Write
Size: 8 bits
Default value: undefined

The PC87560 provides the control signals for the primary IDE interface. See ANSI ATA Standard Rev. 3.2 for register definitions.

Primary Control Block Registers		
Address	**Read Function**	**Write Function**
03F6h	Alternate Status	Device control

6.2.19 SERIAL PORT 1 REGISTERS

I/O Address: 03F8h-0 3FFh (programmable)
Attribute: Read/Write
Size: 8 bits
Default value: undefined

6.2.20 CHANNEL 1 BUS MASTER IDE COMMAND REGISTER

I/O Address: BAR4 + 00h
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bit 0: Start/Stop Bus Master The Start bit is cleared when the last transfer for a region is performed (the EOT flag is set in the descriptor for that region) or when the interrupt flag is set for this channel.

0: Stop Bus Master transfers. Master operation can be halted by writing a 0 to this bit. All state information is lost when a 0 is written.

1: Start Bus Master transfers. This enables bus master operation of the controller. Bus master operation begins when this bit is detected changing from zero to one. The controller will transfer data between the IDE device and memory only when this bit is set.

Bits 2-1: Reserved.

Bit 3: Read or Write Control

0: PCI bus master read

1: PCI bus master write

Bits 7-4: Reserved.

6.2.21 CHANNEL 1 BUS MASTER IDE STATUS REGISTER

I/O Address: BAR4 + 02h
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Writes to this register cause bit(s) to be reset. Bit 1 and 2 are reset whenever the register is written with in the corresponding bit location. Default value is 00h.

Bit 0: Bus Master IDE Active. This bit is set when the Start bit is written to the Bus Master IDE Command Register. This bit is cleared when the last transfer for a region is performed, where the EOT for that region is set in the region descriptor. It is also cleared when the Start bit is cleared in the Bus Master IDE Command Register

Bit 1: Error. This bit is set when the controller encounters an error in transferring data to/from memory. This bit is cleared when a 1 is written to it by software.

Bit 2: Interrupt. This bit is set by the rising edge of CH1_INT. This bit is cleared when a 1 is written to it by software.

Bits 4-3: Reserved.

Bit 5: Drive 1 DMA Capable. Bus Master IDE transfers to drive 1 on channel 1 are qualified by this bit.

0: Drive 1 is not DMA capable

1: Drive 1 is DMA capable

Bit 6: Drive 2 DMA Capable. Bus Master IDE transfers to drive 2 on channel 1 are qualified by this bit.

0: Drive 2 is not DMA capable

1: Drive 2 is DMA capable

Bit 7: Simplex only. This read-only bit is always 0 indicating that both channels can operate independently and can be used at the same time.

6.2.22 CHANNEL 1 BUS MASTER IDE PRD TABLE ADDRESS REGISTER

I/O Address: BAR4 + 04h
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

Bits 1-0: Reserved.

Bits 31-2: Base address of channel 1 Descriptor table. Corresponds to AD[31:2].

6.2.23 CHANNEL 2 BUS MASTER IDE COMMAND REGISTER

I/O Address: BAR4 + 08h
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bit 0: Start/Stop Bus Master. The Start bit is cleared when the last transfer for a region is performed (the EOT flag is set in the descriptor for that region) or when the interrupt flag is set for this channel.

0: Stop Bus Master transfers. Master operation can be halted by writing a 0 to this bit. All state information is lost when a 0 is written.

1: Start Bus Master transfers. This enables bus master operation of the controller. Bus master operation begins when this bit is detected changing from zero to one. The controller will transfer data between the IDE device and memory only when this bit is set.

Bits 2-1: Reserved.

Bit 3: Read or Write Control

0: PCI bus master read

1: PCI bus master write

Bits 7-4: Reserved.

6.2.24 CHANNEL 2 BUS MASTER IDE STATUS REGISTER

I/O Address: BAR4 + 0Ah
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Writes to this register cause bit(s) to be reset. Bit 1 and 2 are reset whenever the register is written with in the corresponding bit location. Default value is 00h.

Bit 0: Bus Master IDE Active. This bit is set when the Start bit is written to the Bus Master IDE Command Register. This bit is cleared when the last transfer for a region is performed, where the EOT for that region is set in the region descriptor. It is also cleared when the Start bit is cleared in the Bus Master IDE Command Register.

Bit 1: Error. This bit is set when the controller encounters an error in transferring data to/from memory. This bit is cleared when a 1 is written to it by software.

Bit 2: Interrupt. This bit is set by the rising edge of CH2_INT. This bit is cleared when a 1 is written to it by software.

Bits 4-3: Reserved.

Bit 5: Drive 1 DMA Capable. Bus Master IDE transfers to drive 1 on channel 2 are qualified by this bit.

0: Drive 1 is not DMA capable

1: Drive 1 is DMA capable

Bit 6: Drive 2 DMA Capable. Bus Master IDE transfers to drive 2 on channel 2 are qualified by this bit.

0: Drive 2 is not DMA capable

1: Drive 2 is DMA capable

Bit 7: Simplex only. This read-only bit is always 0 indicating that both channels can operate independently and can be used at the same time.

6.2.25 CHANNEL 2 BUS MASTER IDE PRD TABLE ADDRESS REGISTER

I/O Address: BAR4 + 0Ch
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

Bits 1-0: Reserved.

Bits 31-2: Base address of channel 2 Descriptor table. Corresponds to AD[31:2].

6.2.26 POWER MANAGEMENT REGISTERS

The following is a table listing all of the Power Management registers. The Power Management Base Address is determined by the Function 1 Power Management Base Address Register (PMBAR) located in the PCI Function 1 Configuration space at 20h-23h. There are 256 Power Management registers within the PC87560, most of them are listed as **Reserved**.

Any register listed as **Reserved** must always be read as all zeros. Also any bit within a register documented as **Reserved** must also be read as zero, unless specifically stated otherwise.

Offset from PMBAR	Register Name
00h	General Purpose I/O Register
01h	**Reserved.**
02h	Miscellaneous Status Register
03h	TRI-STATE Control Register
04h	Function Power Mode Register
05h	Serial Port 2 Power Mode Register
06h	Global Status Register
07h-0Bh	**Reserved.**
0Ch-0Fh	Global System Management Interrupt (SMI) I/O Trap Enable Register
10h-13h	**Reserved.**
14h-17h	Power Management Global Status Register
18h-19h	Primary Activity (PA) Enable Register
1Ah-1Bh	Secondary Activity (SA) Enable Register
1Ch-53h	**Reserved.**
54h-57h	System Event 1 Control Register

58h-5Bh	System Event 1 Status Register
5Ch-6Bh	**Reserved.**
6Ch-AFh	Zero Volt Suspend Shadow Registers
B0h-FFh	**Reserved.**

6.2.27 GENERAL PURPOSE I/O REGISTER

I/O Address: PMBAR + 00h
Attribute: Read/Write
Size: 8 bits
Default value: 00h

When writing to this register the value is written into the General Purpose output register. This General Purpose output register value is driven onto the associated pin if it is configured as a General Purpose output signal (this is determined by the Function1 General Purpose I/O Configuration Register and the Function 1 General Purpose I/O Direction Register.) For writes to this register, the following bit definitions are only valid if the General Purpose I/O pins are configured as General Purpose outputs. Writes to bits of this register with their associated General Purpose pin(s) configured as General Purpose inputs or as their alternate function have no visible effects outside of effecting the value in the register flip-flop itself.

When reading this I/O location, the actual value being driven onto the associated pin will be read if the associated GPIO[7:0] pin is configured to be operating as a GPIO pin (via the Function 1 General Purpose I/O Configuration Register at configuration offset 78h); otherswise the last value written to the corresponding bit will be read back. If a pin is configured as a General Purpose output signal, then reads from this I/O location should return the last value written to the associated bit(s) of this register (this assumes no signal contention on the pin itself). On the other hand, if a pin is configured as a General Purpose input, the data read from this I/O location will have no relationship to the last associated value written to this register.

Bit 0: GPIO0.
0: GPIO0 pin is 0
1: GPIO0 pin is 1

Bit 1: GPIO1.
0: GPIO1 pin is 0
1: GPIO1 pin is 1

Bit 2: GPIO2.
0: GPIO2 pin is 0
1: GPIO2 pin is 1

Bit 3: GPIO3.
0: GPIO3 pin is 0
1: GPIO3 pin is 1

Bit 4: GPIO4.
0: GPIO4 pin is 0
1: GPIO4 pin is 1

Bit 5: GPIO5.
0: GPIO5 pin is 0
1: GPIO5 pin is 1

Bit 6: GPIO6.

0: GPIO6 pin is 0

1: GPIO6 pin is 1

Bit 7: GPIO7.

0: GPIO7 pin is 0

1: GPIO7 pin is 1

6.2.28 MISCELLANEOUS STATUS REGISTER

I/O Address: PMBAR+02h
Attribute: Read Only
Size: 8 bits
Default value: 00h

Bit 0: IDE Channel 1 Write Buffer Status

0: Channel 1 write buffer is empty.

1: Channel 1 write buffer is not empty.

Bit 1: IDE Channel 2 Write Buffer Status

0: Channel 2 write buffer is empty.

1: Channel 2 write buffer is not empty.

Bits 7-2: Reserved.

6.2.29 TRI-STATE CONTROL REGISTER

I/O Address: PMBAR +03h
Attribute: Read/Write
Size: 8 bits
Default value: 00h

This register controls the power down state of various PC87560 pins. When a device/module is disabled or powered down (via its associated bit in the Function Power Mode Register, PMBAR+04h), and its associated bit in this register is set, the output pins of that device/module are placed in TRISTATE and the device/module input pins are gated within the I/O cell in a manner that reduces their leakage current.

If a device/module's TRI-STATE bit (in this register) is a zero, or the device/module's Power Mode bit (in PMBAR+04h) is set to a one (enabling the function), then the device/module's output drivers will be enabled.

Bit 0: Parallel Port/Floppy Multiplexed signals TRI-STATE Control.

0: drive associated outputs when powered down

1: TRI-STATE output drivers when powered down

The Parallel and Floppy Multiplexed signal pins will only be placed in TRI-STATE when the function associated with the presently selected pin operation is placed in power down. This means the following:

To TRI-STATE these signals, if these pins are operating as the Parallel Port, both this bit must be a one and Bit 0 of the Function Power Mode Register must be a zero.

To TRI-STATE these signals, if these pins are operating as a Floppy Disk, this bit must be a one and Bit 3 of the Function Power Mode Register must be a zero.

Bit 1: Serial Port 1 TRI-STATE Control.

0: drive associated outputs when powered down

1: TRI-STATE output drivers when powered down

Bit 2: Serial Port 2 and Serial Infrared TRI-STATE Control.

0: drive associated outputs when powered down

1: TRI-STATE output drivers when powered down

Bit 3: FDC TRI-STATE Control.

0: drive associated outputs when powered down

1: TRI-STATE output drivers when powered down

Bit 4: IDE TRI-STATE Control

0: drive associated outputs when powered down

1: TRI-STATE output drivers when powered down

If this bit is a one and Bit 4 of the Function Power Mode Register (IDE Channel 1 Enable bit) is a zero, then the output signals associated with IDE Channel 1 will be placed in TRI-STATE.

If this bit is a one and Bit 5 of the Function Power Mode Register (IDE Channel 2 Enable bit) is a zero, then the output signals associated with IDE Channel 2 will be placed in TRI-STATE.

NOTE: The IDE data bus (DD[15:0]) is shared between the two IDE channels and will only be guaranteed to be inputs both IDE Channels are disabled. In such a case this bit has no direct effect on the state of the DD[15:0] I/Os.

Bits 7-5: Reserved.

6.2.30 FUNCTION POWER MODE REGISTER

I/O Address: PMBAR+04h
Attribute: Read/Write
Size: 8 bits
Default value: 3Fh

To conserve power, this register is used to enable/disable individual functions such as Parallel Port, Serials Ports, Floppy Disk Controller and IDE channels. When a function is disabled, the clock to the disabled function is stopped and the disabled function will not respond to any internal accesses. The PC87560 will still respond to PCI cycles accessing the disabled functions if that function is enabled for decoding (through the Function Enable Register For Decoding in the Configuration Register). The power management software can disable a function if it is idle, and can program the PC87560 to do an I/O trap on the next access to the disabled function. When the CPU tries to access the disabled function, the PC87560 asserts DEVSEL# and terminates with TRDY# while asserting a System Management Interrupt (SMI) to trap that I/O cycle. The power management software can then turn on the function and retry the access.

Bit 0: Parallel Port Enable.

0: Parallel Port is disabled.

The Parallel Port data bus pins will be placed in TRI-STATE if the PNF input is a one or if the PNF Select bit (Bit 0 of Function 1 System I/O Configuration Register at I/O, configuration offset 5Ch) is a zero. The Parallel Port output pins are driven to their inactive states if the PNF input is a one (or the PNF Select bit is a zero) and Bit 0 of the TRI-STATE Control Register is a zero. The Parallel Port output pins will be placed in TRI-STATE if the PNF input is a one (or the PNF Select bit is a zero) and Bit 0 of the TRI-STATE Control Register is a one. The Parallel Port input pins are gated within their I/O cells in a manner that reduces their leakage current. The internal clock of the Parallel Port is frozen.

1: Parallel Port is enabled.

The Parallel Port drives its output pins (assuming PNF is a one or the PNF Select bit is a zero), with its internal clock running and its configuration registers accessible via the address specified by SP2BAR. Selection of Parallel Port modes is done via the Printer Control Registers.

Bit 1: Serial Port 1 Enable.

0: Serial Port 1 is disabled.

Serial Port 1 output pins are driven to their inactive states if Bit 1 of the TRI-STATE Control Register is a zero. Serial Port 1 output pins are placed in TRI-STATE if Bit 1 of the TRI-STATE Control Register is a one. Serial Port 1 input pins are gated within their I/O cells in a manner that reduces their leakage current. The internal clock of Serial Port 1 is frozen.

1: Serial Port 1 is enabled.

Serial Port 1 drives its output pins, with its internal clock running. Serial Port 1 configuration registers can be accessed at the address specified by FDCBAR.

Bit 2: Serial Port 2 and Serial Infrared Enable.

0: Serial Port 2 and Serial Infrared is disabled.

Serial Port 2 and Serial Infrared output pins are driven to their inactive states if Bit 2 of the TRI-STATE Control Register is a zero. Serial Port 2 and Serial Infrared output pins are placed in TRI-STATE if Bit 2 of the TRI-STATE Control Register is one. Serial Port 2 and Serial Infrared input pins are gated within their I/O cells in a manner that reduces their leakage current. The internal clock of Serial Port 2 and Serial Infrared is frozen.

1: Serial Port 2 and Serial Infrared is enabled.

Serial Port 2 and Serial Infrared drives its output pins, with its internal clock running. Serial Port 2 and Serial Infrared configuration registers can be accessed at the address specified by SP1BAR.

Bit 3: Floppy Disk Controller (FDC) Enable.

0: FDC is disabled.

FDC output pins are driven to their inactive states if Bit 3 of the TRI-STATE Control Register is a zero. FDC output pins are placed in TRI-STATE if Bit 3 of the TRI-STATE Control Register is a one. FDC input pins are gated within their I/O cells in a manner that reduces their leakage current. The internal clock of the FDC is frozen.

The multiplexed Parallel Port/Floppy signals are likewise effected if the PNF input is a zero and the PNF Select bit (Bit 0 of Function 1 System I/O Configuration Register at I/O, configuration offset 5Ch) is a one.

1: FDC is enabled.

FDC drives its output pins, with its internal clock running. FDC configuration registers can be accessed at the address specified by PPBAR.

The multiplexed Parallel Port/Floppy signals are likewise effected if the PNF input is a zero and the PNF Select bit (Bit 0 of Function 1 System I/O Configuration Register at I/O, configuration offset 5Ch) is a one.

Bit 4: IDE Channel 1 Enable.

0: IDE Channel 1 is disabled.

IDE Channel 1 output pins are driven to their inactive states if Bit 4 of the TRI-STATE Control Register is a zero. IDE Channel 1 output pins are placed in TRI-STATE if Bit 4 of the TRI-STATE Control Register is a one. IDE Channel 1 input pins are gated within their I/O cells in a manner that reduces their leakage current. The internal clock associated with IDE Channel 1 is frozen.

1: IDE Channel 1 is enabled.

IDE Channel 1 drives its output pins, with its internal clock running.

Bit 5: IDE Channel 2 Enable.

0: IDE Channel 2 is disabled.

IDE Channel 2 output pins are driven to their inactive states if Bit 4 of the TRI-STATE Control Register is a zero. IDE Channel 2 output pins are placed in TRI-STATE if Bit 4 of the TRI-STATE Control Register is a one. IDE Channel 2 input pins are gated within their I/O cells in a manner that reduces their leakage current. The internal clock associated with IDE Channel 2 is frozen.

1: IDE Channel 2 is enabled.

IDE Channel 2 drives its output pins, with its internal clock running.

Bits 7-6: Reserved.

6.2.31 SERIAL PORT 2 POWER MODE REGISTER

I/O Address: PMBAR+05h
Attribute: Read/Write
Size: 8 bits
Default value: 01h

Bit 0: Serial Port 2 Power Mode.

0: Serial Port 2 is in low power mode. In this mode, Serial Port 2 can be programmed to generate an interrupt on Ring Indicator.

1: Serial Port 2 is in normal power mode (if Bit 2 of the Function Power Mode Register is one).

Bits 7-1: Reserved.

6.2.32 GLOBAL STATUS REGISTER

I/O Address: PMBAR+06h
Attribute: Read Only
Size: 8 bits
Default value: 1Ch

This read only register holds the Idle/Not Idle status of each function.

Bit 1: Floppy Disk Controller Idle Status.

Bit 1: Reserved.

Bit 2: IDE Channel 1 Idle Status.

Bit 3: Serial Port 2 Idle Status.

Bit 4: IDE Channel 2 Idle Status.

Bits 7-5: Reserved.

6.2.33 GLOBAL SYSTEM MANAGEMENT INTERRUPT (SMI) I/O TRAP ENABLE REGISTER

I/O Address: PMBAR+(0Ch-0Fh)
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

Bit 0: Reserved.

Bit 1: Trap on I/O access to Floppy Disk Controller (FDC) Device.

0: Disabled. Bit 1 of the Power Management Global Status Register will not be set to a one upon a FDC access.

1: Enabled. Upon a FDC access (when Global SMI Enable, Bit 25, is a one), set Bit 1 of the Power Management Global Status Register to a one, which will generate a SMI.

Bit 2: Reserved.

Bit 3: Trap on I/O access to Serial Port 1 Device.

0: Disabled. Bit 3 of the Power Management Global Status Register will not be set to a one upon a Serial Port 1 access.

1: Enabled. Upon a Serial Port 1 access (when Global SMI Enable, Bit 25, is a one), set Bit 3 of the Power Management Global Status Register to a one, which will generate a SMI.

Bit 4: Reserved.

Bit 5: Trap on I/O access to IDE Channel1 Device.

0: Disabled. Bit 5 of the Power Management Global Status Register will not be set to a one upon an IDE Channel 1 access.

1: Enabled. Upon an IDE Channel 1 access (when Global SMI Enable, Bit 25, is a one), set Bit 5 of the Power Management Global Status Register to a one, which will generate a SMI.

Bit 6: Reserved.

Bit 7: Trap on I/O access to Serial Port 2 Device.

0: Disabled. Bit 7 of the Power Management Global Status Register will not be set to a one upon a Serial

Port 2 access.

1: Enabled. Upon a Serial Port 2 access (when Global SMI Enable, Bit 25, is a one), set Bit 7 of the Power Management Global Status Register to a one, which will generate a SMI.

Bit 8: **Reserved.**

Bit 9: Trap on I/O access to IDE Channel 2 Device.

0: Disabled. Bit 9 of the Power Management Global Status Register will not be set to a one upon an IDE Channel 2 access.

1: Enabled. Upon an IDE Channel 2 access (when Global SMI Enable, Bit 25, is a one), set Bit 9 of the Power Management Global Status Register to a one, which will generate a SMI.

Bit 10: **Reserved.**

Bit 11: Trap on I/O access to Parallel Port Device.

0: Disabled. Bit 11 of the Power Management Global Status Register will not be set to a one upon a Parallel Port access.

1: Enabled. Upon a Parallel Port access (when Global SMI Enable, Bit 25, is a one), set Bit 11 of the Power Management Global Status Register to a one, which will generate a SMI.

Bits 16-12: **Reserved.**

Bit 17: Enable generation of SMI upon System Event being active.

0: Disabled. No SMI will be generated even if one of the System Event 1 Status Register bits is set to a one.

1: Enabled. When any of the System Event 1 Status Register bits is set to a one (when Global SMI Enable, Bit 25, is a one), a SMI will be generated. It should be noted that Bit 17 of the Power Management Global Status Register is not a physical Latch or Flip-Flop; instead it reflects the ANDing of this bit with the OR of all of the System Event 1 Status Register bits.

Bits 21-18: **Reserved.**

Bit 22: Enable generation of SMI upon receiving an serial SMI.

0: Disabled. No SMI will be generated when an active Serial SMI is received via the Serial IRQ interface.

1: Enabled. Upon receiving a Serial SMI (when Global SMI Enable, Bit 25, is a one), set Bit 22 of the Power Management Global Status Register to a one, which will generate a SMI.

Bit 23: Enable SMI upon writes to the Advanced Power Management Control Port (APMC).

0: Disabled. Bit 23 of the Power Management Global Status Register will not be set to a one upon an APMC write.

1: Enabled. Upon an APMC write (when Global SMI Enable, Bit 25, is a one), set Bit 23 of the Power Management Global Status Register to a one, which will generate a SMI.

Bit 24: Soft ware generated SMI.

0: SMI generation is not effected by this bit.

1: The PC87560's SMI_SB signal will be asserted high whenever this bit is a one.

Bit 25: Global SMI Enable

0: Disabled; none of the Power Management Global Status Register bits will be set to a one and no SMI will be generated. The one exception is the Software generated SMI (Bit 24 of this register) will generate a SMI if it is set to a one.

NOTE: This bit serves two functions when it is a zero. First, it disables the setting of any of the Power Management Global Status Register bits to ones; this does not mean that it clears any bit that is already set to a one, it just means that no Power Management Global Status Register bit may transition from a zero to a one while this bit is a zero. Secondly, when this bit is a zero, it will force the SMI_SB signal inactive low, no matter what the state of any of the Power Management Global Status Register bits are. Remember this bit does not prevent Bit 24, Software generated SMI from generating an active SMI and asserting SMI_SB active high.

1: Enabled; SMI will be generated whenever any of the Power Management Global Status Register bits is a one.

Bit 26: **Reserved.**

Bit 27: Enables generation of SMI when the USB Host Controller's SMI signal goes active.

0: Disabled. No SMI will be generate when the USB Host Controller asserts its SMI signal.

1: Enabled; generate a SMI when the USB Host Controller asserts its SMI signal. It should be noted that Bit 27 of the Power Management Global Status Register is no t a physical Latch or Flip-Flop; instead it reflects the ANDing of this bit with the USB Host Controller's SMI output signal.

Bits 31-28: Reserved.

6.2.34 POWER MANAGEMENT GLOBAL STATUS REGISTER

I/O Address: PMBAR+(14h-17h)
Attribute: Read/Write-Clear-Mask
Size: 32 bits
Default value: 00000000h

The Power Management Global Status Register is used to indicate the source of a System Management Interrupt (SMI).

Bit 0: Reserved.

Bit 1: Trap on I/O access to Floppy Disk Controller (FDC) Device.

0: Did not generate a SMI.

1: Generated a SMI. To clear this bit to a zero, a one must be written to this bit; this will also clear the SMI generated by the I/O trap.

Bit 2: Reserved.

Bit 3: Trap on I/O access to Serial Port 1 Device.

0: Did not generate a SMI.

1: Generated a SMI. To clear this bit to a zero, a one must be written to this bit; this will also clear the SMI generated by the I/O trap.

Bit 4: Reserved.

Bit 5: Trap on I/O access to IDE Channel 1 Device.

0: Did not generate a SMI.

1: Generated a SMI. To clear this bit to a zero, a one must be written to this bit; this will also clear the SMI generated by the I/O trap.

Bit 6: Reserved.

Bit 7: Trap on I/O access Serial Port 2 Device.

0: Did not generate a SMI.

1: Generated a SMI. To clear this bit to a zero, a one must be written to this bit; this will also clear the SMI generated by the I/O trap.

Bit 8: Reserved.

Bit 9: Trap on I/O access to IDE Channel 2 Device.

0: Did not generate a SMI.

1: Generated a SMI. To clear this bit to a zero, a one must be written to this bit; this will also clear the SMI generated by the I/O trap.

Bit 8: Reserved.

Bit 11: Trap on I/O access to Parallel Port Device.

0: Did not generate a SMI.

1: Generated a SMI. To clear this bit to a zero, a one must be written to this bit; this will also clear the SMI generated by the I/O trap.

Bits 16-12: Reserved.

Bit 17: System Event activity.

0: Did not generate a SMI.

1: Generated a SMI. To clear this bit to a zero, all of the bits in the System Event 1 Status Register (B1BAR4+(54h-57h)) must be cleared. Refer to the System Event 1 Status Register for information on how this may be accomplished. It should be noted that this bit is not supported by a physical Latch or Flip-Flop; instead it reflects the ANDing of this Bit 17 of the Global System Management Interrupt (SMI)

I/O Trap Enable Register with the OR of all of the System Event 1 Status Register bits.

Bits 21-18: Reserved.

Bit 22: Serial SMI.

0: Did not generate a SMI.

1: Generated a SMI. To clear this bit to a zero, the Serial Interrupt Request sequence must send an inactive Serial SMI indication to the PC87560. The manner in which this is accomplished is dependent on the external device that generated the active Serial SMI and is beyond the scope of this specification.

Bit 23: Advanced Power Management Control Port (APMC) write.

0: Did not generate a SMI.

1: Generated a SMI. To clear this bit to a zero, a one must be written to this bit; this will also clear the SMI generated by the APMC write.

Bits 26-24: Reserved.

Bit 27: USB Host Controller SMI.

0: Did not generate a SMI.

1: Generated a SMI. To clear this bit to a zero, the USB Host Controller SMI must be cleared via the USB Host Controller; refer to the USB Host Controller section for information regarding the method of clearing its SMI. It should be noted that this bit is not a physical Latch or Flip-Flop; instead it reflects the ANDing of Bit 27 of the Global System Management Interrupt (SMI) I/O Trap Enable Register with the USB Host Controller's SMI output signal.

Bits 31-28:Reserved.

6.2.35 PRIMARY ACTIVITY (PA) ENABLE REGISTER

I/O Address: PMBAR+(18h-19h)
Attribute: Read/Write
Size: 16 bits
Default value: 0000h

Bit 0: Access to Floppy Disk Controller (FDC) generates a Primary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1: Enabled.

Bit 1: Access to Serial Port 1 generates a Primary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1: Enabled.

Bit 2: Access to IDE Channel 1 generates a Primary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1: Enabled.

Bit 3: Access to Serial Port 2 generates a Primary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1: Enabled.

Bit 4: Access to IDE Channel 2 generates a Primary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1: Enabled.

Bit 5: Access to Parallel Port generates a Primary Activity notification on the PicoPower Power Management se-

rial bus (BSER).

0: Disabled.

1: Enabled.

Bits 10-6: Reserved.

Bit 11: Occurrence of System Event generates a Primary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1: Enabled.

Bits 15-12: Reserved.

6.2.36 SECONDARY ACTIVITY (SA) ENABLE REGISTER

I/O Address: PMBAR+(1Ah-1Bh)
Attribute: Read/Write
Size: 16 bits
Default value: 0000h

Bit 0: Access to Floppy Disk Controller (FDC) generates a Secondary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1: Enabled.

Bit 1: Access to Serial Port 1 generates a Secondary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1: Enabled.

Bit 2: Access to IDE Channel 1 generates a Secondary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1:Enabled.

Bit 3: Access to Serial Port 2 generates a Secondary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1: Enabled.

Bit 4: Access to IDE Channel 2 generates a Secondary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1: Enabled.

Bit 5: Access to Parallel Port generates a Secondary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1: Enabled.

Bits 10-6: Reserved.

Bit 11: Occurrence of System Event generates a Secondary Activity notification on the PicoPower Power Management serial bus (BSER).

0: Disabled.

1: Enabled.

Bits 15-12: Reserved.

6.2.37 SYSTEM EVENT 1 CONTROL REGISTER

I/O Address: PMBAR+(54h-57h)
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

The System Event 1 signal is driven on EXTEVNT1 pin when Power Management Configuration is programmed to Slave Mode via Bits 1-0 of the ACPI Function Control Register (ACPIBAR+12h). The System Event 1 signal may also be used to generate a System Management Interrupt (SMI), or Primary Activity (PA) or Secondary Activity notification on the PicoPower Power Management serial bus (BSER).

Bit 0: Global Enable for the System Event 1.

0: Disabled. No system event will set its associated System Event 1 Status Register bit to a one and an active System Event 1 signal will not be generated, regardless of the individual event enable bits.

NOTE: This bit serves two functions when it is a zero. First, it disables the setting of any of the System Event 1 Status Register bits to ones; this does not mean that it clears any bit that is already set to a one, it just means that no System Event 1 Status Register bit may transition from a zero to a one while this bit is a zero. Secondly, when this bit is a zero, it will force the internal PC87560 System Event 1 signal inactive no matter what the state of any of the System Event 1 Status Register bits are.

1: Enabled. All system events enabled by their individual event enable bit may set their associated System Event 1 Status Register bit to a one and as a result generate an active System Event 1 signal.

Bit 1: IRQ0 Enable.

0: Disabled. Bit 1 of the System Event 1 Status Register will not be set to a one if IRQ0 is active.

1: Enabled. When IRQ0 is active (and Bit 0 of this register is a one), Bit 1 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 2: IRQ1 Enable.

0: Disabled. Bit 2 of the System Event 1 Status Register will not be set to a one if IRQ1 is active.

1: Enabled. When IRQ1 is active (and Bit 0 of this register is a one), Bit 2 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 3: IRQ3 Enable.

0: Disabled. Bit 3 of the System Event 1 Status Register will not be set to a one if IRQ3 is active.

1: Enabled. When IRQ3 is active (and Bit 0 of this register is a one), Bit 3 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 4: IRQ4 Enable.

0: Disabled. Bit 4 of the System Event 1 Status Register will not be set to a one if IRQ4 is active.

1: Enabled. When IRQ4 is active (and Bit 0 of this register is a one), Bit 4 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 5: IRQ5 Enable.

0: Disabled. Bit 5 of the System Event 1 Status Register will not be set to a one if IRQ5 is active.

1: Enabled. When IRQ5 is active (and Bit 0 of this register is a one), Bit 5 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 6: IRQ6 Enable.

0: Disabled. Bit 6 of the System Event 1 Status Register will not be set to a one if IRQ6 is active.

1: Enabled. When IRQ6 is active (and Bit 0 of this register is a one), Bit 6 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 7: IRQ7 Enable.

0: Disabled. Bit 7 of the System Event 1 Status Register will not be set to a one if IRQ7 is active.

1: Enabled. When IRQ7 is active (and Bit 0 of this register is a one), Bit 7 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 8: IRQ8 Enable.

0: Disabled. Bit 8 of the System Event 1 Status Register will not be set to a one if IRQ8 is active.

1: Enabled. When IRQ8 is active (and Bit 0 of this register is a one), Bit 8 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 9: IRQ9 Enable.

0: Disabled. Bit 9 of the System Event 1 Status Register will not be set to a one if IRQ9 is active.

1: Enabled. When IRQ9 is active (and Bit 0 of this register is a one), Bit 9 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 10: IRQ10 Enable.
0: Disabled. Bit 10 of the System Event 1 Status Register will not be set to a one if IRQ10 is active.
1: Enabled. When IRQ10 is active (and Bit 0 of this register is a one), Bit 10 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 11: IRQ11 Enable.
0: Disabled. Bit 11 of the System Event 1 Status Register will not be set to a one if IRQ11 is active.
1: Enabled. When IRQ11 is active (and Bit 0 of this register is a one), Bit 11 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 12: IRQ12 Enable.
0: Disabled. Bit 12 of the System Event 1 Status Register will not be set to a one if IRQ12 is active.
1: Enabled. When IRQ12 is active (and Bit 0 of this register is a one), Bit 12 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 13: IRQ13 Enable.
0: Disabled. Bit 13 of the System Event 1 Status Register will not be set to a one if IRQ13 is active.
1: Enabled. When IRQ13 is active (and Bit 0 of this register is a one), Bit 13 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 14: IRQ14 Enable.
0: Disabled. Bit 14 of the System Event 1 Status Register will not be set to a one if IRQ14 is active.
1: Enabled. When IRQ14 is active (and Bit 0 of this register is a one), Bit 14 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 15: IRQ15 Enable.
0: Disabled. Bit 15 of the System Event 1 Status Register will not be set to a one if IRQ15 is active.
1: Enabled. When IRQ15 is active (and Bit 0 of this register is a one), Bit 15 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bit 16: **Reserved.**

Bit 17: **Reserved.**

Bit 18: NMI Enable.
0: Disabled. Bit 18 of the System Event 1 Status Register will not be set to a one if NMI is active.
1: Enabled. When NMI is active (and Bit 0 of this register is a one), Bit 18 of the System Event 1 Status Register will be set to a one, which will generate an active System Event 1 signal.

Bits 31-19: **Reserved.**

6.2.38 SYSTEM EVENT 1 STATUS REGISTER

I/O Address: PMBAR+(58h-5Bh)
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

The System Event 1 Status Register is used to indicate the source of a System Event 1 signal. Any bit that is a "1" can only be cleared by writing a one to that bit. Writing a one to a bit that generated a System Event 1 also clears the System Event 1 indication caused by the specific event.

Bit 0: **Reserved.**

Bit 1: IRQ0
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 2: IRQ1
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 3: IRQ3
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 4: IRQ4
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 5: IRQ5
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 6: IRQ6
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 7: IRQ7
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 8: IRQ8
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 9: IRQ9
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 10: IRQ10
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 11: IRQ11
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 12: IRQ12
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 13: IRQ13
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 14: IRQ14
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 15: IRQ15
0: Did not generate a System Event 1.

1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bit 16: Reserved.

Bit 17: Reserved.

Bit 18: NMI
0: Did not generate a System Event 1.
1: Generated a System Event 1. To clear this bit to a zero, a one must be written to this bit.

Bits 31-19: Reserved.

6.2.39 ZERO VOLT SUSPEND SHADOW REGISTERS

I/O Address: PMBAR+6Ch - PMBAR+AFh
Attribute: Read Only
Size: 8 bits each
Default value: xx

All the shadow registers reflect the last value written to the 8259 Programmable Interrupt Controllers, the RTC Index, the 8254 Timer, the Legacy 8237 DMA Controllers, the Serial Ports, the Parallel Port and the Video DAC.

Offset	Description
6Ch	Interrupt Controller 1 register ICW1. This register saves the value of the last write to I/O port 20h.
6Dh	Interrupt Controller 1 register ICW2. This register saves the value of the last write to I/O port 21h.
6Eh	Interrupt Controller 1 register ICW3. This register saves the value of the last write to I/O port 21h.
6Fh	Interrupt Controller 1 register ICW4. This register saves the value of the last write to I/O port 21h.
70h	Interrupt Controller 1 register OCW2. This register saves the value of the last write to I/O port 21h.
71h	Interrupt Controller 1 register OCW3. This register saves the value of the last write to I/O port 21h.
72h	Interrupt Controller 2 register ICW1. This register saves the value of the last write to I/O port A0h.
73h	Interrupt Controller 2 register ICW2. This register saves the value of the last write to I/O port A1h.
74h	Interrupt Controller 2 register ICW3. This register saves the value of the last write to I/O port A1h.
75h	Interrupt Controller 2 register ICW4. This register saves the value of the last write to I/O port A1h.
76h	Interrupt Controller 2 register OCW2. This register saves the value of the last write to I/O port A1h.
77h	Interrupt Controller 2 register OCW3. This register saves the value of the last write to I/O port A1h.
78h	RTC Index Register. This register saves the value of the last write I/O address 0070h.
79h	8254 Timer Counter 0 Count Low byte. This register saves the value of the last write to I/O address 0040h with Counter 0's Byte Pointer equal to zero.
7Ah	8254 Timer Counter 0 Count High byte. This register saves the value of the last write to I/O address 0040h with Counter 0's Byte Pointer equal to one.
7Bh	8254 Timer Counter 1 Count Low byte. This register saves the value of the last write to I/O address 0041h with Counter 1's Byte Pointer equal to zero.
7Ch	8254 Timer Counter 1 Count High byte. This register saves the value of the last write to I/O address 0041h with Counter 1's Byte Pointer equal to one.
7Dh	8254 Timer Counter 2 Count Low byte. This register saves the value of the last write to I/O address 0042h with Counter 2's Byte Pointer equal to zero.
7Eh	8254 Timer Counter 2 Count High byte. This register saves the value of the last write to I/O address 0042h with Counter 2's Byte Pointer equal to one.

Offset	Description
7Fh	8254 Timer Counter 0 Control Register. This register saves the value of last write to I/O address 0043h when Bits 7-6=00b in the data field.
80h	8254 Timer Counter 1 Control Register. This register saves the value of last write to I/O address 0043h when Bits 7-6=01b in the data field.
81h	8254 Timer Counter 2 Control Register. This register saves the value of last write to I/O address 0043h when Bits 7-6=10b in the data field.
82h	Legacy 8237 DMA channel 0 Mode registers. Bits 7-2 of this register save the value of Bits 7-2 of the last write to the Legacy 8237 DMA Controller's channel 0 Mode Register. Bits 1-0 of this register save the value of Bits 3-2 of the last write to Legacy 8237 DMA Controller's channel 0 Extended Mode Register.
83h	Legacy 8237 DMA channel 1 Mode registers. Bits 7-2 of this register save the value of Bits 7-2 of the last write to the Legacy 8237 DMA Controller's channel 1 Mode Register. Bits 1-0 of this register save the value of Bits 3-2 of the last write to Legacy 8237 DMA Controller's channel 1 Extended Mode Register.
84h	Legacy 8237 DMA channel 2 Mode registers. Bits 7-2 of this register save the value of Bits 7-2 of the last write to the Legacy 8237 DMA Controller's channel 2 Mode Register. Bits 1-0 of this register save the value of Bits 3-2 of the last write to Legacy 8237 DMA Controller's channel 2 Extended Mode Register.
85h	Legacy 8237 DMA channel 3 Mode registers. Bits 7-2 of this register save the value of Bits 7-2 of the last write to the Legacy 8237 DMA Controller's channel 3 Mode Register. Bits 1-0 of this register save the value of Bits 3-2 of the last write to Legacy 8237 DMA Controller's channel 3 Extended Mode Register.
86h	Legacy 8237 DMA channel 4 Mode registers. Bits 7-2 of this register save the value of Bits 7-2 of the last write to the Legacy 8237 DMA Controller's channel 4 Mode Register. Bits 1-0 of this register save the value of Bits 3-2 of the last write to Legacy 8237 DMA Controller's channel 4 Extended Mode Register.
87h	Legacy 8237 DMA channel 5 Mode registers. Bits 7-2 of this register save the value of Bits 7-2 of the last write to the Legacy 8237 DMA Controller's channel 5 Mode Register. Bits 1-0 of this register save the value of Bits 3-2 of the last write to Legacy 8237 DMA Controller's channel 5 Extended Mode Register.
88h	Legacy 8237 DMA channel 6 Mode registers. Bits 7-2 of this register save the value of Bits 7-2 of the last write to the Legacy 8237 DMA Controller's channel 6 Mode Register. Bits 1-0 of this register save the value of Bits 3-2 of the last write to Legacy 8237 DMA Controller's channel 6 Extended Mode Register.
89h	Legacy 8237 DMA channel 7 Mode registers. Bits 7-2 of this register save the value of Bits 7-2 of the last write to the Legacy 8237 DMA Controller's channel 7 Mode Register. Bits 1-0 of this register save the value of Bits 3-2 of the last write to Legacy 8237 DMA Controller's channel 7 Extended Mode Register.
8Ah	Serial Port 1's FCR (only Bits 7-6, 0 are relevant, Bits 2-1 are always'0')
8Bh	Parallel Port Extended mode control register (only direction bit, Bit 5, is relevant)
8Ch	Legacy 8237 DMA (Channels 3-0) Command Register. Last write to I/O port 08h
8Dh	Legacy 8237 DMA (Channels 7-4) Command Register. Last write to I/O port D0h

Offset	Description
8Eh	Legacy 8237 DMA Controller (Channels 3-0) Mask bits and Byte Pointer Register **Bit 0:** Legacy 8237 DMA channel 0 Mask bit. There are four ways this bit may be modified, whatever occurs last will be reflected by this bit. 1) Bit 2 of the last write to I/O address 000Ah with Bits 1-0=00b. 2) A one when a write to I/O address 000Dh occurs. 3) A zero when a write to I/O address 000Eh occurs. 4) Bit 0 of the last write to I/O address 000Fh. **Bit 1:** Legacy 8237 DMA channel 1 Mask bit. There are four ways this bit may be modified, whatever occurs last will be reflected by this bit. 1) Bit 2 of the last write to I/O address 000Ah with Bits 1-0=01b. 2) A one when a write to I/O address 000Dh occurs. 3) A zero when a write to I/O address 000Eh occurs. 4) Bit 1 of the last write to I/O address 000Fh. **Bit 2:** Legacy 8237 DMA channel 2 Mask bit. There are four ways this bit may be modified, whatever occurs last will be reflected by this bit. 1) Bit 2 of the last write to I/O address 000Ah with Bits 1-0=10b. 2) A one when a write to I/O address 000Dh occurs. 3) A zero when a write to I/O address 000Eh occurs. 4) Bit 2 of the last write to I/O address 000Fh. **Bit 3:** Legacy 8237 DMA channel 3 Mask bit. There are four ways this bit may be modified, whatever occurs last will be reflected by this bit. 1) Bit 2 of the last write to I/O address 000Ah with Bits 1-0=11b. 2) A one when a write to I/O address 000Dh occurs. 3) A zero when a write to I/O address 000Eh occurs. 4) Bit 3 of the last write to I/O address 000Fh. **Bit 4:** The present value of the Legacy 8237 DMA Controller Byte Pointer for Channels 3-0. **Bits 7-5: Reserved.**

Offset	Description
8Fh	Legacy 8237 DMA Controller (Channels 7-4) Mask bits and Byte Pointer Register **Bit 0:** Legacy 8237 DMA channel 4 Mask bit. There are four ways this bit may be modified, whatever occurs last will be reflected by this bit. 1) Bit 2 of the last write to I/O address 00D4h with Bits 1-0=00b. 2) A one when a write to I/O address 00DAh occurs. 3) A zero when a write to I/O address 00DCh occurs. 4) Bit 0 of the last write to I/O address 00DEh. **Bit 1:** Legacy 8237 DMA channel 5 Mask bit. There are four ways this bit may be modified, whatever occurs last will be reflected by this bit. 1) Bit 2 of the last write to I/O address 00D4h with Bits 1-0=01b. 2) A one when a write to I/O address 00DAh occurs. 3) A zero when a write to I/O address 00DCh occurs. 4) Bit 1 of the last write to I/O address 00DEh. **Bit 2:** Legacy 8237 DMA channel 6 Mask bit. There are four ways this bit may be modified, whatever occurs last will be reflected by this bit. 1) Bit 2 of the last write to I/O address 00D4h with Bits 1-0=10b. 2) A one when a write to I/O address 00DAh occurs. 3) A zero when a write to I/O address 00DCh occurs. 4) Bit 2 of the last write to I/O address 00DEh. **Bit 3:** Legacy 8237 DMA channel 7 Mask bit. There are four ways this bit may be modified, whatever occurs last will be reflected by this bit. 1) Bit 2 of the last write to I/O address 00D4h with Bits 1-0=11b. 2) A one when a write to I/O address 00DAh occurs. 3) A zero when a write to I/O address 00DCh occurs. 4) Bit 3 of the last write to I/O address 00DEh. **Bit 4:** The present value of the Legacy 8237 DMA Controller Byte Pointer for Channels 7-4. **Bit 7-5: Reserved.**
90h	Legacy 8237 DMA channel 0 Base Address Low Byte. Last write to I/O address 0000h with the Byte Pointer equal to zero.
91h	Legacy 8237 DMA channel 0 Base Address High Byte. Last write to I/O address 0000h with the Byte Pointer equal to one.
92h	Legacy 8237 DMA channel 0 Base Count Low Byte. Last write to I/O address 0001h with the Byte Pointer equal to zero.
93h	Legacy 8237 DMA channel 0 Base Count High Byte. Last write to I/O address 0001h with the Byte Pointer equal to one.
94h	Legacy 8237 DMA channel 1 Base Address Low Byte. Last write to I/O address 0002h with the Byte Pointer equal to zero.
95h	Legacy 8237 DMA channel 1 Base Address High Byte. Last write to I/O address 0002h with the Byte Pointer equal to one.
96h	Legacy 8237 DMA channel 1 Base Count Low Byte. Last write to I/O address 0003h with the Byte Pointer equal to zero.
97h	Legacy 8237 DMA channel 1 Base Count High Byte. Last write to I/O address 0003h with the Byte Pointer equal to one.
98h	Legacy 8237 DMA channel 2 Base Address Low Byte. Last write to I/O address 0004h with the Byte Pointer equal to zero.
99h	Legacy 8237 DMA channel 2 Base Address High Byte. Last write to I/O address 0004h with the Byte Pointer equal to one.
9Ah	Legacy 8237 DMA channel 2 Base Count Low Byte. Last write to I/O address 0005h with the Byte Pointer equal to zero.
9Bh	Legacy 8237 DMA channel 2 Base Count High Byte. Last write to I/O address 0005h with the Byte Pointer equal to one.
9Ch	Legacy 8237 DMA channel 3 Base Address Low Byte. Last write to I/O address 0006h with the Byte Pointer equal to zero.

Offset	Description
9Dh	Legacy 8237 DMA channel 3 Base Address High Byte. Last write to I/O address 0006h with the Byte Pointer equal to one.
9Eh	Legacy 8237 DMA channel 3 Base Count Low Byte. Last write to I/O address 0007h with the Byte Pointer equal to zero.
9Fh	Legacy 8237 DMA channel 3 Base Count High Byte. Last write to I/O address 0007h with the Byte Pointer equal to one.
A0h	Legacy 8237 DMA channel 5 Base Address Low Byte. Last write to I/O address 00C4h with the Byte Pointer equal to zero.
A1h	Legacy 8237 DMA channel 5 Base Address High Byte. Last write to I/O address 00C4h with the Byte Pointer equal to one.
A2h	Legacy 8237 DMA channel 5 Base Count Low Byte. Last write to I/O address 00C6h with the Byte Pointer equal to zero.
A3h	Legacy 8237 DMA channel 5 Base Count High Byte. Last write to I/O address 00C6h with the Byte Pointer equal to one.
A4h	Legacy 8237 DMA channel 6 Base Address Low Byte. Last write to I/O address 00C8h with the Byte Pointer equal to zero.
A5h	Legacy 8237 DMA channel 6 Base Address High Byte. Last write to I/O address 00C8h with the Byte Pointer equal to one.
A6h	Legacy 8237 DMA channel 6 Base Count Low Byte. Last write to I/O address 00CAh with the Byte Pointer equal to zero.
A7h	Legacy 8237 DMA channel 6 Base Count High Byte. Last write to I/O address 00CAh with the Byte Pointer equal to one.
A8h	Legacy 8237 DMA channel 7 Base Address Low Byte. Last write to I/O address 00CCh with the Byte Pointer equal to zero.
A9h	Legacy 8237 DMA channel 7 Base Address High Byte. Last write to I/O address 00CCh with the Byte Pointer equal to one.
AAh	Legacy 8237 DMA channel 7 Base Count Low Byte. Last write to I/O address 00CEh with the Byte Pointer equal to zero.
ABh	Legacy 8237 DMA channel 7 Base Count High Byte. Last write to I/O address 00CEh with the Byte Pointer equal to one.
ACh	8254 Timer Counter Byte Pointers. **Bit 0:** Counter 0 present read byte pointer. **Bit 1:** Counter 0 present write byte pointer. **Bit 2:** Counter 1 present read byte pointer. **Bit 3:** Counter 1 present write byte pointer. **Bit 4:** Counter 2 present read byte pointer. **Bit 5:** Counter 2 present write byte pointer. **Bit 7-6: Reserved.**
ADh	FDC Data Select Rate Register. Last I/O write to FDCBAR offset 04h.

Offset	Description
AEh	Video DAC Mode Status Register **Bit 0:** This register watches for writes to both 3C7h and 3C8h, and remembers which one happened most recently. 0: 3C7h write has been observed. (Default value.) 1: 3C8h write has been observed. **Bit 2-1:** These bits tell if the DAC is in red, green or blue read/write mode. When reading the color registers, a 3C7h write is performed, then 3 reads from 3C9h (the DAC presents red, then green, then blue in response to these reads). For writing the color registers, a 3C8h write is performed, then 3 writes to 3C9h (the DAC accepts red, then green, then blue during these 3 writes). 01b: 03C7h write or 03C8h write has been observed 10b: 03C9h write or read (for red) has been observed 11b: 03C9h write or read (for green) has been observed 00b: 03C9h write or read (for blue) has been observed. This is the end of the sequence and the default value. **Bit 3:** Write data to 3C0h is index or data? A 3C0h write selects an address. Then, a 3C1h read will return the content of the selected address, or a second 3C0h write will write the selected address. This bit watches for 3C0h writes and 3C1h reads and tracks the sequence mentioned above. 0: Second 03C0h write of data or 03C1h read of data has been detected. (Default value.) 1: First 03C0h write of address has been detected. **Bits 7-4: Reserved.**
AFh	Video DAC 3C7/3C8 Data Register. This register holds the data byte of the last write to 3C7h or 3C8h.

6.2.40 RESET CONTROL REGISTER

I/O Address: CF9h
Attribute: Read/Write
Size: 8 bits
Default value: 00h

This register is Reserved.

Writing 00h to this register will have no effect, but writing other values could have undesirable side-effects.

6.2.41 FAST INFRARED (FIR) SCATTER/GATHER DMA CONTROLLER REGISTERS

The following is a table listing all of the Fast Infrared (FIR) Scatter/Gather DMA Controller registers. The FIR Scatter/Gather DMA Controller Base Address is determined by the Function 1 Fast Infrared (FIR) Scatter/Gather DMA Controller Base Address Register (FIRBAR) located in the PCI Function 1 Configuration space at 50h-53h. There are 64 FIR Scatter/Gather DMA Controller registers within the PC87560.

Any register listed as **Reserved** must always be read as all zeros. Also any bit within a register documented as **Reserved** must also be read as zero, unless specifically stated otherwise.

Offset from FIRBAR	Register Name
00h-03h	Transmit Command/Status Register (TCSR)
04h	Transmit Descriptor Count Register (TDSCNT)
05h-07h	**Reserved.**
08h-0Bh	Transmit Descriptor Address Register (TDS_ADR)
0Ch-0Fh	Transmit Data Buffer Address Register (TD_ADR)
10h-13h	**Reserved.**
14h-15h	Transmit Data Buffer Length Register (TDB_LEN)
16h	**Reserved.**
17h	Transmit Status/Command Field Register (TSCFR)
18h-19h	**Reserved.**
1Ah-1Bh	Transmit Timer Register (TTMR)
1Ch-1Fh	**Reserved.**
20h-23h	Receive Command/Status Register (RCSR)
24h	Receive Descriptor Count Register (RDSCNT)
25h-27h	**Reserved.**
28h-2Bh	Receive Descriptor Address Register (RDS_ADR)
2Ch-2Fh	Receive Data Buffer Address Register (RDB_ADR)
30h-31h	Receive Data Buffer Size Register (RDB_SIZ)
32h-33h	**Reserved.**

34h-35h	Receive Data Buffer Length Register (RDB_LEN)
34h-35h	**Reserved.**
37h	Receive Command/Status Field Register (RSCFR)
38h-39h	**Reserved.**
3Ah-3Bh	Receive Timer Register (RTMR)
3Ch-3Fh	**Reserved.**

6.2.42 TRANSMIT COMMAND/STATUS REGISTER (TCSR)

I/O Address: FIRBAR + (00h - 03h)
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

Bit 0: TxCHEN. Transmit Channel Enable. When this bit is set by software, the transmit channel is enabled to perform a transfer operation. When cleared, the channel is disabled.

0: Transmit channel is disabled

1: Transmit channel is enabled

Bits 3-1: **Reserved.** Always 0.

Bit 4: DIR. Direction bit always 1 (transmit).

Bit 5: TxTMRE. Transmit Timer Enable

Bit 6: TxINTE. Transmit interrupt enable.

0: Transmit interrupts are disabled

1: Transmit interrupts are enabled. When this bit is set, the OR of all the interrupt sources from the transmit DMA block are unmasked and passed to the UIR.

Bit 7: **Reserved.**

Bit 8: TxPREQ. Transmit Pause Request. This bit is used to pause the Tx DMA transfer. When this bit is set by software, the DMA transfer will pause after the current frame completes.

0: No Pause Request. If previously paused, clearing this bit will resume the DMA transfer

1: Pause DMA transfer. All state information is kept.

Bits 15-9: **Reserved.**

Bit 16: TxHLT. Transmit Halt. This bit is set by the DMA controller when the DMA transfer is halted. It is cleared by writing a 1 into it. This bit must be cleared before the Tx channel can perform any transfer operation. The Tx channel halts at the end of DMA operation (EODMA set to 1), or when a PCI bus transfer error occurs.

0: DMA transfer not halted.

1: DMA transfer halted.

Bit 17: Active. This bit is set by the DMA controller when the TxCHEN bit is set and a DMA transfer is in progress (a byte is transferred to the UIR). This bit is cleared by the DMA controller when the EODMA flag is set.

0: DMA not active.

1: DMA active. Transmit DMA transfer is in progress.

Bit 18: TxPACK. Transmit Pause Acknowledge. This bit will be set by the DMA controller when the DMA transfer is paused (due to the pause request) after the current frame has completed.

0: Not paused

1: Paused

Bit 19: WMINT. Transmit Water Mark Interrupt flag. This bit will be set if an Interrupt command (INT) is executed. This bit is cleared when a 1 is written to it.

0: No Tx interrupt asserted

1: Tx Interrupt asserted

Bit 20: TOUT. Transmitter timeout interrupt flag. This bit is set to 1 when the timer is enabled and no data byte has been transferred to the serial controller for the amount of time specified by the Transmit Timer Register value. This bit is cleared by writing a 1 into this bit.

Bit 21: EODMA. End of DMA interrupt flag. This bit will be set when the last descriptor is completed (Transmit Buffer Length count goes to 0 and TDSCNT register =0). This bit is cleared by writing a 1 into this bit.

Bit 22: **Reserved.**

Bit 23: DSC_ER. Descriptor error interrupt flag. Set to 1 when an error in the command/status byte of the memory descriptor to be executed is detected. Cleared by writing a 1 into this bit.

Bit 24: **Reserved.**

Bit 25: TABT. PCI target abort interrupt flag. Cleared by writing a 1 into this bit.

Bit 26: MABT. PCI master abort interrupt flag. Cleared by writing a 1 into this bit.

Bits 31-27: Reserved.

6.2.43 TRANSMIT DESCRIPTOR COUNT REGISTER (TDSCNT)

I/O Address: FIRBAR + 04h
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bits 7-0: Transmit Descriptor Count. This register indicates the number of descriptors in the transmit channel. When the FIR DMA operation completes (EODMA flag is set), this register's content is 0.

6.2.44 TRANSMIT DESCRIPTOR ADDRESS REGISTER (TDS_ADR)

I/O Address: FIRBAR + (08h-0Bh)
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

Bits 31-0: Transmit Descriptor Address. This register holds the base address of the transmit descriptor table.

6.2.45 TRANSMIT DATA BUFFER ADDRESS REGISTER (TD_ADR)

I/O Address: FIRBAR + (0Ch-0Fh)
Attribute: Read only
Size: 32 bits
Default value: 00000000h

This register is written by the DMA controller.

Bits 31-0: Transmit Data Buffer Address. This register is loaded from the Transmit Data Buffer Pointer field of the memory descriptor being processed when the descriptor is retrieved by the channel.

6.2.46 TRANSMIT DATA BUFFER LENGTH REGISTER (TDB_LEN)

I/O Address: FIRBAR + (14h-15h)
Attribute: Read only
Size: 16 bits
Default value: 0000h

This register is written by the DMA controller.

Bits 15-0: Transmit Data Buffer Length. Contains the number of bytes in the data buffer associated with the descriptor currently being processed. The contents of this register is the current DMA byte count, which is decrement value of the Transmit Buffer Length field of the memory descriptor being processed when the descriptor is retrieved from memory by the channel.

6.2.47 TRANSMIT STATUS/COMMAND FIELD REGISTER (TSCFR)

I/O Address: FIRBAR + (17h)
Attribute: Read only
Size: 8 bits
Default value: 00h

This register holds the command/status field that is written out to memory after a transmit descriptor is processed. This register is written by the DMA controller.

Bit 0: INT. When this bit is set, an interrupt will be generated upon execution of this descriptor and the TxINT bit will be set in the FIR DMA Transmit Status register.

Bit 1: IR_PULSE. When set to 1, an infrared pulse is transmitted at the end of the frame. This bit will be cleared when the packet has been transmitted.

Bit 2: IR_UNDERR. This bit is set when a transmit underrun occurred. Theoretically this should not happen and would indicate a hardware problem.

Bits 5-3: Reserved.

Bit 6: END of FRAME. When this bit is a 0, it indicates that this is not the last descriptor for this current packet. If this bit is a 1, it indicates that this is the end of the packet. When the packet is complete, an End Of Frame will be sent out to the FIR and an interrupt will be generated and the TxINT bit will be set in the FIR DMA Transmit Status register.

Bit 7: DONE. When the processing of this descriptor has completed, this bit is set by the hardware.

6.2.48 TRANSMIT TIMER REGISTER (TTMR)

I/O Address FIRBAR + (1Ah-1Bh)
Attribute: Read/Write
Size: 16 bits
Default value: 0000h

Bits 15-0: Transmit Timer. The transmit timer, when enabled, generates an interrupt when it counts down to 0. It can be used to notify the software when an idle interval is detected in the transmit channel. It is reloaded whenever a data byte is transmitted. When the CPU writes into this register, the new value is loaded into the timer immediately. Reading this register when the TxTMRE bit is 0, returns the value written into it. Reading it when TxTMRE is 1, returns the current value.

6.2.49 RECEIVE COMMAND/STATUS REGISTER (RCSR)

I/O Address: FIRBAR + (20h - 23h)
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

Bit 0: RxCHEN. Receive Channel Enable. When this bit is set by software, the receive channel is enabled to perform a transfer operation. When cleared, the channel is disabled.

0: Receive channel is disabled

1: Receive channel is enabled

Bits 3-1: **Reserved.** Always 0.

Bit 4: DIR. Direction bit always 0 (receive).

Bit 5: RxTMRE. Receive Timer Enable. This timer is used to specify how long the DMA controller should wait for data from the FIR. When this timer expires, an interrupt is asserted (if enabled).

0: disable

1: enable

Bit 6: RxINTE. Receive Interrupt enable.

0: Receive interrupts are disabled

1: Receive interrupts are enabled. When this bit is set, the OR of all the interrupt sources from the receive DMA block are unmasked and passed to the UIR.

Bit 7: **Reserved.**

Bit 8: RxPREQ. Receive Pause Request. This bit is used to pause the Rx DMA transfer. When this bit is set by software, the DMA transfer will pause after the current frame completes.

0: No Pause Request. If previously paused, clearing this bit will resume the DMA transfer

1: Pause DMA transfer. All state information is kept.

Bit 9: CLSDS. Close descriptor. Setting this bit to a 1 will close the current descriptor (set DONE and write the status and the contents of the receive FIFO out to memory) if the internal timer flag is set.

Bits 15-10: **Reserved.**

Bit 16: RxHLT. Receive Halt. This bit is set by the DMA controller when the DMA transfer is halted. It is cleared by writing a 1 into it. This bit must be cleared before the Rx channel can perform any transfer operation. The Rx channel halts when the RDSCNT register is 0, or when a PCI bus transfer error occurs.

0: DMA transfer not halted.

1: DMA transfer halted.

Bit 17: Active. This bit is set by the DMA controller when the RxEN bit is set and a DMA transfer is in progress. This bit is cleared by the DMA controller when the last transfer (packet or packet fragment) is complete (The FR_END bit is 1).

0: DMA not active.

1: DMA active. Receive DMA transfer is in progress.

Bit 18: RxPACK. Receive Pause Acknowledge. This bit will be set by the DMA controller when the DMA transfer is paused (due to the pause request) after the current frame has completed.

0: Not paused

1: Paused

Bit 19: WMINT. Receive Water Mark Interrupt flag. This bit will be set if an Interrupt command (INT) is executed. This bit is cleared when a 1 is written to it.

0: No Rx interrupt asserted

1: Rx Interrupt asserted

Bit 20: RTOUT. Receive timeout interrupt flag. This bit is set to 1 when the Receive Timer is enabled and no data byte has been received from the serial controller for the amount of time specified by the Receive Timer Register value. This bit is cleared by writing a 1 into this bit.

Bit 21: EODMA. End Of DMA interrupt flag. This bit will be set either an End of Frame is encountered or when the RDSCNT is 0. This bit is cleared by writing a 1 into this bit.

Bit 22: **Reserved.**

Bit 23: DSC_ER. Descriptor error interrupt flag. Set to 1 when an error in the command/status byte of the memory descriptor to be executed is detected. Cleared by writing a 1 into this bit.

Bit 24: **Reserved.**

Bit 25: TABT. PCI target abort interrupt flag. Cleared by writing a 1 into this bit.

Bit 26: MABT. PCI master abort interrupt flag. Cleared by writing a 1 into this bit.

Bits 31-27: **Reserved.**

6.2.50 RECEIVE DESCRIPTOR COUNT REGISTER (RDSCNT)

I/O Address: FIRBAR + 24h
Attribute: Read/Write
Size: 8 bits
Default value: 00h

Bits 7-0: Receive Descriptor. This register indicates the number of descriptors to be processed by the receive channel. After a DMA operation completes (EODMA flag is set), this register's contents is 0.

6.2.51 RECEIVE DESCRIPTOR ADDRESS REGISTER (RDS_ADR)

I/O Address: FIRBAR + (28h-2Bh)
Attribute: Read/Write
Size: 32 bits
Default value: 00000000h

Bits 31-0: Receive Descriptor Address. This register holds the base address of the receive descriptor table.

6.2.52 RECEIVE DATA BUFFER ADDRESS REGISTER (RDB_ADR)

I/O Address: FIRBAR + (2Ch-2Fh)
Attribute: Read only
Size: 32 bits
Default value: 00000000h

This register is written by the DMA controller.

Bits 31-0: Receive Data Buffer Address. This register is loaded from the Receive Data Buffer Pointer field of the memory descriptor being processed when the descriptor is retrieved by the channel.

6.2.53 RECEIVE DATA BUFFER SIZE REGISTER (RDB_SIZ)

I/O Address FIRBAR + (30h-31h)
Attribute: Read only
Size: 16 bits
Default value: 0000h

This register is written by the DMA controller.

Bits 15-0: Receive Data Current Byte Count. This is the 16 bit value of the current DMA receive byte count.

6.2.54 RECEIVE DATA BUFFER LENGTH REGISTER (RDB_LEN)

I/O Address: FIRBAR + (34h-35h)
Attribute: Read only
Size: 16 bits
Default value: 0000h

This register is written by the DMA controller.

Bits 15-0: Receive Data Buffer Length. Contains the number of bytes in the data buffer associated with the descriptor currently being processed. This register is loaded from the Receive Buffer Length field of the memory descriptor being processed when the descriptor is retrieved from memory by the channel.

6.2.55 RECEIVE COMMAND/STATUS FIELD REGISTER (RSCFR)

I/O Address: FIRBAR + (37h)
Attribute: Read only
Size: 8 bits
Default value: 00h

This register holds the command/status field that is written out to memory after a receive descriptor is processed. This register is written by the DMA controller.

Bit 0: INT. When this bit is set, an interrupt will be generated upon execution of this descriptor and the RxINT bit will be set in the FIR DMA Receive Status register.

Bit 1: OVR. This bit is set on an overrun.

Bit 2: BAD_CRC. A 1 means a CRC error occurred.

Bit 3: PHY_ERR. This bit is set to 1 when an encoding error is detected.

Bit 4: MAX_LNGT. This bit is set to 1 when a packet exceeding the maximum length has been received.

Bit 5: **Reserved.**

Bit 6: FR_END. This bit is set to indicate that the reception of the frame has been completed. The EODMA bit will be set in the FIR DMA Receive Status register.

Bit 7: DONE When the processing of this descriptor has completed, this bit is set by the hardware.

6.2.56 RECEIVE TIMER REGISTER (RTMR)

I/O Address FIRBAR + (3Ah-3Bh)
Attribute: Read/Write
Size: 16 bits
Default value: 0000h

Bits 15-0: Receive Timer Register. The receive timer, when enabled, generates an interrupt when it counts down to 0. It can be used to notify the software when an idle interval is detected in the receive channel. It is reloaded whenever a data byte is received. When the CPU writes into this register, the new value is loaded into the timer immediately. Reading this register when the RxTMRE bit is 0, returns the value written into it. Reading it when RxTMRE is 1, returns the current value.