INTEGRATED CIRCUITS

DATA HANDBOOK

RF Communications

Signetics

Philips Semiconductors

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Product Status

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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RF Communications Handbook Alphanumeric product list

RF Communications

Alphanumeric product list

Ordering Information

LINEAR PRODUCTS PART NUMBERING SYSTEM

Example: NE XXXX N

Package Description:
- A = Plastic Leaded Chip Carriers (PLCC)
- D = Plastic SO
- F = Ceramic Dual In-Line
- G = Hermetic Chip Carriers – Leadless
- H = Headers
- N = Plastic Dual In-Line
- P = Pin Grid Array – Hermetic
- W = Hermetic Cerpac
- Y = Ceramic Square Quad Flat Pack

Device Number

Device Family and Temperature Range Prefix
- AU = -40°C to +125°C
- NE = 0 to +70°C
- SE = -55°C to +125°C
- SA = -40°C to +80°C

PHILIPS PRODUCTS PART NUMBERING SYSTEM PREFIXES HE, PC, PN, SA, TD, TE, TS, UM

Example: TD A XXXX P N

Device Family
- HEx = CMOS Circuit
- PCx = CMOS Circuit
- PNx = NMOS Circuit
- SAx = Digital Circuit
- TDx = Linear Circuit
- TEx = Linear Circuit
- TSx = Analog Circuit
- UMx = Digital Circuit

Package Description:
- N = Plastic Dual In-Line
- D = Plastic SO
- F = Ceramic Dual In-Line
- U = Plastic Single In-Line

Package Marking on Part:
- P = Plastic Dual In-Line
- T = Plastic SO
- D = Hermetic Cerdip

Device Number

Operating Temperatures:
- A = Temperature range not specified (see data sheet)
- B = 0 to +70°C
- C = -55°C to +125°C
- D = -25°C to +70°C
- E = -25°C to +85°C
- F = -40°C to +85°C

Section 1
Amplifiers

RF Communications

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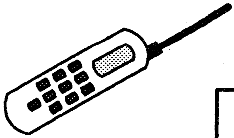


RF AMPLIFIER FAMILY OVERVIEW

	NE5200	NE5204	NE5205	NE5209	NE5219
V_{CC}	4 – 9V	5 – 8V	5 – 8V	4.5 – 7.0V	4.5 – 7.0V
I_{CC}	8mA / 95 µA	24mA	24mA	43mA	43mA
Bandwidth (3dB)	1.2GHz	550MHz	550MHz	850MHz	700MHz
Noise Figure	3.6dB	6.0dB 50 Ω 4.8dB 75 Ω	6.0dB 50 Ω 4.8dB 75 Ω	9.3dB	9.3dB
1dB Compression (output)	–6dBm	+4dBm	+4dBm	–3dBm	–3dBm
3rd Order Intercept (output)	+4dBm	+17dBm	+17dBm	+13dBm	+13dBm
Input Impedance	50 Ω	50 Ω	50 Ω	1.2kΩ	1.2k Ω
Output Impedance	50 Ω	50 Ω	50 Ω	60 Ω	60 Ω
Gain (per amplifier)	7.5dB/–13dB	19dB	19dB	25dB*	25dB*
Package	SO8	DIP8 SO8	DIP8 SO8	DIP16 SO16	DIP16 SO16
Features	+Dual Gain Stage +Enable Pin +Good Noise Figure +Low current consumption	+Low-cost amp +Simple Implementation	+Low-cost amp +Simple Implementation	+Variable gain and attenuation +Excellent Linearity	+Variable gain and attenuation +Excellent Linearity

*Single in / Differential out

RF dual gain-stage

NE/SA5200

DESCRIPTION

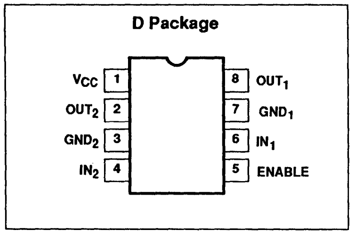
The NE/SA5200 is a dual amplifier with DC to 1200MHz response. Low noise (NF = 3.6dB) makes this part ideal for RF front-ends, and a simple power-down mode saves current for battery operated equipment. Inputs and outputs are matched to 50Ω.

The enable pin allows the designer the ability to turn the amplifiers on or off, allowing the part to act as an amplifier as well as an attenuator. This is very useful for front-end buffering in receiver applications.

FEATURES

- Dual amplifiers
- DC - 1200MHz operation
- Low DC power consumption (4.2mA per amplifier @ V_{CC} = 5V)
- Power-Down Mode (I_{CC} = 95μA typical)
- 3.6dB noise figure at 900MHz
- Unconditionally stable
- Fully ESD protected
- Low cost
- Supply voltage 4-9V
- Gain S_{21} = 7dB at f = 1GHz
- Input and output match S_{11}, S_{22} typically <–14dB

PIN CONFIGURATION



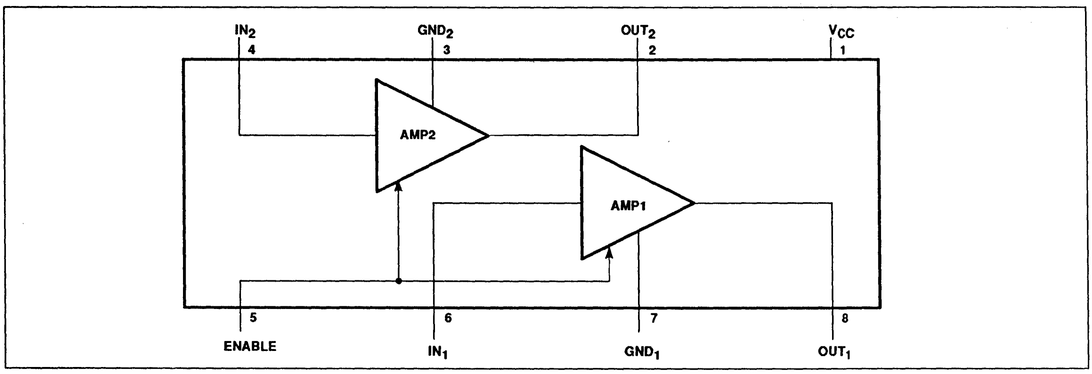
APPLICATIONS

- Cellular radios
- RF IF strips
- Portable equipment

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO (Surface–mount)	0-70°C	NE5200D
8-Pin Plastic SO (Surface–mount)	–40-+85°C	SA5200D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.5 to +9	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 8-Pin Plastic SO	780	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 10.5V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin SO: θ_{JA} = 158°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.0 to 9.0	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS V_{CC} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4	5.0	9.0	V
I_{CC}	Total supply current	V_{CC} = 5V, ENABLE = High	6.4	8.4	10.4	mA
		V_{CC} = 5V, ENABLE = Low		95	255	μA
		V_{CC} = 9V, ENABLE = High		17.8	22.2	mA
		V_{CC} = 9V, ENABLE = Low		320	960	μA
V_T	TTL/CMOS logic threshold voltage[1]			1.25		V
V_{IH}	Logic 1 level	Power-up mode	2.0		V_{CC}	V
V_{IL}	Logic 0 level	Power-down mode	-0.3		0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1	0	1	μA
I_{IH}	Enable input current	Enable = 2.4V	-1	0	1	μA
$V_{IDC,ODC}$	Input and output DC levels		0.6	0.83	1.0	V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the NE/SA5200.

AC ELECTRICAL CHARACTERISTICS[1] V_{CC} = +5V, T_A = 25°C, either amplifier, enable = 5V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S21	Insertion gain	f = 100MHz	9.2	11	13.2	dB
		f = 900MHz	5.2	7.5		dB
S22	Output return loss	f = 900MHz		–14.3		dB
S12	Reverse isolation	f = 900MHz		–17.9		dB
S11	Input return loss	f = 900MHz		–16.5		dB
P-1	Output 1dB compression point	f = 900MHz		–4.3		dBm
NF	Noise figure in 50Ω	f = 900MHz		3.6		dB
IP_2	Input second-order intercept point	f = 900MHz		+4.3		dBm
IP_3	Input third-order intercept point	f = 900MHz		–1.8		dBm
ISOL	Amplifier-to-amplifier isolation[2]	f = 900MHz		–25		dB
P_{OUT}	Saturated output power	f = 900MHz		–1.7		dBm
S21	Insertion gain when disabled	f = 100MHz		–13		dB
		f = 900MHz		–13.5		dB

NOTE:
1. All measurements include the effects of the NE/SA5200 Evaluation Board (see Figure 2). Measurement system impedance is 50Ω.
2. Input applied to one amplifier, output taken at the other output. All ports terminated into 50Ω.

APPLICATIONS

NE/SA5200 is a user-friendly, wide-band, unconditionally stable, low power dual gain amplifier circuit. There are several advantages to using the NE/SA5200 as a high frequency gain block instead of a discrete implementation. First is the simplicity of use. The NE/SA5200 does not need any external biasing components. Due to the higher level of integration and small footprint (SO8) package it occupies less space on the printed circuit board and reduces the manufacturing cost of the system. Also the higher level of integration improves the reliability of the amplifier over a discrete implementation with several components. The power down mode in the NE/SA5200 helps reduce power consumption in applications where the amplifiers can be disabled. And last but not the least is the impedance matching at inputs and outputs. Only those who have toiled through discrete transistor implementations for 50Ω input and output impedance matching can truly appreciate the elegance and simplicity of the NE/SA5200 input and output impedance matching to 50Ω.

A simplified equivalent schematic is shown in Figure 1. Each amplifier is composed of an NPN transistor with an Ft of 13GHz in a classical series-shunt feedback configuration. The two wideband amplifiers are biased from the same bias generator. In normal operation each amplifier consumes about 4mA of quiescent current (at V_{CC} = 5V). In the disable mode the device consumes about 90μA of current, most of it is in the TTL enable buffer and the bias generator. The input impedance of the amplifiers is 50Ω. The amplifiers have typical gain of 11dB at 100MHz and 7dB of gain at 1.2GHz.

It can be seen from Figure 1 that any inductance between Pin 7, 3 and the ground plane will reduce the gain of the amplifiers at higher frequencies. Thus proper grounding of Pins 7 and 3 is essential for maximum gain and increased frequency response. Figure 2 shows the printed circuit board layout and the component placement for the NE/SA5200 evaluation board. The AC coupling capacitors should be selected such that at they are shorts at the desired frequency of operation. Since most low-cost large value surface mount capacitors cease to be simply capacitors in the UHF range and exhibit an inductive behavior, it is recommended that high frequency chip capacitors be utilized in the circuit. A good power supply bypass is also essential for the performance of the amplifier and should be as close to the device as practical.

Figure 3 shows the typical frequency response of the two channels of NE/SA5200. The low frequency gain is about 11dB at 100MHz and slowly drops off to 10dB at 500MHz. The gain is about 8dB at 900MHz and 7dB at 1.2 GHz which is typical of NE/SA5200 with a good printed circuit board layout. It can also be seen that both channels have a very well matched frequency response and matched gain to within 0.1dB at 100MHz and 0.2dB at 900MHz.

NE/SA5200 finds applications in many areas of RF communications. It is an ideal gain block for high performance, low cost, low power RF communications transceivers. A typical radio transceiver front-end is shown in Figure 4. This could be the front-end of a cellular phone, a VHF/ UHF hand-held transceiver, UHF cordless telephone or a spread spectrum system. The NE/SA5200 can be used in the receiver path of most systems as an LNA and pre-amplifier. The bandpass filter between the two amplifiers also minimize the noise into the first mixer. In the transmitter path, NE/SA5200 can be used as a buffer to the VCO and isolate the VCO from any load variations due to the power level changes in the power amplifier. This improves the stability of the VCOs. The NE/SA5200 can also be used as a pre-driver to the power amplifier modules.

The two amplifiers in NE/SA5200 can be easily cascaded to have a 13dB gain block at 900MHz. At 100MHz the gain will be 22dB and a noise figure of about 5.5dB. The NE/SA5200 can be operated at a higher voltage up to 9V for much improved 1dB output compression point and higher 3rd order intercept point.

Several stages of NE/SA5200 can also be cascaded and be used as an IF amplifier strip for DBS/TV/GPS receivers. Figure 5 shows a 60dB gain IF strip at 180MHz. The noise figure for the cascaded amplifier chain is given by equation 1.

NF (total) = NF1 + NF2/G1 + NF3/G1*G2 + NF4/G1*G2*G3 + ... (Equation. 1)

NOTE: The noise figure and gain should not be in dB in the above equation.

Since the noise figure for each stage is about 3.6dB and the gain is about 11dB, the noise figure for the 60dB gain IF strip will be about 6.4dB.

In applications where a single amplifier is required with a 7.5dB gain at 900MHz and current consumption is of paramount importance (battery powered receivers), the amplifier A1 can be used and amplifier A2 can be disabled by leaving GND2 (Pin 3) unconnected. This will reduce the total current consumption for the IC to a meager 4mA.

The ENABLE pin is useful for Time-Division-Duplex systems where the receiver can be disabled for a period of time. In this case the overall system supply current will be decreased by 8mA.

The ENABLE pin can also be used to improve the system dynamic range. For input levels that are extremely high, the NE/SA5200 can be disabled. In this case the input signal is attenuated by 13dB. This prevents the system from being overloaded as well as improves the system's overall dynamic range. In the disabled condition the NE/SA5200 IP_3 increases to nearly +20dBm.

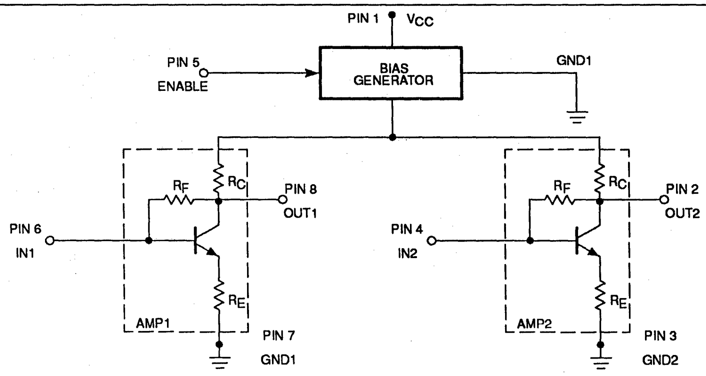
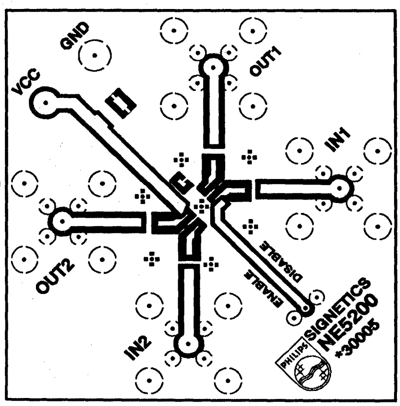
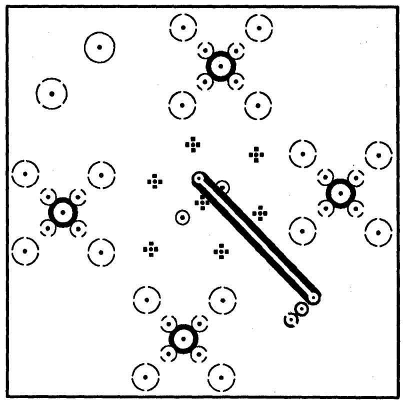


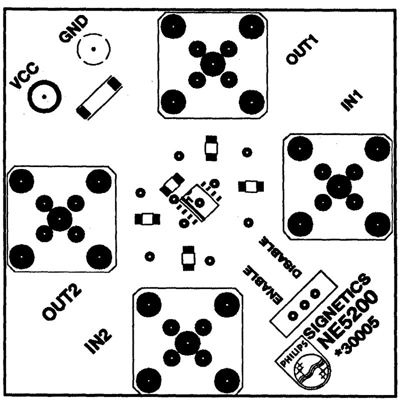
Figure 1. Simplified Equivalent Schematic of NE/SA5200



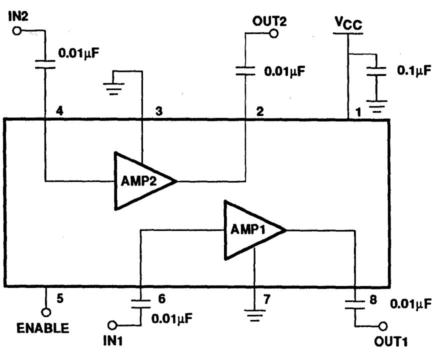
a. Top Side



b. Bottom Side



c. Top Silk Screen



d. NE/SA5200 Evaluation Board Schematic

Figure 2. Printed Circuit Board Layout of the NE/SA5200 Evaluation Board

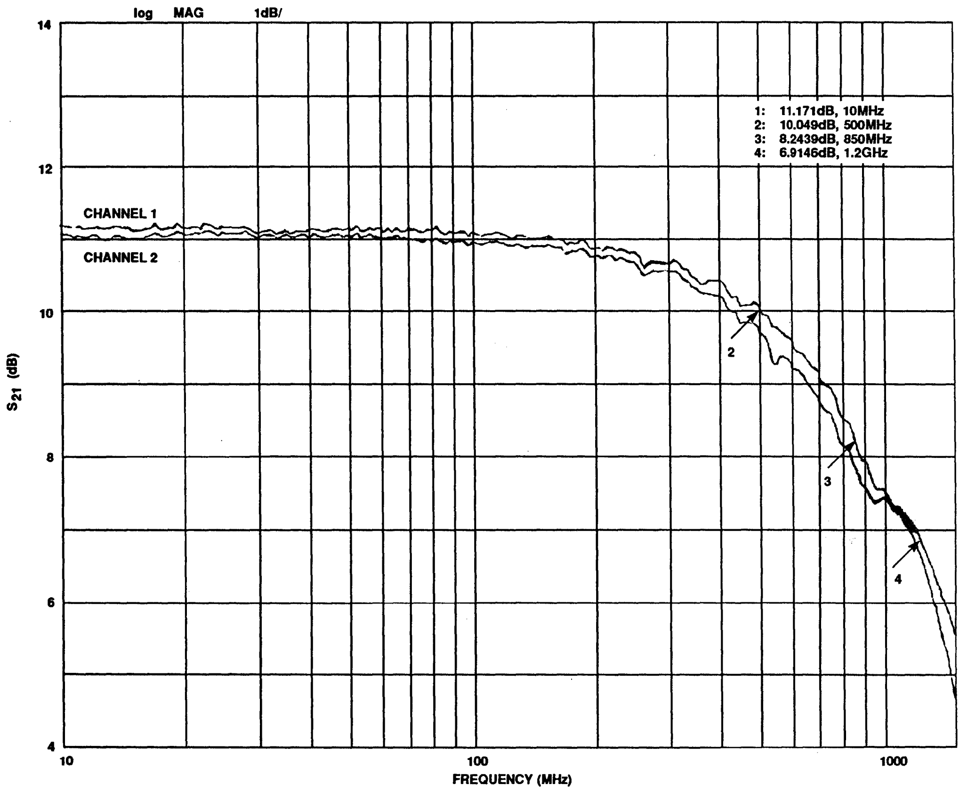


Figure 3. Typical Frequency Response of NE/SA5200 in a 50Ω System

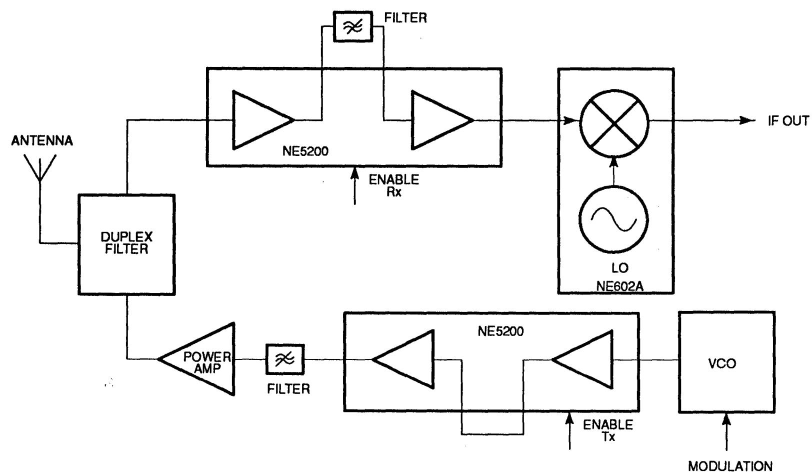


Figure 4. Typical Radio Transceiver Front-End

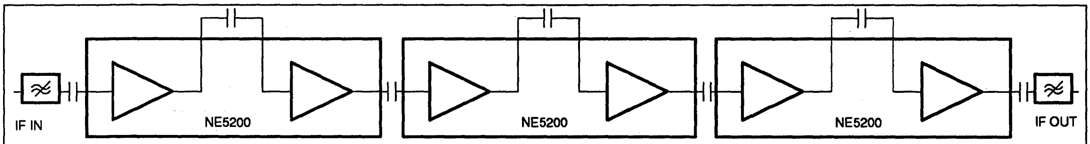


Figure 5. 60dB IF Gain Block for 100-300MHz IF for GPS/DBS Systems

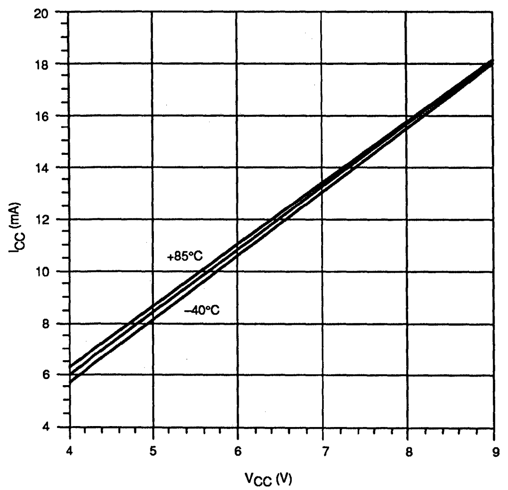


Figure 6. Supply Current vs Supply Voltage and Temperature

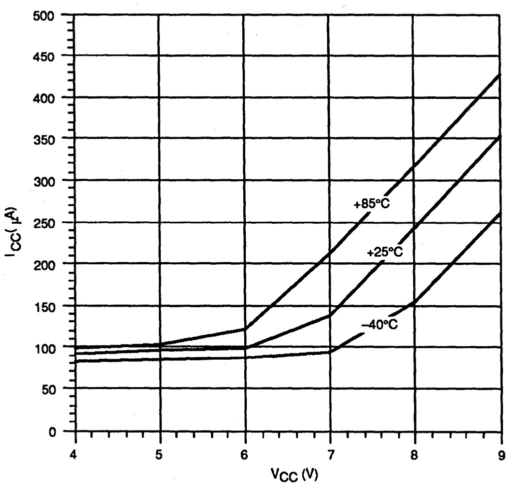


Figure 7. Disabled Supply Current vs V_{CC} and Temperature

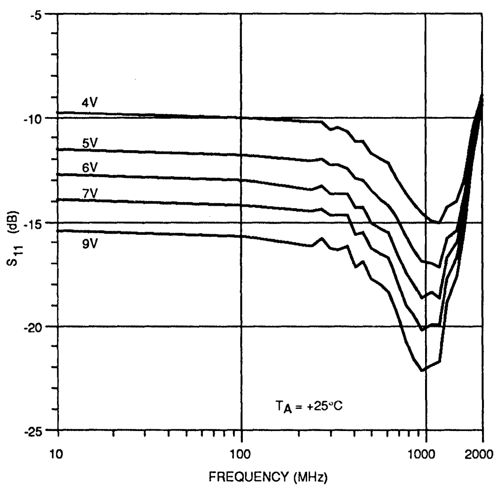


Figure 8. Input Match vs Frequency and V_{CC}

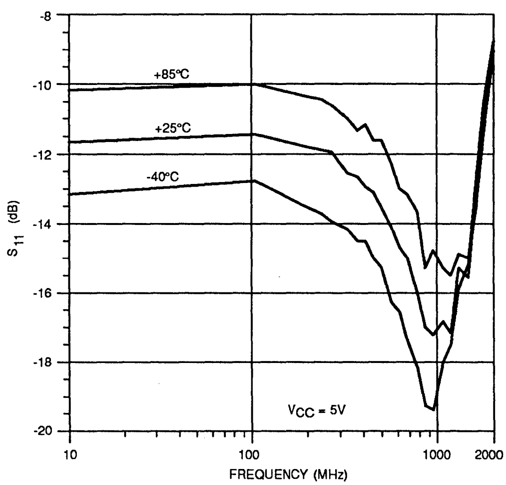


Figure 9. Input Match vs Frequency and Temperature

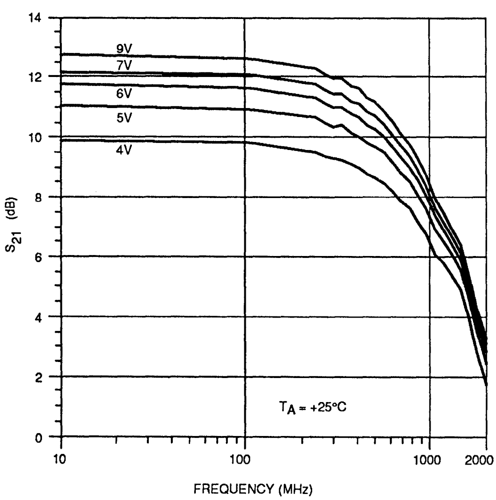


Figure 10. Insertion Gain vs Frequency and V_{CC}

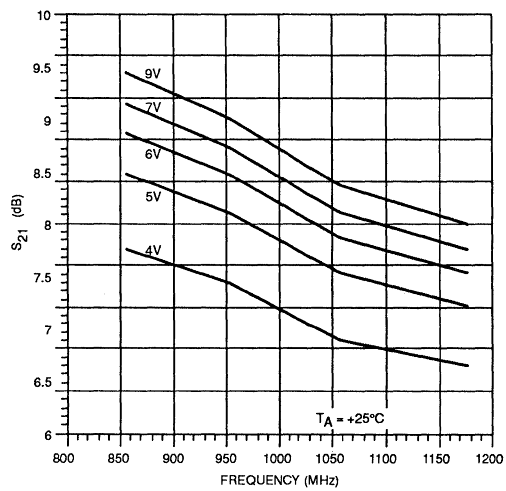


Figure 11. Insertion Gain vs Frequency and V_{CC} — Expanded Detail —

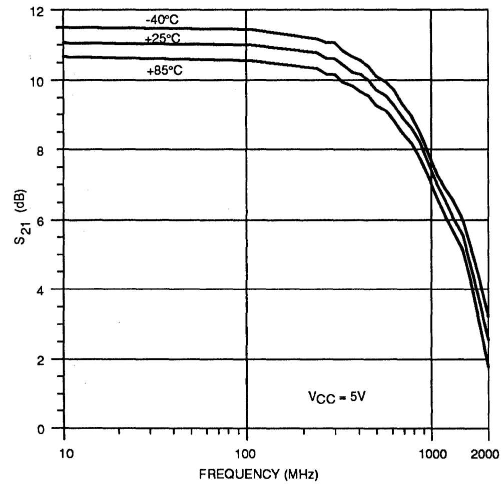


Figure 12. Insertion Gain vs Frequency and Temperature

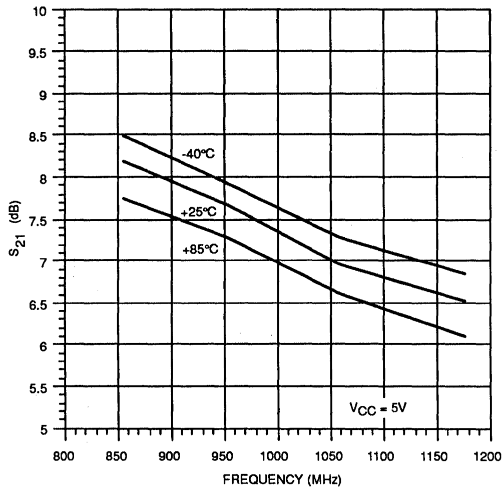


Figure 13. Insertion Gain vs Frequency and Temperature – Expanded Detail –

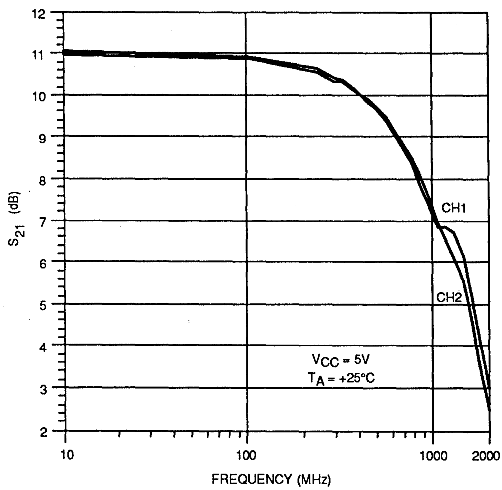


Figure 14. Insertion Gain Matching (CH1 vs CH2) vs Frequency

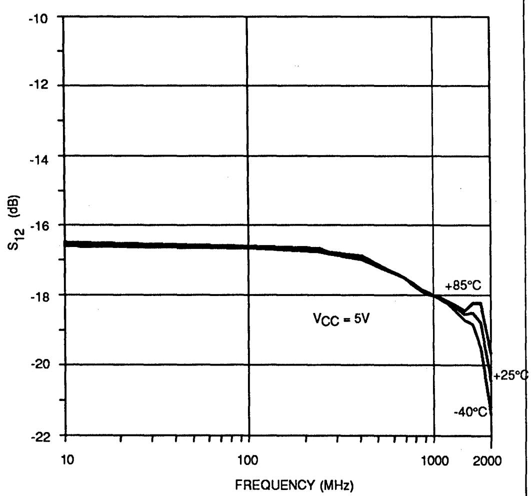


Figure 15. Reverse Insertion Gain vs Frequency and Temperature

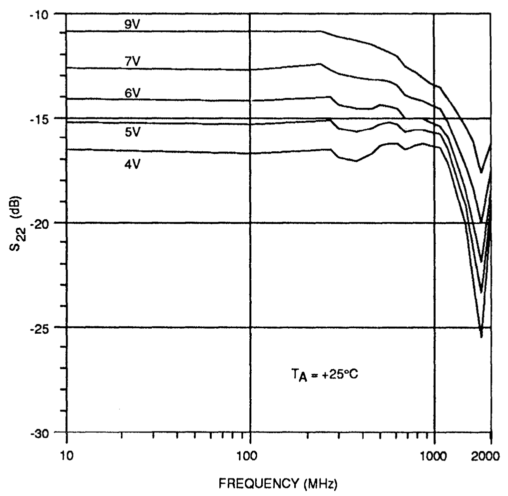


Figure 16. Output Match vs Frequency and V_{CC}

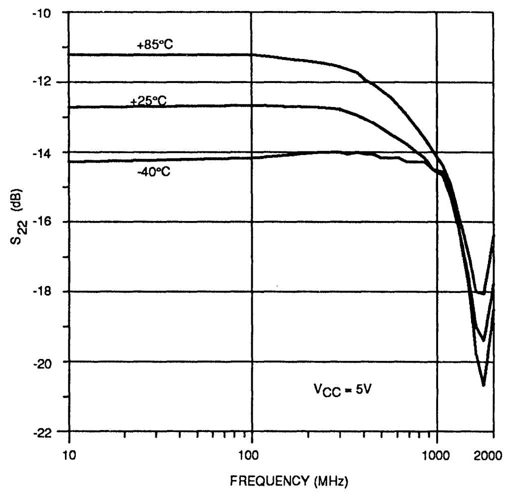


Figure 17. Output Match vs Frequency and Temperature

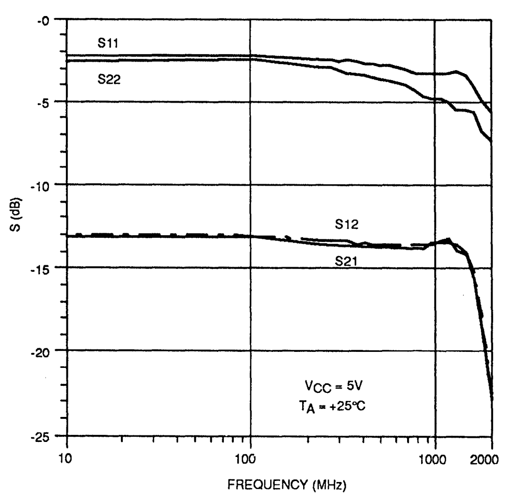


Figure 18. S-parameters vs Frequency for Disabled Amplifier

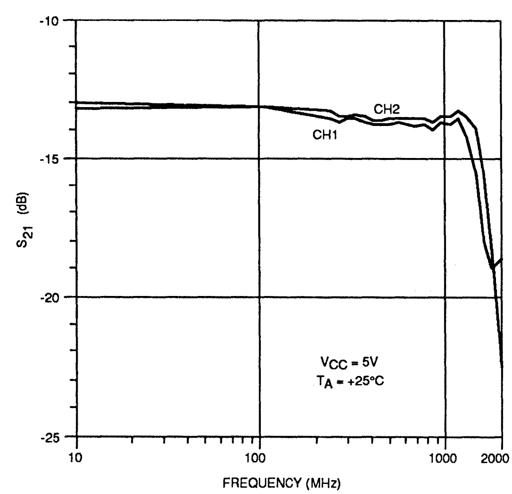


Figure 19. Insertion Gain Matching Disabled (CH1 vs CH2) vs Frequency

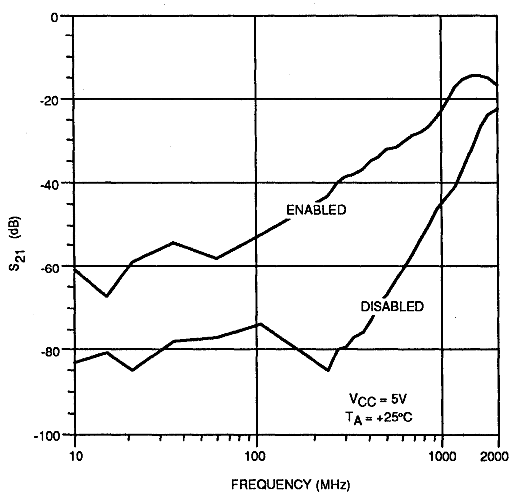


Figure 20. CH1 Input to CH2 Output Isolation vs Frequency

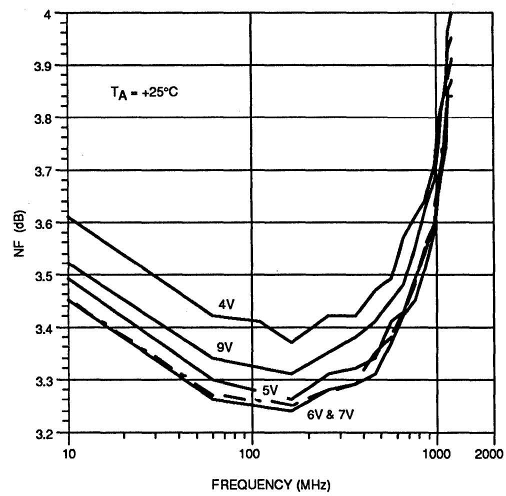


Figure 21. Noise Figure vs Frequency and V_{CC} in a 50Ω System

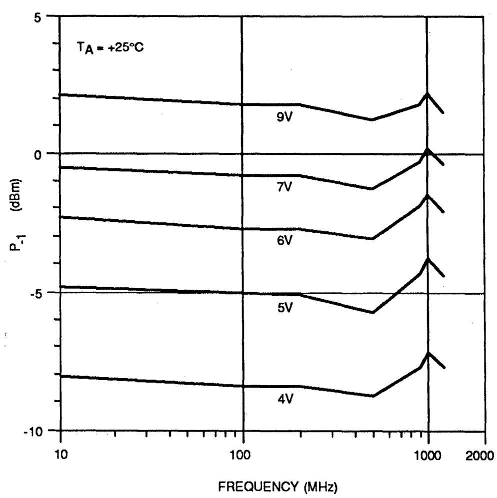


Figure 22. 1dB Output Compression Point vs Frequency and V_{CC}

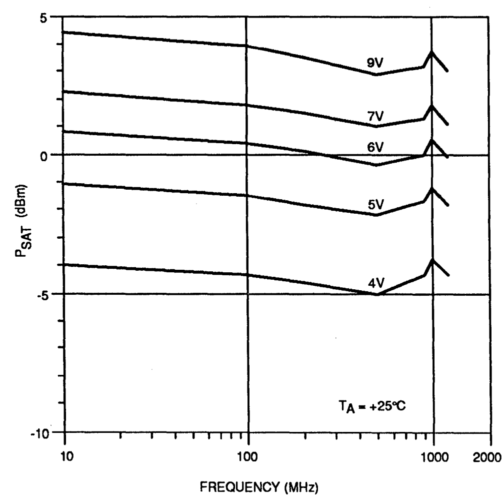


Figure 23. Saturated Output Power vs Frequency and V_{CC}

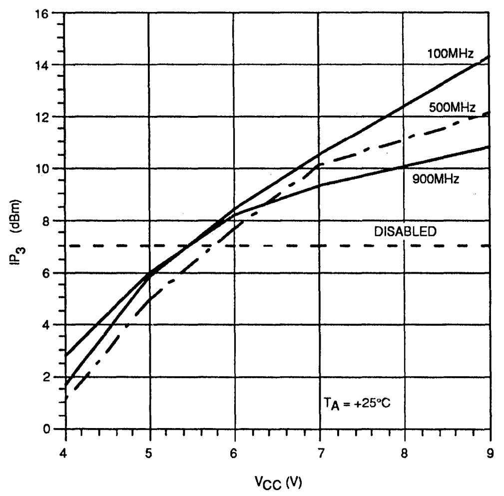


Figure 24. Third-Order Output Intercept vs Frequency and V_{CC}

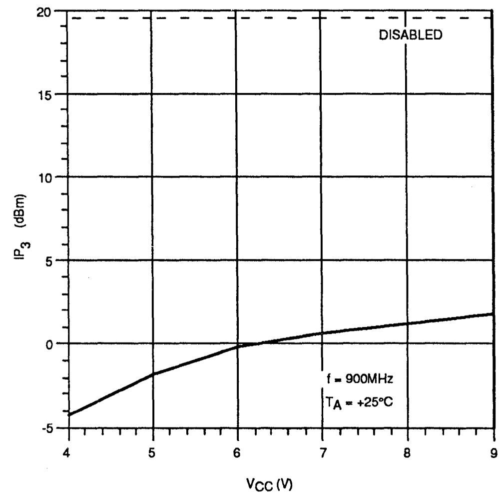


Figure 25. Third-Order Input Intercept vs Frequency and V_{CC}

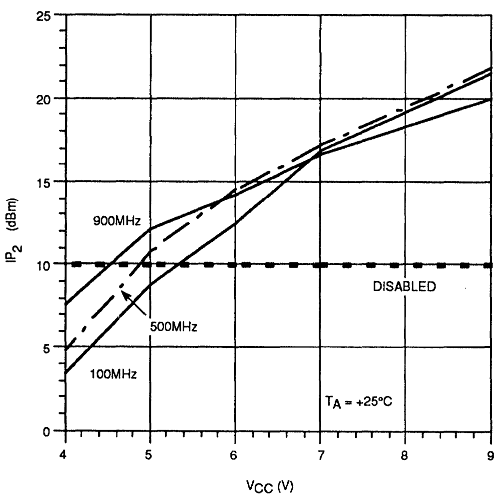


Figure 26. Second-Order Output Intercept vs Frequency and V_{CC}

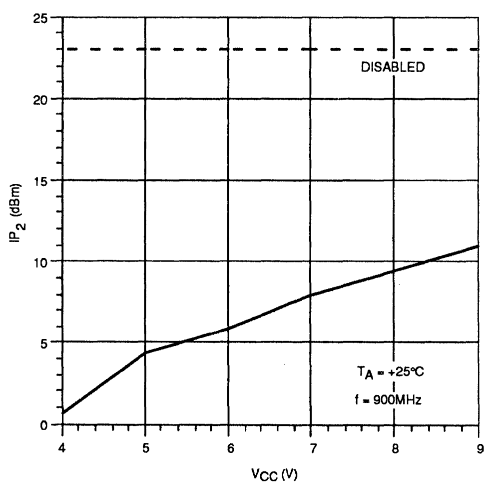


Figure 27. Second-Order Input Intercept vs Frequency and V_{CC}

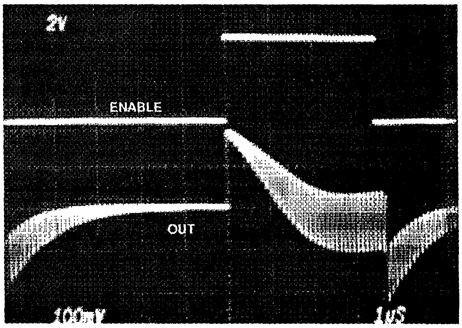


Figure 28. Switching Speed; f_{IN} = 10MHz at –26dBm, V_{DD} = 5V, Coupling Capacitors Set to 0.01μF

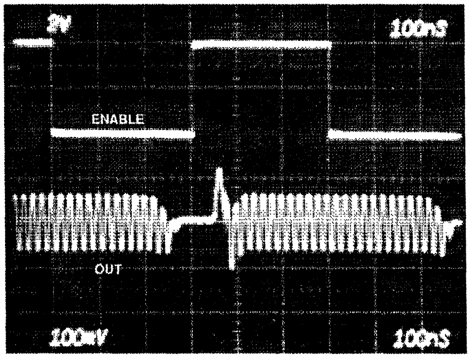


Figure 29. Switching Speed; f_{IN} = 50MHz at –26dBm, V_{DD} = 5V, Coupling Capacitors Set to 100pF

Wide-band high-frequency amplifier — NE/SA5204

DESCRIPTION

The NE/SA5204 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The -3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204 operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204 is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC-coupling capacitors because the NE/SA5204 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

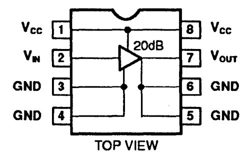
The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204s in series as required, without any degradation in amplifier stability.

FEATURES

- Bandwidth (min.)
  200 MHz, ±0.5dB
  350 MHz, -3dB
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface-mount package available
- Cascadable

PIN CONFIGURATION

N, D Packages



APPLICATIONS

- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broadband LANs
- Networks
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

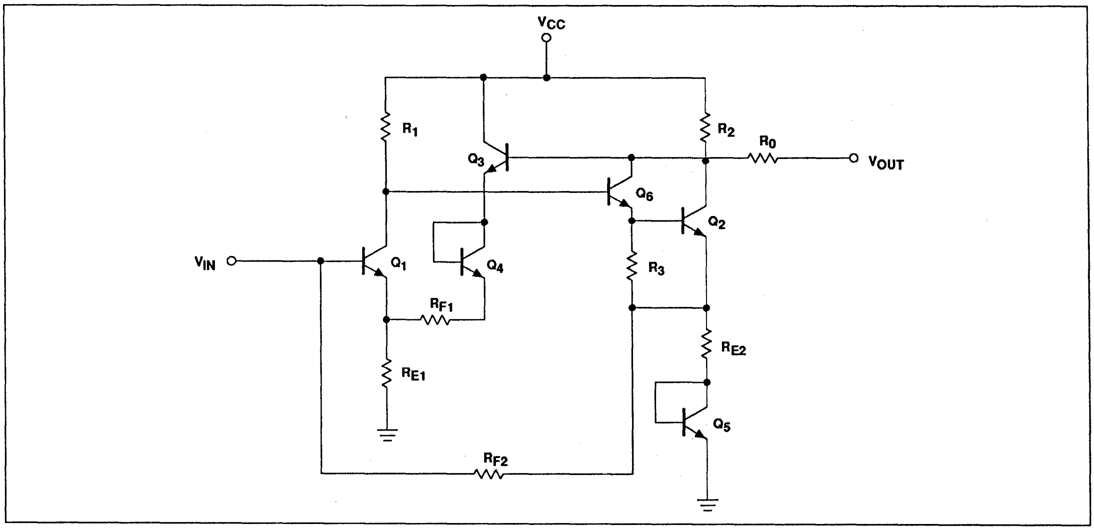
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C –40 to +85°C	NE5204N SA5204N
8-Pin Plastic SO package	0 to +70°C –40 to +85°C	NE5204D SA5204D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	–40 to +85	°C
P_{DMAX}	Maximum power dissipation[1, 2] T_A=25°C(still–air)		
	N package	1160	mW
	D package	780	mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	–55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	24	31	mA
S21	Insertion gain	f=100MHz, over temperature	16	19	22	dB
S11	Input return loss	f=100MHz		25		dB
		DC –550MHz		12		dB
S22	Output return loss	f=100MHz		27		dB
		DC –550MHz		12		dB
S12	Isolation	f=100MHz		–25		dB
		DC –550MHz		–18		dB
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f=100MHz		4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0		dB
	Saturated output power	f=100MHz		+7.0		dBm
	1dB gain compression	f=100MHz		+4.0		dBm
	Third–order intermodulation intercept (output)	f=100MHz		+17		dBm
	Second–order intermodulation intercept (output)	f=100MHz		+24		dBm
t_R	Rise time			5		ps
	Propagation delay			5		ps

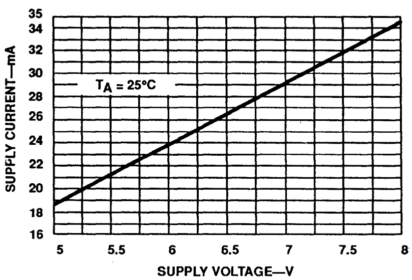


Figure 1. Supply Current vs Supply Voltage

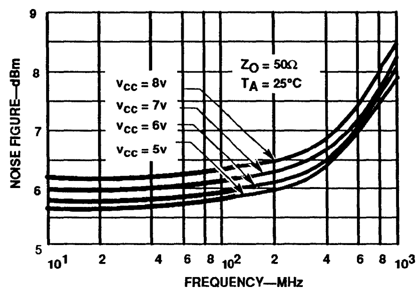


Figure 2. Noise Figure vs Frequency

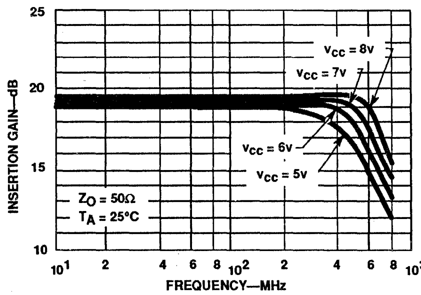


Figure 3. Insertion Gain vs Frequency (S_{21})

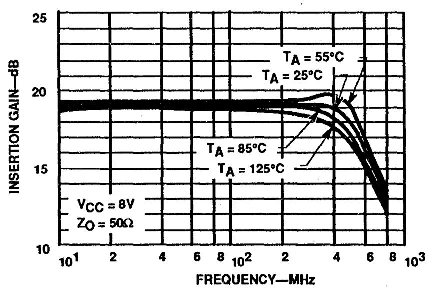


Figure 4. Insertion Gain vs Frequency (S_{21})

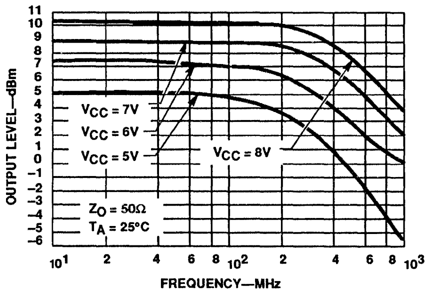


Figure 5. Saturated Output Power vs Frequency

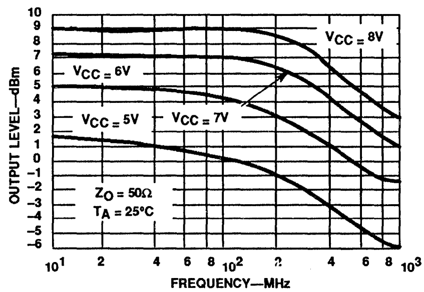


Figure 6. 1dB Gain Compression vs Frequency

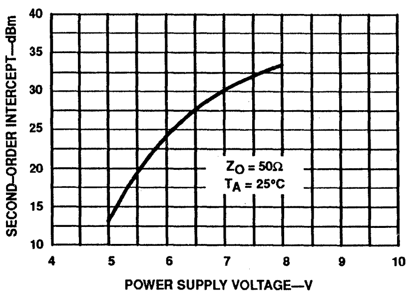


Figure 7. Second-Order Output Intercept vs Supply Voltage

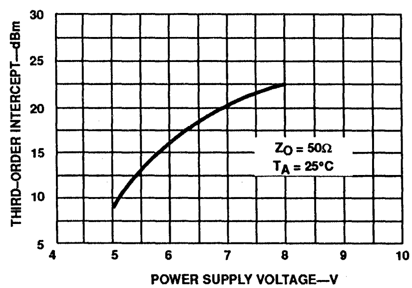


Figure 8. Third-Order Intercept vs Supply Voltage

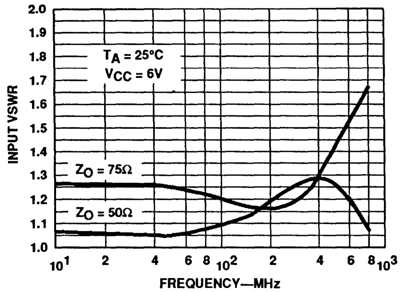


Figure 9. Input VSWR vs Frequency

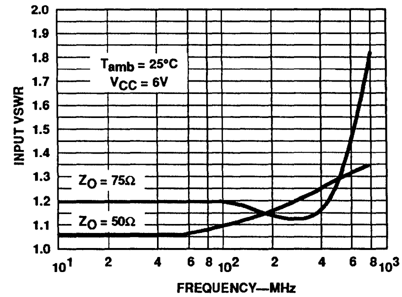


Figure 10. Output VSWR vs Frequency

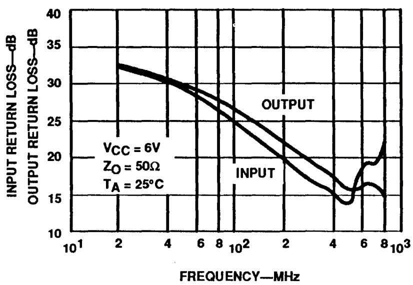


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

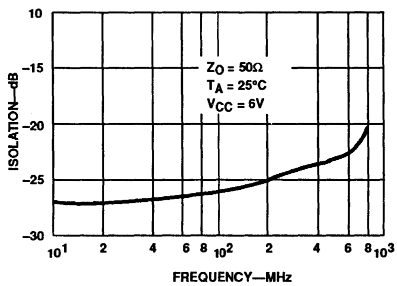


Figure 12. Isolation vs Frequency (S_{12})

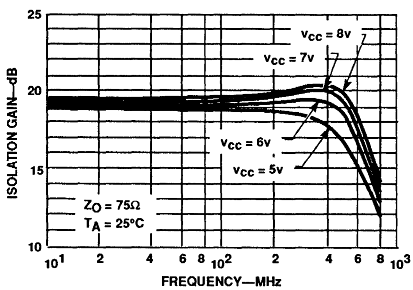


Figure 13. Insertion Gain vs Frequency (S_{21})

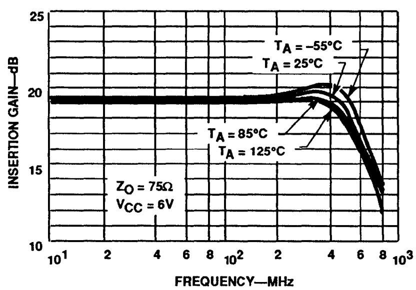


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1}) \;/\; R_{E1} \qquad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10Log\left\{1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_O}\right\} dB \qquad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\,R_{E1} \qquad (3)$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2, \qquad (4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=7mA and I_{C6}=5mA.

From here, it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

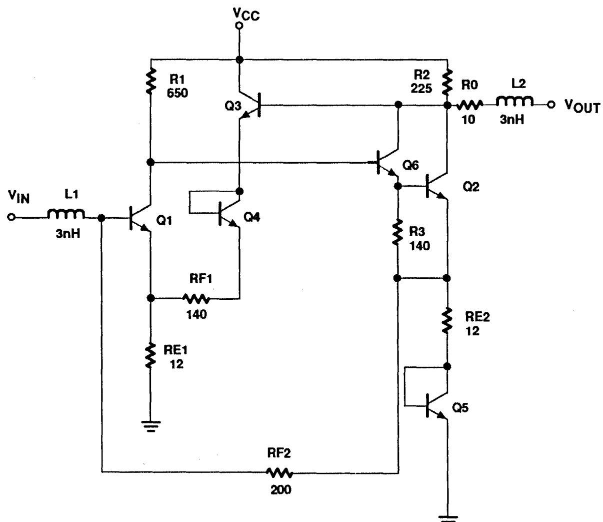


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

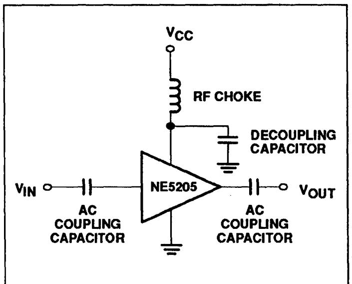
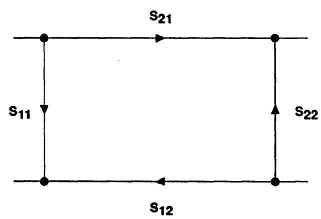


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

SCATTERING PARAMETERS

The primary specifications for the NE5204 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OSOLATION

$$S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

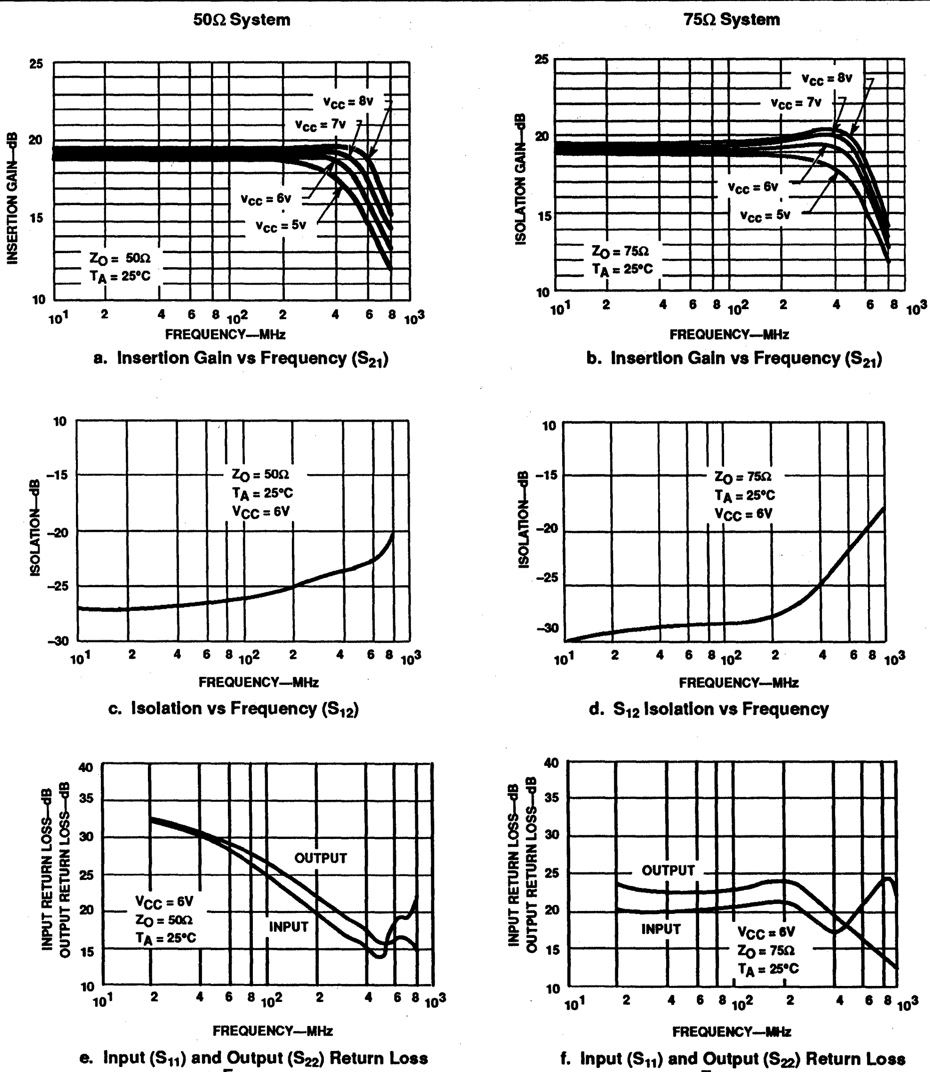
$$S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

b.

Figure 17.



a. Insertion Gain vs Frequency (S_{21})

b. Insertion Gain vs Frequency (S_{21})

c. Isolation vs Frequency (S_{12})

d. S_{12} Isolation vs Frequency

e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18.

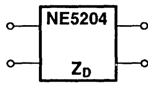
Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205 to other high-frequency amplifiers.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE/SA/SE5205

$P_{IN} + \frac{V_{IN}^2}{Z_D}$



$P_{OUT} + \frac{V_{OUT}^2}{Z_D}$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I = V_I^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the NE/SA/SE5205 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20dB$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20dB$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20dB$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS=S_{11}dB

$S_{11}dB = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS=S_{22}dB

$S_{22}dB = 20 \text{ Log } |S_{22}|$

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1DB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

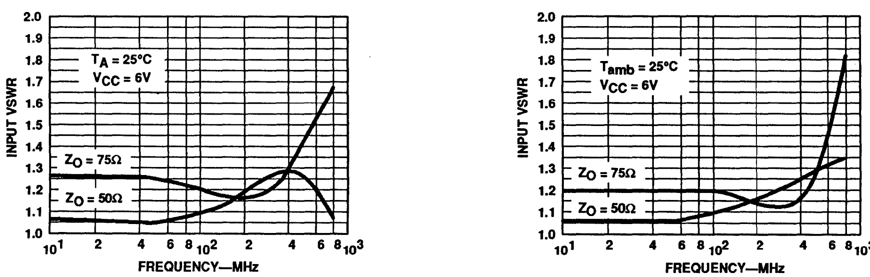
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One



a. Input VSWR vs Frequency **b. Output VSWR vs Frequency**

Figure 19. Input/Output VSWR vs Frequency

must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205 we have chosen an output level of –10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively. *5COL

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

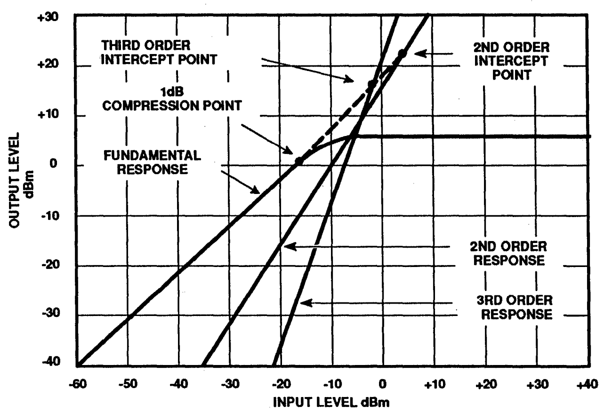


Figure 20.

Wide-band high-frequency amplifier

NE/SA5205

DESCRIPTION

The NE/SA/SE5205 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the -3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205 operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205 solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the -3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the -3dB frequency to 600MHz. The Cerdip package is hermetically sealed, and can operate over the full -55°C to +125°C range.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

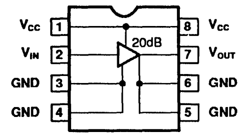
The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205s in series as required, without any degradation in amplifier stability.

FEATURES

- 600MHz bandwidth
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface mount package available
- MIL-STD processing available

PIN CONFIGURATIONS

N, FE, D Packages



TOP VIEW

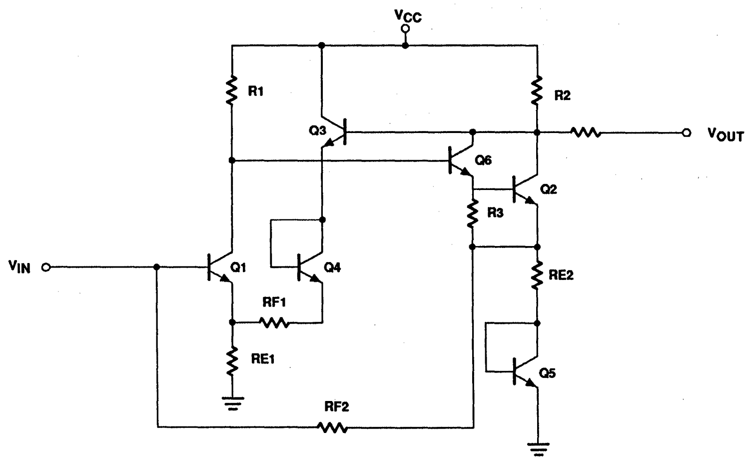
APPLICATIONS

- 75Ω cable TV decoder boxes
- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broad-band LANs
- Fiber-optics
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5205D
8-Pin Cerdip	0 to +70°C	NE5205FE
8-Pin Plastic DIP	0 to +70°C	NE5205N
8-Pin Plastic SO	-40 to +85°C	SA5205D
8-Pin Plastic DIP	-40 to +85°C	SA5205N
8-Pin Cerdip	-40 to +85°C	SA5205FE
8-Pin Cerdip	-55 to +125°C	SE5205FE
8-Pin Plastic DIP	-55 to +125°C	SE5205N

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	-40 to +85	°C
	SE grade	-55 to +125	°C
P_{DMAX}	Maximum power dissipation, T_A=25°C (still-air)[1, 2]		
	FE package	780	mW
	N package	1160	mW
	D package	780	mW

NOTES:
1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Operating supply voltage range	Over temperature	5 5		6.5 6.5	5 5		8 8	V V
I_{CC}	Supply current	Over temperature	20 19	24	30 31	20 19	24	30 31	mA mA
S21	Insertion gain	f=100MHz Over temperature	17 16.5	19	21 21.5	17 16.5	19	21 21.5	dB
S11	Input return loss	f=100MHz D, N, FE		25			25		dB
		DC - f_{MAX} D, N, FE	12			12			dB
S11	Input return loss	f=100MHz EC package					24		dB
		DC - f_{MAX} EC				10			dB
S22	Output return loss	f=100MHz D, N, FE		27			27		dB
		DC - f_{MAX}	12			12			dB
S22	Output return loss	f=100MHz EC package					26		dB
		DC - f_{MAX}				10			dB
S12	Isolation	f=100MHz		-25			-25		dB
		DC - f_{MAX}	-18			-18			dB
t_R	Rise time			5			5		ps
	Propagation delay			5			5		ps
BW	Bandwidth	±0.5dB D, N					450		MHz
f_{MAX}	Bandwidth	±0.5dB EC					500		MHz
f_{MAX}	Bandwidth	±0.5dB FE		300			300		MHz
f_{MAX}	Bandwidth	-3dB D, N				550			MHz
f_{MAX}	Bandwidth	-3dB EC				600			MHz
f_{MAX}	Bandwidth	-3dB FE	400			400			MHz
	Noise figure (75Ω)	f=100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0			6.0		dB
	Saturated output power	f=100MHz		+7.0			+7.0		dBm
	1dB gain compression	f=100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f=100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f=100MHz		+24			+24		dBm

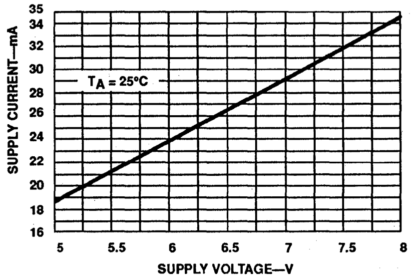


Figure 1. Supply Current vs Supply Voltage

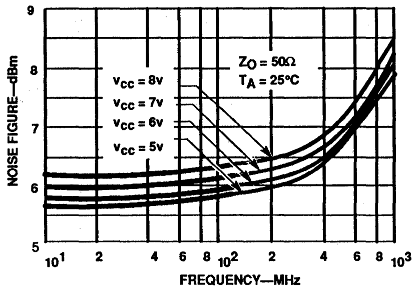


Figure 2. Noise Figure vs Frequency

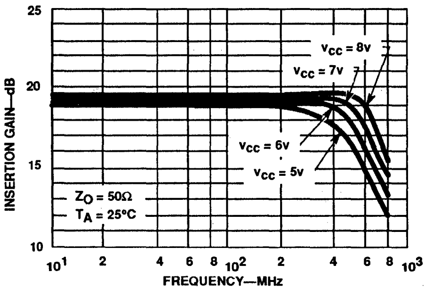


Figure 3. Insertion Gain vs Frequency (S_{21})

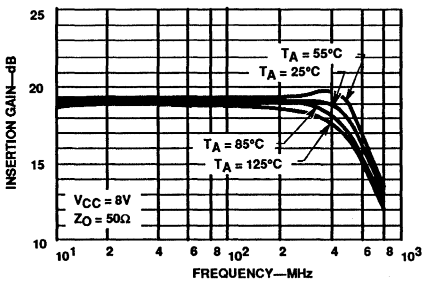


Figure 4. Insertion Gain vs Frequency (S_{21})

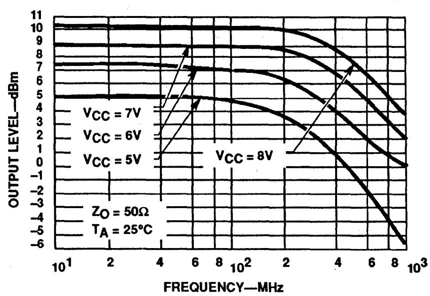


Figure 5. Saturated Output Power vs Frequency

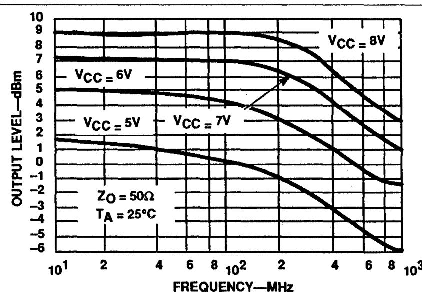


Figure 6. 1dB Gain Compression vs Frequency

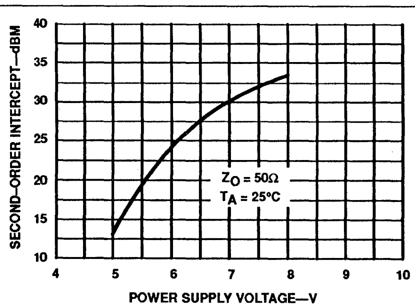


Figure 7. Second-Order Output Intercept vs Supply Voltage

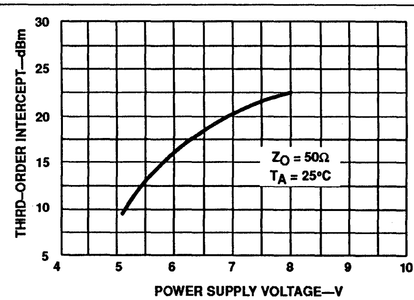


Figure 8. Third-Order Intercept vs Supply Voltage

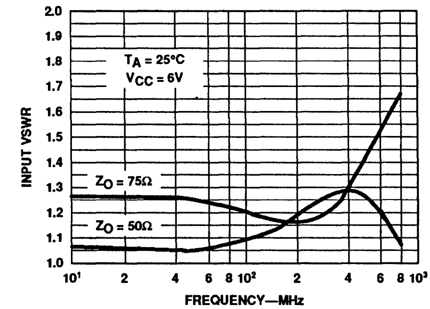


Figure 9. Input VSWR vs Frequency

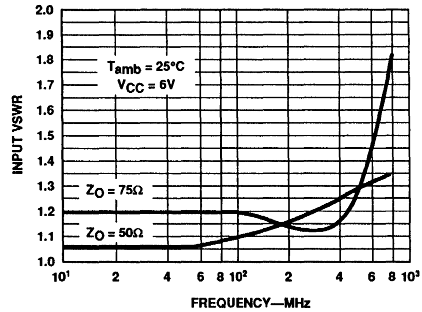


Figure 10. Output VSWR vs Frequency

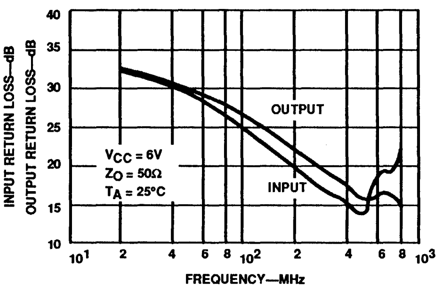


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

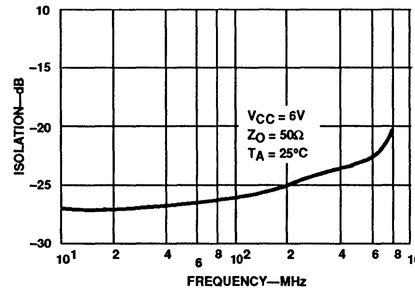


Figure 12. Isolation vs Frequency (S_{12})

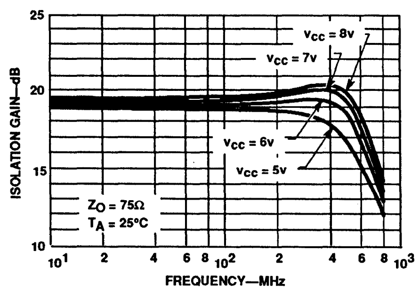


Figure 13. Insertion Gain vs Frequency (S_{21})

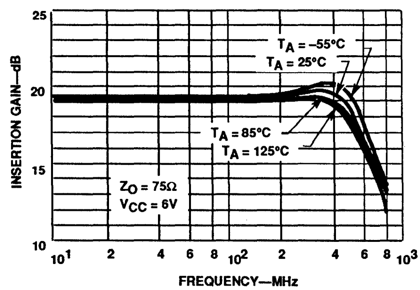


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{(R_{F1} + R_{E1})}{R_{E1}} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10\log\left\{1 + \left[\frac{r_b + R_{E1} + \frac{KT}{2qI_{C1}}}{R_O}\right]\right\} dB \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1}$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2,(4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=7mA and I_{C6}=5mA.

From here it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

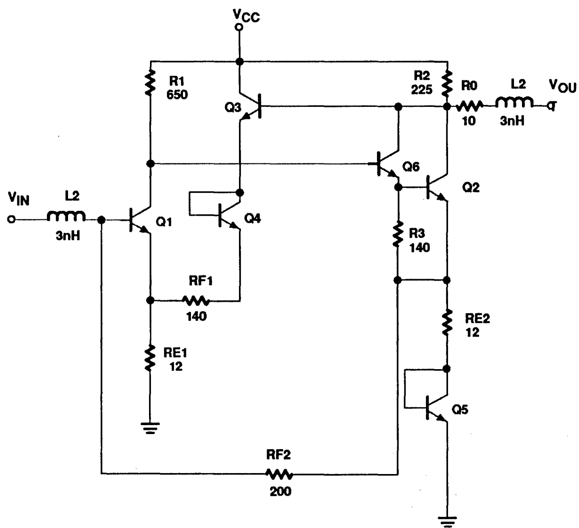


Figure 15. Schematic Diagram

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D and EC package body against the PC board plane.

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). In addition, if the EC package is used, the case should be soldered to the ground plane. The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205 to other high-frequency amplifiers.

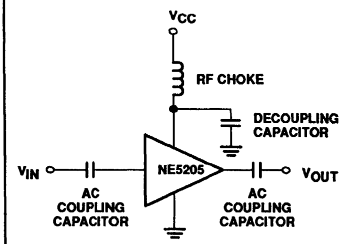


Figure 30. Circuit Schematic for Coupling and Power Supply Decoupling

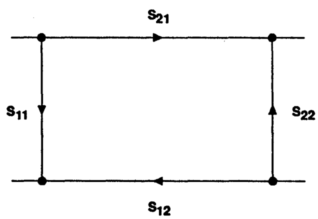


Figure 17a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OSOLATION

$$S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$$

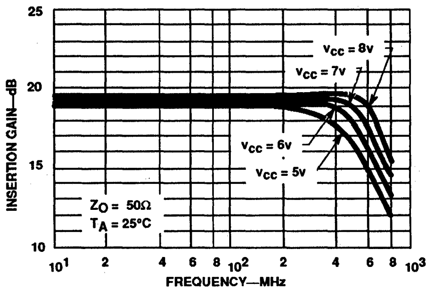
S_{22} — OUTPUT RETURN LOSS

$$S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

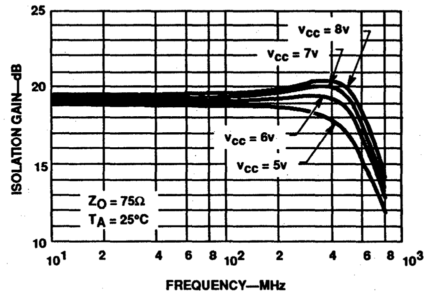
Figure 17b.

50Ω System

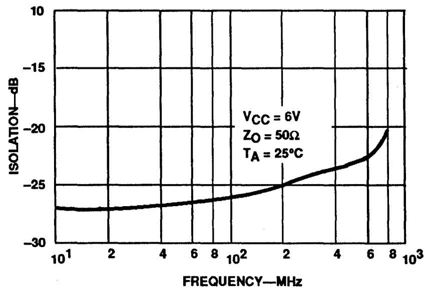
75Ω System



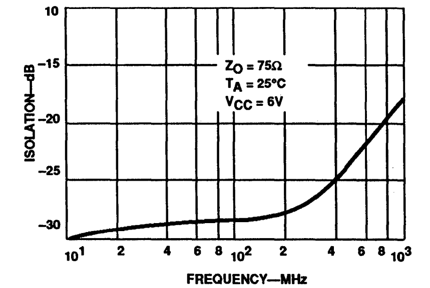
a. Insertion Gain vs Frequency (S_{21})



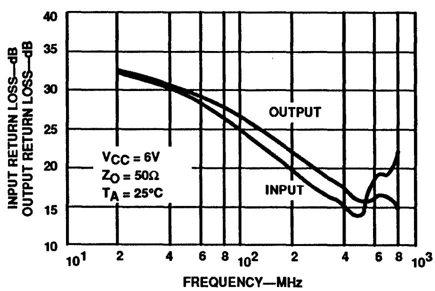
b. Insertion Gain vs Frequency (S_{21})



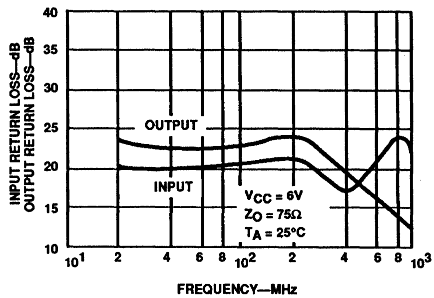
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency



f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE/SA/SE5205

$$P_{IN} + \frac{V_{IN}^2}{Z_D} \quad \text{NE/SA/ SE5205} \; Z_D \quad P_{OUT} + \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I = V_I^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the NE/SA/SE5205 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:
$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$
$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$
$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS=S_{11}dB
$S_{11}\text{dB} = 20 \text{ Log } |S_{11}|$
OUTPUT RETURN LOSS=S_{22}dB
$S_{22}\text{dB} = 20 \text{ Log } |S_{22}|$

INPUT VSWR=≤1.5
OUTPUT VSWR=≤1.5

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

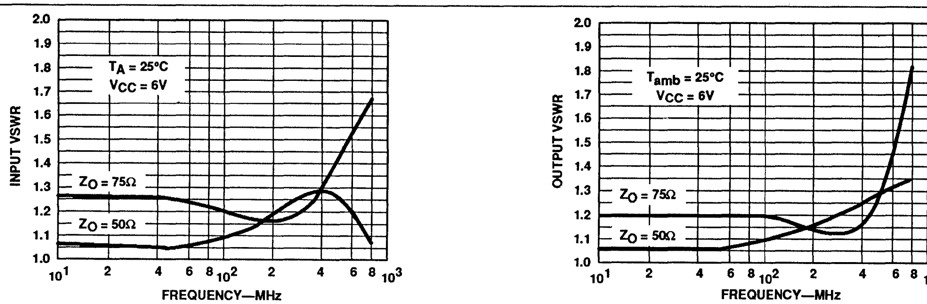
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205 we have chosen an output level of -10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency

b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

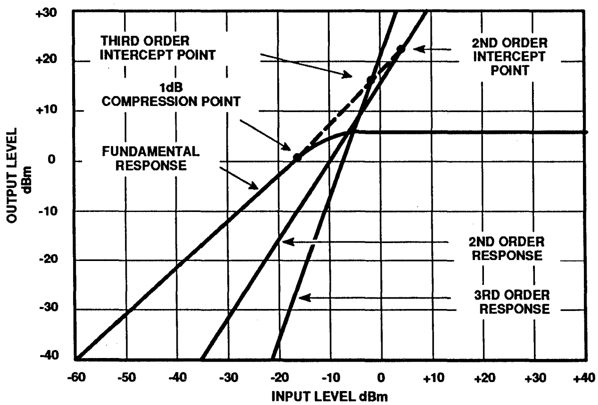


Figure 20.

DESCRIPTION

The NE5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kW) differential inputs. The output is 50W differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

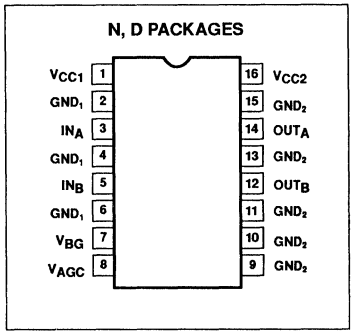
FEATURES

- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50W differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5209D
16-Pin Plastic DIP	0 to +70°C	NE5209N
16-Pin Plastic SO	-40 to +85°C	SA5209D
16-Pin Plastic DIP	-40 to +85°C	SA5209N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	$V_{CC1} = V_{CC2}$ = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, $V_{CC1} = V_{CC2}$ = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	38	43	48	mA
		Over temperature[1]	30		55	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	17	19	21	dB
		Over temperature[1]	16		22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	23	25	27	dB
		Over temperature[1]	22		28	dB
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.9	1.2	1.5	kΩ
		Over temperature[1]	0.8		1.7	kΩ
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	40	60	75	Ω
		Over temperature[1]	35		90	Ω
V_{OS}	Output offset voltage (output referred)			±20	±100	mV
		Over temperature[1]			±250	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
		Over temperature[1]	1.4		2.6	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
		Over temperature[1]	1.7		3.1	V
PSRR	Output offset supply rejection ratio		20	45		dB
	(output referred)	Over temperature[1]	15			dB
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
		Over temperature[1]	1.1		1.55	V

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC1} = V_{CC2} = +5.0V$, $V_{AGC} = 1.0V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
R_{BG}	Bandgap loading	Over temperature[1]	2	10		kΩ
V_{AGC}	AGC DC control voltage range	Over temperature[1]		0-1.3		V
I_{BAGC}	AGC pin DC bias current	$0V<V_{AGC}<1.3V$		-0.7	-6	μA
		Over temperature[1]			-10	μA

NOTES:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC1} = V_{CC2} = +5.0V$, $V_{AGC} = 1.0V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
BW	-3dB bandwidth		600	850		MHz
		Over temperature[1]	500			MHz
GF	Gain flatness	DC - 500MHz		±0.4		dB
		Over temperature[1]		±0.6		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[2]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended)	$R_L = 50Ω$		400		mV_{P-P}
	for linear operation[2]	$R_L = 1kΩ$		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	$R_S = 50Ω$, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	$R_L = 50Ω$		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.
2. With $R_L > 1kΩ$, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With $R_L = 50Ω$, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5209 APPLICATIONS

The NE5209 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5209 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5209 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5209 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5209 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5209. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5209 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5209 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5209 is shown in Figure 2. Three NE5209s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5209s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5209s will give a dynamic range in excess of 60dB.

The NE5209 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

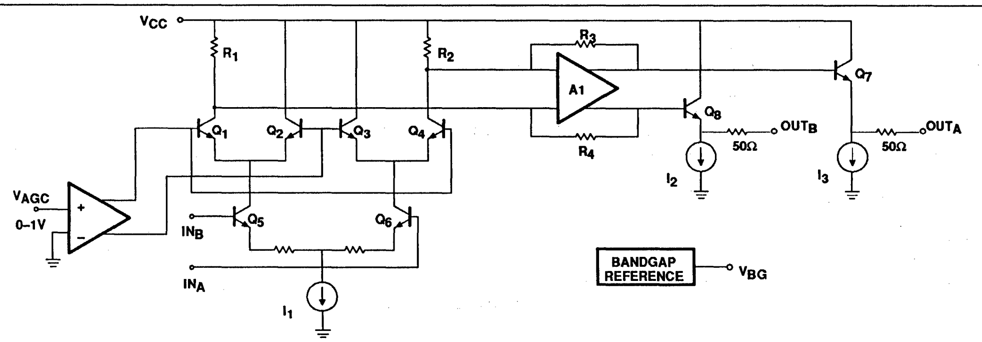


Figure 1. Equivalent Schematic of the VGA

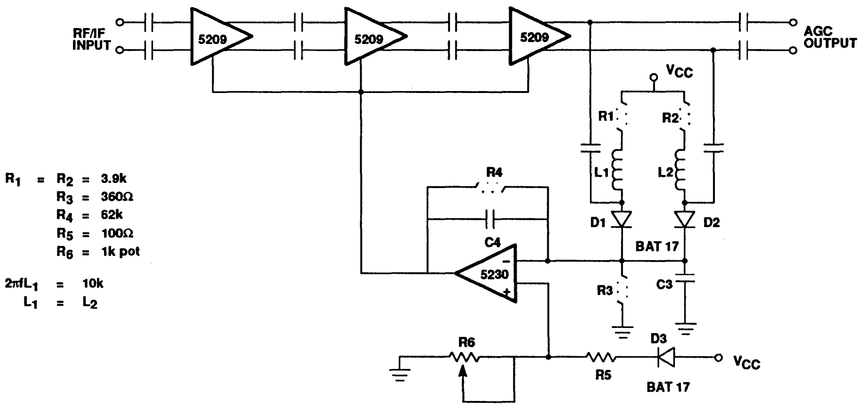


Figure 2. AGC Configuration Using Cascaded NE5209s

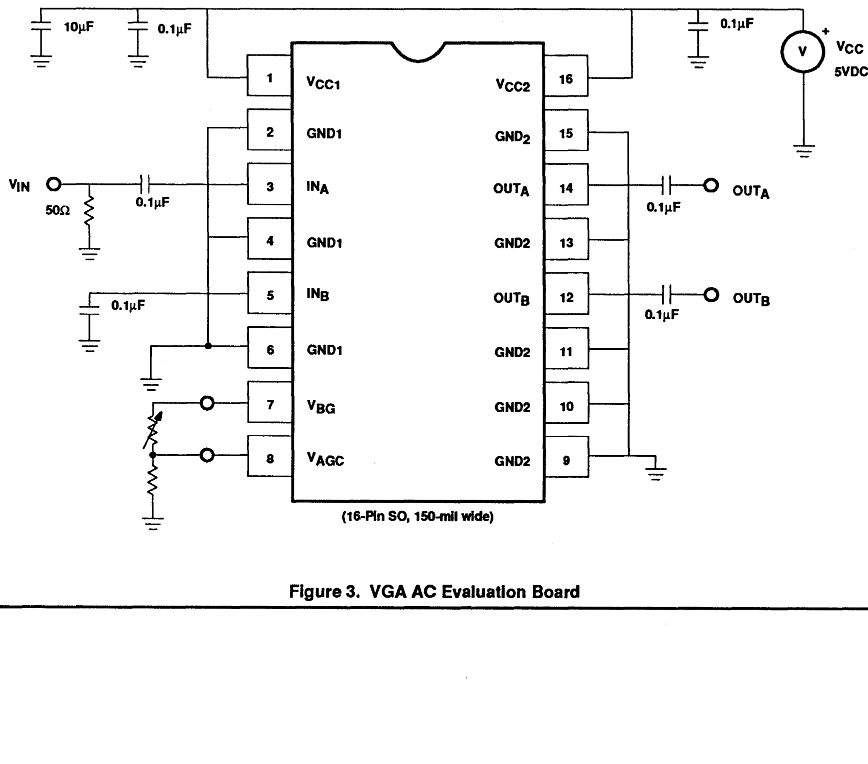
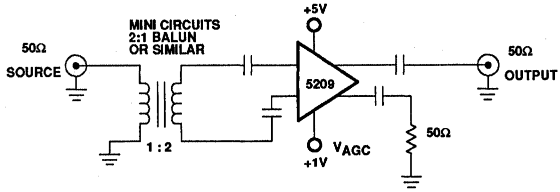
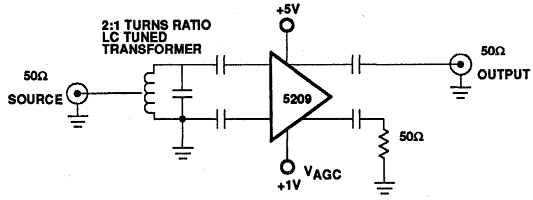


Figure 3. VGA AC Evaluation Board



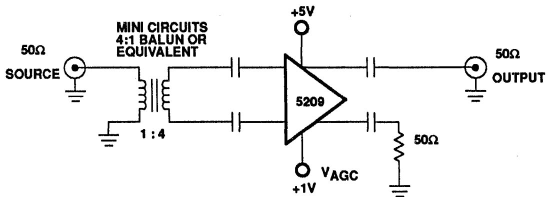
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



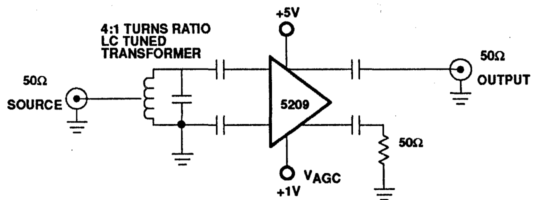
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization



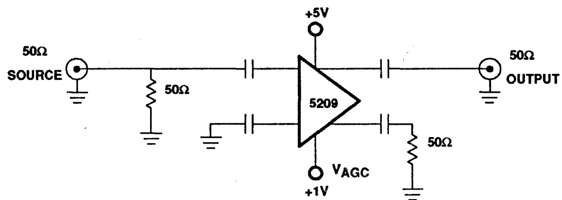
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 6. Broadband Gain Optimization



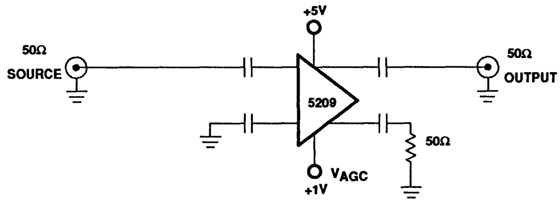
This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 7. Narrowband Gain Optimization



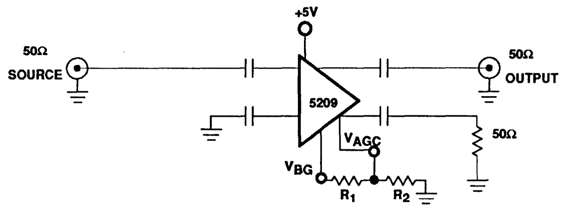
The noise figure of this configuration will be approximately 15dB.

Figure 8. Simple Amplifier Configuration



With the 50Ω source left unterminated, the noise figure is 9dB.

Figure 9 Unterminated Configuration

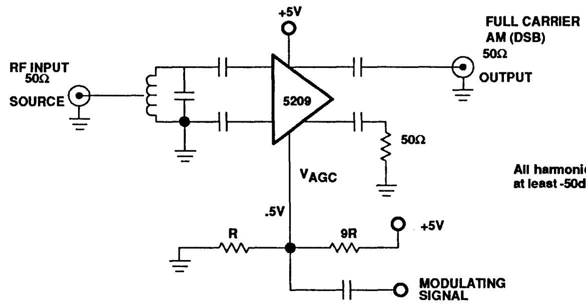


Gain = 19dB + $20\log_{10} V_{AGC}$

where $V_{AGC} = \left[\frac{R_2}{R_1 + R_2} V_{BG}\right]$

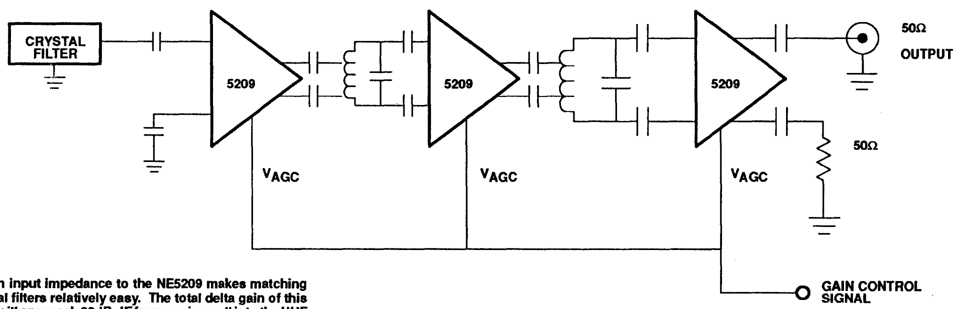
and is in units of Volts, for $V_{AGC} \le 1V$

Figure 10. User-Programmable Fixed Gain Block



All harmonic distortion products will be at least -50dBc over the audio spectrum.

Figure 11. AM Modulator



The high input impedance to the NE5209 makes matching to crystal filters relatively easy. The total delta gain of this system will approach 80dB. IF frequencies well into the UHF region can be configured with this type of architecture.

Figure 12. Receiver AGC IF Chain

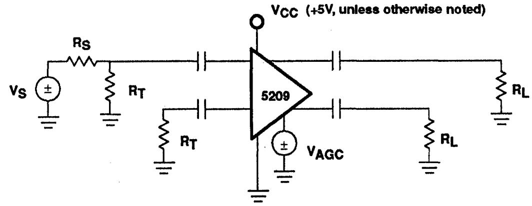


Figure 13. Test Set-up 1 (Used for all Graphs)

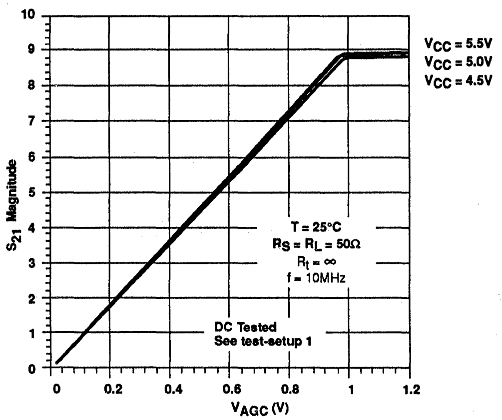


Figure 14. Gain vs V_{AGC} and V_{CC}

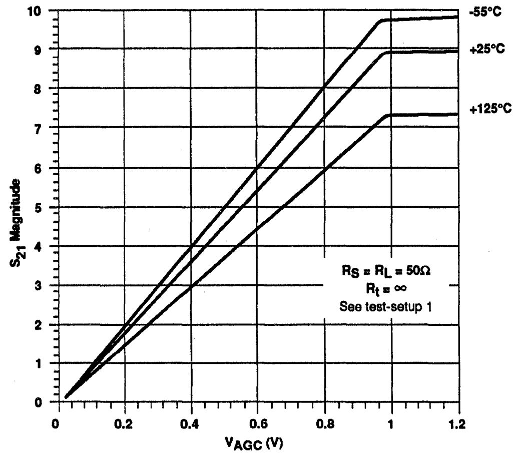


Figure 15. Insertion Gain vs V_{AGC} and Temperature

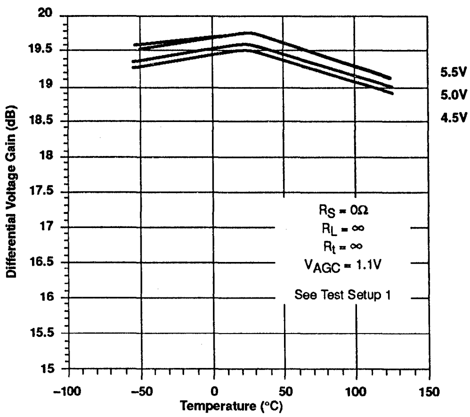


Figure 16. Voltage Gain vs Temperature and V_{CC}

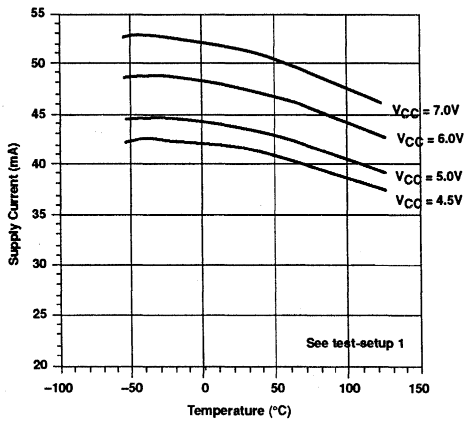


Figure 17. Supply Current vs Temperature and V_{CC}

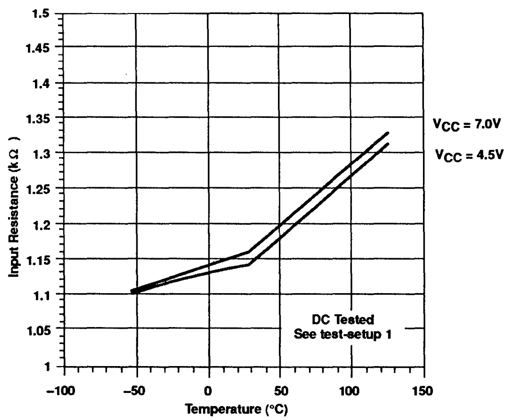


Figure 18. Input Resistance vs Temperature

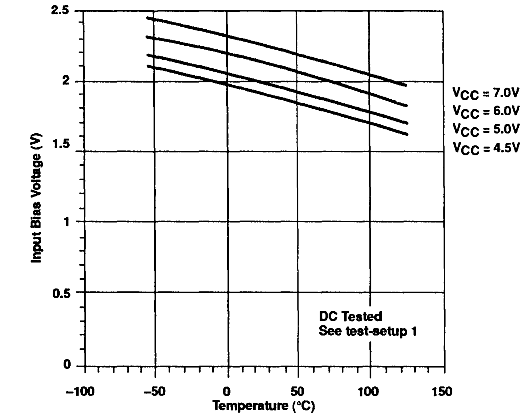


Figure 19. Input Bias Voltage vs Temperature

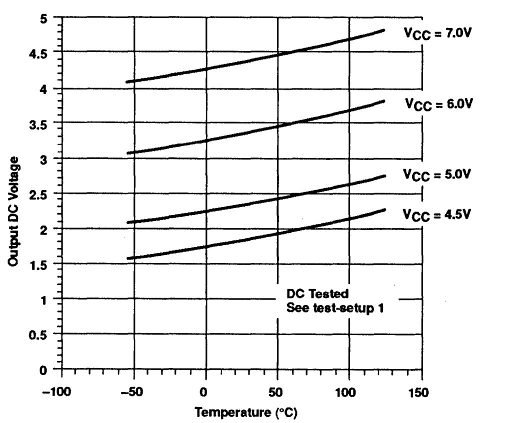


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

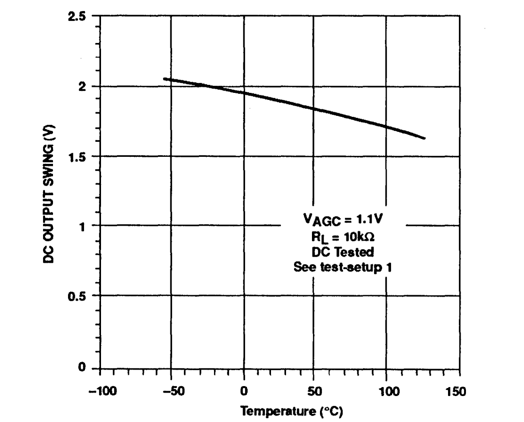


Figure 21. DC Output Swing vs Temperature

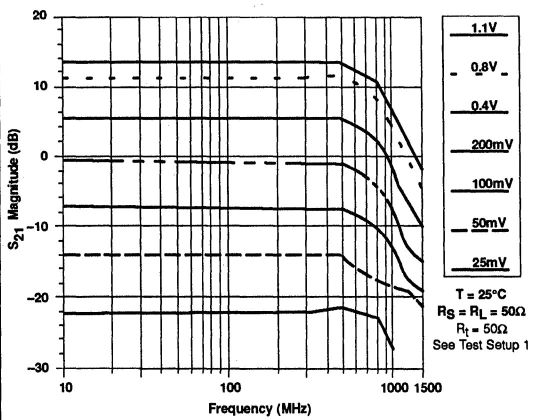


Figure 22. Insertion Gain vs Frequency and V_{AGC}

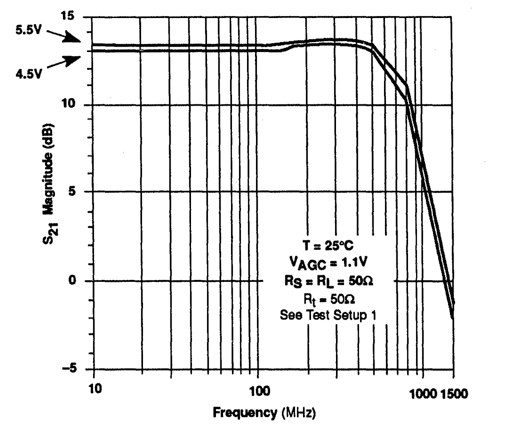


Figure 23. Insertion Gain vs Frequency and V_{CC}

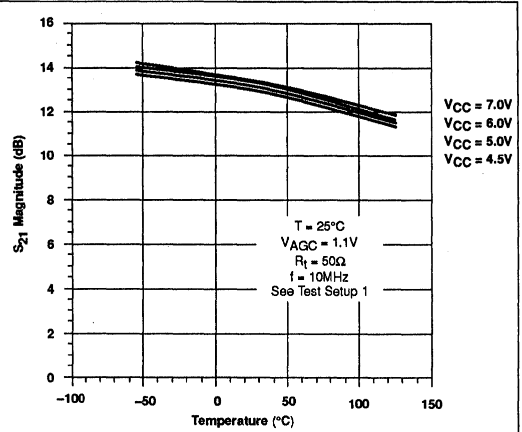


Figure 24. Insertion Gain vs Temperature and V_{CC}

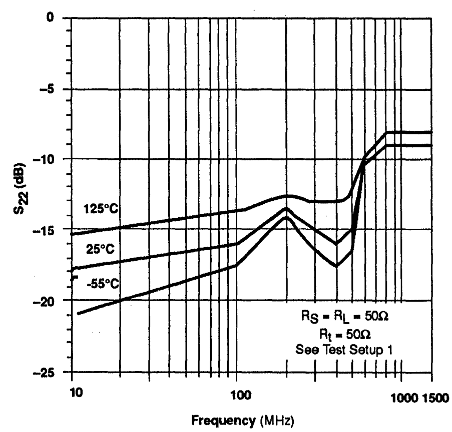


Figure 25. Output Return Loss vs Frequency

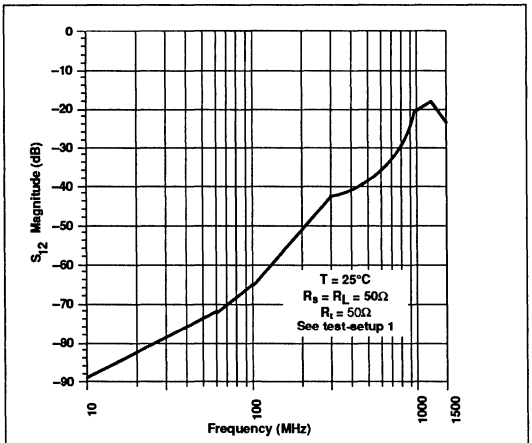


Figure 26. Reverse Isolation vs Frequency

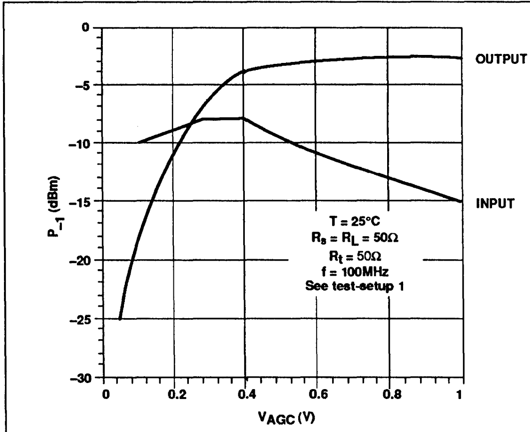


Figure 27. 1dB Gain Compression vs V_{AGC}

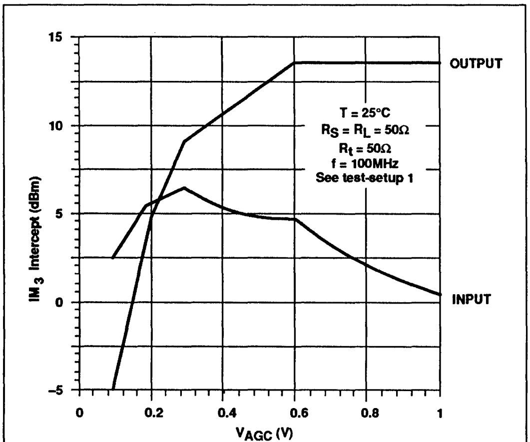


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

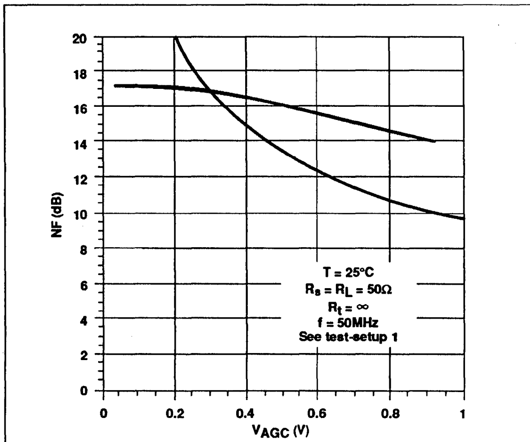


Figure 29. Noise Figure vs V_{AGC}

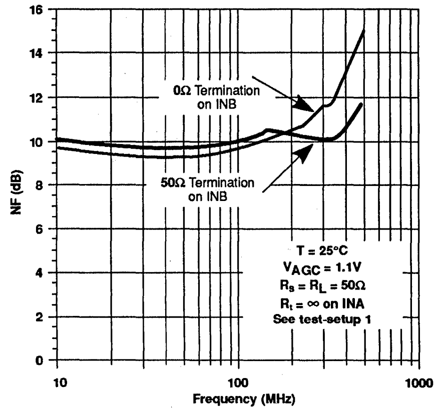


Figure 30. Noise Figure vs Frequency

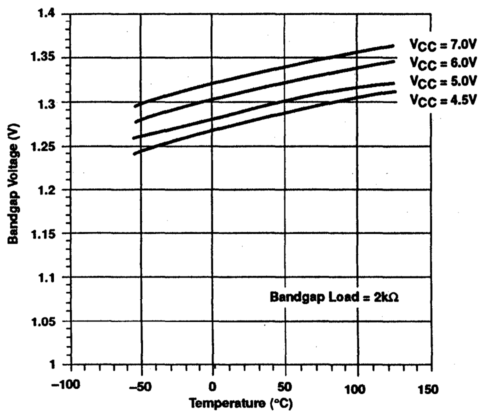


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

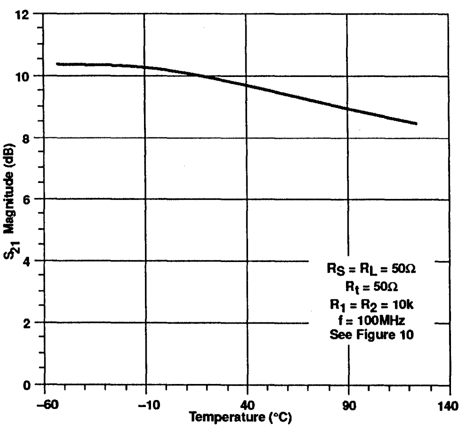
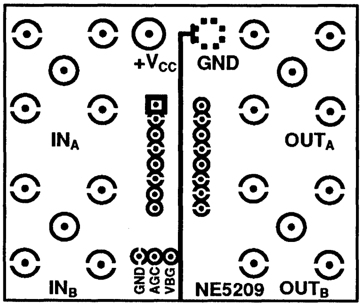
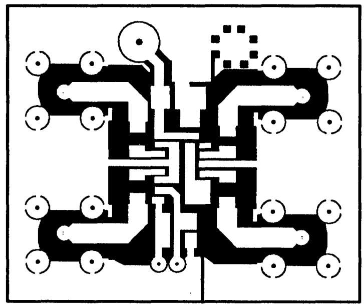


Figure 32. Fixed Gain vs Temperature



TOP VIEW - COMPONENT SIDE

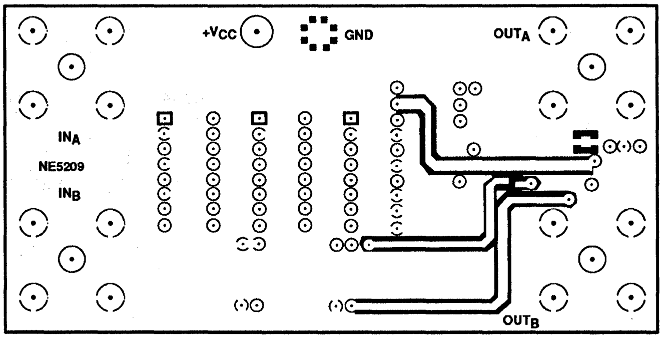


TOP VIEW - SOLDER SIDE

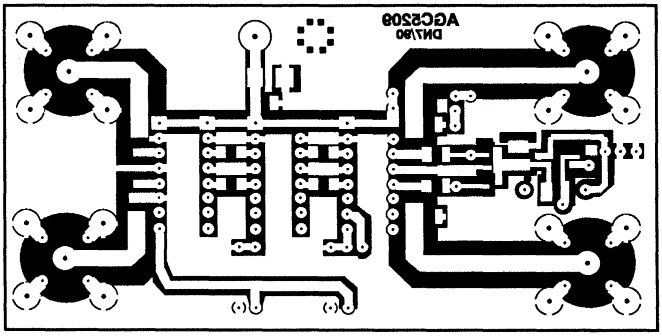
VGA AC Evaluation Board Layout

Wideband variable gain amplifier

NE/SA5209

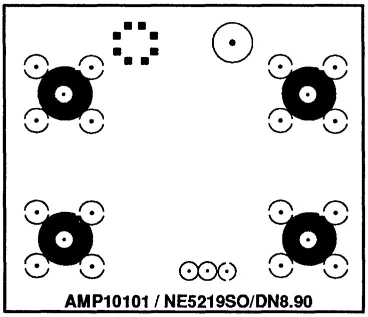


TOP VIEW - COMPONENT SIDE

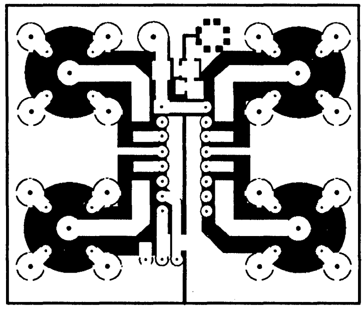


TOP VIEW - SOLDER SIDE

AGC Configuration Using Cascaded NE5209s - Layout



TOP VIEW - COMPONENT SIDE



TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout (DIP Package)

Wideband variable gain amplifier

NE/SA5219

DESCRIPTION

The NE5219 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5219 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5219 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

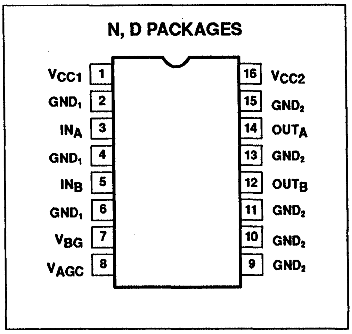
FEATURES

- 700MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5219D
16-Pin Plastic DIP	0 to +70°C	NE5219N
16-Pin Plastic SO	-40 to +85°C	SA5219D
16-Pin Plastic DIP	-40 to +85°C	SA5219N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	$V_{CC1} = V_{CC2}$ = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, $V_{CC1} = V_{CC2}$ = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	36	43	50	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	16	19	22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	22	25	28	dB
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.8	1.2	1.6	kΩ
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	35	60	80	Ω
V_{OS}	Output offset voltage (output referred)			±20	±150	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
PSRR	Output offset supply rejection ratio		18	45		dB
V_{BG}	Bandgap reference voltage	$4.5V<V_{CC}<7V$ R_{BG} = 10kΩ	1.2	1.32	1.45	V
R_{BG}	Bandgap loading		2	10		kΩ
V_{AGC}	AGC DC control voltage range			0-1.3		V
I_{BAGC}	AGC pin DC bias current	$0V<V_{AGC}<1.3V$		-0.7	-6	μA

AC ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $V_{CC1} = V_{CC2} = +5.0V$, $V_{AGC} = 1.0V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
BW	-3dB bandwidth			700		MHz
GF	Gain flatness	DC - 500MHz		±0.4		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[1]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended)	$R_L = 50\Omega$		400		mV_{P-P}
	for linear operation[1]	$R_L = 1k\Omega$		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	$R_S = 50\Omega$, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	$R_L = 50\Omega$		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:
1. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5219 APPLICATIONS

The NE5219 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5219 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5219 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5219 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5219 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5219. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5219 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5219 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5219 is shown in Figure 2. Three NE5219s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5219s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5219s will give a dynamic range in excess of 60dB.

The NE5219 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

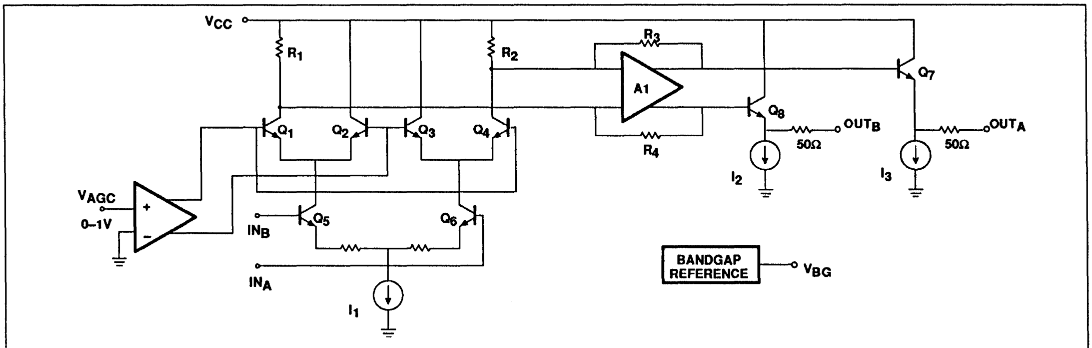


Figure 1. Equivalent Schematic of the VGA

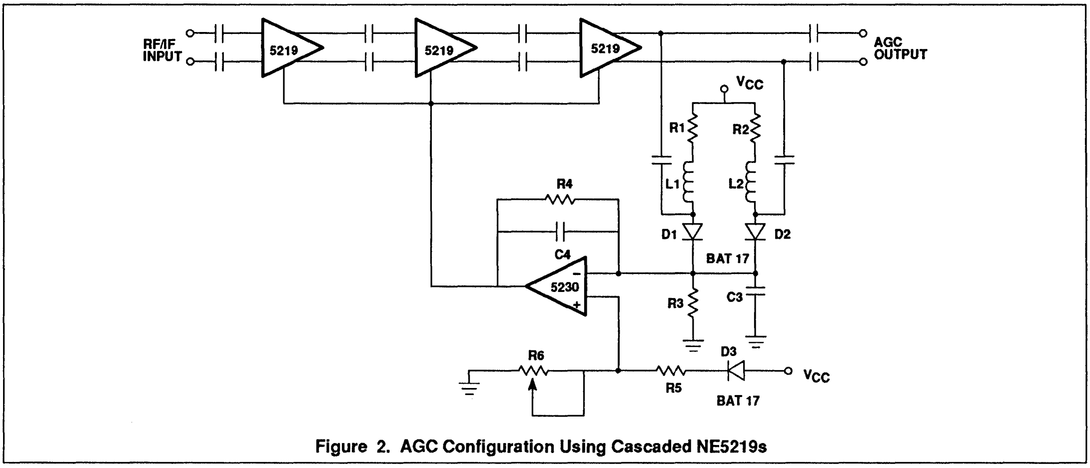


Figure 2. AGC Configuration Using Cascaded NE5219s

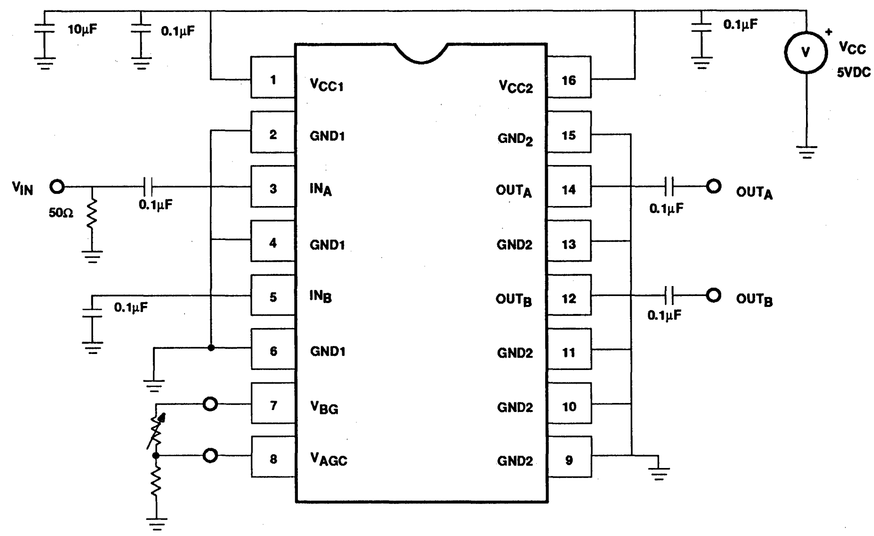
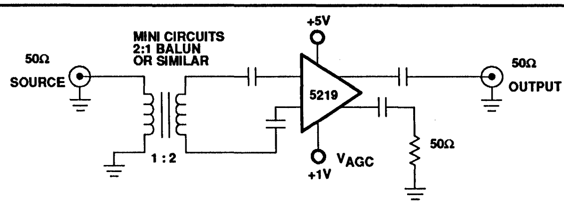
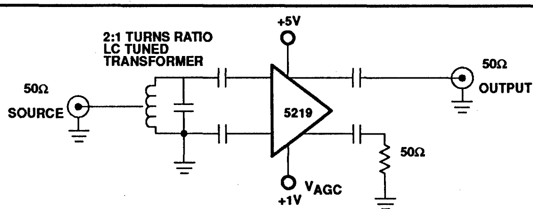


Figure 3. VGA AC Evaluation Board



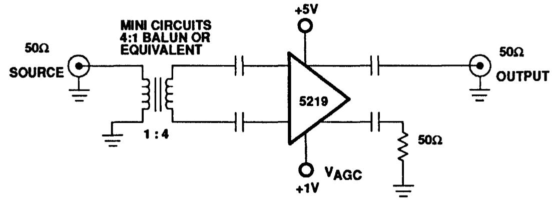
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



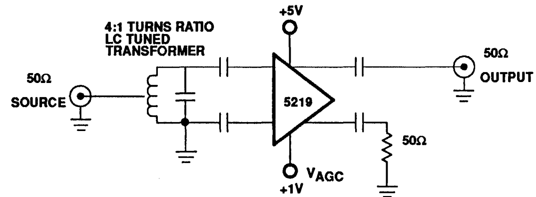
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization



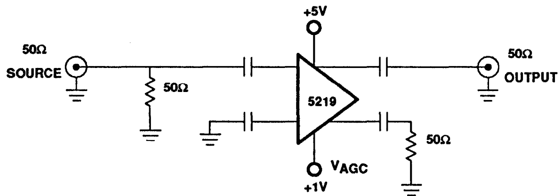
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 6. Broadband Gain Optimization



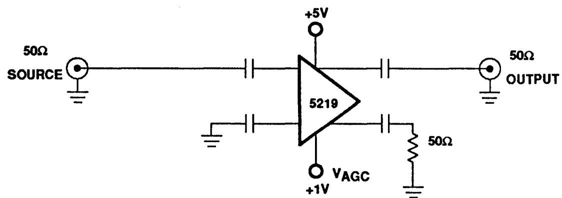
This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 7. Narrowband Gain Optimization



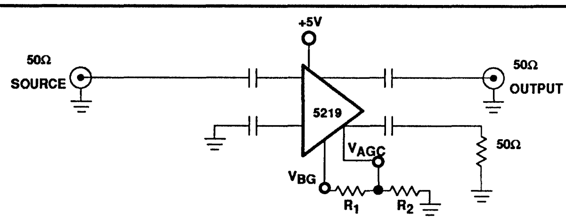
The noise figure of this configuration will be approximately 15dB.

Figure 8. Simple Amplifier Configuration



With the 50Ω source left unterminated, the noise figure is 9dB.

Figure 9 Unterminated Configuration



Gain = 19dB + $20\log_{10} V_{AGC}$

where $V_{AGC} = \left[\frac{R_2}{R_1 + R_2} V_{BG}\right]$

and is in units of Volts, for $V_{AGC} \leq 1V$

Figure 10. User-Programmable Fixed Gain Block

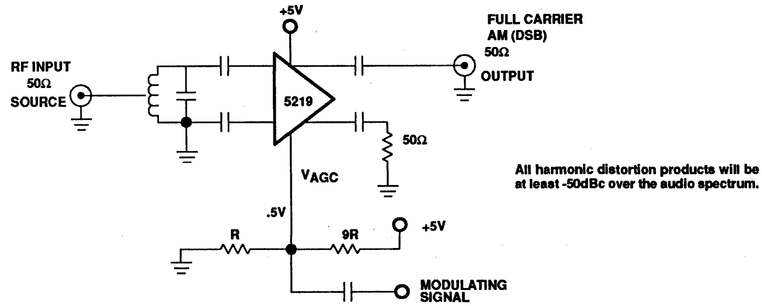
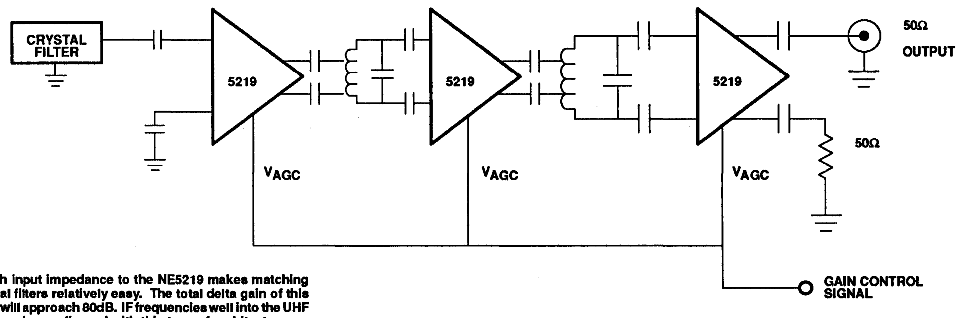


Figure 11. AM Modulator



The high input impedance to the NE5219 makes matching to crystal filters relatively easy. The total delta gain of this system will approach 80dB. IF frequencies well into the UHF region can be configured with this type of architecture.

Figure 12. Receiver AGC IF Chain

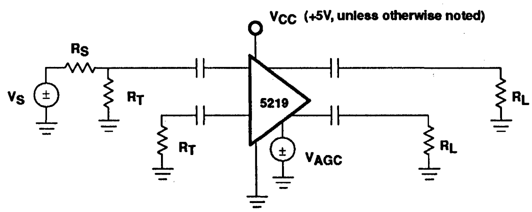


Figure 13. Test Set-up 1 (Used for all Graphs)

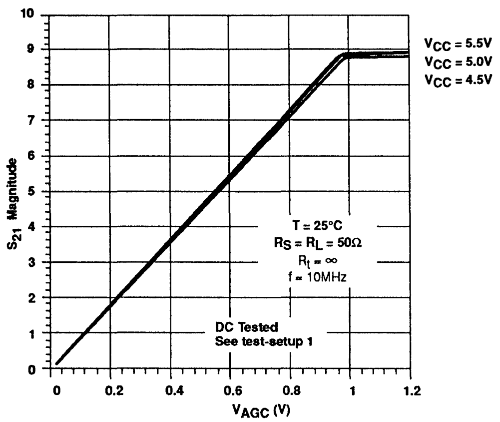


Figure 14. Gain vs V_{AGC} and V_{CC}

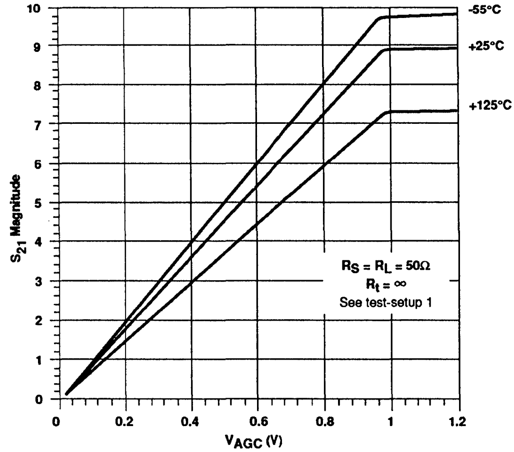


Figure 15. Insertion Gain vs V_{AGC} and Temperature

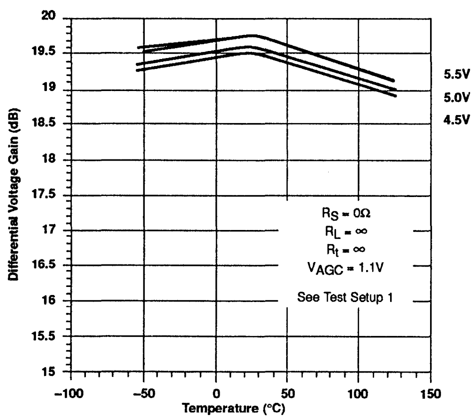


Figure 16. Voltage Gain vs Temperature and V_{CC}

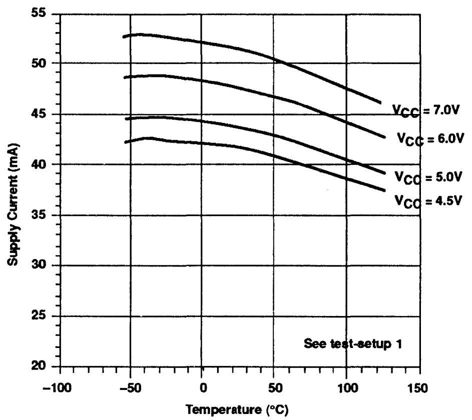


Figure 17. Supply Current vs Temperature and V_{CC}

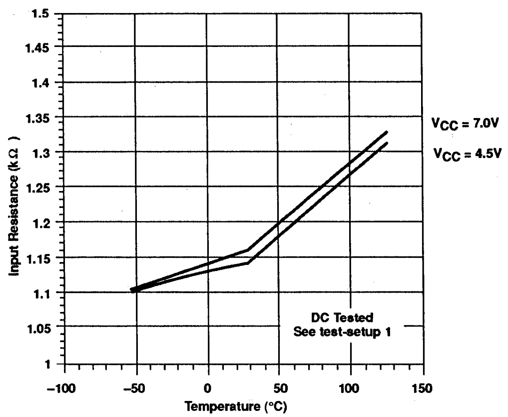


Figure 18. Input Resistance vs Temperature

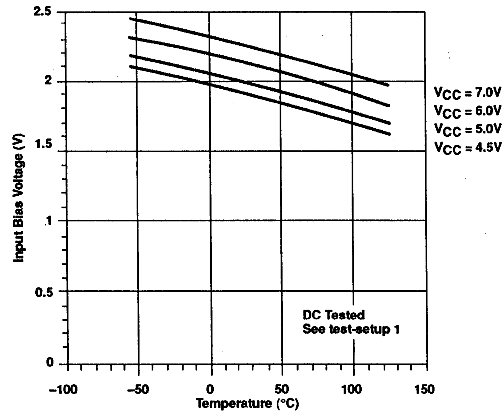


Figure 19. Input Bias Voltage vs Temperature

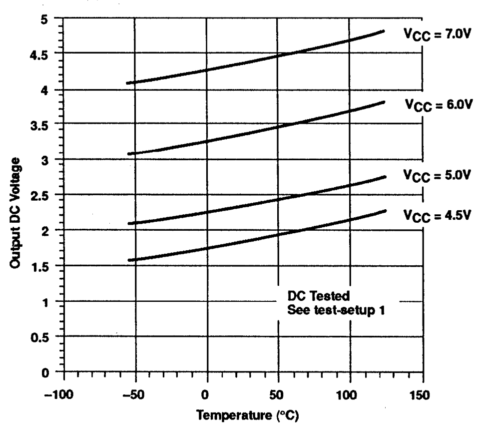


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

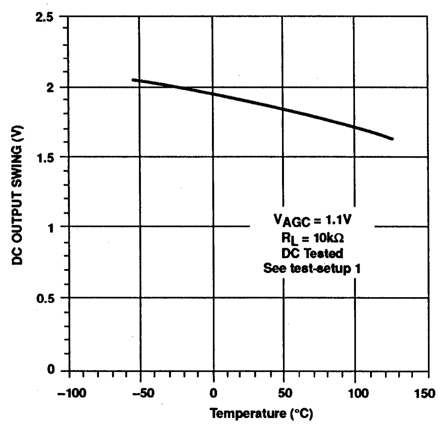


Figure 21. DC Output Swing vs Temperature

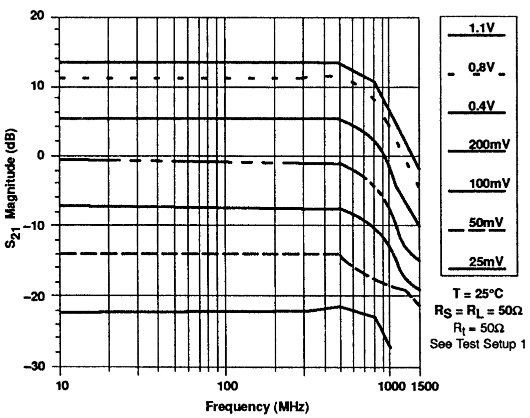


Figure 22. Insertion Gain vs Frequency and V_{AGC}

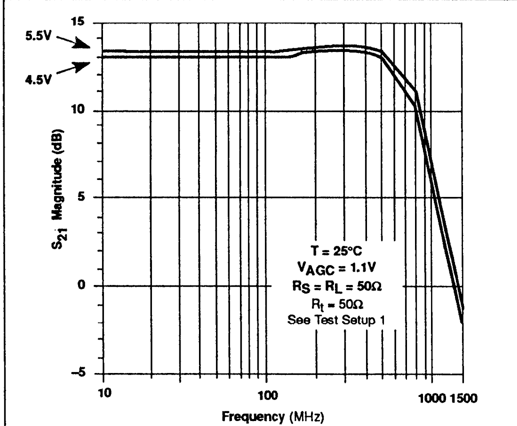


Figure 23. Insertion Gain vs Frequency and V_{CC}

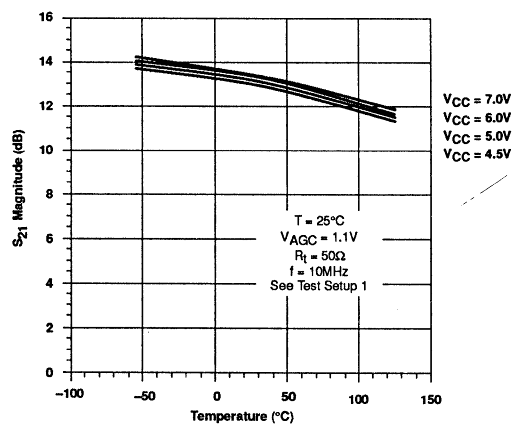


Figure 24. Insertion Gain vs Temperature and V_{CC}

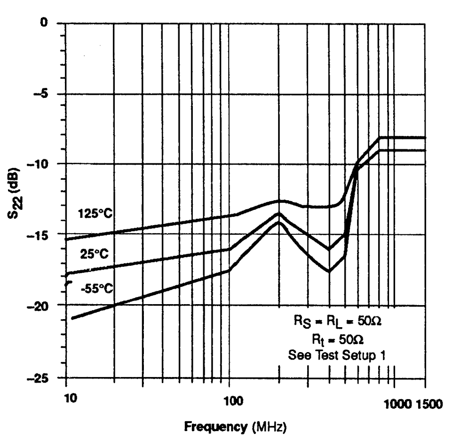


Figure 25. Output Return Loss vs Frequency

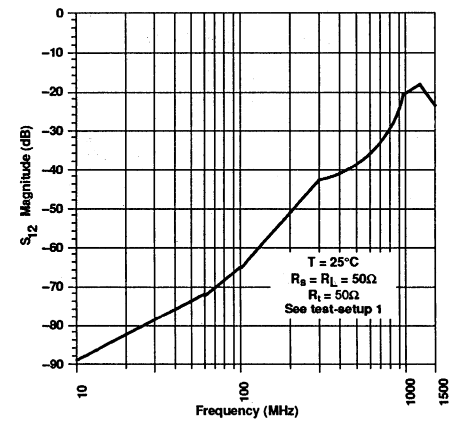


Figure 26. Reverse Isolation vs Frequency

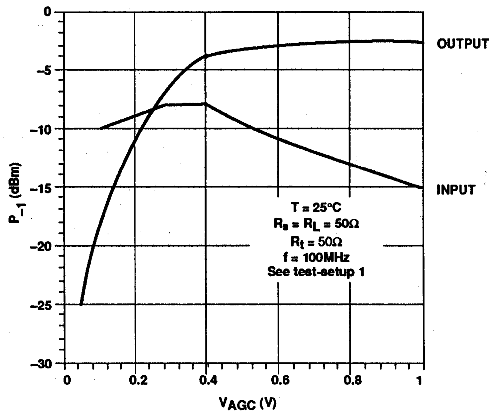


Figure 27. 1dB Gain Compression vs V_{AGC}

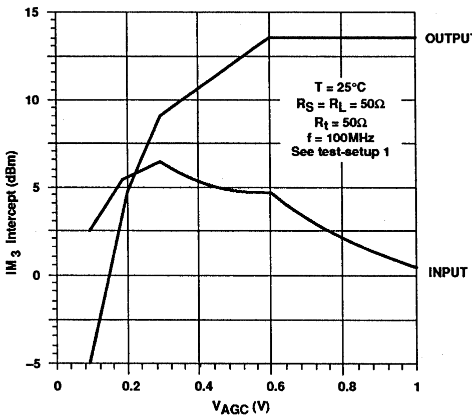


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

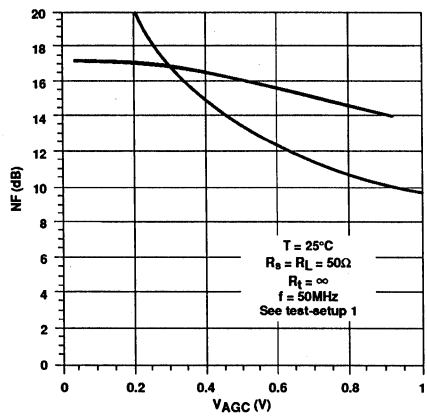


Figure 29. Noise Figure vs V_{AGC}

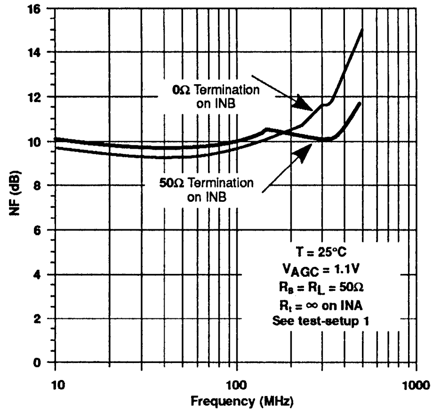


Figure 30. Noise Figure vs Frequency

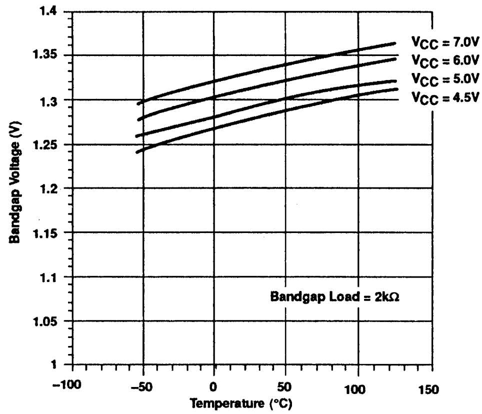


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

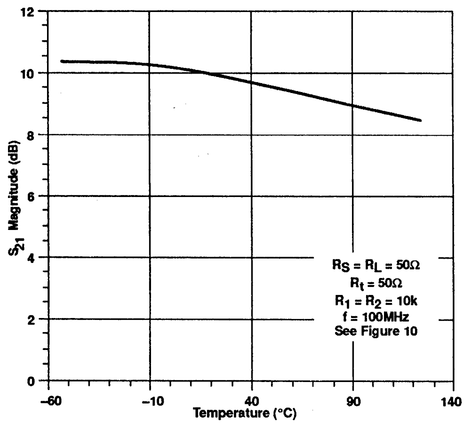
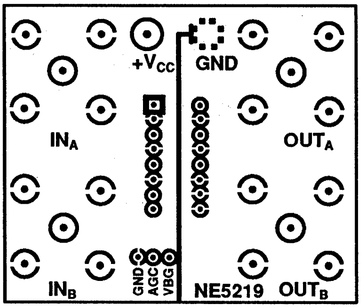
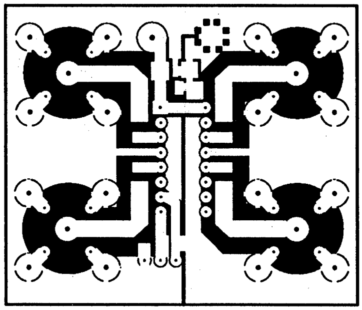


Figure 32. Fixed Gain vs Temperature

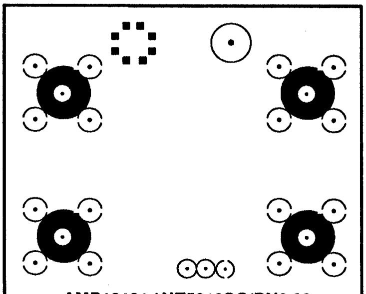


TOP VIEW - COMPONENT SIDE

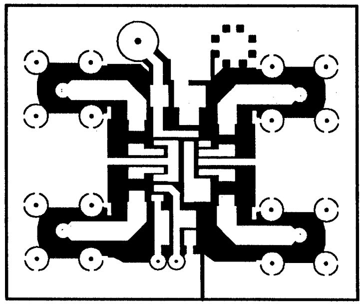


TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout (DIP Package)



BOTTOM VIEW - D Package



TOP VIEW - D Package

VGA AC Evaluation Board Layout (SO Package)

Matched quad high-performance low-voltage operational amplifier

NE/SA5234

DESCRIPTION

The NE/SA5234 is a matched, low voltage, high performance quad operational amplifier. Among its unique input and output characteristics is the capability for both input and output rail-to-rail operation, particularly critical in low voltage applications. The output swings to less than 50mV of both rails across the entire power supply range. The NE/SA5234 is capable of delivering 5.5V peak-to-peak across a 600Ω load and will typically draw only 700μA per amplifier. The bandwidth is 2.5MHz and the 1% settling time is 1.4μs.

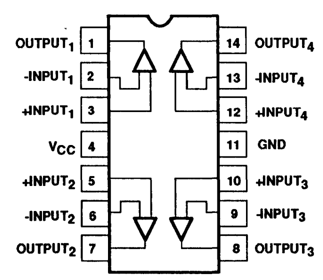
FEATURES

- Wide common-mode input voltage range: 250mV beyond both rails
- Output swing within 50mV of both rails
- Functionality to 1.8V typical
- Low current consumption: 700μA per amplifier
- ±15mA output current capability
- Unity gain bandwidth: 2.5MHz
- Slew rate: 0.8V/μs
- Low noise: 25nV/√Hz
- Electrostatic discharge protection
- Short-circuit protection
- Output inversion prevention

APPLICATIONS

- Automotive electronics
- Signal conditioning and sensing amplification
- Portable instrumentation
  - Test and measurement
  - Medical monitors and diagnostics
  - Remote meters
- Audio equipment
- Security systems
- Communications
  - Pagers
  - Cellular telephone
  - LAN
  - 5V Datacom bus
- Error amplifier in motor drives
- Transducer buffer amplifier

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE5234D
14-Pin Plastic DIP	0 to +70°C	NE5234N
14-Pin Plastic SO	-40 to +85°C	SA5234D
14-Pin Plastic DIP	-40 to +85°C	SA5234N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
V_{ESD}	ESD protection voltage at any pin[5] human body model robot model	 2000 200	 V V
V_S	Dual supply voltage	±3.5	V
V_{DP}	Voltage at any device pin[1]	$V_S \pm 0.5$	V
I_{DP}	Current into any device pin[1]	±50	mA
V_{IN}	Differential input voltage[2]	0.5	V
V_{CM}	Common-mode input voltage (positive)	$V_{CC} + 0.5$	V
V_{CM}	Common-mode input voltage (negative)	$V_{EE} - 0.5$	V
P_D	Power dissipation[3]	500	mW
T_J	Operating junction temperature[3]	+150	°C
V_{SC}	Supply voltage allowing indefinite output short circuit to either rail[3,4]	7	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C
θ_{JA}	Thermal impedance 14 pin Plastic DIP 14 pin Plastic SO	 80 115	 °C/W °C/W

NOTES:
1. Each pin is protected by ESD diodes. The voltage at any pin is limited by the ESD diodes.
2. The differential input of each amplifier is limited by two internal diodes, connected in parallel and opposite to each other. For more differential input range, use differential resistors in series with the input pins.
3. The maximum operating junction temperature is +150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions. Derates above +25°C: F package at 6.7mW/°C; N package at 9.5mW/°C; D package at 6.25mW/°C.
4. Simultaneous short circuits of two or more amplifiers to the positive or negative rail can exceed the power dissipation ratings and cause eventual destruction of the device.
5. Guaranteed by design.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	+2 to +5.5	V
V_S	Dual supply voltage	±1 to ±2.75	V
V_{CM}	Common-mode input voltage (positive)	$V_{CC} + 0.25$	V
V_{CM}	Common-mode input voltage (negative)	$V_{EE} - 0.25$	V
T_A	Temperature NE	 0 to +70	 °C
	SA	-40 to +85	°C

DC ELECTRICAL CHARACTERISTICS V_{CC} = 2 to 5.5V, V_{EE} = 0V, T_A = 25°C; $V_{EE} < V_{CM} < V_{CC}$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_{CC} = 5.5V		2.8	3.5		2.8	3.5	mA
		V_{CC} = 5.5V over full temperature range		3.0	4.2		3.2	4.3	mA
V_{OS}	Offset voltage			±0.2	±4		±0.2	±4	mV
		Over full temperature range		±0.4	±5		±0.6	±5	mV
$\Delta V_{OS}/\Delta T$	Offset voltage drift with temperature			4			4		μV/°C
ΔV_{OS}	Offset voltage difference between any amplifiers in			0.4	3		0.4	3	mV
	the same package at the common mode level[1]	Over full temperature range		0.8	4		1.2	4	mV
I_{OS}	Offset current			±3	±20		±3	±30	nA
		Over full temperature range		±4	±30		±6	±60	nA
$\Delta I_{OS}/\Delta T$	Offset current drift with temperature			0.02	±.3		0.03	±.3	nA/°C
I_B	Input bias current[1]	$V_{EE} < V_{CM} < V_{EE}$ +0.5V	-150	-90		-150	-90		nA
		Over full temperature range	-175	-100		-200	-150		nA
		V_{EE} +1V < $V_{CM} < V_{CC}$		25	70		25	75	nA
		Over full temperature range		35	100		35	120	nA
$\Delta I_B/\Delta T$	Input bias current drift with temperature			0.5			0.5		nA/°C
ΔI_B	Input bias current difference	$V_{EE} < V_{CM} < V_{EE}$ +0.5V		10	30		10	30	nA
	between any amplifier in the same package at the same	Over full temperature range		25	50		50	70	nA
	common mode level.	V_{EE} +1V < $V_{CM} < V_{CC}$		5	20		5	20	nA
		Over full temperature range		15	30		25	50	nA
V_{CM}	Common-mode input range	$V_{OS} \leq$ 6mV	V_{EE}-0.25		V_{CC}+0.25	V_{EE}-0.25		V_{CC}+0.25	V
		$V_{OS} \leq$ 6mV over full temperature range	V_{EE}-0.1		V_{CC}+0.1	V_{EE}-0.1		V_{CC}+0.1	V
CMRR	Common-mode rejection ratio, small signal	$V_{EE} < V_{CM} < V_{EE}$+0.5V, V_{EE}+1V < $V_{CM} < V_{CC}$	90	100		90	100		dB
		Over full temperature range	90	100		80	90		dB
	Common-mode rejection ratio, large signal	$V_{EE} < V_{CM} < V_{CC}$		100			100		dB
		Over full temperature range		90			90		dB
PSRR	Power supply rejection ratio	$V_{EE} < V_{CM} < V_{CC}$	80	100		80	100		dB
		Over full temperature range	80	90		80	90		dB

DC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE5234 MIN	NE5234 TYP	NE5234 MAX	SA5234 MIN	SA5234 TYP	SA5234 MAX	UNITS
I_L	Peak load current, sink and source		10	15		10	15		mA
		Over full temperature range	5	10		5	10		mA
A_{VOL}	Open-loop voltage gain		90	110		90	110		dB
		Over full temperature range		90			90		dB
V_{OUT}	Output voltage swing	I_{PEAK} = 0.1mA	V_{EE}+0.05		V_{CC}-0.05	V_{EE}+0.1		V_{CC}-0.1	V
		I_{PEAK} = 10mA	V_{EE}+0.25		V_{CC}-0.25	V_{EE}+0.25		V_{CC}-0.25	V
		I_{PEAK} = 5mA over full temp range	V_{EE}+0.22		V_{CC}-0.2	V_{EE}+0.2		V_{CC}-0.2	V
	Output voltage swing for V_{CC} = 2.75V, V_{EE} = -2.75V	$R_L = 2k\Omega$	V_{EE}+0.2		V_{CC}-0.2	V_{EE}+0.2		V_{CC}-0.2	V
		$R_L = 600\Omega$,	V_{EE}+0.25		V_{CC}-0.25	V_{EE}+0.25		V_{CC}-0.25	V

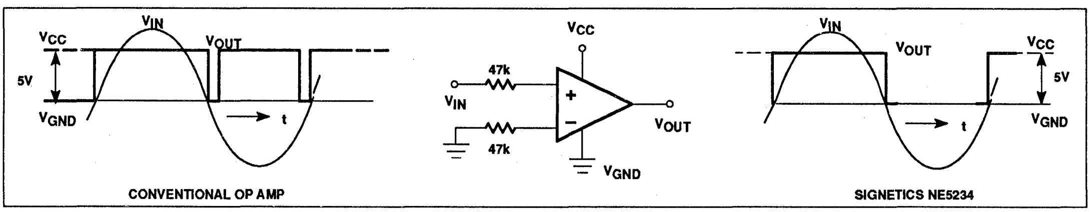
NOTES:

1. These parameters are measured for $V_{EE} < V_{CM} < V_{EE}+.5V$ and for $V_{EE}+1V < V_{CM} < V_{CC}$. By design these parameters are intermediate for common mode ranges between the measured regions.

AC ELECTRICAL CHARACTERISTICS $T_A = +25°C$; V_{CC} = 2 to 5.5V; R_L = 10k; C_L = 100pF; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE5234 MIN	NE5234 TYP	NE5234 MAX	SA/SE5234 MIN	SA/SE5234 TYP	SA/SE5234 MAX	UNITS
SR	Slew rate	Over full temperature range	.5	0.8		.5	0.8		V/µs
BW	Unity gain bandwidth: -3dB	Over full temperature range	2	2.5	4.0	2	2.5	4.0	MHz
θ_M	Phase Margin	C_L = 50pF		55			55		deg
t_S	1% settling time	A_V = 1, 1V step		1.4			1.4		µs
V_N	Input referred voltage noise	$A_V = 1$, $R_S = 0\Omega$, at 1kHz		25			25		nV/ $Hz^{1/2}$
THD	Total harmonic distortion	10kHz, $1V_{P-P}$, A_V = 1		0.1			0.1		%

OUTPUT INVERSION PREVENTION



Using the NE/SA5234 amplifier AN1651

Author: L. Hadley

I. SUMMARY

The NE/SA5234 is a unique low-voltage quad operational amplifier specifically designed to operate in a broadly diverse environment. It is an enhanced pin-for-pin replacement for the LM324 category of devices. Supply conditions can range from 1.8V to 6.0V with a resultant current drain of 2.8mA,-700μA per op amp.

Most notable are the input and output dynamic range characteristics of the individual op amps. The common-mode input voltage can actually exceed the positive and negative supply rails by 250mV with no danger of output latching or polarity reversal. In addition, the output of each op amp will swing to within 50mV of the supply rails over the full supply range.

The frequency related characteristics are also above average for low voltage devices in this class. Internal unity gain compensation makes the NE5234 very resistant to any tendency to oscillate in low closed-loop gain configurations. Even so, a unity-gain bandwidth of 2.5MHz is retained. Slew rate is 0.8V/μs and each op amp will settle to a 1% of nominal level within 1.4μs.

II. DETAILED DESCRIPTION

Input Stage

The input differential amplifier consists of a compound transistor structure of parallel NPN and PNP transistors which account for the unique over-drive characteristics of the NE5234. Referring to Figure 1, it is seen that the NPN pair, Q1 and Q2, allow the input to operate in the common-mode input voltage range of 1V above V_{EE}. This region is designated the N-mode region in Figure 3a. Operation in the common-mode range below 1V transfers the input stage into the P-mode of operation.

In the N-mode operating condition, collector current from Q1 and Q2 is summed in the output emitter node of Q10 and Q12 respectively. Q1's base is the non-inverting input and Q2's base the inverting input node for the amplifier.

Linear operation between the two modes is governed by a current steering circuit consisting of Q5,6 and 7 in conjunction with voltage reference VB1. Operation in the N-region of the common-mode range will automatically cause Q5 to transfer the IB1 current source to Q7 and the NPN transistor pair Q1 and Q2. Operation below the 1V level at the inputs allows the current from IB1 to be fed directly to Q3 and Q4 emitters giving them priority in processing the signal and linearizing their transfer function. (The sum of the NPN and PNP input pair currents remain constant.)

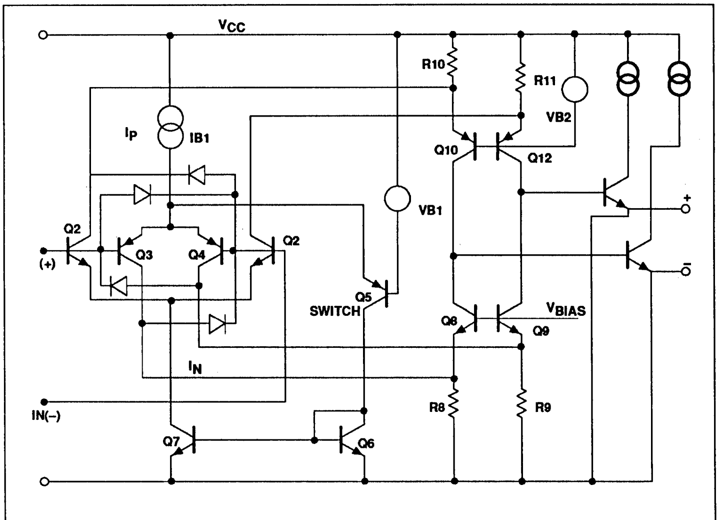


Figure 1. NE5234 Input Stage

Operation in the common-mode range near the positive supply rail would normally cause the input stage NPN transistor's base collector junction to become forward biased (base current flow directly to the collector circuit) reversing the collector current flow direction. In a conventional op amp, this would have the adverse effect of reversing the output signal polarity as the operating region is traversed by the input signal. (see Figure 2)

To prevent this from occurring, large geometry diode-connected transistors are cross-connected to the opposite NPN collector, (Q1, Q2). This current, in turn, is summed at the emitter of Q12 pulling it above the V_{CC} rail voltage and preventing polarity reversal. The inverse condition occurs when Q2 is driven above the positive rail, with Q10 emitter being pulled up and signal polarity preserved. (See Figure 1)

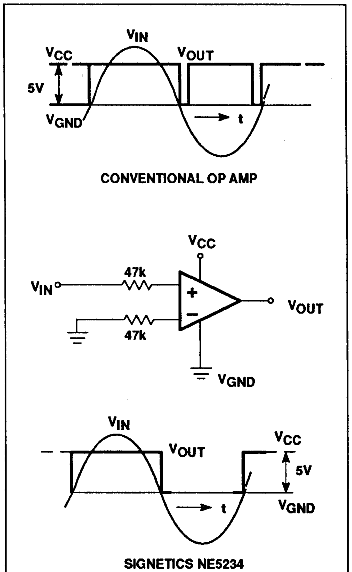
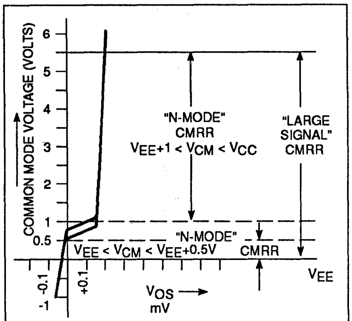


Figure 2. Output Inversion Protection



NE5234 Common-Mode Operating Regions

Figure 3.

For negative going input signals, which drive the inputs toward the V_{EE} rail and below, another set of diode-connected transistors come into operation. These steer the current from the input into Q8 or Q9 emitter circuits again preventing the reversal effect.

Figure 3 shows graphically how the N and P mode transitions relate to the common-mode input voltage and the offset voltage V_{OS}.

Intermediate Amplifier and Output Stage (Figure 4)

The intermediate stage is isolated from the input amplifier by emitter followers to prevent any adverse loading effect. This stage adds gain to the over all amplifier and translates levels for the following class-AB current-control driver. Note that I_2 is the inverting input and I_1 the non-inverting input. The output is taken from multiple collectors on the non-inverting side and provides matching for the following stage.

Class-AB control of the output stage is achieved by Q61 and Q62 with the associated output current regulators. These act to monitor the smallest current of the non-load supporting output transistor to keep it in conduction. Thus, neither Q71 or Q81 is allowed to cutoff but is forced to remain in the proper Class-AB region.

Overload protection is provided by monitor circuits consisting of R76-D2 for sinking and R86-D3 for sourcing condition at the output. When the output current, source or sink, reaches 15 milliamperes, drive current to the stage is shunted away from current sources IB6 or IB9 reducing base current to driver transistors Q72 and Q82 respectively.

The prevention of saturation in the output stage is achieved by saturation detectors Q78 and Q88. When either Q71 or Q81 approaches saturation, current is shunted away from the driver transistors, Q72 or Q83 respectively.

III. CHARACTERISTICS

Internal Frequency Compensation

The use of nested Miller capacitors C2 through C6, in the intermediate and output sections, provides the overall frequency compensation for the amplifier. The dominant pole setting capacitor, C2, provides a constant 6dB/octave roll-off to below the unity gain frequency of 2.5MHz. Figure 5 shows the measured frequency response plot for various values of closed-loop gains.

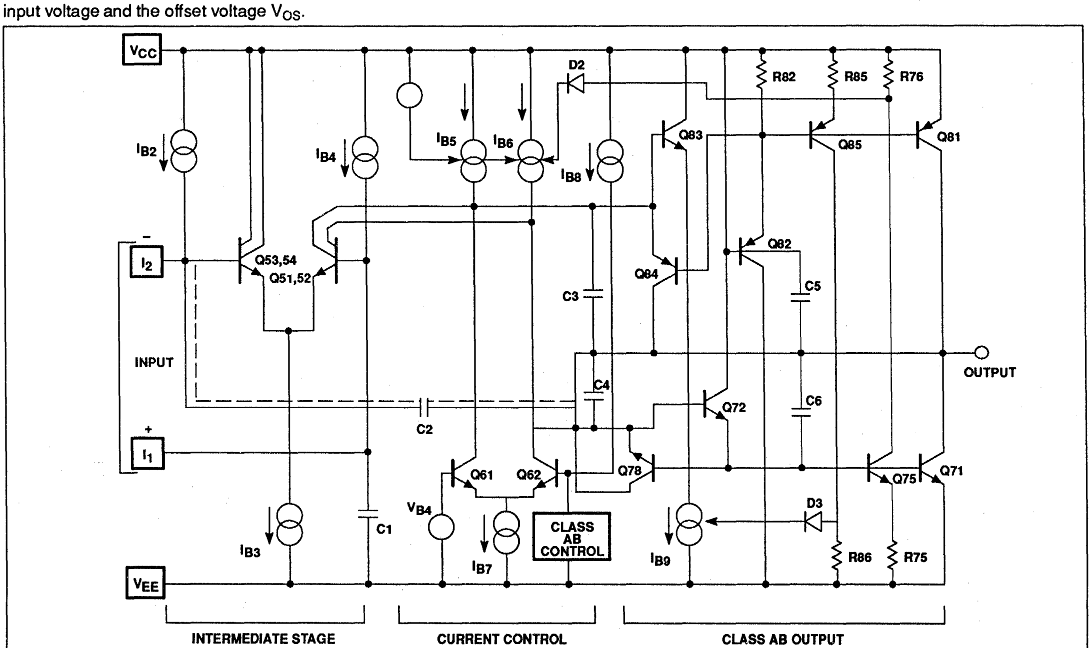


Figure 4.

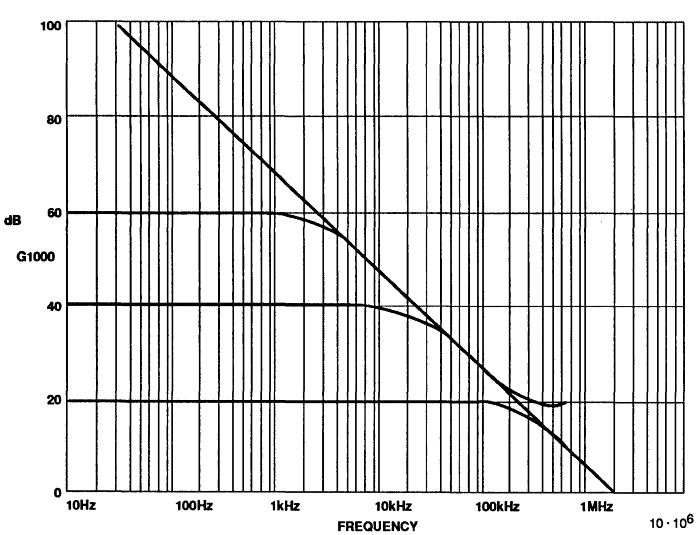


Figure 5. NE5234 Closed Loop Gain vs Frequency

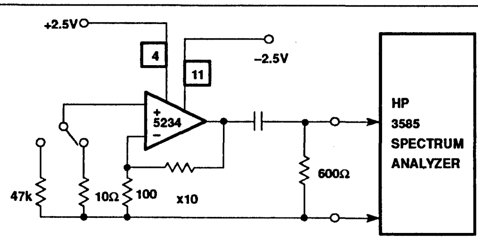


Figure 6. Test Circuit

IV. NOISE REFERRED TO THE INPUT

The typical spectral voltage noise referred to each of the op amps in the NE/SA5234 is specified to be 25nV/√Hz. Current noise is not specified. In the interest of providing a balance of information on the device parameters, a small sample of the standard NE5234s, were tested for input noise current. While this data does not represent a specification, it will give the designer a ball park figure to work with when beginning a particular design with the device. For completeness I have provided the corresponding spectral noise voltage data for the same sample. The data was taken using an HP3585A spectrum analyzer which has the capability of reading noise in nV/√Hz.

The test circuit is shown in Figure 6. As is typical for such measurements the amplifier under test is terminated at its input first with a very low resistance, for the voltage noise reading, followed by the same test with a high value of resistance to register the effect of current noise. The amplifier is set to a non-inverting closed-loop gain of 20dB. Dual supply operation was chosen to allow direct termination of the input resistors to ground.

The measurements were made over the range from 200Hz to 2kHz. Each sample is measured at 200Hz, 500Hz, 1kHz and 2kHz. The data is averaged for each frequency and then the small sample distribution is derived statistically giving the standard deviation relative to the mean.

Referring to the graph in Figure 7a, the equivalent voltage noise is seen to average 18 nV/√Hz. The 95% confidence interval is determined to be approximately one nV/√Hz. The majority of the errors which contribute to this measurement are due to the thermal noise of the parallel combination of the feedback resistor network, in addition to the 10Ω termination resistor on the non-inverting input. At 300° Kelvin a 10Ω resistor generates 0.4 nV/√Hz and the feedback network's equivalent resistance of 90Ω generates 1.2nV/√Hz. Their order-of-magnitude difference from the main noise sources allows them to be neglected in the overall calculation of total stage noise.

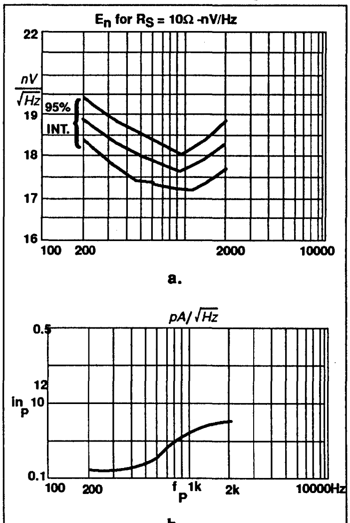


Figure 7.

Noise current is measured across a 47kΩ resistor and averaged in the same manner. The thermal noise generated by this large resistance is not insignificant. At room temperature it is 28nV/√Hz and must be subtracted from the total noise as measured at the output of the op amp in order to arrive at the equivalent current generated noise voltage. Figure 7b shows the derived current noise distribution for the small sample of 10 NE5234 devices. The result shows that noise current in the 200Hz to 2kHz frequency is typically 0.2pA/√Hz. The 1/f region was not determined for either current or voltage noise.

V. GUIDE LINES FOR MINIMIZING NOISE

When designing a circuit where noise must be kept to a minimum, the source resistances should be kept low to limit thermally generated degradation in the overall output response. Orders-of-magnitude should be kept in mind when evaluating noise performance of a particular circuit or in planning a new design. For instance, a transducer with a 10kΩ source resistance will generate 2µV of RMS noise over a 20kHz bandwidth. Using the graphical data above, total noise from a gain stage may be calculated.-

Amplifier Noise Voltage — EQ 1.

$$25nV/\sqrt{Hz}\cdot\sqrt{BW} = 3.5\mu V_{RMS}$$
$$BW = 10kHz$$

Noise from source 10kΩ Resistance-

Noise Voltage from source resistance — EQ 2.

$$14nV/\sqrt{Hz}\cdot\sqrt{BW} = 20\mu V_{RMS}$$

Current generated noise — EQ 3.

$$0.2pA/\sqrt{Hz}\cdot 10^3\cdot\sqrt{BW} = 0.28\mu V_{RMS}$$

The total noise is the root-of-the-sum-of-the-squares of the individual noise voltages-

EQ 4.

$$En = \sqrt{(3.5)^2 + (2.0)^2 + (0.28)^2}$$
$$= 4.04\mu V_{RMS}$$

To determine the signal-to-noise ratio of the stage we must first choose a stage gain, make it 40dB, and a signal voltage magnitude from the transducer which we will set at $10mV_{RMS}$. The resulting signal-to-noise ratio at the output of this stage is determined by first multiplying the gain times the signal which gives $1V_{RMS}$ with a resultant noise of $400\mu V_{RMS}$. The signal-to-noise ratio is calculated as

EQ 5.

$$S/N \quad 20\log_{10}(1.0/4x10^{-4}) = 68dB$$

This is quite adequate for good quality audio applications.

Next, assume that the bandwidth is cut to 3.0kHz with an input of $1mV_{RMS}$. The stage gain is kept at 40dB. The total noise is calculated below. The RMS noise is modified by the ratio of the root of the noise channel bandwidths.

EQ 6.

$$\left[\frac{\sqrt{3x10^3}}{\sqrt{20x10^3}}\right]\cdot En = 1.6\mu V_{RMS}$$

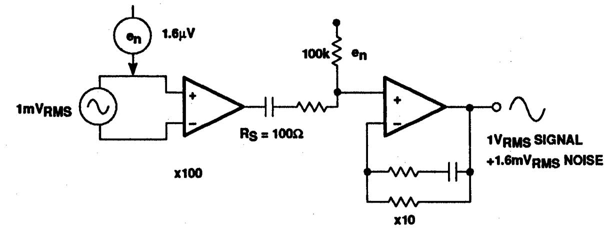


Figure 8.

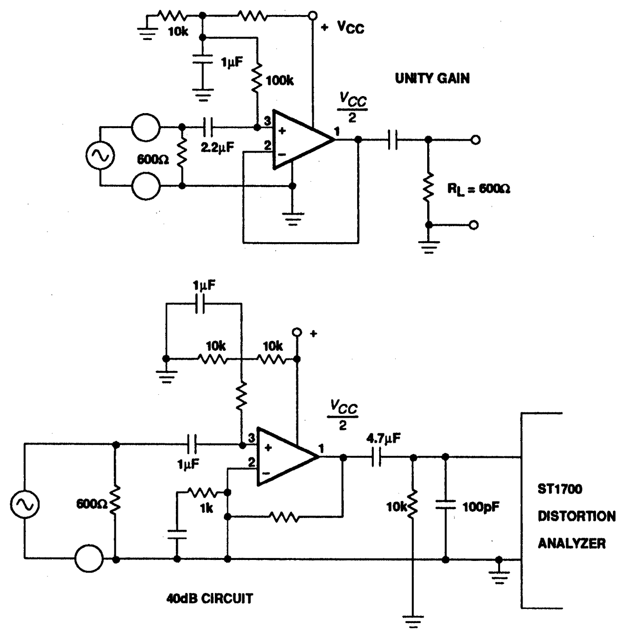


Figure 9.

Amplified Noise = $160\mu V_{RMS}$

EQ 7.

$$S/N \quad 20\log_{10}\left[\frac{100x10^{-3}}{1.6x10^{-4}}\right]$$
$$= 56dB$$

A 56dB S/N will provide superior voice channel communications .

VI. MULTIPLE STAGE CONSIDERATIONS

Since multiple noise generators are non-coherent, their total effect is the root-of-the-sum-of-the-squares of the various noise generators at a given amplifier input. This makes orders-of-magnitude lower noise sources less important than the higher magnitude source. Therefore, when considering the combined signal-to-noise of multiple stages of gain, the first stage in a chain dominates making its design parameters the most critical. For this reason it is good practice to make the preamp stage gain as high as practical to boost signal levels to the second stage allowing at least an order-of-magnitude above the second-stage noise. For instance, a signal input which exceeds the input noise of the following stage by a factor of 10:1 will only be degraded by 0.5% or -46dB, neglecting the first-stage noise. If we use the preceding example with a first-stage output signal of

100mV$_{RMS}$ and a 56dB S/N, and an output noise of 0.16mV. Following this with a 10kHz band limited gain-of-10 second-stage, with a 100kΩ noise source at the non-inverting input, the combined S/N is calculated as follows: (assume a 100Ω source resistance from amplifier #1)

The Second stage output noise is:

EQ 8.

$$\left[\sqrt{(0.163x10^{-3})^2+\left(\sqrt{4KT\cdot 100\cdot 10,000}\right)^2}\right]\cdot 10$$
$$= 1.6mV$$

$$K = Boltzman'sConstant = 1.38x10^{-23}\frac{Joule}{DegKelvin}$$

$$T = 300^{o}K\ ;\ BW = 10kHz$$

The amplified output signal = 1V$_{RMS}$

EQ 10.

$$S/N = 20\log_{10}\left(\frac{1}{1.6x10^{-3}}\right)$$
$$= 56dB$$

Note that there is no effect from the second-stage thermally generated resistor noise due to the dominating effect of the first-stage amplified noise being much greater than the input noise of the second-stage. In addition the equivalent noise resistance of the second-stage is essentially the output resistance of the first-stage plus any series resistance used in coupling the two. This is the parallel combination of source resistance with input terminating or biasing resistance.

VII. LOW HARMONIC DISTORTION

The NE/SA5234 is extremely well adapted to reducing harmonic distortion as it relates to signal level and head room in audio and instrumentation circuits. Its unique internal design limits overdrive induced distortion to a level much below that experienced with other low voltage devices. As will be shown, the device is capable of operating over a wide supply range without causing the typical clipping distortion prevalent in companion operational amplifiers of this class.

A series of tests are shown to allow you to see just how resistant this device is to generating clipping distortion. Two different gain configurations were chosen to demonstrate this particular feature: unity gain non-inverting and 40dB non-inverting. The test set-up was as shown in Figure 9. The Harmonic Distortion analyzer used to make the measurements was a Storage

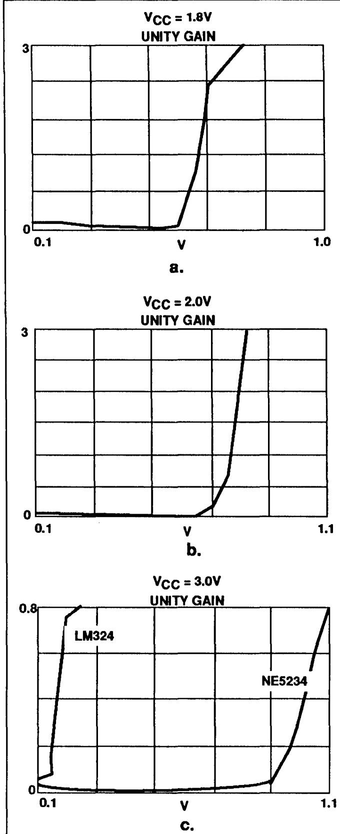


Figure 10.

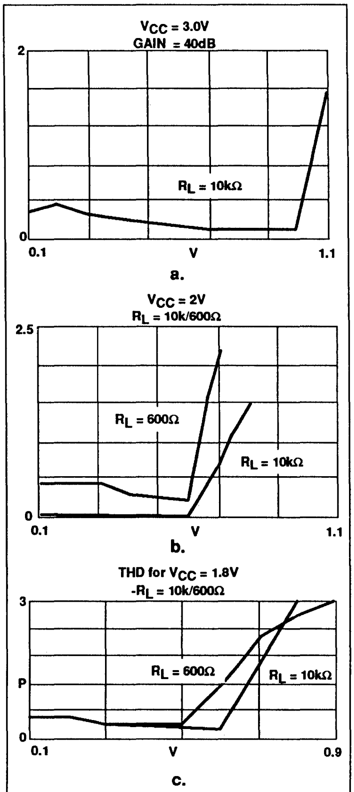


Figure 11.

Technology ST1700. The test frequency is 1kHz. For single supply operation, as previously covered, the amplifier should be biased to half the supply voltage to minimize distortion. Operation with dual supplies is simpler from a parts count standpoint as isolation capacitors are not required. Also the time constants associated with charging and discharging these is eliminated. Figure 10a,b and c shows the total harmonic distortion in percent versus input voltage level at 1kHz in V$_{RMS}$ for a non-inverting, unity gain NE5234. The load on the amplifier output is 10kΩ. Beginning with a supply voltage of 1.8V and an input level of 0.1V$_{RMS}$, distortion is well below 0.2% ad remains there up to an input level just over 0.5V$_{RMS}$ (1.4V$_{P-P}$) and increases to 0.4% for for 0.6V$_{RMS}$ (1.7V$_{P-P}$).

For a 2V supply, the input levels increase to 0.65V$_{RMS}$ and 0.7V$_{RMS}$, respectively for similar levels of distortion. With a supply voltage of 3.0V the input may be increased to 1V$_{RMS}$ before THD rises to 0.2% and 1.1V$_{RMS}$ for only 0.8% THD. Operation with a 600Ω load will only raise the THD figures slightly . By way of comparison, Figure 10c shows the greatly reduced dynamic range experienced when an LM324 is plugged into the test socket in place of the NE5234. Note that The THD is completely off scale for the case of 1.8 and 2.0V supply, then is barely usable for the low level end of the 3.0V supply example. Figure 11a, b, and c demonstrates the effect on harmonic distortion when closed loop gain is increased to 40dB in the non-inverting mode. It is evident that little increase in THD levels result. The graphs for the 2.0 and 3.0V supply case also include additional information on the effect of a 600Ω load on distortion.

VIII. GAIN-BANDWIDTH VS CLOSED LOOP FREQUENCY RESPONSE

Figure 5 shows the small signal frequency response of the NE5234 versus closed-loop gain in dB. The test circuit is shown in Figure 6. The plot is taken from measured data and thus shows how each value of closed-loop gain coincides with the open-loop response curve. The NE/SA5234's open-loop gain response has a uniform 6dB/octave roll-off which continues beyond 2.5MHz. This factor guarantees each op amp in the IC a high stability in virtually any gain configuration. In making these measurements, dual supplies of ±2.5V were used in order to allow a grounded reference plane and no coupling capacitors which might cause frequency related errors.

A critical parameter which affects the reproduction quality of complex waveforms is the gain-bandwidth-product of the operational amplifier. Essentially, this is a measure of the maximum frequency handling characteristics of any operational amplifier for a given closed-loop gain. As is evident from the graph, the NE/SA5234 has a 2.5MHz unity gain cross-over frequency...much higher than most other low voltage op amps. For comparison, the µA741 has a gain-bandwidth-product of 1MHz, as do the LM324 and the MC3403.

IX. LOOP-GAIN

The dynamic signal response of any closed-loop amplifier stage is a function of the Loop-gain of that particular stage. Loop-gain is equal to the open-loop gain in dB, at a given frequency, minus the closed-loop gain of the stage. The greater the Loop-gain, the lower the transfer function error of the device. Essentially, any parametric error is reduced by the factor of the Loop-gain. This includes output resistance and output signal voltage accuracy. It is good practice then to maximize Loop-gain to the degree that stage gain may be sacrificed for bandwidth. In some cases it is actually better to use two stages of gain in order to preserve signal quality than to use one high gain stage. Of course, there is a trade-off between the aforementioned factors that affect the signal-to-noise ratio of the stage and optimizing the Loop-gain. For example, a voice-band audio stage which requires 3kHz bandwidth, should be limited to a closed-loop gain of 40dB for lowest distortion in the output signal. For higher quality audio applications requiring a 20kHz bandwidth, the closed-loop gain must be limited to 20dB. This results in a Loop-gain of 20dB at the highest signal frequency.

A second consideration in the list of frequency dependent parameters is the effect of amplifier slew rate. Not only is it frequency dependent but it is also a function of signal amplitude, as we shall see in the next section.

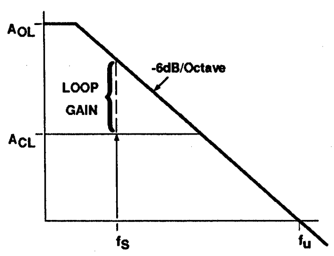


Figure 12.

X. SLEW RATE RESPONSE

The slew rate of an operational amplifier determines how fast it can respond to a signal, and is measured in volts-per-microsecond. The NE5234 has a typical slew rate of 0.8V/µs. Let us see just what this means in terms of signal handling capability. If a sinusoidal input signal, V_S, is used as reference, it is specified by its frequency and peak amplitude, V_P as follows:

$$V_S = V_P \sin(2\pi f t) \qquad \text{EQ. 13}$$

Slew Rate (SR) is the time-rate-of-change of the signal voltage during any complete cycle, that is over the range of 0 to 2π. This amounts to taking the time derivative of the sine wave which results in multiplying the cosine by the factor '2πf'.

An example of the trade off between signal amplitude and frequency is shown below for the NE5234 slew rate of 0.8V/µs. As shown in Figure 13, the maximum allowable amplitude signal which can be reproduced is determined by the slew rate response line which gives peak output volts versus frequency in Hertz.

Mathematically, slew rate is determined, by the equation below, as the derivative of the sine wave signal. The resultant slew rate function changes with both frequency and amplitude.

$$Slew\ Rate = V_P (2\pi f) \cos(2\pi f t)$$

Note that maximum slew rate occurs where the input sine wave signal crosses the values of 0, π, and 2π on the radian axis. To get a feel for what this means in regards to the typical low voltage circuit, let us consider a $1V_{RMS}$ sinusoidal input to a unity gain amplifier. The peak voltage in the above equation is 1.414V. One can then calculate the required slew rate to faithfully reproduce this signal for various signal frequencies. Or with a given slew rate and a required peak signal amplitude, the maximum frequency before slew rate limiting occurs may be determined. For example using the above amplitude of $1V_{RMS}$, and the slew rate of the NE5234 which is 800,000V/sec, one determines that the highest frequency component which may be reproduced before slew rate distortion occurs is:

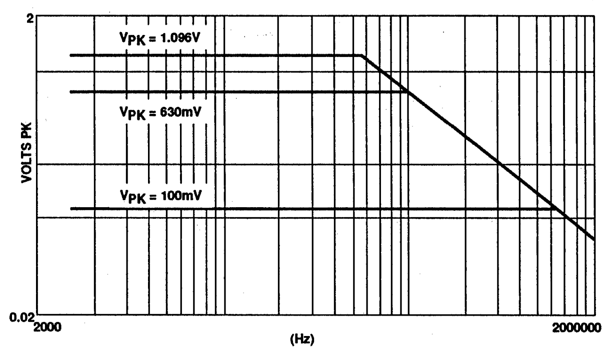


Figure 13. Slew Rate Limiting Amplitude vs Frequency

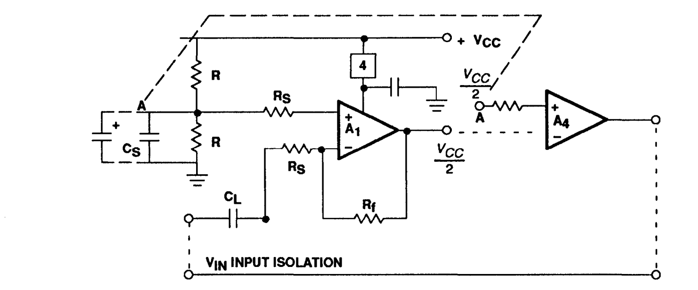


Figure 14. Single Supply Biasing in Cascade

800,000 V/sec / 2π • 1.414 volts peak = 90,090Hz. A graphical representation of this relationship is shown in Figure 13. By using this graph along with the information in the preceding Figure 10 and Figure 11, which relate usable signal levels versus power supply voltage, the dynamic behavior of a particular design may be predicted. For instance, given a single supply configuration operating at 2.0V, Figure 10b shows an upper limit to input amplitude of $0.7V_{RMS}$, or about 1V peak for 1% THD. Using this level with the data in Figure 13 leads to a figure of 116kHz as an upper frequency limit for a unity gain amplifier stage operating at 2V DC.

$$\frac{dV_S}{dt} = V_P\,\omega \cos \omega t = Slew\ Rate \qquad \text{EQ 14.}$$

XI. PROCEDURES

Single Supply Operation

When the NE/SA5234 is used in an application where a single supply is necessary, input common-mode biasing to half the supply is recommended for best signal reproduction. Referring to Figure 14, a simplified inverting amplifier input stage is shown with the simplest form of resistive divider biasing. The value of the divider resistance R is not critical and may be increased above the 10kΩ value shown as long as the bias current does not interfere with accuracy due to DC loading error. However the divider junction must be kept at a low AC impedance This is the purpose of bypass capacitor C_S. Its use provides transient suppression for signals coming from the supply bus. A low cost 0.1μF ceramic disk or chip capacitor is recommended for suppressing fast transients in the microsecond and sub-microsecond region. Foil capacitors are simply too inductive for any high frequency bypass application and should be avoided. If low frequency noise such as 60Hz or 120Hz ripple is present on the supply bus, an electrolytic capacitor is added in parallel as shown. The common-mode input source resistance, R_S, should also be matched within a reasonable tolerance for maximizing the rejection of induced AC noise.

The output of the first stage is now fixed at the common mode bias voltage and the amplified AC signal is referenced to this constant value. Capacitive coupling to the inverting input is of course required to prevent the bias voltage from being multiplied by the stage gain. Second stage biasing may now be provided by the output voltage of the first stage if non-inverting operation is used in the former. For lowest noise in a high gain input stage, the magnitude of the input source resistance is critical; low values of resistance are preferred over high values to minimize thermally generated noise.

Non-Inverting Stage Biasing

Non-inverting operation of an amplifier stage with single supply is similar to the previous example but the bias resistor R_S must now be sufficiently high to allow the signal to pass without significant attenuation. The input source resistance reflects the output resistance of the preceding stage or other sourcing device such as a bridge circuit of relatively high impedance. A simple rule of thumb is to make the bias resistor an order of magnitude larger than the generator resistance. Again the feed back network must be terminated capacitively. In this case R1 and the generator resistance should be matched and then R_S is matched to the feedback resistance ,R_F.

In all cases proper bypassing of the NE5234 supply leads (Pins 4 and 11) is very important particularly in a high noise environment. Bypass capacitors must be of ceramic construction with the shortest possible leads to keep inductance low. Chip capacitors are superior in this respect complimenting the increased use of surface mounted integrated devices. Note that both the NE5234D and the automotive grade SA5234D are available and are the surface mount versions of the device.

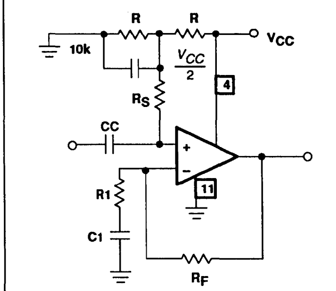


Figure 15. Non-Inverting Biasing

APPLICATIONS EXAMPLES

Instrumentation

Strain Gauge Bridge Amplifier

The circuit below shows a simple strain gauge circuit with a gain of 100 (40dB) and operated from a single supply. The chart illustrates the transfer function of the circuit for a single order-of-magnitude signal differential range from the bridge beginning with 5mV up to 50mV. The circuit is operated from a single 5V supply, but could equally as well be configured to use a dual balanced supply. It is immediately evident that the wide common-mode output range of the NE5234 is very advantageous in handling this wide range of signals with good linearity due to this feature.

A variation on this particular idea is the remote strain gauge circuit operating from a three wire line, one of which is the shield. This full-differential input circuit has balanced

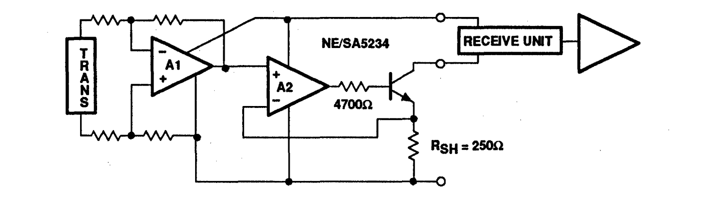
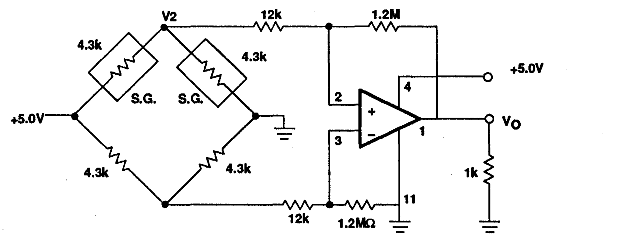


Figure 16. A 4-20mA Current Loop



$\lvert V_2 - V_1 \rvert$	V_O
5.9mV	0.5V
25.6mV	2.50V
46.6mV	4.63V

Figure 17. Strain Gauge Amplifier

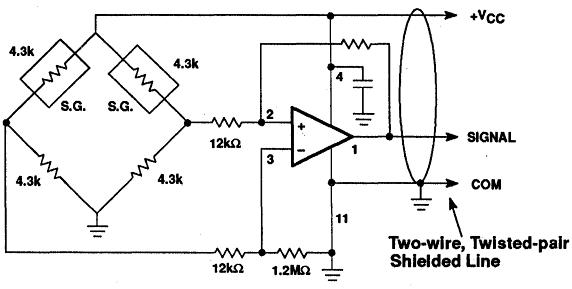


Figure 18. Remote Strain Gauge

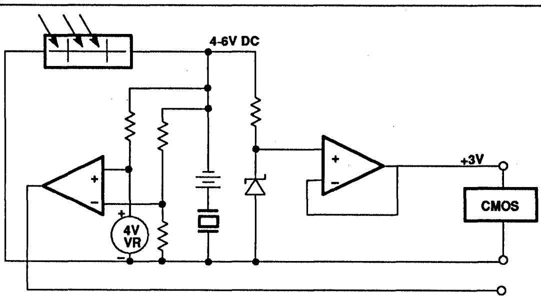


Figure 19. Solar Regulator

input resistance to afford good common-mode noise rejection characteristics. Resistors are metal film or deposited carbon. Supply leads must be carefully bypassed close to the NE/SA5234 with ceramic or chip monolithic capacitors to give optimum noise performance. As shown, an auxiliary sub-regulator may be added to improve the overall DC stability of the bridge signal voltage. A regulator capable of providing the necessary few milliamperes at somewhat reduced voltage for the transducer is shown in one of the following examples. This makes use of one of the op amps in the same device package to provide the voltage regulation. Note that the use of multiple op amps within a single package minimizes the possibility of thermal drift and mismatched response from various DC parameters.

Multiple sets of transducers may be constructed from The NE/SA5234 or the NE5234D surface mount device to form a compact and stable instrumentation package. This is useful for transducer applications in the measurement of pressure, strain, position and temperature, which have similar circuit configurations. First order temperature compensation of the transducers such as semiconductor strain gauges, or resistive units may be achieved by using one of the gauges as a reference device only. It is thermally coupled to the same member as the active gauge, as shown in the example. (Figure 18)

A 4 to 20mA Current Loop

Some instrumentation installations require the 4-20mA current loop. This addition to the above bridge transducer circuit examples is demonstrated in Figure 16.

This circuit makes use of the remote transducer bridge previously described and adds current loop signaling capability. The voltage-to-current converter consists of an additional op amp from the same NE/SA5234 package combined with a single transistor to drive the current loop. The sensitivity is actually in mA/V, or transconductance, which is equal to $1/R_{SH}$. This sensitivity in this particular example is set to 4mA/V. Thus, with a bridge amplifier having a differential gain of 100, an input of 10mV will produce a 4mA output current and 50mV will produce a 20mA output. Of course the line resistance plus receiver resistance must be within the voltage compliance range of the supply voltage to guarantee linear operation over the total range. A negative supply may be used if it is preferred to have the current loop referenced to ground.

DC Regulators and Servos

Closely related to DC and low frequency AC linear transducers are DC regulators and servo circuits. The proliferation of many battery, and solar powered remote instrumentation packages results in a need for adaptable circuits which may readily be made up from existing stock IC's. The examples given here are quite simple, but can be very useful to the designer when economy and size are at a premium.

Solar Regulator for 3-Volt CMOS

Working with small instrumentation packages which are to operate from solar photovoltaic cells may bring a need for simple sub-regulators for MOS circuits requiring only a few milliamperes of drain current.
Figure 19 shows a simple low voltage regulator making use of the particularly excellent DC characteristics of the NE/SA5234. The regulator becomes an integral part of any functional analog signal processing package such as an environmental data instrumentation unit. The low current drain of the the typical 3V or 5V MOS digital IC allows one sub regulator to serve up to 10 or more such devices. If the instrument package is to be subjected to wide temperature variations, the SA5234 is recommended. A second op amp in the package may serve as a low battery alarm with tone modulator as in radio links, or simple logic level comparator. Overcurrent protection is easily added within the regulator loop to detect short circuit failures and automatically limit the current.

DC Servo-amps

Servo control systems for low voltage motor drives require high gain-accuracy and good DC stability for many applications. Applications such as the position control of air flow vanes, servo valves, and optical lenses or apertures, are typical examples. Figure 20 demonstrates one simple DC motor servo application with position control feedback. The motor is a 3V permanent magnet rotor type used in micro-position applications and is adaptable to battery supply environments.

Position information is received from a multi-turn potentiometer to give adequate resolution. The input voltage may be generated from another potentiometer which is remote from the motor drive unit proper, or from a D/A converter output for micro processor controlled systems. The input voltage range is 1.0 to 3.0V and the supply voltage is 4.5V.

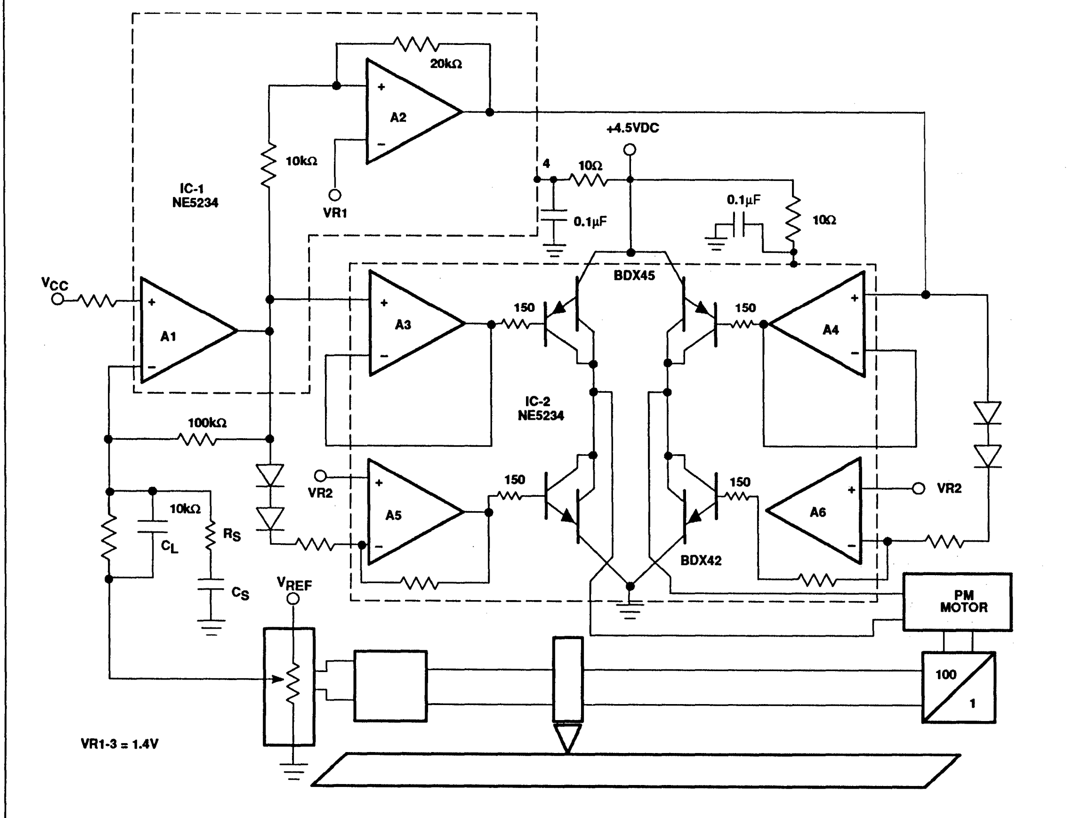


Figure 20. Full Bridge Motor Drive

Active filters

The NE5234 is easily adapted to use in a variety of active filter applications. Its high open-loop gain and excellent unity gain stability make it ideal for high-pass, band-pass and low-pass configurations operated with low voltage single supplies. Its low output impedance also makes it capable of obtaining low noise operation without resorting to separate high current buffers.

Figure 21a shows the circuit for a VCVS low-pass filter with dual supply biasing and 600Ω output termination. Figure Figure 21b is a band-pass filter with AC coupled gain network for single supply operation.

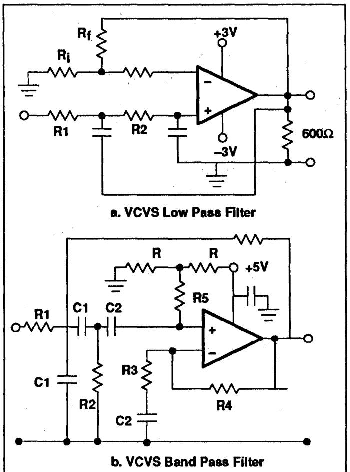


Figure 21.

Communications and Audio

Stereo Bridge Amplifier

Figure 22 shows two NE5234 ICs in a bridge amplifier application. The choice of split supplies allows DC coupling, both from the input signal source and to the load. The gain is set to a nominal 20dB. Either inverting or non-inverting operation is available. The inverting input impedance is chosen as 600Ω in order to match standard audio impedance lines within a system. The use of two such amplifiers will provide stereo operation to +10dBm for a 600Ω load.

Voice Operated Microphone

The processing of voice transmissions for communications channels is generally coupled with the need for keeping the signal-to-noise ratio high and the intelligibility optimized for a given channel bandwidth. In addition, when a circuit is battery operated and portable, the requirement to obtain maximum battery life becomes important. The circuit example shown here is aimed at filling the need for a portable voice operated transmitter, cordless phone, or tape recorder. It utilizes the Signetics NE5234 quad op amp in conjunction with the new low-voltage NE578 compandor to create an audio processor capable of operating in just such an environment. Both devices are operational to a low battery voltage of 2.0V. In addition the design further conserves current by automatically shifting the NE578 compandor to standby during the period when no transmissions are being made. Total current consumption at 3.0V is 2.8mA for the NE5234. In the active mode the NE578 draws 1.4mA and this drops to 170μA in the standby mode. This amounts to reducing the supply current demand by approximately 25% in the 'listen mode'.

Figure 23 shows the VOX audio circuit example. A description of its operation for voice activated transmission follows.

Audio generated by the electret microphone is fed into the non-inverting input of preamp A1 and the signal amplified by 12dB. The biasing is accomplished by the resistive divider which provides a level of half the supply voltage which is connected through a 100k resistor to the non-inverting terminal of A1. This automatically provides ratiometric common mode biasing set at $V_{CC}/2$ for the device. This level is then transferred directly to the following amplifier, A2, setting its DC operating point. The DC gain of both stage A1 and A2 are unity so the cumulative DC error is not multiplied by stage gain. The peak voice level is approximately $100mV_{RMS}$ at the input to A1 from the microphone and this is boosted to $400mV_{RMS}$. The feedback network gain has a low frequency corner at 160Hz and is flat up to the intersection of the closed loop gain with the open loop gain curve at nearly 500kHz. This would increase the noise bandwidth to an excessive degree unnecessary for voice channel communication. A band limiting network is, therefore, inserted across the feedback resistor to limit response to a nominal 5kHz.

Amplifier stage A2 is used to provide high level audio to the rectifier-filter stage for the rapid generation of a DC control signal for operating the voice activated switch function. Stage A2 gain is set to 20dB in order to allow activation of the voice channel on the rising edge of the first voice syllable. An attack time of 20ms is implemented by adjusting the input charging impedance (R_S) between the rectifier and the A2 amplifier output. AC coupling must be used to isolate the DC common-mode voltage of the amplifier from the rectifier/storage capacitor and to allow only audio frequencies to drive the switching circuit. Amplifier A3 provides a high impedance unity gain buffer to allow a very slow decay rate to be applied to the time constant capacitor, C_T. The output of the storage capacitor reaches approximately 3.2V for a 250ms duration 600Hz burst signal. Diode D1 (1N914) provides a negative clamp action

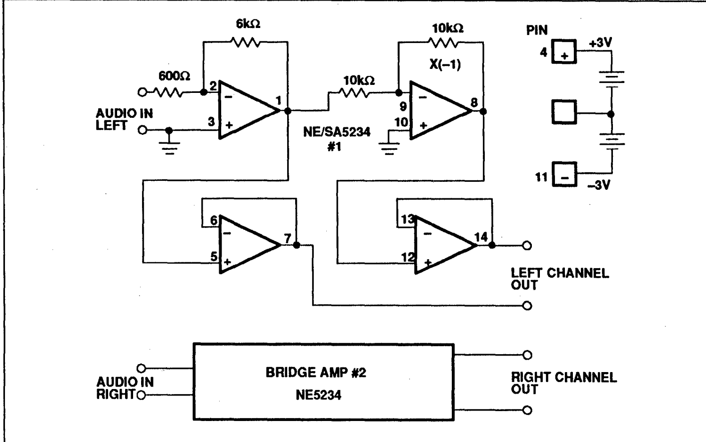


Figure 22. Stereo Bridge Amp

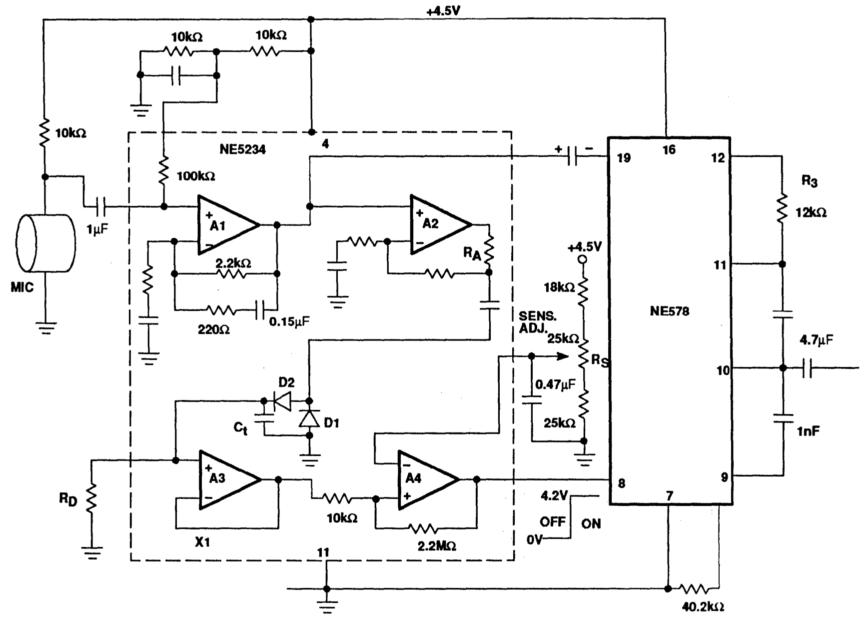


Figure 23. VOX Audio System

which forces the full peak-to-peak voltage from A2 to charge the storage capacitor. D2 then acts to charge the capacitor to the peak input voltage minus one diode drop, 0.7V. Finally, the buffered DC control signal is fed to A4 which acts as a threshold comparator with extremely high gain and controlled hysteresis. This provides a positive going signal for releasing the NE578 from its inhibit mode when voice input is present. The NE578 is switched from standby mode when voice input is present. The NE578 is switched from standby mode to the active state by raising the voltage on Pin 8 of the device above 2V. Shutting the audio channel off requires this pin to be driven below 100mV. This demands the extremely wide output voltage swing of the NE5234 in order to reach this near to the negative rail voltage. The voltage threshold of the comparator, A4, is adjustable by use of the sensitivity control, R_S. It is used to allow the activation level to be raised or lowered depending upon the ambient audio level in the transmitter vicinity.

Other critical parameters in this type of circuit are the attack and decay times of the RC network which controls the operation of the voice operated switch. Attack time determines how quickly the circuit activates after a quiet period, and the decay time sets how long the transmitter channel stays active between words. It is important to reach an optimum balance between the two time constants in order to allow unbroken transmissions of good quality and no lost syllables. A 100 to 1 attack/decay ratio is used in this particular application and this is primarily set by the value of R_A and R_D. A typical delay of two seconds is easily accomplished. Due to extremely high input impedance of the buffer stage A3, R_D may be in the 1 to 2MΩ range allowing a reasonable value of storage capacitor to be used.

The Audio Channel

Audio input from the preamplifier, A1, is fed directly to Pin 14 of the NE578 compandor. Referring to Figure 24, which shows the internal diagram of the device, it can be seen that this is the compressor portion of the NE578. There is the option in this system to operate either in a 2:1 compressor mode or an automatic level control mode, (ALC). The compressor mode simply makes a 2:1 reduction in the amplitude dynamic range of the input signal and brings it up to the chosen nominal 0dB output level which is programmable from 10mV$_{RMS}$ to 1V$_{RMS}$. In this particular example it is programmed for a 0dB level of 0.42V$_{RMS}$ which is approximately 1V$_{P-P}$. This allows for a standardized output level with good characteristics for FM modulation where peak deviation must be controlled. Figure 25 shows the input-output characteristics of the compressor and ALC. The compressor also has an attack time determined by capacitor C6 on Pin 11. Attack time is 10k * C6, decay time equals four times this value. An auxiliary amplifier stage is used following the NE578 in order to allow bandwidth and special forms of equalization to be implemented. Note that 2:1 compression in a transmission will enhance the channel dynamic range and may be used with no further processing at the receiver, but feeding the received signal through the complimentary 2:1 expandor will achieve even greater enhancement of the recovered audio. The NE578 contains both operations in the same package. Please refer to Signetics applications note AN1762 by Alvin K. Wong for complete information on these compandor circuits using the NE578.

Fiber Optic Receiver for Low Frequency Data (Figure 26)

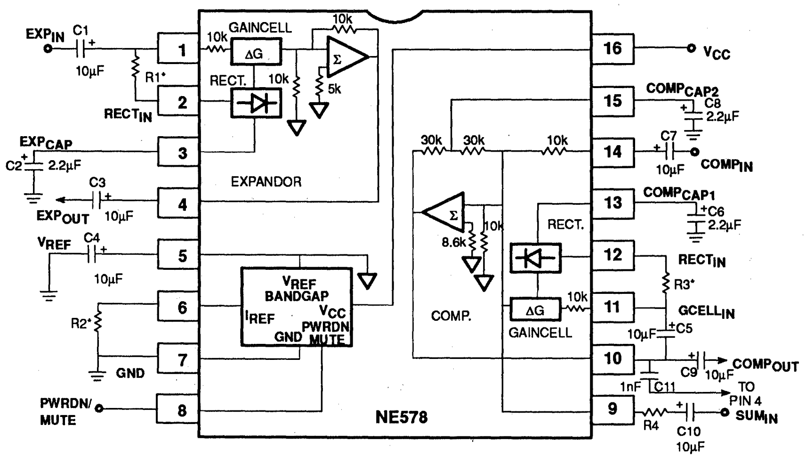
This application makes use of the NE/SA5234 to detect photo-optic signals from either fiber or air transmitted IR (Infra-red) pulses. The signal is digitally encoded for the highest signal-to-noise ratio. The received signal is sensed by an IR photo diode which has its cathode biased to half the supply voltage (2.5V). The first gain stage is configured as a transimpedance amplifier to allow conversion from the microampere diode current signals to a voltage output of approximately $10mV_{0-P}$. The second stage provides a gain-of-ten amplifier to raise this signal level to 1V peak amplitude. This stage is directly coupled from the preamplifier stage in order to provide the necessary common-mode voltage of 2.5V. Its gain control network is capacitively coupled to prevent DC gain as is required in single supply configurations. Since this is essentially a pulse gain stage, low frequency gain below the signal repetition rate is not needed. The third stage acts in a limiting amplifier configuration and its output is squared to swing approximately 5V, the standard TTL level. Again common-mode biasing is passed along from each of the stages up to the last in order minimize parts and simplify circuit layout. The final stage is a simple buffer amplifier to allow the receiver to drive a low impedance long wire line of 600Ω to 900Ω resistance. Some rise time response adjustment may be required. This is easily achieved following stage three by using R_T-C_T to limit the rate of change of the signal voltage prior to the buffer. Note that the last stage acts as a zero-crossing detector. This maximizes noise immunity by allowing a transition only after the third stage output voltage has risen above $2/3V_{CC}$. Phase inversion may be accomplished, if the logic level signals are polarity reversed, by making stage 3 inverting and AC coupling the input signal with a sufficiently large capacitor to reduce droop. Stage 3 must then be biased by connecting its non-inverting node to bias point 'A'. This provides a 2.5V threshold for the proper switching operation of the stage. However, care must be taken not allow the network's time constant to become code dependent as to the average low frequency signal components or errors will result in the output signal.

The advantage of this particular circuit is that it has the simplicity of single supply operation along with the capability of a large output swing making it fully TTL compatible

REFERENCES:

Signetics, a North American Philips Company. Linear Data Manual, Volume 2 : Industrial. Sunnyvale: 1988.

Wong, Alvin K. Companding with the NE577 and NE578..Signetics Applications Note AN1762 : September 1990.



*R1, R2 and R3 are 1% resistors.

Figure 24. Block Diagram of NE578 Test and Application Circuit

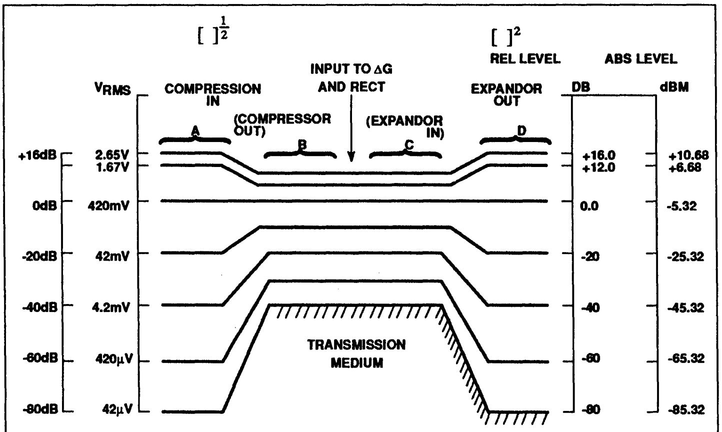


Figure 25. NE570/571/SA571 System Level

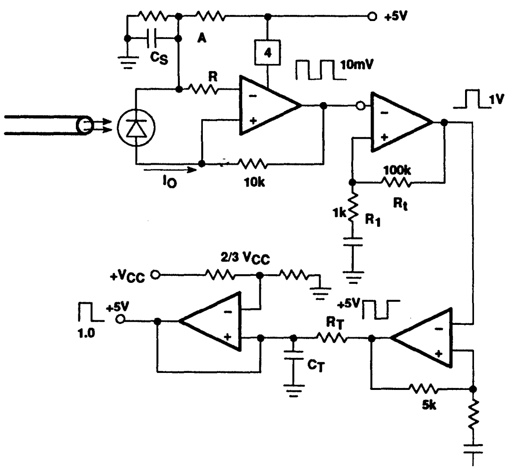


Figure 26. Fiber Optic Data Receiver

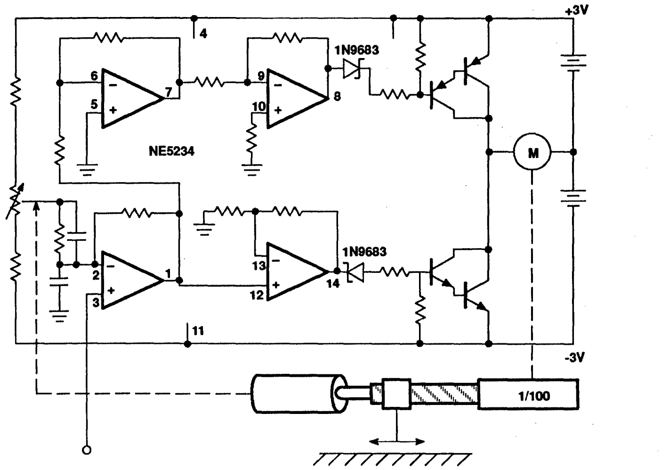


Figure 27.

High frequency operational amplifier | NE/SE5539

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

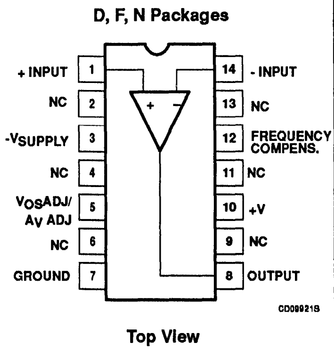
FEATURES

- Bandwidth
  - Unity gain - 350MHz
  - Full power - 48MHz
  - GBW - 1.2GHz at 17dB
- Slew rate: 600/Vµs
- A_{VOL}: 52dB typical
- Low noise - 4nV√Hz typical
- MIL-STD processing available

APPLICATIONS

- High speed datacom
- Video monitors & TV
- Satellite communications
- Image processing
- RF instrumentation & oscillators
- Magnetic storage
- Military communications

PIN CONFIGURATION



ORDERING INFORMATION

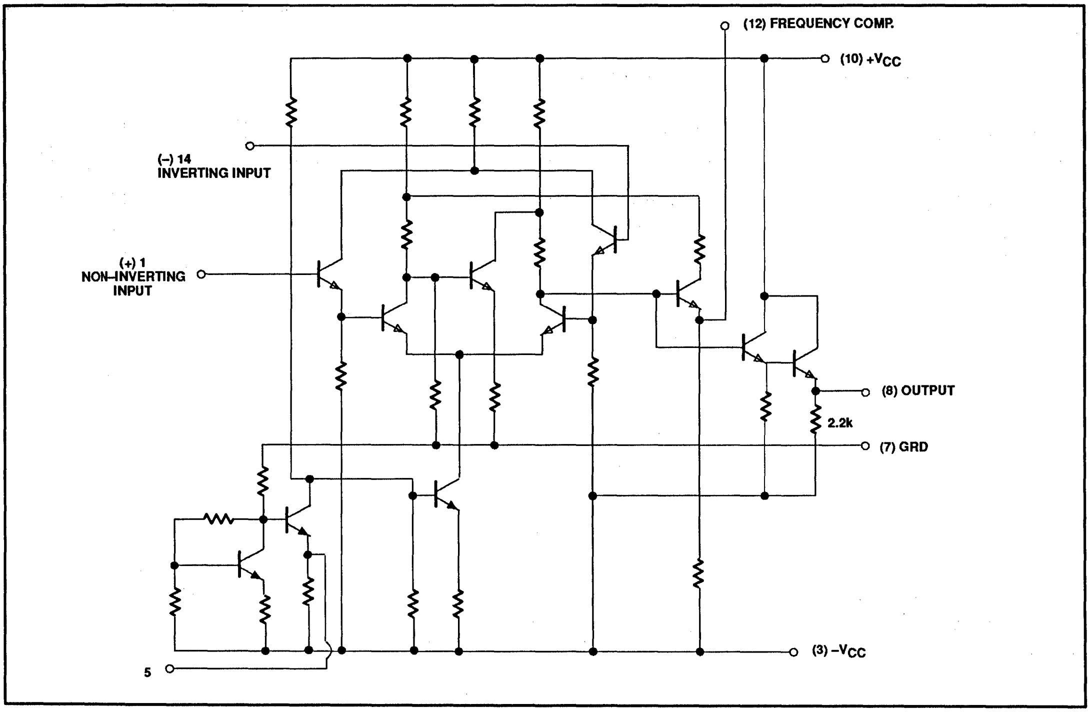
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5539N
14-Pin Plastic SO	0 to +70°C	NE5539D
14-Pin Cerdip	0 to +70°C	NE5539F
14-Pin Plastic DIP	-55 to +125°C	SE5539N
14-Pin Cerdip	-55 to +125°C	SE5539F

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	±12	V
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2] F package N package D package	 1.17 1.45 0.99	 W W W
T_A	Operating temperature range NE SE	 0 to 70 -55 to +125	 °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Max junction temperature	150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:
1. Differential input voltage should not exceed 0.25V to prevent excesive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3mW/°C
   N package at 11.6mW/°C
   D package at 7.9mW/°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 8V$, $T_A = 25°C$; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539 MIN	SE5539 TYP	SE5539 MAX	NE5539 MIN	NE5539 TYP	NE5539 MAX	UNITS
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$	+Swing -Swing				+2.3 -1.7	+2.7 -2.2		V
V_{OUT}	Output voltage swing	$R_L = 25\Omega$ to GND Over temp	+Swing -Swing	+2.3 -1.5	+3.0 -2.1					V
		$R_L = 25\Omega$ to GND $T_A = 25°C$	+Swing -Swing	+2.5 -2.0	+3.1 -2.7					V
I_{CC+}	Positive supply current	$V_O = 0$, $R_1 = \infty$, Over temp			14	18		2.8	3.5	mA
		$V_O = 0$, $R_1 = \infty$, $T_A = 25°C$			14	17		14	18	mA
I_{CC-}	Negative supply current	$V_O = 0$, $R_1 = \infty$, Over temp			11	15		2.8	3.5	mA
		$V_O = 0$, $R_1 = \infty$, $T_A = 25°C$			11	14		11	15	mA
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$, Over temp			300	1000				µV/V
		$\Delta V_{CC} = \pm 1V$, $T_A = 25°C$						200	1000	µV/V
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$, $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$					47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2\Omega$ to GND	Over temp							dB
			$T_A = 25°C$				47	52	57	
A_{VOL}	Large signal voltage gain	$V_O = +2.5V, -2.0V$ $R_L = 2\Omega$ to GND	Over temp	46		60				dB
			$T_A = 25°C$	48	53	58				

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 6V$, $T_A = 25°C$; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539 MIN	SE5539 TYP	SE5539 MAX	UNITS
V_{OS}	Input offset voltage			Over temp		2	5	mV
				$T_A = 25°C$		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	µA
				$T_A = 25°C$		0.1	1	
I_B	Input bias current			Over temp		5	20	µA
				$T_A = 25°C$		4	10	
CMRR	Common-mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85		dB
I_{CC+}	Positive supply current			Over temp		11	14	mA
				$T_A = 25°C$		11	13	
I_{CC-}	Negative supply current			Over temp		8	11	mA
				$T_A = 25°C$mA		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	µV/V
				$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+Swing	+1.4	+2.0		V
				–Swing	–1.1	–1.7		
			$T_A =$ 25°C	+Swing	+1.5	+2.0		
				–Swing	–1.4	–1.8		

AC ELECTRICAL CHARACTERISTICS

V_{CC} = ±8V, R_L = 150Ω to GND and 470Ω to -V_{CC}, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
BW	Gain bandwidth product	A_{CL} = 7, V_O = 0.1 V_{P-P}		1200			1200		MHz
	Small signal bandwidth	A_{CL} = 2, R_L = 150Ω[1]		110			110		MHz
t_S	Settling time	A_{CL} = 2, R_L = 150Ω[1]		15			15		ns
SR	Slew rate	A_{CL} = 2, R_L = 150Ω[1]		600			600		V/μs
t_{PD}	Propagation delay	A_{CL} = 2, R_L = 150Ω[1]		7			7		ns
	Full power response	A_{CL} = 2, R_L = 150Ω[1]		48			48		MHz
	Full power response	A_V = 7, R_L = 150Ω[1]		20			20		MHz
	Input noise voltage	R_S = 50Ω, 1MHz		4			4		nV/√Hz
	Input noise current	1MHz		6			6		pA/√Hz

NOTES:
1. External compensation.

AC ELECTRICAL CHARACTERISTICS

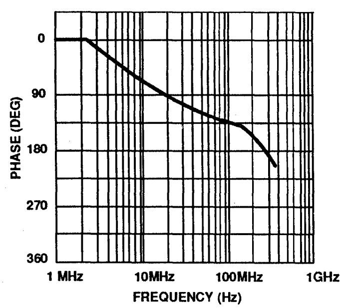
V_{CC} = ±6V, R_L = 150Ω to GND and 390Ω to -V_{CC}, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNITS
			MIN	TYP	MAX	
BW	Gain bandwidth product	A_{CL} = 7		700		MHz
	Small signal bandwidth	A_{CL} = 2[1]		120		MHz
t_S	Settling time	A_{CL} = 2[1]		23		ns
SR	Slew rate	A_{CL} = 2[1]		330		V/μs
t_{PD}	Propagation delay	A_{CL} = 2[1]		4.5		ns
	Full power response	A_{CL} = 2[1]		20		MHz

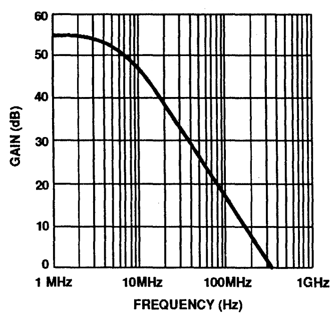
NOTES:
1. External compensation.

TYPICAL PERFORMANCE CURVES

NE5539 Open-Loop Phase

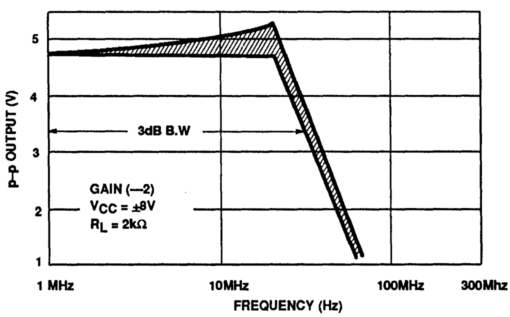


NE5539 Open-Loop Gain

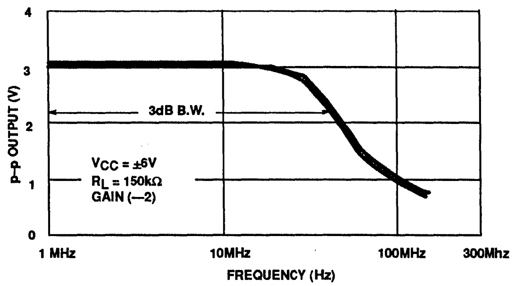


TYPICAL PERFORMANCE CURVES (Continued)

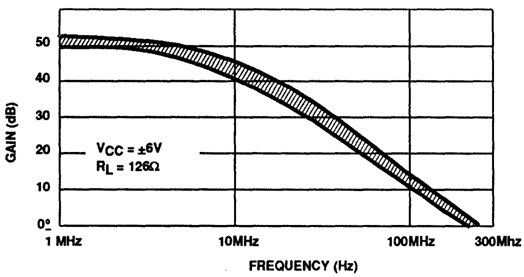
Power Bandwidth (SE)



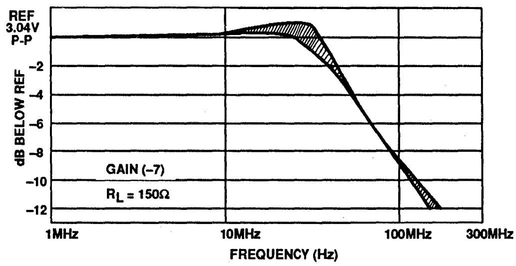
Power Bandwidth (NE)



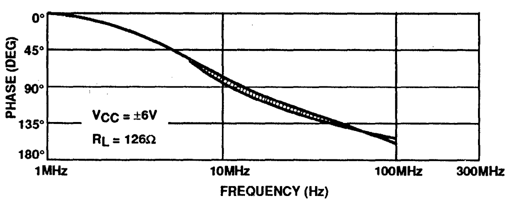
SE5539 Open-Loop Gain vs Frequency



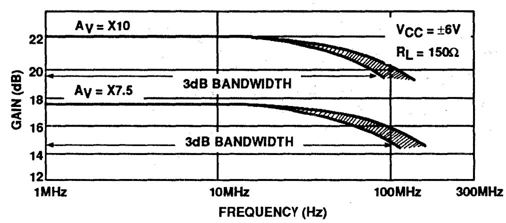
Power Bandwidth



SE5539 Open-Loop Phase vs Frequency



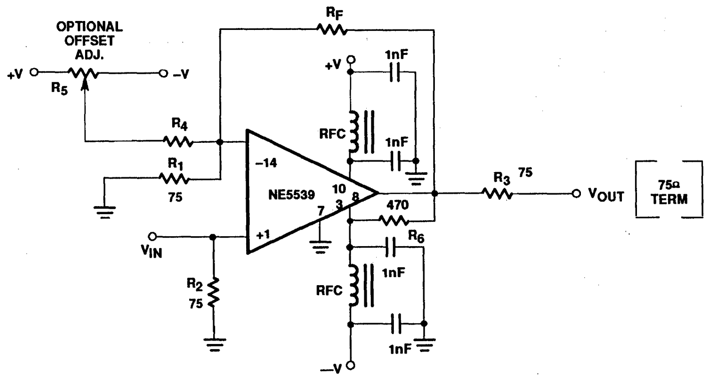
Gain Bandwidth Product vs Frequency



NOTE:
Indicates typical distribution –55°C ≤ T_A ≤ 125°C

CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the physical circuit is extremely critical. Bread-boarding is not recommended. A double-sided copper-clad printed circuit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.



R1 = 75Ω 5% CARBON
R2 = 75Ω 5% CARBON
R3 = 75Ω 5% CARBON
R4 = 36K 5% CARBON

R5 = 20k TRIMPOT (CERMET)
RF = 1.5k (28dB GAIN)
R6 = 470Ω 5% CARBON

RFC 3T # 26 BUSS WIRE ON
FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

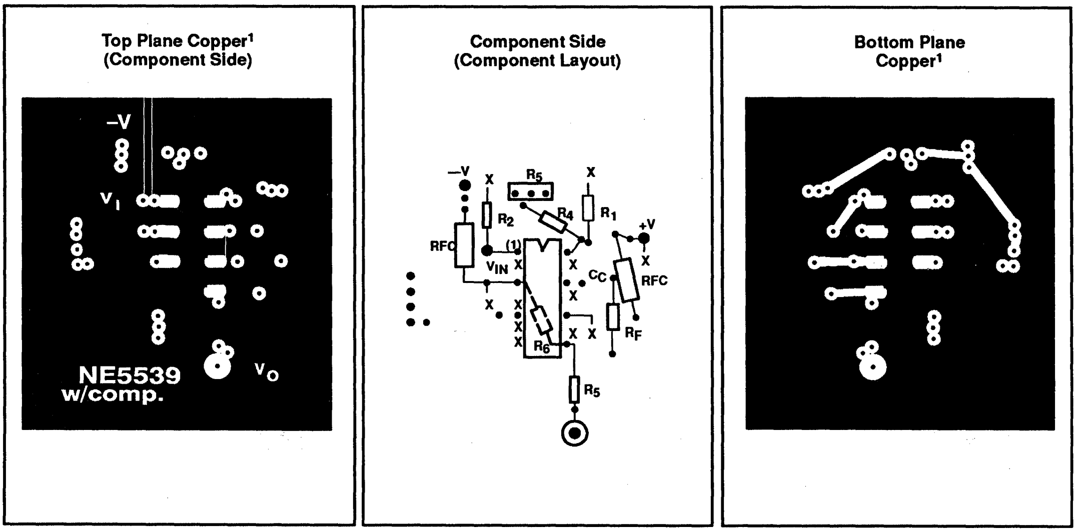


Figure 1. 28dB Non-Inverting Amp Sample PC Layout

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in Figure 2 along with vector-scope1 photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75W input and output termionation impedance with a gain of approximately 10 (20dB).

NOTE:

1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.

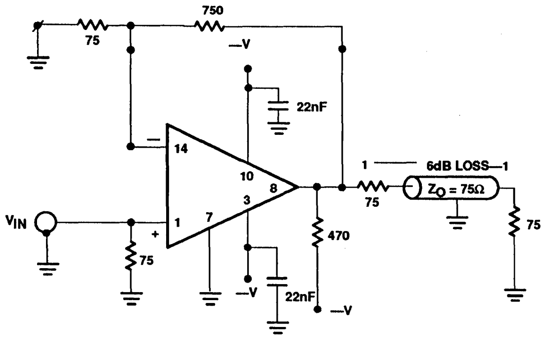


Figure 2. NE5539 Video Amplifier

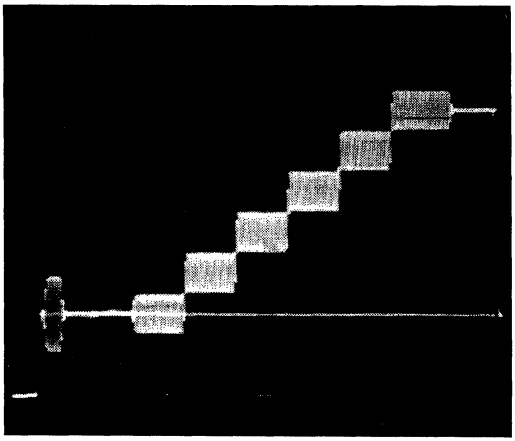


Figure 3. Input Signal

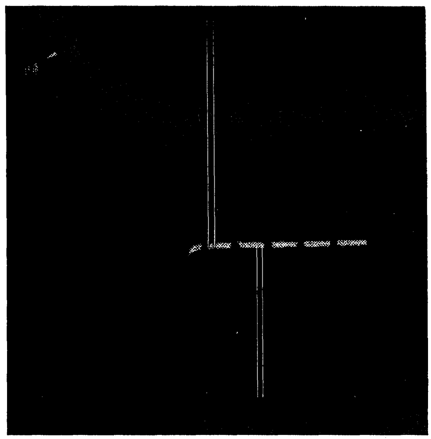


Figure 4. Differential Gain <0.5%

NOTE:
Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

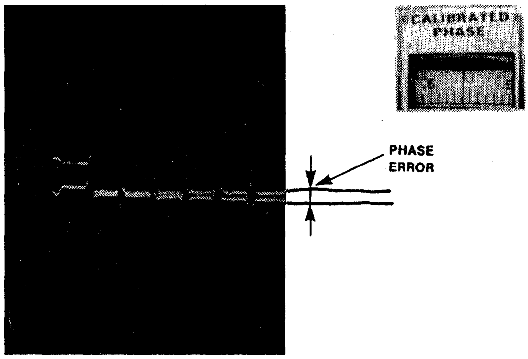


Figure 5. Differential Gain +0.1°

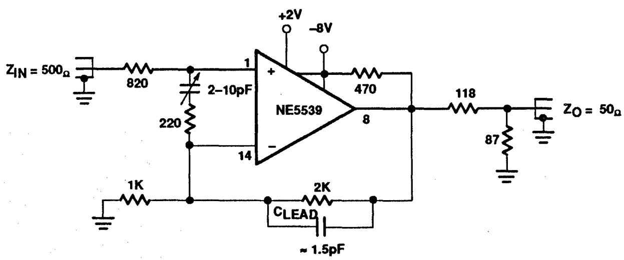


Figure 6. Non-Inverting Follower

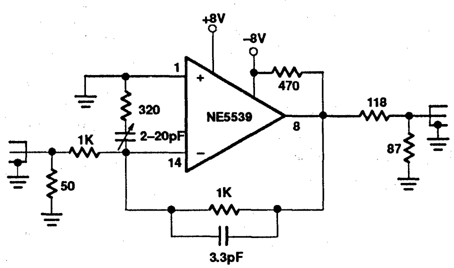


Figure 7. Inverting Follower

Video amplifier

NE5592

DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers a fixed gain of 400 without external components and an adjustable gain from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

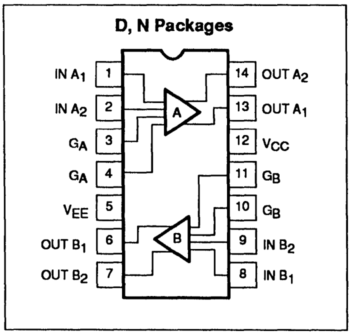
FEATURES

- 110MHz unity gain bandwidth
- Adjustable gain from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components

APPLICATIONS

- Floppy disk head amplifier
- Video amplifier
- Pulse amplifier in communications
- Magnetic memory
- Video recorder systems

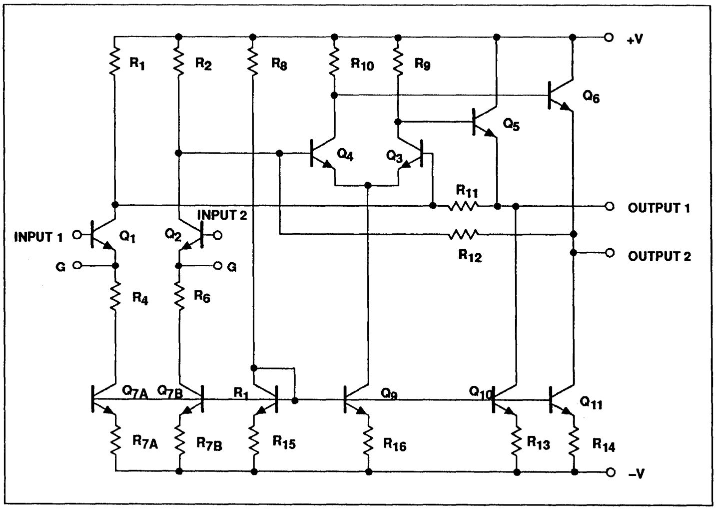
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to 70°C	NE5592N
14-Pin SO package	0 to 70°C	NE5592D

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common mode Input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range NE5592	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\,MAX}$	Maximum power dissipation, T_A=25°C (still air)[1] D package N package	 1.03 1.48	 W W

NOTES:
1. Derate above 25°C at the following rates:
   D package 8.3mW/°C
   N package 11.9mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C, V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltage is V_S = ±6.0V, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	R_L=2kΩ, V_{OUT}=3V_{P-P}	400	480	600	V/V
R_{IN}	Input resistance		3	14		kΩ
C_{IN}	Input capacitance			2.5		pF
I_{OS}	Input offset current			0.3	3	µA
I_{BIAS}	Input bias current			5	20	µA
	Input noise voltage	BW 1kHz to 10MHz		4		nV/√Hz
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	V_{CM} ± 1V, f<100kHz V_{CM} ± 1V, f=5MHz	60	93 87		dB dB
PSRR	Supply voltage rejection ratio	ΔV_S= ± 0.5V	50	85		dB
	Channel separation	V_{OUT}=1V_{P-P}; f=100kHz (output referenced) R_L=1kΩ	65	70		dB
V_{OS}	Output offset voltage gain select pins open	R_L=∞ R_L=∞		0.5 0.25	1.5 0.75	V V
V_{CM}	Output common-mode voltage	R_L=∞	2.4	3.1	3.4	V
V_{OUT}	Output differential voltage swing	R_L=2kΩ	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current (total for both sides)	R_L=∞		35	44	mA

DC ELECTRICAL CHARACTERISTICS

V_{SS}=±6V, V_{CM}=0, 0°C ≤ T_A ≤ 70°C, unless otherwise specified. Recommended operating supply voltage is V_S = ±6.0V, and gain select pins are connected together.

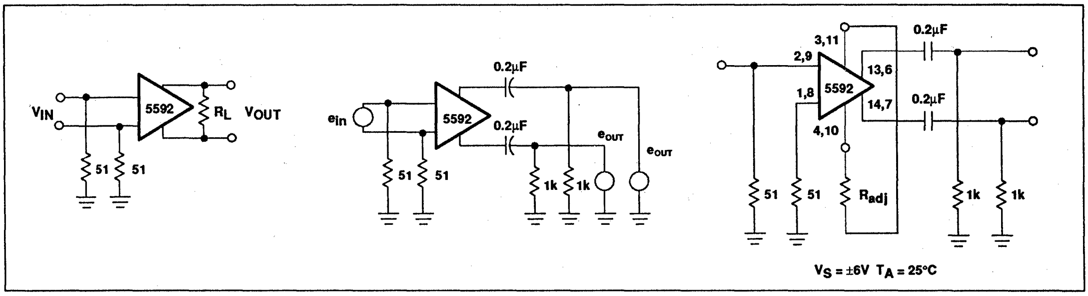
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	R_L=2kΩ, V_{OUT}=3V_{P-P}	350	430	600	V/V
R_{IN}	Input resistance		1	11		kΩ
I_{OS}	Input offset current				5	μA
I_{BIAS}	Input bias current				30	μA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	V_{CM} ± 1V, f<100kHz R_S=ϕ	55			dB
PSRR	Supply voltage rejection ratio	ΔV_S= ± 0.5V	50			dB
	Channel separation	V_{OUT}=1V_{P-P}; f=100kHz (output referenced) R_L=1kΩ		70		dB
V_{OS}	Output offset voltage					
	gain select pins connected together	R_L=∞			1.5	V
	gain select pins open	R_L=∞			1.0	V
V_{OUT}	Output differential voltage swing	R_L=2kΩ	2.8			V
I_{CC}	Power supply current (total for both sides)	R_L=∞			47	mA

AC ELECTRICAL CHARACTERISTICS

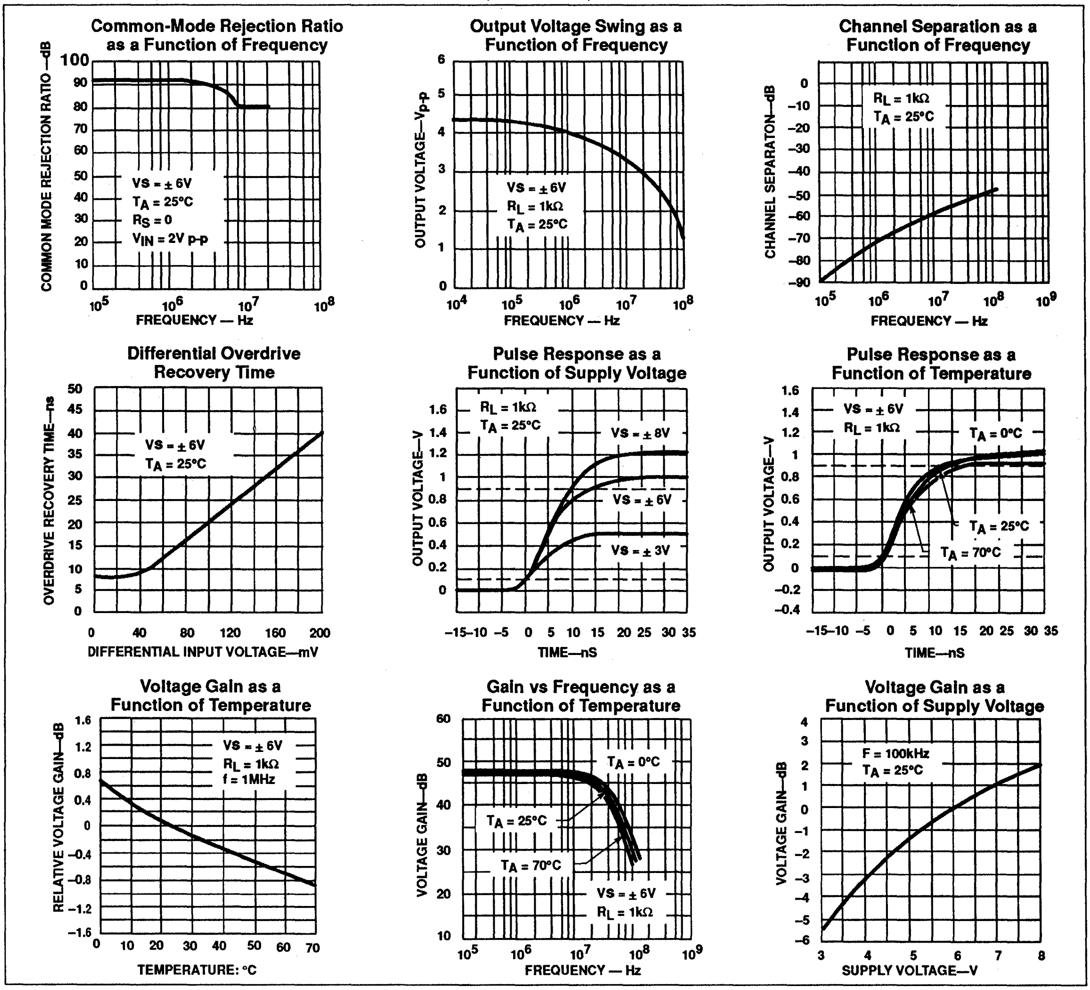
T_A=+25°C V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltage V_S=±6.0V. Gain select pins connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
BW	Bandwidth	V_{OUT}=1V_{P-P}		25		MHz
t_R	Rise time			15	20	ns
t_{PD}	Propagation delay	V_{OUT}=1V_{P-P}		7.5	12	ns

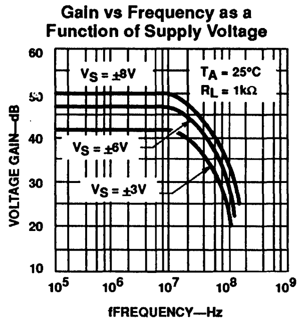
TEST CIRCUITS T_A=25°C unless otherwise specified.

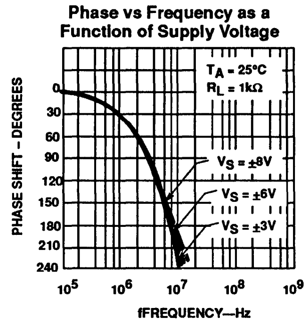


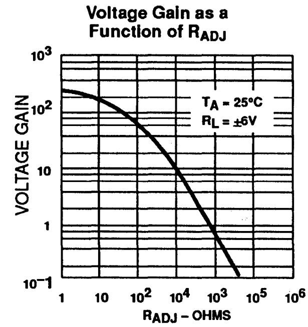
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

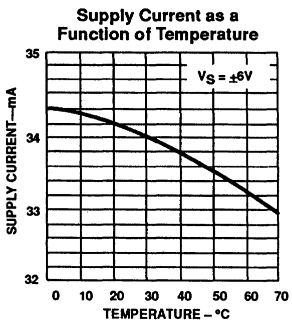


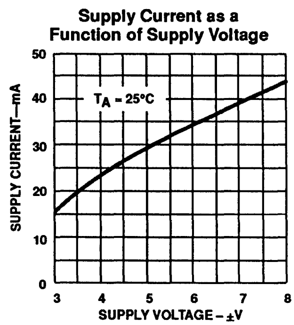
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

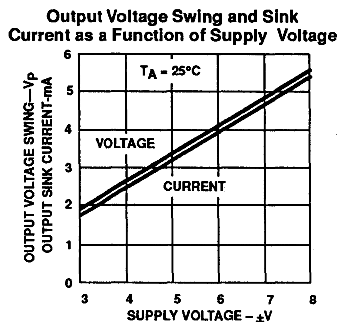


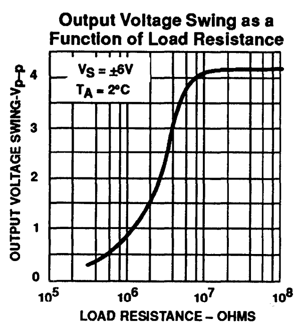


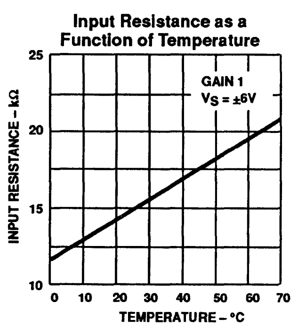


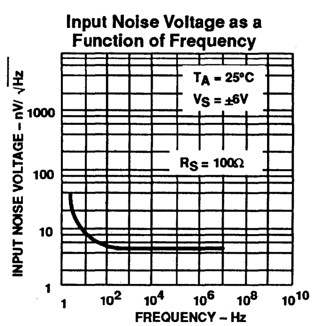












Video amplifier NE/SA/SE592

DESCRIPTION

The NE/SA/SE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

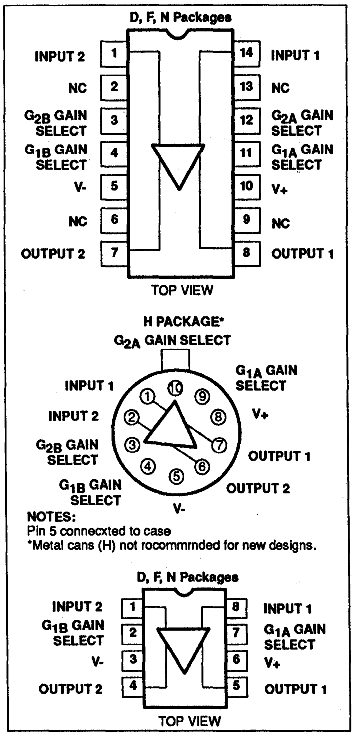
FEATURES

- 120MHz unity gain bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components
- MIL-STD processing available

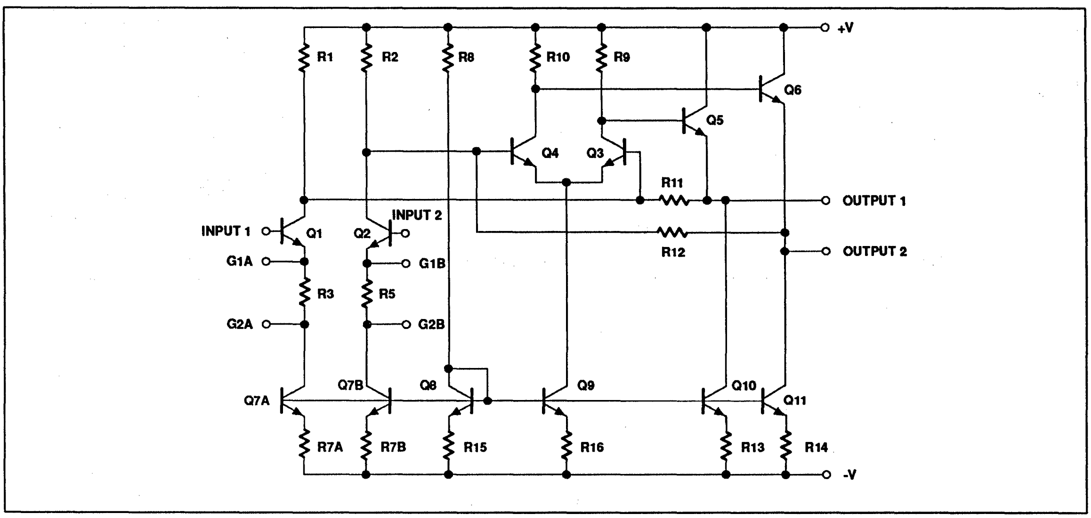
APPLICATIONS

- Floppy disk head amplifier
- Video amplifier
- Pulse amplifier in communications
- Magnetic memory
- Video recorder systems

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE592N14
14-Pin Cerdip	0 to +70°C	NE592F14
14-Pin Cerdip	-55°C to +125°C	SE592F14
14-Pin SO	0 to +70°C	NE592D14
8-Pin Plastic DIP	0 to +70°C	NE592N8
8-Pin Cerdip	-55°C to +125°C	SE592F8
8-Pin Plastic DIP	-40°C to +85°C	SA592N8
8-Pin SO	0 to +70°C	NE592D8
8-Pin SO	-40°C to +85°C	SA592D8
10-Lead Metal Can	0 to +70°C	NE592H
10-Lead Metal Can	-55°C to +125°C	SE592H

NOTES:
N8, N14, D8 and D14 package parts also available in "High" gain version by adding "H" before package designation, i.e., NE592HDB

ABSOLUTE MAXIMUM RATINGS

T_A=+25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating ambient temperature range		
	SE592	-40 to +85	°C
	NE592	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\,MAX}$	Maximum power dissipation,		
	T_A=25°C (still air)[1]		
	F-14 package	1.17	W
	F-8 package	0.79	W
	D-14 package	0.98	W
	D-8 package	0.79	W
	H package	0.83	W
	N-14 package	1.44	W
	N-8 package	1.17	W

NOTES:
1. Derate above 25°C at the following rates:
   F-14 package at 9.3mW/°C
   F-8 package at 6.3mW/°C
   D-14 package at 7.8mW/°C
   D-8 package at 6.3mW/°C
   H package at 6.7mW/°C
   N-14 package at 11.5mW/°C
   N-8 package at 9.3mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C V_{SS}=+6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=+6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	R_L=2kΩ, V_{OUT}=3V_{P-P}	250	400	600	300	400	500	V/V
	Gain 2[2,4]		80	100	120	90	100	110	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 1[1]			4.0			4.0		kΩ
	Gain 2[2,4]		10	30		20	30		kΩ
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	V_{CM}±1V, f<100kHz	60	86		60	86		dB
	Gain 2[4]	V_{CM}±1V, f=5MHz		60			60		dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	ΔV_S=±0.5V	50	70		50	70		dB
V_{OS}	Output offset voltage								
	Gain 1	R_L=∞			1.5			1.5	V
	Gain 2[4]	R_L=∞			1.5			1.0	V
	Gain 3[3]	R_L=∞		0.35	0.75		0.35	0.75	V
V_{CM}	Output common-mode voltage	R_L=∞	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	R_L=2kΩ	3.0	4.0		3.0	4.0		V
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	R_L=∞		18	24		18	24	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

DC ELECTRICAL CHARACTERISTICS

DC Electrical CharacteristicsV_{SS}=±6V, V_{CM}=0, 0°C ≤T_A≤70°C for NE592; -40°C ≤T_A ≤ 85°C for SA592, -55°C ≤T_A ≤ 125°C for SE592, unless otherwise specified. Recommended operating supply voltages V_S=+6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	R_L=2kΩ, V_{OUT}=3V_{P-P}	250		600	200		600	V/V
	Gain 2[2,4]		80		120	80		120	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 2[2,4]		8.0			8.0			kΩ
I_{OS}	Input offset current				6.0			5.0	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	V_{CM}±1V, f<100kHz	50			50			dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	ΔV_S=±0.5V	50			50			dB
V_{OS}	Output offset voltage								
	Gain 1	R_L=∞			1.5			1.5	V
	Gain 2[4]				1.5			1.2	
	Gain 3[3]				1.0			1.0	
V_{OUT}	Output voltage swing differential	R_L=2kΩ	2.8			2.5			V
I_{CC}	Power supply current	R_L=∞			27			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

AC ELECTRICAL CHARACTERISTICS

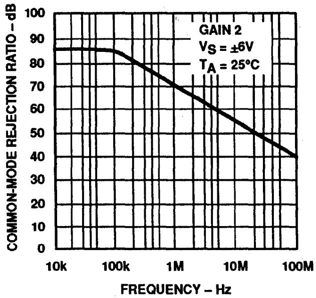
T_A=+25°C V_{SS}=+6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth								
	Gain 1[1]			40			40		MHz
	Gain 2[2,4]			90			90		MHz
t_R	Rise time								
	Gain 1[1]	V_{OUT}=1V_{P-P}		10.5	12		10.5	10	ns
	Gain 2[2,4]			4.5			4.5		ns
t_{PD}	Propagation delay								
	Gain 1[1]	V_{OUT}=1V_{P-P}		7.5	10		7.5	10	ns
	Gain 2[2,4]			6.0			6.0		ns

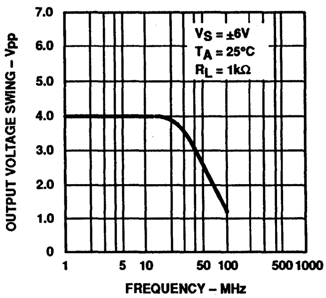
NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

TYPICAL PERFORMANCE CHARACTERISTICS

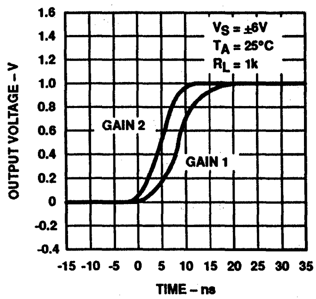
Common-Mode Rejection Ratio as a Function of Frequency



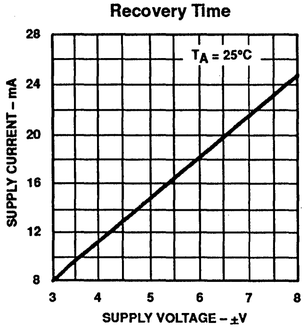
Output Voltage Swing as a Function of Frequency



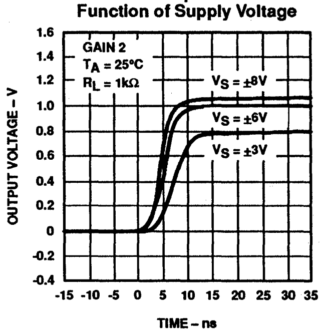
Pulse Response



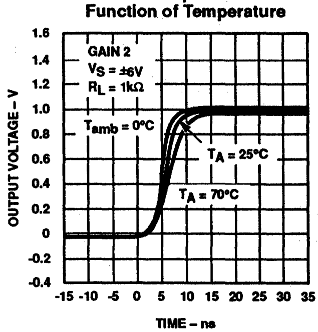
Differential Overdrive Recovery Time



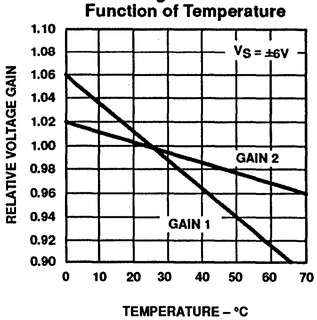
Pulse Response as a Function of Supply Voltage



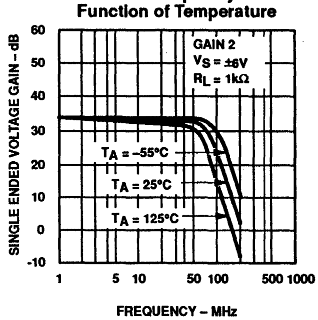
Pulse Response as a Function of Temperature



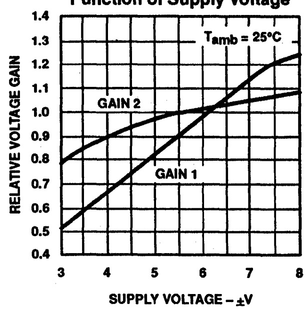
Voltage Gain as a Function of Temperature



Gain vs. Frequency as a Function of Temperature

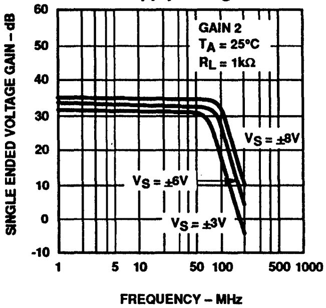


Voltage Gain as a Function of Supply Voltage

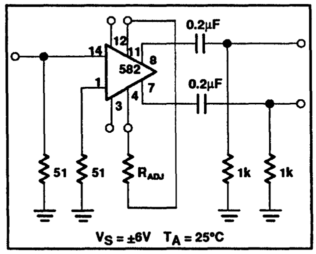


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

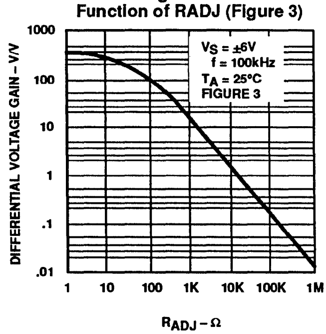
Gain vs. Frequency as a Function of Supply Voltage



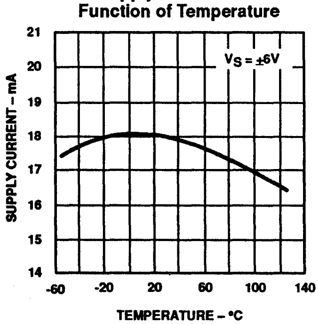
Voltage Gain Adjust Circuit



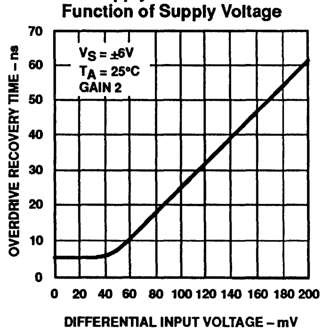
Voltage Gain as a Function of RADJ (Figure 3)



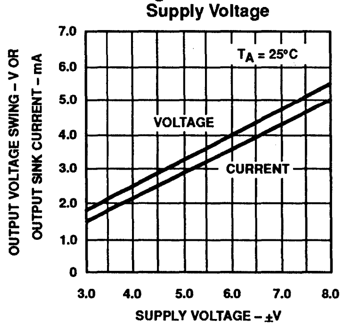
Supply Current as a Function of Temperature



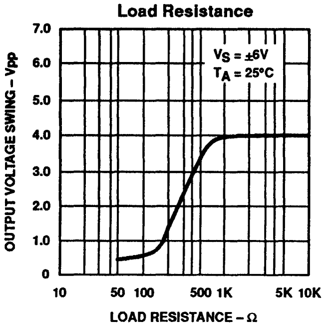
Supply Current as a Function of Supply Voltage



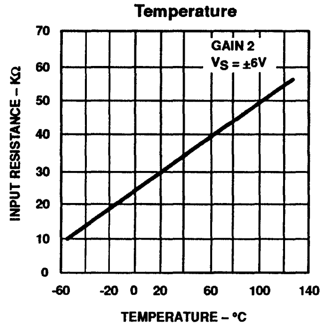
Output Voltage and Current Swing as a Function of Supply Voltage



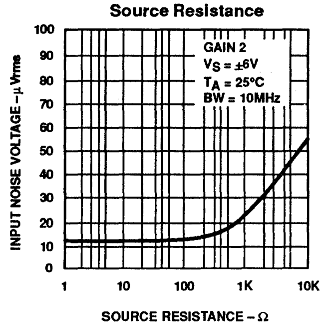
Output Voltage Swing as a Function of Load Resistance



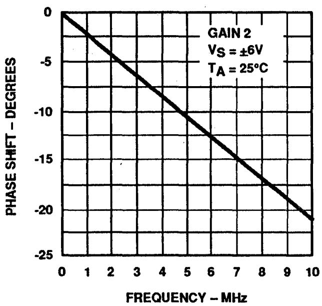
Input Resistance as a Function of Temperature



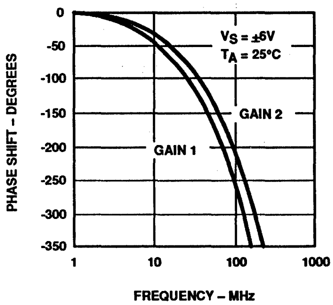
Input Noise Voltage as a Function of Source Resistance



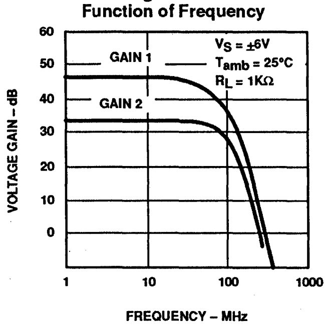
Phase Shift as a Function of Frequency



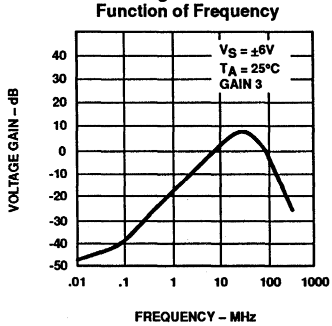
Phase Shift as a Function of Frequency



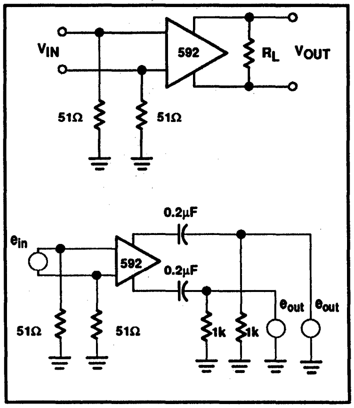
Voltage Gain as a Function of Frequency



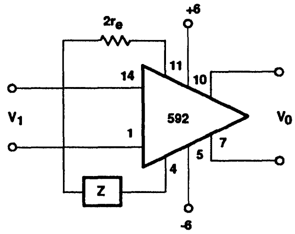
Voltage Gain as a Function of Frequency



TEST CIRCUITS T_A = 25°C, unless otherwise specified.



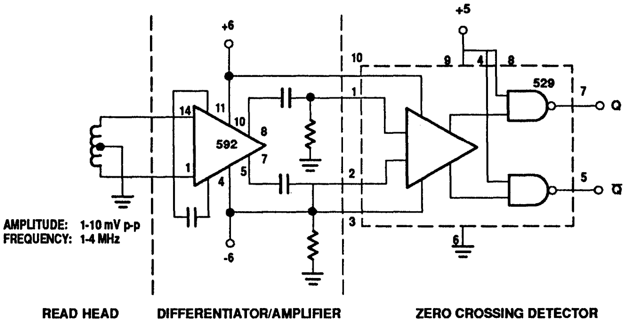
TYPICAL APPLICATIONS



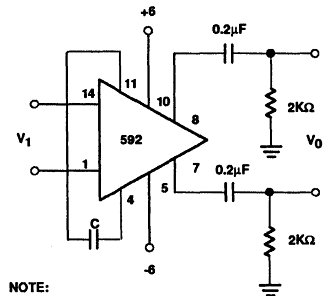
NOTE:

$$\frac{V_O(s)}{V_1(s)} = \frac{1.4 \cdot 10^4}{Z(S) + 2r_e} = \frac{1.4 \cdot 10^4}{Z(S) + 32}$$

Basic Configuration



Disc/Tape Phase-Modulated Readback Systems



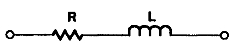
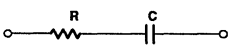
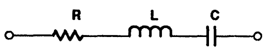
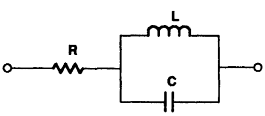
NOTE:

For frequency $F_1 << 1/2\pi(32)C$

$$V_O = 1.4 \times 10^4 C \frac{dVi}{dT}$$

Differentiation with High Common-Mode Noise Rejection

FILTER NETWORKS

Z NETWORK	FILTER TYPE	$\frac{V_O(s)}{V_1(s)}$ TRANSFER FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s+R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s+1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2+R/Ls+1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2+1/LC}{s^2+1/LC+s/RC}\right]$

NOTES:

In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.
$S = j\omega$
$\omega = 2\pi f$

6W audio amplifier with preamplifier — TDA1010A

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4 Ω and 2 Ω load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 10 W.

Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 24	V
Repetitive peak output current	I_{ORM}	max.	3	A
Output power at pin 2; d_{tot} = 10%				
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	6,4	W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6,2	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,4	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\vert Z_i \vert$	typ.	30	kΩ
power amplifier (pin 6)	$\vert Z_i \vert$	typ.	20	kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31	mA
Sensitivity for P_o = 5,8 W; R_L = 4 Ω	V_i	typ.	10	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

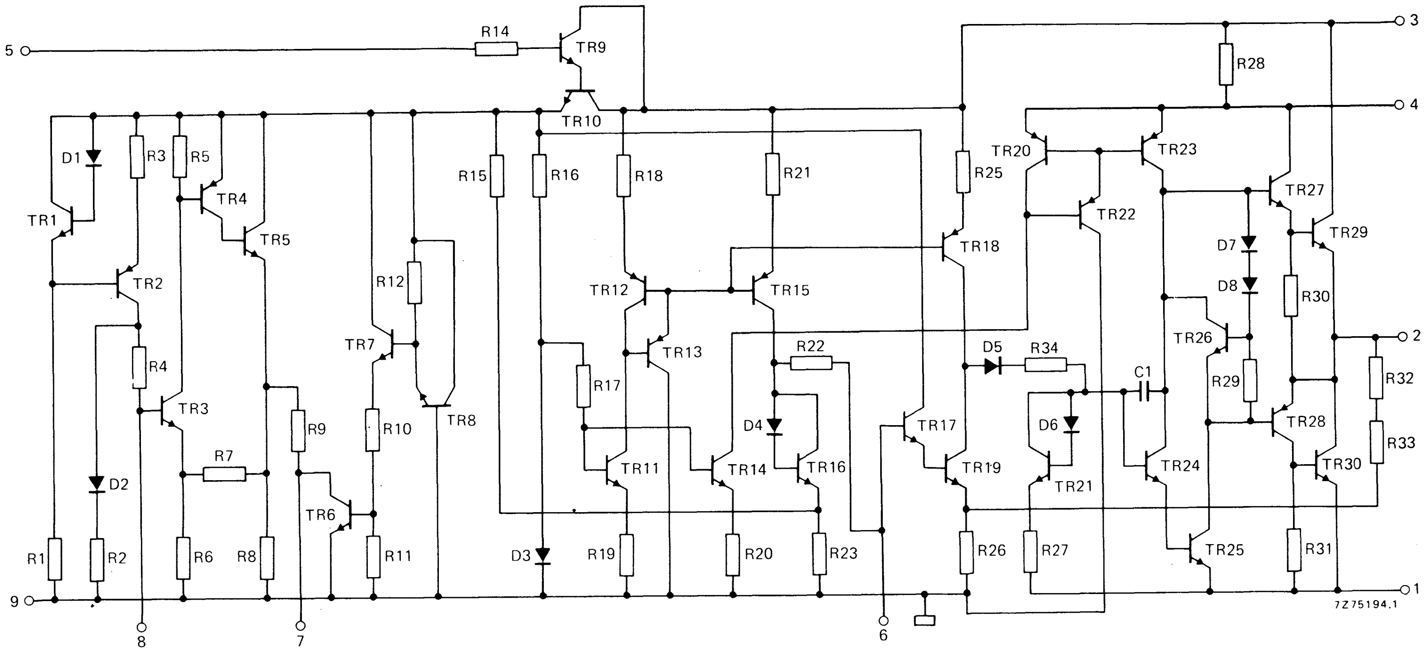


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	5 A
Repetitive peak output current	I_{ORM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150 °C	
Operating ambient temperature	T_{amb}	−25 to + 150 °C	
A.C. short-circuit duration of load during sine-wave drive; without heatsink at V_P = 14,4 V	t_{sc}	max.	100 hours

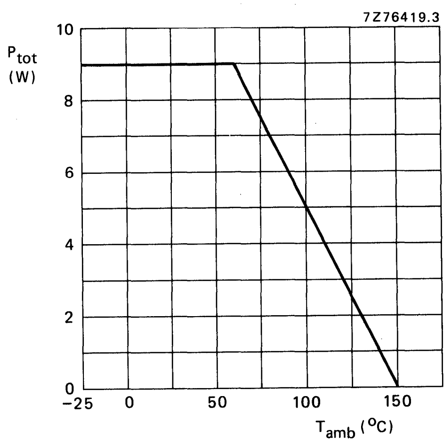


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 14,4 V; R_L = 2 Ω; T_{amb} = 60 °C maximum; thermal shut-down starts at T_j = 150 °C. The maximum sine-wave dissipation in a 2 Ω load is about 5,2 W. The maximum dissipation for music drive will be about 75% of the worst-case sine-wave dissipation, so this will be 3,9 W. Consequently, the total resistance from junction to ambient

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{3{,}9} = 23\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W,

$$R_{th\ h\text{-}a} = 23 - (10 + 1) = 12\ \text{K/W}.$$

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 24	V
Repetitive peak output current	I_{ORM}	<	3	A
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power (see Fig. 4) at d_{tot} = 10%; measured at pin 2; with bootstrap				
V_P = 14,4 V; R_L = 2 Ω (note 1)	P_o	typ.	6,4	W
V_P = 14,4 V; R_L = 4 Ω (note 1 and 2)	P_o	>	5,9	W
		typ.	6,2	W
V_P = 14,4 V; R_L = 8 Ω (note 1)	P_o	typ.	3,4	W
V_P = 14,4 V; R_L = 4 Ω; without bootstrap	P_o	typ.	5,7	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9	W
Voltage gain				
preamplifier (note 3)	G_{v1}	typ.	24	dB
			21 to 27	dB
power amplifier	G_{v2}	typ.	30	dB
			27 to 33	dB
total amplifier	$G_{v\,tot}$	typ.	54	dB
			51 to 57	dB
Total harmonic distortion at P_o = 1 W	d_{tot}	typ.	0,2	%
Efficiency at P_o = 6 W	η	typ.	75	%
Frequency response (–3 dB)	B		80 Hz to 15	kHz
Input impedance				
preamplifier (note 4)	$\|Z_i\|$	typ.	30	kΩ
			20 to 40	kΩ
power amplifier (note 5)	$\|Z_i\|$	typ.	20	kΩ
			14 to 26	kΩ
Output impedance of preamplifier; pin 7 (note 5)	$\|Z_o\|$	typ.	20	kΩ
			14 to 26	kΩ
Output voltage preamplifier (r.m.s. value) d_{tot} < 1% (pin 7) (note 3)	$V_{o(rms)}$	>	0,7	V
Noise output voltage (r.m.s. value; note 6)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,3	mV
R_S = 8,2 kΩ	$V_{n(rms)}$	typ.	0,7	mV
		<	1,4	mV
Ripple rejection at f = 1 kHz to 10 kHz (note 7)	RR	>	42	dB
at f = 100 Hz; C2 = 1 μF	RR	>	37	dB
Sensitivity for P_o = 5,8 W	V_i	typ.	10	mV
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	30	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Up to $P_o \leqslant 3$ W : $d_{tot} \leqslant 1\%$.
3. Measured with a load impedance of 20 kΩ.
4. Independent of load impedance of preamplifier.
5. Output impedance of preamplifier ($|Z_o|$) is correlated (within 10%) with the input impedance ($|Z_i|$) of the power amplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The tab must be electrically floating or connected to the substrate (pin 9).

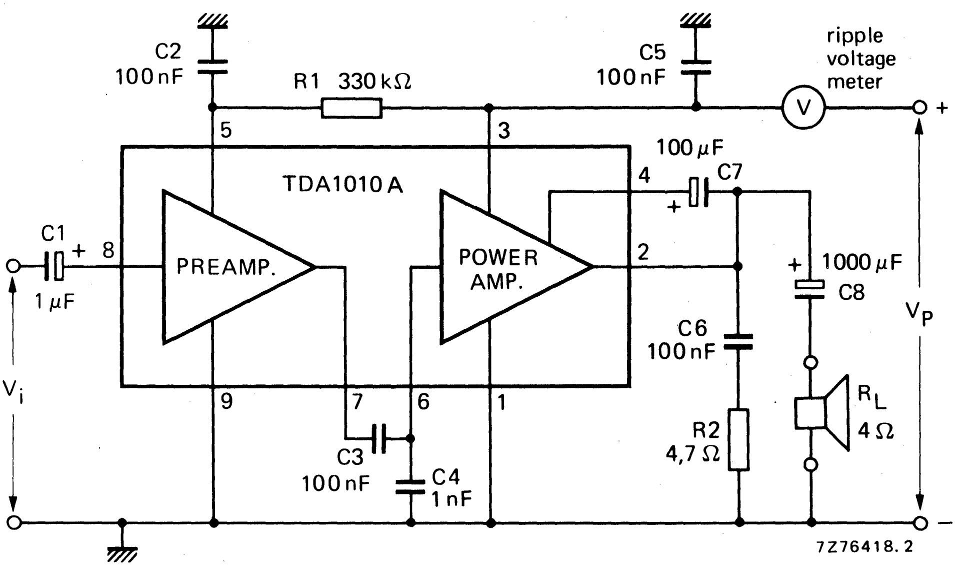


Fig. 3 Test circuit.

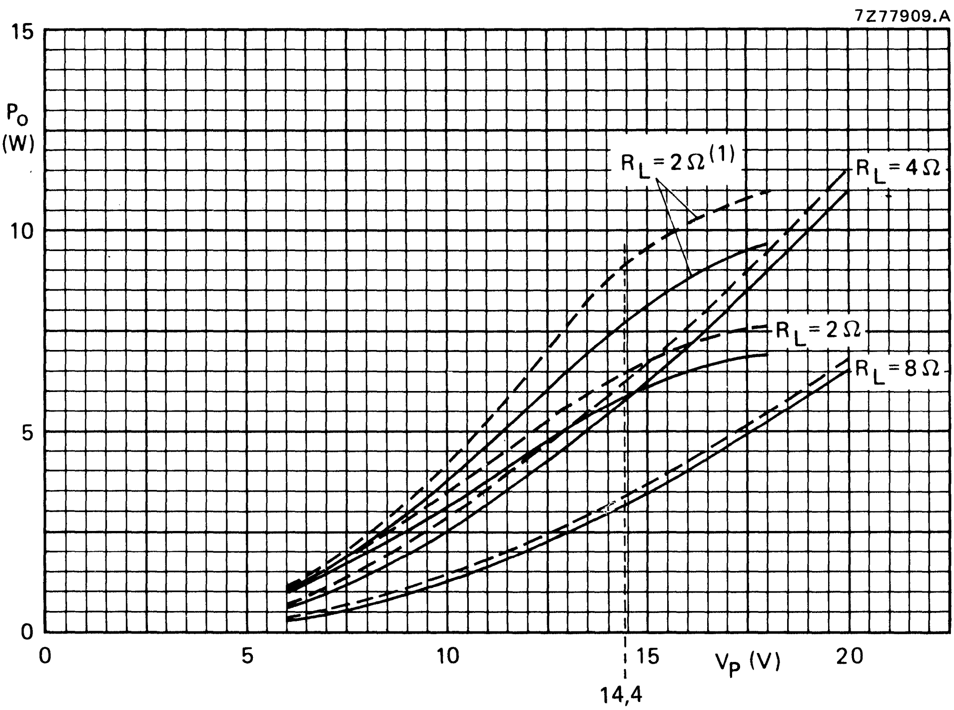


Fig. 4 Output power of the circuit of Fig. 3 as a function of the supply voltage with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\ \Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, d_{tot} = 10%, T_{amb} = 25 °C.

Fig. 5 See next page.
Total harmonic distortion in the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\ \Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, V_P = 14,4 V.

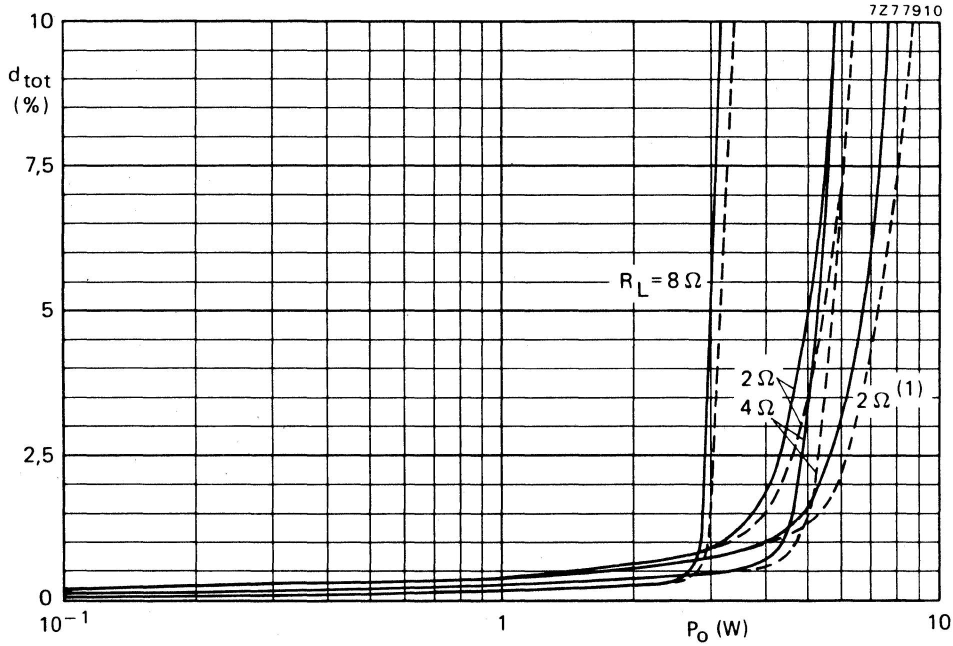


Fig. 5 For caption see preceding page.

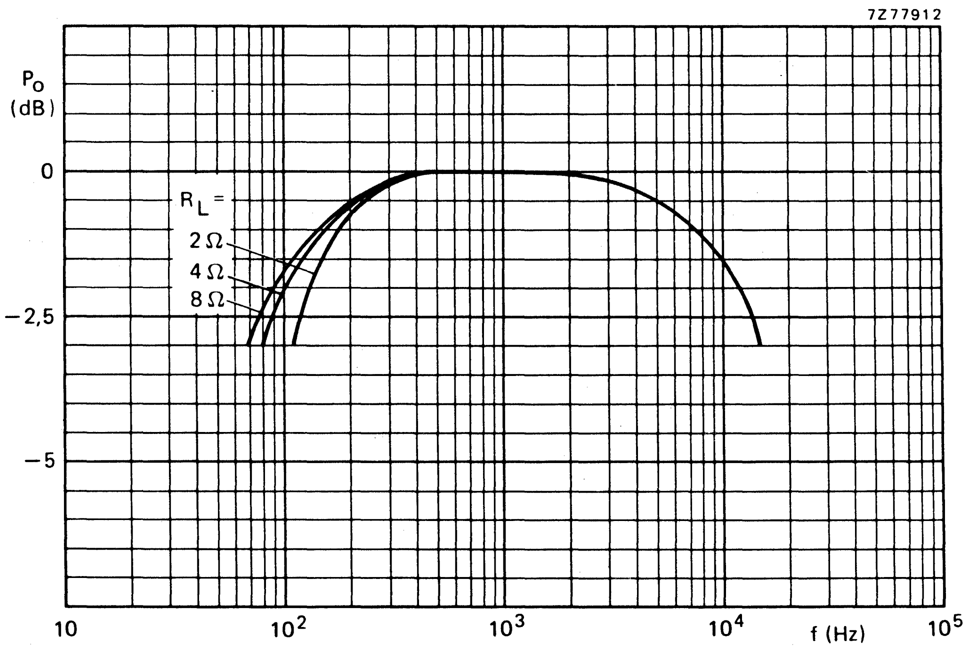


Fig. 6 Frequency characteristics of the circuit of Fig. 3 for three values of load impedance; typical values. P_o relative to 0 dB = 1 W; V_P = 14,4 V.

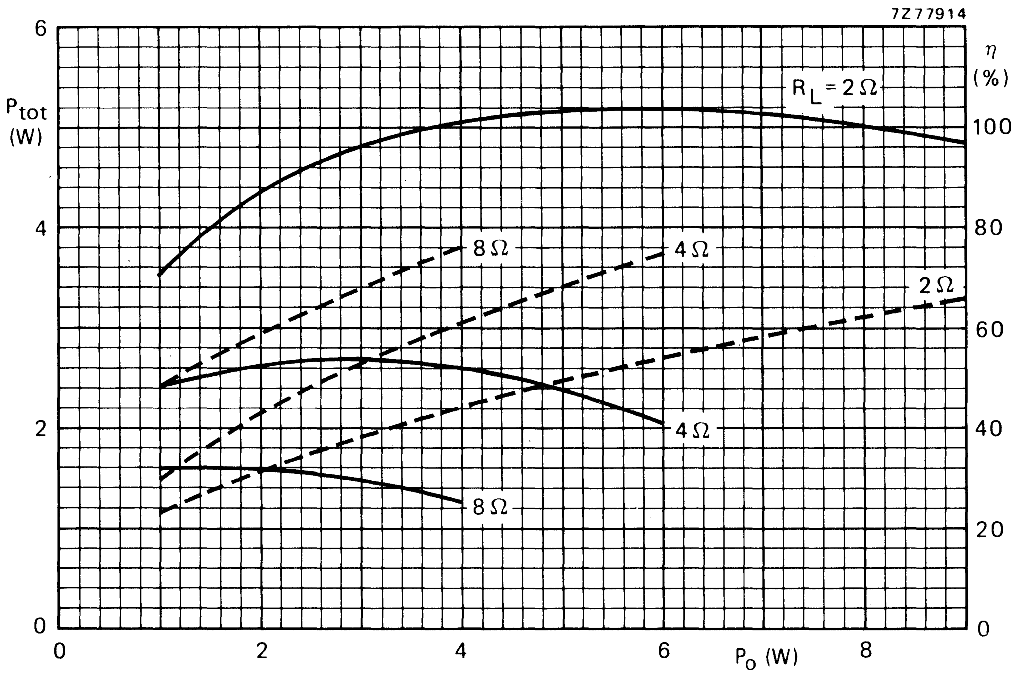


Fig. 7 Total power dissipation (solid lines) and the efficiency (dashed lines) of the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter (for $R_L = 2\ \Omega$ an external bootstrap resistor of 220 Ω has been used); typical values. V_P = 14,4 V; f = 1 kHz.

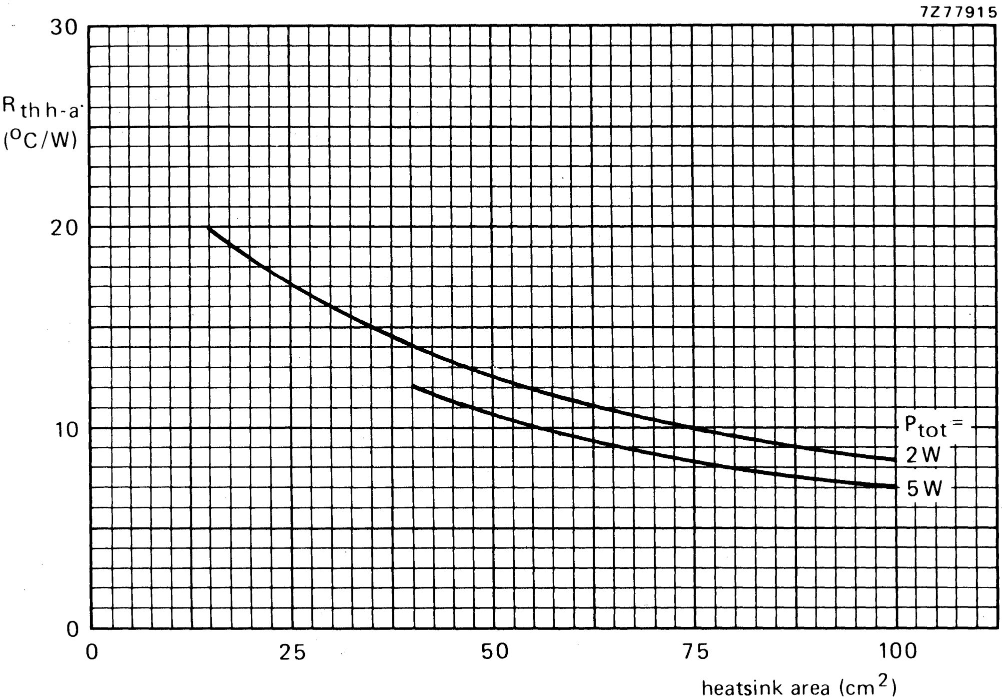


Fig. 8 Thermal resistance from heatsink to ambient of a 1,5 mm thick bright aluminium heatsink as a function of the single-sided area of the heatsink with the total power dissipation as a parameter.

APPLICATION INFORMATION

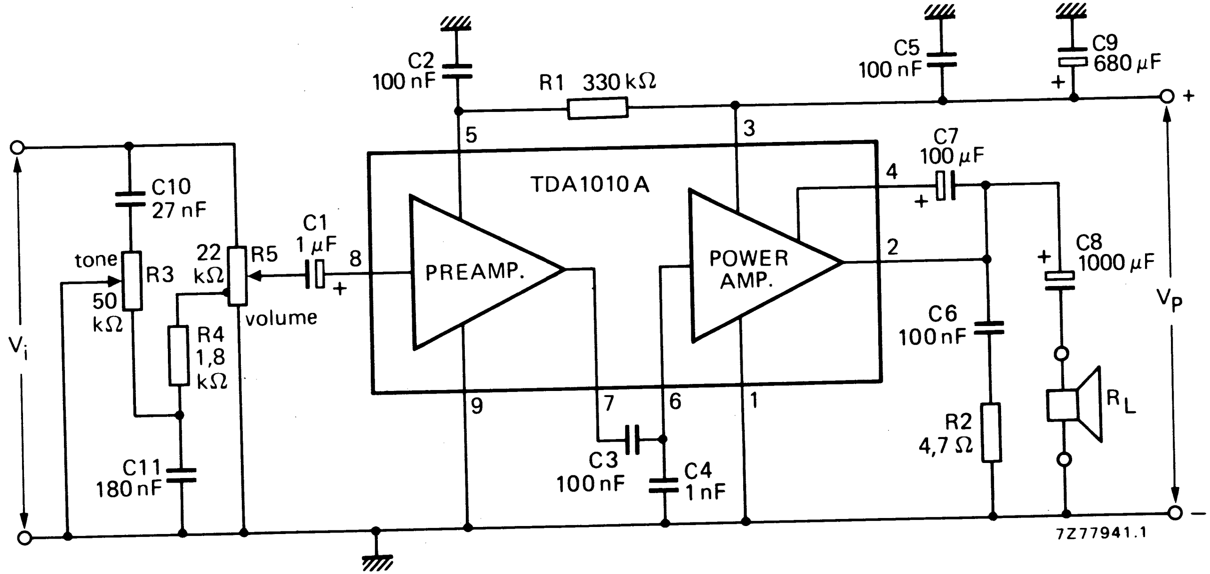


Fig. 9 Complete mono audio amplifier of a car radio.

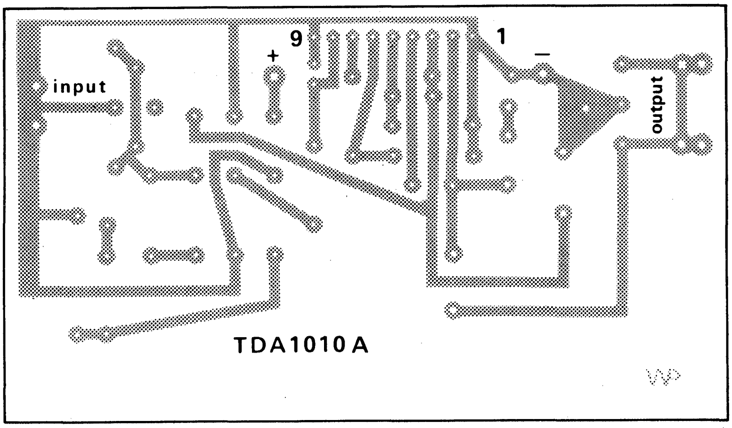


Fig. 10 Track side of printed-circuit board used for the circuit of Fig. 9; p.c. board dimensions 92 mm x 52 mm.

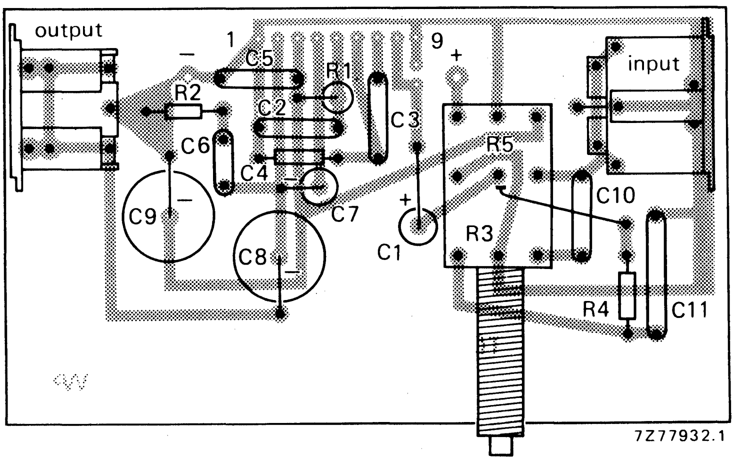


Fig. 11 Component side of printed-circuit board showing component layout used for the circuit of Fig. 9.

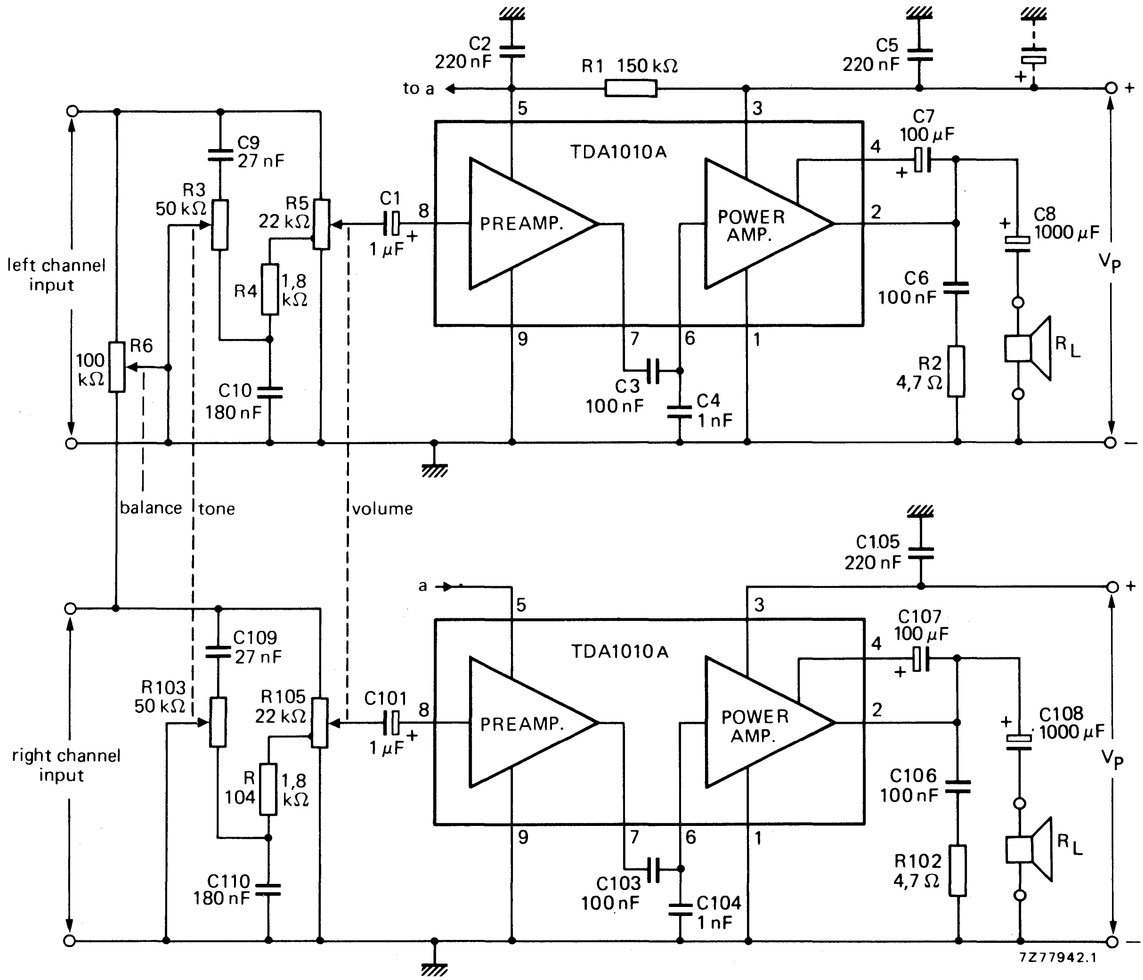


Fig. 12 Complete stereo car radio amplifier.

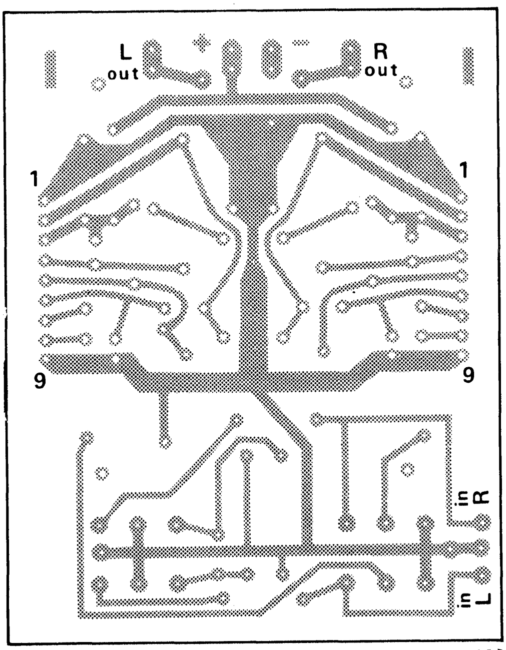


Fig. 13 Track side of printed-circuit board used for the circuit of Fig. 12; p.c. board dimensions 83 mm x 65 mm.

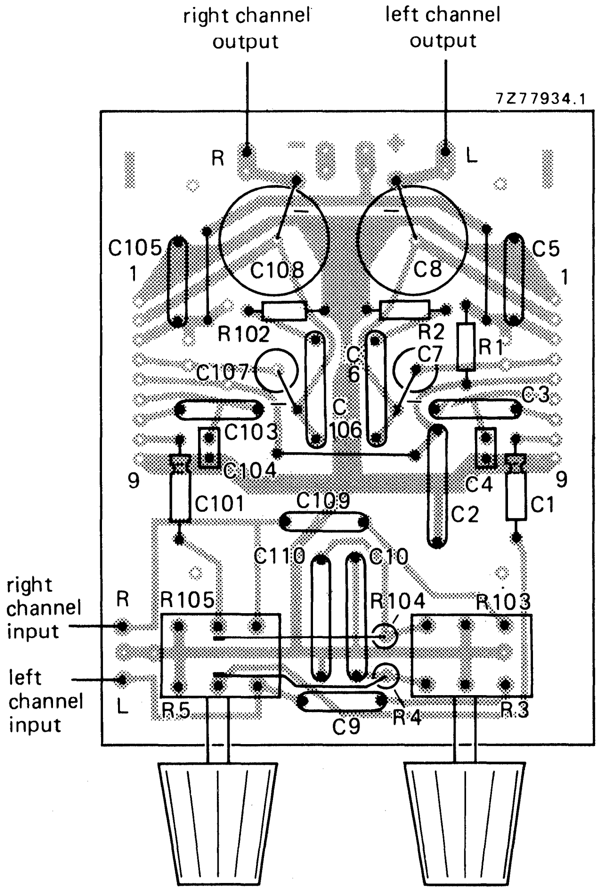


Fig. 14 Component side of printed-circuit board showing component layout used for the circuit of Fig. 12. Balance control is not on the p.c. board.

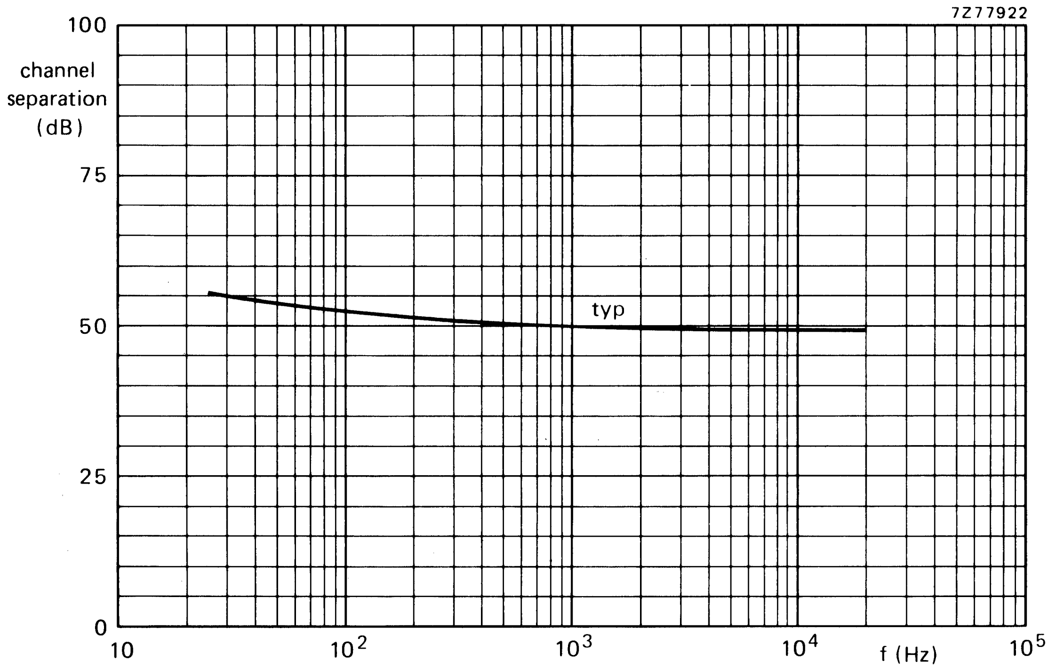


Fig. 15 Channel separation of the circuit of Fig. 12 as a function of the frequency.

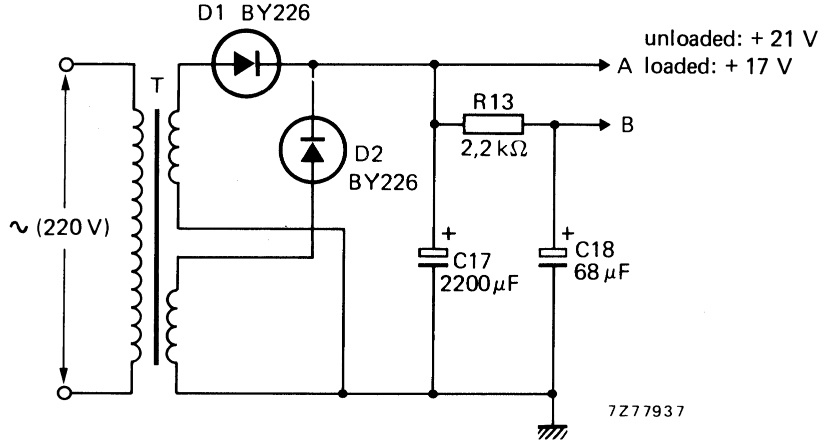


Fig. 16 Power supply of circuit of Fig. 17.

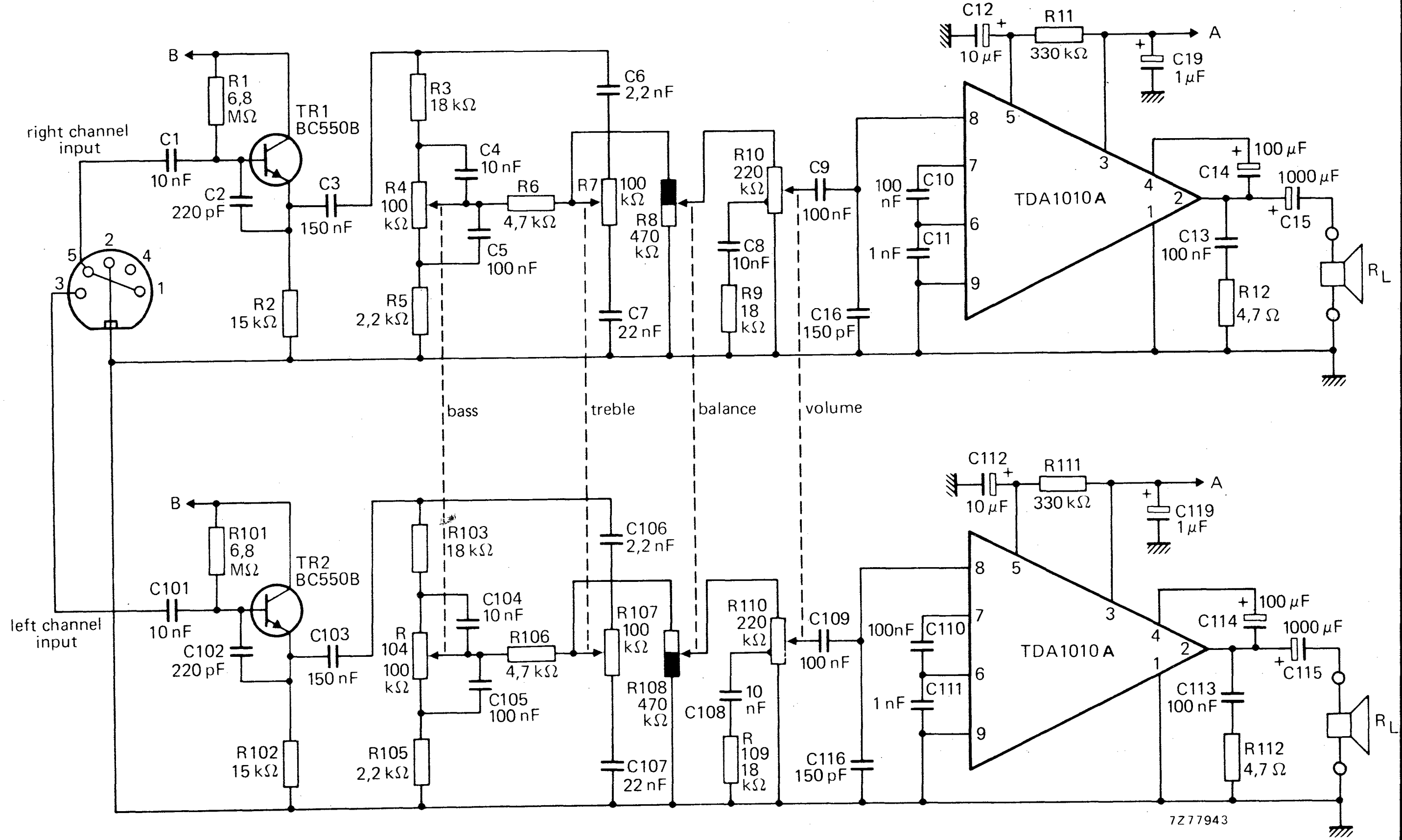


Fig. 17 Complete mains-fed ceramic stereo pick-up amplifier; for power supply see Fig. 16.

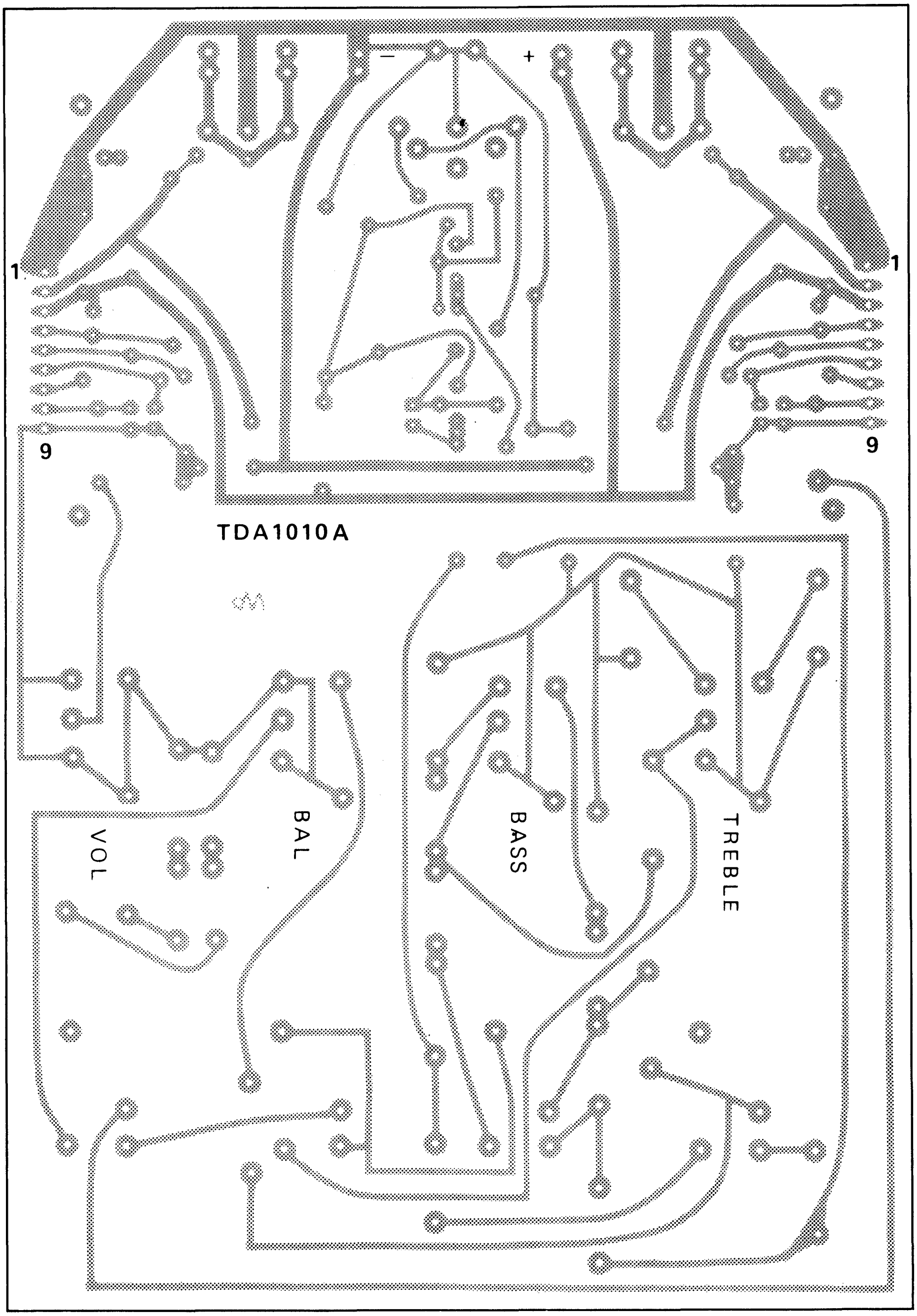


Fig. 18 Track side of printed-circuit board used for the circuit of Fig. 17 (Fig. 16 partly); p.c. board dimensions 169 mm x 118 mm.

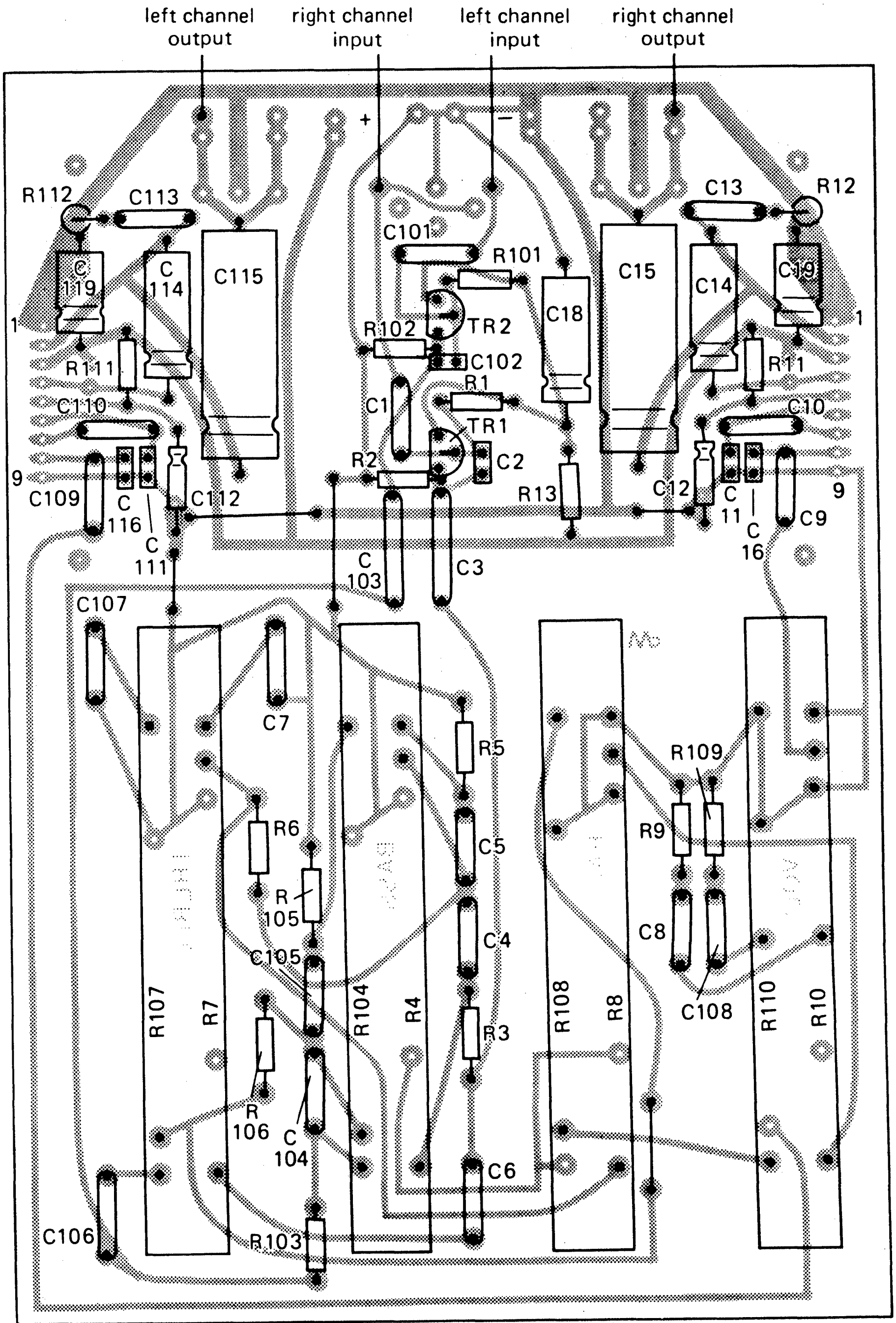


Fig. 19 Component side of printed-circuit board showing component layout used for the circuit of Fig. 17 (Fig. 16 partly).

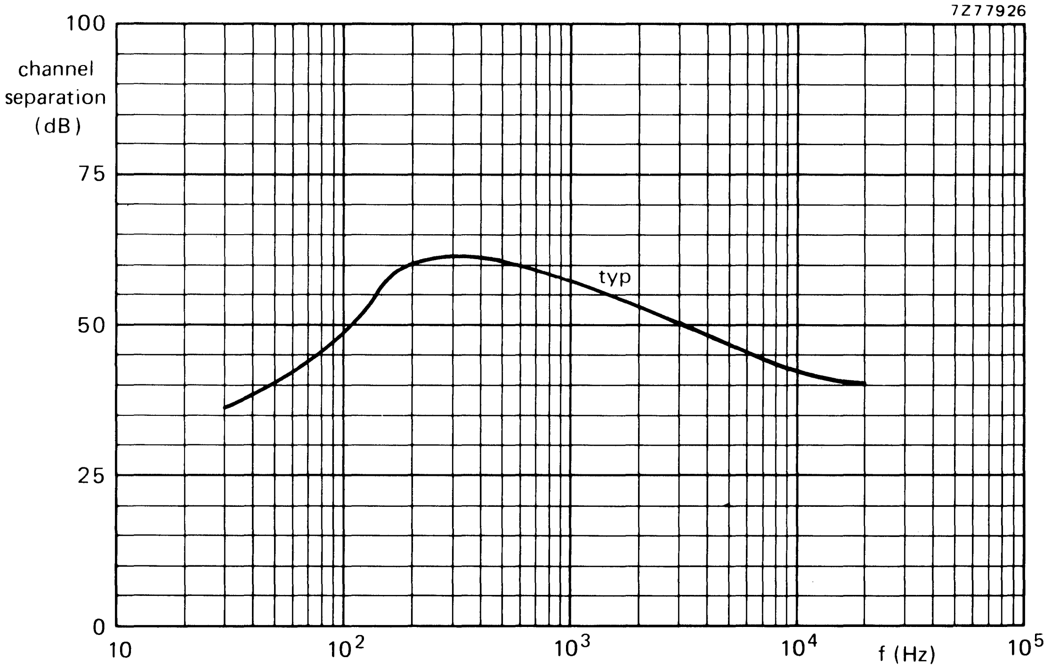


Fig. 20 Channel separation of the circuit of Fig. 17 as a function of frequency.

1 to 4W audio amplifier with preamplifier — TDA1015

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 18	V
Peak output current	I_{OM}	max.	2,5	A
Output power at d_{tot} = 10%				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,3	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	>	100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

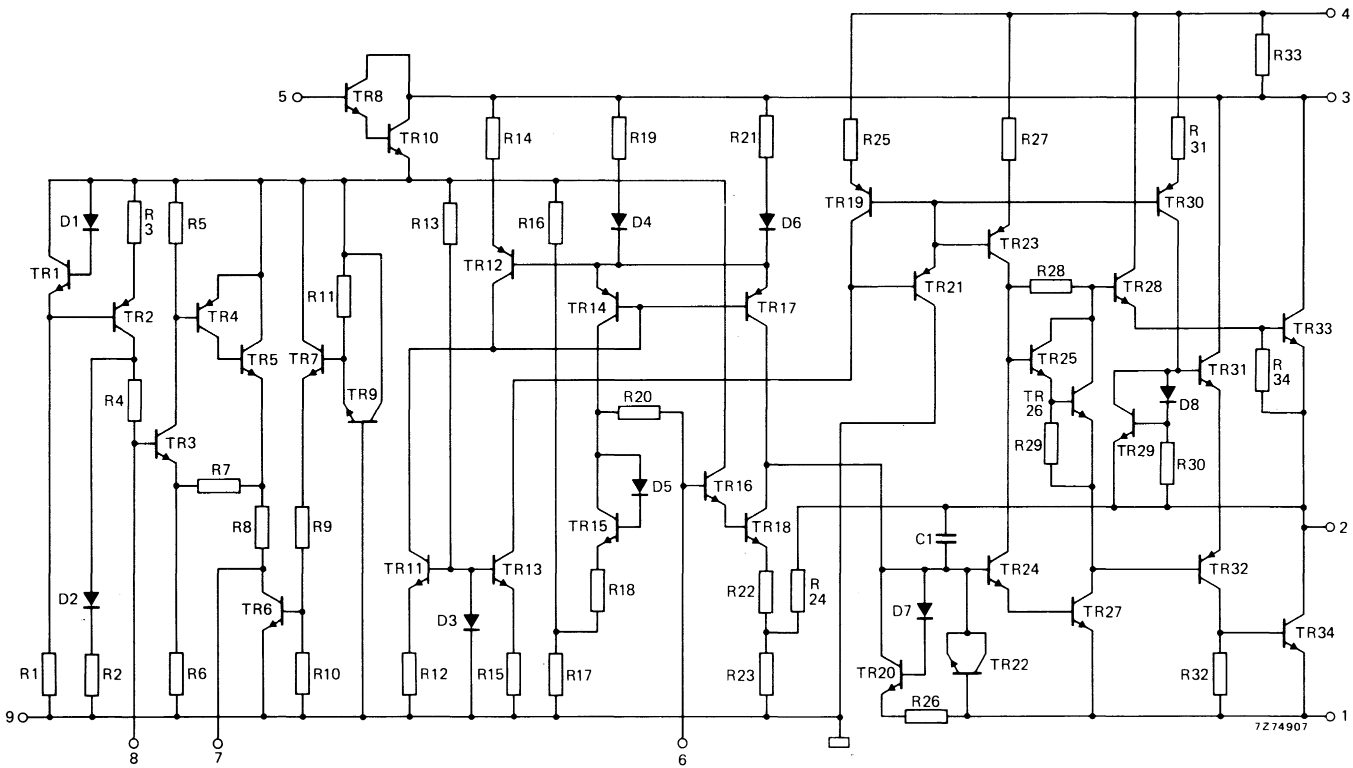


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Peak output current	I_{OM}	max.	2,5	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100	hours

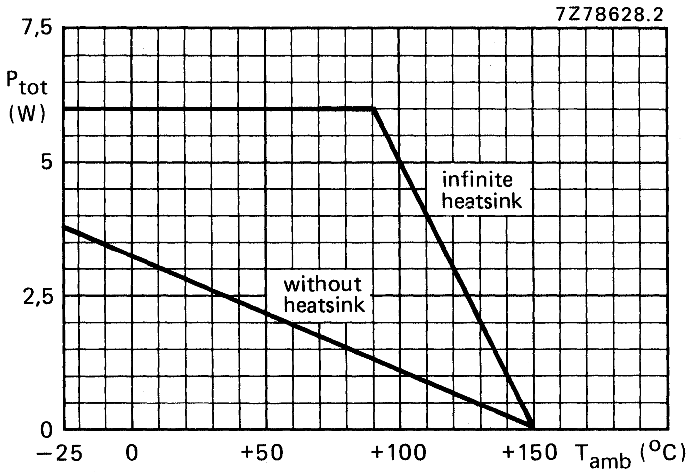


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 45 °C maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150-45}{1,8} = 58\ \text{K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 45 K/W, so no external heatsink is required.

D.C. CHARACTERISTICS

Supply voltage range	V_P		3,6 to 18	V
Repetitive peak output current	I_{ORM}	<	2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ.	14	mA
		<	25	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)				
with bootstrap:				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
without bootstrap:				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	3,0	W
Voltage gain:				
preamplifier (note 2)	G_{v1}	typ.	23	dB
power amplifier	G_{v2}	typ.	29	dB
total amplifier	$G_{v\,tot}$	typ.	52	dB
			49 to 55	dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ.	0,3	%
		<	1,0	%
Frequency response; –3 dB (note 3)	B		60 Hz to 15	kHz
Input impedance:				
preamplifier (note 4)	$\|Z_{i1}\|$	>	100	kΩ
		typ.	200	kΩ
power amplifier	$\|Z_{i2}\|$	typ.	20	kΩ
Output impedance preamplifier	$\|Z_{o1}\|$	typ.	1	kΩ
Output voltage preamplifier (r.m.s. value)				
d_{tot} < 1% (note 2)	$V_{o(rms)}$	typ.	0,8	V
Noise output voltage (r.m.s. value; note 5)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,5	mV
Noise output voltage at f = 500 kHz (r.m.s. value)				
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ.	8	μV
Ripple rejection (note 6)				
f = 100 Hz	RR	typ.	38	dB

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_O = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

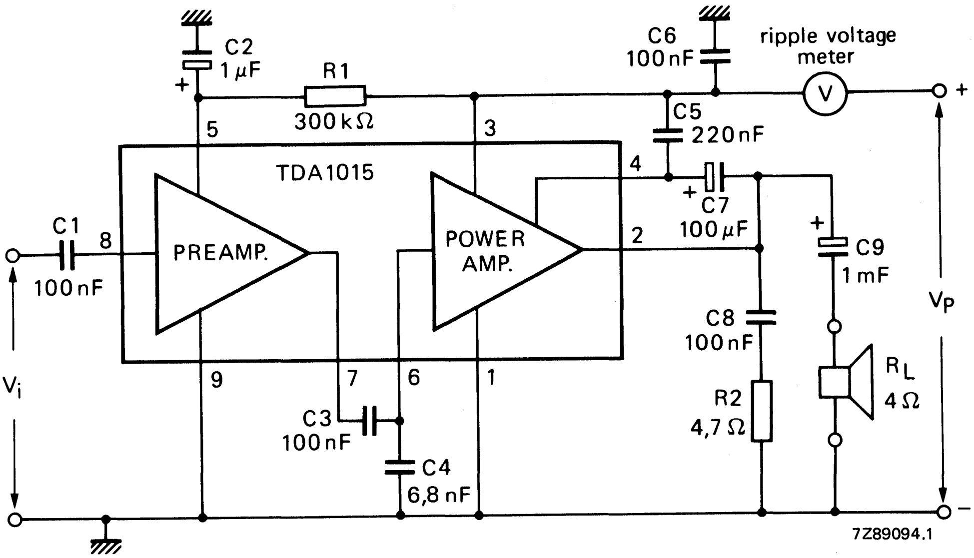


Fig. 3 Test circuit.

1 to 4W audio amplifier with preamplifier

TDA1015

APPLICATION INFORMATION

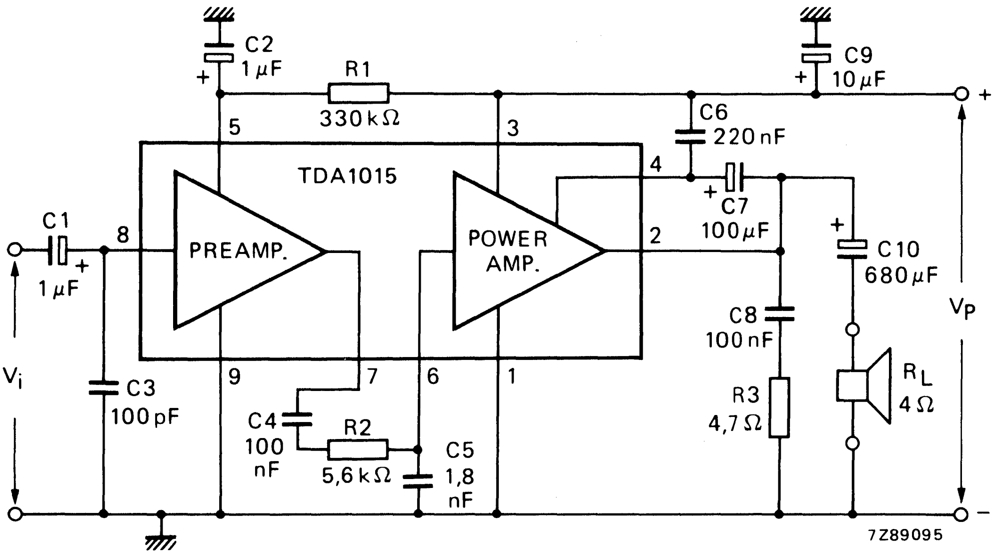


Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

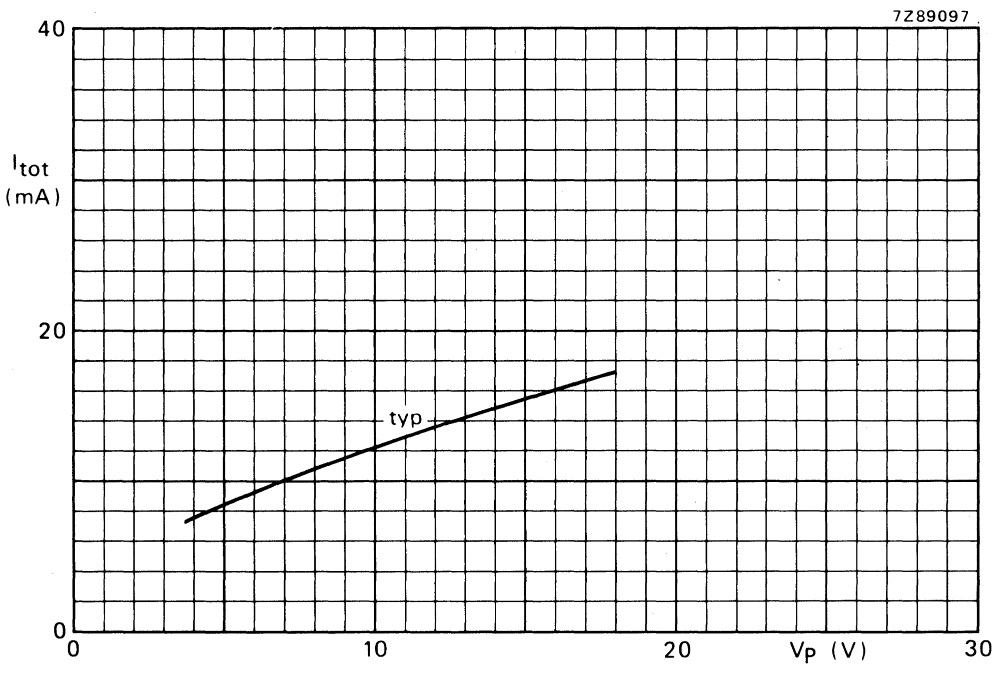


Fig. 5 Total quiescent current as a function of supply voltage.

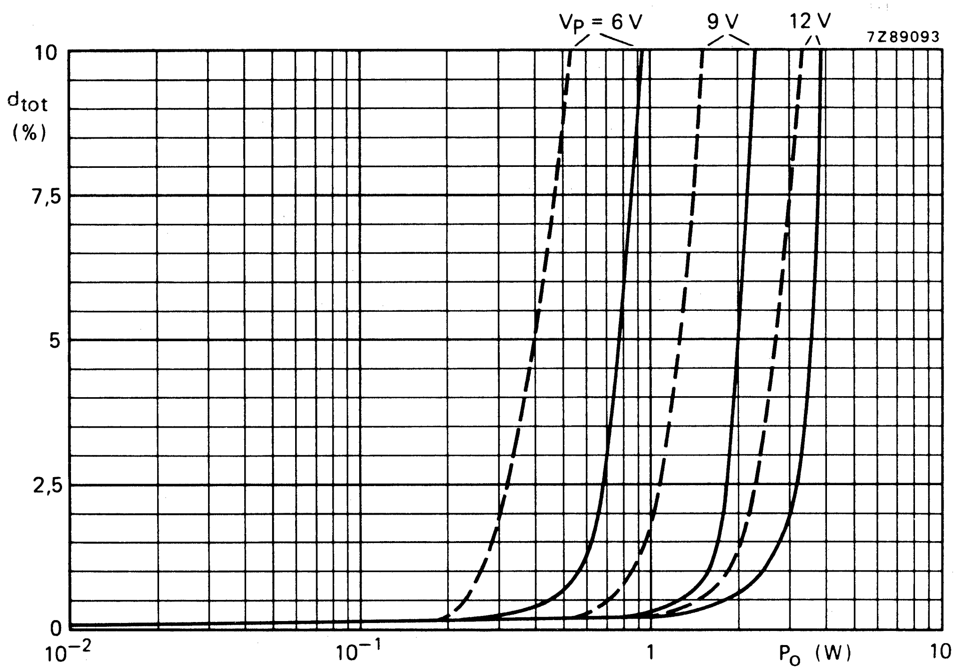


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

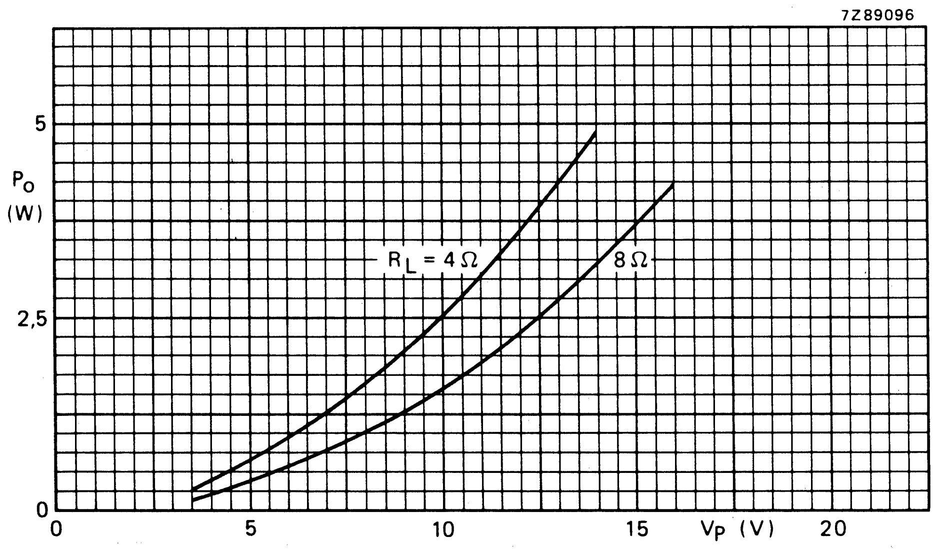


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

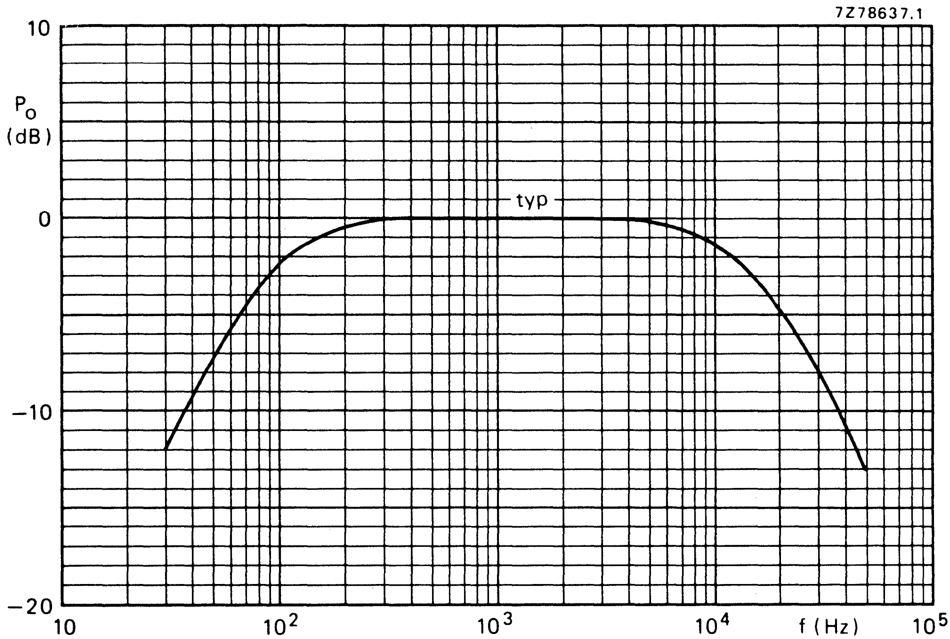


Fig. 8 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

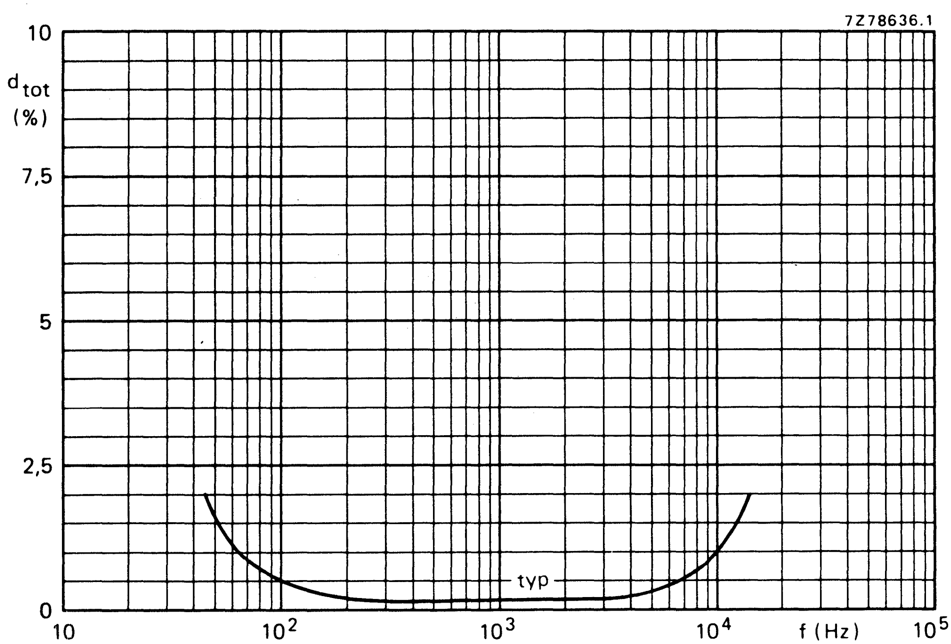


Fig. 9 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

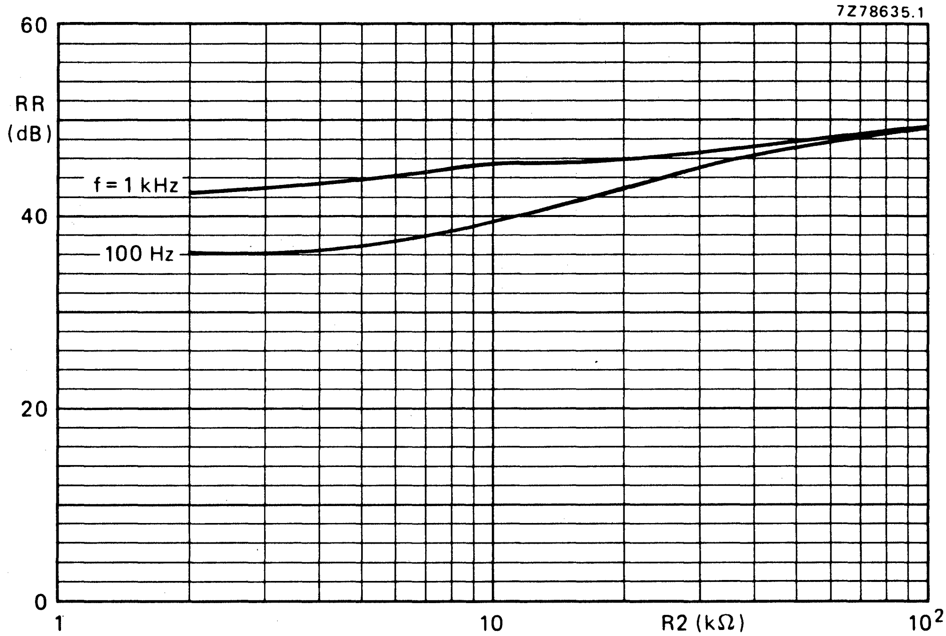


Fig. 10 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

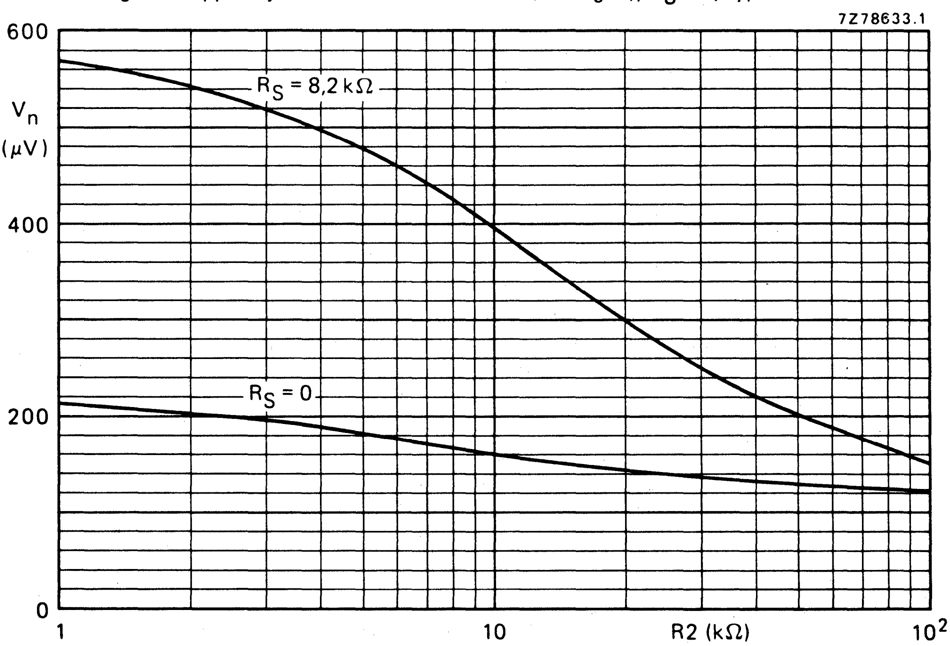


Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

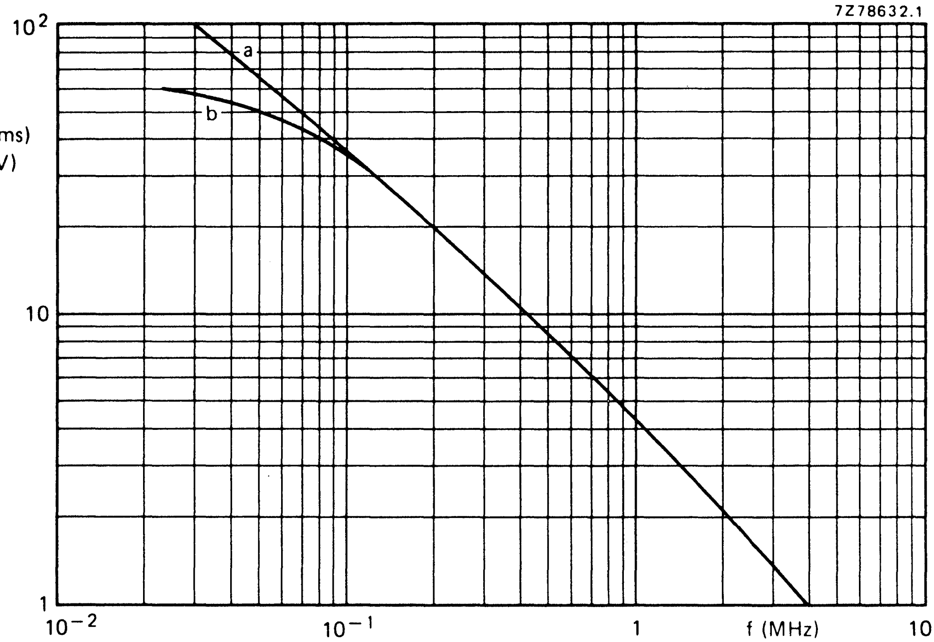


Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

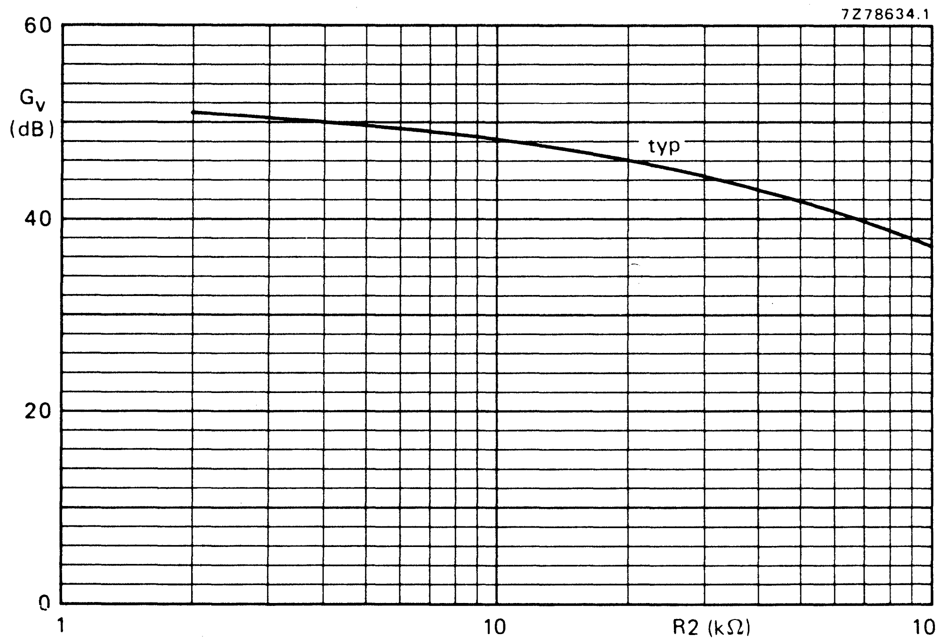


Fig. 13 Voltage gain as a function of R2 (see Fig. 4).

2 to 6W audio power amplifier with preamplifier TDA1011A

The TDA1011A is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the low applicable supply voltage of 5,4 V permits 9 V applications. The power amplifier has an inverted input/output which makes the circuit optimal for applications with active tone control and spatial stereo. Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		5,4 to 20	V
Peak output current	I_{OM}	max.	3	A
Output power at d_{tot} = 10%				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\|Z_i\|$	>	100	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

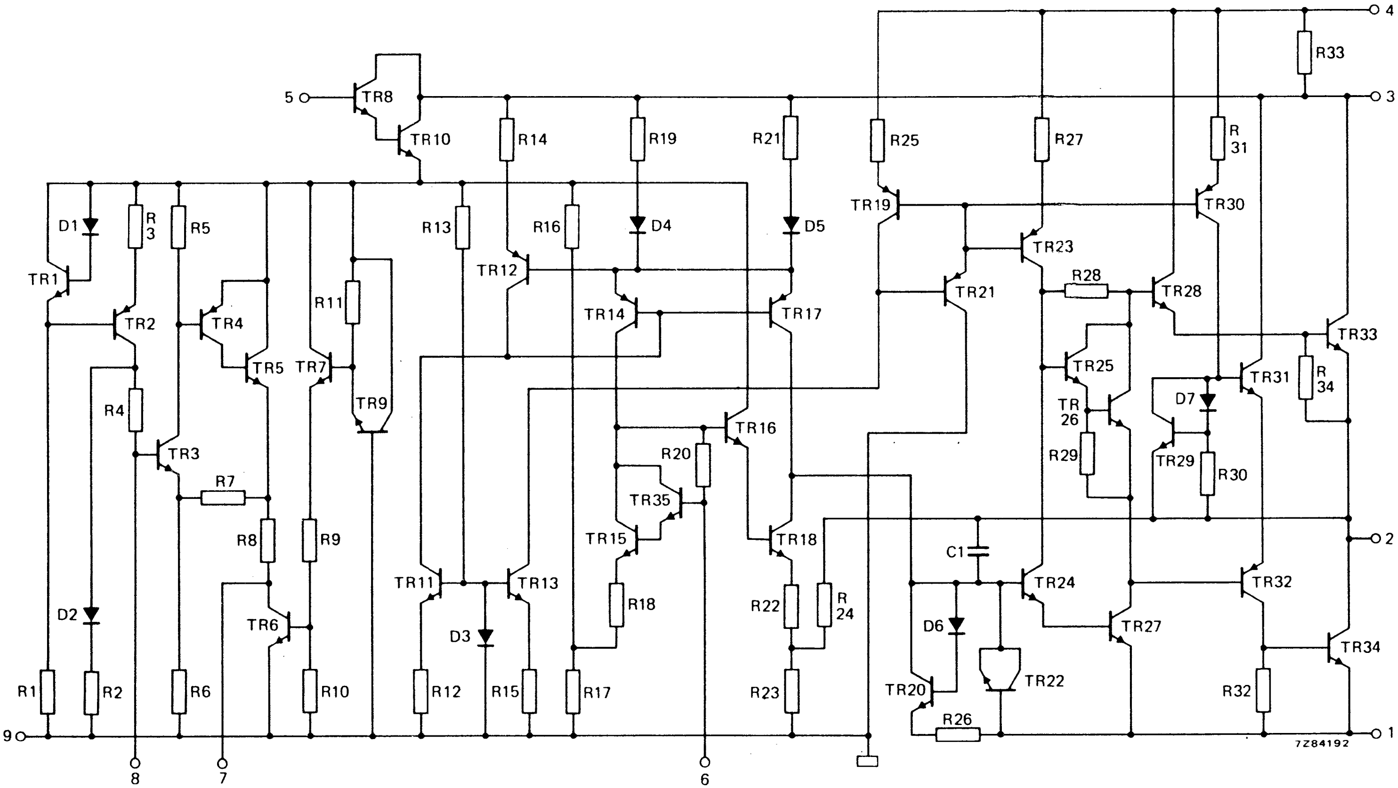


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24	V
Peak output current	I_{OM}	max.	3	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature	T_{amb}	−25 to + 150		°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100	hours

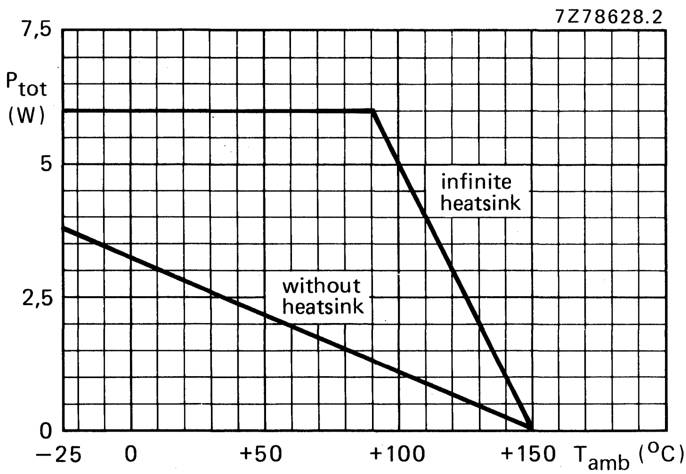


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 60 °C maximum; P_o = 3,8 W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150-60}{1,8} = 50\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 50 − (10 + 1) = 39 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		5,4 to 20	V
Repetitive peak output current	I_{ORM}	<	2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ.	14	mA
		<	22	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)				
with bootstrap:				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	>	3,6	W
		typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
without bootstrap:				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	3,5	W
Voltage gain:				
preamplifier (note 2)	G_{v1}	typ.	23	dB
			21 to 25	dB
power amplifier (note 3)	G_{v2}	typ.	29	dB
total amplifier (note 3)	$G_{v\ tot}$	typ.	52	dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ.	0,3	%
		<	1	%
Frequency response; −3 dB (note 4)	B		60 Hz to 15	kHz
Input impedance:				
preamplifier (note 5)	$\lvert Z_{i1} \rvert$	>	100	kΩ
		typ.	200	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ.	1	kΩ
Output voltage preamplifier (r.m.s. value)				
d_{tot} < 1% (note 2)	$V_{o(rms)}$	>	1,2	V
Noise output voltage (r.m.s. value; note 6)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,5	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,8	mV
Noise output voltage at f = 500 kHz (r.m.s. value)				
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ.	8	μV
Ripple rejection (note 6)				
f = 1 to 10 kHz	RR	typ.	42	dB
f = 100 Hz; C2 = 1 μF	RR	>	35	dB
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	35	mA
Stand-by current at maximum V_P (note 8)	I_{sb}	<	100	μA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured with R2 = 20 kΩ.
4. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
5. Independent of load impedance of preamplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The total current when disconnecting pin 5 or short-circuited to ground (pin 9).
9. The tab must be electrically floating or connected to the substrate (pin 9).

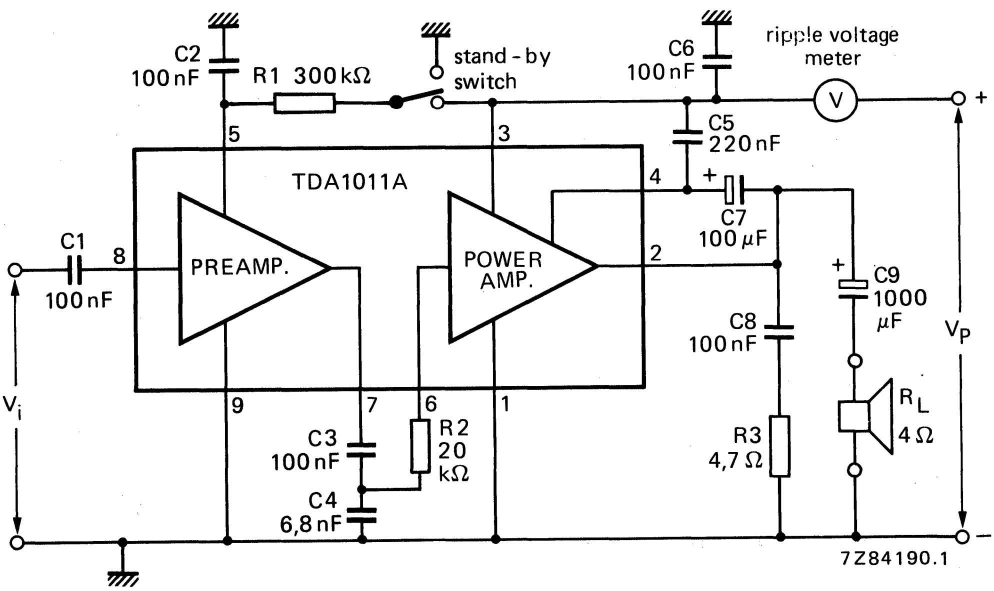


Fig. 3 Test circuit.

APPLICATION INFORMATION

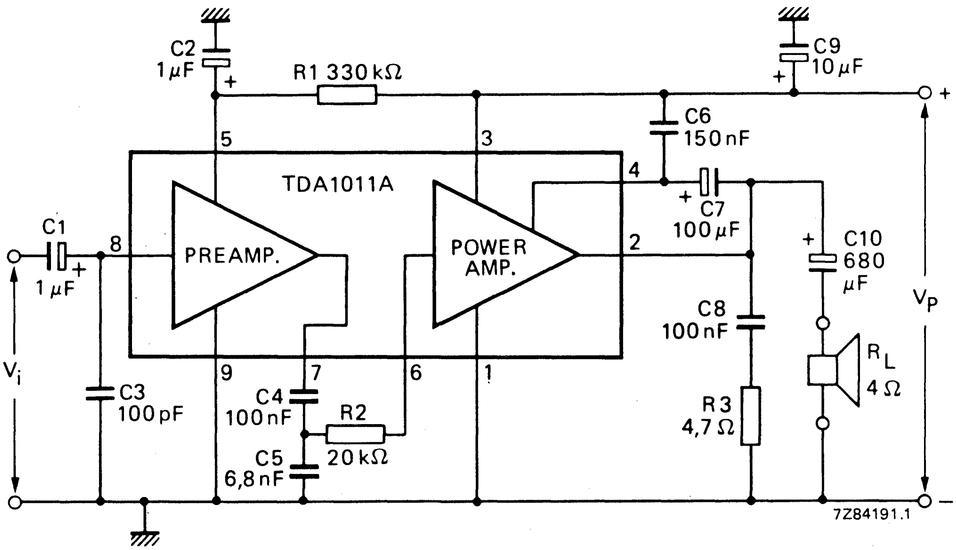


Fig. 4 Circuit diagram of a 4 W amplifier.

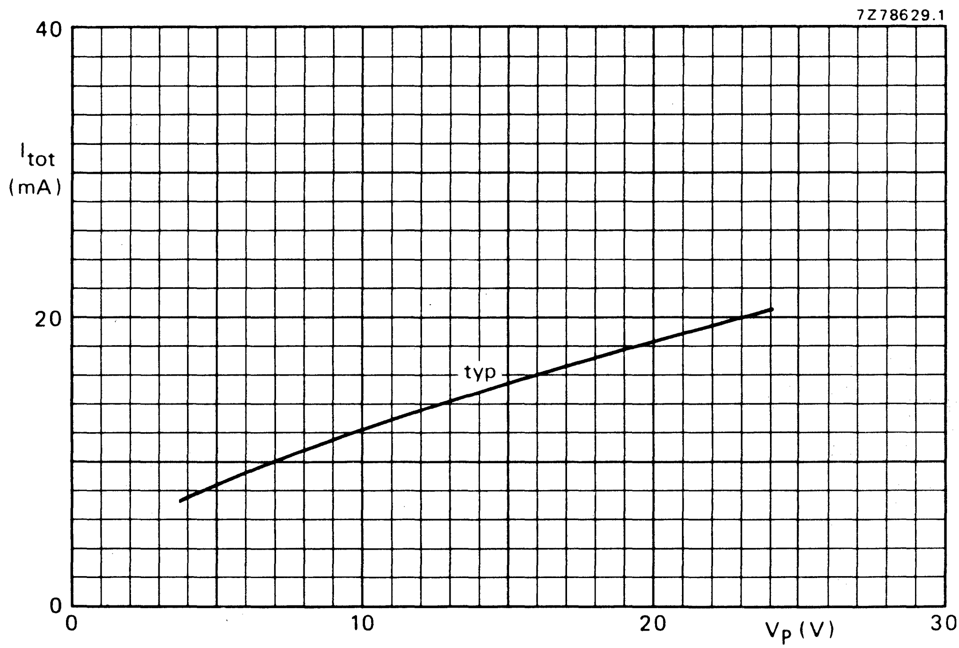


Fig. 5 Total quiescent current as a function of supply voltage.

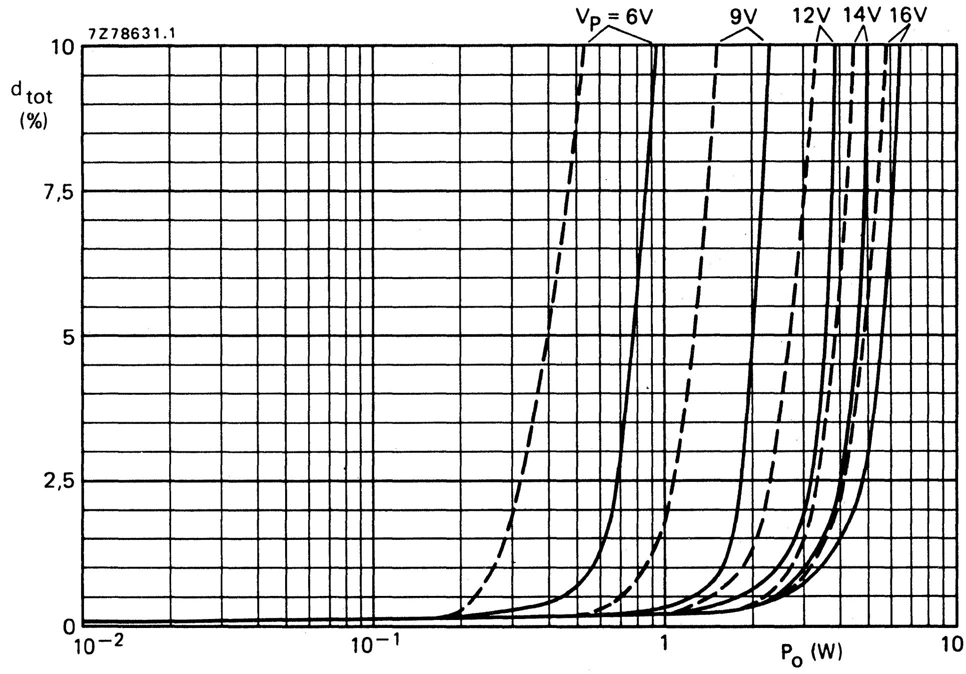


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

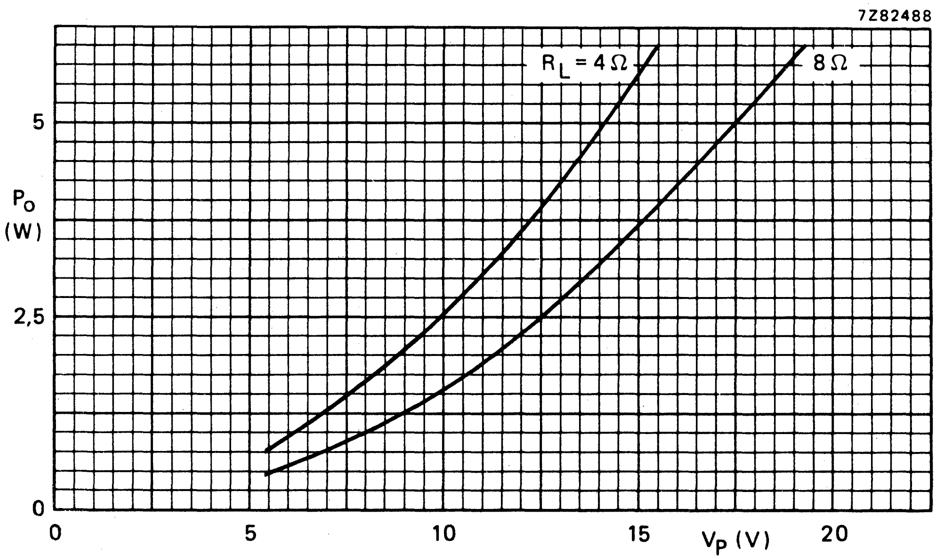


Fig. 7, Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C1

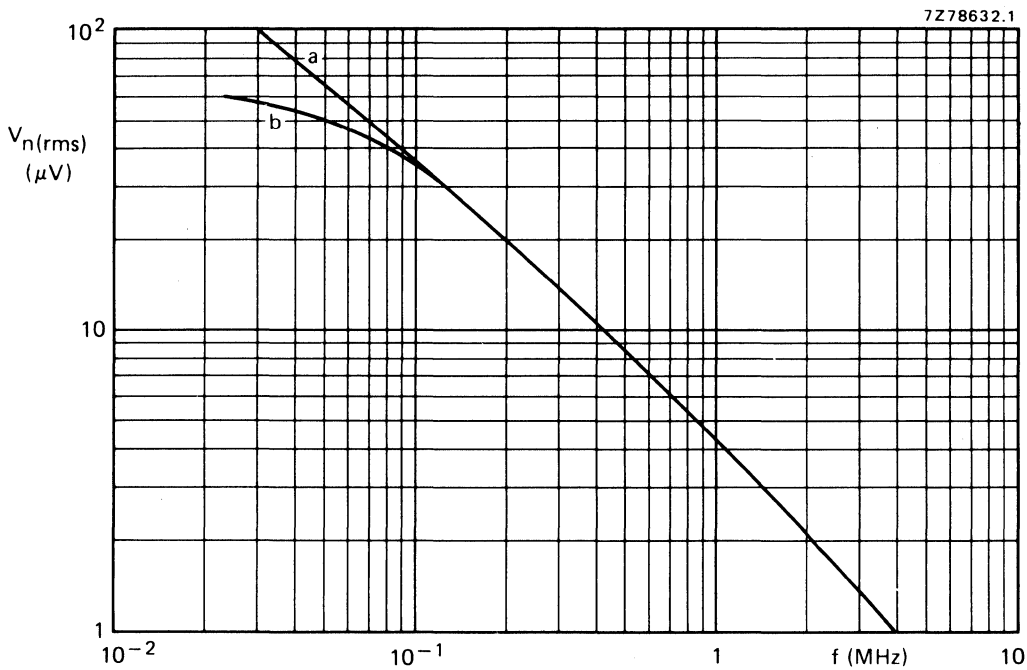


Fig. 8 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

4W amplifier with DC volume control

TDA1013B

GENERAL DESCRIPTION

The TDA1013B is an integrated audio amplifier circuit with DC volume control, encapsulated in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit ideal for applications in mains and battery-fed apparatus such as television receivers and record players.

The DC volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control is by means of a DC voltage variable between 2 and 6.5 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop. This device requires only a few external components and offers stability and performance.

Features

- Few external components
- Wide supply voltage range
- Wide control range
- Pin compatible with TDA1013A
- Fixed gain
- High signal-to-noise ratio
- Thermal protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10	18	40	V
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	0.1	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
DC volume control unit						
Gain control range		$\|\Delta G_V\|$	80	–	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	45	55	mV
Input impedance (pin 8)		$\|Z_i\|$	23	29	35	kΩ

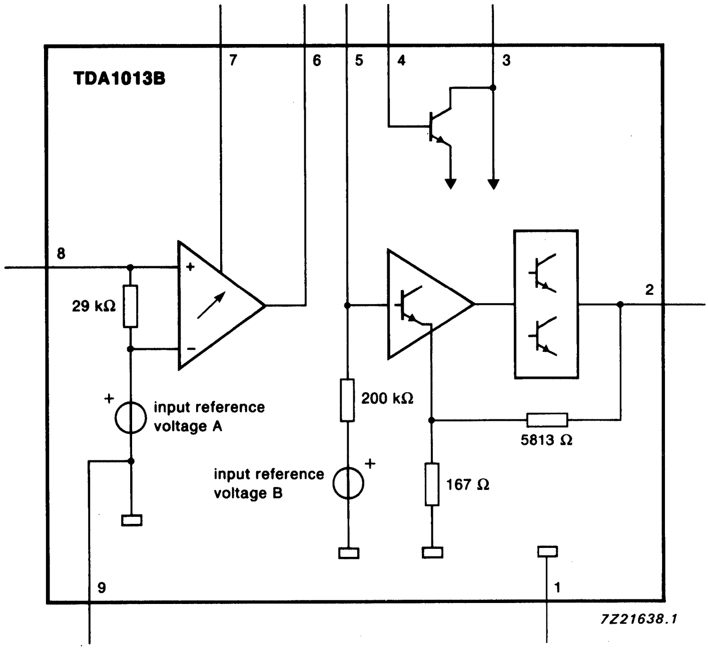


Fig.1 Block diagram.

PINNING

1 signal ground
2 amplifier output
3 supply voltage
4 electronic filter
5 amplifier input
6 control unit output
7 control voltage
8 control unit input
9 power ground

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	40	V
Non-repetitive peak output current	I_{OSM}	–	3	A
Repetitive peak output current	I_{ORM}	–	1.5	A
Storage temperature range	T_{stg}	–65	+ 150	°C
Crystal temperature	T_c	–	+ 150	°C
Total power dissipation	P_{tot}	see Fig. 2		

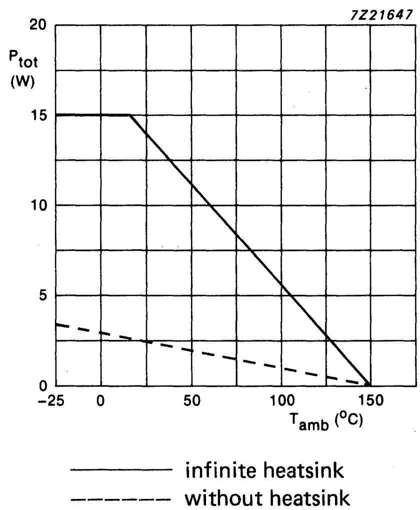


Fig.2 Power derating curve.

HEATSINK DESIGN EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C; T_c = 150 °C (max.); for a 4 W application, the maximum dissipation is approximately 2.5 W. The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} =$$

$$\frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2.5} = 36\ K/W$$

Since $R_{th\ j\text{-}tab}$ = 9 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 – (9 + 1) = 26 K/W.

CHARACTERISTICS

V_P = 18 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; see Fig.10; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	10	18	40	V
Total quiescent current		I_{tot}	–	25	60	mA
Noise output voltage	note 1					
at maximum gain	R_S = 0 Ω	V_n	–	0.5	–	mV
at maximum gain	R_S = 5 kΩ	V_n	–	0.6	1.4	mV
at minimum gain	R_S = 0 Ω	V_n	–	0.25	–	mV
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	1.0	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
Input impedance (pin 5)		$\|Z_i\|$	100	200	500	kΩ
Power bandwidth		B_P	–	30 to 40 000	–	Hz
DC volume control unit						
Gain control range		$\|\Delta G_v\|$	80	90	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	44	55	mV
Input impedance (pin 8)		$\|Z_i\|$	23	29	35	kΩ
Output impedance (pin 6)		$\|Z_o\|$	45	60	75	Ω

Note to the characteristics

1. Measured in a bandwidth in accordance with IEC 179, curve 'A'.

APPLICATION INFORMATION

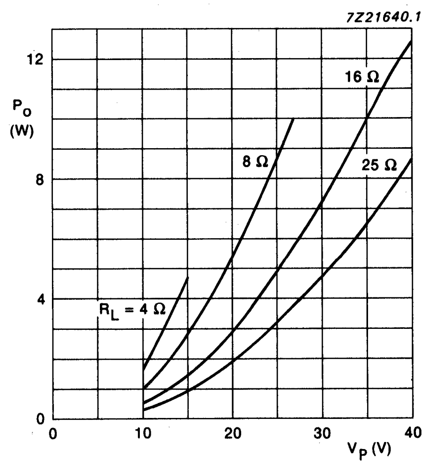


Fig.3 Output power as a function of supply voltage; f = 1 kHz; THD = 10% and control voltage (V_7) = 6.5 V.

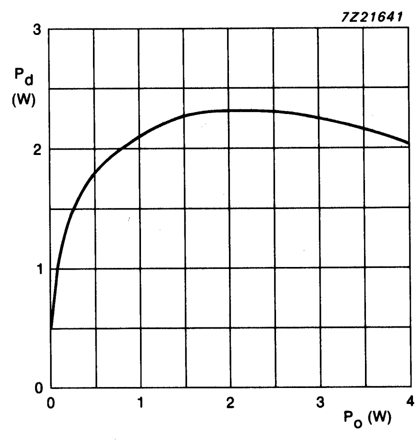


Fig.4 Power dissipation as a function of output power; V_P = 18 V; f = 1 kHz; R_L = 8 Ω and control voltage (V_7) = 6.5 V.

APPLICATION INFORMATION (continued)

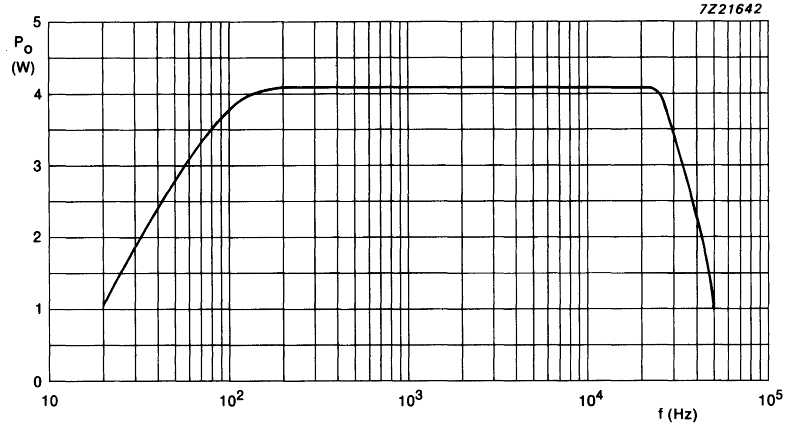


Fig.5 Power bandwidth; V_P = 18 V; R_L = 8 Ω; THD = 10% and control voltage (V_7) = 6.5 V.

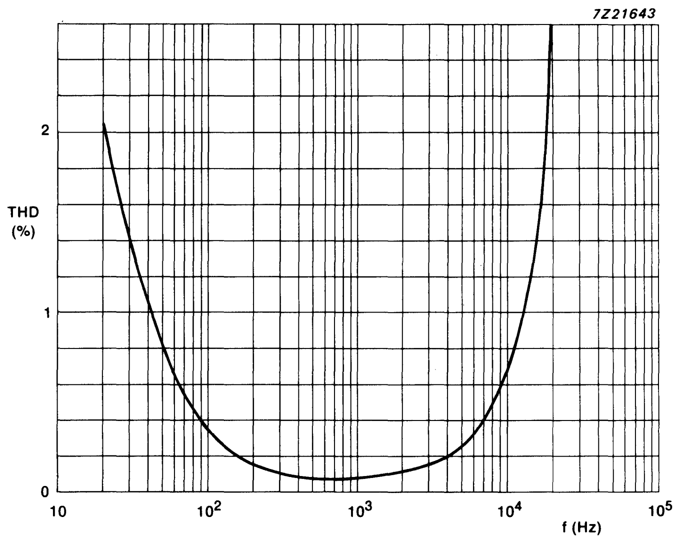


Fig.6 Total harmonic distortion as a function of frequency; V_P = 18 V; R_L = 8 Ω; P_o = 2.5 W and control voltage = 6.5 V.

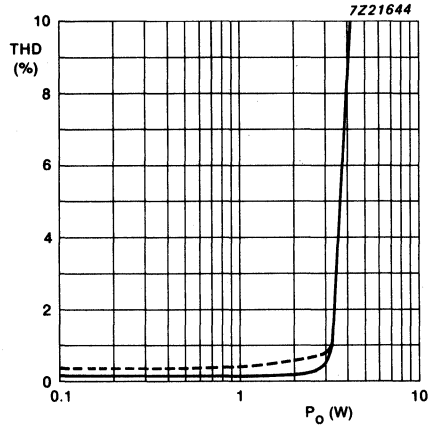


Fig.7 Total harmonic distortion as a function of output power;
V_P = 18 V; R_L = 8 Ω and control voltage = 6.5 V.

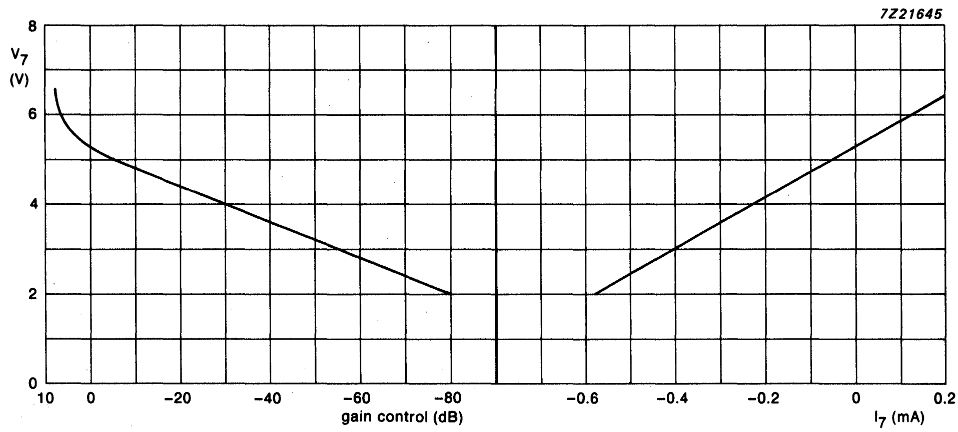


Fig.8 Typical control curve.

APPLICATION INFORMATION (continued)

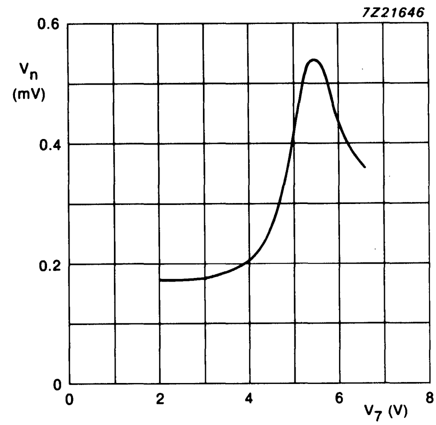
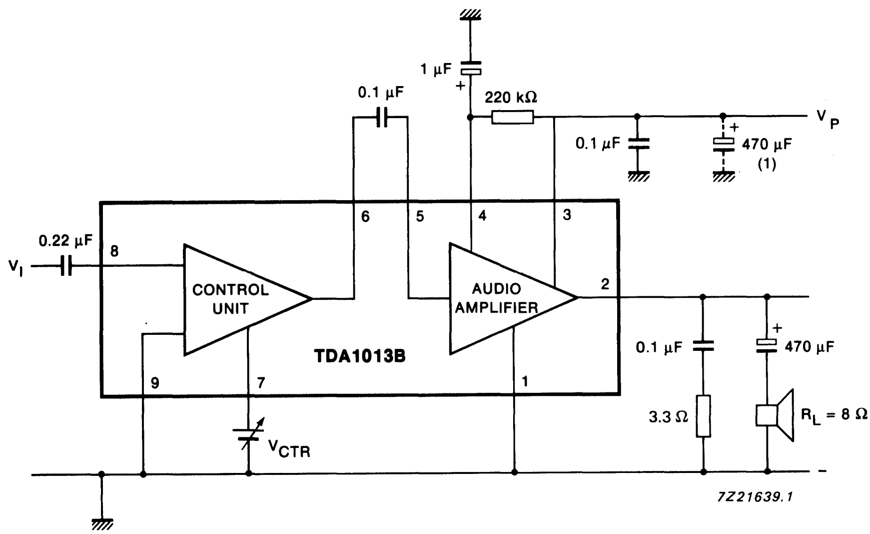


Fig.9 Noise output voltage as a function of the control voltage; V_P = 18 V; R_L = 8 Ω (in accordance with IEC 179, curve 'A').



(1) Belongs to power supply circuitry.

Fig.10 Application diagram.

1 Watt low voltage audio power amplifier TDA7052

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	39	40	41	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

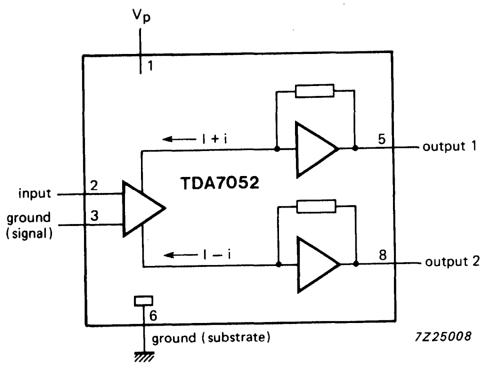


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

FUNCTIONAL DESCRIPTION

The TDA7052 is a mono output amplifier designed for battery-fed portable audio applications, such as tape recorders and radios.
The gain is fixed internally at 40 dB. A large number of tape recorders and radios are still designed for mono sound, plus a space-saving trend by reduction of the number of battery cells. This means a decrease in supply voltage which results in an reduction of output power. To compensate for this reduction, the TDA7052 uses the Bridge-Tied-Load principle (BTL) which can deliver an output power of 1,2 W (THD = 10%) into an 8 Ω load with a power supply of 6 V. The load can be short-circuited at each signal excursion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	18	V
Non-repetitive peak output current	I_{OSM}	–	1,5	A
Total power dissipation	P_{tot}	see Fig. 2		
Crystal temperature	T_c	–	150	°C
Storage temperature range	T_{stg}	–65	+ 150	°C

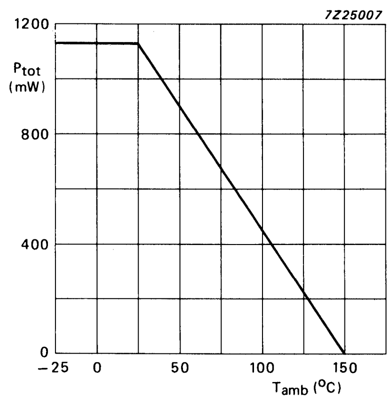


Fig. 2 Power derating curve.

POWER DISSIPATION

Assume V_P = 6 V; R_L = 8 Ω; T_{amb} = 50 °C maximum.
The maximum sinewave dissipation is 0,9 W.

$$R_{th\,j\text{-}a} = \frac{150 - 50}{0,9} \approx 110 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 110 K/W, so no external heatsink is required.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	39	40	41	dB
Output power	THD = 10%	P_o	*	1,2	–	W
Noise output voltage (RMS value)						
	note 1	$V_{no(rms)}$	–	150	300	μV
	note 2	$V_{no(rms)}$	–	60	–	μV
Frequency response		f_r	–	20 Hz to 20 kHz	–	Hz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage pin 5 to 8	R_S = 5 kΩ	ΔV_{5-8}	–	–	100	mV
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%
Input impedance		$\|Z_I\|$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA

Notes to the characteristics

1. The unweighted RMS noise output voltage is measured at a bandwidth of 60 Hz to 15 kHz with a source impedance (R_S) of 5 kΩ.
2. The RMS noise output voltage is measured at a bandwidth of 5 kHz with a source impedance of 0 Ω and a frequency of 500 kHz. With a practical load (R = 8 Ω; L = 200 μH) the noise output current is only 100 nA.
3. Ripple rejection is measured at the output with a source impedance of 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage = 200 mV (RMS value) is applied to the positive supply rail.

APPLICATION INFORMATION

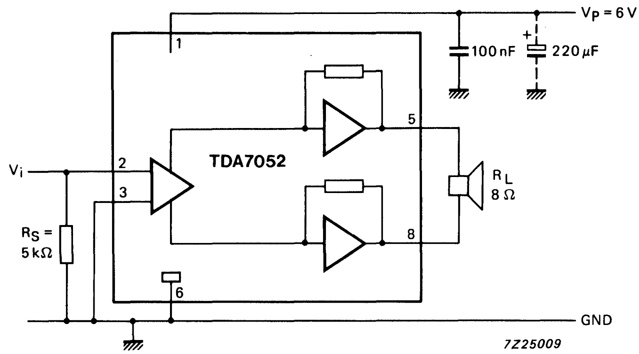


Fig. 3 Application diagram.

1-Watt low voltage audio power amp with DC volume control

TDA7052A/AT

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control. They are designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7052A	8	DIL	plastic	SOT97
TDA7052AT	8	mini-pack	plastic	SOT96A

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		4.5	–	18	V
P_O	output power					
	in 8 Ω (TDA7052A)	$V_P = 6$ V	1	1.1	–	W
	in 16 Ω (TDA7052AT)	$V_P = 6$ V	0.5	0.55	–	W
G_v	maximum total voltage gain		35	36	37	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	$V_P = 6$ V; $R_L = \infty$	–	6	12	mA
THD	total harmonic distortion	$P_O = 0.5$ W	–	0.2	1	%

1-Watt low voltage audio power amp with DC volume control

TDA7052A/AT

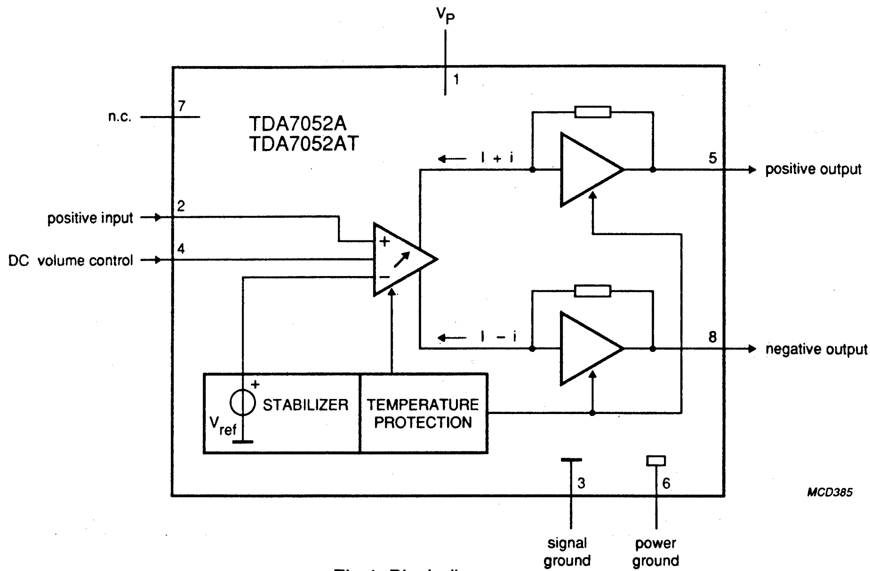


Fig.1 Block diagram.

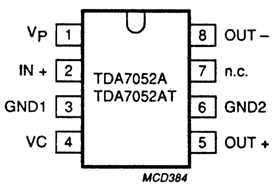


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
IN+	2	positive input
GND1	3	signal ground
VC	4	DC volume control
OUT+	5	positive output
GND2	6	power ground
n.c	7	not connected
OUT–	8	negative output

FUNCTIONAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control, designed for use in TV and monitors but also suitable for battery fed portable recorders and radios.
In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.
In the TDA7052A/AT the DC volume control stage is integrated into the input stage so that no coupling capacitors are required and yet a low offset voltage is maintained. At the same time the minimum supply remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Thus a reduced power supply with smaller capacitors can be used which results in cost savings.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 36 dB. The DC volume control stage has a logarithmic control characteristic.

The total gain can be controlled from 36 dB to –44 dB. If the DC volume control voltage is below 0.3 V, the device switches to the mute mode. The amplifier is short-circuit proof to ground and V_P. Also a thermal protection circuit is implemented. If the crystal temperature rises above 150 °C the gain will be reduced, so the output power is reduced. Special attention is given to switch on and off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\%$			
	TDA7052A		–	1.25	W
	TDA7052AT		–	0.64	W
T_{amb}	operating ambient temperature range		–40	85	°C
T_{stg}	storage temperature range		–55	150	°C
T_{vj}	virtual junction temperature		–	150	°C
T_{sc}	short-circuit time		–	1	hr
V_2	input voltage pin 2		–	8	V
V_4	input voltage pin 4		–	8	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air			
	TDA7052A	–	100	K/W
	TDA7052AT	–	155	K/W

Note

TDA7052A: V_P = 6 V; R_L = 8 Ω.
The maximum sine-wave dissipation is 0.9 W.
Therefore $T_{amb(max)}$ = 150 - 100 x 0.9 = 60 °C.
TDA7052AT: V_P = 6 V; R_L = 16 Ω.
The maximum sine-wave dissipation is 0.46 W.
Therefore $T_{amb(max)}$ = 150 - 155 x 0.46 = 78 °C.

CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; f = 1 kHz; unless otherwise specified (see Fig.6).
TDA7052A: R_L = 8 Ω;
TDA7052AT: R_L = 16 Ω;

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		4.5	–	18	V
I_P	total quiescent current	V_P = 6 V; $R_L = \infty$ note 1	–	6	12	mA
Maximum gain; V_4 = 1.4 V						
P_O	output power TDA7052A TDA7052AT	THD = 10%	 1 0.5	 1.1 0.55	 – –	 W W
THD	total harmonic distortion TDA7052A TDA7052AT	 P_O = 0.5 W P_O = 0.25 W	 – –	 0.2 0.2	 1 1	 % %
G_v	voltage gain		35	36	37	dB
V_I	input signal handling	V_4 = 1 V; THD < 1%	0.6	–	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	f = 500 kHz; note 2	–	tbf	–	µV
B	bandwidth		–	20 Hz to 20 kHz	–	
RR	ripple rejection	note 3	40	–	–	dB
$\|V_{off}\|$	DC output offset voltage		–	tbf	150	mV
Z_I	input impedance (pin 2)		15	20	25	kΩ
Minimum gain; V_4 = 0.5 V						
G_v	voltage gain		–	–44	–	dB
$V_{no(rms)}$	noise output voltage RMS value)	note 4	–	20	30	µV
Mute position						
V_O	output voltage in mute position	$V_4 \leq 0.3$ V; V_I = 600 mV	–	–	30	µV
DC volume control						
ϕ	gain control range		75	80	–	dB
I_4	control current	V_4 = 0.4 V	tbf	65	tbf	µA

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage dividend by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV, (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS-value) is measured with R_S = 5 kΩ unweighted.

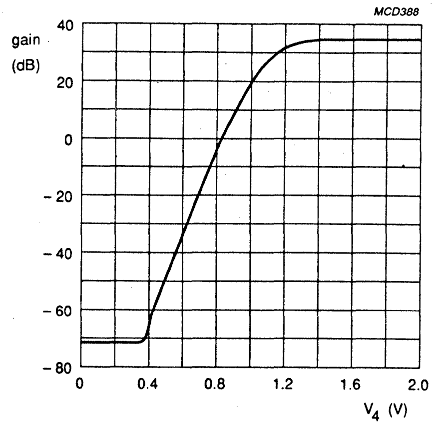


Fig.3 Gain control as a function of DC volume control.

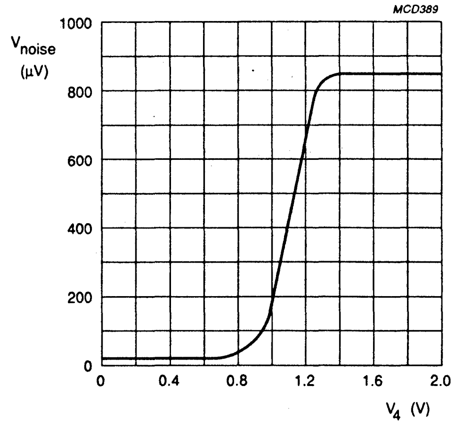


Fig.4 Noise output voltage as a function of DC volume control.

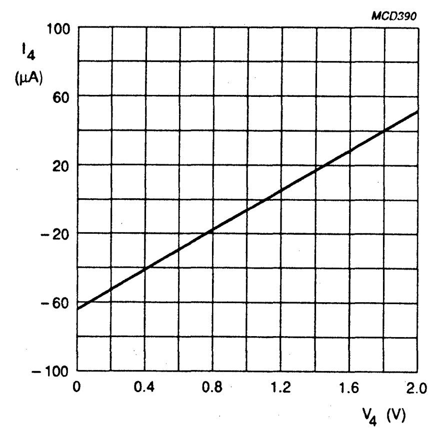
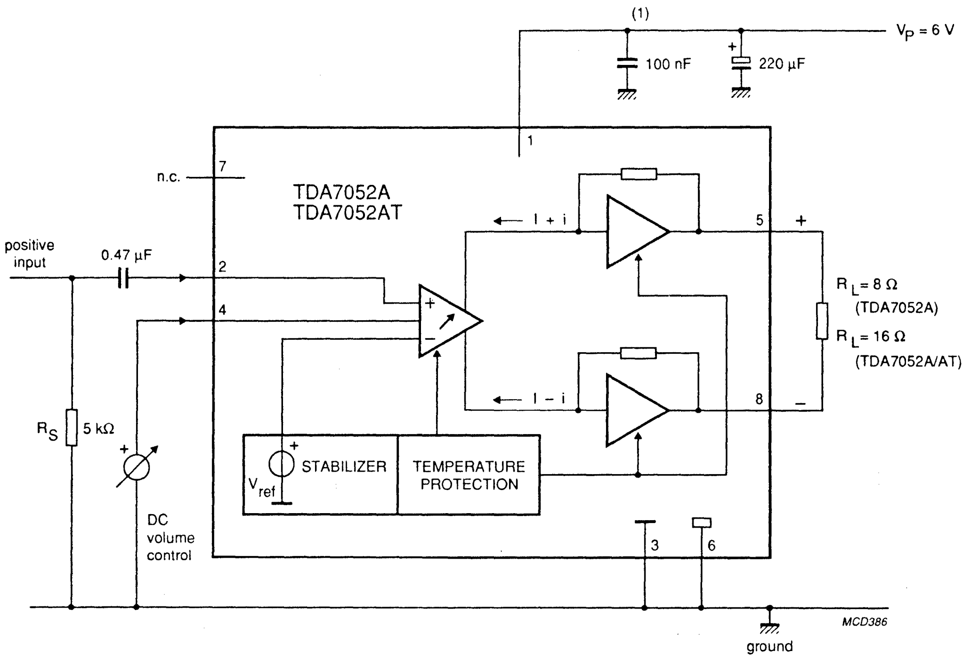


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 1.

Fig.6 Test and application diagram.

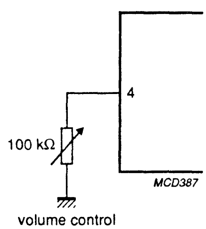


Fig.7 Application with potentiometer as volume control; maximum gain = 30 dB.

3-Watt mono BTL audio output amplifier

TDA7056A

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7056A is a mono BTL output amplifier with DC volume control. It is designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056A	9	SIL	plastic	SOT110BE

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		4.5	–	18	V
P_O	output power in 16 Ω	V_P = 12 V	3	3.4	–	W
G_v	voltage gain		35	36	37	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	V_P = 12 V; $R_L = \infty$	–	8	16	mA
THD	total harmonic distortion	V_P = 0.5 W	–	0.2	1	%

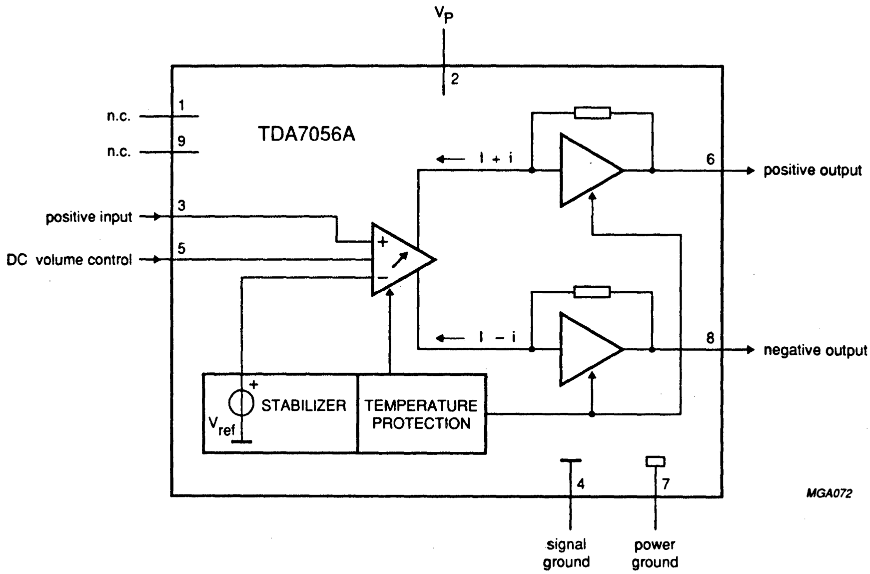


Fig.1 Block diagram.

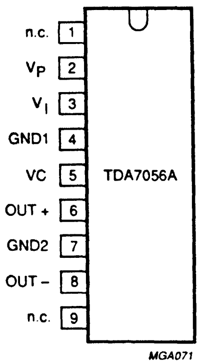


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_P	2	positive supply voltage
V_I	3	voltage input
GND1	4	signal ground
VC	5	DC volume control
OUT+	6	positive output
GND2	7	power ground
OUT−	8	negative output
n.c.	9	not connected

FUNCTIONAL DESCRIPTION

The TDA7056A is a mono BTL output amplifier with DC volume control, designed for use in TV and monitor but also suitable for battery-fed portable recorders and radios.
In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitor to keep the offset voltage low.
In the TDA7056A the DC volume stage is integrated into the input stage so that coupling capacitors are not required and a low offset voltage is maintained.
At the same time the minimum supply voltage remains low.
The BTL principle offers the following advantages:

- lower peak value of the supply current
- the frequency of the ripple on the supply voltage is twice the signal frequency

Thus, a reduced power supply and smaller capacitors can be used which results in cost savings.
For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 36 dB. The DC volume control stage has a logarithmic control characteristic.
The total gain can be controlled from 36 dB to –44 dB.
If the DC volume control voltage is below 0.3 V, the device switches to the mute mode.
The amplifier is short-circuit proof to ground and V_P. Also a thermal protection circuit is implemented. If the crystal temperature rises above 150 °C the gain will be reduced, so the output power is reduced.
Special attention is given to switch-on and off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1	A
I_{OSM}	non repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	T_{case} < 60 °C	–	9	W
T_{amb}	operating ambient temperature range		–40	85	°C
T_{stg}	storage temperature range		–55	150	°C
T_{vj}	virtual junction temperature		–	150	°C
T_{sc}	short-circuit time		–	1	hr
V_3	input voltage pin 3		–	8	V
V_5	input voltage pin 5		–	8	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}c}$	from junction to case	–	10	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air	–	55	k/W

Note

V_P = 12 V; R_L = 16 Ω; The maximum sine-wave dissipation is = 1.8 W. The $R_{th\ vj\text{-}a}$ of the package is 55 K/W;
$T_{amb\ (max)}$ = 150 – 55 x 1.8 = 51 °C

CHARACTERISTICS

V_P = 12 V; f = 1 kHz; R_L = 16 Ω; T_{amb} = 25 °C; unless otherwise specified (see Fig.6)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		4.5	–	18	V
I_P	total quiescent current	V_P = 6 V; R_L = ∞; note 1	–	8	16	mA
Maximum gain (V_5 = 1.4 V)						
P_O	output power	THD = 10%	3	3.4	–	W
THD	total harmonic distortion	P_O = 0.5 W	–	0.2	1	%
G_v	voltage gain		35	36	37	dB
V_I	input signal handling	V_5 = 1 V;THD < 1%	0.6	–	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	f = 500 kHz; note 2	–	tbf	–	μV
B	bandwidth		–	20 Hz to 20 kHz	–	
RR	ripple rejection	note 3	40	–	–	dB
$\|V_{off}\|$	DC output offset voltage		–	tbf	150	mV
Z_I	input impedance pin 3		15	20	25	kΩ
Minimum gain (V_5 = 0.5 V)						
G_v	voltage gain		–	–44	–	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 4	–	20	30	μV
Mute position						
V_O	output voltage in mute position	$V_5 \le$ 0.3 V; V_I = 600 mV	–	–	30	μV
DC volume control						
ϕ	gain control range		75	80	–	dB
I_5	control current	V_5 = 0 V	tbf	65	tbf	μA

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_s = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

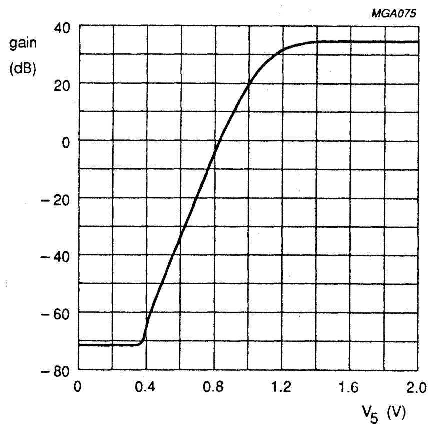


Fig.3 Gain as a function of DC volume control.

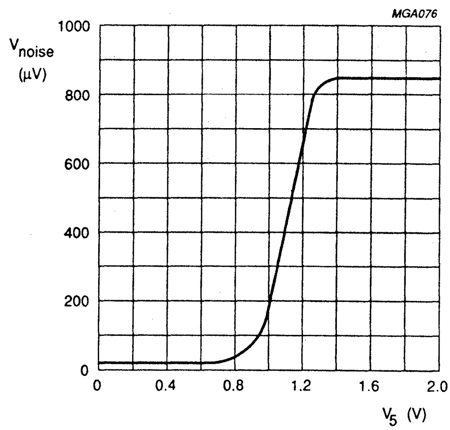


Fig.4 Noise output voltage as a function of DC volume control.

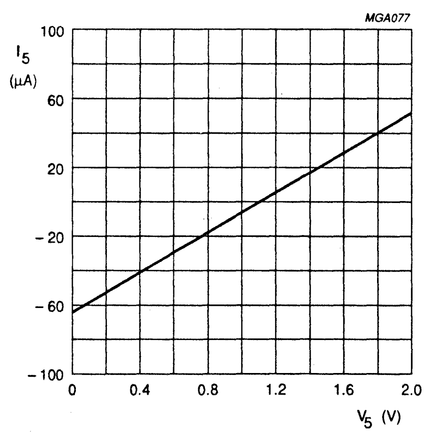
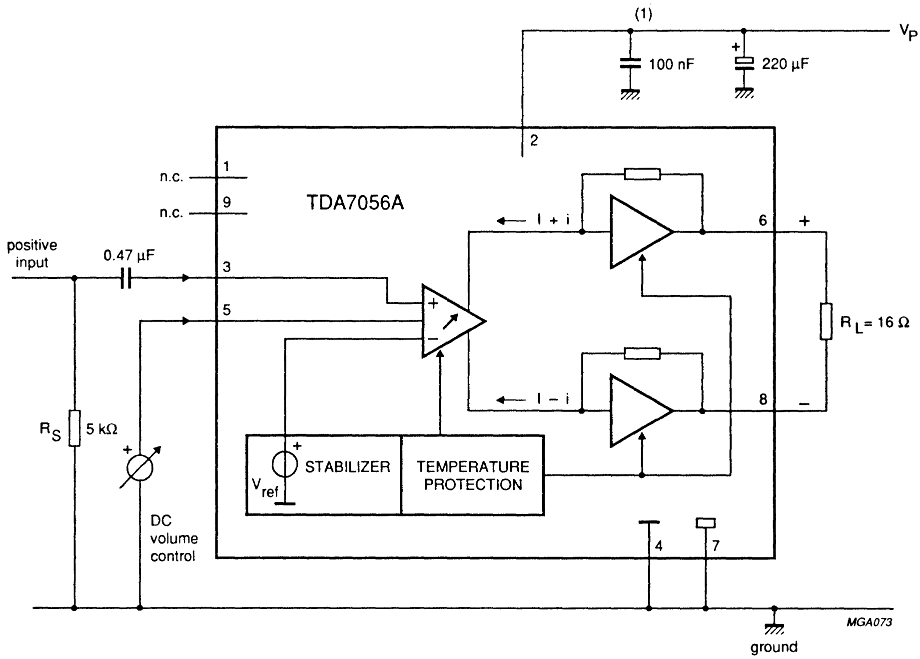


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 μF electrolytic capacitor is connected close to pin 2.

Fig.6 Test and application diagram.

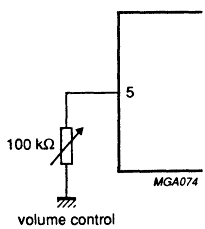
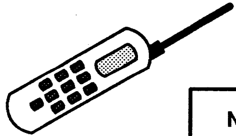


Fig.7 Application using a potentiometer for volume control; G_v = 30 dB.

Section 2
Compandors

INDEX



COMPANDOR FAMILY OVERVIEW

	NE570	NE571	NE572	NE575	NE576	NE577	NE578
V_{CC}	6–24V	6–18V	6–22V	**3–7V**	**2–7V**	**2–7V**	**2–7V**
I_{CC}	3.2mA	3.2mA	6mA	3–5.5mA*	**1–3mA***	**1–2mA***	**1–2mA***
Number of Pins	16	16	16	20	14	14	16
Packages NE: 0 to + 70 C SA: –40 to +85 C N: Plastic DIP D: Plastic SO F: CerDIP DJ: SSOP (Shrink Small Outline Package)	NE570F NE570N NE570D	NE571F NE571N NE571D SA571F SA571N SA571D	NE572N NE572D SA572F SA572N SA572D	NE575N NE575D NE575DK SA575N SA575D SA575DK	NE576N NE576D SA576N SA576D	NE577N NE577D SA577N SA577D	NE578N NE578D SA578N SA578D
ALC	Both Channels	Both Channels	Both Channels	Right Channel	Right Channel	Right Channel	Right Channel
Reference Voltage	Fixed 1.8V	Fixed 1.8V	Fixed 2.5V	Vcc/2	Vcc/2	Vcc/2	Vcc/2
Unity Gain	775mVrms	775mVrms	100mVrms	100mVrms	100mVrms	**10mV to 1V(rms)**	**10mV to 1V(rms)**
Power Down	NO	NO	NO	NO	NO	NO	YES (170µA)
Key Features	– Excellent Unity Gain Tracking Error **– Excellent THD**	– Excellent Unity Gain Tracking Error **– Excellent THD**	**– Independent Attack & Release Time** – Good THD – Needs an Ext. Summing Op Amp	**– 2 Uncommitted On-Chip Op Amps Available** – Low Voltage	**– Low Power** **– Low External Component Count**	**– Low Power** **– Programmable Unity Gain**	**– Low Power** **– Programmable Unity Gain** **– Power Down** **– Mute Function** **– Summing Capability (DTMF)** **– 600Ω Drive Capability**
Applications Cordless Phones Cellular Phones Wireless Mics Modems Consumer Audio Two-way Communications	High Performance Audio Circuits "Hi-Fi Commercial Quality"	High Performance Audio Circuits "Hi-Fi Commercial Quality"	High Performance Audio Circuits **"Hi-Fi Studio Quality"**	Consumer Audio Circuits "Commercial Quality"	**Battery Powered Systems** "Commercial Quality"	**Battery Powered Systems** "Commercial Quality"	**Battery Powered Systems** "Commercial Quality"

NOTE: NE5750/5751 are also Excellent Audio Processor Components for High Performance Cordless and Cellular Applications that Include the Companding Function
*Icc varies with Vcc

Compandor

NE570/571/SA571

DESCRIPTION

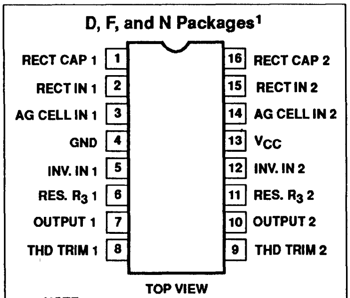
The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

FEATURES

- Complete compressor and expandor in one IChip
- Temperature compensated
- Greater than 110dB dynamic range
- Operates down to 6VDC
- System levels adjustable with external components
- Distortion may be trimmed out
- Dynamic noise reduction systems
- Voltage-controlled amplifier

PIN CONFIGURATION



NOTE:
1. SOL - Released in Large SO Package Only.

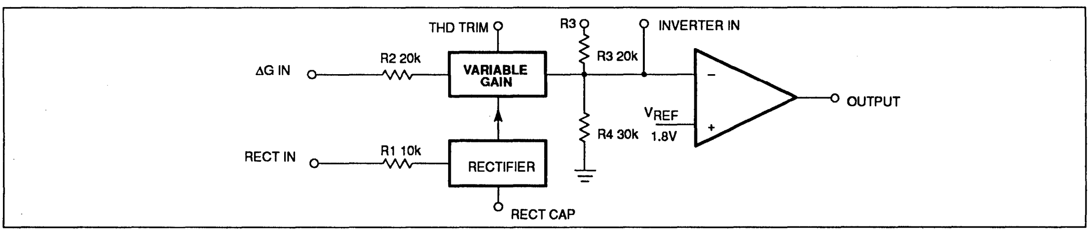
APPLICATIONS

- Cellular radio
- Telephone trunk compandor—570
- Telephone subscriber compandor—571
- High level limiter
- Low level expandor—noise gate
- Dynamic filters
- CD Player

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE570D
16-Pin Cerdip	0 to +70°C	NE570F
16-Pin Plastic DIP	0 to +70°C	NE570N
16-Pin Plastic SOL	0 to +70°C	NE571D
16-Pin Cerdip	0 to +70°C	NE571F
16-Pin Plastic DIP	0 to +70°C	NE571N
16-Pin Plastic SOL	-40 to +85°C	SA571D
16-Pin Cerdip	-40 to +85°C	SA571F
16-Pin Plastic DIP	-40 to +85°C	SA571N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage 570 571	 24 18	VDC
T_A	Operating ambient temperature range NE SA	 0 to 70 -40 to +85	°C
P_D	Power dissipation	400	mW

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE570			LIMITS NE/SA571[5]			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		6		24	6		18	V
I_{CC}	Supply current	No signal		3.2	4.8		3.2	4.8	mA
I_{OUT}	Output current capability		±20			±20			mA
SR	Output slew rate			±.5			±.5		V/µs
	Gain cell distortion[2]	Untrimmed Trimmed		0.3 0.05	1.0		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15		±5	±15	%
	Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±20	±100		±30	±150	mV
	Expandor output noise	No signal, 15Hz-20kHz[1]		20	45		20	60	µV
	Unity gain level[6]	1kHz	-1	0	+1	-1.5	0	+1.5	dBm
	Gain change[2, 4]			±0.1	±0.2		±0.1		dB
	Reference drift[4]			±5	±10		+2, -25	+20, -50	mV
	Resistor drift[4]			+1, -0			+8, -0		%
	Tracking error (measured relative to value at unity gain) equals [V_O - V_O (unity gain)] dB - V_2dBm	Rectifier input, V_2 = +6dBm, V_1 = 0dB V_2 = -30dBm, V_1 = 0dB		+0.2 +0.2	 -0.5, +1		+0.2 +0.2	 -1, +1.5	dB
	Channel separation			60			60		dB

NOTES:
1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at T_A = 25°C.
5. Electrical characteristics for the SA571 only are specified over -40 to +85°C temperature range.
6. 0dBm = 775mV_{RMS}.

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|\ avg}{R_1}$$

or

$$G \propto \frac{|V_{IN}|\ avg}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})_e - t/\tau + G_{final}\ ;\ \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

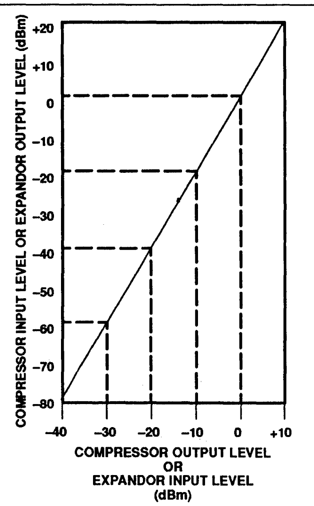
A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expander gain to be determined only by internal components.

The output stage is capable of ±20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

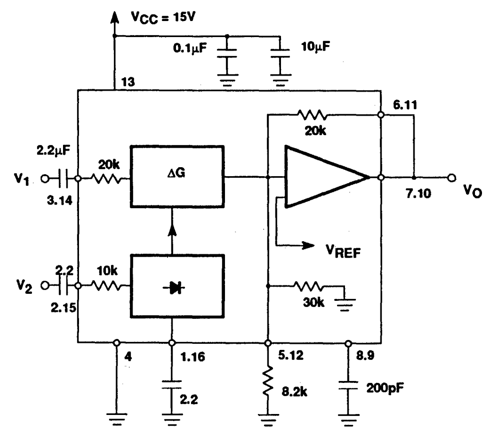
A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expander circuits.



Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT



INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components. This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expander are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

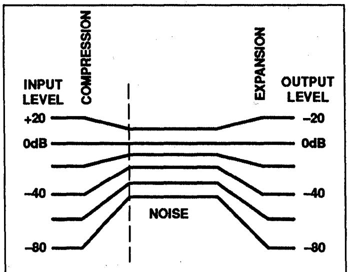


Figure 1. Restricted Dynamic Range Channel

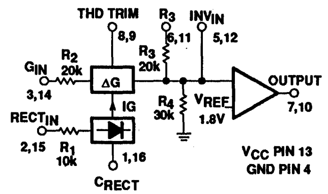


Figure 2. Chip Block Diagram (1 of 2 Channels)

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 4 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\,DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

$$V_{REF} = \left(1 + \frac{R_{DCTOT}}{30k}\right) 1.8V$$

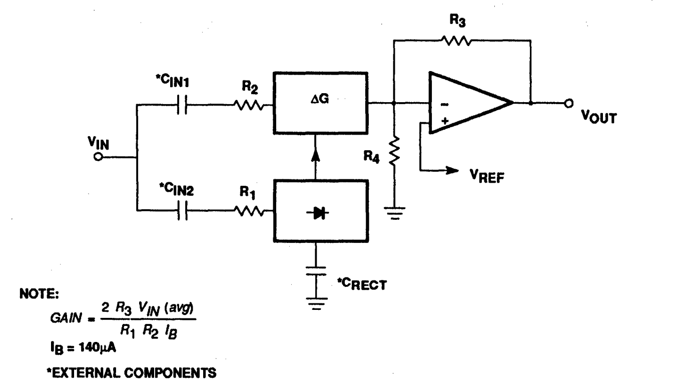


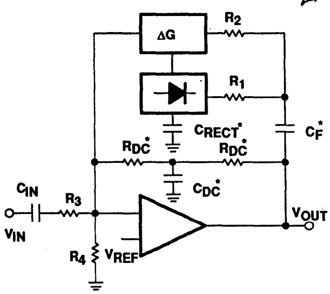
Figure 3. Basic Expander

The output of the expander will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4}\ V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.



NOTES:

$$GAIN = \left(\frac{R_1\ R_2\ I_B}{2R_3\ V_{INavg}}\right)^{\frac{1}{2}}$$

$I_B = 140\mu A$

* External components

Figure 4. Basic Compressor

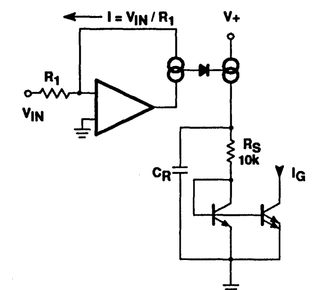
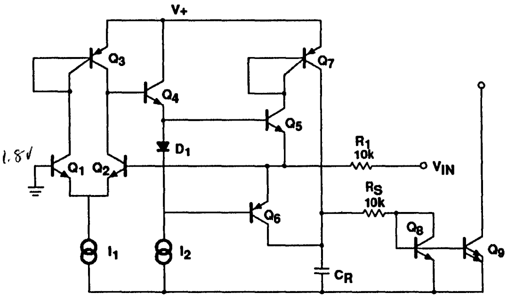


Figure 5. Rectifier Concept

CIRCUIT DETAILS—RECTIFIER

Figure 5 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.



NOTE:

$$I_G = 2\frac{V_{IN\ avg}}{R\ 1}$$

Figure 6. Simplified Rectifier Schematic

Figure 6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the *a* of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The *a*'s of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

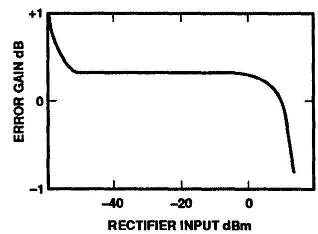


Figure 7. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

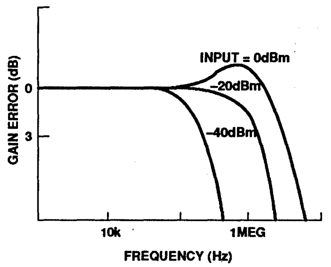


Figure 8. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linearized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} ($=V_{IN}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1}=I_1+I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

$I_2-(I_1+I_{IN})=I_1-I_{IN}=I_{C2}$.

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

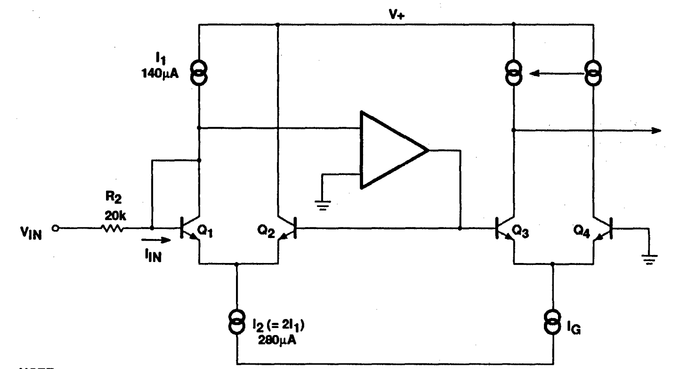
The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G=I_{C3}+I_{C4}$ and $I_{OUT}=I_{C4}-I_{C3}$ will yield the multiplier transfer function,

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN}}{R_2}\frac{I_G}{I_1}$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.



NOTE:

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{I_G V_{IN}}{I_2 R_2}$$

Figure 9. Simplified ΔG Cell Schematic

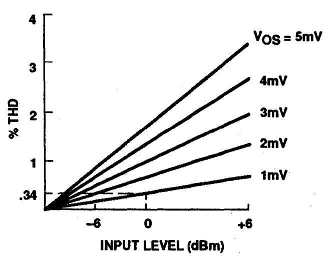


Figure 10. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

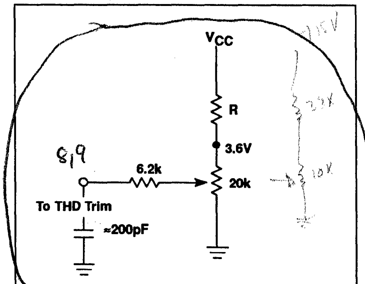


Figure 11. THD Trim Network

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 13 shows such a trim network.

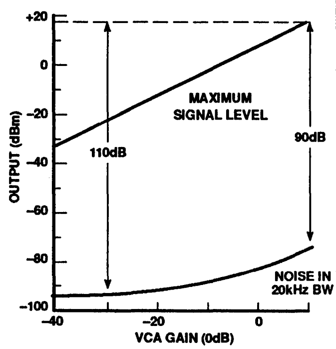


Figure 12. Dynamic Range of NE570

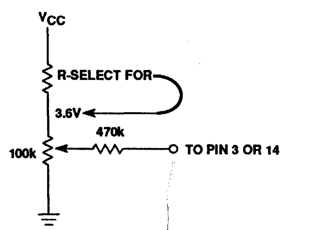


Figure 13. Control Signal Feedthrough Trim

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

RESISTORS

Inspection of the gain equations in Figures 3 and 4 will show that the basic compressor and expander circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

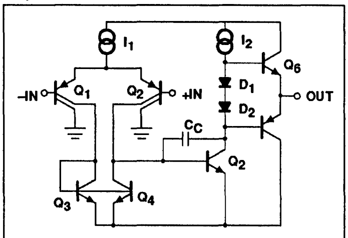


Figure 14. Operational Amplifier

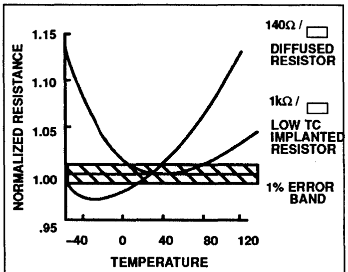
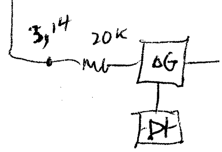


Figure 15. Resistance vs Temperature

Does this set the thresholding of the Log Amp?



APPLICATIONS

The following circuits will illustrate some of the wide variety of applications for the NE570.

BASIC EXPANDOR

Figure 1 shows how the circuit would be hooked up for use as an expandor. Both the rectifier and ΔG cell inputs are tied to V_{IN} so that the gain is proportional to the average value of (V_{IN}). Thus, when V_{IN} falls 6dB, the gain drops 6dB and the output drops 12dB. The exact expression for the gain is

$$Gain\ exp. = \left[\frac{2\ R_3\ V_{IN}\ (avg)}{R_1\ R_2\ I_B}\right]^2$$

$I_B = 140\mu A$

The maximum input that can be handled by the circuit in Figure 1 is a peak of 3V. The rectifier input current can be as large as $I=3V/R_1=3V/10k=300\mu A$. The ΔG cell input current should be limited to $I=2.8V/R_2=2.8V/20k=140\mu A$. If it is necessary to handle larger input voltages than 0 ±2.8V peak, external resistors should be placed in series with R_1 and R_2 to limit the input current to the above values.

Figure 1 shows a pair of input capacitors C_{IN1} and C_{IN2}. It is now necessary to use both capacitors if low level tracking accuracy is not important. If R_1 and R_2 are tied together and share a common capacitor, a small current will flow between the ΔG cell summing node and the rectifier summing node due to offset voltages. This current will produce an error in the gain control signal at low levels, degrading tracking accuracy.

The output of the expandor is biased up to 3V by the DC gain provided by R_3, R_4. The output will bias up to

$$V_{OUTDC} = 1 + \frac{R_3}{R_4}\ V_{REF}$$

For supply voltages higher than 6V, R_4 can be shunted with an external resistor to bias the output up to V_{CC}.

Note that it is possible to externally increase R_1, R_2, and R_3, and to decrease R_3 and R_4. This allows a great deal of flexibility in setting up system levels. If larger input signals are to be handled, R_1 and R_2 may be increased; if a larger output is required, R_3 may be increased. To obtain the largest dynamic range out of this circuit, the rectifier input should always be as large as possible (subject to the ±300μA peak current restriction).

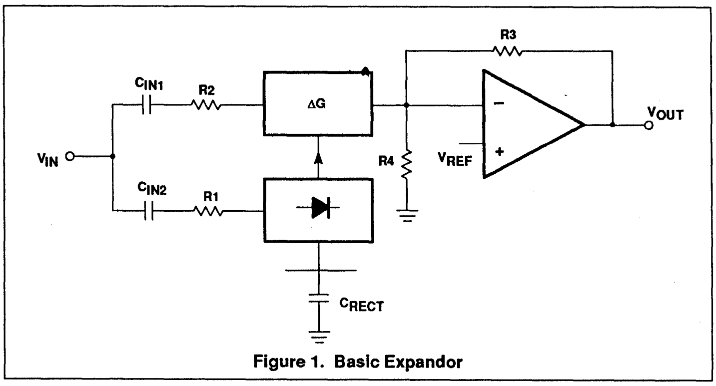


Figure 1. Basic Expandor

BASIC COMPRESSOR

Figure 2 shows how to use the NE570/571 as a compressor. It functions as an expandor in the feedback loop of an op amp. If the input rises 6dB, the output can rise only 3dB. The 3dB increase in output level produces a 3dB increase in gain in the ΔG cell, yielding a 6dB increase in feedback current to the summing node. Exact expression for gain is

$$Gain\ comp. = \left[\frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (avg)}\right]^{\frac{1}{2}}$$

The same restrictions for the rectifier and ΔG cell maximum input current still hold, which place a limit on the maximum compressor output. As in the expandor, the rectifier and ΔG cell inputs could be made common to save a capacitor, but low level tracking accuracy would suffer. Since there is no DC feedback path around the op amp through the ΔG cell, one must be provided externally. The pair of resistors R_{DC} and the capacitor C_{DC} must be provided. The op amp output will bias up to

$$V_{OUTDC} = \left(1 + \frac{R_{DC}}{R_4}\right) V_{REF}$$

For the largest dynamic range, the compressor output should be as large as possible so that the rectifier input is as large as possible (subject to the ±300μA peak current restriction). If the input signal is small, a large output can be produced by reducing R_3 with the attendant decrease in input impedance, or by increasing R_1 or R_2. It would be best to increase R_2 rather than R_1 so that the rectifier input current is not reduced.

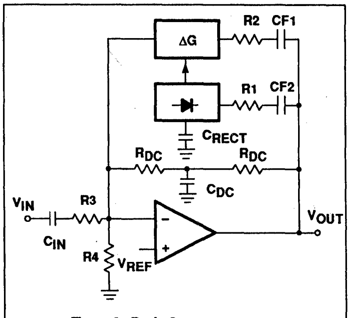


Figure 2. Basic Compressor

DISTORTION TRIM

Distortion can be produced by voltage offsets in the ΔG cell. The distortion is mainly even harmonics, and drops with decreasing input signal (input signal meaning the current into the ΔG cell). The THD trim terminal provides a means for trimming out the offset voltages and thus trimming out the distortion. The circuit shown in Figure 3 is suitable, as would be any other capable of delivering ±30μA into 100Ω resistor tied to 1.8V.

LOW LEVEL MISTRACKING

The compandor will follow a 2-to-1 tracking ratio down to very low levels. The rectifier is responsible for errors in gain, and it is the rectifier input bias current of <100nA that

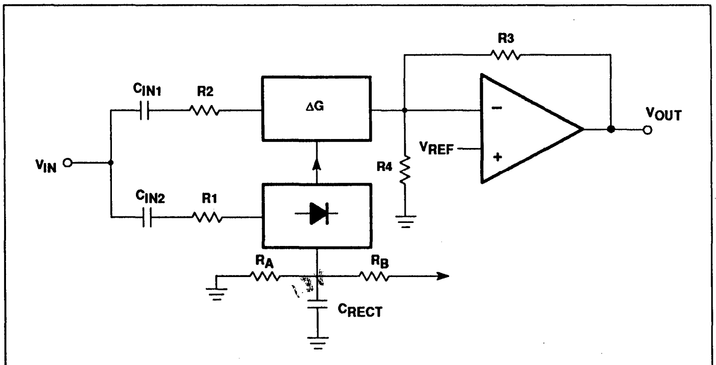


Figure 4. Expandor With Low Level Mistracking

produces errors at low levels. The magnitude signal level drops to a 1μA average, the bias current will produce a 10% or 1dB error in gain. This will occur at 42dB below the maximum input level.

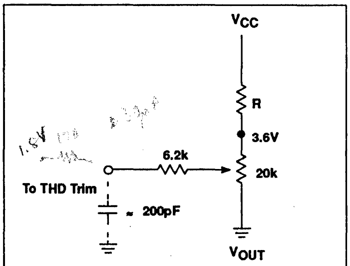


Figure 3. THD Trim Network

It is possible to deviate from the 2-to-1 transfer characteristic at low levels as shown in the circuit of Figure 4. Either R_A or R_B, (but not both), is required. The voltage on C_{RECT} is $2{\times}V_{BE}$ plus V_{IN} avg. For low level inputs V_{IN} avg is negligible, so we can assume 1.3V as the bias on C_{RECT}. If R_A is placed from C_{RECT} to AND we will bleed off a current $I=1.3V/R_A$. If the rectifier average input current is less than this value, there will be no gain control input to the ΔG cell so that its gain will be zero and the expandor output will be zero. As the input level is raised, the input current will exceed $1.3V/R_A$ and the expandor output will become active. For large input signals, R_A will have little effect. The result of this is that we will deviate from the 2-to-1 expansion, present at high levels, to an infinite expansion at low levels where the output shuts off completely. Figure 5 shows some examples of tracking curves which can be obtained. Complementary curves would be obtained for a compressor, where at low level signals the result would be infinite compression. The bleed current through R_A will be a function of temperature because of the two V_{BE} drops, so the low level tracking will drift with temperature. If a negative supply is available, if would be desirable to tie R_A to that, rather than ground, and to increase its value accordingly. The bleed current will then be less sensitive to the V_{BE} temperature drift.

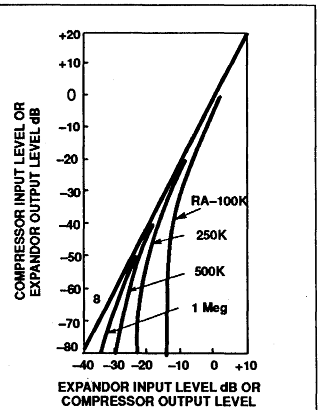


Figure 5. Mistracking With R_A

R_B will supply an extra current to the rectifier equal to $(V_{CC}-1.3V)R_B$. In this case, the expandor transfer characteristic will deviate towards 1-to-1 at low levels. At low levels the expandor gain will stop dropping and the expansion will cease. In a compressor, this would lead to a lack of compression at low levels. Figure 6 shows some typical transfer curves. An R_B value of approximately 2.5M would trim the low level tracking so as to match the Bell system N2 trunk compandor characteristic.

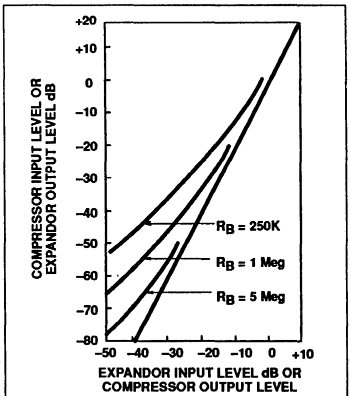


Figure 6. Mistracking With R_B

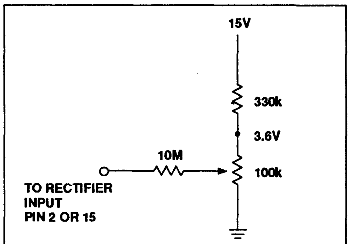


Figure 7. Rectifier Bias Current Compensation

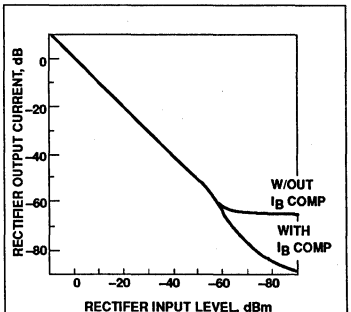


Figure 8. Rectifier Performance With Bias Current Compensation

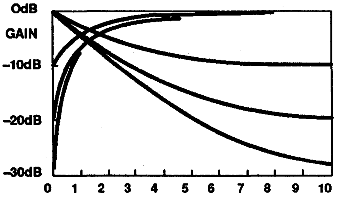


Figure 9. Gain vs Time Input Steps of ±10, ±20, ±30dB

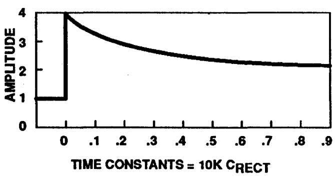


Figure 10. Compressor Attack Envelope +12dB Step

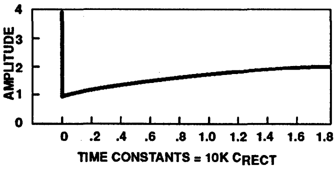


Figure 11. Compressor Release Envelope –12dB Step

RECTIFIER BIAS CURRENT CANCELLATION

The rectifier has an input bias current of between 50 and 100nA. This limits the dynamic range of the rectifier to about 60dB. It also limits the amount of attenuation of the ΔG cell. The rectifier dynamic range may be increased by about 20dB by the bias current trim network shown in Figure 7. Figure 8 shows the rectifier performance with and without bias current cancellation.

ATTACK AND DECAY TIME

The attack and decay times of the compandor are determined by the rectifier filter time constant $10k \times C_{RECT}$. Figure 9 shows how the gain will change when the input signal undergoes a 10, 20, or 30dB change in level.

The attack time is much faster than the decay, which is desirable in most applications. Figure 10 shows the compressor attack envelope for a +12dB step in input level. The initial output level of 1 unit instantaneously rises to 4 units, and then starts to fall towards its final value of 2 units. The CCITT recommendation on attack and decay times for telephone system compandors defines the attack time as when the envelope has fallen to a level of 3 units, corresponding to t=0.15 in the figure. The CCITT recommends an attack time of 3 ±2ms, which suggests an RC product of 20ms. Figure 11 shows the compressor output envelope when the input level is suddenly reduced 12dB. The output, initially at a level of 4 units, drops 12dB to 1 unit and then rises to its final value of 2 units. The CCITT defines release time as when the output has risen to 1.5 units, and suggests a value of 13.5 ±9ms. This corresponds to t=0.675 in the figure, which again suggests a 20ms RC product. Since R_1=10k, the CCITT recommendations will be met if C_{RECT}=2μF.

There is a trade-off between fast response and low distortion. If a small C_{RECT} is used to get very fast attack and decay, some ripple will appear on the gain control line and produce distortion. As a rule, a 1μF C_{RECT} will produce 0.2% distortion at 1kHz. The distortion is inversely proportional to both frequency and capacitance. Thus, for telephone applications where C_{RECT}=2μF, the ripple would cause 0.1% distortion at 1kHz and 0.33% at 800Hz. The low frequency distortion generated by a compressor would be cancelled (or undistorted) by an expandor, providing that they have the same value of C_{RECT}.

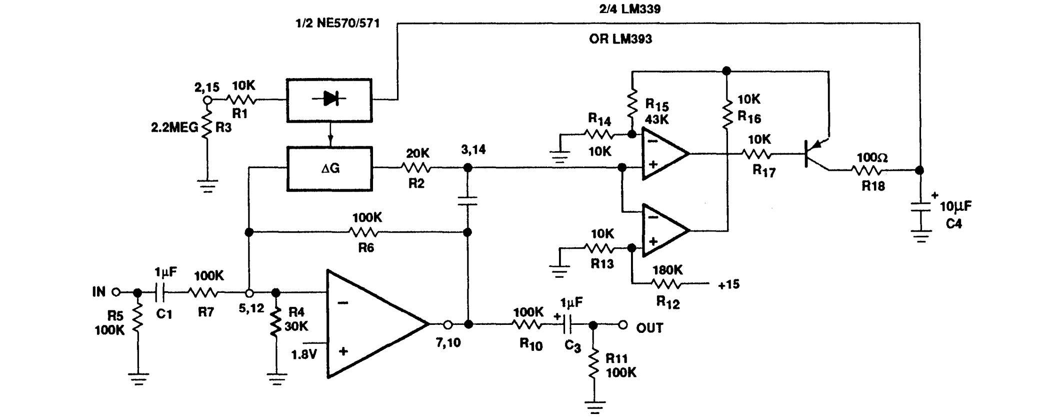
FAST ATTACK, SLOW RELEASE HARD LIMITER

The NE570/571 can be easily used to make an excellent limiter. Figure 12 shows a typical circuit which requires of an NE570/571, of an LM339 quad comparator, and a PNP transistor. For small signals, the ΔG cell is nearly off, and the circuit runs at unity gain as set by R_8, R_7. When the output signal tries to exceed a + or –1V peak, a comparator threshold is exceeded. The PNP is turned on and rapidly charges C_4 which activates the ΔG cell. Negative feedback through the ΔG cell reduces the gain and the output signal level. The attack time is set by the RC product of R_{18} and C_4, and the release time is determined by C_4 and the internal rectifier resistor, which is 10k. The circuit shown attacks in less than 1ms and has a release time constant of 100ms. R_9 trickles about 0.7μA through the rectifier to prevent C_4 from becoming completely discharged. The gain cell is activated when the voltage on Pin 1 or 16 exceeds two diode drops. If C_4 were allowed to become completely discharged, there would be a slight delay before it recharged to >1.2V and activated limiting action.

A stereo limiter can be built out of 1 NE570/571, 1 LM339 and two PNP transistors. The resistor networks R_{12}, R_{13} and R_{14}, R_{15}, which set the limiting thresholds, could be common between channels. To gang the stereo channels together (limiting in one channel will produce a corresponding gain change in the second channel to maintain the balance of the stereo image), then Pins 1 and 16 should be jumpered together. The outputs of all 4 comparators may then be tied together, and only one PNP transistor and one capacitor C_4 need be used. The release time will then be the product $5k \times C_4$ since two channels are being supplied current from C_4.

USE OF EXTERNAL OP AMP

The operational amplifiers in the NE570/571 are not adequate for some applications.



+15V Pin 13
GND Pin 4
R_1, R_2, R_4 are internal to the NE570/571

Figure 12. Fast Attack, Slow Release Hard Limiter

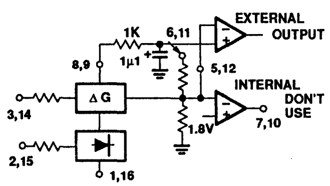


Figure 13. Use of External Op Amp

The slew rate, bandwidth, noise, and output drive capability can limit performance in many systems. For best performance, an external op amp can be used. The external op amp may be powered by bipolar supplies for a larger output swing.

Figure 13 shows how an external op amp may be connected. The non-inverting input must be biased at about 1.8V. This is easily accomplished by tying it to either Pin 8 or 9, the THD trim pins, since these pins sit at 1.8V. An optional RC decoupling network is shown which will filter out the noise from the NE570/571 reference (typically about 10µV in 20kHz BW). The inverting input of the external op amp is tied to the inverting input of the internal op amp. The output of the external op amp is then used, with the internal op amp output left to float. If the external op amp is used single supply (+V_{CC} and ground), it must have an input common-mode range down to less than 1.8V.

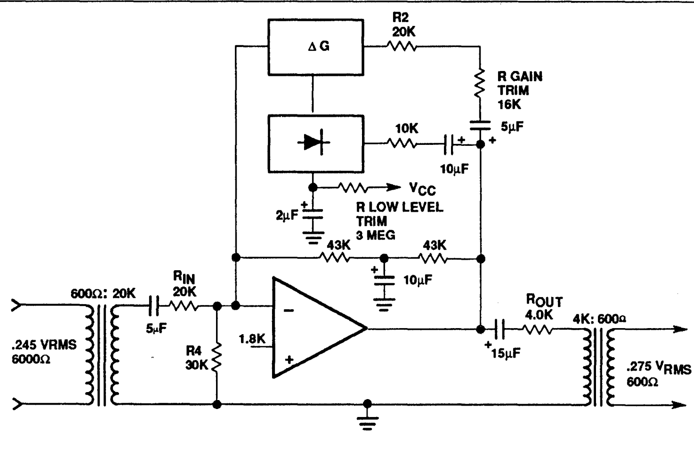


Figure 14. N2 Compressor

N2 COMPANDOR

There are four primary considerations involved in the application of the NE570/571 in an N2 compandor. These are matching of input and output levels, accurate 600Ω input and output impedances, conformance to the Bell system low level tracking curve, and proper attack and release times.

Figure 14 shows the implementation of an N2 compressor. The input level of 0.245V_{RMS} is stepped up to 1.41V_{RMS} by the 600Ω: 20kΩ matching transformer. The 20k input resistor properly terminates the transformer. An internal 20kΩ resistor (R_3) is provided, but for accurate impedance termination an external resistor should be used. The output impedance is provided by the 4kΩ output resistor and the 4kΩ: 600Ω output transformer.

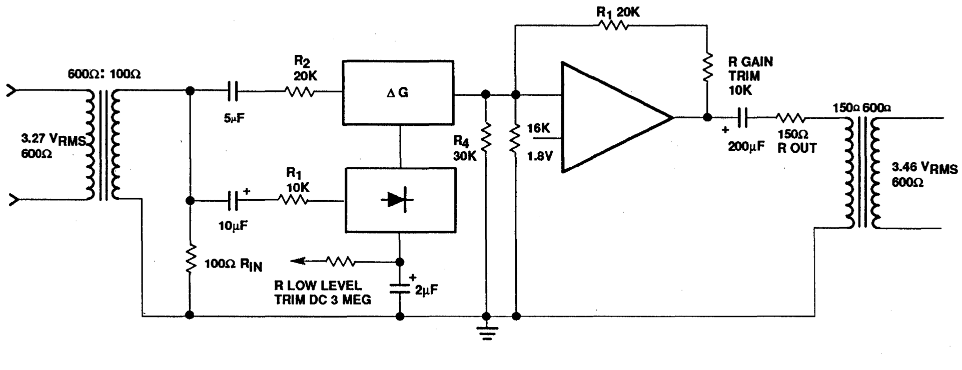


Figure 15. N2 Expandor

The $0.275V_{RMS}$ output level requires a 1.4V op amp output level. This can be provided by increasing the value of R_2 with an external resistor, which can be selected to fine trim the gain. A rearrangement of the compressor gain equation (6) allows us to determine the value for R_2.

$$R_2 = \frac{Gain^2 \ x \ 2 \ R_3 \ V_{IN} \ avg}{R_1 \ I_B}$$
$$= \frac{1^2 \ x \ 2 \ x \ 20k \ x \ 1.27}{10k \ x \ 140\mu A}$$
$$= 36.3k$$

The external resistance required will thus be 36.3k–20k=16.3k.

The Bell-compatible low level tracking characteristic is provided by the low level trim resistor from C_{RECT} to V_{CC}. As shown in Figure 6, this will skew the system to a 1:1 transfer characteristic at low levels. The 2μF rectifier capacitor provides attack and release times of 3ms and 13.5ms, respectively, as shown in Figures 10 and 11. The R-C-R network around the op amp provides DC feedback to bias the output at DC.

An N2 expandor is shown in Figure 15. The input level of $3.27V_{RMS}$ is stepped down to 1.33V by the 600Ω:100Ω transformer, which is terminated with a 100Ω resistor for accurate impedance matching. The output impedance is accurately set by the 150Ω output resistor and the 150Ω:600Ω output transformer. With this configuration, the 3.46V transformer output requires a 3.46V op amp output. To obtain this output level, it is necessary to increase the value of R_3 with an external trim resistor. The new value of R_3 can be found with the expandor gain equation

$$R_3 = \frac{R_1 \ R_2 \ I_B \ Gain}{2 \ V_{IN} \ avg}$$
$$= \frac{10k \ x \ 20k \ x \ 140\mu A \ x \ 2.6}{2 \ x \ 1.20}$$
$$= 30.3k$$

An external addition to R_3 of 10k is required, and this value can be selected to accurately set the high level gain.

A low level trim resistor from C_{RECT} to V_{CC} of about 3M provides matching of the Bell low-level tracking curve, and the 2μF value of C_{RECT} provides the proper attack and release times. A 16k resistor from the summing node to ground biases the output to $7V_{DC}$.

VOLTAGE-CONTROLLED ATTENUATOR

The variable gain cell in the NE570/571 may be used as the heart of a high quality voltage-controlled amplifier (VCA). Figure 16 shows a typical circuit which uses an external op amp for better performance, and an exponential converter to get a control characteristic of –6dB/V. Trim networks are shown to null out distortion and DC shift, and to fine trim gain to 0dB with 0V of control voltage.

Op amp A_2 and transistors Q_1 and Q_2 form the exponential converter generating an exponential gain control current, which is fed into the rectifier. A reference current of 150μA, (15V and R_{20}=100k), is attenuated a factor of two (6dB) for every volt increase in the control voltage. Capacitor C_6 slows down gain changes to a 20ms time constant ($C_6 \times R_1$) so that an abrupt change in the control voltage will produce a smooth sounding gain change. R_{18} assures that for large control voltages the circuit will go to full attenuation. The rectifier bias current would normally limit the gain reduction to about 70dB. R_{18} draws excess current out of the rectifier. After approximately 50dB of attenuation at a –6dB/V slope, the slope steepens and attenuation becomes much more rapid until the circuit totally shuts off at about 9V of control voltage. A_1 should be a low noise high slew rate op amp. R_{13} and R_{14} establish approximately a 0V bias at A_1's output.

With a 0V control voltage, R_{19} should be adjusted for 0dB gain. At 1V(–6dB gain) R_9 should be adjusted for minimum distortion with a large (+10dBm) input signal. The output DC bias (A_1 output) should be measured at full attenuation (+10V control voltage) and then R_8 is adjusted to give the same value at 0dB gain. Properly adjusted, the circuit will give typically less than 0.1% distortion at any gain with a DC output voltage variation of only a few millivolts. The clipping level (140μA into Pin 3, 14) is ±10V peak. A signal-to-noise ratio of 90dB can be obtained.

If several VCAs must track each other, a common exponential converter can be used. Transistors can simply be added in parallel with Q_2 to control the other channels. The transistors should be maintained at the same temperature for best tracking.

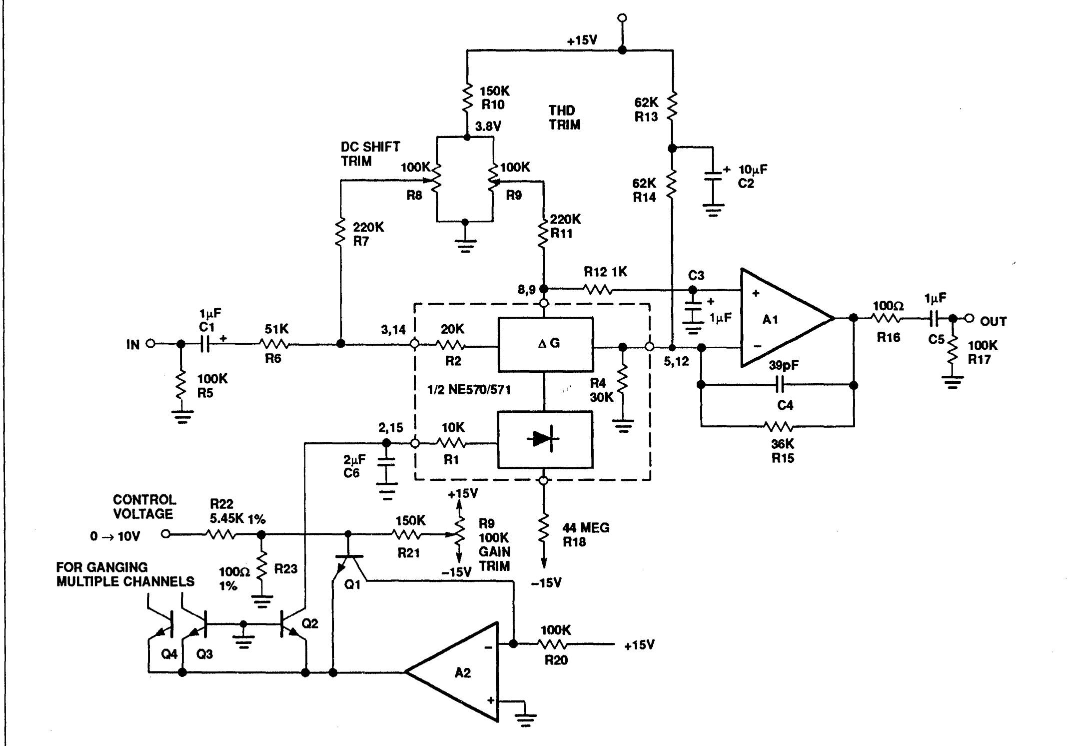


Figure 16. Voltage-Controlled Attenuator

AUTOMATIC LEVEL CONTROL

The NE570 can be used to make a very high performance ALC as shown in Figure 17. This circuit hook-up is very similar to the basic compressor shown in Figure 2 except that the rectifier input is tied to the input rather than the output. This makes gain inversely proportional to input level so that a 20dB drop in input level will produce a 20dB increase in gain. The output will remain fixed at a constant level. As shown, the circuit will maintain an output level of ±1dB for an input range of +14 to −43dB at 1kHz. Additional external components will allow the output level to be adjusted. Some relevant design equations are:

$$Output\ level = \frac{R_1\ R_2\ I_B}{2\ R_3} \left(\frac{V_{IN}}{V_{IN}\ (avg)}\right)$$

$$I_B = 140\mu A$$

$$Gain = \frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (avg)} \quad where$$

$$\frac{V_{IN}}{V_{IN}\ (avg} = \frac{\pi}{2\sqrt{2}} = 1.11\ (for\ sine\ wave)$$

If ALC action at very low input levels is not desired, the addition of resistor R_X will limit the maximum gain of the circuit.

$$Gain\ max = \frac{\frac{R_1 + R_X}{1.8V}\ x\ R_2\ x\ I_B}{2\ R_3}$$

The time constant of the circuit is determined by the rectifier capacitor, C_{RECT}, and an internal 10k resistor.

$$\tau = 10k\ C_{RECT}$$

Response time can be made faster at the expense of distortion. Distortion can be approximated by the equation:

$$THD = \left(\frac{1\mu F}{C_{RECT}}\right)\left(\frac{1kHz}{freq.}\right)\ x\ 0.2\%$$

VARIABLE SLOPE COMPRESSOR-EXPANDOR

Compression and expansion ratios other than 2:1 can be achieved by the circuit shown in Figure 18. Rotation of the dual potentiometer causes the circuit hook-up to change from a basic compressor to a basic expandor. In the center of rotation, the circuit is 1:1, has neither compression nor expansion. The (input) output transfer characteristic is thus continuously variable from 2:1 compression, through 1:1 up to 1:2 expansion. If a fixed compression or expansion ratio is desired, proper selection of fixed resistors can be used instead of the potentiometer. The optional threshold resistor will make the compression or expansion ratio deviate towards 1:1 at low levels. A wide variety of (input) output characteristics can be created with this circuit, some of which are shown in Figure 18.

HI-FI COMPANDOR

The NE570 can be used to construct a high performance compandor suitable for use with music. This type of system can be used for noise reduction in tape recorders, transmission systems, bucket brigade delay lines, and digital audio systems. The circuits to be described contain features which improve performance, but are not required for all applications.

A major problem with the simple NE570 compressor (Figure 2) is the limited op amp gain at high frequencies.

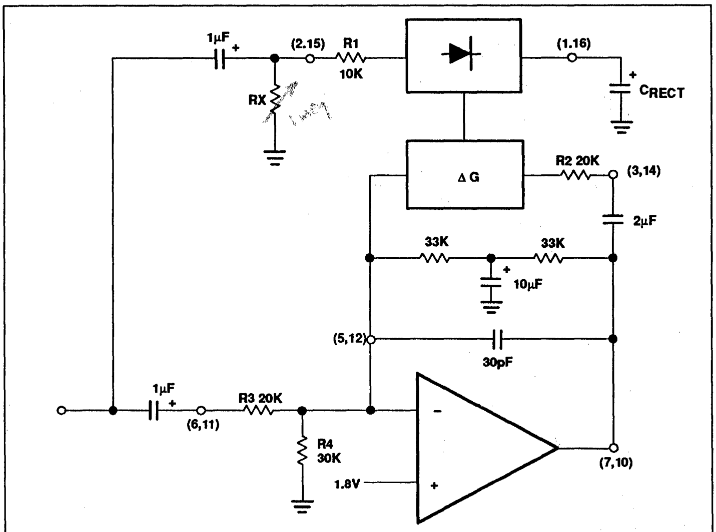


Figure 17. Automatic Level Control

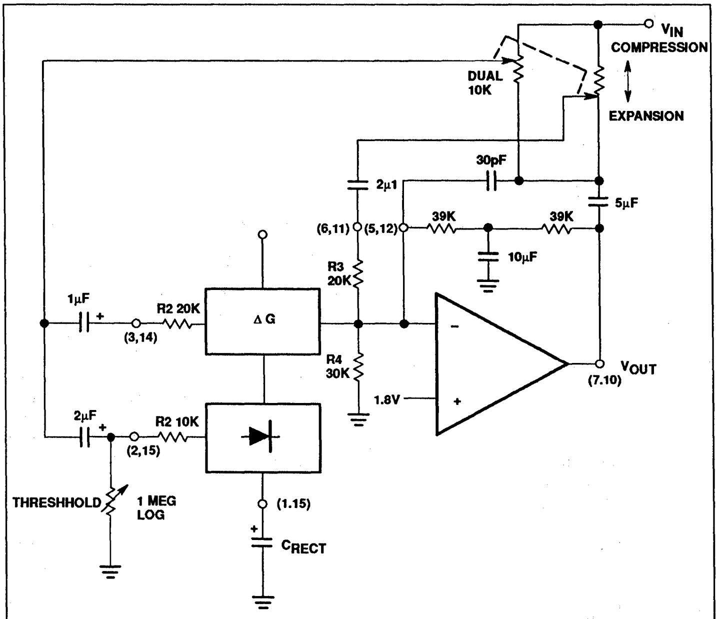


Figure 18. Variable Slope Compressor-Expandor

For weak input signals, the compressor circuit operates at high gain and the 570 op amp simply runs out of loop gain. Another problem with the 570 op amp is its limited slew rate of about 0.6V/μs. This is a limitation of the expandor, since the expandor is more likely to produce large output signals than a compressor.

Figure 20 is a circuit for a high fidelity compressor which uses an external op amp and has a high gain and wide bandwidth. An input compensation network is required for stability.

Another feature of the circuit in Figure 20 is that the rectifier capacitor (C_9) is not grounded, but is tied to the output of an op amp circuit. This circuit, built around an LM324, speeds up the compressor attack time at low signal levels. The response times of the simple expandor and compressor (Figures 1 and 2) become longer at low signal levels. The time constant is not simply $10k \times C_{RECT}$, but is really:

$$\left(10k + 2\left(\frac{0.026V}{I_{RECT}}\right)\right) x\ C_{RECT}$$

When the rectifier input level drops from 0dBm to –30dBm, the time constant increases from $10.7k \times C_{RECT}$ to $32.6k \times C_{RECT}$. In systems where there is unity gain between the compressor and expandor, this will cause no overall error. Gain or loss between the compressor and expandor will be a mistracking of low signal dynamics. The circuit with the LM324 will greatly reduce this problem for systems which cannot guarantee the unity gain.

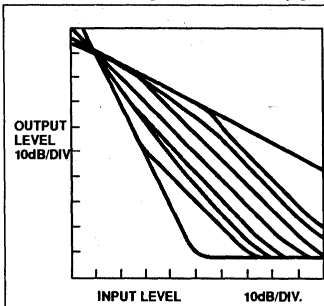


Figure 19. Typical Input-Output Tracking Curves of Variable Ratio Compressor-Expandor

When a compressor is operating at high gain, (small input signal), and is suddenly hit with a signal, it will overload until it can reduce its gain. Overloaded, the output will attempt to swing rail to rail. This compressor is limited to approximately a $7V_{P-P}$ output swing by the brute force clamp diodes D_3 and D_4. The diodes cannot be placed in the feedback loop because their capacitance would limit high frequency gain. The purpose of limiting the output swing is to avoid overloading any succeeding circuit such as a tape recorder input.

The time it takes for the compressor to recover from overload is determined by the rectifier capacitor C_9. A smaller capacitor will allow faster response to transients, but will produce more low frequency third harmonic distortion due to gain modulation. A value of 1μF seems to be a good compromise value and yields good subjective results. Of course, the expandor should have exactly the same value rectifier capacitor for proper transient response. Systems which have good low frequency amplitude and phase response can use compandors with smaller rectifier capacitors, since the third harmonic distortion which is generated by the compressor will be undistorted by the expandor.

Simple compandor systems are subject to a problem known as breathing. As the system is changing gain, the change in the background noise level can sometimes be heard.

The compressor in Figure 20 contains a high frequency pre-emphasis circuit (C_2, R_5 and C_8, R_{14}), which helps solve this problem. Matching de-emphasis on the expandor is required. More complex designs could make the pre-emphasis variable and further reduce breathing.

The expandor to complement the compressor is shown in Figure 21. Here an external op amp is used for high slew rate. Both the compressor and expandor have unity gain levels of 0dB. Trim networks are shown for distortion (THD) and DC shift. The distortion trim should be done first, with an input of 0dB at 10kHz. The DC shift should be adjusted for minimum envelope bounce with tone bursts. When applied to consumer tape recorders, the subjective performance of this system is excellent.

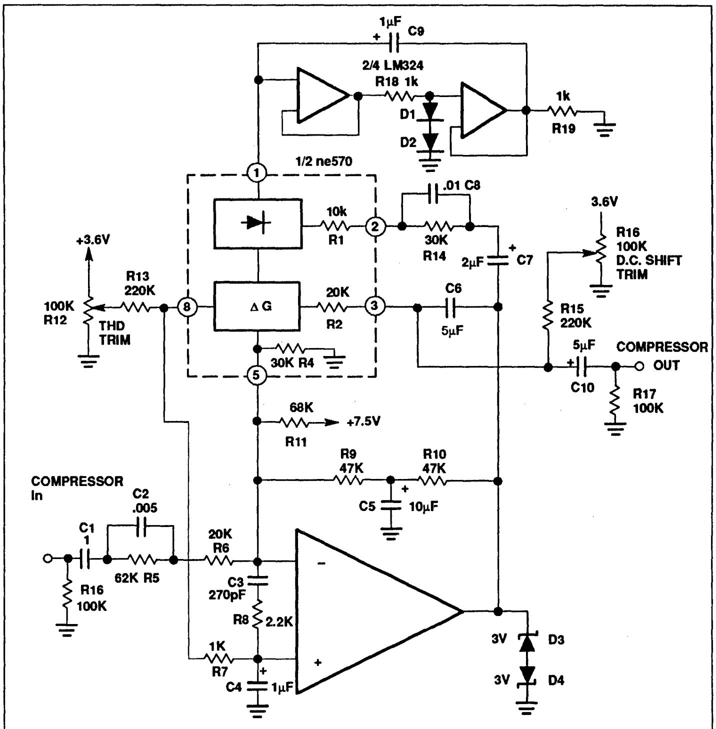


Figure 20. Hi-Fi Compressor With Pre-emphasis

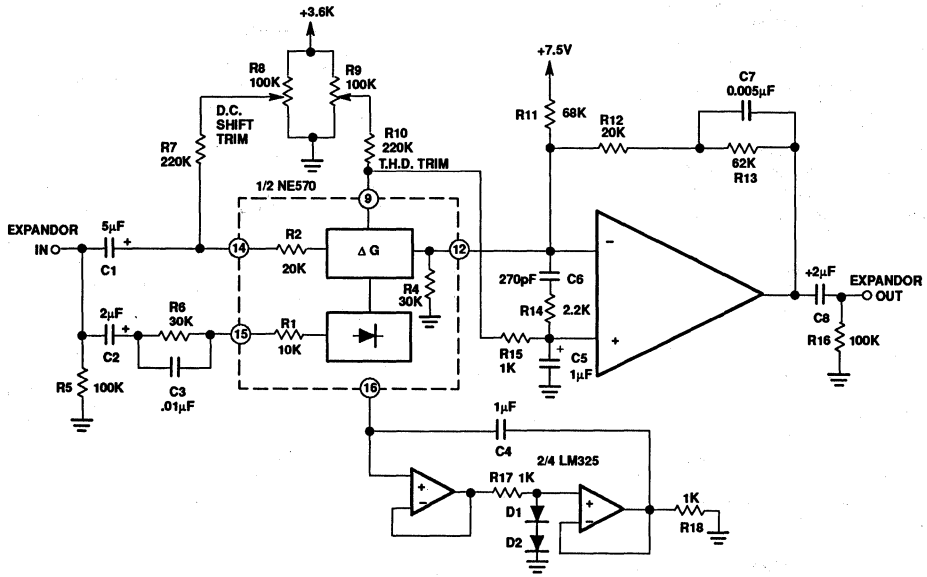


Figure 21. Hi-Fi Expandor With De-emphasis

Compandor cookbook
AN176

Compandors are versatile, low cost, dual-channel gain control devices for audio frequencies. They are used in tape decks, cordless telephones, and wireless microphones performing noise reduction. Electronic organs, modems and mobile telephone equipment use compandors for signal level control.

So what is companding? Why do it at all? What happens when we do it? Compandor is the contraction of the two words compressor and expandor. There is one basic reason to compress a signal before sending it through a telephone line or recording it on a cassette tape: to process that signal (music, speech, data) so that all parts of it are above the inherent noise floor of the transmission medium and yet not running into the max. dynamic range limits, causing clipping and distortion. The diagrams below demonstrate the idea; they are not totally correct because in the real world of electronics the 3kHz tone is riding on the 1kHz tone. They are shown separated for better explanation.

Figure 1 is the signal from the source. Figure 2 shows the noise always in the transmission medium. Figure 3 shows the max limits of the transmission medium and what happens when a signal larger than those limits is sent through it. Figure 4 is the result of compressing the signal (note that the larger signal would not be clipped when transmitted).

The received/playback signal is processed (expanded) in exactly the same — only inverted — ratio as the input signal was compressed. The end result is a clean, undistorted signal with a high signal-to-noise ratio.

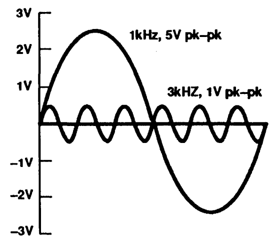


Figure 1. Original Signal Input

Figure 2. Wide-Band Noise Floor of Transmission Line

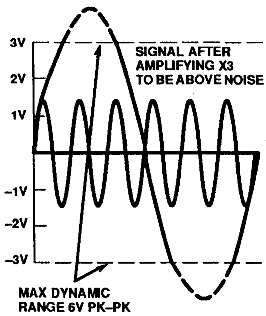


Figure 3.

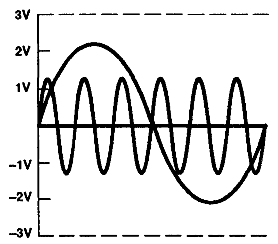


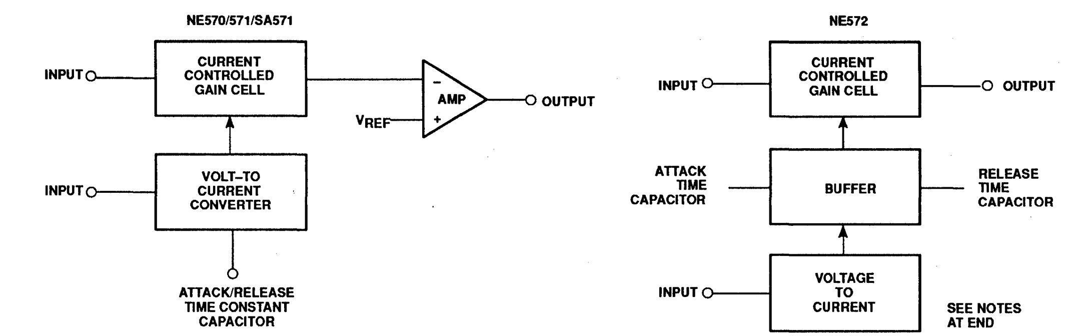
Figure 4. Signal After Compression

This document has been designed to give the reader a basic working knowledge of the Signetics Compandor family. The analyses of three primary applications will be accompanied by "recipes" describing how to select external components (for both proper operation and function modification). Schematic and artwork for an application board are also provided. For comprehensive technical information consult the Compandor Product Guide or the Linear Data Manual.

The basic blocks in a compandor are the current-controlled variable gain cell (ΔG), voltage-to-current converter (rectifier), and operational amplifier. Each Signetics compandor package has two identical, independent channels with the following block diagrams (notice that the 570/71 is different from the 572).

The operational amplifier is the main signal path and output drive.

BLOCK DIAGRAMS



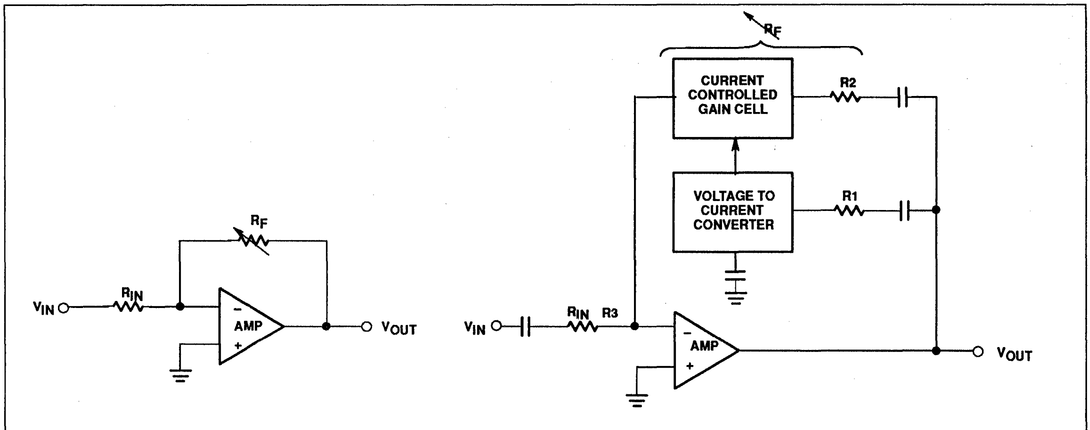


Figure 5. Basic Compressor

The full-wave averaging rectifier measures the AC amplitude of a signal and develops a control current for the variable gain cell.

The variable gain cell uses the rectifier control current to provide variable gain control for the operational amplifier gain block.

The compandor can function as a Compressor, Expandor, and Automatic Level Controller or as a complete compressor/expandor system as described in the following:

1) The COMPRESSOR function processes uncontrolled input signals into controlled output signals. The purpose of this is to avoid distortion caused by a narrow dynamic range medium, such as telephone lines, RF and satellite transmissions, and magnetic tape. The Compressor can also limit the level of a signal.

2) The EXPANDOR function allows a user to increase the dynamic range of an incoming compressed signal such as radio broadcasts.

3) The compressor/expandor system allows a user to retain dynamic range and reduce the effects of noise introduced by the transmission medium.

4) The AUTOMATIC LEVEL CONTROL (ALC) function (like the familiar automatic gain control) adjusts its gain proportionally with the input amplitude. This ALC circuit therefore transforms a widely varying input signal into a fixed amplitude output signal without clipping and distortion.

HOW TO DESIGN COMPANDOR CIRCUITS

The rest of the cookbook will provide you with basic compressor, expandor, and automatic level control application information. A NE570/571 has been used in all of the circuits. If high-fidelity audio or separately programmable attack and decay time are needed, the NE572 with a low noise op amp should be used.

The compressor (see Figure 5) utilizes all basic building blocks of the compandor. In this configuration, the variable gain cell is placed in the feedback loop of the standard inverting amplifier circuit. The gain equation is $A_V=-R_F/R_{IN}$. As shown above, the variable gain cell acts as a variable feedback resistor (R_F) (See Figure 5).

As the input signal increases above the crossover level of 0dB, the variable resistor decreases in value. This causes the gain to decrease, thus limiting the output amplitude.

Below the crossover level of 0dB, an increase in input signal causes the variable resistor to increase in value, thereby causing the output signal's amplitude to increase.

In the compressor configuration, the rectifier is connected to the output.

The complete equation for the compressor gain is:

$$Gain\ comp. = \left[\frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (avg)}\right]^{\frac{1}{2}}$$

where: $R_1 = 10k$
$R_2 = 20k$
$R_3 = 20k$
$I_B = 140\mu A$

$V_{IN}(avg)=0.9(V_{IN(RMS)})$

COMPRESSOR RECIPE

1) DC bias the output half way between the supply and ground to get maximum headroom. The circuit in Figure 6 is designed around a system supply of 6V, thus the output DC level should be 3V.

$$V_{OUT\ DC}=(1+(2R_{DC}/R_4))\ V_{REF}$$

where: R_4=30k
V_{REF}=1.8V
R_{DC} is external

manipulating the equation, the result is. . .

$$R_{DC} = \left(\left(\frac{V_{OUT}}{V_{REF}}\right) - 1\right)\frac{R_4}{2}$$

Note that the $C_{(DC)}$ should be large enough to totally short out any AC in this feedback loop.

2) Analyze the OUTPUT signal's anticipated amplitude.

a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section)

b) if larger than 3.0V peak, R_1 will also need to be increased.

By limiting the peak input currents we avoid signal distortion.

3) The input and output coupling caps need to be large enough not to attenuate any desired frequencies ($X_C=1/(6.28xf)$).

4) The C_{RECT} should be 1μF to 2μF for initial setup. This directly affects Attack and Release times.

5) An input buffer may be necessary if the source's output impedance needs matching.

6) Pre-emphasis may be used to reduce noisepumping, breathing, etc., if present. See the NE570/571 data sheet for specific details.

7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. Refer to data sheet for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.

8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network. (This technique prevents infinite compression at low input levels.)

The EXPANDOR utilizes all the basic building blocks of the compandor (see Figure 7). In this configuration the variable gain cell is placed in the inverting input lead of the operational amplifier and acts as a variable input resistance, R_{IN}. The basic gain equation for operational amplifiers in the standard inverting feedback loop is $A_V=-R_F/R_{IN}$.

As the input amplitude increases above the crossover level of 0dBM, this variable resistor decreases in value, causing the gain to increase, thus forcing the output amplitude to increase (refer to Figure 10).

Below the crossover level, an increase in input amplitude causes the variable resistor to increase in value, thus forcing the output amplitude to decrease.

The complete equation for the expandor gain is:

$$\text{Gain expandor}=(2R_3V_{IN}(avg))/R_1R_2I_B$$

where: $R_1 = 10k$
$R_2 = 20k$
$R_3 = 20k$
$I_B = 140\mu A$

$$V_{IN}(avg)=0.9\ (V_{IN(RMS)})$$

In the expandor configuration the rectifier is connected to the input.

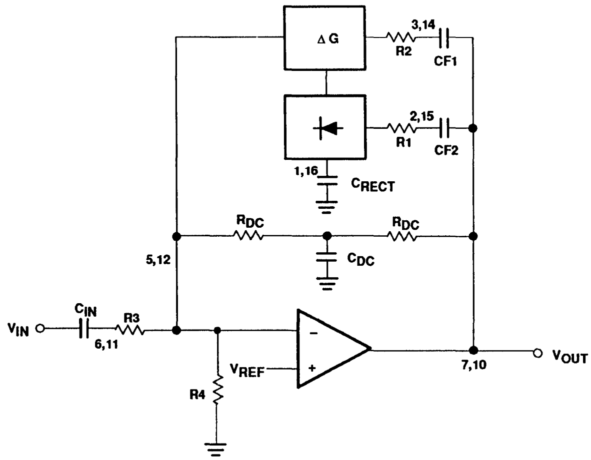


Figure 6. Basic Compressor

EXPANDOR RECIPE

1) DC bias the output halfway between the supply and ground to get maximum headroom. The circuit in Figure 8 is designed around a system supply of 6V so the output DC level should be 3V.

$$V_{OUT\ DC}=(1+R_3/R_4)V_{REF}$$

where: $R_3 = 20k$
$R_4 = 30k$
$V_{REF} = 1.8V$

Note that when using a supply voltage higher than 6V the DC output level should be adjusted. To increase the DC output level, it is recommended that R_4 be decreased by adding parallel resistance to it. (Changing R_3 would also affect the expandor's AC gain and thus cause a mismatch in a companding system.)

2) Analyze the input signal's anticipated amplitude:

a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section)

b) if larger than 3.0V peak, R_1 will also need to be increased. (see INGREDIENTS)

By limiting the peak input currents we avoid signal distortion.

3) The input and output decoupling caps need to be large enough not to attenuate any desired frequencies.

4) The C_{RECT} should be 1μF to 2μF for initial setup.

5) An input buffer may be necessary if the source's output impedance needs matching.

6) De-emphasis would be necessary if the complementary compressor circuit had been pre-emphasized (as in a tape deck application). See the Hi-Fi Expandor application in the Linear Data Manual.

7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. See Linear Data Manual for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.

8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network (see Linear Data Manual). (This technique prevents infinite expansion at low input levels.)

In the ALC configuration, (Figure 9), the variable gain cell is placed in the feedback loop of the operational amplifier (as in the Compressor) and the rectifier is connected to the input.

As the input amplitude increases above the crossover point, the overall system gain decreases proportionally, holding the output amplitude constant.

As the input amplitude decreases below the crossover point, the overall system gain increases proportionally, holding the output amplitude at the same constant level.

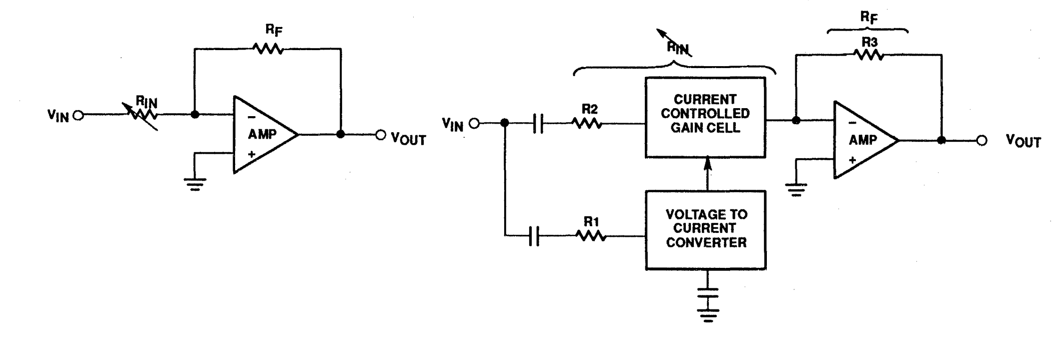


Figure 7. Basic Expandor

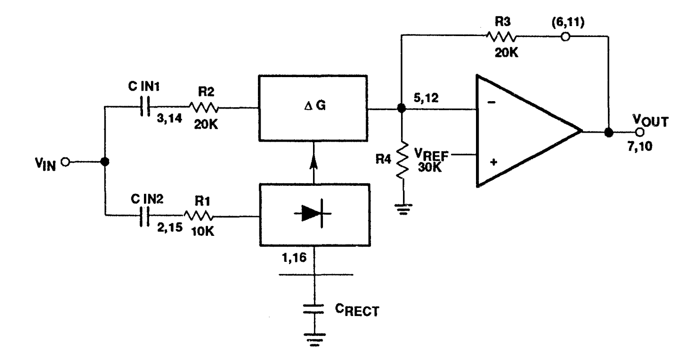


Figure 8. Basic Expandor

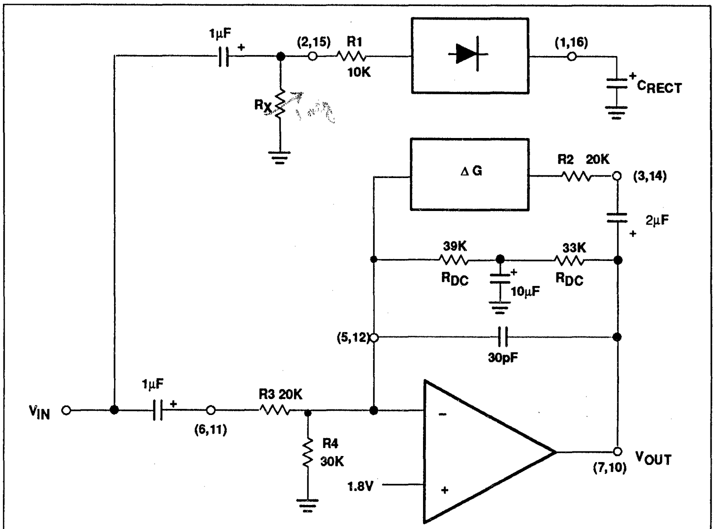


Figure 9. Automatic Level Control

The complete gain equation for the ALC is:

$$Gain = \frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (avg)}$$

$$Output\ Level = \frac{R_1\ R_2\ I_B}{2\ R_3}\left(\frac{V_{IN}}{V_{IN}\ (avg)}\right)$$

$$where\ \frac{V_{IN}}{V_{IN}\ (avg)} = \frac{\pi}{2\sqrt{2}} = 1.11\ (for\ sine\ wave)$$

Note that for very low input levels, ALC may not be desired and to limit the maximum gain, resistor R_X has been added. The modified gain equation is:

$$Gain\ max. = \frac{(R_1 + R_X)\cdot R_2 \cdot I_B}{2\ R_3}$$

$R_X \cong$ ((desired max gain)×26k)–10k

INGREDIENTS

[Application guidelines for internal and external components (and input/output constraints) needed to tailor (cook) each of the three entrees (applications) to your taste.]

R_1 (10kΩ) limits input current to the rectifier. This current should not exceed an AC peak value of ±300µA. An external resistor may be placed in series with R_1 if the input voltage to the rectifier will exceed ±3.0V peak (i.e., 10k×300µA=3.0V).

R_2 (20kΩ) limits input current to the variable gain cell. This current should not exceed an AC peak value of ±140µA. Again, an external resistor has to be placed in series with R_2 if the input voltage to the variable gain cell exceeds ±2.8V (i.e., 20k×140µA).

R_3 (20kΩ) acts in conjunction with R_4 as the feedback resistor (R_F) (expandor configuration) in the equation. (R_3's value can be either reduced or increased externally.) However, it is recommended that R_4 be the one to change when adjusting the output DC level.

R_4 (30kΩ) acts as the input resistor (R_{IN}) in the standard non-inverting op amp circuit. (Its value can only be reduced.)

$V_{OUT\ DC}=(1+(R_3/R_4))V_{REF}$
(for the Expandor)
$V_{OUT\ DC}=(1+(2R_{DC}/R_4))V_{REF}$
(for the Compandor, ALC)

[The purpose of these DC biasing equations is to allow the designer to set the output halfway between the supply rails for largest headroom (usually some positive voltage and ground).]

C_{DC} acts as an AC shunt to ground to totally remove the DC biasing resistors from the AC gain equation.

C_F caps are AC signal coupling caps.

C_{RECT} acts as the rectifier's filter cap and directly affects the response time of the circuit. There is a trade-off, though, between fast attack and decay times and distortion.

The time constant is: $10k \times C_{RECT}$

The total harmonic distortion (THD) is approximated by:

$THD \cong (1\mu F/C_{RECT})(1kHz/freq.) \times 0.2\%$

NOTES:
The NE572 differs from the 570/571 in that:
1. There is no internal op amp.
2. The attack and release times are programmed separately.

SYSTEM LEVELS OF A COMPLETE COMPANDING SYSTEM

Figure 10 demonstrates the compressing and expanding functions:

Point A represents a wide dynamic range signal with a maximum amplitude of +16dB and minimum amplitude of –80dB.

Point B represents the compressor output showing a 2:1 reduction in dynamic range (–40dB is increased to –20dB, for example). Point B can also be seen as the dynamic range of a transmission medium. Transmission noise is present at the –60dB level from Point B to Point C.

Point C represents the input signal to the expandor.

Point D represents the output of the expandor. The signal transformation from Point C to D represents a 1:2 expansion.

APPLICATION BOARD

Shown below is the schematic (Figure 11) for Signetics' NE570/571 evaluation/demo board. This board provides one channel of Expansion and one channel of Compression (which can be switched to Automatic Level Control).

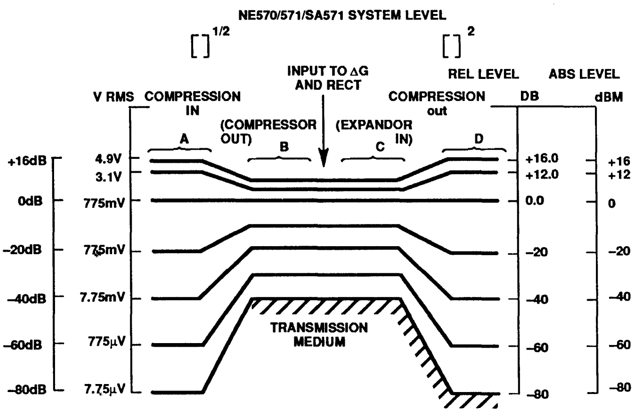


Figure 10. System Levels of a Complete Companding System

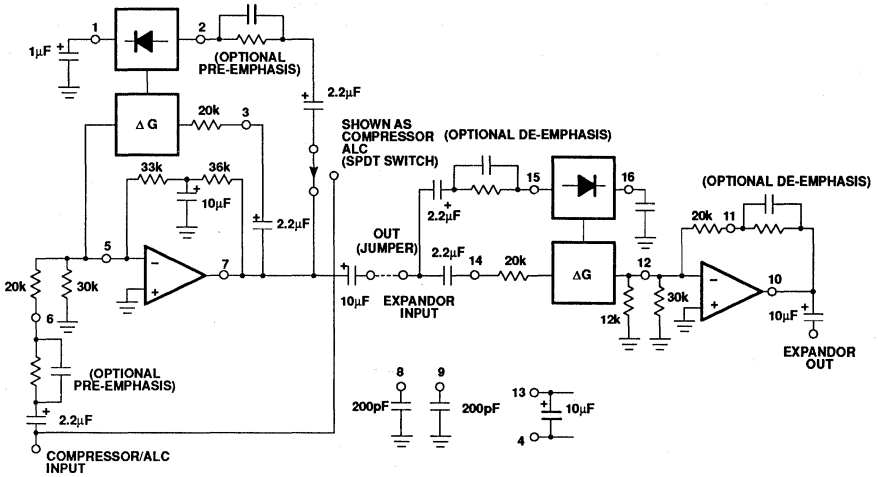

1µF
1
2
(OPTIONAL PRE-EMPHASIS)
2.2µF
ΔG
20k
3
SHOWN AS COMPRESSOR ALC (SPDT SWITCH)
(OPTIONAL DE-EMPHASIS)
33k
36k
10µF
2.2µF
15
16
(OPTIONAL DE-EMPHASIS)
2.2µF
20k
11
OUT (JUMPER)
2.2µF
14
20k
ΔG
12
5
7
10
20k
30k
10µF
EXPANDOR INPUT
12k
30k
10µF
6
EXPANDOR OUT
(OPTIONAL PRE-EMPHASIS)
8
9
200pF
200pF
13
10µF
4
2.2µF
COMPRESSOR/ALC INPUT

Figure 11.

Programmable analog compandor

NE/SA572

DESCRIPTION

The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

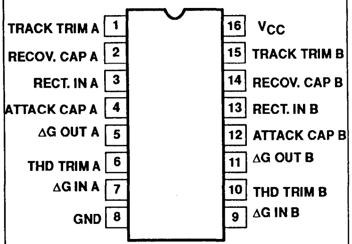
- Independent control of attack and recovery time
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external op amp
- Wide dynamic range—greater than 110dB
- Temperature-compensated gain control
- Low distortion gain cell
- Low noise—6μV typical
- Wide supply voltage range—6V-22V
- System level adjustable with external components

APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expandor
- Automatic level control
- High-level limiter
- Low-level noise gate
- State variable filter

PIN CONFIGURATION

D[1], N, F Packages



NOTE:
1. D package released in large SO (SOL) package only.

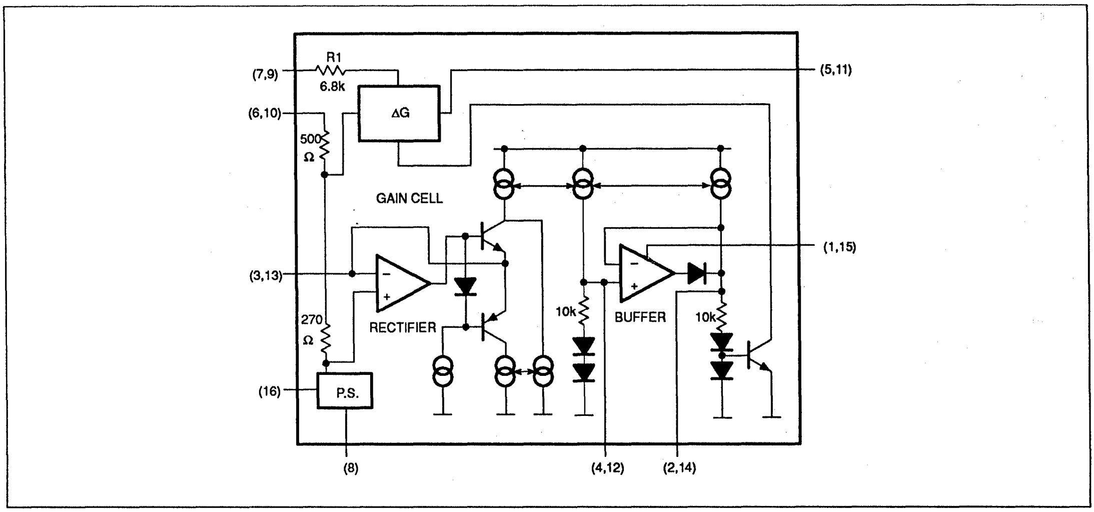
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE572D
16-Pin Plastic DIP	0 to +70°C	NE572N
16-Pin Plastic SO	–40 to +85°C	SA572D
16-Pin Cerdip	–40 to +85°C	SA572F
16-Pin Plastic DIP	–40 to +85°C	SA572N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	V_{DC}
T_A	Operating temperature range		
	NE572	0 to +70	°C
	SA572	–40 to +85	
P_D	Power dissipation	500	mW

BLOCK DIAGRAM

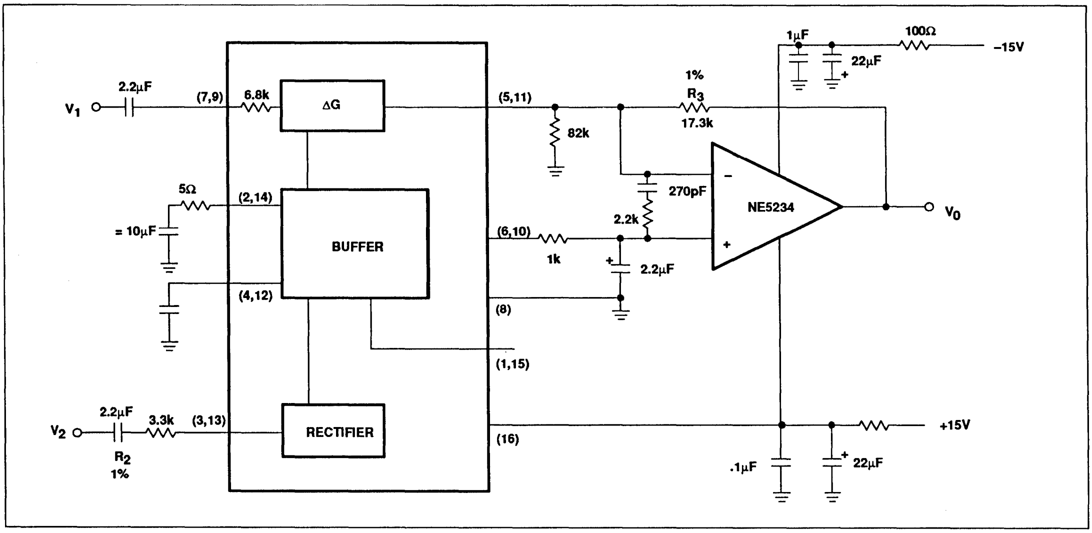


DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) V_{CC}=15V, T_A=25°C; Expandor mode (see Test Circuit). Input signals at unity gain level (0dB) = 100mV_{RMS} at 1kHz; $V_1 = V_2$; $R_2 = 3.3kΩ$; $R_3 = 17.3kΩ$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE572			SA572			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		22	6		22	V_{DC}
I_{CC}	Supply current	No signal			6			6.3	mA
V_R	Internal voltage reference		2.3	2.5	2.7	2.3	2.5	2.7	V_{DC}
THD	Total harmonic distortion (untrimmed)	1kHz C_A=1.0μF		0.2	1.0		0.2	1.0	%
THD	Total harmonic distortion (trimmed)	1kHz C_R=10μF		0.05			0.05		%
THD	Total harmonic distortion (trimmed)	100Hz		0.25			0.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20–20kHz)		6	25		6	25	μV
	DC level shift (untrimmed)	Input change from no signal to 100mV_{RMS}		±20	±50		±20	±50	mV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dB
	Large–signal distortion	V_1=V_2=400mV		0.7	3.0		0.7	3	%
	Tracking error (measured relative to value at unity gain)= [V_O–V_O (unity gain)]dB –V_2dB	Rectifier input V_2=+6dB V_1=0dB V_2=–30dB V_1=0dB		±0.2 ±0.5	−1.5 +0.8		±0.2 ±0.5	−2.5 +1.6	dB
	Channel crosstalk	200mV_{RMS} into channel A, measured output on channel B	60			60			dB
PSRR	Power supply rejection ratio	120Hz		70			70		dB

TEST CIRCUIT



AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10k resistor R_A defines the attack time t_A. The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10k resistor R_R. Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1μF and 1.0μF attack capacitors, respectively. Recovery time of 200ms can be obtained with a 4.7μF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0-70 The SA572 is intended for applications from –40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs Q_1-Q_2 and Q_3-Q_4 are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of Q_1-Q_2 and the V_{BE} of Q_3-Q_4 equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q3Q4}} = \Delta_{BE_{Q1Q2}}$$

$$(V_{BE} = V_T \; I_{IN} \; IC/IS)$$

$$V_T ln\left(\frac{\frac{1}{2}I_G+\frac{1}{2}I_O}{I_S}\right) - V_T ln\left(\frac{\frac{1}{2}I_G-\frac{1}{2}I_O}{I_S}\right)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

$$V_T ln\left(\frac{I_1+I_{IN}}{I_S}\right) - V_T ln\left(\frac{I_2-I_1-I_{IN}}{I_S}\right) \quad (2)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \quad (3)$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within ±25μA into the THD trim pin.

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only 6μV in the audio spectrum (10Hz-20kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

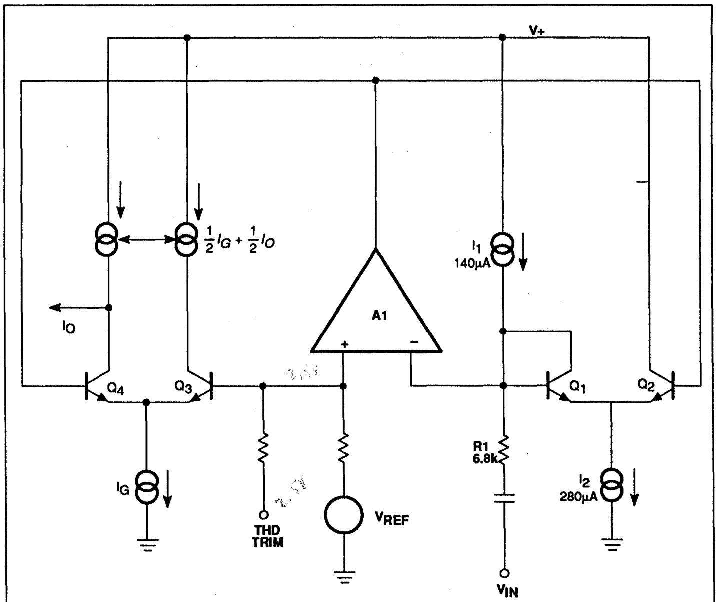


Figure 1. Basic Gain Cell Schematic

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (4)$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN}(AVG)}{R_2}$$

The internal bias scheme limits the maximum output current I_R to be around 300μA. Within a ±1dB error band the input range of the rectifier is about 52dB.

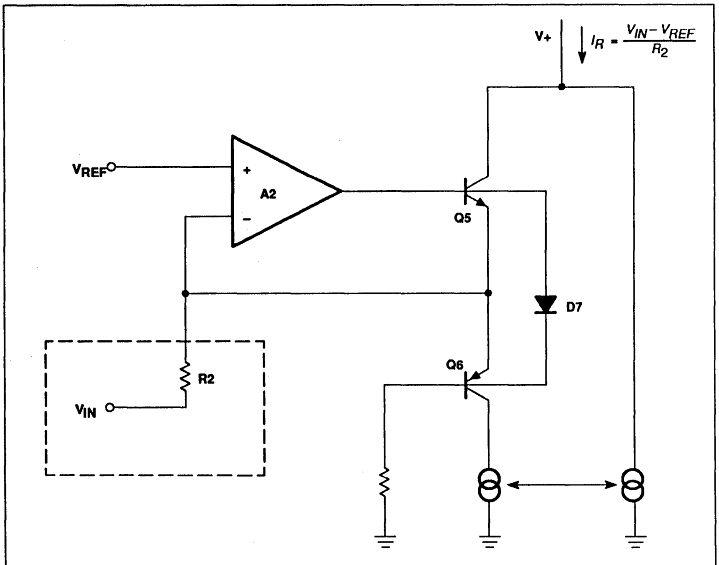


Figure 2. Simplified Rectifier Schematic

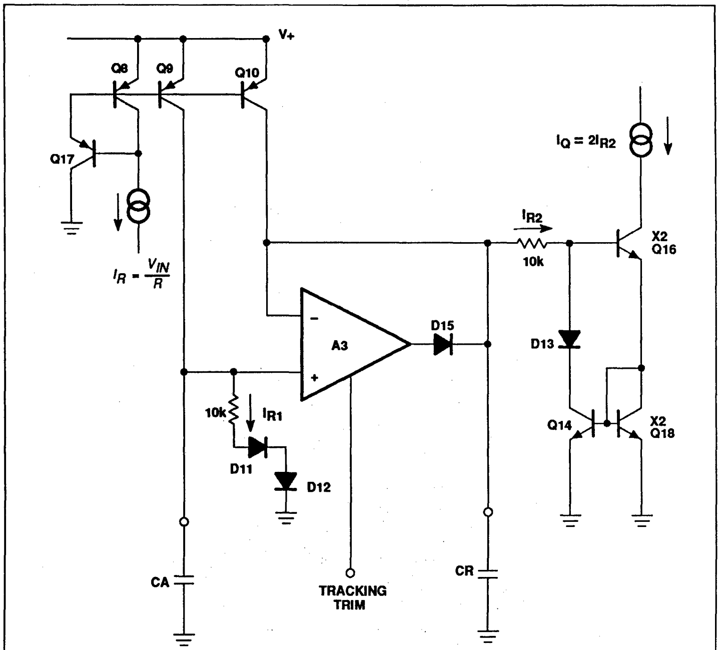


Figure 3. Buffer Amplifier Schematic

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL}\; e^{\frac{-t}{\tau A}} + Ga_{FNL}$$

Ga_{INT}=Initial Gain

Ga_{FNL}=Final Gain

$\tau_A = R_A \bullet CA = 10k \bullet CA$

where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{RINT} - G_{RFNL}\; e^{\frac{-t}{\tau R}} + G_{RFNL}$$

$G_R(t) = (G_{R\,INT} - G_{R\,FNL})\; e + G_{R\,FNL}$

$\tau R = R_R \bullet CR = 10k \bullet CR$

where τR is the recovery time constant and R_R is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of $\pm 3\mu A$.

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \qquad (5)$$

(I_1=140µA)

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140µA. This corresponds to a voltage level of 140µA • 6.8k=952mV peak. The input peak current into the rectifier is limited to 300µA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B \frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant. *5COL

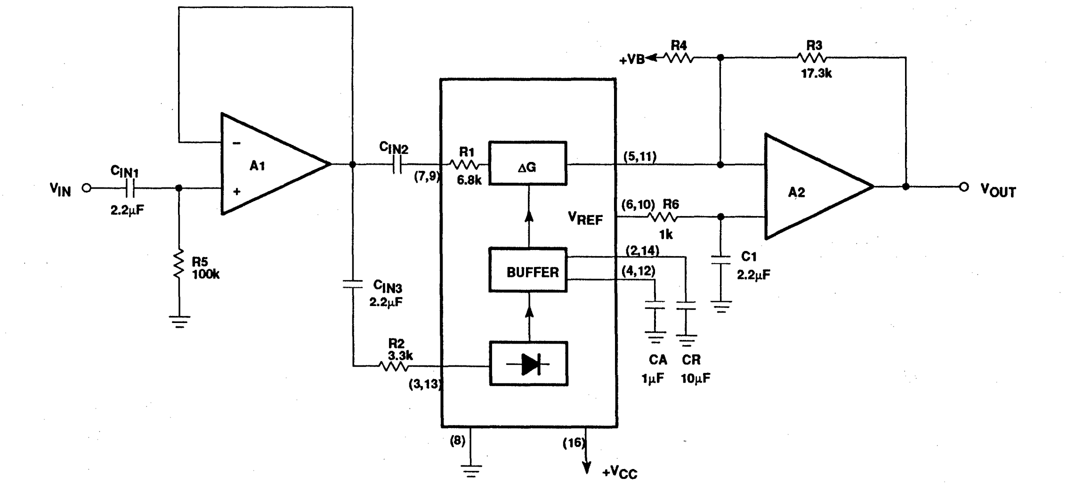


Figure 4. Basic Expandor Schematic

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}}\right)^{\frac{1}{2}} \quad (7)$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4}\right) \quad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

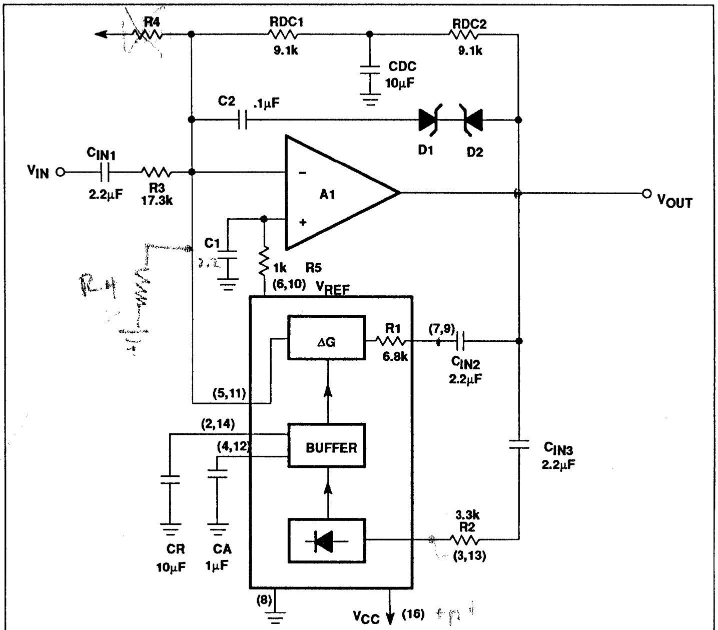


Figure 5. Basic Compressor Schematic

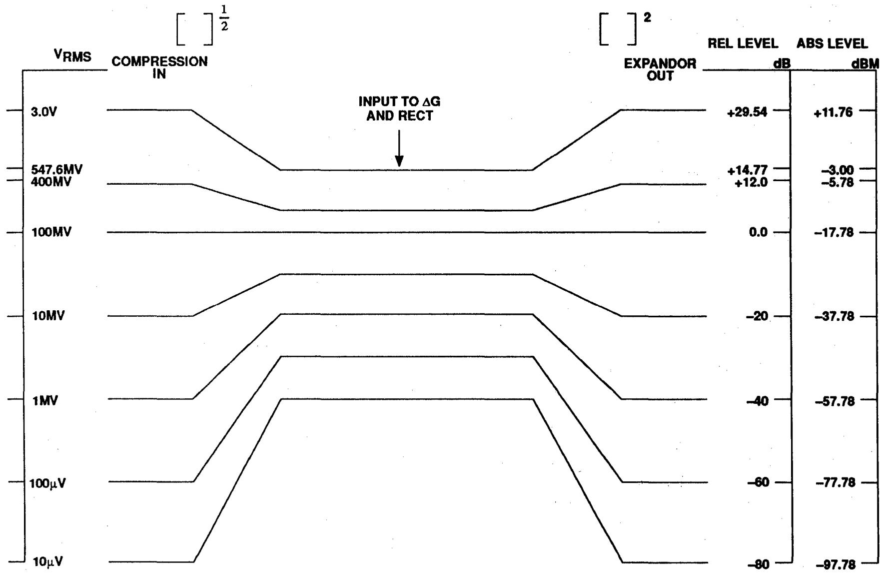
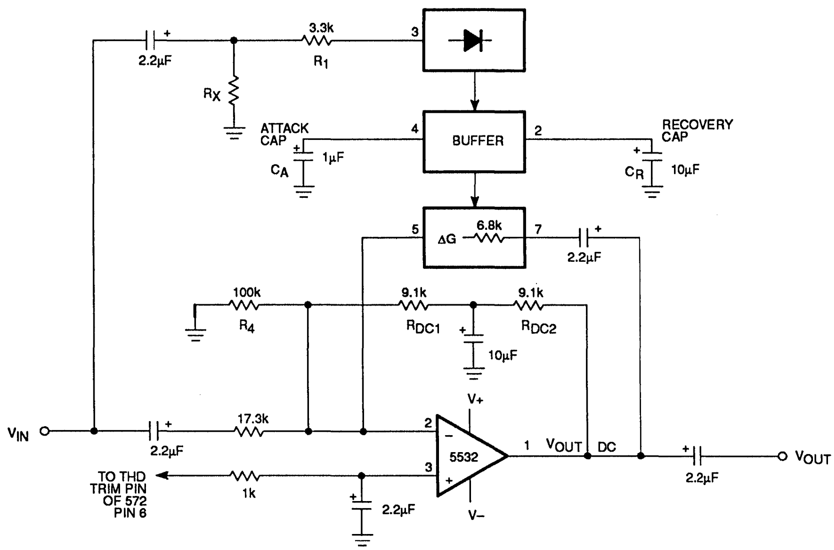


Figure 6. NE572 System Level

NE572 AUTOMATIC LEVEL CONTROL



$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right)$$

WHERE: $R_4 = 100k$
$R_{DC1} = R_{DC2} = 9.1k$
$V_{REF} = 2.5V$

$$OUTPUT\ LEVEL = \left(\frac{R_1\ R_2\ I_B}{2R_3}\right)\left(\frac{V_{IN}}{V_{IN(avg)}}\right)$$

WHERE: $R_1 = 6.8k$ (Internal)
$R_2 = 3.3k$
$R_3 = 17.3k$
$I_B = 140\mu A$

$$Gain = \frac{R_1\ R_2\ I_B}{2R_3\ V_{IN}\ (avg)}$$

ATTACK TIME = (10k) C_A

RECOVERY TIME = (10k) C_R

TO LIMIT THE GAIN AT VERY LOW INPUT LEVELS, ADD R_X:

$$GAIN\ MAX. = \frac{\frac{R_1 + R_X}{2.5V} \times R_2 \times I_B}{2R_3}$$

$$\frac{V_{IN}}{V_{IN(avg)}} = \frac{\pi}{2\sqrt{2}} = 1.11$$

(FOR SINE WAVES)

NOTE:
Pin numbers are for side A of the NE572.

Low voltage compandor

NE/SA575

DESCRIPTION

The NE/SA575 is a precision dual gain control circuit designed for low voltage applications. The NE575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

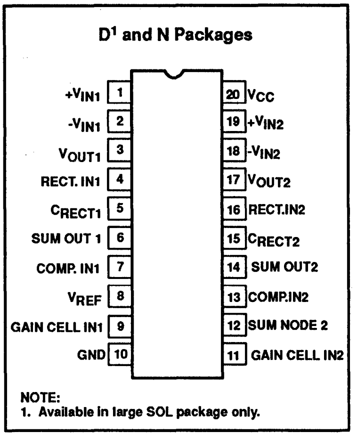
FEATURES

- Operating voltage range from 3V to 7V
- Reference voltage of $100mV_{RMS}$ = 0dB
- One dedicated summing op amp per channel and two extra uncommitted op amps
- 600Ω drive capability
- Single or split supply operation
- Wide input/output swing capability

APPLICATIONS

- Portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Portable broadcast mixers
- Wireless microphones
- Modems
- Electric organs
- Hearing aids

PIN CONFIGURATION



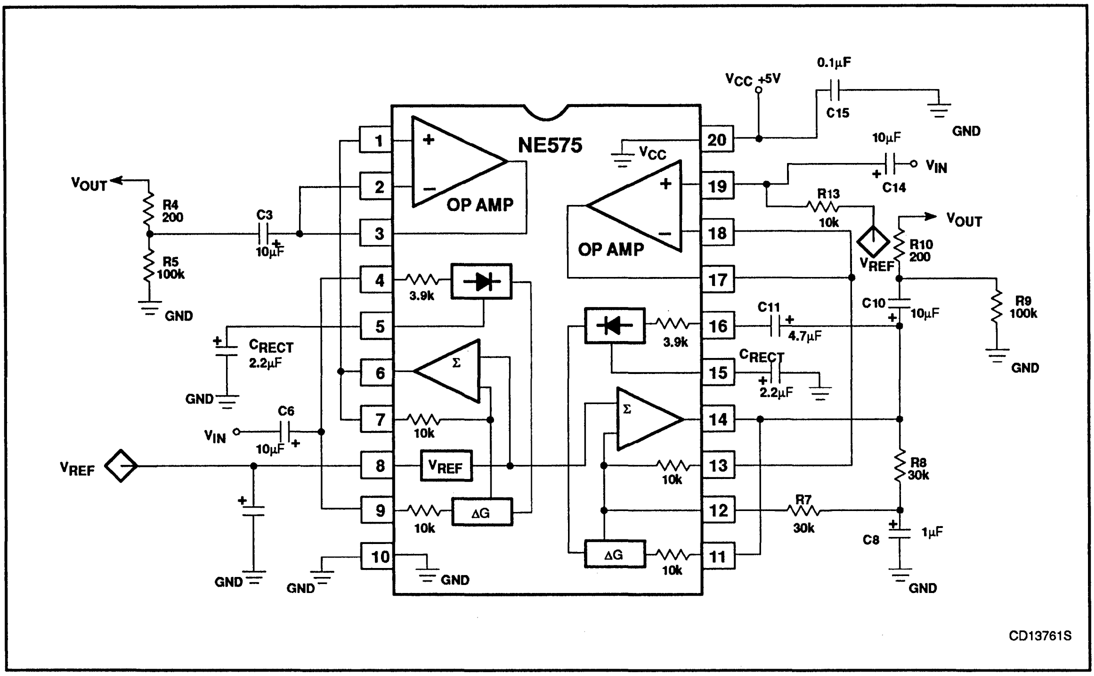
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE575N
20-Pin Plastic SOL	0 to +70°C	NE575D
20-Pin Plastic DIP	-40 to +85°C	SA575N
20-Pin Plastic SOL	-40 to +85°C	SA575D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE575	SA575	
V_{CC}	Single supply voltage	8	8	V
T_A	Operating ambient temperature range	-40 to +85	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C
θ_{JA}	Thermal impedance DIP	68	68	°C/W
	SOL	112	112	°C/W

BLOCK DIAGRAM and TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 25°C. Minimum and Maximum values are for the full operating temperature range: 0 to 70°C for NE575, -40 to +85°C for SA575. V_{CC} = 5V, unless otherwise stated. Both channels are tested in the Expandor mode (see Test Circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
For compandor, including summing amplifier									
V_{CC}	Supply voltage[1]		3	5	7	3	5	7	V
I_{CC}	Supply current	No signal	3	4.2	5.5	3	4.2	5.5	mA
V_{REF}	Reference voltage[2]	V_{CC} = 5V	2.4	2.5	2.6	2.4	2.5	2.6	V
R_L	Summing amp output load		10			10			kΩ
THD	Total harmonic distortion	1kHz, 0dB BW = 3.5kHz		0.12	1.0		0.12	1.5	%
E_{NO}	Output voltage noise	BW = 20kHz, R_S = 0Ω		6	20		6	30	μV
0dB	Unity gain level	1kHz	-1.0		1.0	-1.5		1.5	dB
V_{OS}	Output voltage offset	No signal	-100		100	-150		150	mV
	Output DC shift	No signal to 0dB	-50		50	-100		100	mV
	Tracking error relative to 0dB	Gain cell input = 0dB, 1kHz Rectifier input = 6dB, 1kHz	-0.5		0.5	-1.0		1.0	dB
		Gain cell input = 0dB, 1kHz Rectifier input = -30dB, 1kHz	-0.5		0.5	-1.0		1.0	dB
	Crosstalk	1kHz, 0dB, C_{REF} = 220μF		-80	-65		-80	-65	dB

DC ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
For operational amplifier									
V_O	Output swing	$R_L = 10k\Omega$	V_{CC}-0.4	V_{CC}-0.2		V_{CC}-0.4	V_{CC}-0.2		V
R_L	Output load	1kHz	600			600			Ω
CMR	Input common-mode range		0		V_{CC}	0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		60	80		dB
I_B	Input bias current	V_{IN} = 0.5V to 4.5V	-0.5		0.5	-1		1	μA
V_{OS}	Input offset voltage			3			3		mV
A_{VOL}	Open-loop gain	$R_L = 10k\Omega$		80			80		dB
SR	Slew rate	Unity gain		1			1		V/μs
GBW	Bandwidth	Unity gain		3			3		MHz
E_{NI}	Input voltage noise	BW = 20kHz		2.5			2.5		μV
PSRR	Power supply rejection ratio	1kHz, 250mV		60			60		dB

NOTES:
1. Operation down to V_{CC} = 2V is possible, but performance is significantly reduced. See curve in Figure 5.
2. Reference voltage, V_{REF}, is typically at 1/2V_{CC}.

FUNCTIONAL DESCRIPTION

This section describes the basic subsystems and applications of the NE/SA575 Compandor. More theory of operation on compandors can be found in AN174 and AN176. The typical applications of the NE575 low voltage compandor in an Expandor (1:2), Compressor (2:1) and Automatic Level Control (ALC) function are explained. These three circuit configurations are shown in Figures 1, 2, 3 respectively.

The NE575 has two channels for a complete companding system. The left channel, A, can be configured as a 1:2 Expandor while the right channel, B, can be configured as either a 2:1 Compressor, a 1:2 Expandor or an ALC. Each channel consists of the basic companding building blocks of rectifier cell, variable gain cell, summing amplifier and V_{REF} cell. In addition, the NE575 has two additional high performance uncommitted op amps which can be utilized for application such as filtering, pre-emphasis/de-emphasis or buffering.

Figure 4 shows the complete schematic for the applications demo board. Channel A is configured as an expandor while channel B is configured so that it can be used either as a compressor or as an ALC circuit. The switch, S1, toggles the circuit between compressor and ALC mode. Jumpers J1 and J2 can be used to either include the additional op amps for signal conditioning or exclude them from the signal path. Bread boarding space is provided for R1, R2, C1, C2, R10, R11, C10 and C11 so that the response can be tailored for each individual need. The components as specified are suitable for the complete audio spectrum from 20Hz to 20kHz.

The most common configuration is as a unity gain non-inverting buffer where R1, C1, C2, R10, C10 and C11 are eliminated and R2 and R11 are shorted. Capacitors C3, C5, C8, and C12 are for DC blocking, and R4 and R8 provide termination (for the capacitors). In systems where the inputs and outputs are AC coupled, these capacitors and resistors can be eliminated. Capacitors C4 and C9 are for setting the attack and release time constant.

C6 is for decoupling and stabilizing the voltage reference circuit. The value of C6 should be such that it will offer a very low impedance to the lowest frequencies of interest. Too small a capacitor will allow supply ripple to modulate the audio path. The better filtered the power supply, the smaller this capacitor can be. R5 and R12 provide DC reference voltage to the amplifiers of channel B. R6 and R7 provide a DC feedback path for the summing amp of channel B, while C7 is a short-circuit to ground for signals. C14 and C15 are for power supply decoupling. C14 can also be eliminated if the power supply is well regulated with very low noise and ripple. Figure 8 shows the PC board layout of the applications demo board.

DEMONSTRATED PERFORMANCE

The applications demo board was built and tested for a frequency range of 20Hz to 20kHz with the component values as shown in Figure 4 and V_{CC} = 5V. In the expandor mode, the typical input dynamic range was from -34dB to +12dB where 0dB is equal to 100mV$_{RMS}$. The typical unity gain level measured at 0dB @ 1kHz input was ±0.5dB and the typical tracking error was ±0.1dB for input range of -30 to +10dB.

In the compressor mode, the typical input dynamic range was from -42dB to ±18dB with a tracking error +0.1dB and the typical unity gain level was ±0.5dB.

In the ALC mode, the typical input dynamic range was from -42dB to +8dB with typical output deviation of ±0.2dB about the nominal output of 0dB. For input greater than +9dB in ALC configuration, the summing amplifier sometimes exhibits high frequency oscillations. There are several solutions to this problem. The first is to lower the values of R7 and R8 to 20kΩ each. the second is to add a current limiting resistor in series with C13 at Pin 13. the third is to add a compensating capacitor of about 22 to 30pF between the input and output of summing amplifier (Pins 12 and 14). With any one of the above recommendations, the typical ALC mode input range increased to +18dB yielding a dynamic range of over 60dB.

EXPANDOR

The typical expandor configuration is shown in Figure 1. The variable gain cell and the rectifier cell are in the signal input path. The V_{REF} is always 1/2 V_{CC} to provide the maximum headroom without clipping. The 0dB ref is 100mV$_{RMS}$. The input is AC coupled through C5, and the output is AC coupled through C3. If in a system the inputs and outputs are AC coupled, then C3, C5, R3 and R4 can be eliminated, thus requiring only one external component, C4. The variable gain cell and rectifier cell are DC coupled so any offset voltage between Pins 4 and 9 will cause small offset error current in the rectifier cell. This will affect the accuracy of the gain cell. This can be improved by using an extra capacitor from the input to Pin 4 and eliminating the DC connection between Pins 4 and 9.

The expandor gain expression and the attach and release time constant is given by Equation 1 and Equation 2, respectively.

Equation 1.

$$\text{Expandor gain} = \frac{4V_{IN}(avg)}{3.9k \times 100\mu A}$$

where $V_{IN}(avg) = 0.975V_{IN(RMS)}$

Equation 2.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

COMPRESSOR

The typical compressor configuration is shown in Figure 2. In this mode, the rectifier cell and variable gain cell are in the feedback path. R6 and R7 provide the DC feedback to the summing amplifier. The input is AC coupled through C12 and output is AC coupled through C8. In a system with inputs and outputs AC coupled, C8, C12, R8, and R9 could be eliminated and only R5, R6, R7, C7, and C13 would be required. If the external components R5, R6, R7 and C7 are eliminated, then the output of the summing amplifier will motor-boat in absence of signals or at extremely low signals. This is because there is no DC feedback path from the output to input. In the presence of an AC signal this phenomenon is not observed and the circuit will appear to function properly.

The compressor gain expression and the attack and release time constant is given by Equation 3 and Equation 4, respectively.

Equation 3.

$$\text{Compressor gain} = \left[\frac{3.9k \times 100\mu A}{4V_{IN}(avg)}\right]^{1/2}$$

where $V_{IN}(avg) = 0.975V_{IN(RMS)}$

Equation 4.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

AUTOMATIC LEVEL CONTROL

The typical Automatic Level Control circuit configuration is shown in Figure 3. It can be seen that it is quite similar to the compressor schematic except that the input to the rectifier cell is from the input path and not from the feedback path. The input is AC coupled through C12 and C13 and the output is AC coupled through C8. Once again, as in the previous cases, if the system input and output signals are already AC coupled, then C12, C13, C8, R8 and R9 could be eliminated. Concerning the compressor, removing R5, R6, R7 and C7 will cause motor-boating in absence of signals. C_{COMP} is necessary to stabilize the summing amplifier at higher input levels. This circuit provides an input dynamic range greater than 60dB with the output within ±0.5dB typical. The necessary design expressions are given by Equation 5 and Equation 6, respectively.

Equation 5.

$$\text{ALC gain} = \frac{3.9k \times 100\mu A}{4V_{IN}(avg)}$$

Equation 6.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C9$$

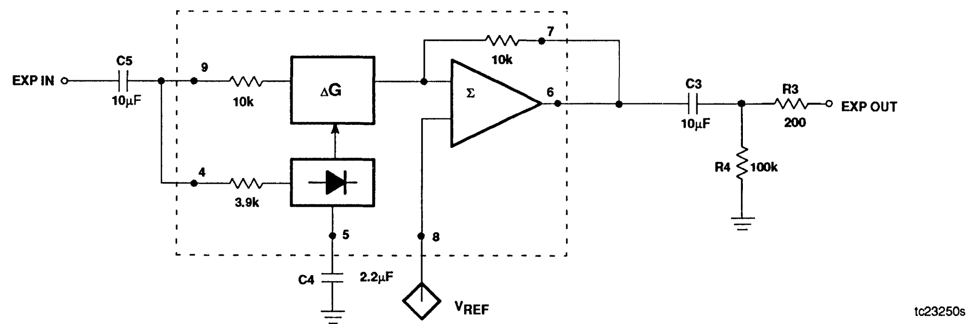


Figure 1. Typical Expandor Configuration

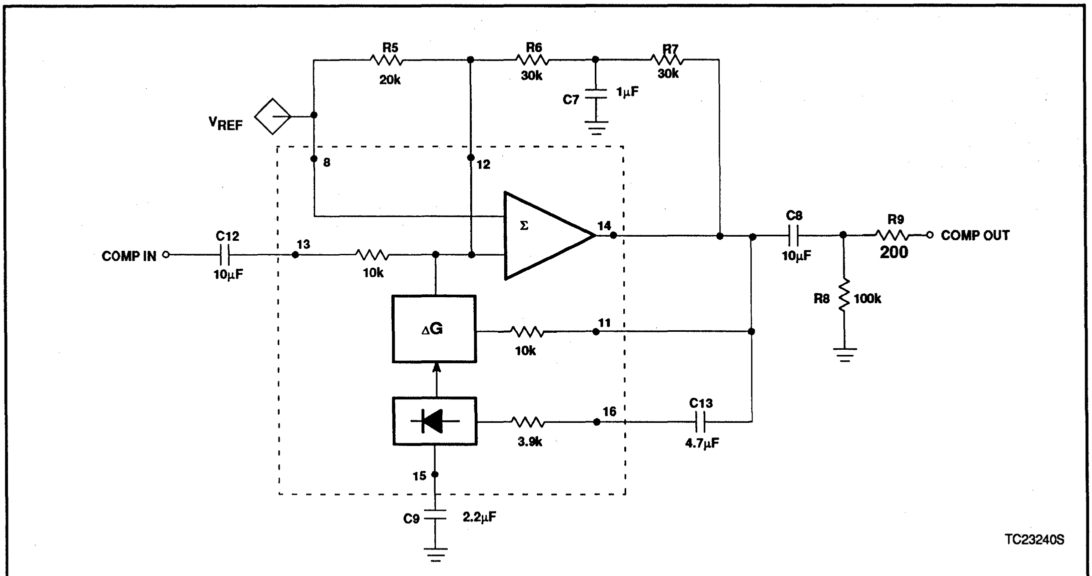


Figure 2. Typical Compressor Configuration

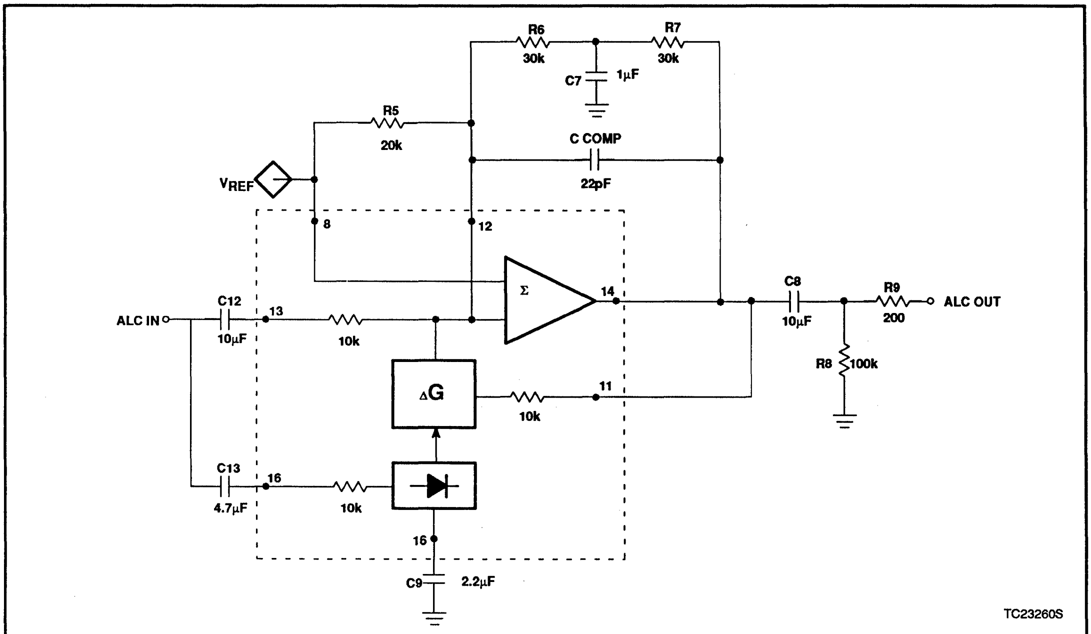


Figure 3. Typical ALC Configuration

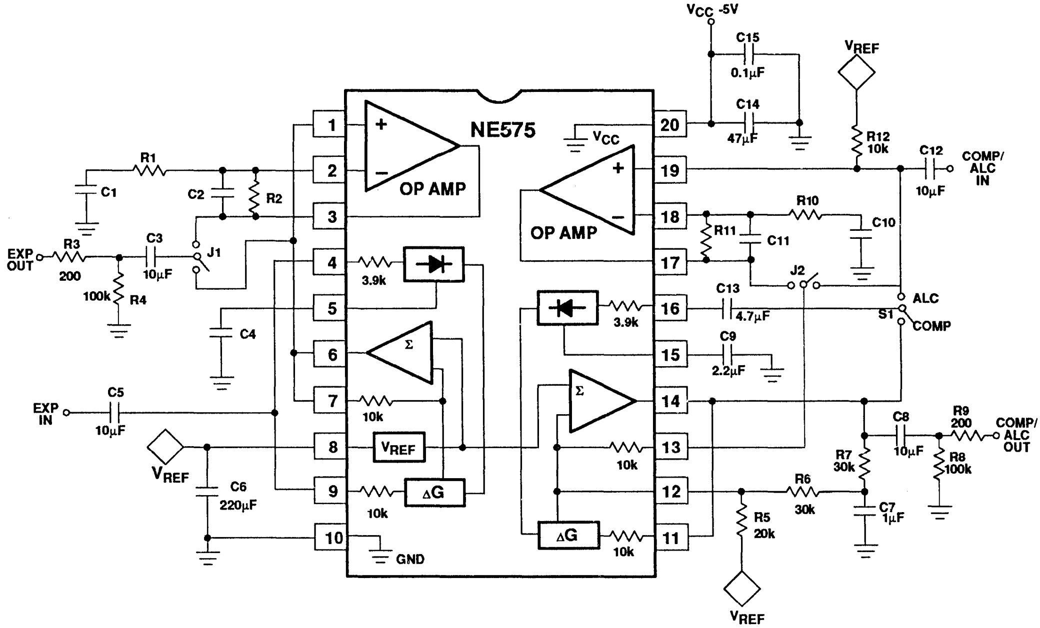


Figure 4. Signetics NE575 Low Voltage Expandor/Compressor/ALC Demo Board

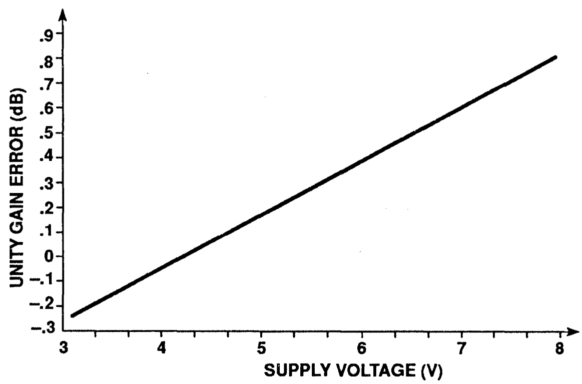


Figure 5. Unity Gain Error vs Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

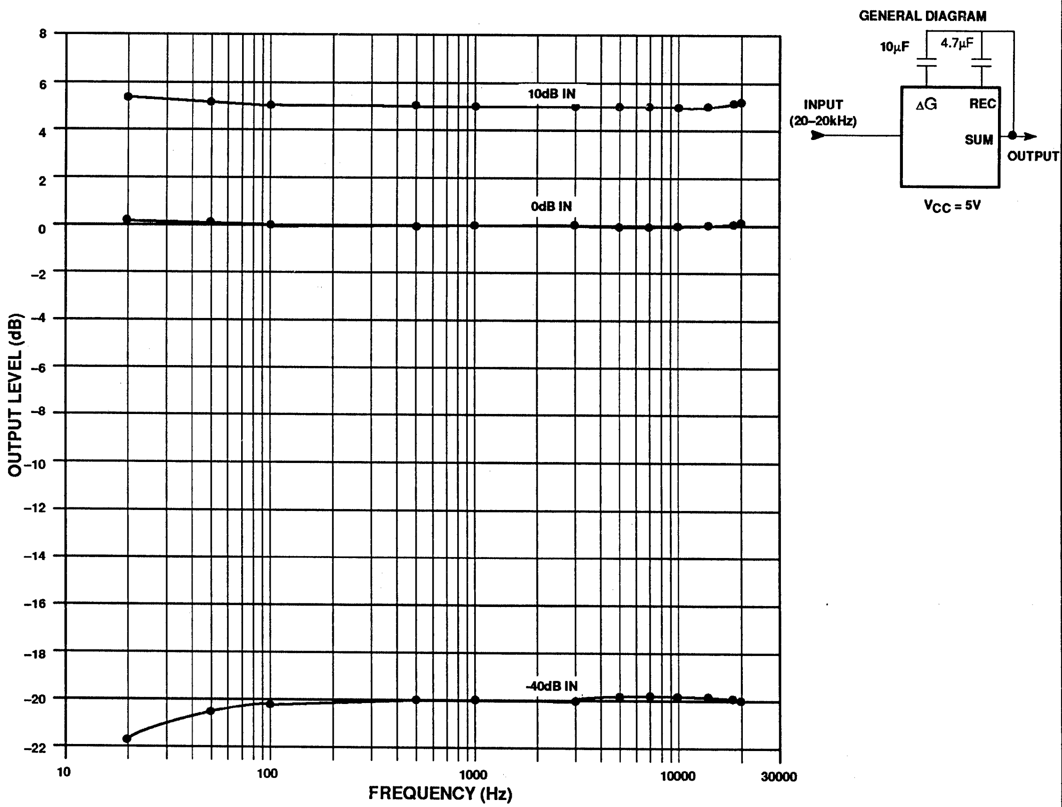


Figure 6. Compressor Output Frequency Response

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

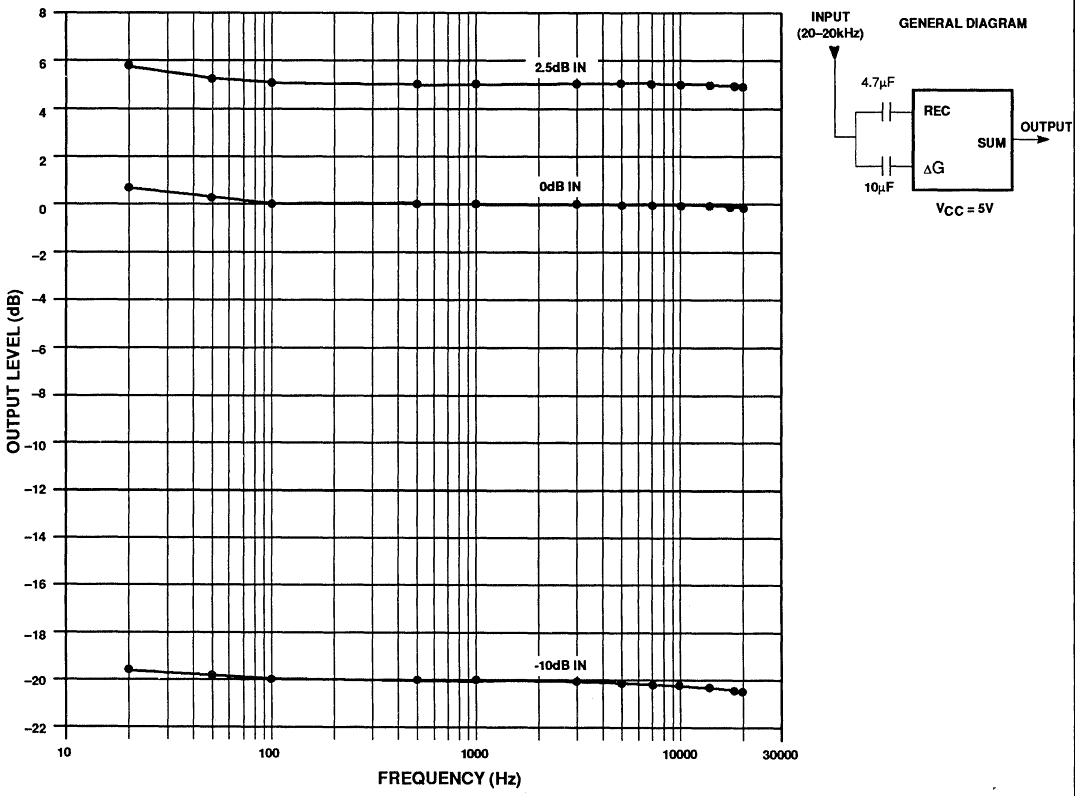
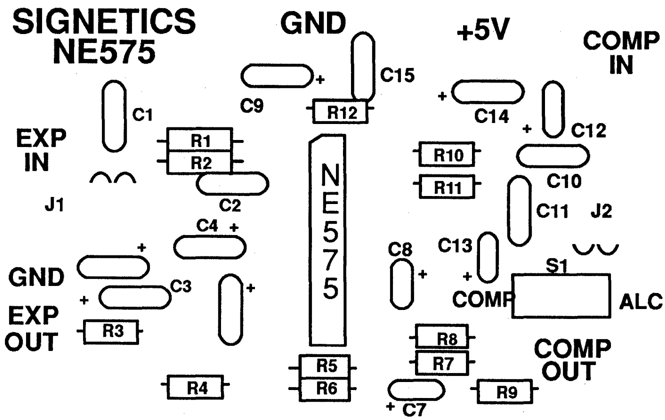
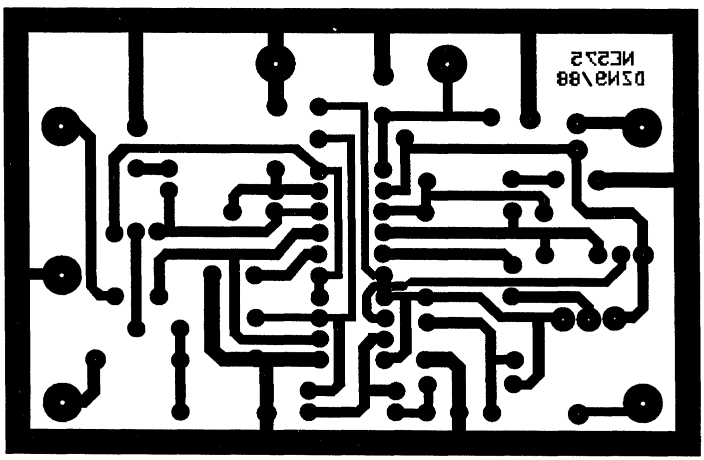


Figure 7. NE575 Expandor Output Frequency Response



8a. Application Board Component Placement



8B. Application Board Layout

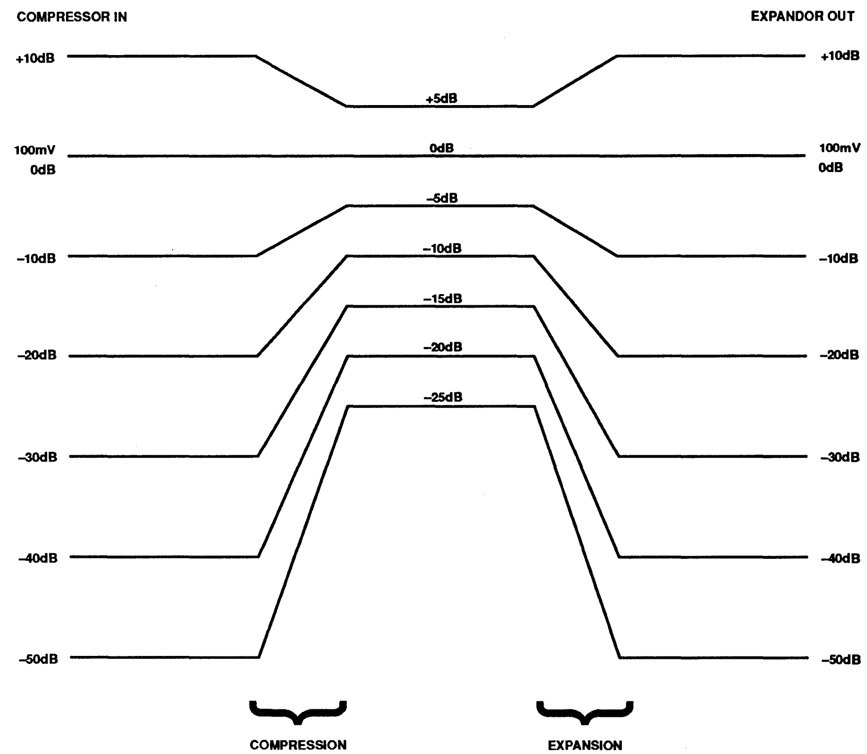


Figure 9. The Companding Function

Low voltage compandor in shrink small outline package

NE/SA575SSOP

DESCRIPTION

The NE/SA575 is a precision dual gain control circuit designed for low voltage applications. The NE575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

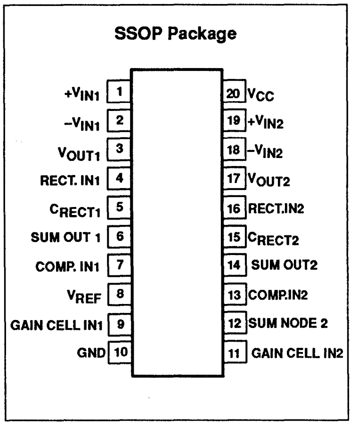
FEATURES

- Operating voltage range from 3V to 7V
- Reference voltage of $100mV_{RMS}$ = 0dB
- One dedicated summing op amp per channel and two extra uncommitted rail-to-rail op amps
- 600Ω drive capability
- Single or split supply operation
- Wide input/output swing capability
- DTMF summing

APPLICATIONS

- Portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Portable broadcast mixers
- Wireless microphones
- Modems
- Electric organs
- Hearing aids

PIN CONFIGURATION



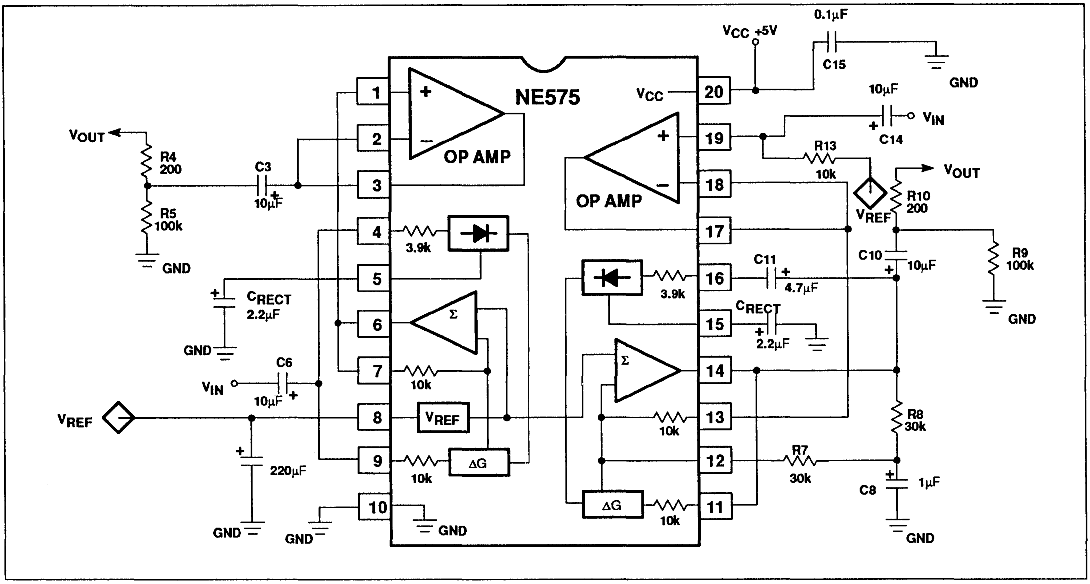
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SSOP	0 to +70°C	NE575DK
20-Pin Plastic SSOP	–40 to +85°C	SA575DK

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE575	SA575	
V_{CC}	Single supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance SSOP	117	117	°C/W

BLOCK DIAGRAM and TEST CIRCUIT



AC/DC ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$; $V_{CC} = 5V$, unless otherwise stated. Both channels are tested in the Expandor mode (see Test Circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
For compandor, including summing amplifier									
V_{CC}	Supply voltage[1]		3	5	7	3	5	7	V
I_{CC}	Supply current	No signal	3	4.2	5.5	3	4.2	5.5	mA
V_{REF}	Reference voltage[2]	$V_{CC} = 5V$	2.4	2.5	2.6	2.4	2.5	2.6	V
R_L	Summing amp output load		10			10			kΩ
THD	Total harmonic distortion	1kHz, 0dB BW = 3.5kHz		0.12	1.0		0.12	1.5	%
E_{NO}	Output voltage noise	BW = 20kHz, $R_S = 0\Omega$		6	20		6	30	µV
0dB	Unity gain level	1kHz	–1.0		1.0	–1.5		1.5	dB
V_{OS}	Output voltage offset	No signal	–100		100	–150		150	mV
	Output DC shift	No signal to 0dB	–50		50	–100		100	mV

AC/DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Tracking error relative to 0dB	Gain cell input = 0dB, 1kHz Rectifier input = 6dB, 1kHz	–0.5		0.5	–1.0		1.0	dB
		Gain cell input = 0dB, 1kHz Rectifier input = –30dB, 1kHz	–0.5		0.5	–1.0		1.0	dB
	Crosstalk	1kHz, 0dB, C_{REF} = 220µF		–80	–65		–80	–65	dB
For operational amplifier									
V_O	Output swing	R_L = 10kΩ	V_{CC}–0.4	V_{CC}–0.2		V_{CC}–0.4	V_{CC}–0.2		V
R_L	Output load	1kHz	600			600			Ω
CMR	Input common-mode range		0		V_{CC}	0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		60	80		dB
I_B	Input bias current	V_{IN} = 0.5V to 4.5V	–0.5		0.5	–1		1	µA
V_{OS}	Input offset voltage			3			3		mV
A_{VOL}	Open-loop gain	R_L = 10kΩ		80			80		dB
SR	Slew rate	Unity gain		1			1		V/µs
GBW	Bandwidth	Unity gain		3			3		MHz
E_{NI}	Input voltage noise	BW = 20kHz		2.5			2.5		µV
PSRR	Power supply rejection ratio	1kHz, 250mV		60			60		dB

NOTES:
1. Operation down to V_{CC} = 2V is possible, but performance is significantly reduced. See curve in Figure 5.
2. Reference voltage, V_{REF}, is typically at 1/2V_{CC}.

FUNCTIONAL DESCRIPTION

This section describes the basic subsystems and applications of the NE/SA575 Compandor. More theory of operation on compandors can be found in AN174 and AN176. The typical applications of the NE575 low voltage compandor in an Expandor (1:2), Compressor (2:1) and Automatic Level Control (ALC) function are explained. These three circuit configurations are shown in Figures 1, 2, 3 respectively.

The NE575 has two channels for a complete companding system. The left channel, A, can be configured as a 1:2 Expandor while the right channel, B, can be configured as either a 2:1 Compressor, a 1:2 Expandor or an ALC. Each channel consists of the basic companding building blocks of rectifier cell, variable gain cell, summing amplifier and V_{REF} cell. In addition, the NE575 has two additional high performance uncommitted op amps which can be utilized for application such as filtering, pre-emphasis/de-emphasis or buffering.

Figure 4 shows the complete schematic for the applications demo board. Channel A is configured as an expandor while channel B is configured so that it can be used either as a compressor or as an ALC circuit. The switch, S1, toggles the circuit between compressor and ALC mode. Jumpers J1 and J2 can be used to either include the additional op amps for signal conditioning or exclude them from the signal path. Bread boarding space is provided for R1, R2, C1, C2, R10, R11, C10 and C11 so that the response can be tailored for each individual need. The components as specified are suitable for the complete audio spectrum from 20Hz to 20kHz.

The most common configuration is as a unity gain non-inverting buffer where R1, C1, C2, R10, C10 and C11 are eliminated and R2 and R11 are shorted. Capacitors C3, C5, C8, and C12 are for DC blocking, and R4 and R8 provide termination (for the capacitors). In systems where the inputs and outputs are AC coupled, these capacitors and resistors can be eliminated. Capacitors C4 and C9 are for setting the attack and release time constant.

C6 is for decoupling and stabilizing the voltage reference circuit. The value of C6 should be such that it will offer a very low impedance to the lowest frequencies of interest. Too small a capacitor will allow supply ripple to modulate the audio path. The better filtered the power supply, the smaller this capacitor can be. R5 and R12 provide DC reference voltage to the amplifiers of channel B. R6 and R7 provide a DC feedback path for the summing amp of channel B, while C7 is a short-circuit to ground for signals. C14 and C15 are for power supply decoupling. C14 can also be eliminated if the power supply is well regulated with very low noise and ripple. Figure 8 shows the PC board layout of the applications demo board.

DEMONSTRATED PERFORMANCE

The applications demo board was built and tested for a frequency range of 20Hz to 20kHz with the component values as shown in Figure 4 and V_{CC} = 5V. In the expandor mode, the typical input dynamic range was from –34dB to +12dB where 0dB is equal to 100mV_{RMS}. The typical unity gain level measured at 0dB @ 1kHz input was ±0.5dB and the typical tracking error was ±0.1dB for input range of –30 to +10dB.

In the compressor mode, the typical input dynamic range was from –42dB to ±18dB with a tracking error +0.1dB and the typical unity gain level was ±0.5dB.

In the ALC mode, the typical input dynamic range was from –42dB to +8dB with typical output deviation of ±0.2dB about the nominal output of 0dB. For input greater than +9dB in ALC configuration, the summing amplifier sometimes exhibits high frequency oscillations. There are several solutions to this problem. The first is to lower the values of R7 and R8 to 20kΩ each. The second is to add a current limiting resistor in series with C13 at Pin 13. The third is to add a compensating capacitor of about 22 to 30pF between the input and output of summing amplifier (Pins 12 and 14). With any one of the above recommendations, the typical ALC mode input range increased to +18dB yielding a dynamic range of over 60dB.

EXPANDOR

The typical expandor configuration is shown in Figure 1. The variable gain cell and the rectifier cell are in the signal input path. The V_{REF} is always 1/2 V_{CC} to provide the maximum headroom without clipping. The 0dB ref is 100mV_{RMS}. The input is AC coupled through C5, and the output is AC coupled through C3. If in a system the inputs and outputs are AC coupled, then C3, C5, R3 and R4 can be eliminated, thus requiring only one external component, C4. The variable gain cell and rectifier cell are DC coupled so any offset voltage between Pins 4 and 9 will cause small offset error current in the rectifier cell. This will affect the accuracy of the gain cell. This can be improved by using an extra capacitor from the input to Pin 4 and eliminating the DC connection between Pins 4 and 9.

The expandor gain expression and the attack and release time constant is given by Equation 1 and Equation 2, respectively.

Equation 1.

$$\text{Expandor gain} = \frac{4V_{IN}(avg)}{3.9k \times 100\mu A}$$

where $V_{IN}(avg) = 0.975V_{IN(RMS)}$

Equation 2.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

COMPRESSOR

The typical compressor configuration is shown in Figure 2. In this mode, the rectifier cell and variable gain cell are in the feedback path. R6 and R7 provide the DC feedback to the summing amplifier. The input is AC coupled through C12 and output is AC coupled through C8. In a system with inputs and outputs AC coupled, C8, C12, R8, and R9 could be eliminated and only R5, R6, R7, C7, and C13 would be required. If the external components R5, R6, R7 and C7 are eliminated, then the output of the summing amplifier will motor-boat in absence of signals or at extremely low signals. This is because there is no DC feedback path from the output to input. In the presence of an AC signal this phenomenon is not observed and the circuit will appear to function properly.

The compressor gain expression and the attack and release time constant is given by Equation 3 and Equation 4, respectively.

Equation 3.

$$\text{Compressor gain} = \left[\frac{3.9k \times 100\mu A}{4V_{IN}(avg)}\right]^{1/2}$$

where $V_{IN}(avg) = 0.975V_{IN(RMS)}$

Equation 4.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

AUTOMATIC LEVEL CONTROL

The typical Automatic Level Control circuit configuration is shown in Figure 3. It can be seen that it is quite similar to the compressor schematic except that the input to the rectifier cell is from the input path and not from the feedback path. The input is AC coupled through C12 and C13 and the output is AC coupled through C8. Once again, as in the previous cases, if the system input and output signals are already AC coupled, then C12, C13, C8, R8 and R9 could be eliminated. Concerning the compressor, removing R5, R6, R7 and C7 will cause motor-boating in absence of signals. C_{COMP} is necessary to stabilize the summing amplifier at higher input levels. This circuit provides an input dynamic range greater than 60dB with the output within ±0.5dB typical. The necessary design expressions are given by Equation 5 and Equation 6, respectively.

Equation 5.

$$\text{ALC gain} = \frac{3.9k \times 100\mu A}{4V_{IN}(avg)}$$

Equation 6.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C9$$

Figure 5 shows that the unity gain error remains small over a wide range of supply voltages. The unity gain error is important because it effects the tracking error. So, to achieve the best unity gain error, provide a power supply voltage of 4 to 5V to the NE575.

Figures 6 and 7 show the output level over a range of frequencies and inputs for the compressor and expandor, respectively. These graphs reveal that the compandor has a constant and flat output. This is important because the signal will not be altered.

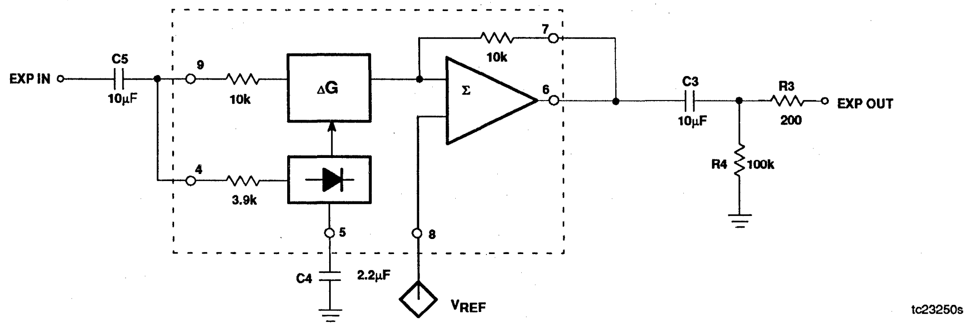


Figure 1. Typical Expandor Configuration

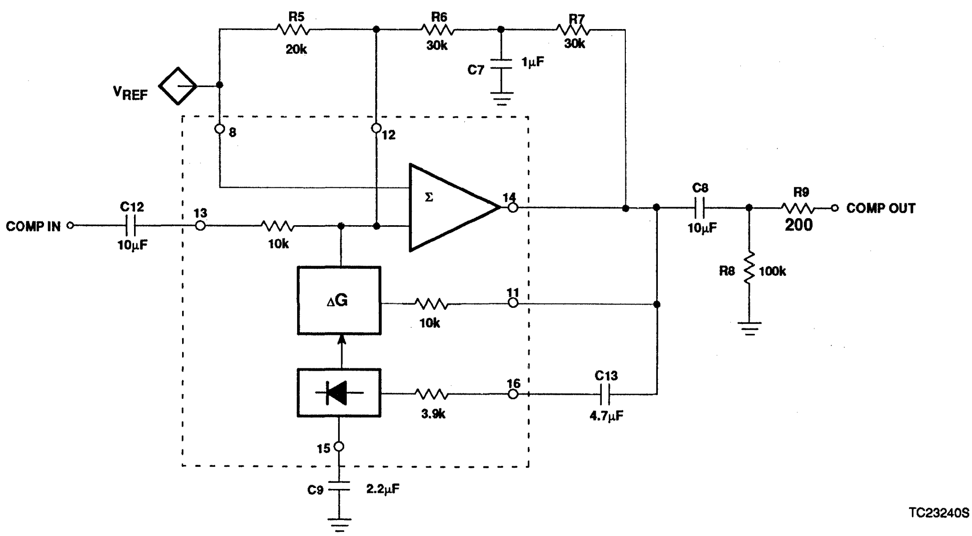


Figure 2. Typical Compressor Configuration

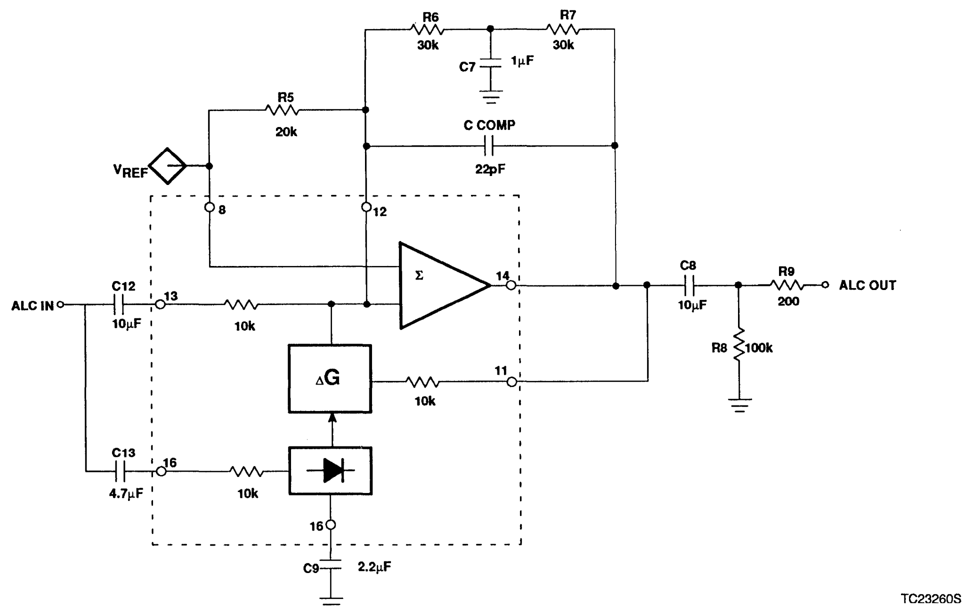


Figure 3. Typical ALC Configuration

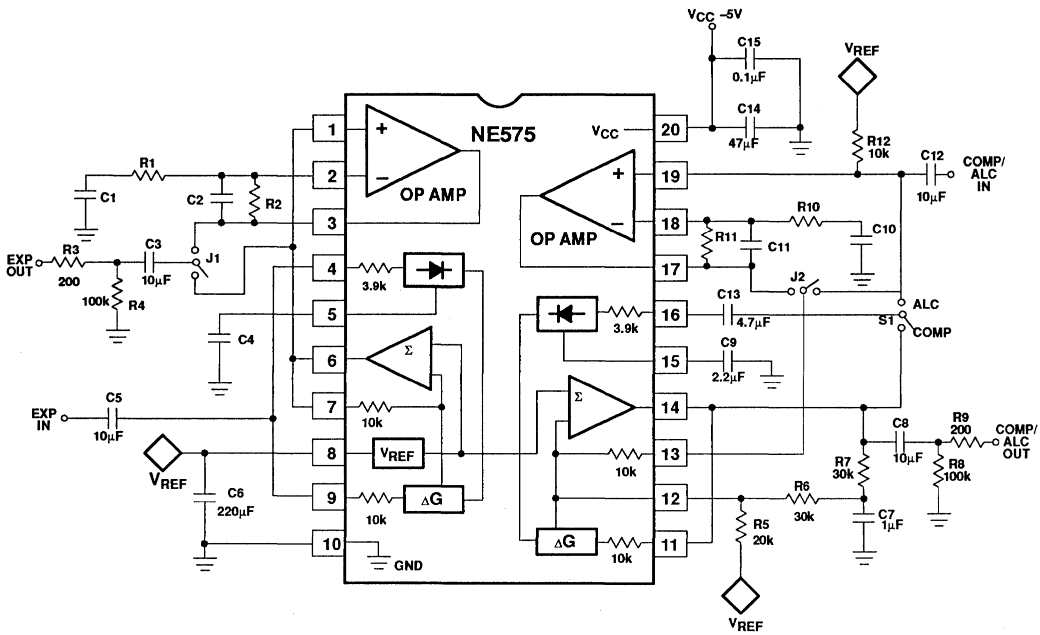


Figure 4. Signetics NE575 Low Voltage Expandor/Compressor/ALC Demo Board

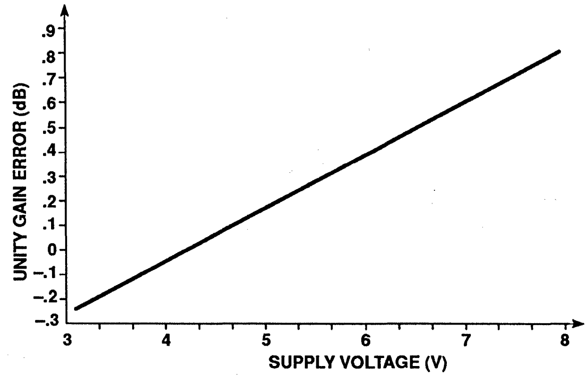


Figure 5. Unity Gain Error vs Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

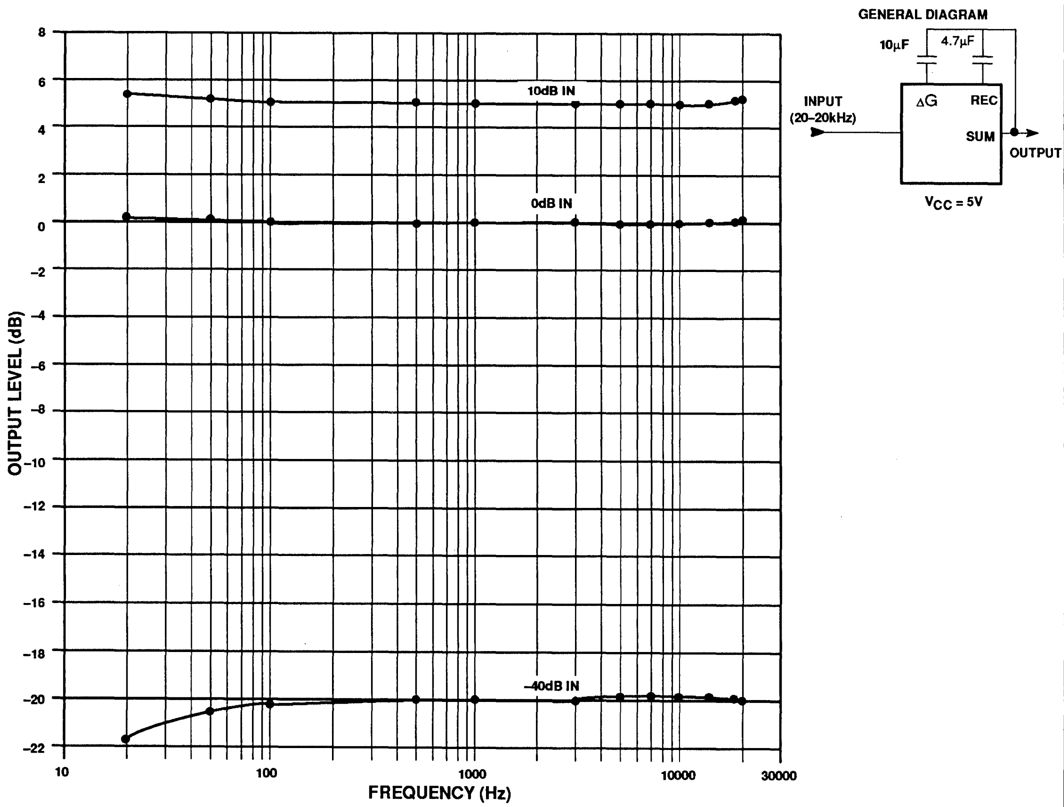


Figure 6. Compressor Output Frequency Response

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

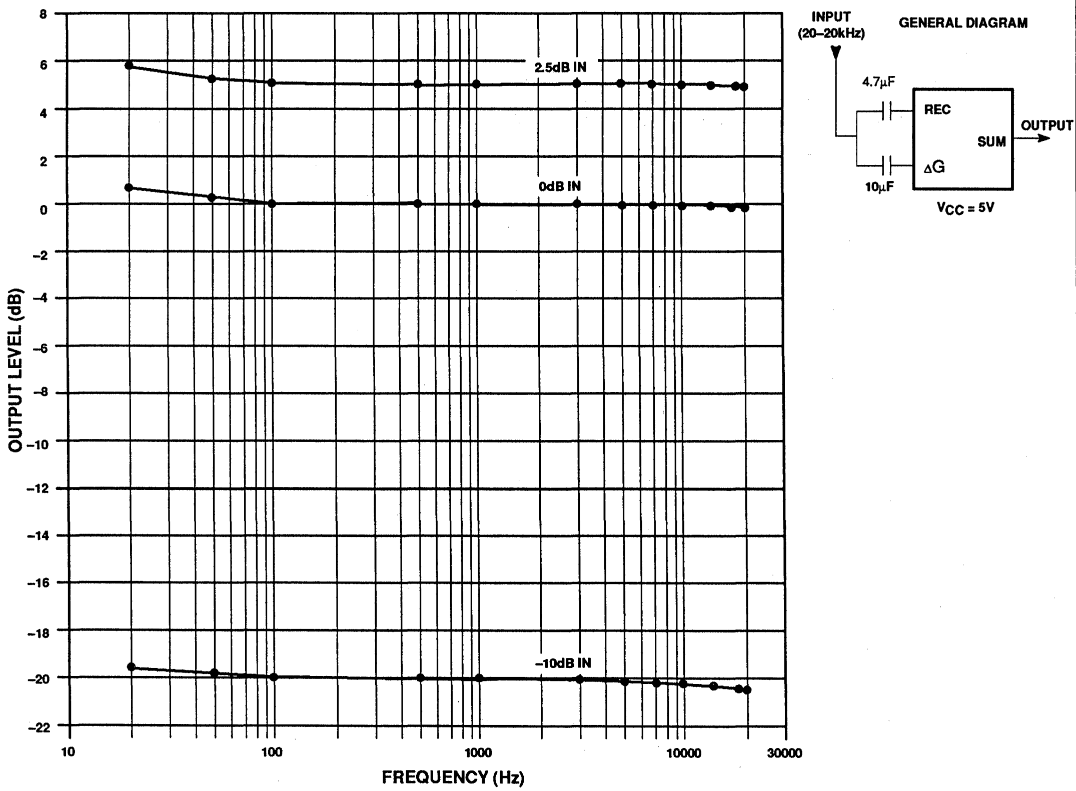


Figure 7. NE575 Expandor Output Frequency Response

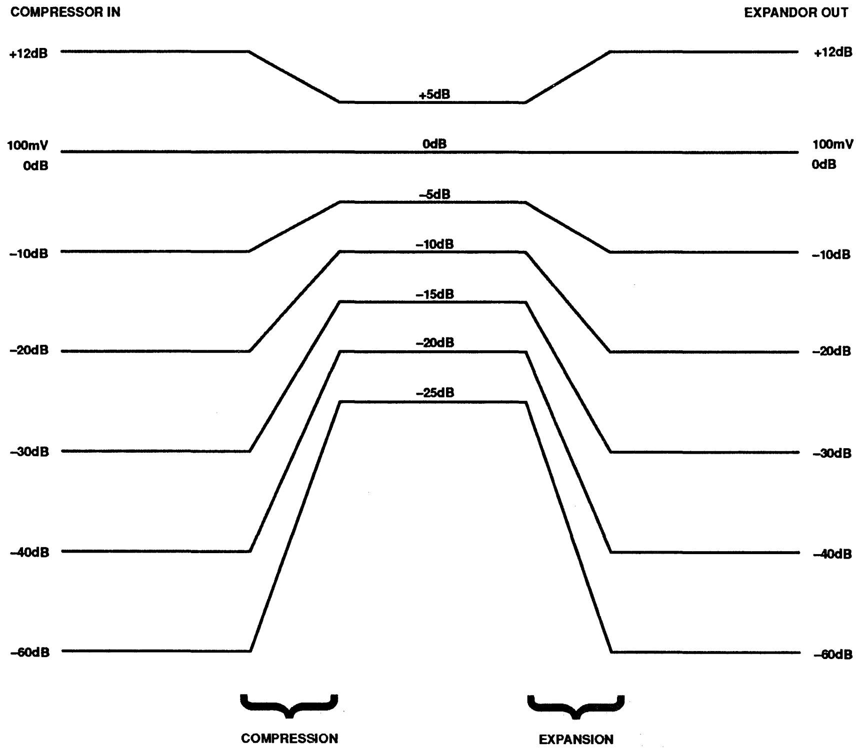


Figure 9. The Companding Function

Low power compandor

NE/SA576

DESCRIPTION

The NE/SA576 is a unity gain level programmable compandor designed for low power applications. The NE576 is internally configured as an expandor and a compressor to minimize external component count.

The NE576 can operate at 1.8V. During normal operations, the NE576 can operate from at least a 2V battery. If the battery voltage drops to 1.8V, this part will still continue to function, however, turning on the part at a V_{CC} of 1.8V requires two external resistors to bring V_{REF} to half V_{CC}. One resistor connects between V_{CC} and V_{REF}; the other connects from V_{REF} to ground. A typical value for these external resistors is approximately 20k. A lower value can be used, but the power consumption will go up.

The NE576 is available in a 14-pin plastic DIP and SO packages.

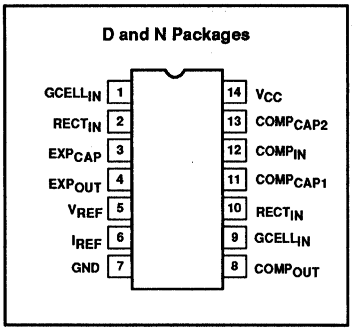
FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- Over 80dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- ESD hardened

APPLICATIONS

- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control

PIN CONFIGURATION



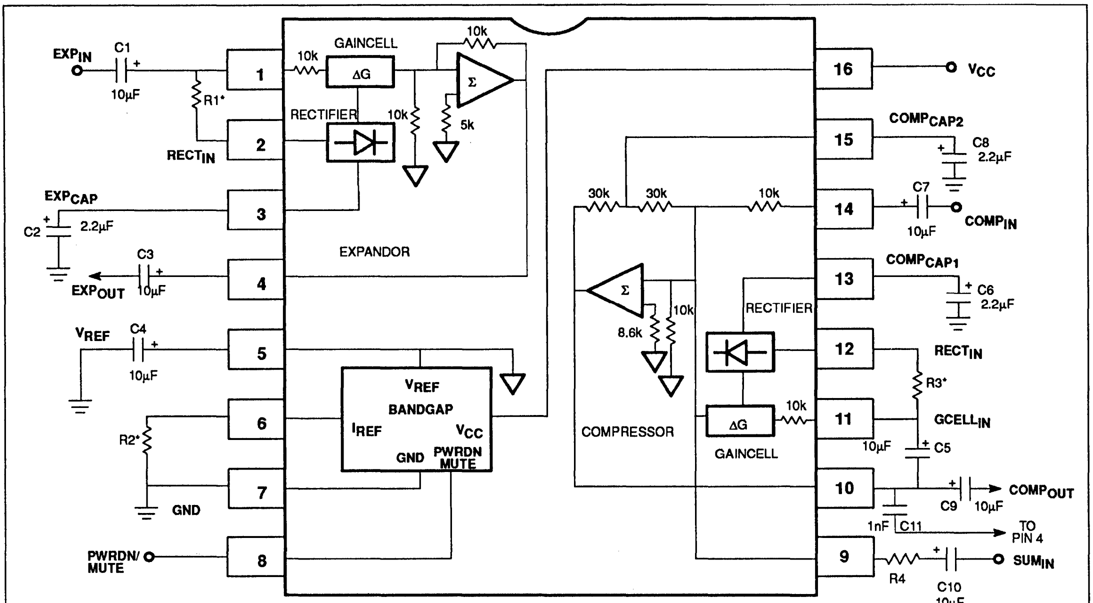
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE576N
14-Pin Plastic SO	0 to +70°C	NE576D
14-Pin Plastic DIP	–40 to +85°C	SA576N
14-Pin Plastic SO	–40 to +85°C	SA576D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE576	SA576	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



*R1, R2 and R3 are 1% resistors.

ELECTRICAL CHARACTERISTICS

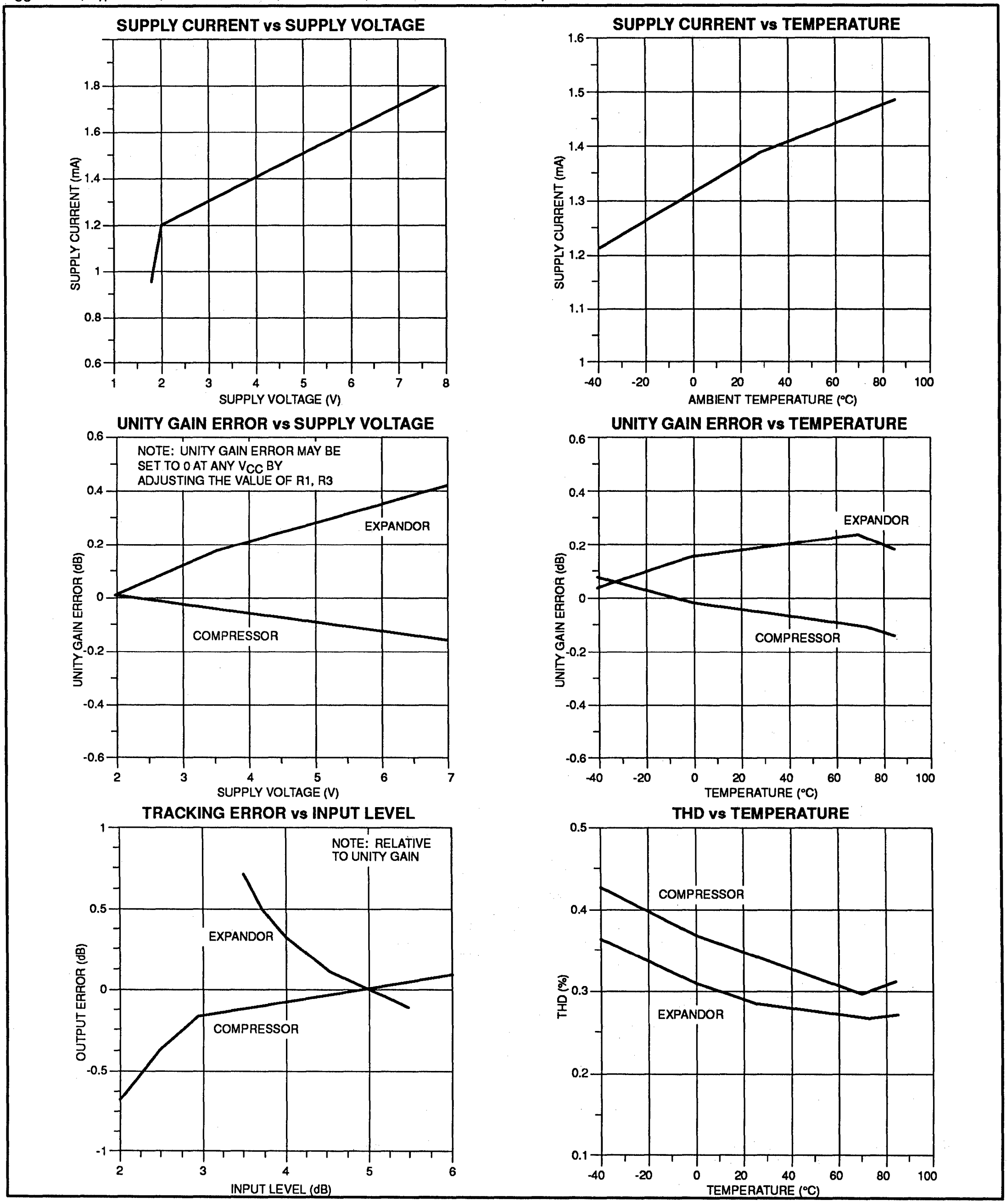
T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA576 MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	3	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V		1.8		V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	30	µV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80		dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		V

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see description on front page of NE576 data sheet.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=18.7kΩ, R2=24.3kΩ, 0dB level = 100mV, Freq. = 1kHz



Unity gain level programmable power compandor — NE/SA577

DESCRIPTION

The NE/SA577 is a unity gain level programmable compandor designed for low power applications. The NE577 is internally configured as an expandor and a compressor to minimize external component count.

The NE577 is available in a 14-pin plastic DIP and SO packages.

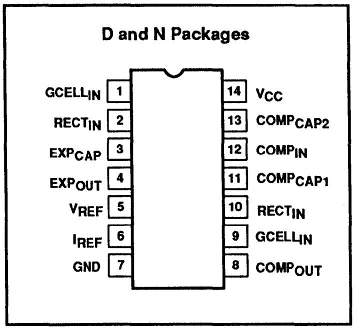
FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable (10mV$_{RMS}$ to 1.0V$_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- SA577 meets cellular radio specifications
- ESD hardened

APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE577N
14-Pin Plastic SO	0 to +70°C	NE577D
14-Pin Plastic DIP	–40 to +85°C	SA577N
14-Pin Plastic SO	–40 to +85°C	SA577D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE577	SA577	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

ELECTRICAL CHARACTERISTICS

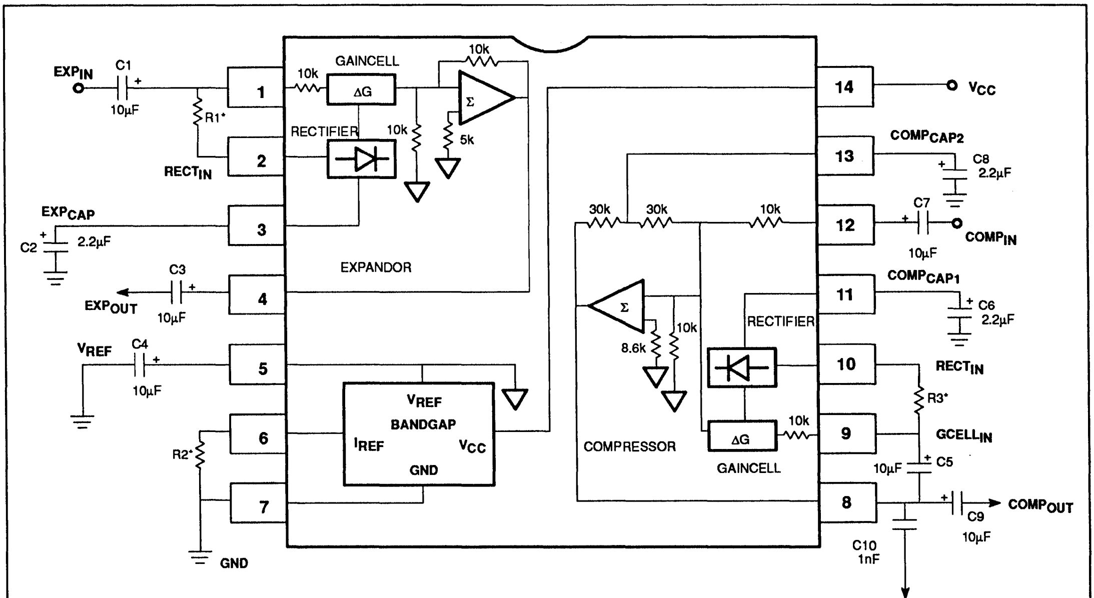
T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA577 MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	2	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V	1.7	1.8	1.9	V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	25	µV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		dBV
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		dBV
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		dBV
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		V

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see application note AN1762.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV_{RMS} and 0dBV = 1.0V_{RMS}. For details see application note AN1762.

Unity gain level programmable power compandor　　NE/SA577

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT

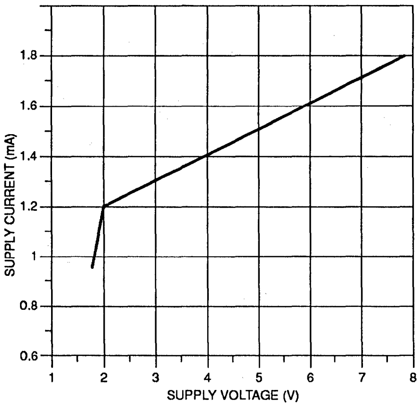


*R1, R2 and R3 are 1% resistors.

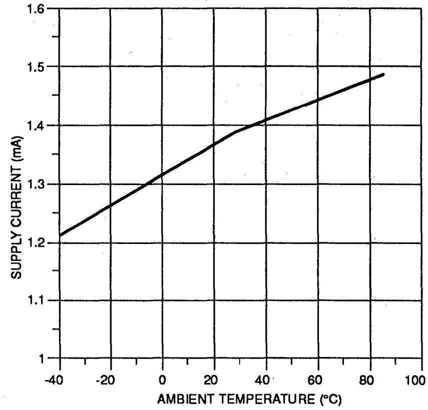
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=18.7kΩ, R2=24.3kΩ, 0dB level = 100mV, Freq. = 1kHz

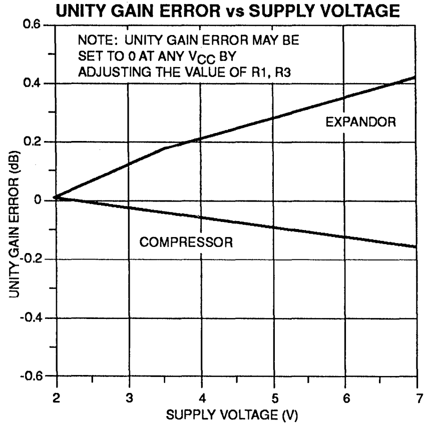
SUPPLY CURRENT vs SUPPLY VOLTAGE



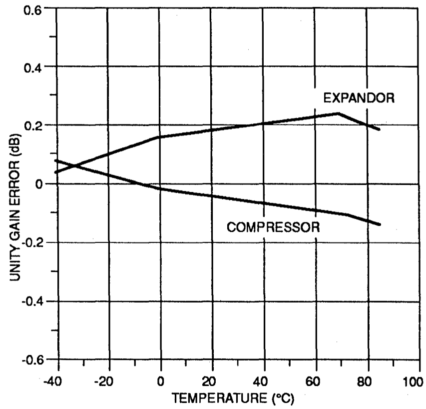
SUPPLY CURRENT vs TEMPERATURE



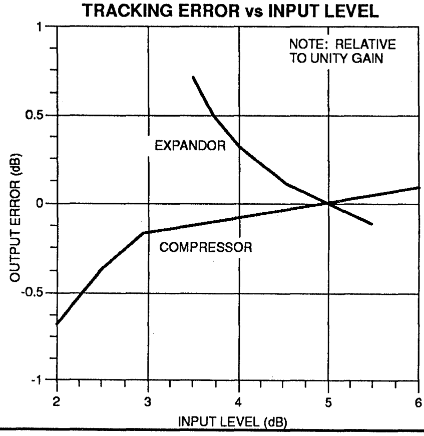
UNITY GAIN ERROR vs SUPPLY VOLTAGE



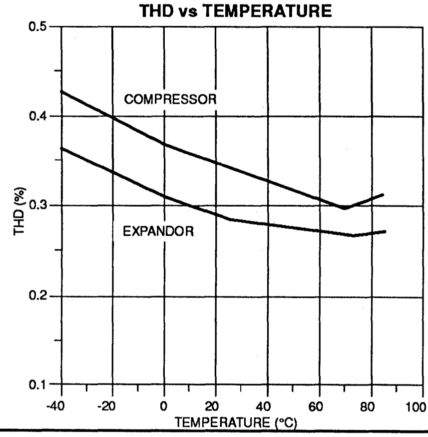
UNITY GAIN ERROR vs TEMPERATURE



TRACKING ERROR vs INPUT LEVEL



THD vs TEMPERATURE



Unity gain level programmable low power compandor

NE/SA578

DESCRIPTION

The NE/SA578 is a unity gain level programmable compandor designed for low power applications. The NE578 is internally configured as an expandor and a compressor to minimize external component count.

The summing amplifiers of the NE578 have 600W drive capability and the inverting input of the compressor amplifier is accessible through Pin 9 for summing multiple external signals. Power Down/Mute function is active low and requires an open collector output logic configuration at Pin 8. If Power Down/ Mute is not needed, Pin 8 should be left open. When the part is muted, supply current drops to 170mA at 3.6V. The NE578 is available in a 16-pin plastic DIP and SO packages.

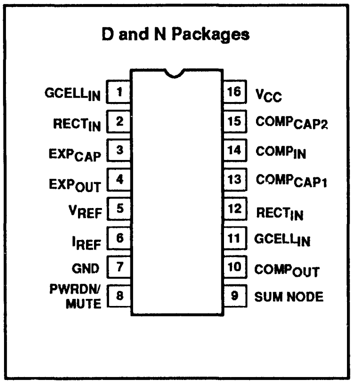
FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable ($10mV_{RMS}$ to $1.0V_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability
- Low external component count
- SA578 meets cellular radio specifications
- ESD hardened
- Power Down mode (I_{CC} = 170mA @ 3.6V)
- Mute function
- Multiple external summing capability
- 600W drive capability

APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

PIN CONFIGURATION



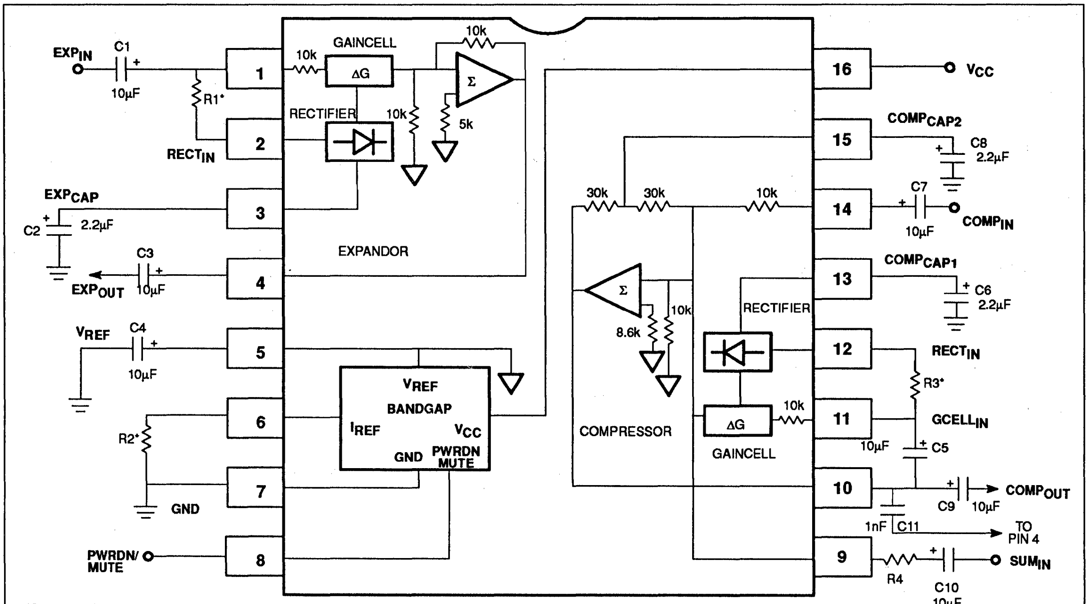
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE578N
16-Pin Plastic SO	0 to +70°C	NE578D
16-Pin Plastic DIP	–40 to +85°C	SA578N
16-Pin Plastic SO	–40 to +85°C	SA578D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE578	SA578	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



*R1, R2 and R3 are 1% resistors.

ELECTRICAL CHARACTERISTICS

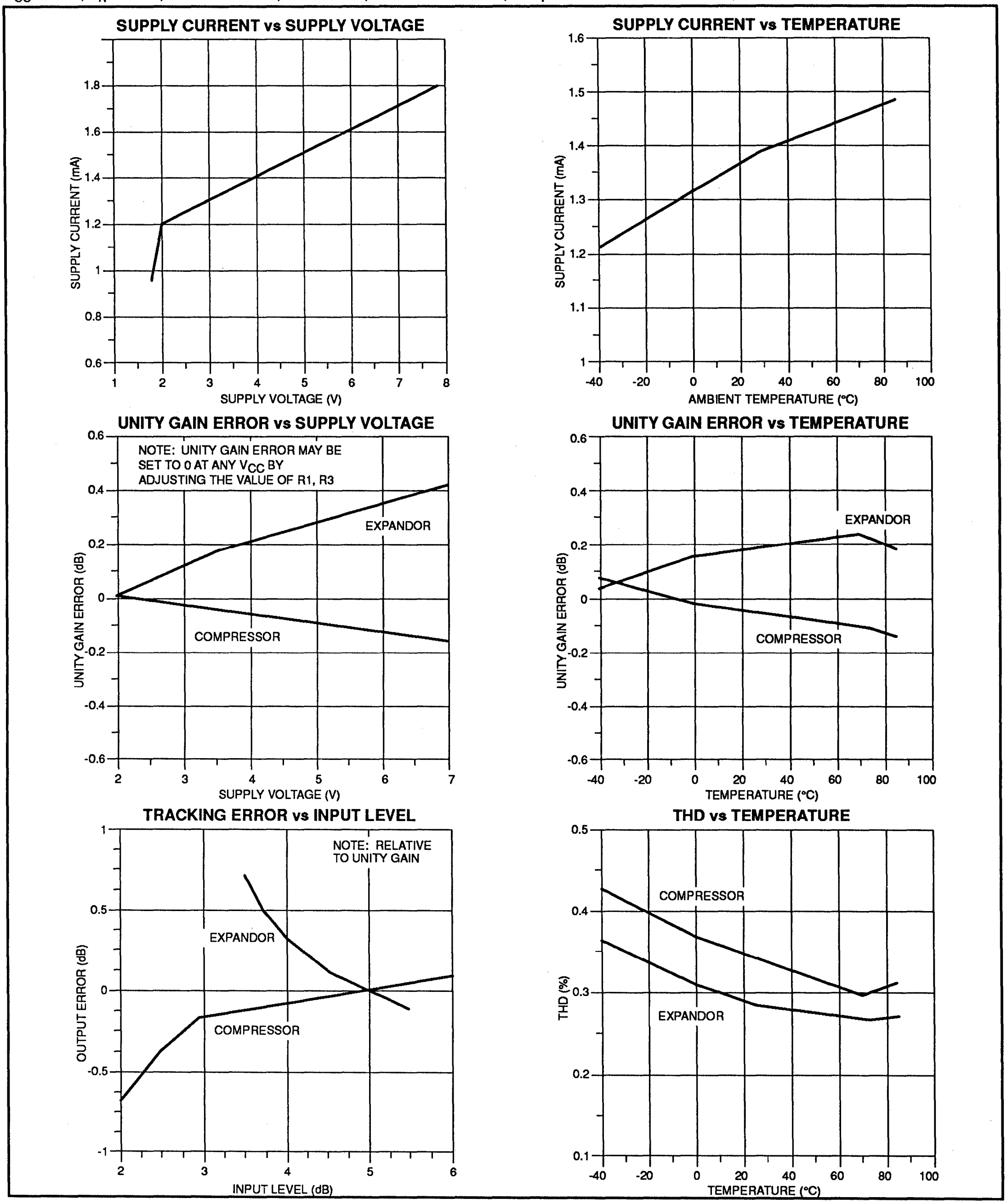
$T_A = 25°C$, $V_{CC} = 3.6VDC$, compandor 0dB level = –20dBV = $100mV_{RMS}$, output load $R_L = 10k\Omega$, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA578 MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current operating power down	No signal, $R_2 = 100k\Omega$		1.4 170	2	mA µA
V_{REF}	Reference voltage[2]	$V_{CC} = 3.6V$	1.7	1.8	1.9	V
R_L	Summing amp minimum output load			600		Ω
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.0	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, $R_S = 0\Omega$		10	20	µV
0dB	Unity gain level	0dB at 1kHz	–1.0	0.18	1.0	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		dBV
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		dBV
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		dBV
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, $C_{REF} = 10\mu F$		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			$V_{CC} - 0.2$		V
	Power Down/Mute low level		0		0.4	V
	Power Down/Mute input current	Pin 8 grounded		–65		µA

NOTE:
1. Operation down to $V_{CC} = 1.8V$ is possible, see application note AN1762.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = $10mV_{RMS}$ and 0dBV = $1.0V_{RMS}$. For details see application note AN1762.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=18.7kΩ, R2=24.3kΩ, 0dB level = 100mV, Freq. = 1kHz



Companding with the NE577 and NE578

AN1762

Author: Alvin K. Wong

INTRODUCTION

This application note is written for the designer who understands the basic functions of companding and wants to use the NE577 or NE578. If a designer is not familiar with the functionality of compandors, a good discussion can be found in the earlier Philips Components-Signetics compandor data sheets and applications notes.

Key topics discussed in this paper are:

- How to program the unity gain level (0dB)
- How to implement an automatic level control
- How to get the best companding performance under strict design requirements
- How to set the attack and recovery time
- How to operate at 1.8V
- How to sum external signals using the NE578
- How to power-down the NE578
- How to mute the NE578
- How to use the NE577 and NE578 as a dual expandor

But before reviewing these areas, a summary of Philips Components-Signetics compandor family will be presented. A system designer can then determine which compandor is best for the design.

SUMMARY OF COMPANDOR FAMILY

In the past, Philips Components-Signetics offered four different types of compandors: the NE570, NE571, NE572, and NE575. Each of the four compandors has its own 'claim to fame'. The NE570 and NE571 are known to work well in high performance audio applications. The only real difference between the two is that the NE570 has a slight edge in performance. However when separate attack and recovery times are needed, the NE572 is the compandor to choose. The NE575 becomes useful when there are low voltage requirements.

With the increasing demand for low current consumption, good flexibility, and ease of use in semiconductors, Philips Components-Signetics is offering three additional compandors to its family, the NE576, NE577 and NE578. These compandors typically require an I_{CC} of 1.4mA at a V_{CC} of 3.6V, but Philips Components-Signetics has demonstrated that these new chips are functional down to 1.8V.

In addition to having low power consumption, the NE578 has a power-down mode. In this mode, the chip consumes only 170µA. This power-down mode is useful when the functionality of the chip is not needed at all times. In the power-down mode , the NE578 maintains all of its pin voltages at all their normal DC operating voltages. Because all of the capacitors remain charged in this mode, the power-up state will occur quickly. Powering down automatically mutes the NE578. Having the mute function internal to the NE578 audio section eliminates the need for an external switch. The NE578 is the only compandor in the family that has power-down and mute functions.

To allow for greater flexibility, the 0dB level is now programmable for the NE577 and NE578. However, for the NE576, the 0dB level is specified and set at $100mV_{RMS}$. The earlier compandors also have a set unity gain (0dB) level. The NE570 and NE571 have a set 0dB level at $775mV_{RMS}$. While the NE572 and the NE575 both have their 0dB levels at $100mV_{RMS}$. If a designer wanted a different 0dB level, two op amps would have to be implemented in the design. One of the op amps would connect to the input of the compandor, while the other op amp would connect to the output. But with the NE577 and NE578, these external op amps are no longer needed. The 0dB level can be programmed from $10mV_{RMS}$ to $1V_{RMS}$ with three external resistors.

Many of the external parts in the previous family of compandors are now internal to the device. Additionally, the left side of the chip is configured as an expandor, and the right side is configured as a compressor. This allows for minimum part count and fewer variations in systems design. The external capacitors are also reduced in value which saves board space and cost. The only trade-off with using smaller capacitors is that there is less filtering. Because of this new approach, the NE576, NE577 and NE578 are easy to implement in any design.

Table 1 shows a brief summary of all the compandors. The seven different compandors offer a wide range of flexibility: different types of packages, power-down capability, programmable or fixed unity gain, different reference voltages, a wide range of operating voltages and currents, different pin outs, etc. From this information, a designer can quickly choose a compandor which best meets the design requirements. After a compandor is chosen from the table, a designer can find additional help from data sheets and application notes.

Since power consumption is important in most designs, it is important to discuss them in this application note. The NE570, NE571, and NE572 have built in voltage regulators, therefore, the current consumption remains roughly the same over the specified supply voltages. This can be especially useful when the power supply is not regulated very well. However with the NE575, NE576, NE577, and NE578, the current consumption will drop as the supply voltage decreases. For this, the power consumption will drop also. This means one can operate the part at a very low power level. This is a good feature for any design having strict power consumption guidelines.

INTRODUCING NE577 AND NE578

Figure 1 and 2 show block diagrams of the NE577 and NE578 respectively. The only substantial difference between the two is that the NE578 has a power-down capability, mute function and summing capabilities (for signals like DTMF tones). In addition the NE578 summing amplifiers are capable of driving 600Ω loads. Listed below are the basic functions of each external component for Figure 1 (NE577).

Table 1. Compandor Family Overview

	NE570	NE571	NE572	NE575	NE576	NE577	NE578
V_{CC}	6–24V	6–18V	6–22V	3–7V	2–7V	2–7V	2–7V
I_{CC}	3.2mA	3.2mA	6mA	3–5.5mA*	1–3mA*	1–2mA*	1–2mA*
Number of Pins	16	16	16	20	14	14	16
Packages NE: 0 to +70°C SA: –40 to +85°C N: Plastic DIP D: Plastic SO F: Ceramic DIP DJ: SSOP (Shrink Small Outline Package)	NE570F NE570N NE570D	NE571F NE571N NE571D SA571F SA571N SA571D	NE572N NE572D SA572F SA572N SA572D	NE575N NE575D NE575DJ SA575N SA575D SA575DJ	NE576N NE576D SA576N SA576D	NE577N NE577D SA577N SA577D	NE578N NE578D SA578N SA578D
ALC (Automatic Level Control)	Both Channels	Both Channels	Both Channels	Right Channel	Right Channel	Right Channel	Right Channel
Reference Voltage	Fixed 1.8V	Fixed 1.8V	Fixed 2.5V	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2
Unity Gain	775mV$_{RMS}$	775mV$_{RMS}$	100mV$_{RMS}$	100mV$_{RMS}$	100mV$_{RMS}$	10mV to 1V$_{RMS}$	10mV to 1V$_{RMS}$
Power-Down	NO	NO	NO	NO	NO	NO	YES (170μA)
Key Features	-Excellent Unity Gain Tracking Error -Excellent THD	-Excellent Unity Gain Tracking Error -Excellent THD	-Independent Attack & Recovery Time -Good THD -Needs ext. summing op amp	-2 Uncommited on-chip op amps available -Low voltage	-Low power -Low external component count	-Low power -Programmable unity gain	-Low power -Programmable unity gain -Power down -Mute function -Summing capability (DTMF) -600Ω drive capability
Applications Cordless Phones Cellular Phones Wireless Mics Modems Consumer Audio Two-way Communications	High performance audio circuits "Hi–Fi Commercial Quality"	High performance audio circuits "Hi–Fi Commercial Quality"	High performance audio circuits "Hi–Fi Studio Quality"	Consumer audio circuits "Commercial Quality"	Battery powered systems "Commercial Quality"	Battery powered systems "Commercial Quality"	Battery powered systems "Commercial Quality"

NOTES: NE5750/5751 are also excellent audio processor components for high performance cordless and cellular applications that include the companding function..
*I_{CC} varies with V_{CC}.

R1 – Determines the Unity Gain Level for the Expandor

R2 – Determines What Value the Reference Current (I_{REF}) will be for the Part (Also Affects Unity Gain Level)

R3 – Determines the Unity Gain Level for the Compressor

C1 – DC Blocking Capacitor

C2 – Determines the Attack and Recovery Time for the Expandor

C3 – DC Blocking Capacitor

C4 – Used to AC Ground the V_{REF} Pin

C5 – Provides AC Path from Gain Cell to Output of Summing Amp

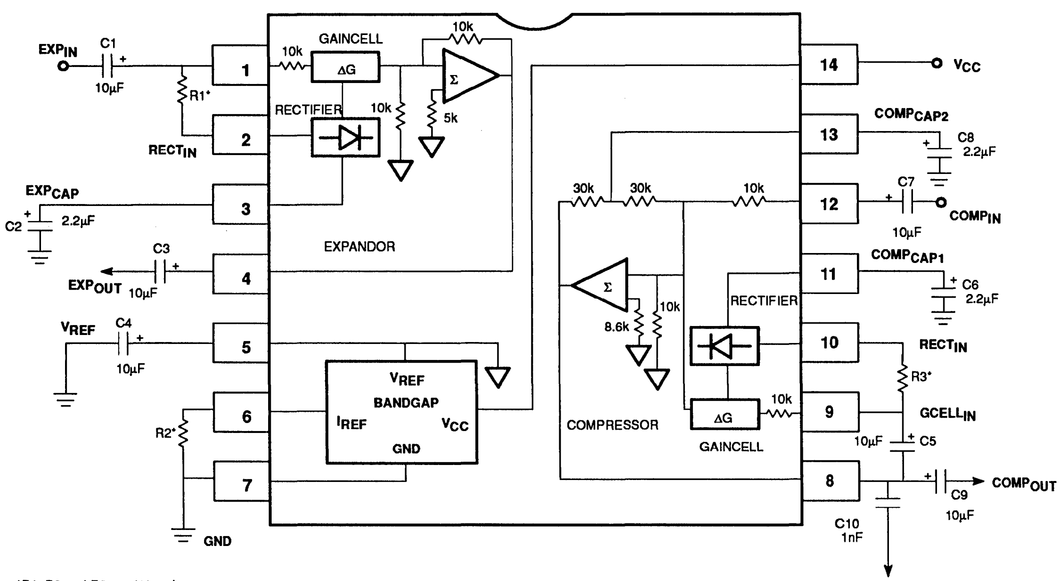
C7 – DC Blocking Capacitor

C8 – Provides AC Ground for the DC Feedback Path

C9 – DC Blocking Capacitor

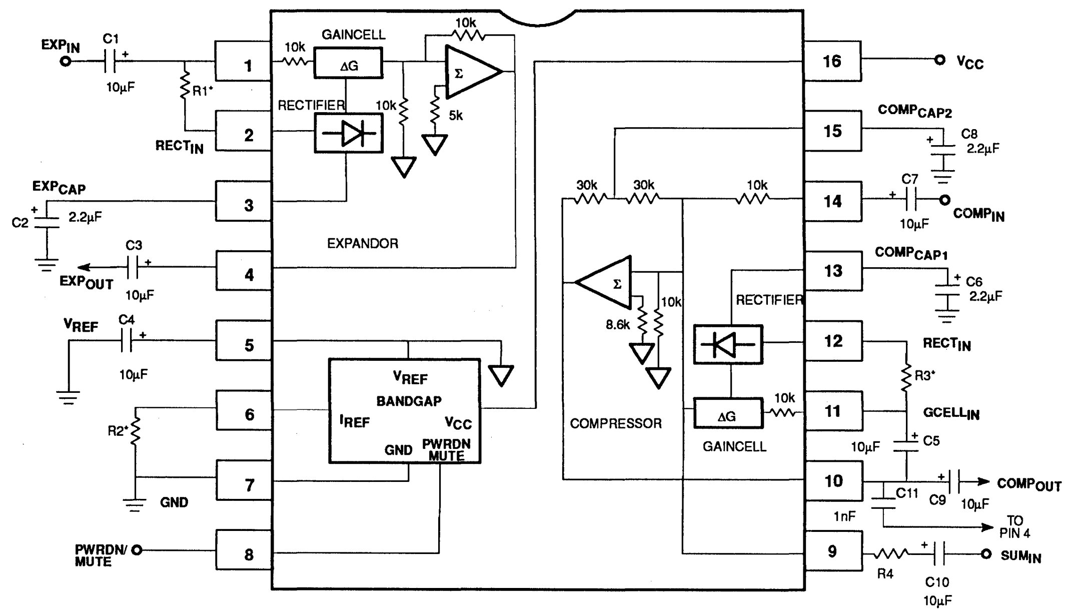
*C10 – Increases the Dynamic Range and limits the Frequency Response to less than 500kHz

Companding with the NE577 and NE578 AN1762



*R1, R2 and R3 are 1% resistors.

Figure 1. NE577 Block Diagram



*R1, R2 and R3 are 1% resistors.

Figure 2. NE578 Block Diagram

Listed below are the basic functions of each external component for Figure 2 (NE578).

R1 – Determines the Unity Gain Level for the Expandor

R2 – Determines What Value the Reference Current (I_{REF}) will be for the Part (Also Affects Unity Gain Level)

R3 – Determines the Unity Gain Level for the Compressor

R4 – Used to Set the Gain of an External Signal like DTMF Tones and Sum them with the Companded Signal

C1 – DC Blocking Capacitor

C2 – Determines the Attack and Recovery Time for the Expandor

C3 – DC Blocking Capacitor

C4 – Used to AC Ground the V_{REF} Pin

C5 – Provides AC Path from Gain Cell to Output of Summing Amp

C6 – Determines the Attack and Recovery Time for the Compressor

C7 – DC Blocking Capacitor

C8 – Provides AC Ground for the DC Feedback Path

C9 – DC Blocking Capacitor

C10 – DC Blocking Capacitor

*C11 – Increases the Dynamic Range and limits the Frequency Response to less than 500kHz

*Note: Bandwidth limiting is done to increase high frequency noise immunity and to make the performance of the part independent of layout or load capacitance.

HOW TO PROGRAM THE UNITY GAIN LEVEL (0dB)

Three external resistors R1, R2, and R3 define the unity gain level. Both the NE577 and the NE578 0dB levels can vary from $10mV_{RMS}$ to $1.0V_{RMS}$. These limits are used in product characterization, but these parts can function over a wider 0dB level range.

In most applications the 0dB level is equal for both the compressor and expandor side. Therefore, R1 and R3 are equal in value. R3 sets the 0dB level for the compressor side, and R1 sets the 0dB level for the expandor side. However, there could be a situation where a design requires different 0dB levels for compression and expansion. This will not be a problem with the NE577 or NE578, due to the separate 0dB level programming.

Using the formulas below, a designer can calculate the resistor values for a desired unity gain level.

Formula 1: $$R_2 = \frac{V_{BG}}{I_{REF}}$$

where V_{BG} = Bandgap Voltage
I_{REF} = Reference Current
(V_{BG} is brought out on Pin 6 and R2 determines the I_{REF} value)

Formula 2: $$R_1 = \frac{0.9 \cdot V_{IN_{RMS}}}{I_{REF}}$$

where $V_{IN_{RMS}}$ *is the 0dB level*
($R_1 = R_3$ in most cases)

Programming the Unity Gain Level for the NE577 also applies for the NE578.

Example:

Program the NE577 or NE578 for a 0dB Level at $100mV_{RMS}$

Step 1: V_{BG}=1.26V.......Typically
I_{REF}=12.6µA.....Good Starting Point

$$R_2 = \frac{1.26V}{12.6}\mu A$$

R_2 = 100k

Step 2:

$$R_1 = R_3 = \frac{0.9V_{IN_{RMS}}}{I_{REF}}$$

$$R_1 = R_3 = \frac{(0.9V)\ (100mV_{RMS})}{12.6\mu A}$$

$\therefore R_1 = R_3 = 7.15k$

Step 3: $R_1 = R_3$ = 7.15k (1% value)
R_2 = 100k (1% value)

Step 4: Plug in these resistor values and measure for unity gain. Adjust accordingly for accuracy.

NOTE: Rough Limits for Resistors:
$1k \leq R1 \leq 100k$ (1% values)
$20k \leq R2 \leq 200k$ (1% values)
$1k \leq R3 \leq 100k$ (1% values)

Rough Limits for I_{REF}
$6.3\mu A \leq I_{REF} \leq 63\mu A$

The example above gives pretty close results. A designer should use 1% resistors to get the best performance. Below in Table 2 are some recommended values to get started:

Table 2. Recommended Resistor Values for Different 0dB Levels

0dB Level	dBv	R_2	R_1 & R_3
$1.0V_{RMS}$	0	24.3k	18.7k
$316.2mV_{RMS}$	–10	100k	22.6k
$100mV_{RMS}$	–20	100k	7.15k
$10mV_{RMS}$	–40	200k	1.33k

PARAMETERS THAT LIMIT THE DYNAMIC RANGE

The above example is a good place to start, but to get the optimum performance from the NE577 and NE578, a designer needs to understand certain key parameters. I_{REF} is important because it determines the values for all three resistors (R1, R2, and R3). Since I_{REF} is directly related to I_{CC} (see Figure 3), one should be careful in choosing a value. If one chooses a high I_{REF} current, power consumption goes up. However the output signal will have excellent low level distortion (see Figures 4 and 5). If one chooses a low I_{REF} value, distortion at the output will increase slightly. Conversely, the power consumption is reduced, which might be worth the trade-off in battery operated designs.

The dynamic range of the NE577 and NE578 is determined by supply voltage (V_{CC}) and reference current (I_{REF}). I_{REF} determines how well the compandor will perform with low level input signals. The supply voltage determines how high (in level) an input signal can be before clipping appears on the output (in some cases increasing I_{REF} also helps). A designer needs to estimate the input range going into the compandor so that an appropriate V_{CC} and I_{REF} can be chosen.

The bandgap voltage (V_{BG}) slightly varies over a wide range of I_{REF} currents (Figure 6). Figure 7 shows how I_{REF} varies with R2. The higher R2 is, the lower I_{REF} is. Figure 8 shows how the dynamic range varies over different values of I_{REF} (the higher the supply voltage the better the dynamic range). The graphs in Figures 3 - 8 were taken at V_{CC}=3.6V, F=1kHz and 0dB level=$100mV_{RMS}$. The I_{REF} current was limited between 5µA and 40µA.

It can be seen that I_{REF} plays an important role in current consumption, THD, and dynamic range. With the aid of these figures, one can determine an I_{REF} which meets the design goals.

Example:

Making use of the graphs in Figures 3 - 8 and formulas 1 and 2, design a compandor with a 0dB level of $100mV_{RMS}$. Try to achieve a THD of 0.1 on the compressor side with wide dynamic range. Operate at a supply voltage of 3.6V but with the lowest possible current consumption.

Step 1: According to Figure 5, an I_{REF} of 30µA is required for approximately 0.1% distortion.

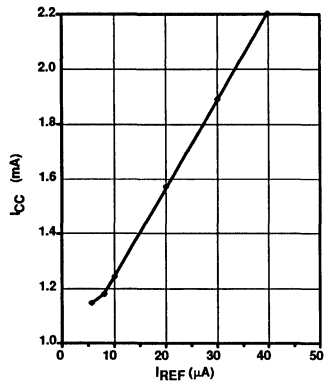


Figure 3. I_{REF} vs I_{CC}

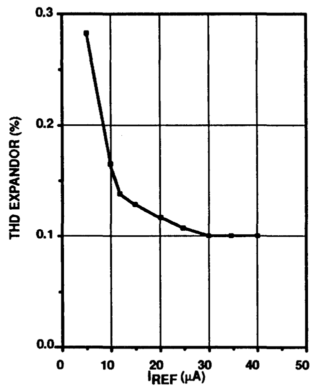


Figure 4. I_{REF} vs THD, Expandor Side

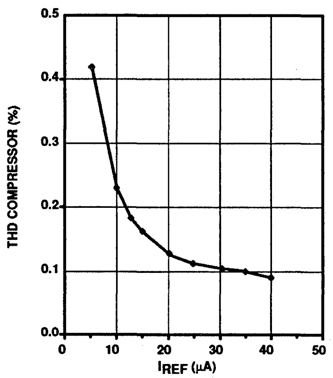


Figure 5. I_{REF} vs THD, Compressor Side

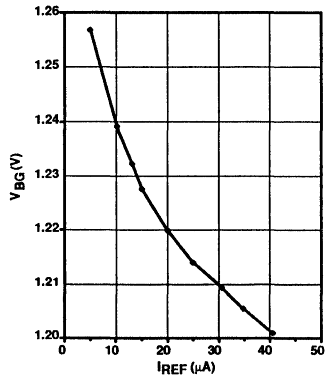


Figure 6. I_{REF} vs V_{BG}

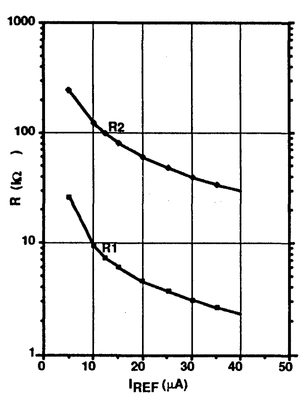


Figure 7. I_{REF} vs R2, R1

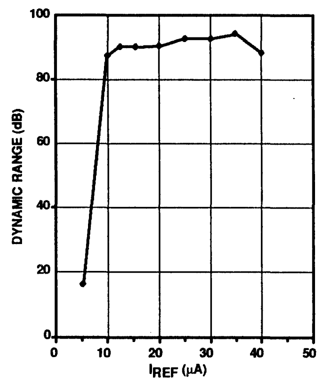


Figure 8. I_{REF} vs Dynamic Range

Test Conditions: V_{CC} = 3.6V F = 1kHz 0dB = $100mV_{RMS}$

Step 2: From Figure 8, the dynamic range is approximately 92dB. So far the requirements have been met.

Step 3: Figure 3 shows us that I_{CC} is at 1.9mA with no input signal (that's not bad at all!).

Step 4: Calculating R1, R2, and R3

Graphical Method:

From Figure 7: For I_{REF}=30µA and 0dB=$100mV_{RMS}$ R1=R3=3k R2=40k

Actual resistors available: R1=R3=3.01k (1%) R2=40.2k (1%)

Formula Method:

From Figure 6: V_{BG}=1.21V for I_{REF}=30µA therefore, using formula 1:

$$R_2 = \frac{V_{BG}}{I_{REF}}$$

$$R_2 = \frac{1.21V}{30\mu A}$$

R_2 = 40.33k

R_2 = 40.2k (available in 1%)

Recall from formula 2:

$$R_1 = \frac{0.9V_{IN_{RMS}}}{I_{REF}}$$

$$R_1 = \frac{(0.9V)\ (100mV_{RMS})}{30\mu A}$$

R_1 = 3k

R_1 = 3.01k (available in 1%)

Connect these external resistors with the determined values and adjust for optimum performance.

Bench results:

After completing the exercise above, the resistors were connected and the results are given below.

I_{CC} = 1.89mA (with no input signal)
THD = 0.1 (meausured on spectrum analyzer)
0dB = $109mV_{RMS}$ (off by 0.8dB...good!)
Dynamic Range = 92dB

These results are very close to what was predicted and by tweaking R1 and R3, the 0dB error can be further reduced to zero.

BANDWIDTH OF COMPANDOR

Figure 9 shows the typical bandwidth for the NE577 and NE578. The graphs were taken with a V_{CC} of 3.6V and a 0dB level of $100mV_{RMS}$. The bandwidth of the expandor, the compressor, and the compandor (where a signal goes through the compressor and the expandor) is shown in this figure. Although the NE577 and NE578 are conservatively specified with a 20kHz bandwidth, Figure 9 reveals that it is actually around 300kHz.

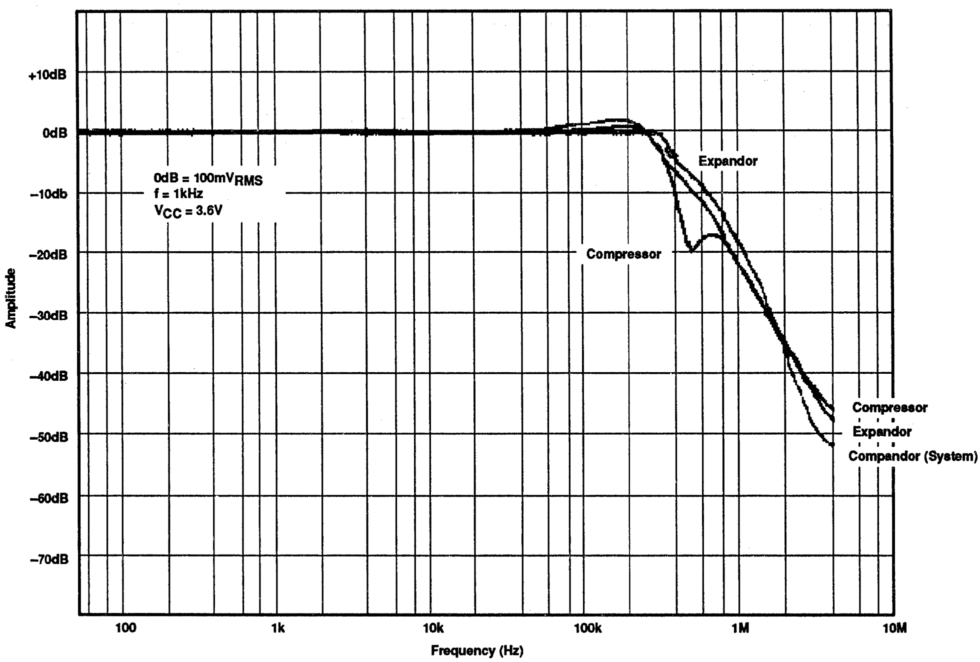


Figure 9. Bandwidth of NE577 and NE578 Demo Board

HOW TO SET THE ATTACK AND RECOVERY TIMES

C2 and C6, from figures 1 and 2, set the attack and recovery times for the NE577 and NE578. Application Note 174 (AN174) defines A and R times and also describes how they are measured on the bench. Formula 3 shows how the A and R time can be calculated.

Formula 3:

Attack Time [ms] = 10k * C2 or C6
Release Time [ms] = 4 * Attack Time

Although a fast attack time is desirable, one must remember that there is a trade-off with low distortion. As a general rule, a 1μF capacitor for C2 will produce 0.2% THD at 1kHz. Since CCITT recommends an RC time constant of 20ms for the attack time, a 2μF capacitor is recommended for telephony applications because it has only 0.1% THD at 1kHz and 0.33% at 800Hz.

Note: AN174 can be found in the 1989 Linear Data Manual, Volume 1, or the RF Handbook.

IMPLEMENTING A PROGRAMMABLE AUTOMATIC LEVEL CONTROL

The function of an automatic level control (ALC) is to take a given range of input signals and provide a constant AC output level. This type of function is useful in many audio applications. One such application can be found in tape recorders. When a tape recorder with ALC is recording a conversation, a soft spoken person will be heard just as well as a loud spoken person during play back. Another useful application for ALC could be with telephony. A person who has difficulty hearing, will not have to ask the other party to speak up. If the phone already has a volume control, the user has to adjust the volume for different parties. But with the ALC, the volume only has to be set once.

Different constant AC output levels of an ALC can be 'programmed' with the NE577 and NE578. This allows the designer to choose the output level that is needed in the design, and eliminates the need for an external op amp.

The compressor side of the NE577 and NE578 can be configured to function as an automatic level control (ALC). Figure 10 and 11 show how this can be done. The circuit shown for the NE577/78 ALC is set up to provide a constant output level of $100mV_{RMS}$ with an input range from –34dB to +20dB at 1kHz (see Figure 12).

Below are some design equations for the ALC:

Eq 1.

$$AC\ output\ level(V_{RMS}) = \left[\frac{R_3 \cdot R_{2_a} \cdot I_{REF}}{R_{1_a}}\right] \cdot 1.11$$

$$where\ R_{1_a} = R_{2_a} = 10k\ (internal)$$

$$I_{REF} = \frac{V_{BG}}{R_2}$$

Eq 2.

$$Maximum\ Gain = \frac{4(R_3 + R_X) \cdot R_{2_a} \cdot I_{REF}}{R_{1_a} \cdot V_{CC}}$$

Eq 3.

$$Gain = \frac{R_3 \cdot R_{2_a} \cdot I_{REF}}{R_{1_a} \cdot V_{IN_{RMS}}}$$

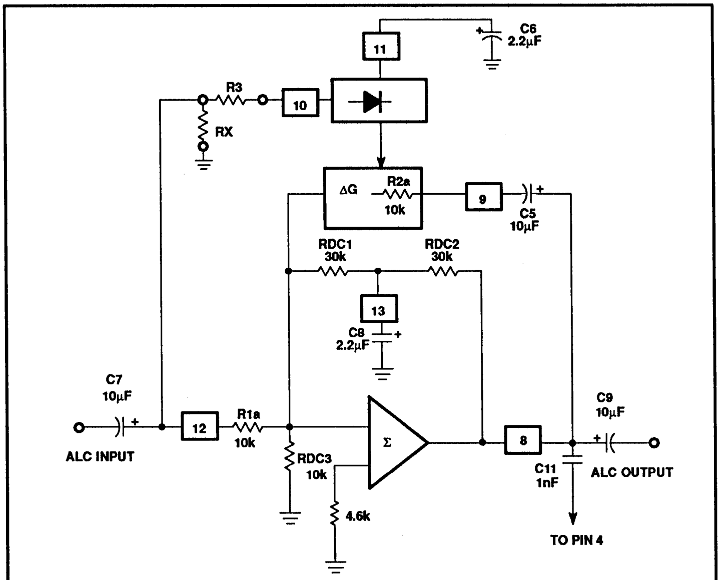


Figure 10. NE577 ALC Configuration

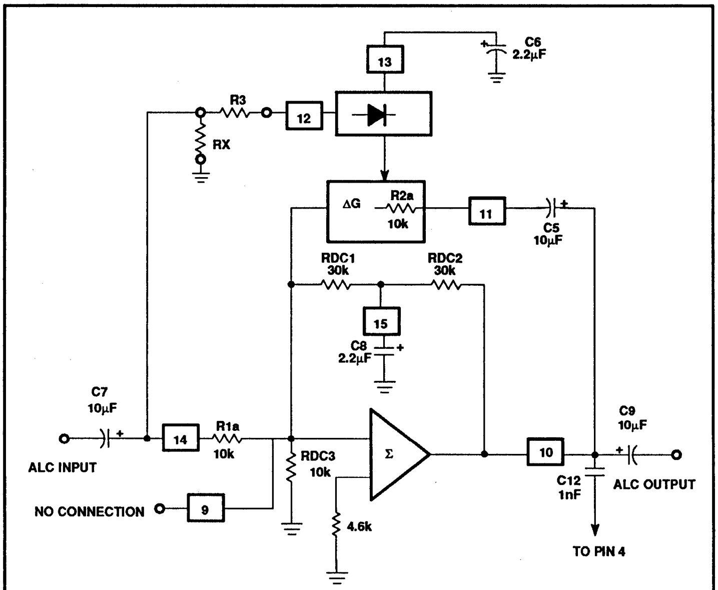


Figure 11. NE578 ALC Configuration

Example:
Design an ALC with a constant output level of $100mV_{RMS}$ with a maximum gain of 10.

Step 1: From Eq 1

$$AC\ output\ level(V_{RMS}) = \left[\frac{R_3 \cdot R_{2_a} \cdot I_{REF}}{R_{1_a}}\right] \cdot 1.11$$

$$where\ R_{1_a} = R_{2_a} = 10k\ (internal)$$

$$I_{REF} = \frac{V_{BG}}{R_2}$$

In terms of R_3

$$R_3 = \frac{\left[AC\ output\ level(V_{RMS})\right] R_{1_a}}{(1.11)\ (R_{2_a})\ I_{REF}}$$

assuming $R_2 = 100k$ and $V_{BG} = 1.26V$.

$$R_3 = \frac{100mV_{RMS} \cdot 10k}{1.11 \cdot 10k \cdot 12.6\mu A}$$

$$R_3 = 7.15k$$

Step 2: From Eq 2

$$Maximum\ Gain = \frac{4(R_3 + R_X) \cdot R_{2_a} \cdot I_{REF}}{R_{1_a} \cdot V_{CC}}$$

In terms of R_X

$$R_X = \frac{(Max.\ Gain)\ (V_{CC})\ (R_{1_a})}{4R_{2_a} \cdot I_{REF}} - R_3$$

$$R_X = \frac{(10)\ (3.6V)\ (10k)}{4\ (10k)\ 12.6\mu A} - 7.15k$$

$$R_X = 707.1k$$

$$R_X = 715k\ (available)$$

Step 3:

–connect resistors to circuit
–measure AC output level and adjust R3 for best accuracy
–check maximum gain by applying a low input level and adjust Rx for best results

Figure 12 shows the characteristics of the NE577/578 ALC circuit without Rx. The output stays at a constant $100mV_{RMS}$ level for a wide range of different input AC voltages. Any AC input signal above the cross-over point (unity gain level) is attenuated while any signal below the cross-over point is amplified. The cross-over point is where the input signal is equal to the output signal, where A_V=1.

Figure 13 reveals the dynamic range of the NE577 ALC circuit using Rx. The input range of the ALC is reduced. Instead of a $2mV_{RMS}$ input signal to get $100mV_{RMS}$ on the output, a $10mV_{RMS}$ input signal is now required (for Rx=681k). The purpose of limiting the maximum gain of the circuit is to prevent amplification of background noise. To alleviate this problem, Rx is used. Since the ALC was designed with a maximum gain of

10, any input signal below 10mV will not be amplified with a gain greater than 10 ($100mv_{RMS}/10=10mv_{RMS}$). Using Rx can be an advantage because the threshold of the ALC can be set.

Figure 14 shows that as Rx increases so does A_V. In some applications it might be useful to make Rx a potentiometer. This will allow the user to adjust the threshold for different environmental conditions.

Figures 15-18 show the results of using the ALC for different constant output levels. V_{CC} and I_{REF} limit the dynamic range. The upper part of the range can be increased by either increasing V_{CC} and/or I_{REF}. The lower part of the range can be improved by increasing I_{REF}.

EXTRA FEATURES FOR NE578

The NE578 has three extra functions over the NE577. These are power-down, mute and summing capabilities. To implement the power-down/mute mode, Pin 8 should be active low (open collector configuration, see Figure 19). If the power-down/mute feature is not used, Pin 8 should be left open. The NE578 only consumes 170µA of current at 3.6V when Pin 8 is activated. The power-down/mute mode is useful in designs when the function of the chip is not utilized at all times. This feature is a necessity where power conservation is critical.

In cellular and cordless applications, it is common to mix DTMF tones with the audio signal. This usually requires another op amp in which to mix the signals. With the NE578, however, the DTMF tones can be mixed internally on the compressor side. The DTMF signal is also compressed with the audio signal and ready for data transmission. Figure 2 shows that the summing of signals can be done at Pin 9 with R4 and C10. If amplification is not needed, then a 10k resistor is a recommended value for R4. In addition the summing amplifiers are capable of driving 600Ω loads.

THE NE577 AND NE578 AS A DUAL EXPANDOR

The compressor side can actually be configured as an expandor for both the NE577 and NE578. Figure 20 shows how this can be done. Because Pin 9 of the NE578 is available to the designer, the compressor side can not only be configured as an expandor, but as an expandor with summing capabilities.

OPERATING AT 1.8V

The NE577 and NE578 can operate at 1.8V. However, turning on the part at a V_{CC} of 1.8V requires two external resistors to bring V_{REF} to half V_{CC}. One resistor connects between V_{CC} and V_{REF}; the other connects from V_{REF} to ground. A typical value for these external resistors is approximately 20k. A lower value can be used, but power consumption will increase.

There are two cases where the external resistors can be eliminated.

Case 1: NE578 only

With the power supply at 1.8V and Pin 8 active low (power-down/mute activated), turn on the part. Then disable Pin 8 to power up.

Case 2: NE577 or NE578

During normal operations, the NE577 and NE578 can operate from at least a 2V battery. If the battery voltage drops to 1.8V, these parts will still continue to function.

NE577 AND NE578 DEMO BOARDS

Figures 21 shows the DIP package layout for the NE577 and NE578 demo boards, respectively. Figures 22 shows the SO layout for the NE577 and NE578 demo boards, respectively. The layouts are configured such that R1, R2, R3, and Rx can be removed and replaced easily. A switch is also available to change the operating mode of the compressor to an ALC configuration and vice versa (position the switch to the right for ALC mode).

When the compressor side is being evaluated, disconnect Rx completely from the socket on the demo boards. Rx should only be used when the compandor is being used for ALC.

For the NE578 demo board, two extra post are available. One is for power-down; the other is for summing external signals. To power-down, simply ground this post. To sum signals, connect the external signal to the proper post.

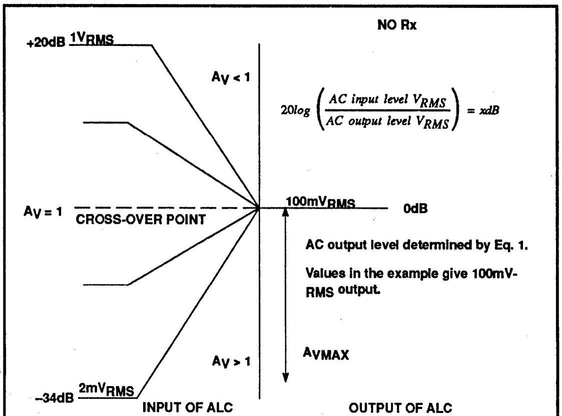


Figure 12. Dynamic Range of NE577 ALC Demonstration Board Without R_X

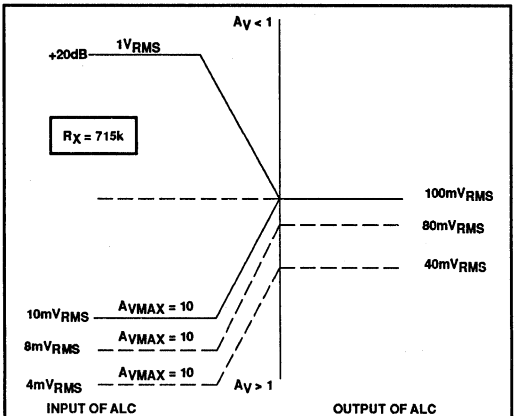


Figure 13. Dynamic Range of NE577 ALC Demo Board with R_X = 715kΩ

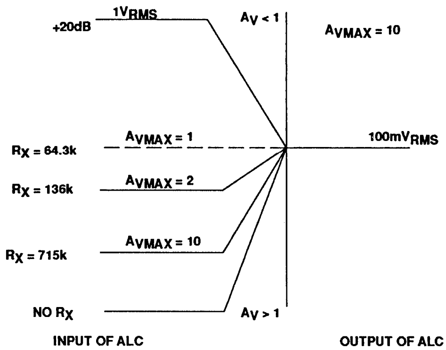


Figure 14. Dynamic Range of NE577 ALC Demo Board with Different R_X Values

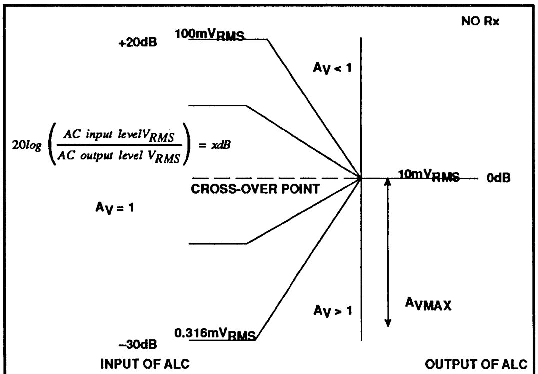


Figure 15. NE577 ALC: AC Output Level = $10mV_{RMS}$

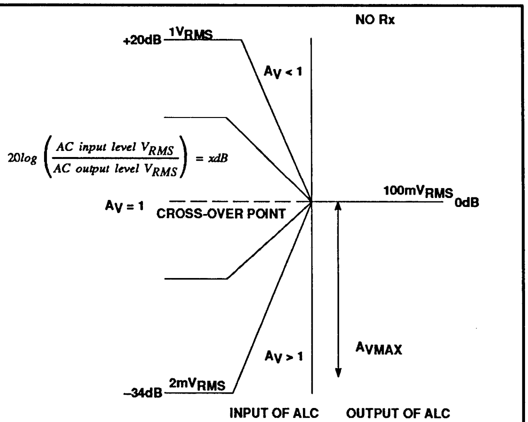


Figure 16. NE577 ALC: AC Output Level = $100mV_{RMS}$

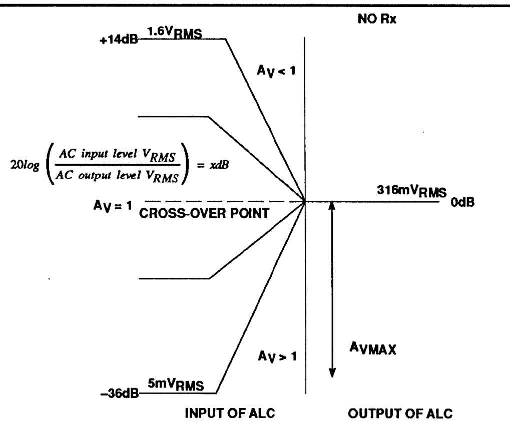


Figure 17. NE577 ALC: AC Output Level = $316mV_{RMS}$

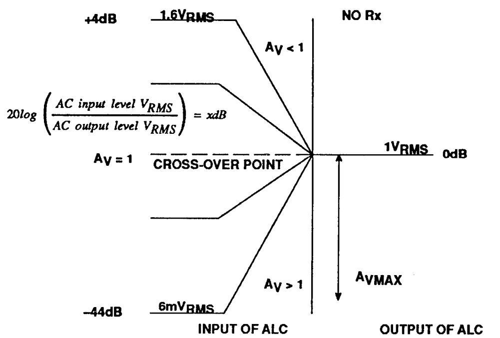
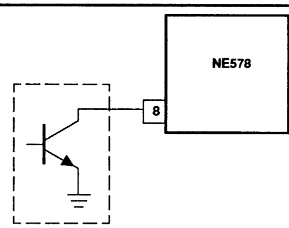


Figure 18. NE577 ALC: AC Output Level = $1V_{RMS}$



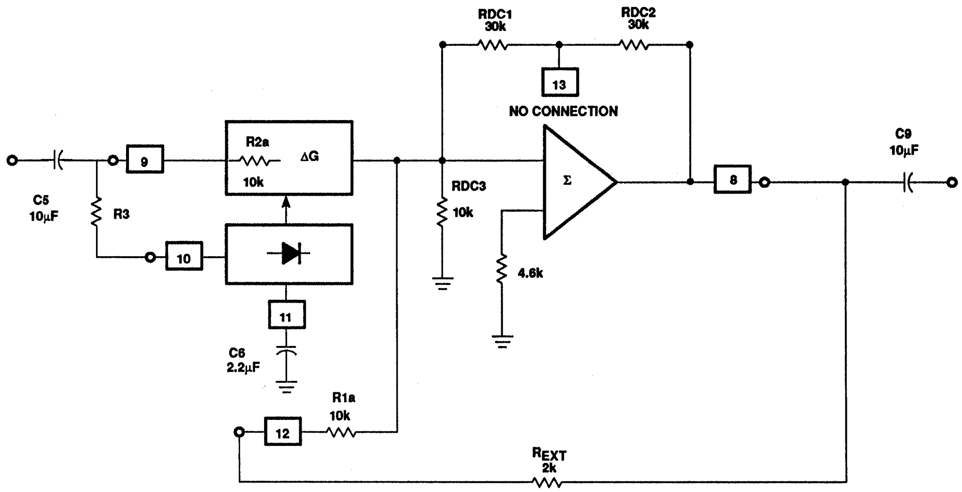
LEVEL AT PIN 8 SHOULD BE OPEN COLLECTOR TTL LEVELS

THE REASON FOR OPEN COLLECTOR CONFIGURATION IS TO ENSURE:

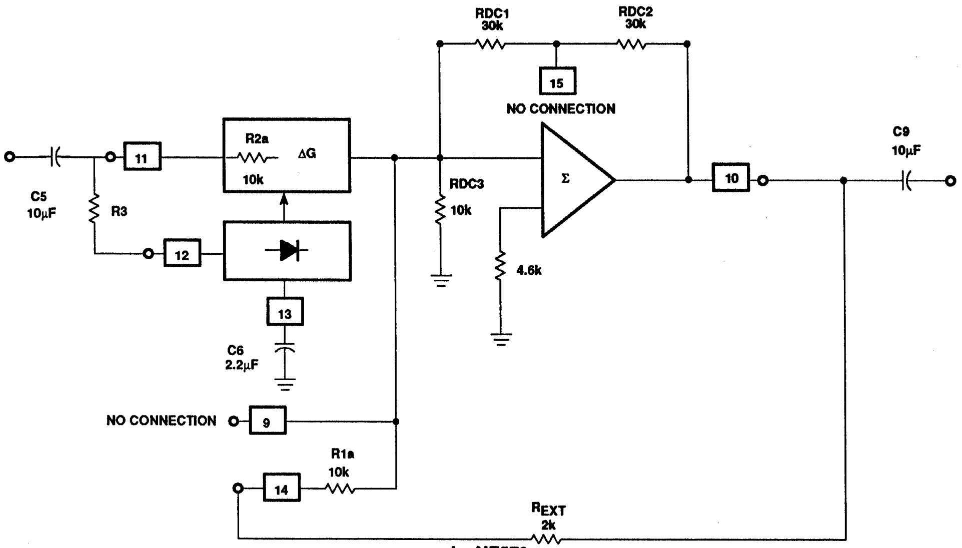
1) PIN 8 IS FLOATING WHEN POWER-DOWN/MUTE IS NOT IMPLEMENTED

2) PIN 8 IS GROUNDED WHEN POWER-DOWN/MUTE IS ACTIVE

Figure 19. Proper Use of NE578 Pin 8



a. NE577



b. NE578

Figure 20. Expandor Configuration for the Compressor Side

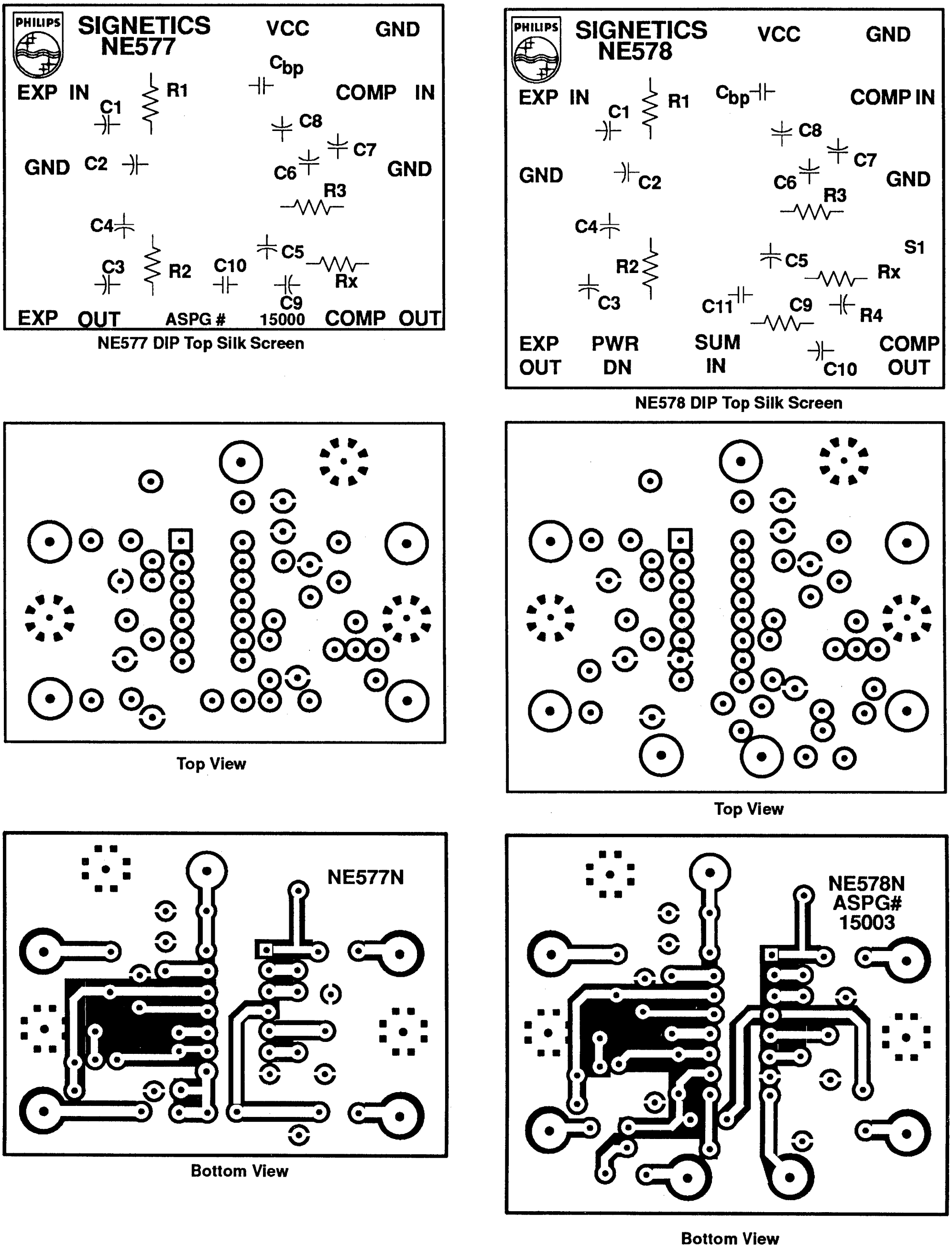


Figure 21. NE577 and NE578 DIP Application Board Layout

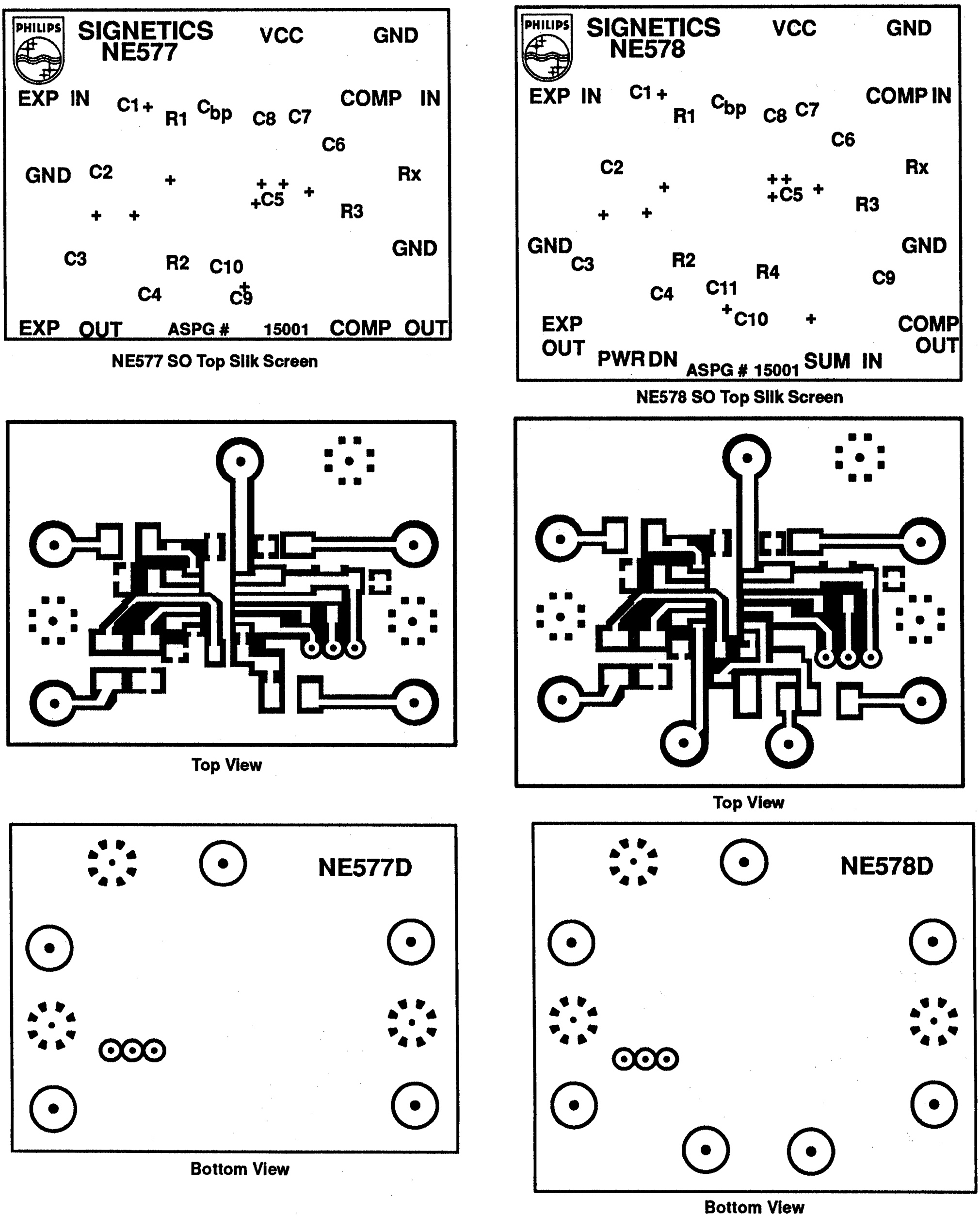


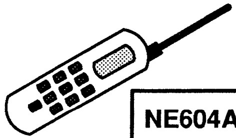
Figure 22. NE577 and NE578 SO Application Board Layout

Signetics

Section 3
FM IF Systems

RF Communications

INDEX



FM IF SYSTEMS FAMILY OVERVIEW

	NE604A	NE614A	NE605	NE615	NE606	NE616	NE607	NE617
V_{CC}	4.5–8V	4.5–8V	4.5–8V	4.5–8V	2.7–7V	2.7–7V	2.7–7V	2.7–7V
I_{CC}	3.3mA @ 6V	3.3mA @ 6V	5.7mA @ 6V	5.7mA @ 6V	3.5mA @ 3V	3.5mA @ 3V	3.5mA @ 3V	3.5mA @ 3V
Number of Pins	16	16	20	20	20	20	20	20
Package	DIP, SO	DIP, SO	DIP, SO, SSOP	DIP, SO, SSOP	DIP, SO, SSOP	DIP, SO, SSOP	DIP, SO, SSOP	DIP, SO, SSOP
Input Frequency (Max.)	Same as IF	Same as IF	500MHz	500MHz	150MHz	150MHz	150MHz	150MHz
Sensitivity Input Pin	0.22μV	0.22μV	0.22μV	0.22μV	0.31μV	0.31μV	0.31μV	0.31μV
Rin	1.6kΩ	1.6kΩ	4.7k	4.7kΩ	8kΩ	8kΩ	8kΩ	8kΩ
Mixer Conversion Gain	N/A	N/A	13dB	13dB	17dB	17dB	17dB	17dB
Input 3rd Order Intercept*	N/A	N/A	+4dBm	+4dBm	–10dBm	–10dBm	–10dBm	–10dBm
Process ft	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz
IF Frequency (Max.)	25MHz	25MHz	25MHz	25MHz	2MHz	2MHz	2MHz	2MHz
RSSI Range	90dB	80dB	90dB	80dB	90dB	80dB	90dB	80dB
RSSI Temp Comp	YES	YES	YES	YES	YES	YES	YES	YES
Conver Stages	N/A	N/A	Single	Single	Single	Single	Single	Single
Features	– High Sensitivity – High IF Frequency	– High Sensitivity – High IF Frequency – Relaxed 604A	– High Sensitivity – High Input/IF Frequency – SSOP 20	– High Sensitivity – High Input/IF Frequency – SSOP 20 – Relaxed 605	– Low Power – Audio Op–amp on output – RSSI Op–amp on output – SSOP 20	– Low Power – Audio Op–amp on output – RSSI Op–amp on output – SSOP 20 – Relaxed 606	– Low Power – Audio Op–amp on output – Frequency check – Buffered RSSI – Differential limiter output – SSOP 20	– Low Power – Audio Op–amp on output – Frequency check – Buffered RSSI – Differential limiter output – SSOP 20 – Relaxed 607
Applications	– Can combine with NE602A to produce a single conver receiver	– Can combine with NE612A to produce a single conver receiver	– Cellular – High Performance receivers – Industry Standard	– Cellular – Cordless Phone	– Portable Cellular – Portable Receivers – Cordless Phones	– Portable Cellular – Portable Receivers – Cordless Phones	– Portable Cellular AMPS/TACS NAMPS/NTACS – Portable eceiver – Cordless Phone	– Portable Cellular AMPS/TACS NAMPS/NTACS – Portable Receiver – Cordless Phone

*Note – 50Ω Source

Low-power FM IF

MC3361

DESCRIPTION

The MC3361 is a monolithic low-power FM IF signal processing system consisting of an oscillator, mixer, limiting amplifier, quadrature detector, filter amplifier, squelch, scan control and mute switch. It is intended for use in narrow band FM dual conversion communications equipment. The MC3361 is available in a 16-lead, dual-in-line plastic package and 16-lead SOL (surface-mounted miniature package).

FEATURES

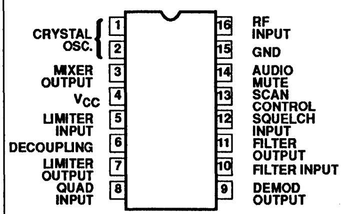
- 2.0V to 8.0V operation
- Low current: 4.2mA typ at VCC=4.0VDC
- Excellent sensitivity: 2.0µV for –3dB limiting typ
- Low external parts count
- Operation to 60MHz

APPLICATIONS

- Cordless telephone
- Narrow band receivers
- Remote control

PIN CONFIGURATION

D[1] and N Package

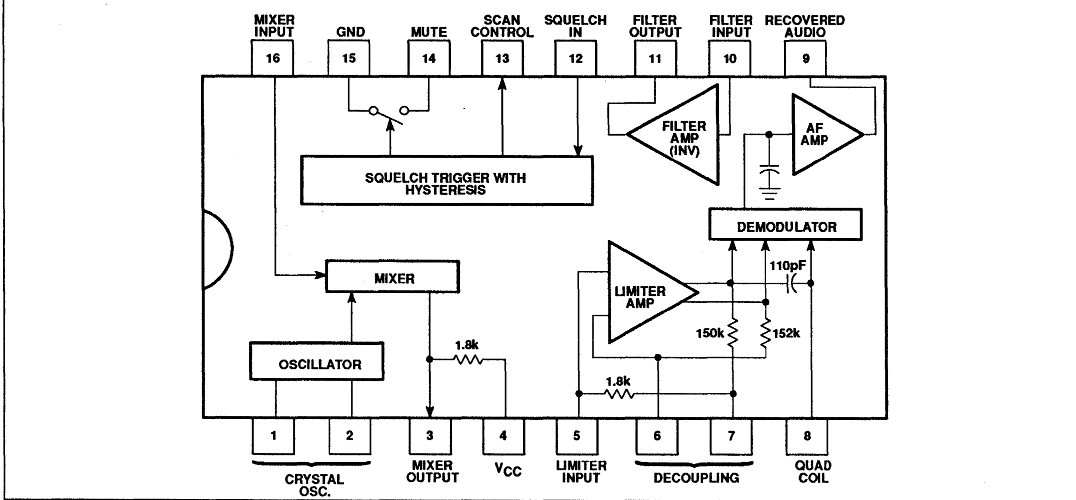


NOTE:
1. Available in 16-pin SOL package.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	–40 to +85°C	MC3361N
16-Pin Plastic SOL	–40 to +85°C	MC3361D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

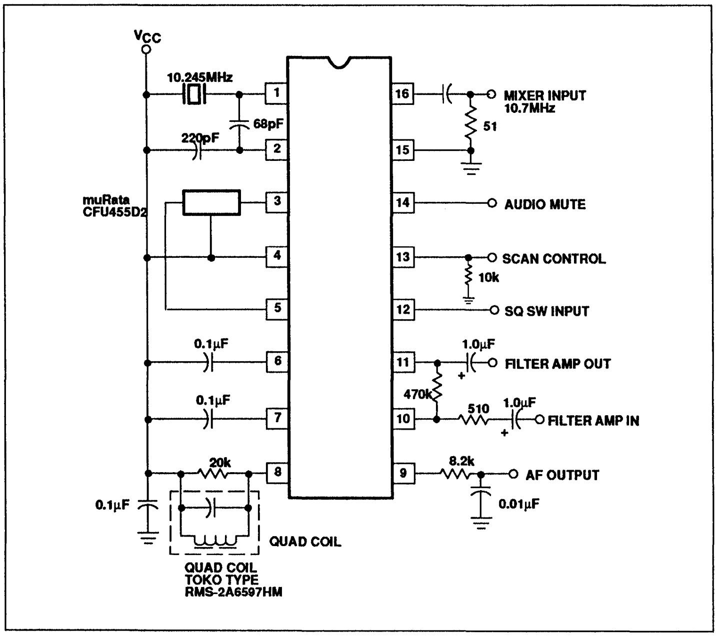
SYMBOL	PARAMETER	PIN	RATING	UNIT
V_{CC} (Max)	Power supply voltage	4	10	V_{DC}
V_{CC}	Generating supply voltage range	4	2.0 to 8.0	V_{DC}
	Detector input voltage	8	1.0	V_{P-P}
V_{16}	Input voltage (V_{CC}≥4.0V)	16	1.0	V_{RMS}
V_{14}	Mute function	14	–0.5 to 5.0	V_{PK}
T_J	Junction temperature		150	°C
T_A			–40 to +85	°C
T_{STG}	Storage temperature range		–65 to +150	°C

AC AND DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.0V_{DC}, f_O = 10.7MHz, Δf = +3.0kHz, f_{MOD} = 1.0kHz, T_A = 25°C unless otherwise noted.

PARAMETER	PIN	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Drain current (no signal) squelch off	4			4.2	7.0	mA
squelch on				5.4		
Input limiting voltage	16	–3.0dB limiting		2.0	6.0	μV
Detector output voltage	9			2.0		V_{DC}
Detector output impedance				450		Ω
Recovered audio output voltage	9	100	150	270		mV_{RMS}
Filter gain (10kHz)		V_{IN}=1.0mV_{RMS}	40	46		dB
Filter output voltage	11			1.7		V_{DC}
Trigger hysteresis				50		mV
Mute function low	14			10		Ω
Mute function high	14			10		MΩ
Scan function low (mute off)	13			0.5		V_{DC}
Scan function high (mute on)	13	V_{12}=GND				V_{DC}
Mixer conversion gain	3			27		dB
Mixer input resistance	16			3.6		kΩ
Mixer input capacitance	16			2.2		pF

TEST CIRCUIT



High performance low power FM IF system

NE/SA604A

DESCRIPTION

The NE/SA604A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA604A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA604A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

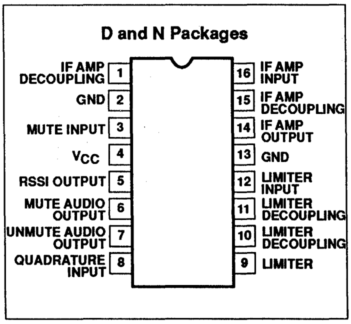
FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5µV across input pins (0.22µV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA604A meets cellular radio specifications

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

PIN CONFIGURATION



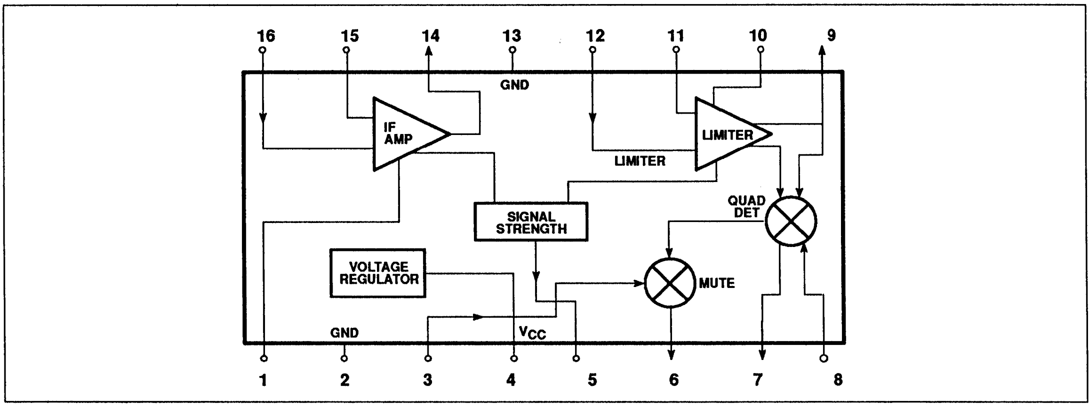
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE604AN
16-Pin Plastic SO (Surface-mount)	0 to +70°C	NE604AD
16-Pin Plastic DIP	-40 to +85°C	SA604AN
16-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA604AD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE604A SA604A	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE604A			SA604A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

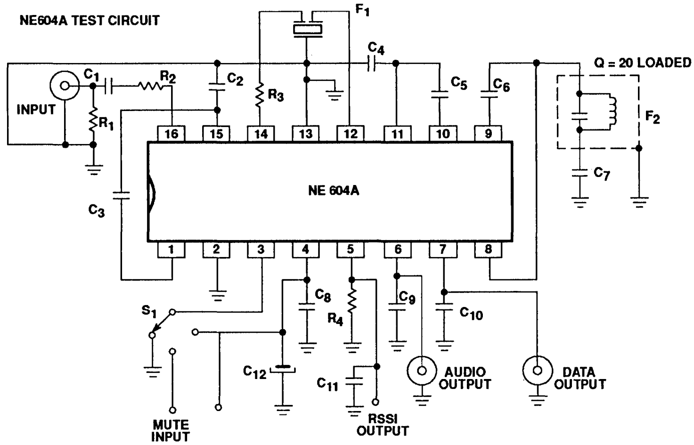
Typical reading at $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE604A			SA604A			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92			-92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de-emphasis	110	175	250	80	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530			530		mV_{RMS}
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = -118dBm	0	160	550	0	160	650	mV
		RF level = -68dBm	2.0	2.65	3.0	1.9	2.65	3.1	V
		RF level = -18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI range	R_4 = 100k (Pin 5)		90			90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ

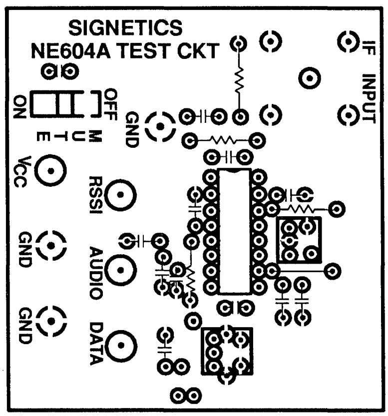
NOTE:
1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

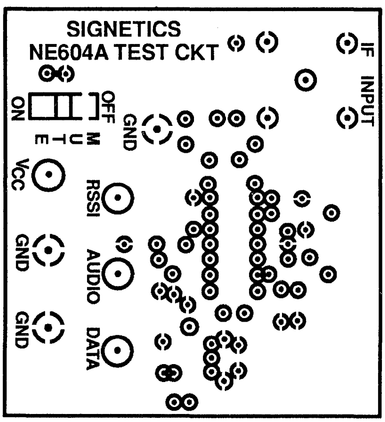
NE604 (50)	NE604A (1.5k)/NE605 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

The NE605 and NE604A are both derived from the same basic die. The NE605 performance plots are directly applicable to the NE604A.



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8μF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz IF Filter
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film





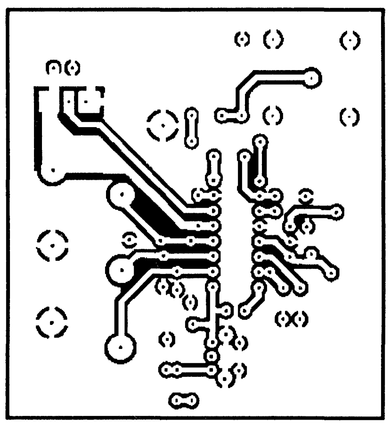


Figure 1. NE/SA604A Test Circuit

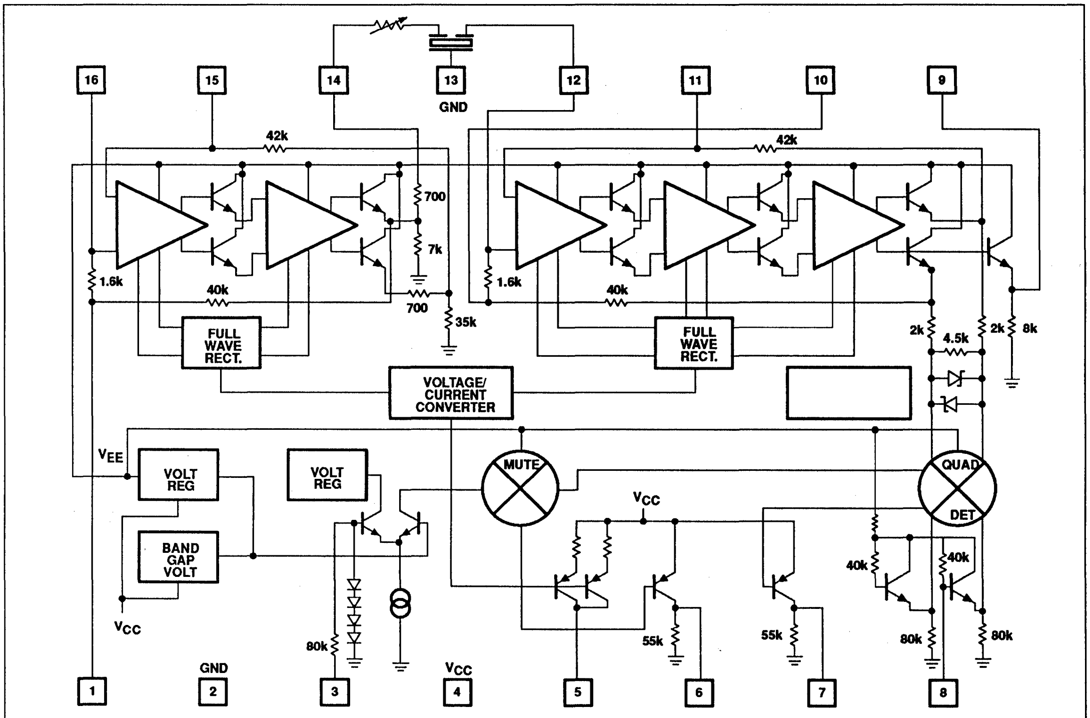


Figure 2. Equivalent Circuit

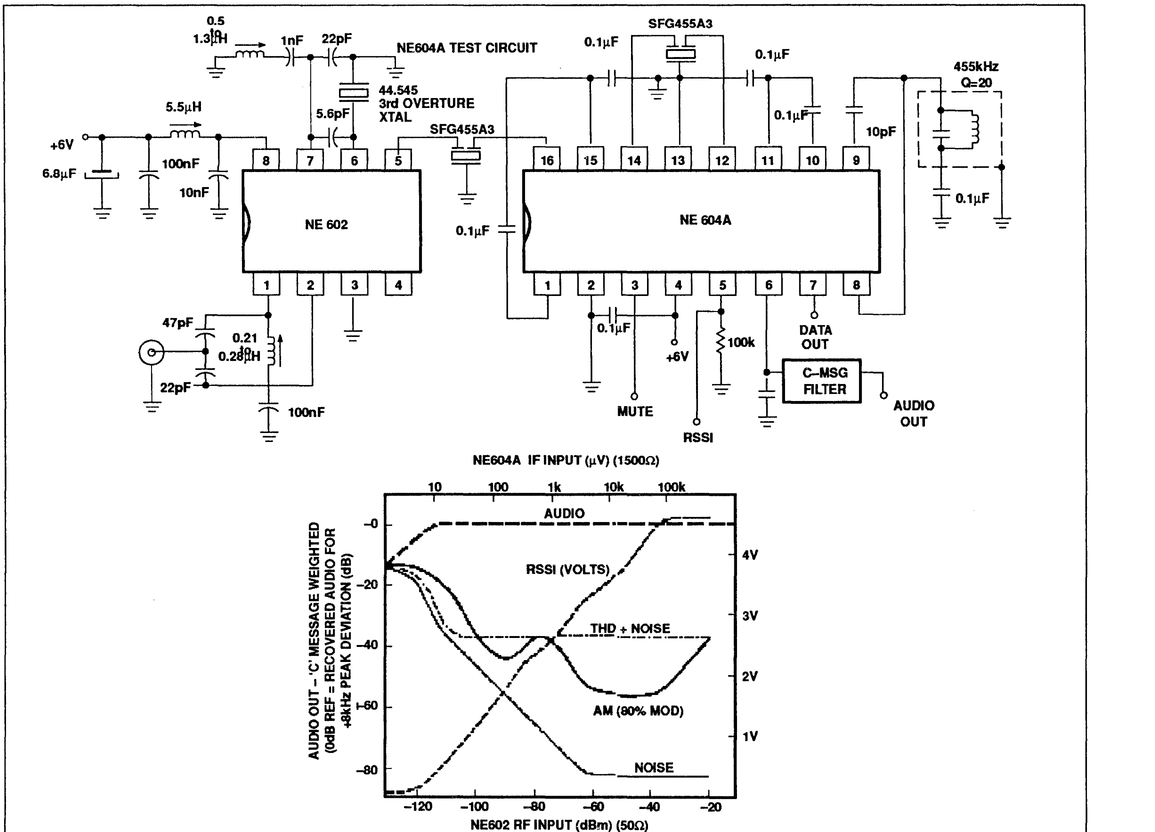


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA604A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA604A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

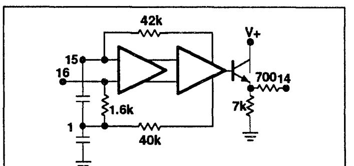


Figure 4. First Limiter Bias

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields)

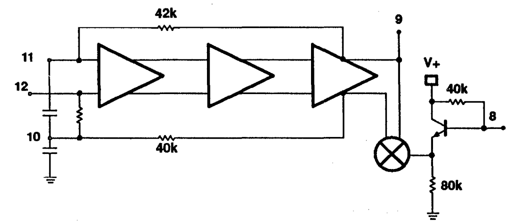


Figure 5. Second Limiter and Quadrature Detector

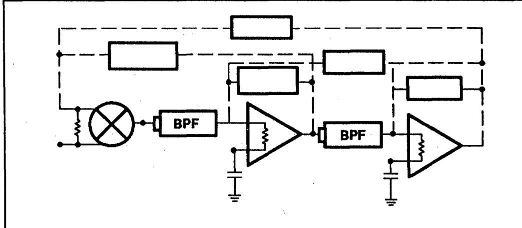


Figure 6. Feedback Paths

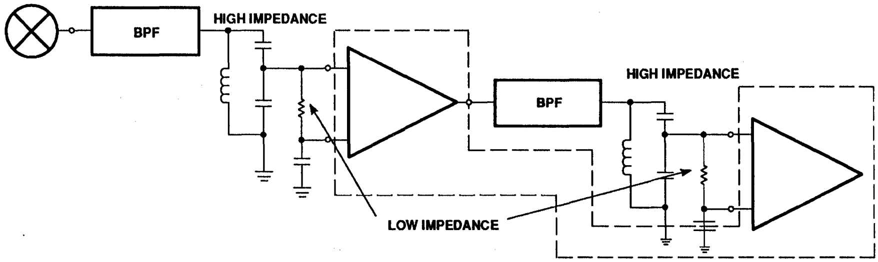


Figure 7. Terminating High Impedance Filters with Transformation to Low Impedance

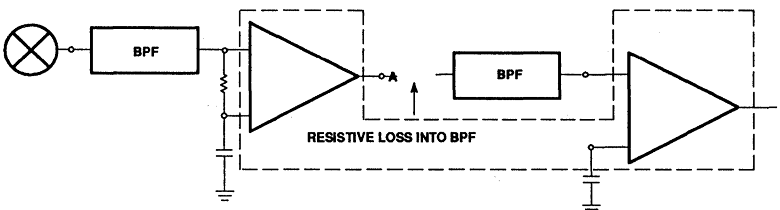


Figure 7. Low Impedance Termination and Gain Reduction
Figure 7. Practical Termination

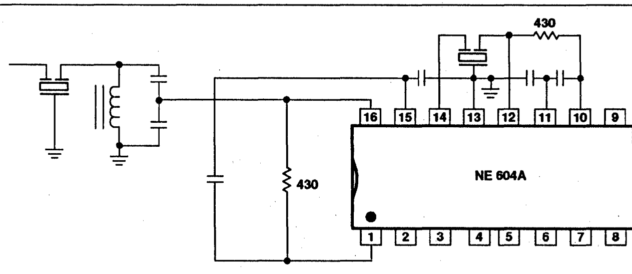


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in

Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE604A IF amplifiers, which is not specified, is low phase shift. The NE604A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

Stability Considerations

The high gain and bandwidth of the NE604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE604A

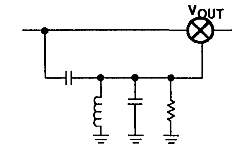


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \dot{V}_O - \dot{V}_{IN} = tg^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$ with respect to the V_{IN}.

$$\text{If } V_{IN} = A \sin \omega t \Rightarrow V_O = A \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] \quad (3)$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin \omega t \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] \quad (4)$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] = \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega \quad (5)$$

$$V_{OUT} \propto 2Q_1 \frac{\omega_1}{\omega} = \left[2Q_1 \left(\frac{\omega_1 + \Delta\omega}{\omega_1} \right) \right] \quad (6)$$

$$\text{For } \frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) ⇒ Choose a Q = 20

The internal R of the 604A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and L = 0.7mH.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10\text{pF}$ and $C_P = 164\text{pF}$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1\text{pF}$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers.

Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE604A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25µV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22µV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

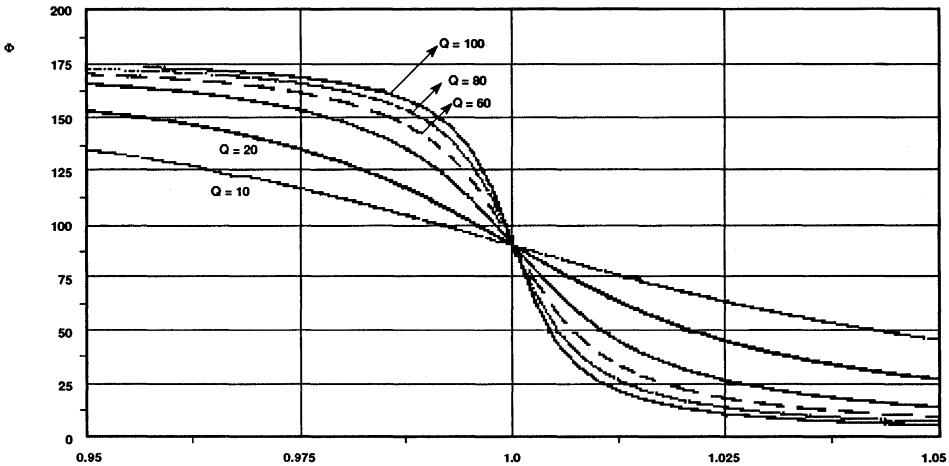


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

DESCRIPTION

The NE/SA614A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA614A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA614A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

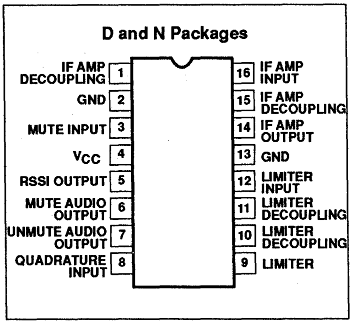
FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5µV across input pins (0.22µV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA614A meets cellular radio specifications

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

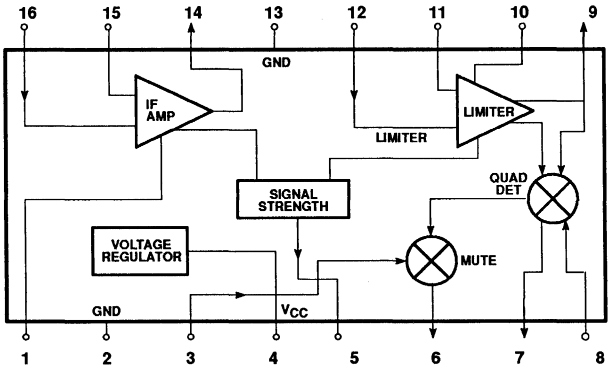
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE614AN
16-Pin Plastic SO (Surface-mount)	0 to +70°C	NE614AD
16-Pin Plastic DIP	-40 to +85°C	SA614AN
16-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA614AD

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE614A SA614A	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE614A			SA614A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at T_A = 25°C; V_{CC} = ±6V, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

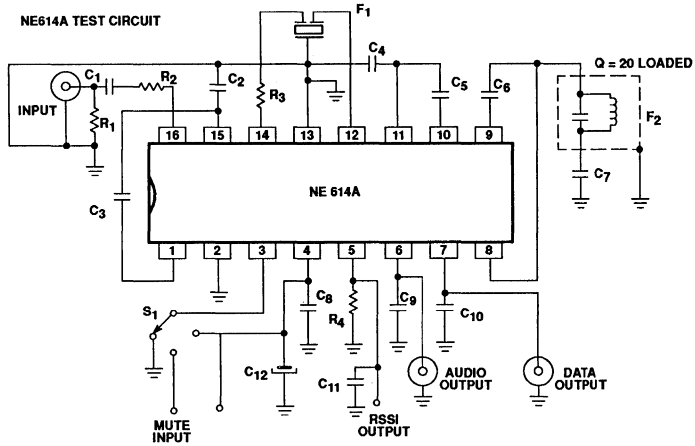
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA614A			UNITS
			MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92		dBm/50Ω
	AM rejection	80% AM 1kHz	25	33		dB
	Recovered audio level	15nF de-emphasis	60	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530		mV_{RMS}
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	RSSI output[1]	RF level = -118dBm	0	160	800	mV
		RF level = -68dBm	1.7	2.50	3.3	V
		RF level = -18dBm	3.6	4.80	5.8	V
	RSSI range	R_4 = 100k (Pin 5)		80		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±2.0		dB
	IF input impedance		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ

NOTE:

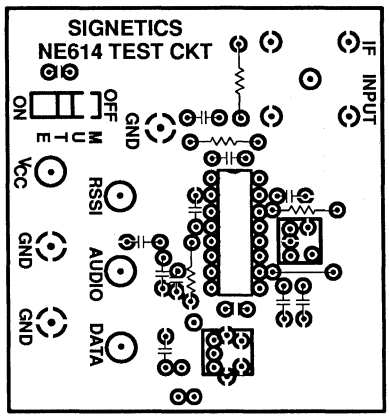
1. NE614A data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE614A (50)	NE614A (1.5k)/NE615 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

The NE615 and NE614A are both derived from the same basic die. The NE615 performance plots are directly applicable to the NE614A.



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8μF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz IF Filter
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film



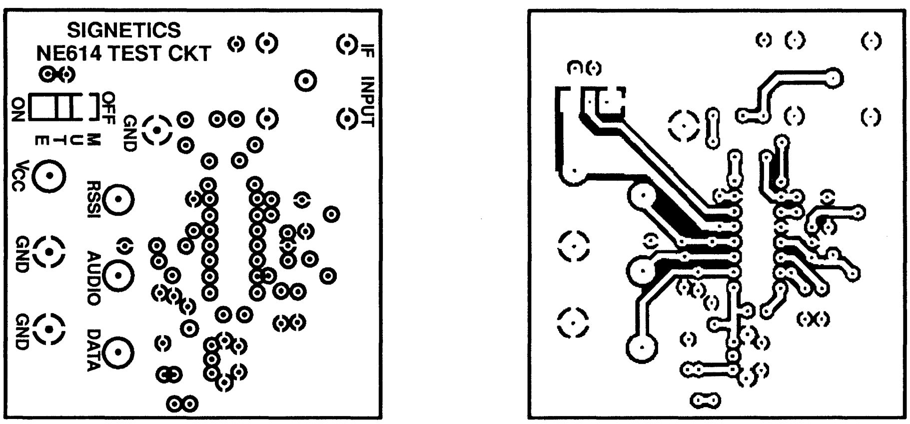


Figure 1. NE/SA614A Test Circuit

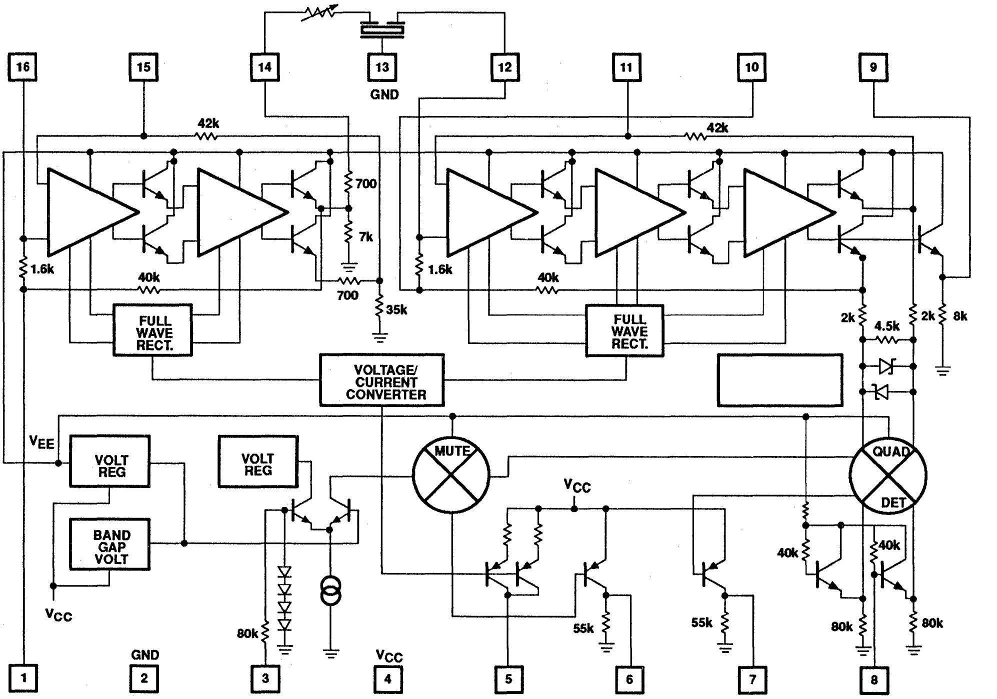


Figure 2. Equivalent Circuit

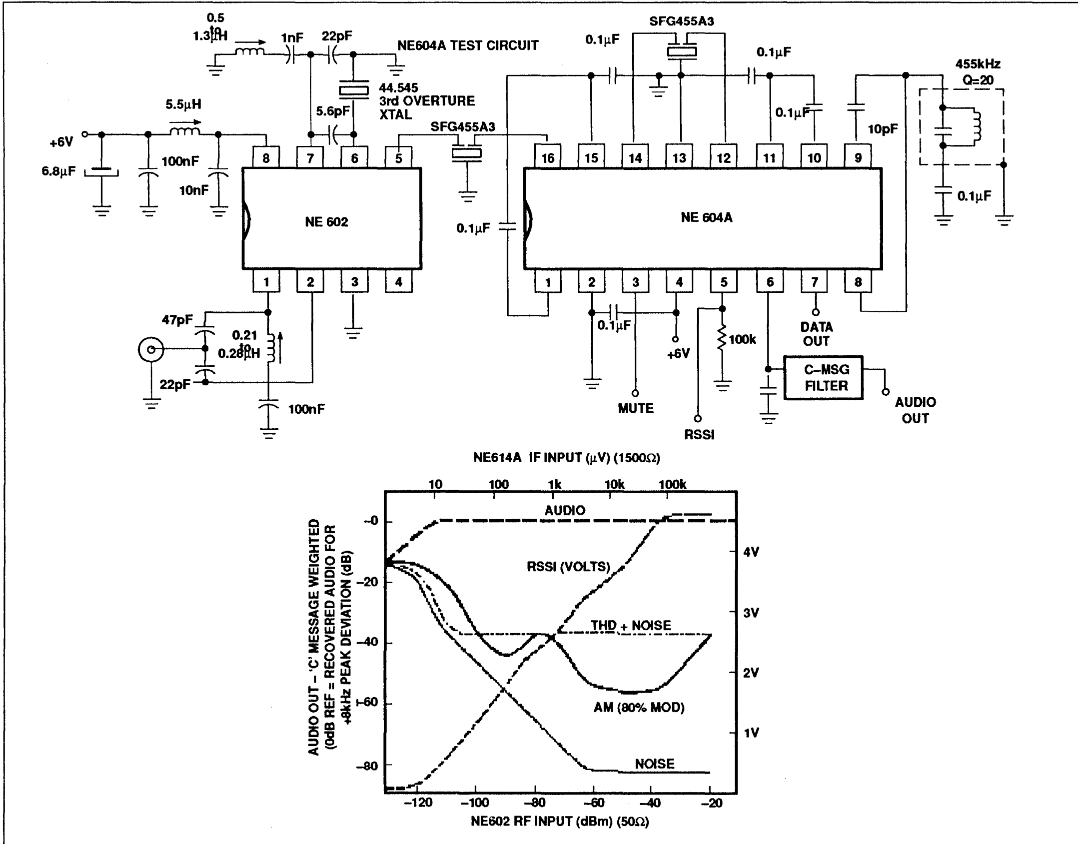


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA614A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA614A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA614A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

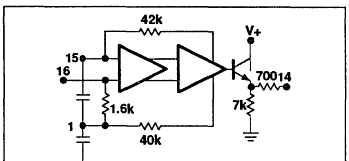


Figure 4. First Limiter Bias

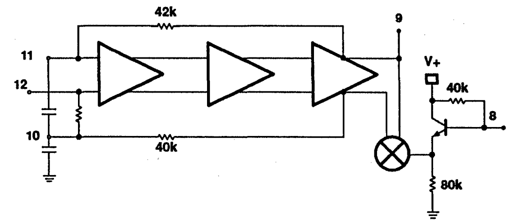


Figure 5. Second Limiter and Quadrature Detector

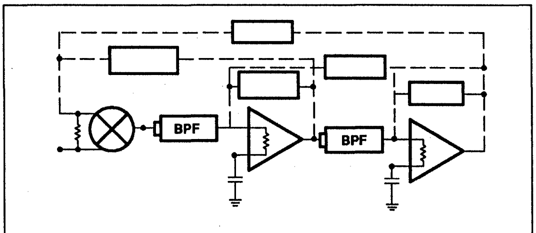


Figure 6. Feedback Paths

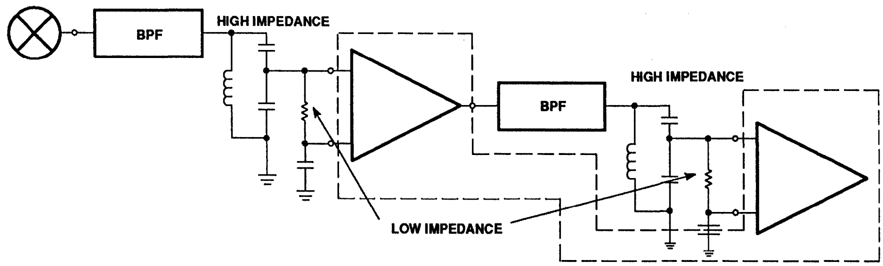


Figure 7. Terminating High Impedance Filters with Transformation to Low Impedance

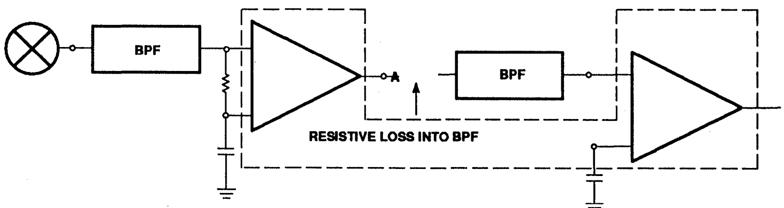


Figure 7. Low Impedance Termination and Gain Reduction
Figure 7. Practical Termination

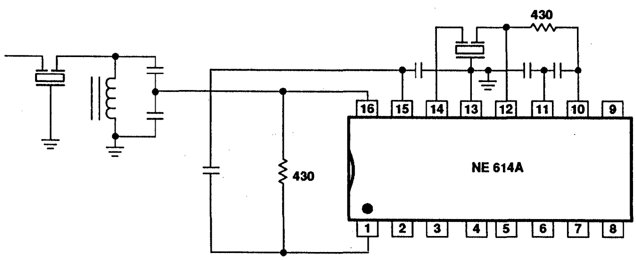


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain.

Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE614A IF amplifiers, which is not specified, is low phase shift. The NE614A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

Stability Considerations

The high gain and bandwidth of the NE614A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430W external resistors are applied in parallel to the internal 1.6kW load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE614A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated).

If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE614A

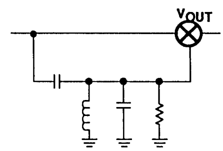


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = \quad t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

$$\text{If } V_{IN} = A \sin \omega t \Rightarrow V_O = A \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (3)$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin \omega t \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (4)$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1} \omega\right] \quad (5)$$

$$= \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right) \omega$$

$$V_{OUT} \propto 2Q_1 \frac{\omega_1}{\omega} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

$$\text{For } \frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) ⇒ Choose a Q = 20

The internal R of the 614A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S$ = 174pF and L = 0.7mH.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a C_S = 10pF and C_P = 164pF (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of C_S = 1pF is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers.

Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE614A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25µV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22µV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE614A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

Low power FM IF system NE/SA614A

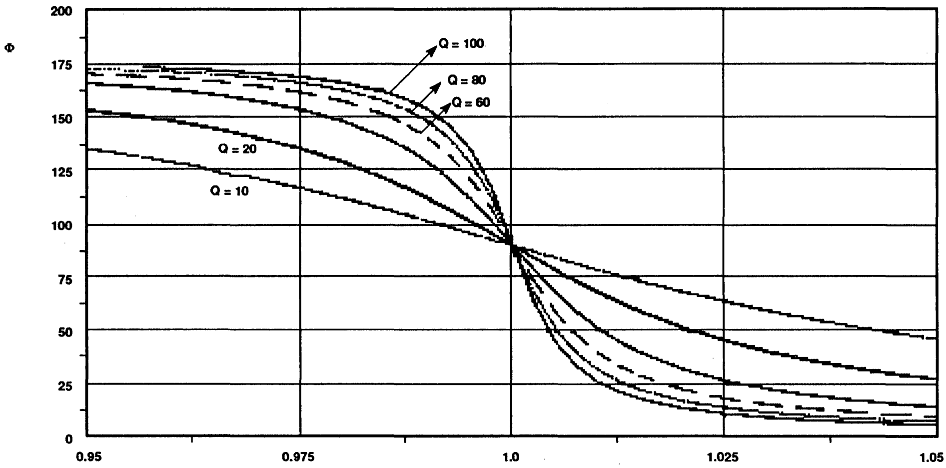


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

Audio decibel level detector with meter driver

AN1991

Author: Robert J. Zavrel Jr.

DESCRIPTION

Although the NE604 was designed as an RF device intended for the cellular radio market, it has features which permit other design configurations. One of these features is the Received Signal Strength Indicator (RSSI). In a cellular radio, this function is necessary for continuous monitoring of the received signal strength by the radio's microcomputer. This circuit provides a logarithmic response proportional to the input signal level. The NE604 can provide this logarithmic response over an 80dB range up to a 15MHz operating frequency. This paper describes a technique which optimizes this useful function within the audio band.

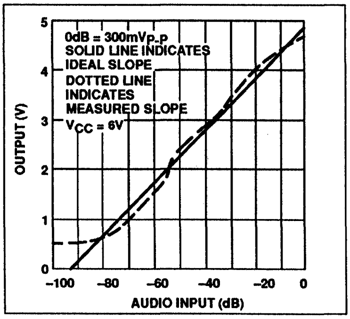
A sensitive audio level indicator circuit can be constructed using two integrated circuits: the NE604 and NE532. This circuit draws very little power (less than 5mA with a single 6V power supply) making it ideal for portable battery operated equipment. The small size and low-power consumption belie the 80dB dynamic range and 10.5µV sensitivity.

The RSSI function requires a DC output voltage which is proportional to the $\log_{10}$ of the input signal level. Thus a standard 0-5 voltmeter can be linearly calibrated in decibels over a single 80dB range. The entire circuit is composed of 9 capacitors and two resistors along with the two ICs. No tuning or calibration is required in a manufacturing setting.

The Audio Input vs Output Graph shows that the circuit is within 1.5dB tolerance over the 80dB range for audio frequencies from 100Hz to 10kHz. Higher audio levels can be measured by placing an attenuator ahead of the input capacitor. The input impedance is high (about 50k), so lower impedance terminations (50 or 600Ω) will not be affected by the input impedance. If very accurate tracking is required (<0.5dB accuracy), a 40 or 50dB segment can be "selected". A range switch can then be added with appropriate attenuators if more than 40 or 50dB dynamic range is required.

There are two amplifier sections in the 604 with 2 and 3 stages in the first and second sections respectively. Each stage outputs a sample current to a summing circuit. The summing circuit has a current mirror which appears at Pin 5. This current is proportional to the $\log_{10}$ of the input audio signal. A voltage is dropped across the 100k resistor by the current, and a 0.1µF capacitor is used to bypass and filter the output signal. The 532 op amp is used as a buffer and meter driver, although a digital voltmeter could replace both the op amp and the meter shown. The rest of the capacitors are used for power supply and amplifier input bypassing.

The RC circuit between Pins 14 and 12 forms a low-pass filter which can be adjusted by changing the value of C1. Raising the capacitance will lower the cut-off frequency and also lower the zero signal output resting voltage (about 0.6V). Lowering the capacitance value will have the opposite effect with some reduction in dynamic range, but will raise the frequency response. The 2kΩ resistor value provides the near-ideal inter-stage loss for maximum RSSI linearity. C2 can also be changed. The trade-off here is between output damping and ripple. Most analog and digital metering methods will tend to cancel the effects of small or moderate ripple voltages through integration, but high ripple voltages should be avoided.



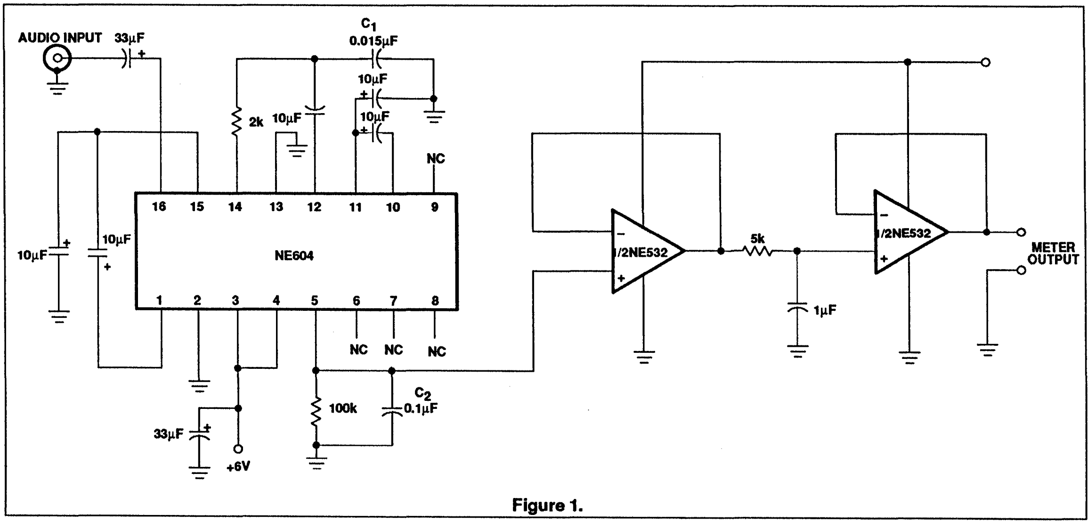


Figure 1.

A second op amp is used with an optional second filter. This filter has the advantage of a low impedance signal source by virtue of the first op amp. Again, a trade-off exists between meter damping and ripple attenuation. If very low ripple and low damping are both required, a more complex active low-pass filter should be constructed.

Some applications of this circuit might include:

1. Portable acoustic analyzer
2. Microphone tester
3. Audio spectrum analyzer
4. VU meters
5. S-meter for direct conversion radio receiver
6. Audio dynamic range testers
7. Audio analyzers (THD, noise, separation, response, etc.)

High sensitivity applications of low-power RF/IF integrated circuits

AN1993

ABSTRACT

This paper discusses four high sensitivity receivers and IF (Intermediate Frequency) strips which utilize intermediate frequencies of 10.7MHz or greater. Each circuit utilizes a low-power VHF mixer and high-performance low-power IF strip. The circuit configurations are

1. 45 or 49MHz to 10.7MHz narrowband,
2. 90MHz to 21.4MHz narrowband,
3. 100MHz to 10.7MHz wideband, and
4. 152.2MHz to 10.7MHz narrowband.

Each circuit is presented with an explanation of component selection criteria, (to permit adaptation to other frequencies and bandwidths). Optional configurations for local oscillators and data demodulators are summarized.

INTRODUCTION

Traditionally, the use of 10.7MHz as an intermediate frequency has been an attractive means to accomplish reasonable image rejection in VHF/UHF receivers. However, applying significant gain at a high IF has required extensive gain stage isolation to avoid instability and very high current consumption to get adequate amplifier gain bandwidth. By enlightened application of two relatively new low power ICs, Signetics NE602 and NE604A, it is possible to build highly producible IF strips and receivers with input frequencies to several hundred megahertz, IF frequencies of 10.7 or 21.4MHz, and sensitivity less than 2μV (in many cases less than 1μV). The Signetics new NE605 combines the function of the NE602 and the NE604A. All of the circuits described in this paper can also be implemented with the NE605. The NE602 andNE604A were utilized for this paper to permit optimum gain stage isolation and filter location.

THE BASICS

First let's look at why it is relevant to use a 10.7 or 21.4MHz intermediate frequency. 455kHz ceramic filters offer good selectivity and small size at a low price. Why use a higher IF? The fundamental premise for the answer to this question is that the receiver architecture is a hetrodyne type as shown in Figure 1.

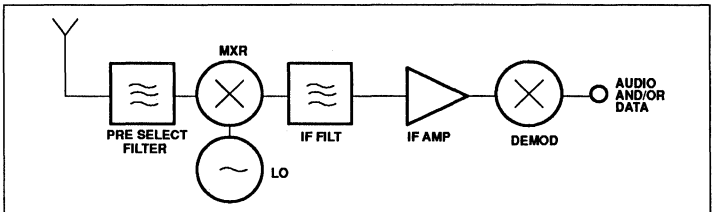


Figure 1. Basic Hetrodyne Receiver

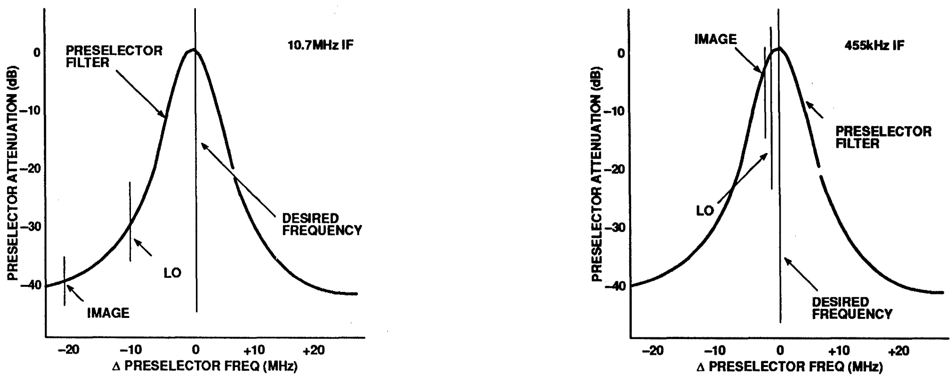


Figure 2. Effects of Preselection on Images

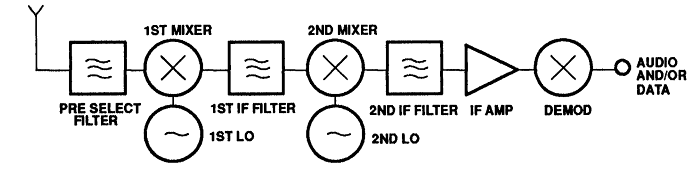


Figure 3. Dual Conversion

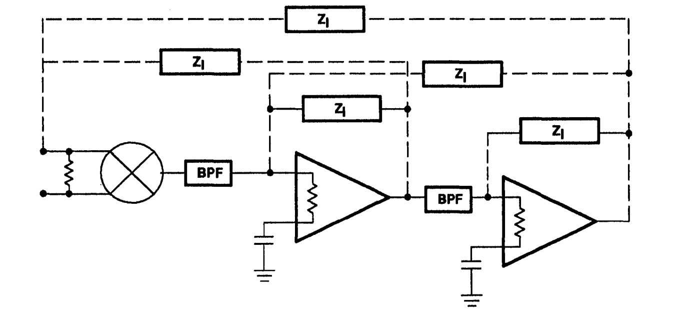


Figure 4. Feedback Paths

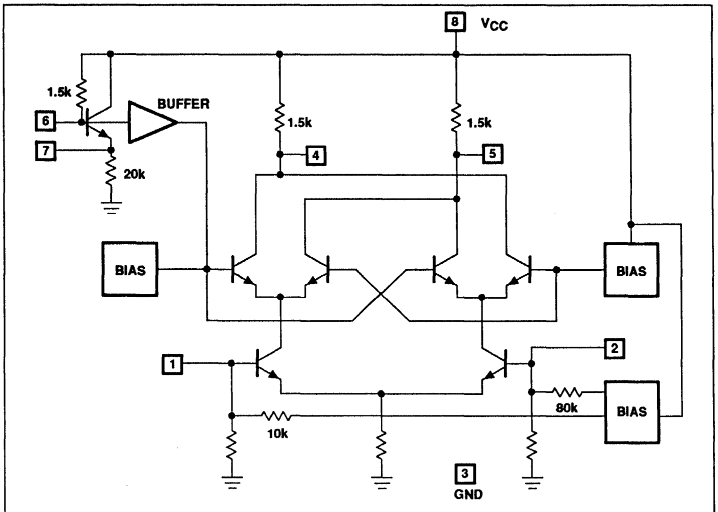


Figure 5. NE602 Equivalent Circuit

A pre-selector (bandpass in this case) precedes a mixer and local oscillator. An IF filter follows the mixer. The IF filter is only supposed to pass the difference (or sum) of the local oscillator (LO) frequency and the preselector frequency.

The reality is that there are always two frequencies which can combine with the LO: The pre-selector frequency and the "image" frequency. Figure 2 shows two hypothetical pre-selection curves. Both have 3dB bandwidths of 2MHz. This type of pre-selection is typical of consumer products such as cordless telephone and FM radio. Figure 2A shows the attenuation of a low side image with 10.7MHz. Figure 2B shows the very limited attenuation of the low side 455kHz image.

If the single conversion architecture of Figure 1 were implemented with a 455kHz IF, any interfering image would be received almost as well as the desired frequency. For this reason, dual conversion, as shown in Figure 3, has been popular.

In the application of Figure 3, the first IF must be high enough to permit the pre-selector to reject the images of the first mixer and must have a narrow enough bandwidth that the second mixer images and the intermod products due to the first mixer can be attenuated. There's more to it than that, but those are the basics. The multiple conversion hetrodyne works well, but, as Figure 3 suggests, compared to Figure 2 it is more complicated. Why, then, don't we use the approach of Figure 2?

THE PROBLEM

Historically there has been a problem: Stability! Commercially available integrated IF amplifiers have been limited to about 60dB of gain. Higher discrete gain was possible if each stage was carefully shielded and bypassed, but this can become a nightmare on a production line. With so little IF gain available, in order to receive signals of less than 10μV it was necessary to add RF gain and this, in turn, meant that the mixer must have good large signal handling capability. The RF gain added expense, the high level mixer added expense, both added to the potential for instabilities, so the multiple conversion started looking good again.

But why is instability such a problem in a high gain high IF strip? There are three basic mechanisms. First, ground and the supply line are potentially feedback mechanisms from stage-to-stage in any amplifier. Second, output pins and external components create fields which radiate back to inputs. Third,

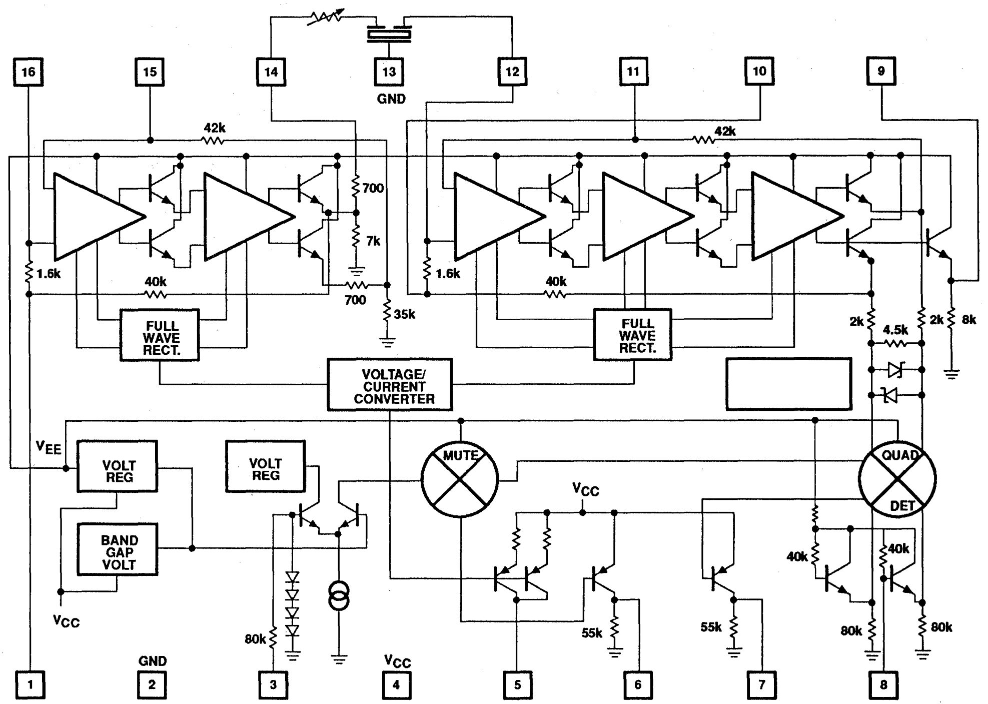


Figure 6. NE604A Equivalent Circuit

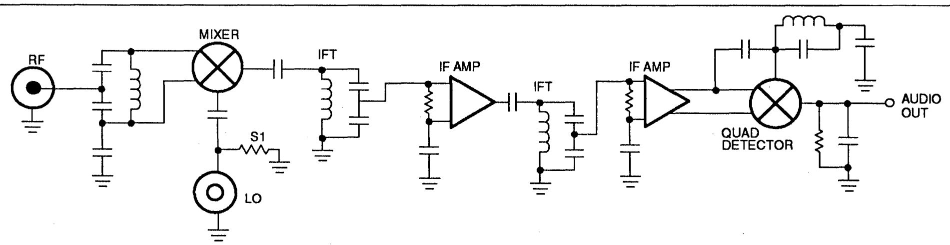


Figure 7. Symbolic Circuit

layout capacitances become feedback mechanisms. Figure 4 shows the fields and capacitances symbolically.

If Z_F represents the impedance associated with the circuit feedback mechanisms (stray capacitances, inductances and radiated fields), and Z_{IN} is the equivalent input impedance, a divider is created. This divider must have an attenuation factor greater than the gain of the amplifier if the amplifier is to remain stable.

- If gain is increased, the input-to-output isolation factor must be increased.
- As the frequency of the signal or amplifier bandwidth increases, the impedance of the layout capacitance decreases thereby reducing the attenuation factor.

The layout capacitance is only part of the issue. In order for traditional 10.7MHz IF amplifiers to operate with reasonable gain bandwidth, the amount of current in the amplifiers needed to be quite high. The CA3089 operates with 25mA of typical quiescent current. Any currents which are not perfectly differential must be carefully bypassed to ground. The higher the current, the more difficult the challenge. And limiter outputs and quadrature components make excellent field generators which add to the feedback scenario. The higher the current, the larger the field.

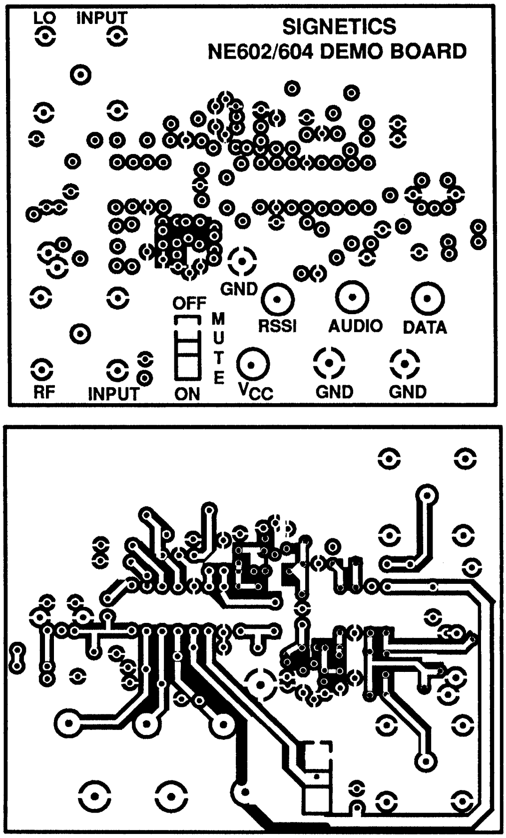


Figure 8. Circuit Board Layout

THE SOLUTION

The NE602 is a double balanced mixer suitable for input frequencies in excess of 500MHz. It draws 2.5mA of current. The NE604A is an IF strip with over 100dB of gain and a 25MHz small signal bandwidth. It draws 3.5mA of current. The circuits in this paper will demonstrate ways to take advantage of this low current and 75dB or more of the NE604A gain in receivers and IF strips that would not be possible with traditional integrated circuits. No special tricks are used, only good layout, impedance planning and gain distribution.

THE MIXER

The NE602 is a low power VHF mixer with built-in oscillator. The equivalent circuit is shown in Figure 5. The basic attributes of this mixer include conversion gain to frequencies greater than 500MHz, a noise figure of 4.6dB @ 45MHz, and a built-in oscillator which can be used up to 200MHz. LO can be injected.

For best performance with any mixer, the interface must be correct. The input impedance of the NE602 is high, typically 3kΩ in parallel with 3pF. This is not an easy match from 50Ω. In each of the examples which follow, an equivalent 50:1.5k match was used. This compromise of noise, loss, and match yielded good results. It can be improved upon. Match to crystal filters will require special attention, but will not be given focus in this paper.

This oscillator is a single transistor with an internal emitter follower driving the mixer. For best mixer performance, the LO level needs to be approximately 220mV$_{RMS}$ at the base of the oscillator transistor (Pin 6). A number of oscillator configurations are presented at the end of this paper. In each of the prototypes for this paper, the LO source was a signal generator. Thus, a 51Ω resistor was used to terminate the signal generator. The LO is then coupled to the mixer through a DC blocking capacitor. The signal generator is set for 0dBm. The impedance at the LO input (Pin 6) is approximately 20kΩ. Thus, required power is very low, but 0dBm across 51Ω does provide the necessary 220mV$_{RMS}$.

The outputs of the NE602 are loaded with 1.5kΩ internal resistors. This makes interface to 455kHz ceramic filters very easy. Other filter types will be addressed in the examples.

THE IF STRIP

The basic functions of the NE604A are ordinary at first glance: Limiting IF, quadrature detector, signal strength meter, and mute switch. **However, the performance of each of these blocks is superb.** The IF has 100dB of gain and 25MHz bandwidth. This feature will be exploited in the examples. The signal strength indicator has a 90dB log output characteristic with very good linearity. There are two audio outputs with greater than 300kHz bandwidth (one can be muted greater than 70dB). The total supply current is typically 3.5mA. This is the other factor which permits high gain and high IF.

Figure 6 shows an equivalent circuit of the NE604A. Each of the IF amplifiers has a 1.6kΩ input impedance. The input impedance is achieved by splitting a DC feedback bias resistor. The input impedance will be manipulated in each of the examples to aid stability.

BASIC CONSIDERATIONS

In each of the circuits presented, a common layout and system methodology is used. The basic circuit is shown symbolically in Figure 7.

At the input, a frequency selective transformation from 50Ω to 1.5kΩ permits analysis of the circuit with an RF signal generator. A second generator provides LO. This generator second generator provides LO. This generator is terminated with a 51Ω resistor. The output of the mixer and the input of the first limiter are both high impedance (1.5Ω nominal). As indicated previously, the input impedance of the limiter must be low enough to attenuate feedback signals. So, the input impedance of the first limiter is modified with an external resistor. In most of the examples, a 430Ω external resistor was used to create a 330Ω input impedance (430//1.5kΩ). The first IF filter is thus designed to present 1.5kΩ to the mixer and 330Ω to the first limiter.

The same basic treatment was used between the first and second limiters. However, in each of the 10.7MHz examples, this interstage filter is not an L/C tank; it is a ceramic filter. This will be explained in the first example.

After the second limiter, a conventional quadrature detector demodulates the FM or FSK information from the carrier and a simple low pass filter completes the demodulation process at the audio outputs.

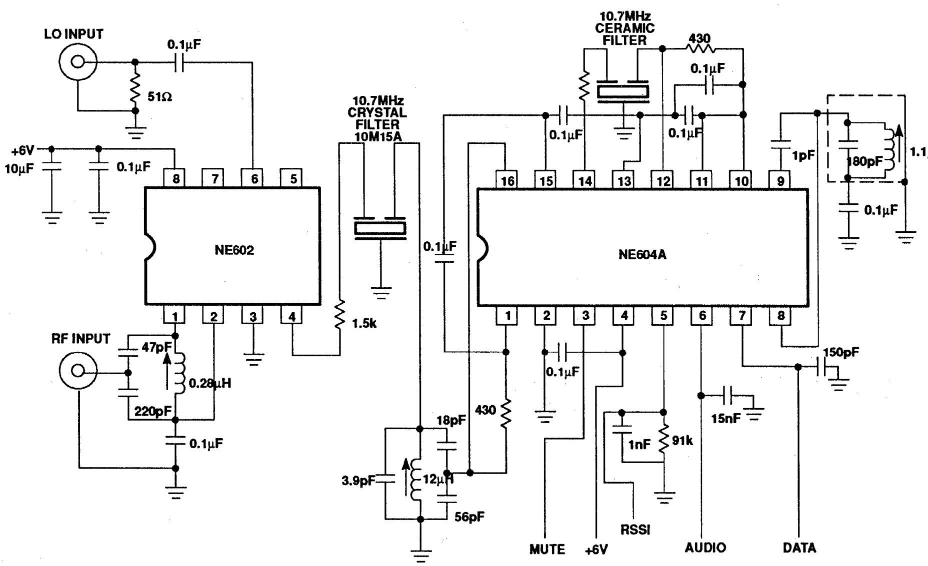


Figure 9. NE602/604A Demonstration Circuit with RF Input of 45MHz and IF of 21.4MHz ±7.5kHz

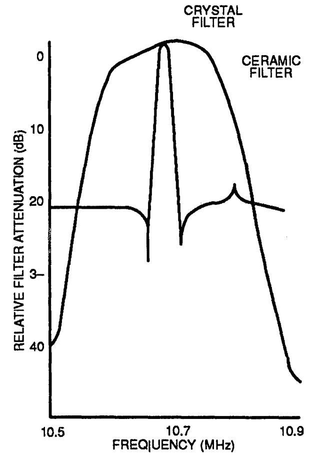


Figure 10. Passband Relationship

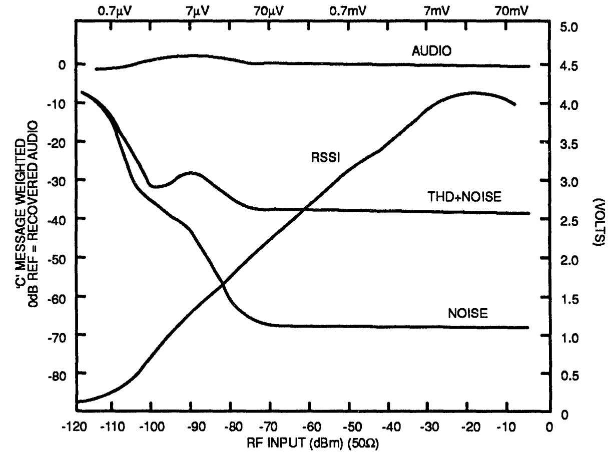


Figure 11. VHF or UHF 2nd Conversion (Narrow Band)

As mentioned, a single layout was used for each of the examples. The board artwork is shown in Figure 8. Special attention was given to: (1) Creating a maximum amount of ground plane with connection of the component side and solder side ground at locations all over the board; (2) careful attention was given to keeping a ground ring around each of the gain stages. The objective was to provide a shunt path to ground for any stray signal which might feed back to an input; (3) leads were kept short and relatively

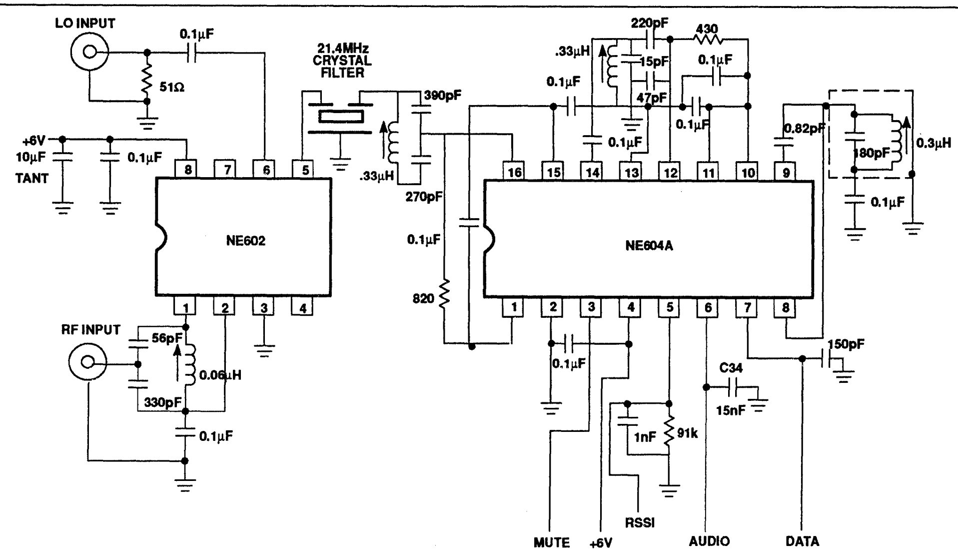


Figure 12. NE602/604A Demonstration Circuit with RF Input of 90MHz and IF of 21.4MHz ±7.5kHz

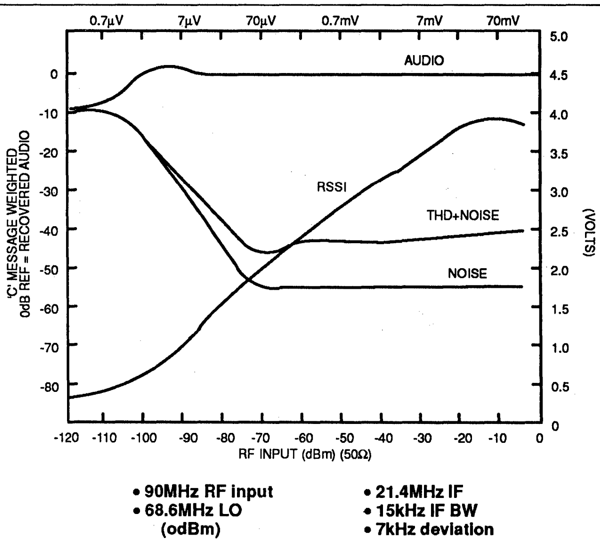


Figure 13. UHF Second Conversion (Narrow Band) or VHF Single Conversion (Narrow Band)

wide to minimize the potential for them to radiate or pick up stray signals; finally (and very important), (4) RF bypass was done as close as possible to supply pins and inputs, with a good (10µF) tantalum capacitor completing the system bypass.

EXAMPLE: 45MHZ TO 10.7MHZ NARROWBAND

As a first example, consider conversion from 45MHz to 10.7MHz. There are commercially available filters for both frequencies so this is a realistic combination for a second IF in a UHF receiver. This circuit can also be applied to cordless telephone or short range communications at 46 or 49MHz. The circuit is shown in Figure 9.

The 10.7MHz filter chosen is a type commonly available for 25kHz channel spacing. It has a 3dB bandwidth of 15kHz and a termination requirement of 3kΩ/2pF. To present 3kΩ to the input side of the filter, a 1.5kΩ resistor was used between the NE602 output (which has a 1.5kΩ impedance) and the filter. Layout capacitance was close enough to 2pF that no adjustment was necessary. This series-resistance approach introduces an insertion loss which degrades the sensitivity, but it has the benefit of simplicity.

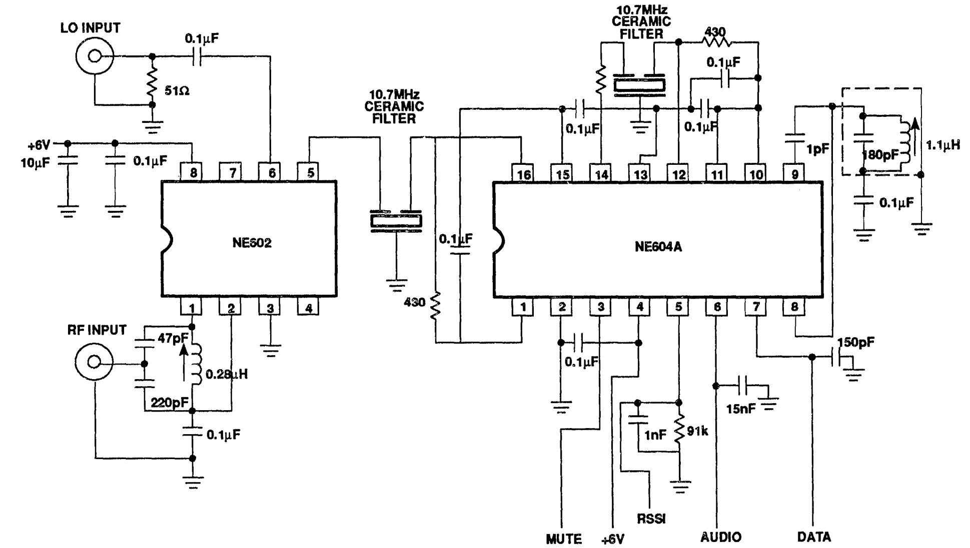
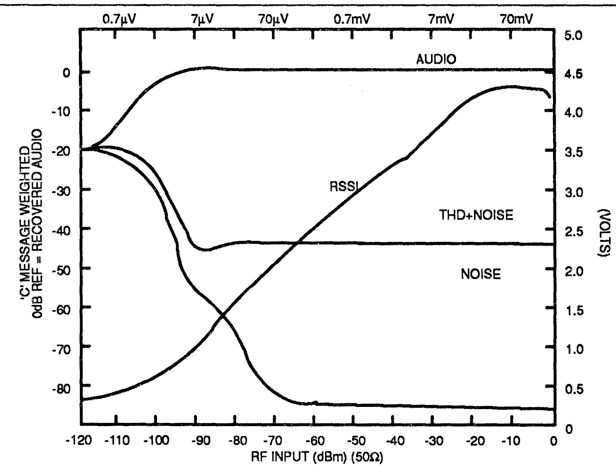


Figure 14. NE602/604A Demonstration Circuit with RF Input of ~100MHz and IF of 10.7MHz ±140kHz

The secondary side of the crystal filter is terminated with a 10.7MHz tuned tank. The capacitor of the tank is tapped to create a transformer with the ratio for 3k:330. With the addition of the 430Ω resistor in parallel with the NE604A 1.6kΩ internal input resistor, the correct component of resistive termination is presented to the crystal filter. The inductor of the tuned load is adjusted off resonance enough to provide the 2pF capacitance needed. (Actual means of adjustment was for best audio during alignment).

If appropriate or necessary for sensitivity, the same type of tuned termination used for the secondary side of the crystal filter can also be used between the NE602 and the filter. If this is desired, the capacitors should be ratioed for 1.5k:3k. Alignment is more complex with tuned termination on both sides of the filter. This approach is demonstrated in the fourth example.

A ceramic filter is used between the first and second limiters. It is directly connected between the output of the first limiter and the input of the second limiter. Ceramic filters act much like ceramic capacitors, so direct connection between two circuit nodes with different DC levels is acceptable. At the input to the second limiter, the impedance is again reduced by the addition of a 430Ω external



- **94.7MHz RF Input**
- **84MHz LO (odBm)**
- **10.7MHz IF**
- **280kHz IF BW**
- **75kHz deviation**

Figure 15. FM Broadcast Receiver (Wide Band)

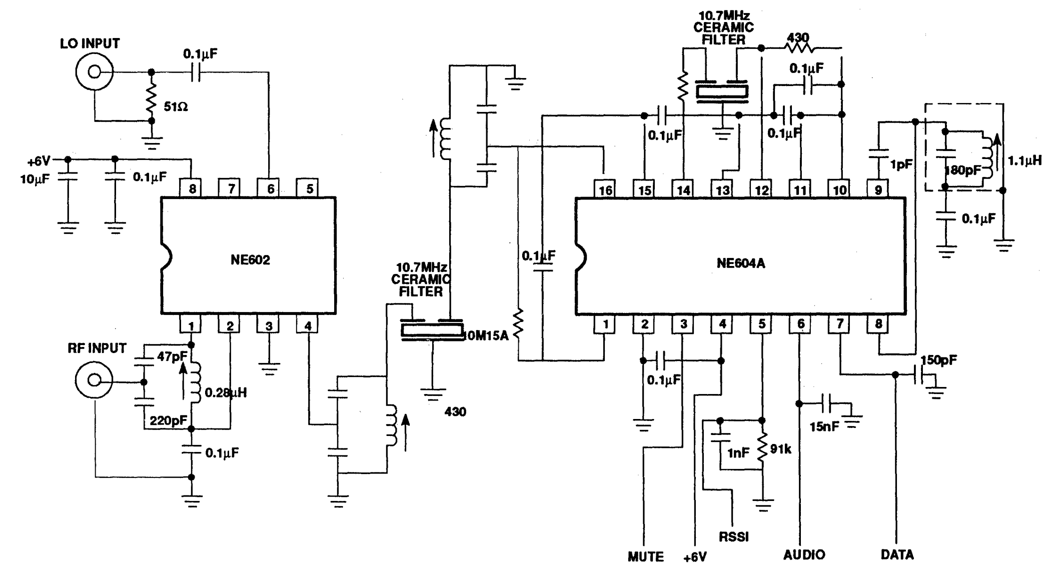
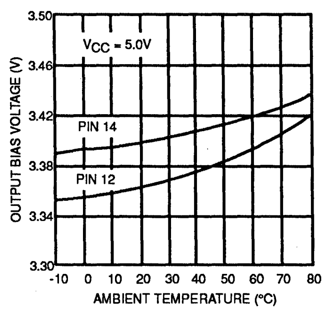


Figure 16. NE602/604A Demonstration Circuit with RF Input of 152.2MHz and IF of 10.7MHz ±7.5kHz

resistor in parallel with the internal 1.6kΩ input load resistor. This presents the 330Ω termination to the ceramic filter which the manufacturers recommend.

On the input side of the ceramic filter, no attempt was made to create a match. The output impedance of the first limiter is nominally 1kΩ. Crystal filters are tremendously sensitive to correct match. Ceramic filters are relatively forgiving. A review of the manufacturers' data shows that the attenuation factor in the passband is affected with improper match, but the degree of change is small and the passband stays centered. Since the principal selectivity for this application is from the crystal filter at the input of the first limiter, the interstage ceramic filter only has to suppress wideband noise. The first filter's passband is right in the center of the ceramic filter passband. (The crystal filter passband is less than 10% of the ceramic filter passband). This passband relationship is illustrated in Figure 10.

After the second limiter, demodulation is accomplished in the quadrature detector. Quadrature criteria is not the topic of this paper, but it is noteworthy that the choice of loaded Q will affect performance. The NE604A is specified at 455kHz using a quadrature capacitor of 10pF and a tuning capacitor of 180pF. (180pF gives a loaded Q of 20 at 455kHz). A careful look at the quadrature equations (Ref 3.) suggests that at 10.7MHz a value of about 1pF should be substituted for the 10pF at 455kHz.



- **152.2MHz RF input**
- **141.5MHz LO (odBm)**
- **10.7MHz IF**
- **15kHz IF BW**
- **7kHz deviation**

Figure 17. VHF Single Conversion (Narrow Band)

The performance of this circuit is presented in Figure 11. The –12dB SINAD (ratio of Signal to Noise And Distortion) was achieved with a 0.6μV input.

EXAMPLE: 90MHZ TO 21.4MHZ NARROWBAND

This second example, like the first, used two frequencies which could represent the intermediate frequencies of a UHF receiver. This circuit can also be applied to VHF single conversion receivers if the sensitivity is appropriate. The circuit is shown in Figure 12.

Most of the fundamentals are the same as explained in the first example. The 21.4MHz crystal filter has a 1.5kΩ/2pF termination requirement so direct connection to the output of the NE602 is possible. With strays there is probably more than 2pF in this circuit, but the performance is good nonetheless. The output of the crystal filter is terminated with a tuned impedance-step-down transformer as in the previous example. Interstage filtering is accomplished with a 1kΩ:330 step-down ratio. (Remember, the output of the first limiter is 1kΩ and a 430Ω resistor has been added to make the second limiter input 330Ω). A DC blocking capacitor is needed from the output of the first limiter. The board was not laid out for an interstage transformer, so an "XACTO" knife was used to make some minor mods. Figure 13 shows the performance. The +12dB SINAD was with 1.6μV input.

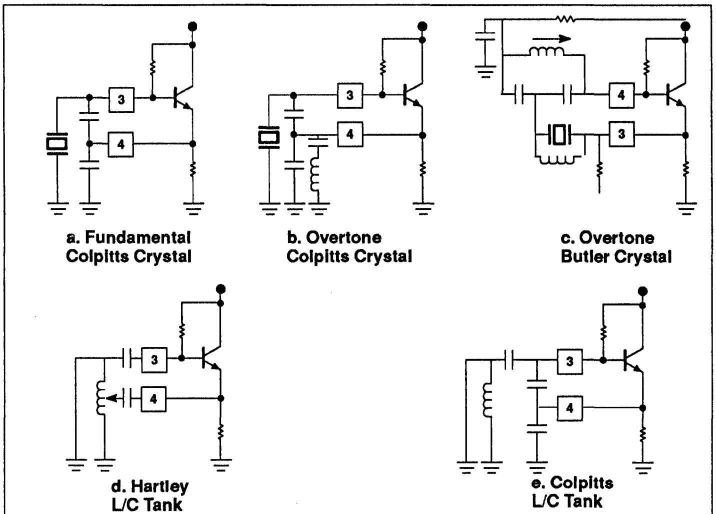


Figure 18. Oscillator Configurations

EXAMPLE: 100MHZ TO 10.7MHZ WIDEBAND

This example represents three possible applications: (1) low cost, sensitive FM broadcast receivers, (2) SCA (Subsidiary Communications Authorization) receivers and (3) data receivers. The circuit schematic is shown in Figure 14. While this example has the greatest diversity of application, it is also the simplest. Two 10.7MHz ceramic filters were used. The first was directly connected to the output of the NE602. The second was directly connected to the output of the first IF limiter. The secondary sides of both filters were terminated with 330Ω as in the two previous examples. While the filter bandpass skew of this simple single conversion receiver might not be tolerable in some applications, to a first order the results are excellent. (Please note that sensitivity is measured at +20dB in this wideband example.) Performance is illustrated in Figure 15. +20dB SINAD was measured with 1.8μV input.

EXAMPLE: 152.2MHZ TO 10.7MHZ NARROWBAND

In this example (see Figure 16) a simple, effective, and relatively sensitive single conversion VHF receiver has been implemented. All of the circuit philosophy has been described in previous examples. In this circuit, tuned-transformed termination was used on the input and output sides of the crystal filter. Performance is shown in Figure 17. The +12dB SINAD sensitivity was 0.9μV.

OSCILLATORS

The NE602 contains an oscillator transistor which can be used to frequencies greater than 200MHz. Some of the possible configurations are shown in Figures 18 and 19.

L/C

When using a synthesizer, the LO must be externally buffered. Perhaps the simplest approach is an emitter follower with the base connected to Pin 7 of the NE602. The use of a dual-gate MOSFET will improve performance because it presents a fairly constant capacitance at its gate and because it has very high reverse isolation.

CRYSTAL

With both of the Colpitts crystal configurations, the load capacitance must be specified. In the overtone mode, this can become a sensitive issue since the capacitance from the emitter to ground is actually the equivalent capacitive reactance of the harmonic selection network. The Butler oscillator uses an overtone crystal specified for series mode operation (no parallel capacitance). It may require an extra inductor (L_0) to null out C_0 of the crystal, but otherwise is fairly easy to implement (see references).

The oscillator transistor is biased with only 220μA. In order to assure oscillation in some configurations, it may be necessary to increase transconductance with an external resistor from the emitter to ground. 10kΩ to 20kΩ are acceptable values. Too small a resistance can upset DC bias (see references).

DATA DEMODULATION

It is possible to change any of the examples from an audio receiver to an amplitude shift keyed (ASK) or frequency shift keyed (FSK) receiver or both with the addition of an external op amp(s) or comparator(s). A simple example is shown in Figure 20. ASK decoding is accomplished by applying a comparator across the received signal strength indicator (RSSI). The RSSI will track IF level down to below the limits of the demodulator (–120dBm RF input in most of the examples). When an in-band signal is above the comparator threshold, the output logic level will change.

FSK demodulation takes advantage of the two audio outputs of the NE604A. Each is a PNP current source type output with 180° phase relationship. With no signal present, the quad tank tuned for the center of the IF passband, and both outputs loaded with the same value of capacitance, if a signal is received which is frequency shifted from the

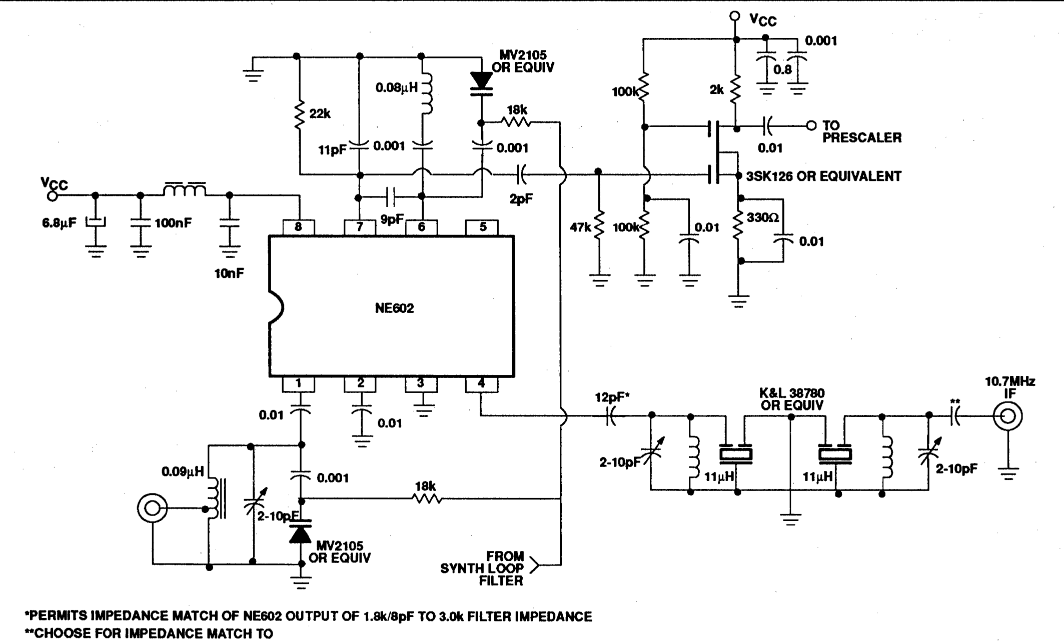


Figure 19. Typical Varactor Tuned Application

IF passband, and both outputs loaded with the same value of capacitance, if a signal is received which is frequency shifted from the IF center, one output voltage will increase and the other will decrease by a corresponding absolute value. Thus, if a comparator is differentially connected across the two outputs, a frequency shift in one direction will drive the comparator output to one supply rail, and a frequency shift in the opposite direction will cause the comparator output to swing to the opposite rail. Using this technique, and L/C filtering for a wide IF bandwidth, NRZ data at rates greater than 4Mb have been processed with the new NE605.

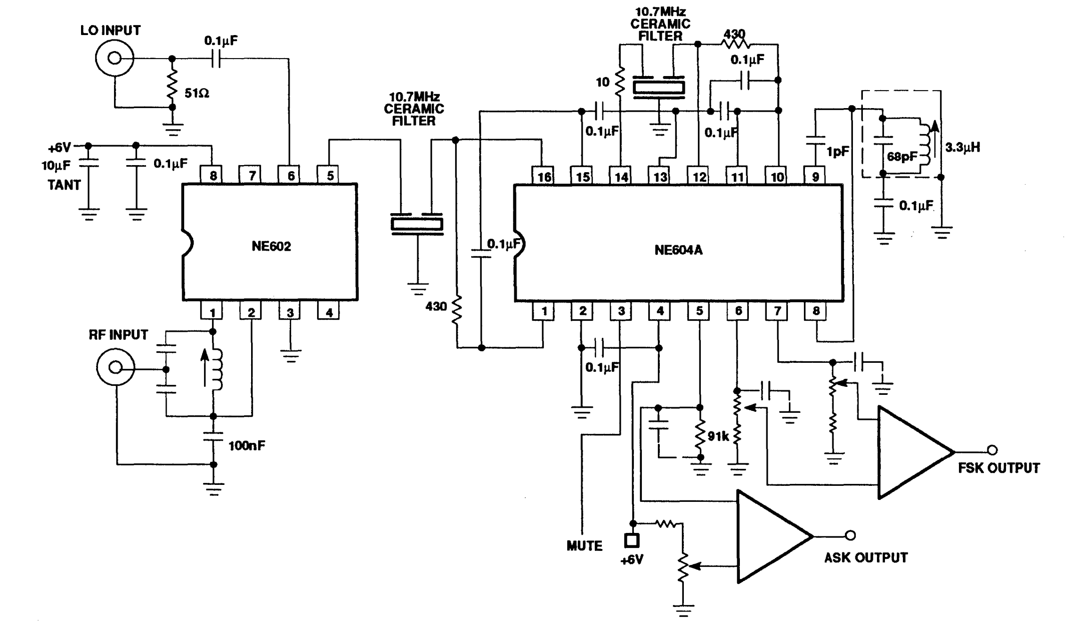


Figure 20. Basic NE602/604A Data Receiver

SUMMARY

The NE602, NE604A and NE605 provide the RF system designer with the opportunity for excellent receiver or IF system sensitivity with very simple circuitry. IFs at 455kHz, 10.7MHz and 21.4MHz with 75 to 90dB gain are possible without special shielding. The flexible configuration of the built-in oscillator of the NE602/605 add to ease of implementation. Either data or audio can be recovered from the NE604A/605 outputs.

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High performance low power mixer FM IF system

NE/SA605

DESCRIPTION

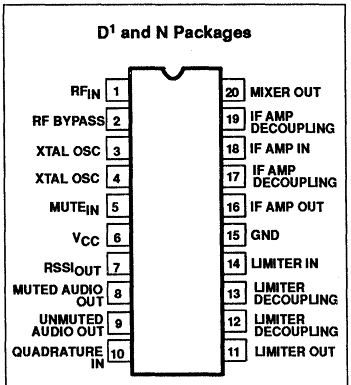
The NE/SA605 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA605 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA605 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package).

The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA605. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA605 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION



NOTE:
1. Large SO (SOL) package only.

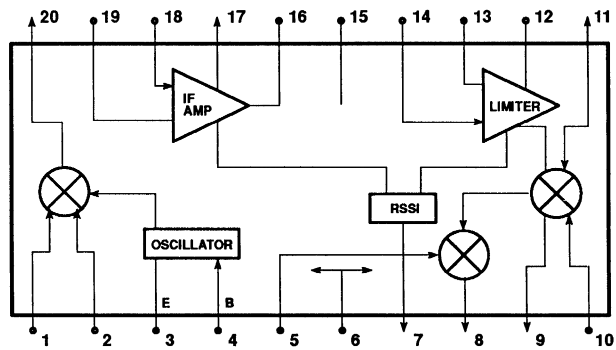
APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE605N
20-Pin Plastic SOL (Surface-mount)	0 to +70°C	NE605D
20-Pin Plastic DIP	-40 to +85°C	SA605N
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA605D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE605	0 to +70	°C
	SA605	-40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	N package	75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.7	6.5	4.55	5.7	6.55	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

Typical reading at T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		480			480		mV
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		1.40	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
RF/IF section (Int LO)									
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450			450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:

1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA605 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

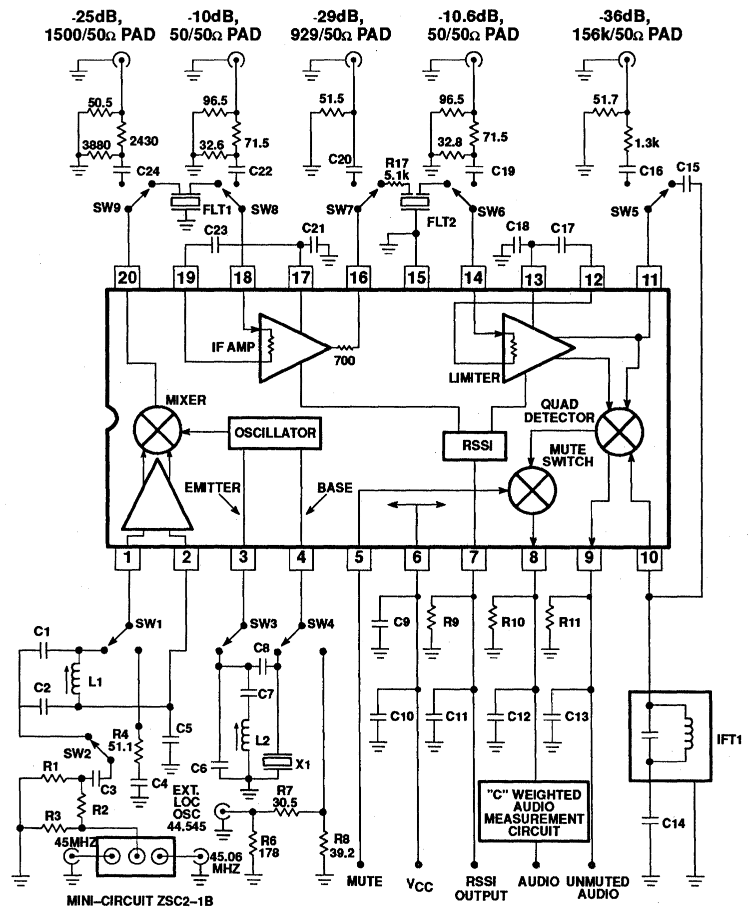
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

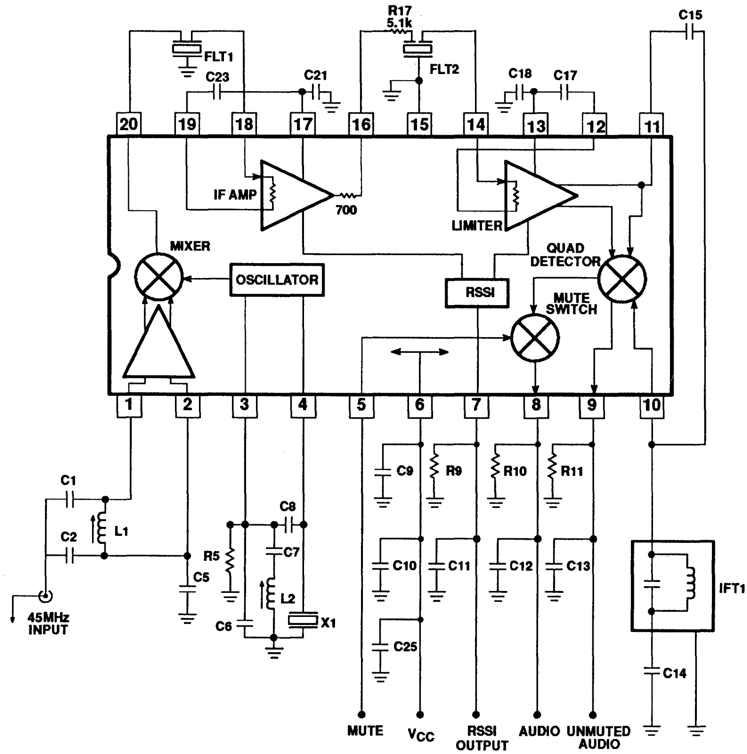
NOTE: dB(v) = 20log V_{OUT}/V_{IN}



Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C9	100nF ±10% Monolithic Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C10	15μF Tantalum (minimum)	L2	3.3μH nominal Toko 292CNS–T1046Z
C11	100nF ±10% Monolithic Ceramic	X1	44.545MHz Crystal ICM4712701
C12	15nF ±10% Ceramic	R9	100k ±1% 1/4W Metal Film
C13	150pF ±2% N1500 Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C14	100nF ±10% Monolithic Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C15	10pF NPO Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic		
C18	100nF ±10% Monolithic Ceramic		

Figure 1. NE/SA605 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C9	100nF ±10% Monolithic Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C10	15μF Tantalum (minimum)	L2	3.3μH nominal Toko 292CNS–T1046Z
C11	100nF ±10% Monolithic Ceramic	X1	44.545MHz Crystal ICM4712701
C12	15nF ±10% Ceramic	R9	100k ±1% 1/4W Metal Film
C13	150pF ±2% N1500 Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C14	100nF ±10% Monolithic Ceramic	R5	Not Used in Application Board (see Note 8)
C15	10pF NPO Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

Figure 2. NE/SA605 45MHz Application Circuit

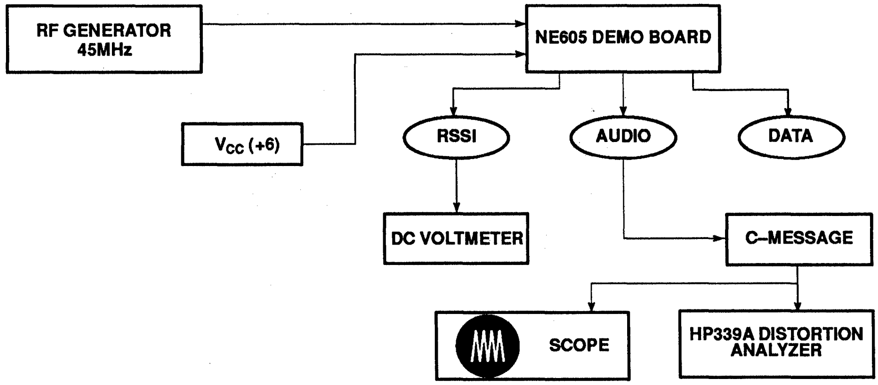


Figure 3. NE/SA605 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22µV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

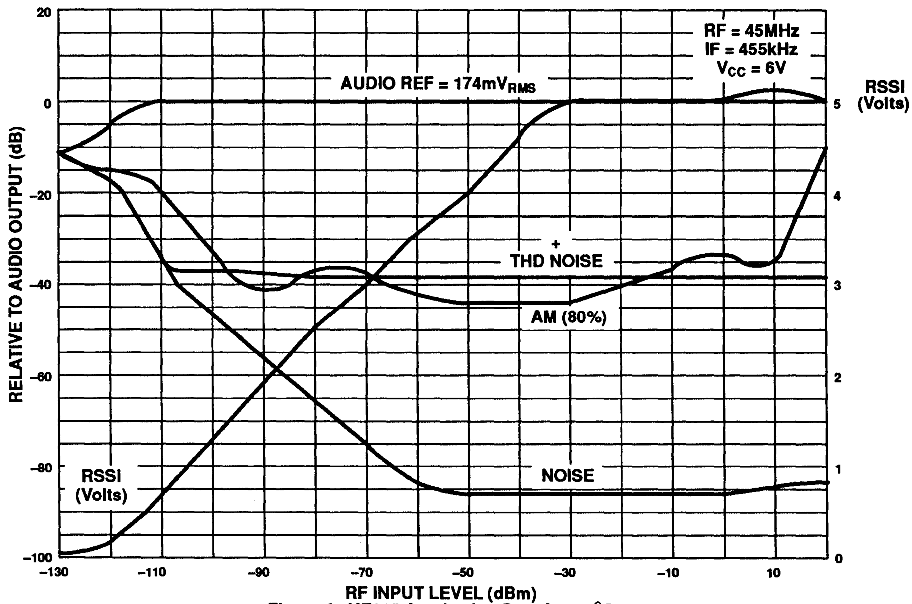


Figure 4. NE605 Application Board at 25°C

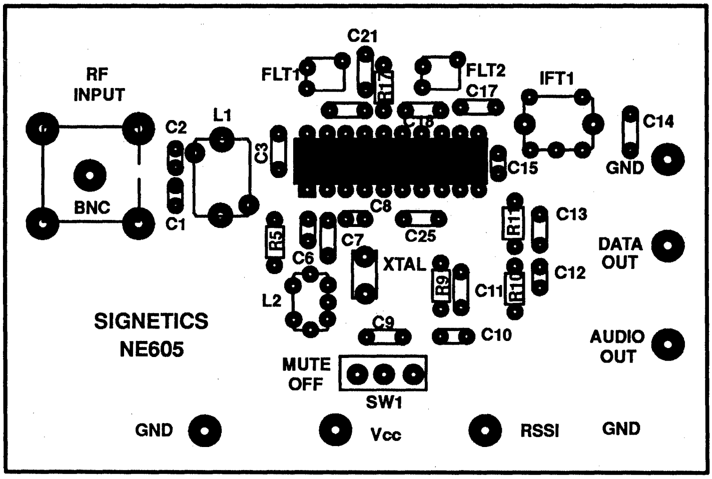
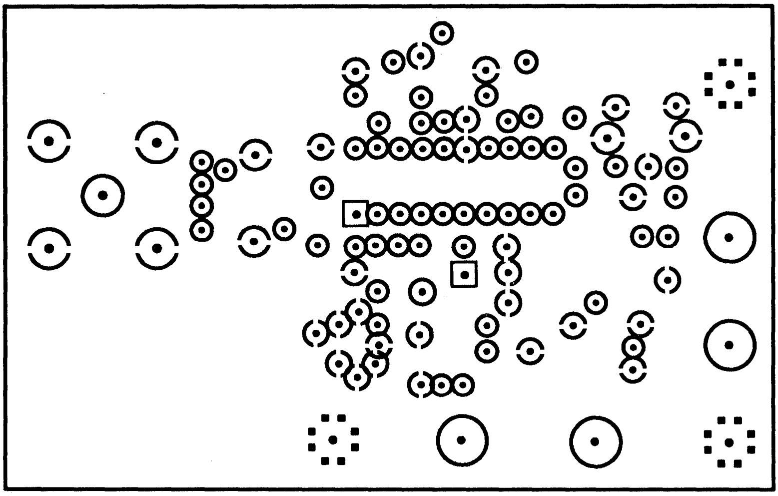
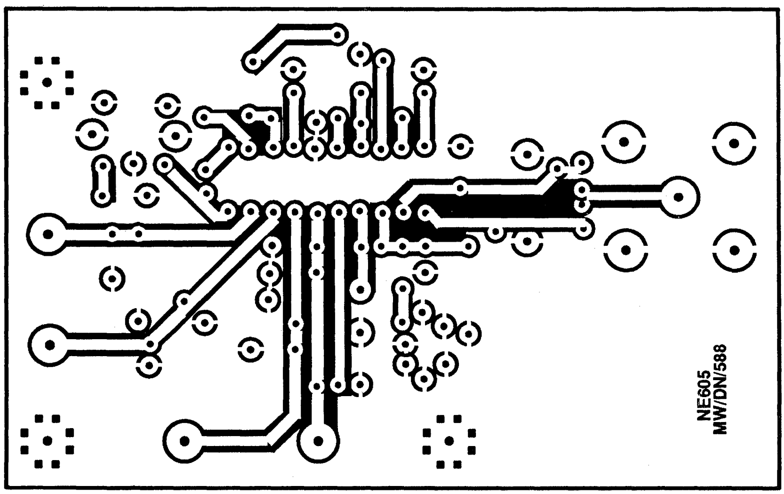


Figure 5. Component Placement for NE605 Application Circuit



TOP VIEW



BOTTOM VIEW

Figure 6. Layout for NE/SA605 Application Board

High performance low power mixer FM IF system in shrink small outline package

NE/SA605SSOP

DESCRIPTION

The NE/SA605 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA605 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA605 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package).

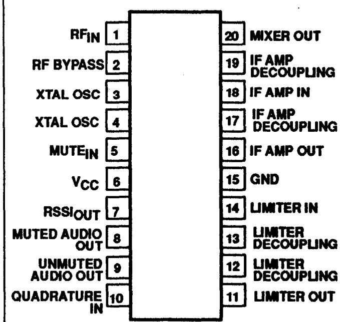
The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA605. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA605 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

SSOP Package



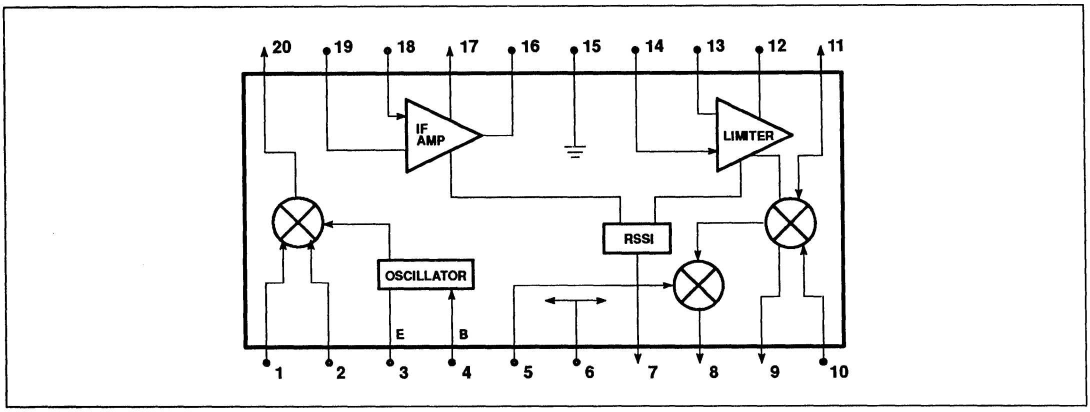
APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SSOP	0 to +70°C	NE605DK
20-Pin Plastic SSOP	-40 to +85°C	SA605DK

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE605	0 to +70	°C
	SA605	-40 to +85	°C
θ_{JA}	Thermal impedance SSOP package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.7	6.5	4.55	5.7	6.55	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		480			480		mV
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		1.40	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
RF/IF section (int LO)									
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450			450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA605 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

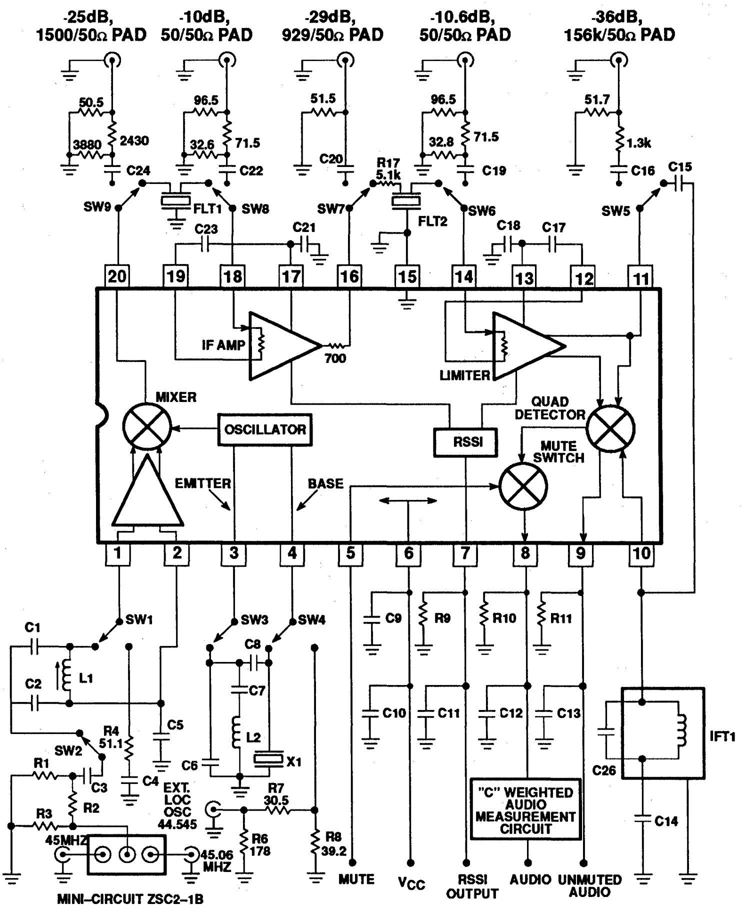
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

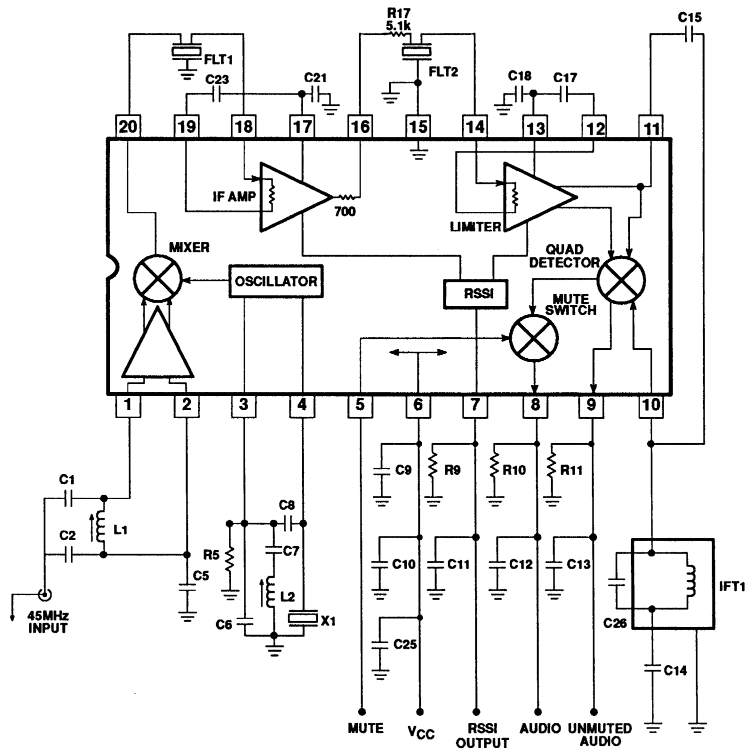
NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



Automatic Test Circuit Component List

C1	47pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	180pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	C26	390pF ±10% Monolithic Ceramic
C7	1nF Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C9	100nF ±10% Monolithic Ceramic	IFT 1	455kHz 270μH TOKO #303LN-1129
C10	15μF Tantalum (minimum)	L1	300nH TOKO #5CB-1055Z
C11	100nF ±10% Monolithic Ceramic	L2	1.2μH Coilcraft #1008CS 122
C12	15nF ±10% Ceramic	X1	44.545MHz Crystal ICM4712701
C13	150pF ±2% N1500 Ceramic	R9	100k ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C15	10pF NPO Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

Figure 1. NE/SA605SSOP 45MHz Test Circuit (Relays as shown)



Application Component List

C1	47pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	180pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	C26	390pF ±10% Monolithic Ceramic
C7	1nF Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C9	100nF ±10% Monolithic Ceramic	IFT 1	455kHz 270μH TOKO #303LN-1129
C10	15μF Tantalum (minimum)	L1	300nH TOKO #5CB-1055Z
C11	100nF ±10% Monolithic Ceramic	L2	1.2μH Coilcraft #1008CS 122
C12	15nF ±10% Ceramic	X1	44.545MHz Crystal ICM4712701
C13	150pF ±2% N1500 Ceramic	R9	100k ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C15	10pF NPO Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

Figure 2. NE/SA605 45MHz Application Circuit

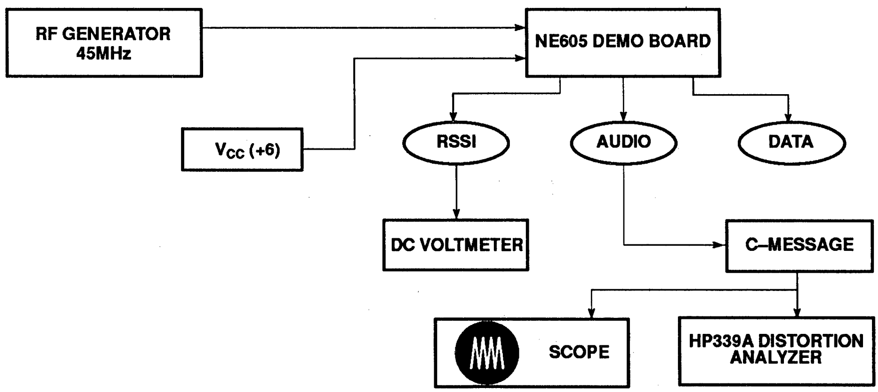


Figure 3. NE/SA605 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22µV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

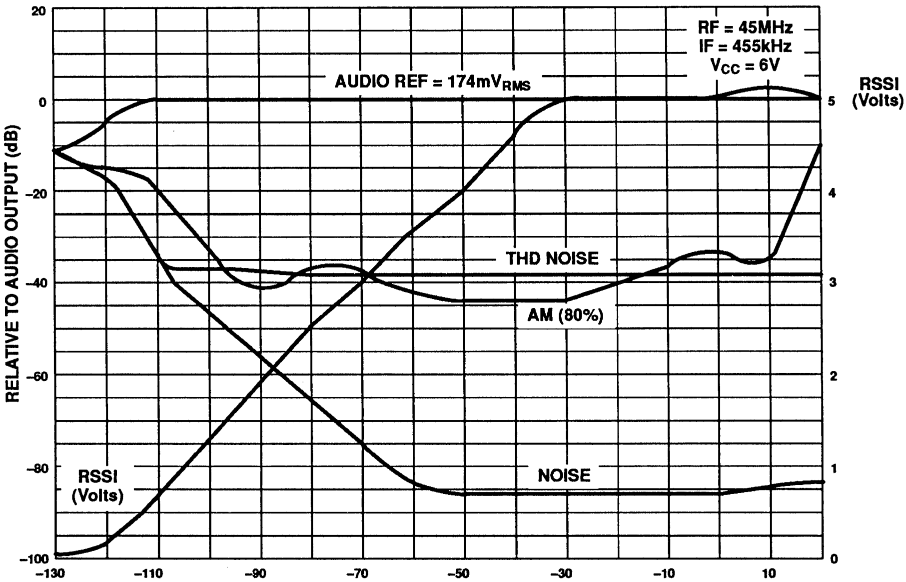
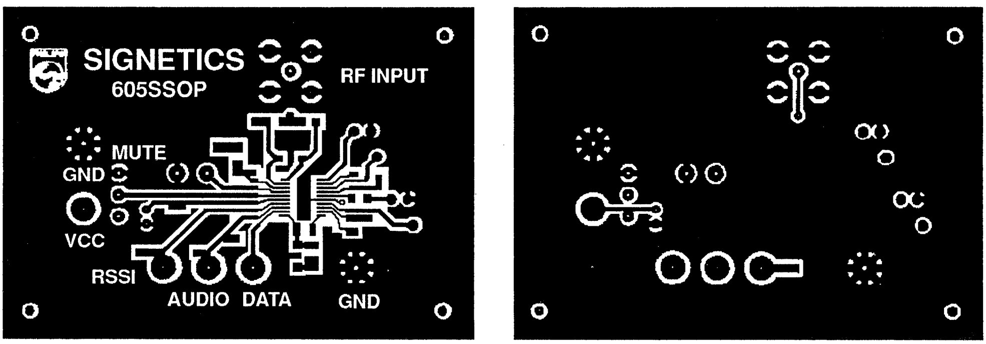


Figure 4. NE605 Application Board at 25°C



TOP VIEW - COMPONENT SIDE

TOP VIEW - SOLDER SIDE

High performance low power mixer FM IF system

NE/SA615

DESCRIPTION

The NE/SA615 is a consumer monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA615 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package).

The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed spcifications. the NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA605. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

FEATURES

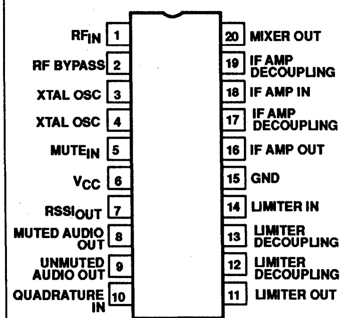
- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs – muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- ESD hardened

APPLICATIONS

- Consumer cellular radio FM IF
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

PIN CONFIGURATION

D[1] and N Packages

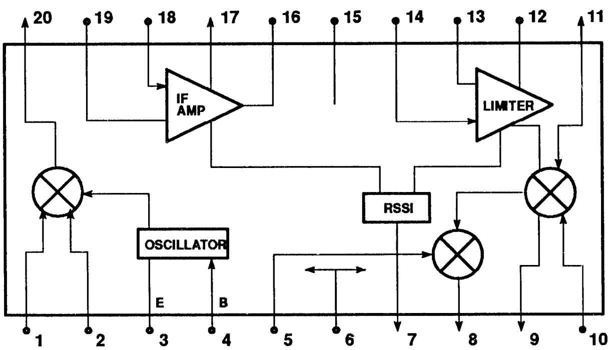


NOTE:
1. Large SO (SOL) package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE615N
20-Pin Plastic SOL (Surface–mount)	0 to +70°C	NE615D
20-Pin Plastic DIP	–40 to +85°C	SA615N
20-Pin Plastic SOL (Surface–mount)	–40 to +85°C	SA615D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE615	0 to +70	°C
	SA615	-40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	N package	75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA615 MIN	TYP	MAX	UNITS
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain			5.7	7.4	mA
	Mute switch input threshold (ON)		1.7			V
	(OFF)				1.0	V

AC ELECTRICAL CHARACTERISTICS

Typical reading at T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz +14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA615 MIN	TYP	MAX	UNITS
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order input intercept point	f1 = 45.00; f2 = 45.06MHz		-12		dBm
	Conversion power gain	Matched 14.5dBV step-up	8.0	13		dB
		50Ω source		-1.7		dB
	RF input resistance	Single-ended input	3.0	4.7		kΩ
	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.50		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz	25	33	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	60	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		530		mV
	SINAD sensitivity	RF level -118dB		12		dB
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	800	mV
		IF level = -68dBm	1.7	2.5	3.3	V
		IF level = -18dBm	3.6	4.8	5.8	V
	RSSI range	R_9 = 100kΩ Pin 16		80		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±2		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		kΩ
			MIN	**TYP**	**MAX**	
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ
RF/IF section (int LO)						
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA615 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for x-tal configurations. Butler oscillators are recommended for x-tal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

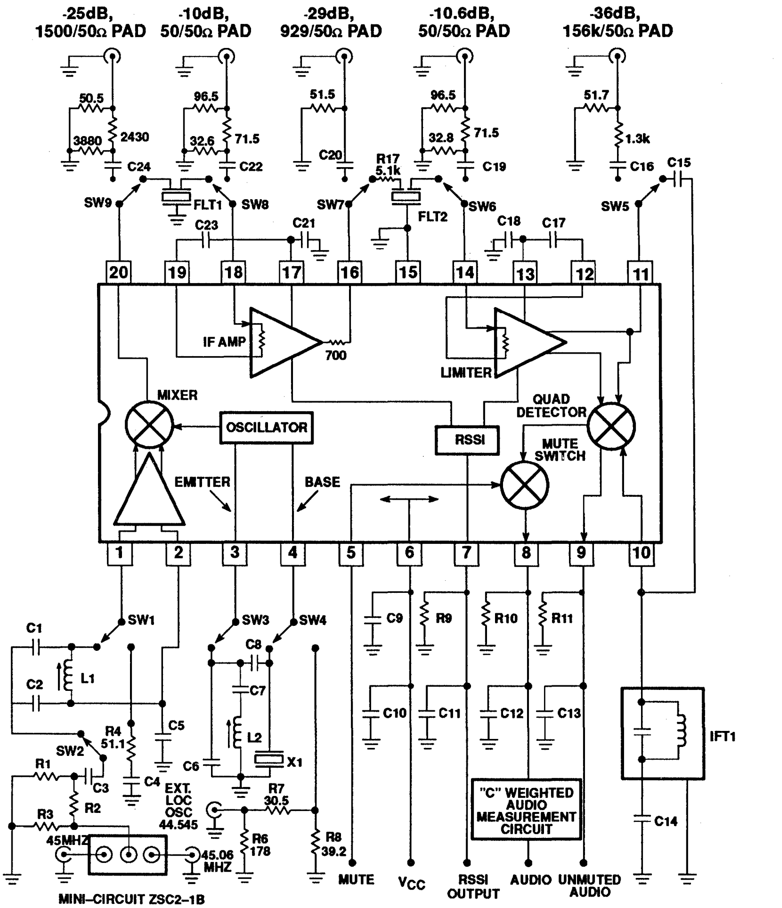
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

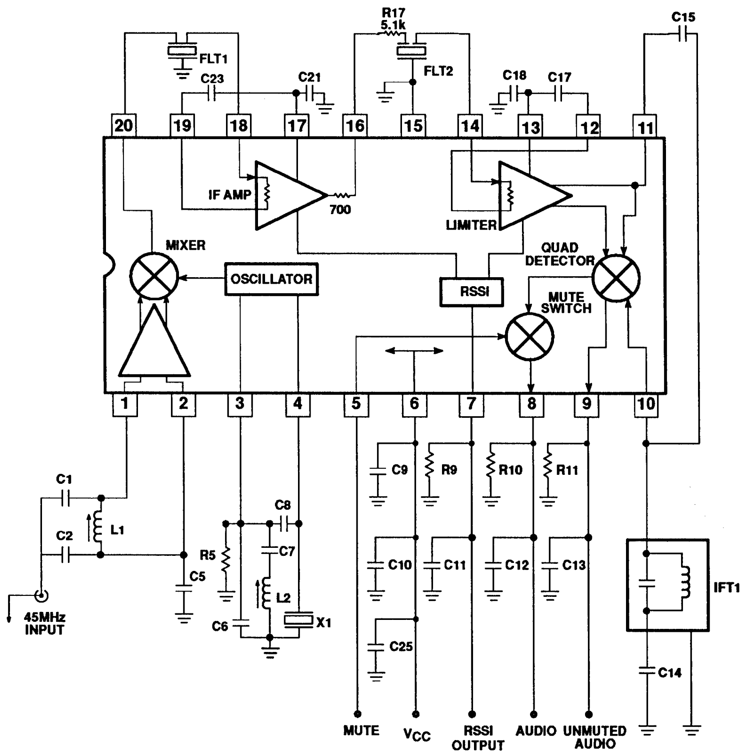
NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C9	100nF ±10% Monolithic Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C10	15μF Tantalum (minimum)	L2	3.3μH nominal Toko 292CNS–T1046Z
C11	100nF ±10% Monolithic Ceramic	X1	44.545MHz Crystal ICM4712701
C12	15nF ±10% Ceramic	R9	100k ±1% 1/4W Metal Film
C13	150pF ±2% N1500 Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C14	100nF ±10% Monolithic Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C15	10pF NPO Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic		
C18	100nF ±10% Monolithic Ceramic		

Figure 1. NE/SA615 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C9	100nF ±10% Monolithic Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C10	15µF Tantalum (minimum)	L2	3.3µH nominal Toko 292CNS–T1046Z
C11	100nF ±10% Monolithic Ceramic		
C12	15nF ±10% Ceramic	X1	44.545MHz Crystal ICM4712701
C13	150pF ±2% N1500 Ceramic	R9	100k ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C15	10pF NPO Ceramic	R5	Not Used in Application Board (see Note 8)
C17	100nF ±10% Monolithic Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic	R11	100k ±1% 1/4W Metal Film (optional)

Figure 2. NE/SA615 45MHz Application Circuit

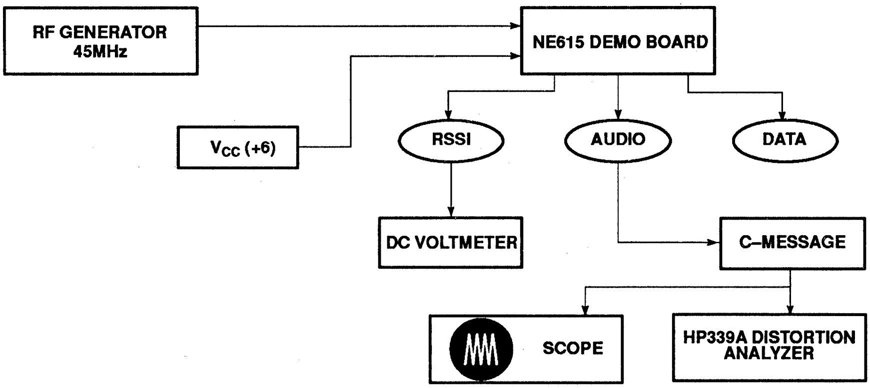


Figure 3. NE/SA615 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or -116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

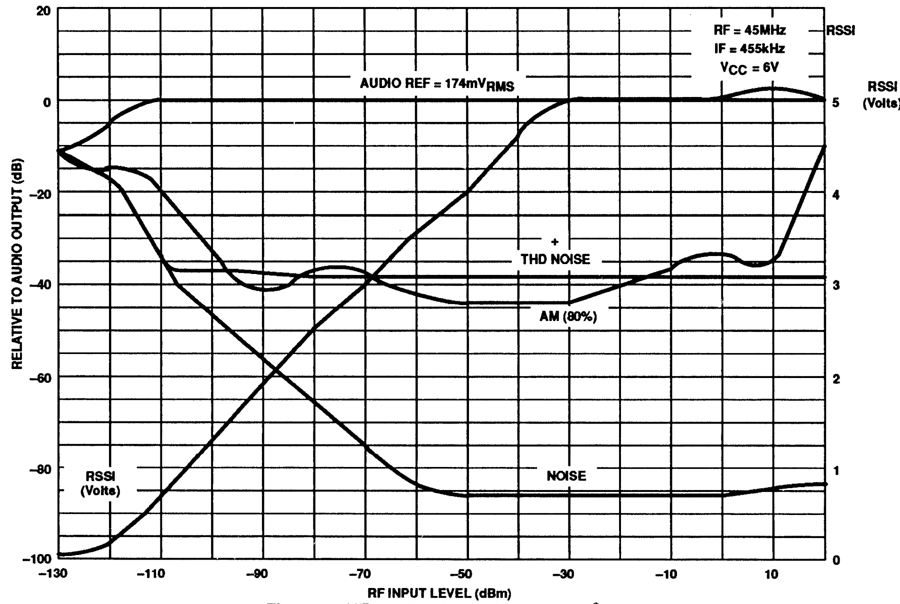


Figure 4. NE615 Application Board at 25°C

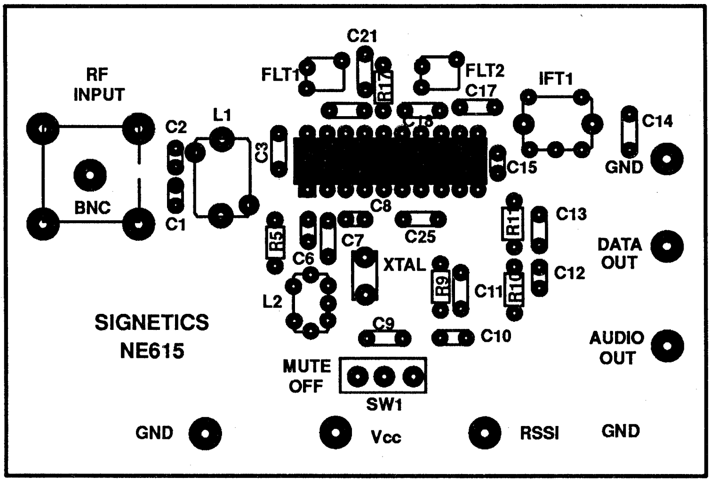


Figure 5. Component Placement for NE615 Application Circuit

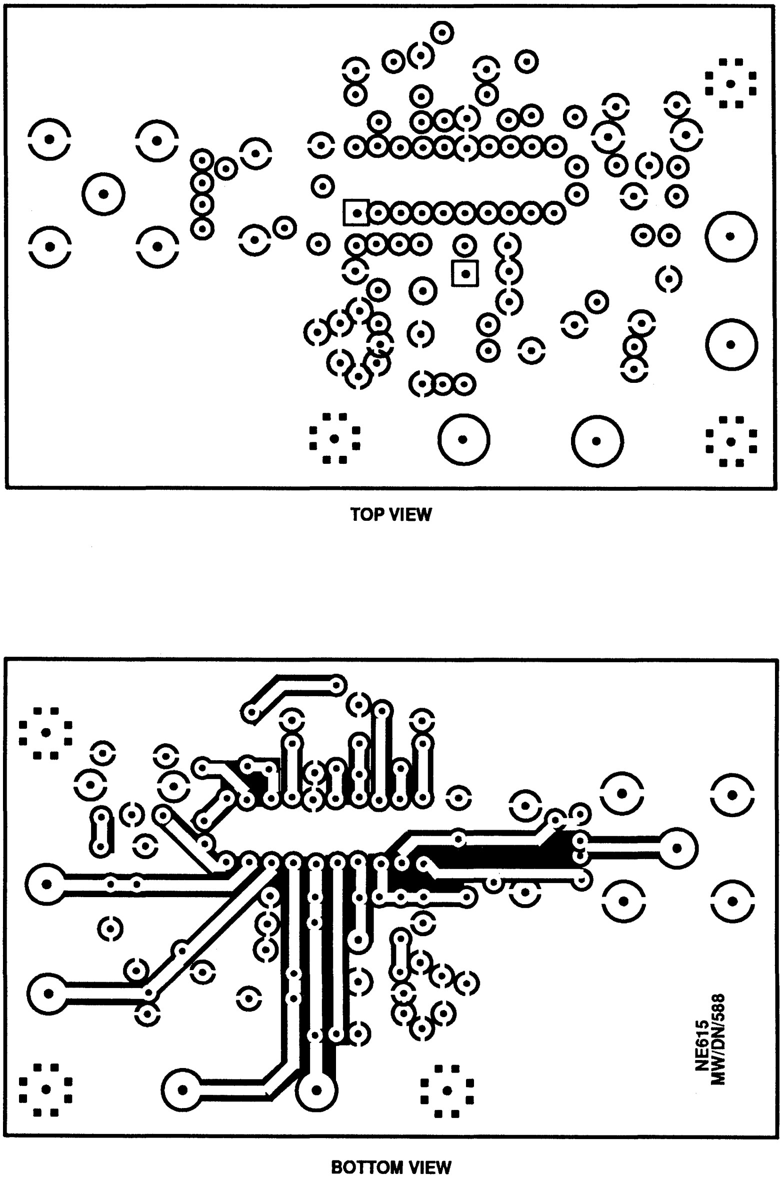


Figure 6. Layout for NE/SA615 Application Board

High performance low power mixer FM IF system in shrink small outline package

NE/SA615 (SSOP)

DESCRIPTION

The NE/SA615 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA615 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA615 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package).

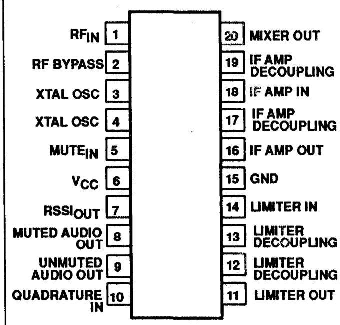
The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA615. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs – muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA615 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

SSOP Package



NOTE:
See back page for package dimensions

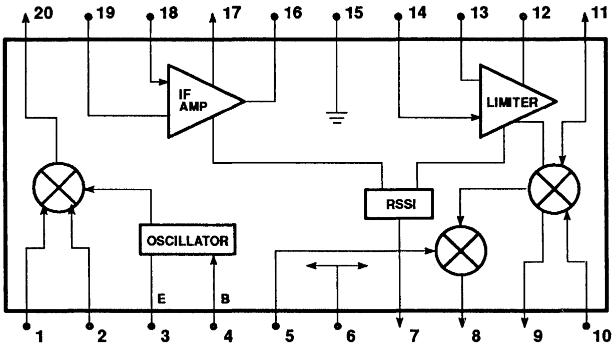
APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SSOP	0 to +70°C	NE615DK
20-Pin Plastic SSOP	–40 to +85°C	SA615DK

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range NE615	0 to +70	°C
	SA615	–40 to +85	°C
θ_{JA}	Thermal impedance SSOP package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA615			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain			5.7	7.4	mA
	Mute switch input threshold (ON)		1.7			V
	(OFF)				1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step–up; IF frequency = 455kHz; R17 = 5.1k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA615 MIN	TYP	MAX	UNITS
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order input intercept point	f1 = 45.00; f2 = 45.06MHz		-12		dBm
	Conversion power gain	Matched 14.5dBV step-up	8.0	13		dB
		50Ω source		-1.7		dB
	RF input resistance	Single-ended input	3.0	4.7		kΩ
	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.50		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz	25	33	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	60	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		530		mV
	SINAD sensitivity	RF level -118dB		12		dB
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	800	mV
		IF level = -68dBm	1.7	2.5	3.3	V
		IF level = -18dBm	3.6	4.8	5.8	V
	RSSI range	R_9 = 100kΩ Pin 16		80		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±2		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ
RF/IF section (int LO)						
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA615 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of −10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

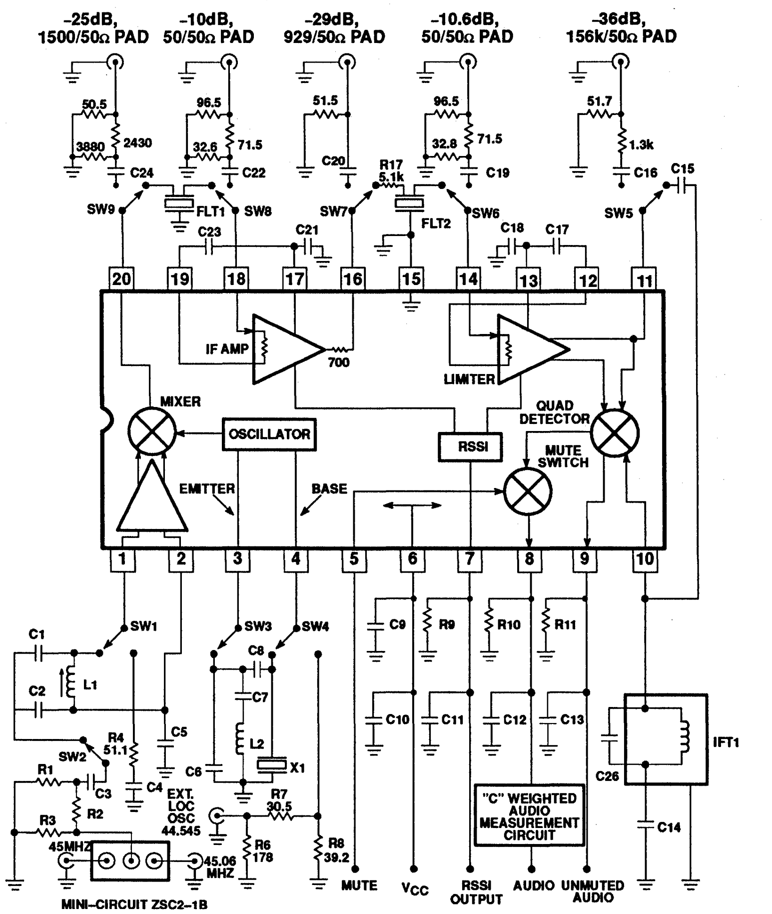
The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

High performance low power mixer FM IF system in shrink small outline package

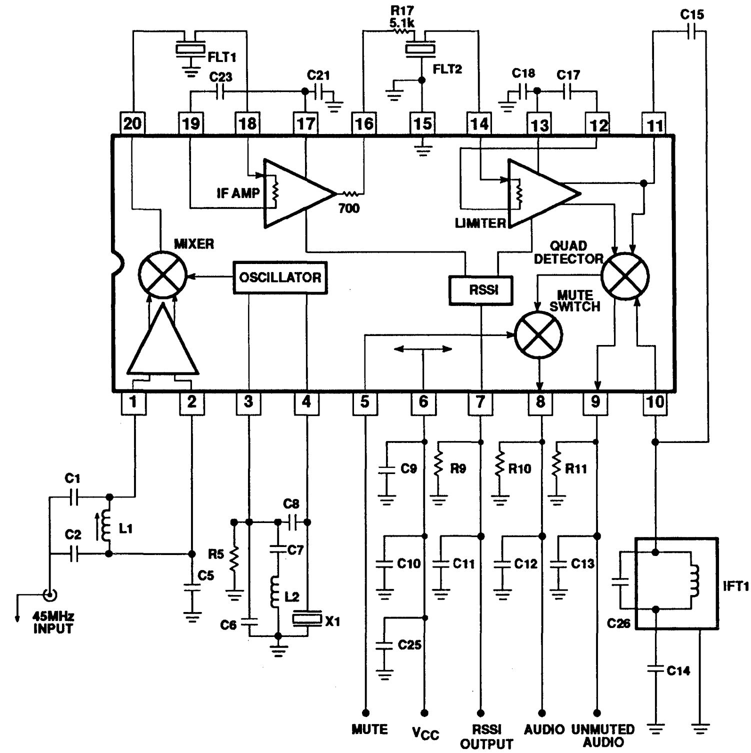
NE/SA615 (SSOP)



Automatic Test Circuit Component List

C1	47pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	180pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	C26	390pF ±10% Monolithic Ceramic
C7	1nF Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C9	100nF ±10% Monolithic Ceramic	IFT 1	455kHz 270μH TOKO #303LN-1129
C10	15μF Tantalum (minimum)	L1	300nH TOKO #5CB-1055Z
C11	100nF ±10% Monolithic Ceramic	L2	1.2μH Coilcraft #1008CS 122
C12	15nF ±10% Ceramic	X1	44.545MHz Crystal ICM4712701
C13	150pF ±2% N1500 Ceramic	R9	100k ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C15	10pF NPO Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

Figure 1. NE/SA615SSOP 45MHz Test Circuit (Relays as shown)



Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270μH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	1.2μH Coilcraft #1008CS 122
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

Figure 2. NE/SA615 45MHz Application Circuit

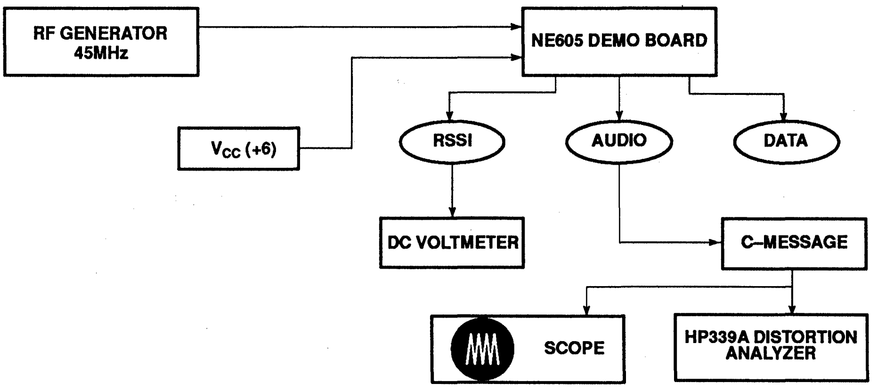


Figure 3. NE/SA615 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22µV or –120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10–15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2–3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

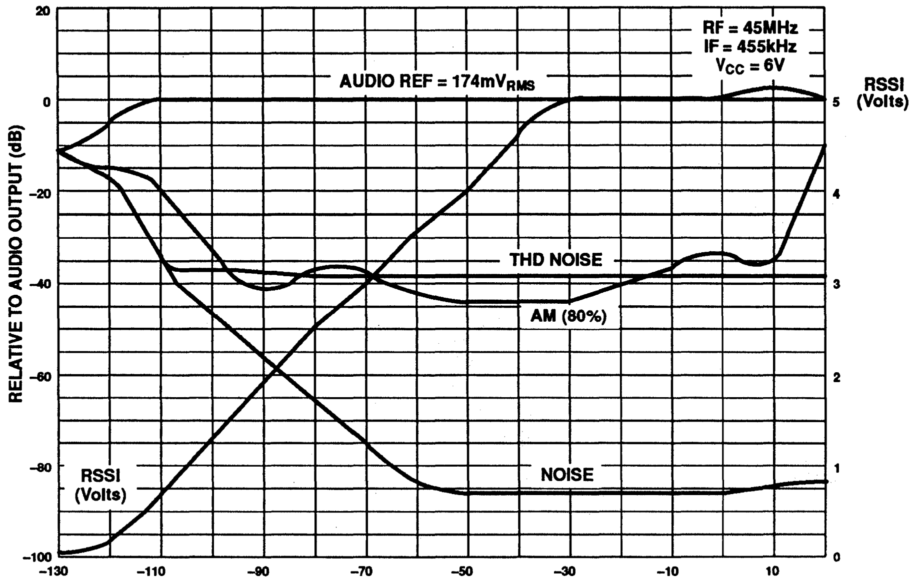
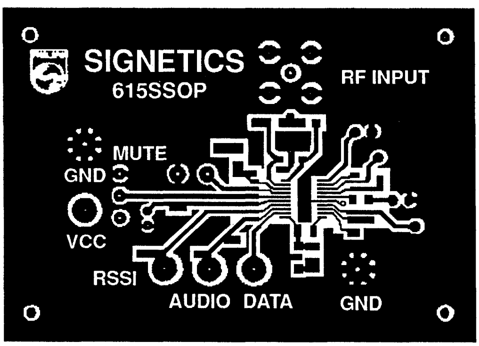
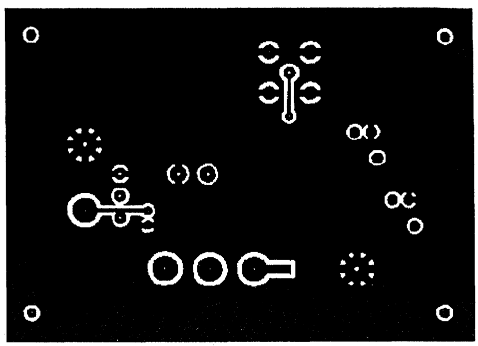


Figure 4. NE615 Application Board at 25°C



TOP VIEW – COMPONENT SIDE



TOP VIEW – SOLDER SIDE

Reviewing key areas when designing with the NE605

AN1994

Author: Alvin K. Wong

INTRODUCTION

This application note addresses key information that is needed when designing with the NE605. Since the NE602 and the NE604 are closely related to the NE605, a brief overview of these chips will be helpful. Additionally, this application note will divide the NE605 into four main blocks where a brief theory of operation, important parameters, specifications, tables and graphs of performance will be given. A question & answer section is included at the end. Below is an outline of this application note:

I. BACKGROUND

History of the NE605

Before the NE605 was made, the NE602 (double-balanced mixer and oscillator) and the NE604 (FM IF system) existed. The combination of these two chips make up a high performance low cost receiver. Soon after the NE605 was created to be a one chip solution, using a newer manufacturing process and design. Since the newer process and design in the NE605 proved to be better in performance and reliability, it was decided to make the NE602 and the NE604 under this new process. The NE602A and the NE604A were created. To assist the cost-conscious customer, Signetics also offered an inexpensive line of the same RF products: the NE612, NE614, and NE615.

Because the newer process and design proved to be better in performance and reliability, the older chips are going to be discontinued. Therefore, only the NE602A, NE612A, NE604A, NE614A, NE605 and NE615 will be available.

Figure 1 shows a brief summary of the RF chips mentioned above. Under the newer process, minor changes were made to improve the performance. A designer, converting from the NE602 to the NE602A, should have no problem with a direct switch. However, switching from the NE604 to the NE604A, might require more attention. This will depend on how good the original design was in the system. In the "Questions & Answers" section, the NE604 and NE604A are discussed in greater detail. This will help the designer, who used the NE604 in their original design, to switch to the "A" version. In general, a direct switch to the NE604A is simple.

Related Application Notes

There have been many application notes written on the NE602 and NE604A. Since the combination of those parts is very similar to the NE605, many of the ideas and applications still apply. In addition, many of the topics discussed here will also apply to the NE602A and NE604A.

Table 1 (see back of app note) shows the application notes available to the designer. They can be found in either the Signetics Linear Data Manual, Volume 1, or the Signetics RF Communications Handbook. Your local PhilipsComponents-Signetics sales representative can provide you with copies of these publications, or you can contact Signetics Publication Services.

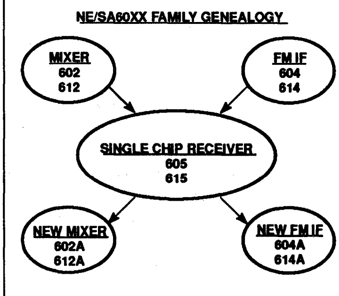


Figure 1. Overview of Selected RF Chips

II. OVERVIEW OF THE NE605

In Figure 2, the NE605 is broken up into four main areas; the mixer section, the IF section, the demodulator section and the output section. The information contained in each of the four areas focuses on important data to assist you with the use of the NE605 in any receiver application.

Mixer Section

There are three areas of interest that should be addressed when working with the mixer section. The RF signal, LO signal and the output. The function of the mixer is to give the sum/difference of the RF and LO frequencies to get an IF frequency out. This mixing of frequencies is done by a Gilbert Cell four quadrant multiplier. The Gilbert Cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell.

The RF input impedance of the mixer plays a vital role in determining the values of the matching network. Figure 3 shows the RF input impedance over a range of frequency. From this information, it can be determined that matching 50Ω at 45MHz requires matching to a 4.5kΩ resistor in parallel with a 2.5pF capacitor. An equivalent model can be seen in Figure 4 with its component values given for selected frequencies. Since there are many questions from the designer on how to match the RF input, an example is given below.

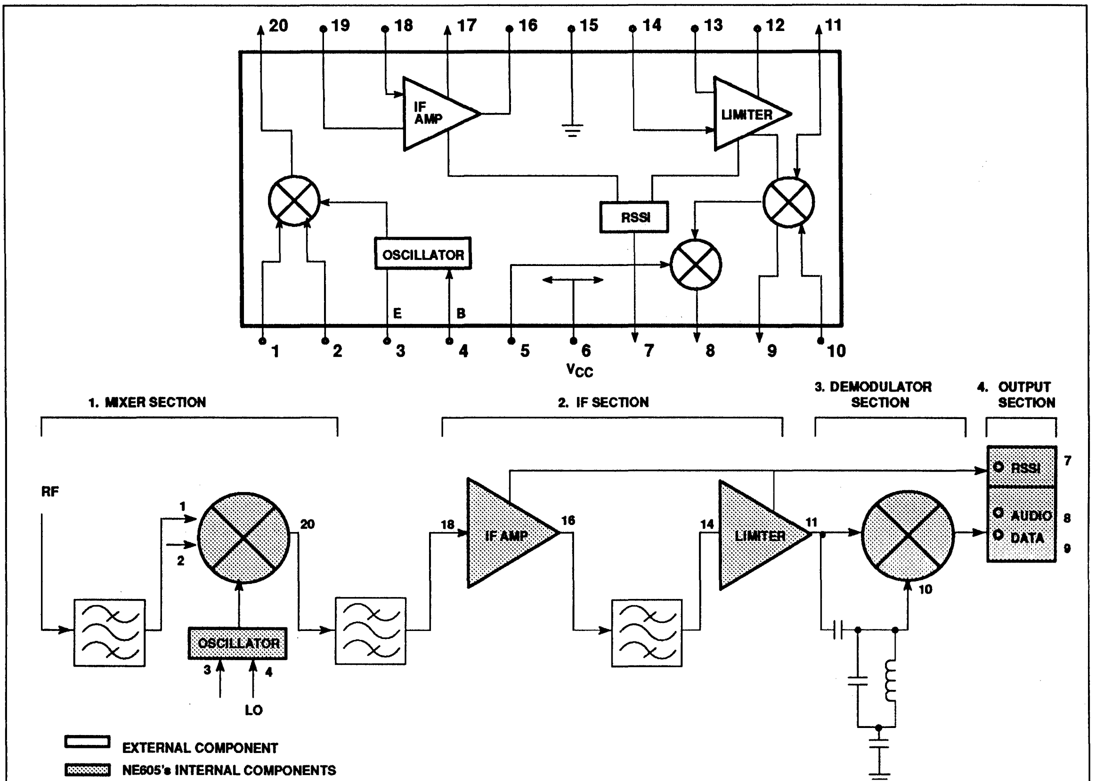


Figure 2. NE605 Broken Down Into Four Areas

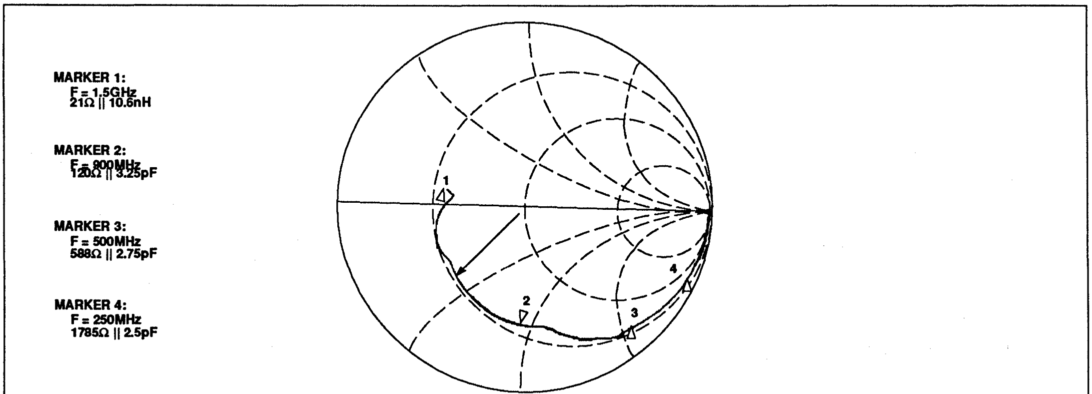


Figure 3. Smith Chart of NE605's RF Input Impedance (Pin 1 or 2)

RF Section of Mixer

The mixer has two RF input pins (Pin 1 and 2), allowing the user to choose between a balanced or unbalanced RF matching network. Table 2 (see back of app note) shows the advantages and disadvantages for either type of matching. Obviously, the better the matching network, the better the sensitivity of the receiver.

Reviewing key areas when designing with the NE605

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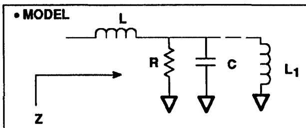
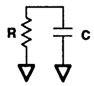


• INDUCTOR L_1 CAN BE NEGLECTED UNTIL THE FREQUENCY APPROACHES 1GHz (NEGLECT 'C')

•TWO ELEMENT MODEL



FREQ	R || C
10MHz	5kΩ || 2.5pF
50MHz	4651Ω || 2.5pF
100MHz	3100Ω || 2.5pF
250MHz	1785kΩ || 2.5pF
500MHz	588Ω || 2.75pF
750MHz	1751Ω || 3.12pF
900MHz	120Ω || 3.2pF
1.1GHz	48Ω || 3.4pF
1.56GHz	21Ω || 10.6nH

Figure 4. Equivalent Model of RF Input Impedance

Example: Using a tapped-C network, match a 50Ω source to the RF input of the NE605 at 45MHz. (refer to Figure 5)

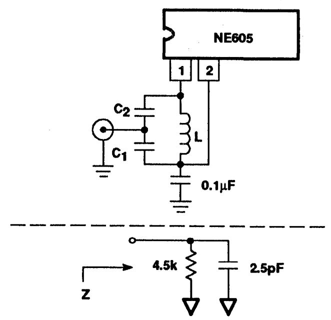


Figure 5. Tapped-C Network

Step 1. Choose an inductor value and its "Q"
$L = 0.22\mu H$ $Q_P = 50$ (specified by manufacturer)

Step 2. Find the reactance of the inductor
$X_P = 2\pi FL$
$= 2\pi (45MHz)(0.22\mu H)$
$\therefore X_P = 62.2\Omega$

Step 3. Then,
$R_P = Q_P X_P$
$=(50)(62.2)$
$\therefore R_P = 3.11k\Omega$ (the inductance resistance)

Step 4. $Q = R_{TOTAL}/X_P$
$= (R_S' \,//\, R_L \,//\, R_P) / X_P$
where $R_S' = R_L$
$= 4.5k \,//\, 4.5k \,//\, 3.11k / 62.2$
$= 21.39$
$\therefore Q \cong 21$ (the Q of the matching network)

where:
R_S = source resistance;
R_L = load resistance;
R_S' = what the source resistance should look like to match R_L;
R_P = inductance resistance

Step 5. $$\frac{C1}{C2} = \sqrt{\frac{R_S'}{R_S}} - 1 = 8.6$$

Step 6. $$C_T = \frac{1}{X_P\,\omega} = \frac{1}{(62.2)\ 2\pi\ 45MHz}$$
$$= 56.86pF$$

Step 7.
$$\text{using } C_T = \frac{C1\,C2}{C1 + C2}$$
where $C_T = 56.86pF$, $\frac{C1}{C2} = 8.6$
$$C_T = \frac{C1}{\frac{C1}{C2} + 1}$$
$$\therefore C_1 = C_T\left(\frac{C1}{C2} + 1\right)$$
$$\text{and } C_2 = \frac{C1}{8.6}$$
thus...
$C1 = 539pF$
$C2 = 64pF$
$L = 0.22\mu H$ *(value started with)*

Step 8. Frequency check
$$\omega = \frac{1}{\sqrt{LC}}$$
$$2\pi F = \frac{1}{\sqrt{LC}}$$
$F = 45MHz$ *(... so far so good)*

Step 9. Taking care of the 2.5pF capacitor that is present at the RF input at 45MHz
$$\frac{C2_A}{C1_A} = \frac{64pF}{540pF} \qquad \text{Eq. 1.}$$
$$C_{TN} = \frac{C1_A C2_A}{C1_A + C2_A} \qquad \text{Eq. 2.}$$
where $C_{TN} = C_T - 2.5pF$
(recall value of C_T from Step 6.)

Making use of Equations 1 and 2, the new values of C1 and C2 are:
$C1_A = 524pF$
$C2_A = 60.6pF$

[NOTE: At this frequency the 2.5pF capacitor could probably be ignored since its value at 45MHz has little effect on C1 and C2.]

Step 10. Checking the bandwidth
$$Q = \frac{F}{BW}$$
$$BW = F_U - F_L$$
BW = bandwidth
F_U = upper 3dB frequency
F_L = lower 3dB frequency

Using the above formulas results in
$F_U = 46MHz$
$F_L = 44MHz$
$BW = 2MHz$

The above shows the calculations for a single-ended match to the NE605. For a balanced matching network, a transformer can be used. The same type of calculations will still apply once the input impedance of the NE605 is converted to the primary side of the transformer (see Figure 6). But before we transform the input impedance to the primary side, we must first find the new input impedance of the NE605 for a balanced configuration. Because we have a balanced input, the 4.5kΩ transforms to 9kΩ (4.5k + 4.5k = 9k) while the capacitor changes from 2.5pF to 1.3pF (2.5pF in series with 2.5pF is 1.3pF). Notice that the resistor values double while the capacitor values are halved. Now the 9kΩ resistor in parallel with the 1.3pF capacitor must be transformed to the primary side of the transformer (see Figure 6).

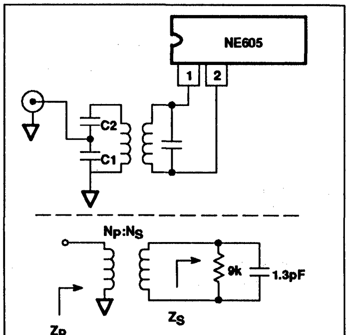


Figure 6. Using a Transformer to Achieve a Balanced Match

Procedure:

Step 1. $$\frac{Z_P}{Z_S} = \left(\frac{N_P}{N_S}\right)^2$$

where:
Z_P = impedance of primary side
Z_S = impedance of secondary side
N_P = number of turns on primary side
N_S = number of turns on secondary side

Step 2. Recall,

$Z_S = R \parallel X_C$

$Z_S = 9k \parallel j2.7k$

where

$R = 9k$

$$X_C = \frac{1}{2\pi FC} = 2.7k \text{ at } F = 45MHz$$

Step 3. Assume 1:N turns ratio for the transformer

$$Z_P = \frac{Z_S}{N^2} = 2.25k \parallel j\,680$$

(assuming N = 2)

Step 4.

$$\therefore C = \frac{1}{2\pi\ FX_C} = 5.2pF$$

R = 2.25k

(these are the new values to match using the formulas in tapped-C)

Step 5. Because the transformer has a magnetization inductance L_M, (inductance presented by the transformer), we can eliminate the inductor used in the previous example and tune the tapped-C network with the inductance presented by the transformer.

Lets assume $L_M = 0.22\mu H$ (Q=50)

Therefore

C1 = 381pF

C2 = 66.8pF

F_U = 46.7MHz

F_L = 43.3MHz

BW = 3.4MHz

taking the input capacitor into consideration

C1 = 347pF

C2 = 61pF

L = 0.22µH (Q=50)

Because of leakage inductance, the transformer is far from ideal. All of these leakages affect the secondary voltage under load which will seem like the indicated turns ratio is wrong. The above calculations show one method of impedance matching. The values calculated for C1 and C2 do not take into account board parasitic capacitance, and are, therefore, only theoretical values. There are many ways to configure and calculate matching networks. One alternative is a tapped-L configuration. But the ratio of the tapped-C network is easier to implement than ordering a special inductor. The calculations of these networks can be done on the Smith Chart. Furthermore, there are many computer programs available which will help match the circuit for the designer.

Local Oscillator Section of Mixer

The NE605 provides an NPN transistor for the local oscillator where only external components like capacitors, inductors, or resistors need to be added to achieve the LO frequency. The oscillator's transistor base and emitter (Pins 4 and 3 respectively) are available to be configured in Colpitts, Butler or varactor controlled LC forms. Referring to Figure 7, the collector is internally connected directly to V_{CC}, while the emitter is connected through a 25kΩ resistor to ground. Base bias is also internally supplied through an 18kΩ resistor. A buffer/divider reduces the oscillator level by a factor of three before it is applied across the upper tree of the Gilbert Cell. The divider de-sensitizes the mixer to oscillator level variations with temperature and voltage. A typical value for the LO input impedance is approximately 10kΩ.

The highest LO frequency that can be achieved is approximately 300MHz with a 200mV_{RMS} signal on the base (Pin 4). Although it is possible to exceed the 300MHz LO frequency for the on-board oscillator, it is not really practical because the signal level drops too low for the Gilbert Cell. If an application requires a higher LO frequency, an external oscillator can be used with its 200mV_{RMS} signal injected at Pin 4 through a DC blocking capacitor. Table 3 (see back of app note) can be used as a guideline to determine which configuration is best for the required LO frequency.

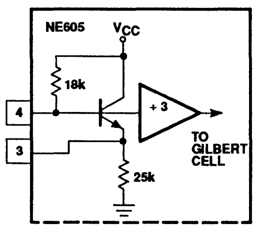


Figure 7. On-board NPN Transistor for Local Oscillator

Because the Colpitts configuration is for parallel resonance mode, it is important to know, when ordering crystals, that the load capacitance of the NE605 is 10pF. However, for the Butler configuration, the load capacitance is unimportant since the crystal will be in the series mode. Figure 8 shows the different types of LO configurations used with NE605.

If a person decides to use the Colpitts configuration in their design, they will probably find that most crystal manufacturers have their own set of standards of load capacitance. And in most cases, they are unwilling to build a special test jig for an individual's needs. If this occurs, the designer should tell them to go ahead with the design. But, the designer should also be ready to accept the crystal's frequency to be off by 200–300Hz from the specified frequency. Then a test jig provided by the designer and a 2nd iteration will solve the problem.

Output of Mixer

Once the RF and LO inputs have been properly connected, the output of the mixer supplies the IF frequency. Knowing that the mixer's output has an impedance of 1.5kΩ, matching to an IF filter should be trivial.

Choosing the Appropriate IF Frequency

Some of the standard IF frequencies used in industry are 455kHz, 10.7MHz and 21.4MHz. Selection of other IF frequencies is possible. However, this approach could be expensive because the filter manufacturer will probably have to build the odd IF filter from scratch.

There are several advantages and disadvantages in choosing a low or high IF frequency. Choosing a low IF frequency like 455kHz can provide good stability, high sensitivity and gain. Unfortunately, it can also present a problem with the image frequency (assuming single conversion). To improve the image rejection problem, a higher IF frequency can be used. However, sensitivity is decreased and the gain of the IF section must be reduced to prevent oscillations.

If the design requires a low IF frequency and good image rejection, it is best to use the double conversion method. This method allows the best of both worlds. Additionally, it is much easier to work with a lower IF frequency because the layout will not be as critical and will be more forgiving in production. The only drawback to this method is that it will require another mixer and LO. But, a transistor can be used for the first mixer stage (which is an inexpensive approach) and the NE605 can be used for the second mixer stage. The NE602A can also be used for the first conversion stage if the transistor approach does not meet the design requirements.

If the design requires a high IF frequency, good layout and RF techniques must be exercised. If the layout is sound and instability still occurs, refer to the "RSSI output" section which suggests solutions to these types of problems.

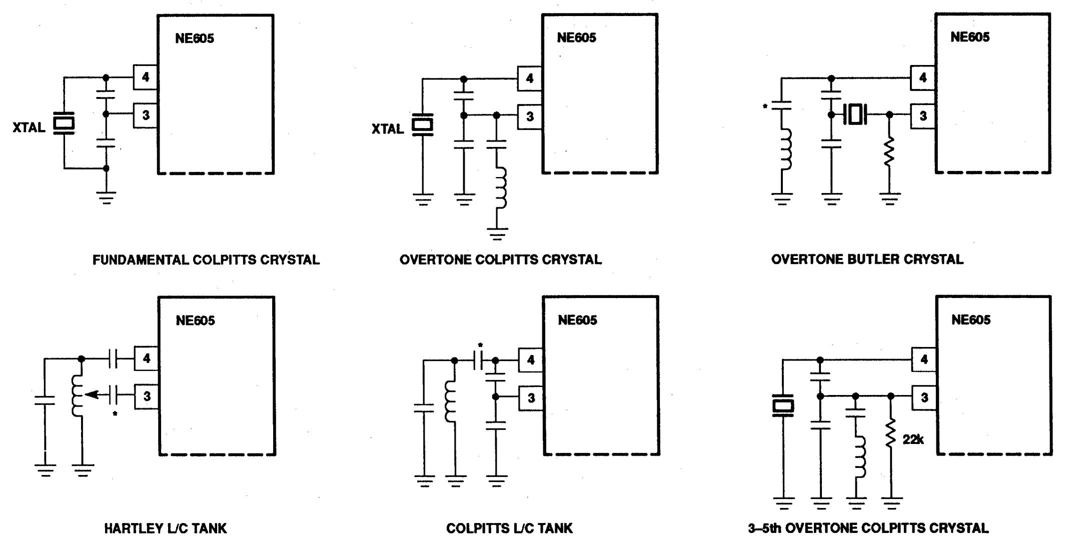
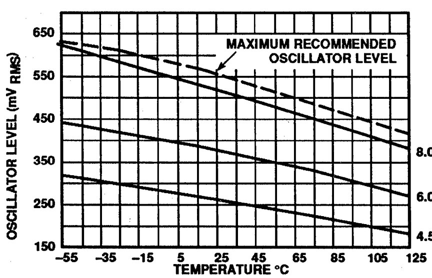


Figure 8. Oscillator Configurations



C_{BE} = 5.6pF

Figure 9. NE605 Application Oscillator Level

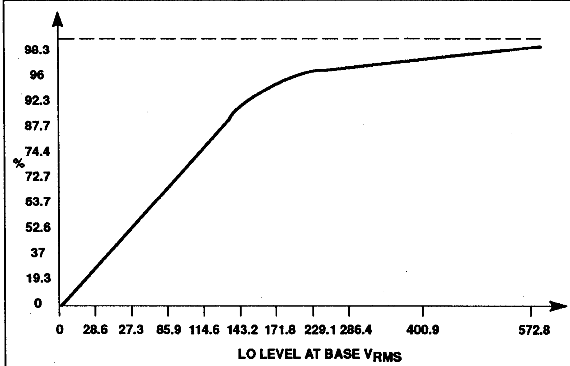


Figure 10. Mixer Efficiency vs Normalized LO Level

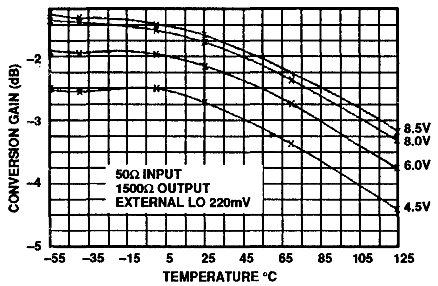


Figure 11. 50Ω Conversion Gain

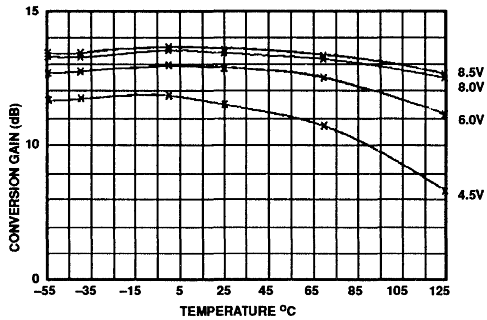


Figure 12. Single-Ended Matched Input Conversion Gain (50Ω to 1.5kΩ, 14.5dB Matching Step-up Network)

Performance Graphs of Mixer

Fig.	Description
9	Oscillator Levels vs. Temperature with Different Supply Voltages for the 44.545MHz Crystal Colpitts Applications
10	LO Efficiency vs. Normalized Peak Level at the Base of the Oscillator Transistor
11	50Ω Conversion Gain vs. Temperature with Different Supply Voltages Using an External LO
12	Mixer Matched Input Conversion Gain vs. Temperature with Different Supply Voltages
13	IF Output Power vs. RF Input Level (3rd-order Intercept Point) 1st mixer = diode mxr, 2nd mixer = 605 mxr
14	NE605 and Diode Mixer Test Set Up
15	NE605 LO Power Requirements vs. Diode Mixer
16	NE605 Conversion Gain vs. Diode Mixer
17	Comparing Intercept Points with Different Types of Mixers

Another issue to consider when determining an IF frequency is the modulation. For example, a narrowband FM signal (30kHz IF bandwidth) can be done with an IF of 455kHz. But for a wideband FM signal (200kHz IF bandwidth), a higher IF is required, such as 10.7MHz or 21.4MHz.

IF Section

The IF section consists of an IF amplifier and IF limiter. With the amplifier and limiter working together, 100dB of gain with a 25MHz bandwidth can be achieved (see Figure 18). The linearity of the RSSI output is directly affected by the IF section and will be discussed in more detail later in this application note.

IF Amplifier

The IF amplifier is made up of two differential amplifiers with 40dB of gain and a small signal bandwidth of 41MHz (when driven by a 50Ω source). The output is a low impedance emitter follower with an output resistance of about 230Ω, and an internal series build out of 700Ω to give a total of 930Ω. One can expect a 6dB loss in each amplifier's input since both of the differential amplifiers are single-ended.

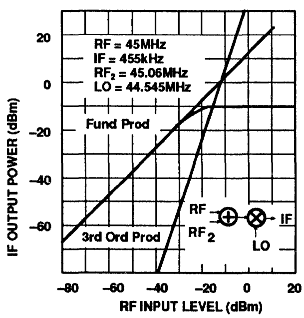


Figure 13. Third-Order Intercept and Compression

The basic function of the IF amp is to boost the IF signal and to help handle impulse noise. The IF amp will not provide good limiting over a wide range of input signals, which is why the IF limiter is needed.

IF Limiter

The IF limiter is made up of three differential amplifiers with a gain of 63dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. The IF limiter's output resistance is about 260Ω with no internal build-out. The limiter's output signal (Pin 9 onNE604A, Pin 11 on NE605) will vary from a good approximation of a square wave at lower IF frequencies like 455kHz, to a distorted sinusoid at higher IF frequencies, like 21.4MHz.

The basic function of the IF limiter is to apply a tremendous amount of gain to the IF frequency such that the top and bottom of the waveform are clipped. This helps in reducing AM and noise presented upon reception.

Function of IF Section

The main function of the IF section is to clean up the IF frequency from noise and amplitude modulation (AM) that might occur upon reception of the RF signal. If the IF section has too much gain, then one could run into instability problems. This is where crucial layout and insertion loss can help (also addressed later in this paper).

Important Parameters for the IF Section

Limiting: The audio output level of an FM receiver normally does not change with the RF level due to the limiting action. But as the RF signal level continues to decrease, the limiter will eventually run out of gain and the audio level will finally start to drop. The point where the IF section runs out of gain and the audio level decreases by 3dB with the RF input is referred to as the –3dB limiting point.

In the application test circuit, with a 5.1kΩ interstage resistor, audio suppression is dominated by noise capture down to about the –120dBm RF level at which point the phase detector efficiency begins to drop (see Interstage Loss section below).

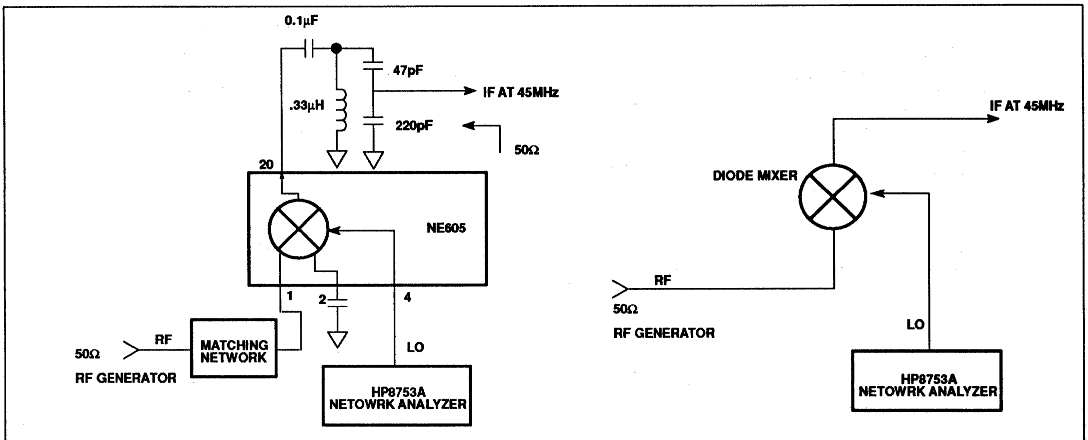


Figure 14. Test Circuits for NE605 Mixer vs Diode Mixer

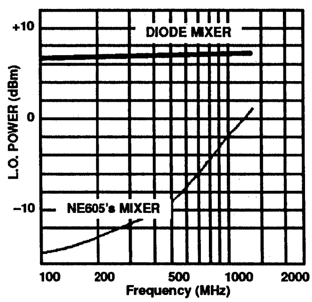


Figure 15. LO Power Requirements (Matched Input)

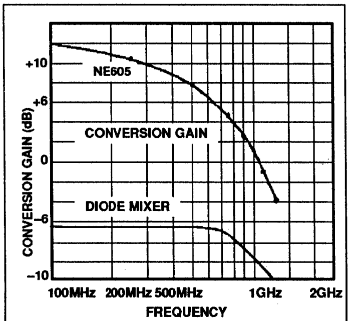


Figure 16. NE605 Conversion Gain vs. Diode Mixer

The audio drop that occurs is a function of two types of limiting. The first type is as follows: As the input signal drops below a level which is sufficient to keep the phase detector compressed, the efficiency of the detector drops, resulting in premature audio attenuation. We will call this "gain limiting". The second type of limiting occurs when there is sufficient amount of gain without destabilizing regeneration (i.e. keeping the phase detector fully limited), the audio level will eventually become suppressed as the noise captures the receiver. We will call this "limiting due to noise capture".

Figure 19 shows the 3dB drop in audio at about $0.26\mu V_{RMS}$, with a –118.7dBm/50Ω RF level for the NE605. Note that the level has not improved by the 11dB gain supplied by the mixer/filter since noise capture is expected to slightly dominate here.

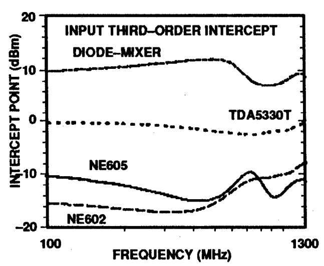


Figure 17. Comparing Different Types of Mixers

AM rejection: The AM rejection provided by the NE605/604A is extremely good even for 80% modulation indices as depicted in Figures 20a through 20d. This performance results from the 370mV peak signal levels set at the input of each IF amplifier and limiter stage. For this level of compression at the inputs, even better performance could be expected except that finite AM to PM conversion coefficients limit ultimate performance for high level inputs as indicated in Figure 20b.

Low level AM rejection performance degrades as each stage comes out of limiting. In particular as the quadrature phase detector input drops below 100mV peak, all limiting will be lost and AM modulation will be present at the input of the quad detector (See Figure 20d).

AM to PM conversion: Although AM rejection should continue to improve above –95dBm IF inputs, higher order effects, lumped under the term AM to PM conversion, limit the application rejection to about 40dB. In fact this value is proportional to the maximum frequency deviation. That is lower deviations producing lower audio outputs result directly in lower AM rejection. This is consistent with the fact that the interfering audio signal produced by the AM/PM conversion process is independent of deviation within the IF bandwidth and depends to a first estimate on the level of AM modulation present. As an example reducing the maximum frequency deviation to 4kHz from 8kHz, will result in 34dB AM rejection. If the AM modulation is reduced from 80% to 40%, the AM rejection for higher level IFs will go back to 40dB as expected. AM to PM conversion is also not a function of the quad tank Q, since an increase in Q increases both the audio and spurious AM to PM converted signal equally.

As seen above, these relationships and the measured results on the application board

(Figure 36) can be used to estimate high level IF AM rejection. For higher frequency IFs (such as 21.4MHz), the limiter's output will start to deviate from a true square wave due to lack of bandwidth. This causes additional AM rejection degradation.

Interstage Loss: Figure 21 plots the simulated IF RSSI magnitude response for various interstage attenuation. The optimum interstage loss is 12dB. This has been chosen to allow the use of various types of filters, without upsetting the RSSI's linearity. In most cases, the filter insertion loss is less than 12dB from point A to point B. Therefore, some additional loss must be introduced externally. The easiest and simplest way is to use an external resistor in series with the internal build out resistor (Pin 14 in the NE604A, Pin 16 in the NE605). Unfortunately, this method mismatches the filter which might be important depending on the design. To achieve the 12dB insertion loss and good matching to the filter, an L-pad configuration can be used. Figure 22 shows the different set-ups.

Below is an example on how to calculate the resistors values for both Figures 22a and 22b.

Step 1.

$$X_{dB} = 20 log \frac{\sqrt{(960 + R_{EXT})\ R_{FLT}}}{960 + R_{EXT} + R_{FLT}} - FIL\ [dB]$$

(just solve for R_{EXT})

where
X = the insertions loss wanted in dB
R_{EXT} = the external resistor
R_{FLT} = the filter's input impedance
FIL = insertion loss of filter in dB

2. For our application board
X=12dB
R_{FLT} = 1.5k
FIL = 3dB
Therefore, using the above eq. gives
R_{EXT} = 5.1K

$$R_{EXT} = \left| 960 - \frac{R_{FLT}}{2 \times 10^{\left(\frac{-X_{dB}}{20}\right)}} \right|$$

Step 2.

$$R_{SHUNT} = \frac{R_{FLT}}{1 - 2 \times 10^{\left(\frac{-X_{dB}}{20}\right)}}$$

3. In this case, lets assume: FIL = −2dB therefore, X_{dB} = +10, R_{FLT} = 1.5k. The results are: R_{EXT} = 1.41k, R_{SHUNT} = 4.08k

IF noise figure

The IF noise figure of the receiver may be expected to provide at best a 7.7dB noise figure in a 1.5kΩ environment from about 25kHz to 100MHz. From a 25Ω source the noise figure can be expected to degrade to about 15.4db.

Performance Graphs of IF Section

Fig.	Description
24	IF Amp Gain vs. Temperature with Various Supply Voltages
25	IF Limiter Gain vs. Temperature with Various Supply Voltages
26	IF Amp 20MHz Response vs. Temperature
27	IF Limiter 20MHz Response vs. Temperature

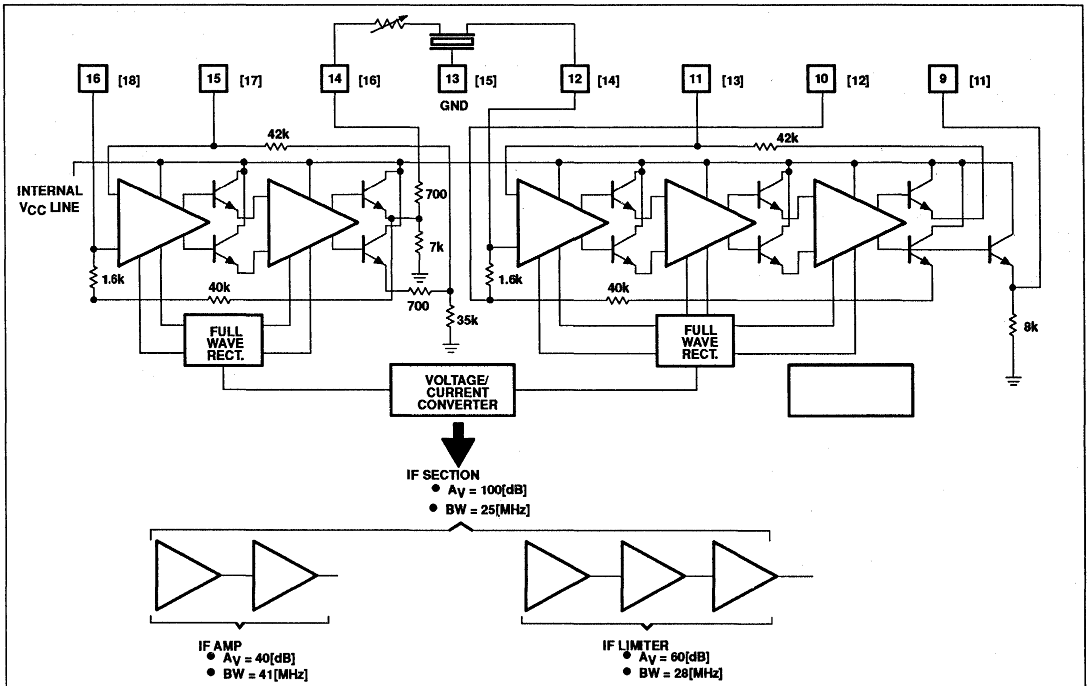


Figure 18. IF Section of NE604A [NE605]

Demodulator Section

Once the signal leaves the IF limiter, it must be demodulated so that the baseband signal can be separated from the IF signal. This is accomplished by the quadrature detector. The detector is made up of a phase comparator (internal to theNE605) and a quadrature tank (external to theNE605).

The phase comparator is a multiplier cell, similar to that of a mixer stage. Instead of mixing two different frequencies, it compares the phases of two signals of the same frequency. Because the phase comparator needs two input signals to extract the information, the IF limiter has a balanced output. One of the outputs is directly connected to the input of the phase comparator. The other signal from the limiter's output (Pin 11) is phase shifted 90 degrees (through external components) and frequency selected by the quadrature tank. This signal is then connected to the other input of the phase comparator (Pin 10 of the NE605). The signal coming out of the quadrature detector (phase detector) is then low-passed filtered to get the baseband signal. A mathematical derivation of this can be seen in the NE604A data sheet.

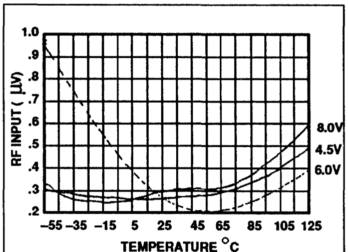


Figure 19. NE605 Application Board, –3dB Limiting (Drop in Audio)

The quadrature tank plays an important role in the quality of the baseband signal. It determines the distortion and the audio output amplitude. If the "Q" is high for the quadrature tank, the audio level will be high, but the distortion will also be high. If the "Q" is low, the distortion will be low, but the audio level will become low. One can conclude that there is a trade-off.

Output Section

The output section contains an RSSI, audio, and data (unmuted audio) outputs which can be found on Pins 7, 8, and 9, respectively, on the NE605. However, amplitude shift keying (ASK), frequency shift keying (FSK), and a squelch control can be implemented from these pins. Information on ASK and FSK can be found in Philips Components-Signetics application note AN1993.

Although the squelch control can be implemented by using the RSSI output, it is not a good practice. A better way of implementing squelch control is by comparing the bandpassed audio signal to high frequency colored FM noise signal from the unmuted audio. When no baseband signal is present, the noise coming out of the unmuted audio output will be stronger, due to the nature of FM noise. Therefore, the output of the external comparator will go high (connected to Pin 5 of the NE605) which will mute the audio output. When a baseband signal is present, the bandpassed audio level will dominate and the audio output will now unmute the audio.

Audio and Unmuted Audio (Data)

The audio and unmuted audio outputs (Pin 8 and 9, respectively, on the NE605) will be discussed in this section because they are basically the same. The only difference between them is that the unmuted audio output is always "on" while the audio output can either be turned "on" or "off". The unmuted audio output (data out) is for signaling tones in systems such as cellular radio. This allows the tones to be processed by the system but remain silent to the user. Since these tones contain information for cellular operation, the unmuted audio output can also be referred to as the "data" output. Applying 5V to Pin 5 on the NE605 mutes the audio on Pin 8 (connecting ground on Pin 5 unmutes it).

Both of these outputs are PNP current-to-voltage converters with a 55kΩ nominal internal load. The nominal frequency response of the audio and data outputs are 300kHz. However, this response can be increased with the addition of an external resistor (<58kΩ) from the output pins to ground. This will affect the time constant and lower the audio's output amplitude. This technique can be applied to SCA receivers and data transceivers (as mentioned in the NE604A data sheet).

RSSI Output

RSSI (Received Signal Strength Indicator) determines how well the received signal is being captured by providing a voltage level on its output. The higher the voltage, the stronger the signal.

The RSSI output is a current-to-voltage converter, similar to the audio outputs. However, a 91kΩ external resistor is needed to get an output characteristic of 0.5V for every 20dB change in the input amplitude.

As mentioned earlier, the linearity of the RSSI curve depends on the 12dB insertion loss between the IF amplifier and IF limiter. The reason the RSSI output is dependent on the IF section is because of the V/I converters. The amount of current in this section is monitored to produce the RSSI output signal. Thus, the IF amplifier's rectifier is internally calibrated under the assumption that the loss is 12dB.

Because unfiltered signals at the limiter inputs, spurious products, or regenerated signals will affect the RSSI curve, the RSSI is a good indicator in determining the stability of the board's layout. With no signal applied to the front end of the NE605, the RSSI voltage level should read 250mV$_{RMS}$ or less to be a good layout. If the voltage output is higher, then this could indicate oscillations or regeneration in the design.

Performance Graphs of Output Section

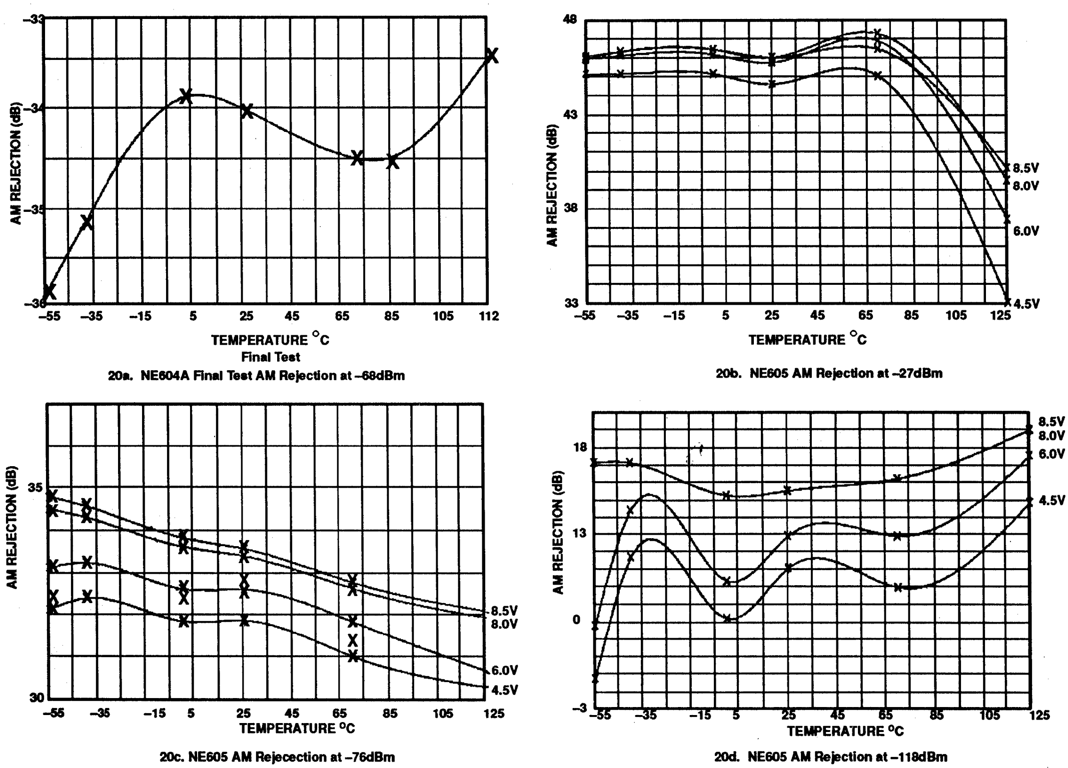
Fig.	Description
28	51kΩ Thermistor in Series with 100kΩ Resistor Across Quad Tank (Thermistor Quad Q Compensation)
29a	NE605 Application Board at –55°C
29b	NE605 Application Board at –40°C
29c	NE605 Application Board at +25°C
29d	NE605 Application Board at +85°C
29e	NE605 Application Board at +125°C
30a	NE604A for –68dBm RSSI Output vs. Temperature at Different Supply Voltages
30b	NE604A for –18dBm RSSI Output vs. Temperature at Different Supply Voltages
30c	NE605 for –120dBm RSSI Output vs. Temperature at Different Supply Voltages
30d	NE605 for –76dBm RSSI Output vs. Temperature at Different Supply Voltages
30e	NE605 for –28dBm RSSI Output vs. Temperature at different Supply Voltages
31	NE605 Audio level vs. Temperature and Supply Voltage
32	NE605 Data Output at –76dBm vs. Temperature

Referring to the NE/SA604A data sheet, there are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can be accomplished by adding attenuation between stages. More details on regeneration and stability considerations can be found in the NE/SA604A data sheet.

III. QUESTIONS & ANSWERS:

Q.–Bypass. How important is the effect of the power supply bypass on the receiver performance?

A. While careful layout is extremely critical, one of the single most neglected components is the power supply bypass in applications of NE604A or NE605. Although increasing the value of the tantalum capacitor can solve the problem, more careful testing shows that it is actually the capacitor's ESR (Equivalent Series Resistance) that needs to be checked. The simplest way of screening the bypass capacitor is to test the capacitor's dissipation factor at a low frequency (a very easy test, because most of the low frequency capacitance meters display both C, and Dissipation factor).



20a. NE604A Final Test AM Rejection at –68dBm

20b. NE605 AM Rejection at –27dBm

20c. NE605 AM Rejecection at –76dBm

20d. NE605 AM Rejection at –118dBm

Figure 20. AM Rejection Results at Different Input Levels

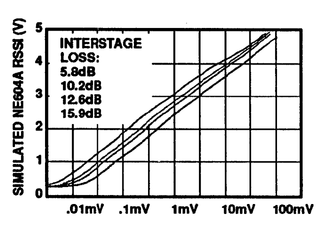


Figure 21. NE604A's RSSI Curve at Different Interstage Losses

Q.–On-chip oscillator. We cannot get the NE605 on-chip oscillator to work. What is the problem?

A. The on board oscillator is just one transistor with a collector that is connected to the supply, an emitter that goes to ground through a 25k resistor, and a base that goes to the supply through an 18k resistor. The rest of the circuit is a buffer that follows the oscillator from the transistor base (this buffer does not affect the performance of the oscillator).

Fundamental mode Colpitts crystal oscillators are good up to 30MHz and can be made by a crystal and two external capacitors. At higher frequencies, up to about 90MHz, overtone crystal oscillators (Colpitts) can be made like the one in the cellular application circuit. At higher frequencies, up to about 170MHz, Butler type oscillators (the crystal is in series mode) have been successfully demonstrated. Because of the 8GHz peak f_T of the transistors, LC Colpitts oscillators have been shown to work up to 900MHz. The problem encountered above 400MHz is that the on-chip oscillator level is not sufficient for optimum conversion gain of the mixer. As a result, an external oscillator should be used at those frequencies.

Generally, about 220mV$_{RMS}$ is the oscillator level needed on Pin 4 for maximum conversion gain of the mixer. An external oscillator driving Pin 4 can be used throughout the band. Finally, since the NE605's oscillator is similar to the NE602, all of the available application notes on NE602 apply to this case (assuming the pin out differences are taken into account by the user).

Below are a couple of points to help in the oscillator design. The oscillator transistor is biased around 250μA which makes it very hard to probe the base and emitter without disturbing the oscillator (a high impedance, low capacitance active FET probe is desirable). To solve these problems, an external 22k resistor (as low as 10k) can be used from Pin 3 to ground to double the bias current of the oscillator transistor. This external resistor is put there to ensure the start up of the crystal in the 80MHz range, and to increase the f_T of the transistor for above 300–400MHz operation. Additionally, this resistor is required for operations above 80–90MHz. When a 1k resistor from Pin 1 to ground is connected on the NE605, half of the mixer will shut off. This causes the mixer to act like an amplifier. As a result, Pin 20 (the mixer, now amplifier output) can be probed to measure the oscillator frequency. Furthermore, the signal at Pin 20 relates to the true oscillator level . This second resistor is just for optimizing the oscillator of course. Without the 1k resistor, the signal at Pin 20 will be a LO feedthrough which is very small and frequency dependent.

Finally in some very early data sheets, the base and emitter pins of the oscillator were inadvertently interchanged. The base pin is Pin 4, and the emitter pin is Pin 3. Make sure that your circuit is connected correctly.

Q.–Sensitivity at higher input frequencies. We cannot get good sensitivity like the 45MHz case at input frequencies above 70MHz. Do you have any information on sensitivity vs. input frequency?

A. The noise figure and the gain of the mixer degrade by less than 0.5dB, going from 50 to 100MHz. Therefore, this does not explain the poor degradation in sensitivity. If other problems such as layout, supply bypass etc. are already accounted for, the source of the problem can be regeneration due to the 70MHz oscillator. What is probably happening is that the oscillator signal is feeding through the IF, getting mixed with the 455kHz signal, causing spurious regeneration. The solution is to reduce the overall gain to stop the regeneration.

This gain reduction can be done in a number of places. Two simple points are the attenuator network before the second filter and the LO level (see Figure 22). The second case will reduce the mixer's noise figure which is not desirable. Therefore, increasing the Interstage loss, despite minimal effect on the RSSI linearity, is the correct solution. As the Interstage loss is increased, the regeneration problem is decreased, which improves sensitivity, despite lowering of the over-all gain (the lowest RSSI level will keep decreasing as the regeneration problem is decreased). For an 81MHz circuit it was found that increasing the Interstage loss from 12dB to about 17dB produced the best results (–119dBm sensitivity). Of course, adding any more Interstage loss will start degrading sensitivity.

Conversely, dealing with the oscillator design, low LO levels could greatly reduce the mixer conversion gain and cause degradation of the sensitivity. For the 81MHz example, a 22k parallel resistor from Pin 3 to ground is required for oscillator operation where a Colpitts oscillator like the one in the cellular application circuit is used. The LO level at Pin 4 should be around 220mV$_{RMS}$ for good operation. Lowering the LO level to approximately 150mV$_{RMS}$ may be a good way of achieving stability if increasing Interstage attenuation is not acceptable. In that case the 22k resistor can be made a thermistor to adjust the LO level vs. temperature for maintaining sensitivity and ensuring crystal start-up vs. temperature. At higher IF frequencies (above 30MHz), the interstage gain reduction is not needed. The bandwidth of the IF section will lower the overall gain. So, the possibility of regeneration decreases.

Q.–Mixer noise figure. How do you measure the mixer noise figure in NE605, and NE602?

A. We use the test circuit shown in the NE602 data sheet. The noise figure tester is the HP8970A. The noise source we use is the HP346B (ENR = 15.46dB). Note that the output is tuned for 10.7MHz. From that test circuit the NF-meter measures a gain of approximately 15dB and 5.5dB noise figure.

More noise figure data is available in the paper titled "Gilbert-type Mixers vs. Diode Mixers" presented at RF Expo '89 in Santa Clara, California. (Reprints available through Signetics Publication Services.)

Q.– What is the value of the series resistor before the IF filter in the NE605 or NE604A applications?

A. A value of 5.1kΩ has been used by us in our demo board. This results in a maximally straight RSSI curve. A lower value of about 1k will match the filter better. A better solution is to use an L pad as discussed earlier in this application note.

Q.– What is the low frequency input resistance of the NE605?

A. The data sheets indicated a worst case absolute minimum of 1.5k. The typical value is 4.7k.

Q.– What are BE-BC capacitors in the NE605 oscillator transistor?

A. The oscillator is a transistor with the collector connected to the supply and the emitter connected to the ground through a 25k resistor. The base goes to the supply through an 18k resistor. The junction capacitors are roughly about 24fF (fempto Farads) for CJE (Base-emitter capacitors), and 44fF for CJC (Collector-base capacitors). There is a 72fF capacitor for CJS (Collector-substrate capacitor). This is all on the chip itself. It should be apparent that the parasitic packaging capacitors (1.5–2.5pF) are the dominant values in the oscillator design.

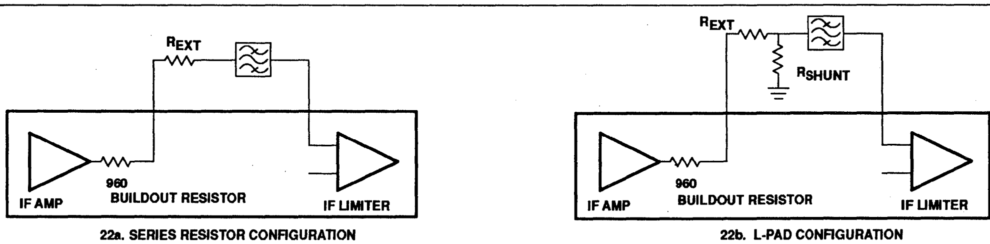


Figure 22. Implementing the 12dB Insertion Loss

Summary of Differences for NE/SA604/604A

	NE/SA604	NE/SA604A
RSSI	No temperature compensation	Internally temperature compensated
IF Bandwidth	15MHz	25MHz
IF Limiter Output	No buffer	Emitter follower buffer output with 8k in the emitter
Current Drain	2.7mA	3.7mA

Q.– What are the differences between the NE604 and NE604A? (see Table below)

A. The NE/SA604A is an improved version of the NE/SA604. Customers, who have been using the NE604 in the past, should have no trouble doing the conversion.

The main differences are that the small signal IF bandwidth is 25MHz instead of 15MHz, and the RSSI is internally temperature compensated. If external temperature compensation was used for the NE604, the designer can now cut cost with the NE604A. The designer can either get rid of these extra parts completely or replace the thermistor (if used in original temperature compensated design) with a fixed resistor.

Those using the NE604 at 455kHz should not see any change in performance. For 10.7MHz , a couple of dB improvement in performance will be observed. However, there may be a few cases where instability will occur after using NE604A. This will be the case if the PC-board design was marginal for the NE604 in the first place. This problem, however, can be cured by using a larger than 10μF tantalum bypass capacitor on the supply line, and screening the capacitors for their ESR (equivalent series resistance) as mentioned earlier. The ESR at 455kHz should be less than 0.2Ω. Since ESR is a frequency dependent value, the designer can correlate good performance with a low frequency dissipation factor, or ESR measurement, and screen the tantalum capacitors in production. There are some minor differences as well. The NE/SA604A uses about 1mA more current than the NE/SA604. An emitter follower has been added at the limiter output to present a lower and more stable output impedance at Pin 9. The DC voltage at the audio and data outputs is approximately 3V instead of 2V in the NE604, but that should not cause any problems. The recovered audio level, on the other hand, is slightly higher in the NE604A which should actually be desirable. Because of these changes, it is now possible to design 21.4MHz IFs using the NE604A, which was not possible with the NE604.

The two chips are identical, otherwise. The customers are encouraged to switch to the NE604A because it is a more advanced bipolar process than the previous generation used in theNE604. As a result we get much tighter specifications on the NE604A.

Q.– How does the NE605 mixer compare with a typical double balanced diode mixer?

A. Some data on the comparison of the conversion gain and LO power requirements are shown in this application note. These two parameters reveal the advantages in using the NE605 mixer.

The only drawback of the NE605 may seem to be its lower third-order intercept point in comparison to a diode mixer. But, this is inherent in the NE605 as a result of the low power consumption. If one compares the conversion gain of the NE605 with the conversion loss of a low cost diode mixer, it turns out that the third-order intercept point, referred to the output, is the same or better in the NE605. Another point to take into account is that a diode mixer cannot be used in the front end of a receiver without a preamp due to its poor noise figure. A third-order intercept analysis shows that the intercept point of the combination of the diode mixer and preamp will be degraded at least by the gain of the preamp. A preamp may not be needed with NE605 because of its superior noise figure.

For more detailed discussion of this topic please refer to the paper titled "Gilbert-type Mixers vs. Diode Mixers").

Q.– How can we use the NE605 for SCA FM reception?

A. The 10.7MHz application circuit described in AN1993 can be used in this case. The LO frequency should be changed and the RF front-end should be tuned to the FM broadcast range. The normal FM signal, coming out of Pin 8 of the NE605, could be expected to have about 1.5μV (into 50Ω) sensitivity for 20dB S/N. This signal should be band-pass filtered and amplified to recover the SCA sub-carrier. The output of that should then go to a PLL SCA decoder, shown on the data sheet of Signetics NE565 phase lock loop, to demodulate the base-band audio. The two outputs of the NE605 Pins 8 and 9 can be used to receive SCA data as well as voice, or features such as simultaneous reception of both normal FM, and SCA. The RSSI output, with its 90dB dynamic range, is useful for monitoring signal levels.

Q.– What is the power consumption of the NE605 or NE604A vs. temperature and V_{CC}?

A. The NE605 consumes about 5.6mA of current at 6V. This level is slightly temperature and voltage dependent as shown in Figure 33. Similar data for the NE604A is shown in Figure 34.

Q.– How can you minimize RF and LO feedthroughs

A. The RF and LO feedthroughs are due to offset voltages at the input of the mixer's differential amplifiers and the imbalance of the parasitic capacitors. A circuit, such as the one shown in Figure 35, can be used to adjust the balance of the differential amplifiers. The circuit connected to Pins 1 and 2 will minimize RF feedthrough while the circuit shown connected to Pin 6 will adjust the LO feedthrough. The only limitation is that if the RF and LO frequencies are in the 100MHz range or higher, these circuits will probably be effective for a narrow frequency range.

Q.– Distortion vs. RF input level. We get a good undistorted demodulated signal at low RF levels, but severe distortion at high RF levels. What is happening?

A. This problem usually occurs at 10.7MHz or at higher IF's. The IF filters have not been properly matched on both sides causing a sloping IF response. The resulting distortion can be minimized by adjusting the quad tank at the FM threshold where the IF is out of limiting. As the RF input increases, the IF stages will limit and make the IF response flat again. At this point, the effect of the bad setting of the quad tank will show itself as distortion. The solution is to always tune the quad tank for distortion at a medium RF level, to make sure that the IF is fully limited. Then, to avoid excessive distortion for low RF levels, one should make sure that the IF filters are properly matched.

Q.–The most commonly asked questions: "Why doesn't the receiver sensitivity meet the specifications?"; "Why is the RSSI dynamic range much less than expected?"; "Why does the RSSI curve dip at 0.9V and stay flat at 1V as the RF input decreases?"; "Why does the audio output suddenly burst into oscillation, or output wideband noise as the RF input goes down, instead of dying down slowly?"; "When looking at the IF output with a spectrum analyzer, why do high amplitude spurs become visible near the edge of the IF band as the RF level drops?"

A. These are the most widely observed problems with the NE605. They are all symptoms of the same problem; instability. The instability is due to bad layout and grounding.

Regenerative instability occurs when the limiter's output signals are radiated and picked up by the high impedance inputs of the mixer and IF amp. This signal is amplified by both the IF amp and limiter. Positive feedback causes the signal to grow until the signal at the limiter's output becomes limited. Due to the nature of FM, this instability will dominate any low RF input levels and capture the receiver (see Figure 23).

Since the receiver behaves normally for high RF inputs, it misleads the designer into believing that the design is okay. Additionally the RSSI circuit cannot determine whether the signal being received is coming from the antenna or the result of regenerative instability. Therefore, RSSI will be a good instability indicator in this instance because the RSSI will stay at a high level when the received signal decreases. Looking at the IF spectrum (Pin 11 for 605, Pin 9 for 604A) with the RF carrier present (no modulation), the user will see a shape as shown below. When regenerative instability occurs, the receiver does not seem to have the ultimate sensitivity of which it is capable.

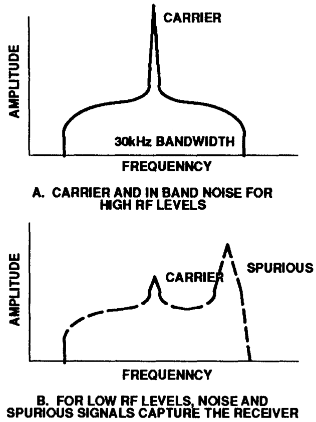


Figure 23.

Make sure that a double sided layout with a good ground plane on both sides is used. This will have RF/IF loops on both sides of the board. Follow our layouts as faithfully as you can. The supply bypass should have a low ESR 10–15μF tantalum capacitor as discussed earlier. The crystal package, the inductors, and the quad tank shields should be grounded. The RSSI output should be used as a progress monitor even if is not needed as an output. The lowest RSSI level should decrease as the circuit is made more stable. The overall gain should be reduced by lowering the input impedance of the IF amplifier and IF limiter, and adding attenuation after the IF amplifier, and before the 2nd filter. A circuit that shows an RSSI of 250mV or less with no RF input should be considered close to the limit of the performance of the device. If the RSSI still remains above 250mV, the recommendations mentioned above should be revisited.

Q.– Without the de-emphasis network at the audio output, the –3dB bandwidth of the audio output is limited to only 4.5kHz. The maximum frequency deviation is 8kHz, and the IF bandwidth is 25kHz. What is the problem?

A. What is limiting the audio bandwidth in this case is not the output circuit, but the IF filters. Remember that Carson's rule for FM IF bandwidth requires the IF bandwidth to be at least:

2(Max frequency Dev. + Audio frequency)

With a 25kHz IF bandwidth and 8kHz frequency deviation, the maximum frequency that can pass without distortion is approximately 4.5kHz. 2(8kHz + 4.5kHz) is 25kHz as expected.

REFERENCES:

"High-Performance Low-Power FM IF System" (NE604A data sheet), Signetics Linear Data Manual, Signetics, 1988.

"AN199-Designing with the NE/SA604", Signetics Linear Data Manual, 1987.

"AN1981–New Low Power Single Sideband Circuits", Signetics Linear Data Manual, 1988.

"Applying the Oscillator of the NE602 in Low Power Mixer Applications", Signetics Linear Data Manual, 1988.

"AN1993–High Sensitivity Applications of Low-Power RF/IF Integrated Circuits", Signetics Linear Data Manual, 1988.

"RF Circuit Design", Bowick. C., Indiana: Howard W. Sams & Company, 1982.

"The ARRL Handbook for the Radio Amateur", American Radio Relay League, 1986.

"Communications Receivers: Principles & Design", Rohde, U., Bucher, T.T.N., McGraw Hill, 1988.

"Gilbert-type Mixers vs. Diode Mixers", proceedings of R.F. Expo 1989, Fotowat, A., Murthi, E., pp. 409-413.

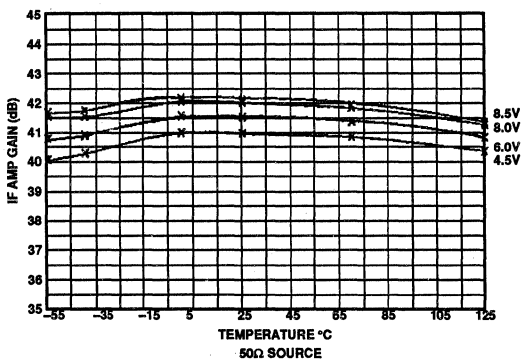


Figure 24. IF Amplifier Gain

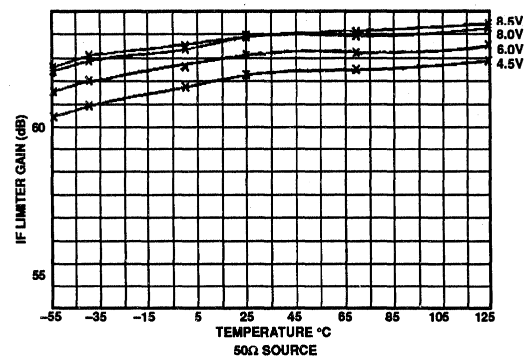


Figure 25. IF Limiter Gain

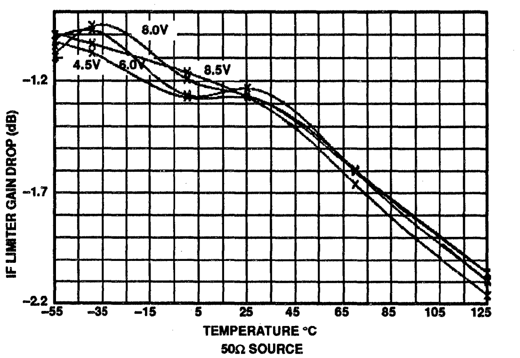


Figure 26. IF Amplifier Gain Drop, 20MHz Response

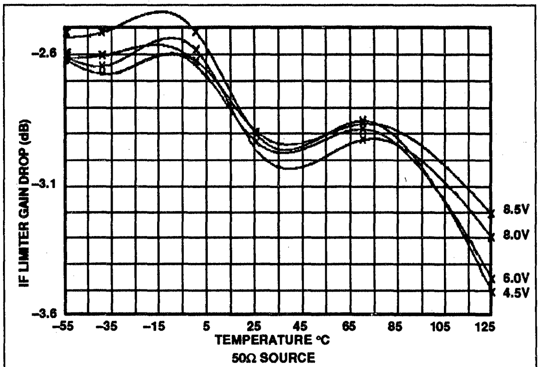


Figure 27. IF Limiter Drop, 20MHz Response

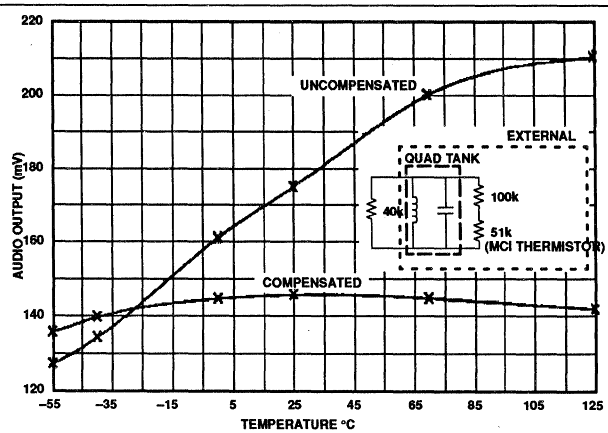
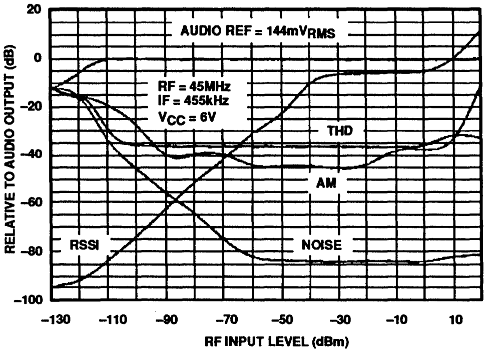
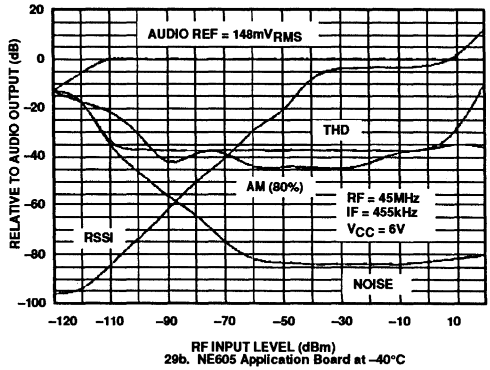


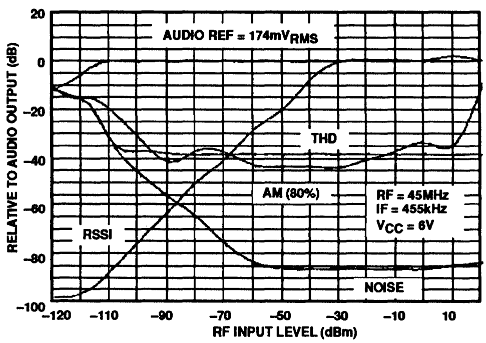
Figure 28. Audio Output: Compensated vs Uncompensated



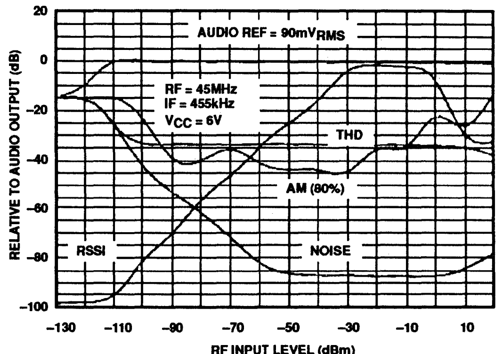
29a. NE605 Application Board at –55°C



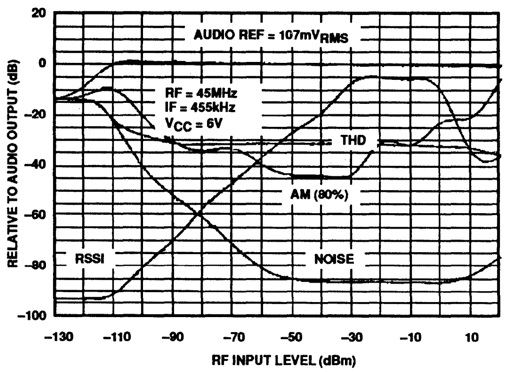
29b. NE605 Application Board at –40°C



29c. NE605 Application Board at 25°C

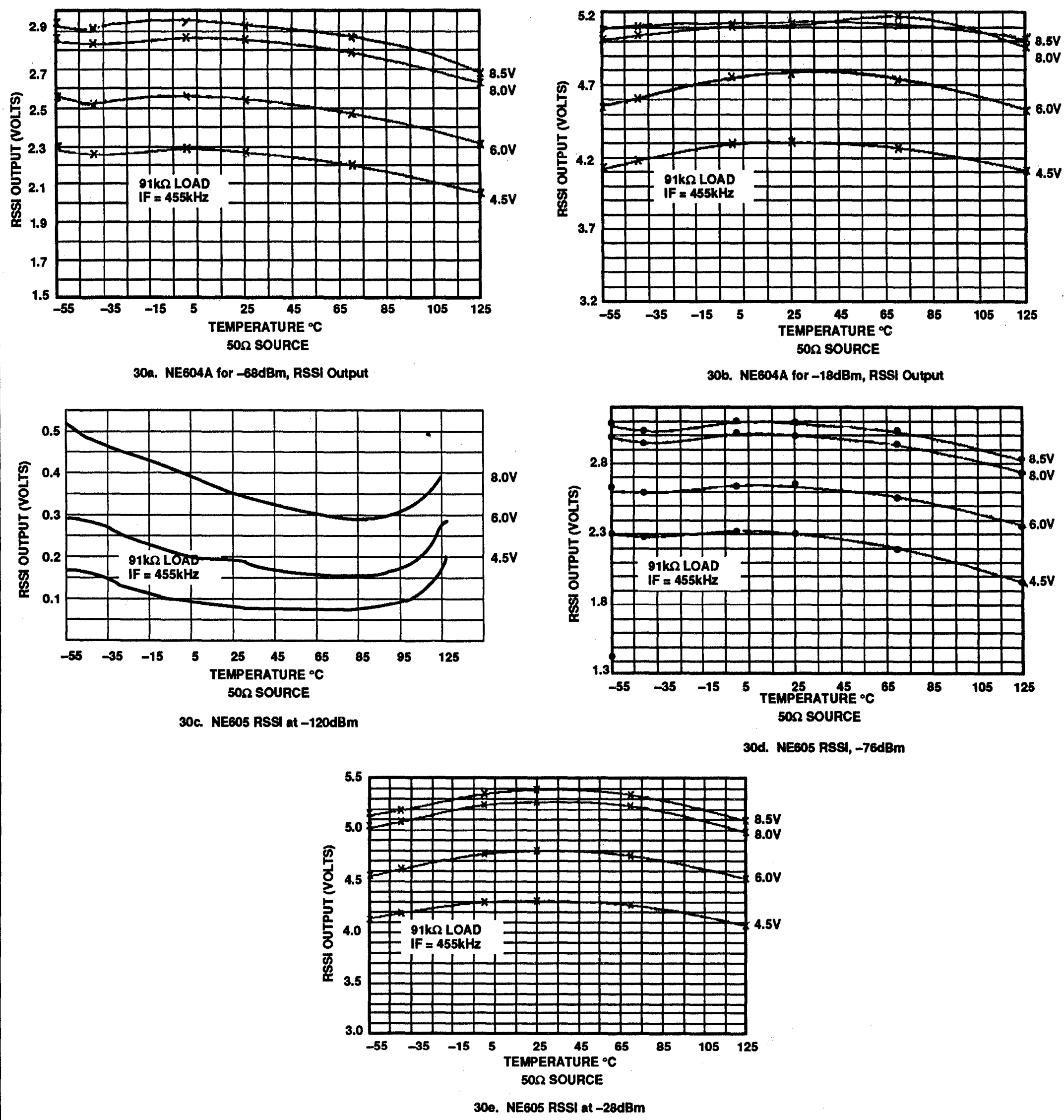


29d. NE605 Application Board at 85°C



29e. NE605 Application Board at 125°C

Figure 29. Performance of the NE605 Application Board at Different Temperatures



30a. NE604A for –68dBm, RSSI Output

30b. NE604A for –18dBm, RSSI Output

30c. NE605 RSSI at –120dBm

30d. NE605 RSSI, –76dBm

30e. NE605 RSSI at –28dBm

Figure 30. RSSI Response for Different Inputs

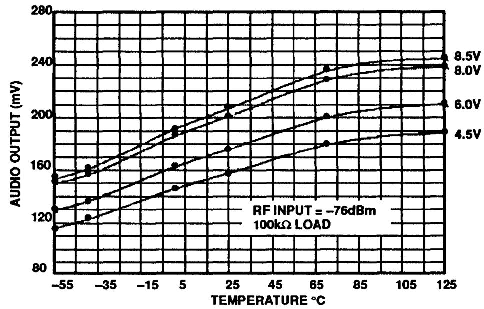


Figure 31. Audio Level vs Temperature and Supply Voltage

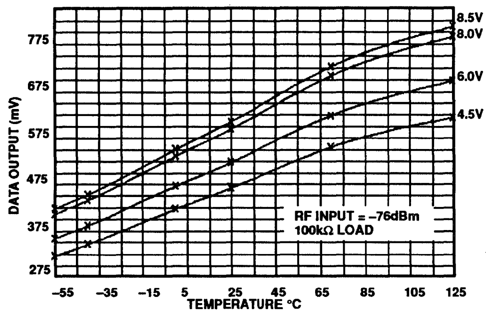


Figure 32. Data Level vs Temperature and Supply Voltage

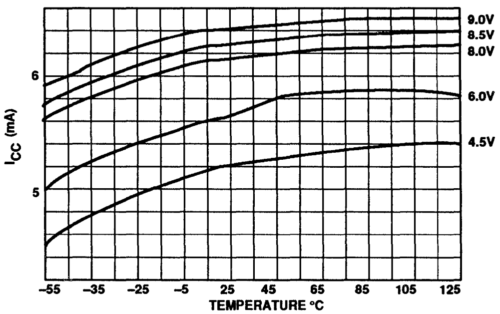


Figure 33. NE605 I_{CC} vs Temperature

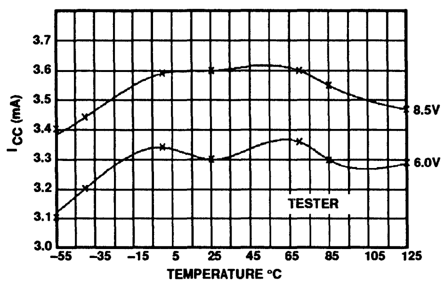


Figure 34. NE604A I_{CC} vs Temperature

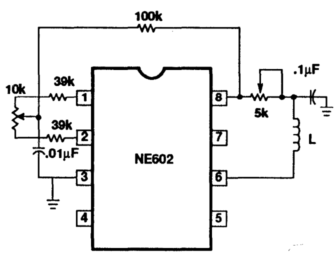
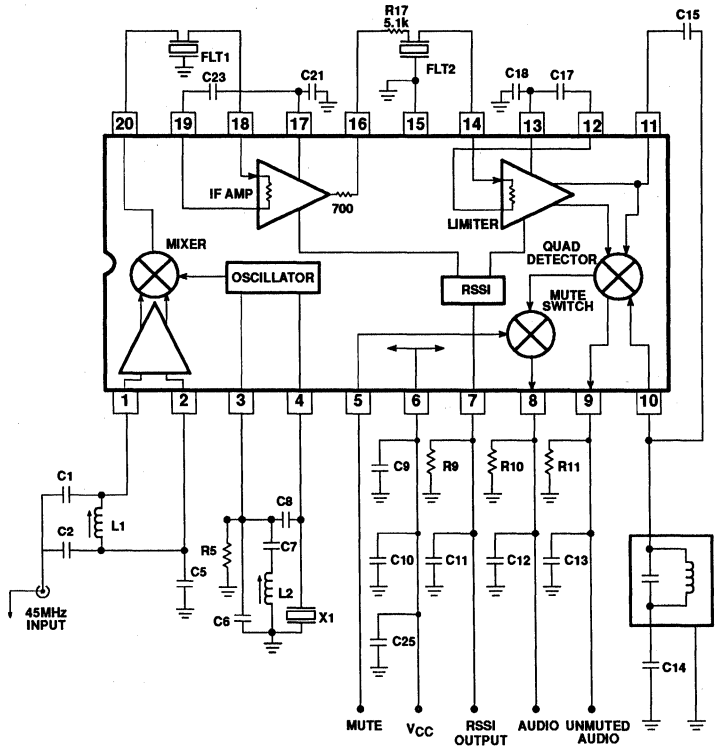


Figure 35. Minimizing RF and LO Feedthrough



Application Component List

C1	100pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C9	100nF ±10% Monolithic Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C10	15µF Tantalum (minimum)	L2	3.3µH nominal Toko 292CNS–T1046Z
C11	100nF ±10% Monolithic Ceramic	X1	44.545MHz Crystal ICM4712701
C12	15nF ±10% Ceramic	R9	100k ±1% 1/4W Metal Film
C13	150pF ±2% N1500 Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C14	100nF ±10% Monolithic Ceramic	R5	Not Used in Application Board (see Note 8)
C15	10pF NPO Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

Figure 36. NE/SA605 45MHz Application Circuit

Reviewing key areas when designing with the NE605 AN1994

Table 1. Related Application Notes

App. Note	Date	Title	Main Topics
AN198	Feb. 1987	Designing with the NE/SA602	– Advantages/Disadvantages to single-ended or balanced matching
AN1981	Dec. 1988	New Low Power Single Sideband Circuits	– General discussion on SSB circuits – Audio processing – Phasing-filter technique
AN1982	Dec. 1988	Applying the Oscillator of the NE602 in Low Mixer Applications	– Oscillator configurations
AN199	Feb. 1987	Designing with the NE/SA604	Circuits of: – AM synchronous det. – Temp. compensated RSSI circuit – Field strength meter – Product detector
AN1991	Dec. 1988	Audio Decibel Level Detector with Meter Driver	– Uses of the 604 in application
AN1993	Dec. 1988	High Sensitivity Application Low-Power RF/IF Integrated Circuits	– An overview of the NE602 and NE604 in typical applications – Good information before getting started

Table 2. Comparing Balanced vs Unbalanced Matching

NE605 or NE602	Matching	Advantages	Disadvantages
Pins 1 and 2 (RF input)	Single-ended (unbalanced)	– Very simple circuit – No sacrifice in 3rd-order performance	– Increase in 2nd-order products
	Balanced	– Reduce 2nd-order products	– Impedance match difficult to achieve

Table 3. LO Configurations

LO (MHz)	Suggested Configuration Using On-board Oscillator
0 - 30	Fundamental mode, use Colpitts
30 - 70	3rd overtone mode, use Colpitts
70 - 90	3-5th overtone mode, use Colpitts with 22kΩ resistor connected from the emitter pin to ground
90 - 170	Use Butler, crystal in series mode, and a 22kΩ resistor connected from the emitter pin to ground
170 - 300	LC configuration

Evaluating the NE605 SO and SSOP demo-board

AN1995

Author: Alvin K. Wong

INTRODUCTION:

With the increasing demand for smaller and lighter equipment, designers are forced to reduce the physical size of their systems. There are several approaches to solving the size problem. A designer needs to look for sophisticated integrated single chip solutions, chips that are smaller in size, and chips that require minimum external components.

Signetics offers all of these solutions in their NE605. The NE605 single-chip receiver converts the RF signal to audio and is available in three packages: DIP,SO, and SSOP. This offers total flexibility for layout considerations. The SSOP package is the smallest 20 pin package available in the market today, and allows the designer the flexibility to reduce the overall size of a layout.

When working with a smaller and tighter layout in a receiver design, it becomes important to follow good RF techniques. This application note shows the techniques used in the SO and SSOP demo-board. It does not cover the basic functionality of the NE605 but instead focuses more on the layout constraints. This application note also has a trouble-shooting chart to aid the designer in evaluating the SO and SSOP demo-board. For a complete explanation of the NE605, please refer to application note AN1994 which describes the basic block diagrams, reviews the common problems encountered with the NE605, and suggests solutions to them. Reading AN1994 is highly recommended before attempting the SO and SSOP layout.

The recommended layout demonstrates how well the chip can perform. But it should be pointed out that the combination of external parts with their tolerances plays a role in achieving maximum sensitivity.

The minimum and maximum 12dB SINAD measurement for both boards is -118dBm and -119.7dBm, respectively. A typical reading taken in the lab for both SO and SSOP demo-boards is -119dBm.

There were two different design approaches for both layouts. For the SO layout, there are inductive tuning elements (except for the LO section); for the SSOP layout there are capacitive tuning elements. This approach was taken to show the designer that both ways can be used to achieve the same 12dB SINAD measurement. However, it is worth mentioning that capacitive tuning elements are less expensive than the inductive tuning elements.

Packages Available

As mentioned above, there are three packages available for the NE605. See the "Package Outline" section of the Signetics 1992 RF Handbook for the physical dimensions of all three packages. Notice that the DIP package is the largest of the three in physical size; the SSOP is the smallest. The recommended layout and performance graphs for the DIP package are shown in the NE605 data sheet and AN1994. But the SO and SSOP recommended layout and performance graphs are shown in this application note.

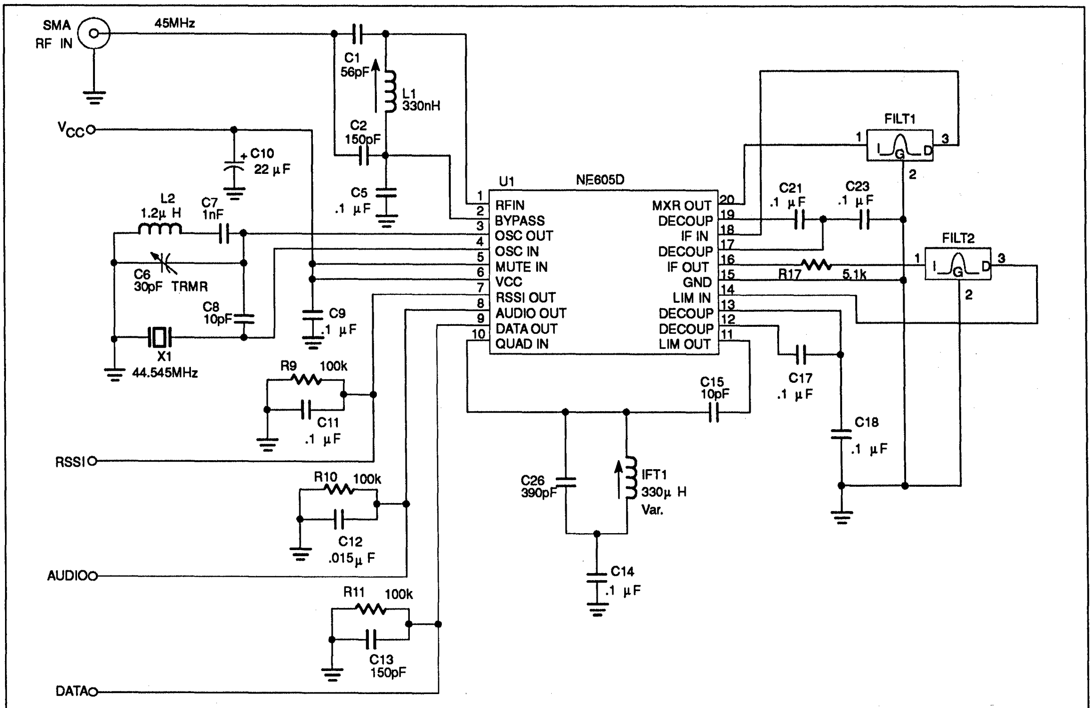


Figure 1. NE605 Schematic for the SO Layout

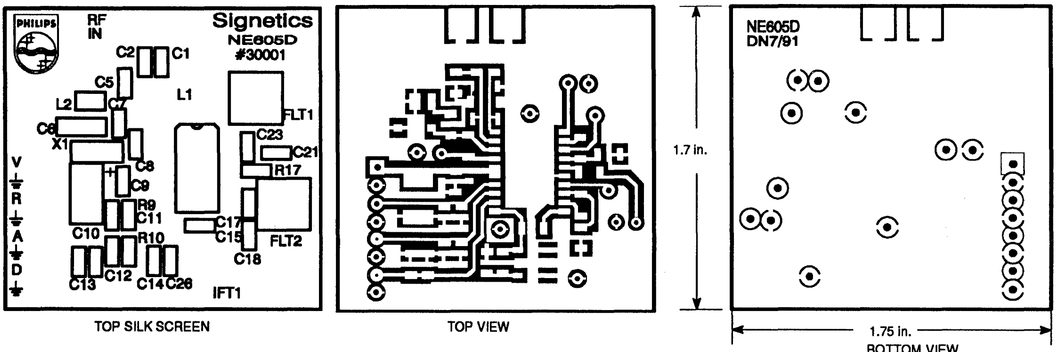


Figure 2. NE605 SO Demo-board Layout (Not Actual Size)

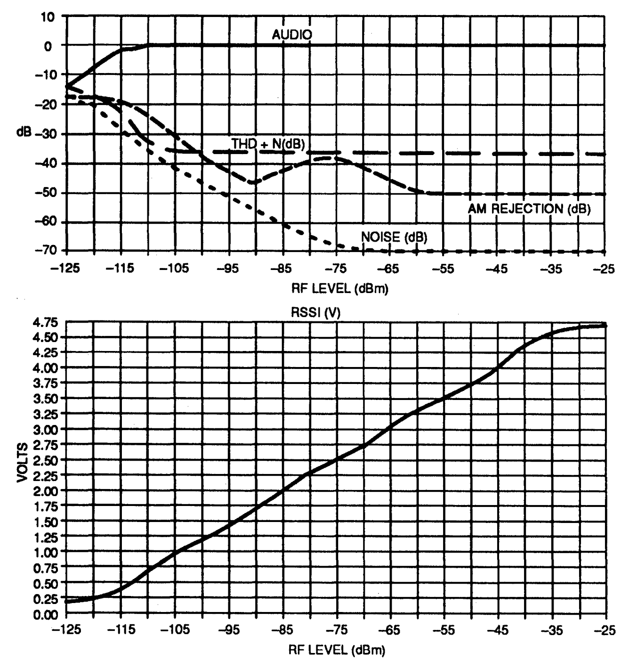


Figure 3. NE605 SO Performance Curves

SO LAYOUT:

Figure 1 shows the schematic for the SO layout. Listed below are the basic functions of each external component for Figure 1.

C1 – Part of the tapped-C network to match the front-end

C2 – Part of the tapped-C network to match the front-end

C5 – Used as an AC short to Pin 2

C6 – Used to tune the LO for the Colpitts oscillator

C7 – Used as part of the Colpitts oscillator

C8 – Used as part of the Colpitts oscillator

C9 – Supply bypassing

C10 – Supply bypassing

C11 – Used as filter

C12 – Used as filter

C13 – Used as filter

C14 – Used to AC ground the Quad tank

C15 – Used to provide the 90° phase shift to the phase detector

C17 – IF limiter decoupling cap

C18 – IF limiter decoupling cap

C21 – IF amp decoupling cap

C23 – IF amp decoupling cap

C26 – Quad tank component

L1 – Part of tapped-C network to match the front-end TOKO 5CB-1320Z

L2 – Part of the Colpitts oscillator Coilcraft 1008CS-122

R9 – Used to convert the current into the RSSI voltage

R10 – Converts the audio current to a voltage

R11 – Converts the data current to a voltage

R17 – Used to achieve the –12dB insertion loss

IFT1 – Inductor for the Quad tank TOKO 303LN-1130

FILT1 – Murata SFG455A3 455kHz bandpass filter

FILT2 – Murata SFG455A3 455kHz bandpass filter

X1 – Standard 44.545MHz crystal in QC38 package

The recommended SO layout can be found in Figure 2 and should be used as an example to help designers get started with their projects.

The SO NE605 board performance graphs can be found in Figure 3.

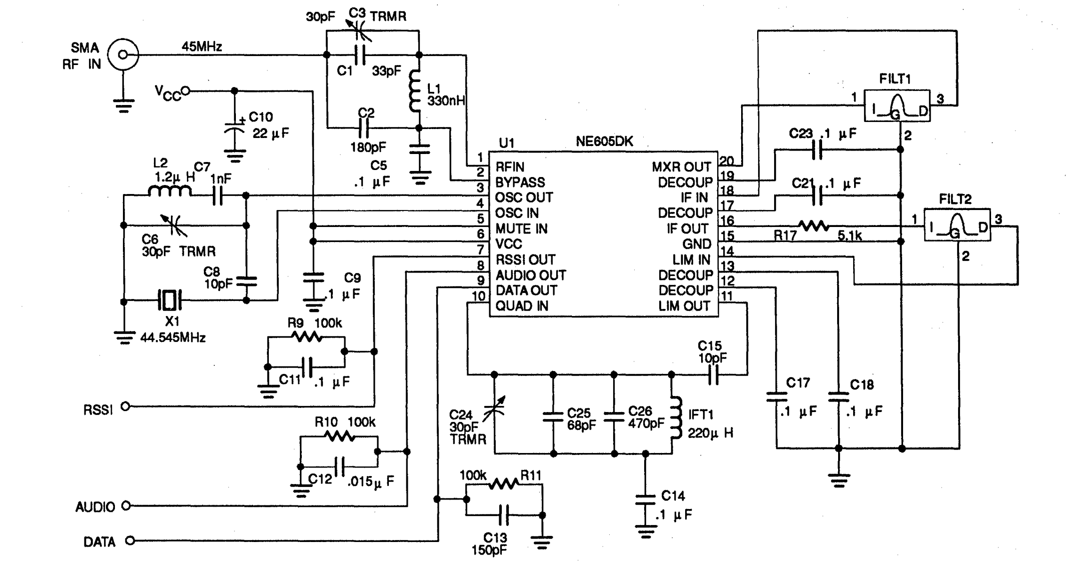


Figure 4. NE605 Schematic for the SSOP Layout

SSOP LAYOUT:

Figure 4 shows the schematic for the SSOP layout.

- C1 – Part of the tapped-C network to match the front-end
- C2 – Part of the tapped-C network to match the front-end
- C3 – Part of the tapped-C network to match the front-end
- C5 – Used as an AC short to Pin 2
- C6 – Used to tune the LO for the Colpitts oscillator
- C7 – Used as part of the Colpitts oscillator
- C8 – Used as part of the Colpitts oscillator
- C9 – Supply bypassing
- C10 – Supply bypassing
- C11 – Used as filter
- C12 – Used as filter
- C13 – Used as filter
- C14 – Used to AC ground the Quad tank
- C15 – Used to provide the 90° phase shift to the phase detector
- C17 – IF limiter decoupling cap
- C18 – IF limiter decoupling cap
- C21 – IF amp decoupling cap
- C23 – IF amp decoupling cap
- C24 – Part of the Quad tank
- C25 – Part of the Quad tank
- C26 – Part of the Quad tank
- L1 – Part of tapped-C network to match the front-end Coilcraft 1008CS-331
- L2 – Part of the Colpitts oscillator Coilcraft 1008CS-122
- R9 – Used to convert the current into the RSSI voltage
- R10 – Converts the audio current to a voltage
- R11 – Converts the data current to a voltage
- R17 – Used to achieve the –12dB insertion loss
- IFT1 – Inductor for the Quad tank Mouser ME435-2200
- FILT1 – Murata SFGCC455BX 455kHz bandpass filter
- FILT2 – Murata SFGCC455BX 455kHz bandpass filter
- X1 – Standard 44.545MHz crystal

The SSOP layout can be found in Figure 5. The SSOP NE605 board performance graphs can be found in Figure 6.

The main difference between the SO and SSOP demo-boards is that the SSOP demo-board incorporates the low profile 455kHz Murata ceramic filter. It has an input and output impedance of 1.0kΩ. This presents a mismatch to our chips, but we have found that the overall performance is similar to that when we use the "blue" Murata filters that have the proper 1.5kΩ input and output impedance.

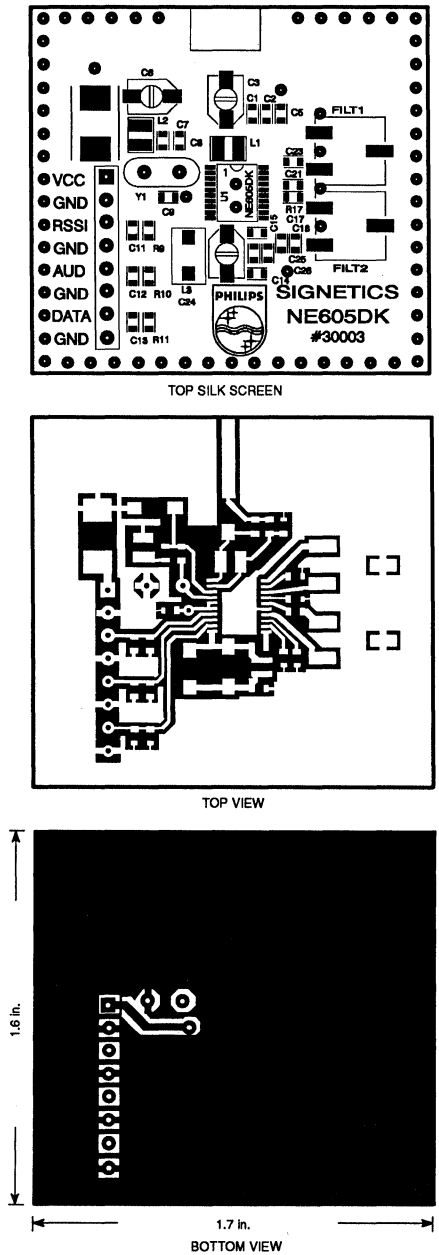


Figure 5. NE605 SSOP Demo-board Layout (Not Actual Size)

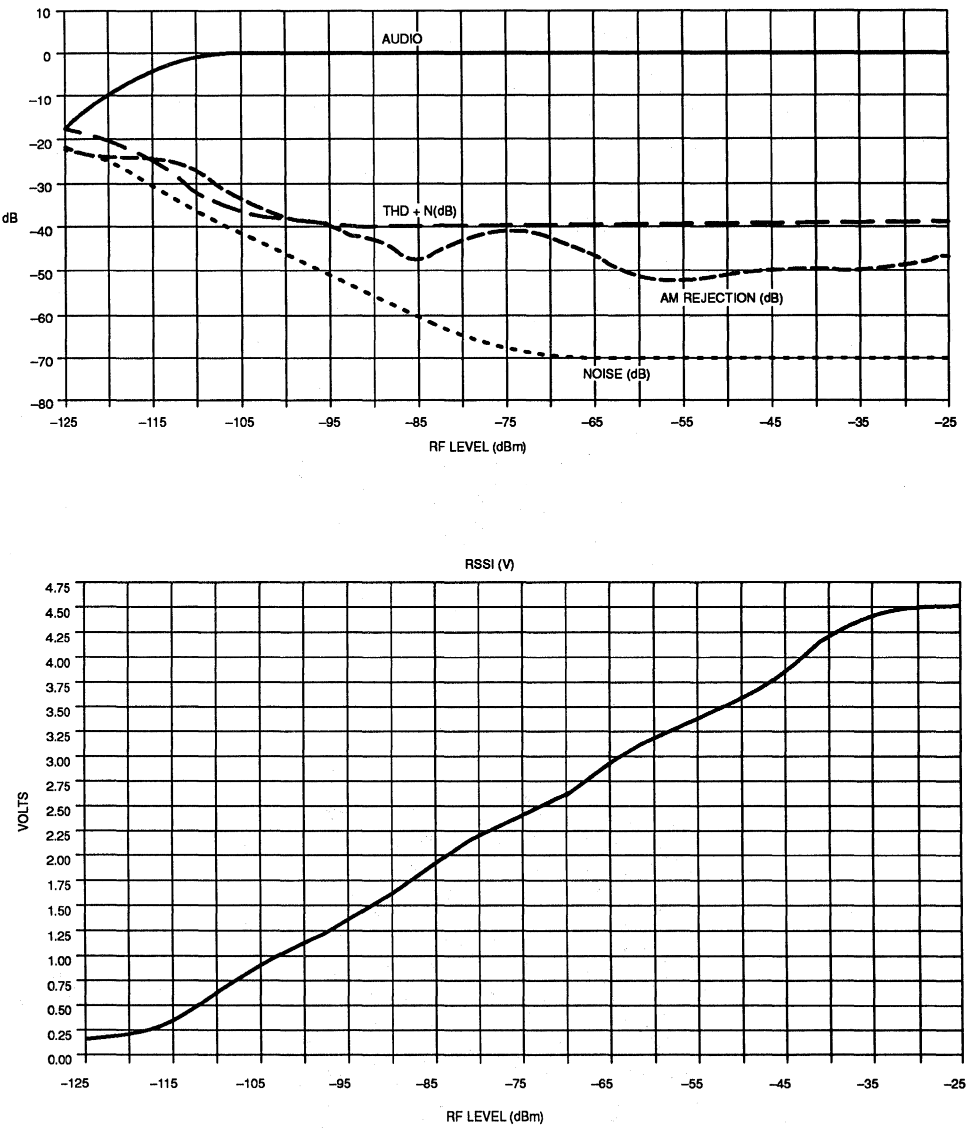


Figure 6. NE605 SSOP Performance Graphs

HOW TO TUNE THE NE605 DEMO-BOARD

Figure 7 shows a trouble-shooting chart for the NE605. It can be used as a general guide to tune the DIP, SO, and SSOP demo-boards. Below are some of the highlights from the trouble shooting chart that are explained in more detail.

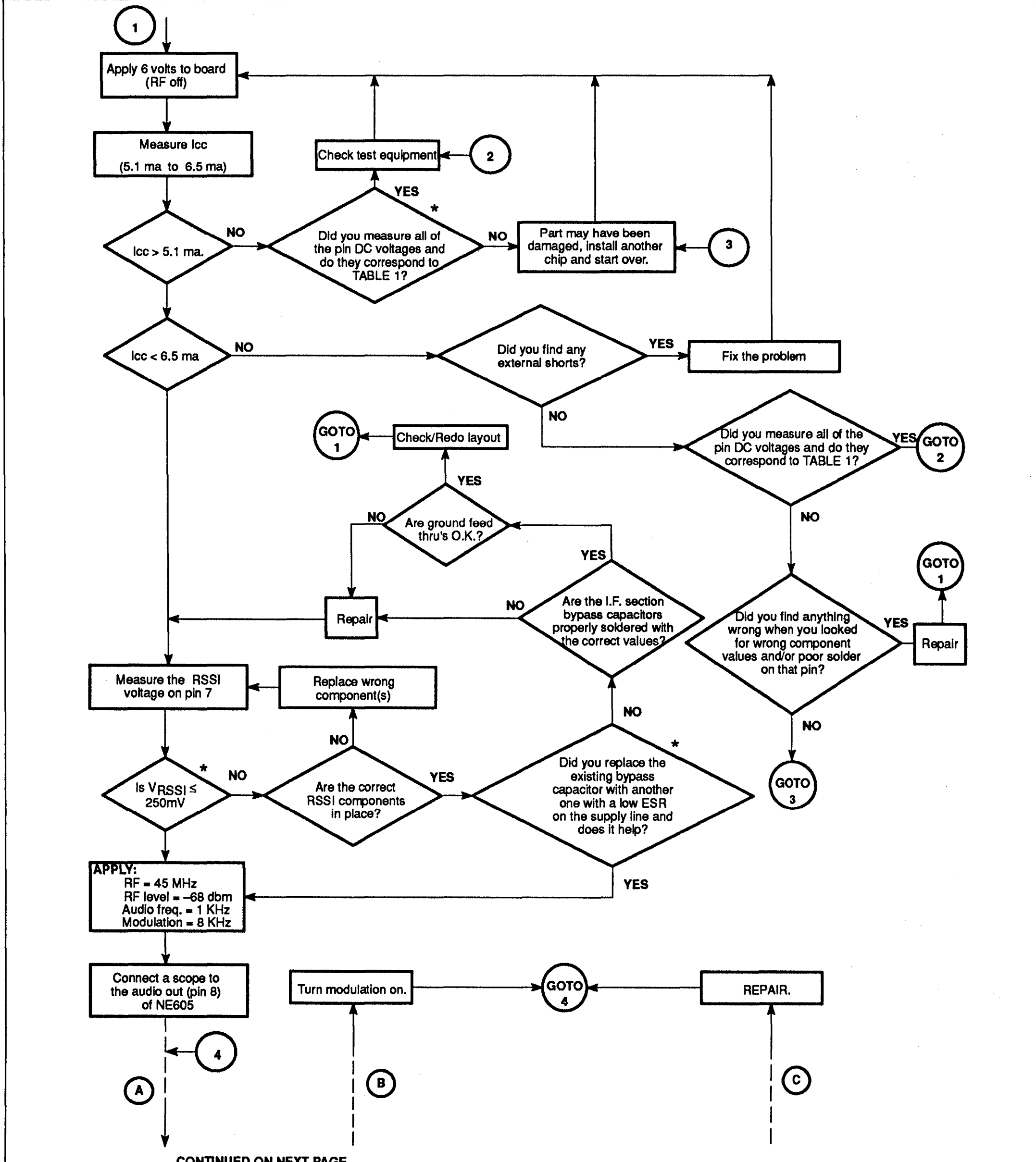


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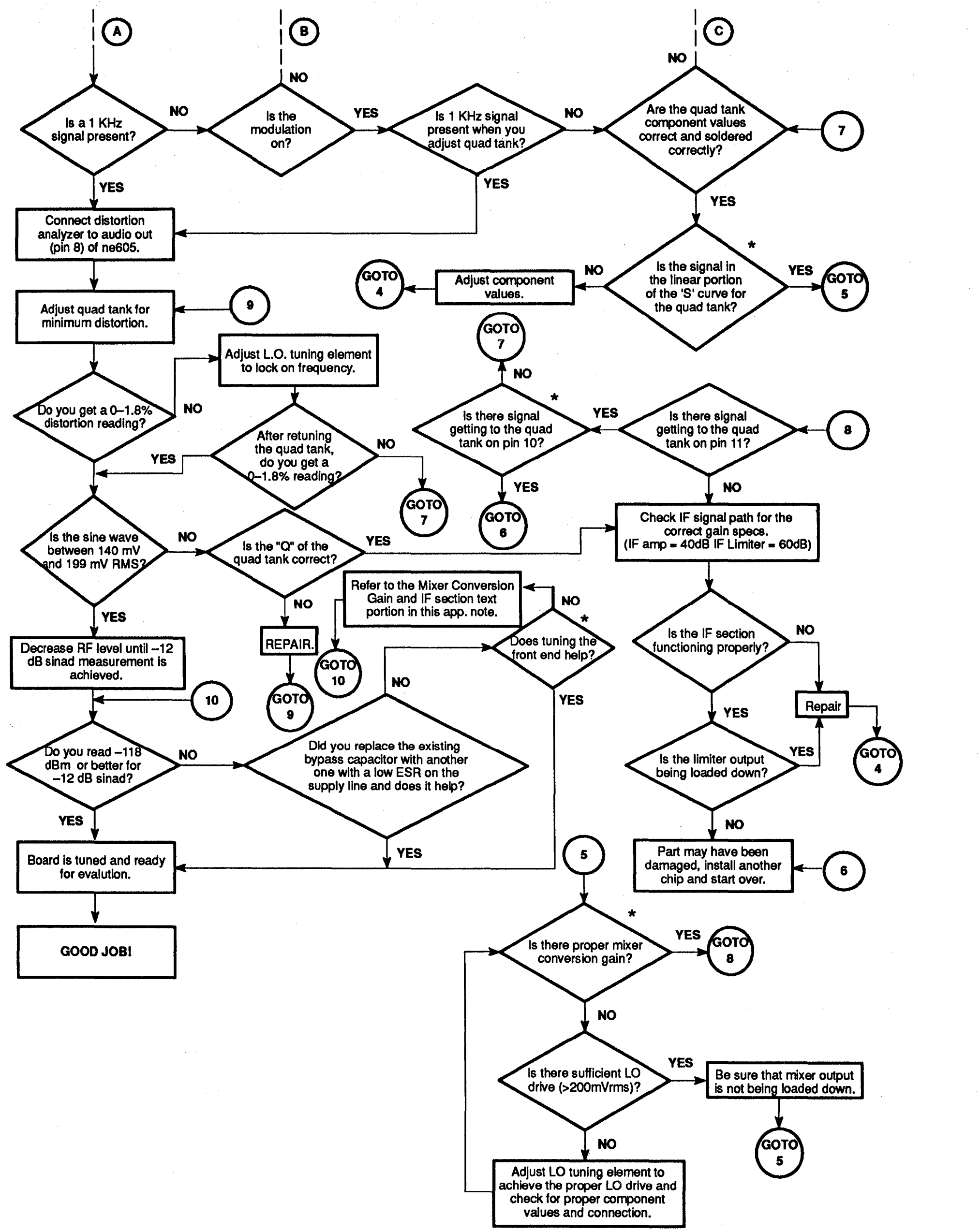
Figure 7. Trouble-shooting Chart for the NE605 Demo-board



*NOTE: Refer to the appropriate text section of the app. note for further details.

How to tell when a part is damaged

Since most SO and SSOP sockets hinder the maximum performance of the NE605, it is advisable to solder the packages directly to the board. By this approach, one will be able to evaluate the part correctly. However, it can be a tedious chore to switch to another part using the same layout. Therefore, to be absolutely certain that the chip is damaged, one can measure the DC voltages on the NE605. Table 1 shows the DC voltages that each pin should roughly have to be a good part.

Table 1. Approximate DC Voltages for the NE605

Pin Number	DC Voltage (V)
1	1.37
2	1.37
3	5.16
4	5.94
5	N/A
6	6.00 (V_{CC})
7	N/A
8	2.00
9	2.00
10	3.49
11	1.59
12	1.59
13	1.59
14	1.65
15	0.00 (GND)
16	1.60
17	1.60
18	1.60
19	1.60
20	4.87

Note: The DC voltage on Pin 5 is not specified because it can either be V_{CC} or ground depending if the audio is muted or not (Connecting ground on Pin 5 mutes the audio on Pin 8, while V_{CC} on Pin 5 unmutes the audio).

The DC voltage on Pin 7 is not specified because its DC voltage depends on the strength of the RF signal getting to the input of the NE605. It also can be used as a stability indicator.

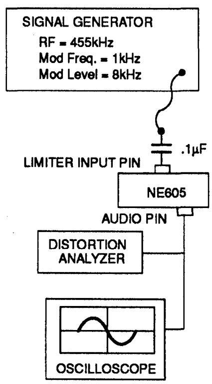
If any of the DC voltages are way off in value, and you have followed the trouble-shooting chart, the part needs to be changed.

RSSI Indicator

The next important highlight is using the RSSI pin as a stability indicator. With power connected to the part and no RF signal applied to the input, the DC voltage should read 250mV or less on Pin 7. Any reading higher than 250mV, indicates a regeneration problem. To correct for the regeneration problem, one should check for poor layout, poor bypassing, and/or poor solder joints. Bypassing the NE605 supply line with a low equivalent series resistance (ESR) capacitor to reduce the RSSI reading can improve the 12dB SINAD measurement by 8dB, as found in the lab. If the regeneration problem still exists, read AN1994.

Quad tank and S-Curve

As briefly mentioned in the chart, it is important to measure the Q of the quad tank if a distortion reading of 1.8% or less cannot be measured. Recall that if the Q of the quad tank is too high for the deviation, then premature distortion will occur. However, if the Q is too low for the deviation, the audio level will be too low. The audio level coming out of the audio pin should be $140mV_{RMS}$ to $190mV_{RMS}$.



FREQ. kHz	DC VOLTAGE (V)
400	1.66
430	1.24
455	2.13
480	3.08
510	2.88
⋮	⋮

Figure 8. Test Set-up to Measure S-Curve of the Quad Tank

If the distortion reading is too high and/or the audio level is too low, then it is important to measure and plot the S-curve of the quad tank. The test set-up used in the lab can be seen in Figure 8.

The following steps were taken to measure the S-curve for the SO and SSOP demo-boards.

Step 1. Remove the second IF ceramic filter from the demo-board.

Step 2. Connect a signal generator to the limiters input through a DC blocking capacitor.

Step 3. Connect a DC voltmeter and an oscilloscope to the audio output pin.

Step 4. Set the signal generator to a 455kHz signal and be sure that the modulation is on (RF=455kHz Mod Freq = 1kHz Mod Level=8kHz). Apply this 455Khz signal to the limiter input such that there is a sinewave on the oscilloscope screen. Adjust the quad tank for maximum sinewave amplitude on the oscilloscope or for lowest distortion. Additionally, adjust the supply input signal to the NE605 such that the 1kHz sinewave reaches its maximum amplitude.

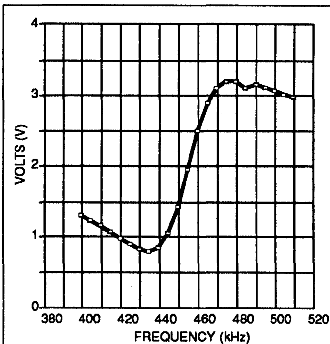


Figure 9. S-Curve for NE605 SO Demo-board

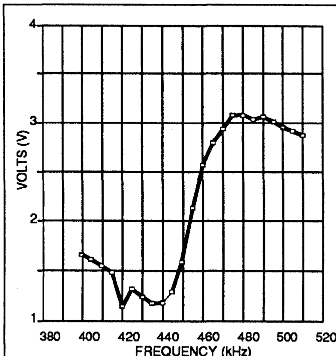


Figure 10. S-Curve for NE605 SSOP Demo-board

Step 5. Turn off the modulation and start taking data. Measure the Frequency vs DC voltage. Vary the frequency incrementally and measure the DC voltage coming out of the audio pin. Remember that once the modulation is turned off, the sinewave will disappear from the oscilloscope screen.

Step 6. Plot the S-curve.

Figures 9 and 10 show the S-curve measurements for the SO and SSOP demo-boards. Notice that the center of the S-curve is at 455kHz. The overall linearity determines how much deviation is allowed before premature distortion. Since our application requires ±8kHz of deviation, our S-curve is good because it exceeds the linear range of 447kHz to 463kHz.

If the Q of the quad tank needs to be lowered, a designer should put a resistor in parallel with the inductor. The lower the resistor value, the more the Q will be lowered. If the Q needs to be increased, choose a higher Q component. More information on the Quad tank can be found in the NE604A data sheet.

If the linear section of the S-curve is not centered at 455kHz, the quad tank component values need to be recalculated. The way to determine the component values is by using $F = \frac{1}{2\pi\sqrt{LC}}$ where F should be the IF frequency. In the case of the demo-boards, the IF = 455kHz.

Front End Tuning

The best way to tell if the front end of the NE605 is properly matched is to use a network analyzer in a S11 setting. The lower the dip, the greater the absorption of the wanted frequency. Figures 11 and 12 show the S11 dip for the front end matching of the SO and SSOP demo-boards, respectively.

We have found in the lab that a -8dB to -10dB dip is usually sufficient to get the maximum signal transfer such that a good 12dB SINAD reading is met. The front end circuit uses a tapped-C impedance transformation circuit which matches the 50Ω source with the input impedance of the mixer.

In the process of matching the front end, we have found that the ratio of the two capacitors play an important role in transferring the signal from the source to the mixer input. There should be approximately a 4:1 or 5:1 ratio.

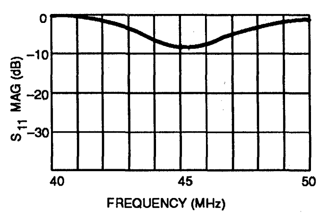


Figure 11. S11 Front-End Response for SO Demo-board

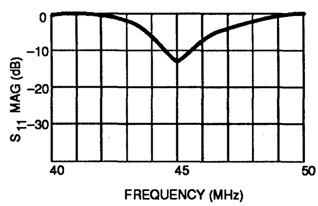


Figure 12. S11 Front-End Response for SSOP Demo-board

Checking the Conversion Gain of the Mixer

Once the front end has been properly matched, a designer should check the conversion gain if there are problems with the SINAD measurement. Be sure to turn off the modulation when making this measurement.

The method of measuring conversion gain on the bench is fairly simple. For our demo-boards, measure the strength of the 455kHz signal on the matching output network of the mixer with a FET probe. Then measure the 45MHz RF input signal on the matching input network of the mixer. Subtract the two numbers and the measured conversion gain should be around 13dB. Make sure that the input and output matching networks for the mixer have the same impedance since we are measuring voltage gain to get power gain ($P = V^2/R$). Of course this conversion gain value will change if there is a different RF input. In AN1994, Figure 16 shows how the conversion gain varies with different RF input frequencies.

Checking the gains in the IF Section

If the IF section does not give 100dB of gain, then the -118dBm SINAD measurement cannot be achieved. In fact some symptoms of low or no audio level can be due to the IF section.

One way of checking the function of the IF section is to check the gain of the IF amplifier and the IF limiter. The IF amplifier gain should be around 40dB and the IF limiter gain should be around 60dB.

To check this, connect a FET probe to the output of the amplifier. Apply a strong input signal with no modulation and then slowly lower the input signal and wait for the output of the amplifier to decrease. Measure the strength of the output signal in dB and then subtract from it the strength of the input signal in dB. This resulting number indicates the maximum gain of that section. (This method assumes matched input and output impedance.)

If a designer finds one of the sections with lower gain, then one area to check are the IF bypass capacitors. Be sure that the IF bypass capacitors have a good solid connection to the pad. It was also found in the lab that the RSSI stability reading improves when the IF bypass is properly installed.

QUESTION & ANSWER SECTION

Q: When I measure the bandpass response of the IF filters on the SSOP demo-board, it appears to have a little hump compared to the SO demo-board which has a flat filter response. Why is there a difference in the bandpass response when the SO and SSOP 605 chips are similar?

A: The answer has to do with the ceramic filters and not the package of the NE605. The reason why the SO demo-board has a flat bandpass response is because it is matched properly with the filter. The SSOP demo board uses the new Murata low profile ceramic 455kHz filter. Unfortunately, the input and output impedance is now 1kΩ instead of 1.5kΩ. This presents an impedance mismatch which creates the hump to occur in the bandpass response. But one does not have to worry too much about this response because the situation does not affect the overall performance that much. Additionally, the 12 SINAD measurement is similar whether using the "blue" (1.5kΩ) or "white" (1.0kΩ) Murata filters.

If you are worried about this, then switch to the correct "blue" Murata filters. The SSOP package will work with those filters as well.

But if your design has strict height requirements, the white filters are a good solution.

Q: How much LO signal do you see at the RF port?

A: The worst LO leakage seen at the RF input on the SO and SSOP demo-board is -40dBm/441mV. This seems to vary with the LO level into the base of the on board transistor. This measurement will also vary with different LO frequencies. The NE605 SO and SSOP demo-boards have a LO frequency of 44.545MHz. Since there are so many variables, a designer needs to measure his/her own board for an accurate LO-RF isolation measurement.

There are several ways to improve the LO leakage from getting to the antenna. One can choose a higher IF frequency and tighten up the bandwidth of the front-end filter. Another solution is to add a low noise amplifier between the antenna and the mixer, and/or design a double conversion receiver and make sure the 1st mixer has a LO-RF isolation which meets the system specifications.

Q: On the SO and SSOP demo-board, the LO oscillator circuit is tunable with a variable capacitor. Is this a requirement?

A: No. The variable capacitor is used to tune the LO freq., but one can use a fixed value. The advantage of going with a fixed value capacitor is that it is a cheaper component part and there is no need for tuning. The only advantage with a tunable LO is that a designer can optimize the performance of the receiver.

Q: I know that the IF bandwidth of the NE605 allows me to build an IF of 21.4MHZ. Will the NE605 SSOP package perform just as good at 21.4MHz IF as it does at 455kHz?

A: Although we have not worked with NE605 SSOP at 21.4MHZ, we believe that it would be difficult to get a 12dB SINAD measurement at -120dBm. The wavelengths are much smaller at 21.4MHz than 455kHz. Since the wavelengths are smaller, there is a higher probability of regeneration occurring in the IF section. Therefore, a designer will probably have to reduce the gain in the IF section. Additionally, the SSOP package has pins that are physically closer together than with the normal type of packaged parts which can contribute to the unstable state with higher IF frequencies.

Low-voltage high performance mixer FM IF system | NE/SA606

DESCRIPTION

The NE/SA606 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The NE/SA606 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The NE606 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to level adjust the outputs or add filtering.

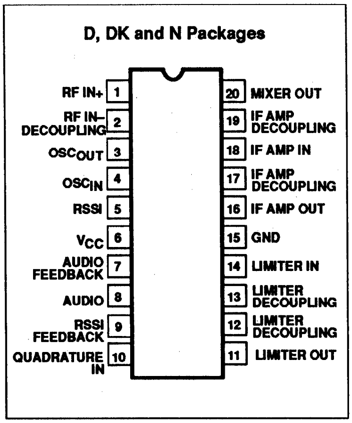
FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA606 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

PIN CONFIGURATION



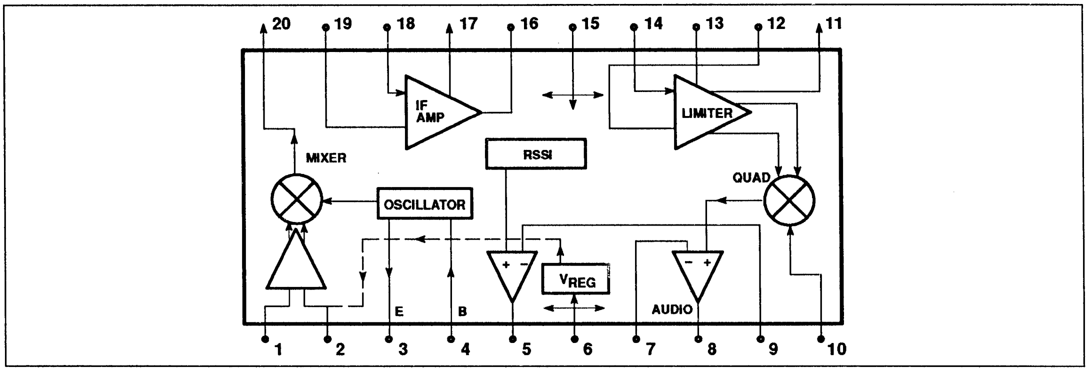
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE606N
20-Pin Plastic SOL (Surface-mount)	0 to +70°C	NE606D
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE606DK
20-Pin Plastic DIP	-40 to +85°C	SA606N
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA606D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA606DK

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range NE606	0 to +70	°C
	SA606	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA606			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA606			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE606 MIN	LIMITS NE606 TYP	LIMITS NE606 MAX	UNITS
	Input limiting –3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	114	160	mV
	SINAD sensitivity	IF level –110dBm		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	.80	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.20	1.8	2.50	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (Int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		240		mV_{RMS}
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA606 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA606 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA606 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

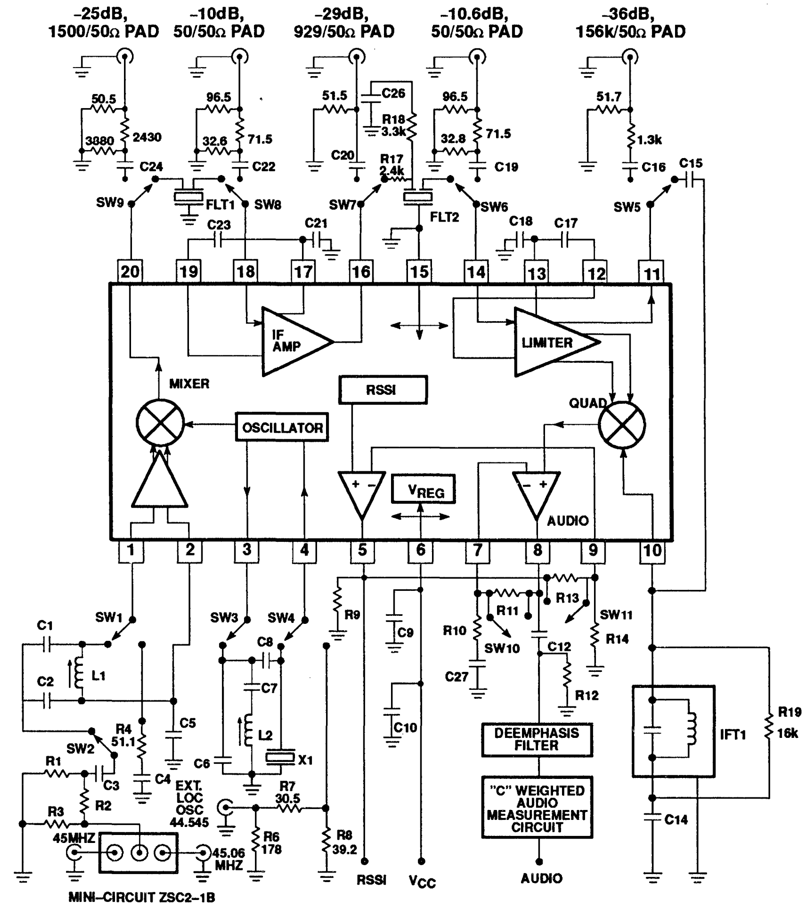
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 2kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}

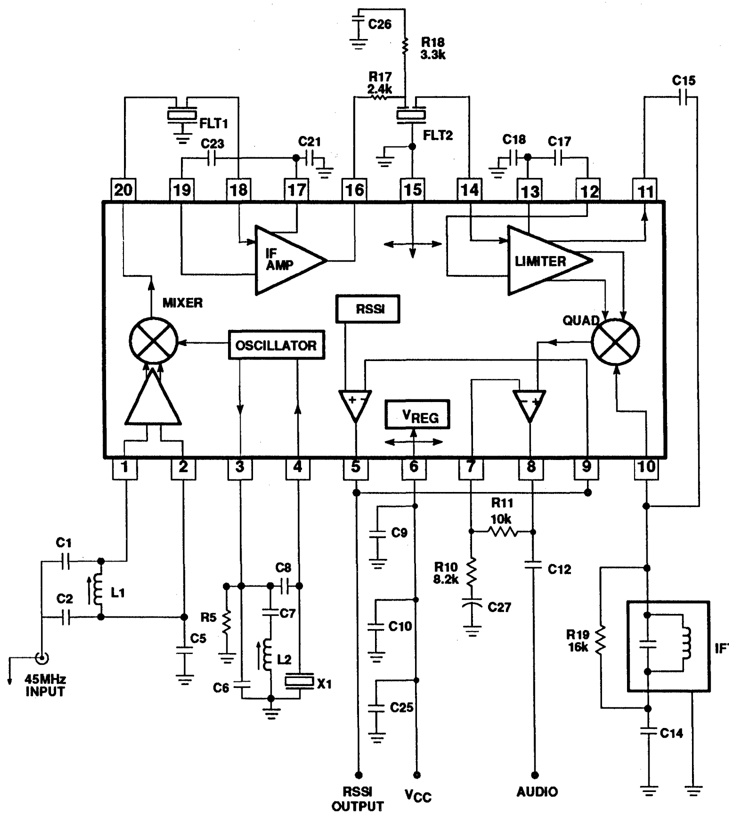
Low-voltage high performance mixer FM IF system NE/SA606



Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
C7	1nF Ceramic	L1	147–160nH Coilcraft UNI-10/142-04J08S
C8	10.0pF NPO Ceramic	L2	0.8μH nominal
C9	100nF ±10% Monolithic Ceramic		Toko 292CNS-T1038Z
C10	15μF Tantalum (minimum)	X1	44.545MHz Crystal ICM4712701
C12	2.2μF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	8.2kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C23	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C26	100nF ±10% Monolithic Ceramic	R19	16kΩ

Figure 1. NE/SA606 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C12	2.2μF ±10% Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2μF Tantalum or Electrolytic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	16k ±5% 1/4W Carbon Composition

Figure 2. NE/SA606 45MHz Application Circuit

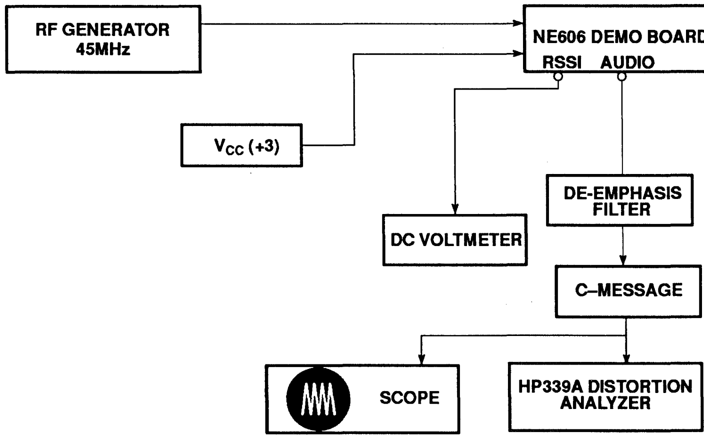


Figure 3. NE/SA606 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or −116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

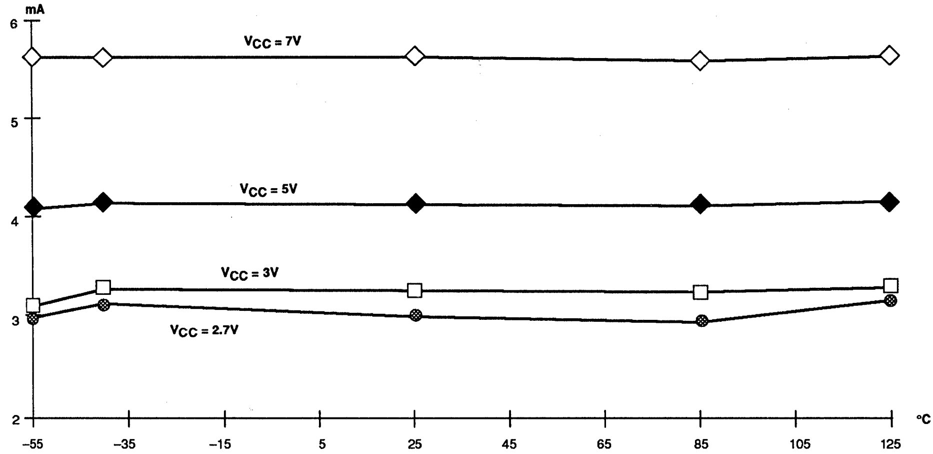


Figure 4. I_{CC} vs Temperature

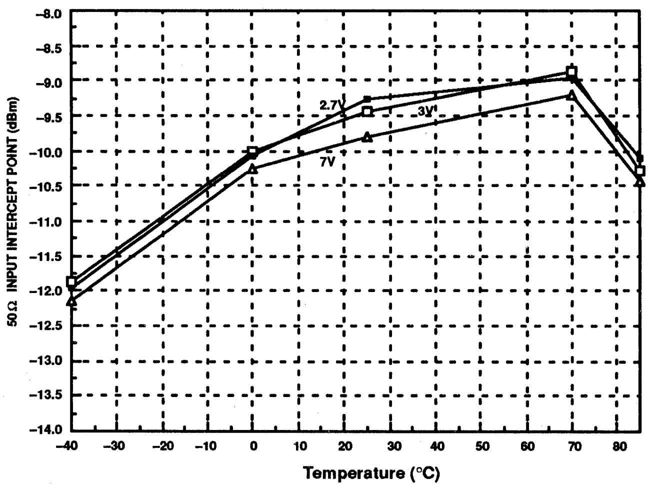


Figure 5. Third Order Intercept Point vs Supply Voltage

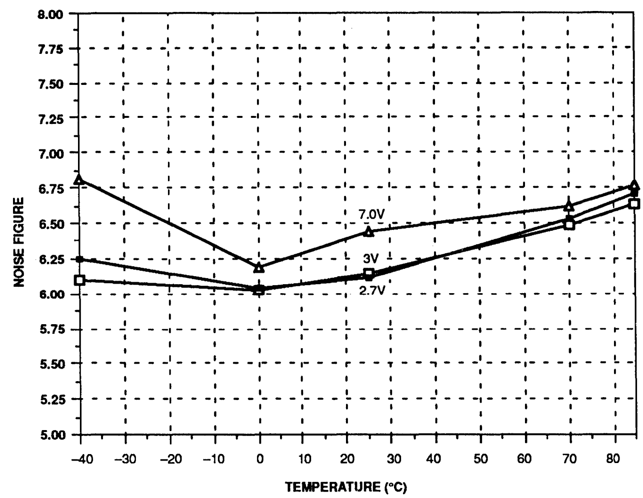


Figure 6. Mixer Noise Figure vs Supply Voltage

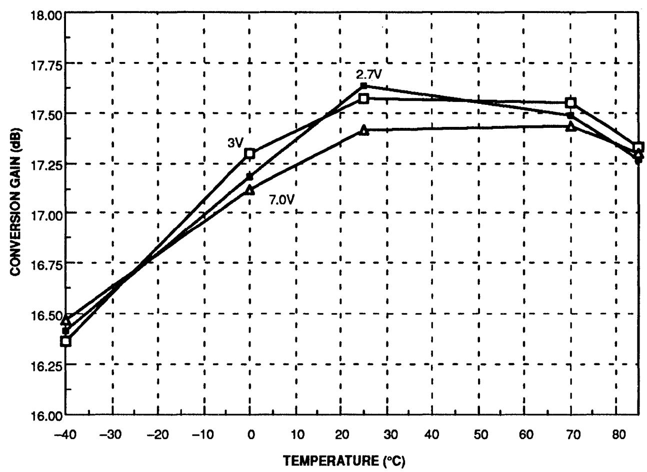
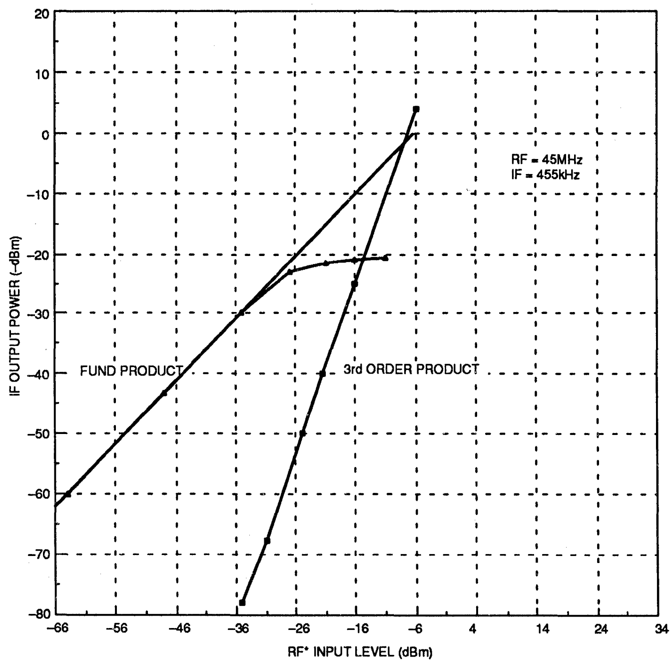


Figure 7. Conversion Gain vs Supply Voltage



*50Ω INPUT

Figure 8. Mixer Third Order Intercept and Compression

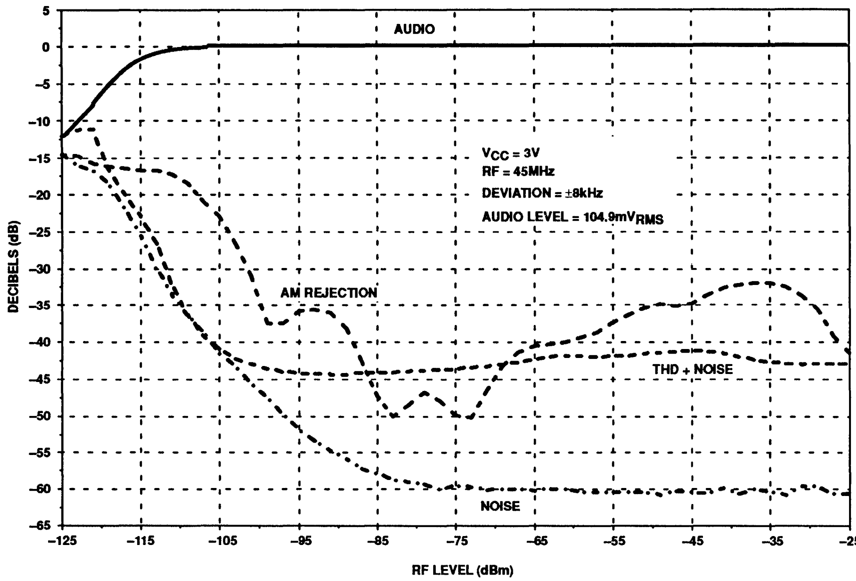


Figure 9. Sensitivity vs RF Level (–40°C)

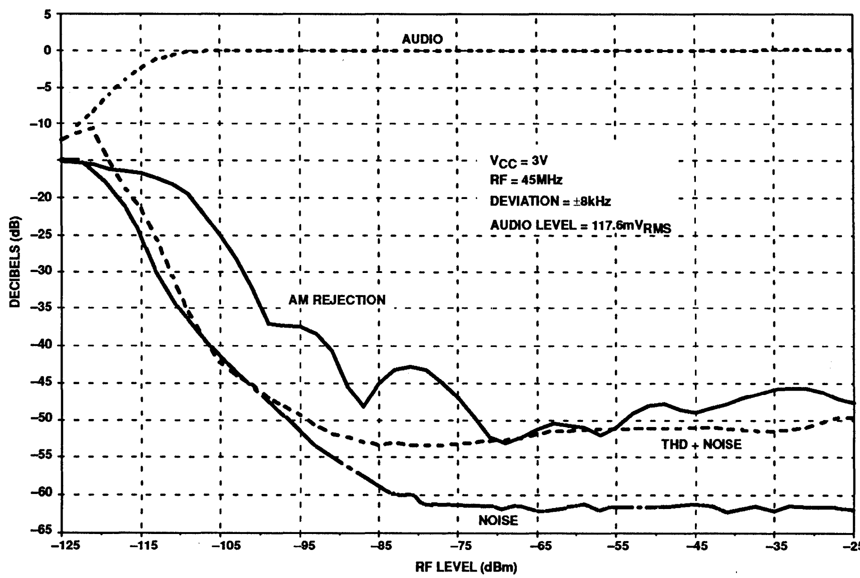


Figure 10. Sensitivity vs RF Level (+25°C)

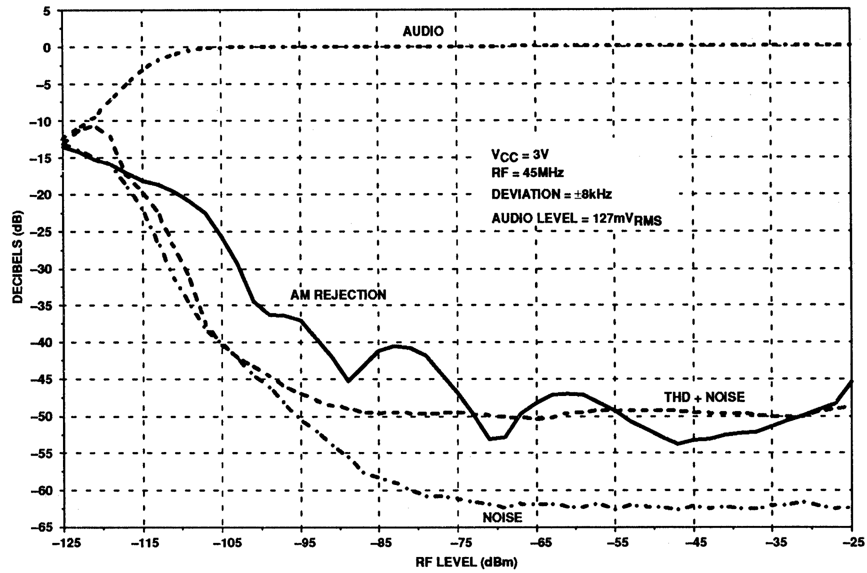


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

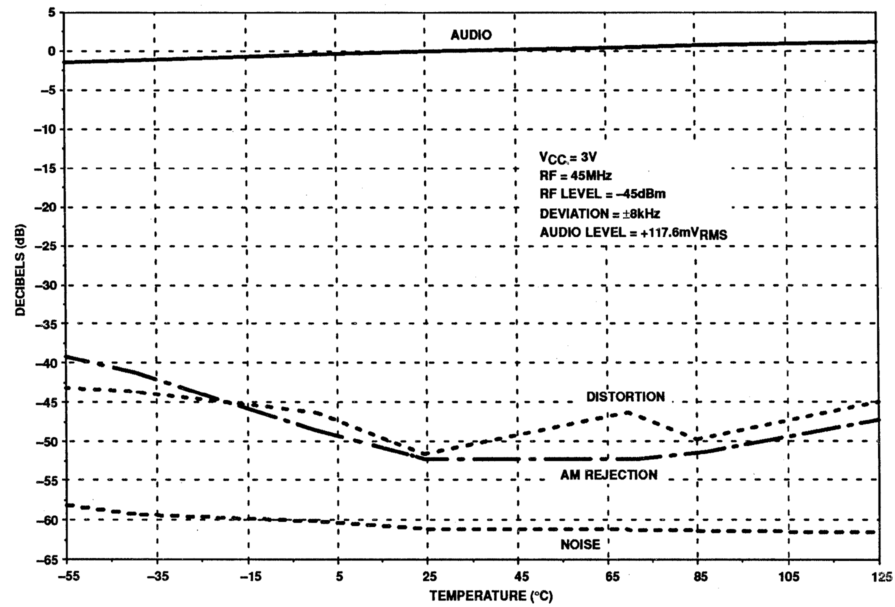


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

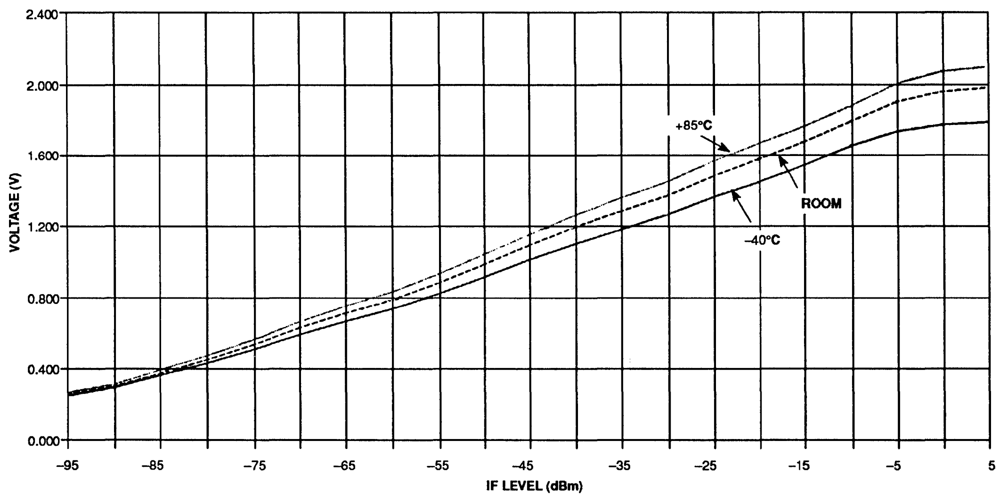


Figure 13. RSSI (455kHz IF @ 3V)

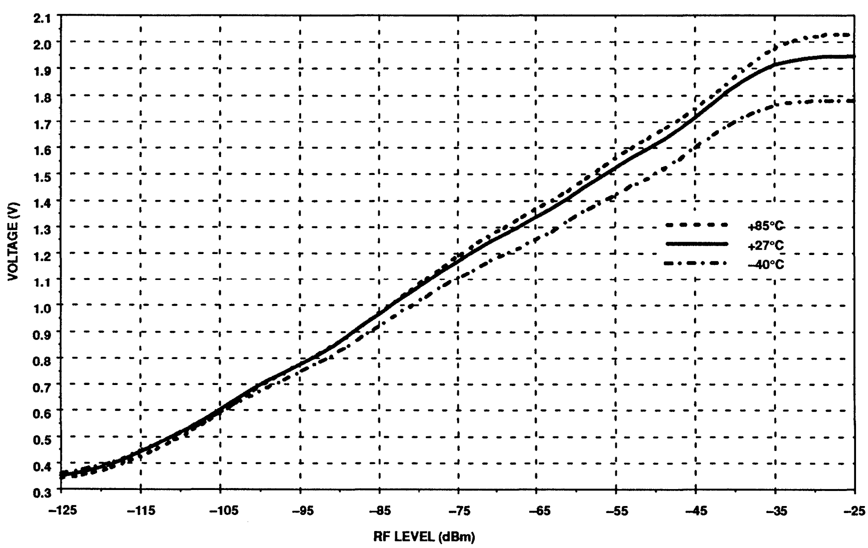


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

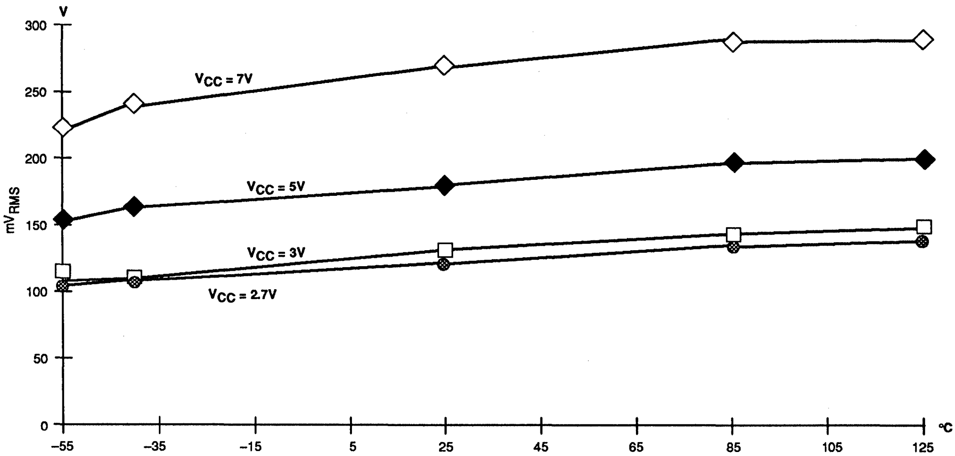
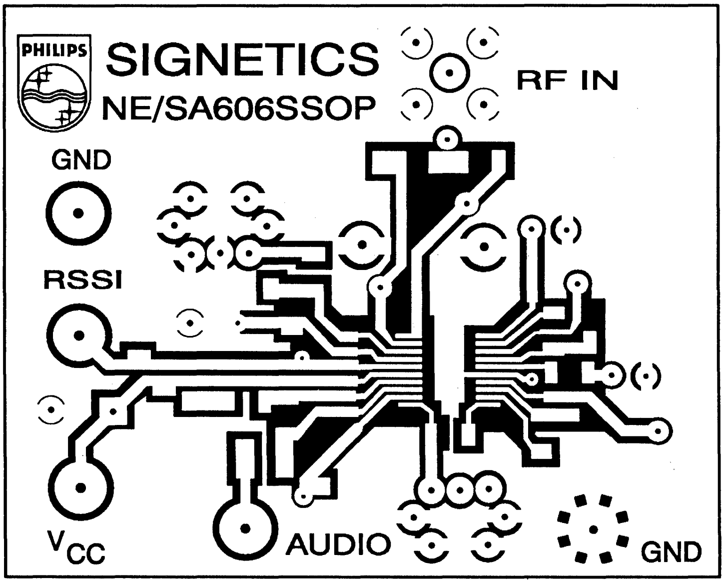


Figure 15. Audio Output vs Temperature



*Applies to Stand-Alone data sheets only.

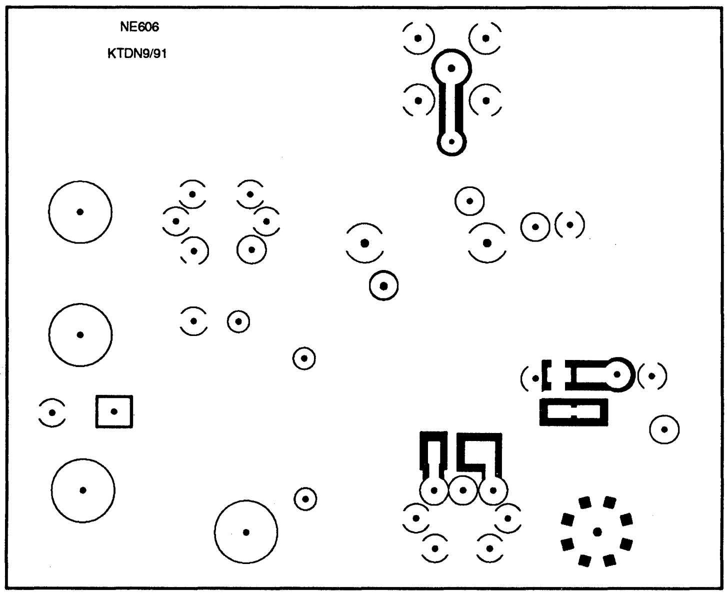
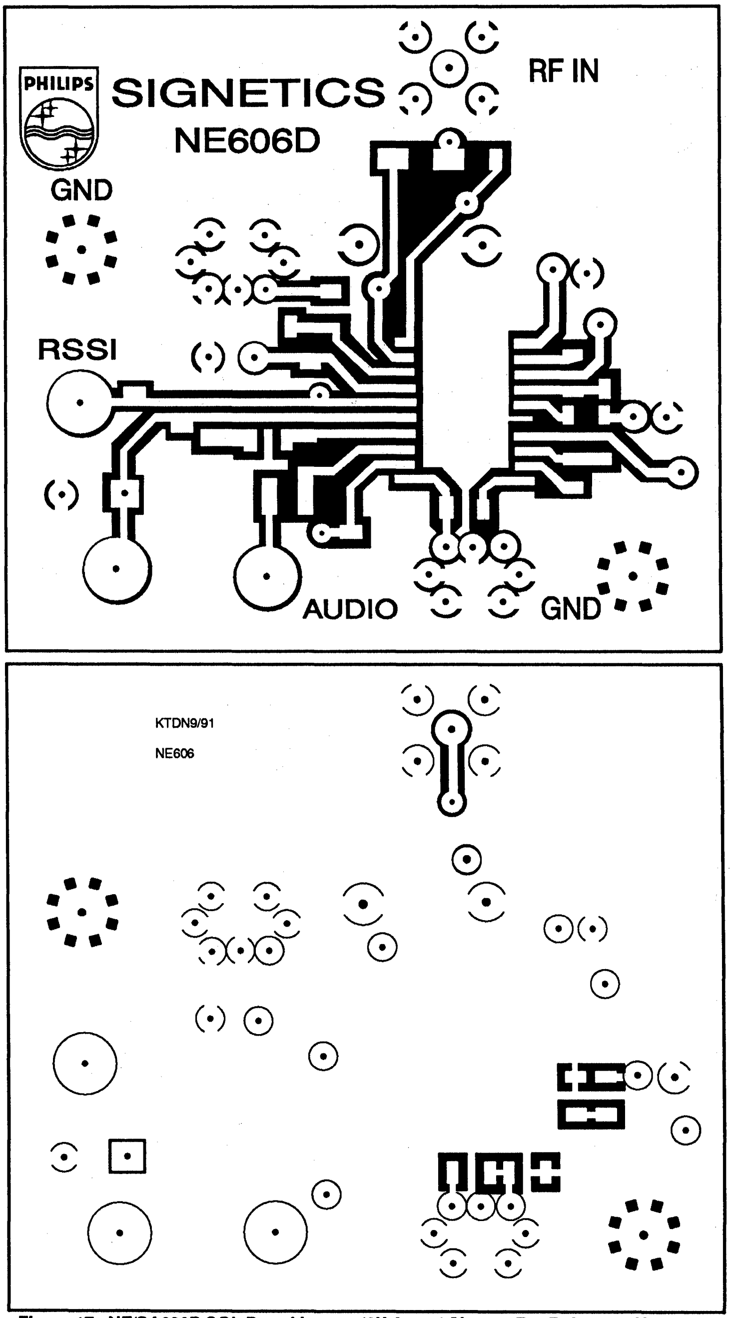
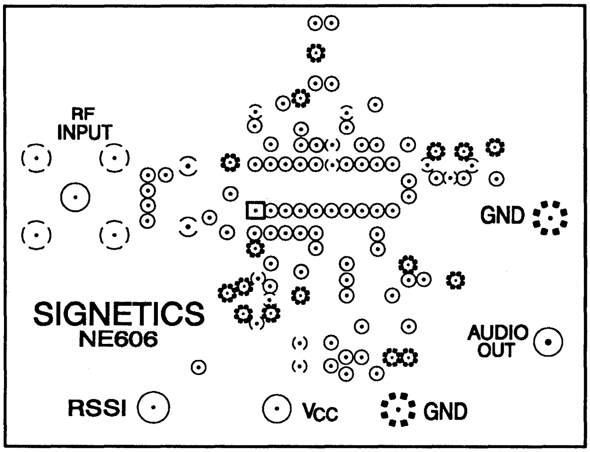


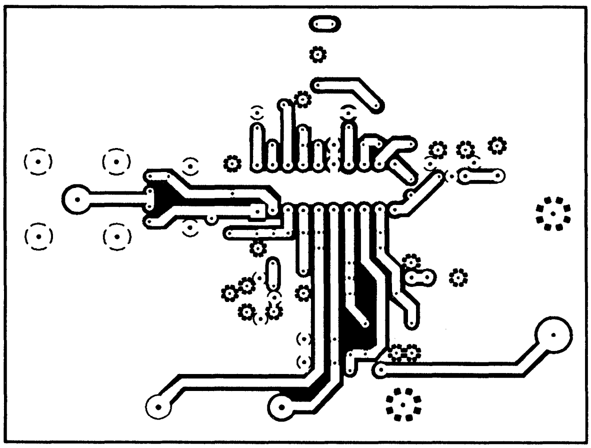
Figure 16. NE/SA606DK SSOP Board Layout (2X Actual Size* — For Reference Use Only)



*Applies to Stand-Alone data sheets only.

Figure 17. NE/SA606D SOL Board Layout (2X Actual Size* — For Reference Use Only)





*Applies to Stand-Alone data sheets only.

Figure 18. NE/SA606N DIP Board Layout (Actual Size* — For Reference Use Only)

Low-voltage high performance mixer FM IF system

NE/SA616

DESCRIPTION

The NE/SA616 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The NE/SA616 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The NE616 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE615. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to adjust the output levels or add filtering.

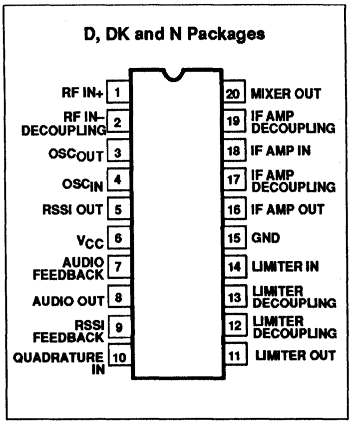
FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 80dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA616 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV, Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

PIN CONFIGURATION



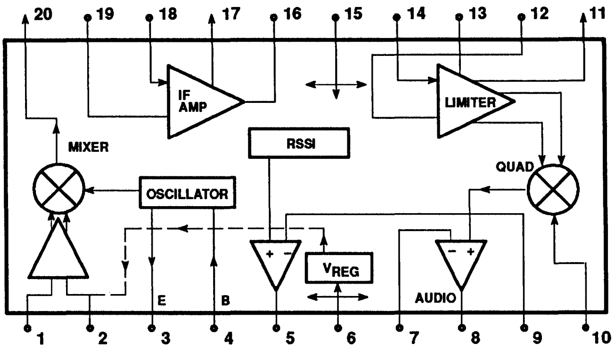
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE616N
20-Pin Plastic SOL (Surface-mount)	0 to +70°C	NE616D
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE616DK
20-Pin Plastic DIP	-40 to +85°C	SA616N
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA616D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA616DK

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range NE616	0 to +70	°C
	SA616	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA616			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA616			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.8		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	11	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE616			
			MIN	TYP	MAX	
	Input limiting –3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		40		dB
	Audio level	Gain of two (2kΩ AC load)	60	114		mV
	SINAD sensitivity	IF level –110dBm		13		dB
THD	Total harmonic distortion		–30	–45		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	.80	V
		IF level = –68dBm	.70	1.1	2	V
		IF level = –23dBm	1.0	1.8	2.50	V
	RSSI range			80		dB
	RSSI accuracy			±2		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (Int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		240		mV_{RMS}
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA616 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA616 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA616 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

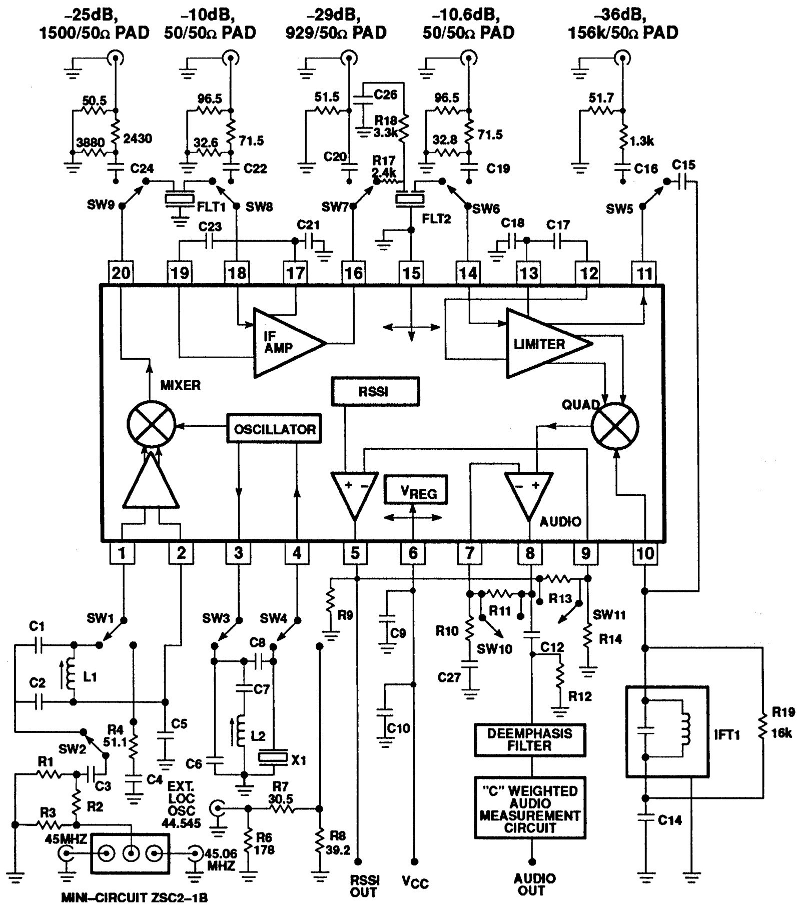
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 2kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

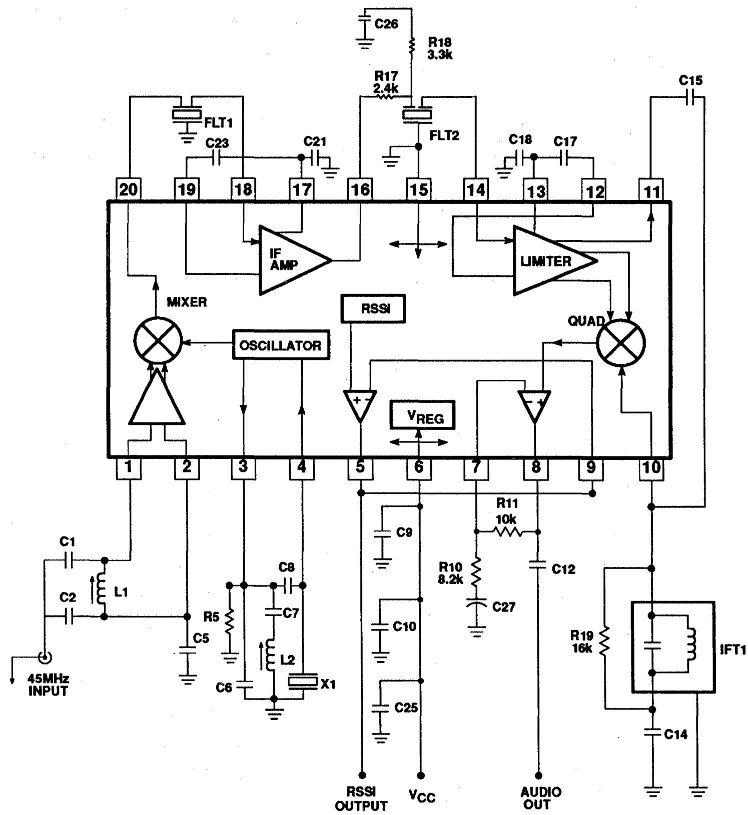
NOTE: dB(v) = 20log V_{OUT}/V_{IN}



Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C7	1nF Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C8	10.0pF NPO Ceramic	L2	0.8μH nominal
C9	100nF ±10% Monolithic Ceramic		Toko 292CNS–T1038Z
C10	15μF Tantalum (minimum)	X1	44.545MHz Crystal ICM4712701
C12	2.2μF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	8.2kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C23	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C26	100nF ±10% Monolithic Ceramic	R19	16kΩ

Figure 1. NE/SA616 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic	C26	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C27	2.2μF Tantalum or Electrolytic
C5	100nF ±10% Monolithic Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C8	10.0pF NPO Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C9	100nF ±10% Monolithic Ceramic	L2	0.8μH nominal Toko 292CNS–T1038Z
C10	15μF Tantalum (minimum)		
C12	2.2μF ±10% Ceramic	X1	44.545MHz Crystal ICM4712701
C14	100nF ±10% Monolithic Ceramic	R5	Not Used in Application Board (see Note 8, pg 8)
C15	10pF NPO Ceramic	R10	8.2k ±5% 1/4W Carbon Composition
C17	100nF ±10% Monolithic Ceramic	R11	10k ±5% 1/4W Carbon Composition
C18	100nF ±10% Monolithic Ceramic	R17	2.4k ±5% 1/4W Carbon Composition
C21	100nF ±10% Monolithic Ceramic	R18	3.3k ±5% 1/4W Carbon Composition
C23	100nF ±10% Monolithic Ceramic	R19	16k ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic		

Figure 2. NE/SA616 45MHz Application Circuit

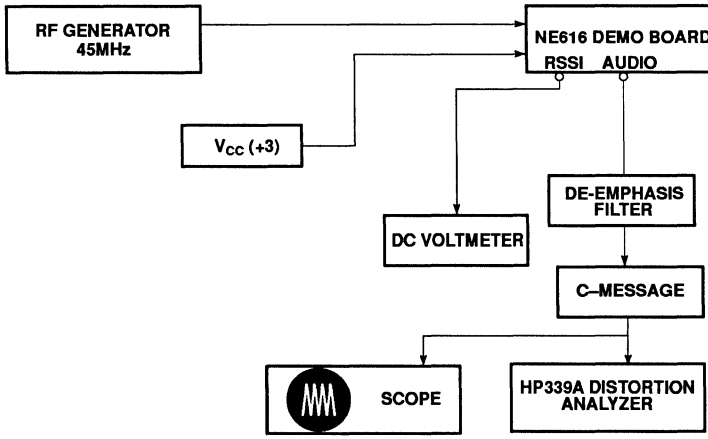


Figure 3. NE/SA616 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

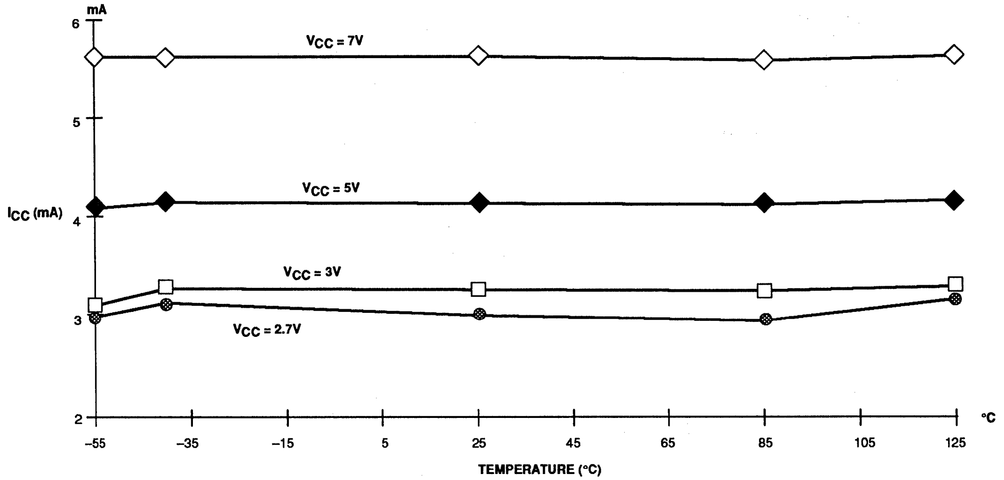


Figure 4. I_{CC} vs Temperature

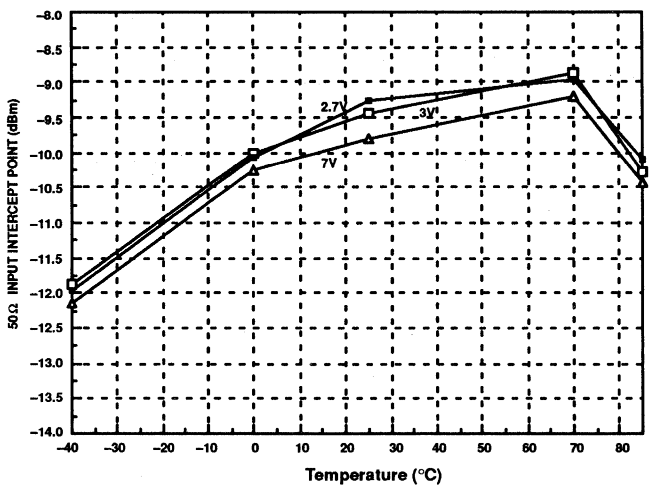


Figure 5. Third Order Intercept Point vs Supply Voltage

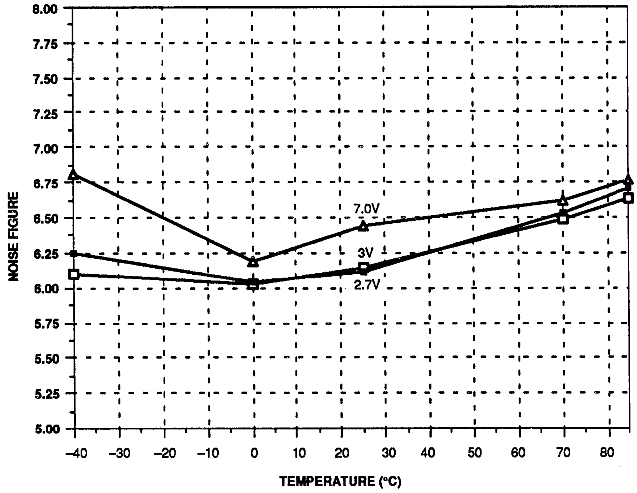


Figure 6. Mixer Noise Figure vs Supply Voltage

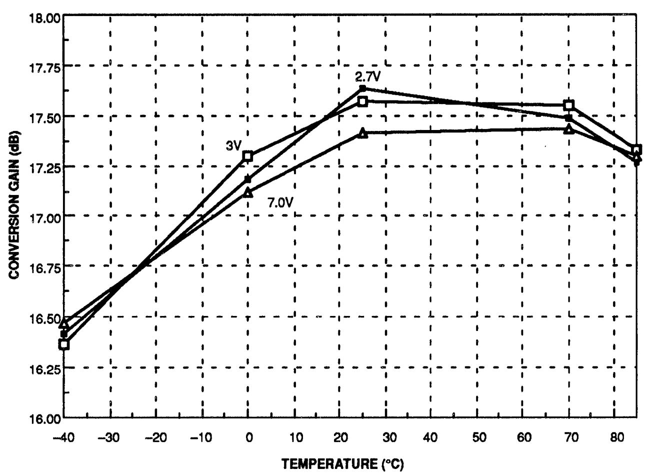


Figure 7. Conversion Gain vs Supply Voltage

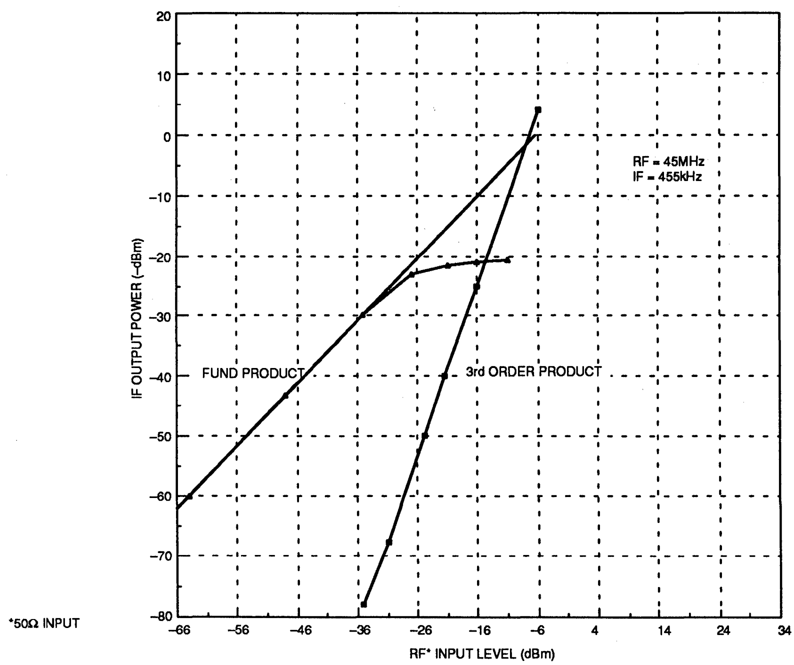


Figure 8. Mixer Third Order Intercept and Compression

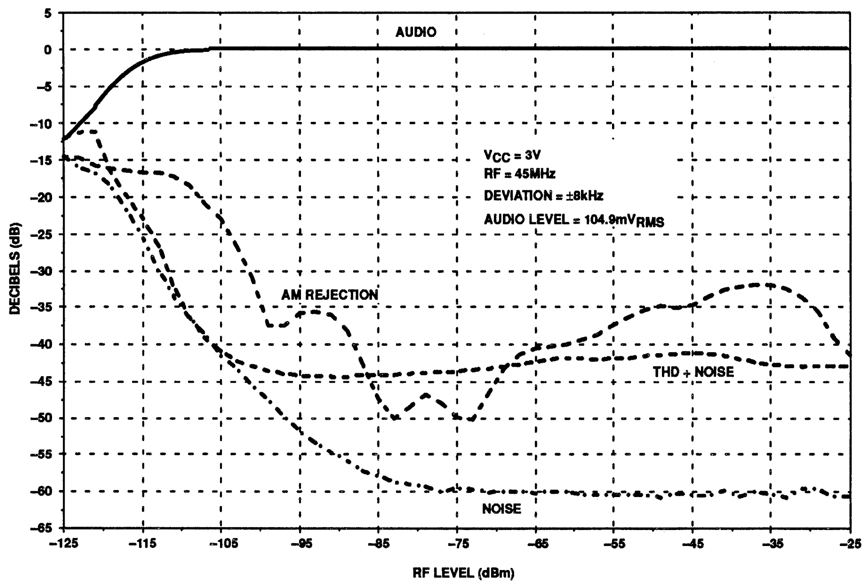


Figure 9. Sensitivity vs RF Level (–40°C)

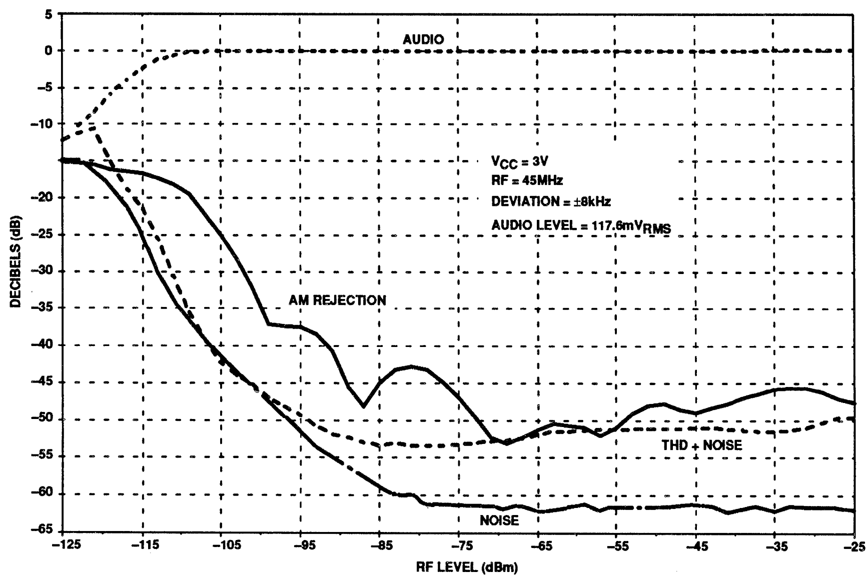


Figure 10. Sensitivity vs RF Level (+25°C)

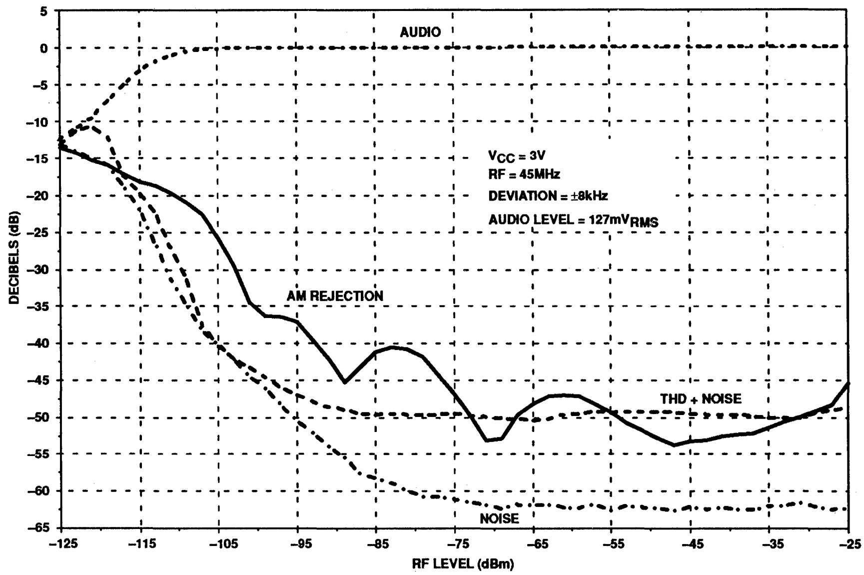


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

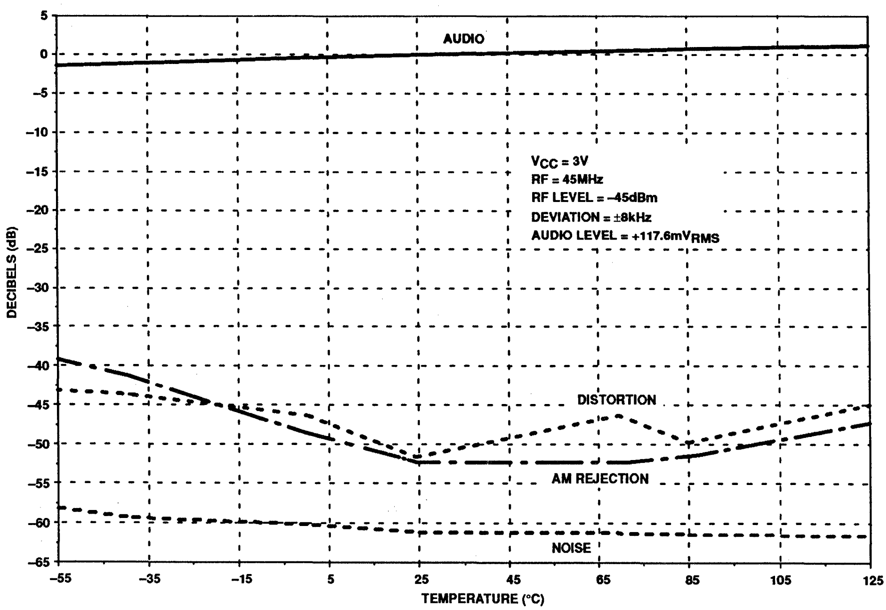


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

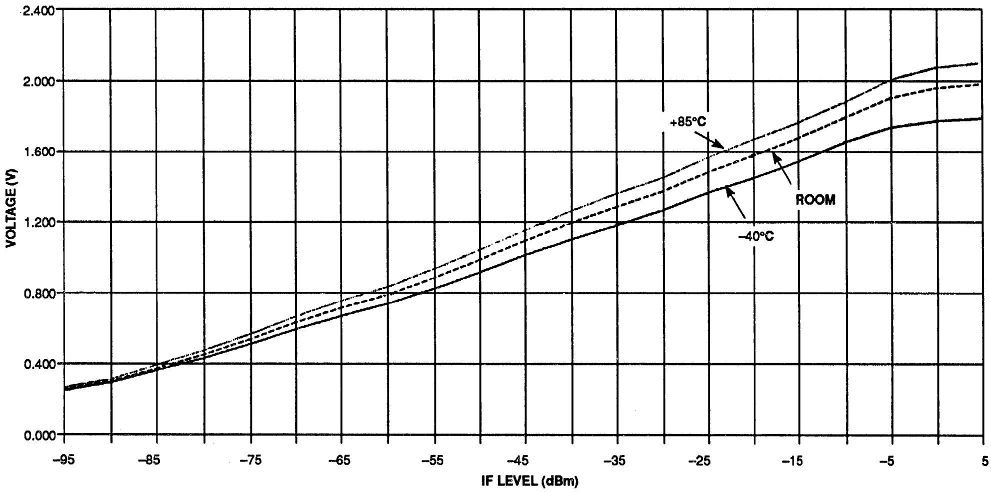


Figure 13. RSSI (455kHz IF @ 3V)

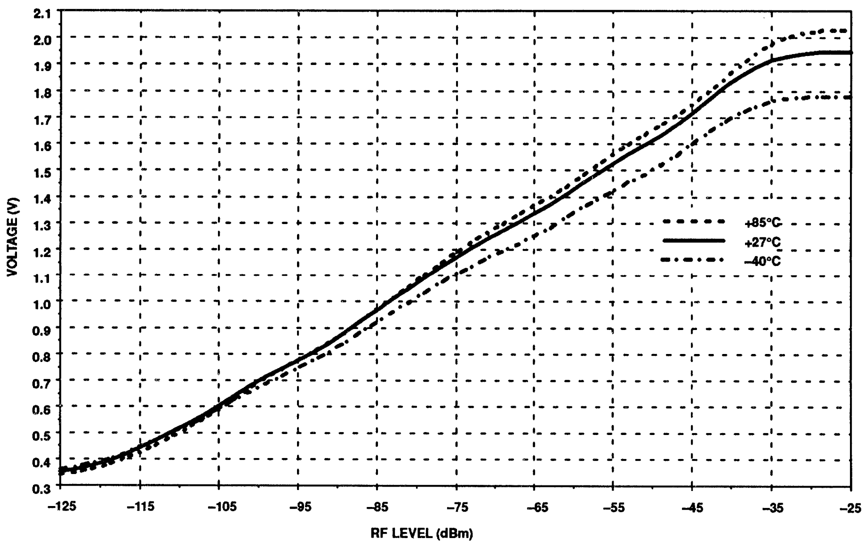


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

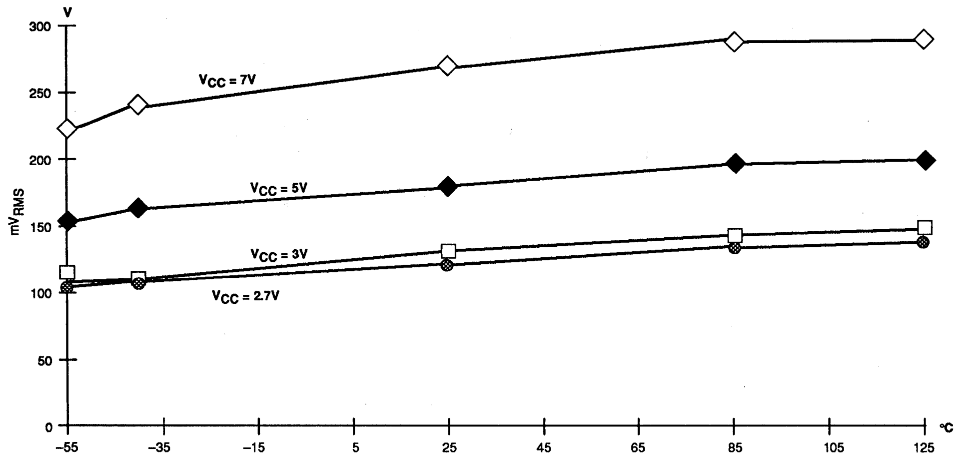
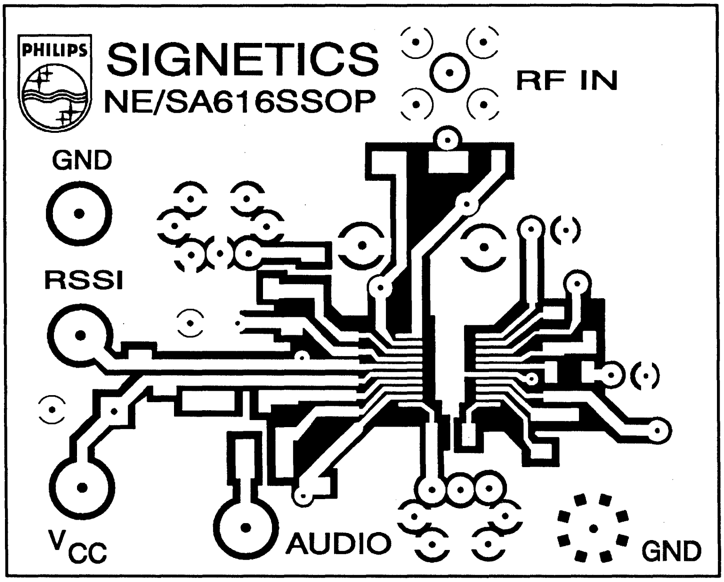


Figure 15. Audio Output vs Temperature



*Applies to Stand-Alone data sheets only.

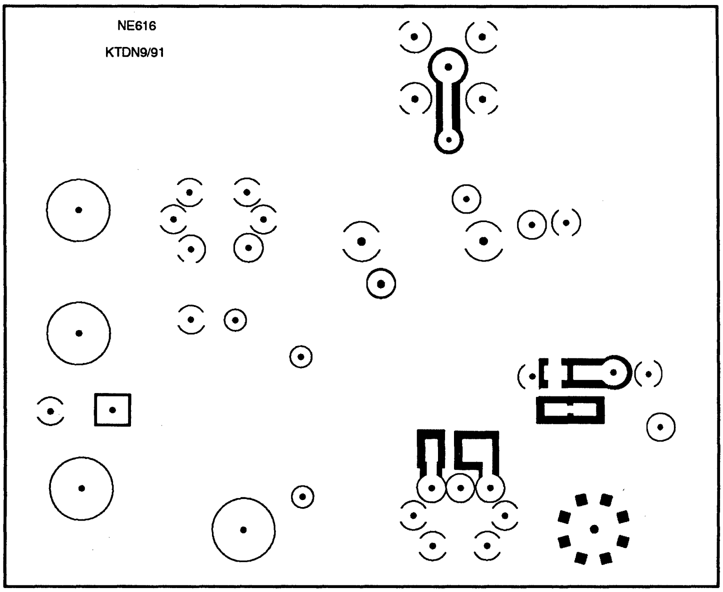
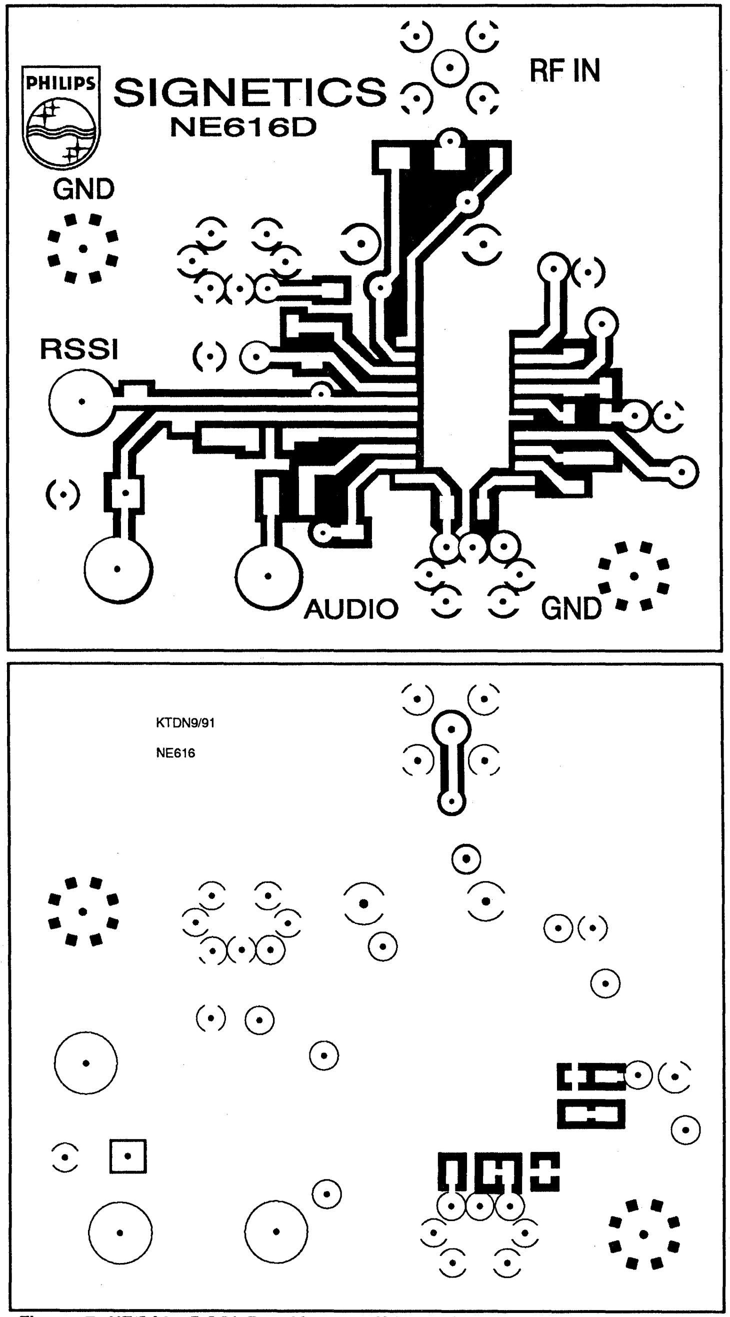
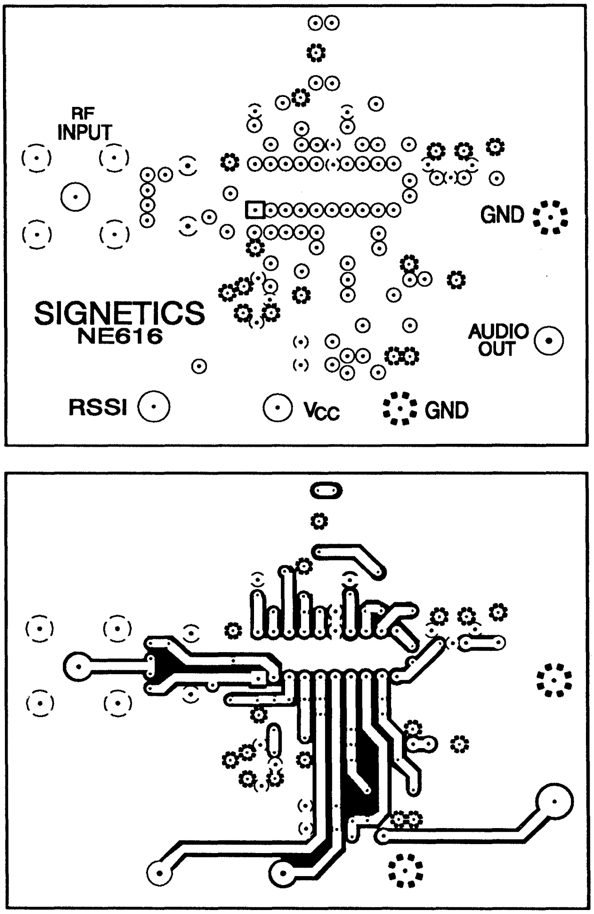


Figure 16. NE/SA616DK SSOP Board Layout (2X Actual Size* — For Reference Use Only)



*Applies to Stand-Alone data sheets only.

Figure 17. NE/SA616D SOL Board Layout (2X Actual Size* — For Reference Use Only)



*Applies to Stand-Alone data sheets only.

Figure 18. NE/SA616N DIP Board Layout (Actual Size* — For Reference Use Only)

Low voltage high performance mixer FM IF system

NE/SA607

DESCRIPTION

The NE/SA607 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The NE/SA607 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The NE607 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The NE607 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

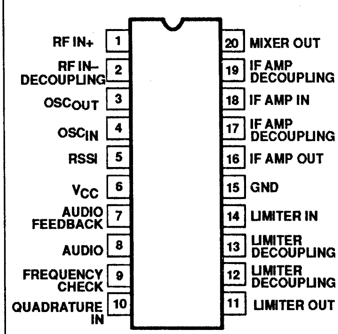
FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA607 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

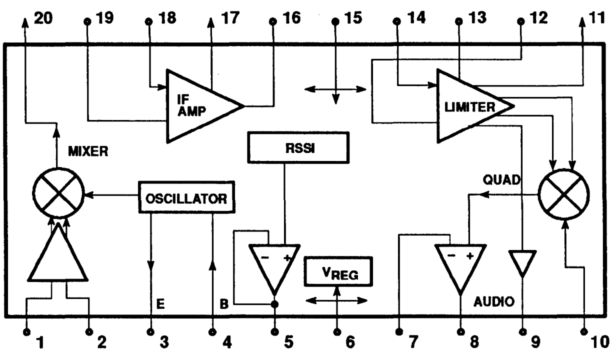
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE607N
20-Pin Plastic SOL (Surface-mount)	0 to +70°C	NE607D
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE607DK
20-Pin Plastic DIP	-40 to +85°C	SA607N
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA607D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA607DK

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range NE607	0 to +70	°C
	SA607	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA607			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA607			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	114	160	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output voltage	(Pin 11)		130		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		240		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA607 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA607 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA607 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

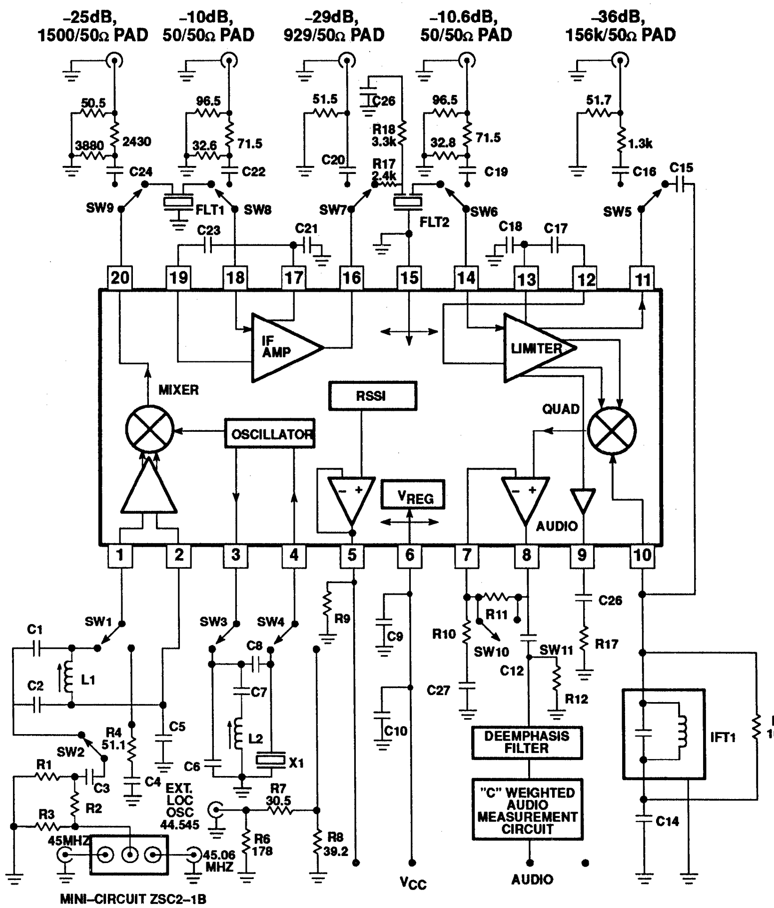
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 2kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

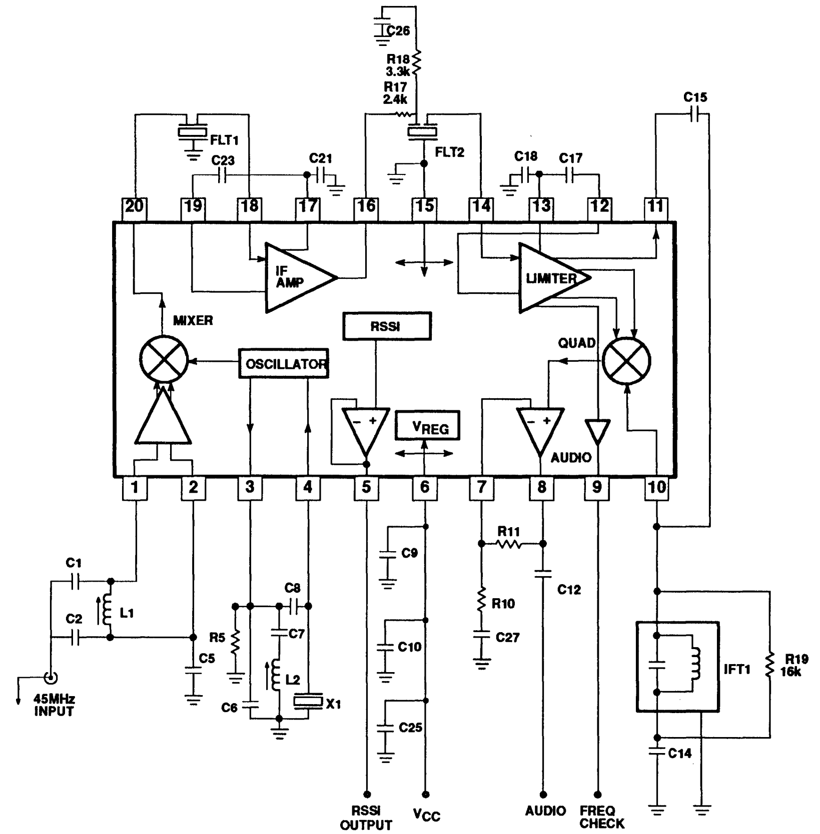
NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C26	0.1μF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C27	2.2μF
C5	100nF ±10% Monolithic Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
C8	10.0pF NPO Ceramic	L1	147–160nH Coilcraft UNI-10/142-04J08S
C9	100nF ±10% Monolithic Ceramic	L2	3.3μH nominal Toko 292CNS-T1046Z
C10	15μF Tantalum (minimum)	X1	44.545MHz Crystal ICM4712701
C12	2.2μF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	8.2kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C23	100nF ±10% Monolithic Ceramic	R18	3.3kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R19	16kΩ ±5% 1/4W Carbon Composition

Figure 1. NE/SA607 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C25	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C26	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	C27	2.2μF ±10% Monolithic Ceramic
C7	1nF Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C9	100nF ±10% Monolithic Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C10	15μF Tantalum (minimum)	L1	147–160nH Coilcraft UNI–10/142–04J08S
C12	2.2μF ±10% Ceramic	L2	0.8μH nominal Toko 292CNS–T1038Z
C14	100nF ±10% Monolithic Ceramic	X1	44.545MHz Crystal ICM4712701
C15	10pF NPO Ceramic	R5	Not Used in Application Board (see Note 8)
C17	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C18	100nF ±10% Monolithic Ceramic	R18	3.3kΩ ±5% 1/4W Carbon Composition
C21	100nF ±10% Monolithic Ceramic	R19	16kΩ ±5% 1/4W Carbon Composition

Figure 2. NE/SA607 45MHz Application Circuit

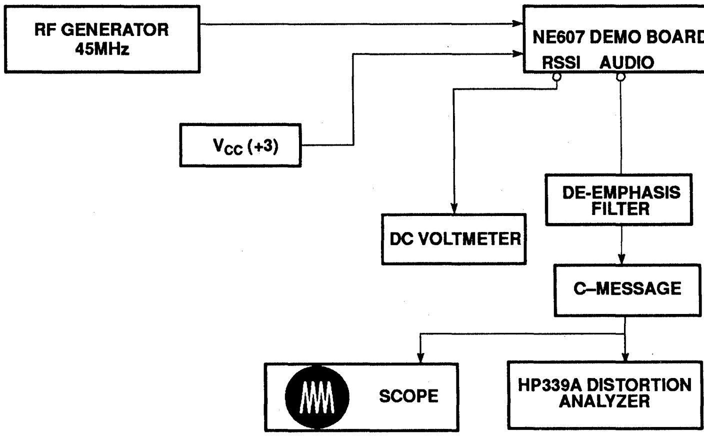


Figure 3. NE/SA607 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

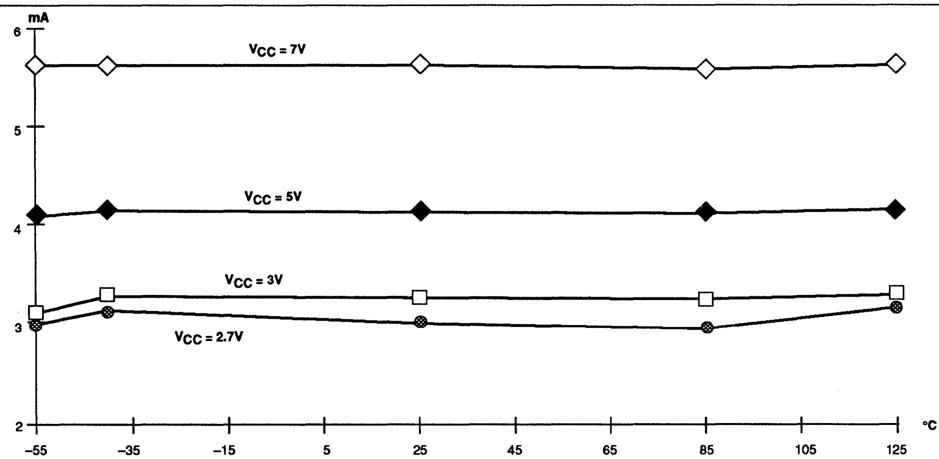


Figure 4. I_{CC} vs Temperature

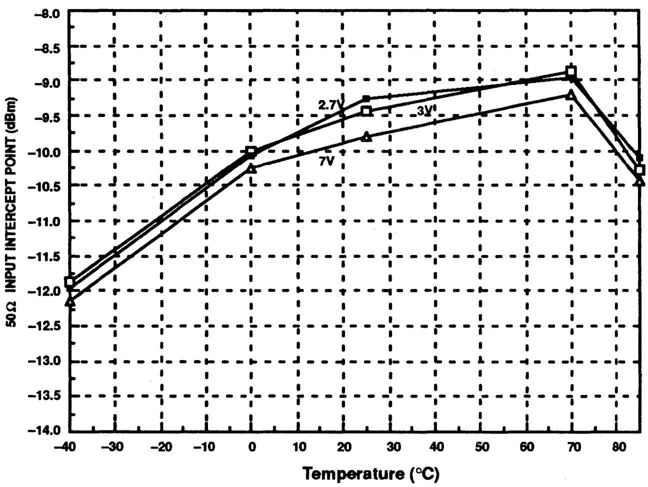


Figure 5. Third Order Intercept Point vs Supply Voltage

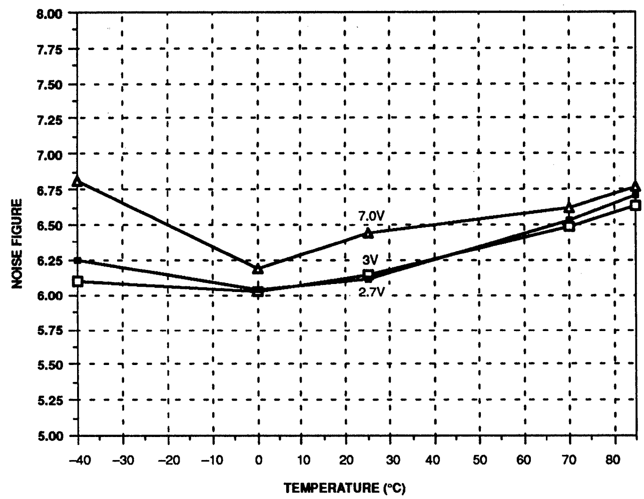


Figure 6. Mixer Noise Figure vs Supply Voltage

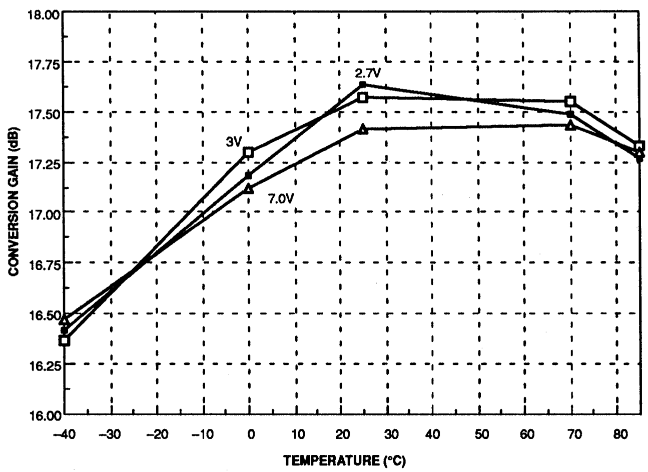


Figure 7. Conversion Gain vs Supply Voltage

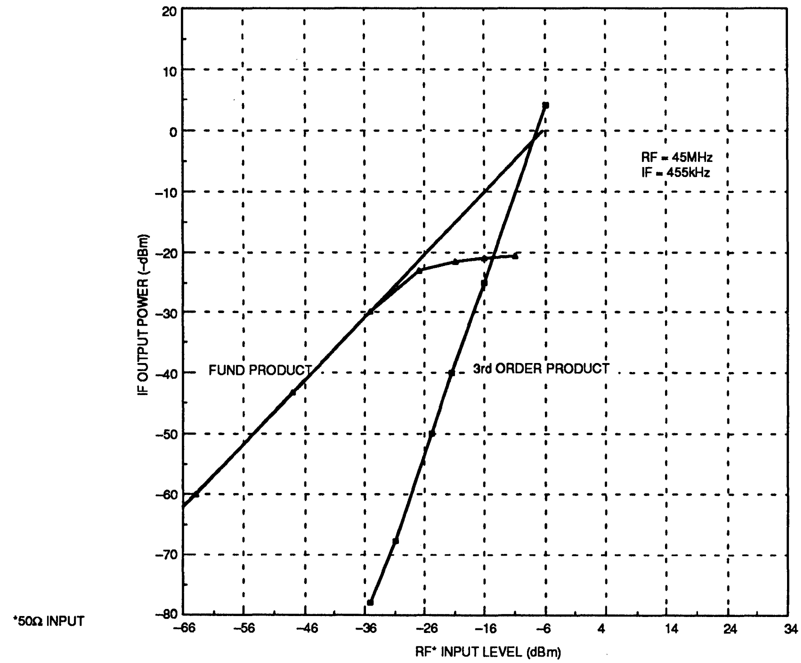


Figure 8. Mixer Third Order Intercept and Compression

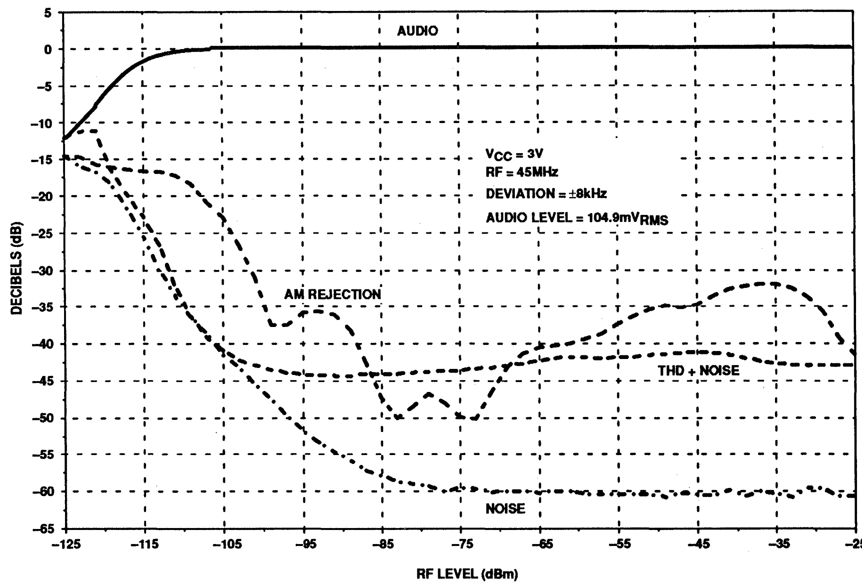


Figure 9. Sensitivity vs RF Level (–40°C)

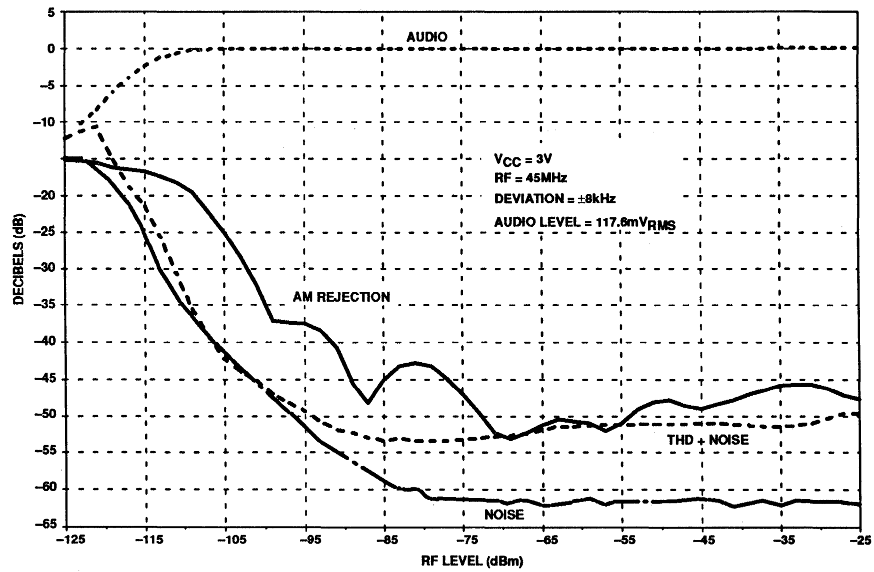


Figure 10. Sensitivity vs RF Level (+25°C)

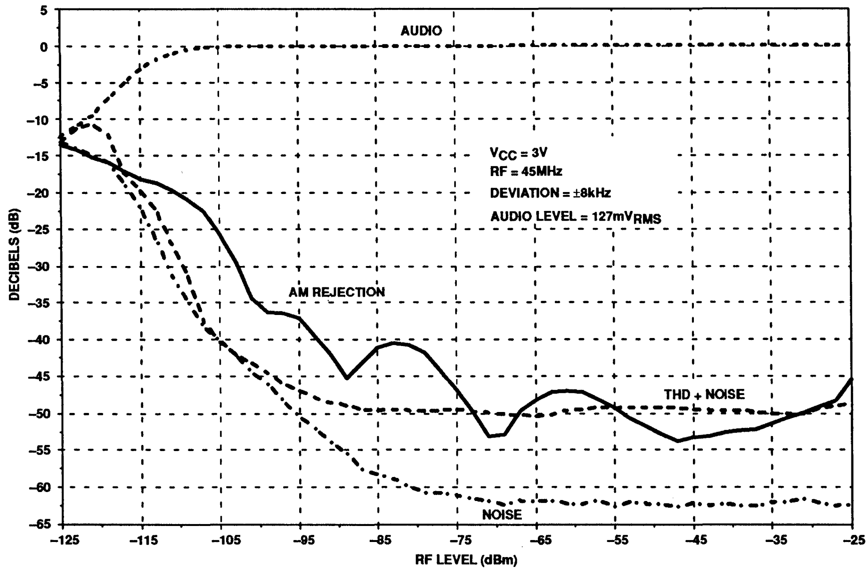


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

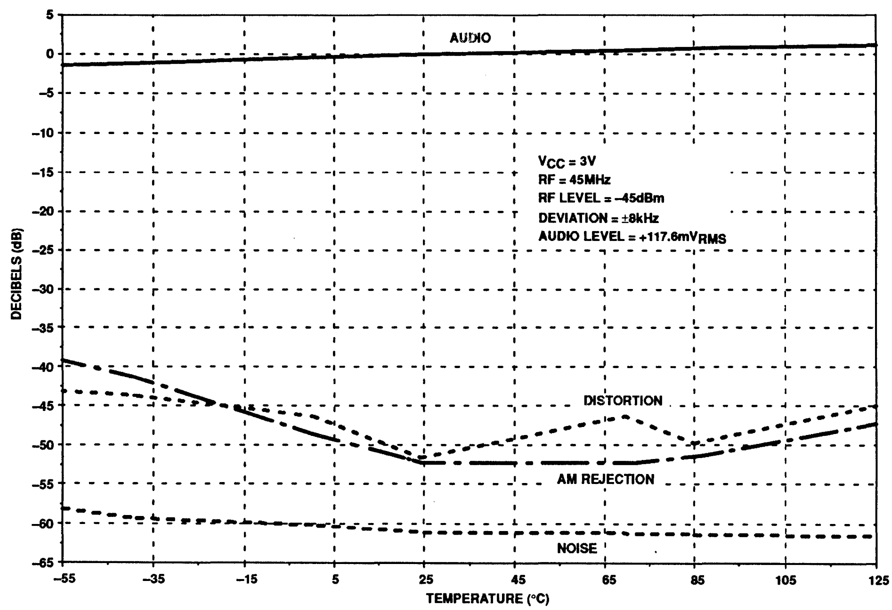


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

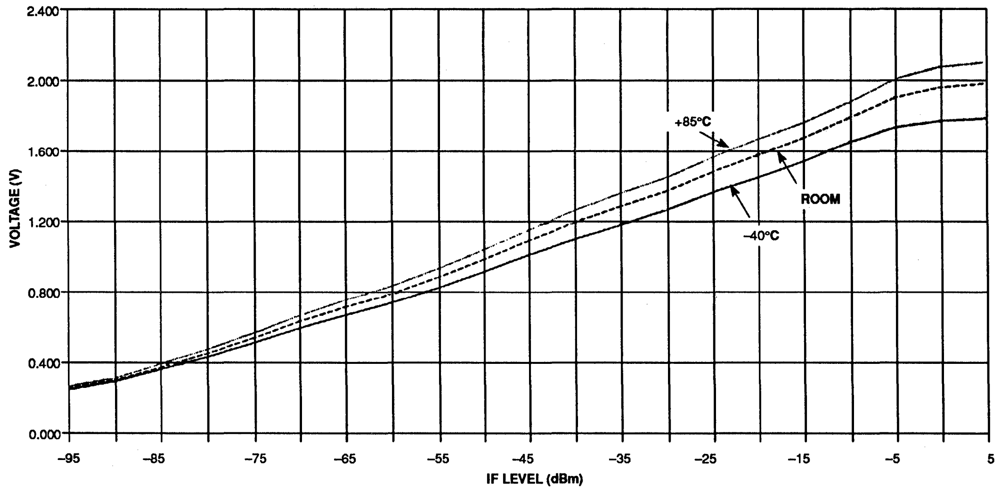


Figure 13. RSSI (455kHz IF @ 3V)

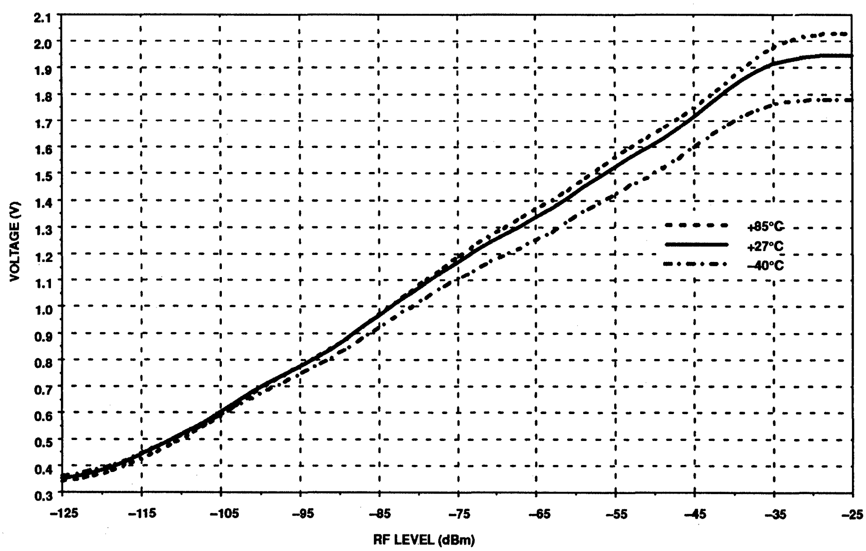


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

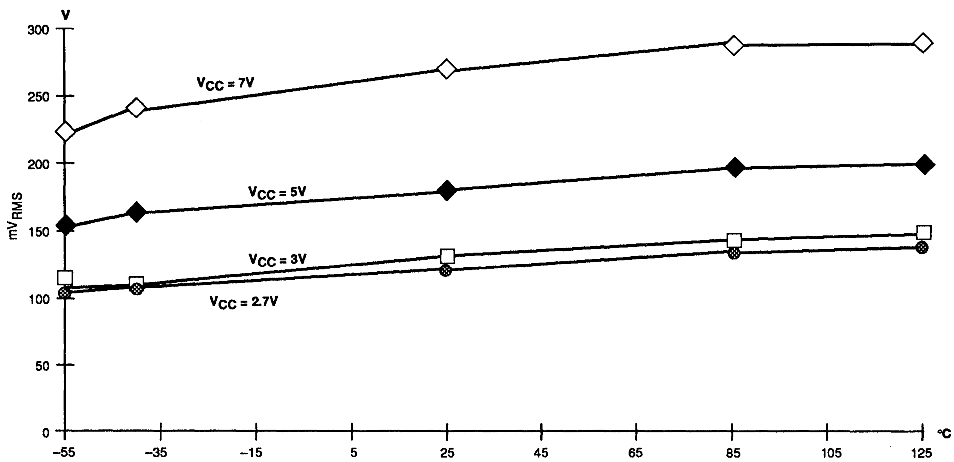


Figure 15. Audio Output vs Temperature

Low-voltage high performance mixer FM IF system — NE/SA617

DESCRIPTION

The NE/SA617 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The NE/SA617 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The NE617 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The NE617 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

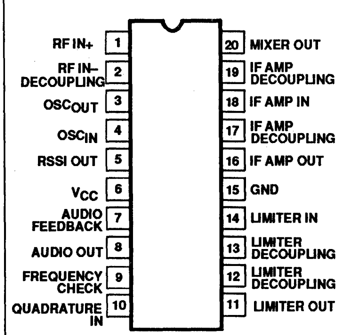
- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 80dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA617 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

PIN CONFIGURATION

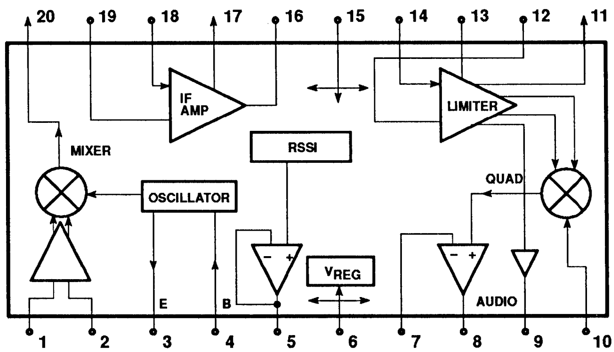
D, DK and N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE617N
20-Pin Plastic SOL (Surface-mount)	0 to +70°C	NE617D
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE617DK
20-Pin Plastic DIP	-40 to +85°C	SA617N
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA617D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA617DK

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

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V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range NE617	0 to +70	°C
	SA617	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA617 MIN	TYP	MAX	UNITS
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA617			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.8		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	11.0	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		40		dB
	Audio level	Gain of two (2kΩ AC load)	60	114		mV
	SINAD sensitivity	RF level –110dB		13		dB
THD	Total harmonic distortion		–30	–45		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	2.0	V
		IF level = –23dBm	1.0	1.8	2.5	V
	RSSI range			80		dB
	RSSI accuracy			±2.0		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		0.3		kΩ
	Limiter output voltage	(Pin 11)		130		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		240		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:
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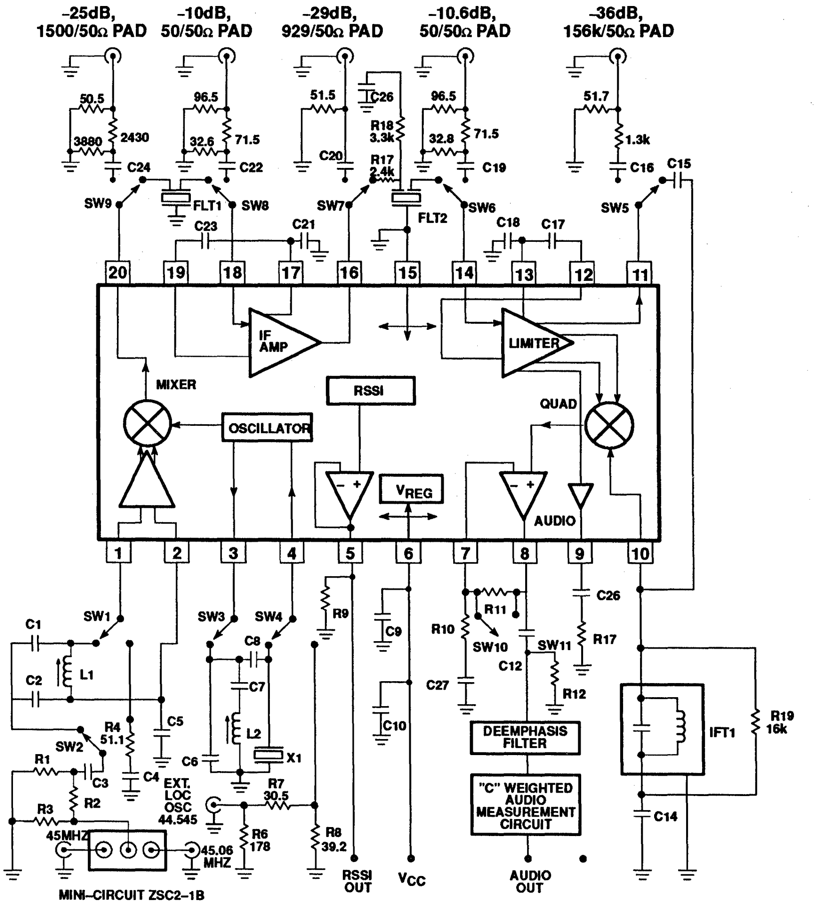
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 2kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

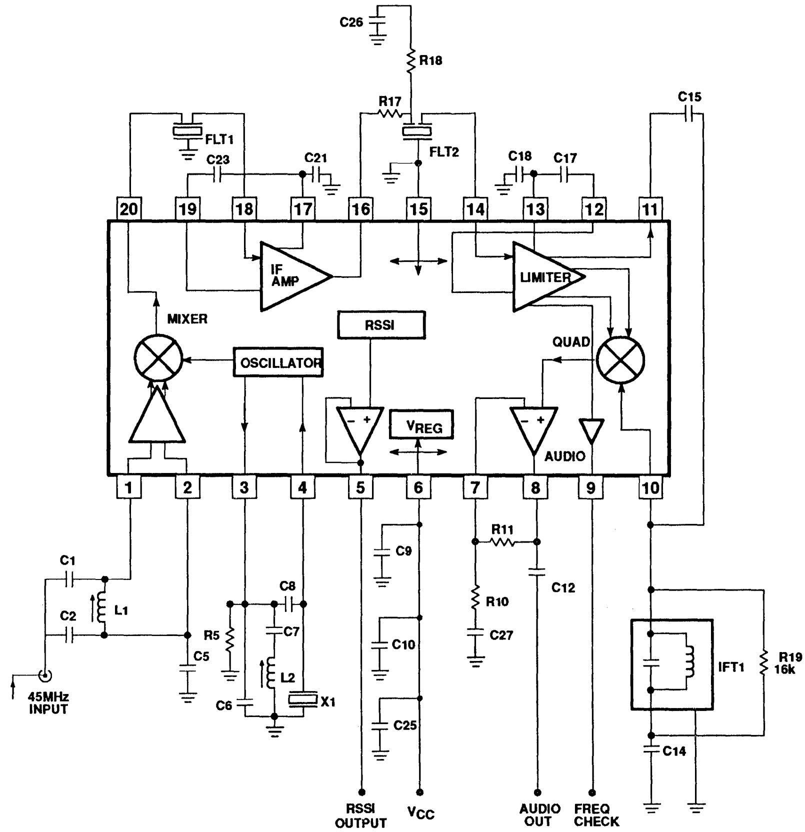
NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C26	0.1μF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C27	2.2μF
C5	100nF ±10% Monolithic Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C8	10.0pF NPO Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C9	100nF ±10% Monolithic Ceramic	L2	3.3μH nominal Toko 292CNS–T1046Z
C10	15μF Tantalum (minimum)	X1	44.545MHz Crystal ICM4712701
C12	2.2μF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	8.2kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C23	100nF ±10% Monolithic Ceramic	R18	3.3kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R19	16kΩ ±5% 1/4W Carbon Composition

Figure 1. NE/SA617 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C12	2.2μF ±10% Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2μF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8)
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

Figure 2. NE/SA617 45MHz Application Circuit

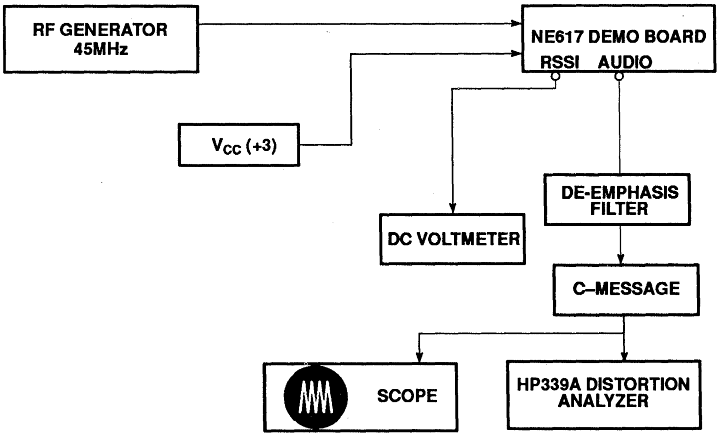


Figure 3. NE/SA617 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

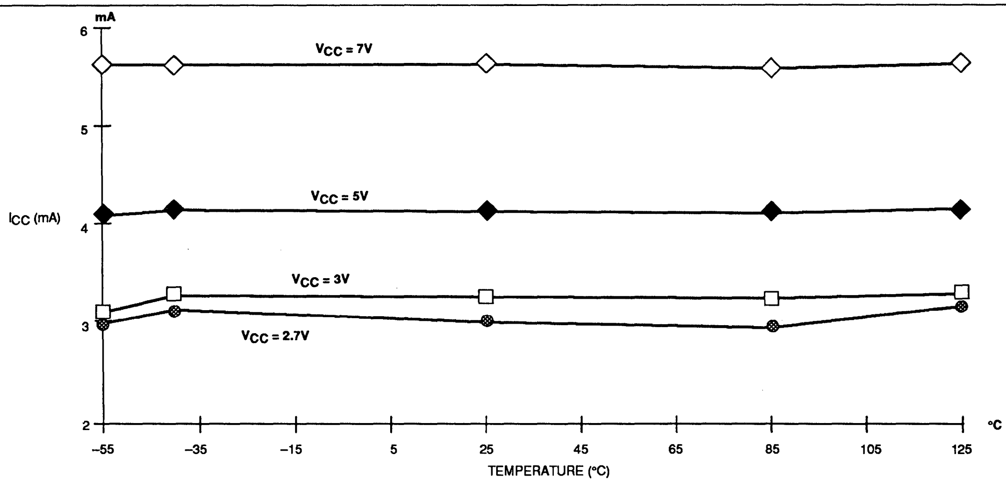


Figure 4. I_{CC} vs Temperature

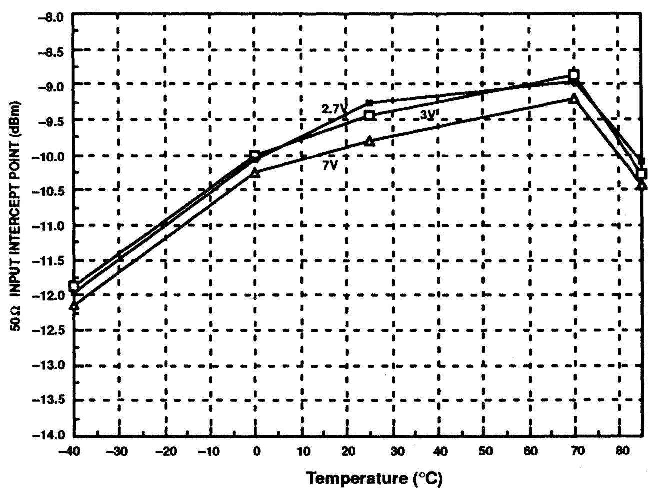


Figure 5. Third Order Intercept Point vs Supply Voltage

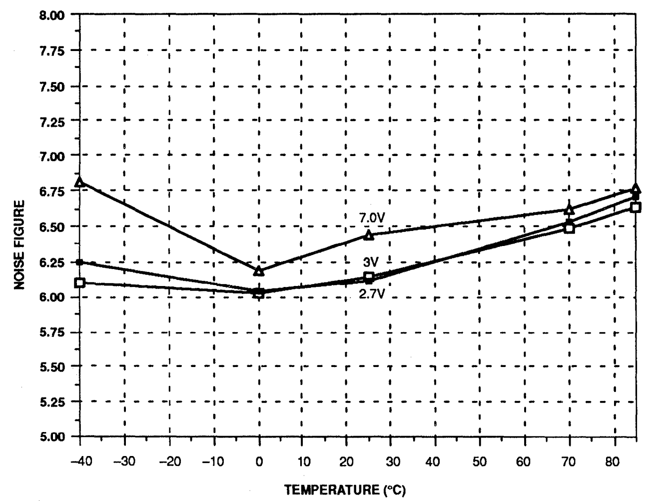


Figure 6. Mixer Noise Figure vs Supply Voltage

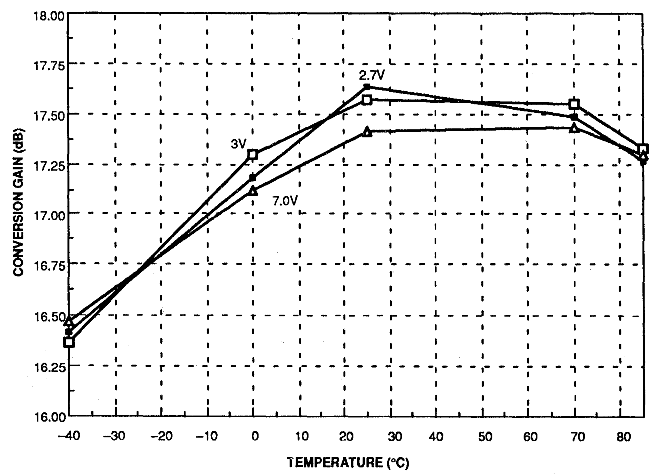


Figure 7. Conversion Gain vs Supply Voltage

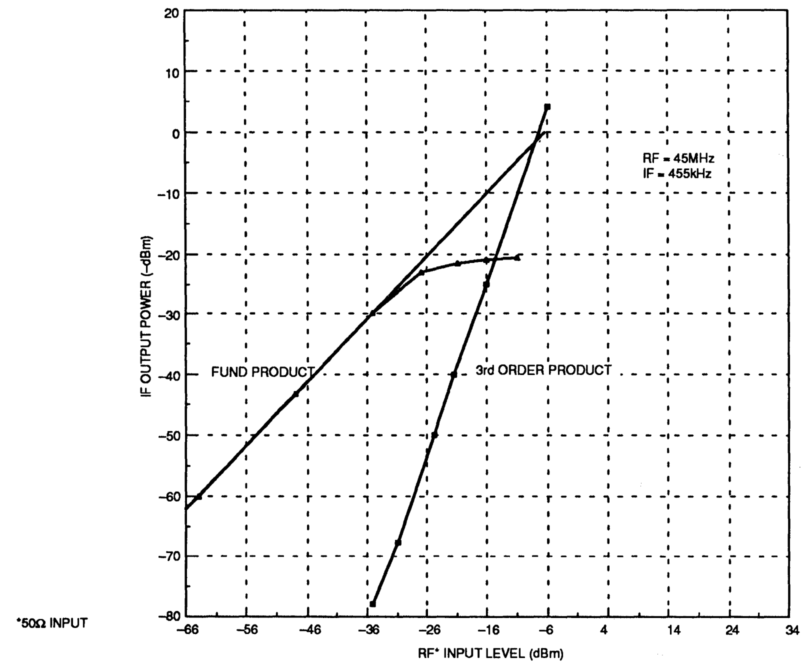


Figure 8. Mixer Third Order Intercept and Compression

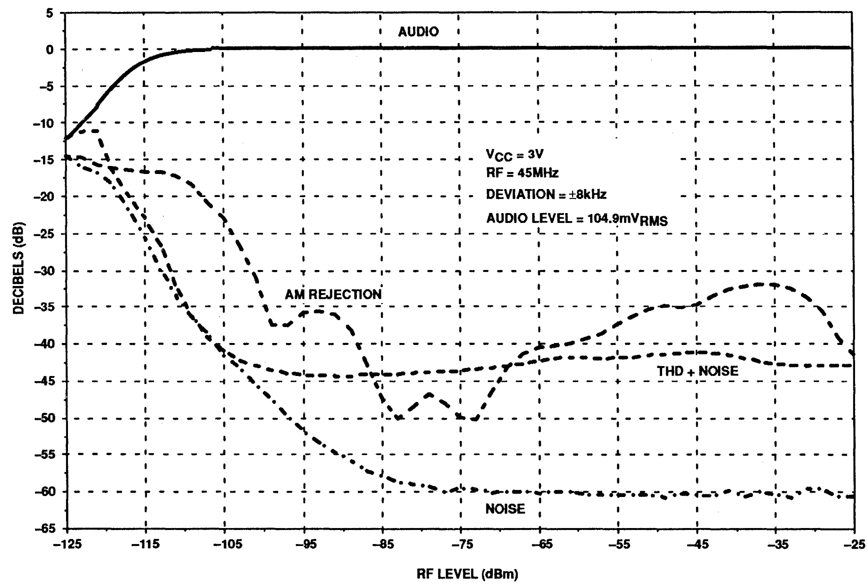


Figure 9. Sensitivity vs RF Level (–40°C)

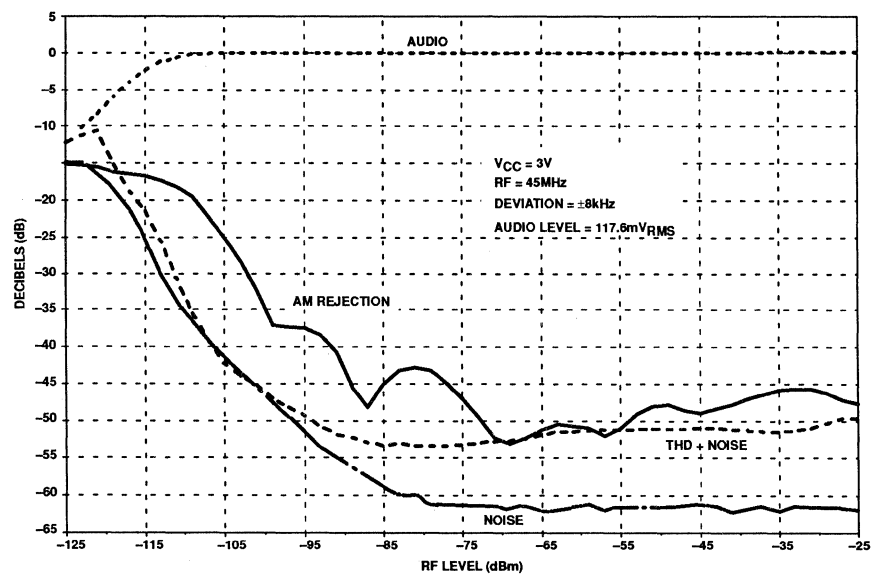


Figure 10. Sensitivity vs RF Level (+25°C)

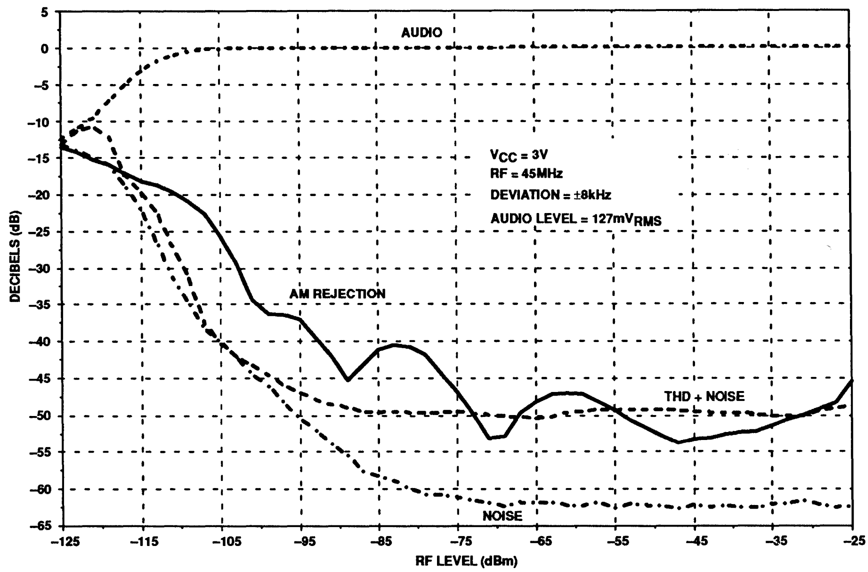


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

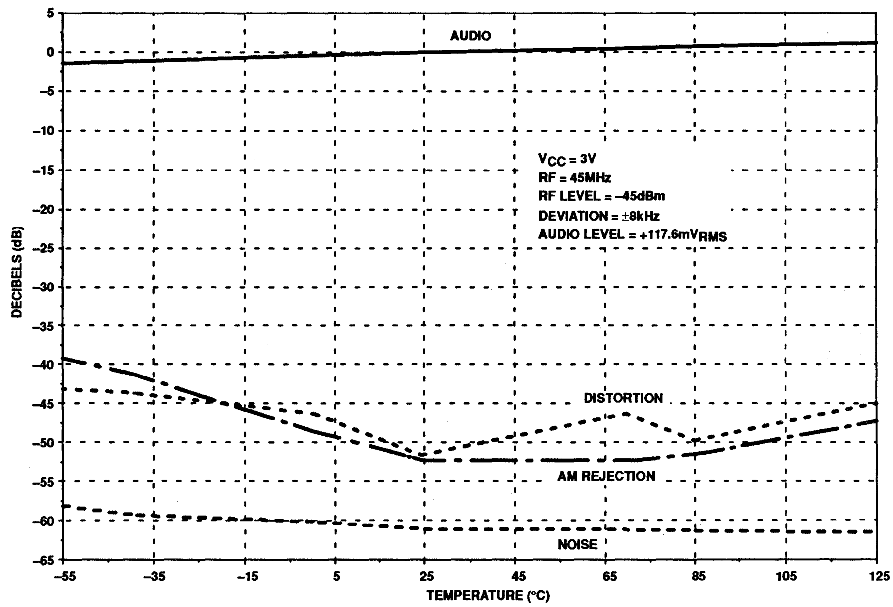


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

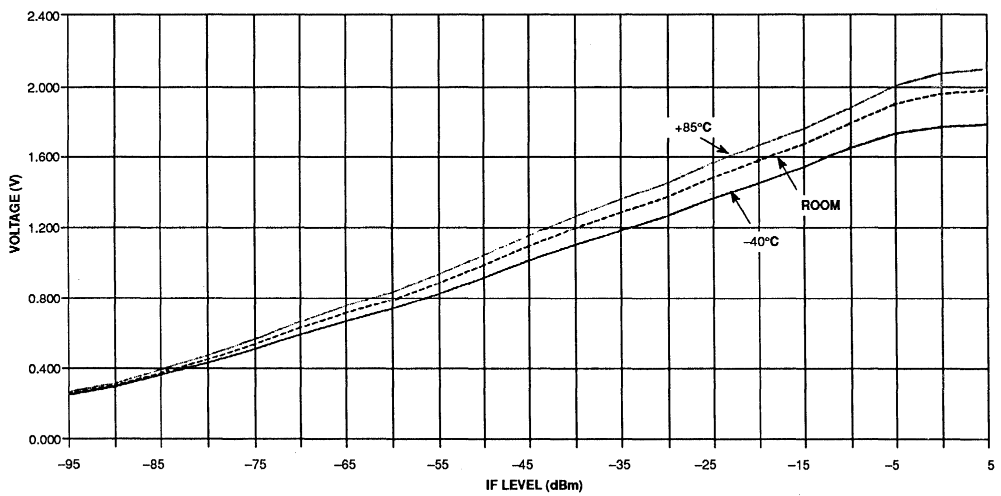


Figure 13. RSSI (455kHz IF @ 3V)

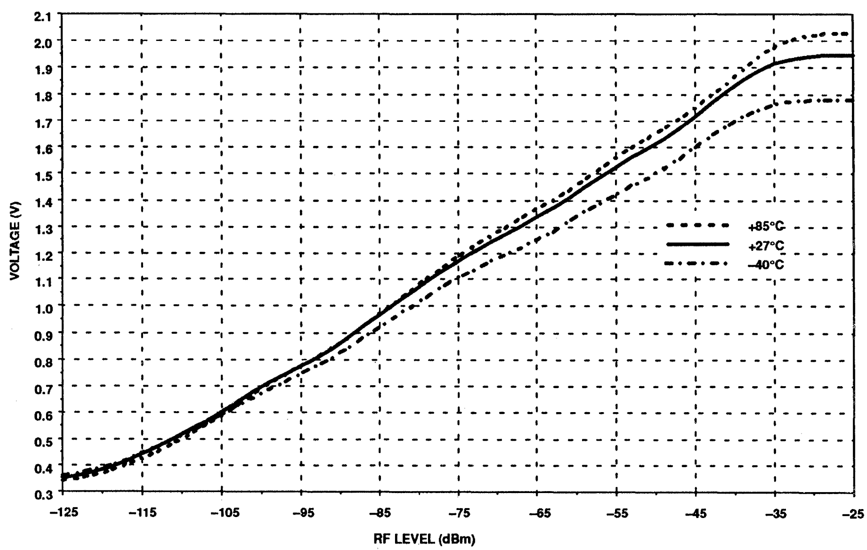


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

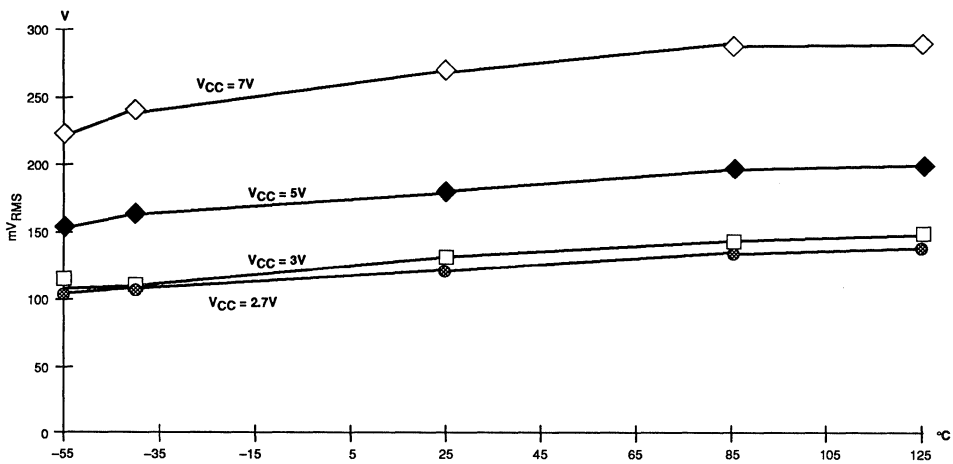


Figure 15. Audio Output vs Temperature

FM/IF amplifier/demodulator circuit

TDA1576T

FEATURES

- Fully balanced 4-stage limiting IF amplifier
- Symmetrical quadrature demodulator
- Field-strengh indication output for 1 mA ammeter
- Detune detector for side response and noise attenuation
- Detune voltage output
- Internal muting circuit
- 0° and 180° AF output signals
- Reference voltage output
- Electronic smoothing of the supply voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)	7.5	8.5	15	V
I_P	supply current	10	16	23	mA
V_{iIF}	input sensivity (RMS value)				
	–3 dB before limiting	14	22	35	μV
	S/N = 26 dB	-	10	-	μV
	S/N = 46 dB	-	55	-	μV
V_{oAF}	AF output signal (RMS value)	-	67	-	mV
THD	total harmonic distortion with double resonant circuits	-	0.02	-	%
S/N	signal-to-noise ratio (V_i > 1 mV)	-	72	-	dB
α_{AM}	AM suppression	-	50	-	dB
RR	ripple rejection (f = 100 Hz)	43	48	-	dB
I_{15}	maximum indicator output current	-	-	2	mA
T_{amb}	operating ambient temperature	–30	-	+80	°C

GENERAL DESCRIPTION

The TDA1576T is a monolithic integrated FM-IF amplifier circuit for use in mono and stereo FM-receivers of car radios or home sets.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1576T	20	mini-pack	plastic	SOT163A

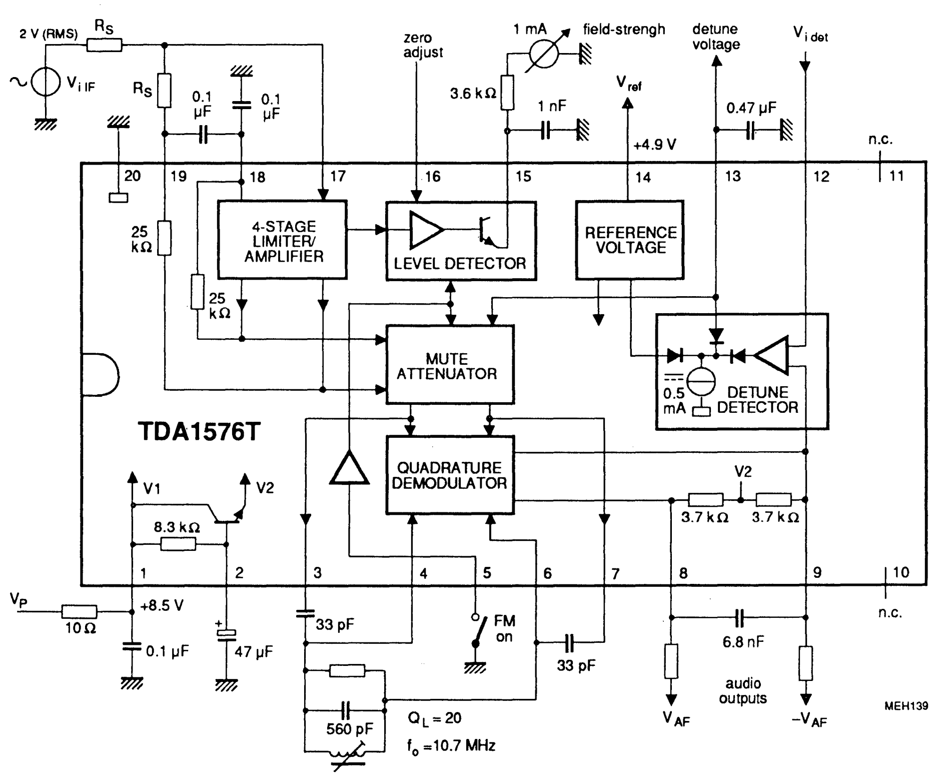


Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
C_{PS}	2	smoothing capacitor of power supply
IF1	3	IF signal to resonant circuit
RES1	4	resonant circuit
FMON	5	FM-ON, standby switch
RES2	6	resonant circuit
IF2	7	IF signal to resonant circuit
$V_{o\ AF1}$	8	AF output voltage (0° phase)
$V_{o\ AF2}$	9	AF output voltage (180° phase)
n.c.	10	not connected
n.c.	11	not connected
$V_{i\ det}$	12	detune detector input for external audio reference
$V_{o\ det}$	13	detune detector output voltage
V_{ref}	14	reference voltage output
V_F	15	level output for field-strengh
$V_{F\ o}$	16	zero adjust for field-strengh
$V_{i\ IF}$	17	FM-IF input signal
IN2	18	input 2 of differential IF amplifier
IFLV	19	IF input level
GND	20	ground (0 V)

PIN CONFIGURATION

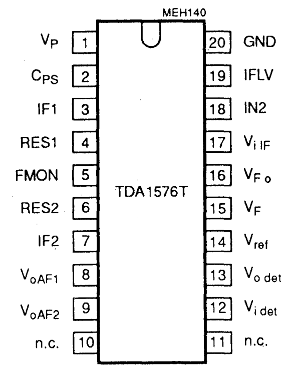


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	15	V
$V_{2, 5, 16}$	voltage on pins 2, 5 and 16	0	V_P	V
P_{tot}	total power dissipation	0	450	mW
T_{stg}	storage temperature range	−55	150	°C
T_{amb}	operating ambient temperature range	−30	+85	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	85	K/W

CHARACTERISTICS

V_P = 8.5 V; $f_{i\ ZF}$ = 10.7 MHz; R_S = 60 Ω; f_m = 400 Hz with Δf = ±22.5 kHz; 50 µs de-emphasis ($C_{8\text{-}9}$ = 6.8 nF); T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified. The demodulator circuit is adjusted at minimum second harmonic distortion for $V_{i\ ZF}$ = 1 mV and a deviation Δf = ±75 kHz.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		7.5	8.5	15	V
I_P	supply current	$V_5 = V_9 = V_{13} = 0$	10	16	23	mA
Reference voltage						
V_{ref}	reference voltage (pin 14)	I_{14} = −1 mA	-	4.9	-	V
ΔV_{ref}	reference voltage dependence on temperature	$\Delta V_{14} / V_{14} \cdot \Delta T$	-	0.3	-	%/K
I_{14}	maximum output current	short-circuit current	4	6	7.5	mA
R_{14}	output resistor ($\Delta V_{14} / \Delta I_{14}$)	I_{14} < 1.2 mA	-	60	150	Ω
IF amplifier						
$V_{i\ IF}$	input sensivity (RMS value, pin 17)	−3 dB before limiting	14	22	35	µV
$R_{17\text{-}18}$	input resistance	$V_{i\ IF}$ = 200 mV (RMS)	10	-	-	kΩ
$C_{17\text{-}18}$	input capacitance	$V_{i\ IF}$ = 200 mV (RMS)	-	5	-	pF
$V_{o\ IF}$	output signal at pins 3 and 7 (peak-to-peak value)	$Z_{3,7}$ = 10 pF // 1MΩ	610	680	750	mV
$R_{3\text{-}7}$	output impedance		200	250	300	Ω
Demodulator						
$R_{4\text{-}6}$	input resistance		20	30	40	kΩ
$C_{4\text{-}6}$	input capacitance		-	1	2.5	pF
$R_{8,9}$	output impedance		2.9	3.7	4.5	kΩ
$V_{8,9}$	DC offset voltage on output pins at $V_{4\text{-}6}$ = 0	V_5 > 3 V or $V_{3\text{-}7}$ = 0 or V_{13} < 0.3 V	-	0	±100	mV
$\Delta V/\Delta\varphi$	demodulator efficiency	$\Delta V_{8\text{-}9}/\Delta\varphi$	-	40	-	mV/°
	demodulator efficiency dependent on supply voltage (note 1)	K	-	6.2	-	mV/°
V/V	DC voltage ratio	$V_8 + V_9 / 2 \cdot V_2$	0.653	0.667	0.680	V/V
$\Delta V/\Delta T$	dependence on temperature	$\Delta(V_8 + V_9 / 2 \cdot V_2)/\Delta T$	-	10^{-5}	-	1/K
Field-strengh output						
V_{15}	output voltage (Fig.4)	$V_{i\ IF}$ = 0	0	0.1	0.25	V
		$V_{i\ IF}$ = 1 mV (RMS)	1.1	1.5	1.9	V
		$V_{i\ IF}$ = 250 mV (RMS)	3.2	3.6	4.1	V
S	control steepness	Fig.4	-	0.85	-	V/dec
R_{15}	output resistance		-	150	200	Ω
$\Delta V/\Delta T$	dependence on temperature	$V_{i\ IF} = \Delta V_{15} / (\Delta T \cdot V_{15})$	-	0.3	-	%/K
I_{15}	stand-by operational cut-off current	$V_5 \geq 3$ V; V_{15} = 0 to 5 V	-	-	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero level adjustment						
V_{16}	internal bias voltage		-	260	-	mV
R_{16}	input resistance		-	19	-	kΩ
S	control steepness	$V_{i\ IF}$ = 100 mV; $A = \Delta V_{15}/\Delta V_{16}$	0.87	1.0	1.2	V/V
Detuning detector						
I_{12}	input bias current		-	20	100	nA
R_{12}	input resistance (Fig.5)	$5\ V/\Delta I_{12}$	6	30	-	MΩ
V_{13}/V_{14}	output voltage ratio for $\Delta\varphi = \varphi$ (pins 3-7) – φ (pins 4-6) –90°; (Fig.6)	$V_1 = V_2 = 7.5$ V; $R_{13\text{-}14}$ = 10 kΩ; pins 9 and 12 short-circuit				
	$\Delta\varphi$ = 9.2° (43 kHz), Q = 20	$V_{9,\ 12}$ = 334 mV	0.45	0.5	0.55	V/V
	$\Delta\varphi$ = 3.5° (16 kHz), Q = 20	$V_{9,\ 12}$ = 138 mV	0.75	0.8	0.85	V/V
	$\Delta\varphi$ = 14° (65 kHz), Q = 20	$V_{9,\ 12}$ = 501 mV	0.335	0.345	0.355	V/V
I_{13}	maximum output current (Fig.7)	V_{13} = 6 V	0.4	0.5	0.6	mA
	cut-off current	V_{13} = 2.5 V; $V_{9,\ 12}$ = 0	-	-	–100	nA
Internal audio attenuation						
V_{13}/V_{14}	output voltage ratio (Fig.8)	α = attenuation factor				
	for α = 1 dB		0.11	0.12	0.13	
	for α = 7.2 dB		0.095	0.1	0.105	
	for $\alpha \geq$ 40 dB		-	0.06	-	
I_{13}	input current	$V_{13} / V_{13} \leq 0.1$	-	-	–225	nA
Stand-by switch						
V_5	input voltage for FM-on	$V_{3,\ 7} / V_{3,\ 7(max)} = 0.9$	2.4	2.5	-	V
	input voltage for FM-off	V_{19} = 0.3 V	-	2.9	3	V
	linear range (Fig 9)		-	350	-	mV
I_5	input current	V_5 = 0 to 2 V	-	-	–100	µA
		V_5 = 3.5 to 15 V	-	-	1	µA
$V_5/\Delta T$	temperature dependence	FM-on ($3.5V_{BE}$)	-	7	-	mV/K
		FM-off ($5V_{BE}$)	-	10	-	mV/K
Supply voltage smoothing						
$V_{1\text{-}2}$	internal voltage drop	proportional to $V_1 - 3V_{BE}$	80	210	400	mV
$R_{1\text{-}2}$	internal resistor		5.8	8.3	10.8	kΩ

OPERATING CHARACTERISTICS

V_P = 8.5 V; $f_{i\ ZF}$ = 10.7 MHz; R_S = 60 Ω; f_m = 400 Hz with Δf = ±22.5 kHz; 50 μs de-emphasis ($C_{8\text{-}9}$ = 6.8 nF); T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified. The demodulator circuit is adjusted at minimum second harmonic distortion with $V_{i\ ZF}$ = 1 mV.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF amplifier and demodulator						
$V_{i\ IF}$	input sensivity (RMS value, pin 17)	−3 dB before AF limiting	14	22	35	μV
	input signal for S/N = 26 dB	f = 250 to 15000 Hz	-	10	-	μV
	input signal for S/N = 46 dB	f = 250 to 15000 Hz	-	55	-	μV
$V_{o\ AF}$	output signal at (RMS value, pins 8 and 9)		60	67	75	mV
$V_{o\ N}$	noise voltage for $V_{i\ IF}$ = 0 (RMS value, pins 8 and 9)	R_S = 300 Ω f = 250 to 15000 Hz	-	900	-	μV
	weighted noise voltage according to	DIN 45405	-	2	-	mV
S/N	signal-to-noise ratio Fig.3 (pin 8 and 9)	$V_{i\ IF}$ = 1 mV (RMS)	-	72	-	dB
α_{AM}	AM suppression	$V_{i\ IF}$ = 0.5 to 200 mV FM: 70 Hz, ±15 kHz AM: 1 kHz, m = 30%	-	50	-	dB
α_{FM}	FM rejection for FM-off	$V_{i\ IF}$ = 500 mV; V_5 = 3V	80	-	-	dB
$\Delta V_{8,\ 9}$	AFC shift in relation to minimum second harmonic distortion α_{2H}	$V_{i\ IF}$ = 0.03 to 500 mV	-	25	-	mV
	DC offset at second harmonic distortion	operating	-	0	±100	mV
		mute or FM-off	-	0	±50	mV
α_{3H}	distortion for third harmonic		-	0.65	-	%
RR	ripple rejection V_{ripple} = 200 mV on V_P	f = 100 Hz	43	48	-	dB

Note to the characteristics

1. $V_{8\text{-}9} / \Delta\varphi = K(V_P - 3\ V_{BE})$

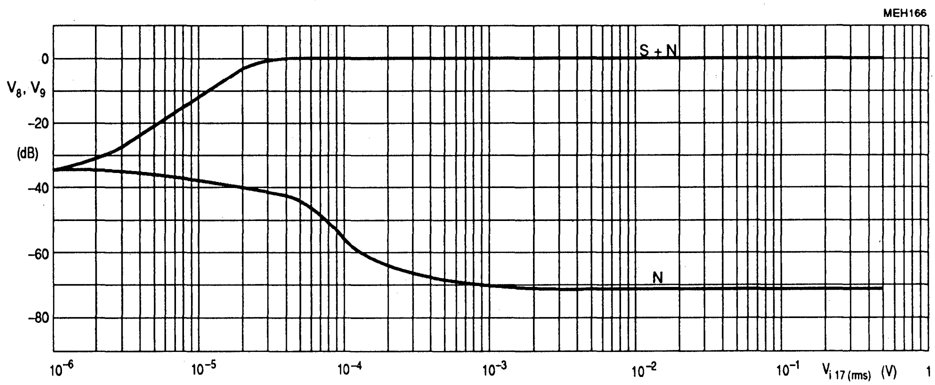


Fig.3 AF output voltage level on pins 8 and 9 as a function of $V_{i\ IF}$ at V_P = 8.5 V; f_m = 1 kHz; Q_L = 20 and with de-emphasis. S = signal; N = noise.

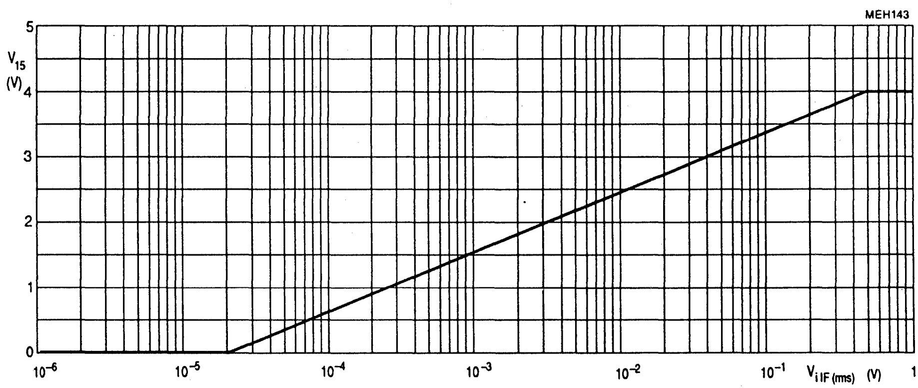


Fig.4 Field-strengh output (I_{16} = 0).

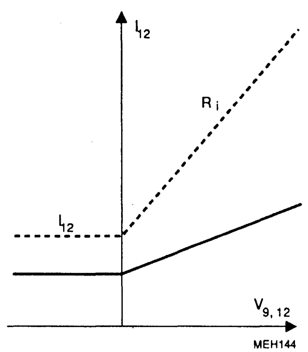


Fig.5 Detuning input impedance.

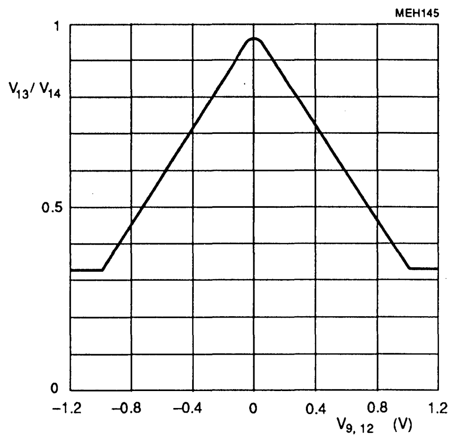


Fig.6 Detuning curve.

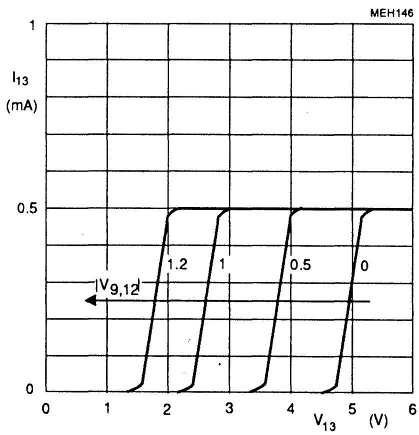


Fig.7 Detuning output.

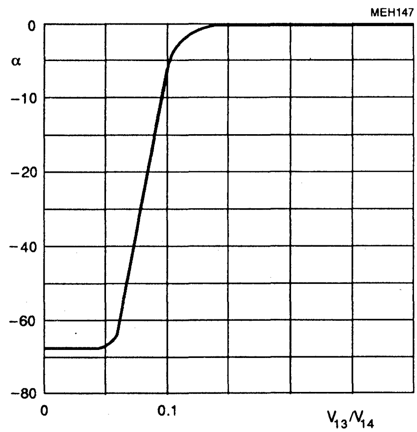


Fig.8 Internal audio attenuation.

A complete FM radio on a chip

AN192

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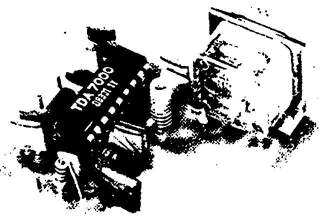
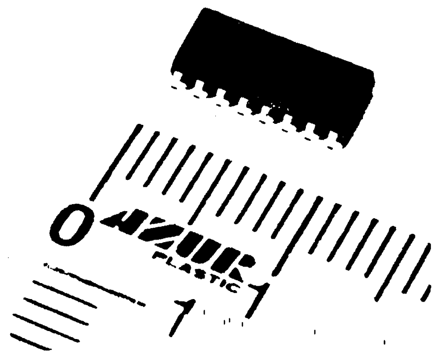
Until now, the almost total integration of an FM radio has been prevented by the need for LC tuned circuits in the RF, IF, local oscillator and demodulator stages. An obvious way to eliminate the coils in the IF and demodulator stages is to reduce the normally used intermediate frequency of 10.7MHz to a frequency that can be tuned by active RC filters, the op amps and resistors of which can be integrated. An IF of zero deems to be ideal because it eliminates spurious signals such as repeat spots and image response, but it would not allow the IF signal to be limited prior to demodulation, resulting in poor signal-to-noise ratio and no AM suppression. With an IF of 70kHz, these problems are overcome and the image frequency occurs about halfway between the desired signal and the center of the adjacent channel. However, the IF image signal must be suppressed and, in common with conventional FM radios, there is also a need to suppress interstation noise and noise when tuned to a weak signal. Spurious responses above and below the center frequency of the desired station (side tunings), and harmonic distortion in the event of very inaccurate tuning must also be eliminated.

We have now developed a mono FM reception system which is suitable for almost total integration. It uses an active 70kHz IF filter and a unique correlation muting circuit for suppressing spurious signals such as side responses caused by the flanks of the demodulator S-curve. With such a low IF, distortion would occur with the ±75kHz IF swing due to received signals with maximum modulation. The maximum IF swing is therefore compressed to ±15kHz by controlling the local oscillator in a frequency-locked loop (FLL). The combined action of the muting circuit and the FLL also suppresses image response.

The new circuit is the TDA7000 which integrates a mono FM radio all the way from the aerial input to the audio output. External to the IC are only one tunable LC circuit for the local oscillator, a few inexpensive ceramic plate capacitors and one resistor. The TDA7000 dramatically reduces assembly and post-production alignment costs because only the oscillator circuit needs adjustment during manufacture to set the limits of the tuned frequency band. The complete FM radio can be made small enough to fit inside a calculator, cigarette lighter, key-ring fob or even a slim watch. The TDA7000 can also be used as receiver in equipment such as cordless telephones, CB radios, radio-controlled models, paging systems, the sound channel of a TV set or other FM demodulating systems.





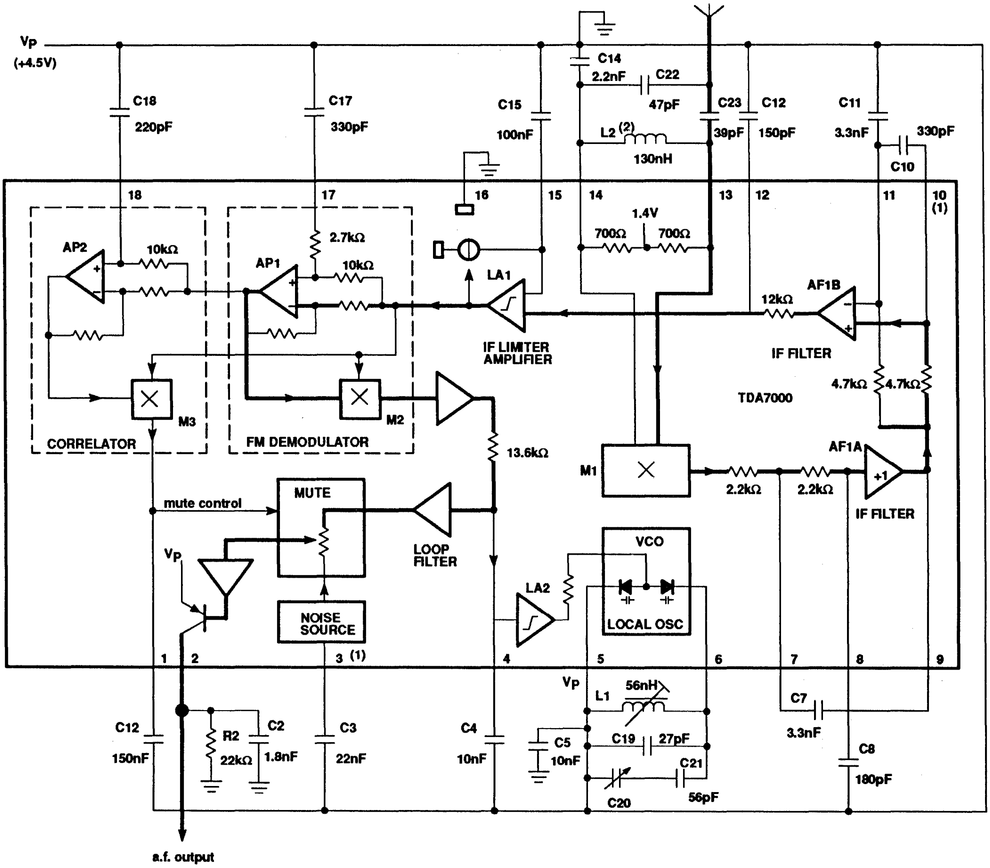
A Laboratory Model of the TDA7000 in a Complete FM Radio. Also Shown is the TDA7010T in the SO Package Against a CM Scale.

BRIEF DATA

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{CC}	Typical supply voltage		4.5		V
I_{CC}	Typical supply current		8		mA
f_{RF}	RF input frequency range	1.5		110	MHz
V_{RF-3dB}	Sensitivity for –3dB limiting EMF with $Z_S = 75\Omega$, mute disabled		1.5		µV
V_{RF}	Maximum signal input for THD < 10%, $\Delta f = \pm$ 75kHz EMF with $Z_S = 75\Omega$		200		mV
V_O	Audio output (RMS) with $R_L = 22k\Omega$, $\Delta f = \pm$ 22.5kHz		75		mV

Using the TDA7000 results in significant improvements for all classes of FM radio. For simpler portables, the small size, lack of IF coils, easy assembly and low power consumption are not the only attractive features. The unique correlation muting system and the FLL make it very easy to tune, even when using a tiny tuning knob. For higher-performance portables and clock radios, variable-capacitance diode tuning and station presetting facilities are often required. These are easily provided with the TDA7000 because there are no variable tuned circuits in the RF signal path. Only the local oscillator needs to be tuned, so tracking and distortion problems are eliminated.

The TDA7000 is available in either an 18-lead plastic DIP package (TDA7000), or in a 16-pin SO package (TDA7010T). Future developments will include reducing the present supply voltage (4.5V typ.), and the introduction of FM stereo and AM/FM versions.



NOTES:
1. These pins are not used in the SO package version (TDA7010T) AP = All-Pass filter.
2. L_2 is printed on the experimental PCB (Figure 12).
   L_1 = Toko MC108 No. 514 HNE 150013S13.
   C_{20} = Toko No.2A-15BT-R01.

Figure 1. The TDA7000 as a Variable Capacitor-Tuned FM Broadcast Receiver

CIRCUIT DESCRIPTION

As shown in Figure 1, the TDA7000 consists of a local oscillator and a mixer, a two-stage active IF filter followed by an IF limiter/amplifier, a quadrature FM demodulator, and an audio muting circuit controlled by an IF waveform correlator. The conversion gain of the mixer, together with the high gain of the IF limiter/amplifier, provides AVC action and effective suppression of AM signals. The RF input to the TDA7000 for –3dB limiting is 1.5µV. In a conventional portable radio, limiting at such a low RF input level would cause instability because higher harmonics of the clipped IF signal would be radiated to the aerial. With the low IF used with the TDA7000, the radiation is negligible.

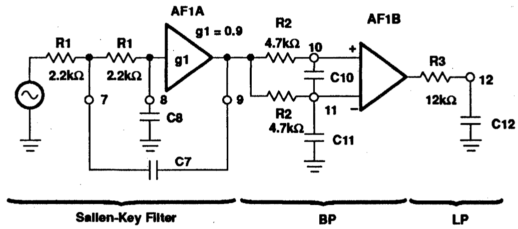
To prevent distortion with the low IF used with the TDA7000, it is necessary to restrict the IF deviation due to heavily modulated RF signals to ±15kHz. This is achieved with a frequency-locked loop (FLL) in which the output from the FM demodulator shifts the local oscillator frequency in inverse proportion to the IF deviation due to modulation.

Active IF Filter

The first section of the IF filter (AF1A) is a second-order low-pass Sallen-Key circuit with its cut-off frequency determined by internal 2.2kΩ resistors and external capacitors C_7 and C_8. The second section (AF1B) consists of a first-order bandpass filter with the lower limit of the passband determined by an internal 4.7kΩ resistor and external capacitor C_{11}. The upper limit of the passband is determined by an internal 4.7kΩ resistor and external capacitor C_{10}. The final section of the IF filter consists of a first-order low-pass network comprising an internal 12kΩ resistor and external capacitor C_{12}. The overall IF filter therefore consists of a fourth-order low-pass section and a first-order high-pass section. Design equations for the filter are given in Figure 2. Figure 3 shows the measured response for the filter.

FM Demodulator

The quadrature FM demodulator M2 converts the IF variations due to modulation into an audio frequency voltage. It has a conversion gain of –3.6V/MHz and requires phase quadrature inputs from the IF limiter/amplifier. As shown in Figure 4, the 90° phase shift is provided by an active all-pass filter which has about unity gain at all frequencies but can provide a variable phase shift, dependent on the value of external capacitor C_{17}.



Sallen-Key circuit

$$A_{SK} = \frac{g}{1 + j\omega a - \omega^2 b}$$

$$\text{With } f_O = \frac{1}{2\pi R_1 \sqrt{(C_7 C_8)}} \text{ and } Q = 0.5\sqrt{\frac{C_7}{C_8}}$$

$$A_{SK} = \frac{g}{1 + \left(j\frac{\omega}{\omega_O}\cdot\frac{1}{Q}\right)} - \frac{\omega^2}{\omega^2_O}$$

For $C_7 = 3.3nF$, $C_8 = 180pF$; $Q = 2.1$ and $f_O = 94kHz$

Bandpass circuit

$$A_{BP} = \frac{1}{1 + j\omega C_{10} R_2} \cdot \frac{j\omega C_{11} R_2}{1 + j\omega C_{11} R_2 + \frac{j\omega C_{10} R_2}{1 + j\omega C_{10} R_2}}$$

$$\text{For } f_{LP} = \frac{1}{2\pi R_2 C_{10}} \text{ and } f_{HP} = \frac{1}{2\pi R_2 C_{11}}$$

$$A_{BP} = \frac{f_{LP}}{f_{HP}} \cdot \frac{1}{\left(1 + j\frac{f}{f_{HP}}\right)\left(1 - j\frac{f_{LP}}{f}\right) + 1}$$

For $C_{10} = 330pF$, $C_{11} = 3.3nF$, $f_{LP} = 103kHz$, $f_{HP} = 10.3kHz$

Low-Pass circuit

$$A_{LP} = \frac{1}{1 + j\omega C_{12} R_3}$$

$$\text{for } f_{LP} = \frac{1}{2\pi C_{12} R_3}$$

$$A_{LP} = \frac{1}{j\frac{\omega}{\omega_{LP}}}$$

For $C_{12} = 150pF$, $f_{LP} = 88.4kHz$

Figure 2. IF Filter of the TDA7000

IF Swing Compression With the FLL

With a nominal IF as low as 70kHz, severe harmonic distortion of the audio output would occur with an IF deviation of ±75kHz due to full modulation of a received FM broadcast signal. The FLL of the TDA7000 is therefore used to compress the IF swing by using the audio output from the FM demodulator to shift the local oscillator frequency in opposition to the IF deviation. The principle is illustrated in Figure 5, which shows how an IF deviation of 75kHz is compressed to about 15kHz. The THD is thus limited to 0.7% with ±22.5kHz modulation, and to 2.3% with ±75kHz modulation.

Correlation Muting System With Open FLL

A well-known difference between FM and AM is that, for FM, each station is received in at least three tuning positions. Figure 6 shows the frequency spectrum of the output from the demodulator of a typical portable FM radio receiving an RF carrier frequency-modulated with a tone of constant frequency and amplitude. In addition to the audio response at the correct tuning point in the center of Figure 6, there are two side responses due to the flanks of the demodulator S-curve. Because the flanks of the S-curve are non-linear, the side responses have increased harmonic distortion. In Figure 6, the frequency and intensity of the side responses are functions of the signal strength, and they are separated from the correct tuning point by amplitude minima. However, in practice, the amplitude minima are not well defined because the modulation frequency and index are not constant and, moreover, the side response of adjacent channels often overlap.

High performance FM radios incorporate squelch systems such as signal strength-dependent muting and tuning deviation-dependent muting to suppress side responses. They also have a tuning meter to facilitate correct tuning. Although the TDA7000 is mainly intended for use in portables and clock radios, it incorporates a very effective new correlation muting system which suppresses interstation noise and spurious responses due to detuning to the flanks of the demodulator S-curve. The muting system is controlled by a circuit which determines the correlation between the waveform of the IF signal and an inverted version of it which is delayed (phase-shifted) by half the period of the nominal IF (180°). A noise generator works in conjunction with the muting system to give an audible indication

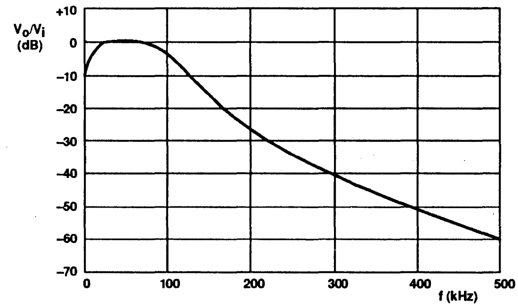
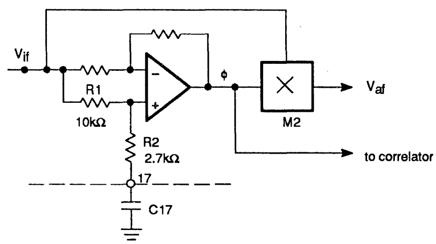


Figure 3. Measured Response of the IF Filter



With $R_2 = 0$

$\phi = -2\tan^{-1} \omega R_1 C_{17}$

for $\phi = -90^o$, $C_{17} = \dfrac{1}{\omega R_1} = 227pF$

for $f_L = 70kHz$

To improve the performance of the all-pass filter with the amplitude-limited IF waveform, R_2 has been added. Since this influences the phase angle by 45%, i.e., to 330pF for f_{IF} = 70kHz.

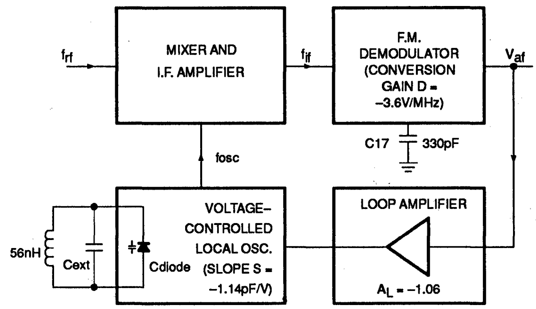
Figure 4. FM Demodulator Phase Shift Circuit (All-Pass Filter)

High performance FM radios incorporate squelch systems such as signal strength-dependent muting and tuning deviation-dependent muting to suppress side responses. They also have a tuning meter to facilitate correct tuning. Although the TDA7000 is mainly intended for use in portables and clock radios, it incorporates a very effective new correlation muting system which suppresses interstation noise and spurious responses due to detuning to the flanks of the demodulator S-curve. The muting system is controlled by a circuit which determines the correlation between the waveform of the IF signal and an inverted version of it which is delayed (phase-shifted) by half the period of the nominal IF (180°). A noise generator works in conjunction with the muting system to give an audible indication of incorrect tuning.

Figure 7 illustrates the function of the muting system. Signal IF' is derived by delaying the IF signal by half the period of the nominal IF and inverting it. With correct tuning as shown in Figure 7a, the waveforms of the two signals are identical, resulting in large correlation. In this situation, the audio signal is not muted. With detuning as shown in Figure 7b, signal IF' is phase-shifted with respect to the IF signal. The correlation between the two waveforms is therefore small and the audio output is muted. Figure 7c shows that, because of the low Q of the IF filter, noise causes considerable fluctuations of the period of the IF signal waveform. There is then small correlation between the two waveforms and the audio is muted. The correlation muting system thus suppresses noise and side responses due to detuning to the flanks of the demodulator S-curve. Since the mute threshold is much lower than that obtained with most other currently-used muting systems, this muting system is ideal for portable radios which must often receive signals with a level only slightly above the input noise.

As shown in Figure 8, the correlation muting circuit consists of all-pass filter AP2 connected in series with FM demodulator all-pass filter AP1 and adjusted by an external capacitor to provide a total phase shift of 180°. The output from AP2 is applied to mixer M3 which determines the correlation between the undelayed limited IF signal at one of its inputs and the delayed and inverted version of it at its other input. The output from mixer M3 controls a muting circuit which feeds the demodulated audio signal to the output when the correlation is high, or feeds the output from a noise source to the output to give an audible indication of incorrect tuning when the correlation is low. The switching of the muting circuit is progressive (soft muting) to prevent the generation of annoying audio transients. The output from mixer M3 is available externally at Pin 1 and can also used to drive a detuning indicator.

Figure 9 shows that there are two regions where the demodulated audio signal is fed to the output because the muting is inactive. One region is centered on the correct tuning point f_L. The other is centered on the image frequency $-f_L$. The image response is therefore not suppressed by the muting system when the frequency-locked loop is open. When the loop is closed, the time constant of the muting system, which is determined by external capacitor C_1, prevents the image response being passed to the audio output. This is described under the next heading.



$C_O = C_{EXT} + C_{STRAY} + C_{DIODE}$ with open loop = 49pF at f_O = 96MHz

Feedback factor $\beta = \frac{A_L S f_O}{2 C_O}$

Open-loop conversion gain = D = −3.6V/MHz

Closed-loop conversion gain $= \frac{D}{1 + D\beta} = 0.68 V/MHz$ for $f_O = 96 MHz$

Modulation compression factor $k = \frac{open-loop\ gain}{closed-loop\ gain} = \frac{3.6 V/MHz}{0.684 V/MHz} = 5$

$\Delta f_{OSC} = \Delta f_{RF}\left(1 - \frac{1}{K}\right)$

$\Delta f_{IF} = \frac{\Delta f_{RF}}{K}$

for $\Delta f_{RF} = 75kHz$, $\Delta f_{OSC} = 60kHz$, $\Delta f_{IF} = 15kHz$

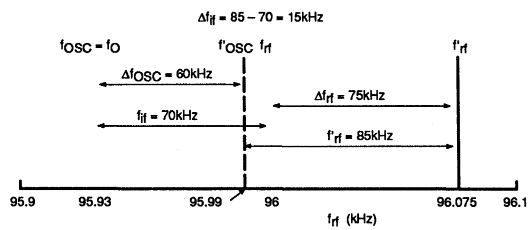


Figure 5. IF Swing Compression with the FLL

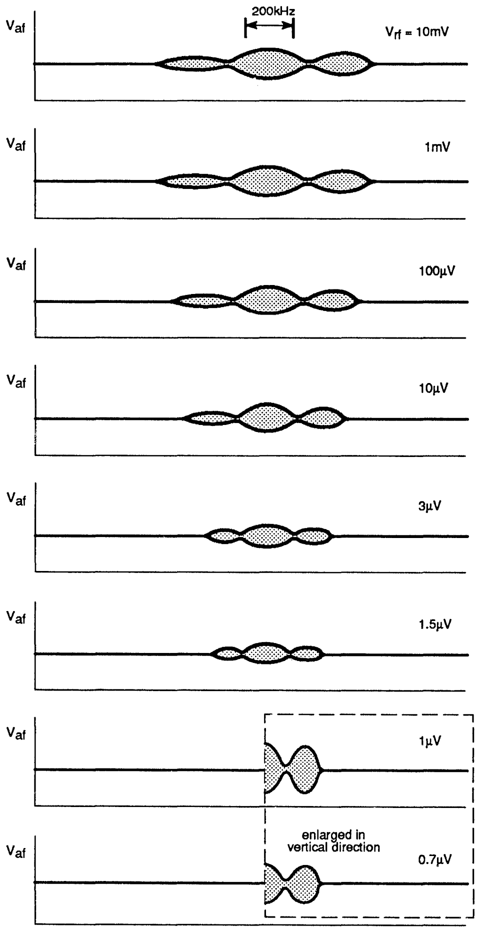


Figure 6. Audio Signal of a Typical Portable Radio as a Function of Tuned Frequency With RF Input as a Parameter. The Modulation and Amplitude are Both Constant.

Correlation Muting System With Closed FLL

The closed-loop response of the FLL is shown in Figure 10, in which the point of origin is the nominal IF ($f_{RF}-f_{OSC}=f_L$). With correct tuning, the muting is inactive and the audio signal is fed to the output. Spurious responses due to the flanks of the demodulator S-curve which occur outside the IF band $-f_2$ to f_2 are suppressed because the muting is active. Fast transients of the audio signal due to locking of the loop (A and B), and to loss of lock (C and D) are suppressed in two ways.

Lock and loss of lock transients B and D occur when the IF is greater than f_2 and are therefore suppressed because the muting is active. The situation is different during loss of lock transient C because the muting is only active for the last part of the transient. To completely suppress this transient, capacitor C_1 in Figure 1 holds the muting control line positive (muting active) during the short interval while the IF traverses from $-f_1$ to $-f_2$. The same applies for lock transient A during the short interval while the IF traverses from $-f_2$ to $-f_1$. Since the image response occurs halfway between $-f_1$ and $-f_2$, it is also suppressed.

Figure 11 shows the audio output from the TDA7000 radio as a function of tuned frequency with aerial signal level as a parameter. Compared with the similar diagram for a typical conventional portable radio (Figure 6), there are three important improvements:

1. There are no side responses due to the flanks of the demodulator S-curve. This is due to the action of the correlation muting system (soft mute) which combines the function of a detuning-dependent muting system with that of a signal strength-dependent muting system.

2. The correct tuning frequency band is wide, even with weak aerial signals. This is due to the AFC action of the FLL which reduces a large variation of aerial input frequency (equivalent to detuning) to a small variation of the IF. There is no audio distortion when the radio is slightly detuned.

3. Although the soft muting system remains operative with low level aerial signals, there is no degradation of the audio signal under these conditions. This is due to the high gain of the IF limiter/amplifier which provides –3dB limiting of the IF signal with an aerial input level of 1.5µV. However, the soft muting action does reduce the audio output level with low level aerial signals.

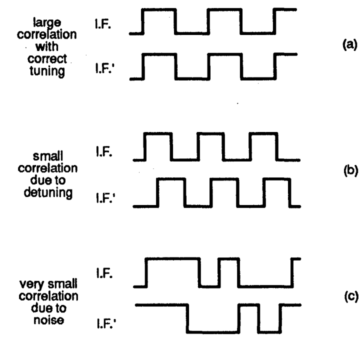
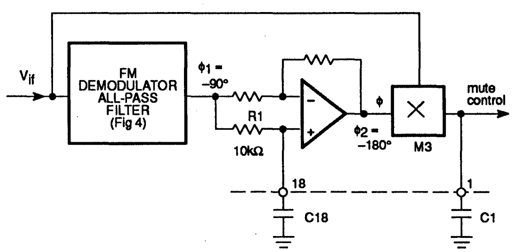


Figure 7. Function of the Correlation Muting System



$$\phi_2 = -2\tan^{-1}\omega R_1 C_{18} - \phi_1$$

$$\text{for } \phi_2 = -180^\circ \; C_{18} = \frac{1}{\omega R_1}$$

$$\text{for } f_{if} = 70kHz, \; C_{18} = 227pF$$

Figure 8. Correlator of the TDA7000

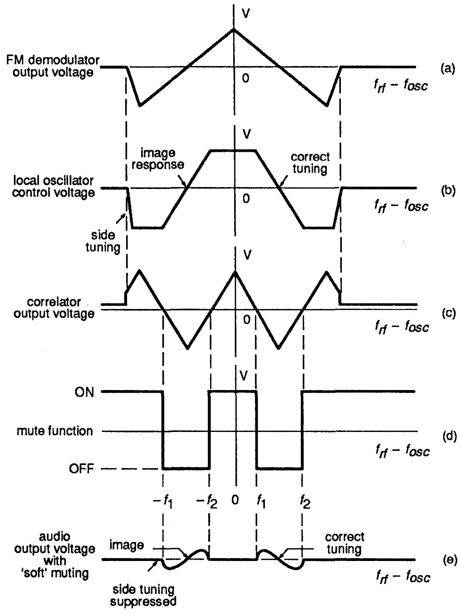


Figure 9. Operation of the Correlation Muting System with Open-Loop FLL

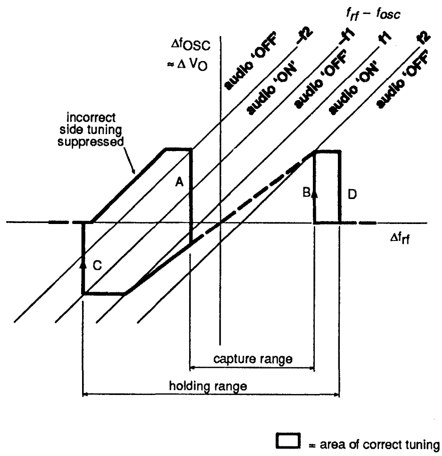


Figure 10. Closed-Loop Response of the FLL

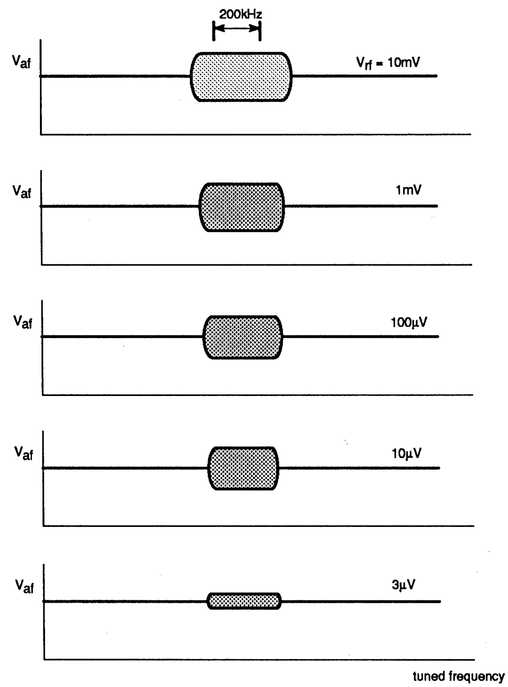


Figure 11. Audio Signal of the TDA7000 as a Function of the Tuned Frequency with RF Input as a Parameter

RECEIVER CIRCUITS

Circuits With Variable Capacitor Tuning

The circuit diagram of the complete mono FM radio is given in Figure 1. An experimental printed-wiring board layout is given in Figure 12. Special attention has been paid to supply lines and the positioning of large-signal decoupling capacitors.

The functions of the peripheral components of Figure 1 not already described are as follows:

C_1 – Determines the time constant required to ensure muting of audio transients due to the operation of the FLL.

C_2 – Together with R_2 determines the time constant for audio de-emphasis (e.g., R_2C_2 = 40µs.

C_3 – The output level from the noise generator during muting increases with increasing value of C_3. If silent mute is required, C_3 can be omitted.

C_4 – Capacitor for the FLL filter. It eliminates IF harmonics at the output of the FM demodulator. It also determines the time constant for locking the FLL and influences the frequency response.

C_5 – Supply decoupling capacitor which must be connected as close as possible to Pin 5 of the TDA7000.

C_7 to C_{12}, C_{17} and C_{18} – Filter and demodulator capacitors. The values shown are for an IF of 70kHz. For other intermediate frequencies, the values of these capacitors must be changed in inverse proportion to the IF change.

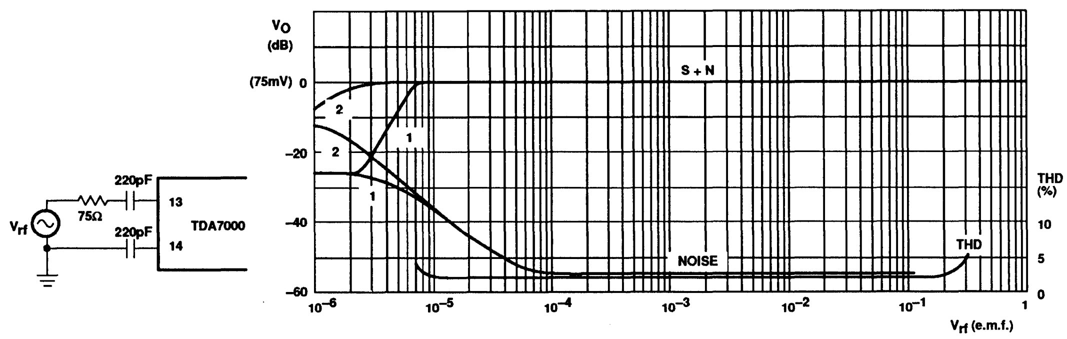
C_{14} – Decouples the reverse RF input. It must be connected to the common return via a good quality short connection to ensure a low-impedance path. Inductive or capacitive coupling between C_{14} and the local oscillator circuit or IF output components must be avoided.

C_{15} – Decouples the DC feedback for IF limiter/amplifier LA_1.

C_{19} and C_{21} – Local oscillator tuning capacitors. Their values depend on the required tuning range and on the value of tuning capacitor C_{20}.

C_{22}, C_{23}, L_1, L_2 – The values given are for an RF bandpass filter with Q = 4 for the European and USA domestic FM broadcast band (87.5MHz to 108MHz). For reception of the Japanese FM broadcast band (76MHz to 91MHz), L_1 must be increased to 78nH and L_2 must be increased to 150nH. If stopband attenuation for high level AM or TV signals is not required, L_2 and C_{22} can be omitted and C_{23} changed to 220pF.

R_2 – The load for the audio output current source. It determines the audio output level, but its value must not exceed 22kΩ for V_{CC} = 4.5V, or 47kΩ for V_{CC} = 9V.



NOTES:
The curves numbered 1 were measured with the muting system active. The curves numbered 2 were measured with the muting system disabled by injecting about 20μA into Pin 1 of the TDA7000. The input frequency was 96MHz modulated with 1kHz with a deviation of ±75kHz for the distortion curve.

Figure 12. Audio Output as a Function of Input EMF

PERFORMANCE OF THE CIRCUIT

V_{CC}=4.5V, T_A=25°C f_{RF}=96MHz, V_{RF}=0.2mV EMF from a 75Ω source, modulated with Δf=±22.5kHz, f_M=1kHz. Noise voltage measured unweighted over the bandwidth 300Hz to 20kHz, unless otherwise specified.

SYMBOL	PARAMETER	TYP	MAX	
EMF EMF EMF	<80>Sensitivity (EMF voltage)for –3dB limiting: muting disabled for –3dB muting for (S+N)/N=26dB	1.5 6 5.5		
EMF	<80>Signal handling (EMF voltage) for THD<10%; Δf=±75kHz	200		
(S+N)/N	Signal–to–noise ratio (see Figure 13)	60		
THD THD	<80>Total harmonic distortion (see Figure 13) at Δf=±22.5kHz at Δf=±75kHz			
AMS	<80>AM suppression (ratio of the AM output signalreferred to the FM output signal) FM signal: f_m=1kHz;Δf=±75kHz AM signal: f_m=1kHz; m=80%			
RR	10			
$V_{6-5\ RMS}$	250			
Δf_{OSC}	80Variation of oscillator frequencywith supply voltage (ΔV_{CC}=1V)	60		
S_{+300} S_{-300}	45 35			
Δf_{RF}	AFC range	±300		
B	80Audio bandwidth at ΔV_O=3dBmeasured with pre–emphasis (t=50μs)	10		
$V_{O(RMS)}$	80AF output voltage (RMS value)at R_L=22kΩ	75		
R_L R_L		22 47		

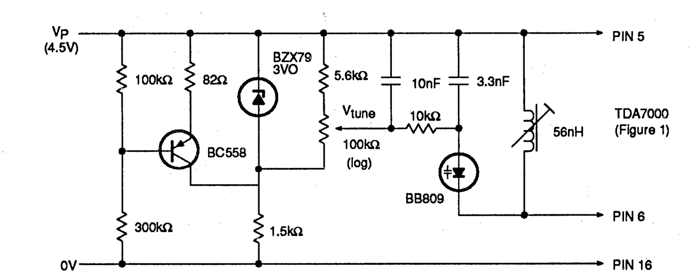


Figure 13. Variable-Capacitance Diode Tuning for the Local Oscillator. Additional Measures Must be Taken to Ensure Temperature Stability.

Circuit With Variable-Capacitance Diode Tuning

Since it is only necessary to tune the local oscillator coil, it is very simple to modify the circuit of Figure 1 for variable-capacitance diode tuning. The modifications are shown in Figure 13. A circuit board layout for the modified receiver and a photograph of a complete laboratory model are shown in Figure 14.

Narrow-Band FM Receiver

The TDA7000 can also be used for reception of narrowband FM signals. In this case, the local oscillator is crystal-controlled (as shown in Figure 15) and there is therefore hardly any compression of the IF swing by the FLL. The deviation of the transmitted carrier frequency due to modulation must therefore be limited to prevent severe distortion of the demodulated audio signal.

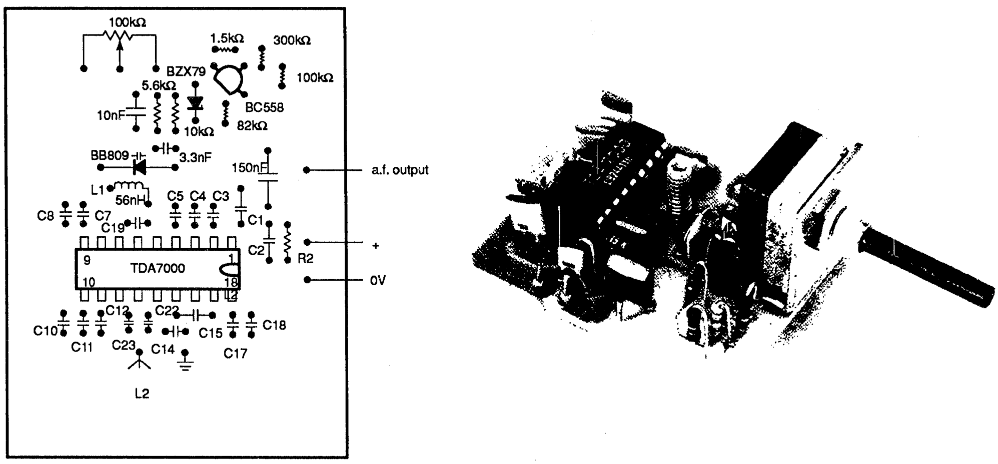


Figure 14. Circuit Board Layout and Complete Model of a TDA7000 Radio With Variable-Capacitance Diode Tuning

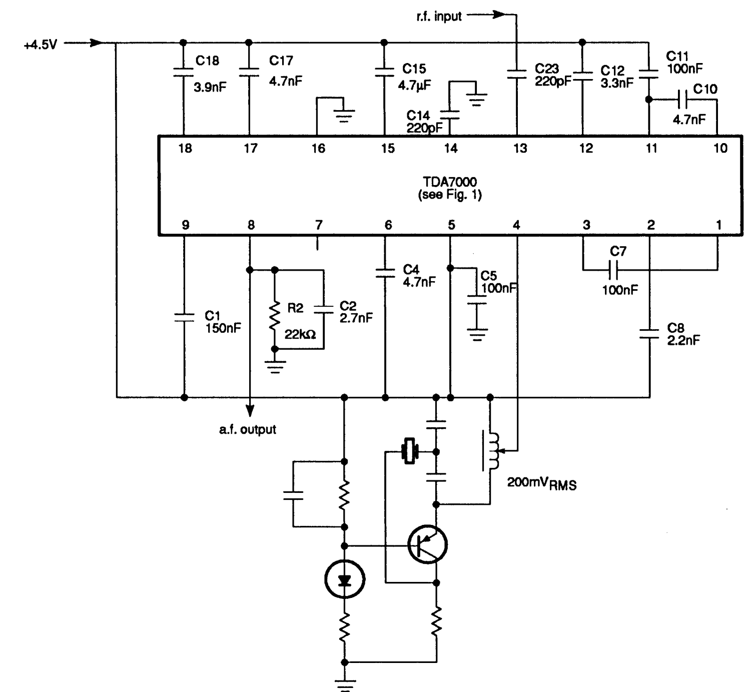


Figure 15. A Narrowband FM Receiver With a Crystal-Controlled Local Oscillator

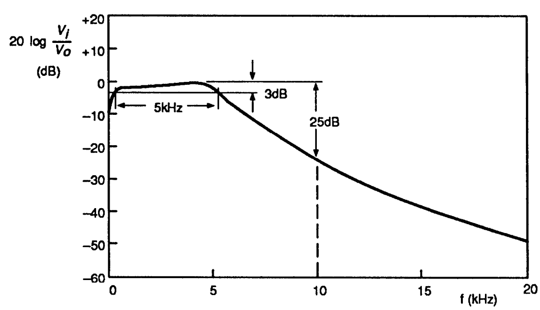


Figure 16. IF Selectivity for the Narrowband FM Receiver

The component values in Figure 16 result in an IF of 4.5kHz and an IF bandwidth of 5kHz (Figure 16). If the IF is multiplied by N, the values of capacitors C_{17} and C_{18} in the all-pass filters and the values of filter capacitors C_7, C_8, C_{10}, C_{11}, and C_{12} must be multiplied by 1/N. For improved IF selectivity to achieve greater adjacent channel attenuation, second-order networks can be used in place of C_{10} and C_{11}.

In this circuit the detuning noise generator is not used. Since the circuit is mainly for reception of audio signals, the audio output must be passed through a low-pass Chebyshev filter to suppress IF harmonics.

AUDIO AMPLIFIER AND DETUNING INDICATOR CIRCUITS

Audio output stages suitable for use with the TDA7000 are shown in Figures 17 and 18. Figure 19 shows how the muting signal can be used to operate an LED to give an indication of detuning.

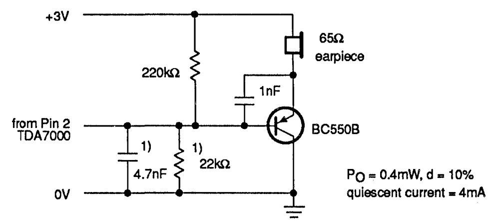
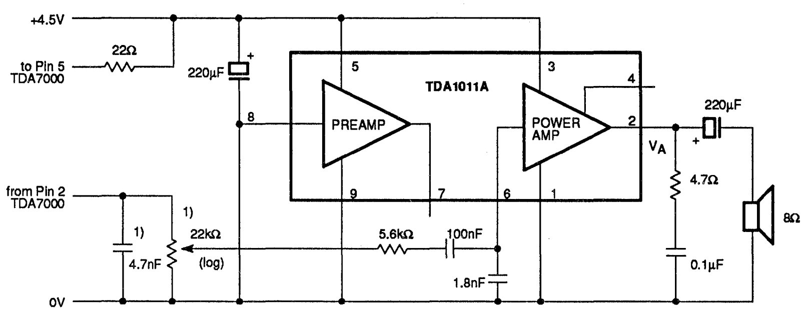


Figure 17. A 0.4mW Transistor Audio Output Stage Without Volume Control for Driving an Earpiece



NOTE:
1. These components replace C2 and R2 in Figure 1. P_O = 250mW, d = 10% quiescent current = 8mA.

Figure 18. An Integrated 250mW Audio Output Stage

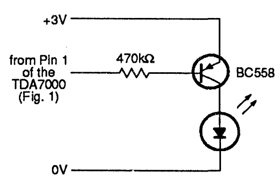


Figure 19. A Detuning Indicator Driven by the Mute Signal From the TDA7000

ACKNOWLEDGEMENTS

The authors wish to acknowledge the information provided by D. Kasperkovitz and H.v. Rumpt for incorporation in this article.

REFERENCE

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TDA7000 for narrowband FM reception | AN193

Author: W.V. Dooremolen

INTRODUCTION

Today's cordless telephone sets make use of duplex communication with carrier frequencies of about 1.7MHz and 49MHz.

- In the base unit incoming telephone information is frequency-modulated on a 1.7MHz carrier.
- This 1.7MHz signal is radiated via the AC mains line of the base unit.
- The remote unit receives this signal via a ferrite bar antenna.
- The remote unit transmits the call signals and speech information from the user at 49MHz via a telescopic antenna.
- The base unit receives this 49MHz FM-modulated signal via a telescopic aerial.

Today's Remote Unit Receivers

In cordless telephone sets, a normal superheterodyne receiver is used for the 1.7MHz handset. The suppression of the adjacent channel at, e.g., 30kHz, must be 50dB, and the bandwidth of the channel must be 6-10kHz for good reception. Therefore, an IF frequency of 455kHz is chosen. Since at this frequency there are ceramic filters with a bandwidth of 9kHz (AM filters), the 1.7MHz is mixed down to 455kHz with an oscillator frequency of 2.155MHz. Now there is an image reception at 2.61MHz. To suppress this image sufficiently, there must be at least two RF filter sections at the input of the receiver.

The ceramic IF filter with its subharmonics is bad for far-off selectivity, so there must be an extra LC filter added between the mixer output and the ceramic filter.

After the selectivity there is a hard limiter for AGC function and suppression of AM.

Next, there is an FM detector which must be accurate because it must detect a swing of ±2.5kHz at 455kHz; therefore, it must be tuned.

Figure 1 shows the block diagram which fulfills this principal. The total number of alignment points of this receiver is then 5:

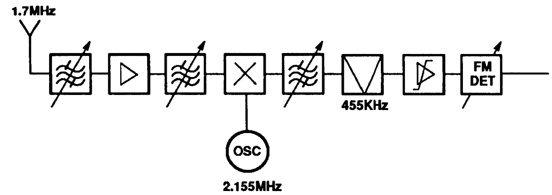


Figure 1. Remote-unit Receiver: 1..7MHz

2 RF filters
1 Oscillator
1 IF filter
1 FM detector

5 Alignments

A Remote Unit Receiver With TDA7000

The remote unit receiver (see Figure 2) has as its main component the IC TDA7000, which contains mixer, oscillator, IF amplifiers, a demodulator, and squelch functions.

To avoid expensive filtering (and expensive filter-adjustments) in RF, IF, and demodulator stages, the TDA7000 mixes the incoming signal to such a low IF frequency that filtering can be realized by active RC filters, in which the active part and the Rs are integrated.

To select the incoming frequency, only one tuned circuit is necessary: the oscillator tank circuit. The frequency of this circuit can be set by a crystal.

IMAGE RECEPTION

For today's concept, a number of expensive components are necessary to suppress the image sufficiently. The suppression of the image is very important because the signal at the image can be much larger than the wanted signal and there is no correlation between the image and the wanted signal.

In a concept with 455kHz IF frequency, the 1.7MHz receiver has image reception at 2.155MHz. In the TDA7000 receiver, the IF frequency is set at 5kHz. Then the 1.7MHz receiver (with 1.695MHz oscillator frequency) has image reception at 1.69MHz, which is at 10kHz from the required frequency (see Figure 3).

An IF frequency of 5kHz has been chosen because:

- this frequency is so low, there will be no neighboring channel reception at the image frequency.
- this frequency is not so low that at maximum deviation (maximum modulation) distortion could occur (folding distortion, caused by the higher-order bessel functions)
- this frequency gives the opportunity to obtain the required neighboring channel suppression with minimum components in the IF selectivity.

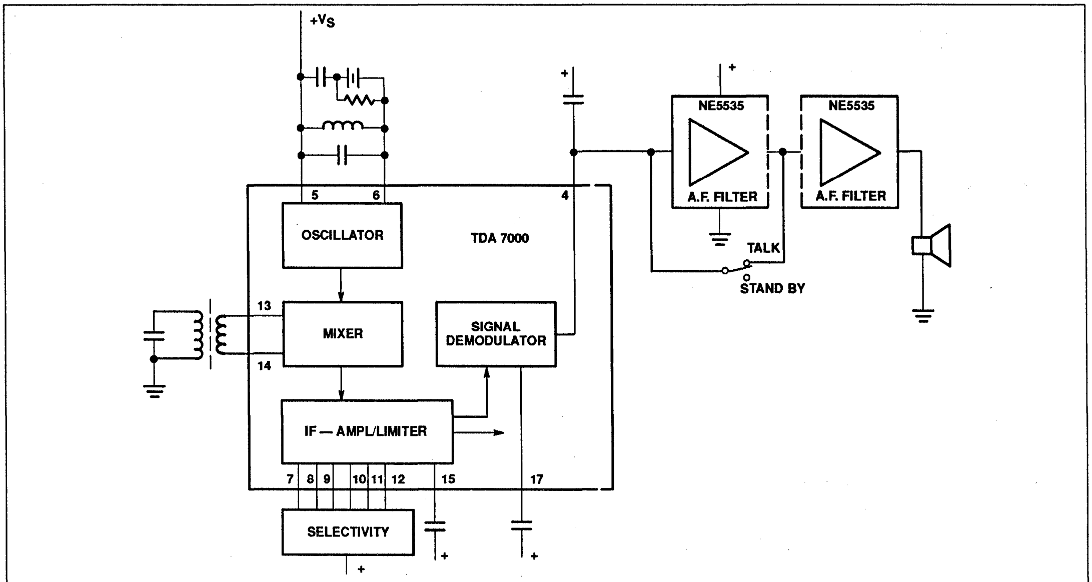


Figure 2.

CIRCUIT DESCRIPTION (SEE FIGURE 2)

When a remote unit is at "power-on" in the "standby" position, it is ready to receive a "bell signal". A bell signal coming through the telephone line will set the base unit in the mode of transmitting a 1.7MHz signal, modulated with, e.g., 0.75kHz with ±3kHz deviation.

The ferrite antenna of the remote unit receives this signal and feeds it to the mixer, where it is converted into a 5kHz IF signal.

Before the RF signal enters the mixer (at Pins 13 and 14) it passes RF selectivity, taking care of good suppression of unwanted signals from, e.g., TV or radio broadcast frequencies. The IF signal from the mixer output passes IF selectivity (Pins 7 to 12) and the IF amplifier/limiter (Pin 15), from which the output is supplied to a quadrature demodulator (Pin 17). Due to the low IF frequency, cheap capacitors can be used for both IF selectivity and the phase shift for the quadrature demodulator.

The AF output of the demodulator (Pin 4) is fed to the AF filter and AF amplifier NE5535.

The RF Input Circuit

As the image reception is an in-channel problem, solved by the choice of IF frequency and IF selectivity, the RF input filter is only required for stopband selectivity (a far-off selectivity to suppress unwanted large signals from, e.g., radio broadcast transmitters).

In a remote unit receiver at 1.7MHz, this filter is at the ferrite rod. Figure 4 shows the bandpass behavior of such a filter at 1.7MHz.

The Mixer

The mixer conversion gain depends on the level of the oscillator voltage as shown in Figure 5, so the required oscillator voltage at Pin 6 is 200mV$_{RMS}$.

The Oscillator

To obtain the required frequency stability in a cordless telephone set, where adjacent channels are at 20 or 30kHz, crystal oscillators are commonly used.

The crystal oscillator circuits usable for this kind of application always need an LC-tuned resonant circuit to suppress the other modes of the crystal. In this type of oscillator (see Figure 6 as an example) the crystal is in the feedback line of the oscillator amplifier. Integration of such an amplifier should give a 2-pin oscillator.

The TDA7000 contains a 1-pin oscillator. An amplifier with current output develops a voltage across the load impedance. Voltage feedback is internal to the IC.

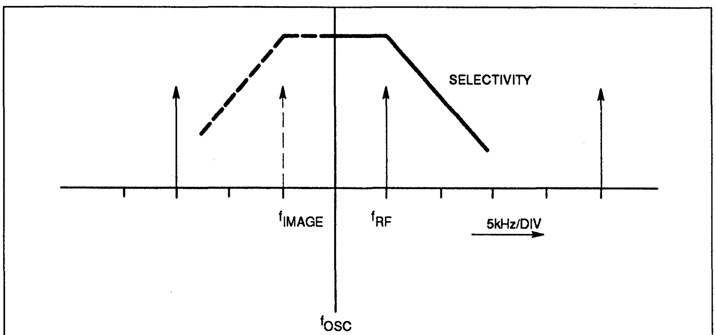


Figure 3.

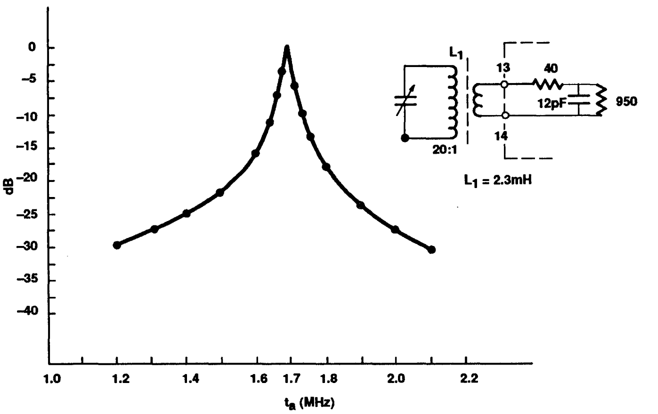


Figure 4.

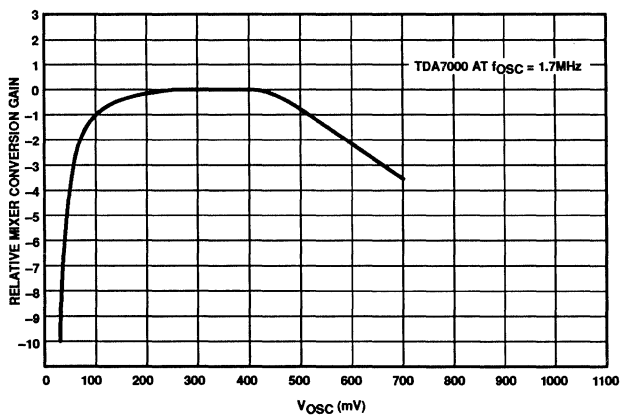


Figure 5. Relative Mixer Conversion Gain

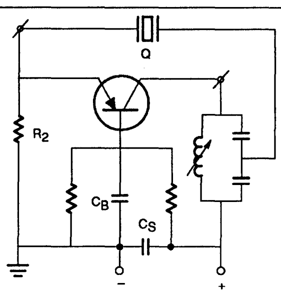


Figure 6.

To obtain a crystal oscillator with the TDA7000 1-pin concept, a parallel circuit configuration as shown in Figure 7 has to be used.

Explanation of this circuit:

1. Without the parallel resistor RP— Figure 8 shows the relevant part of the equivalent circuit. There are three frequencies where the circuit is in resonance (see Figure 9, and the frequency response for "impedance" and "phase", shown in Figure 10). The real part of the highest possible oscillation frequency dominates, and, as there is also a zero-crossing of the imaginary part, this highest frequency will be the oscillator frequency. However, this frequency (fPAR) is not crystal-controlled; it is the LC oscillation, in which the parasitic capacitance of the crystal contributes.
2. With parallel resistor RP— The frequency response (in "amplitude" and "phase") of the oscillator circuit of Figure 7 with RP is given in Figure 11. As the resistor value of RP is large related to the value of the crystal series resistance R1 or R3, the influence of RP at crystal resonances is negligible. So, at crystal resonance (see Figure 9b), R3 causes a circuit damping

$$R = \frac{1}{W^2} \cdot R_3 \cdot C_1^2 + R_3 \left(1 + \frac{C_2}{C_1}\right)^2$$

However, at the higher LC-oscillation frequency f_{PAR} (see Figure 9c), R_P reduces the circuit impedance R_O to

$$\frac{R_O \cdot R_{DAMPING}}{R_O + R_{DAMPING}} = R_C$$

where

$$R_{DAMPING} = \frac{1}{W^2} \cdot R_P \cdot C_1^2 + R_P \left(1 + \frac{C_2}{C_1}\right)^2$$

Thus a damping resistor parallel to the crystal (Figure 7) damps the parasitic LC oscillation at the highest frequency. (Moreover, the imaginary part of the impedance at this frequency shows incorrect zero-crossing.)

Taking care that $R_P > R_{SERIES}$, the resistor is too large to have influence on the crystal resonances. Then with the impedance R_C at the parasitic resonance lower than R at crystal resonance, oscillation will only take place at the required crystal frequency, where impedance is maximum and phase is correct (in this example, at third-overtone resonance).

Remarks:

1. It is advised to avoid inductive or capacitive coupling of the oscillator tank circuit with the RF input circuit by careful positioning of the components for these circuits and by avoiding common supply or ground connections.

The IF Amplifier

Selectivity

Normal selectivity in the TDA7000 is a fourth-order low-pass and a first-order high-pass filter. This selectivity can be split up in a Sallen and Key section (Pins 7, 8, 9), a bandpass filter (Pins 10, 11), and a first-order low-pass filter (Pin 12).

Some possibilities for obtaining required selectivity are given:

1. In the basic application circuit, Figure 12a, the total filter has a bandwidth of 7kHz and gives a selectivity at 25kHz IF frequency of 42dB.
   In this filter the lower limit of the passband is determined by the value of C4 at Pin 11, where C3 at Pin 10 determines the upper limit of the bandpass filter section.
2. To obtain a higher selectivity, there is the possibility of adding a coil in series with the capacitor between Pin 11 and ground. The so-obtained fifth-order filter has a selectivity at 25kHz of 57dB (see Figure 12b).
3. If this selectivity is still too small, there is a possibility of increasing the 25kHz selectivity to 65dB by adding a coil in series with the capacitor at Pin 11 to ground. In this application, where at 5kHz IF frequency an adjacent channel at -30kHz will cause a (30-5)=25kHz interfering IF frequency, the pole of the last-mentioned LC filter (trap function) is at 25kHz (see Figure 12c).

For cordless telephone sets with channels at 15kHz distance, the filter characteristics are optimum as shown in the curves in Figure 13, in which case the filters are dimensioned for 5kHz IF bandwidth (instead of 7kHz). So for this narrow channel spacing application, the required selectivity is obtained by reducing the IF bandwidth; this at the cost of up to 2dB loss in sensitivity.

NOTE:

At 5kHz IF frequency adjacent channels at ±15kHz give undesired IF frequencies of 20kHz and 10kHz, respectively.

Limiter/Amplifier

The high gain of the limiter/amplifier provides AVC action and effective suppression of AM modulation. DC feedback of the limiter is decoupled at Pin 15.

The Signal Demodulator

The signal demodulator is a quadrature demodulator driven by the IF signal from the limiter and by a phase-shifted IF signal derived from an all-pass filter (see Figure 14).

This filter has a capacitor connected at Pin 17 which fixes the IF frequency. The IF frequency is where a 90 degree phase shift takes care of the center position in the demodulator output characteristics (see Figure 15, showing the demodulator output (at Pin 4) as a function of the frequency, at 1mV input signal).

The AF Output Stage

The signal demodulator output is available at Pin 4, where a capacitor, C, serves for elimination of IF harmonics. This capacitor also influences the audio frequency response. The output from this stage, available at Pin 2, has an audio frequency response as shown in Figure 16, curve a. The output at Pin 2 can be muted.

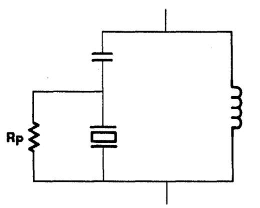


Figure 7.

Output Signal Filtering

Output signal filtering is required to suppress the IF harmonics and interference products of these harmonics with the higher-order bessel components of the modulation. Active filtering with operational amplifiers has been used (see Figure 17). The frequency response of such a filter is given in Figure 16, Curve b, for an active second-order filter with an additional passive RC filter.

Output Amplification

The dimensioning of the operational amplifier of Figure 17a results in no amplification of the AF signal. In case amplification of this op amp is required, a feedback resistor and an RC filter at the reverse input can be added (see Figure 17b, for about 30dB amplification).

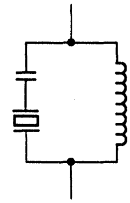


Figure 8a.

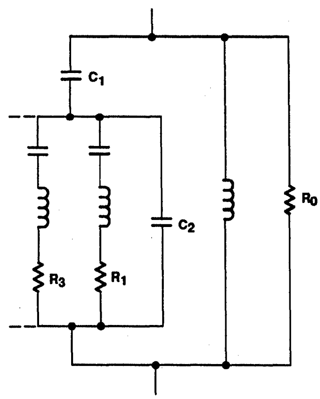
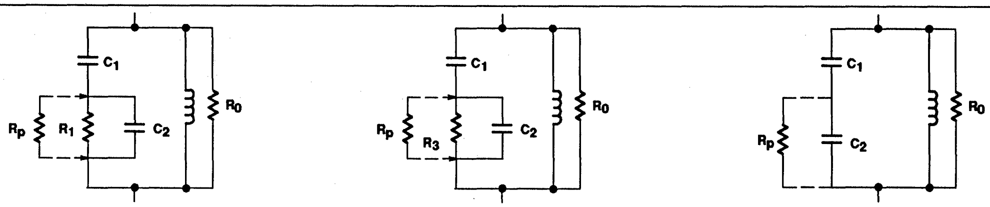


Figure 8b.



a. At f_1 b. At f_3 c. At f_{PAR}

Figure 9.

MEASUREMENTS

For sensitivity, signal handling, and noise behavior information in a standard application as shown in Figure 18, the signal and noise output as a function of input signal has been measured at 1.7MHz, at 400Hz modulation where the deviation is ±2.5kHz (see Figure 19). As a result the S+N/N ratio is as given in Figure 19, Curve 3.

APPENDIX

RF-Tuned Input Circuit at 46MHz

In Figure 20 a filter is given which matches at 46MHz a 75Ω aerial to the input of the TDA7000. Extra suppression of RF frequencies outside the passband has been obtained by a trap function.

RF Pre-Stage at 46MHz

For better quality receivers at 46MHz, an RF pre-stage can be added (see Figure 21) to improve the noise figure. Without this transistor, a noise figure F=11dB was found. With a transistor (BFY 90) with RC coupling at 3mA, F=7dB or at 6mA F=6dB.

With a transistor stage having an LC-tuned circuit, one can obtain F=7dB at I=0.3mA.

NOTE:

The noise figure includes image-noise.

An LC Oscillator at 1.7MHz

An LC oscillator can be designed with or without AFC. If for better stability external AFC is required, one can make use of the DC output of the signal demodulator, which delivers 80mV/kHz at a DC level of 0.65V to +supply. An LC oscillator as shown in Figure 22a, using a capacitor with a temperature coefficient of -150ppm, gives an oscillator signal of 190mV, with a temperature stability of 1kHz/50°.

With the use of AFC, as shown in Figure 22b, one can further improve the stability, as AFC reduces the influence of frequency changes in the transmitter (due to temperature influence or aging). The given circuit gives a factor 2 reduction. Note that the temperature behavior of the AFC diode has to be compensated. In Figure 22b, with BB405B having a capacitance of 18pF at the reverse voltage V4=0.7V, the temperature coefficient of the capacitor C has to be -200ppm.

AF Output Possibilities

The AF output from the signal demodulator, available at Pin 4, depends on the slope of the demodulator as shown in Figure 15. The TDA7000 AF output is also available at Pin 2 (see Figure 23). The important difference between the output at Pin 2 and the output at Pin 4 is that the Pin 4 output is amplified and limited before it is led to Pin 2 (see Figure 24). Moreover, the Pin 2 output is controlled by the mute function, a mute which operates in case the received signal is bad as far as noise and distortion are concerned.

The Pin 2 output delivers a higher AF signal; however, the AF output spectrum shows more mixing products between IF harmonics and modulation frequency harmonics. This is due to the "limited output situation" at Pin 2. In narrow-band application with relatively large deviation these products are so high that extra AF output filtering is required and, moreover, the IF center frequency has to be higher compared to the concept, using AF output at Pin 4.

So for those sets where the mute/squelch function of the TDA7000 is not used, and the higher AF output is not required, the use of the AF output at Pin 4 is advised, giving less interfering products and simplified AF output filtering.

Squelch and Squelch Indication

The TDA7000 contains a mute function, controlled by a "waveform correlator", based on the exactness of the IF frequency.

The correlation circuit uses the IF frequency and an inverted version of it, which is delayed (phase-shifted) by half the period of nominal IF. The phase shift depends on the value of the capacitor at Pin 18 (see Figure 23).

This mute also operates at low field strength levels, where the noise in the IF signal indicates bad signal definition. (The correlation between IF signal and the inverted phase-shifted version is small due to fluctuations caused by noise; see Figure 25.) This field strength-dependent mute behavior is shown in Figure 26, Curve 2, measured at full mute operation. The AF output is not "fast-switched" by the mute function, but there is a "progressive (soft muting) switch". This soft muting reduces the audio output signal at low field strength levels, without degradation of the audio output signal under these conditions.

The capacitor, C_1, at Pin 1 (see Figure 23) determines the time constant for the mute action.

Part operation of the mute is also a possibility (as shown by Figure 26, Curve 3) by circuiting a resistor in parallel with the mute capacitor at Pin 1.

In Figure 26 the small signal behavior with the mute disabled has been given also (see Curve 1).

One can make use of the mute output signal, available at Pin 1, to indicate squelch situation by an LED (see Figure 27). Operation of the mute by means of an external DC voltage (see Figure 28) is also possible.

Bell Signal Operation

To avoid tone decoder filters and tone decoder rectifiers for bell signal transmission, use can be made of the mute information in the TDA7000 to obtain a bell signal without the transmission of a bell pilot signal.

With a handset receiver as shown in Figure 23 in the "standby" position, the high mute output level turns amplifier 1 off via transistor T1 until a correct IF frequency is obtained. This situation appears at the moment that a bell signal switches the base unit in transmission mode. If the transmitted field strength is high enough to be received above a certain noise level, the mute level output goes down; T1 will be closed and amplifier 1 starts operating. However, due to feedback, this amplifier starts oscillating at a low frequency (a frequency dependent on the filter concept). This low-frequency signal serves for bell signal information at the loudspeaker.

Switching the handset to "talk" position will stop oscillation. Then amplifier 1 serves to amplify normal speech information.

Mute at Dialing

During dial operation, the key-pulser IC delivers a mute voltage. This voltage can be used to mute the AF amplifier, e.g., via T1 of the bell signal circuit/amplifier (see Figure 23).

CONCLUSIONS

The application of the TDA7000 in the remote unit (handset) as narrow-band FM receiver is very attractive, as the TDA7000 reduces assembly and post-production alignment costs. The only tunable circuit is the oscillator circuit, which can be a simple crystal-controlled tank circuit.

A TDA7000 with:

- fifth-order IF filter
- third-order AF output filter
- matched input circuit
- crystal oscillator tank circuit
- disabled mute circuit

gives a sensitivity of 2.5μV for 20dB signal-to-noise ratio, at adjacent channel selectivity of 40dB (at 15kHz) in cordless telephone application at 1.7MHz.

The TDA7000 circuit is:

- without an RF pre-stage

- without RF-tuned circuits
- without oscillator transistor (and its components)
- without LC or ceramic filters in IF and demodulator.

For improved performance, the TDA7000 circuit can be expanded:

- with an RF pre-stage and RF selectivity
- with higher-order IF filtering
- with mute/squelch function.

For reduced performance the TDA7000 circuit can be simplified:

- to LC-tuned oscillator
- to lower-order IF filter
- to bell signal operation without pilot transmission.

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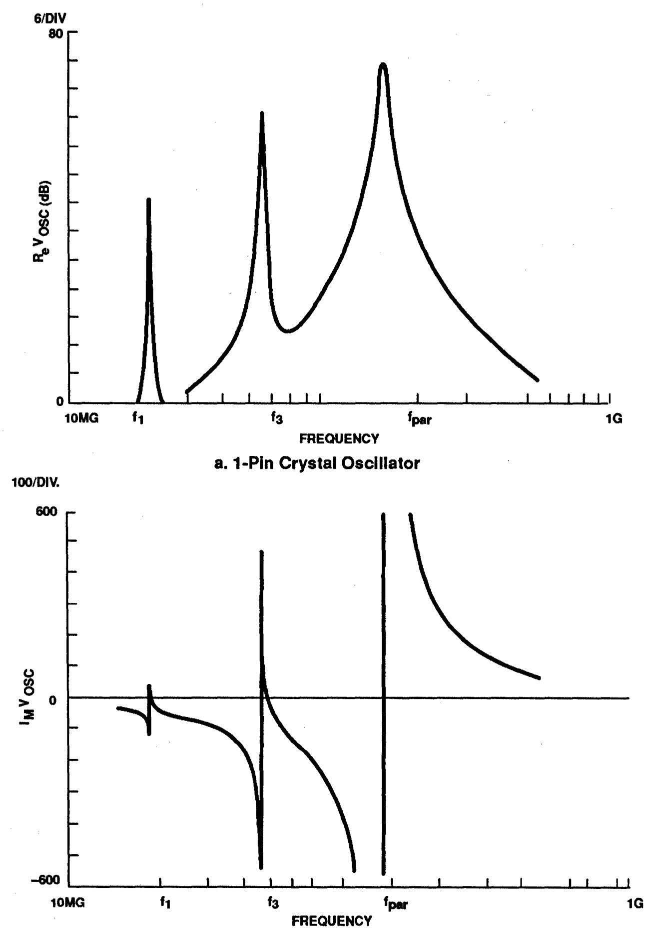
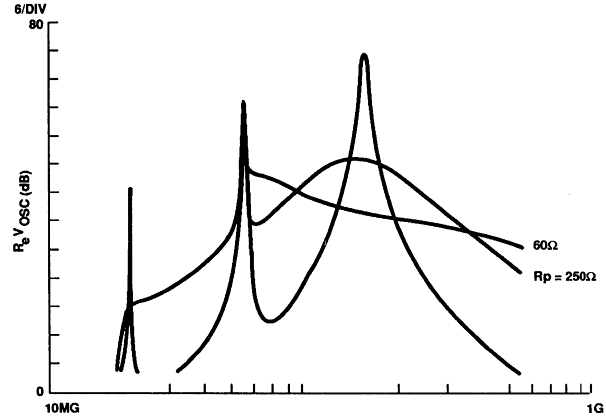


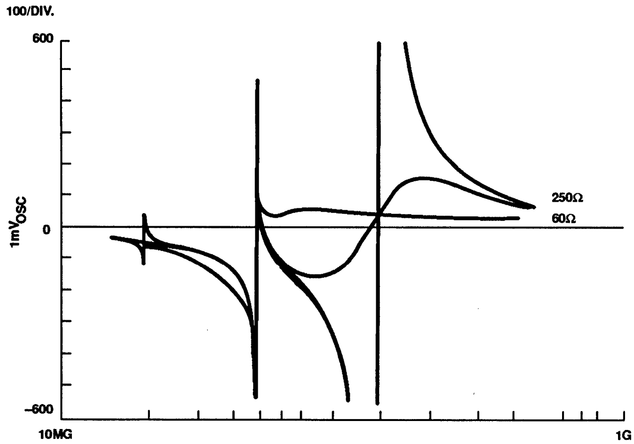
a. 1-Pin Crystal Oscillator

b. 1-Pin Crystal Oscillator

Figure 10.



a. 1-Pin Crystal Oscillator
(R = ∞, 250, 60)



b. 1-Pin Crystal Oscillator
(R = ∞, 250, 60)

Figure 11.

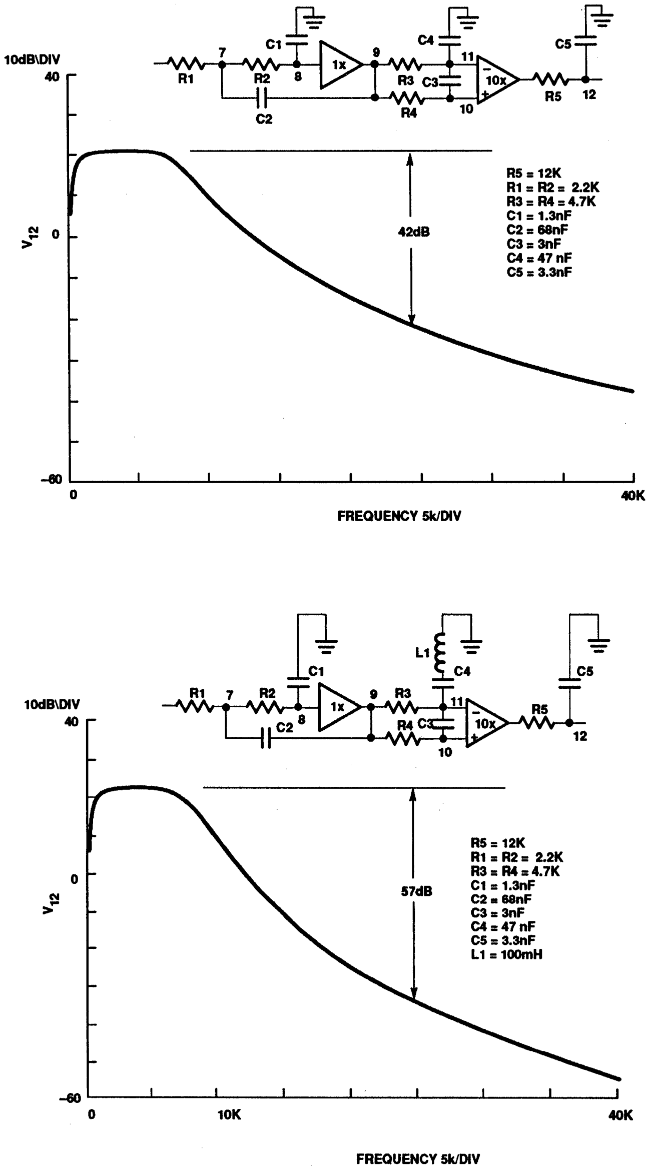

10dB\DIV
40
0
-60
V12
0
40K
FREQUENCY 5k/DIV
R1
R2
C1
C2
R3
R4
C3
C4
C5
R5
1x
10x
42dB
R5 = 12K
R1 = R2 = 2.2K
R3 = R4 = 4.7K
C1 = 1.3nF
C2 = 68nF
C3 = 3nF
C4 = 47 nF
C5 = 3.3nF
10dB\DIV
40
0
-60
V12
0
10K
40K
FREQUENCY 5k/DIV
L1
57dB
R5 = 12K
R1 = R2 = 2.2K
R3 = R4 = 4.7K
C1 = 1.3nF
C2 = 68nF
C3 = 3nF
C4 = 47 nF
C5 = 3.3nF
L1 = 100mH

Figure 12.

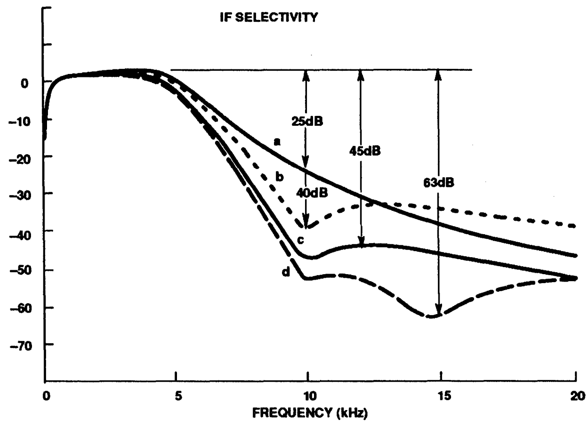


Figure 12 (Continued)

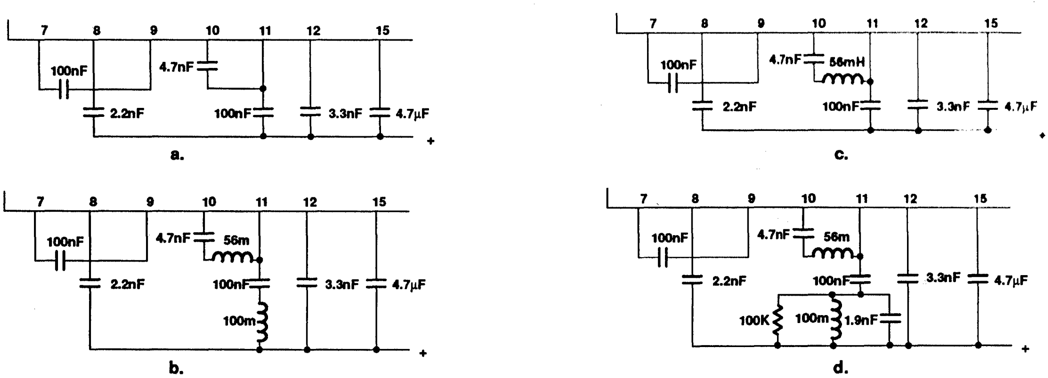
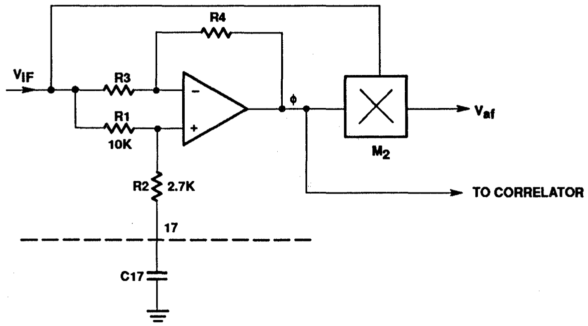


Figure 13.



NOTES:
With $R_2 = 0$.
$\phi = -2\tan_1 sR_1C_{17}$

for $\phi = -90°C$, $C_{17} = \frac{1}{wR_1\sqrt{\frac{R_4}{R_3}}} = 4.1nF$ for $f_{IF} = 5kHz$.

To improve the performance of the all-pass filter with the amplitude limited IF waveform, R_2 has been added. Since this influences the phase angle, the value of C_{17} must be increased by 13%, i.e., to 4.7nF.

Figure 14. FM Demodulator Phase-Shift Circuit (All-Pass Filter)

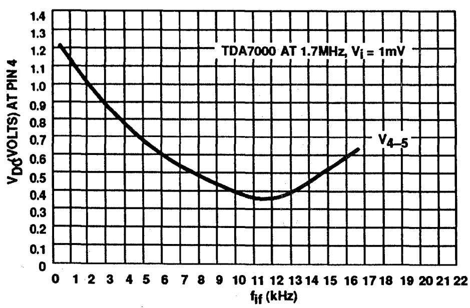


Figure 15.

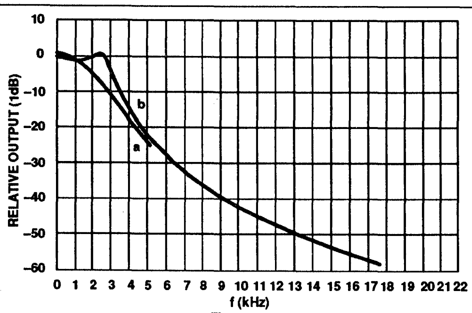


Figure 16.

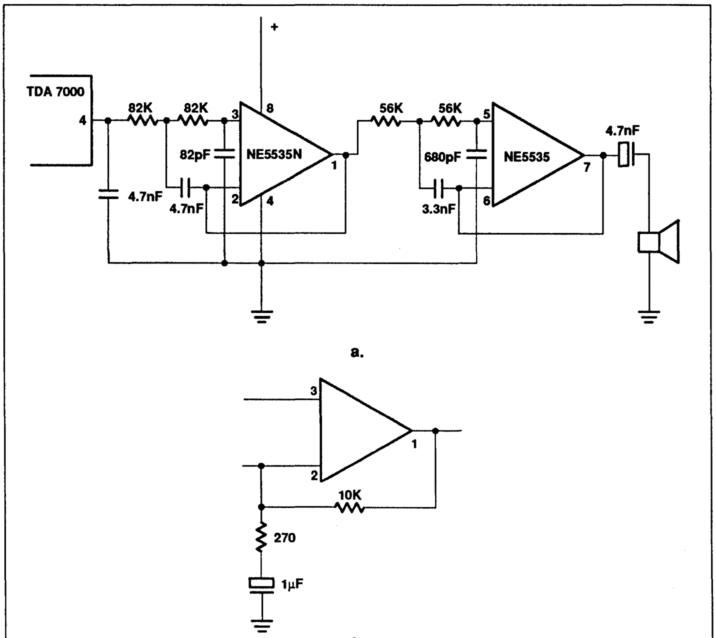


Figure 17

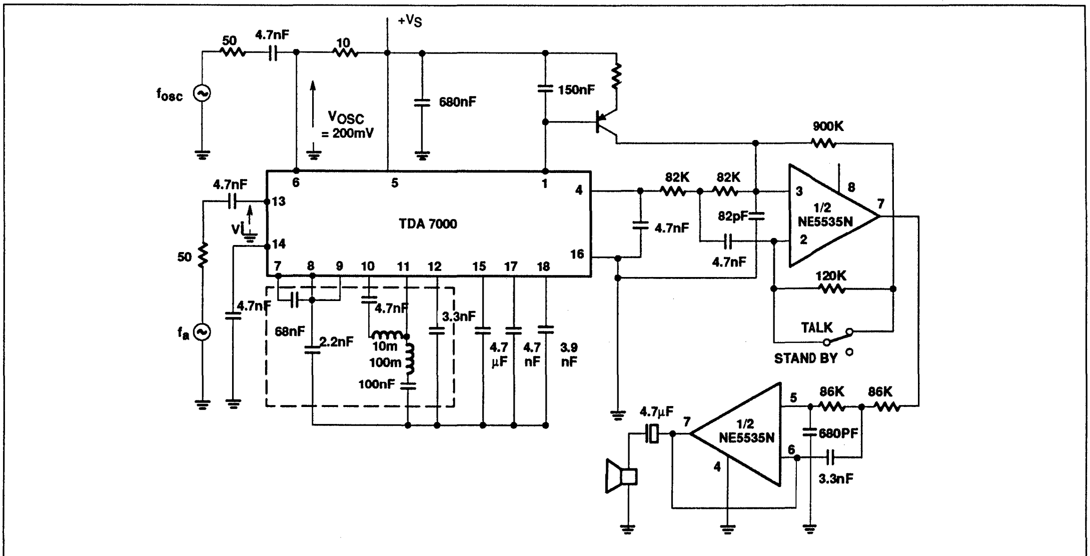


Figure 18.

TDA7000 for narrowband FM reception

AN193

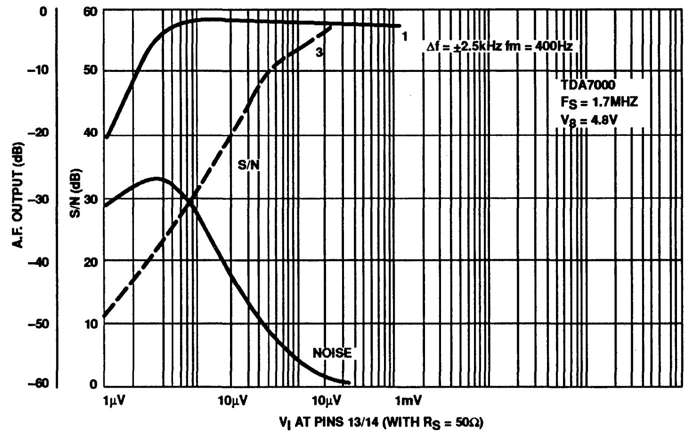


Figure 19.

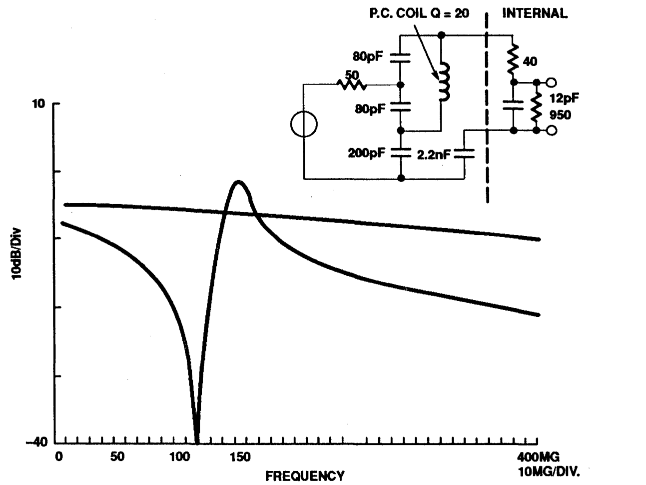


Figure 20.

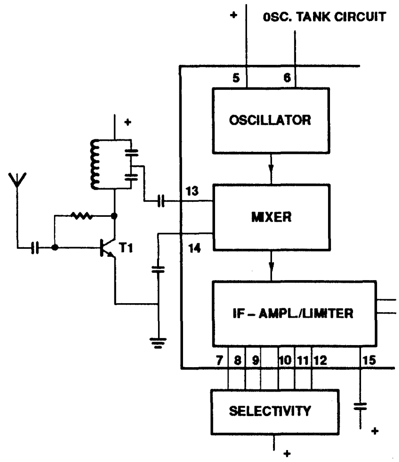
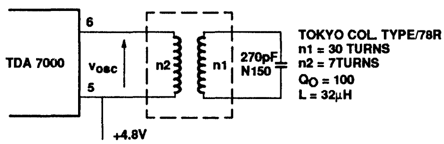
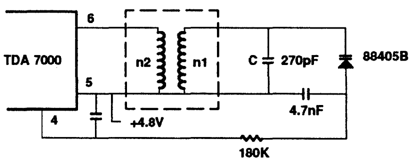


Figure 21.



a.



b.

Figure 22.

0

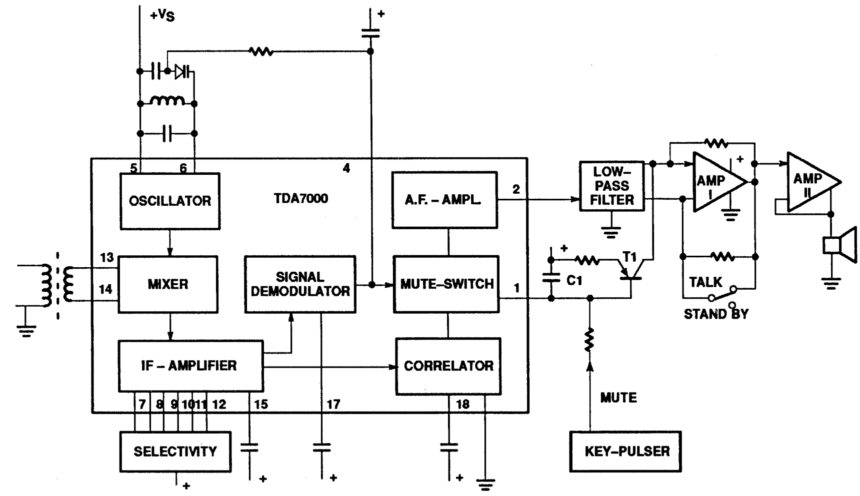


Figure 23. Remote Unit Receiver: 1.7MHz

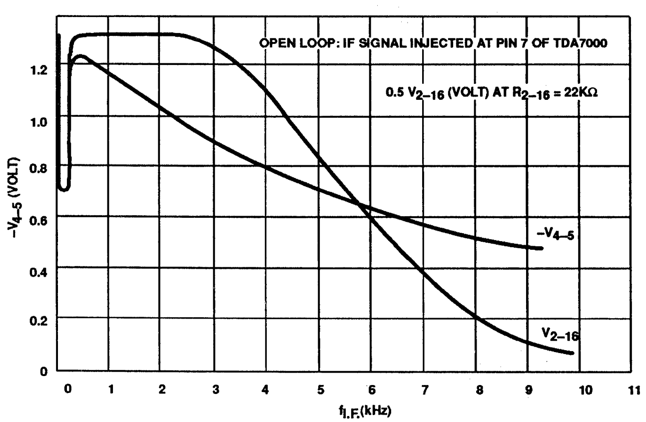


Figure 24. Demodulator Characteristics

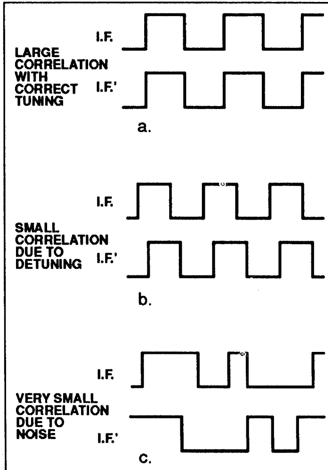


Figure 25. Function of the Correlation Muting System

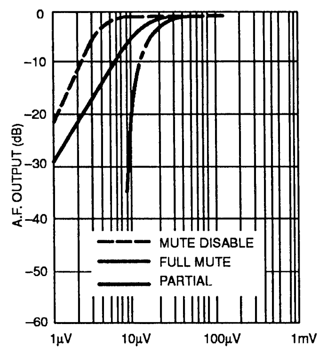


Figure 26.

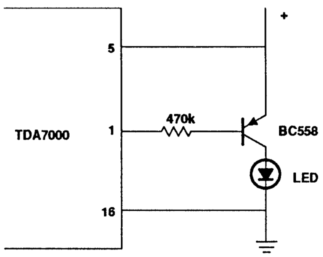


Figure 27. Function of the Correlation Muting System

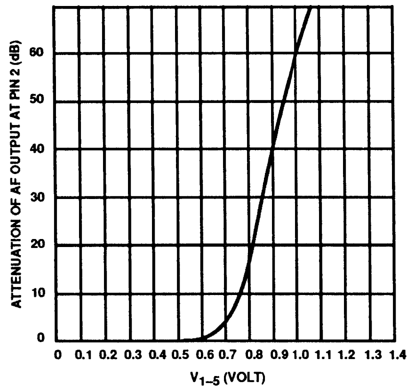


Figure 28.

Single-chip FM radio circuit TDA7000

GENERAL DESCRIPTION

The TDA7000 is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7000 includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

QUICK REFERENCE DATA

Supply voltage range (pin 5)	V_P		2,7 to 10	V
Supply current at V_P = 4,5 V	I_P	typ.	8	mA
R.F. input frequency range	f_{rf}		1,5 to 110	MHz
Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled)	EMF	typ.	1,5	μV
Signal handling (e.m.f. voltage) (source impedance: 75 Ω)	EMF	typ.	200	mV
A.F. output voltage at R_L = 22 kΩ	V_o	typ.	75	mV

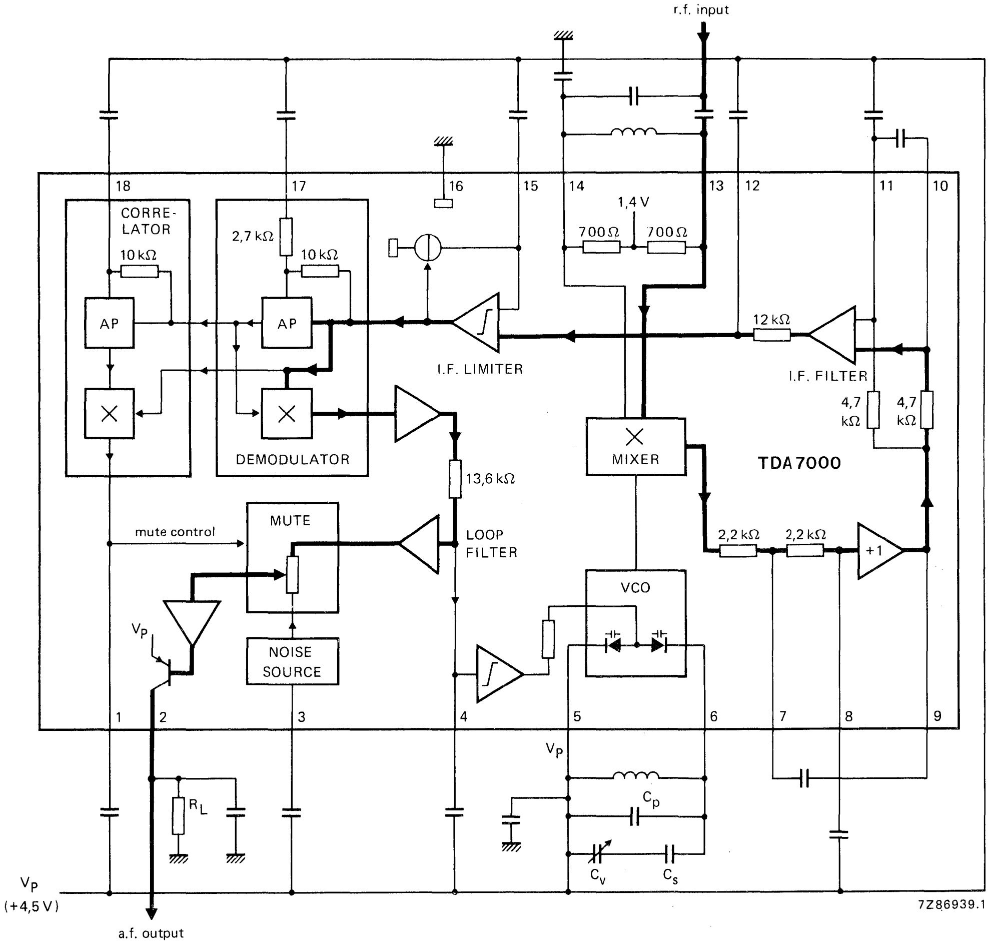


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 5)	V_P	max.	12 V
Oscillator voltage (pin 6)	$V_{6\text{-}5}$	V_P–0,5 to V_P +0,5	V
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	–55 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to +60	°C

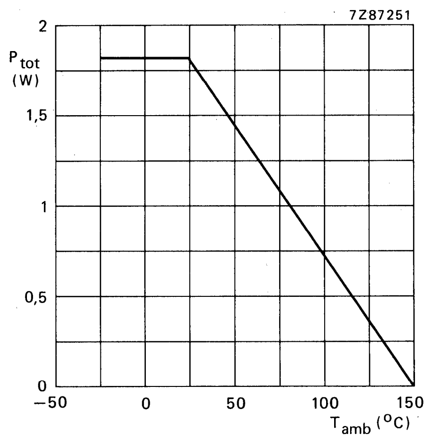


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 5)	V_P	2,7	4,5	10	V
Supply current at V_P = 4,5 V	I_P	–	8	–	mA
Oscillator current (pin 6)	I_6	–	280	–	μA
Voltage at pin 14	$V_{14\text{-}16}$	–	1,35	–	V
Output current at pin 2	I_2	–	60	–	μA
Voltage at pin 2; R_L = 22 kΩ	$V_{2\text{-}16}$	–	1,3	–	V

A.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for −3 dB limiting; muting disabled	EMF	–	1,5	–	μV
for −3 dB muting	EMF	–	6	–	μV
for S/N = 26 dB	EMF	–	5,5	–	μV
Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio	S/N	–	60	–	dB
Total harmonic distortion at Δf = ± 22,5 kHz	THD	–	0,7	–	%
at Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ± 75 kHz AM signal: f_m = 1 kHz; m = 80%	AMS	–	50	–	dB
Ripple rejection (ΔV_P = 100 mV; f = 1 kHz)	RR	–	10	–	dB
Oscillator voltage (r.m.s. value) at pin 6	$V_{6\text{-}5(rms)}$	–	250	–	mV
Variation of oscillator frequency with supply voltage (ΔV_P = 1 V)	Δf_{osc}	–	60	–	kHz/V
Selectivity	S_{+300}	–	45	–	dB
	S_{-300}	–	35	–	dB
A.F.C. range	Δf_{rf}	–	± 300	–	kHz
Audio bandwidth at ΔV_o = 3 dB measured with pre-emphasis (t = 50 μs)	B	–	10	–	kHz
A.F. output voltage (r.m.s. value) at R_L = 22 kΩ	$V_{o(rms)}$	–	75	–	mV
Load resistance at V_P = 4,5 V	R_L	–	–	22	kΩ
at V_P = 9,0 V	R_L	–	–	47	kΩ

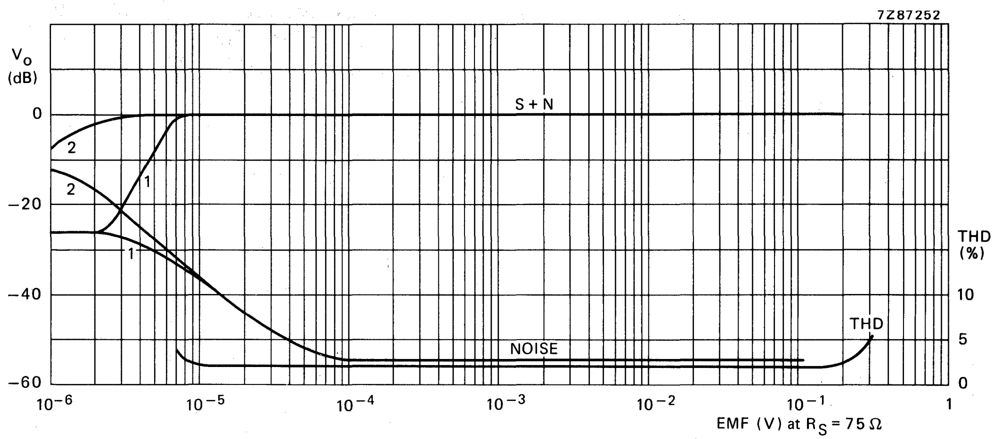


Fig. 3 A.F. output voltage (V_o) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV; f_{rf} = 96 MHz.
for S + N curve: Δf = ± 22,5 kHz; f_m = 1 kHz.
for THD curve: Δf = ± 75 kHz; f_m = 1 kHz.

Notes

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.

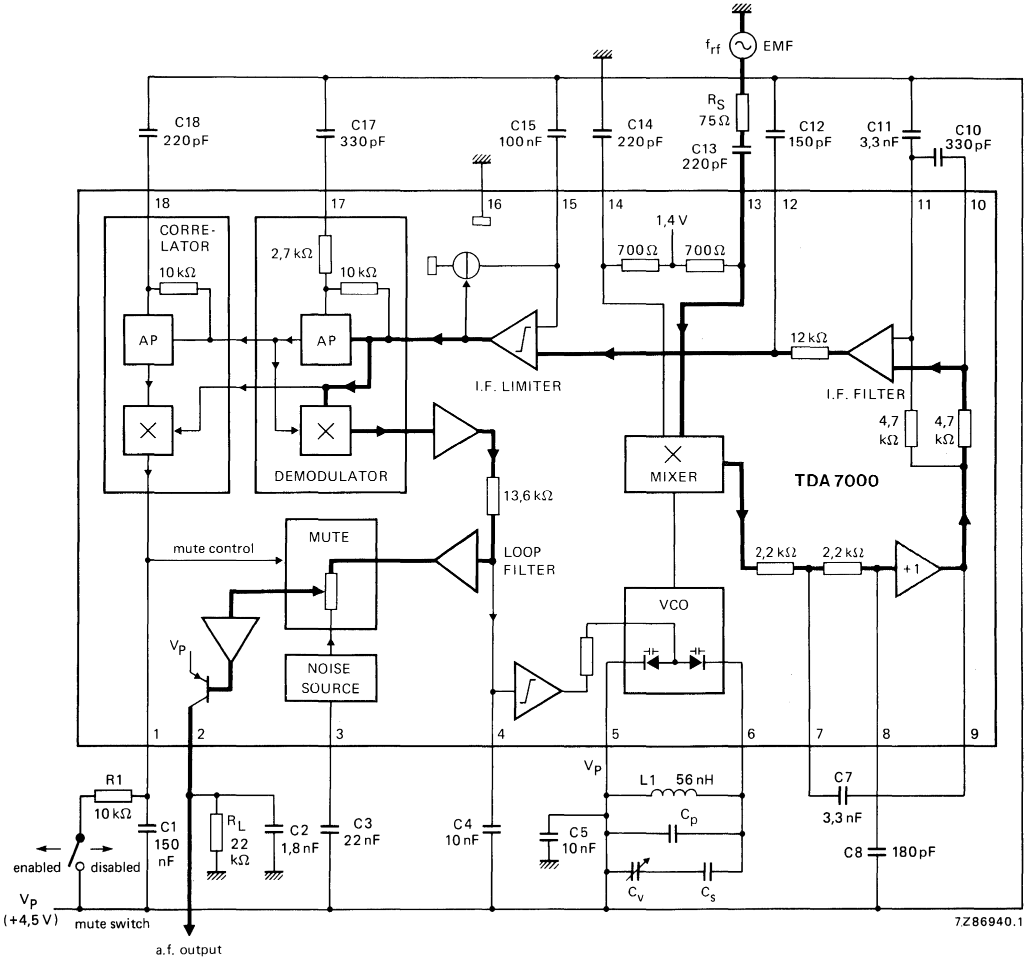


Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.

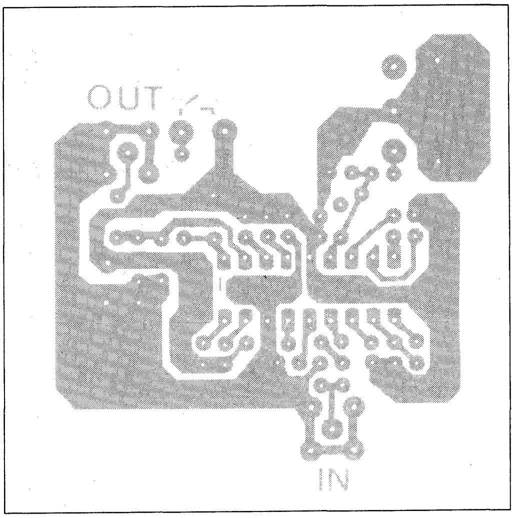


Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.

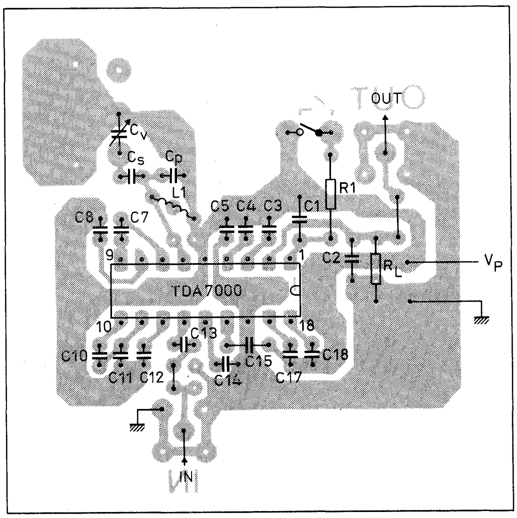


Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

Single-chip FM radio circuit TDA7021T

GENERAL DESCRIPTION

The TDA7021T integrated radio receiver circuit is for portable radios, stereo as well as mono, where a minimum of periphery is important in terms of small dimensions and low cost. It is fully compatible for applications using the low-voltage micro tuning system (MTS). The IC has a frequency locked loop (FLL) system with an intermediate frequency of 76 kHz. The selectivity is obtained by active RC filters. The only function to be tuned is the resonant frequency of the oscillator. Interstation noise as well as noise from receiving weak signals is reduced by a correlation mute system.

Special precautions have been taken to meet local oscillator radiation requirements. Because of the low intermediate frequency, low pass filtering of the MUX signal is required to avoid noise when receiving stereo. 50 kHz roll-off compensation, needed because of the low pass characteristic of the FLL, is performed by the integrated LF amplifier. For mono application this amplifier can be used to directly drive an earphone. The field-strength detector enables field-strength dependent channel separation control.

Features

- RF input stage
- Mixer
- Local oscillator
- IF amplifier/limiter
- Frequency detector
- Mute circuit
- MTS compatible
- Loop amplifier
- Internal reference circuit
- LF amplifier for
  - mono earphone amplifier or
  - MUX filter
- Field-strength dependent channel separation control facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	1,8	–	6,0	V
Supply current	$V_P = 3$ V	I_4	–	6,3	–	mA
RF input frequency		f_{rf}	1,5	–	110	MHz
Sensitivity (e.m.f.) for –3 dB limiting	source impedance = 75 Ω; mute disabled	EMF	–	4	–	μV
Signal handling (e.m.f.)	source impedance = 75 Ω	EMF	–	200	–	mV
AF output voltage		V_o	–	90	–	mV

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

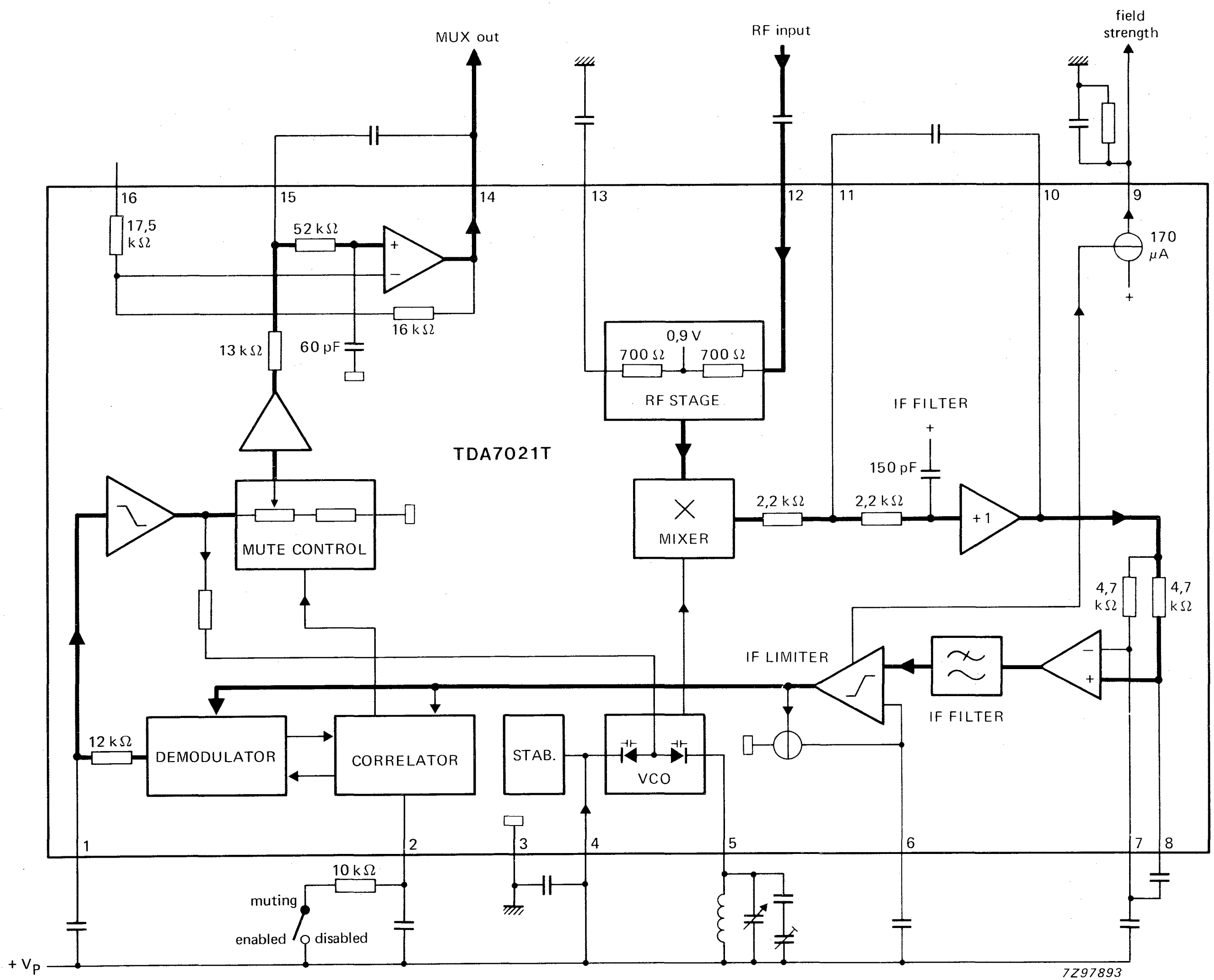


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4\text{-}3}$	–	7,0	V
Oscillator voltage		$V_{5\text{-}4}$	V_P–0,5	V_P + 0,5	V
Storage temperature range		T_{stg}	–55	+150	^oC
Operating ambient temperature range		T_{amb}	–10	+70	^oC

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 300 K/W

DC CHARACTERISTICS

V_P = 3 V, T_{amb} = 25 ^oC, measured in circuit of Fig. 4, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4\text{-}3}$	1,8	3,0	6,0	V
Supply current	V_P = 3 V	I_4	–	6,3	–	mA
Oscillator current		I_5	–	250	–	μA
Voltage at pin 13		$V_{13\text{-}3}$	–	0,9	–	V
Output voltage (pin 14)		$V_{14\text{-}3}$	–	1,3	–	V

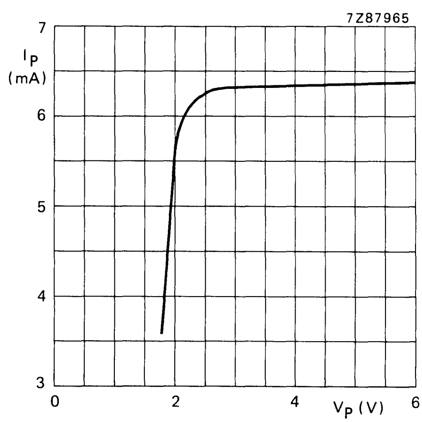


Fig. 2 Supply current as a function of the supply voltage.

AC CHARACTERISTICS (MONO OPERATION)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 5; f_{rf} = 96 MHz modulated with $\Delta f = \pm$ 22,5 kHz; f_m = 1 kHz; EMF = 0,3 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity (e.m.f.)	see Fig. 3					
for −3 dB limiting	muting disabled	EMF	–	4,0	–	µV
for −3 dB muting		EMF	–	5,0	–	µV
for (S+N)/N = 26 dB		EMF	–	7,0	–	µV
Signal handling (e.m.f.)	THD < 10%; $\Delta f = \pm$ 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio		(S+N)/N	–	60	–	dB
Total harmonic distortion	$\Delta f = \pm$ 22,5 kHz	THD	–	0,7	–	%
	$\Delta f = \pm$ 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage	ratio of AM signal (f_m = 1 kHz; m = 80%) to FM signal (f_m = 1 kHz; Δf = 75 kHz)	AMS	–	50	–	dB
Ripple rejection	ΔV_P = 100 mV; f = 1 kHz	RR	–	30	–	dB
Oscillator voltage (r.m.s. value)		$V_{5\text{-}4(rms)}$	–	250	–	mV
Variation of oscillator frequency with supply voltage	ΔV_P = 1 V	$\frac{\Delta f_{osc}}{\Delta V_P}$	–	5	–	kHz/V
Selectivity	see Fig. 9; no modulation	S_{+300}	–	46	–	dB
		S_{-300}	–	30	–	dB
AFC range		$\pm\Delta f_{rf}$	–	160	–	kHz
Mute range		$\pm\Delta f_{rf}$	–	120	–	kHz
Audio bandwidth	ΔV_o = 3 dB; measured with 50 µs pre-emphasis	B	–	10	–	kHz
AF output voltage (r.m.s. value)	R_L (pin 14) = 100 Ω	$V_{o(rms)}$	–	90	–	mV
AF output current						
max. d.c. load		$I_{o(dc)}$	−100	–	+100	µA
max. a.c. load (peak value)	THD = 10%	$I_{o(ac)}$	–	3	–	mA

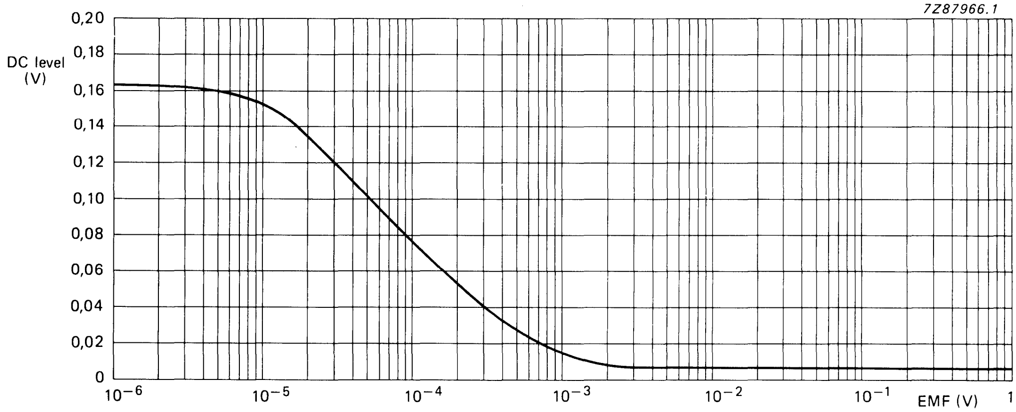


Fig. 3 Field strength voltage (V_{9-3}) at R_{source} = 1 kΩ; f = 96,75 MHz; VP = 3 V.

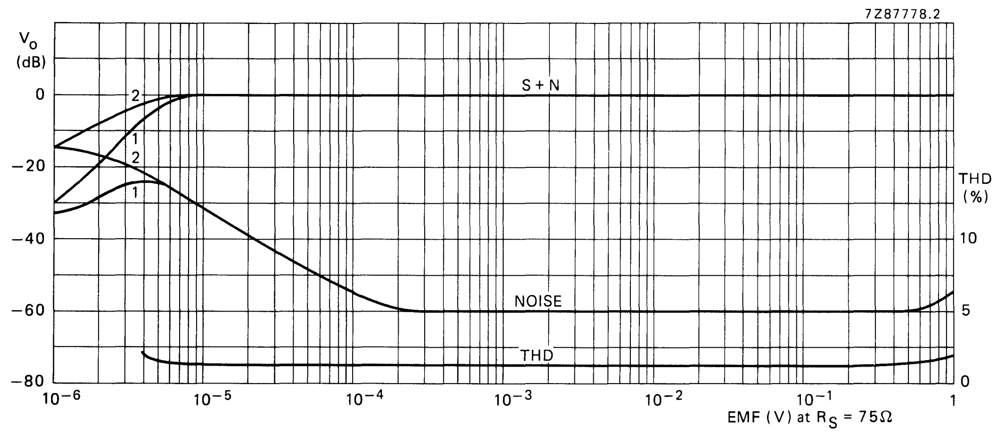
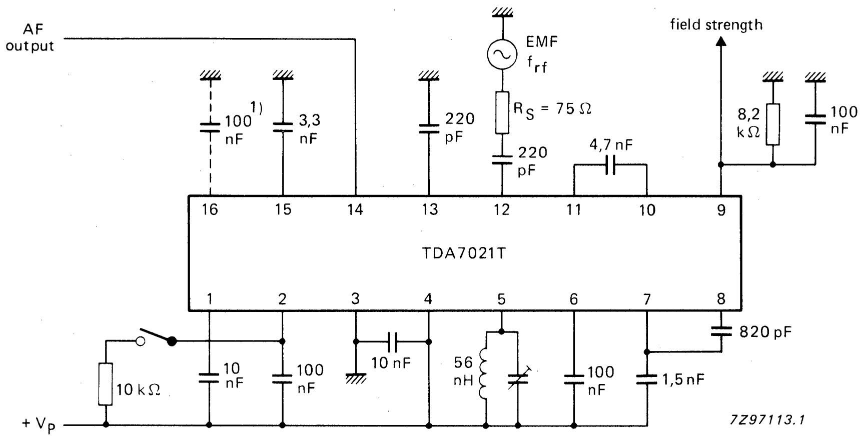


Fig. 4 Mono operation: AF output voltage (V_o) and total harmonic distortion (THD) as functions of input e.m.f. (EMF); R_{source} = 75 Ω; f_{rf} = 96 MHz; 0 dB = 90 mV. For S+N and noise curves (1) is with muting enabled and (2) is with muting disabled; signal Δf = ± 22,5 kHz and f_m = 1 kHz. For THD curve, Δf = ± 75 kHz and f_m = 1 kHz.



1) The AF output can be decreased by disconnecting the 100 nF capacitor from pin 16.

Fig. 5 Test circuit for mono operation.

AC CHARACTERISTICS (STEREO OPERATION)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 8; f_{rf} = 96 MHz modulated with pilot Δf = ± 6,75 kHz and AF signal Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 1 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity (e.m.f.) for (S+N)/N = 26 dB	see Fig. 8; pilot off	EMF	–	11	–	μV
Selectivity	see Fig. 9; no modulation	S_{+300}	–	40	–	dB
		S_{-300}	–	22	–	dB
Signal-to-noise ratio		(S+N)/N	–	50	–	dB
Channel separation	V_i = L-signal; f_m = 1 kHz; pilot on:					
	at f_{rf} = 97 MHz	α	–	26	–	dB
	at f_{rf} = 87,5 MHz and 108 MHz	α	–	14	–	dB

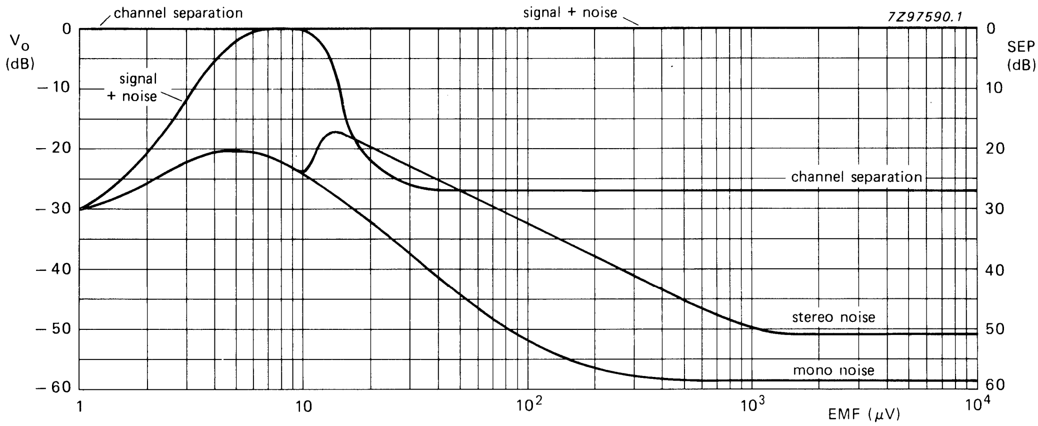


Fig. 6 Stereo operation: signal/noise and channel separation of TDA7021T when used in the circuit of Fig. 8.

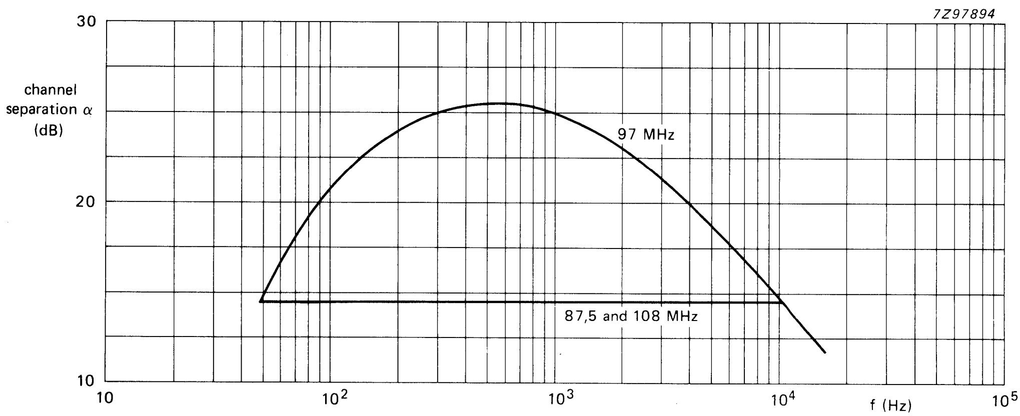


Fig. 7 Stereo operation: channel separation as a function of audio frequency in the circuit of Fig. 8.

Single-chip FM radio circuit TDA7021T

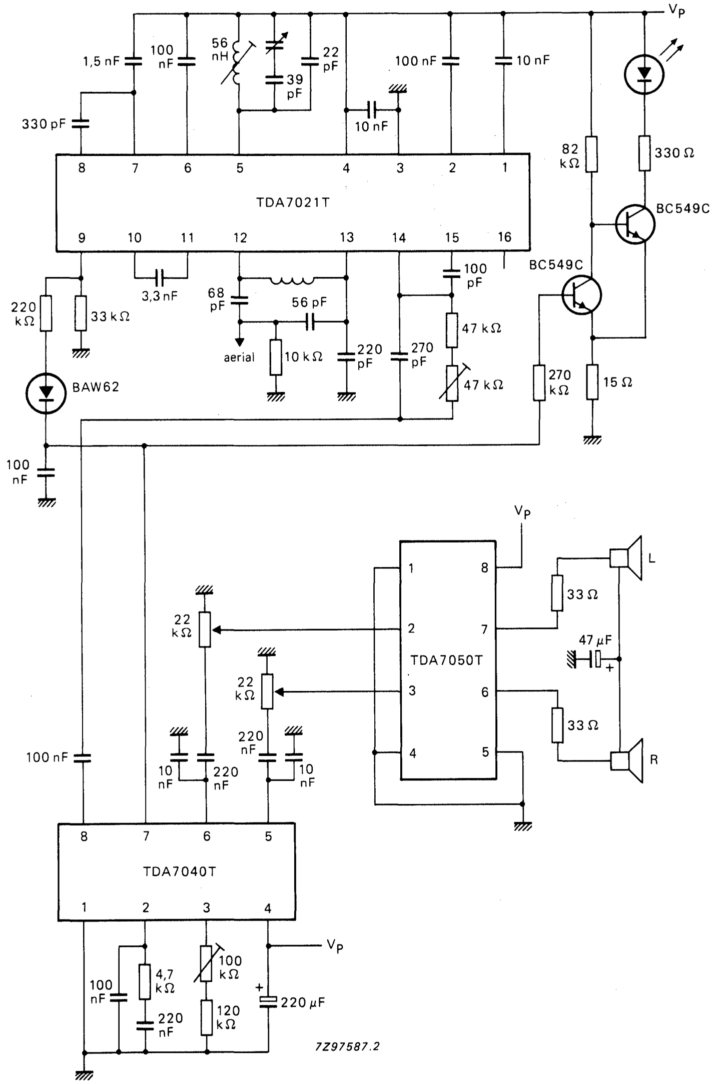


Fig. 8 Stereo application in combination with a low voltage PLL stereo decoder (TDA7040T) and a low voltage mono/stereo power amplifier (TDA7050T).

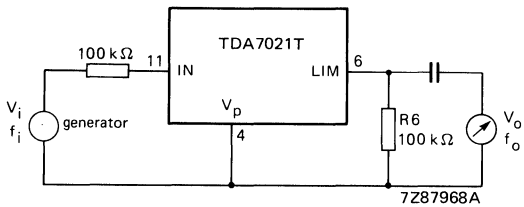


Fig. 9 Test set-up; V_i = 30 mV; f_i = 76 kHz; selective voltmeter at output has $R_i \geqslant 1$ MΩ and $C_i \leqslant 8$ pF; $f_o = f_i$.

Note to Fig. 9

This test set-up is to incorporate the circuit of Fig. 5 for mono operation or the circuit of Fig. 8 for stereo operation. For either circuit, replace the 100 nF capacitor at pin 6 with R6 (100 kΩ) as shown above.

Selectivity

$$S_{+300} = 20 \log \frac{V_o \mid (300\ \text{kHz} - f_i)}{V_o \mid f_i}$$

$$S_{-300} = 20 \log \frac{V_o \mid (300\ \text{kHz} + f_i)}{V_o \mid f_i}$$

Signetics

Section 4
Mixers

RF Communications

INDEX

Balanced modulator/demodulator

MC1496/MC1596

DESCRIPTION

The MC1496 is a monolithic double-balanced modulator/demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The MC1596 will operate over the full military temperature range of -55 to +125°C. The MC1496 is intended for applications within the range of 0 to +70°C.

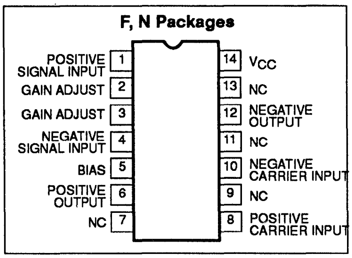
FEATURES

- Excellent carrier suppression
  65dB typ @ 0.5MHz
  50dB typ @ 10MHz
- Adjustable gain and signal handling
- Balanced inputs and outputs
- High common-mode rejection—85dB typ

APPLICATIONS

- Suppressed carrier and amplitude modulation
- Synchronous detection
- FM detection
- Phase detection
- Sampling
- Single sideband
- Frequency doubling

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Cerdip	0 to +70°C	MC1496F
14-Pin Plastic	0 to +70°C	MC1496N
14-Pin Cerdip	-55 to +125°C	MC1596F
14-Pin Plastic	-55 to +125°C	MC1596N

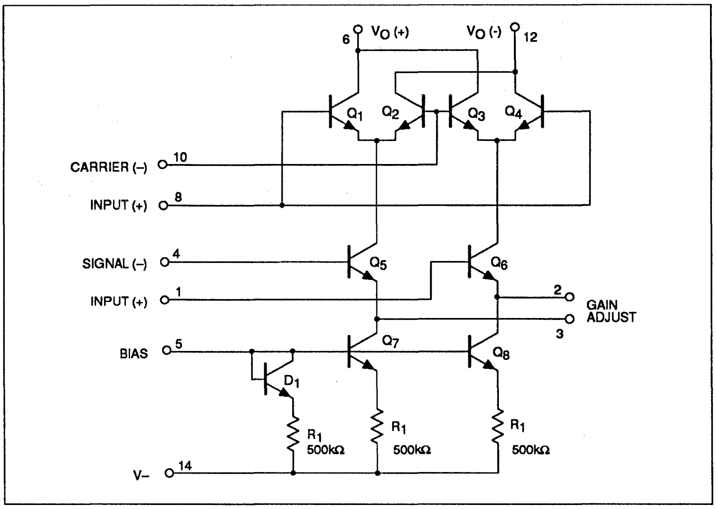
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Applied voltage	30	V
V_8-V_{10}	Differential input signal	±5.0	V
V_4-V_1	Differential input signal	$(5 \pm I_5 R_e)$	V
V_2-V_1, V_3-V_4	Input signal	5.0	V
I_5	Bias current	10	mA
P_D	Maximum power dissipation, T_A=25°C (still-air)[1] F package N package	 1190 1420	 mW mW
T_A	Operating temperature range MC1496 MC1596	 0 to +70 -55 to +125	 °C °C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

V_{CC}=+12V_{DC}; V_{CC}=-8.0V_{DC}; I5=1.0mADC; R_L=3.9kΩ; R_E=1.0kΩ; T_A=25°C, unless otherwise specified.

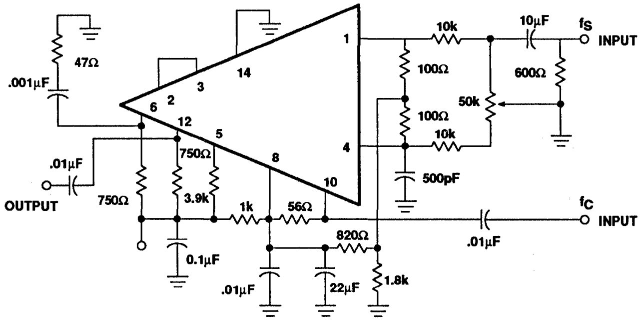
SYMBOL	PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Single-ended input impedance	Signal port, f=5.0MHz							
R_{IP}	Parallel input resistance			200			200		kΩ
C_{IP}	Parallel input capacitance			2.0			2.0		pF
	Single-ended output impedance	f=10MHz							
R_{OP}	Parallel output resistance			40			40		kΩ
C_{OP}	Parallel output capacitance			5.0			5.0		pF
	Input bias current								µA
I_{BS}	I_{BS}=			12	25		12	30	
I_{BC}	I_{BC}=			12	25		12	30	µA
	Input offset current								µA
I_{IOS}	$I_{IOS}=I_1-I_4$			0.7	5.0		0.7	7.0	
I_{IOC}	$I_{IOC}=I_8-I_{10}$			0.7	5.0		0.7	7.0	µA
T_CI_{IO}	Average temperature coefficient of input offset current			2.0			2.0		nA/°C
	Output offset current								
I_{OO}	I_6-I_{12}			14	50		15	80	µA
T_CI_{OO}	Average temperature coefficient of output offset current			90			90		nA/°C
	Common-mode quiescent								
V_O	output voltage (Pin 6 or Pin 12)			8.0			8.0		V_{DC}
	Power supply current								mA_{DC}
I_{D+}	I_6+I_{12}			2.0	3.0		2.0	4.0	
I_{D-}	I_{14}			3.0	4.0		3.0	5.0	
P_D	DC power dissipation			33			33		mW

AC ELECTRICAL CHARACTERISTICS

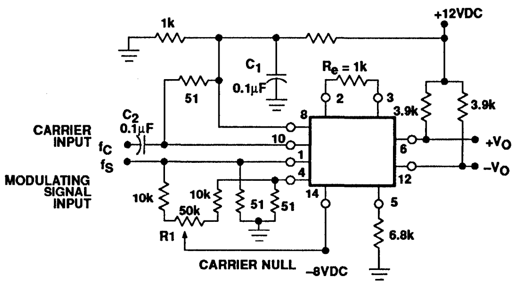
V_{CC}=+12$_{DC}$; V_{CC}=-9.0V_{DC}; I_5=1.0mA_{DC}; R_L=3.9kΩ; R_E=1.0kΩ; T_A=+25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CFT}	Carrier feedthrough	V_C=60mV_{RMS} sinewave and offset adjusted to zero							
		f_C=1.0kHz		40			40		μV_{RMS}
		f_C=10MHz		140			140		
		V_C=300mV_{P-P} squarewave:							
		Offset adjusted to zero f_C=1.0kHz		0.04	0.2		0.04	0.4	mV_{RMS}
		Offset not adjusted f_C=1.0kHz		20	100		20	200	
V_{CS}	Carrier suppressions	f_S=10kHz, 300mV_{RMS} sinewave							
		f_C=500kHz, 60mV_{RMS} sinewave	50	65		40	65		dB
		f_C=10MHz, 60mV_{RMS} sinewave		50			50		
BW_{3dB}	Transadmittance bandwidth (Magnitude) (R_L=50Ω)	Carrier input port, V_C=60mV_{RMS} sinewave f_S=1.0kHz, 300mV_{RMS} sinewave		300			300		MHz
		Signal input port, V_S=300mV_{RMS} sinewave $\|V_C\|$ = 0.5V_{DC}		80			80		MHz
A_{VS}	Signal gain	V_S=100mV_{RMS}; f=1.0kHz $\|V_C\|$ = 0.5V_{DC}	2.5	3.5		2.5	3.5		V/V
CMV	Common-mode input swing	Signal port, f_S=1.0kHz		5.0			5.0		V_{P-P}
A_{CM}	Common-mode gain	Signal port, f_S=1.0kHz $\|V_C\|$ = 0.5V_{DC}		-85			-85		dB
DV_{OUT}	Differential output voltage swing capability			8.0			8.0		V_{P-P}

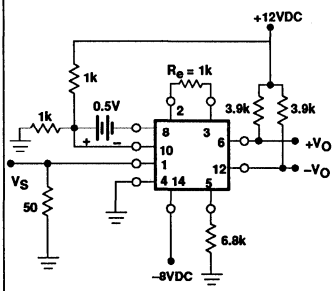
TEST CIRCUITS



Carrier Rejection and Suppression



Carrier Rejection and Suppression



Signal Gain and Output Swing

Balanced modulator/demodulator applications using the MC1496/1596

BALANCED MODULATOR/DEMODULATOR APPLICATIONS USING MC1496/MC1596

The MC1496 is a monolithic transistor array arranged as a balanced modulator-demodulator. The device takes advantage of the excellent matching qualities of monolithic devices to provide superior carrier and signal rejection. Carrier suppressions of 50dB at 10MHz are typical with no external balancing networks required.

Applications include AM and suppressed carrier modulators, AM and FM demodulators, and phase detectors.

THEORY OF OPERATION

As Figure 1 suggests, the topography includes three differential amplifiers. Internal connections are made such that the output becomes a product of the two input signals V_C and V_S.

To accomplish this the differential pairs Q1-Q2 and Q3-Q4, with their cross-coupled collectors, are driven into saturation by the zero crossings of the carrier signal V_C. With a low level signal, V_S driving the third differential amplifier Q5-Q6, the output voltage will be full wave multiplication of V_C and V_S. Thus for sine wave signals, V_{OUT} becomes:

$$V_{OUT} = E_X E_Y \left[\cos(\omega x + \omega y)t + \cos(\omega x - \omega y)t\right] \quad (1)$$

As seen by equation (1) the output voltage will contain the sum and difference frequencies of the two original signals. In addition, with the carrier input ports being driven into saturation, the output will contain the odd harmonics of the carrier signals. (See Figure 4.)

Internally provided with the device are two current sources driven by a temperature-compensated bias network. Since the transistor geometries are the same and since V_{BE} matching in monolithic devices is excellent, the currents through Q_7 and Q_8 will be identical to the current set at Pin 5. Figures 2 and 3 illustrate typical biasing arrangements from split and single-ended supplies, respectively.

Of primary interest in beginning the bias circuitry design is relating available power supplies and desired output voltages to device requirements with a minimum of external components.

The transistors are connected in a cascode fashion. Therefore, sufficient collector voltage must be supplied to avoid saturation if linear operation is to be achieved. Voltages greater than 2V are sufficient in most applications.

Biasing is achieved with simple resistor divider networks as shown in Figure 3. This configuration assumes the presence of symmetrical supplies. Explaining the DC biasing technique is probably best accomplished by an example. Thus, the initial assumptions and criteria are set forth:

1. Output swing greater than $4V_{P-P}$.
2. Positive and negative supplies of 6V are available.
3. Collector current is 2mA. It should be noted here that the collector output current is equal to the current set in the current sources.

As a matter of convenience, the carrier signal ports are referenced to ground. If desired, the modulation signal ports could be ground referenced with slight changes in the bias arrangement. With the carrier inputs at DC ground, the quiescent operating point of the outputs should be at one-half the total positive voltage or 3V for this case. Thus, a collector load resistor is selected which drops 3V at 2mA or 1.5kΩ. A quick check at this point reveals that with these loads and current levels the peak-to-peak output swing will be greater than 4V. It remains to set the current source level and proper biasing of the signal ports.

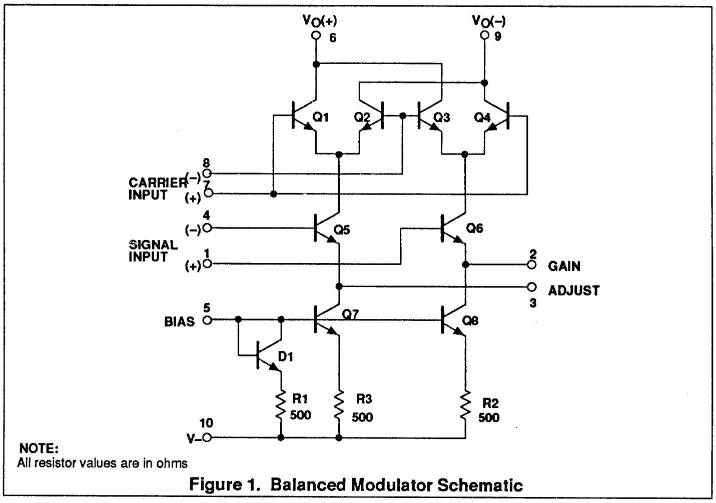
The voltage at Pin 5 is expressed by

$$V_{BIAS} = V_{BE} = 500 \cdot I_S$$

where I_S is the current set in the current sources.

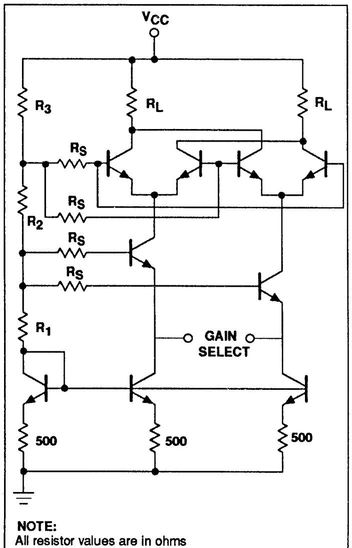
BIASING

Since the MC1496 was intended for a multitude of different functions as well as a myriad of supply voltages, the biasing techniques are specified by the individual application. This allows the user complete freedom to choose gain, current levels, and power supplies. The device can be operated with single-ended or dual supplies.



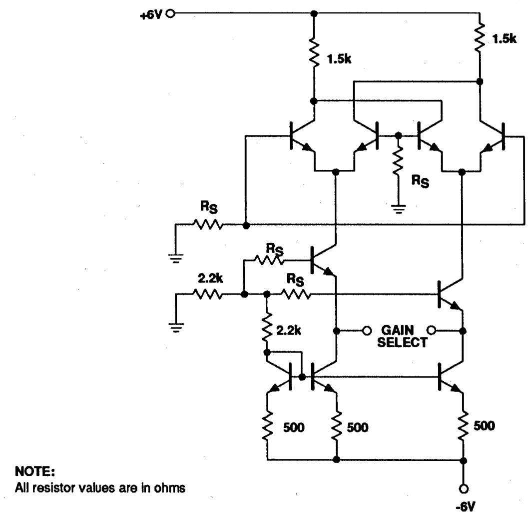
NOTE:
All resistor values are in ohms

Figure 1. Balanced Modulator Schematic



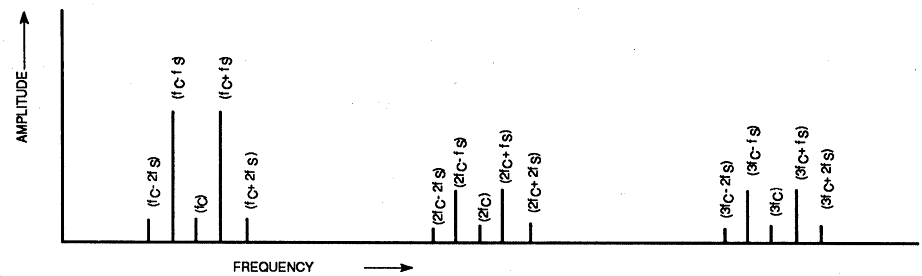
NOTE:
All resistor values are in ohms

Figure 2. Single-Supply Biasing



NOTE:
All resistor values are in ohms

Figure 3. Dual Supply Biasing



NOTES:
f_C Carrier Fundamental
f_S Modulating Signal
$f_C \pm f_S$ Fundamental Carrier Sidebands
$f_C \pm nf_S$ Fundamental Carrier Sideband Harmonics
nf_C Carrier Harmonics
$nf_C \pm nf_S$ Carrier Harmonic Sidebands

Figure 4. Modulator Frequency Spectrum

$V_{BIAS} = V_{BE} = 500 \times I_S$

where I_S is the current set in the current sources.

For the example V_{BE} is 700mV at room temperature and the bias voltage at Pin 5 becomes 1.7V. Because of the cascode configuration, both the collectors of the current sources and the collectors of the signal transistors must have some voltage to operate properly. Hence, the remaining voltage of the negative supply (–6V+1.7V=–4.3V) is split between these transistors by biasing the signal transistor bases at –2.15V. Countless other bias arrangements can be used with other power supply voltages. The important thing to remember is that sufficient DC voltage is applied to each bias point to avoid collector saturation over the expected signal wings.

BALANCED MODULATOR

In the primary application of balanced modulation, generation of double sideband suppressed carrier modulation is accomplished. Due to the balance of both modulation and carrier inputs, the output, as mentioned, contains the sum and difference frequencies while attenuating the fundamentals. Upper and lower sideband signals are the strongest signals present with harmonic sidebands being of diminishing amplitudes as characterized by Figure 4.

Gain of the 1496 is set by including emitter degeneration resistance located as R_E in Figure 5. Degeneration also allows the maximum signal level of the modulation to be increased. In general, linear response defines the maximum input signal as

$V_S \leq 15 \bullet R_E$ (Peak)

and the gain is given by

$$A_{VS} = \frac{R_L}{R_E + 2r_e} \quad (2)$$

This approximation is good for high levels of carrier signals. Table 1 summarizes the gain for different carrier signals.

As seen from Table 1, the output spectrum suffers an amplitude increase of undesired sideband signals when either the modulation or carrier signals are high. Indeed, the modulation level can be increased if R_E is increased without significant consequence. However, large carrier signals cause odd harmonic sidebands (Figure 4) to increase. At the same time, due to imperfections of the carrier waveforms and small imbalances of the device, the second harmonic rejection will be seriously degraded. Output filtering is often used with high carrier levels to remove all but the desired sideband. The filter removes unwanted signals while the high carrier level guards against amplitude variations and maximizes gain. Broadband modulators, without benefit of filters, are implemented using low carrier and modulation signals to maximize linearity and minimize spurious sidebands.

AM MODULATOR

The basic current of Figure 5 allows no carrier to be present in the output. By adding offset to the carrier differential pairs, controlled amounts of carrier appear at the output whose amplitude becomes a function of the modulation signal or AM modulation. As shown, the carrier null circuit is changed from Figure 5 to have a wider range so that wider control is achieved. All connections are shown in Figure 6.

AM DEMODULATION

As pointed out in Equation 1, the output of the balanced mixer is a cosine function of the angle between signal and carrier inputs. Further, if the carrier input is driven hard enough to provide a switching action, the output becomes a function of the input amplitude. Thus the output amplitude is maximum when there is 0° phase difference as shown in Figure 7.

Amplifying and limiting of the AM carrier is accomplished by IF gain block providing 55dB of gain or higher with limiting of 400µV. The limited carrier is then applied to the detector at the carrier ports to provide the desired switching function. The signal is then demodulated by the synchronous AM demodulator (1496) where the carrier frequency is attenuated due to the balanced nature of the device. Care must be taken not to overdrive the signal input so that distortion does not appear in the recovered audio. Maximum conversion gain is reached when the carrier signals are in phase as indicated by the phase-gain relationship drawn in Figure 7.

Output filtering will also be necessary to remove high frequency sum components of the carrier from the audio signal.

PHASE DETECTOR

The versatility of the balanced modulator or multiplier also allows the device to be used as a phase detector. As mentioned, the output of the detector contains a term related to the cosine of the phase angle. Two signals of equal frequency are applied to the inputs as per Figure 8. The frequencies are multiplied together producing the sum and difference frequencies. Equal frequencies cause the difference component to become DC while the undesired sum component is filtered out. The DC component is related to the phase angle by the graph of Figure 9.

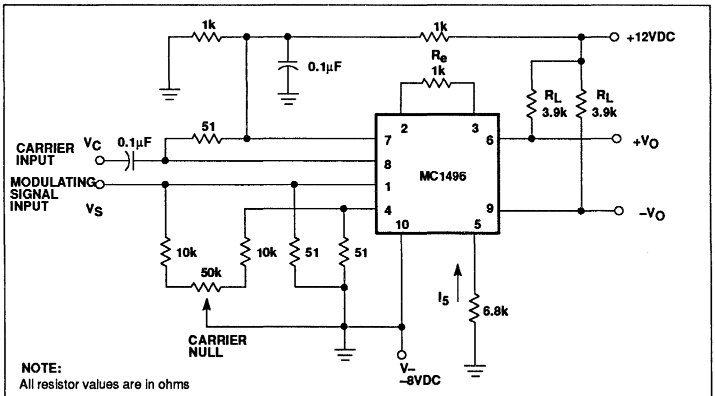


Figure 5. Double Suppressed Carrier Modulator

Table 1. Voltage Gain and Output vs Input Signal

CARRIER INPUT SIGNAL (V_C)	APPROXIMATE VOLTAGE GAIN	OUTPUT SIGNAL FREQUENCY(S)
Low-level DC	$\frac{R_L V_C}{2(R_E + 2r_E)\left(\frac{KT}{q}\right)}$	f_M
High-level DC	$\frac{R_L}{R + 2r_e}$	f_M
Low-level AC	$\frac{R_L V_C\ (rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level AC	$\frac{0.637 R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$. $5f_C \pm f_M$...

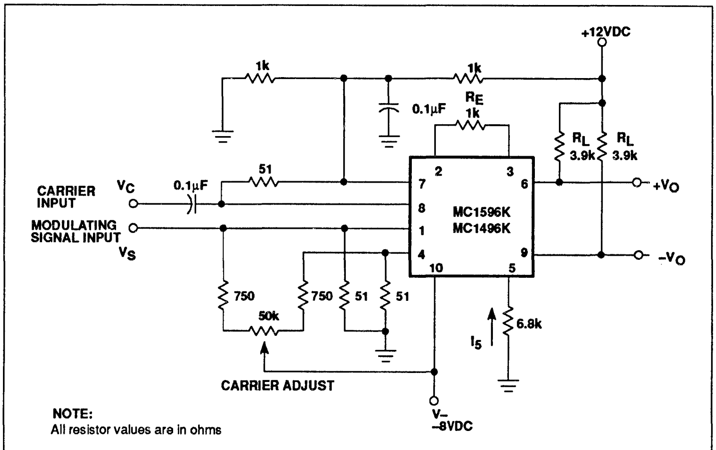


Figure 6. AM Modulator

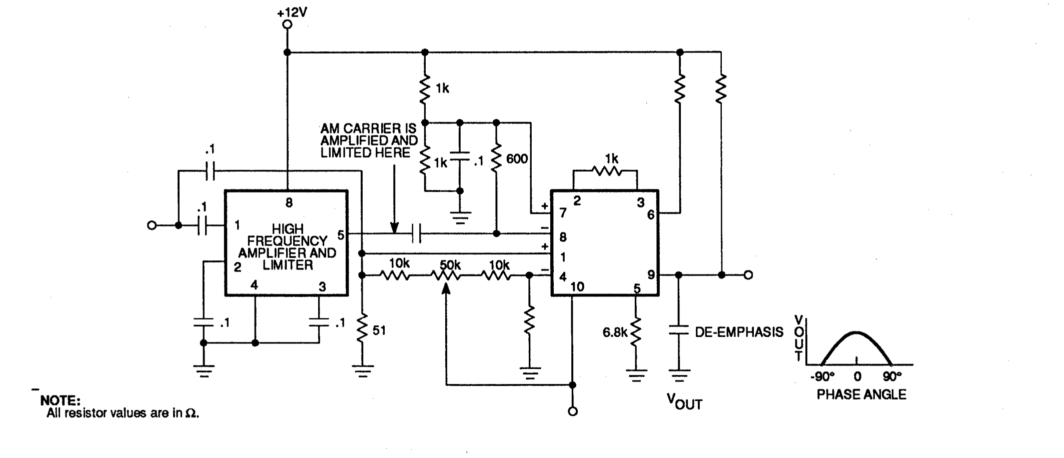


Figure 7. AM Demodulator

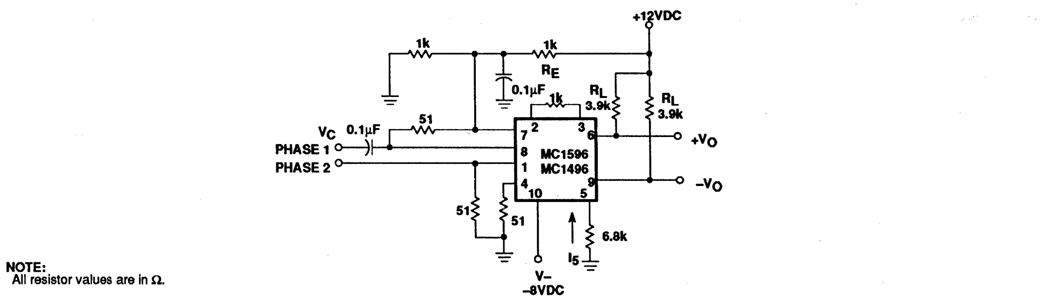


Figure 8. Phase Comparator

At 90° the cosine becomes zero, while being at maximum positive or maximum negative at 0° and 180°, respectively.

The advantage of using the balanced modulator over other types of phase comparators is the excellent linearity of conversion. This configuration also provides a conversion gain rather than a loss for greater resolution. Used in conjunction with a phase-locked loop, for instance, the balanced modulator provides a very low distortion FM demodulator.

FREQUENCY DOUBLER

Very similar to the phase detector of Figure 8, a frequency doubler schematic is shown in Figure 10. Departure from Figure 8 is primarily the removal of the low-pass filter. The output then contains the sum component which is twice the frequency of the input, since both input signals are the same frequency.

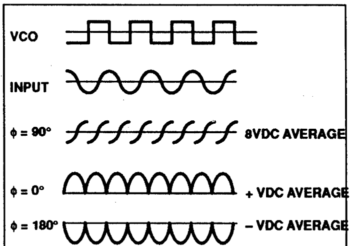


Figure 9. Phase Detector ± Voltages

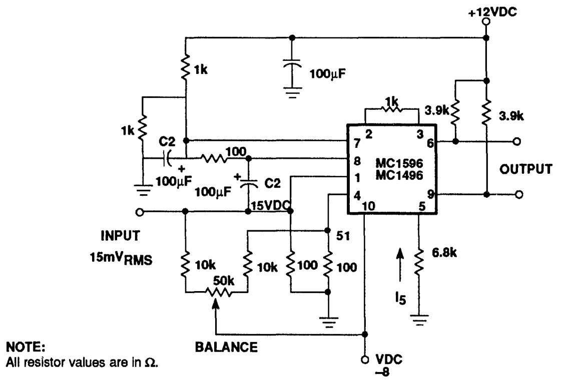


Figure 10. Low Frequency Doubler

Double-balanced mixer and oscillator

NE/SA602A

DESCRIPTION

The NE/SA602A is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602A make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external LO. For higher frequencies the LO input may be externally driven. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the NE/SA602A a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

FEATURES

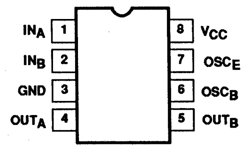
- Low current consumption: 2.4mA typical
- Excellent noise figure: <4.7dB typical at 45MHz
- High operating frequency
- Excellent gain, intercept and sensitivity
- Low external parts count; suitable for crystal/ceramic filters
- SA602A meets cellular radio specifications

APPLICATIONS

- Cellular radio mixer/oscillator
- Portable radio
- VHF transceivers
- RF data links
- HF/VHF frequency conversion
- Instrumentation frequency conversion
- Broadband LANs

PIN CONFIGURATION

F, D and N Packages



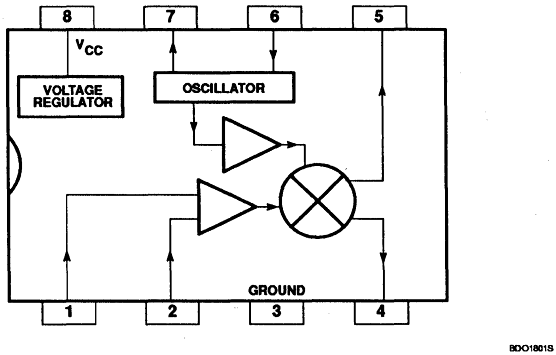
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE602AN
8-Pin Plastic SO (Surface-mount)	0 to +70°C	NE602AD
8-Pin Cerdip	0 to +70°C	NE602AFE
8-Pin Plastic DIP	-40 to +85°C	SA602AN
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA602AD
8-Pin Cerdip	-40 to +85°C	SA602AFE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE602A	0 to +70	°C
	SA602A	-40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	N package	75	°C/W

BLOCK DIAGRAM



AC/DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA602A			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figure at 45MHz			5.0	5.5	dB
	Third-order intercept point	RF_{IN} = -45dBm: f_1 = 45.0MHz f_2 = 45.06MHz		-13	-15	dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The NE/SA602A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA602A is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio second IF and demodulator, the SA602A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -13dBm (that is approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues are not critical, the input to the NE602A should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE/SA602A is designed to be flexible. The input, RF mixer output and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required LO is beyond oscillation limits, or the system calls for an external LO, the external signal can be injected at Pin 6 through a DC blocking capacitor. External LO should be at least 200mV_{P-P}.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 6 shows a Colpitts varactor tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non-critical applications.

The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. A 22kΩ resistor will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

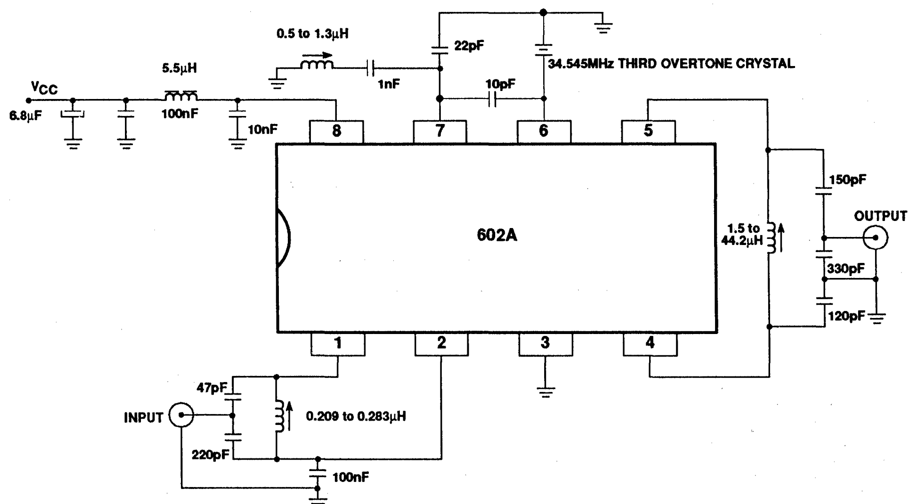


Figure 1. Test Configuration

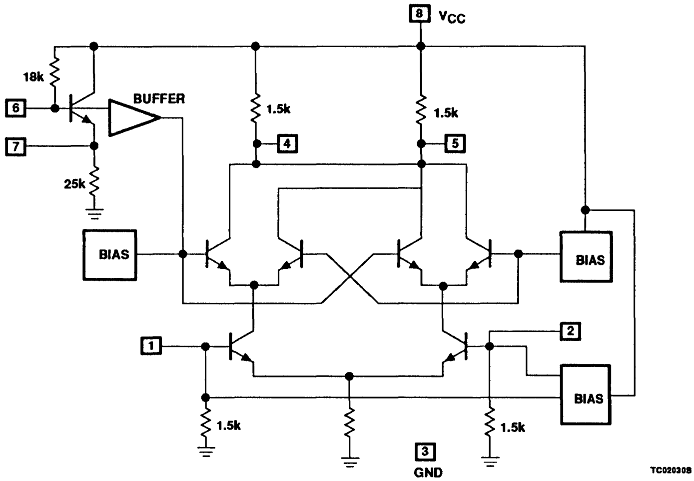
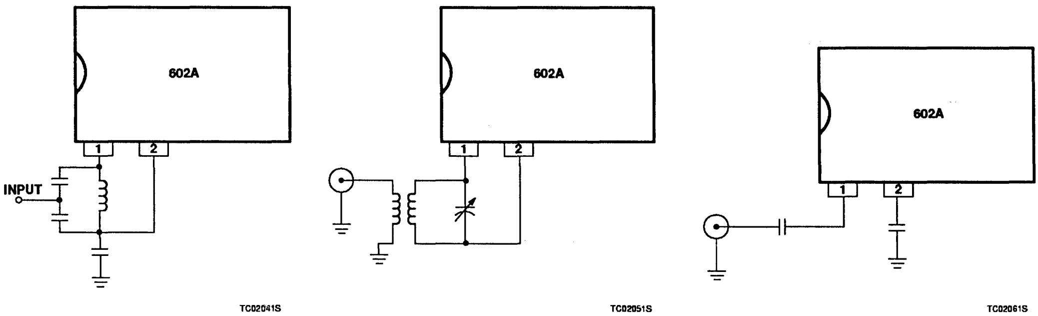


Figure 2. Equivalent Circuit



a. Single-Ended Tuned Input

b. Balanced Input (For Attenuation of Second-Order Products)

c. Single-Ended Untuned Input

Figure 3. Input Configuration

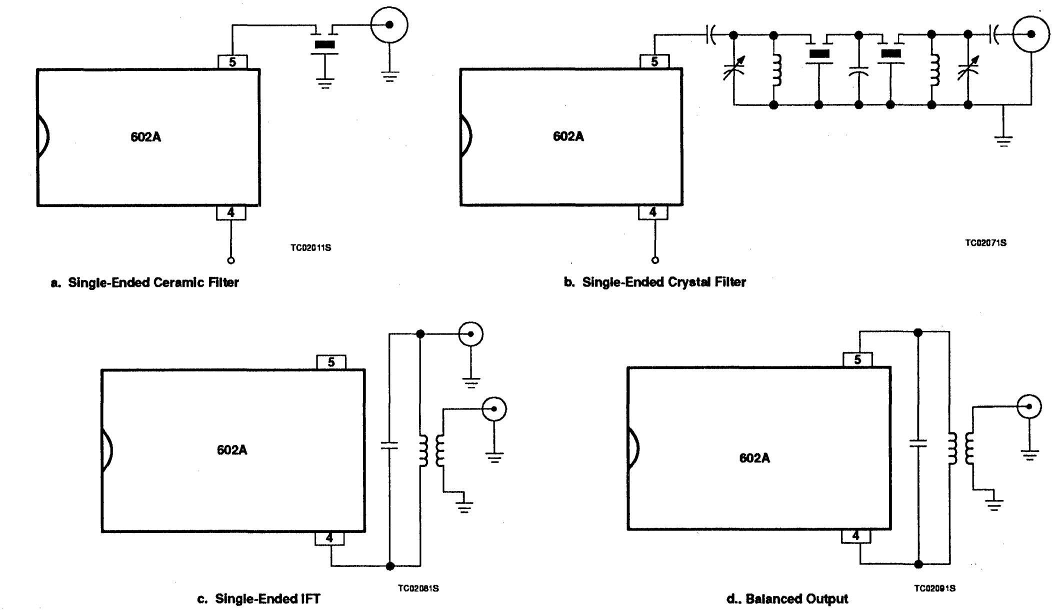


Figure 4. Output Configuration

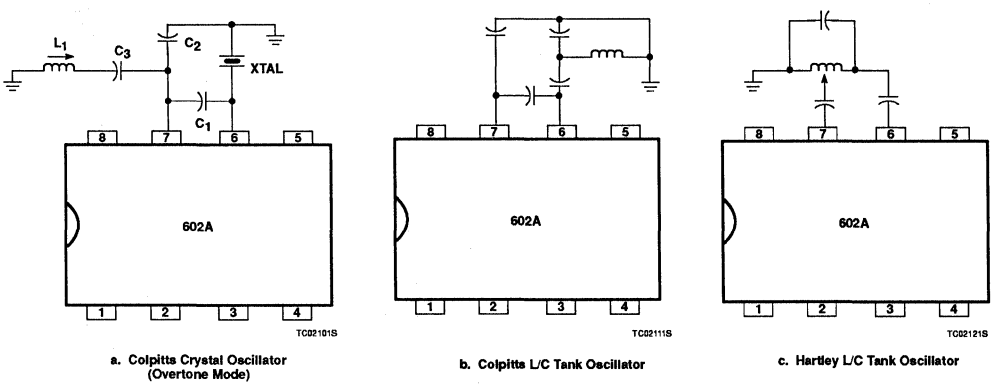


Figure 5. Oscillator Circuits

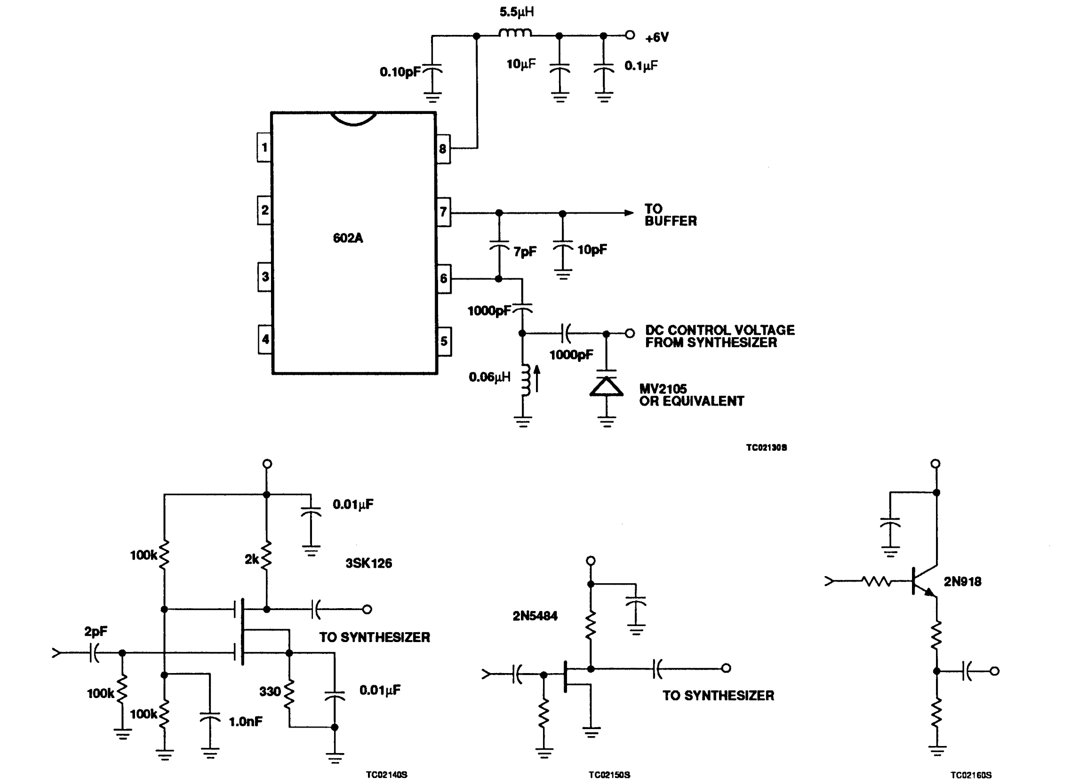


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

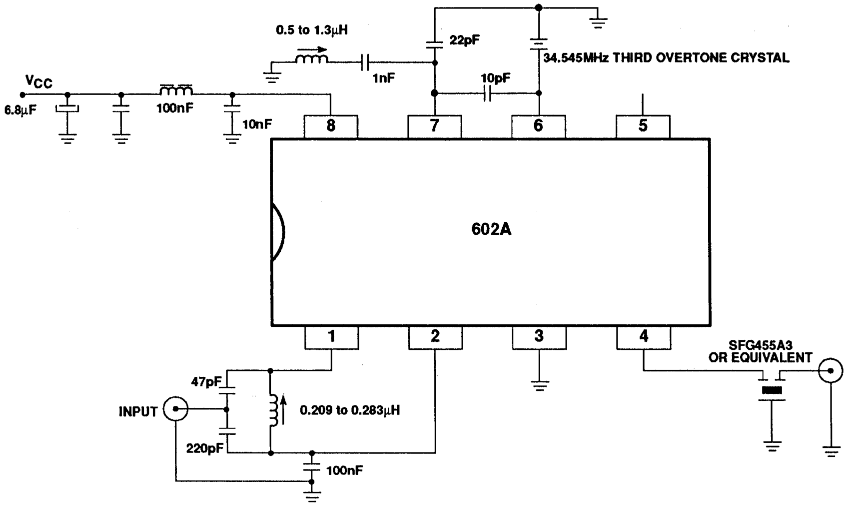


Figure 7. Typical Application for Cellular Radio

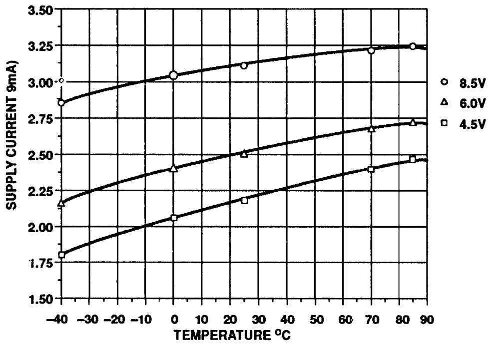


Figure 8. I_{CC} vs Supply Voltage

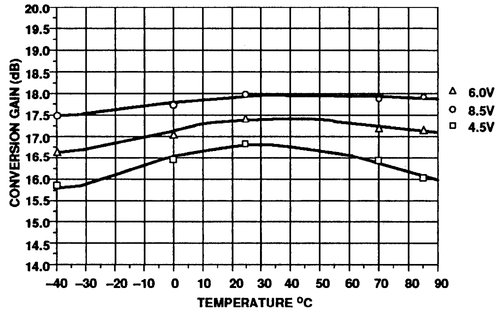


Figure 9. Conversion Gain vs Supply Voltage

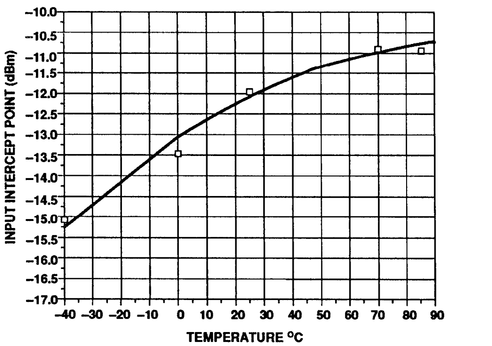


Figure 10. Third-Order Intercept Point

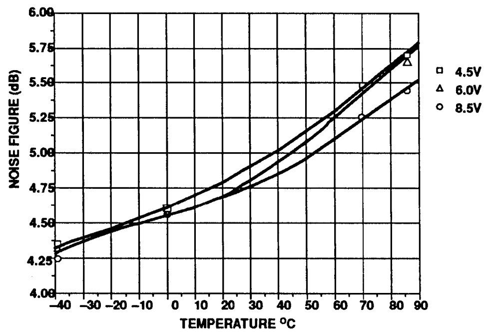


Figure 11. Noise Figure

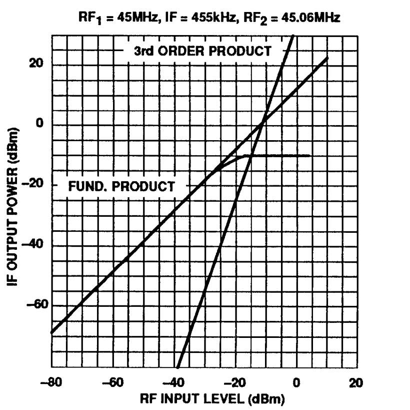


Figure 12. Third-Order Intercept and Compression

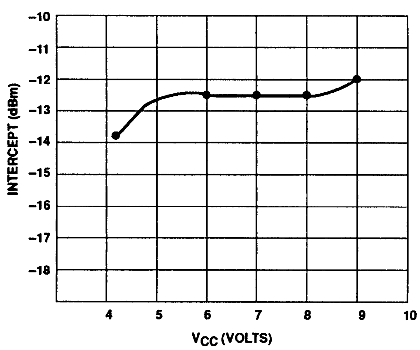


Figure 13. Input Third-Order Intermod Point vs V_{CC}

Double-balanced mixer and oscillator | NE/SA612A

DESCRIPTION

The NE/SA612A is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 45MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 45MHz is typically below 6dB and makes the device well suited for high performance cordless phone/cellular radio. The low power consumption makes the NE/SA612A excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE/SA612A is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

FEATURES

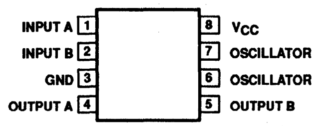
- Low current consumption
- Low cost
- Operation to 500MHz
- Low radiated energy
- Low external parts count; suitable for crystal/ceramic filter
- Excellent sensitivity, gain, and noise figure

APPLICATIONS

- Cordless telephone
- Portable radio
- VHF transceivers
- RF data links
- Sonabuoys
- Communications receivers
- Broadband LANs
- HF and VHF frequency conversion
- Cellular radio mixer/oscillator

PIN CONFIGURATION

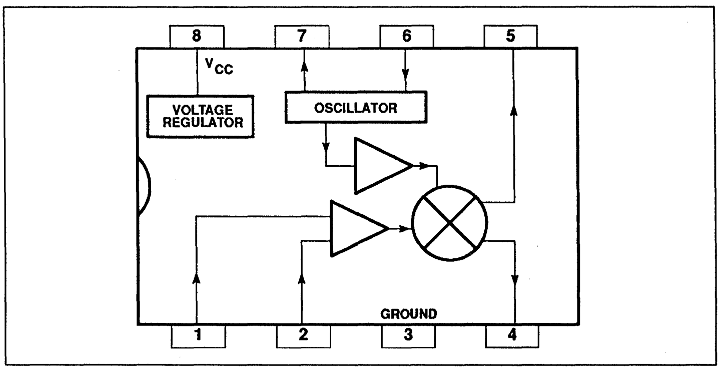
D, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE612AN
8-Pin Plastic SO (Surface-Mount)	0 to +70°C	NE612AD
8-Pin Plastic DIP	-40 to +85°C	SA612AN
8-Pin Plastic SO (Surface-Mount)	-40 to +85°C	SA612AD

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Operating ambient temperature range NE SA	 0 to +70 -40 to +85	°C

AC/DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC} = 6V, Figure 1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	3.0	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0		dB
	Third-order intercept point at 45MHz	RF_{IN}=-45dBm		-13		dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The NE/SA612A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA612A is designed for optimum low power performance. When used with the NE614A as a 45MHz cordless phone/cellular radio 2nd IF and demodulator, the NE/SA612A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE/SA612A should be appropriately scaled.

TEST CONFIGURATION

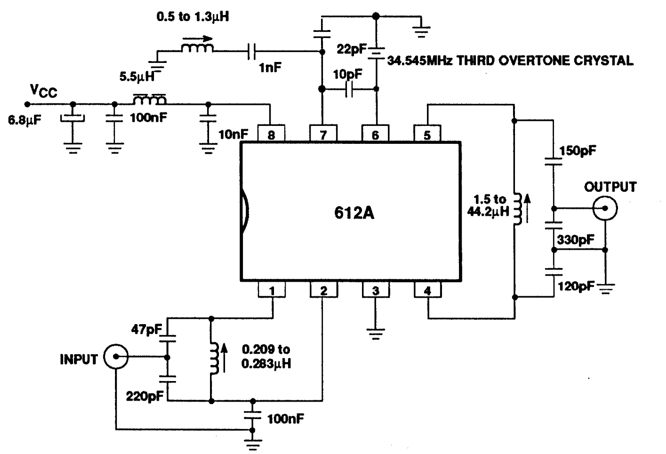


Figure 1. Test Configuration

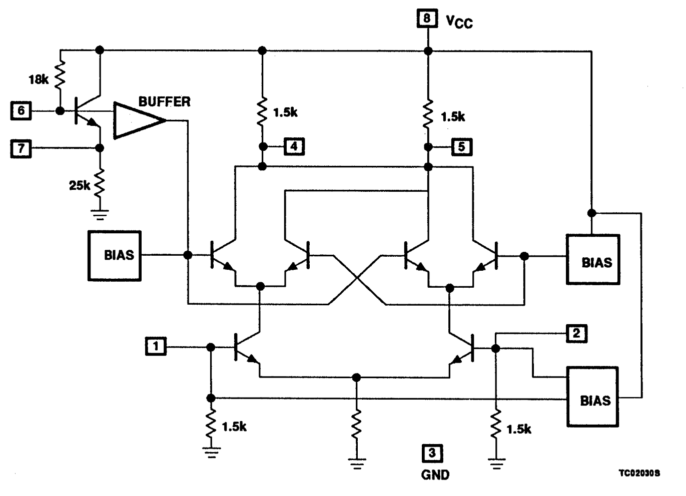


Figure 2. Equivalent Circuit

Besides excellent low power performance well into VHF, the NE/SA612A is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

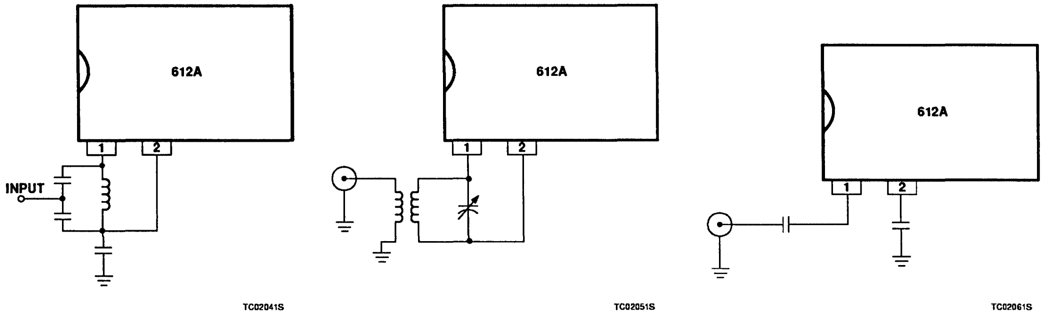
The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the

permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be 200mV_{P-P} minimum to 300mV_{P-P} maximum.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cordless phones/cellular radio. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

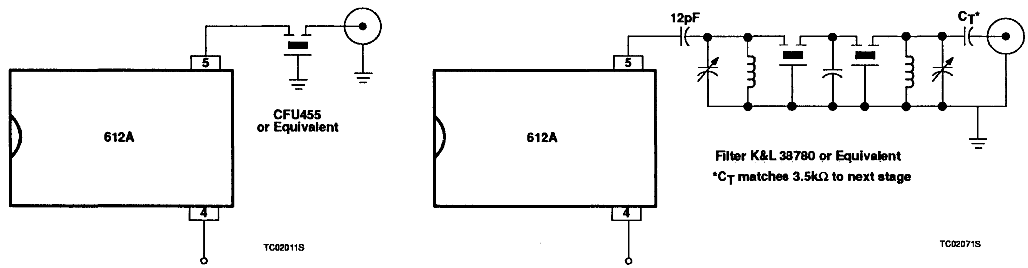


a. Single-Ended Tuned Input

b. Balanced Input (For Attenuation of Second-Order Products)

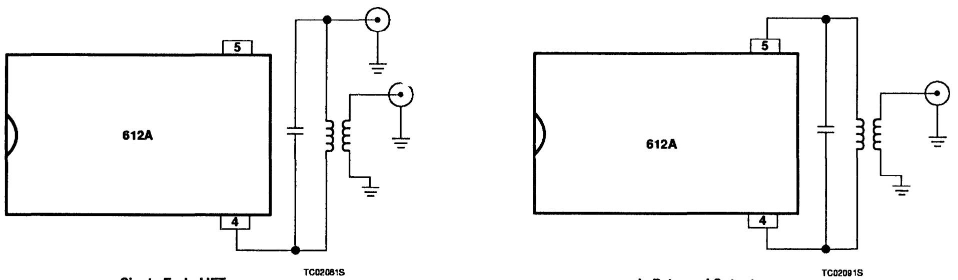
c. Single-Ended Untuned Input

Figure 3. Input Configuration



a. Single-Ended Ceramic Filter

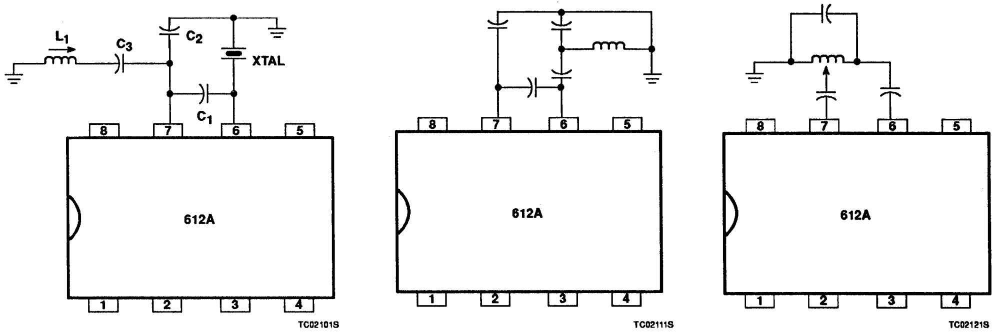
b. Single-Ended Crystal Filter



c. Single-Ended IFT

d.. Balanced Output

Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)

b. Colpitts L/C Tank Oscillator

c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

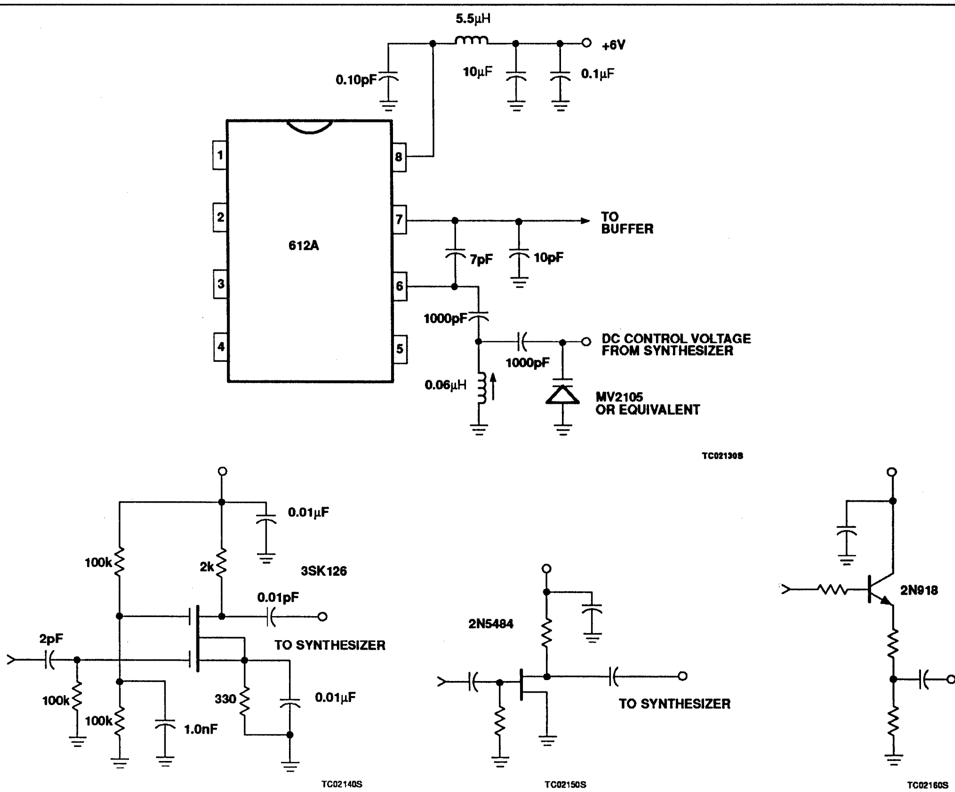


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

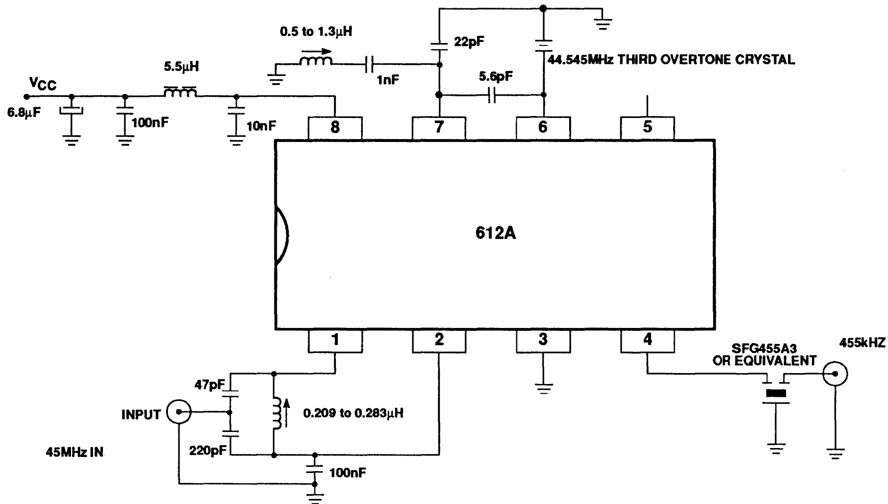


Figure 7. Typical Application for Cordless/Cellular Radio

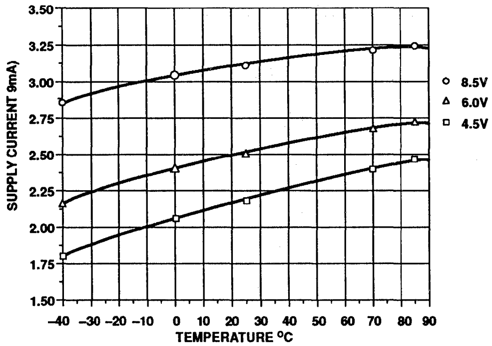


Figure 8. I_{CC} **vs Supply Voltage**

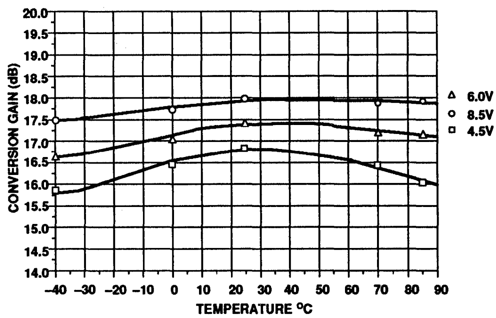


Figure 9. Conversion Gain vs Supply Voltage

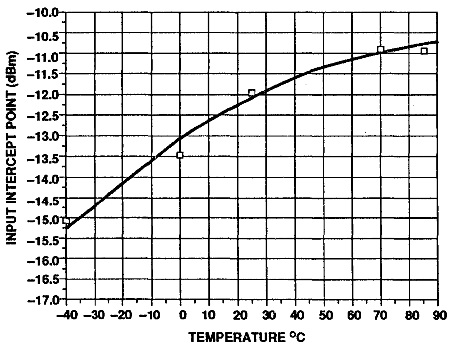


Figure 10. Third-Order Intercept Point

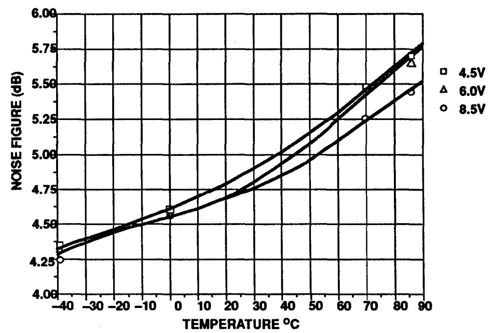


Figure 11. Noise Figure

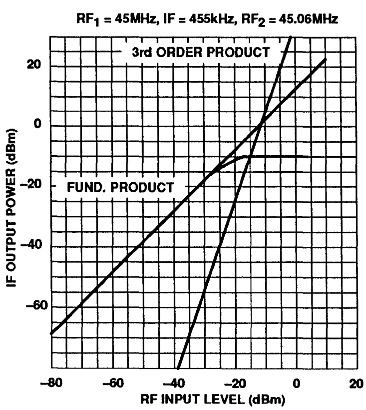


Figure 12. Third-Order Intercept and Compression

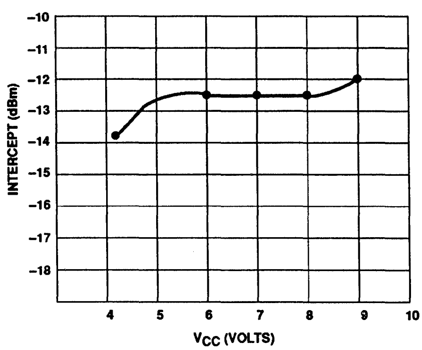


Figure 13. Input Third-Order Intermod Point vs V_{CC}

New low-power single sideband circuits

AN1981

Author: Robert J. Zavrell Jr.

INTRODUCTION

Several new integrated circuits now permit RF designers to resurrect old techniques of single-sideband generation and detection. The high cost of multi-pole crystal filters limits the use of the SSB mode to the most demanding applications, yet the advantages of SSB over full-carrier AM and FM are well documented (Ref 1 &2). The use of multi-pole filters can now be circumvented by reviving some older techniques without sacrificing performance. This has been made possible by the availability of some new RF and digital integrated circuits.

DESCRIPTION

Figure 1 shows the frequency spectrum of a 10MHz full-carrier double-sideband AM signal using a 1kHz modulating tone. This well-known type of signal is used by standard AM broadcast radio stations. Full-carrier AM's advantage is that envelope detection can be used in the receiver. Envelope detection is a simple and economical technique because it simplifies receiver circuitry. Figure 2 shows the time domain "envelope" of the same AM signal.

The 1kHz tone example of Figures 1 and 2 serves as a simple illustration of an AM signal. Typically, the sidebands contain complex waveforms for voice or data communications. In the full-carrier double sideband mode (AM), all the modulation information is contained in both sidebands, while the carrier "rides along" without contributing to the transfer of intelligence. Only one sideband without the carrier is needed to effectively transmit the modulation information. This mode is called "single-sideband suppressed carrier". Because of its reduced bandwidth, it has the advantages of improved spectrum utilization, better signal-to-noise ratios at low signal levels, and improved transmitter efficiency when compared with either FM or full-carrier AM. A finite frequency allocation using SSB can support three times the number of channels when compared with comparable FM or AM full-carrier systems.

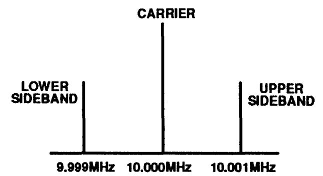


Figure 1. Frequency Domain Display of a 10MHz Carrier AM Modulated by a 1kHz Tone (Spectrum Analyzer Display)

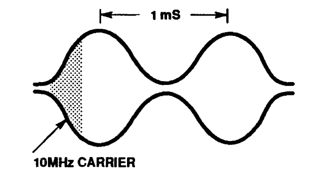


Figure 2. Time Domain Display of the Same Signal Shown in Figure 1. (Oscilloscope Display)

There are three basic methods of single-sideband generation. All three use a balanced modulator to produce a double-sideband suppressed carrier signal. The undesired sideband is then removed by phase and amplitude nulling (the phasing method), high Q multi-pole filters (the filter method), or a "third" method which is a derivation of the phasing technique called here the "Weaver" method for the apparent inventor. The reciprocal of the generator functions is employed to produce sideband detectors. Generators start with audio and produce the SSB signal; detectors receive the SSB signal and reproduce the audio. Since the sideband signal is typically produced at radio frequencies, it can be amplified and applied to an antenna or used as a subcarrier.

Reproduction of the audio signal in a full-carrier AM receiver is simplified because the carrier is present. The signal envelope, which contains the carrier and the sidebands, is applied to a non-linear device (typically a diode). The effect of envelope detection is to multiply the sideband signal by the carrier; this results in the recovery of the audio waveform. The mathematical basis for this process can be understood by studying trigonometric identities.

Since the carrier is not present in the received SSB signal, the receiver must provide it for proper audio detection. This signal from the local oscillator (LO) is applied to a mixer (multiplier) together with the SSB signal and detection occurs. This technique is called product detection and is necessary in all SSB methods. A major problem in SSB receivers is the ability to maintain accurate LO frequencies to prevent spectral shifting of the audio signal. Errors in this frequency will result in a "Donald Duck" sound which can render the signal unintelligible for large frequency errors.

Theory of Single-Sideband Detection

Figures 3 through 8 illustrate the three methods of SSB generation and detection. Since they are reciprocal operations, the circuitry for generation and detection is similar with all three methods. Duplication of critical circuitry is easy to accomplish in transceiver applications by using appropriate switching circuits.

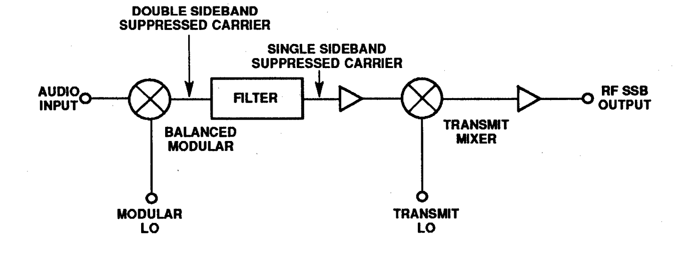


Figure 3. Filter Method SSB Generator

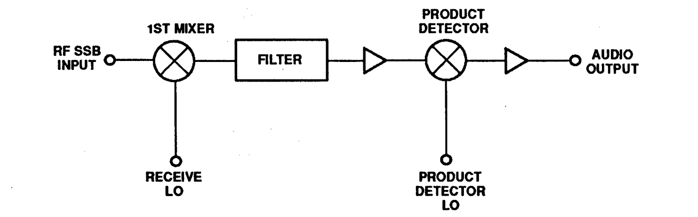


Figure 4. Filter Method SSB Detector

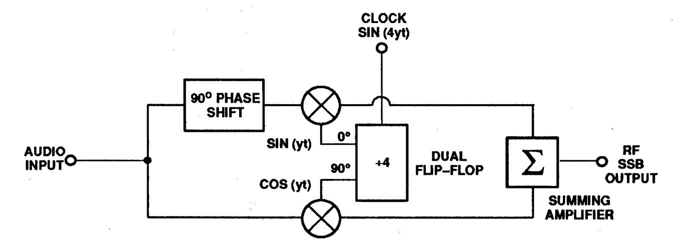


Figure 5. Phasing Method Generator

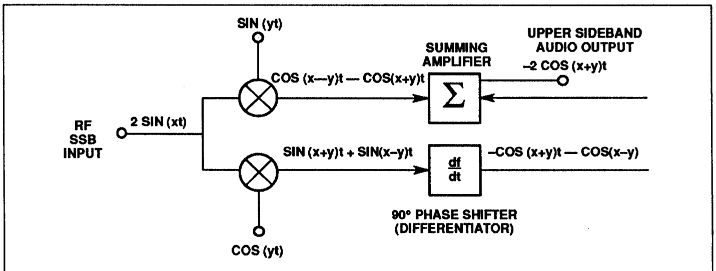


Figure 6. Phasing Method Detector with Simplified Mathematical Model

Figures 3 and 4 show the generation and detection techniques employed in the filter method. In the generator a double sideband signal is produced while the carrier is eliminated with the balanced modulator. Then the undesired sideband is removed with a high Q crystal bandpass filter. A transmit mixer is usually employed to convert the SSB signal to the desired output frequency. The detection scheme is the reciprocal. A receive mixer is used to convert the selected input frequency to the IF frequency, where the filter removes the undesired SSB response. Then the signal is demodulated in the product detector. A major drawback to the filter method is the fact that the filter is fixed-tuned to one frequency. This necessitates the receive and transmit mixers for multi-frequency operation.

Figures 5 and 6 show block diagrams of a generator and demodulator which use the phase method. Figure 6 also includes a mathematical model. The input signal (Cos(Xt)) is fed in-phase to two RF mixers where "X" is the frequency of the input signal. The other inputs to the mixers are fed from a local oscillator (LO) in quadrature (Cos(Yt) and Sin(Yt)), where "Y" is the frequency of the LO signal. By differentiating the output of one of the mixers and then summing with the other, a single sideband response is obtained. Switching the mixer output that is differentiated will change the selected sideband, upper (USB) or lower (LSB). In most cases the mixer outputs will be the audio passband (300 to 3000Hz). Differentiating the passband involves a 90 degree phase shift over more than three octaves. This is the most difficult aspect of using the phasing method for voice band SSB.

For voice systems, difficulty of maintaining accurate broadband phase shift is eliminated by the technique used in Figures 7 and 8. The "Weaver" method is similar to the phasing method because both require two quadrature steps in the signal chain. The difference between the two methods is that the Weaver method uses a low frequency (1.8kHz) subcarrier in quadrature rather than the broad-band 90 degree audio phase shift. The desired sideband is thus "folded over" the 1.8kHz subcarrier and its energy appears between 0 and 1.5kHz. The undesired sideband appears 600Hz farther away between 2.1 and 4.8kHz. Consequently, sideband rejection is determined by a low-pass filter rather than by phase and amplitude balance. A very steep low-pass response in the Weaver method is easier to achieve than the very accurate phase and amplitude balance needed in the phasing

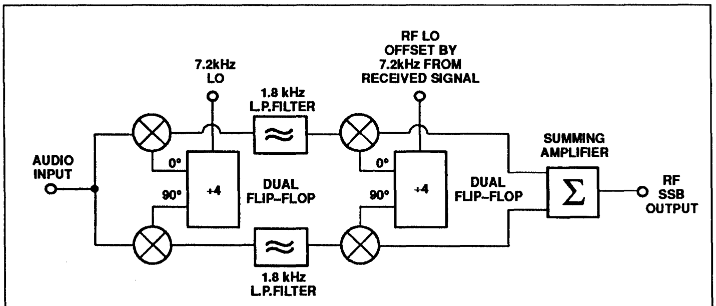


Figure 7. Weaver Method Generator

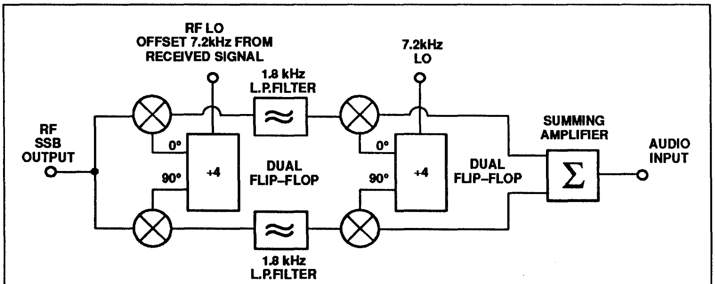


Figure 8. Weaver Method Detector

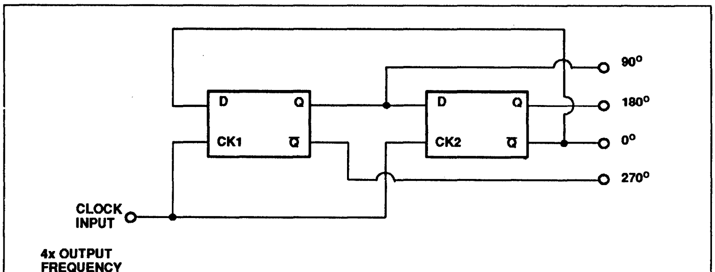


Figure 9. Dual Flip-Flop Quadrature Synthesis

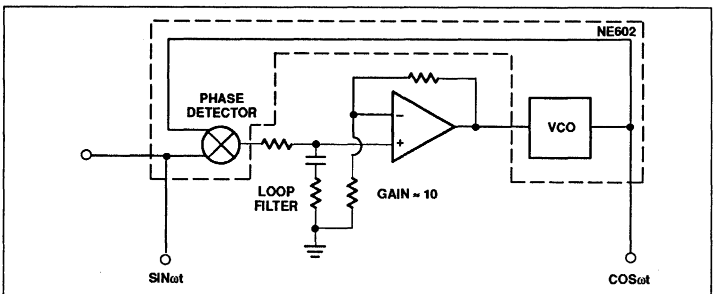


Figure 10. PLL Quadrature Synthesis

method. Therefore, better sideband rejection is possible with the Weaver method than with the phasing method.

Quadrature Dual Mixer Circuits

One of the two critical stages in the phasing method and both critical stages in the Weaver method require quadrature dual mixer circuits. Figures 9 and 10 show two methods of obtaining quadrature LO signals for dual mixer applications. Other methods exist for producing quadrature LO signals, particularly use of passive LC circuits. LC circuits will not maintain a quadrature phase relationship when the operating frequency is changed. The two illustrated circuits are inherently broad-banded; therefore, they are far more flexible and do not require adjustment. These circuits are very useful for SSB circuits, but also can be applied to FSK, PSK, and QPSK digital communications systems.

The NE602 is a low power, sensitive, active, double-balanced mixer which shows excellent phase characteristics up to 200MHz. This makes it an ideal candidate for this and many other applications.

The circuit in Figure 9 uses a divide-by-four dual flip-flop that generates all four quadratures. Most of the popular dual flip-flops can be used in different situations. The HEF4013 CMOS device uses very little power and can maintain excellent phase integrity at clock rates up to several megahertz. Consequently, the HEF4013 can be used with the ubiquitous 455kHz intermediate frequency with excellent power economy. For higher clock rates (up to 120MHz for up to 30MHz operation), the fast TTL 74F74 is a good choice. It has been tested to 30MHz operating frequencies with good results (>30 dB SSB rejection). At lower frequencies (5MHz) sideband rejection increases to nearly 40dB with the circuits shown. The ultimate low frequency rejection is mainly a function of the audio phase shifter. Better performance is possible by employing higher tolerance resistors and capacitors.

The circuit in Figure 10 shows another technique for producing a broadband quadrature phase shift for the LO. The advantage of this circuit over the flip-flops is that the clock frequency is identical to the operating frequency; however, phase accuracy is more difficult to achieve. A PLL will maintain a quadrature phase relationship when the loop is closed and the VCO voltage is zero. The DC amplifier will help the accuracy of the quadrature condition by presenting gain to the VCO control circuit. The other problem that can arise is that PLL circuits tend to be noisy. Sideband noise is troublesome in both SSB and FM systems,

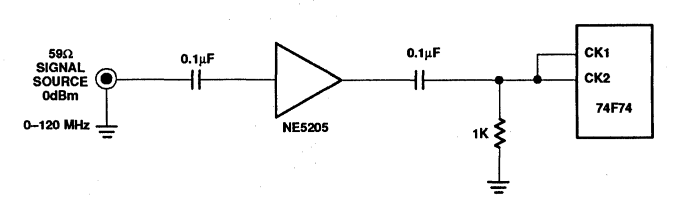


Figure 11. FAST TTL Driver from Analog Signal Source Using NE5205

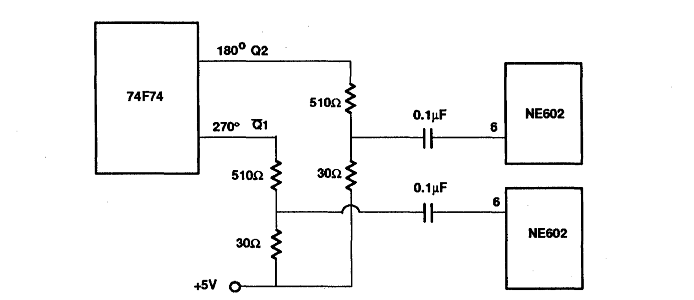


Figure 12. Interface Circuitry Between 74F74 and the NE602s

but SSB is less sensitive to phase noise problems in the LO.

Figure 11 shows a circuit that is effective for driving the 74F74, or other TTL gates, with a signal generator or analog LO. The NE5205 provides about 20dB gain with 50Ω input and output impedances from DC to 450MHz. Minimum external components are required. The 1kΩ resistor is about optimum for "pulling" the input voltage down near the logic threshold. A 50Ω output level of 0dBm can be used to drive the NE5205 and 74F74 to 100MHz. Two NE5205s can be cascaded for even more sensitivity while maintaining extremely wide bandwidth. An advantage of using digital sources for the LO is that low-frequency power supply ripple will not cause hum in the receiver front end. This is a common problem in direct conversion designs.

Figure 12 shows the interface circuitry between the 74F74 and the NE602 LO ports. The total resistance reflects conservative current drain from the 74F74 outputs, while the tap on the voltage divider is optimized for proper NE602 operation. The low signal source impedance further helps maintain phase accuracy, and the isolation capacitor is miniature ceramic for DC isolation.

Audio Amplifiers and Switching

Using active mixers (NE602) in these types of circuits gives conversion gain, typically 18dB. More traditional applications use passive diode ring mixers which yield conversion loss, typically 7dB. Consequently, the detected audio level will be about 25dB higher when using the NE602. This fact can greatly reduce the first audio stage noise and gain requirements and virtually eliminate the "microphonic" effect common to direct conversion receivers. Traditional direct conversion receivers use passive audio LC filters at the mixer output and low noise, discrete JFETs or bipolars in the first stages. The very high audio sensitivity required by these amplifiers makes them respond to mechanical vibration – thus the "microphonics" result. The conversion gain allows use of a simple op amp stage (Figure 13) set up as an integrator to eliminate ultra-sonic and RF instability. The NE5534 is well known for its low noise, high dynamic range, and excellent audio characteristics (Reference 12) and makes an ideal audio amp for the 602 detector.

The sideband select function is easily accomplished with an HEF4053 CMOS analog switch. This triple double-pole switch drives the phase network discussed in the next section and also chooses one of two amplitude balance potentiometers, one for each sideband. Figure 14 illustrates this circuit. A buffer op amp is used with the two sideband select sections to reduce THD, maintain amplitude integrity, and not change the filter network input resistance values. The gain distribution within both legs of the receiver was found to be very consistent (within 1dB), thus the amplitude balance pots may be eliminated in less demanding applications. The NE602s have excellent gain as well as phase integrity.

Audio Phase Shift Circuits

The two critical stages for the phasing method are a dual quadrature mixer and a broadband audio phase shifter (differentiator). There are several broadband, phase shift techniques available. Figure 15 shows an analog all-pass differential phase shift circuit. When the inputs are shorted and driven with a microphone circuit, the outputs will be 90 degrees out-of-phase over the 300 to 3000Hz band. This "splitting" and phase shift is necessary for the phasing generator. For phasing demodulation the two audio detectors are fed to the two inputs. The outputs are then summed to affect the sideband rejection and audio output.

Standard 1% values are shown for the resistors and capacitors, although better gain tolerances can be obtained with 0.1% laser-trimmed integrated resistors. Polystyrene capacitors are preferred for better value tolerance and audio performance. Two quad op amps fit nicely into this application. One op amp serves as a switch buffer and the other three form a phasing section. The NE5514 quad op amps perform well for this application. Careful attention to active filter configurations can yield highly linear and very high dynamic range circuits. Yet these characteristics are much easier to achieve at audio than the common IF RF frequencies. This fact, coupled with the lack of IF tuned circuits, shielding, and higher power requirements make audio IF systems attractive indeed.

Figure 16 shows a "tapped" analog delay circuit which uses weighted values of resistors to affect the phase shift. Excellent phase and amplitude balance are possible with this technique, but the price for components is high. It should be stressed that the audio phase shift accuracy and amplitude balance are the limiting factors for SSB rejection when using the phase method; thus the higher cost may be justified in some applications.

Audio Processing

The summing amplifier is a conventional, inverting op amp circuit. It may be useful to configure a low-pass filter around this amplifier, and thus help the sharp audio filters which follow. Audio filters are necessary to shape the desired bandpass. Steep slope audio bandpass filters can be built from switched capacitor filters or from active filters

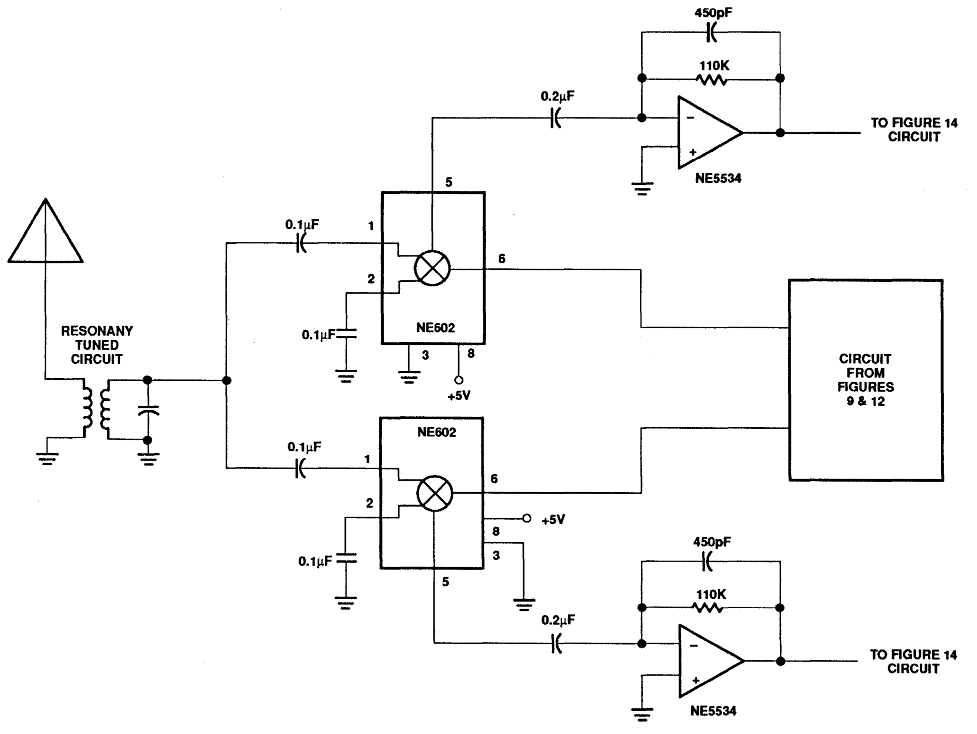


Figure 13. Phasing Method Detector for Direct Conversion Receiver

requiring more op amps. Switched capacitor filters have the disadvantage of requiring a clock frequency in the RF range. Harmonics can cause interference problems if careful design techniques are not used. Also, better dynamic range is obtained with active filter techniques using "real" resistors although much work is being done with SCF's and performance is improving.

Direct conversion receivers rely heavily on audio filters for selectivity. Active analog or switched capacitor filters can produce the high Q and dynamic ranges necessary. Signal strength or "S-meters" can be constructed from the NE602's companion part, the NE604. The "RSSI" or "received signal strength indicator" function on the 604 provides a logarithmic response over a 90dB dynamic range and is easy to use at audio frequencies. Finally, the AGC (automatic gain control) function can also be performed in the audio section. Attack and delay times can be independently set with excellent distortion specifications with the NE572 compandor IC. The audio-derived AGC eliminates the need for gain controlling and RF stage, but relies on an excellent receiver front-end dynamic range. In ACSSB (Amplitude Compandored Single-Side Band) systems transmitter compression and receiver expansion are defined by individual system specifications.

Phasing-Filter Technique

High quality SSB radio specifications call for greater than 70dB sideband rejection. Using the circuits described in this paper for the phasing method, rejection levels of 35dB are obtainable with good reliability. Coupled with an inexpensive two-pole crystal or ceramic filter, the 70dB requirement is obtained. Also, the filtering ahead of the NE602 greatly improves the intermodulation performance of the receiver. Figure 17 shows a complete SSB receiver using the Phasing-Filter technique. The sensitivity of the NE602 allows low gain stages and low power consumption for the RF amplifier and first mixer. A new generation of low power CMOS frequency synthesizers is now available from several manufacturers including the TDD1742 and dual chip HEF4750/51 solutions.

Direct Conversion Receiver

The antenna can be connected directly to the input of the NE602 (via a bandpass filter) to form a direct conversion SSB receiver using the phasing method. 35dB sideband rejection is adequate for many applications, particularly where low power and portable battery operation are required. Figure 13 shows a typical circuit for direct conversion applications.

There are many other applications which can make use of SSB technology. Cordless telephones use FM almost exclusively. Eavesdropping could be greatly reduced for systems which employ SSB rather than FM. Furthermore, the better signal-to-noise ratio will extend the range, and battery life will be extended because no carrier is needed.

SSB is also used for subcarriers on microwave links and coaxial lines. Telephone communications networks that use SSB are called FDM or Frequency Domain Multiplex systems. The low power and high sensitivity of the NE602 can offer FDM designers new techniques for system configuration.

Weaver Method Receiver Techniques

The same quadrature dual mixer can be used for the first stage in both the phasing and Weaver method receiver. The subcarrier stage in the Weaver method receiver can use CMOS analog switches (HEF4066) for great power economy. Figure 18 shows a circuit for the subcarrier stage. A 1.8kHz subcarrier requires a 7.2kHz clock frequency. If switched capacitor filters are used for the low-pass and audio filters, a single clock generator can be used for all circuits with appropriate dividers. Furthermore, if the receiver is used as an IF circuit, the fixed LO signal could also be derived from the same clock. This has the added advantage that harmonics from the various circuits will not interfere with the received signal.

Results

The circuit shown in Figures 13, 14, and 15 has a 10dB S/N sensitivity of 0.5µV with a dynamic range of about 80dB. Single-tone audio harmonic distortion is below 0.05% with two-tone intermodulation products below 55dB at RF input levels only 5dB below the 1dB compression point. The sideband rejection is about 38dB at a 9MHz operating frequency. The good audio specifications are a side benefit to direct conversion receivers. When used with inexpensive ceramic or crystal filters, this circuit can provide these specifications with >70dB sideband rejection.

Conclusions

Single sideband offers many advantages over FM and full-carrier double-sideband modulation. These advantages include: more efficient spectrum use, better signal-to-noise ratios at low signal levels, and better transmitter efficiency. Many of the disadvantages can now be overcome by using old techniques and new state-of-the-art integrated circuits. Effective and inexpensive circuits can use direct conversion techniques with good results. 35dB sideband rejection with less than 1µV sensitivity is obtained with the NE602 circuits. 70dB sideband rejection and superior sensitivity are obtained by using phasing-filter techniques. Either the phasing or Weaver methods can be used in either the direct conversion or IF section applications. The filter and phase-filter methods can be used in only the IF application.

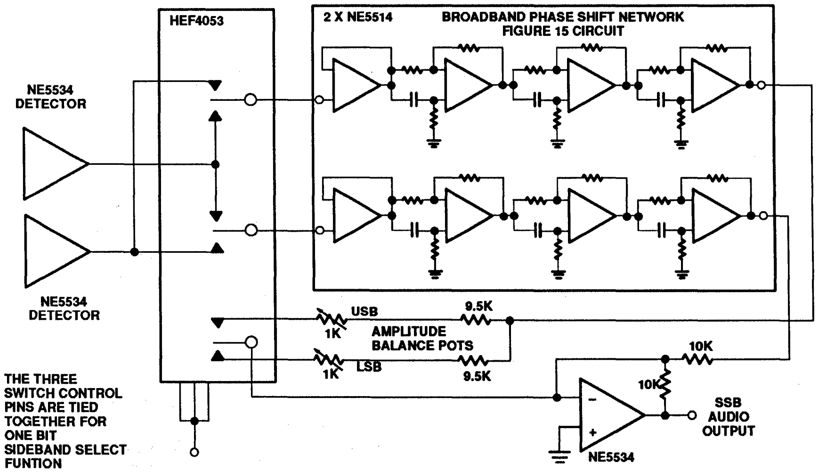


Figure 14. Sideband Select Switching Function

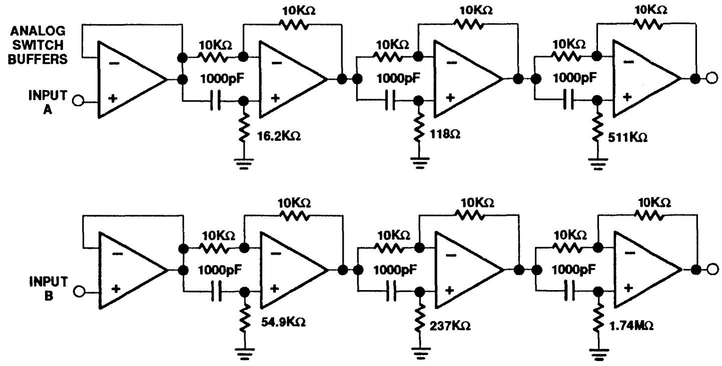


Figure 15

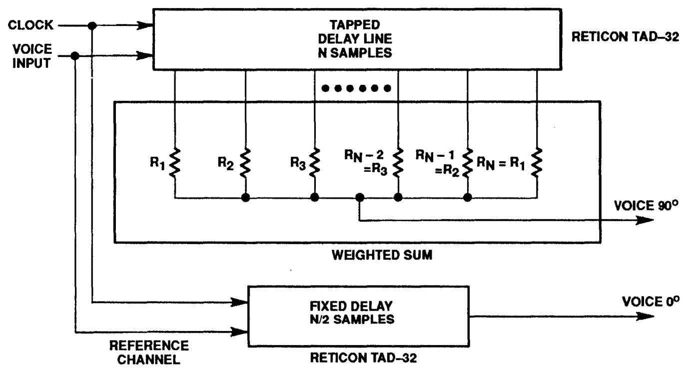
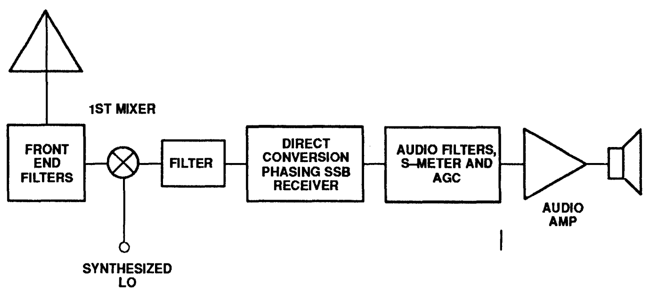


Figure 16. Broadband 90° Audio Phase Shift Technique Using Tapped Delay Line (Reference 4)



Receivers built using this technique can exhibit excellent characteristics without resorting to expensive multi-pole filters or an IF amplifier chain.

Figure 17. Complete Phasing-Filter Receiver

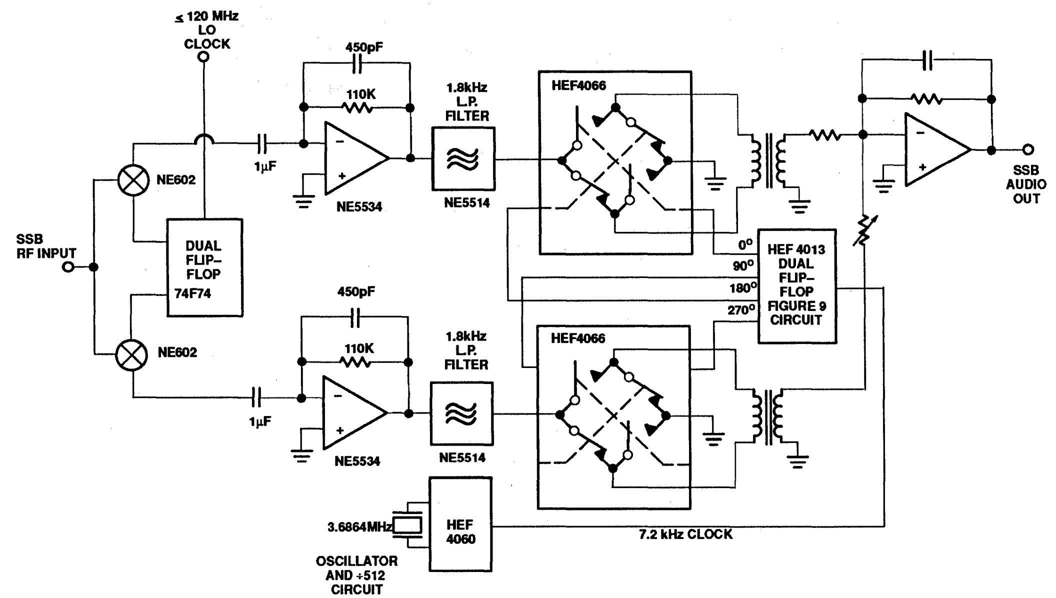


Figure 18. Weaver Method Receiver Concept Example for ≤ 30MHz Operation

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Applying the oscillator of the NE602 in low-power mixer applications

AN1982

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INTRODUCTION

For the designer of low power RF systems, the Signetics NE602 mixer/oscillator provides mixer operation beyond 500MHz, a versatile oscillator capable of operation to 200MHz, and conversion gain, with only 2.5mA total current consumption. With a proper understanding of the oscillator design considerations, the NE602 can be put to work quickly in many applications.

DESCRIPTION

Figure 1 shows the equivalent circuit of the device. The chip is actually three subsystems: A Gilbert cell mixer (which provides differential input gain), a buffered emitter follower oscillator, and RF current and voltage regulation. Complete integration of the DC bias permits simple and compact application. The simplicity of the oscillator permits many configurations.

While the oscillator is simple, oscillator design isn't. This article will not address the rigors of oscillator design, but some practical guidelines will permit the designer to accomplish good performance with minimum difficulty.

Either crystal or LC tank circuitry can be employed effectively. Figure 2 shows the four most commonly used configurations in their most basic form.

In each case the Q of the tank will affect the upper frequency limits of oscillation: the higher the Q the higher the frequency. The NE602 is fabricated with a 6GHz process, but the emitter resistor from Pin 7 to ground is nominally 20k. With 0.25mA typical bias current, 200MHz oscillation can be achieved with high Q and appropriate feedback.

The feedback, of course, depends on the Q of the tank. It is generally accepted that a minimum amount of feedback should be used, so even if the choice is entirely empirical, a good trade-off between starting characteristics, distortion, and frequency stability can be quickly determined.

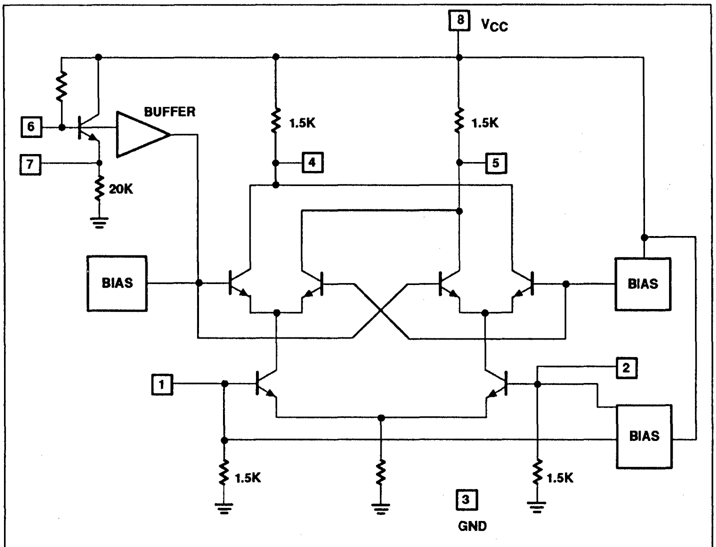


Figure 1

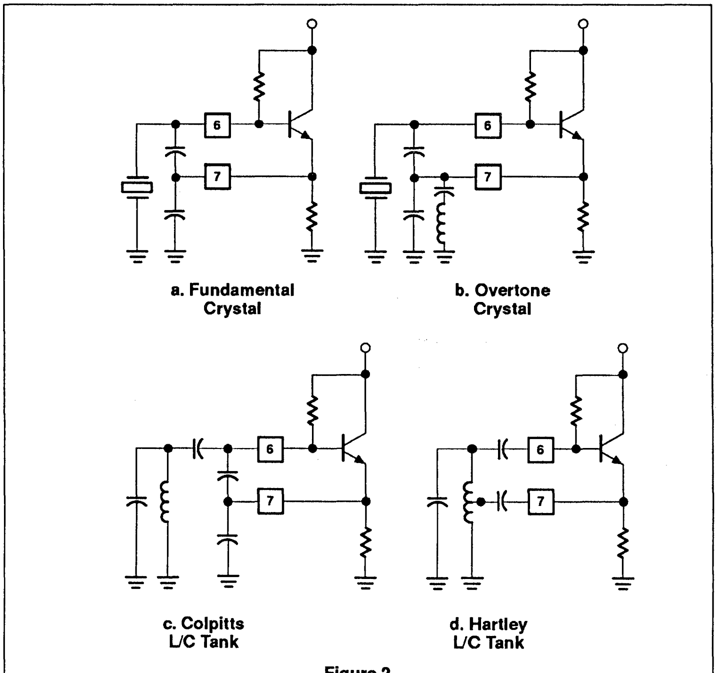


Figure 2

Applying the oscillator of the NE602 in low-power mixer applications

Crystal Circuit Considerations

Crystal oscillators are relatively easy to implement since crystals exhibit higher Q's than LC tanks. Figure 3 shows a complete implementation of the SA602 (extended temperature version) for cellular radio with a 45MHz first IF and 455kHz second IF.

The crystal is a third overtone parallel mode with 5pF of shunt capacitance and a trap to suppress the fundamental.

LC Tank Circuits

LC tanks present a little greater challenge for the designer. If the Q is too low, the oscillator won't start. A trick which will help if all else fails is to shunt Pin 7 to ground with a 22k resistor. In actual applications this has been effective to 200MHz with high Q ceramic capacitors and a tank inductor of 0.08mH and a Q of 90. Smaller resistor value will upset DC bias because of inadequate base bias at the input of the oscillator. An external bias resistor could be added from VCC to Pin 6, but this will introduce power supply noise to the frequency spectrum.

The Hartley configuration (Figure 2D) offers simplicity. With a variable capacitor tuning the tank, the Hartley will tune a very large range since all of the capacitance is variable. Please note that the inductor must be coupled to Pin 7 with a low impedance capacitor. The Colpitts oscillator will exhibit a smaller tuning range since the fixed feedback capacitors limit variable capacitance range; however, the Colpitts has good frequency stability with proper components.

Synthesized Frequency Control

The NE602 can be very effective with a synthesizer if proper precautions are taken to minimize loading of the tank and the introduction of digital switching transients into the spectrum. Figure 4 shows a circuit suitable for aircraft navigation frequencies (108–118MHz) with 10.7MHz IF.

The dual gate MOSFET provides a high degree of isolation from prescaler switching spikes. As shown in Figure 4, the total current consumption of the NE602 and 3SK126 is typically 3mA. The MOSFET input is from the emitter of the oscillator transistor to avoid loading the tank. The Gate 1 capacitance of the MOSFET in series with the 2pF coupling capacitor adds slightly to the feedback capacitance ratio. Use of the 22k resistor at Pin 7 helps assure oscillation without upsetting DC bias.

For applications where optimum buffering of the tank, or minimum current are not mandatory, or where circuit complexity must be minimized, the buffers shown in Figure 5 can be considered.

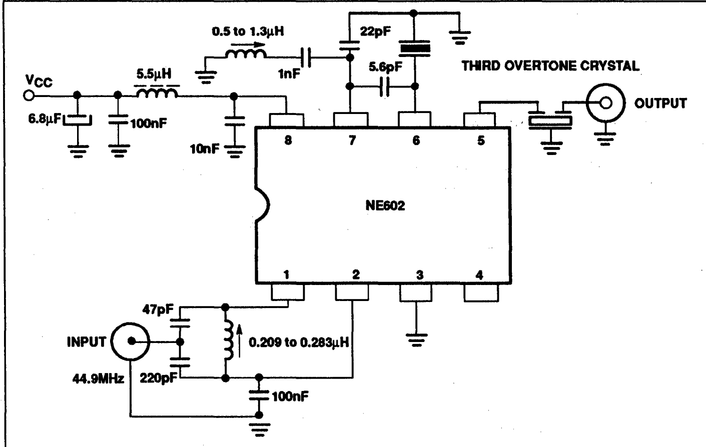


Figure 3. Cellular Radio Application

The effectiveness of the MRF931 (or other VHF bipolar transistors) will depend on frequency and required input level to the prescaler. A bipolar transistor will generally provide the least isolation. At low frequencies the transistor can be used as an emitter follower, but by VHF the base emitter junction will start to become a bidirectional capacitor and the buffer is lost.

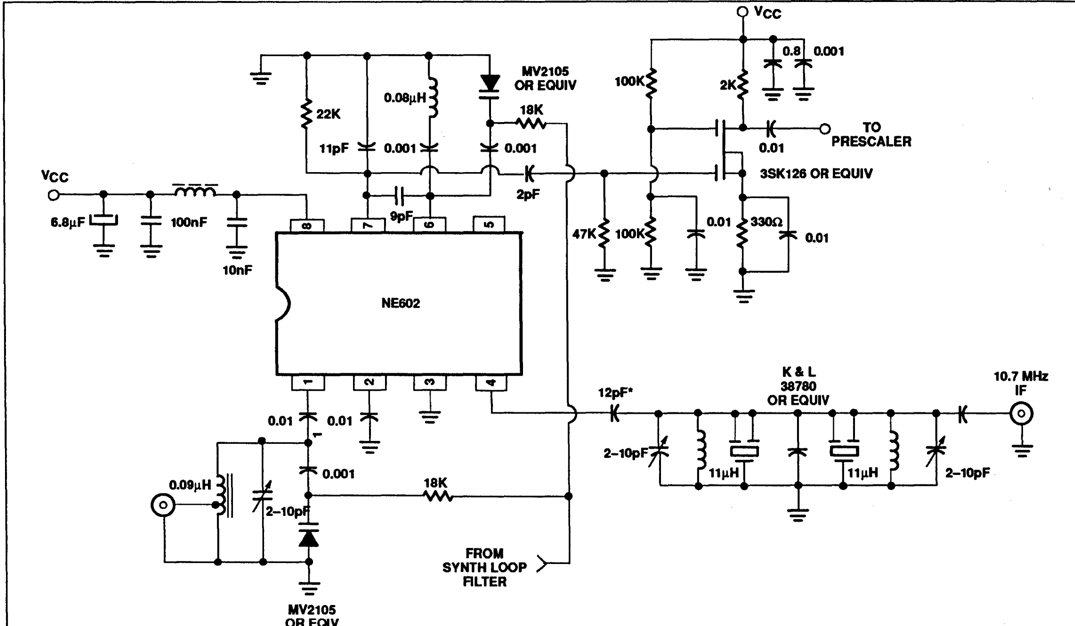
The 2N5484 has an IDSS of 5mA max. and the 2SK126 has IDSS of 6mA max. making them suitable for low parts count, modest current buffers. The isolation is good.

Injected LO

If the application calls for a separate local oscillator, it is acceptable to capacitively-couple 200 to 300mV at Pin 6.

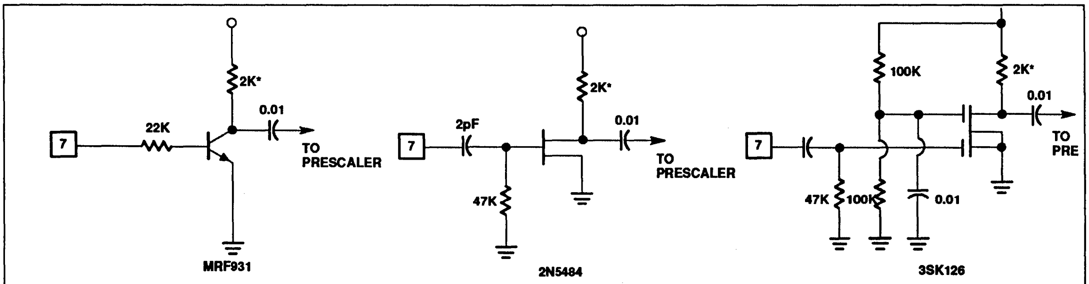
Summary

The NE602 can be an effective low power mixer at frequencies to 500MHz with oscillator operation to 200MHz. All DC bias is provided internal to the device so very compact designs are possible. The internal bias sets the oscillator DC current at a relatively low level so the designer must choose frequency selective components which will not load the transistor. If the guidelines mentioned are followed, excellent results will be achieved.



NOTES:
* Permits impedance match of NE602 output, i.e.: 1.5k filter impedance.
** Choose for impedance match to next stage.

Figure 4



NOTES:
* 2k or as necessary for current limits or prescaler impedance match.

Figure 5

GENERAL DESCRIPTION

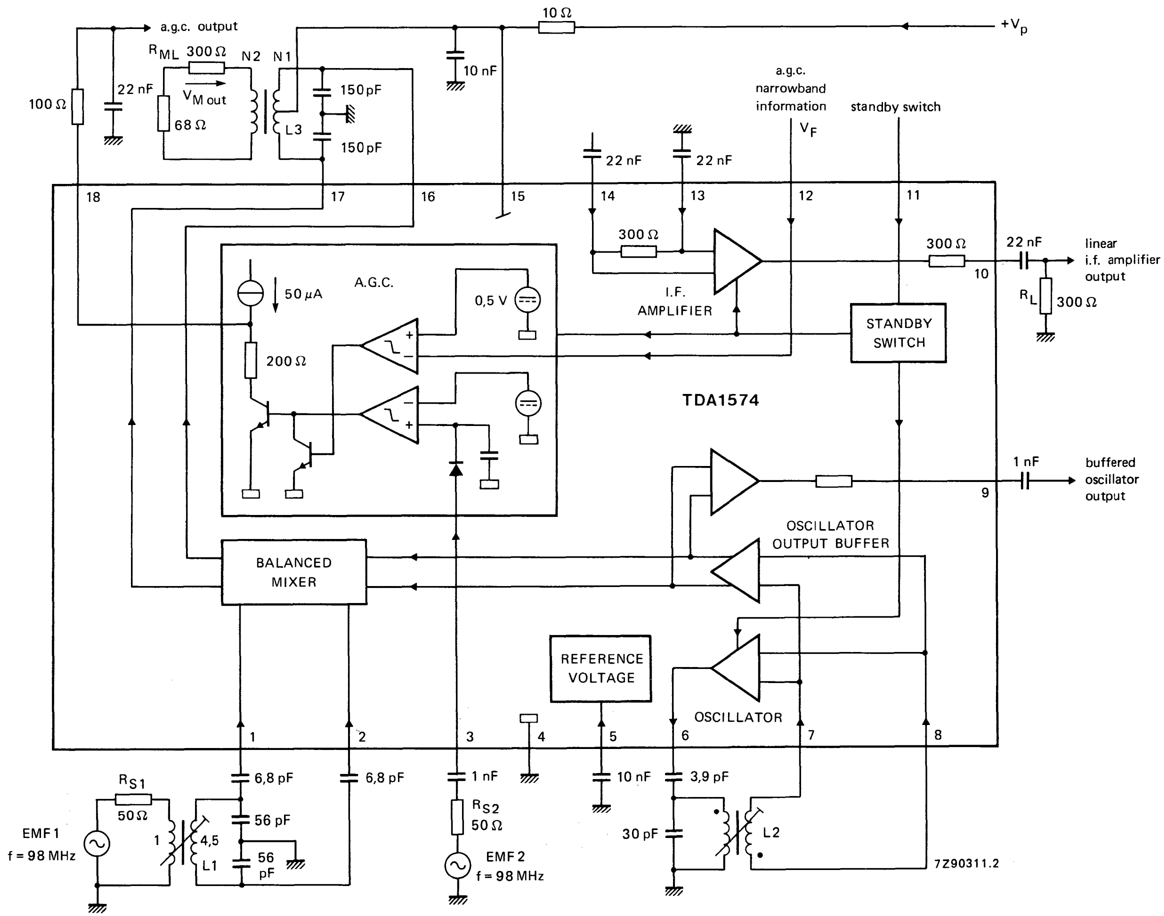
The TDA1574 is a monolithic integrated FM tuner circuit designed for use in the r.f./i.f. section of car radios and home-receivers. The circuit comprises a mixer, oscillator and a linear i.f. amplifier for signal processing, plus the following additional features.

Features

- Keyed automatic gain control (a.g.c.)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

Supply voltage range (pin 15)	V_P		7 to 16	V
Mixer input bias voltage (pins 1 and 2)	$V_{1,2\text{-}4}$	typ.	1	V
noise figure	NF	typ.	9	dB
Oscillator output voltage (pin 6)	$V_{6\text{-}4}$	typ.	2	V
output admittance at pin 6 for f = 108,7 MHz	Y22	typ.	1,5 + j2	mS
Oscillator output buffer				
D.C. output voltage (pin 9)	$V_{9\text{-}4}$	typ.	6	V
Total harmonic distortion	THD	typ.	−15	dBC
Linear i.f. amplifier output voltage (pin 10)	$V_{10\text{-}4}$	typ.	4,5	V
noise figure at R_S = 300 Ω	NF	typ.	6,5	dB
Keyed a.g.c. output voltage range (pin 18)	$V_{18\text{-}4}$		+ 0,5 to V_P−0,3	V



Coil data

L1: TOKO MC-108, 514HNE-150014S14; L = 0,078 μH
L2: TOKO MC-111, E516HNS-200057; L = 0,08 μH
L3: TOKO coil set 7P, N1 = 5,5 + 5,5 turns, N2 = 4 turns

Fig. 1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit is a double balanced multiplier with a preamplifier (common base input) to obtain a large signal handling range and a low oscillator radiation.

Oscillator

The oscillator circuit is an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tanh-transfer-function to obtain low order 2nd harmonics.

Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow- and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent, current sinking output has an active load, which sets the AGC threshold.
The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC), or by a wideband information only, or by narrowband information only. If only narrow-band AGC is wanted pin 3 should be connected to pin 5. If only wideband AGC is wanted pin 12 should be connected to pin 13.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15\text{-}4}$	max.	18	V
Mixer output voltage (pins 16 and 17)	$V_{16,\,17\text{-}4}$	max.	35	V
Standby switch input voltage (pin 11)	$V_{11\text{-}4}$	max.	23	V
Reference voltage (pin 5)	$V_{5\text{-}4}$	max.	7	V
Field strength input voltage (pin 12)	$V_{12\text{-}4}$	max.	7	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−40 to	+ 85	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}amb}$	=	80	K/W

Note

All pins are short-circuit protected to ground.

CHARACTERISTICS

$V_P = V_{15\text{-}4} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15\text{-}4}$	7	–	16	V
Supply current (except mixer)	$I_P = I_{15}$	16	23	30	mA
Reference voltage (pin 5)	$V_{5\text{-}4}$	3,9	4,1	4,4	V
Mixer					
D.C. characteristics					
Input bias voltage (pins 1 and 2)	$V_{1,2\text{-}4}$	–	1	–	V
Output voltage (pins 16 and 17)	$V_{16,17\text{-}4}$	4	–	35	V
Output current (pin 16 + pin 17)	$I_{16} + I_{17}$	–	4,0	–	mA
A.C. characteristics (f_i = 98 MHz)					
Noise figure	NF	–	9	–	dB
Noise figure including transforming network	NF	–	11	–	dB
3rd order intercept point	$EMF1_{IP3}$	–	115	–	dBμV
Conversion power gain $10 \log \frac{4\ (V_{M(out)}\ 10{,}7\ MHz)^2}{(EMF1\ 98\ MHz)^2} \times \frac{R_{S1}}{R_{ML}}$	G_P	–	14	–	dB
Input resistance (pins 1 and 2)	$R_{1,2\text{-}4}$	–	14	–	Ω
Output capacitance (pins 16 and 17)	$C_{16,17}$	–	13	–	pF
Oscillator					
D.C. characteristics					
Input voltage (pins 7 and 8)	$V_{7,8\text{-}4}$	–	1,3	–	V
Output voltage (pin 6)	$V_{6\text{-}4}$	–	2	–	V
A.C. characteristics (f_{osc} = 108,7 MHz)					
Residual FM (Bandwidth 300 Hz to 15 kHz); de-emphasis = 50 μs	Δf	–	2,2	–	Hz

parameter	symbol	min.	typ.	max.	unit
Linear i.f. amplifier					
D.C. characteristics					
Input bias voltage (pin 13)	$V_{13\text{-}4}$	–	1,2	–	V
Output voltage (pin 10)	$V_{10\text{-}4}$	–	4,5	–	V
A.C. characteristics (f_i = 10,7 MHz)					
Input impedance					
	$R_{14\text{-}13}$	240	300	360	Ω
	$C_{14\text{-}13}$	–	13	–	pF
Output impedance					
	$R_{10\text{-}4}$	240	300	360	Ω
	$C_{10\text{-}4}$	–	3	–	pF
Voltage gain					
$20 \log \frac{V_{10\text{-}4}}{V_{14\text{-}13}}$	G_{VIF}	27	30	–	dB
T_{amb} = –40 to + 85 °C	ΔG_{VIF}	–	0	–	dB
1 dB compression point (r.m.s. value)					
at V_P = 8,5 V	$V_{10\text{-}4rms}$	–	750	–	mV
at V_P = 7,5 V	$V_{10\text{-}4rms}$	–	550	–	mV
Noise figure					
at R_S = 300 Ω	NF	–	6,5	–	dB
Keyed a.g.c.					
D.C. characteristics					
Output voltage range (pin 18)	$V_{18\text{-}4}$	0,5	–	V_P–0,3	V
A.G.C. output current					
at I_3 = ϕ or $V_{12\text{-}4}$ = 450 mV; $V_{18\text{-}4}$ = $V_P/2$	$-I_{18}$	25	50	100	μA
at $V_{3\text{-}4}$ = 2 V and $V_{12\text{-}4}$ = 1 V; $V_{18\text{-}4}$ = $V_{15\text{-}4}$	I_{18}	2	–	5	mA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Narrowband threshold					
at $V_{3\text{-}4}$ = 2 V; $V_{12\text{-}4}$ = 550 mV	$V_{18\text{-}4}$	–	–	1	V
at $V_{3\text{-}4}$ = 2 V; $V_{12\text{-}4}$ = 450 mV	$V_{18\text{-}4}$	V_P–0,3	–	–	V
A.C. characteristics (f_i = 98 MHz)					
Input impedance					
	$R_{3\text{-}4}$	–	4	–	kΩ
	$C_{3\text{-}4}$	–	3	–	pF
Wideband threshold (r.m.s. value) (see figures 2, 3, 4 and 5)					
at $V_{12\text{-}4}$ = 0,7 V; $V_{18\text{-}4}$ = $V_P/2$; I_{18} = 0	$EMF2_{rms}$	–	17	–	mV
Oscillator output buffer (pin 9)					
D.C. output voltage	$V_{9\text{-}4}$	–	6,0	–	V
Oscillator output voltage (r.m.s. value)					
at $R_L = \infty$; C_L = 2 pF	$V_{9\text{-}4(rms)}$	–	110	–	mV
at R_L = 75 Ω	$V_{9\text{-}4(rms)}$	30	50	–	mV
D.C. output impedance	$R_{9\text{-}15}$	–	2,5	–	kΩ
Signal purity					
Total harmonic distortion	THD	–	–15	–	dBC
Spurious frequencies					
at EMF1 = 0,2 V; R_{S1} = 50 Ω	f_S	–	–35	–	dBC
Electronic standby switch (pin 11)					
Oscillator; linear i.f. amplifier; a.g.c.					
at T_{amb} = –40 to + 85 °C					
Input switching voltage					
for threshold ON; $V_{18\text{-}4} = \geqslant V_P - 3$ V	$V_{11\text{-}4}$	0	–	2,3	V
for threshold OFF; $V_{18\text{-}4} = \leqslant 0,5$ V	$V_{11\text{-}4}$	3,3	–	23	V
Input current					
at ON condition; $V_{11\text{-}4}$ = 0 V	$-I_{11}$	–	–	150	μA
at OFF condition; $V_{11\text{-}4}$ = 23 V	I_{11}	–	–	10	μA
Input voltage					
at $I_{11} = \phi$	$V_{11\text{-}4}$	–	–	4,4	V

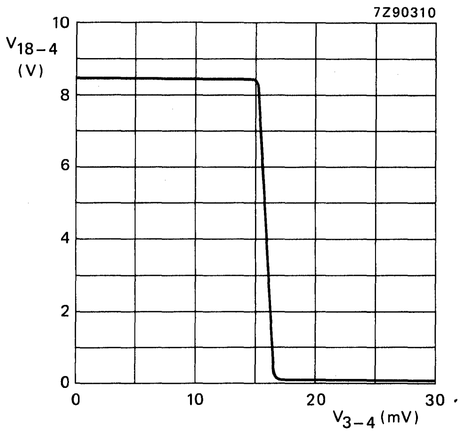


Fig. 2 Keyed a.g.c. output voltage $V_{18\text{-}4}$ as a function of r.m.s. input voltage $V_{3\text{-}4}$. Measured in test circuit Fig. 1 at $V_{12\text{-}4} = 0{,}7$ V; $I_{18} = \phi$.

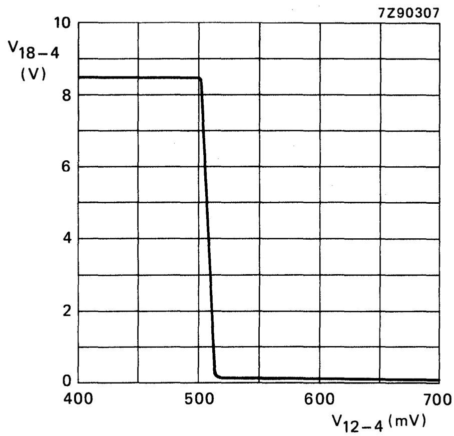


Fig. 3 Keyed a.g.c. output voltage $V_{18\text{-}4}$ as a function of input voltage $V_{12\text{-}4}$. Measured in test circuit Fig. 1 at $V_{3\text{-}4} = 2$ V; $I_{18} = \phi$.

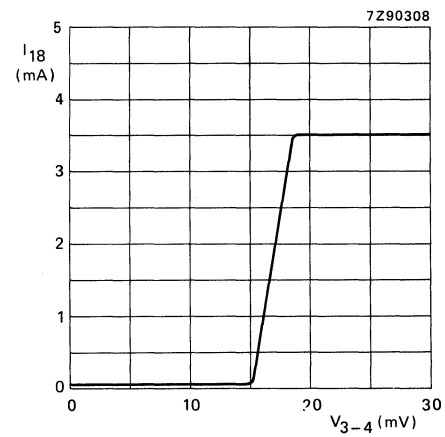


Fig. 4 Keyed a.g.c. output current I_{18} as a function of r.m.s. input voltage $V_{3\text{-}4}$. Measured in test circuit Fig. 1 at $V_{12\text{-}4} = 0{,}7$ V; $V_{18\text{-}4} = 8{,}5$ V.

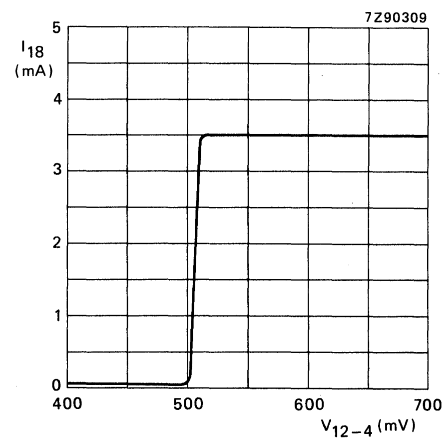
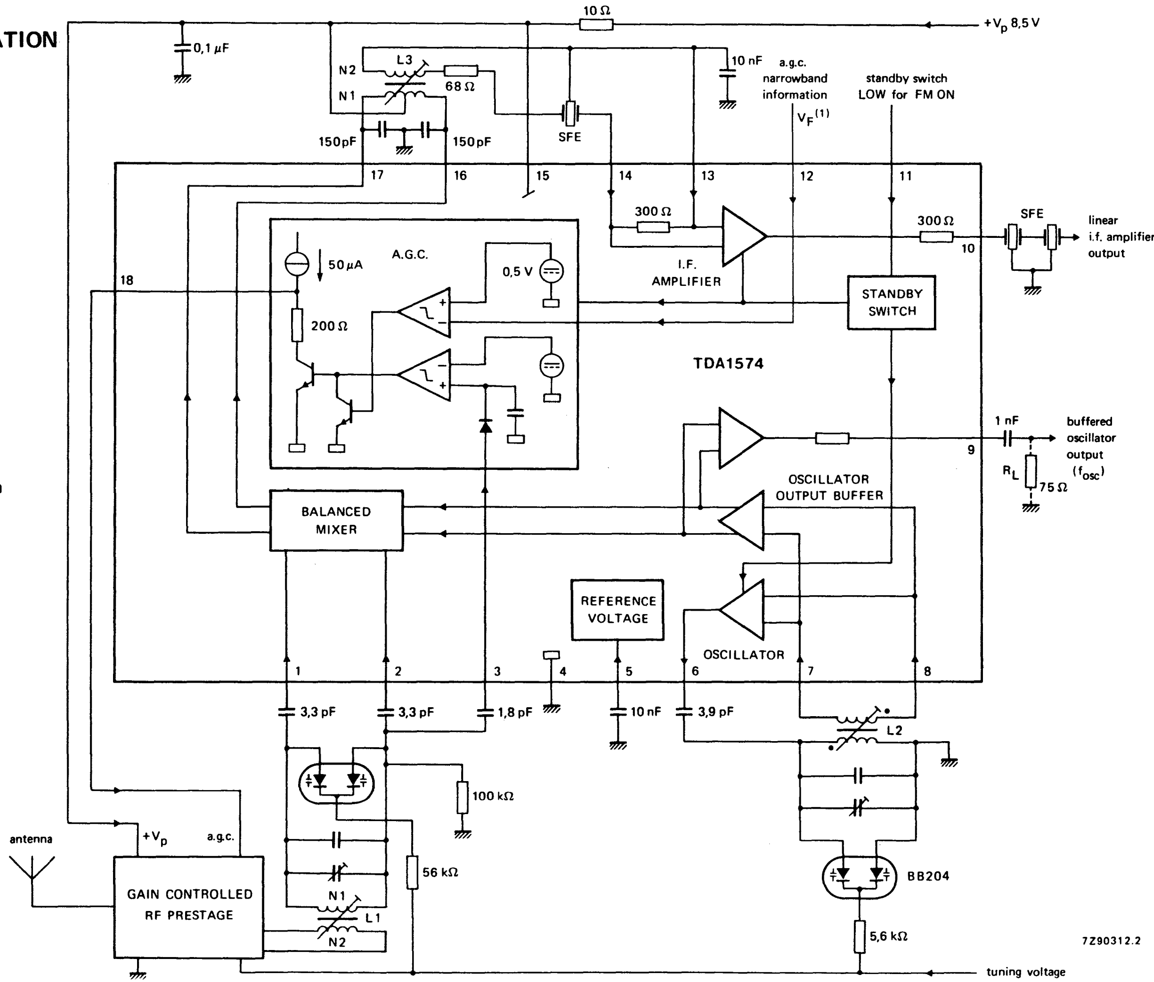


Fig. 5 Keyed a.g.c. output current I_{18} as a function of input voltage $V_{12\text{-}4}$. Measured in test circuit Fig. 1 at $V_{3\text{-}4} = 2$ V; $V_{18\text{-}4} = 8{,}5$ V.

APPLICATION INFORMATION



Coil data

L1: TOKO MC-108,
514HNE-15023S15,
N1 = 5,5 turns, N2 = 1 turn

L2:
L3: see Fig. 1

(1) Field strength indication of main i.f. amplifier.

Integrated FM tuner for radio receivers — TDA1574T

GENERAL DESCRIPTION

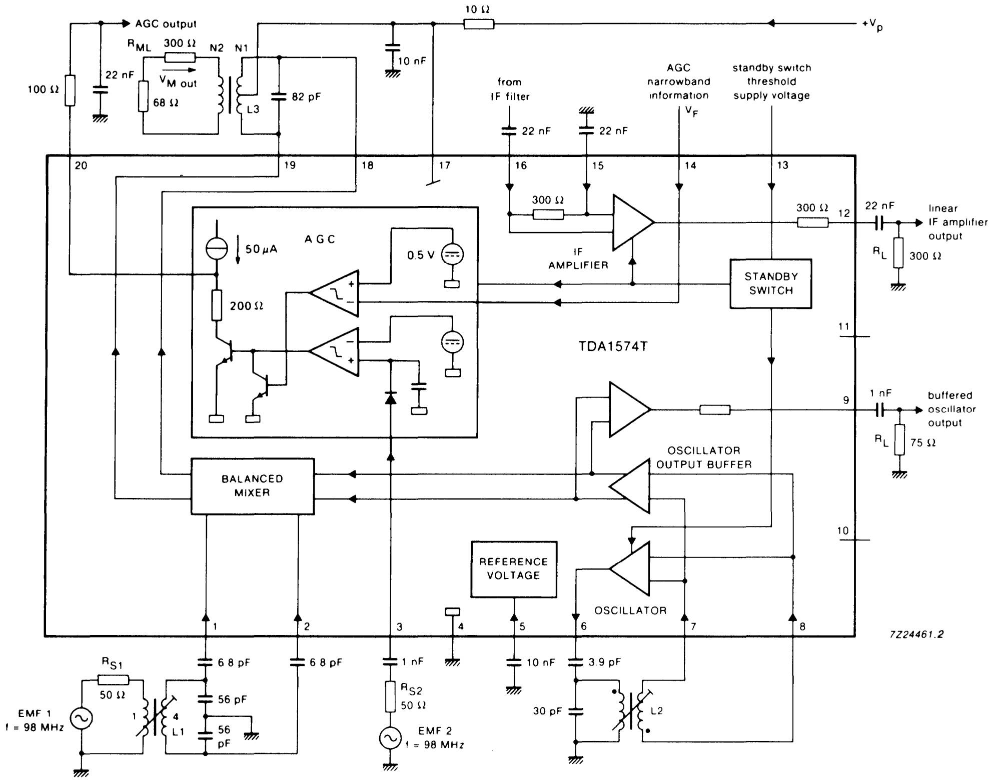
The TDA1574T is an integrated FM tuner circuit designed for use in the RF/IF section of car radios and home-receivers. The circuit contains a mixer and an oscillator and a linear IF amplifier for signal processing. The circuit also incorporates the following features.

Features

- Keyed Automatic Gain Control (AGC)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 17)		V_P	7	–	14	V
Mixer input bias voltage (pins 1 and 2)		$V_{1,2\text{-}4}$	–	1	–	V
Noise factor		NF	–	9	–	dB
Oscillator output voltage (pin 6)		$V_{6\text{-}4}$	–	2	–	V
Output admittance at pin 6	f = 108.7 MHz	Y22	–	1.5 + j2		ms
Oscillator output buffer DC output voltage (pin 9)		$V_{9\text{-}4}$	–	6	–	V
Total harmonic distortion		THD	–	−15	–	dB
Linear IF amplifier output voltage (pin 12)		$V_{12\text{-}4}$	–	4.5	–	V
Noise factor	R_S = 300 Ω	NF	–	6.5	–	dB
Keyed AGC output voltage range (pin 20)		$V_{20\text{-}4}$	0.5	–	V_P−0.3	V



Coil data

L1: TOKO MC-108, 514HNE-150023S14; L = 0.078 μH
L2: TOKO MC-111, E516HNS-200057; L = 0.08 μH
L3: TOKO Coil set 7P, N1 = 5.5 + 5.5 turns, N2 = 4 turns

Fig.1 Block diagram and test circuit.

Integrated FM tuner for radio receivers TDA1574T

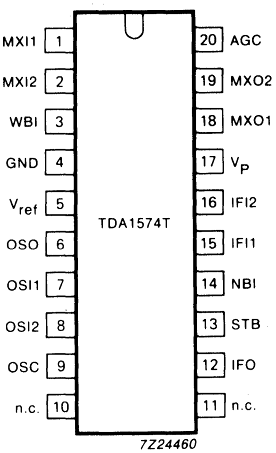


Fig.2 Pinning diagram.

PINNING

1. Mixer input 1
2. Mixer input 2
3. Wideband information input
4. Ground
5. Voltage reference
6. Oscillator output
7. Oscillator input 1
8. Oscillator input 2
9. Buffered oscillator output
10. Not connected
11. Not connected
12. IF output
13. Standby switch
14. Narrowband information input
15. IF input 1
16. IF input 2
17. Supply voltage
18. Mixer output 1
19. Mixer output 2
20. AGC output

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit uses a double balanced multiplier with a preamplifier (common base input) in order to obtain a large signal handling range and low oscillator radiation.

Oscillator

The oscillator circuit uses an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tan h-transfer-function to obtain low order 2nd harmonics.

Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent current sinking output has an active load which sets the AGC threshold.
The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC) or by a wideband/narrowband information only. If narrowband AGC is required pin 3 should be connected to pin 5. If wideband AGC is required pin 14 should be connected to pin 15.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 17)		$V_{17\text{-}4}$	–	14	V
Mixer output voltage (pins 18 and 19)		$V_{18,19\text{-}4}$	–	35	V
Standby switch input voltage (pin 13)		$V_{13\text{-}4}$	–	23	V
Reference voltage (pin 5)		$V_{5\text{-}4}$	–	7	V
Total power dissipation		P_{tot}	–	500	mW
Storage temperature range		T_{stg}	–55	+ 150	°C
Operating ambient temperature range		T_{amb}	–40	+ 85	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a}$ = 95 K/W

CHARACTERISTICS

$V_P = V_{17\text{-}4} = 8.5$ V; $T_{amb} = 25$ °C; measured in test circuit Fig.1;
All measurements are with respect to ground (pin 4); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 17)						
Supply voltage	$V_P = V_{17}$	V_{17}	7	–	14	V
Supply current (except mixer)	$I_P = I_{17}$	I_{17}	16	23	30	mA
Reference voltage (pin 5)		V_5	4.0	4.2	4.4	V
Mixer						
DC characteristics						
Input bias voltage (pins 1 and 2)		$V_{1,2}$	–	1	–	V
Output voltage (pins 18 and 19)		$V_{18,19}$	4	–	35	V
Output current (pins 18 and 19)		I_{18+19}	–	4.5	–	mA
AC characteristics	$f_i = 98$ MHz					
Noise figure		NF	–	9	–	dB
Noise figure including transforming network		NF	–	11	–	dB
3rd order intercept point		$EMF1_{IP3}$	–	115	–	dB/μV
Conversion power gain	note 1	G_{CP}	–	14	–	dB
Input resistance (pins 1 and 2)		$R_{1,2}$	–	14	–	Ω
Output capacitance (pins 18 and 19)		$C_{18,19}$	–	13	–	pF
Oscillator						
DC characteristics						
Input voltage (pins 7 and 8)		$V_{7,8}$	–	1.3	–	V
Output voltage (pin 6)		V_6	–	2	–	V
AC characteristics						
Residual FM (bandwidth = 300 Hz to 15 kHz)	de-emphasis = 50 μs	Δf	–	2.2	–	Hz
Linear IF amplifier						
DC characteristics						
Input bias voltage (pin 15)		V_{15}	–	1.2	–	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage (pin 12)		V_{12}	–	4.5	–	V
AC characteristics	f_i = 10.7 MHz					
Input impedance		$R_{16\text{-}15}$	240	300	360	Ω
		$C_{16\text{-}15}$	–	13	–	pF
Output impedance		R_{12}	240	300	360	Ω
		C_{12}	–	3	–	pF
Voltage gain	note 2	G_v	27	30	–	dB
Voltage gain with variation of temperature	T_{amb} = –40 to + 85 °C	ΔG_T	–	0	–	dB
1 dB compression point (RMS value)						
at V_P = 8.5 V		$V_{12(rms)}$	–	750	–	mV
at V_P = 7.5 V		$V_{12(rms)}$	–	550	–	mV
Signal-to-noise ratio	R_S = 300 Ω	S/N	–	6.5	–	dB
Keyed AGC						
DC characteristics						
Output voltage range (pin 20)		ΔV_{20}	0.5	–	V_P–0.3	V
AGC output current						
at I_3 = 0 or V_{14} = 450 mV; V_{20} = $V_P/2$		$-I_{20}$	25	50	100	μA
at V_3 = 2 V and V_{14} = 1 V; V_{20} = V_{15}		I_{20}	2	–	5	mA
Narrowband threshold						
at V_3 = 2 V; V_{14} = 550 mV		V_{20}	–	–	1	V
at V_3 = 2 V; V_{14} = 450 mV		V_{20}	V_P–0.3	–	–	V
AC characteristics	f_i = 98 MHz					
Input impedance		R_3	–	4	–	kΩ
		C_3	–	3	–	pF

parameter	conditions	symbol	min.	typ.	max.	unit
Wideband threshold (RMS value) (see Figs 3, 4, 5 and 6) at V_{14} = 0.7 V; $V_{20} = V_P/2$; I_{20} = 0		$EMF_{2(rms)}$	–	17	–	mV
Oscillator output buffer (pin 9)						
DC output voltage		V_9	–	6	–	V
Oscillator output voltage (RMS value)						
at R_L = oo; C_L = 2 pF		$V_{9(rms)}$	–	110	–	mV
at R_L = 75 Ω		$V_{9(rms)}$	30	50	–	mV
DC output resistance		$R_{9\text{-}17}$	–	2.5	–	kΩ
Signal purity						
Total harmonic distortion		THD	–	–15	–	dB
Spurious frequencies at EMF1 = 1 V; R_{S1} = 50 Ω		f_S	–	–35	–	dB
Electronic standby switch (pin 11)						
Oscillator; linear IF amplifier; AGC	T_{amb} = –40 to + 85 °C					
Input switching voltage						
for threshold ON	$V_{20} = > V_P–3$ V	V_{13}	0	–	2.3	V
for threshold OFF	$V_{20} = < 0.5$ V	V_{13}	3.3	–	23	V
Input current						
at ON condition	V_{13} = 0 V	$-I_{13}$	–	–	150	µA
at OFF condition	V_{13} = 23 V	$-I_{13}$	–	–	10	µA
Input voltage	I_{13} = 0	V_{13}	–	–	4.4	V

Notes to the characteristics

1. Power gain conversion is equated by the following equation:

$$10 \log \frac{4\,(V_{M(out)}\ 10.7\ \text{MHz})^2}{(EMF1\ 98\ \text{MHz})^2} \times \frac{R_{S1}}{R_{ML}}$$

2. Voltage gain is equated by the following equation:

$$20 \log \frac{V_{12}}{V_{16\text{-}15}}$$

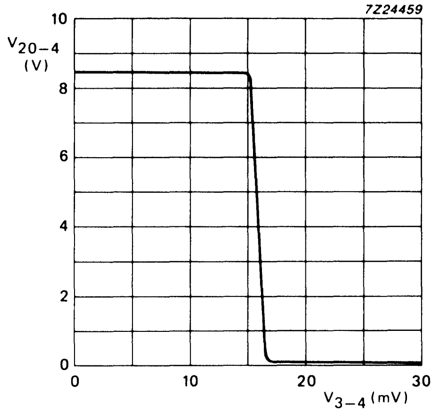


Fig.3 Keyed AGC output voltage V_{20} as a function of RMS input voltage V_3. Measured in test circuit Fig.1 at V_{14} = 0.7 V; I_{20} = 0.

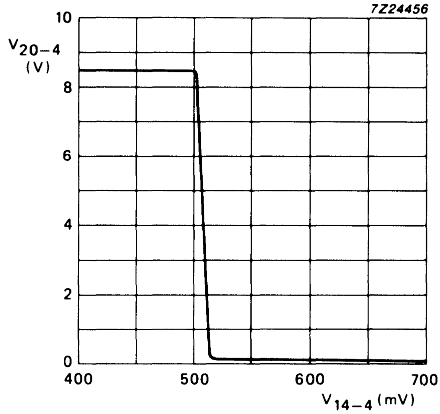


Fig.4 Keyed AGC output voltage V_{20} as a function of input voltage V_{14}. Measured in test circuit Fig.1 at V_3 = 2 V; I_{20} = 0.

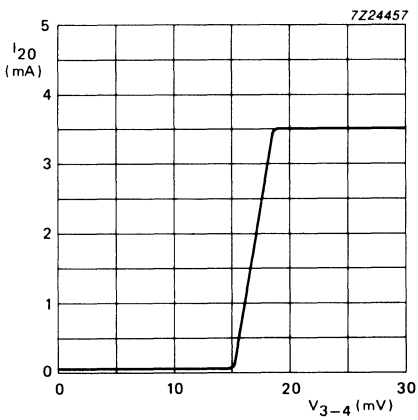


Fig.5 Keyed AGC output current I_{20} as a function of RMS input voltage V_3. Measured in test circuit Fig.1 at V_{14} = 0.7 V; V_{20} = 8.5 V.

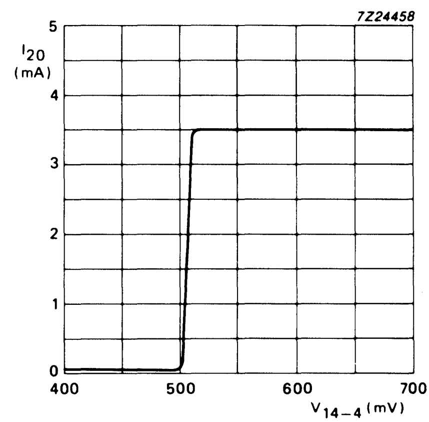
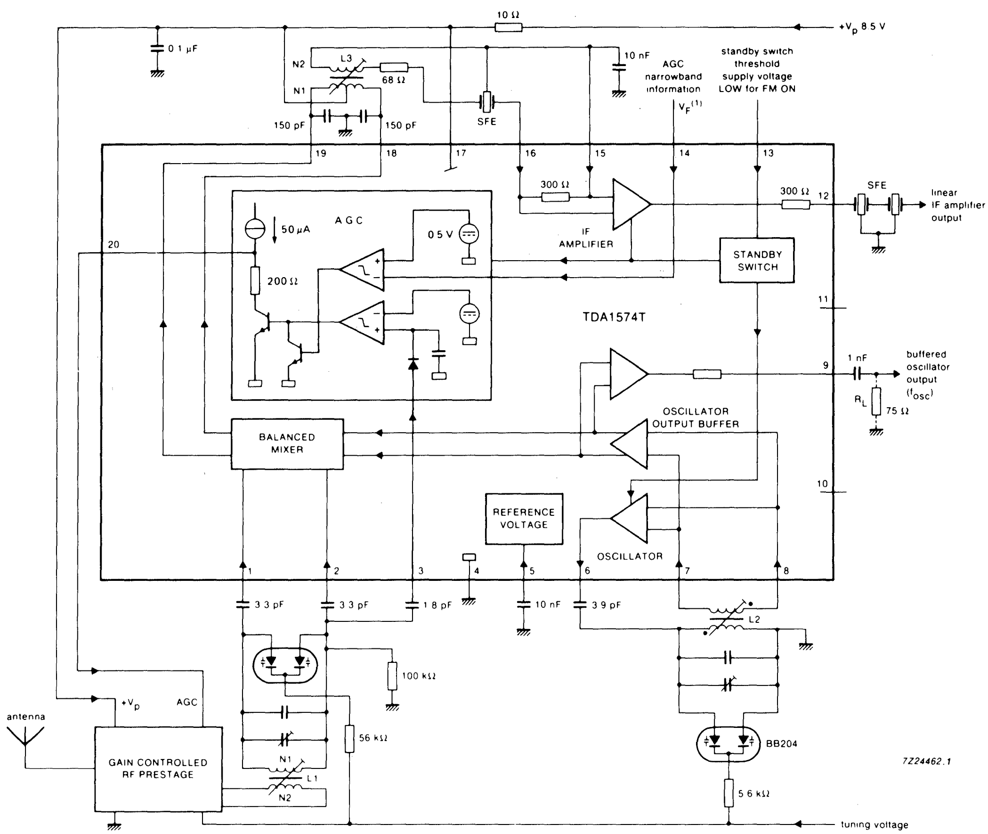


Fig.6 Keyed AGC output voltage I_{20} as a function of input voltage V_{14}. Measured in test circuit Fig.1 at V_3 = 2 V; V_{20} = 8.5 V.



Coil data

L1: TOKO MC-108, N1 = 5.5 turns, N2 = 1 turn

L2: }
L3: } see Fig.1

(1) Field strength indication of main IF amplifier.

Fig.7 TDA1574T application diagram.

GENERAL DESCRIPTION

The TDA5030A provides VHF local oscillator, VHF mixer and UHF IF preamplifier functions for VHF/UHF television receivers. It includes a buffered output from the VHF local oscillator, a VHF/UHF switching circuit and an IF amplifier stage for an external SAW filter.

Features

- Balanced VHF mixer
- Voltage-controlled VHF local oscillator
- IF amplifier for SAW filter
- UHF IF preamplifier
- Local oscillator buffer output for external prescaler
- Voltage stabilizer
- UHF/VHF switching circuit
- Electrostatic discharge protection diodes at pins 10, 11, 12 and 13

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 15	V_P	10	–	13,2	V
Supply current		I_P	–	42	–	mA
VHF mixer frequency range		f	50	–	470	MHz
Conversion gain			–	24,5	–	dB
Conversion noise	300 MHz		–	10	–	dB
Input signal for 1% cross modulation			–	99	–	dBμV
Storage temperature range		T_{stg}	–55	–	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	–	+ 85	°C

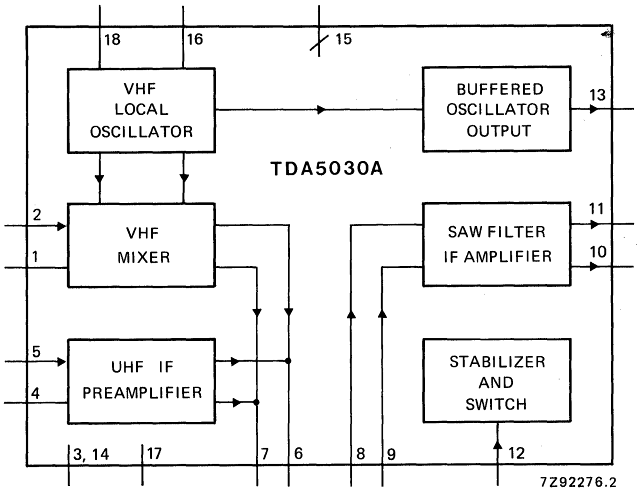


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 15	$V_P = V_{15\text{-}3}$	–	14	V
Input voltage	pins 1, 2, 4 and 5	V_i	0	5	V
VHF switching voltage	pin 12	V_{12}	0	V_{15}+ 0,3	V
Output current	pins 10, 11 or 13	$-I_{10, 11, 13}$	–	10	mA
Short-circuit time on outputs	pins 10 and 11	t_{ss}	–	10	s
Storage temperature range		T_{stg}	–55	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	+ 85	°C
Junction temperature range		T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 55 K/W

CHARACTERISTICS

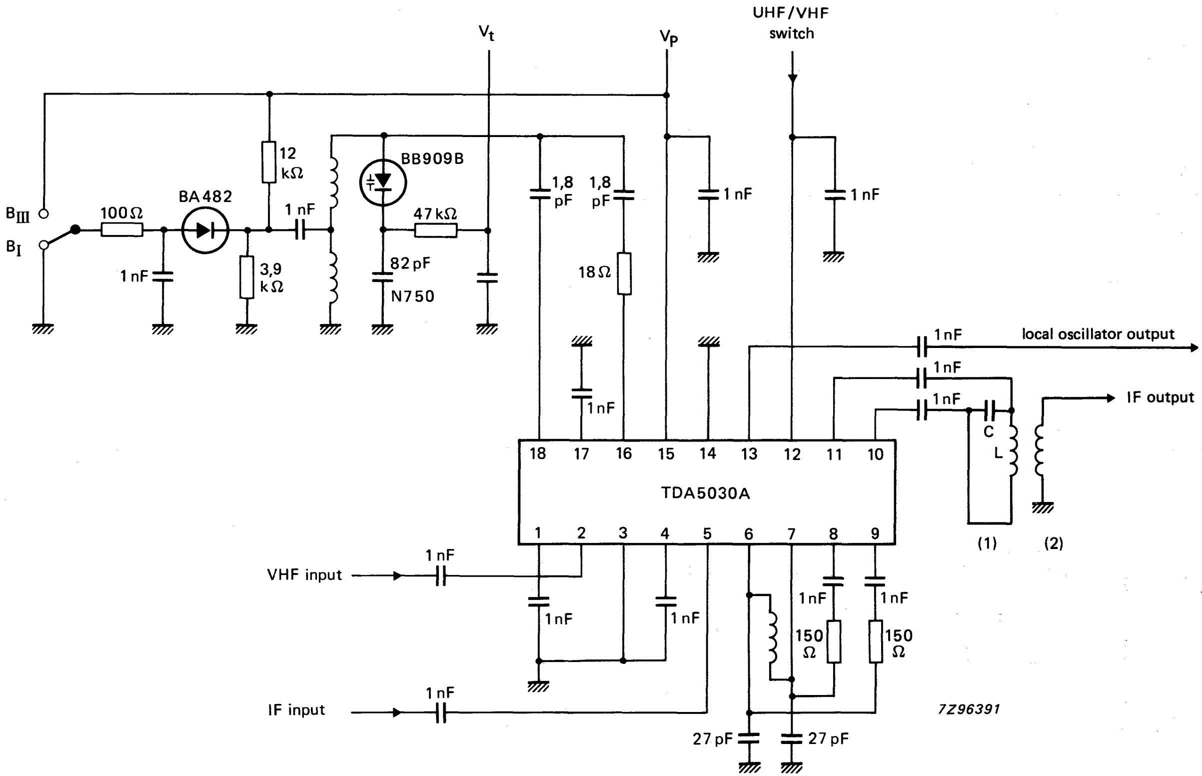
Measured in circuit of Fig. 2, $V_P = V_{15\text{-}3} = 12$ V, $T_{amb} = 25\ ^oC$, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	pin 15	$V_{15\text{-}3}$	10	–	13,2	V
Supply current		I_{15}	–	42	55	mA
Switch voltage level for VHF	pin 12	V_{12}	0	–	2,5	V
Switch voltage level for UHF	pin 12	V_{12}	9,5	–	V_{15}+0,3	V
Switch current	UHF selected	I_{12}	–	–	0,7	mA
VHF mixer (including IF amplifier)						
Frequency range		f	50	–	470	MHz
Noise factor	pin 2					
	f = 50 MHz	F	–	7,5	9	dB
	f = 225 MHz	F	–	9	10	dB
	f = 300 MHz	F	–	10	12	dB
	f = 470 MHz	F	–	11	13	dB
Optimum source conductance	pin 2					
	f = 50 MHz	G	–	0,5	–	mS
	f = 225 MHz	G	–	1,1	–	mS
	f = 300 MHz	G	–	1,2	–	mS
Input conductance	pin 2					
	f = 50 MHz	G_i	–	0,23	–	mS
	f = 225 MHz	G_i	–	0,5	–	mS
	f = 300 MHz	G_i	–	0,67	–	mS
Input capacitance	pin 2					
	f = 50 MHz	C_i	–	2,5	–	pF
Input voltage for 1% cross-modulation (in channel)		$V_{2\text{-}3}$	97	99	–	dBμV
Input voltage for 10 kHz pulling (in channel)	$f < 300$ MHz	$V_{2\text{-}14}$	100	–	–	dBμV
Voltage gain		A_V	22,5	24,5	26,5	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
UHF preamplifier (including IF amplifier)						
Input conductance	pin 5	G_i	–	0,3	–	mS
Input capacitance	pin 5	C_i	–	3,0	–	pF
Noise factor	pin 5	F	–	5	6	dB
Optimum source conductance	pin 5	G	–	3,3	–	mS
Input voltage for 1% cross-modulation (in channel)		$V_{5\text{-}14}$	88	90	–	dBμV
Voltage gain		A_v	31,5	33,5	35,5	dB
VHF mixer						
Conversion transadmittance	pins 2 to 6,7	$Y_{c2\text{-}6,7}$	–	5,7	–	mS
Output impedance	pins 6 and 7	Z_o	–	1,6	–	kΩ
VHF oscillator						
Frequency range		f	70	–	520	MHz
Frequency shift	ΔV_P = 10%; f = 70–330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 15 K; f = 70–330 MHz	Δf	–	–	250	kHz
Frequency drift	between 5 s and 15 min after switch-on	Δf	–	–	200	kHz
SAW filter IF amplifier						
Input impedance	$Z_{10,11}$ = 2 kΩ; f = 36 MHz	$Z_{8,9}$	–	300+ j100	–	Ω
Transimpedance		$Z_{8,9\text{-}10,11}$	–	2,2	–	kΩ
Output reflection coefficient:	f = 36 MHz					
modulus			0,45	0,37	0,41	
phase			−63	−112	−134	deg

parameter	conditions	symbol	min.	typ.	max.	unit
VHF local oscillator output buffer						
Output voltage	pin 13 R_L = 75 Ω f < 100 MHz	V_{13}	14	20	–	mV
	f > 100 MHz	V_{13}	10	20	–	mV
Output impedance	f = 100 MHz	Z_{13}	–	90	–	Ω
RF signal on local oscillator output	R_L = 75 Ω V_i = 1 V; f ⩽ 225 MHz	RF/(RF+LO)	–	–	10	dB
	V_i = 0,3 V; f = 225–300 MHz	RF/(RF+LO)	–	–	10	dB
IF signal on local oscillator output	UHF selected; R_L = 75 Ω; V_i = 350 mV	IF/(IF+LO)	–	–	3	mV
Local oscillator harmonics w.r.t. local oscillator output signal	R_L = 75 Ω		–	–	–14	dB



(1) C = 18 pF, L = 2,2 μH, f_{CL} = 36,5 MHz.

(2) Turns ratio = 7 : 1, load = 50 Ω.

Fig. 2 Test circuit.

Section 5
Audio and Data Processors

RF Communications

INDEX

Audio processor - companding and amplifier section NE/SA5750

DESCRIPTION

The NE/SA5750 is a high performance low power audio signal processing system. The NE/SA5750 subsystems include a low noise microphone preamplifier with adustable gain, a noise cancellation switching amplifier with adjustable threshold, a voice operated transmitter (VOX) switch, VOX control, an audio compressor with buffered input, audio expandor, a unity gain power amplifier to drive a speaker, a summing power amplifier for sidetone attenuation and headphone (earpiece) drive, and an internal bandgap voltage regulator with power down capability. When used with Signetics' NE/SA5751, the complete audio processing function of an AMPS or TACS cellular telephone is easily implemented. The NE/SA5750 can also be used without the NE/SA5751 in a wide variety of radio communications applications.

FEATURES

- High performance
- 5V supply
- Adjustable VOX and noise cancellation threshold
- Adjustable gain preamplifier
- Audio companding
- ESD protected
- Open collector VOX output
- Logic inputs CMOS compatible
- Power down mode
- Built-in drivers for speaker and earpiece
- Few external components
- SOL and DIP packages

BENEFITS

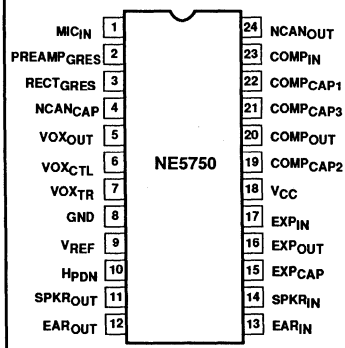
- Very compact applications
- Long battery life in portable equipment
- Complete cellular audio function with the SA5751

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION

D[1] and N PACKAGE



NOTE:
1. Available only in SOL (large SO) package.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	0 to +70°C	NE5750N
24-Pin Plastic SOL	0 to +70°C	NE5750D
24-Pin Plastic DIP	-40 to +85°C	SA5750N
24-Pin Plastic SOL	-40 to +85°C	SA5750D

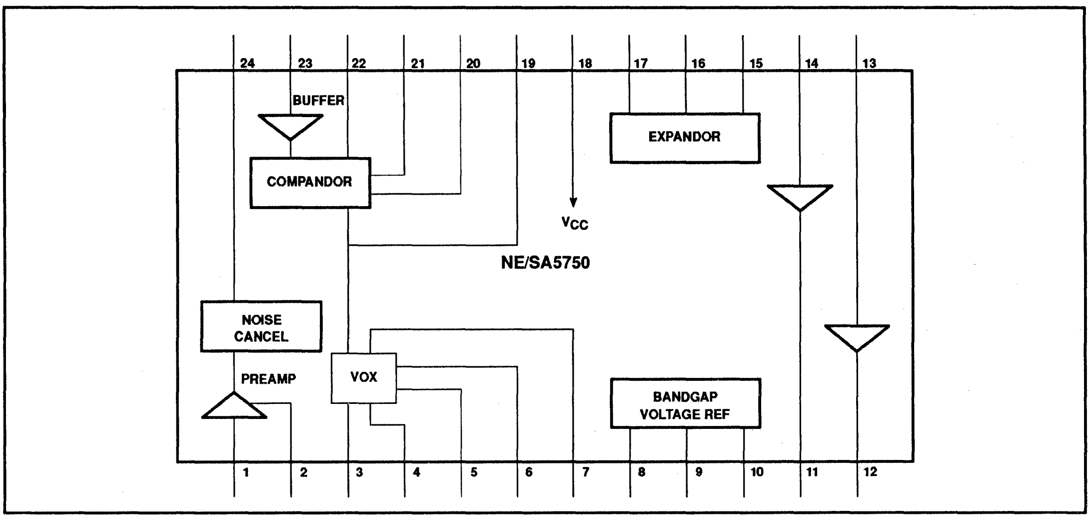
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage Voltage applied to any pin	6 -0.3 to (V_{CC} + 0.3)	V V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature NE5750 SA5750	 0 to 70 -40 to +85	°C

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	MIC_{IN}	Microphone input
2	$PREAMP_{GRES}$	Preamplifier gain resistor
3	$RECT_{GRES}$	Reactifier gain resistor
4	$NCAN_{CAP}$	Noise cancellation timing capacitor
5	VOX_{OUT}	Voice operated transmission output
6	VOX_{CTL}	Voice operated transmission control
7	VOX_{TR}	Voice operated transmission threshold resistor
8	GND	Ground
9	V_{REF}	Reference voltage
10	H_{PDN}	Hardware power down
11	$SPKR_{OUT}$	Speaker output
12	EAR_{OUT}	Earpiece output
13	EAR_{IN}	Earpiece input, side tone input
14	$SPKR_{IN}$	Speaker input
15	EXP_{CAp}	Expandor timing capacitor
16	EXP_{OUT}	Expandor output
17	EXP_{IN}	Expandor input
18	V_{CC}	Positive supply
19	$COMP_{CAP2}$	Compressor timing capacitor 2
20	$COMP_{OUT}$	Compressor output
21	$COMP_{CAP3}$	Compressor timing capacitor 3
22	$COMP_{CAP1}$	Compressor timing capacitor 1
23	$COMP_{IN}$	Compressor input
24	$NCAN_{OUT}$	Noise cancellation output

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5.0V, 0dB = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.75	5.0	5.25	V
I_{CC}	Supply current	No signal Power down mode		8.4 1.8	12.0 3.0	mA mA
Z_L	Load impedance pins $NCAN_{OUT}$, EXP_{OUT}		50			kΩ
	$COMP_{OUT}$[1]		10			kΩ
Z_{IN}	Input impedance $COMP_{IN}$, MIC_{IN}, $SPKR_{IN}$		40	50	60	kΩ
	EXP_{IN}[2]		2.0	2.5		kΩ
	Noise cancellation current	Pin 7, grounded	40	50	60	μA
V_{OS}	DC offset $NCAN_{OUT}$[3]		-50		50	mV

NOTES:
1. Compressor is tested in production with 50kΩ load.
2. Not tested in production.
3. Offset values are identical for both gain states of noise reduction circuit.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5.0V, 0dB level = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	Preamplifier gain range Preamplifier voltage gain 0dB Preamplifier voltage gain 40dB	 Pin 2 open Pin 2 AC ground	0 -1.0 39.0	 0 40	40 1.0 41.0	dB dB dB
	Preamplifier noise density	Pin 2 AC grounded RS = 0 - 50kΩ unweighted 20Hz-20kHz		7		$nV/\sqrt{Hz}$
		weighted CCIR DIN45405 20-20kHz		8		$nV/\sqrt{Hz}$
	Switch amplifier gain		9	10	11	dB
	Sidetone attenuation range				30	dB
Compandor 1kHz, all tests[1]						
$COMP_{OUT}$	Compressor error at -21dB output level	Input level = -42dB		0.38		dB
$COMP_{OUT}$	Compressor error at -10dB output level	Input level = -20dB	-1.0		1.0	dB
$COMP_{OUT}$	Compressor error at 0dB output level	Input level = 0dB	-1.5	0.12	1.5	dB
$COMP_{OUT}$	Compressor error at +5dB output level	Input level = +10dB	-1.0		1.0	dB
$COMP_{OUT}$	Compressor error at +12.3dB output level	Input level = +24.6dB	-1.0		1.0	dB
EXP_{OUT}	Expandor error at -42dB output level	Input level = -21dB		-0.41		dB
EXP_{OUT}	Expandor error at -21dB output level	Input level = -10.5dB	-1.0		1.0	dB
EXP_{OUT}	Expandor error at -10dB output level	Input level = -5dB	-1.0		1.0	dB
EXP_{OUT}	Expandor error at 0dB output level	Input level = 0dB	-1.5	-0.18	1.5	dB
EXP_{OUT}	Expandor error at +10dB output level	Input level = +5dB	-1.0		1.0	dB
EXP_{OUT}	Expandor error at +24.6dB output level[2]	Input level = +12.3dB	-1.5		1.5	dB
EXP_{OUT}	Expandor V_{OS}	No signal	-50.0		50.0	mV
EXP_{OUT}	Expandor output DC shift	No signal to 0dB	-100		100	mV

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = +5.0V$, 0dB level = $77.5mV_{RMS}$. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
	Timing capacitors compandor			2.2		μF
THD	Total harmonic distortion Compressor	1kHz, 0dB		0.09	1	%
	Expandor	1kHz, 0dB		0.09	1	%
	$NCAN_{OUT}$	1kHz. Pin 2 open output level = 0dB		0.18	1	%
		1kHz, Pin 2 open output level = +25dB		0.13	1	%
	Speaker amplifier Drive capability				40	mA_{P-P}
	Output swing (<1% THD)	50Ω load	2	3.2		V_{P-P}
		100Ω load	3	4.1		V_{P-P}
		No load	4	4.9		V_{P-P}
	Ear amplifier Drive capability				10	mA_{P-P}
	Output swing (<1% THD)	300Ω load	3	4.3		V_{P-P}
		2000Ω load	4	4.9		V_{P-P}
		No load	4	4.9		V_{P-P}
VOX_{OUT}	Sink current				0.5	mA
	Low level High level	Open collector $I_L = 0.5mA$	 4	0.07 5	0.4	V V
VOX_{CTL}	Input current Low		-50	-21	0	μA
	High		-10		+10	μA
	Input level Low High		0 3.5		1.5 5	V V
H_{PDN}	Input current Low		-10		+10	μA
	High		-10		+10	μA
	Input level Low High		0 3.5		1.5 5	V V
	Reference filter capacitor			10		μF

NOTE:

1. Measurements are relative to 0dB output.
2. Measurement is absolute and indicative of the output dynamic range capability.

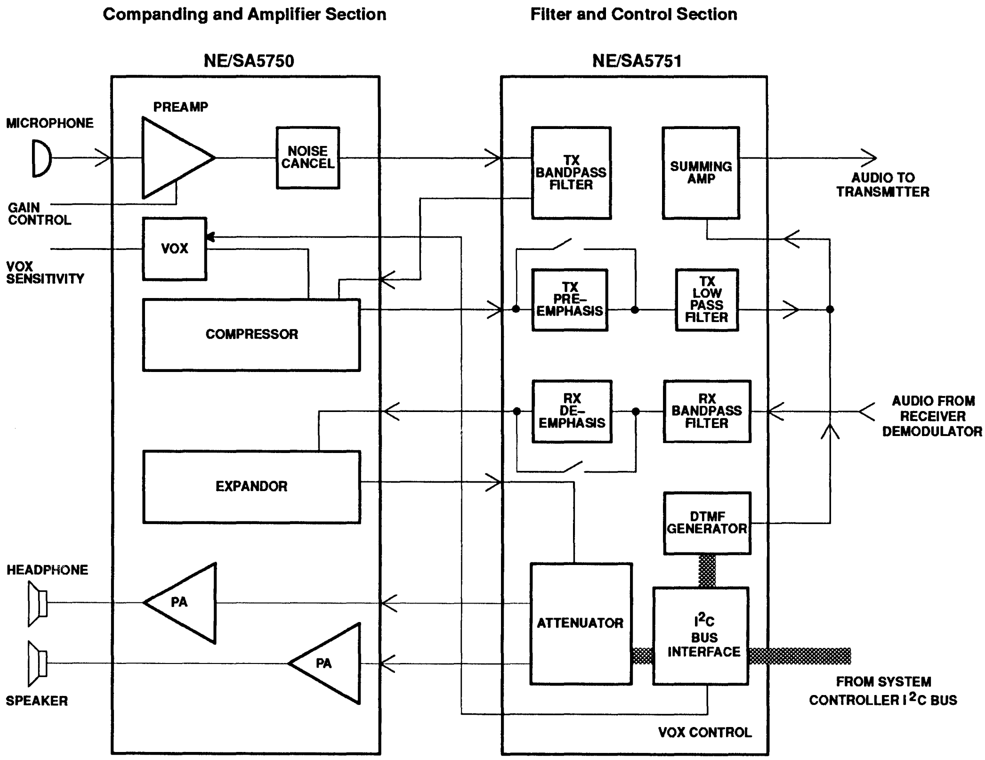


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

New Devices

CMOS

NE 5752

NE 5753

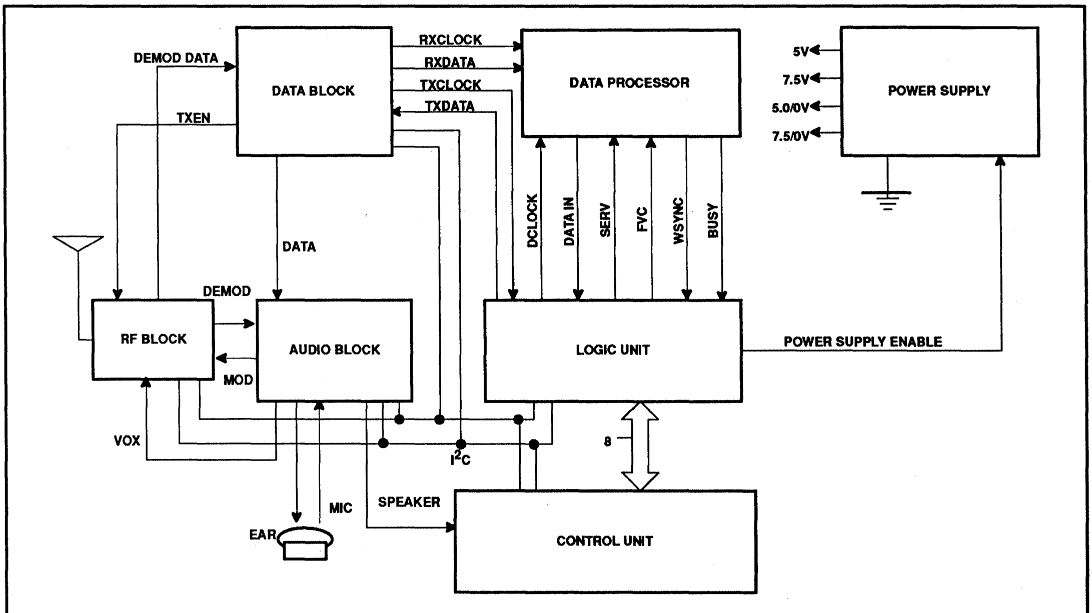


Figure 2. Cellular Radio System

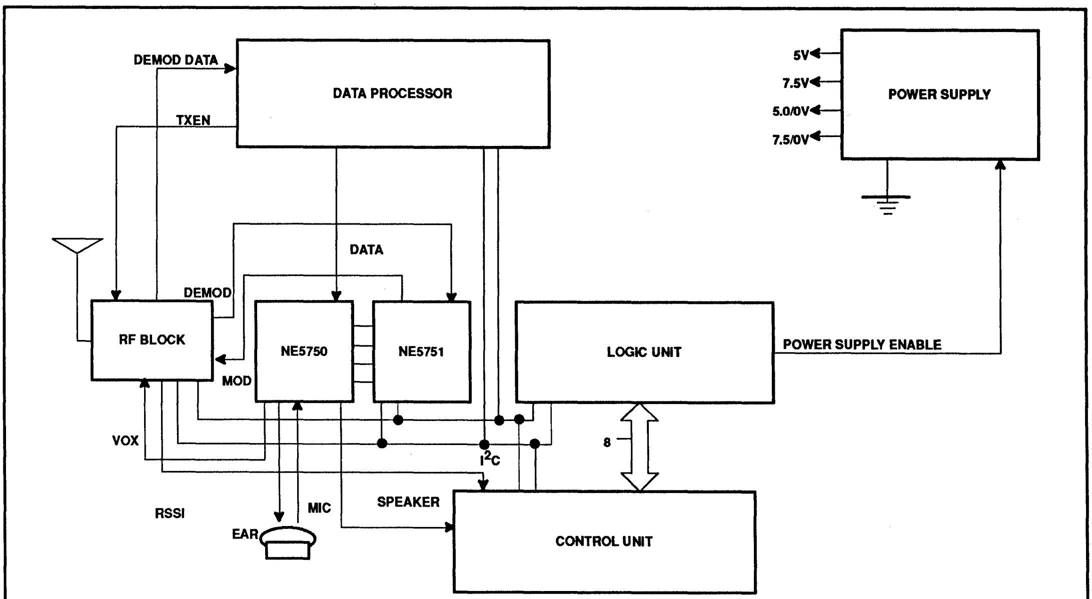


Figure 3. APROC Application Diagram

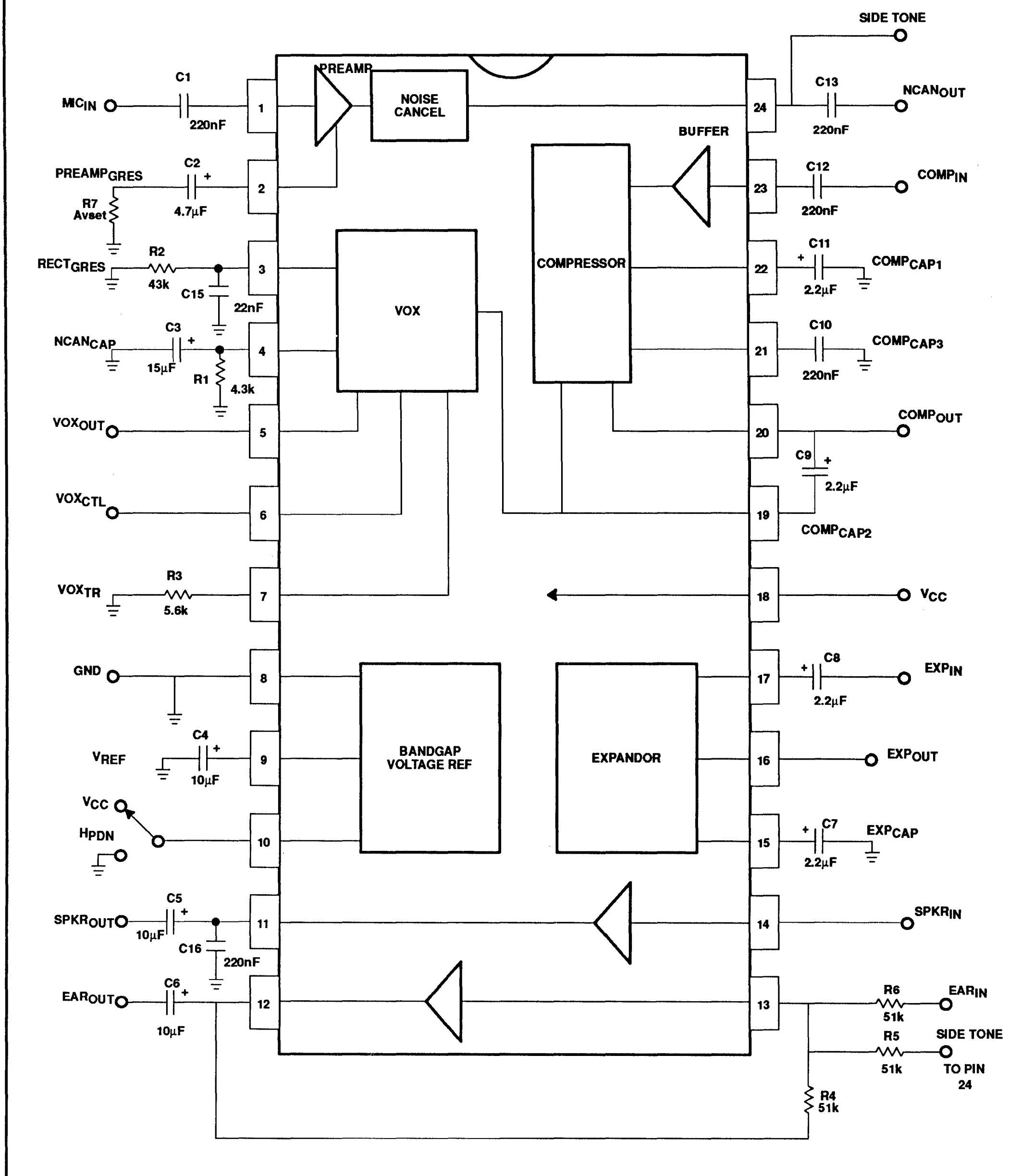


Figure 4. NE/SA5750 Test and Application Circuit

Audio processor - filter and control section

NE/SA5751

DESCRIPTION

The NE/SA5751 is a high performance low power CMOS audio signal processing system. The NE/SA5751 subsystems include complementary transmit/receive voice band (300-3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, a digitally controlled volume control with 30dB range (in 2dB steps), audio path mute switches, a programmable DTMF generator, power- down circuitry for low current standby, power-on reset capability, and an I^2C interface. When the SA5751 is used with an SA5750 (companding function), the complete audio processing system of an AMPs or TACs cellular telephone is easily implemented.

FEATURES

- Low power
- High performance
- 5V supply
- Built-in programmable DTMF generator
- Built-in digitally controlled volume control
- Built-in peak-deviation limit
- I^2C Bus controlled
- Power-on reset
- Power-down capability

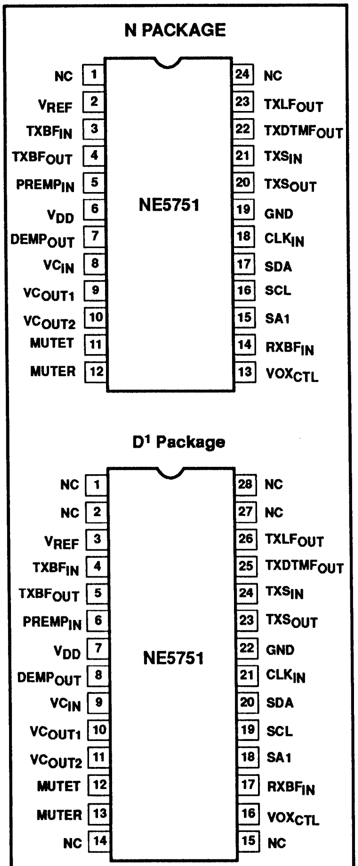
BENEFITS

- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5750

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION



NOTE:
1. Available in SOL (large surface mount) package only

ORDERING INFORMATION

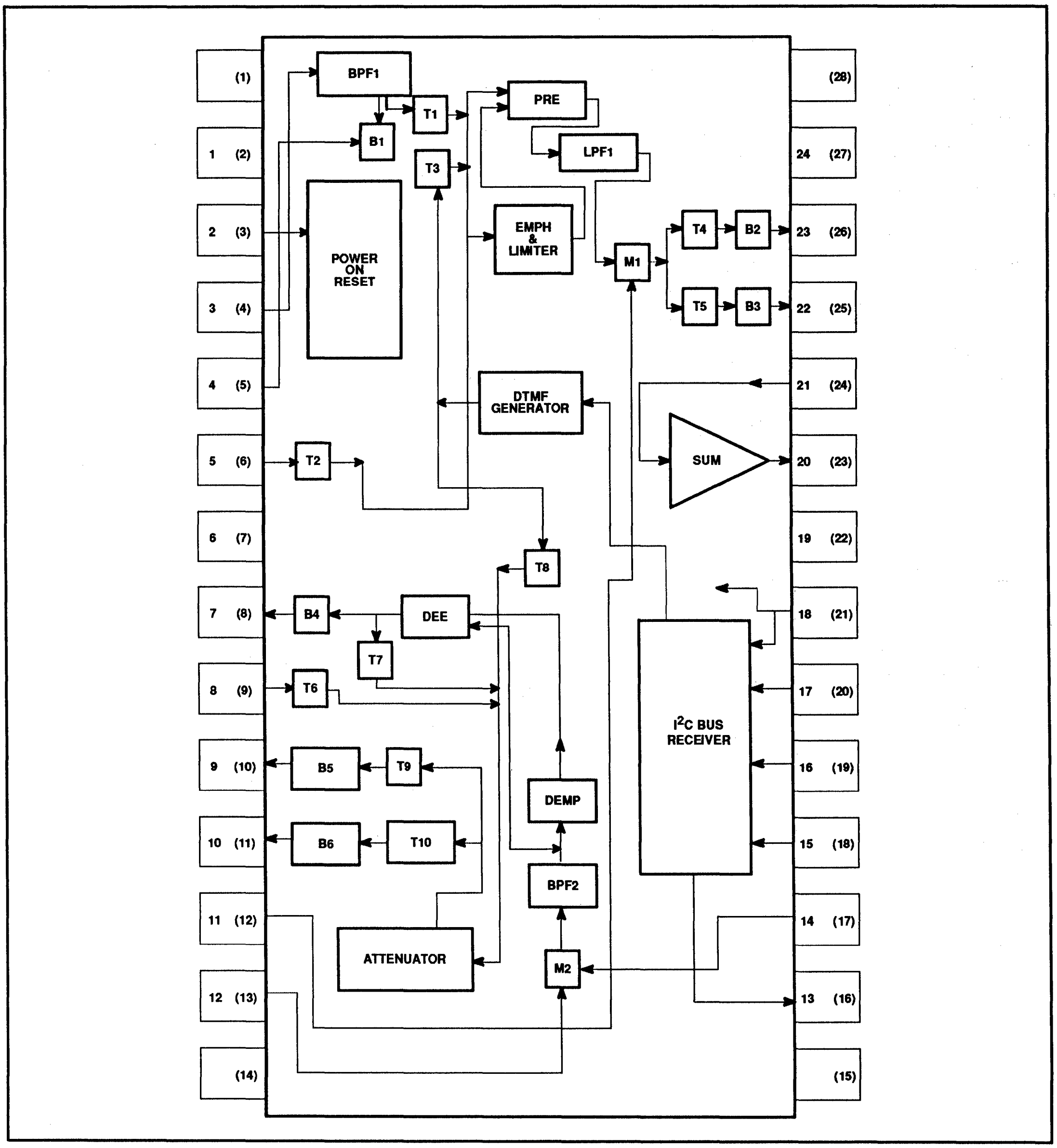
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	0 to +70°C	NE5751N
28-Pin Plastic SOL	0 to +70°C	NE5751D
24-Pin Plastic DIP	-40 to +85°C	SA5751N
28-Pin Plastic SOL	-40 to +85°C	SA5751D

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
(1)	NC	Not connected
1 (2)	NC	Not connected
2 (3)	V_{REF}	Reference voltage
3 (4)	$TXBF_{IN}$	Transmit bandpass filter input
4 (5)	$TXBF_{OUT}$	Transmit bandpass filter output
5 (6)	$PREMP_{IN}$	Pre-emphasis input
6 (7)	V_{DD}	Positive supply
7 (8)	$DEMP_{OUT}$	De-emphasis output
8 (9)	VC_{IN}	Volume control input
9 (10)	VC_{OUT1}	Volume control output 1
10 (11)	VC_{OUT2}	Volume control output 2
11 (12)	MUTET	TX analog voice path mute input
12 (13)	MUTER	RX analog voice path mute input
(14)	NC	Not connected
(15)	NC	Not connected
13 (16)	VOX_{CTL}	Vox control output
14 (17)	$RXBF_{IN}$	Receive bandpass filter input
15 (18)	SA1	Serial bus address
16 (19)	SCL	Serial clock line
17 (20)	SDA	Serial data line
18 (21)	CLK_{IN}	Clock input
19 (22)	GND	Ground
20 (23)	TXS_{OUT}	Transmit summer output
21 (24)	TXS_{IN}	Transmit summer input
22 (25)	$TXDTMF_{OUT}$	Transmit DTMF output
23 (26)	$TXLF_{OUT}$	Transmit low-pass filter output
24 (27)	NC	Not connected
(28)	NC	Not connected

NOTE:
1. Callouts are for N package; those in parentheses are for the D (SOL) package.

BLOCK DIAGRAM



NOTES:
1. T1 to T10 represent the signal path switches.
2. M1 and M2 represent the mute switches.
3. PRE and DEE represent the bypass switches for pre-emphasis and de-emphasis, respectively.
4. B1 to B6 represent the output buffers.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Power supply voltage[1]	6	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature NE5751	0 to 70	°C
	SA5751	-40 to +85	°C

NOTE:
1. Voltage applied to any pin -0.3 to V_{DD} +0.3V

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V, unless otherwise specified. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
V_{DD}	Power supply voltage range		4.75	5.0	5.25	V
I_{DD}	Supply current	Operating Standby		2.7 0.9	5.0 2.0	mA mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V. See test circuit, Figure 4. Clock frequency = 1.2MHz; test level = 0dBV = 77.5mV_{RMS} = -20dBm, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f= 1kHz		500		kΩ
	RX BPF gain with de-emphasis	f = 1kHz	-0.5	0	0.5	dB
	RX BPF gain with de-emphasis	f = 100Hz		-31	-29	dBm0
	RX BPF gain with de-emphasis	f = 300Hz	9.0	9.6	11.0	dBm0
	RX BPF gain with de-emphasis	f = 3kHz	-11.0	-10.0	-9.0	dBm0
	RX BPF gain with de-emphasis	f = 5.9kHz		-68	-50	dBm0
	RX BPF noise with de-emphasis	300Hz-3kHz		170		μV_{RMS}
	RX dynamic range	with deemphasis		80		dB
	$DEMP_{OUT}$ output impedance	f = 1kHz		40		Ω
	$DEMP_{OUT}$ output swing (1%)	2.3kΩ to V_{REF}; f = 1kHz	V_{DD} -3	3.5		V_{P-P}
	VC_{OUT1} ouput swing (1%)	50kΩ toV_{REF}; f = 1kHz	V_{DD} -1	4.5		V_{P-P}
	VC_{OUT2} output swing (1%)	50kΩ to V_{REF}; f = 1kHz	V_{DD} -1	4.5		V_{P-P}
	VC_{OUT1} noise	VC_{IN} grounded C - message		25		μV_{RMS}
	VC_{OUT2} noise	VC_{IN} grounded C - message		25		μV_{RMS}
	Mute threshold off		0		0.8	V
	Mute threshold on		2.0		5.0	V
	CLK1, 2 high		4.0		5.0	V
	CLK1, 2 low		0		1.0	V
	TX BPF anti alias rejection			40		dB
	TX BPF input impedance	f = 3kHz		500		KΩ

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
	TX BPF noise	300 - 3000kHz		90		μV_{RMS}
	TX LPF gain	f = 5.9kHz		-39	-36	dB
	TX LPF gain with pre-emphasis	f = 1kHz, 20dBV		12.06		dB
	TX LPF gain with pre-emphasis	f = 100Hz		-19		dBm0
	TX LPF gain with pre-emphasis	f = 300Hz		-10.45		dBm0
	TX LPF gain with pre-emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre-emphasis	f = 5900Hz		-39		dBm0
	TX LPF gain with pre-emphasis	f = 9kHz		-51		dBm0
	TX overall gain	1kHz	11.3	11.8	12.5	dB
	TX overall gain	100Hz		-47	-45	dBm0
	TX overall gain	300Hz	-11	-10.4	-9	dBm0
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		-52	-45	dBm0
	TX BPF output impedance	f = 1kHz		360		Ω
	TX BPF output swing (1%THD)	50kΩ to V_{REF} f = 1kHz		4.5		V_{P-P}
	TX BPF dynamic range			90		dB
	$PREMP_{IN}$ input impedance	f = 3kHz		500		kΩ
	Summing op amp					
	Slew rate	C_L = 15pF		0.75		V/μs
	Output impedance	Unity gain; f = 3kHz		40		Ω
	Output swing (1% THD)	1kHz, 5kΩ load (25°C)		4.3		V_{P-P}
	Volume control accuracy	-30dB to 0dB	-1	0	+1	dB
	Analog switches					
	Insertion loss			60		dB
	On time transition	MUTET, MUTER 0.8V ->2.0V		3		μs
	Off time transition	MUTET, MUTER 2.0V ->0.8V		0.25		μs

I²C CHARACTERISTICS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are high. Data transfer may be initiated only when the bus is not busy.

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired-AND function.

Data at the I²C bus can be transferred at a rate up to 100kbits/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

Due to the variety of different devices which can be connected to the I²C bus, the levels of the logical "0" and "1" are not fixed and depend on the appropriate level of V_{DD}. For the typical supply voltage of 5V which is chosen here, logical "1" and logical "0" are, however, fixed respectively on maximum input LOW voltage, 1.5V and minimum input HIGH voltage, 3.0V.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock's cycle. If it does not remain HIGH, it may be interrupted as a control signal.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line while the clock line is HIGH is defined as a start condition S. A LOW to HIGH transition of the data line while the clock is HIGH is defined as a stop condition.

SYSTEM CONFIGURATIONS

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master"; and devices which are controlled by the master are the "slaves".

ACKNOWLEDGE

The number of data bytes transferred between the start and the stop condition from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set up and hold times must be taken into account.

I²C BUS DATA CONFIGURATIONS

The NE5751 is always a slave receiver in the I²C bus configuration (R/W bit-0). The slave address consists of seven bits in the serial mode where the least significant bit is selectable by hardware on input A0 and the other more significant bits are internally fixed.

POWER ON RESET

In order to avoid undefined states of the NE5751 when the power is switched on, a power on reset is supplied. The reset is active when Pin V_{REF} is held below 0.8V. The reset is off when Pin V_{REF} is above 2.0V. Pin V_{REF} is normally at 2.5V generated by a resistive divider from V_{DD}. Nominal impedance is 20kΩ. In a typical application a capacitor is connected to Pin V_{REF} to improve power supply rejection. The time delay of the network resets the internal registers when power is first applied. The signal paths are off in the reset condition. The NE5751 must be programmed via the I²C bus for normal operation. The Power Down mode is defined only when all register values are zero.

CONTROL REGISTERS

Register Map

The address register is as follows:

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	SA1	0

SA1 is controlled by serial bus address pin.

Signal Path Register

MSB							LSB
T10	T9	T8	T6	VOX_{EN}	T4	T3T5	T2

T2 is the transmission gate between Pin $PREEMP_{IN}$ and the emphasis input.

T3T5 connects the output of the DTMF generator to the emphasis input and connects the output of the XMT LPF to Pin $TXDTMF_{OUT}$.

T4 connects the output of the XMT LPF to Pin $TXLF_{OUT}$.

VOX_{EN} enables the VOX function of NE5750.

T6 connects Pin VC_{IN} to the volume control.

T8 connects the output of the DTMF generator to the volume control.

T9 enables VC_{OUT1}.

T10 enables VC_{OUT2}.

Volume Control and Test Register

MSB							LSB
PDW	T1T7	DEE	PRE	V1	V2	V3	V4

V4 is volume control bit 4. This is the MSB. A zero is 16dB attenuation.

V3 is volume control bit 3. A zero is 8dB attenuation.

V2 is volume control bit 2. A zero is 4dB attenuation.

V1 is volume control bit 1. A zero is 2dB attenuation.

PRE is the bypass for the pre-emphasis.

DEE is the bypass for the de-emphasis.

T1T7 is the bypass for the compressor and expandor.

PDW is the control for power down mode.

This mode is defined only when all register values are reset to zero.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

High Frequency = 1200kHz/6/HD
where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

Low Frequency = 1200kHz/12/LD
where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading the two DTMF registers before 96ms have elapsed.

Single tones can be obtained by loading 0, 1 or 2 into one of the registers to silence it.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during operation.

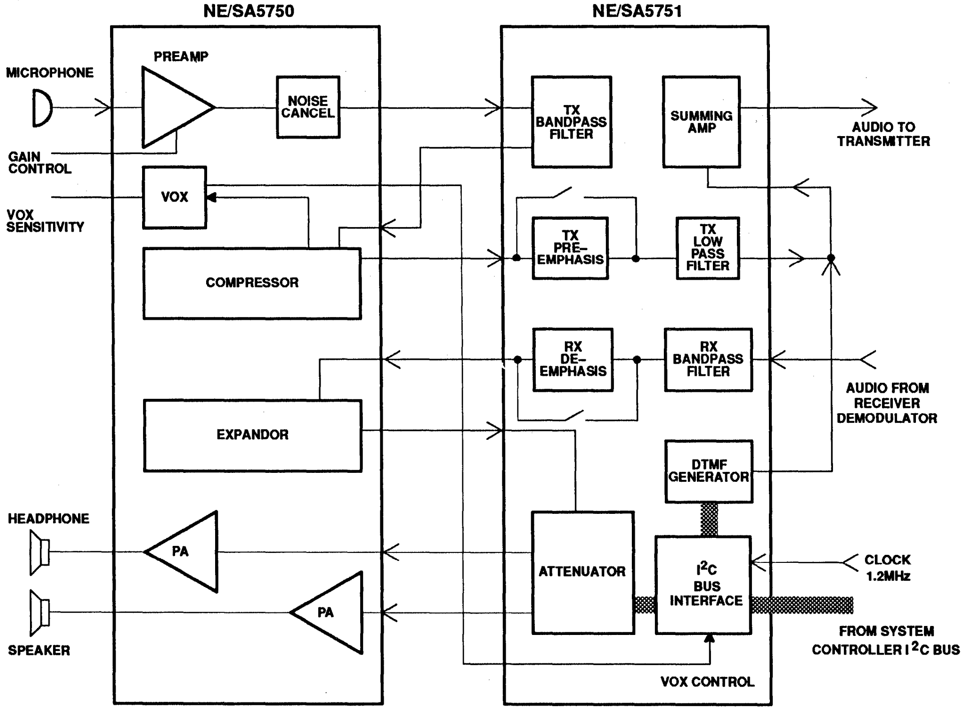


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

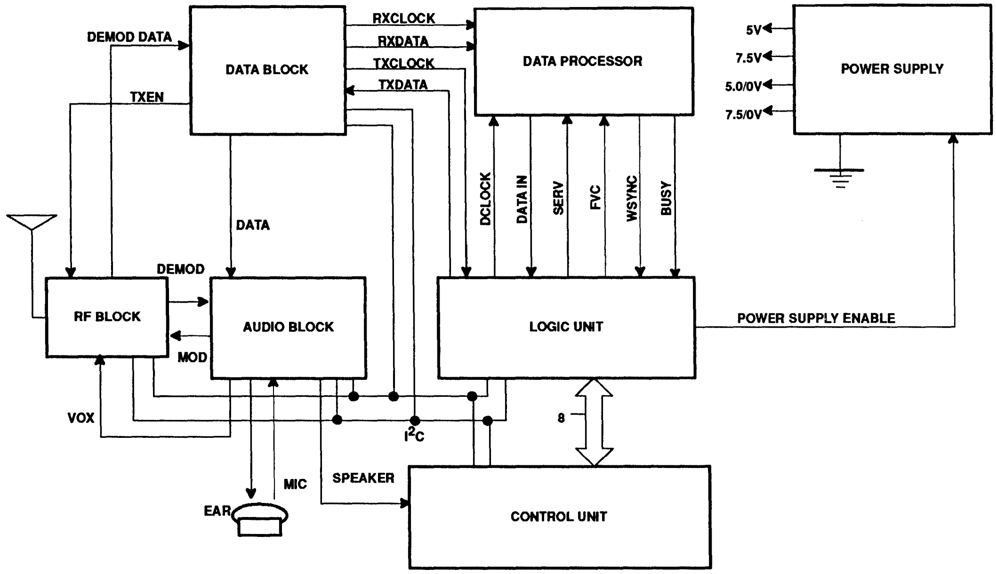


Figure 2. Cellular Radio System

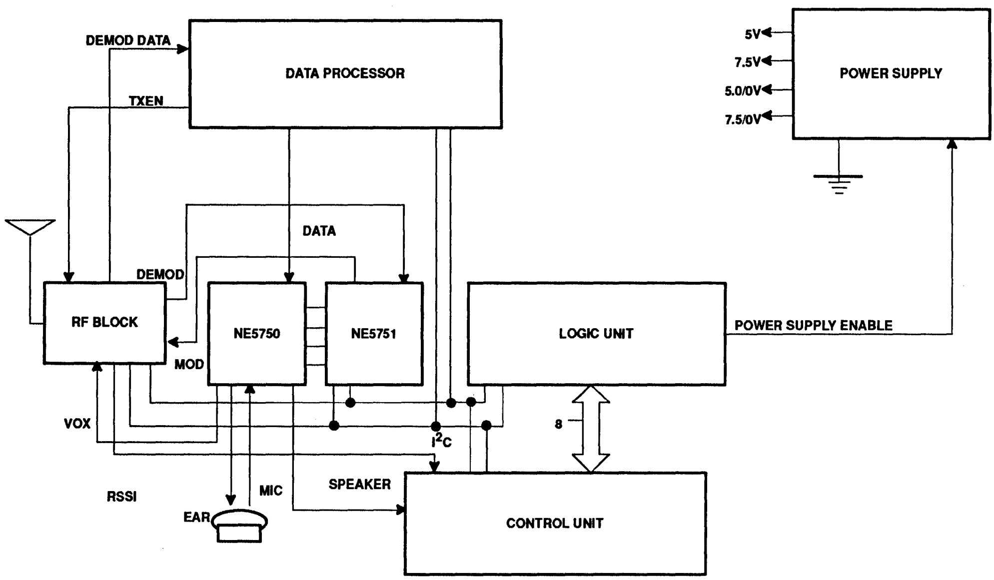


Figure 3. APROC Application Diagram

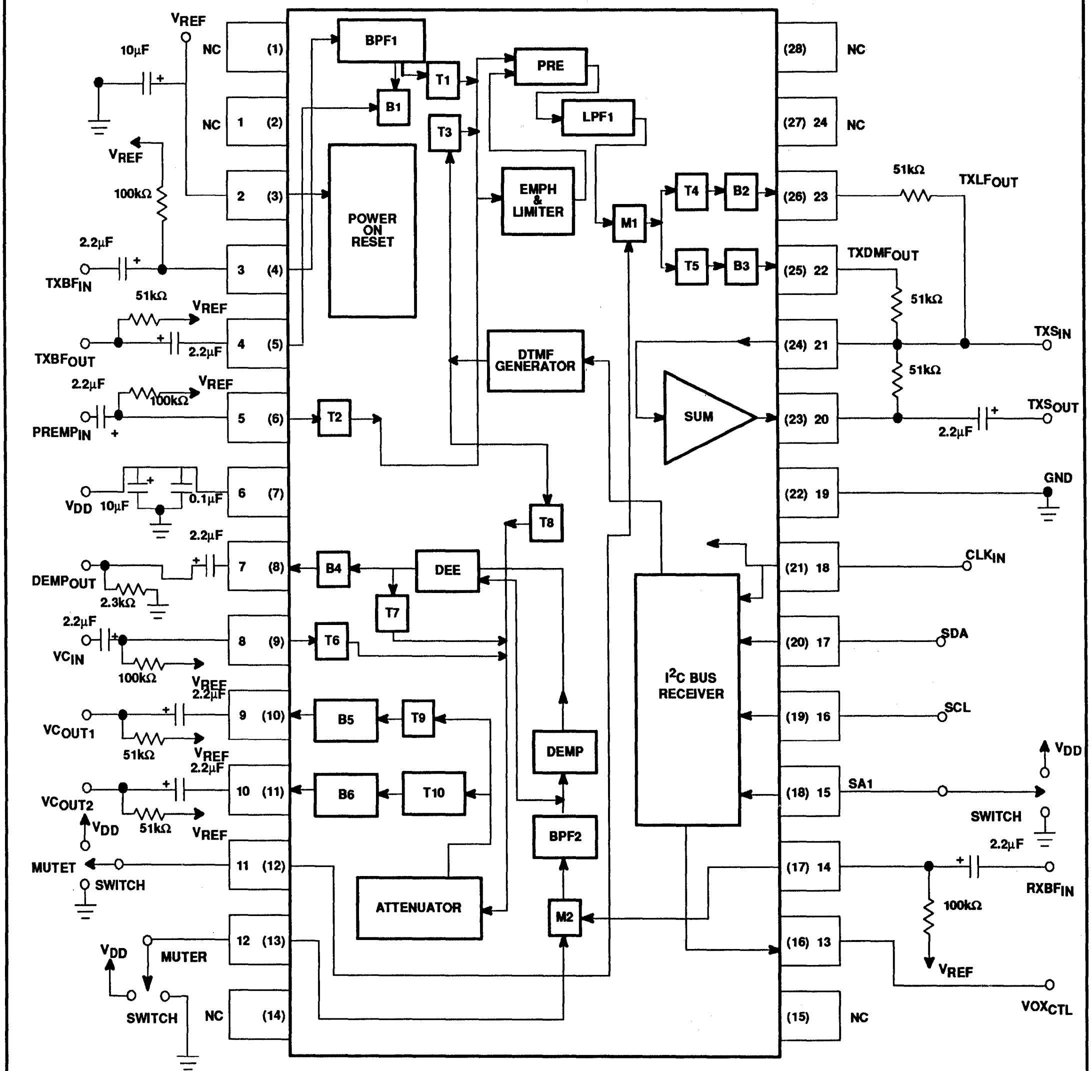
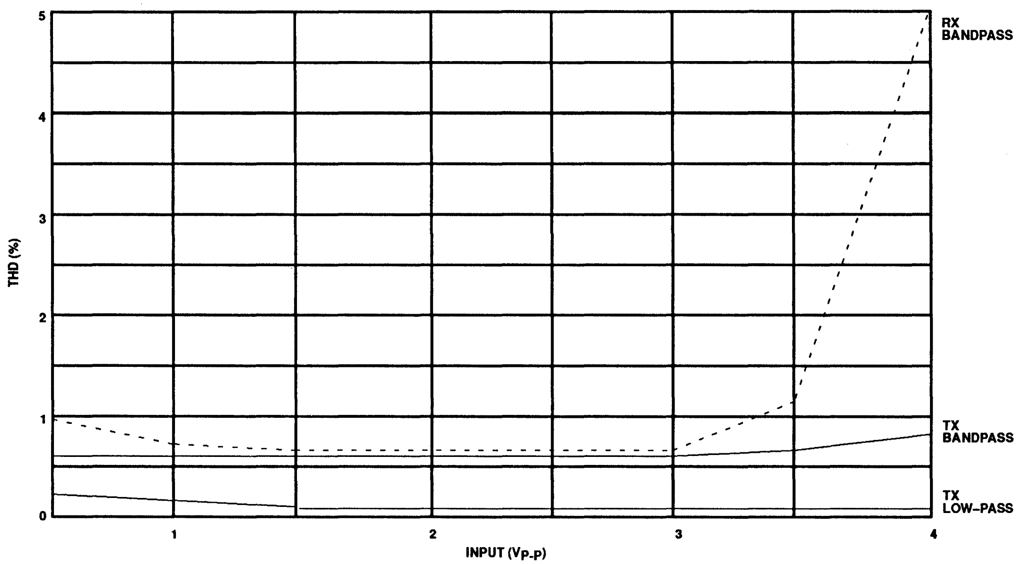


Figure 4. NE/SA5751 Test and Application Circuit

PERFORMANCE CHARACTERISTIC

THD (%) vs INPUT SIGNAL VOLTAGE (1kHz)
FOR THE RX BANDPASS, TX BANDPASS, AND TX LOW–PASS FILTERS



Using the NE5750 and NE5751 for audio processing AN1741

Author: Alvin K. Wong

INTRODUCTION

The NE5750 and the NE5751 are two audio processor chips that can be used in RF communications. The chip-set processes a voice so that by the time it is transmitted and received, the quality is preserved. This is accomplished through the use of compression/expansion and pre-emphasis/de-emphasis.

The audio processor chip-set (APROC) has a wide variety of high performance applications such as cellular phones, cordless voice microphones, cordless intercom systems, standard phones, and hand-held, base, or mobile two-way communications equipment.

Below is an outline of this application note:

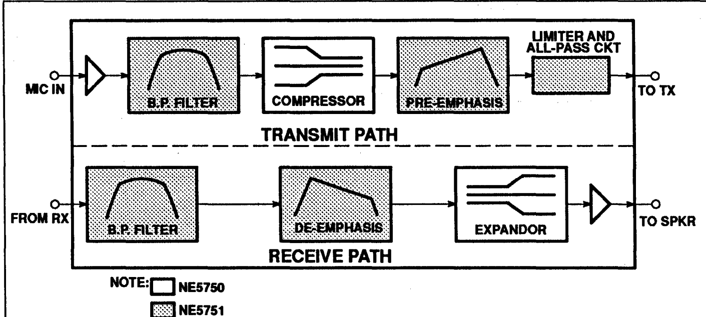


Figure 1. Key Functions of the NE5750 and NE5751 That Contribute to Improving the S/N Ratio and Sensitivity in the System.

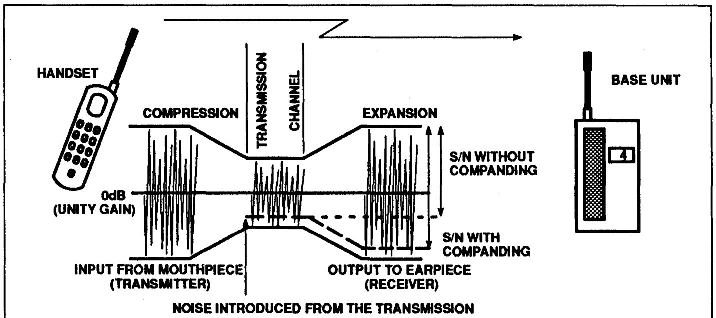


Figure 2. S/N Ratio With Companding vs Without Companding

I. WHAT IS AUDIO PROCESSING

HOW THE VOICE IS PROCESSED BY THE NE5750 and NE5751:

Audio processing begins when a person speaks into a microphone (see Figure 1). The signal is first amplified by the preamp, then screened by a bandpass filter. After the noise is filtered out, the voice signal is processed by the compressor. The function of the compressor is to attenuate loud voices and amplify soft ones. The upper voice frequencies are then amplified by pre-emphasis before their voltage amplitudes are restricted by the limiter and all-pass circuit. When this is completed, the processed voice is ready for transmission.

Since the voice signal was processed by the APROC before transmission, it must be unprocessed upon reception. The received signal is screened again so that the unwanted received noise is blocked before it goes through de-emphasis. In de-emphasis, the upper voice frequencies are attenuated. Then the signal is expanded back to its primary dynamic range by the expandor. Because the voice is restored to its original state, it is ready for amplification by the power amp whose output can be connected to an external speaker. The receiving party will now be able to hear the transmitting party.

MORE DETAIL ON THE KEY FEATURES:

During compression, low level signals are amplified to "jump" over the transmitter channel noise, while the high level signals are compressed to prevent distortion. In general, because we are dealing with a limited dynamic range transmission medium, it is desirable to compress the signal prior to transmission. However, in order to preserve the dynamic range of the original voice signal, the compressed signal is expanded at reception. Figure 2 shows a diagram of a cordless phone application using companding. Note the signal-to-noise ratio with and without companding.

Another key function of the APROC is the pre-emphasis/de-emphasis capability which is used to overcome the "colored" noise, present in all FM receivers, generated by the FM demodulator. This noise worsens at the upper voice band as shown in Figure 3. Therefore, to keep the same signal-to-noise ratio in the lower and upper voice bands, pre-emphasis/de-emphasis is required. A person with a high-pitched voice will now be heard just as well as a person with a low, deep voice.

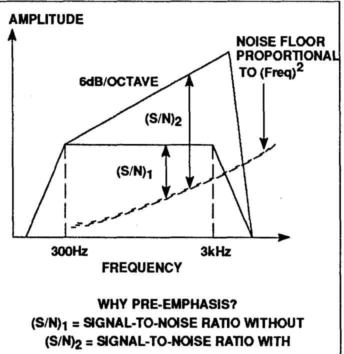


Figure 3. Pre-emphasis Response

Another key stage of the APROC is the limiter with the all-pass circuit. Its main function is to limit the amplitude of the voice signal so that the maximum frequency deviation is limited to 12kHz. Cellular radio specifications allow for a 30kHz channel spacing with an audio bandwidth of 3kHz. Therefore, by Carson's rule the maximum frequency deviation of the limiter must be 12kHz as shown below.

1. Bandwidth = 2 (Modulating Freq + Max Freq Dev)

or

2. Max Freq Dev = Bandwidth/2 – (Mod Freq)
= 30kHz/2 - 3kHz
= 15kHz-3kHz
= 12kHz

PERFORMANCE GRAPHS OF APROC DEMO-BOARD:

Figure 4 shows the general diagram of the audio processor chip set without the external components. External components for the chip set can be found in Figure 31, and the values were chosen for AMPS/TACS specs. To demonstrate the performance of the chip set, data was taken in the lab and resulted in the following figures.

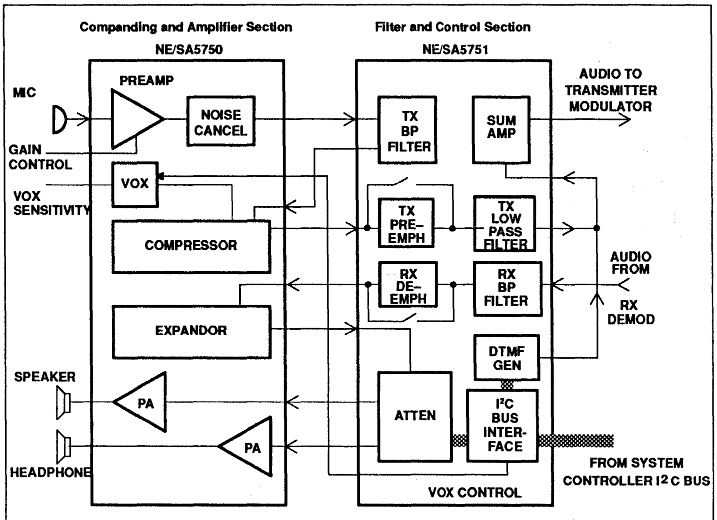


Figure 4. Typical Configuration of Audio Processor (APROC) System Chip Set

Figure 5 Description

Figure 5 reveals what the signal would look like on the bench with different input levels. Figures 5a, b, and c all use the same audio input signal. The audio signal (0-6kHz) varies from 20dB to -30dB in 10dB steps.

Figure 5a

This graph shows the Tx channel. Notice the signal's increase in amplitude as the frequency is increased due to pre-emphasis. Additionally, the slope of the signal decreases as the input increases.

The compressor function is readily shown where a 5dB change in the output level occurs for every 10dB change in the input.

Figure 5b

The 2:1 expansion of audio (20dB change for every 10dB), bandpass filtering and the de-emphasis filter response (300-3kHz) are shown. The graph shows the Rx channel. Notice the signal's decrease in amplitude as the frequency increases due to de-emphasis.

Figure 5c

This shows that a flat frequency response is achieved upon normal reception. Notice the 20dB gap, although the input steps are for 10dB. This is due to the noise canceller turning on. The decrease in amplitude for higher level, higher frequency tones is the result of the deviation limiter action.

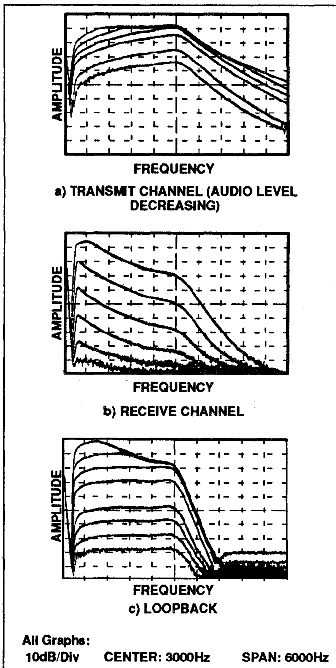


Figure 5.

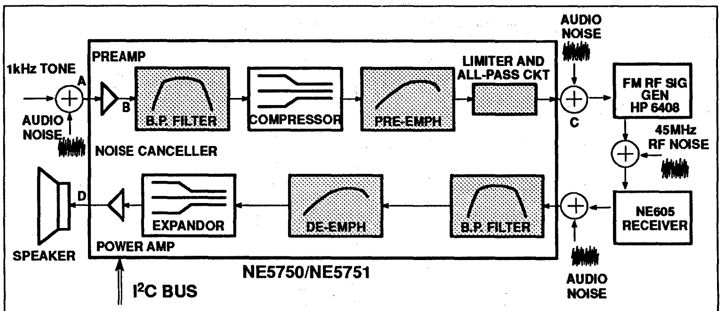
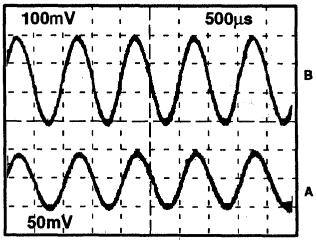
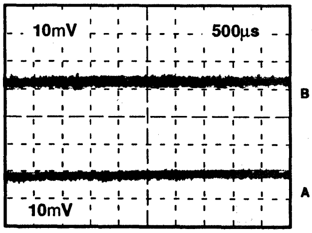


Figure 6. NE5750/NE5751 Test Set-Up

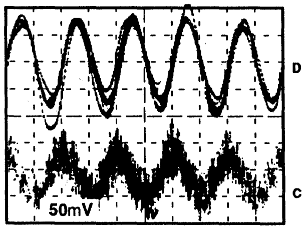


THERE IS GAIN IN THE PREAMP WITH A TONE PRESENT.

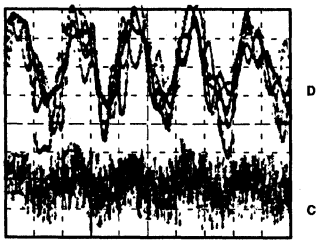


NO GAIN IS OBSERVED IN THE NOISE LEVEL.

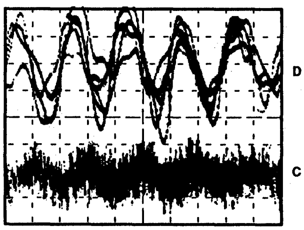
Figure 7.



WITH COMPANDING AND PRE-EMPHASIS/DE-EMPHASIS



NO COMPANDING, NO PRE-EMPHASIS/DE-EMPHASIS

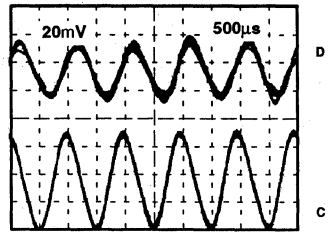


NO COMPANDING, PRE-EMPHASIS/DE-EMPHASIS ONLY

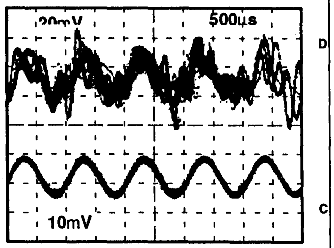
C = BOTTOM TRACE AUDIO SIGNAL BEFORE GOING TO THE RF TRANSMITTER

D = TOP TRACE FINAL SPEAKER OUTPUT

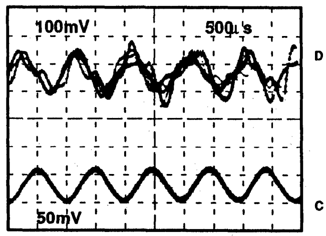
Figure 8. Audio Output with Baseband Channel Noise



WITH COMPANDING AND PRE-EMPHASIS/DE-EMPHASIS



NO COMPANDING, NO PRE-EMPHASIS/DE-EMPHASIS



NO COMPANDING, PRE-EMPHASIS/DE-EMPHASIS ONLY

C = BOTTOM TRACE AUDIO SIGNAL BEFORE GOING TO THE RF TRANSMITTER

D = TOP TRACE FINAL SPEAKER OUTPUT

Figure 9. Audio Output with a Noisy RF Channel

Figure	Description
7	No noise gain is observed at the output of the Tx channel because of the noise canceller circuit.
8	Shows why companding and emphasis are needed to improve the quality of the audio signal when BASEBAND NOISE is present in the system
9	Shows why companding and emphasis are needed to improve the quality of the audio signal when RF NOISE is present in the system.
10	Shows that the sensitivity and the signal-to-noise ratio of a receiver improved due to audio processing.

After studying these figures, a designer will have a graphical understanding of how the APROC processes a signal.

Figure 6 shows the test set-up using the APROC demo-board to simulate a real cellular phone call. Audio noise is added to the input of the microphone and RF noise is added to the receiver. The table for Figures 7-10 describes what the associated waveforms reveal when certain key stages of the APROC are activated or bypassed.

As seen from the following figures, there is a definite advantage in using the chip set in high performance communication systems.

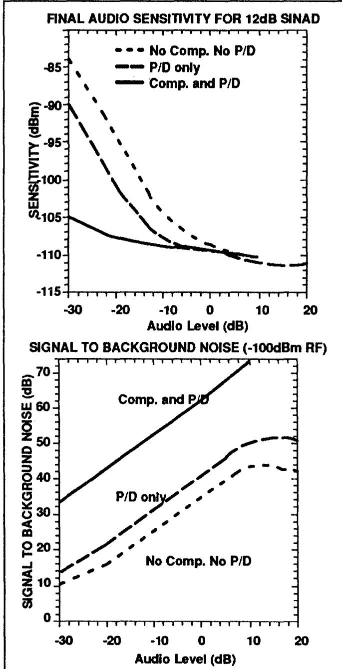


Figure 10.

II. NE5750

A CLOSER LOOK AT THE NE5750:

Referring to Figure 11, the NE5750 has seven main features which make this chip unique: preamp, noise canceller, VOX, compressor, expandor, buffer, and power amplifiers. (NOTE: All component labels in this section are referenced to Figure 11, unless otherwise indicated.)

Preamp:

The NE5750 provides a preamp with adjustable gain. This allows the designer to boost the low level audio signal coming out of the microphone. The microphone can be connected to Pin 1 through a DC blocking capacitor, C1 (see Figure 12). The input impedance at this Pin is 50kΩ.

The preamp gain of the NE5750 can be adjusted from 0dB to 40dB by an external resistor, R7, connected to Pin 2 through a capacitor C2. Below is a formula which allows the designer to determine the value of R7 for a certain value of gain.

If a designer wanted a preamp gain of 20dB, a 5kΩ resistor would be required (see Table 2).

$$R7 = \left[\frac{50,000}{10^{\left(\frac{X(dB)}{20}\right)} - 1}\right] - 500 \qquad (1)$$

"X" in dB

Table 2. Calculated R7 Values for Different Preamp Gains

X (dB)	R7
0	Leave Pin 2 open
5	64k
10	22k
15	10k
20	5.1k
25	2.5k
30	1.1k
35	405
40	Pin 2 AC grounded

Noise Canceller:

The output of the preamp is connected to the input of the noise canceller circuit which is internal to the device. The function of the noise canceller is to automatically provide a set gain of either 0dB when no signal is present, or 10dB when a signal is present. With this feature, background noise is minimized from transmission.

This automatic gain setting can only be implemented when the noise canceller circuitry is used in conjunction with the VOX circuitry. The threshold and attack and release time can be set externally. This will be described in more detail in the "VOX" section.

Although the noise canceller circuit is really designed to be used with the VOX circuitry, it can be implemented without it. The noise canceller circuit can be set up to provide either 0dB or 10dB of gain at all times (regardless of the presence of a signal). Table 3 shows how to achieve either gain settings when the VOX function is bypassed.

Table 3. Setting Up the Gain of the Noise Canceller

Pin	Gain of Noise Canceller	
No.	0dB	10dB
3	Ground	Ground
4	Ground	V_{CC}
7	10k to GND	Ground

The output of the noise canceller is accessible to the designer at Pin 24. C13 is used as a DC blocking capacitor.

VOX:

As mentioned earlier, the VOX circuitry works together with the noise canceller circuit. Pins 3, 4, 5, 6, and 7 all deal with the VOX's performance.

All of the resistor and capacitor values given in the NE5750 data sheet are chosen to meet AMPS/TACS specification for cellular radio. So any deviation from these values should be considered carefully if the application is in cellular radio.

Connected to Pin 3 is a resistor R2 and capacitor C15, as shown in Figure 13. These components set the gain of the VOX. The values here are for internal use only and have no direct relationship with the performance. So the values should be kept as shown. In some special applications, R2 may be adjusted such that the voltage on Pin 4 can be increased. By increasing this voltage, the voltage on Pin 7 can be set to a higher range (more details later).

Pin 4 has C3 and R1 connected to it which affects the attack and release time of the VOX circuit. In general the attack time should be faster than the release time.

The values given for C3 and R1 provide an approximate attack time of 12ms and release time of 120ms. These values should be kept as shown.

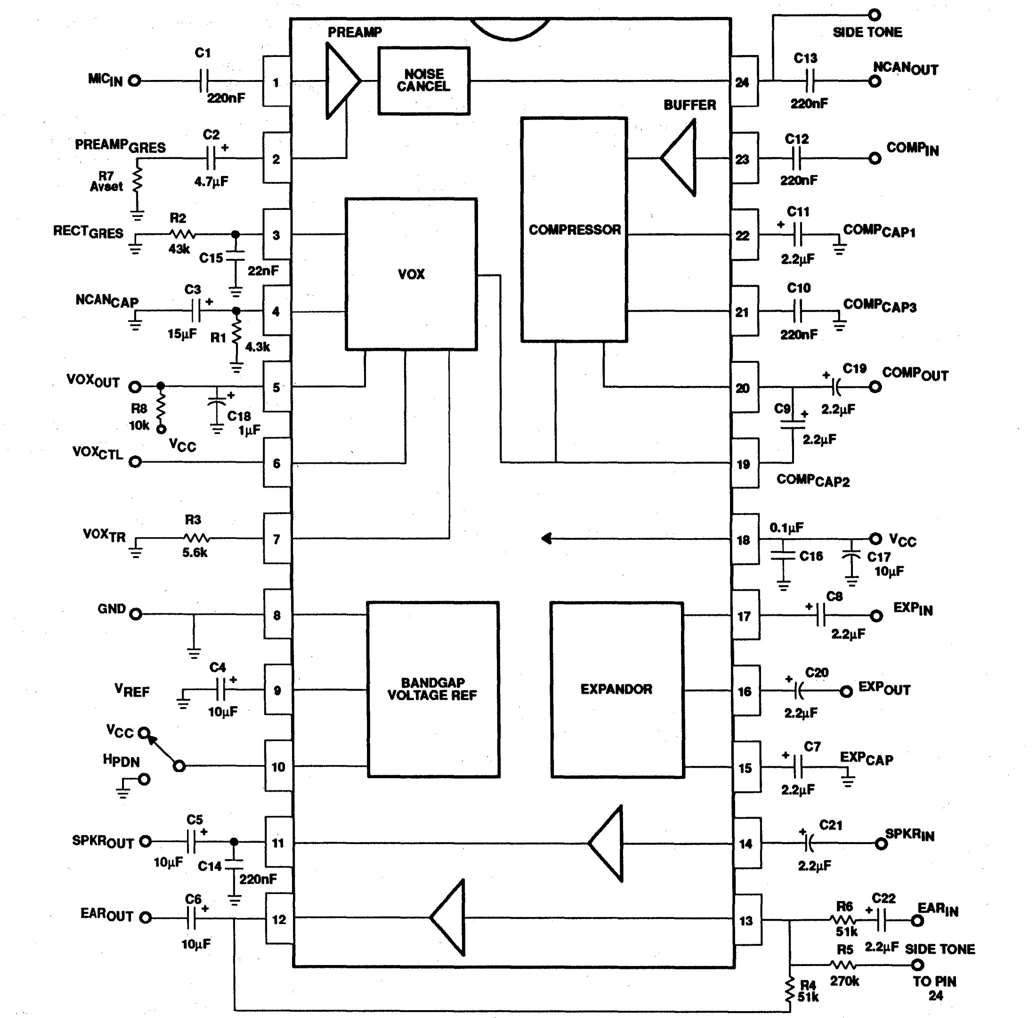
The timing of the VOX circuit is important because it controls the gain of the noise canceller, and can also turn the transmitter on and off.

- VOX_{OUT} and VOX_{CTRL}

By using VOX_{OUT} and VOX_{CTRL}, Pins 5 and 6 respectively, the NE5750 can control the status of the transmitter. The VOX_{OUT} Pin should have a 10kΩ pull-up resistor to V_{CC}. When probing Pin 5, a logic '1' or '0' will be read. The VOX_{CTRL} pin should have a logic '1' or '0' connected to it. Table 4 shows how Pins 5 and 6 can be used:

Having a logic '0' on Pin 6 is sufficient in most applications. When voice is present, the noise canceller kicks on while the VOXout Pin supplies a logic '1'; when voice is not present, VOXout Pin supplies a logic '0'. In a cordless phone application this logic level could be used to turn the transmitter on and off, thereby conserving power for any battery operated applications.

Supplying a logic '1' on Pin 6 would cause the transmitter to stay on regardless of any signal input to Pin 1. However, the functionality of the noise canceller will still be signal dependent.



NE5750 COMPONENT LIST

C1 DC blocking cap for Mic amp
C2 DC blocking cap for Mic gain
C3 used to set attack and release time of VOX
C4 V_{REF} filter capacitor
C5 DC blocking cap for speaker at Pin 11
C6 DC blocking cap for EAR_{OUT} pin
C7 sets attack and release time for expandor
C8 DC blocking cap for expandor's input
C9 AC bypassing for compressor
C10 passes AC to GND
C11 sets attack and release time of compressor
C12 DC blocking cap for compressor's input
C13 DC blocking cap
C14 low pass filtering for speaker output
C15 used for filtering, internal use only

R1 used to set release time of VOX
R2 set gain of VOX, but for internal use only effects voltage on Pin 4
R3 sets threshold level of VOX
R4 feedback resistor for ear amp
R5 sets gain of ear amp for side tone signals
R6 sets gain of ear amp for baseband signals
R7 sets microphone preamp gain

ADDED FOR NE5750 DEMO-BOARD

R8 pull-up resistor to get logic levels out

C16 bypass capacitor
C17 bypass capacitor
C18 passes AC to GND (low pass)
C19 DC blocking cap for compandor out
C20 DC blocking cap for expandor out
C21 DC blocking cap for speaker in
C22 DC blocking cap for ear in

Figure 11. NE/SA5750 Application Demo-Board

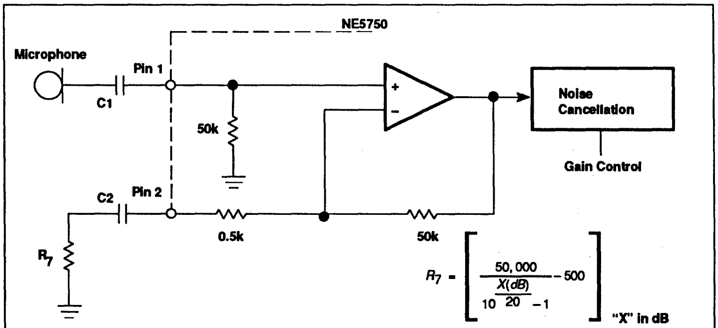


Figure 12. Setting Microphone Preamplifier Gain

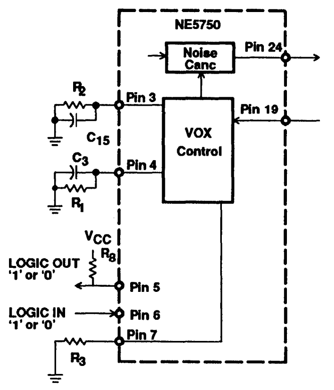


Figure 13. VOX Circuit

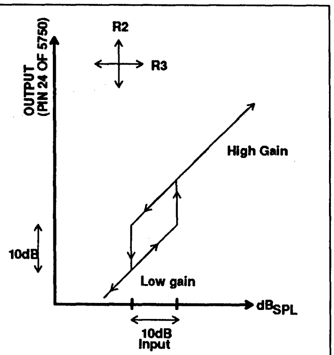


Figure 14.

This condition is mainly used if the battery consumption is not a problem. Such a condition would be for any car cellular radios.

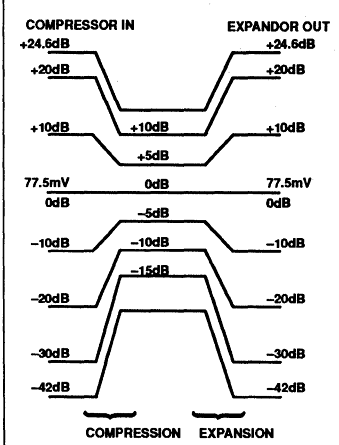


Figure 15. Compandor Dynamic Range

- setting the threshold
R3 at Pin 7 is used to set the threshold of the VOX. Setting the threshold determines the voltage level input at which the noise canceller and VOX will activate. Formula 4 shows how to calculate the VOX's threshold.

$$VOX_{THRESH}\,(mV) = 50\mu A \cdot R3\ (K\Omega) \quad (4)$$

Where $R3 > 3k\Omega$)

If R3 = 5.6k, the measured voltage at Pin 7 should be approximately 280mV.

The way to adjust the VOX is to first determine what signal level is desired at Pin 1 to activate the VOX noise canceller circuits. Once that level is applied to Pin 1, connect a voltmeter to Pin 4. The voltage level measured here should be plugged into formula 4 to determine R3.

As mentioned earlier, the voltage at Pin 4 can be increased by R2. But one should only deviate from the R2 value if the voltage at Pin 7 cannot come down. In most cases, setting R2 to 43kΩ and setting Pin 7 to the voltage at Pin 4 is sufficient.

Figure 14 shows graphically how R3 and R2 affect the location of the "box". The "box" is always 10dB, which is due to the noise canceller circuit.

EXAMPLE I : Set the VOX threshold such that it "kicks on" when $30mV_{P-P}$ is applied to Pin 1 of the NE5750 with a preamp gain of 0dB.

Step 1: Make sure:

a. Pin 7 is left open.

b. The VOX attack and recovery components are in place at Pin 4.

c. R2 and C15 are connected to Pin 3.

d. If using the NE5750 alone, be sure to connect the preamp output (Pin 24) to the compressor input (Pin 23) with a DC blocking cap.

e. The preamp gain is already set (in this instance the preamp gain is 0dB).

f. Make sure that the compressor's components are also connected; compressor's attack time has to be functional

Step 2: Apply a constant 1kHz sinewave signal to Pin 1 with the desired threshold. In this case, $30mV_{P-P}$.

Step 3: Measure the DC voltage on Pin 4; V4=260mV

Step 4: Calculate R3:

R3 = V4(V) /(50μA)
= 0.260/50μA
= 5.2k

let's use a 5.3kΩ

Step 5: Connect R3 to Pin 7 and verify that VOX "kicks on" at the desired threshold.

- This set-up has the VOX kicking on at $30mV_{P-P}$ and kicking off at $11mV_{P-P}$.

Referring to the above example, if a preamp gain of 10dB was chosen before setting the threshold, the threshold will also change. So it is vital that the preamp gain be set before setting the VOX threshold.

Table 4. VOX Truth Table

Inputs		Outputs	
Voice (Pin 1)	**VOX_{CTRL} (Pin 6 of NE5750)**	**Noise Canceller Gain**	**VOX_{OUT}**
Not Present	logic '0'	0dB	logic '0'
Present	logic '0'	10dB	logic '1'
Not Present	logic '1'	0dB	logic '1'
Present	logic '1'	10dB	logic '1'

NOTE: To apply a logic '0' on Pin 6 by the I^2C evaluation program, be sure that the VOX_{EN} is high, and low for a logic '1' on Pin 6. If the NE5750 is used alone, be sure that the output of the noise canceller is AC coupled to the input of the compressor. Also, make sure that all of the components for the compressor are connected.

Compandor:

- compressor

The compressor input at Pin 23 requires an external DC blocking capacitor (C12). The input impedance is roughly 50kΩ. Unlike the older compandors, this input can be directly driven from CMOS circuits (e.g. NE5751).

The gain from the preamp should be adjusted such that there is enough signal getting to the compandor. However, one must be careful not to overdrive the inputs. Additionally, do not forget the extra 10dB gain from the noise canceller (assuming it is being used).

Figure 15 shows the typical dynamic range of the compandor. The maximum input signal that the compressor can handle is $3.72V_{P-P}$ or 24.6dB. The minimum input is approximately $1.74mV_{P-P}$ or -42dB. Knowing that the 0dB point of the compandor is at $77.5mV_{RMS}$, one can easily convert from volts to dB. Formula 5 shows the conversion from V_{RMS} to dB.

$$X(dB) = 20\log\left(\frac{V_{RMS}}{77.5(mV_{RMS})}\right) \qquad (5)$$

where
X = value in dB
V = voltage in RMS.

Usually it is easier to work in voltages, but in this case it is better to work in dB. If one knows the input signal in dB, the designer can predict the output of the compressor (also in dB) to be half or two times the input. For instance, if the input were 10dB, we could expect the output to be 5dB. On the other hand, if the input was -20dB, we could expect the output to be -10dB.

Capacitor C11 on Pin 22 controls both the attack and release time of the compressor. The attack time may be calculated by Formula 6.

$$Attack\ time = R \cdot C \qquad (6)$$

where R=10kΩ

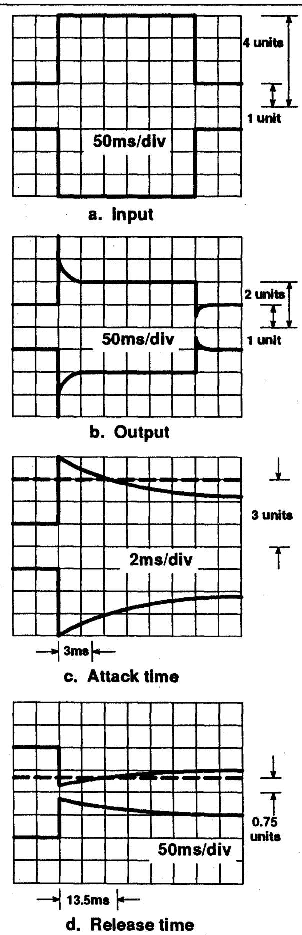


Figure 16. Compressor Dynamic Response

NOTE: The release time is roughly 4 times slower than the attack time by design.

$$Release\ time = 4 \cdot Attack\ time$$

Capacitor C10 on Pin 21 is used for AC bypassing. Capacitor C9 on Pins 19 and 20 is also for AC bypassing.

- expandor

The expandor input at Pin 17 requires an external DC blocking capacitor (C8). The input impedance is around 2.5kΩ. Referring to Figure 15, the input range of the expandor is from $19.53mV_{P-P}$ (-21dB) to $903mV_{P-P}$ (12.3dB). The output range is from $1.74mV_{P-P}$ (-42dB) to $3.72V_{P-P}$ (24.6dB).

Capacitor C7 is used to set the attack and release time of the expandor. Formula 6 can also be used to determine those values.

- how to measure attack and recovery time

In this section we will briefly describe the bench procedure for measuring attack and recovery times. Additional information can be found in AN174 in the "Attack and Decay Time" section.

Let's assume that C_{RECT} =2µF and $R_{INTERNAL}$=10k. Since T=R · C, then T=20ms. If we wanted a different "RC" time constant we would change the C_{RECT} value ($R_{INTERNAL}$ is a fixed value).

Using these component values let's measure the attack and recovery times to see if the CCITT and EIA specifications are met.

measurement at compressor:

EIA Specifications

Attack time is the time required for the transmitter deviation to settle to a value equal to "1.5" times the final steady state value, for a 12dB step up.

Release time is the time required for the transmitter deviation to settle to a value equal to "0.75" times the final steady state value, for a 12dB step down.

The compressor must have a nominal attack time of 3ms and a nominal recovery time of 13.5ms as defined by CCITT.

Bench Procedure for Compressor Test

1. Apply a 1kHz sinewave signal at 0dB to the input of the compressor (0dB is defined where the compandor passes the input signal through to the output — unity gain level for the APROC is $77.5mV_{RMS}$.
2. Modulate the 1kHz input signal with a 1Hz-2Hz square wave.
3. Connect an oscilloscope probe to the input of the compressor and adjust both the modulation and oscilloscope (uncalibrate it) so that a 1:4 ratio is achieved on the screen of the oscilloscope (see Figure 16a).

Adjusting for a 1:4 ratio produces a 0dB to 12dB step at the input. The unit "1" represents the 0dB input level and the unit "4" represents the 12dB input level (20log (4/1) =12dB).

4. Connect another oscilloscope probe to the output of the compressor and observe the waveform (see Figure 16b). The "final steady-state" value for the attack time is "2" units while the release time is "1" unit. These output values are expected because, for a compressor, the ratio is 2:1 unless the input is at 0dB, in which case, the ratio is 1:1.
5. Now to measure the attack and release time, capture the beginning and end of the output waveform where the changes occur (see Figure 16c and Figure 16d).

To measure the attack time (T_A):

-According to the EIA specifications:

$$T_A = 1.5 \cdot \textit{Final Steady-State Value}$$

-therefore

$$T_A = 1.5 \cdot 2 \textit{ units} = 3 \textit{ units}$$

-Measure the time it takes for the output to drop to the 3rd unit. According to Figure 16c, our attack time is 3ms. This indeed meets CCITT specs..

To measure the release time (T_R):

-According to the EIA specifications:

$$T_R = 0.75 \cdot \textit{Final Steady-State Value}$$

-therefore

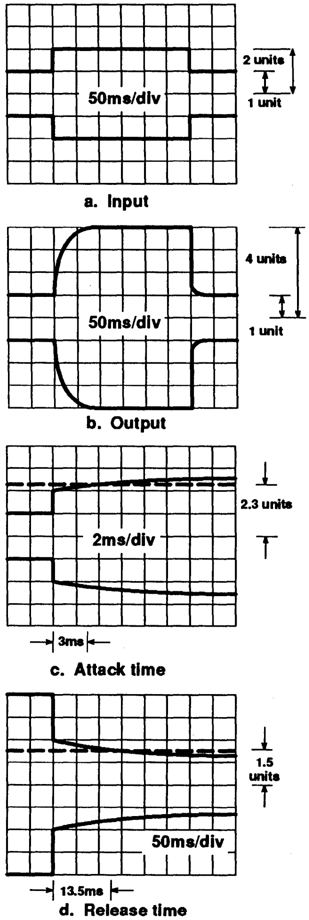


Figure 17. Expandor Dynamic Response

$$T_A = 0.75 \cdot 1 \textit{ unit} = 0.75 \textit{ units}$$

-Measure the amount of time it takes for the output to rise up to 0.75 units. According to Figure 16d, our release time is 13ms. Again the CCITT spec. is met.

measurement at expandor:
EIA Specifications

Attack time is the time required for the transmitter deviation to settle to a value equal to "0.57" times the final steady state value, for a 6dB step up.

Release time is the time required for the transmitter deviation to settle to a value equal to "1.5" times the final steady state value, for a 6dB step down.

The expandor must have a nominal attack time of 3ms and a nominal recovery time of 13.5ms as defined by CCITT.

Bench Procedure for Expandor Test

1. Apply a 1kHz sinewave signal at 0dB to the input of the expandor (0dB is defined where the compandor passes the input signal through to the output — unity gain level).
2. Modulate the 1kHz input signal with a 1Hz-2Hz square wave.
3. Connect an oscilloscope probe to the input of the expandor and adjust both the modulation and oscilloscope (uncalibrate it) so that a 1:2 ratio is achieved on the screen of the oscilloscope (see Figure 17a).

Adjusting for a 1:2 ratio produces a 0dB to 6dB step at the input. The unit "1" represents the 0dB input level and the unit "2" represents the 6dB input level (20log(2/1)=6dB).

4. Connect another oscilloscope probe to the output of the expandor and observe the waveform (see Figure 17b). The "final steady-state" value for the attack time is "4" units while the release time is "1" unit.
5. These output values are expected because for an expandor the ratio is 1:2 unless the input is at 0dB, in which case, the ratio is 1:1.
6. Now to measure the attack and release time, capture the beginning and end of the output waveform where the changes occur (see Figure 17c and Figure 17d).

To measure the attack time (T_A):

-According to the EIA specifications:

$$T_A = 0.57 \cdot \textit{Final Steady-State Value}$$

-therefore

$$T_A = 0.57 \cdot 4 \textit{ units} = 2.28 \textit{ units}$$

-Measure the time it takes for the output to reach 2.28 units. According to Figure 17c, our attack time is 3ms. This indeed meets CCITT specs..

To measure the release time (T_R):

-According to the EIA specs.:

$$T_R = 1.5 \cdot \textit{Final Steady-State Value}$$

-therefore

$$T_A = 1.5 \cdot 1 \textit{ unit} = 1.5 \textit{ units}$$

-Measure the amount of time it takes for the output to drop to 1.5 units. According to Figure 17d, our release time is 13ms. Again the CCITT specification is met.

These results show that the release time is about 4 times slower than the attack time. All Signetics compandors are internally set up this way so that once the attack time is set by C_{RECT}, the release time is automatically set.

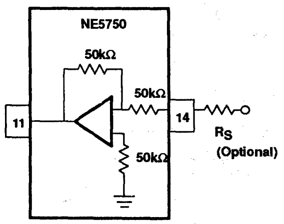
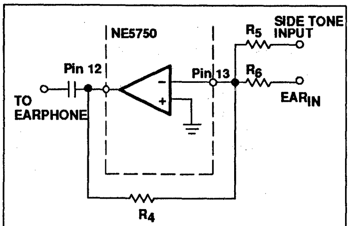


Figure 18. Speaker Amplifier for the NE5750



Earphone Gain $A_V = -\frac{R_4}{R_6}$

Sidetone Gain $A_V = -\frac{R_4}{R_5}$

Figure 19. Setting Gain for Earphone Amplifier

Special Note: In AN174, Figures 10 and 11 show the X-axis as being in fractions of the time constant. The way to clarify this is by multiplying 20ms to these numbers to convert them to the measured attack and recovery time. The 20ms comes from the "RC" time constant which can be varied by varying the C_{RECT} value. But again, once these numbers are converted, one can see that these figures show similar results as ours in the lab.

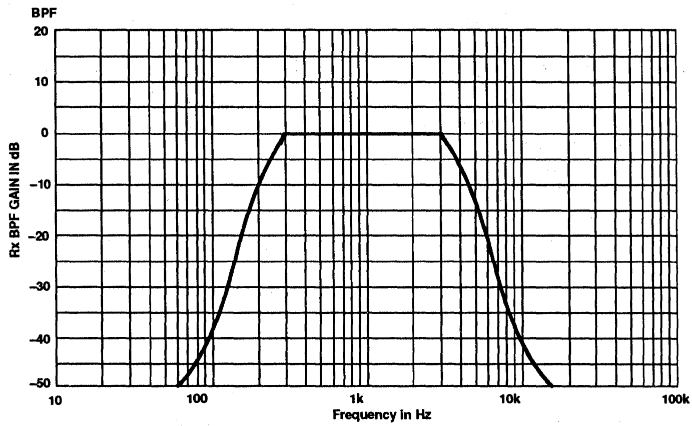


Figure 20. NE5751 Tx Bandpass Filter

Amplifier Section:

-speaker amplifier

The speaker amplifier is a unity gain amplifier with a high input impedance. Located on Pin 11, the output of the amplifier, are two capacitors C5 and C16. Capacitor C5 is for DC blocking, while C16 is for high pass filtering.

Since the amplifier's input is not directly accessible to the designer (see Figure 18), it is impossible to exceed a gain of one. However, if external attenuation is desired, use formula 7 to determine the series resistor that would connect to Pin 14.

$$A_V = \frac{-R_F}{R_{IN}} = \frac{-50k}{(50k + R_S)} \qquad (7)$$

In most cases, the attenuation takes place in the NE5751 before the signal gets to the amplifier. Therefore, adding external attenuation is rare.

-earphone amplifier:

Unlike the speaker amplifier, the gain of the earphone amplifier can be set by external resistors. In this case, the required output and input are directly accessible. Figure 19 is a diagram of the earphone amplifier with the required equations. Sidetone gain can also be implemented with an external resistor.

How To Power Down

"Power down" or "power up" can be implemented by Pin 10 of the NE5750. When Pin 10 is connected to V_{CC}, the chip is in the "power up" state. In this mode, the chip is fully functional. However, when Pin 10 is connected to ground, the chip is in the "power down" state where the current consumption drops dramatically (CMOS or TTL levels will suffice). In this mode, the chip is not expected to be functional, but all of the capacitors remain charged so that "power up" can occur quickly. Having this capability allows the system to conserve battery power.

III. NE5751

A CLOSER LOOK AT THE NE5751:

Figure 24 shows a block diagram of the NE5751. Key functions for this chip include a TX bandpass filter, TX pre-emphasis filter, TX low pass filter, summing amplifier, RX bandpass filter, RX de-emphasis, programmable DTMF generator, programmable attenuator, and an I²C bus interface.

-TX path

The input and output of the TX bandpass filter are located on Pins 3 and 4, respectively. The 4th-order Chebyshev bandpass filter is designed to pass 300 to 3000Hz (voice band). (see Figure 20).

The input to the pre-emphasis circuit is accessible through Pin 5. This filter shapes the spectrum with a +6dB per octave slope in the pass band (see Figure 21). The output is then connected internally to a low pass filter and limiter circuit (see Figure 22). The functions of the last two filters guarantee that the 12kHz maximum frequency deviation for cellular radio is not violated.

The output of the limiter filter (Pin 23) and the output of the programmable DTMF generator (Pin 22) can be connected to the input of the summing amplifier. The gain of this amplifier can be controlled with external resistors. In Figure 24, the resistors are all 51kΩ which creates a unity gain configuration. The output of the amp is then connected to the transmitter.

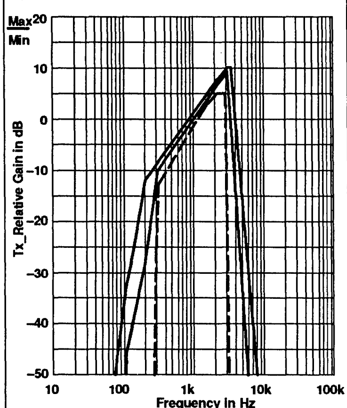


Figure 21. Pre-emphasis Curve

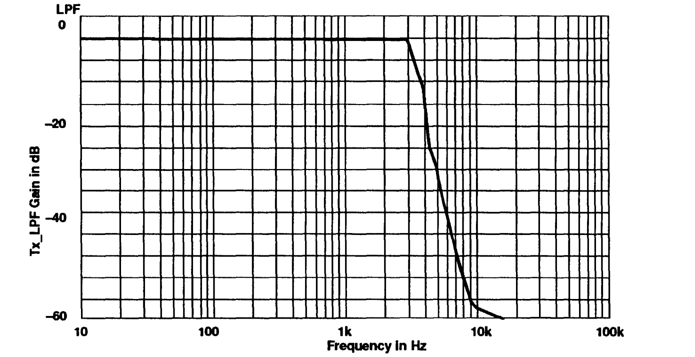


Figure 22. NE5751 Tx Low Pass Filter

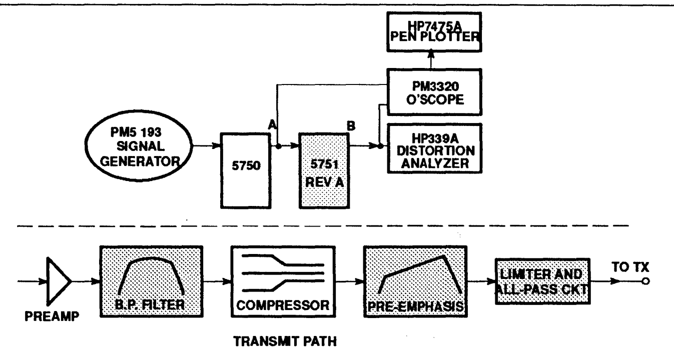


Figure 23. Test Set-up and Tx Path of Signal

The Limiter and All-pass Circuit:
An important aspect of the AMPS specification is concerned with the 12kHz maximum frequency deviation. The output of the APPROC should be less than 12kHz regardless of the input signal. Figure 23 shows the equipment used for the test measurements and how the signal was processed. A 1kHz signal was applied to the input of the demo-board until a 5% distorted signal was measured at the limiter output. This waveform's peak-to-peak voltage was recorded as a reference, then, at various chosen frequencies, the input of the demo-board was overdriven so we could record the distorted peak-to-peak waveform. (See Figure 26)

Formula 8 was used to calculate maximum frequency deviation from the waveforms shown in Figure 26.

$$\text{Max Freq Dev with All-Pass Ckt} = \frac{BW_F}{BW_R} \cdot 8kHz \quad (8)$$

where

BW_F = the bottom waveform's peak-to-peak voltage from one of the observed Figures.

BW_R = the bottom waveform's peak-to-peak voltage from the reference Figure.

Table 5. Maximum Frequency Deviation Results for the 12kHz Test

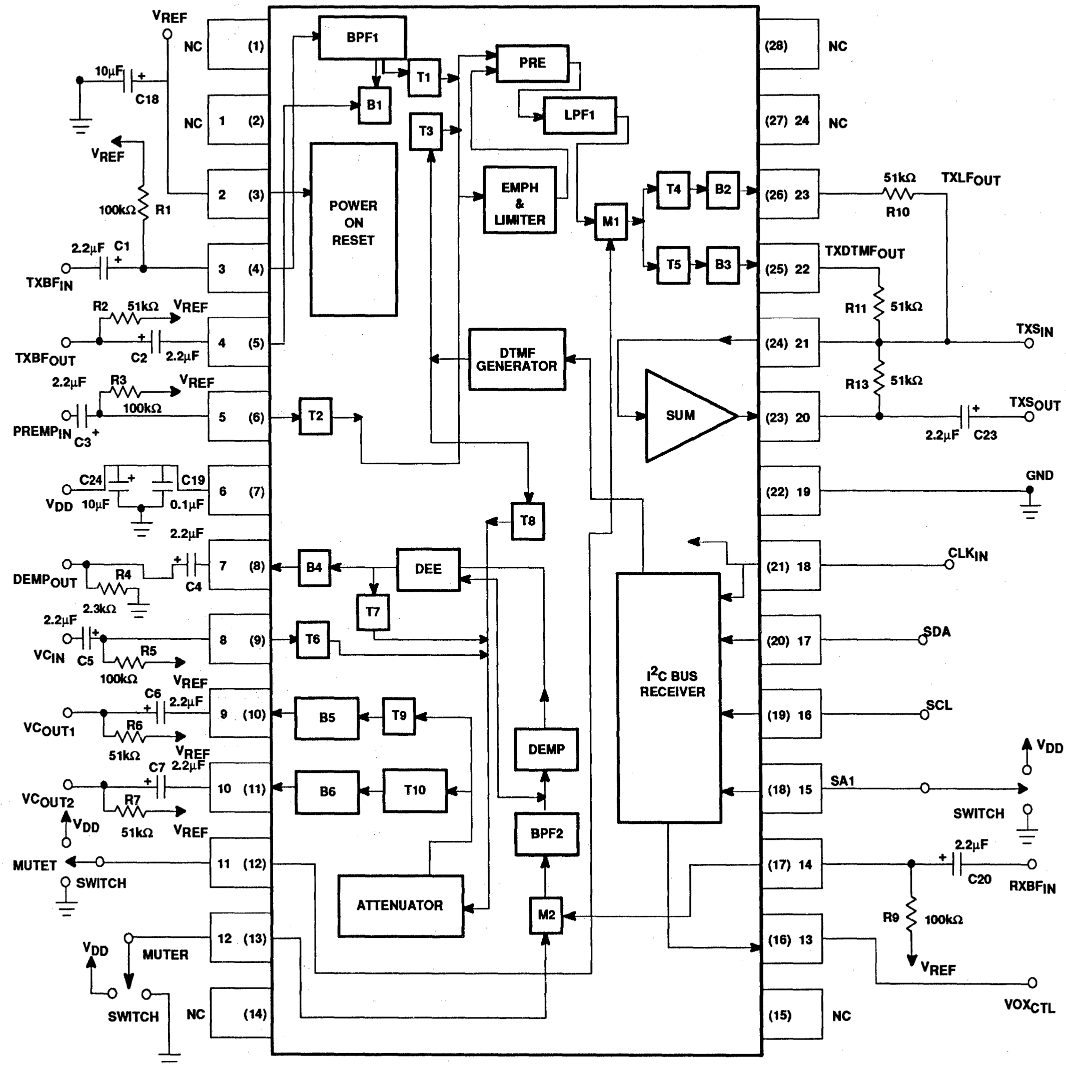
Frequency (Hz)	With All-Pass (kHz)
300	5.91
500	9.04
800	10.09
1000	10.09
1200	10.09
2000	11.13
3000	10.78

Table 5 reveals the calculated results for maximum frequency deviation over the voice band. The test results show that the NE5750 and NE5751 will meet the 12kHz AMPS specification. If a customer needs further assurance that the 12kHz specification will be satisfied, an Automatic Level Control (ALC) circuit can be placed after the summing amplifier output of the NE5751. Keep in mind, though, that this ALC will only provide attenuation.

- RX path
For the receive side of the NE5751, the signal goes to the input of the RX bandpass filter (Pin 13) which has the same characteristics as the TX bandpass filter. The only difference is that this filter also has a stop-band notch filter at 6kHz to reject the Supervisory Audio Tone (SAT) signals as seen in Figure 27.

The output is then internally connected to the de-emphasis filter. This filter provides a -6dB/octave slope over the passband to compensate for the pre-emphasis function (see Figure 28).

The attenuator can be digitally programmed by I^2C. The input signal level can be attenuated 16 steps in 2dB increments. This



R10 Input resistor for summing amp out can be used to set gain of signal input
R11 Resistor for summing amp out can be used to set gain of DTMF feedback
R13 Resistor for sum amp can be used to set gain of all the inputs Used to bias up

R1, R2, R3, R4, R5, R6, R7, R9 } Used to bias respective pins to 2.5V by connecting the other end of the resistor to the V_{REF} pin without loading down the V_{REF} source

C18 Used to AC GND V_{REF} pin
C19 Power supply bypass cap
C20 DC blocking cap for Rec input
C23 DC blocking cap for sum amp out
C24 Power supply bypass cap

C1, C2, C3, C4, C5, C6, C7 } Provides DC blocking for the respective pins

Figure 24. NE/SA5751 Test and Application Circuit

Table 6. Maximum Frequency Deviation Results for the 12kHz Test

Number Dialed	High Freq.	Low Freq.	DTMF HI	DTMF LO
1	1209	697	A5	8F
2	1336	697	96	8F
3	1477	697	87	8F
4	1209	770	A5	82
5	1336	770	96	82
6	1477	770	87	82
7	1209	852	A5	75
8	1336	852	96	75
9	1447	852	87	75
0	1336	941	96	6A
*	1209	941	A5	6A
#	1477	941	87	6A

gives a range from 0dB to -30dB. The attenuator error is shown in Figure 29.

I^2C Bus Interface:

The NE5751 is controlled by a serial control bus comprised of a clock input, serial bus address, serial clock line, and serial data line.

A designer who is unfamiliar with I^2C can refer to the following documents for assistance: 1) I^2C Bus Specification and 2) Signetics AN168. Both of these documents can be found in the 1989 Signetics Linear Data Manual or the 1991 RF Communications Handbook.

The clock input requires an input frequency of 1.2MHz. This frequency is vital for the operation of the part because it effects the DTMF generator and the 3dB point of all the switch capacitor filters.

The output of the DTMF generator can be determined by Formula 8.

$$Low\ Freq = \frac{\frac{Clock\ Input\ Freq}{12}}{LD} \qquad (8a)$$

where LD is the value of the register This translates to: DTMF LO REG = 100000/ LO REG (Hz)

$$High\ Freq = \frac{\frac{Clock\ Input\ Freq}{6}}{HD} \qquad (8b)$$

where HD is the value of the register

This translates to: DTMF HI REG = 200000/ HI REG (Hz)

Table 6 can be used to help the designer program the DTMF generator.

There are a few key points that should not be overlooked when programming the NE5751. The control registers consist of the

1. Register map
2. Signal path register
3. Volume control and test register
4. High tone DTMF register
5. Low tone DTMF register

To generate a single tone from the DTMF generator, use the appropriate registers (high or low DTMF) and load the other one with a '0', '1', or '2' to silence it.

The order of these registers is important. If the programmer wanted to turn down the volume, he/she would have to re-program the register map, signal path, and then give the new data to the volume control and test register.

IV. APROC DEMO-BOARD

About the APROC demo-board:

The NE5750/51 demo-board layout can be seen in Figure 30, Figure 31, and Figure 32. It incorporates the use of DIP packages. However, an SO adapter could be made to test the SO APROC chips.

A separate board is used to interface the APROC demo-board with the computer's parallel port. This converter utilizes the 74LS05 as a buffer scheme.

An I^2C program for the APROC is provided so that a designer can easily program and evaluate the chip set. This eliminates the need to write an evaluation program. However, it does not eliminate the need for a final system program.

The evaluation program has a graphic display that shows the transmit and receive path of the APROC on the terminal, as seen in Figure 33. By selecting a function, one can toggle the space bar on the key board to turn on or off any key features. The designer could also type in the codes for any registers to control the functions.

Figure 25 shows how the interface board and the demo-board can be used in conjunction with a computer. Once everything is connected properly, one can make his own evaluations on the chip set.

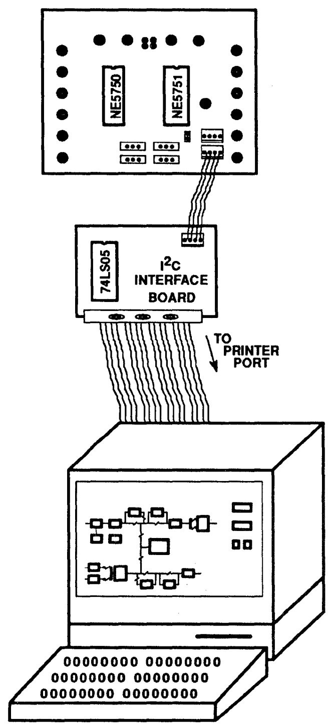


Figure 25. Interfacing the APROC Demo-board with the I^2C Evaluation Program

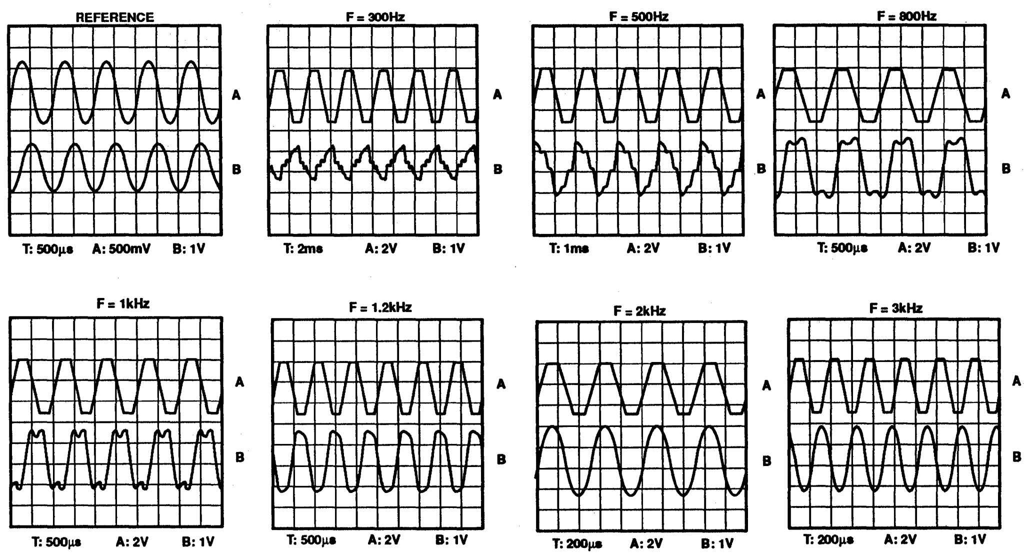


Figure 26. Results From the 12kHz Maximum Frequency Deviation Test

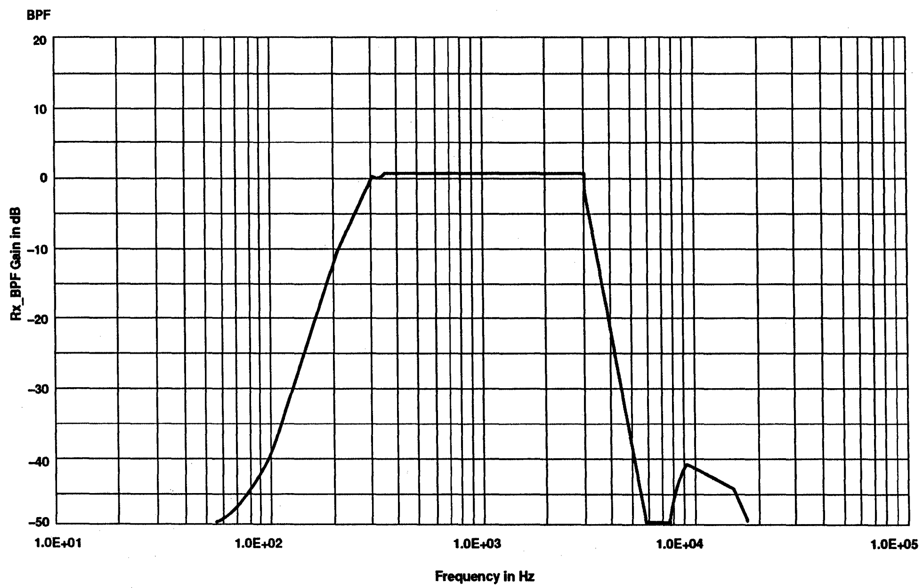


Figure 27. NE5751 Rx Bandpass Filter

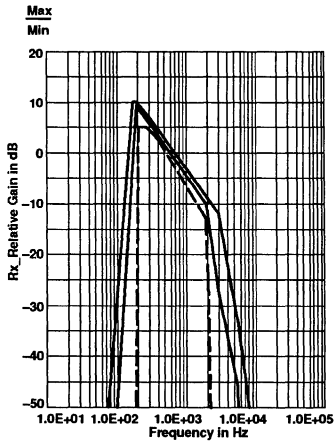


Figure 28. NE5751 Rx De-emphasis

How to Power Down on the NE5750/51 Demo-Board:

In general, power down mode is a condition where a system has just enough power to "stay alive" and, therefore, is not expected to be fully operational. When called upon, the system can quickly get out of this mode and into the power up mode and be ready to perform its functions. This fast reaction time is possible because all of the capacitors have maintained their charges. This is because power was not cut-off completely. The power down function reduces overall current consumption when the system is not fully operational, and is especially helpful when the system is operating from a battery powered source.

There are three power down conditions when we refer to to the NE5750/51 demo-board. They are listed and described as follows:

1. NE5750 Power Down

Purpose:

- to reduce current consumption

- to maintain all DC voltages on the device pin to keep the capacitors charged

How To:

- use hardware switch on demo-board which forces Pin 10 to ground

- or use a CMOS logic output into Pin 10

Benefits:

- reduces current consumption while maintaining readiness

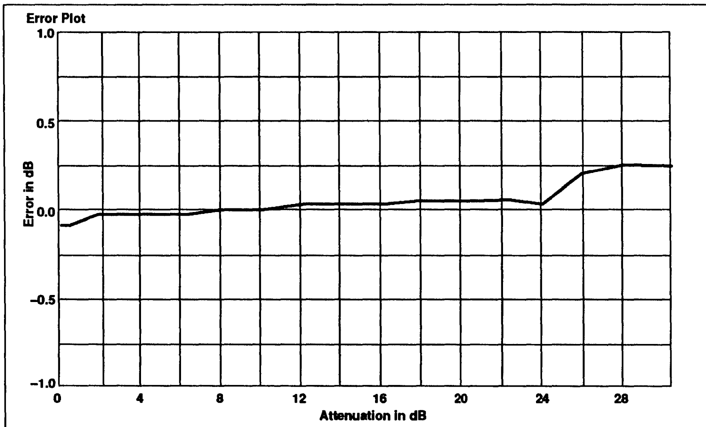


Figure 29. NE5751 Attenuation Error

- current drops from 8.4mA to 1.8mA (typically)

Mode of Operation:

- Everything is semi-functional, although performance is not, and will not be, guaranteed

2. NE5751 Power Down

Purpose:

- to reduce current consumption

- to maintain all DC voltages on the device Pin to keep the capacitors charged up

- to open all voice paths so that no signals will flow

How To:

- program the I²C bus under the condition that all registers are set to zero

Benefits:

- all the registers are always at zero when powering up from the power down mode

- reduces current consumption while maintaining readiness

- current drops from 2.7mA to 1.1mA (typically)

Mode of Operation:

- Everything is semi-functional, although performance is not, and will not be, guaranteed

3. Chip-Set Power Down

Definition:

-the NE5750 and NE5751 demo-board is in the power down mode when:

1. The transmitter and receiver are muted on the NE5751
2. The NE5751 is powered down (all registers are set to zero), and
3. The NE5750 is powered down

How to Power Down the Chip-Set Properly (1st Choice):
Please follow this recommended sequence;

1. Mute both the transmitter and receiver on the NE5751.
2. Program the following registers as follows:

Signal Path Register: 00000000

Volume Control Register: 00000000

High DTMF Register: 00

Low DTMF Register: 00

3. Power Down the NE5750.

How to Simulate the Power Down on the Chip-Set (2nd choice)*
Please follow this recommended sequence;

1. Program the following registers as follows:

Signal Path Register: 00010000

Volume Control Register: 01100000

High DTMF Register: 00

Low DTMF Register: 00

2. Power Down the NE5750

*NOTE: this method is only used when the NE5751 mute switches are not accessible, by design.

Comments

1. Muting both the transmitter and receiver on the NE5751 can be done by the two "hardware" switches on the demo-board (forces Pins 11 and 12 to V_{CC}).
2. Powering down the NE5751 can be done by programming the correct assigned register to zero (For more details, consult the NE5751 data sheet).
3. Powering down the NE5750 can be done by the "hardware" switch on the demo-board (forces Pin 10 to ground).
4. When coming out of the power down mode to the power up mode, reverse the procedure given above.
5. If functions are activated while in the power down mode before power up occurs, the "chip-set power down" is no longer valid.
6. We recommend that a 2.2µF capacitor be placed between the NE5751 de-emphasis output to the NE5750 expandor input. The purpose of this capacitor is to block any DC offset that might occur between the two chips while in the power down mode. If this capacitor is not used, an abnormal reaction might occur where white noise is generated.

V. NE5750 DEMO-BOARD

Figure 34 shows the layout for the NE5750 demo-board. This board can be used to evaluate the NE5750, alone, and allows the designer to do extensive testing without having to worry about other external factors. Again, this board makes use of dip packages only. However, a SO adapter can be made to implement the SO version of the NE5750.

VI. QUESTION AND ANSWER SECTION

NE5750 and NE5751 (APROC):

Q: Is it OK to connect the V_{REF} pins together for the NE5750 and NE5751? My circuit seems to be working properly.

A: No, this is not a good idea. Although both V_{REF}s are at 2.5V ($V_{REF} = V_{CC}/2$), there is no guarantee that they will be exactly equal over temperature. One of the V_{REF}s might influence the function of the other chip which, in turn, might have a detrimental effect on the performance of the chips.

Q: Will the APROC chip set work for TACS, NMT or NAMPS specifications as it does for AMPS specification?

A: The APROC was designed to meet AMPS and TACS specifications, however, as it stands now, the chip set will also meet the NAMPs requirements. The chip set will not work for NMT specifications.

Q: In the power down mode, is it OK to program the DTMF registers before powering up?

A: No. This will break the rules of powering down. All the registers are set to zero in this mode. Please review the section on powering down the chip set properly.

NE5750:

Q: Even though I have all the required external components in place on Pins 1,2,3,4,5,6 and 7, my VOX circuit does not work. What is wrong?

A: The VOX circuit is not a trivial connection. Even though all the components are connected, be sure that the output of the NE5750 noise canceller is AC coupled to the input of the compressor to complete the VOX loop. This holds true if the NE5750 is used alone. However, if the NE5751 is used make sure that the signal is fed from the band-pass filter to the input of the NE5750 compressor input. For further advice, please read example 1 in the "setting the threshold" section of this application note.

Q: Do I have to use I^2C if I use the NE5750 alone?

A: No, the NE5750 can be used by itself and does not require the use of I^2C.

Q: Can I speed up the release time of the compressor?

A: Not directly. The release time is dependent on the attack time setting. Once the attack time is set by C11 on Pin 22 of the NE5750, the release time is set internally to be four times slower. So to increase the release time requires that the attack time be increased. One should be careful because setting the attack time too fast could cause more distortion on the output.

Q: The NE5750 compressor input impedance is around 50kΩ. Why is this impedance higher than that of others in your family of compandors?

A: The NE5750 was designed to be compatible with the NE5751. The NE5750 compressor input was modified to accept CMOS driven outputs like the NE5751. This internal modification eliminates the need for an external buffer.

NE5751:

Q: Can I change the filter characteristics?

A: Yes, by changing the master clock input frequency the 3dB points will be effected. For example, if F=1.2MHz, then BPF1=3kHz. Now, if F=600kHz, BPF1=1.5kHz; and if F=2.4MHz, BPF1=6kHz. This type of application is not recommended because the part was not designed to be used this way and, therefore, performance will not be guaranteed. Additionally, the DTMF generator will be off in frequency from the calculated values because of the assumption of a 1.2MHz clock, and the I^2C interface will not be functional.

Q: Besides I^2C, can I communicate to the NE5751 with another type of operating scheme?

A: Yes, by bit banging. Instead of using the I^2C hardware one can supply the clock and data defined in the I^2C protocol software. But this takes up a lot of memory, therefore, it is preferable to implement the I^2C hardware.

Q: The limiter seems to work when I overdrive the input with a strong signal. However, when I try to pass DTMF tones, the limiter's level varies when switches T3/T5 and T4 are set to different settings Why is this? Isn't the output supposed to stay constant regardless of the input being overdriven or passing DTMF tones?

A: Yes, the limiter should hold the output constant when an overdriven signal is applied, but only when the switches are used properly. When passing DTMF tones, T1, T2, and T4 should be left open, while T3/T5 are closed. The voice path should be disconnected when DTMF tones are being passed. Hence, T3/T5 should be left open when DTMF is not used.

Q: When I program a DTMF tone, it only stays on for 96ms. How can I make it stay on longer?

A: The way to make it stay on longer than 96ms is to re-load the DTMF registers (re-program the DTMF registers before 96ms expires).

REFERENCES:

"Audio Processing for Cellular Radio or High Performance Transceivers", proceedings of R.F. Expo 1989, A. Fotowat, S. Navid, L. Engh, pp. 195-203.

"Designing Cellular Radios with the Philips Components-Signetics Cellular Chip Set", Cellular Radio Chip Set Design Manual, Feb. 25, 1990.

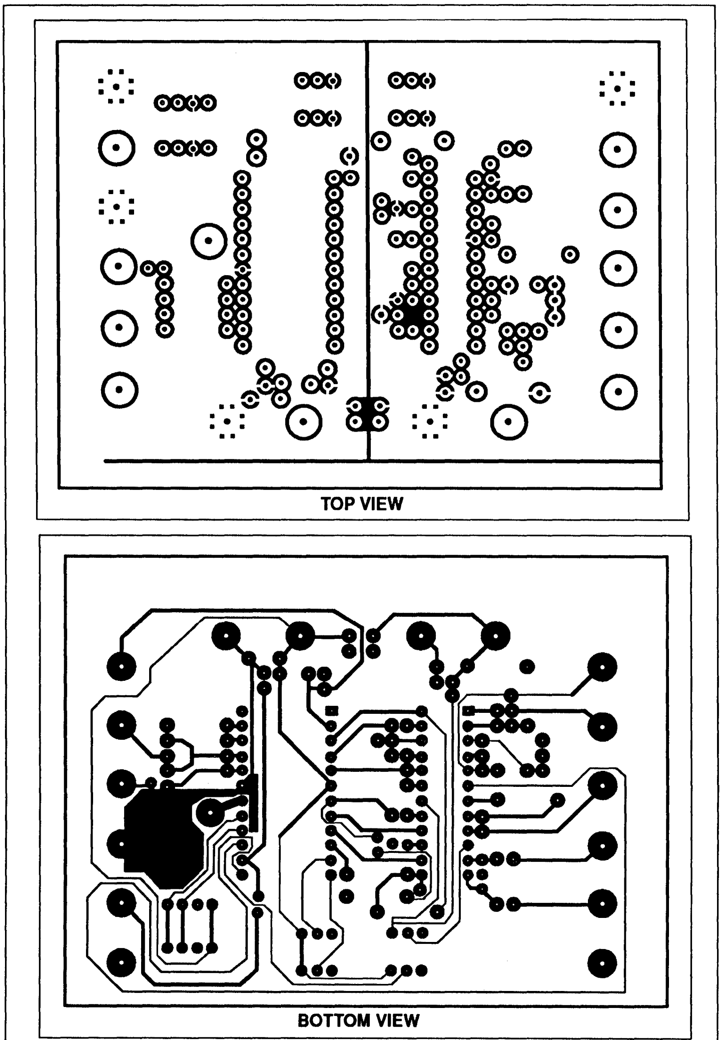


Figure 30. Layout of the APROC Demo-board

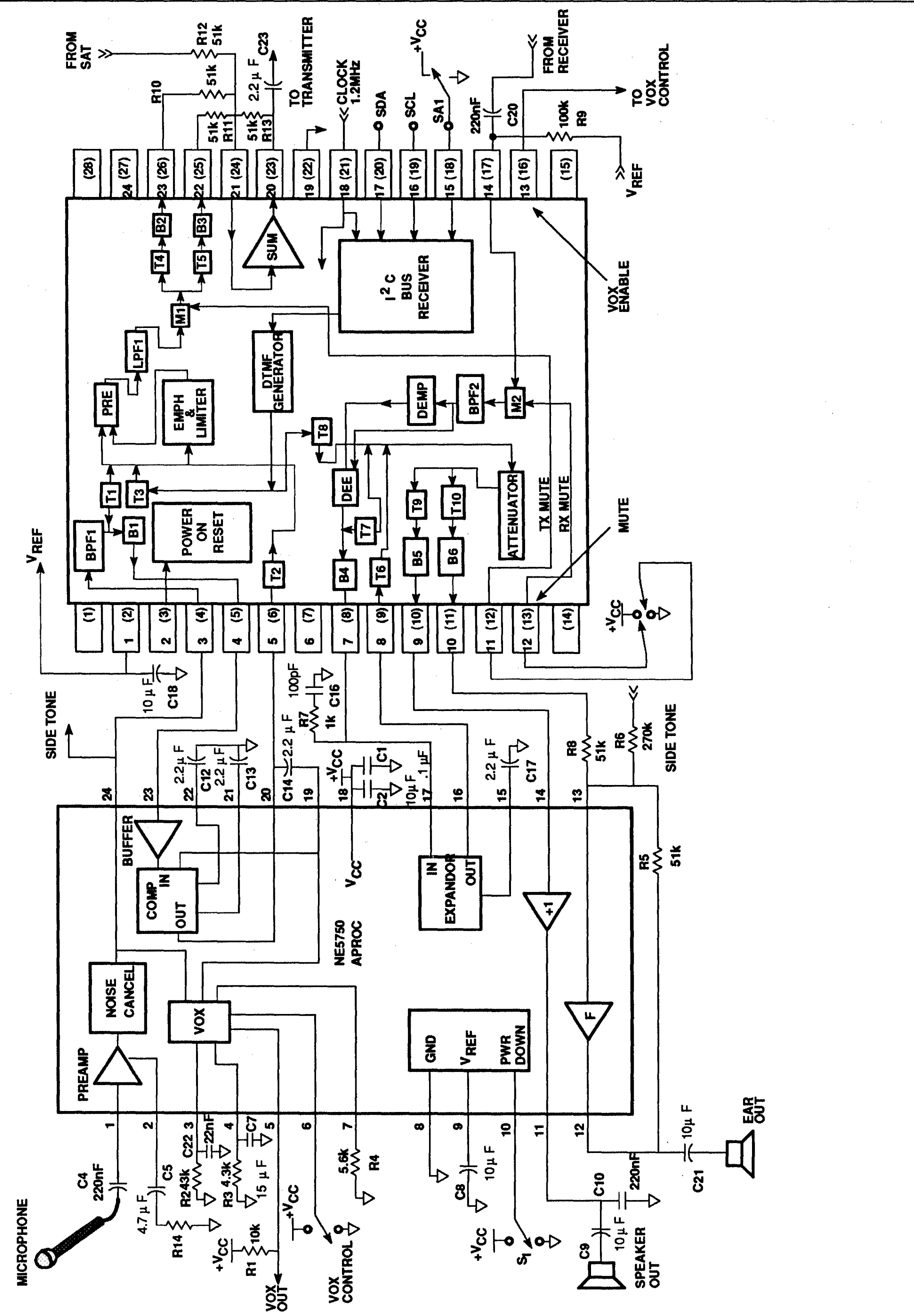
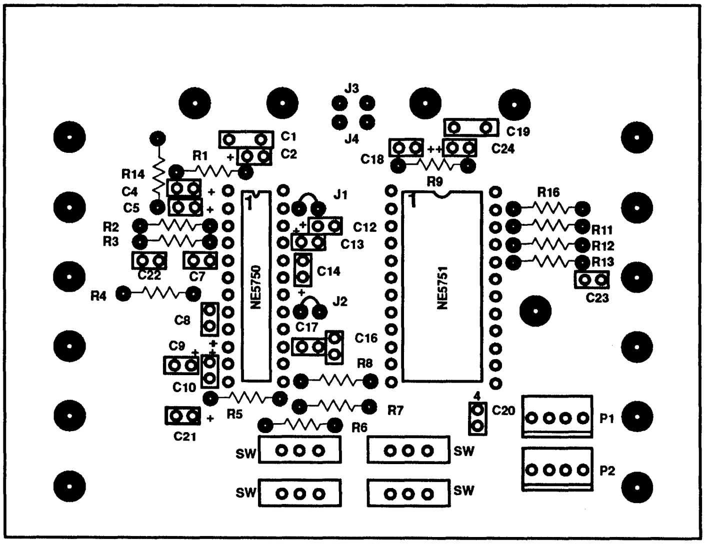


Figure 31. NE5750, NE5751 Cellular Radio Application Circuit



Component Values

C1	0.1µF	R1	10kΩ
C2	10µF	R2	43kΩ
C4	0.22µF	R3	4.3kΩ
C5	4.7µF	R4	5.6kΩ
C7	15µF	R5	51kΩ
C8	10µF	R6	270kΩ
C9	10µF	R7	1kΩ
C10	0.22µF	R8	51kΩ
C12	2.2µF	R9	100kΩ
C13	2.2µF	R10	51kΩ
C14	2.2µF	R11	51kΩ
C16	100pF	R12	51kΩ
C17	2.2µF	R13	51kΩ
C18	10µF	R14	OPTIONAL
C19	.1µF	J1	JUMPER
C20	0.22µF	J2	JUMPER
C21	10µF	IC	NE5750 NARROW 24-PIN SOCKET
C22	.022µF	IC	NE5751 WIDE 24-PIN SOCKET
C23	2.2µF	P1	4 PRONG HEADER
C24	10µF	P2	4 PRONG HEADER
		SW	MINI SLIDE SWITCH

Component Functions

R1	Pull-up resistor for VOX_{OUT} logic levels
R2	Sets gain of VOX, but for internal use only effects voltage on Pin 4
R3	Used to set release time of VOX
R4	Sets threshold level of VOX
R5	Feedback resistor for ear amplifier
R6	Sets gain of ear amplifier for the side tone input
R7	Used in conjunction with C10 to filter out unwanted noise. Optional
R8	Sets gain of ear amplifier
R9	Used to bias up Pin 14 to 2.5V by connecting V_{THRESH} to V_{REF} without loading down V_{REF} source
R10	Input resistor for summing amp out. Can be used to set gain of signal
R11	Input resistor for summing amp out. Can be used to set the gain of the DTMF
R12	Input resistor for summing amp. Can be used to set gain of the side tone input
R13	Feedback resistor for summing amp. Can be used to set gain of all the inputs
R14	Used to set gain of the preamp of NE5750 (OPTIONAL)
J1	JUMPER
J2	JUMPER

C1	Bypass cap for VCC of NE5750
C2	Bypass cap for VCC of NE5750
C4	DC blocking cap for mic input
C5	DC blocking cap for mic gain setting resistor
C7	Used to set attack a release time of VOX
C8	Used to AC ground the V_{REF} pin (5750)
C9	DC blocking cap for speaker out
C10	filter for speaker out
C12	Sets attack and release time of compressor
C13	Used to AC short the DC path for the compressor
C14	Provides AC path to the VOX circuitry
C16	OPTIONAL. Basically to filter out noise
C17	Sets attack and release time for the expandor
C18	Used to AC ground V_{REF} pin (5751)
C19	Bypass cap for V_{CC} of NE5751
C20	DC blocking cap for receiver input
C21	DC blocking cap for ear amplifier output
C22	Sets gain of VOX, internal use only
C23	DC blocking cap for summing amp out
C24	Bypass cap for V_{CC} of NE5751

NOTE: The board is constructed in such a way as to allow a single power supply to power the chip set, or for each chip to be powered by a separate power supply. Using separate power supplies will permit monitoring of current consumption of each part when Jumpers 3 and 4 are removed.

Figure 32. Parts and Function List of APROC Demo-board

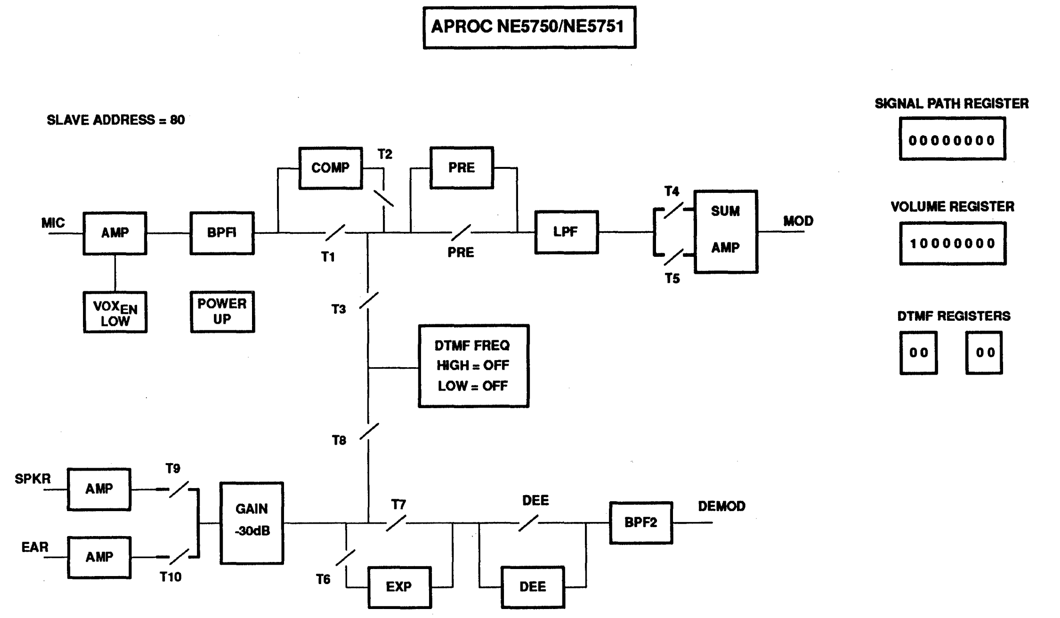


Figure 33. Graphical Display of the I²C Evaluation Program

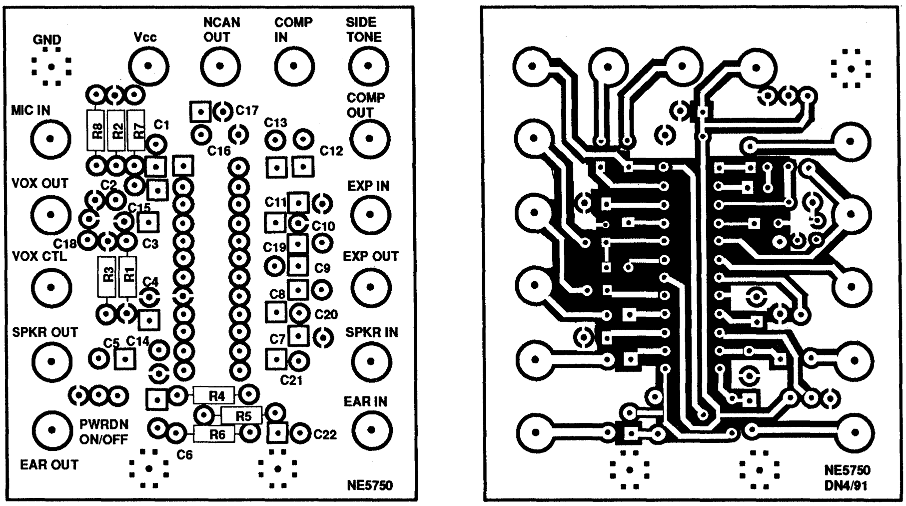


Figure 34. NE5750 Demo-board Layout

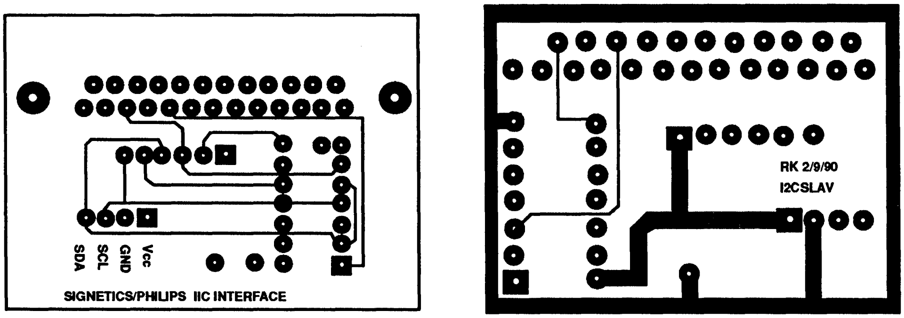

SDA
SCL
GND
Vcc
SIGNETICS/PHILIPS IIC INTERFACE
RK 2/9/90
I2CSLAV

Figure 35.

Paging decoder PCA5000AT

GENERAL DESCRIPTION

The PCA5000AT is a fully integrated decoder for the CCIR Radio Paging Code number 1 (POCSAG-code). It supports two basic modes of operation:

Alert-Only-Pager. This is a stand-alone mode in which the PCA5000AT scans inputs from three external switches that relate to the states ON, OFF and SILENT. Only a few external components are required to build an Alert-Only pager.

Display-Pager. In this mode, received calls and messages are transferred via the IC's serial communication interface to an external microcontroller. A built-in voltage converter can double the supply voltage output and perform level shifting on the interface signals.

Call-alert cadences are generated when valid calls and messages are received, and status cadences to indicate the present state of the decoder are generated following a status interrogation. An on-chip 5 x 9-bit static RAM with battery back-up is provided for programming two user-addresses and for special functions. Synchronization of the input data stream is achieved by the built-in ACCESS algorithm which allows data to be synchronized without preamble detection and minimizes battery power consumption by receiver-enable control. One of three error correction algorithms is applied to received code words to optimize the call success rate.

The PCA5000AT is fabricated in SACMOS-technology to ensure low power consumption at low supply voltages. Typical applications are alert-only pagers, numeric/alphanumeric display pagers, cellular radio and data/telemetry decoders.

Features

- Wide operating supply voltage range (1.7 to 6.0 V)
- Very low supply current (15 μA typ.)
- Decodes CCIR Radio Paging Code number 1
- Data rate: 512 bits/s
- Powerful 'ACCESS' synchronisation algorithm
- Supports two user addresses
- Four cadences per user address
- Silent call storage, up to four different calls
- Interfaces directly to the UAA2033 digital paging receiver
- Directly drives a 2 kHz bleeper
- High-level alert facility requires only a single external transistor
- Receiver-enable control for battery economy
- On-chip static RAM, non-volatile with battery back-up
- On-chip voltage converter
- Level-shifted microcontroller interface
- Battery-low alert
- Out-of-range indication (optional)

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A.)

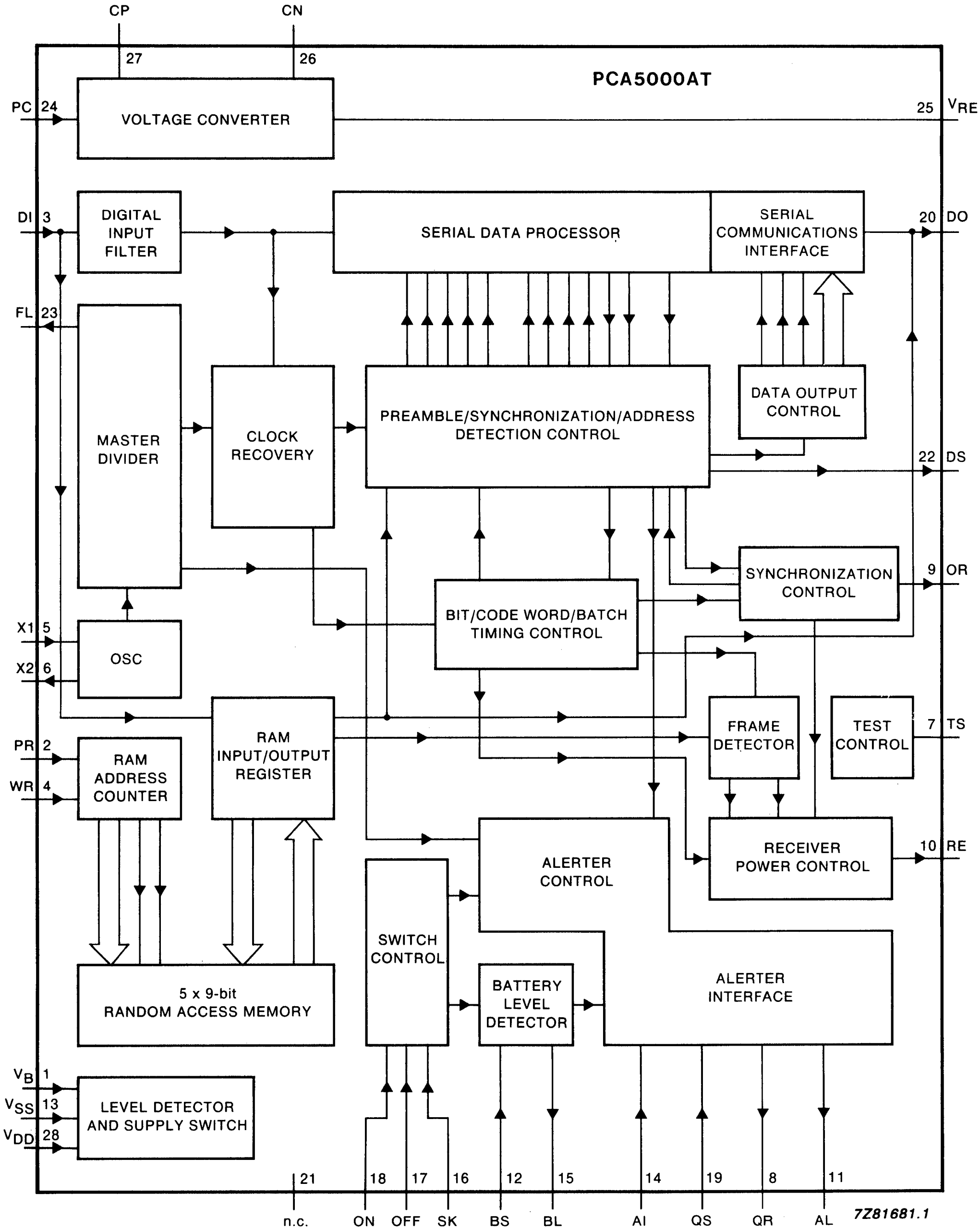


Fig. 1 Block diagram.

Paging decoder PCA5000AT

PINNING

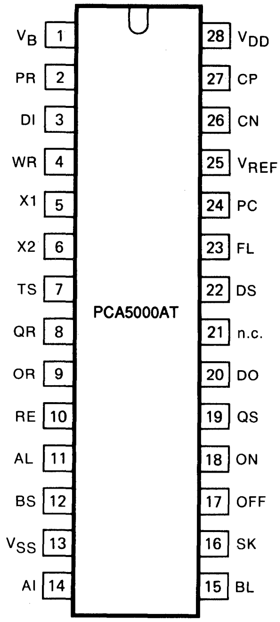


Fig. 2 Pinning diagram.

pin	mnemonic	description
1	V_B	RAM back-up negative supply voltage
2	PR	programming enable input
3	DI	serial data input
4	WR	programming WRITE input
5	X1	oscillator input
6	X2	oscillator output
7	TS	test mode enable input
8	QR	alert high-level output/vibrator output
9	OR	out-of-range output
10	RE	receiver enable output
11	AL	alert low-level output
12	BS	battery sense input
13	V_{SS}	negative supply voltage
14	AI	alarm input
15	BL	battery-low output
16	SK	silent key/mute input
17	OFF	off key/reset input
18	ON	on key/on-off input
19	QS	vibrator enable input
20	DO	received data output
21	n.c.	not connected
22	DS	received data strobe output
23	FL	frequency reference output
24	PC	power control input to voltage converter
25	V_{REF}	microcontroller interface negative reference voltage
26	CN	voltage converter external capacitor (negative)
27	CP	voltage converter external capacitor (positive)
28	V_{DD}	positive supply voltage (common)

FUNCTIONAL DESCRIPTION

Operating modes

The decoder has two basic operating modes; alert-only-pager and display-pager. There is also a programming mode in which the contents of the internal RAM are programmed or verified. The RAM holds two user-addresses and special function bits.

Alert-Only-Pager

No external microcontroller is required in this mode.

Tone-alert cadences are generated when valid calls are received. Four different alert cadences are available and are called by combinations of the function bits. The voltage doubler is disabled in this mode.

The decoder continually scans the inputs ON, OFF and SK from the external switches ON, OFF and SILENT that determine the internal operating status. Operating one of the switches first causes the cadence of the existing internal status to be generated and then, after 1.5 s switch operation, generation of a cadence to indicate the new internal status of the decoder.

Display-Pager

In this mode the decoder receives calls/messages and directs those addressed to one of the two stored user addresses to an external microcontroller for post-processing and display. Tone-alert cadences are generated when valid calls are received.

The decoder provides a doubled supply voltage output to the microcontroller and associated hardware, and the interface signals are level-shifted to allow direct coupling to the microcontroller.

The internal state of the decoder is determined by the logic levels on the static inputs ON and SK.

Internal states

If the decoder is in one of the two operating modes, its internal status is always one of the following:

OFF state. This is the power-saving inactive state in which no decoding takes place and the paging receiver is disabled. Scanning of the ON, OFF and SK inputs is maintained to allow state-changes to be effected.

ON state. This is the normal active state of the decoder. Received calls and messages are compared with the two user addresses stored in the RAM. When the validity of incoming calls is confirmed, appropriate cadences are generated and data is shifted out via the serial microcontroller interface.

SILENT state. This is the same as the ON state except that alert cadences are not generated following valid calls. Instead, if programmed as an alert-only pager, the decoder stores up to four different calls. The appropriate alert cadences are generated after the decoder has been returned to the ON-state. However, special silent override calls will cause generation of alert cadences.

POCSAG code structure

A transmission using the CCIR Radio Paging Code No. 1 (POCSAG code) is structured according to the following rules (see Fig. 3)

The transmission is started by sending a preamble which is a sequence of at least 576 continually alternating bits (01010101 . . .). The preamble precedes a number of batch blocks. The transmission is terminated after the last batch.

Every batch comprises a synchronisation code word with a fixed 32-bit pattern followed by eight frames (numbered 0 to 7). Only complete batches are transmitted.

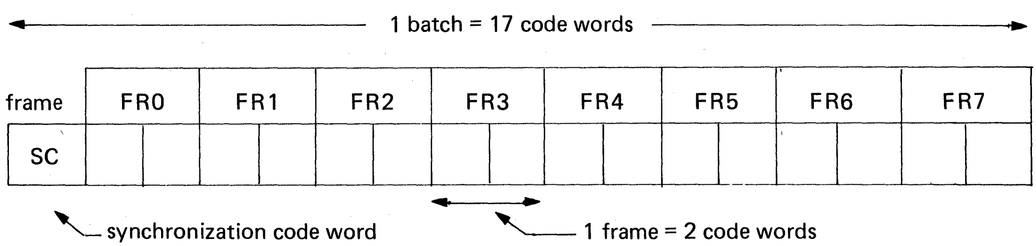
A frame comprises two code words, each 32 bits long. A code word is either an address, message or an idle code word. Idle code words are transmitted to fill empty batches or to separate messages.

An address code word is coded as shown in Fig. 3; 18 bits of the 21-bit user address are coded in the code word and are protected against transmission errors by a CRC check word (bits 22 to 31). The other three bits of the user address are coded in the number of the frame in which the address code word is transmitted. Two function bits (bits 20 and 21) allow distinction between four different calls to one user address.

A message code word contains 20 bits of any information, these are also protected by a check word.

preamble	1st batch	2nd batch	subsequent batches →

a) Call structure



b) Batch structure

bit	1	2 to 19	20	21	22 to 31	32
	0	user address	FC	FC	parity check	

c) Address code word structure (FC are function code bits)

bit	1	2 to 21	22 to 31	32
	1	message	parity check	

d) Message code word structure

Fig. 3 POCSAG coding structure.

FUNCTIONAL DESCRIPTION (continued)

Decoding

The POCSAG-coded input data is first noise-filtered by a digital filter. A sampling clock, synchronous to the 512 bits/s data rate, is derived from the filtered data.

Synchronization is performed on the POCSAG code structure using the ACCESS algorithm, which is a five-stage state mechanism.

The decoder first searches the data stream for preamble or synchronization code word patterns. Before synchronism can be achieved, the decoder must ascertain that synchronization code words are correctly positioned at the beginning of each batch. When the correct structure is detected, the decoder switches to the 'receive mode'. (The receiver enable output (RE) is active before input data is required.) Error correction algorithms are applied to the data.
If synchronization is lost (i.e. no synchronization code word found at the beginning of the next batch) the decoder enters a two-step recovery mechanism. In the first step, over the next 15 batches, the decoder attempts to resynchronize by bit-wise shifting its frame window. A 'carrier off' state is entered in the second step, in this the data stream is tested convolutionally for a preamble or synchronization code word at every effective bit position within a continuous stream of at least 17 batches. When synchronization is regained, the decoder returns to the 'receive mode'.

In the 'receive mode', the input data stream is sampled at the frame position pointed to by the RAM program and the sampled code words are error-corrected. If they are address code words, they are compared with the two user addresses from the RAM. If the result of this comparison is 'true', the following actions take place:

- a store is set for a call-alert cadence. The cadence will relate to the combination of the function bits in the accepted code word but will not be generated until the call has been terminated;
- the receiver enable output (RE) is held active so that reception of the call can continue. This condition remains until
  - another address code word or an IDLE instruction is received
  - the error-correction algorithm fails to generate a code word
  - synchronisation is lost;
- message code words attached to the validated address code word are transferred via the serial communication interface to the external microcontroller.

Programming

The on-chip RAM is organized in five 9-bit words (Fig. 4). It is used to store two user addresses (receiver identification codes) and six programmed special function bits. A lithium back-up battery maintains data retention when the main power supply is removed.

	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
word 0	A08	A07	A06	A05	A04	A03	A02	A01	A00
word 1	A17	A16	A15	A14	A13	A12	A11	A10	A09
word 2	B08	B07	B06	B05	B04	B03	B02	B01	B00
word 3	B17	B16	B15	B14	B13	B12	B11	B10	B09
word 4	FR2	FR1	FR0	SP6	SP5	SP4	SP3	SP2	SP1

where:

AXX are 18 bits of user address 'A'
BXX are 18 bits of user address 'B'
FR2 to FR0 are frame number bits common to both addresses 'A' and 'B'
SP6 to SP1 are special function bits.

Fig. 4 RAM organization.

A user address in POCSAG code comprises 21 bits, three of which are coded in the frame number. In the PCA5000AT the frame number is common to both user addresses.

The special function bits are programmable to select from the following:

bit SP1: 0 alert-only-pager mode; silent override enabled on address 'B'
1 display-pager mode

SP2: 0 enable voltage converter (SP1 = 1)
1 disable voltage converter (SP1 = 1); cadence 1 also for FC = 11

SP3: 0 1-bit error-correction on message code words
1 4-bit burst error-correction on message code words on address 'B' (FC = 00 or 11)

SP4: free for user-application

SP5: 0 silent override enabled on address 'B' (FC = 01 or 10)
1 silent override enabled on address 'B' (FC = 00 or 11)

SP6: 0 silent override disabled on address 'A' (FC = 10)
1 silent override enabled on address 'A' (FC = 10)

The programming mode is entered by holding input PR at V_{DD} during power-on; exit from the programming mode is made by removing the main power supply. The back-up battery must remain connected to the PCA5000AT to keep the RAM contents when the main power supply is removed. During programming, inputs ON, OFF and SK must not all be '1' at the same time.

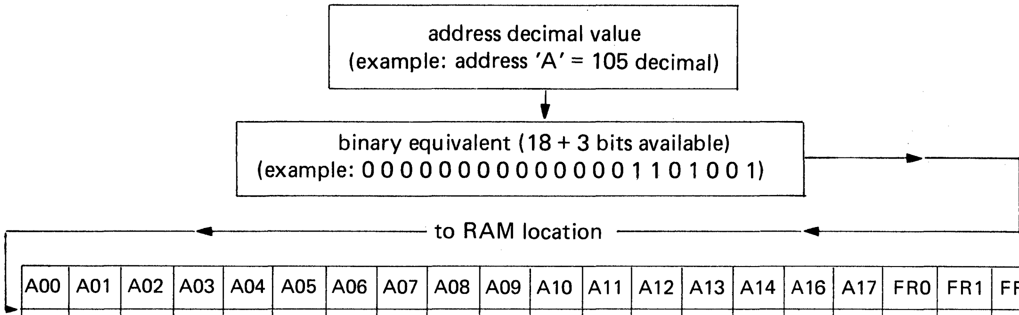
Programming of the RAM and verifying its contents is performed in a sequence starting with word 0, bit 0 and progressing through each of the five words in turn. Input and output is a serial operation; X1 is the shift clock input and DI, DO are respectively the data input and output.

During the RAM programming operation, a negative-going pulse first on WR and then on PR copies the 9 bits just shifted in into the RAM and switches to the next word (see Fig. 10).

During the RAM verify operation, reading the first word is triggered by a negative-going pulse on PR, which also switches to the next word in the sequence after 9 bits have been read (see Fig. 11).

Exit from the programming mode should be made after programming or verification of the RAM contents has been performed on all five words.

FUNCTIONAL DESCRIPTION (continued)



A00	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A16	A17	FR0	FR1	FR2
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1

Fig. 5 Example of bit conversion in user address programming.

Generation of output signals

Alerter interface

The alerter interface provides for the acoustic signalling of calls received (Fig. 8) and of changes of pager status (Fig. 9).

When valid calls are received and the pager is in the ON state, the decoder generates 2 kHz squarewave output signals to produce tone alert cadences via a magnetic or piezoceramic 2 kHz bleeper. The cadence signals differ in modulation according to the two function bits FC in the address code word (Fig. 6b). The PCA5000AT supports two levels of alerter loudness: during the first four seconds, cadences are generated at low intensity (output AL active, output QR inactive); during the following twelve seconds, the intensity is increased (outputs AL and QR both active).

The alert tone generation is automatically terminated after sixteen seconds. Alert cadences are also terminated by an ON, OFF or SILENT input when in alert-only-pager mode, or by pulsing the status/reset input in display-pager mode.

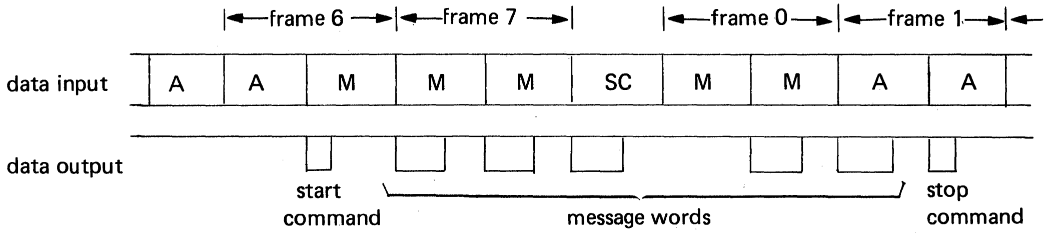
If the call is a message with subsequent message code words, alert cadence generation begins after the message has been terminated.

The alerter generates cadences to indicate the present internal status when interrogated and, when the main supply is low, gives a battery-low indicator output and generates an alarm tone.

Serial communication interface

This interface facilitates communication with an external microcontroller. Data is transmitted serially in the format shown in Fig. 6.

After receiving a valid address code word, transmission commences by sending a start command. The start command contains function data from the RAM, user address called (A or B) and function control bits FC from the address code word. The transmission continues with message words that contain the data from the received message code words. The end of a message transfer is marked by the sending of a stop command or another start command. In a stop command, bit 2 indicates that the call was successfully terminated.



a) Message format

bit	0	1	2	3	4	5	6	7
	0	1	SP3	SP6	SP5	user address A or B	address bit 20 (FC)	address bit 21 (FC)

b) Start command format

bit	0	1	2	3	4 to 23
	1	1	1	1	message code word bits 2 to 21 as received

c) Message word format

bit	0	1	2	3	4	5	6	7
	0	0	successful termination	$\overline{QS}$ input	SP4	SP2	not used	not used

d) Stop command format

Fig. 6 Serial communication interface.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
V_{DD} is referred to as 0 V (ground)

parameter	symbol	min.	max.	unit
Supply voltage	$V_{SS} = V_{13\text{-}28}$	+ 0.5	−7.0	V
RAM back-up supply voltage	V_B	V_{SS} + 0.8	−6.0	V
Input voltage on pins ON, OFF, SK, AI, PC, FL, BL, DS, DO	V_I	0.8	V_{REF}−0.8	V
Input voltage on any other pin	V_I	0.8	V_{SS}−0.8	V
Power dissipation per output	P_O	–	100	mW
Total power dissipation	P_{tot}	–	250	mW
Operating ambient temperature range	T_{amb}	−10	+ 60	°C
Storage temperature range	T_{stg}	−55	+ 125	°C

CHARACTERISTICS: Alert-Only-Pager (SP1 = 0)

V_{DD} = 0 V; V_{SS} = −2.7 V; V_{REF} = −2.7 V; V_B = −3.0 V; T_{amb} = 25 °C; quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 12) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	−1.7	−2.7	−6.0	V
Operating supply current	all outputs open; all inputs at V_{SS}; voltage converter off	I_{SS}	–	–	−22.0	μA
Level at which RAM switches to V_B		$V_{SS(sw)}$	−1.0	–	−1.7	V
Supply current; peak value	AL = LOW	I_{SSM}	–	–	−45.0	mA
Input voltage LOW PR, DI, BS, QS, WR, TS		V_{IL}	0.7 V_{SS}	–	–	V
AI, ON, OFF, SK, PC		V_{IL}	0.7 V_{REF}	–	–	V
Input voltage HIGH PR, DI, BS, QS, WR, TS		V_{IH}	–	–	0.3 V_{SS}	V
AI, ON, OFF, SK, PC		V_{IH}	–	–	0.3 V_{REF}	V

CHARACTERISTICS: Alert-Only-Pager (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input current						
PR, TS, BS	$V_I = V_{DD}$	I_I	7.0	–	18.0	μA
WR	$V_I = V_{SS}$	I_I	–9.0	–	–28.0	μA
DI	$V_I = V_{DD}$; $V_{RE} = V_{SS}$	I_I	6	–	16	μA
PR, TS, BS, DI, QS, PC	$V_I = V_{SS}$	I_I	–	–	–0.1	μA
WR, QS, PC	$V_I = V_{DD}$	I_I	–	–	0.1	μA
AI, ON, OFF, SK,	$V_I = V_{DD}$	I_I	6.0	–	16.0	μA
AI, ON, OFF, SK	$V_I = V_{SS}$	I_I	–	–	–0.1	μA
Input capacitance						
BS, DI, PR, WR, QS, TS		C_I	–	–	5	pF
AI, ON, OFF, SK, PC		C_I	–	–	5	pF
X1		C_I	–	–	5	pF
Output current LOW						
RE, OR, QR	$V_{OL} = -1.35$ V	I_{OL}	10.0	–	–	μA
DO, DS, BL, FL	$V_{OL} = -1.35$ V	I_{OL}	10.0	–	–	μA
AL	$V_{OL} = -1.5$ V	I_{OL}	17.5	–	41.5	mA
Output current HIGH						
RE	$V_{OH} = -1.35$ V	$-I_{OH}$	10.0	–	–	μA
OR, QR	$V_{OH} = -1.35$ V	$-I_{OH}$	10.0	540	750	μA
DO, DS, BL, FL	$V_{OH} = -1.35$ V	$-I_{OH}$	10.0	–	–	μA
AL	AL = high impedance	$-I_{OH}$	–	–	0.2	μA
Output capacitance						
X2		C_O	19	–	23	pF

CHARACTERISTICS: Display-pager; alphanumeric mode (SP1 = 1, SP2 = 1)

CN and CP open circuit;
$V_{DD} = 0$ V; $V_{SS} = -3.0$ V; $V_{REF} = -6.0$ V; $T_{amb} = 25$ °C; quartz crystal f = 32.768 kHz, $R_{Smax} = 40$ kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	–1.7	–	–3.0	V
Microcontroller interface negative reference		V_{REF}	V_{SS}	–	–6.0	V
Input current AI, ON, OFF, SK	$V_I = V_{REF}$ or V_{DD}	I_I	–	–	0.1	μA

CHARACTERISTICS: Display-pager; numeric mode (SP1 = 1, SP2 = 0)

220 nF capacitor connected to CN, CP;
V_{DD} = 0 V; V_{SS} = –3.0 V; T_{amb} = 25 °C;
quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	–1.7	–	–3.0	V
Voltage converter V_{REF} output: output voltage	V_{SS} = –3.0 V; no load	V_{REF}	–5.95	–	–6.0	V
	V_{SS} = –2.0 V; I_{VREF} = 150 μA; PC = 0	V_{REF}	–2.7	–	–	V
	V_{SS} = –2.0 V; I_{VREF} = 45 μA; PC = 1	V_{REF}	–2.7	–	–	V
output current	V_{SS} = –2.0 V; PC = 0	I_{VREF}	–150	–	–	μA
	V_{SS} = –2.0 V; PC = 1	I_{VREF}	–45	–	–	μA
Input current AI, ON, OFF, SK	V_I = V_{REF} or V_{DD}	I_I	–	–	0.1	μA

TIMING: Display-pager (SP1 = 1)

V_{DD} = 0 V; V_{SS} = –2.7 V; T_{amb} = 25 °C;
quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency		f_{osc}	–	32.768	–	kHz
Alerter frequency		f_{alert}	–	2048	–	Hz
Data input rate		f_{DI}	–	512	–	bits/s
Frequency reference FL output		f_{FL}	–	16.384	–	kHz
Data input transition time		t_{TDI}	–	–	100	μs
Preamble duration			1125	–	–	ms
Batch duration		t_{BAT}	–	1062.5	–	ms
Bit period		t_{BIT}	–	1.9531	–	ms
Data output rate		f_{DO}	–	512	–	bit/s
Data output transition time	C_L = 5 pF	t_{DTO}	–	–	100	ns
Data strobe clock period		t_{DS}	–	1.9531	–	ms
Data output set-up time		t_{DOS}	–	1.77	–	ms
Data strobe pulse width		t_{DSW}	61	122	–	μs
Data hold time		t_{DH}	30.5	61	–	μs
Call alert period		t_{ALT}	–	16	–	s
Call alert (low level) AL output only		t_{ALL}	–	4.0	–	s
Call alert (high level) QR and AL outputs		t_{ALH}	–	12.0	–	s

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parameter	conditions	symbol	min.	typ.	max.	unit
Call alert cycle period		t_{ALC}	–	1.0	–	s
Call alert pulse period		t_{ALP}	–	125	–	ms
Status pulse set-up time		t_{STP}	10.0	330	–	μs
Status pulse duration		t_{STD}	10.0	330	–	μs
Status alert period		t_{STON}	–	62.5	–	ms
Status alert delay		t_{STOF}	–	62.5	–	ms
Receiver control RE transition time	C_L = 5 pF	t_{RXT}	–	–	100	ns
RE establishment time		t_{RXON}	–	31.2	–	ms
Programming:						
data clock period		t_{PDC}	–	100	–	μs
data settling time		t_{PDS}	20.0	–	–	μs
write set-up time		t_{WSU}	20.0	–	–	μs
write pulse width		t_{WP}	10.0	–	–	μs
program input pulse width		t_{PR}	10.0	–	–	μs
program input settling time		t_{PRS}	20	–	–	μs
Power-on reset pulse width		t_{POR}	7.5	–	–	μs
Program start delay time		t_{CSU}	20.0	–	–	μs
Program data hold time		t_{PDE}	10.0	–	–	μs
Data clock period LOW		t_{X1}	10.0	50.0	–	μs

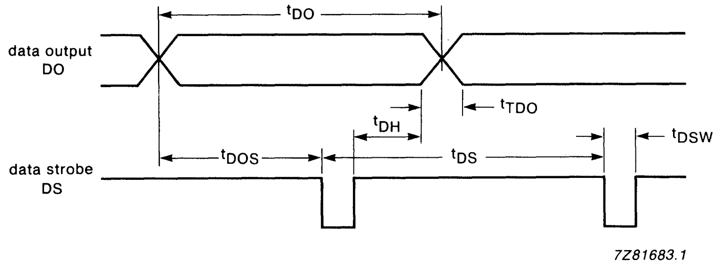


Fig. 7 Serial communications interface timing.

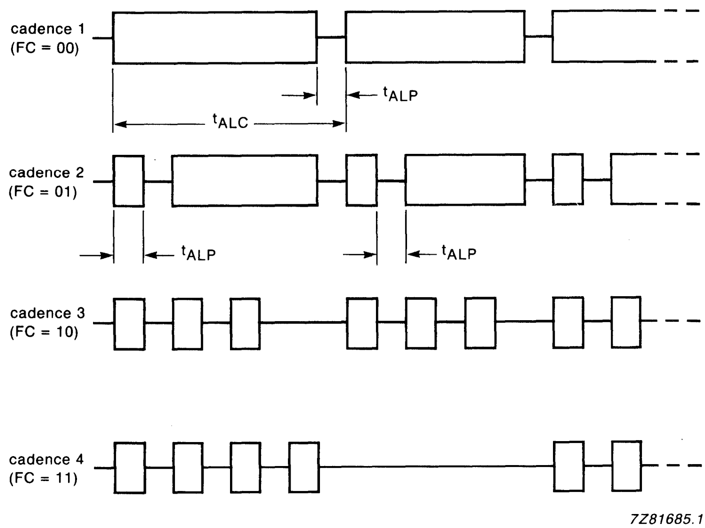


Fig. 8 Call alert cadences; FC refers to function control bits 20 and 21 in the address code word.

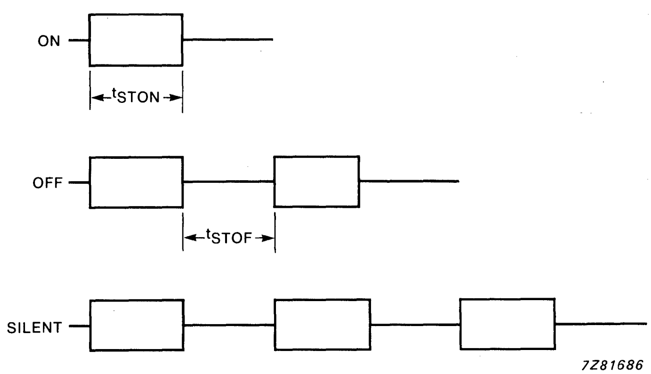


Fig. 9 Status indication cadences.

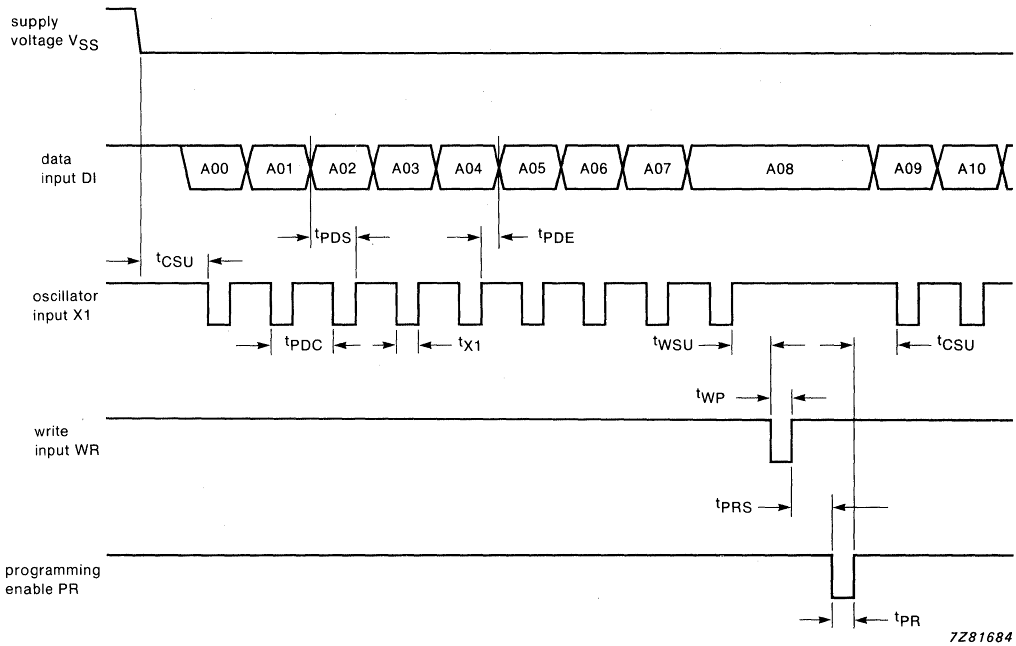


Fig. 10 Timing of RAM programming operation.

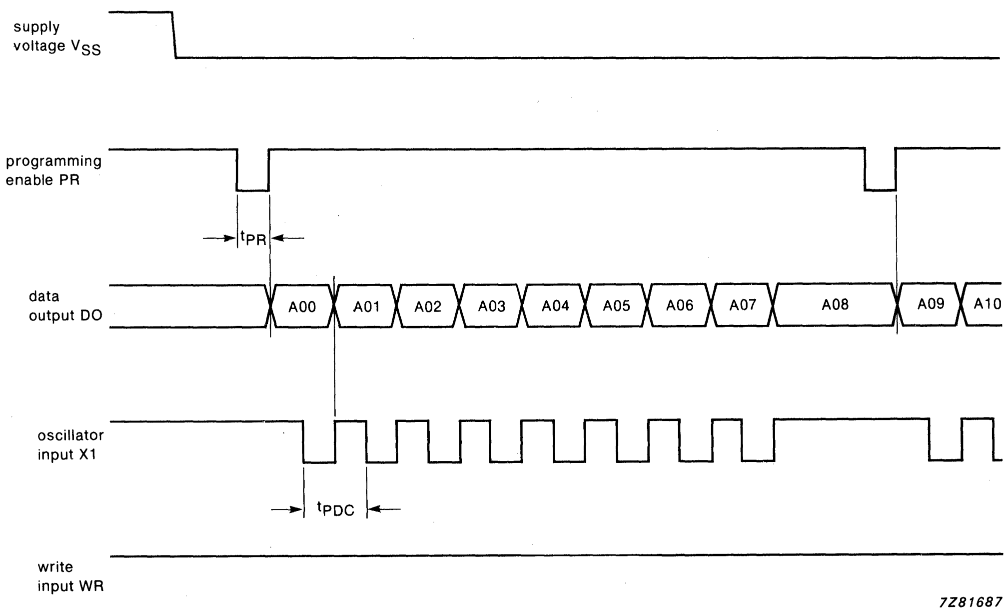


Fig. 11 Timing of RAM verify operation.

APPLICATION INFORMATION

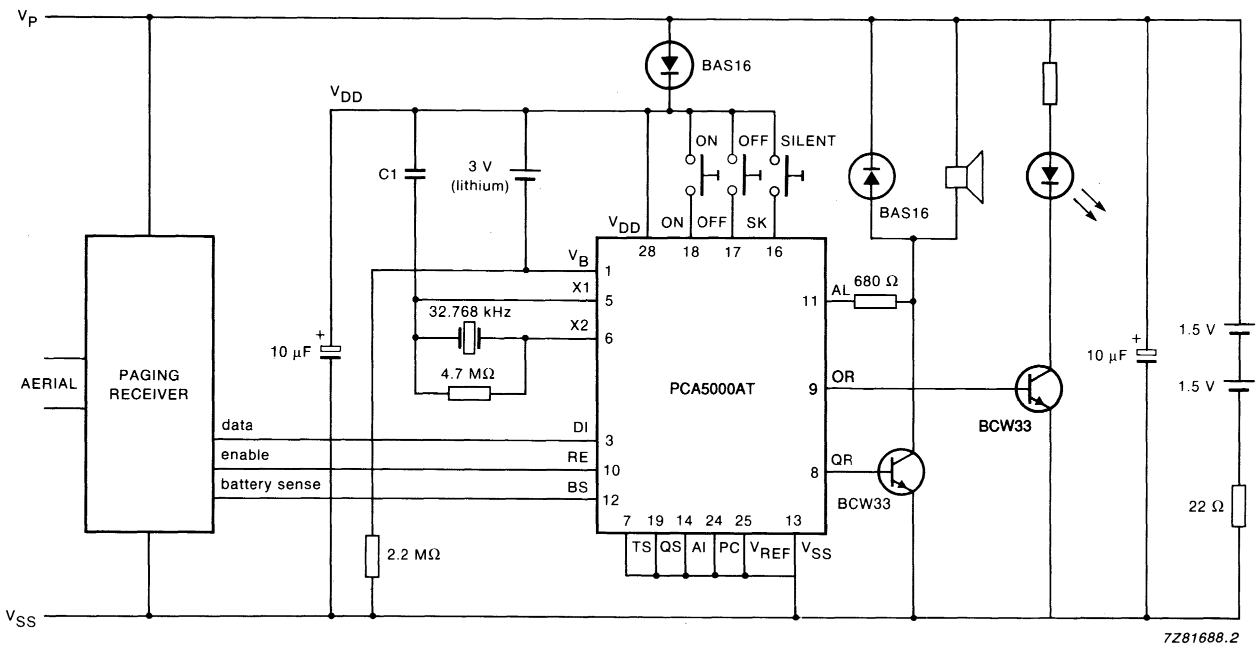


Fig. 12 Example of alert-only pager.

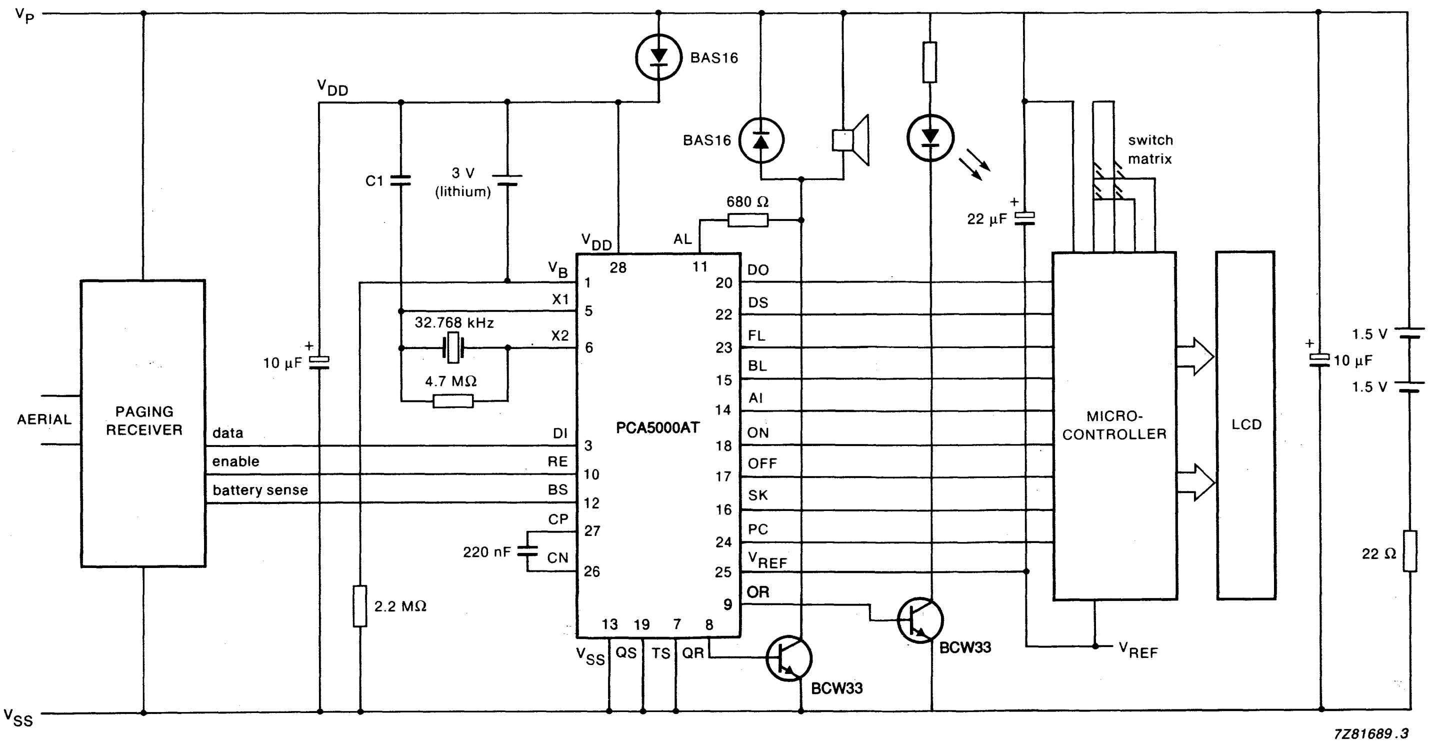


Fig. 13 Example of display-pager in alphanumeric mode with voltage converter enabled.

Application notes

Input pins

The programming control inputs have internal biasing resistors of sufficiently low impedance to provide safe operation even if the pins are left open circuit.

Pin 1 (V_B): RAM back-up battery negative supply. Connect this pin to the negative terminal of a lithium battery and connect the positive battery terminal to V_{DD}. This battery supply ensures data retention when the main supply voltage is removed.

Pin 2 (PR): programming enable, normally LOW. To enter the programming mode, pull this input HIGH when connecting the main supply voltage.

Pin 3 (DI): serial data input. During normal operation, POCSAG-coded data is received via this pin. When in programming mode, data to be stored in the internal RAM is read from this input whenever a pulse on X1 occurs.

Pin 4 (WR): programming write input, normally HIGH. A positive edge on this pin copies the preceding word shifted into the internal RAM. Keep this pin HIGH during RAM-read operations.

Pin 5 (X1): oscillator input. Connect a 32 kHz crystal to this pin during normal operation. When in programming write mode, a positive edge on X1 shifts the data present on DI to the internal register. When in programming read mode, a positive edge on X1 moves the next bit from the internal register to DO.

Pin 6 (X2): oscillator output. Return connection to the 32 kHz crystal.

Pin 7 (TS): test mode enable input, **always** LOW.

Pin 12 (BS): battery sense input. The decoder samples this input when it is in the ON state and the receiver is enabled. Every single sample is copied to the BL output. A continuous high-level alert tone is generated if four sequential samples are HIGH.

Pin 13 (V_{SS}): main negative supply voltage. Remove the voltage from this pin to leave the programming mode. The RC combination of 22 Ω and 10 μF (Figs 12 and 13) should remain connected; disconnect the battery only.

Pin 14 (AI): alarm input, normally LOW. A HIGH on this input causes a continuous high-level alert tone to be generated. The input may be pulsed to modulate the output tone.

Pin 16 (SK): silent key/mute input.
Alert-Only-Pager: push-button switch input, pushing the switch selects SILENT state.
Display-Pager: static input, when HIGH no calls are stored and no alert tones are generated for calls received.

Pin 17 (OFF): off key/reset input.
Alert-Only-Pager: push-button switch input, pushing the switch selects OFF state.
Display-Pager: static input, normally LOW. A positive-going pulse on this input causes (a) status indication cadences to be generated if the decoder is not alerting or (b) resetting an alert call or a battery-low alert if active.

Pin 18 (ON): on key/on-off input.
Alert-Only-Pager: push-button switch input. Pushing the switch selects ON state.
Display-pager: static input. LOW level selects OFF state, HIGH level selects ON state.

Pin 19 (QS): vibrator enable input, normally LOW. A HIGH level enables the vibrator output logic and switches QR to vibrator output.

Pin 24 (PC): voltage converter power control. The level on this pin determines the output impedance of the voltage converter. LOW selects low impedance, HIGH selects high impedance.

Pin 26 (CN): voltage converter external capacitor, negative connection.

Input pins (continued)

Pin 27 (CP): voltage converter external capacitor, positive connection.

Pin 28 (V_{DD}): main positive supply input. This pin is common to all supply voltages and is referred to as GROUND.

Output pins

Pin 8 (QR): alert high-level output/vibrator output. This output can directly drive an external bipolar transistor to control a vibrator-type alerter if QS is set HIGH, or supports high-level alerting in conjunction with AL.

Pin 9 (OR): out-of-range output, active HIGH. If the decoder detects 'carrier-off', an output is generated for the duration of the synchronization scan period. Connecting OR to QR provides alert tone generation during 'carrier-off'.

Pin 10 (RE): receiver enable output, active HIGH. Connect the radio paging receiver power control input to this pin to minimize power consumption. Whenever no input data is required, the PCA5000AT will disable the paging receiver to conserve power.

Pin 11 (AL): alert low-level output, active LOW. The low-level alert tone is generated via this output; the alert becomes high-level in conjunction with QR.

Pin 15 (BL): battery-low output, active HIGH. Every time the PCA5000AT samples the BS input, data sensed is output on this pin.

Pin 20 (DO): received data output. During normal operation, accepted calls and possibly subsequent message code words are output via this pin at a rate of 512 bits/s. When in programming read mode, data read from the internal RAM is presented bit-by-bit on this pin.

Pin 22 (DS): received data strobe output, active LOW. In normal operation, every time this output goes LOW, the next bit on the DO output is valid.

Pin 23 (FL): frequency reference output. If the decoder is programmed as a Display-Pager, a 16 kHz squarewave reference is output from this pin.

Pin 25 (V_{REF}): microcontroller interface negative reference voltage. The LOW level of pins FL, BL, DO, DS, AI, ON, OFF, SK and PC is related to the voltage on V_{REF}.

Alert-Only-Pager: Connect V_{REF} output to V_{SS}.

Display-Pager: The doubled negative supply voltage generated by the internal voltage converter is output from V_{REF}. The V_{REF} pin may also be driven from an external supply if the capacitor across CN/CP is removed and CN/CP are left open circuit.

POCSAG paging decoder with EEPROM storage | PCF5001T

DESCRIPTION

The PCF5001T is a very low power Decoder and Pager Controller specially designed for use in Radiopagers. The architecture of the PCF5001T allows for flexible application in a wide variety of Radiopager designs.

The PCF5001T is fully compatible with CCIR Radiopaging Code Number 1 (also known as the POCSAG code) operating at the 512 bps data rate, and 1200 bps data rate. 2400 bps operation is also possible. The PCF5001T also offers features which extend the basic flexibility and efficiency of this code standard.

On-chip non-volatile 114 bit EEPROM storage is provided to hold up to four user addresses, two frame numbers and the programmed decoder condifuration.

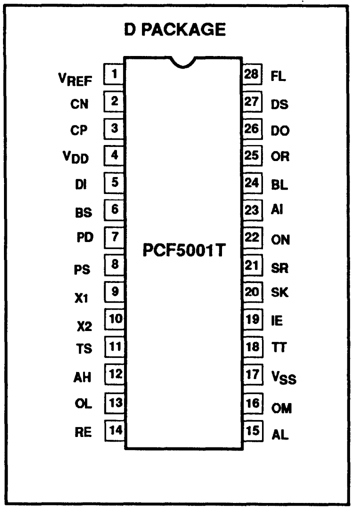
FEATURES

- Wide operating supply voltage range (1.5 to 6.0V)
- Extended temperature range: –40 to +85°C
- Very low supply current (60μA typ. with 76.8kHz crystal)
- Programmable call termination conditions
- Eight different alert cadences
- Directly drives magnetic or piezoelectric beeper
- Silent call storage, up to eight different calls
- Repeat alarm facility
- Programmable duplicate call suppression
- Interfaces directly to UAA2050T and UAA2080T digital paging receivers
- Programmable receiver power control for battery economy
- On-chip voltage converter with improved drive capability
- Serial microcontroller interface for display pager applications
- Optional visual indication of received call data using a modified RS-232 format
- Level shifted microcontroller interface signals
- Alert on low battery
- Optional out-of-range indication

APPLICATIONS

- Alert-only pagers, display pagers
- Telepoint
- Telemetry/data receivers

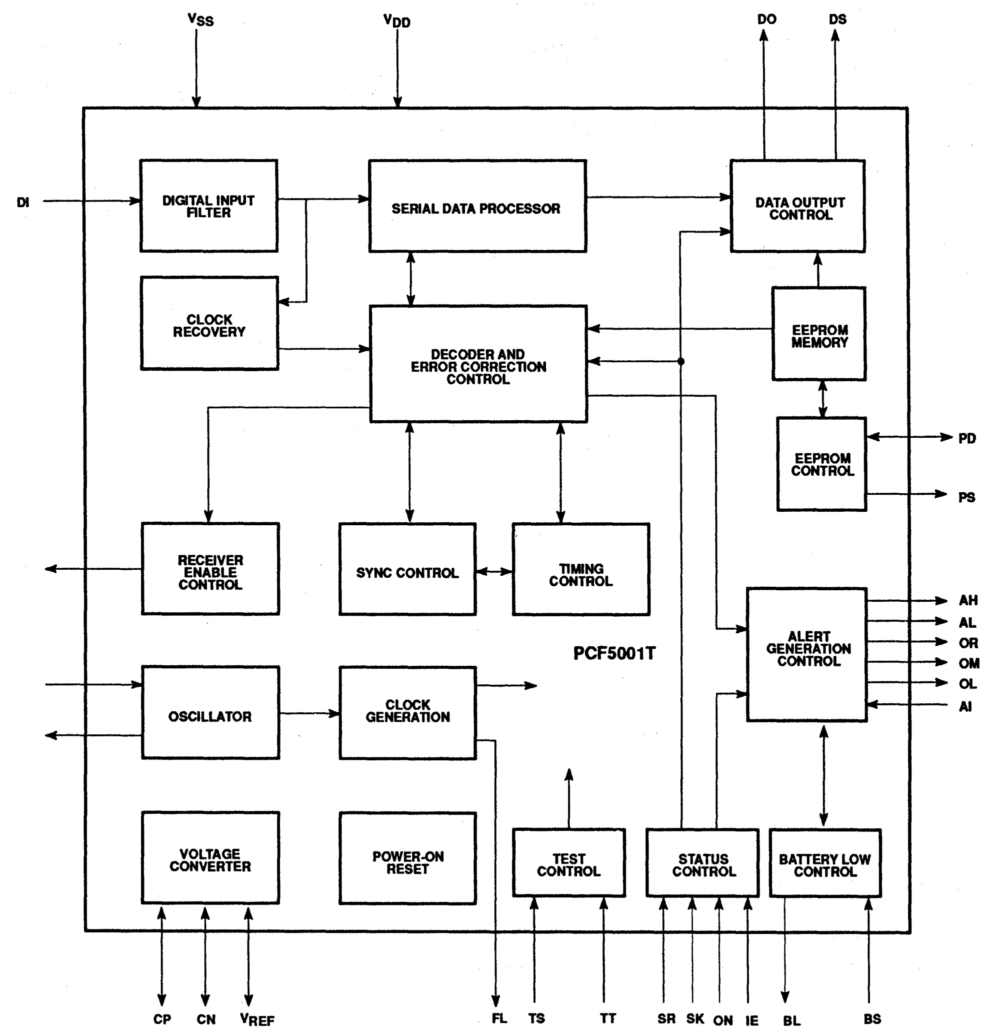
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic SO	0 to +70°C	SOT-136A

BLOCK DIAGRAM,



Sound fader control circuit | TEA6300

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I^2C-bus controlled preamplifier for car radios.

Features

- Source selector for three stereo inputs
- Inputs and outputs for noise reduction circuits
- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control from + 15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control from 0 dB to −30 dB in steps pf 2 dB
- Fast muting
- Low noise suitable for DOLBY* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- I^2C-bus control for all functions
- ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	70	92	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal plus noise-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licencing Corporation, San Fransisco, California (U.S.A.).

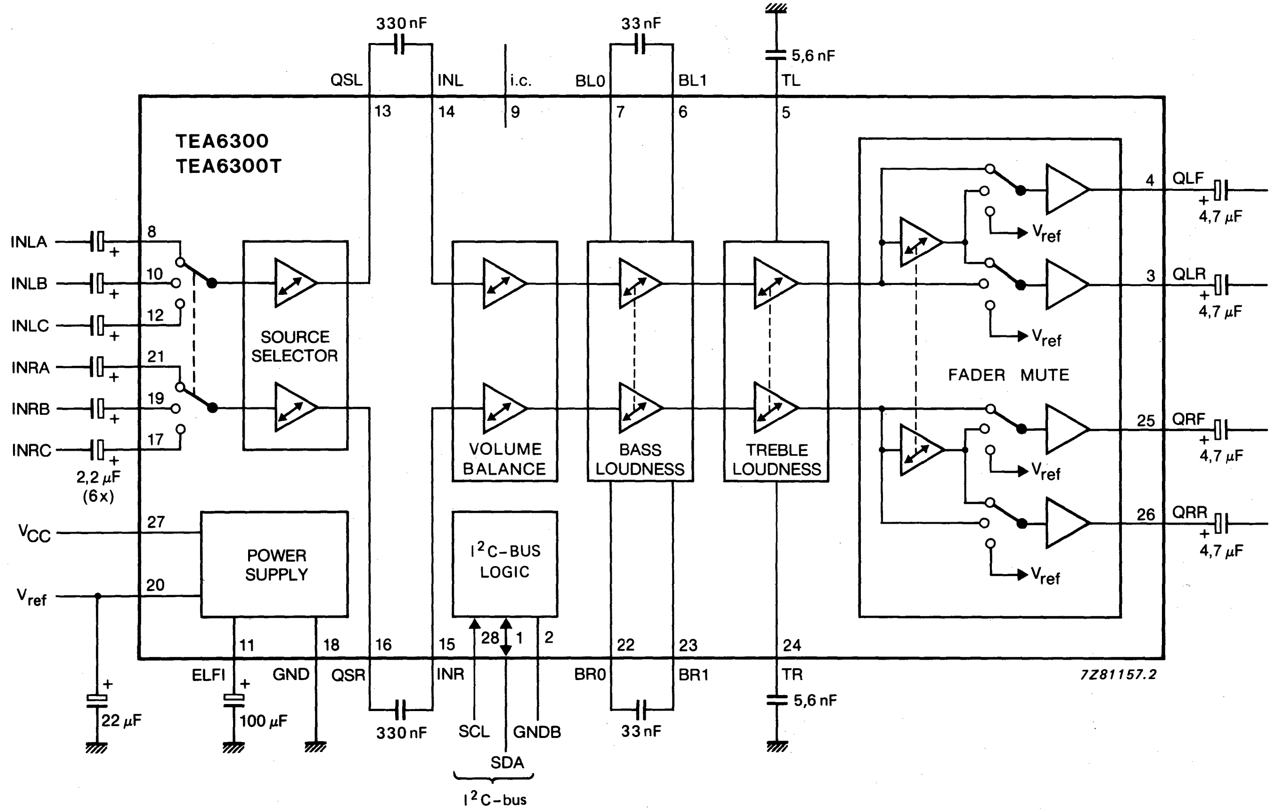


Fig. 1 Block diagram.

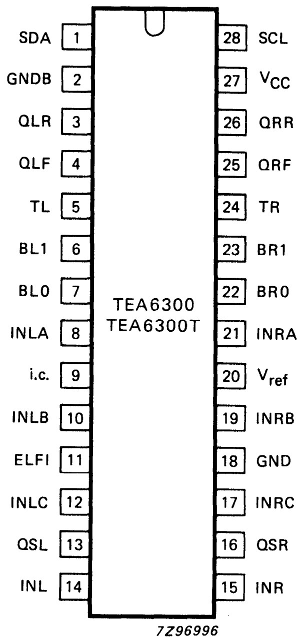


Fig. 2 Pinning diagram.

PINNING

1	SDA	serial data input/output (I^2C-bus)
2	GNDB	ground for I^2C-bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BLO	bass control capacitor; left channel
8	INLA	input left source A
9	i.c.	internally connected
10	INLB	input left source B
11	ELFI	electronic filtering for supply
12	INLC	input left source C
13	QSL	output source selector left
14	INL	input left control part
15	INR	input right control part
16	QSR	output source selector right
17	INRC	input right source C
18	GND	ground
19	INRB	input right source B
20	V_{ref}	reference voltage (1/2 V_{CC})
21	INRA	input right source A
22	BRO	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2C-bus)

FUNCTIONAL DESCRIPTION

The source selector selects three stereo channels –RF part (AM/FM), recorder and compact disc. As the outputs of the source selector and the inputs of the main control part are available, additional circuits such as compander and equalizer systems may be inserted into the signal path. The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6300 has four outputs a low-level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. An extra pop suppression circuit is built in for pop-free switching on and off. As all switching and control functions are controllable via the two-wire I^2C-bus, no external interface between the microcomputer and the TEA6300 is required.

The on-chip power-on-reset sets the TEA6300 to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	16	V
Maximum power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	–55	+ 150	°C
Operating ambient temperature range	T_{amb}	–40	+ 85	°C

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Supply current at 8,5 V	I_{CC}	–	–	33	mA
Supply current at 13,2 V	I_{CC}	–	–	44	mA
DC voltage inputs, outputs and reference	V_{DC}	0,45	0,5	0,55	V
Internal reference voltage (pin 20) V_{ref} = 0,5 V_{CC}	V_{REF}	–	4,25	–	V
Maximum voltage gain bass and treble linear, fader off	G_v	19	20	21	dB
Output voltage level for P_{max} at the output stage	$V_{o(rms)}$	–	500	–	mV
for start of clipping	$V_{o(rms)}$	–	1000	–	mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency −1 dB	f_r	35	–	20 000	Hz
Channel separation G_v = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	70	92	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz V_i = 50 mV; G_v = 20 dB	THD	–	0,1	0,3	%
V_i = 500 mV; G_v = 0 dB	THD	–	0,05	0,2	%
V_i = 1,6 V; G_v = −10 dB	THD	–	0,2	0,5	%
Ripple rejection $V_{r(rms)} < 200$ mV; G_v = 0 dB; bass and treble linear; at f = 100 Hz	RR_{100}	–	70	–	dB
at f = 40 Hz to 12,5 kHz	RR_{range}	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal plus noise-to-noise ratio bass and treble linear; notes 1 and 2 CCIR 468-2 weighted; quasi peak					
V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	(S + N)/N	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	(S + N)/N	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	65	70	–	dB
V_i = 500 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	65	78	–	dB
V_i = 50 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	70	–	dB
V_i = 500 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	85	–	dB
Noise output power mute position, only contribution of TEA6300; power amplifier for 25 W	P_{no}	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$) between bus inputs and signal outputs G_V = 0 dB; bass and treble linear	α_B	–	110	–	dB
Source selector					
Input impedance	Z_i	20	30	40	kΩ
Output impedance	Z_o	–	–	100	Ω
Output load resistance	R_L	10	–	–	kΩ
Output load capacity	C_L	0	–	200	pF
Input isolation not selected source; frequency range 40 Hz to 12,5 kHz	α_S	–	80	–	dB
Voltage gain $R_L \geq 10$ kΩ	G_V	–	0	–	dB
Internal bias voltage ratio	$V_{b\,int}/V_{ref}$	–	1	–	
Maximum input voltage level (RMS value)					
THD < 0,5%	$V_{i(rms)}$	–	1,65	–	V
THD < 0,5%; V_{CC} = 7,5 V	$V_{i(rms)}$	–	1,5	–	V
Total harmonic distortion V_i = 500 mV; R_L = 10 kΩ	THD	–	–	0,1	%
Noise output voltage weighted CCIR 468-2, quasi peak	V_{no}	–	9	20	μV
DC offset voltage between any inputs	V_o	–	–	10	mV
Control part					
Source selector disconnected, source resistance 600 Ω					
Input impedance	Z_i	35	50	65	kΩ
Output impedance	Z_o	–	100	150	Ω
Output load resistance	R_L	5	–	–	kΩ
Output load capacity	C_L	0	–	2500	pF

Sound fader control circuit TEA6300

parameter	symbol	min.	typ.	max.	unit
Maximum input voltage THD < 0,5%; G_V = −10 dB; bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise output voltage weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off					
G_V = 20 dB	V_{no}	–	110	220	μV
G_V = 0 dB	V_{no}	–	25	50	μV
G_V = −66 dB	V_{no}	–	19	38	μV
mute position	V_{no}	–	11	22	μV
Volume control					
Continuous control range	G_c	–	86	–	dB
Step resolution		–	2	–	dB
Attenuator set error (G_V = + 20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error (G_V = + 20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error balance in mid position, bass and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_m	72	90	–	dB
DC step offset					
Between any adjoining step and any step to mute					
G_V = 0 to −66 dB		–	0,2	10	mV
G_V = 20 to 0 dB		–	2	15	mV
In any treble and fader position G_V = 0 to −66 dB		–	–	10	mV
In any bass position G_V = 0 to −66 dB		–	–	20	mV
Bass control					
Bass control range					
f = 40 Hz; maximum boost	G_b	14	15	16	dB
f = 40 Hz; maximum attenuation	G_b	11	12	13	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Treble control					
Treble control range					
f = 15 kHz; maximum boost	G_t	11	12	13	dB
f = 15 kHz; maximum attenuation	G_t	11	12	13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Fader control					
Continuous attenuation fader control range	G_f	–	30	–	dB
Step resolution		–	2	–	dB
Attenuator set error		–	–	1,5	dB
Mute attenuation	α_m	74	84	–	dB
Digital part					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	–0,3	–	+ 1,5	V
Input current					
HIGH	I_{IH}	–10	–	+ 10	μA
LOW	I_{IL}	–10	–	+ 10	μA
Output voltage LOW I_L = 3 mA	V_{OL}	–	–	0,4	V
AC characteristics					
in accordance with the I^2C-bus specification					
Power-on-Reset					
When RESET is active the GMU (general mute) bit is set and the I^2C-bus receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage					
start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the circuit. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average meter reading are 4,5 dB better than on CCIR 468-2 quasi peak.

I^2C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 1000 0000
A = acknowledge, generated by the slave
SUBADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Table 1 I^2C-bus; subaddress/data

function	subaddress	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	SCC	SCB	SCA

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel (front or rear)
SCA to SCC	source selector control
GMU	mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	don't care bits (logic 1 during testing)

Table 2 Bass setting

G_V dB	DATA			
	BA3	BA2	BA1	BA0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_V dB	DATA			
	TR3	TR2	TR1	TR0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 4 Volume setting LEFT

G_V dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.			.			
.			.			
.			.			
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_V dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting front dB	setting rear dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
−2	0	1	1	1	1	1	0
−4	0	1	1	1	1	0	1
−6	0	1	1	1	1	0	0
−8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting front dB	setting rear dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	−2	1	0	1	1	1	0
0	−4	1	0	1	1	0	1
0	−6	1	0	1	1	0	0
0	−8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Selected inputs

selected inputs	DATA SCC	SCB	SCA
data not allowed	1	1	1
data not allowed	1	1	0
data not allowed	1	0	1
INLC, INRC	1	0	0
data not allowed	0	1	1
INLB, INRB	0	1	0
INLA, INRA	0	0	1
data not allowed	0	0	0

Table 8 Mute control

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

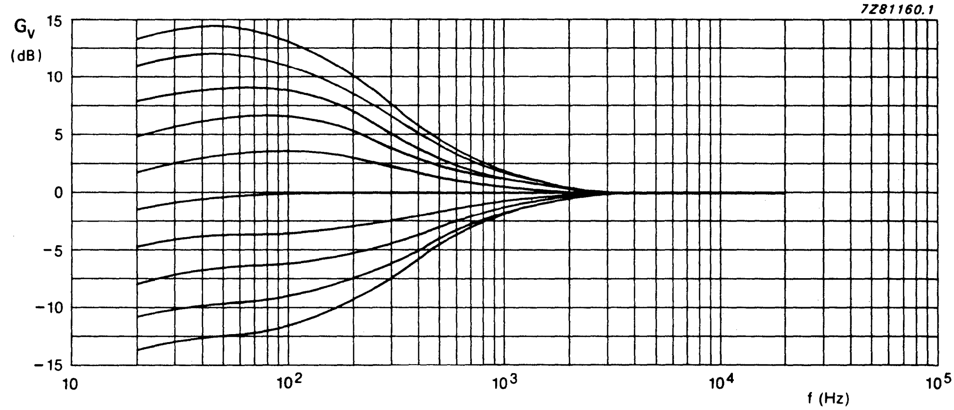


Fig. 3 Bass control without T-pass filter.

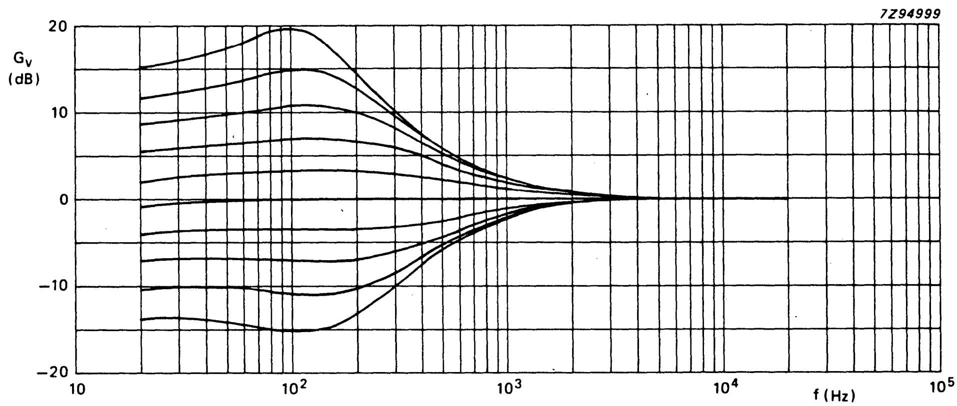
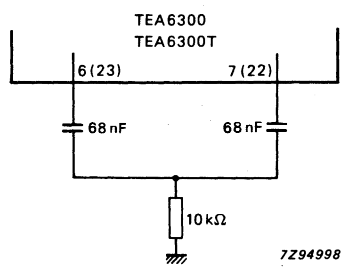


Fig. 4 Bass control with T-pass filter.



Pin numbers in parenthases refer to the bass control, right channel.

Fig. 5 T-pass filter.

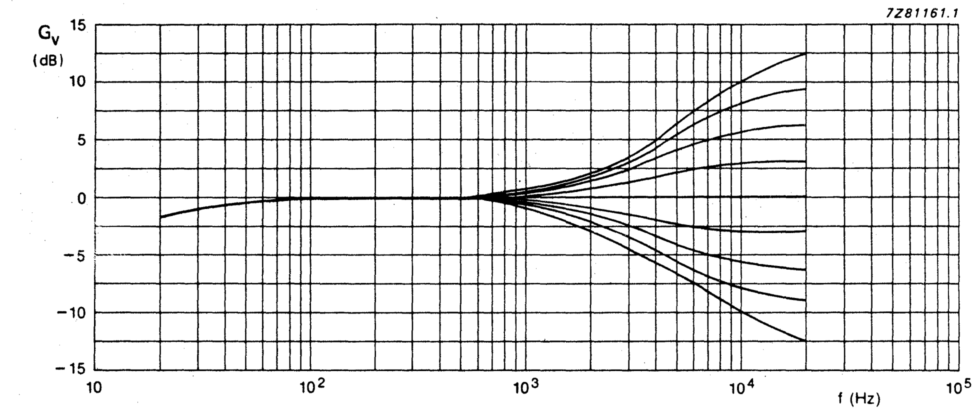


Fig. 6 Treble control.

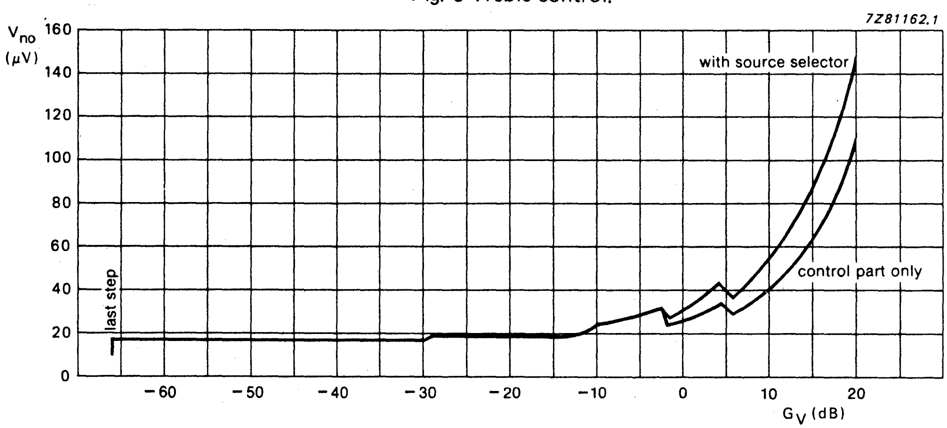


Fig. 7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

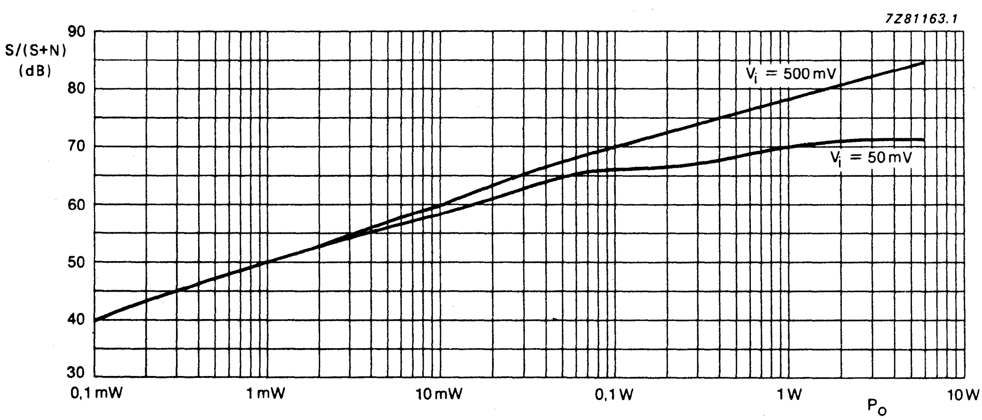


Fig. 8 Signal-to-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig. 9).

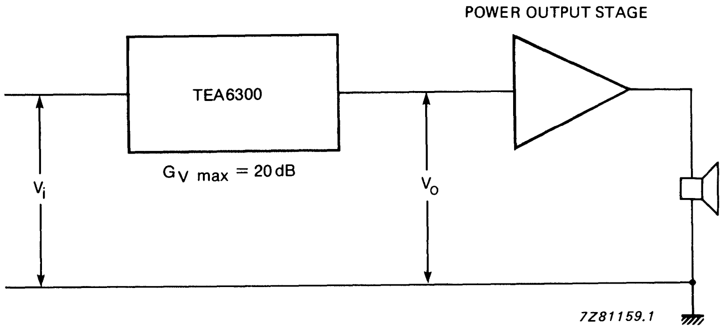


Fig. 9 Recommended level diagram; $V_{i\ min} = 50$ mV, $V_o = 500$ mV for P_{max}.

APPLICATION INFORMATION

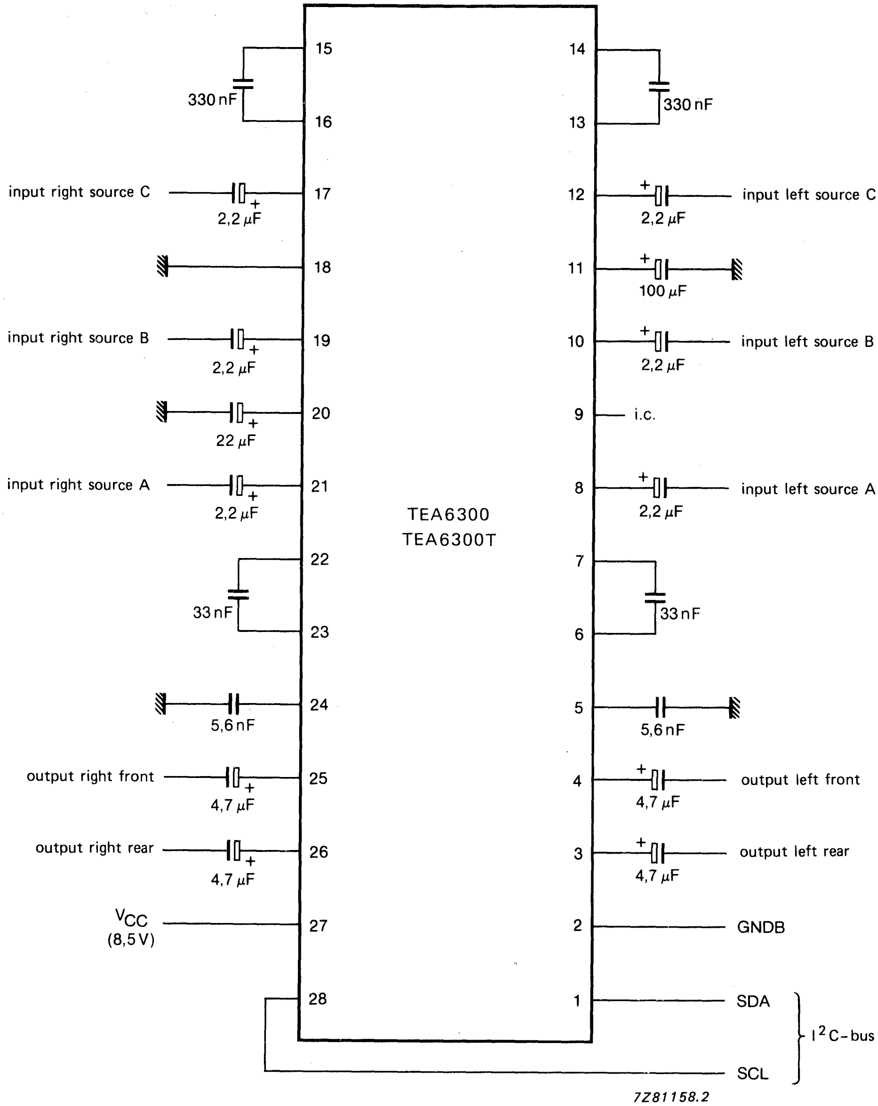


Fig. 10 Test and application circuit.

Data processor for cellular radio (DPROC) UMA1000T

GENERAL DESCRIPTION

The UMA1000T is a low power CMOS LSI device incorporating the data transceiving, data processing, and SAT functions (including on-chip filtering) for an AMPS or TACS hand-held portable cellular radio telephone.

Features

- Single chip solution to all the data handling and supervisory functions
- Configurable to both AMPS and TACS
- I^2C serial bus control
- All analog interface and filtering functions fully implemented on chip
- Error handling in hardware reduces software requirements
- Robust SAT decoding and transponding circuitry
- Low current consumption
- Small physical size
- Minimum external peripheral components required

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 28)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 28)					
normal operation	I_{DD}	–	2	–	mA
Operating ambient temperature range	T_{amb}	–40	–	+ 85	^oC

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

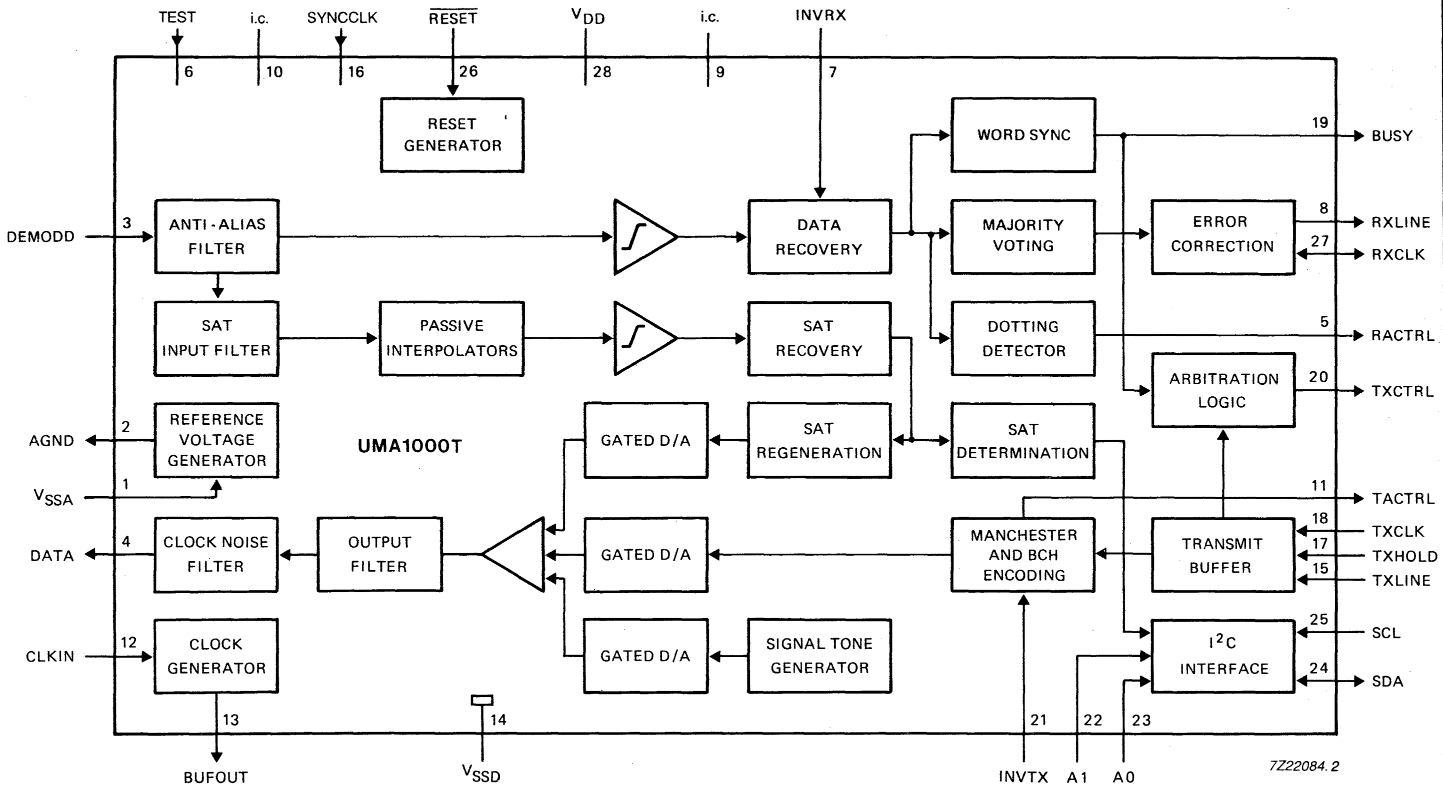


Fig. 1 Block diagram.

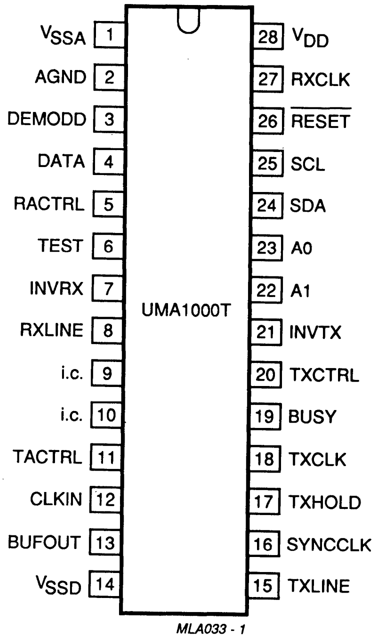


Fig.2 Pinning diagram.

PINNING

1	V_{SSA}	analog negative supply (0 V)
2	AGND	$(V_{DD} - V_{SSA})/2$ analog reference ground
3	DEMODD	received data signal input
4	DATA	transmitted data signal output
5	RACTRL	received audio control output
6	TEST	SCAN Control input - used for power on reset
7	INVRX	inverts sense of received data stream
8	RXLINE	received data signal output
9	i.c.	internally connected; must be left open -circuit
10	i.c.	
11	TACTRL	transmitter audio control output
12	CLKIN	1.2 MHz external master clock input
13	BUFOUT	buffered output of internal clock oscillator
14	V_{SSD}	digital ground
15	TXLINE	transmitted data signal
16	SYNCCLK	SCAN CLOCK Control input - used for power-on reset
17	TXHOLD	holds off transmission of data
18	TXCLK	transmitted data clock input
19	BUSY	reverse control channel status output
20	TXCTRL	transmitter control output
21	INVTX	inverts sense of transmitted data stream
22	A1	address input 1 - used for power-on reset (I² C-bus)
23	A0	address input 0 (I² C-bus)
24	SDA	serial data input/output (I² C-bus)
25	SCL	serial clock input (I² C-bus)
26	$\overline{RESET}$	master rest input
27	RXCLK	received data clock input
28	V_{DD}	positive supply voltage (+ 5 V)

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Supply current	normal operation	I_{DD}	–	2.0	–	mA
Digital inputs	note 1					
Input voltage LOW		V_{IL}	0	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD} + 0.3	V
Input capacitance		C_I	–	–	6	pF
Digital outputs	note 1					
Output voltage LOW	I_{sink} = 1 mA	V_{OL}	–	–	0.4	V
Output voltage HIGH	I_{source} = 1 mA	V_{OH}	V_{DD} – 0.4	–	–	V
Open-drain outputs	note 2					
Output voltage LOW	I_{sink} = 2 mA	V_{OL}	–	–	0.4	V
Open-drain SDA						
Output voltage LOW	I_{sink} = 3 mA	V_{OL}	–	–	0.4	V

Notes to the characteristics

1. All digital inputs and outputs of DPROC are compatible with standard CMOS devices and the following general characteristics apply.
2. Open-drain outputs have no internal pull-up resistors.

FUNCTIONAL DESCRIPTION

General

The UMA1000T (DPROC) is a single chip CMOS device which handles the data and supervisory functions of an AMPS or TACS subscriber set.
These functions are:

- Data reception and transmission
- Control and voice channel exchanges
- Error detection, correction, decoding and encoding
- Supervisory Audio Tone decoding and transponding
- Signalling Tone generation

In an AMPS or TACS cellular telephone system, mobile stations communicate with a base over full duplex RF channels. A call is initially set up using one out of a number of dedicated control channels. This establishes a duplex voice connection using a pair of voice channels. Any further transmission of control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticable by the user. A data rate of 10 kbit/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig. 3.

A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz), is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analagous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice Channel. The signal must be accurately recovered and transponded back to the base station to complete the 'loop'. At the base station this signal is used to ascertain the overall quality of the communication link.

Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.

The key requirements of a hand held portable cellular set are:

- small physical size
- minimum number of interconnections (serial bus)
- low power consumption
- low cost

The DPROC is a member of our Cellular Radio chipset, based on the I^2C-bus, which meets these requirements. A cellular radio system schematic using the chip set is shown in Fig. 4.

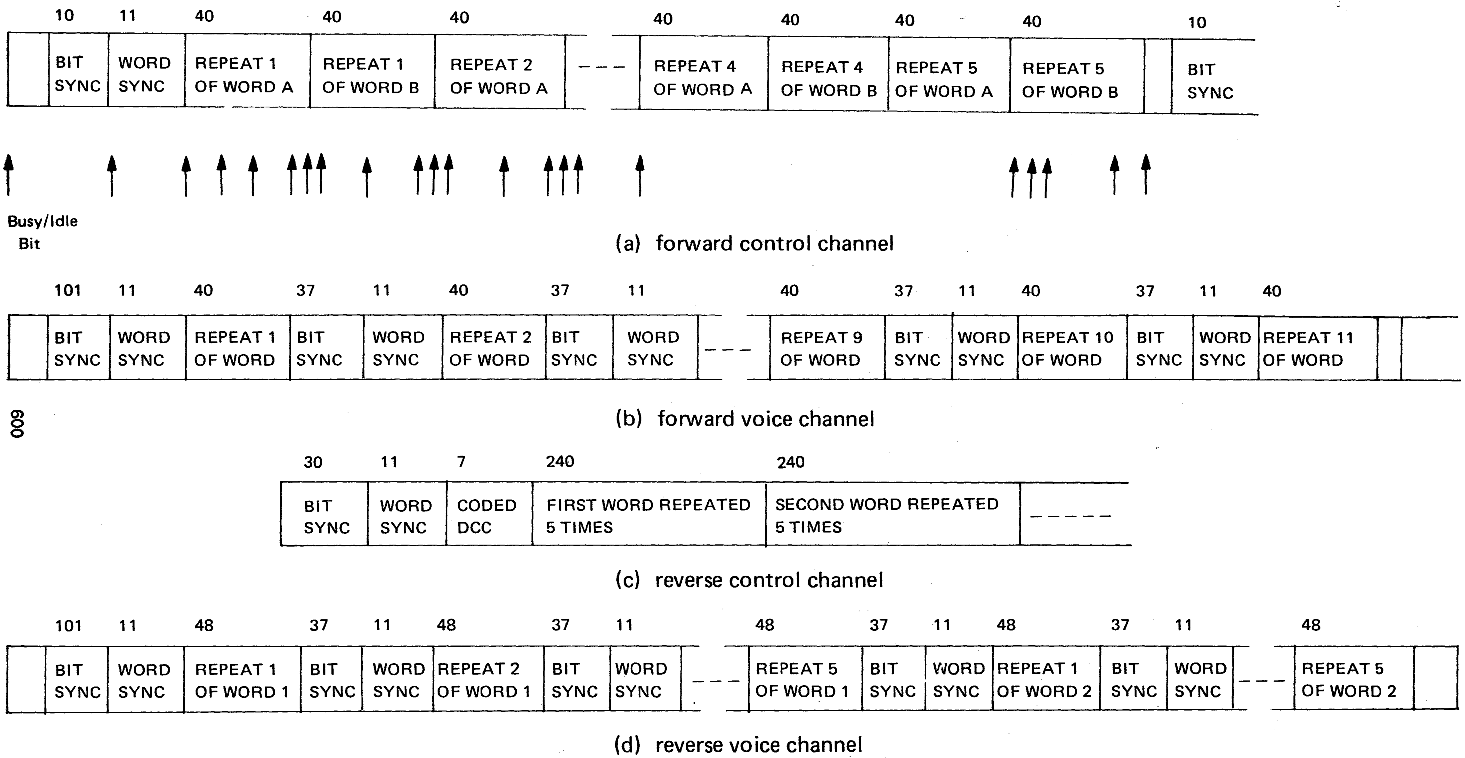


Fig. 3 Signalling formats.

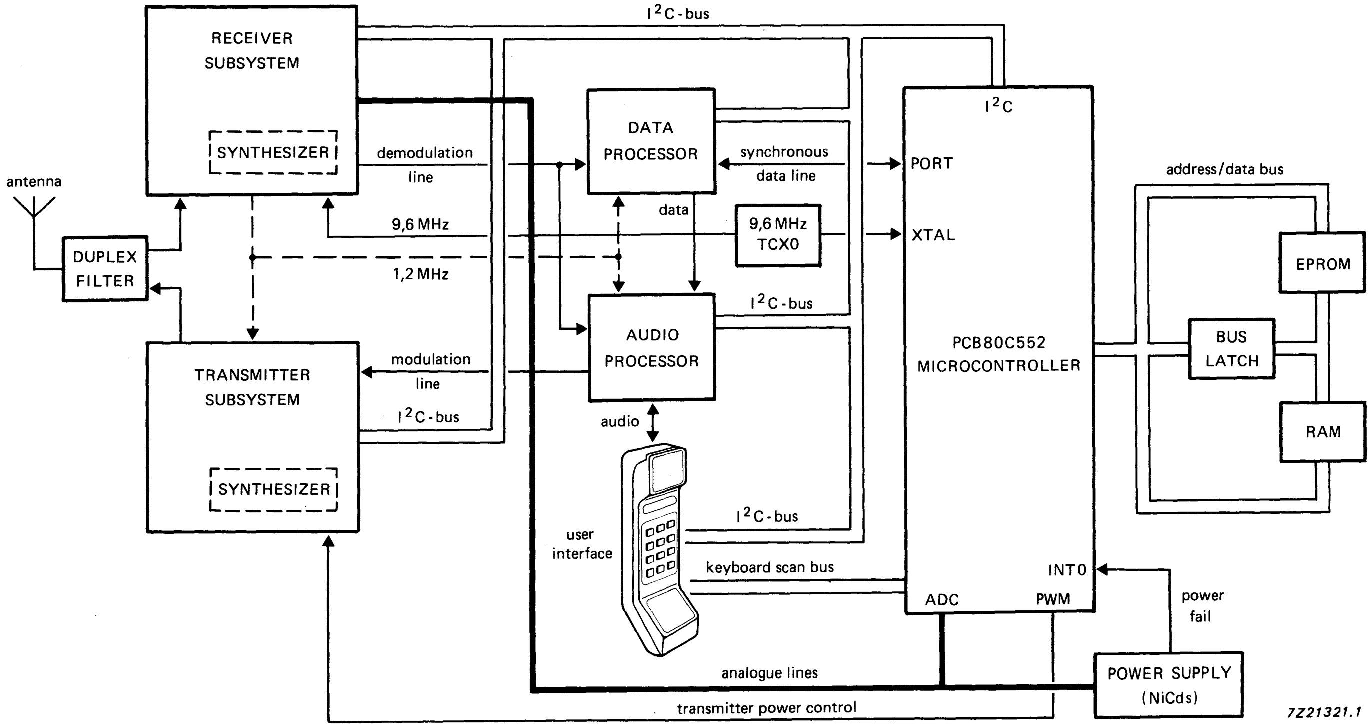


Fig. 4 Cellular radio system schematic.

EXTERNAL PIN DESCRIPTION

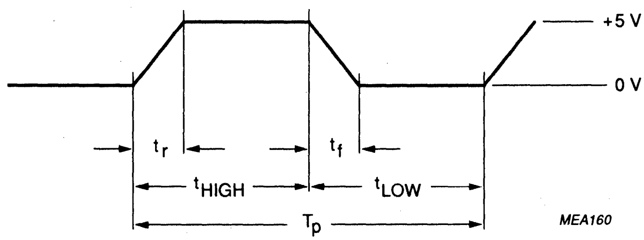
Supply (V_{DD}; V_{SSA}; V_{SSD}; AGND)

V_{DD} : Positive supply voltage for digital and analog circuitry (± 5 V +10%)
V_{SSA} : Negative supply voltage for analog circuitry (0 V)
V_{SSD} : Digital ground (0 V)
AGND: Internally generated reference ground used by internal analog circuitry. Voltage level $(V_{DD} - V_{SSA})/2 \pm 2\%$.

Both V_{SSA} and V_{SSD} must be connected to common ground.

System clock (CLKIN; BUFOUT)

CLKIN is a digital input for the externally generated 1.2 MHz master clock. This signal should be accurate to 100×10^{-6} and have a worst case of 60 : 40 mark-space ratio. BUFOUT is the buffered output of the clock oscillator and provides the option of generating the clock signal on chip by connecting a 1.2 MHz crystal between BUFOUT and CLKIN.



parameter	symbol	min.	typ.	max.	unit
Clock period time	T_p	833.25	833.33	833.42	ns
HIGH time	t_{HIGH}	40%	50%	60%	T_p
LOW time	t_{LOW}	–	T_p-t_{HIGH}	–	
Rise time	t_r	–	50	–	ns
Fall time	t_f	–	50	–	ns

I²C serial data link (SDA; SCL)

SDA is the bi-directional data line; SCL the clock input from an I²C master. These constitute a typical I²C link and conform to standard characteristics as defined in the I²C-bus specification.

- data rate: up to 100 kbit/s

Slave Address Select (A0; A1)

Selection of the device slave address is achieved by connecting A0 to either V_{SSD} or V_{DD} and connecting A1 to either pin 16 and pin 6 or to V_{DD}. The slave address is defined in accordance with the I²C specifications as shown in Fig. 5.

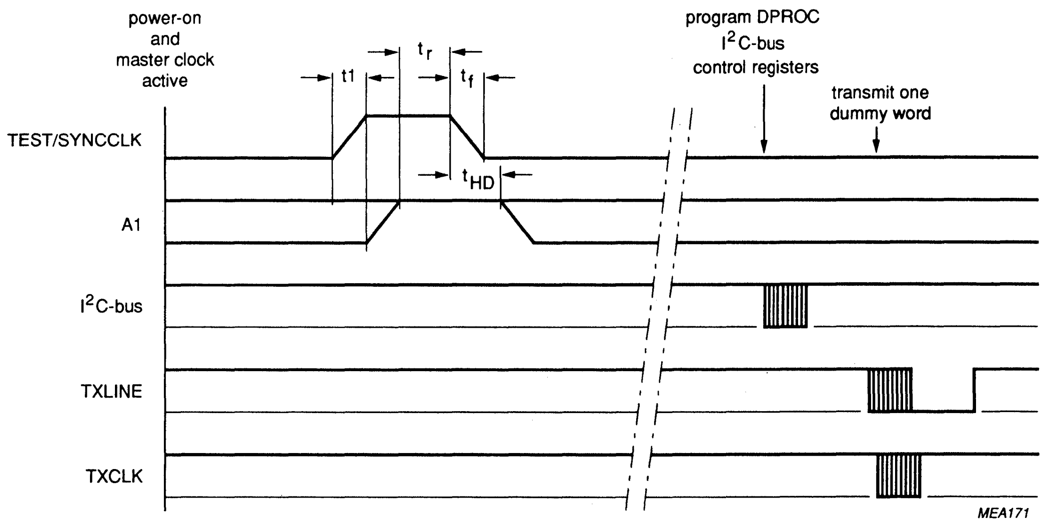
1	1	0	1	1	A1	A0	R/$\overline{W}$

Fig. 5 Device slave address.

Power-up state

DPROC will not respond reliably to any inputs (including $\overline{RESET}$) until 100 μs after the power supply has settled within the specified tolerance. The analog sections of the device will have stabilized within 5 ms. No power-on-reset is provided, therefore before the device can enter normal operation TEST and SYNCCLK must be pulsed HIGH. The reset pulse on these pins must have a minimum period of 250 μs and the fall time of the negative going edge must be faster than 1 μs. Pin A1 must remain HIGH during this reset period therefore if the A1 bit of the I^2C address is required to be logic 0. A1 may be connected to TEST and SYNCCLK. If it is required to be at logic 1 then A1 may be permanently connected to V_{DD}. If it is required that A0 = logic 1, then a normal master reset (pin 26) sequence must follow the power-on-reset sequence to get the internal registers in the defined state.

After the power-on-reset a dummy transmission should be made to initiate internal DPROC counters. This transmission should be made with arbitration (ABREN) disabled and the RF transmitter stage switched OFF. Figure 6 shows the power-on reset sequence.



Where:

t1 = time not critical.
t_r = reset time = 250 μs max.
t_f = pulse fall time = 1 μs max.
t_{HD} = Al hold time = 0 μs min.

Note

The RF transmitter is OFF during reset sequence.

Fig.6 Power-on reset programming sequence.

Master reset ($\overline{RESET}$)

$\overline{RESET}$ is an asynchronous active LOW master reset input, with a minimum active pulse width of 2 μs which may be used to reset certain logic within DPROC to a predefined state as illustrated in Tables 1 and 2. Alternatively, DPROC may be set into a known initial state be setting the I^2C control register as required. The internal reset sequence after a negative pulse on $\overline{RESET}$ takes 250 μs.

EXTERNAL PIN DESCRIPTION (continued)

Table 1 Predefined state of the digital output pins

output	state
RXLINE	HIGH
TXCTRL	HIGH
TACTRL	HIGH
RACTRL	HIGH
BUSY	HIGH

Table 2 Predefined state of the I^2C registers

register	bit							
	7	6	5	4	3	2	1	0
control	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
SATD	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
TST	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

Data Transfer Link (RXLINE; TXLINE; TXHOLD; TXCLK and RXCLK)

RXLINE, TXLINE, TXCLK and RXCLK provide a dedicated serial data link for the transfer of system data messages between DPROC and the system controller at variable rates of up to 200 kbits/s. TXHOLD allows the system controller to preload the DPROC transmit register with one word without the data being transmitted. DPROC then starts transmitting the instant TXHOLD is driven LOW.

- RXCLK : clock input from system controller
- RXLINE : data output from DPROC to system controller
- TXCLK : clock input from system controller
- TXLINE : open drain data bi-directional line to the system controller
- TXHOLD : (HIGH) holds off transmission of data
- data rate : up to 200 kbit/s

Note

A minimum mean data transfer rate for the received data of 2.1 kbits/s (AMPS) and 1.7 kbits/s (TACS) is required to ensure contiguity of message words.

The format for received and transmitted data words is shown in Fig. 14 (a) and Fig. 14 (b) respectively. The receive and transmit data timing is illustrated in Fig. 15 (a) and Fig. 15 (b) respectively.

Transmitter Control (TXCTRL)

TXCTRL is an open-drain output used to disable the transmitter during a Reverse Control Channel access failure.

- output level HIGH : RF enable
- output level LOW : RF disable

Transmitter Audio Enable (TACTRL)

TACTRL is an open-drain digital output signal used to blank the audio path and enable the data path to the modulator during data bursts on the Reverse Voice Channel.

- output level HIGH : audio enabled
- output level LOW : audio muted

Receiver Audio Enable (RACTRL)

RACTRL is an open-drain digital output used to blank the audio path to the earpiece when a sequence of dotting and word sync is detected.

RACTRL and TACTRL functions can be combined using one line.

- output level HIGH : audio enabled
- output level LOW : audio muted

Reverse Control Channel Status (BUSY)

BUSY is a digital output giving the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy-Idle bits and has the following logic levels:

- output level HIGH : channel busy
- output level LOW : channel idle

On a voice channel BUSY indicates channel idle.

Invert Receive Data (INVRX)

Enables an additional inverter in the receive data path. This allows RF demodulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC depends on the receiver local oscillator.

- input HIGH : data inverted
- input LOW : data normal

Invert Transmit Data (INVTX)

Enables an additional inverter in the transmit data path. This allows RF modulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the modulated data stream depends on the transmitter local oscillator.

- input HIGH : data inverted
- input LOW : data normal

EXTERNAL PIN DESCRIPTION (continued)

Transmitted Data Output (DATA)

Data is an analog output which provides Manchester encoded and filtered data signal SAT and signalling tone. This signal should normally be AC coupled into the Audio/Data summer.

- DC level : analog ground (AGND)
- signal level : 2 V (p-p) * for signalling tone
- signal tolerance : 2% + supply voltage variation (ΔV_{DD})
- minimum load impedance : 10 kΩ
- maximum load capacitance : 2 nF
- maximum output impedance : 50 Ω

Received Data Input (DEMODD)

Demodd inputs analog data and SAT signals from the RF demodulator. This pin should normally be AC coupled (characteristics for UMA1000T/F4 upwards).

- DC level : analog ground (AGND)
- maximum data level : 1 V (p-p)
- nominal data level : 250 mV (p-p)
- minimum data level : 200 mV (p-p)
- minimum SAT level : 50 mV (p-p)
- input impedance : > 1 MΩ

CHARACTERISTICS OF THE I^2C BUS

The I^2C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

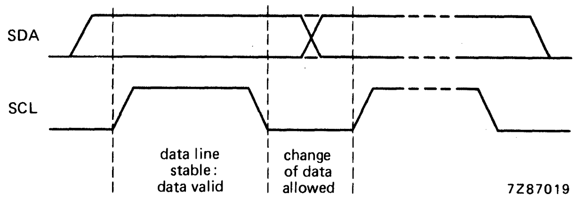


Fig. 7 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

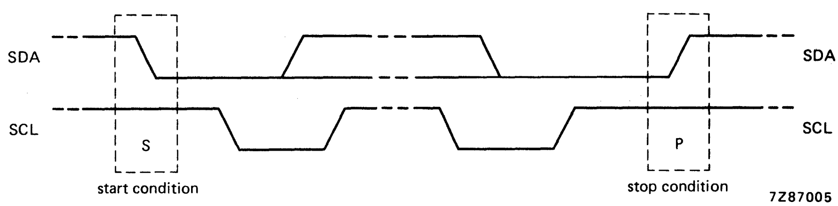


Fig. 8 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

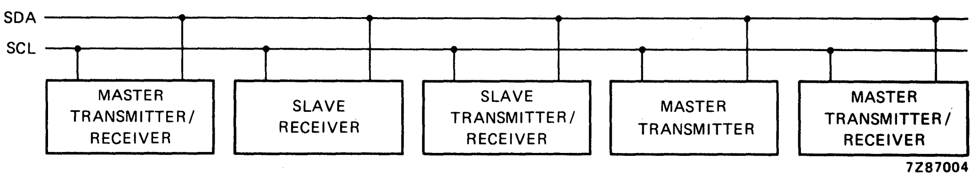


Fig. 9 System configuration.

CHARACTERISTICS OF THE I²C BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

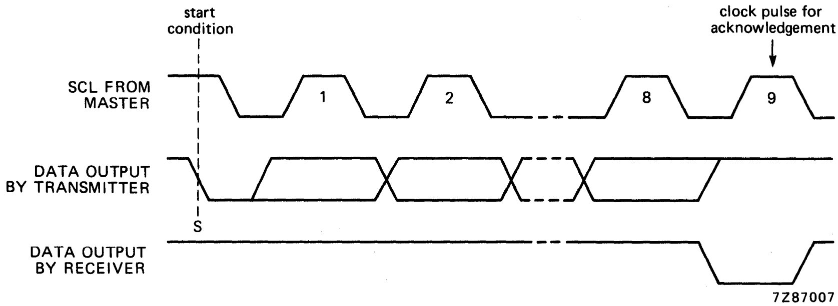


Fig. 10 Acknowledgement on the I^2C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 11.

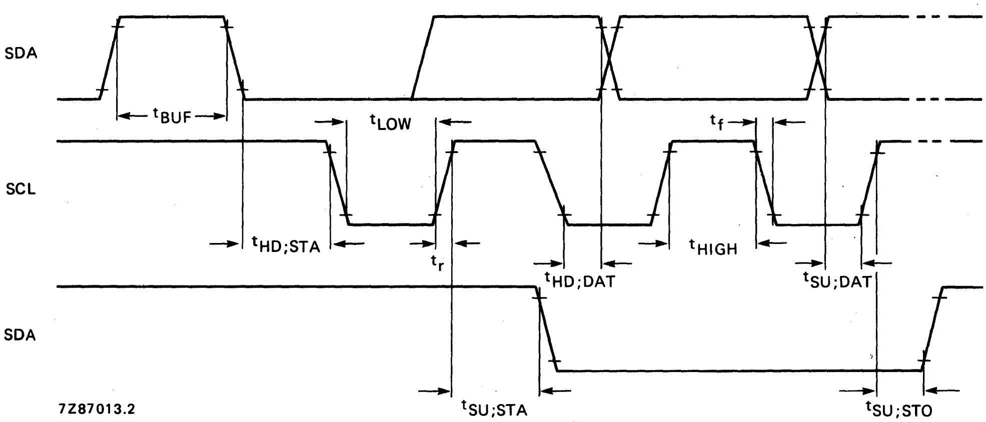


Fig. 11 Timing.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD; STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4.7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU; STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD; DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU; DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU; STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS}.

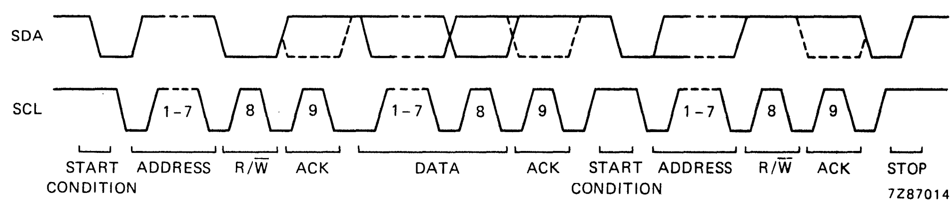


Fig. 12 Complete data transfer.

Where:

Clock t_{LOWmin}	4.7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Max. number of bytes	Unrestricted
Premature termination of transfer	Allowed by generation of STOP condition
Acknowledge clock bit	Must be provided by the master

I²C REGISTERS

General

The I²C register block resides internally within the I²C interface block and contains various items of status and control information which are transferred to and from DPROC via the I²C-bus. The block is organized into four 8-bit registers:

- Status Register — contains read only items
- Control Register
- SAT Programmable Phase Shift Register
- TEST Register

(Control, SAT Programmable Phase Shift and TEST Registers: contain write only items)

Note

In normal operation the SAT delay register and the TEST register require programming only after a device reset.

Table 3 Register map

register	bit 7	6	5	4	3	2	1	0
status	–	–	WSYNC	BUSY	TXABRT	TXIP	MSCC1	MSCC0
control	–	SERV	STS	TXRST	ABREN	FVC	STEN	SATEN
SATD	<---------- SAT delay data ---------->							

S	DPROC ADR	R	A	STATUS	A	P

(a) read from DPROC status register

S	DPROC ADR	W	A	CONTROL	A	P

(b) write to DPROC control register

S	DPROC ADR	W	A	CONTROL	A	SAT DELAY	A	TEST	A	P

(c) write to all DPROC registers

Where:

S	: START condition
W	: read/write bit (logic 0 = write)
R	: read/write bit (logic 1 = read)
A	: acknowledge bit
P	: STOP condition
DPROC ADR	: slave address of DPROC
TEST	: must be programmed to logic 0 for normal operation

Fig. 13 I²C data format.

Status Register

This is a read only register containing DPROC status information.

Measured SAT Colour Code (MSCC1; MSCC0)

MSCC1 and MSCC0 provide information about the current measured SAT colour code in accordance with Table 4.

Table 4 Measured SAT Colour Code

MSCC1	MSCC0	SAT frequency (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

Transmission In Progress (TXIP)

TXIP indicates whether DPROC is currently accessing the Reverse Control or Voice Channels.

- logic 1 : data transmission in progress
- logic 0 : transmission not in progress

Transmission Abort Status (TXABRT)

TXABRT indicates that a Reverse Control Channel Access Attempt has been aborted by DPROC without successful message transmission.

- logic 1 : transmission attempt aborted
- logic 0 : no access collision detected

Reverse Control Channel Status (BUSY)

BUSY gives the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy-Idle bits on the Forward Control Channel.

- logic 1 : channel busy
- logic 0 : channel idle

On a voice channel the BUSY bit defaults to the set state.

Note

This signal is also routed to the BUSY output pin.

Word Synchronization Indicator (WSYNC)

WSYNC indicates whether DPROC has acquired frame synchronization according to the Forward Control Channel format.

- logic 1 : frame synchronization acquired
- logic 0 : no frame synchronization

I²C REGISTERS (continued)

Control Register

This is a write only register containing DPROC control information.

SAT Path Enable (SATEN)

SATEN enables the SAT transponded signal to be output on external pin DATA.

- logic 1 : SAT tone enabled
- logic 0 : SAT tone inhibited

Signalling Tone (ST) Path Enable (STEN)

STEN enables the Signalling Tone to be output on external pin Data.

- logic 1 : ST enabled
- logic 0 : ST inhibited

Channel Format Select (FVC)

FVC selects the required channel format.

- logic 1 : Voice channel format
- logic 0 : Control channel format

Transmission Abort Permission (ABREN)

ABREN indicates whether DPROC has permission to abort data transmission and disable RF on the Reverse Control Channel following the detection of a channel access attempt collision.

- logic 1 : RF disable allowed
- logic 0 : RF disable inhibited

Message Transmission Abort (TXRST)

TXRST terminates a message being transmitted on the reverse channel. It is a monostable signal which when activated causes a reset of the message transmission circuitry and causes TXABRT and TXIP I²C signals to be reset.

This signal does not clear the DPROC transmit register; therefore if a word has been loaded into DPROC after a TXABRT has occured the control line TXHOLD should be held LOW to allow the word to be cleared from the DPROC input register.

- logic 1 : reset active
- logic 0 : reset inactive

System Type Select (STS)

STS selects required system format.

- logic 1 : AMPS
- logic 0 : TACS

Note

Toggling this signal also resets the receive logic in DPROC.

Serving System Select (SERV)

SERV selects which of the serving system data streams (A or B) is accepted.

- logic 1 : system A selected
- logic 0 : system B selected

SAT Programmable Delay Register (SATD)

SATD programs the value of phase shift which is applied to the SAT tones in the SAT Regeneration Block. This value will be determined and programmed into the System Controller during manufacture. The recovered SAT is delayed in time by approximately 0.8 μs x value in the register which corresponds to approximately 1,8 degrees x value in the register. The total phase shift is limited to 360 degrees.

The ability to adjust SAT phase angle is not necessary in current AMPS and TACS systems. Therefore this register should normally be in AMPS and TACS, this function is not necessary and should programmed to zero.

DIGITAL CIRCUIT BLOCKS

General

The majority of the digital circuitry within the DPROC device is identical for both AMPS and TACS. The device has little additional redundancy to implement both systems. The functions of these blocks are described in the following sections and relate to those shown in Fig. 1.

Data Recovery

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Strobed Comparator Block, on which it performs the following functions:

- clock recovery
- Manchester decoding
- data regeneration

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase locked clock signal from the Manchester encoded data stream. This is implemented using a digital-phase-locked-loop (PLL) which has an adjustable "bandwidth" to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1.2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output. The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a 1 otherwise it is latched as a 0.

SAT Processing

The Supervisory Audio Tone processing consists of the following functions:

- SAT recovery
- SAT determination
- SAT regeneration

SAT recovery

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.
The recovery is performed using a digital phase-locked-loop.

SAT determination

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and the SAT not valid events. The result is then coded into the I^2C status registers MSCC0 and MSCC1 as shown in Table 5.

Table 5 Status registers MSCC0, MSCC1; decoded SAT frequencies

register		SAT frequency band (Hz ± 4 Hz)	decoded SAT (Hz)
MSCC0	MSCC1		
1	1	< 5956	not valid
0	0	5956 to 5986	5970
0	1	5986 to 6014	6000
1	0	6014 to 6046	6030
1	1	> 6046	not valid

SAT regeneration

The SAT Regeneration Block generates a digital SAT stream from the recovered SAT stream for transponding back to the base station. The AMPS and TACS specifications require the SAT to be transponded with a maximum phase shift of 20 degrees between the point the modulated RF signal enters the mobile from the base station, and the point the modulated RF leaves the mobile. A variable phase compensation circuit is provided in DPROC to shift the recovered SAT through 0 to 360 degrees before being passed to the output summing network. The degree of phase shift is determined during manufacture of the set and the required additional phase shift is stored in non-volatile RAM and programmed via I^2C at each power-on cycle. The phase correction is performed by a counter delay method using signals which are phase locked to the recovered SAT.

Dotting Detector

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of 32 bits of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked-loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL, after a Word Synchronization Block has been received, for the duration of the burst.

Word Synchronization Detector

The Word Synchronization Block performs the following functions:

- Frame synchronization
- Reverse Control Channel status (B/I determination)
- Valid Serving System determination

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word. This synchronization word is an 11 bit-Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROC has achieved frame synchronization. In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode. On the Forward Voice Channel detection of the synchronization word indicates that the following 40 bits are valid data. Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word. The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

Majority Voting Block

The Majority Voting Block performs the following functions:

- identifying position and validity of frames in the received data stream
- extracting 5 repeats of each word from a valid frame
- performing a bit-wise majority decision on the five repeats of the data word

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROC is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searched for and extracted by DPROC. On the forward Voice Channel DPROC will extract the first five words that occur for which a correct synchronization word is found. These words can occur in any position in the frame. A serial majority vote is performed as the fifth word is being extracted.

Error Correction Block

The Error Correction Block performs the following functions:

- extraction of a valid message from the Majority-Voted Word
- computation of the S1 and S3 syndromes
- correction of up to one error in the word
- communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic equations:

$$1 + X + X^6 \text{ and } 1 + X + X^2 + X^4 + X^6$$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROC only corrects up to one error although the code used has a Hamming distance of five. The occurence of two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

Received Data Serial Link

The Received Data Serial Link transfers data and control information from DPROC to the System Controller. The data is transferred on RXLINE under control of a clock signal RXCLK, generated by the System Controller. The system controller is informed of the arrival of a decoded data word in the DPROC output register by RXLINE being driven LOW. If the system controller chooses to ignore the received data or only partially clock the data out, the DPROC will reset the receive buffer for the next word after the period RWIN (see Fig. 15).

Data Format

Each Received Data word consists of 4 bytes. The word format is shown in Fig. 14 (a). The sense and function of the fields is shown in Table 6.

Table 6 Received Data word

bit	title	sense	function
31	start	LOW	identifies start of word
30	BCH error	active HIGH	indicates that an uncorrected BCH error is associated with the word
29 to 2	received data	binary data	received data word
1	RXLINE error	LOW	if detected as HIGH indicates that a transmission error has occured on the microprocessor to DPROC serial link
0	stop	HIGH	identifies end of the word

Link Protocol

The Received Data protocol is described by the timing diagram Fig. 15 (a) and has the following parameters:

- maximum receive window (RWIN)
  Control Channel (TACS) = 47 ms
  Control Channel (AMPS) = 37 ms
- minimum clock period ($t_{CLK(min)}$ = 2 μs
- minimum clock hold-off (t_{WAIT}) = 100 μs

Transmit Data Serial Interface

The Transmit Data Serial Link performs reception of data from the System Controller to DPROC over a dedicated line TXLINE. The transfer of data is synchronous with a clock signal TXCLK, generated by the System Controller.

Data Format

Each Transmit Data word consists of 5 bytes. The word format is shown in Fig. 14 (b). The sense and function of the fields is shown in Table 7.

Table 7 Transmit Data word

bit	title	sense	function
39	start	LOW	identifies start of word
38, 37	DCC	binary data	digital colour code
36 to 1	transmit data	binary data	transmit data word
0	stop	HIGH	identifies end of the word

Link Protocol

Messages are normally up to 5 words in length on the Reverse Control Channel and up to 2 words in length on the Reverse Voice Channel. However, DPROC will transmit messages of any word length. These must be transmitted on the data stream without interruption. To avoid the need for large buffer areas, a flexible protocol is used to allow DPROC to control the transfer of data words. DPROC has an on-chip buffer which can hold one complete word of a message. Whilst new words are being loaded into DPROC, within the time period Buffer clear to end of TWIN, DPROC will maintain uninterrupted data transmission. The System Controller can abort the transmission of a message at any point activating the I^2C signal TXRST. This signal causes the interface to return to its power-up state and resets TXIP and TXABRT (see Table 3). On completion of these tasks TXRST will return to its inactive state. The Transmit Data Protocol is described by the timing diagram shown in Fig. 15(b) and has the following parameters:

- maximum transmit window (TWIN)
  - voice channel (TACS) = 60 ms
  - voice channel (AMPS) = 48 ms
  - control channel (TACS) = 29 ms
  - control channel (AMPS) = 23 ms
- minimum clock period ($t_{CLK(min)}$) = 2 μs

MSB					LSB
START	BCH ERROR	RECEIVED WORD (28 bits)		CHECK BIT (= 0)	STOP
Bit 31	Bit 30	Bit 29	Bit 2	Bit 1	Bit 0

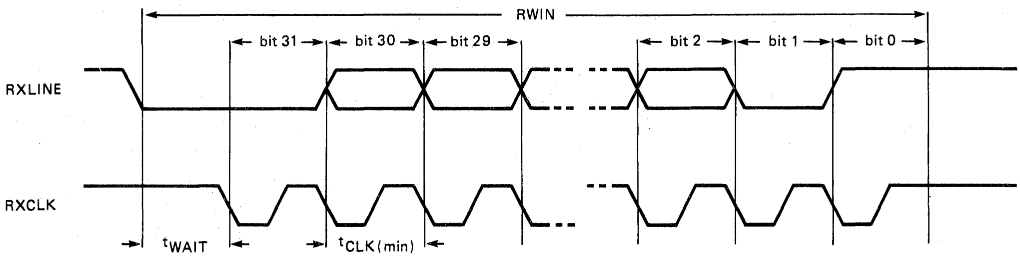
(a) received data word

MSB						LSB
START	DCC 1	DCC 0	TRANSMIT WORD (36 bits)			STOP
Bit 39	Bit 38	Bit 37	Bit 36		Bit 1	Bit 0

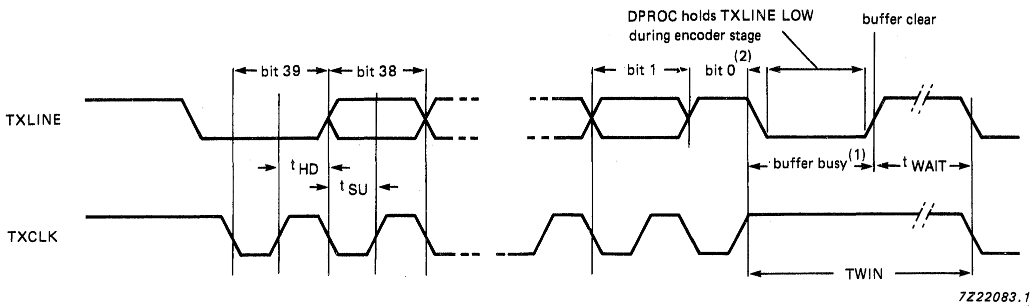
(b) transmit data word

Fig. 14 Data word formats.

DIGITAL CIRCUIT BLOCKS (continued)



(a) DPROC to microcontroller link; receive data timing.



Where:

t_{HD} = 100 ns minimum
t_{SU} = 0 ns minimum
t_{WAIT} = 0 ns minimum

(b) Microcontroller to DPROC link; transmit data timing.

(1) The buffer busy time depends on whether the first or subsequent words are being loaded.

(2) The system controller should monitor the TXLINE during bit 0, if the status of TXLINE does not change from a HIGH to a LOW on the rising edge of TXCLK, then a framing error has occured. This can be caused by glitches on the clock line or if an arbitration error occured while the DPROC transmit register was being loaded. The system controller should recover the situation by holding TXLINE HIGH and supplying clocks on TXCLK until TXLINE goes LOW. Then the situation should be treated as a normal channel arbitration failure as described in **Reverse Control Channel Access Arbitration** — Abort Procedure.

Fig. 15 Data timing diagrams.

BCH and Manchester Encoding Block

The functions performed by this circuit block include:

- reception of data from the System Controller
- parity generation
- message construction
- Manchester encoding

Each 36-bit Information Word sent on the Reverse Voice and Control Channels is coded into a 48 bit code word. The code word consists of the 36-bit word followed by 12 parity bits. These parity bits are formed by clocking the information word into a 12-bit feedback shift register with characteristic equation:

$$1 + X^3 + X^4 + X^5 + X^8 + X^{10} + X^{12}$$

The BCH Encoder Block constructs the Reverse Voice and Control Channel data streams from the information it receives from the System Controller.
The streams are formed out of the four possible field types:

- Dotting (data inversions)
- 11-bit Synchronization Word
- Digital Colour Code
- 48-bit code word

The 2 bits of DCC received from the System Controller are coded into a 7-bit word as shown in Table 8.

Table 8 Digital Colour Code; 7-bit word

DCC1	DCC0	Coded DCC						
0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1
1	0	1	1	0	0	0	1	1
1	1	1	1	1	1	1	0	0
		DCC1		DCC0			DCC1.EXOR.DCC0	

The data sense for Manchester Encoding has a NRZ logic 1 encoded as a 0-to-1 transition and a NRZ logic 0 encoded as a 1-to-0 transition.

DIGITAL CIRCUIT BLOCKS (continued)

Reverse Control Channel Access Arbitration

The AMPS and TACS specifications require a method of arbitration on the Reverse Control Channel to prevent two mobiles from transmitting on the same channel at the same time. This function is performed by DPROC monitoring the Busy/Idle stream sent on the Forward Control Channel.

The AMPS and TACS specifications state that once the mobile has commenced transmitting on the Reverse Control Channel it must monitor the Busy/Idle stream. If this stream becomes active outside a predetermined 'window', measured from the start of the transmission of the message, the mobile must terminate its transmission and disable the transmitter immediately.

In the Cellular Radio chip-set there are two levels of control of the RF transmitter; the first is absolute control by the System Controller, the second is conditional by other devices in the set. In DPROC the conditional control of the transmitter is performed via the output TXCTRL. This line is effectively wired ANDed together, using open-drain outputs, with other devices which may wish to control the transmitter. When these devices do not wish to disable the transmitter their output is in a HIGH impedance state.

An exception to this procedure occurs when the Serving System instructs the mobile not to monitor the Busy/Idle bits. In this event the arbitration logic can be disabled by clearing I^2C register bit ABREN.

The flow of events during a Control Channel Access attempt is as follows:

Initial State

- transmitter power off via I^2C
- DPROC transmit circuitry in power-up state
- TXCTRL line HIGH

Access Attempt Procedure

1. System Controller decides to send message (note 1).
2. System Controller drives TXCTRL low directly.
3. System Controller switches transmitter power on and waits for power-up for the transmitter module (RF transmitter is still disabled by TXCTRL).
4. System Controller sets TXRST via I^2C to DPROC.
5. System Controller sets ABREN via I^2C (if required) allowing DPROC to control the transmitter.
6. System Controller determines status of Reverse Control Channel by monitoring the Busy/Idle bit. If busy, waits a random time then tries again.
7. System Controller releases TXCTRL allowing it to be pulled HIGH enabling the transmitter output.
8. System Controller transfers the first word of the message to DPROC via serial link (note 1).
9. DPROC sets I^2C signal TXIP and starts sending message while monitoring Busy/Idle status.
10. If channel becomes busy before 56 bits and ABREN is set then perform Abort Procedure.
11. If channel remains idle after 104 bits and ABREN is set then perform Abort Procedure.
12. System controller loads the subsequent words of the message into DPROC when the buffer becomes clear (Fig.15b).
13. On completion of entire message DPROC clears TXIP and 25 ms later the System Controller disables transmitter via I^2C.
14. System Controller finally sends TXRST to prepare DPROC for next transmission.

Note to the Access Attempt Procedure

1. At stage 1 the system controller may choose to preload DPROC with the first word of the message and hold it from transmission until stage 7 using the TXHOLD line. This gives a lower time overhead between detecting an IDLE channel and commencing the transmission. To use this feature TXHOLD must be driven HIGH before the last bit of data has been transferred into DPROC.
   Figure 16 illustrates the DPROC data transmission timing.

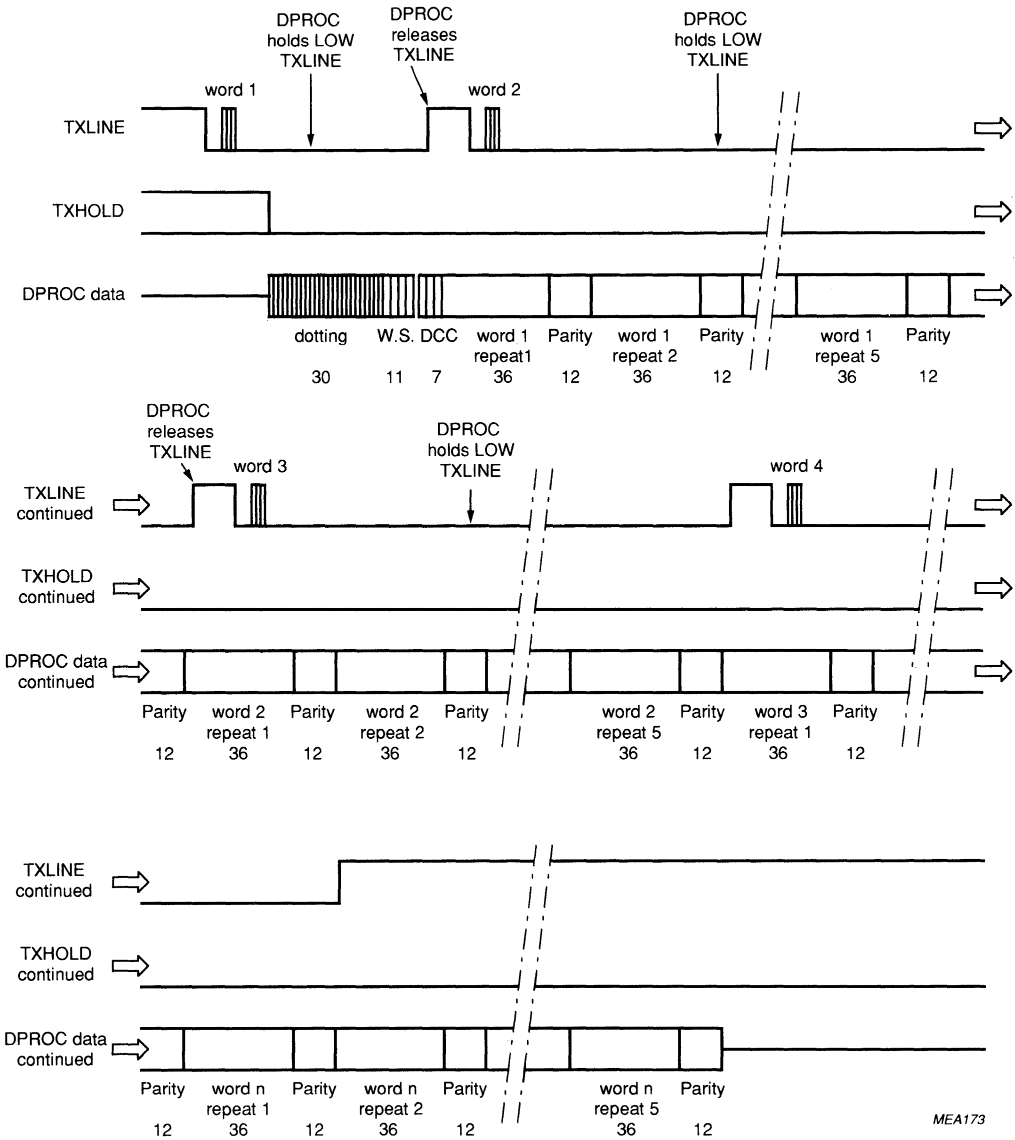


Fig. 16 DPROC data transmission timing/microcontroller interface.

DIGITAL CIRCUIT BLOCKS (continued)

Abort Procedure (see Fig. 17)

1. DPROC immediately disables transmitter output by driving TXCTRL low.
2. DPROC sets TXABRT.
3. System Controller detects failure by monitoring TXCTRL and TXABRT.
4. System Controller disables transmitter via RF power amplifier.
5. System Controller sends TXRST to prepare DPROC for next transmission.

Note

If a message is loaded into DPROC after a TXABRT has occured this word will remain in the DPROC transmit register and will not be cleared to TXRST.
If this situation arises the method of clearing the buffer ready for a second access attempt is to leave TXHOLD LOW and then send a TXRST prior to setting up a new transmission after TXLINE goes HIGH; this will clear any residual data in the buffer.

Signal Tone Generation (ST)

The 8 or 10 kHz (TACS or AMPS) tone generated from the Manchester Encoding Block is used as the Signalling Tone stream.

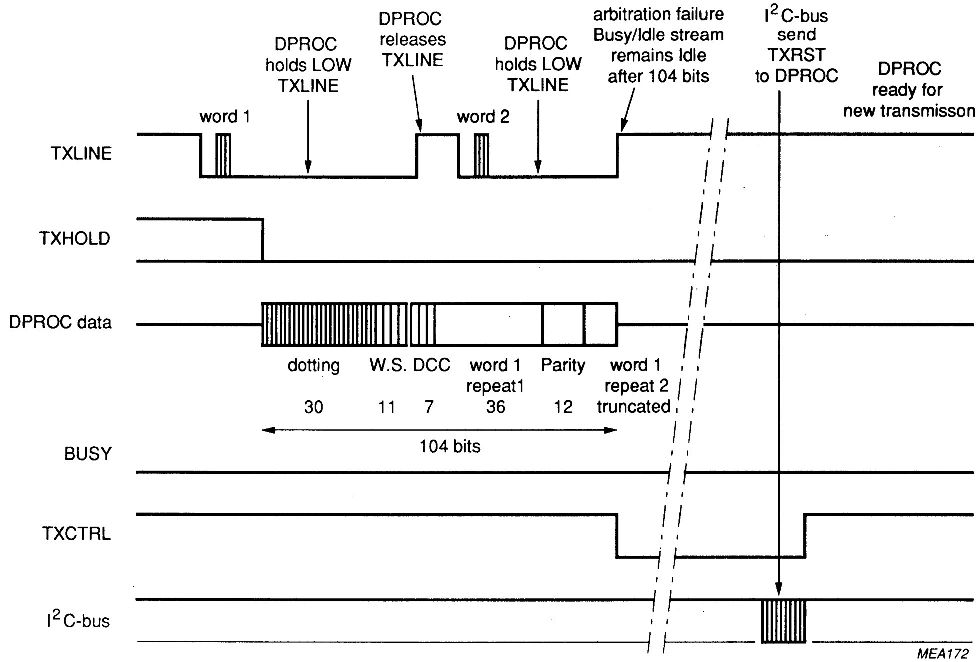


Fig. 17 DPROC data transmission timing/microcontroller interface during arbitration failure.

ANALOG CIRCUIT BLOCKS

General

The analog signal processing functions on DPROC are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by distributed RC active filters, passive interpolators and comparators.

The distributed RC sections, the Anti-Alias Filter and the Clock Noise Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolators increase the sampling rate from 300 kHz to 1.2 MHz. The sampled analog signals from the Passive Interpolators are converted to sampled 2-state digital signals by the Strobed Comparators. The Gated Digital-to-Analog converters and Analog Summer blocks perform resynchronization and sub-sampling of the digitally generated DPROC output signals, and conversion to the sampled analog domain.

These analog section of the device are shown in Fig. 1.

Reference Voltage Generator

The Reference Voltage Generator generates the analog ground reference voltage (AGND) used internally within the DPROC device. To minimize noise AGND must be externally decoupled to V_{SSA} as shown in Fig. 18.

Anti-Alias Filter

The Anti-Alias Filter is placed before the SAT sampling block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Alias Filter is a continuous time-distributed RC-active low-pass filter.

SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the switched-capacitor filters. This reduces the coarseness of the zero crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

Strobed Comparators

The Strobed Comparators form the analog-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers wich convert the filtered sampled analog signals into 2-state sampled digital signals containing only the zero-crossing information from the analog signal.

Gated Digital-to-Analog and Analog Summer

The Gated Digital-to-Analog converters and Analog Summer form the interface between the digital and analog circuitry on the transmit path of DPROC. It is at this point that the three sampled digital signals, containing SAT, ST and encoded digital data, are combined to form a composite signal.
The data streams are enabled by the I^2C signals STEN, SATEN and the internal signal DATAEN respectively (DATAEN disables SAT and ST when data is being transmitted). The digital-to-analog conversion and sub-sampling operation is performed by the Gated Digital-to-Analog converters and Analog Summer. The relative signal weights applied in the summer (with respect to the data path) are shown in Table 9.

Table 9 Relative signal weights

signal	relative output level AMPS and TACS
ST	1.0
SAT	0.25
DATA	1.0

Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROC output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC coupling from the DATA pin.

Clock Noise Filter

The filter is a non-critical continuous time-distributed RC-active low-pass filter used to remove any switching transient residues from the output signal.

APPLICATION INFORMATION

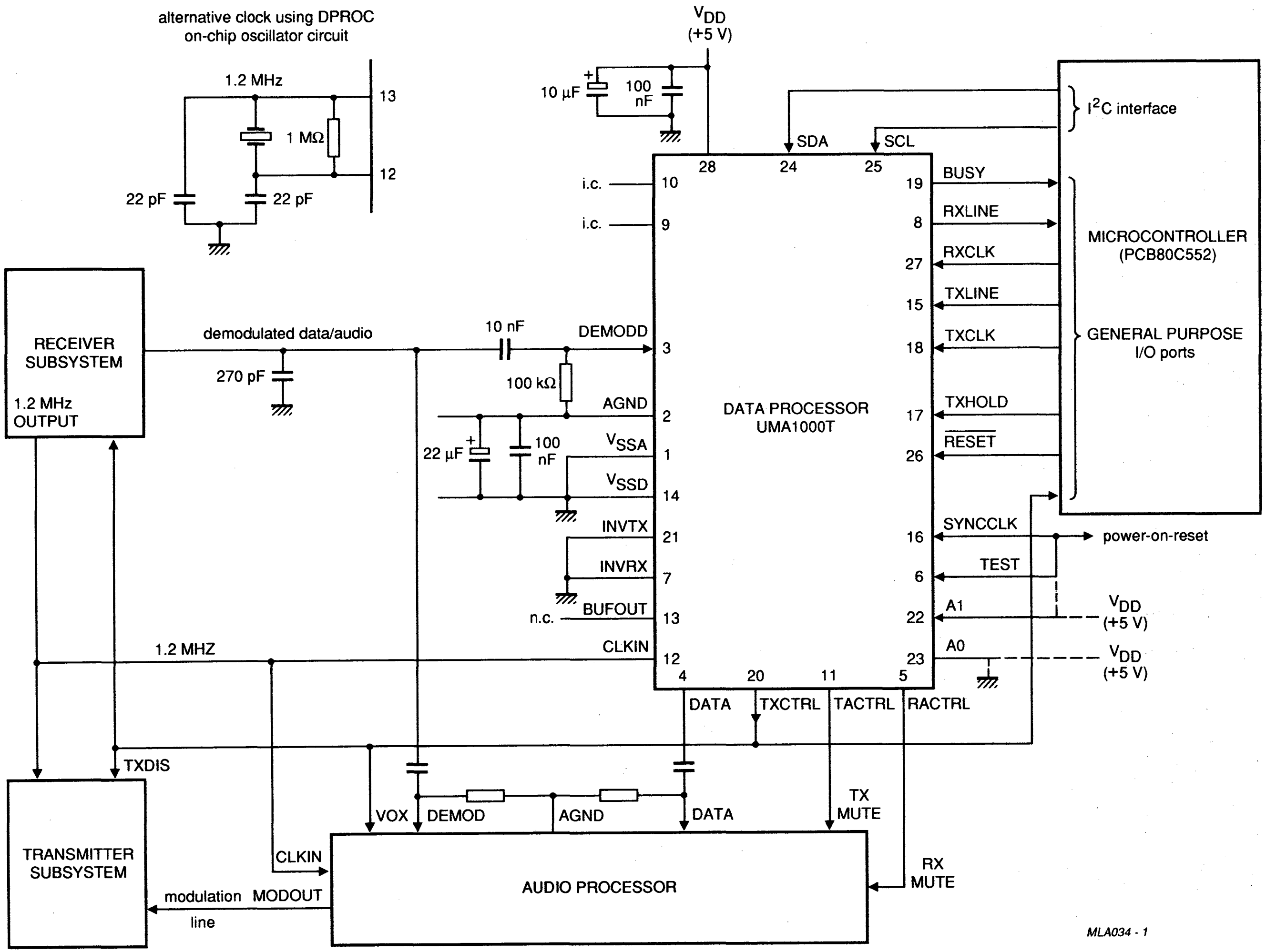


Fig. 18 DPROC application circuit.

Signetics

Section 6
Frequency Synthesizers, Pagers, and Data Receivers

RF Communications

INDEX

Divide by: 128/129-64/65 dual modulus low power ECL prescaler

NE/SA701

DESCRIPTION

The NE701 is an advanced dual modulus (Divide By 128/129 or 64/65) low power ECL prescaler. The minimum supply voltage is 2.5V for compatibility with the new CMOS UMF1005 and UMF1009 synthesizers from Philips and other logic circuits. The maximum supply current is 2.8mA allowing application in battery operated low-power equipment. Maximum input signal frequency is 1.2GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the HS4+ process (the bipolar portion of the QUBiC process). The circuit will be available in an 8 pin SO package with 150 mil package width.

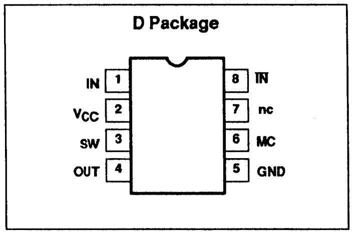
FEATURES

- Low voltage operation
- Low current consumption
- Operation up to 1.2GHz

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO (Surface-mount)	0 to +70°C	NE701D
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA701D

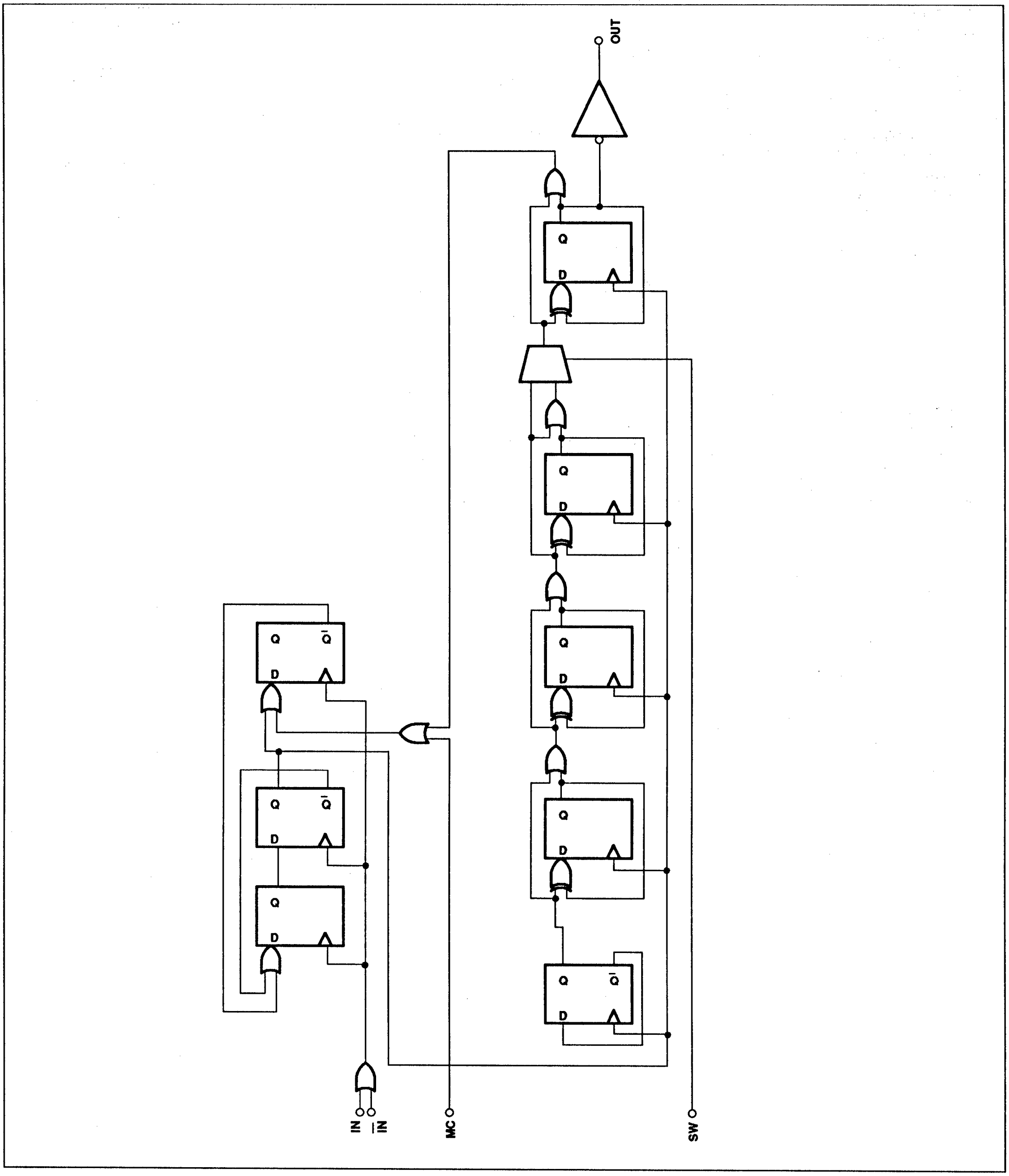
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to V_{CC}	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance	90	°C/W

Divide by: 128/129-64/65 dual modulus low power ECL prescaler

NE/SA701

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for -40°C < T_A < +85°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.5		6.0	V
I_{CC}	Supply current				2.8	mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level	$V_{CC} \geq 3.2V$			V_{CC}-3.0	V
		V_{CC} < 3.2V			0.2	V
V_{IH}	MC input high threshold	I_{MC} = 60μA	2.0			V
V_{IL}	MC input low threshold	I_{MC} = 20μA			0.8	V
I_I	MC input current	$V_{MC} = V_{CC}$ = 5.0V			150	μA
V_{IH}	SW input high threshold		2.0			V
V_{IL}	SW input low threshold				0.8	V
I_I	SW input current	$V_{SW} = V_{CC}$ = 5.0V			100	μA

AC ELECTRICAL CHARACTERISTICS

The following AC specifications are valid for V_{CC} = 3.0V, -40°C < T_A < +85°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude	1000pF input coupling	0.1		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input	0		1.2	GHz
		1000pF input coupling			1.2	GHz
R_{ID}	Differential input resistance	DC measurement	5			kΩ
C_I	Input capacitance				TBD	pF
V_O	Output voltage	V_{CC} = 5.0V	1.6			V_{P-P}
		V_{CC} = 3.0V	1.2			V_{P-P}
t_S	Modulus set-up time	f_{IN} = 1.2GHz		TBD		ns
t_H	Modulus hold time	f_{IN} = 1.2GHz		TBD		ns
t_{PD}	Propagation time			TBD		ns

DESCRIPTION OF OPERATION

The NE701 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a fixed 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for SW (Modulus Set Switch) input to be set low and MC (Modulus Control) input to be set high in which case the circuit comprises a divide by 128. For divide by 129 the MC singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. Similarly, for divide by 64 and 65 the NE701 will generate those respective moduli with the SW signal forced high, in which the fourth stage of the synchronous divider is bypassed.

A truth table for the modulus values is given below:

Table.

Modulus	MC	SW
128	1	0
129	0	0
64	1	1
65	0	1

For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 for modulus 128/129 or count 32 for modulus 64/65 with delay t_{PD}. The SW input is not designed for synchronous switching.

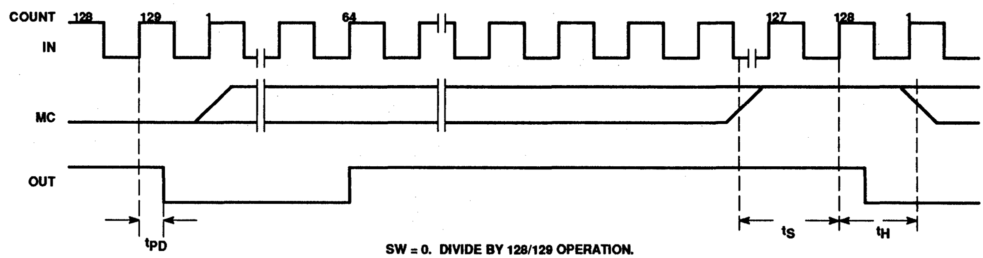
The MC and SW inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed. The SW input has an internal pull-down simplifying modulus group selection. With SW open the divide by 128/129 mode is selected and with SW connected to V_{CC} divide by 64/65 is selected.

The prescaler input is differential and ECL compatible. The output is single-ended ECL compatible.

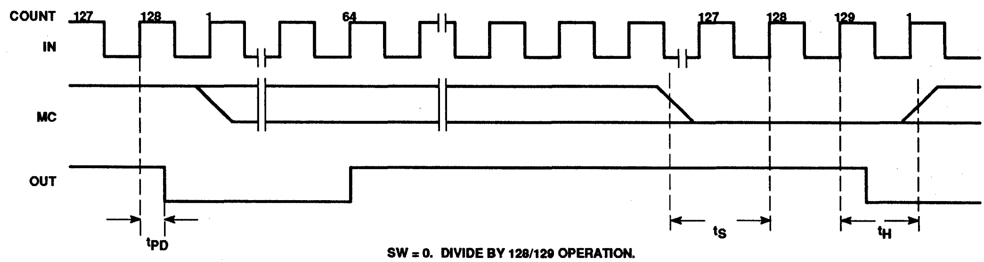
Divide by: 128/129-64/65 dual modulus low power ECL prescaler

NE/SA701

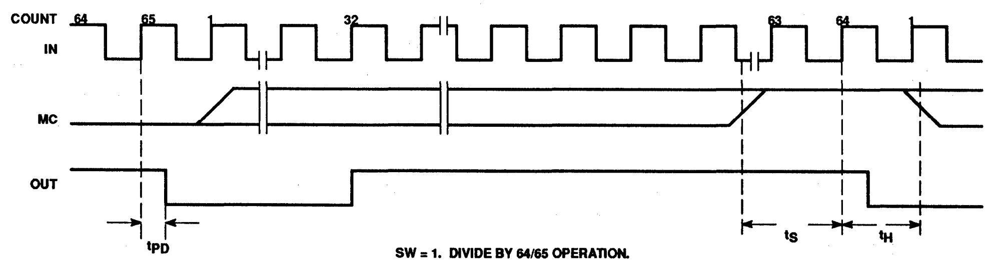
AC TIMING CHARACTERISTICS



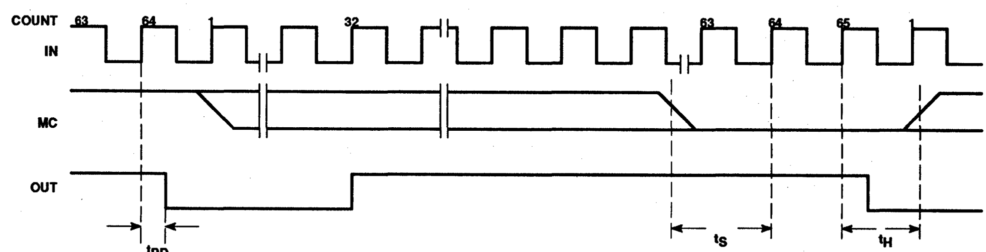
SW = 0. DIVIDE BY 128/129 OPERATION.



SW = 0. DIVIDE BY 128/129 OPERATION.



SW = 1. DIVIDE BY 64/65 OPERATION.



SW = 1. DIVIDE BY 64/65 OPERATION.

Divide by: 64/65/72 triple modulus low power ECL prescaler

NE/SA702

DESCRIPTION

The NE702 triple modulus (Divide By 64/65/72) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.5V for compatibility with the new CMOS UMF1005 and UMF1009 synthesizers from Philips and other logic circuits. The maximum supply current is 2.8mA allowing application in battery operated low-power equipment. Maximum input signal frequency is 1.2GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the HS4+ process (the bipolar portion of the QUBiC process). The circuit will be available in an 8 pin SO package with 150 mil package width.

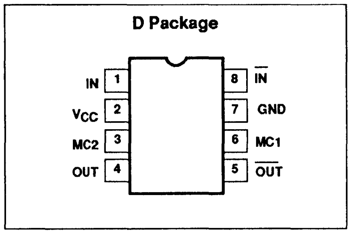
FEATURES

- Low voltage operation
- Low current consumption
- Operation up to 1.2GHz

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION



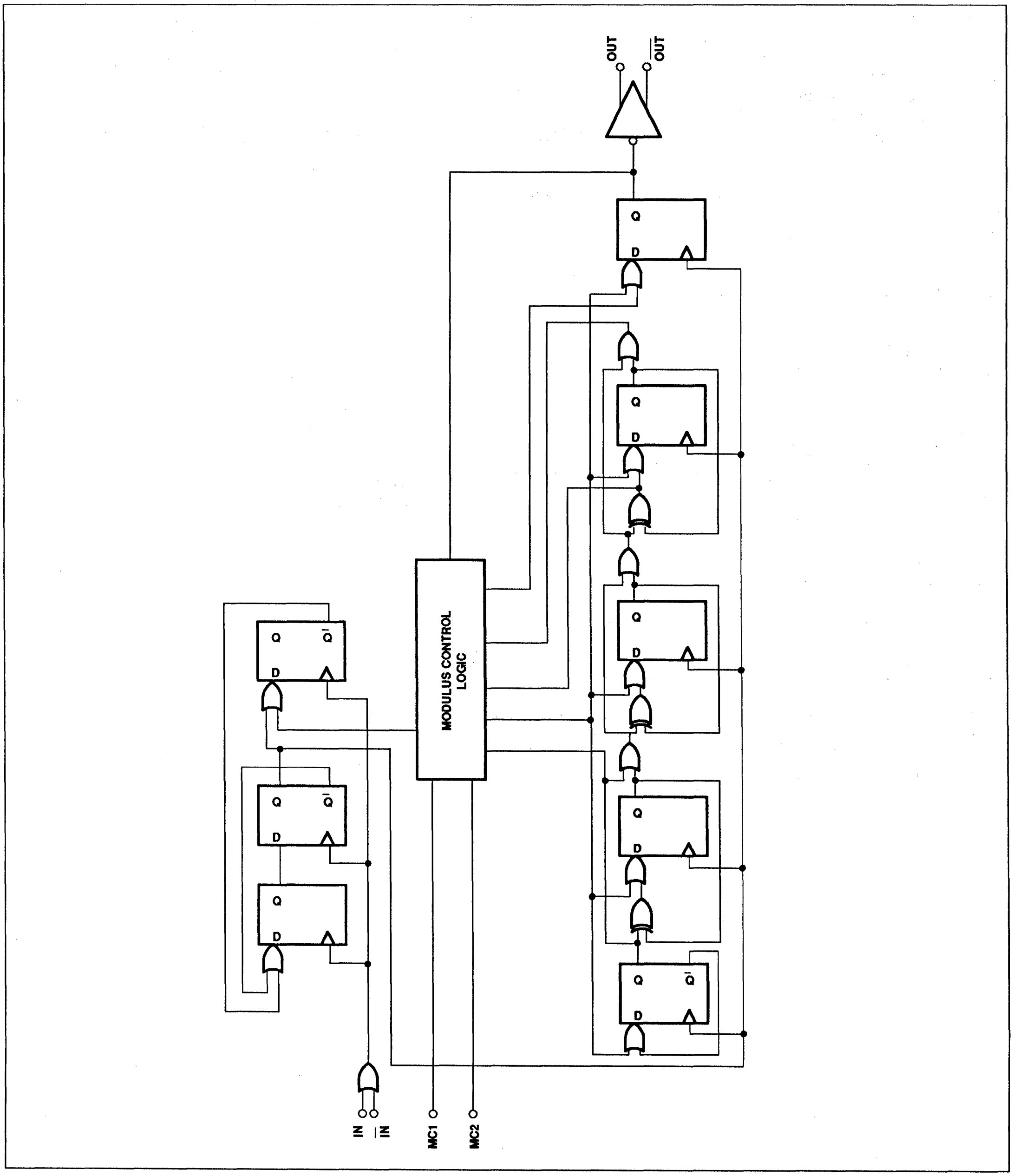
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO (Surface-mount)	0 to +70°C	NE702D
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA702D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to V_{CC}	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance	90	°C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for -40°C < T_A < +85°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.5		6.0	V
I_{CC}	Supply current				2.8	mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level	$V_{CC} \geq 3.2V$			V_{CC}-3.0	V
		V_{CC} < 3.2V			0.2	V
V_{IH}	MC1,2 input high threshold	I_{MC} = 60μA	2.0			V
V_{IL}	MC1,2 input low threshold	I_{MC} = 20μA			0.8	V
I_I	MC1,2 input current	$V_{MC} = V_{CC}$ = 5.0V			150	μA

AC ELECTRICAL CHARACTERISTICS

The following AC specifications are valid for V_{CC} = 3.0V, -40°C < T_A < +85°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude	1000pF input coupling	0.1		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input	0		1.2	GHz
		1000pF input coupling			1.2	GHz
R_{ID}	Differential input resistance	DC measurement	5			kΩ
C_I	Input capacitance				TBD	pF
V_O	Output voltage	V_{CC} = 5.0V	1.6			V_{P-P}
		V_{CC} = 3.0V	1.2			V_{P-P}
t_S	Modulus set-up time	f_{IN} = 1.2GHz		TBD		ns
t_H	Modulus hold time	f_{IN} = 1.2GHz		TBD		ns
t_{PD}	Propagation time			TBD		ns

DESCRIPTION OF OPERATION

The NE702 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 64. For divide by 65 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the sunchronous counter. For divide by 72, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 18. A truth table for the modulus values is given below:

Table.

Modulus	MC1	MC2
64	1	0
65	0	0
72	0	1
72	1	1

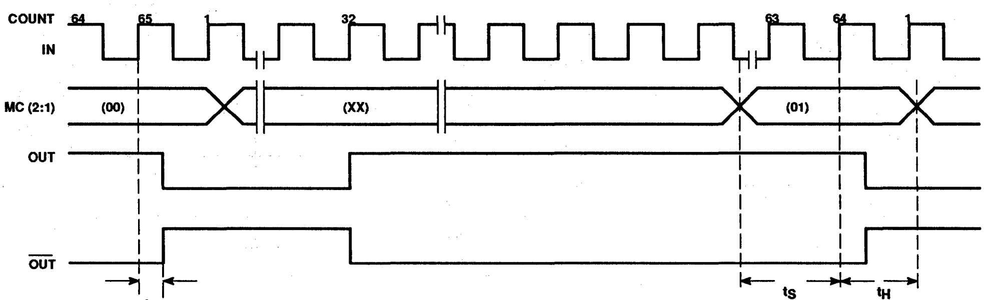
For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 32 with delay t_{PD}.

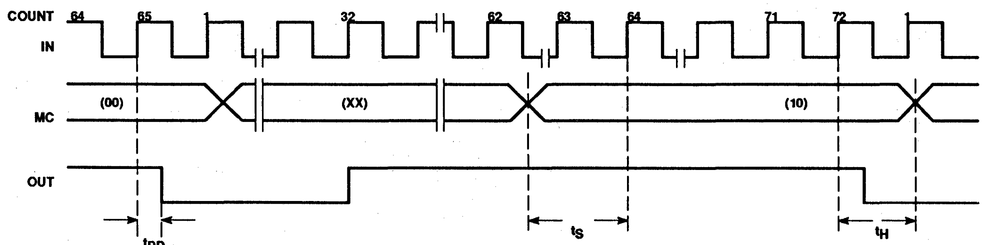
The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

AC TIMING CHARACTERISTICS



SWITCH FROM /65 TO /64



SWITCH FROM /65 TO /72

Divide by: 128/129/144 triple modulus low power ECL prescaler

NE/SA703

DESCRIPTION

The NE703 triple modulus (Divide By 128/129/144) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.5V for compatibility with the UMF1005 and UMF1009 synthesizers from Philips and other logic circuits. The maximum supply current is 2.8mA allowing application in battery operated low-power equipment. Maximum input signal frequency is 1.2GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the HS4+ process (the bipolar portion of the QUBiC process). The circuit will be available in an 8 pin SO package with 150 mil package width.

FEATURES

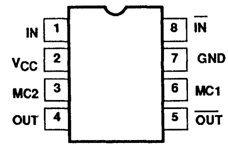
- Low voltage operation
- Low current consumption
- Operation up to 1.2GHz

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION

D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO (Surface-mount)	0 to +70°C	NE703D
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA703D

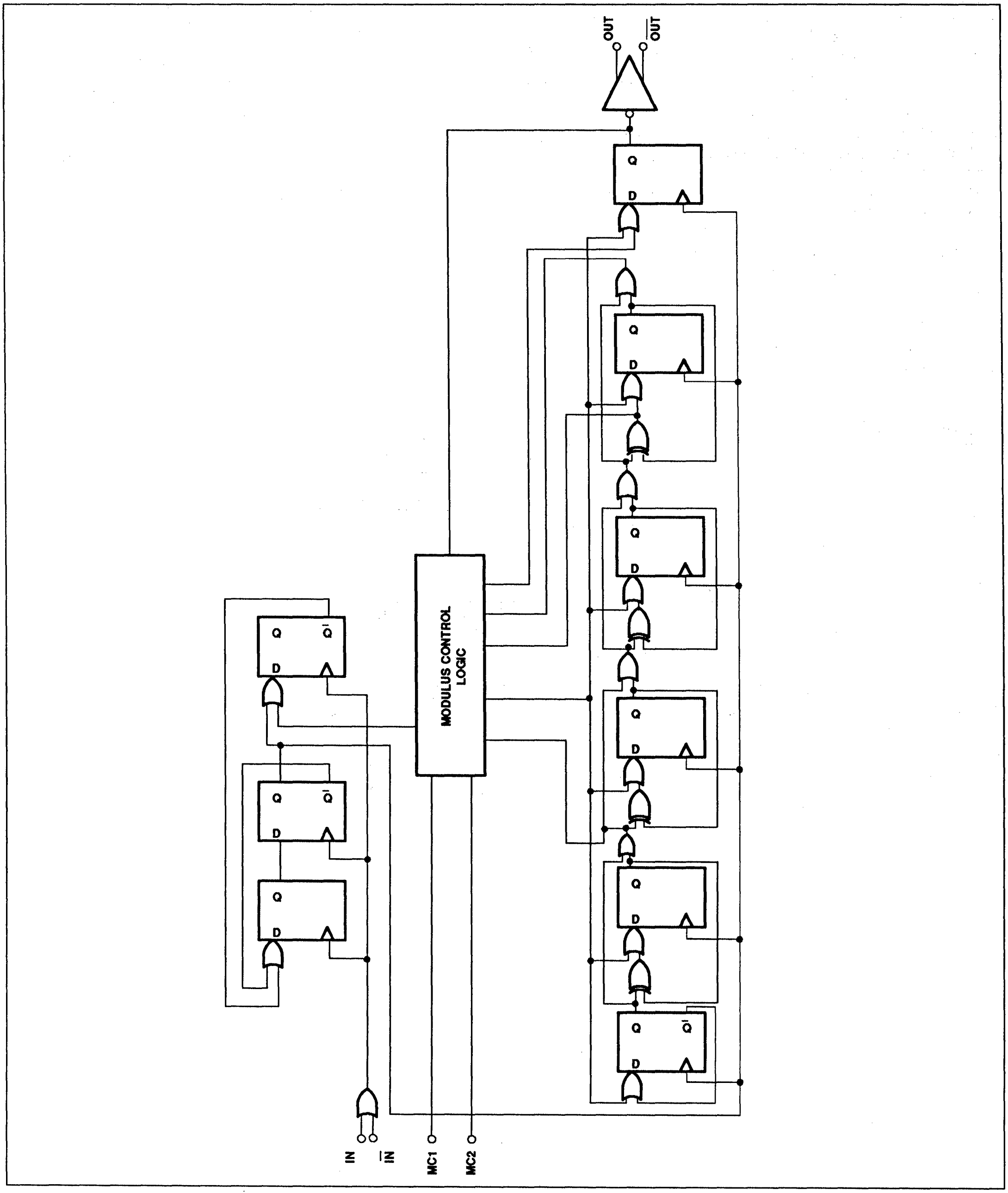
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to V_{CC}	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance	90	°C/W

Divide by: 128/129/144 triple modulus low power ECL prescaler

NE/SA703

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for -40°C < T_A < +85°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.5		6.0	V
I_{CC}	Supply current				2.8	mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level	$V_{CC} \geq$ 3.2V			V_{CC}-3.0	V
		V_{CC} < 3.2V			0.2	V
V_{IH}	MC1,2 input high threshold	I_{MC} = 60μA	2.0			V
V_{IL}	MC1,2 input low threshold	I_{MC} = 20μA			0.8	V
I_I	MC1,2 input current	V_{MC} = V_{CC} = 5.0V			150	μA

AC ELECTRICAL CHARACTERISTICS

The following AC specifications are valid for V_{CC} = 3.0V, -40°C < T_A < +85°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude	1000pF input coupling	0.1		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input	0		1.2	GHz
		1000pF input coupling			1.2	GHz
R_{ID}	Differential input resistance	DC measurement	5			kΩ
C_I	Input capacitance				TBD	pF
V_O	Output voltage	V_{CC} = 5.0V	1.6			V_{P-P}
		V_{CC} = 3.0V	1.2			V_{P-P}
t_S	Modulus set-up time	f_{IN} = 1.2GHz		TBD		ns
t_H	Modulus hold time	f_{IN} = 1.2GHz		TBD		ns
t_{PD}	Propagation time			TBD		ns

DESCRIPTION OF OPERATION

The NE703 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 6 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 128. For divide by 129 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the sunchronous counter. For divide by 144, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 36. A truth table for the modulus values is given below:

Table.

Modulus	MC1	MC2
128	1	0
129	0	0
144	0	1
144	1	1

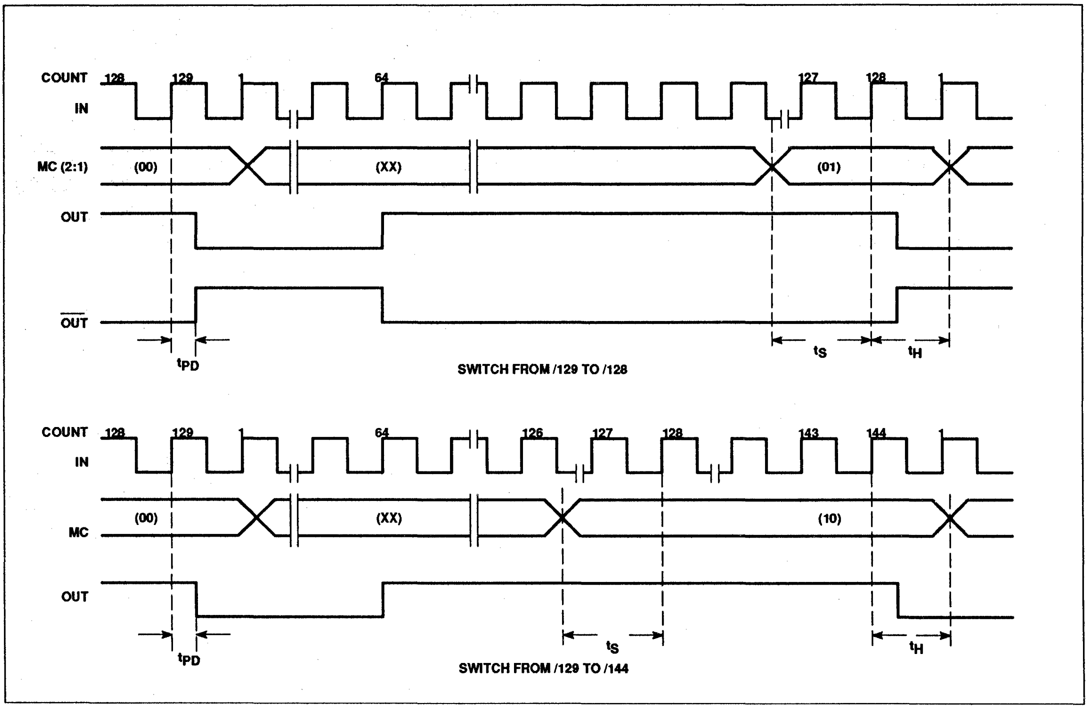
For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 with delay t_{PD}.

The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

AC TIMING CHARACTERISTICS



CMOS frequency synthesizer | TDD1742T

GENERAL DESCRIPTION

The TDD1742T is a low power, high-performance frequency synthesizer in local oxidation CMOS (LOCMOS) technology. The device is designed for use in channelized VHF/UHF applications especially portable and mobile radios.

The circuit incorporates many of the features of the HEF4750V (frequency synthesizer) and HEF4751 (universal divider), including a high-gain phase comparator together with an on-chip sample-and-hold capacitor and phase modulator.

A multiplexed or bus-structured programming sequence allows interface to a microcontroller or external memory (ROM/PROM); power is applied to the memory only when it is required for programming via additional on-chip circuitry.

Operation is possible with a minimum supply voltage of 7 V and a maximum input frequency of 8,5 MHz.

Encapsulation in a 28-lead mini-pack enables the construction of small, low power consumption synthesizers with low noise performance and high side-band attenuation.

Features

- On-chip sample-and-hold capacitor
- Low power consumption
- High-gain phase comparator with low levels of noise and spurious outputs
- Auxiliary digital phase comparator for fast locking
- On-chip phase modulator
- Simple interfacing to external memory
- Microcontroller compatible
- Power-on reset circuitry

QUICK REFERENCE DATA

Supply voltage ranges			
pin 14	$V_{DD1} = V_{14\text{-}6}$		7 to 10 V
pin 8	$V_{DD2} = V_{8\text{-}6}$		4,5 to 5 V
pin 1	$V_{DD3} = V_{1\text{-}6}$		7 to 10 V
Supply current (at T_{amb} = 25 °C; $V_{DD1} = V_{DD3}$ = 7,4 V; V_{DD2} = 5 V)			
pin 14 (phase modulator OFF)	$I_{DD1} = I_{14}$	max.	1,5 mA
pin 8	$I_{DD2} = I_8$	max.	100 μA

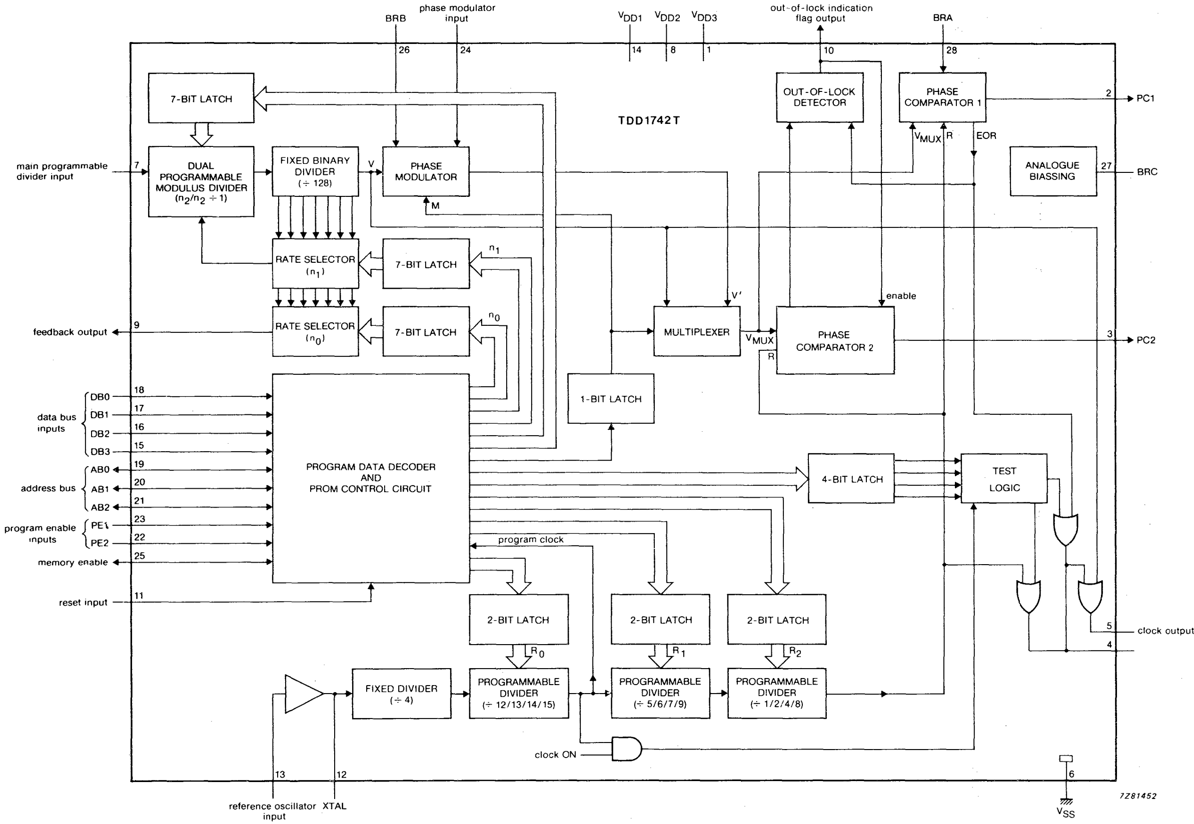


Fig. 1 Block diagram.

PINNING

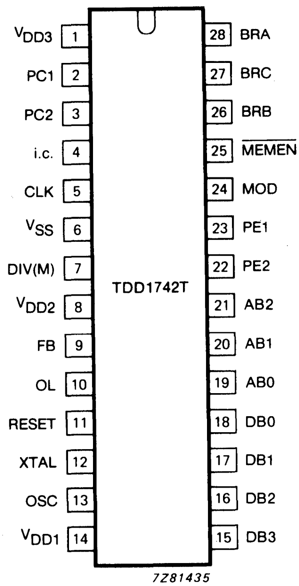


Fig. 2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	V_{DD3}	**Power Supply 3:** analogue supply voltage (7 to 10 V).
2	PC1	**Phase Comparator 1:** high-gain analogue phase comparator output which is used when the system is in-lock to give low levels of noise and spurious outputs.
3	PC2	**Phase Comparator 2:** low-gain digital phase comparator 3-state output which enables the achievement of fast lock times when the system is initially out-of-lock. Phase comparator 2 is inhibited when the phase is within the locking range of phase comparator 1.
4	i.c.	**internally connected** (must be left floating).
5	CLK	**Clock:** clock output.
6	V_{SS}	**Ground:** circuit earth potential.
7	DIV(M)	**Divider:** input to the main programmable divider (8,5 MHz max.), usually from prescaler.
8	V_{DD2}	**Power Supply 2:** supply voltage for TTL-compatible stages (+ 5 V ± 10%).
9	FB	**Feedback:** feedback output to control the modulus of the external prescaler.
10	OL	**Out-of-lock:** out-of-lock indication flag output. This output is HIGH when phase comparator 2 is in operation (when the system is out-of-lock).
11	RESET	**Power-on-Reset:** Following power up an initial pulse is applied to this input pin to set the internal counters.

Pin functions (continued)

pin no.	mnemonic	description
12	XTAL	**Crystal:** output to external crystal to form the oscillator circuit in combination with the OSC input. Alternatively this pin may be used as a buffer output.
13	OSC	**Oscillator:** input to reference oscillator which together with the XTAL output and an external crystal is used to generate the reference frequency. Alternatively to OSC input may be used as a buffer amplifier for an external reference oscillator.
14	V_{DD1}	**Power Supply 1:** digital supply voltage (7 to 10 V).
15-18	DB3-DB0	**Data Bus:** Data Bus inputs (TTL compatible).
19-21	AB0-AB2	**Address Bus:** TTL compatible bidirectional address bus. Provides address output to an external memory or input from microcontroller. The outputs are 3-state with internal pull-downs.
22	PE2	**Program Enable 2:** } TTL compatible inputs to initiate the programming cycle or strobe the internal data latches.
23	PE1	**Program Enable 1:**
24	MOD	**Modulator:** high impedance linear phase modulator input, which applies a voltage controlled delay to the programmable divider output to the phase comparator.
25	$\overline{\text{MEMEN}}$	**Memory Enable:** mode control and memory enable bidirectional pin. If pin 25 is LOW at general reset the TDD1742T is set to the micro-controller mode; if pin 25 is HIGH at general reset the TDD1742T is set to the memory mode and the ROM/PROM is enabled.
26	BRB	**Bias Resistor B:** current mirror which acts as gain control for the phase modulator.
27	BRC	**Bias Resistor C:** current mirror pin which provides analogue biassing.
28	BRA	**Bias Resistor A:** current mirror pin which acts as gain control for phase comparator 1.

FUNCTIONAL DESCRIPTION

Reference oscillator chain

The reference oscillator chain comprises a crystal oscillator and dividers to give the required frequency to drive the phase comparators.
The oscillator stage is a single inverter connected between pin 12 (XTAL) and pin 13 (OSC). Satisfactory operation is achieved with crystals up to 9 MHz. Alternatively, the OSC input may be used as a buffer amplifier for an external reference oscillator.
The reference divider chain comprises a fixed divide by 4-stage followed by three cascaded programmable dividers of ratios ÷ 12/13/14/15, ÷ 5/6/7/9 and ÷ 1/2/4/8. The output of the last stage is applied as one input (R) to the two phase comparators. Thus a number of division ratios between 240 and 4320 are possible which provides all the required VHF and UHF channel spacings with reference crystals in a 1 to 9 MHz range.

Main programmable divider

The main programmable divider is a rate feedback binary divider. As shown in figure 1 it comprises a fixed 7-bit binary divider (÷ 128) and two rate selectors (n_1 and n_0). One rate selector controls a 7-bit fully programmable dual modulus divider (÷ $n_2/n_2 + 1$) and the other controls the external dual modulus prescaler (÷ A/A + 1).

The overall division rate (N) is given by:

$$N = (128\, n_2 + n_1)\, A + n_0$$

Where:

$$0 \leq n_0 \leq 127$$
$$0 \leq n_1 \leq 127$$
$$1 \leq n_2 \leq 127.$$

The output from the programmable divider is fed to the phase comparators via the phase modulator and the multiplexer. The phase modulator is bypassed if not selected.

Phase comparison

The TDD1742T contains 2 phase comparators which act in close co-operation. Phase comparator 1 is the main comparator. It is designed to have a high-gain analogue output, 4500 volts/cycle at 10 kHz (typ.). This enables a low noise performance to be achieved. However, the output of phase comparator 1 will saturate at high or low levels for very small phase excursions.
Phase comparator 2 is an auxiliary comparator with a wide range, which enables faster lock times to be achieved than otherwise would be possible. This digital phase comparator has a linear $\pm\, 2\,\pi$ radians phase range, which corresponds to a gain of $\frac{V_{DD}}{2}$ volts/cycle.

To avoid degrading the noise performance of the system by the relatively low gain of phase comparator 2, once a small phase error has been achieved an internal switch disconnects phase comparator 2, leaving only phase comparator 1 connected. Thus the low noise properties of phase comparator 1 are obtained once phase-lock has been achieved.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 1 (see Fig. 3)

Phase comparator 1 is comprised of a linear ramp generator and a sample and hold circuit.

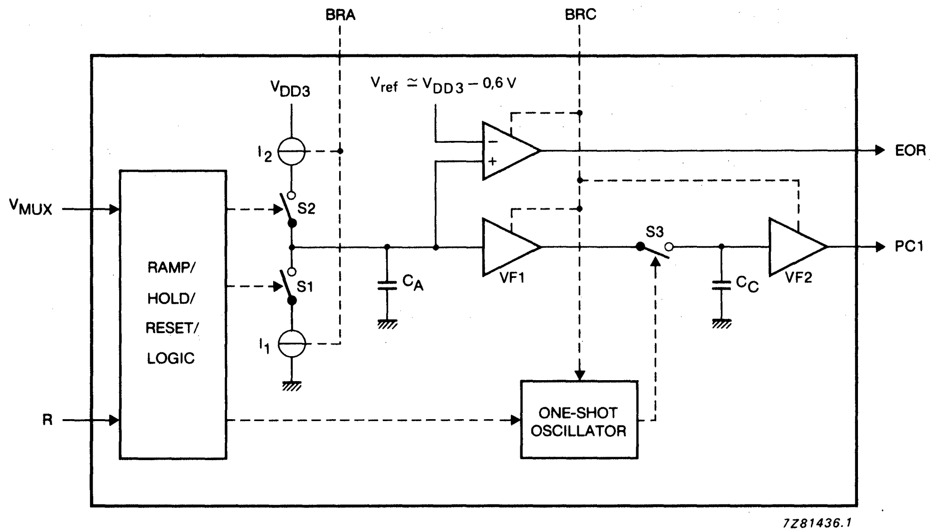


Fig. 3 Simplified block diagram of phase comparator 1.

A negative-going transition at the V_{MUX} input causes the hold capacitor C_A to be discharged via switch S1 and constant current source I_1.
A positive-going transition at the V_{MUX} input causes the hold capacitor C_A to be charged via switch S2 and constant current source I_2, which produces a linear ramp.
A negative-going transition at the R input terminates the linear ramp.
Capacitor C_A holds the voltage that the ramp has attained, and is buffered by the voltage follower VF1. After the output of VF1 is stable (2 μs), the sample switch S3 is closed for approximately 1 μs by the one-shot oscillator. This enables the capacitor C_C to charge to the voltage level of VF1 and in turn buffered by voltage follower VF2 made available at output PC1.
The construction and small duty cycle of the sample switch S3 provides a low hold step, resulting in a minimum side-band level.
If the linear ramp terminates before a negative-going transition at the R input is present, an end of ramp (EOR) signal is produced, generating in turn an out-of-lock (OL) signal. OL enables phase comparator 2 via the out-of-lock detector.

These actions are illustrated in the waveforms of Fig. 4 and Fig. 5.

The gain of phase comparator 1 as measured at PC1 is given by:

$$\text{PC gain} \simeq \frac{446\ I_{BRA}}{F_R}$$

Where:

I_{BRA} is in μA
F_R is the phase comparator reference frequency in kHz

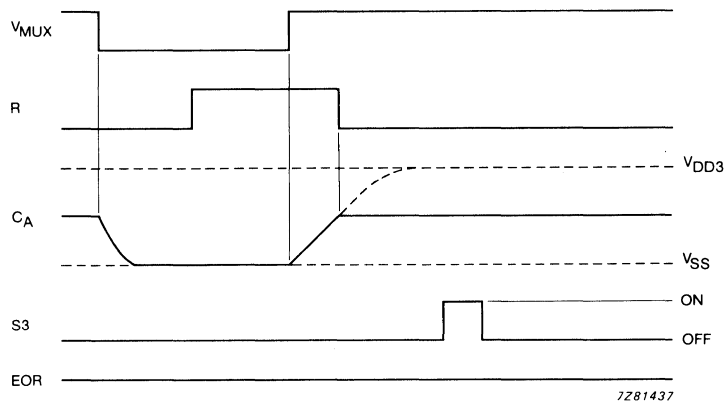


Fig. 4 Waveforms of phase comparator 1; in-lock condition.

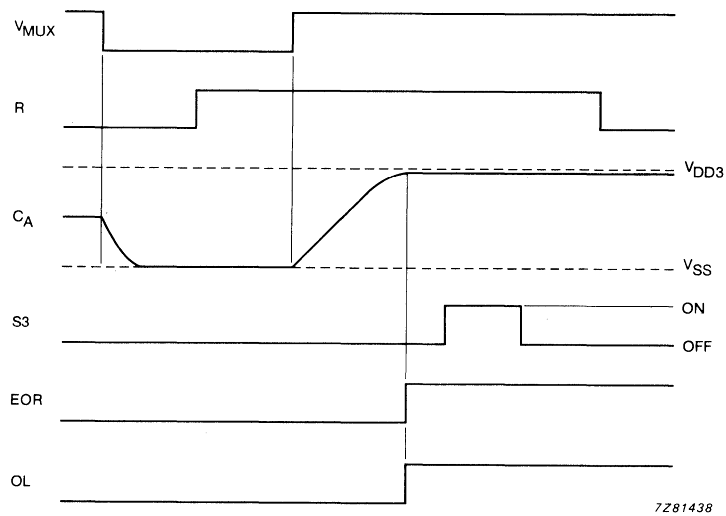


Fig. 5 Waveforms of phase comparator 1; out-of-lock condition.

When V_{MUX} leads R the output signal at pin 2 (PC1) is proportional to the phase difference (in-lock condition) or HIGH (out-of-lock condition).
When R leads V_{MUX} the output signal at pin 2 (PC1) remains LOW.

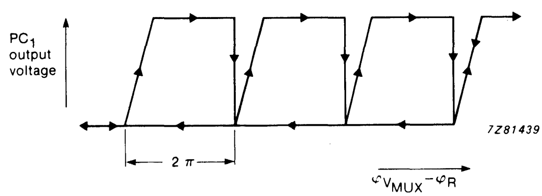


Fig. 6 Phase characteristic of output PC1.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 2 (see Fig. 7)

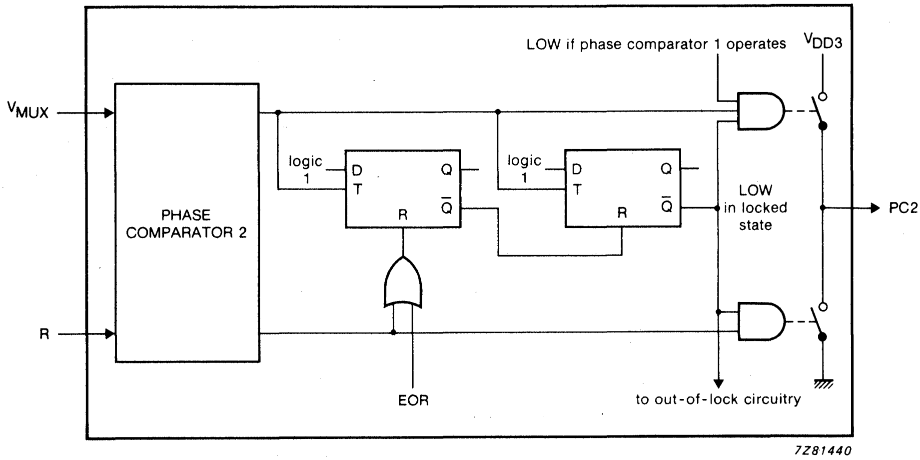


Fig. 7 Simplified block diagram of phase comparator 2.

The digital phase comparator (PC2) has three stable states:

- Reset
- V_{MUX} leads R
- R leads V_{MUX}

Table 1 Phase comparator 2: stable states and corresponding output levels

state	V_{MUX} leads R	R leads V_{MUX}
reset	0	0
V_{MUX} leads R	1	0
R leads V_{MUX}	0	1

Transition from one state to another takes place on command of either an active V_{MUX}-edge or an active R-edge as shown in Fig. 8.

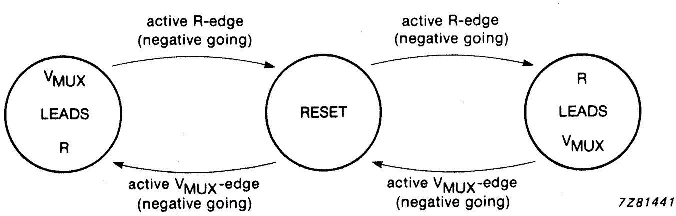


Fig. 8 Transition of state; phase comparator 2.

The output of phase comparator 2 produces positive or negative going pulses with variable width, dependent on the phase relationship of R and V_{MUX}.
The average output voltage is a linear function of the phase difference. Output at pin 3 (PC2) remains in the high impedance OFF-state in the region in which phase comparator 1 operates

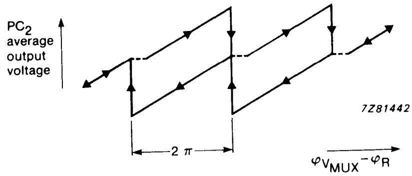


Fig. 9 Phase characteristic of output PC2.

To reach the reset state of phase comparator 2 it is necessary to apply:

- $2V_{MUX} + R$*
  or
- $2R + V_{MUX}$

Thus to achieve the R leads V_{MUX} state 2R must be applied; to achieve the V_{MUX1} leads R state $2V_{MUX}$ must be applied.

Out-of-lock function

There are several situations when the system goes from the locked to the out-of-lock state (OL output goes HIGH):

- V_{MUX} leads R, however out of the range of phase comparator 1
- R leads V_{MUX}
- R-pulse is missing
- V_{MUX}-pulse is missing

In the first three situations the locked state can be reset by applying two successive cycles within the range of phase comparator 1.
In the fourth situation the locked state can be reset by applying a V_{MUX} pulse followed by two successive cycles within the range of phase comparator 1.

Phase modulator (see Fig. 10)

The linear phase modulator applies a voltage controlled delay to the signal from the programmable divider to the phase comparator input. The gain of the phase modulator is adjustable via an external bias resistor (BRB) which is connected between pin 26 and ground.
The time delay introduced into the V path to the phase modulator is:

$$\frac{909}{I_{BRB}} \text{ ns/volt of input applied to pin 24 (MOD)}$$

When a positive-going transition appears at the V-input, the D type flip-flop produces a HIGH V′ level and causes capacitor C_B to produce a positive-going ramp via switch S1 and constant current source I_1 starting at the V_{SS} potential. When the ramp has reached a value equal to the modulation input voltage (at MOD), the comparator resets the D type flip-flop, which terminates the V pulse. C_B now discharges to V_{SS} via switch S1 and constant current source I_2 and the circuit returns to the start position. Because the trailing edge of the V′ pulse is the active edge for the phase comparators, a linear phase modulation is achieved. The associated waveforms are shown in Fig. 11. The phase modulator can be switched OFF, via the programming logic, to avoid superfluous dissipation. To achieve, this the M signal must be programmed to logic 0. The V pulse will then be connected via switch S2 to V_{MUX}.

* This means apply two successive active V_{MUX} edges followed by one active R edge.

FUNCTIONAL DESCRIPTION (continued)

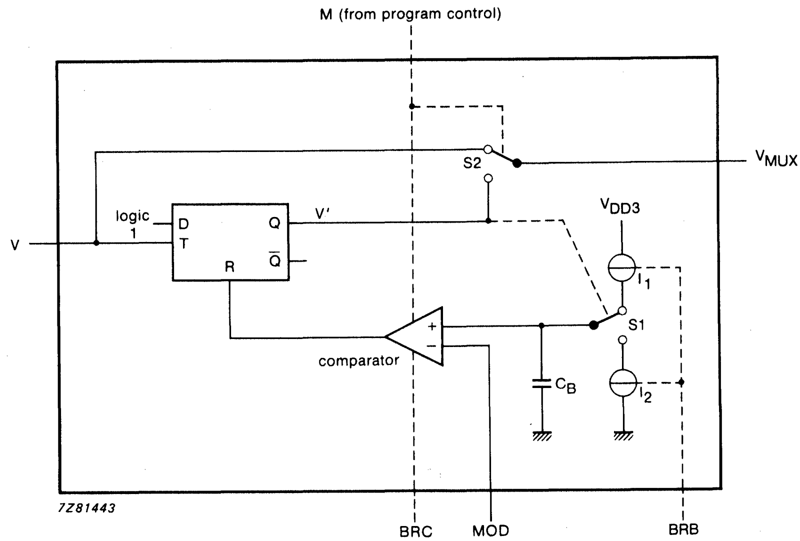


Fig. 10 Simplified block diagram of the phase modulator.

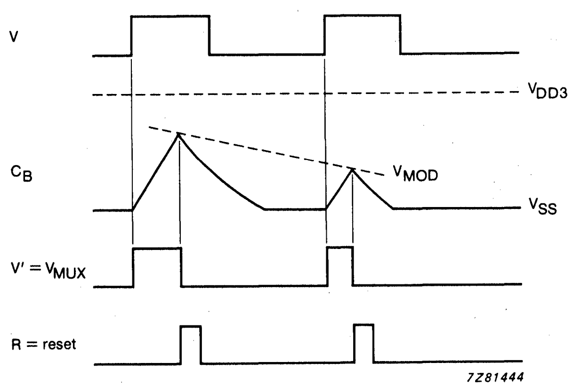


Fig. 11 Phase modulator waveforms; M = 1.

Program control

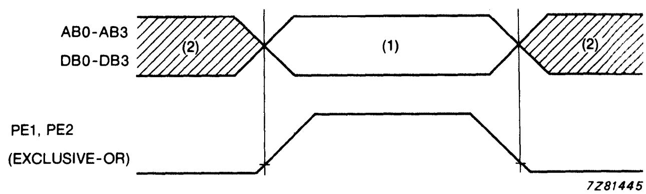
A multiplexed or bus structured sequence allows the TDD1742T to be interfaced to a microcontroller or a PROM.
The device is fully programmable in terms of:

- 6 bits to define the reference divider ratio
- 21 bits to define the main divider ratio
- 1 bit to switch the modulator
- 4 bits to determine the test status

Thus the TDD1742T is programmed with a total of 32 bits which are organized as eight 4-bit words. The address bus is 3 bits wide and the data bus is 4 bits wide. Both buses are TTL compatible.
The data words are described in detail in Tables 3 to 7.

Microcontroller mode

If pin 25 ($\overline{\text{MEMEN}}$) is LOW at general reset, the device is set to the micro-controller mode. In this mode a 7-bit word, comprised of 3 address bits (AB0 to AB2) and 4 data bits (DB0 to DB3), may be strobed into the TDD1742T when the program enable pins PE1 and PE2 are set to opposite state (EXCLUSIVE -OR condition; see Fig. 12 and Table 2). One frame of 8 words is necessary to completely program the TDD1742T. Incoming data is not clocked into the internal counter latches until after the receipt of data corresponding to address 111. Upon subsequent reprogramming it is not necessary to change all eight words but a reprogramming sequence must always finish with the data corresponding to address 111.



(1) Address and data valid.
(2) Address and data not valid.

Fig. 12 Waveforms for program enable function; microcontroller mode.

Table 2 Truth table for program enable function; microcontroller mode

PE1	PE2	load
0	0	NO
1	0	YES
0	1	YES
1	1	NO

Program control (continued)

Memory mode (PROM)

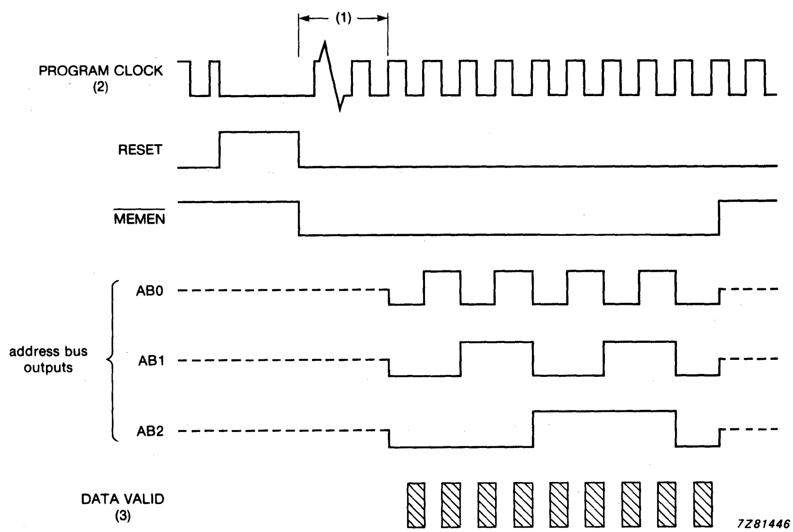
If pin 25 ($\overline{\text{MEMEN}}$) is HIGH at general reset, TDD1742T is set to the memory mode and a programming cycle is initiated. Subsequent reprogramming is performed by applying a pulse to program enable PE1 (pin 23) or PE2 (pin 22). If PE1 is LOW, programming will occur on the LOW-to-HIGH transition of PE2. If PE1 is HIGH, programming will occur on the HIGH-to-LOW transition of PE2. PE1 and PE2 are interchangeable. Reprogramming will also occur by applying a pulse to RESET (pin 11).

At the start of a programming sequence pin 25 goes LOW and may be used to apply power to the memory via an external driver. After a settling time the address bus outputs 000 followed by the remaining seven addresses. During the second half of each address period data, from the memory is latched into the TDD1742T so that the access time of the PROM is not critical.

Note

The program clock is derived from the reference divider chain and its frequency equals $f_{OSC}/4R_0$.

After the full 32 bits have been read the address returns to address 000 before going 3-state. This step transfers data from the internal data latches to the appropriate divider latches. Pin 25 now returns to a high impedance state and power is removed from the memory. Fig. 13 shows the timing for a reset initiated programming sequence; the timing is similar for program enable initiated sequence.



(1) Delay time for PROM settling.
(2) The program clock is derived from the reference divider chain.
(3) Data is valid during the shaded period.

Fig. 13 Timing diagram for TDD1742T PROM control.

Data memory maps

Table 3 Bit programming of the eight 4-bit words

address			data			
AB2	AB1	AB0	DB3	DB2	DB1	DB0
0	0	0	see Table 4			
0	0	1	$n_0 3$	$n_0 2$	$n_0 1$	$n_0 0$
0	1	0	$R_0 0$	$n_0 6$	$n_0 5$	$n_0 4$
0	1	1	$n_1 3$	$n_1 2$	$n_1 1$	$n_1 0$
1	0	0	$R_0 1$	$n_1 6$	$n_1 5$	$n_1 4$
1	0	1	$n_2 3$	$n_2 2$	$n_2 1$	$n_2 0$
1	1	0	M	$n_2 6$	$n_2 5$	$n_2 4$
1	1	1	$R_2 1$	$R_2 0$	$R_1 1$	$R_1 0$

In Table 3

n_0, n_1 and n_2 comprises the main programmable divider.

$n_0 0$ is the LSB of n_0, $n_0 6$ the MSB and so forth.

If M is 1 the modular is ON.

Table 4 Memory map for address 000

DB3	DB2	DB1	DB0	program clock to output CLK	mode
0	0	X	X	yes	idle
0	1	0	0	no	idle
all other combinations				not defined	not defined

Where

X = don't care.

For optimum performance (minimum crosstalk) 0100 should be programmed into address 000.

Memory maps (continued)

Table 5 Reference divider control; part 1

$R_0$1	$R_0$0	division ratio
0	0	12
0	1	13
1	0	14
1	1	15

In Table 5:

$R_0$0 and $R_0$1 control the ÷ 12/13/14/15 portion of the reference divider.

Table 6 Reference divider control; part 2

$R_1$1	$R_1$0	division ratio
0	0	9
0	1	5
1	0	6
1	1	7

In Table 6:

$R_1$0 and $R_1$1 control the ÷ 5/6/7/9 portion of the reference divider.

Table 7 Reference divider control; part 3

$R_2$1	$R_2$0	division ratio
0	0	1
0	1	2
1	0	4
1	1	8

In Table 7:

$R_2$0 and $R_2$1 control the ÷ 1/2/4/8 portion of the reference divider.

Current biassing

Current biassing is provided by 3 external bias resistors A, B and C.

Bias Resistor A: is connected between pin 28 (BRA) and ground. The value of the resistor must be such that I_{BRA} = 20 μA, which acts as gain control for analogue phase comparator 1.
Bias Resistor B: is connected between pin 26 (BRB) and ground. The value of the resistor must be such that I_{BRB} = 3 to 25 μA, which acts as gain control for the phase modulator.
Bias Resistor C: is connected between pin 27 (BRC) and ground. The value of the resistor must be such that I_{BRC} = 5 to 30 μA, which provides biassing for the remainder of the analogue circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges			
pin 14	V_{DD1}		−0,5 to + 15 V
pin 8	V_{DD2}		−0,5 to + 15 V
pin 1	V_{DD3}		−0,5 to + 15 V
Voltage on any input	V_I		−0,5 to V_{DD1} + 0,5 V
Relative supply voltage	V_{DD2}-V_{DD1}	max.	0,5 V
Relative supply voltage	V_{DD3}-V_{DD1}	max.	0,5 V
D.C. current into any input or output	± I	max.	10 mA
Power dissipation per package for T_{amb} = 0 to + 85 °C	P_{tot}	max.	400 mW
Power dissipation per output for T_{amb} = 0 to + 85 °C	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to 150 °C
Operating ambient temperature range	T_{amb}		−40 to 85 °C

D.C. CHARACTERISTICS

$V_{DD1} = V_{DD3} = 7{,}4$ V; $V_{DD2} = 5$ V; $V_{SS} = 0$ V; $T_{amb} = 25$ °C unless otherwise specified; for definitions see note 1.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage					
pin 14	V_{DD1}	7	–	10	V
pin 8	V_{DD2}	4,5	–	5	V
pin 1	V_{DD3}	7	–	10	V
Supply current					
pin 14 (phase modulator OFF)	I_{DD1}	–	–	1,5	mA
pin 8	I_{DD2}	–	–	100	µA
pin 1 (phase modulator OFF)	I_{DD3}	–	–	1,5	mA
Input leakage current (notes 2 and 3)					
logic inputs, MOD	$\pm I_{LI}$	–	–	300	nA
Output leakage current (notes 2 and 3) at ½ V_{DD}					
PC2 high impedance OFF state	$\pm I_{LO}$	–	–	50	nA
$\overline{\text{MEMEN}}$ high impedance state	$\pm I_{LO}$	–	–	1,6	µA
I/O current					
AB0 to AB2 high impedance state	$I_{I/O}$	5	–	30	µA
Logic input voltage LOW					
CMOS inputs; CMOS I/Os	V_{IL}	–	–	$0{,}3V_{DD1}$	V
TTL inputs; TTL I/Os	V_{IL}	–	–	0,8	V
Logic input voltage HIGH					
CMOS inputs; CMOS I/Os	V_{IH}	$0{,}7V_{DD1}$	–	–	V
TTL inputs; TTL I/Os	V_{IH}	2	–	–	V
Logic output voltage LOW (note 2)					
at $\lvert I_O \rvert < 1$ µA	V_{OL}	–	–	50	mV
Logic output voltage HIGH (note 2)					
at $\lvert I_O \rvert < 1$ µA	V_{OH}	V_{DD1}-50	–	–	mV

parameter	symbol	min.	typ.	max.	unit
Logic output voltage LOW (note 2)					
$\overline{\text{MEMEN}}$ at I_{OL} = 4 mA	V_{OL}	–	–	1	V
PC2 at I_{OL} = 1,5 mA	V_{OL}	–	–	0,5	V
CLK; OL at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
XTAL at I_{OL} = 3 mA	V_{OL}	–	–	0,5	V
FB at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
AB0; AB1; AB2 at I_{OL} = 0,2 mA	V_{OL}	–	–	0,4	V
Logic output voltage HIGH (notes 2 and 3)					
PC2 at $-I_{OH}$ = 1,5 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
CLK; OL at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
XTAL at $-I_{OH}$ = 3 mA	V_{OH}	$V_{DD1}-1$	–	–	V
FB at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD2}-1$	–	–	V
AB0; AB1 at I_{OH} = 0,2 mA	V_{OH}	2,4	–	–	V
AB2 at I_{OH} = 0,8 mA	V_{OH}	2,4	–	–	V
Output PC1					
sink current (notes 2, 3 and Fig. 15)	I_O	1	–	–	mA
source current (notes 2, 3 and Fig. 16)	$-I_O$	1	–	–	mA
Internal resistance of phase comparator 1 (notes 2 and 3) locked state |output swing| < 200 mV specified output range: 0,5 V_{DD} −0,5 V to 0,5 V_{DD} + 0,5 V	R_i	–	2,0	–	Ω

A.C. CHARACTERISTICS

A dynamic specification is given for the circuit, built-up with external components as shown in Fig. 14, under the following conditions; for definitions see note 1; V_{DD} = 7,4 ± 0,4 V; T_{amb} = 25 °C; input transition times ⩽ 40 ns; $C_A = C_B = C_C$ = 10 nF; R_A chosen so that I_{RA} = 20 μA ± 1 μA; R_B chosen so that I_{RB} = 3 to 25 μA; R_C chosen so that I_{RC} = 5 to 30 μA; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Main programmable divider (DIV(M); pin 7) input frequency all divider ratios (square wave input)	$f_{DIV(M)}$	8,5	–	–	MHz
Reference divider input frequency all divider ratios (square wave input)	$f_{DIV(R)}$	9	–	–	MHz
Oscillator frequency (OSC; pin 13)	f_{OSC}	9	12	–	MHz
Input capacitance					
DIV(M); OSC	C_I	–	–	3	pF
DB0 to DB3; PE1; PE2; AB0 to AB2	C_I	–	–	5	pF
Propagation delay (see Fig. 17)					
Feedback output to external prescaler DIV (M) → FB at C_L = 10 pF					
HIGH to LOW*	t_{PHL}	–	35	70	ns
LOW to HIGH*	t_{PLH}	–	35	70	ns
Average power supply current (notes 3 and 4) in-lock state	I_{DD1}	–	2	–	mA
	I_{DD2}	–	0,15	–	mA
	I_{DD3}	–	0,45	–	mA

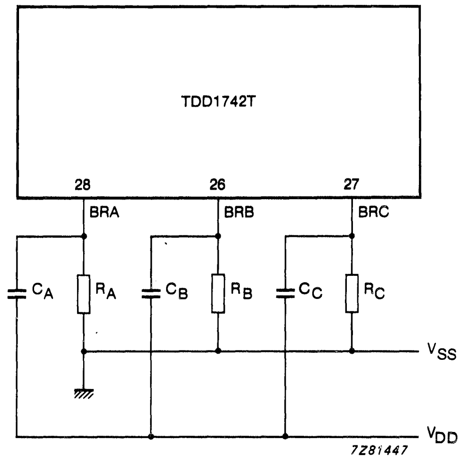


Fig. 14 Test circuit for measuring a.c. characteristics.

Notes to the characteristics

1. Definitions:
   R_A = external biassing resistor between pins BRA and V_{SS}.
   R_B = external biassing resistor between pins BRB and V_{SS}.
   R_C = external biassing resistor between pins BRC and V_{SS}.
   C_A = decoupling capacitor between pins BRA and V_{DD}.
   C_B = decoupling capacitor between pins BRB and V_{DD}.
   C_C = decoupling capacitor between pins BRC and V_{DD}.
   CMOS logic inputs: RESET, OSC.
   CMOS logic outputs: PC2, CLK, OL, XTAL.
   CMOS logic I/O: $\overline{\text{MEMEN}}$.
   TTL logic inputs: DB0 to DB3, PE2, PE1.
   TTL logic output: FB.
   TTL logic I/O: AB0 to AB2.
   Analogue inputs: DIV(M), MOD.
   Analogue output: PC1.
   Analogue biassing pins: BRA, BRB, BRC.
2. All logic inputs at V_{SS} or V_{DD}.
3. R_A connected; its value chosen such that I_{BRA} = 20 μA.
   R_B connected; its value chosen such that I_{BRB} = 20 μA.
   R_C connected; its value chosen such that I_{BRC} = 20 μA.
4. Average power supply current measured at:
   f_{OSC} = 5 MHz, external clock, divider ratio 420;
   $f_{DIV(M)}$ = 2 MHz, divider ratio 168.

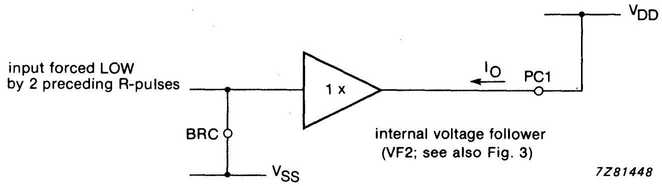


Fig. 15 Equivalent circuit for output PC1 sink current.

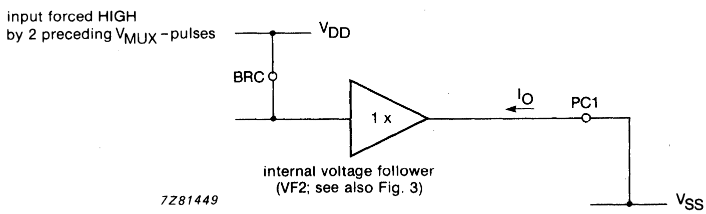


Fig. 16 Equivalent circuit for output PC1 source current.

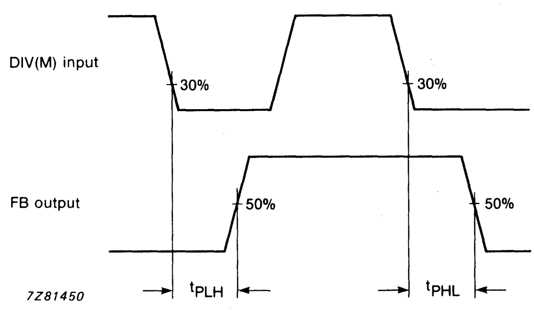


Fig. 17 Waveforms showing propagation delay; DIV (M) → FB.

APPLICATION INFORMATION

Fig. 18 shows a typical application circuit using the TDD1742T in the memory mode with the following design parameters:

Frequency range	150 to 155 MHz
VCO sensitivity	1 MHz/V
Reference frequency	12,5 kHz
Prescaler	÷ 80/81
Reference crystal frequency	5,25 MHz
Reference divider chain	÷ 15; ÷ 7; ÷ 1
Total division ratio	12000 to 12400
Loop bandwidth	300 Hz

APPLICATION INFORMATION (continued)

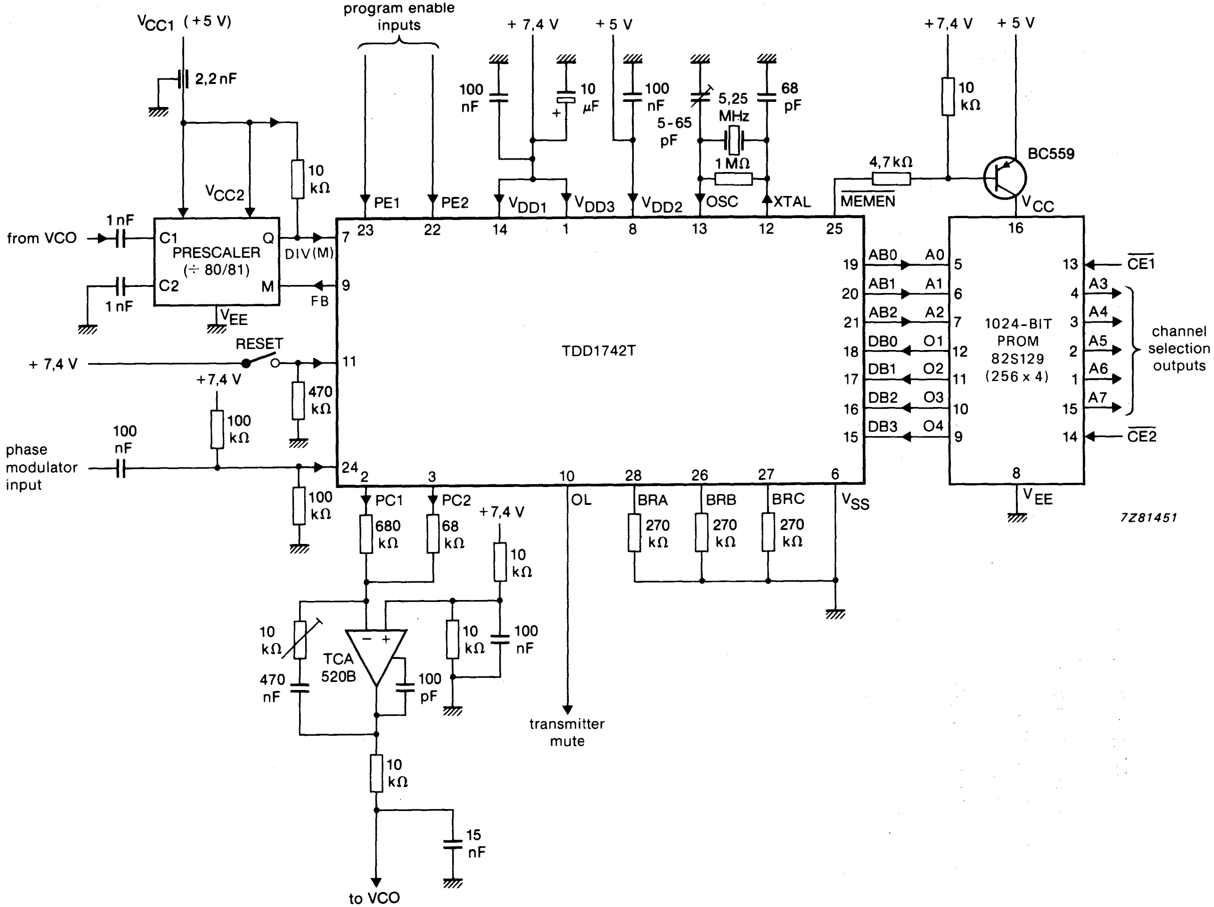


Fig. 18 Typical application circuit using the TDD1742T in memory mode.

Radio tuning PLL frequency synthesizer

TSA6057/T

GENERAL DESCRIPTION

The TSA6057/6057T is a bipolar single chip frequency synthesizer manufactured in SUBILO-N technology (components laterally separated by oxide). It performs all the tuning functions of a PLL radio tuning system. The IC is designed for application in all types of radio receivers.

Features

- On-chip AM and FM prescalers with high input sensitivity
- On-chip high performance one input (two output) tuning voltage amplifier for the AM and FM loop filters
- On-chip 2-level current amplifier (charge pump) to adjust the loop gain
- Only one reference oscillator (4 MHz) for both AM and FM
- High speed tuning due to a powerful digital memory phase detector
- 40 kHz output reference frequency for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100)
- Oscillator frequency ranges of: 512 kHz to 30 MHz and 30 MHz to 150 MHz
- Three selectable reference frequencies of 1 kHz, 10 kHz or 25 kHz for both tuning ranges
- Serial 2-wire I^2C-bus interface to a microcomputer and one programmable address input
- Software controlled bandswitch output

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 3		$V_{CC1} = V_{3\text{-}4}$	4.5	5.0	5.5	V
pin 16		$V_{CC2} = V_{16\text{-}4}$	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_3	12	20	28	mA
pin 16		I_{16}	0.7	1.0	1.3	mA
Max. input frequency on AM_I		f_{iAM}	30	–	–	MHz
Min. input frequency on AM_I		f_{iAM}	–	–	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	–	–	MHz
Min. input frequency on FM_I		f_{iFM}	–	–	30	MHz
Input voltage on AM_I (RMS value)	$V_{iFM} = 0$ V	$V_{iAM(rms)}$	30	–	500	mV
Input voltage on FM_I (RMS value)	$V_{iAM} = 0$ V	$V_{iFM(rms)}$	20	–	300	mV
Total power dissipation		P_{tot}	–	0.14	–	W
Operating ambient temperature range		T_{amb}	–30	–	+ 85	^oC

PACKAGE OUTLINES

TSA6057: 16-lead DIL; plastic (SOT38).
TSA6057T: 16-lead minipack; plastic (SO16L; SOT162A).

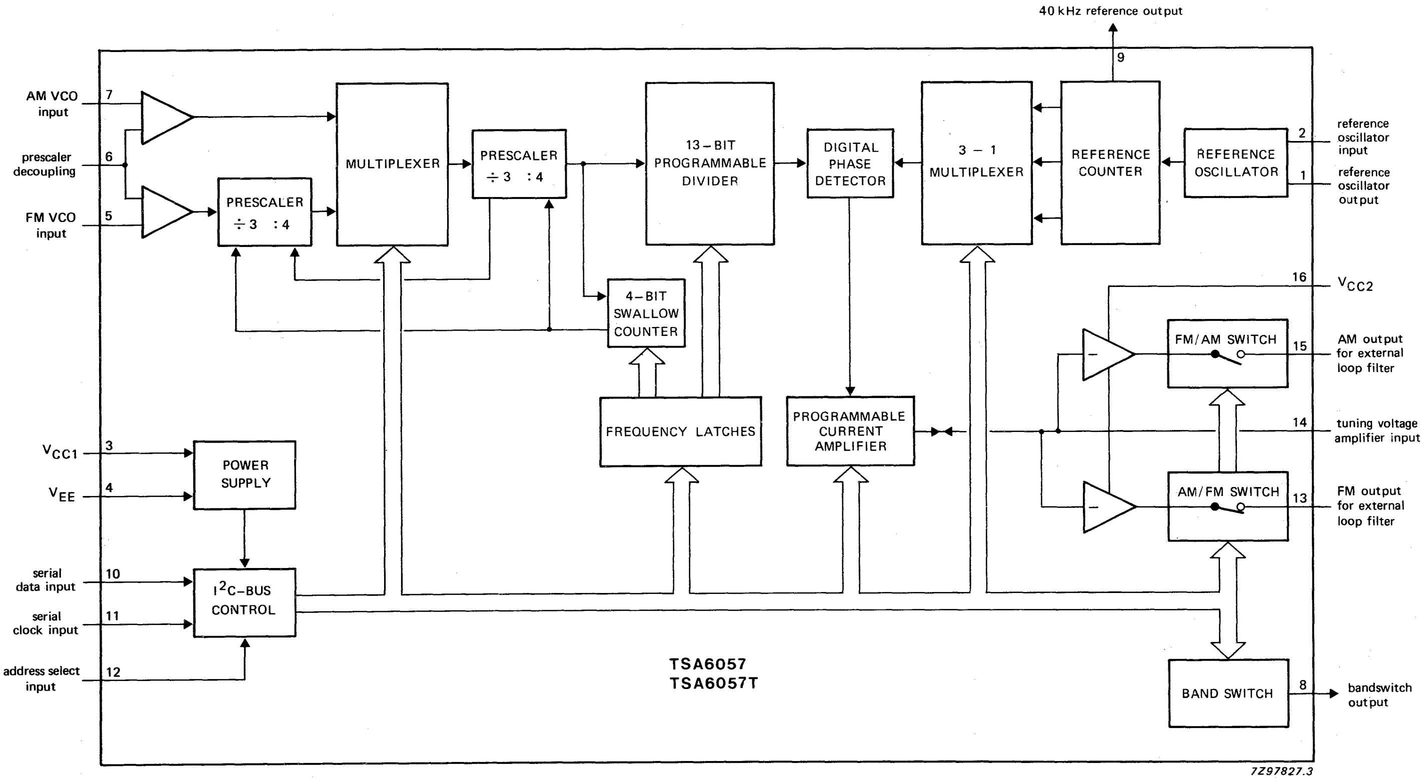


Fig.1 Block diagram.

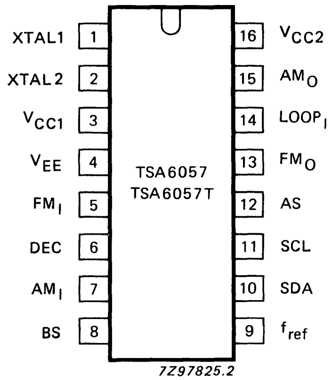


Fig.2 Pinning diagram.

PINNING

1	XTAL1	reference oscillator output
2	XTAL2	reference oscillator input
3	V_{CC1}	positive supply voltage
4	V_{EE}	ground
5	FM_I	FM VCO input
6	DEC	prescaler decoupling
7	AM_I	AM VCO input
8	BS	bandswitch output
9	f_{ref}	40 kHz reference output
10	SDA	serial data input (I²C-bus)
11	SCL	serial clock input (I²C-bus)
12	AS	address select input (I²C-bus)
13	FM_O	FM output for external loop filter
14	$LOOP_I$	tuning voltage amplifier input
15	AM_O	AM output for external loop filter
16	V_{CC2}	positive supply voltage

FUNCTIONAL DESCRIPTION

The TSA6057/6057T contains the following parts and facilities:

- Separate input amplifiers for the AM and FM VCO-signals.
- A prescaler with the divisors 3:4 on AM and 15:16 on FM, a multiplexer to select AM or FM and a 4-bit programmable swallow counter.
- A 13-bit programmable counter.
- A digital memory phase detector.
- A reference frequency channel comprised of a 4 MHz crystal oscillator followed by a reference counter. The reference frequency can be 1 kHz, 10 kHz or 25 kHz and is applied to the digital memory phase detector. The reference counter also outputs a 40 kHz reference frequency to pin 9 for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100).
- A programmable current amplifier (charge pump) which consists of a 5 μA and a 450 μA current source. This allows adjustment of loop gain, thus providing high current-high speed tuning and low current-stable tuning.
- A one input – two output tuning voltage amplifier. One output is connected to the external AM loop filter and the other output to the external FM loop filter. Under software control, the AM output is switched to a high impedance state by the FM/AM switch in the FM position and the FM output is switched to a high impedance state by the AM/FM switch in the AM position. The outputs can deliver a tuning voltage of up to 10.5 V.
- An I^2C-bus interface with data latches and control logic. The I^2C-bus is intended for communication between microcontrollers and different ICs or modules. Detailed information on the I^2C-bus specification is available on request.
- A software-controlled bandswitch output.

FUNCTIONAL DESCRIPTION (continued)

Controls

The TSA6057/6057T is controlled via the 2-wire I^2C-bus. For programming there is one module address, a logic 0 R/W bit, a subaddress byte and four data bytes. The subaddress determines which one of the four data bytes is transmitted first. The module address contains a programmable address bit (D1) which with address select input AS (pin 12) makes it possible to operate two TSA6057s in one system.

The auto increment facility of the I^2C-bus allows programming of the TSA6057/6057T within one transmission (address + subaddress + 4 data bytes).

- The TSA6057/6057T can also be partially programmed. Transmission must then be ended by a stop condition.

The bit organization of the 4 data bytes is shown in Fig.3 and are described in sections (a) to (f).

(a) The bits S0 to S16 (DB0: D7-D1; DB1: D7-D0; DB2: D1-D0) together with bit FM/AM (DB2: D5) are used to set the divisor of the input frequency at inputs AM_I (pin 7) or FM_I (pin 5). If the system is in lock the following is valid:

FM/$\overline{AM}$	input frequency (f_i)	input
0	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S13 \times 2^{13} + S14 \times 2^{14}) \times f_{ref}$	AM_I
1	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S15 \times 2^{15} + S16 \times 2^{16}) \times f_{ref}$	FM_I

Where

The minimum dividing ratio for AM mode is 2^6 = 64
The minimum dividing ratio for FM mode is 2^8 = 256

(b) The bit CP is used to control the charge pump current (DB0: D0).

CP	current
0	low
1	high

(c) The bits REF1 and REF2 are used to set the reference frequency applied to the phase detector (DB2: D7-D6).

REF1	REF2	frequency (kHz)
0	0	1
0	1	10
1	0	25
1	1	none

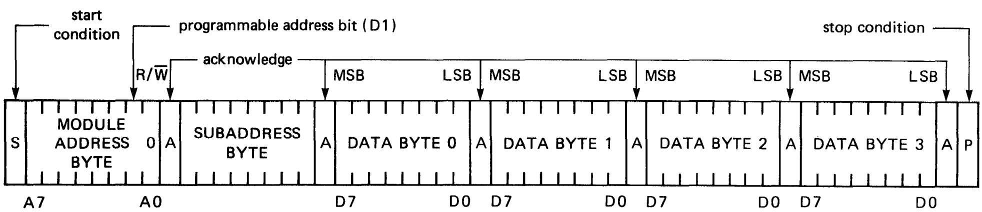
(d) The bit $\overline{FM}$/AM OPAMP controls the switch AM/FM; FM/AM in the tuning voltage amplifier output circuitry (DB2: D4).

$\overline{FM}$/AM OPAMP	switch FM/AM	switch AM/FM
1	closed	open
0	open	closed

(e) The bit BS controls the open collector bandswitch output (DB2: D2).

BS	bandswitch output
1	sink current
0	floating

(f) The data byte DB3 must be set to 0 . . . . . .0. It is also used for test purposes.



	MSB (A7/D7)							LSB (A0/D0)
MODULE ADDRESS	1	1	0	0	0	1	0/1	0
SUBADDRESS	0	0	0	0	0	0	0/1	0/1
DATA BYTE 0 (DB0)	S6	S5	S4	S3	S2	S1	S0	CP
DATA BYTE 1 (DB1)	S14	S13	S12	S11	S10	S9	S8	S7
DATA BYTE 2 (DB2)	REF1	REF2	FM/$\overline{AM}$	F$\overline{M}$/AM OPAMP	NOT USED	BS	S16	S15
DATA BYTE 3 (DB3)	T1	T2	T3	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED

Examples using auto-increment facility

S	ADDRESS	A	SUBADDRESS 02	A	DB2	A	DB3	A	P				
S	ADDRESS	A	SUBADDRESS 00	A	DB0	A	DB1	A	P				
S	ADDRESS	A	SUBADDRESS 03	A	DB3	A	DB0	A	DB1	A	DB2	A	P

7Z97826.2

Fig.3 Bit organization.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	$V_{CC1} = V_{3\text{-}4}$	−0.3	5.5	V
Supply voltage (pin 16)	$V_{CC2} = V_{16\text{-}4}$	V_{CC1}	12.5	V
Total power dissipation	P_{tot}	−	0.85	W
Operating ambient temperature	T_{amb}	−30	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{CC1} = 5 V; V_{CC2} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_{CC1}	4.5	5.0	5.5	V
Supply voltage (pin 16)		V_{CC2}	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_{CC1}	12	20	28	mA
pin 16		I_{CC2}	0.7	1.0	1.3	mA
I^2C-bus inputs (SDA; SCL)						
Input voltage HIGH		V_{IH}	3.0	−	5.0	V
Input voltage LOW		V_{IL}	−0.3	−	1.5	V
Input current HIGH		I_{IH}	−	−	10	µA
Input current LOW		I_{IL}	−	−	10	µA
SDA output	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	−	−	0.4	V
AS input						
Input voltage HIGH		V_{IH}	3.0	−	5.0	V
Input voltage LOW		V_{IL}	−0.3	−	1.0	V
Input current HIGH		I_{IH}	−	−	10	µA
Input current LOW		I_{IL}	−	−	10	µA
RF input (AM; FM)						
Max. input frequency on AM_I		f_{iAM}	30	−	−	MHz
Min. input frequency on AM_I		f_{iAM}	−	−	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	−	−	MHz
Min. input frequency on FM_I		f_{iFM}	−	−	30	MHz
Input voltage on AM_I (RMS value)	V_{iFM} = 0 V measured in Fig.4	$V_{iAM(rms)}$	30	−	500	mV
Input impedance AM_I						
resistance		R_{AM}	−	5.9	−	kΩ
capacitance		C_{AM}	−	2	−	pF

parameter	conditions	symbol	min.	typ.	max.	unit
RF input (continued)						
Input voltage on FM_I (RMS value)	V_{iAM} = 0 V measured in Fig.4	$V_{iFM(rms)}$	20	–	300	mV
Input impedance FM_I						
resistance		R_{FM}	–	3.6	–	kΩ
capacitance		C_{FM}	–	2	–	pF
Oscillator (XTAL1; XTAL2)						
Crystal resonance resistance (4 MHz)	see Fig.5	R_{XTAL}	–	–	150	Ω
Programmable charge pump						
Output current to loop filter						
bit CP = logic 0		I_{chp}	3	5	7	μA
bit CP = logic 1		I_{chp}	400	500	600	μA
Ripple rejection	f_{ripple} = 100 Hz					
20 log $\Delta V_{CC1}/\Delta V_O$		RR	40	50	–	dB
20 log $\Delta V_{CC2}/\Delta V_O$		RR	40	50	–	dB
Bandswitch output (pin 8)						
Output voltage HIGH		V_{OH}	–	–	12	V
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0.8	V
Output leakage current	V_{OH} = 12 V	I_{LO}	–	–	10	μA
Reference frequency output (pin 9)						
Output frequency	4 MHz crystal	f_{ref}	–	40	–	kHz
Output voltage HIGH	I_{source} = 5 μA	V_{OH}	1.2	1.4	1.7	V
Output voltage LOW		V_{OL}	–	0.1	0.2	V
Tuning voltage amplifier outputs						
AM output (pin 15)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
FM output (pin 13)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
Impedance of switched off output		$Z_{O(off)}$	5	–	–	MΩ
Input bias current (absolute value)		I_{bias}	–	1	5	nA

SENSITIVITY MEASUREMENT

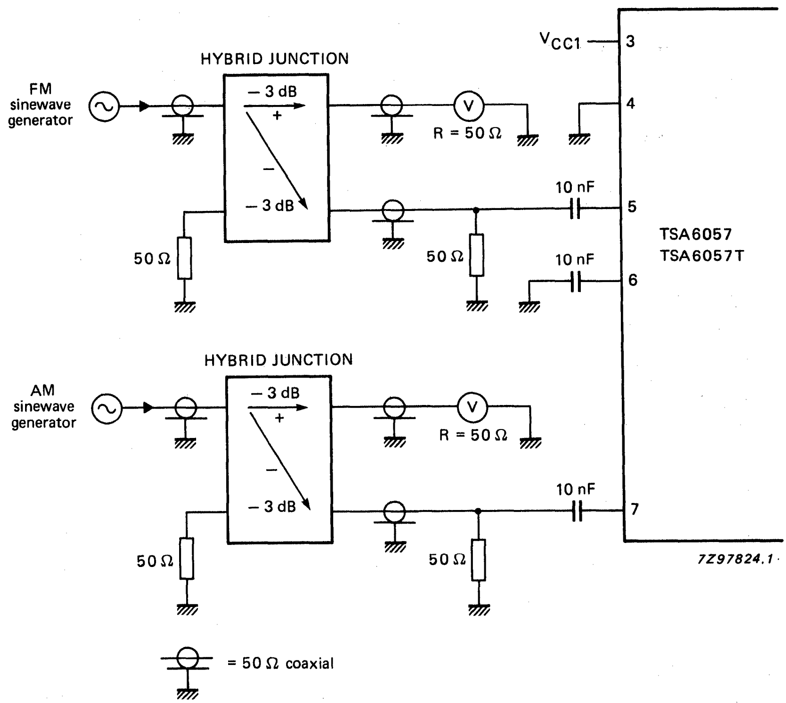


Fig.4 Prescaler input sensitivity.

APPLICATION INFORMATION

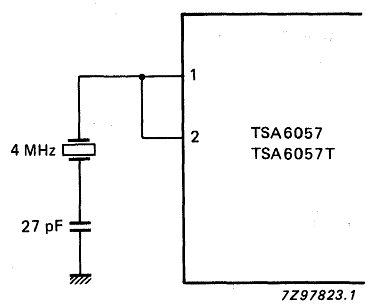


Fig.5 Crystal connection (4 MHz).

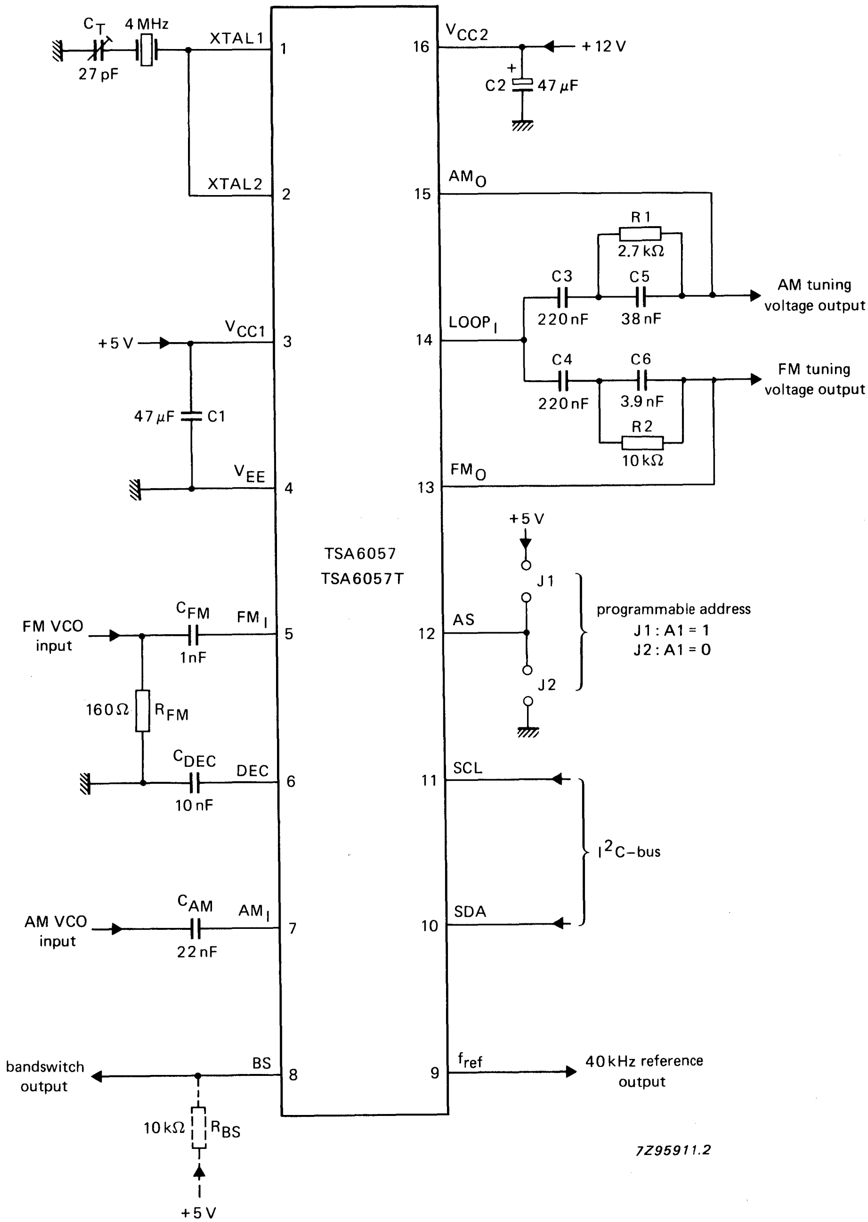


Fig.6 Application diagram

1.3GHz bi-directional I²C bus controlled synthesizer TSA5511

FEATURES

- Complete 1.3 GHz single chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner
- Analog-to-digital converter
- 8 bus controlled ports (5 for TSA5511T), 4 open collector outputs (bi-directional)
- Power-down flag

APPLICATIONS

- TV tuners
- VCR Tuners

DESCRIPTION

The TSA5511 is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the eight output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning those ports can be read out of the TSA5511 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage on Port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δf	frequency range	64	–	1300	MHz
V_I	input voltage level				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator	3.2	4	4.48	MHz
I_O	open–collector output current	10	–	–	mA
I_O	current–limited output current	–	1	–	mA
T_{amb}	operating ambient temperature range	–10	–	80	°C
T_{stg}	storage temperature range (IC)	–40	–	150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5511	18	DIL	plastic	SOT102
TSA5511T	16	SO	plastic	SOT109
TSA5511AT	20	SO	plastic	SOT163

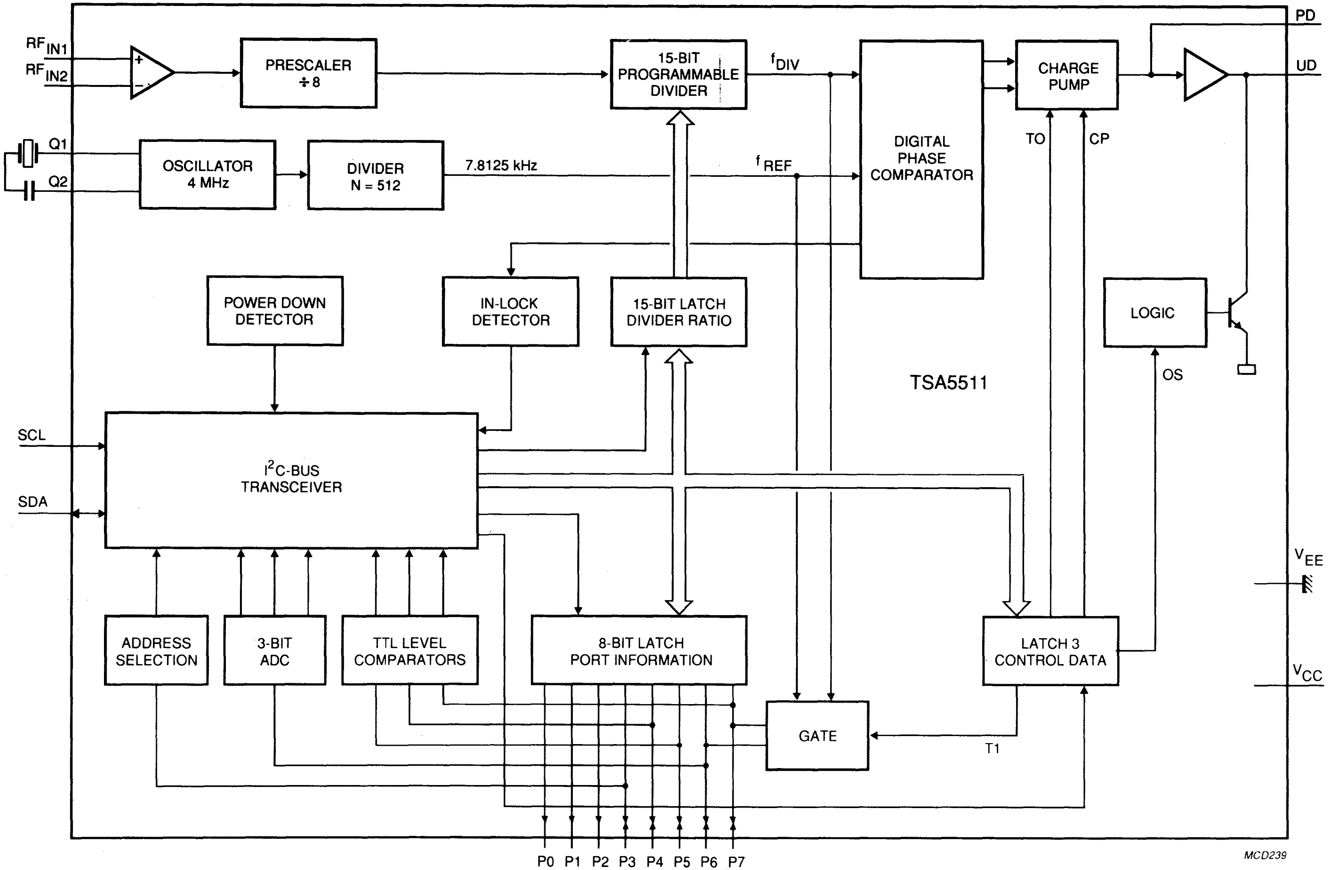


Fig.1 Block diagram.

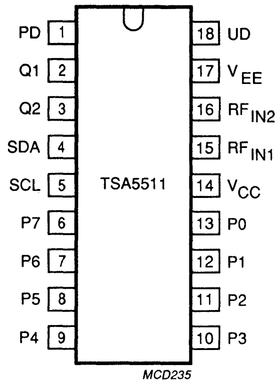


Fig.2 Pin configuration (SOT102).

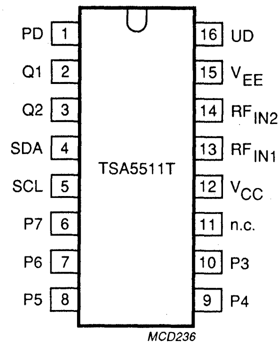


Fig.3 Pin configuration (SOT109).

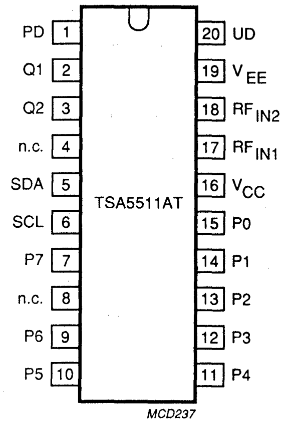


Fig.4 Pin configuration (SOT163).

PINNING

SYMBOL	PIN DIL 18	PIN SO16	PIN SO20	DESCRIPTION
PD	1	1	1	charge-pump output
Q1	2	2	2	crystal oscillator input 1
Q2	3	3	3	crystal oscillator input 2
n.c.			4	not connected
SDA	4	4	5	serial data input/output
SCL	5	5	6	serial clock input
P7	6	6	7	port output/input (general purpose)
n.c.			8	not connected
P6	7	7	9	port output/input for general purpose ADC
P5	8	8	10	port output/input (general purpose)
P4	9	9	11	port output/input (general purpose)
P3	10	10	12	port output/input for address selection
P2	11		13	port output
n.c.		11		not connected
P1	12		14	port output
P0	13		15	port output
V_{CC}	14	12	16	voltage supply
RF_{IN1}	15	13	17	UHF/VHF signal input 1
RF_{IN2}	16	14	18	UHF/VHF signal input 2 (decoupled)
V_{EE}	17	15	19	GND
UD	18	16	20	drive output

FUNCTIONAL DESCRIPTION

The TSA5511 is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/W̄ bit for selecting READ or WRITE mode.

WRITE mode : R/W̄ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5511. The bus transceiver has an auto-increment facility which permits the programming of the TSA5511 within one single transmission (address + 4 data bytes).

The TSA5511 can also be partially programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purpose. At power-on the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of UHF/VHF signal is first divided by 8 the step size is 62.5 kHz. A 3.2 MHz crystal can offer step sizes of 50 kHz.

Table 1 Write data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports control bits	P7	P6	P5	P4	P3	P2*	P1*	P0*	A	byte 5

note

* not valid for TSA5511T.

MA1, MA0 programmable address bits (see Table 4)

A acknowledge bit

$N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$

CP charge-pump current

CP = 0 50 µA

CP = 1 220 µA

P3 to P0 = 1 limited-current output is active

P7 to P4 = 1 open-collector output is active

P7 to P0 = 0 output are in high impedance state

T1 = 1 P6 = f_{ref}, P7 = f_{DIV}

T0 = 1 3-state charge-pump

OS = 1 operational amplifier output is switched off (varicap drive disable)

FUNCTIONAL DESCRIPTION (continued)

READ mode : R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5511 by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5511 generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.
A second data byte can be read out of the TSA5511 if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.
The TSA5511 will then release the data line to allow the processor to generate a STOP condition.
When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state.
The POR flag (power-on-reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5511 (end of a READ sequence).
Control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked. The bits I2, I1 and I0 represent the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 a HIGH level (TTL levels).
A built-in 5-level ADC is available on I/O port P6. This converter can be used to feed AFC information to the controller from the IF section of the television as illustrated in the typical application circuit in Fig. 5. The relationship between bits A2, A1 and A0 and the input voltage on port P6 is given in Table 3.

Table 2 Read data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–	byte 2

POR	power-on-reset flag. (POR = 1 on power-on)
FL	in-lock flag (FL = 1 when the loop is phase-locked)
I2, I1, I0	digital information for I/O ports P7, P5 and P4 respectively
A2, A1, A0	digital outputs of the 5-level ADC. Accuracy is 1/2 LSB (see Table 3)

MSB is transmitted first.

Address selection

The module address contains programmable address bits (MA1 and MA0) which together with the I/O port P3 offers the possibility of having several synthesizers (up to 3) in one system.
The relationship between MA1 and MA0 and the input voltage I/O port P3 is given in Table 4.

Table 3 A/D converter levels

Voltage applied on the port P6	A2	A1	A0
0.6 V_{CC} to 13.5 V	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V	0	0	0

Table 4 Address selection

MA1	MA0	Voltage applied on port P3
0	0	0 to 0.1 V_{CC}
0	1	always valid
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	6	V
V_1	charge-pump output voltage	–0.3	V_{CC}	V
V_2	crystal (Q1) input voltage	–0.3	V_{CC}	V
V_4	serial data input/output	–0.3	6	V
V_5	serial clock input	–0.3	6	V
V_{6-13}	P7 to P1 I/O voltage	–0.3	+16	V
V_{15}	prescaler input	–0.3	V_{CC}	V
V_{18}	drive output voltage	–0.3	V_{CC}	V
I_6	P7 to P0 output current (open collector)	–1	15	mA
I_4	SDA output current (open collector)	–1	5	mA
T_{stg}	storage temperature range (IC)	–40	+150	°C
T_j	maximum junction temperature		150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air (DIL18)	-	80	K/W
	from junction to ambient in free air (SO16)	-	110	K/W
	from junction to ambient in free air (SO20)	-	80	K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified
All pin numbers refer to DIL 18 version

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Functional range						
V_{CC}	supply voltage range		4.5	–	5.5	V
T_{amb}	operating ambient temperature range		–10	–	80	°C
f_{CLK}	clock input frequency		64	–	1300	MHz
N	divider		256	–	32767	
I_{CC}	supply current		25	35	50	mA
f_{XTAL}	crystal oscillator		3.2	4	4.48	MHz
Z_I	input impedance (pin 2)		–480	–400	–320	Ω
	input level	V_{CC} = 4.5 V to 5.5 V; T_{amb} = –10 to 80 °C; see typical sensitivity curve in Fig. 6				
	f = 80 to 150 MHz		12/–25	–	300/2.6	mV/dBm
	f = 150 to 1000 MHz		9/–28	–	300/2.6	mV/dBm
	f = 1000 to 1300 MHz		40/–15	–	300/2.6	mV/dBm
R_I	prescaler input resistance see SMITH chart in Fig. 7		–	50	–	Ω
C_I	input capacitance		–	2	–	pF
Output ports (current-limited) P0-P3						
I_{LO}	leakage current	V_{13} = 13.5 V	–	–	10	μA
I_{sink}	output sink current	V_{13} = 12 V	0.7	1.0	1.5	mA
Output ports (open collector) P4-P7 (see note 1)						
I_{LO}	leakage current	V_9 = 13.5 V	–	–	10	μA
V_{OL}	output voltage LOW	I_9 = 10 mA; note 2	–	–	0.7	V
Input P3						
I_{OH}	input current HIGH	V_{OH} = 13.5 V	–	–	10	μA
I_{OL}	input current LOW	V_{OL} = 0 V	–10	–	–	μA
Input ports P4-5, P7						
V_{IL}	input voltage LOW		–	–	0.8	V
V_{IH}	input voltage HIGH		2.7	–	–	V
I_{IH}	input current HIGH	V_6 = 13.5 V	–	–	10	μA
I_{IL}	input current LOW	V_6 = 0 V	–10	–	–	μA
Input port P6						
I_{IH}	input current HIGH	V_7 = 13.5 V	–	–	10	μA
I_{IL}	input current LOW	V_7 = 0 V	–10	–	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA inputs						
V_{IH}	input voltage HIGH		3.0	–	5.5	V
V_{IL}	input voltage LOW		–	–	1.5	V
I_{IH}	input current HIGH	V_5 = 5 V, V_{CC} = 0 V; V_5 = 5 V, V_{CC} = 5 V	– –	– –	10 10	µA µA
I_{IL}	input current LOW	V_5 = 0 V, V_{CC} = 0 V; V_5 = 0 V, V_{CC} = 5 V	–10 –10	– –	– –	µA µA
Output SDA (open collector)						
I_{LO}	leakage current	V_4 = 5.5 V	–	–	10	µA
V_4	output voltage	I_4 = 3 mA	–	–	0.4	V
Charge-pump output PD						
I_{IH}	input current HIGH (absolute value)	CP = 1	90	220	300	µA
I_{IL}	input current LOW (absolute value)	CP = 0	22	50	75	µA
V_O	output voltage	in-lock	1.5	–	2.5	V
I_{1Leak}	off-state leakage current	T0 = 1	–5	–	5	nA
Operational amplifier output UD (test mode : T0 = 1)						
V_{18}	output voltage	V_{IL} = 0 V	–	–	100	mV
V_{18}	output voltage when switched-off	OS = 1; V_{IL} = 2 V	–	–	200	mV
G	operational amplifier current gain; $I_{18}/(I_1 - I_{1leak})$	OS = 0; V_{1L} = 2 V; I_{18} = 10 µA	2000	–	–	

Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with a single open-collector port active.

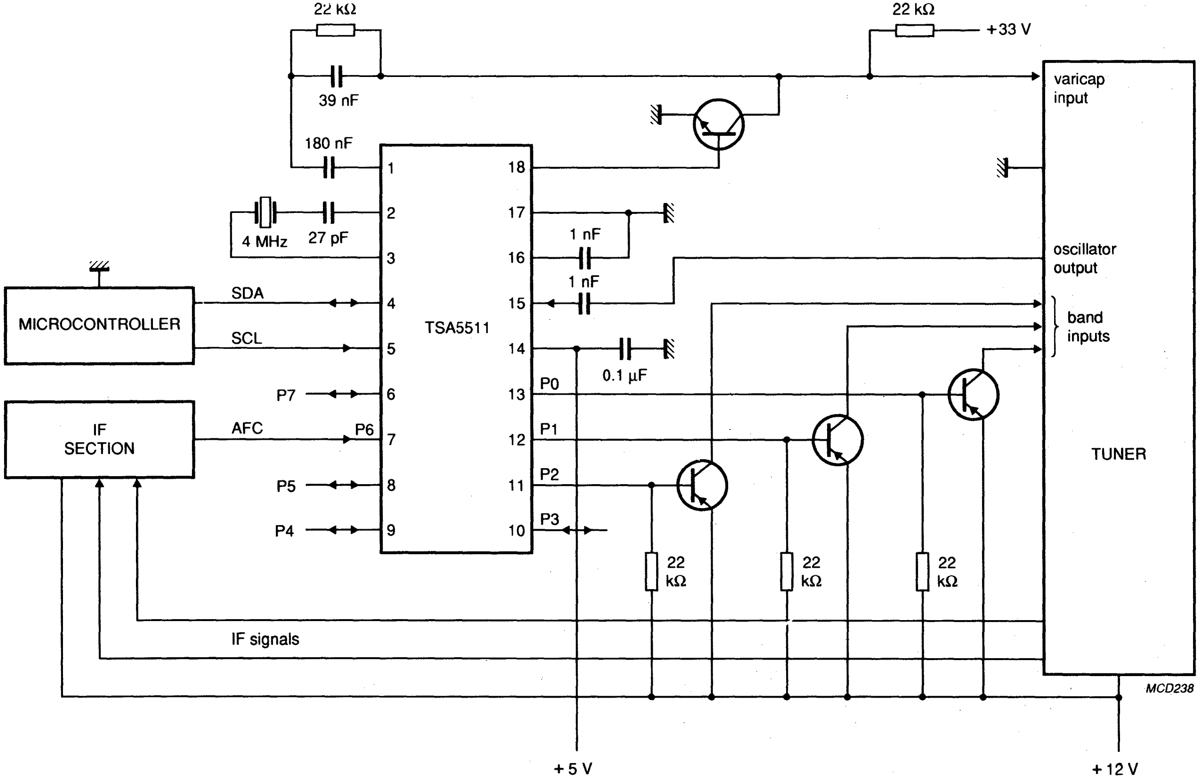


Fig.5 Typical application (DIL18).

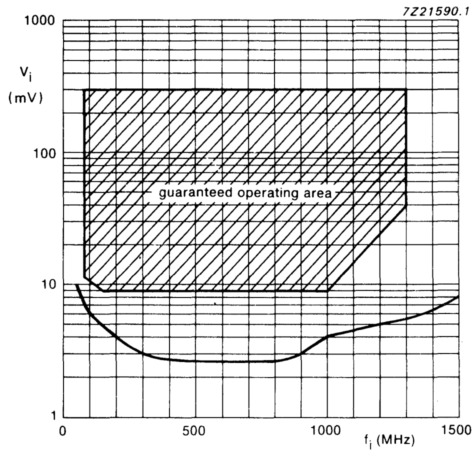


Fig.6 Prescaler typical input sensitivity curve; V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to +80 °C.

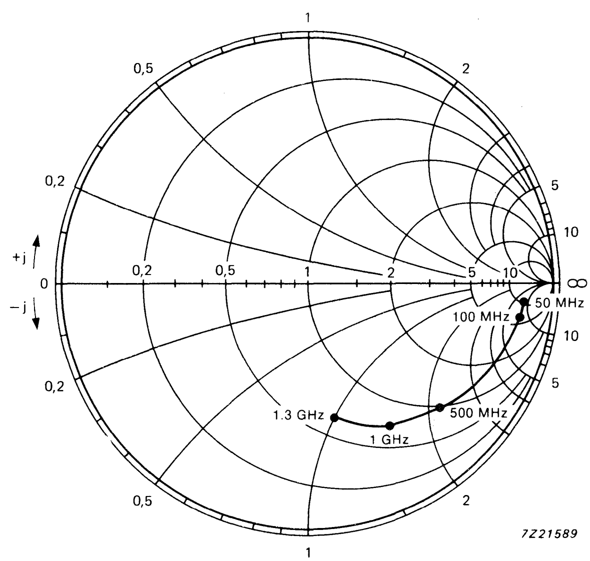


Fig.7 Prescaler Smith chart of typical input impedance; V_{CC} = 5 V; reference value = 50 Ω.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$\Delta f = \pm (K_{VCO}/K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$

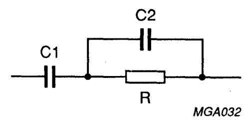


Fig.8 Loop filter.

where:

K_{VCO}	=	oscillator slope (Hz/V)
I_{CP}	=	charge-pump current (A)
K_O	=	4 x 10E6
C1 and C2	=	loop filter capacitors

FLOCK FLAG APPLICATION

- K_{VCO} = 16 MHz/V (UHF band)
- I_{CP} = 220 µA
- C1 = 180 nF
- C2 = 39 nF
- $\Delta f = \pm$ 27.5 kHz.

Table 5 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	µs
Time span between the loop losing lock and FL-flag resetting	0	128	µs

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

Frequency synthesizer for cellular radio communication — UMA1014T

FEATURES

- Single chip synthesizer solution;
- Compatible with Philips Cellular Radio chipset;
- Fully programmable RF divider;
- IIC two-line serial bus interface;
- On chip crystal oscillator \ TCXO buffer from 3 to 16 MHz;
- 16 reference division ratios allowing 5 to 100 kHz channel spacing;
- Crystal frequency divide-by-8 output;
- On chip out-of-lock indication ;
- Two VCO control outputs;
- Latched synthesizer alarm output;
- Status register including out-of-lock indication and power failure;
- Power down mode.

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC & VCP	Supply voltage range	4.5	5.0	5.5	V
ICC + ICP	Supply current	-	13	-	mA
ICCpd	ICC in power down	-	2.5	-	mA
FREF	Phase comparator reference frequency	5	-	100	KHz
RFin	RF frequency input	50	-	1100	MHz
Tamb	Operating temperature range	-40	-	85	°C

APPLICATIONS

- Cellular mobile radio (NMT, AMPS, TACS)
- Private Mobile Radio (PMR)
- Cordless telephones

GENERAL DESCRIPTION

The UMA1014T is a low power universal synthesizer which has been designed for use in channelized radio communications. The IC is manufactured in bipolar technology and is designed to operate from 5 to 100 kHz channel spacing with an RF input of 50 to 1100 MHz. The channel is programmed via the standard IIC bus. A low power sensitive RF divider is integrated as well as a dead zone eliminated tri-state phase comparator. A low noise charge pump delivers 1 mA or 1/2 mA output current enabling better compromise between fast switching and loop bandwidth. A power down circuit allows the synthesizer to be idled.

ORDERING AND PACKAGE INFORMATION

Extended Type number	Package			
	Pins	Pin Position	Material	Code
UMA1014T	16	SO16	plastic	SOT109A
UMA1014M	20	SSOP20	plastic	SOT266A

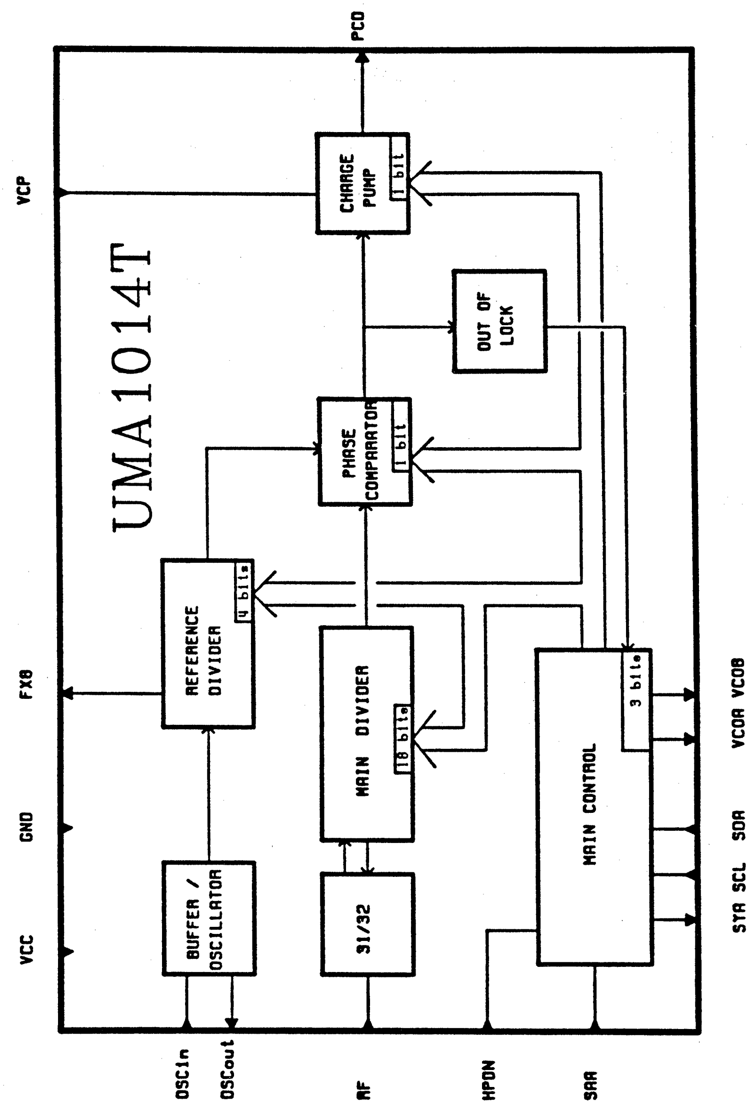
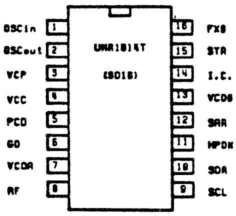
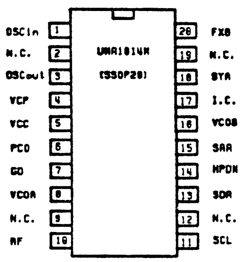


FIG. 1 Block diagram

FIG 2 PIN CONFIGURATION





PINNING

Symbol	Pin SO16	Pin SSOP20	Description
OSCin	1	1	Oscillator input or TCXO input
OSCout	2	3	Oscillator output
VCP	3	4	Charge pump 5 Volts supply
VCC	4	5	5 Volts supply
PCD	5	6	Charge pump output
GD	6	7	Ground
VCOA	7	8	VCO buffer switch output A (including out-of-lock)
RF	8	10	RF input
SCL	9	11	Serial clock line input
SDA	10	13	Serial data line input/output
HPDN	11	14	Hardware power down (low active)
SAA	12	15	Slave address select input A
VCOB	13	16	VCO buffer switch output B
I.C.	14	17	Internally connected (for test purpose only)
SYA	15	18	Synthesizer alarm output
FX8	16	20	1/8 crystal frequency output

N.C. = not connected

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

Symbol	Parameter	Min	Max	Unit
VCC	Supply voltage range	-0.3	7	V
Vi	Voltage range at pin i to ground	0	Vcc	V
Tstg	Storage temperature range	-55	+125	°C
Tamb	Operating ambient temperature range	-40	85	°C

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class A (method 3015-2). Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling Integrated Circuits.

FUNCTIONAL DESCRIPTION

The UMA1014T is a low power frequency synthesizer for radio communications which operates in the 50 to 1100 MHz range. The device includes an oscillator\buffer circuit, a reference divider, an RF main divider, a tri-state phase comparator, a charge pump and a control circuit which transfers the serial data into the four internal 8 bit-registers. The VCC supply feeds the logic part while VCP feeds the charge-pump only. Both supplies are +5 Volts (+/-10%). The power down facility puts the synthesizer in the idle mode (all current supplies are switched off except in the control part). Any IIC transfer is permitted during this mode and all information in the registers is retained allowing fast power-up.

MAIN DIVIDER.

The main divider is a fully programmable pulse swallow type counter. After a sensitive input amplifier (50 mV, -13 dBm), the RF signal is applied to a 31/32 dual-modulus counter. The output is then used as the clock for the 5-bit swallow counter R= (MD4,..., MD0) and the 13 bit main counter N= (MD17, ..., MD5). The ratio is sent via the IIC bus into the registers B, C and D. It is then buffered in a 18-bit latch. The ratio in the divider chain is updated with this new information only after the least significant bit (D0) is received. This update is synchronized to the output of the divider in order to limit the phase error during small jumps of the synthesized frequency.

MAIN COUNTER								SWALLOW COUNTER		
:N								:R		
MD17	MD16	MD15		MD8	MD7		MD5	MD4		MD0
B1	B0	C7	...	C0	D7	...	D5	D4	...	D0
MSB										LSB

Division ratio in the main divider

The main divider can be programmed to any value between 2048 and 262143 (i.e. 2^{18}-1). If a ratio X, which is less than 2048, is sent to the divider, the ratio (X+2048) will be programmed. For switching between adjacent channels it is possible to program only register D allowing shorter IIC programming time.

OSCILLATOR.

The oscillator is a common collector Colpitts type with external capacitive feedback. It has been designed to function also as a buffer when a TCXO or any clock is used. The oscillator has very small temperature drift and high voltage supply rejection. When acting as a buffer, no additional external components will be necessary.

REFERENCE DIVIDER.

The reference divider is semi-programmable with 16 division ratios which are selected via the IIC bus. The programming uses bits A3 to A0 of register A as shown below. These ratios can be used with crystal frequencies from 3 to 16 MHz. All popular channel spacings can be obtained from a single crystal / TCXO frequency of 9.6 MHz.

A3 RD3	A2 RD2	A1 RD1	A0 RD0	reference division ratio	Channel spacing for 9.6 MHz at OSCin
0	0	0	0	128	75 kHz
0	0	0	1	160	60 kHz
0	0	1	0	192	50 kHz
0	0	1	1	240	40 kHz
0	1	0	0	256	37.5 kHz
0	1	0	1	320	30 kHz
0	1	1	0	384	25 kHz
0	1	1	1	480	20 kHz
1	0	0	0	512	18.75 kHz
1	0	0	1	640	15 kHz
1	0	1	0	768	12.5 kHz
1	0	1	1	960	10 kHz
1	1	0	0	1024	9.375 kHz
1	1	0	1	1280	7.5 kHz
1	1	1	0	1536	6.25 kHz
1	1	1	1	1920	5 kHz

reference divider programming

PHASE COMPARATOR AND CHARGE PUMP.

The block diagram of the phase comparator and charge pump is shown below. The phase comparator is both a phase and frequency detector. It comprises dual flip-flops together with logic circuitry which eliminates the dead zone. When a phase error is detected, the UP or DOWN signal becomes high . It switches on the corresponding current generator which sources or sinks current as appropriate into the loop filter. When no phase error is detected, PCD goes tristate. The final tuning voltage of the VCO is provided by the loop filter. The charge pump current is programmable via the IIC bus. When bit IPCD (bit A5) is set to logic 1, the charge pump will deliver 1 mA. When IPCD is logic 0, the charge pump will deliver 0.5 mA.

The phase comparator has a phase inverter logic input (PHI). This allows the use of inverted or non-inverted loop filter configurations. It is thus possible to use a passive loop filter which can offer high performance without an operational amplifier. The function of the phase comparator and charge pump is given in the table below and a typical transfer curve is shown overleaf.

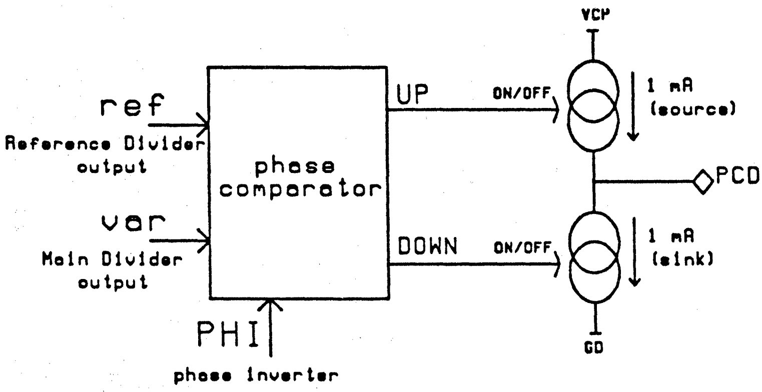


FIG. 3 Phase comparator and charge pump

	PHI = 0	(Passive loop filter)		PHI = 1	(Active loop filter)	
	Fref<Fvar	Fref>Fvar	Fref=Fvar	Fref<Fvar	Fref>Fvar	Fref=Fvar
UP	0	1	0	1	0	0
DOWN	1	0	0	0	1	0
Ipcd	- 1 mA	1 mA	< +/- 5 nA	1 mA	- 1 mA	< +/- 5 nA

Operation of the phase comparator

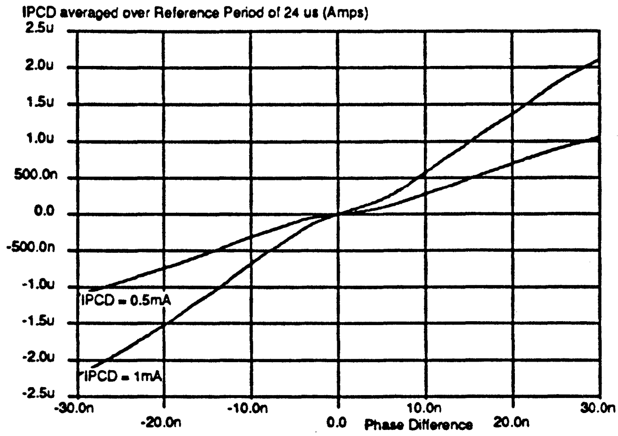


FIG. 4 Gain of phase detector and charge pump

OUT-OF-LOCK DETECTOR.

An out-of-lock detector using the UP and DOWN signals from the phase comparator is included on chip. Pin VCOA is an open collector output which is forced low during out-of-lock. This information is also available via the IIC bus in the status register. When the phase error (measured at the phase comparator) is greater than approximately 200 ns, an out-of-lock condition is immediately flagged. The flag is only released after 6 reference cycles of phase error less than 200 ns.

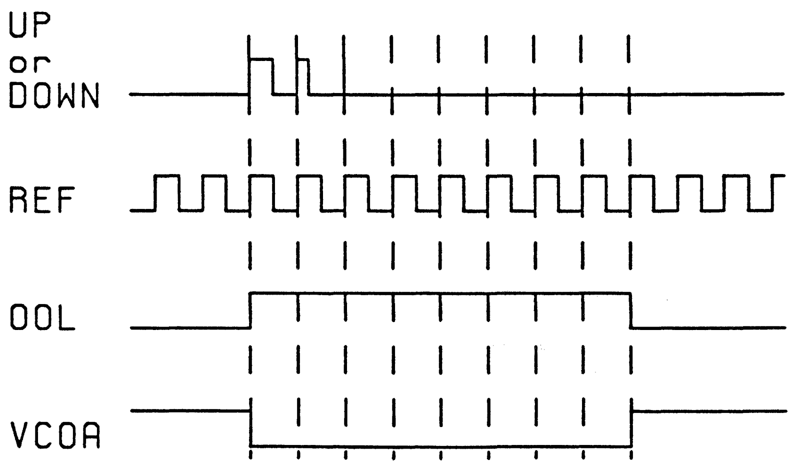


FIG. 5 Out-of-lock function

MAIN CONTROL

The control part consists mainly of the IIC control interface and a set of four registers, A, B, C and D. The serial input data (SDA) is converted to 8 bit parallel words and stored in the appropriate registers. The data transmission to the synthesizer is executed in the burst mode with the following format:

//slave addr./subaddr./data1/data2/.../datan// ; n up to 4.

Data byte 1 is written in the register indicated by the subaddress. An auto-increment circuit if enabled (AVI=1) then provides the correct addressing for the following data bytes. Since the length of the data burst is not fixed, it is possible to program the whole set of registers or just one. The registers are structured in such a way so that the burst, for normal operation, is kept as short as possible. The bits that are only programmed during the set-up (reference division ratio, power down, phase inversion and current on PCD) are stored in registers A and B.

In the slave address, six bits are fixed. The remaining two bits depend on the application.

1	1	0	0	0	1	SAAN	R/WN

Slave address

SAAN is the slave address select not. When SAA (pin 12) is high, then SAAN = 0, and when pin 12 goes low SAAN = 1. This allows the use of two UMA1014Ts on the same IIC bus with a different address. R/WN (read/write not) should be set to 0 when writing to the synthesizer or set to 1 when reading the status register.

The subaddress includes the register pointer, and sets the flags related to the auto-increment (AVI) and the alarm disable (DI) :

x	x	x	DI	AVI	x	SB1	SB0

Subaddress

DI (Disable Interrupt); DI=1 disables SYA alarm
DI=0 allows SYA alarm
AVI (Auto Value Increment); AVI=1 enables auto-increment
AVI=0 disables auto-increment
SB1/SB0 point to the register where DATA1 will be written. (see table attached)
x means not used.

SB1	SB0	register pointed
0	0	A
0	1	B
1	0	C
1	1	D

Pointer of the registers

MAIN CONTROL (continued)

When the auto-increment is disabled (AVI=0) , the subaddress pointer will maintain the same value during the IIC bus transfer. All the databytes will then be written consecutively in the same register pointed to by the subaddress.

STATUS REGISTER and synthesizer alarm.

When an out-of-lock condition or a power dip occurs, open collector output SYA (pin 15) is forced low and latched. The pin SYA will be only released after the status register is read via the IIC bus.

The status register contains information as shown below:

0	0	0	OOL	0	LOOL	LPD	DI

where :

OOL	momentary out-of-lock
LOOL	latched out-of-lock
LPD	latched power dip
DI	disable interrupt (of the last write cycle)

The IIC bus protocol to read this internal register is a single byte without subaddressing:

//slave address (R/WN=1)/status register (read)//

MAIN CONTROL (continued)

BIT ALLOCATION :

BIT ALLOCATION										
register.	pointer.	7	6	5	4	3	2	1	0	preset
A	00	PD	X	IPCD	X	RD3	RD2	RD1	RD0	00001110
B	01	1	0	1	PHI	VCOB	VCOA	MD17	MD16	10100101
C	10	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	00111000
D	11	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	10000000

X means not used

register name	bit name	function		preset value
A	PD	power down	PD=0 normal operation	0
	IPCD	programmable current in PCD	IPCD=1 : 1mA IPCD=0 : 1/2mA	0
	RD3...RD0	reference ratio	see table	1110; r=1536
B	PHI	phase inverter	PHI=0 passive loop filter	0
	VCOA	VCO switch A	set the pin 7	1
	VCOB	VCO switch B	set the pin 13	0
	MD17 MD16	bits 17 and 16	MSB of main divider ratio	0 1
C	MD15 ... MD8	bits 15 ... 8	main divider ratio	00111000
	MD7 ... MD0	bits 7 ... 0	main divider ratio	10000000 r=80000

Registers in UMA1014T

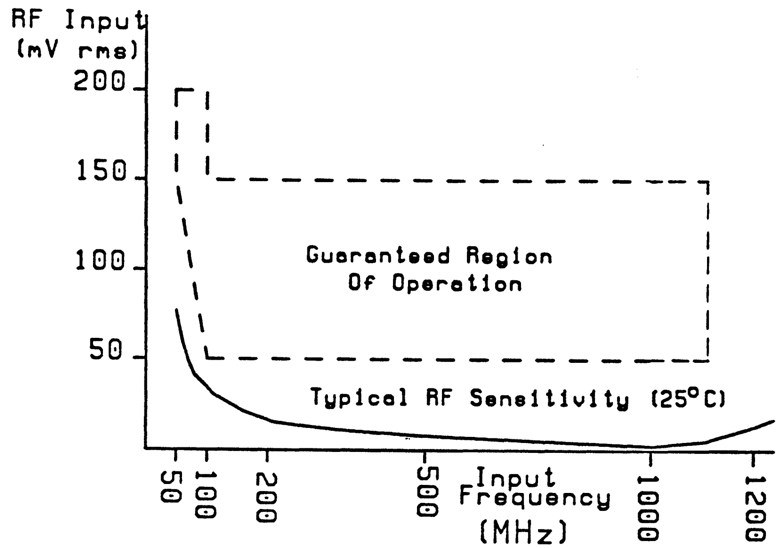
CHARACTERISTICS

Vcc = 4.5 to 5.5V ; 25 deg; unless otherwise specified.

Symbol	Parameter	Conditions	Min..	Typ.	Max.	Unit.
Supply (pins VCC & VCP).						
VCC	Supply voltage range		4.5	-	5.5	V
ICC	Supply current		-	11.5	-	mA
ICCpd	Supply current	power down	-	2.5	-	mA
VCP	Supply voltage of the charge pump		4.5	-	5.5	V
ICP	Supply current C-P	IPCD=0.5mA	-	1.4	-	mA
ICPpd	Supply current C-P	power down	-	0.01	-	mA
RF dividers (pin RF)						
F_{RF}	Frequency range		50	-	1100	MHz
V_{RFrms}	input voltage level	50 to 100 MHz	150	-	200	mV
		100 to 1100 MHz	50	-	150	mV
Rin	Input resistance	at 1 GHz	-	200	-	Ω
		at 100 MHz	-	600	-	Ω
Cin	Input Capacitance*		-	2	-	pF
R_{RF}	Division ratios		2048	-	262143	-
* Note: Cin in parallel with Rin						
Oscillator and reference divider (pins OSCin, OSCout)						
FOSC	Oscillator frequency range		3	-	16	MHz
VOSC(rms)	Input level sine wave		0.1	-	VCC + 2.8	Vrms
VOSC(p-p)	Input level square wave		0.3	-	VCC	Vpp
Z_{OSCout}	output impedance at OSCout pin		-	-	2	KΩ
R_{REF}	Reference division ratio	see table	128	-	1920	-
F_o	Output frequency range		5	-	100	KHz

CHARACTERISTICS (continued)

Symbol	Parameter	Conditions	Min..	Typ.	Max.	Unit.
1/8 crystal frequency open collector output (pin FX8)						
I_{OL}	Current output low	$V_{OL} \geq 0.6$ V	1	-	-	mA
Phase comparator (pin PCD)						
F_{PCD}	Frequency range		5		100	KHz
I_{PCD}	Output current V_{PCD} = 2.5 V	Bit IPCD = 1	0.8	1	1.3	mA
		Bit IPCD = 0	0.4	0.5	0.7	mA
I_{PCDlk}	Output leakage current		-5	+/- 1	5	nA
V_{PCD}	Output voltage		0.4		V_{CP}-0.5	V
Serial clock input, serial data input (pins SDA, SCL)						
Fclk	clock frequency		0	-	100	KHz
VIH	input voltage high		3	-	-	V
VIL	input voltage low		-	-	1.5	V
IIH	input current high		-	3	10	µA
IIL	input current low		-10	-5	-	µA
CI	input capacitance		-	-	10	pF
IOL	SDA sink current	VOL = 0.4 V	-	-	3	mA
Slave address select input (pin SAA) hardware power down input (pin HPDN)						
VIH	input voltage high		3	-	-	V
VIL	input voltage low		-	-	0.4	V
IIH	input current high		-	-	0.1	µA
IIL	input current low		-10	-	-	µA
VCO output switches (pins VCOA, VCOB), synthesizer alarm (pin SYA)						
VOL	output voltage low	note 1	-	-	0.4	V
IOL	sink current low		400	-	-	µA
Note : 1. The pin VCOA is forced to zero state during out-of-lock						



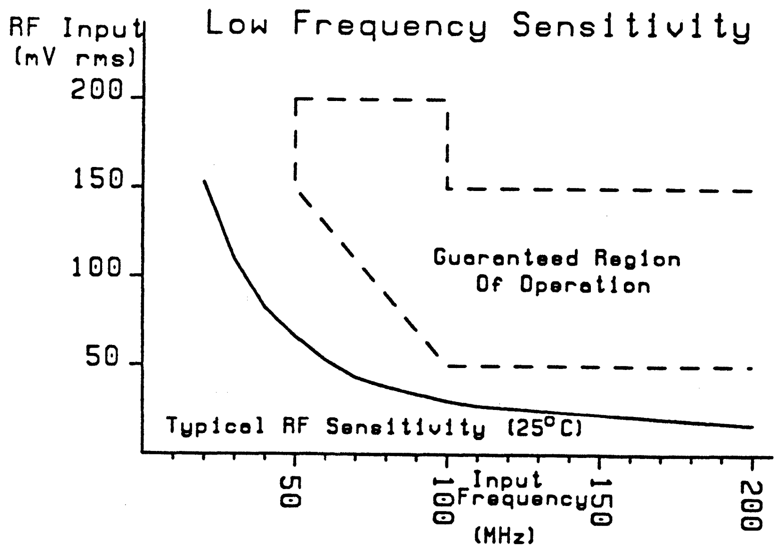
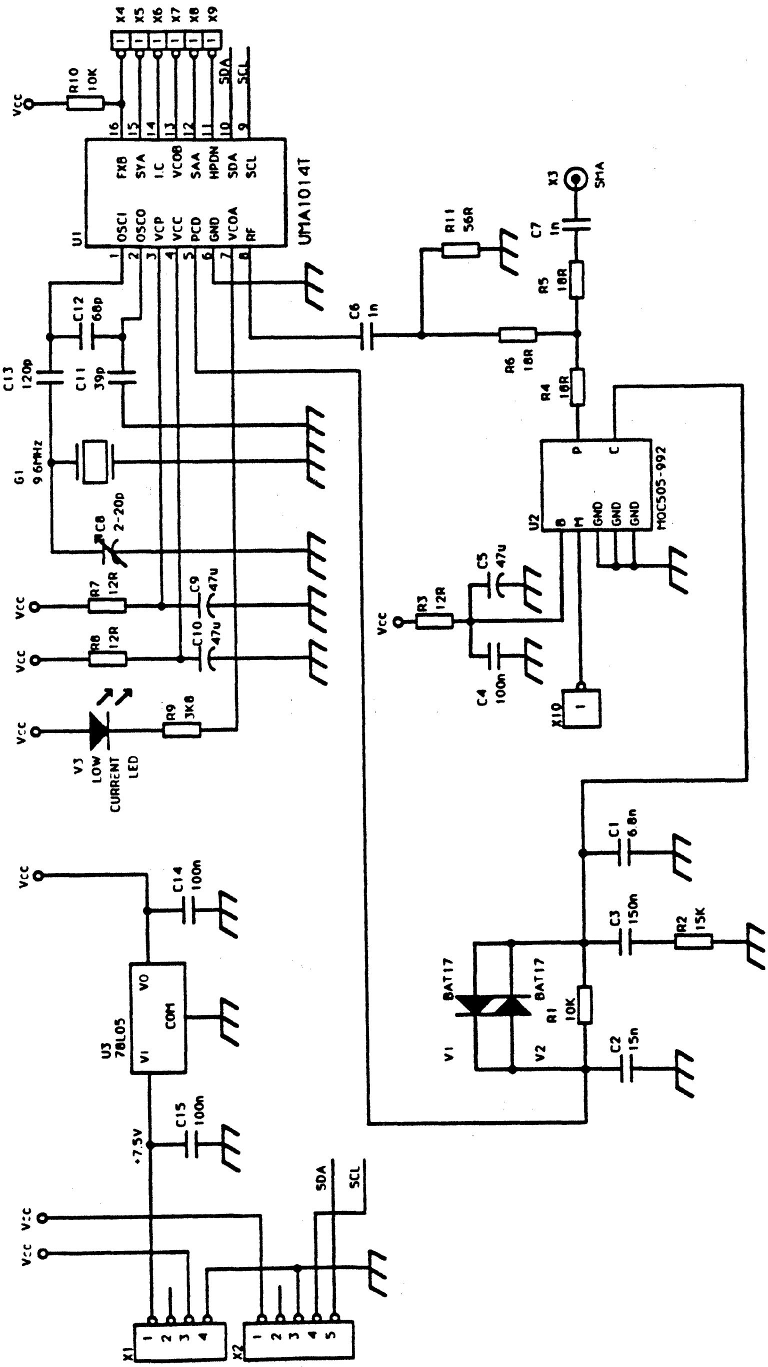


FIG. 6 RF Input Sensitivity

Frequency synthesizer for cellular radio communication

UMA1014T



DESCRIPTION

The UMF1005 is a low power, high performance frequency synthesizer in CMOS technology. This integrated circuit is designed to achieve 10-2000 KHz channel spacing. The channel is selected via a high speed serial interface.

FEATURES

- Fast locking by "Fractional-N" divider
- Auxiliary synthesizer.
- Digital phase comparator with proportional and integral charge pump output.
- High speed serial input.
- Low power consumption.

Applications

- Mobile telephony
- Portable battery-powered radio equipment

Package outlines

UMF1005T: 20-lead plastic mini-pack; (SSOP20,SOT266)

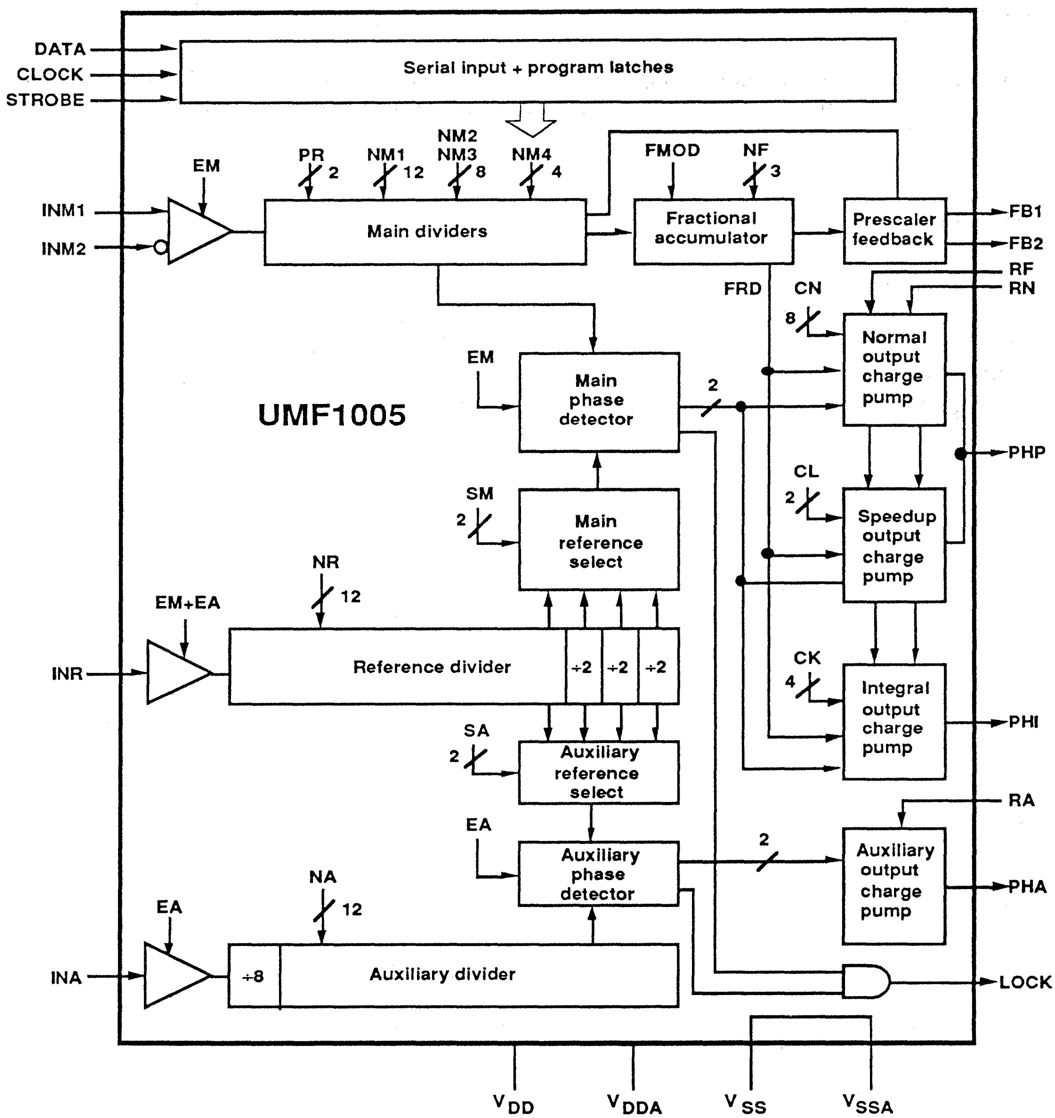


Fig. 1: Block diagram UMF 1005T

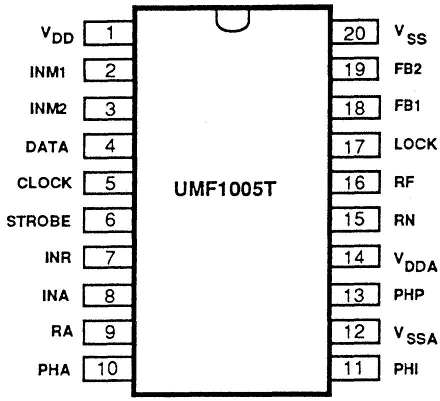


Fig. 2: Pinning UMF1005T

PINNING

Symbol	Pin	Description
V_{DD}	1	digital supply voltage
INM1	2	main divider positive input
INM2	3	main divider negative input
DATA	4	serial data input line
CLOCK	5	serial clock input line
STROBE	6	serial strobe input line
INR	7	reference divider input line
INA	8	auxiliary divider input line
RA	9	auxiliary current setting; resistor to V_{SS}
PHA	10	auxiliary phase detector output
PHI	11	integral phase detector output
V_{SSA}	12	analog ground; internally connected to V_{SS}
PHP	13	proportional phase detector output
V_{DDA}	14	analog supply voltage
RN	15	main current setting; resistor to V_{SS}
RF	16	frac. comp. current setting; resistor to V_{SS}
LOCK	17	lock detector output
FB1	18	feedback output for prescaler modulus control
FB2	19	feedback output for prescaler modulus control
V_{SS}	20	common ground connection

Serial programming input

The serial input is a 3 wire input (CLOCK, STROBE, DATA) to program all counter ratios, DAC's, selection and enable bits. The programming data is structured into 24 or 32 bit words; each word includes 1 or 4 address bits. Figure 3 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent: D, C, B and A. Figure 4 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for NM4, CN, and PR is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24 bit A0 word is used. CN will be directly loaded by programming a long 32 bit A1 word. The flag LONG in the D word determines whether A0 (LONG = "0") or A1 (LONG = "1") format is applicable. The A word contains new data for the main divider. The A word is loaded only when a main divider synchronization signal is also active, to avoid phase jumps when reprogramming the main divider. The synchronisation signal is generated by the main dividers. It disables the loading of the A word each main divider cycle during maximum 300 main divider input cycles. To be sure that the A word will be correctly loaded the STROBE signal must be H for at least 300 main divider input cycles. Programming the A word means also that the main charge pumps on output PHP and PHI are set into the speed-up mode as long as the STROBE is H.

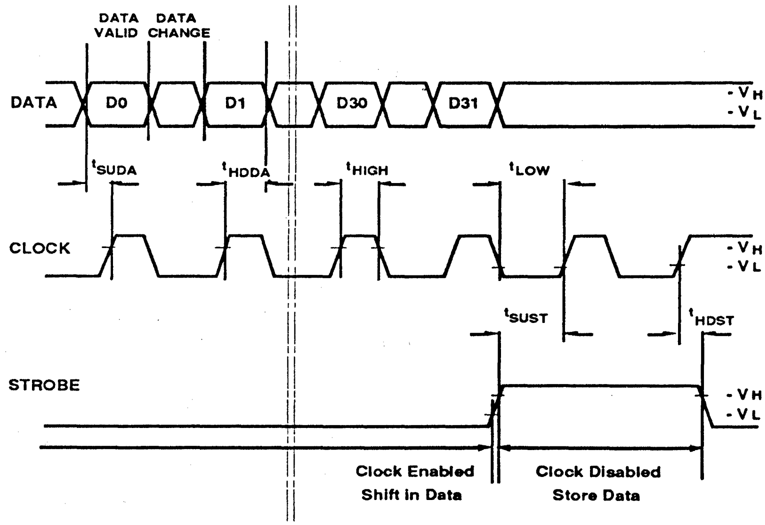


Fig. 3 Serial Input timing sequence

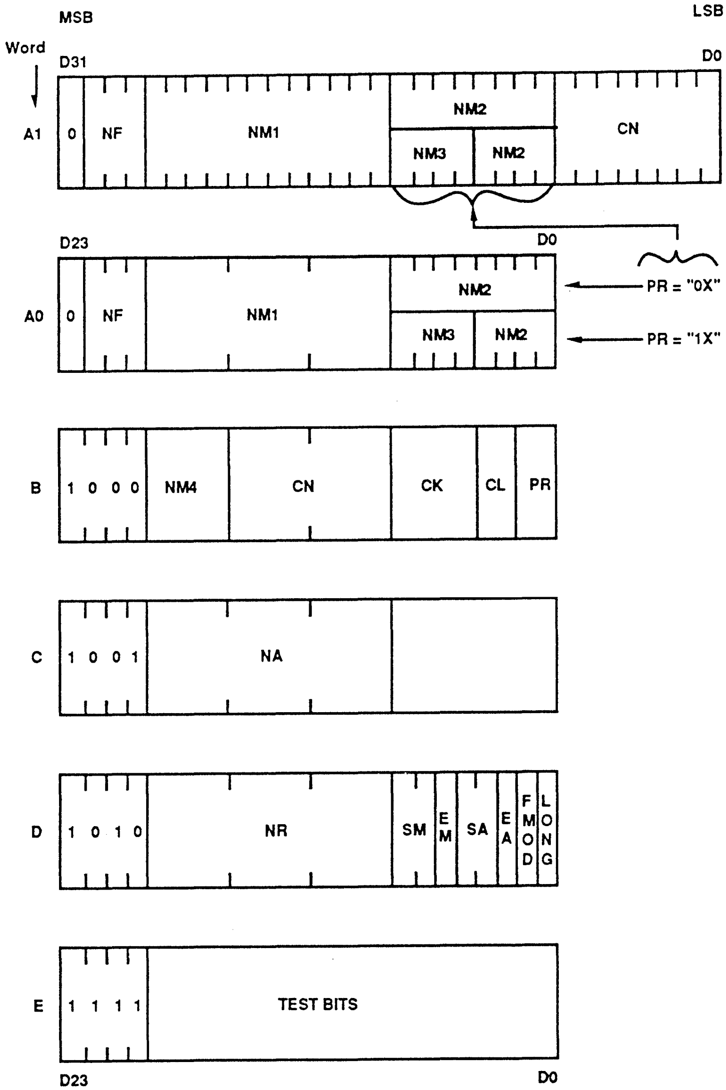


Fig. 4 Serial input word format

Symbol	Bits	Function
NM1	12	number of main divider cycles when prescaler is programmed in ratio R1 (FB1 = "1", FB2 = "0")*
NM2	8 if PR = "0x" 4 if PR = "1x"	number of main divider cycles when prescaler is programmed in ratio R2 (FB1 = "0", FB2 = "0")*
NM3	4 if PR = "1x"	number of main divider cycles when prescaler is programmed in ratio R3 (FB1 = "0", FB2 = "1")*
NM4	4 if PR = "11"	number of main divider cycles when prescaler is programmed in ratio R4 (FB1 = "0", FB2 = "1")*
PR	2	prescaler type in use PR = "00": modulus 2 prescaler PR = "10": modulus 3 prescaler PR = "11": modulus 4 prescaler
NF	3	fractional - N increment
FMOD	1	fractional - N modulus selection flag "1" : modulo 8
LONG	1	A word format selection flag "0": 24 bit A0 format "1": 32 bit A1 format
CN	8	current setting factor for main charge pumps
CL	2	acceleration factor for proportional charge pump current
CK	4	acceleration factor for integral charge pump current
EM	1	main divider enable flag
EA	1	auxiliary divider enable flag
SM	2	reference select for main phase detector
AM	2	reference select for aux. phase detector
NR	12	reference divider ratio
NA	12	auxiliary divider ratio

* not including reset cycles and fractional - N effects.

Auxiliary variable divider
The input signal on INA is amplified to logic level by a single ended input buffer, which accepts low level AC coupled input signals. This input stage is enabled if the serial control bit EA = "1". Disabling means that all currents in the buffer are switched off. A fixed divide by 8 divider is the first stage of the counter, which has been optimized to accept a 100 MHz input signal. The second stage is a 12-bit programmable counter. The total division ratio can be expressed as:

N Aux = 8 x NA; with NA = 4 to 4095

Reference variable divider (fig. 5)

The input signal on INR is amplified to logic level by a single ended input buffer, which accepts low level AC coupled input signals. This input stage is enabled by the OR function of the serial intput bits EA and EM. Disabling means that all currents are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 4095) followed by a three bit binary counter. The 2 bit SM determines which of the 4 output pulses is selected as main phase detector input. The 2 bit SA determines the selection of the auxiliary phase detector signal. To obtain the best time spacing for the main and auxiliary reference signals, the opposite output will be used for the auxiliary phase detector, reducing the possibility of unwanted interactions. For this reason the programmable divider produces a symmetric output pulse for even ratios and a 1 input cycle asymmetric pulse for odd ratios.

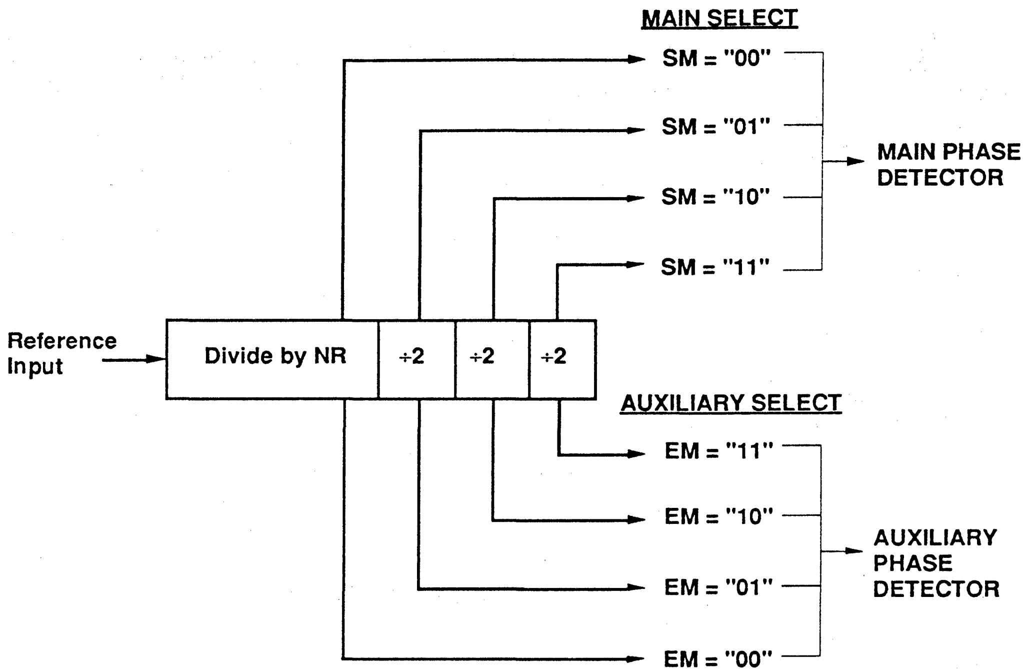


Fig. 5 Reference variable divider

Main variable divider

The input signals on INM1, INM2 are amplified to a logic level by a balanced input comparator giving a common mode rejection. This input stage is enabled by serial control bit EM = 1. Disabling means that all currents in the comparator are switched off. The main divider is built up by a 12 bit counter plus a sign bit. Depending on the serial input values NM1, NM2, NM3, NM4 and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles according to the following table:

Counter Status	FB1	FB2	Prescaler ratio
(-NM1 - 1) to 0	1	0	R1
(-NM1 - 1) to -1	1	0	R1*
1 to NM2	0	0	R2
0 to NM2	0	0	R2*
0 to NM3	0	1	R3 if PR = "1X"
0 to NM4	1	1	R4 if PR = "11"

* when the fractional accumulator overflows

The total division ratio from prescaler to the phase detector may be expressed as:

$$N = (NM1 + 2) \times R1 + NM2 \times R2 + [(NM3 + 1) \times R3 + [(NM4 + 1) \times R4]]$$

or when the fractional accumulator overflows:

$$N' = (NM1 + 1) \times R1 + (NM2 + 1) \times R2 + [(NM3 + 1) \times R3 + [(NM4 + 1) \times R4]]$$

with prescaler ratio R2 = R1 + 1 --> N' = N + 1

PR defines the prescaler type in use and the bit capacity for NM2, NM3 according to the following table:

PR	Modulus prescaler	Bit capacity			
		NM1	NM2	NM3	NM4
00	2	12	8	-	-
01	2	12	8	-	-
10	3	12	4	4	-
11	4	12	4	4	4

When a number of prescaler ratios is set on 2, respectively 3, the reset cycles for R3, respectively R4 will also not occur. Programming to e.g. 2 prescaler ratios will result in an overall divider ratio:

$$N = (NM1 + 2) \times R1 + NM2 \times R2$$

The loading of the work registers NM1, NM2, NM3, NM4, PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as is explained in the Serial Programming Input chapter.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = "1". Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1. As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider cycles will then be:

NQ = (NM1 + NM2 +2) x R1 + [(NM3 + 1) x R3 + [(NM4 + 1) x R4] + NF / Q

Programming a fraction means the prescaler with main divider will divide by N or N + 1. The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

Phase detectors (fig. 6)

The auxiliary and main phase detectors are a 2 D-type flipflop phase and frequency detector. The flipflops are set by the negative edges of output signals of the dividers. The reset inputs are activated when both flipflops have been set and when the reset enable signal is active (L). Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flipflops drive on-chip charge pumps. A pull-up current from the charge pump indicates the VCO frequency shall be increased while a pull-down pulse indicates the VCO frequency shall be decreased.

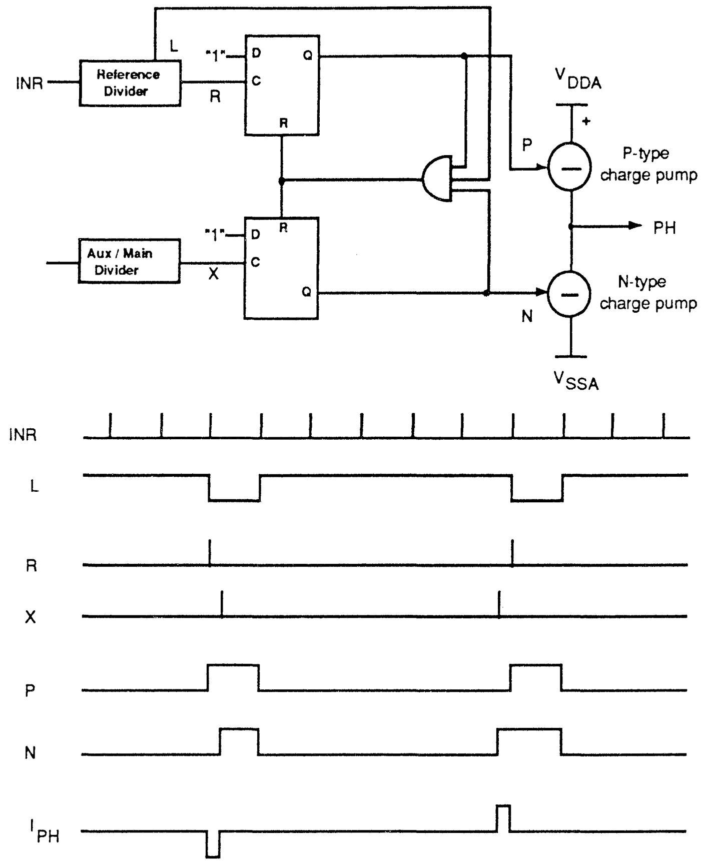


Fig. 6 Phase detector structure with timing

Current settings

The UMF1005 has 3 current setting pins RA, RN, and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current in the current setting pins. This current I_R can be set by an external resistor to be connected between the current setting pin and V_{SS}. The typical value R (current setting resistor) can be calculated with the formula:

$$R = (V_{DDA} - 1.1 - 80 \times SQRT(I_R)) / I_R$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary output charge pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor RA at pin RA. The active charge pump current is typically:

$I_{PHA} = 8 \times I_{RA}$

Main output charge pumps and fractional compensation currents

The main charge pumps on pin PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 7 shows the waveforms for a typical case.

When the serial input A word is loaded, the output circuits are in the "speed-up mode" as long as the STROBE is H, else the "normal mode" is active. In the "normal mode" the current output PHP is:

$I_{PHP\_N} = I_{pump10} + I_{comp10}$

where:

$I_{pump10} = \pm CN \times I_{RN} / 32$:charge pump current
$I_{comp10} = \pm FRD \times I_{RF} / 128$:fractional compensation current

The current in PHI is in "normal mode" zero.
In "speed-up mode" the current in output PHP is:

$I_{PHP\_S} = I_{PHP\_N} + I_{pump11} + I_{comp11}$

where:

$I_{pump11} = I_{pump10} \times 2^{(CL+1)}$:charge pump current
$I_{comp11} = I_{comp10} \times 2^{(CL+1)}$:fractional compensation current

In "speed-up mode" the current in output PHI is:

$I_{PHI\_S} = I_{pump21} + I_{comp21}$

where:

$I_{pump21} = I_{pump11} \times CK$:charge pump current
$I_{comp21} = I_{comp11} \times CK$:fractional compensation current

Figure 7 shows that for a proper fractional compensation the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output. This means that the current setting on the input RN, RF must have the following ratio:

$I_{RN} / I_{RF} = (Q \times f_{VCO}) / (2 \times CN \times f_{IRA})$

where: Q : fractional-N modulus
$f_{VCO} = f_{INM} \times N$: input frequency of the prescaler

Lock detect

The output LOCK is H when the auxiliary phase detector AND the main phase detector indicates a lock condition. The lock condition is defined as a phase difference of less than ±1 cycle on the reference input INR. The look condition is also fullfilled when the relative counter is disabled (EM = "0" or respectively EA = "0") for the main, respectively auxiliary counter.

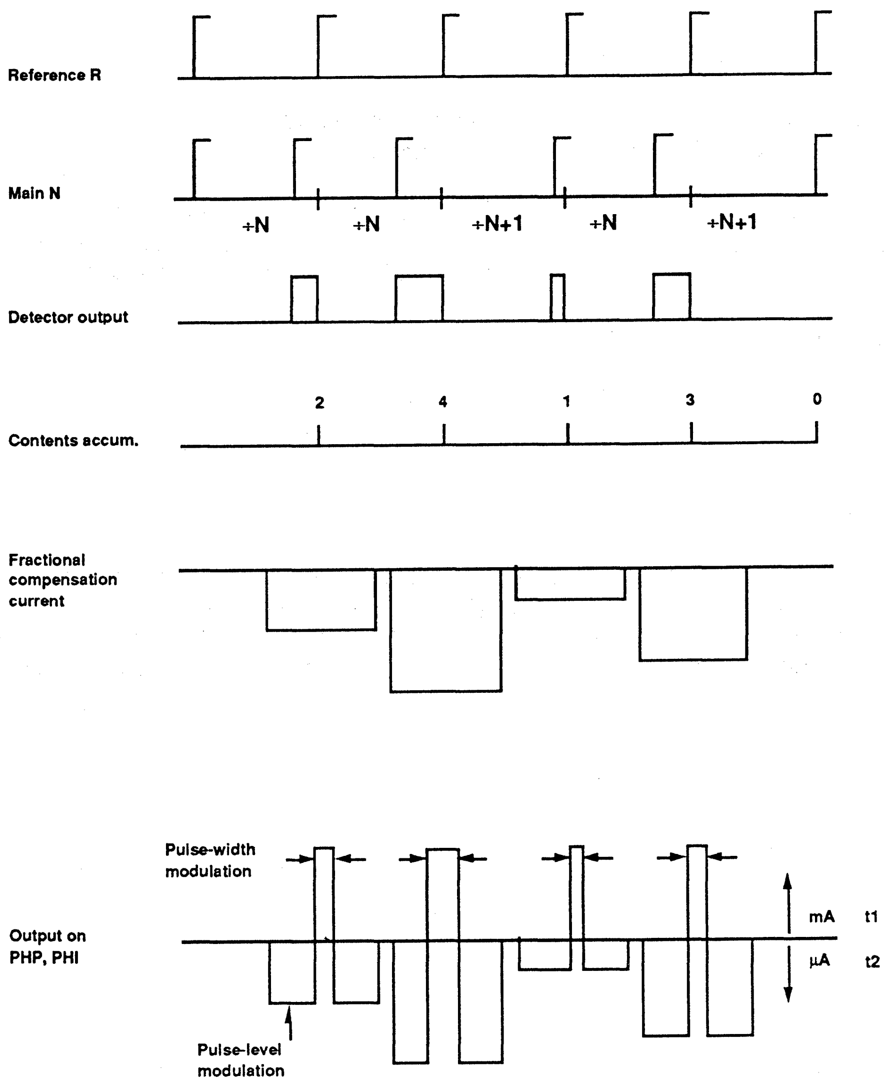


Fig. 7 Waveforms for NF=2, Fraction=0.4

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

Symbol	Parameter	Min	Max	Unit
V_{DD}	supply voltage	-0.5	6.5	V
VI	voltage on any input	-0.5	V_{DD} + 0.5	V
I	DC current into any input or output	-10	10	mA
P_{tot}	total power dissipation		tbf	mW
Tstg	storage temperature range	-65	150	°C
Tamb	operating ambient temperature range	-40	85	°C

DC CHARACTERISTICS

$V_{DD} = V_{DDA} = 4.5$ to 5.5 V; $T_{amb} = -40$ to + 85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	standby digital supply current	ENM=ENA=0; inputs on V_{DD} or 0	-	-	1	µA
I_{DD}	Operational supply current	ENM=ENA=1; $f_{INM}=f_{REF}=10$ MHz $f_{INA}=50$ MHz	-	-	tbf	µA
I_{DDA}	Standby analog supply currents	$V_{RA}= V_{DDA}$; $V_{RF} = V_{DDA}$; $V_{RN}=V_{DDA}$	-	-	1	µA
I_{DDA}	Operational analog supply current		-	-	tbf	µA

Digital outputs FB1, FB2, LOCK

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output voltage LOW	IO = 1 µA	-	-	50	mV
V_{OL}	Output voltage LOW	IO = 2 mA	-	-	0.4	V
V_{OH}	Output voltage HIGH	IO = -1 µA	V_{DD}-50	-	-	mV
V_{OH}	Output voltage HIGH	IO = -2 mA	V_{DD}-0.5	-	-	V

Charge pump PHA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{PHA}	output current PHA	$I_{RA} = -62.5$ µA; $V_{PHA} = V_{DD} / 2$	±450	±500	±550	µA
I_{PHA}	output current PHA	$I_{RA} = -6.25$ µA; $V_{PHA} = V_{DD} / 2$	±45	±50	±55	µA
$\Delta I_{PHA}/\|I_{PHA}\|$	relative output current variation PHA	$I_{RA} = -62.5$ µA; note 2	-	-	10	%

Charge pump PHP, normal mode (note 1), I_{RN} = -5 to -100 µA, $V_{RF} = V_{DD}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{PHP}	output current PHP	CN x I_{RN} = -16 mA; $V_{PHP} = V_{DD} / 2$	±450	±500	±550	µA
I_{PHP}	output current PHP	CN x I_{RN} = -1.6 mA; $V_{PHP} = V_{DD} / 2$	±45	±50	±55	µA
$\Delta I_{PHP}/\|I_{PHP}\|$	relative output current variation PHP	CN x I_{RN} = -1.6 mA; note 2	-	-	10	%
	CN monotonic output current range PHP	CN = 0 to255; V_{PHP} = 0.4 to V_{DD} - 0.4 V	0	-	±500	µA

Charge pump PHP, speed up mode (note 1), I_{RN} = -5 to -100 μA, $V_{RF} = V_{DD}$

I_{PHP}	output current PHP	CN x $(2^{(CL+1)}+1)$ x I_{RN} = -96 mA; $V_{PHP} = V_{DD}/2$	±2.5	±3.0	±3.5	mA
I_{PHP}	output current PHP	CN x $(2^{(CL+1)}+1)$ x I_{RN} = -9.6 mA; $V_{PHP} = V_{DD}/2$	±0.25	±0.30	±0.35	mA
$\Delta I_{PHP}/\lvert I_{PHP}\rvert$	relative output current variation PHP	CN x $(2^{(CL+1)}+1)$ x I_{RN} = -96 mA; note 2	-	-	10	%
	CN monotonic output current range PHP	CN = 0 to 255; V_{PHP} = 0.4 to V_{DD} - 0.4 V	0	-	±3.0	mA

Charge pump PHI, speed up mode (note 1), I_{RN} = -5 to -100 μA, $V_{RF} = V_{DD}$

I_{PHI}	output current PHI	CN x $2^{(CL+1)}$ x CK x I_{RN} = -320 mA; $V_{PHI} = V_{DD}/2$	±8	±10	±12	mA
I_{PHI}	output current PHI	CN x $2^{(CL+1)}$ x CK x I_{RN} = -32 mA; $V_{PHI} = V_{DD}/2$	±0.8	±1.0	±1.2	mA
$\Delta I_{PHI}/\lvert I_{PHI}\rvert$	relative output current variation PHI	CN x $2^{(CL+1)}$ xCK x I_{RN} = -320 mA ; note2	-	-	15	%
	CN monotonic output current range PHI	CN = 0 to 255; V_{PHI} = 0.4 to V_{DD}-0.4 V	0	-	±10	mA

Fractional compensation PHP, normal mode (note 1), I_{RF} = -5 to -100 μA, $V_{RN} = V_{DD}$

I_{PHP_F} / FRD	fractional comp. output current PHP versus FRD note 3	I_{RF} = -76.8 μA; FRD = 1 to 7	-700	-600	-500	nA
I_{PHP_F} / FRD	fractional comp. output current PHP versus FRD note 3	I_{RF} = -7.68 μA; FRD = 1 to 7	-70	-60	-50	nA

Fractional compensation PHP, speed up mode (note 1), I_{RN} = -5 to -100 μA, $V_{RN} = V_{DD}$

I_{PHP_F} / FRD	fractional compensation output current PHP versus FRD note 3	$(2^{(CL+1)}+1) \times I_{RF}$ = -460.8 μA; FRD = 1 to 7	-4.5	-3.6	-2.7	mA
I_{PHP_F} / FRD	fractional compensation output current PHP versus FRD note 3	$(2^{(CL+1)}+1) \times I_{RF}$ = -46.08 μA; FRD = 1 to 7	-0.45	-0.36	-0.27	mA

Fractional compensation PHI, speed up mode (note 1), I_{RN} = -5 to -100 μA, $V_{RN} = V_{DD}$

I_{PHI_F} / FRD	fractional compensation output current PHI versus FRD note 3	$2^{(CL+1)} \times CK \times I_{RF}$ = -1536 μA; FRD = 1 to 7	-16	-12	-8	μA
I_{PHI_F} / FRD	fractional compensation output current PHI versus FRD note 3	$2^{(CL+1)} \times CK \times I_{RF}$ = -153.6 μA; FRD = 1 to 7	-1.6	-1.2	-0.8	μA

Charge Pump Leakage Currents

I_{PHP_L}	output leakage current PHP	$V_{RF} = V_{DDA}$ $V_{RN} = V_{DDA}$ V_{PHP} = 0 to V_{DDA}	-	-	±10	nA
I_{PHI_L}	output leakage current PHI	$V_{RF} = V_{DDA}$ $V_{RN} = V_{DDA}$ V_{PHI} = 0 to V_{DDA}	-	-	±10	nA
I_{PHA_L}	output leakage current PHA	$V_{RF} = V_{DDA}$ $V_{RN} = V_{DDA}$ V_{PHA} = 0 to V_{DDA}	-	-	±10	nA

note 1:When a serial input "A" word is programmed, the main charge pumps on PHP and PHI are in the "speed up mode" as long as STROBE = H. When this is not the case, the main charge pumps are in the "normal mode".
note 2:The relative output current variation is defined thus:

$\Delta I_{OUT} / I_{OUT} = 2 \times (I_2 + I_1) / |(I_2 - I_1)|$; with V_1 = 0.4 V, $V_2 = V_{DD}$ - 0.4 V (see fig. 8)

note 3:FRD is the value of the 3 bit fractional accumulator

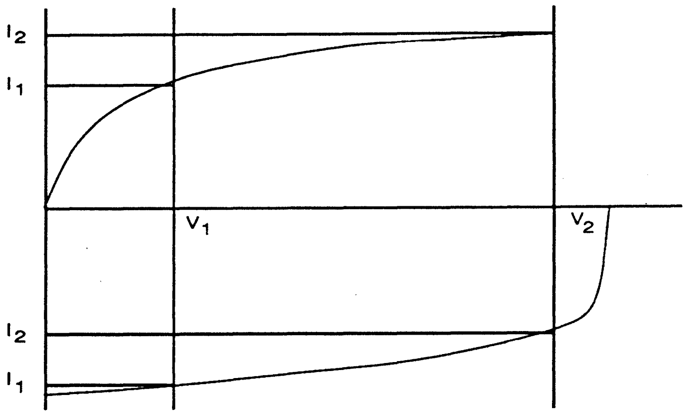


Fig. 8 Output current definition

AC CHARACTERISTICS

symbol	parameter	min	typ	max	unit
Main divider					
f_{INM}	Max. input frequency	20	-	-	MHz
$V_{INM1,2}$	Differential input signal amplitude	600	-	-	mV_{pp}
t_{PHL}	Prop. delay V_{INM1}-V_{INM2} to falling edge FB1, FB2	-	-	25	ns
t_{PLH}	Prop. delay V_{INM1}-V_{INM2} to rising edge FB1, FB2	-	-	25	ns
t_{MSM}	Mark-space ratio	35/65	-	65/35	%
Z_{INM}	Minimum impedance				
	Resistive,	5	-	-	kΩ
	Capacitive	-	-	5	pF
Reference divider					
f_{INR}	Max. input frequency	30	-	-	MHz
V_{INR}	Input signal amplitude	300	-	-	mV_{pp}
t_{MSR}	Mark-space ratio	35/65	-	65/35	%
Z_{IMR}	Min. impedance				
	Resistive	5	-	-	kΩ
	Capacitive	-	-	5	pF

AC CHARACTERISTICS (Con't)

Auxiliary					
f_{INA}	Max. input frequency	100	-	-	MHz
V_{INA}	input signal amplitude	300	-	-	mV_{pp}
t_{MSA}	Mark-space ratio	35/65	-	-	%
Z_{INA}	Min. impedance				
	Resistive	5	-	-	kΩ
	Capacitive	-	-	5	pF
Serial Interface					
f_{clock}	Clock frequency	-	-	10	MHz

DEFINITIONS

Data sheet status

Objective specification:	This data sheet contains target or goal specifications for product development.
Preliminary specification:	This data sheet contains preliminary data; supplementary data may be published later.
Product specification:	This data sheet contains final product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application report for the UMA1014T frequency synthesizer

SCO/AN91004

1. INTRODUCTION

This application note is intended as a guide to designing a phase locked loop based on the Philips UMA1014T frequency synthesizer integrated circuit. The UMA1014T is a low power single chip solution to frequency synthesis in the range 100 MHz to 1100 MHz and is primarily intended for use in analogue cellular radio applications.

The device comprises of the following functional blocks:

- RF dual-modulus prescaler.
- RF programmable divider.
- Reference oscillator.
- Reference programmable divider.
- Digital phase comparator.
- In-lock detection circuitry.
- I²C serial programming interface.

In addition, the device features a power down mode for battery conservation and a XTAL/8 output for use with the Philips cellular radio chipset. The only major external component required is a voltage controlled oscillator (VCO).

This application report presents a design for a frequency synthesizer based on the UMA1014T suitable for the local oscillator for analogue cellular radio applications in the 900 MHz band. A PCB layout is suggested. For detailed device specifications of the UMA1014T refer to the data sheet (Reference 1).

2. FUNCTIONAL DESCRIPTION OF THE UMA1014T

The main functions are illustrated in a Phase Lock Loop (PLL) block diagram (Fig 1). A temperature controlled crystal oscillator (TCXO) provides a reference frequency to the PLL. A phase comparator uses a charge pump to send correction current pulses to a low pass filter. The filter integrates the pulses giving a voltage which controls a VCO. VCO and TCXO o/ps are divided down to a common comparison frequency to control the phase comparator. When the VCO o/p is on frequency the current pulses need only be large enough to cancel leakage currents thus maintaining the required voltage on the VCO.

2.1 Main Divider Chain

The UMA1014T contains a fully programmable main divider chain with an on-chip RF prescaler. The range of the main divider is from 2048 to 262143, thus permitting all useful phase detector comparison frequencies over the full range of input frequencies.

2.2 Reference Divider Chain

Since current analogue systems have only a few different channel spacings, and in any system there is a restricted choice of reference crystal frequencies, the UMA1014T implements a reference divider with limited programmability. A total of 16 different division ratios can be selected which enables all the required phase detector comparison frequencies to be generated. These ratios are 128, 160, 192, 240, 256, 320, 384, 480, 512, 640, 768, 960, 1024, 1280, 1536 and 1920.

In addition, there is one eighth of the crystal frequency available on an output for use with the Philips cellular radio chipset. This chipset uses a 1.2 MHz clock for the analogue and digital baseband circuits which is provided by the frequency synthesizer; the synthesizer thus requires the use of a 9.6 MHz crystal in this application.

2.3 Phase Detector

There are three requirements for the phase detector; firstly it should cover the full 360 degree phase range, secondly it should have good noise performance, and thirdly it should have good comparison frequency suppression. In order to meet these requirements, the use of a high gain digital phase comparator is beneficial. The comparator covers the complete phase range while introducing little noise owing to the high proportion of time that is spent in a high impedance state. Good reference rejection is achieved due to low leakage currents.

2.3.1 Digital Phase Comparator

The Digital Phase Comparator (PCD) has three states, sinking current, sourcing current and a high impedance tristate. The design is based on D type flip-flops and responds to the full 360 degree range of phase inputs. The D type flip-flops control two current sources arranged in a push pull configuration. PCD delivers a constant current while the main and reference dividers are out of phase, either sinking or sourcing (Fig 2). The current IPCD is programmed via the I^2C interface to be either 1 mA or 0.5 mA. The phase comparator gain is hence:

$$PCD\,gain = \frac{IPCD}{2 \times \pi}\ A/rad \qquad (1)$$

The phase comparator circuit incorporates a delay which eliminates a dead band that would otherwise be present in digital phase comparators. Dead bands are due to the finite time the current sources take to switch on. The design of the UMA1014T takes this into account by introducing the delay into the D type reset line. This gives the current sources enough time to respond. Both current sources are switched on for the duration of the delay thus cancelling each other at PCD.

3. INTERFACING TO THE UMA1014T

The UMA1014T provides two way communication to a controller, power down facility, programmable o/p ports, oscillator circuitry and PLL control. The UMA1014T is designed to have the minimum of external components to enable low cost, compact and reliable circuits.

3.1 Programming the UMA1014T

The UMA1014T is programmed via the Philips Standard I^2C bus. To program information into the device registers, it is necessary to transmit first the device address, then the sub-address, and finally the data bytes for the register(s) (Reference 2). To read the status register, it is only necessary to transmit the address before reading back the value of the status register. When writing to the UMA1014T the sub-address allows writing to any single register, or a burst mode where all registers can be written in one I^2C transfer. The formats are thus:

Write to one register:

```
START - address - sub-address - data - STOP
            |            |
            |            |____contains register number to be accessed
            |
            |____R/WN (read/write not) bit set to 0 (write)
```

Write to several registers:

```
START - address - sub-address - data 1 - ... - data n - STOP
            |            |
            |            |____ contains first register number to be
            |                  accessed in the sequence and auto-
            |                  increment enabled
            |
            |____R/WN bit set to 0 (write)
```

Read from status register:

```
START - address - status - STOP
            |
            |____R/WN bit set to 1 (read)
```

The address byte, in addition to containing the R/WN bit as shown above, has one bit that reflects the inverse of the SAA pin logic level. This allows the addressing of up to two synthesizer circuits on the same I²C bus.

The format for the address bus is as follows:

```
1   1   0   0   0   1   SAAN  R/WN
|                        |     |
|                        |     |____0 (write), 1 (read)
|                        |
|                        |__opposite logic level to that of SAA pin
|
|____MSB of device address, transmitted first after START condition
```

The sub-address has the following format: (X means not used)

```
X   X   X  DI  AVI  X   SB1   SB0
           |    |        |     |
           |    |        |_____|____register pointer
           |    |
           |    |____auto-increment - 0 (disable), 1 (enable)
           |
           |____SYA interrupt - 1 (disable), 0 (enable)
```

The status register relates to the alarm of the ciruit as follows:

0	0	0	00L	0	L00L	LPD	DI

Each bit is active high.

00L	Momentarily out of lock,	L00L	Latched out of lock (†),
LPD	Latched power dip (†),	DI	Interupt disabled on SYA,

(†) Reading status register clears these if the error condition has been removed.

Data is formatted as a series of registers as follows:

Reg/ister	SB1 SB0	Bit Allocation								Preset
		7	6	5	4	3	2	1	0	
A	00	PD	0	IPCD	X	RD3	RD2	RD1	RD0	00001110
B	01	1	0	1	PHI	VCOB	VCOA	MD17	MD16	10101001
C	10	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	00111000
D	11	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	10000000

Register map bit polarities:

	0	1
PD	Normal operation	Power down
IPCD	Current in PCD = 0.5 mA	PCD = 1 mA
RD3..0	Reference divider ratio MSB = RD3	
PHI	Passive loop (no inversion)	Active loop (Phase inversion)
VCOA	Set pin 7 low	Set pin 7 high
VCOB	Set pin 13 low	Set pin 13 high
MD17..0	Main divider ratio MSB = MD17	

RD3..RD0 reference divider programming:

RD3	RD2	RD1	RD0	Reference Division Ratio
0	0	0	0	128
0	0	0	1	160
0	0	1	0	192
0	0	1	1	240
0	1	0	0	256
0	1	0	1	320
0	1	1	0	384
0	1	1	1	480
1	0	0	0	512
1	0	0	1	640
1	0	1	0	768
1	0	1	1	960
1	1	0	0	1024
1	1	0	1	1280
1	1	1	0	1536
1	1	1	1	1920

MD17..MD0 main divider value 2048 to 262143 (hex $800 to $3ffff).

3.2 Hardware Control Inputs and Outputs

There are a number of status and control signals generated by the UMA1014T and also a hardware control input.

3.2.1 HPD Input

This input is used to disable the divider chains in order to save power when the synthesizer is not required to be operational. The power down state can be activated either by taking this pin low or by setting the power down bit in the I^2C register to a '1'. The input has an internal pull-up resistor so that normal operation will be obtained if the pin is left open circuit.

The power down state does not have any effect on the I^2C circuitry, so that the device may still be addressed, and new information programmed into the registers even in the power down mode.

3.2.2 FX8 Output

This is an open collector output of one eighth of the crystal or TCXO input frequency. It is required for use with the Philips cellular radio chipset for AMPS and TACS systems; in this application the synthesizer should be used with a 9.6 MHz TCXO. The recommended pull-up load is 27 k Ohm.

3.2.3 SYA (Synthesizer Alarm) Output

This is an open collector output which is normally held high by an external 27 k Ohm load. Under error conditions, the synthesizer latches SYA low. The error conditions that set SYA low are a power dip or an out-of-lock condition. A power dip occurs when VCC supply falls below about 3.5 V. SYA is reset again by reading the status register, which contains the relevant alarm information. The SYA output can also be enabled and disabled via I^2C as required.

The typical use of SYA would be to interrupt a microcontroller to warn of the error condition. As the output is open collector, it is possible to connect more than one device together directly; in this case the microcontroller would poll the relevant devices to locate the source of the error condition.

3.2.4 VCO0 and VCO1 Outputs

These are open collector outputs and are intended for enabling the power supply to VCOs or buffer stages so that these parts of the set can be powered down when not required to be operational. The outputs are controlled via I^2C. In addition, the VCO0 output is forced low during an out-of-lock condition; this output could therefore be used to disable the transmitter when this condition occurs to prevent causing interference. In this case, there may well be other parts of the circuitry also controlling the transmitter in the same way; as the VCO0 and VCO1 lines are open collector, they may be directly connected to other such controlling signals.

The VCO1 output is not affected by the hardware power down input or power down via I^2C. The VCO0 output will of course be forced low due to the out-of-lock condition resulting from a power down.

3.3 Crystal Oscillator

For analogue cellular radio applications, the UMA1014T will almost certainly be used with an external oscillator in order to provide the stability necessary to ensure operation within the specification. However, in case some other applications do not require such accuracy, provision has been made to form a crystal oscillator using the OSCIN and OSCOUT inputs (pins 1 and 2 respectively). The oscillator circuit should be of the Colpitts type and requires the addition of four capacitors to function. This is shown in Fig 3, with capacitor values suitable for operation at 9.6 MHz.

The internal biasing provides possible operation over the range 3 MHz to 16 MHz with the addition of a suitable crystal. It may be necessary to adjust the values of the capacitors slightly to guarantee oscillation under all conditions for frequencies significantly different to 9.6 MHz.

The crystal used in this circuit is parallel resonant, fundamental mode, with a load capacitance of 30 pF which is approximately the series combination of the three fixed capacitors in parallel with the trimmer capacitor.

3.4 External Oscillator

When using an external oscillator such as a TCXO module, the output from the oscillator should be connected directly to the OSCin pin (pin 1). The OSCout pin (pin 2) should either be left open circuit, or could be used as a buffered version of the signal applied to OSCin.

3.5 RF Connection to Main Divider

The output from the VCO needs to be split between the synthesizer RF o/p and the UMA1014T main divider input. A matched splitter is used as shown in Fig 4. Ideally, the splitter should provide maximum isolation to the VCO to prevent pulling or modulation due to changes in the load impedance at the RF o/p and main divider input. The amount of isolation is limited by the required RF output power and the main divider input sensitivity. Emphasis is placed on the importance of providing sufficient isolation between the VCO and the main divider to keep spurious modulations at a minimum level.

3.6 Loop Filter Design

The correct design of the loop filter is of considerable importance to the optimum performance of the synthesizer. The filter should be designed so as to achieve the required compromise between noise performance and switching time. The actual circuit will therefore depend on the particular application. A procedure has been established to ensure quick and simple loop filter design. The method, based on first order approximations, provides a working solution without a need for computer simulation and modelling.

Design Procedure

For typical applications a passive loop is used thus removing the need for an operational amplifier. The following design is based on a second order low pass filter (Reference 3). Then, for applications requiring further reference breakthrough rejection, a third order is incorporated. The third order loop filter is used for circuits and measurements in this report.

Loop parameters are first chosen, these are:

- Radio frequency — RF
- Comparison frequency — CF
- Switching time — St
- Minimum modulating frequency — MF
- VCO gain rad/Volt — Ko
- Phase comparator gain Amps/rad — Kd
- Phase margin — ϕ

Determine the loop bandwidth Fn from

$$\frac{3}{switching\ time} = Fn \qquad (2)$$

Determine main divider ratio N from N = RF / CF (3)

Determine angular velocity wn rads / s from wn = 2 x π x Fn

The loop filter circuit (Fig 5) has three time constants, these are:

- T1 = C3 x R2 (4)
- T2 = R2 x C1 x C3 / (C3 + C4) (5)
- T3 = C2 x R1 (6)

The second order loop is designed by omitting R1 and C2 (T3) and uses the equations below:

$$T2 = \frac{\frac{1}{COS\ \phi} - Tan\ \phi}{wn} \qquad (7)$$

$$T1 = 1 / (wn^2\ x\ T2) \qquad (8)$$

$$C3 + C1 = K \sqrt{\frac{1 + (wn\ x\ T1)^2}{1 + (wn\ x\ T2)^2}} \qquad (9)$$

$$where\,K = \frac{Kd\,x\,Ko}{N\,x\,wn^2} \tag{10}$$

$$C1 = \frac{T2\,x\,(C3 + C1)}{T1} \tag{11}$$

$$C3 = (C3 + C1) - C1 \tag{12}$$

$$R2 = T1\,/\,C3 \tag{13}$$

Measuring the reference spurs and comparing with a particular specification establishes if a third order is necessary.

If a further 'A' dB of breakthrough suppression is needed to meet specification, then T3 is included to make a third order filter. Note 'A' should not be so large that T3 x 10 > T1. A good starting value for 'A' is 20 dB.

$$T3 = \sqrt{\left(\frac{10^{(A/20)} - 1}{(2\,x\,\pi\,x\,Fc)^2}\right)} \tag{14}$$

T2 determines the loop stability and remains the same as for 2nd order loop.

A calculated value of closed loop bandwidth wnc is used. This is usually slightly less than wn so the switching time will be slightly longer than originally specified.

$$wnc = \frac{(T2 + T3)}{T2^2}\,x\,tan\,\phi\,x\left(\sqrt{1 + \frac{4\,x\,T2^2}{(2\,x\,tan\,\phi\,x\,(T2 + T3))^2}} - 1\right) \tag{15}$$

$$T1 = \frac{1}{wnc^2\,x\,(T2 + T3)} \tag{16}$$

$$C3 + C1 = K\sqrt{\frac{1 + (wnc\,x\,T1)^2}{(1 - wnc^2\,x\,T2\,x\,T3)^2 + \frac{T3 + T2}{T1}}} \tag{17}$$

$$where\ K = \frac{Ko\,x\,Kd}{N\,x\,wnc^2} \quad (18)$$

$$C1 = \frac{(C3 + C1)\,x\,T2}{T1} \quad (19)$$

$$C3 = (C3 + C1) - C1 \quad (20)$$

$$C2 = C1\ /16 \quad (21)$$

$$R2 = T1\,/\,C3 \quad (22)$$

$$R1 = T3\,/\,C2 \quad (23)$$

For a successful filter it is important that C3 >> C1 and C1 >> C2.

3.6.1 Worked Example

As an example the design of the third order loop filter for the UMA1014T under the following conditions is shown below. This design on the PCAL1143-1 board suitable for ETACS transmit application. Switching time is set sightly shorter than expected to compensate for the reduction in the final loop bandwidth Fnc.

VCO frequency		=	888 MHz
VCO gain	Ko	=	13 MHz / V
Channel spacing		=	25 kHz (with half channel offset)
Reference oscillator		=	9.6 MHz
Switching time		=	12 ms (for a requirement < 14 ms)
Min mod frequency		=	300 Hz
Phase margin(degrees)		=	45
Additional reference Rejection	A	=	20 dB

In this example the phase comparator gain Kd chosen is 1 mA / cycle as opposed to 0.5 mA / cycle. In open environments a loop based on this is less susceptible to interference as capacitor values are higher. A comparison frequency of 12.5 kHz is chosen to allow for the half channel offset specified in ETACS.

The first order loop bandwidth Fn:

$$\frac{3}{12\,x\,10^{3}} = 250\,Hz \quad wn = 2\,x\,\pi\,x\,Fn = 1570\,rads/s \qquad Use\ (2)$$

The main divider ratio N:

$$\frac{888\,x\,10^{6}}{12.5\,x\,10^{3}} = 71040 \qquad Use\ (3)$$

$$T2 = \frac{\frac{1}{cos\ 45} - tan\ 45}{1570} = 2.64\,x\,10^{-4} \qquad Use\ (7)$$

$$T3 = \sqrt{\left(\frac{10^{20/20} - 1}{(2\,x\,\pi\,x\,12500)^{2}}\right)} = 3.82\,x\,10^{-5} \qquad Use\ (14)$$

$$wnc = \frac{(2.64\,x\,10^{-4} + 3.82\,x\,10^{-5})\,x\,tan\ 45}{(2.64\,x\,10^{-4})^{2}}\ x$$

$$\left(\sqrt{1 + \frac{4\,x\,(2.64\,x\,10^{-4})^{2}}{(2\,x\,tan\ 45\ x\ (2.64\,x\,10^{-4} + 3.82\,x\,10^{-5}))^{2}}} - 1\right) = 1421 \qquad Use\ (15)$$

$$T1\ \frac{1}{1421^{2}\,x\,(2.64\,x\,10^{-4} + 3.82\,x\,10^{-5})} = 1.64\,x\,10^{-3} \qquad (Use\ (16)$$

$$K = \frac{13\,x\,10^{6}\,x\,10^{-3}}{71040\,x\,1421^{2}} = 9.04\,x\,10^{-8} \qquad Use\ (18)$$

$$C1 + C3 = K\sqrt{\frac{1 + (1421\ x\ 1.64\,x\,10^{-3})^{2}}{(1 - 1421^{2}\,x\,2.64\,x\,10^{-4}\,x\ 3.82^{-5})^{2} + \dfrac{3.82\ x\ 10^{-5} + 2.64^{-4}}{1.64\ x\ 10^{-3}}}}$$

$$= 2.14\ x\ 10^{-7} \qquad Use\ (17)$$

$$C1 = \frac{2.14\,x\,10^{-7}\,x\,2.64\,x\,10^{-4}}{1.64\,x\,10^{-3}} = 3.45\,x\,10^{-8} \qquad Use\ (19)$$

$$C3 = 2.14\,x\,10^{-7} - 3.45\,x\,10^{-8} = 1.8\,x\,10^{-7} \qquad Use\ (20)$$

$$C2 = 3.45\,x\,10^{-8}/16 = 2.15\,x\,10^{-9} \qquad Use\ (21)$$

$$R2 = 1.64\,x\,10^{-3}/1.8\,x\,10^{-7} = 9111 \qquad Use\ (22)$$

$$R1 = 3.82\,x\,10^{-5}\,/\,2.15\,x\,10^{-9} = 17767 \qquad Use\ (23)$$

Check C2 << C1 << C3.

Values chosen for filter components are:

C1 = 33 nF	R1 = 18 k Ohms
C2 = 2.2 nF	R2 = 10 k Ohms
C3 = 180 nF	

3.7 PCB Layout Considerations

The circuit of the UMA1014T demonstration board (PCAL1143-1) is shown in Fig 6, with the layout shown in Fig 7. This PCB has a solid ground plane on one side (apart from isolated pads for non-grounded connections to leaded components). In addition, there are areas of ground plane on the surface mount side of the board to ensure satisfactory grounding of important components. There are a good number of plated-through holes connecting the two layers of ground plane. Normal RF design practices should of course be taken into account when laying out the circuit.

There are a number of particular points that should be borne in mind when considering the circuit and layout.

- The non-surface mount side of the board (if a 2 sided board is used) should be virtually solid ground plane to give good RF performance.

- The 5 V digital supply (VCC) should be well decoupled as close to the pin as possible, preferably with a large value capacitor (eg: 47 uF) and in series with a small value resistor (eg: 12 Ohms) from the 5 V line.

- The 5 V charge pump supply (VCP) should be decoupled separately from VCC but in a similar manner. Routing the 5 V supply under the IC is to be avoided.

- Incorporating a ground plane on the surface mount side of the PCB underneath the synthesizer helps isolate digital noise from the charge pump parts. This ground plane should be well connected with vias to the full ground plane.

4. TYPICAL PERFORMANCE

This section describes the typical performance obtainable with the UMA1014T with the circuit shown in Fig 6 and parameters listed in 3.6.1. The relevant performance criteria for a synthesizer are usually:

Close-in phase noise (ie: noise within the loop bandwidth).

Noise floor at an offset from the carrier.

Comparison breakthrough components.

Switching time.

It should be noted of course that these criteria can be traded off against each other to some extent to tailor the overall performance, and that the performance described here is only one compromise between the various criteria. In general, the choice of a low loop bandwidth will improve the comparison frequency breakthrough and will filter out more of the close-in phase noise, but will result in a longer switching time. The use of a higher order filter can improve comparison frequency breakthrough with little effect on the noise or switching time. The noise floor at offsets significantly higher than the loop bandwidth are determined completely by the VCO itself.

Plots of the close-in spectrum (span of 2 kHz) and also a span of 50 kHz are shown in Figs 8 and 9 respectively for a carrier frequency of 888 MHz and a comparison frequency of 12.5 kHz. From Fig 8 we can see from the noise plateau that the loop bandwidth is around 270 Hz, and Fig 9 shows the spectrum analyser noise floor at offsets greater than about 15 kHz from the carrier with the first and second comparison frequency breakthrough component being visible at 12.5 kHz and 25 kHz from the carrier respectively.

Figure 10 shows switching waveforms for a frequency jump of 10 MHz. The top trace (labelled CH1) is the I^2C transfer to the UMA1014T; the second (CH2) is the VCO control line. The third trace (CH3) is the VCOA output showing the out-of-lock condition. The fourth trace (CH4) is the RF output of the VCO mixed down to 0 Hz with a signal generator at the destination frequency. The VCO output is coupled to the mixer via an amplifier with 17 dB gain followed by a 10 dB attenuator. This is to provide isolation to the VCO from the mixer.

The mixer output trace shows that the switching time is 13 m seconds, which is a little longer than the VCO control line trace appears to show. This is because observation of the VCO control line is not accurate due to the very high VCO gain (13 MHz / V).

From Fig 10, we can see that the VCO control line has a single overshoot during switching; this shows that the loop is properly damped, so the phase margin is correct.

To summarise the performance of the circuit in Fig 6:

loop bandwidth	270 Hz
close-in noise	- 55 dBc / Hz at 200 Hz from carrier
VCO noise floor	- 113 dBc / Hz at 25 kHz from carrier
residual fm	< 18 Hz rms, CCITT weighted
comparison frequency breakthrough	- 65 dBc at 12.5 kHz - 82 dBc at 25 kHz
typical switching time	< 13 m seconds for 10 MHz jump to within 1 kHz of the destination frequency

5. CONCLUSIONS

Information regarding the use of the UMA1014T in a frequency synthesizer application has been presented. A methodology for determining the loop filter components has been described since the switching and noise performance of the complete circuit depends on a good filter design. The layout of the PCAL1143-1 demonstration board has been shown as an example PCB layout.

6. REFERENCES

1. UMA1014T, Initial Specification Data Sheet, September 1990.

2. N M W Oatley;
   Application Information for the UMA1010T/UMA1012T, Philips Components Application Report MC090001.

3. Ulriche, L Rhode;
   Digital PLL Frequency Synthesizers Theory and Design.
   28/3/91.

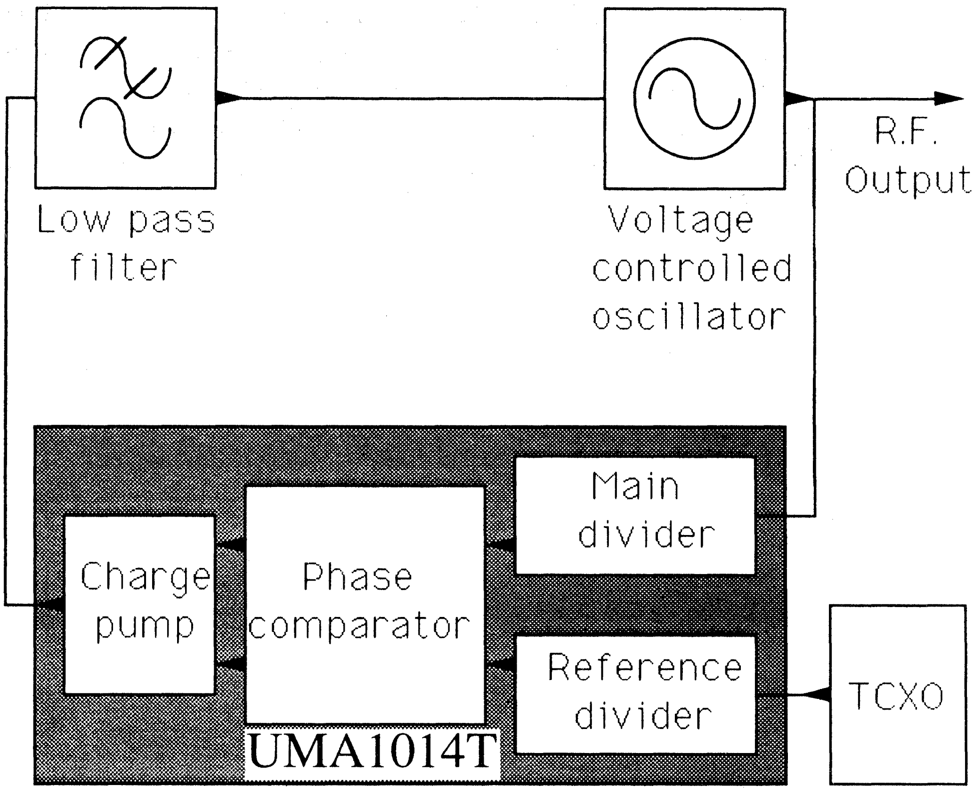


Fig 1 PLL Circuit Block Diagram

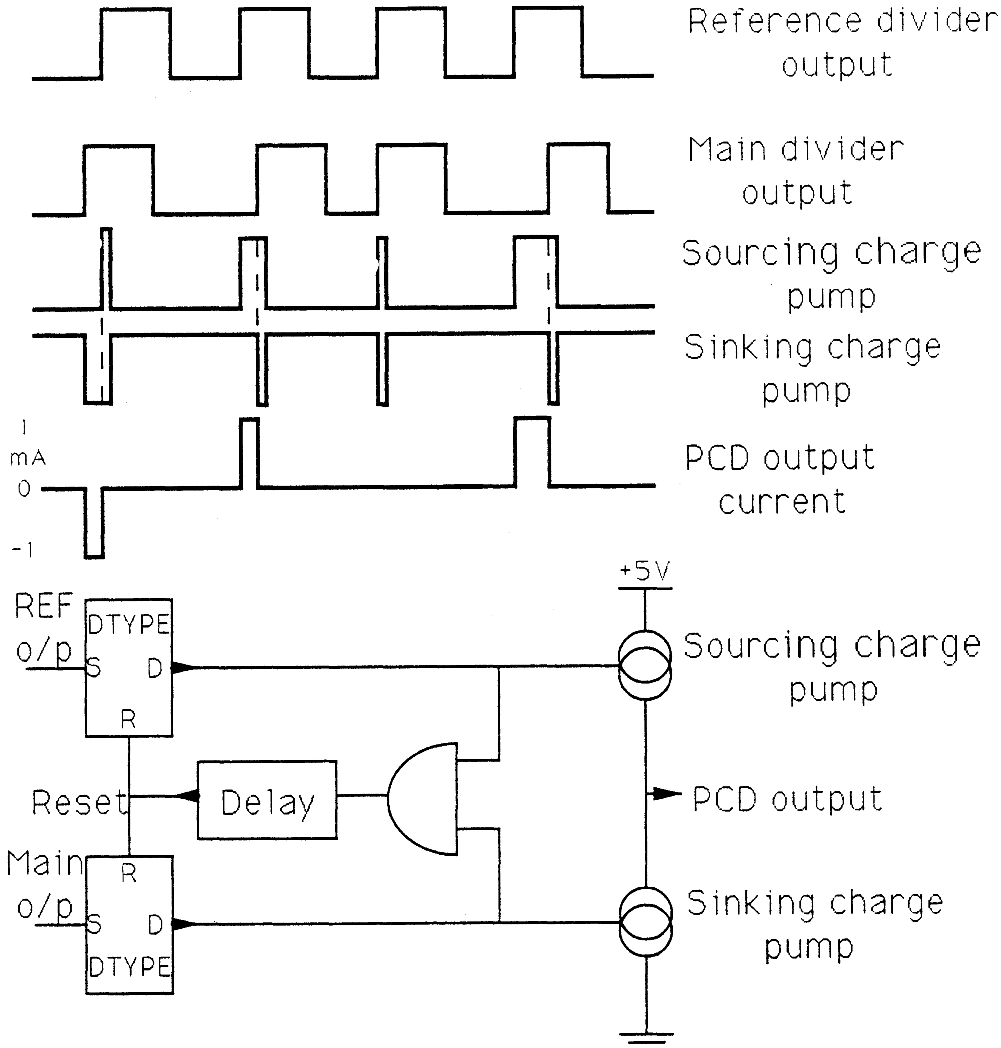


Fig 2 Digital Phase Comparator Operation

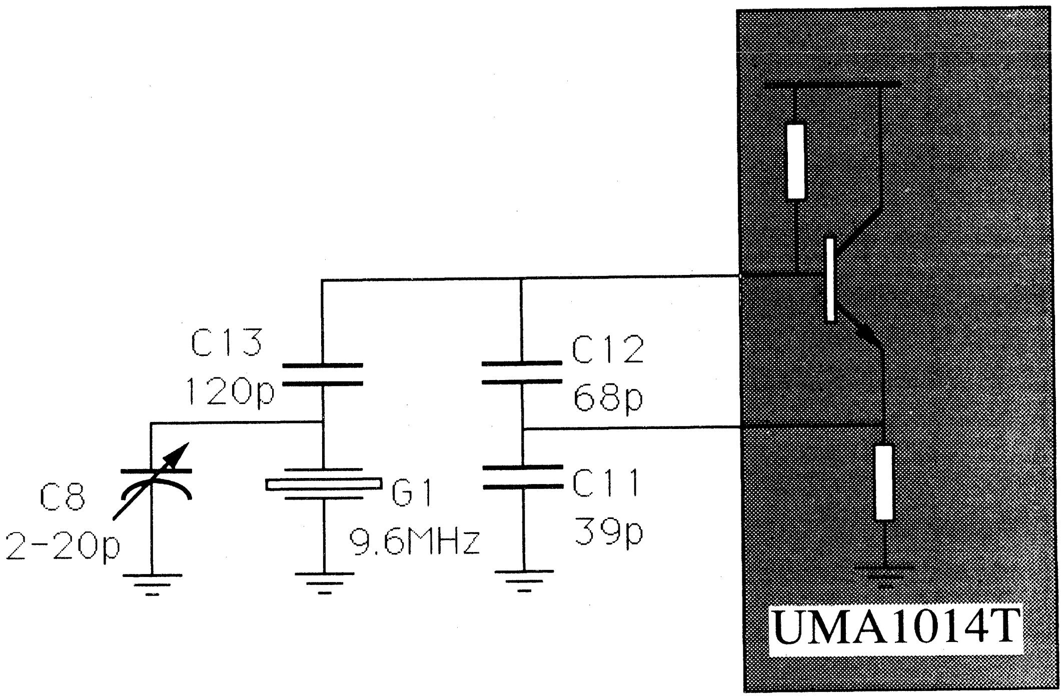


Fig 3 Crystal Oscillator Circuit Diagram

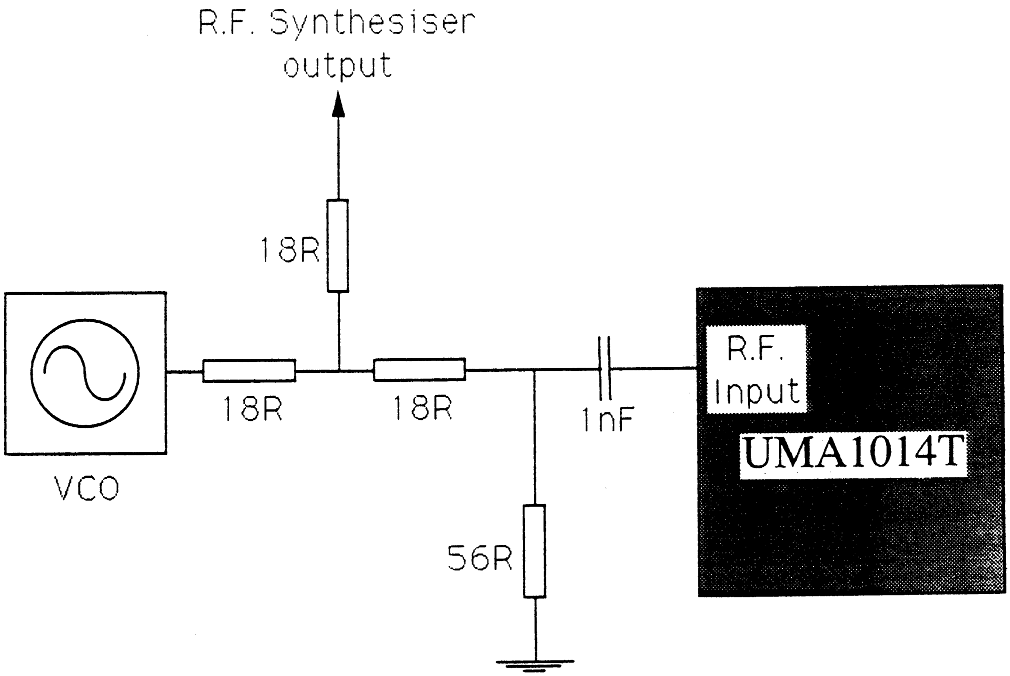


Fig 4 RF Power Splitter Circuit Diagram

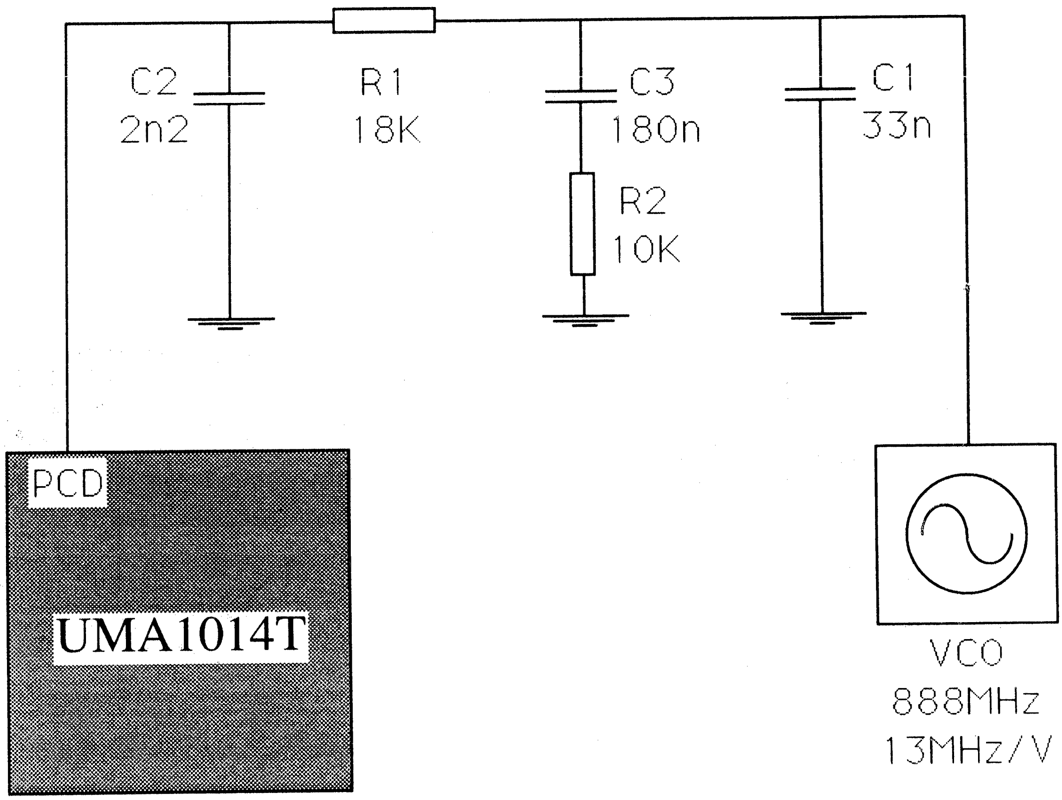


Fig 5 Loop Filter Circuit Diagram

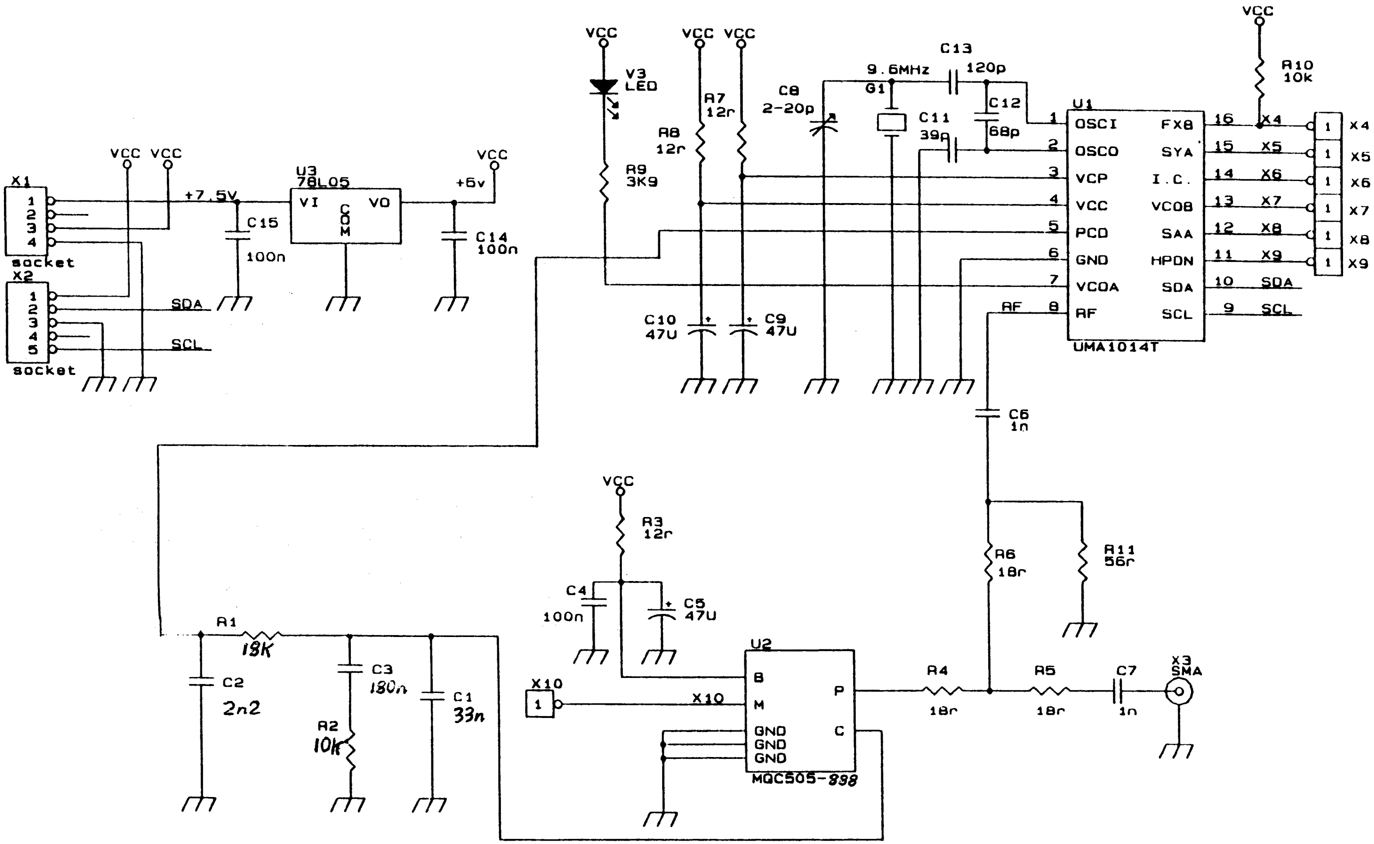


Fig 6 Frequency Synthesizer Circuit using the UMA1014T

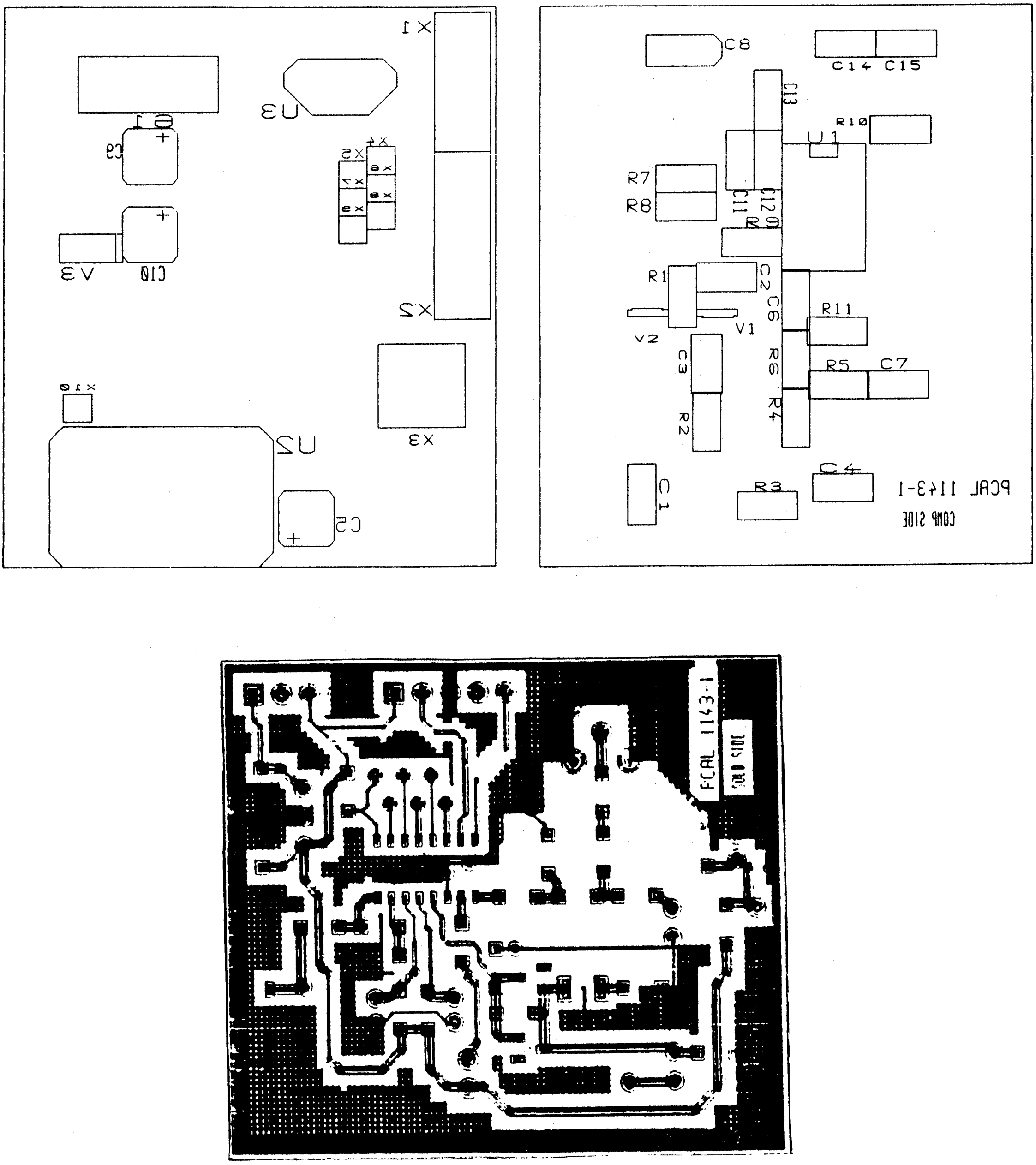


Fig 7 Board Layout for UMA1014T Frequency Synthesizer

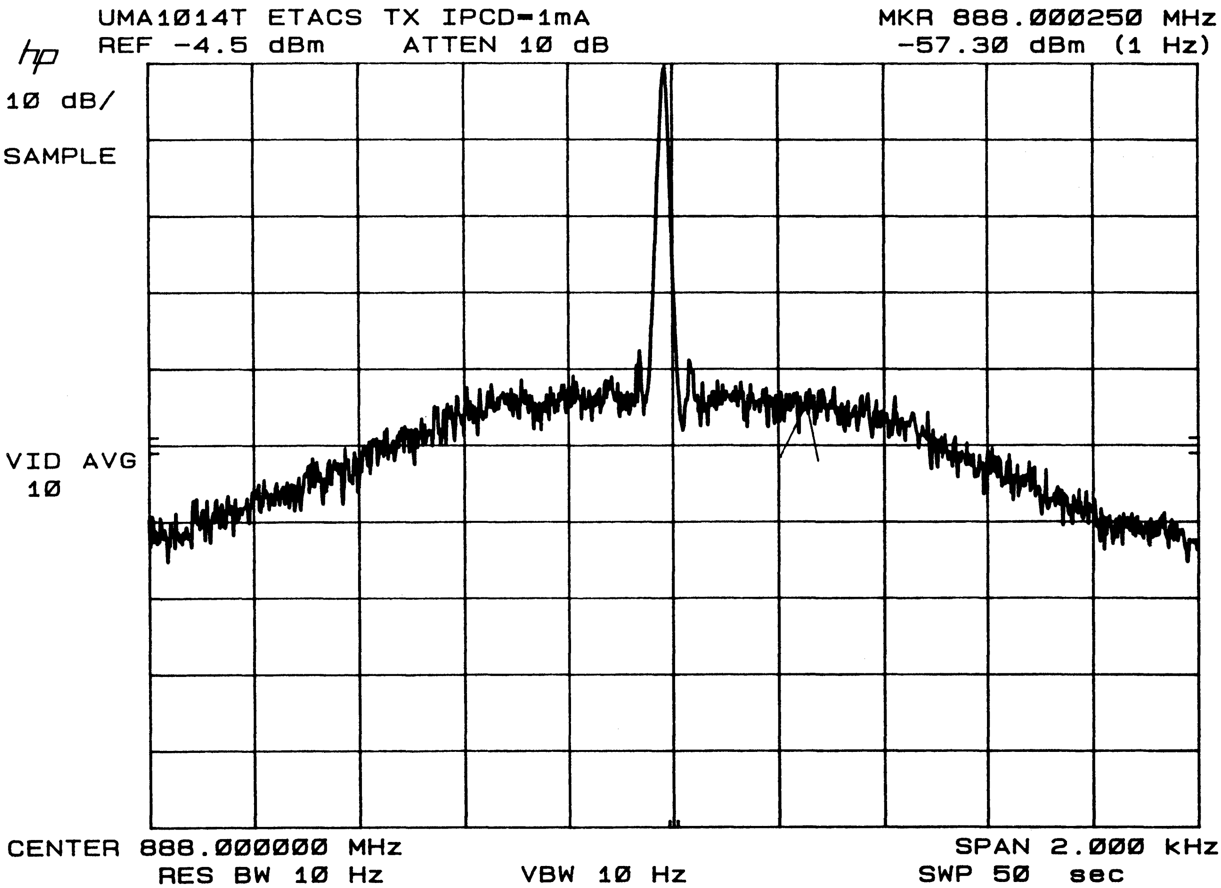


Fig 8 Typical Carrier Spectrum - 2 kHz Span

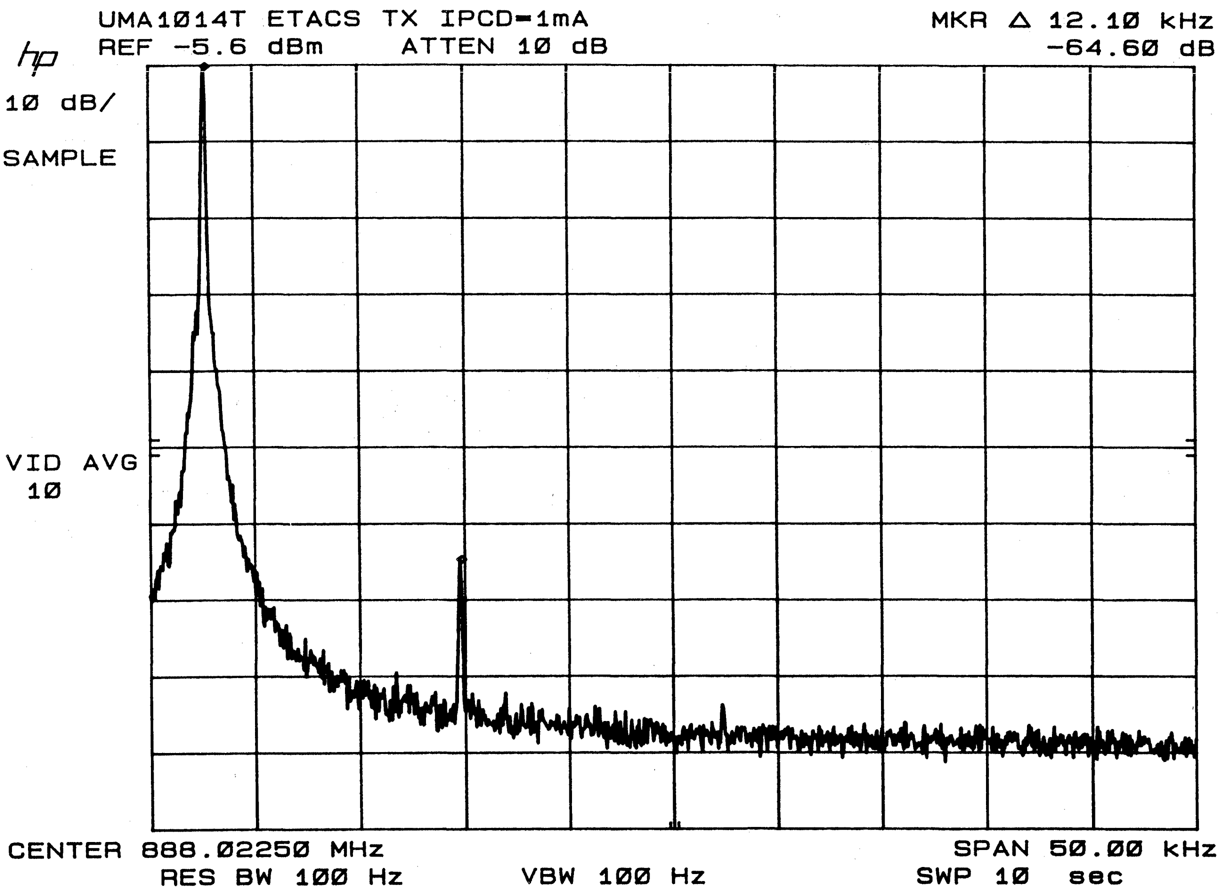


Fig 9 Typical Carrier Spectrum - 50 kHz Span

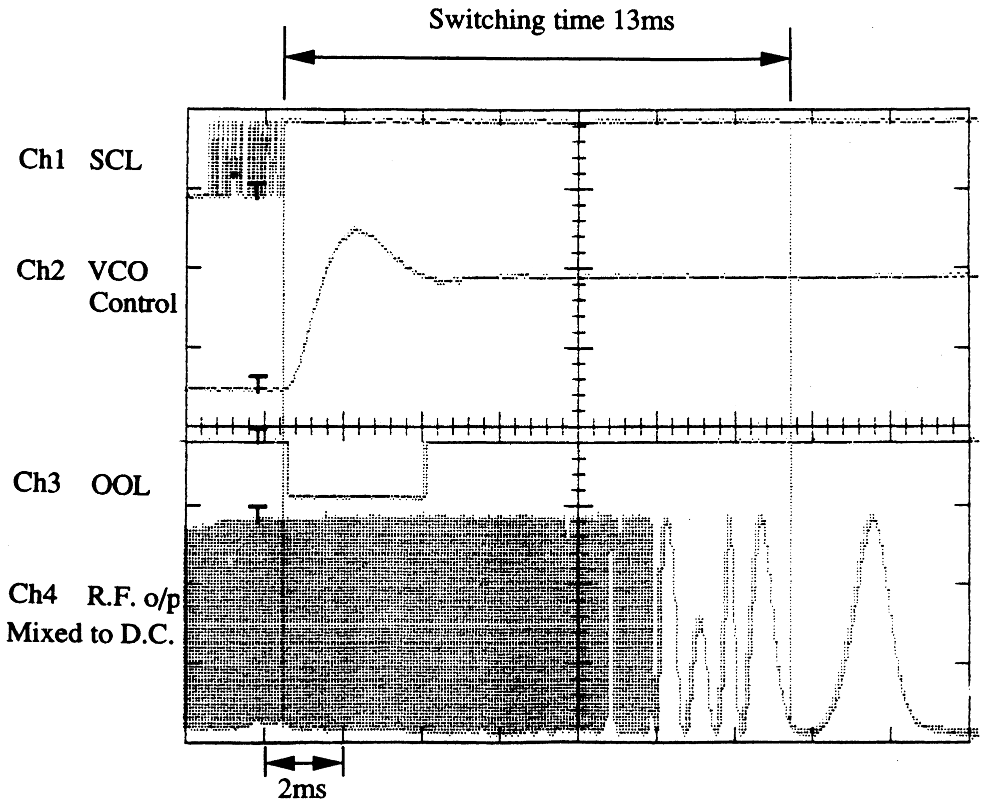


Fig 10 Typical Switching Waveforms

Low power frequency synthesizer for radio communication — UMF1009T

GENERAL DESCRIPTION

The UMF1009T is a low-power, high performance dual modulus frequency synthesizer designed in CMOS technology. The device is designed for use in channelled VHF/UHF applications, especially portable and mobile radios. The synthesizer is programmed via the standard two-line serial I^2C-bus.

FEATURES

- On-chip sample-and-hold capacitor
- Low power consumption
- High gain phase comparator with low levels of noise and low level spurious outputs
- Digital phase comparator for fast locking
- On-chip crystal oscillator from 2.4 to 16.8 MHz; circuit can be used with a crystal or a tuned-circuit TCXO
- A large reference frequency range at the phase detector (binary 15-bit programmable reference counter)
- In-lock detector open-drain output
- 1.2 MHz output for easy interface to the other cellular radio chip set devices
- Single supply voltage (2.7 to 5.5 V).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMF1009T	16	SO16	plastic	SOT109A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage range						
V_{DDD}	supply voltage digital		2.7	-	5.5	V
V_{DDA}	supply voltage analog		2.7	-	5.5	V
Operating current						
I_{DDD}	digital	V_{DD} = 5 V	-	-	1.5	mA
		V_{DD} = 3 V	-	-	0.8	mA
I_{DDA}	analog	V_{DD} = 5 V	-	-	1.0	mA
		V_{DD} = 3 V	-	-	0.6	mA
Frequency range						
f_i	input frequency	V_{DD} = 5 V	0	-	18.0	MHz
		V_{DD} = 3 V	0	-	8.0	MHz
f_{OSC}	crystal frequency range	V_{DD} = 5 V	2.4	-	16.8	MHz
		V_{DD} = 3 V	2.4	-	8.0	MHz
Temperature						
T_{amb}	operating ambient temperature range		-40	-	+85	°C

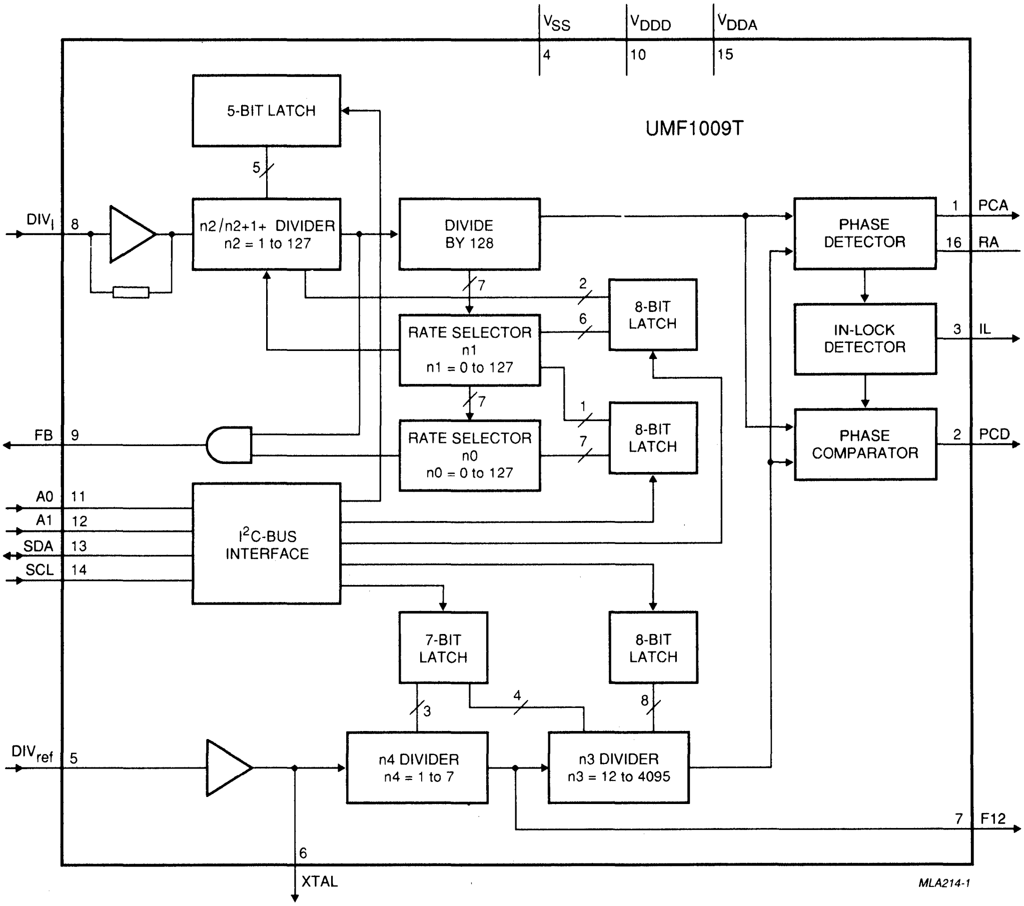


Fig.1 Block diagram.

Low power frequency synthesizer for radio communication UMF1009T

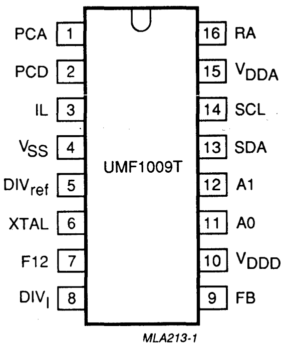


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
PCA	1	analog phase detector output
PCD	2	digital phase detector output
IL	3	in-lock detector output (HIGH when in lock)
V_{SS}	4	ground
DIV_{ref}	5	reference divider input
XTAL	6	output to external crystal
F12	7	1.2 MHz output
DIV_I	8	main divider input from prescaler
FB	9	feedback output for prescaler modulus control
V_{DDD}	10	digital supply; 2.7 to 5.5 V
A0	11	address input 0
A1	12	address input 1
SDA	13	serial data input/output
SCL	14	serial clock input
V_{DDA}	15	analog supply; 2.7 to 5.5 V
RA	16	PCA gain setting resistor

FUNCTIONAL DESCRIPTION

Figure 1 shows the functional block diagram of the UMF1009T.
The main divider, reference divider, phase detectors and the I[2]C-bus interface are described in the subsequent sections.

Main divider

The main divider is a rate-feedback binary type comprising a fixed 7-bit binary divider and two rate selectors n1 and n0. One rate selector controls a 7-bit fully programmable dual modulus divider (n2/n2 + 1), and the other controls an external dual modulus prescaler (A/A + 1).
The total division ratio is given by:

$$N = (128.n2 + n1)\bullet A + n0$$

Where:

$0 \le n0 \le 127$, $0 \le n1 \le 127$ and
$1 \le n2 \le 127$

Thus if the division ratio is expressed as a binary number and A is chosen to be 128, then the n0 rate selector will contain the least significant bits, the n1 selector the next 7 bits and the n2 divider the most significant 7 bits. If A is chosen to be a lower power of 2, then the number of bits of the n0 divider that require programming can be reduced. For example, if A = 32, then only 5 bits of n0 need to be programmed and the most significant 2 bits can remain at zero while still retaining full programmability. If the most significant bits of n0 are used in this situation, then several combinations of values for the n0, n1 and n2 counters will give the same division ratio.

The output from the programmable divider is fed to the phase detectors.

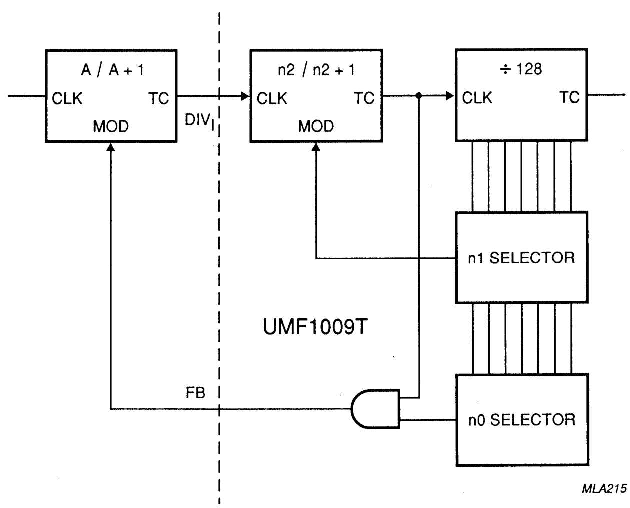


Fig.3 Main divider structure.

Reference divider

The reference oscillator chain comprises a crystal oscillator and dividers to produce the required frequency to drive the phase detectors. The oscillator stage is a simple inverter connected between pin 6 (XTAL) and pin 5 (DIV_{ref}). Satisfactory operation is achieved using a crystal up to 16.8 MHz (V_{DD} = 4.5 V), (up to 8 MHz V_{DD} = 2.7 V). Alternatively, the DIV_{ref} input may be used as a buffer amplifier for an external reference oscillator.

The reference divider contains two sections; the first divider section is programmed to divide by a suitable ratio to give the correct 1.2 MHz output frequency. The second divider section will now operate at 2.4 MHz and is fully programmable. Thus the input frequency at DIV_{ref} can be any of the frequencies given in Table 1.

If the 1.2 MHz output is not required, then the n4 divider can be programmed to any suitable value. Setting n4 = 1 will give access to the fully programmable n3 reference divider without any fixed division. The n3 divider is fully programmable over the range 12 to 4095 to allow complete flexibility in the choice of input frequency to the DIV_{ref} pin for the required reference frequency.

The total reference division is given by: N = n3 x n4

Where:

$12 \le n3 \le 4095$ (FFF hex)
$1 \le n4 \le 7$

Phase detectors

There are two phase detectors which work in close co-operation to provide both a good noise performance and fast frequency locking over a large range. Phase detector 1 (PCA) is the main analog detector. It is designed to have a high gain, typically

$$\frac{5 \times 10^{12} \times (V_{DDD} - 0.7)}{R_A \times f_{DIV(ref)}} \text{ V/Cycle}$$

thus enabling low noise operation to be achieved. **Phase comparator 2 (PCD) is a digital phase comparator with a linear 2π radians phase range corresponding to a gain of $V_{DDD}/2$ V/cycle.**

In order to avoid degrading the noise performance of PCA, once a small phase error has been achieved, an internal switch is used to disconnect PCD.

PCA phase detector

The analog phase detector consists of a linear ramp generator and a sample-and-hold circuit. At the beginning of the reference cycle an internal capacitor is charged from a constant current source to give the linear ramp. The output voltage from the capacitor is buffered by a voltage follower. When both the main and reference divider outputs are in phase, the ramp is terminated. After a short delay, to allow the voltage follower to settle, the follower output is sampled and held by a second internal capacitor. This is buffered and routed to the PCA output pin. After the sample has been acquired, the first capacitor is discharged by a constant current sink to provide a controlled discharge, thus minimizing the disturbance to the sample-and-hold circuit.

If the linear ramp approaches the value of the analog supply rail and

Table 1 DIV_{ref} input frequencies

n4	DIV_{ref} input for 1.2 MHz output	n3 for reference frequency	
		12.5 kHz	15 kHz
1	2.4 MHz	192	160
2	4.8 MHz	192	160
3	7.2 MHz	192	160
4	9.6 MHz	192	160
5	12.0 MHz	192	160
6	14.4 MHz	192	160
7	16.8 MHz	192	160

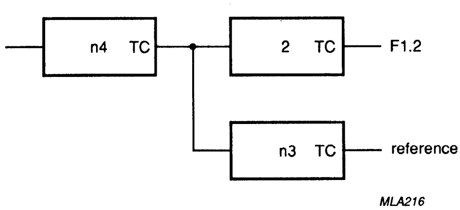


Fig.4 Reference divider structure.

the two divider outputs are not in phase, then the digital phase comparator PCD will be enabled and an out-of-lock error will be indicated as a LOW state on the open drain output IL (pin 3).

To allow for more flexibility in the design of the loop dynamics, the gain of PCA is controlled by a variable resistor connected between RA and V_{SS}. This resistor controls a current source via a current mirror; a typical value for the resistor is 470 kΩ.

PCD phase comparator

The output of the PCD is a series of positive (V_{DD}) or negative (V_{SS}) voltage pulses with variable width which is dependent on the phase relationship of the main and reference divider outputs. During the time the two outputs are in phase, the output from PCD is in a high impedance state. If PCA is in its operating range then PCD is disabled. The enable signal for PCD is inverted and routed to the IL pin so that when PCD is enabled, pin IL is pulled LOW.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	supply voltage (analog)		–0.5	6.5	V
V_{DDD}	supply voltage (digital)		–0.5	6.5	V
V_I	voltage on any input		–0.5	V_{DDD}+0.5	V
V_{DDD} - V_{DDA}	relative supply voltage		-	0.5	V
I_I	DC current into any input or output		–10	+10	mA
P_{tot}	total power dissipation per package	T_{amb} = 0 to +85 °C	-	400	mW
P_D	power dissipation per output		-	100	mW
T_{stg}	storage temperature range		–65	+150	°C
T_{amb}	operating ambient temperature range		–40	+85	°C

DC CHARACTERISTICS

Tamb = -40 to +85 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage						
V_{DDA}	analog supply		2.7	-	5.5	V
V_{DDD}	digital supply		2.7	-	5.5	V
Supply current (note 1)						
I_{DDA}	analog supply	V_{DD} = 5 V	-	-	1	mA
		V_{DD} = 3 V	-	-	0.6	mA
I_{DDD}	digital supply	V_{DD} = 5 V	-	-	1.5	mA
		V_{DD} = 3 V	-	-	0.8	mA
Logic						
V_{IL}	input voltage LOW		–0.5	-	0.3 V_{DDD}	V
V_{IH}	input voltage HIGH		0.7 V_{DDD}	-	V_{DDD}+0.5	V
V_{OL}	CMOS output voltage LOW	I_O < 1 µA	-	-	50	mV
V_{OH}	CMOS output voltage HIGH	I_O < 1 µA	V_{DDD}–0.05	-	-	V
V_{OL}	output voltage LOW (IL, PCD and F12)	V_{DD} = 4.5 V; I_{OL} = 2 mA	-	-	0.4	V
		V_{DD} = 2.7 V; I_{OL} = 1 mA	-	-	0.4	V
V_{OL}	SDA output voltage LOW	V_{DD} = 4.5 V; I_{OL} = 3 mA	-	-	0.4	V
		V_{DD} = 2.7 V; I_{OL} = 1.5 mA	-	-	0.4	V
V_{OH}	output voltage HIGH (PCD, FB and F12)	V_{DD} = 4.5 V; -I_{OL} = 2 mA	V_{DDD}–0.5	-	-	V
		V_{DD} = 2.7 V; -I_{OL} = 1 mA	V_{DDD}–0.5	-	-	V
I_L	leakage current					
	PCD 3-state mode		-	-	50	nA
	CMOS inputs/outputs		-	-	100	nA
Analog output current (pin 1)						
I_{sink}	sink current	V_{DD} = 4.5 V; V_{PCA} = V_{DDD}	1	-	-	mA
		V_{DD} = 2.7 V; V_{PCA} = V_{DDD}	0.5	-	-	mA
I_{source}	source current	V_{PCA} = V_{SS}; V_{DD} = 4.5 V	–1	-	-	mA
		V_{PCA} = V_{SS}; V_{DD} = 2.7 V	–0.5	-	-	mA
Operating voltage range (pin 1)						
V_{PCAL}	operating voltage LOW	V_{DD} = 4.5 V; I_{PCA} = 0	2	-	-	V
		V_{DD} = 2.7 V; I_{PCA} = 0	0.5	-	-	V
V_{PCAH}	operating voltage HIGH	V_{DD} = 4.5 V; I_{PCA} = 0	-	-	3	V
		V_{DD} = 2.7 V; I_{PCA} = 0	-	-	1	V
Input capacitance						
C_I	DIV_I and DIV_{ref} (pins 5 and 8)		-	-	3	pF
	all other inputs		-	-	5	pF

Note to the DC characteristics

1 Supply current at maximum frequency (DIV_I and DIV_{ref}), maximum reference division ratio without any load at the outputs.

AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Main programmable divider						
$f_{DIV(M)}$	input frequency	V_{DD} = 5 V	0	-	18	MHz
		V_{DD} = 3 V	0	-	8	MHz
$V_{I(p-p)}$	input signal amplitude (peak-to-peak value)		0.5	-	-	V
t_{PHL}	propagation delay (HIGH-to-LOW)	DIV_I > FB; C_L = 10 pF				
		V_{DD} = 5 V	-	17	35	ns
		V_{DD} = 3 V	-	40	80	ns
t_{PLH}	propagation delay (LOW-to-HIGH)	DIV_I > FB; C_L = 10 pF				
		V_{DD} = 5 V	-	17	35	ns
		V_{DD} = 3 V	-	40	80	ns
Reference divider						
$f_{DIV(R)}$	input frequency	V_{DD} = 5 V	0	-	16	MHz
		V_{DD} = 3 V	0	-	8	MHz
f_{ref}	reference frequency	V_{DD} = 5 V	-	-	100	kHz
		V_{DD} = 3 V	-	-	50	kHz
t_{H-L}	1.2 MHz output (F12) (HIGH-to-LOW)	V_{DD} = 5 V; C_L = 10 pF	-	-	40	ns
		V_{DD} = 3 V; C_L = 10 pF	-	-	90	ns
I^2C-bus						
f_{CLK}	SDA clock frequency		-	-	100	kHz
t_{spike}	tolerable spike width at SDA and SCL		-	-	100	ns

CHARACTERISTICS OF THE I^2C-bus

The I^2C-bus is for 2-way, 2-line communication between different IC modules. The two lines are serial data line (SDA) and serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

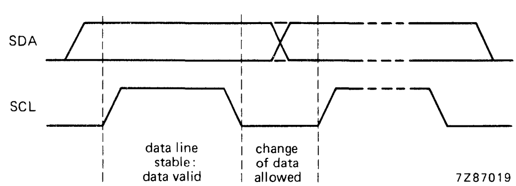


Fig.5 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

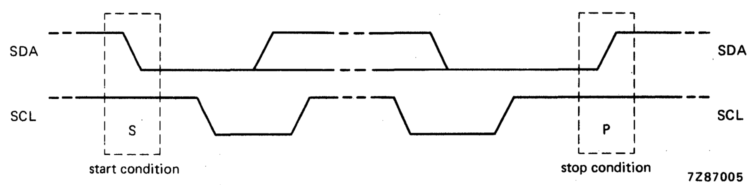


Fig.6 Definition of start and stop conditions.

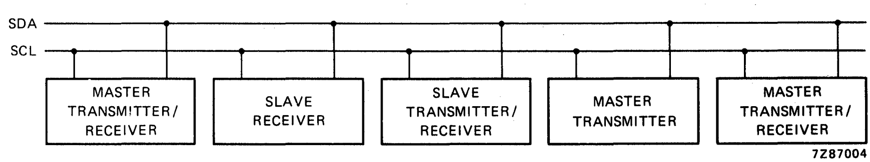


Fig.7 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set up and hold times must also be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig.9.

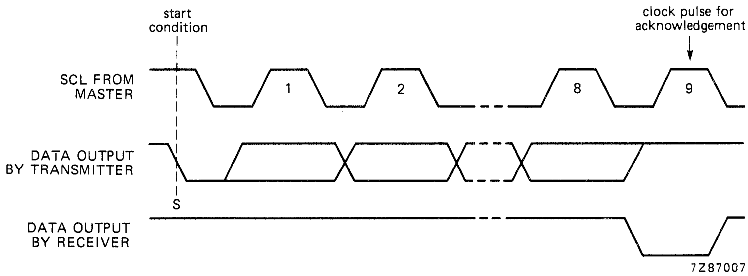


Fig.8 Acknowledgement on the I²C-bus.

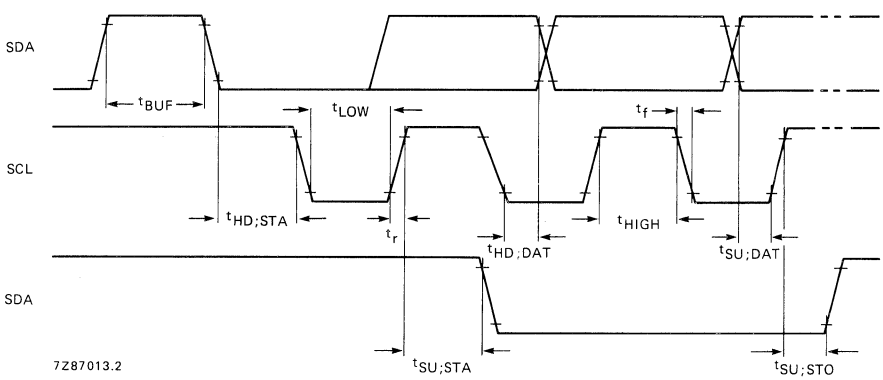


Fig.9 Timing.

Where:

t_{BUF}	$t \geq t_{LOW\,(min)}$	the minimum time the bus must be free before a new transmission can start
$t_{HD;\,STA}$	$t \geq t_{HIGH\,(min)}$	start condition hold time
$t_{LOW\,(min)}$	4.7 µs	clock LOW period
$t_{HIGH\,(min)}$	4 µs	clock HIGH period
$T_{SU;STA}$	$t \geq t_{LOW\,(min)}$	start condition set-up time, only valid for repeated start code
$T_{HD;DAT}$	$t \geq 0$ µs	data hold time
$T_{SU;DAT}$	$t \geq 250$ ns	data set-up time
t_r	$t \leq 1$ µs	rise time of both SDA and SCL line
t_f	$t \leq 300$ ns	fall time of both SDA and SCL line
$T_{SU;STO}$	$t \geq t_{LOW\,(min)}$	stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS}.

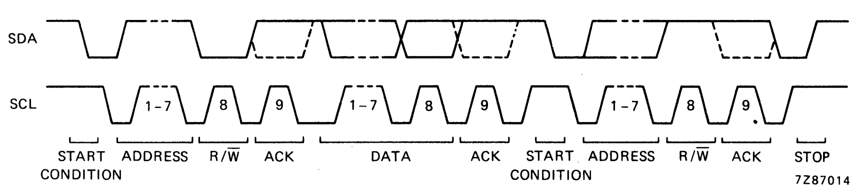


Fig.10 Complete data transfer.

Where:

Clock; $t_{LOW\,(min)} = 4.7\ \mu s$
Clock; $t_{HIGH\,(min)} = 4\ \mu s$

The dashed line is the acknowledgement of the receiver

Maximum number of bytes unrestricted

Premature termination of transfer allowed by generation of STOP condition

Acknowledge clock bit must be provided by the master

I²C protocol

In order to fully program the synthesizer, a sequence of five data bytes is necessary. The data bytes are organized so that on subsequent transfers, not all five bytes need to be sent.
This is achieved by the arrangement in Figure 11.

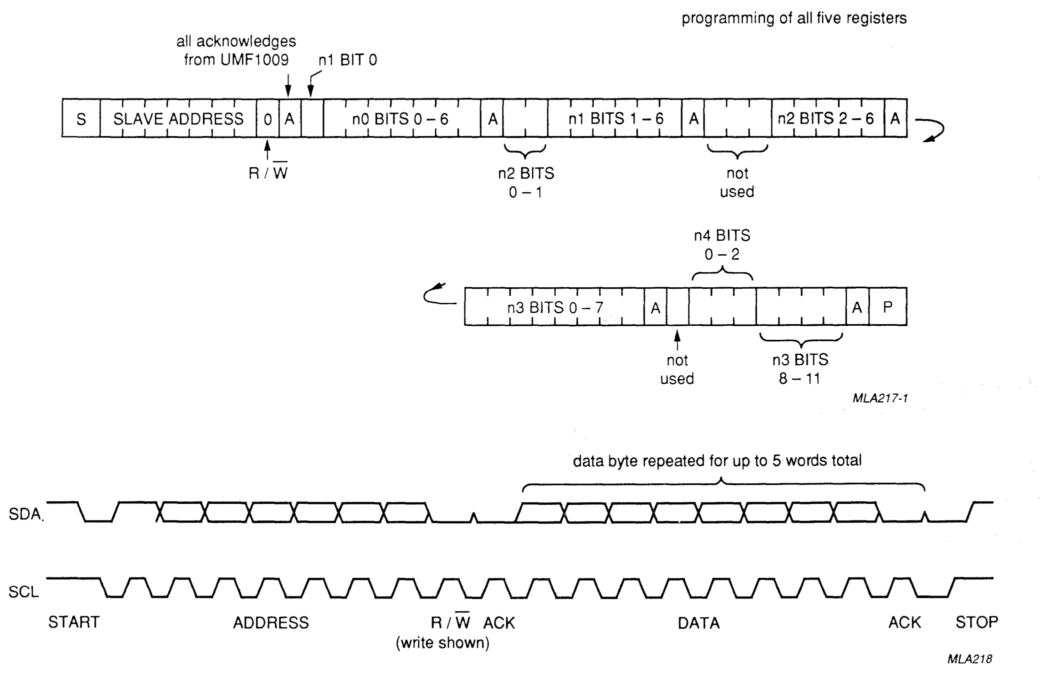


Fig.11 I²C protocol timing.

The information from the I^2C-bus interface is only transferred to the relevant divider(s) on successful completion of the data after the STOP condition. For subsequent programming, e.g. on changing channels, it is only necessary to program the dividers which need altering.

The new information will only be locked into the lower 14 bits of the main divider registers. This reduces the loading on the I^2C-bus.

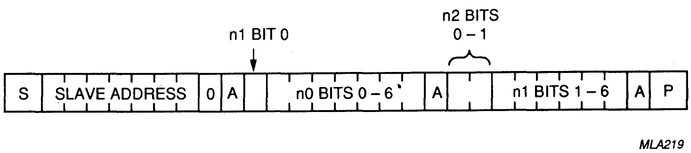


Fig.12 n0 and n1 programming.

Table 1 Data bit map

Register	bit							
	7 MSB	6	5	4	3	2	1	0 LSB
1	n1.0	n0.6	n0.5	n0.4	n0.3	n0.2	n0.1	n0.0
2	n2.1	n2.0	n1.6	n1.5	n1.4	n1.3	n1.2	n1.1
3	X	X	X	n2.6	n2.5	n2.4	n2.3	n2.2
4	n3.7	n3.6	n3.5	n3.4	n3.3	n3.2	n3.1	n3.0
5	X	n4.2	n4.1	n4.0	n3.11	n3.10	n3.9	n3.8

Where:

n0, n1, n2 comprise the main divider
n3, n4 comprise the reference divider
n0.0 is the least significant bit of n0 and so forth
X = don't care - bit position is not used.
Bit 7 (the MSB) is transmitted first on the bus.

Slave address select (A0, A1)

Selection of the device slave address is achieved by connecting A0 and A1 to either V_{SS} or V_{DD}.

The slave address is defined in accordance with the I^2C-bus specification as shown in Figure 13.

1	1	0	0	0	A1	A0	R/$\overline{W}$

Fig.13 Slave address.

APPLICATION DIAGRAM

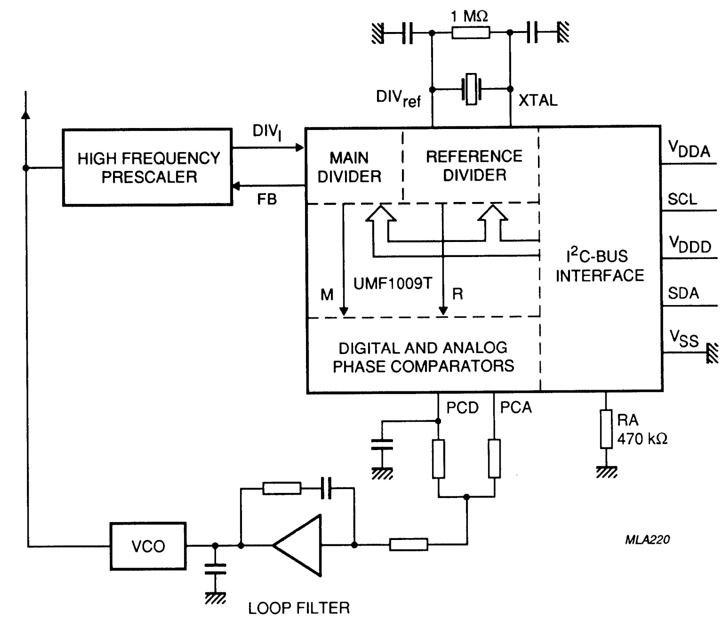


Fig.14 Application diagram.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

Signetics

Section 7
Cellular chip set

RF Communications

INDEX

Cellular chip set design guide

RF Communications

The Philips Components-Signetics Cellular chip set is the world's first complete chip set commercially available from one manufacturer. It combines both Bipolar and CMOS technologies to bring a highly integrated solution to the market. The complete chip set consists of 12 ICs that handle the processing of data, the processing of audio, the receiver, the switching of channels and the transmitter.

This section describes how the chip set functions and how the software interacts with the chip set. A complete demo board can be ordered through any local Philips Components-Signetics sales office.

INTRODUCTION

1. CELLULAR SYSTEM DEFINITION

A cellular system consists of an FM radio network covering a set of geographical areas (known as Cells) inside of which mobile two-way radio units, like Cellular Telephones, can communicate. The radio network is defined by a set of Base Stations distributed over the area of system coverage, managed and controlled by a centralized or de-centralized digital switch equipment known as MTSO, or Mobile Telephone Switching Office. A base station in its geographical placement is known as a cell site. It is composed of low powered FM transceivers, power amplifiers, control unit, and other hardware depending on the system configuration. Its function is to interface between cellular mobiles and the MTSO. It communicates with the MTSO over dedicated data links, wire or non-wire, and communicates with mobiles over the air waves. The MTSO's function is controlling call processing, call setup, and release which includes signalling, supervision, switching and allocating RF channels. MTSO also provides a centralized administration and maintenance point for the entire network. It interfaces with Public Switched Telephone Network (PSTN), over wire line voice facility, to honor services to and from conventional wire line telephones. Figure 1.1 depicts the components and layout of a cellular system.

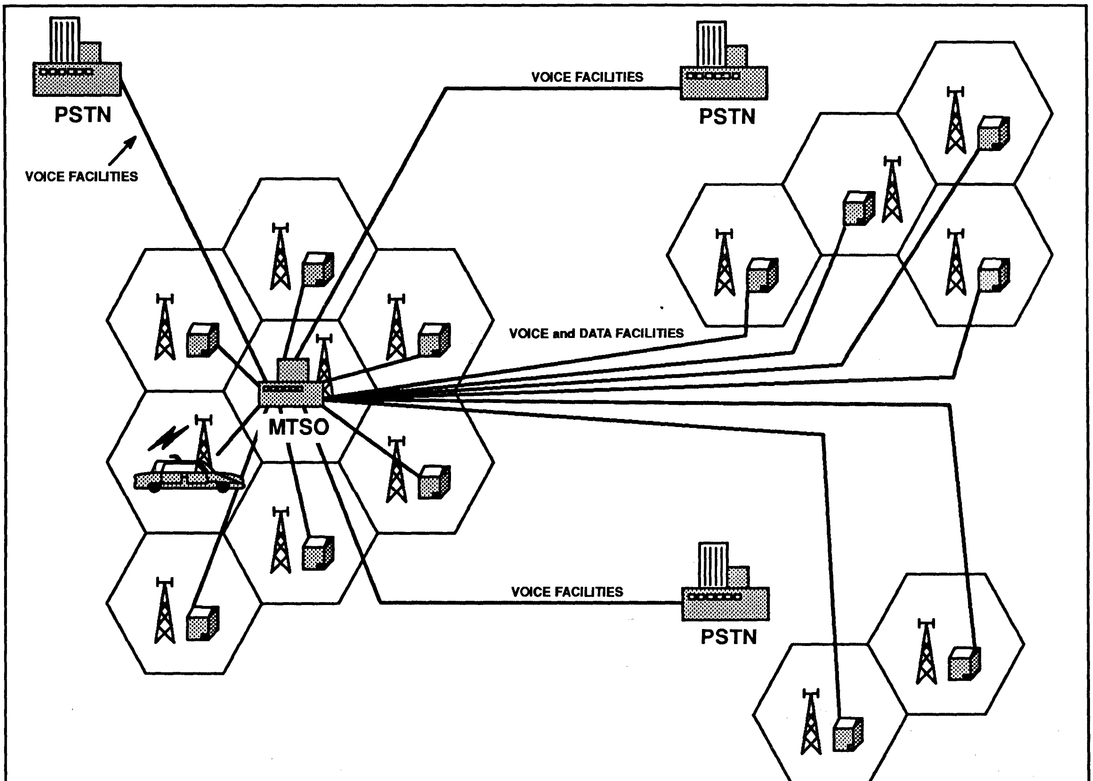


Figure 1.1. The Components and Layout of a Cellular System.

An MTSO is known under different names depending on the manufacturer and on the system configuration. MTSO (Mobile Telephone Switching Office) was given to it by Bell Labs; EMX[1] (Electronic Mobile Xchange) by Motorola; AEX[2] by Ericcson; NEAX[3] by NEC; SMC (Switching Mobile Center) and MMC[4] (Master Mobile Center) are Novatel's.

There are several types of Cellular telephones: mobiles, or car mount; portable, or pocket phone; and hand-held, or transportable phone. They fall into three classes (TACS has 4 classes) defined by the amount of their power output: Mobiles (Class 1) radiate the most power; Transportables (Class 2); Pocket phones (Class 3; Classes 3 and 4 for TACS) have minimum power output. Tables 1.1a and 1.1b show the classes of cellular phones and their power levels for AMPS and TACS, respectively.

Table 1.1a. Power of Mobile Phone for AMPS

Power Level	Power of Mobile Phone for AMPS					
	Mobile Station Power Class					
	I		II		III	
	dBW	mW	dBW	mW	dBW	mW
0	6	4000	2	1600	-2	630
1	2	1600	2	1600	-2	630
2	-2	630	-2	630	-2	630
3	-6	250	-6	250	-6	250
4	-10	100	-10	100	-10	100
5	-14	40	-14	40	-14	40
6	-19	15	-18	15	-18	15
7	-22	6	-22	6	-22	6

Table 1.1b. Power of Mobile Phone for TACS

Power Level	Power of Mobile Phone for TACS							
	Mobile Station Power Class							
	I		II		III		IV	
	dBW	mW	dBW	mW	dBW	mW	dBW	mW
0	10	10000	6	4000	2	1600	-2	630
1	2	1600	2	1600	2	1600	-2	630
2	-2	630	-2	630	-2	630	-2	630
3	-6	250	-6	250	-6	250	-6	250
4	-10	100	-10	100	-10	100	-10	100
5	-14	40	-14	40	-14	40	-14	40
6	-19	15	-18	15	-18	15	-18	15
7	-22	6	-22	6	-22	6	-22	6

A cell is defined by its physical size, and more importantly by the size of its population and its traffic patterns. An entire city like Chicago can be one cell. There are disadvantages, however, to such definition in that the number of channels would be limited to a small fraction of inhabitants, i.e., the system's capacity would be very limited, and the transmitter of the cell would have to be very powerful to cover such a large area.

The major advantage behind a cell-based system configuration is the frequency re-use scheme, whereby, the same set of frequencies/channels can be allocated to more than one nearby cell provided the cells are a certain distance apart. Most cellular systems adopt a frequency re-use pattern of 7.

The last constituent of a Cellular system is the communication protocol that governs the way a phone call is established. Cellular protocols differ between countries, e.g., in the USA the Advanced Mobile Phone Service standard (AMPS) is used, while in Canada the AURORA 800 is used. In Europe each country has its own standard. Total Access Communication System (TACS) is used in the United Kingdom; NMT or Nordic system is used in the Scandinavian countries (Denmark, Norway, Sweden, and Finland); RC2000 is used in France; and NETZ C-450 is used in Germany. NTT is the Japanese standard for cellular.

1.1. AMPS and TACS Spectrum Allocation

In 1980 the FCC changed its policy towards a one-system-per-market, and established two licensed carriers per service area. It was the FCC 's view that such an approach would eliminate monopoly and provide some competitive advantages. Two systems (A and B) emerged, each with its own group of channels, to share the allocated spectrum (Figure 1.2). System A is defined for the non-wire-line companies, and system B is defined for the wire-line companies.

AMPS Cellular systems employ a frequency spectrum of 20MHz made up of 666 channels with 30kHz channel spacing. The transmit frequency at 825.030MHz is specified as channel 1, and transmit frequency at 844.980MHz is specified as channel 666. The receiver operates at 45MHz above the transmit frequency, therefore, channel 1 receives at 870.030MHz and channel 666 receives at 889.980MHz. An additional 5MHz spectrum was subsequently added to the existing 20MHz which increased the number of channels from 666 to 832.

As for the TACS Cellular standards, its frequency spectrum is 15MHz comprised of 600 channels with 25kHz channel spacing. The transmit frequency at 890.0125MHz is specified as channel 1, and the transmit frequency at 904.9875MHz is specified as channel 600. The receiver operates at 45MHz above the transmit frequency, therefore, channel 1 receives at

935.0125MHz and channel 600 receives at 959.9875MHz.

The AMPS and TACS channel spectrum is divided into 2 basic groups. A set of channels are dedicated for control information exchange (mobile ↔ cell site) and are termed control channels (shaded areas). The second group, made up of the remaining channels, are termed voice channels and are used for conversations.

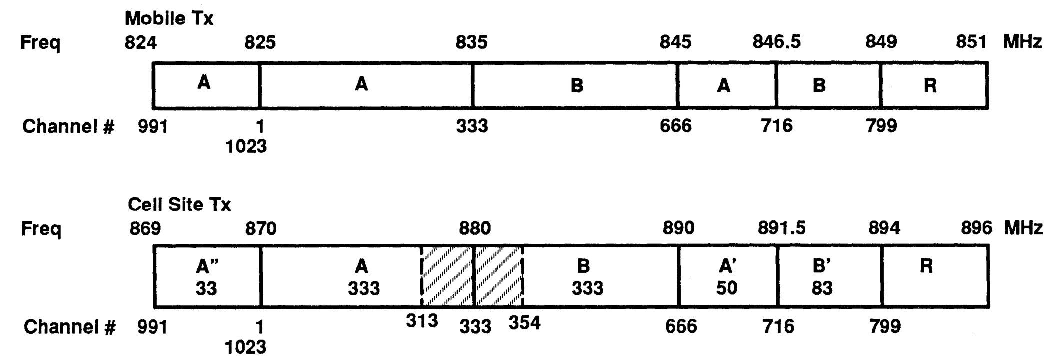


Figure 1.2. AMPS Frequency Management.

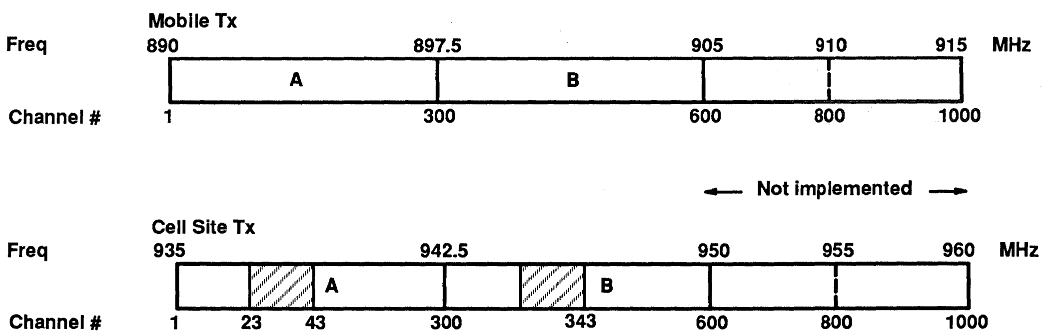


Figure 1.3. TACS Frequency Management

Figures 1.2 and 1.3 show the frequency spectrum and channel assignment for AMPS and TACS, respectively. Both figures include the additional spectrum of 166 extra channels for AMPS and 400 channels for TACS. Note, however, that TACS' additional spectrum has not been implemented and the dedicated control channels are for the 600 channel system. The shaded area outlines the set of DEdicated Control Channels. Table 1.2 below summarizes the frequency parameters of AMPS and TACS. The set of control channels may be split by the system operator (MTSO) into subsets of DEdicated Control Channels, Paging Channels and Access Channels. Figure 1.4 depicts an optional configuration of control channels by the MTSO, based on the Combined Page/Access channels variable (CPA) which is set by an overhead message.

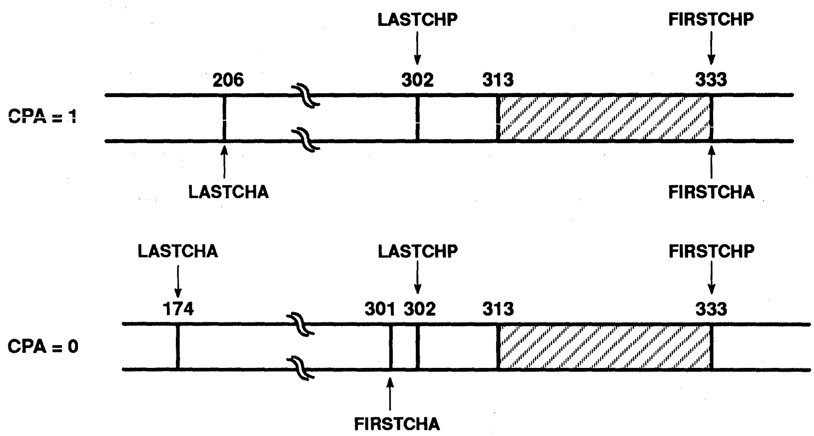


Figure 1.4. Optional Division of Control Channels for 'System A' Based on CPA.

1.2. An Integrated chip-set addressing cellular market needs

Cellular mobile telephones have been with us for several years. The first equipment was complex and highly priced (affordable only by the business sector). A rapid build-up in the number of users, fuelled by competition, has resulted in a steadily decreasing selling price to the consumer. In order to remain competitive, setmakers must continually strive to reduce costs. Key to achieving this aim is the adoption of an optimum architecture. Such an architecture must minimize complexity through the use of VLSI.

Existing sets tend to comprise a mix of analog functions provided by standard integrated circuits coupled with digital functions using custom/semi-custom circuits. By adopting a total chip-set approach using bipolar and CMOS technologies where most appropriate, a more optimal solution can be achieved. A series of developments with careful attention to low current consumption has resulted in a chip set of six ICs that is applicable to portables, transportables and mobile telephony. The chip set is suitable for both the American AMPS and the English (United Kingdom) TACS standards.

A software package implementing the AMPS and TACS standards, written entirely in PL/M51, has been developed to introduce a fully functional cellular radio.

References

1. EMX is a trade mark or symbol of· Motorola
2. AEX is a trade mark or symbol of Ericcson
3. NEAX is a trade mark or symbol of NEC
4. SMC and MMC are trade mark or symbols of Novatel

Table 1.2 AMPS and TACS Frequency Allocation

	AMPS	TACS
Channel Spacing	30kHz	25kHz
Spectrum Allocation	20MHz	15MHz
Additional Spectrum	5MHz	10MHz
Total # of Channels	832	1000

System A Frequency Allocation					
AMPS			TACS		
CH #	Mobile TX MHz	Mobile RX MHz	CH #	Mobile TX MHz	Mobile RX MHz
1	825.030	870.030	1	890.0125	935.0125
313[1]	834.390	879.390	23[2]	890.5625	935.5625
333[2]	834.990	879.990	43[1]	891.5625	936.5625
667	845.010	890.010	300	897.5625	942.5625
716	846.480	891.480			
991	824.040	869.040			
1023	825.000	870.000			
System B Frequency Allocation					
AMPS			TACS		
334[3]	835.020	880.020	323[3]	897.0625	942.0625
354[4]	835.620	880.620	343[4]	897.5625	942.5625
666	844.980	890.000	600	904.9875	949.9875
717	846.510	891.000			
799	848.970	894.000			

NOTES:
1. Last DEdicated Control Channel for System A
2. First DEdicated Control Channel for System A
3. Last DEdicated Control Channel for System B
4. First DEdicated Control Channel for System B

SYSTEM ARCHITECTURE

2. OVERALL ARCHITECTURE

The RF section includes low power frequency synthesizers (UMA1014) and a single chip second mixer/oscillator/IF amplifier/demodulator (NE605). A single chip CMOS data processor (UMA1000) performs all functions associated with control data, supervisory and signaling tones. All voice, alert and DTMF functions are contained on two audio processor devices; one CMOS and the other bipolar (NE/SA5751 and NE/SA5750, respectively). Switched capacitor integrated filter technology is used in all baseband processing functions to achieve a minimum number of external passive components. The system's master controller is the 80C552 which is a derivative of the Intel 80C52 µcontroller with integrated ADC (Analog–to–Digital Converter), PWM (Pulse Width Modulator), I^2C and UART interfaces. The DPROC, the APROCs, and the LOPSYs are interconnected via an I^2C bus which is a 2–wire serial bus that can transfer data at 100kb/s. Refer to Figure 2.1 to view the system's architecture.

2.1. Clocking

A 9.6Hz VTCXO (Voltage controlled Temperature Compensated Xtal Oscillator) is divided by 8 to provide a 1.2MHz frequency for the data processor (DPROC, UMA1000), and the audio processors (APROCs, NE/SA5750/5751). The µcontroller is clocked by aseparate11.059MHz crystal.

2.2. RF Architecture

2.2.1. Receiver Front–End

The receiver adopts a double conversion superhet architecture with a first IF of 45MHz and a second IF of 455kHz. A single transistor circuit is used for the RF amplifier and first mixer stages. The second mixer, second local oscillator, all IF amplification, limiter, demodulator and RSSI functions are provided by the NE605. The receiver's local oscillator comprises a single loop frequency synthesizer, UMA1014 a 7.2MHz oscillator for the frequency synthesizers, and another division by 6 to provide, normally operating at 45MHz above the receive frequency. An on–chip divide by 8, generating a 1.2MHz clock, for the Data and Audio processors, from a 9.6MHz VTCXO.

2.2.2. Transmitter

The modulation is applied to the transmit VCO. A loop bandwidth of approximately 200Hz is used in the transmit synthesizer path, achieving a flat modulation characteristic above 300Hz and permitting sufficiently fast switching time. Hybrid power modules are used to amplify the transmit signal to the level required according to the power class of the equipment.

The cellular system requires the transmit power to be reduced in 4dB steps down to 6mW. To achieve a flat characteristic, independent of gain spreads in the amplifier stages, a power leveling loop external to the PA module is used (Figure 2.2). The output of the power module is adjustable by varying the supply voltage to one or more of the amplifier stages. A power sensor in the output of the transmitter generates a DC voltage related to the transmitter output power. This can comprise a simple diode detector, or a more complex system using a coupler with multiple sensing to reduce sensitivity to load VSWR. The sensor output is compared with a reference DC level using a voltage comparator and the difference used to control the power output. The loop will settle, such that the sensor output will be equal to the reference level. The reference level is derived by integrating the PWM0 output from the µcontroller and is set according to the required output power. Non–linearities in the sensor may be accommodated by suitable software calibration of the reference level.

There are a number of circuit functions which need to disable the transmitter (signal TX_{DIS}): the µcontroller for system control (in the case of a malfunction); audio processor for VOX control in discontinuous voice mode; and data processor if a collision is detected during reverse control channel access. Control of the transmitter is provided by a single line with controlling devices 'pulling low' to disable in a wired–OR configuration.

2.3. Baseband Architecture

2.3.1. Audio Processors

All audio functions associated with the voice channel are processed in the NE5750/51 (Figure 2.4). Microphone amplification, VOX provision, compression, expansion and audio power output are provided in a bipolar IC, the NE5750. All filters, pre–emphasis, deviation limiting, de–emphasis, signal path switching, volume control and tone generation are provided in a CMOS IC, the NE5751.

Switched capacitor techniques have been used to fully integrate all filter functions. The tone generator is used for DTMF signaling, ringing tones and key confirmation. The pinouts of the two ICs have been arranged so that a straightforward interconnection is achieved on the PCB layout. Access to different parts of the audio signal path is inherent in this approach and eases the connection of ancillary units such as modem, hands–free adaptor, etc.

2.3.2. Data Processor

All functions associated with control data, supervision (SAT) and signaling (ST) are incorporated into a single CMOS data processor IC, the UMA1000 (Figure 2.5).

In the receive path, a dedicated two–wire serial link (RX_{CLOCK}, RX_{LINE}) passes the fully decoded data word to the µcontroller. Clocking is under control of the µcontroller and is not time–critical. When operating on a voice channel, the dotting detector, which precedes a data burst, is used to blank the audio path directly to prevent data bursts from being heard by the user (RA_{CTRL}).

In the transmit path, a 40–bit (36 data bits and 4bits of framing and DCC) word to be transmitted is passed from the µcontroller to the data processor via another dedicated two–wire serial link (TX_{CLOCK}, TX_{LINE}) where it is held in a buffer. The µcontroller can trigger immediate transmission of the data at the appropriate time. The base station returns the status of the channel access within the busy/idle stream. If the busy/idle stream does not revert to 'busy' during the specified window, transmission is aborted (TX_{CTRL}). This time–critical channel arbitration sequence is performed by the data processor IC independent of the µcontroller.

2.3.3. Microcontroller

The PCB80C552 µcontroller handles the functions of the cellular portable with low power and high operating speed. This CMOS processor is a derivative of the 8051 µcontroller. It can operate with an instruction cycle time of less than 1µS, and about 50% of its operations execute in a single machine cycle. This device also supports extensive power saving modes, giving approximately 75% power saving in a standby mode, and a micropower power–down mode for backup battery operation. The low power modes ideally complement the UMA1000T data processor which processes the continuous cellular data stream, enabling the µcontroller to operate in a burst processing mode. Thus the processor may spend in excess of 90% of the time in a standby mode.

The processor operates over a wide temperature range and has a high degree of EMC protection. It has an 8–channel–multiplexed 10–bit ADC, used for RSSI processing, battery voltage monitoring etc, and a pseudo 8–bit analog output (based on PWM) used to control the transmit amplifier's power level. A full hardware implementation of an I²C UART (in addition to the standard RS–232 UART), six 8–bit I/O ports and an 'on–chip' watchdog timer are all included. It has an industry standard 8052 core, which gives access to an extensive range of development support facilities, including 'High Level Language' support (PL/M51, a Pascal–like language), 'In Circuit Emulation' and symbolic debug facilities. This promotes fast development and debugging of equipment software.

A software package implementing the AMPS and TACS standards, written entirely in PL/M51, has been developed to introduce a fully functional cellular radio.

2.3.4. I²C Bus

The I²C bus (Figure 2.3) is essentially a Local Area Network (LAN) for integrated circuits. Each device has its own 7–bit address and is connected to a two–wire serial bus. The interface protocol is self–checking and self–arbitrating, allowing a multi–master control of the bus. Data is transferred at a rate of 100kb/s as a message block consisting of device address, a read/write indication, and the data block. A general description of the I²C bus is specified in the publication "The I²C Bus Specification" (order code 9398–358–10011).

The multi–master mode of the I²C bus can allow a simple test harness to take full control of the equipment for functional system tests and alignment in production. Test functions of the devices not used in normal operation can be exercised in this way.

2.4. Other I²C Peripherals

In addition to the major components of the Cellular Radio Chip Set, there are a large number of general purpose peripheral ICs with I²C interfaces.

The PCF8576 is one of a range of LCD matrix and segment drivers. This device can address up to 160 segments, and is cascadable for larger displays. It is available in TAB packaging, allowing the device to be directly mounted onto a flexible connector driving the LCD. A six–wire connection to the main PCB (power, I²C and contrast control), shows further cost advantages by reducing PCB area over that needed for normal direct LCD drivers.

This device exhibits most of the advantages that can be attained when using I²C peripherals for adding features to any particular equipment. The range of such devices cover most requirements, with the availability of EEPROMs, RAMs, clock/calendars, tone generators and I/O expandors, all usable on the same bus with no compatibility problems.

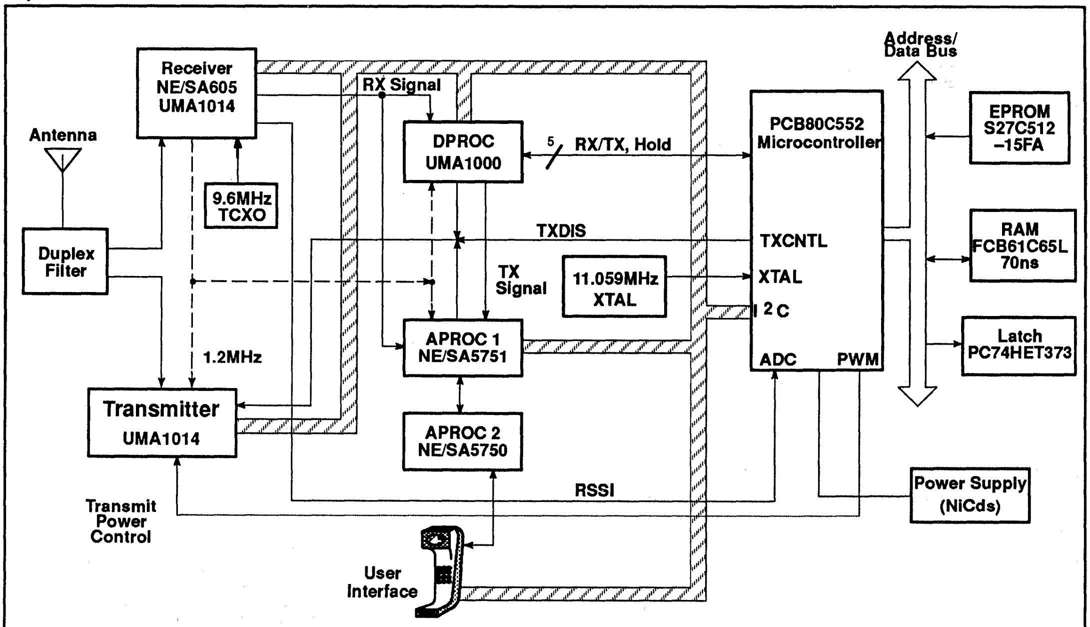


Figure 2.1 System Architecture

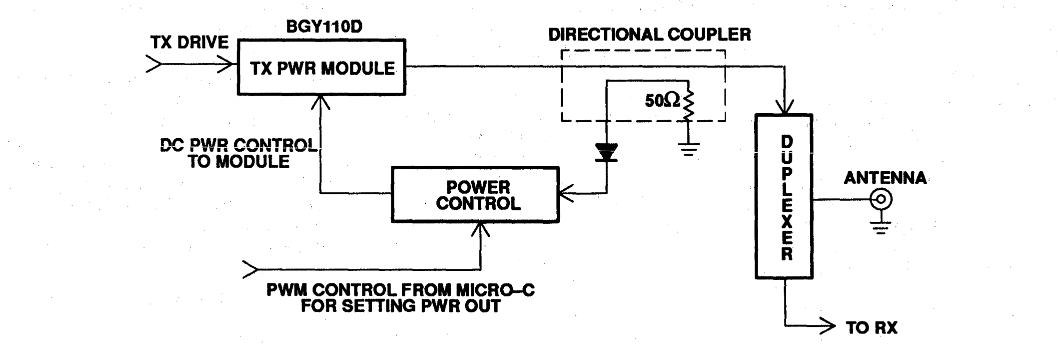


Figure 2.2 Transmitter Power Loop

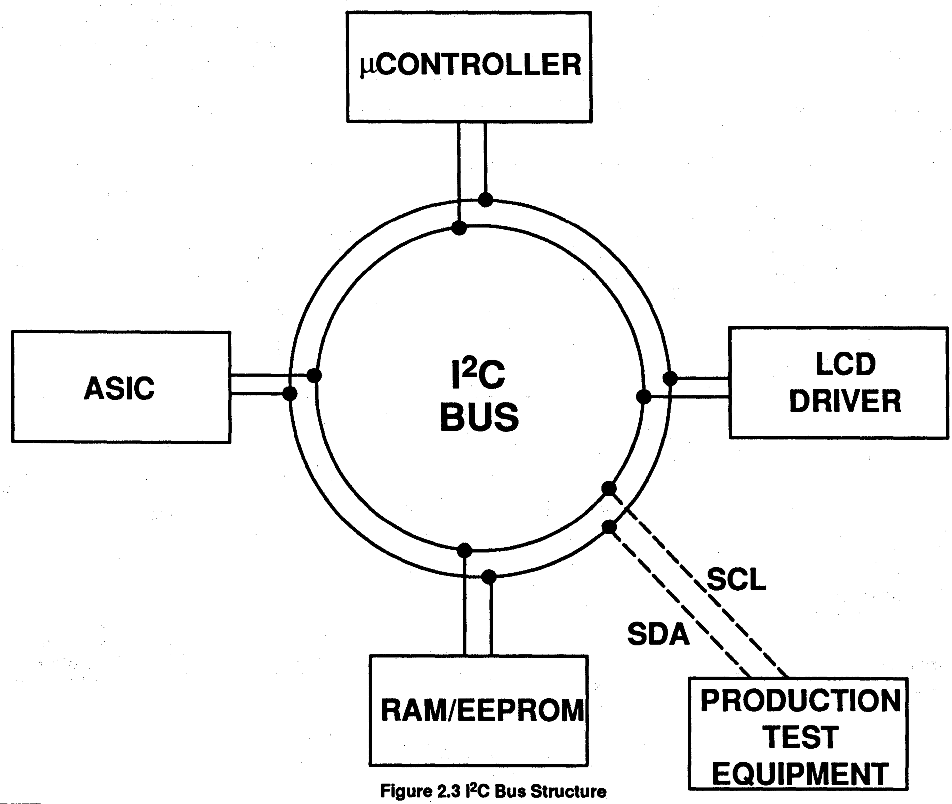


Figure 2.3 I²C Bus Structure

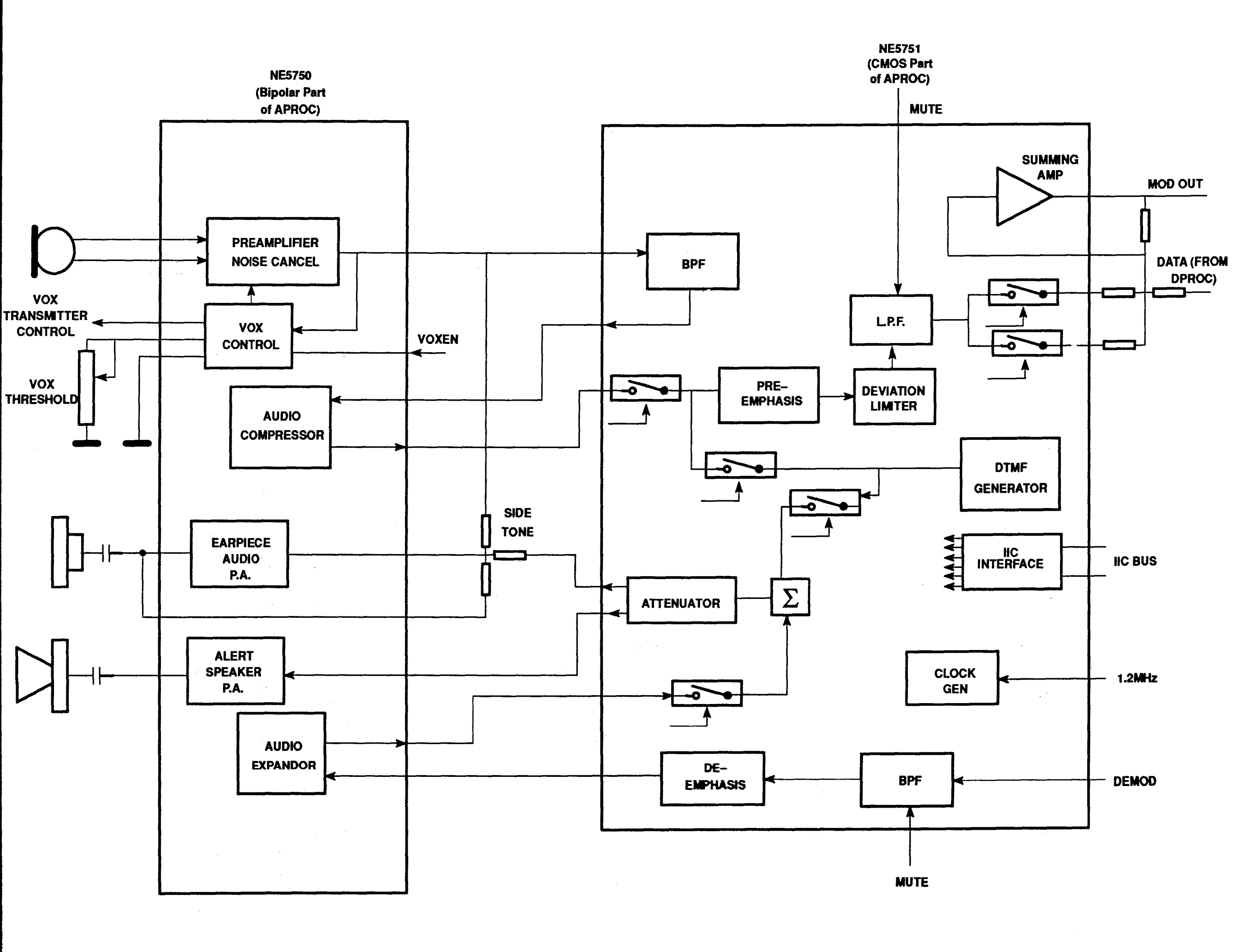


Figure 2.4 NE5750 and NE5751 Audio Processor Block Diagram

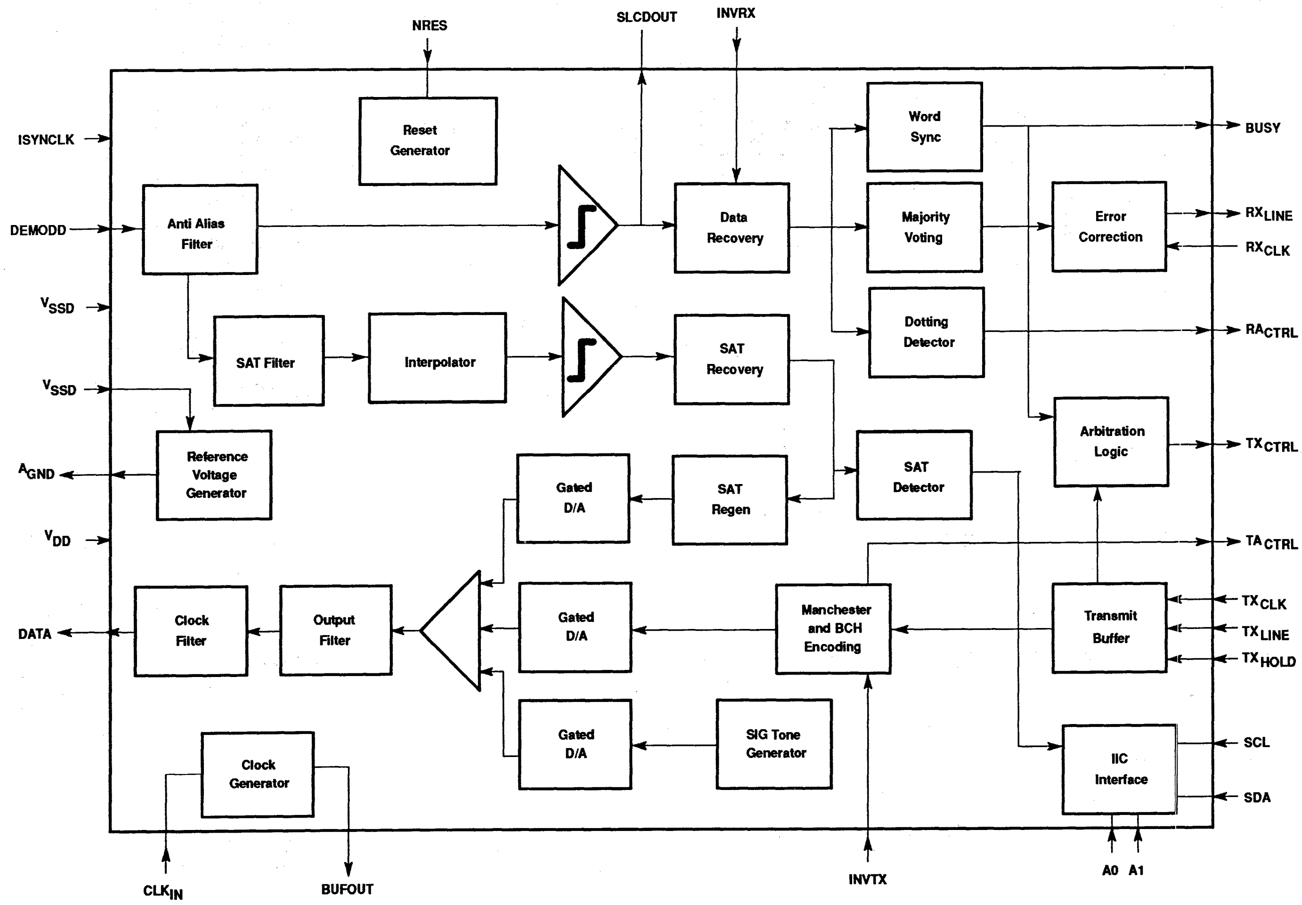


Figure 2.5 UMA1000T Data Processor Block Diagram

HARDWARE DESCRIPTION

3. OVERVIEW

The chip-set evaluator hardware design is divided into two major sections: RF section, and Data/Audio and Program Control section, also known as the Baseband section.

The RF section consists of a receive and a transmit Local Oscillators, a receiver front-end circuit, a duplexer, and a transmit module. The Local Oscillators are clocked from a single source, a Temperature Compensated Xtal Oscillator (9.6MHz VTCXO). The receiver front-end circuit is composed of a preamp mixer for 1st IF, and 2nd IF and a demodulator circuit (NE605, Figure 3.1). The Local Oscillators' circuits utilize the UMA1014, a single chip frequency synthesizer with on-board IIC interface allowing easy programmability and control from the micro. (Figures 3.3, 3.4).

The Base Band section consists of the Logic and Program Control circuit (Figure 3.6), a Data PROCessing circuit (UMA1000, Figure 3.9), and an Audio PROCessing circuit which includes an Audio Power Amplifier, (NE/SA5750/51, TDA7052, Figure 3.10). A separate MAX-232 driver board is provided to interface the Program Control circuit to a dumb terminal. This will aid the user in software development and debugging (Figure 3.8).
Tables 3.4 and 3.5 show the codes and specifications a cellular phone should meet and how they can be met [Ref. 3]. Next we will identify the specifications that require further careful design.

3.1. RF

3.1.1. Receiver Design Consideration

3.1.1.1. Preamp Mixer Design

The AMPS specification calls for a -116dBm sensitivity at 12dB (SINAD) demodulated signal-to-noise ratio (EIA/IS-19-B 2.3.1.3.). There is 6dB improvement in performance due to the pre-emphasis/de-emphasis function on board the NE/SA5751. This means that the detected S/N ratio has to be 6dB prior to pre-emphasis/de-emphasis. For a 1kHz tone and a typical frequency deviation of 8kHz, normal FM demodulation characteristic curves show that a S/N ratio of 1-2dB is required. For a channel bandwidth of 30kHz, the input noise will be -129dBm. If we choose -119dBm as our sensitivity design goal, it appears that this noise can only be degraded 8dB by the front-end in order to achieve the minimum detectable input carrier level of -119dBm. Assuming a worst case loss of 5dB by the duplexer, a post duplexer amplifier with 3dB noise figure is required. In addition, because the front-end amplifier is followed by an 881MHz ceramic filter and a mixer, the distribution of gains has to be optimized so that the overall noise figure of the front-end (including the duplexer) is not going to exceed 8dB. In Figure 3.2 the gains and NFs are shown on the block diagram.

While all of the gain of the front-end can be achieved in the preamp, this has to be traded off against the required intercept characteristics. The AMPS specification calls for good detection in the presence of signals that are 60kHz and 120kHz away from the carrier. The carrier should be close to the minimum acceptable level for good detection. In this condition, the interfering signals should be 65dB larger than the desired carrier until they begin to cause reduction in detected signal level. A little bit of analysis shows that this specification (EIA 2.3.3.3) translates into a -17dBm system third-order intercept as measured from the antenna. Looking at Figure 3.2, since the first IF filter (30kHz wide, 4-pole crystal filter at 45MHz) is narrow enough to eliminate the interfering signals, the intercept point of the overall system is set mostly by the front-end and the first mixer. Assuming a 5dB worst case loss in the duplexer, a 10dB gain in the front-end amplifier and 2dB loss in the 881MHz ceramic filter, the first mixer must have an input intercept of about -14dBm (See Figure 3.1). For every dB of improvement in the intercept point of this mixer, the gain of the front-end can be improved by 1dB to help it better overcome the noise figure of the following stages. Having said this, however, it is recommended that the intercept point of the 2nd mixer not be ignored because future cellular requirements call for dynamic frequency allocations, or other modulation methods that may cause adjacent channels to be used within the same cell.

While we have used a bipolar device as our first mixer, a dual gate MOSFET has the potential of exhibiting better third-order intermod characteristics. Another technique for the front-end is to combine the preamp and mixer in one device. This has the advantage of relaxing the mixer intercept point by about 8dB. The problem, however, is that one has to depend on the duplexer filter for all of the image rejection to reduce the effective noise figure of the mixer.

3.1.1.2. FM IF

The Signetics NE605 chip is used to produce the FM IF. This chip first mixes the 45MHz first IF signal down to 455kHz (2nd IF). The signal then goes through approximately 100dB of gain in a multi-stage limiter. The fully limited signal is then demodulated in the final quad-tank FM demodulator. The demodulator provides two outputs: Data and Audio. The data output contains data bursts and goes to the DPROC DEMODD input (Pin 3). The audio output is mutable; it goes to the APROC-NE5751's $RXBF_{IN}$ input (Pin 17). The Audio channel is muted for the 100ms data bursts period during a conversation. Another output of the chip is an internally temperature-compensated RSSI, Received Signal Strength Indicator, with more than 90dB dynamic range. With about 115dB overall gain and high impedances, the 2nd IF can pick up a multitude of signals and frequencies that are readily available in a cellular phone. (We will cover these when we discuss the layout and shielding issues). In recent years a number of cellular phone manufacturers have increased the first IF frequency to around 80-90MHz to be able to use SAW device first IF filters, and obtain better image rejection characteristics. While this can easily be accomplished with the NE605 chip, the increase of the IF frequency will increase the probability of closing spurious feedback loops that can cause regenerative oscillations in case layout is not done carefully. The AMPS spec for RSSI linearity (2.6.3) is directly satisfied by this FM IF, while other specs, such as sensitivity and hum and noise S/N (2.2.2.4.3), are partially satisfied by the FM/IF. In the case of the hum and noise S/N, the phase noise of the receive synthesizer is also important, but it can be neglected as long as its residual FM noise is much less than 100Hz.

3.1.2. VTCXO

The 9.6MHz Voltage controlledTemperature Compensated Xtal Oscillator provides a reference clock to the transmit and receive Local Oscillators where it is divided by 8 to generate a 1.2MHz clock source to the APROCs and the DPROC.

3.1.3. Local Oscillators

The receive Local Oscillator circuit consists of the single chip frequency synthesizer, UMA1014, with on-board prescaler and loop filter, and a 926MHz VCO (45MHz above receive frequency. (Figure 3.3)

The transmit Local Oscillator circuit is similar to that of the receive LO circuit except that the VCO frequency is 836MHz and is used to modulate the signal (data or SAT+Audio) to be transmitted. (Figure 3.4)

The receive local oscillator frequency is set by the master µcontroller as follows: The µcontroller accesses the frequency synthesizer, via IIC interface, and loads it with a reference and main divider values. The reference divider divides the 9.6MHz reference frequency down to 15kHz. The main divider value divides the VCO output frequency, after a fixed divide by 2 prescaler, to produce 15kHz. A mismatch, detected by the small phase comparator, causes the VCO to adjust its frequency such that, when divided by the main divider, it will yield 15kHz. Note that the VCO output is 45MHz above the carrier frequency, and the main divider value must be set accordingly.

The transmit Local Oscillator frequency is set similarly by the master µcontroller. Note however that the VCO output equals the carrier frequency, and that the reference frequency is 1.2MHz.

3.1.3.1. Receiver Frequency Synthesizer

The design of the loop filter of the synthesizer and its resulting phase noise will help satisfy the (2.2.2.4.3) spec. In this case we have used a 200Hz filter which will give acceptable phase noise characteristics, and be fast enough for switching between channels.

3.1.3.2. Transmitter Frequency Synthesizer

While a variety of synthesizer configurations are available, a more reliable operation with fewer spurious signals can be achieved if both transmit and receive frequencies are directly synthesized independent of each other. The transmit synthesizer has the same loop time constant as the receive synthesizer. The only difference is that a 300Hz-6kHz bandpass filtered signal (Voice + SAT) is added to the VCO modulating input.

3.1.4. Transmitter Design Considerations

3.1.4.1. Power Leveling Loop

A cellular system requires the transmit power to be reduced in 4dB steps down to 6mW. To achieve a flat characteristic, independent of gain spreads in the amplifier stages, a power leveling loop external to the PA module is used. The output of the power module is adjusted by varying the supply voltage to one or more of the amplifier stages. A PWM signal coming out of the µcontroller is low-pass filtered to get a DC control signal. A phone could, in principle, be calibrated in this mode using an external power meter to find the corresponding PWM number for each power level. The problem, however, is that with small variations in gains or load impedance, the power out could fluctuate as well. Also, if the antenna is accidentally removed with the unit in operation, the reverse power may damage the unit. To solve these problems, a feedback loop is generated by making a -15dB directional coupler which senses the reverse power (see Figure 3.5) and rectifies it. This can be a simple diode detector, or a more complex system using a coupler with multiple sensing and a dynamic matching network to further reduce sensitivity to load VSWR. This error signal is, in effect, added to the DC control signal coming from the µcontroller PWM so as to control the power module with a 20µs time constant. The loop will settle, such that the directional-coupler diode detector output will be equal to the reference level. The reference level is derived directly from the µcontroller (PWM0 port) and is set according to the required output power. Non-linearities in the sensor may be accommodated by suitable software calibration of the reference level. (This part of the circuit satisfies the 3.2.1.3 RF power output levels.)

3.2. BASEBAND

3.2.1. Logic and Program Control

This section of the baseband consists of a central processing and management unit, the PCB80C552 µController, and its associated circuitry. The µcontroller fetches program instructions stored on board a 64kBytes Programmable Read Only Memory (PROM, SN27C512-15 FA). An 8kBytes of Static RAM (FCB61C65-70) is used to store data structures and program variables. Because the µcontroller is based on Intel's 8051 family of µcontrollers, and the data bus and the lower-order address bus share the same port (port0), a 3-state Octal D-type transparent latch (74HC573D) is used to separate data from address (Figures 3.6, and 3.8). Table 3.1 lists the I/O signals on the µcontroller and their functions in the Cellular application.

3.2.2. Data Processing

The data processing circuit consists of a DPROC, UMA1000T IC, with a small number of external passive components. The DPROC function is to decode received, demodulated data (DEMODD), from the NE605 and to encode and transmit digital data from the µcontroller (Figure 3.9). The following sections will describe the receive and transmit paths of the DPROC, and Table 3.2 will describe its inputs and outputs and their functions.

<u>Note on DPROC RESET sequence:</u>

The following sequence should be followed to insure proper operation of the DPROC:

1. Pin 22 - IIC address Pin A1, must be tied HIGH; at least during the reset pulse. (Note that this will alter the DPROC IIC address from 0D8h to 0DCh)
2. Pin 26 - NRESET must be tied HIGH.
3. Pins 6 and 16 - must be tied to the RESET signal from the µcontroller, which was connected to Pin 26 (NRESET). Note that the reset from the µcontroller must be active HIGH, because Pins 6 and 16 are active HIGH. The software must, therefore, change the polarity of the reset pulse accordingly.
4. The RESET signal timing is as follows: $\geq$ 250µsec in the HIGH state; < 1µsec fall time.

3.2.2.1. Receiving Data

The data processor extracts digital data from the NE605 demodulated signal output (DATA). The data stream transmitted on the FOrward Control Channel is composed of a 463-bit message made up of word blocks, where each word block is a 28-bit data word and 12 parity bits repeated 5 times, and preceded by a preamble (dotting) and word synchronization bits (as per EIA/IS-3-D).

Detection of the Dotting sequence (10101010...) is an indication to the DPROC that a message has arrived. The word synch, WSYNC, sequence trains the clock recovery circuitry and synchronizes it.

DPROC then extracts from each word block the 5–time repeated word and selects, by majority voting, one word. The selected word goes through error detection and correction where up to one error can be corrected. The DPROC then pulls RX_{LINE} low, indicating to the µcontroller that a data word is available. The DPROC repeats this process for each word block in the FOCC message.

3.2.2.2. Transmitting Data

Data to be transmitted is fed to the DPROC, from the µcontroller, for Manchester and BCH encoding, and conversion to an analog signal. The resultant analog signal output (DATA) goes to the APROC (NE5751) transmit summer input where it is added to an Audio signal (DTMF or speech) path. The transmit summer output is then modulated, in the transmit Local Oscillator block, and sent to the transmit module.

Two other analog components are outputted at Pin 4 (DATA), during Voice CHANnel state:

Signaling Tone (ST) and Supervisory Audio Tone (SAT). ST, a 10kHz carrier, is generated on board the DPROC and is used to acknowledge reception of control messages from the cell site. When ST is transmitted the audio signal in the transmit path is muted (TACTRL, disabling NE5751 T4 & T5 switches). SAT (6kHz $\pm$ 30Hz signal) is used by the cell site to measure the mobile's signal quality. It is received by DPROC's Digital PLL, and transponded to the cell site by summing it with the speech signal coming from the APROC (NE5751, T4 & T5 enabled). Both ST and SAT are disabled when data is transmitted on the reverse voice channel (done inside DPROC).

3.2.3. Audio Processing

The audio processing functions for cellular applications are implemented on two IC's, the NE5750 and the NE5751 (Figure 3.10).

3.2.3.1. NE5750

The NE5750 is a Bipolar IC. It integrates a noise cancellation circuit, a VOX circuit and a Companding circuit.

Noise Cancellation

When the input signal, produced by the microphone, drops below a certain threshold (e.g., when there is no speech), the noise cancellation circuitry reduces the overall gain by 10dB. This threshold is set by an external resistor R3 (R3 Ohm x 0.05 V_{RMS}). The background noise canceller circuit has a built-in hysteresis to prevent VOX activation when the input signal is approximately at the threshold level.

VOX

Voice Operated Transmission, with an attack (C3), and decay (T = C3R1) set with external components.

Companding

The audio signal's dynamic range is compressed before transmission, and expanded after reception.

3.2.3.2. NE5751

The NE5751 is a CMOS IC. It integrates a de-emphasis, a pre-emphasis, a deviation limiter, and a DTMF generator. It also provides programmable digital switches to control the signal path (audio mute), and a digital volume control.

Pre-emphasis/de-emphasis: In order to improve FM receiver sensitivity and maintain good S/N for higher audio tones, the baseband audio signal's higher frequency components are amplified before transmission (pre-emphasis), and attenuated after reception (de-emphasis).

Deviation limiter: It guarantees a maximum audio signal (voice) deviation of $\pm$12kHz.

DTMF generator: Two DTMF registers are accessible form the I^{2}C bus: High tone and Low tone DTMF registers. The High and Low frequency tones are computed as follows:
High frequency = 1200kHz/6/HD
where HD is the High register value.
Low frequency = 1200kHz/12/LD
where LD is the Low register value.
This translates to:
DTMF HI REG = 200000 / HI REG Hz and
DTMF LO REG = 100000 / LO REG Hz

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VOX

Voice Operated Transmission, with an attack (C3), and decay (T = C3R1) set with external components.

Companding

The audio signal's dynamic range is compressed before transmission, and expanded after reception.

3.2.3.4. NE5751

The NE5751 is a CMOS IC. It integrates a de-emphasis, a pre-emphasis, a deviation limiter, and a DTMF generator. It also provides programmable digital switches to control the signal path (audio mute), and a digital volume control.

Pre-emphasis/de-emphasis: In order to improve FM receiver sensitivity and maintain good S/N for higher audio tones, the baseband audio signal's higher frequency components are amplified before transmission (pre-emphasis), and attenuated after reception (de-emphasis).

Deviation limiter: It guarantees a maximum audio signal (voice) deviation of $\pm$12kHz.

DTMF generator: Two DTMF registers are accessible form the I^{2}C bus: High tone and Low tone DTMF registers. The High and Low frequency tones are computed as follows:

High frequency = 1200kHz/6/HD
where HD is the High register value.

Low frequency = 1200kHz/12/LD
where LD is the Low register value.

This translates to:
DTMF HI REG = 200000 / HI REG Hz and

DTMF LO REG = 100000 / LO REG Hz

Table 3.0 Std DTMF Freq./Corresponding Values of DTMF HI/LO Registers

Number Dialed	High Freq.	Low Freq.	DTMF HI	DTMF LO
1	1209	697	A5	8F
2	1336	697	96	8F
3	1477	697	87	8F
4	1209	770	A5	82
5	1336	770	96	82
6	1477	770	87	82
7	1209	852	A5	75
8	1336	852	96	75
9	1447	852	87	75
0	1336	941	A5	6A
*	1209	941	96	6A
#	1477	941	87	6A

The register values quoted will not give exactly these frequencies. Note that single tones can also be generated by loading 0, 1, or 2 in the high frequency register.

3.2.3.5. Receiving Audio

The demodulated signal (AUDIO) produced by the NE605 circuit carries FM audio. It is fed to the NE5751 receiver input (Pin 17) where it is filtered by a 4th-order band-pass filter with a stop-band notch at 6kHz to reject the SAT signal. The resultant audio signal (300 - 3000Hz) is then de-emphasized with -6dB/Octave slope filter, over the higher frequency range, to compensate for the pre-emphasis function in the transmitter. The de-emphasized signal then goes to the NE5750 for expansion, to compensate for the compression in the transmitter. The recovered audio signal (expander output) comes back to the NE5751 into a digitally programmable attenuator circuit where the volume can be adjusted to 1 out of 16 levels, each with 2dB increments (level 0 = 0dB, level 15 = 32dB). Finally, the attenuated signal feeds an audio power amp on board the NE5750 which drives the speaker. The same signal is summed to the side tone coming from the microphone using an audio power amplifier which drives the earpiece (Figure 3.10a).

3.2.3.6. Transmitting Audio

The voice signal produced by the microphone is preamplified with a low noise, programmable gain preamplifier controlled by R7, on board the NE5750. The signal then feeds the noise cancellation circuit where gain is reduced by 10dB in the presence of background noise (or absence of speech). The resultant signal then enters the NE5751 at Pin 4 where it is filtered with a 4th-order 300 - 3000Hz band-pass filter. The filtered signal leaves the NE5751 to be compressed on the NE5750. The compressed signal leaves the NE5750 and enters the NE5751 at Pin 6 where it is pre-emphasized 6dB/Octave slope in the pass band; a limiter circuit guarantees a maximum frequency deviation of ±12kHz, and a 5th-order 3000Hz low-pass splatter filter controls the spectrum occupancy of the baseband signal to 3kHz (±15kHz from center frequency). Before leaving the NE5751, the signal is summed to DTMF signals, generated internally, and to the SAT signal coming from the DPROC. The summer output is then modulated inside the transmit Local Oscillator block before going to the transmit module (Figure 3.10a).

3.3. Data Path Description

3.3.1. Receiving Data/Audio

The incoming 800MHz RF modulated carrier through the Duplexer is mixed, using a single transistor circuit, with the receiver Local Oscillator to produce a 45MHz IF signal. This 45MHz modulated IF is then mixed down to 455kHz, filtered, and demodulated on board the NE605 (see 3.1.1.2). Only one of the two resultant demodulated signals from the NE605 goes to the APROC and DPROC for further filtering and separation into voice and data signals, respectively. The NE605 also provides a Received Signal Strength Indicator (RSSI). RSSI is routed to the ADC (Analog-to-Digital Converter) input of the main µcontroller which can determine, based on the quantized value of the RSSI, the best channel from which to receive.

The NE605 demodulated output provides a data signal (DEMODD) to the data processor (DPROC) for digital data recovery and error correction. The recovered data is presented to the µcontroller over a dedicated 2-wire bus (RX_{LINE} & RX_{CLK}). The controller then reads the data by clocking it out of the DPROC via RX_{CLK} and processes it as dictated by the AMPS/TACS specifications. The DEMODD data signal also goes to the APROC (NE/SA5751, Pin 17) where it is DEMPhesized, band-pass filtered to receive audio frequencies ranging from 300Hz to 3kHz, EXPANDed by the NE/SA5750, then sent to the earpiece.

3.3.2. Transmitting Data/Audio

Outgoing data frames are set up by the master µcontroller and sent to the DPROC over a dedicated 2-wire bus (TX_{LINE} & TX_{CLK}); the µcontroller clocks the data into the DPROC via TX_{CLK}. Refer to DPROC application note for transmitter link protocol [5]. The DPROC encodes the data into BCH and Manchester, converts it into an analog signal (DATA), and sends it to the APROC (NE/SA5751, Pin 24) transmit summer input. Speech signals coming from the microphone are fed into a noise cancellation circuit (NE/SA5750), band-pass filtered on the NE5751, then fed to the NE5750 for COMPression. The COMPressor output goes through the NE/SA5751 where it is PREMphasized and low-pass filtered, and goes out at Pin 26 to the transmit summer input.

The APROC NE/SA5751 summer output, Pin 23 (signal TXMOD), goes to the transmit local oscillator circuit where the signal is modulated, and then sent to the transmit module. For more information on Audio Processing refer to a paper by Ali Fotowat, et al [2].

3.4. LAYOUT

3.4.1. Layout and Shielding Techniques for Reducing Spurious Signals

The full-duplex feature of the cellular phone and the requirement for light and small phones, makes the layout very critical. Several paths for receiver blockage and instability do exist that have to be identified and eliminated. It should be made certain, however, that the gain blocks are designed with enough gain (e.g., for an FM IF chip with -106dBm sensitivity, at least 10dB of noise free gain is required in the front-end and the first IF). In the case of the NE605, however, with better than -116dBm sensitivity already at the IF, the problem is reduced to calculating the noise figures and having just enough gain to overcome the front-end noise as it was calculated before. In either case, the final IF spectrum of a "noise" or "gain" limited receiver looks deceptively symmetric and clean; the only problem being not enough sensitivity. After these problems have been solved, the spurious signals start to show up in the final IF. There are several sources of these spurious signals that we have determined through experimentation and during the course of our design:

- The first and most important is the leakage of the transmitter power or its sub-harmonics into the receiver section. This can be in the form of radiated or conducted spurious emission. The former can be eliminated by making certain that the whole phone package is made of metal or that at least the receiver section is totally shielded from the antenna. The latter can only be eliminated by the duplexer and the transmit-receive filters. Paths through the power supply should be eliminated by filtering the supply and using separate regulators for the RF power amp and the receiver.

- The second important source of spurious signals is due to the receiver synthesizer and mixing products. Any phase noise or low frequency signal riding on the VCO input will end up in the IF pass-band. Too much LO level (overdrive of the first mixer) will also mix with other available spurs, causing many unwanted in-band spurs.

- The third type of spur is due to the 2nd IF chip. Although the IF frequency is 455kHz, most of the gains are here and a poorly designed 2nd IF PC board layout can cause multiple loops. The 455kHz IF, although not a mixer, can reproduce the 45MHz IF component by mixing the LO and noise due to the nonlinearity of the amplification in limiters.

- Finally, spurs can be generated by the μcontroller communication with the EPROM software, or other logic circuits (like the extra RS-232 interface used in our phone for demonstration purposes) or the dividers that divide the VTCXO frequency. All three circuits generated 455kHz IF band spurs. Although the clock frequencies in these sections are around 10MHz, the random pattern of data transmission can also generate strong enough non-harmonic spurs as high as 80 or 90MHz that can block the first IF for low levels, as well.

There are several techniques for detecting the presence of spurs. The easiest one is to check the DC voltage in the received signal strength indicator. RSSI in the NE605 has a wide dynamic range and does not distinguish between signals actually coming from the antenna or spurs looping in the receiver. Consequently, as the signal from the antenna weakens, the RSSI curve drops logarithmically, making a small (but distinguishable) dip, but remains flat at the RSSI level of the spurs, instead of going down to 0.5V or lower (depending on the front-end gain), which is the case in the absence of such spurs. The second method is to use a low capacitance high impedance probe to look at the final 455kHz IF output on a spectrum analyzer. With no modulation and large RF signals (e.g., -80dBm), the rough shape of IF filters will be observable. As the RF input decreases, the noise level increases correspondingly and, eventually, the spurs will show up in the final IF. As long as the carrier level is a couple of dB above the spurs, the receiver seems to behave normally due to the FM capture effect. As the RF input becomes comparable or less than the spurs (as seen in the final IF), the receiver will be captured by the spur and the audio output will exhibit a lot of noise. To find out the source of each spur, one has to eliminate the sources by going back through the receiver stages. For example, if shorting the final 455kHz input to ground eliminates a spur, it is a sign that a simple 2nd IF loop is present. In this case, improvement in the grounding around the IF amps and use of low ESR tantalum supply bypass capacitors can help solve the problem. The same procedure is used in stopping or reducing the 2nd LO level, and/or shorting the 45MHz input of the FM/IF chip to ground. If a spur is eliminated this way, it is a sign of a 45MHz loop. The solution in this case, ironically, may be to reduce the gain. This can be done easily after the first 455kHz IF limiter without degrading the system noise figure. Of course, too much reduction in gain can also reduce sensitivity. As a result, the optimum reduction in gain which will eliminate the spur may be of the order of only 1 or 2dB, as we observed in our design. Disabling or reducing the 1st LO level is the next thing to try in the same manner as above. This procedure will identify the place and the frequency at which the spurs enter the receiver. Finally, by eliminating other sources of noise, like turning off the μprocessor or disconnecting various voltage regulators, the source of the fourth type of spurious signals can be systematically identified and eliminated.

The layout, shown in Figure 3.11, is divided into two sections: the top portion is the RF section, and the bottom portion consists of the μcontroller, Audio, and baseband signal processing. The transmitter and receiver stages use different voltage regulators, and have also been separated as much as possible. The VTCXO is placed between the transmit and receive synthesizers. In the baseband portion, the APROC chips are placed close to the modulator synthesizer to minimize pick-up on the modulation input. The positioning of the μcontroller and EPROM could be improved by placing them further away from the FM IF section. The current positioning required shielding of the FM IF chip.

Finally, each block was separated from the others by a grounded strip with many feedthrough holes. This allowed us to shield different parts of the board after we had eliminated many of the more obvious spurious signals, and helped in finding more potentially hazardous ones. Table 3.1 shows the measurements on sensitivity with various sections shielded. It is obvious that the shielding of the IF section seems to have had the most effect.

Table 6. 1. Receiver Sensitivity Measurement Based on Shielding

Shielding on:	Receiver sensitivity
Front-end	-115dBm
2nd IF	-116dBm
Receive synthesizer	-115dBm
TCXO/Divider	-116dBm
Transmit synthesizer	-115dBm
Microcontroller/EPROM	-115dBm

Finally, comparison of our board with other existing phones of similar size shows a reduction from a 4 layer board to a two layer board, a 50% reduction in the number of ICs, and a 75% reduction in the number of external components in addition to minimum shielding.

REFERENCES:

1. "The I²C Bus Specification", order code 9398-358-10011, Signetics, September 1988
2. "Audio Processing For Cellular Radio or High Performance Transceivers", proceedings of RF Technology Expo, February 1989, A. Fotowat, S. Navid, L. Engh.
3. "EIA Interim Standard, Recommended Minimum Standards for 800-MHz Cellular Subscriber Units", EIA/IS-19-B, May 1988.
4. "An Integrated Chip Set for Cellular Mobile Telephones", Proceedings RF Expo West, 1989, T.G.R. Hall, P.J. Hart.
5. " The UMA1000T 'DPROC' Data Processor For Cellular Radio", T.G.R. Hall, August 31, 1989. Report No: MCO89005.

Table 6. 2. μController I/O Signals and Their Functions in the Cellular Application

Port #	Pin #	Signal Name	Description
0	50-57	AD0-AD7	Data bus and low order address bus.
1	16	PWRDWN	Output. Power down control. It shuts off the power to the transmit LO circuit. It is active high: 1 = power down.
	17	HPDN	Output. Power down control. It powers down the APROC NE5750. IOt is active low: 0 = power down.
	18	TXCTRL	Open-drain. It enables/disables the transmit module. The μcontroller must disable transmission at the end of Conversation, or in the case of malfunction. It is also connected to DPROC which will disable transmission if a collision is detected during SYStem access state, and to APROC (NE5750) to implement VOX during Voice CHANnel state.
	19	BUSY	Input from DPROC. Indicates the status of the REverse Control Channel. It is used in the SYStem access state to control the number of access attempts.
	20, 21	RX_{CLK}, RX_{LINE}	A two-wire dedicated serial bus used to ship data from DPROC to the μcontroller. RX_{LINE} is input, RX_{CLK} is output. Four bytes of data are made available by the DPROC. RX_{LINE} is first pulled low, signaling to the μcontroller that data is available. the μcontroller responds by targeting RX_{CLK} and clocks data out of the DPROC.
	22, 23	SCL, SDA	I^2C bus clock and data signals, respectively. Please refer to appendix ii for description of the I^2C bus specification.
2	39-46	A8-A15	High order address bus.
3	24, 25	RXD, TXD	Receive and transmit signals for the on-board UART (Universal Asynchronous Receiver/Transmitter). They are connected via a MAX232 IC to the RS-232 connector of a dumb terminal.
	26, 27	TX_{LINE}, TX_{CLK}	Dedicated two-wire serial bus used to ship data from the μcontroller to DPROC. TX_{CLK} is output; TX_{LINE} is I/O. When the mcontroller needs to send data to DPROC it polls TX_{LINE}. TX_{LINE} in the high state indicates that DPROC is ready to receive it. Five bytes of data are sent to DPROC and will eventually be transmitted on the reverse access channel.
	28	TXHOLD	Output. Active high. It disables DPROC transmit buffer. It can be used to control message transmission.
	29	NRESET	Output. Active low. A pulse is generated to reset the DPROC.
4	7-14	KB0-KB7	I/O. They form a matrix for scanning the keypad.
5	1	RSSI	Input to ADC0. Received Signal Strength Indicator coming from NE605 is converted to digital. Selection of Best and 2nd Best of Dedicated, Page, or Access channels is done based on RSSI's digital value.
	62-68	ADC1-ADC7	Unused.
	4	PWM	Output of PWM0. Used to provide a voltage level to regulate power output of the transmit module. The output has a dty cycle for responding to one of the seven power levels.

Table 6. 3. DPROC I/O Signals and Their Functions in the Cellular Application

Pin #	Signal Name	Description
1		Analog ground.
2		Analog reference ground.
3	DEMODD	Input. Demodulated signal carrier data or audio from the NE605 circuit.
4	DATA	Output, to NE5751. Analog output providing Manchester encoding and filtered data signal, SAT, and Signaling Tone.
5	RACTRL	Open drain, connected to APROC (NE5751). Receiver audio control. While in VCHAN state, and a dotting sequence is detected indicating the arrival of a control message, the audio path to the earpiece (switch M2) is muted to prevent the user from hearing the the data burst.
6, 7, 16, 21		See DPROC specification.
8, 27	RX_{LINE}, RX_{CLK}	Two-wire serial bus used to ship received data words from DPROC to the µcontroller.
11	TACTRL	Open drain connected to APROC (NE5751). Transmit audio control. While in VCHAN state and data needs to be transmitted, the audio path (switch M1) is muted allowing only data path to the APROC summer input.
15, 18	TX_{LINE}, TX_{CLK}	Two-wire serial bus used to ship data words to be transmitted from the µcontroller to DPROC.
17	TXHOLD	Input, from µcontroller. It disables data words from going through the transmit path of the DPROC. The µcontroller may load the DPROC transmit buffer, but inhibit transmission until the BUSY signal changes to IDLE.
19	BUSY	Output, to µcontroller. Multiplexed with a data stream transmitted on FOCC is the BUSY/IDLE bit indicating the status of the reverse control channel. DPROC sets BUSY signal accordingly. It is used to determine whether a collision has occurred during transmission: if the channel becomes busy before 56 bits have been transmitted, or if channel does not become busy after 104 bits have been transmitted.
20	TXCTRL	Open drain disables transmit module. DPROC control over transmission is activated when a collision, as defined in EIA/IS-3-D (also, on page 13 of DPROC spec, items 9, 10 of Access Attempt Procedure), is detected (see BUSY).
24, 25	SDA, SCL	I^2C bus data and clock signals, respectively. For a description of I^2C bus refere to Appendix ii. DPROC I^2C address = 0D8h

Table 6. 4. Meeting Receiver Specifications

AMPS Standards		
EIA/IS-19-B	**Specification**	**Met By**
2.2.2.1.3	Audio Frequency Response	APROC
2.2.2.2.3	Audio Muting	APROC OR NE605
2.2.2.3.3	expander Tracking	NE5750
2.2.2.4.3	Hum and Noise S/N	NE605
2.2.2.5.3	Audio Distortion	APROC AND NE605
2.2.2.6.3	Audio Sound Level	SPEAKER, NE5750
2.2.3.2.3	Bad SAT Report	DPROC
2.3.1.3	Sensitivity	FRONT-END AND NE605
2.3.2.3	Adjacent Channel Selectivity	MURATA FILTERS
2.3.3.3	Intermods	FRONT-END
2.3.4.3	Spurious Response Interference	SYSTEM DESIGN
2.3.5.3	Bit-Error-Rate	DPROC, NE605
2.4.3	Conducted Spurious Emission	LAYOUT, FILTERING
2.5.3	Radiated Spurious Power	PACKAGING AND FCC
2.6.3	RSSI Linearity	NE605

Table 6. 5. Meeting Transmitter Specifications

AMPS Standards		
EIA/IS-19-B	**Specification**	**Met By**
3.1.2.3	Frequency Stability	TCXO, UMA1014
3.1.3.3	Carrier Switching Time	RF Power Module
3.1.4.3	Channel Switching Time	UMA1014
3.2.1.3	RF Power Output Levels	Power Mod, PWM Cal.
3.2.2.3	Switching Time Between Power Levels	Power Leveling Loop
3.2.3.3	Carrier-On State	RF Power Module and Driver
3.3.1.3	Modulation Stability	APROC
3.3.2.1.3	Compressor Tracking	NE5750
3.3.2.2.3	Transmit Frequency Response	NE5751
3.3.2.3.3	Inst. Peak Deviation	NE5751
3.3.2.4.3	Audio Muting	APROC
3.3.2.5.3	Transmit Audio Sensitivity	Microphone, NE5750
3.3.3.3	Wideband Data	DPROC
3.3.4.3	SAT Deviation and Phase Error	DPROC
3.3.5.3	ST Frequency and Deviation	DPROC and 5751
3.3.6.3	FM Hum and Noise	NE5750, UMA1014, VCO
3.3.7.3	Residual AM	Synthesizer and RF Amp
3.3.8.3	Modulation Distortion and Noise	APROC
3.4.1.3	Spectrum Noise Suppression	APROC, Filtering, Shielding
3.4.2.3	Conducted Spurious Emissions	Duplexer, RF Power Mod
3.4.3.3	Radiated Spurious Emissions	Shielding
3.5.3	Crosstalk (Audio)	APROC, Packaging
4.	Environmental	Ruggedness
EIA/IS-3-D		
	CELLULAR SYSTEM MOBILE STATION - LAND STATION COMPATIBILITY SPECIFICATION	Signetics AMPS Software

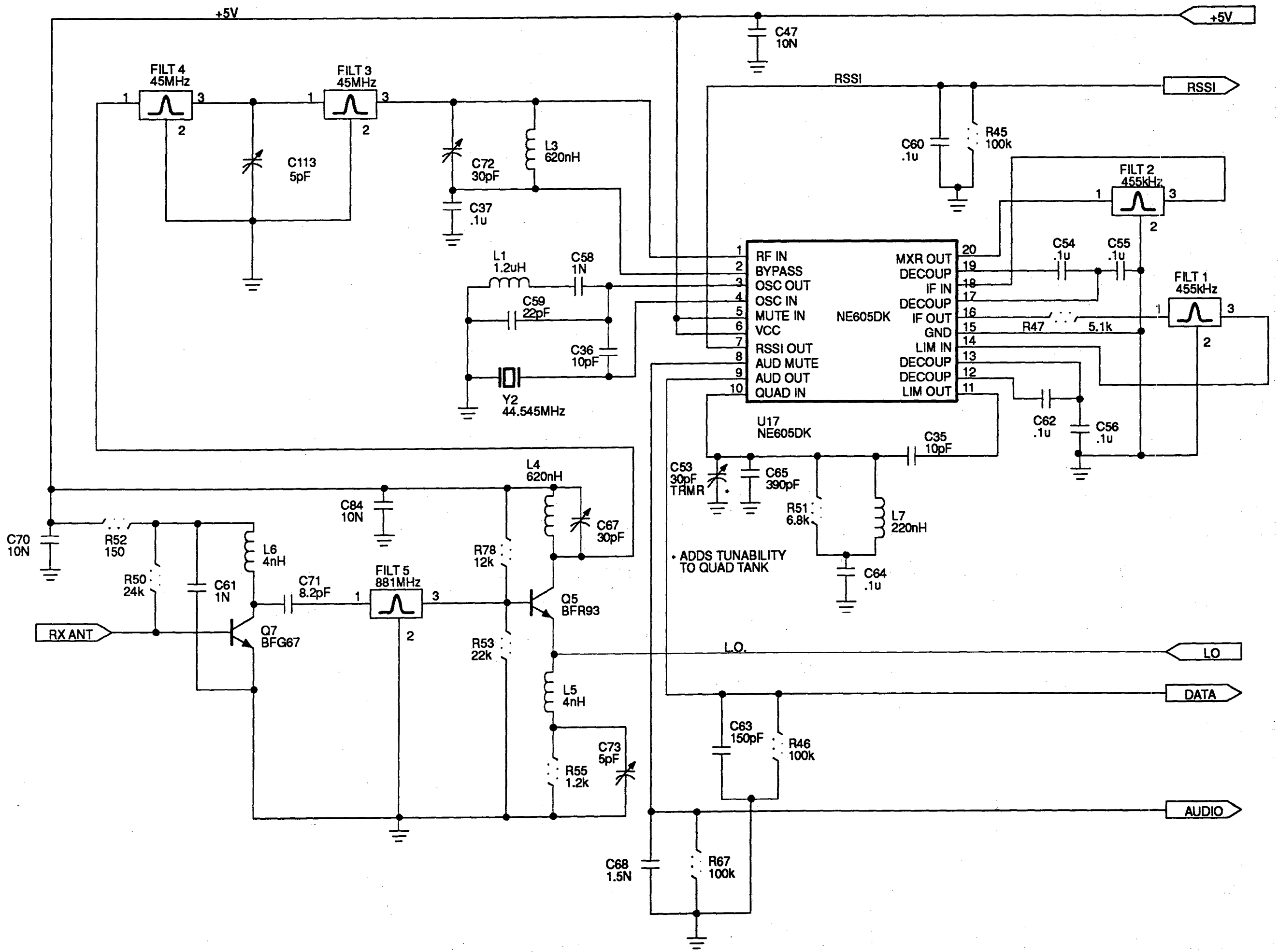

Figure 3.1 First IF, Second IF and Demodulation Circuit

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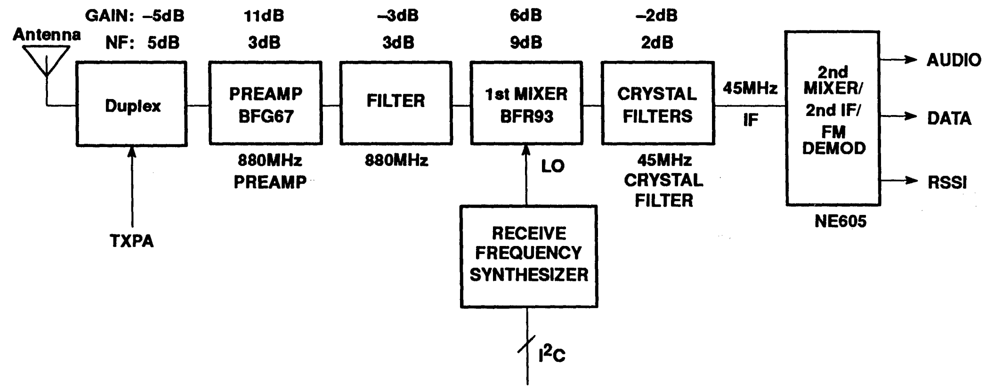


Figure 3.2 Front-End Gains and Noise Figures

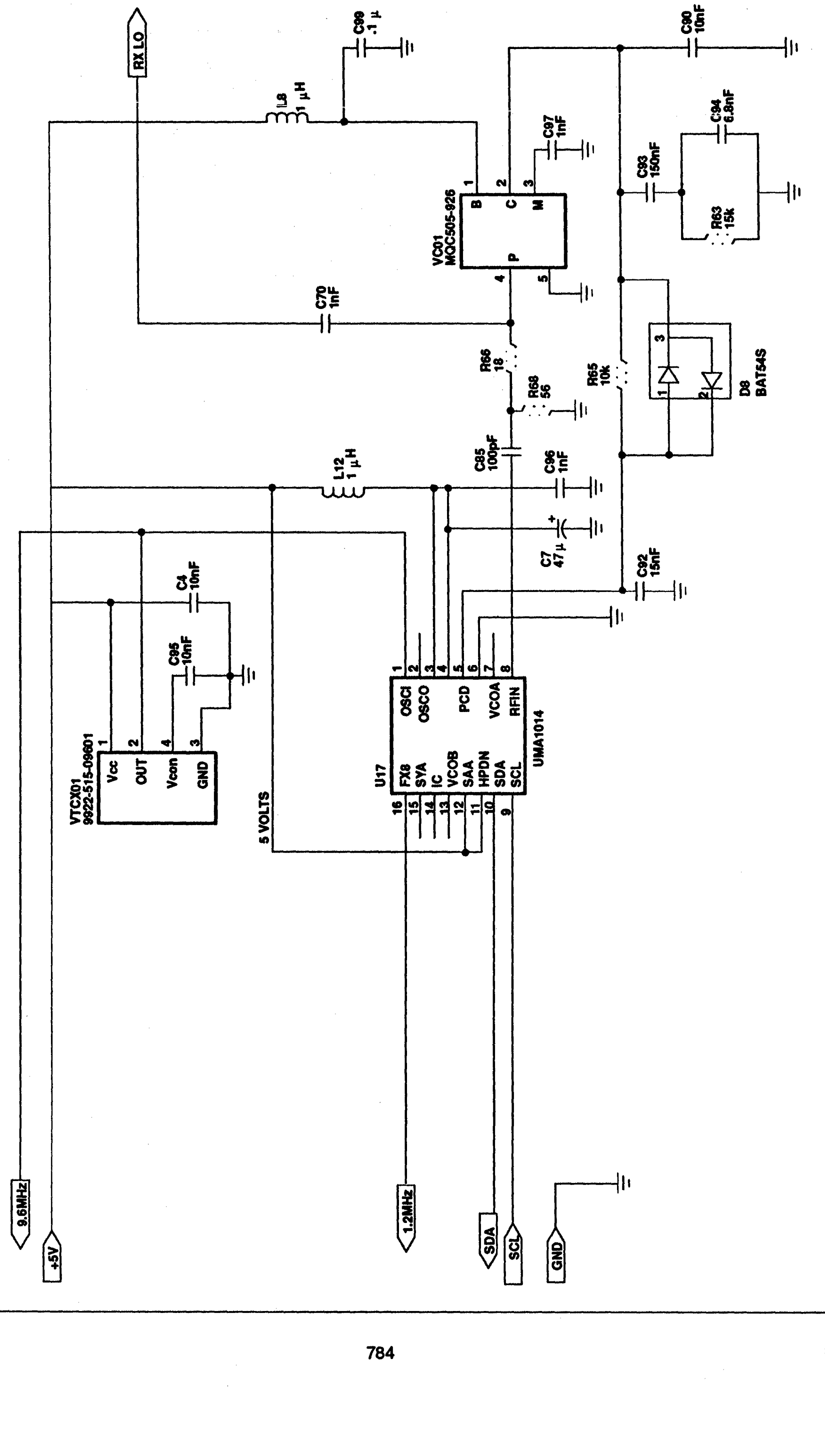


Figure 3.3 Receive Synthesizer

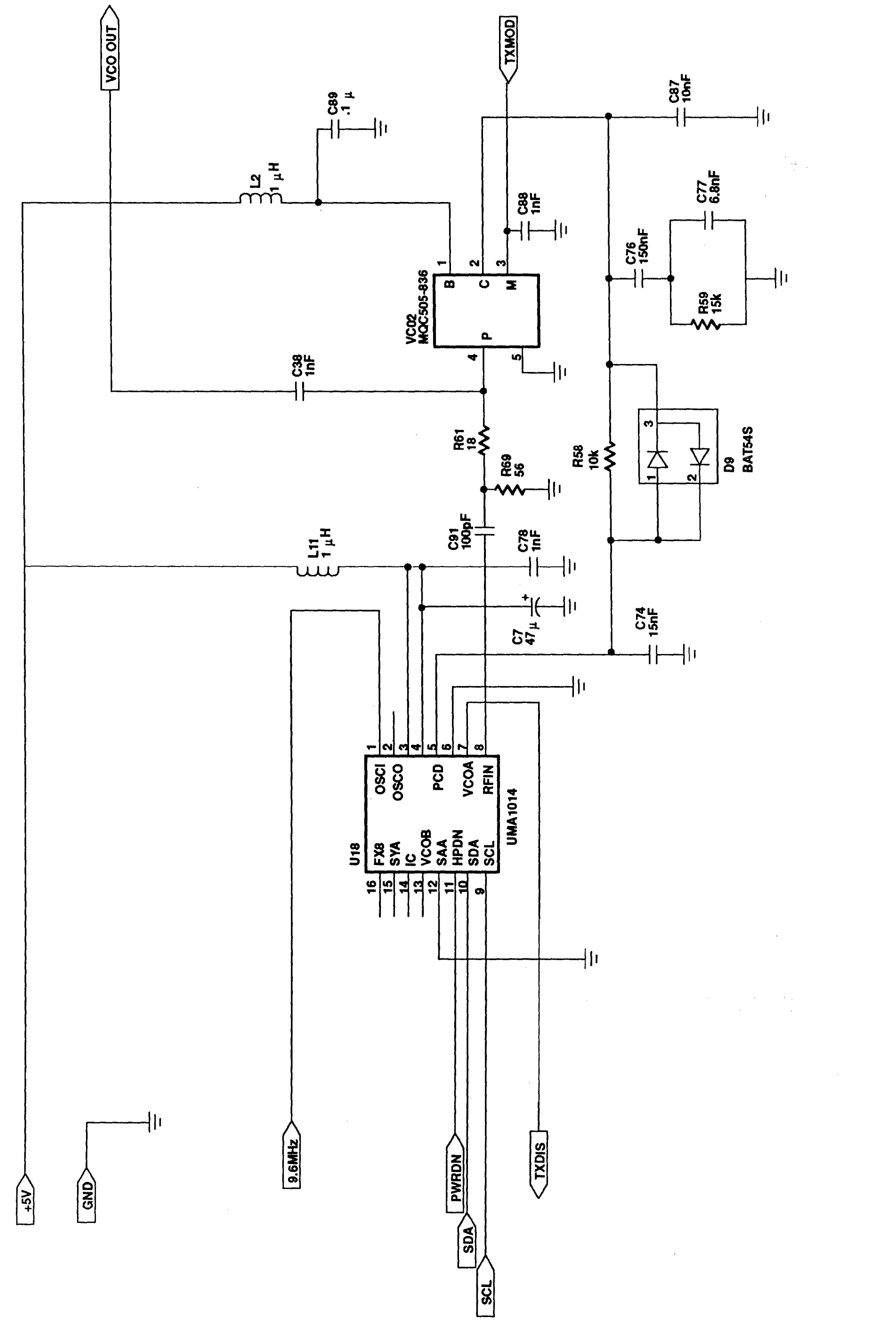


Figure 3.4 Transmit Synthesizer

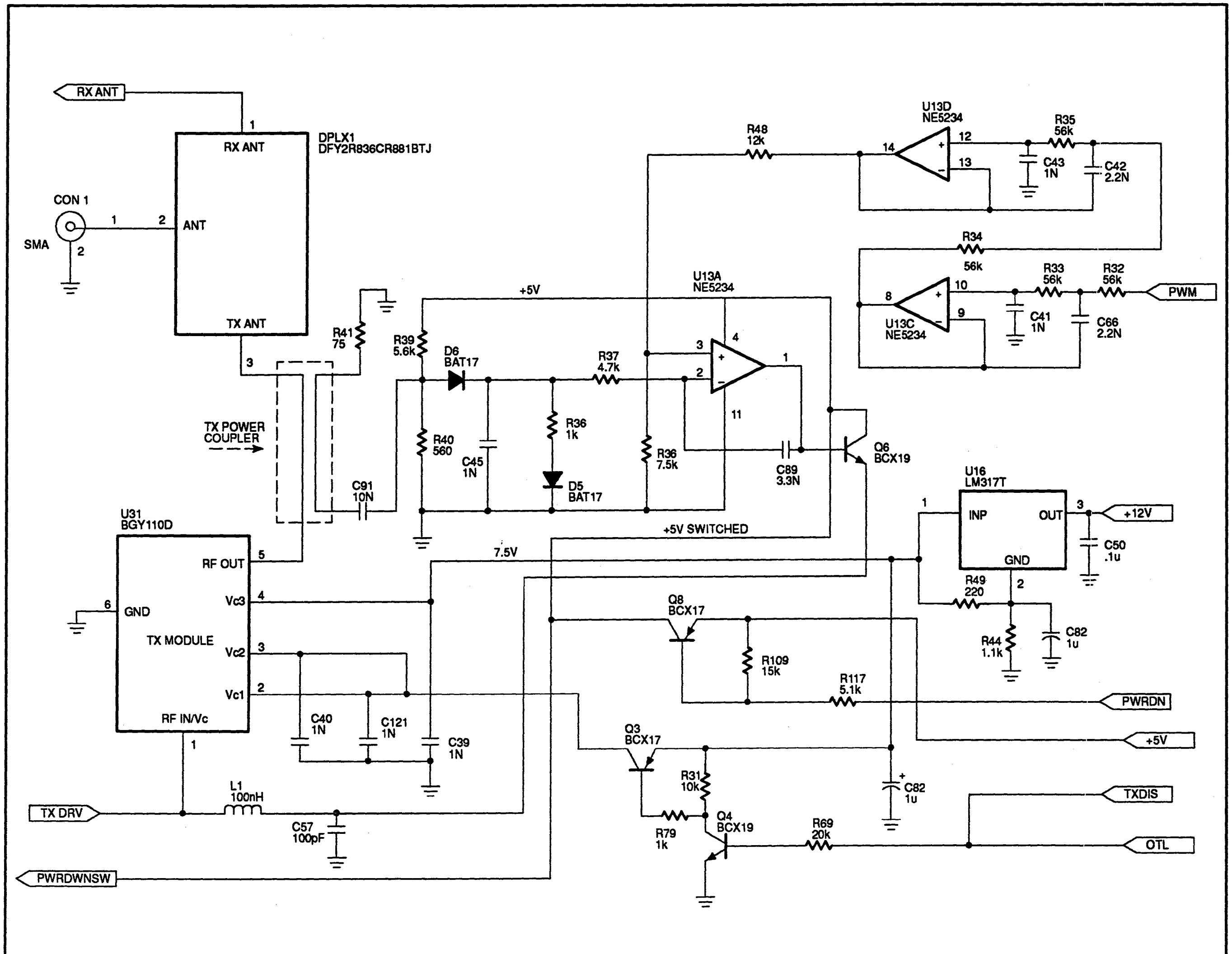


Figure 3.5 Transmit Module and Power Control

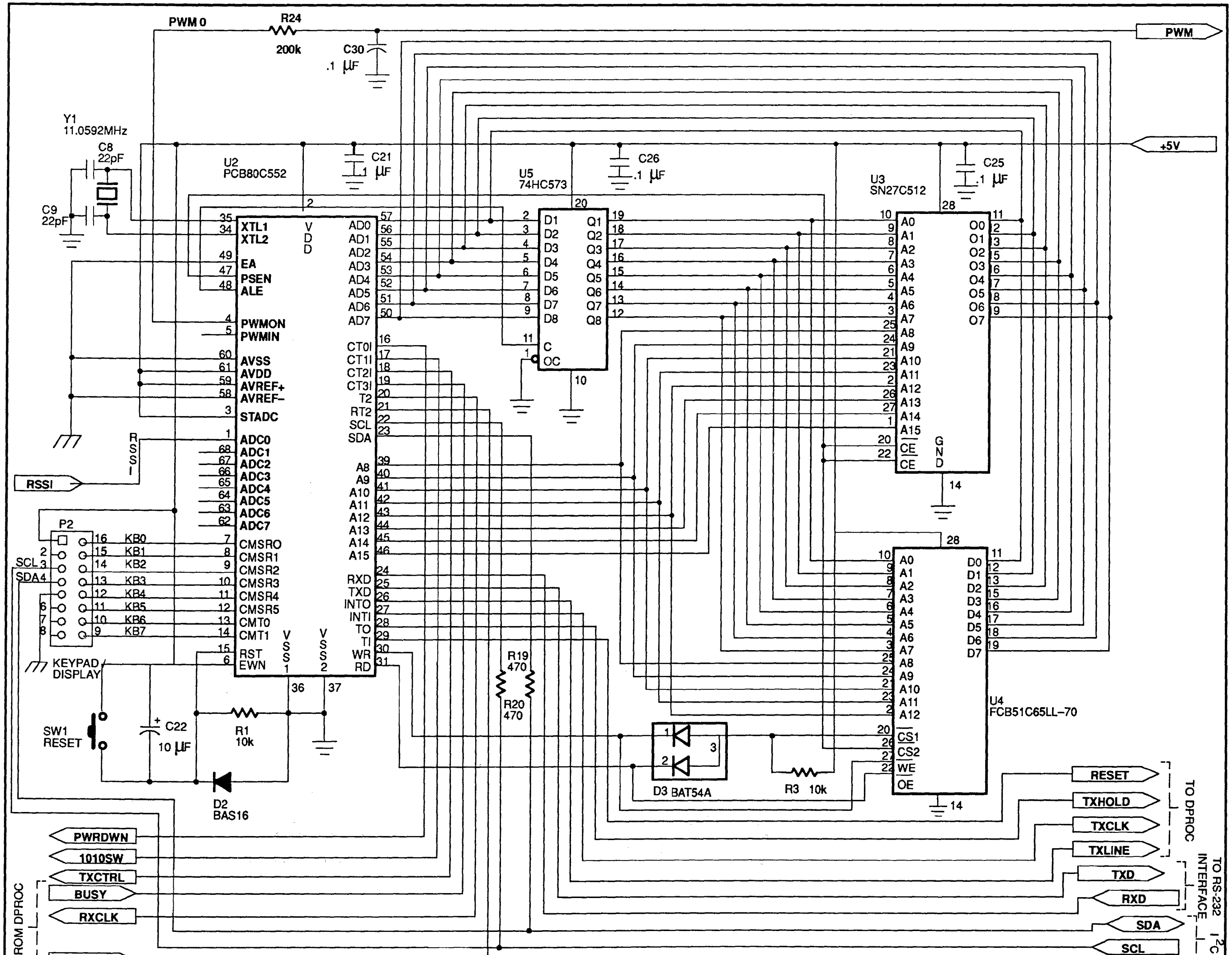


Figure 3.6 Logic and Program Control

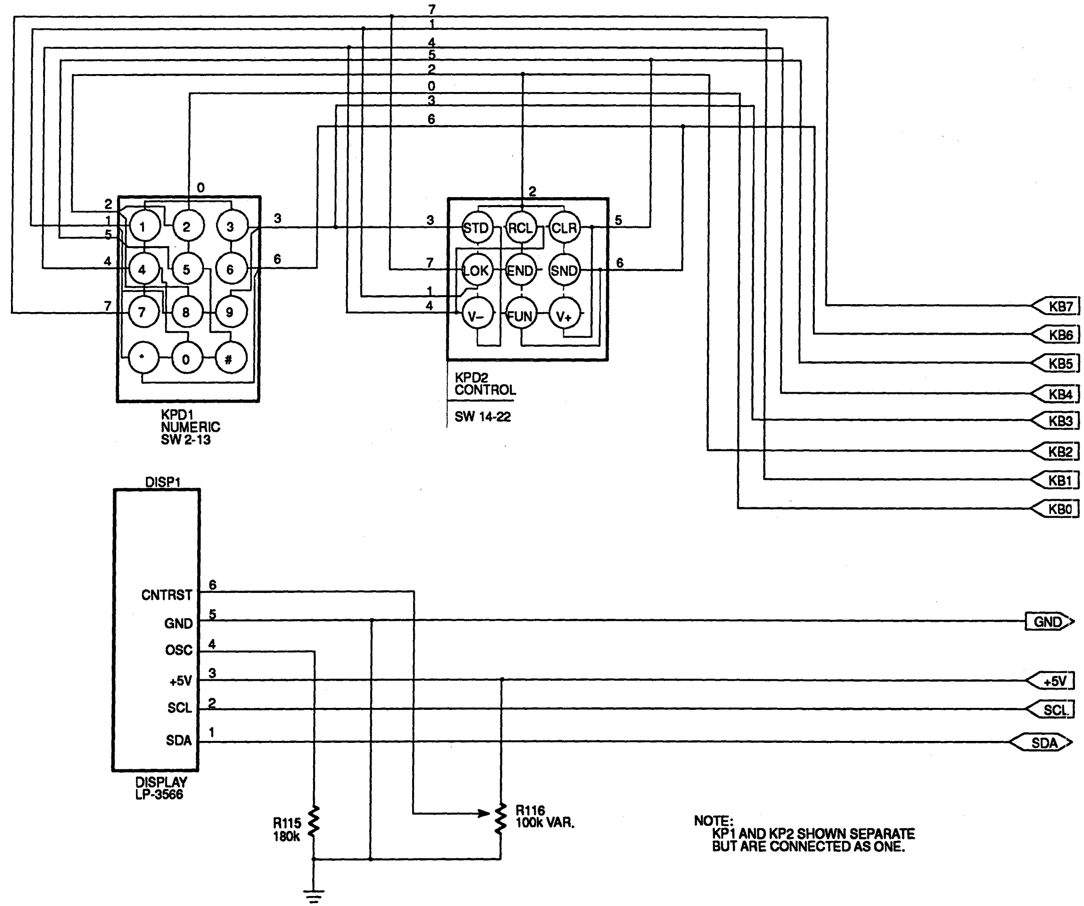


Figure 3.7 Keypad and Display

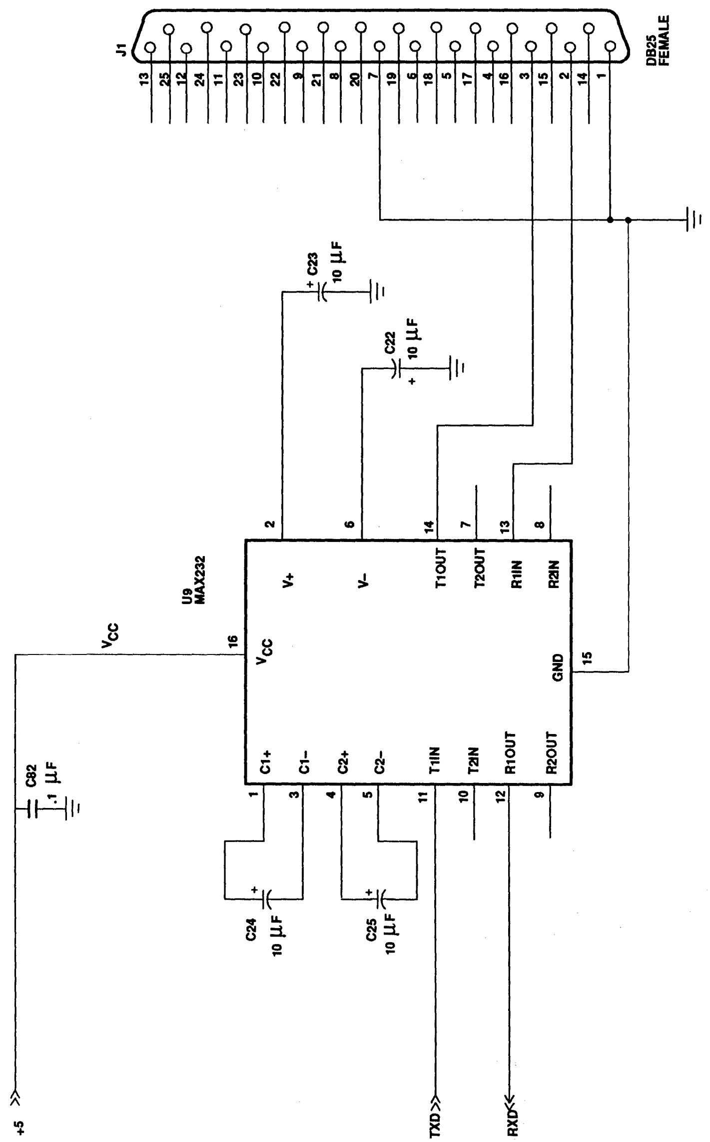


Figure 3.8 MAX–232 with DB–25 Connector

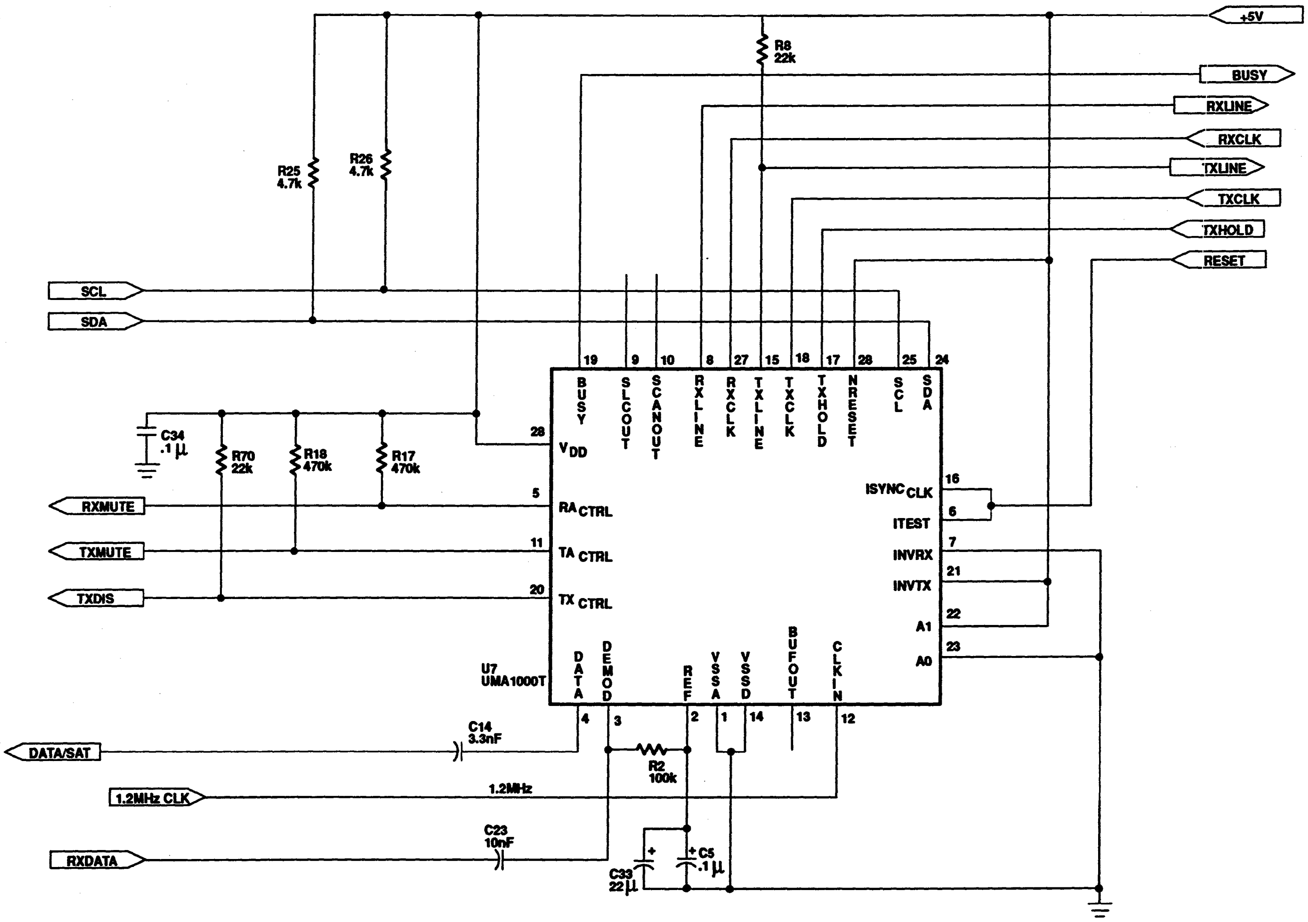


Figure 3.9 Data Processing Circuit

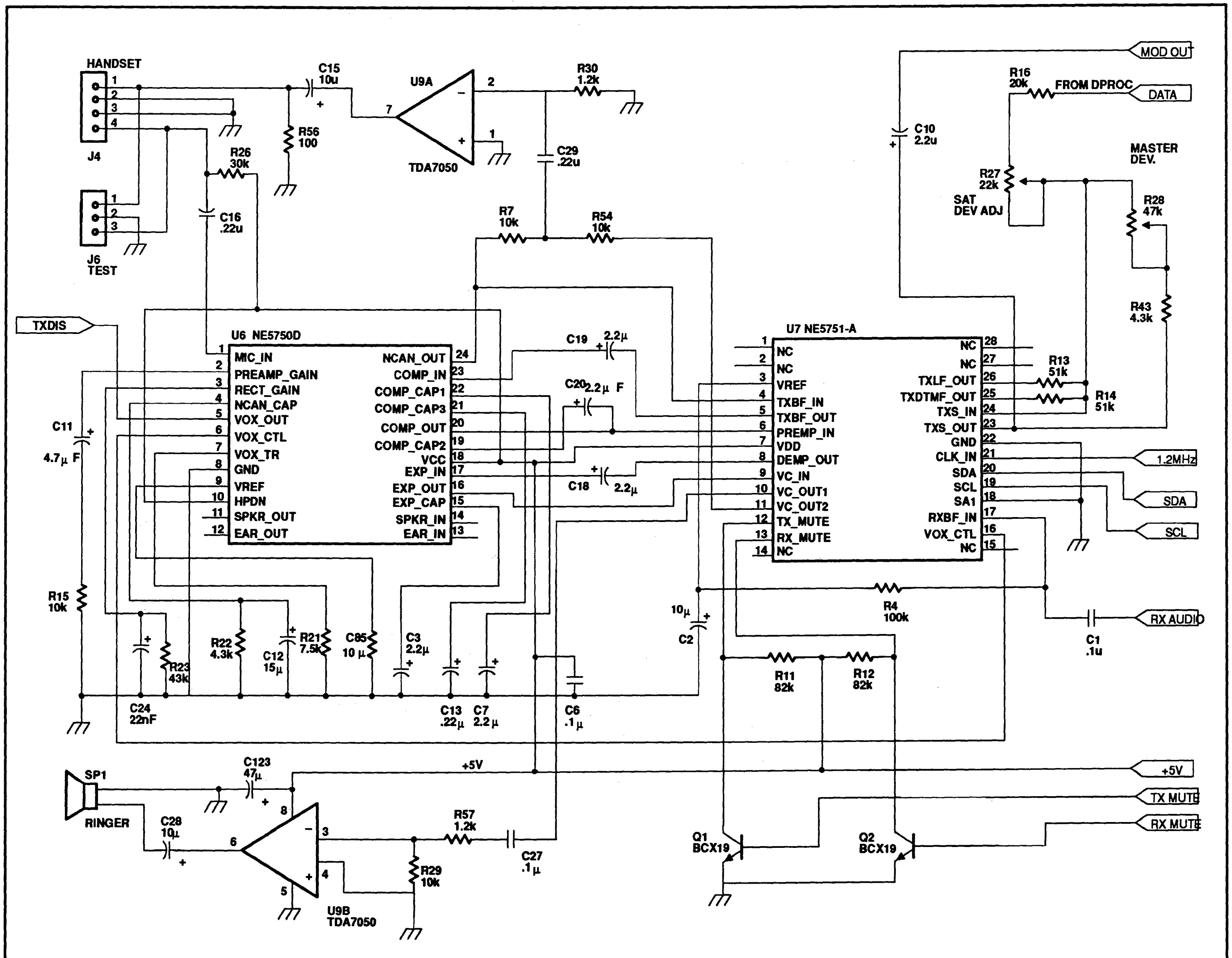
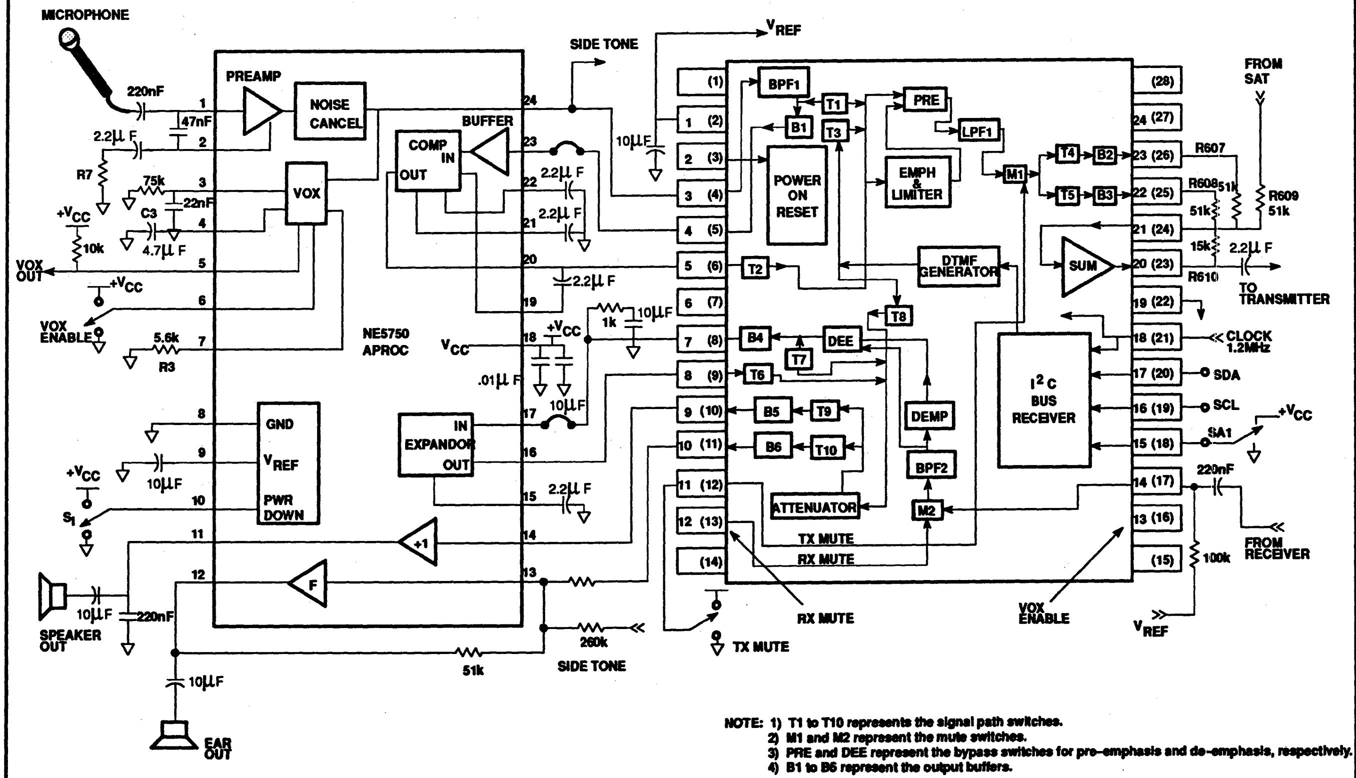


Figure 3.10 Audio Processing Circuit



NOTE: 1) T1 to T10 represents the signal path switches.
2) M1 and M2 represent the mute switches.
3) PRE and DEE represent the bypass switches for pre-emphasis and de-emphasis, respectively.
4) B1 to B6 represent the output buffers.

Figure 3.10A NE5750/NE5751 Typical Aulo Processing Application for Cellular Radio

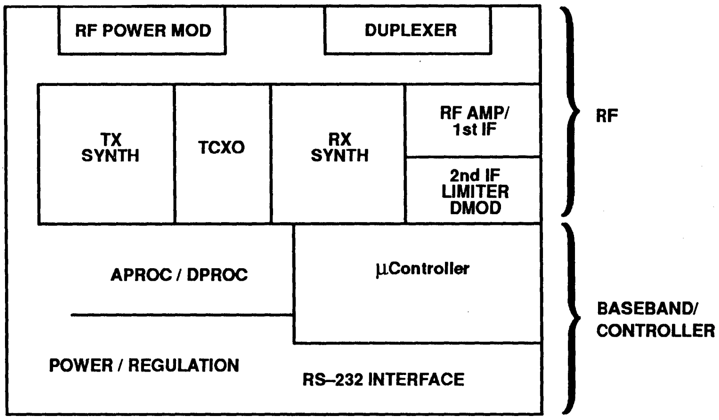


Figure 3.11 PCB Layout

SOFTWARE DESCRIPTION

4. OVERVIEW

The source code is developed using Intel's Programming Language for µController 8051 family (PLM51) and PLM51 compiler. The software was initially developed to implement TACS (Total Access Systems, United Kingdom) protocol. The AMPS parameters were extracted from the EIA IS-3-D specifications and added to the existing source code to result in a single piece of software that can run either AMPS or TACS standards. To select between the two standards, a compilation switch would have to be set accordingly, and ALL the high level software modules would have to be recompiled. An example of a compilation batch file is shown in the Appendix.

4.1. Cellular Phone Operation

From a protocol stand point, a cellular telephone operates as a state machine switching between four major states: INIT (INITialization), IDLE, SYS (SYStem access), and VCHAN (Voice CHANnel). Four software modules, with similar names but with .PLM extension, implement these states respectively, and are described in section 4.2.2, High Level Modules. Following is a description of the software's top level state diagram (Figure 4.1) linking these states together.

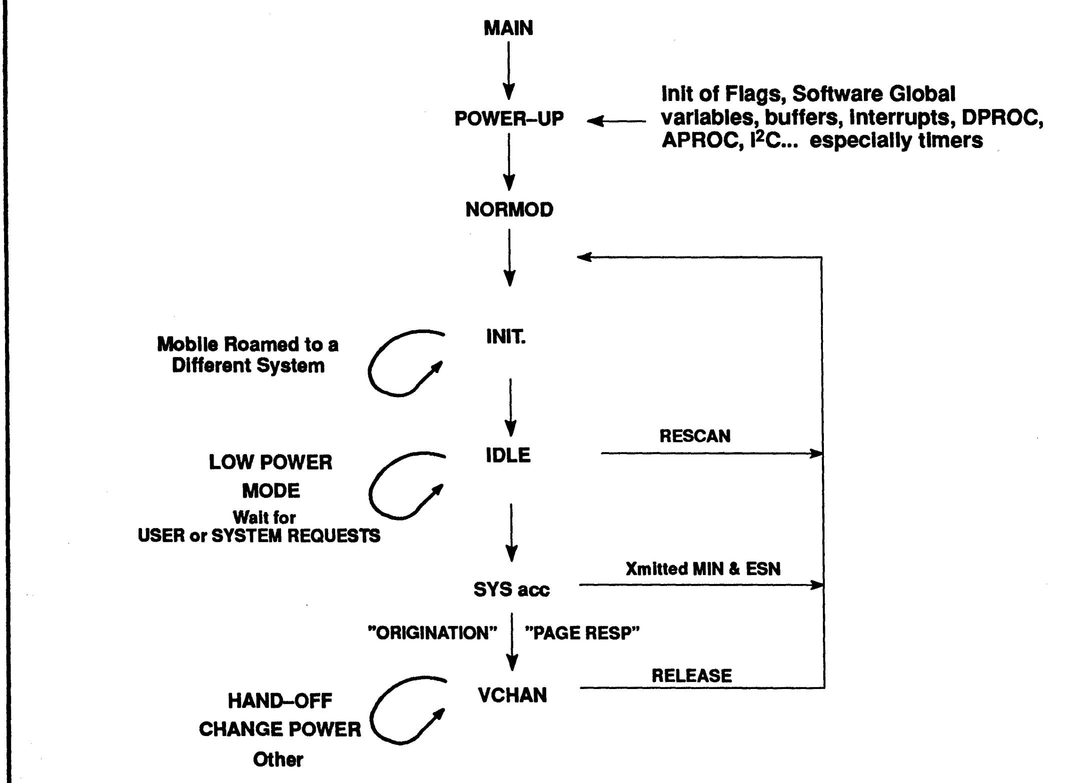


Figure 4.1. Main Program Structure

At hardware power up or system reset, the mobile executes POWRUP routine followed by NORMOD, the state machine handler, which then switches the phone state to the INIT state.

Figures 4.2 through 4.5 show a high level flowchart of the AMPS protocol/software. It is designed to give the reader a general idea of the activities of a cellular telephone. The major states are enclosed in rectangular boxes, and are interconnected with arrows leading to decisions (lozanges) and reasons for exiting any particular state. Each of the states is tagged with a reference number corresponding to a paragraph in the EIA/IS-3-D specification.

4.1.1. INIT

In the INIT state the mobile scans the Dedicated Control Channels spectrum and selects the two best channels based on the quantized value of the RSSI signal coming from the RF FRONT-END circuit (NE605).

The mobile then locks onto the best channel and reads and decodes overhead control messages (OHD) which are periodically transmitted by the cell site on the FOrward Control Channels(FOCC). Part of the OHD messages read are information to configure the Paging channels.

If unable to read any messages from best channel (mobile roamed away from nearest cell site), the mobile tries again by listening to the 2nd best channel. If the mobile fails again to read messages from the 2nd best channel, it repeats the INIT state and re-scans the Dedicated Control Channels spectrum. Otherwise, the mobile does the following:

Once configured, Paging Channels are scanned and OHD messages are decoded from best or 2nd best Page Channel, then compared to information already read from best or 2nd best Dedicated Control Channel (EIA 2.6.1.2.2). The need for such comparison arises due to the roaming feature of cellular. The user may have roamed out of his Home System between reading data from the Dedicated Control Channel and reading data from the Paging Channel. Upon verification, i.e. the mobile is still in Home System, the mobile switches to the IDLE state. Otherwise, the mobile has roamed to another system and the INIT state is re-executed.

4.1.2. IDLE

In the IDLE state the mobile listens to the Best or 2nd Best Page channel, as determined in the INIT state, and waits for requests from the User or from the system, i.e. the cell site. Requests from the system are sent in OverHeaD messages, such as REGISTRATION and RESCAN, and as mobile Station Control Messages, such as AUDIT order and PAGE order. User request can only be a call ORIGINATION, and is issued by pressing the SEND key. All requests, such as Registration, Audit, or Page (from the system) and Origination (from the user) require the mobile to transmit control information back to the system on the REverse access Control Channel (RECC) (see SYStem access below). Hence, following the receipt of a request, the mobile goes into SYStem access state. In the case of a RESCAN order, the mobile does not need to go to the SYStem access state; it simply loops back into the INITialization state. Note that OHD messages received over Page channel carry information to configure Access channels which are used in the system access state. During the IDLE state the mobile's transmitter and its Audio processing circuitry are not operational, so they can be powered down and reduce the phone's power consumption level.

4.1.3. SYS Access

The main task in the system access state is to seize a Reverse access Control Channel and transmit to the cell site the mobile Identification Number (MIN or Tel. #) followed by the mobile Electronic Serial Number (ESN), as per EIA 2.6.3.7 (Service Request). Criteria for reverse control channel seizure, like maximum number of seizure attempts and maximum number of channel busy indications, are communicated to the mobile over the best forward access control channel. The mobile starts the SYStem access state by scanning the set of access channels and selecting the 2 best channels, as done for dedicated and paging channel selection. The mobile then attempts to acquire a reverse access channel by first monitoring the Busy/Idle bit. If the channel is busy, the number of busy attempts is incremented. However, if the channel is not busy, and the mobile has started transmission of its MIN and ESN, but a collision is detected (by DPROC, which will abort the transmission), the number of seizure attempts is incremented. In either case of channel acquisition failure (due to Busy or collision), the mobile waits 200msec before attempting another channel seizure. If the number seizure attempts, or the number of busy occurrences, have been incremented to exceed a certain maximum, the mobile aborts SYStem access and goes to INIT state. Otherwise, if the system access timer times out before it was able to seize a REverse Control Channel, the mobile exits system access state and goes to INIT state. If the system access timer did not time out, channel seizure was successful, and MIN and ESN were transmitted, the mobile changes its internal state to Service Request (Figures 4.4 and 4.5) where a next step decision is made based on the reason for entering SYS access state (i.e., Registration, Audit, Page Response, or Origination).
If the mobile has entered the SYStem access state in response to an Audit order, the mobile goes to INIT state. (Audit is a way for the system to poll roaming mobiles to determine their geographic location on a cell boundary.)
If the mobile has entered the SYStem access state in response to a Registration indication, it waits for the cell site to acknowledge the receipt of MIN and ESN by sending a Registration Confirmation control message. The mobile, having received the confirmation message, will then update its Registration timestamp and return to INIT state. (Figure 4.5, Auto Reg Update, "success")
If system access is entered in response to Origination or Paging Request, the mobile waits for the cell site to assign it an initial voice channel, and then goes to the voice channel state. If system access timer times out before a voice channel is assigned, the mobile exits system access and goes to INIT state. Note that in response to a user originated call, the mobile transmits the dialed number in addition to transmitting MIN and ESN.

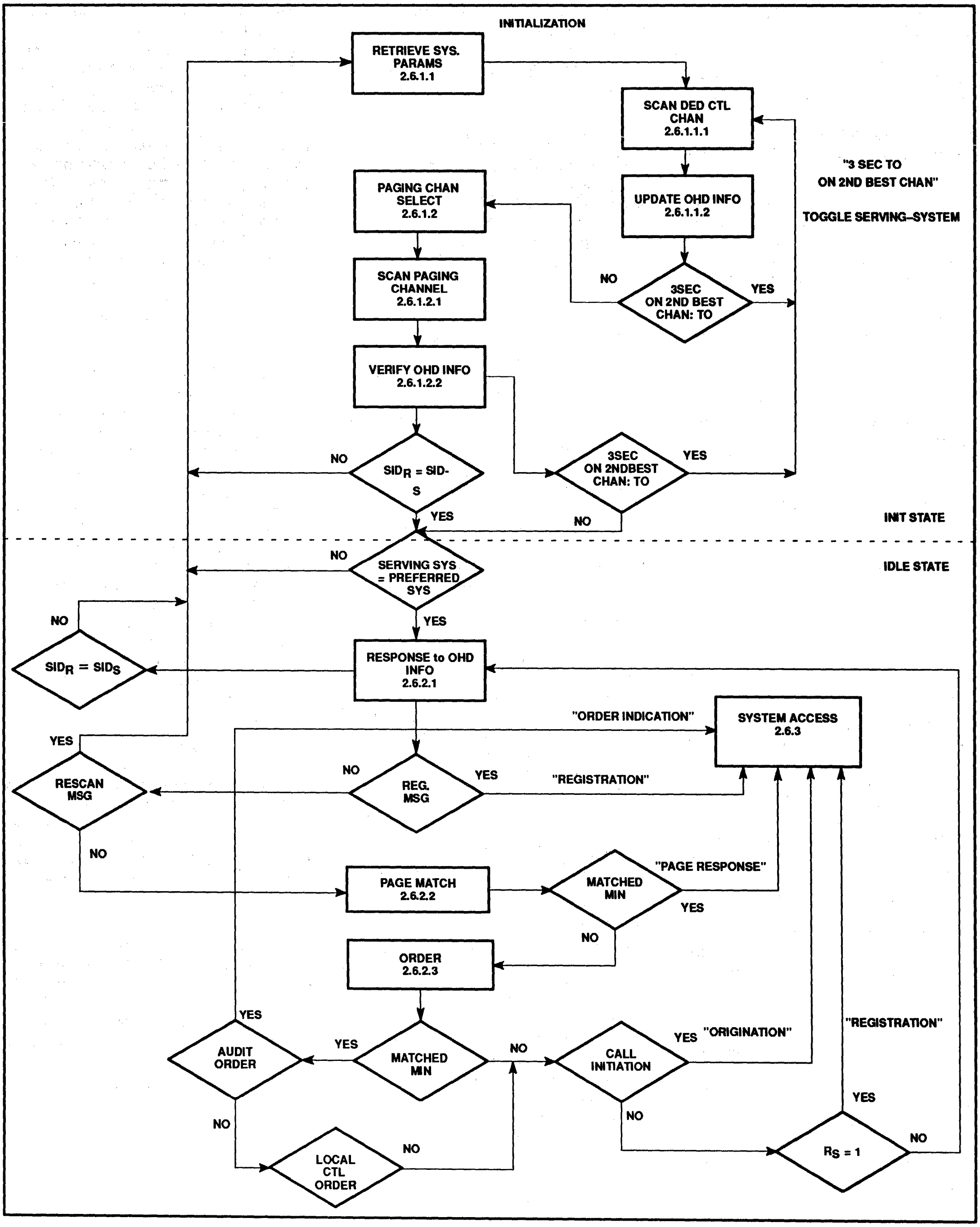
4.1.4. VCHAN

The mobile verifies that the initial voice channel assigned to it in SYStem access state is a valid channel, i.e., within the spectrum of voice channels, then tunes to it. Voice channel state consists of three sub-states: Conversation, Waiting for Order and Waiting for Answer. If the mobile enters VCHAN in response to a user originated call, it goes directly to Conversation sub-state and remains there until ordered by the cell site to change sub-states (or state, e.g. Release state). If the mobile enters VCHAN in response to system originated call (or paging), it goes to Wait for Order sub-state. In this sub-state the cell site sends an Alert message to the mobile ordering it to ring. The mobile rings and changes sub-state to Wait for Answer.

The user would answer the phone by pressing the SEND key, changing the mobile sub-state to Conversation. During sub-states the mobile can be handed off to another channel, or the power level changed, by order messages from the cell site. Receipt of cell site orders are acknowledged by the mobile by generating a 10kHz signaling tone with variable duration, based on the received message.

When the conversation is terminated, by the user pressing the END key or by a Release order from the cell site, the mobile turns on its signaling tone for 1.8sec to indicate to the cell site that it will release the voice channel and shut off its transmitter. The mobile then goes to INIT state.

This was an overall description on the cellular behavior. Following is a brief description of each of the software modules.


INITIALIZATION
RETRIEVE SYS. PARAMS 2.6.1.1
SCAN DED CTL CHAN 2.6.1.1.1
UPDATE OHD INFO 2.6.1.1.2
"3 SEC TO ON 2ND BEST CHAN"
TOGGLE SERVING–SYSTEM
PAGING CHAN SELECT 2.6.1.2
SCAN PAGING CHANNEL 2.6.1.2.1
NO
3SEC ON 2ND BEST CHAN: TO
YES
VERIFY OHD INFO 2.6.1.2.2
NO
SIDR = SID-S
3SEC ON 2NDBEST CHAN: TO
YES
YES
NO
INIT STATE
NO
SERVING SYS = PREFERRED SYS
IDLE STATE
NO
YES
SIDR = SIDS
RESPONSE to OHD INFO 2.6.2.1
"ORDER INDICATION"
SYSTEM ACCESS 2.6.3
YES
RESCAN MSG
NO
REG. MSG
YES
"REGISTRATION"
NO
PAGE MATCH 2.6.2.2
MATCHED MIN
"PAGE RESPONSE"
YES
NO
ORDER 2.6.2.3
YES
AUDIT ORDER
YES
MATCHED MIN
NO
CALL INITIATION
YES
"ORIGINATION"
"REGISTRATION"
YES
NO
NO
LOCAL CTL ORDER
NO
RS = 1
NO

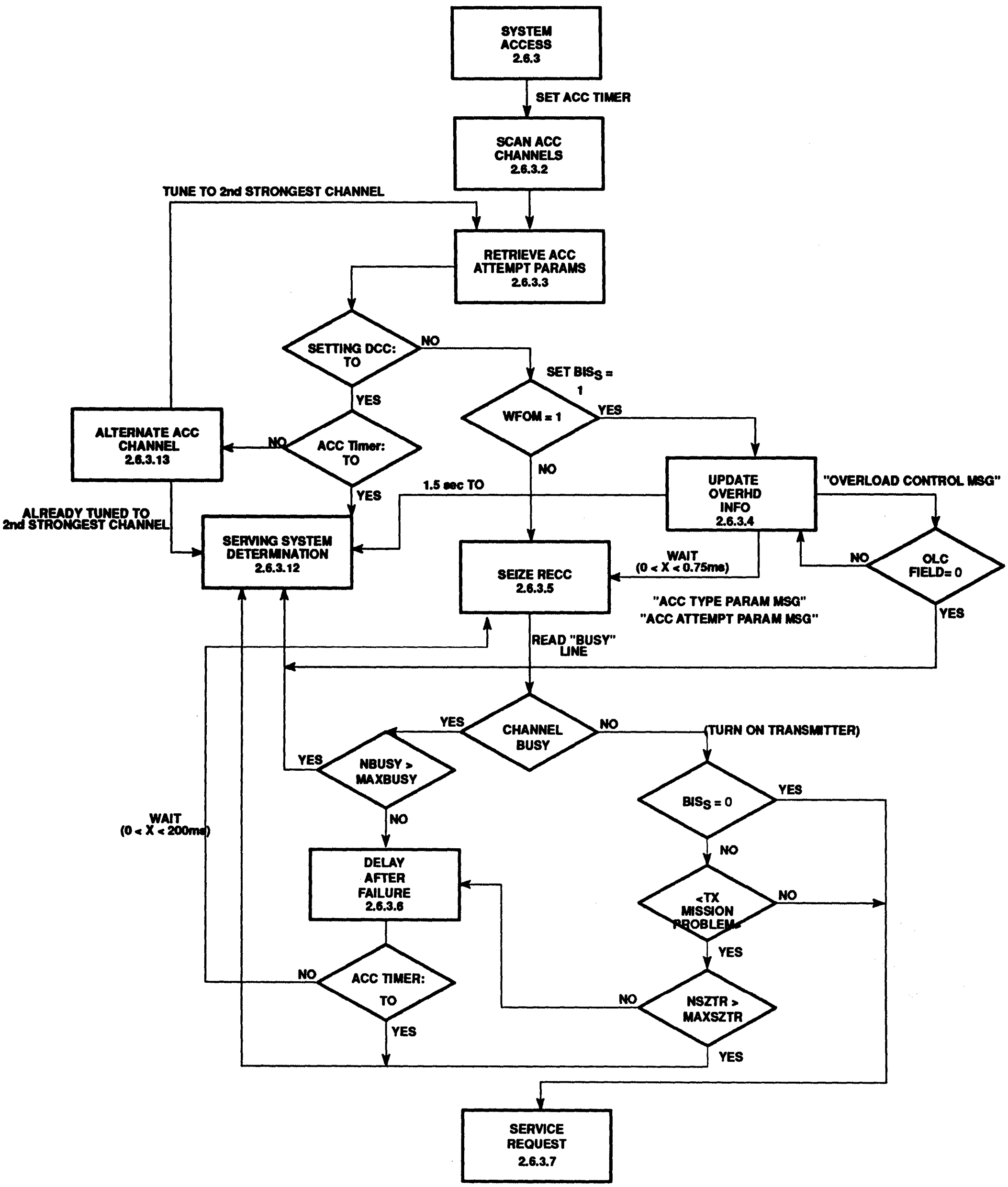


Figure 4.3. AMPS Flow Chart: System Access State

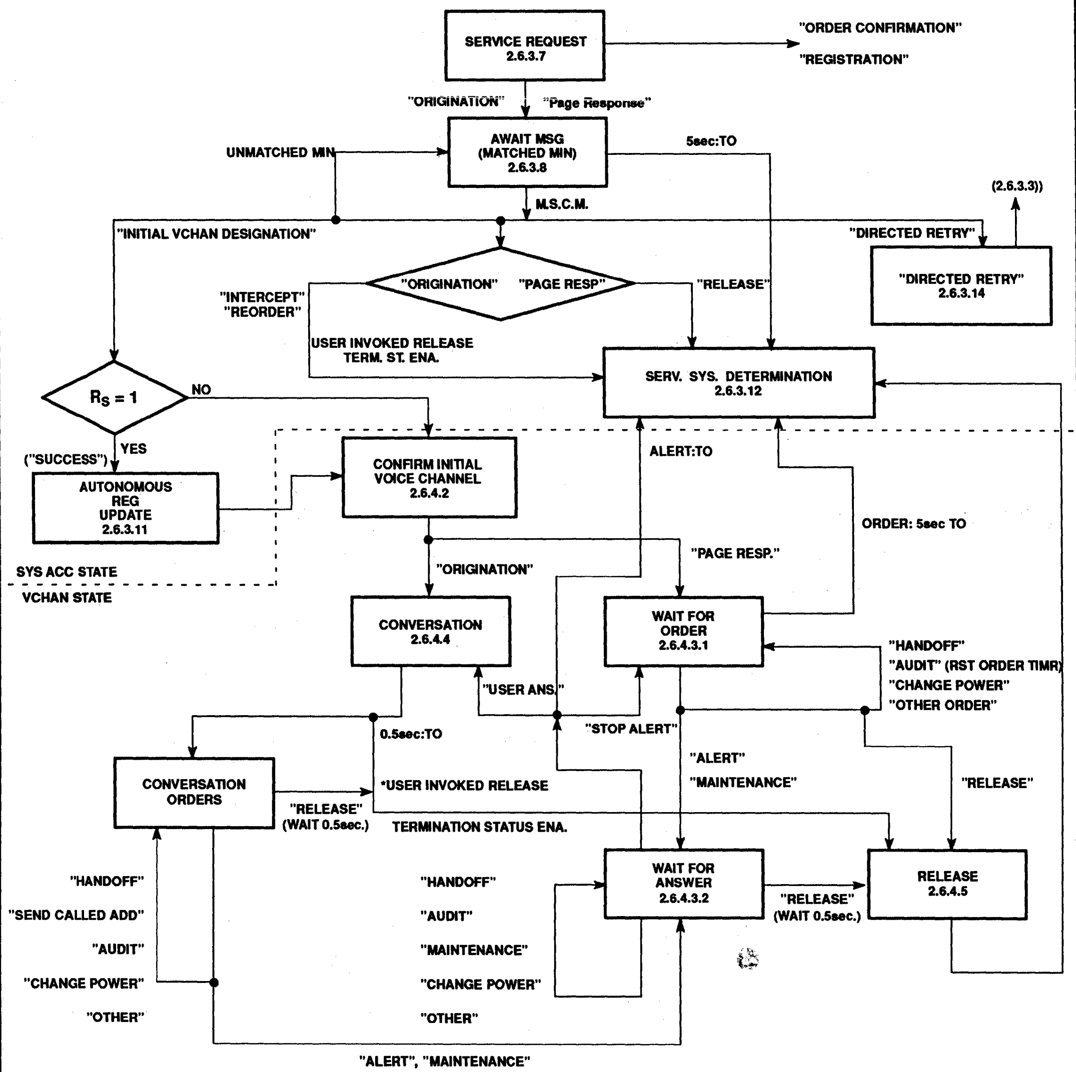


Figure 4.4. AMPS Flow Chart: System Access State (cont) and Voice Channel State

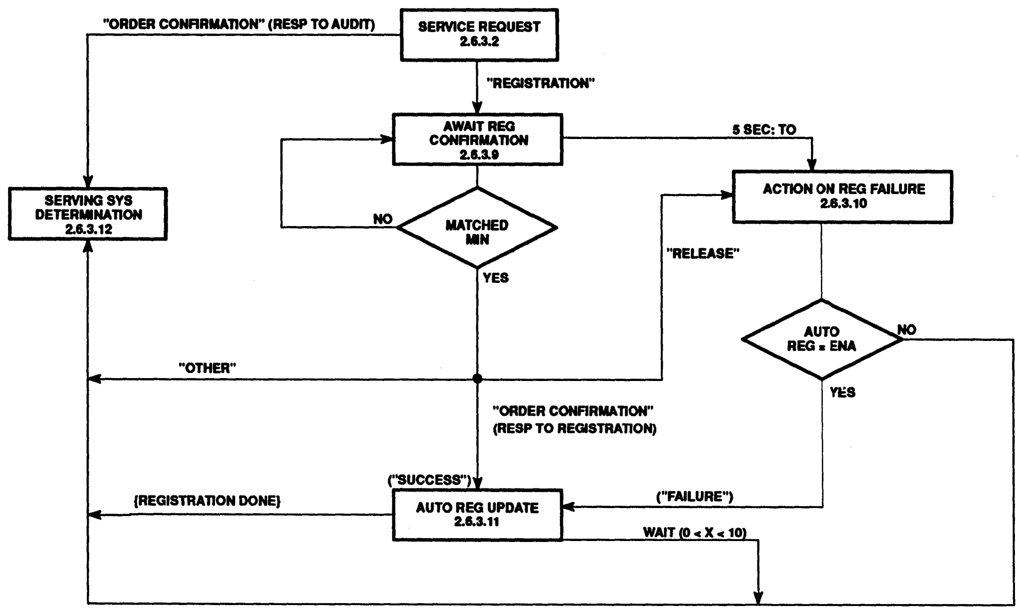


Figure 4.5. AMPS Flow Chart: System Access State (cont)

4.2. Setup & Implementation

The software modules can be divided into two categories:

1. Device driver modules.
2. High level, protocol dependent modules.

Device drivers are hardware dependent routines allowing the user control over the ICs using a high level language. High level modules are hardware independent routines and typically address the device drivers during normal operation. Following is the list of device drivers for the cellular chip set.

4.2.1. Device Drivers

ADCINT.PLM: This file programs the Analog-to-Digital Converter on board the µcontroller PCB80C552. The software waits until the ADC has converged before reading the digital value of the analog signal (typically RSSI).

DPROC.PLM: This file is temporary. It is a patch for the DPROC, version TN2682. It contains routines that perform message set-up and transmission, bypassing the DPROC transmit path. This is due to the fact that the TN2682 has a faulty Manchester encoder (see note in INTDAT.PLM below). Two other programs, described below, are developed to work in conjunction with this module: SENDI.ASM and INTERRUP.ASM.

IIC.PLM: This file programs the I^{2}C bus interface on board the µcontroller PCB80C552. The software performs retries in the case of no acknowledgment.

INTDAT.PLM: DPROC communication software with the system controller over the dedicated xmit/receive lines:

RX_{CLK}, RX_{LINE} DPROC -> µcontroller

TX_{CLK}, TX_{LINE} µcontroller -> DPROC

Hold µcontroller -> DPROC

Transmitter Routine

When the system controller needs to send data (typically MIN and ESN during a system access), it polls TX_{LINE}, indicating DPROC readiness to receive data. The transmit routine will not be called unless the TX_{LINE} has been released HIGH by the DPROC, signifying buffer Not busy, or readiness for receiving more data. The transmit routine picks up the data (5 bytes) from the data structure TX_MESSAGE(TX_WORD_NUMBER).TX_WRD_DATPRO, and transmits it serially on TX_{LINE} while toggling TX_{CLK} (data stable on positive edge). On the last rising edge of TX_{CLK}, DPROC will pull the TX_{LINE} LOW as an ACK/(buffer)BUSY signal. The transmitted word has the following format (e.g., word1).

BYTE 0								BYTE 1								BYTE 2								BYTE 3								BYTE 4								
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
E	S	D	D	F	NAWC			T	S	E	R	SCM				<---------------- MIN_{23-0} ---------------->																							S
M	T	C	C								S																													T
P	A	C	C								V																													O
T	R	1	0								D																													P
Y	T																																							

NOTES:

1. The STOP bit is not part of the structure.
2. The EMPTY bit is not used and is always set to zero.

Message to be transmitted is stored in structure: TX_MESSAGE (m).TX_WRD_DATPRO (b)
where: m is word number (0-5)
b is byte number within word (0-4) counting from left

NOTE: Due to the DPROC hardware problem in transmission, the µController performs message formatting and transmission instead of the DPROC. To that effect, the transmit software routine which normally passes to the DPROC a data word (40bits), namely DPROC_SEND_DATA_WORD, has been replaced with another routine, SEND_DPROC_MESSAGE in DPROC.PLM module.

SEND_DPROC_MESSAGE now forms the message to be transmitted by calculating the parity for each of the repeats of the word (5 repeats) and forms a frame. This frame of 5 data words is then preceded with Dotting, Word synchronization, and encoded DCC to form the final message to be transmitted.

SND_DATA_ASM routine is then called to perform the transmission on the TX_{LINE}. The transmit driver routine, SND_DATA_ASM, is written in assembly language for better efficiency, and is located in a file called SENDI.ASM. Note that TX_{LINE} wire is used to transmit the data. It must be routed to the APROC's summing input. TX_{CLK} is unused (not toggled by software).

We have included in the software a compilation variable, BYPASS, in order to invoke the appropriate transmit routine. With the new DPROC (TN2683) which fixes the transmit hardware problem, the transmit software routine can be removed. The user should, however, re-compile all modules with BYPASS =0 (see compilation example) in order to select DPROC_SEND_DATA_WORD routine (DPROC.PLM and SENDI.ASM may be deleted).

Summary: If BYPASS =1, the parity is computed and appended at the end of each word of the 5-word frame, and Dotting + WSYNC + encoded DCC are inserted at the beginning of that frame before the whole message is transmitted on TX_{LINE} to APROC summing input, by SENDI.ASM.

Receiver Routine

When the DPROC has received and decoded the incoming DEMODD data of the Forward control channel (FOCC), it pulls the RX_{LINE} LOW. The system controller, which is now in receive message mode polling RX_{LINE} continuously looking for messages on FOCC, supplies RX_{CLK} to clock the data out of the DPROC according to the received data timing (page 12 of DPROC spec.). The receive routine, DATA_PRO_RX, first pulls the clock line LOW, waits some time for the hardware to settle, then clocks out DPROC data on the rising edge. A total of 32 bits (4 bytes) are clocked in and the clock is left in a HIGH state as the spec. shows.

The received word has the following format (word1).

BYTE 0								BYTE 1								BYTE 2								BYTE 3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
START	BCHERR	T1	T2	DCC1	DCC0	<---------------- SID_1 ---------------->														RSVD			NAWC				OHD			SPARE	STOP

Received message is stored in structure: RX_MESSAGE (m).RX_WRD_DATPRO (b)
where: m is word number (0-15)
b is byte number within word (0-3) counting from left

IOMOD.PLM: This file contains a list of high level routines used to program devices on the I^2C bus. Such routines rely on lower level I^2C routines, in I2C.PLM, to perform the actual data transfer. Note that a specific data structure must be adopted in order to make use of IOMOD.PLM independently.

MSGXHAND.PLM: This file contains high level routines that perform string processing for the UART interface. They rely on lower level routines, in V24INT.PLM, to maintain the data structure for data received from the Dumb terminal keyboard, and data sent to the Dumb terminal screen.

SENDI.PLM: This is a program written in assembly language and designed to transmit the message for the DPROC. The data bits are shifted out on TX_{LINE} at a frequency equals twice the data rate, due to Manchester encoding.

SYNTH.PLM (LOPSY.PLM): This file contains procedures to program the synthesizers (Receive and Transmit). They use the I^2C routines which do the actual data transfer. SYNTH.PLM MUST be used with the UMA1010/12 synthesizers only, and LOPSY.PLM MUST be used with TDD1742 synthesizers. Both files contain the same set of routine names. So if they are both compiled, the one that is linked last will be the effective one. Note that TDD1742 has no I^2C interface, and must be used with an I/O expander PCF8574.

V24INT.PLM: This file holds the µcontroller PCB80C552 UART interface routines for data transfer from and to the Dumb terminal. This file sits below MSGXHAND.PLM hierarchically.

NOTE: V24INT.PLM and MSGXHAND.PLM are NOT part of cellular operation. They were developed to support test programs and utilities in TESTH.PLM.

4.2.2. High Level Modules

This is the list of modules that implement the AMPS/TACS standards. It is presented alphabetically.

CODMSG.PLM: This module is a support module. It deals with encoding of words A..E, as labeled in EIA spec, for transmission on the reverse control channel. It also encodes words F..H for transmission on the reverse voice channel. Note that words F, G and H are Order Confirmation, Called-Address Word, and Called-Address Word 2, respectively.

IDLE.PLM: The Idle mode has several main functions to perform. These include:

1. Check data fading,
   (5sec. timer to read OverHeaD message)
2. Check non-preferred system timeout,
   (TACS only)
3. Respond to Overhead MSG,
4. Respond to mobile control MSG
   (Page and Order),
5. Check re-registration timeup,
   (TACS only)
6. Support call initiation request
   (SEND key pressed)

When certain conditions specific to the function involved are satisfied, the above functions can cause the mobile to exit from Idle state into either INITialization or SYStem access states. When this happens, the program returns IDLE_EXIT_REASON flag which will be used by a higher level module (NORMOD) to decide on the next action to take. IDLE_EXIT_REASON is initially set to NULL and is used to keep the mobile in Idle state.

While the mobile is in IDLE state, and IDLE_EXIT_REASON = NULL, the µcontroller is put in idle or "sleep" mode by setting register PCON[0] = 1. In addition, we set variable LO_POWER_MODE = TRUE to indicate to the master timer routine, in TIMINT.PLM, to change the periodic interrupts from 1msec to 25msec. At the next timer interrupt, the µcontroller wakes up (every 25msec.) and resumes execution of the IDLE state starting from the line of code following the assignment statement: 'PCON = 0000001'.

INIT.PLM: The top level routine, INITIALIZATION_STATE, consists of three nested loops. The inner most one dictates that an overhead message must be read on the DEDICATED CONTROL CHANNEL and parameters updated. It is possible that the mobile alternates between two serving systems if no overhead message can be received from either system.

Coming out of the inner loop, the mobile needs to read an overhead message on the PAGING CHANNEL. If it failed on the current serving system (system A or system B), it has to restart on the other serving system. If it has successfully gone through the above two stages, the overhead information collected on the Dedicated Control Channel is compared with that collected on the Paging Channel. Unless they match, the above activities are repeated indefinitely.

There is another requirement of the spec (SSDT) which allows the mobile to enter this procedure at the middle, skipping stages of initialization and the inner loop described above. That is dealt with using a flag INIT_1ST_STAGE.

MAIN.PLM: Contains a call to POWERUP to initialize the software and the hardware and a call to the state machine handler (NORMOD) which decides which of the four states to go to next (Figure 4.1).

NORMOD.PLM: State machine handler. Based on the ...EXIT_REASON of one state, this routine selects next state and calls the corresponding routine. Debug messages can be placed here, displaying reasons for exiting one state and entering another.

PWRUP.PLM: Initializes global variables such as control registers for DPROC and APROC, serving system, etc.

RDMSSG.PLM: This is a support module. It reads state dependent messages from DPROC.

REG.PLM: This is a support module. It deals with updating the registration variables, and keeps track of the last four visited areas (NEXTREGs-p SIDs-p pair).

REPLY.PLM: This is a support module. It contains functional blocks related to handling replies from land station during system access.

RFXHIXLE.PLM: High level to SYNTH.PLM (or LOPSY.PLM). It scans the dedicated control channel spectrum of system A or system B and chooses the best channel.

SYS.PLM: When a mobile enters System Access state from Idle, its IDLE EXIT REASON becomes the ACCESS AIM in the context of this state. A SYSACC EXIT REASON is initially set to NULL on entry. When changed to one of the following reasons, the SYSACC EXIT REASON causes an exit from this state.

ORDER_CONFIRMED
MSG_TIMOUT

OVERLOAD_DISTB_DELAY,
(TACS)
EXCEED_MAX_BUSY

EXCEED MAX SEIZE
RELEASE

INTERCEPT
RE-ORDER

USR_HALT
ACCESS_TIMOUT

VCHAN_ASSIGNED

Apart from VCHAN ASSIGNED in which case the mobile enters 'Control of voice channel' state, the other reasons cause it to go to SSDT (Serving System Determination Task). The mobile can retry to gain access if it received a directed retry message from the land station by selecting from a new set of access channels' two best ones.

TIMINT.PLM: Interrupts occur every 1msec during the active states of the mobile, i.e., POWER UP, INITIALIZATION, SYSTEM ACCESS and VCHAN; but during IDLE state the interrupts occur every 25msec with the timer increments being adjusted accordingly. This allows the processor to spend more time in the low power mode which is flagged by a bit (LO_POWER_MODE), and the timer interrupt sets another bit (LONG_TIMER_INT) to flag the change from 1ms to 25msec increments.

Timers are configured into two arrays of 5 entries each. One array measures in MSEC (millisecond), and the other measures in MINutes. They are considered as high level timers and are declared as follows:

GP_TIMER_MSEC (NUM_OF_GP_TIMERS)	word	external auxiliary
GP_TIMER_MIN (NUM_OF_GP_TIMERS)	byte	external auxiliary

where NUM_OF_GP_TIMERS = 5

Note that handling these is the responsibility of the user, i.e., they can be used as any system timer as defined by AMPS or TACS.

The main part of this module is the T0 interrupt vector routine which is called every 1msec (or 25msec). The msec portions of the timers is decremented by one. When msec reaches zero, the MIN portion is examined and decremented if > 0 while the MSEC portion is loaded with 60000. If the MIN portion is zero and the MSEC portion is also zero, the timer is no longer decremented. Note that the timers can be Enabled and Disabled by loading 00h and 0FFh, respectively, in the MIN part. If the timer value is more than 1 minute, it is automatically enabled.

The timer interrupt allocates timeslots within a 128msec frame to perform the various time related functions. The low level timers are updated every 1msec, and high level timers are updated every 4msec to prevent timer interrupt overrun. The keypad is scanned every 32msec.

The interrupt by timer T0 is caused by a 16-bit counter overflow. Therefore, T0 must be loaded with an initial value of 0FC65hex to cause 1msec interrupt, and must be loaded with 0A5FFhex for a 25msec interrupt according to the following:

Xtal = 11.059MHz.

Timer Period of 1msec is TP = (XTAL Hz/12)10^{-3} sec. = 1ms;

where 12 = 1 machine cycle.

@ 11.059MHz, 1msec period	= 039Ah	
1 ms TIMER	= 0FFFFh - 039A	= 0FC65h; counting up
@ 11.059MHz, 25msec period	= 5A00h	
25 msec TIMER	= 0FFFFh - 5A00h	= 0A5FFh; counting up

Hence

TIMER_RELOAD_HI	= 0FCh
TIMER_RELOAD_LO	= 065h
TIMER_RELOAD_HI_25	= 0A5h
TIMER_RELOAD_LO_25	= 0FFh:

This module also handles the telephone keypad by scanning it. Routine KBOARD_SC scans the keypad and returns the declared value of the key pressed; NULL if no key pressed, or 0FFh if two keys pressed. The key pressed is checked again in 32msec for debounced. If the key is accepted the key value is stored into the keypad buffer and later used by READ_USER_INPUT routine, called from various points in the software to update the LCD. Note that if a key remains pressed, it is only accepted once.

TXMSSG.PLM: High level to INTDAT.PLM (or DPROC.PLM) in that it deals with transmission of data words to DPROC. It monitors channel arbitration (BUSY/IDLE signal from DPROC) and turns OFF transmitter (TXDIS = 0) in the case of collision, as specified by UMA1000 specification, **Reverse Control Channel Access Arbitration**, page 11. The arbitration is specified as follows:

1. Initial condition: Busy/Idle = Idle; transmission in progress.
2. If B/I reverts to Busy before the first 54 bits have been transmitted, a collision has occurred.
3. If B/I does not revert to Busy after 104 bits have been transmitted, a collision has occurred.

VCHAN.PLM (mobile station control of voice channel): The Control of Voice channel state consists of the following sub-states:

1. WAIT FOR ORDER
2. WAIT FOR ANSWER
3. CONVERSATION
4. RELEASE VOICE CHANNEL

Within these sub-states, the mobile waits to receive either a user command or an order from the land station. Apart from having received a command/order which requires the mobile to come out of the wait loop, it also emerges when other conditions are satisfied. These conditions are

1. Fade timeout
2. Time to check channel quality (SAT), at least every 250msec

After having processed the order/command/emerge condition, the sub-states report the result to its immediate calling routine (1 level up, control of voice channel) which directs the mobile to enter a new sub-state as listed above, or re-enter the same sub-state. The mobile stays on the voice channel until there is a reason to leave such as Answer timeout, Fade timeout or Release command. When VCHAN is first entered, the task of 'Confirming initial voice channel ' is carried out. For as long as the mobile remains on the voice channel, the quality of the voice channel is monitored by reading SAT color code (SCC).

XTRCT.PLM: This is a support module. It unpacks received messages into individual fields and sets appropriate variables.

4.2.3. Include Files

DATETIME.DCL: This file contains a declaration of a CONSTant string which, when called by the software, will display a date and time stamp. It is included in MAIN.PLM. This file must be updated to reflect the current date and time before compilting MAIN.PLM. Such utility is not provided with the source code.

DECLAR.DCL: This is a list of declaration of variables. It is inluded in all *.PLM files.

EXTRNS.DCL: This is a list of declaration of external variables and external procedures. It is inluded in PWRUP.PLM file.

REG552.DCL: This file contains the 80C552 Special Function Register map and declarations of those registers. It is developed by INTEL.

REPEAT.DCL: This file contains a macro definition of REPEAT...UNTIL statement. It is included in DPROC.PLM.

PUBLIC.DCL: This is a list of global variable declarations. It is included in MAIN.PLM. A change in this list must be followed by a compilation of MAIN.PLM.

UTIL51.DCL: This is a list of library routines to aid in the programming. It is developed by INTEL, the supplier of PLM51 compiler.

4.2.4. Installation

The hardware platform is assumed to be an IBM PC or compatible. There are three floppies containing all the files needed to generate the PROM code for the chip-set evaluator unit. The PLM51 compiler and linker programs must be resident, or reachable, from the working directory. Insert the floppies and use the COPY command to copy the content into a working directory. Proceed to next section to learn about compilation and linking, but here is a summary of commands to get PROM code:

1. COPY B:*.* <CR>
   { Repeat for all three floppies }
2. BUILD <CR>
3. LINK <CR>

The final PROM code resides in file CELL1.HEX

4.2.5. Compiling and Linking

There are several command files set up to aid the programmer in the compilation of the source modules, and link their corresponding object modules. After every source module is compiled, it is added to a library called USERLIB.LIB (this file can be created by running LIB51 program). When all modules have been compiled and added to USERLIB.LIB, the linker must be invoked by running RL51 program to resolve all external definitions and produce the final HEX code. Below is a list of the command files and their functions.

PLMA.BAT This command file calls up the PLM51 compiler and, if there are no errors, invokes the library program LIB51 to add the compiled module to the list of object modules. When done, it deletes the .OBJ file to free up disk space. An example of PLMA content is shown below.

USAGE: PLMA < module name, without .PLM extension >

Example: PLMA ADCINT

NOTE: The user must provide a program to automatically update file DATETIME.DCL every time PLMA is called on MAIN(.PLM). Date and Time stamping is important to keep track of software revisions.

Example: PLMA.BAT

```
echo off
if exist %1.plm goto COMPILE
echo ERROR ! File does not exist
goto END
:COMPILE
echo Compiling...  AMPS = SET, BYPASS = SET
if %1==main echo Running date stamp
if %1==MAIN echo Running date stamp
if %1==main < Include a call to a program to update the date/time stamp in DATETIME.DCL file >
if %1==MAIN < Include a call to a program to update the date/time stamp in DATETIME.DCL file >
plm51 %1.PLM SET(BYPASS) SET(AMPS) DEBUG LIST OPTIMIZE(3) CODE
if not errorlevel 2 goto LIBRARY
echo ERROR in compilation !
echo MODULE has not been updated in library
goto END
:LIBRARY
if %1==main goto END
if %1==MAIN goto END
echo Adding to Library
lib51 replace %1.obj in userlib.lib
del %1.obj
del %1.lst
:END
echo on
```

LINK.BAT This routine must be called to link the object modules and produce the final hex code. Below is an example of LINK.BAT.

USAGE: LINK

Example: LINK.BAT

```
echo off
RL51 MAIN.OBJ, SENDI.OBJ, INTERRUP.OBJ, USERLIB.LIB, PLM51.LIB, UTIL51.LIB TO
CELL1.ABS IXREF overlay
oh cell1.abs to cell1.hex
echo on
```

BUILD.BAT This utility file will compile all the modules and add them to USERLIB.LIB. It must be followed by LINK.BAT to generate the PROM code. Below is an example of BUILD.BAT.

USAGE: BUILD

Example: BUILD.BAT

```
call PLMA codmsg
call PLMA dproc
call PLMA except
call PLMA hsekpr
call PLMA idle
call PLMA iic
call PLMA init
call PLMA intdat
call PLMA lopsy
call PLMA main
call PLMA msgxhand
call PLMA normod
call PLMA pwrup
call PLMA rdmssg
call PLMA reg
call PLMA reply
call PLMA sys
call PLMA testh
call PLMA timint
call PLMA txmssg
call PLMA v24int
call PLMA vchan
call PLMA xtrct
```

I²C Bus specification

RF Communications

INTRODUCTION

For 8-bit applications, such as those requiring single-chip microcomputers, certain design criteria can be established:

- A complete system usually consists of at least one microcomputer and other peripheral devices, such as memories and I/O expanders.
- The cost of connecting the various devices within the system must be kept to a minimum.
- Such a system usually performs a control function and does not require high-speed data transfer.
- Overall efficiency depends on the devices chosen and the interconnecting bus structure.

In order to produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the through-put capability of parallel buses, they do require less wiring and fewer connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

Devices communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss, and blockage of information. Fast devices must be able to communicate with slow devices. The system must not be dependent on the devices connected to it; otherwise, modifications or improvements would be impossible. A procedure has also to be resolved to decide which device will be in control of the bus and when. And if different devices with different clock speeds are connected to the bus, the bus clock source must be defined.

All these criteria are involved in the specification of the I²C bus.

THE I²C BUS CONCEPT

Any manufacturing process (NMOS, CMOS, I²L) can be supported by the I²C bus. Two wires (SDA—serial data, SCL—serial clock) carry information between the devices connected to the bus. Each device is recognized by a unique address—whether it is a microcomputer, LCD driver, memory or keyboard interface—and can operate as either a transmitter or receiver, depending on the function of the device. Obviously an LCD driver is only a receiver, while a memory can both receive and transmit data. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers (see Table 1). A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The I²C bus is a multimaster bus. This means that more than one device capable of controlling the bus can be connected to it. As masters are usually microcomputers, let's consider the case of a data transfer between two microcomputers connected to the I²C bus (Figure 1). This highlights the master-slave and receiver-transmitter relationships to be found on the I²C bus. It should be noted that these relationships are not permanent, but only depend on the direction of data transfer at that time. The transfer of data would follow in this way:

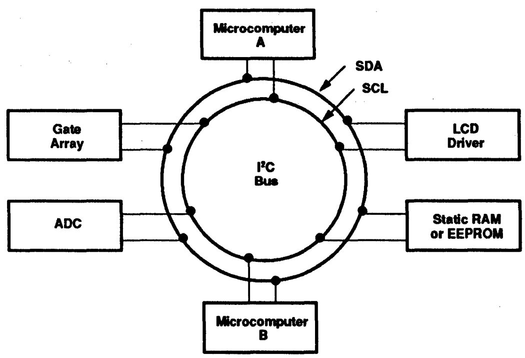


Figure 1. Typical I²C Bus Configuration

I^2C Bus specification

Table 1. Definition of I^2C Bus Terminology

TERM	DESCRIPTION
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals, and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

1. Suppose microcomputer A wants to send information to microcomputer B.
   - –Microcomputer A (master) addresses microcomputer B (slave)
   - –Microcomputer A (master transmitter) sends data to microcomputer B (slave receiver)
   - –Microcomputer A terminates the transfer.
2. If microcomputer A wants to receive information from microcomputer B
   - –Microcomputer A (master) addresses microcomputer B (slave)
   - –Microcomputer A (master receiver) receives data from microcomputer B (slave transmitter)
   - –Microcomputer A terminates the transfer.

Even in this case, the master (microcomputer A) generates the timing and terminates the transfer.

The possibility of more than one microcomputer being connected to the I^2C bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event, an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all devices to the I^2C bus.

If two or more masters try to put information on to the bus, the first to produce a one when the other produces a zero will lose the arbitration. The clock signals during arbitration are a synchronized combination of the clocks generated by the masters using the wired-AND connection to the SCL line (for more detailed information concerning arbitration see Arbitration and Clock Generation).

Generation of clock signals on the I^2C bus is always the responsibility of master devices; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow slave device holding down the clock line or by another master when arbitration takes place.

GENERAL CHARACTERISTICS

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Figure 2). When the bus is free, both lines are High. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. Data on the I^2C bus can be transferred at a rate up to 100kbit/s. The number of devices connected to the bus is solely dependent on the limiting bus capacitance of 400pF.

BIT TRANSFER

Due to the variety of different technology devices (CMOS, NMOS, I^2L) which can be connected to the I^2C bus, the levels of the logical 0 (Low) and 1 (High) are not fixed and depend on the appropriate level of V_{DD} (see Electrical Specifications). One clock pulse is generated for each data bit transferred.

Data Validity

The data on the SDA line must be stable during the High period of the clock. The High or Low state of the data line can only change when the clock signal on the SCL line is Low (Figure 3).

Start and Stop Conditions

Within the procedure of the I^2C bus, unique situations arise which are defined as start and stop conditions (see Figure 4).

A High-to-Low transition of the SDA line while SCL is High is one such unique case. This situation indicates a start condition.

A Low-to-High transition of the SDA line while SCL is High defines a stop condition.

Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition. The bus is considered to be free again a certain time after the stop condition. This bus free situation will be described later in detail.

Detection of start and stop conditions by devices connected to the bus is easy if they have the necessary interfacing hardware. However, microcomputers with no such interface have to sample the SDA line at least twice per clock period in order to sense the transition.

I²C Bus specification

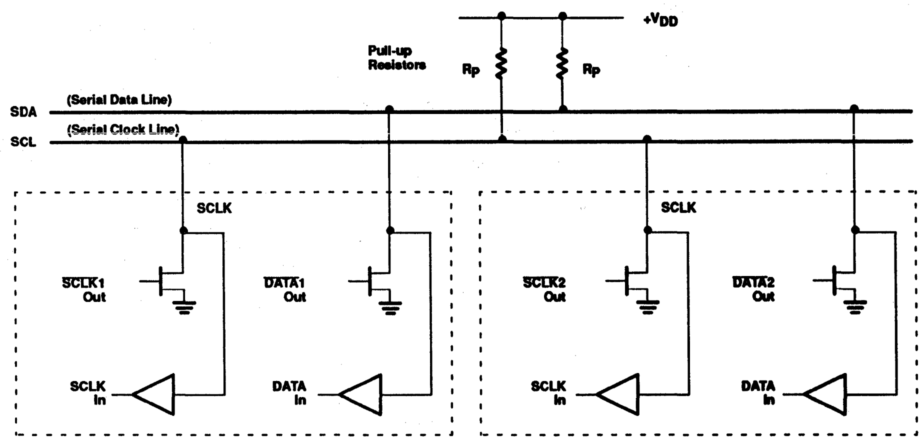


Figure 2. Connection of Devices to the I²C Bus

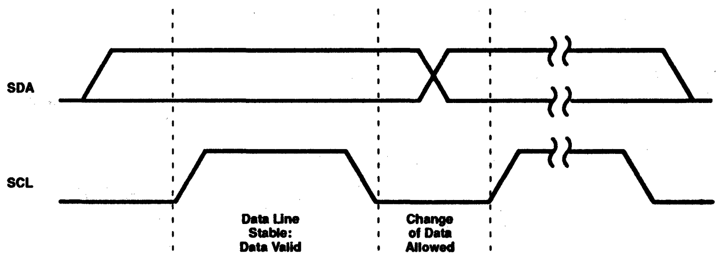


Figure 3. Bit Transfer on the I²C Bus

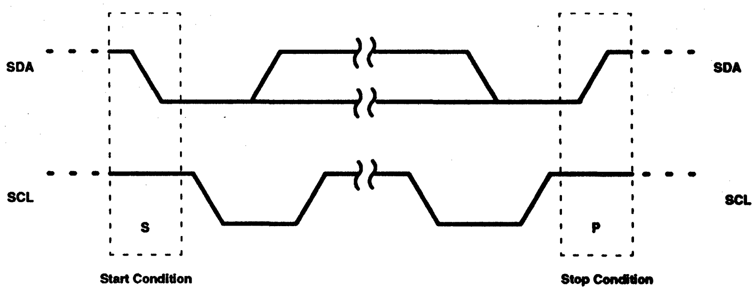


Figure 4. Start and Stop Conditions

I²C Bus specification

TRANSFERRING DATA

Byte Format

Every byte put on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit.

Data is transferred with the most significant bit (MSB) first (Figure 5). If a receiving device cannot receive another complete byte of data until it has performed some other function, for example, to service an internal interrupt, it can hold the clock line SCL Low to force the transmitter into a wait state. Data transfer then continues when the receiver is ready for another byte of data and releases the clock line SCL.

In some cases, it is permitted to use a different format from the I²C bus format, such as CBUS compatible devices. A message which starts with such an address can be terminated by the generation of a stop condition, even during the transmission of a byte. In this case, no acknowledge is generated.

Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitting device releases the SDA line (High) during the acknowledge clock pulse.

The receiving device has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable Low during the high period of this clock pulse (Figure 6). Of course, setup and hold times must also be taken into account and these will be described in the Timing section.

Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received (except when the message starts with a CBUS address).

When a slave receiver does not acknowledge on the slave address, for example, because it is unable to receive while it is performing some real-time function, the data line must be left High by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave receiver does acknowledge the slave address, but some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave not generating the acknowledge on the first byte following. The slave leaves the data line High and the master generates the STOP condition.

In the case of a master receiver involved in a transfer, it must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate the STOP condition.

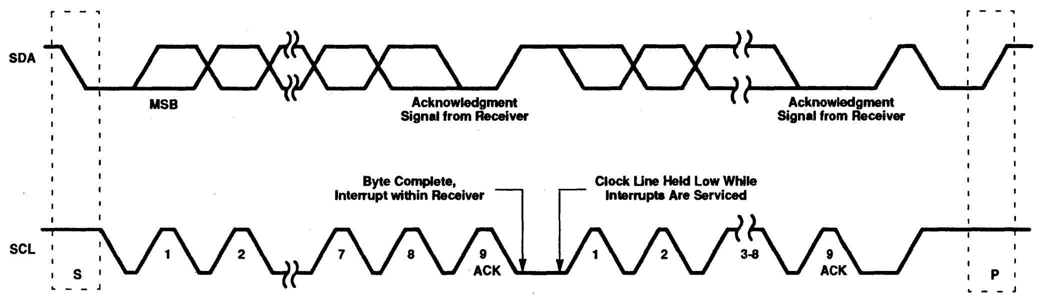


Figure 5. Data Transfer on the I²C Bus

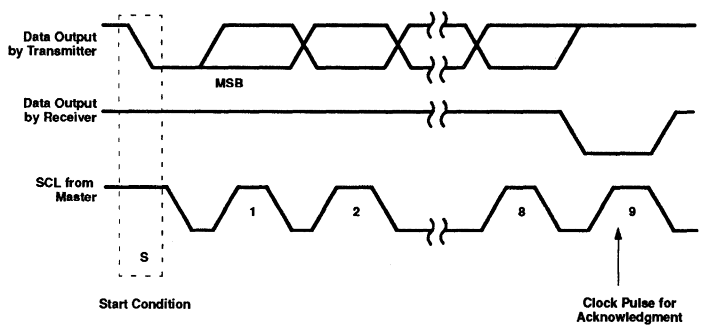


Figure 6. Acknowledge on the I²C Bus

I²C Bus specification

ARBITRATION AND CLOCK GENERATION

Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I²C bus. Data is only valid during the clock High period on the SCL line; therefore, a defined clock is needed if the bit-by-bit arbitration procedure is to take place.

Clock synchronization is performed using the wired-AND connection of devices to the SCL LINE. This means that a High-to-Low transition on the SCL line will affect the devices concerned, causing them to start counting off their Low period. Once a device clock has gone Low it will hold the SCL line in that state until the clock High state is reached (Figure 7). However, the Low-to-High change in this device clock may not change the state of the SCL line if another device clock is still within its Low period. Therefore, SCL will be held Low by the device with the longest Low period. Devices with shorter Low periods enter a High wait state during this time.

When all devices concerned have counted off their Low period, the clock line will be released and go High. There will then be no difference between the device clocks and the state of the SCL line and all of them will start counting their High periods. The first device to complete its High period will again pull the SCL line Low.

In this way, a synchronized SCL clock is generated for which the Low period is determined by the device with the longest clock Low period while the High period on SCL is determined by the device with the shortest clock High period.

Arbitration

Arbitration takes place on the SDA line in such a way that the master which transmits a High level, while another master transmits a Low level, will switch off its DATA output stage since the level on the bus does not correspond to its own level.

Arbitration can carry on through many bits. The first stage of arbitration is the comparison of the address bits. If the masters are each trying to address the same device, arbitration continues into a comparison of the data. Because address and data information is used on the I²C bus for the arbitration, no information is lost during this process.

A master which loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

If a master does lose arbitration during the addressing stage, it is possible that the winning master is trying to address it. Therefore, the losing master must switch over immediately to its slave receiver mode.

Figure 8 shows the arbitration procedure for two masters. Of course more may be involved, depending on how many masters are connected to the bus. The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a High output level is then connected to the bus. This will not affect the data transfer initiated by the winning master. As control of the I²C bus is decided solely on the address and data sent by competing masters, there is no central master, nor any order of priority on the bus.

Use of the Clock Synchronizing Mechanism as a Handshake

In addition to being used during the arbitration procedure, the clock synchronization mechanism can be used to enable receiving devices to cope with fast data transfers, either on a byte or bit level.

On the byte level, a device may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slave devices can then hold the SCL line Low, after reception and acknowledge of a byte, to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

On the bit level, a device such as a microcomputer without a hardware I²C interface on-chip can slow down the bus clock by extending each clock Low period. In this way, the speed of any master is adapted to the internal operating rate of this device.

Formats

Data transfers follow the format shown in Figure 9. After the start condition, a slave address is sent. This address is 7 bits long; the eighth bit is a data direction bit (R/$\overline{W}$). A zero indicates a transmission (WRITE); a one indicates a request for data (READ). A data transfer is always terminated by a stop condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate another start condition, and address another slave without first generating a stop condition. Various combinations of read/write formats are then possible within such a transfer.

At the moment of the first acknowledge, the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter. This acknowledge is still generated by the slave.

The stop condition is generated by the master.

During a change of direction within a transfer, the start condition and the slave address are both repeated, but with the R/$\overline{W}$ bit reversed.

I^2C Bus specification

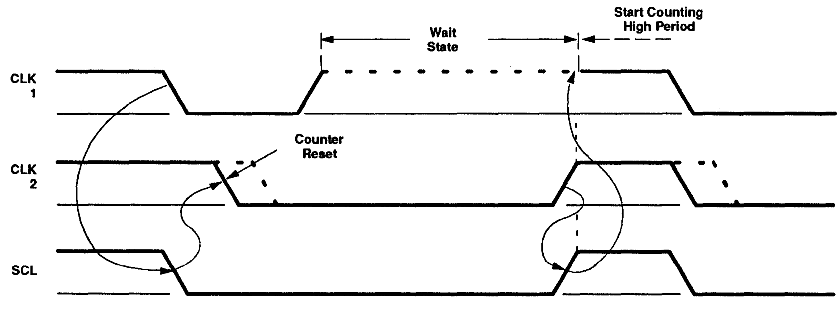


Figure 7. Clock Synchronization During the Arbitration Procedure

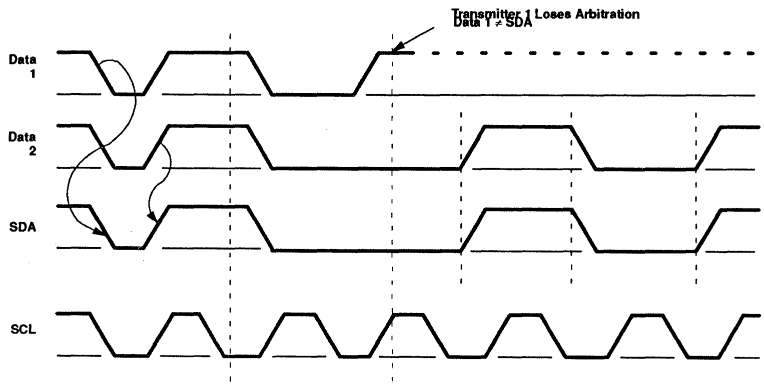


Figure 8. Arbitration Procedure of Two Masters

I²C Bus specification

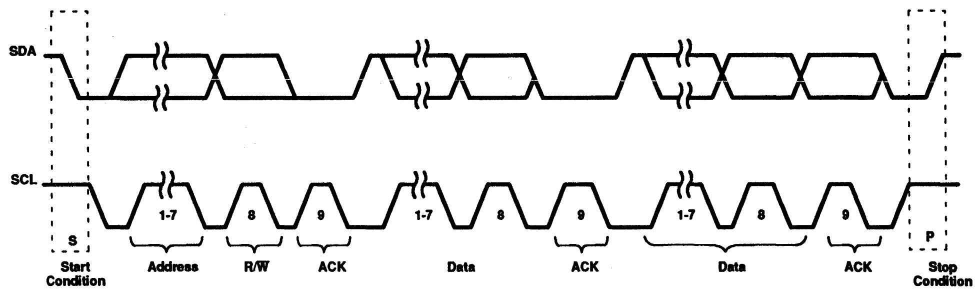
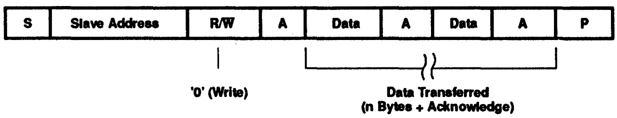


Figure 9. Complete Data Transfer

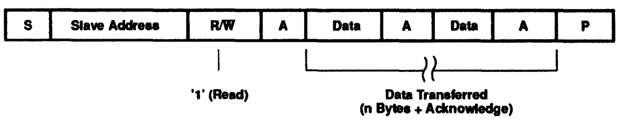
Possible Data Transfer Formats Are:

a) Master transmitter transmits to slave receiver. Direction is not changed.

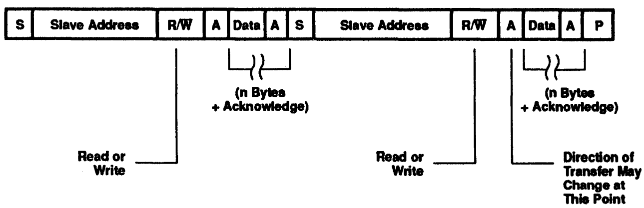
A = Acknowledge
S = Start
P = Stop



b) Master reads slave immediately after first byte.



c) Combined formats.



NOTES:

1. Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the start condition is repeated, data can then be transferred.
2. All decisions on auto-increment or decrement of previously accessed memory locations, etc., are taken by the designer of the device.
3. Each byte is followed by an acknowledge as indicated by the A blocks in the sequence.
4. I²C devices have to reset their bus logic on receipt of a start condition so that they all anticipate the sending of a slave address.

I²C Bus specification

ADDRESSING

The first byte after the start condition determines which slave will be selected by the master. Usually, this first byte follows that start procedure. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge, although devices can be made to ignore this address. The second byte of the general call address then defines the action to be taken.

Definition of Bits in the First Byte

The first seven bits of this byte make up the slave address (Figure 10). The eighth bit (LSB—least significant bit) determines the direction of the message. A zero on the least significant position of the first byte means that the master will write information to a selected slave; a one in this position means that the master will read information from the slave.

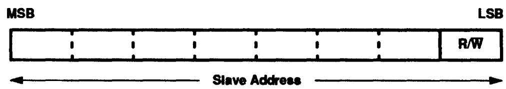


Figure 10. The First Byte After the Start Procedure

When an address is sent, each device in a system compares the first 7 bits after the start condition with its own address. If there is a match, the device will consider itself addressed by the master as a slave receiver or slave transmitter, depending on the R/W̄ bit.

The slave address can be made up of a fixed and a programmable part. Since it is expected that identical ICs will be used more than once in a system, the programmable part of the slave address enables the maximum possible number of such devices to be connected to the I²C bus. The number of programmable address bits of a device depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of eight identical devices can be connected to the same bus.

The I²C bus committee is available to coordinate allocation of I²C addresses.

The bit combination 1111XXX of the slave address is reserved for future extension purposes.

The address 1111111 is reserved as the extension address. This means that the addressing procedure will be continued in the next byte(s). Devices that do not use the extended addressing do not react at the reception of this byte. The seven other possibilities in group 1111 will also only be used for extension purposes but are not yet allocated.

The combination 0000XXX has been defined as a special group. The following addresses have been allocated:

FIRST BYTE			
SLAVE ADDRESS		R/W̄	
0000	000	0	General call address
0000	000	1	Start byte
0000	001	X	CBUS address
0000	010	X	Address reserved for different bus format
0000	011	X	
0000	100	X	To be defined
0000	101	X	To be defined
0000	110	X	To be defined
0000	111	X	To be defined

No device is allowed to acknowledge at the reception of the start byte.

The CBUS address has been reserved to enable the intermixing of CBUS and I²C devices in one system. I²C bus devices are not allowed to respond at the reception of this address.

The address reserved for a different bus format is included to enable the mixing of I²C and other protocols. Only I²C devices that are able to work with such formats and protocols are allowed to respond to this address.

General Call Address

The general call address should be used to address every device connected to the I²C bus. However, if a device does not need any of the data supplied within the general call structure, it can ignore this address by not acknowledging. If a device does require data from a general call address, it will acknowledge this address and behave as a slave receiver. The second and following bytes will be acknowledged by every slave receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not acknowledging.
The meaning of the general call address is always specified in the second byte (Figure 11).

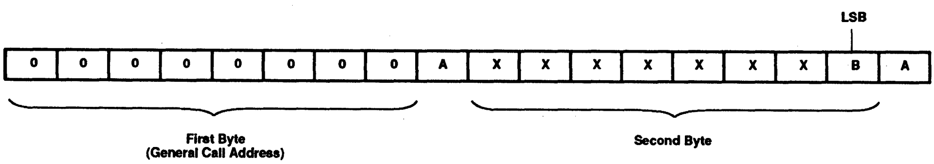


Figure 11. General Call Address Format

I²C Bus specification

There are two cases to consider:

1. When the least significant bit is a zero.
2. When the least significant bit is a one.

When B is a zero, the second byte has the following definition:

00000110 (H'06') Reset and write the programmable part of slave address by software and hardware. On receiving this two-byte sequence, all devices (designed to respond to the general call address) will reset and take in the programmable part of their address.
Precautions must be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.

00000010 (H'02') Write slave address by software only. All devices which obtain the programmable part of their address by software (and which have been designed to respond to the general call address) will enter a mode in which they can be programmed. The device will not reset.

An example of a data transfer of a programming master is shown in Figure 12 (ABCD represents the fixed part of the address).

00000100 (H'04') Write slave address by hardware only. All devices which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two-byte sequence. The device will not reset.

00000000 ('H00') This code is not allowed to be used as the second byte.

Sequences of programming procedure are published in the appropriate device data sheets.

The remaining codes have not been fixed and devices must ignore these codes.

When B is a one, the two-byte sequence is a hardware general call. This means that the sequence is transmitted by a hardware master device, such as a keyboard scanner, which cannot be programmed to transmit a desired slave address. Since a hardware master does not know in advance to which device the message must be transferred, it can only generate this hardware general call and its own address, thereby identifying itself to the system (Figure 13).

The seven bits remaining in the second byte contain the device address of the hardware master. This address is recognized by an intelligent device, such as a microcomputer, connected to the bus which will then direct the information coming from the hardware master. If the hardware master can also act as a slave, the slave address is identical to the master address.

In some systems an alternative could be that the hardware master transmitter is brought in the slave receiver mode after the system reset. In this way, a system configuring master can tell the hardware master transmitter (which is now in slave receiver mode) to which address data must be sent (Figure 14). After this programming procedure, the hardware master remains in the master transmitter mode.

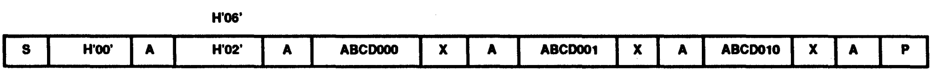


Figure 12. Sequence of a Programming Master

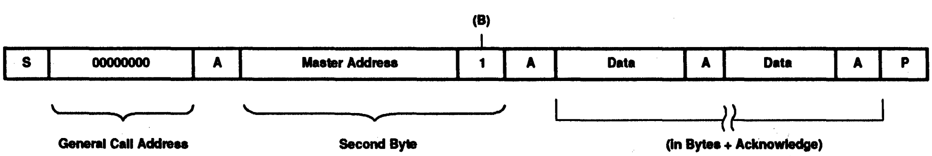


Figure 13. Data Transfer From Hardware Master Transmitter

I^2C Bus specification

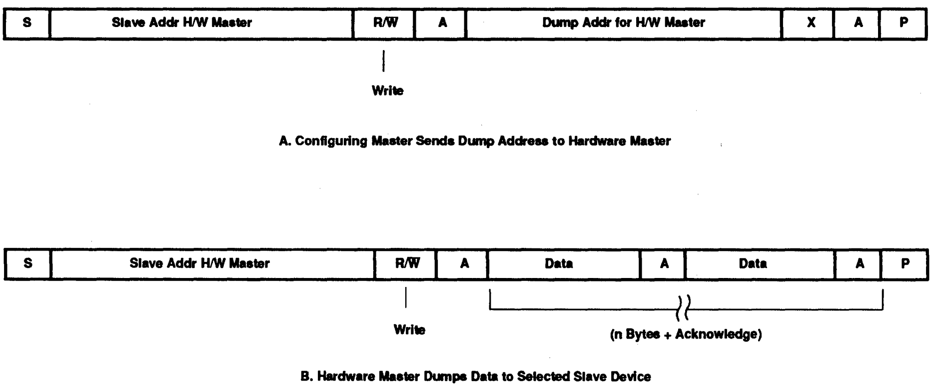


Figure 14. Data Transfer From Hardware Master Transmitter Capable of Dumping Data Directly to Slave Devices

Start Byte

Microcomputers can be connected to the I^2C bus in two ways. If an on-chip hardware I^2C bus interface is present, the microcomputer can be programmed to be interrupted only by requests from the bus. When the device possesses no such interface, it must constantly monitor the bus via software. Obviously, the more times the microcomputer monitors, or polls, the bus, the less time it can spend carrying out its intended function.

Therefore, there is a difference in speed between fast hardware devices and the relatively slow microcomputer which relies on software polling.

In this case, data transfer can be preceded by a start procedure which is much longer than normal (Figure 15). The start procedure consists of:

1. A start condition, (S)
2. A start byte 00000001
3. An acknowledge clock pulse
4. A repeated start condition, (Sr)

After the start condition (S) has been transmitted by a master requiring bus access, the start byte (00000001) is transmitted. Another microcomputer can therefore sample the SDA line on a low sampling rate until one of the seven zeros in the start byte is detected. After detection of the Low level on the SDA line, the microcomputer is then able to switch to a higher sampling rate in order to find the second start condition (Sr), which is then used for synchronization.

A hardware receiver will reset at the reception of the second start condition (Sr) and will therefore ignore the start byte.

After the start byte, an acknowledge-related clock pulse is generated. This is present only to conform with the byte-handling format used on the bus. No device is allowed to acknowledge the start byte.

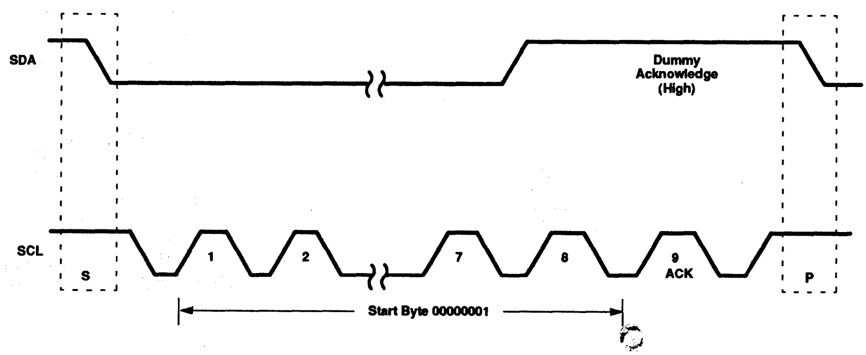


Figure 15. Start Byte Procedure

I²C Bus specification

CBUS Compatibility
Existing CBUS receivers can be connected to the I²C bus. In this case, a third line, called DLEN, has to be connected and the acknowledge bit omitted. Normally, I²C transmissions are multiples of 8-bit bytes; however, CBUS devices have different format.

In a mixed bus structure, I²C devices are not allowed to respond on the CBUS message. For this reason, a special CBUS address (0000001X) has been reserved. No I²C device will respond to this address. After the transmission of the CBUS address, the DLEN line can be made active and transmission, according to the CBUS format, can be performed (Figure 16).

After the stop condition, all devices are again ready to accept data.

Master transmitters are allowed to generate CBUS formats after having sent the CBUS address. Such a transmission is terminated by a stop condition, recognized by all devices. In the low speed mode, full 8-bit bytes must always be transmitted and the timing of the DLEN signal adapted.

If the CBUS configuration is know and no expansion with CBUS devices is foreseen, the user is allowed to adapt the hold time to the specific requirements of device(s) used.

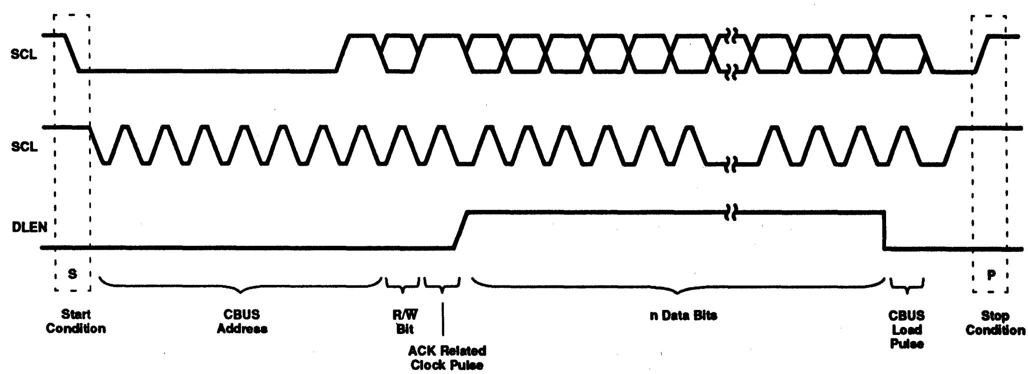


Figure 16. Data Format of Transmissions with CBUS Receiver/Transmitter

ELECTRICAL SPECIFICATIONS OF INPUTS AND OUTPUTS OF I²C DEVICES

The I²C bus allows communications between devices made in different technologies which might also use different supply voltages.

For devices with fixed input levels, operating on a supply voltage of +5V ±10%, the following levels have been defined:

V_{ILmax} =1.5V (maximum input Low voltage)
V_{IHmin} =3V (minimum input High voltage)

Devices operating on a fixed supply voltage different from +5 (e.g., I²L) must also have these input levels of 1.5V and 3V for V_{IL} and V_{IH}, respectively.

For devices operating over a wide range of supply voltages (e.g., CMOS), the following levels have been defined:

V_{ILmax} =0.3V_{DD} (maximum input Low voltage)
V_{IHmin} =0.7V_{DD} (minimum input High voltage)

For both groups of devices, the maximum output Low value has been defined:

V_{OLmax} =0.4V (max. output voltage Low) at 3mA sink current)

The maximum low-level input current at V_{OLmax} of both the SDA pin and the SCL pin of an I²C device is −10μA, including the leakage current of a possible output stage.

The maximum high-level input current at 0.9V_{DD} of both the SDA pin and SCL pin of an I²C device is 10μA, including the leakage current of a possible output stage.

The maximum capacitance of both the SDA pin and the SCL pin of an I²C device is 10pF.

Devices with fixed input levels can each have their own power supply of +5V ±10%. Pull-up resistors can be connected to any supply (see Figure 17).

However, the devices with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (see Figure 18).

When devices with fixed input levels are mixed with devices with V_{DD}-related levels, the latter devices have to be connected to one common supply line of +5V ±10% along with the pull-up resistors (Figure 19).

Input levels are defined in such a way that:

1. The noise margin on the Low level is 0.1 V_{DD}.
2. The noise margin on the High level is 0.2 V_{DD}.
3. Series resistors (R_S) up to 300Ω can be used for flash-over protection against high voltage spikes on the SDA and SCL line (due to flash-over of a TV picture tube, for example) (Figure 20).

The maximum bus capacitance per wire is 400pF. This includes the capacitance of the wire itself and the capacitance of the pins connected to it.

I²C Bus specification

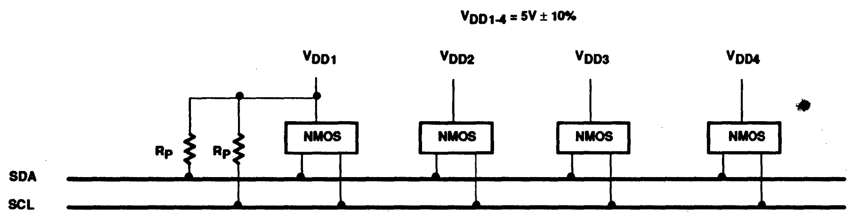


Figure 17. Fixed Input Level Devices Connected to the I²C Bus

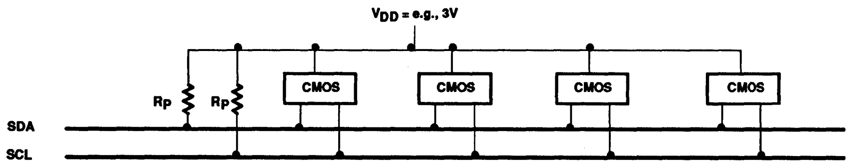


Figure 18. Devices with a Wide Range of Supply Voltages Connected to the I²C Bus

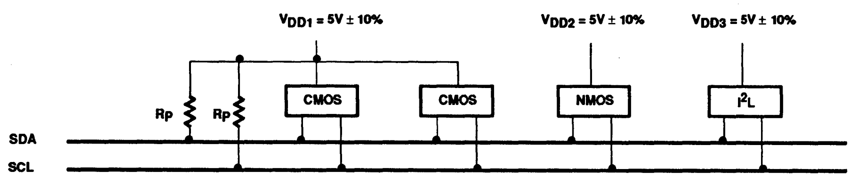


Figure 19. Devices with V_{DD} Related Levels Mixed with Fixed Input Level Devices on the I²C Bus

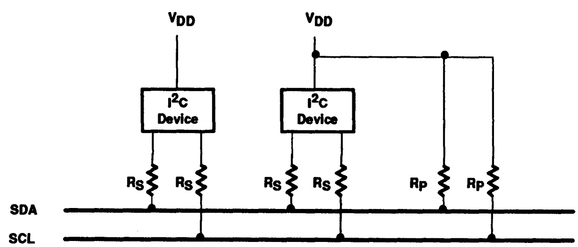


Figure 20. Serial Resistors (R_S) for Protection Against High Voltage

I²C Bus specification

TIMING

The clock on the I²C bus has a minimum Low period of 4.7µs and a minimum High period of 4µs. Masters in this mode can generate a bus clock with a frequency from 0 to 100kHz.

All devices connected to the bus must be able to follow transfers with frequencies up to 100kHz, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure which will force the master into a wait state and stretch the Low periods. In the latter case the frequency is reduced.

Figure 21 shows the timing requirements in detail. A description of the abbreviations used is shown in Table 2. All timing references are at V_{ILmax} and V_{ILmin}.

LOW-SPEED MODE

As explained previously, there is a difference in speed on the I²C bus between fast hardware devices and the relatively slow microcomputer which relies on software polling. For this reason a low speed mode is available on the I²C bus to allow these microcomputers to poll the bus less often.

Start and Stop Conditions

In the low-speed mode, data transfer is preceded by the start procedure.

Data Format and Timing

The bus clock in this mode has a Low period of 130µs +25µs and a High period of 390µs +25µs, resulting in a clock frequency of approximately 2kHz. The duty cycle of the clock has this Low-to-High ratio to allow for more efficient use of microcomputers without an on-chip hardware I²C bus interface. In this mode also, data transfer with acknowledge is obligatory. The maximum number of bytes transferred is not limited (Figure 22).

In this mode, a transfer cannot be terminated during the transmission of a byte.

The bus is considered busy after the first start condition. It is considered free again one minimum clock Low period, 105µs, after the detection of the stop condition. Figure 23 shows the timing requirements in detail Table 3 explains the abbreviations.

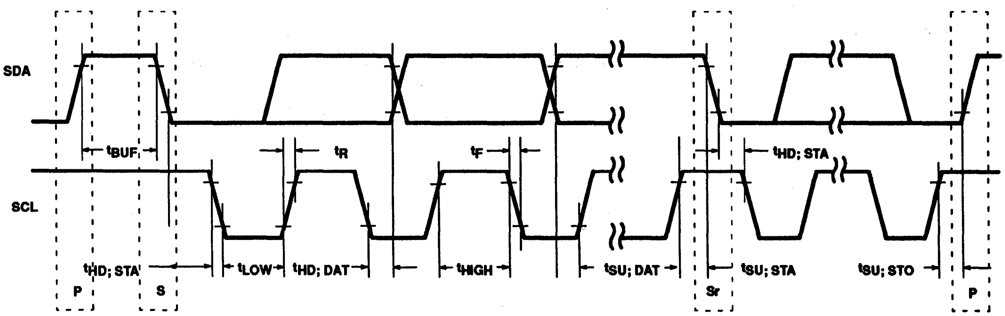


Figure 21. Timing Requirements for the I²C Bus

I^2C Bus specification

Table 2. Timing Requirement for the I^2C Bus

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
f_{SCL}	SCL clock frequency	0	100	kHz
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		µs
$t_{HD;STA}$	Hold time start condition. After this period the first clock pulse is generated	4		µs
t_{LOW}	The Low period of the clock	4.7		µs
t_{HIGH}	The High period of the clock	4		µs
$t_{SU;STA}$	Setup time for start condition (only relevant for a repeated start condition)	4.7		µs
$t_{HD;DAT}$	Hold time DATA for CBUS compatible masters for I^2C devices	 5 0*		 µs µs
$t_{SU;DAT}$	Setup time DATA	250		ns
t_R	Rise time of both SDA and SCL lines		1	µs
t_F	Fall time of both SDA and SCL lines		300	ns
$t_{SU;STO}$	Setup time for stop condition	4.7		µs

NOTES:
All values referenced to V_{IH} and V_{IL} levels.
* Note that a transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

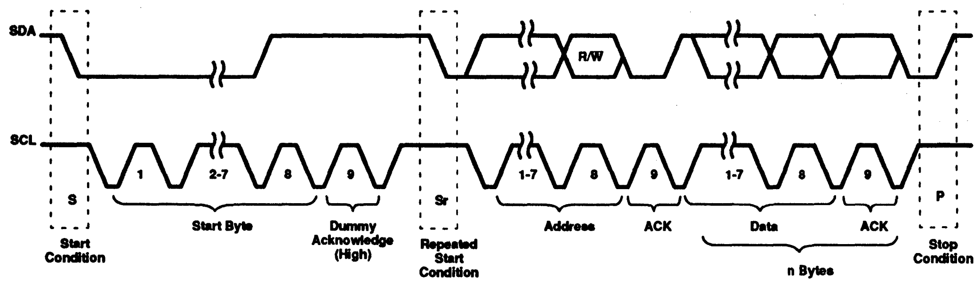


Figure 22. Data Transfer Low-Speed Mode

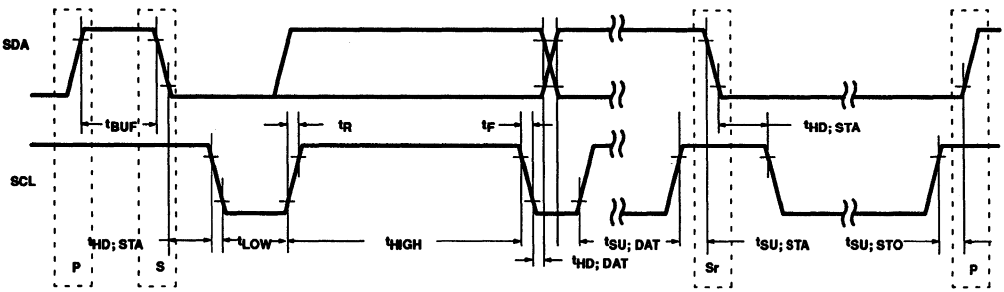


Figure 23. Timing Low-Speed Mode

I^2C Bus specification

LOW SPEED MODE

CLOCK DUTY CYCLE	: t_{LOW} = 130µs ± 25µs : t_{HIGH} = 390µs ± 25µs : 1:3 Low-to-High (Duty cycle of clock generator)
START BYTE	: 0000 0001
MAX. NO. OF BYTES	: UNRESTRICTED
PREMATURE TERMINATION OF TRANSFER	: NOT ALLOWED
ACKNOWLEDGE CLOCK BIT	: ALWAYS PROVIDED
ACKNOWLEDGMENT OF SLAVES	: OBLIGATORY

Table 3. Timing Low-Speed Mode

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
t_{BUF}	Time the bus must be free before a new transmission can start	105		µs
$t_{HD;STA}$	Hold time start condition. After this period the first clock pulse is generated	365		µs
$t_{HD;STA}$	Hold time (repeated start condition only)	210		µs
t_{LOW}	The Low period of the clock	105	155	µs
t_{HIGH}	The High period of the clock	365	415	µs
$t_{SU;STA}$	Setup time for start condition (only relevant for a repeated start condition)	105	155	µs
$t_{HD;DAT}$	Hold time DATA for CBUS compatible masters for I^2C devices	 5 0*		 µs µs
$t_{SU;DAT}$	Setup time DATA	250		ns
t_R	Rise time of both SDA and SCL lines		1	µs
t_F	Fall time of both SDA and SCL lines		300	ns
$t_{SU;STO}$	Setup time for stop condition	105	155	µs

NOTES:

All values referenced to V_{IH} and V_{IL} levels.

* Note that a transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

I²C Bus specification

APPENDIX 1

Maximum and minimum values of the pull-up resistors R_P and series resistors R_S (see Figure 20).

In an I²C bus system these values depend on the following parameters:

- Supply voltage
- Bus capacitance
- Number of devices (input current + leakage current)

1. The supply voltage limits the minimum value of the R_P resistor due to the specified 3mA as minimum sink current of the output stages, at 0.4V as maximum low voltage. In graph 1, V_{DD} against R_{Pmin} is shown.

The desired noise margin of 0.1 V_{DD} for the low level limits the maximum value of R_S.

In Graph 2, R_{Smax} against R_P is shown.

2. The bus capacitance is the total capacitance of wire, connections, and pins. This capacitance limits the maximum value of R_P because of the specified rise time of 1µs.

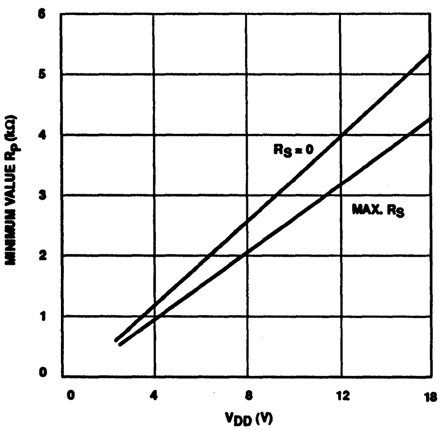
In Graph 3, the bus capacitance-R_{Pmax} relationship is shown.

3. The maximum high-level input current of each input/output connection has a specified value of 10µA max. Due to the desired noise margin of 0.2 V_{DD} for the high level, this input current limits the maximum value of R_P. This limit is dependent on V_{DD}.

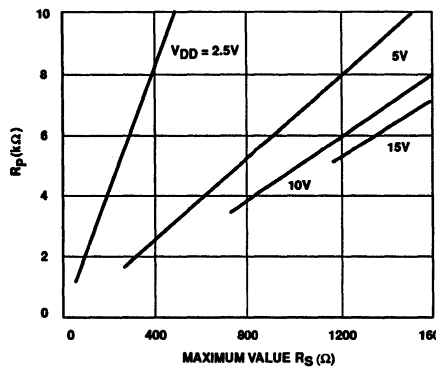
In Graph 4 the total high-level input current-R_{Pmax} relationship is shown.

I²C LICENSE

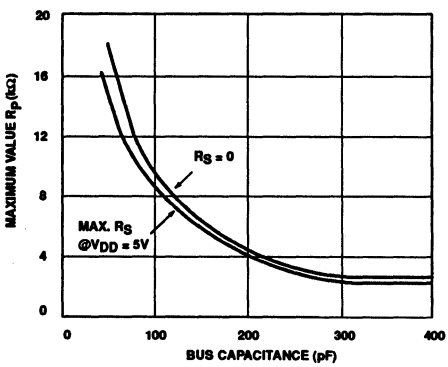
Purchase of Signetics or Philips I²C components conveys a license under the Philips I²C patent rights to use these components in an I²C system, provided that the system conforms to the I²C standard specification as defined by Philips.



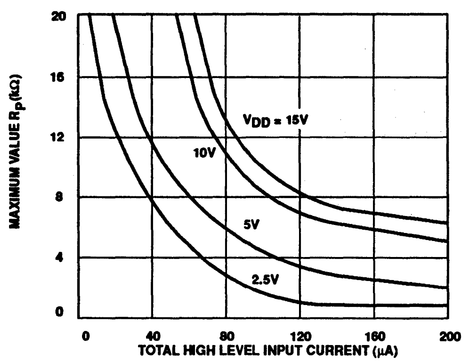
Graph 1



Graph 2



Graph 3



Graph 4

The inter-integrated circuit (I^2C) serial bus: theory and practical consideration

AN168

Author: Carl Fenger

INTRODUCTION

The I^2C (Inter-IC) bus is becoming a popular concept which implements an innovative serial bus protocol that needs to be understood. On the hardware level I^2C is a collection of microcomputers (MAB8400, PCD3343, 83C351, 84CXX) and peripherals (LCD/LED drivers, RAM, ROM, clock/timer, A/D, D/A, IR transcoder, I/O, DTMF generator, and various tuning circuits) that communicate serially over a two-wire bus, serial data (SDA) and serial clock (SCL). The I^2C structure is optimized for hardware simplicity. Parallel address and data buses inherent in conventional systems are replaced by a serial protocol that transmits both address and bidirectional data over a 2-line bus. This means that interconnecting wires are reduced to a minimum; only V_{CC}, ground and the two-wire bus are required to link the controller(s) with the peripherals or other controllers. This results in reduced chip size, pin count, and interconnections. An I^2C system is therefore smaller, simpler and cheaper to implement that its parallel counterpart.

The data rate of the I^2C bus makes it suited for systems that do not require high speed. An I^2C controller is well suited for use in systems such as television controllers, telephone sets, appliances, displays or applications involving human interface. Typically an I^2C system might be used in a control function where digitally-controllable elements are adjusted and monitored via a central processor.

The I^2C bus is an innovative hardware interface which provides the software designer the flexibility to create a truly multi-master environment. Built into the serial interface of the controllers are status registers which monitor all possible bus conditions: bus free/busy, bus contention, slave acknowledgement, and bus interference. Thus an I^2C system might include several controllers on the same bus each with the ability to asynchronously communicate with peripherals or each other. This provision also provides expandability for future add-on controllers. (The I^2C system is also ideal for use in environments where the bus is subject to noise. Distorted transmissions are immediately detected by the hardware and the information presented to the software.) A slave acknowledgement on every byte also facilitates data integrity.

An I^2C system can be as simple or sophisticated as the operating environment demands. Whether in a single master or multi-master system, noisy or 'safe', correct system operation can be insured under software control.

CONTROLLERS

Currently the family of I^2C controllers include the MAB8400, and the PCD3343 (the PCD3343 is basically a CMOS version of the MAB8400). The MAB8400 is based on the 8048, with a few instructions added and a few deleted. Tables 1 and 2 summarize the differences.

Programs for the MAB8400 and PCD3343 may be assemmbled on an 8048-assembler using the macros listed in Appendix A. The serial I/O instructions involve moving data to and from the S0, S1, and S2 serial I/O control registers. The block diagram of the I^2C interface is shown in Figure 1.

SERIAL I/O INTERFACE

A block diagram of the Serial Input/Output (SIO) is shown in Figure 1. The clock line of the serial bus (SCL) has exclusive use of Pin 3, while the Serial Data (SDA) line shares Pin 2 with parallel I/O signal P23 of port 2. Consequently, only three I/O lines are available for port 2 when the I^2C interface is enabled.

Communication between the microcomputer and interface takes place via the internal bus of the microcomputer and the Serial Interrupt Request line. Four registers are used to store data and information controlling the operation of the interface:

- data shift register S0
- address register S0'
- status register S1
- clock control register S2

THE I^2C BUS INTERFACE SERIAL CONTROL REGISTERS S0, S1

All serial I^2C transfers occur between the accumulator and register S0. The I^2C hardware takes care of clocking out/in the data, and receiving/generating an acknowledge. In addition, the state of the I^2C bus is controlled and monitored via the bus control register S1. A definition of the registers is as follows:

Table 1. MAB8400 Family Instructions not in the MAB8048 Instruction Set

SERIAL I/O	REGISTER	CONTROL	CONDITIONAL BRANCH

MOV A,Sn
MOV Sn,A
MOV Sn,#data
EN SI
DIS SI
	DEC @Rr
	DJNZ @Rr,addr
		SEL MB2
		SEL MB3
			JNTF addr

Table 2. MAB8048 Instructions not in the MAB8400 Family Instruction Set

DATA MOVES	FLAGS	BRANCH	CONTROL

MOVX A,@R
MOVX @R,A
MOVP3 A,@A
MOVD A,P
MPVD P,A
ANLD P,A
ORLD P,A
	CLR F0
	CPL F0
	CLR F1
	CPL F1
		*JNI addr
		JF0 addr
		JF1 addr
		
		*replaced by JT0, JNT0
			ENTOCLK

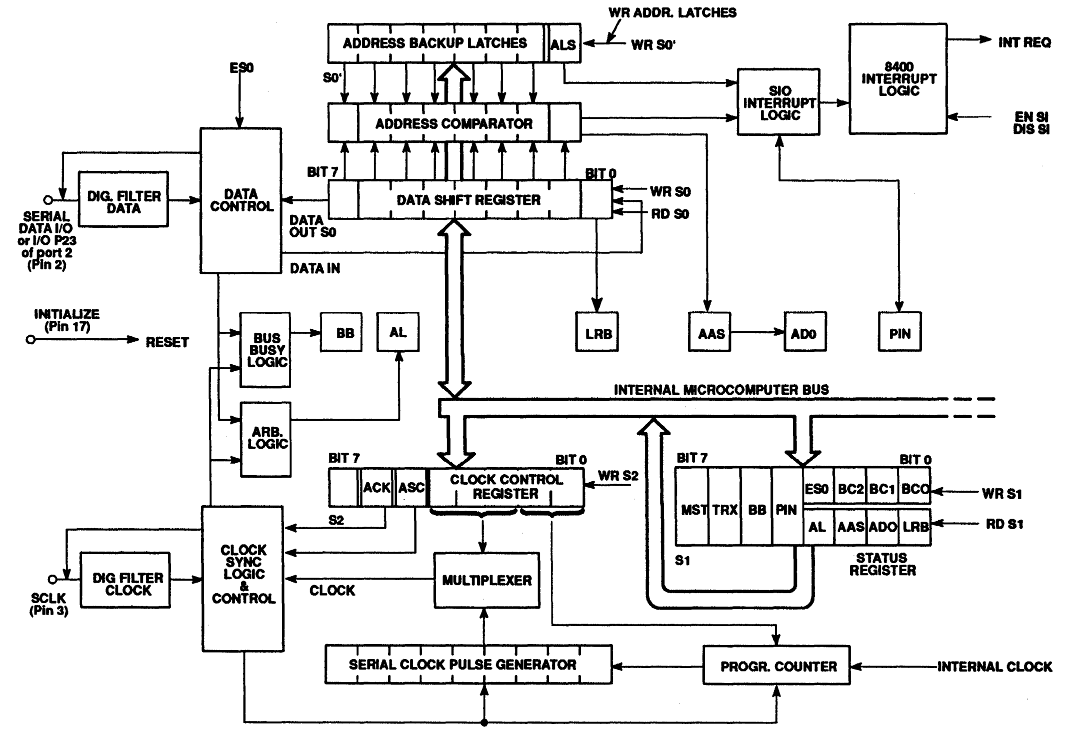


Figure 1. Block Diagram of the MAB8400 SIO Interface

Data Shift Register S0 – S0 is the data shift register used to perform the conversion between serial and parallel data format. All transmissions or receptions take place through register S0 MSB first. All I²C bus receptions or transmissions involve moving data to/from the accumulator from/to S0.

Address Register S0' – In multi-master systems, this register is loaded with a controller's slave address. When activated, (ALS = 0), the hardware will recognize when it is being addressed by setting the AAS (Addressed As Slave) flag. This provision allows a master to be treated as a slave by other masters on the bus.

Status Register S1 – S1 is the bus status register. To control the SIO interface, information is written to the register. The lower 4 bits in S1 serve dual purposes; when written to, the control bits ES0, BC2, Bc1, Bc0 are programmed (Enable Serial Output and a 3-bit counter which indicates the current number of bits left in a serial transfer). When reading the lower four bits, we obtain the status information AL, AAS, AD0, LRB (Arbitration Lost, Addressed As Slave, Address Zero (the general call has been received), the Last Received Bit (usually the acknowledge bit)). The upper 4 bits are the MST, TRX, BB and PIN control bits (Master, Transmitter, Bus Busy, and Pending Interrupt Not). These bits define what role the controller has at any particular time. The values of the master and transmitter bits define the controller as either a master or slave (a master initiates a transfer and generates the serial clock; a slave does not), and as a transmitter or receiver. Bus Busy keeps track of whether the bus is free or not, and is set and reset by the 'Start' and 'Stop' conditions which will be defined. Pending Interrupt Not is reset after the completion of a byte transfer + acknowledge, and can be polled to indicate when a serial transfer has been completed. An alternative to polling the PIN bit is to enable the serial interrupt; upon completion of a byte transfer, an interrupt will vector program control to location 07H.

SERIAL CLOCK/ACKNOWLEDGE CONTROL REGISTER S2

Register S2 contains the clock-control register and acknowledge mode bit. Bits S20-S24 program the bus clock speed. Bit S26 programs the acknowledge or not-acknowledge mode (1/0). The various

I²C bus clock speed possibilities are shown in Table 3.

Table 3. Clock Pulse Frequency Control When Using a 4.43MMHz Crystal

HEX S20-S24 CODE	DIVISOR	APPROX. f_{CLOCK} (kHz)
0	0	0
1	39	114
2	45	98
3	51	87
4	63	70
5	75	59
6	87	51
7	99	45
8	123	36
9	147	30
A	171	26
B	195	23
C	243	18
D	291	15
E	339	13
F	387	11
10	483	9.2
11	579	7.7
12	675	6.6
13	771	5.8
14	963	4.6
15	1155	3.8
16	1347	3.3
17	1539	2.9
18*	1923	2.3
19*	2307	1.9
1A*	2691	1.7
1B*	3075	1.4
1C	3843	1.2
1D	4611	1.0
1E	5379	0.8
1F	6147	0.7

*only values that may be used in the low speed mode (ASC = 1)

These speeds represent the frequency of the serial clock bursts and do not reflect the speed of the processor's main clock (i.e., it controls the bus speed and has no effect on the CPU's execution speed).

BUS ARBITRATION

Due to the wire-AND configuration of the I²C bus, and the self-synchronizing clock circuitry of I²C masters, controllers with varying clock speeds can access the bus without clock contention. During arbitration, the resultant clock on the bus will have a low period equal to the longest of the low periods; the high period will equal the shortest of the high periods. Similarly, when two masters attempt to drive the data line simultaneously, the data is 'ANDed', the master generating a low while the other is driving a high will win arbitration. The resultant bus level will be low, and the loser will withdraw from the bus and set its 'Arbitration Lost' flag (S1 bit 3).

The losing Master is now configured as a slave which could be addressed during this very same cycle. These provisions allow for a number of microcomputers to exist on the same bus. With properly written subroutines, software for any one of the controllers may regard other masters as transparent.

I²C PROTOCOL AND ASSEMBLY LANGUAGE EXAMPLES

I²C data transfers follow a well-defined protocol. A transfer always takes place between a master and a slave. Currently a microcomputer can be master or slave, while the 'CLIPS' peripherals are always salves. In a 'bus-free' condition, both SCL and SDA lines are kept logical high be external pull-up resistors. All bus transfers are bounded by a 'Start' and a 'Stop' condition. A 'Start' condition is defined as the SDA line making a high-to-low transition **while the SCL line is high**. At this point, the internal hardware on all slaves are activated and are prepared to clock-in the next 8 bits and interpret it as a 7-bit address and a R/$\overline{W}$ control bit (MSB first). All slaves have an internal address I²C data transfers follow a well-defined protocol. A transfer always takes place between a master and a slave. Currently a microcomputer can be master or slave, while the 'CLIPS' peripherals are always salves. In a 'bus-free' condition, both SCL and SDA lines are kept logical high be external pull-up resistors. All bus transfers are bounded by a 'Start' and a 'Stop' condition. A 'Start' condition is defined as the SDA line making a high-to-low transition **while the SCL line is high**. At this point, the internal hardware on all slaves are activated and are prepared to clock-in the next 8 bits and interpret it as a 7-bit address and a R/$\overline{W}$ control bit (MSB first). All slaves have an internal address (most have 2 – 3 programmable address bits) which is then compared with the received address. The slave that recognized its address will respond by pulling the data line low during a ninth clock generated by the master (all I²C byte transfers require the master to generate 8 clock pulses plus a ninth acknowledge-related clock pulse). The slave-acknowledge will be registered by the master as a '0' appearing in the LRB (Last Received Bit) position of the S1 serial I/O status register. If this bit is high after a transfer attempt, this indicates that a slave did not acknowledge and that the transfer should be repeated.

After the desired slave has acknowledged its address, it is ready to either send or receive data in response to the master's driving clock. All other slaves have withdrawn from the bus. In addition, for multi-master systems, the start condition has set the 'Bus Busy' bit of the serial I/O register S1 on all masters on the bus. This gives a software indication to other master that the bus is in use and to wait until the bus is free before attempting an access.

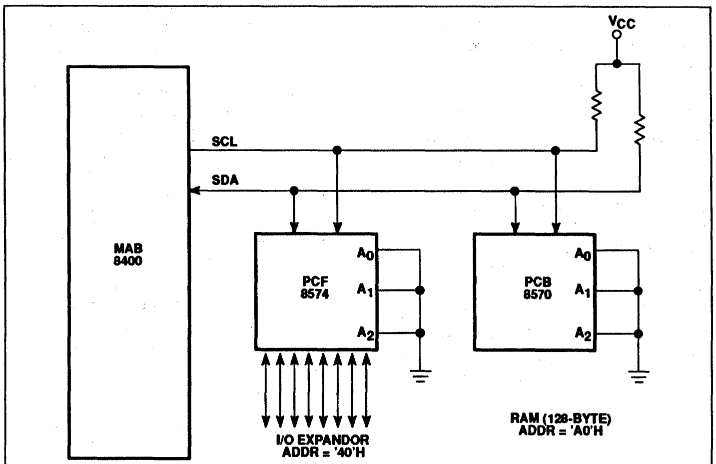


Figure 2. Schematic for Assembly Examples

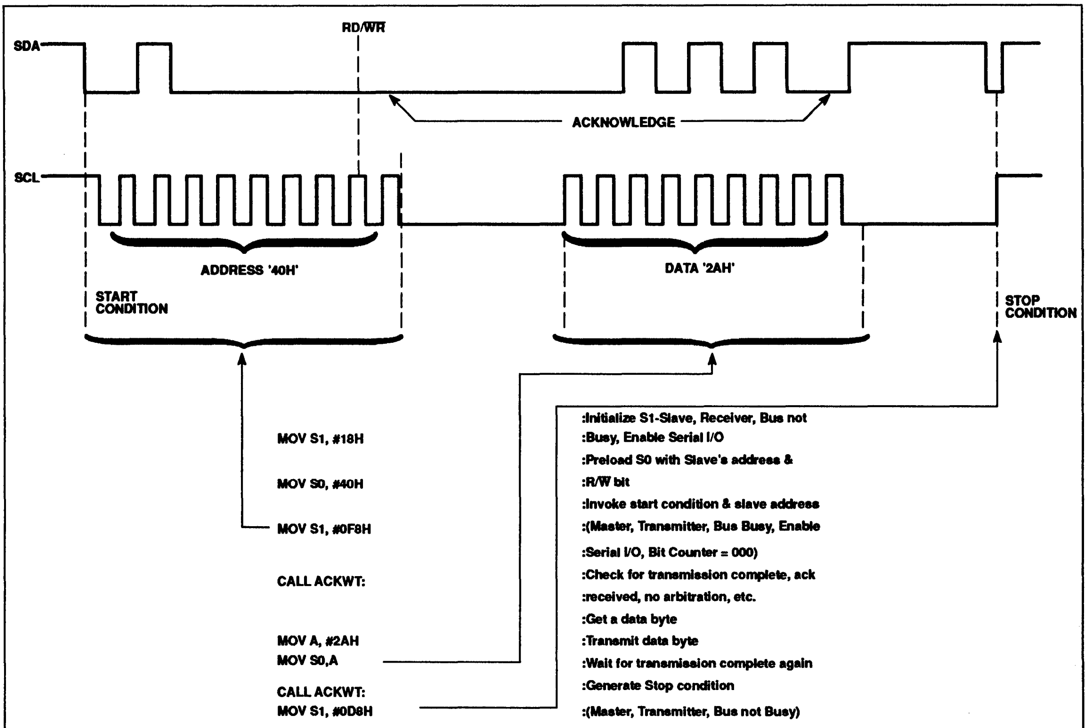


Figure 3

There are two types of I²C peripherals that now must be defined: there are those with only a chip address such as the I/O expandor, PCF8574, and those with a chip address plus an internal address such as the static RAM, PCF8570. Thus after sending a start condition, address, and R/W bit, we must take into account what type of slave is being addressed. In the case of a slave with only a chip address, we have already indicated its address and data direction (R/W) and are therefore ready to send or receive data. This is performed by the master generating bursts of 9 clock pulses for each byte that is sent or received. The transaction for writing one byte to a slave with a chip address only is shown in Figure 3.

In this transfer, all bus activity is invoked by writing the appropriate control byte to the serial I/O control register S1, and by moving data to/from the serial bus buffer register S0. Coming from a known state (MOV S1, #18H-Slave, Receiver, Bus not Busy) we first load the serial I/O buffer S0 with the desired slave's address (MOV S0, #40H). To transmit this preceded by a start condition, we must first examine the control register S1, which, after initialization, looks like this:

MASTER	TRANS	BUS BUSY	PIN	ESO	BC2	BC1	BC0
0	0	0	1	1	0	0	0

To transmit to a slave, the Master, Transmitter, Bus Busy, PIN (Pending Interrupt Not), and ESO (Enable Serial Output) must be set to a 1. This results in an 'F8H' being written to S1. This word defines the controller as a Master Transmitter, invokes the transfer by setting the 'Bus Busy' bit, clears the Pending Interrupt Not (an inverted flag indicating the completion of a compete byte transfer), and activates the serial output logic by setting the Enable Serial Output (ESO) bit.

BIT COUNTER S12, S11, S10

BC2, BC1 and BC0 comprise a bit-counter which indicates to the logic how long the word is to be clocked out over the serial data line. By setting this to a 000H, we are telling

Table 4. Binary Numbers in Bit-Count Locations BC2, BC1 and BC0

BC2	BC1	BC0	BITS/BYTE WITHOUT ACK	BITS/BYTE WITH ACK
0	0	1	1	2
0	1	0	2	3
0	1	1	3	4
1	0	0	4	5
1	0	1	5	6
1	1	0	6	7
1	1	1	7	8
0	0	0	8	9

it to produce 9 clocks (8 bits plus an acknowledge clock) for this transfer. The bit counter will then count off each bit as it is transmitted. The bit counter possibilities are shown in Table 4.

Thus the bit counter keeps track of the number of clock pulses remaining in a serial transfer. Additionally, there is a not-acknowledge mode (controlled through bit 6 of clock control register S2) which inhibits the acknowledge clock pulse, allowing the possibility of straight serial transfer. We may thus define the word size for a serial transfer (by pre-loading BC2, BC1, BC0 with the appropriate control number), with or without an acknowledge-related clock pulse being generated. This makes the controller able to transmit serial data to most any serial device regardless of its protocol (e.g., C-bus devices).

CHECKING FOR SLAVE ACKNOWLEDGE

After a 'Start' condition and address have been issued, the selected slave will have recognized and acknowledged its address by pulling the data line low during the ninth clock pulse. During this period, the software (which runs on the processor's 4MHz clock) will have been either waiting for the transfer to be completed by polling the PIN bit in S1 which goes low on completion of a transfer/reception (whose length is defined by the pre-loaded Bit-counter value), or by the hardware in Serial Interrupt mode. The serial interrupt (vectored to 07H) is enabled via the EN SI (enable serial interrupt) instruction.

At the point when PIN goes low (or the serial interrupt is received) the 9-bit transfer has been completed. The acknowledgement bit will now be in the LRB position of register S1, and may be checked in the routine 'ACKWT' (Wait for Acknowledge) as shown in Figure 4.

This routing must go one step further in multi-master systems; the possibility of an Arbitration Lost situation may occur if other masters are present on the bus. This condition may be detected by checking the 'AL' bit (bit 3). If arbitration has been lost, provisions for re-attempting the transmission should be taken. If arbitration is lost, there is the possibility that the controller is being addressed as a Slave. If this condition is to be recognized, we must test on the 'AAS' bit (bit 2). A 'General Call' address (00H) has also been defined as an 'all-call' address for all slaves; bit1, AD0, must be tested if this feature is to be recognized by a Master.

```
ACKWT:   MOV A,S1        ;Get bus status word
                         ;from S1.
         JB4 ACKWT       ;Poll the PIN bit
                         ;until it goes low
                         ;indicating transfer
                         ;completed
         JBO BUSERR      ;Jump to BUSERR
                         ;routine if acknowledge
                         ;not received.
         RET             ;transfer complete,
                         ;acknowledge received – return.
```

Figure 4

After a successful address transfer/acknowledge, the slave is ready to be sent its data. The instruction MOV S0,A will now automatically send the contents of the accumulator out on the bus. After calling the ACKWT routine once more, we are ready to terminate the transfer. The Stop condition is created by the instruction 'MOV S1, #0D8H'. This re-sets the bus-busy bit, which tells the hardware to generate a Stop – the data line makes a low-to-high transition while the clock remains high. All bus-busy flags on other masters on the bus are reset by this signal.

The transfer is now complete – PCF8574 I/O Expandor will transfer the serial data stream to its 8 output pins and latch them until further update.

MASTER READS ONE BYTE FROM SLAVE

A read operation is a similar process; the address, however, will be 41H, the LSB indicating to the I/O device that a read is to be performed. During the data portion of a read, the I/O port 8574 will transmit the contents of its latches in response to the clock generated by the master. The Master/Receiver in this case generates a low-level acknowledge on reception of each byte (a 'positive' acknowledge). Upon completion of a read, the master must generate a 'negative' acknowledge during the ninth clock to indicate to the slaves that the read operation is finished. This is necessary because an arbitrary number of bytes may be read within the same transfer. A negative acknowledge consists of a high signal on the data line during the ninth clock of the last byte to be read. To accomplish this, the master 8400 must leave the acknowledge mode just before the final byte, read the final byte (producing only 8 clock pulses), program the bit-counter with 001 (preparing for a one-bit negative acknowledge pulse), and simply move the contents of S0 to the accumulator. This final instruction accomplishes two things simultaneously: it transfers the final byte to the accumulator and produces one clock pulse on the SCL line. The structure of the serial I/O register S0 is such that a read from it causes a double-buffered transfer from the I^2C bus to S0, while the original contents of S0 are transferred to the accumulator. Because the number of clocks produced on the bus is determined by the control number in the Bit Counter, by presetting it to 001, only one clock is generated. At this point in time the slave is still waiting for an acknowledge; the bus is high due to the pull-up, as single clock pulse in this condition is interpreted as a 'negative' acknowledge. The slave has now been informed that reading is completed, a Stop condition is now generated as before. The read process (one byte from a slave with only a chip address) is shown in Figure 5.

These examples apply to a slave with a chip address – more than one byte can be written/read within the same transfer; however, this option is more applicable to I^2C devices with sub-addresses such as the static RAMs or Clock/Calendar. In the case of these types of devices, a slightly different protocol is used. The RAM, for example, requires a chip address and an internal memory location before it can deliver or accept a byte of information. During a write operation, this is done by simply writing the secondary address right after the chip address – the peripheral is designed to interpret the second byte as an internal address. In the case of a Read operation, the slave peripheral must send data back tot he Master after it has been addressed and sub-addressed. To accomplish this, first the Start, Address, and Sub-address is transmitted. Then we have repeated start condition to reverse the direction of the data transfer, followed by the chip address and RD, than a data string (w/acknowledges). This repeated Start does not affect other peripherals – they have been deactivated and

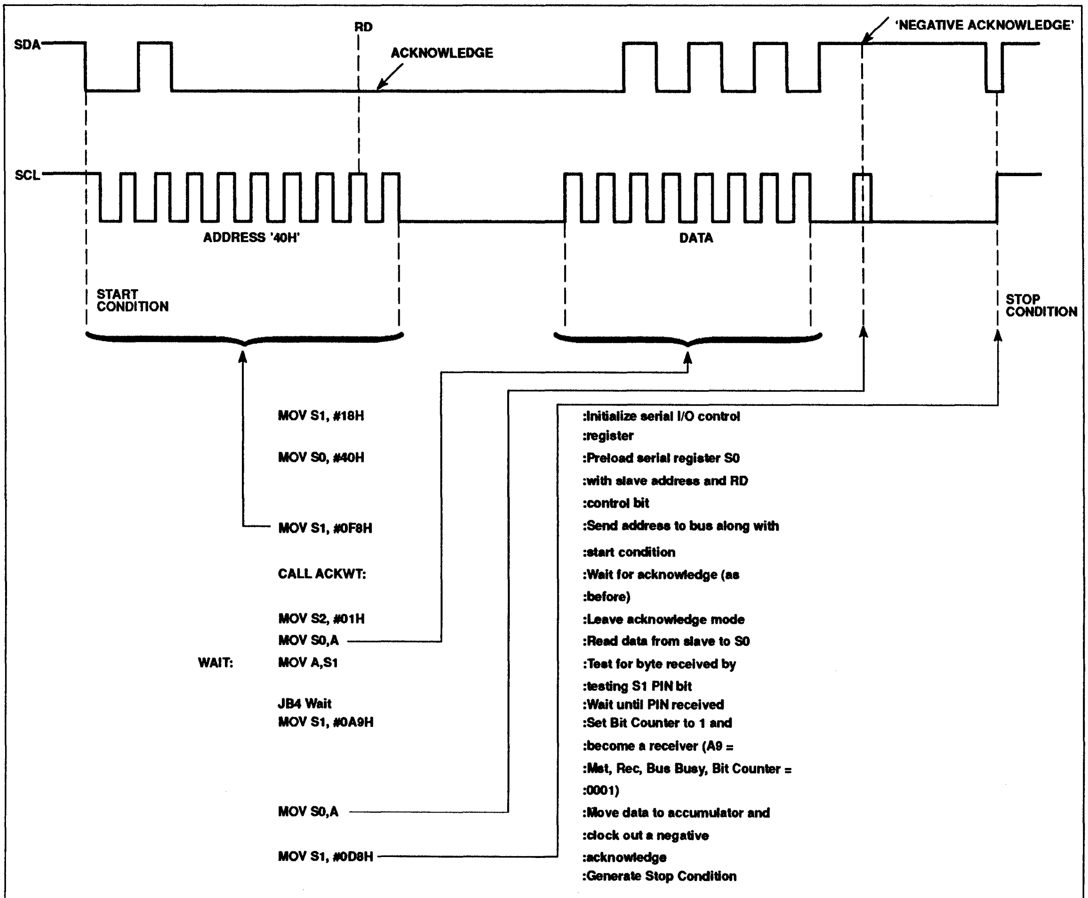

SDA
SCL
RD
ACKNOWLEDGE
'NEGATIVE ACKNOWLEDGE'
ADDRESS '40H'
DATA
START CONDITION
STOP CONDITION
MOV S1, #18H
MOV S0, #40H
MOV S1, #0F8H
CALL ACKWT:
MOV S2, #01H
MOV S0,A
WAIT: MOV A,S1
JB4 Wait
MOV S1, #0A9H
MOV S0,A
MOV S1, #0D8H
:Initialize serial I/O control
:register
:Preload serial register S0
:with slave address and RD
:control bit
:Send address to bus along with
:start condition
:Wait for acknowledge (as
:before)
:Leave acknowledge mode
:Read data from slave to S0
:Test for byte received by
:testing S1 PIN bit
:Wait until PIN received
:Set Bit Counter to 1 and
:become a receiver (A9 =
:Mst, Rec, Bus Busy, Bit Counter =
:0001)
:Move data to accumulator and
:clock out a negative
:acknowledge
:Generate Stop Condition

Figure 5

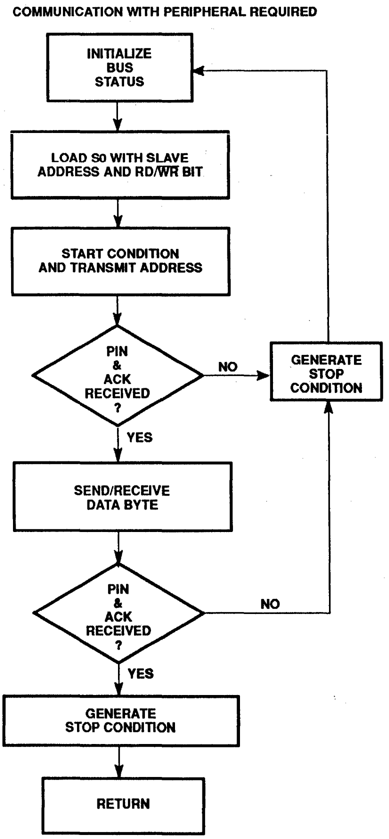


Figure 6. Flowchart for Reading/Writing One Byte to an I^2C Peripheral; Single-Master, Single-Address Slave

```
        MOV S1, #18H        :Initialize bus-status register
                            :Master, Transmitter,
                            :Bus-not-Busy, Enable SIO,
        MOV S0, #0A0H       :Load S0 with RAM's chip
                            :address
        MOV S1, #0F8H       :Start cond. and transmit
                            :address
        CALL ACKWT          :Wait until address received
        MOV A, #00H         :Set up for transmitting RAM
                            :location address
        MOV S0,A            :Transmit first RAM address
        CALL ACKWT          :Wait
        MOV S1, #18H        :Set up for a repeated Start
                            :condition
        MOV A, #0A1H        :Get RAM chip address & RD bit
        MOV SO, A           :Send out to bus
        MOV S1, #0F8H       :preceded by repeated Start

        CALL ACKWT          :Wait
        MOV A,S0            :First data byte to S0
        CALL ACKWT          :Wait
        MOV A,S0            :Second data byte to S0
                            :And First data byte to Acc.
        CALL ACKWT          :Wait
        MOV R0,A            :Save first byte in R0
        MOV A,S0            :Third data byte to S0
                            :and second data byte to Acc.
        CALL ACKWT          :Wait
        MOV R1,A            :Save second data byte
                            :in R1
        MOV S2, #01H        :Leave ack. mode
                            :Bit Counter=001 for neg ack.
        MOV A,S0            :Third data byte to acc
                            :negative ack. generated
        MOV R2,A            :Save third data byte in R2
WAIT1:  MOV A,S1            :Get bus status
        JB4 WAIT1           :Wait until transfer complete
        MOV S1, #0D8H       :Stop condition
        MOV S2, #41H        :Restore acknowledge mode
```

Figure 7

will not reactivate until a Stop condition is detected. I^2C peripherals are equipped with auto-incrementing logic which will automatically transmit or receive data in consecutive (increasing) locations. For example, to read 3 consecutive bytes to PCB8571 RAM locations 00, 01 and 02, we use the following format as shown in Figure 7.

This routine reads the contents of location 00, 01 and 02 of the PCB8571 128-byte RAM and puts them in registers R0, R1, and R2. The auto-incrementing feature allows the programmer to indicate only a starting location, then read an arbitrary block of consecutive memory addresses. The WAIT 1 loop is required to poll for the completion of the final byte because the ACKWT routine will not recognize the negative acknowledge as a valid condition.

BUS ERROR CONDITIONS: ACKNOWLEDGE NOT RECEIVED

In the above routines, should a slave fail to acknowledge, the condition is detected during the 'ACKWT' routine. The occurrence may indicate one of two conditions: the slave has failed to operate, or a bus disturbance has occurred. The software response to either event is dependent on the system application. In either case, the 'BusErr' routine should reinitialize the bus by issuing a 'Stop' condition. Provision may then be taken to repeat the transfer an arbitrary number of times. Should the symptom persist, either an error condition will be entered, or a backup device can be activated.

These sample routines represent single-master systems. A more detailed analysis of multi-master/noisy environment systems will be treated in further application notes. Examples of more complex systems can be found in the 'Software Examples' manual; publication 9398 615 70011.

APPENDIX A

Only the 8048 assembler is capable of assembling MAB8400 source code when it has at least a "DATA" or "Define Byte" assembler directive, possibly in combination with a MACRO facility.

The new instructions can be simply defined by MACROs. The instructions which are not in the MAB8400 should not be in the MAB8400 source program.

An example of a macro definitions list is given here for the Intel Macro Assembler.

This list can be copied in front of a MAB8400 source program; the new instructions are added to the MAB8400 via its name in the op-code field and (if required) followed by an operand in the operand field.

MACRO DEFINITIONS

```
LINE                                 SOURCE STATEMENT

$MACROFILE
;MACROS FOR 8048 ASSEMBLER RECOGNITION
;OF 8400 COMMANDS
                            MOVS0A      MACRO       ;MOV S0,A
                            DB 3CH
                            ENDM
                            MOVAS0      MACRO       ;MOV A,S0
                            DB 0CH
                            ENDM
                            MOVS1A      MACRO       ;MOV S1,A
                            DB 3DH
                            ENDM
                            MOVAS1      MACRO       ;MOV A,S1
                            DBODH
                            ENDM
                            MOVS2A      MACRO       ;MOV S2,A
                            DB 3EH
                            ENDM
                            MOVS0       MACRO L     ;MOV S0,#DATA
                            DB 9CH,L
                            ENDM
                            MOVS1       MACRO L     ;MOV S1,#DATA
                            DB 9DH,L
                            ENDM
                            MOVS2       MACRO L     ;MOV S2,#DATA
                            DB 9EH,L
                            ENDM
                            ENSI        MACRO       ;EN SI
                            DB 85H
                            ENDM
                            DISSI       MACRO       ;DIS SI (Disable serial interrupt)
                            DB          95H
                            ENDM
;
;PORT 0 INSTRUCTIONS:
;                           INAP0       MACRO       ;IN A,P0
                            DB          08H
                            ENDM
;
                            OUTP0A      MACRO       ;OUTL P0,A
                            DB          38H
                            ENDM
;
                            ORLP0       MACRO L     ;ORL P0,#DATA
                            DB          88H,L
                            ENDM
;
                            ANLP0       MACRO L     ;ANL P0,#DATA
                            DB          98H,L
                            ENDM
;
```

MACRO DEFINITIONS (Continued)

LINE SOURCE STATEMENT

```
 DATA MEMORY INSTRUCTIONS;
                      DECAR0     MACRO       ;DEC @R0
                      DB         0C0H
                      ENDM
;
                      DECAR1     MACRO       ;SEL MB2
                      DB         0A5H
                      ENDM
;
 SELECT MEMORY BANK INSTRUCTIONS:
                      SELMB2     MACRO       ;SEL MB2
                      DB         0C1H
                      ENDM
;
                      SELMB3     MACRO       ;SEL MB3
                      DB         0B5H
                      ENDM
;
;CONDITIONAL JUMP INSTRUCTIONS:
                      DJNZA0     MACRO L     ;DJNZ @R0,ADDR
                      DB         0E0H,L AND 0FFH
                      ENDM
;
                      DJNZA1     MACRO L     ;DJNZ @R1,ADDR
                      DB         0E1H,L AND 0FFH
                      ENDM
;
                      JNTF       MACRO L     ;JUMP IF TIMERFLAG IS
                                              NON ZERO
                      DB         06H,L AND 0FFH
                      ENDM

;END OF MACRO DEFINITIONS
```

THE 8400 INSTRUCTIONS BUILT FROM THE MACRO LIST

LOC/OBJ	LINE	SOURCE STATEMENT		
0000	1	ORG 0		
	2	MOVASO		
0000 0C	3+	DB	0CH	
		MOVAS1		;MACRO for MOV A,S1
0001 0D	5+	DB	0DH	
	6	MOVS0A		;MACRO for MOV S0,A
0002 3C	7+	DB	3CH	
	8	MOVS1A		;MACRO for MOV S1,A
0003 3D	9+	DB	3DH	
	10	MOVS2A		;MACRO for MOV S2,A
0004 3E	11+	DB	3EH	
	12	MOVS0	56H	;MACRO for MOV S0,#56H
0005 9C	13+	DB	9CH,56H	
0006 56				
	14	MOVS1	9FH	;MACRO for MOV S1,#9FH
0007 9D	15+	DB	9DH,9FH	
0008 9F				
	16	MOVS2	0E8H	;MACRO for MOV S2,#0E8H
0009 9E	17+	DB	9EH,0E8H	
000A E8				
	18	ENS1		;MACRO for EN S1
000B 85	19+	DB	85H	
	20	DISSI	;MACRO for DIS SI	
000C 95	21+	DB	95H	
	22	INAPO		;MACRO for IN A,P0
000D 08	23+	DB	08H	
	24	OUTP0A		;MACRO for OUTL P0,A
000E 38	25+	DB	38H	
	26	ORLP0	5AH	;MACRO for ORL P0,A
000F 88	27+	DB	88H,5AH	
0010 5A				
	28	ANLP0	2FH	;MACRO for ANL P0,A
0011 98	29+	DB	98H,2FH	
0012 2F				
	30	DECAR0		;MACRO for DEC @R0
0013 C0	31+	DB	0C0H	
	32	DECAR1		;MACRO for DEC @R1
0014 C1	33+	DB	0C1H	
	34	SELMB2		;MACRO for SEL MB2
0015 A5	35+	DB	0A5H	
	36	SELMB3		;MACRO for SEL MB3
0016 B5	37+	DB	0B5H	
	38	DJNZA0	567H	;MACRO for DJNZ @R0,567H
0017 E0	39+	DB	0E0H,567H AND 0FFH	
0019 67				
	40	DJNZA1	0EFEH	;MACRO for DJNZ @R1,0EFEH
0019 E1	41+	DB	0E1H,0EFEH AND 0FFH	
001A FE				
	42	JNTF	789H	;MACRO for JNTF 789H
001B 06	43+	DB	06H, 789H AND 0FFH	
001C 89				
	44	END		

Signetics

Section 8
Complementary RF Products

RF Communications

INDEX

Single pole double throw (SPDT) switch

NE/SA630

DESCRIPTION

The NE630 is a wideband RF switch fabricated in BiCMOS technology and incorporating on-chip CMOS/TTL compatible drivers. Its primary function is to switch signals in the frequency range DC - 1GHz from one 50Ω channel to another. The switch is activated by a CMOS/TTL compatible signal applied to the enable channel 1 pin (ENCH1).

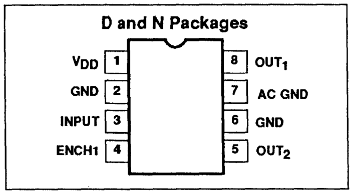
The extremely low current consumption makes the NE/SA630 ideal for portable applications. The excellent isolation and low loss makes this a suitable replacement for PIN diodes.

The NE/SA630 is available in an 8-pin dual in-line plastic package and an 8-pin SO (surface mounted miniature) package.

FEATURES

- Wideband (DC - 1GHz)
- Low through loss (1dB typical at 200MHz)
- Unused input is terminated internally in 50Ω
- Excellent overload capability (1dB gain compression point +18dBm at 300MHz)
- Low DC power (170µA from 5V supply)
- Fast switching (20ns typical)
- Good isolation (off channel isolation 60dB at 100MHz)
- Low distortion (IP_3 intercept +33dBm)
- Good 50Ω match (return loss 18dB at 400MHz)
- Full ESD protection
- Bidirectional operation

PIN CONFIGURATION



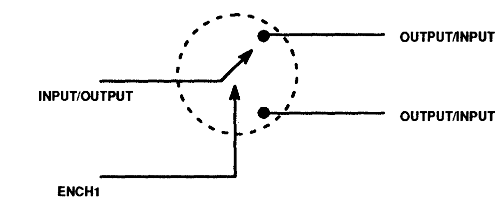
APPLICATIONS

- Digital transceiver front-end switch
- Antenna switch
- Filter selection
- Video switch
- FSK transmitter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to 70°C	NE630N
8-Pin Plastic SO (Surface-mount)	0 to 70°C	NE630D
8-Pin Plastic DIP	-40 to +85°C	SA630N
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA630D

BLOCK DIAGRAM



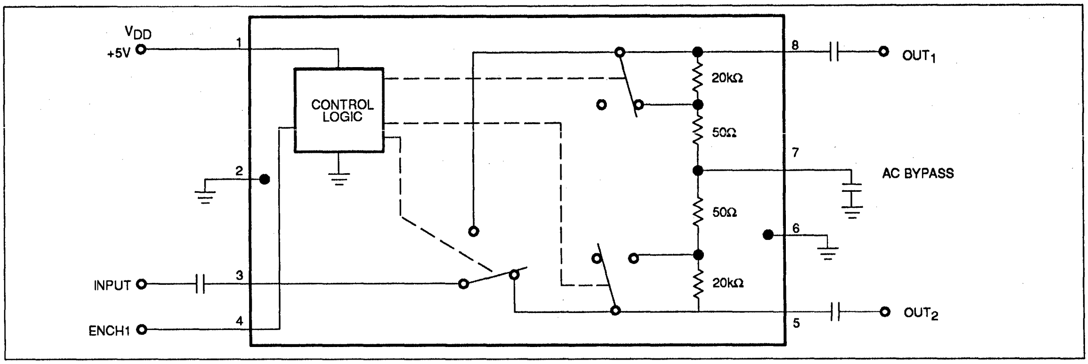
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	-0.5 to +5.5	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 8-Pin Plastic DIP 8-Pin Plastic SO	 1160 780	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin DIP: θ_{JA} = 108°C/W
   8-Pin SO: θ_{JA} = 158°C/W

EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	3.0 to 5.5V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA630 MIN	TYP	MAX	UNITS
I_{DD}	Supply current		40	170	300	µA
V_T	TTL/CMOS logic threshold voltage[1]		1.1	1.25	1.4	V
V_{IH}	Logic 1 level	Enable channel 1	2.0		V_{DD}	V
V_{IL}	Logic 0 level	Enable channel 2	-0.3		0.8	V
I_{IL}	ENCH1 input current	ENCH1 = 0.4V	-1	0	1	µA
I_{IH}	ENCH1 input current	ENCH1 = 2.4V	-1	0	1	µA

NOTE:
1. The ENCH1 input must be connected to a valid Logic Level for proper operation of the NE/SA630.

AC ELECTRICAL CHARACTERISTICS[1] - D PACKAGE

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA630 MIN	TYP	MAX	UNITS
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2	 2.8	dB
S_{21}, S_{12}	Isolation (OFF channel)[2]	10MHz 100MHz 500MHz 900MHz	70 24	80 60 50 30		dB
S_{11}, S_{22}	Return loss (ON channel)	DC - 400MHz 900MHz		20 12		dB
S_{11}, S_{22}	Return loss (OFF channel)	DC - 400MHz 900MHz		17 13		dB
t_D	Switching speed (on-off delay)	50% TTL to 90/10% RF		20		ns
t_r, t_f	Switching speeds (on-off rise/fall time)	90%/10% to 10%/90% RF		5		ns
	Switching transients			165		mV_{P-P}
P_{-1dB}	1dB gain compression	DC - 1GHz		+18		dBm
IP_3	Third-order intermodulation intercept	100MHz		+33		dBm
IP_2	Second-order intermodulation intercept	100MHz		+52		dBm
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.0		dB

NOTE:
1. All measurements include the effects of the D package NE/SA630 Evaluation Board (see Figure 1B). Measurement system impedance is 50Ω.
2. The placement of the AC bypass capacitor is critical to achieve these specifications. See the applications section for more details.

AC ELECTRICAL CHARACTERISTICS[1] - N PACKAGE

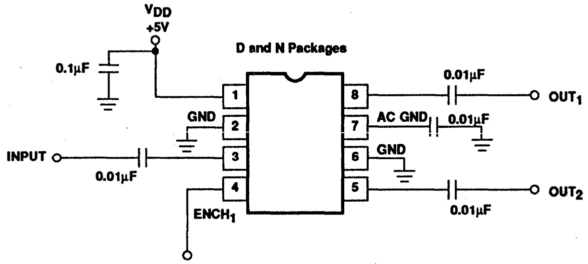
V_{DD} = +5V, T_A = 25°C; all other characteristics similar to the D-Package, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA630 MIN	TYP	MAX	UNITS
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2.5		dB
S_{21}, S_{12}	Isolation (OFF channel)	10MHz 100MHz 500MHz 900MHz	58	68 50 37 15		dB
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.5		dB

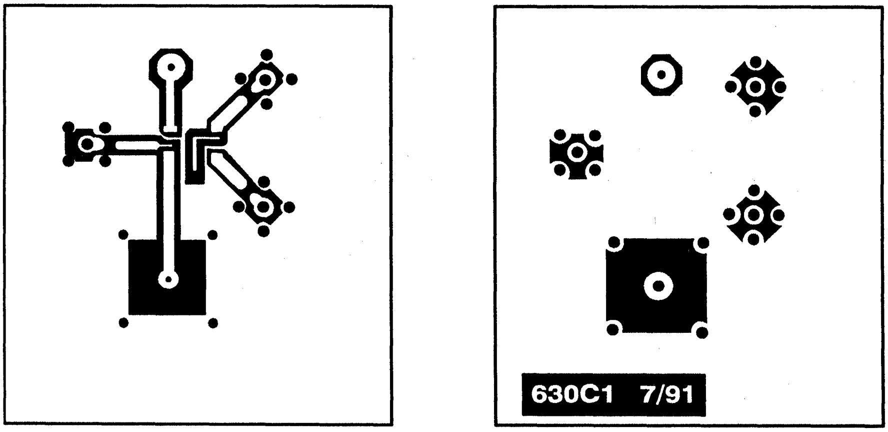
NOTE:
1. All measurements include the effects of the N package NE/SA630 Evaluation Board (see Figure 1C). Measurement system impedance is 50Ω.

APPLICATIONS

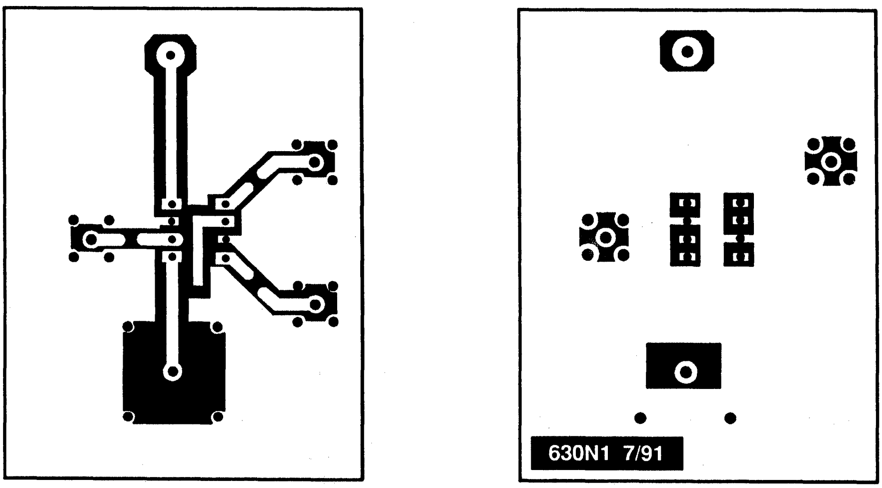
The typical applications schematic and printed circuit board layout of the NE/SA630 evaluation board is shown in Figure 1. The layout of the board is simple, but a few cautions need to be observed. The input and output traces should be 50Ω. The placement of the AC bypass capacitor is *extremely critical* if a symmetric isolation between the two channels is desired. The trace from Pin 7 should be drawn back towards the package and then be routed downwards. The capacitor should be placed straight down as close to the device as practical. For better isolation between the two channels at higher frequencies, it is also advisable to run the two output/input traces at an angle. This also minimizes any inductive coupling between the two traces. The power supply bypass capacitor should be placed close to the device. Figure 7 shows the frequency response of the NE/SA630. The loss matching between the two channels is excellent to 1.2GHz as shown in



a. NE/SA Evaluation Board Schematic



b. NE/SA630 D-Package Board Layout



c. NE/SA630 N-Package Board Layout

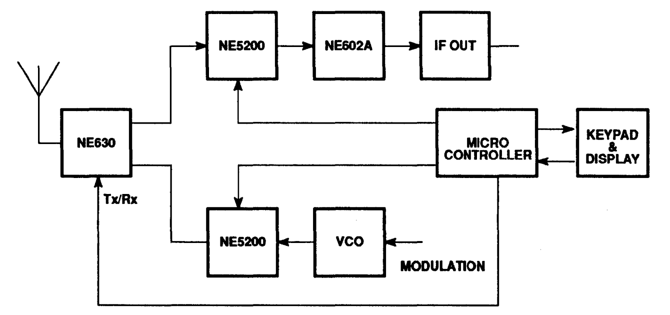
Figure 1

Figure 10. The isolation and matching of the two channels over frequency is shown in Figure 12 and Figure 14, respectively.

The NE630 is a very versatile part and can be used in many applications. Figure 2 shows a block diagram of a typical Digital RF transceiver front-end. In this application the NE630 replaces the duplexer which is typically very bulky and lossy. Due to the low power consumption of the device, it is ideally suited for handheld applications such as in CT2 cordless telephones. The NE630 can also be used to generate Amplitude Shift Keying (ASK) or On-Off Keying (OOK) and Frequency Shift Keying (FSK) signals for digital RF communications systems. Block diagrams for these applications are shown in Figure 3 and Figure 4, respectively.

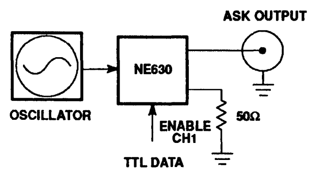
For applications that require a higher isolation at 1GHz than obtained from a single NE630, several NE630s can be cascaded as shown in Figure 5. The cascaded configuration will have a higher loss but greater than 35dB of isolation at 1GHz and greater than 65dB @ 500MHz can be obtained from this configuration. By modifying the enable control, an RF multiplexer/ de-multiplexer or antenna selector can be constructed. The simplicity of NE630 coupled with its ease of use and high performance lends itself to many innovative applications.

The NE/SA630 switch terminates the OFF channel in 50Ω. The 50Ω resistor is internal and is in series with the external AC bypass capacitor. Matching to impedances other than 50Ω can be achieved by adding a resistor in series with the AC bypass capacitor (e.g., 25Ω additional to match to a 75Ω environment).



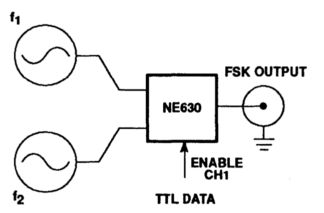
A TYPICAL TDMA/DIGITAL RF TRANSCEIVER SYSTEM FRONT-END

Figure 2



AMPLITUDE SHIFT KEYING (ASK) GENERATOR

Figure 3



FREQUENCY SHIFT KEYING (FSK) GENERATOR

Figure 4

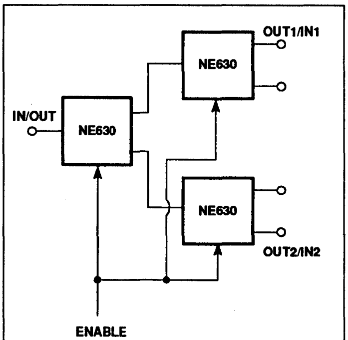


Figure 5

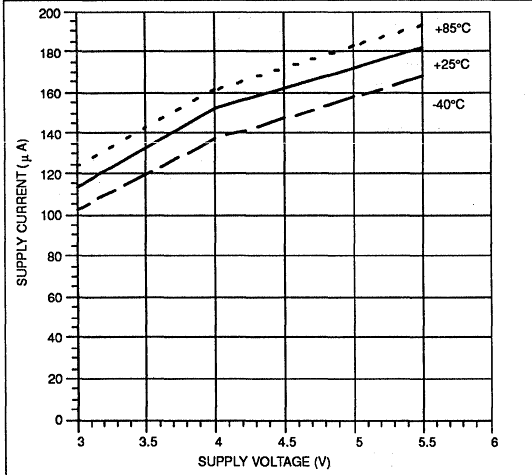


Figure 6 Supply Current vs. V_{DD} and Temperature

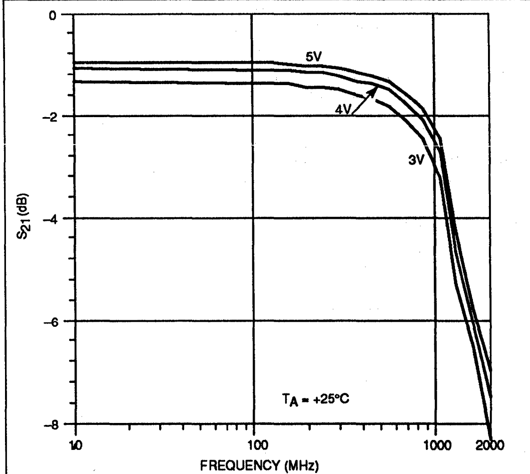


Figure 7 Loss vs. Frequency and V_{DD} for D-Package

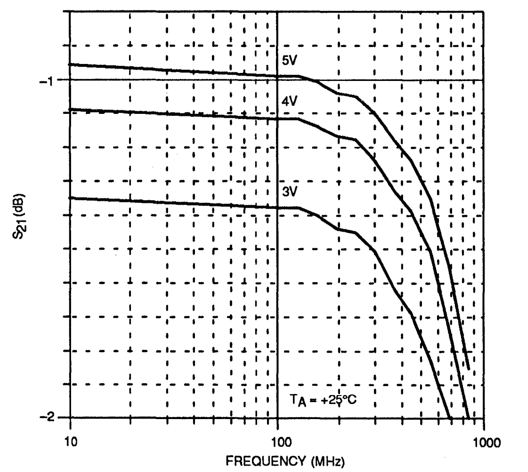


Figure 8 Loss vs. Frequency and V_{DD} for D-Package -Expanded Detail-

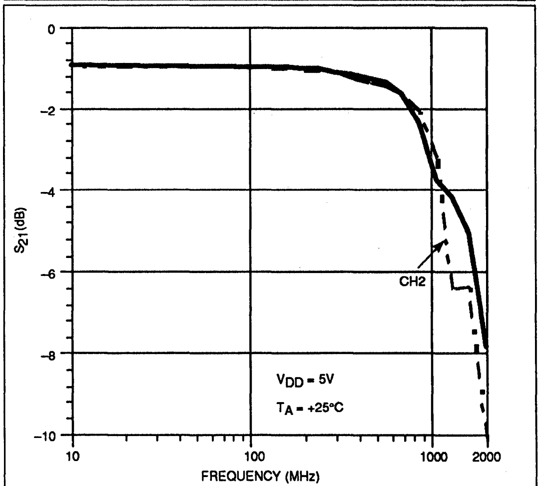


Figure 9 Loss Matching vs. Frequency for N-Package (DIP)

Single pole double throw (SPDT) switch NE/SA630

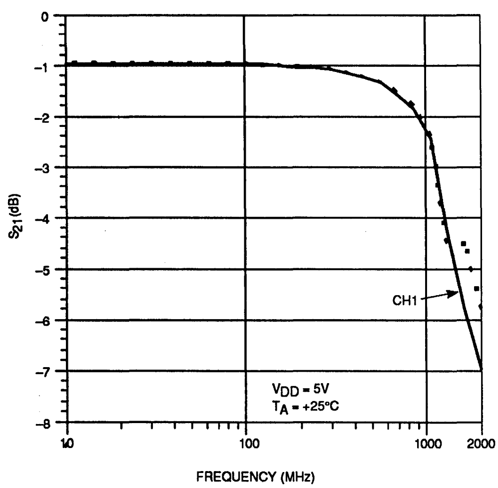


Figure 10 Loss Matching vs. Frequency; CH1 vs. CH2 for D-Pakage

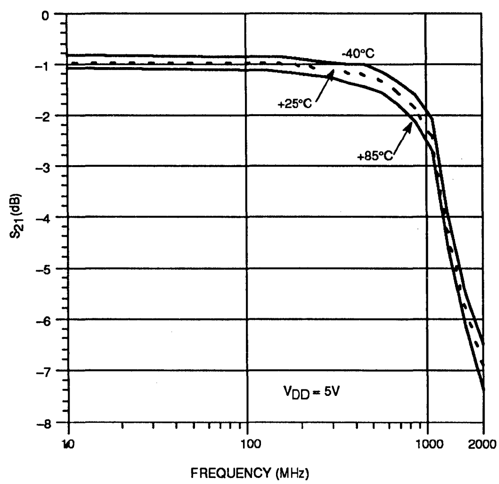


Figure 11 Loss vs. Frequency and Temperature for D-Package

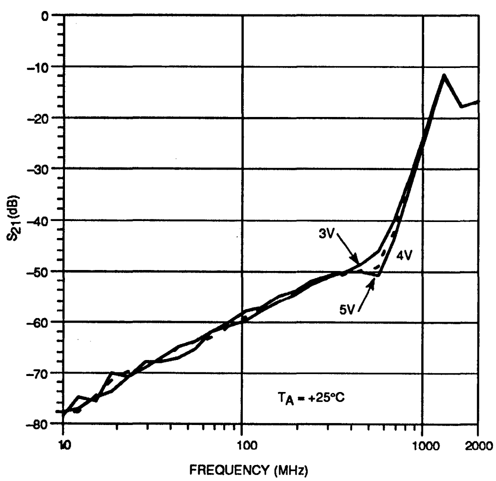


Figure 12 Isolation vs. Frequency and V_{DD} for D-Package

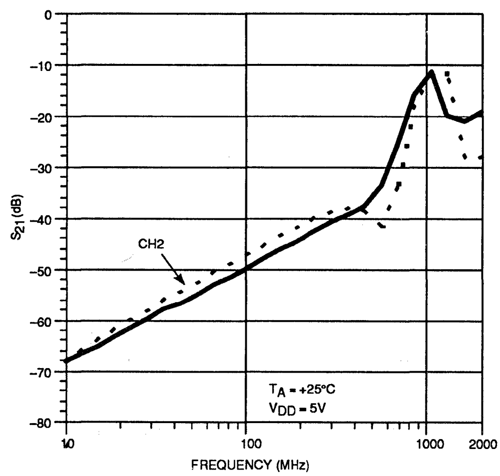


Figure 13 Isolation Matching vs. Frequency for N-Package (DIP)

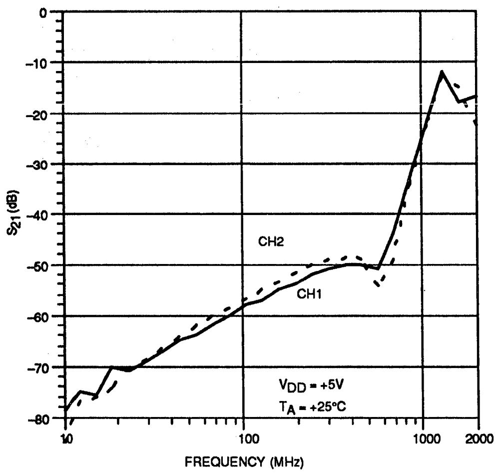


Figure 14 Isolation Matching vs. Frequency; CH1 vs. CH2 for D-Package

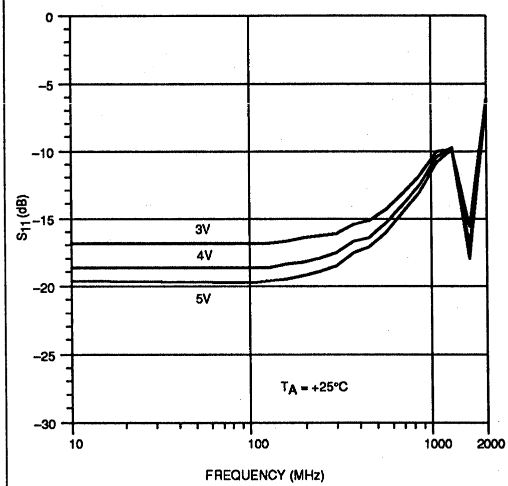


Figure 15 Input Match On-Channel vs. Frequency and V_{DD}

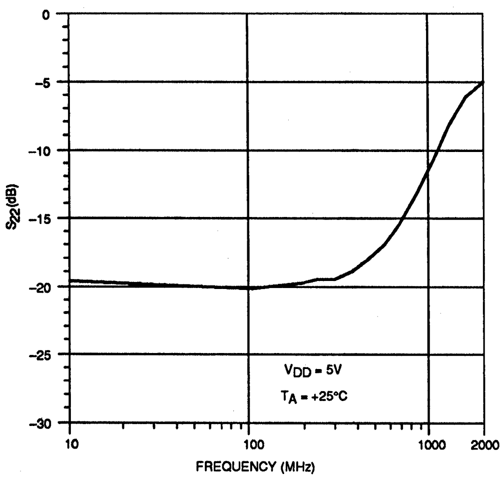


Figure 16 Output Match On-Channel vs. Frequency

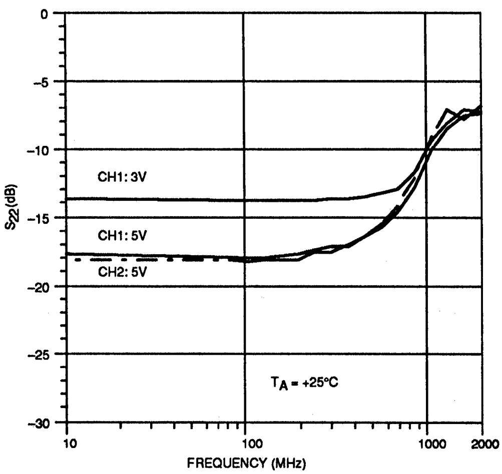


Figure 17 OFF-Channel Match vs. Frequency and V_{DD}

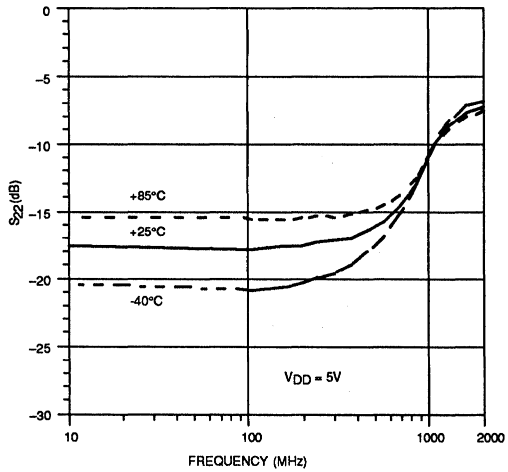


Figure 18 OFF Channel Match vs. Frequency and Temperature

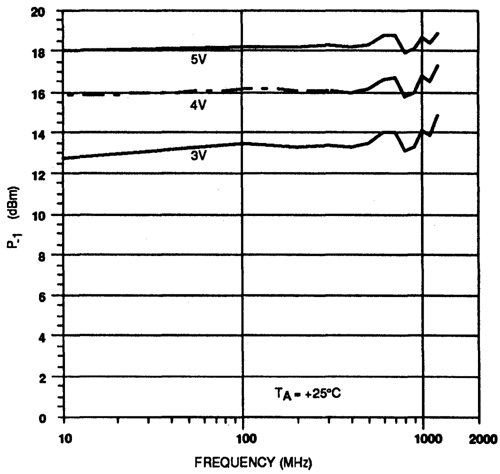


Figure 19 P_{-1} dB vs. Frequency and V_{DD}

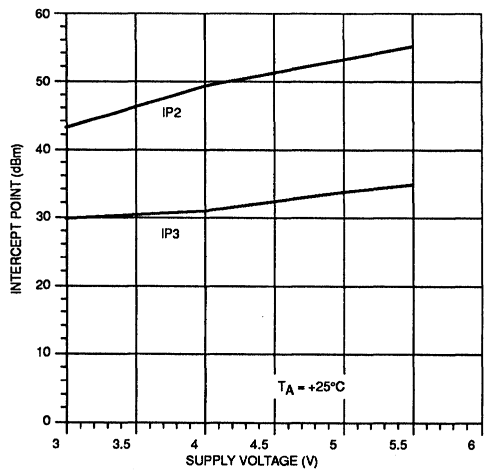


Figure 20 Intercept Points vs.V_{DD}

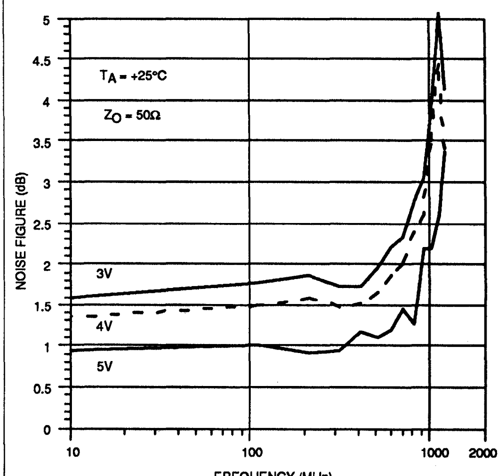


Figure 21 Noise Figure vs. Frequency and V_{DD} for D-Package

ENCH1 (Pin4)

OUT1 (Pin 8)

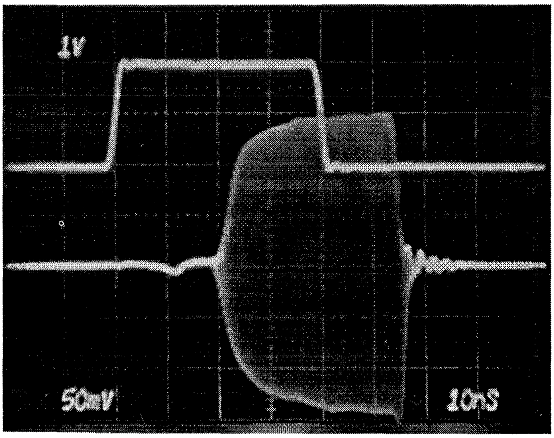


Figure 22 Switching Speed; f_{IN} = 100MHz at -6dBm, V_{DD} = 5V

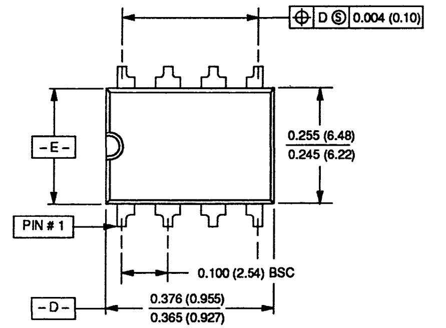
Section 9
Package outlines

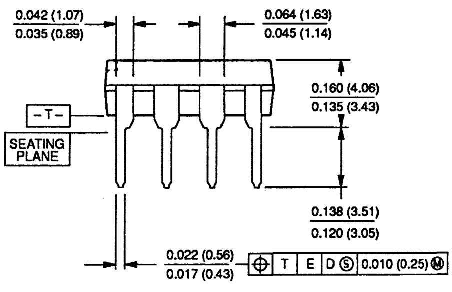
RF Communications

INDEX

Package outlines

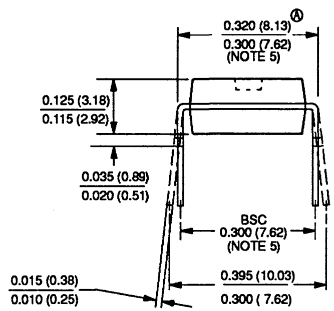
8-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE





NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AB for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 8 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from the top.

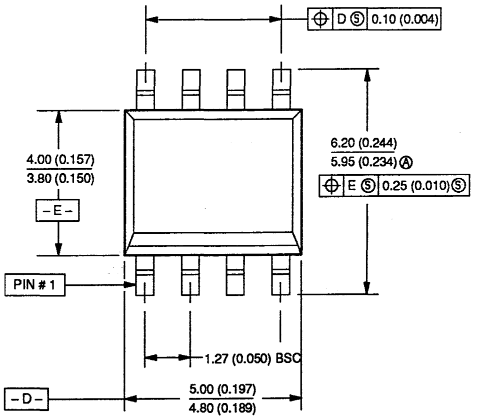


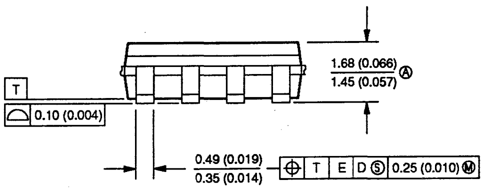
853-0404A 02880

NE1

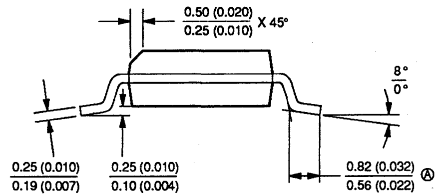
Package outlines

8-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE





NOTES
1. Package dimensions conform to JEDEC Specification MS-012-AA for standard Small Outline (SO) package, 8 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm (0.010") on any side.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from top.
6. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.

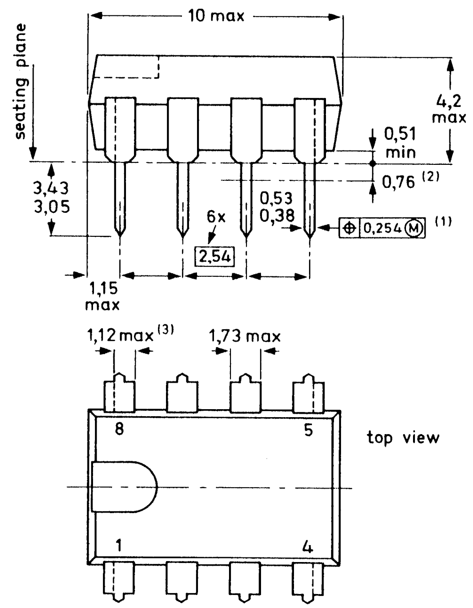


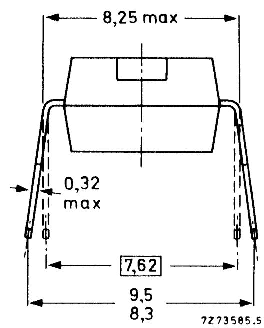
853-0174B 04142

DE1

Package outlines

8-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

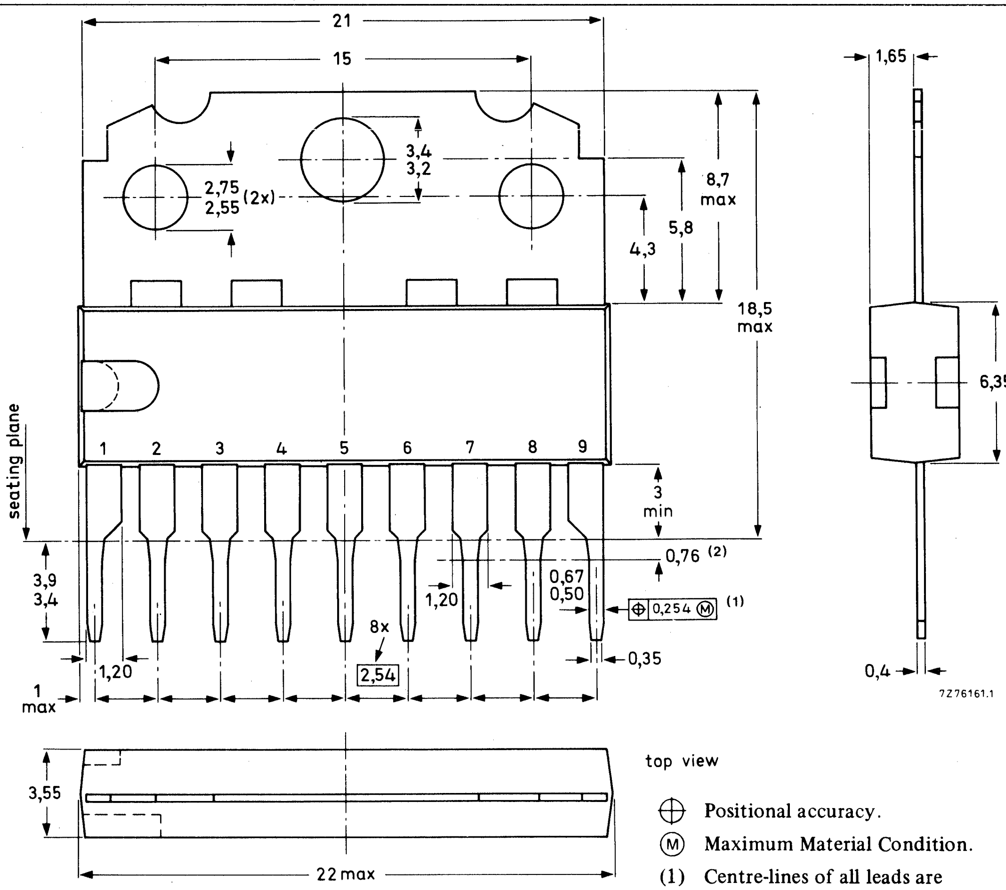
Dimensions in mm

SOT 97

7Z73585.5

Package outlines

9-PIN PLASTIC SINGLE IN-LINE (U) PACKAGE



⊕ Positional accuracy.

(M) Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

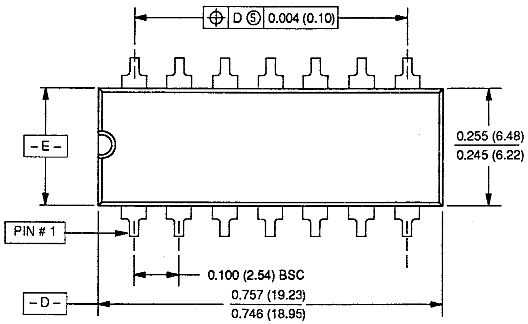
SOT 110B

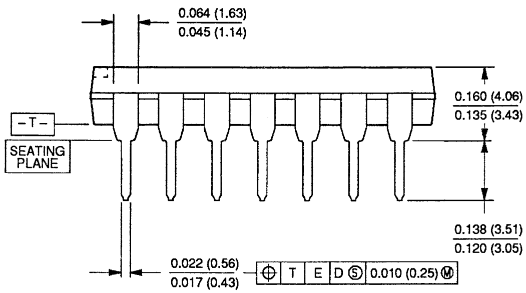
7Z76161.1

Package outlines

14-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE

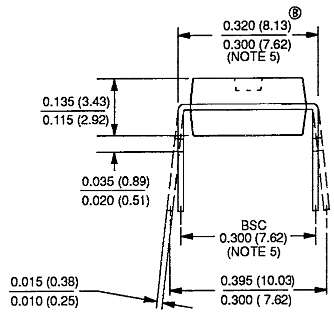
853-0405B 02880





NOTES

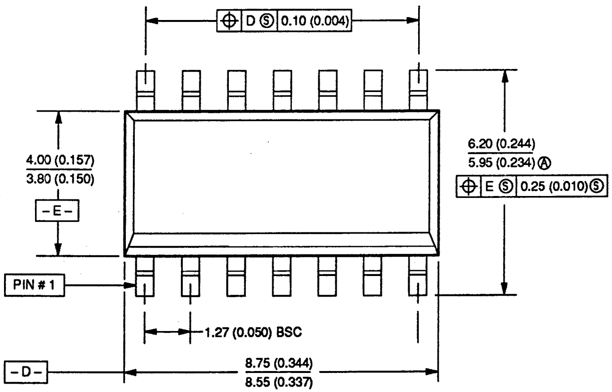
1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AC for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 14 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.



NH1

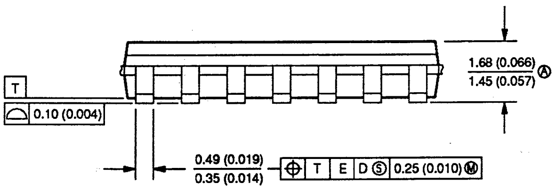
Package outlines

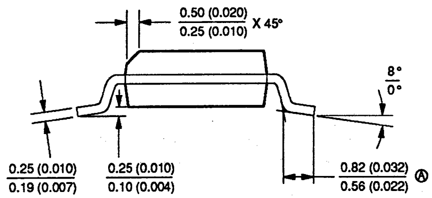
14-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE



NOTES

1. Package dimensions conform to JEDEC Specification MS-012-AB for standard Small Outline (SO) package, 14 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm (0.010") on any side.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.
6. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.



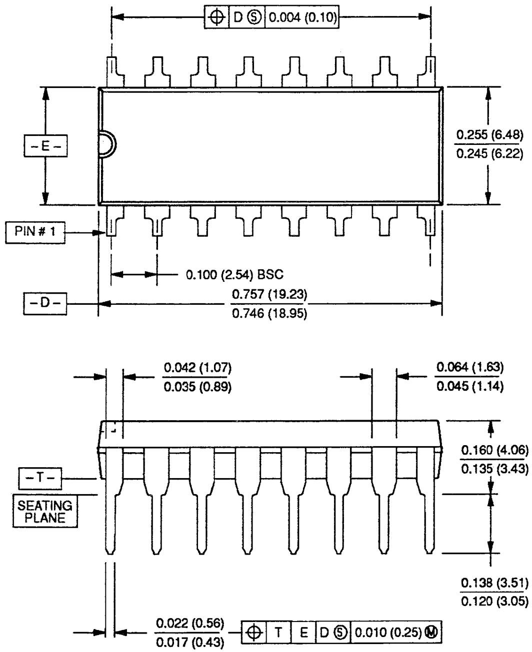


853–0175C 04142

DH1

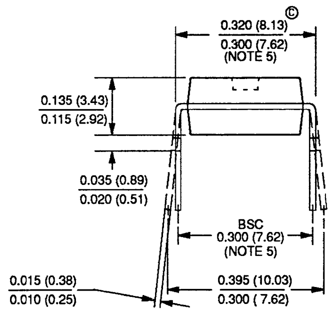
Package outlines

16-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AA for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 16 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #16 when viewed from the top.

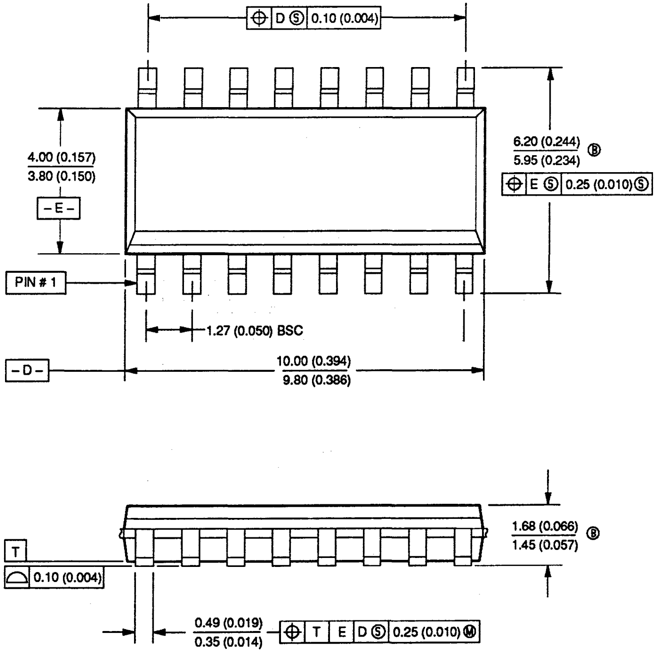


853-0406C 02880

NJ1

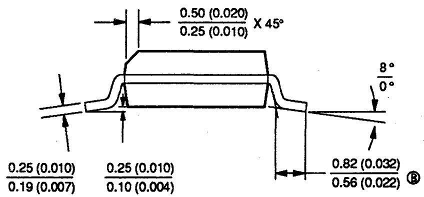
Package outlines

16-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE



NOTES

1. Package dimensions conform to JEDEC Specification MS-012-AC for standard Small Outline (SO) package, 14 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm (0.010") on any side.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #16 when viewed from top.
6. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.

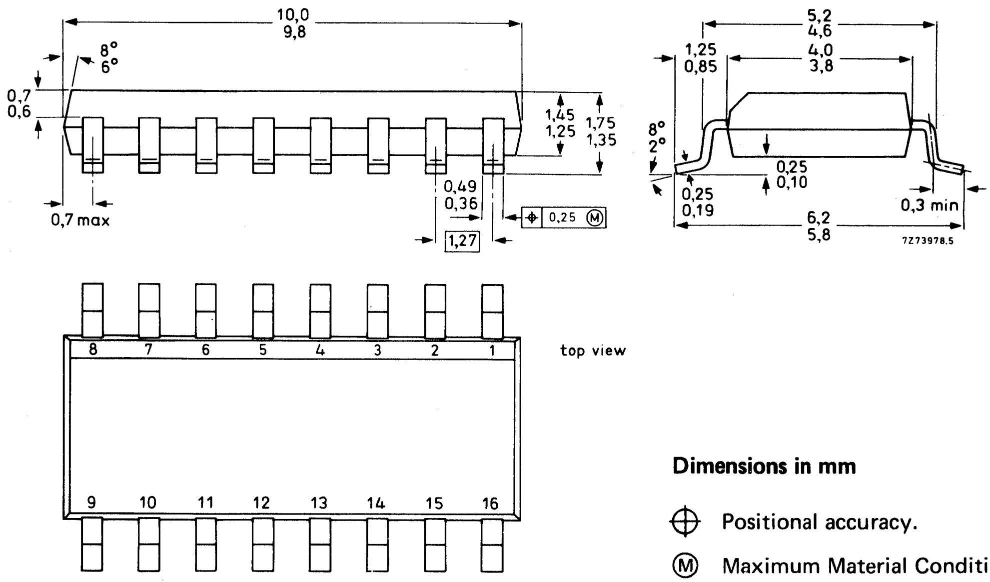


853-0005C 04142

DJ1

Package outlines

16-PIN PLASTIC SO DUAL IN-LINE (D/T) PACKAGE



Dimensions in mm

⊕ Positional accuracy.

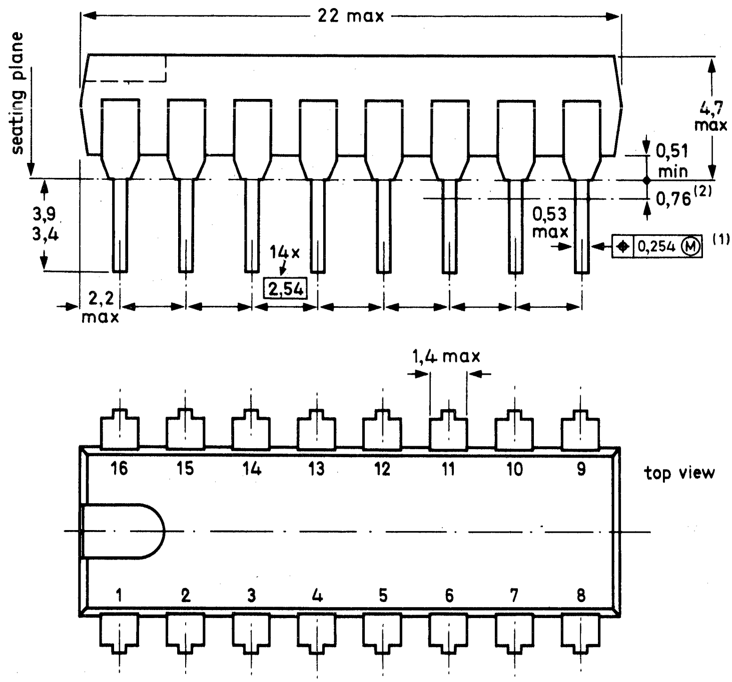
Ⓜ Maximum Material Condition.

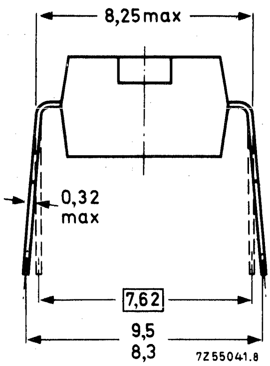
SOT 109A

7Z73978.5

Package outlines

16-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE





(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

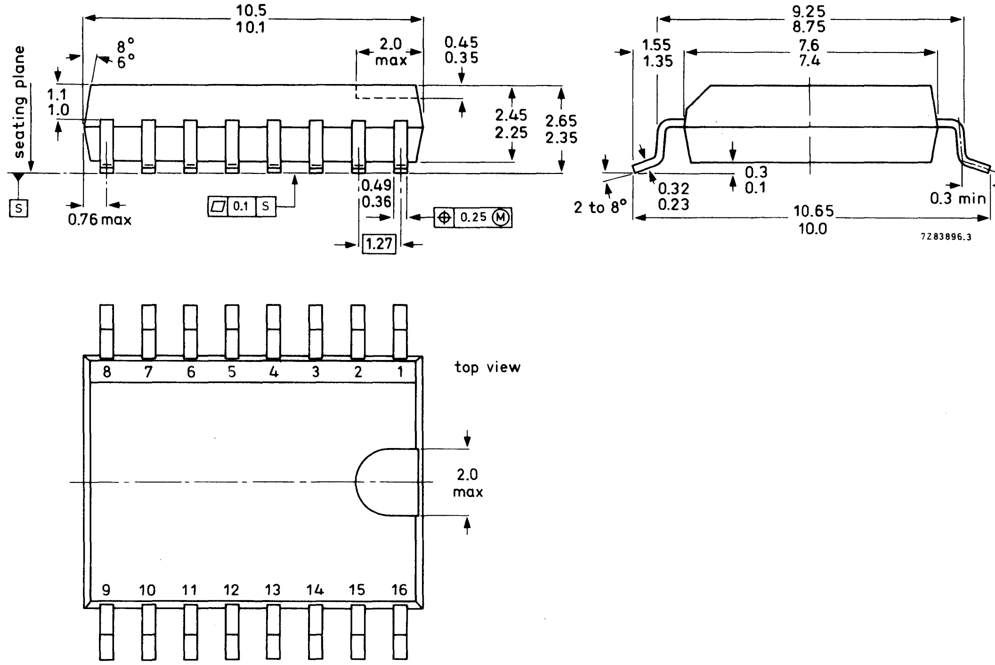
(3) Dimensions in mm.

SOT 38

7Z55041.8

Package outlines

16-PIN PLASTIC SOL DUAL IN-LINE (D/T) PACKAGE



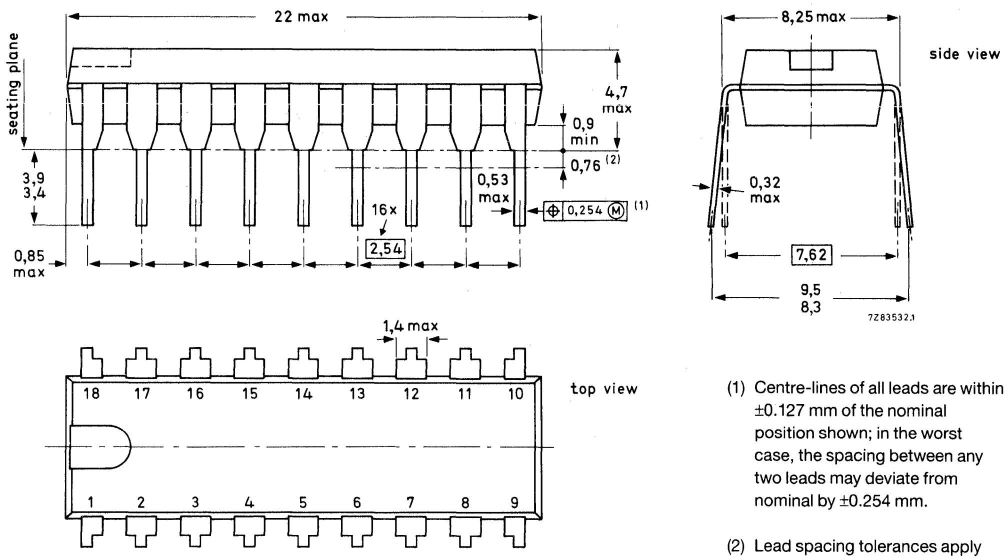
(1) Dimensions in mm.

SOT 162A

7Z83896.3

Package outlines

18-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE



(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

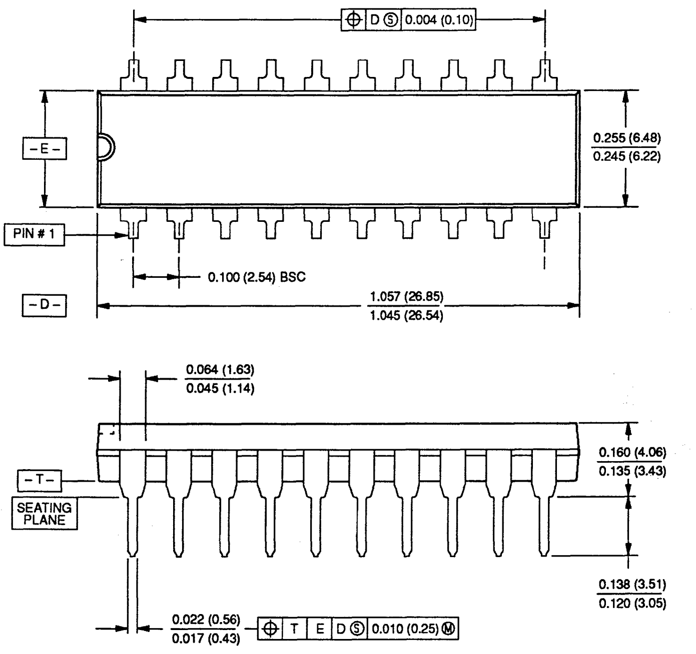
(3) Dimensions in mm.

SOT 102

7Z83532.1

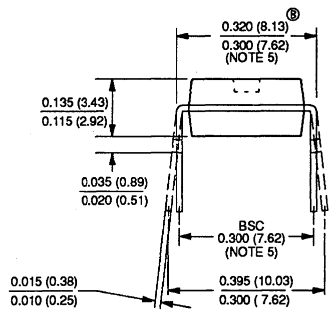
Package outlines

20-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



NOTES

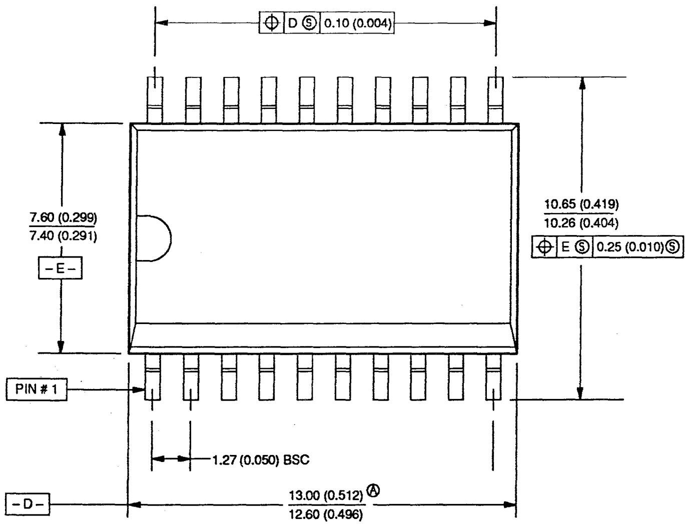
1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AE for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 20 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #20 when viewed from the top.



853-0408B 02880

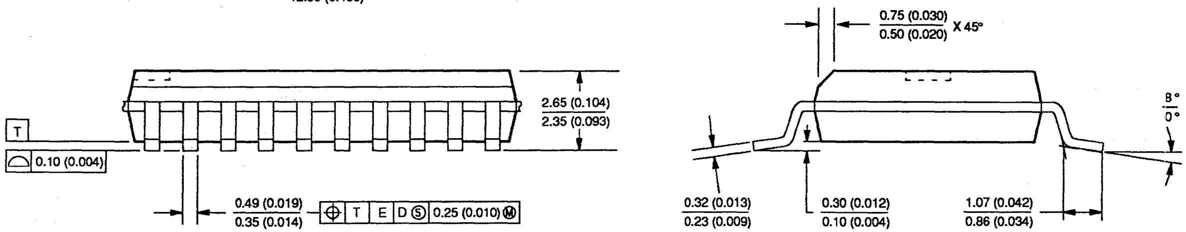
NL1

20-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



NOTES

1. Package dimensions conform to JEDEC Specification MS-013-AC for standard Small Outline (SO) package, 20 leads, 7.50mm (0.300") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm (0.010") on any side.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic Small Outline (SO) package is the suffix D after the product number.

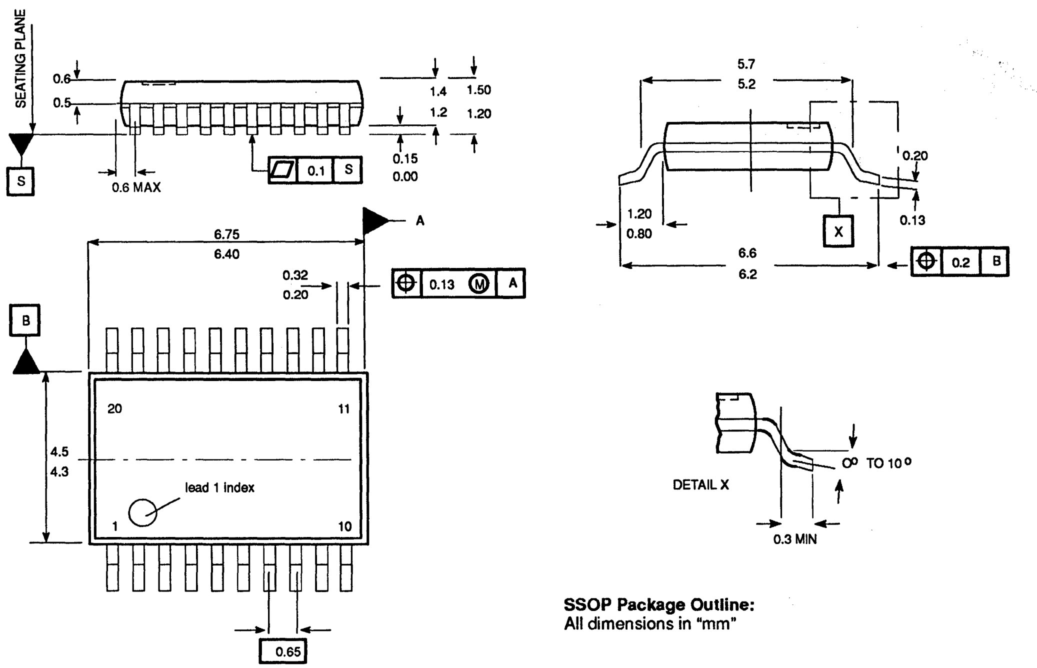


853-0172C 04142

DL2

Package outlines

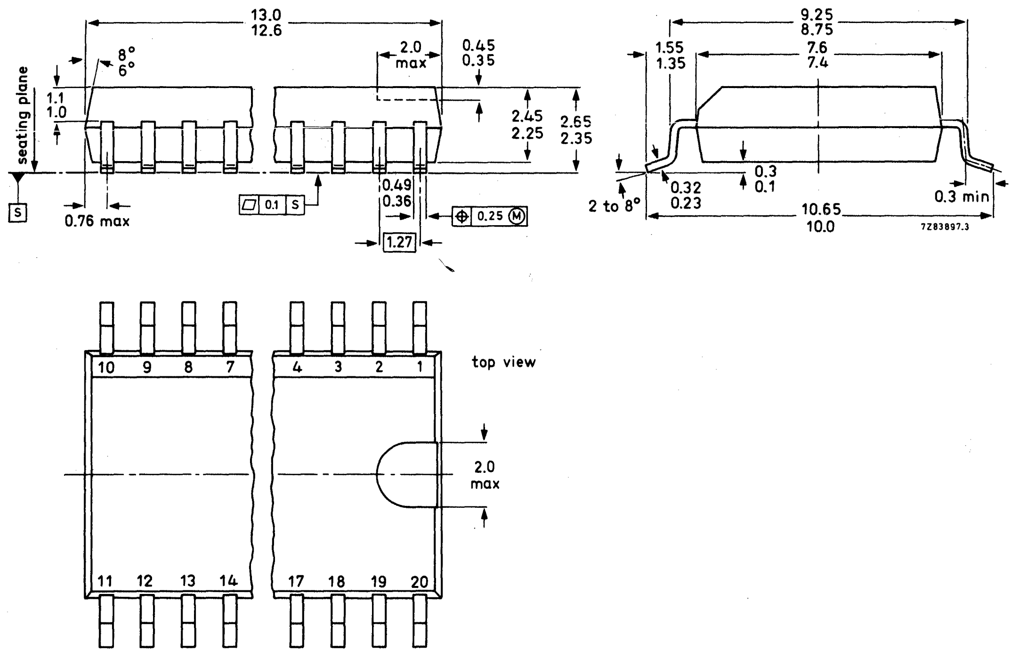
20-PIN PLASTIC SHRINK SMALL OUTLINE PACKAGE (SSOP) (DK PACKAGE)



SSOP Package Outline:
All dimensions in "mm"

Package outlines

20-PIN PLASTIC SO DUAL IN-LINE (D/T) PACKAGE



(1) Dimensions in mm.

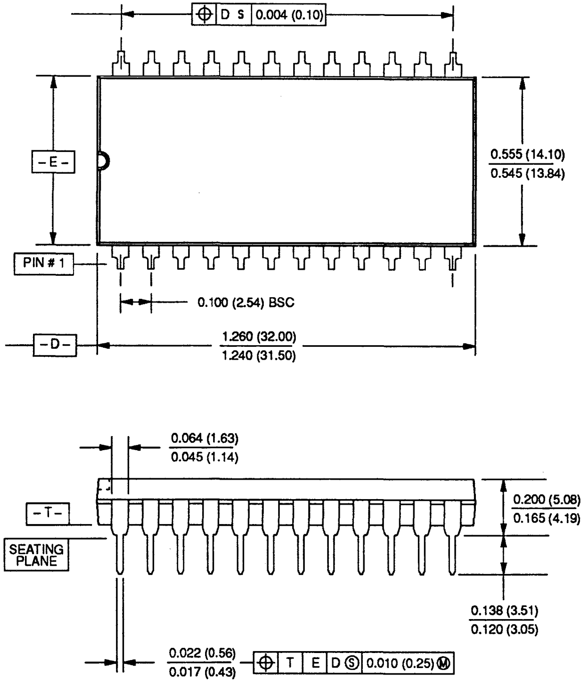
SOT 163A

7Z83897.3

Package outlines

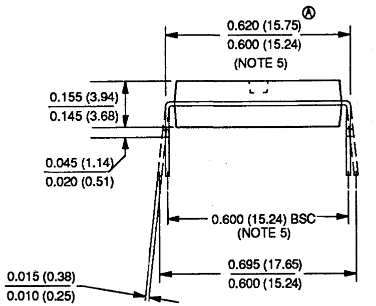
24-PIN (600 mils wide) PLASTIC DUAL IN-LINE PACKAGE

853-0412A 02880



NOTES:

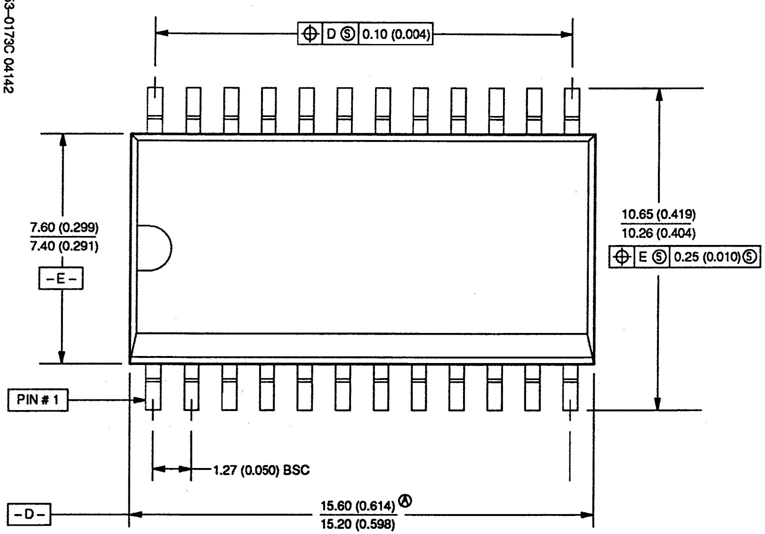
1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-011-AA for standard Dual In-Line (DIP) package 0.600 inch row spacing (plastic) 24 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #24 when viewed from the top.

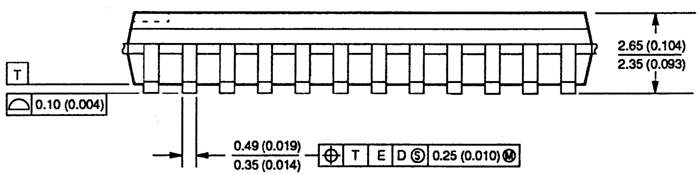


NN3

Package outlines

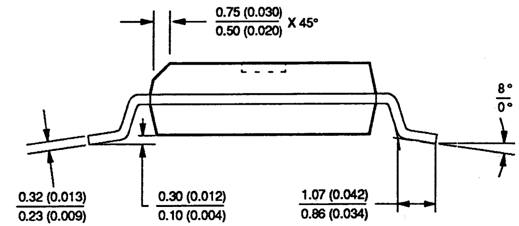
24-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE





NOTES

1. Package dimensions conform to JEDEC Specification MS-013-AD for standard Small Outline (SO) package, 24 leads, 7.50mm (0.300") body width (Issue A. June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D", and "E" are reference datums on the molded body and do not incluce mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm (0.010") on any side.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic Small Outline (SO) package is the suffix D after the product number.

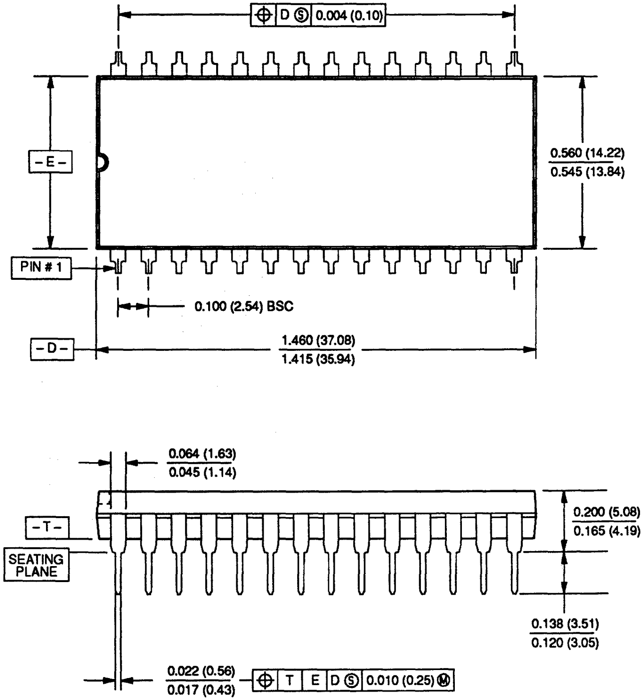


853-0173C 04142

DN2

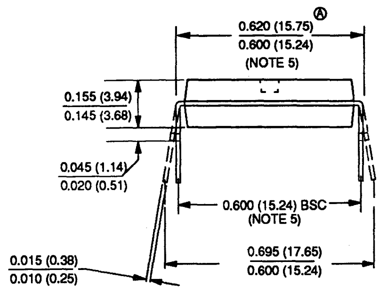
Package outlines

28-PIN (600 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



NOTES:

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-011-AB for standard Dual In-Line (DIP) package 0.600 inch row spacing (plastic) 28 leads (Issue B, 7/84).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #28 when viewed from the top.

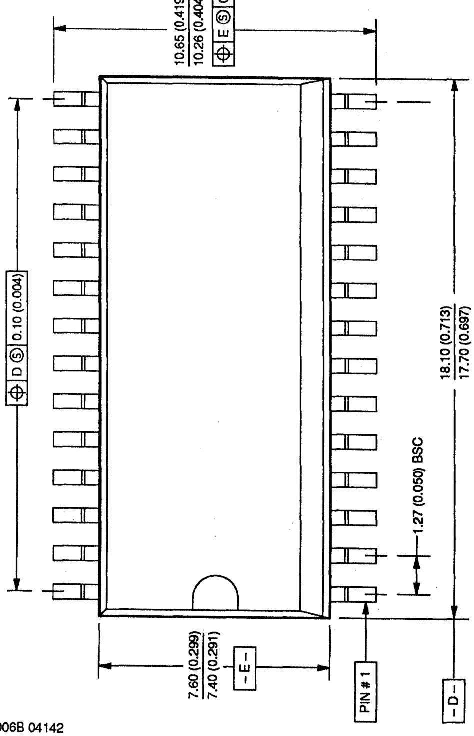


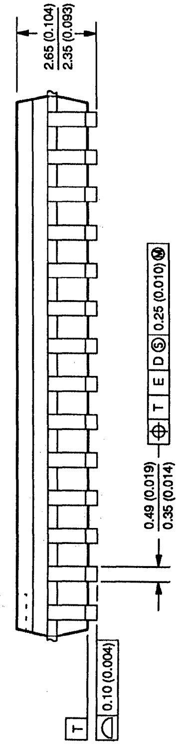
853-0413B 01988

NQ3

Package outlines

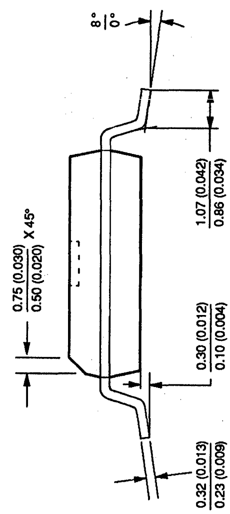
28-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE





NOTES

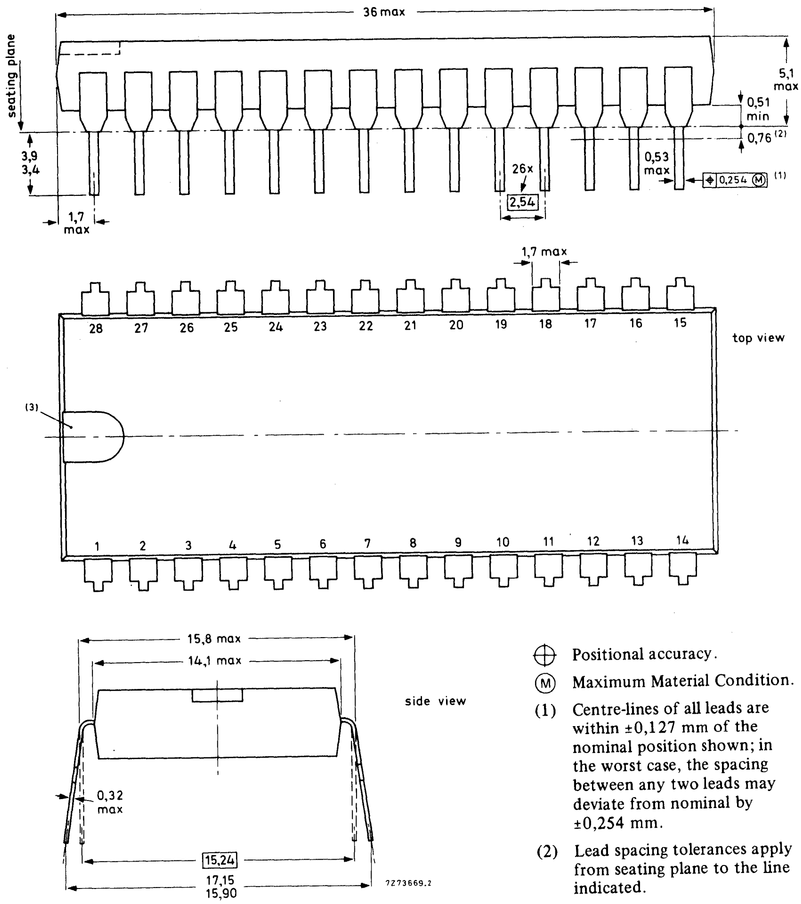
1. Package dimensions conform to JEDEC Specification MS-013-AE for standard Small Outline (SO) package, 28 leads, 7.50mm (0.300") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D", and "E" are reference datums on the molded body and do not incluce mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm (0.010") on any side.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic Small Outline (SO) package is the suffix D after the product number.



DQ2

Package outlines

28-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

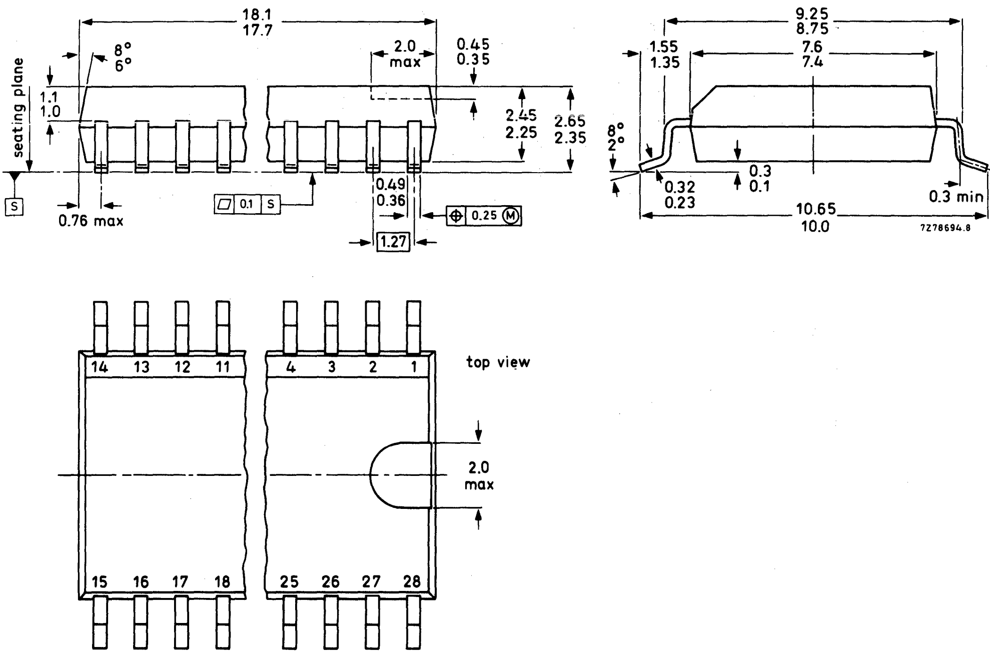
Dimensions in mm

SOT 117

7Z73669.2

Package outlines

28-PIN PLASTIC SO DUAL IN-LINE (D/T) PACKAGE



(1) Dimensions in mm.

SOT 136A

7Z78694.8

Section 10
Sales offices

RF Communications

Sales Offices, Representatives & Distributors

RF Communications

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811 East Arques Avenue
P.O. Box 3409
Sunnyvale, CA 94088-3409

ALABAMA
Huntsville
Phone: (205) 464-0111

CALIFORNIA
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Irvine
Phone: (714) 833-8980
(714) 752-2780

San Diego
Phone: (619) 560-0242

Sunnyvale
Phone: (408) 991-3737

COLORADO
Englewood
Phone: (303) 792-9011

GEORGIA
Atlanta
Phone: (404) 594-1392

ILLINOIS
Itasca
Phone: (708) 250-0050

INDIANA
Kokomo
Phone: (317) 459-5355

MASSACHUSETTS
Westford
Phone: (508) 692-6211

MICHIGAN
Farmington Hills
Phone: (313) 553-6070

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