82C611A VL IDE Controller

Data Book

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VL IDE Controller

1.0 Overview

The OPTi 82C611A is a high performance IDE disk drive controller ASIC. The 82C611A interfaces directly to the VL-bus and up to two IDE disk drives with no additional TTL logic or buffers needed. This chip also supports all of the high speed ANSI standard IDE devices using modes 1, 2 and 3. Non-ANSI standard IDE devices can be optimized by using programmable timing registers. An integrated four-level read pre-fetch FIFO and a four-level posted write FIFO support zero wait state operations; substantially improving performance over conventional interface devices. The 82C611A also supports an 82C611-compatible mode that makes the chip functionally equivalent, pin-for-pin, with the 82C611 IDE controller.

2.0 Features

- Supports VESA 32-bit VL Bus
- 100-pin PQFP
- Enhanced ATA Specification Support
- Zero Wait-State with Four-Level Write Posting
- Four-Level Read Pre-fetch FIFO
- 32-bit CPU transfers to and from IDE data port
- SMI support & IDE command trapping
- Compatible with 82C611 IDE Controller

The 32-bit VL-bus interface provides substantial performance improvement over controllers on the AT-bus. The integrated read pre-fetch FIFO and posted write FIFO allow IDE cycles to be performed concurrently with CPU cycles; providing additional performance gain. These features and the flexible IDE interface timing registers provide the optimum performance for any IDE drive.

Figure 2-1 Block Diagram

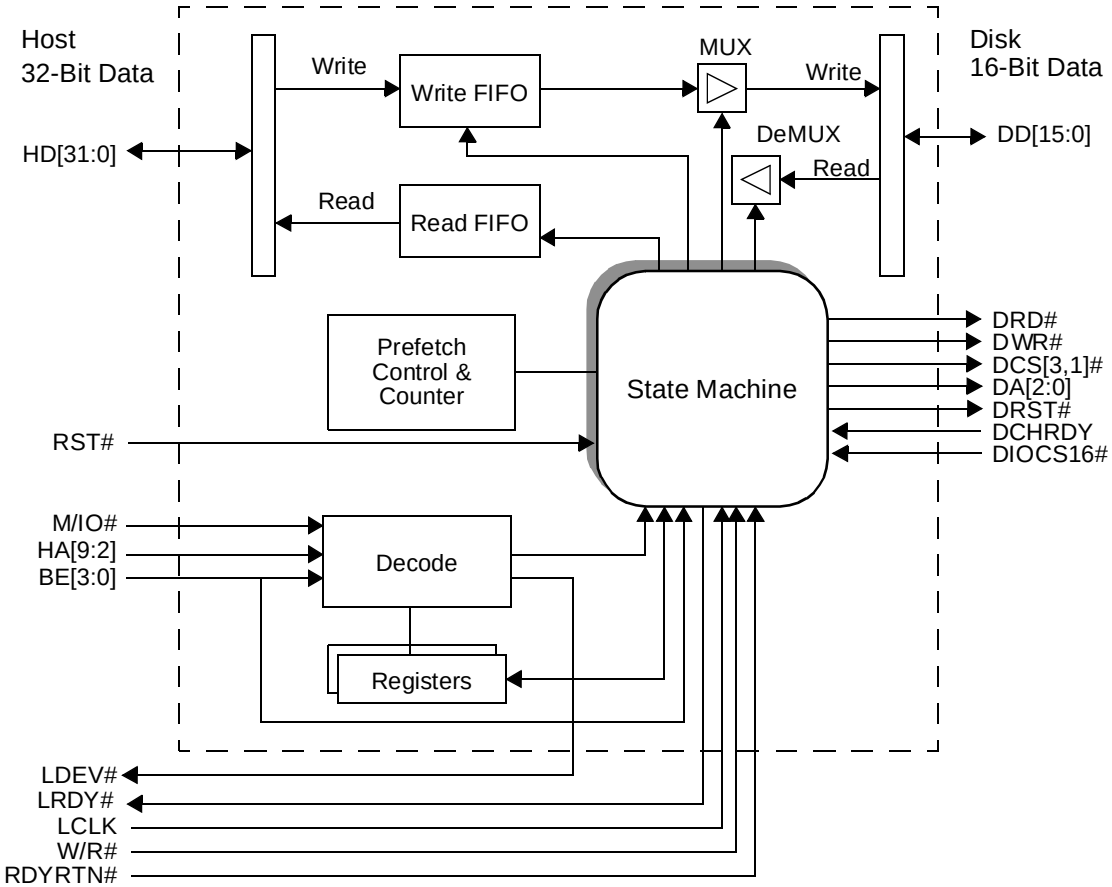


Figure 2-2 Example Block Diagram using the OPTi 82C611A in Enhanced Mode

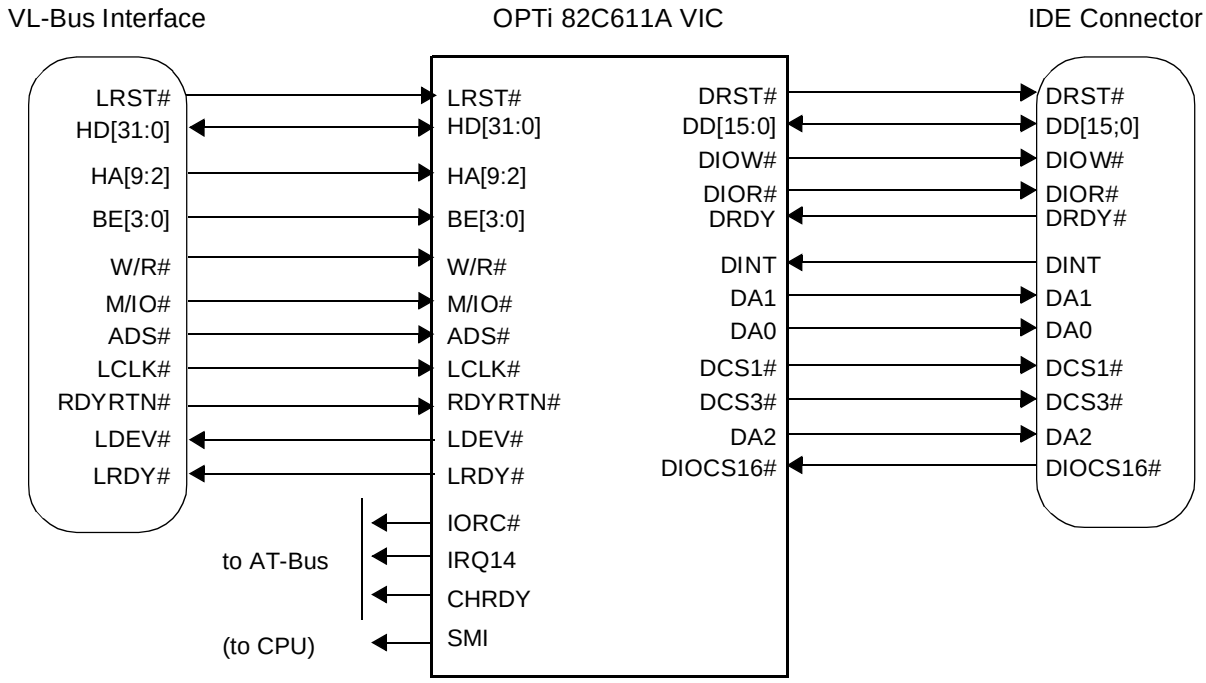
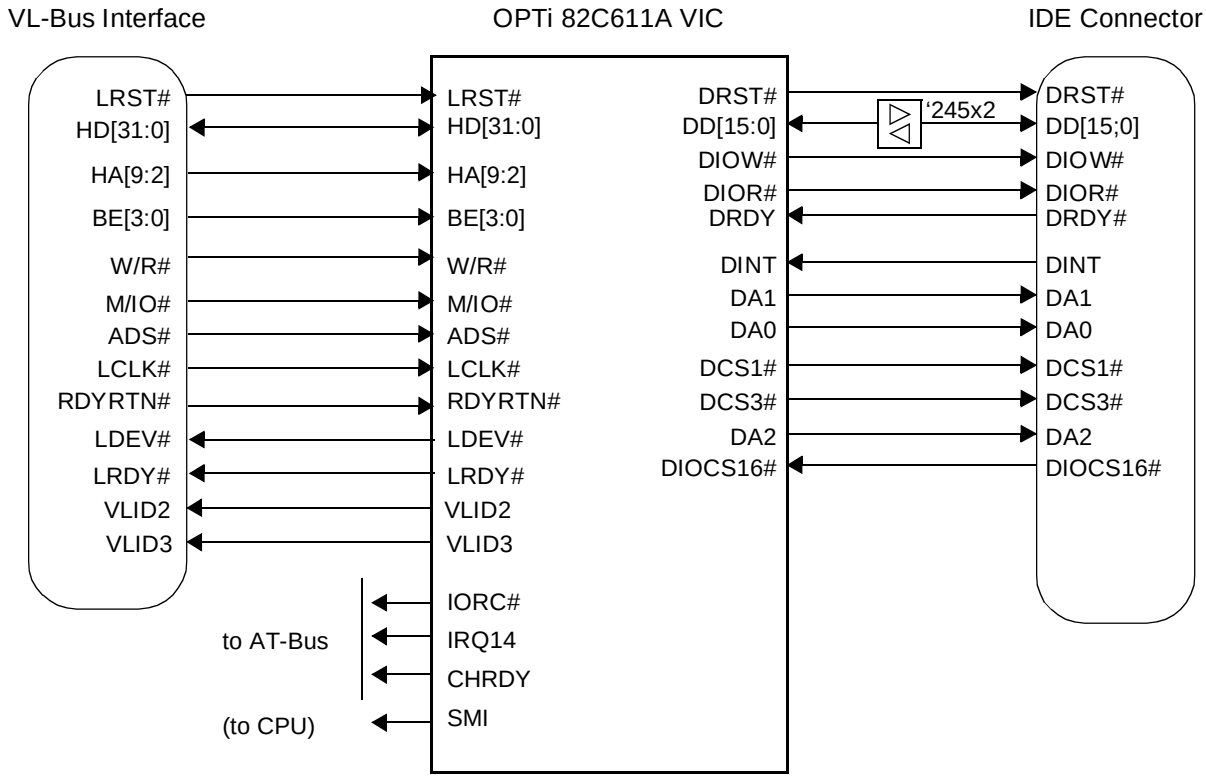


Figure 2-3 Example Block Diagram using the OPTi 82C611A in Compatible Mode



3.0 Signal Descriptions

Figure 3-1 82C611A Pinout Diagram - 82C611 Enhanced Mode

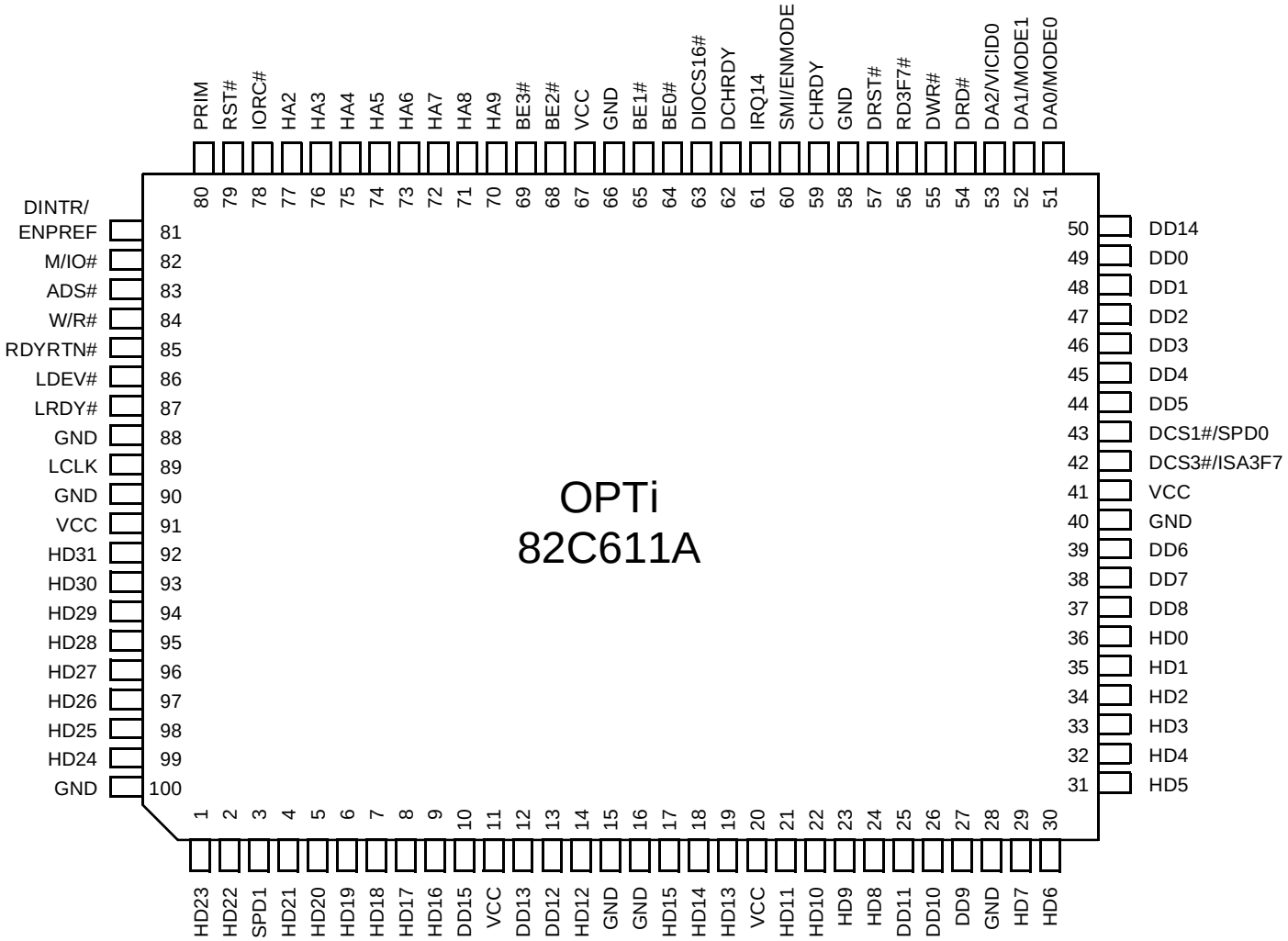


Figure 3-2 82C611A Pinout Diagram - 82C611 Compatible Mode

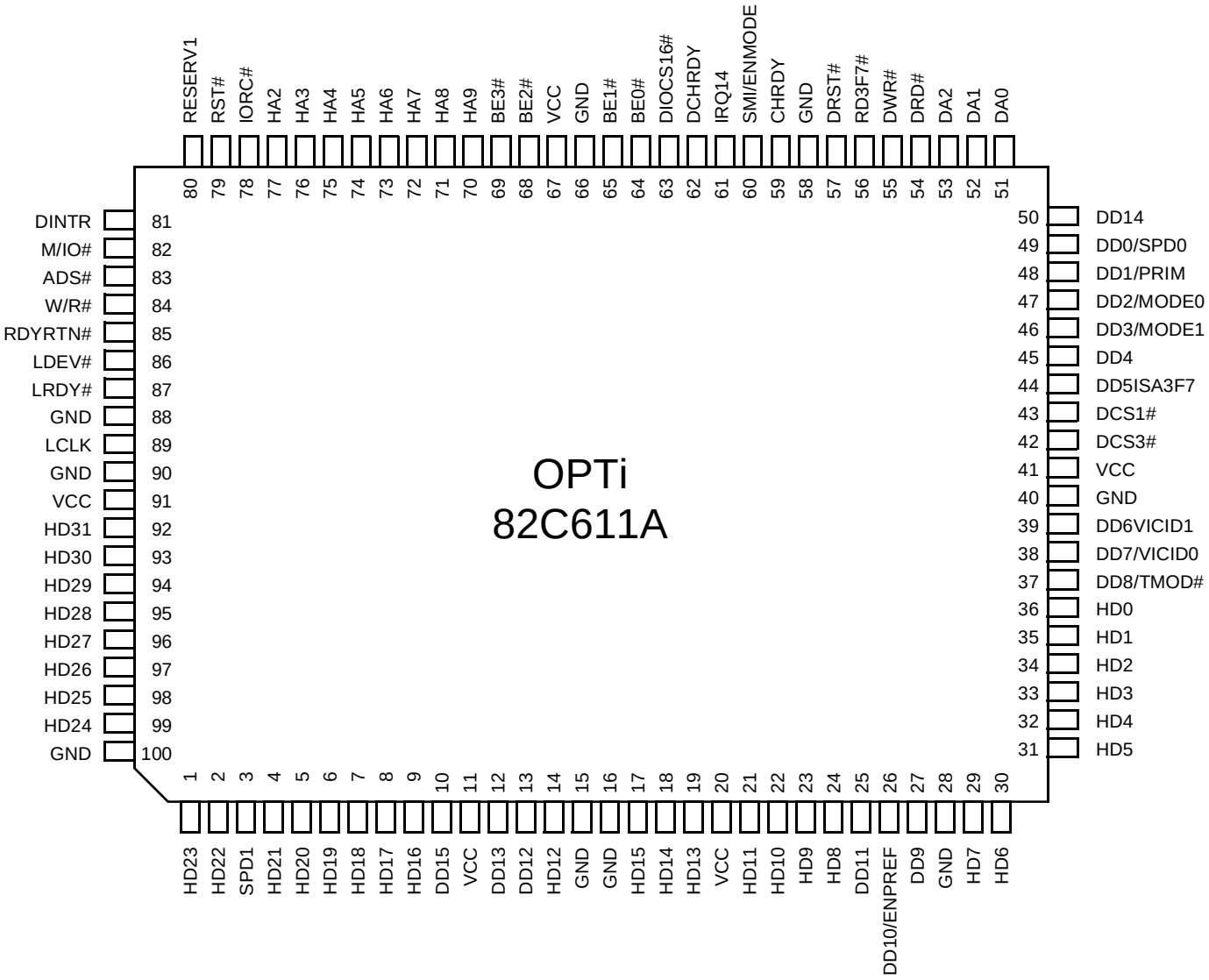


Table 3-1 Numerical Pin List - Enhanced Mode

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	HD23	26	DD10	51	DA0/MODE0	76	HA3
2	HD22	27	DD9	52	DA1/MODE1	77	HA2
3	SPD1	28	GND	53	DA2/VICID0	78	IORC#
4	HD21	29	HD7	54	DRD#	79	RST#
5	HD20	30	HD6	55	DWR#	80	PRIM
6	HD19	31	HD5	56	RD3F7#	81	DINTR/ENPREF
7	HD18	32	HD4	57	DRST#	82	M/IO#
8	HD17	33	HD3	58	GND	83	ADS#
9	HD16	34	HD2	59	CHRDY	84	W/R#
10	DD15	35	HD1	60	SMI/ENMODE	85	RDYRTN#
11	Vcc	36	HD0	61	IRQ14	86	LDEV#
12	DD13	37	DD8	62	DCHRDY	87	LRDY#
13	DD12	38	DD7	63	DIOCS16#	88	GND
14	HD12	39	DD6	64	BE0#	89	LCLK
15	GND	40	GND	65	BE1#	90	GND
16	GND	41	Vcc	66	GND	91	Vcc
17	HD15	42	DCS3#/ISA3F7	67	Vcc	92	HD31
18	HD14	43	DCS1#/SPD0	68	BE2#	93	HD30
19	HD13	44	DD5	69	BE3#	94	HD29
20	Vcc	45	DD4	70	HA9	95	HD28
21	HD11	46	DD3	71	HA8	96	HD27
22	HD10	47	DD2	72	HA7	97	HD26
23	HD9	48	DD1	73	HA6	98	HD25
24	HD8	49	DD0	74	HA5	99	HD24
25	DD11	50	DD14	75	HA4	100	GND

Table 3-2 Alphabetical Pin List - Enhanced Mode

Pin	Name	Pin	Name	Pin	Name	Pin	Name
83	ADS#	12	DD13	36	HD0	98	HD25
64	BE0#	50	DD14	35	HD1	97	HD26
65	BE1#	10	DD15	34	HD2	96	HD27
68	BE2#	81	DINTR/ENPREF	33	HD3	95	HD28
69	BE3#	63	DIOCS16#	32	HD4	94	HD29
59	CHRDY	54	DRD#	31	HD5	93	HD30
51	DA0/MODE0	57	DRST#	30	HD6	92	HD31
52	DA1/MODE1	55	DWR#	29	HD7	78	IORC#
53	DA2/VICID0	15	GND	24	HD8	61	IRQ14
62	DCHRDY	16	GND	23	HD9	89	LCLK
43	DCS1#/SPD0	28	GND	22	HD10	86	LDEV#
42	DCS3#/ISA3F7	40	GND	21	HD11	87	LRDY#
49	DD0	58	GND	14	HD12	82	M/IO#
48	DD1	66	GND	19	HD13	80	PRIM
47	DD2	88	GND	18	HD14	56	RD3F7#
46	DD3	90	GND	17	HD15	85	RDYRTN#
45	DD4	100	GND	9	HD16	79	RST#
44	DD5	77	HA2	2	HD17	60	SMI/ENMODE
39	DD6	76	HA3	7	HD18	3	SPD1
38	DD7	75	HA4	6	HD19	11	Vcc
37	DD8	74	HA5	5	HD20	20	Vcc
27	DD9	73	HA6	4	HD21	41	Vcc
26	DD10	72	HA7	2	HD22	67	Vcc
25	DD11	71	HA8	1	HD23	91	Vcc
13	DD12	70	HA9	99	HD24	84	W/R#

Table 3-3 OPTi 82C611A Numerical Pin List - Compatible Mode

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	HD23	26	DD10/ENPREF	51	DA0	76	HA3
2	HD22	27	DD9	52	DA1	77	HA2
3	SPD1	28	GND	53	DA2	78	IORC#
4	HD21	29	HD7	54	DRD#	79	RST#
5	HD20	30	HD6	55	DWR#	80	RESRV1
6	HD19	31	HD5	56	RD3F7#	81	DINTR
7	HD18	32	HD4	57	DRST#	82	M/IO#
8	HD17	33	HD3	58	GND	83	ADS#
9	HD16	34	HD2	59	CHRDY	84	W/R#
10	DD15	35	HD1	60	SMI/ENMODE	85	RDYRTN#
11	Vcc	36	HD0	61	IRQ14	86	LDEV#
12	DD13	37	DD8/TMOD#	62	DCHRDY	87	LRDY#
13	DD12	38	DD7/VICID0	63	DIOCS16#	88	GND
14	HD12	39	DD6/VICID1	64	BE0#	89	LCLK
15	GND	40	GND	65	BE1#	90	GND
16	GND	41	Vcc	66	GND	91	Vcc
17	HD15	42	DCS3#	67	Vcc	92	HD31
18	HD14	43	DCS1#	68	BE2#	93	HD30
19	HD13	44	DD5/ISA3F7	69	BE3#	94	HD29
20	Vcc	45	DD4	70	HA9	95	HD28
21	HD11	46	DD3/MODE1	71	HA8	96	HD27
22	HD10	47	DD2/MODE0	72	HA7	97	HD26
23	HD9	48	DD1/PRIM	73	HA6	98	HD25
24	HD8	49	DD0/SPD0	74	HA5	99	HD24
25	DD11	50	DD14	75	HA4	100	GND

Table 3-4 OPTi 82C611A Alphabetical Pin List - Compatible Mode

Pin	Name	Pin	Name	Pin	Name	Pin	Name
83	ADS#	12	DD13	36	HD0	98	HD25
64	BE0#	50	DD14	35	HD1	97	HD26
65	BE1#	10	DD15	34	HD2	96	HD27
68	BE2#	81	DINTR	33	HD3	95	HD28
69	BE3#	63	DIOCS16#	32	HD4	94	HD29
59	CHRDY	54	DRD#	31	HD5	93	HD30
51	DA0	57	DRST#	30	HD6	92	HD31
52	DA1	55	DWR#	29	HD7	78	IORC#
53	DA2	15	GND	24	HD8	61	IRQ14
62	DCHRDY	16	GND	23	HD9	89	LCLK
43	DCS1#	28	GND	22	HD10	86	LDEV#
42	DCS3#	40	GND	21	HD11	87	LRDY#
49	DD0/SPD0	58	GND	14	HD12	82	M/IO#
48	DD1/PRIM	66	GND	19	HD13	56	RD3F7#
47	DD2/MODE0	88	GND	18	HD14	85	RDYRTN#
46	DD3//MODE1	90	GND	17	HD15	80	RESRV1
45	DD4	100	GND	9	HD16	79	RST#
44	DD5/ISA3F7	77	HA2	8	HD17	60	SMI/ENMODE
39	DD6/VICID1	76	HA3	7	HD18	3	SPD1
38	DD7/VICID0	75	HA4	6	HD19	11	Vcc
37	DD8/TMOD#	74	HA5	5	HD20	20	Vcc
27	DD9	73	HA6	4	HD21	41	Vcc
26	DD10/ENPREF	72	HA7	2	HD22	67	Vcc
25	DD11	71	HA8	1	HD23	91	Vcc
13	DD12	70	HA9	99	HD24	84	W/R#

3.1 Signal Definitions - 82C611 Enhanced Mode

3.1.1 Power Management Interface

Name	Type	Pin	Description
SMI / ENMODE	I/O	60	***System Management Interrupt/Enhanced Mode.*** This signal is used to signal to the host system that an SMI event has occurred. At reset time, this signal must be sampled high to set the 82C611A into 82C611 Enhanced Mode (a pull-up resistor is required). The 82C611A Register Description section describes the additions to 82C611 Enhanced Mode.

3.1.2 VL-BUS Interface

Name	Type	Pin	Description
ADS#	I	83	***Address Data Strobe.*** This signal indicates the start of the VL-Bus cycle.
BE[3:0]#	I	69, 68, 65, 64	***Byte Enable Lines 0 to 3.*** These signals indicate which bytes of the 32-bit VL-Bus are currently being transferred.
HA[9:2]	I	70-77	***Address Lines 2 to 9.*** These are the address lines for I/O or memory accesses.
HD[31:0]	I/O	92-99,1, 2, 4-9, 17-19, 14, 21-24, 29-36	***Data Bus Lines 0 to 31.*** This is the bi-directional data path from the host system to the VIC.
LCLK	I	89	***Local Bus Clock.*** This is the 1X system clock from the host.
LDEV#	O	86	***Local Device.*** This output indicates to the host that the current address on the VL-Bus is addressing the VIC.
LRDY#	O	87	***Local Ready.*** This signal begins the handshake with the host system that will eventually terminate the current VL-Bus cycle.
M/IO#	I	82	***Memory or I/O Status.*** This signal from the host system indicates that the current access on the VL-Bus is memory or I/O.
PRIM	I	80	***Primary Address.*** At reset time, this pin is sampled to set the Primary or Secondary IDE port address: 1 = Primary IDE (Address 1Fxh & 3Fxh) 0 = Secondary IDE (Address 17xh & 37xh)
RDYRTN#	I	85	***Ready Return.*** This signal indicates that the current cycle has ended.
RST#	I	79	***System Reset.*** This signal is used to initialize the VIC and any drives attached.
SPD1	I	3	***VL Bus Frequency Select (MSB).*** At reset time, this signal is sampled to set the Strap Register bit 1 which (along with Strap Register bit 0) decides the VL-Bus clock frequency. This may be connected to an external jumper or ID3 of the VL-Bus.
W/R#	I	84	***Write or Read Status.*** This signal from the host system indicates that the current access on the VL-Bus is a write or a read.

3.1.3 IDE Interface

Name	Type	Pin	Description
DA2/VICID0	I/O	53	***Drive Address Line 2/VL-Bus IDE Controller ID 0.*** This is the MSB of the 3-bit binary coded address asserted by the host to access a register or data port in the drive. At reset time, this pin is sampled to set the ID of the VIC chip. The value read determines the ID of this device. After reset, the VIC with VICID0 = 1 has its IDE port enabled and the other VIC has its IDE port disabled. When programming the VIC configuration registers, the VICID0 field of the ID register must match the VICID0 strap option. The VICID1 field of the ID register must be 1 in the new mode.
DA[1:0] / MODE[1:0]	I/O	52-51	***Drive Address Lines/Mode.*** These are the two lower bits of the 3-bit binary coded address asserted by the host to access a register or data port in the drive. At reset time, Mode[1,0] pins are sampled to set the IDE Device Modes for 16-bit Cycle Times: Mode 1 Mode 0 Cycle-Time 0 0 ≥ 480ns 0 1 ≥ 383ns 1 0 ≥ 240ns 1 1 ≥ 180ns
DCHRDY	I	62	***Data Channel Ready.*** This signal is negated to extend the host transfer cycle of any host register access (read or write) when the drive is not ready to respond to a data transfer request. When DCHRDY is not negated, DCHRDY is in a high impedance state.
DCS1# / SPD0	I/O	43	***Drive Chip Select 1/VL-Bus Frequency Select (LSB).*** This is the chip select signal decoded from the host address bus used to select the Command Block Registers. At reset time, this pin is sampled to set the Strap Register bit 0 (VL-bus frequency select, LSB). Along with SPD1 (MSB), SPD0 determines the exact VL-Bus frequency: SPD1 SPD0 Frequency 0 0 50 MHz 0 1 40 MHz 1 0 33 MHz 1 1 25 MHz
DCS3# / ISA3F7	I/O	42	***Drive Chip Select 3/IO Port 3F7 Bus Select.*** This is the chip select signal decoded from the host address bus used to select the control Block Registers. At reset time, ISA3F7 is sampled to set the Strap Register bit 7 which decides whether read accesses to I/O port 3F7h come from the local bus or from the AT-Bus. 0 = 3F7h read from local bus, 1 = 3F7h read from AT-Bus bus
DIOCS16#	I	63	***Drive 16-bit I/O.*** DIOCS16# indicates that the 16-bit data port has been addressed and that the drive is prepared to send or receive a 16-bit data word. If DIOCS16# is not asserted, transfers are 8-bit using DD[7:0]. If DIOCS16# is asserted, transfers are 16-bit using DD[15:0].
DRD#	O	54	***Drive I/O read.*** This is the Read strobe signal. The low level of DRD# enables data from a register or the data port of the drive onto the data bus DD[7:0] or DD[15:0].

Name	Type	Pin	Description
DWR#	O	55	***Drive I/O write.*** This is the Write strobe signal. The rising edge of DWR# samples data from the data bus DD[7:0] or DD[15:0] into a register or the data port of the drive.
DINTR / ENPREF	I	81	***Drive Interrupt/Enable Prefetch.*** This signal is used to interrupt the host system. DINTR is asserted only when the drive has a pending interrupt, the drive is selected, and the host has cleared nIEN in the Device Control Register. DINTR is negated by: - assertion of DRST# - the setting of SRST of the Device Control Register, or - the host writing the Command Register or - the host reading the Status Register DINTR is asserted at the beginning of each data block to be transferred. A data block is typically a single sector, except when declared otherwise by use of the Set Multiple command. An exception to this occurs on Format Track, Write Sector(s), Write Buffer and Write Long commands where DINTR is not asserted at the beginning of the first data block to be transferred. At reset time, ENPREF is sampled to set the Miscellaneous Register bit 6 which decides whether to enable or disable read prefetch. 1 = Enable, 0 = Disable
DRST#	O	57	***Drive reset.*** This signal is asserted for at least 25 µsec after voltage levels have stabilized during power on and negated thereafter unless some event requires that the drive(s) be reset following power on.
RD3F7#	O	56	***Read Port 3F7h Buffer Enable.*** This pin enables the buffer for SD[6:0] for a register 3F7h read if pin ISA3F7 has been sampled high.
DD[15:0]	I/O	10, 50, 12, 13, 25-27, 37-39, 44-49	***Disk Data Bus Lines 0 to 15.*** These sixteen data bus lines require an external pull-up.

3.1.4 AT-Bus Interface

Name	Type	Pin	Description
CHRDY	O	59	***I/O Channel Ready.*** This signal to the AT-Bus is used to extend the current cycle for non-0WS operations. This signal may go active for reads to I/O address 3F7h if the ISA3F7 pin strap is high.
IORC#	I	78	***I/O Read or Disk Change Line.*** This signal from the AT-Bus indicates that an I/O read operation is occurring. This signal is used to map read accesses to the 3F7h register. For configurations including a floppy controller, this signal can be connected to the drive-change line for shared operation.
IRQ14	O	61	***Interrupt Request Line 14.*** This output to the AT-Bus is used to request interrupt service from the host system.

3.1.5 Power and Ground Pins

Name	Type	Pin	Description
GND	I	15, 16, 28, 40, 58, 66, 88, 90, 100	VSS or Ground
Vcc	I	11, 20, 41, 67, 91	Vcc or +5v

3.2 Signal Definitions - 82C611 Compatible Mode

3.2.1 Power Management Interface

Name	Type	Pin	Description
SMI / ENMODE	I/O	60	***System Management Interrupt/Enhanced Mode.*** This signal is used to signal to the host system that an SMI event has occurred. At reset time, this signal must be sampled low to set the 82C611A into 82C611 Compatible Mode (a pull-down resistor is required). In the 82C611 Compatible Mode, external TTL buffering is required for disk data lines.

3.2.2 VL-Bus Interface in the 82C611 Compatible Mode

Name	Type	Pin	Description
ADS#	I	83	***Address Data Strobe.*** This signal indicates the start of the VL-Bus cycle.
BE[3:0]#	I	69, 68, 65, 64	***Byte Enable Lines 0 to 3.*** These signals indicate which bytes of the 32-bit VL-Bus are currently being transferred.
HA[9:2]	I	70-77	***Address Lines 2 to 9.*** These are the address lines for I/O or memory accesses.
HD[31:0]	I/O	92-99, 1, 2, 4-9, 17-19, 14, 21-24, 29-36	***Data Bus Lines 0 to 31.*** This is the bi-directional data path from the host system to the VIC.
LCLK	I	89	***Local Bus Clock.*** This is the 1X system clock from the host.
LDEV#	O	86	***Local Device.*** This output indicates to the host that the current address on the VL-Bus is addressing the VIC.
LRDY#	O	87	***Local Ready.*** This signal begins the handshake with the host system that will eventually terminate the current VL-Bus cycle.
M/IO#	I	82	***Memory or I/O Status.*** This signal from the host system indicates that the current access on the VL-Bus is memory or I/O.
RESRV1	I	80	***Unused Input.*** Need to have a pull-up or pull-down.
RDYRTN#	I	85	***Ready Return.*** This signal indicates that the current cycle has ended.
RST#	I	79	***System Reset.*** This signal is used to initialize the VIC and any drives attached.
SPD1	I	3	***VL Bus Frequency Select (MSB).*** At reset time, this signal is sampled to set the Strap Register bit 1 which (along with Strap Register bit 0) decides the VL-Bus clock frequency. This may be connected to an external jumper or ID3 of the VL-Bus.

Name	Type	Pin	Description
W/R#	I	84	***Write or Read Status.*** This signal from the host system indicates that the current access on the VL-Bus is a write or a read.

3.2.3 IDE Interface in the 82C611 Compatible Mode

Name	Type	Pin	Description
DA[2:0]	O	53-51	***Drive Address Lines.*** This is the 3-bit binary coded address asserted by the host to access a register or data port in the drive.
DCHRDY	I	62	***I/O Channel Ready.*** This signal is negated to extend the host transfer cycle of any host register access (read or write) when the drive is not ready to respond to a data transfer request. When DCHRDY is not negated, DCHRDY is in a high impedance state.
DCS1#, DCS3#	O	43, 42	***Drive Chip Select 1 and 3 (bits 1 and 0).*** This is the chip select signal decoded from the host address bus used to select the Command and Control Block Registers.
DIOCS16#	I	63	***Drive 16-bit I/O.*** DIOCS16# indicates that the 16-bit data port has been addressed and that the drive is prepared to send or receive a 16-bit data word. If DIOCS16# is not asserted, transfers are 8-bit using DD[7:0]. If DIOCS16# is asserted, transfers are 16-bit using DD[15:0].
DRD#	O	54	***Drive I/O read.*** This is the Read strobe signal. The low level of DRD# enables data from a register or the data port of the drive onto the data bus DD[7:0] or DD[15:0].
DWR#	O	55	***Drive I/O write.*** This is the Write strobe signal. The rising edge of DWR# samples data from the data bus DD[7:0] or DD[15:0] into a register or the data port of the drive.
DINTR	I	81	***Drive interrupt.*** This signal is used to interrupt the host system. DINTR is asserted only when the drive has a pending interrupt, the drive is selected, and the host has cleared nIEN in the Device Control Register. DINTR is negated by: - assertion of DRST# or - the setting of SRST of the Device Control Register, or - the host writing the Command Register or - the host reading the Status Register DINTR is asserted at the beginning of each data block to be transferred. A data block is typically a single sector, except when declared otherwise by use of the Set Multiple command. An exception to this occurs on Format Track, Write Sector(s), Write Buffer and Write Long commands where DINTR is not asserted at the beginning of the first data block to be transferred
DRST#	O	57	***Drive reset.*** This signal is asserted for at least 25 µsec after voltage levels have stabilized during power on and negated thereafter unless some event requires that the drive(s) be reset following power on.
RD3F7#	O	56	***Read Port 3F7h Buffer Enable.*** This pin enables the buffer for SD[6:0] for a register 3F7h read if pin ISA3F7 has been sampled high.

Name	Type	Pin	Description
DD0 / SPD0	I/O		***Disk Data Bus Line 0/VL Bus Frequency Select (LSB).*** At reset time, this pin is sampled to set the Strap Register bit 0 (VL-bus frequency select, LSB). Along with SPD1 (MSB), SPD0 determines the exact VL-Bus frequency: SPD1 SPD0 Frequency 0 0 50 MHz 0 1 40 MHz 1 0 33 MHz 1 1 25 MHz
DD1 / PRIM	I/O		***Disk Data Bus Line 1/Primary Address.*** At reset time, this pin is sampled to set the Primary or Secondary IDE Port Address: 1 = Primary IDE (Address 1Fxh & 3Fxh), 0 = Secondary IDE (Address 17xh & 37xh)
DD[3:2]/ MODE[1:0]	I/O	47, 46	***Disk Data Bus Lines 3 and 2/Mode.*** At reset time, these pins are sampled to set the IDE Device Modes for 16-bit Cycle Times: Mode 1 Mode 0 Cycle-Time 0 0 ≥ 480ns 0 1 ≥ 383ns 1 0 ≥ 240ns 1 1 ≥ 180ns These pins are also used to enter one of four test modes if TMOD# is sampled low: Mode 1 Mode 0 Test Mode 0 0 Tri-state all output and bi-directional signals, 0 1 Output of input & bi-directional NAND chain on RD3F7# (all bi-directional signals tri-stated), 1 0 Drive all even pin outputs high and odd low, 1 1 Drive all odd pin outs high and even low
DD5/ISA3F7	I/O	44	***Disk Data Bus Line 5.*** At reset time, ISA3F7 is sampled to set the Strap Register bit 7 which decides whether read accesses to I/O port 3F7h come from the local bus or from the AT-Bus. 0 = 3F7h read from local bus, 1 = 3F7h read from AT-Bus bus
DD[7:6]/ VICID[1:0]	I/O	39, 38	***Disk Data Bus Lines 6 and 7/VL Bus IDE Controller ID.*** At reset time, these pins are sampled to set the ID of the VIC chip. The value read determines the ID of this device. After reset, the VIC with VICID = 11 (3h) has its IDE port enabled and all other VICs have their IDE port disabled. When programming the VIC configuration registers, the VICID field of the index register must match these VICID strap options.
DD8 / TMOD#	I/O	37	***Disk Data Bus Line 8/Test Mode.*** At reset time, TMOD# is sampled to enable test mode. This data bus line requires an external pull-up, and must be sampled high at the end of reset for normal operation. 0 = Test Mode, 1 = User Mode
DD10 / ENPREF	I/O	26	***Disk Data Bus Lines 10/Enable Prefetch.*** At reset, this signal is sampled to set the Miscellaneous Register bit 6 which enables or disables read prefetch. 1 = Enable, 0 = Disable

Name	Type	Pin	Description
DD[15:11, 9, 4]	I/O	10, 50, 12, 13, 25, 27, 45	***Disk Data Bus Lines 4, 9, 11 to 15.*** These are the data bus between the host and the drive and require external pull-ups.

3.2.4 AT-Bus Interface

Name	Type	Pin	Description
CHRDY	O	59	***I/O Channel Ready.*** This signal to the AT-Bus is used to extend the current cycle for non-0WS operations. This signal may go active for reads to I/O address 3F7h if the ISA3F7 pin strap is high.
IORC#	I	78	***I/O Read or Disk Change Line.*** This signal from the AT-Bus indicates that an I/O read operation is occurring. This signal is used to map read accesses to the 3F7h register. For configurations including a floppy controller, this signal can be connected to the drive-change line for shared operation.
IRQ14	O	61	***Interrupt Request Line 14.*** This output to the AT-Bus is used to request interrupt service from the host system.

3.2.5 Power and Ground Pins

Name	Type	Pin	Description
GND	I	15, 16, 28, 40, 58, 66, 88, 90, 100	VSS or Ground
Vcc	I	11, 20, 41, 67, 91	Vcc or +5v

4.0 Register Descriptions

The VIC contains registers at seven I/O ports accessible after two consecutive 16-bit I/O reads from address 1F1h (171h if secondary IDE address). Any other I/O cycle between these two reads will disable access to the VIC registers.

4.1 ID Register (1F2h / 172h, Write Only)

Bits	Mnemonic	Description	Default
7	CNFDIS	***Configuration Disable:*** This bit must be set to '0' in order to access VIC Internal Registers. Any write to this register with CNFDIS = 1 will disable all accesses to the VIC registers until another two consecutive I/O reads from 1F1h/171h.	1
6	CNFOFF*	***Configuration Off.*** This bit must be set to '0' in order to access VIC Internal Registers. Any write to this register with CNFOFF = 1 will disable all accesses to the VIC registers until power down or reset.	0
[5:2]	----	***Reserved:*** Must be written 0.	x
[1:0]	VICID[1:0]	***ID:*** This bit must match the VICID strap option in order to access VIC internal registers. In the New Mode, VICID1 strap option is not available and bit 1 of this register must always be written 1.	xx

4.2 Read Cycle Timing Register-A (1F0h / 170h, Index-0, R/W)

This register shares the I/O address with the Read Cycle Timing Register-B, indexed by the Miscellaneous Register bit 0. It controls the read cycle timing of IDE data register for the drive selected by the Control register bits [3:2]. The bit field of this register is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	RDPW[3:0]	***Read Pulse Width:*** The value programmed in this register determines the DRD# pulse width in LCLKs (for a 16-bit read from the IDE Data Register). See Table 4-6.	xxxx
[3:0]	RDREC[3:0]	***Read Recovery Time:*** The value programmed in this register determines the recovery time between the end of DRD# and the next DA[2:0]/DCSx# being presented (after a 16-bit read from the IDE Data Register), measured in LCLKs. See Table 4-7.	xxxx

4.3 Read Cycle Timing Register-B (1F0h / 170h, Index-1, R/W)

This register shares the I/O address with the Read Cycle Timing Register-A, indexed by the Miscellaneous Register bit 0. It controls the read cycle timing of IDE data register for the drive not selected by the Control register bits [3:2], if the Control Register bit 7 is set The bit fields of these registers is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	RDPW[3:0]	***Read Pulse Width:*** The value programmed in this register determines the DRD# pulse width in LCLKs (for a 16-bit read from the IDE Data Register). See Table 4-6.	xxxx
[3:0]	RDREC[3:0]	***Read Recovery Time:*** The value programmed in this register determines the recovery time between the end of DRD# and the next DA[2:0]/DCSx# being presented (after a 16-bit read from the IDE Data Register), measured in LCLKs. See Table 4-7.	xxxx

4.4 Write Cycle Timing Register-A (1F1h / 171h, Index-0, R/W)

This register shares the I/O address with the Write Cycle Timing Register-B, indexed by the Miscellaneous Register bit 0. It controls the write cycle timing of IDE data register for the drive selected by the Control register bits [3:2]. The bit field of this register is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	WRPW[3:0]	***Write Pulse Width:*** The value programmed in this register determines the DWR# pulse width in LCLKs (for a 16-bit write from the IDE Data Register). See Table 4-6.	xxxx
[3:0]	WRREC[3:0]	***Write Recovery Time:*** The value programmed in this register determines the recovery time between the end of DWR# and the next DA[2:0]/DCSx# being presented (after a 16-bit write from the IDE Data Register), measured in LCLKs. See Table 4-7.	xxxx

4.5 Write Cycle Timing Register-B (1F1h / 171h, Index-1, R/W)*

This register shares the I/O address with the Write Cycle Timing Register-A, indexed by the Miscellaneous Register bit 0. It controls the write cycle timing of IDE data register for the drive not selected by the Control register bits [3:2], if the Control Register bit 7 is set The bit fields of these registers is defined as follows:

Bits	Mnemonic	Description	Default
[7:4]	WRPW[3:0]	***Write Pulse Width:*** The value programmed in this register determines the DWR# pulse width in LCLKs (for a 16-bit write from the IDE Data Register). See Table 4-6.	xxxx
[3:0]	WRREC[3:0]	***Write Recovery Time:*** The value programmed in this register determines the recovery time between the end of DWR# and the next DA[2:0]/DCSx# being presented (after a 16-bit write from the IDE Data Register), measured in LCLKs. See Table 4-7.	xxxx

4.6 Control Register (1F3h / 173h, R/W)

Bits	Mnemonic	Description	Default
7	REGTIM2*	***Enable Timing Registers-B.*** When set, this bit enables cycle-timing registers-B (1F0h & 1F1h of the Index-1) to override the IDE timing set by the strap options for any drive not selected by 1F3h bit [3:2]. It also enables the miscellaneous timing register 1F6h bits [5:1] to override the timing set by the strap options.	0
6	EN0WSWR*	***Enable 0 Wait State Write.*** 1 = 0 WS for data writes, 0 = 1 WS minimum.	0
5	-	***Reserved:*** Must be written 0.	0
4	EN1WSRD	***Enable 1-Wait State Read.*** 1 = 1 WS minimum for data reads, 0 = 2 WS minimum.	0
3	REGTIM1	***Enable Timing Register-A, Drive 1:*** When set, this bit enables cycle-timing registers-A (1F0h & 1F1h of the Index-0) to override the IDE timing set by the strap options for Drive-1.	0
2	REGTIM0	***Enable Timing Register-A, Drive 0:*** When set, this bit enables cycle-timing registers-A (1F0h & 1F1h of the Index-0) to override the IDE timing set by the strap options for Drive-0.	0
1	ENSMI	***Enable SMI:*** When set, this bit generates an SMI upon access to any IDE I/O address, if ENDO is 1 and CNFDIS is 1. Clearing this bit will reset SMI and disables it.	0
0	ENDO	***Enable Operation:*** When set, this bit will enable IDE operation and IRQ14. When cleared, this bit will disable IDE operation (sets all outputs to tri-state/inactive state). After reset, ENDO = 1 for the VIC with VICID[1:0] = 11 and ENDO = 0 for any other VIC.	1

*. These registers are available in the 82C611 Enhanced Mode only.

Note For all new software controls the IDE timing through registers programming, bits 2, 3 and 7 of the Control register should be enabled after the Cycle Timing Registers and Miscellaneous Register are programmed. Refer to Table 4-1 to program those 3 bits.

4.7 Strap Register (1F5h/175h)

Bits	Mnemonic	Description	Default
7	ISA3F7*	***ISA 3F7 Read (Read/Write).*** Decides whether read access to 3F7h comes from local bus or ISA Bus. 0 = 3F7h read from local bus. 1 = 3F7h read from ISA Bus	
[6:5]	REV[1:0]	***Revision Number Register (Read Only).*** First Production Samples are set to '01'.	01
4	DINTR	***DINTR Status (Read Only).*** Returns the state of DINTR input.	
[3:2]	MODE[1:0]	***Mode (Read Only).*** Returns information about drive speed as determined by MODE[1:0] strap options. Please refer to the Mode Strap description for specific information.	
[1:0]	SPD[1:0]*	***LCLK Speed (Read/Write).*** VL-Bus LCLK frequency select. At reset time, the value of these bits is set by the sampling of SPD[1:0] strap options. SPD[1:0]LCLK 0 0 50 MHz 0 1 40 MHz 1 0 33 MHz 1 1 25 MHz	

*. These register-bits were read-only in the 82C611.

4.8 SMI Address Register (1F2h/172h, Read Only)

Bits	Mnemonic	Description	Default
7	SMI	***SMI Status:*** This reflects the state of the SMI output from the VIC.	x
6	SMIW/R#	***SMI Last W/R#:*** The value of W/R# during the cycle that last caused an SMI.	x
5	SMIA9	***SMI Last A9:*** The value of HA9 during the cycle that last caused an SMI.	x
4	SMIA2	***SMI Last A2:*** The value of HA2 during the cycle that last caused an SMI.	x
[3"0]	SMIBE[3:0]	***SMI Last BEx#:*** The value of BE[3:0] during the cycle that last caused an SMI.	xxxx

4.9 SMI Data Register (1F4h/174h, Read Only)

Bits	Mnemonic	Description	Default
[7:0]	SMIDATA	SMI Data: If an 8-bit write cycle caused an SMI, this register returns the data written in that cycle.	xxxx xxxx

4.10 Miscellaneous Register (1F6h/176h, R/W)*

Bits	Mnemonic	Description	Default
7	IDEFLOAT	***IDE Pins Float:*** When set, tri-states all the outputs and bi-directional pins connected to the IDE drive. (DRST#, DRD#, DWR#, DCS#3, DCS1#, DA[2:0] and DD[15:0])	0
6	ENPREF	***Enable Read Prefetch:*** Enables/Disables Read Prefetch. At reset time, the value of this register is set by ENPREF strap option.	1 = Enable, 0 = Disable.
[5:4]	ASU[1:0]	***Address Setup Time:*** The value programmed in this register determines the address setup time between the DRD# or DWR# going active and the DA[2:0], DCS3#, DCS1# being presented, measured in LCLKs. See Table 4-4.	x
[3:1]	DRDY[2:0]	***DRDY Delay:*** The value programmed in this register determines the minimum number of LCLKs between DRDY# going high and DRD# or DWR# going inactive. See Table 4-5.	xx
0	INDEX-0	***Index-0:*** This bits is used to select between Cycle Timing Registers-A and -B located at 1F0h and 1F1h.	0

4.11 Programming the IDE Controller Registers

The following steps describe how to program the 82C611A index registers to support different IDE modes. The chip should be booted at 50MHz, mode 0 (from strapping), before you program different modes.

1. Program proper values into 1F0h and 1F1h, they are the default for Timing Register-A.
2. Set bit 0 of 1F6h to 1 to switch to Timing Register-B.
3. Program proper values into 1F0h and 1F1h, they reflect Timing Register-B.
4. Program proper values into bits [5:1] of 1F6h. It affects both Timing Register-A and Timing Register-B.
5. Enable bits 2, 3 and 7 in 1F3h. The following table describes the options for programming these three bits:

Table 4-1 REGTIMx Programming Options

REGTIM0	REGTIM1	REGTIM2	Drive 0 Control	Drive 1 Control
1*	0	1	Index-0	Index-1
0	1	1	Index-1	Index-0
0	0	1	Index-1	Index-1
1	0	0	Index-0	Straps
0	1	0	Straps	Index-0
0	0	0	Straps	Straps
1	1	x	Index-0	Index-0

*. Recommended Configuration

The following tables show the recommended index register clock settings to interface to different modes of the IDE drives.

*. These registers are available in the 82C611 Enhanced Mode only

Table 4-2 16-Bit Timing (LCLKs)

	VESA Bus Frequency															
	25MHz, 40ns				33MHz, 30ns				40MHz, 25ns				50MHz, 20ns			
Mode	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
Address Setup	2	2	1	1	3	2	2	1	3	3	2	2	4	3	2	2
Command Pulse	5	4	3	2	6	5	4	3	7	6	5	4	9	7	6	5
Recovery Time	8	4	2	2	11	6	2	2	14	7	3	2	17	10	4	2
DRDY	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2

Table 4-3 8-Bit Timing (LCLKs)

	VESA Bus Frequency															
	25MHz, 40ns				33MHz, 30ns				40MHz, 25ns				50MHz, 20ns			
Mode	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
Address Setup	2	2	1	1	3	2	2	1	3	3	2	2	4	3	2	2
Command Pulse	8	8	8	8	10	10	10	10	12	12	12	12	15	15	15	15
Recovery Time	6	6	6	6	9	9	9	9	11	11	11	11	14	14	14	14
DRDY	3	3	3	3	4	4	4	4	5	5	5	5	6	6	6	6

Note The 8-bit settings are fixed and cannot be programmed.

Table 4-4 Address Setup

Bit 5	Bit 4	Timing, in LCLKs
0	0	1
0	1	2
1	0	3
1	1	4

Note Index Registers 1F6h/176h bits [5:4]

Table 4-5 DRDY Delay

Bit 3	Bit 2	Bit 1	Timing, in LCLKs
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	7
1	1	0	8
1	1	1	9

Note Index Registers 1F6h/176h bits [3:1]

Table 4-6 Read/Write Command Pulse

Bit 7	Bit 6	Bit 5	Bit 4	Timing, in LCLKs	
				Read Command 1F0h/170h	Write Command 1F1h/171h
0	0	0	0	1	1
0	0	0	1	2	2
0	0	1	0	3	3
0	0	1	1	4	4
0	1	0	0	5	5
0	1	0	1	6	6
0	1	1	0	7	7
0	1	1	1	8	8
1	0	0	0	9	9
1	0	0	1	10	10
1	0	1	0	11	11
1	0	1	1	12	12
1	1	0	0	13	13
1	1	0	1	14	14
1	1	1	0	15	15
1	1	1	1	16	16

Note Index Registers 1F0h/170h (Read) or 1F1h/171h (Write), Index 0/1, bits [7:4]

Table 4-7 Read/Write Recovery Time

Bit 3	Bit 2	Bit 1	Bit 0	Timing, in LCLKs	
				Read Recovery 1F0h/170h	Write Recovery 1F1h/171h
0	0	0	0	2	2
0	0	0	1	3	3
0	0	1	0	4	4
0	0	1	1	5	5
0	1	0	0	6	6
0	1	0	1	7	7
0	1	1	0	8	8
0	1	1	1	9	9
1	0	0	0	10	10
1	0	0	1	11	11
1	0	1	0	12	12
1	0	1	1	13	13
1	1	0	0	14	14
1	1	0	1	15	15
1	1	1	0	16	16
1	1	1	1	17	17

Note Index Registers 1F0h/170h (Read) or 1F1h/171h (Write) Index 0/1, bits [3:0]

5.0 Electrical Specification

Temperature: 0C to 70C, Vcc: 5V +/- 5%, 50pF load

5.1 Absolute Maximum Ratings

Sym.	Description	Min	Max	Units
V_{CC}	Supply Voltage		6.5	V
V_I	Input Voltage	-0.5	V_{CC} + 0.5	V
V_O	Output Voltage	-0.5	V_{CC} + 0.5	V
T_{OP}	Operating Temperature	0	70	°C
T_{STG}	Storage Temperature	-40	125	°C

5.2 DC Characteristics

Sym.	Description	Min	Max	Units
$V_{IL}1$	Input Low Voltage (DA[2:0], DCS1#, DCS3#)		0.8	V
$V_{IH}1$	Input High Voltage (DA[2:0], DCS1#, DCS3#)	3.85		V
$V_{IL}2$	Input Low Voltage (for all other pins)		0.8	V
$V_{IH}2$	Input High Voltage (for all other pins)	2.0		V
V_{OL}	Output Low Voltage - 4mA for SMI, HD[31:0], IRQ14, RD3F7#. - 8mA for LDEV#, LRDY#. - 12mA for CHRDY, DA[2:0], DCS1#, DCS3#, DD[15:0], DRD#, DWR#.		0.5	V
V_{OH}	Output High Voltage - 4mA for SMI, HD[31:0], IRQ14, RD3F7#. - 8mA for LDEV#, LRDY#. - 12mA for CHRDY, DA[2:0], DCS1#, DCS3#, DD[15:0], DRD#, DWR#.	2.4		V
I_{IL}	Input Leakage Current (V_{IN} = V_{CC})		10	uA
I_{OZ}	Tri-state Leakage Current		10	uA
C_{IN}	Input Capacitance		10	pF
C_{OUT}	Output Capacitance		10	pF
C_{IO}	I/O Capacitance		12	pF
I_{CC}	Power Supply Current		TBA	mA
I_{CCS}	Power Supply Current, Standby		TBA	mA

5.3 AC Characteristics

Sym.	Description	Min (ns)	Typ. (ns)	Max (ns)
t1	ADS# setup time to LCLK ⇧	4.0		
t2	ADS# hold time to LCLK ⇧	1.7		
t3	HA[9:2], M/IO#, W/R#, BE[3:0]# setup time to LCLK ⇧	4.0		

Sym.	Description	Min (ns)	Typ. (ns)	Max (ns)
t4	HA[9:2], M/IO#, W/R#, BE[3:0]# hold time to LCLK ⇧	1.0		
t5	RDYRTN# setup time to LCLK ⇧	4.0		
t6	RDYRTN# hold time to LCLK ⇧	2.0		
t7	HD[31:0] setup time to LCLK ⇧	4.0		
t8	HD[31:0] hold time to LCLK ⇧	0.0		
t9	M/IO#, W/R#, BE[2:0]#, HA[9:2] to LDEV# valid	1.0	6.0	20.0
t10	LCLK⇧ to LDEV# valid (reg/parll)	2.0	9.0	25.0
t11	LCLK⇧ to LRDY# active	4.0	9.0	14.0
t12	LCLK⇧ to LRDY# inactive	3.0	8.0	17.0
t13	LCLK⇩ to LRDY# float	5.0	12.0	20.0
t14	MIO#, W/R#, BE[2:0]#, HA[9:2] to LRDY# valid (0 WS)	1.0	8.0	22.0
t15	LCLK⇧ to HD[31:0] valid	3.0	14.0	35.0
t16	LCLK⇧ to HD[31:0] float	3.0	12.0	21.0
t17	LCLK⇩ to HD[31:0] valid (1 WS Read)	3.0	12.0	23.0
t21	DSKCHG# active to HD[31:0] valid	1.0	9.0	30.0
t22	DINTR active to HD[31:0] valid	1.0	9.0	30.0
t23	LCLK⇧ to DD[15:0] valid	3.0	12.0	35.0
t24	LCLK⇧ to DD[15:0] float	3.0	12.0	30.0
t25	LCLK⇧ to CHRDY# valid	3.0	9.0	20.0
t26	LCLK⇧ to CHRDY# float	3.0	9.0	20.0
t27	LCLK⇧ to SMI active	3.0	14.0	40.0
t28	LCLK⇧ to RD3F7# active	6.0	17.0	33.0
t29	IORC# active to RD3F7# active	2.0	10.0	33.0
t30	IORC# inactive to RD3F7# inactive	2.0	10.0	33.0
t31	LCLK⇧ to DRD#, DWR#, DA[2:0], DCS3#, DCS1# valid	3.0	11.0	30.0
t32	LCLK⇧ to DRD#, DWR#, DA[2:0], DCS3#, DCS1# invalid	3.0	11.0	30.0
t33	RST# active to DRST# active delay	2.0	10.0	20.0
t34	DINTR active to IRQ14 active delay	1.0	10.0	30.0

5.4 Timing Waveforms

Figure 5-1 82C611A to IDE Interface

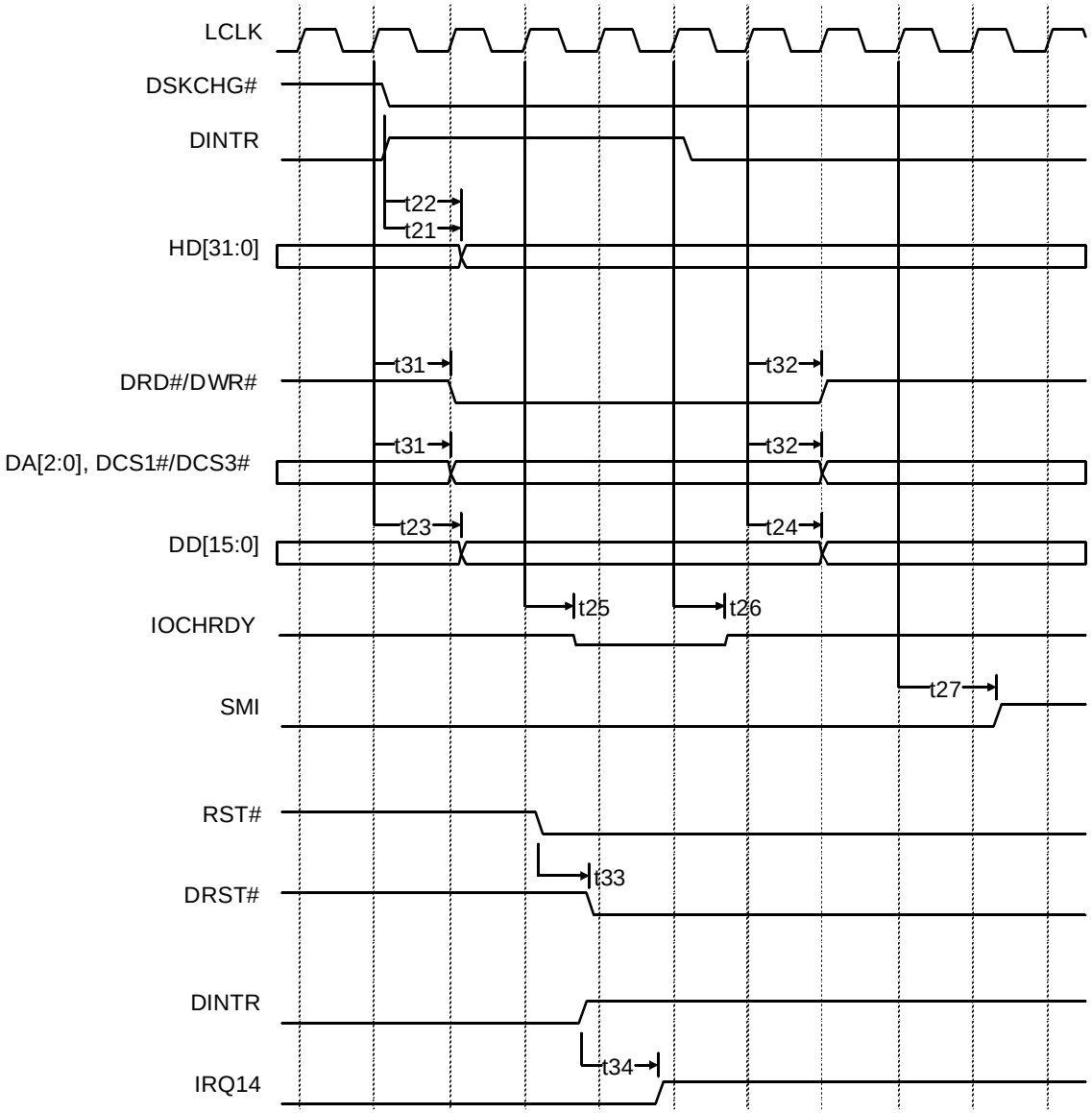


Figure 5-2 82C611A to IDE Interface

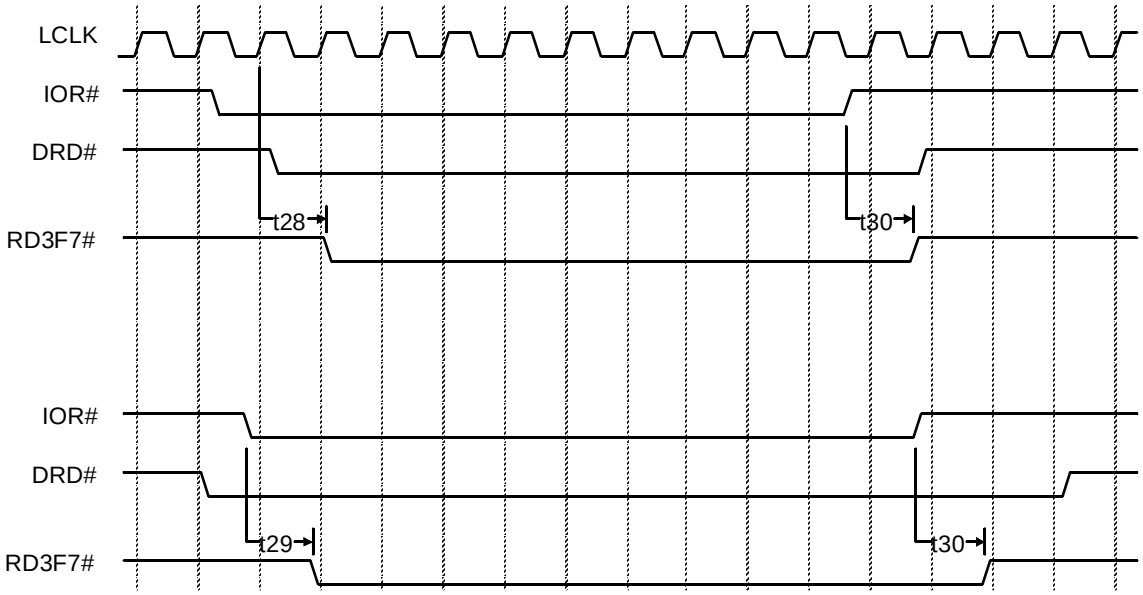
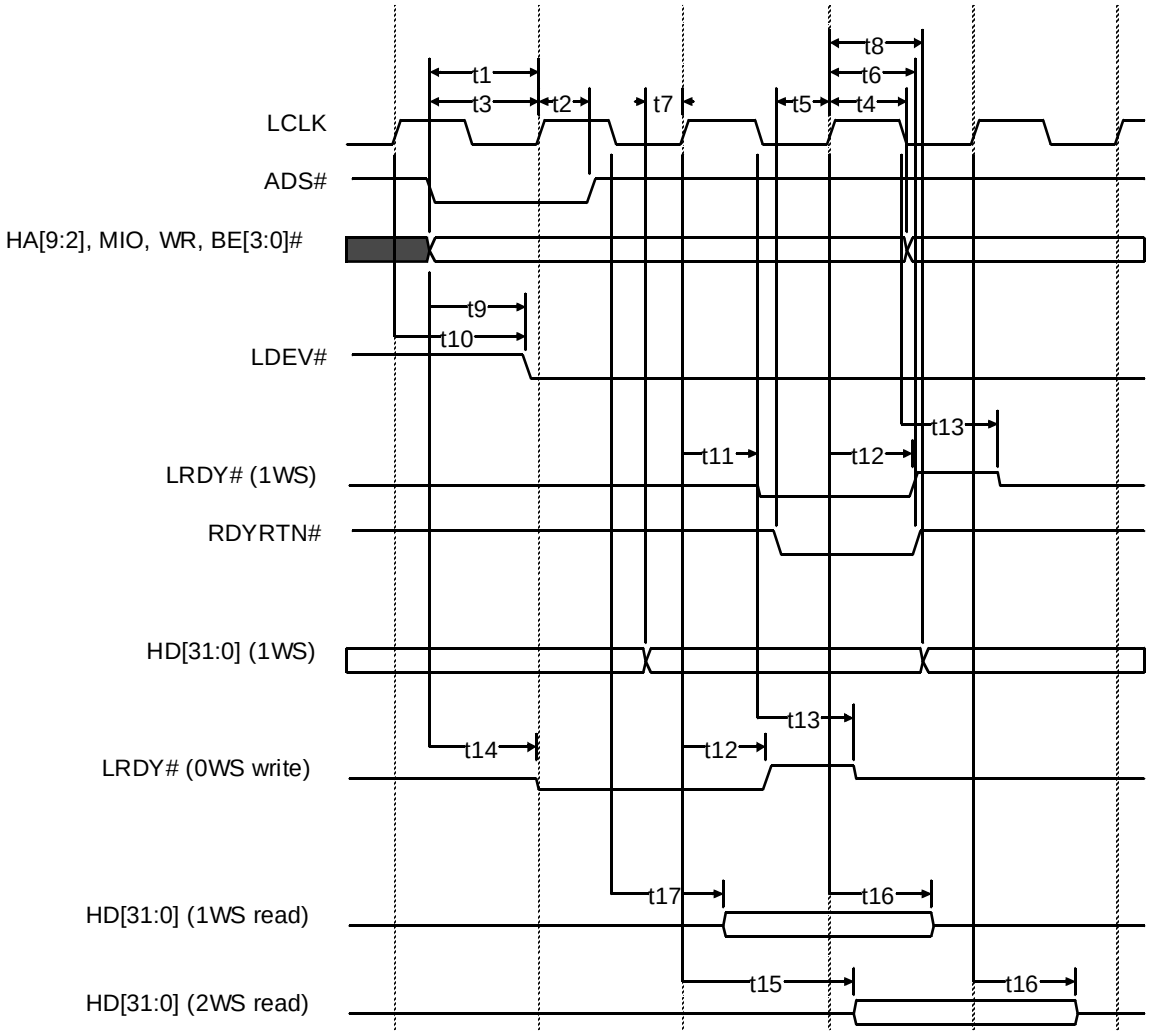
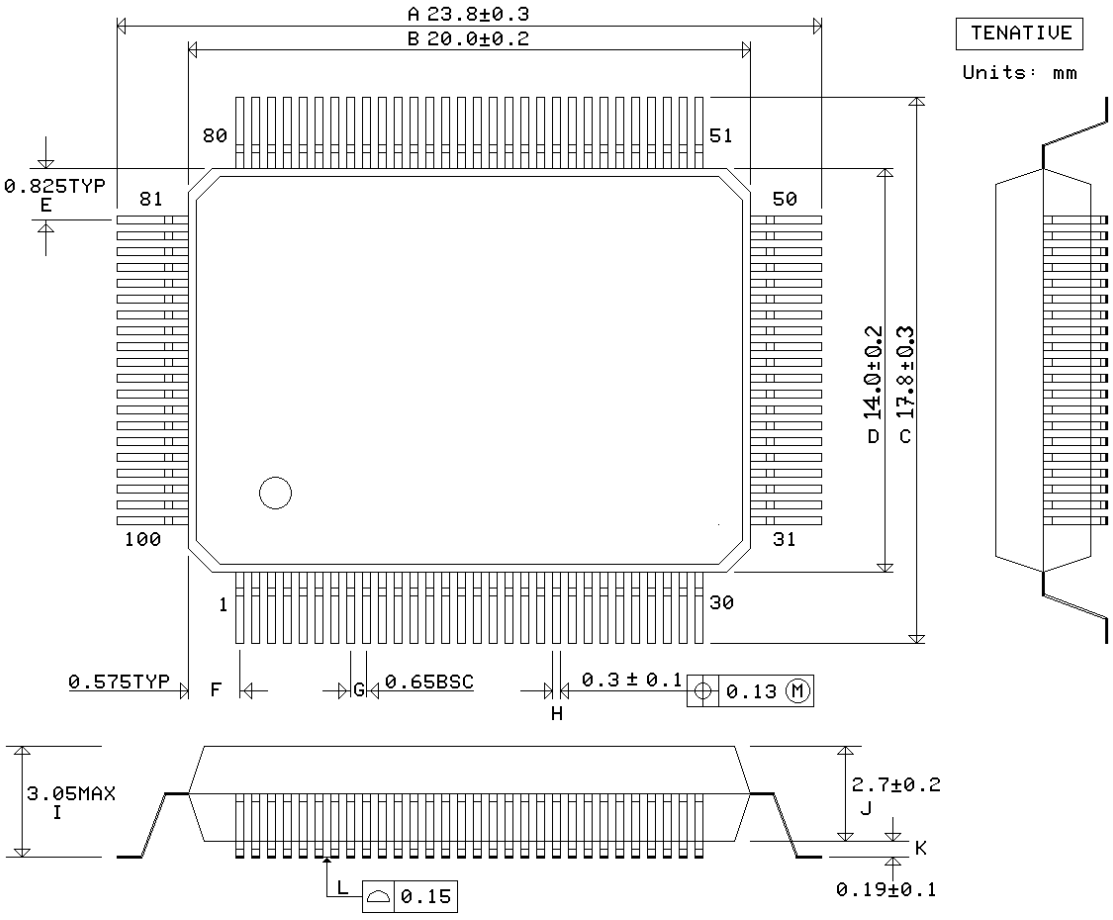


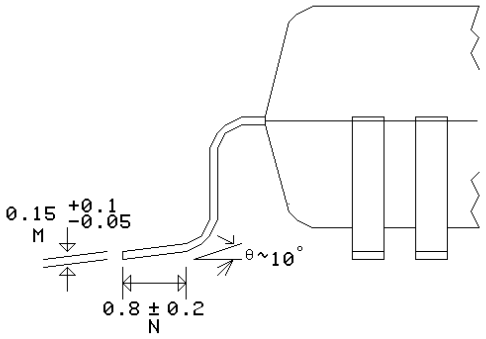
Figure 5-3 82C611A to VESA Interface



6.0 Mechanical Package



DIM	MILLIMETERS		INCHES		DESCRIPTION
	MIN	MAX	MIN	MAX	
A	23.5	24.1	.925"	.949"	Maximum Width LEAD TO LEAD
B	19.8	20.2	.779"	.795"	Maximum Width PACKAGE ENVELOPE
C	17.5	18.1	.689"	.713"	Maximum Height LEAD TO LEAD
D	13.8	14.2	.543"	.559"	Maximum Height PACKAGE ENVELOPE
E	0.825 TYP		.0325" TYP		LEAD CENTER TO PERP. LEAD PLANE
F	0.575 TYP		.0226" TYP		LEAD CENTER TO PERP. LEAD PLANE
G	0.65 BSC		.0256" BSC		LEAD TO LEAD CENTER SPACING
H	0.2	0.4	.008"	.016"	LEAD WIDTH
I	——	3.05	——	.120"	PACKAGE HEIGHT LEAD PLANE TO TOP
J	2.5	2.9	.098"	.114"	MAXIMUM THICKNESS PACKAGE ENVELOPE
K	0.09	0.29	.0035"	.0114"	LEAD PLANE TO PACKAGE BOTTOM
L	——	0.15	——	.006"	LEAD PLANE SKEW
M	0.1	0.25	.004"	.010"	LEAD THICKNESS
N	0.6	1.0	.024"	.039"	LEAD FOOTPRINT



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