

OAK TECHNOLOGY

OTI-911LP

IDE CD-ROM Controller

FEATURES

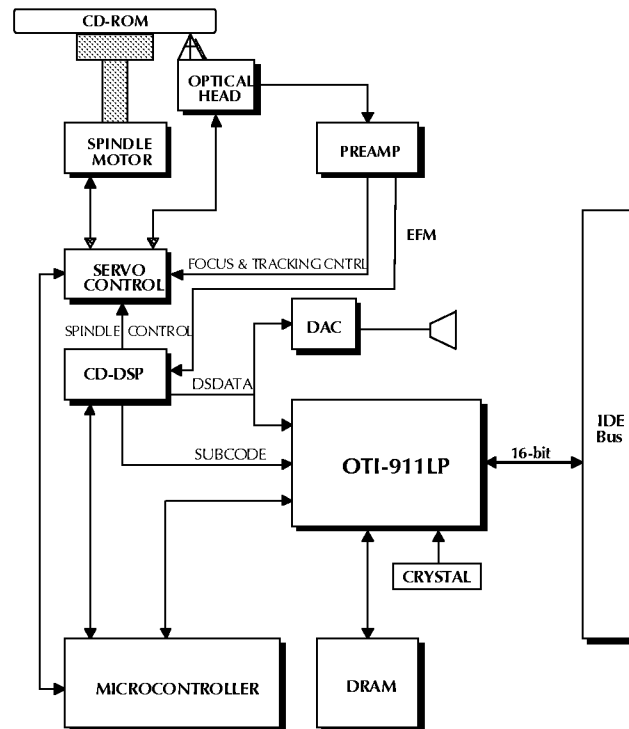
- ◆ ATAPI (SFF-8020) standard support
- ◆ Supports CD-ROM disk speeds greater than 20x
- ◆ PIO Native Mode 4 support
- ◆ Mode 0, 1, and 2 multi-word DMA support
- ◆ Reduced power consumption and EMI
- ◆ Supports higher disk speed than OTI-911 with H/W flow control
- ◆ Direct register addressing
- ◆ Increased FIFO buffering depth for improved host performance
- ◆ Multi-block support transfers up to 31 blocks in a single transfer
- ◆ Can be used in design with popular microcontrollers and CD-DSPs
- ◆ Memory interface supports industry-standard DRAMs (256K x 4, 256K x 8, 128K x 8, 1 Meg x 4)
- ◆ Real-time error correction up to 138 P and Q byte errors per block
- ◆ Allows data transfers from RAM to the host bus through the microcontroller
- ◆ Segmented memory support for sophisticated caching schemes
- ◆ 100-pin PQFP

DESCRIPTION

Oak Technology's OTI-911LP CD-ROM controller contains new features and enhancements required by tomorrow's ATAPI CD-ROM drives. Peak data rates required by the drive interface controller have increased dramatically due to a recent shift towards CAV (Constant Angular Velocity) drives. The flexible architecture and features of the OTI-911LP allow for use at peak data rates above 20X while supporting PIO mode 4 and DMA mode 2 timing requirements. This capability has already been realized and proven at the system level. Designs with firmware are available that ease the task of implementing an ATAPI interface capable of handling the high data rates of a CAV drive.

The OTI-911LP has advanced power management and EMI (Electromagnetic Interference) reduction features. It also has a programmable DRAM refresh rate and programmable I/O drive buffers on all of its major interfaces. This, in conjunction with a more efficient internal architecture, provides a significant reduction in both power consumption and EMI.

(continued)



Block Diagram of CD-ROM Drive Electronics

OTI-911LP

Description and Enhancements

Description (continued)

The OTI-911LP performs simultaneous disk data buffering, real-time error correction, and data transfers to the host. This provides the fastest possible access to data as it is available from the DSP during transfers at peak disk speeds and after seeks.

The OTI-911LP is designed for operation in a system with industry standard microcontrollers, DRAMs, and CD-DSPs. The OTI-911LP decodes CD-ROM data according to the Sony-Philips CD-ROM, CD-ROM/XA, CD-I, Multi-Session Photo CD, CD-G, CD+, CD-Extra, and CD-Audio formats. By programming the serial data input pin, the OTI-911LP can work with CD-DSPs from a variety of suppliers. Once data is passed from the CD-DSP to the OTI-911LP, real-time ECC logic corrects 138 P and Q byte errors per block. The OTI-911LP can perform repeated ECC passes without disabling CD-DSP buffering for data integrity without compromising speed. The OTI-911LP host interface supports the IDE interface on an ISA, PCI, or VL bus, providing 16-bit data transfers from chip to host. The host interface has built-in output buffers that directly drive the IDE bus and also contains control and transfer-status registers to which the host has access.

OTI-911LP Enhancements Summary

- ◆ Drop-in replacement for OTI-911
- ◆ Improved power management (sleep with refresh and programmable refresh rate)
- ◆ Glitch filters (1.5 ns nominal) on rising edge of HRD#, HWR#, DMACK#, URD#, UWR#
- ◆ Glitch filter (4-5 RXIN clocks) on falling edge of HRST# and PRST#
- ◆ Eliminated unnecessary accesses and cycles to DRAM
- ◆ Reduced current output of: RAD10 - 13 to 4 mA (8 mA)
- ◆ Eliminated DECCLR from clearing the 91XADVCL register
- ◆ MCK pin has selectable output 1X, 1/2X, or 1/4X of RXIN
- ◆ Doubled the EDAC threshold range by adding EDACSCCLR bit
- ◆ I/O pads for DRAM, microcontroller and host I/F have programmable drive current levels

OTI-911LP

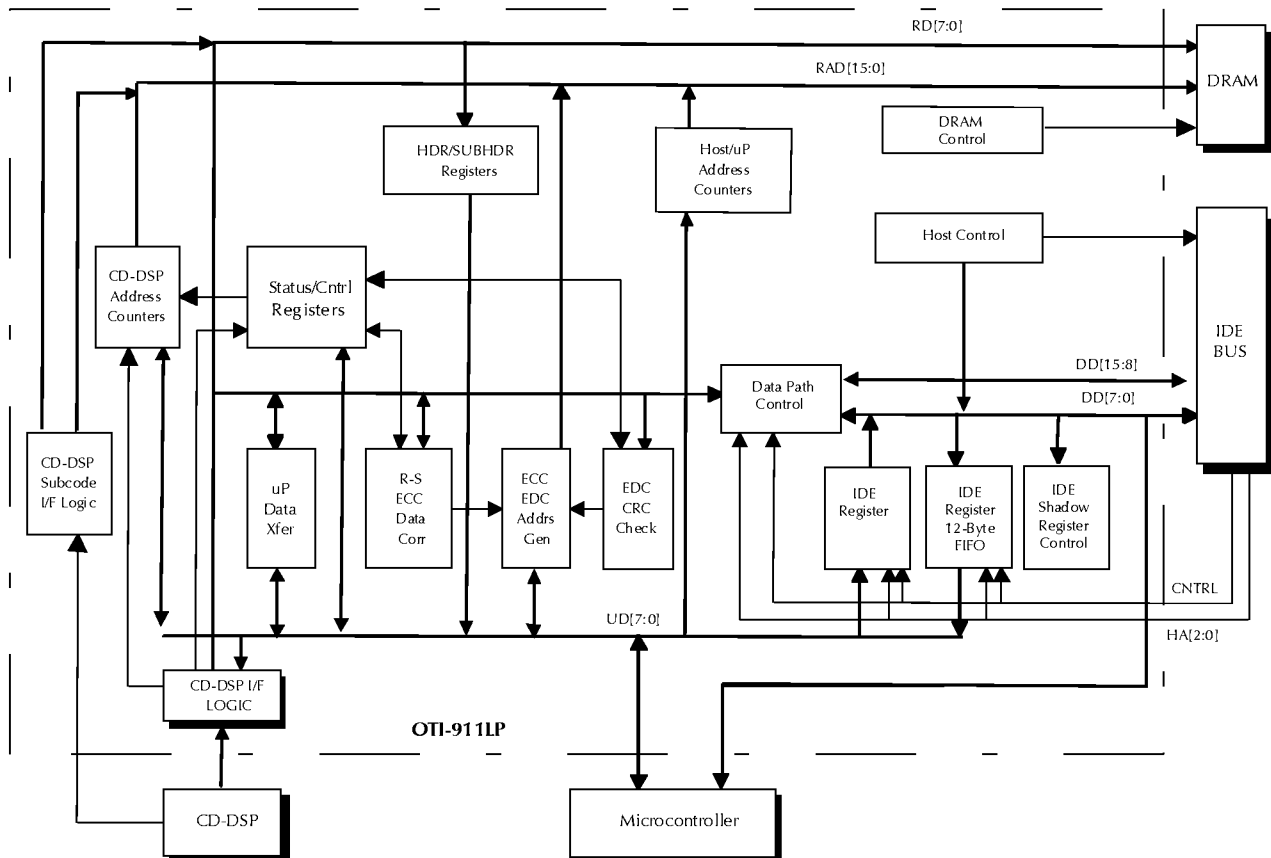
Block Diagram Description

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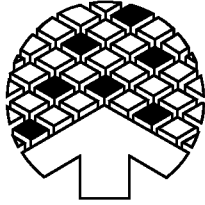
The key functional blocks in the OTI-911LP are: CD-DSP Interface, Buffer RAM Control, ECC Data Corrector, EDC CRC Checker, Microcontroller Interface, and IDE Interface. The CD-DSP Interface descrambles and assembles data from the CD-DSP chip, then stores the data into the RAM. The CD-DSP interface also assembles subcode and stores P-W data into the RAM. The ECC Data Corrector performs Reed-Solomon Error Correction on each block, then the EDC CRC Checker performs a cyclic redundancy check of the corrected data. The IDE Interface allows the corrected data to be transferred from the RAM to the Host. Operation of the OTI-911LP is controlled by the microcontroller through an 8-bit bus.

CD-ROM formats divide each 2KB data block into two planes, each plane containing 43 P-codewords and 26 Q-codewords. Each codeword contains two parity bytes. The OTI-911LP can correct one error in each code-word. Error correction and CRC checking is done by hardware inside the OTI-911LP. Normally, the correction sequence is Q-codeword followed by P-codeword.

The OTI-911LP also provides registers for transferring data between the microcontroller and the RAM.



OTI-911LP Block Diagram



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