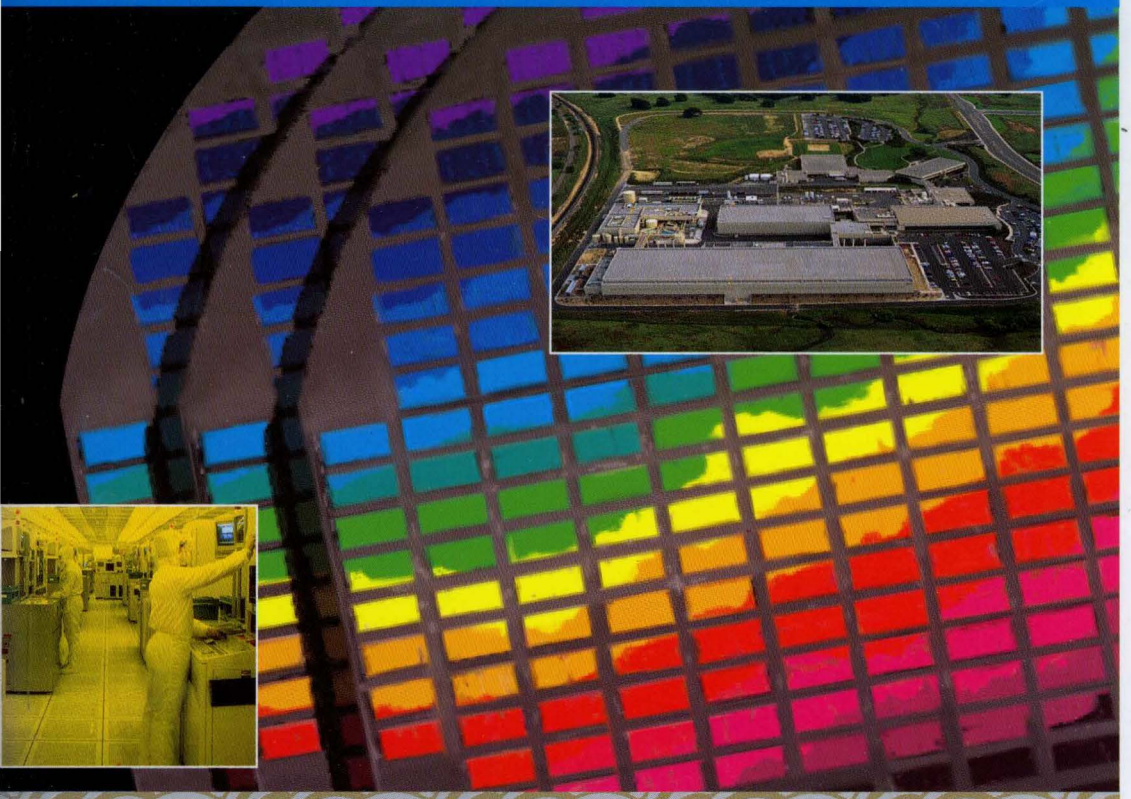


MEMORY PRODUCTS DATA BOOK
Volume 1 of 2
DRAMs, DRAM Modules, Video RAMs

NEC

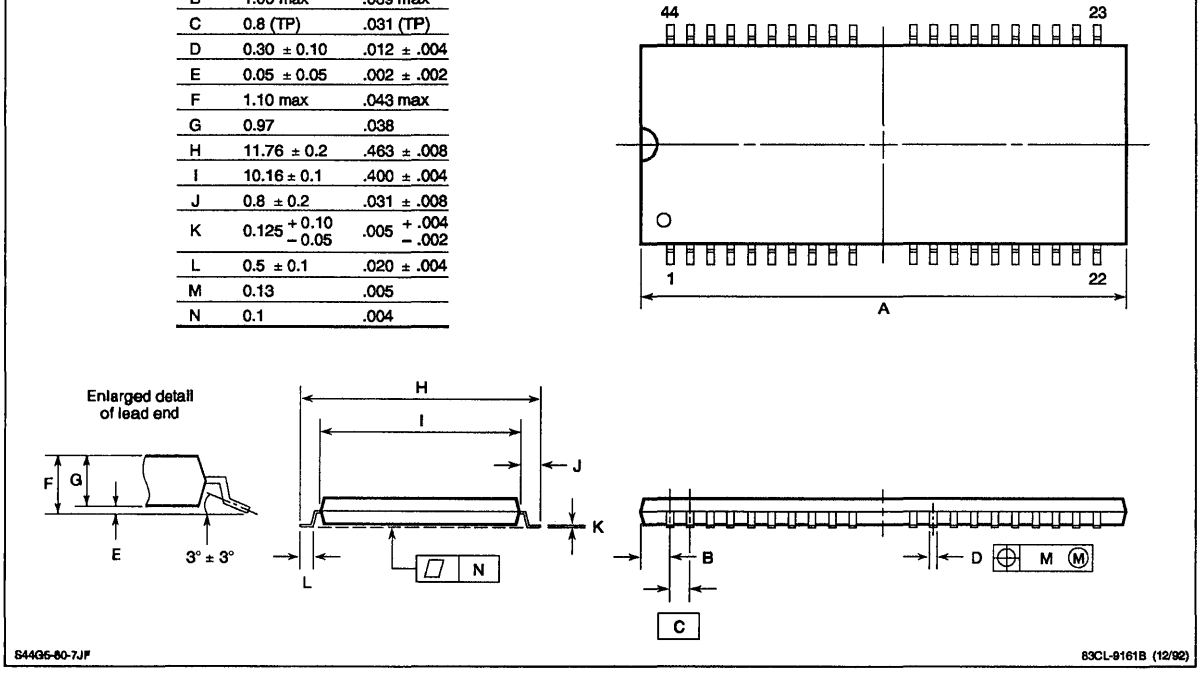
These corrections are applicable to the Package Drawings, Section 16 in Volume 1 and Section 29 in Volume 2. Devices affected are the 256K x 16/18 DRAMs listed below.

μPD424170A	μPD42S4170A
190A	190A
260A	260A
263A	263A
280A	280A
μPD424170L	μPD42S4170L
190L	190L
260L	260L
263L	263L
280L	280L

- Sections 16 and 29, pages 7, 8, and 12:
  In the descriptions of the affected devices, change "300-mil" to "400-mil".
- Sections 16 and 29, page 52:
  Replace the 300-mil package drawing with the 400-mil package drawing below.

44/40-Pin Plastic TSOP II (400-mil)

Item	Millimeters	Inches
A	18.81 max	.741 max
B	1.00 max	.039 max
C	0.8 (TP)	.031 (TP)
D	0.30 ± 0.10	.012 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.043 max
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	.020 ± .004
M	0.13	.005
N	0.1	.004



NEC Electronics Inc.

NEC

1993
MEMORY PRODUCTS
DATA BOOK

Volume 1 of 2
DRAMs, DRAM Modules, Video RAMs

Document No. 60105-1-V1

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NEC

Volume 1

Section 1. General Information

Section 2. Reliability and Quality Control

Section 3. 256K DRAMs

Volume 1 (cont)

Volume 1 (cont)

Volume 1 (cont)

Section 7. 4M DRAMs (256K x 16/18) (cont)

Section 8. 16M DRAMs

Volume 1 (cont)

Section 8. 16M DRAMs (cont)

Volume 1 (cont)

Volume 1 (cont)

Volume 1 (cont)

Section 15. Application Notes

Section 16. Package Drawings

Volume 2

Section 17. General Information

Section 18. Application Specific Devices (See App Notes 54 thru 58, 90-03, 90-06.)

Volume 2 (cont)

Volume 2 (cont)

Volume 2 (cont)

Section 27. EEPROMs

Section 28. Application Notes

Section 29. Package Drawings

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Section 1
General Information

The 1993 MEMORY DATA BOOK is for your reference. The most complete information available at printing is included; however, several new devices will be available soon. The table below gives you a preview. For further assistance, contact one of the sales offices.

Upcoming Products

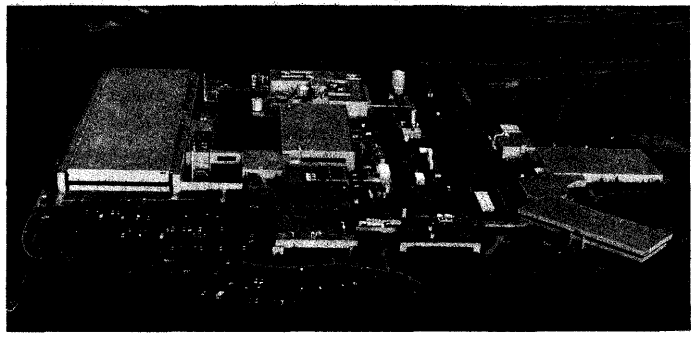
Description	Device Number	Comments
DRAM SIMM Modules		
4M x 8 DRAM Module	MC-424000A8BB/FB	Uses 16M devices
4M x 9 DRAM Module	MC-424000A9BB/FB	Uses 16M devices
16M x 8 DRAM Module	MC-4216000A8BH/FA/AA	Uses 16M devices
16M x 9 DRAM Module	MC-4216000A9BH/FA/AA	Uses 16M devices
4M x 40 DRAM Module	MC-424000AA40BH/FH	Uses 16M devices
8M x 40 DRAM Module	MC-428000AA40BH/FH	Uses 16M devices
Video RAMs		
4M Video RAM	μPD482445	256K x 16; RAM port access times to 60 ns; serial port access times to 15 ns; 64-pin SSOP, 70-pin TSOP
Standard SRAMs		
32K x 8	μPD43256A-10X, 12X	−25 to +85°C; speeds to 100 ns
32K x 8	μPD43256A-10Y, 12Y	−40 to +85°C; speeds to 100 ns
32K x 8	μPD43256B-A12	3.0 to 5.5 V; 120-ns access time
32K x 8	μPD43256B-B12	2.7 to 5.5 V; 120-ns access time
128K x 8	μPD431000A-70X, 85X, 100X	−25 to +85°C; speeds to 70 ns
128K x 8	μPD431000A-70Y, 85Y, 100Y	−40 to +85°C; speeds to 70 ns
128K x 8	μPD431000B-55L/LL, 70L/LL, 85L/LL	Low power; speeds to 55 ns
128K x 8	μPD431000B-B10, B12	2.7 to 5.5 V; speeds to 100 ns
128K x 9	μPD431003	Low power; speeds to 55 ns; two Chip Enables
128K x 9	μPD431003-B10, B12	2.7 to 5.5 V; speeds to 100 ns; two Chip Enables
512K x 8	μPD434000-B15	2.7 to 5.5 V; 150-ns access time; two Chip Enables
BiCMOS Fast SRAMs		
32K x 8	μPD46258	Speeds to 6 ns; 3.3- and 5-V versions
32K x 9	μPD46259	Speeds to 6 ns; 3.3- and 5-V versions
128K x 8	μPD461008	Speeds to 8 ns; 3.3- and 5-V versions
128K x 9	μPD461009	Speeds to 8 ns; 3.3- and 5-V versions
64K x 16	μPD461016	Speeds to 8 ns; 3.3- and 5-V versions
64K x 18	μPD461018	Speeds to 8 ns; 3.3- and 5-V versions

Upcoming Products (cont)

Description	Device Number	Comments
ECL RAMs (10K Interface)		
16K x 4	μPD10494	T_{AA} = 6, 7 ns; 28-pin PDIP/PFP
16K x 4	μPD10494LL	Tcycle = 10, 12 ns; 32-pin PDIP/PFP
32K x 9	μPD10509	Tcycle = 6, TDQ=3; registered I/O, scannable; 52-pin PLCC
64K x 4	μPD10504	T_{AA} = 8, 10 ns; 32-pin PDIP/PFP
ECL RAMs (101/100K Interface)		
16K x 4	μPD101/100494	T_{AA} = 6, 7 ns; 28-pin PDIP/PFP
16K x 4	μPD101/100494LL	Tcycle = 10, 12 ns; 32-pin PDIP/PFP
32K x 9	μPD101/100509	Tcycle = 6, TDQ=3; registered I/O, scannable; 52-pin PLCC
64K x 4	μPD101/100504	T_{AA} = 8, 10 ns; 32-pin PDIP/PFP

Manufacturing in Roseville, California

The planning was completed in 1981, ground was broken in 1982 and products were rolling off the line in 1984 at our semiconductor fabrication facility in Roseville, California. This milestone represented NEC's bold approach to "make products where the customer lives," and it was the first such venture by a Japanese semiconductor company in the United States. The foresight of this decision has paid off handsomely for NEC, its U.S. customers and for the community of greater Sacramento, the capital of California. The original facility has been manufacturing 256K DRAMs and VRAMs, 32K x 8 SRAMs, CMOS ASICs and single-chip microprocessors using 1.2-micron CMOS and NMOS technologies.



Now another milestone has been reached. In November 1991, production of the 4M DRAM began from a newly constructed 456,000-square-foot plant. Combined with the existing 220,000 square-foot facility, NEC Electronics (NECEL) in Roseville is one of the largest merchant fab lines in the world, according to industry source DataQuest.

In addition to the 4M DRAM, the new plant will be capable of producing advanced VLSI products including 16M DRAMs, 4M SRAMs as well as ASICs and microprocessors. The expanded facility will be able to produce 30,000 6-inch wafers per month using 0.55-micron CMOS technology.

The fab has been designed with the most sophisticated technology available, incorporating state-of-the-art environmental controls and efficiencies. A considerable amount of money has been invested for this purpose, as NEC regards environmental conservation as one of the most important international issues.

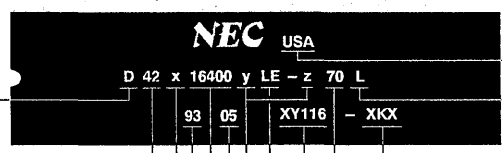
When running at full capacity, equipment in place will allow up to 60-percent of the water used for the DI process to be recycled—an important benefit for drought-ridden California. In addition, the new plant has eliminated the use of chlorofluorocarbons (CFC) in the manufacturing process. (The existing facility will eliminate all CFC usage by 1993.)

NECEL's manufacturing presence in Roseville is of significant benefit to the local community as well as the state of California. When running at full capacity, the plant will employ over 1,350 people, and nearly $5 million in tax revenue will be generated for the city, county and state.

As one of the biggest employers in the area, NECEL views itself as a partner with the local community and takes seriously its role as a good corporate citizen. Through numerous community relations activities, employees volunteer their time to support worthwhile educational and charitable causes. The company also has a generous policy for contributions and donations of equipment and money to help maintain a high quality of life for the area's residents.

In addition to the manufacturing facility in Roseville, NECEL has headquarter offices in Mountain View, California, in the heart of Silicon Valley. Sales offices are located throughout the United States so that customers have immediate access to qualified personnel. These national presences, combined with on-shore manufacturing capabilities, allow NEC Electronics to respond quickly to customer demand and to work closely with customers to meet their changing requirements. The company considers quality customer service to be a number one priority, a trademark of all NEC operations worldwide.

The NECEL facility in Roseville is an outstanding example of successful cultural meshing, offering the best of both worlds. The results are production yields and quality standards that are among the highest obtained by any NEC semiconductor manufacturing facility anywhere.



Country of Origin

Device Type
B = Digital bipolar
D = Digital MOS

Low-Power Indicator (Optional)
L = Low power
LL = Very low power

Date Code Year, Week

NEC Lot Code

TSOP Pinout Identifier
(Middle letter is significant)
J = Normal pinouts
K = Reverse pinouts

Product Class

10	10K ECL RAM
100	100K ECL RAM
23(H)C	CMOS ROM
27(H)C	CMOS EPROM
28C	CMOS EEPROM
28F	CMOS flash memory
41	NMOS dynamic RAM
42	CMOS dynamic RAM
43	CMOS static RAM
44	CMOS static RAM (6-T cell)
46	BiCMOS static RAM
48	CMOS application specific device

Speed Selection

–10	100 ns or 10 ns
–12	120 ns or 12 ns
–15	150 ns or 15 ns
–50	50 ns
–60	60 ns
–70	70 ns
–80	80 ns
–85	85 ns
–XX	Etc.

DRAM Option
S = Self-refresh and low-power devices

DRAM Power Supply

y	z	
–	–	5V ±10%
A	–	5V ±10% (with internal voltage regulator)
–	A	3.0 – 5.5V
–	B	2.7 – 5.5V
L	A	3.3V ±10%
L	B	3.0V ±10%

Device Identifier

Package

B or BH	Ceramic flatpack
C, CR or CZ	Plastic DIP (dual inline package)
D, DH, DX or DZ	Cerdip or ceramic DIP
G (≤ 40 pins), GU or GW	Plastic SOP (small-outline package)
G (> 40 pins) or GF	Plastic QFP (quad flatpack)
G5, GX or GZ	Plastic TSOP (thin small-outline package)
K	Ceramic LCC (leadless chip carrier)
L	PLCC (plastic leaded chip carrier)
LA, LB or LE	Plastic SOJ (small-outline J-lead package)
R	Ceramic PGA (pin grid array)
V	Plastic ZIP (zigzag inline package)

Notes:
(1) The marking location and format may vary among package types.
(2) Regardless of the format, the device number does not change.
(3) The "μP" in NEC part numbers does not appear on the package.

83SL-7321B

DRAMs

Size	Organ-ization	μPD	Features	Row Access Time (ns)	Package and Pins				Sect.
					SOJ	TSOP	ZIP	Other	
256K	256K x 1	41256	Page	80, 85, 100				16-DIP, 18-PLCC	3a
	64K x 4	41464	Page	80, 100, 120				16-DIP 18-PLCC	3b
1M	1M x 1	421000	FP	60, 70, 80, 100	26/20	24/20	20	18-DIP	4a
	256K x 4	424256	FP	60, 70, 80, 100	26/20	24/20	20	20-DIP	4b
4M	4M x 1	424100	FP	60, 70, 80, 100	26/20	26/20	20		5a
	4M x 1	424100A	FP	50, 60, 70, 80	26/20	26/20	20		
	4M x 1	424100L	FP; 3.3 V	70, 80	26/20	26/20	20		
	4M x 1	42S4100A	FP; SR	50, 60, 70, 80	26/20	26/20	20		
	4M x 1	42S4100L	FP; SR; 3.3 V	70, 80	26/20	26/20	20		
	4M x 1	424101	Nibble	60, 70, 80, 100	26/20	26/20	20		5b
	4M x 1	424102	SC	60, 70, 80, 100	26/20	26/20	20		5c
	1M x 4	424400	FP	60, 70, 80	26/20	26/20	20		5d
	1M x 4	424400A	FP	50, 60, 70, 80	26/20	26/20	20		
	1M x 4	424400L	FP; 3.3 V	70, 80	26/20	26/20	20		
	1M x 4	42S4400A	FP; SR	50, 60, 70, 80	26/20	26/20	20		
	1M x 4	42S4400L	FP; SR; 3.3 V	70, 80	26/20	26/20	20		
	1M x 4	424402	SC	60, 70, 80, 100	26/20	26/20	20		5e
	1M x 4	424410	FP; WPB	60, 70, 80, 100	26/20	26/20	20		5f
	1M x 4	424412	SC; WPB	60, 70, 80, 100	26/20	26/20	20		5g
	1M x 4	424440	FP; 4 $\overline{\text{CAS}}$	60, 70, 80	26/24				5h
	1M x 4	424440L	FP; 4 $\overline{\text{CAS}}$; 3.3 V	60, 70, 80	26/24				
	1M x 4	42S4440	FP; 4 $\overline{\text{CAS}}$; SR	60, 70, 80	26/24				
	1M x 4	42S4440L	FP; 4 $\overline{\text{CAS}}$; SR; 3.3 V	60, 70, 80	26/24				

FP Fast page
SR Self-refresh
SC Static column
WPB Write-per-bit

DRAMs (cont)

Size	Organ-ization	μPD	Features	Row Access Time (ns)	Package and Pins			Sect.
					SOJ	TSOP	ZIP	
4M (cont)	512K x 8	424800A	FP	60, 70, 80	28	28	28	6a
	512K x 8	424800L	FP; 3.3V	60, 70, 80	28	28	28	
	512K x 8	42S4800A	FP; SR	60, 70, 80	28	28	28	
	512K x 8	42S4800L	FP; SR; 3.3 V	60, 70, 80	28	28	28	
	512K x 8	424810A	FP; WPB	60, 70, 80	28	28	28	6b
	512K x 8	424810L	FP; WPB; 3.3 V	60, 70, 80	28	28	28	
	512K x 8	42S4810A	FP; WPB; SR	60, 70, 80	28	28	28	
	512K x 8	42S4810L	FP; WPB; SR; 3.3 V	60, 70, 80	28	28	28	
	512K x 9	424900A	FP	60, 70, 80	28	28	28	6c
	512K x 9	424900L	FP; 3.3 V	60, 70, 80	28	28	28	
	512K x 9	42S4900A	FP; SR	60, 70, 80	28	28	28	
	512K x 9	42S4900L	FP; SR; 3.3 V	60, 70, 80	28	28	28	
	256K x 16	424170A	FP; 2 $\overline{WE}$; 1K ref	60, 70, 80	40	44/40	40	7a
	256K x 16	424170L	FP; 2 $\overline{WE}$; 1K ref; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 16	42S4170A	FP; 2 $\overline{WE}$; 1K ref; SR	60, 70, 80	40	44/40	40	
	256K x 16	42S4170L	FP; 2 $\overline{WE}$; 1K ref; SR; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 18	424190A	FP; 2 $\overline{WE}$; 1K ref	60, 70, 80	40	44/40	40	7b
	256K x 18	424190L	FP; 2 $\overline{WE}$; 1K ref; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 18	42S4190A	FP; 2 $\overline{WE}$; 1K ref; SR	60, 70, 80	40	44/40	40	
	256K x 18	42S4190L	FP; 2 $\overline{WE}$; 1K ref; SR; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 16	424260A	FP; 2 $\overline{CAS}$; 512 ref	60, 70, 80	40	44/40	40	7c
	256K x 16	424260L	FP; 2 $\overline{CAS}$; 512 ref; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 16	42S4260A	FP; 2 $\overline{CAS}$; 512 ref; SR	60, 70, 80	40	44/40	40	
	256K x 16	42S4260L	FP; 2 $\overline{CAS}$; 512 ref; SR; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 16	424263A	FP; 2 $\overline{CAS}$; 512 ref; WPB	60, 70, 80	40	44/40	40	7d
	256K x 16	424263L	FP; 2 $\overline{CAS}$; 512 ref; WPB; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 16	42S4263A	FP; 2 $\overline{CAS}$; 512 ref; WPB; SR	60, 70, 80	40	44/40	40	
	256K x 16	42S4263L	FP; 2 $\overline{CAS}$; 512 ref; WPB; SR; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 18	424280A	FP; 2 $\overline{CAS}$; 512 ref	60, 70, 80	40	44/40	40	7e
	256K x 18	424280L	FP; 2 $\overline{CAS}$; 512 ref; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 18	42S4280A	FP; 2 $\overline{CAS}$; 512 ref; SR	60, 70, 80	40	44/40	40	
	256K x 18	42S4280L	FP; 2 $\overline{CAS}$; 512 ref; SR; 3.3 V	60, 70, 80	40	44/40	40	

FP Fast page
SR Self-refresh
WPB Write-per-bit
ref Refresh
$\overline{WE}$ Write enable

DRAMs (cont)

Size	Organ-ization	μPD	Features	Row Access Time (ns)	Packages and Pins			Sect.
					SOJ	TSOP	ZIP	
16M	16M x 1	4216100	FP; 4K ref	60, 70, 80, 100	28/24	28/24	24	8a
	16M x 1	4217100	FP; 2K ref	60, 70, 80, 100	28/24	28/24	24	
	16M x 1	4216101	Nibble; 4K ref	60, 70, 80, 100	28/24	28/24	24	8b
	16M x 1	4217101	Nibble; 2K ref	60, 70, 80, 100	28/24	28/24	24	
	16M x 1	4216102	SC; 4K ref	60, 70, 80, 100	28/24	28/24	24	8c
	16M x 1	4217102	SC; 2K ref	60, 70, 80, 100	28/24	28/24	24	
	4M x 4	4216400	FP; 4K ref	60, 70, 80, 100	28/24	28/24	24	8d
	4M x 4	4217400	FP; 2K ref	60, 70, 80, 100	28/24	28/24	24	
	4M x 4	4216402	SC; 4K ref	60, 70, 80, 100	28/24	28/24	24	8e
	4M x 4	4217402	SC; 2K ref	60, 70, 80, 100	28/24	28/24	24	
	4M x 4	4216410	FP; 4K ref; WPB	60, 70, 80, 100	28/24	28/24	24	8f
	4M x 4	4217410	FP; 2K ref; WPB	60, 70, 80, 100	28/24	28/24	24	
	4M x 4	4216412	SC; 4K ref; WPB	60, 70, 80, 100	28/24	28/24	24	8g
	4M x 4	4217412	SC; 2K ref; WPB	60, 70, 80, 100	28/24	28/24	24	
	2M x 8	4216800	FP; 4K ref	50, 60, 70, 80	28	28		8h
	2M x 8	4216800L	FP; 4K ref; 3.3 V	60, 70, 80	28	28		
	2M x 8	42S16800	FP; 4K ref; SR	50, 60, 70, 80	28	28		
	2M x 8	42S16800L	FP; 4K ref; SR; 3.3 V	60, 70, 80	28	28		
	2M x 8	4217800	FP; 2K ref	50, 60, 70, 80	28	28		
	2M x 8	4217800L	FP; 2K ref; 3.3 V	60, 70, 80	28	28		
	2M x 8	42S17800	FP; 2K ref; SR	50, 60, 70, 80	28	28		
	2M x 8	42S17800L	FP; 2K ref; SR; 3.3 V	60, 70, 80	28	28		
	2M x 8	4216802	SC; 4K ref	50, 60, 70, 80	28	28		8i

FP Fast page
SR Self-refresh
SC Static column
WPB Write-per-bit
ref Refresh

DRAMs (cont)

Size	Organ-ization	μPD	Features	Row Access Time (ns)	Packages and Pins			Sect.
					SOJ	TSOP	ZIP	
16M (cont)	2M x 9	4216900	FP; 4K ref	50, 60, 70, 80	32	32		8j
	2M x 9	4216900L	FP; 4K ref; 3.3 V	60, 70, 80	32	32		
	2M x 9	42S16900	FP; 4K ref; SR	50, 60, 70, 80	32	32		
	2M x 9	42S16900L	FP; 4K ref; SR; 3.3 V	60, 70, 80	32	32		
	2M x 9	4217900	FP; 2K ref	50, 60, 70, 80	32	32		
	2M x 9	4217900L	FP; 2K ref; 3.3 V	60, 70, 80	32	32		
	2M x 9	42S17900	FP; 2K ref; SR	50, 60, 70, 80	32	32		
	2M x 9	42S17900L	FP; 2K ref; SR; 3.3 V	60, 70, 80	32	32		
	2M x 9	4216902	SC; 4K ref	50, 60, 70, 80	32	32		8k
	1M x 16	4216160	FP; 4K ref	50, 60, 70, 80	42	50/44		8l
	1M x 16	4216160L	FP; 4K ref; 3.3 V	60, 70, 80	42	50/44		
	1M x 16	42S16160	FP; 4K ref; SR	50, 60, 70, 80	42	50/44		
	1M x 16	42S16160L	FP; 4K ref; SR; 3.3 V	60, 70, 80	42	50/44		
	1M x 16	4217160	FP; 2K ref	50, 60, 70, 80	42	50/44		
	1M x 16	4217160L	FP; 2K ref; 3.3 V	60, 70, 80	42	50/44		
	1M x 16	42S17160	FP; 2K ref; SR	50, 60, 70, 80	42	50/44		
	1M x 16	42S17160L	FP; 2K ref; SR; 3.3 V	60, 70, 80	42	50/44		
	1M x 16	4218160	FP; 1K ref	50, 60, 70, 80	42	50/44		
	1M x 16	4218160L	FP; 1K ref; 3.3 V	60, 70, 80	42	50/44		
	1M x 16	42S18160	FP; 1K ref; SR	50, 60, 70, 80	42	50/44		
	1M x 16	42S18160L	FP; 1K ref; SR; 3.3 V	60, 70, 80	42	50/44		
	1M x 18	4216180	FP; 4K ref	50, 60, 70, 80	42	50/44		8m
	1M x 18	4216180L	FP; 4K ref; 3.3 V	60, 70, 80	42	50/44		
	1M x 18	42S16180	FP; 4K ref; SR	50, 60, 70, 80	42	50/44		
	1M x 18	42S16180L	FP; 4K ref; SR; 3.3 V	60, 70, 80	42	50/44		
	1M x 18	4217180	FP; 2K ref	50, 60, 70, 80	42	50/44		
	1M x 18	4217180L	FP; 2K ref; 3.3 V	60, 70, 80	42	50/44		
	1M x 18	42S17180	FP; 2K ref; SR	50, 60, 70, 80	42	50/44		
	1M x 18	42S17180L	FP; 2K ref; SR; 3.3.V	60, 70, 80	42	50/44		
	1M x 18	4218180	FP; 1K ref	50, 60, 70, 80	42	50/44		
	1M x 18	4218180L	FP; 1K ref; 3.3 V	60, 70, 80	42	50/44		
	1M x 18	42S18180	FP; 1K ref; SR	50, 60, 70, 80	42	50/44		
	1M x 18	42S18180L	FP; 1K ref; SR: 3.3 V	60, 70, 80	42	50/44		

FP Fast page
SC Static column
ref Refresh

DRAM SIMM Modules

Organization	Pins	MC	Operation	Access Time (ns)	Module Size (inch)		DRAM Devices		Sect.
					Thickness	Height	Qty	μPD	
256K x 8	30	-42256AB8	Fast page	60, 70, 80, 100	.200	.661	2	424256LA	9a
256K x 9	30	-42256AB9	Fast page	60, 70, 80, 100	.200	.661	2 1	424256LA 42256L	9b
256K x 32	72	-42256A32	Fast page	70, 80, 100	.200	1.000	2	424260LE	9c
256K x 36	72	-42256A36	Fast page	70, 80, 100	.200	1.000	2	424280LE	9d
256K x 40	72	-42256AA40	Fast page	60, 70, 80, 100	.200	1.000	10	424256LA	9e
512K x 32	72	-42512A32	Fast page	70, 80, 100	.354	1.000	4	424260LE	9f
512K x 36	72	-42512A36	Fast page	70, 80, 100	.366	1.000	4	424280LE	9g
512K x 40	72	-42512AA40	Fast page	60, 70, 80, 100	.366	1.000	20	424256LA	9h
		-42512AB40	Fast page	70, 80, 100	.200	1.000	5	424800LE	
1M x 8	30	-421000A8	Fast page	60, 70, 80, 100	.200	.661	2	424400LA	10a
1M x 9	30	-421000A9	Fast page	60, 70, 80, 100	.200	.661	2 1	424400LA 421000LA	10b
1M x 32	72	-421000A32	Fast page	60, 70, 80, 100	.200	1.000	8	424400LA	10c
					.106	1.000	8	424400GS	
					.200	1.250	8	424400LA	
1M x 36	72	-421000A36	Fast page	60, 70, 80, 100	.200	1.000	8 4	424400LA 421000GX	10d
					.106	1.000	8 4	424400GS 421000GX	
					.208	1.250	8 4	424400LA 421000LA	
			Fast page	60, 70, 80	.366	1,000	8 4	424400LA 421000LA	
1M x 40	72	-421000AA40	Fast page	60, 70, 80, 100	.200	1.000	10	424400LA	10e
		-421000AB40	Fast page	60, 70, 80, 100	.354	.799	10	424800LE	
2M x 32	72	-422000A32	Fast page	60, 70, 80, 100	.354	1.000	16	424400LA	10f
					.161	1.000	16	424400GS	
					.354	1.250	16	424400LA	

DRAM SIMM Modules (cont)

Organization	Pins	MC	Operation	Access Time (ns)	Module Size (inch)		DRAM Devices		Sect.
					Thickness	Height	Qty	μPD	
2M x 36	72	-422000A36	Fast page	60, 70, 80	.366	1.000	16 8	424400LA 421000GX	10g
					.161	1.000	16 8	424400GS 421000GX	
					.366	1.250	16 8	424400LA 421000LA	
2M x 40	72	-422000AA40	Fast page	70, 80	.354	1.000	20	424400LA	10h
4M x 8	30	-424000A8	Fast page	60, 70, 80, 100	.208	.799	8	424100LA	11a
4M x 9	30	-424000A9	Fast page	60, 70, 80, 100	.200	.799	9	424100LA	11b
4M x 32	72	-424000A32	Fast page	60, 70, 80	.200	1.250	8	4217400LE	11c
					.366	1.000	8	4217400LE	
4M x 36	72	-424000A36	Fast page	60, 70, 80	.200	1.250	8 4	4217400LE 424100LA	11d
					.366	1.000	8 4	4217400LE 424100LA	
8M x 32	72	-428000A32	Fast page	60, 70, 80	.366	1.250	16	4217400LE	11e
8M x 36	72	-428000A36	Fast page	60, 70, 80	.366	1.250	16 8	4217400LE 424100LA	11f

Video RAMs

Size	Organ-ization	μPD	Row Access Time (ns)	Serial Access Time (ns)	Mode	Packages and Pins				Sect.
						DIP	SOJ	TSOP	ZIP	
256K	64K x 4	41264	120, 150	40, 60		24			24	12a
	64K x 4	42264	100	25		24	24		24	12b
1M	256K x 4	42273	100, 120	30, 40	FP		28		28	12c
	256K x 4	42274	100, 120	30, 40	FP		28		28	12d
	256K x 4	42274-80	80	25	FP		28		28	12e
	128K x 8	42275	80, 100, 120	25, 40	FP		40			12f
2M	256K x 8	482234	70, 80	17, 20	FP		40	44	40	12g
		482235	70, 80	17, 20	HP					

FP Fast page
HP Hyper page (extended data out)

Synchronous DRAM

Size	Organ-ization	μPD	Clock Rate (MHz)	Row Access Time (ns)	Burst Access Time (ns)	Packages and Pins				Sect.
						DIP	SOJ	TSOP	ZIP	
16M	4M x 4	42116420	66 100	70 50	15 10			44		13a
	2M x 8	42116820						44		
	2M x 9	42116920						44		
	1M x 16	42116162						50		
	1M x 18	42116182						50		

RAMBUS DRAM

Size	Organ-ization	μPD	Read Hit Access Time (ns)	Burst Access Time (ns)	Packages and Pins				Sect.
					DIP	SOJ	TSOP	SVP	
16M	2M x 8	488130	40	2				32	14a
	2M x 9	488170	40	2				32	

Application Specific Devices

Description	μPD	Access Time (ns)	Packages and Pins					Sect.
			DIP	SOJ	TSOP	ZIP	Other	
910 x 8-bit line buffer for NTSC TV	42101	27, 49	24				24-SOP	18a
1134 x 8-bit line buffer for PAL TV	42102	18, 21, 40	24				24-SOP	18b
263 lines of 910 x 4 bits NTSC field buffer	42270	40	28					18c
Picture-in-picture generator	42271 42272	6 MHz input sampling					64-QFP	18d
256K x 8-bit field buffer	42280	25, 30, 40				28	28-SOP	18e
5048 x 8-bit line buffer for communications	42505	40, 55	24			28		18f
5048 x 8-bit line buffer	485505	18, 25				24	24-SOP	18g
5048 x 16 line buffer	485506	18, 25			44			18h
32K x 8 bidirectional data buffer	42532	50	40					18i
1M x 1 silicon file	42601	600		26/20		20		18j
4M x 1 silicon file	42641	80		26/20	26/20			18k
1M x 4 silicon file	42644	80		26/20	26/20			18l
256K x 16 graphics DRAM	481440	70, 80		40				18m

Fast Static RAMs

Size	Organ-ization	μPD	Access Time (ns)	Packages and Pins						Sect
				DIP	SOJ	SOP	TSOP	ZIP	Other	
64K	64K x 1	4361B	12, 15, 20	22	24					19a
	16K x 4	4362B	12, 15, 20	22	24					19b
	16K x 4	4363B	12, 15, 20	24	24					19c
	8K x 8	4368	15, 20	28	28					19d
	8K x 9	4369	15, 20	28	28					19e
256K	256K x 1	43251B	15, 20, 25	24	24					20a
	64K x 4	43253B	15, 20, 25	28	28					20b
	64K x 4	43254B	15, 20, 25	24	24					20c
	32K x 8	43258A	15, 20, 25	28	28					20d
	32K x 9	43259A	15, 20, 25	32	32					20e
1M	1M x 1	431001	20, 25, 35		28					21a
	256K x 4	431004	20, 25, 35		28					21b
	128K x 8	431008	15, 17, 20		32					21c
	128K x 9	431009	15, 17, 20		36					21d
	64K x 16	431016	15, 17, 20		44		44			21e
	64K x 18	431018	15, 17, 20		44		44			21f
4M	4M x 1	434001	20, 25		32					22a
	1M x 4	434004	20, 25		32					22b
	512K x 8	434008	20, 25		36					22c

Cache Data RAMs

Size	Organization	μPD	Access Time (ns)	Packages and Pins					Sect.
				DIP	SOJ	SOP	TSOP	PLCC	
256K	16K x 10 bit x 2	46710A	12, 15					52	23a
	8K x 20 bit x 2	46741A	12, 15					68	23b

Standard Static RAMs

Size	Organization	μPD	Access Time (ns)	Packages and Pins					Sect.
				DIP	SOJ	SOP	TSOP	ZIP	
256K	32K x 8	43256A	85, 100, 120, 150	28		28	32		24a
	32K x 8	43256B	55, 70, 85	28		28			24b
1M	128K x 8	431000A	70, 85, 100	32		32	32		24c
4M	512K x 8	434000	55, 70, 85, 100	32		32	32		24d
	512K x 8	MC-434000	85, 100	32					24e

ECL RAMs (10K Interface)

Size	Organization	μPB	Access Time (ns)	Packages and Pins			Sect.
				DIP	LCC	Flatpack	
1K	256 x 4	10422	7, 10	24			25a
4K	4K x 1	10470	10, 15	18			25b
	1K x 4	10474	8, 10, 15	24			25c
	1K x 4	10474A	5, 6	24			25d
	1K x 4	10474E	3, 4	24		24	25e
	1K x 4	10476LL	6	28		28	25f
16K	16K x 1	10480	10, 15	20		20	25g
	4K x 4	10484	10, 15	28		28	25h
	4K x 4	10484A	5, 7	28		28	25i
	4K x 4	10A484	5, 7	28		28	25j
256K	256K x 1	μPD10500	15, 20	24			25k

ECL RAMs (100K Interface)

Size	Organization	μPB	Access Time (ns)	Packages and Pins			Sect.
				DIP	LCC	Flatpack	
1K	256 x 4	100422	7, 10	24		24	26a
4K	4K x 1	100470	10, 15	18			26b
	1K x 4	100474	4.5, 6, 8, 10, 15	24	24	24	26c
	1K x 4	100474A	5, 6	24		24	26d
	1K x 4	100474E	3, 4	24		24	26e
	1K x 4	100476LL	6	28		28	26f
16K	16K x 1	100480	10, 15	20		20	26g
	4K x 4	100484	10, 15	28		28	26h
	4K x 4	100484A	5, 7	28		28	26i
	4K x 4	100A484	5, 7	28		28	26j
256K	256K x 1	μPD100500	15, 20	24			26k

EEPROMs

Size	Organization	μPD	Access Time (ns)	Packages and Pins						Sect.
				DIP	SOJ	SOP	TSOP	ZIP	Other	
4K	512 x 8	28C04	200, 250	24		24				27a
	512 x 8	28C05	200, 250	24		24				27b
64K	8K x 8	28C64	200, 250	28						27c
256K	32K x 8	28C256	200, 250	28						27d

NEC

Section 2
Reliability and Quality Control

As large-scale integration (LSI) reaches a higher level of density, the reliability of individual devices imposes a more profound impact on system reliability. As a result, great emphasis has been placed on assuring device reliability.

Conventionally, performing reliability tests and using feedback from the field have been the only methods of monitoring and measuring reliability. As LSI density increases, however, it has become more difficult to activate internal circuit elements in a device from external terminals and to detect their degradation. Testing and feedback alone cannot provide enough information to ensure today's demanding reliability requirements.

To guarantee and improve high levels of reliability for large-scale integrated circuits, a new philosophy and methodology are needed for reliability assurance. Quality and reliability must not only be monitored and measured but, most importantly, must be built into the product.

BUILT-IN TQC

NEC has introduced the concept of total quality control (TQC) across its entire semiconductor product line to implement this philosophy. Rather than performing only a few simple quality inspections, quality control has become an integral part of each process step involving production, engineering, quality control staffs, and all management personnel. Figure 1 is a flowchart that shows how these activities form a comprehensive quality control system at NEC.

In addition to TQC, NEC has introduced a prescreening method into the production line that eliminates potentially defective units. This combination of building in quality and screening out projected early failures has resulted in superior quality and reliability.

Most large-scale integrated circuits use high-density MOS technology with state-of-the-art high performance due to improved fine-line generation techniques. When physical parameters are reduced, circuit-density and performance increase while active circuit power dissipation decreases. The information presented here will show that this advanced technology combined with the practice of TQC yields products as reliable as those from previous technologies.

APPROACHES TO TQC

TQC activities are geared toward total customer satisfaction. The success of these activities depends on management's commitment to enhancing employee development, maintaining a customer-first attitude, and fulfilling community responsibilities.

TQC is implemented in the following steps. First, quality control is embedded into each process, allowing early detection of possible failure mechanisms and immediate feedback. Second, the reliability and quality assurance policy is upheld through company-wide quality control activities. Third, emphasis is placed on research and development efforts to achieve even higher standards of device quality and reliability. Fourth, extensive failure analysis is performed periodically, and appropriate corrective actions are taken as preventative measures.

Process control limits are based on statistical data gathered from this analysis and used to determine the effectiveness of the in-process quality control steps.

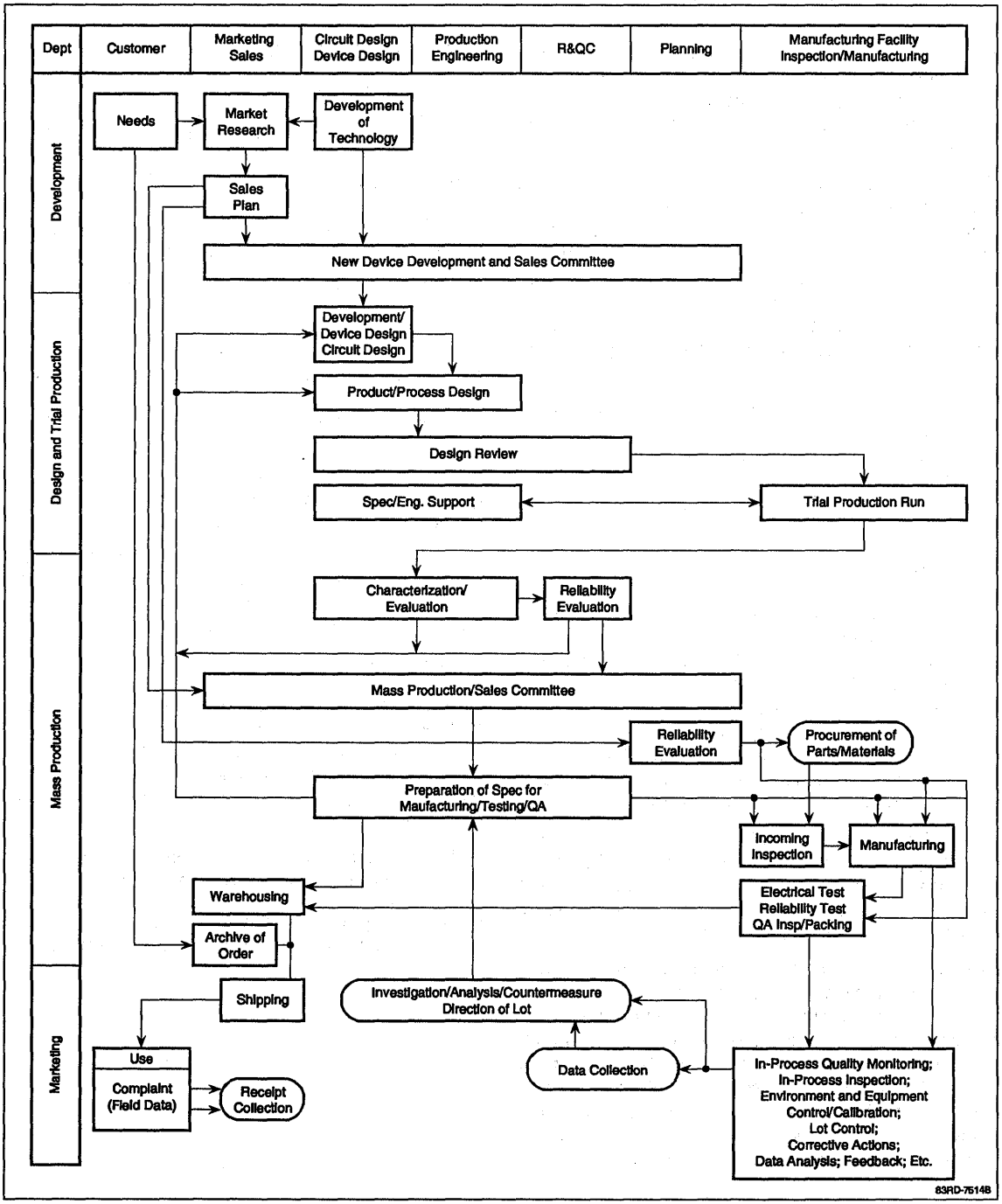
New standards are continuously upgraded, and the iterative process continues. The goal is to maintain the superior product quality and reliability that has become synonymous with the NEC name.

Zero Defects Program

One of the quality control activities that involves every staff level is the Zero Defects (ZD) Program. The purpose of the ZD Program is to minimize, if not prevent, defects due to controllable causes. These activities are organized by groups of workers around these four premises.

- A group must have a target or purpose to pursue.
- Several groups can be organized to pursue a common target.
- Each group must have a responsible leader.
- Each group is well supported by management.

Figure 1. NEC's Quality Control System



The group's target is selected from items relating to specifications, inspections, operation standards, etc. When past data is available, a Pareto diagram is created and reviewed to select an item most in need of quality improvement. Target defects related to this item are clearly defined. Records are analyzed to compute numerical equivalents of the defects. Then, action is taken to control these defects.

Statistical Approach

Another approach to quality control is statistical analysis. NEC uses statistical analysis at each stage of LSI product development, trial runs, and mass production. Some implementations of this statistical approach are:

- Process comparisons
- Control charts
- Data analysis
  — Correlation, regression, multivariance, etc.
- Cp/Cpk studies
  — Variables and attributes data (performed monthly)

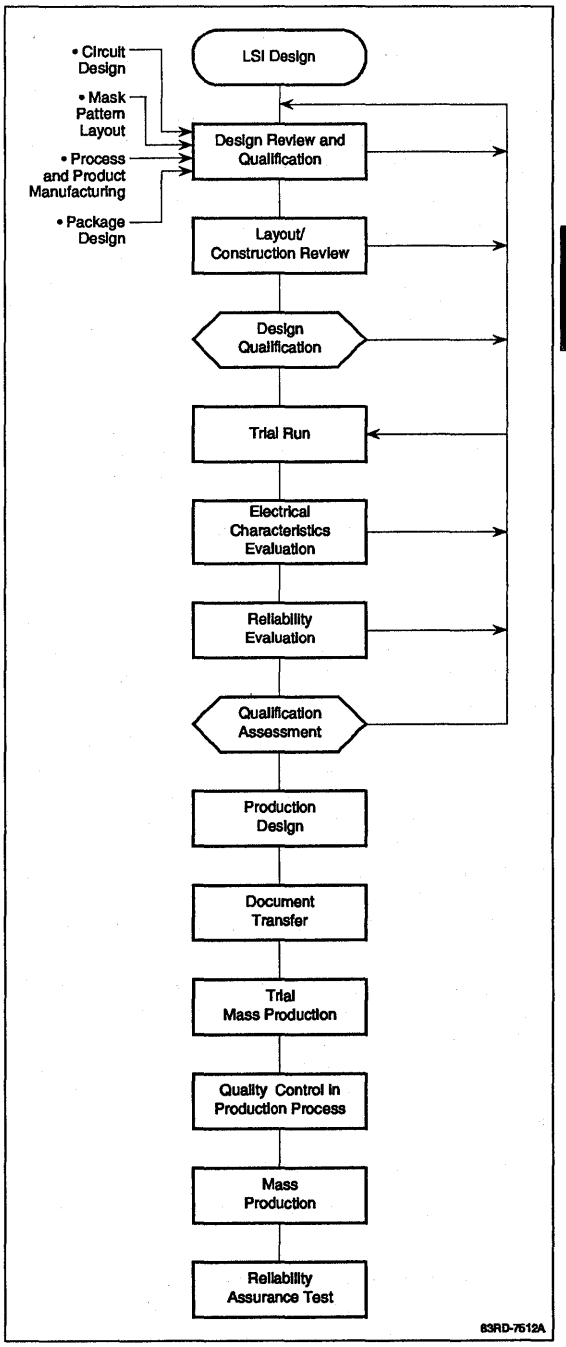
Process control sheets and other QC tools are used to monitor important parameters such as Cp, Cpk, X, X-R, electrical parameters, pattern dimensions, bond strength, test percentage defects, etc. The results of these studies are monitored by the production staff, QC engineers, and other associated engineers. If any out-of-control or out-of-specification limit is observed, corrective procedures are quickly taken.

IMPLEMENTATION OF QUALITY CONTROL

Building quality into a product requires early detection of possible failure mechanisms and immediate feedback to remove such problems. A fixed quality inspection station often cannot provide prompt and accurate feedback about the process steps prior to the inspection. Quality control functions have therefore been distributed into each process step including the conceptual stage. The most significant areas where quality control has been placed include:

- Product development
- Incoming material inspection
- Wafer processing
- Chip mounting and packaging
- Electrical testing and infant mortality screening
- Outgoing material inspection
- Reliability assurance tests
- Process/product changes

Figure 2. New Product Development



2

Product Development

New product development includes the product concept, device proposal review, physical element design and organization, engineering evaluation, and, finally, product transfer to manufacturing. Quality and reliability are considered at every step. The new product development flow at NEC is shown in figure 2.

Design is the first and most important step in new product development. NEC believes that the foundation of device quality is determined at the design stage. The four steps involved are circuit design, mask pattern layout, package design, and the setting of process and product manufacturing conditions. Design standards have been established at NEC to maximize quality and reliability.

After completion of the design, a design review is performed to check for conformity to design standards and to consider other factors influencing reliability and quality. At this stage, modification or re-design may be necessary. NEC believes that design reviews are essential for product modifications as well as newly designed products.

Once a design successfully passes its review, a trial run takes place in which the product's electrical and mechanical characteristics, quality, and reliability are evaluated.

Additional runs are performed in which process conditions are varied deliberately, causing characteristic factors to change in mass production. These samples are evaluated to determine the best combination of process conditions. Reliability tests are then conducted to check the new product's electrical and mechanical stress resistance. If no problems are found at this stage, the product is approved for mass production.

Mass production begins after the product design department prepares a schedule that includes reliability and quality control steps. The standards for production and control steps are continuously re-examined for possible improvement, even after mass production has started.

Incoming Material Inspection

NEC has the following programs to control incoming materials:

- Vendor/material qualification system
- Purchasing specifications for materials
- Incoming materials inspection
- Inspection data feedback
- Meetings with vendors concerning quality
- Vendor audits

If any parts or materials are rejected at incoming inspection, they are returned to the vendor with a rejection notification form specifying the failure items and modes. The results of these inspections are used to rate the vendors for future purchasing.

In-Process Quality Inspection

Typical in-process quality inspections performed at wafer fabrication, chip mounting and packaging, and device testing stages are listed in appendix 1A and appendix 1B.

Electrical Testing and Screening

At the first electrical test, dc parameters are tested according to electrical specifications on 100% of each lot. This is a prescreening prior to any infant mortality test. At the second electrical test, ac functional tests as well as dc parameter tests are performed on 100% of each lot. If the percentage of defective units in a lot is unacceptably high in this test, the lot is subjected to an infant mortality rescreen. During this time, any defective units undergo extensive failure analysis. The results of these analyses are fed back into the process through corrective actions.

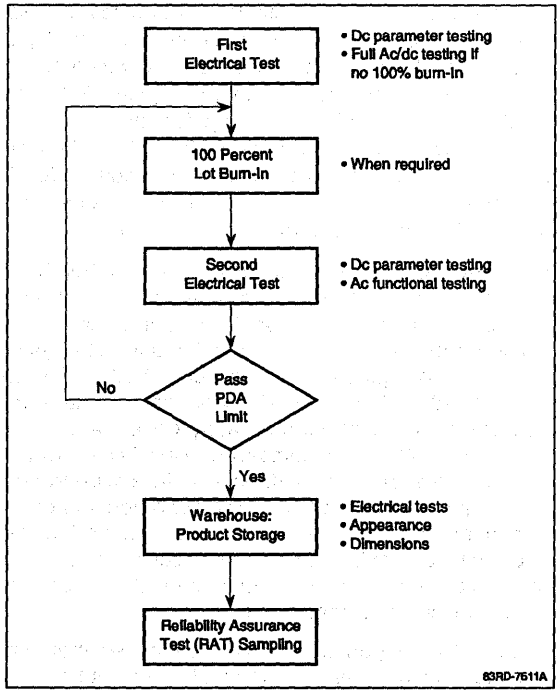
Figure 3 is a flowchart of the typical infant mortality screening and electrical testing.

Outgoing Inspection

Prior to warehouse storage or shipment, lots are subjected to an outgoing inspection according to the following sampling plan:

- Electrical
  - — Dc parameters, lot tolerance parts defective (LTPD) 3%
  - — Ac functional LTPD 3%
- Appearance
  - — Major LTPD 3%
  - — Minor LTPD 7%

Figure 3. Electrical Testing and Screening



Reliability Assurance Tests

Prior to shipment, representative samples from each process family are taken on a regular basis and subjected to monitoring reliability tests. This testing is performed to confirm that NEC's products continually meet their field reliability targets.

Process/Product Changes

As mentioned previously, a design review occurs for product changes as well as for new products. Once a design is approved and processes are altered for maximum quality, qualification testing is performed to check reliability. If the test results are acceptable, the product is internally qualified for mass production.

The typical reliability qualification tests performed at NEC are listed in appendix 3.

RELIABILITY THEORY

Reliability is defined as a characteristic of an item expressed by the probability that it will perform a required function, under specific conditions, for a certain period of time. The concept of probability, the definition of required function, and the knowledge of how time affects the item of concern are therefore necessary tools for the study of reliability.

Definition of a required function, by implication, treats the definition of a failure. Failure of a device is defined as the termination of a device's ability to perform its required function. A device has failed if it is unable to meet guaranteed values given in its electrical specifications.

Failures are categorized by the period of time in which they occur. The critical times used in the discussion of device reliability and failure are the periods of early, random, and wearout failures. Probability is used to quantitatively estimate reliability levels during these periods as well as overall reliability. The relevant theories and methods of calculation will be discussed later.

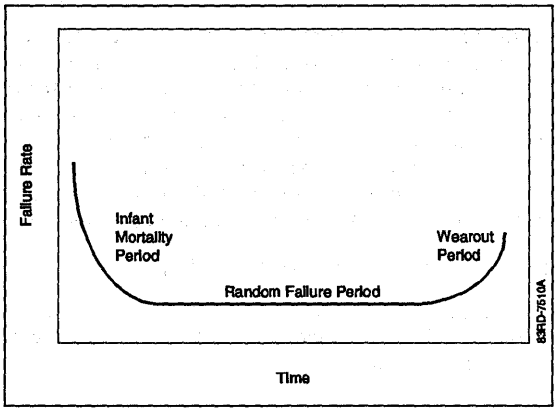
Regarding individual devices, specific failure mechanisms seen in life tests and in infant mortality screening tests are the parameters of concern in the determination of overall device failure rates, thus reliability levels.

Regarding systems, the sum of individual device failure rates is the expected failure rate of the system hardware.

Life Distribution

The fundamental principles of reliability engineering predict that the failure rate of a group of devices will follow the well-known bathtub curve in figure 4.

Figure 4. Reliability Life (Bathtub) Curve



The curve is divided into three regions: infant mortality, random failures, and wearout failures.

The infant mortality section of the curve, where the failure rate is declining rapidly, represents the early-life device failures. These failures are usually associated with one or more manufacturing defects.

After a period of time, the failure rate reaches a low value. This random failure area of the curve represents the useful portion of a device's life. During this random failure period, a slight decline is observed due to the depletion of potential random failures from the general population.

Wearout failures occur at the end of useful device life. These failures are observed in the rapidly rising failure rate portion of the curve; devices are wearing out both physically and electrically.

Therefore, for a device that has a very long life expectancy compared to the system that contains it, the areas of concern will be the infant mortality and random failure portions of the bathtub curve.

Failure Distribution at NEC

To eliminate infant mortality failures, NEC subjects its products to production burn-in whenever necessary. This burn-in is performed at an elevated temperature on 100% of the devices involved and is designed to remove potentially defective units.

After elimination of early device failures, a system will be left to the random failures of its components. To make proper projections of the failure rate of a system in the operating environment, random failure rates must be predicted for the system's components.

To qualitatively study random failures, integrated circuits returned from the field, as well as in-house life testing failures, undergo extensive failure analyses at respective NEC manufacturing divisions. Failure mechanisms are identified and resulting data is fed back to appropriate production and engineering groups. Long-term failure rates are determined from this data to quantitatively study this random failure population.

Infant Mortality Failure Screening

Establishing infant mortality screening requires knowledge of likely failure mechanisms and their associated activation energies.

Typical problems associated with infant mortality failures are manufacturing defects and process anomalies, which consist of contamination, cracked chips, wire bond shorts, or bad wire bonds. Since these problems can result from a number of possible failure mechanisms, the activation energy for infant mortality can vary considerably. Correspondingly, the effectiveness of an infant mortality screening condition (preferably at some stress level to shorten the screening time) varies greatly with the failure mechanism.

For example, failures due to ionic contamination have an activation energy of approximately 1.0 eV. Therefore, a 15-hour stress at 125°C junction temperature would be the equivalent of approximately 314 days of operation at a junction temperature of 55°C. On the other hand, failures due to oxide defects have an activation energy of approximately 0.3 eV. A 15-hour stress at 125°C junction temperature in this case would be the equivalent of approximately 4 days of operation at 55°C junction temperature. The condition and duration of infant mortality screening is determined by the economic factors involved in the screening and by the allowable rate of component failure. A component failure causes a system failure.

Empirical data gathered at NEC indicates that any early failures generally occur after less than 4 hours of stress at 125°C ambient temperature. This fact is supported by the bathtub curve created from actual life test results. The failure rate after 4 hours of such stress testing shows random distribution as opposed to the rapidly decreasing failure rate observed in the early life portion of the curve.

Whenever necessary, NEC has adopted this infant mortality burn-in at 125°C as a standard production screening procedure. NEC believes it is imperative that failure modes associated with such infant mortality screens be understood and fixed at the manufacturing level. Failure analysis is performed on all infant mortality failures for this purpose. This in-line data coupled with data accumulated from the field is used to introduce corrective actions and quality improvement measures. If the early-life failures of a device can be minimized or eliminated and countermeasures appropriately monitored, then such screens can be eliminated. The result of such practices is that field reliability of NEC devices is an order of magnitude higher than NEC's long-term failure rate goals.

Table 1. Typical Reliability Test Results

Name	Type	HTB	T/H	PCT	T/C
Micro (Note 1)	NMOS	9/23817 (15 FIT)	3/13625	0/5034	0/1817
	CMOS	7/20361 (6.6 FIT)	6/15155	8/16727	0/5913
Memory (HTOL)	DRAM (Note 2)	9/13072 (8.2 FIT)	2/12796	4/8477	3/3085
	1 Meg DRAM (Note 3)	24/13459 (68 FIT)	0/5414	0/2920	0/2100
	4 Meg DRAM (Note 4)	4/2150 (4.2 FIT)	0/550	0/550	0/760
	SRAM (Note 5)	0/3966 (6.6 FIT)	0/275	0/316	0/305
	1 Meg SRAM (Note 5)	0/458 (5.8 FIT)	1/3026	0/3838	0/1350
ASIC (Note 6)	CMOS	7/6146 (43 FIT)	2/2848	4/9159	6/5738
	ECL	0/1368 (8 FIT)	—	—	0/246
	BiCMOS	3/2801 (29 FIT)	0/3505	0/4370	0/5555

Note:

Information in the table above has been extracted from NEC report numbers:

(1) IRQ-3Q-22833
(2) TRQ-89-01-0021
(3) TRQ-89-01-0021
(4) IRQ-2Q-70117
(5) TRQ-90-11-0085
(6) TRQ-91-02-0093

Accelerated Reliability Testing

NEC performs extensive reliability testing at both pre-production and post-production levels to ensure that all products meet NEC's minimum expectations and those of the field.

Assume an electronic system contains 1000 integrated circuits and that 1% system failures per month can be tolerated by this system. The allowable failure rate per component is then calculated as follows:

$$\frac{1\%\text{ failures}}{720\text{ hours} \times 1000\text{ pieces}} = (0.0014)\frac{\%\text{ failures}}{1000\text{ hours}}$$

$$= 14\text{ FITs}$$

The rate of 14 FITs corresponds to one failure in 85 devices during an operating test of approximately 10,000 hours. To demonstrate this reliability level in a reasonable amount of time, a test condition is apparently required to accelerate the time-to-failure in a predictable and understandable way.

The most common method for decreasing time-to-failure is the use of high temperature to accelerate physiochemical reactions that can lead to device failure. Other stressful environmental conditions are voltage, current, humidity, vibration, or some combination of these. Appendix 2 lists typical accelerated reliability assurance tests performed at NEC on molded integrated circuits. Table 1 shows the results of some of these tests for various process types.

Reliability Assurance Tests

NEC's life tests consist of the high-temperature operating/bias life (HTOL/HTB), the high-humidity storage life (HHSL), the high-temperature, high-humidity (T/H = HHSL + bias), and the high-temperature storage life (HTSL). Additionally, NEC performs various environmental and mechanical tests.

HTOL/HTB Test. These tests are used to accelerate failure mechanisms by operating devices in a dynamic (operating life) or static (bias) condition at an elevated temperature of 125°C. The data obtained is translated to a lower temperature to estimate device life expectancy using the Arrhenius relationship explained later.

HHSL and T/H Tests. Integrated circuits are extremely sensitive to the effects of humidity such as electrolytic corrosion between biased lines. The high-temperature and high-humidity tests are performed to detect failure mechanisms accelerated by temperature and humidity, such as leakage related problems and drifts in device parameters due to process instability.

HTSL Test. Another common test is the high-temperature storage life test in which devices are subjected to elevated temperatures with no applied bias. This test is used to detect process instability and stress migration problems.

Environmental Tests. Other environmental tests such as the pressure cooker test (PCT) or the temperature cycling test (T/C) detect problems related to the package and/or interactions between materials as well as the degradation of environmentally sensitive device characteristics.

Failure Rate Calculation/Prediction

To predict the device failure rate from accelerated life test data, the activation energies of the failure mechanisms involved should be considered. In some cases, an average activation energy is assumed to accomplish a quick first-order approximation. NEC assumes an average activation energy of 0.7 eV for most products (0.3 eV for high-density memory devices). This average value has been assessed from extensive reliability test results and yields a conservative failure rate.

Since most semiconductor failures are temperature dependent, the Arrhenius relationship is used to normalize failure rate predictions at a system operation temperature of 55°C. It assumes that temperature dependence is an exponential function that defines the probability of failure occurrence, and that degradation of a performance parameter is linear with time. The Arrhenius model includes the effects of temperature and activation energies of the failure mechanisms in the following Arrhenius equation:

$$A = \exp \frac{-E_A(T_{J1}-T_{J2})}{k(T_{J1})(T_{J2})}$$

Where:
A(T) = Acceleration factor
E_A = Activation energy
T_{J1} = Junction temperature (in K) at T_{A1} = 55°C
T_{J2} = Junction temperature (in K) at T_{A2} = 125°C
k = Boltzmann's constant = 8.62×10^{-5} eV/K

Because the thermal resistance and power dissipation of a particular device type cannot be ignored, junction temperatures (T_{J1} and T_{J2}) are used instead of ambient temperatures (T_{A1} and T_{A2}). We calculate junction temperatures using the following formula:
$T_J = T_A +$ (thermal resistance)(power diss. at T_A)

With this information, a temperature acceleration factor can be calculated.

In some cases, the effect of voltage acceleration on failure rate must also be considered. Voltage acceleration can be characterized by the following equation:
$A(V) = \exp [-\beta(Vd - Vs)]$

Where:
Vd = Operating voltage (5.5 V)
Vs = Life test stress voltage (7 V)
β = Empirically determined constant (dependent on electric field constant and oxide thickness)

The constant β has been given the value ≈ 1, which is a conservative figure. Therefore, the overall acceleration factor will be determined as the product:
$A(T,V) = A(T) * A(V)$

To estimate long-term failure rate, the acceleration factor must be multiplied by the actual time to determine the simulated test time. From the high-temperature operating or bias life test results, failure rates can then be predicted at a 60% confidence level using the following equation:

$$L = \frac{(X^2)10^5}{2T}$$

Where:
L = Failure rate in %/1000 hours
X^2 = The tabular value of chi-squared distribution at a given confidence level and calculated degrees of freedom (2f + 2, where f = number of failures) See note below.
T = # of equivalent device hours = (# of devices) x (# of test hours) x (acceleration factor)

Note: Since the failures of concern here are the long-term failures, not the infant mortality failures (that is, the end of the downward slope and the middle constant section of the bathtub curve in figure 4), X^2 is determined by assuming a one-sided, fixed time test.

Another method of expressing failures is in FITs (failures in time). One FIT is equal to one failure in 10^9 hours. Since L is already expressed as %/1000 hours (10^{-5} failure/hr), an easy conversion from %/1000 hours to FIT would be to multiply the value of L by 10^4.

To accurately determine this failure rate, a statistically large sample size must be accumulated. Depending on the accuracy needed, the following conditions should be imposed:

- A minimum of 1.2 million device hours (equal to sample size multiplied by test period) at 125°C should be accumulated to accurately predict a failure rate of 0.02% per 1000 hours at 55°C, with a 60% confidence level.
- A minimum of 3 million device hours at 125°C should be accumulated to accurately predict a failure rate of 0.01% per 1000 hours at 55°C, with a 60% confidence level.

Failure Rate Calculation Example. As an example of how this failure rate is calculated, assume a sample of 960 pieces was subjected to 1000 hours at 125°C burn-in. One reject was observed. Given that the acceleration factor was calculated to be 34.6 using the Arrhenius equation, what is the failure rate normalized to 55°C using a confidence level of 60%? Express the failure rate in FITs.

Solution:

For $n = 2f + 2 = 2(1) + 2 = 4$, $X^2 = 4.046$

$$\text{Then } L = \frac{(X^2)10^5}{2T} \text{ (\%/1000 hours)}$$

$$= \frac{(X^2)10^5 \text{ (\%/1000 hours)}}{2(\#\text{ devices})(\#\text{ test hours})(\text{accel. factor})}$$

$$= \frac{(4.046)10^5}{2(960)(1000)(34.6)} = 0.0061 \text{ (\%/1000 hours)}$$

Therefore, $FIT = (0.0061)(10^4) = 61$

Failure Rate Goals

Reject rates at customer's incoming inspection, infant mortality rates, and long-term failure rates are monitored and checked against quality and reliability targets. Long-term failure rate goals are based on mask and process designs. NEC's quality and reliability targets are listed in table 2.

Table 2. Quality and Reliability Targets

	Memory		Micro	ASIC		
Year	ECL RAM	MOS		BiCMOS	ECL	CMOS
Reject Rate at Customer's Incoming Equipment Inspection (PPM)						
1991	30	30	70	300	80	80
1992	30	30	50	200	50	60
Long-Term Reliability (FIT)						
1991	30	30	30	300	30	90
1992	30	30	20	300	30	80
Infant Mortality						
1991	30	30	40	300	50	270
1992	30	30	30	300	50	240

FAILURE ANALYSIS

At NEC, failure analysis is performed not only on reliability testing and field failures, but also on products that exhibit defects during production. This data is closely checked for correlation process quality information, inspection results, and reliability test data. Information derived from these failure analyses is fed back into the process.

Since many failure mechanisms can be exhibited by LSI devices, highly advanced analytical tools and methodologies are required to investigate such LSI failures in detail. The standard failure analysis flowchart relating to the returned products from customers is shown in appendix 4.

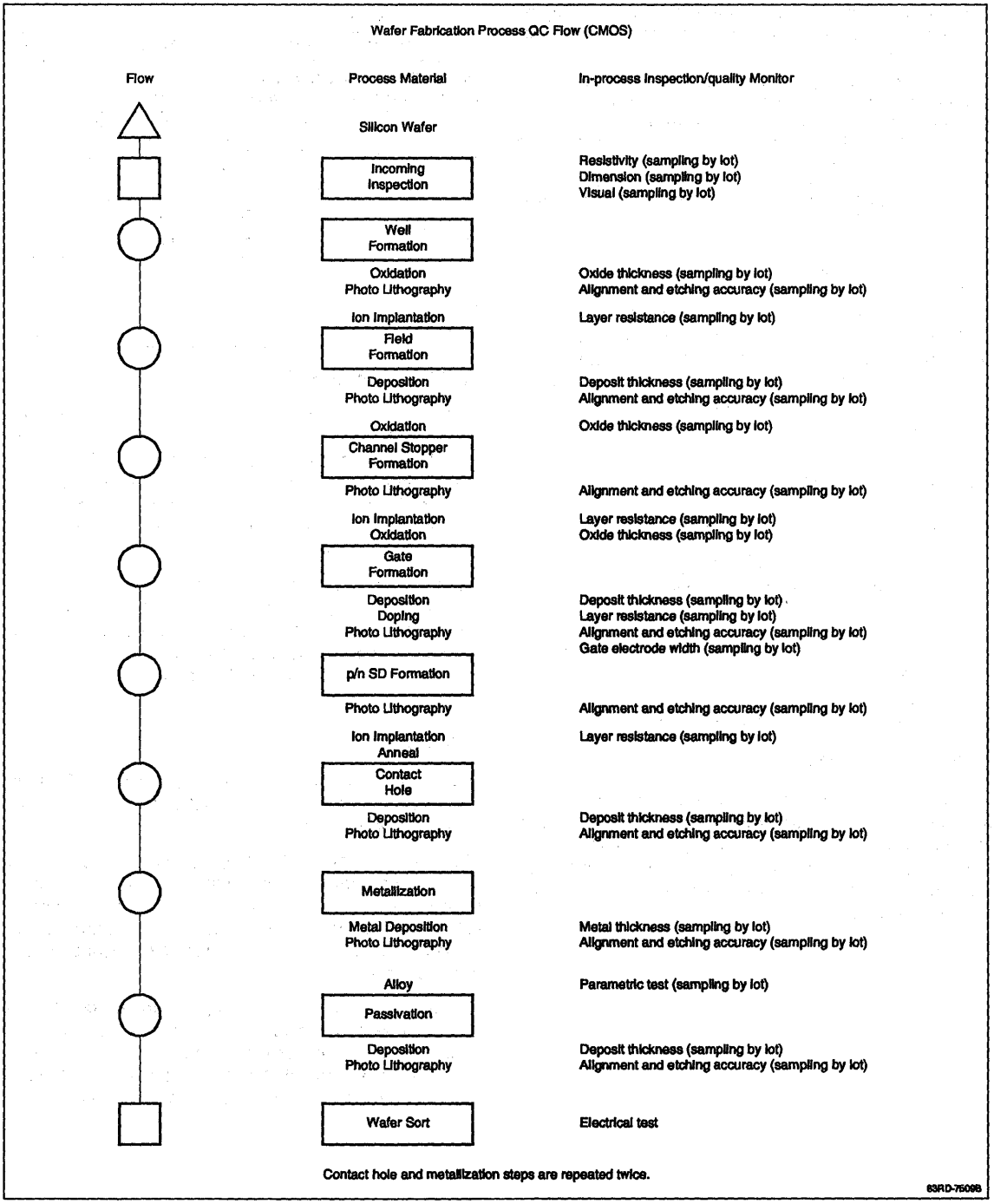
SUMMARY

Building quality and reliability into products by forming a total quality control system is the most efficient way to ensure product success.

The combination of building quality into products, effective prescreening of potential failures, and monitoring of reliability through extensive testing has established a singularly high standard for NEC's large-scale integrated circuits, as demonstrated in the most recent year's production.

The company's quality control program supports continuous research and development activities, extensive failure analysis, and process improvements. With this extensive program, NEC continuously sets and maintains higher standards of quality and reliability.

Appendix 1A. Typical QC Flow for CMOS Fabrication



Appendix 1B. Typical QC Flow for PLCC Assembly/Test

Process/Materials	Inspection of Manufacturing Conditions				Inspection of Manufacturing Qualities			
	Inspection Item	Frequency	Instrument	Inspected by	Inspection Item	Frequency	Instrument	Inspected by
1 Sorted Wafers								
2 Wafer Visual					Wafer Visual	100%	Naked Eye	Operator
3 Dicing	Table Speed DI Water Blade Height	Every Shift	Indicators Gauges	P.C.	Sawing Dimensions	Before Running	Microscope With Filter Eyepiece	Operator
4 Break and Expand	Wafer Break Conditions Wafer Expand Conditions	Every Shift	Indicators Gauges	P.C.	Wafer Visual	100%	Naked Eye	Operator
5 Die Visual Inspection					Die Visual	Every Lot Sampling (Or 100%)	Microscope	Operator
6 Lead Frames	Die Attached Conditions	Every Shift	Indicators Thermocouple, Potentiometer	P.C.	Die Visual Epoxy Coverage	Every Magazine	Naked Eye	Operator
7 Die Attached	Temperature					Every Shift	Microscope	
8 Epoxy Cure (Not Done for Gold Die Attached product)	Heat Temperature N_2 Flow	Every Shift	Indicators Gauges	P.C.	Shear Strength	Every Shift	Dynamometer	Operator
9 Fine Wire	Bonding Conditions	Every Shift	Indicators	P.C.	Visual	Every Magazine	Microscope	Operator
10 Wire Bonding	Temperature	Every Week	Thermocouple and Potentiometer	P.C.	Wire Pull Test	Every Shift	Tension Gauge	Operator
11 Pre-Seal Visual Inspection					Die Visual	Every Lot Sampling (Or 100%)	Microscope	Inspector
12 Molding Compound	Temperature of Pellet, Expiration Date	Every Shift	Thermocouple	P.C.				
13 Molding	Temperature Profile of Die Set Preheat Temperature Pressure Cure Time	Every Shift	Thermocouple, Potentiometer	P.C.	Visual	100%	Naked Eye	Operator
14 Mold Aging	Temperature	Every Shift	Indicator	P.C.				
15 Deflashing	Deflashing Conditions	Every Shift	Indicators	P.C.	Visual	Every Lot	Naked Eye	Operator
	Concentration	Every Week	Titration	Tech.				
	Density	Every Week	Density Meter	Tech.				
	Water Jet Pressure	Every Day	Gauge	Tech.				
16 Plating	Plating Conditions	Every Day	Indicators	P.C.				
	Concentration	Every Week	Titration	Tech.				

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Appendix 1B. Typical QC Flow for PLCC Assembly/Test (cont)

Process/Materials	Inspection of Manufacturing Conditions				Inspection of Manufacturing Qualities			
	Inspection Item	Frequency	Instrument	Inspected by	Inspection Item	Frequency	Instrument	Inspected by
17 Plating Inspection					Visual	Every Lot	Naked Eye	Technician
					Plating Thickness	Every Lot	X-ray	Technician
					Composition	Every Lot	X-ray	Technician
					Solderability	Once/Day	Naked Eye	Technician
18 Marking Ink	Marking Conditions	Every Shift	Indicators	P.C.	Visual	Every Lot	Naked Eye	Operator
19 Marking								
20 Mark Cure	Temperature	Every Shift	Thermocouple	P.C.	Marking Permanency	Twice/Shift	Automatic Tester	Operator
21 Lead Forming	Dimensions	Every Shift (Before Running)	Test Jig. Caliper	Operator	Visual	Every Lot	Naked Eye	Operator
22 Final Assembly Inspection					Visual	Every Lot	Magnifying Lamp	Operator
23 First Electrical Sorting	P.M. Check	Every Day	P.M. Jig.	Operator				
	Sample Check	Before Testing	Test Samples	Operator	Electrical Characteristics	100%	IC Tester	Operator
24 Burn-In (When Necessary)	Burn-In Conditions	Every Batch	Indicator	P.C.				
25 First Electrical Sorting		Every Day Before Testing	P.M. Jig. Test Samples	Operator Operator	Electrical Characteristics	100%	IC Tester	Operator
26 Reliability Assurance Test		Every Month						
27 In-Warehouse Inspection		Every Day Before Testing	P.M. Jig. Test Samples		Electrical Characteristics	Every Lot	IC Tester	Inspector
					Visual (Major)	Every Lot	Naked Eye and Microscope	Inspector
					Visual (Minor)	Every Lot	Naked Eye	Inspector
28 Warehousing								

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Appendix 2. Typical Reliability Assurance Tests

Test	Symbol	MIL-STD-883C Method	Test Conditions
High-temperature operating/bias life (Note 1)	HTOL/HTB	1005	T_A = 125°C; V_{DD} specified per device type
High-temperature storage life (Note 1)	HTSL	1008	T_A = 150°C (175° or 200°C in some cases)
High-temperature/high-humidity (Note 1)	T/H		T_A = 85°C; RH = 85%; V_{DD} = 5.5 V
High-humidity storage life (Note 1)	HHSL		T_A = 85°C; RH = 85%
Pressure cooker (Note 1)	PCT		T_A = 125°C; P = 2.3 atm; RH = 100%
Temperature cycling (Note 1)	T/C	1010	−65°C to +150°C; 1 hour/cycle
Lead fatigue (Note 2)	C3	2004	90-degree bends; 3 bends without breaking
Solderability (Note 3)	C4	2003	230°C; 5 sec; rosin base flux
Soldering heat/temperature cycle/ thermal shock (Note 1)	C6	1010 1011 (Note 4)	10 sec @ 230°C; rosin base flux Ten 1-hour cycles @ −65°C to +150°C Fifteen 10-minute cycles @ 0°C to +100°C

Notes:

(1) Electrical test per data sheet is performed. Devices that exceed the data sheet limits are considered rejects.

(2) Broken lead is considered a reject.

(3) Less than 95% coverage is considered a reject.

(4) MIL-STD-750A, method 2031.

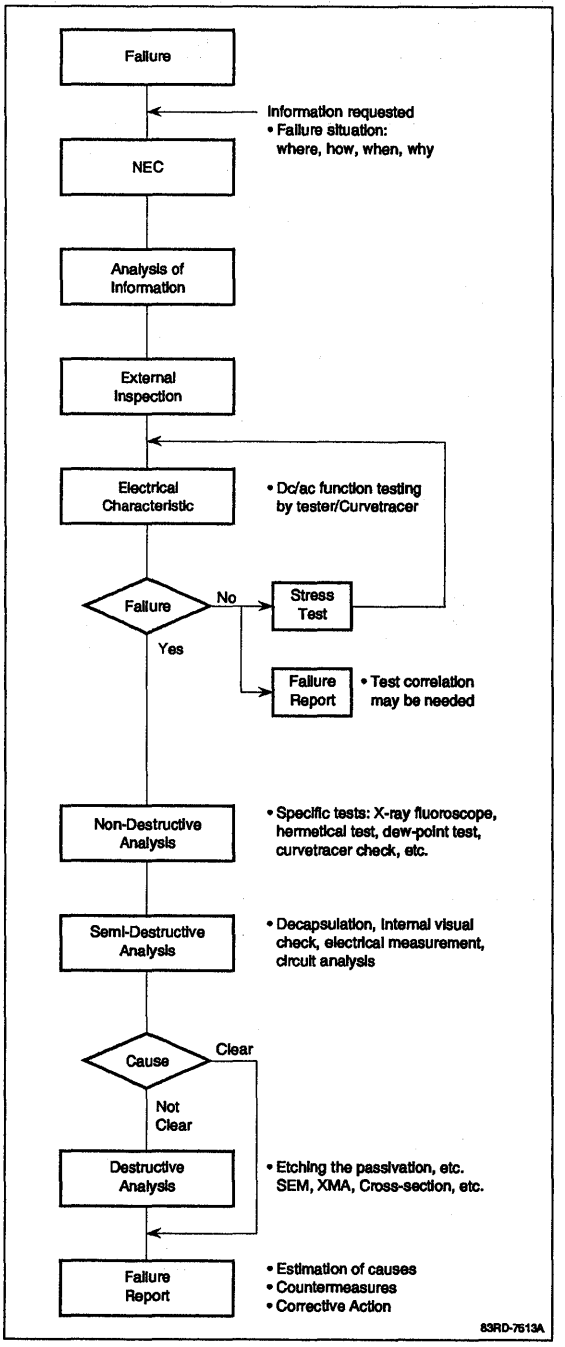
Appendix 3. New Product/Process Change Tests

Test	Sample Size	Newly Developed Product	Shrink Die	New Package	Wafer	Assembly	Test Conditions
High-temperature operating/bias life	20 - 50 pieces; 1 - lots	0	0	0	0	0	See appendix 2; 1000H
High-temperature storage life	10 - 20 pieces; 1 - 3 lots	0	0	0	0	0	T = 150°C (plastic); T = 175°C (ceramic); 1000H
High-temperature/ high-humidity bias life (plastic package)	20 - 50 pieces; 1 - 3 lots	0	0	0	0	0	See appendix 2; 1000H
Pressure cooker (plastic package)	10 - 20 pieces; 1 - 3 lots	0	0	0	0	0	See appendix 2; 288H
Thermal environmental	10 - 20 pieces; 1 - 3 lots	0	X	0	X	0	See appendix 2
Mechanical environmental (ceramic package)	10 - 20 pieces; 1 - 3 lots	0	X	0	X	0	20G, 10 - 2000Hz; 1500G, 0.5 ms; 20000G, 1 min
Lead fatigue	5 pieces; 1 - 3 lots	X	–	X	–	X	See appendix 2
Solderability	5 pieces; 1 - 3 lots	X	–	X	–	X	See appendix 2
ESD	20 pieces; 1 - 3 lots	0	0		0	X	(1) C = 200 pF, R = 0 (2) C = 100 pF, R = 1.5 k
Long term T/C	10 - 50 pieces; 1 - 3 lots	0	0	0	0	0	See appendix 2; 1000 cy

Notes:

0: Performed. X: Perform if necessary. –: Not performed.

Appendix 4. Failure Analysis Flowchart



NEC

Section 3
256K DRAMs

μPD41256
262,144 x 1-Bit
Dynamic NMOS RAM

Description

The μPD41256 is a 262,144-word by 1-bit dynamic RAM designed to operate from a single +5-volt power supply and fabricated with a double polylayer, N-channel, silicon-gate process for high density, high performance, and high reliability. A single-transistor storage cell and advanced dynamic circuitry, including 1024 sense amplifiers, ensure that power dissipation is minimized, while an on-chip circuit generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. A hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute refresh cycles.

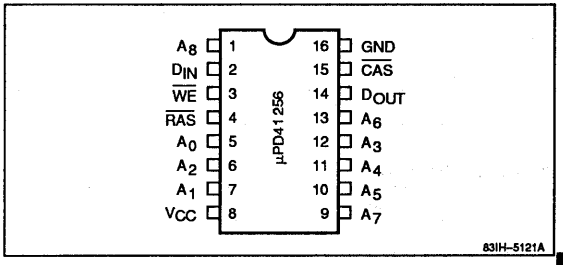
Refreshing may be accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms refresh period.

Features

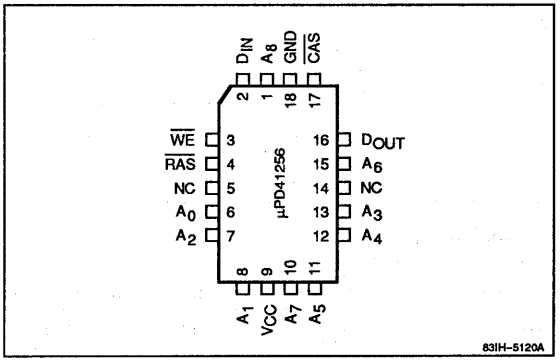
- 262,144-word x 1-bit organization
- High-density plastic DIP and PLCC packaging
- Multiplexed address inputs
- Single +5-volt power supply
- On-chip substrate bias generator
- Low power dissipation of 28 mW max (standby)
- Nonlatched, three-state outputs
- Fully TTL-compatible inputs and outputs
- Low input capacitance
- 256 refresh cycles every 4 ms
- Optional page cycle
- $\overline{RAS}$-only, hidden, and $\overline{CAS}$ before $\overline{RAS}$ refreshing

Pin Configurations

16-Pin Plastic DIP



18-Pin Plastic Leaded Chip Carrier (PLCC)



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Ordering Information

Part Number	Row Access Time (max)	R/W Cycle (min)	Page Cycle (min)	Power Supply Tolerance	Package
μPD41256C-80	80 ns	160 ns	70 ns	±5%	16-pin plastic DIP
C-85	85 ns	165 ns	70 ns		
C-10	100 ns	200 ns	100 ns	±10%	
μPD41256L-80	80 ns	160 ns	70 ns	±5%	18-pin plastic leaded chip carrier
L-85	85 ns	165 ns	70 ns		
L-10	100 ns	200 ns	100 ns	±10%	

Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}$	Column address strobe
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	A_0 - A_8, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_{OUT}	7	pF	D_{OUT}

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_A (ambient)	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

Notes:

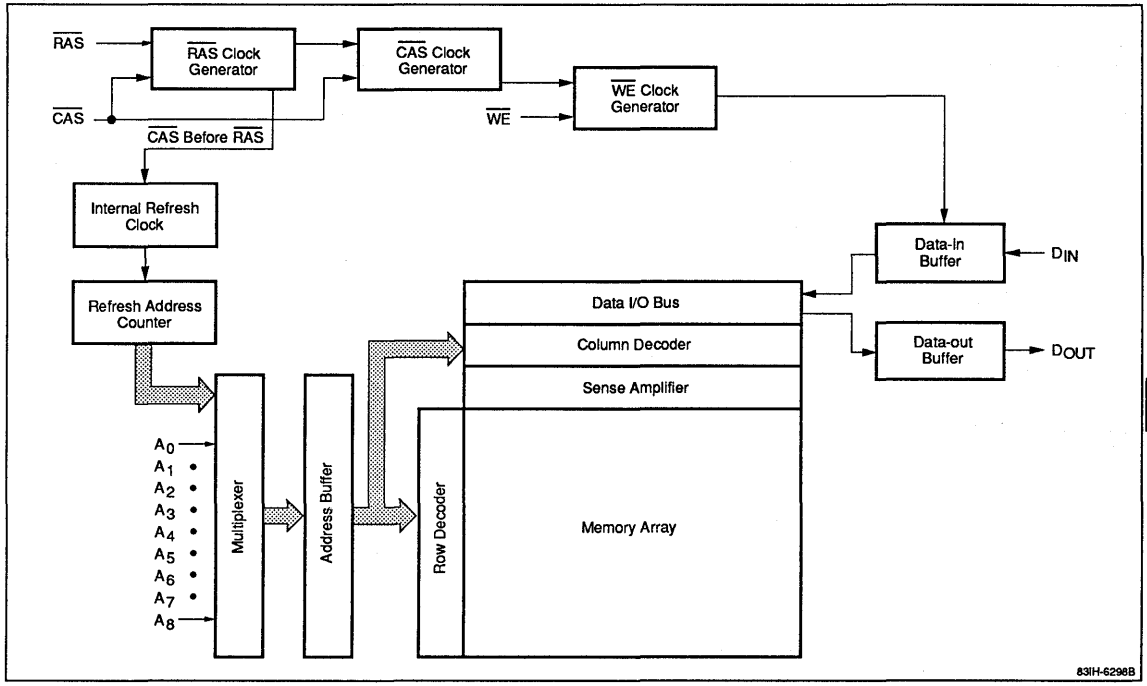
(1) V_{CC} = +5 V ±5% for the −80 and −85 versions.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby supply current	I_{CC2}		5.0	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance
Input leakage current	$I_{I(L)}$	−10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OUT} = −5 mA

Block Diagram



3a

AC Characteristics

T_A = 0 to +70°C

Parameter	Symbol	μPD41256-80 Min	μPD41256-80 Max	μPD41256-85 Min	μPD41256-85 Max	μPD41256-10 Min	μPD41256-10 Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.75	5.25	4.75	5.25	4.5	5.5		
Operating supply current, average	I_{CC1}		90		90		80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} (min); I_O = 0 mA (Note 5)
Operating supply current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		80		80		65	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} (min); I_O = 0 mA (Note 5)
Operating supply current, page cycle, average	I_{CC4}		70		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} (min); I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		80		80		65	mA	$\overline{CAS}$ ≤ V_{IL}; $\overline{RAS}$ cycling; t_{RC} = t_{RC} (min); I/O = 0 mA (Note 5)
Random read or write cycle time	t_{RC}	180		165		200		ns	(Note 6)
Read-write cycle time	t_{RWC}	185		195		240		ns	(Note 6)
Page cycle time	t_{PC}	70		70		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		85		100	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		40		40		50	ns	(Notes 7, 9)

AC Characteristics (cont)

Parameter	Symbol	μPD41256-80		μPD41256-85		μPD41256-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Output buffer turnoff delay	t_{OFF}	0	20	0	20	0	25	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		70		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	16,000	85	16,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	40		40		50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10,000	40	10,000	50	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		85		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	45	20	50	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	20		20		40		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		65		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	20		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		65		75		ns	
Write command pulse width	t_{WP}	20		15		15		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		30		35		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		65		75		ns	
Refresh period	t_{REF}		4		4		4	ms	Addresses A_0 - A_7
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		50		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		85		100		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	(Note 16)

AC Characteristics (cont)

Parameter	Symbol	μPD41256-80 Min	μPD41256-80 Max	μPD41256-85 Min	μPD41256-85 Max	μPD41256-10 Min	μPD41256-10 Max	Unit	Test Conditions
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	20		15		20		ns	(Note 16)
Read-write cycle time (counter test cycle)	t_{TRC}	N/A		N/A		220		ns	(Note 18)
Read-write cycle time (counter test cycle)	t_{TRWC}	N/A		N/A		260		ns	(Note 18)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Output load = 2 TTL loads and 100 pF

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max)

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ in early write cycles and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

(16) DIP products with process codes E, K, P and X do not have the $\overline{CAS}$ before $\overline{RAS}$ refresh feature. All other package types and process codes do have $\overline{CAS}$ before $\overline{RAS}$ refreshing.

On DIP products with process codes E, K, P and X, the external address inputs are required in hidden refresh cycles and the address timing must satisfy t_{ASR} and t_{RAH}, which are specified with respect to the falling edge of $\overline{RAS}$.

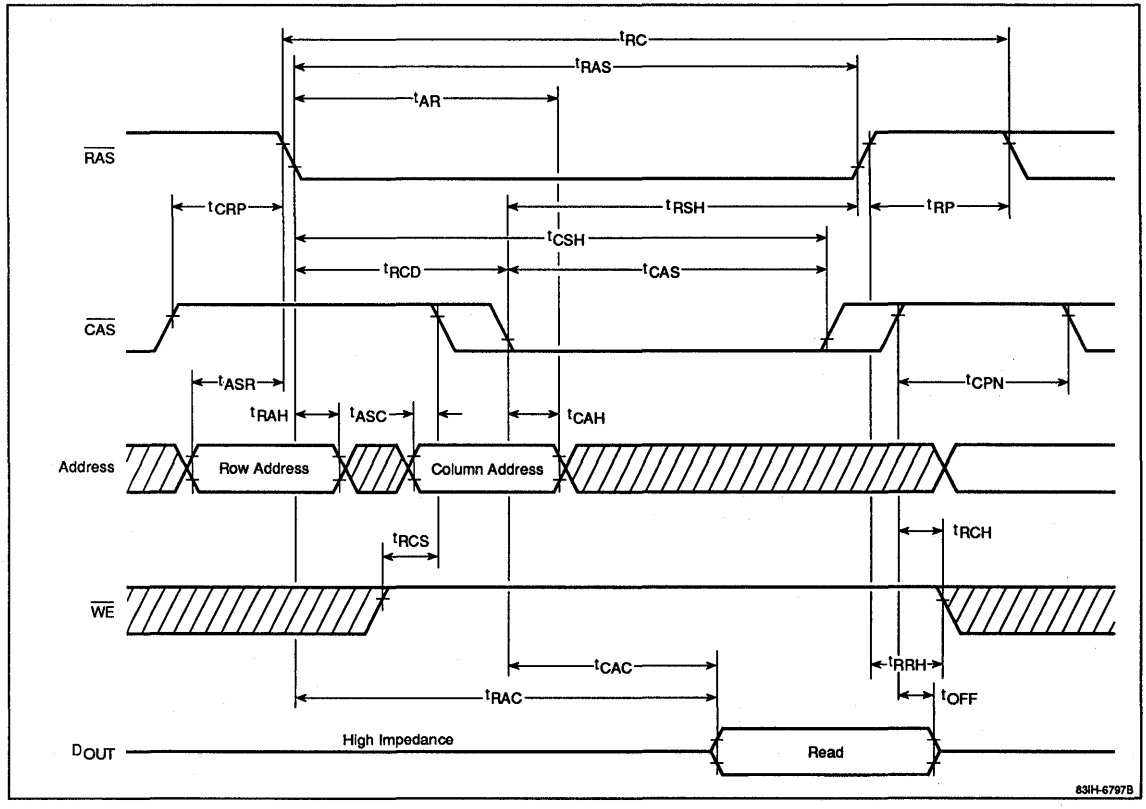
(17) t_{WP} is applicable for a delayed write cycle. If the cycle is early write, it should be satisfied with the specified value of t_{WCH}.

(18) t_{TRC} and t_{TRWL} are applicable for a $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle.

3a

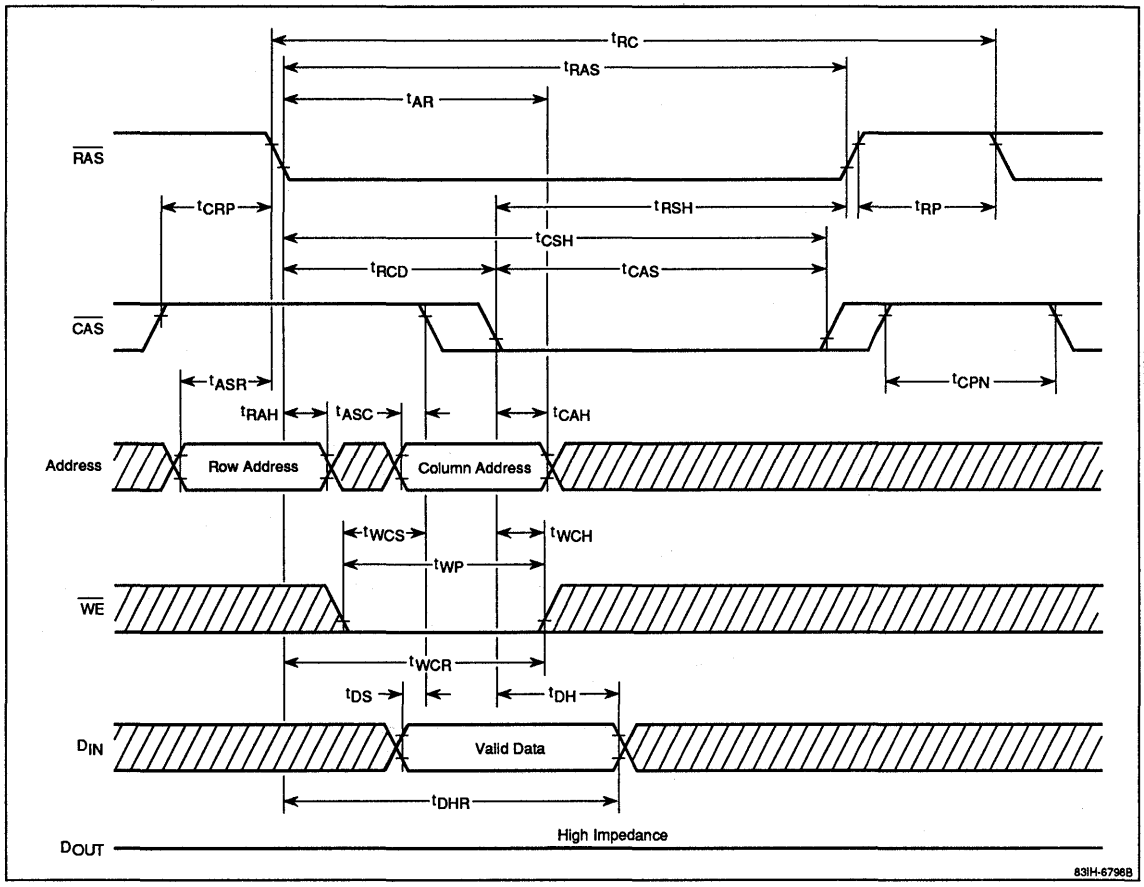
Timing Waveforms

Read Cycle



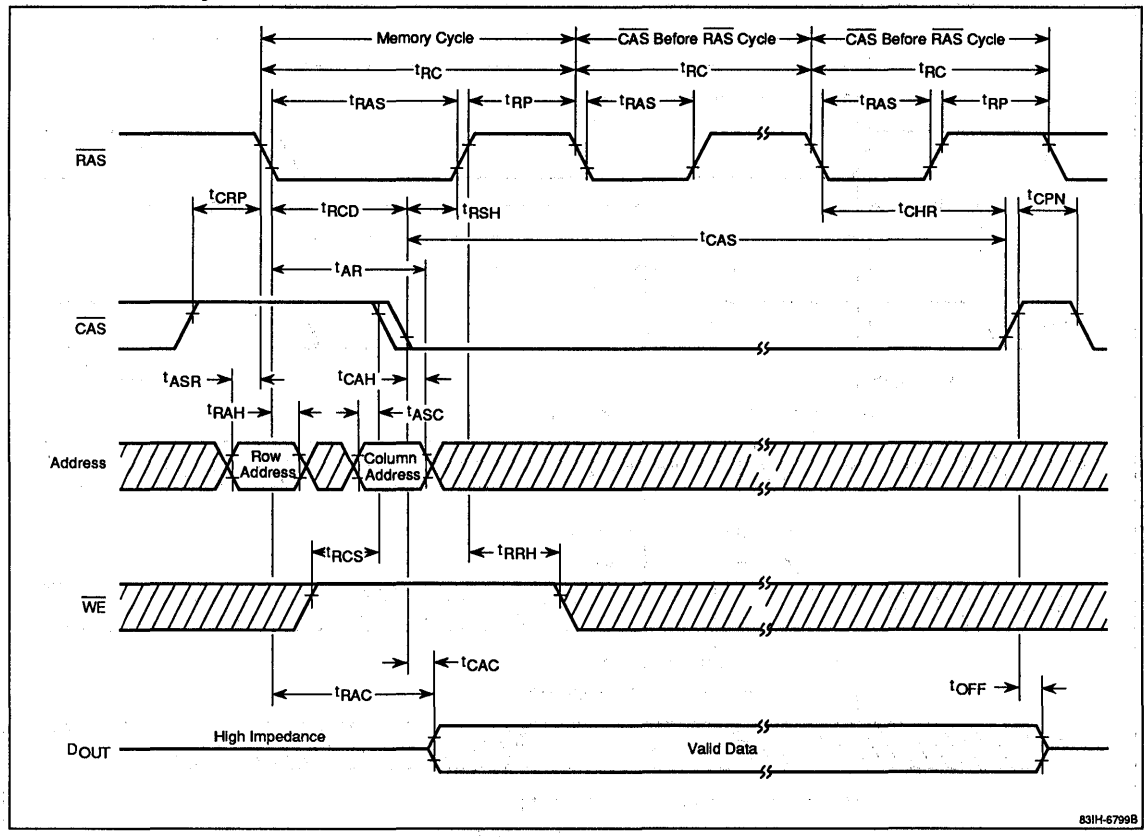
Timing Waveforms (cont)

Early Write Cycle



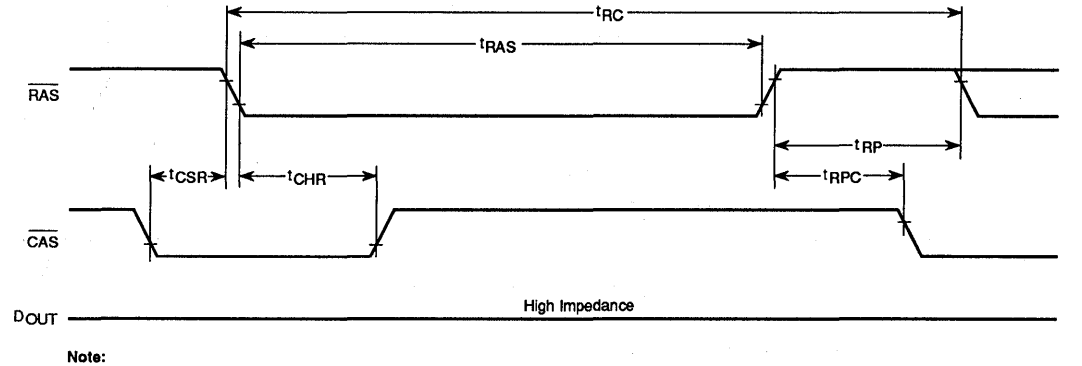
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

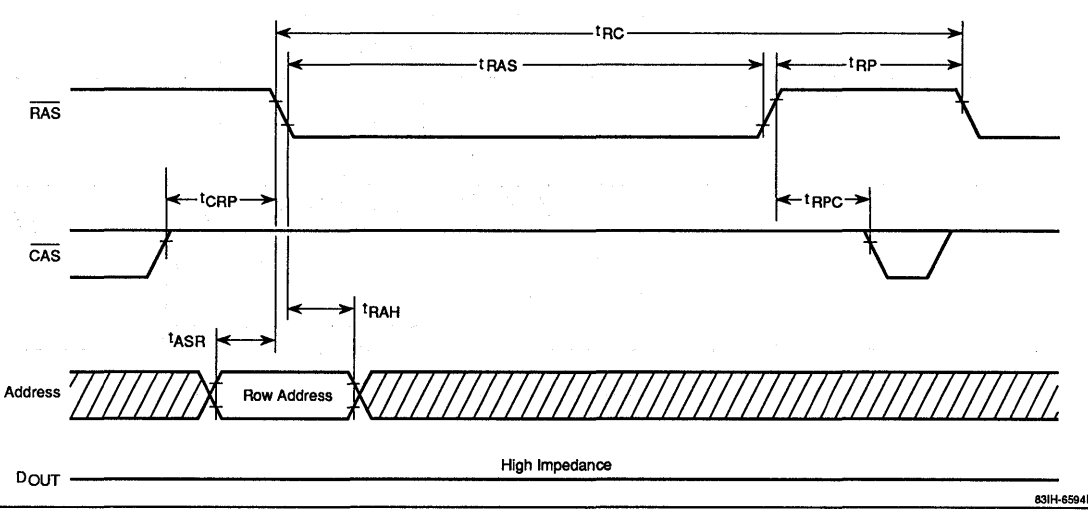
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$ and Address = don't care.

83IH-6592B

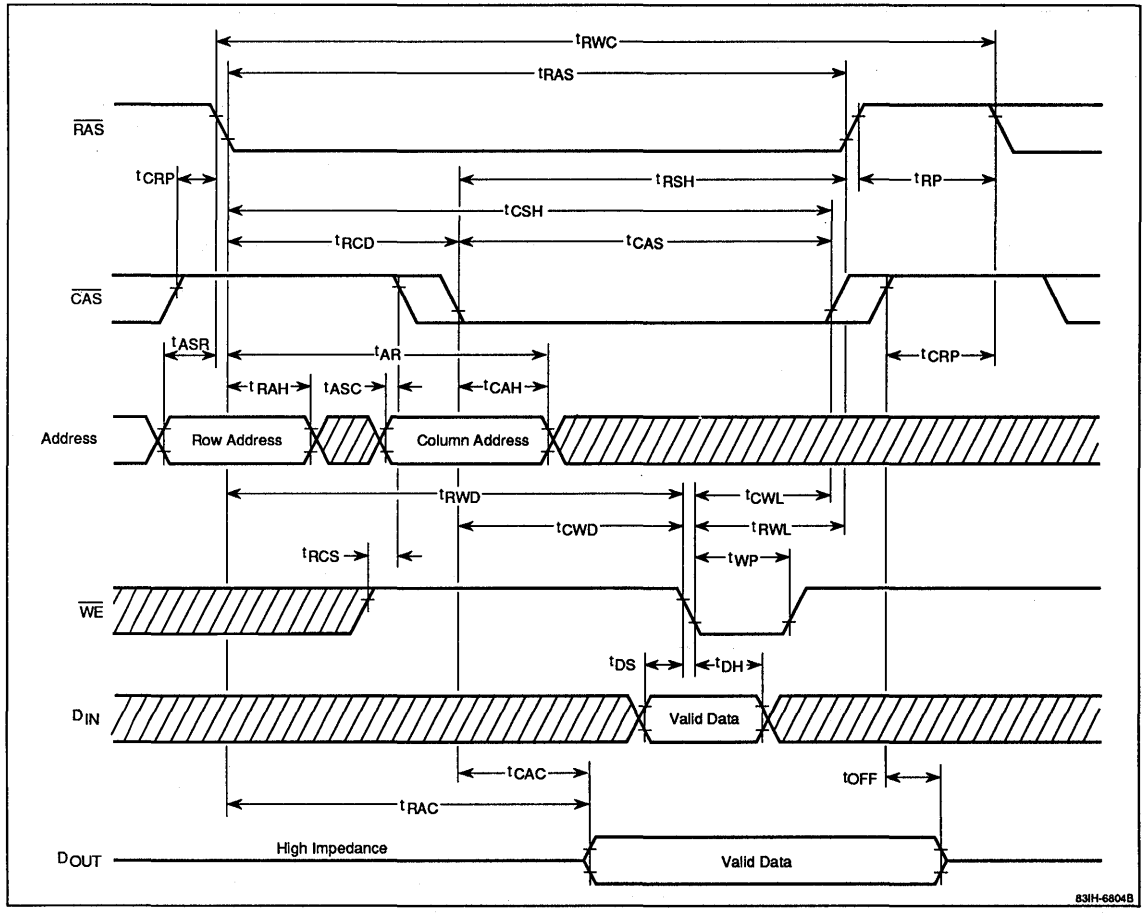
$\overline{RAS}$-Only Refresh Cycle



83IH-6594B

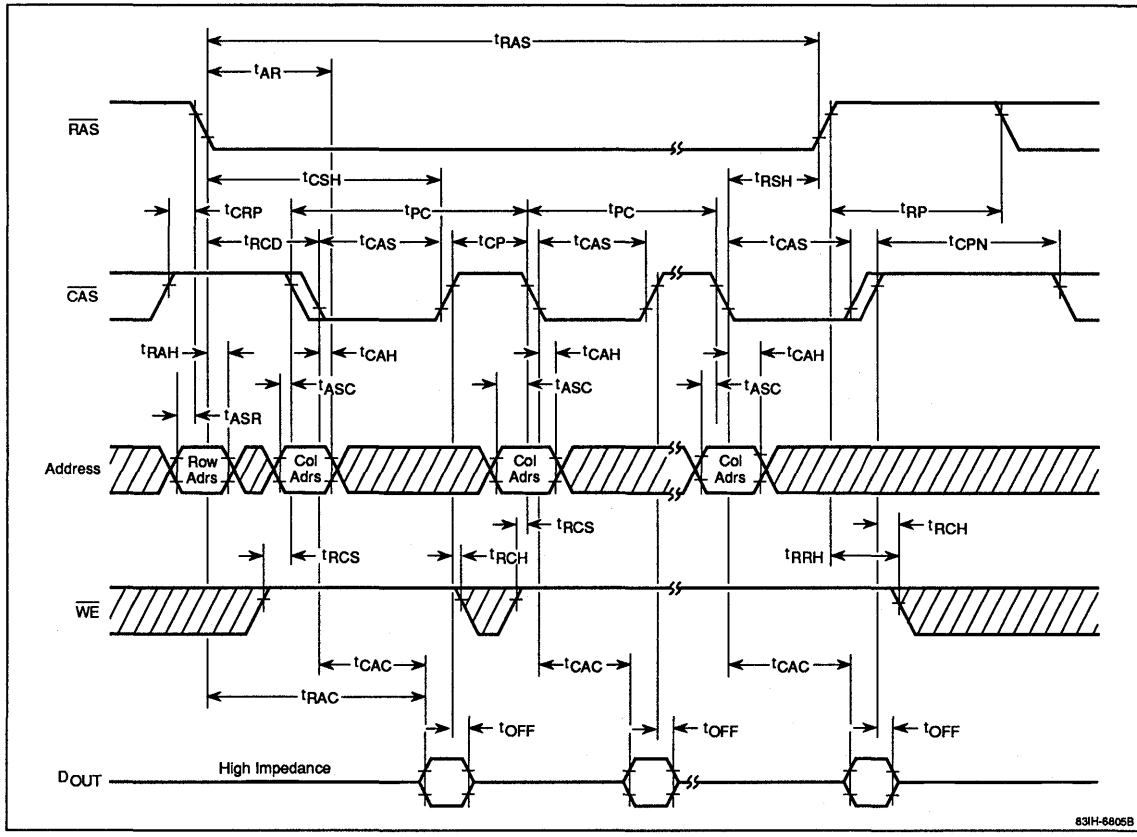
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

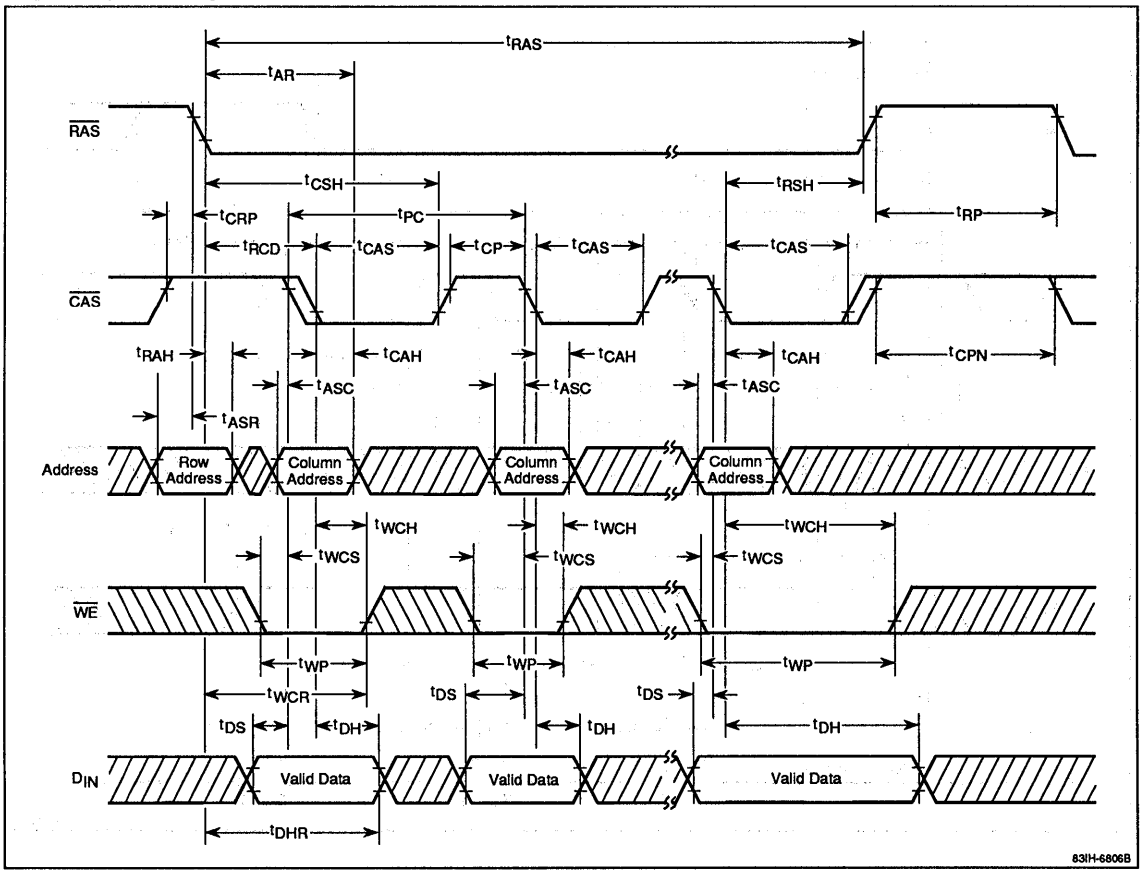
Page Read Cycle



3a

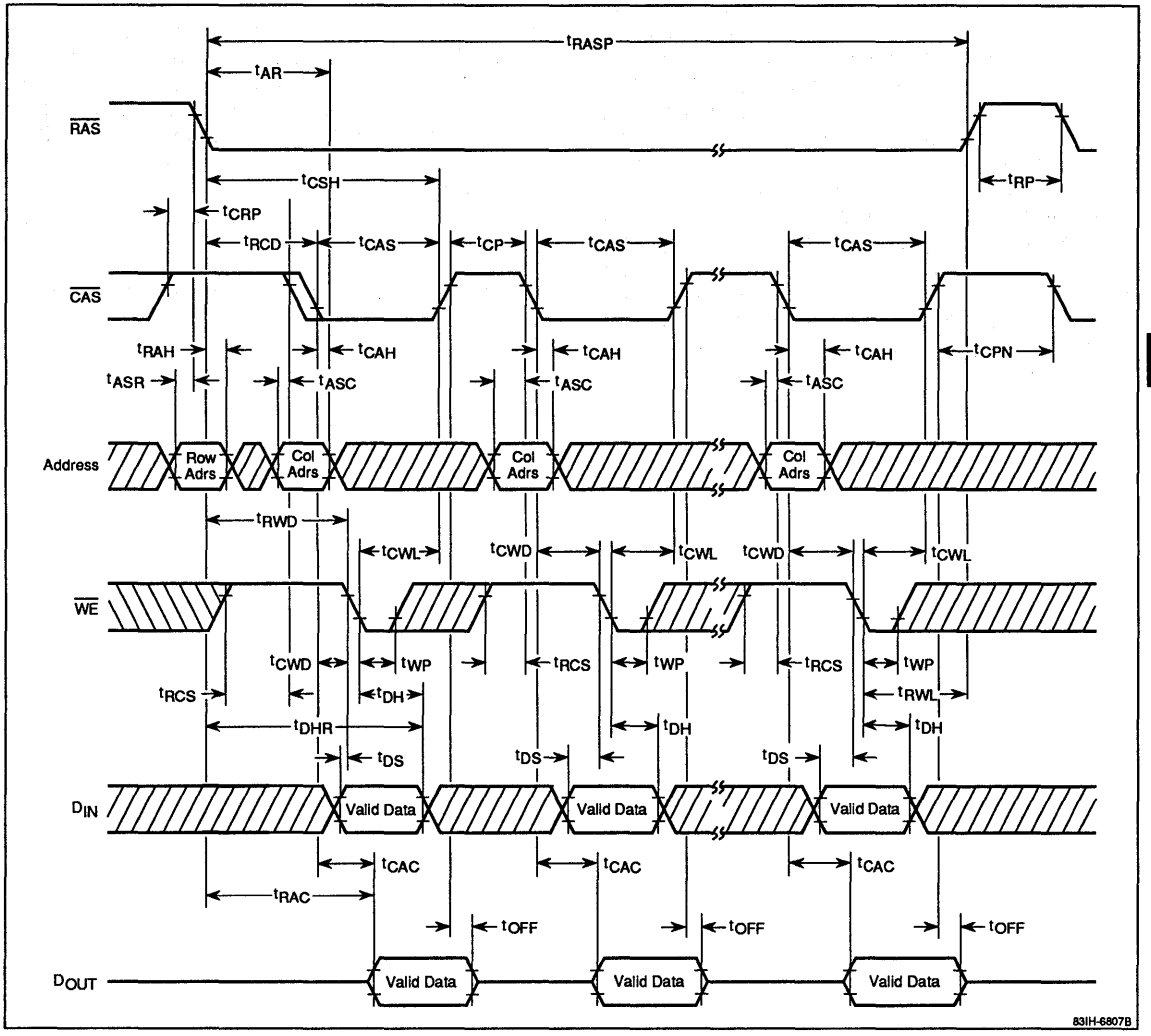
Timing Waveforms (cont)

Page Early Write Cycle



Timing Waveforms (cont)

Page Read-Write/Read-Modify-Write Cycle



3a

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test

The μPD41256 provides a method to verify proper operation of the internal address counter used in $\overline{CAS}$ before $\overline{RAS}$ refreshing. After a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is initiated, $\overline{CAS}$ satisfies a hold time (t_{CHR}), a precharge time (t_{CP}), and then returns low while $\overline{RAS}$ is held low to enable read, write, or read-modify-write operation. As shown in the appropriate timing waveforms, a refresh counter test can be initiated at this point on specified row and column addresses. The row is selected by the internal address counter, and the column is defined by an external address supplied at the second falling edge of $\overline{CAS}$. Test patterns can be generated in several ways; the following example is one possibility. Any pattern must be preceded by the normal power-up procedure containing a pause of 100 μs and then eight $\overline{RAS}$ cycles to initialize the internal counter.

(1) Write "0" into 256 memory cells with 256 $\overline{CAS}$ before $\overline{RAS}$ refresh counter test write cycles. Use the same column address in each cycle.

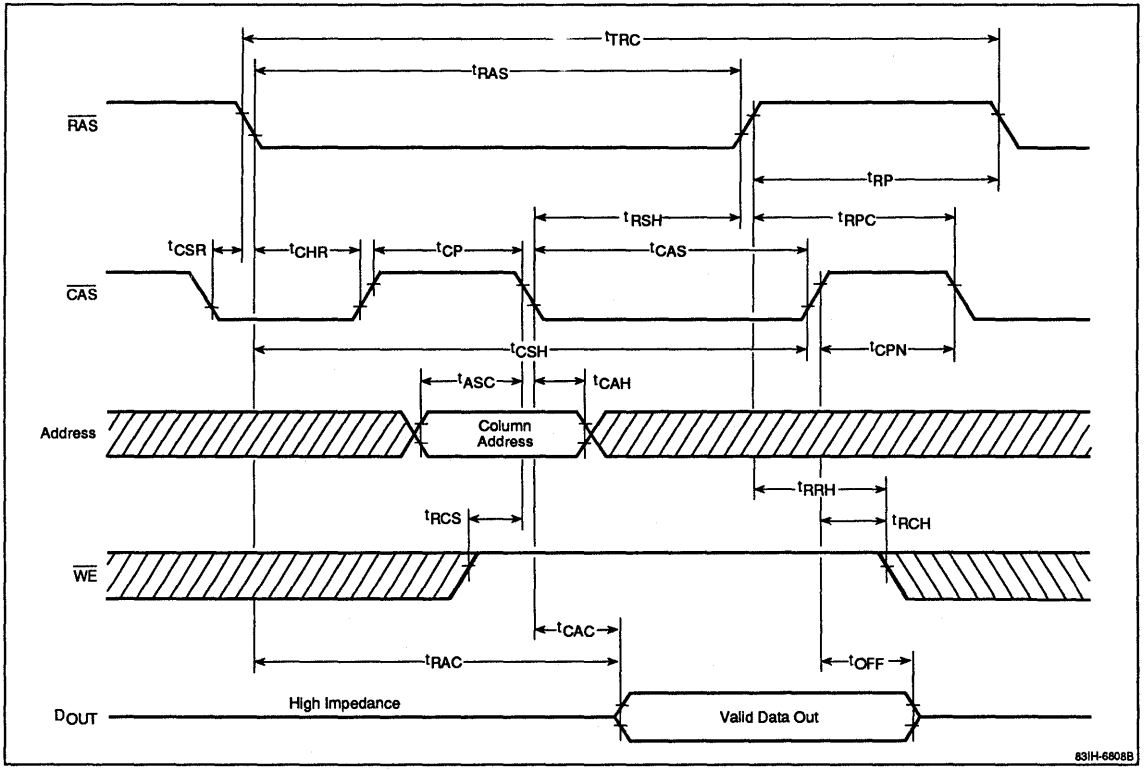
(2) Use a counter test read-modify-write cycle to read the "0" written in the first cycle of step 1 and then write a "1" into that location in the same cycle. Perform this operation 256 times, until a "1" is written into each of the 256 memory cells. Continue using the same column address as specified in step 1.

(3) Read each "1" written in step 2 using a counter test read cycle.

(4) Complement the test pattern and repeat steps 1, 2, and 3.

Timing Waveforms (cont)

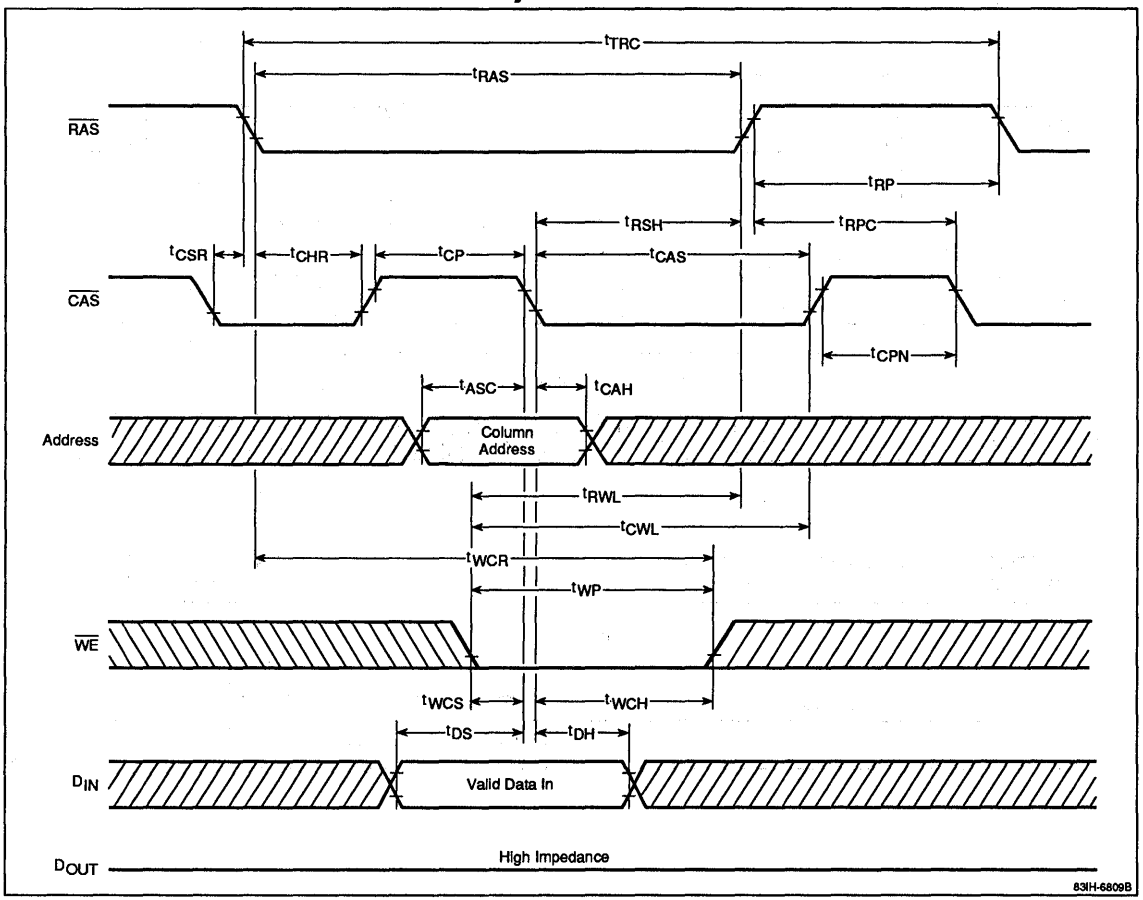
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read Cycle



3a

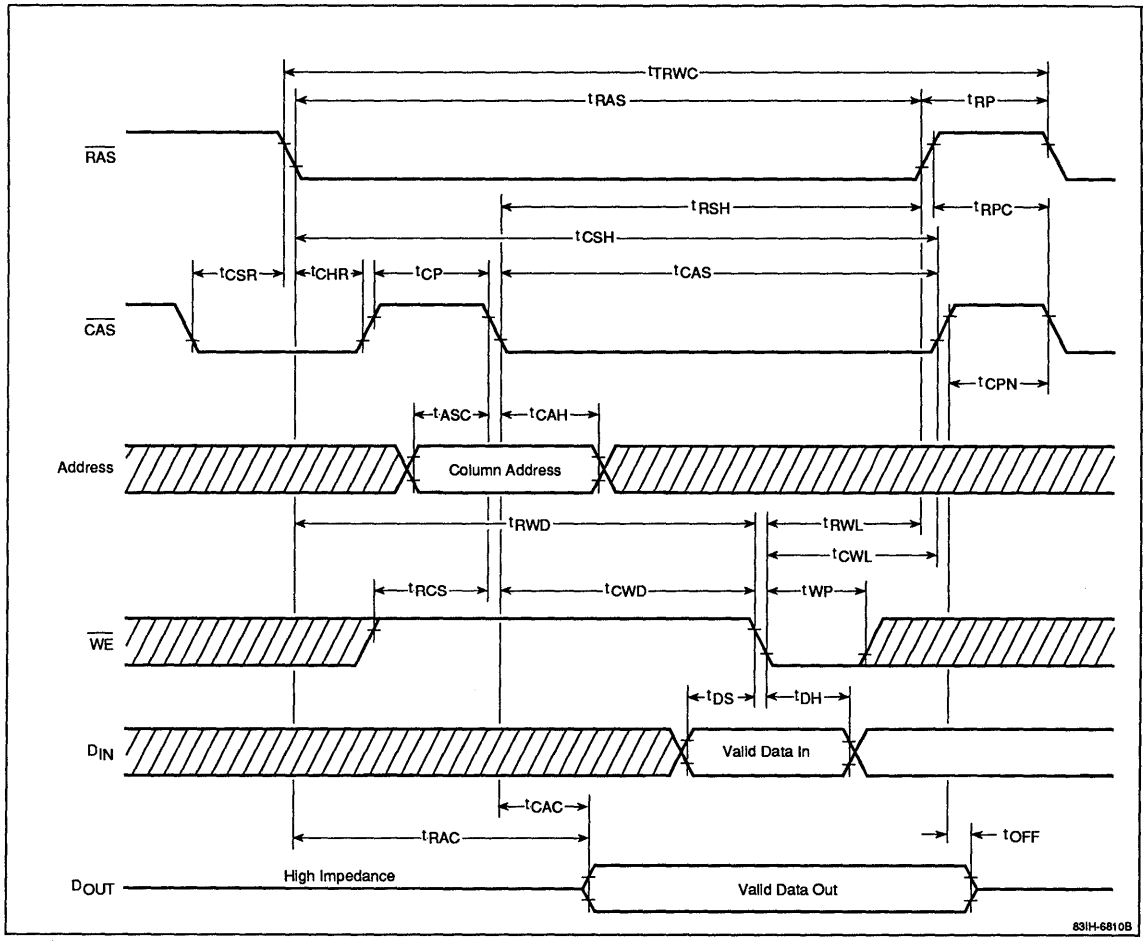
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Write Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read-Modify-Write Cycle



μPD41464
65,536 x 4-Bit
Dynamic NMOS RAM

Description

The μPD41464 is a 65,536-word by 4-bit dynamic RAM designed to operate from a single + 5-volt power supply and fabricated with a double polylayer, N-channel silicon-gate process for high density, high performance, and high reliability. A single-transistor storage cell and advanced dynamic circuitry ensure minimum power dissipation, while an on-chip feature internally generates the negative voltage substrate bias—automatically and transparently.

The three-state I/O is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or hidden refresh cycle, data is held by holding $\overline{CAS}$ low. Data input and output is returned to high impedance by returning $\overline{CAS}$ high. Hidden refreshing allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address, by means of $\overline{RAS}$-only refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms refresh period.

Features

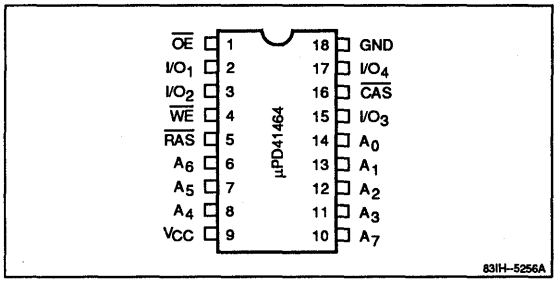
- 65,536-word by 4-bit organization
- Single + 5-volt ±10% power supply
- $\overline{CAS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- Low power dissipation
  - —28 mA max (standby)
  - —440 mW (active, t_{RC} = t_{RC} min)
- Nonlatched, TTL-compatible inputs and outputs
- Low input capacitance
- 256 refresh cycles every 4 ms
- Standard 18-pin plastic DIP and PLCC packaging

Ordering Information

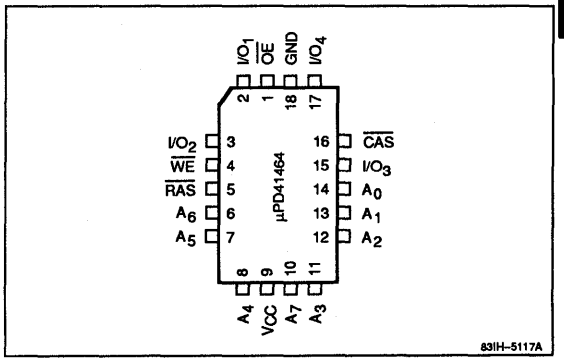
Part Number	Row Access Time (max)	Package
μPD41464C-80	80 ns	18-pin plastic DIP
C-10	100 ns	
C-12	120 ns	
μPD41464L-80	80 ns	18-pin PLCC
L-10	100 ns	
L-12	120 ns	

Pin Configurations

18-Pin Plastic DIP



18-Pin Plastic Leaded Chip Carrier (PLCC)



3b

Pin Identification

Name	Function
A_0 - A_7	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	A_0 through A_7
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 through I/O_4

Absolute Maximum Ratings

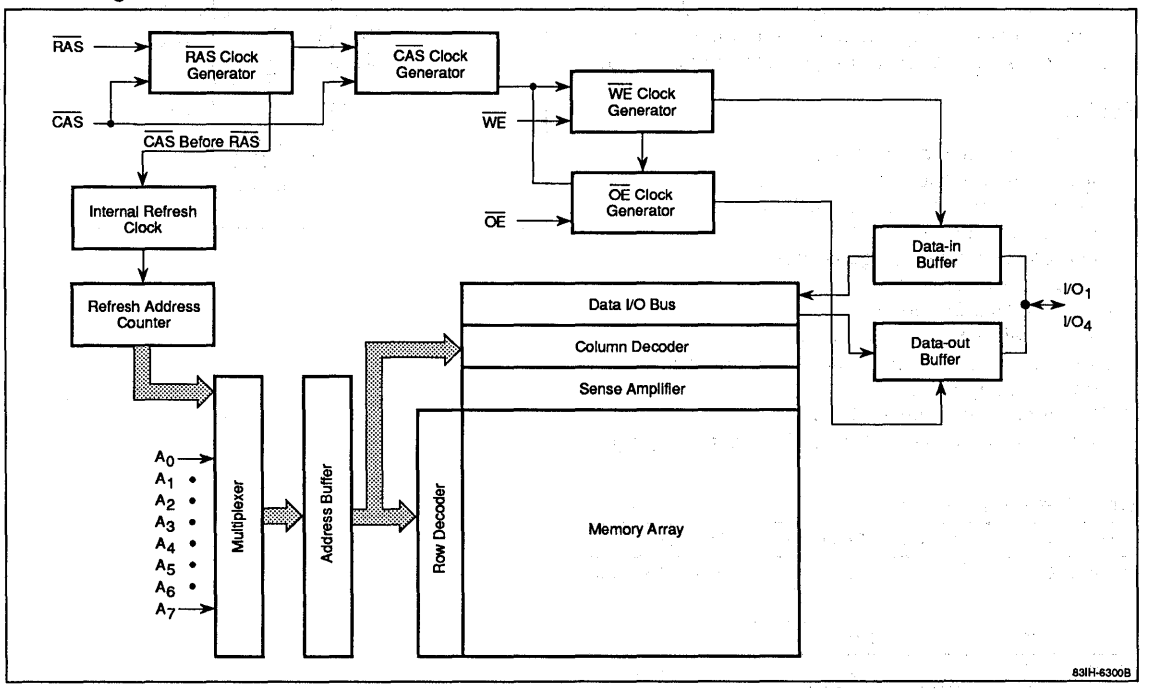
Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1	V
Input voltage, low	V_{IL}	−1		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		5.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
Input leakage current	$I_{I(L)}$	−10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	I/O is high-Z; $V_{I/O}$ = 0 V to V_{CC}
Output voltage, low	V_{OL}	0	0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4	V_{CC}	V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD41464-80		μPD41464-10		μPD41464-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		85		80		75	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, refresh cycle, average	I_{CC3}		70		65		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Operating current, page cycle, average	I_{CC4}		60		55		50	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		70		70		65	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min (Note 5)
Random read or write cycle time	t_{RC}	160		200		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	230		270		300		ns	(Note 6)
Page cycle time	t_{PC}	70		100		120		ns	(Note 6)
Refresh period	t_{REF}		4		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		40		50		60	ns	(Notes 7, 9)
Ouput buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Notes 2, 3)
$\overline{RAS}$ precharge time	t_{RP}	70		90		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10000	50	10000	60	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time for nonpage cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ precharge time for page cycle	t_{CP}	30		40		50		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		80		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD41464-80 Min	μPD41464-80 Max	μPD41464-10 Min	μPD41464-10 Max	μPD41464-12 Min	μPD41464-12 Max	Unit	Test Conditions
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	20		25		30		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		75		90		ns	
Write command pulse width	t_{WP}	20		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		35		40		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		35		40		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	20		25		30		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		75		90		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		155		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	65		80		95		ns	(Note 15)
Access time from $\overline{OE}$	t_{OEA}		20		25		30	ns	
Data delay time	t_{OED}	20		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		10		ns	
Read or write cycle time for counter test cycle	t_{TRC}	185		220		245		ns	(Note 16)
Read or write cycle time for counter test cycle	t_{TRWC}	245		290		325		ns	(Note 16)
$\overline{CAS}$ setup time for $\overline{CAS}$-before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		25		ns	

Notes:

(1) An initial pause of 100 μs ($\overline{RAS}$ inactive) is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(2) AC measurements assume t_T = 5 ns.

(3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals.

(4) All voltages are referenced to GND.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. For lot code K of the μPD41464-15, t_{RC} (min) must be 270 ns and I_{CC3} = 60 mA.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured. For lot code K of the μPD41464-15, t_{RC} (min) must be 270 ns.

(7) Load = 2 TTL loads and 100 pF

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown. For a $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle, t_{RAC} is specified as $t_{RAC} = t_{CHR} + t_{CP} + t_{CAC} + 2t_T$ and is greater than the maximum specified value shown in this table.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

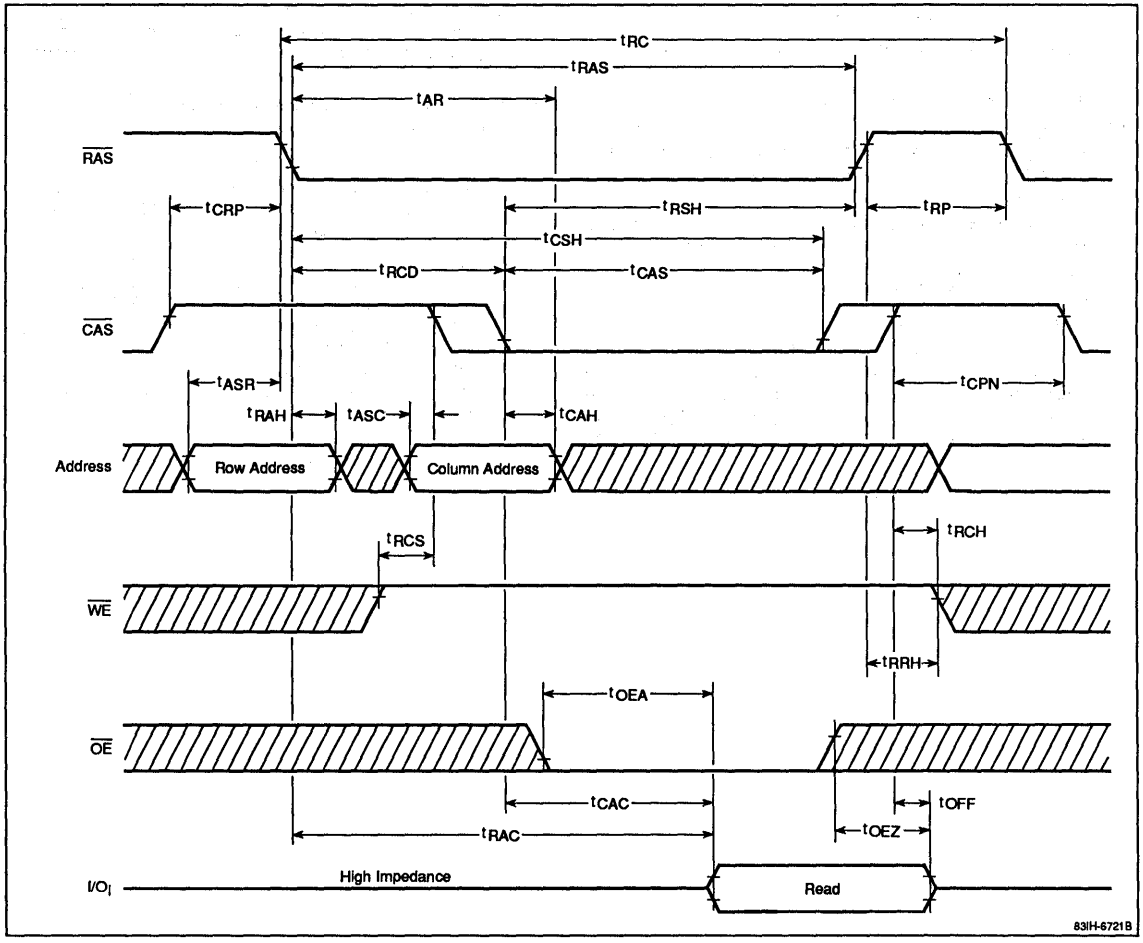
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(16) t_{TRC} and t_{TRWC} are applicable for $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycles.

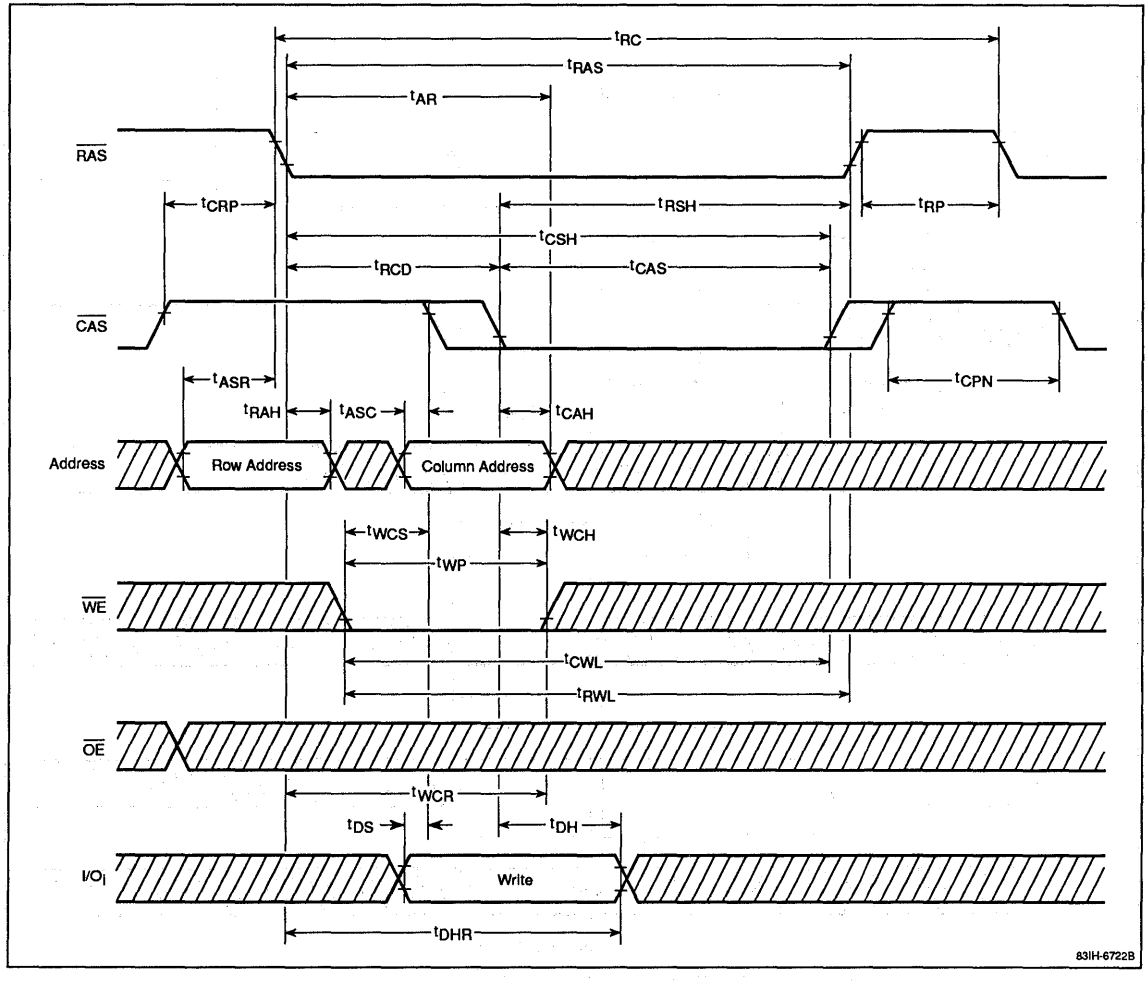
Timing Waveforms

Read Cycle



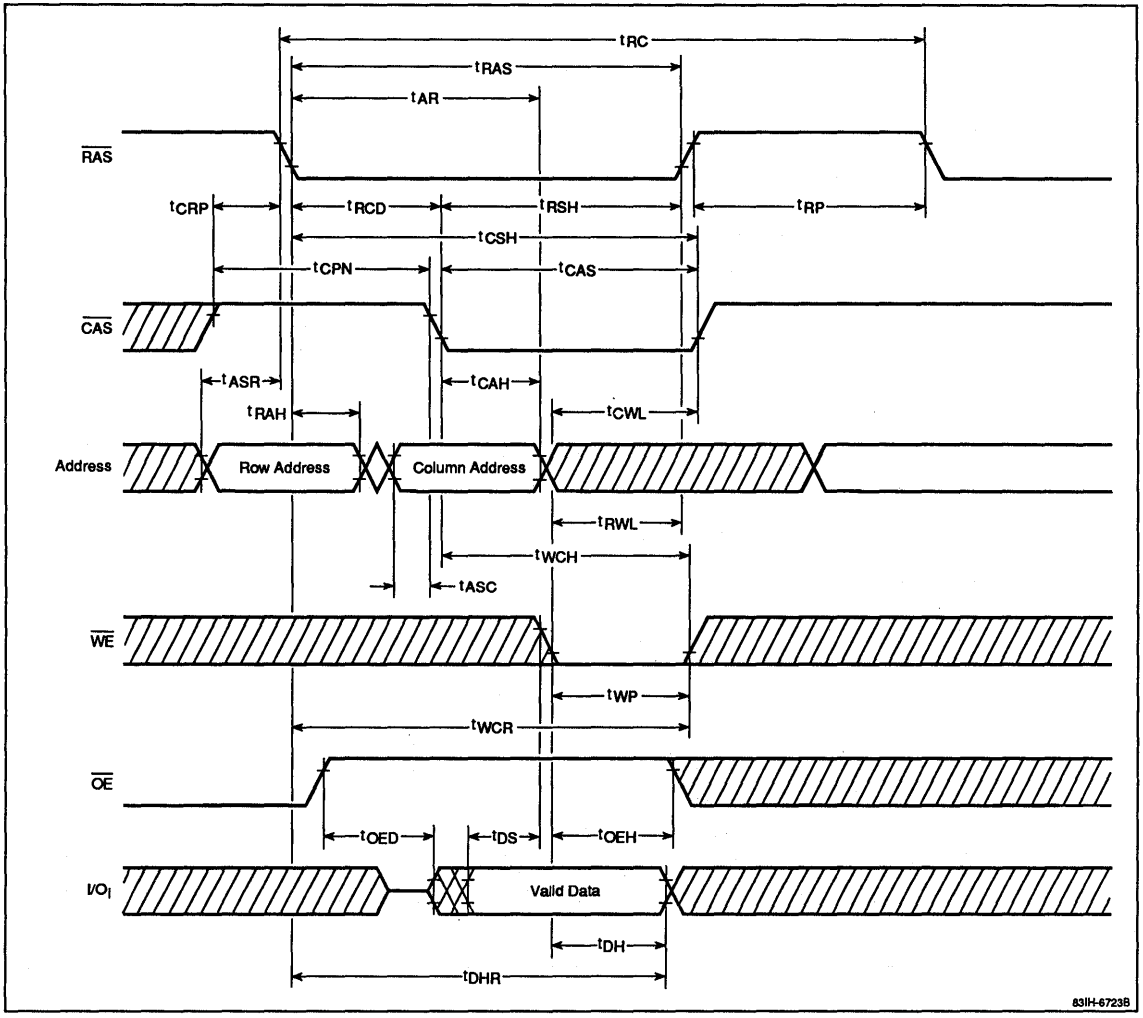
Timing Waveforms (cont)

Early Write Cycle



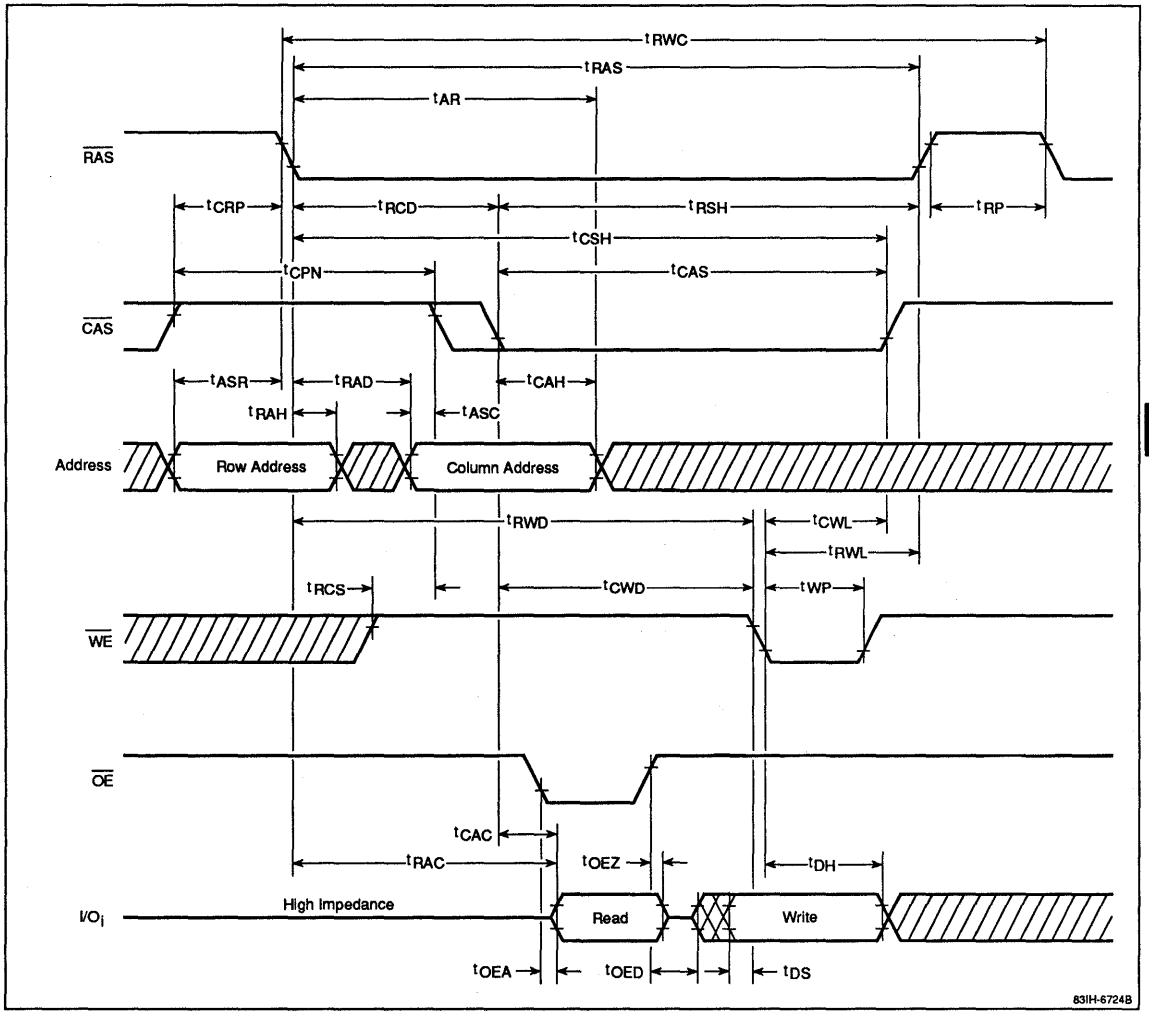
Timing Waveforms (cont)

$\overline{OE}$ -Controlled Write Cycle



Timing Waveforms (cont)

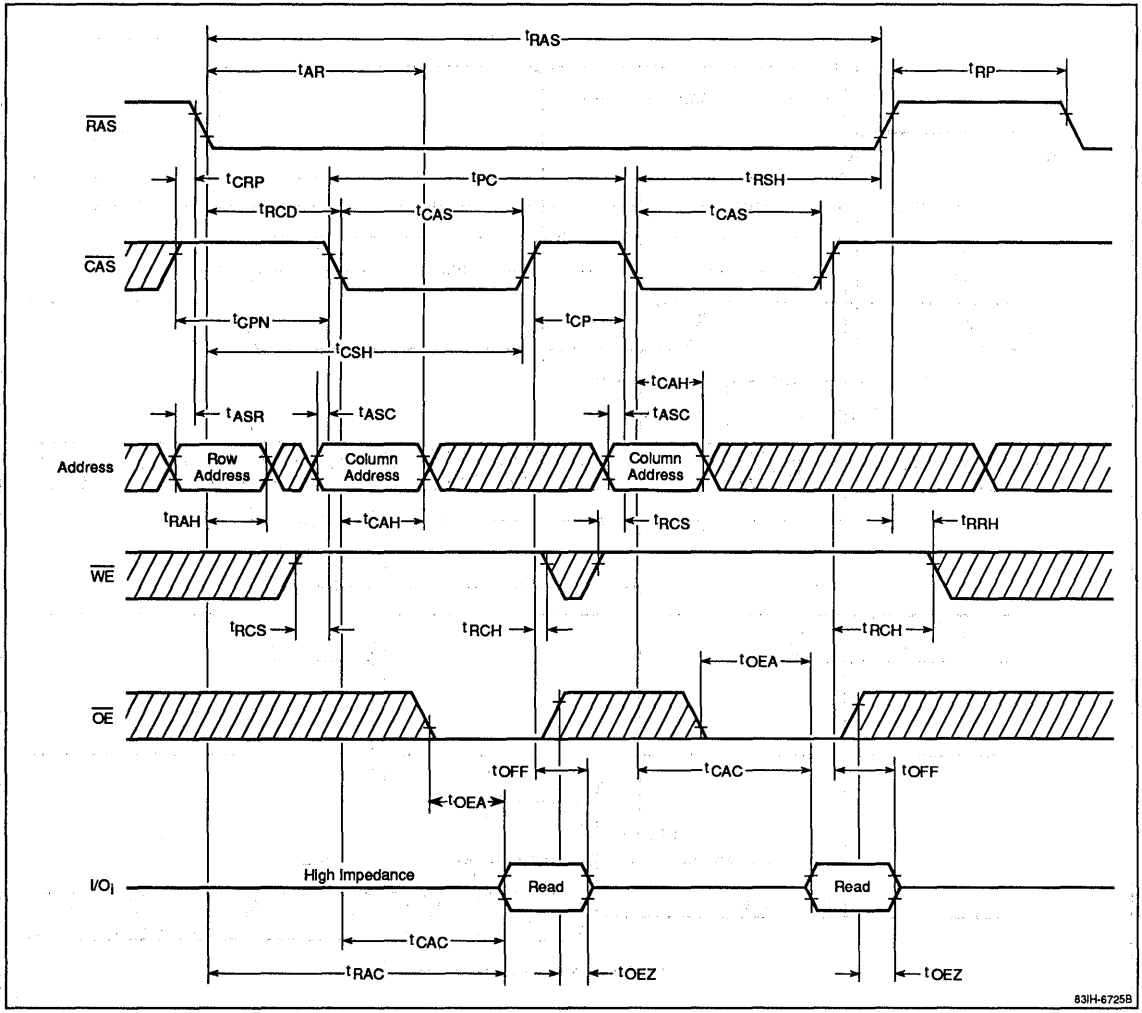
Read-Write/Read-Modify-Write Cycle



3b

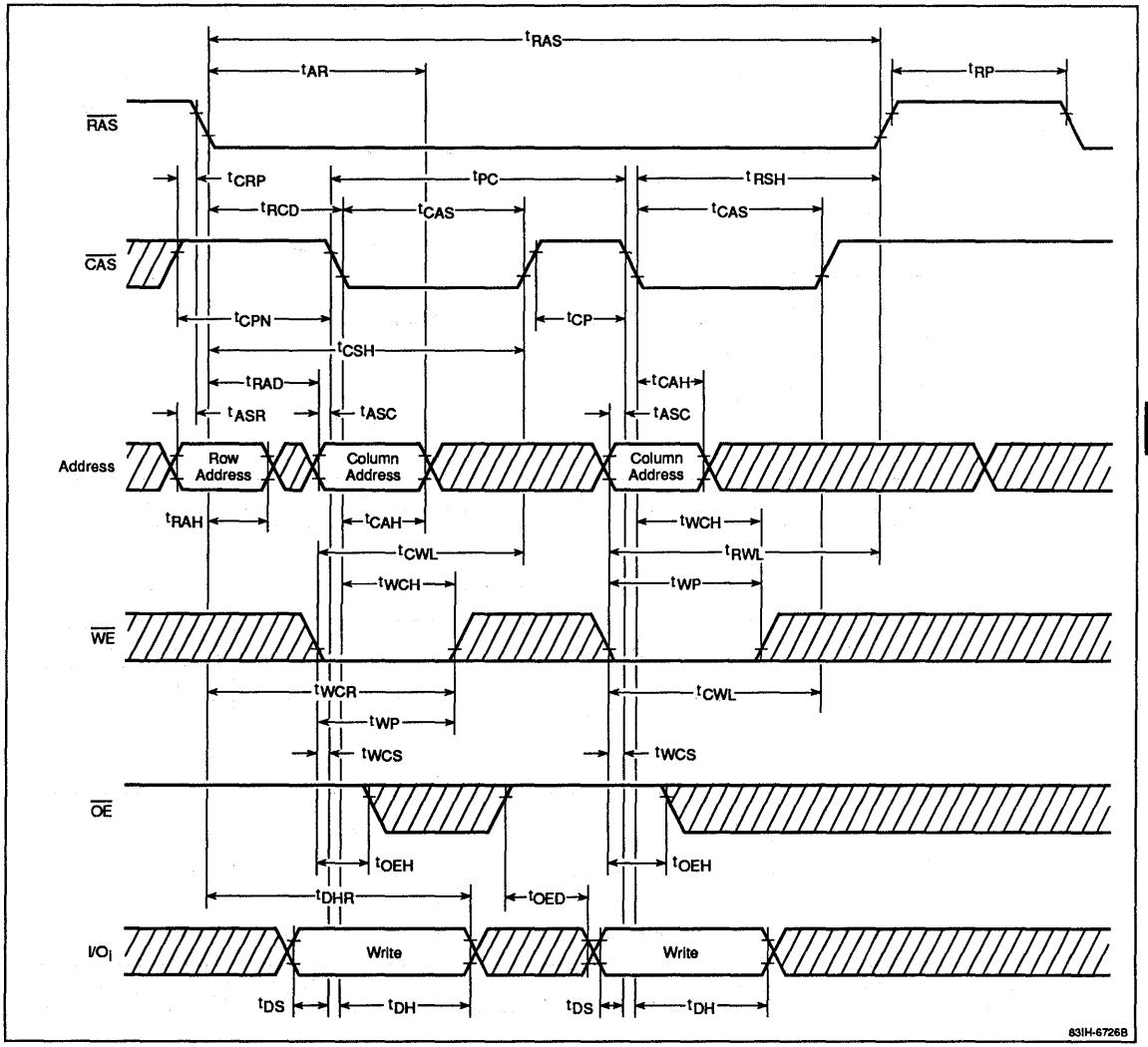
Timing Waveforms (cont)

Page Read Cycle



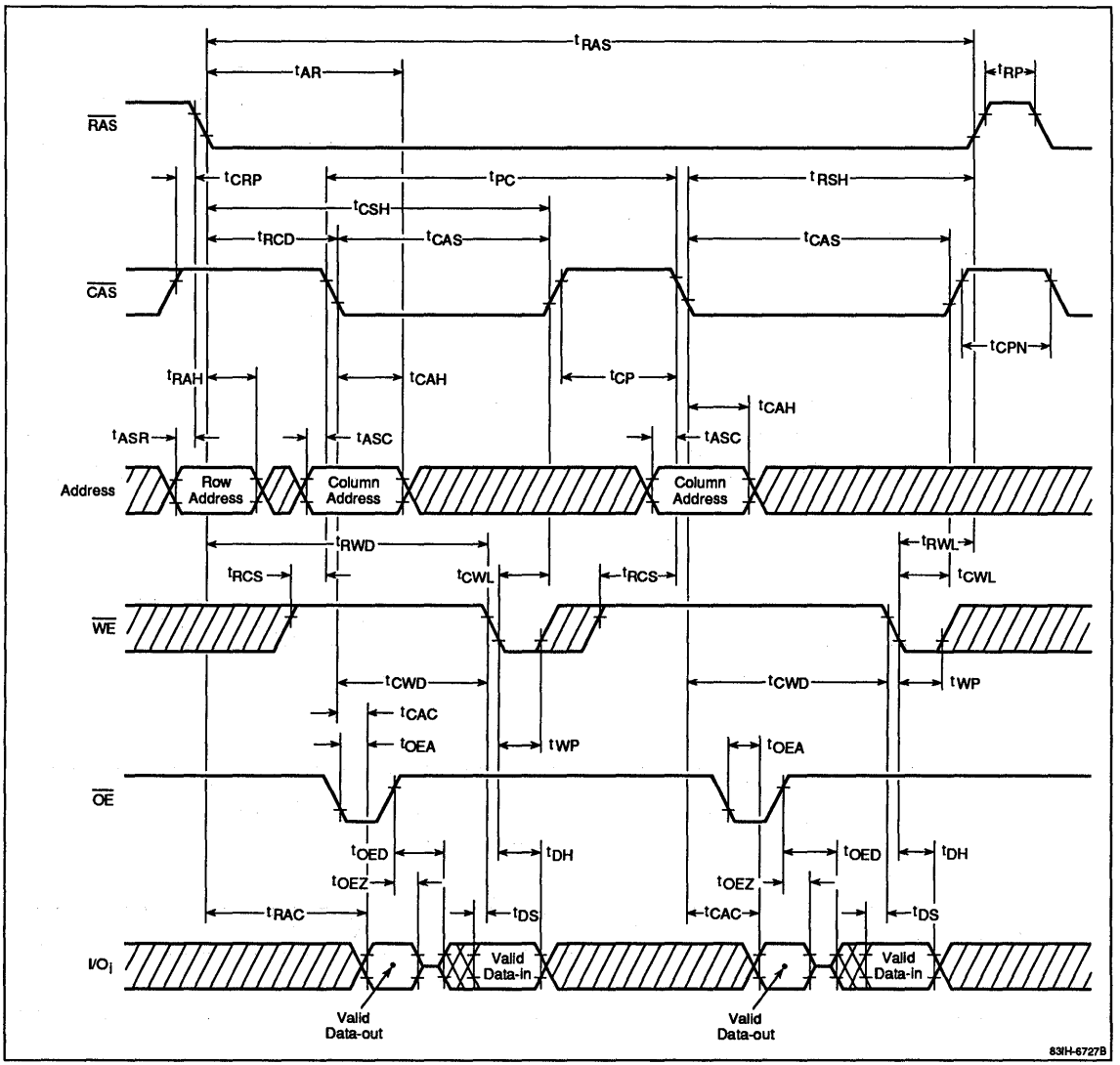
Timing Waveforms (cont)

Page Write Cycle (Early Write)



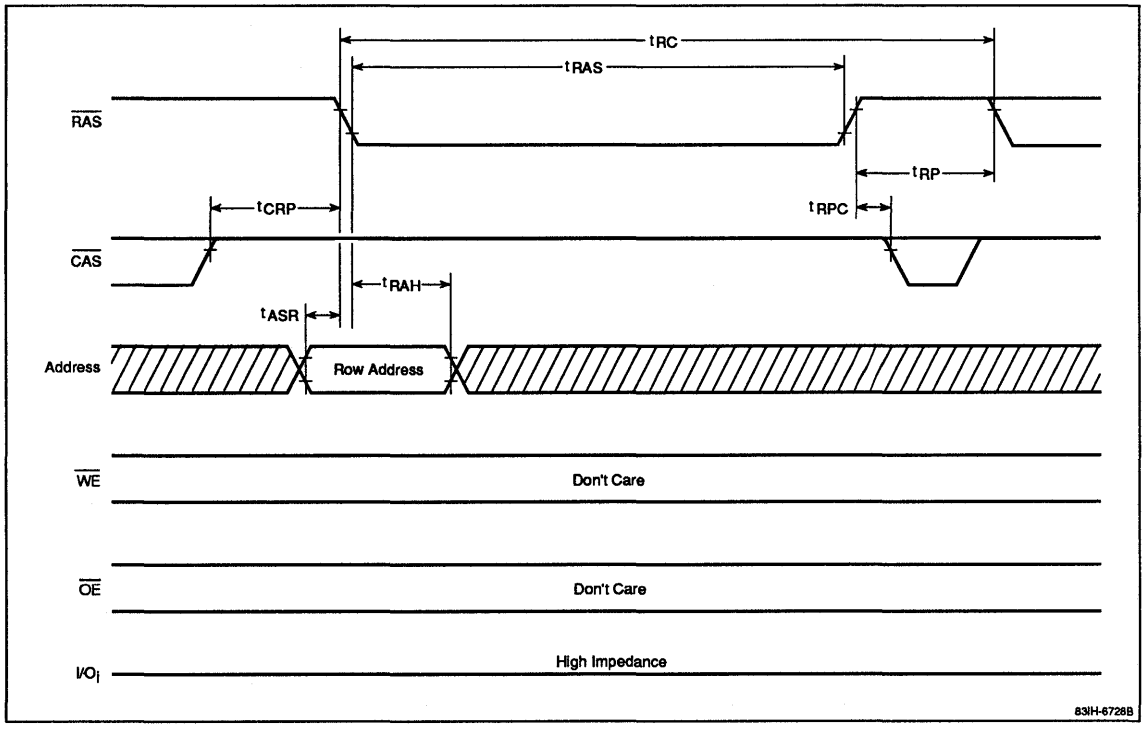
Timing Waveforms (cont)

Page Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



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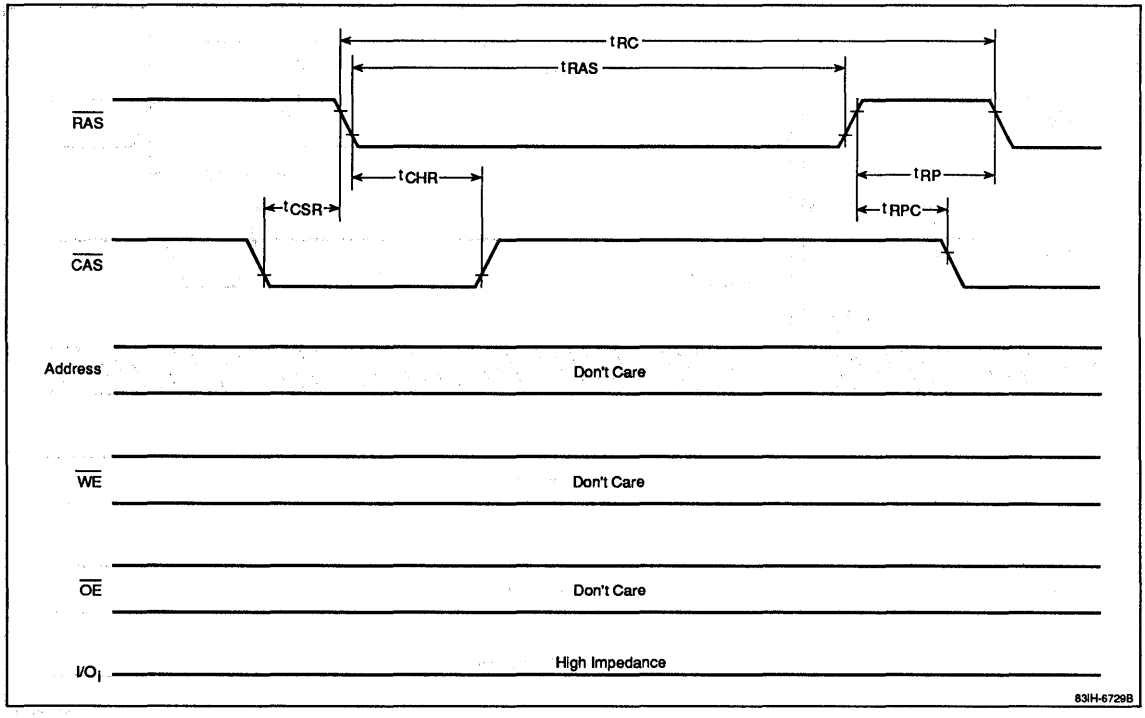
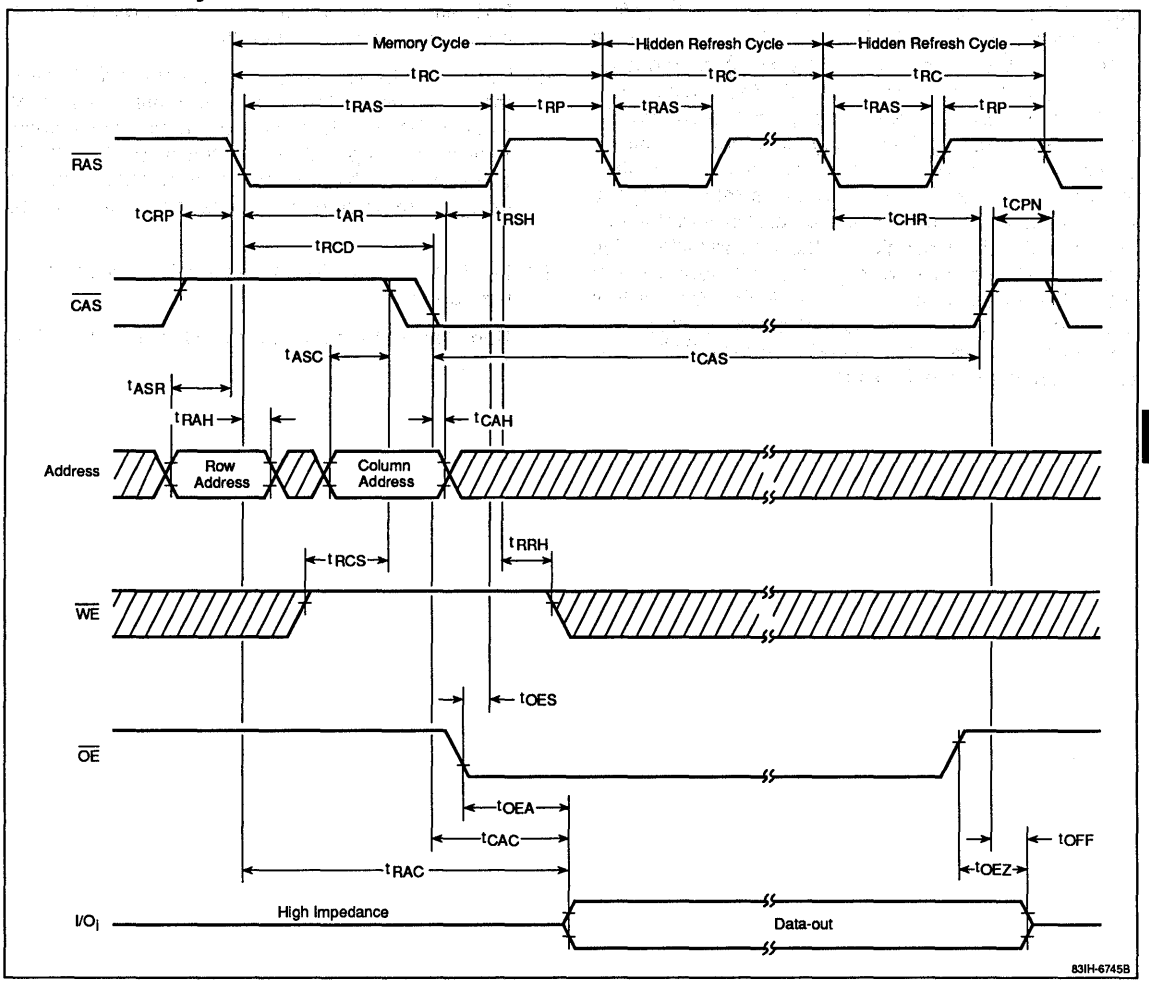
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



3b

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test

The μPD41464 provides a method to verify proper operation of the internal address counter used in $\overline{CAS}$ before $\overline{RAS}$ refreshing. After a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is initiated, $\overline{CAS}$ satisfies a hold time (t_{CHR}), a precharge time (t_{CP}), and then returns low while $\overline{RAS}$ is held low to enable read, write, or read-modify-write operation. As shown in the appropriate timing waveforms, a refresh counter test can be initiated at this point on specified row and column addresses. The row is selected by the internal address counter, and the column is defined by an external address supplied at the second falling edge of $\overline{CAS}$. Test patterns can be generated in several ways; the following example is one possibility. Any pattern must be preceded by the normal power-up procedure containing a pause of 100 μs and then eight $\overline{RAS}$ cycles to initialize the internal counter.

(1) Write "0" into 256 memory cells with 256 $\overline{CAS}$ before $\overline{RAS}$ refresh counter test write cycles. Use the same column address in each cycle.

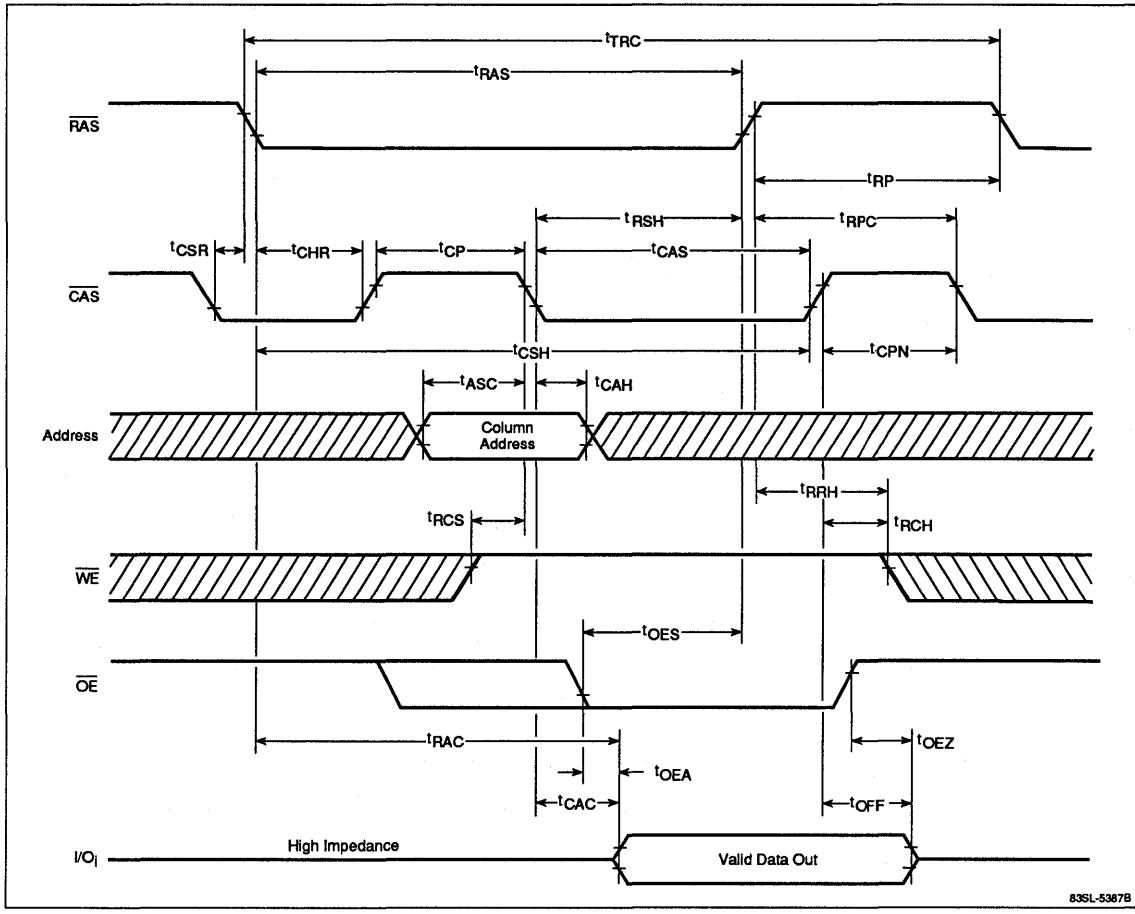
(2) Use a counter test read-modify-write cycle to read the "0" written in the first cycle of step 1 and then write a "1" into that location in the same cycle. Perform this operation 256 times, until a "1" is written into each of the 256 memory cells. Continue using the same column address as specified in step 1.

(3) Read each "1" written in step 2 using a counter test read cycle.

(4) Complement the test pattern and repeat steps 1, 2, and 3.

Timing Waveforms (cont)

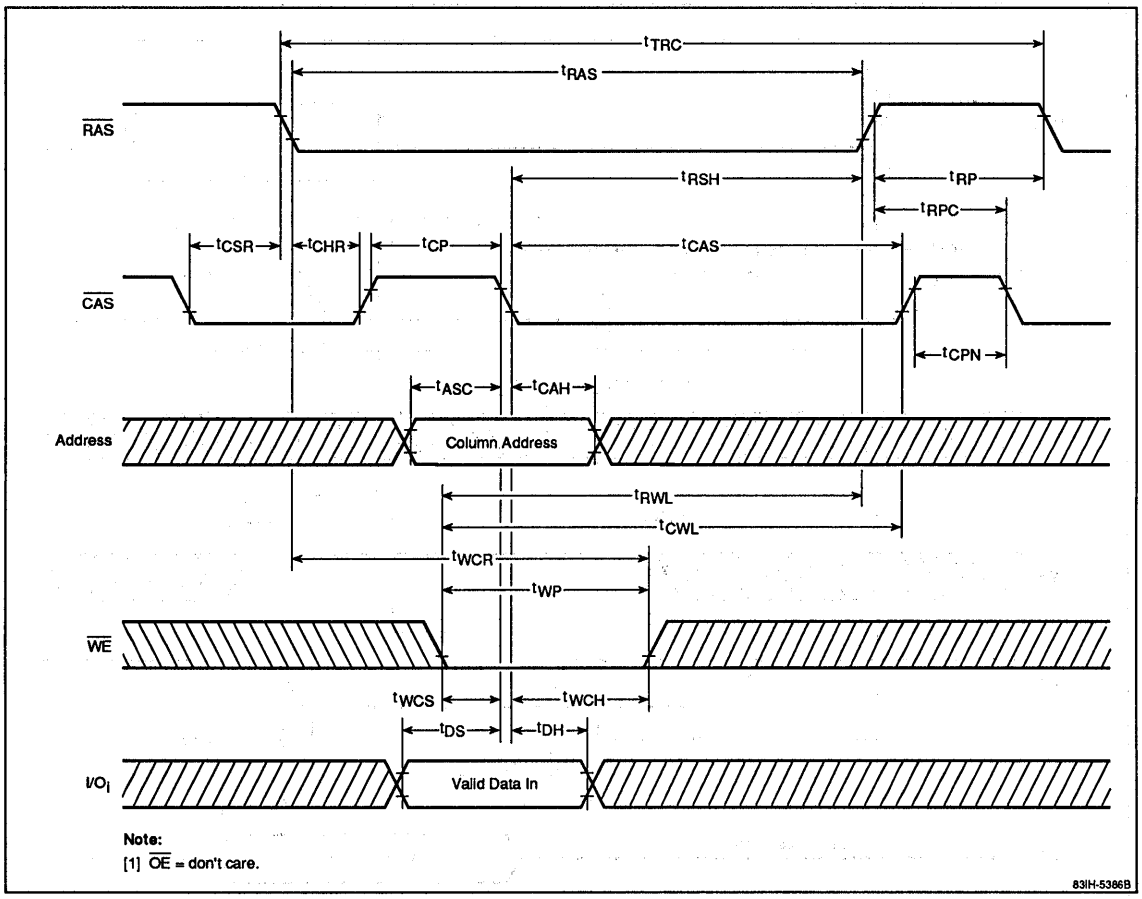
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read Cycle



3b

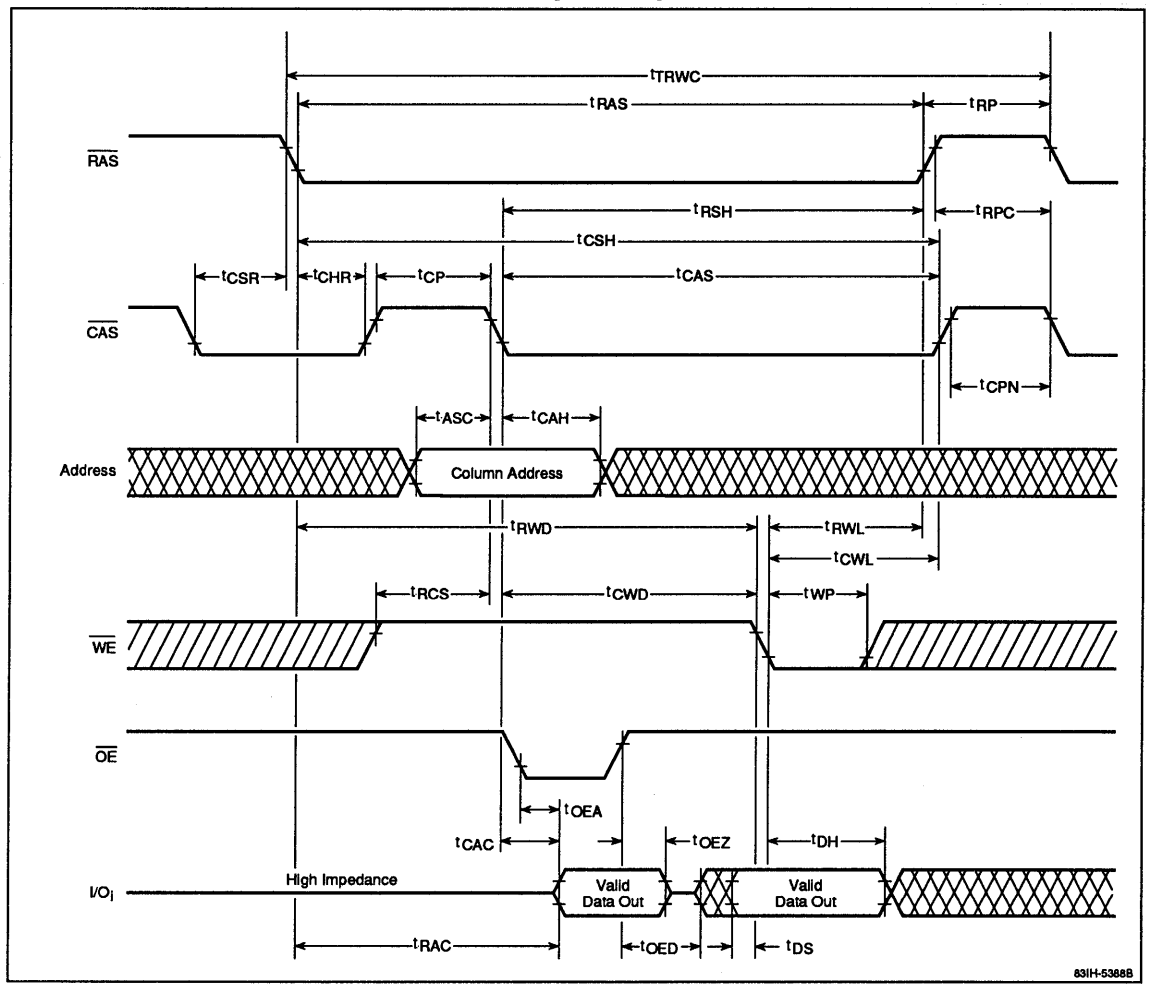
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Write Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read-Modify-Write Cycle



3b

NEC

Section 4
1M DRAMs

μPD	Organization	Features	
421000	1M x 1	Fast-page (See App Note 53.)	4a
424256	256K x 4	Fast-page	4b

μPD421000
1,048,576 x 1-Bit
Dynamic CMOS RAM

Description

The μPD421000 is a fast-page dynamic RAM organized as 1,048,576 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

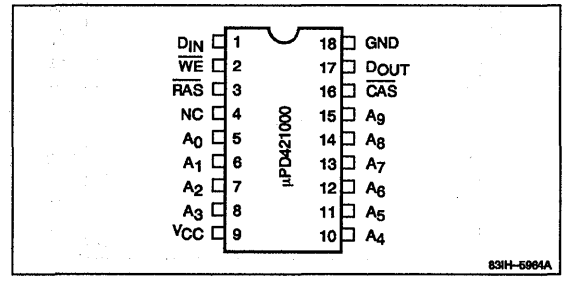
Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 - A_8 during an 8-ms refresh period.

Features

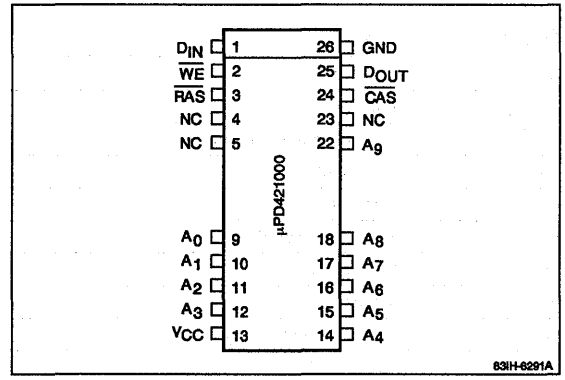
- 1,048,576-word by 1-bit organization
- Single +5-volt power supply
- Fast-page option
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- 512 refresh cycles every 8 ms
- High-density 18-pin DIP, 26/20-pin SOJ, 20-pin ZIP, or 24/20-pin TSOP plastic packaging

Pin Configurations

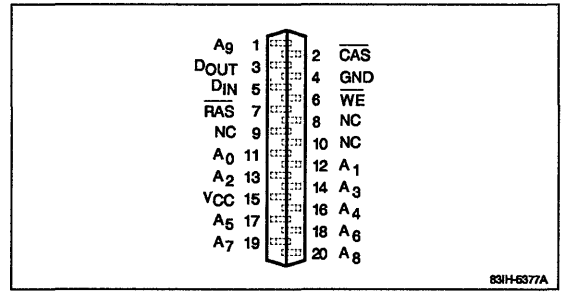
18-Pin Plastic DIP



26/20-Pin Plastic SOJ



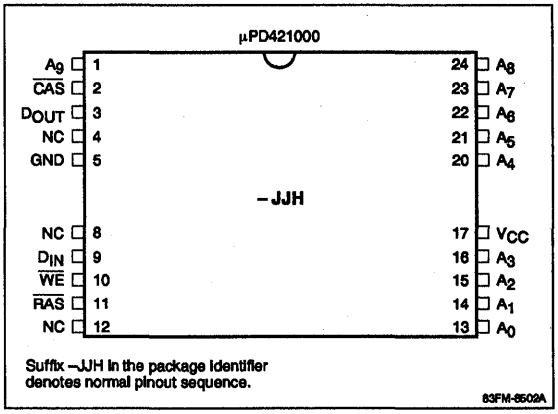
20-Pin Plastic ZIP



4a

Pin Configurations (cont)

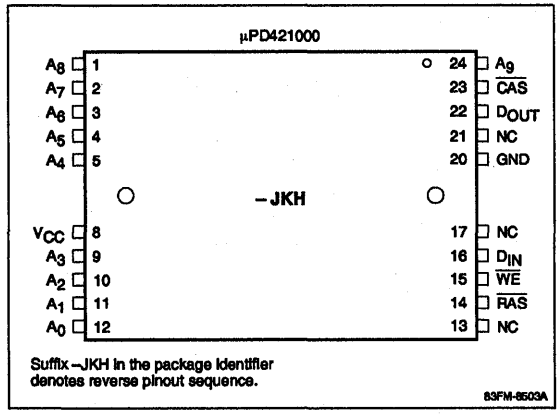
24/20-Pin Plastic TSOP (Normal Pinouts)



Suffix –JJH in the package identifier denotes normal pinout sequence.

83FM-8502A

24/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –JKH in the package identifier denotes reverse pinout sequence.

83FM-8503A

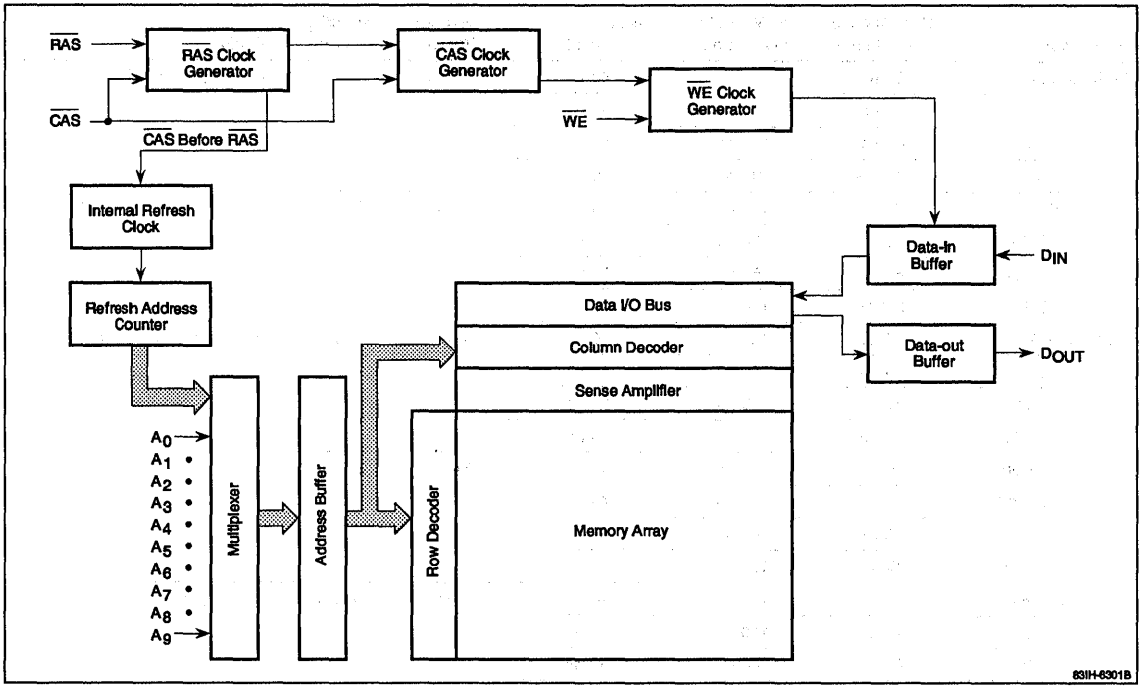
Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS}$	Column address strobe
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Refresh Period	Standby Current	Package
μPD421000C-60	60 ns	120 ns	40 ns	8 ms	1 mA	20-pin plastic DIP
C-70	70 ns	130 ns	45 ns			
C-80	80 ns	160 ns	50 ns			
C-10	100 ns	190 ns	60 ns			
μPD421000C-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
C-70L	70 ns	130 ns	45 ns			
C-80L	80 ns	160 ns	50 ns			
C-10L	100 ns	190 ns	60 ns			
μPD421000LA-60	60 ns	120 ns	40 ns	8 ms	1 mA	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	45 ns			
LA-80	80 ns	160 ns	50 ns			
LA-10	100 ns	190 ns	60 ns			
μPD421000LA-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
LA-70L	70 ns	130 ns	45 ns			
LA-80L	80 ns	160 ns	50 ns			
LA-10L	100 ns	190 ns	60 ns			
μPD421000V-60	60 ns	120 ns	40 ns	8 ms	1 mA	20-pin plastic ZIP
V-70	70 ns	130 ns	45 ns			
V-80	80 ns	160 ns	50 ns			
V-10	100 ns	190 ns	60 ns			
μPD421000V-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
V-70L	70 ns	130 ns	45 ns			
V-80L	80 ns	160 ns	50 ns			
V-10L	100 ns	190 ns	60 ns			
μPD421000GX-60	60 ns	120 ns	40 ns	8 ms	1 mA	24/20-pin plastic TSOP (normal pinouts)
GX-70	70 ns	130 ns	45 ns			
GX-80	80 ns	160 ns	50 ns			
GX-10	100 ns	190 ns	60 ns			
μPD421000GX-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
GX-70L	70 ns	130 ns	45 ns			
GX-80L	80 ns	160 ns	50 ns			
GX-10L	100 ns	190 ns	60 ns			
μPD421000GXM-60	60 ns	120 ns	40 ns	8 ms	1 mA	24/20-pin plastic TSOP (reverse pinouts)
GXM-70	70 ns	130 ns	45 ns			
GXM-80	80 ns	160 ns	50 ns			
GXM-10	100 ns	190 ns	60 ns			
μPD421000GXM-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
GXM-70L	70 ns	130 ns	45 ns			
GXM-80L	80 ns	160 ns	50 ns			
GXM-10L	100 ns	190 ns	60 ns			

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_O	7	pF	D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–10	10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}	0	0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4	V_{CC}	V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10, 13)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 13)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		70		ns	(Note 19)
Column address setup time	t_{ASC}	0		0		0	20	0	20	ns	(Note 13)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		45		50		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10, 13)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10	20	10	25	ns	(Note 13)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 14)

4a

AC Characteristics (cont)

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	(Note 19)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 17)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	10,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 15)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 15)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	145		155		190		225		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 18)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	(Note 19)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 18)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 16)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(13) For fast-page read operation, the definition of access time is as follows:

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{CAC}

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(19) This parameter is not needed for the μPD421000-60 and μPD421000-70.

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Low-Power Battery Backup (-L Versions Only)

The μPD421000-L is capable of low-power battery backup during times of reduced system power, when the input buffers and all nonessential internal circuits are turned off. For the input buffers to be turned off and the amount of leakage current flowing through them reduced, the μPD421000-L must be in standby and all control lines within 0.2 V of either V_{CC} or GND, as appropriate. When $\overline{RAS}$ and $\overline{CAS}$ are both within 0.2 V of V_{CC}, the internal circuits are inactive and power requirements reduced even further. Standby current can drop as low as 200 μA.

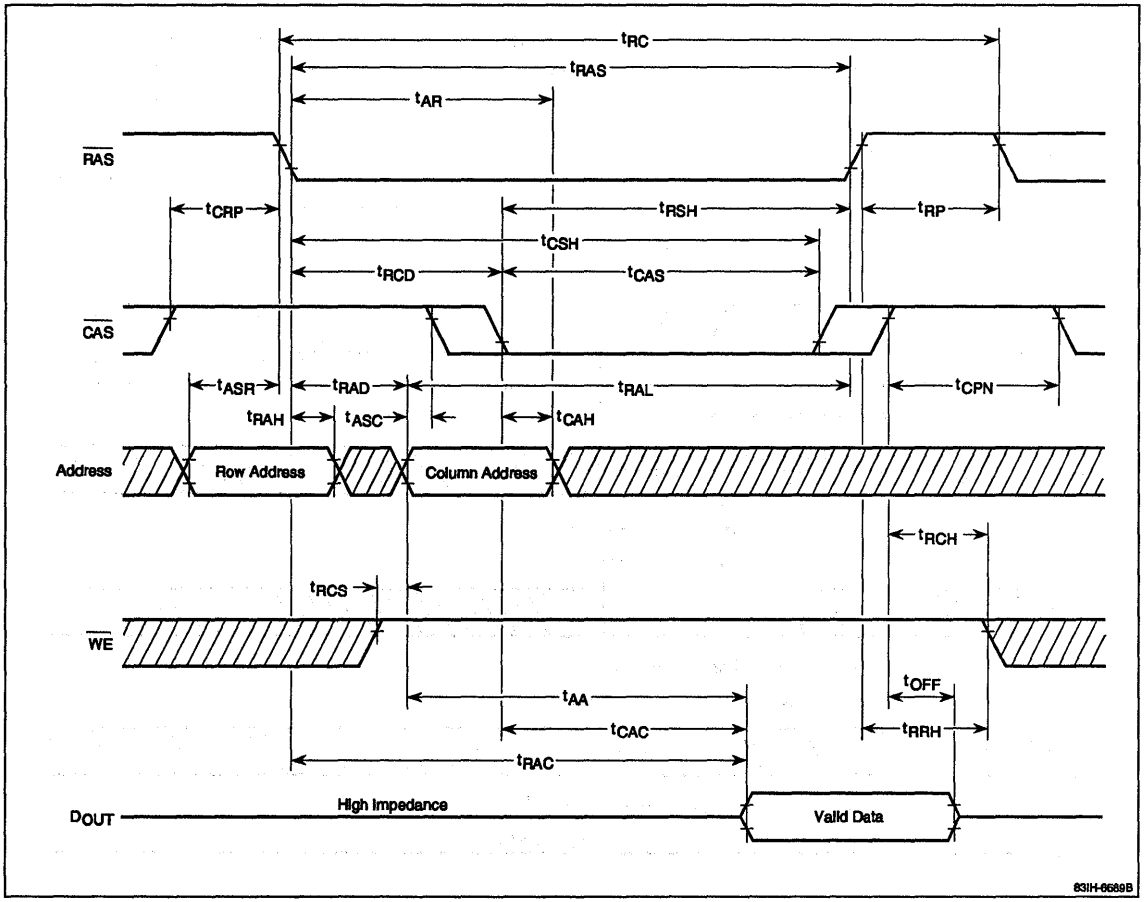
$\overline{CAS}$ before $\overline{RAS}$ refresh cycles are executed at a minimum rate to ensure that all 512 rows are refreshed only once every 64 ms. The time that $\overline{RAS}$ is low (t_{RAS}) and the μPD421000-L active needs to be as short as possible, typically less than 300 ns, to minimize power usage during refresh operation. The following table shows the conditions under which the lowest average standby current can be obtained.

Battery Backup Current

Symbol	Max	Unit	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	200	μA	$t_{RAS} \leq 300$ ns	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V; $\overline{OE} \geq V_{CC} - 0.2$ V; $\overline{WE}$ = Addresses $\geq V_{CC} - 0.2$ V or ≤ 0.2 V; $D_{IN} \geq V_{CC} - 0.2$ V or ≤ 0.2 V or high-Z
I_{CC6}	300	μA	$t_{RAS} \geq 300$ ns and ≤ 1 μs	
t_{REF}	64	ms		

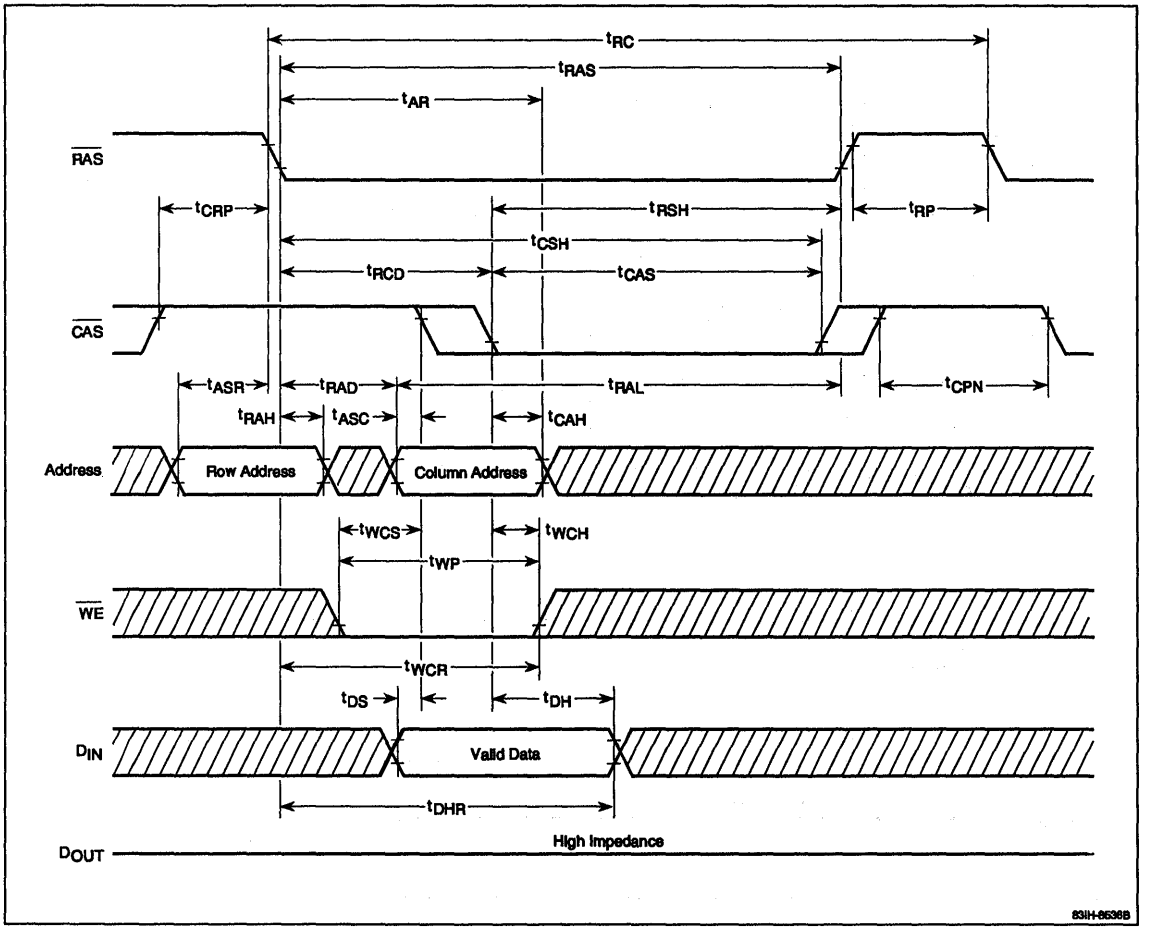
Timing Waveforms

Read Cycle



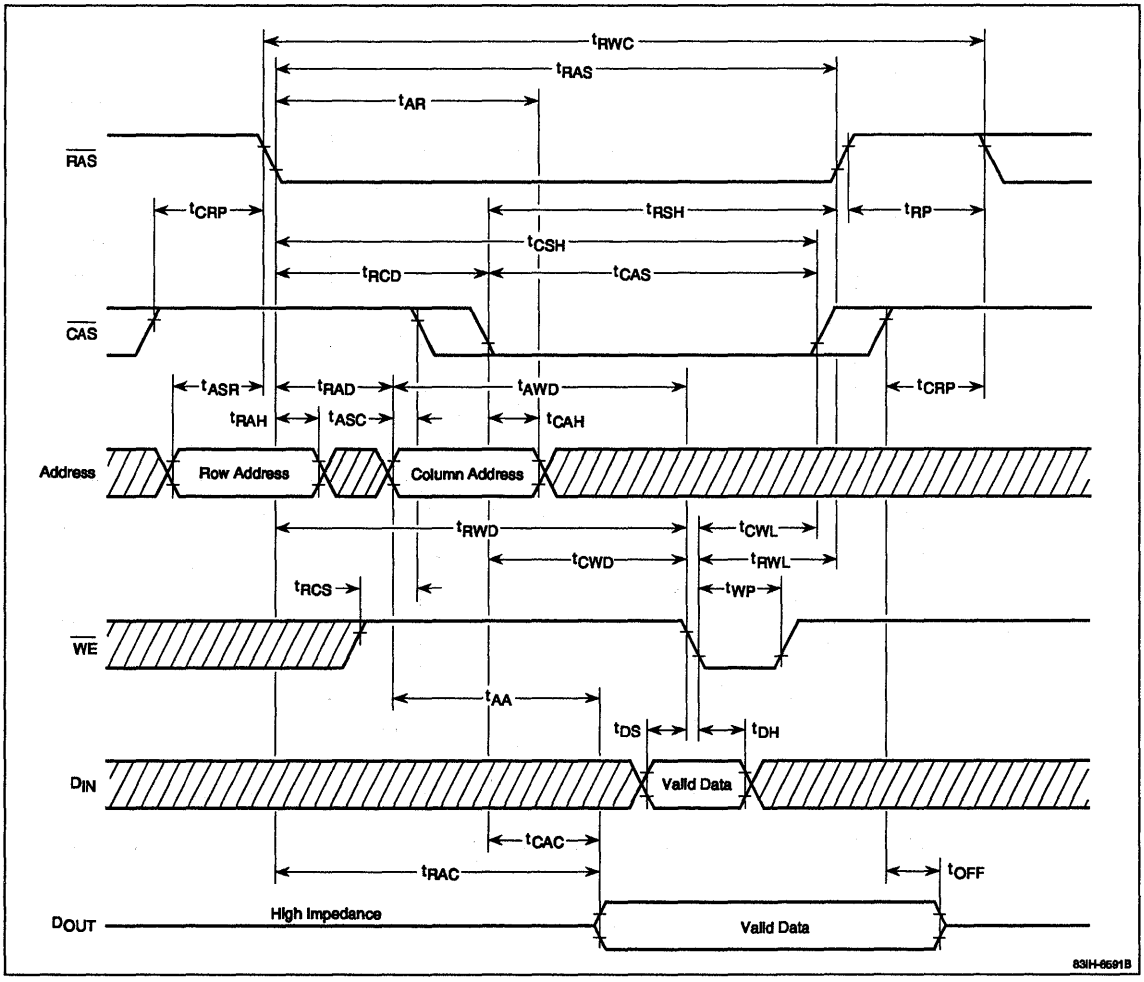
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

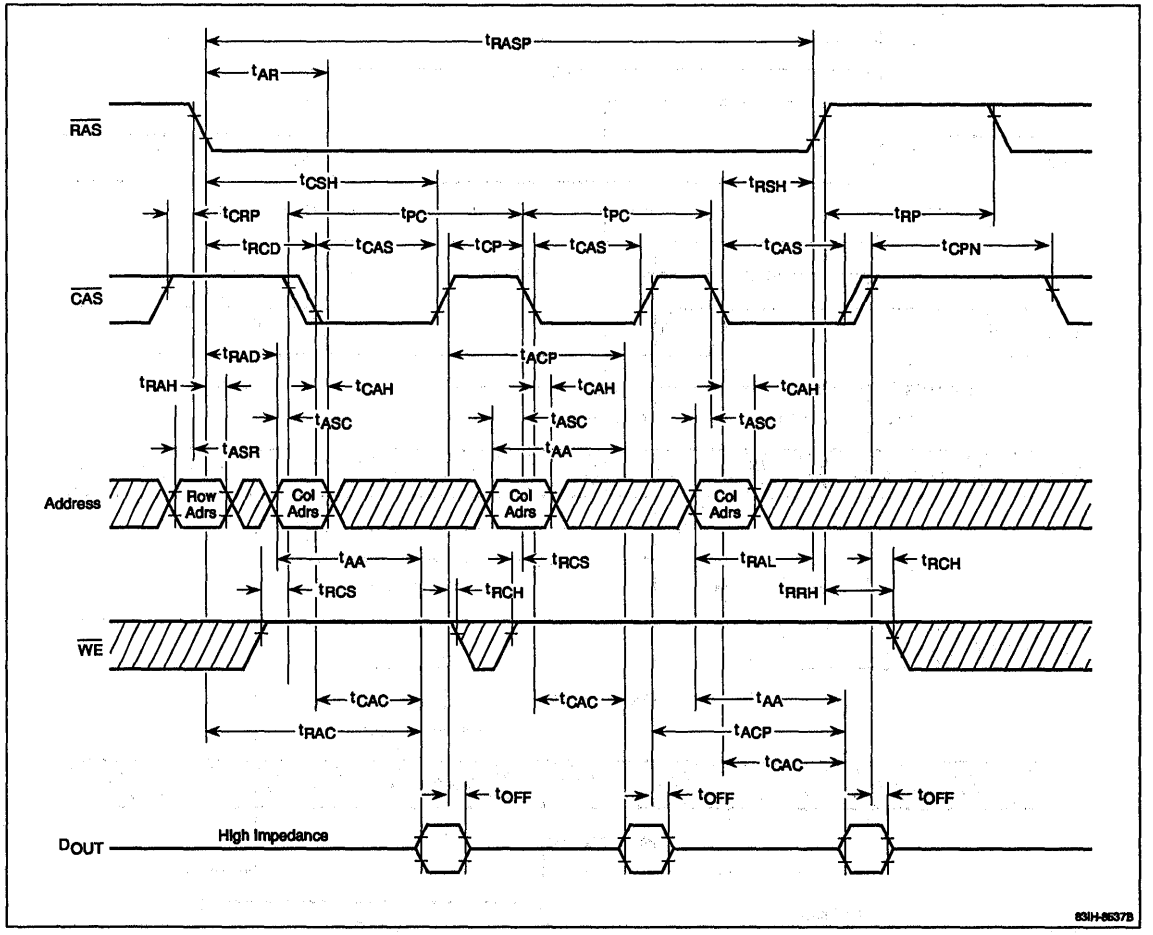
Read-Write/Read-Modify-Write Cycle



4a

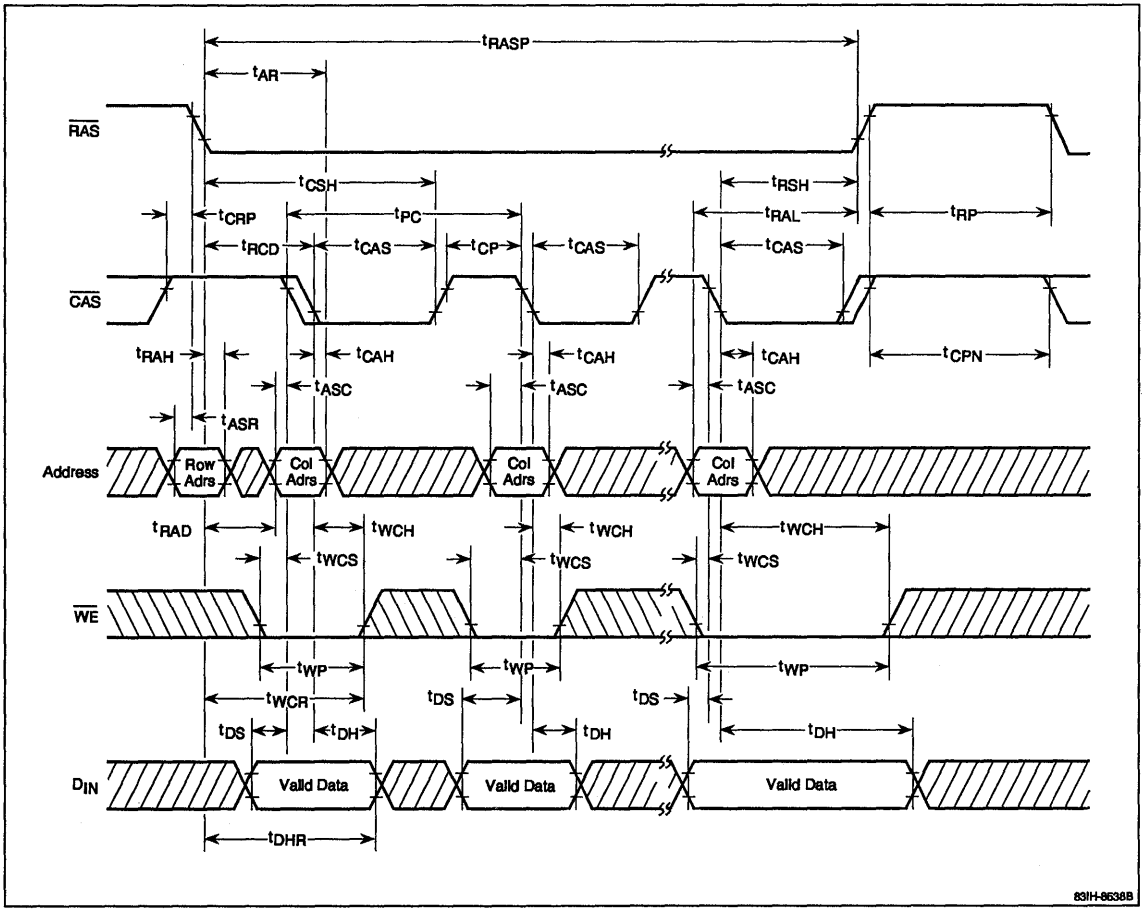
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

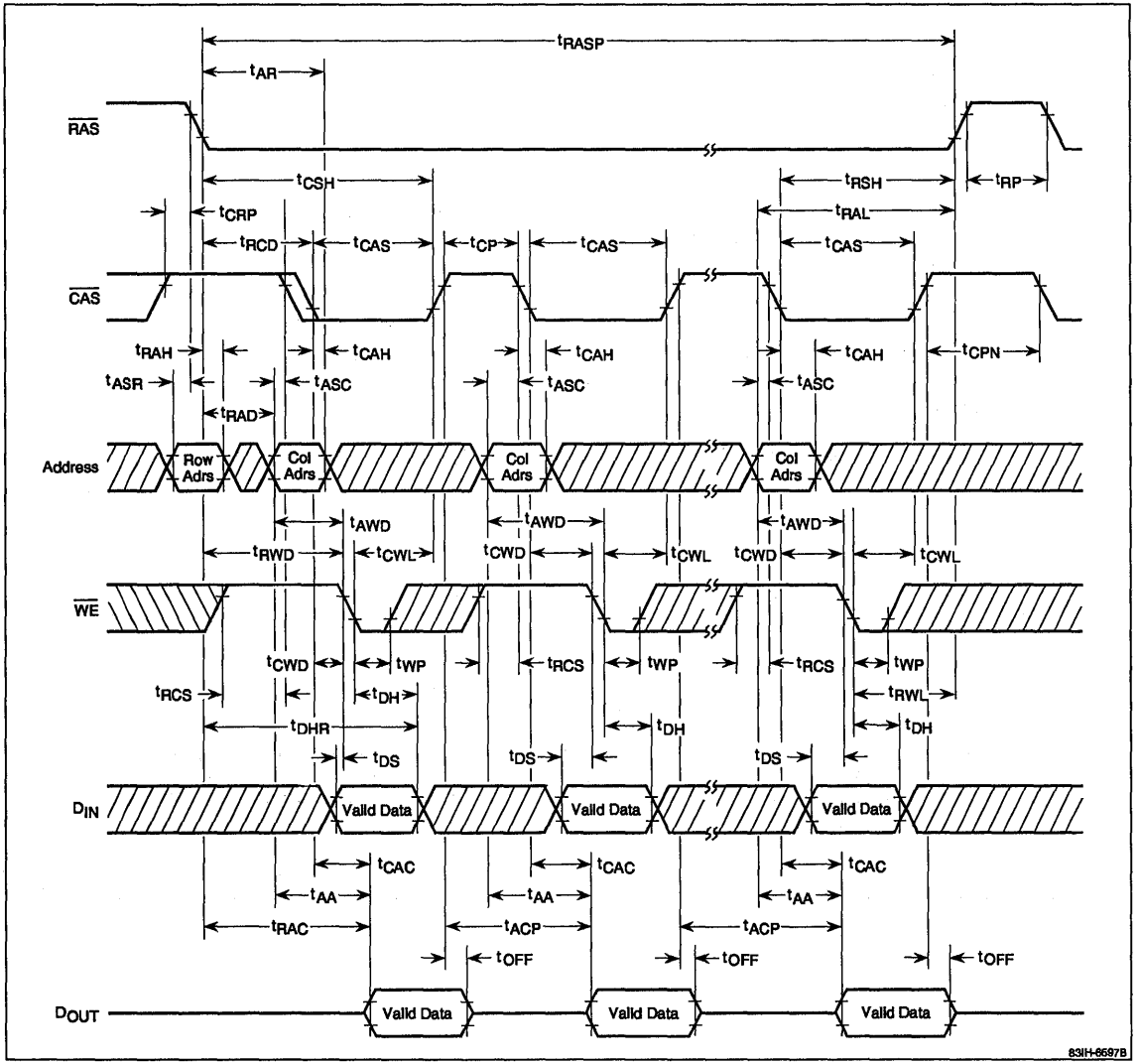
Fast-Page Early Write Cycle



4a

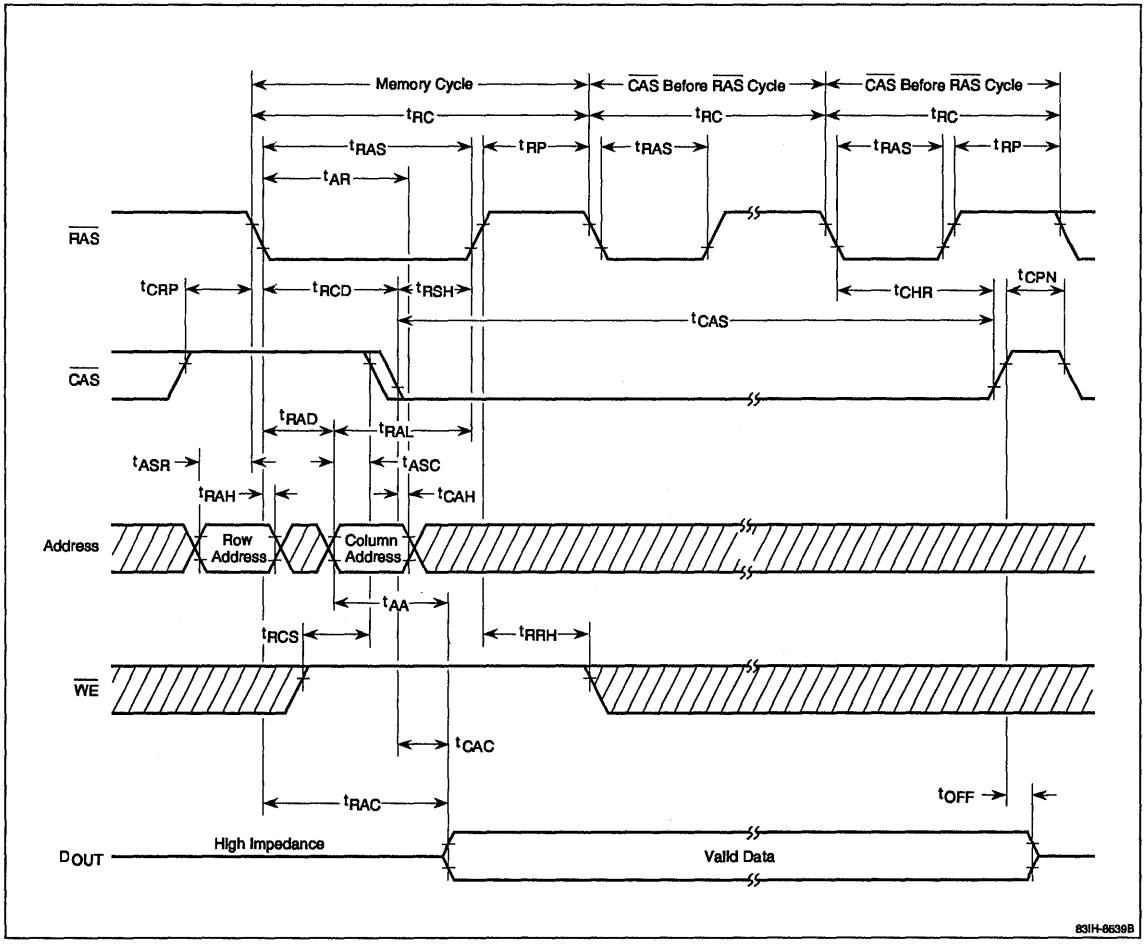
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

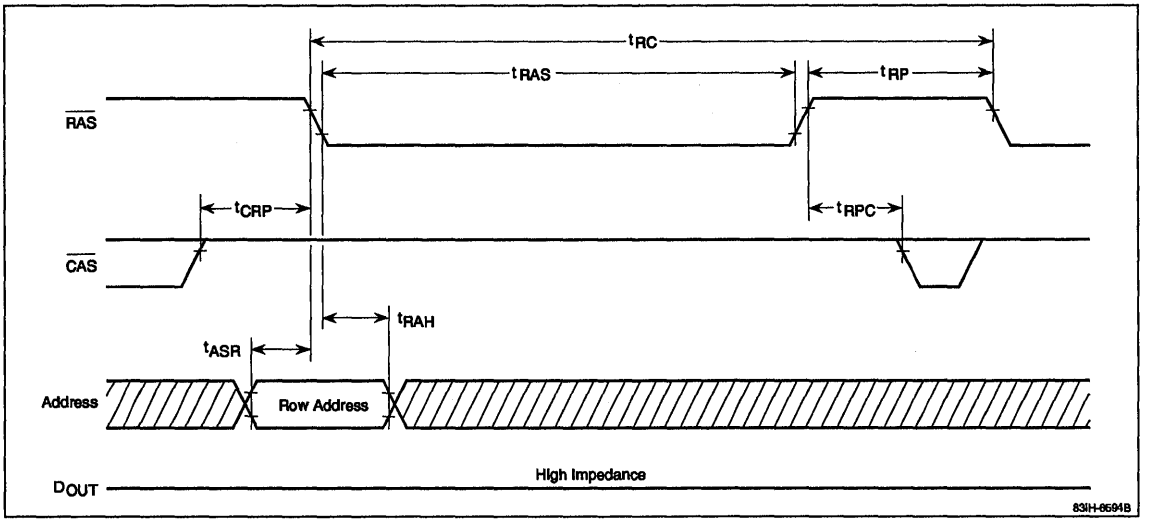
Hidden Refresh Cycle



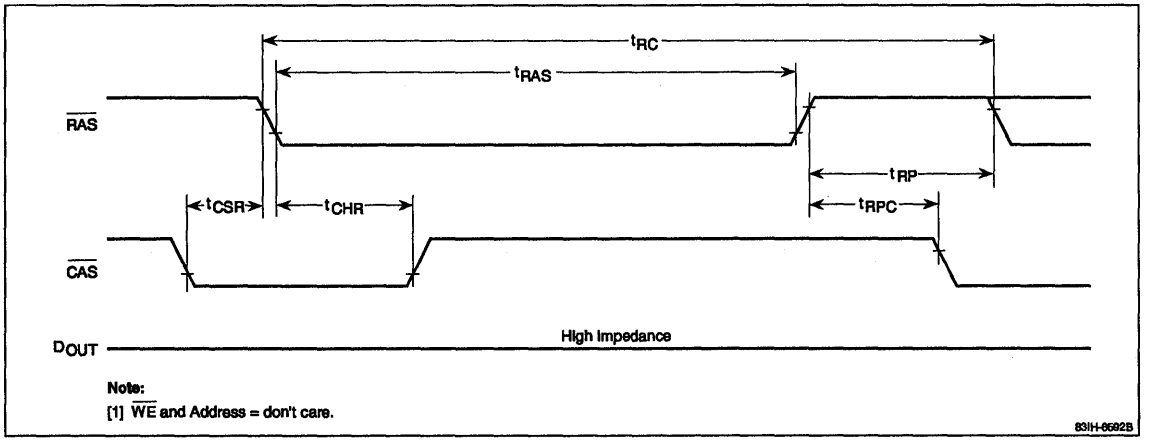
4a

Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



μPD424256
262,144 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424256 is a fast-page dynamic RAM organized as 262,144 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit generates the negative-voltage substrate bias automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. The data outputs are returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

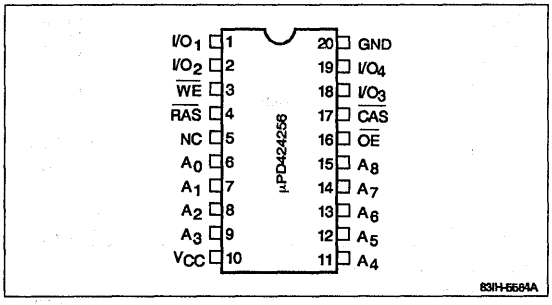
Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle whereby the refresh addresses are internally generated. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms refresh period (64 ms for -L versions).

Features

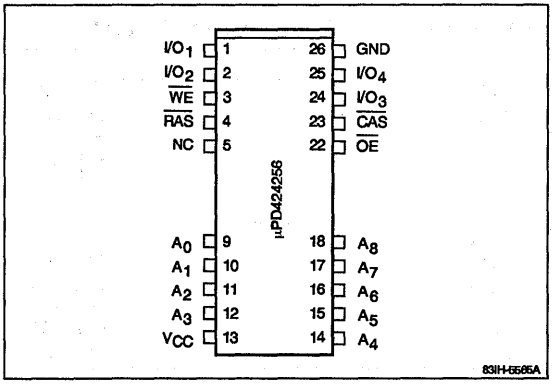
- 262,144-word by 4-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power available in -L version
- $\overline{CAS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state I/O
- TTL-compatible inputs and outputs
- High-density 20-pin DIP, 26/20-pin SOJ, 20-pin ZIP, or 24/20-pin TSOP plastic packaging

Pin Configurations

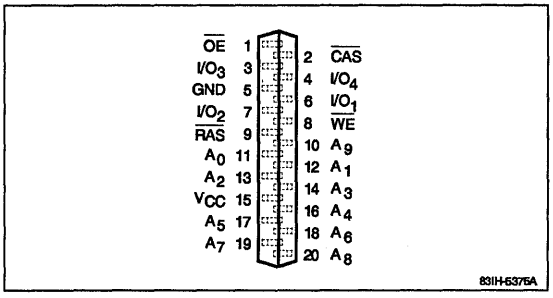
20-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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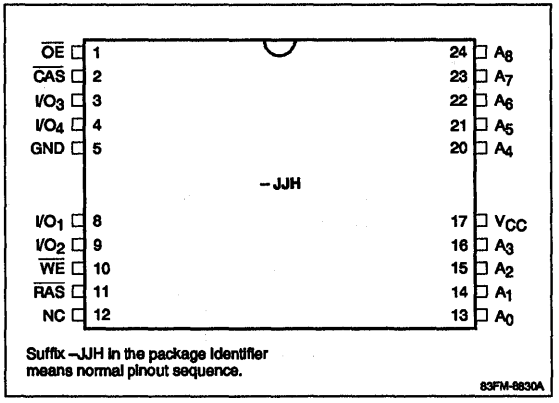
Pin Configurations (cont)

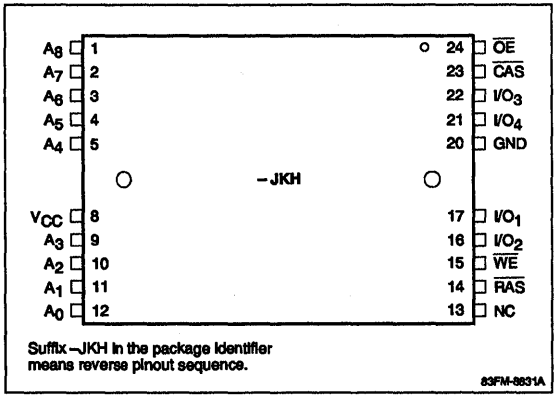
24/20-Pin Plastic TSOP (Normal Pinouts)



Suffix –JJH in the package identifier means normal pinout sequence.

83FM-8830A

24/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –JKH in the package identifier means reverse pinout sequence.

83FM-8831A

Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

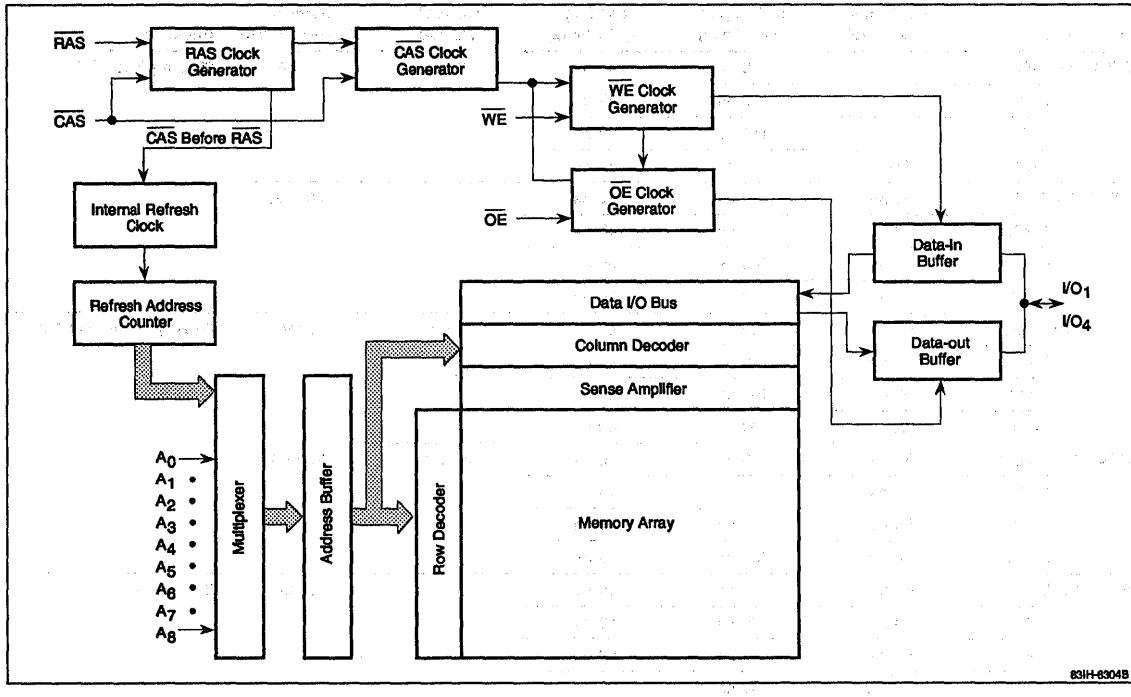
Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_{IO}	7	pF	I/O

Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Refresh Period	Standby Current (min)	Package
μPD424256C-60	60 ns	120 ns	40 ns	8 ms	1 mA	20-pin plastic DIP
C-70	70 ns	130 ns	45 ns			
C-80	80 ns	160 ns	50 ns			
C-10	100 ns	190 ns	60 ns			
μPD424256C-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
C-70L	70 ns	130 ns	45 ns			
C-80L	80 ns	160 ns	50 ns			
C-10L	100 ns	190 ns	60 ns			
μPD424256LA-60	60 ns	120 ns	40 ns	8 ms	1 mA	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	45 ns			
LA-80	80 ns	160 ns	50 ns			
LA-10	100 ns	190 ns	60 ns			
μPD424256LA-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
LA-70L	70 ns	130 ns	45 ns			
LA-80L	80 ns	160 ns	50 ns			
LA-10L	100 ns	190 ns	60 ns			
μPD424256V-60	60 ns	120 ns	40 ns	8 ms	1 mA	20-pin plastic ZIP
V-70	70 ns	130 ns	45 ns			
V-80	80 ns	160 ns	50 ns			
V-10	100 ns	190 ns	60 ns			
μPD424256V-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
V-70L	70 ns	130 ns	45 ns			
V-80L	80 ns	160 ns	50 ns			
V-10L	100 ns	190 ns	60 ns			
μPD424256GX-60	60 ns	120 ns	40 ns	8 ms	1 mA	24/20-pin plastic TSOP (normal leads)
GX-70	70 ns	130 ns	45 ns			
GX-80	80 ns	160 ns	50 ns			
GX-10	100 ns	190 ns	60 ns			
μPD424256GX-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
GX-70L	70 ns	130 ns	45 ns			
GX-80L	80 ns	160 ns	50 ns			
GX-10L	100 ns	190 ns	60 ns			
μPD424256GXM-60	60 ns	120 ns	40 ns	8 ms	1 mA	24/20-pin plastic TSOP (reverse bent leads)
GXM-70	70 ns	130 ns	45 ns			
GXM-80	80 ns	160 ns	50 ns			
GXM-10	100 ns	190 ns	60 ns			
μPD424256GXM-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
GXM-70L	70 ns	130 ns	45 ns			
GXM-80L	80 ns	160 ns	50 ns			
GXM-10L	100 ns	190 ns	60 ns			

4b

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70 °C; V_{CC} = +5.0V ±10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IL}; t_{RC} = t_{RC} min; (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10, 13)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 13)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		70		ns	
Column address setup time	t_{ASC}	0		0		0	20	0	20	ns	(Note 13)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		80		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10, 13)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10	15	10	20	10	25	ns	(Note 13)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 14)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		55		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 17)

4b

AC Characteristics (cont)

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 17)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Fast-page read-write cycle time	t_{PRWC}	85		90		105		125		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 15)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8; 64 ms for -L versions
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 15)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	165		175		215		255		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		130		ns	(Note 18)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 18)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 16)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(12) Operation with the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(13) For fast-page read operation, the definition of access time is as follows:

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq$ CP (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq$ CP (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq$ CP (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

Low Power Battery Backup (-L Versions Only)

The μPD424256-L is capable of low power battery backup during times of reduced system power, when the input buffers and all nonessential internal circuits are turned off. For the input buffers to be turned off and the amount of leakage current flowing through them reduced, the μPD424256-L must be in standby and all control lines within 0.2 V of either V_{CC} or GND, as appropriate. When $\overline{RAS}$ and $\overline{CAS}$ are both within 0.2 V of V_{CC}, the internal circuits are inactive and power requirements reduced even further. Standby current can drop as low as 200 μA.

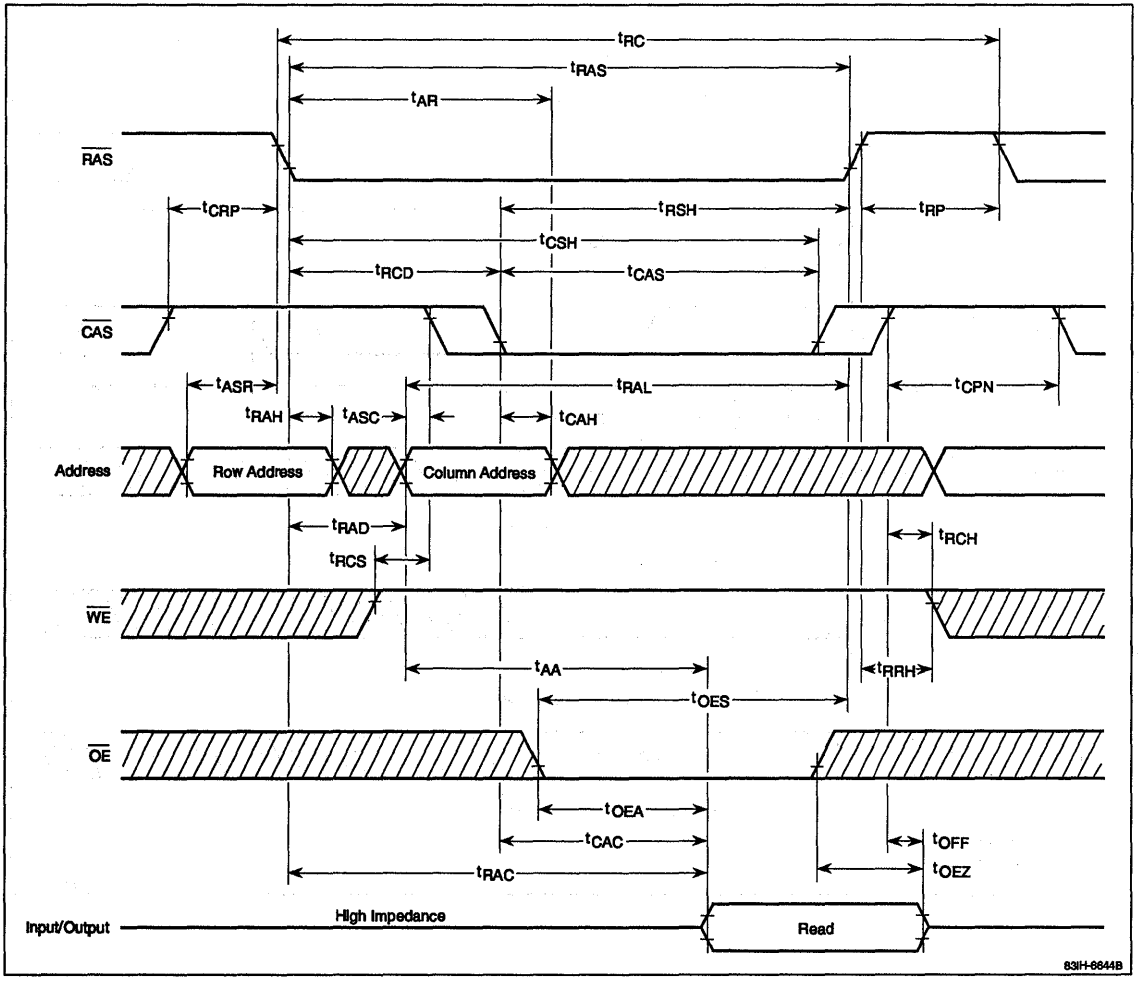
$\overline{CAS}$ before $\overline{RAS}$ refresh cycles are executed at a minimum rate to ensure that all 512 rows are refreshed only once every 64 ms. The time that $\overline{RAS}$ is low (t_{RAS}) and the μPD424256-L active needs to be as short as possible, typically less than 300 ns, to minimize power usage during refresh operation. The following table shows the conditions under which the lowest average standby current can be obtained.

Battery Backup Current

Symbol	Max	Unit	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	200	μA	$t_{RAS} \leq 300$ ns	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V; $\overline{OE} \geq V_{CC} - 0.2$ V; $\overline{WE}$ = Addresses $\geq V_{CC} - 0.2$ V or ≤ 0.2 V; I/O $\geq V_{CC} - 0.2$ V or ≤ 0.2 V or high-Z
I_{CC6}	300	μA	$t_{RAS} \geq 300$ ns and ≤ 1 μs	

Timing Waveforms

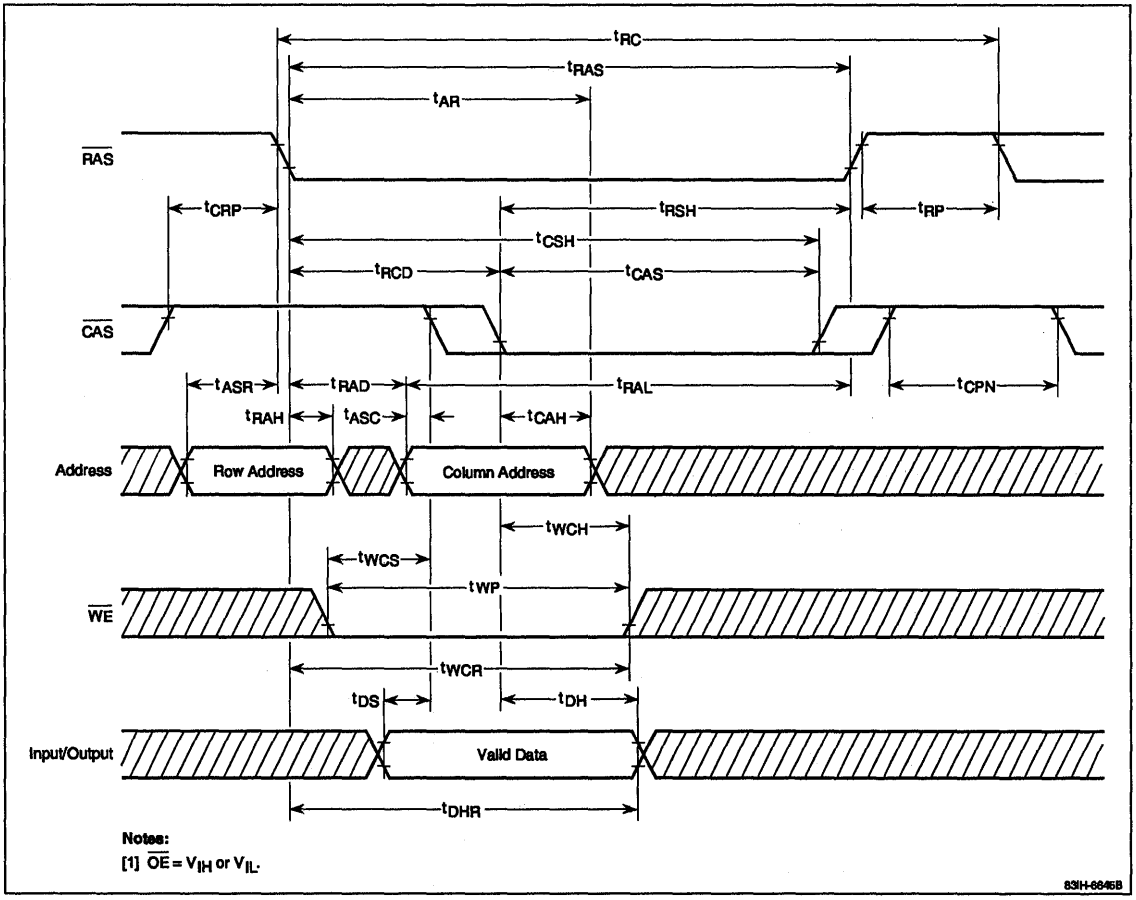
Read Cycle



4b

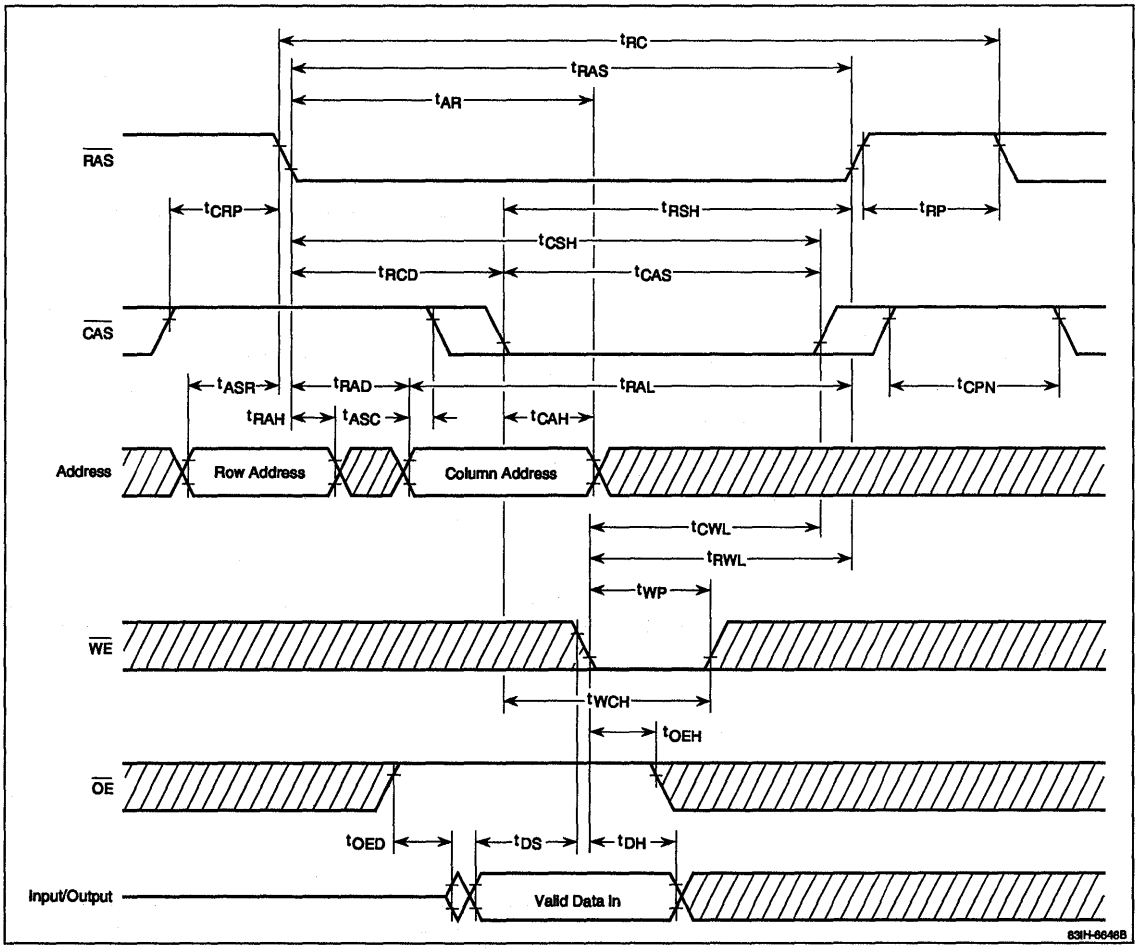
Timing Waveforms (cont)

Early Write Cycle



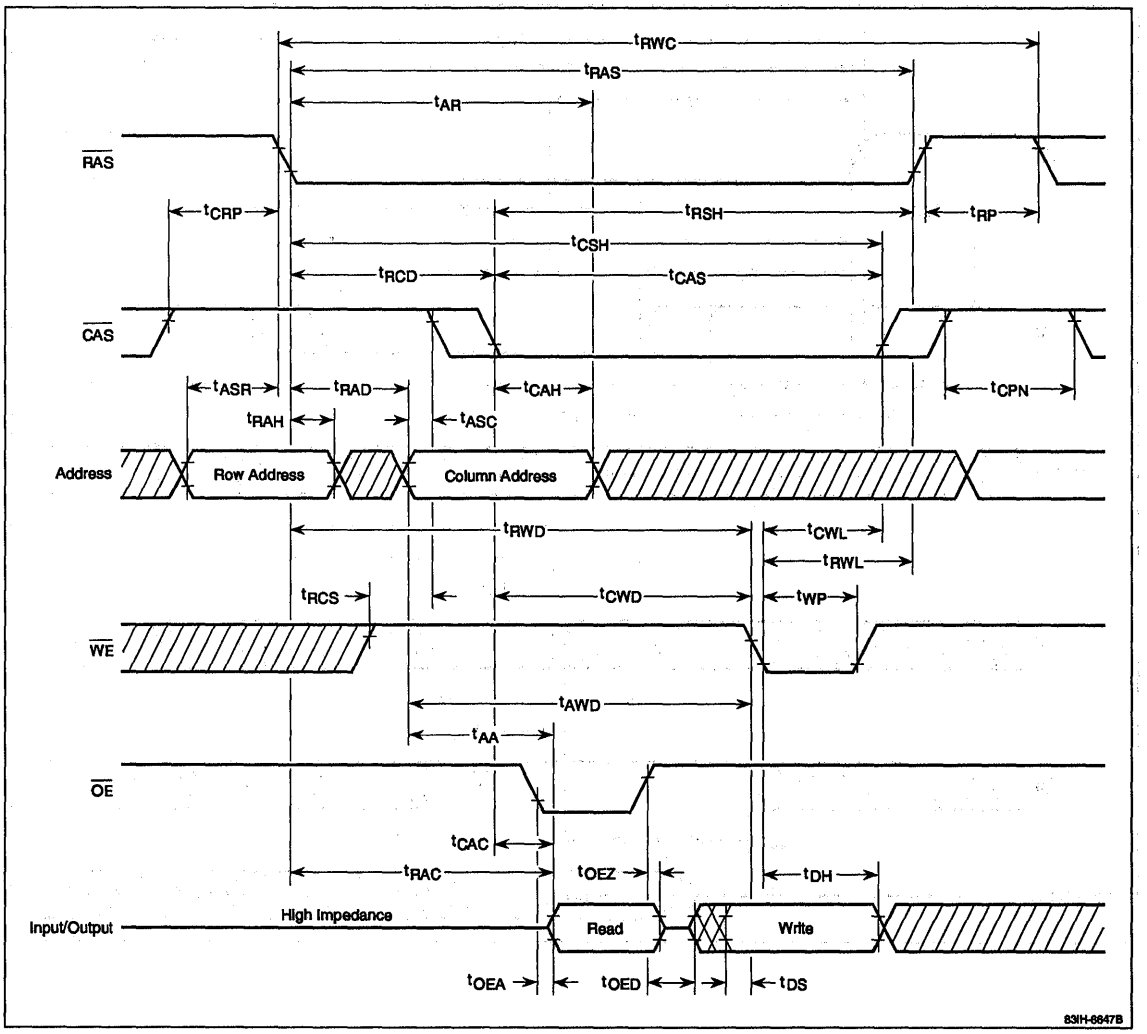
Timing Waveforms (cont)

$\overline{OE}$-Controlled Write Cycle



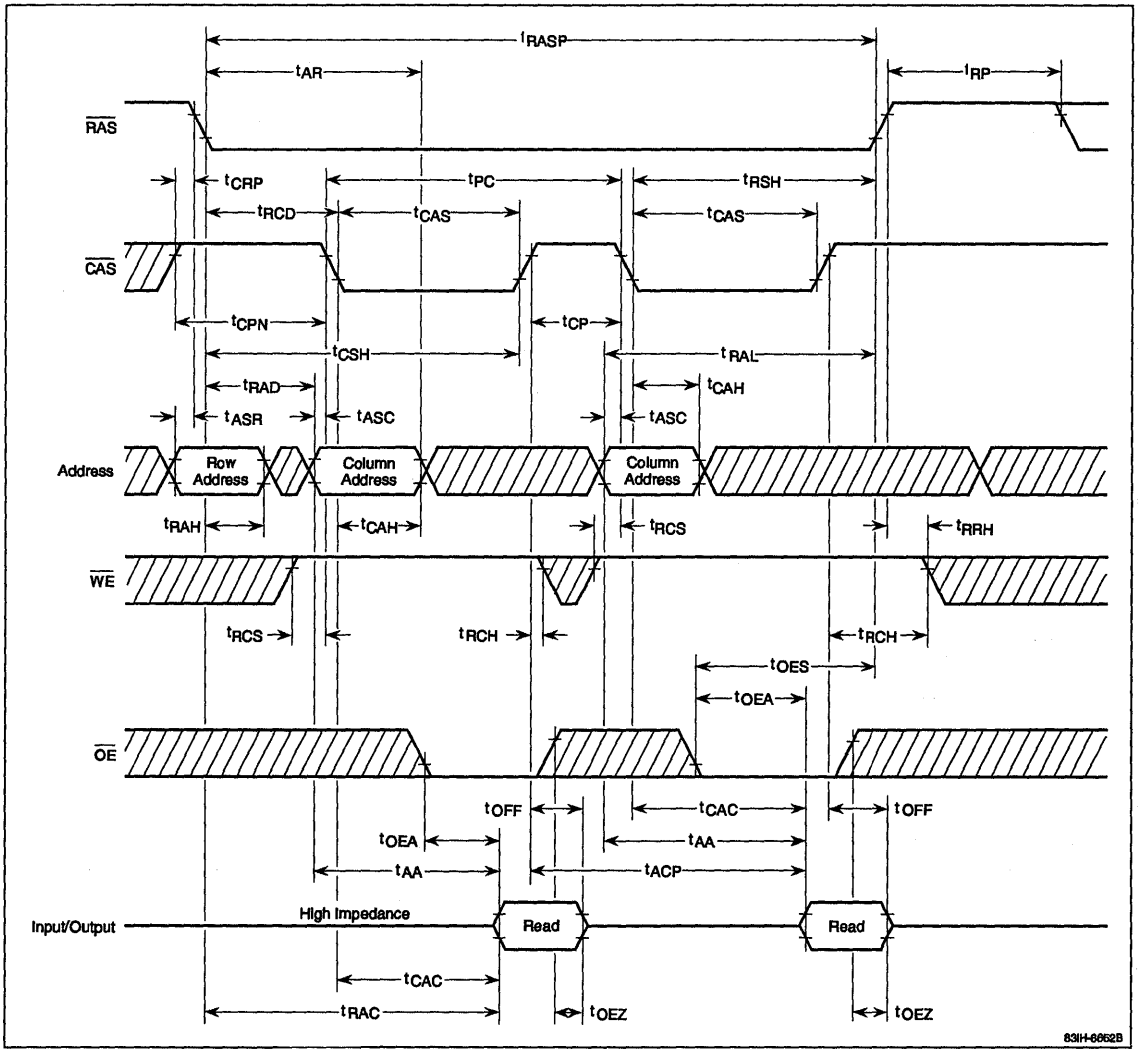
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

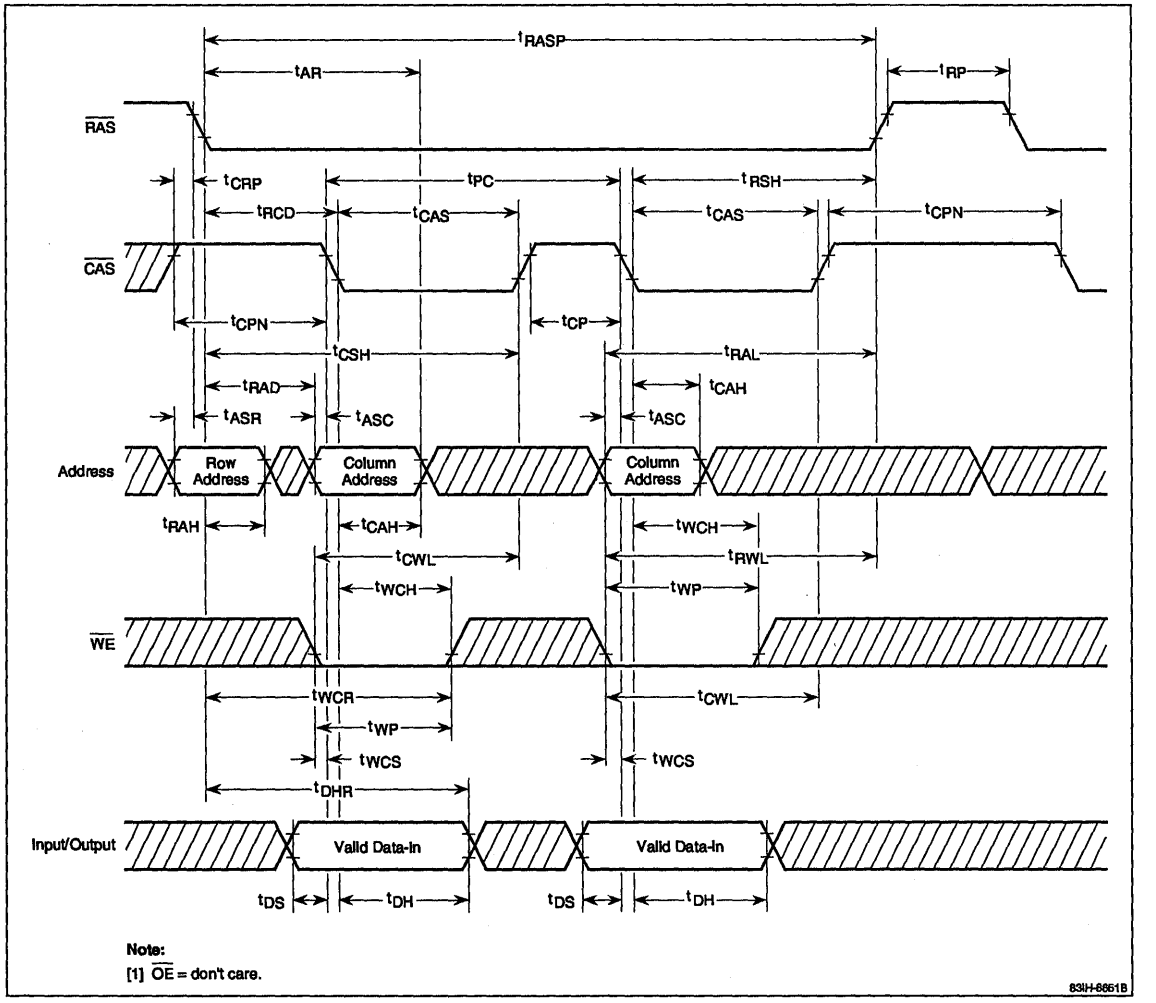
Fast-Page Read Cycle



4b

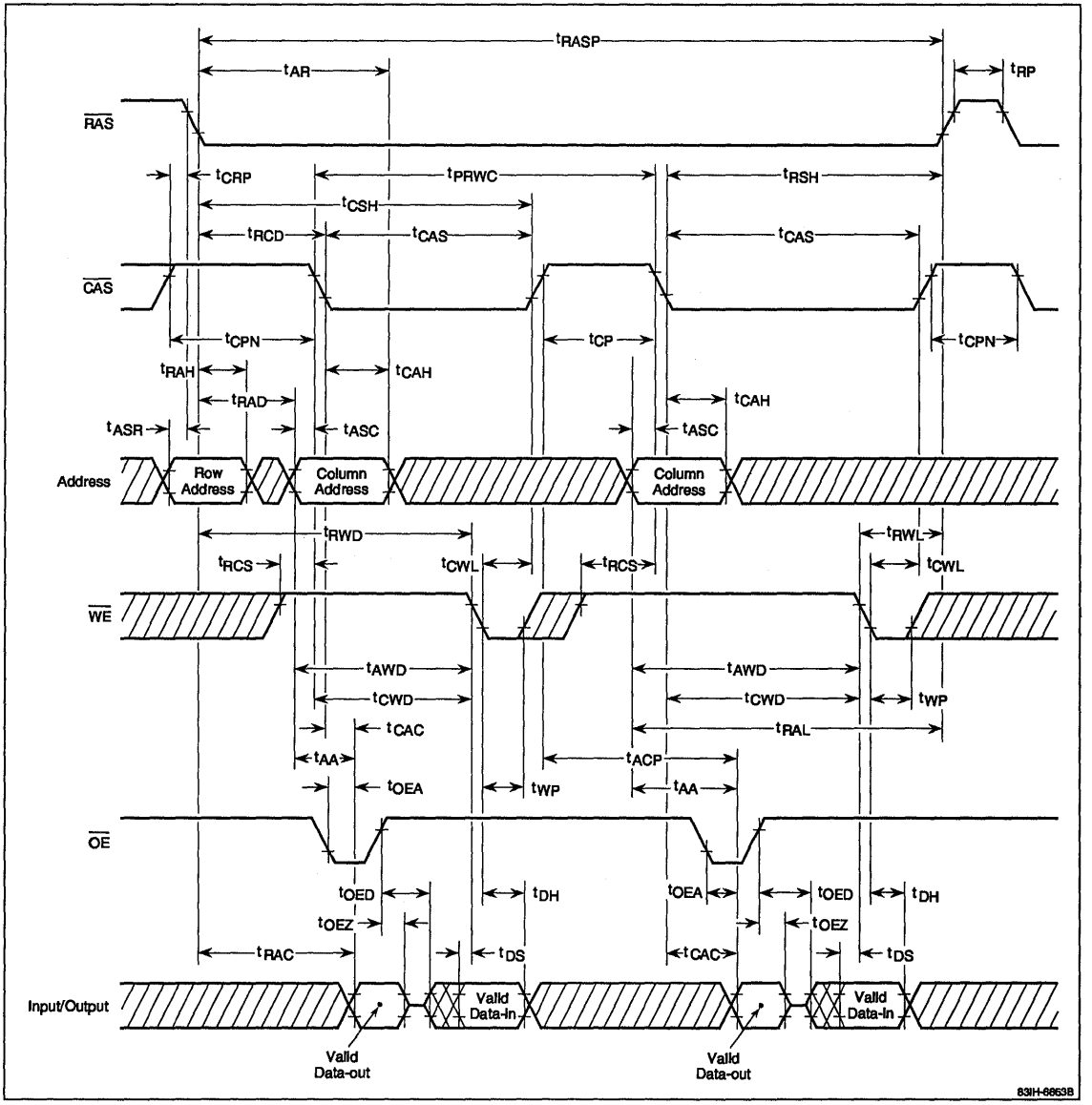
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

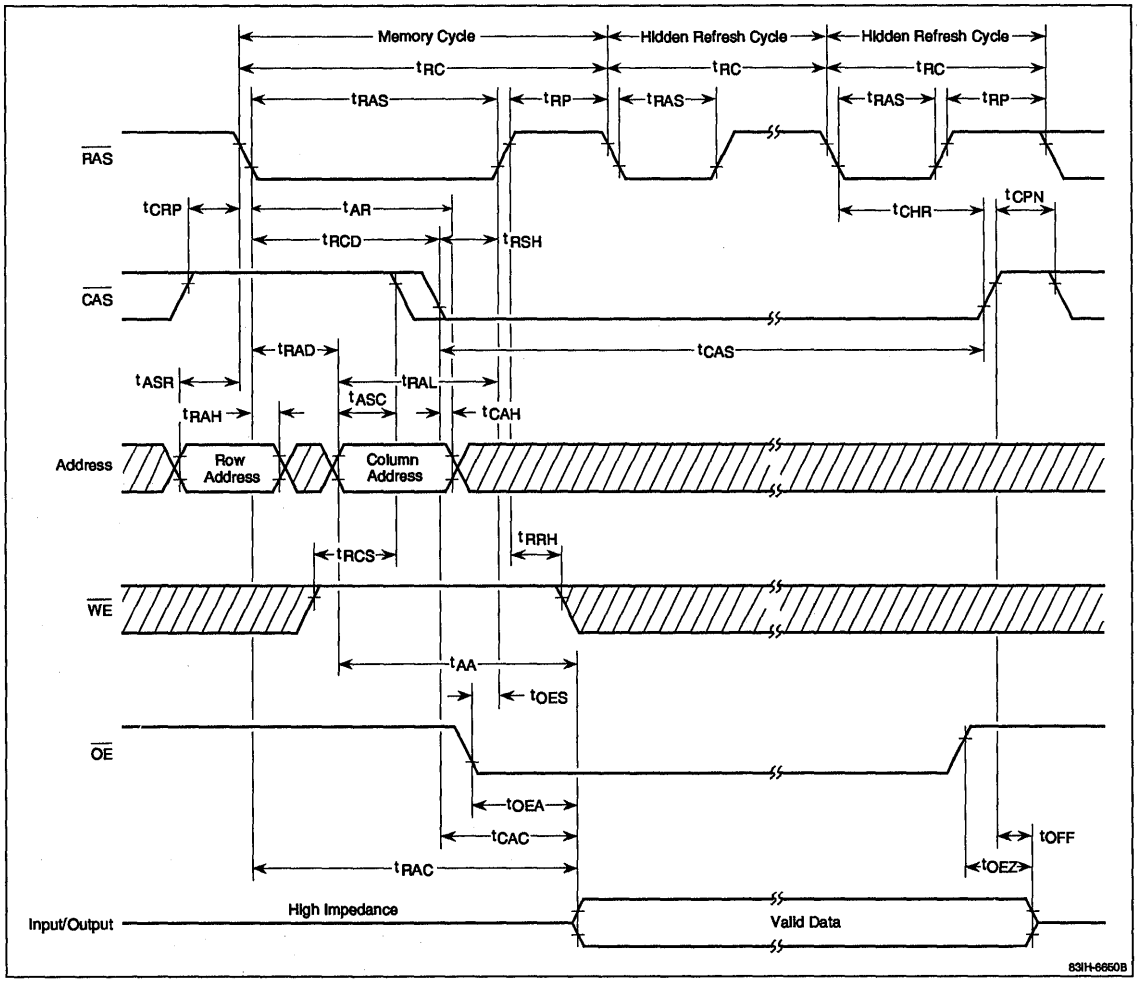
Fast-Page Read-Write/Read-Modify-Write Cycle



4b

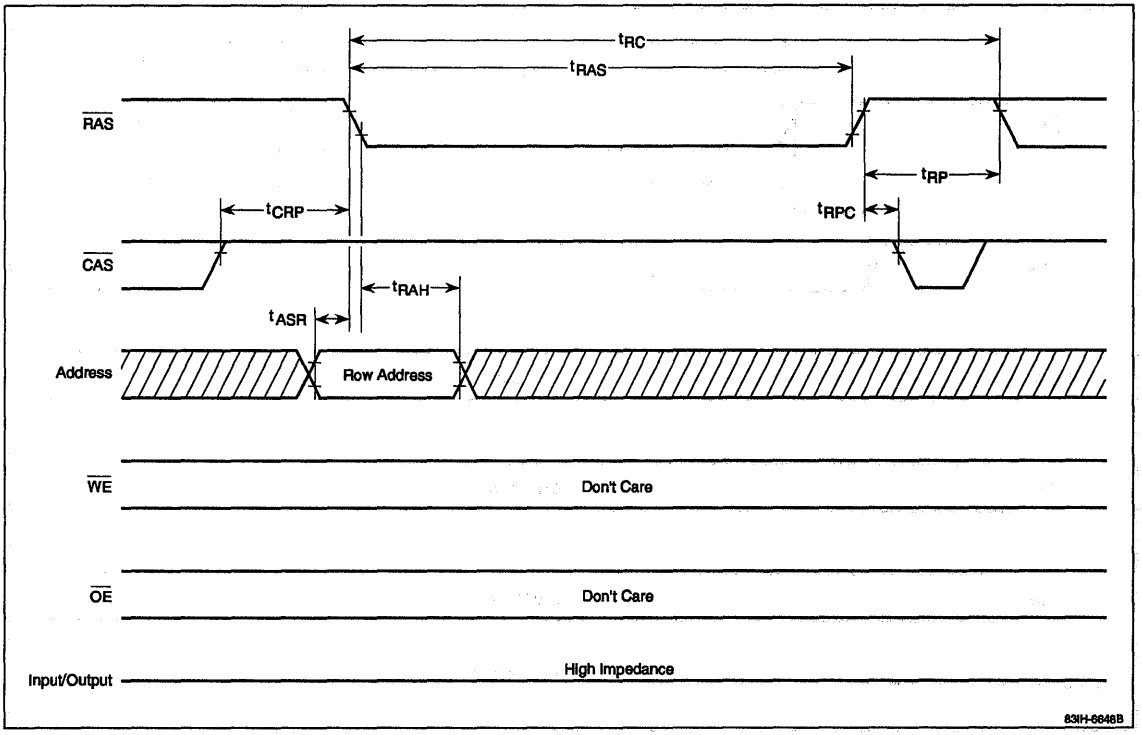
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

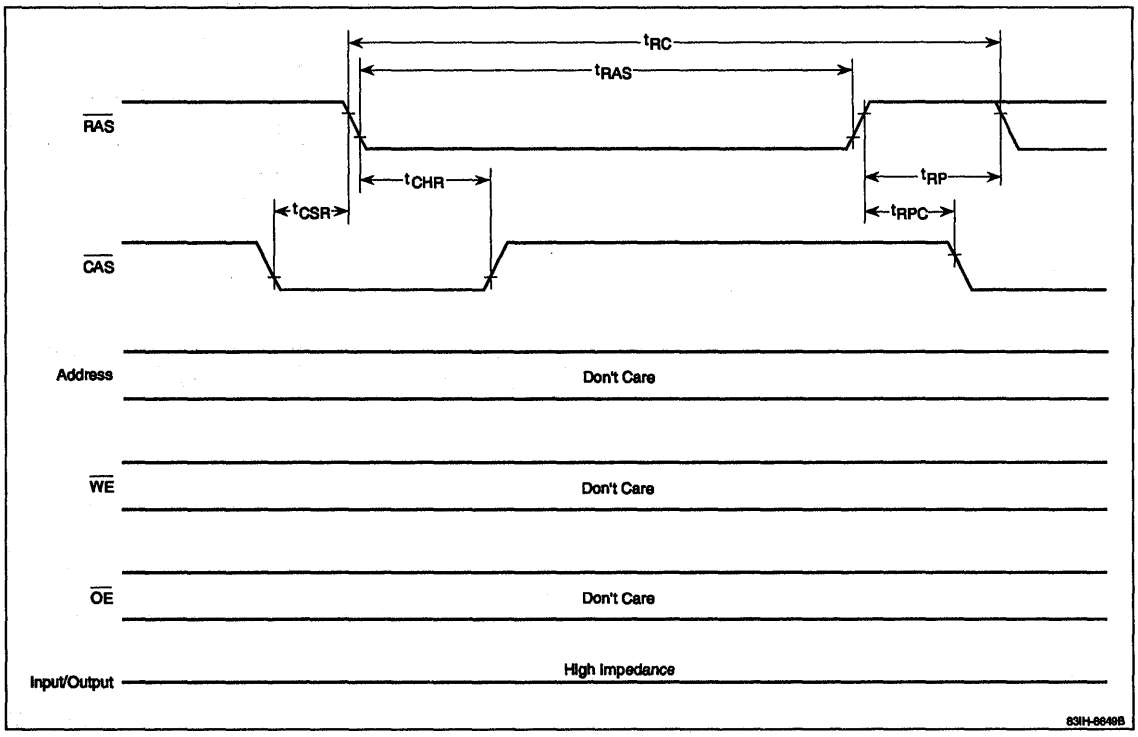
$\overline{RAS}$-Only Refresh Cycle



4b

Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



NEC

Section 5
4M DRAMs (4M x 1 and 1M x 4)

μPD	Organization	Features	
424100	4M x 1	Fast-page	5a
424100A	4M x 1	Fast-page	
424100L	4M x 1	Fast-page; 3.3-volt	
42S4100A	4M x 1	Fast-page; self-refresh	
42S4100L	4M x 1	Fast-page; self-refresh; 3.3-volt	
424101	4M x 1	Nibble	5b
424102	4M x 1	Static-column	5c
424400	1M x 4	Fast-page	5d
424400A	1M x 4	Fast-page	
424400L	1M x 4	Fast-page; 3.3-volt	
42S4400A	1M x 4	Fast-page; self-refresh	
42S4400L	1M x 4	Fast-page; self-refresh; 3.3-volt	
424402	1M x 4	Static-column	5e
424410	1M x 4	Fast-page; write-per-bit	5f
424412	1M x 4	Static-column; write-per-bit	5g
424440	1M x 4	Fast-page; 4 $\overline{\text{CAS}}$	5h
424440L	1M x 4	Fast-page; 4 $\overline{\text{CAS}}$; 3.3-volt	
42S4440	1M x 4	Fast-page; 4 $\overline{\text{CAS}}$: self-refresh	
42S4440L	1M x 4	Fast-page; 4 $\overline{\text{CAS}}$; self-refresh; 3.3-volt	

μPD424100, 424100A/L, 42S4100A/L
4,194,304 x 1-Bit
Dynamic CMOS RAM

Description

The devices listed below are fast-page dynamic RAMs organized as 4,194,304 words by 1 bit and designed to operate from a single power supply.

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
Second-generation products	
424100-xx	+5 V
424100-xxL	+5 V; low-power
Third-generation products	
424100A-xx	+5 V
42S4100A-xx	+5 V; self-refresh, low-power
424100L-Axx	+3.3 V
42S4100L-Axx	+3.3 V; self-refresh, low-power

-xx indicates speed grade (RAS access time).

Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by maintaining $\overline{CAS}$ low. The data output returns to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1024 address combinations of A_0 - A_9 during a 16-ms refresh period.

The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

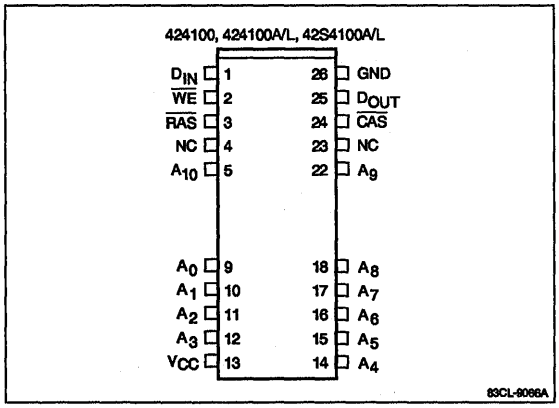
- 4,194,304 by 1-bit organization
- Single +5- or +3.3-volt power supply
- Fast-page option
- Self-refresh option (slow internal automatic refresh)
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- 26/20-pin SOJ, 20-pin ZIP, and 26/20-pin TSOP plastic packaging

Pin Identification

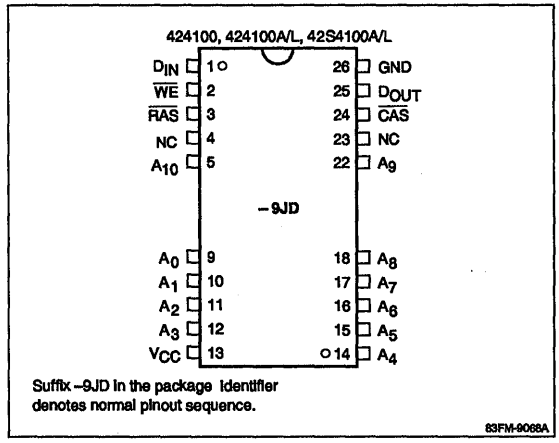
Name	Function
A_0 - A_{10}	Address inputs
$\overline{CAS}$	Column address strobe
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configurations

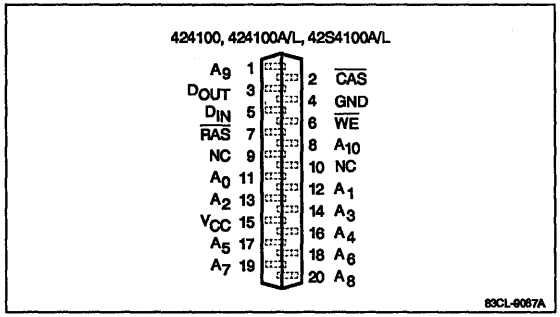
26/20-Pin Plastic SOJ



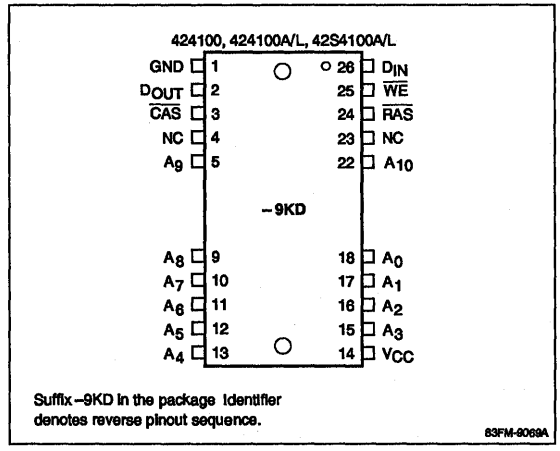
26/20-Pin Plastic TSOP (Normal Pinouts)



20-Pin Plastic ZIP



26/20-Pin Plastic TSOP (Reverse Pinouts)



Ordering Information, μPD424100 (+ 5 V; standard version; 2nd generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Power Option	Package
μPD424100LA-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic SOJ (300-mil)
LA-70	70 ns	140 ns	45 ns		
LA-80	80 ns	160 ns	50 ns		
LA-10	100 ns	190 ns	60 ns		
μPD424100LA-60L	60 ns	120 ns	40 ns	Low-power	
LA-70L	70 ns	140 ns	45 ns		
LA-80L	80 ns	160 ns	50 ns		
LA-10L	100 ns	190 ns	60 ns		
μPD424100V-60	60 ns	120 ns	40 ns	Standard	20-pin plastic ZIP
V-70	70 ns	140 ns	45 ns		
V-80	80 ns	160 ns	50 ns		
V-10	100 ns	190 ns	60 ns		
μPD424100V-60L	60 ns	120 ns	40 ns	Low-power	
V-70L	70 ns	140 ns	45 ns		
V-80L	80 ns	160 ns	50 ns		
V-10L	100 ns	190 ns	60 ns		
μPD424100GS-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic TSOP (normal pinouts)
GS-70	70 ns	140 ns	45 ns		
GS-80	80 ns	160 ns	50 ns		
μPD424100GS-60L	60 ns	120 ns	40 ns	Low-power	
GS-70L	70 ns	140 ns	45 ns		
GS-80L	80 ns	160 ns	50 ns		
μPD424100GSM-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic TSOP (reverse pinouts))
GSM-70	70 ns	140 ns	45 ns		
GSM-80	80 ns	160 ns	50 ns		
μPD424100GSM-60L	60 ns	120 ns	40 ns	Low-power	
GSM-70L	70 ns	140 ns	45 ns		
GSM-80L	80 ns	160 ns	50 ns		

Ordering Information, μPD424100A (+ 5 V; standard version; 3rd-generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD424100ALA-50	50 ns	100 ns	35 ns	26/20-pin plastic SOJ (300-mil)
LA-60	60 ns	120 ns	40 ns	
LA-70	70 ns	140 ns	45 ns	
LA-80	80 ns	160 ns	50 ns	
μPD424100AV-50	50 ns	100 ns	35 ns	20-pin plastic ZIP
V-60	60 ns	120 ns	40 ns	
V-70	70 ns	140 ns	45 ns	
V-80	80 ns	160 ns	50 ns	
μPD424100AGS-50	50 ns	100 ns	35 ns	26/20-pin plastic TSOP (normal pinouts)
GS-60	60 ns	120 ns	40 ns	
GS-70	70 ns	140 ns	45 ns	
GS-80	80 ns	160 ns	50 ns	
μPD424100AGSM-50	50 ns	100 ns	35 ns	26/20-pin plastic TSOP (reverse pinouts)
GSM-60	60 ns	120 ns	40 ns	
GSM-70	70 ns	140 ns	45 ns	
GSM-80	80 ns	160 ns	50 ns	

Ordering Information, μPD42S4100A (+ 5 V; self-refresh, low-power version; 3rd-generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Self-Refresh Current (max)	Package
μPD42S4100ALA-50	50 ns	100 ns	35 ns	200 μA	26/20-pin plastic SOJ (300-mil)
LA-60	60 ns	120 ns	40 ns		
LA-70	70 ns	140 ns	45 ns		
LA-80	80 ns	160 ns	50 ns		
μPD42S4100AV-50	50 ns	100 ns	35 ns	200 μA	20-pin plastic ZIP
V-60	60 ns	120 ns	40 ns		
V-70	70 ns	140 ns	45 ns		
V-80	80 ns	160 ns	50 ns		
μPD42S4100AGS-50	50 ns	100 ns	35 ns	200 μA	26/20-pin plastic TSOP (normal pinouts)
GS-60	60 ns	120 ns	40 ns		
GS-70	70 ns	140 ns	45 ns		
GS-80	80 ns	160 ns	50 ns		
μPD42S4100AGSM-50	50 ns	100 ns	35 ns	200 μA	26/20-pin plastic TSOP (reverse pinouts)
GSM-60	60 ns	120 ns	40 ns		
GSM-70	70 ns	140 ns	45 ns		
GSM-80	80 ns	160 ns	50 ns		

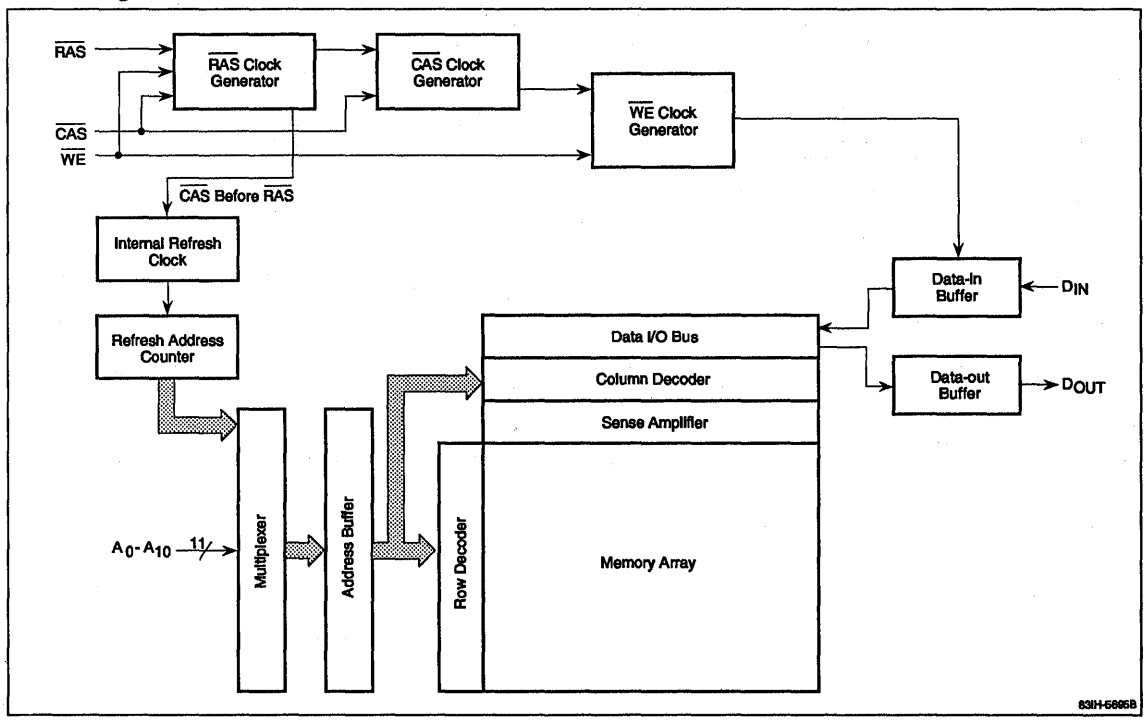
Ordering Information, μPD424100L (+ 3.3 V; standard version; 3rd-generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD424100LLA-A70	70 ns	140 ns	45 ns	26/20-pin plastic SOJ (300-mil)
LA-A80	80 ns	160 ns	50 ns	
μPD424100LV-A70	70 ns	140 ns	45 ns	20-pin plastic ZIP
V-A80	80 ns	160 ns	50 ns	
μPD424100LGS-A70	70 ns	140 ns	45 ns	26/20-pin plastic TSOP (normal pinouts)
GS-A80	80 ns	160 ns	50 ns	
μPD424100LGSM-A70	70 ns	140 ns	45 ns	26/20-pin plastic TSOP (reverse pinouts)
GSM-A80	80 ns	160 ns	50 ns	

Ordering Information, μPD42S4100L (+ 3.3 V; self-refresh, low-power version; 3rd-generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Self-Refresh Current (max)	Package
μPD42S4100LLA-A70	70 ns	140 ns	45 ns	100 μA	26/20-pin plastic SOJ (300-mil)
LA-A80	80 ns	160 ns	50 ns		
μPD42S4100LV-A70	70 ns	140 ns	45 ns	100 μA	20-pin plastic ZIP
V-A80	80 ns	160 ns	50 ns		
μPD42S4100LGS-A70	70 ns	140 ns	45 ns	100 μA	26/20-pin plastic TSOP (normal pinouts)
GS-A80	80 ns	160 ns	50 ns		
μPD42S4100LGSM-A70	70 ns	140 ns	45 ns	100 μA	26/20-pin plastic TSOP (reverse pinouts)
GSM-A80	80 ns	160 ns	50 ns		

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
5-volt devices	50 mA
3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses, D_{IN}
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_O	7	pF	D_{OUT}

DC Characteristics; 5-Volt Devices

Recommended operating conditions unless otherwise noted.

		424100, 424100A		42S4100A			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Standby current	I_{CC2}		2.0		2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
			1.0		0.2	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10	10	−10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	−10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		2.4		V	I_{OH} = −5 mA
Self-refresh current	I_{CC7}	Not applicable			200	μA	I_O = 0 mA; all input pins ≥ V_{CC} − 0.2 V or ≤ 0.2 V or open; t_{RAS} ≥ 100 μs; 1024 refresh cycles must be performed within 16 ms before entering self-refresh and after exiting self-refresh

5a

DC Characteristics; 3.3-Volt Devices

Recommended operating conditions unless otherwise noted.

		424100L		42S4100L			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Standby current	I_{CC2}		2.0		0.5	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
			0.5		0.1	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−5	5	−5	5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−5	5	−5	5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4		0.4	V	I_{OL} = 2 mA
Output voltage, high	V_{OH}	2.4		2.4		V	I_{OH} = −2 mA
Self-refresh current	I_{CC7}	Not applicable			100	μA	I_O = 0 mA; all input pins ≥ V_{CC} − 0.2 V or ≤ 0.2 V or open; t_{RAS} ≥ 100 μs; 1024 refresh cycles must be performed within 16 ms before entering self-refresh and after exiting self-refresh

Low-Power Battery Backup (Low-Power and Self-Refresh Versions Only)

Symbol	424100-xxL	42S4100A	42S4100L	Unit	t_{RAS}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6} (max)	500	300	150	μA	≤ 1 μs	1024 refresh cycles (min) every 128 ms;	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; D_{IN}, $\overline{WE}$, Addresses ≥ V_{CC} – 0.2 V or ≤ 0.2 V; D_{OUT} open
	300	200	100	μA	≤ 200 ns	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V or ≤ 0.2 V, as appropriate; D_{OUT} open; all other inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V	

Recommended Operating Conditions

Parameter	Symbol	5-Volt Devices Min	Typ	Max	3.3-Volt Devices Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–1.0		0.8	–0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

AC Characteristics

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	-50 Min	-50 Max	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5 V)		100		120		100		90	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC1} (+3.3 V)						70		60	mA	
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5 V)		100		120		100		90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC3} (+3.3 V)						70		60	mA	
Operating current, fast-page cycle, average	I_{CC4} (+5 V)		90		90		80		70	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
	I_{CC4} (+3.3 V)						60		50	mA	
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5 V)		100		120		100		90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC5} (+3.3 V)						70		60	mA	
Access time from column address	t_{AA}		25		30		35		40	ns	(Notes 3, 4, 7, 8, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		30		35		40		45	ns	(Notes 3, 4, 7, 11)
Column address setup time	t_{ASC}	0	5	0	5	0	10	0	15	ns	(Note 9)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	25		30		35		40		ns	(Note 16)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		15		15		20		20	ns	(Notes 3, 4, 7, 8, 11)
Column address hold time	t_{CAH}	15		15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	10		15		15		15		ns	

AC Characteristics (cont)

Parameter	Symbol	-50		-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ hold (CBR self-refresh)	t_{CHS}	−50		−50		−50		−50		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		0		ns	(Note 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10	10	10	10	10	15	10	20	ns	(Note 9)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	15		20		20		20		ns	(Note 16)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		15		ns	
Data-in hold time	t_{DH}	10		15		15		15		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	15	0	20	ns	(Note 10)
Fast-page cycle time	t_{PC}	35		40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	55		65		70		75		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	30	15	35	17	40	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	25		30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ width (CBR self-refresh)	t_{RASS}	100		100		100		100		μs	
Random read or write cycle time	t_{RC}	100		120		140		160		ns	(Note 6)
		—		—		130		150		ns	(Notes 6, 18)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	30	20	40	20	50	25	60	ns	(Notes 8, 9)

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AC Characteristics (cont)

		-50		-60		-70		-80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9 (Note 19)
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		70		ns	
		—		—		50		60		ns	(Note 18)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ precharge (CBR self-refresh)	t_{RPS}	90		110		130		150		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	15		15		20		20		ns	
Read-write cycle time	t_{RWC}	125		145		165		185		ns	(Note 6)
		—		—		155		175		ns	(Notes 6, 18)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	50		60		70		80		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	10		10		15		15		ns	(Note 14)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		15		ns	
Write command pulse width	t_{WP}	10		10		15		15		ns	(Note 14)
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

AC Characteristics

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) For random read cycles, access time is defined as follows.

Input Conditions	Access Time
$t_{RAD} \leq t_{RAD}$ (max), $t_{RCD} \leq t_{RCD}$ (max)	t_{RAC}
$t_{RAD} \geq t_{RAD}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{RAD} \geq t_{RAD}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(9) t_{RCD} (max), t_{RAD} (max), t_{ASC} (max), and t_{CP} (max) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA}, t_{CAC}, or t_{ACP}) is to be used for determing when output data will be available.

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(11) For fast-page read operation, access time is defined follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

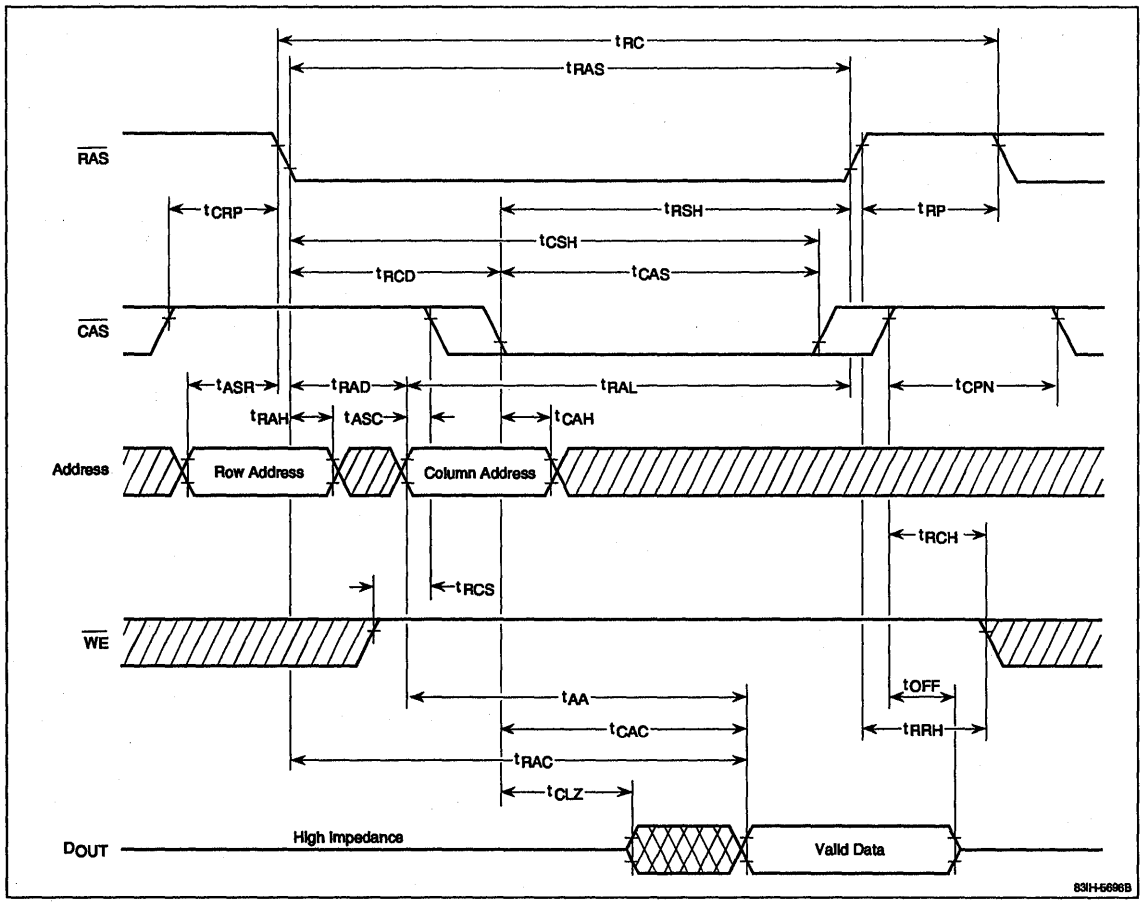
(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

(18) Applies to μPD424100L and μPD42S4100L.

(19) 1024 refresh cycles must be performed within 16 ms before entering self-refresh and after exiting self-refresh.

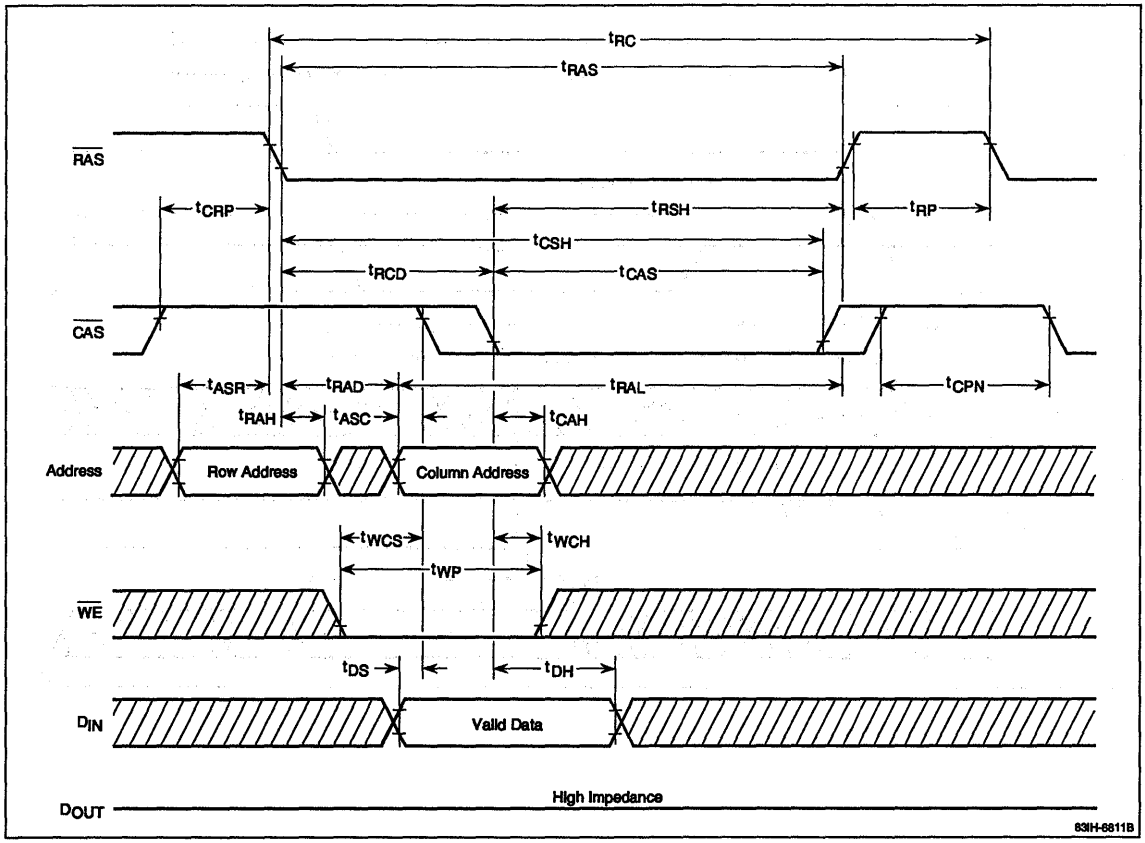
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



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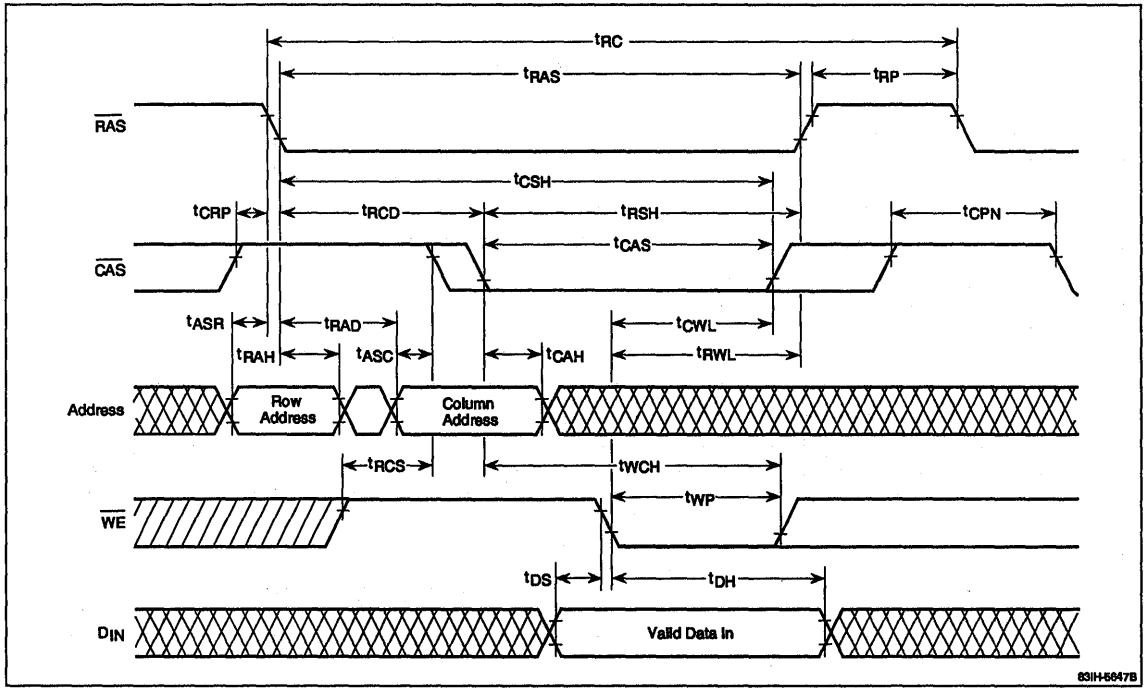
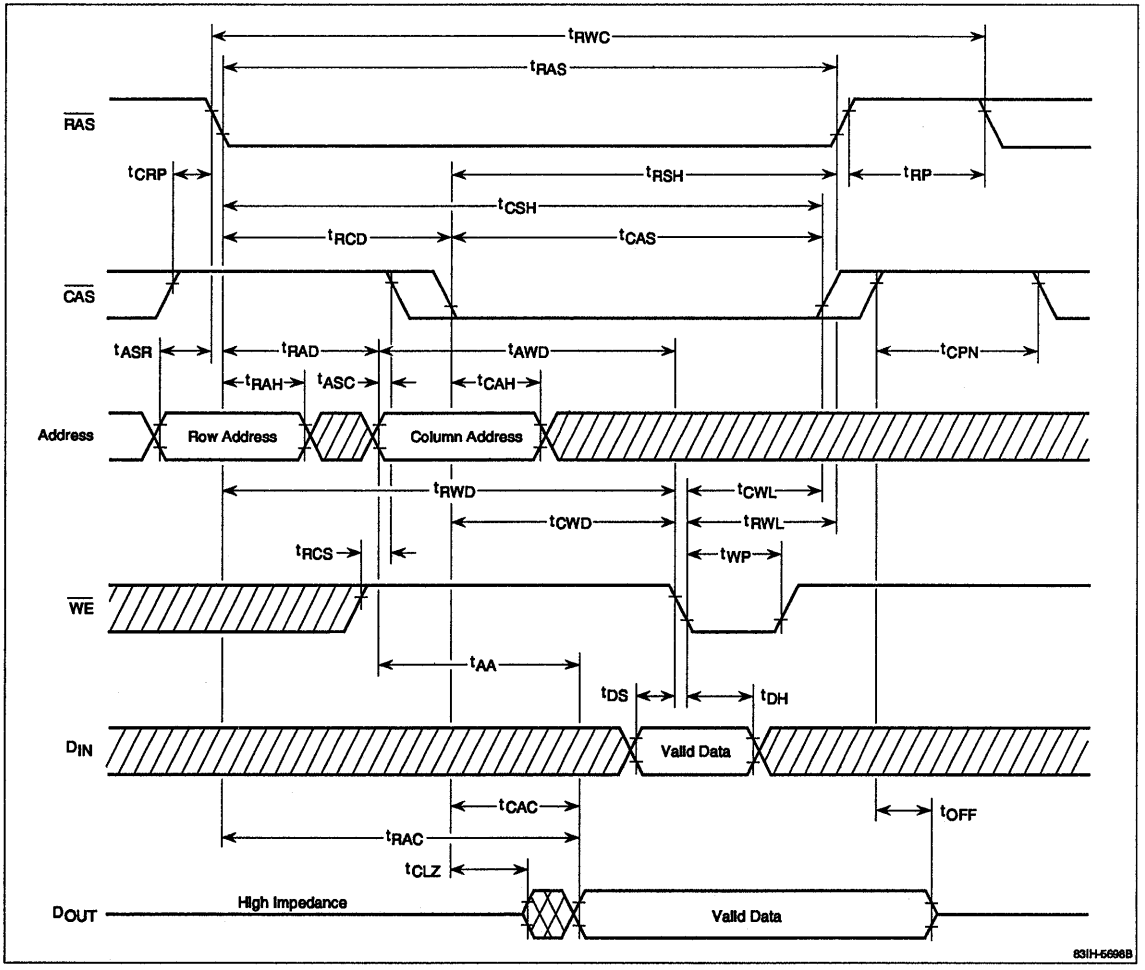
Timing Waveforms (cont)

Late Write Cycle



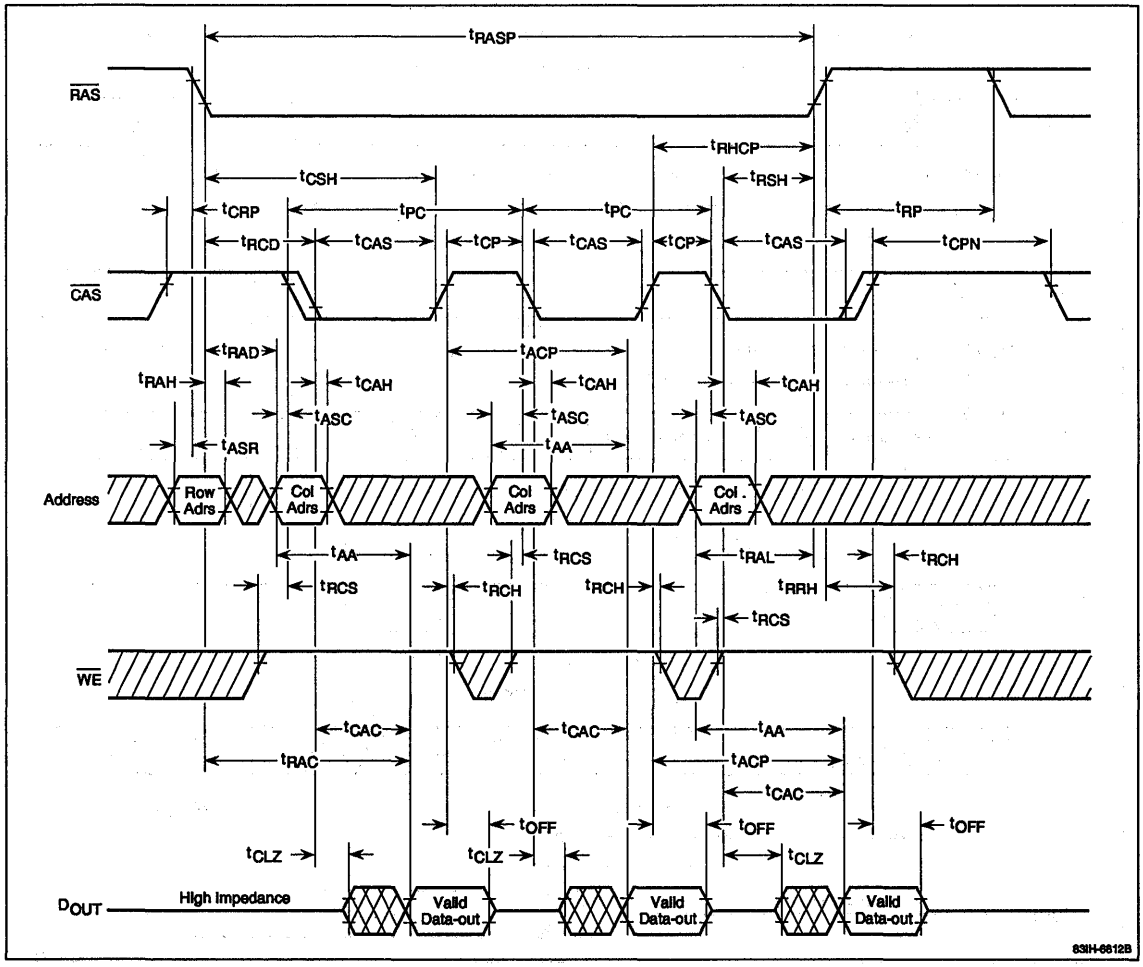
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



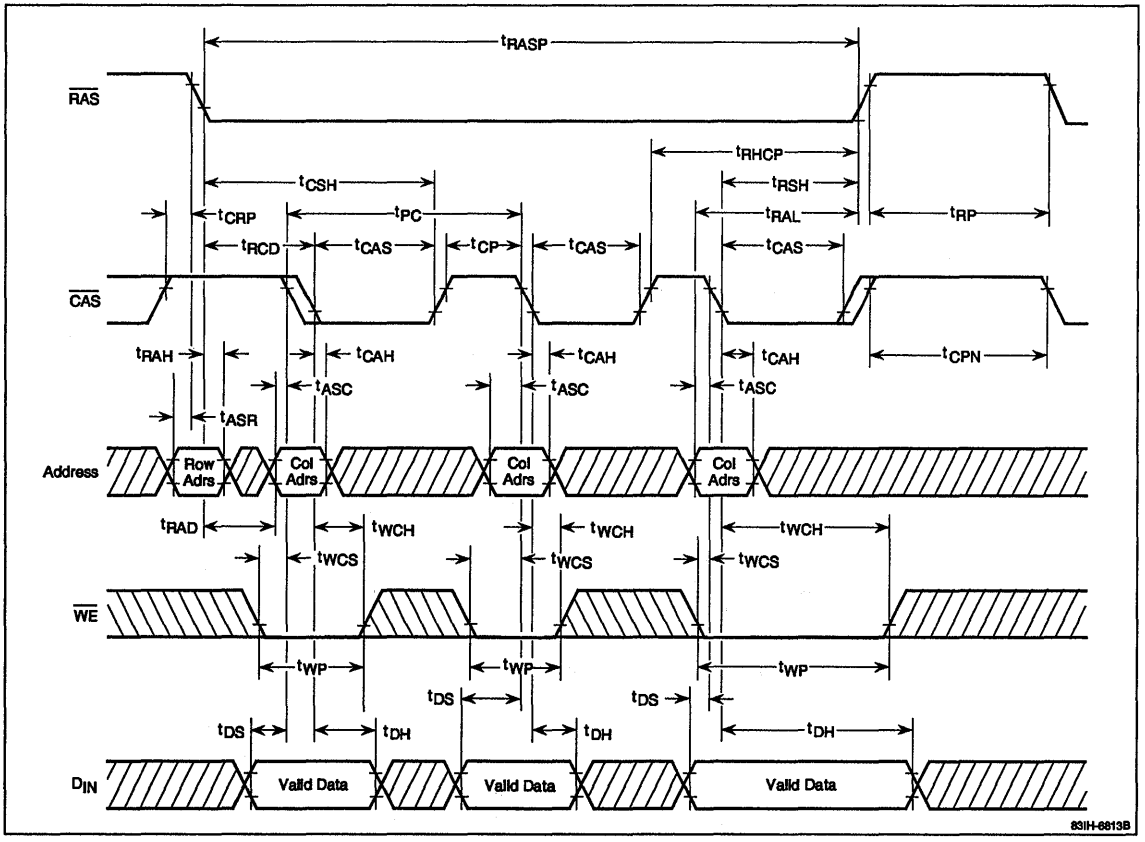
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



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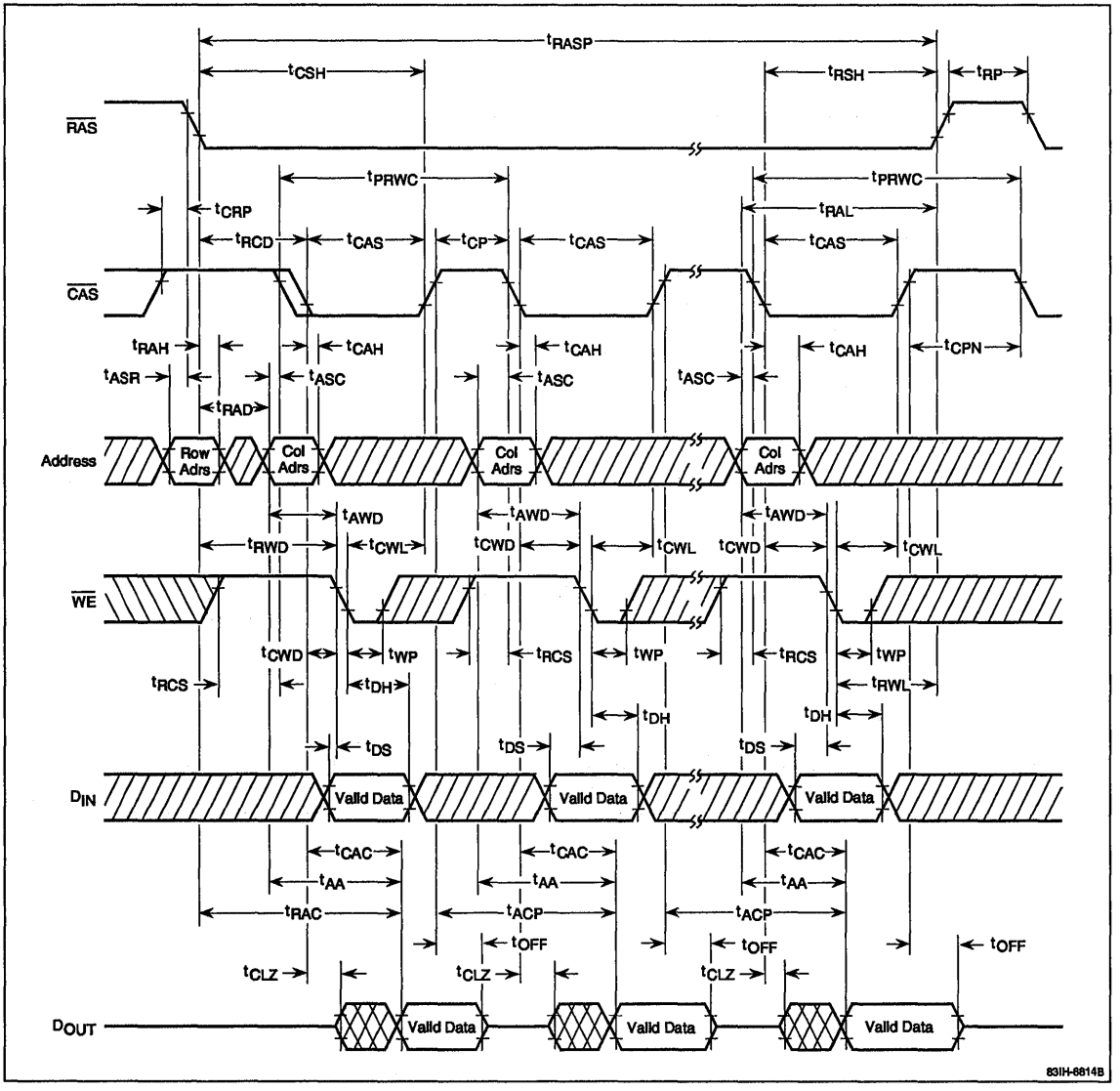
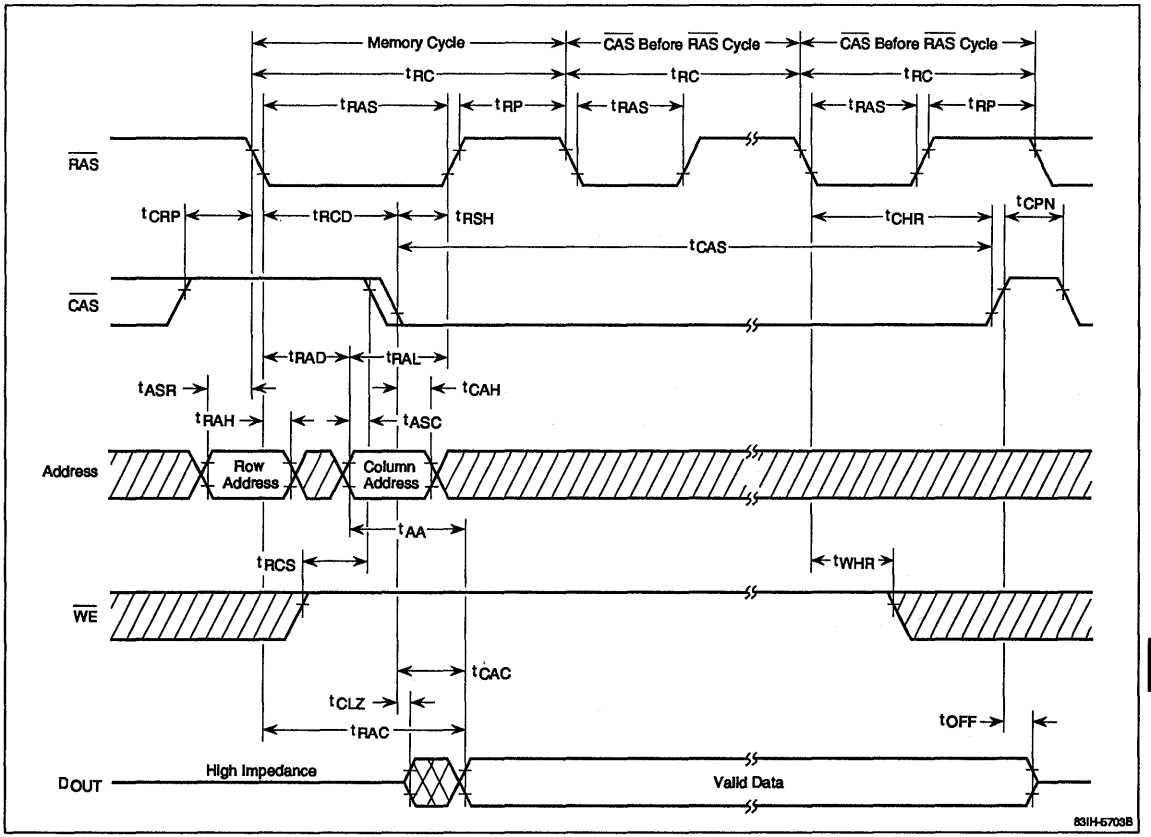
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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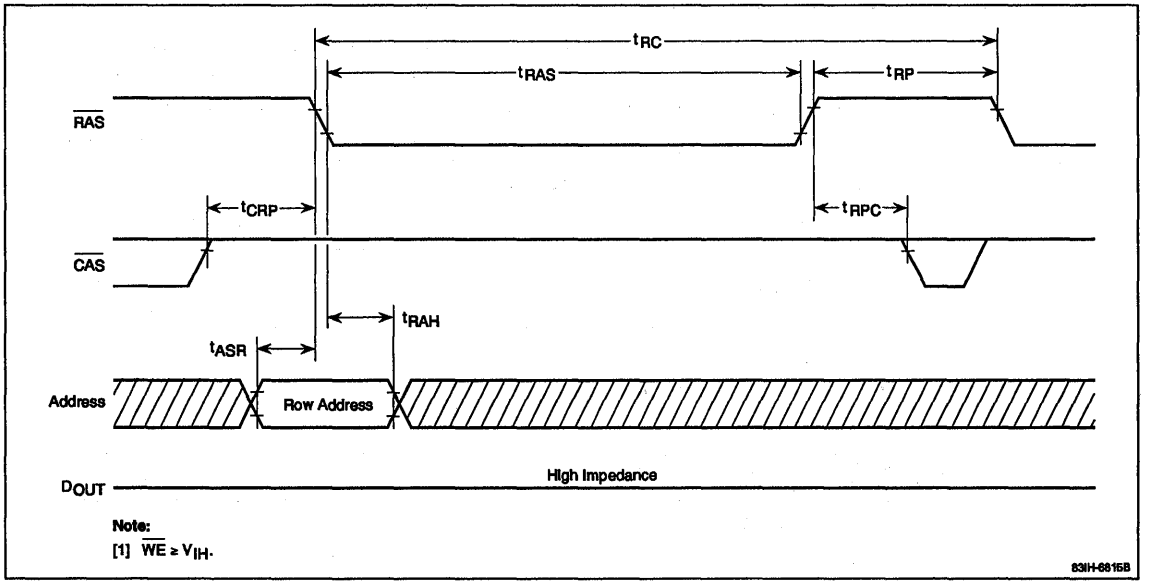
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

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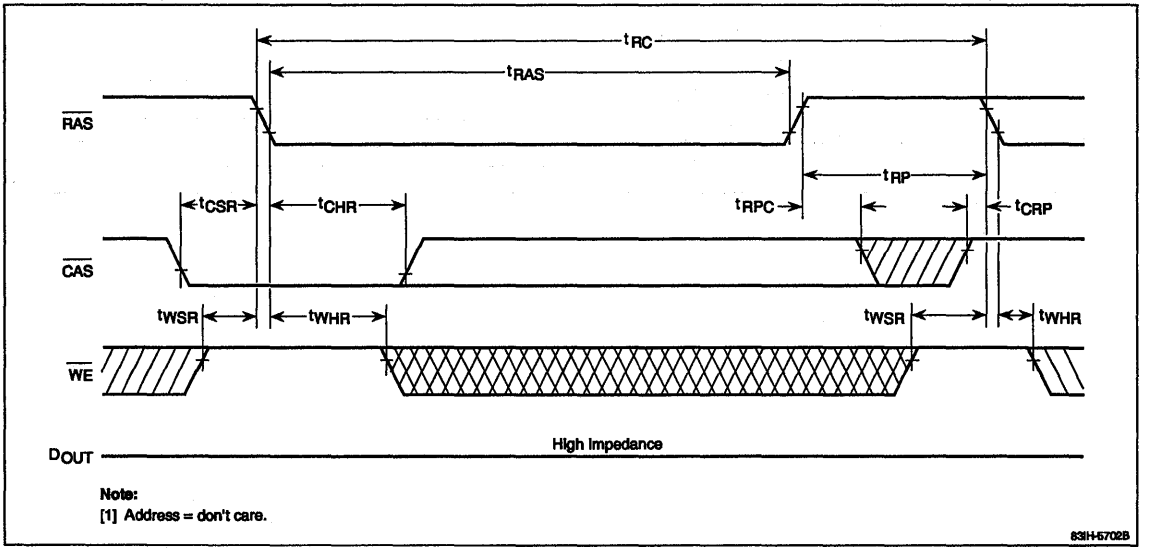
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

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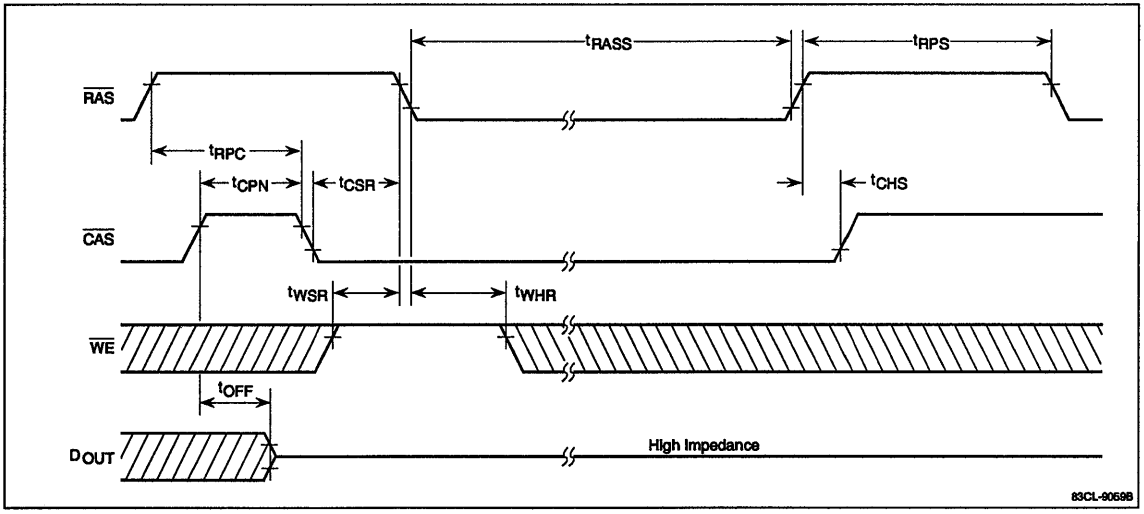
Timing Waveforms (cont)

CBR Self-Refresh Cycle



μPD424101
4,194,304 x 1-Bit
Dynamic CMOS RAM

Description

The μPD424101 is a nibble-mode dynamic RAM organized as 4,194,304 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. Nibble-mode read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1024 address combinations of A_0 - A_9 during a 16-ms refresh period.

Features

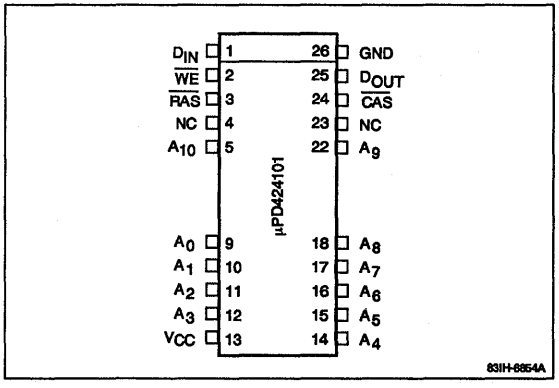
- 4,194,304-word by 1-bit organization
- Single +5-volt power supply
- Nibble-mode option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- 1024 refresh cycles every 16 ms
- 26/20-pin SOJ, 20-pin ZIP, or 26/20-pin TSOP plastic packaging

Pin Identification

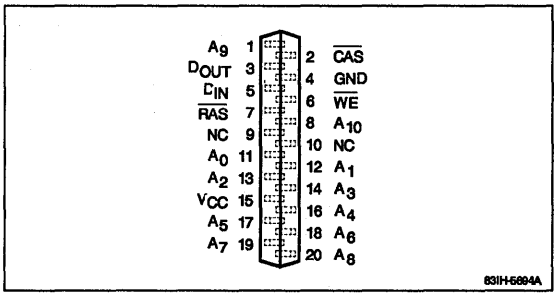
Name	Function
A_0 - A_{10}	Address inputs
$\overline{CAS}$	Chip select
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configurations

26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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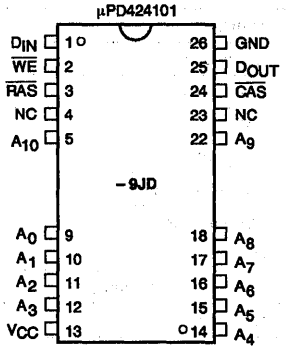
Pin Configurations (cont)

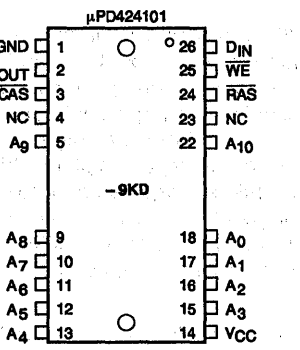
26/20-Pin Plastic TSOP (Normal Pinouts)



Suffix –9JD in the package identifier denotes normal pinout sequence.

83FM-8575A

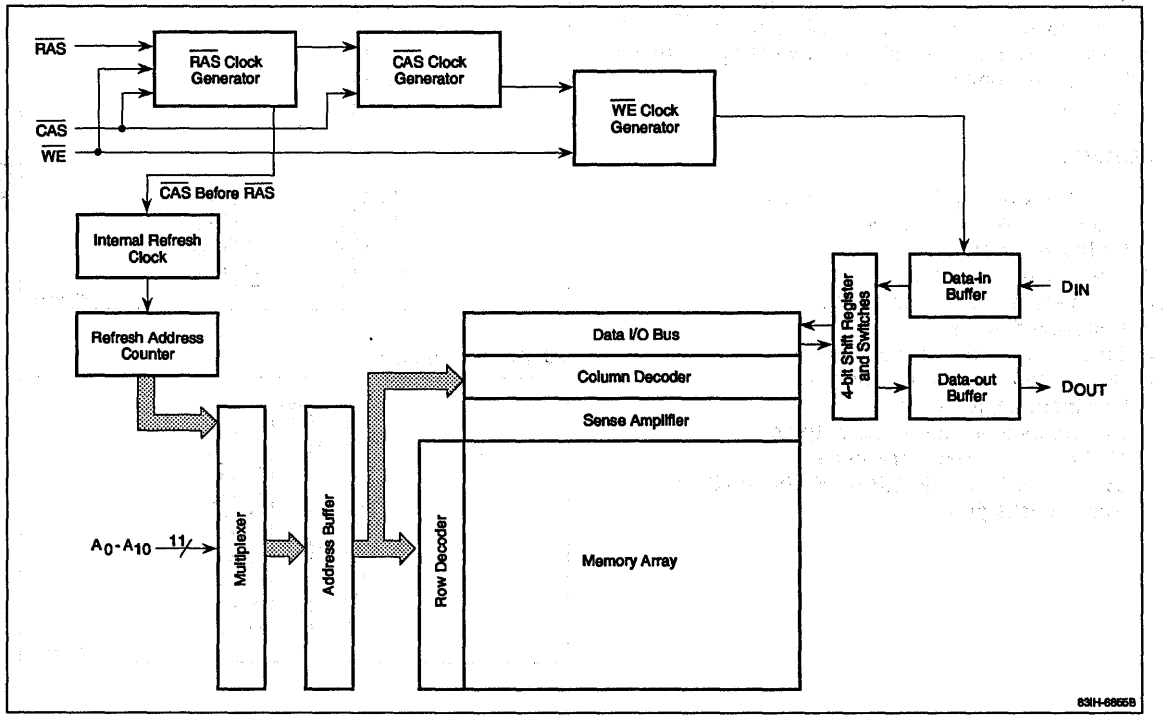
26/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –9KD in the package identifier denotes reverse pinout sequence.

83FM-8576A

Block Diagram



83IH-8855B

Ordering Information

Part Number	RAS Access Time	R/W Cycle Time	Nibble Cycle Time	Refresh Period	Standby Current	Package
μPD424101LA-60	60 ns	120 ns	40 ns	16 ms	1 mA	26/20-pin plastic SOJ (300-mil)
LA-70	70 ns	140 ns	40 ns			
LA-80	80 ns	160 ns	40 ns			
LA-10	100 ns	190 ns	45 ns			
μPD424101LA-60L	60 ns	120 ns	40 ns	128 ms	300 μA	
LA-70L	70 ns	140 ns	40 ns			
LA-80L	80 ns	160 ns	40 ns			
LA-10L	100 ns	190 ns	45 ns			
μPD424101V-60	60 ns	120 ns	40 ns	16 ms	1 mA	20-pin plastic ZIP
V-70	70 ns	140 ns	40 ns			
V-80	80 ns	160 ns	40 ns			
V-10	100 ns	190 ns	45 ns			
μPD424101V-60L	60 ns	120 ns	40 ns	128 ms	300 μA	
V-70L	70 ns	140 ns	40 ns			
V-80L	80 ns	160 ns	40 ns			
V-10L	100 ns	190 ns	45 ns			
μPD424101GS-60	60 ns	120 ns	40 ns	16 ms	1 mA	26/20-pin plastic TSOP (normal pinouts)
GS-70	70 ns	140 ns	40 ns			
GS-80	80 ns	160 ns	40 ns			
GS-10	100 ns	190 ns	45 ns			
μPD424101GS-60L	60 ns	120 ns	40 ns	128 ms	300 μA	
GS-70L	70 ns	140 ns	40 ns			
GS-80L	80 ns	160 ns	40 ns			
GS-10L	100 ns	190 ns	45 ns			
μPD424101GSM-60	60 ns	120 ns	40 ns	16 ms	1 mA	26/20-pin plastic TSOP (reverse pinouts)
GSM-70	70 ns	140 ns	40 ns			
GSM-80	80 ns	160 ns	40 ns			
GSM-10	100 ns	190 ns	45 ns			
μPD424101GSM-60L	60 ns	120 ns	40 ns	128 ms	300 μA	
GSM-70L	70 ns	140 ns	40 ns			
GSM-80L	80 ns	160 ns	40 ns			
GSM-10L	100 ns	190 ns	45 ns			

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_O	7	pF	D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

Low-Power Battery Backup (-L Versions Only)

Symbol	Max	Unit	t_{RAS}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	500	μA	≤ 1 μs	1024 refresh cycles (min) every 128 ms; $\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V or ≤ 0.2 V, as appropriate; D_{OUT} open; all other inputs ≥ V_{CC} − 0.2 V or ≤ 0.2 V	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; D_{IN}, $\overline{WE}$, Addresses ≥ V_{CC} − 0.2 V or ≤ 0.2 V; D_{OUT} open
	300	μA	≤ 200 μs		
t_{REF}	128	ms			

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD424101-60		μPD424101-70		μPD424101-80		μPD424101-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		120		100		90		80	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		120		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Operating current, nibble mode, average	I_{CC4}		80		80		70		60	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{NC} = t_{NC}$ min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		120		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		40		50		ns	(Note 16)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ precharge time, non-nibble cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 16)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 15)
Nibble mode access time	t_{NAC}		20		20		20		25	ns	

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AC Characteristics (cont)

Parameter	Symbol	μPD424101-60		μPD424101-70		μPD424101-80		μPD424101-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ pulse width in nibble mode	t_{NAS}	20		20		20		25		ns	
Nibble mode cycle time	t_{NC}	40		40		40		45		ns	
$\overline{CAS}$ to $\overline{WE}$ delay in nibble mode	t_{NCWD}	20		20		20		25		ns	
Write command to $\overline{CAS}$ lead time in nibble mode	t_{NCWL}	15		15		20		25		ns	
$\overline{CAS}$ precharge time in nibble mode	t_{NP}	10		10		10		10		ns	
$\overline{RAS}$ hold time for nibble read cycle	t_{NRRSH}	20		20		20		25		ns	
$\overline{RAS}$ hold time for nibble write cycle	t_{NWRSH}	20		20		20		25		ns	
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 10)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width in nibble mode	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD424101-60 Min	μPD424101-60 Max	μPD424101-70 Min	μPD424101-70 Max	μPD424101-80 Min	μPD424101-80 Max	μPD424101-10 Min	μPD424101-10 Max	Unit	Test Conditions
Read-write cycle time	t_{RWC}	145		165		185		220		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		20		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 14)
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each nibble cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition an is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

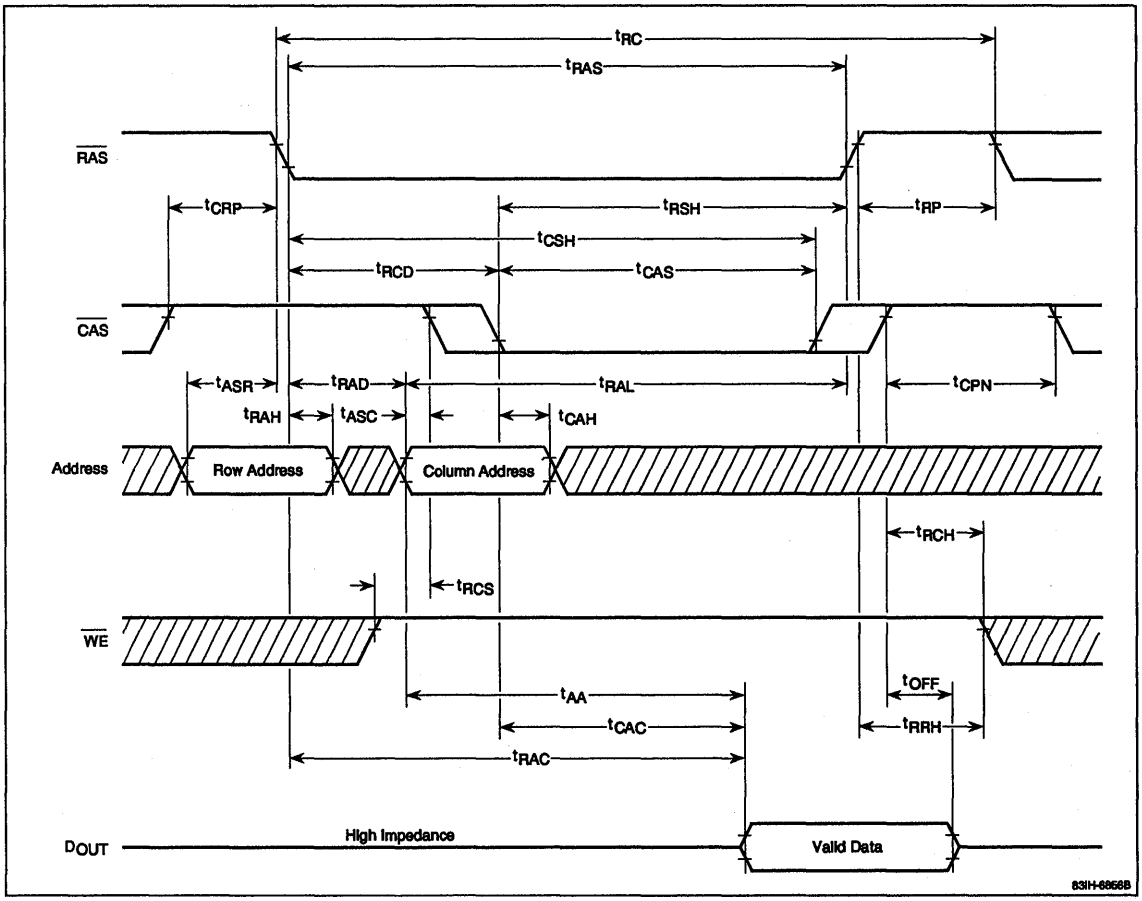
(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

5b

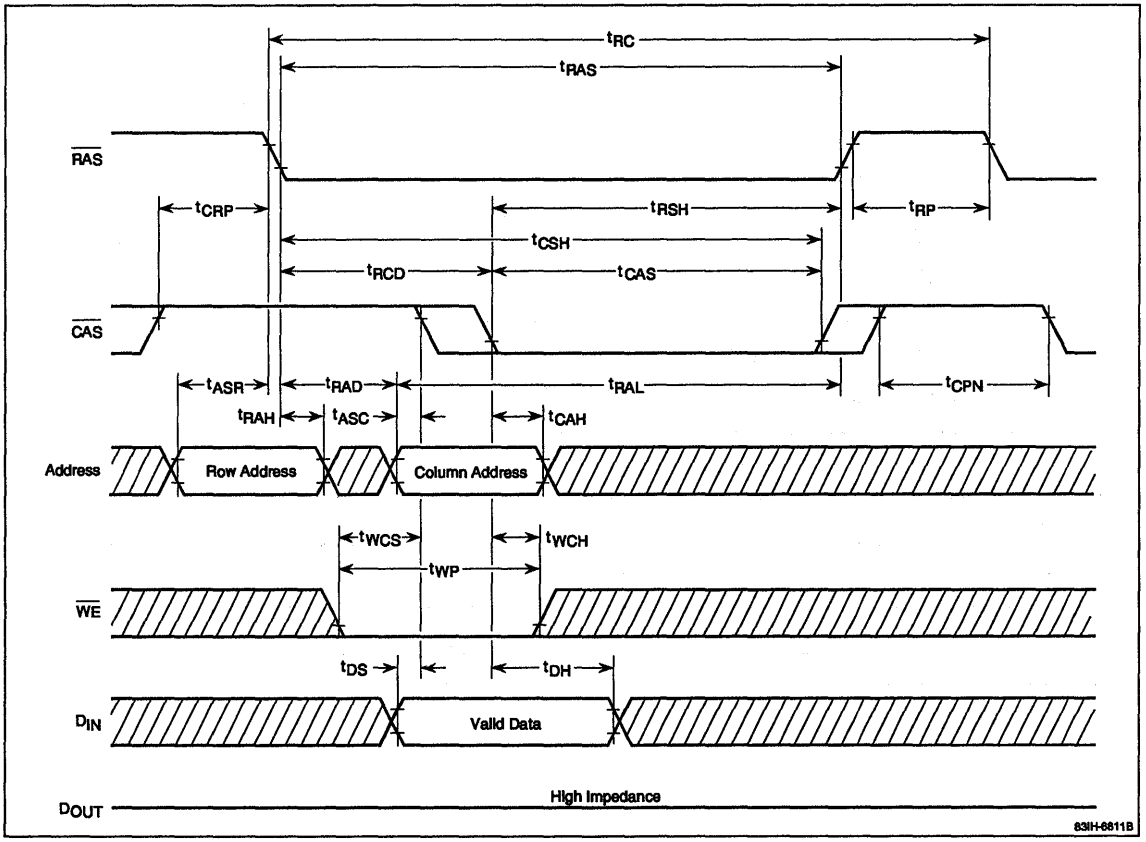
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

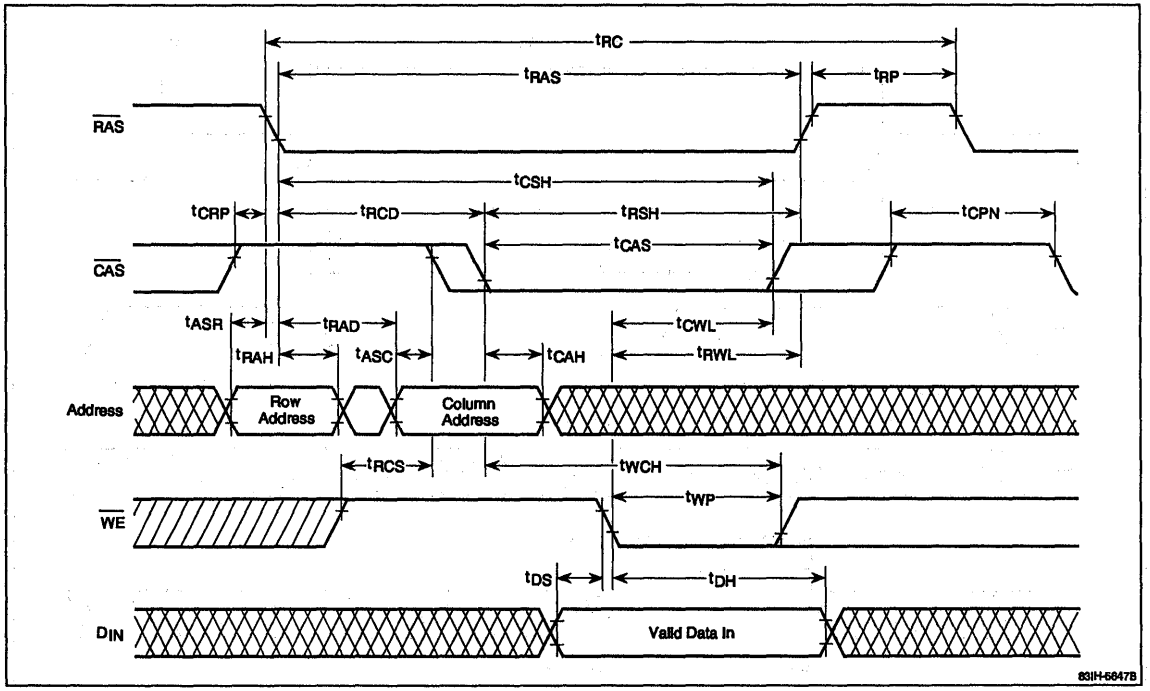
Early Write Cycle



5b

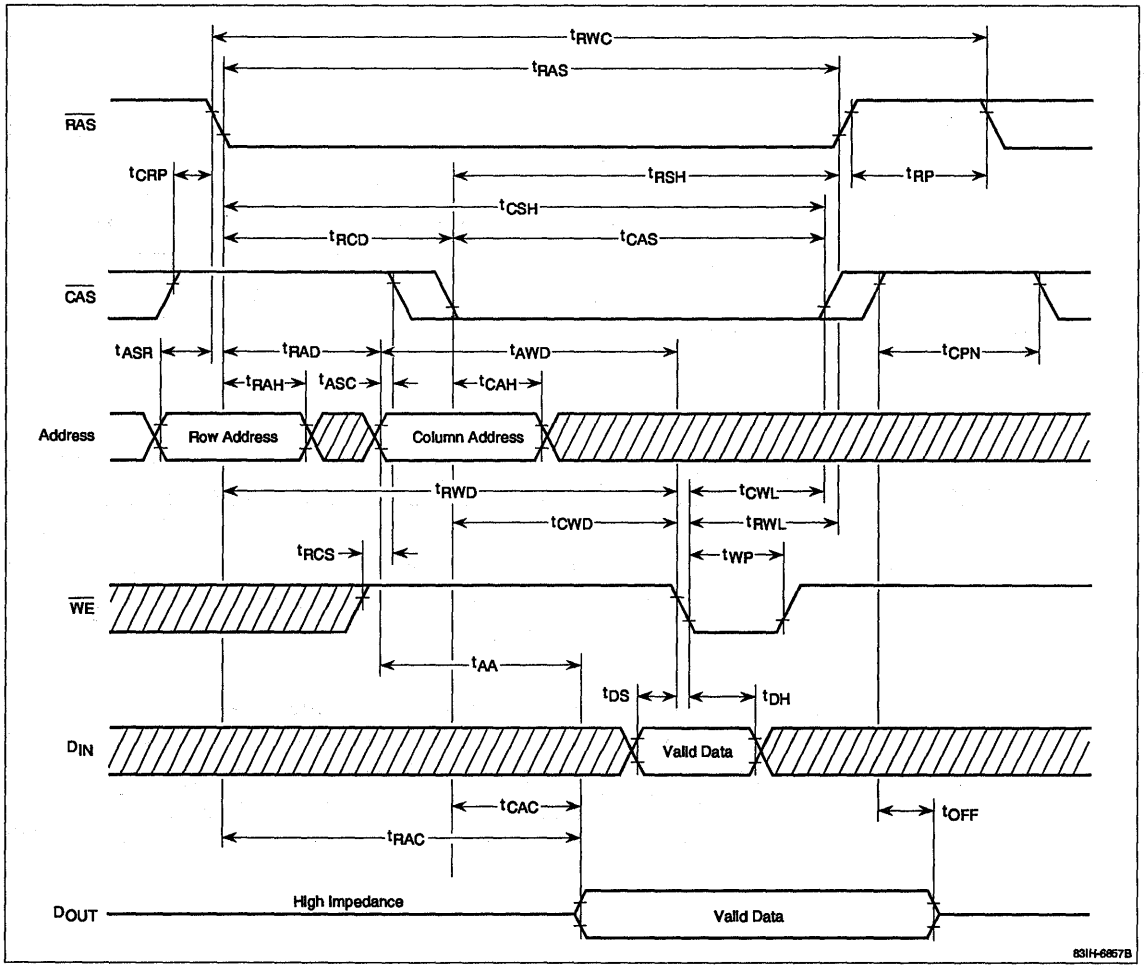
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



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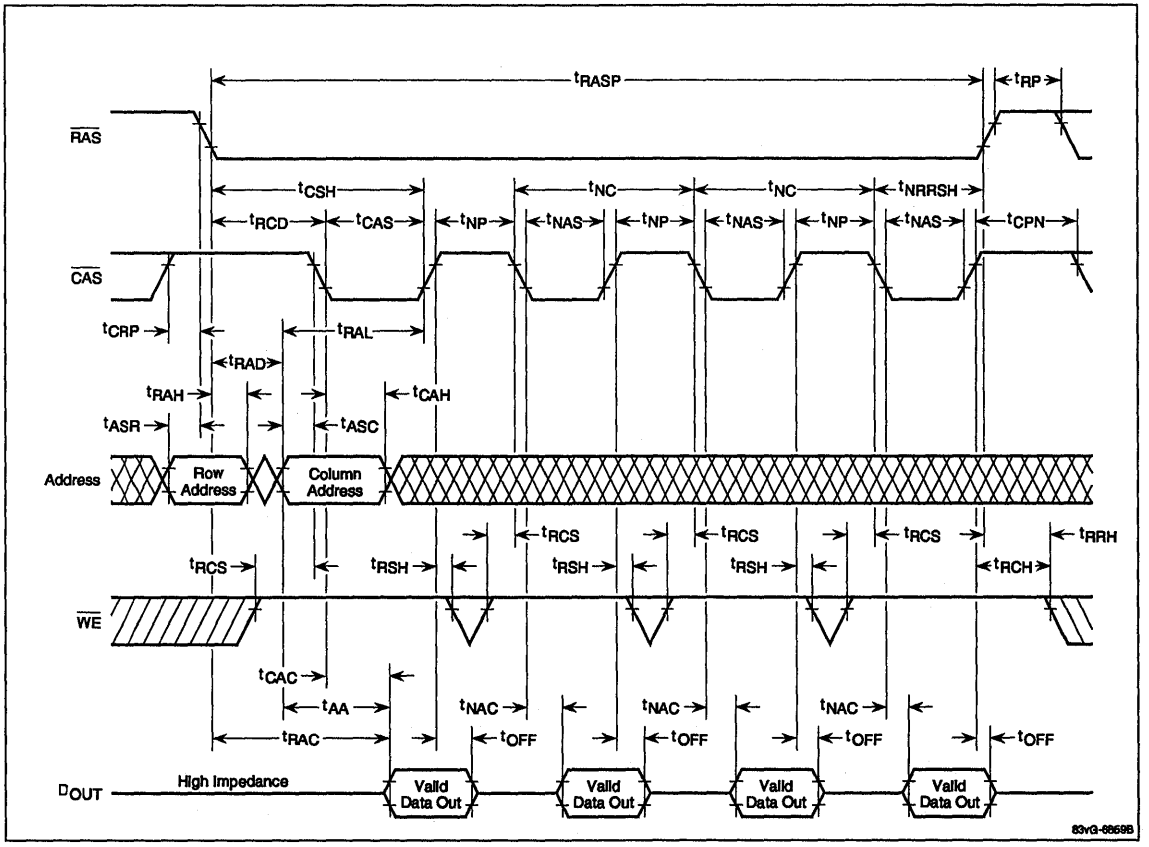
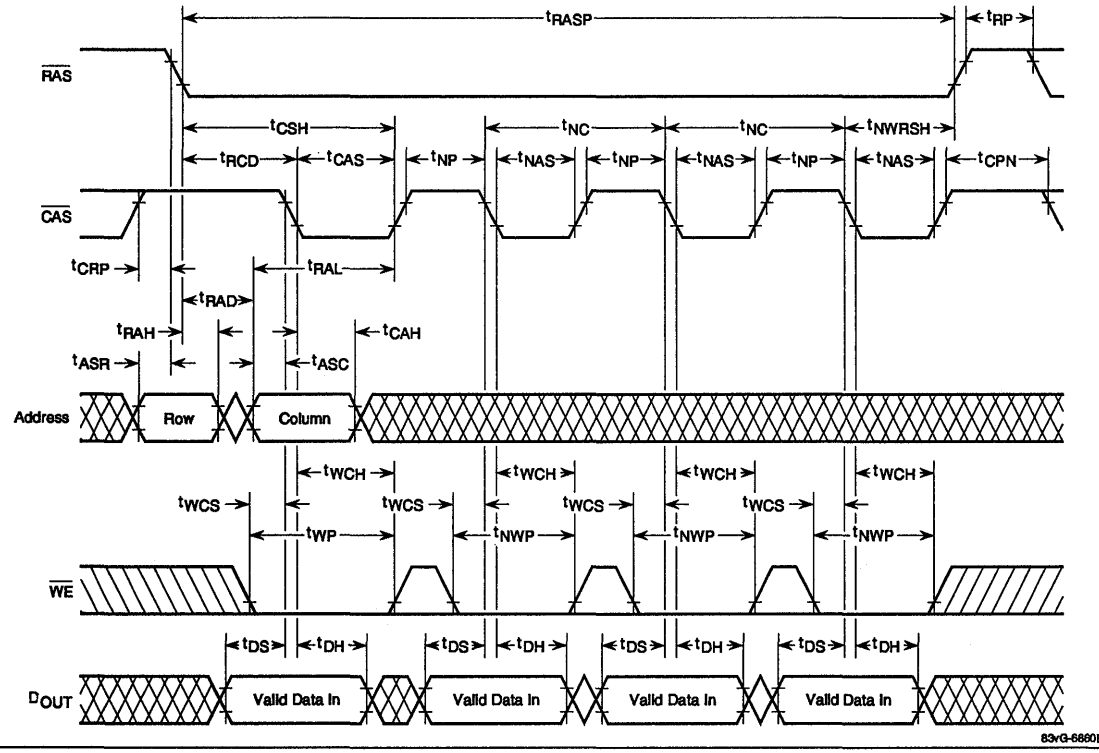
Timing Waveforms (cont)

Nibble Read Cycle



Timing Waveforms (cont)

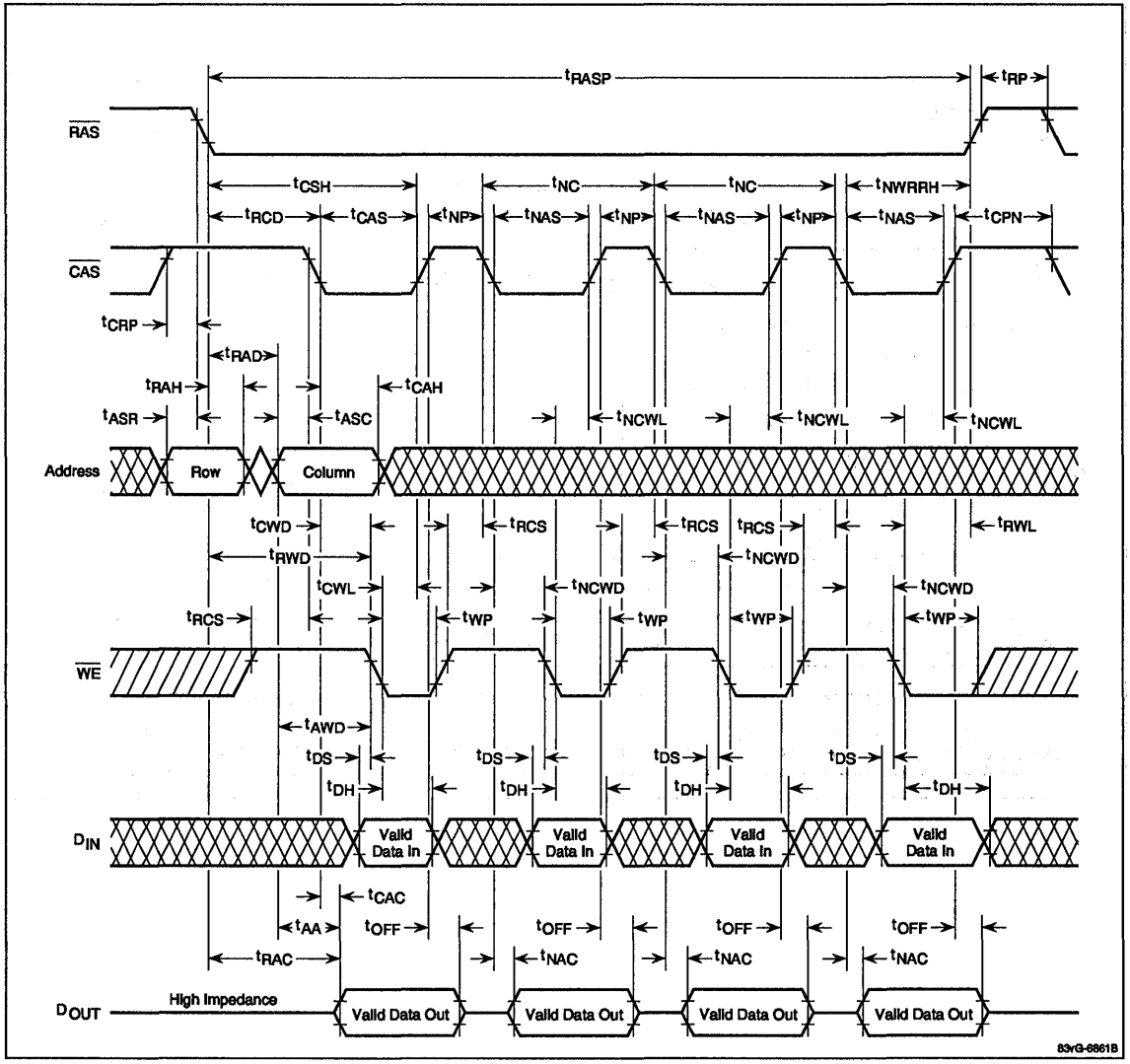
Nibble Early Write Cycle



5b

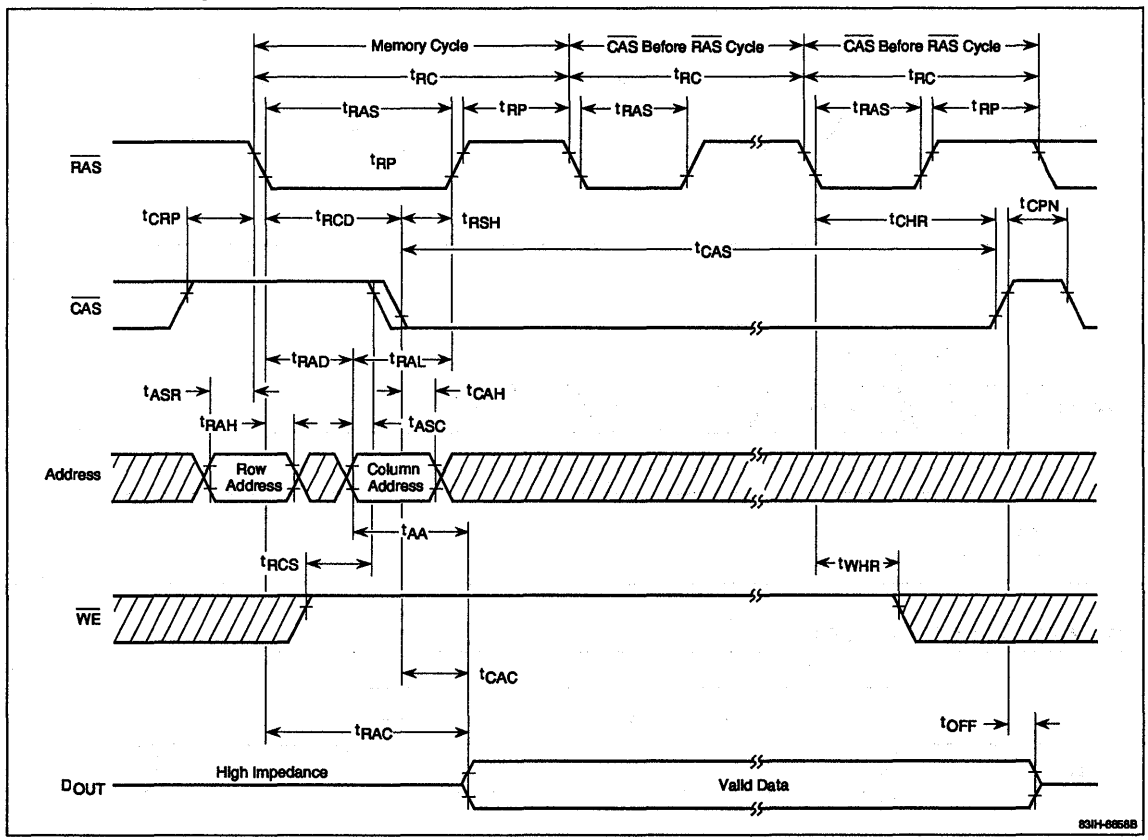
Timing Waveforms (cont)

Nibble Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

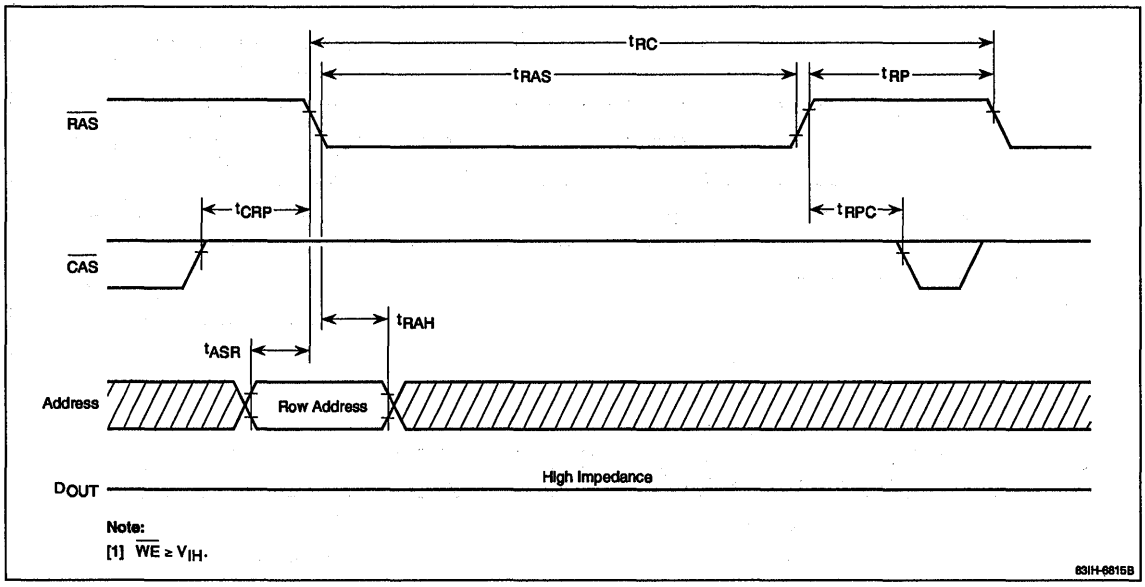
Hidden Refresh Cycle



5b

Timing Waveforms (cont)

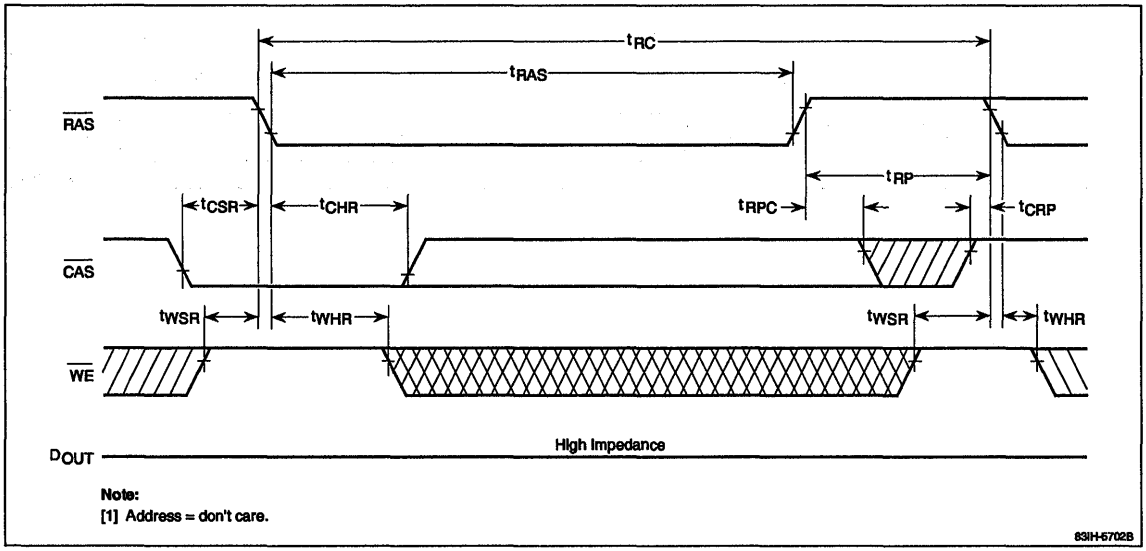
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

83IH-5702B

μPD424102
4,194,304 x 1-Bit
Dynamic CMOS RAM

Description

The μPD424102 is a static-column dynamic RAM organized as 4,194,304 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CS}$ low. The data output is returned to high impedance by returning $\overline{CS}$ high. Static-column read and write cycles can be executed by cycling $\overline{CS}$.

Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1024 address combinations of A_0 - A_9 during a 16-ms refresh period.

Features

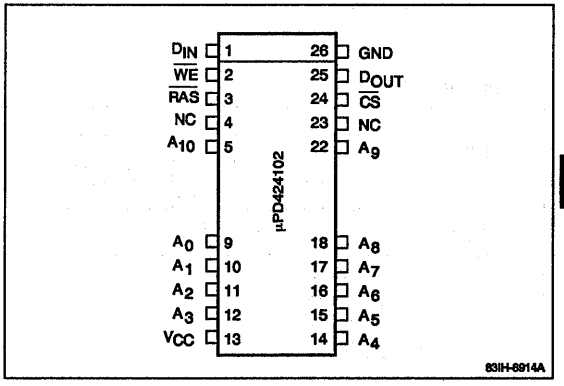
- 4,194,304-word by 1-bit organization
- Single +5-volt power supply
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- 1024 refresh cycles every 16 ms
- 26/20-pin SOJ, 20-pin ZIP, or 26/20-pin TSOP plastic packaging

Pin Identification

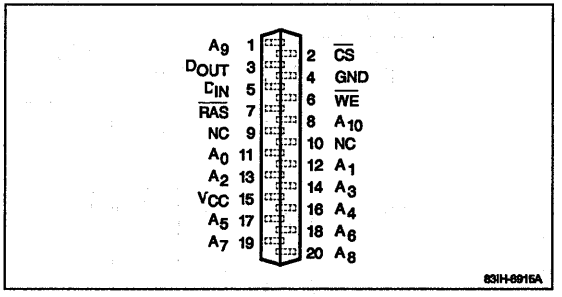
Name	Function
A_0 - A_{10}	Address inputs
$\overline{CS}$	Chip select
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configurations

26/20-Pin Plastic SOJ



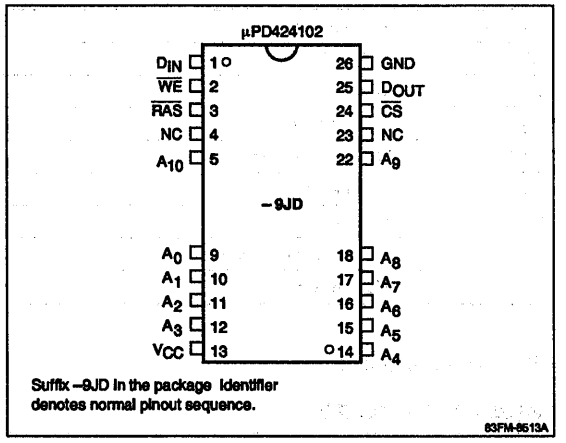
20-Pin Plastic ZIP



5c

Pin Configurations (cont)

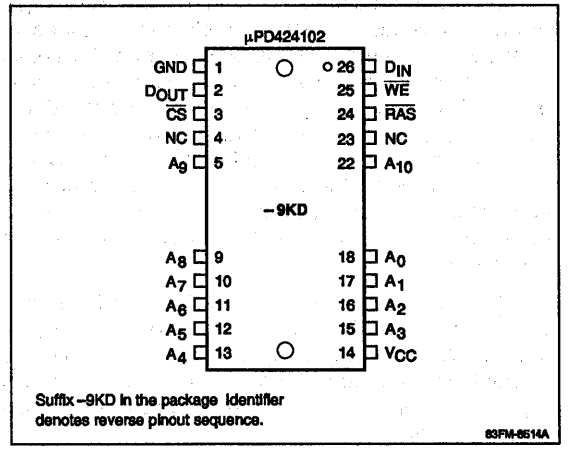
26/20-Pin Plastic TSOP (Normal Pinouts)



Suffix –9JD in the package identifier denotes normal pinout sequence.

83FM-8513A

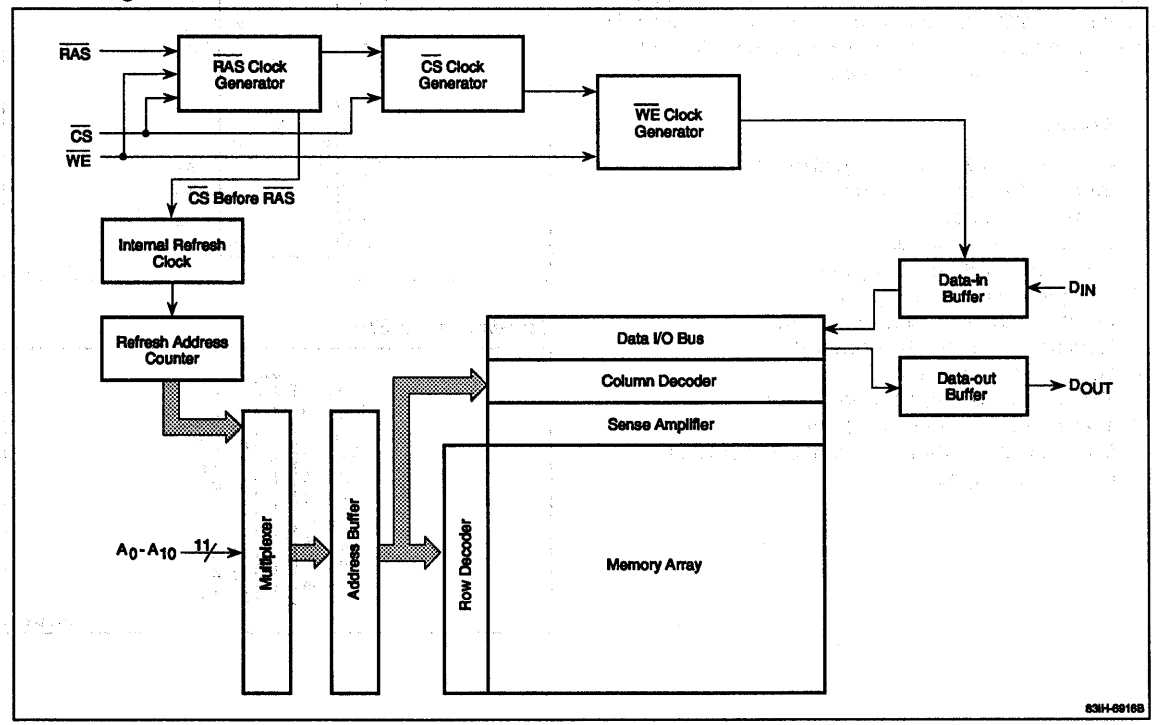
26/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –9KD in the package identifier denotes reverse pinout sequence.

83FM-8514A

Block Diagram



83IH-8916B

Ordering Information

Part Number	RAS Access Time	R/W Cycle Time	Static-Column Cycle Time	Refresh Period	Standby Current	Package
μPD424102LA-60	60 ns	120 ns	35 ns	16 ms	1 mA	26/20-pin plastic SOJ (300-mil)
LA-70	70 ns	140 ns	40 ns			
LA-80	80 ns	160 ns	50 ns			
LA-10	100 ns	190 ns	60 ns			
μPD424102LA-60L	60 ns	120 ns	35 ns	128 ms	300 μA	
LA-70L	70 ns	140 ns	40 ns			
LA-80L	80 ns	160 ns	50 ns			
LA-10L	100 ns	190 ns	60 ns			
μPD424102V-60	60 ns	120 ns	35 ns	16 ms	1 mA	20-pin plastic ZIP
V-70	70 ns	140 ns	40 ns			
V-80	80 ns	160 ns	50 ns			
V-10	100 ns	190 ns	60 ns			
μPD424102V-60L	60 ns	120 ns	35 ns	128 ms	300 μA	
V-70L	70 ns	140 ns	40 ns			
V-80L	80 ns	160 ns	50 ns			
V-10L	100 ns	190 ns	60 ns			
μPD424102GS-60	60 ns	120 ns	35 ns	16 ms	1 mA	26/20-pin plastic TSOP (normal pinouts)
GS-70	70 ns	140 ns	40 ns			
GS-80	80 ns	160 ns	50 ns			
GS-10	100 ns	190 ns	60 ns			
μPD424102GS-60L	60 ns	120 ns	35 ns	128 ms	300 μA	
GS-70L	70 ns	140 ns	40 ns			
GS-80L	80 ns	160 ns	50 ns			
GS-10L	100 ns	190 ns	60 ns			
μPD424102GSM-60	60 ns	120 ns	35 ns	16 ms	1 mA	26/20-pin plastic TSOP (reverse pinouts)
GSM-70	70 ns	140 ns	40 ns			
GSM-80	80 ns	160 ns	50 ns			
GSM-10	100 ns	190 ns	60 ns			
μPD424102GSM-60L	60 ns	120 ns	35 ns	128 ms	300 μA	
GSM-70L	70 ns	140 ns	40 ns			
GSM-80L	80 ns	160 ns	50 ns			
GSM-10L	100 ns	190 ns	60 ns			

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$
Output capacitance	C_O	7	pF	D_{OUT}

Low-Power Battery Backup (-L Versions Only)

Symbol	Max	Unit	t_{RAS}	$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	500	μA	≤ 1 μs	1024 refresh cycles (min) every 128 ms; $\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V or ≤ 0.2 V, as appropriate; D_{OUT} open; all other inputs ≥ V_{CC} − 0.2 V or ≤ 0.2 V	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V; D_{IN}, $\overline{WE}$, Addresses ≥ V_{CC} − 0.2 V or ≤ 0.2 V; D_{OUT} open
	300	μA	≤ 200 μs		
t_{REF}	128	ms			

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{IH} (min)
			1.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD424102-60		μPD424102-70		μPD424102-80		μPD424102-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80		90		80	mA	$\overline{RAS}$ and $\overline{CS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Static column operating current, average	I_{CC4}		70		60		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)

AC Characteristics (cont)

Parameter	Symbol	μPD424102-60		μPD424102-70		μPD424102-80		μPD424102-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Operating current, $\overline{CS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 9)
Column address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		40		50		ns	(Note 15)
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 8, 9)
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CS}$ precharge time, static-column	t_{CP}	10		10		10		10		ns	
$\overline{CS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 11)
$\overline{CS}$ pulse width	t_{CS}	20	100,000	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 15)
Write command to $\overline{CS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 14)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 14)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 10)
Output hold time from address	t_{OH}	5		5		5		5		ns	
Output enable time from $\overline{WE}$ (rising edge)	t_{OW}		25		25		25		25	ns	
Access time from previous $\overline{WE}$	t_{PWA}		60		70		90		110	ns	(Note 7, 17)

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AC Characteristics (cont)

Parameter	Symbol	μPD424102-60		μPD424102-70		μPD424102-80		μPD424102-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Column address hold time referenced to previous $\overline{WE}$	t_{PWH}	60		70		90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
Static-column $\overline{RAS}$ pulse width	t_{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	(Note 12)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 12)
Read cycle time	t_{RSC}	35		40		50		60		ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSW}	75		85		95		115		ns	
Read-write cycle time	t_{RWC}	145		165		185		220		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 15)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Static-column read/write cycle time	t_{RWSC}	65		75		95		115		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)

AC Characteristics (cont)

Parameter	Symbol	μPD424102-60 Min	μPD424102-60 Max	μPD424102-70 Min	μPD424102-70 Max	μPD424102-80 Min	μPD424102-80 Max	μPD424102-10 Min	μPD424102-10 Max	Unit	Test Conditions
$\overline{WE}$ to column address delay time	t_{WAD}	20	30	22	35	20	45	25	55	ns	(Note 17)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 15)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		20		ns	
Write invalid time	t_{WI}	10		10		10		10		ns	
Output hold time from $\overline{WE}$	t_{WOH}	0		0		0		0		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 13)
Write cycle time	t_{WSC}	35		40		50		60		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CS}$ cycles preceded by any cycle.

(12) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(13) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(14) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

(16) A test mode may be initiated by executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

(17) Assumes that $t_{WAD} \leq t_{WAD}$ (max).

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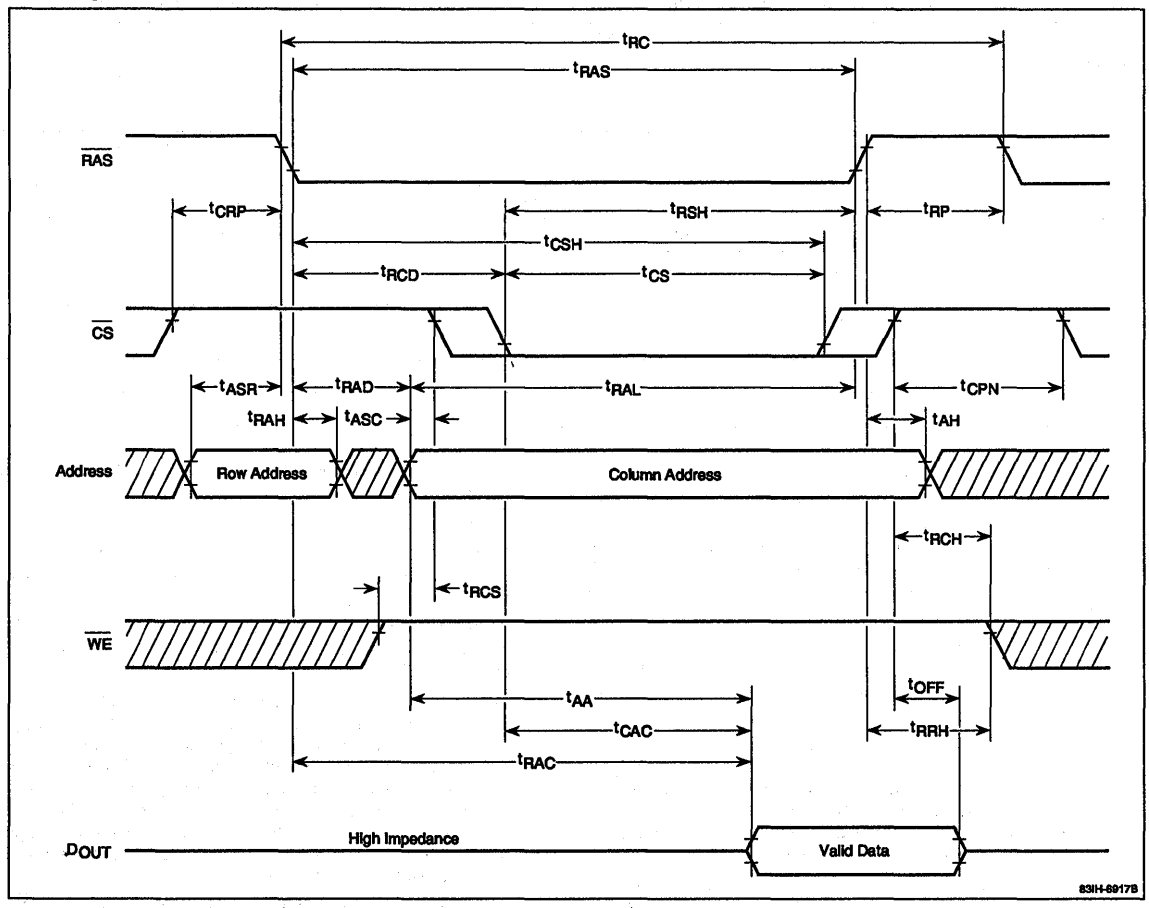
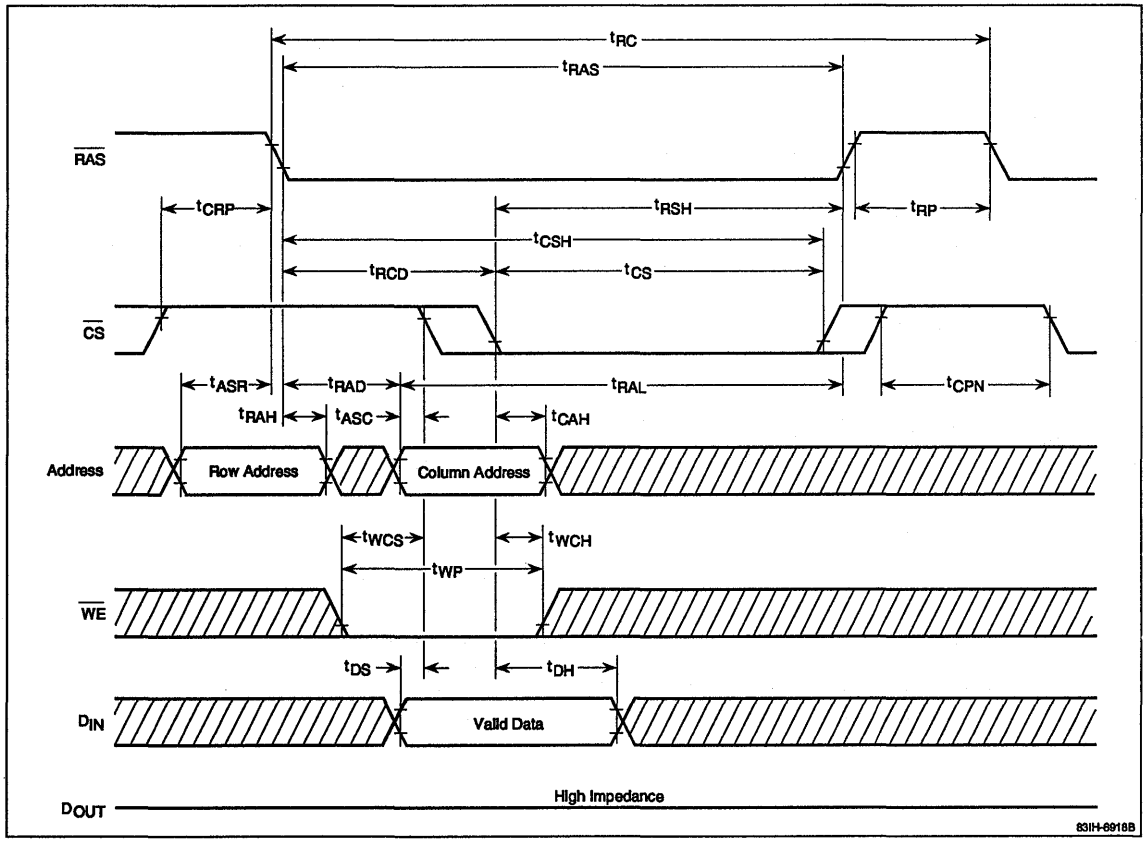
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



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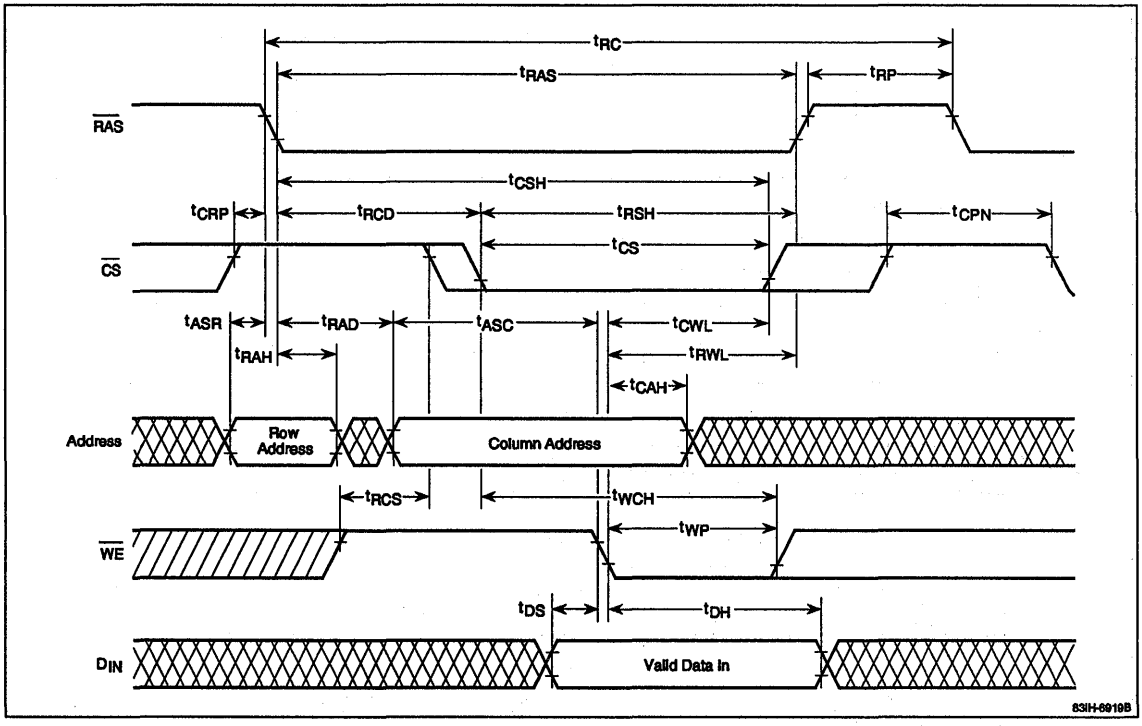
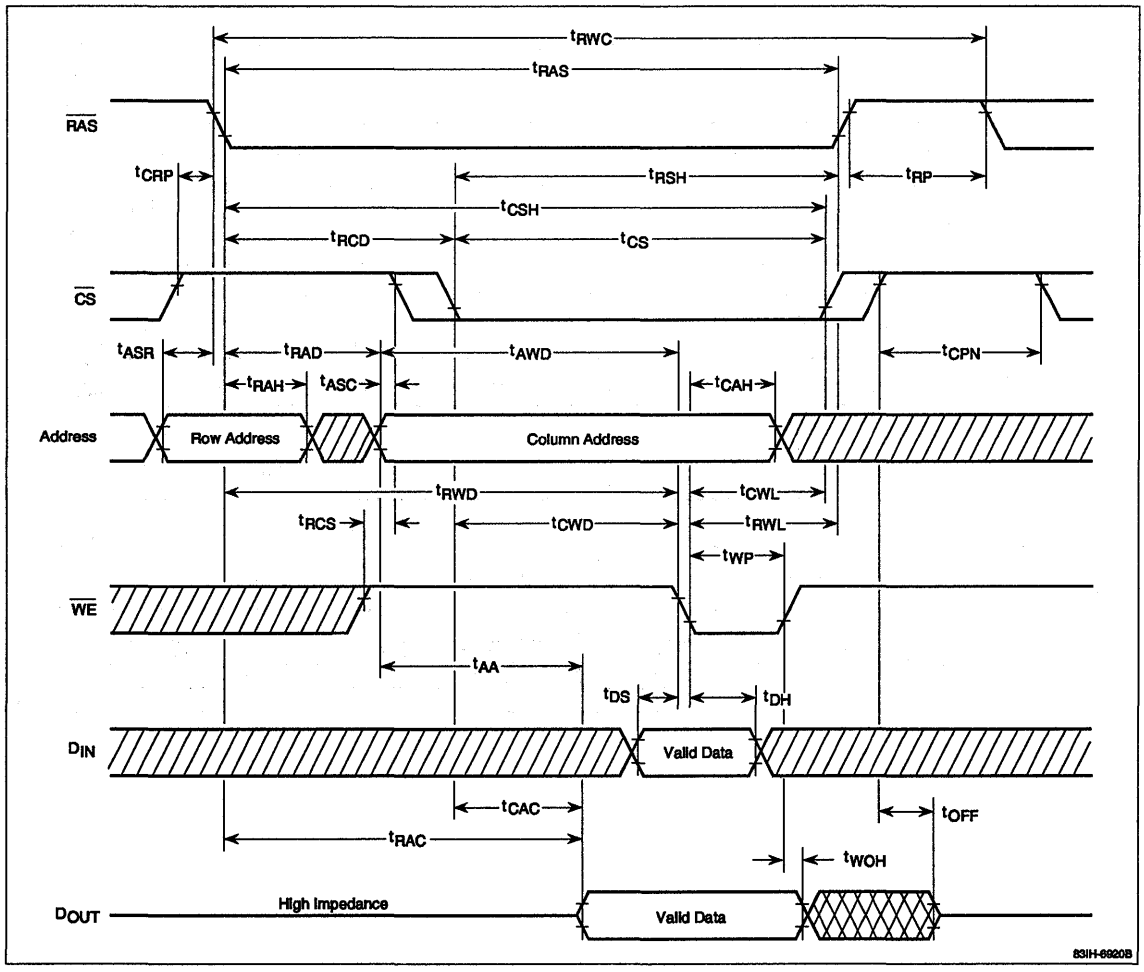
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



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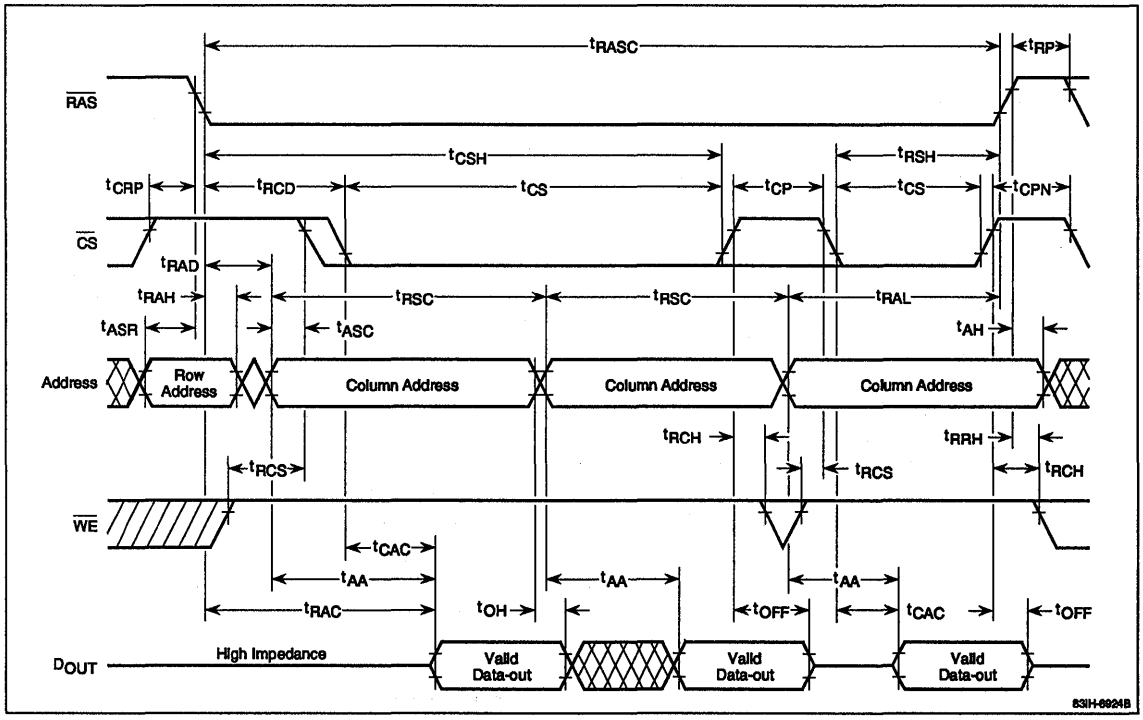
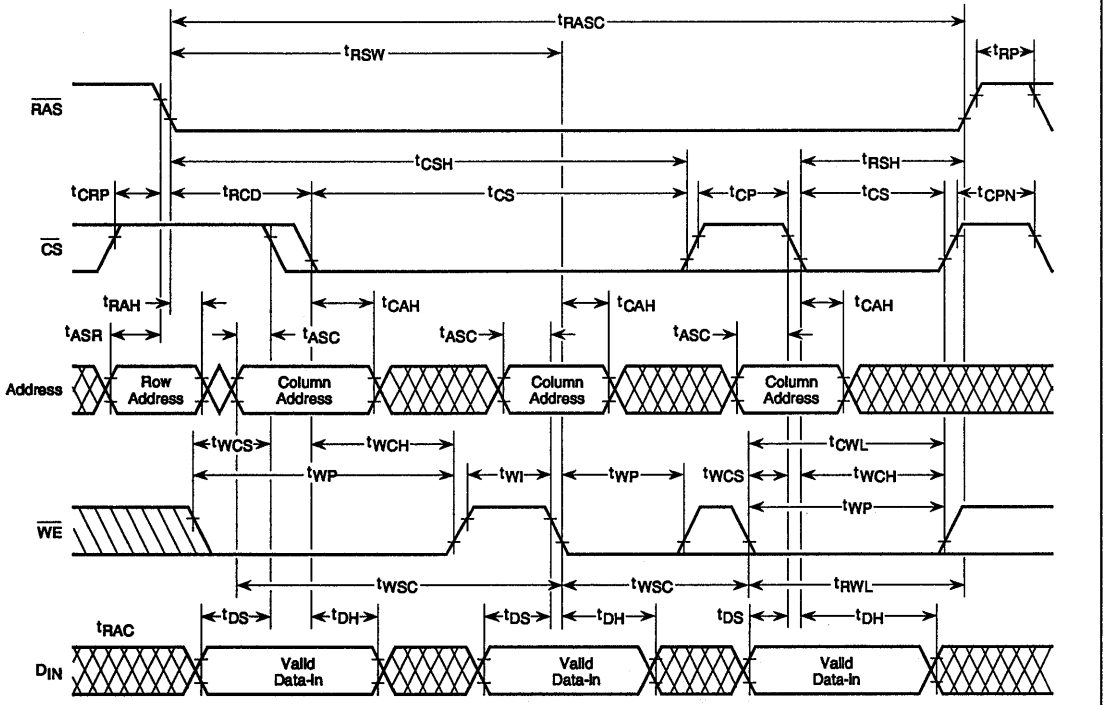
Timing Waveforms (cont)

Static-Column Read Cycle



Timing Waveforms (cont)

Static-Column Early Write Cycle



Notes:

[1] D_{OUT} = high impedance.

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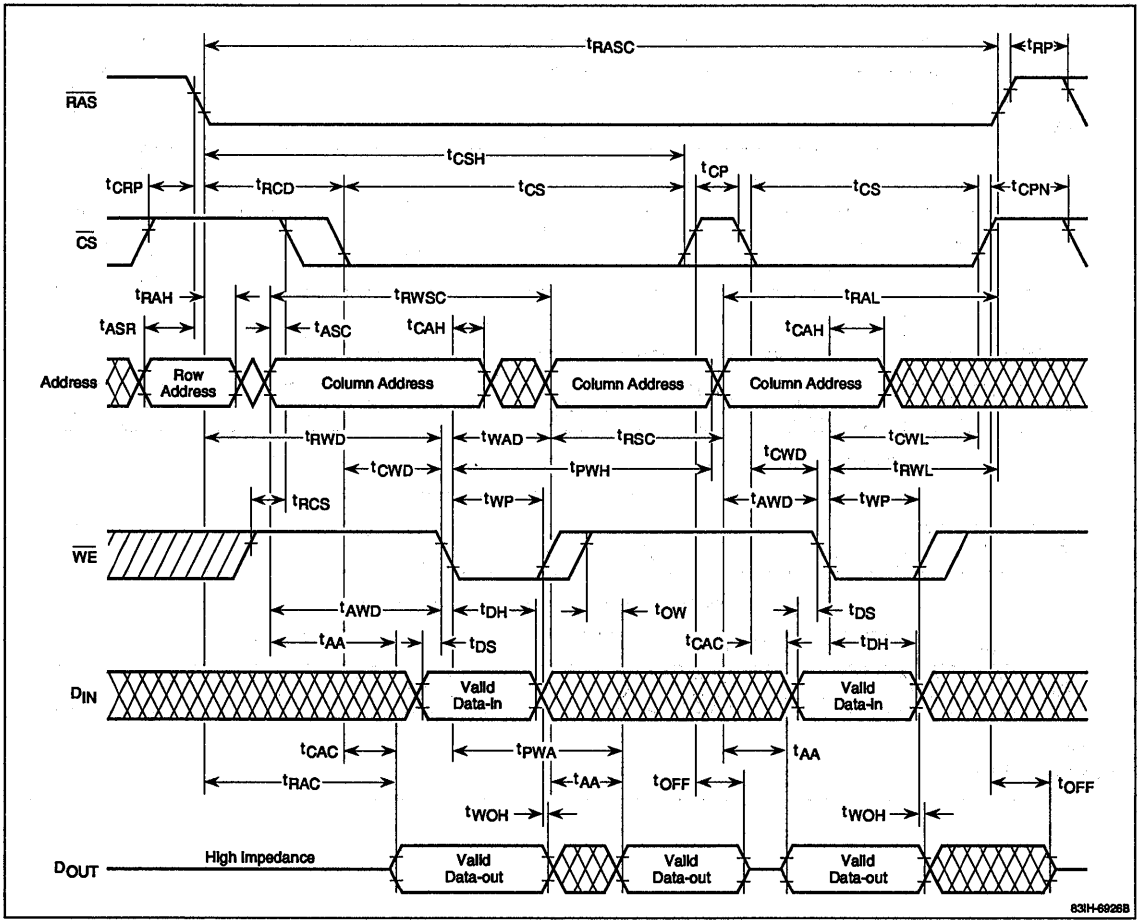
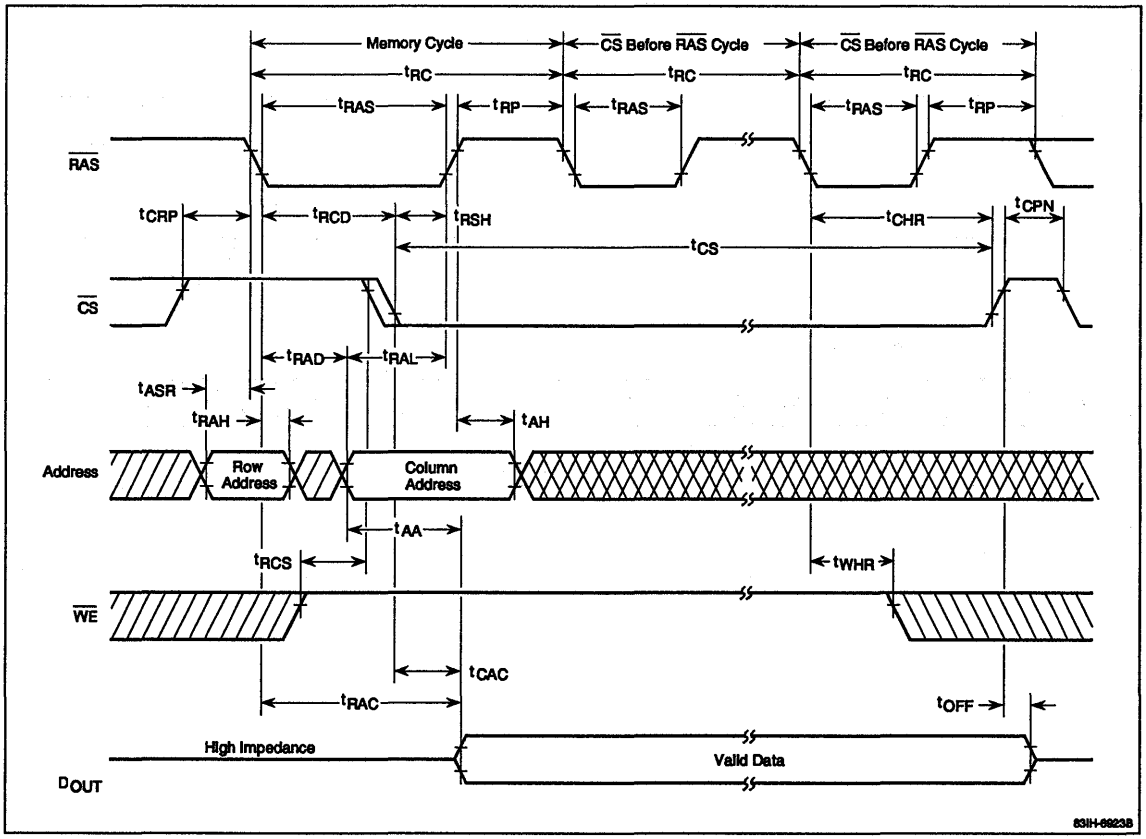
Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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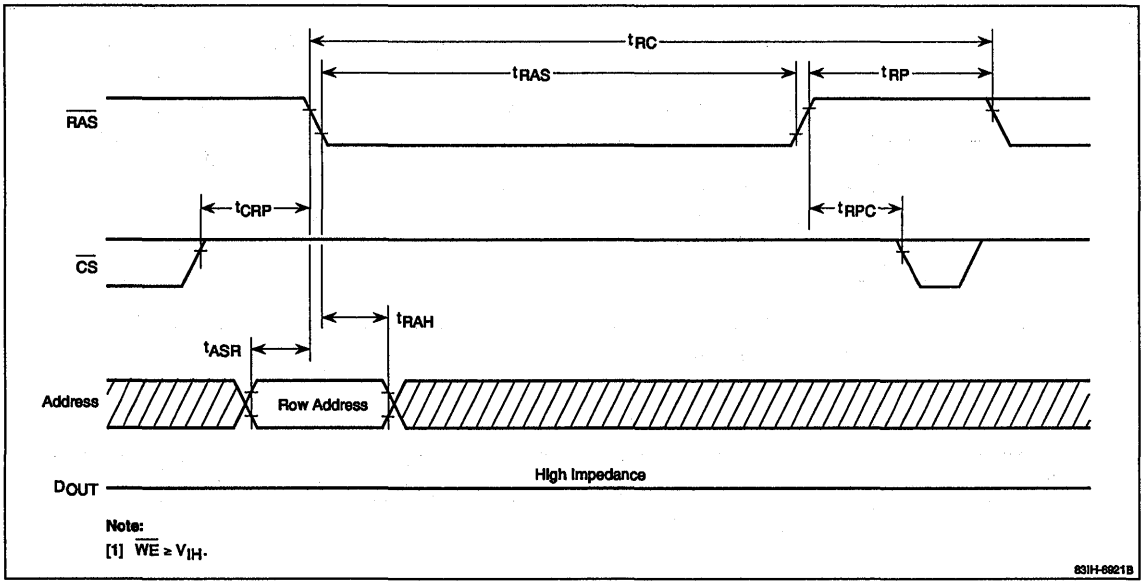
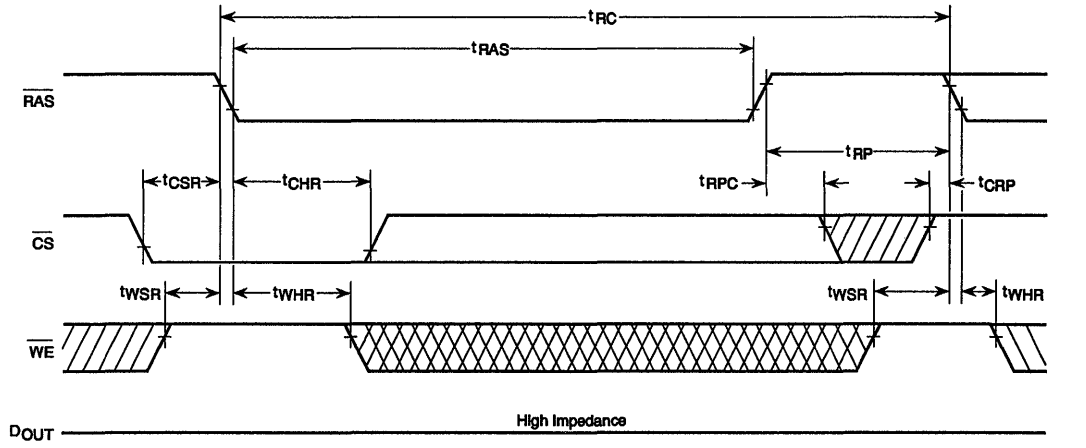
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Timing Waveforms (cont)

$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



Note:

[1] Address = don't care.

83IH-6922B

μPD424400, 424400A/L, 42S4400A/L
1,048,576 x 4-Bit Dynamic CMOS RAM

Description

The devices listed below are fast-page dynamic RAMs organized as 1,048,576 words by 4 bits and designed to operate from a single power supply.

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
Second-generation products	
424400-xx	+5 V
424400-xxL	+5 V; low-power
Third-generation products	
424400A-xx	+5 V
42S4400A-xx	+5 V; self-refresh, low-power
424400L-Axx	+3.3 V
42S4400L-Axx	+3.3 V; self-refresh, low-power

-xx indicates speed grade (RAS access time).

Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1024 address combinations of A_0 - A_9 during a 16-ms refresh period.

The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

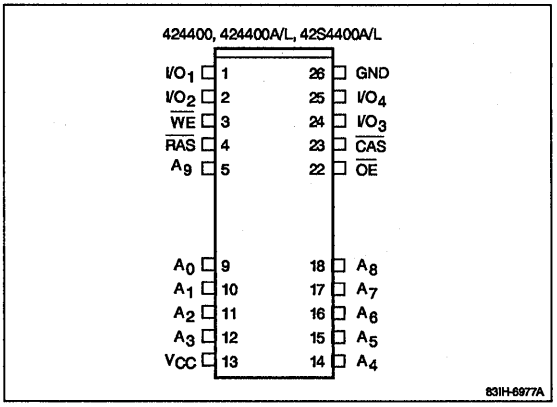
- 1,048,576 by 4-bit organization
- Single +5-volt power supply
- Fast-page option
- Self-refresh option (slow internal automatic refresh)
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- 26/20-pin SOJ, 20-pin ZIP, and 26/20-pin TSOP plastic packaging

Pin Identification

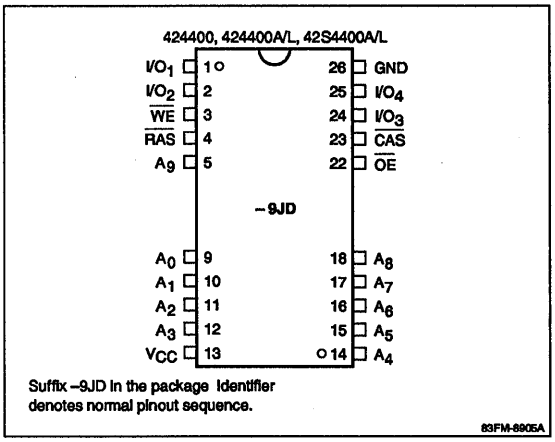
Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Pin Configurations

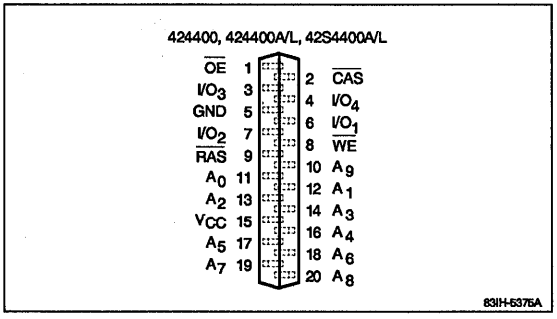
26/20-Pin Plastic SOJ



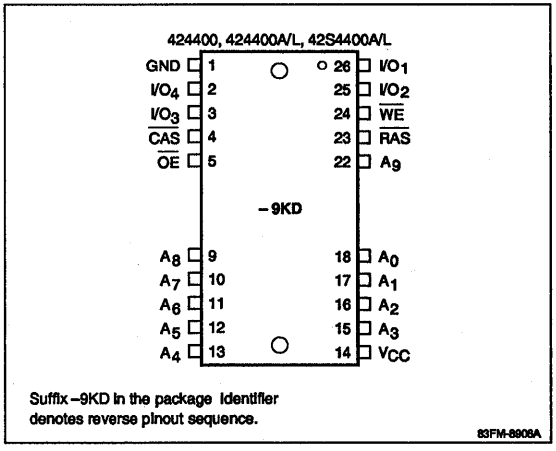
26/20-Pin Plastic TSOP (Normal Pinouts)



20-Pin Plastic ZIP



26/20-Pin Plastic TSOP (Reverse Pinouts)



Ordering Information, μPD424400 (+ 5 V; standard version; 2nd-generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Power Option	Package
μPD424400LA-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic SOJ (300-mil)
LA-70	70 ns	140 ns	45 ns		
LA-80	80 ns	160 ns	50 ns		
μPD424400LA-60L	60 ns	120 ns	40 ns	Low-power	
LA-70L	70 ns	140 ns	45 ns		
LA-80L	80 ns	160 ns	50 ns		
μPD424400V-60	60 ns	120 ns	40 ns	Standard	20-pin plastic ZIP
V-70	70 ns	140 ns	45 ns		
V-80	80 ns	160 ns	50 ns		
μPD424400V-60L	60 ns	120 ns	40 ns	Low-power	
V-70L	70 ns	140 ns	45 ns		
V-80L	80 ns	160 ns	50 ns		
μPD424400GS-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic TSOP (normal pinouts)
GS-70	70 ns	140 ns	45 ns		
GS-80	80 ns	160 ns	50 ns		
μPD424400GS-60L	60 ns	120 ns	40 ns	Low-power	
GS-70L	70 ns	140 ns	45 ns		
GS-80L	80 ns	160 ns	50 ns		
μPD424400GSM-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic TSOP (reverse pinouts))
GSM-70	70 ns	140 ns	45 ns		
GSM-80	80 ns	160 ns	50 ns		
μPD424400GSM-60L	60 ns	120 ns	40 ns	Low-power	
GSM-70L	70 ns	140 ns	45 ns		
GSM-80L	80 ns	160 ns	50 ns		

Ordering Information, μPD424400A (+ 5 V; standard version; 3rd-generation product)

Part Number	RAS Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD424400ALA-50	50 ns	100 ns	35 ns	26/20-pin plastic SOJ (300-mil)
LA-60	60 ns	120 ns	40 ns	
LA-70	70 ns	140 ns	45 ns	
LA-80	80 ns	160 ns	50 ns	
μPD424400AV-50	50 ns	100 ns	35 ns	20-pin plastic ZIP
V-60	60 ns	120 ns	40 ns	
V-70	70 ns	140 ns	45 ns	
V-80	80 ns	160 ns	50 ns	
μPD424400AGS-50	50 ns	100 ns	35 ns	26/20-pin plastic TSOP (normal pinouts)
GS-60	60 ns	120 ns	40 ns	
GS-70	70 ns	140 ns	45 ns	
GS-80	80 ns	160 ns	50 ns	
μPD424400AGSM-50	50 ns	100 ns	35 ns	26/20-pin plastic TSOP (reverse pinouts)
GSM-60	60 ns	120 ns	40 ns	
GSM-70	70 ns	140 ns	45 ns	
GSM-80	80 ns	160 ns	50 ns	

Ordering Information, μPD42S4400A (+ 5 V; self-refresh, low-power version; 3rd-generation product)

Part Number	RAS Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Self-Refresh Current (max)	Package
μPD42S4400ALA-50	50 ns	100 ns	35 ns	200 μA	26/20-pin plastic SOJ (300-mil)
LA-60	60 ns	120 ns	40 ns		
LA-70	70 ns	140 ns	45 ns		
LA-80	80 ns	160 ns	50 ns		
μPD42S4400AV-50	50 ns	100 ns	35 ns	200 μA	20-pin plastic ZIP
V-60	60 ns	120 ns	40 ns		
V-70	70 ns	140 ns	45 ns		
V-80	80 ns	160 ns	50 ns		
μPD42S4400AGS-50	50 ns	100 ns	35 ns	200 μA	26/20-pin plastic TSOP (normal pinouts)
GS-60	60 ns	120 ns	40 ns		
GS-70	70 ns	140 ns	45 ns		
GS-80	80 ns	160 ns	50 ns		
μPD42S4400AGSM-50	50 ns	100 ns	35 ns	200 μA	26/20-pin plastic TSOP (reverse pinouts)
GSM-60	60 ns	120 ns	40 ns		
GSM-70	70 ns	140 ns	45 ns		
GSM-80	80 ns	160 ns	50 ns		

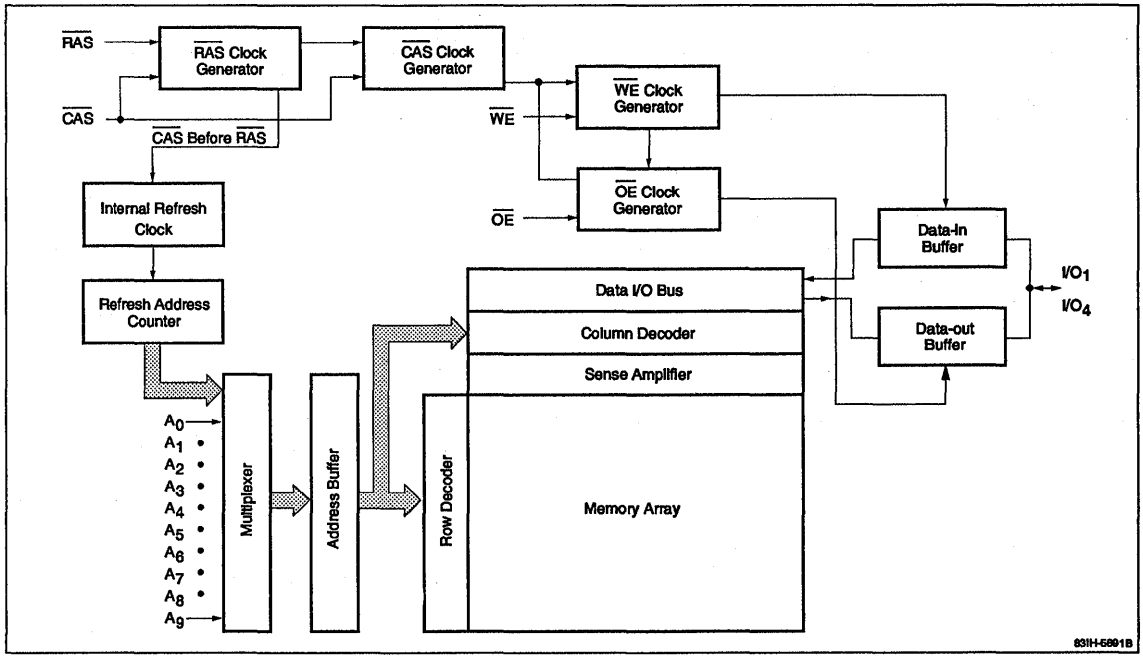
Ordering Information, μPD424400L (+ 3.3 V; standard version; 3rd-generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD424400LLA-A70	70 ns	140 ns	45 ns	26/20-pin plastic SOJ (300-mil)
LA-A80	80 ns	160 ns	50 ns	
μPD424400LV-A70	70 ns	140 ns	45 ns	20-pin plastic ZIP
V-A80	80 ns	160 ns	50 ns	
μPD424400LGS-A70	70 ns	140 ns	45 ns	26/20-pin plastic TSOP (normal pinouts)
GS-A80	80 ns	160 ns	50 ns	
μPD424400LGSM-A70	70 ns	140 ns	45 ns	26/20-pin plastic TSOP (reverse pinouts)
GSM-A80	80 ns	160 ns	50 ns	

Ordering Information, μPD42S4400L (+ 3.3 V; self-refresh, low-power version; 3rd-generation product)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Self-Refresh Current (max)	Package
μPD42S4400LLA-A70	70 ns	140 ns	45 ns	100 μA	26/20-pin plastic SOJ (300-mil)
LA-A80	80 ns	160 ns	50 ns		
μPD42S4400LV-A70	70 ns	140 ns	45 ns	100 μA	20-pin plastic ZIP
V-A80	80 ns	160 ns	50 ns		
μPD42S4400LGS-A70	70 ns	140 ns	45 ns	100 μA	26/20-pin plastic TSOP (normal pinouts)
GS-A80	80 ns	160 ns	50 ns		
μPD42S4400LGSM-A70	70 ns	140 ns	45 ns	100 μA	26/20-pin plastic TSOP (reverse pinouts)
GSM-A80	80 ns	160 ns	50 ns		

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
5-volt devices	50 mA
3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_4

DC Characteristics; 5-Volt Devices

Recommended operating conditions unless otherwise noted.

		424400, 424400A		42S4400A			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0		2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
			1.0		0.2	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10	10	−10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	−10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		2.4		V	I_{OH} = −5 mA
Self-refresh current	I_{CC7}	Not applicable			200	μA	I_O = 0 mA; all I/O and input pins ≥ V_{CC} −0.2 V or ≤ 0.2 V or open; t_{RAS} ≥ 100 μs; 1024 refresh cycles must be performed within 16 ms before entering self-refresh and after exiting self-refresh

5d

DC Characteristics; 3.3-Volt Devices

Recommended operating conditions unless otherwise noted.

		424400L		42S4400L			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0		0.5	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
			0.5		0.1	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−5	5	−5	5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−5	5	−5	5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4		0.4	V	I_{OL} = 2 mA
Output voltage, high	V_{OH}	2.4		2.4		V	I_{OH} = −2 mA
Self-refresh current	I_{CC7}	Not applicable			100	μA	I_O = 0 mA; all I/O and input pins ≥ V_{CC} −0.2 V or ≤ 0.2 V or open; t_{RAS} ≥ 100 μs; 1024 refresh cycles must be performed within 16 ms before entering self-refresh and after exiting self-refresh

Low-Power Battery Backup (Low-Power and Self-Refresh Versions Only)

Symbol	424400-xxL	42S4400A	42S4400L	Unit	t_{RAS}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6} (max)	500	300	150	μA	≤ 1 μs	1024 refresh cycles (min) every 128 ms; $\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V or ≤ 0.2 V, as appropriate; I/O open; all other inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; D_{IN}, $\overline{WE}$, $\overline{OE}$, Addresses ≥ V_{CC} – 0.2 V or ≤ 0.2 V; I/O open
	300	200	100	μA	≤ 200 ns		

Recommended Operating Conditions

Parameter	Symbol	5-Volt Devices Min	Typ	Max	3.3-Volt Devices Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–1.0		0.8	–0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

AC Characteristics

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	-50 Min	-50 Max	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5 V)		100		120		100		90	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC1} (+3.3 V)						70		60	mA	
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5 V)		100		120		100		90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC3} (+3.3 V)						70		60	mA	
Operating current, fast-page cycle, average	I_{CC4} (+5 V)		90		90		80		70	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
	I_{CC4} (+3.3 V)						60		50	mA	
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5 V)		100		120		100		90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC5} (+3.3 V)						70		60	mA	
Access time from column address	t_{AA}		25		30		35		40	ns	(Notes 3, 4, 7, 8, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		30		35		40		45	ns	(Notes 3, 4, 7, 11)
Column address setup time	t_{ASC}	0	5	0	5	0	10	0	15	ns	(Note 9)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		50		55		65		ns	(Note 16)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		15		15		20		20	ns	(Notes 3, 4, 7, 8, 11)
Column address hold time	t_{CAH}	15		15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	10		15		15		15		ns	

AC Characteristics (cont)

Parameter	Symbol	-50		-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ hold (CBR self-refresh)	t_{CHS}	−50		−50		−50		−50		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		0		ns	(Note 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10	10	10	10	10	15	10	20	ns	(Note 9)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		40		45		ns	(Note 16)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		15		ns	
Data-in hold time	t_{DH}	10		15		15		15		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 15)
Access time from $\overline{OE}$	t_{OEA}		15		15		20		20	ns	(Notes 3, 4, 7, 8, 11)
$\overline{OE}$ delay data time	t_{OED}	15		15		15		20		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	0	20	ns	(Note 10)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	15	0	20	ns	(Note 10)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		0		ns	(Notes 6, 7)
Fast-page cycle time	t_{PC}	35		40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	80		85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	17	40	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	25		30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ width (CBR self-refresh)	t_{RASS}	100		100		100		100		μs	

5d

AC Characteristics (cont)

		-50		-60		-70		-80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Random read or write cycle time	t_{RC}	100		120		140		160		ns	(Note 6)
						130		150		ns	(Notes 6, 18)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	35	20	40	20	50	25	60	ns	(Notes 8, 9)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9 (Note 19)
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		40		60		70		ns	
						50		60		ns	(Note 18)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ precharge (CBR self-refresh)	t_{RPS}	90		110		130		150		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	15		15		20		20		ns	
Read-write cycle time	t_{RWC}	145		165		185		210		ns	(Note 6)
						175		200		ns	(Notes 6, 18)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	75		80		90		105		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	10		10		15		15		ns	(Note 14)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		15		ns	
Write command pulse width	t_{WP}	10		10		15		15		ns	(Note 14)
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

AC Characteristics

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) For random read cycles, access time is defined as follows.

Input Conditions	Access Time
$t_{RAD} \leq t_{RAD}$ (max), $t_{RCD} \leq t_{RCD}$ (max)	t_{RAC}
$t_{RAD} \geq t_{RAD}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{RAD} \geq t_{RAD}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

The above access times assume that $\overline{OE}$ has been active t_{OEA} (max) prior to when data is expected on the output.

(9) t_{RCD} (max), t_{RAD} (max), t_{ASC} (max) and t_{CP} (max) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA}, t_{CAC}, or t_{ACP}) is to be used for determining when output data will be available.

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(11) For fast-page read operation, access time is defined follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

The above access times assume that $\overline{OE}$ has been active t_{OEA} (max) prior to when data is expected on the output.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

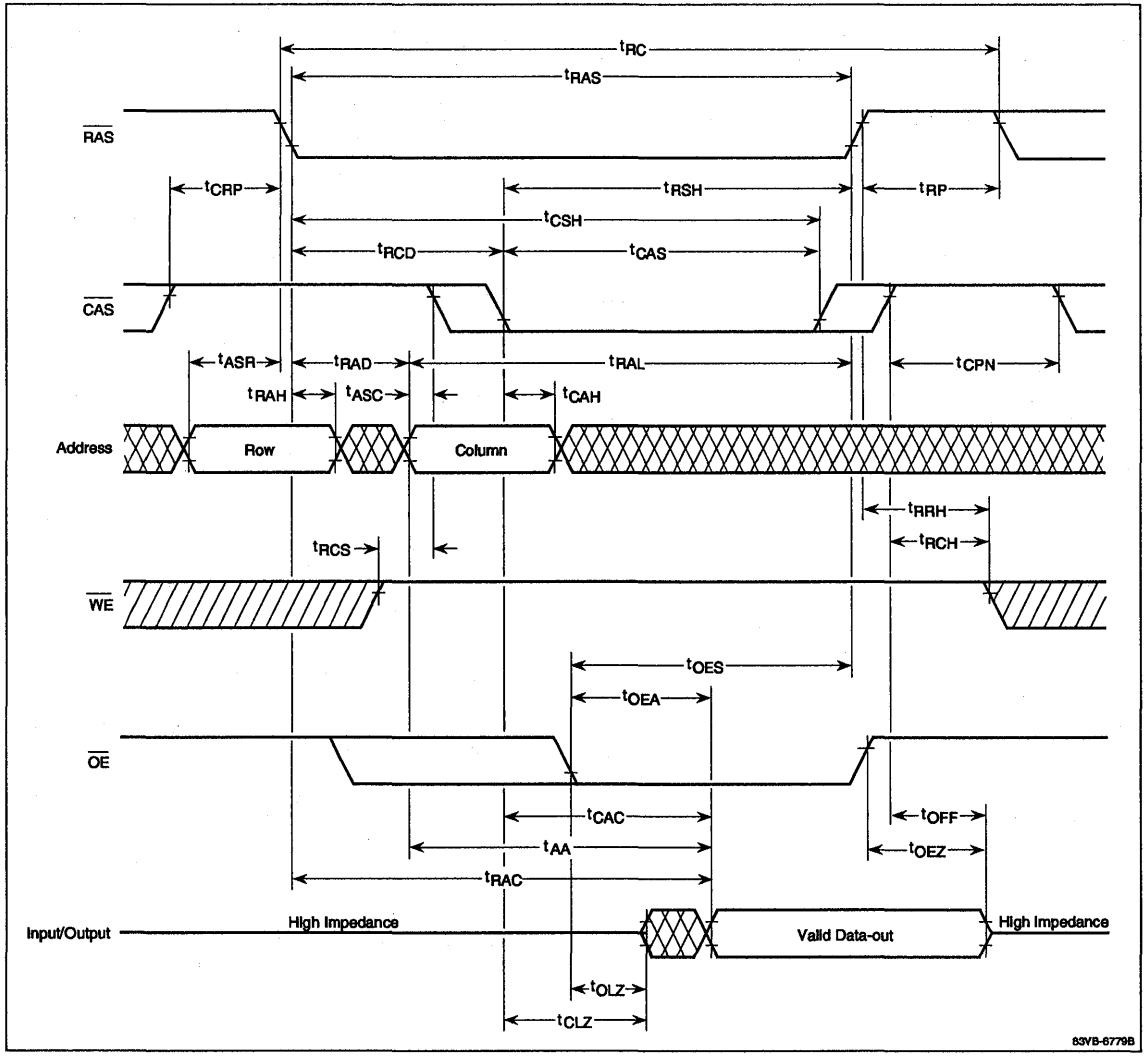
(18) Applies to μPD424400L and μPD42S4400L.

(19) 1024 refresh cycles must be performed within 16 ms before entering self-refresh and after exiting self-refresh.

5d

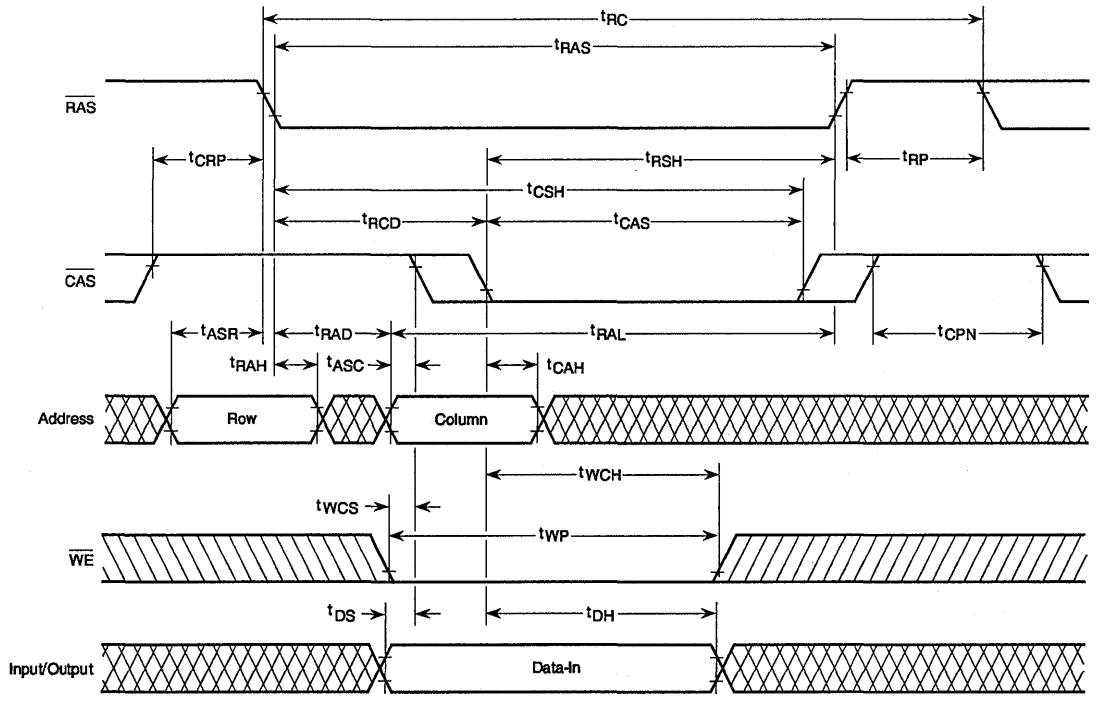
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

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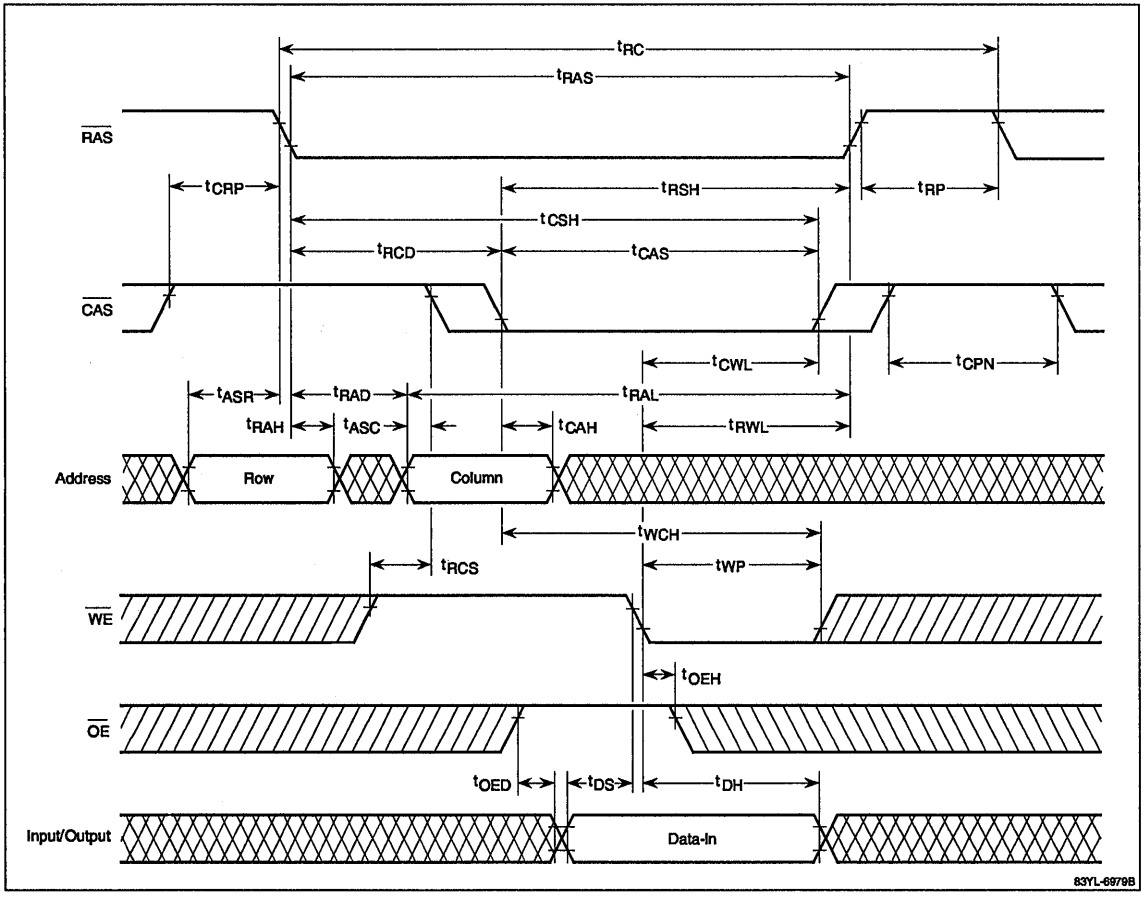
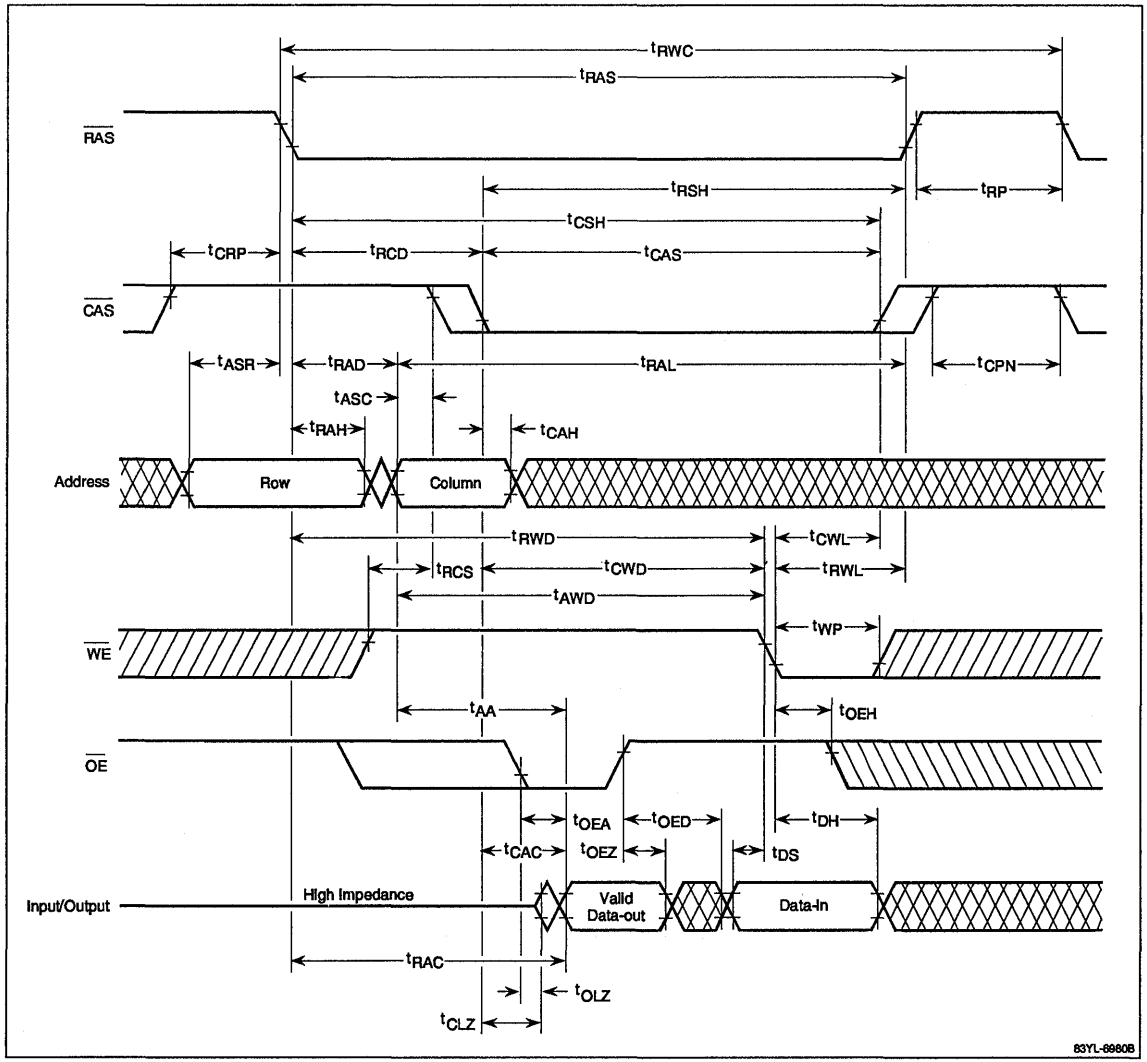
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

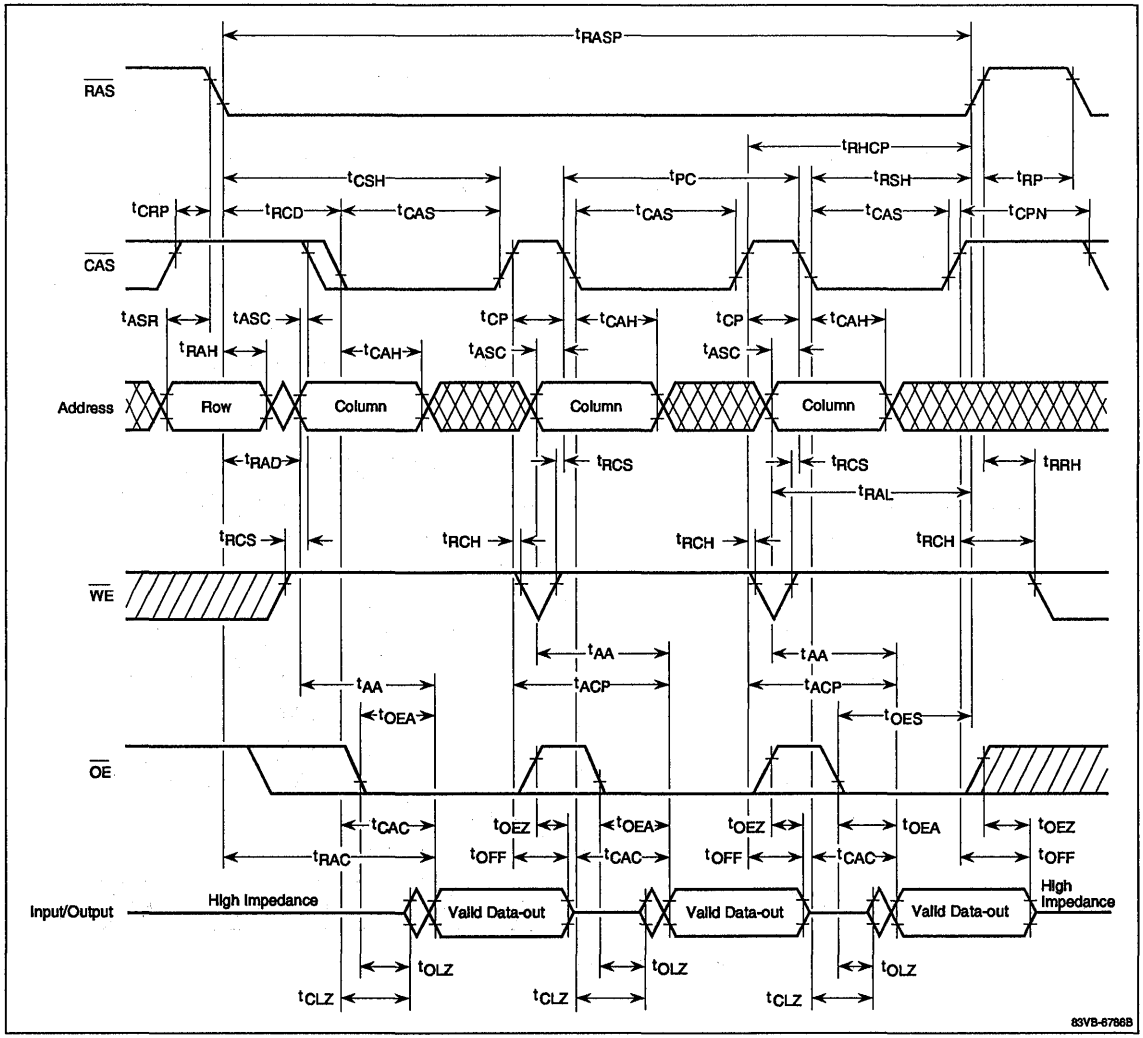
Read-Write/Read-Modify-Write Cycle



5d

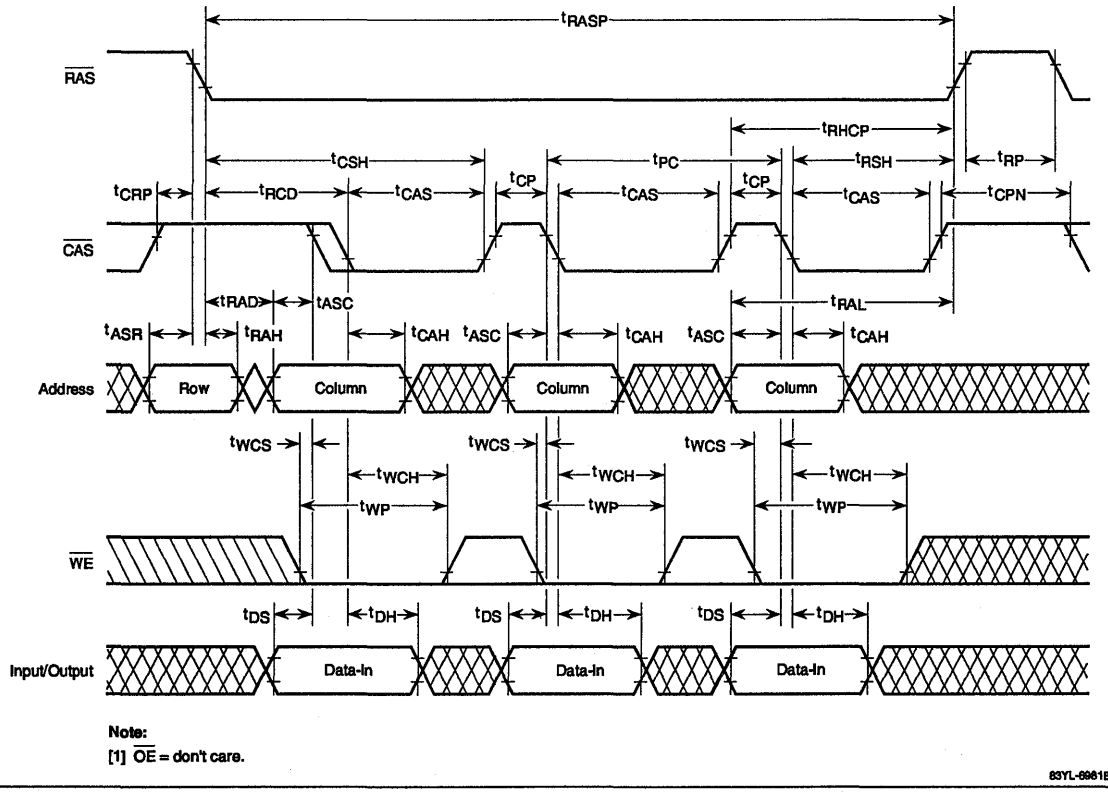
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

83YL-6981B

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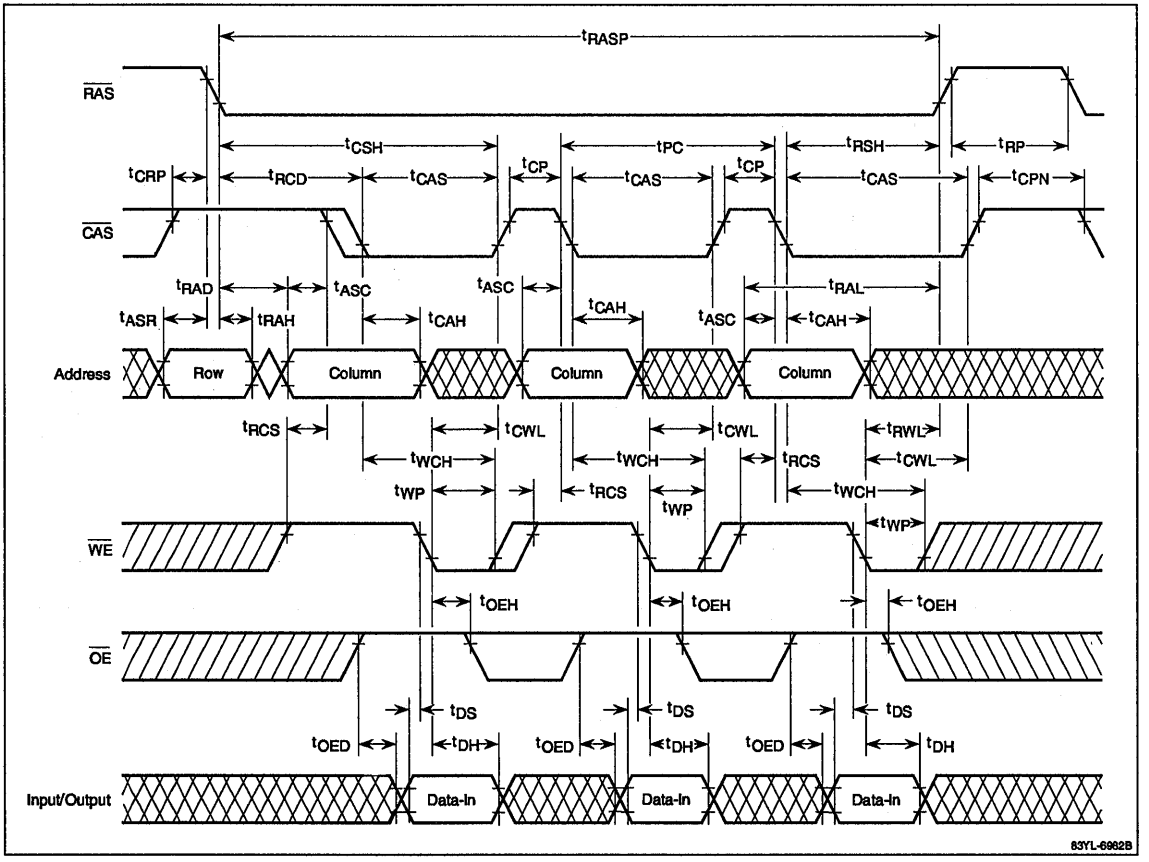
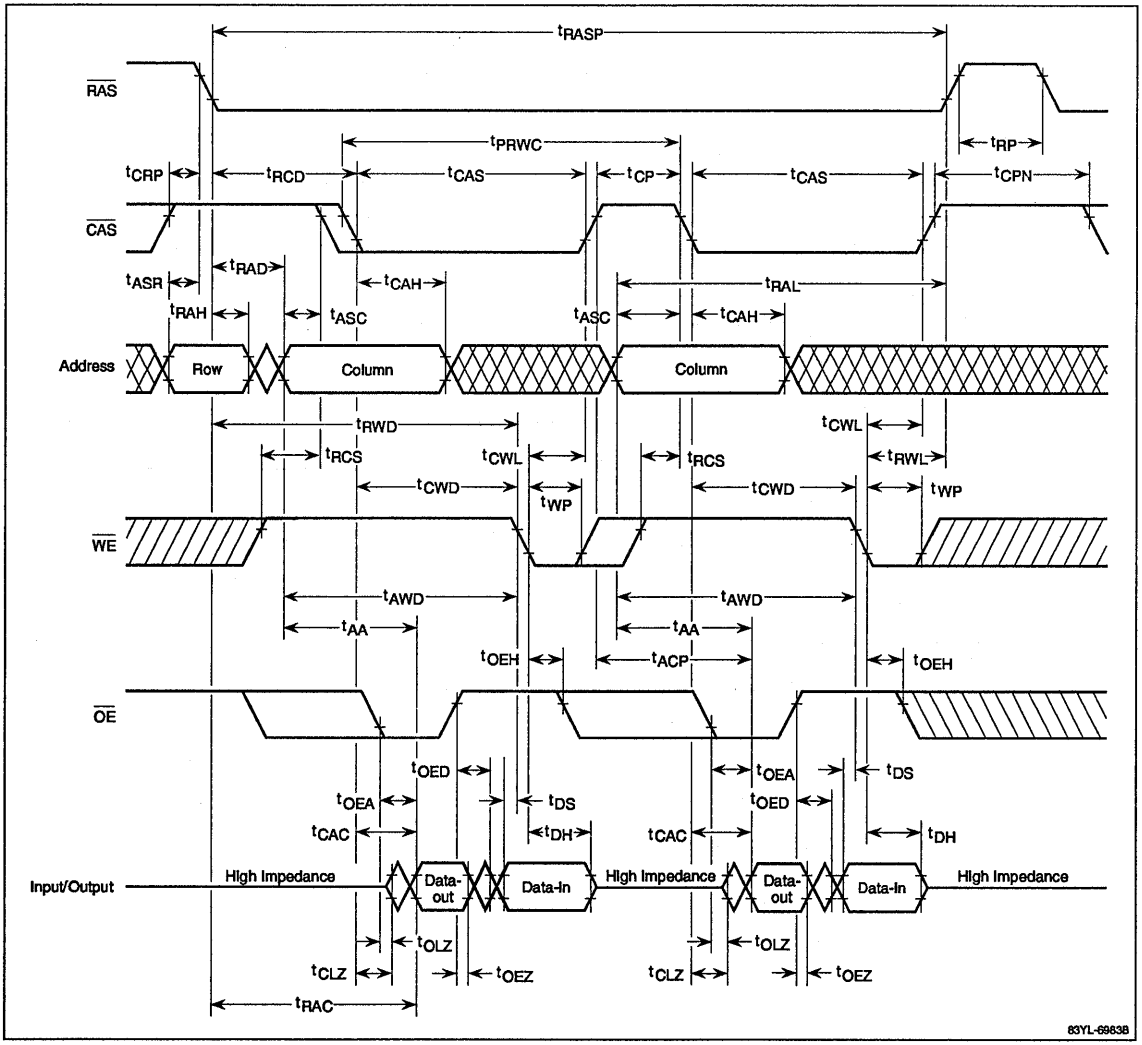
Timing Waveforms (cont)

Fast-Page Late Write Cycle



Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



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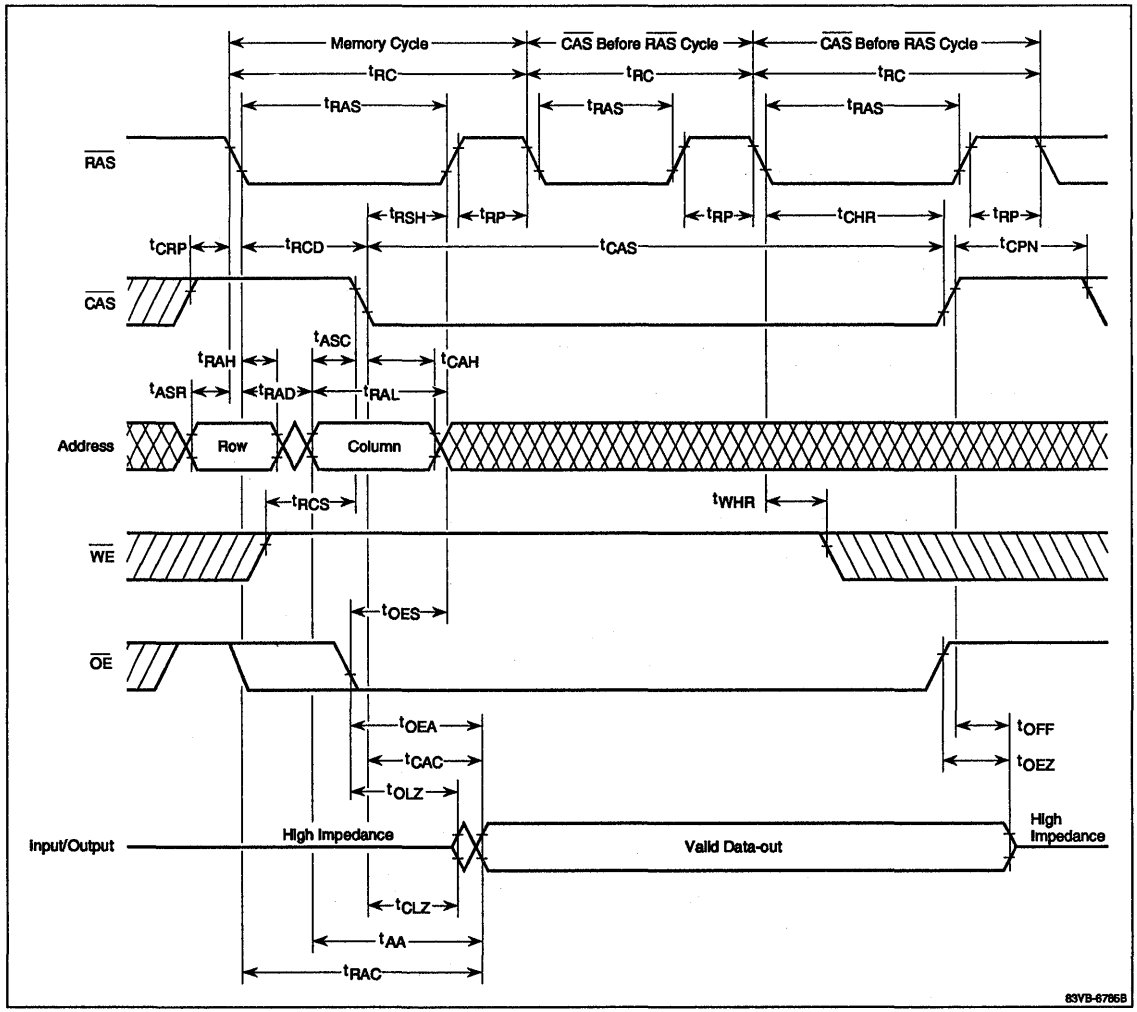
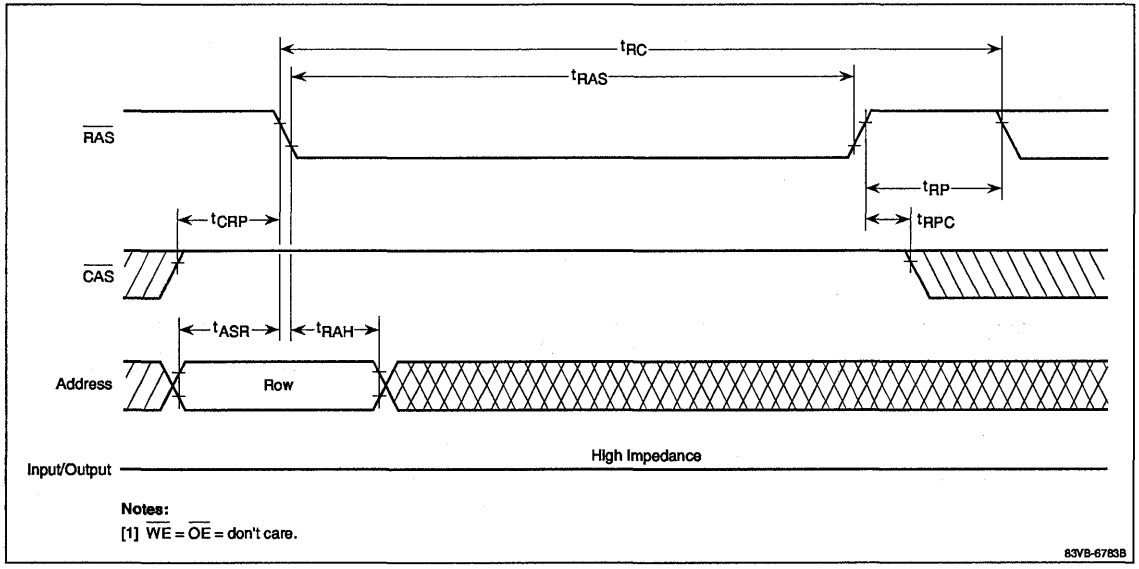
Timing Waveforms (cont)

Hidden Refresh Cycle



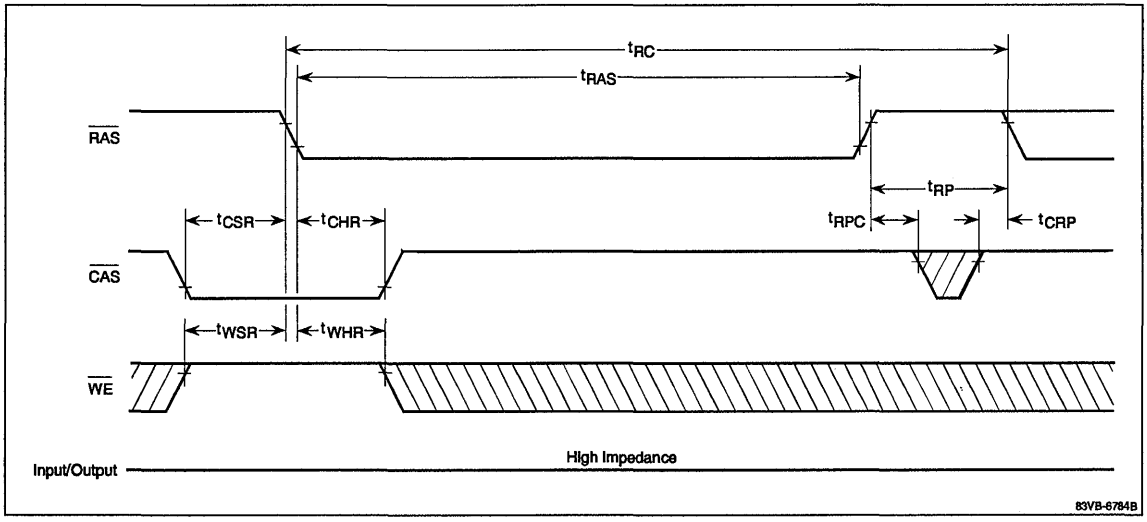
Timing Waveforms (cont)

$\overline{\text{RAS}}$-Only Refresh Cycle



Notes:
[1] $\overline{\text{WE}}$ = $\overline{\text{OE}}$ = don't care.

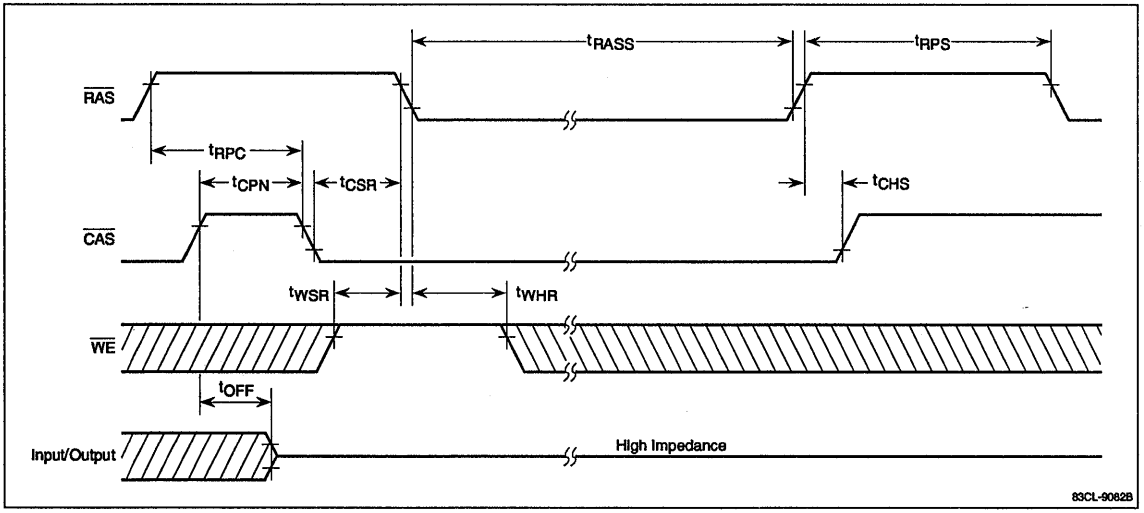
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



5d

Timing Waveforms (cont)

CBR Self-Refresh Cycle



μPD424402
1,048,576 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424402 is a static-column dynamic RAM organized as 1,048,576 by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. Data outputs return to high impedance when $\overline{CS}$ goes high. Static column read and write cycles can be executed by cycling $\overline{CS}$.

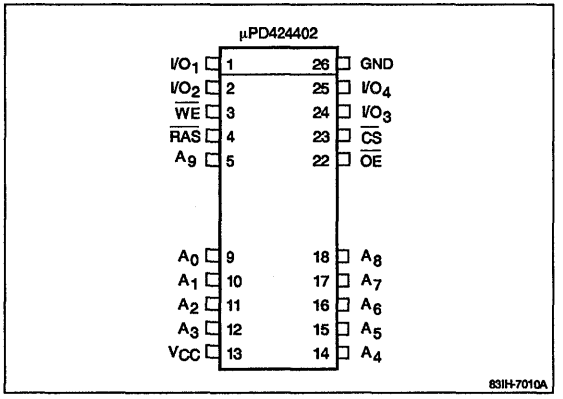
Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1,024 address combinations of A_0 through A_9 during a 16-ms refresh period.

Features

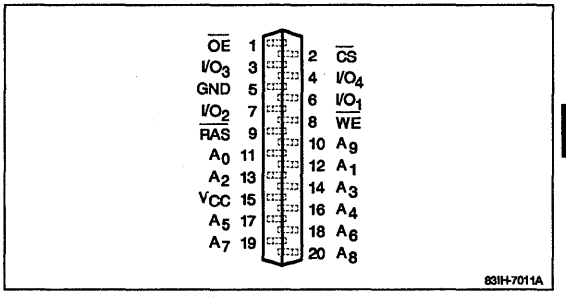
- 1,048,576 by 4-bit organization
- Single +5-volt power supply
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- 26/20-pin plastic SOJ, 26/20-pin plastic TSOP, or 20-pin plastic ZIP packaging

Pin Configurations

26/20-Pin Plastic SOJ



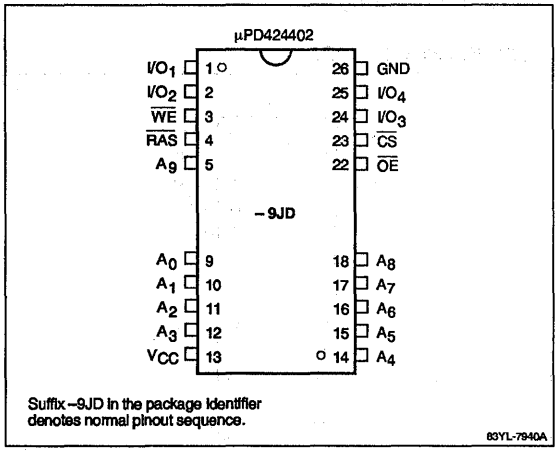
20-Pin Plastic ZIP



5e

Pin Configurations (cont)

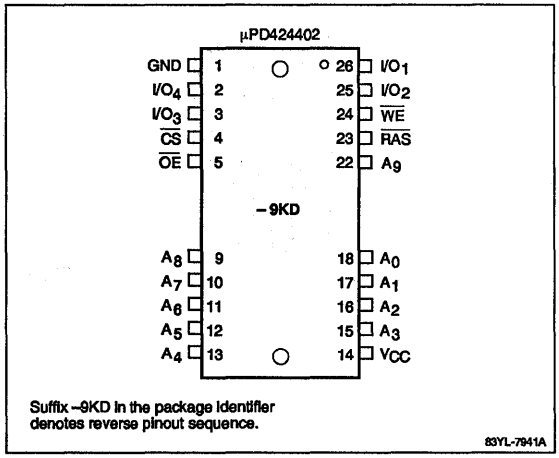
26/20-Pin Plastic TSOP (Normal Pinouts)



Suffix –9JD in the package identifier denotes normal pinout sequence.

83YL-7940A

26/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –9KD in the package identifier denotes reverse pinout sequence.

83YL-7941A

Pin Identification

Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_4

Absolute Maximum Ratings

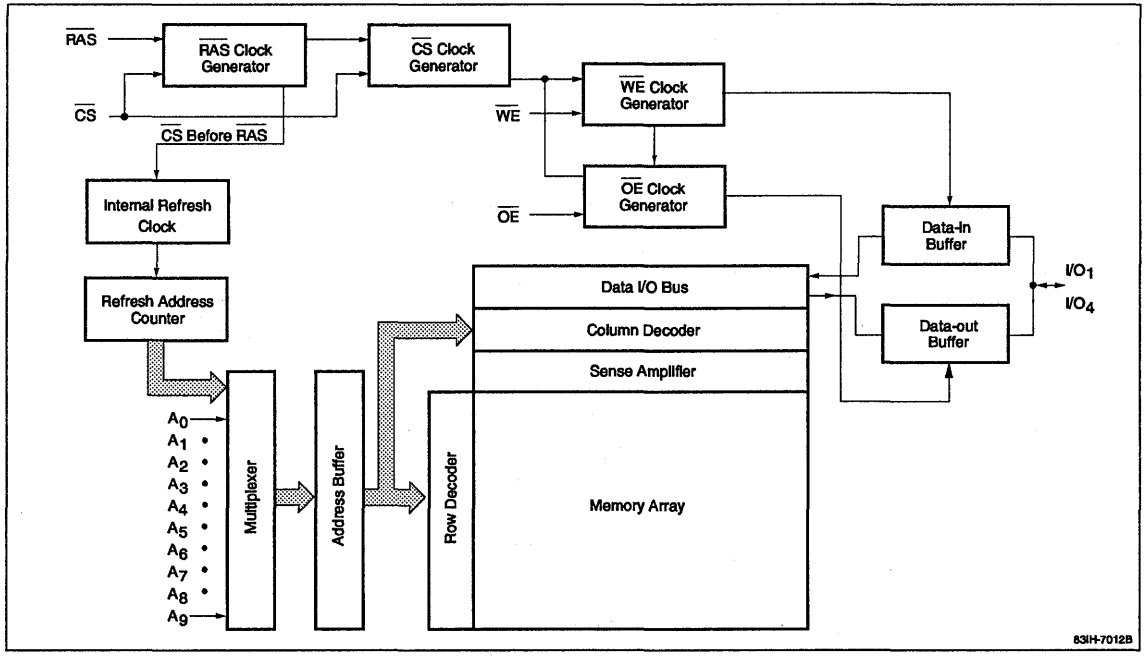
Voltage on any pin relative to GND	–1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	–55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	–1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{IH} (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –5 mA

Low Power Battery Backup (-L Versions Only)

Symbol	Max	Unit	t_{RAS}	$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	500	μA	≤ 1 μs	1024 refresh cycles (min) every 128 ms; $\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} – 0.2 V or ≤ 0.2 V, as appropriate; I/O open; all other inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} – 0.2 V; $\overline{WE}$, $\overline{OE}$, Addresses ≥ V_{CC} – 0.2 V or ≤ 0.2 V; I/O open
	300	μA	≤ 200 ns		

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Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Static-Column Cycle (max)	Power Option	Package
μPD424402LA-60	60 ns	120 ns	35 ns	Standard	26/20-pin plastic SOJ (300 mil)
LA-70	70 ns	140 ns	40 ns		
LA-80	80 ns	160 ns	50 ns		
LA-10	100 ns	190 ns	60 ns		
μPD424402LA-60L	60 ns	120 ns	35 ns	Low power	
LA-70L	70 ns	140 ns	40 ns		
LA-80L	80 ns	160 ns	50 ns		
LA-10L	100 ns	190 ns	60 ns		
μPD424402LB-70	70 ns	140 ns	40 ns	Standard	26/20-pin plastic SOJ (350 mil)
LB-80	80 ns	160 ns	50 ns		
LB-10	100 ns	190 ns	60 ns		
μPD424402LB-70L	70 ns	140 ns	40 ns	Low power	
LB-80L	80 ns	160 ns	50 ns		
LB-10L	100 ns	190 ns	60 ns		
μPD424402V-60	60 ns	120 ns	35 ns	Standard	20-pin plastic ZIP
V-70	70 ns	140 ns	40 ns		
V-80	80 ns	160 ns	50 ns		
V-10	100 ns	190 ns	60 ns		
μPD424402V-60L	60 ns	120 ns	35 ns	Low power	
V-70L	70 ns	140 ns	40 ns		
V-80L	80 ns	160 ns	50 ns		
V-10L	100 ns	190 ns	60 ns		
μPD424402GS-60	60 ns	120 ns	35 ns	Standard	26/20-pin plastic TSOP (normal pinouts)
GS-70	70 ns	140 ns	40 ns		
GS-80	80 ns	160 ns	50 ns		
μPD424402GS-60L	60 ns	120 ns	35 ns	Low power	
GS-70L	70 ns	140 ns	40 ns		
GS-80L	80 ns	160 ns	50 ns		
μPD424402GSM-60	60 ns	120 ns	35 ns	Standard	26/20-pin plastic TSOP (reverse pinouts)
GSM-70	70 ns	140 ns	40 ns		
GSM-80	80 ns	160 ns	50 ns		
μPD424402GSM-60L	60 ns	120 ns	35 ns	Low power	
GSM-70L	70 ns	140 ns	40 ns		
GSM-80L	80 ns	160 ns	50 ns		

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		120		100		90		80	mA	$\overline{RAS}$, $\overline{CS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		120		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
Operating current, static-column cycle, average	I_{CC4}		90		80		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CS}$ cycling; t_{RSC} = t_{RSC} min or t_{WSC} = t_{WSC} min (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		120		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 3, 4, 7, 8)
Column address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		55		65		80		ns	(Note 15)
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		20		ns	
$\overline{CS}$ precharge time, static-column cycle	t_{CP}	10		10		10		10		ns	
$\overline{CS}$ precharge time	t_{CPN}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 11)
$\overline{CS}$ pulse width	t_{CS}	20	100,000	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	20		40		45		55		ns	(Note 15)
Write command referenced to $\overline{CS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 14)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 14)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 10)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 10)
Output hold time for address	t_{OH}	5		5		5		5		ns	
Output enable time from $\overline{WE}$	t_{OW}		25		25		25		30	ns	
Access time from $\overline{WE}$	t_{PWA}		60		70		90		110	ns	(Notes 7, 16)
Column address hold time referenced to $\overline{WE}$	t_{PWH}	60		70		90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, static-column cycle	t_{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	(Note 12)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Address A_0 through A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 12)
Read cycle time	t_{RSC}	35		40		50		60		ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSW}	75		85		95		115		ns	
Read-modify-write cycle time	t_{RWC}	145		185		210		250		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		90		105		130		ns	(Note 15)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Read/write cycle time	t_{RWSC}	65		95		120		145		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
$\overline{WE}$ to column address delay time	t_{WAD}	20	30	22	35	20	45	25	55	ns	(Note 16)
Write command hold time	t_{WCH}	15		15		15		20		ns	(Note 13)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 15)
$\overline{WE}$ command hold time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{WHR}	15		15		15		20		ns	
Write invalid time	t_{WI}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 13)
Write cycle time	t_{WSC}	35		40		50		60		ns	
$\overline{WE}$ command setup time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each static column cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V and V_{OL} = 0.8 V).

(8) If $t_{RCD} \leq$ exceeds t_{RAD} max, then t_{RAC} will increase by the amount t_{RCD} exceeds t_{RCD} (max).

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CS}$ cycles preceded by any cycle.

(12) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(13) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(14) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

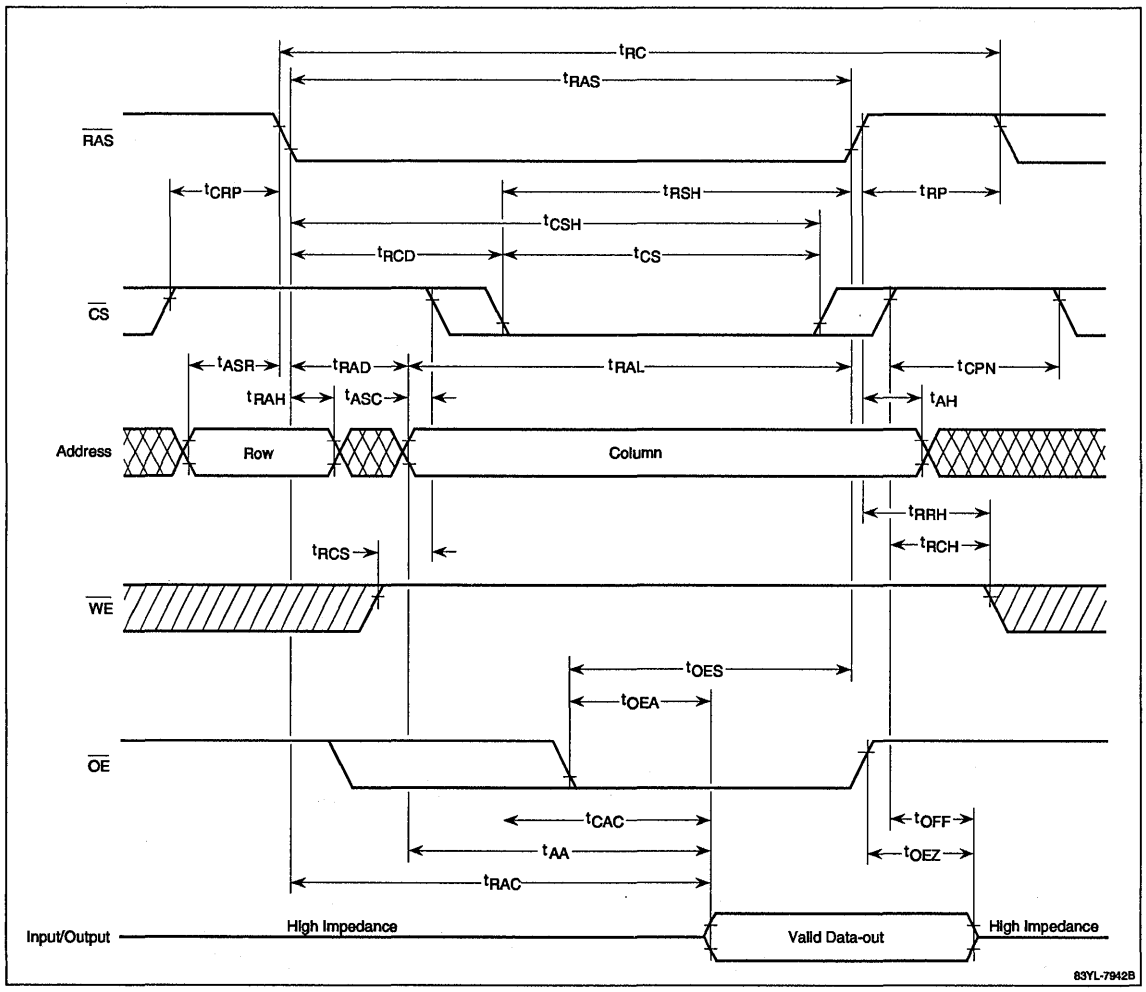
(16) A test mode may be initiated by executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

(17) Assumes $t_{WAD} \leq t_{WAD}$ (max).

5e

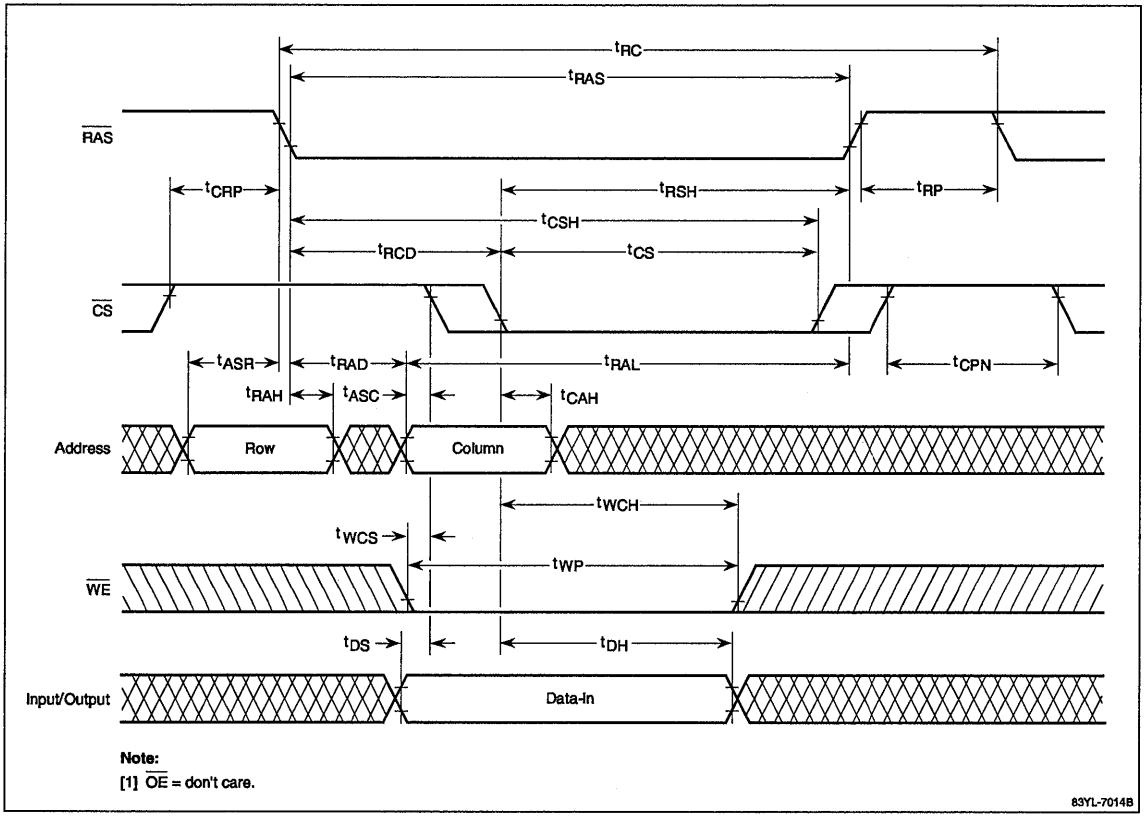
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



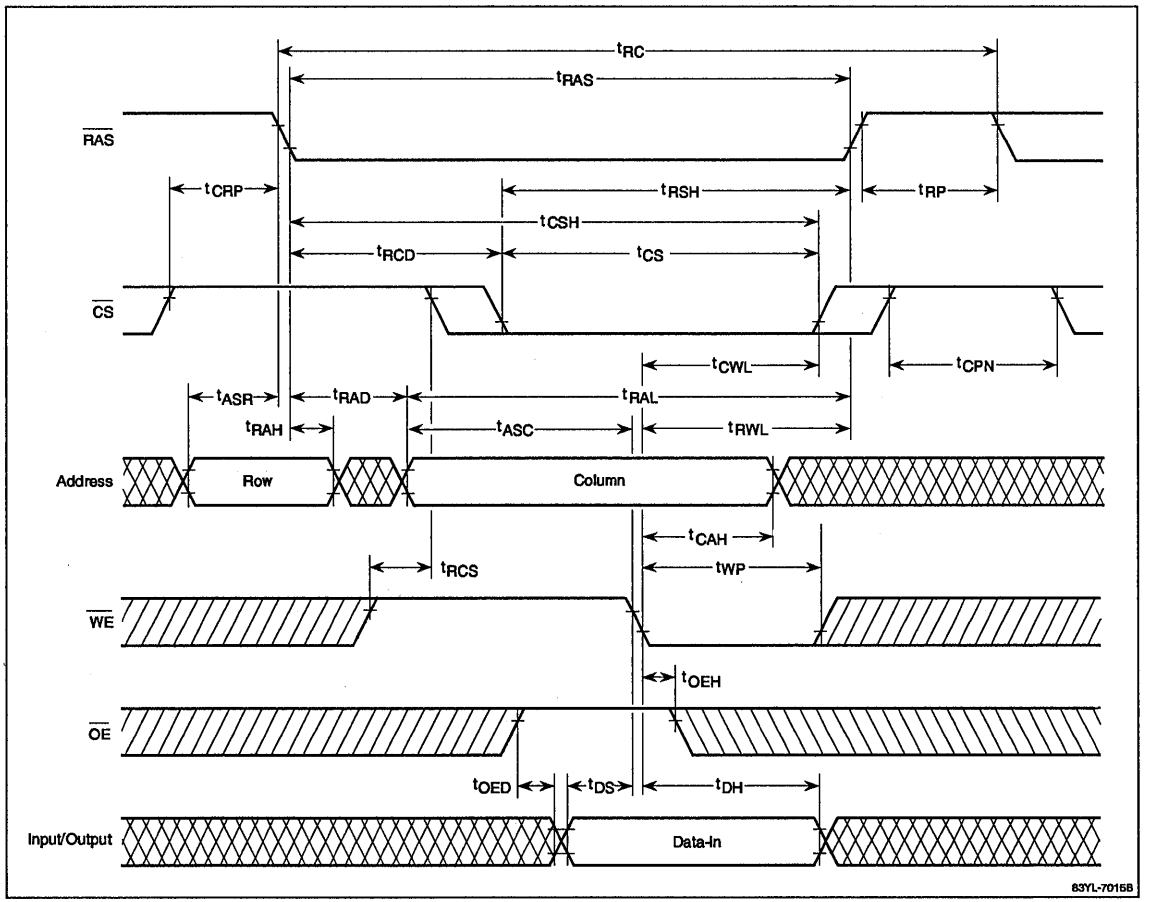
Note:
[1] $\overline{OE}$ = don't care.

83YL-7014B

5e

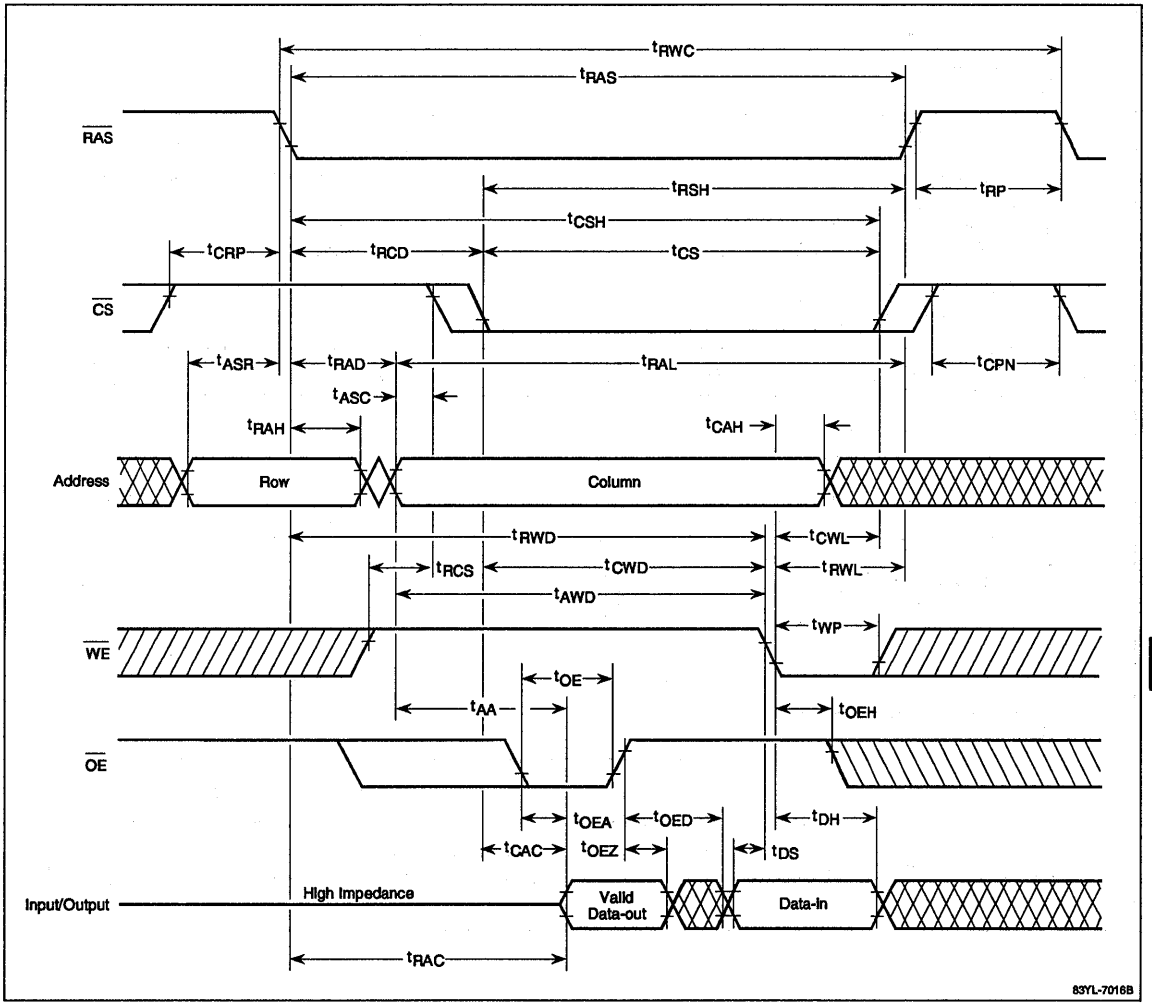
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



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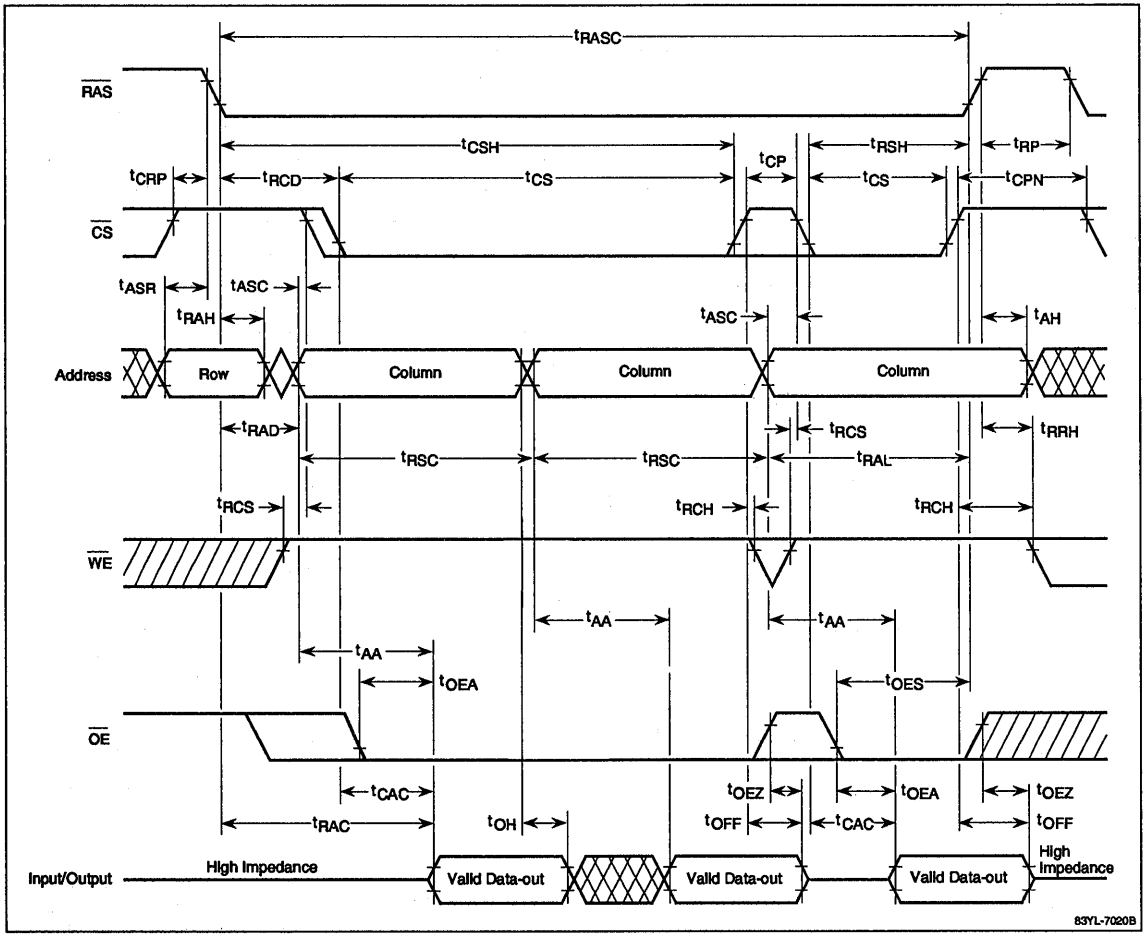
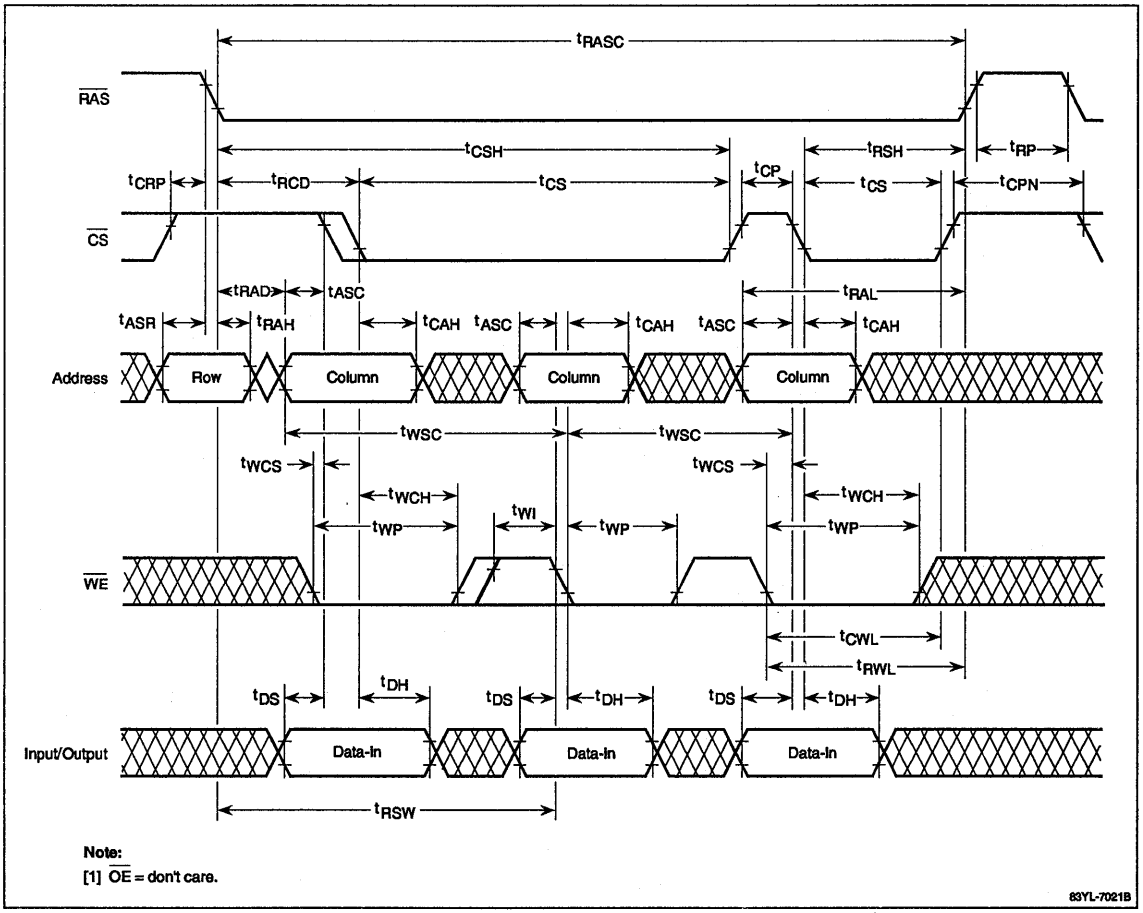
Timing Waveforms (cont)

Static-Column Read Cycle



Timing Waveforms (cont)

Static-Column Early Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

83YL-7021B

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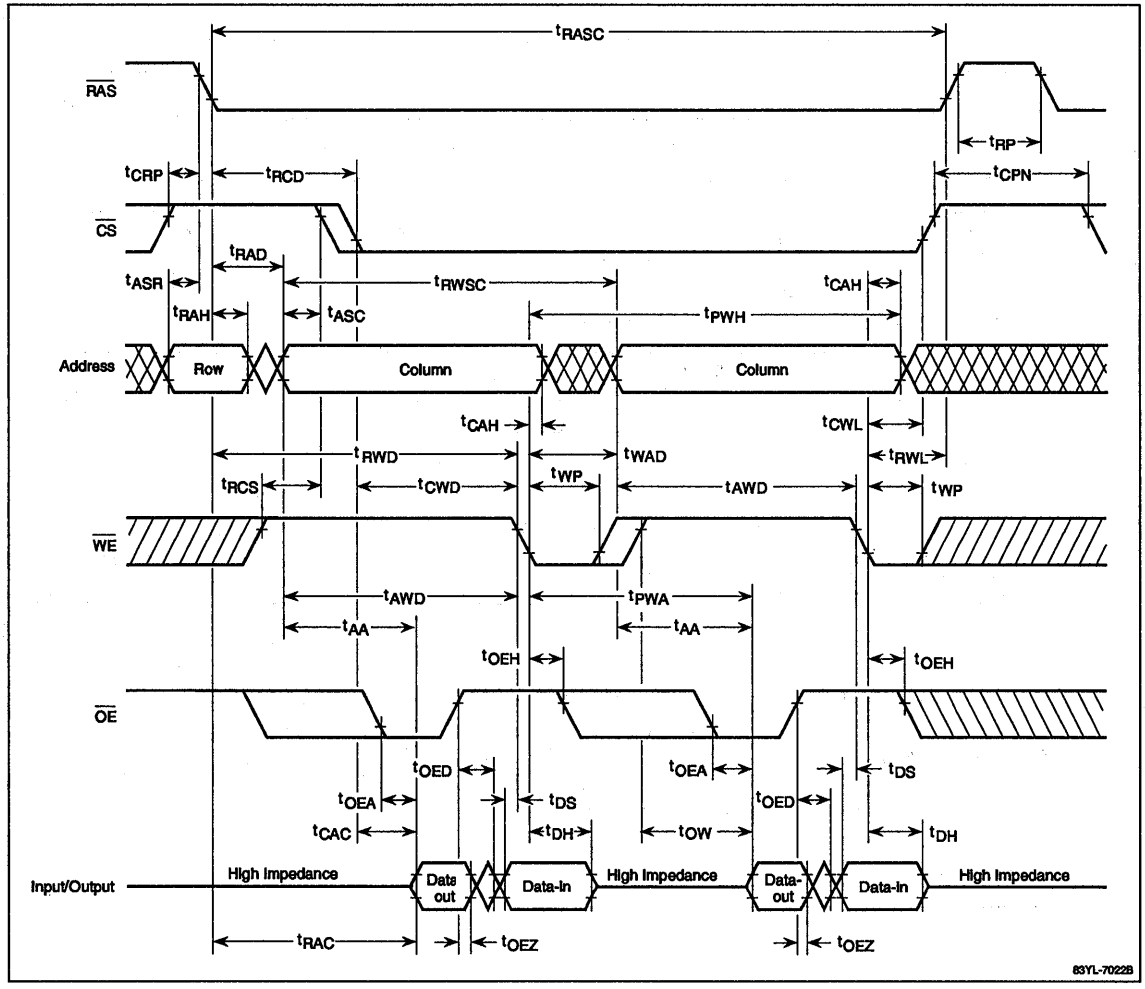
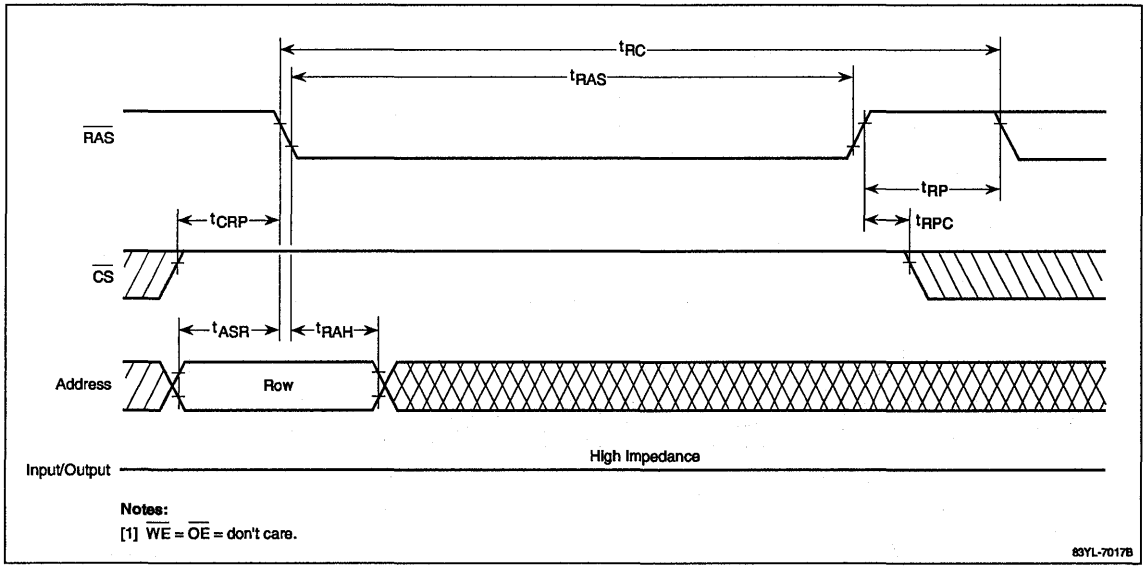
Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

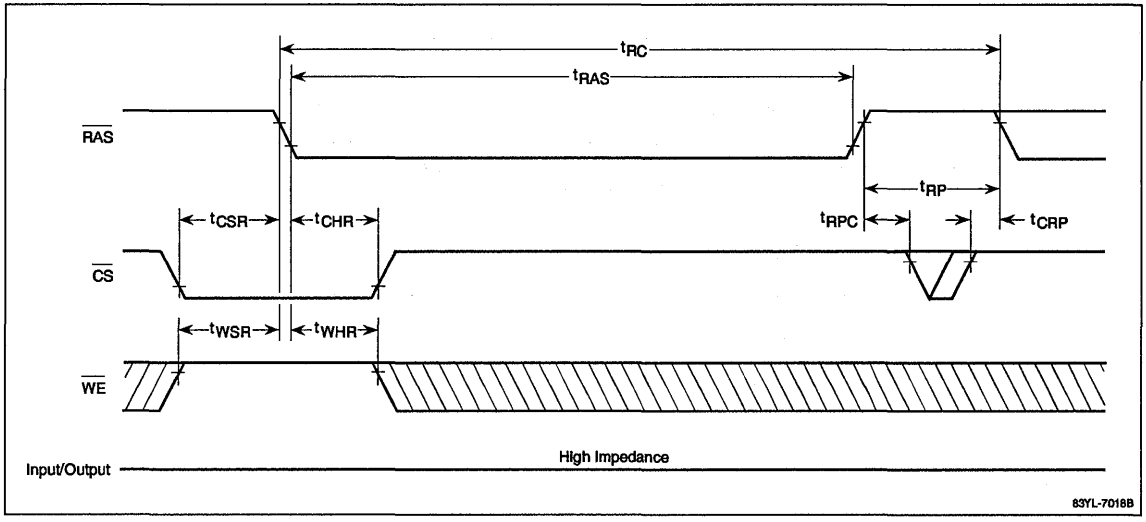
$\overline{RAS}$-Only Refresh Cycle



Notes:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

83YL-7017B

$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



83YL-7018B

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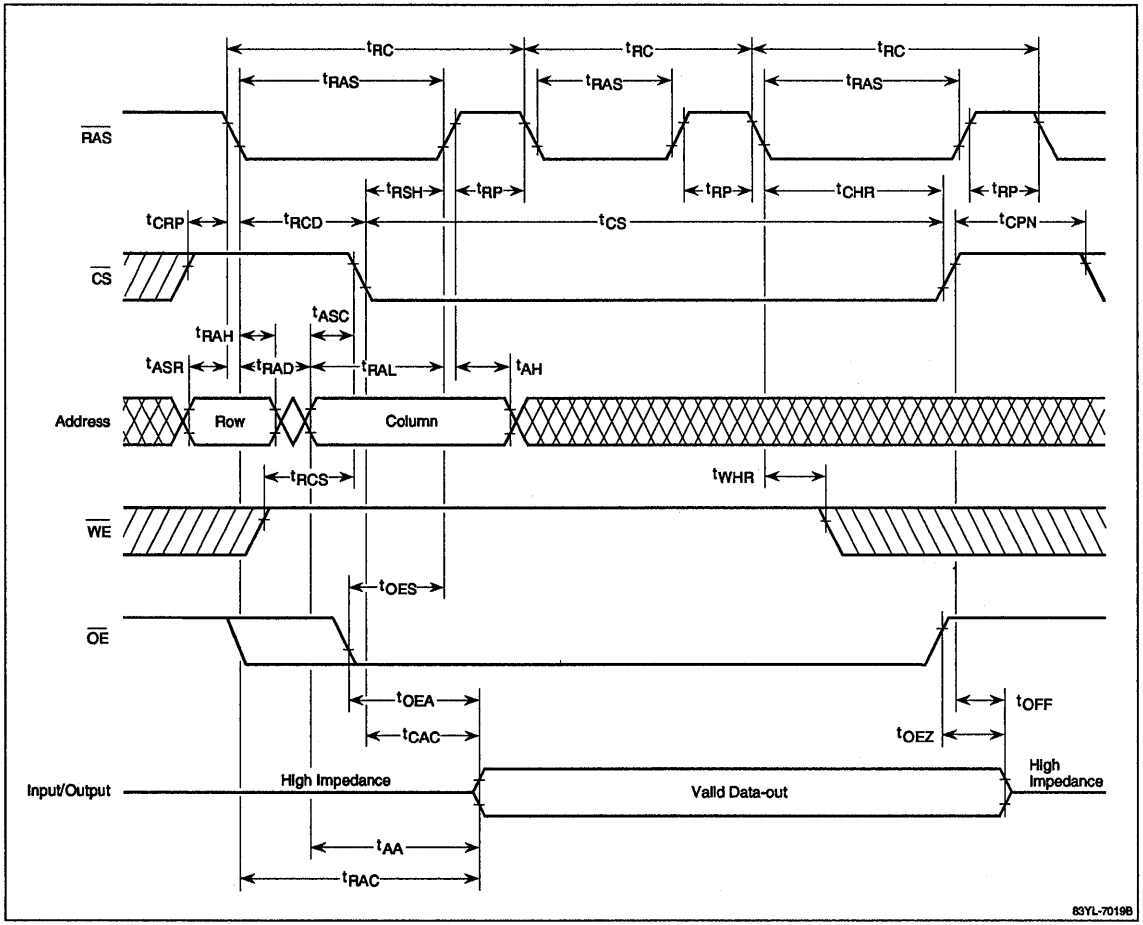
Timing Waveforms (cont)

Hidden Refresh Cycle



μPD424410
1,048,576 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424410 is a 1,048,576 by 4-bit dynamic RAM designed with a write-per-bit option to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1,024 address combinations of A_0 through A_9 during a 16-ms refresh period.

Features

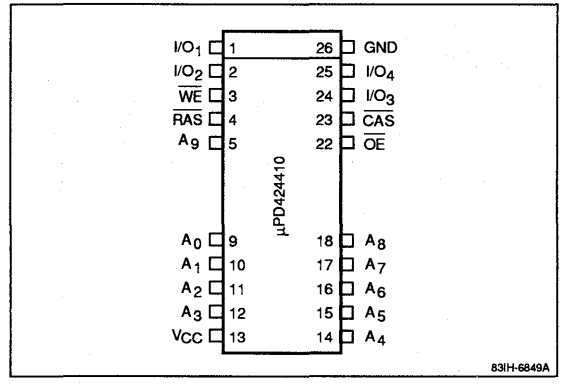
- 1,048,576 by 4-bit organization
- Single +5-volt power supply
- Write-per-bit option
- Fast-page option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- High-density 26/20-pin plastic SOJ, 26/20-pin plastic TSOP, or 20-pin plastic ZIP packaging

Pin Identification

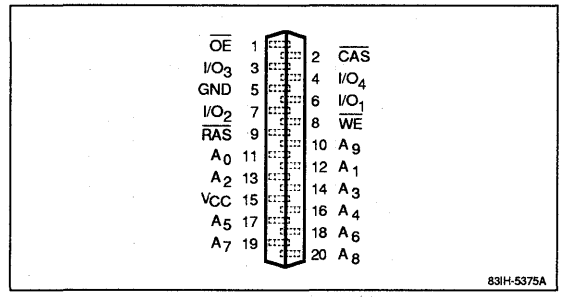
Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configurations

26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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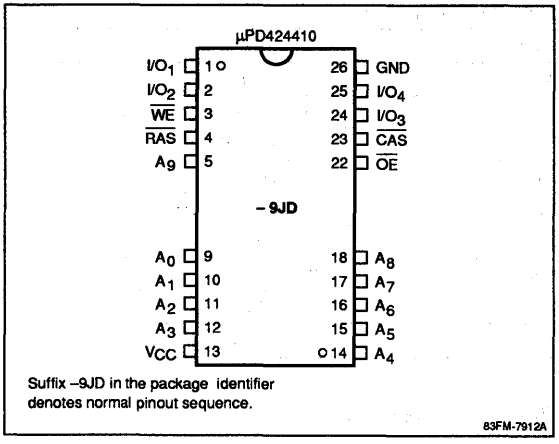
Pin Configurations (cont)

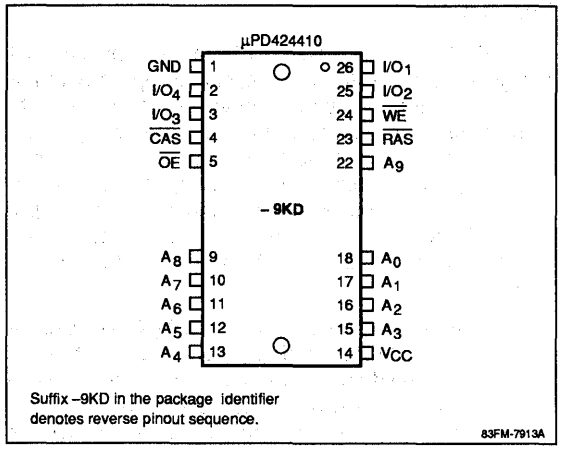
26/20-Pin Plastic TSOP (Normal Pinouts)



Suffix –9JD in the package identifier denotes normal pinout sequence.

83FM-7912A

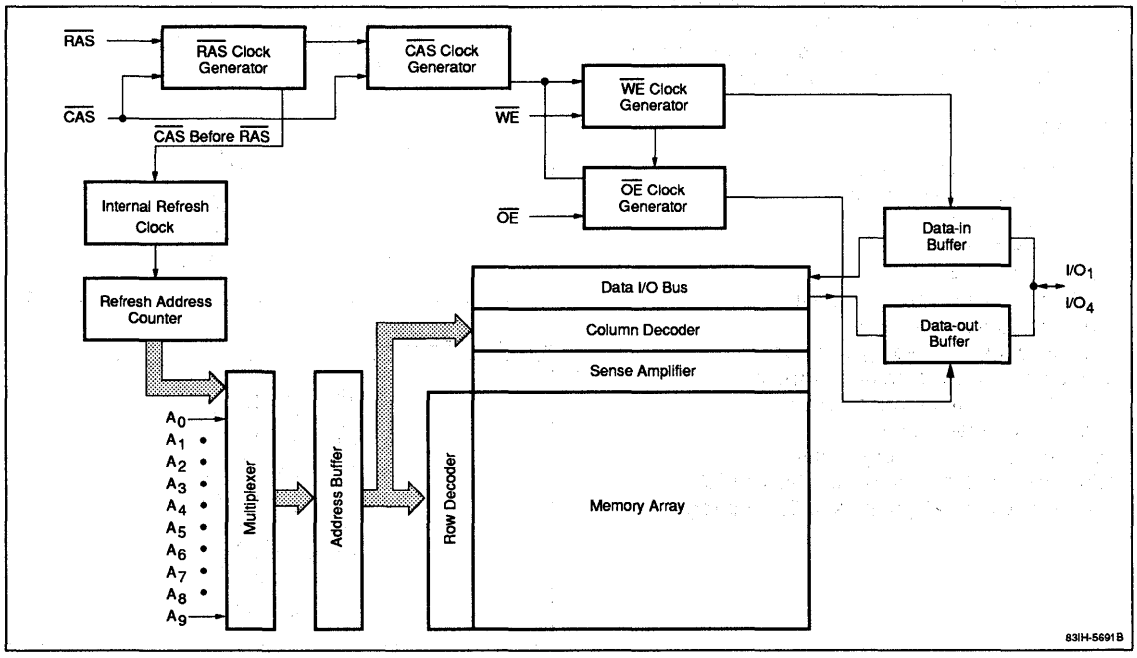
26/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –9KD in the package identifier denotes reverse pinout sequence.

83FM-7913A

Block Diagram



83IH-5691B

Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Power Option	Package
μPD424410LA-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic SOJ (300 mil)
LA-70	70 ns	140 ns	45 ns		
LA-80	80 ns	160 ns	50 ns		
LA-10	100 ns	190 ns	60 ns		
μPD424410LA-60L	60 ns	120 ns	40 ns	Low power	
LA-70L	70 ns	140 ns	45 ns		
LA-80L	80 ns	160 ns	50 ns		
LA-10L	100 ns	190 ns	60 ns		
μPD424410LB-70	70 ns	140 ns	45 ns	Standard	26/20-pin plastic SOJ (350 mil)
LB-80	80 ns	160 ns	50 ns		
LB-10	100 ns	190 ns	60 ns		
μPD424410LB-70L	70 ns	140 ns	45 ns	Low power	
LB-80L	80 ns	160 ns	50 ns		
LB-10L	100 ns	190 ns	60 ns		
μPD424410V-60	60 ns	120 ns	40 ns	Standard	20-pin plastic ZIP
V-70	70 ns	140 ns	45 ns		
V-80	80 ns	160 ns	50 ns		
V-10	100 ns	190 ns	60 ns		
μPD424410V-60L	60 ns	120 ns	40 ns	Low power	
V-70L	70 ns	140 ns	45 ns		
V-80L	80 ns	160 ns	50 ns		
V-10L	100 ns	190 ns	60 ns		
μPD424410GS-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic TSOP (normal pinouts)
GS-70	70 ns	140 ns	45 ns		
GS-80	80 ns	160 ns	50 ns		
μPD424410GS-60L	60 ns	120 ns	40 ns	Low power	
GS-70L	70 ns	140 ns	45 ns		
GS-80L	80 ns	160 ns	50 ns		
μPD424410GSM-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic TSOP (reverse pinouts)
GSM-70	70 ns	140 ns	45 ns		
GSM-80	80 ns	160 ns	50 ns		
μPD424410GSM-60L	60 ns	120 ns	40 ns	Low power	
GSM-70L	70 ns	140 ns	45 ns		
GSM-80L	80 ns	160 ns	50 ns		

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_D	7	pF	I/O_1 – I/O_4

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} \geq V_{IH}$ (min); I_O = 0 mA
				1.0	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

Low Power Battery Backup (-L Versions Only)

Symbol	Max	Unit	t_{RAS}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	500	μA	≤ 1 μs	1024 refresh cycles (min) every 128 ms; $\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V or ≤ 0.2 V, as appropriate; I/O open; all other inputs ≥ $V_{CC} - 0.2$ V or ≤ 0.2 V	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V; D_{IN}, $\overline{WE}$, $\overline{OE}$, Addresses ≥ $V_{CC} - 0.2$ V or ≤ 0.2 V; I/O open
	300	μA	≤ 200 ns		

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		120		100		90		80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		120		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		90		80		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		120		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55		45		55	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		65		80		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ to output active delay time	t_{CLZ}	0		0		0		0		ns	(Notes 4, 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		55		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 9)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 9)
$\overline{OE}$ to output active delay time	t_{OLZ}	0		0		0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Fast page read-modify-write cycle time	t_{PRWC}	85		90		100		120		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 3, 4, 7, 8)

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AC Characteristics (cont)

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Address A_0 through A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-modify-write cycle time	t_{RWC}	165		185		210		250		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		130		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write-per-bit hold time	t_{WBH}	15		15		15		20		ns	
Write-per-bit setup time	t_{WBS}	10		10		10		10		ns	
Write command hold time	t_{WCH}	15		15		15		20		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 14)
Write-per-bit mask data hold time	t_{WH}	15		15		15		20		ns	
$\overline{WE}$ command hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{WHR}	15		15		15		20		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 12)
Write-per-bit mask data setup time	t_{WS}	10		10		10		10		ns	
$\overline{WE}$ command setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power up sequence, either a $\overline{RAS}$-only or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max). If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

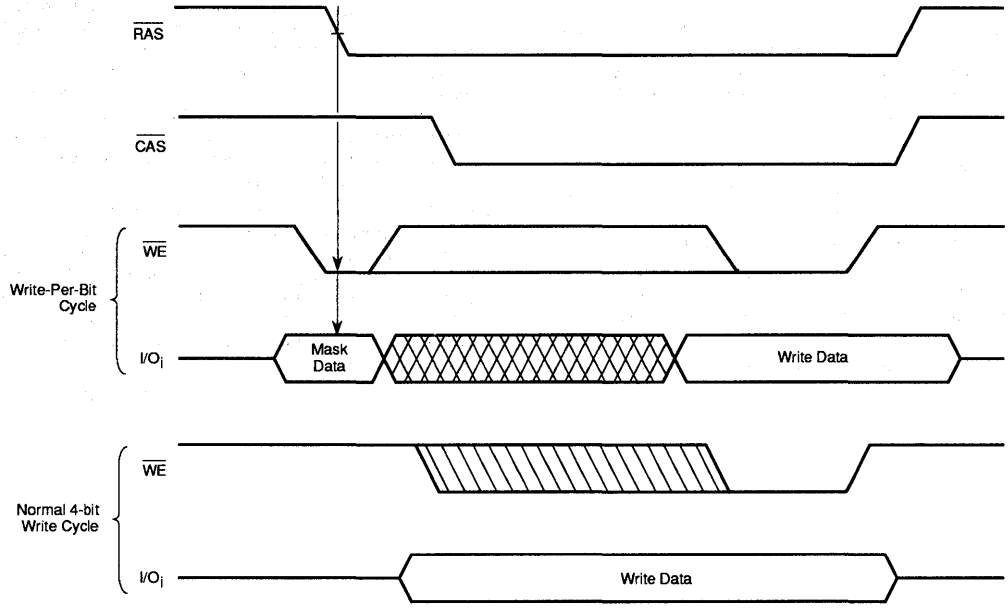
(16) These parameters define a read-modify-write cycle.

5f

Write-Per-Bit Option

The write-per-bit option may be used to allow a write cycle to change any number of bits in the 4-bit word. The mask is loaded from the four I/O lines at the falling edge of $\overline{RAS}$ if $\overline{WE} = V_{IL}$. If the I/O line is high, then the corresponding bit will be written when the write cycle executes. If an I/O line is low, the corresponding bit does not change. A mask loaded during fast-page operation will remain set and active for each write cycle that executes while $\overline{RAS}$ remains low. The mask may be changed at the falling edge of $\overline{RAS}$ only.

Comparison of Write-Per-Bit Cycle Versus Standard 4-Bit Write Cycle

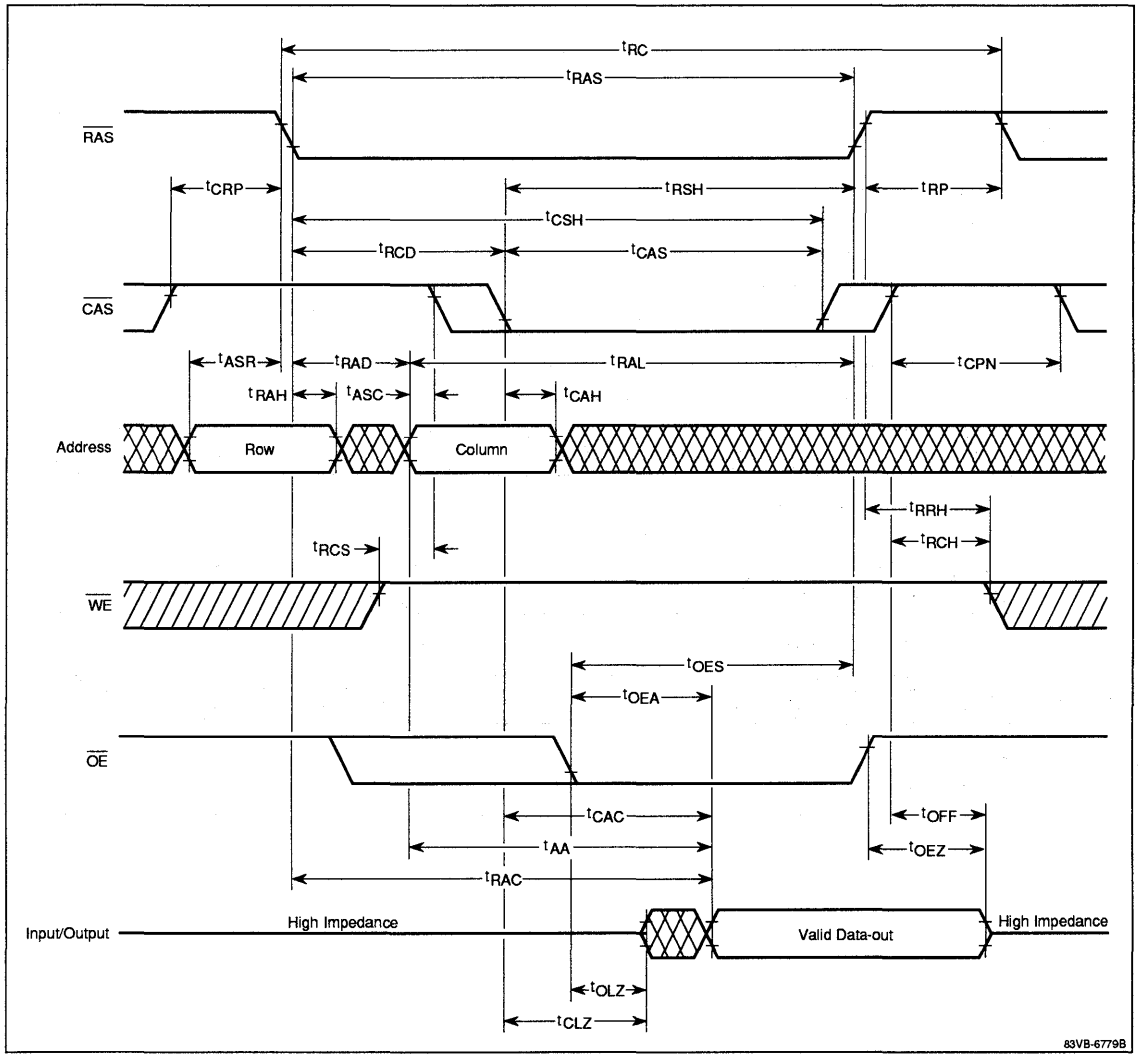


I/O	Mask Data		Write Operation
I/O_1	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_2	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_3	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_4	1	(High)	Write Bit
	0	(Low)	Disable Bit Write

83VB-6778B

Timing Waveforms

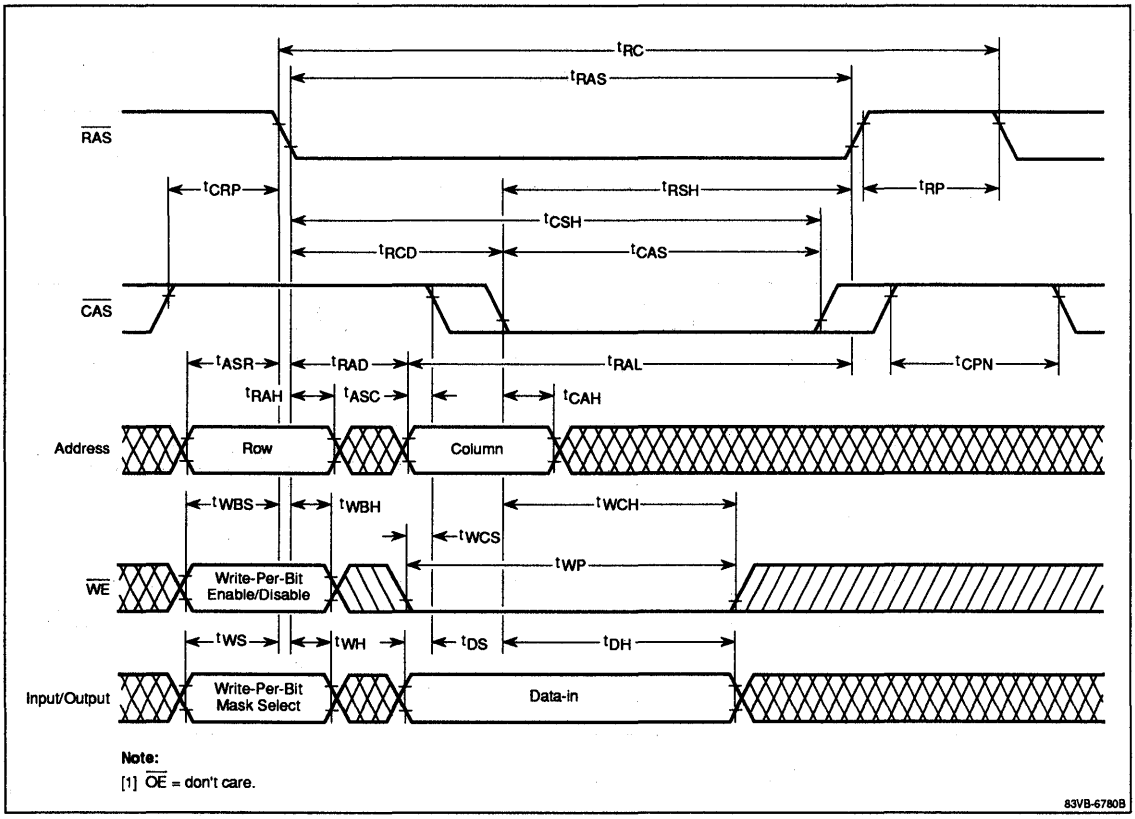
Read Cycle



5f

Timing Waveforms (cont)

Early Write Cycle



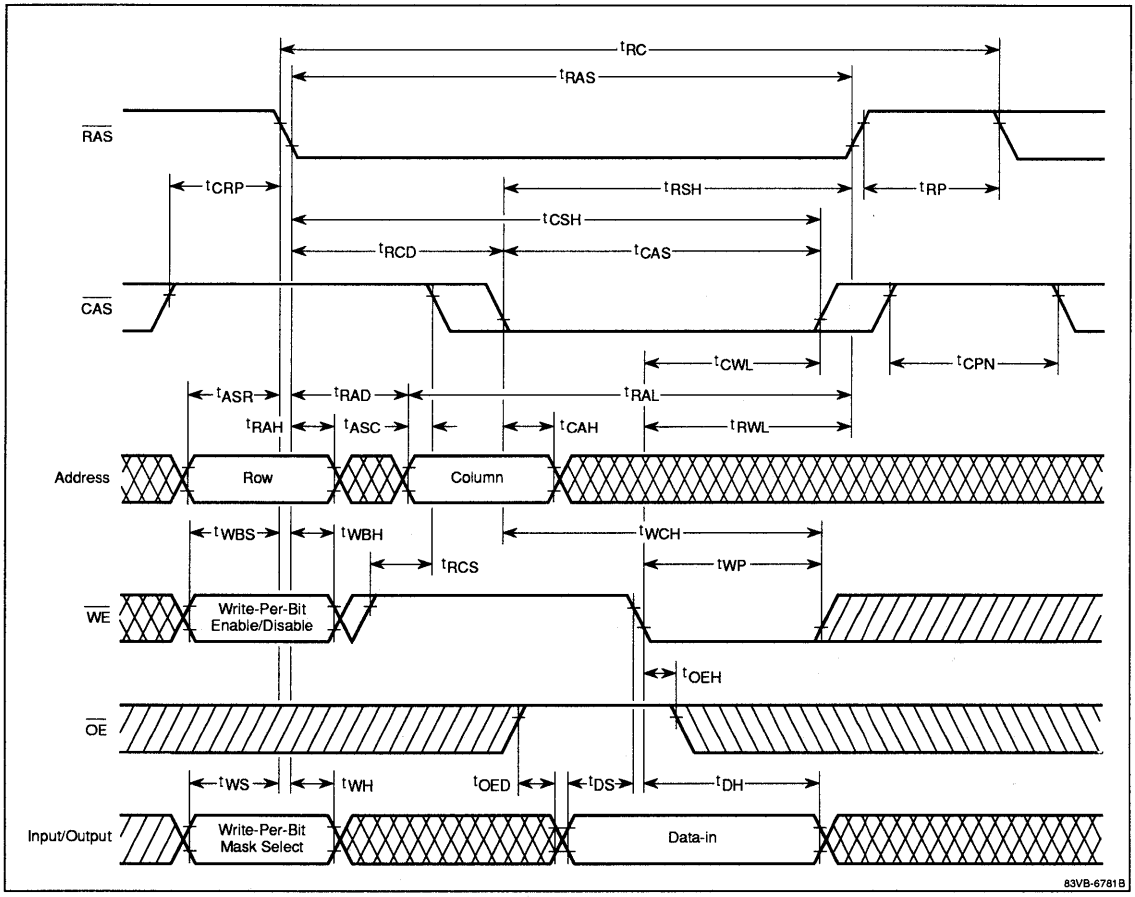
Note:

[1] $\overline{OE}$ = don't care.

83VB-6780B

Timing Waveforms (cont)

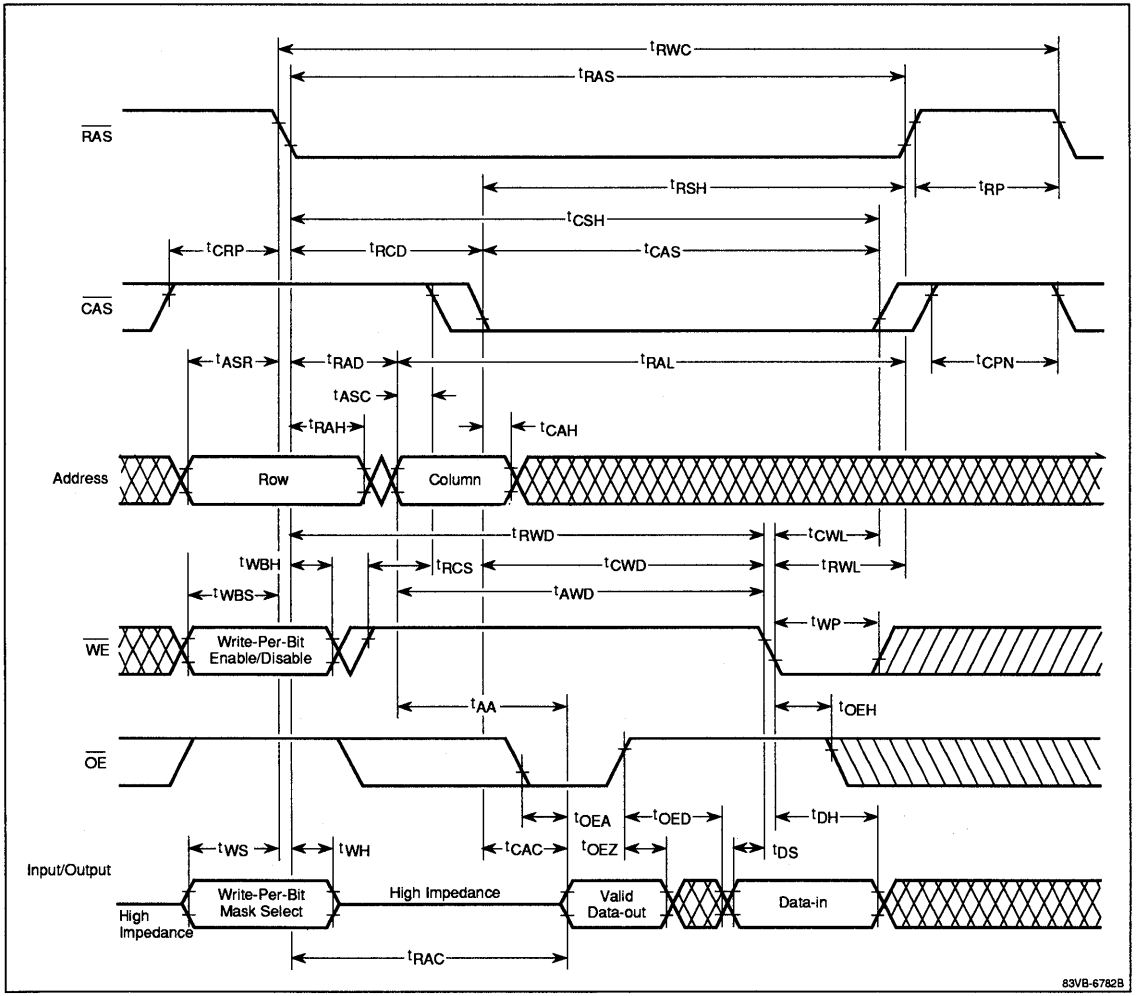
Late Write Cycle



5f

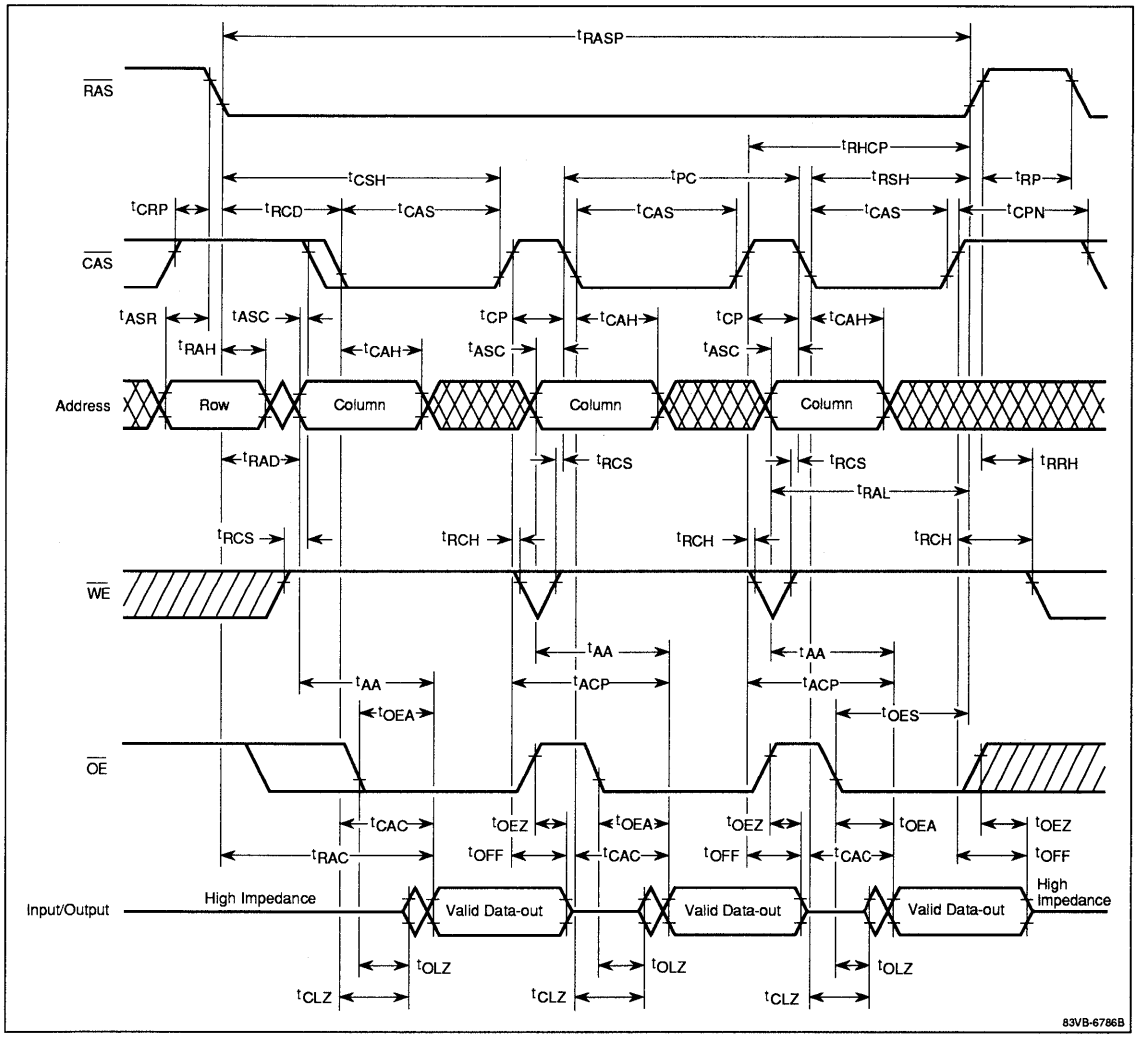
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

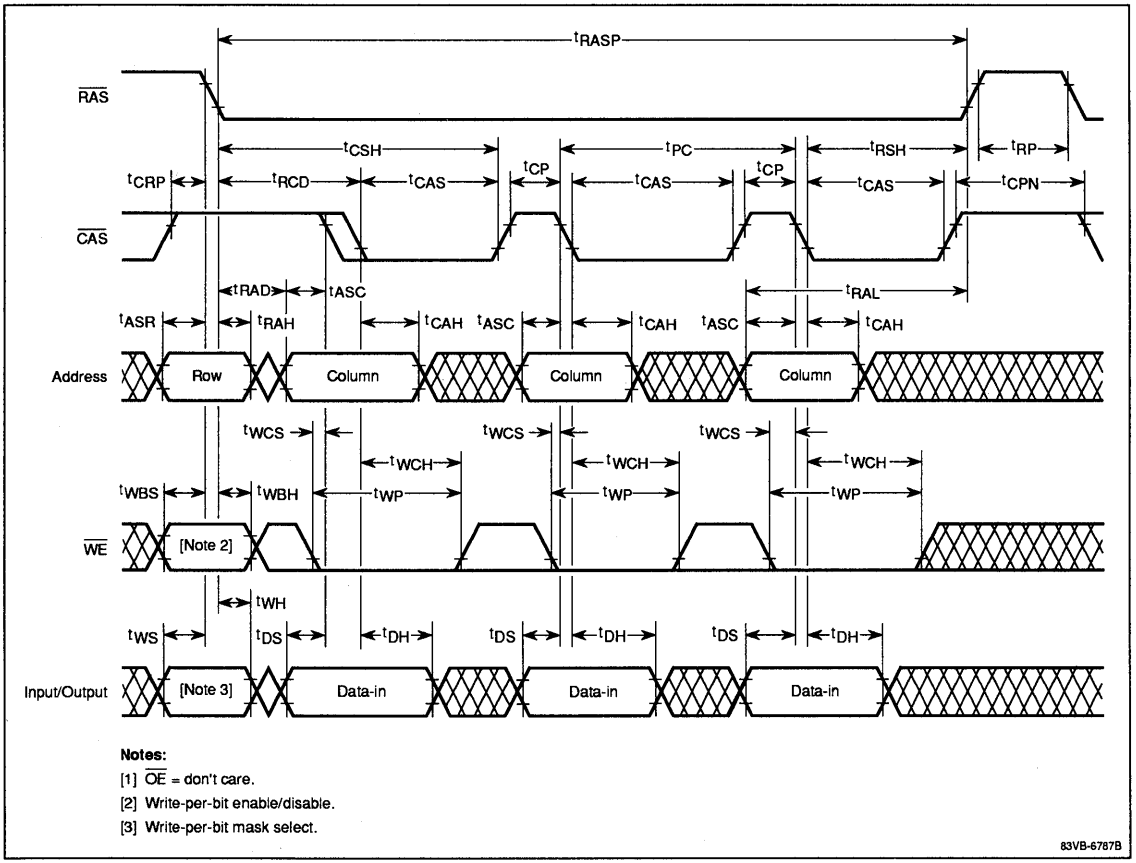
Fast-Page Read Cycle



5f

Timing Waveforms (cont)

Fast-Page Early Write Cycle



Notes:

[1] $\overline{OE}$ = don't care.

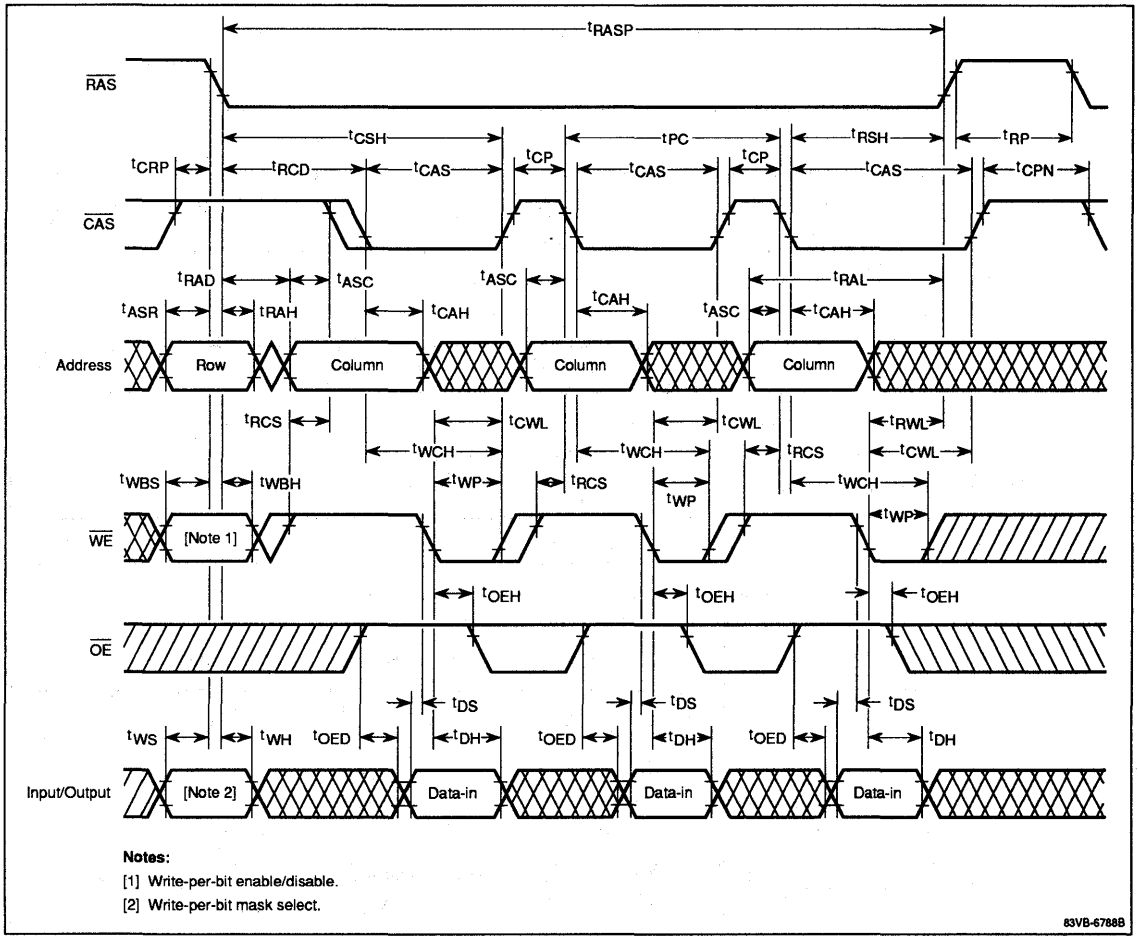
[2] Write-per-bit enable/disable.

[3] Write-per-bit mask select.

83VB-6787B

Timing Waveforms (cont)

Fast-Page Late Write Cycle



Notes:

[1] Write-per-bit enable/disable.

[2] Write-per-bit mask select.

83VB-6788B

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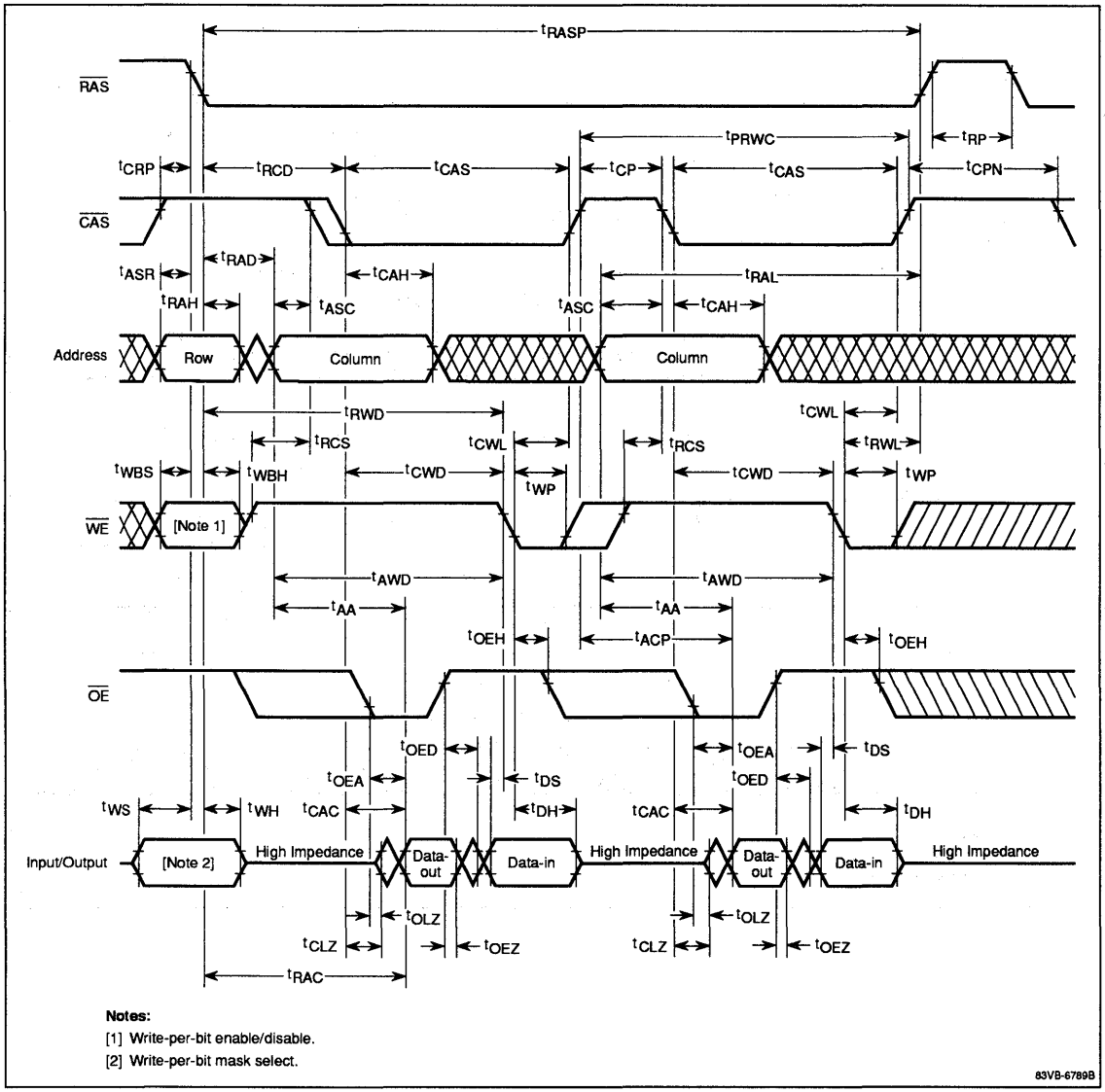
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



Notes:

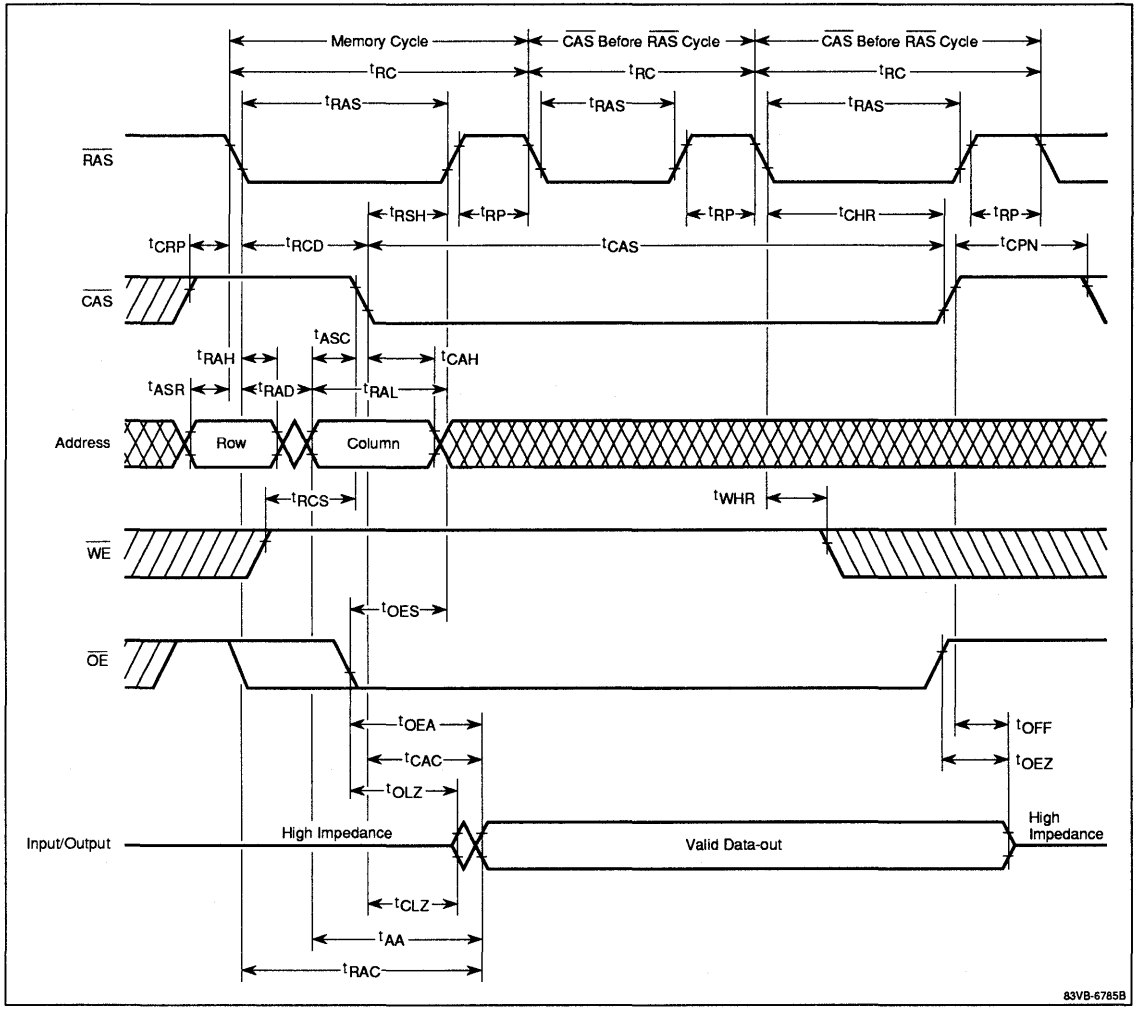
[1] Write-per-bit enable/disable.

[2] Write-per-bit mask select.

83VB-6789B

Timing Waveforms (cont)

Hidden Refresh Cycle



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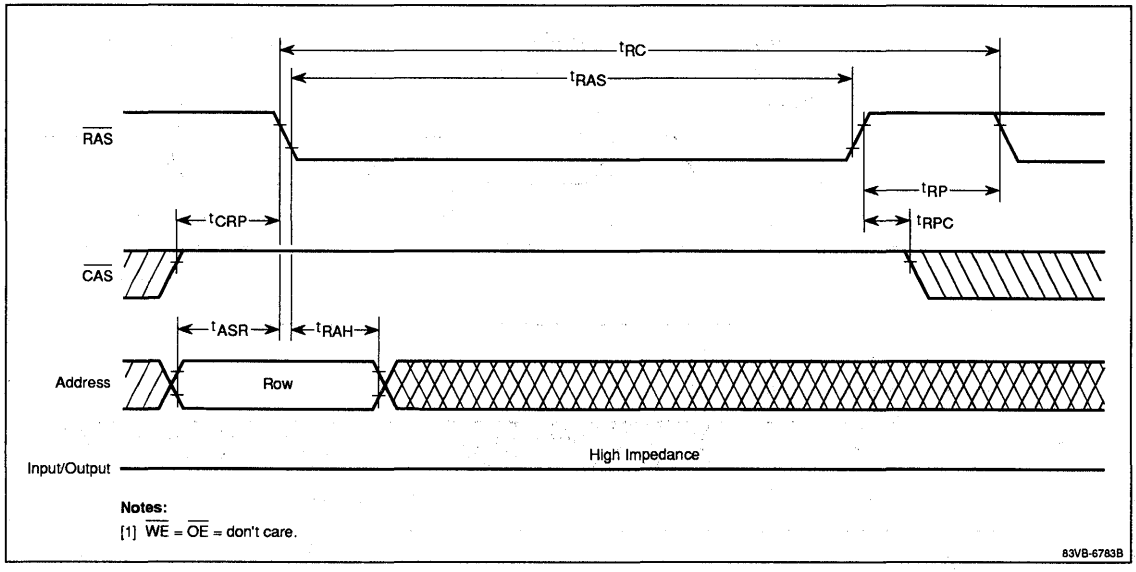
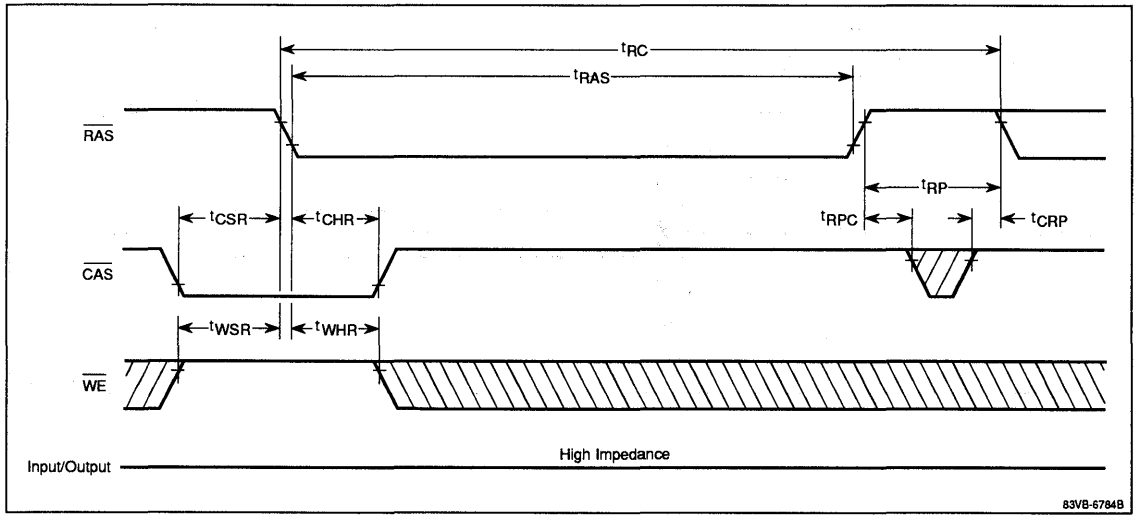
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



μPD424412
1,048,576 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424412 is a static-column 1,048,576 by 4-bit dynamic RAM designed with a write-per-bit option to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. Data outputs return to high impedance when $\overline{CS}$ goes high. Static-column read and write cycles can be executed by cycling $\overline{CS}$.

Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1024 address combinations of A_0 - A_9 during a 16-ms refresh period.

Features

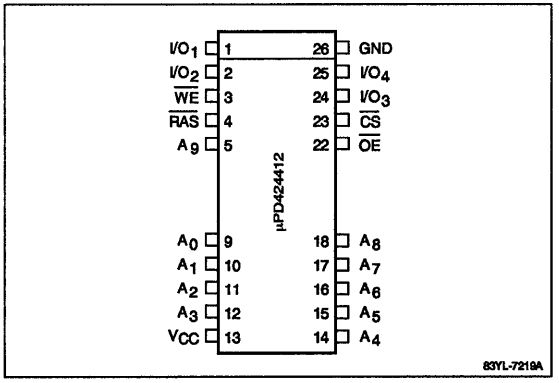
- 1,048,576 by 4-bit organization
- Single +5-volt power supply
- Write-per-bit option
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- High-density 26/20-pin SOJ, 20-pin ZIP, or 26/20-pin TSOP plastic packaging

Pin Identification

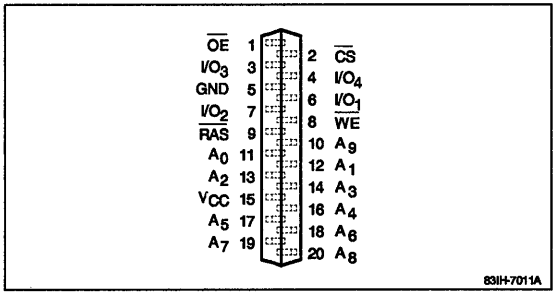
Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Pin Configurations

26/20-Pin Plastic SOJ



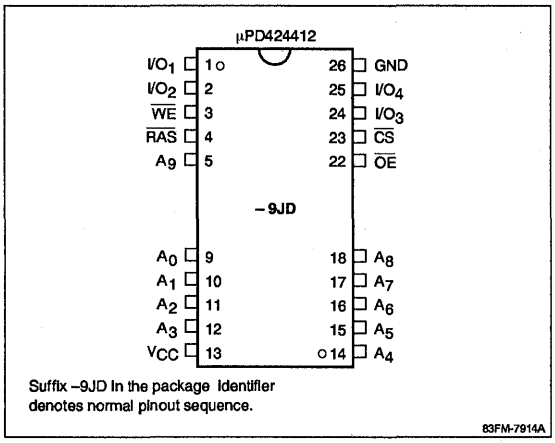
20-Pin Plastic ZIP



5g

Pin Configurations (cont)

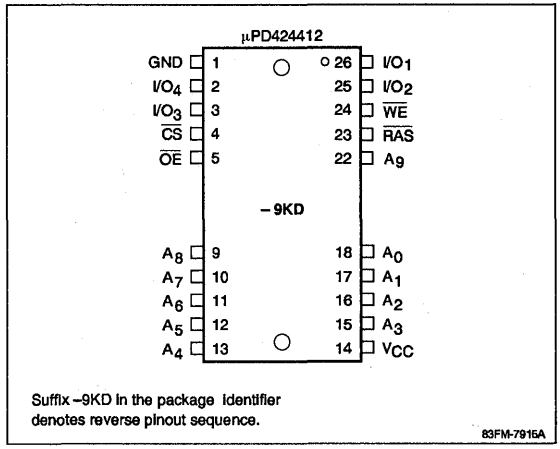
26/20-Pin Plastic TSOP (Normal Pinouts)



Suffix –9JD in the package identifier denotes normal pinout sequence.

83FM-7914A

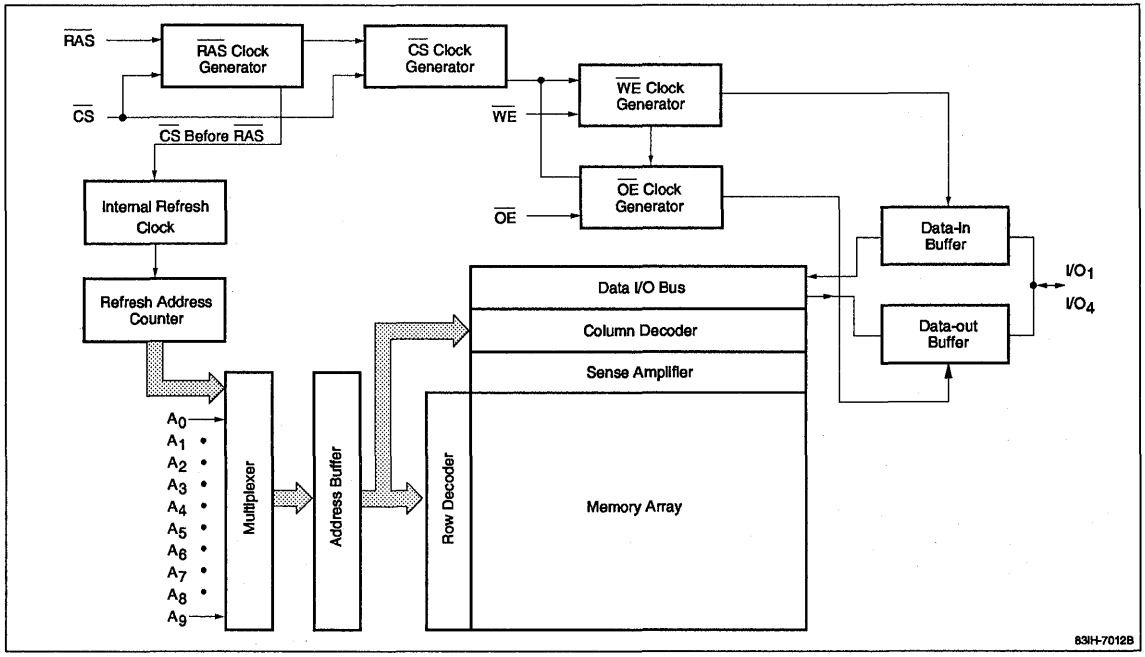
26/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –9KD in the package identifier denotes reverse pinout sequence.

83FM-7915A

Block Diagram



83IH-7012B

Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Static-Column Cycle (max)	Power Option	Package
μPD424412LA-60	60 ns	120 ns	35 ns	Standard	26/20-pin plastic SOJ (300-mil)
LA-70	70 ns	140 ns	40 ns		
LA-80	80 ns	160 ns	50 ns		
LA-10	100 ns	190 ns	60 ns		
μPD424412LA-60L	60 ns	120 ns	35 ns	Low power	
LA-70L	70 ns	140 ns	40 ns		
LA-80L	80 ns	160 ns	50 ns		
LA-10L	100 ns	190 ns	60 ns		
μPD424412V-60	60 ns	120 ns	35 ns	Standard	20-pin plastic ZIP
V-70	70 ns	140 ns	40 ns		
V-80	80 ns	160 ns	50 ns		
V-10	100 ns	190 ns	60 ns		
μPD424412V-60L	60 ns	120 ns	35 ns	Low power	
V-70L	70 ns	140 ns	40 ns		
V-80L	80 ns	160 ns	50 ns		
V-10L	100 ns	190 ns	60 ns		
μPD424412GS-60	60 ns	120 ns	35 ns	Standard	26/20-pin plastic TSOP (normal pinouts)
GS-70	70 ns	140 ns	40 ns		
GS-80	80 ns	160 ns	50 ns		
μPD424412GS-60L	60 ns	120 ns	35 ns	Low power	
GS-70L	70 ns	140 ns	40 ns		
GS-80L	80 ns	160 ns	50 ns		
μPD424412GSM-60	60 ns	120 ns	35 ns	Standard	26/20-pin plastic TSOP (reverse pinouts)
GSM-70	70 ns	140 ns	40 ns		
GSM-80	80 ns	160 ns	50 ns		
μPD424412GSM-60L	60 ns	120 ns	35 ns	Low power	
GSM-70L	70 ns	140 ns	40 ns		
GSM-80L	80 ns	160 ns	50 ns		

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 – I/O_4

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{IH} (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	I/O disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

Low Power Battery Backup (-L Versions Only)

Symbol	Max	Unit	t_{RAS}	$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	500	μA	≤ 1 μs	1024 refresh cycles (min) every 128 ms; $\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V or ≤ 0.2 V, as appropriate; I/O open; all other inputs ≥ V_{CC} − 0.2 V or ≤ 0.2 V	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V; $\overline{WE}$, $\overline{OE}$, Addresses ≥ V_{CC} − 0.2 V or ≤ 0.2 V; I/O open
	300	μA	≤ 200 ns		

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		120		100		90		80	mA	$\overline{RAS}$, $\overline{CS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		120		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
Operating current, static-column cycle, average	I_{CC4}		90		80		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CS}$ cycling; t_{RSC} = t_{RSC} min or t_{WSC} = t_{WSC} min (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		120		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 3, 4, 7, 8)
Colum address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		55		65		80		ns	(Note 15)
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		20		ns	
$\overline{CS}$ precharge time, static-column cycle	t_{CP}	10		10		10		10		ns	
$\overline{CS}$ precharge time	t_{CPN}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 11)
$\overline{CS}$ pulse width	t_{CS}	20	100,000	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	20		40		45		55		ns	(Note 15)
Write command referenced to $\overline{CS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 14)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 14)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 10)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 10)
Output hold time for address	t_{OH}	5		5		5		5		ns	
Output enable time from $\overline{WE}$	t_{OW}		25		25		25		30	ns	
Access time from $\overline{WE}$	t_{PWA}		60		70		90		110	ns	(Notes 7, 16)
Column address hold time referenced to $\overline{WE}$	t_{PWH}	60		70		90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, static-column cycle	t_{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	(Note 12)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 12)
Read cycle time	t_{RSC}	35		40		50		60		ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSW}	75		85		95		115		ns	
Read-modify-write cycle time	t_{RWC}	145		185		210		250		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		90		105		130		ns	(Note 15)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Read/write cycle time	t_{RWSC}	65		95		120		145		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
$\overline{WE}$ to column address delay time	t_{WAD}	20	30	22	35	20	45	25	55	ns	(Note 16)
Write-per-bit hold time	t_{WBH}	15		15		15		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write-per-bit setup time	t_{WBS}	10		10		10		10		ns	
Write command hold time	t_{WCH}	15		15		15		20		ns	(Note 13)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 15)
Write-per-bit mask data hold time	t_{WH}	15		15		15		20		ns	
$\overline{WE}$ command hold time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{WHR}	15		15		15		20		ns	
Write invalid time	t_{WI}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 13)
Write-per-bit mask data setup time	t_{WS}	10		10		10		10		ns	
Write cycle time	t_{WSC}	35		40		50		60		ns	
$\overline{WE}$ command setup time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each static column cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) If $t_{RCD} \leq$ exceeds t_{RAD} max, then t_{RAC} will increase by the amount t_{RCD} exceeds t_{RCD} (max).

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CS}$ cycles preceded by any cycle.

(12) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(13) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(14) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

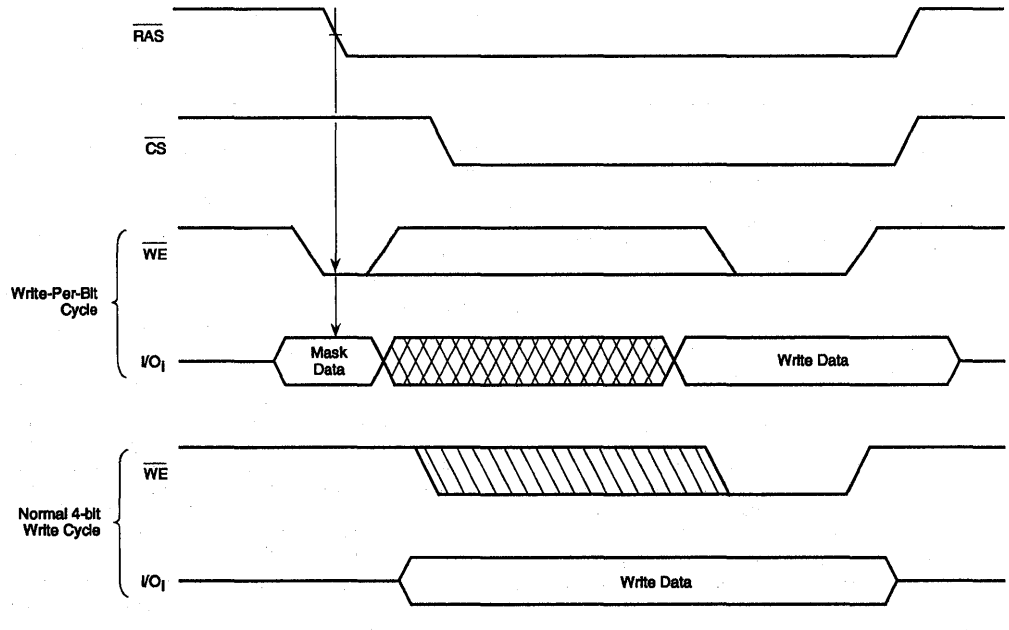
(16) A test mode may be initiated by executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

(17) Assumes $t_{WAD} \leq t_{WAD}$ (max).

Write-Per-Bit Option

The write-per-bit option may be used to allow a write cycle to change any number of bits in the 4-bit word. The mask is loaded from the four I/O lines at the falling edge of $\overline{RAS}$ if $\overline{WE}$ = V_{IL}. If the I/O line is high, then the corresponding bit will be written when the write cycle executes. If an I/O line is low, the corresponding bit does not change. A mask loaded during static-column operation will remain set and active for each write cycle that executes while $\overline{RAS}$ remains low. The mask may be changed at the falling edge of $\overline{RAS}$ only.

Comparison of Write-Per-Bit Cycle Versus Standard 4-Bit Write Cycle



I/O	Mask Data	Write Operation
I/O_1 ~ I/O_4	1 (High)	Write Bit
	0 (Low)	Disable Bit Write

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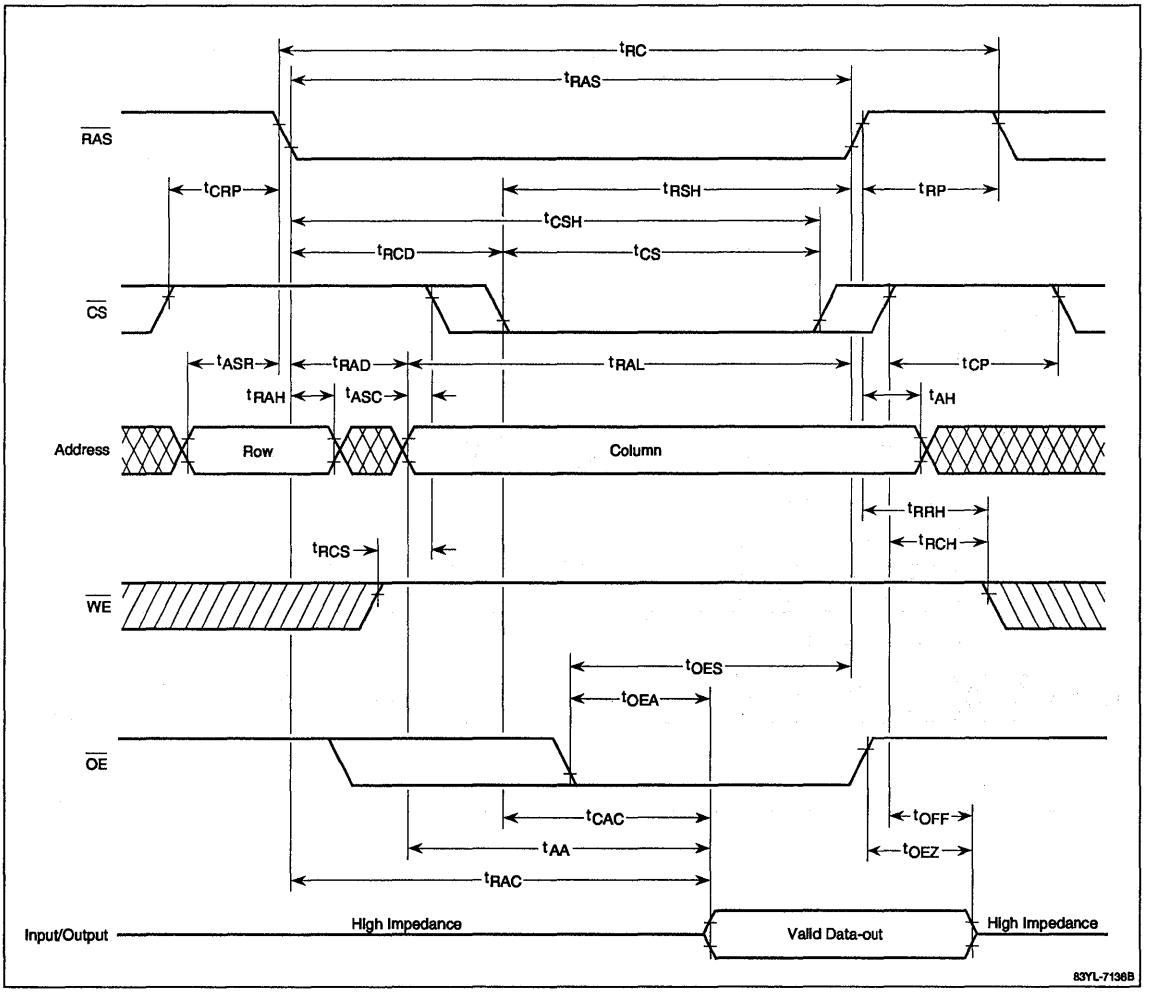
Timing Waveforms

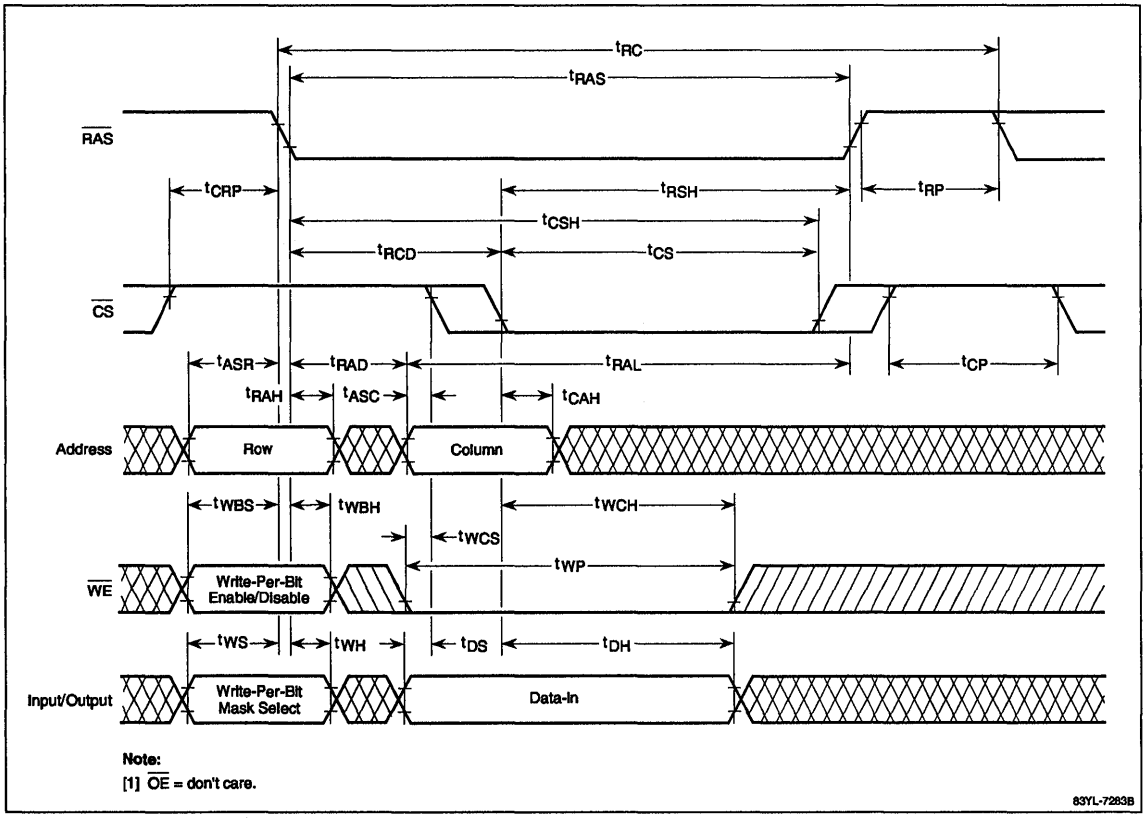
Read Cycle



5g

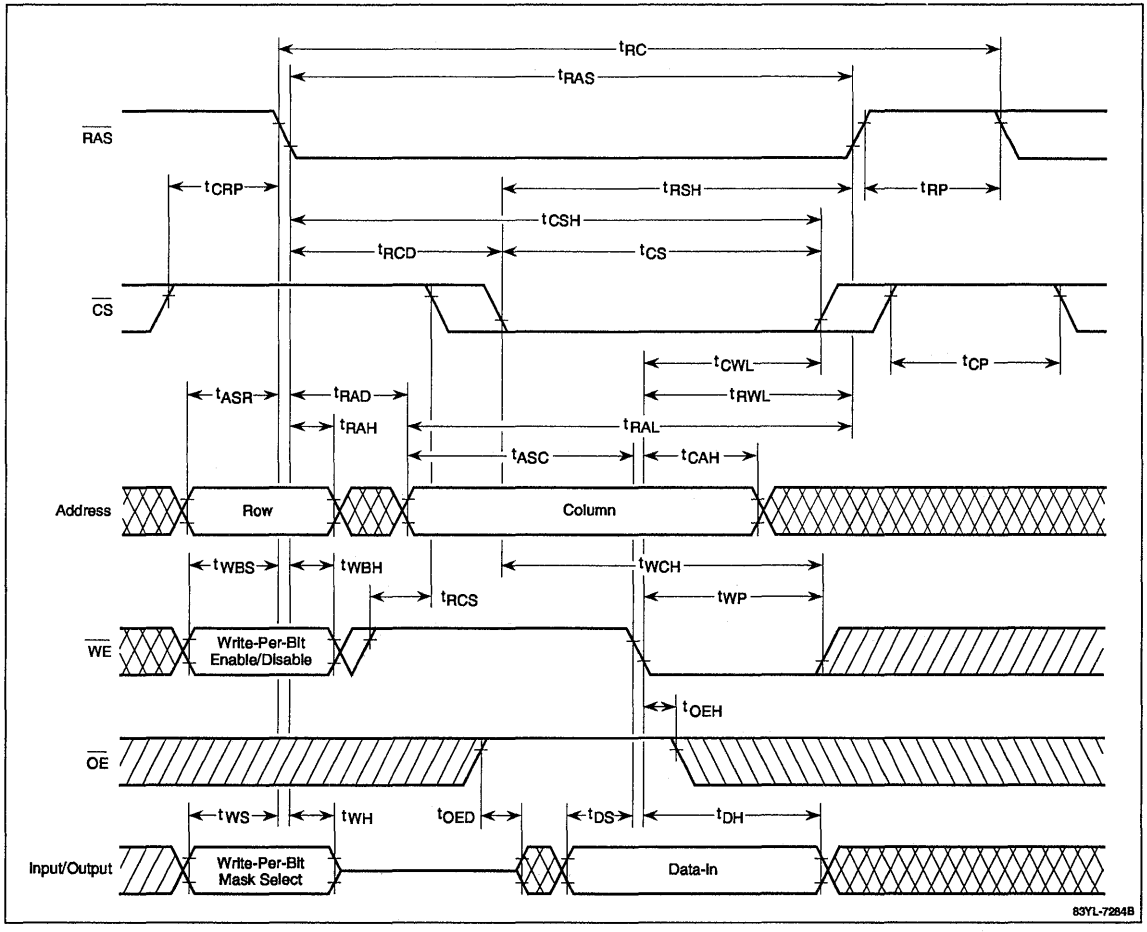
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Late Write Cycle



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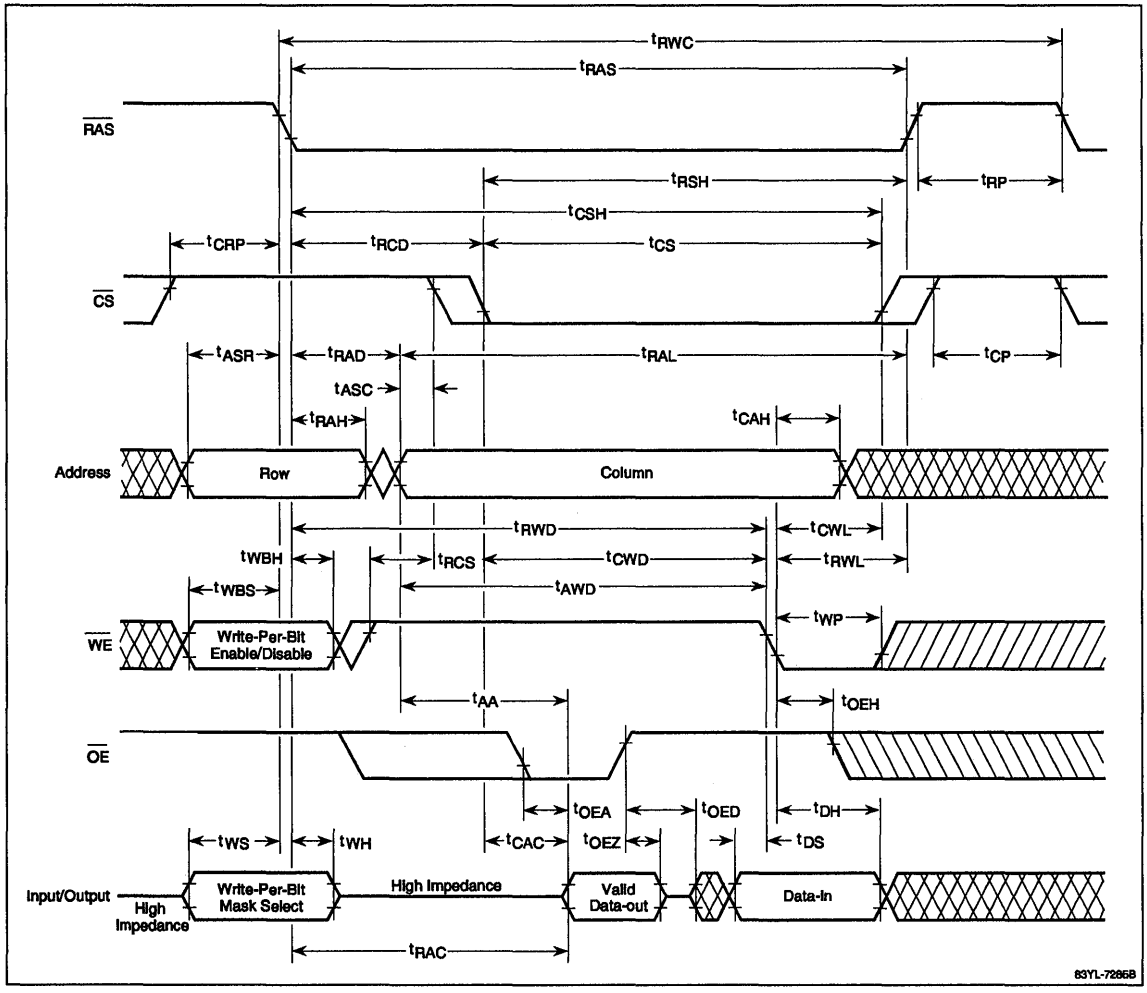
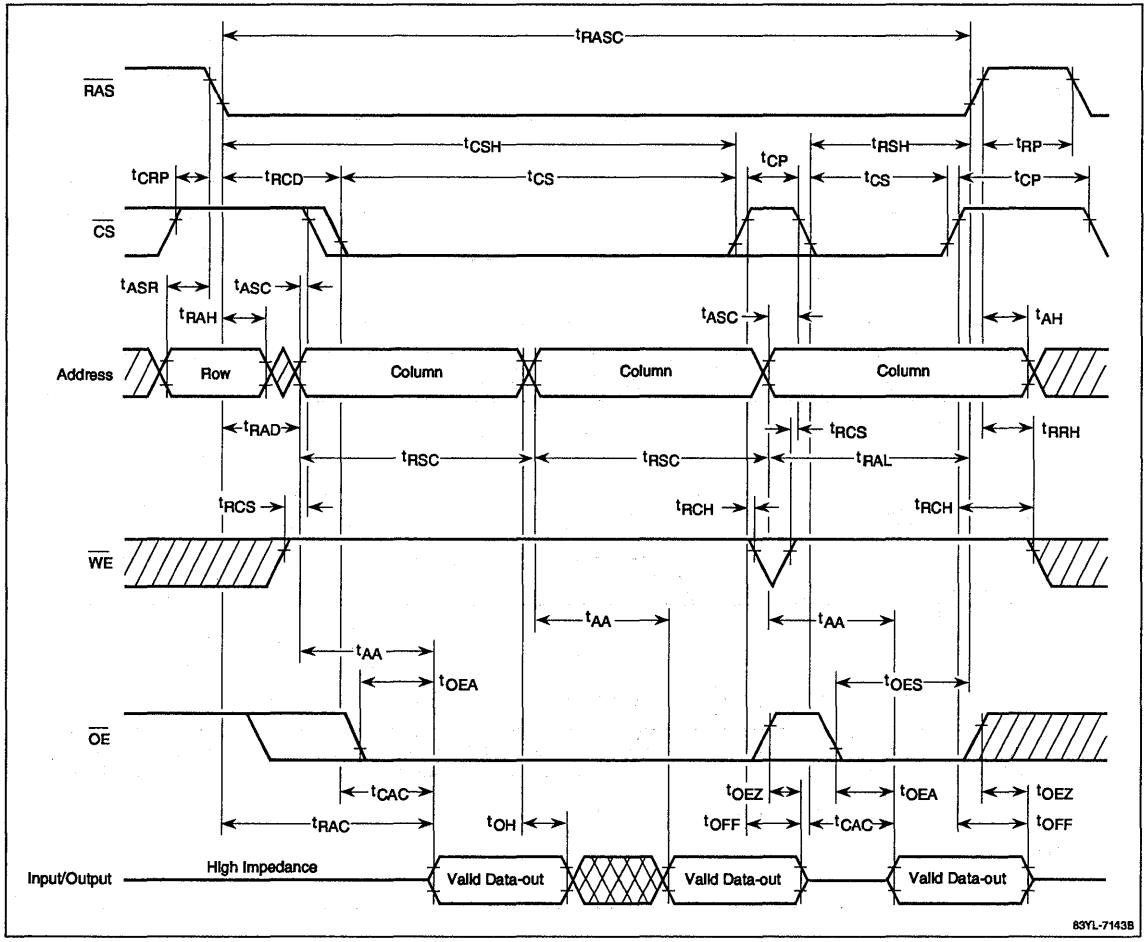
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Static-Column Read Cycle



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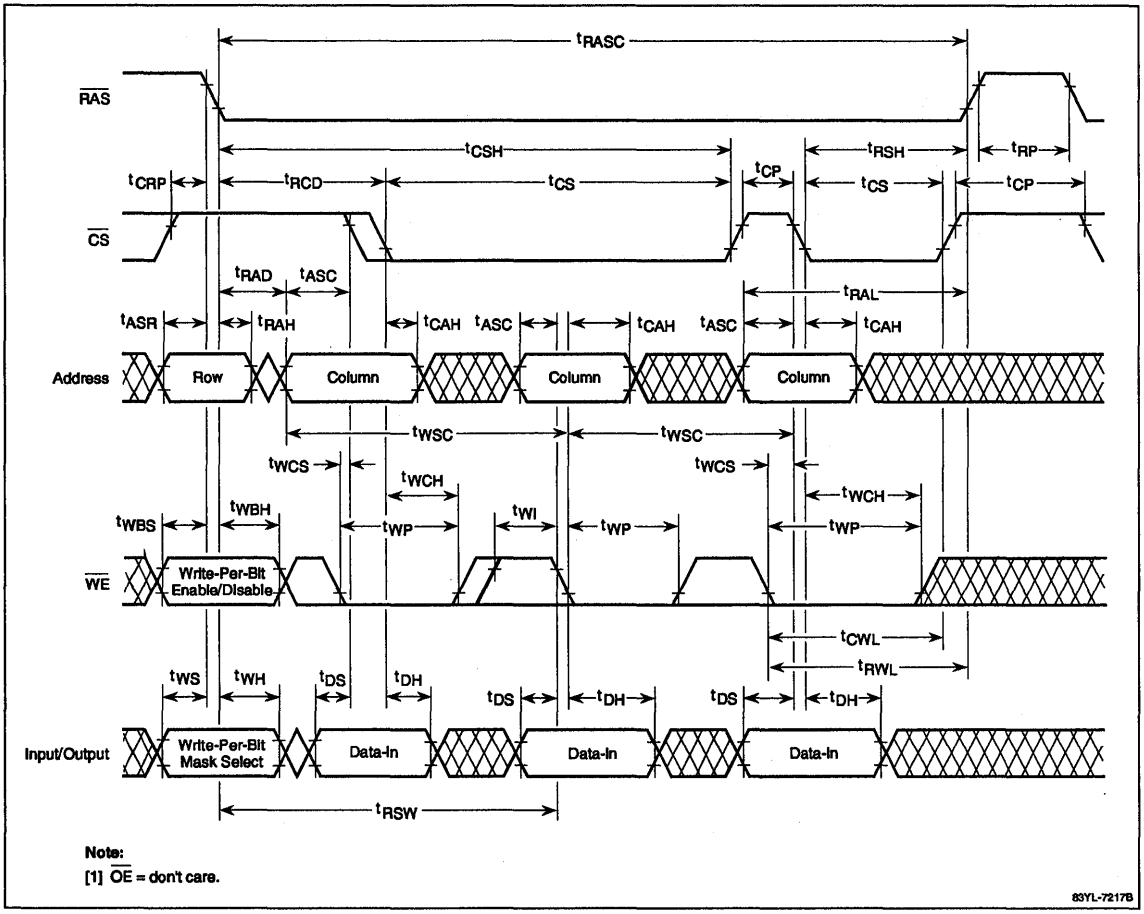
Timing Waveforms (cont)

Static-Column Early Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

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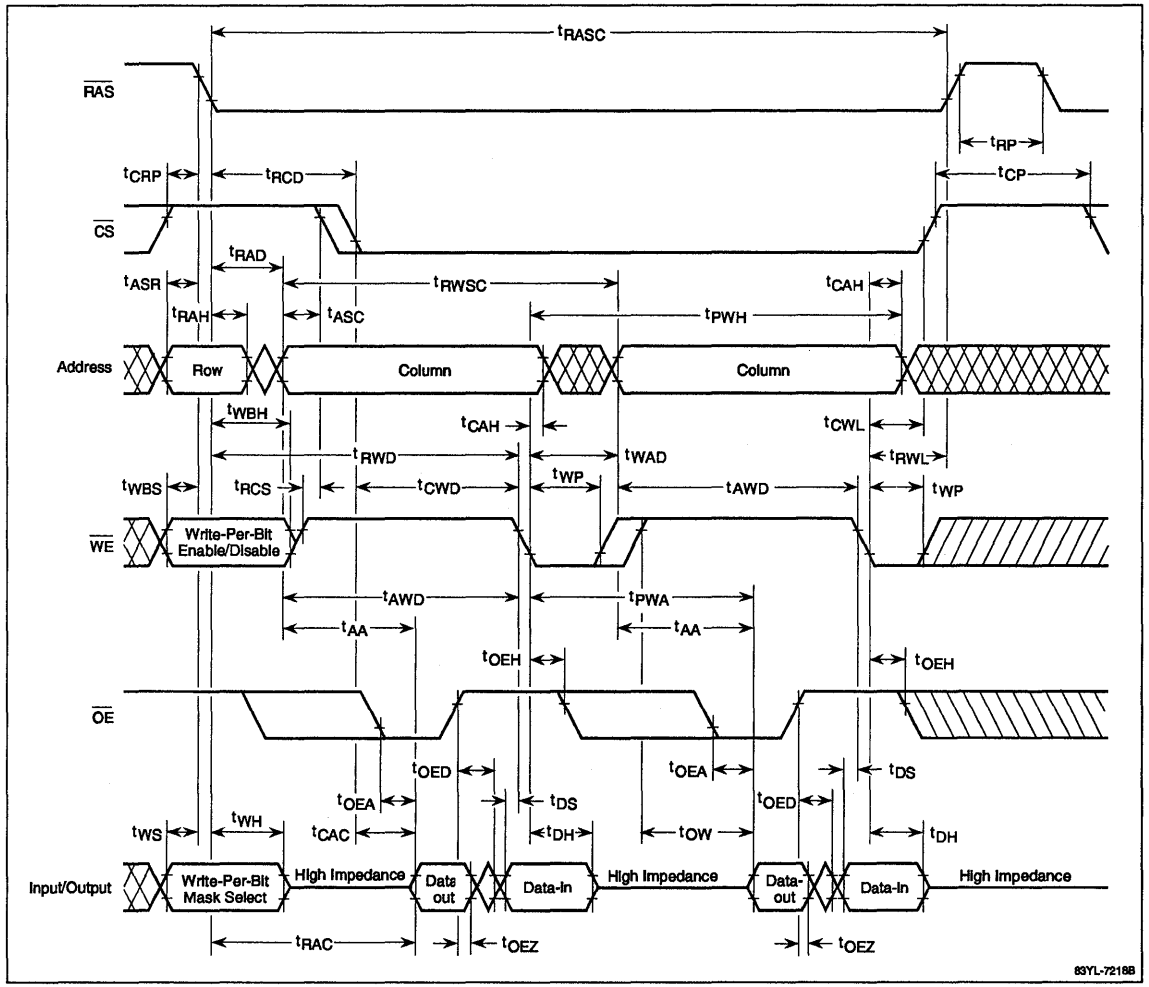
Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle



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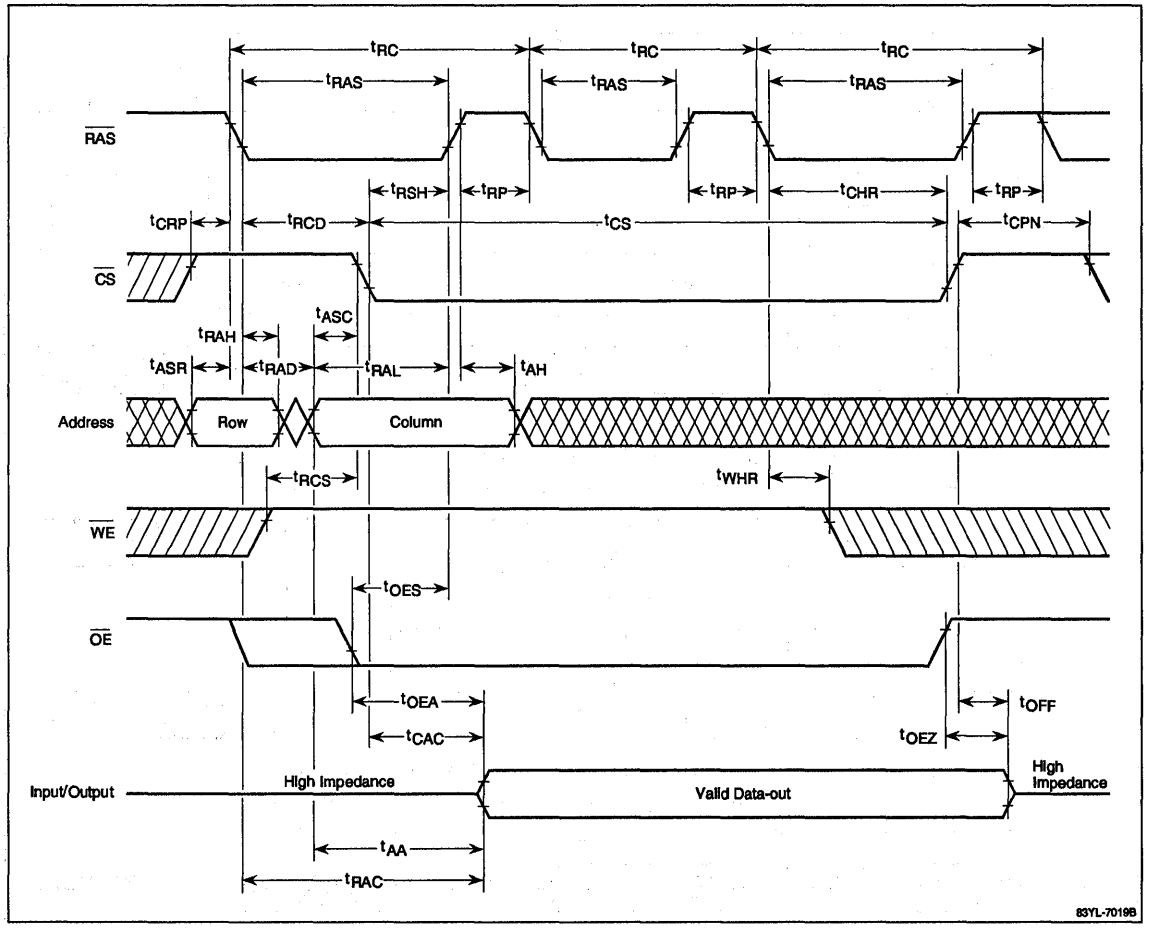
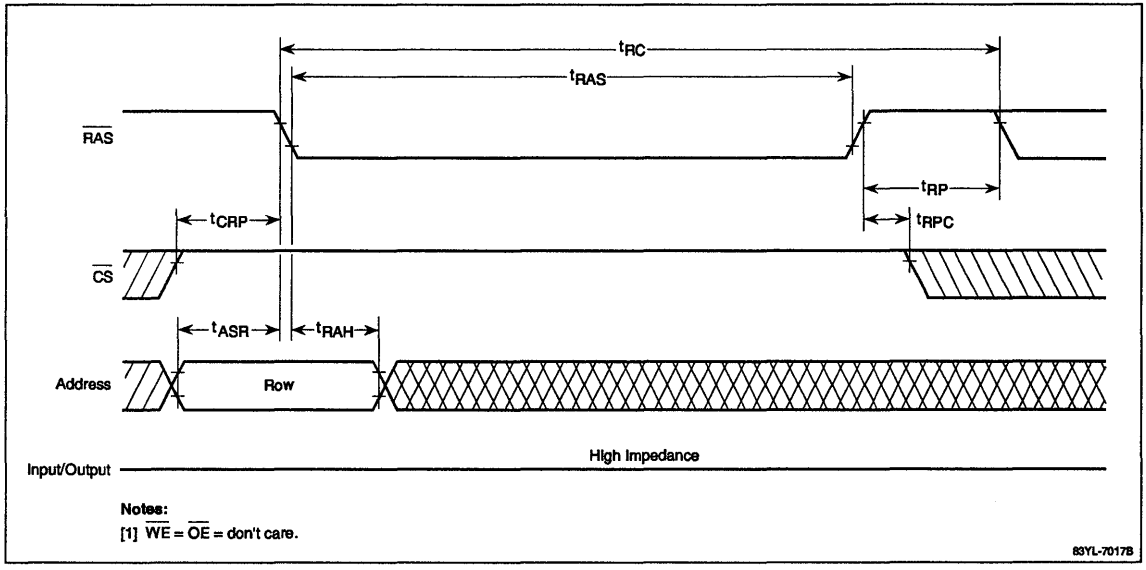
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Notes:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

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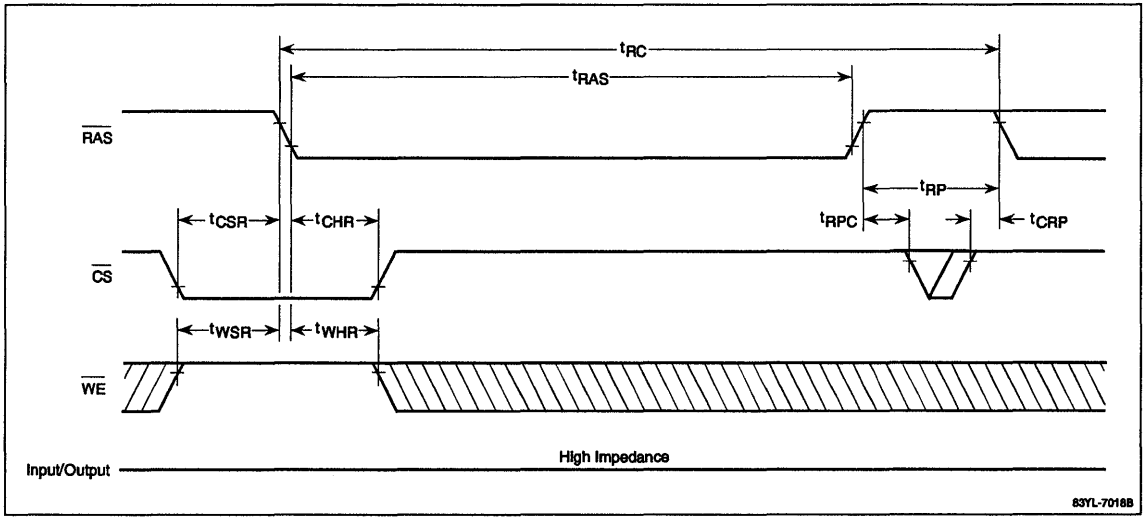
$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



83YL-7016B

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NEC
NEC Electronics Inc.

μPD424440/L, 42S4440/L
1,048,576 x 4-Bit Dynamic CMOS RAM With Four $\overline{CAS}$ controls

Description

The μPD424440/L and μPD42S4440/L are fast-page dynamic RAMs organized as 1,048,576 words by 4 bits and designed to operate from a single power supply. The four $\overline{CAS}$ controls, $\overline{CAS}_1$ - $\overline{CAS}_4$, are paired with I/O_1 - I/O_4

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
424440	+5 V
424440L	+3.3 V
42S4440	+5 V; self-refresh mode
42S4440L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O_{1-4} pins are controlled by $\overline{CAS}_{1-4}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by maintaining $\overline{CAS}$ low. The output returns to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh address. $\overline{RAS}$-only refresh cycles will also refresh all memory locations.

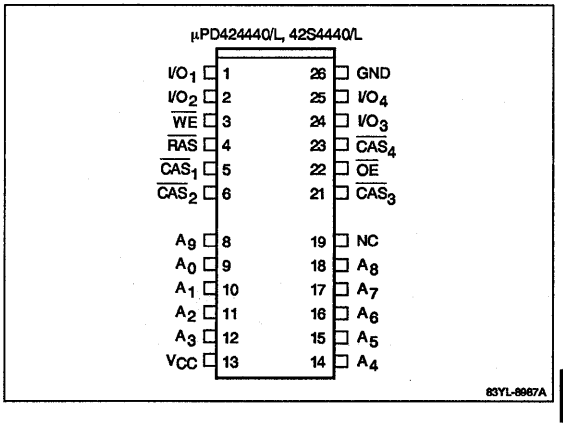
The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

- 1,048,576 by 4-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option
- Low power dissipation
- Four I/O and $\overline{CAS}$ pairs
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- 26/24-pin (350-mil) plastic SOJ package

Pin Configuration

26/24-Pin Plastic SOJ



Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}_1$ - $\overline{CAS}_4$	Column address strobes
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

5h

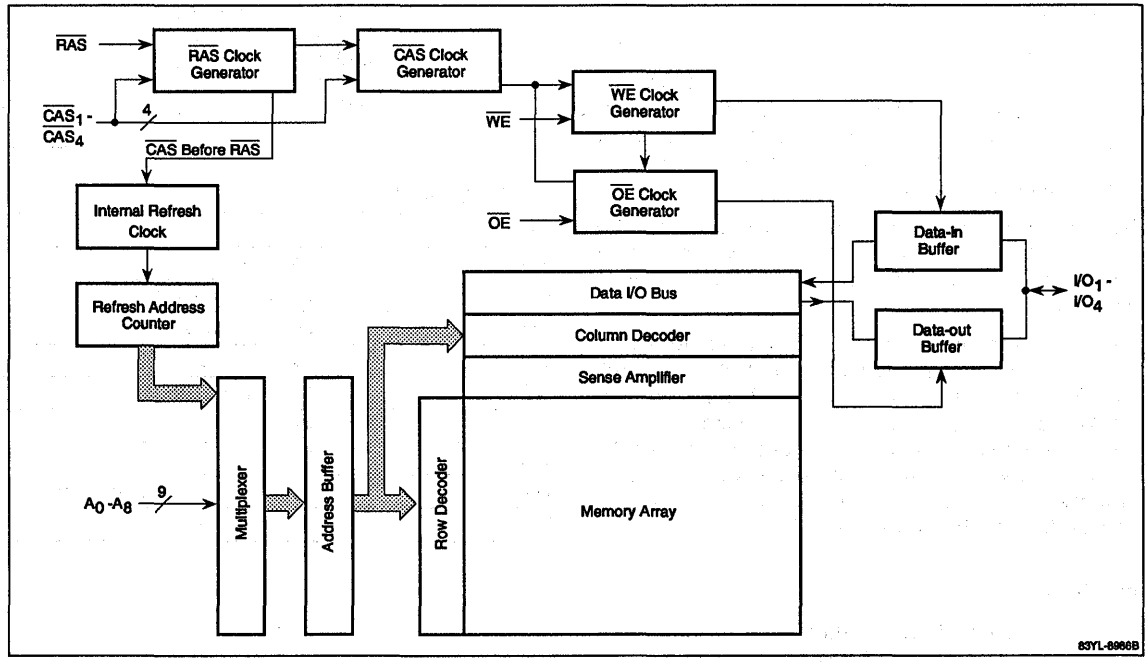
Ordering Information, Standard Devices

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	Power Supply	$\overline{CAS}$ Access Time (max)	Package
μPD424440LE-60	60 ns	40 ns	+5 V	20 ns	26/24-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD424440LLE-60	60 ns	40 ns	+3.3 V		
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			

Ordering Information, Self-Refresh Devices

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	Power Supply	$\overline{CAS}$ Access Time (max)	Package
μPD42S4440LE-60	60 ns	40 ns	+5 V	20 ns	26/24-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4440LLE-A60	60 ns	40 ns	+3.3 V		
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	
+5-volt devices	−1.0 to +7.0 V
+3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
+5-volt devices	50 mA
+3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{CAS}_1$ - $\overline{CAS}_4$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_4

Recommended Operating Conditions

		+5-Volt Devices			+3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} +0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.5		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

Self-Refresh Current

T_A = 0 to +70°C; V_{CC} = +5 V ±10% (42S4440) or +3.3 V ±0.3 V (42S4440L)

Symbol	42S4440	42S4440L	Conditions
I_{CC7}	300 μA max	100 μA max	I/O pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. Other input pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. $t_{RAS} \geq 100$ μs

5h

DC Characteristics; +5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$ (min); I_O = 0 mA
				300	μA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

DC Characteristics; +3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			500	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				100	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–5		5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–5		5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

AC Characteristics

T_A = 0 to +70°C

V_{CC} = +5.0 V ±10% or +3.3 V ±0.3 V

		-60		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5)		90		80		70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 3)
	I_{CC1} (+3.3)		80		70		60		
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5)		90		80		70	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 3)
	I_{CC3} (+3.3)		80		70		60		
Operating current, fast-page cycle, average	I_{CC4} (+5)		80		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 3)
	I_{CC4} (+3.3)		70		60		50		
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5)		90		80		70	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 3)
	I_{CC5} (+3.3)		80		70		60		
Access time from column address	t_{AA}		30		35		40	ns	(Notes 4, 5, 7)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 4, 5, 7)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		65		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		15		20		20	ns	(Notes 4, 5, 7)
Column address hold time	t_{CAH}	15		15		15		ns	
Delay time, column address to $\overline{CAS}$ high	t_{CAL}	30		35		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		ns	
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	–35		–40		–50		ns	Self-refresh devices
Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	t_{CLCH}	5		5		5		ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		12		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		75		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		ns	
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in hold time	t_{DH}	15		15		15		ns	
Data-in setup time	t_{DS}	0		0		0		ns	
Masked write hold time referenced to $\overline{RAS}$	t_{MRH}	0		0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		20	ns	(Notes 4, 5, 7)
$\overline{OE}$ data delay time	t_{OED}	15		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	(Note 8)
Output disable from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	(Note 8)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Note 5)
Fast-page read or write cycle time	t_{PC}	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with exended data output	t_{PRWC}	85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 4, 5, 7)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	(Note 7)
Row address hold time	t_{RAH}	10		10		10		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		μs	Self-refresh devices
Random read or write cycle time	t_{RC}	120		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	ns	(Note 7)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_8
			128		128		128	ms	Self-refresh devices

5h

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	120		130		150		ns	Self-refresh devices
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		25		ns	
Read-modify-write cycle time	t_{RWC}	165		175		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		ns	
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Rise and fall times	t_T	3	50	3	50	3	50	ns	
Write command hold time	t_{WCH}	15		15		15		ns	
Write command setup time	t_{WCS}	0		0		0		ns	
Write command pulse width	t_{WP}	15		15		15		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(4) Ac measurements assume t_T = 5 ns.

(5) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max); if $t_{RAD} \geq t_{RAD}$ (max) access time is defined by t_{AA} (max).

(8) t_{OFF} (max) defines the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(9) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(10) Parameter t_{WP} is applicable for late-write or read-modify-write cycles. In early-write cycles, t_{WCH} (min) should be satisfied.

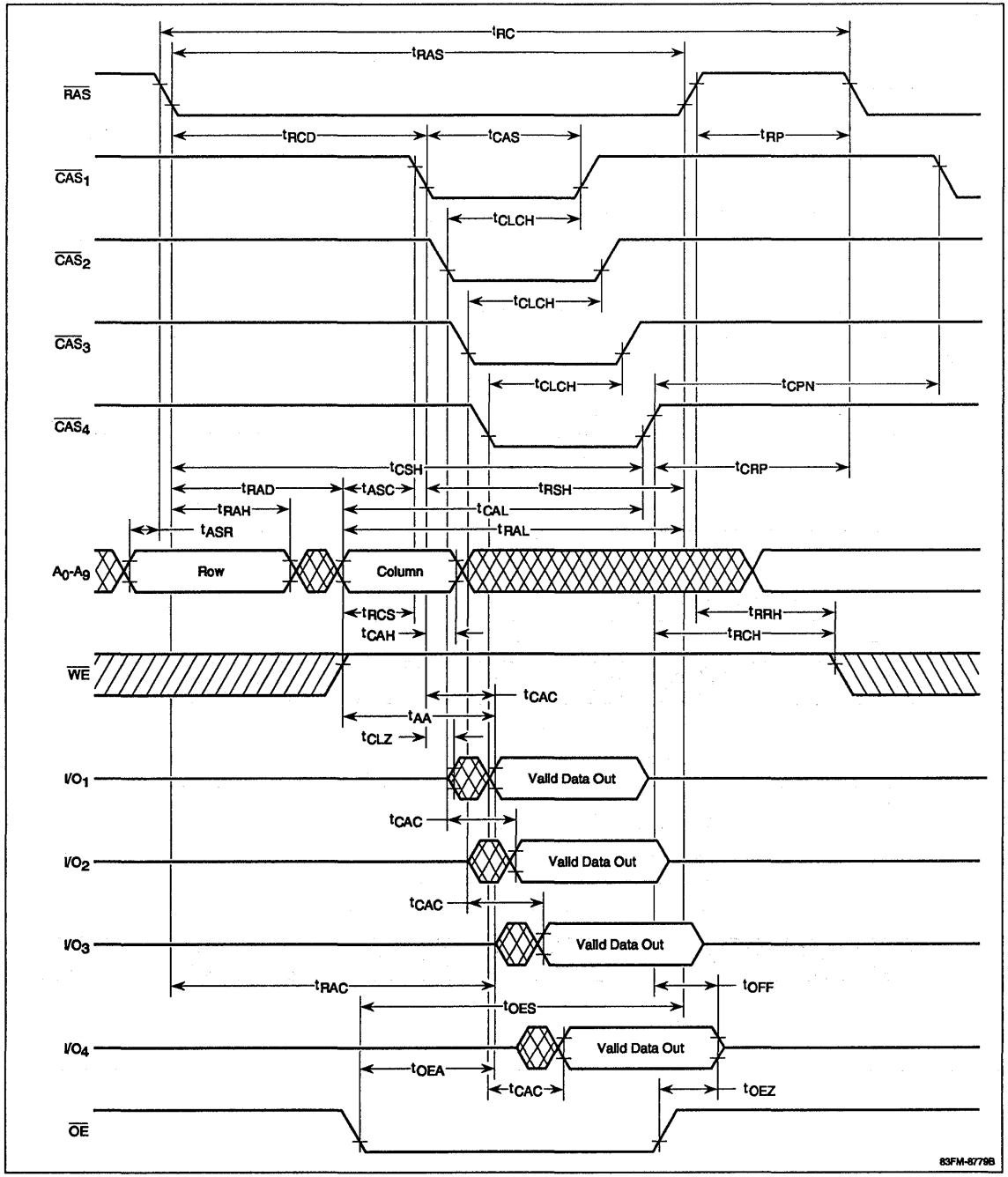
(11) These parameters are referenced to the leading edge of one of the $\overline{CAS}$ signals in early write cycles and to the leading edge of $\overline{WE}$ in late write or read-modify-write cycles.

(12) These parameters are the conditions defining read-modify-write cycles.

(13) Load = 2 TTl (–1 mA, +4 mA) loads and 100 pF. For 3.3-volt devices, V_{OH} = 2.0 V and V_{OL} = 0.8 V (ac reference levels).

Timing Waveforms

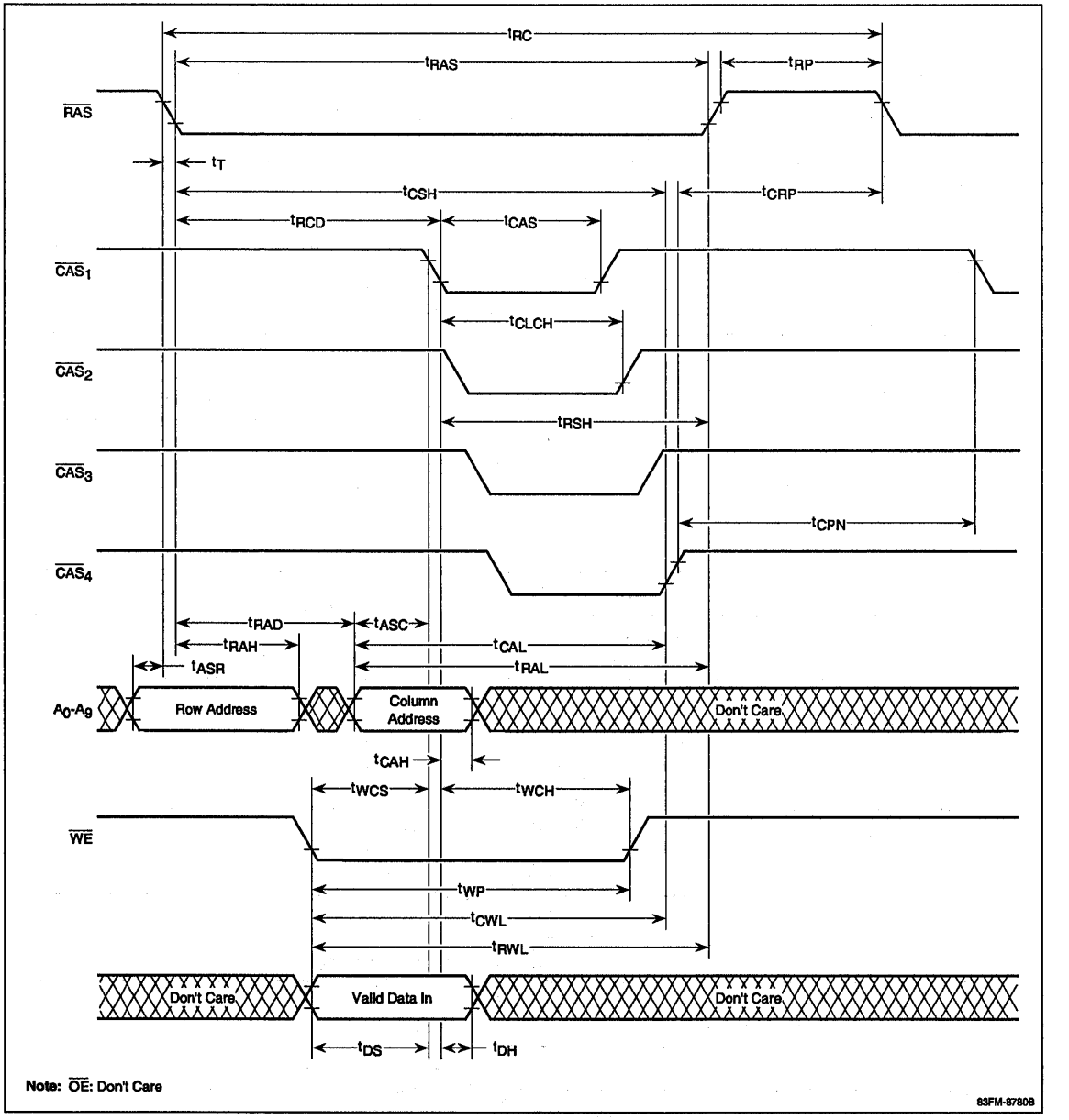
Read Cycle



5h

Timing Waveforms (cont)

Early Write Cycle

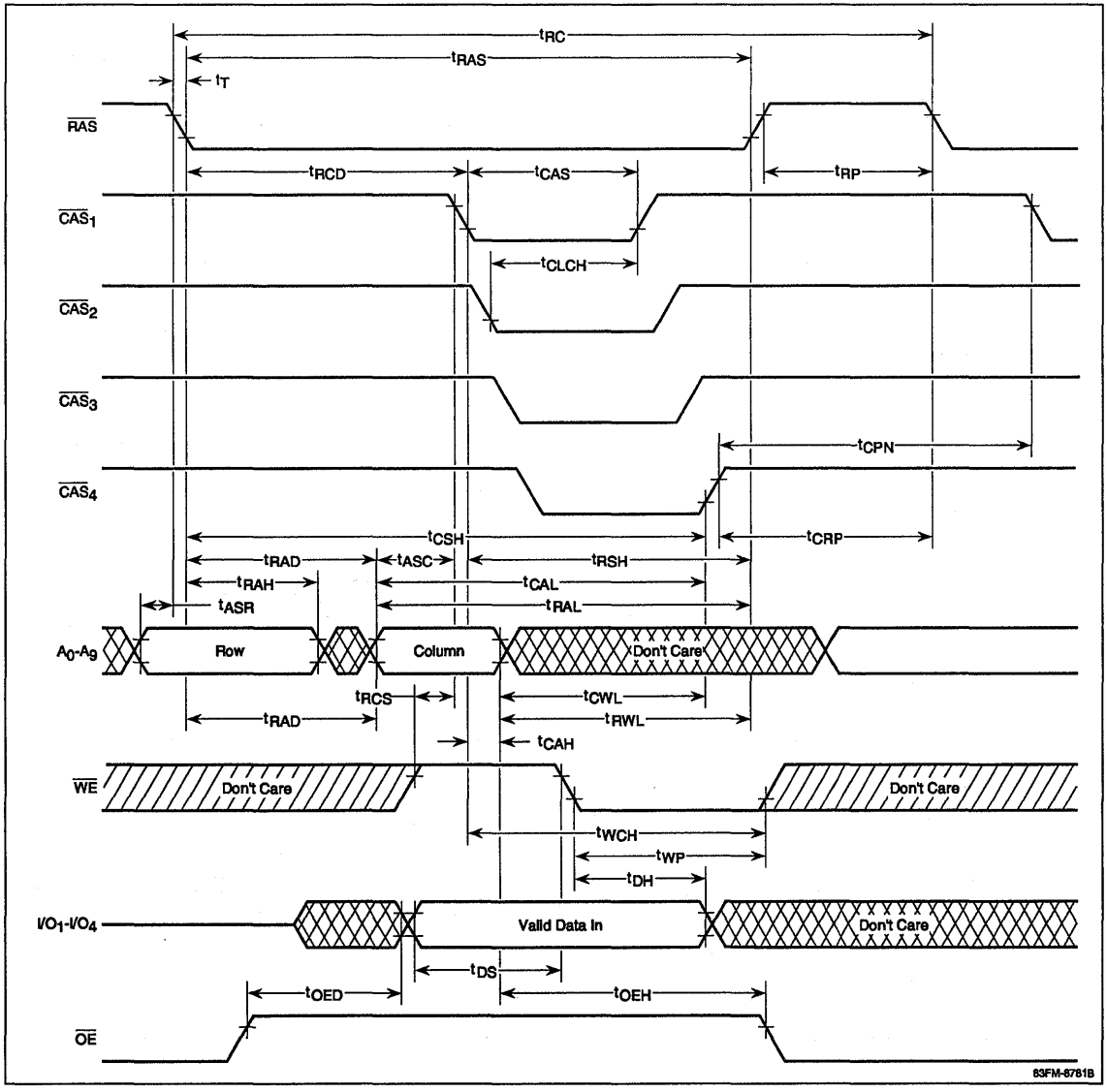


Note: $\overline{OE}$: Don't Care

83FM-8780B

Timing Waveforms (cont)

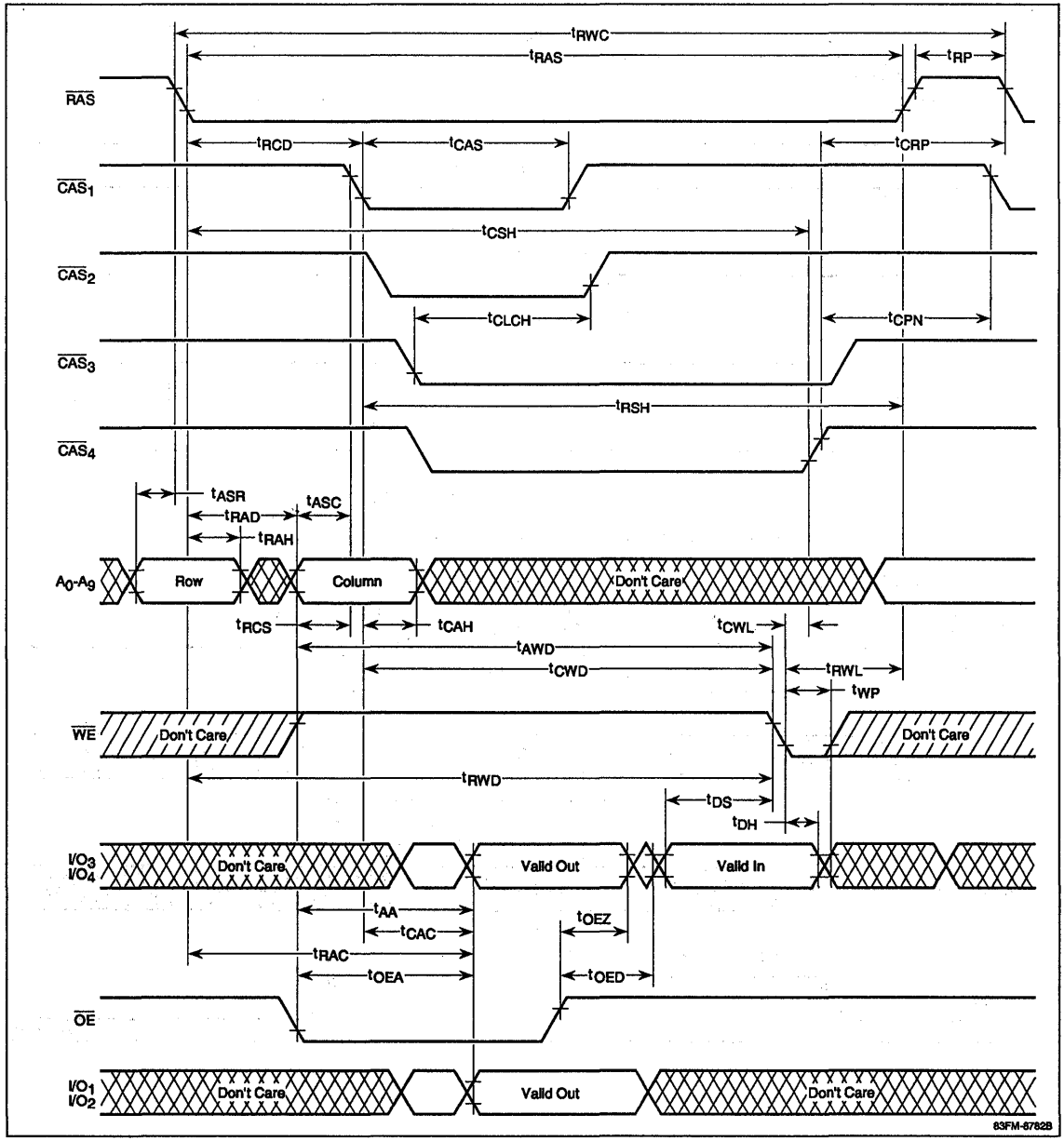
Late Write Cycle



5h

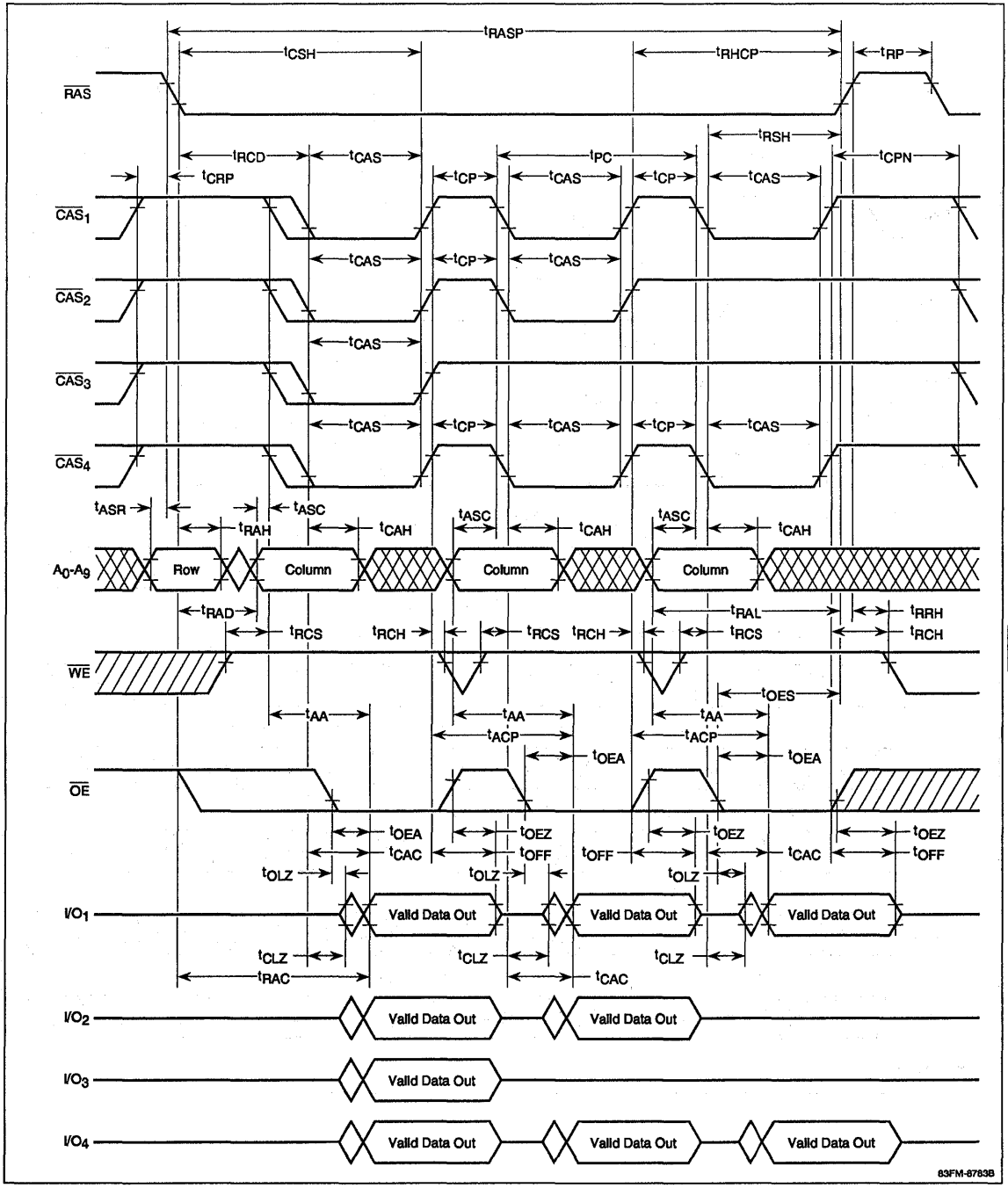
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

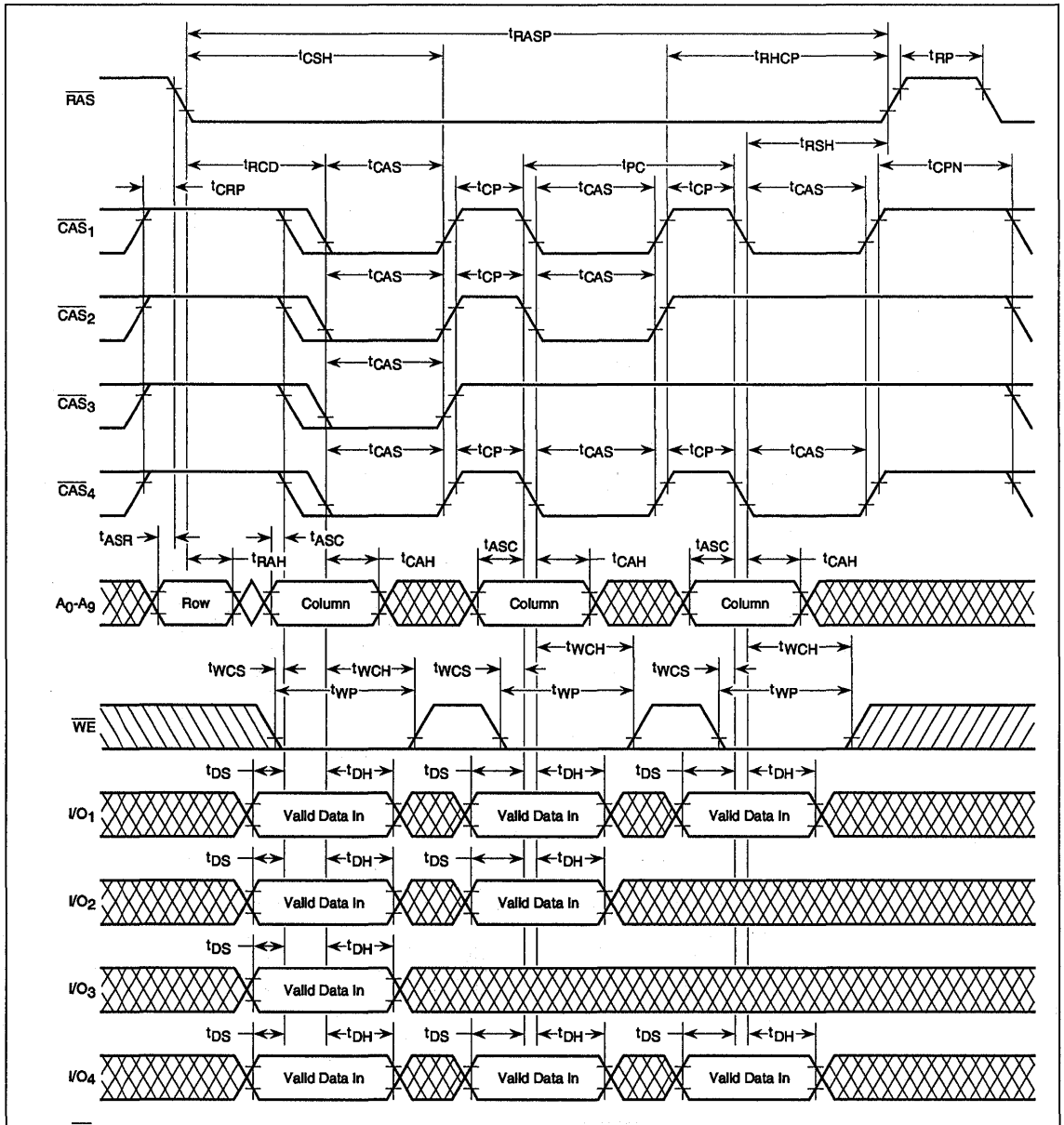
Fast-Page Read Cycle



5h

Timing Waveforms (cont)

Fast-Page Early Write Cycle

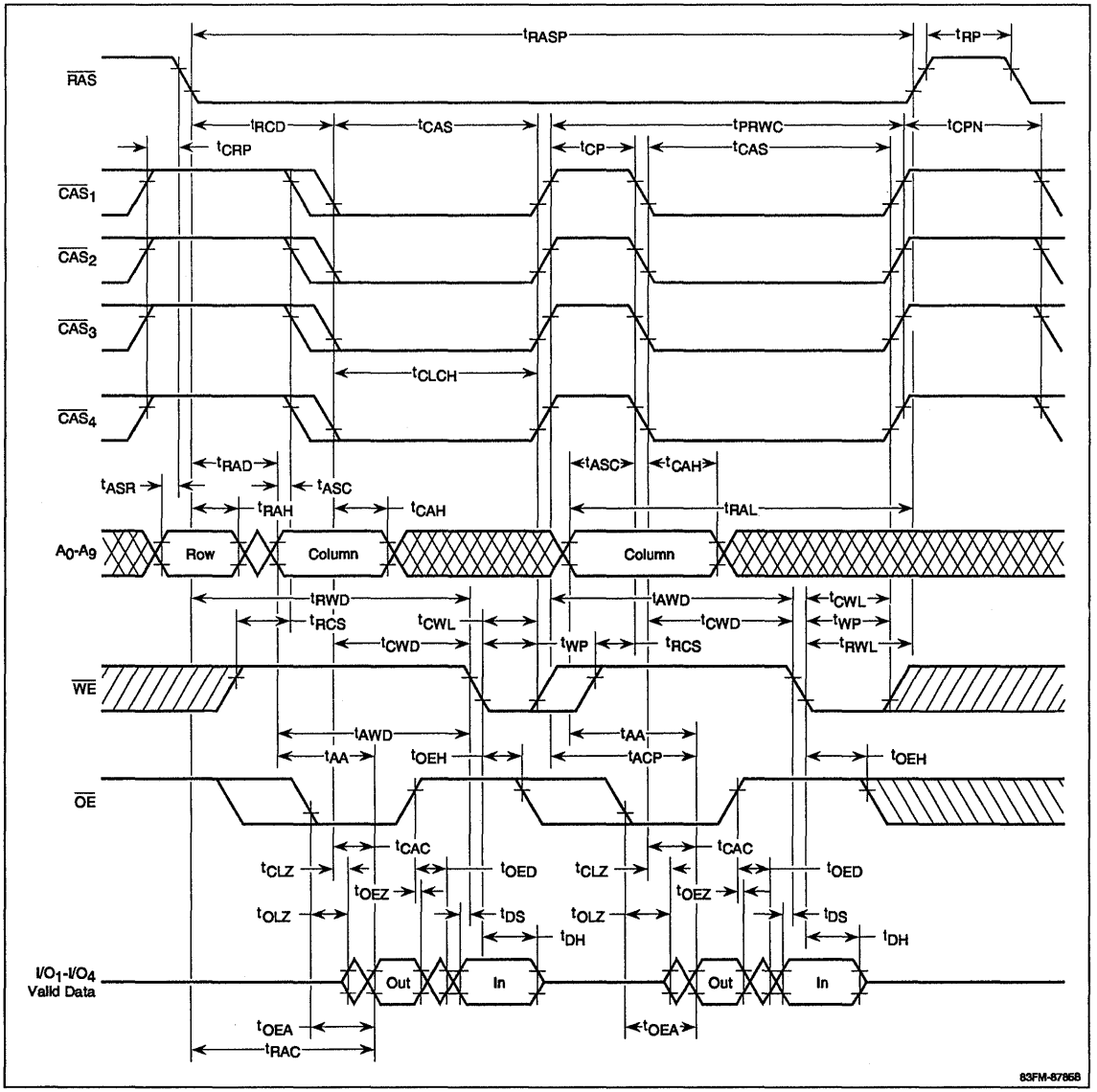


Note: $\overline{OE}$: Don't Care

83FM-8784B

Timing Waveforms (cont)

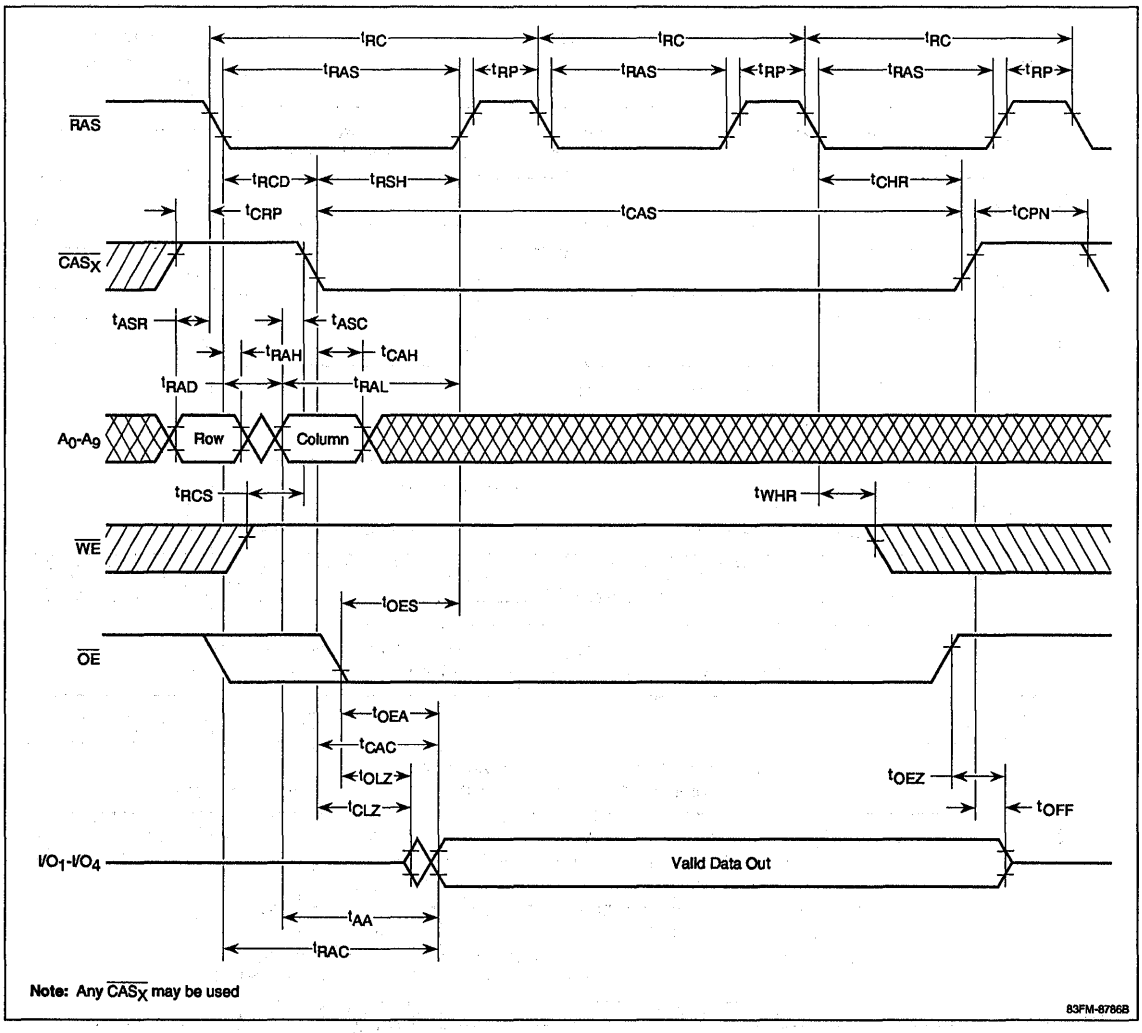
Fast-Page Read-Write/Read-Modify-Write Cycle



5h

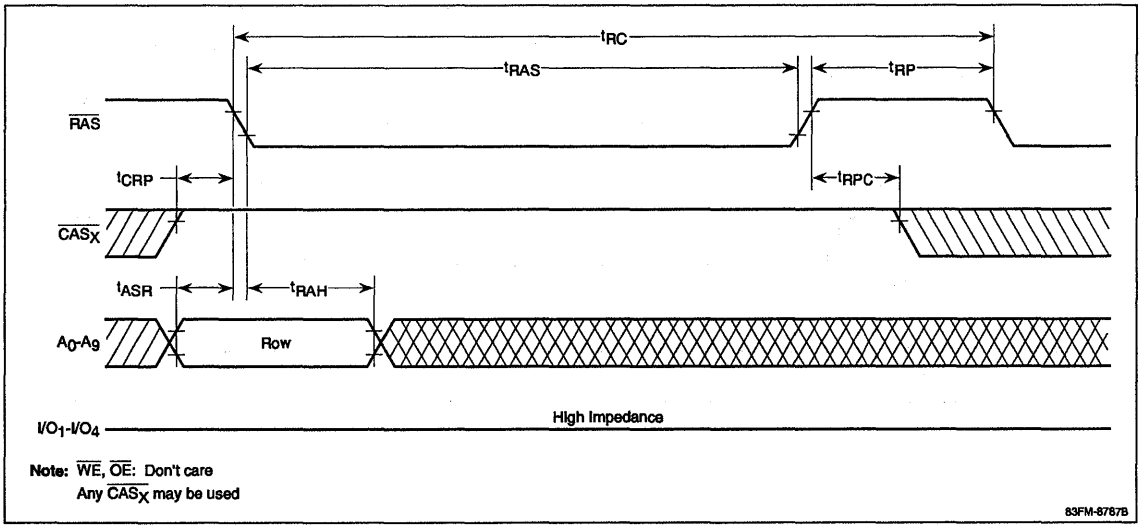
Timing Waveforms (cont)

Hidden Refresh Cycle

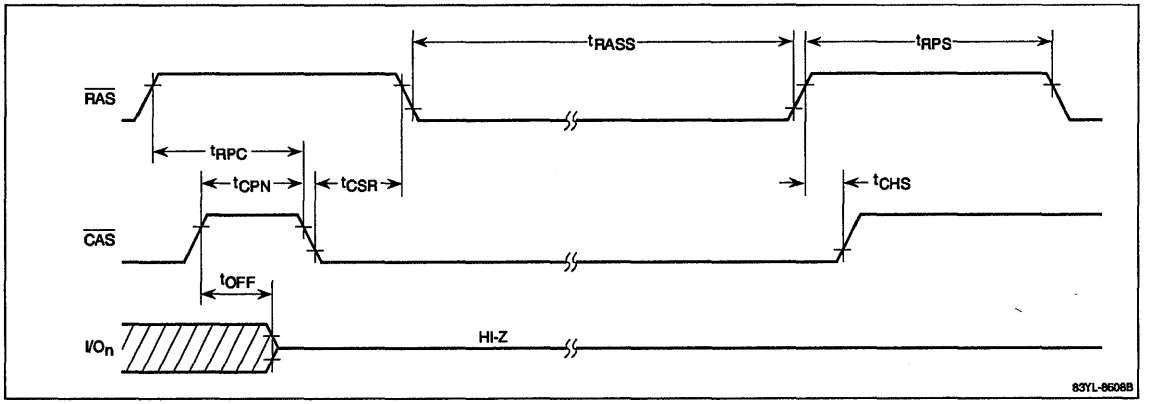


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



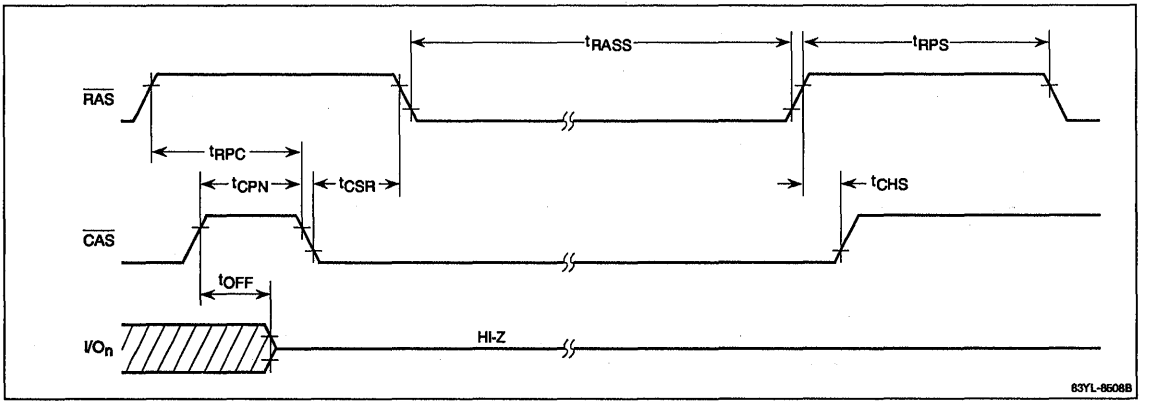
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



5h

Timing Waveforms (cont)

CBR Self-Refresh Cycle



NEC

Section 6
4M DRAMs (512K x 8/9)

μPD	Organization	Features	
424800A	512K x 8	Fast-page	6a
424800L	512K x 8	Fast-page; 3.3-volt	
42S4800A	512K x 8	Fast-page; self-refresh	
42S4800L	512K x 8	Fast-page; self-refresh; 3.3-volt	
424810A	512K x 8	Fast-page; write-per-bit	6b
424810L	512K x 8	Fast-page; write-per-bit; 3.3-volt	
42S4810A	512K x 8	Fast-page; write-per-bit; self-refresh	
42S4810L	512K x 8	Fast-page; write-per-bit; self-refresh; 3.3-volt	
424900A	512K x 9	Fast-page	6c
424900L	512K x 9	Fast-page; 3.3-volt	
42S4900A	512K x 9	Fast-page; self-refresh	
42S4900L	512K x 9	Fast-page; self-refresh; 3.3-volt	

μPD424800A/L, 42S4800A/L
524,288 x 8-Bit
Dynamic CMOS RAM

Description

The μPD424800A/L and μPD42S4800A/L are fast-page dynamic RAMs organized as 524,288 words by 8 bits and designed to operate from a single power supply.

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
424800A	+5 V
424800L	+3.3 V
42S4800A	+5 V; self-refresh mode
42S4800L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh address. $\overline{RAS}$-only refresh cycles will also refresh all memory locations.

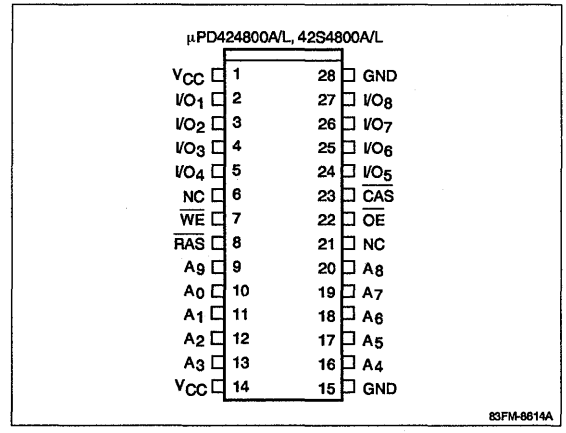
The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

- 524,288 by 8-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 1024 refresh cycles every 16 ms
- 28-pin SOJ, ZIP, and TSOP plastic packaging

Pin Configurations

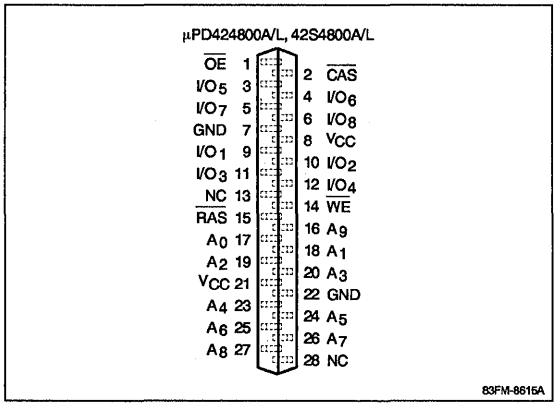
28-Pin Plastic SOJ



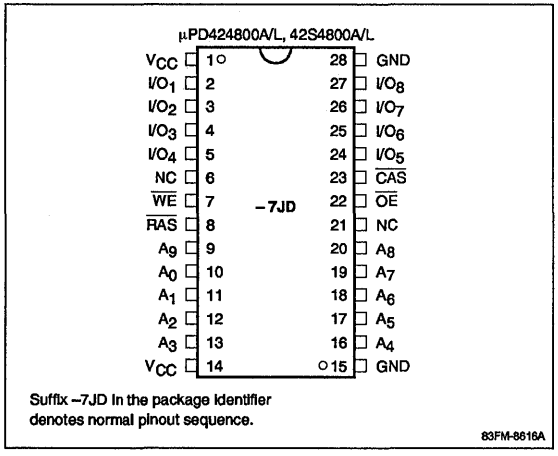
6a

Pin Configurations (cont)

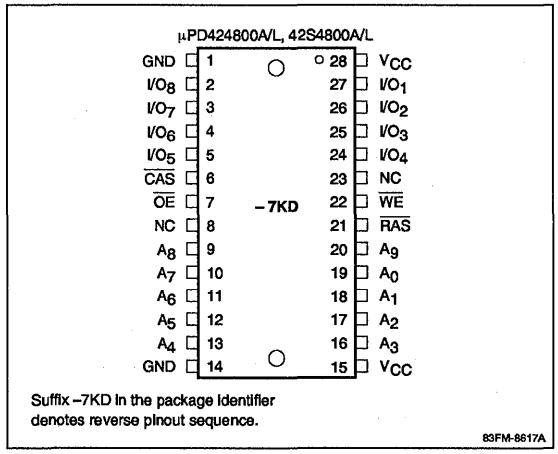
28-Pin Plastic ZIP



28-Pin Plastic TSOP (Normal Pinouts)



28-Pin Plastic TSOP (Reverse Pinouts)



Pin Identification

Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

Ordering Information, μPD424800A (+5-volt power)

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Package
μPD424800ALE-60	60 ns	40 ns	20 ns	28-pin plastic SOJ
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD424800AV-60	60 ns	40 ns	20 ns	28-pin plastic ZIP
V-70	70 ns	45 ns		
V-80	80 ns	50 ns		
μPD424800AG5-60	60 ns	40 ns	20 ns	28-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD424800AG5M-60	60 ns	40 ns	20 ns	28-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD424800L (+3.3-volt power)

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Package
μPD424800LLE-A60	60 ns	40 ns	20 ns	28-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD424800LV-A60	60 ns	40 ns	20 ns	28-pin plastic ZIP
V-A70	70 ns	45 ns		
V-A80	80 ns	50 ns		
μPD424800LG5-A60	60 ns	40 ns	20 ns	28-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD424800LG5M-A60	60 ns	40 ns	20 ns	28-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

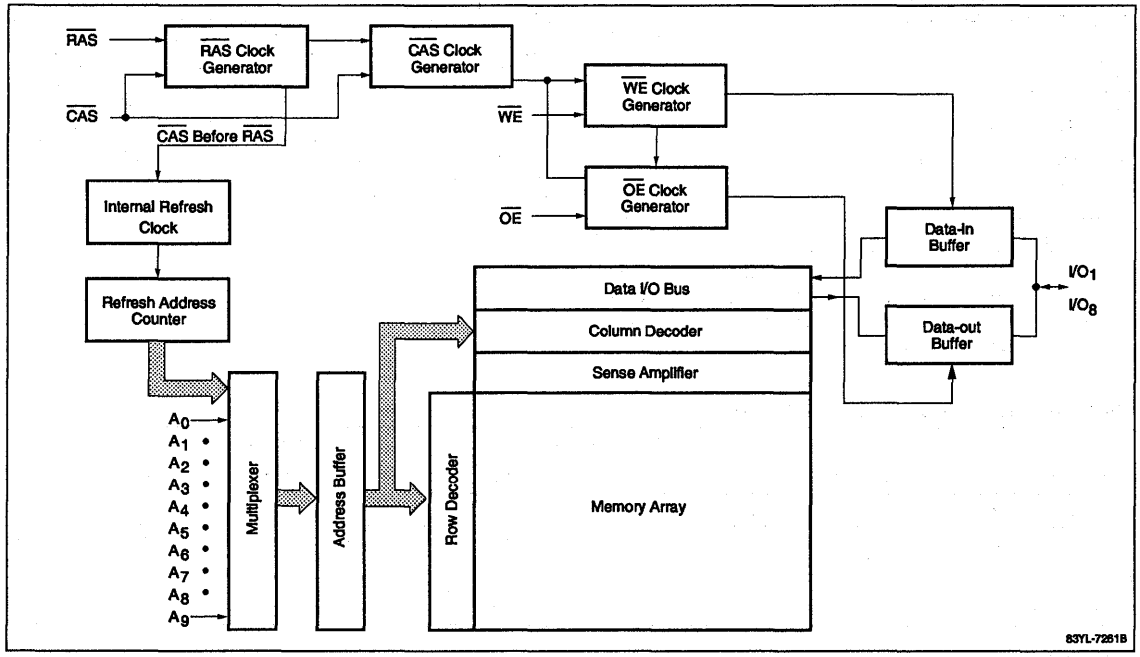
Ordering Information, μPD42S4800A (+ 5-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4800ALE-60	60 ns	40 ns	20 ns	300 μA	28-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4800AV-60	60 ns	40 ns	20 ns	300 μA	28-pin plastic ZIP
V-70	70 ns	45 ns			
V-80	80 ns	50 ns			
μPD42S4800AG5-60	60 ns	40 ns	20 ns	300 μA	28-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns			
G5-80	80 ns	50 ns			
μPD42S4800AG5M-60	60 ns	40 ns	20 ns	300 μA	28-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns			
G5M-80	80 ns	50 ns			

Ordering Information, μPD42S4800L (+ 3.3-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4800LLE-A60	60 ns	40 ns	20 ns	100 μA	28-pin plastic SOJ
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			
μPD42S4800LV-A60	60 ns	40 ns	20 ns	100 μA	28-pin plastic ZIP
V-A70	70 ns	45 ns			
V-A80	80 ns	50 ns			
μPD42S4800LG5-A60	60 ns	40 ns	20 ns	100 μA	28-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns			
G5-A80	80 ns	50 ns			
μPD42S4800LG5M-A60	60 ns	40 ns	20 ns	100 μA	28-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns			
G5M-A80	80 ns	50 ns			

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	I/O_1 - I/O_8
Standby	H	X	X	X	High-Z
Refresh cyle	L	H	X	X	High-Z
Read cycle	L	L	H	L	Data output
Write cycle	L	L	L	H	Data input
___	L	L	H	H	High-Z

X = don't care.

6a

Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
5-volt devices	50 mA
3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_8

Recommended Operating Conditions

		5-Volt Devices			3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.5		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

Self-Refresh Current

T_A = 0 to +70°C; V_{CC} = +5 V ±10% (42S4800A) or +3.3 V ±0.3 V (42S4800L)

Symbol	42S4800A	42S4800L	Conditions
I_{CC7}	300 μA max	100 μA max	I/O pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. Other input pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. $t_{RAS} \geq 100$ μs

DC Characteristics; 5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				300	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

DC Characteristics; 3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			500	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				100	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–5		5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–5		5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

AC Characteristics

T_A = 0 to +70°C

μPD424800A, 42S4800A: V_{CC} = +5.0 V ±10%

μPD424800L, 42S4800L: V_{CC} = +3.3 V ±0.3 V

		-60		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5)		100		90		80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
	I_{CC1} (+3.3)		100		80		70		
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5)		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
	I_{CC3} (+3.3)		100		80		70		
Operating current, fast-page cycle, average	I_{CC4} (+5)		80		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
	I_{CC4} (+3.3)		80		70		60		
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5)		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
	I_{CC5} (+3.3)		100		80		70		
Access time from column address	t_{AA}		30		35		40	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		ns	(Note 15)
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	–35		–40		–50		ns	For 42S4800A/L only

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	(Notes 4, 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		75		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		50		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		20		20		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	(Note 9)
Output disable from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t_{PC}	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with exended data output	t_{PRWC}	85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 3, 4, 7, 8)

AC Characteristics (cont)

Parameter	Symbol	-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		10		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		μs	For 42S4800A/L
Random read or write cycle time	t_{RC}	120		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	120		130		150		ns	For 42S4800A/L
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Read-modify-write cycle time	t_{RWC}	165		175		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Rise and fall times	t_T	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		ns	(Note 14)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Write command pulse width	t_{WP}	15		15		15		ns	(Note 12)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF. For 3.3-volt devices, V_{OH} = 2.0 V and V_{OL} = 0.8 V.

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max).
If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

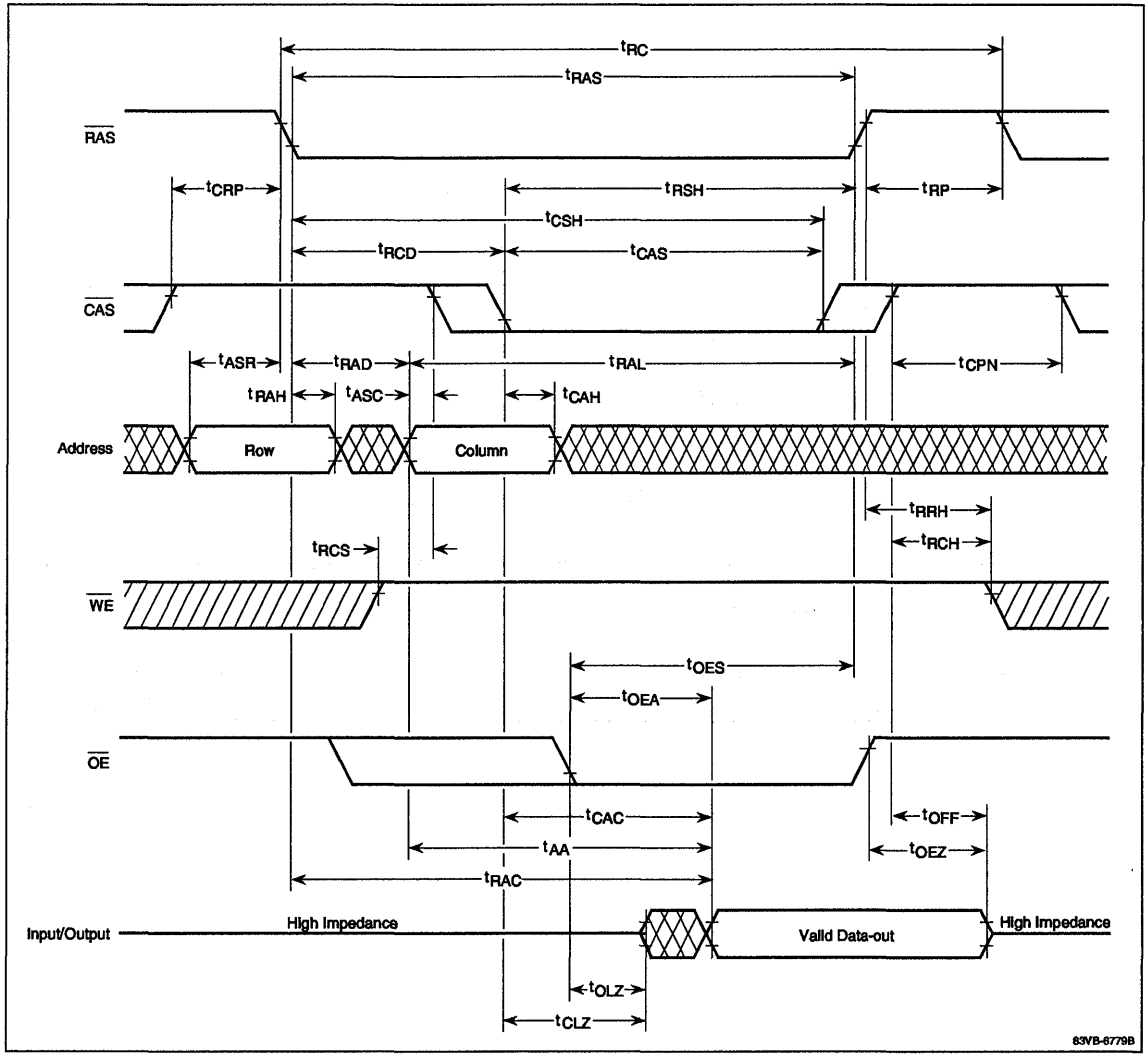
(13) These parameters are referenced to the falling edge of one of the $\overline{CAS}$ signals for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD} and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) Holding $\overline{CAS}$ low prior to $\overline{RAS}$ going negative will initiate a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (t_{CSR} and t_{CHR} must be satisfied).

Timing Waveforms

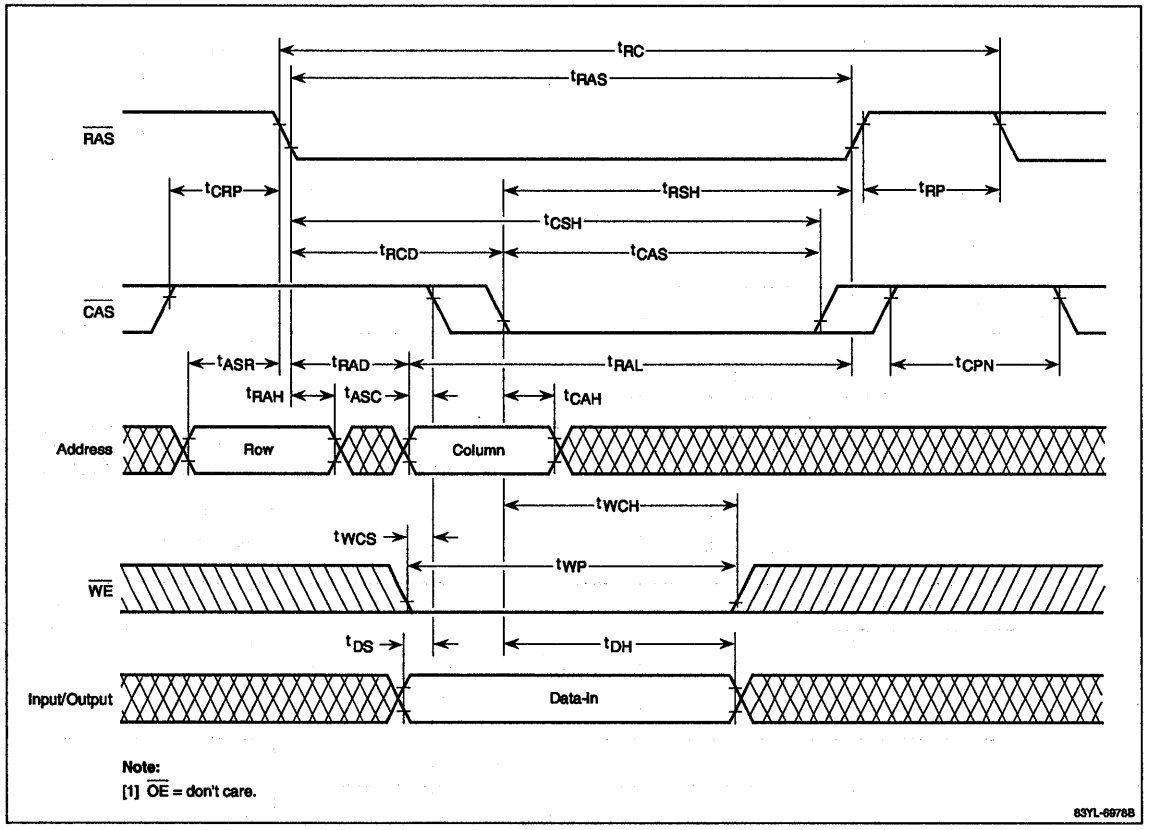
Read Cycle



6a

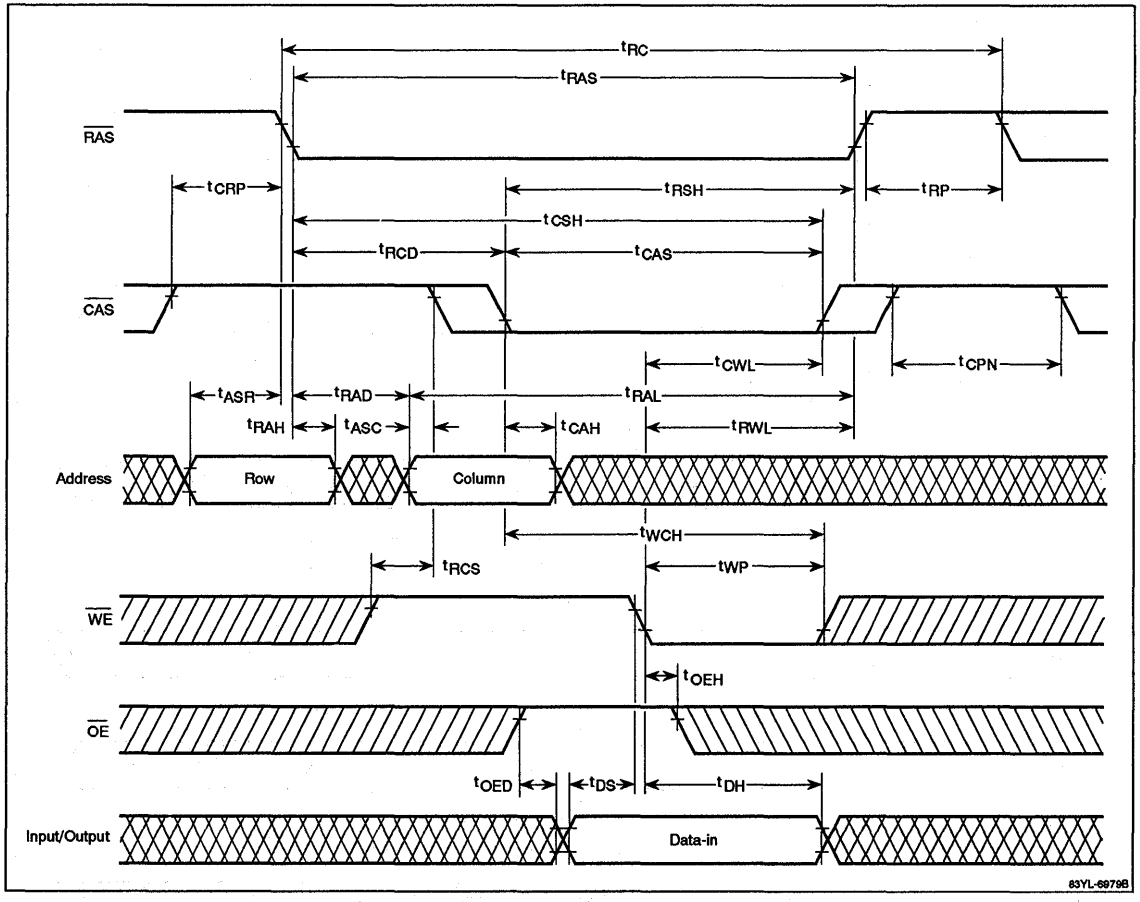
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

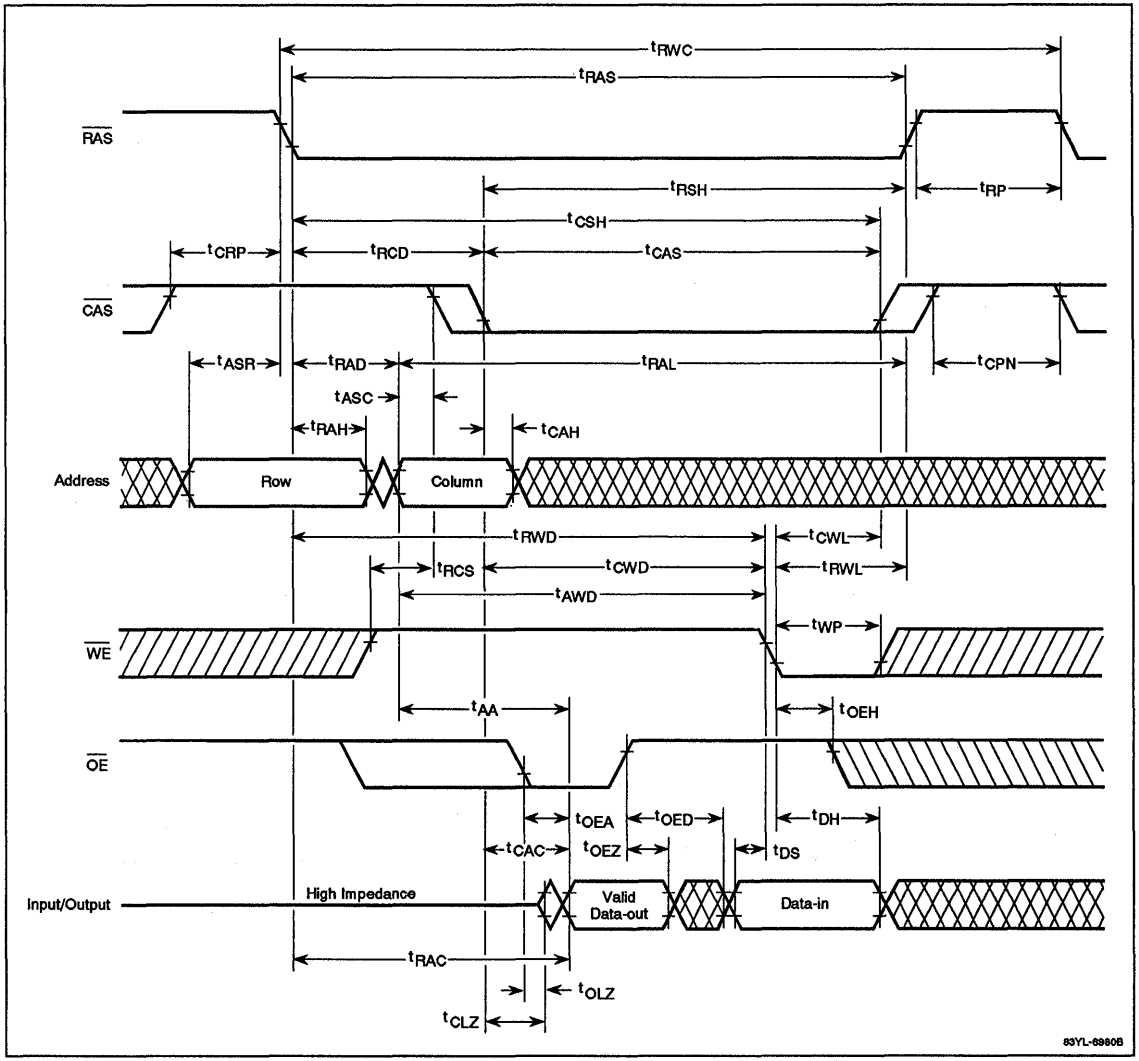
Late Write Cycle



6a

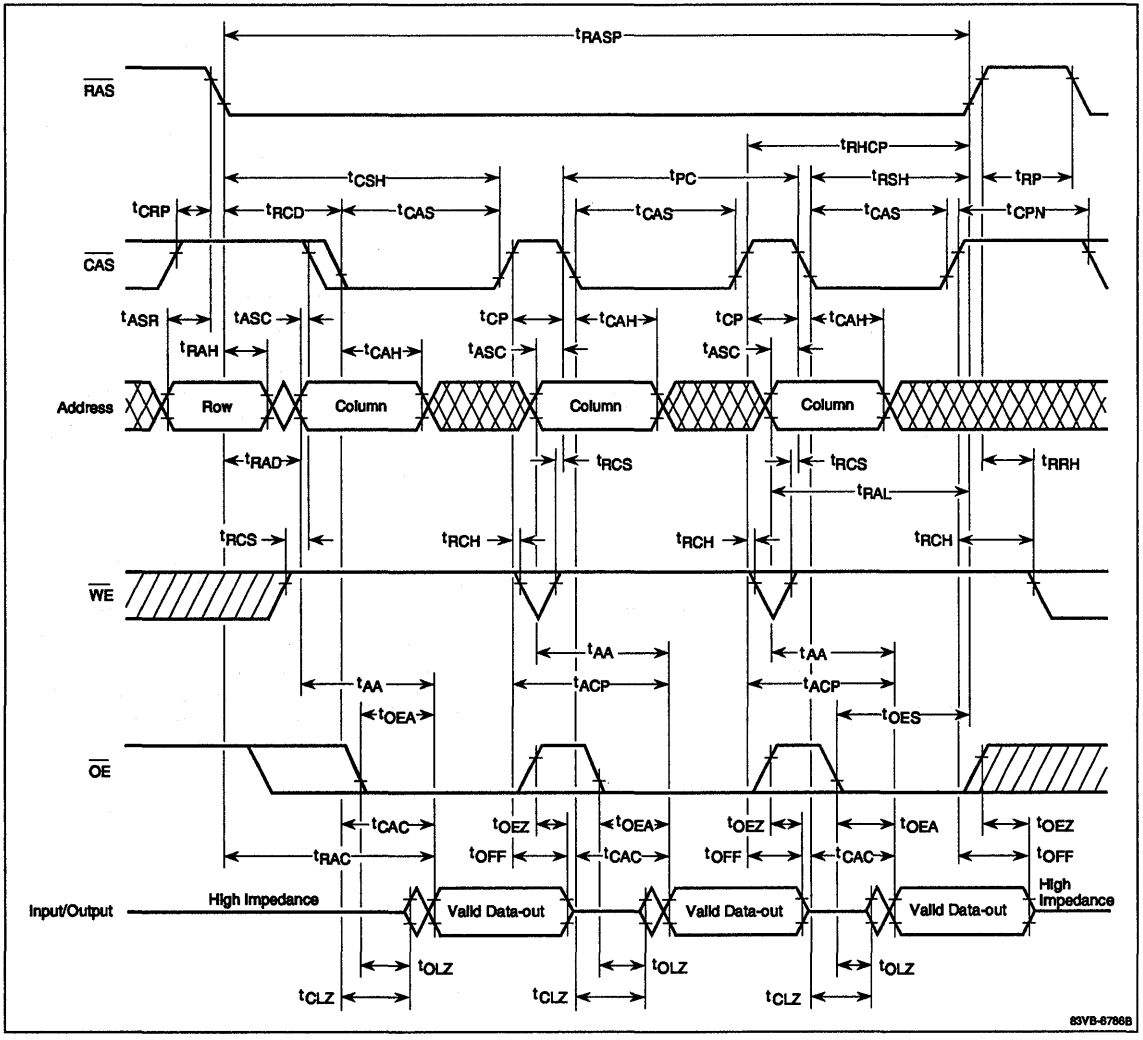
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Fast-Page Read Cycle



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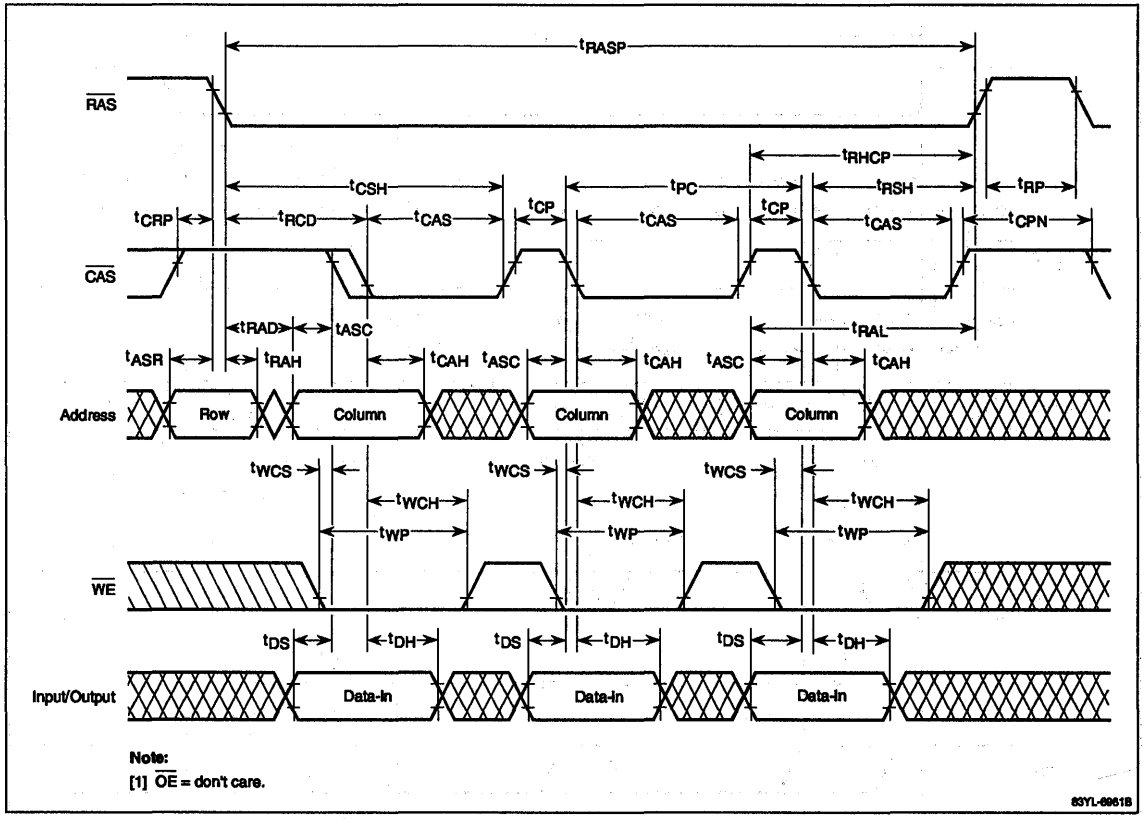
Timing Waveforms (cont)

Fast-Page Early Write Cycle

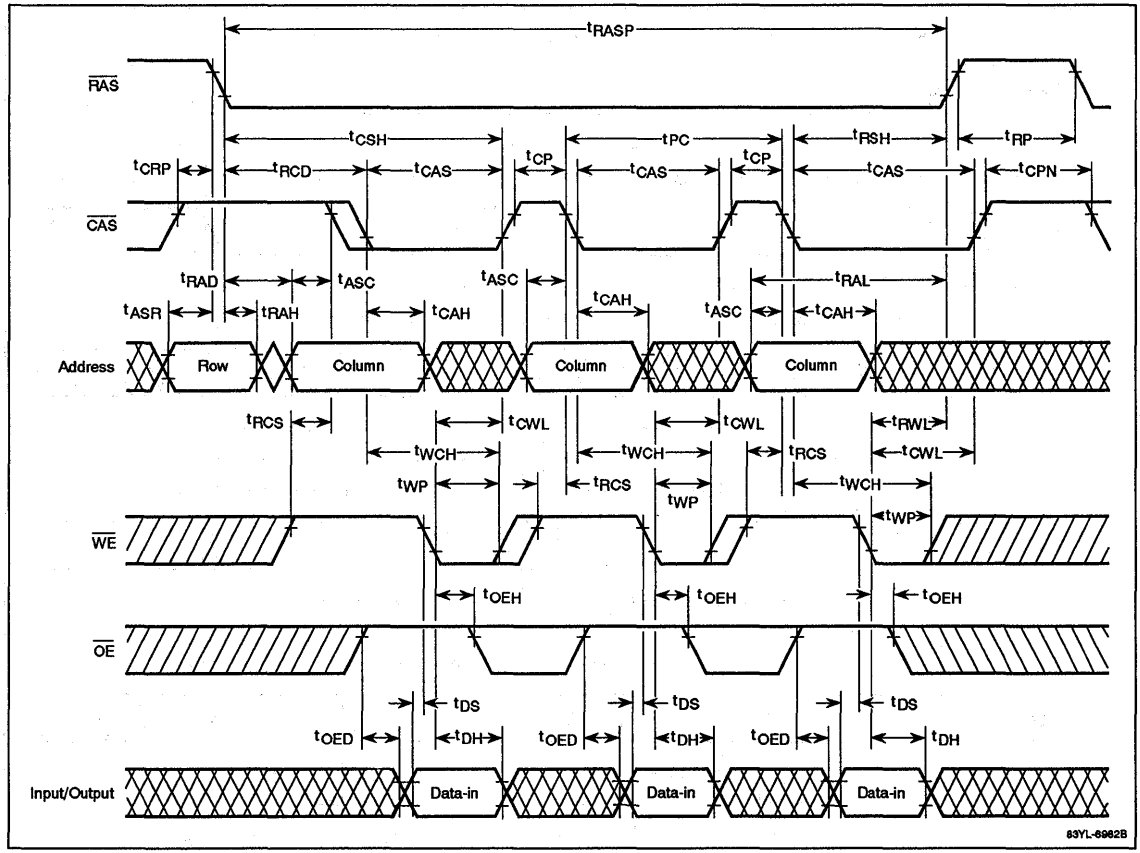


Note:
[1] $\overline{OE}$ = don't care.

83YL-6961B

Timing Waveforms (cont)

Fast-Page Late Write Cycle



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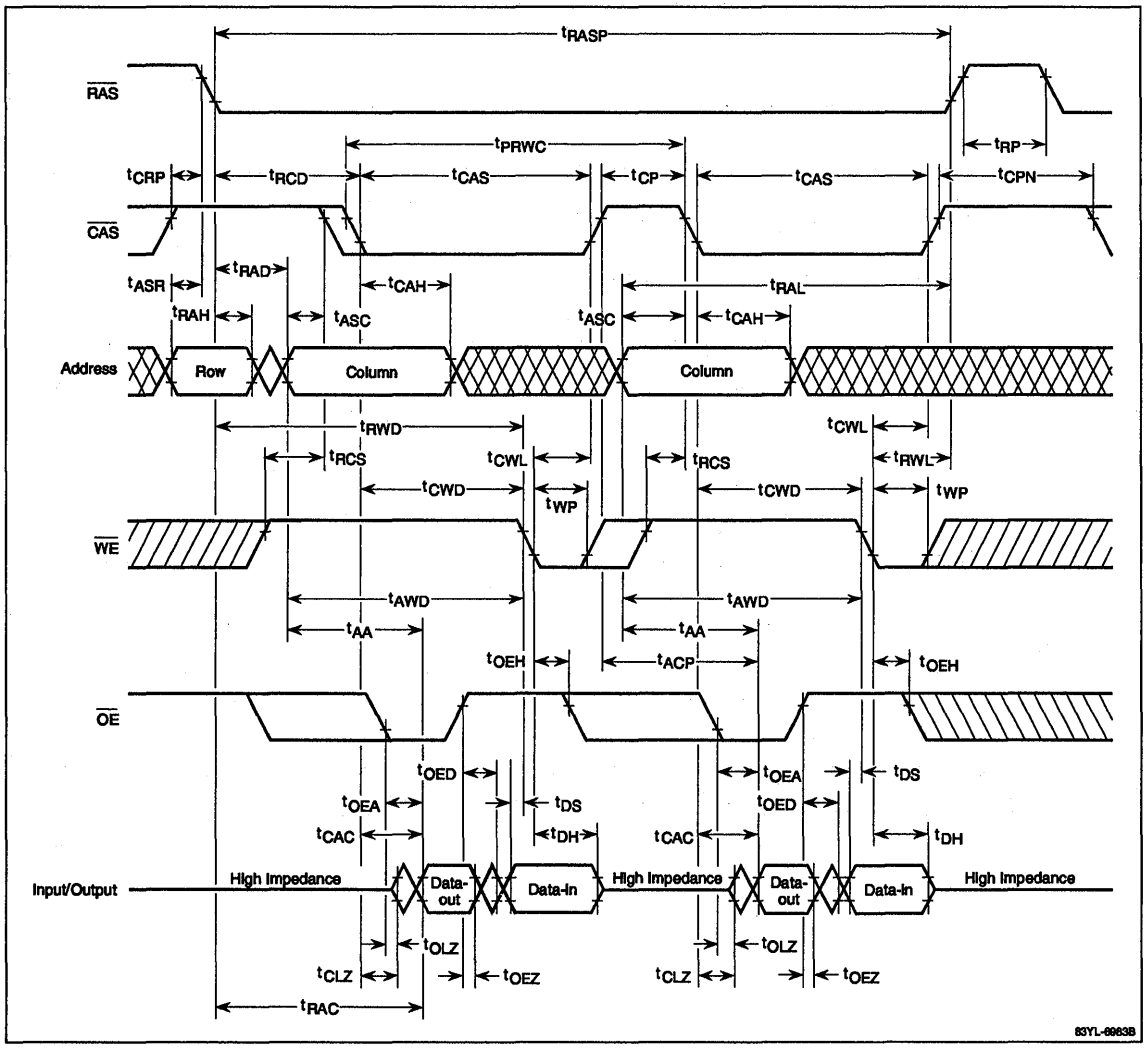
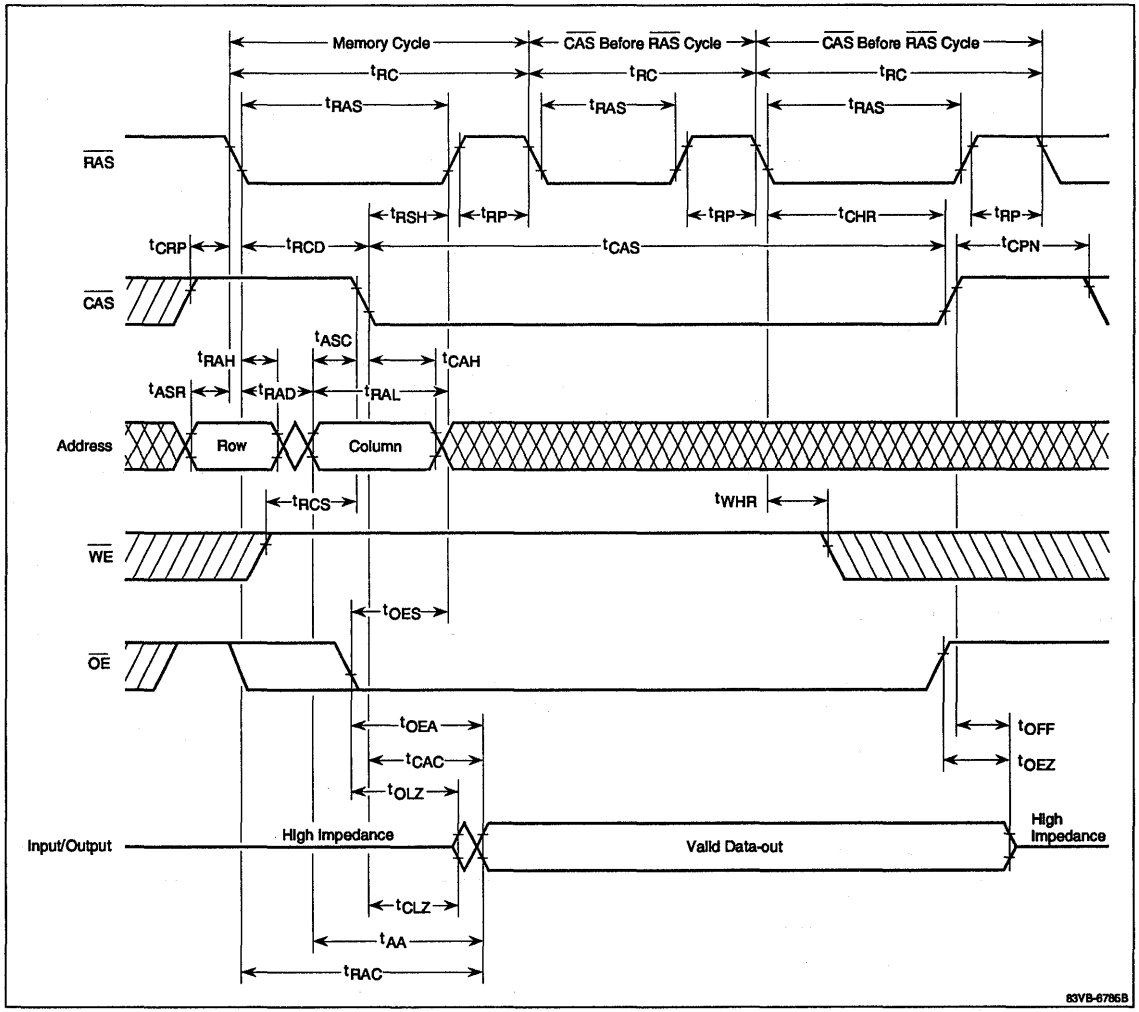
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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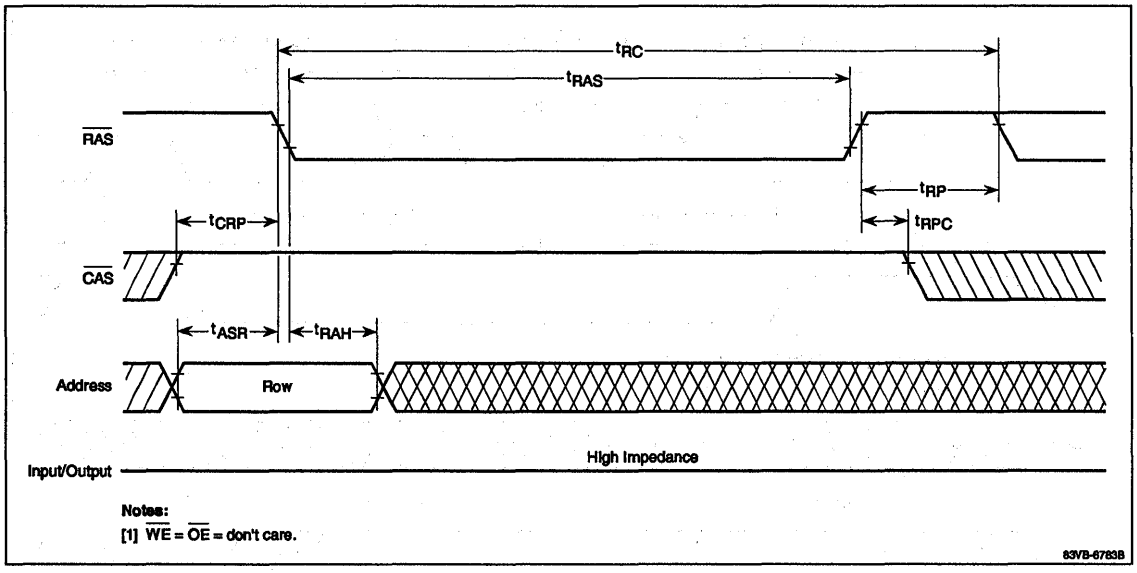
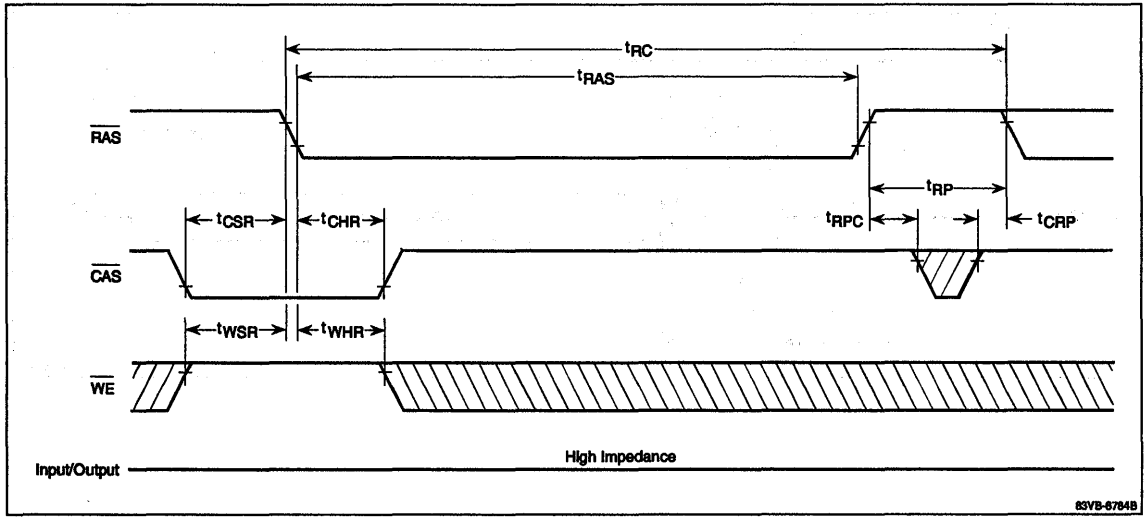
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle

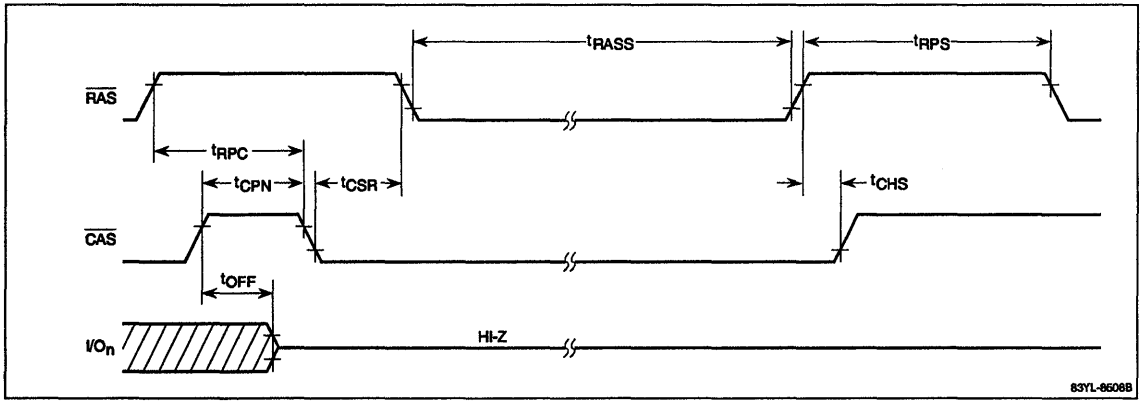


$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

CBR Self-Refresh Cycle



6a

μPD424810A/L, 42S4810A/L
524,288 x 8-Bit
Dynamic CMOS RAM

Description

The μPD424810A/L and μPD42S4810A/L are fast-page dynamic RAMs with the write-per-bit option, organized as 524,288 words by 8 bits, and designed to operate from a single power supply.

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
424810A	+5 V
424810L	+3.3 V
42S4810A	+5 V; self-refresh mode
42S4810L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh address. $\overline{RAS}$-only refresh cycles will also refresh all memory locations.

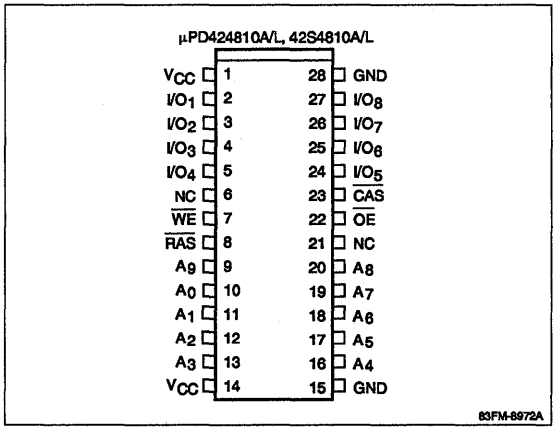
The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

- 524,288 by 8-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option
- Write-per-bit option; independent write control on eight I/O's
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 1024 refresh cycles every 16 ms
- 28-pin SOJ, ZIP, and TSOP plastic packaging

Pin Configurations

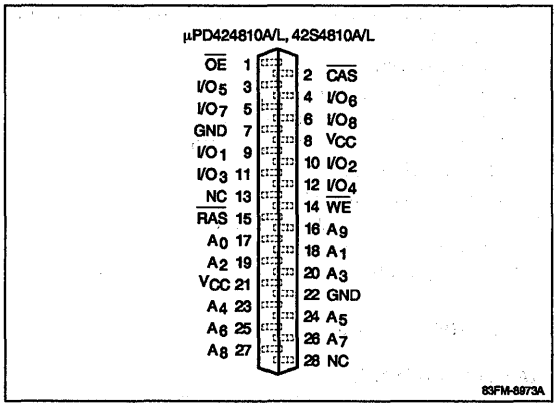
28-Pin Plastic SOJ



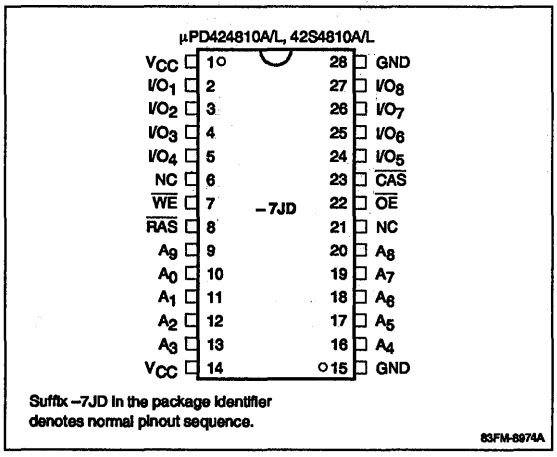
6b

Pin Configurations (cont)

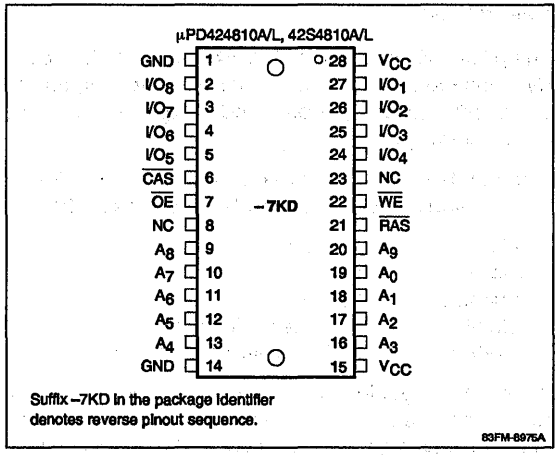
28-Pin Plastic ZIP



28-Pin Plastic TSOP (Normal Pinouts)



28-Pin Plastic TSOP (Reverse Pinouts)



Pin Identification

Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

Ordering Information, μPD424810A (+ 5-volt power)

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Package
μPD424810ALE-60	60 ns	40 ns	20 ns	28-pin plastic SOJ
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD424810AV-60	60 ns	40 ns	20 ns	28-pin plastic ZIP
V-70	70 ns	45 ns		
V-80	80 ns	50 ns		
μPD424810AG5-60	60 ns	40 ns	20 ns	28-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD424810AG5M-60	60 ns	40 ns	20 ns	28-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD424810L (+ 3.3-volt power)

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Package
μPD424810LLE-A60	60 ns	40 ns	20 ns	28-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD424810LV-A60	60 ns	40 ns	20 ns	28-pin plastic ZIP
V-A70	70 ns	45 ns		
V-A80	80 ns	50 ns		
μPD424810LG5-A60	60 ns	40 ns	20 ns	28-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD424810LG5M-A60	60 ns	40 ns	20 ns	28-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

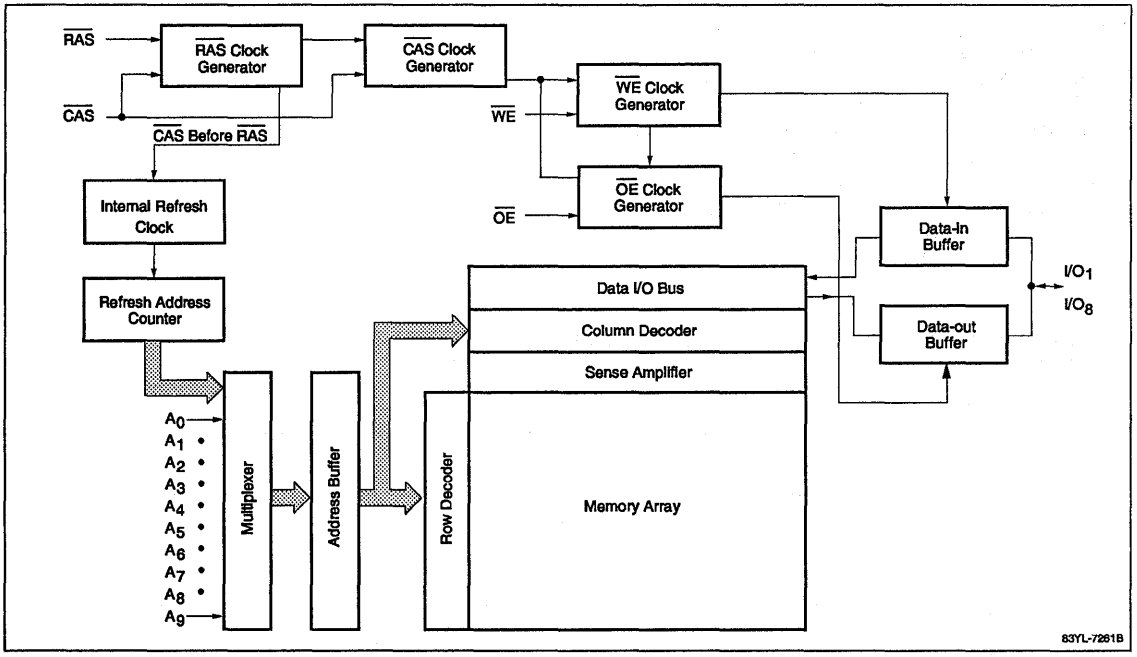
Ordering Information, μPD42S4810A (+ 5-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4810ALE-60	60 ns	40 ns	20 ns	300 μA	28-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4810AV-60	60 ns	40 ns	20 ns	300 μA	28-pin plastic ZIP
V-70	70 ns	45 ns			
V-80	80 ns	50 ns			
μPD42S4810AG5-60	60 ns	40 ns	20 ns	300 μA	28-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns			
G5-80	80 ns	50 ns			
μPD42S4810AG5M-60	60 ns	40 ns	20 ns	300 μA	28-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns			
G5M-80	80 ns	50 ns			

Ordering Information, μPD42S4810L (+ 3.3-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4810LLE-A60	60 ns	40 ns	20 ns	100 μA	28-pin plastic SOJ
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			
μPD42S4810LV-A60	60 ns	40 ns	20 ns	100 μA	28-pin plastic ZIP
V-A70	70 ns	45 ns			
V-A80	80 ns	50 ns			
μPD42S4810LG5-A60	60 ns	40 ns	20 ns	100 μA	28-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns			
G5-A80	80 ns	50 ns			
μPD42S4810LG5M-A60	60 ns	40 ns	20 ns	100 μA	28-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns			
G5M-A80	80 ns	50 ns			

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	I/O_1 - I/O_8
Standby	H	X	X	X	High-Z
Refresh cyle	L	H	X	X	High-Z
Read cycle	L	L	H	L	Data output
Write cycle	L	L	L	H	Data input
—	L	L	H	H	High-Z

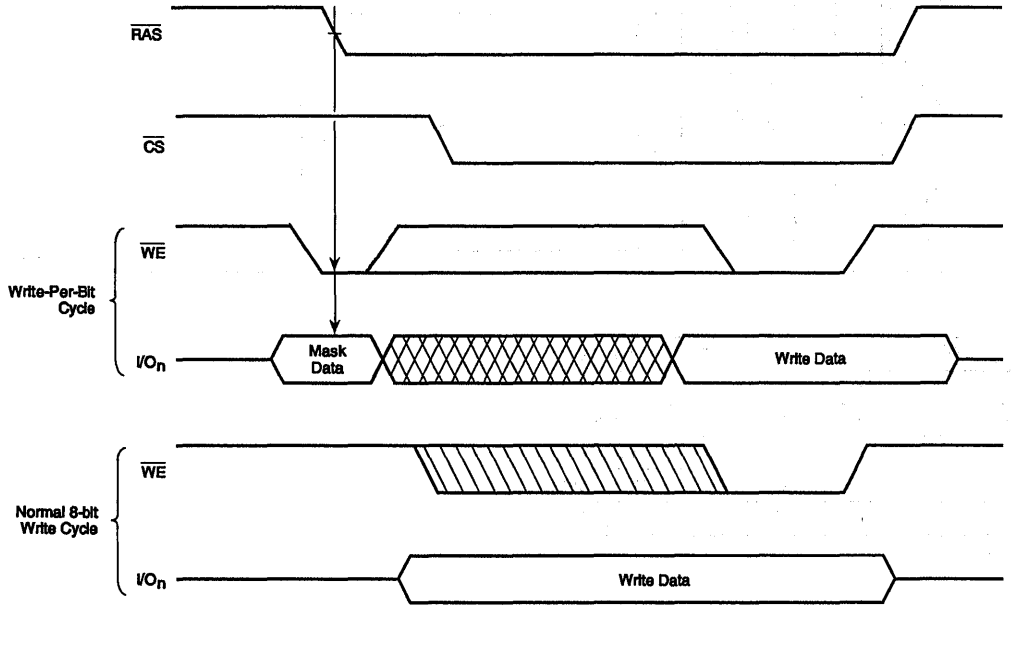
X = don't care.

6b

Write-Per-Bit Option

The write-per-bit option may be used to allow a write cycle to change any number of bits in the 16-bit word. The mask is loaded from the I/O lines at the falling edge of $\overline{RAS}$ if $\overline{WE}$ = V_{IL}. If the I/O line is high, then the corresponding bit will be written when the write cycle executes. If the I/O line is low, the bit does not change. A mask loaded during fast-page operation will remain set and active for each write cycle that executes while $\overline{RAS}$ remains low. The mask may be changed only at the falling edge of $\overline{RAS}$.

Comparison of Write-Per-Bit Cycle Versus Standard 8-Bit Write Cycle



I/O	Mask Data		Write Operation
I/O_1 ~ I/O_8	1	(High)	Write Bit
	0	(Low)	Disable Bit Write

83YL-86258

Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
5-volt devices	50 mA
3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_8

Recommended Operating Conditions

		5-Volt Devices			3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} +0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.5		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

Self-Refresh Current

T_A = 0 to +70°C; V_{CC} = +5 V ±10% (42S4810A) or +3.3 V ±0.3 V (42S4810L)

Symbol	42S4810A	42S4810L	Conditions
I_{CC7}	300 μA max	100 μA max	I/O pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. Other input pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. $t_{RAS} \geq 100$ μs

DC Characteristics; 5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				300	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

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DC Characteristics; 3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			500	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				100	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–5		5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–5		5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

AC Characteristics

T_A = 0 to +70°C

μPD424810A, 42S4810A: V_{CC} = +5.0 V ±10%

μPD424810L, 42S4810L: V_{CC} = +3.3 V ±0.3 V

		-60		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5)		100		90		80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
	I_{CC1} (+3.3)		100		80		70		
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5)		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
	I_{CC3} (+3.3)		100		80		70		
Operating current, fast-page cycle, average	I_{CC4} (+5)		80		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
	I_{CC4} (+3.3)		80		70		60		
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5)		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
	I_{CC5} (+3.3)		100		80		70		
Access time from column address	t_{AA}		30		35		40	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		ns	(Note 15)
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	–35		–40		–50		ns	For 42S4810A/L only

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	(Notes 4, 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		75		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		50		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		20		20		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	(Note 9)
Output disable from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t_{PC}	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with exended data output	t_{PRWC}	85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		10		ns	

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		μs	For 42S4810A/L
Random read or write cycle time	t_{RC}	120		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	120		130		150		ns	For 42S4810A/L
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Read-modify-write cycle time	t_{RWC}	165		175		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Rise and fall times	t_T	3	50	3	50	3	50	ns	(Note 4)
Write-per-bit mode hold time	t_{WBH}	10		10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		0		ns	
Write command hold time	t_{WCH}	15		15		15		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		ns	(Note 14)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Write-per-bit mask data hold time	t_{WH}	10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		ns	(Note 12)
Write-per-bit mask data setup time	t_{WS}	0		0		0		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF. For 3.3-volt devices, V_{OH} = 2.0 V and V_{OL} = 0.8 V.

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max).
If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of one of the $\overline{CAS}$ signals for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

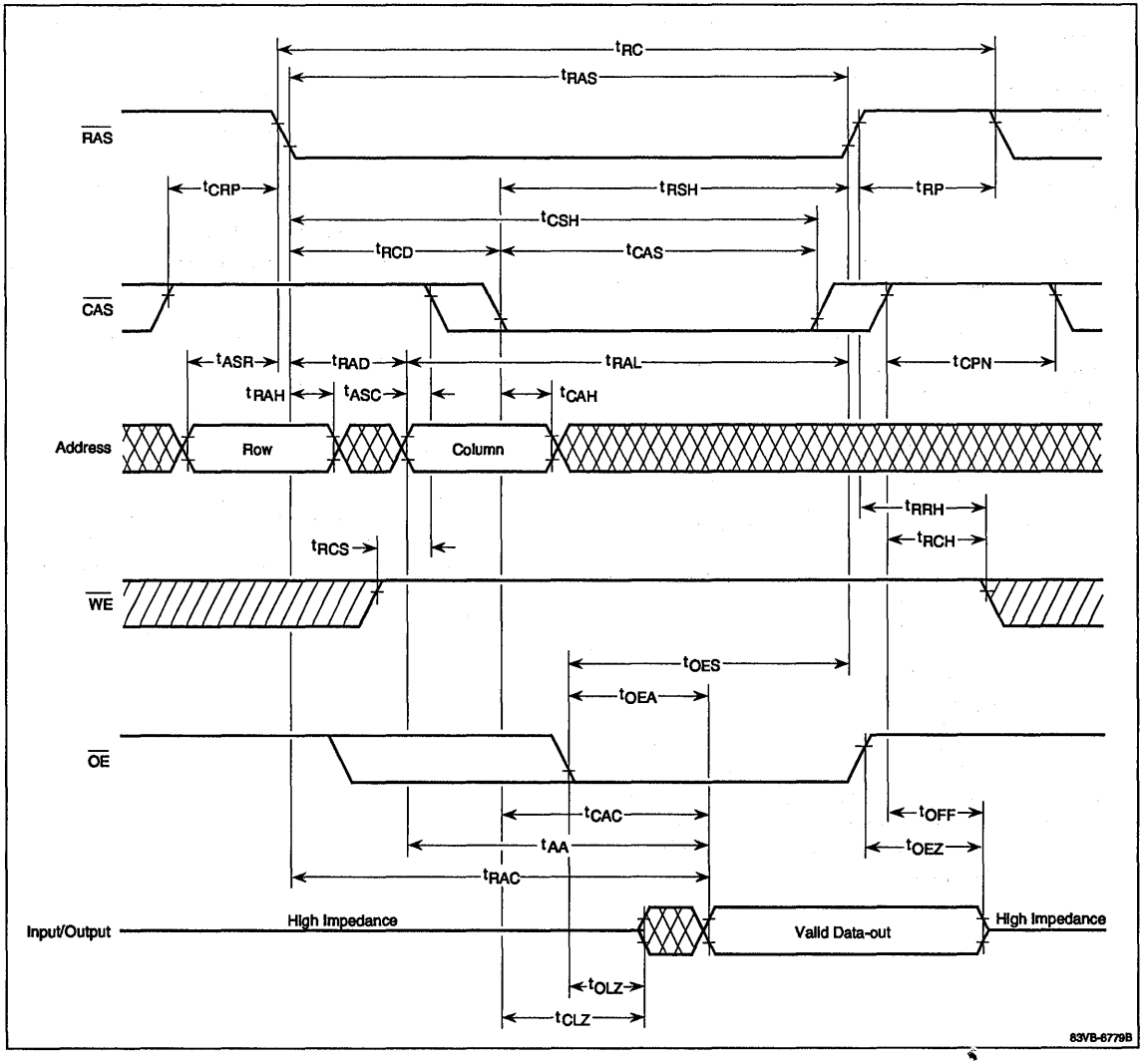
(14) t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD} and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) Holding $\overline{CAS}$ low prior to $\overline{RAS}$ going negative will initiate a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (t_{CSR} and t_{CHR} must be satisfied).

6b

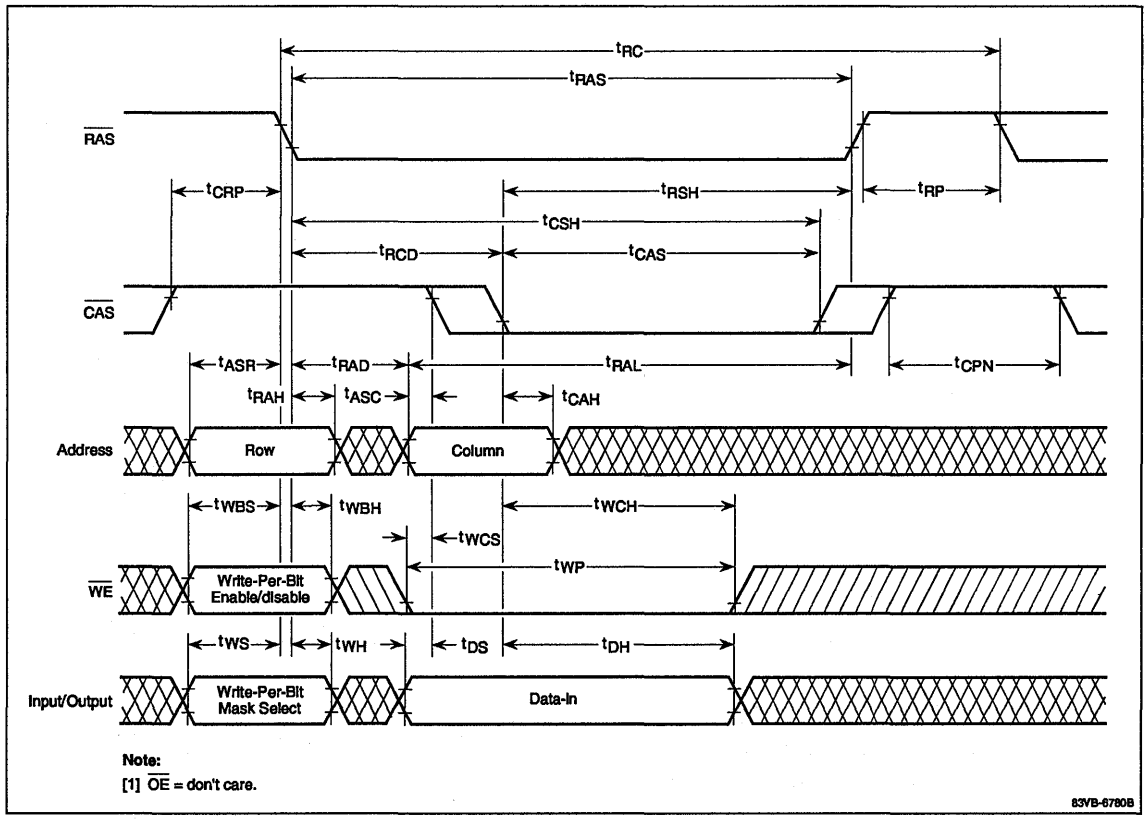
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

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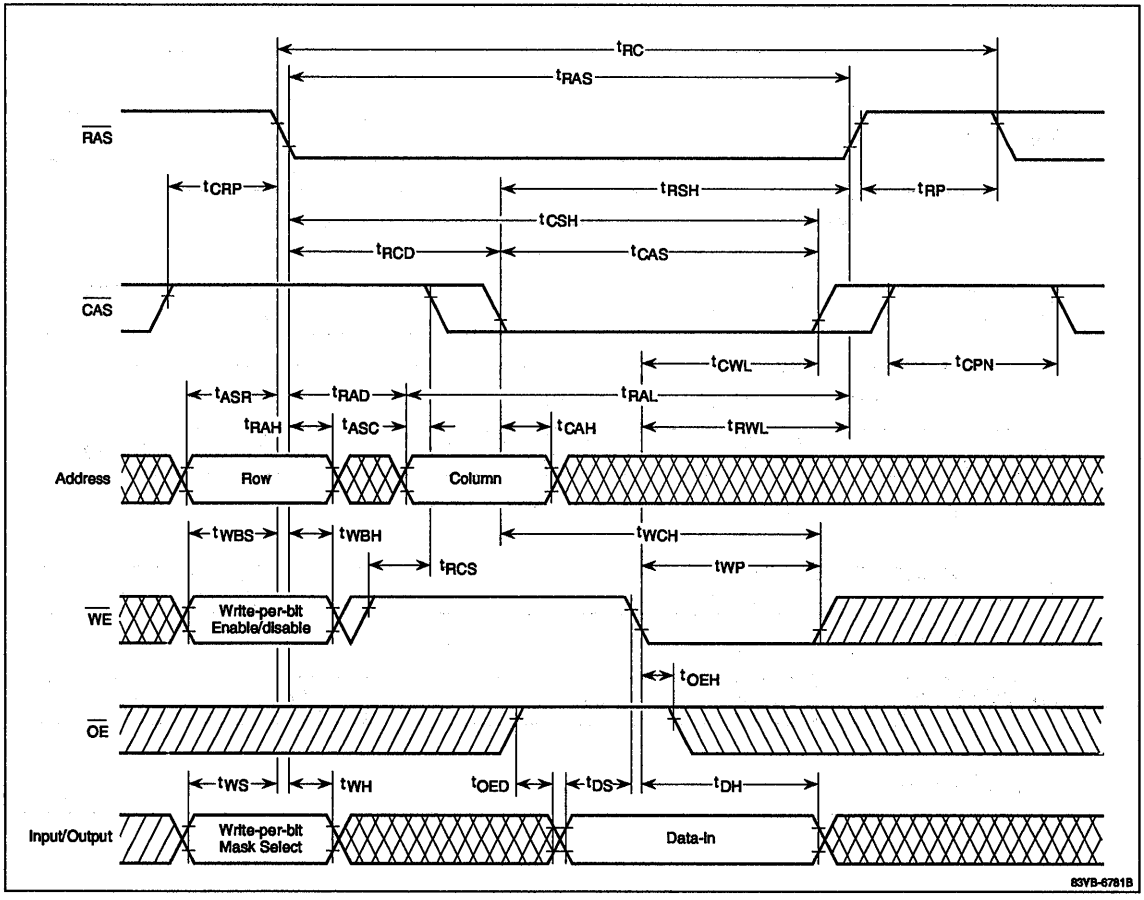
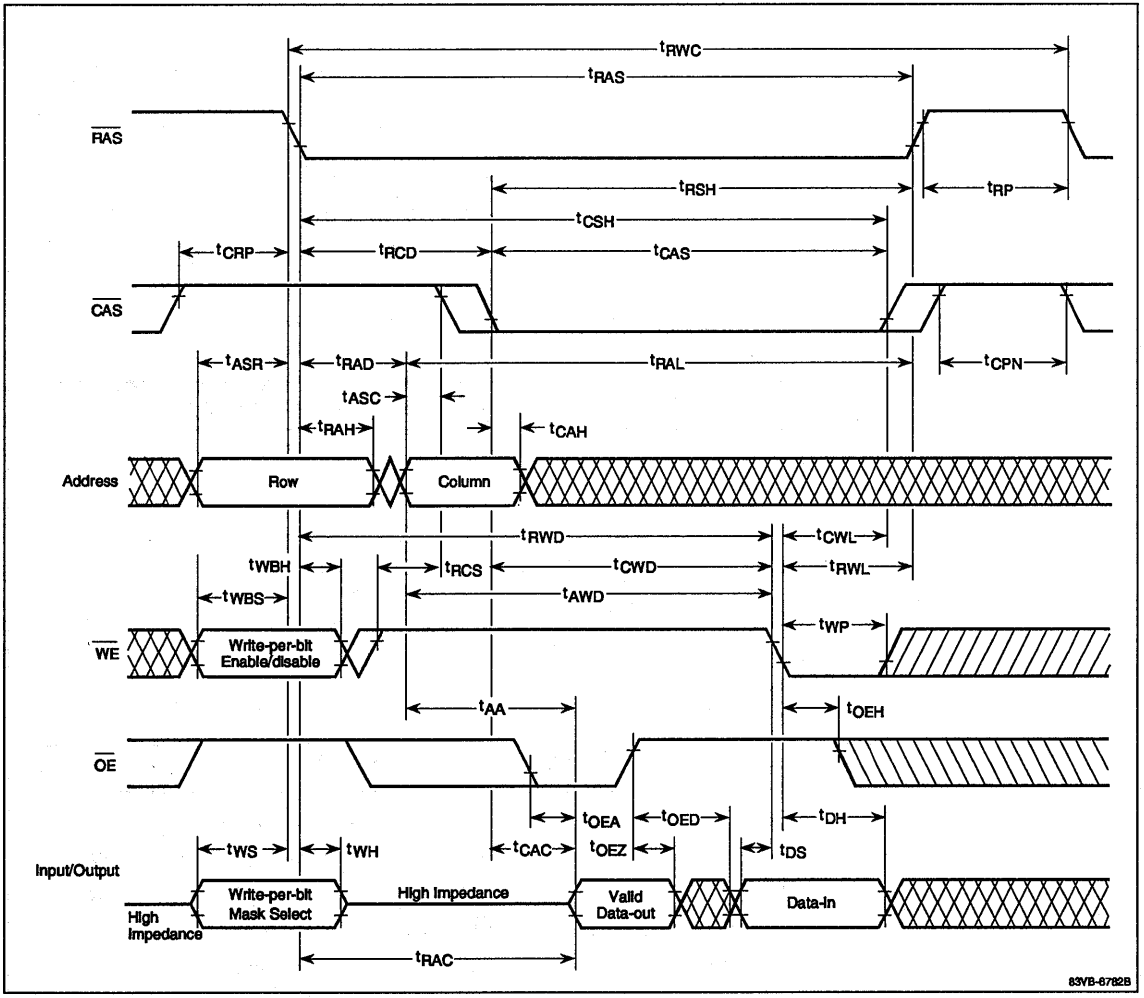
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

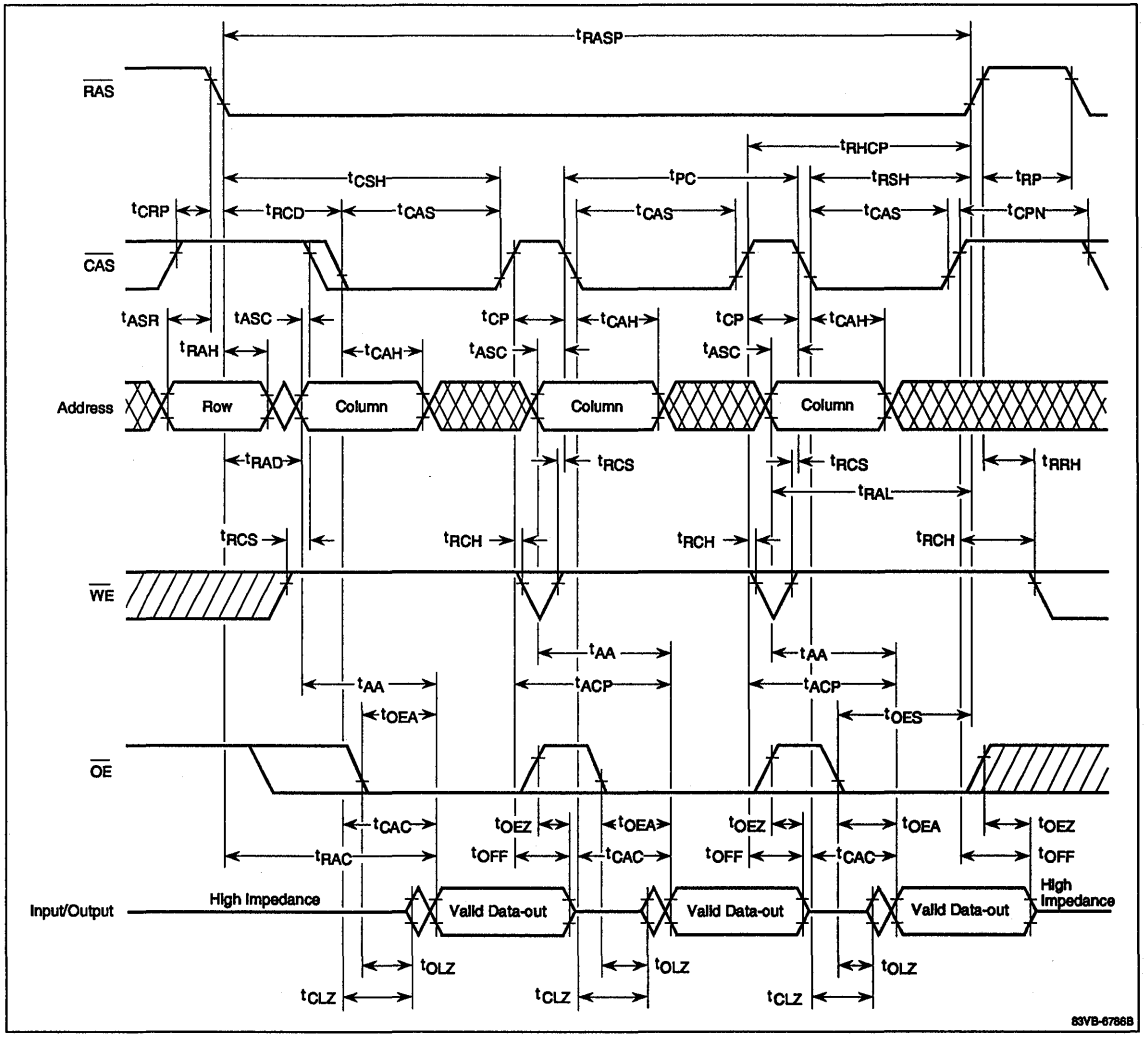
Read-Write/Read-Modify-Write Cycle



6b

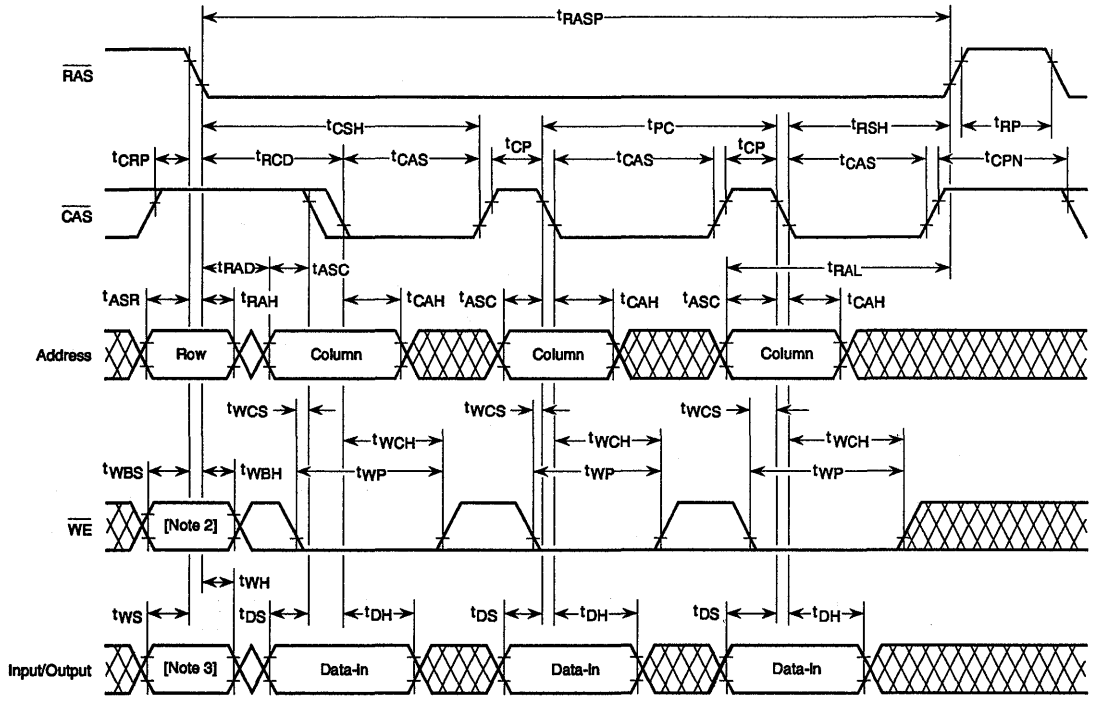
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



Notes:

[1] $\overline{OE}$ = don't care.

[2] Write-per-bit enable/disable.

[3] Write-per-bit mask select.

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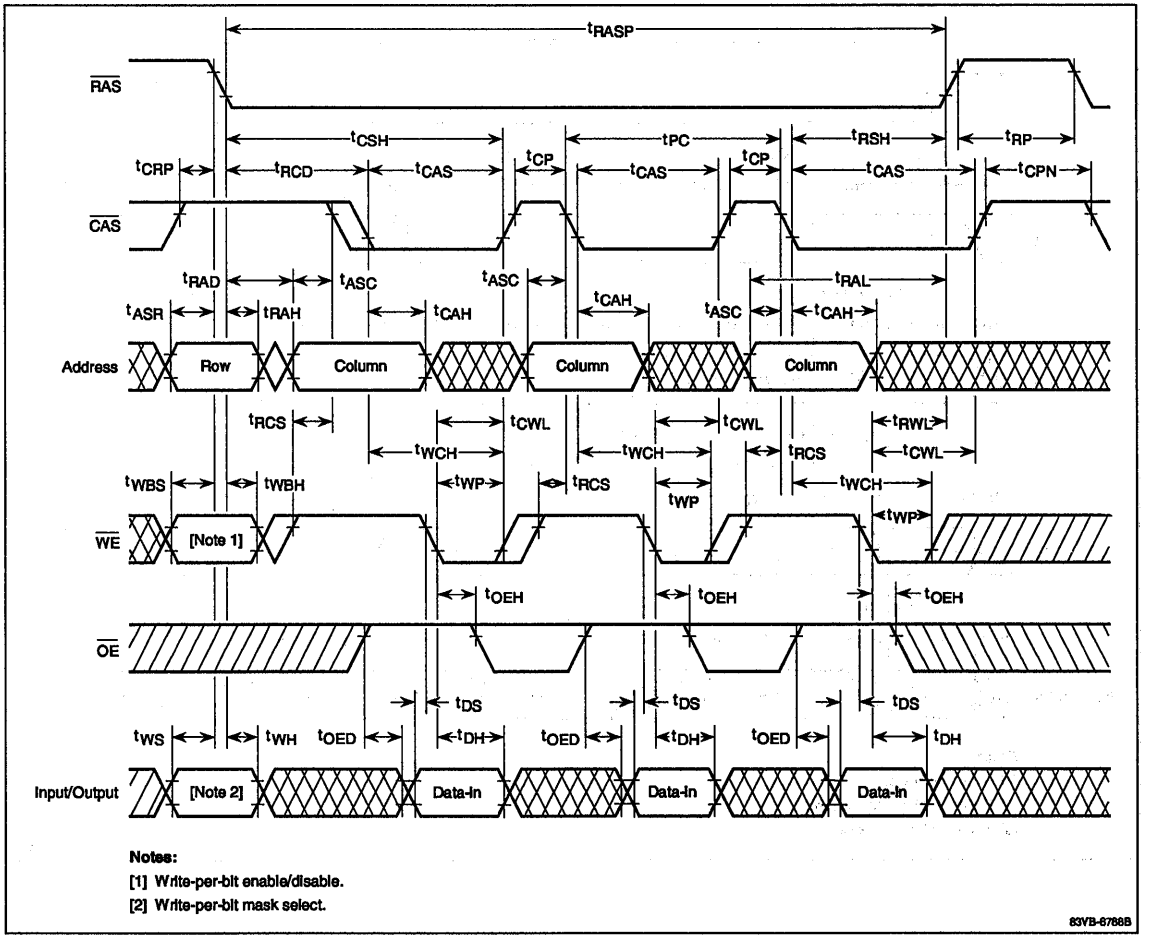
Timing Waveforms (cont)

Fast-Page Late Write Cycle



Notes:

[1] Write-per-bit enable/disable.

[2] Write-per-bit mask select.

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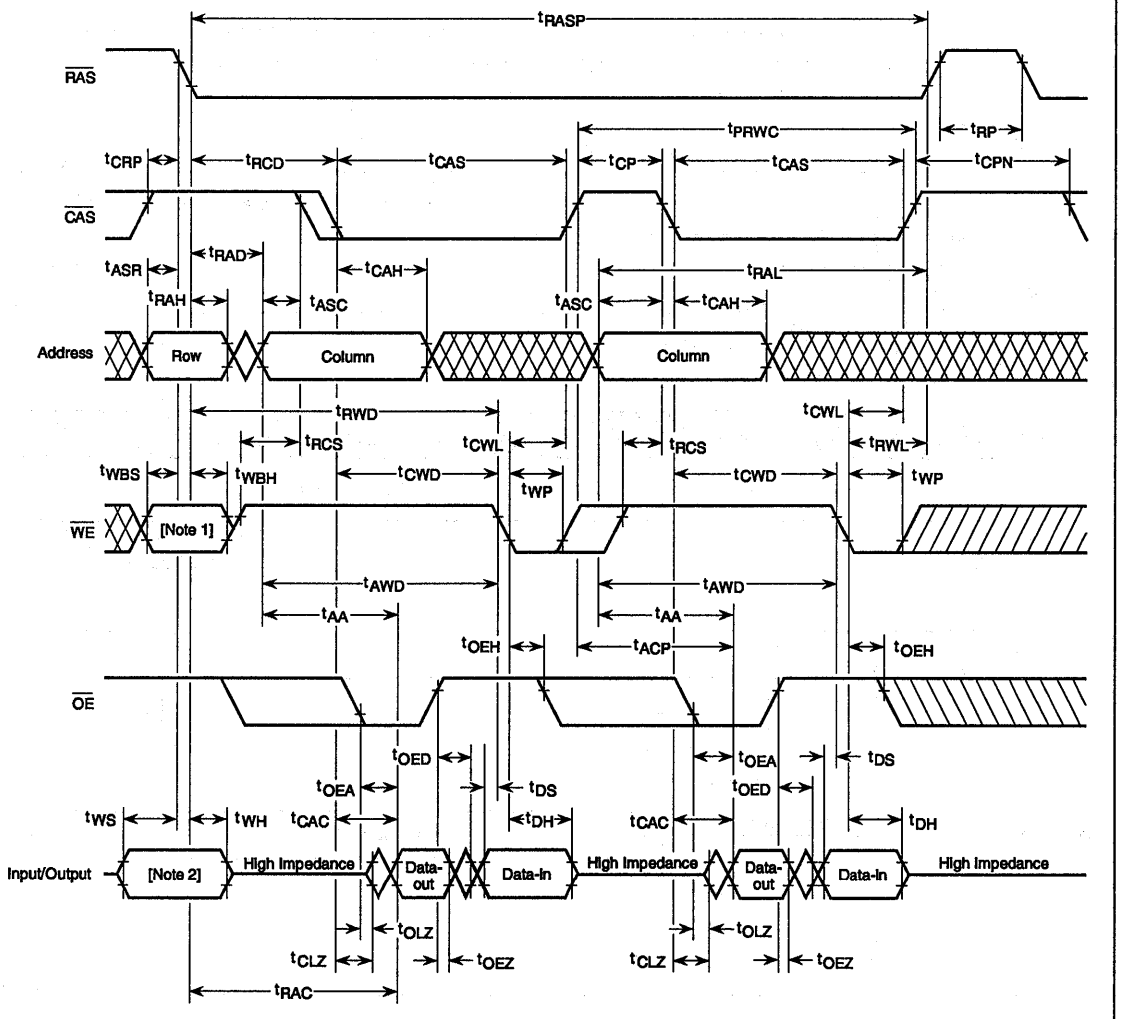
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



Notes:
[1] Write-per-bit enable/disable.
[2] Write-per-bit mask select.

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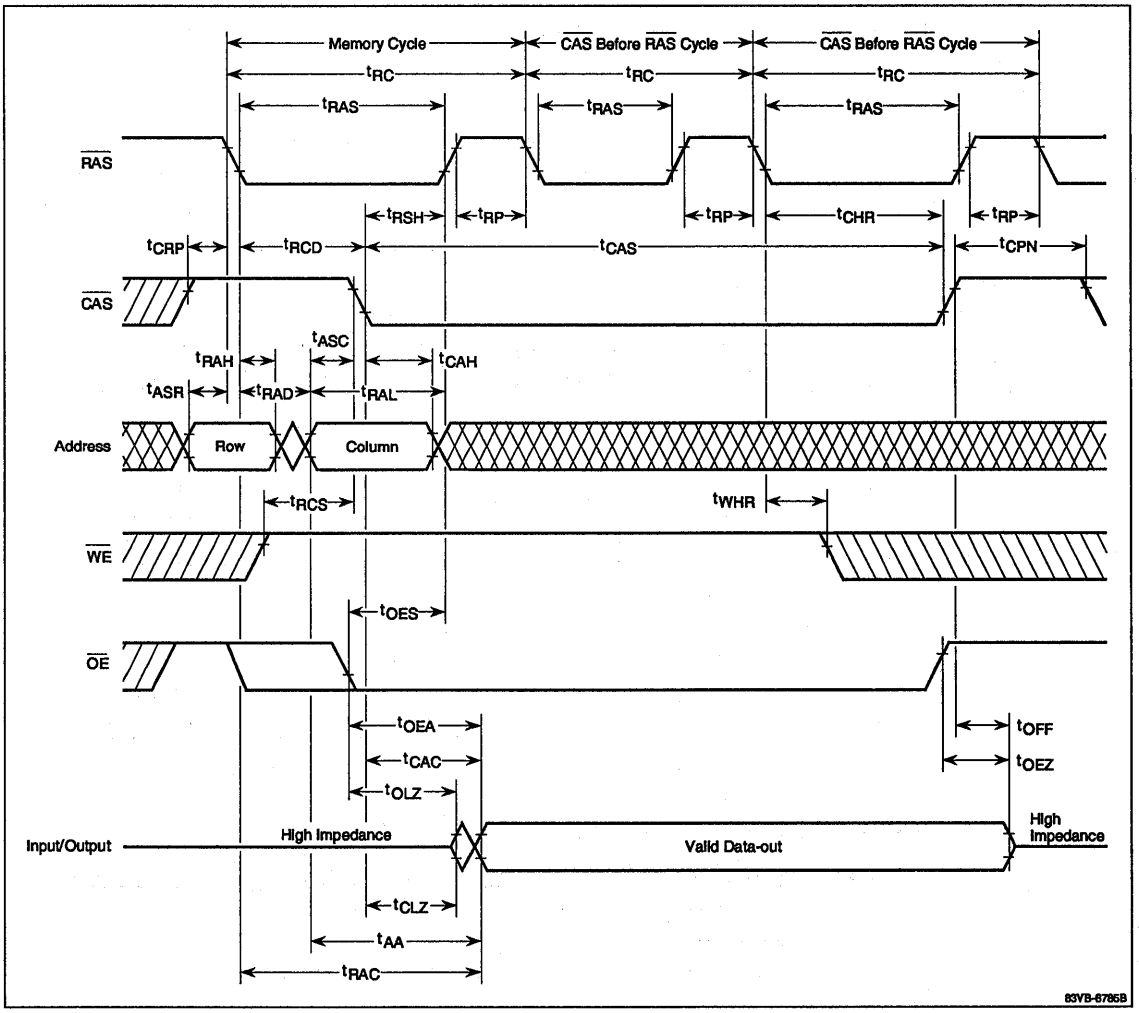
6b

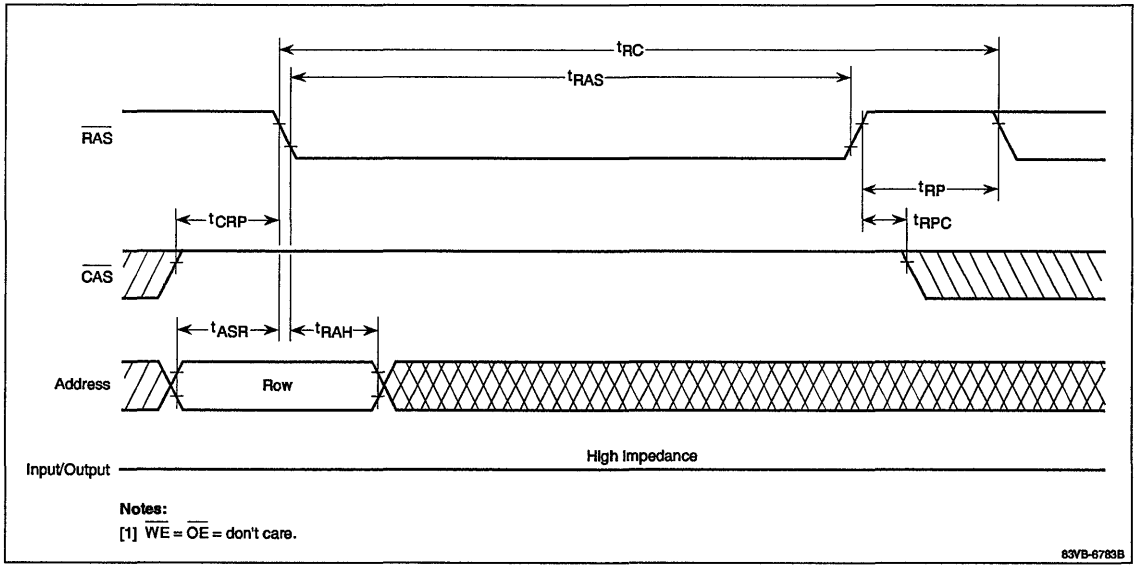
Timing Waveforms (cont)

Hidden Refresh Cycle

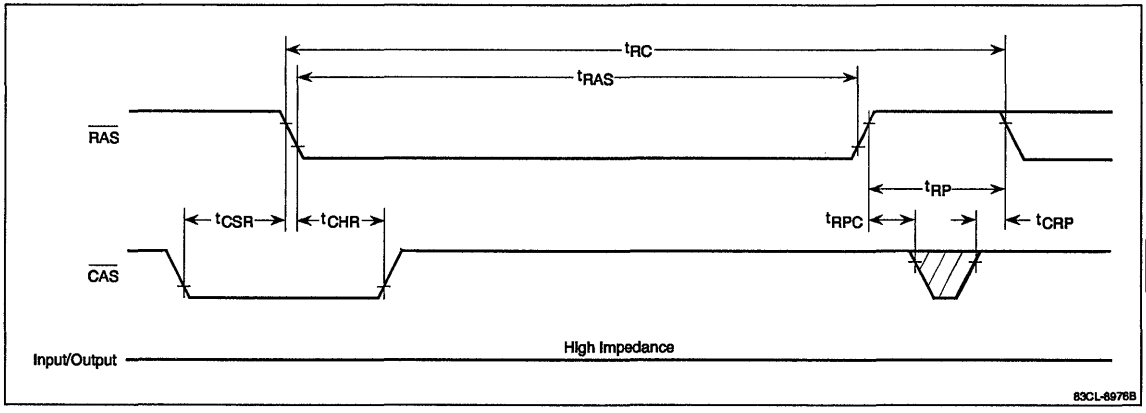


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



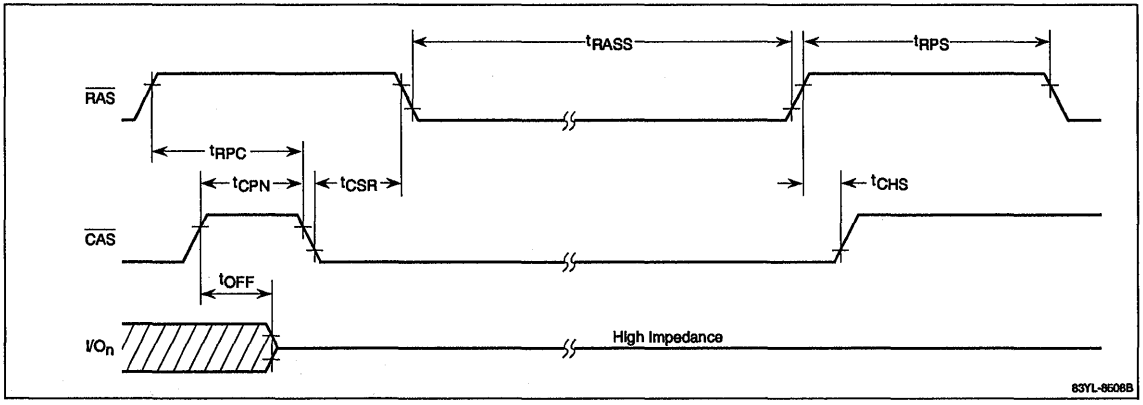
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



6b

Timing Waveforms (cont)

CBR Self-Refresh Cycle



μPD424900A/L, 42S4900A/L
524,288 x 9-Bit
Dynamic CMOS RAM

Description

The μPD424900A/L and μPD42S4900A/L are fast-page dynamic RAMs organized as 524,288 words by 9 bits and designed to operate from a single power supply.

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
424900A	+5 V
424900L	+3.3 V
42S4900A	+5 V; self-refresh mode
42S4900L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh address. $\overline{RAS}$-only refresh cycles will also refresh all memory locations.

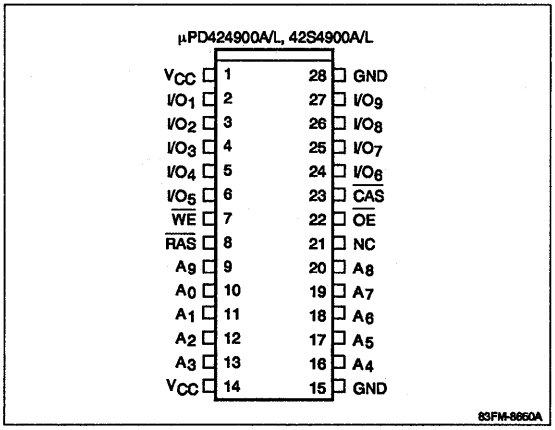
The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

- 524,288 by 9-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 1024 refresh cycles every 16 ms
- 28-pin SOJ, 28-pin ZIP, and 28-pin TSOP plastic packaging

Pin Configurations

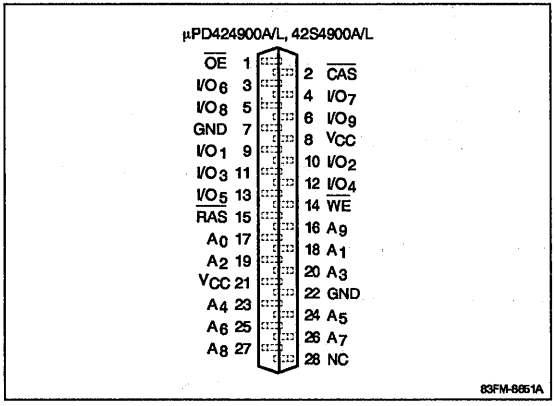
28-Pin Plastic SOJ



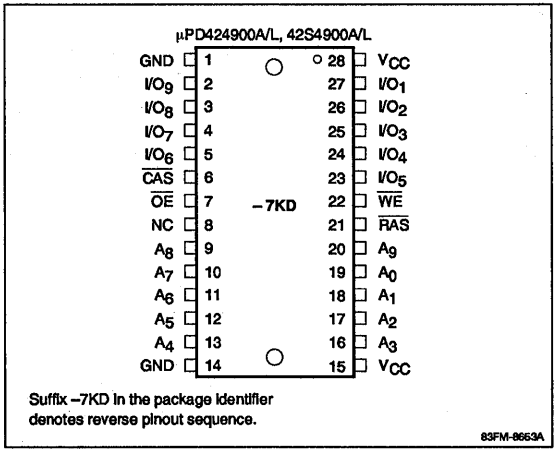
6c

Pin Configurations (cont)

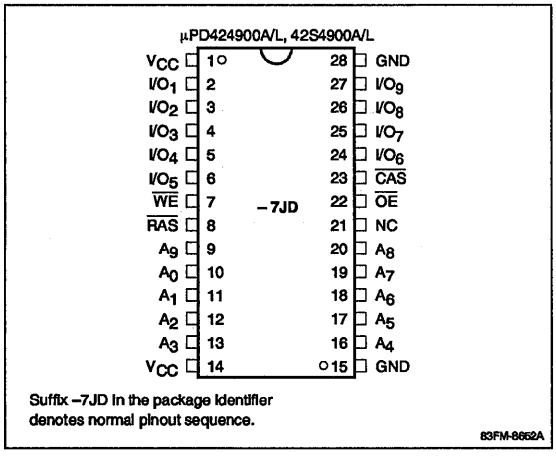
28-Pin Plastic ZIP



28-Pin Plastic TSOP (Reverse Pinouts)



28-Pin Plastic TSOP (Normal Pinouts)



Pin Identification

Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_9	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Ordering Information, μPD424900A (+ 5-volt power)

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Package
μPD424900ALE-60	60 ns	40 ns	20 ns	28-pin plastic SOJ
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD424900AV-60	60 ns	40 ns	20 ns	28-pin plastic ZIP
V-70	70 ns	45 ns		
V-80	80 ns	50 ns		
μPD424900AG5-60	60 ns	40 ns	20 ns	28-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD424900AG5M-60	60 ns	40 ns	20 ns	28-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD424900L (+ 3.3-volt power)

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Package
μPD424900LLE-A60	60 ns	40 ns	20 ns	28-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD424900LV-A60	60 ns	40 ns	20 ns	28-pin plastic ZIP
V-A70	70 ns	45 ns		
V-A80	80 ns	50 ns		
μPD424900LG5-A60	60 ns	40 ns	20 ns	28-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD424900LG5M-A60	60 ns	40 ns	20 ns	28-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

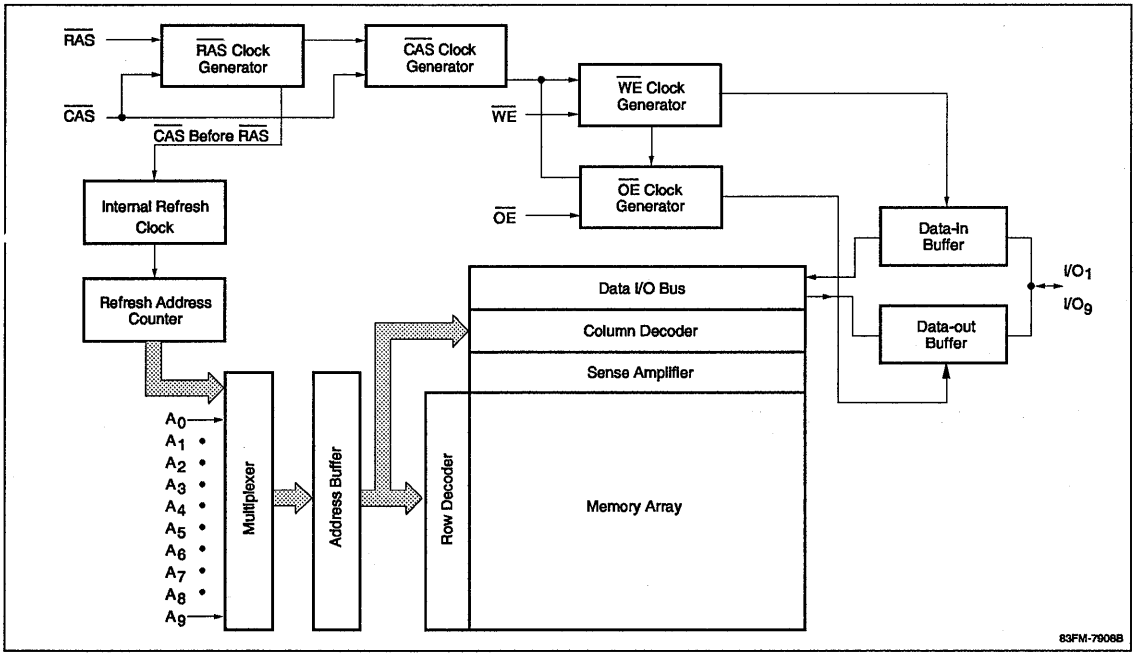
Ordering Information, μPD42S4900A (+ 5-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4900ALE-60	60 ns	40 ns	20 ns	300 μA	28-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4900AV-60	60 ns	40 ns	20 ns	300 μA	28-pin plastic ZIP
V-70	70 ns	45 ns			
V-80	80 ns	50 ns			
μPD42S4900AG5-60	60 ns	40 ns	20 ns	300 μA	28-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns			
G5-80	80 ns	50 ns			
μPD42S4900AG5M-60	60 ns	40 ns	20 ns	300 μA	28-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns			
G5M-80	80 ns	50 ns			

Ordering Information, μPD42S4900L (+ 3.3-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4900LLE-A60	60 ns	40 ns	20 ns	100 μA	28-pin plastic SOJ
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			
μPD42S4900LV-A60	60 ns	40 ns	20 ns	100 μA	28-pin plastic ZIP
V-A70	70 ns	45 ns			
V-A80	80 ns	50 ns			
μPD42S4900LG5-A60	60 ns	40 ns	20 ns	100 μA	28-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns			
G5-A80	80 ns	50 ns			
μPD42S4900LG5M-A60	60 ns	40 ns	20 ns	100 μA	28-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns			
G5M-A80	80 ns	50 ns			

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	I/O_1 - I/O_9
Standby	H	X	X	X	High-Z
Refresh cycle	L	H	X	X	High-Z
Read cycle	L	L	H	L	Data output
Write cycle	L	L	L	H	Data input
——	L	L	H	H	High-Z

X = don't care.

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Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
5-volt devices	50 mA
3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_9

Recommended Operating Conditions

		5-Volt Devices			3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} +0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.5		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

Self-Refresh Current

T_A = 0 to +70°C; V_{CC} = +5 V ±10% (42S4900A) or +3.3 V ±0.3 V (42S4900L)

Symbol	42S4900A	42S4900L	Conditions
I_{CC7}	300 μA max	100 μA max	I/O pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. Other input pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. $t_{RAS} \geq 100$ μs

DC Characteristics; 5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$ (min); I_O = 0 mA
				300	μA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

DC Characteristics; 3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			500	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				100	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–5		5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–5		5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

AC Characteristics

T_A = 0 to +70°C

μPD424900A, 42S4900A: V_{CC} = +5.0 V ±10%

μPD424900L, 42S4900L: V_{CC} = +3.3 V ±0.3 V

		-60		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5)		120		110		100	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
	I_{CC1} (+3.3)		110		100		90		
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5)		120		110		100	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
	I_{CC3} (+3.3)		110		100		90		
Operating current, fast-page cycle, average	I_{CC4} (+5)		100		90		80	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
	I_{CC4} (+3.3)		100		90		80		
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5)		120		110		100	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
	I_{CC5} (+3.3)		110		100		90		
Access time from column address	t_{AA}		30		35		40	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		ns	(Note 15)

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	−35		−40		−50		ns	For 42S4900A/L only
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	(Notes 4, 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		75		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		50		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		20		20		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	(Note 9)
Output disable from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t_{PC}	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with exended data output	t_{PRWC}	85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 3, 4, 7, 8)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		10		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		μs	For 42S4900A/L
Random read or write cycle time	t_{RC}	120		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	120		130		150		ns	For 42S4900A/L
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Read-modify-write cycle time	t_{RWC}	165		175		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Rise and fall times	t_T	3	50	3	50	3	50	ns	(Note 4)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Write command hold time	t_{WCH}	15		15		15		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		ns	(Note 14)
Write command pulse width	t_{WP}	15		15		15		ns	(Note 12)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF. For 3.3-volt devices, V_{OH} = 2.0 V and V_{OL} = 0.8 V.

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max).
If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

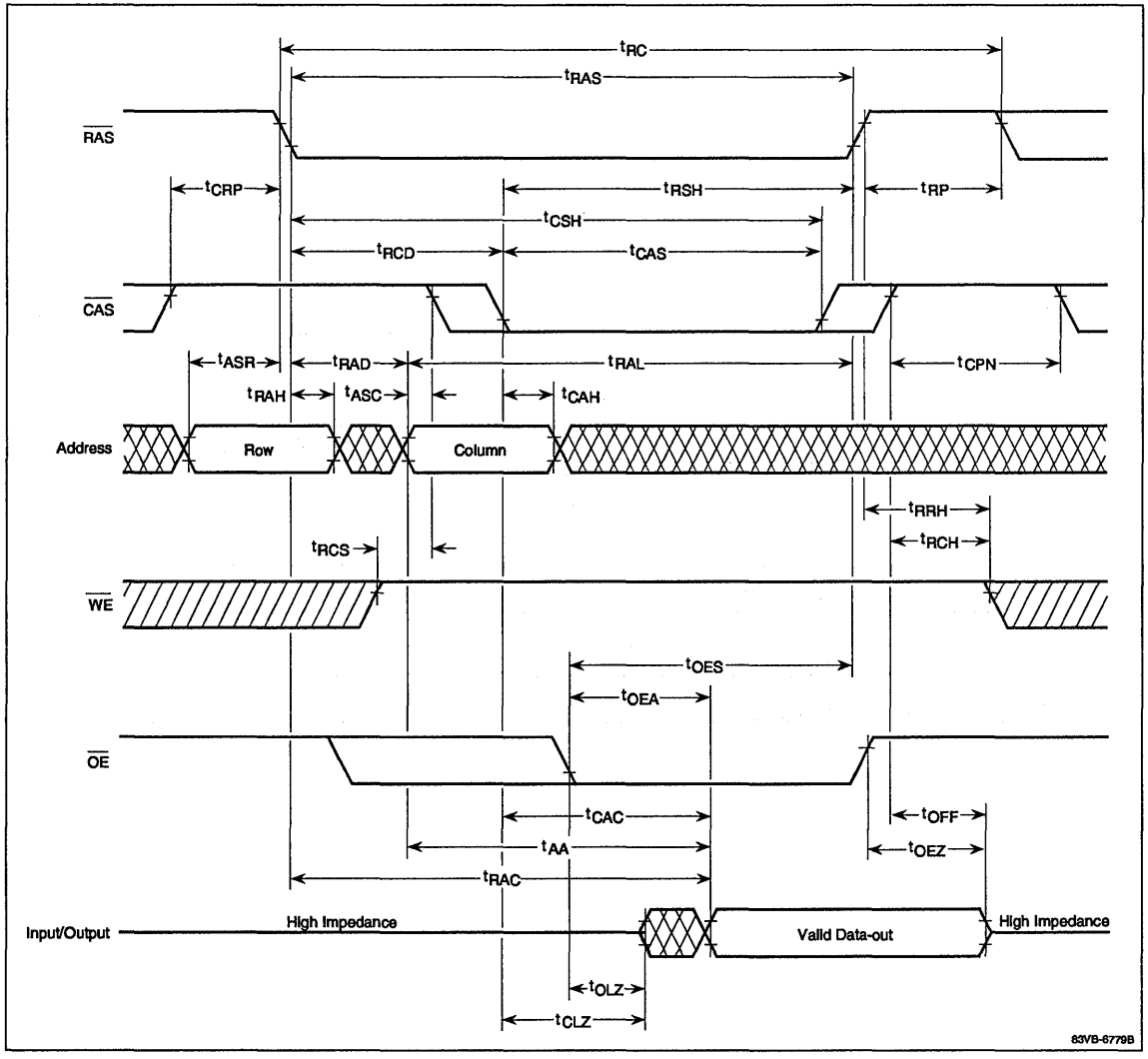
(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD} and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) Holding $\overline{CAS}$ low prior to $\overline{RAS}$ going negative will initiate a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (t_{CSR} and t_{CHR} must be satisfied).

Timing Waveforms

Read Cycle



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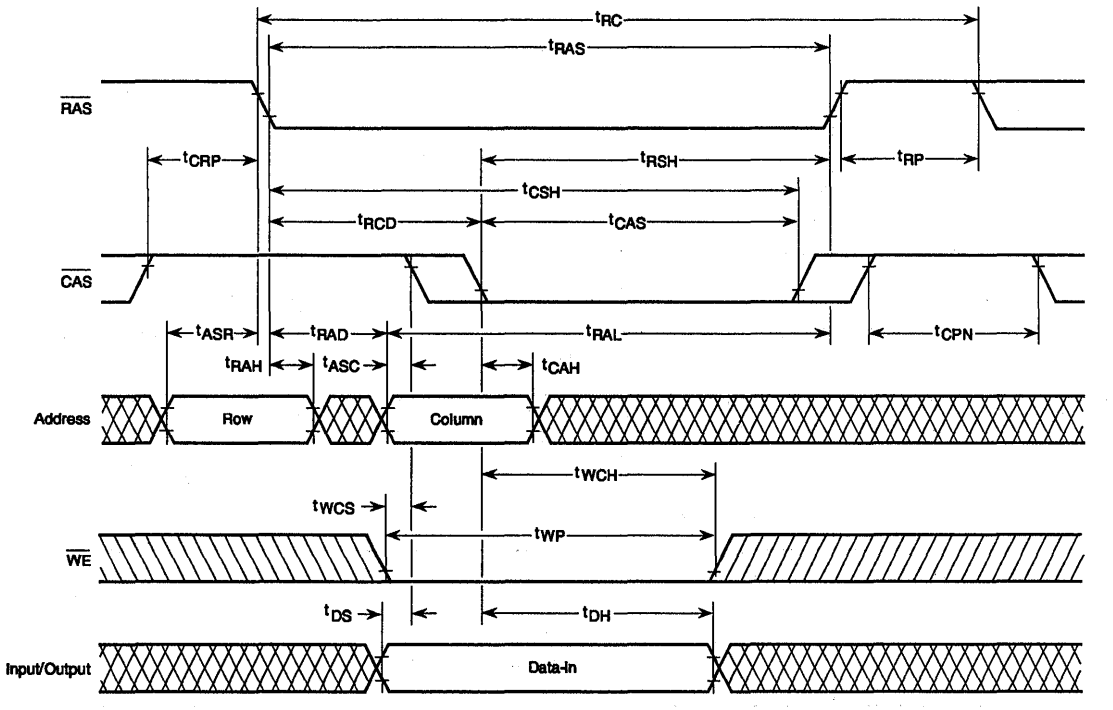
Timing Waveforms (cont)

Early-Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

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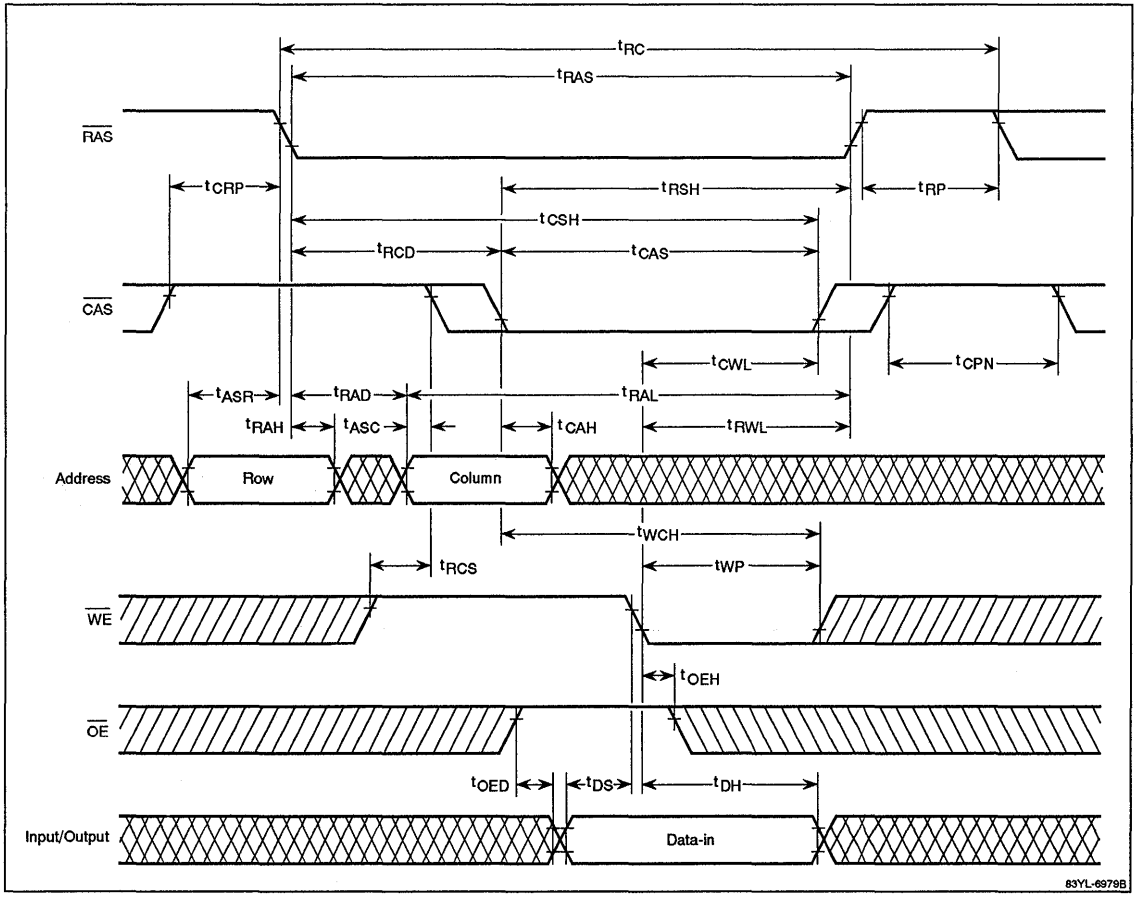
Timing Waveforms (cont)

Late-Write Cycle



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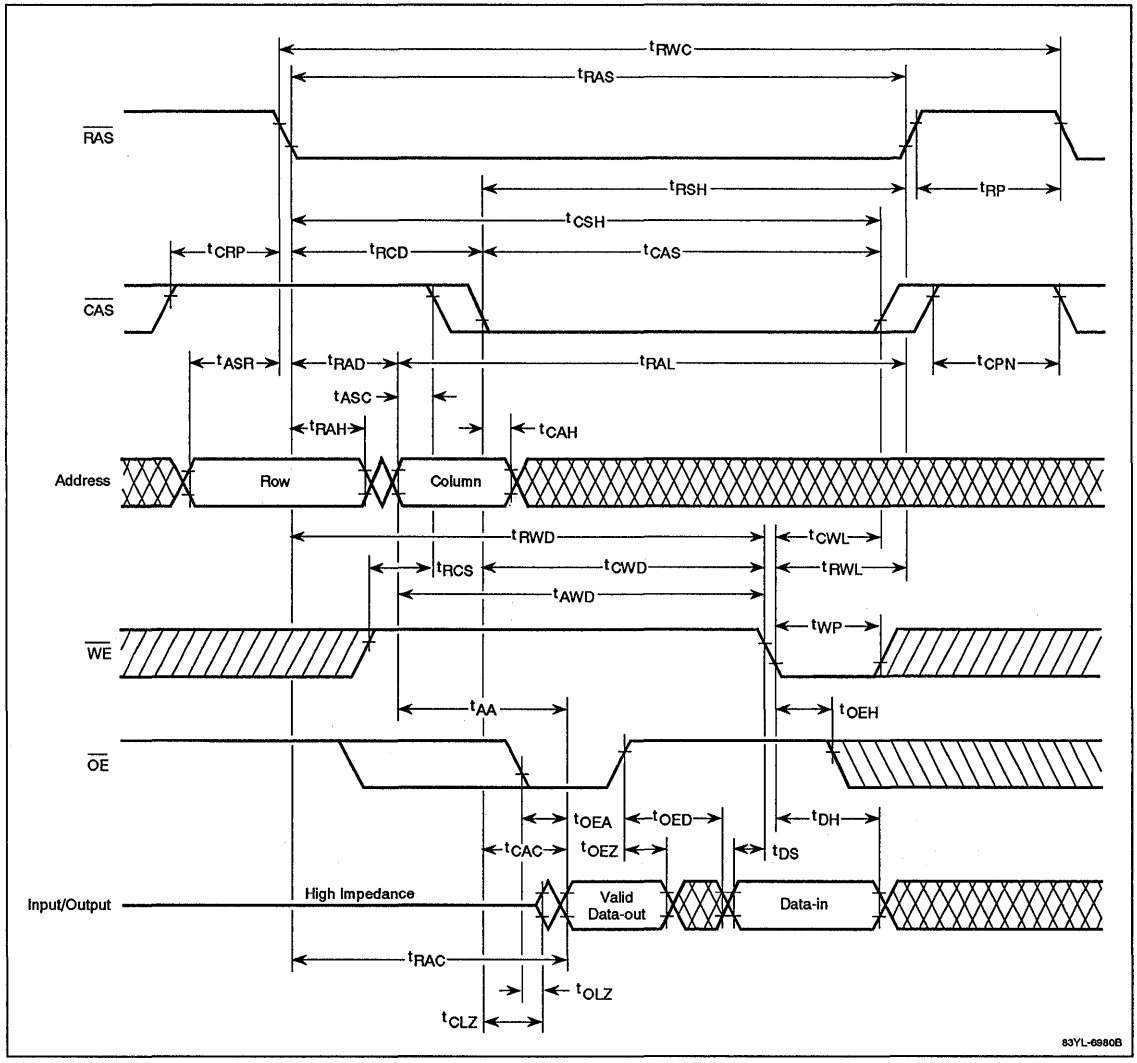
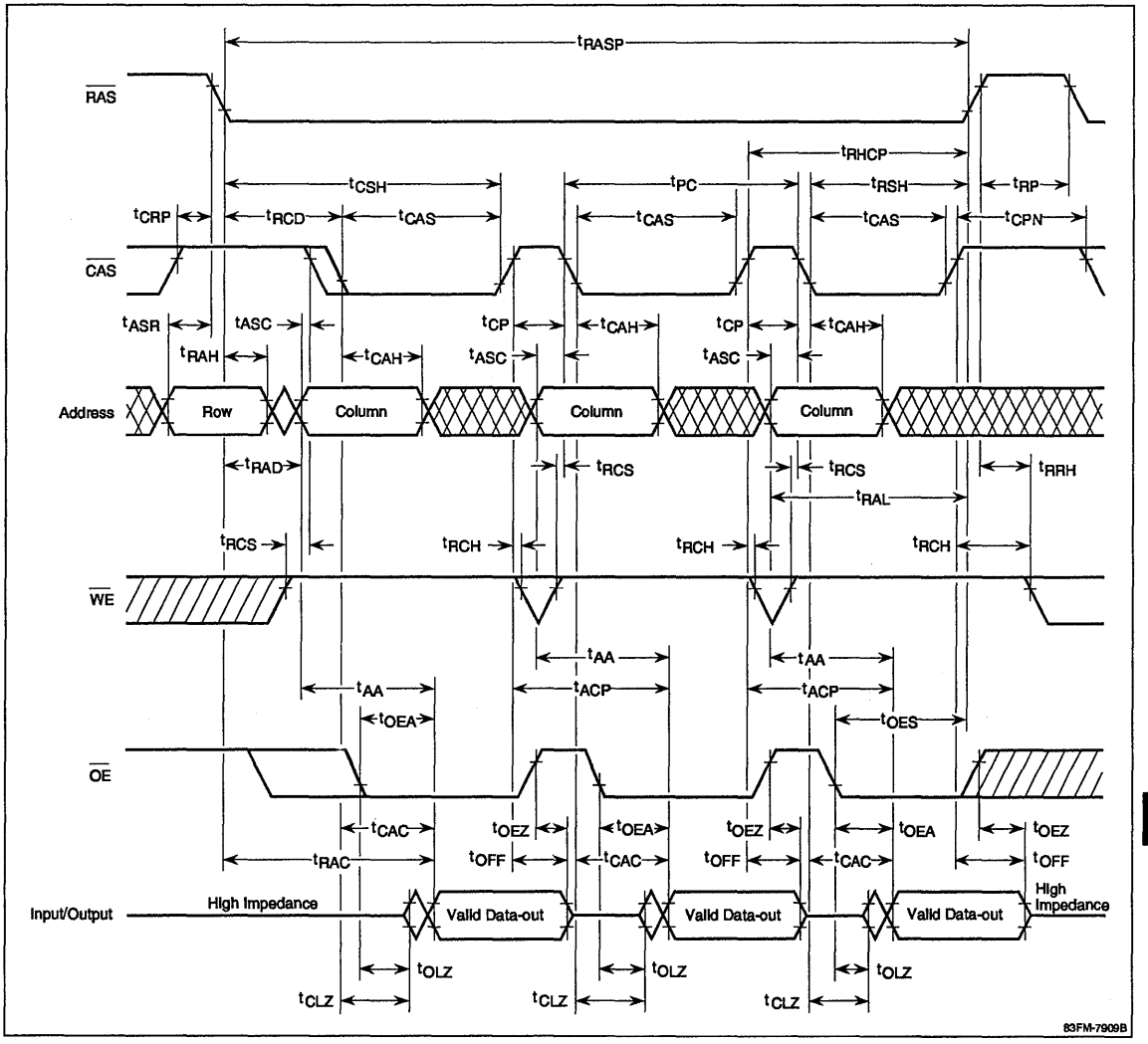
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Fast-Page Read Cycle



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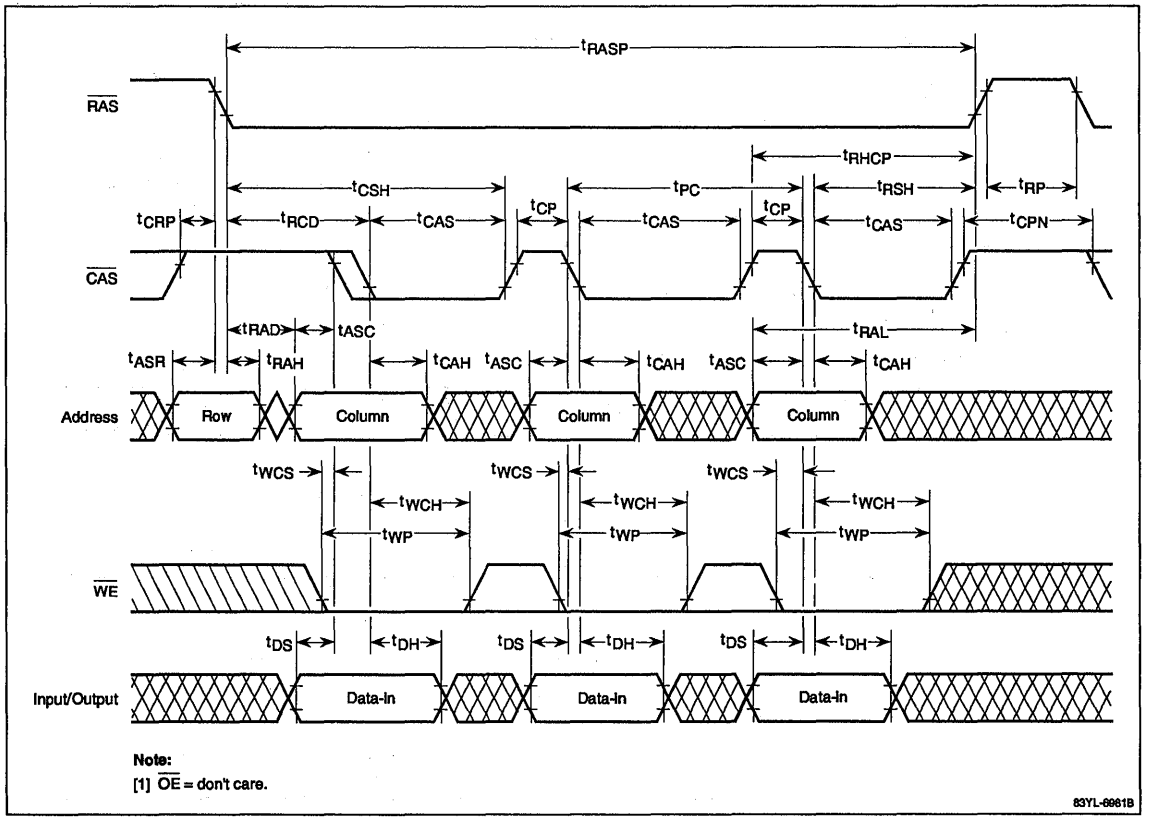
Timing Waveforms (cont)

Fast-Page Early-Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

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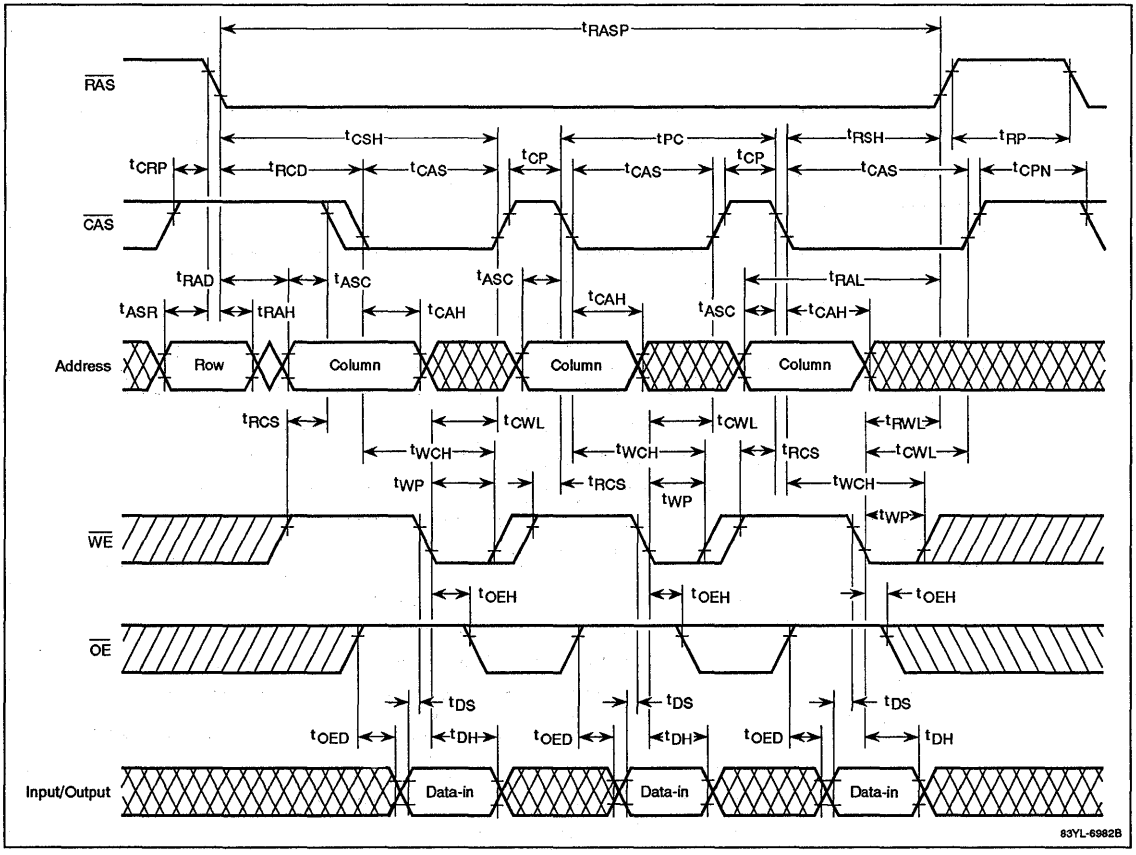
Timing Waveforms (cont)

Fast-Page Late-Write Cycle



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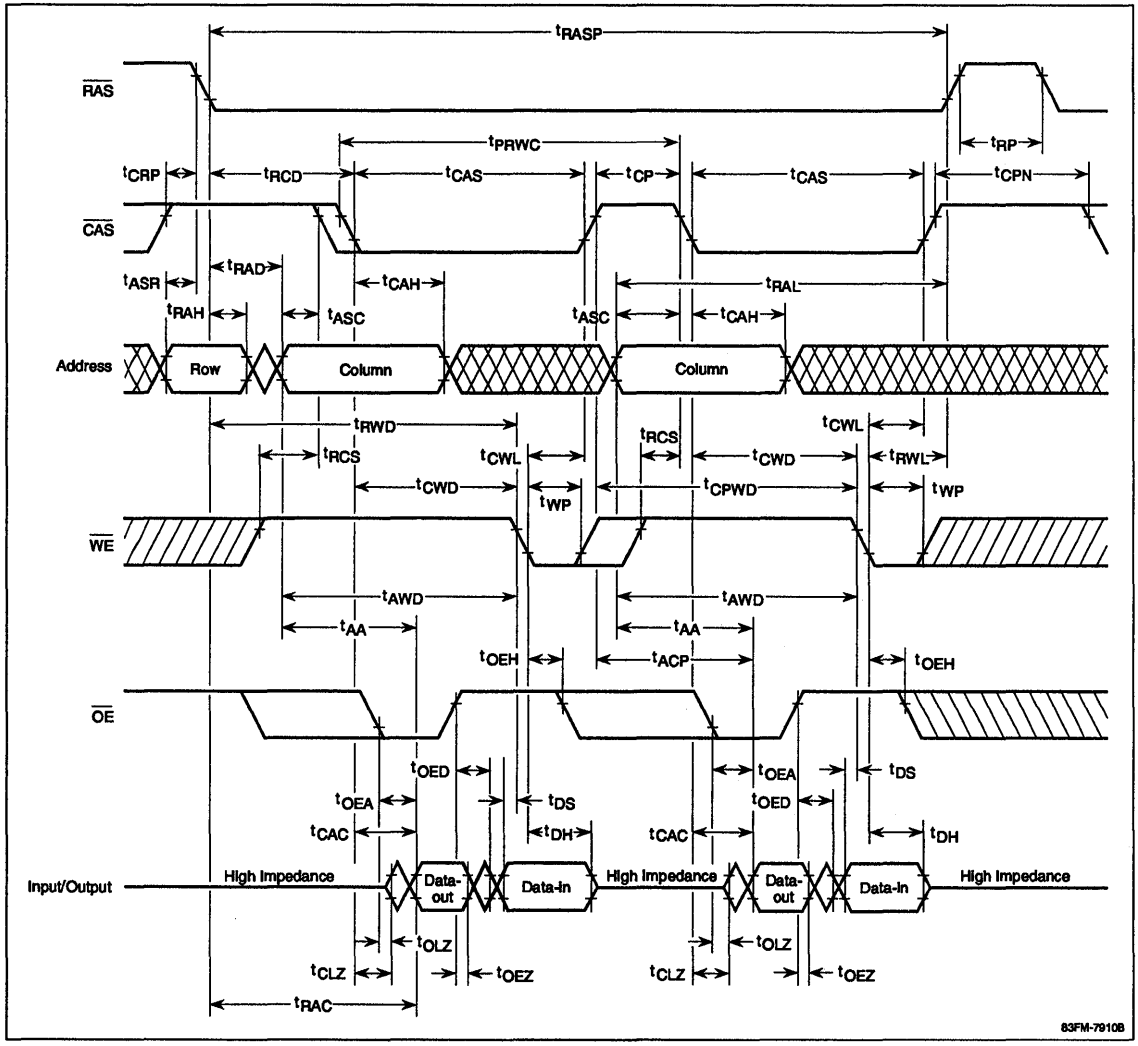
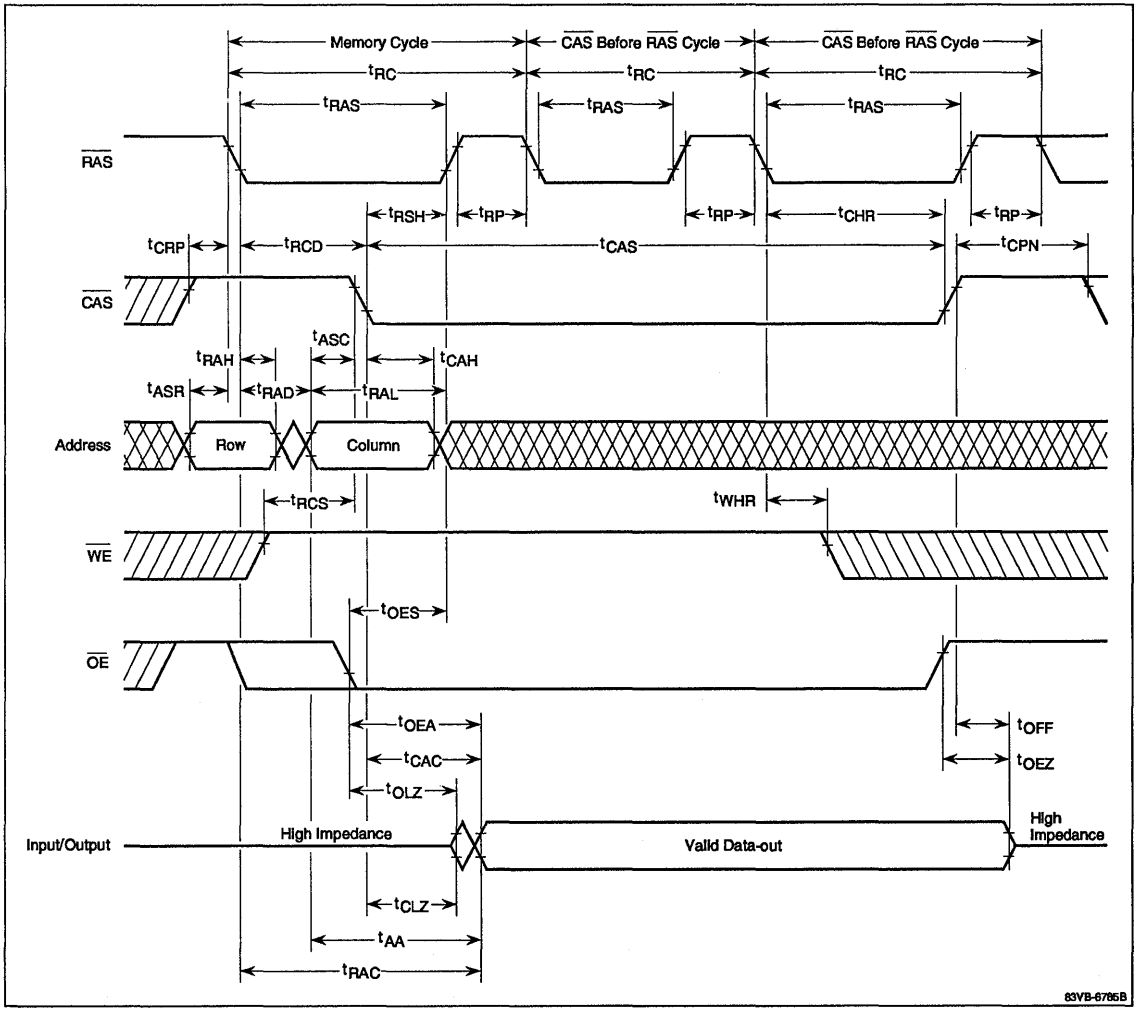
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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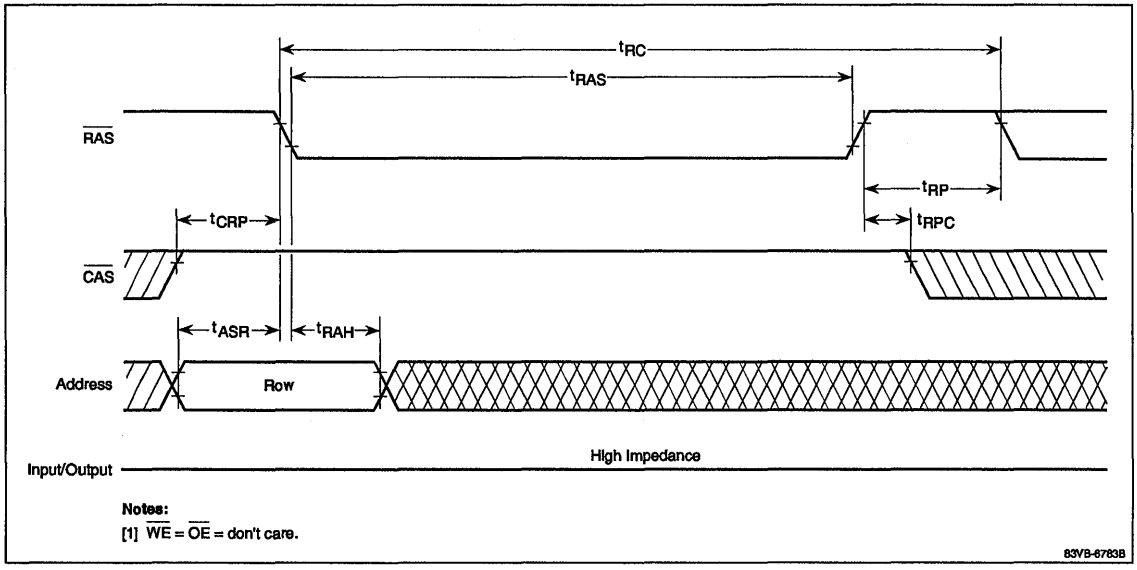
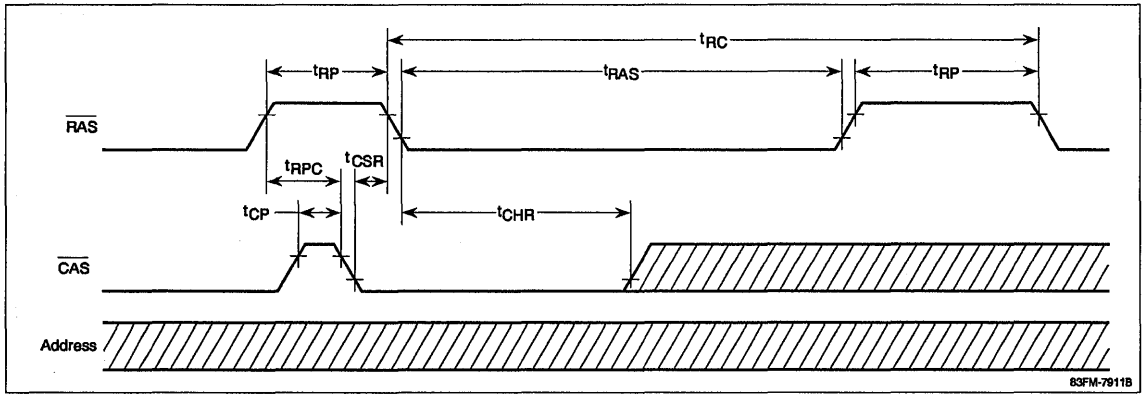
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle

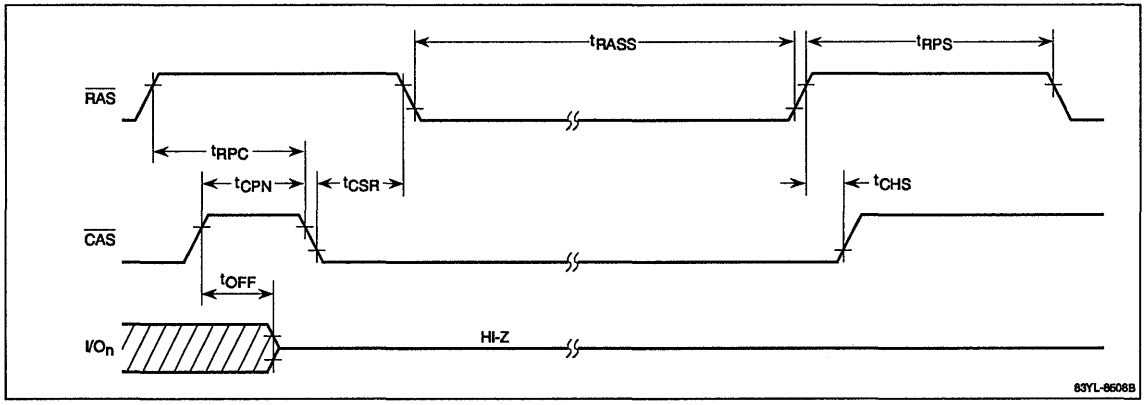


$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms

CBR Self-Refresh Cycle



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NEC

Section 7
4M DRAMs (256K x 16/18)

μPD	Organization	Features	
424170A	256K x 16	Fast-page; 2 $\overline{WE}$; 1K refresh	7a
424170L	256K x 16	Fast-page; 2 $\overline{WE}$; 1K refresh; 3.3-volt	
42S4170A	256K x 16	Fast-page; 2 $\overline{WE}$; 1K refresh; self-refresh	
42S4170L	256K x 16	Fast-page; 2 $\overline{WE}$; 1K refresh; self-refresh; 3.3-volt	
424190A	256K x 18	Fast-page; 2 $\overline{WE}$; 1K refresh	7b
424190L	256K x 18	Fast-page; 2 $\overline{WE}$; 1K refresh; 3.3-volt	
42S4190A	256K x 18	Fast-page; 2 $\overline{WE}$; 1K refresh; self-refresh	
42S4190L	256K x 18	Fast-page; 2 $\overline{WE}$; 1K refresh; self-refresh; 3.3-volt	
424260A	256K x 16	Fast-page; 2 $\overline{CAS}$; 512 refresh	7c
424260L	256K x 16	Fast-page; 2 $\overline{CAS}$; 512 refresh; 3.3-volt	
42S4260A	256K x 16	Fast-page; 2 $\overline{CAS}$; 512 refresh; self-refresh	
42S4260L	256K x 16	Fast-page; 2 $\overline{CAS}$; 512 refresh; self-refresh; 3.3-volt	

μPD	Organization	Features	
424263A	256K x 16	Fast-page; 2 $\overline{CAS}$; 512 refresh; write-per-bit	7d
424263L	256K x 16	Fast-page; 2 $\overline{CAS}$; 512 refresh; write-per-bit; 3.3-volt	
42S4263A	256K x 16	Fast-page; 2 $\overline{CAS}$; 512 refresh; write-per-bit; self- refresh	
42S4263L	256K x 16	Fast-page; 2 $\overline{CAS}$; 512 refresh; write-per-bit; self- refresh; 3.3-volt	
424280A	256K x 18	Fast-page; 2 $\overline{CAS}$; 512 refresh	7e
424280L	256K x 18	Fast-page; 2 $\overline{CAS}$; 512 refresh; 3.3-volt	
42S4280A	256K x 18	Fast-page; 2 $\overline{CAS}$; 512 refresh; self-refresh	
42S4280L	256K x 18	Fast-page; 2 $\overline{CAS}$; 512 refresh; self-refresh; 3.3-volt	

μPD424170A/L, 42S4170A/L
262,144 x 16-Bit
Dynamic CMOS RAM

Description

The μPD424170A/L and μPD42S4170A/L are fast-page dynamic RAMs organized as 262,144 words by 16 bits and designed to operate from a single power supply.

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
424170A	+5 V
424170L	+3.3 V
42S4170A	+5 V; self-refresh mode
42S4170L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

Word writing (I/O_1 - I/O_{16}), upper byte writing (I/O_9 - I/O_{16}), and lower byte writing (I/O_1 - I/O_8) are all possible using $\overline{UWE}$ and $\overline{LWE}$. If $\overline{UWE}$ or $\overline{LWE}$ goes low during an early write cycle, all data outputs remain in high impedance. Either going low causes a byte write cycle, while bringing both low at the same time results in a word write cycle. $\overline{UWE}$ and $\overline{LWE}$ cannot be staggered within the same write cycle.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh address. $\overline{RAS}$-only refresh cycles will also refresh all memory locations.

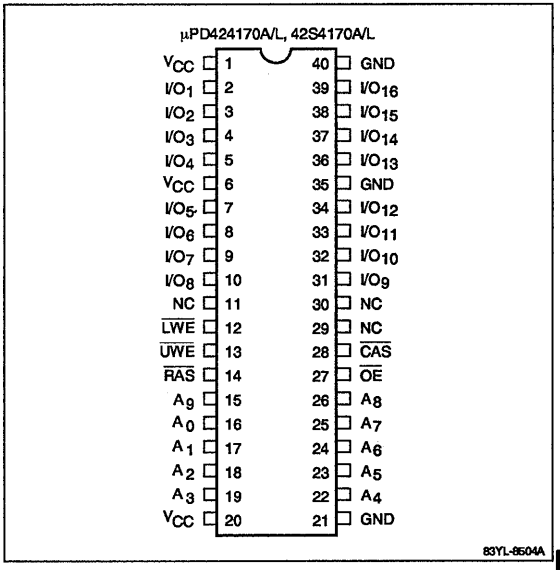
The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

- 262,144 by 16-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option
- Byte write control with $\overline{UWE}$ and $\overline{LWE}$
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 1024 refresh cycles every 16 ms
- 40-pin SOJ, 40-pin ZIP, and 44/40-pin TSOP plastic packaging

Pin Configurations

40-Pin Plastic SOJ



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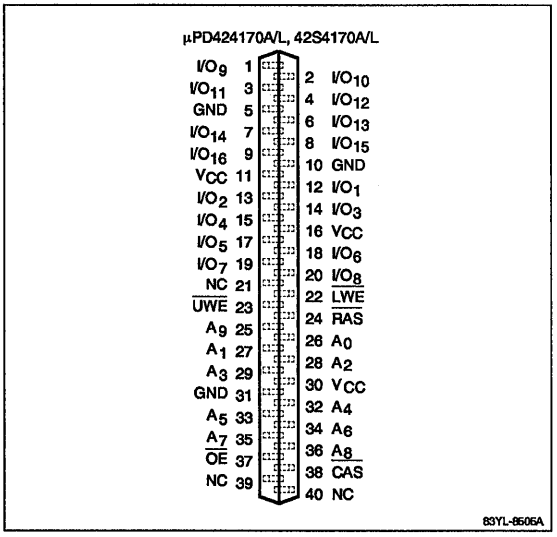
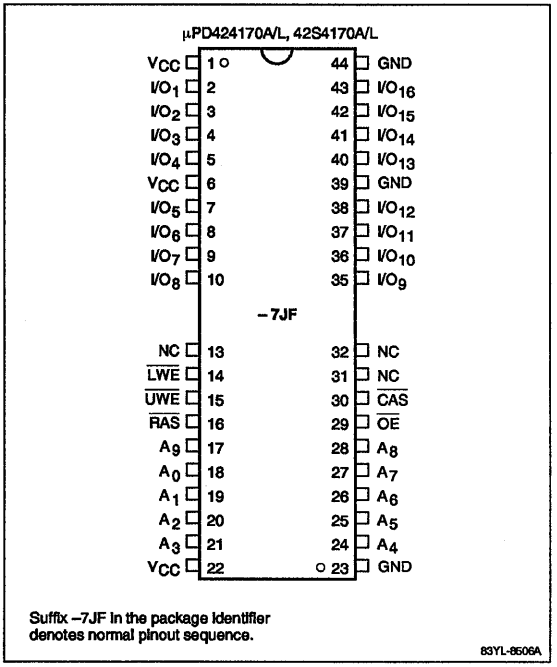
Pin Configurations (cont)

40-Pin Plastic ZIP

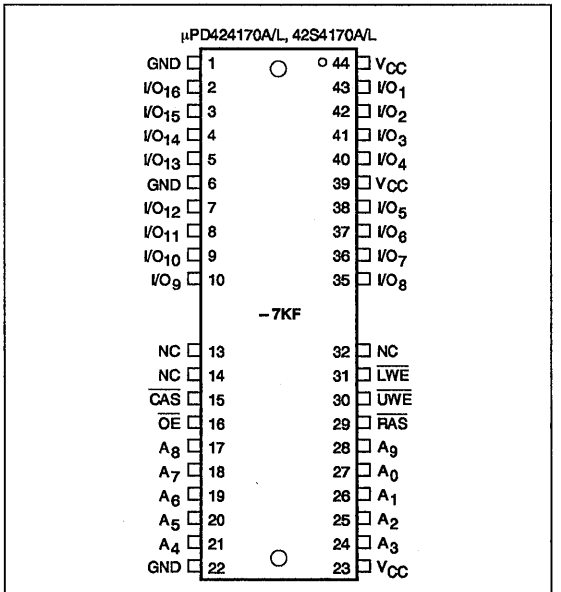


44/40-Pin Plastic TSOP (Normal Pinouts)



Suffix –7JF in the package identifier denotes normal pinout sequence.

44/40-Pin Plastic TSOP (Reverse Pinouts)

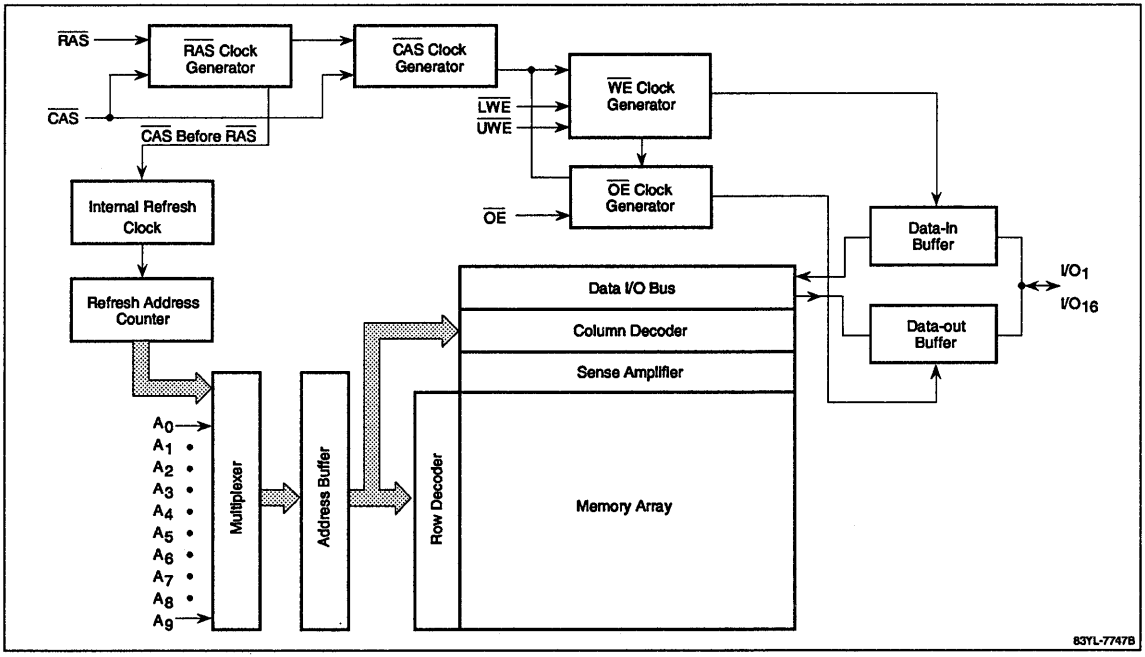


Suffix –7KF in the package identifier denotes reverse pinout sequence.

Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS}$	Column address strobe
I/O_1 - I/O_{16}	Data inputs and outputs
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{UWE}$ and $\overline{LWE}$	Byte write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{LWE}$	$\overline{UWE}$	$\overline{CAS}$	$\overline{OE}$	I/O_1 - I/O_8	I/O_9 - I/O_{16}
Standby	V_{IH}	X	X	X	X	High-Z	High-Z
Refresh cycle	V_{IL}	X	X	V_{IH}	X	High-Z	High-Z
Byte write cycle	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data input	High-Z
	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High-Z	Data input
Word read cycle	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	Data output	Data output
Word write cycle	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Data input	Data input
——	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	High-Z	High-Z

X = don't care.

7a

Ordering Information, μPD424170A (+ 5-volt power)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Package
μPD424170ALE-60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD424170AV-60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-70	70 ns	45 ns		
V-80	80 ns	50 ns		
μPD424170AG5-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD424170AG5M-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD424170L (+ 3.3-volt power)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Package
μPD424170LLE-A60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD424170LV-A60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-A70	70 ns	45 ns		
V-A80	80 ns	50 ns		
μPD424170LG5-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD424170LG5M-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD42S4170A (+ 5-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4170ALE-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4170AV-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic ZIP
V-70	70 ns	45 ns			
V-80	80 ns	50 ns			
μPD42S4170AG5-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns			
G5-80	80 ns	50 ns			
μPD42S4170AG5M-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns			
G5M-80	80 ns	50 ns			

Ordering Information, μPD42S4170L (+ 3.3-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4170LLE-A60	60 ns	40 ns	20 ns	100 μA	40-pin plastic SOJ
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			
μPD42S4170LV-A60	60 ns	40 ns	20 ns	100 μA	40-pin plastic ZIP
V-A70	70 ns	45 ns			
V-A80	80 ns	50 ns			
μPD42S4170LG5-A60	60 ns	40 ns	20 ns	100 μA	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns			
G5-A80	80 ns	50 ns			
μPD42S4170LG5M-A60	60 ns	40 ns	20 ns	100 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns			
G5M-A80	80 ns	50 ns			

Absolute Maximum Ratings

Voltage on any pin relative to GND	
+5-volt devices	−1.0 to +7.0 V
+3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
+5-volt devices	50 mA
+3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{LWE}$, $\overline{UWE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_{16}

Recommended Operating Conditions

		+5-Volt Devices			+3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} +0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.5		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

Self-Refresh Current

T_A = 0 to +70°C; V_{CC} = +5 V ±10% (42S4170A) or +3.3 V ±0.3 V (42S4170L)

Symbol	42S4170A	42S4170L	Conditions
I_{CC7}	300 μA max	100 μA max	I/O pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. Other input pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. $t_{RAS} \geq 100$ μs

DC Characteristics; +5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS} \geq V_{IH}$ (min); I_O = 0 mA
				300	μA	$\overline{RAS}$ = $\overline{CAS} \geq V_{CC} - 0.2$ V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

DC Characteristics; +3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			500	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				100	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–5		5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–5		5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10% or +3.3 V ±0.3 V

		-60		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5)		110		100		90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
	I_{CC1} (+3.3)		100		90		80		
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5)		110		100		90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
	I_{CC3} (+3.3)		100		90		80		
Operating current, fast-page cycle, average	I_{CC4} (+5)		90		80		70	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
	I_{CC4} (+3.3)		90		80		70		
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5)		110		100		90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
	I_{CC5} (+3.3)		100		90		80		
Access time from column address	t_{AA}		30		35		40	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		ns	(Note 15)
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	–35		–40		–50		ns	For 42S4170A/L only

7a

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	(Notes 4, 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		75		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		50		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Notes 13, 16)
Data-in setup time	t_{DS}	0		0		0		ns	(Notes 13, 16)
Masked write hold time referenced to $\overline{CAS}$	t_{MCH}	0		0		0		ns	
Masked write setup time referenced to $\overline{CAS}$	t_{MCS}	0		0		0		ns	
Masked write hold time referenced to $\overline{RAS}$	t_{MRH}	0		0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	(Note 9)
Output disable from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t_{PC}	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with exended data output	t_{PRWC}	85		90		100		ns	(Note 6)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		10		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		μs	For 42S4170A/L
Random read or write cycle time	t_{RC}	120		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	120		130		150		ns	For 42S4170A/L
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Read-modify-write cycle time	t_{RWC}	165		175		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Rise and fall times	t_T	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		ns	(Note 12)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Write command setup time	t_{WCS}	0		0		0		ns	(Note 14)
Write command pulse width	t_{WP}	15		15		15		ns	(Note 12)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF. For 3.3-volt devices, V_{OH} = 2.0 V and V_{OL} = 0.8 V (ac reference levels).

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max).
If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{UWE}$ and $\overline{LWE}$ for delayed write or read-modify-write cycles.

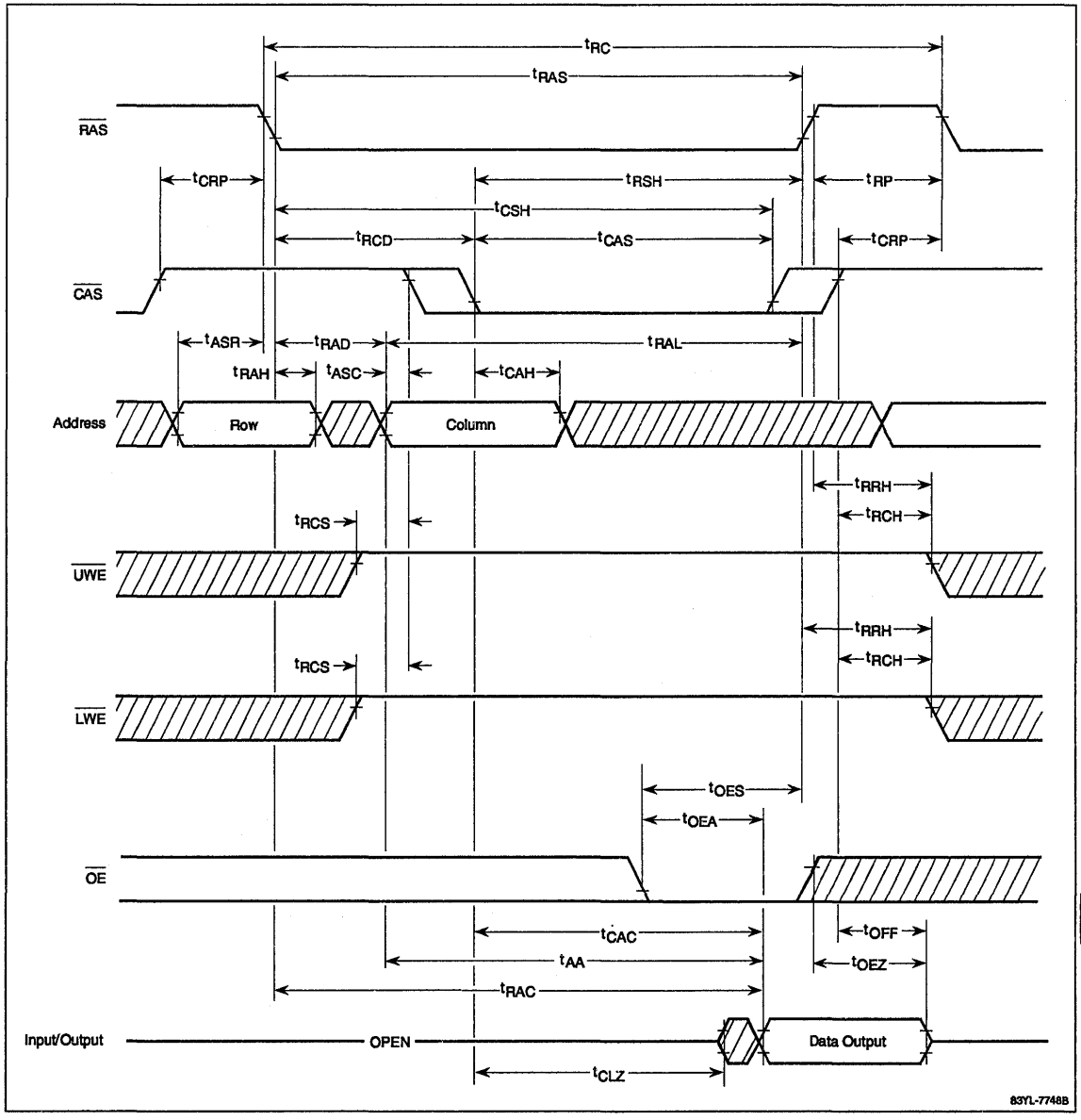
(14) t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD} and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) Holding $\overline{CAS}$ low prior to $\overline{RAS}$ going negative will initiate a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (t_{CSR} and t_{CHR} must be satisfied).

(16) The first $\overline{WE}$ falling edge is used as a reference for the setup and hold requirements of t_{DS} and t_{DH} (late write cycle).

Timing Waveforms

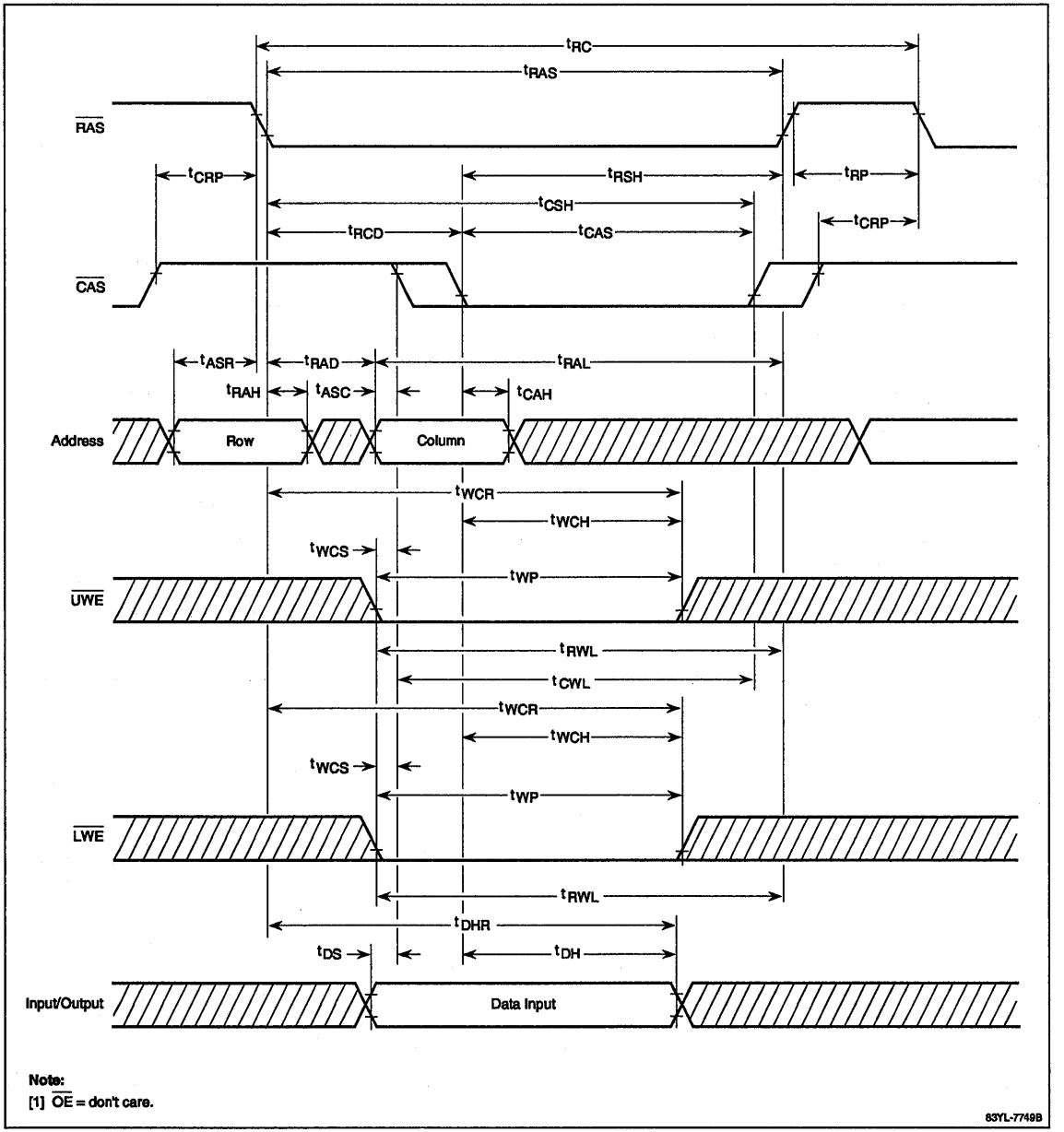
Word Read Cycle



7a

Timing Waveforms (cont)

Word Early-Write Cycle

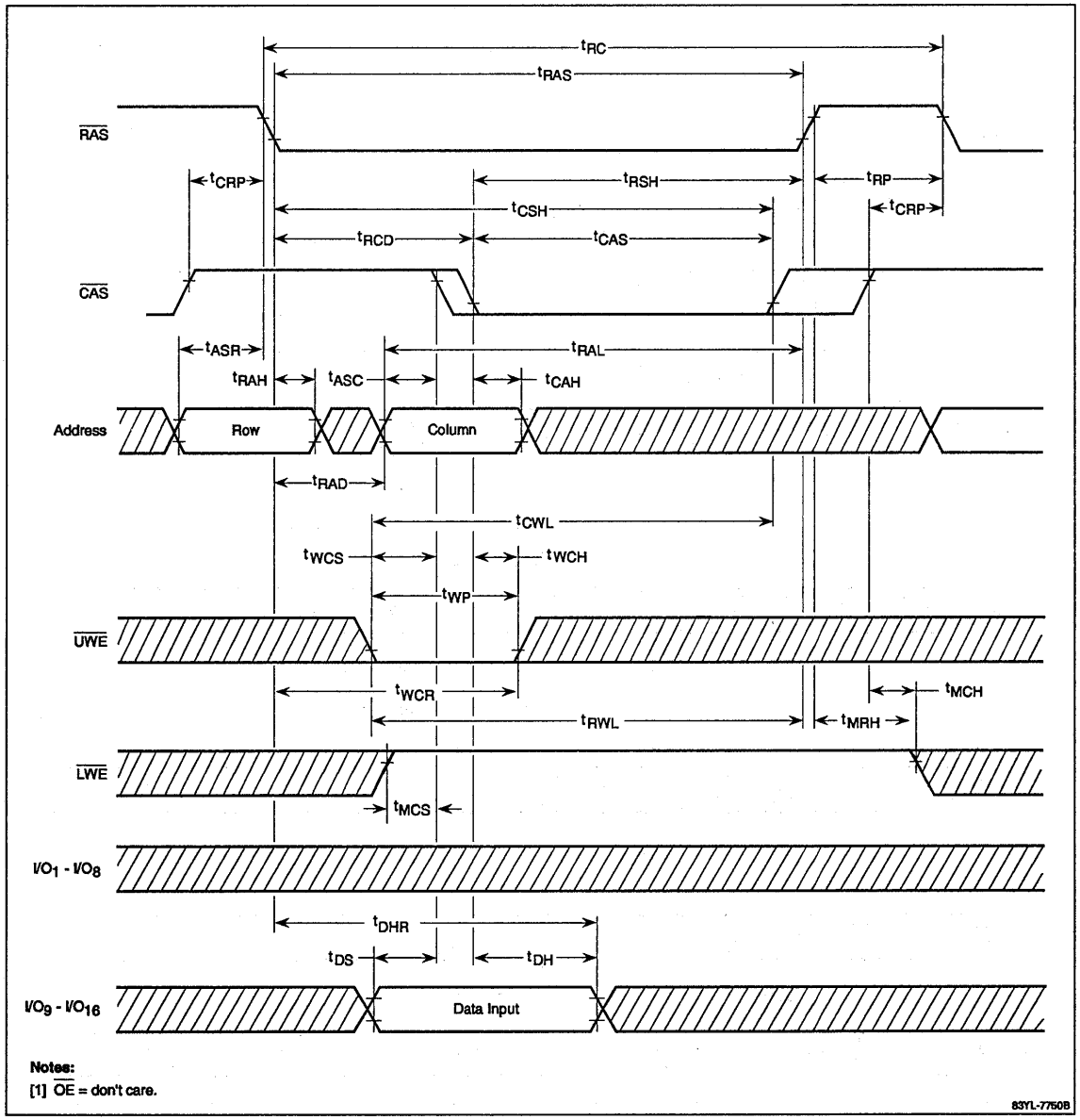


Note:
[1] $\overline{OE}$ = don't care.

83YL-7749B

Timing Waveforms (cont)

Byte Early-Write Cycle

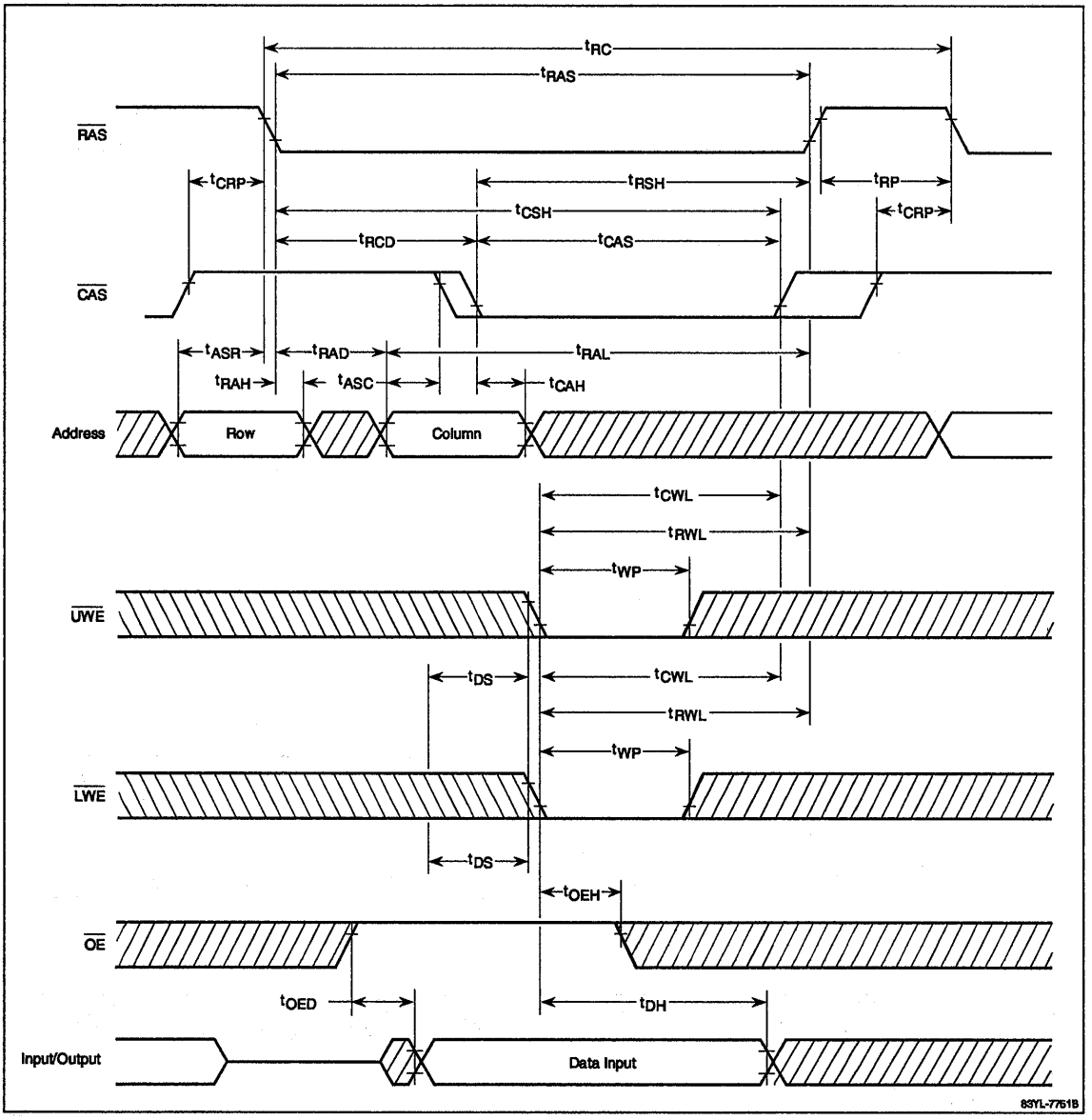


Notes:
[1] $\overline{OE}$ = don't care.

83YL-7750B

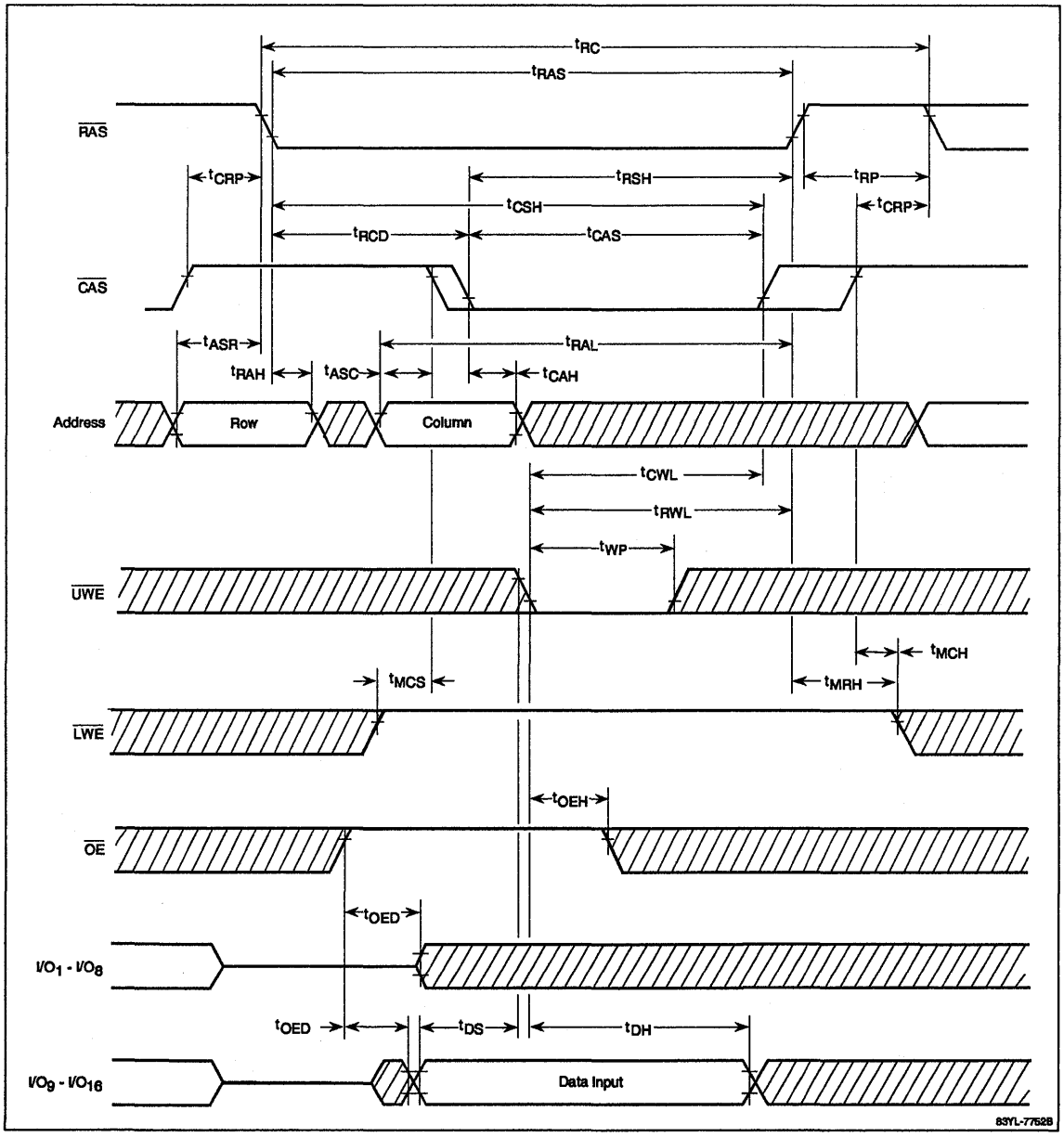
Timing Waveforms (cont)

Word Late-Write Cycle



Timing Waveforms (cont)

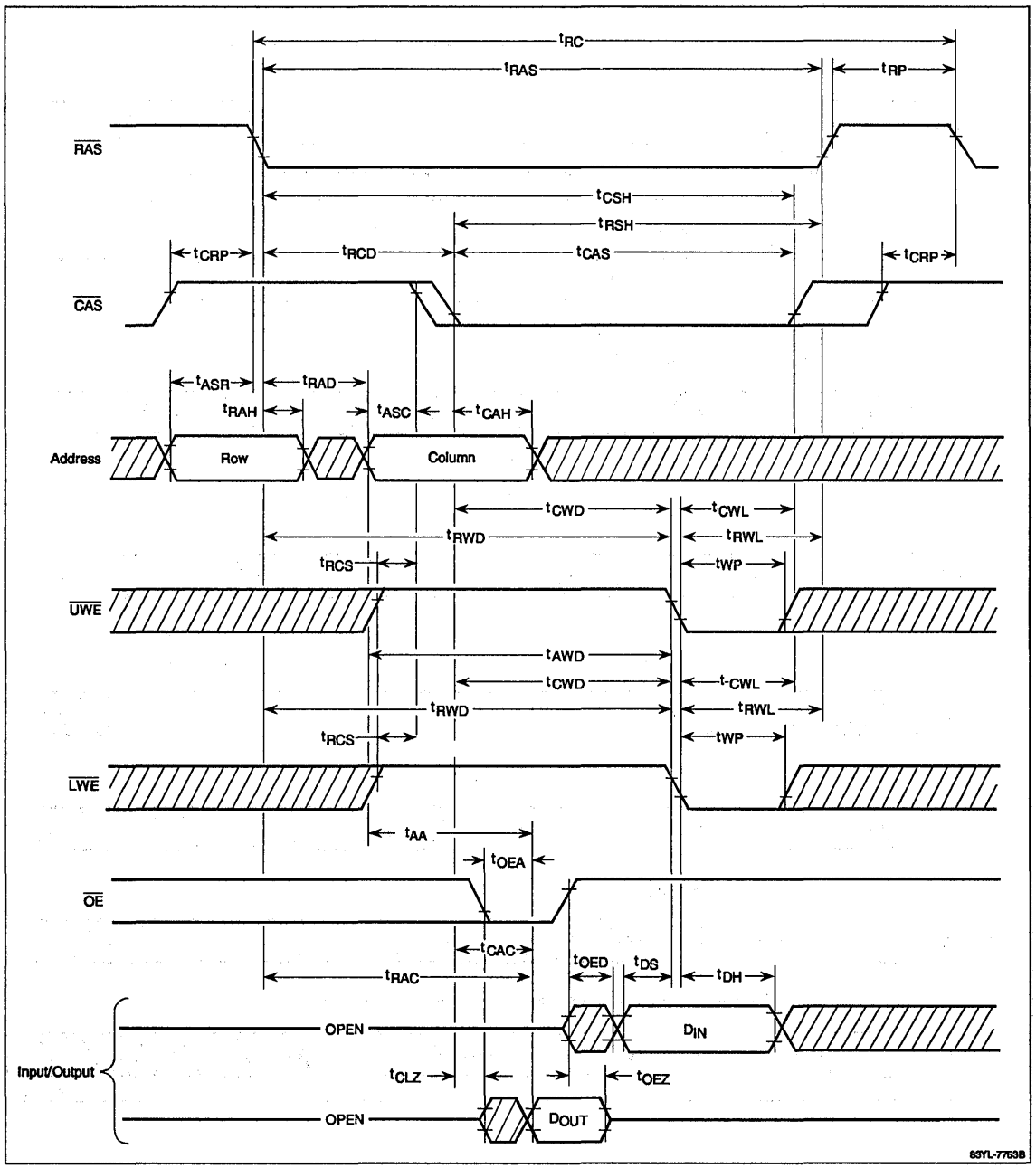
Byte Late-Write Cycle



7a

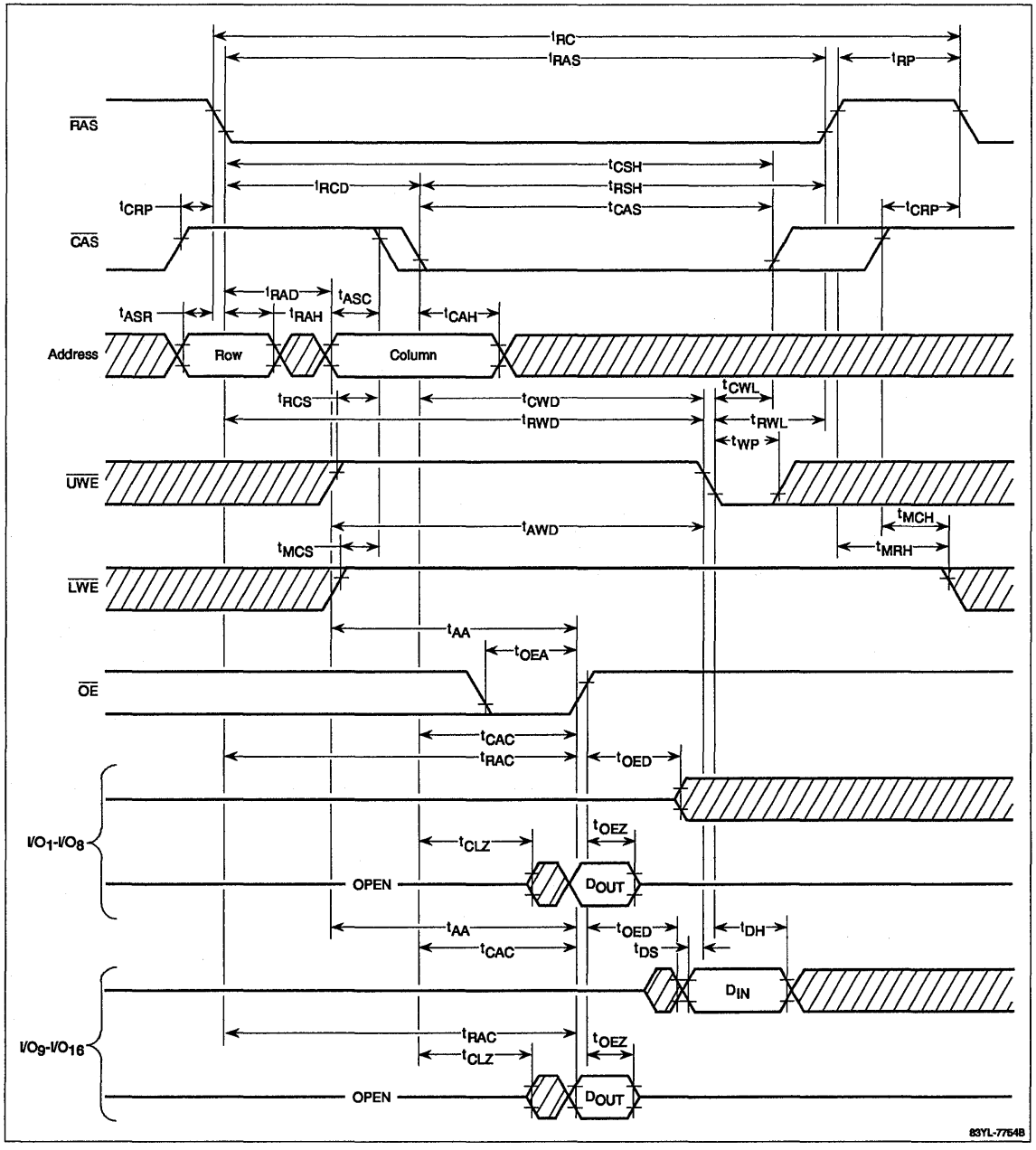
Timing Waveforms (cont)

Word Read-Modify-Write Cycle



Timing Waveforms (cont)

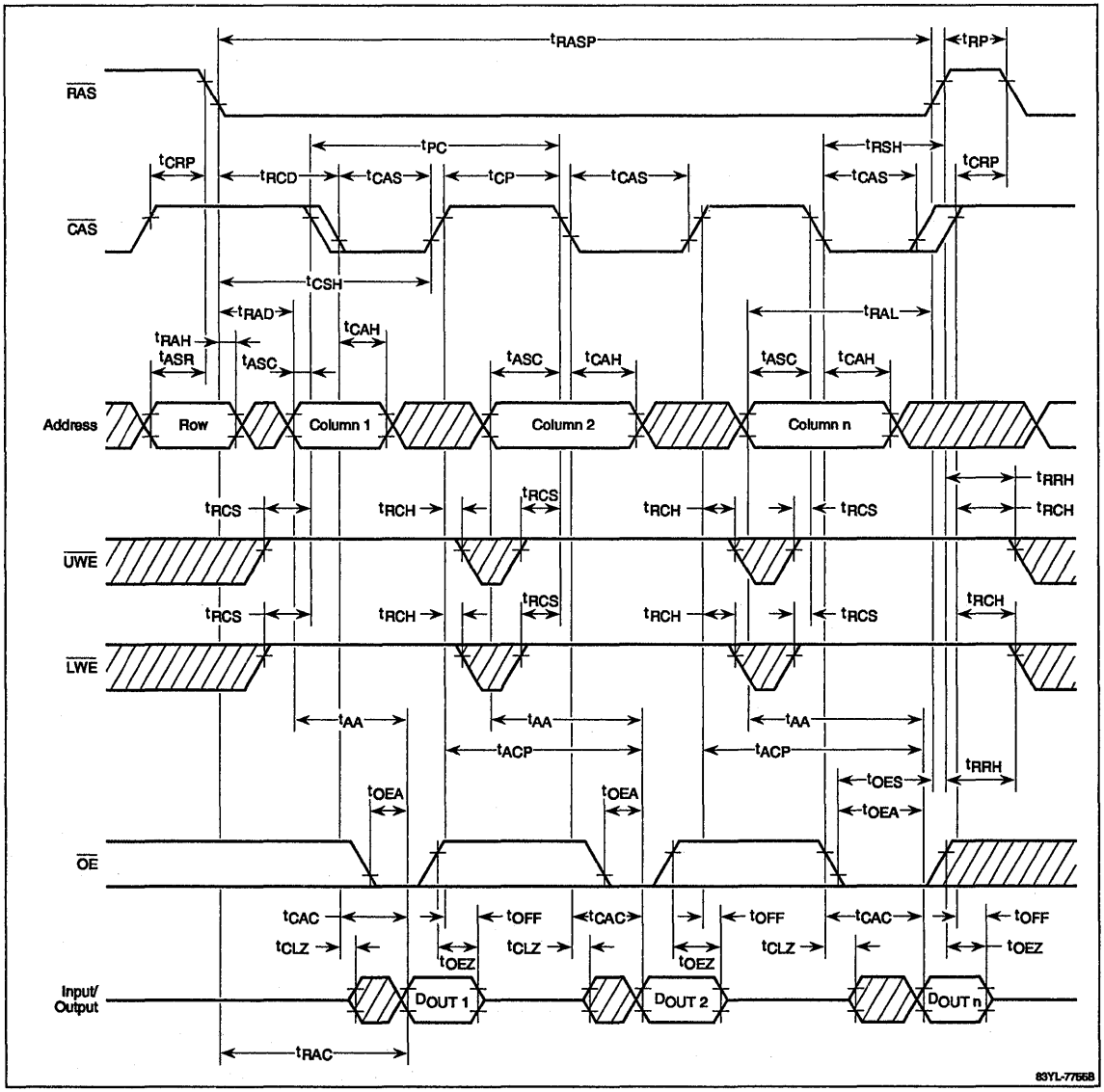
Byte Read-Modify-Write Cycle



7a

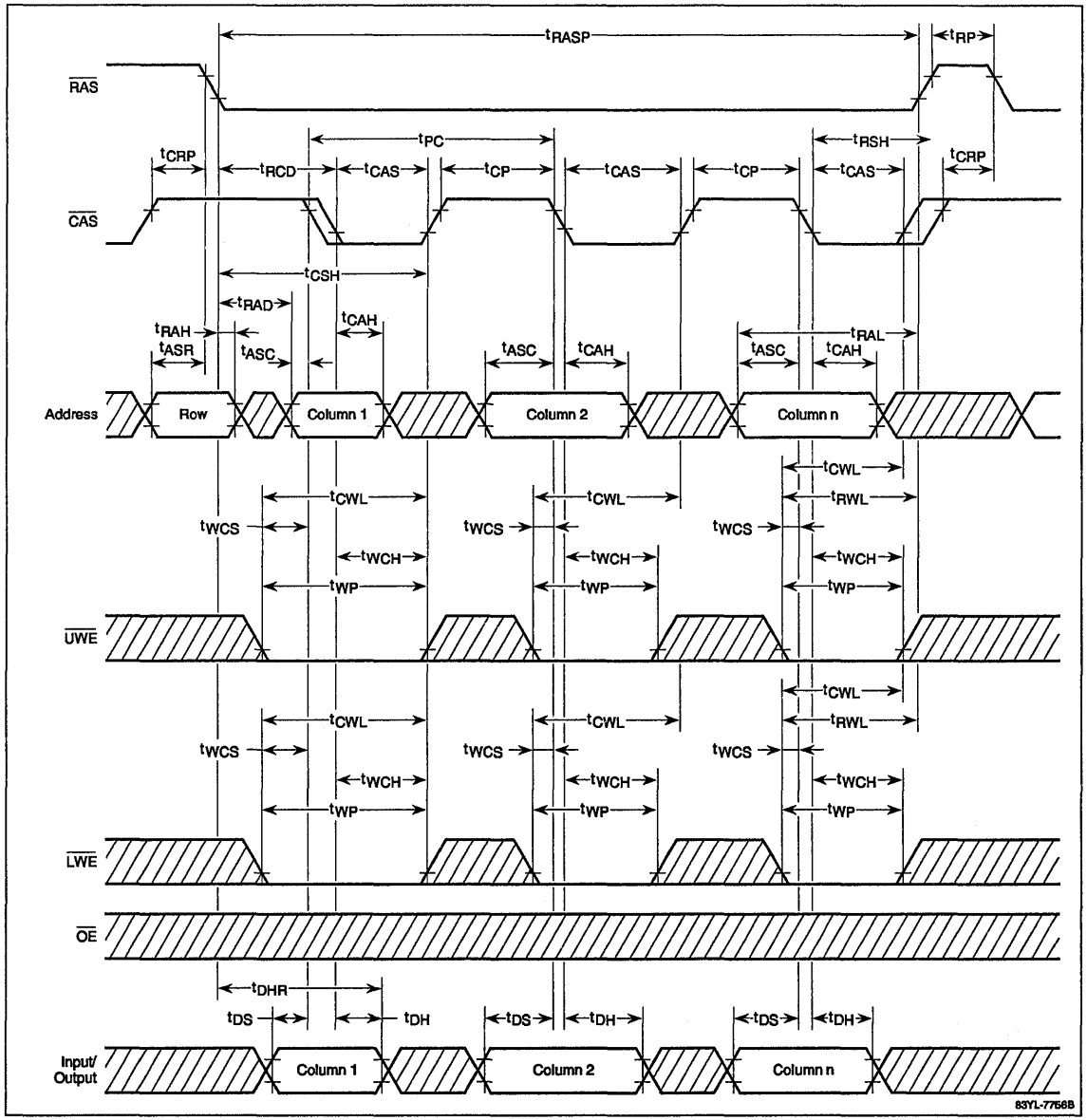
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

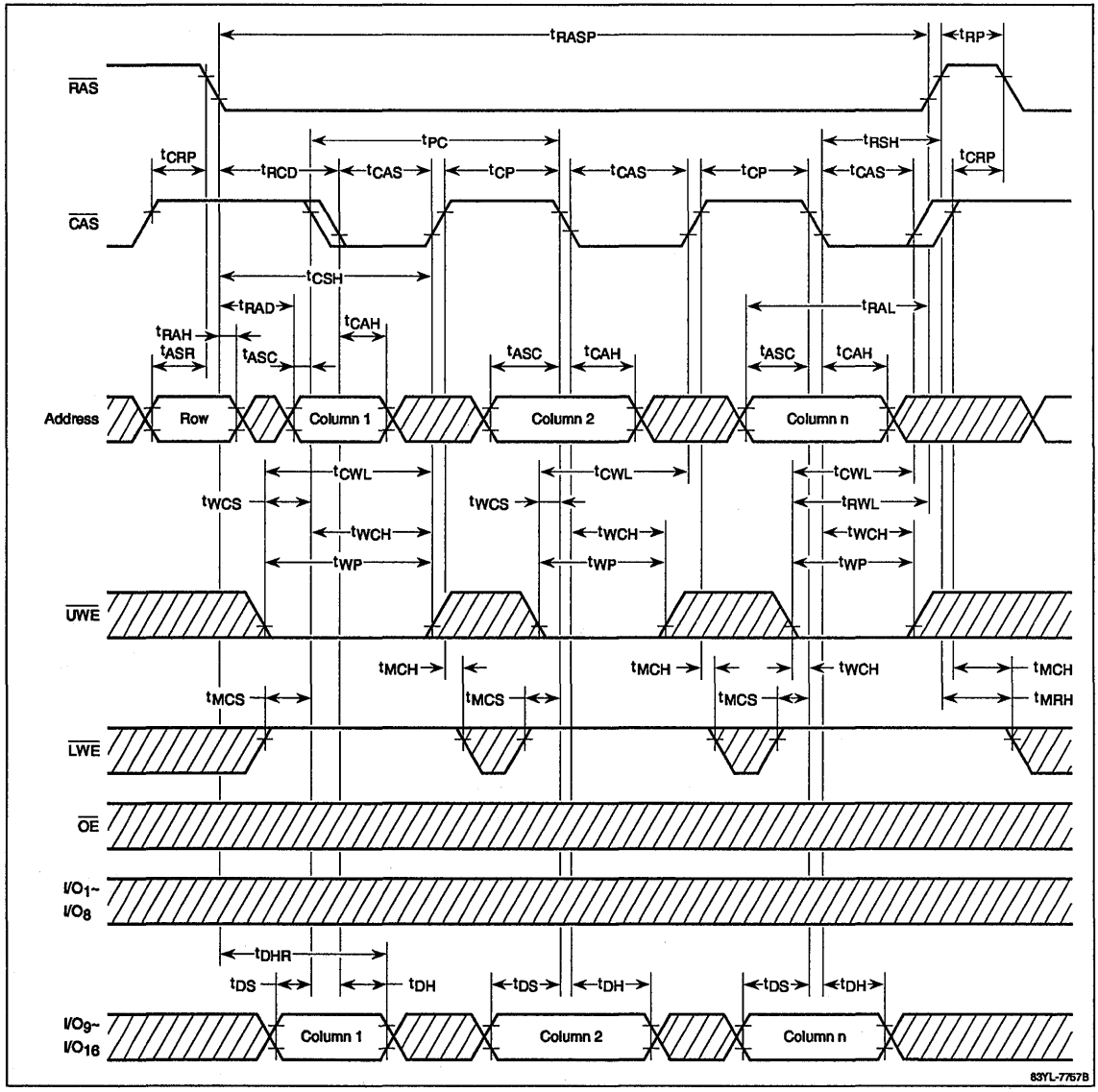
Word Fast-Page Write Cycle



7a

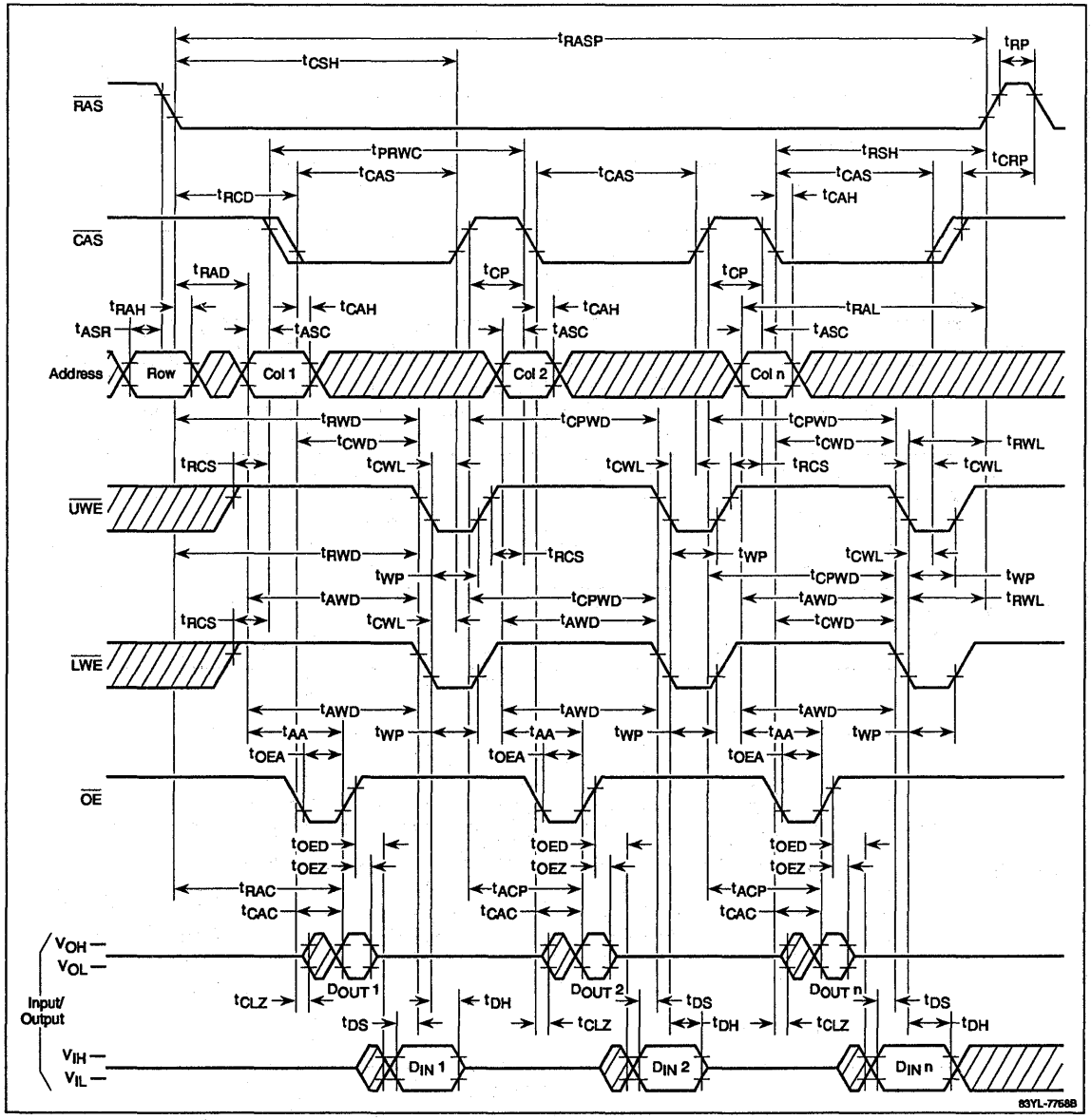
Timing Waveforms (cont)

Byte Fast-Page Write Cycle



Timing Waveforms (cont)

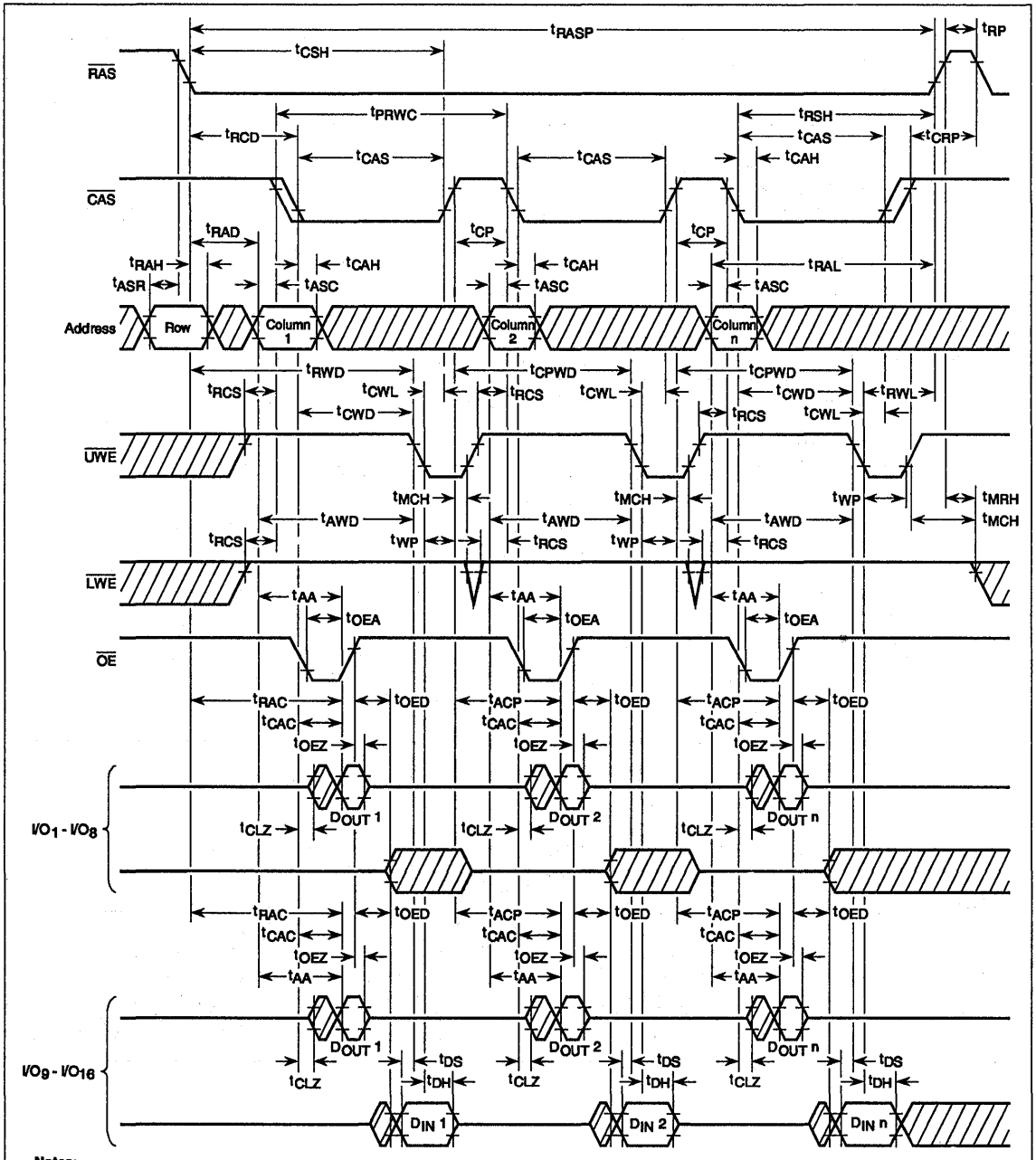
Word Fast-Page Read-Modify-Write Cycle



7a

Timing Waveforms (cont)

Byte Fast-Page Read-Modify-Write Cycle



Notes:

[1] $\overline{WE}$ = $\overline{LWE}$ or $\overline{UWE}$ for lower byte write and upper byte write cycles, respectively.

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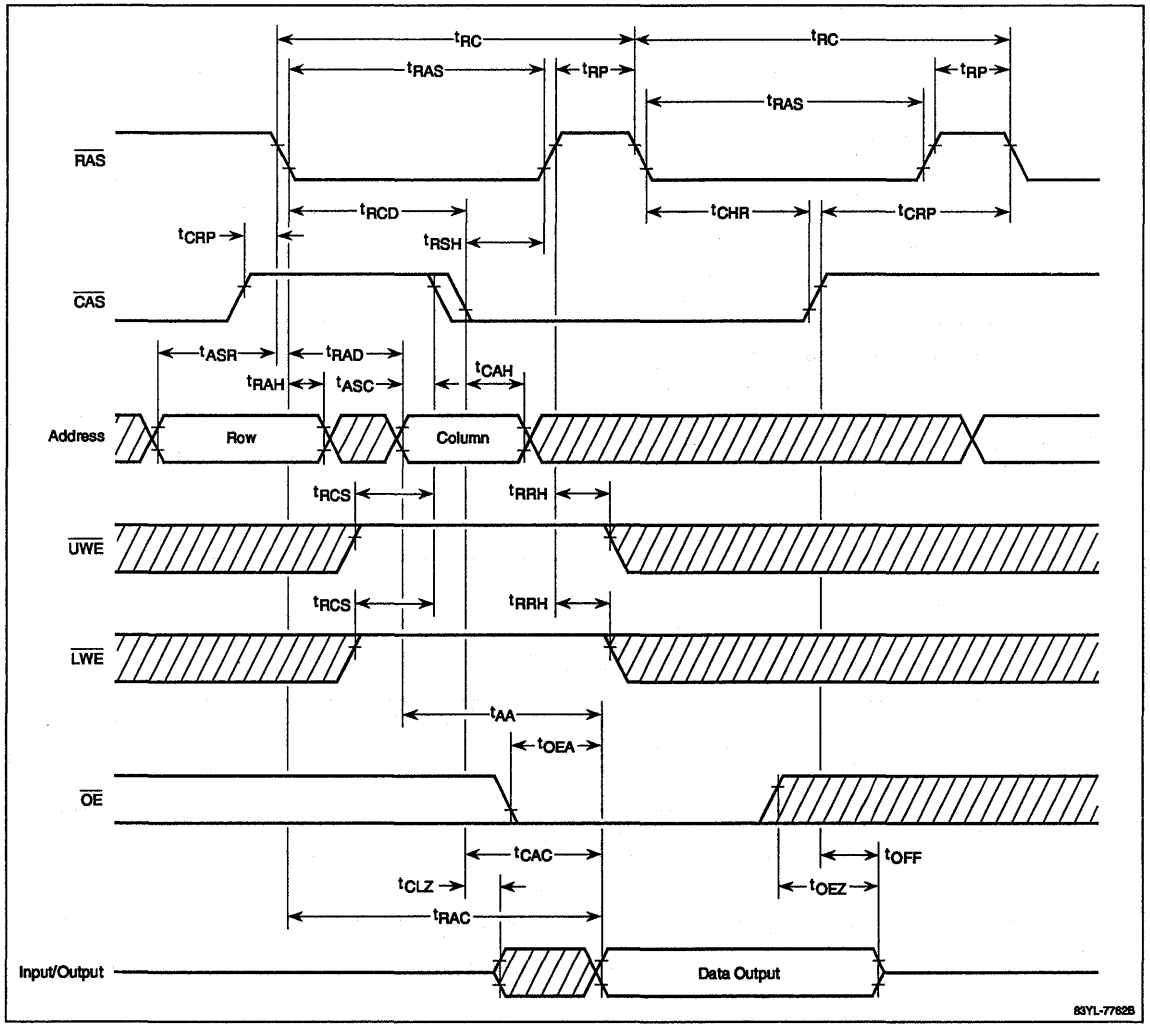
Timing Waveforms (cont)

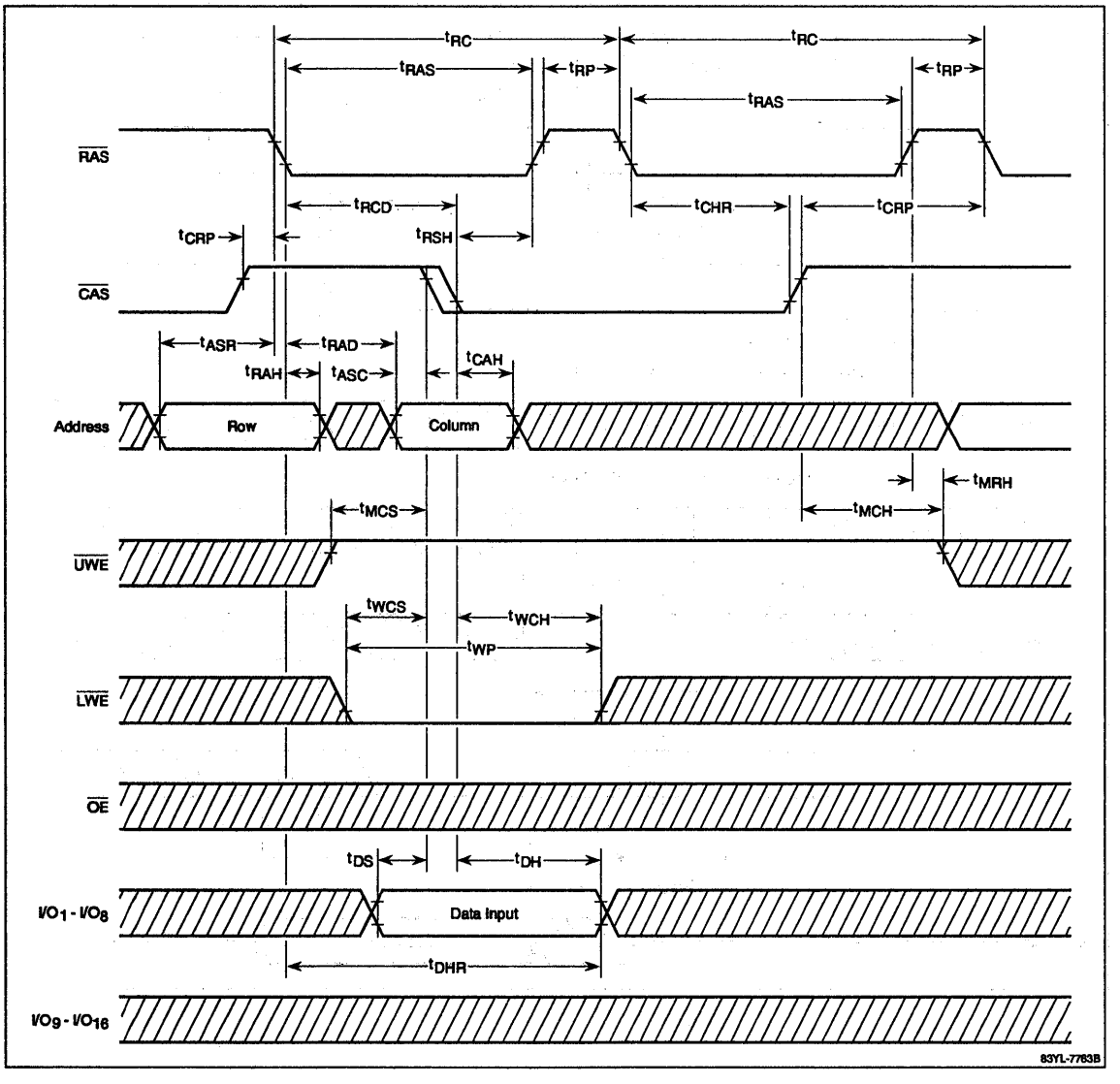
Hidden Refresh Cycle (Read Cycle)



7a

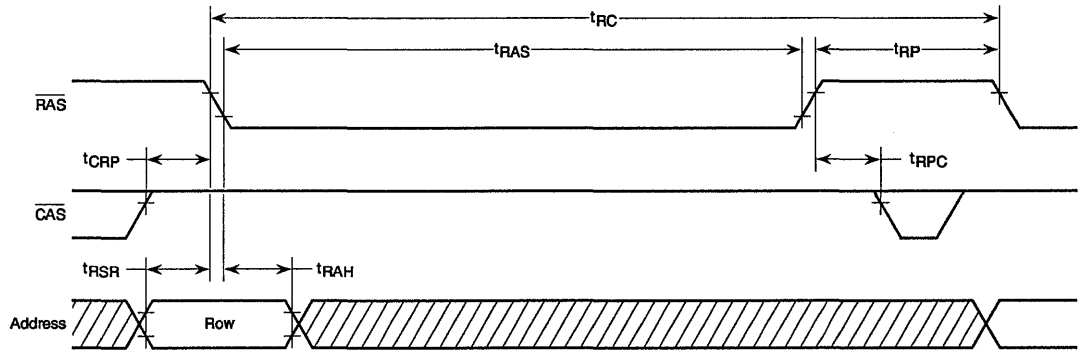
Timing Waveforms (cont)

Byte Hidden-Refresh Cycle (Write)



Timing Waveforms (cont)

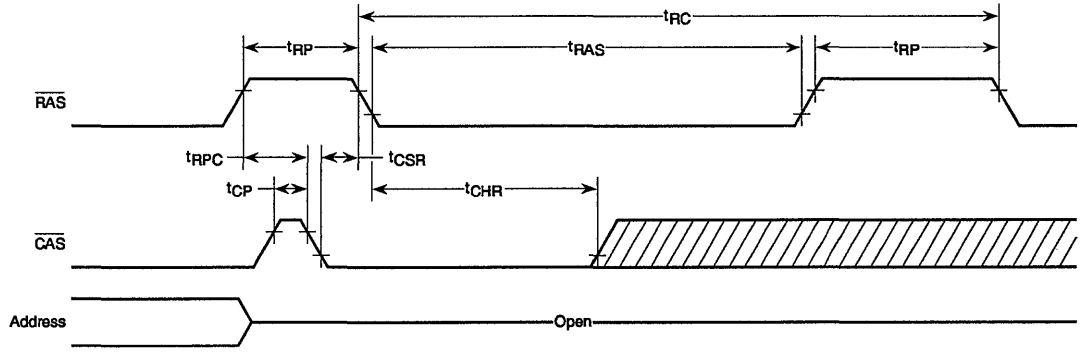
$\overline{RAS}$-Only Refresh Cycle



Notes:
(1) $\overline{UWE}$, $\overline{LWE}$ and $\overline{OE}$ = V_{IH} or V_{IL}.

83YL-7760B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Notes:
(1) D_{IN}, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$ and Addresses = V_{IH} or V_{IL}.

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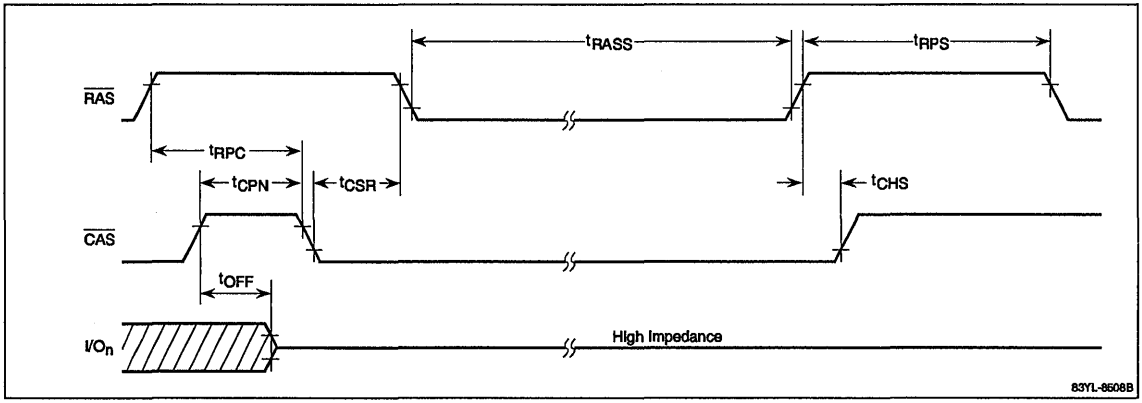
7a

Timing Waveforms (cont)

CBR Self-Refresh Cycle



μPD424190A/L, 42S4190A/L
262,144 x 18-Bit
Dynamic CMOS RAM

Description

The μPD424190A/L and μPD42S4190A/L are fast-page dynamic RAMs organized as 262,144 words by 18 bits and designed to operate from a single power supply.

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
424190A	+5 V
424190L	+3.3 V
42S4190A	+5 V; self-refresh mode
42S4190L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

Word writing (I/O_1 - I/O_{18}), upper byte writing (I/O_{10} - I/O_{18}), and lower byte writing (I/O_1 - I/O_9) are all possible using $\overline{UWE}$ and $\overline{LWE}$. If $\overline{UWE}$ or $\overline{LWE}$ goes low during an early write cycle, all data outputs remain in high impedance. Either going low causes a byte write cycle, while bringing both low at the same time results in a word write cycle. $\overline{UWE}$ and $\overline{LWE}$ cannot be staggered within the same write cycle.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh address. $\overline{RAS}$-only refresh cycles will also refresh all memory locations.

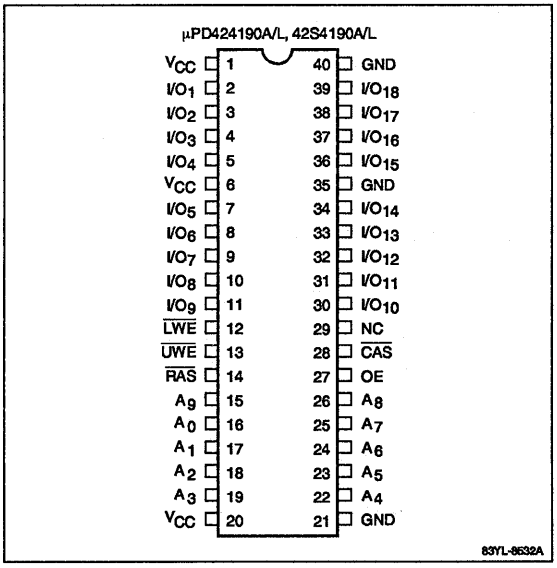
The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

- 262,144 by 18-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option
- Byte write control with $\overline{UWE}$ and $\overline{LWE}$
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 1024 refresh cycles every 16 ms
- 40-pin SOJ, 40-pin ZIP, and 44/40-pin TSOP plastic packaging

Pin Configurations

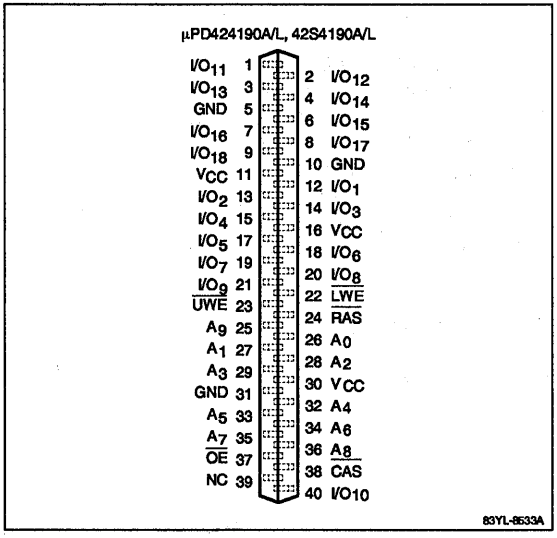
40-Pin Plastic SOJ



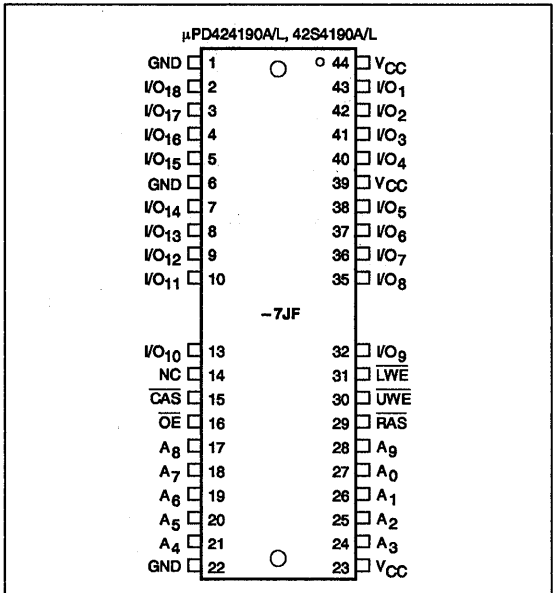
7b

Pin Configurations (cont)

40-Pin Plastic ZIP

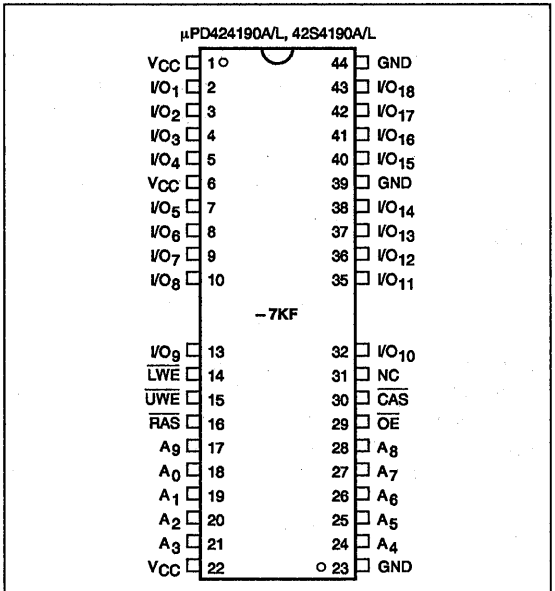


44/40-Pin Plastic TSOP (Reverse Pinouts)



Suffix –7JF in the package identifier denotes reverse pinout sequence.

44/40-Pin Plastic TSOP (Normal Pinouts)



Suffix –7KF in the package identifier denotes normal pinout sequence.

Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS}$	Column address strobe
I/O_1 - I/O_{18}	Data inputs and outputs
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{UWE}$ and $\overline{LWE}$	Byte write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

Ordering Information, μPD424190A (+ 5-volt power)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Package
μPD424190ALE-60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD424190AV-60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-70	70 ns	45 ns		
V-80	80 ns	50 ns		
μPD424190AG5-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD424190AG5M-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD424190L (+ 3.3-volt power)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Package
μPD424190LLE-A60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD424190LV-A60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-A70	70 ns	45 ns		
V-A80	80 ns	50 ns		
μPD424190LG5-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD424190LG5M-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

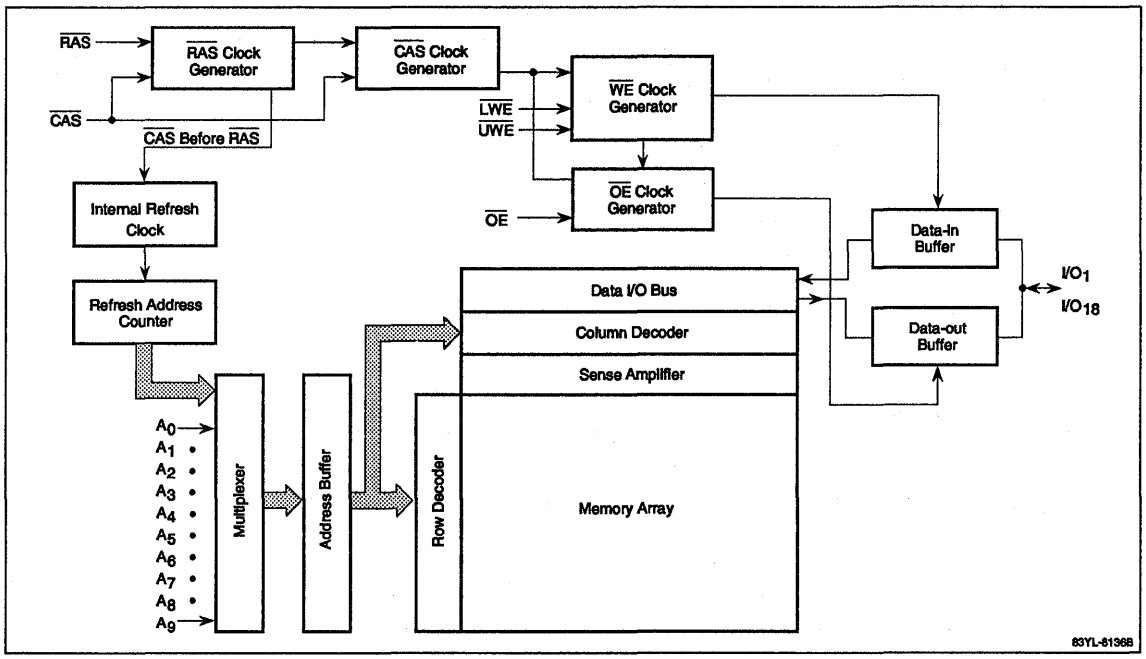
Ordering Information, μPD42S4190A (+ 5-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4190ALE-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4190AV-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic ZIP
V-70	70 ns	45 ns			
V-80	80 ns	50 ns			
μPD42S4190AG5-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns			
G5-80	80 ns	50 ns			
μPD42S4190AG5M-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns			
G5M-80	80 ns	50 ns			

Ordering Information, μPD42S4190L (+ 3.3-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4190LLE-A60	60 ns	40 ns	20 ns	300 μA	40-pin plastic SOJ
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			
μPD42S4190LV-A60	60 ns	40 ns	20 ns	300 μA	40-pin plastic ZIP
V-A70	70 ns	45 ns			
V-A80	80 ns	50 ns			
μPD42S4190LG5-A60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns			
G5-A80	80 ns	50 ns			
μPD42S4190LG5M-A60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns			
G5M-A80	80 ns	50 ns			

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{LWE}$	$\overline{UWE}$	$\overline{CAS}$	$\overline{OE}$	I/O_1 - I/O_9	I/O_{10} - I/O_{18}
Standby	V_{IH}	X	X	X	X	High-Z	High-Z
Refresh cycle	V_{IL}	X	X	V_{IH}	X	High-Z	High-Z
Byte write cycle	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data input	High-Z
	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High-Z	Data input
Word read cycle	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	Data output	Data output
Word write cycle	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Data input	Data input
——	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	High-Z	High-Z

X = don't care.

7b

Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
5-volt devices	50 mA
3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{LWE}$, $\overline{UWE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_{18}

Recommended Operating Conditions

		5-Volt Devices			3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} +0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.5		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

Self-Refresh Current

T_A = 0 to +70°C; V_{CC} = +5 V ±10% (42S4190A) or +3.3 V ±0.3 V (42S4190L)

Symbol	42S4190A	42S4190L	Conditions
I_{CC7}	300 μA max	100 μA max	I/O pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. Other input pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. $t_{RAS} \geq 100$ μs

DC Characteristics; 5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$ (min); I_O = 0 mA
				300	μA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

DC Characteristics; 3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			500	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				100	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–5		5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–5		5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = –2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

AC Characteristics

T_A = 0 to +70°C

μPD424190A, 42S4190A: V_{CC} = +5.0 V ±10%

μPD424190L, 42S4190L: V_{CC} = +3.3 V ±0.3 V

		-60		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5)		130		120		110	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
	I_{CC1} (+3.3)		120		110		100		
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5)		130		120		110	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
	I_{CC3} (+3.3)		120		110		100		
Operating current, fast-page cycle, average	I_{CC4} (+5)		110		100		90	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
	I_{CC4} (+3.3)		110		100		90		
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5)		140		130		120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
	I_{CC5} (+3.3)		130		120		110		
Access time from column address	t_{AA}		30		35		40	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		ns	(Note 15)
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	–35		–40		–50		ns	For 42S4190A/L only

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	(Notes 4, 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		75		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		50		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Notes 13, 16)
Data-in setup time	t_{DS}	0		0		0		ns	(Notes 13, 16)
Masked write hold time referenced to $\overline{CAS}$	t_{MCH}	0		0		0		ns	
Masked write setup time	t_{MCS}	0		0		0		ns	
Masked write hold time referenced to $\overline{RAS}$	t_{MRH}	0		0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	(Note 9)
Output disable from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t_{PC}	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with exended data output	t_{PRWC}	85		90		100		ns	(Note 6)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		10		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		μs	For 42S4190A/L
Random read or write cycle time	t_{RC}	120		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	120		130		150		ns	For 42S4190A/L
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Read-modify-write cycle time	t_{RWC}	165		175		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Rise and fall times	t_T	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		ns	(Note 12)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Write command setup time	t_{WCS}	0		0		0		ns	(Note 14)
Write command pulse width	t_{WP}	15		15		15		ns	(Note 12)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF. For 3.3-volt devices, V_{OH} = 2.0 V and V_{OL} = 0.8 V (ac reference levels).

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max).
If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

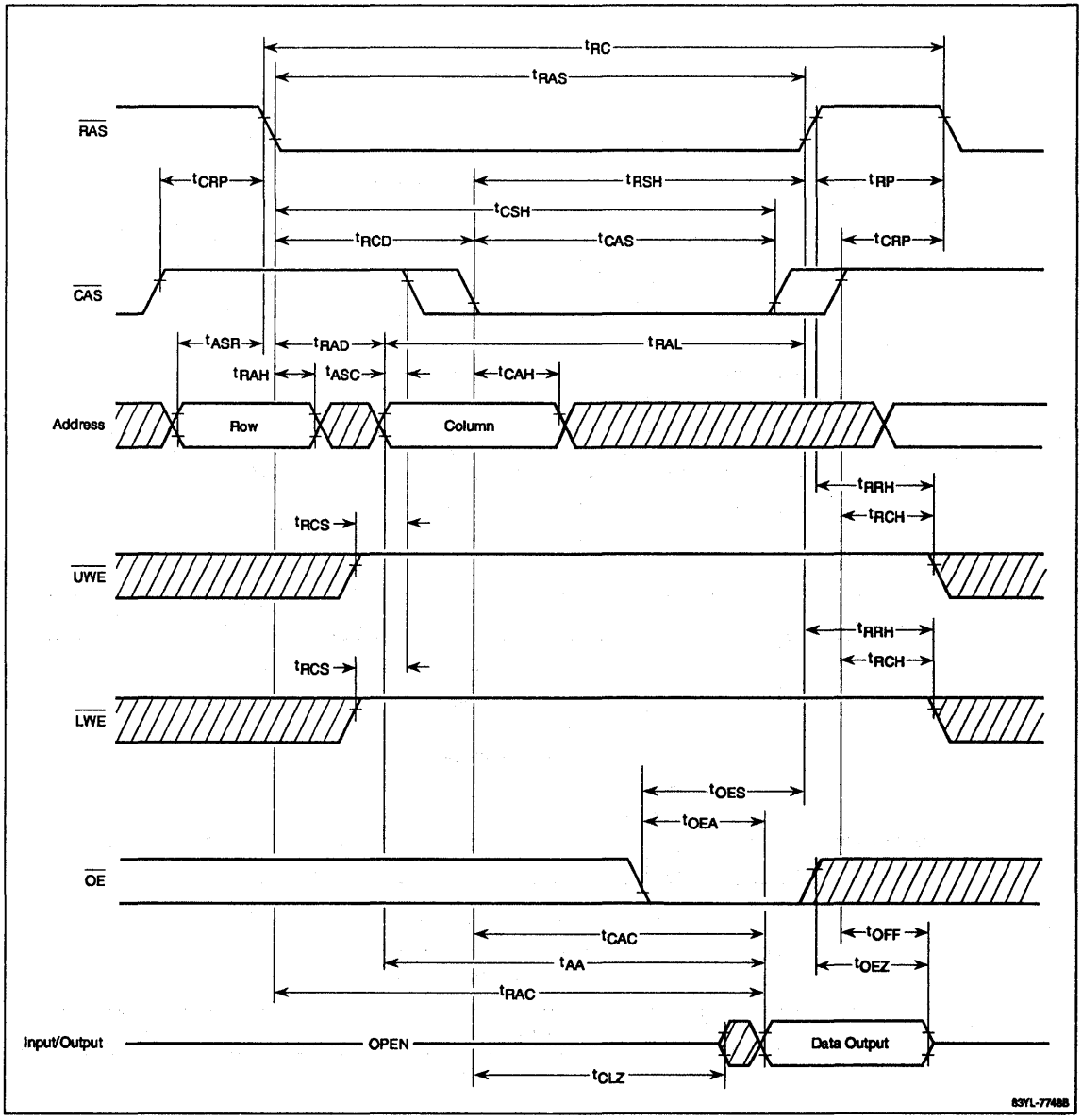
(14) t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD} and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) Holding $\overline{CAS}$ low prior to $\overline{RAS}$ going negative will initiate a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (t_{CSR} and t_{CHR} must be satisfied).

(16) The first $\overline{WE}$ falling edge is used as a reference for the setup and hold requirements of t_{DS} and t_{DH} (late write cycle).

Timing Waveforms

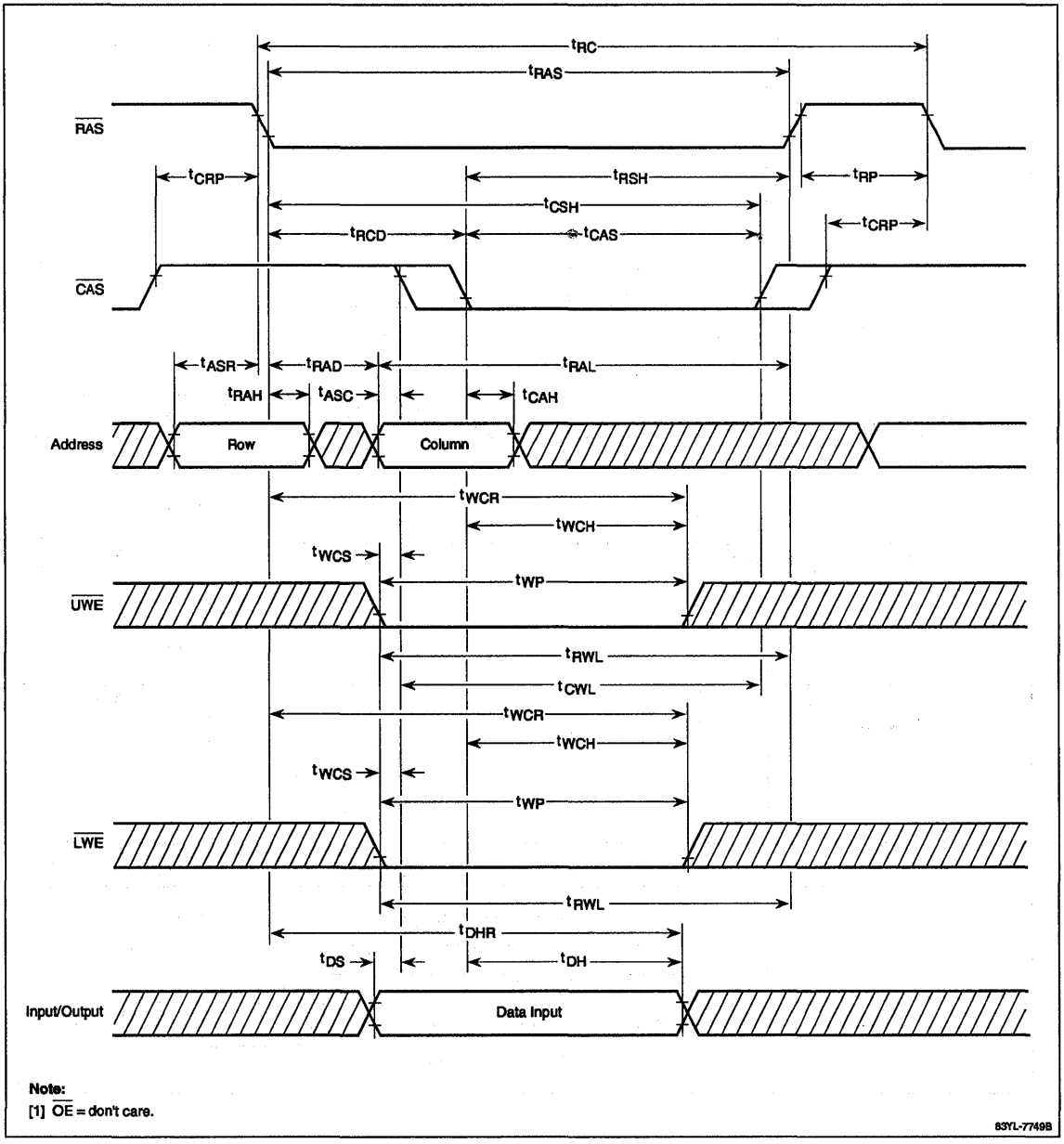
Word Read Cycle



7b

Timing Waveforms (cont)

Word Early-Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

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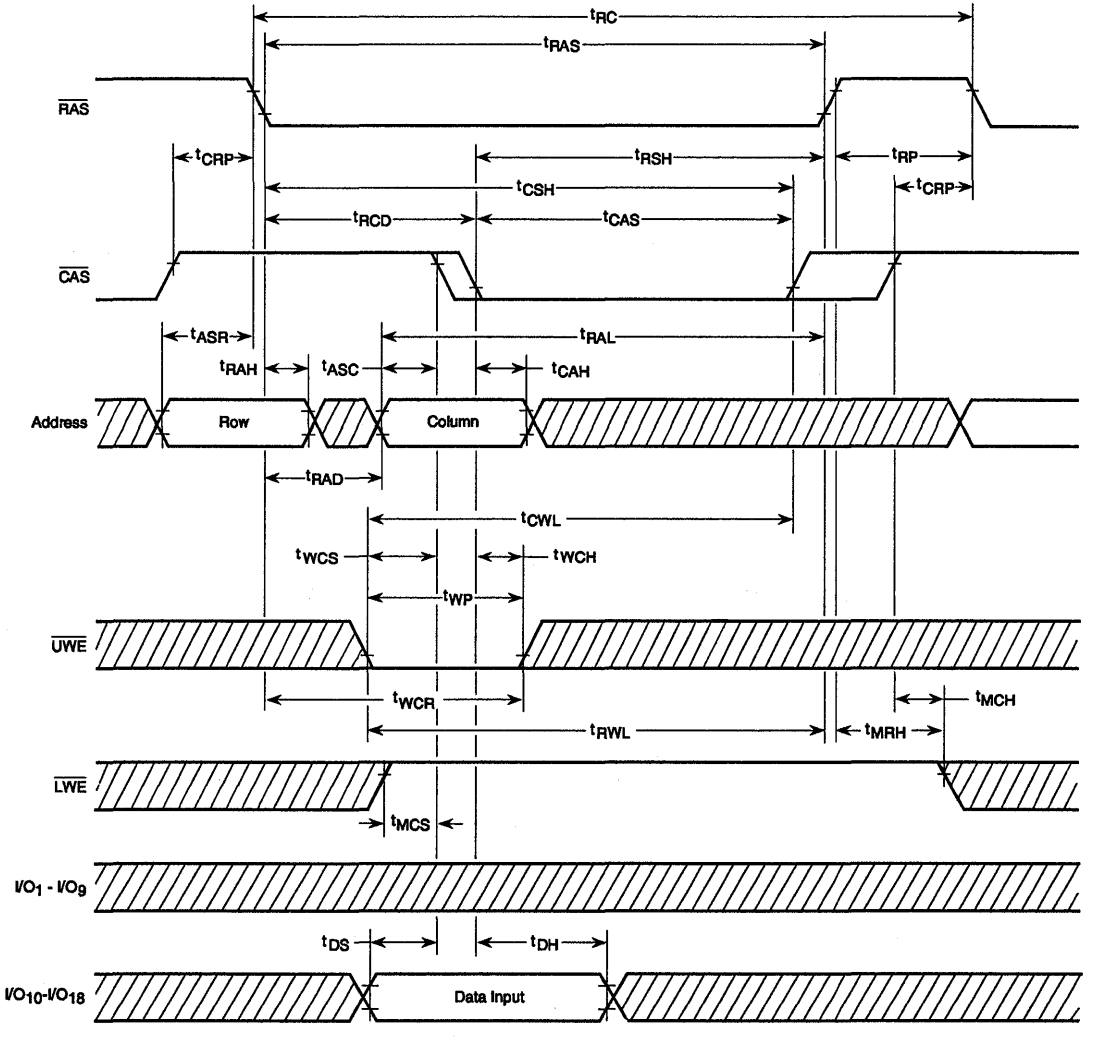
Timing Waveforms (cont)

Byte Early-Write Cycle



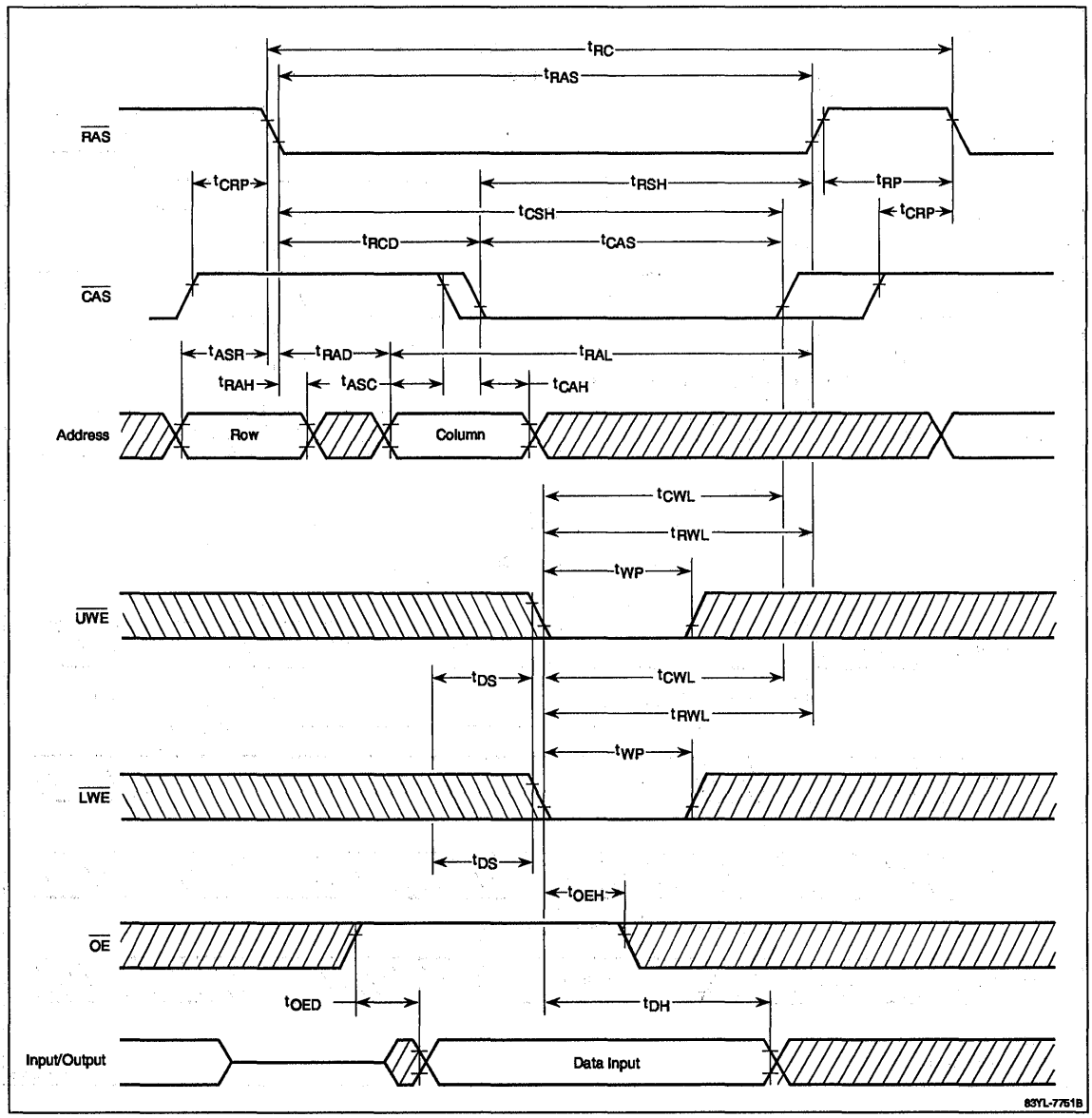
Notes:
[1] $\overline{OE}$ = don't care.

83YL-6137B

7b

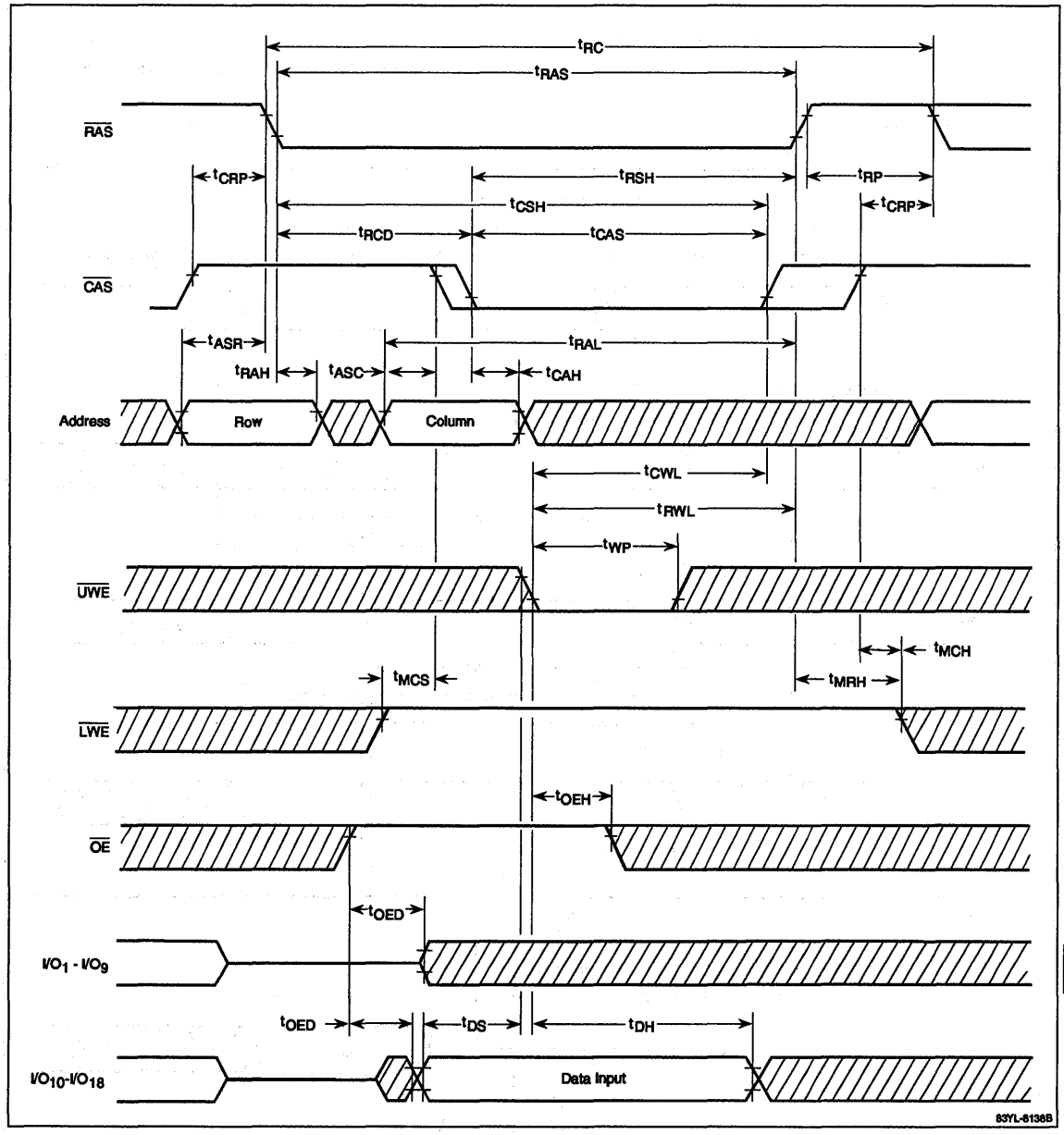
Timing Waveforms (cont)

Word Late-Write Cycle



Timing Waveforms (cont)

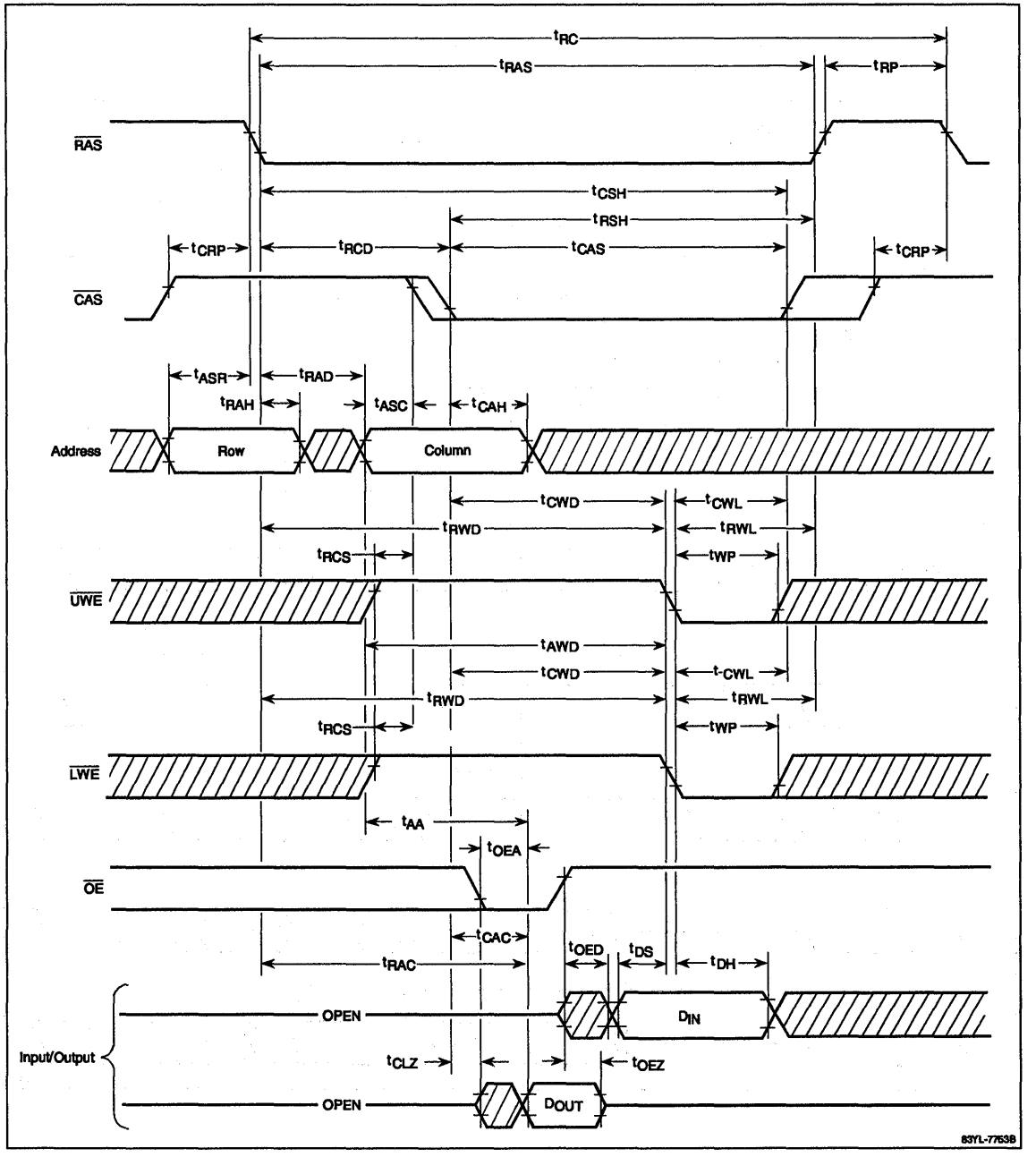
Byte Late-Write Cycle



7b

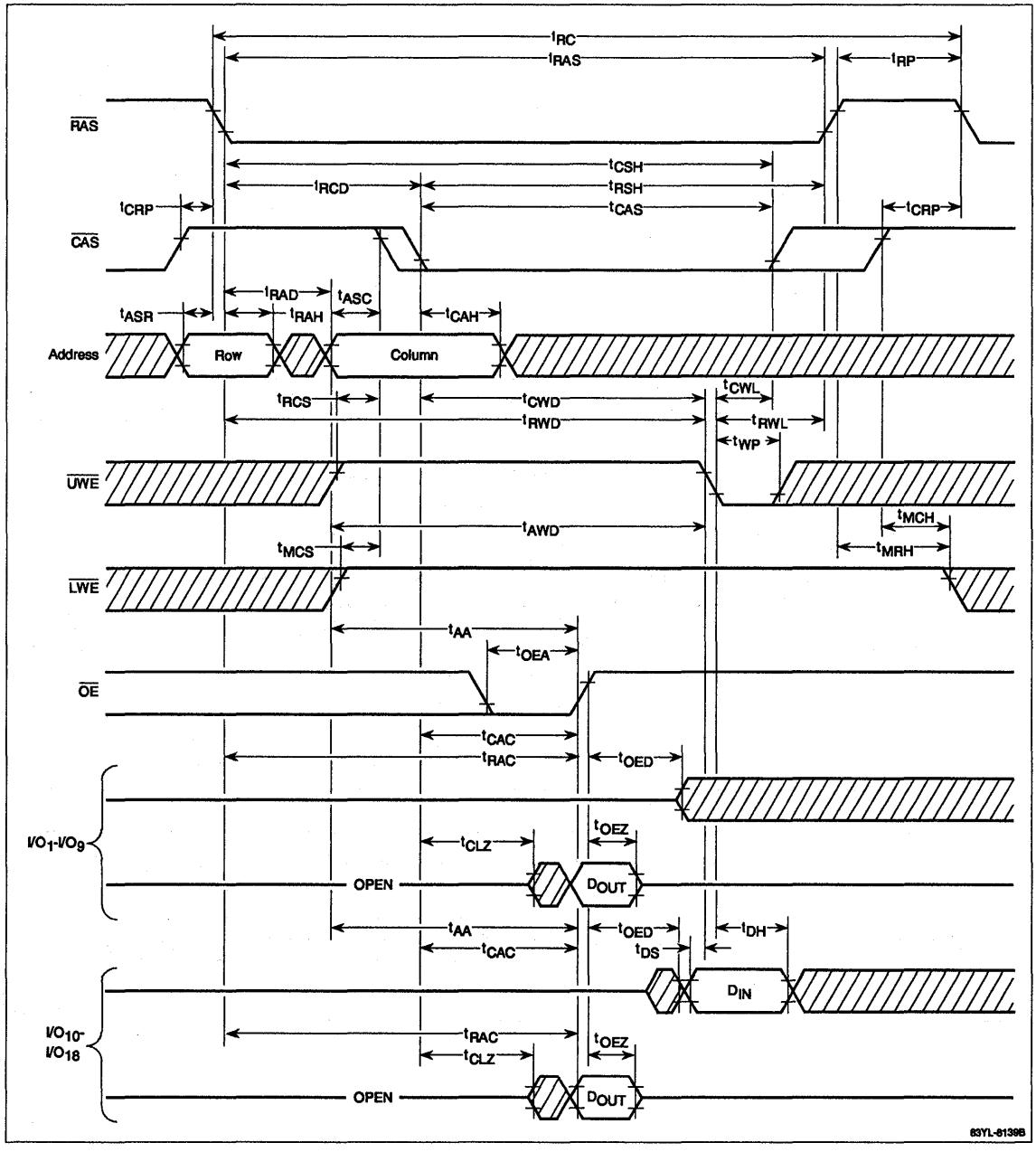
Timing Waveforms (cont)

Word Read-Modify-Write Cycle



Timing Waveforms (cont)

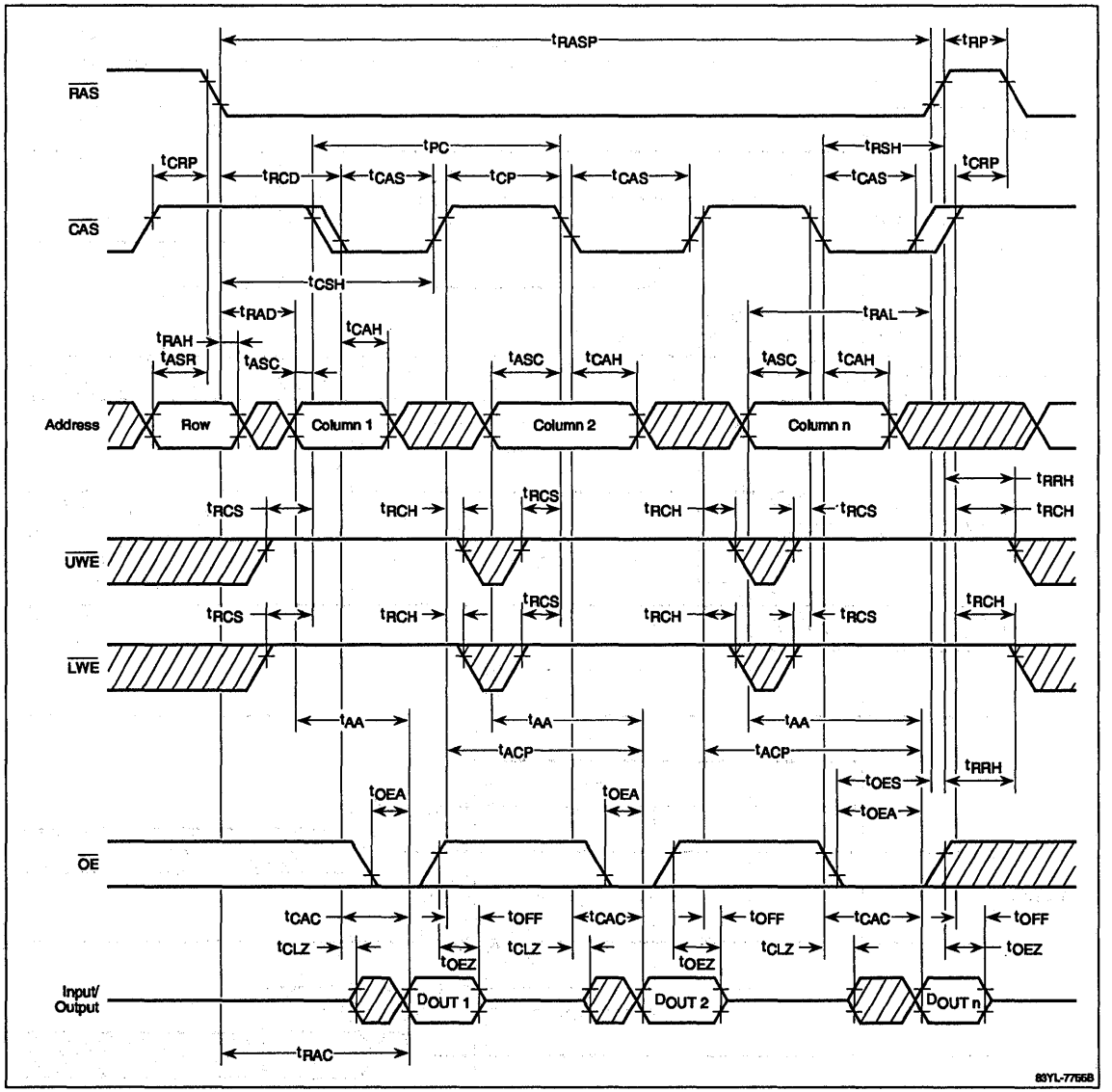
Byte Read-Modify-Write Cycle



7b

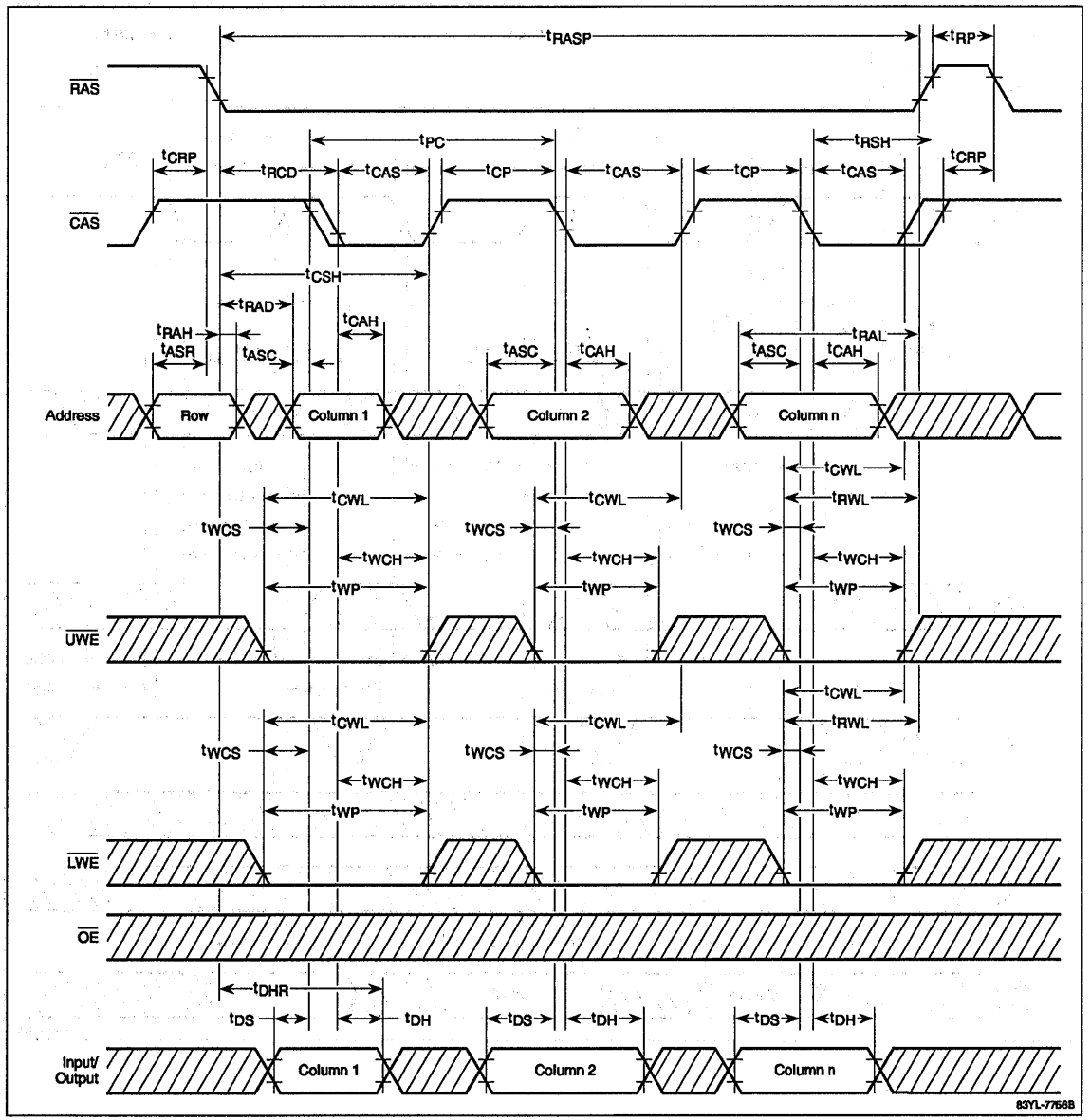
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

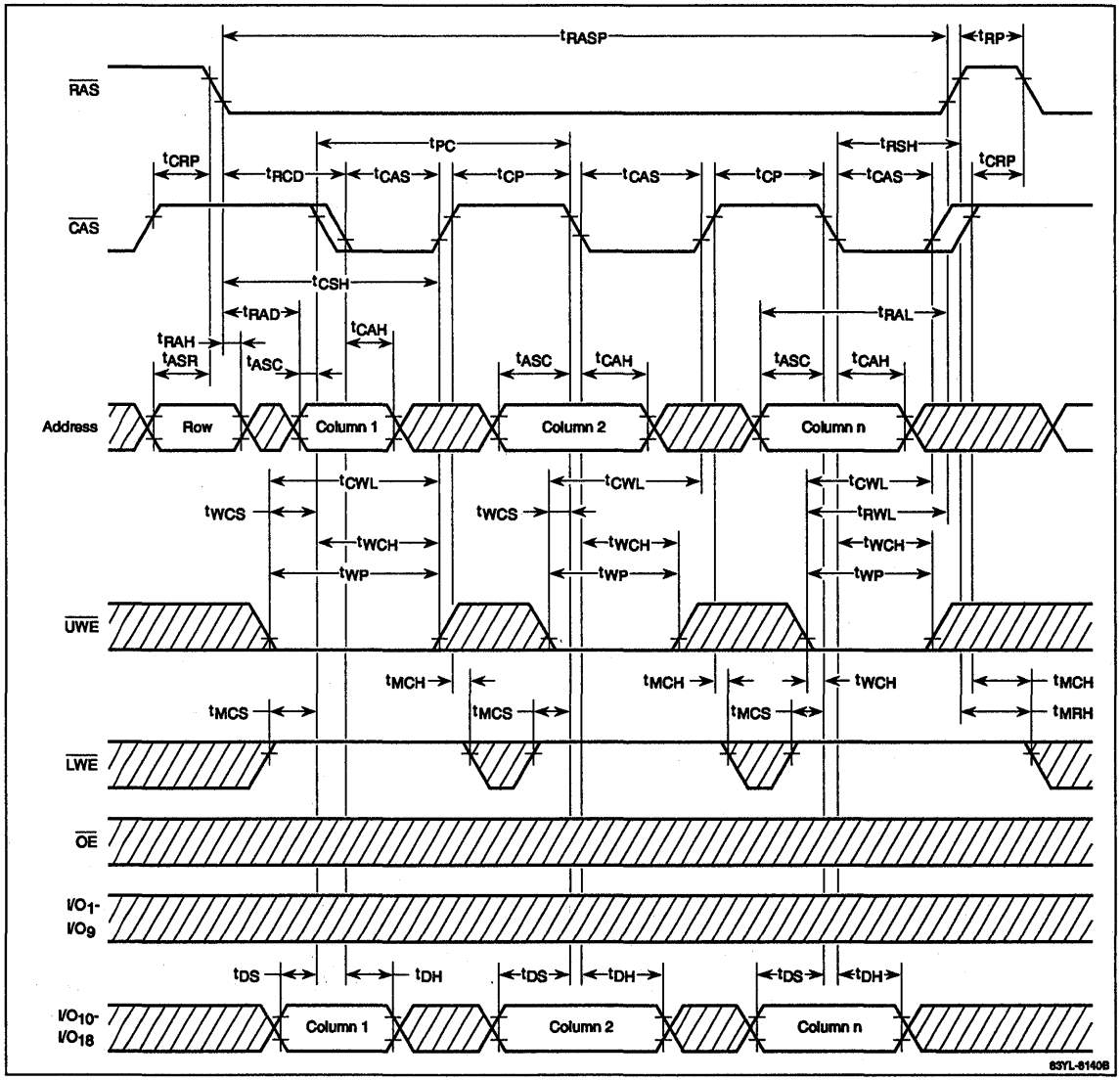
Word Fast-Page-Write Cycle



7b

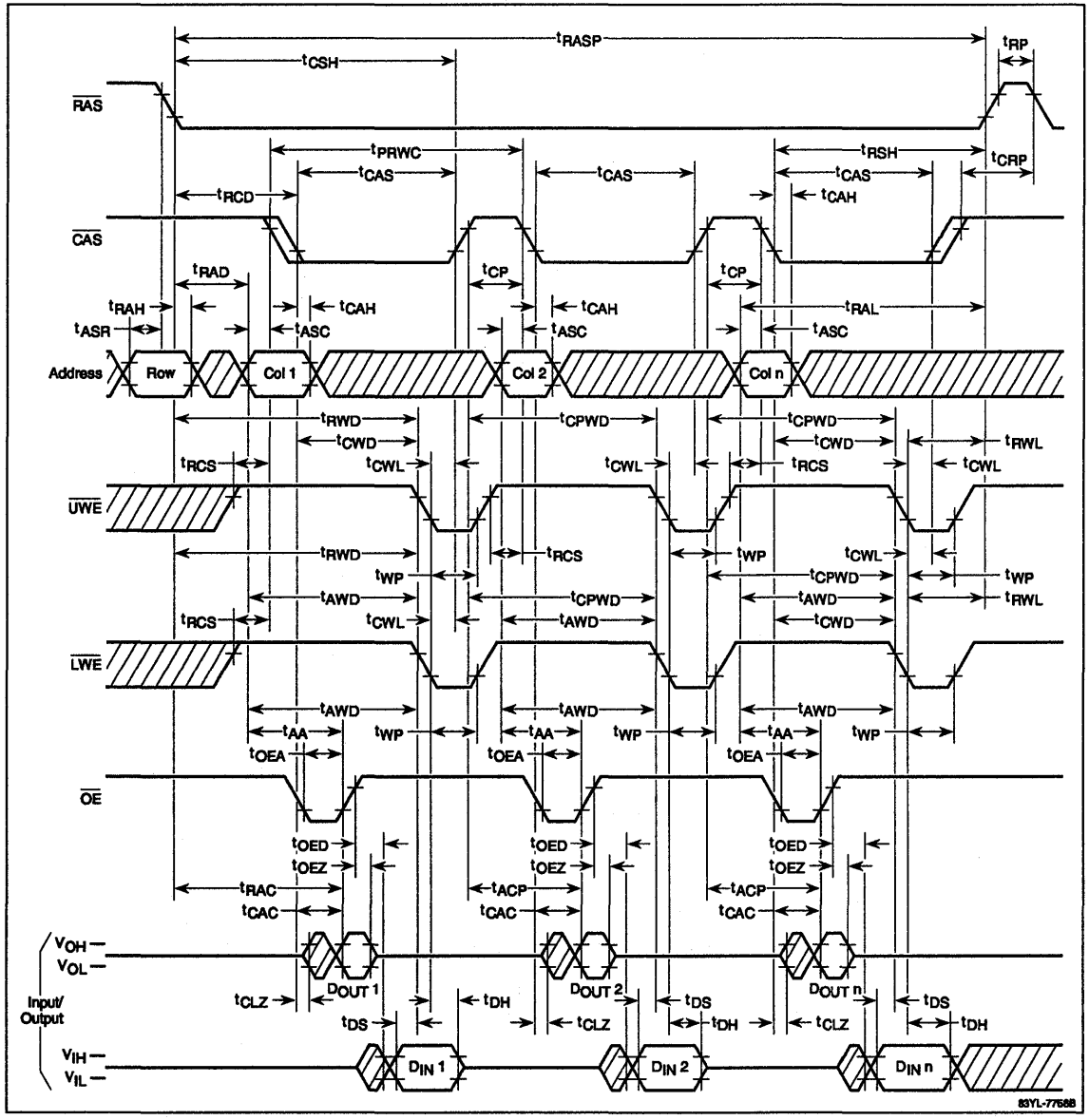
Timing Waveforms (cont)

Byte Fast-Page Write Cycle



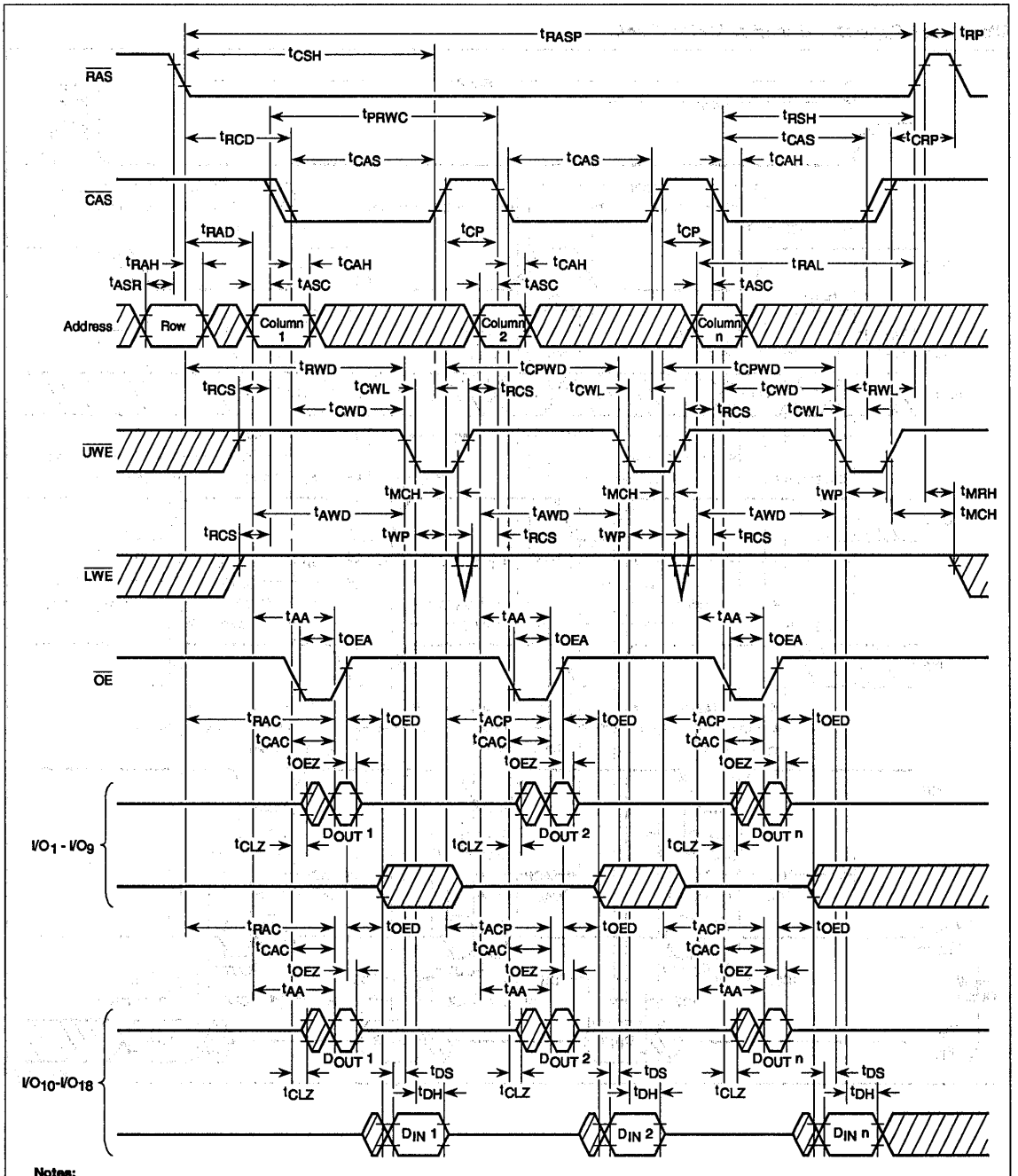
Timing Waveforms (cont)

Word Fast-Page Read-Modify-Write Cycle



7b

Byte Fast-Page Read-Modify-Write Cycle



Notes:

[1] $\overline{WE}$ = $\overline{LWE}$ or $\overline{UWE}$ for lower byte write and upper byte write cycles, respectively.

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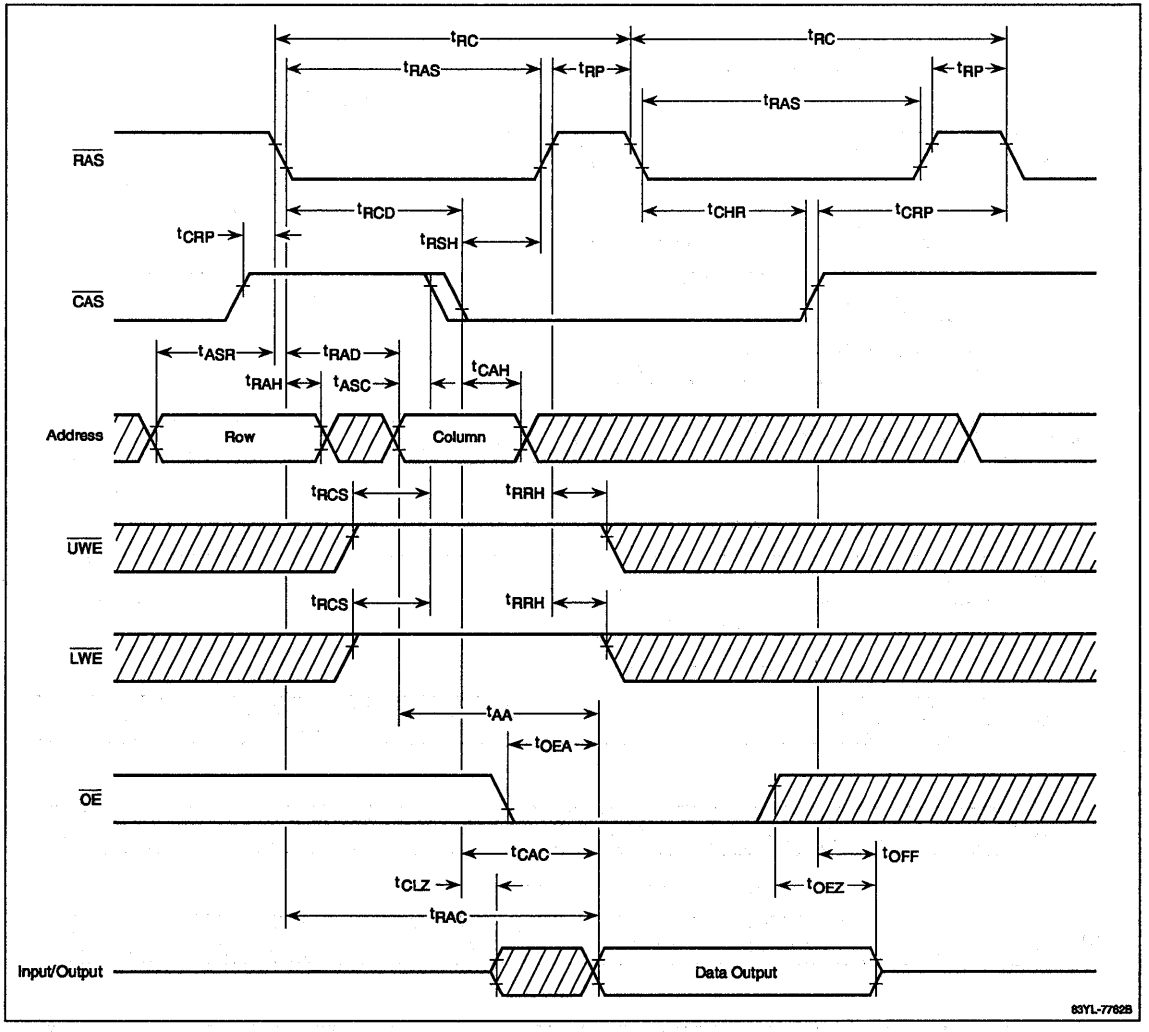
Timing Waveforms (cont)

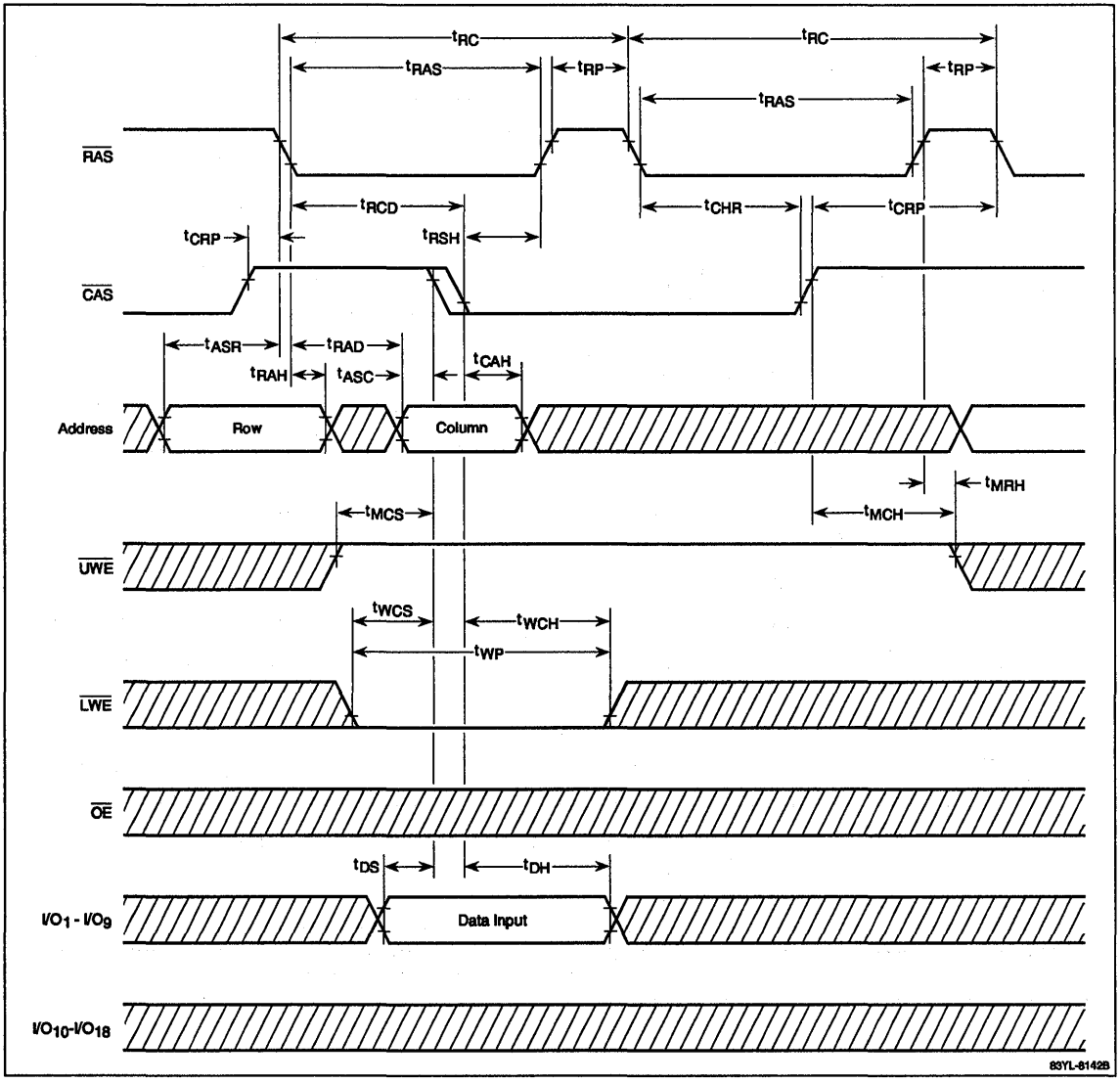
Hidden Refresh Cycle (Read Cycle)



7b

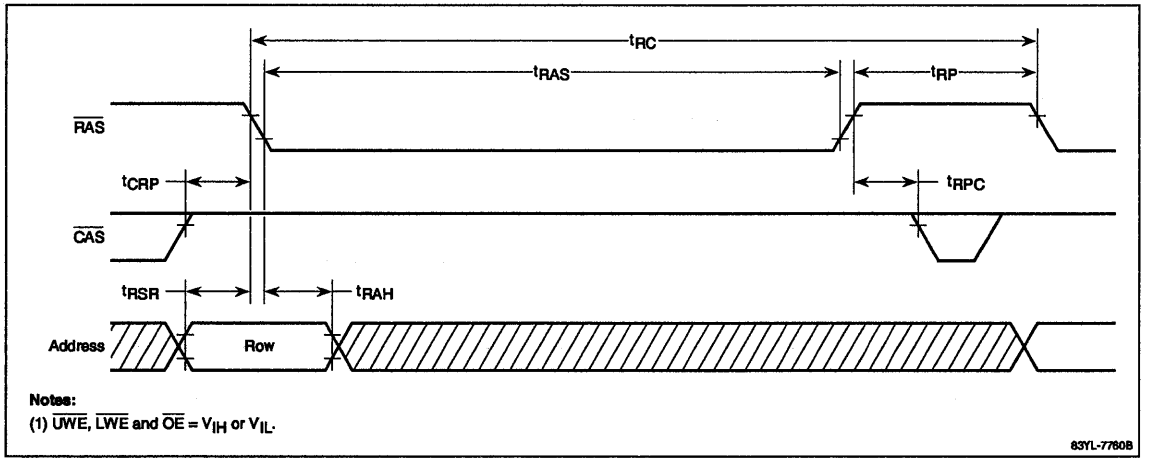
Timing Waveforms (cont)

Byte Hidden-Refresh Cycle (Write)



Timing Waveforms (cont)

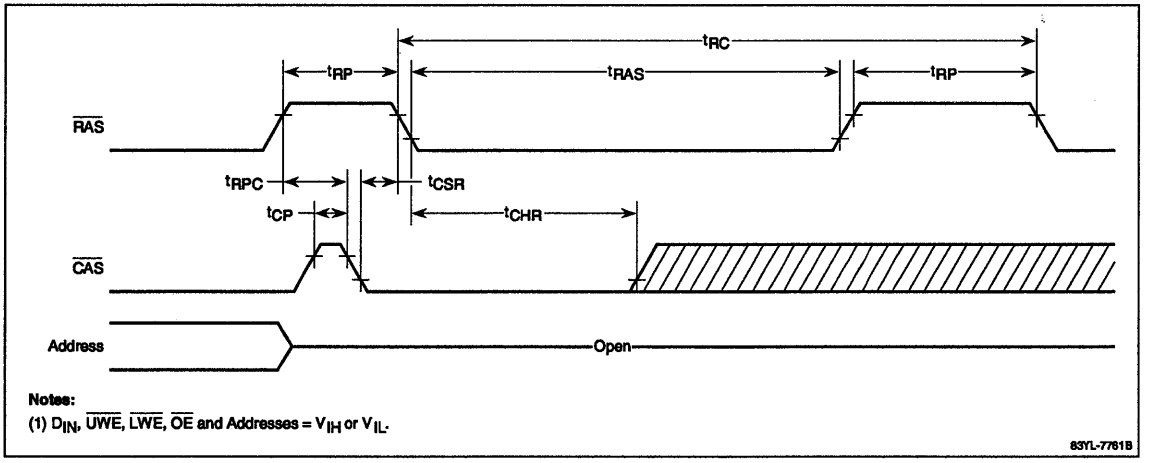
$\overline{RAS}$ Refresh Cycle



Notes:
(1) $\overline{UWE}$, $\overline{LWE}$ and $\overline{OE}$ = V_{IH} or V_{IL}.

83YL-7760B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Notes:
(1) D_{IN}, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$ and Addresses = V_{IH} or V_{IL}.

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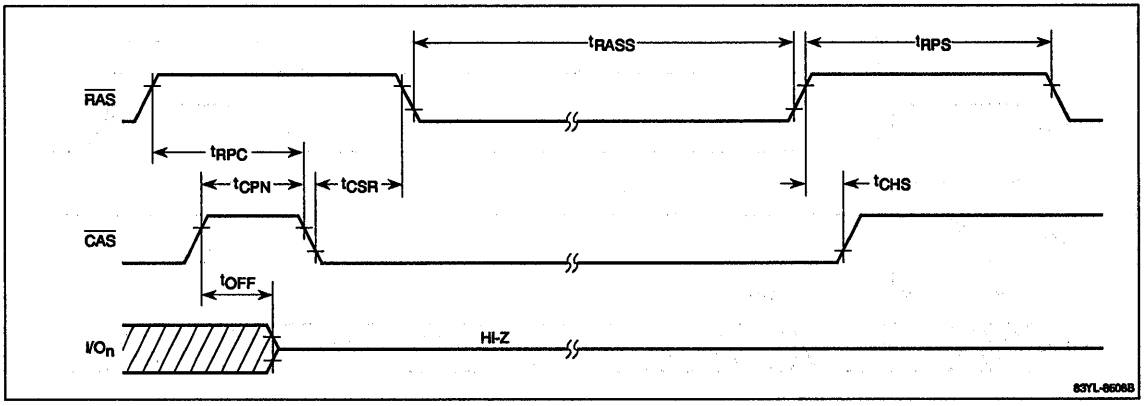
Timing Waveforms (cont)

CBR Self-Refresh Cycle



μPD424260A/L, 42S4260A/L
262,144 x 16-Bit
Dynamic CMOS RAM

Description

The μPD424260A/L and μPD42S4260A/L are fast-page dynamic RAMs organized as 262,144 words by 16 bits and designed to operate from a single power supply:

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
424260A	+5 V
424260L	+3.3 V
42S4260A	+5 V; self-refresh mode
42S4260L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{UCAS}$ and $\overline{LCAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, upper or lower byte data is held on the outputs by maintaining $\overline{UCAS}$ or $\overline{LCAS}$ low. Data outputs return to high impedance when either $\overline{UCAS}$ or $\overline{LCAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{UCAS}$ or $\overline{LCAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh address. $\overline{RAS}$-only refresh cycles will also refresh all memory locations.

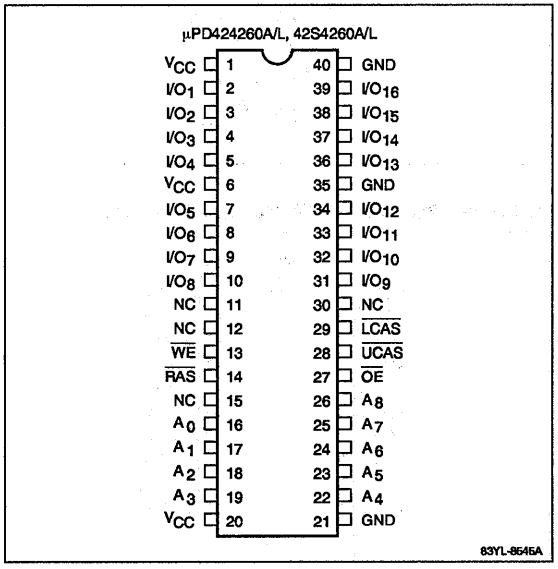
The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

- 262,144 by 16-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option
- Byte read/write control with $\overline{UCAS}$ and $\overline{LCAS}$
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 512 refresh cycles every 8 ms
- 40-pin SOJ, 40-pin ZIP, and 44/40-pin TSOP plastic packaging

Pin Configurations

40-Pin Plastic SOJ



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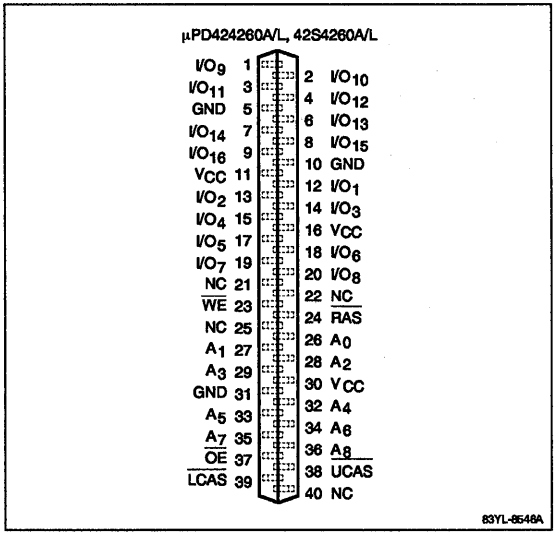
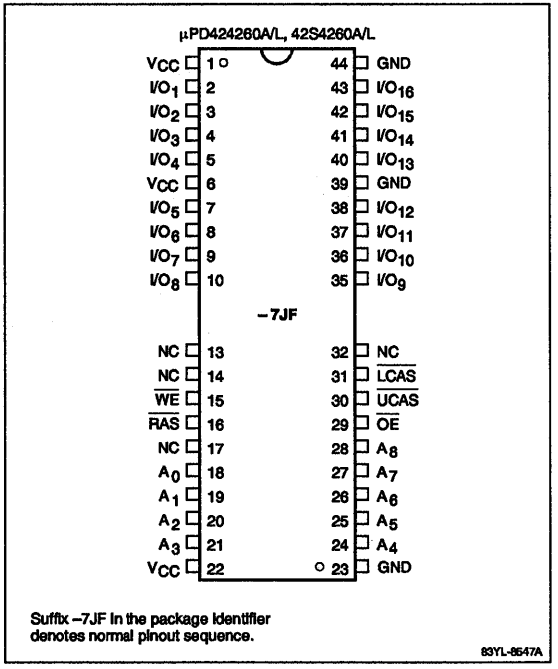
Pin Configurations (cont)

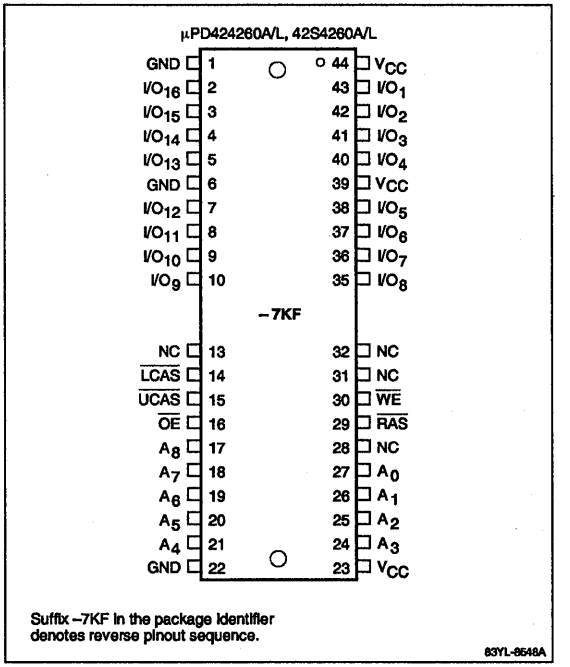
40-Pin Plastic ZIP



44/40-Pin Plastic TSOP (Normal Pinouts)



44/40-Pin Plastic TSOP (Reverse Pinouts)



Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_{16}	Data inputs and outputs
$\overline{LCAS}$, $\overline{UCAS}$	Column address strobes
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

Ordering Information, μPD424260A (+ 5-volt power)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Package
μPD424260ALE-60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD424260AV-60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-70	70 ns	45 ns		
V-80	80 ns	50 ns		
μPD424260AG5-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD424260AG5M-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD424260L (+ 3.3-volt power)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Package
μPD424260LLE-A60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD424260LV-A60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-A70	70 ns	45 ns		
V-A80	80 ns	50 ns		
μPD424260LG5-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD424260LG5M-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

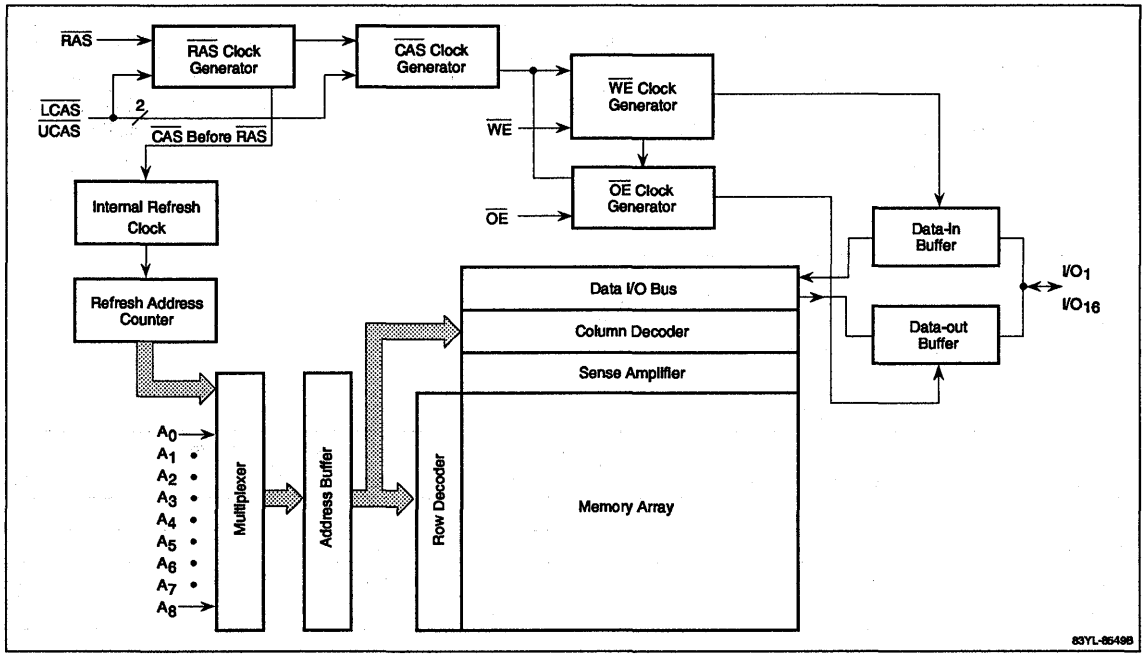
Ordering Information, μPD42S4260A (+ 5-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4260ALE-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4260AV-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic ZIP
V-70	70 ns	45 ns			
V-80	80 ns	50 ns			
μPD42S4260AG5-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns			
G5-80	80 ns	50 ns			
μPD42S4260AG5M-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns			
G5M-80	80 ns	50 ns			

Ordering Information, μPD42S4260L (+ 3.3-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4260LLE-A60	60 ns	40 ns	20 ns	100 μA	40-pin plastic SOJ
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			
μPD42S4260LV-A60	60 ns	40 ns	20 ns	100 μA	40-pin plastic ZIP
V-A70	70 ns	45 ns			
V-A80	80 ns	50 ns			
μPD42S4260LG5-A60	60 ns	40 ns	20 ns	100 μA	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns			
G5-A80	80 ns	50 ns			
μPD42S4260LG5M-A60	60 ns	40 ns	20 ns	100 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns			
G5M-A80	80 ns	50 ns			

Block Diagram



Truth Table

Function	RAS	LCAS	UCAS	WE	OE	I/O_1 - I/O_8	I/O_9 - I/O_{16}
Standby	H	X	X	X	X	High-Z	High-Z
Refresh cycle	L	H	H	X	X	High-Z	High-Z
Byte read cycle	L	L	H	H	L	Data output	High-Z
	L	H	L	H	L	High-Z	Data output
Word read cycle	L	L	L	H	L	Data output	Data output
Byte write cycle	L	L	H	L	H	Data input	—
	L	H	L	L	H	—	Data input
Word write cycle	L	L	L	L	H	Data input	Data input
——	L	L	L	H	H	High-Z	High-Z

X = don't care.

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Absolute Maximum Ratings

Voltage on any pin relative to GND	
424260A, 42S4260A	−1.0 to +7.0 V
424260L, 42S4260L	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
424260A, 42S4260A	50 mA
424260L, 42S4260L	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_{16}

Recommended Operating Conditions

		424260A, 42S4260A			424260L, 42S4260L			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.5		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

Self-Refresh Current

T_A = 0 to +70°C; V_{CC} = +5 V ±10% (42S4260A) or +3.3 V ±0.3 V (42S4260L)

Symbol	42S4260A	42S4260L	Conditions
I_{CC7}	300 μA max	100 μA max	I/O pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. Other input pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. $t_{RAS} \geq 100$ μs

DC Characteristics; μPD424260A, 42S4260A

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				300	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

DC Characteristics; μPD424260L, 42S4260L

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			500	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				100	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–5		5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–5		5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

AC Characteristics

T_A = 0 to +70°C

μPD424260A, 42S4260A: V_{CC} = +5.0 V ±10%

μPD424260L, 42S4260L: V_{CC} = +3.3 V ±0.3 V

		-60		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5)		140		130		120	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
	I_{CC1} (+3.3)		130		120		110		
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5)		140		130		120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
	I_{CC3} (+3.3)		130		120		110		
Operating current, fast-page cycle, average	I_{CC4} (+5)		90		80		70	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
	I_{CC4} (+3.3)		90		80		70		
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5)		140		130		120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
	I_{CC5} (+3.3)		130		120		110		
Access time from column address	t_{AA}		30		35		40	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		ns	(Note 15)
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	–35		–40		–50		ns	For 42S4260A/L only

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AC Characteristics (cont)

Parameter	Symbol	-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	(Notes 4, 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		75		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		50		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Notes 13, 16)
Data-in setup time	t_{DS}	0		0		0		ns	(Notes 13, 16)
Masked write hold time referenced to $\overline{RAS}$	t_{MRH}	0		0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	(Note 9)
Output disable from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t_{PC}	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with exended data output	t_{PRWC}	85		90		100		ns	(Note 6)

AC Characteristics (cont)

		-60		-70		-80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		10		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		μs	For 42S4260A/L
Random read or write cycle time	t_{RC}	120		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	120		130		150		ns	For 42S4260A/L
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Read-modify-write cycle time	t_{RWC}	165		175		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Rise and fall times	t_T	3	50	3	50	3	50	ns	(Note 4)

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Write command hold time	t_{WCH}	15		15		15		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		ns	(Note 14)
Write command pulse width	t_{WP}	15		15		15		ns	(Note 12)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF. For 3.3-volt devices, V_{OH} = 2.0 V, V_{OL} = 0.8 V.

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max); if $t_{RAD} \geq t_{RAD}$ (max) access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of one of the $\overline{CAS}$ signals for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD} and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

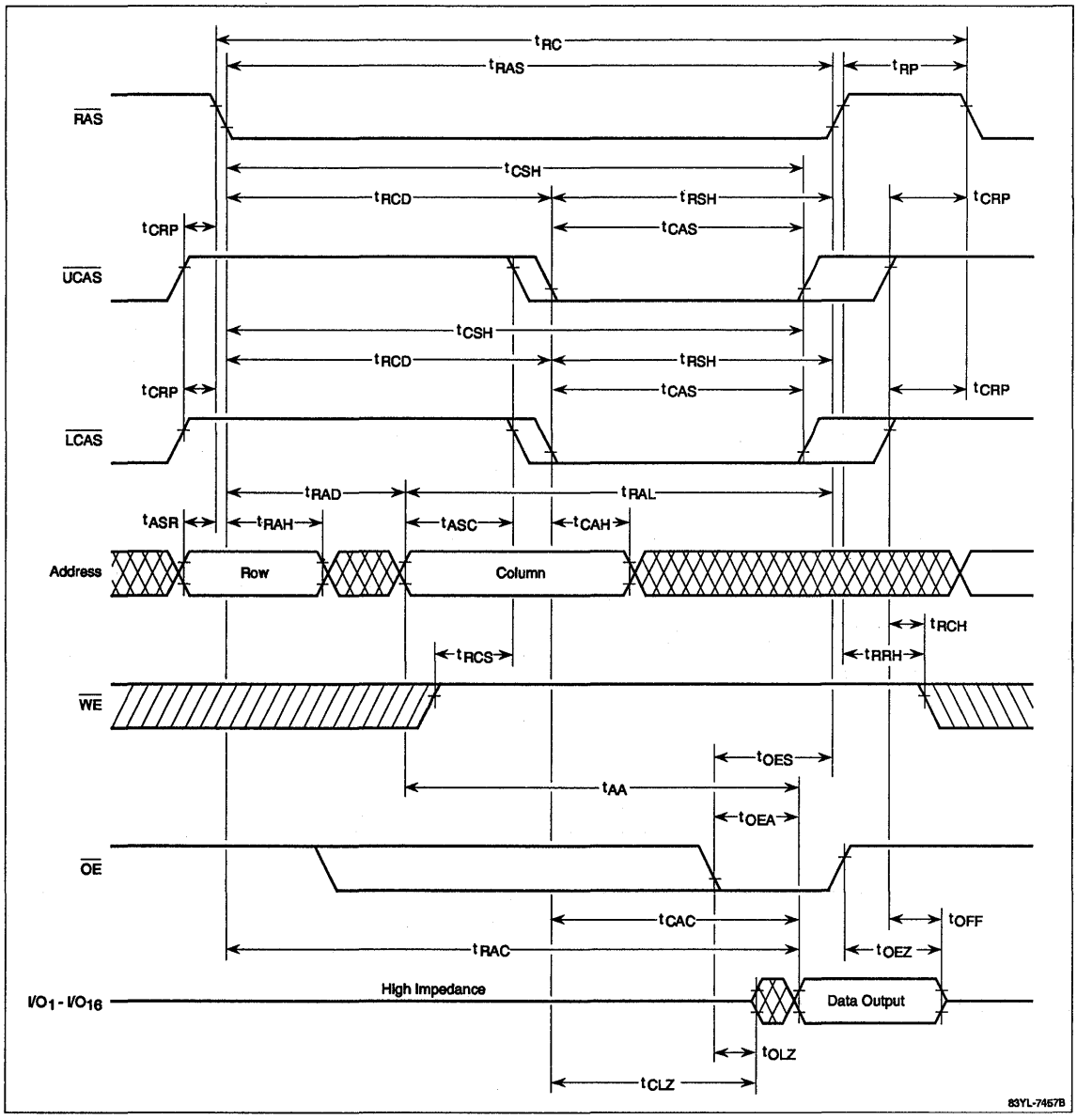
(15) Holding $\overline{LCAS}$ or $\overline{UCAS}$ low prior to $\overline{RAS}$ going negative will initiate a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (t_{CSR} and t_{CHR} must be satisfied).

(16) The first $\overline{WE}$ falling edge is used as a reference for the setup and hold requirements of t_{ASC}, t_{CAH}, t_{DS}, and t_{DH} (early write cycle).

(17) The first $\overline{CAS}$ falling edge is used as a reference for the start of t_{ACP} ($\overline{CAS}$ precharge access time).

Timing Waveforms

Word Read Cycle



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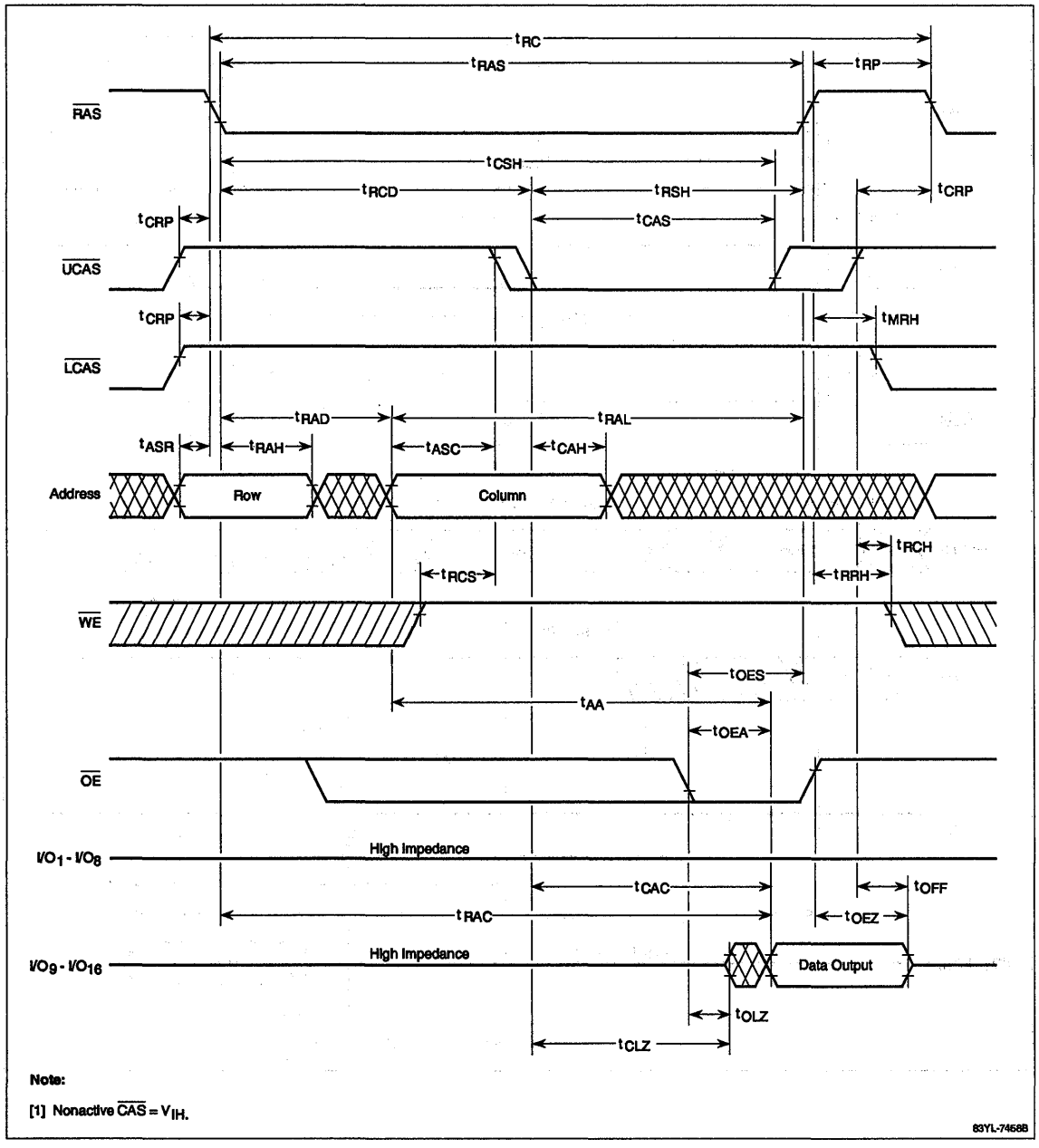
Timing Waveforms (cont)

Byte Read Cycle



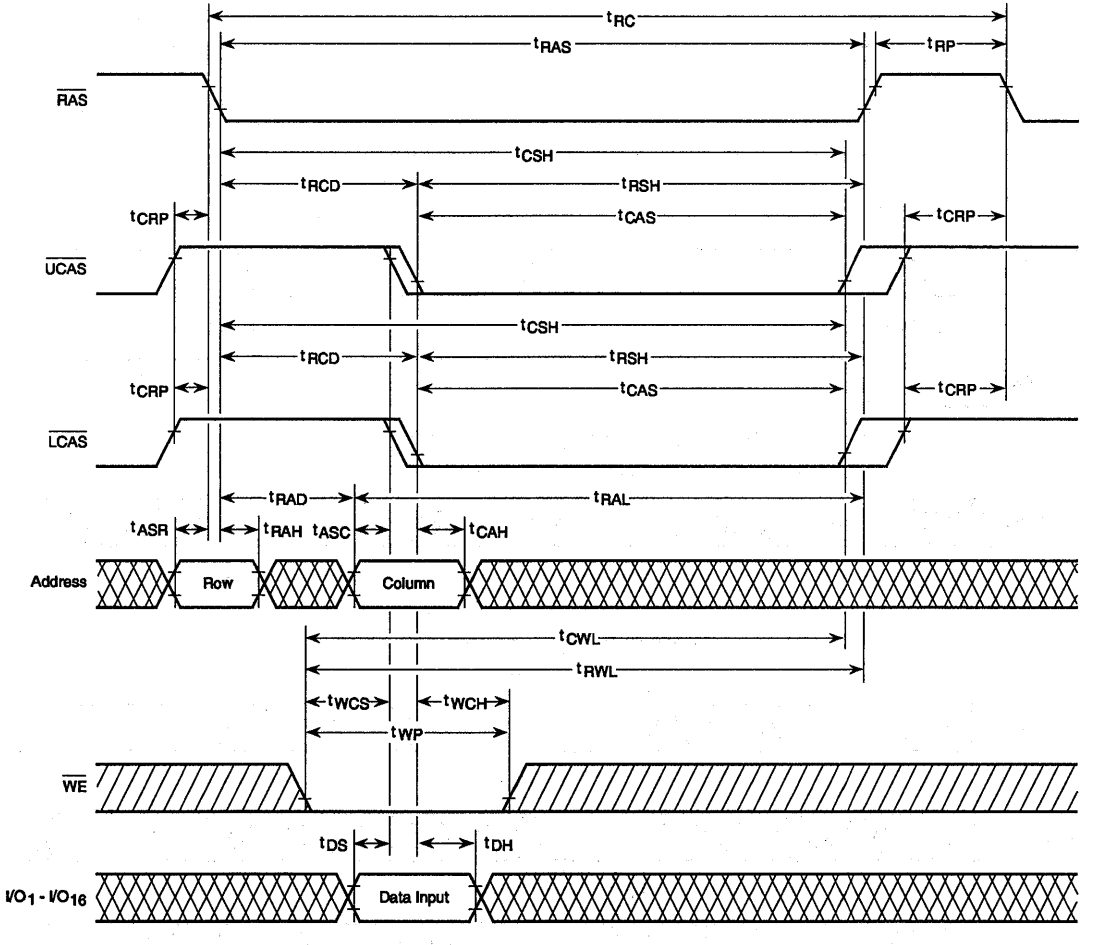
Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-7456B

Timing Waveforms (cont)

Word Early-Write Cycle



Note:

[1] $\overline{OE}$ = don't care.

83YL-7667B

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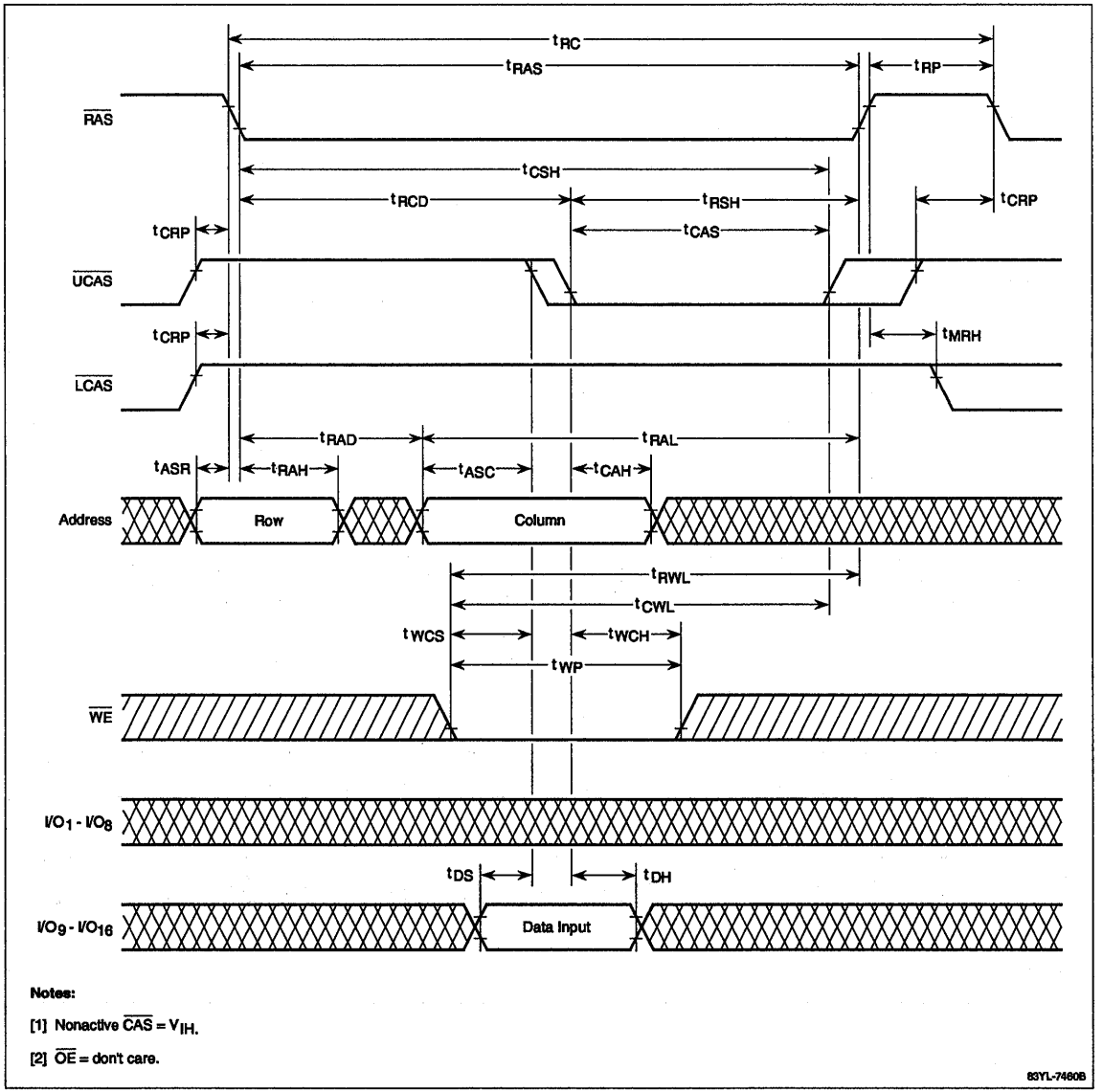
Timing Waveforms (cont)

Byte Early-Write Cycle



Notes:

[1] Nonactive $\overline{CAS}$ = V_{IH}.

[2] $\overline{OE}$ = don't care.

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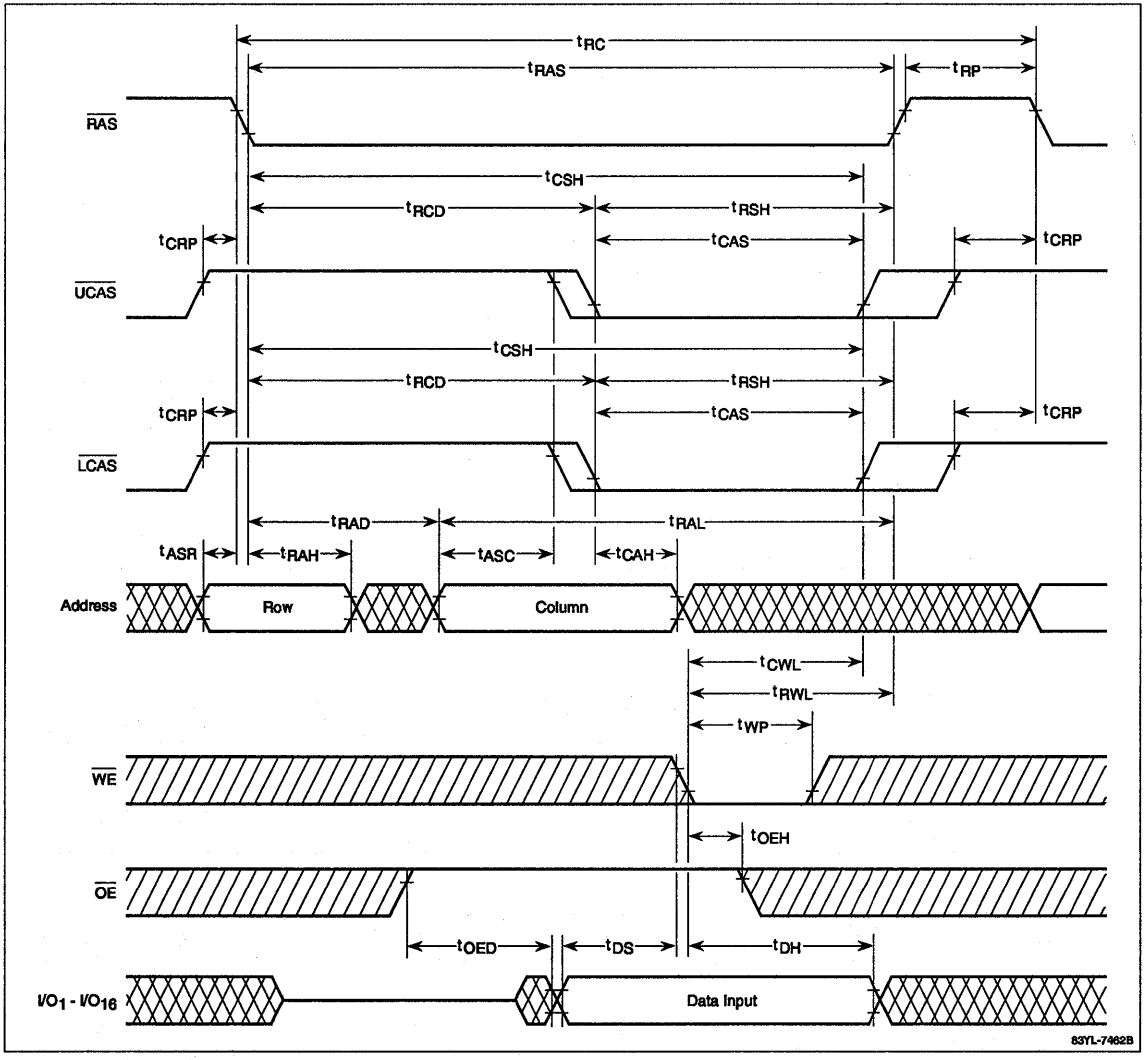
Timing Waveforms (cont)

Word Late-Write Cycle



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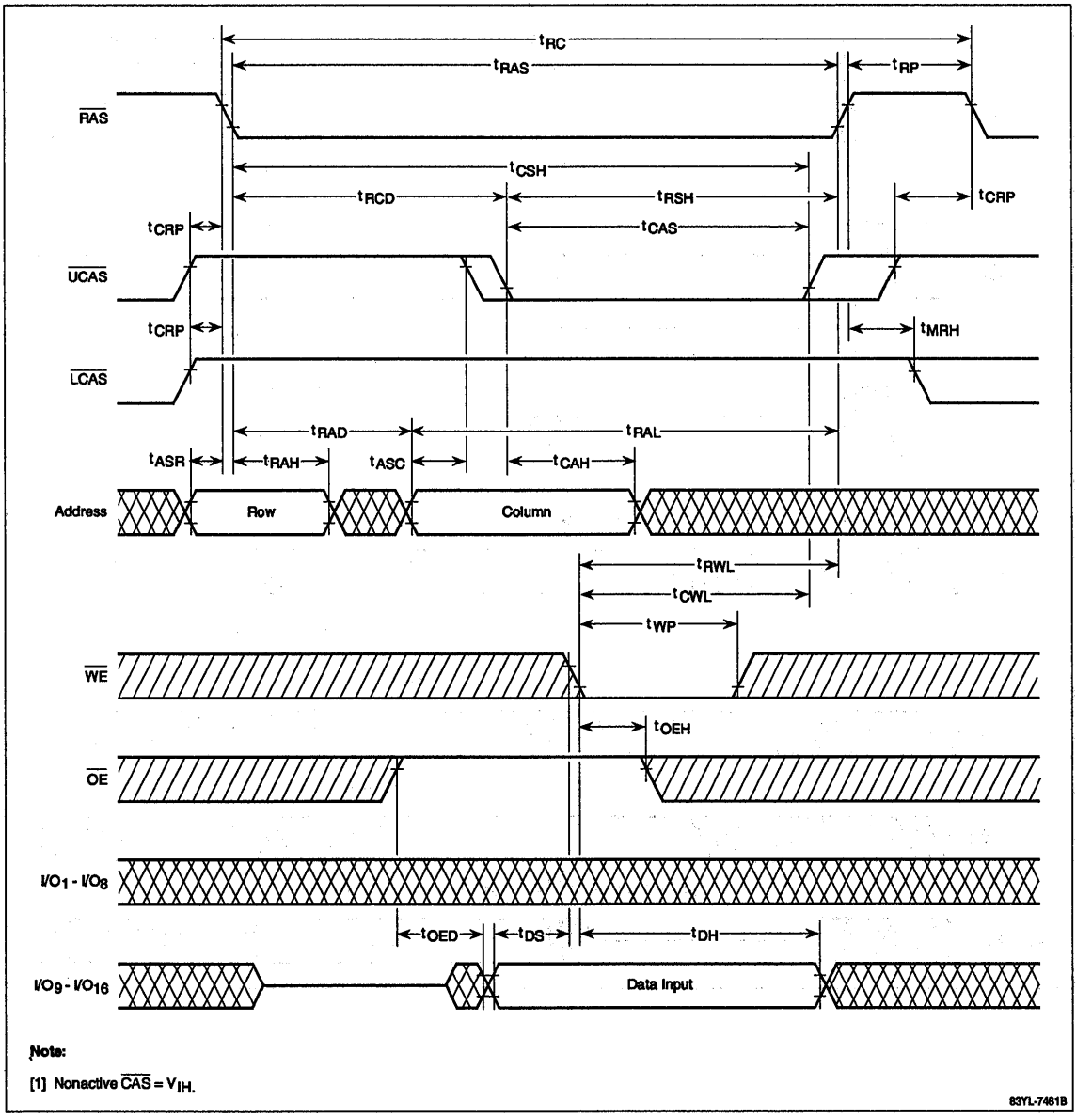
Timing Waveforms (cont)

Byte Late-Write Cycle



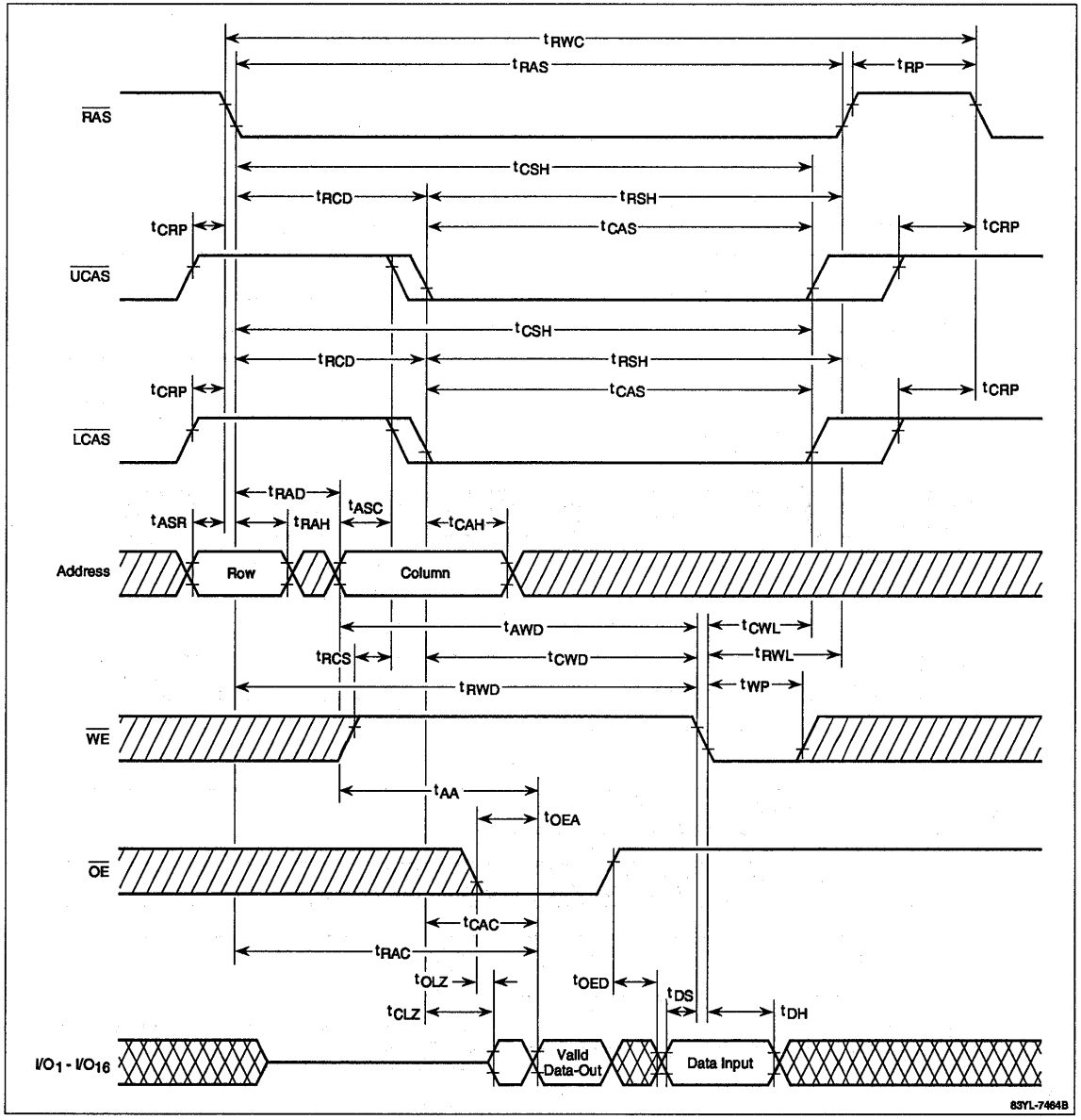
Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-7461B

Timing Waveforms (cont)

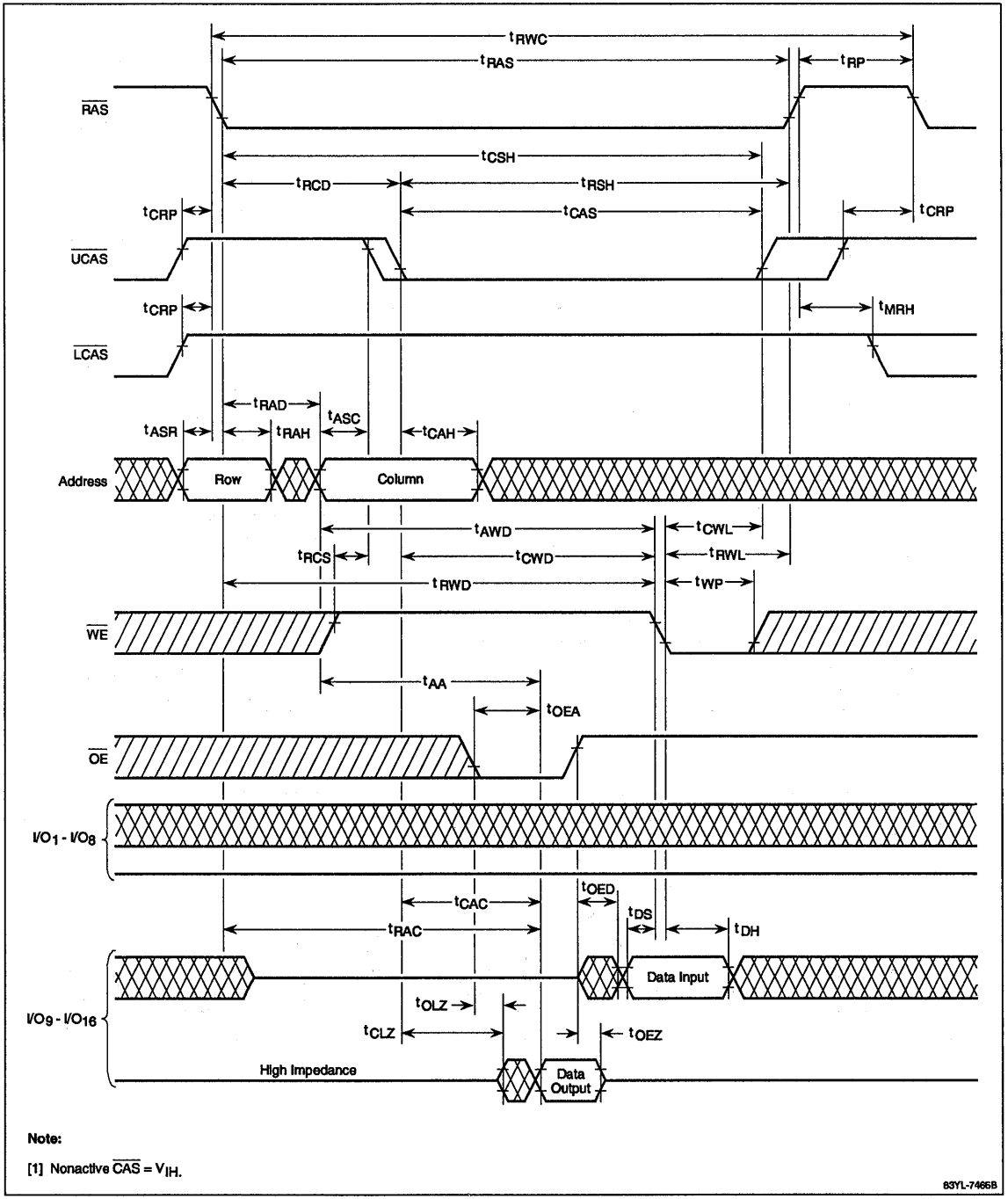
Word Read-Modify-Write Cycle



7c

Timing Waveforms (cont)

Byte Read-Modify-Write Cycle



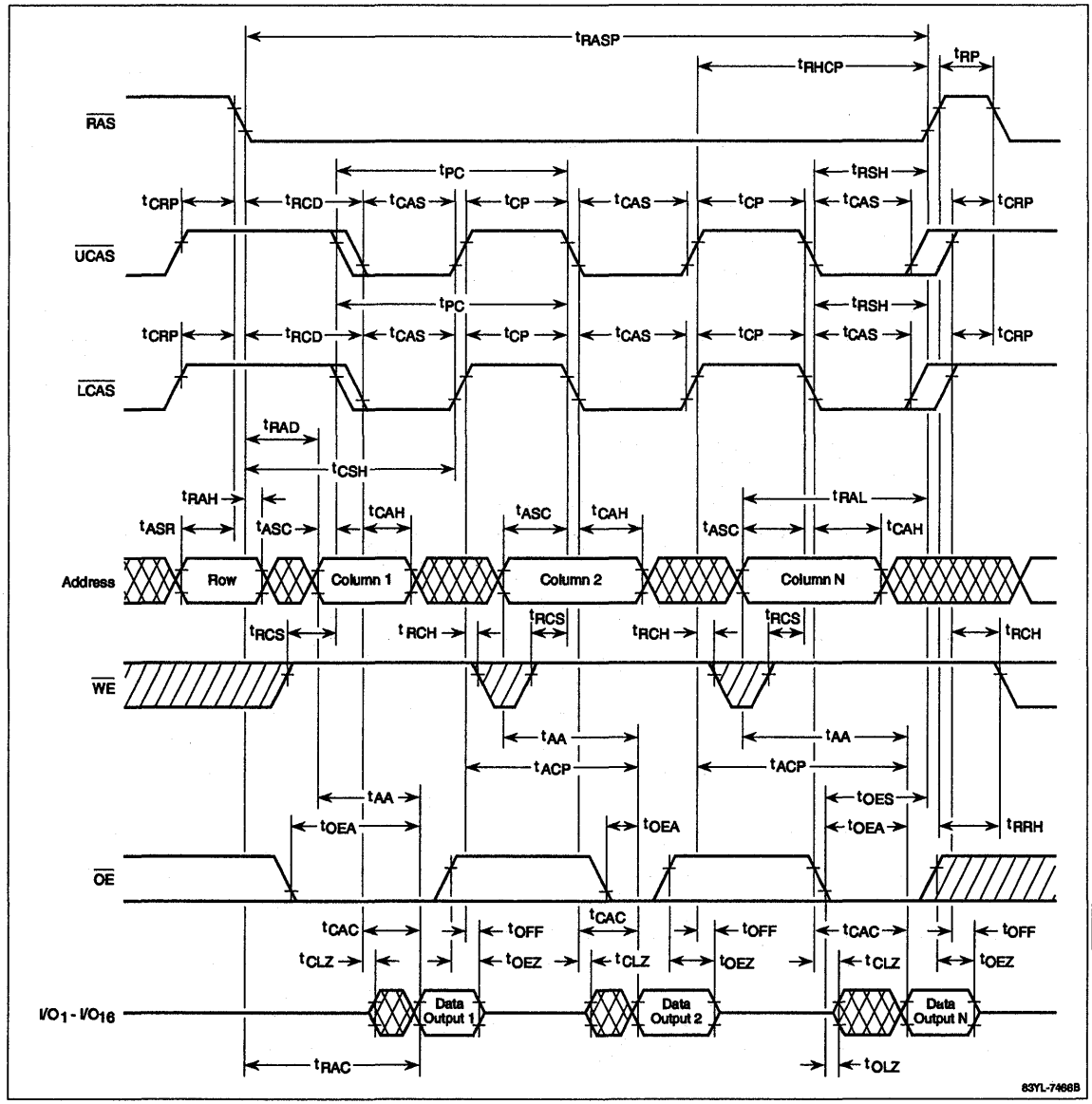
Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-7466B

Timing Waveforms (cont)

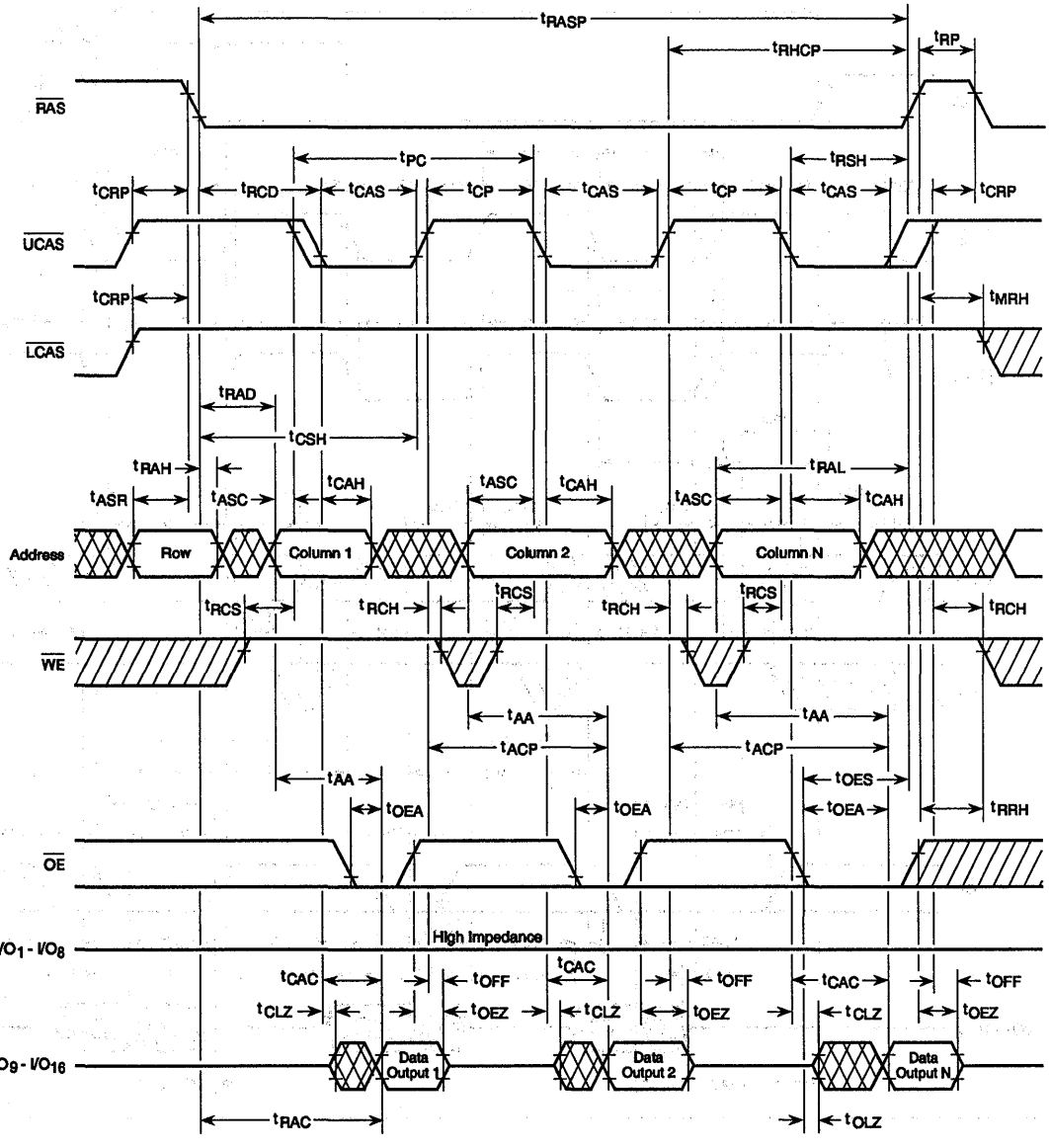
Word Fast-Page Read Cycle



7c

Timing Waveforms (cont)

Byte Fast-Page Read Cycle



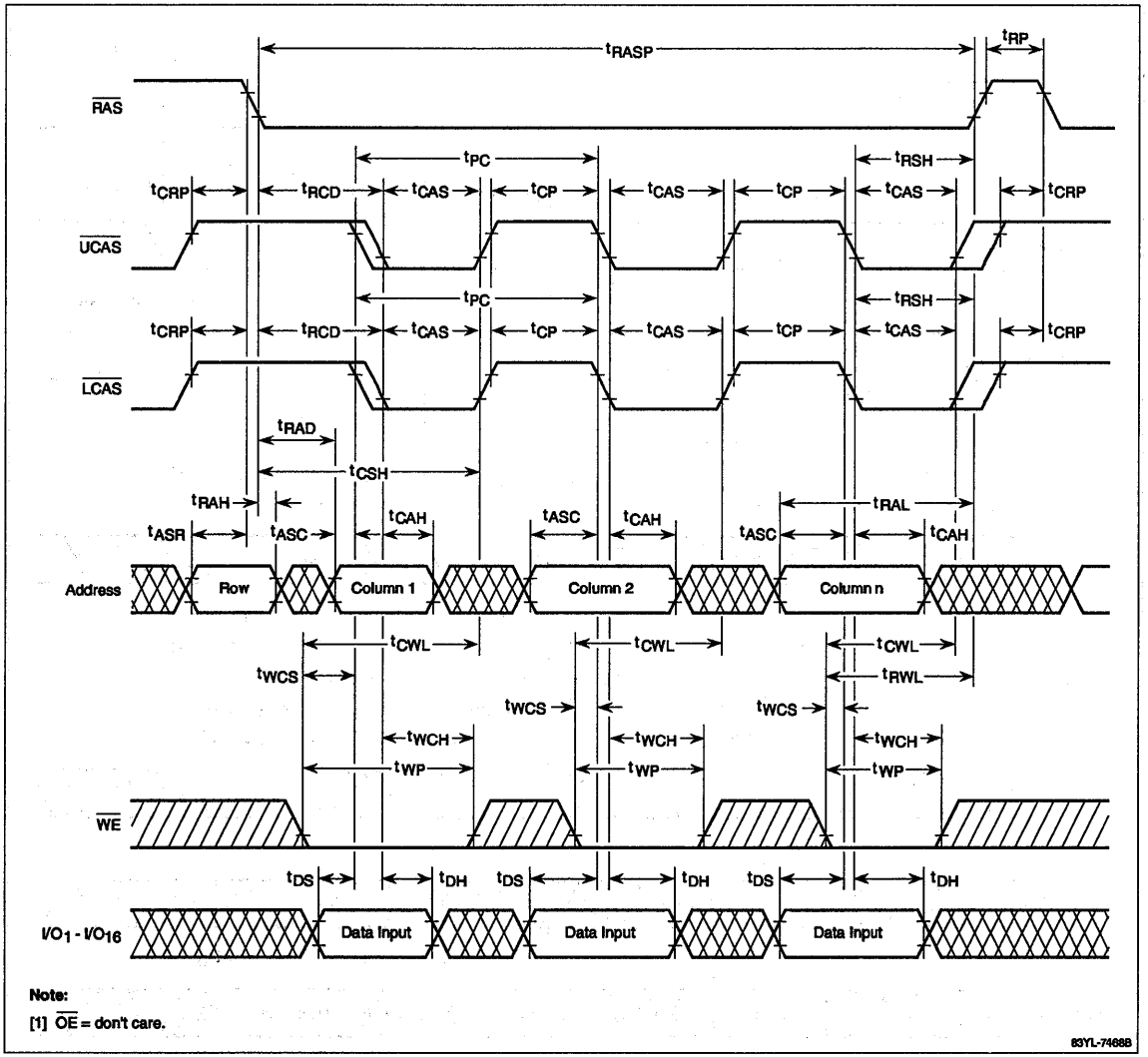
Note:

[1] Nonactive $\overline{CAS}$ = V_{IH}.

83YL-7467B

Timing Waveforms (cont)

Word Fast-Page Early-Write Cycle



Note:

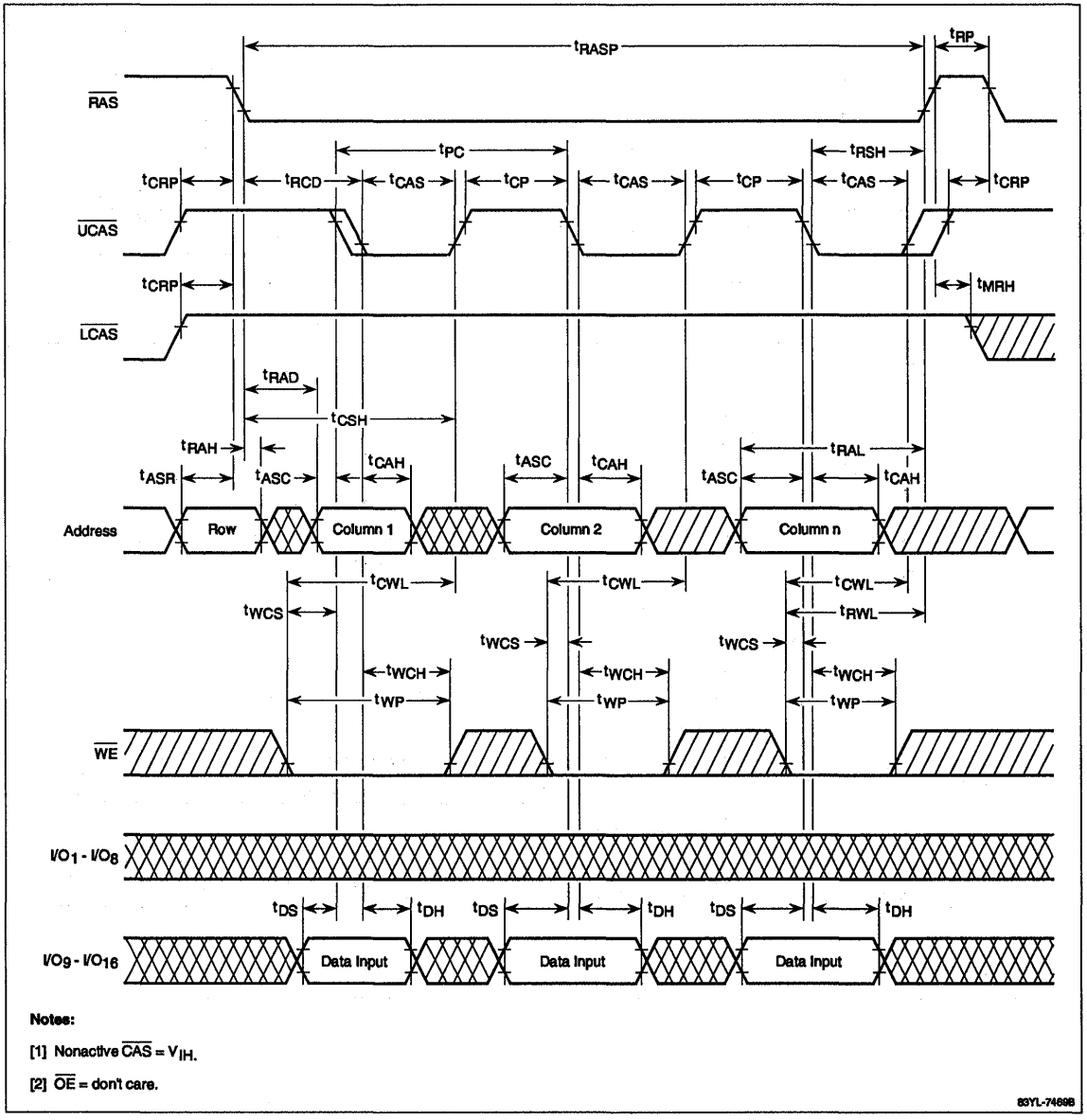
[1] $\overline{OE}$ = don't care.

83YL-7468B

7c

Timing Waveforms (cont)

Byte Fast-Page Early-Write Cycle



Notes:

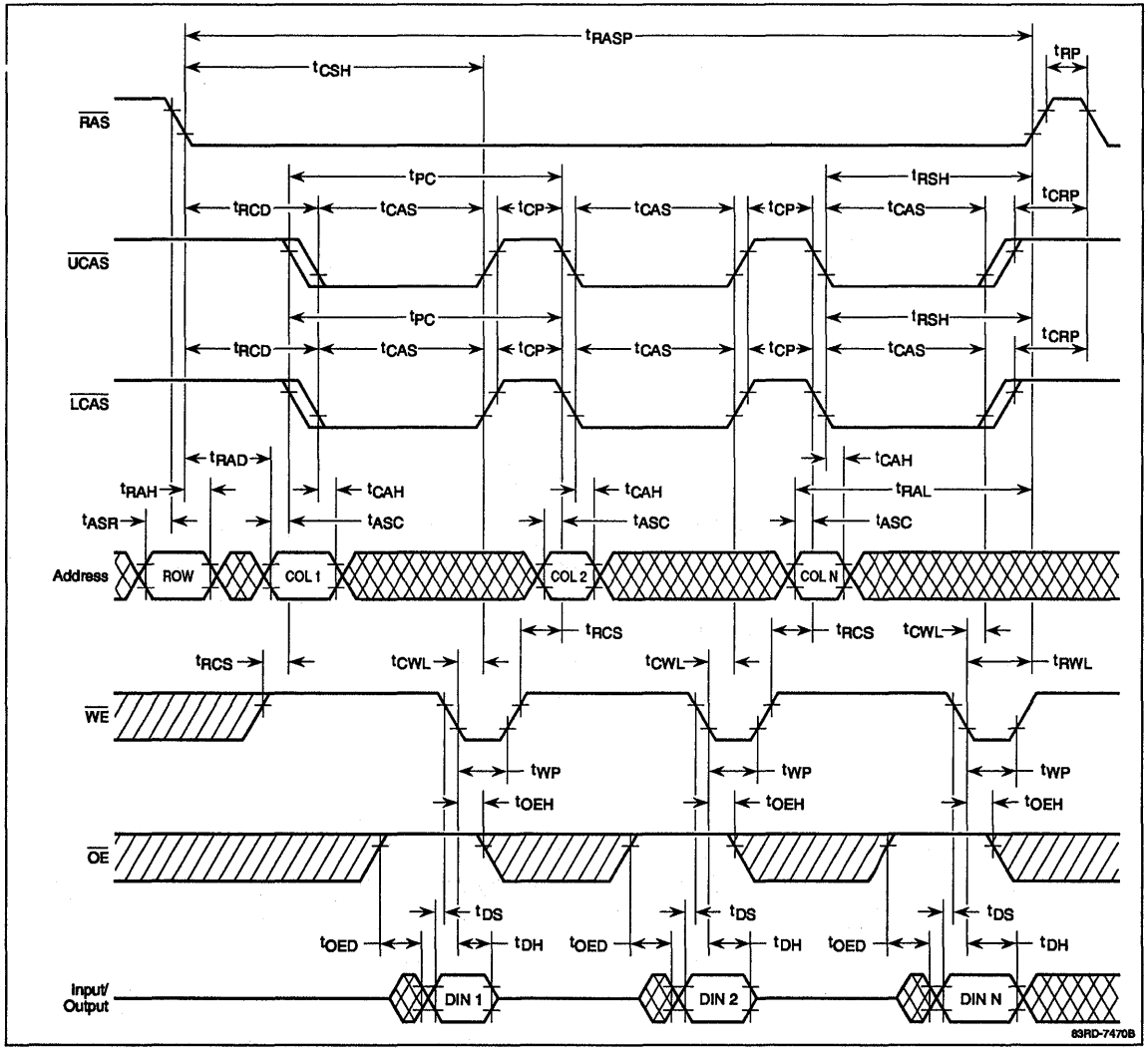
[1] Nonactive $\overline{CAS}$ = V_{IH}.

[2] $\overline{OE}$ = don't care.

83YL-74698

Timing Waveforms (cont)

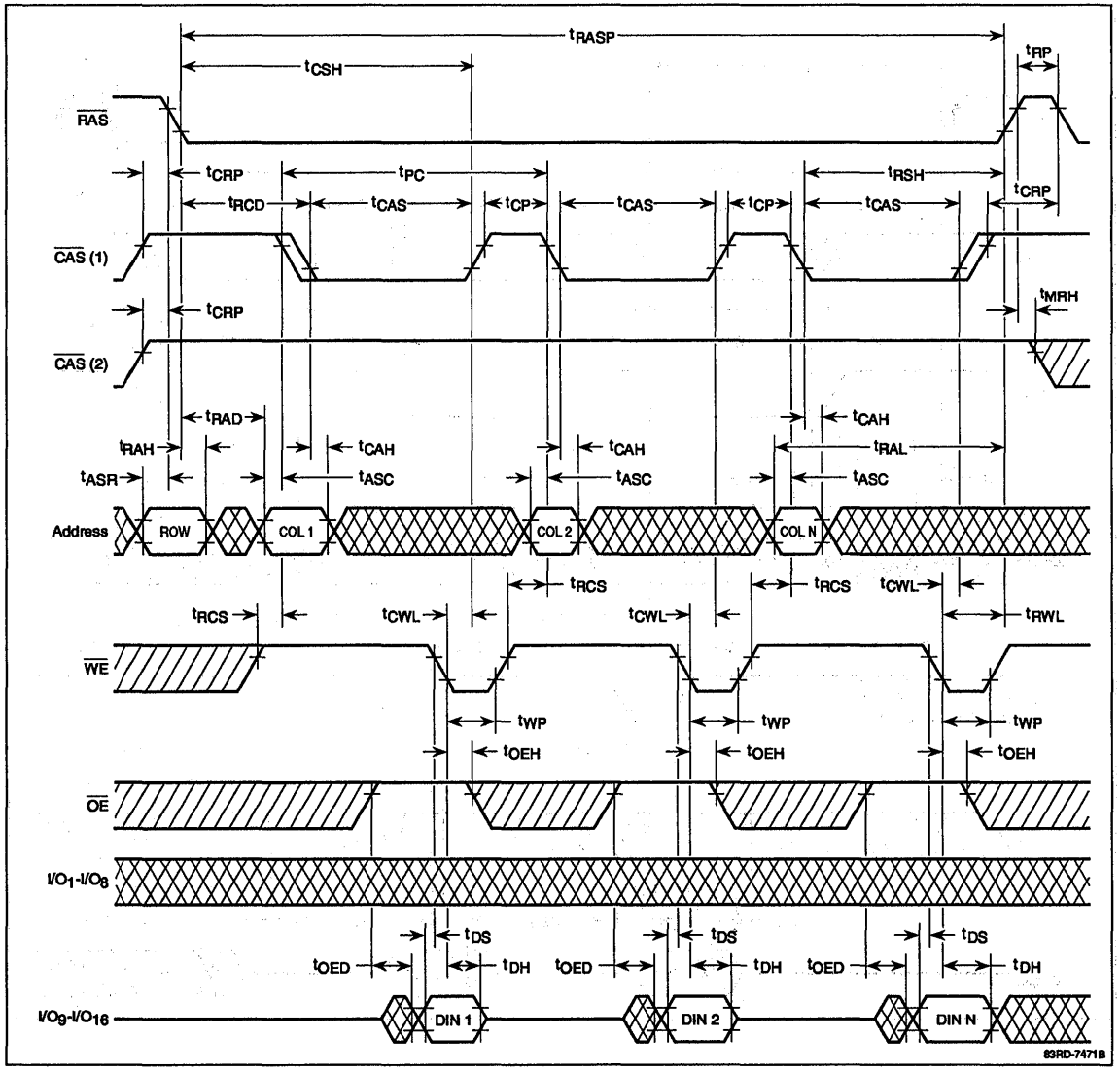
Word Fast-Page Late-Write Cycle



7c

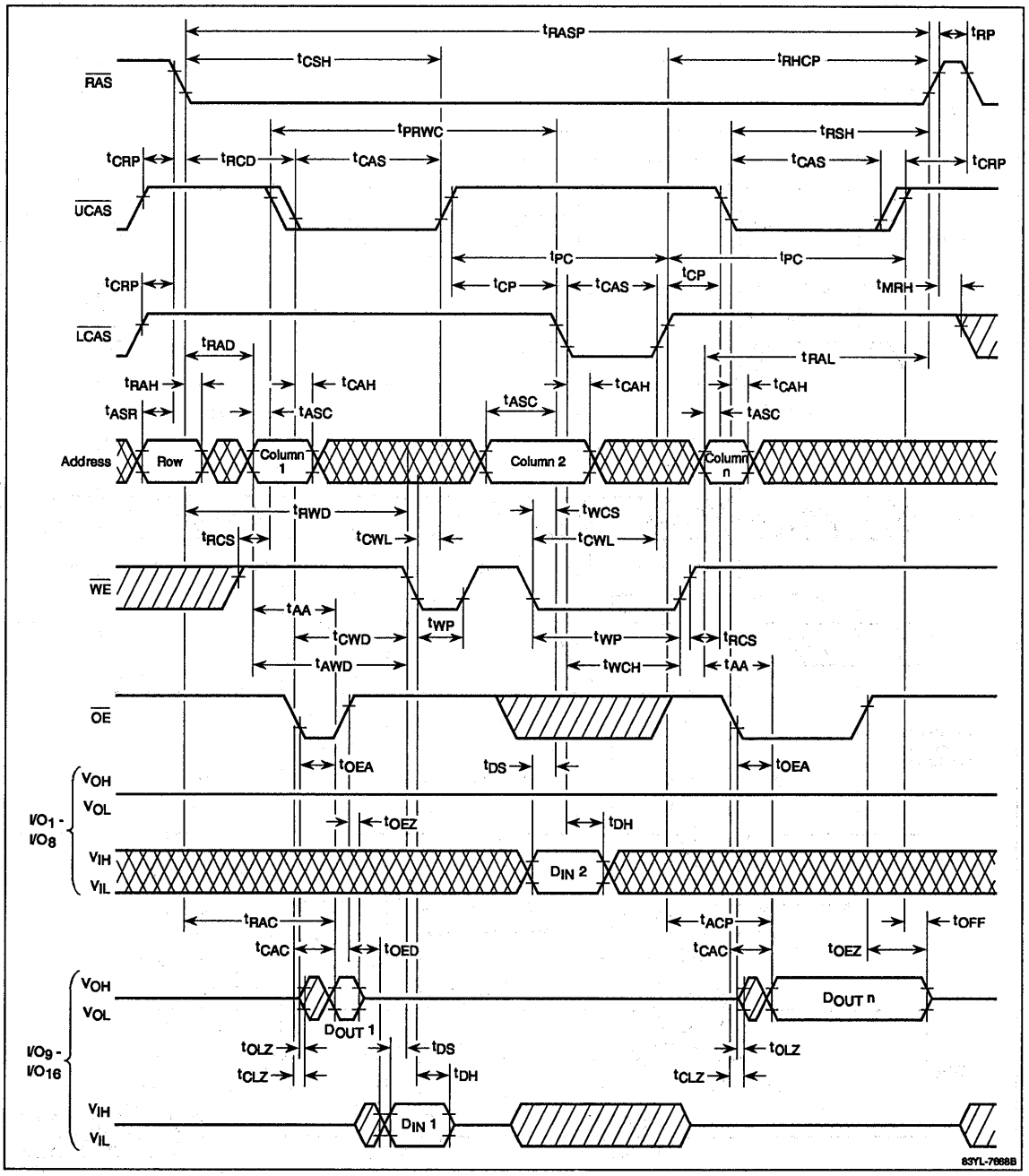
Timing Waveforms (cont)

Byte Fast-Page Late-Write Cycle



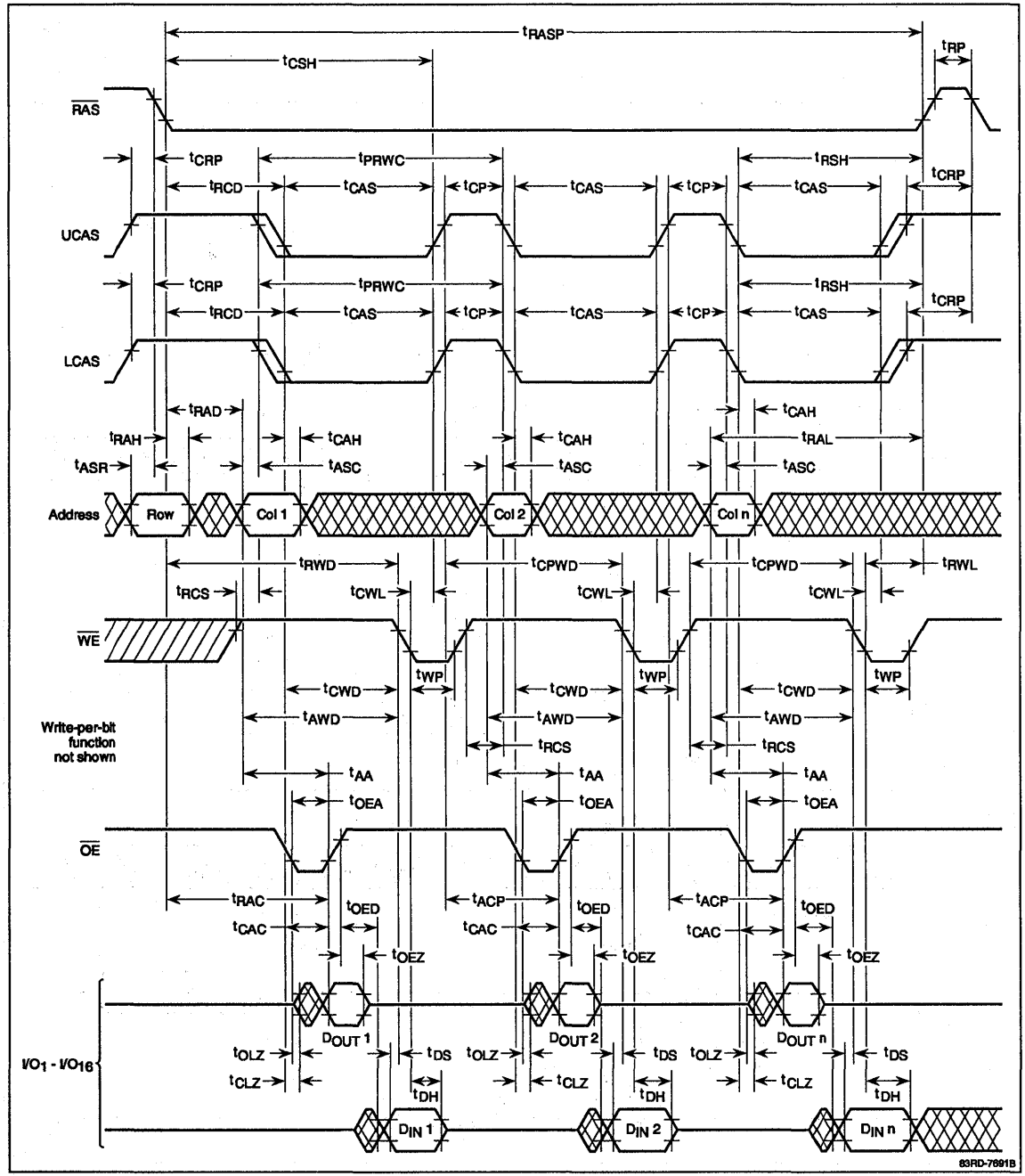
Timing Waveforms (cont)

Byte Fast-Page Read/Write Cycle



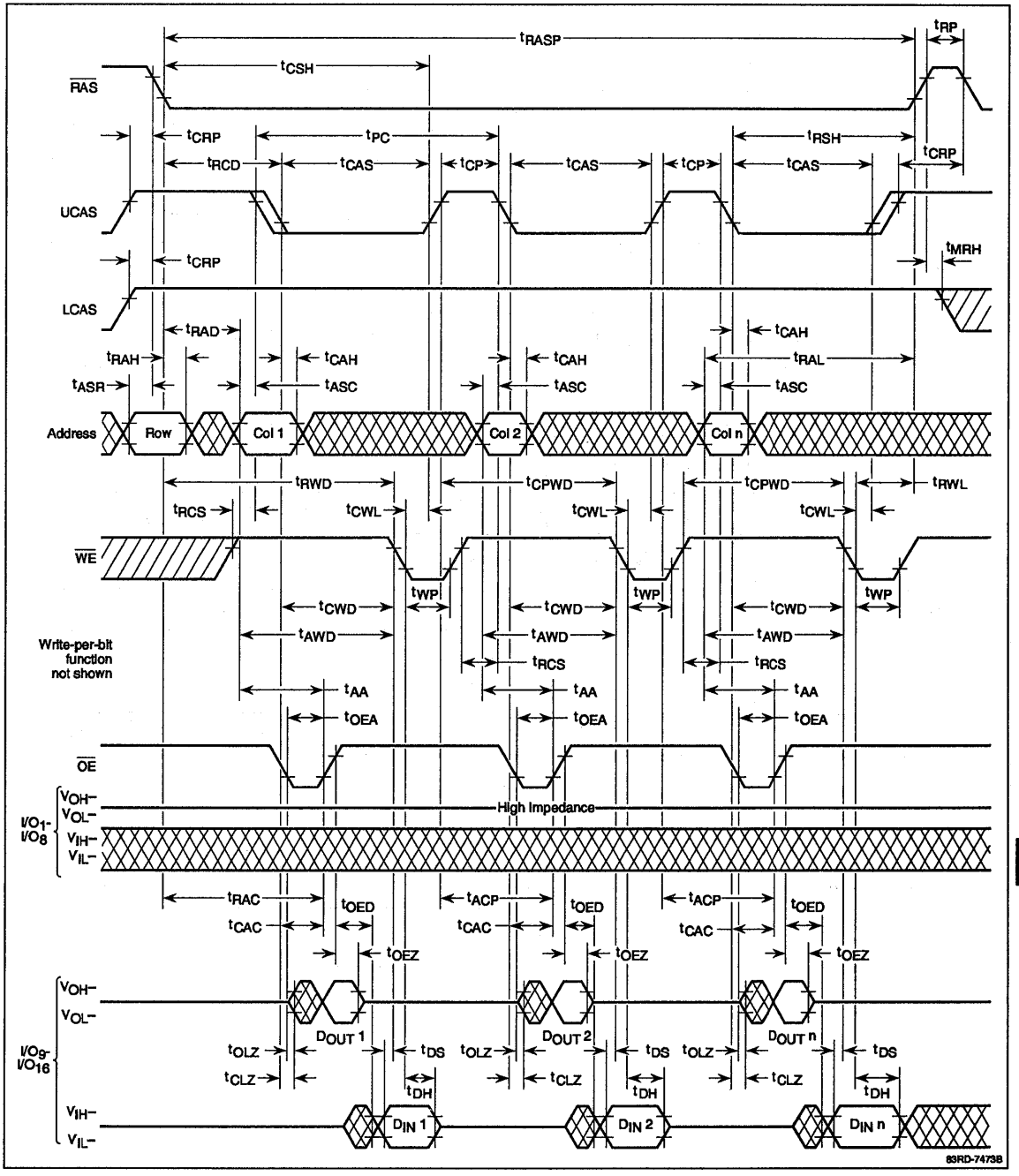
Timing Waveforms (cont)

Word Fast-Page Read-Modify-Write Cycle



Timing Waveforms (cont)

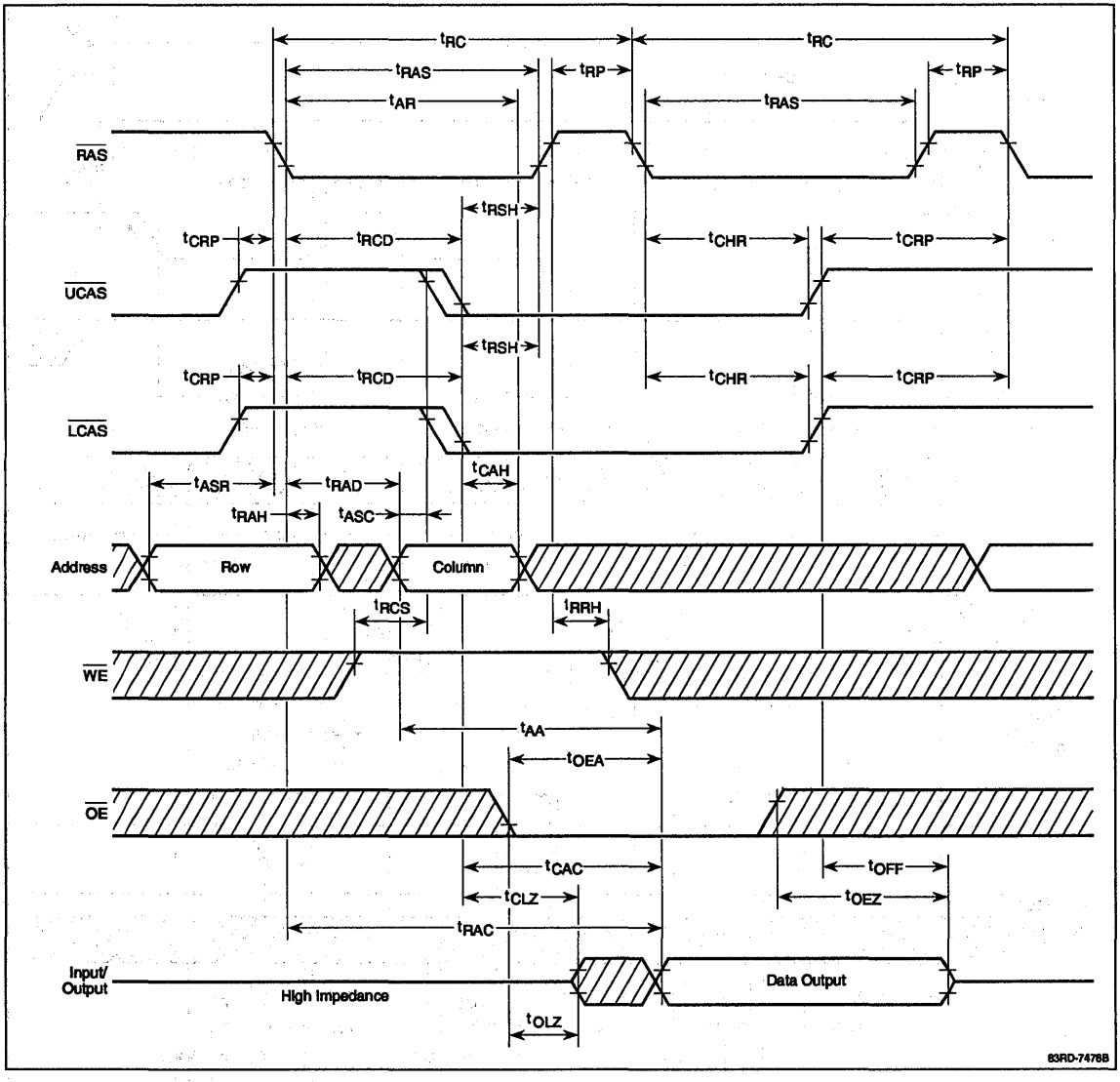
Byte Fast-Page Read-Modify-Write Cycle



7c

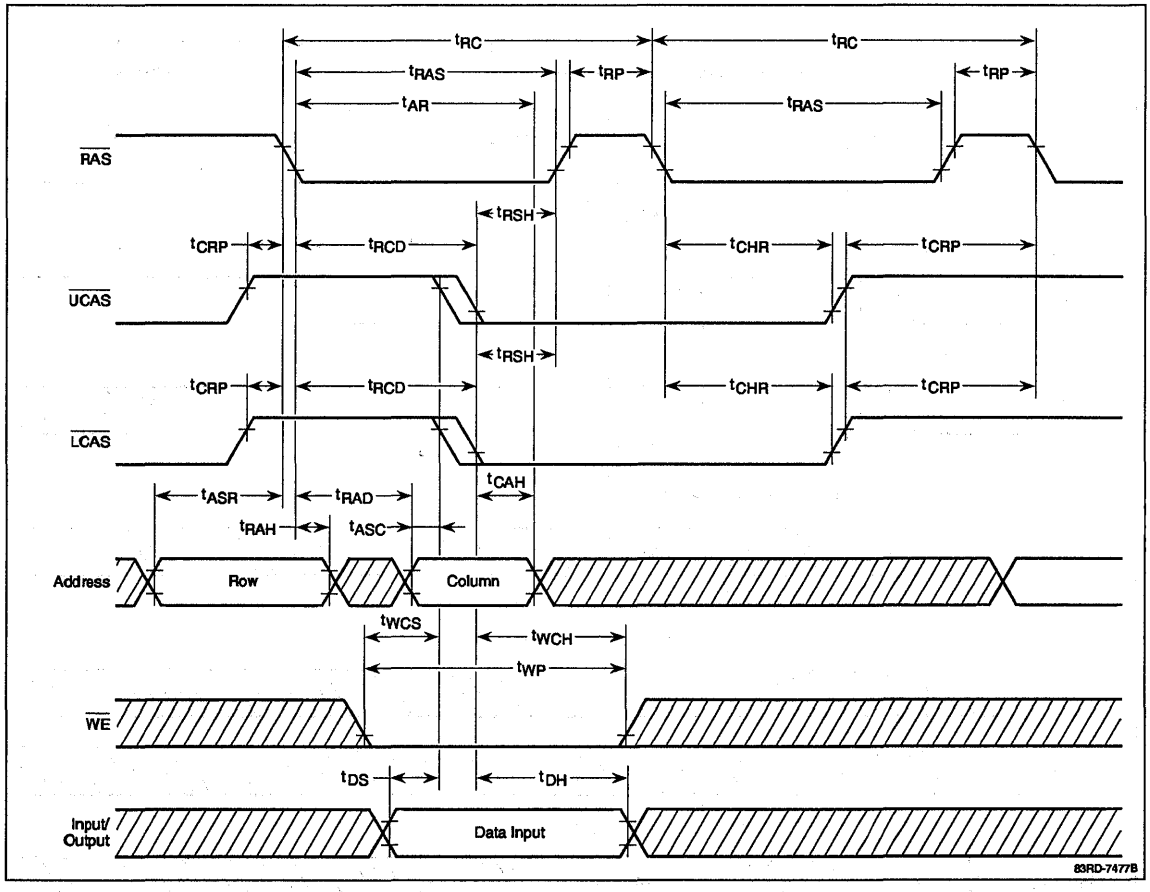
Timing Waveforms (cont)

Hidden Refresh Cycle (Word Read Cycle)



Timing Waveforms (cont)

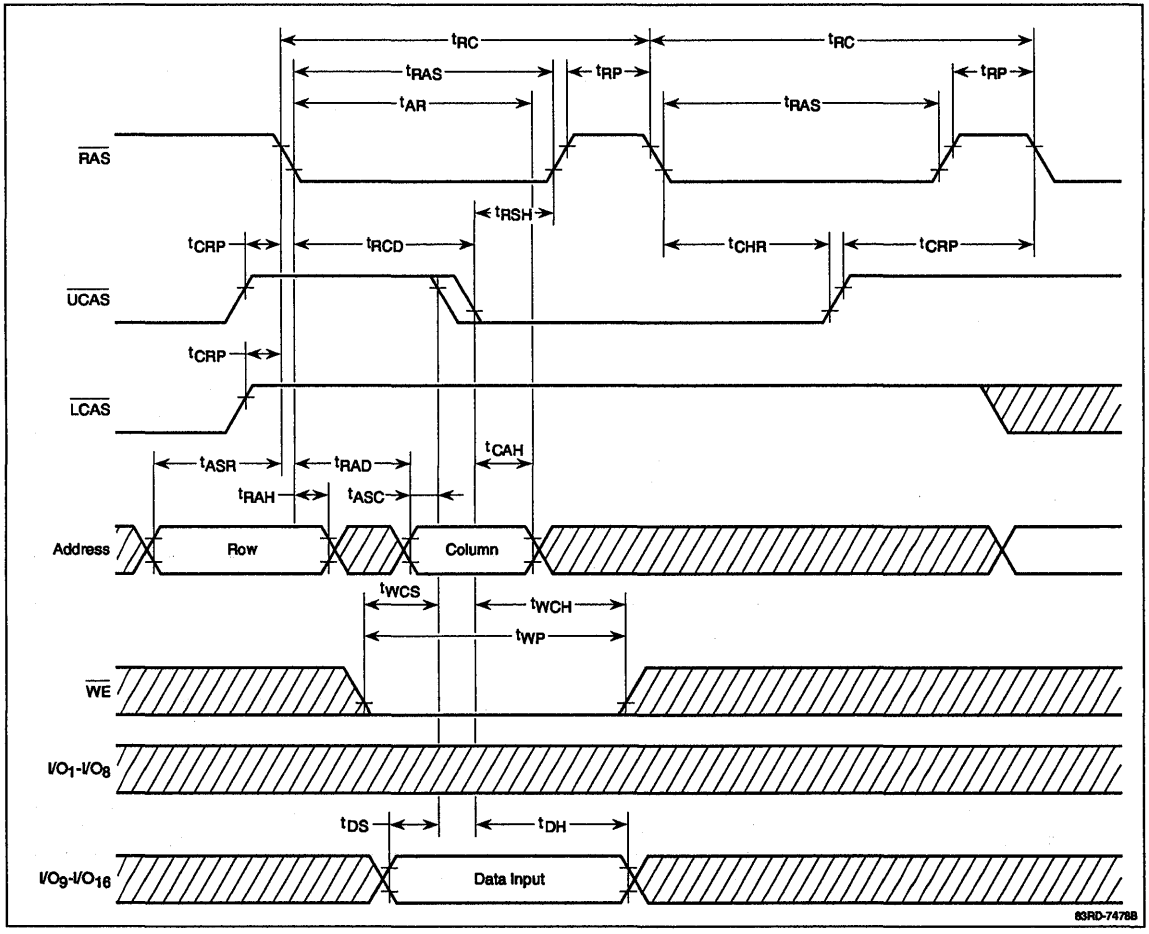
Hidden-Refresh Cycle (Word Write Cycle)



7c

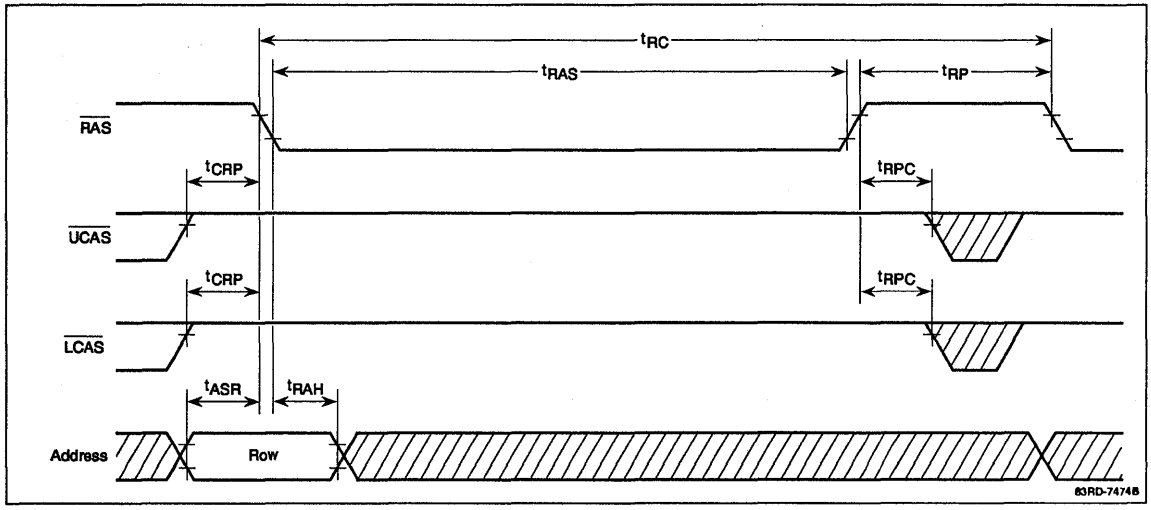
Timing Waveforms (cont)

Hidden-Refresh Cycle (Byte Write Cycle)

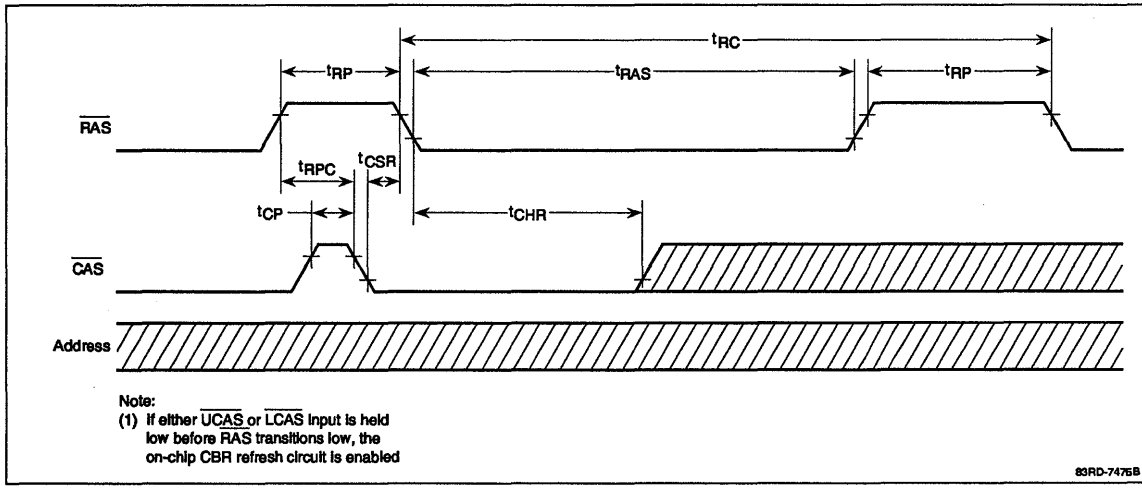


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



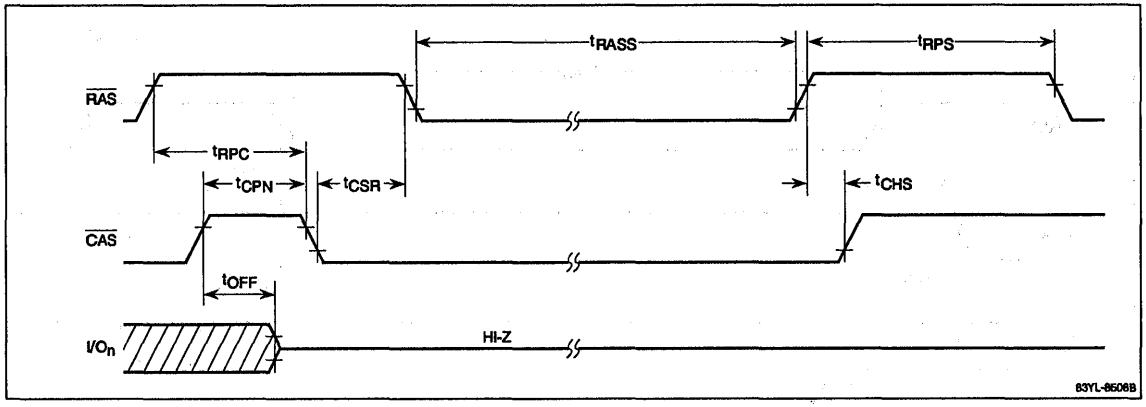
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



7c

Timing Waveforms (cont)

CBR Self-Refresh Cycle



μPD424263A/L, 42S4263A/L
262,144 x 16-Bit
Dynamic CMOS RAM

Description

The μPD424263A/L and μPD42S4263A/L are fast-page dynamic RAMs with the write-per-bit option, organized as 262,144 words by 16 bits, and designed to operate from a single power supply.

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
424263A	+5 V
424263L	+3.3 V
42S4263A	+5 V; self-refresh mode
42S4263L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{UCAS}$ and $\overline{LCAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, upper or lower byte data is held on the outputs by maintaining $\overline{UCAS}$ or $\overline{LCAS}$ low. Data outputs return to high impedance when either $\overline{UCAS}$ or $\overline{LCAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{UCAS}$ or $\overline{LCAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle ($\overline{CBR}$) that internally generates the refresh address. $\overline{RAS}$-only refresh cycles will also refresh all memory locations.

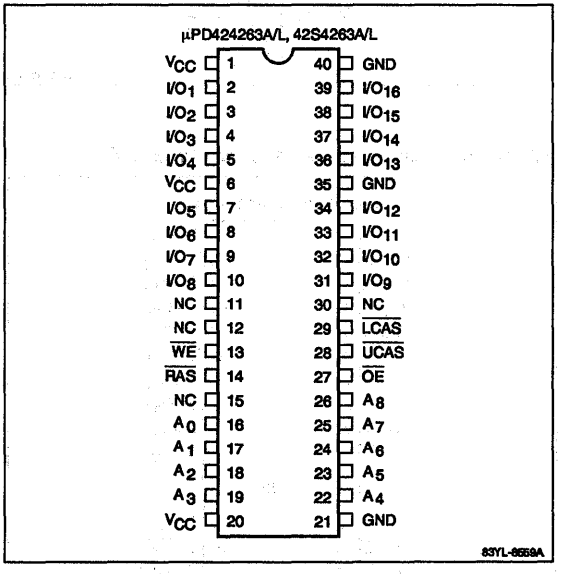
The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a $\overline{CBR}$ cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

- 262,144 by 16-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option
- Byte read/write control with $\overline{UCAS}$ and $\overline{LCAS}$
- Write-per-bit option; independent write control on 16 I/O's
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 512 refresh cycles every 8 ms
- 40-pin SOJ, 40-pin ZIP, and 44/40-pin TSOP plastic packaging

Pin Configurations

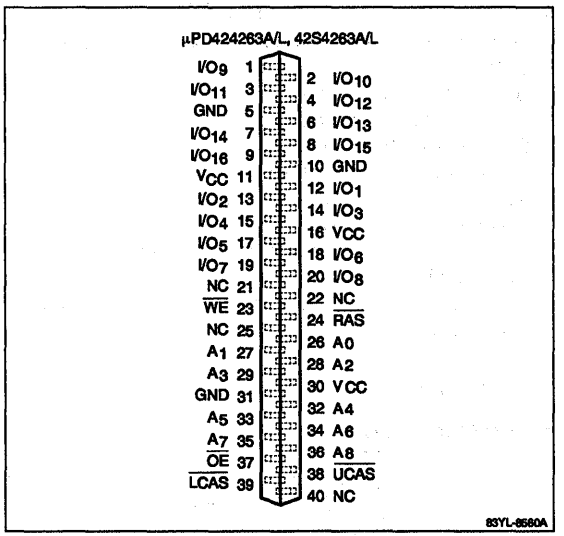
40-Pin Plastic SOJ



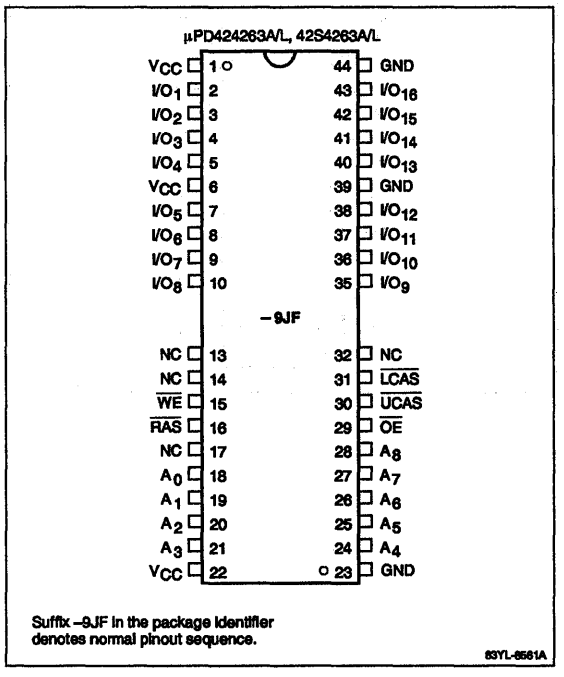
7d

Pin Configurations (cont)

40-Pin Plastic ZIP



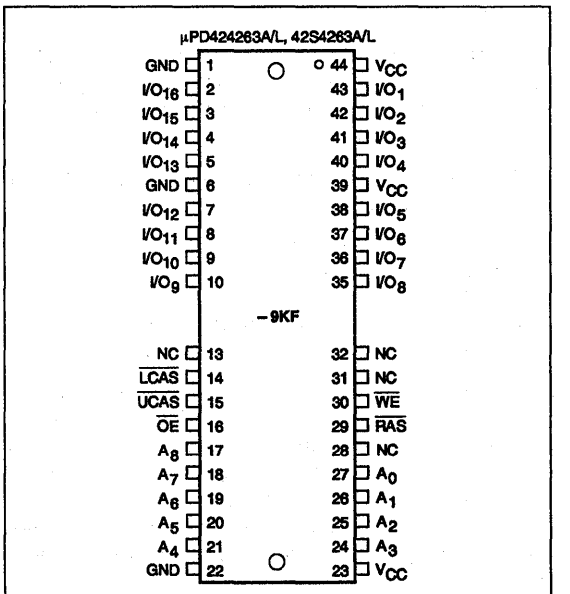
44/40-Pin Plastic TSOP (Normal Pinouts)



Suffix -9JF in the package identifier denotes normal pinout sequence.

83YL-8561A

44/40-Pin Plastic TSOP (Reverse Pinouts)



Suffix -9KF in the package identifier denotes reverse pinout sequence.

83YL-8562A

Pin Identification

A_0 - A_8	Address inputs
I/O_1 - I/O_{16}	Data inputs and outputs
$\overline{LCAS}$, $\overline{UCAS}$	Column address strobes
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

Ordering Information, μPD424263A (+ 5-volt power)

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Package
μPD424263ALE-60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD424263AV-60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-70	70 ns	45 ns		
V-80	80 ns	50 ns		
μPD424263AG5-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD424263AG5M-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD424263L (+ 3.3-volt power)

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Package
μPD424263LLE-A60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD424263LV-A60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-A70	70 ns	45 ns		
V-A80	80 ns	50 ns		
μPD424263LG5-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD424263LG5M-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

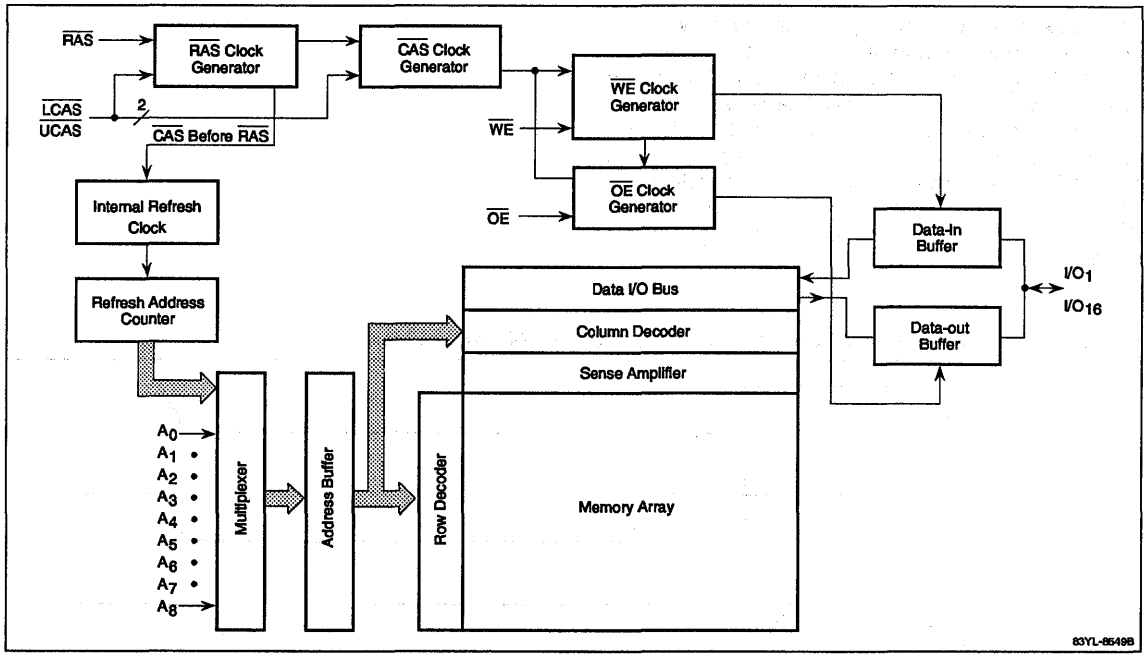
Ordering Information, μPD42S4263A (+ 5-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4263ALE-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4263AV-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic ZIP
V-70	70 ns	45 ns			
V-80	80 ns	50 ns			
μPD42S4263AG5-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns			
G5-80	80 ns	50 ns			
μPD42S4263AG5M-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns			
G5M-80	80 ns	50 ns			

Ordering Information, μPD42S4263L (+ 3.3-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4263LLE-A60	60 ns	40 ns	20 ns	100 μA	40-pin plastic SOJ
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			
μPD42S4263LV-A60	60 ns	40 ns	20 ns	100 μA	40-pin plastic ZIP
V-A70	70 ns	45 ns			
V-A80	80 ns	50 ns			
μPD42S4263LG5-A60	60 ns	40 ns	20 ns	100 μA	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns			
G5-A80	80 ns	50 ns			
μPD42S4263LG5M-A60	60 ns	40 ns	20 ns	100 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns			
G5M-A80	80 ns	50 ns			

Block Diagram



Truth Table

Function	RAS	LCAS	UCAS	WE	OE	I/O_1 - I/O_8	I/O_9 - I/O_{16}
Standby	H	X	X	X	X	High-Z	High-Z
Refresh cycle	L	H	H	X	X	High-Z	High-Z
Byte read cycle	L	L	H	H	L	Data output	High-Z
	L	H	L	H	L	High-Z	Data output
Word read cycle	L	L	L	H	L	Data output	Data output
Byte write cycle	L	L	H	L	H	Data input	—
	L	H	L	L	H	—	Data input
Word write cycle	L	L	L	L	H	Data input	Data input
——	L	L	L	H	H	High-Z	High-Z

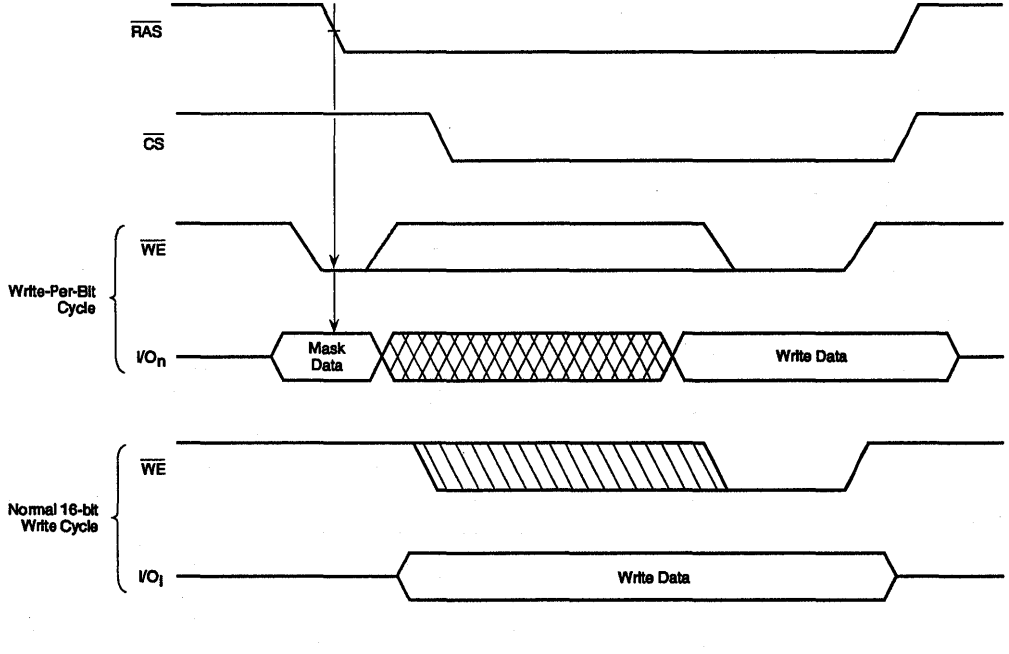
X = don't care.

7d

Write-Per-Bit Option

The write-per-bit option may be used to allow a write cycle to change any number of bits in the 16-bit word. The mask is loaded from the I/O lines at the falling edge of $\overline{RAS}$ if $\overline{WE}$ = V_{IL}. If the I/O line is high, then the corresponding bit will be written when the write cycle executes. If the I/O line is low, the bit does not change. A mask loaded during fast-page operation will remain set and active for each write cycle that executes while $\overline{RAS}$ remains low. The mask may be changed only at the falling edge of $\overline{RAS}$.

Comparison of Write-Per-Bit Cycle Versus Standard 16-Bit Write Cycle



I/O	Mask Data		Write Operation
I/O_1 ~ I/O_{16}	1	(High)	Write Bit
	0	(Low)	Disable Bit Write

83YL-8563B

Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
5-volt devices	50 mA
3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_{16}

Recommended Operating Conditions

		5-Volt Devices			3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.5		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

Self-Refresh Current

T_A = 0 to +70°C; V_{CC} = +5 V ±10% (42S4263A) or +3.3 V ±0.3 V (42S4263L)

Symbol	42S4263A	42S4263L	Conditions
I_{CC7}	300 μA max	100 μA max	I/O pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. Other input pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. $t_{RAS} \geq 100$ μs

7d

DC Characteristics; 5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				300	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –5 mA

DC Characteristics; 3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			500	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				100	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–5		5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–5		5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

AC Characteristics

T_A = 0 to +70°C

μPD424263A, 42S4263A: V_{CC} = +5.0 V ±10%

μPD424263L, 42S4263L: V_{CC} = +3.3 V ±0.3 V

		-60		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5)		140		130		120	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
	I_{CC1} (+3.3)		130		120		110		
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5)		140		130		120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
	I_{CC3} (+3.3)		130		120		110		
Operating current, fast-page cycle, average	I_{CC4} (+5)		90		80		70	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
	I_{CC4} (+3.3)		90		80		70		
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5)		140		130		120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
	I_{CC5} (+3.3)		130		120		110		
Access time from column address	t_{AA}		30		35		40	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 3, 4, 7, 8, 16)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		ns	(Note 14)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		ns	(Note 15)
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	−35		−40		−50		ns	For 42S4263A/L only
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	(Notes 4, 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		75		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		50		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 13)
Masked write hold time referenced to $\overline{RAS}$	t_{MRH}	0		0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	(Note 9)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Output disable from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t_{PC}	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with exended data output	t_{PRWC}	85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		10		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		μs	For 42S4263A/L
Random read or write cycle time	t_{RC}	120		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	120		130		150		ns	For 42S4263A/L
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	(Note 11)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Read-modify-write cycle time	t_{RWC}	165		175		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Rise and fall times	t_T	3	50	3	50	3	50	ns	(Note 4)
Write-per-bit hold time	t_{WBH}	10		10		15		ns	
Write-per-bit setup time	t_{WBS}	0		0		0		ns	
Write command hold time	t_{WCH}	15		15		15		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		ns	(Note 14)
Write mask data hold time	t_{WH}	10		10		15		ns	
Write command pulse width	t_{WP}	15		15		15		ns	(Note 12)
Write mask data setup time	t_{WS}	0		0		0		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF. For 3.3-volt devices, V_{OH} = 2.0 volts and V_{OL} = 0.8 volt (ac reference levels)

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max); if $t_{RAD} \geq t_{RAD}$ (max) access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of one of the $\overline{CAS}$ signals for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

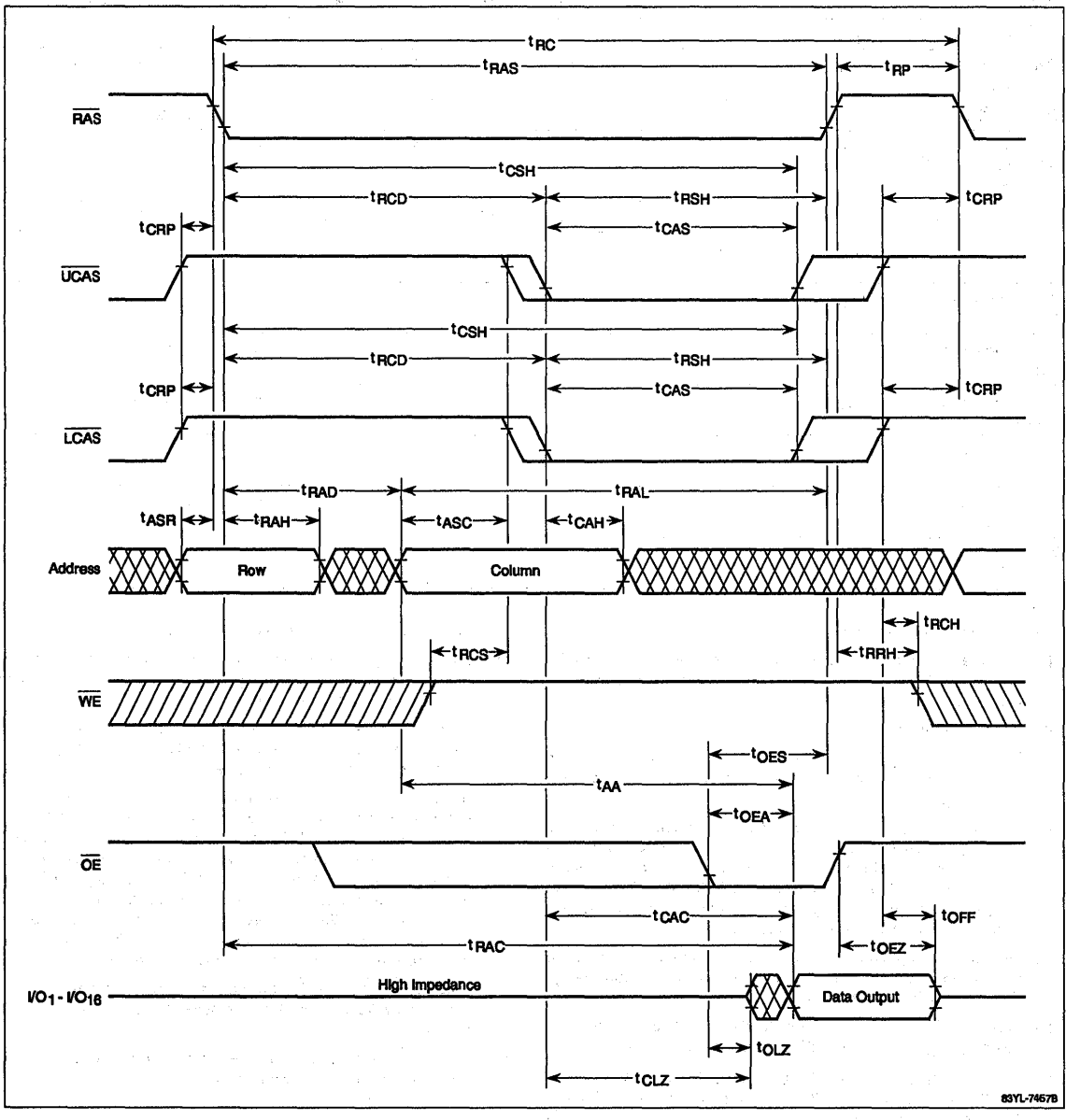
(14) t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD} and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) Holding $\overline{LCAS}$ or $\overline{UCAS}$ low prior to $\overline{RAS}$ going negative will initiate a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (t_{CSR} and t_{CHR} must be satisfied).

(16) The first $\overline{CAS}$ falling edge is used as a reference for the start of t_{ACP} ($\overline{CAS}$ precharge access time).

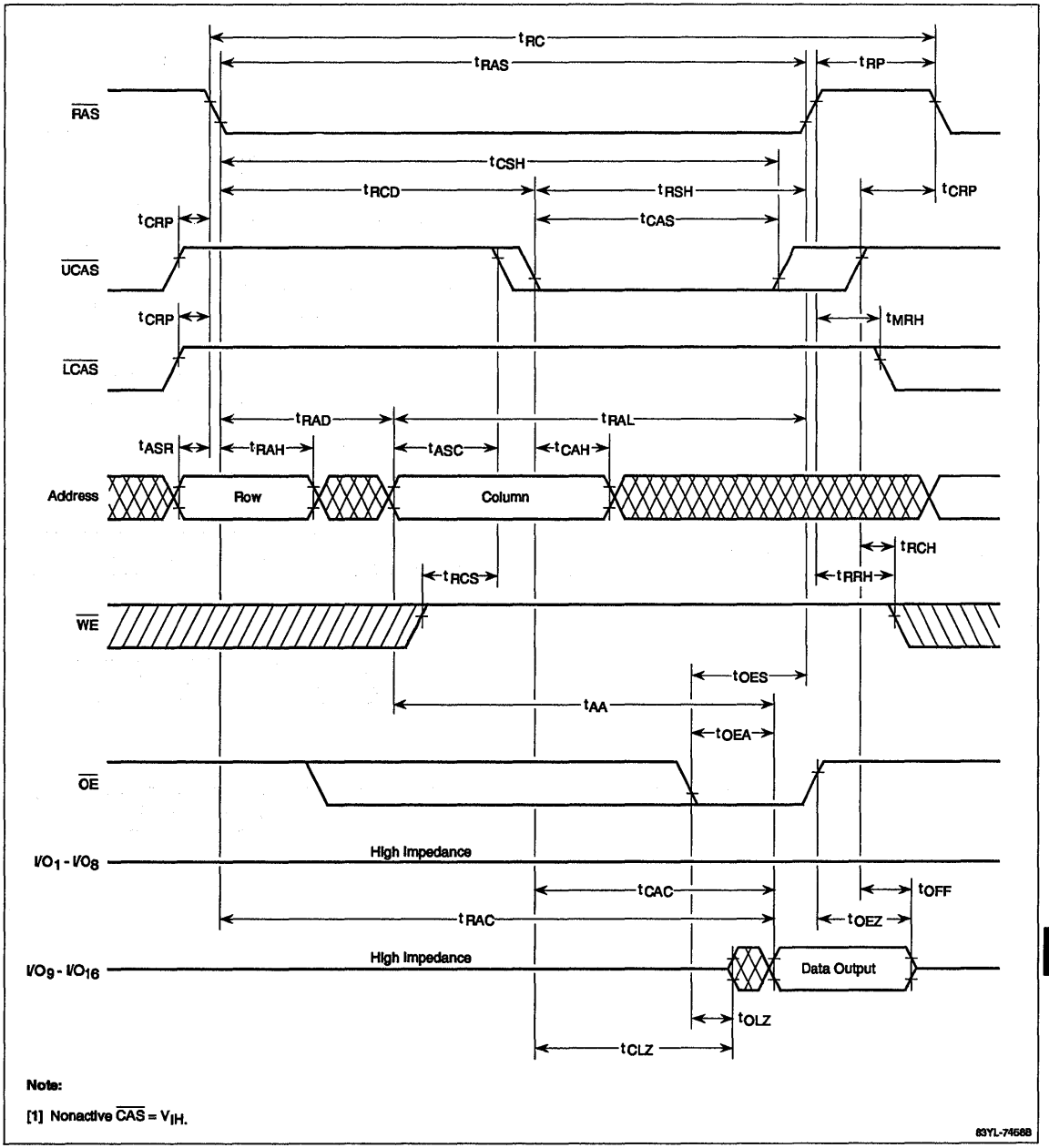
Timing Waveforms

Word Read Cycle



Timing Waveforms (cont)

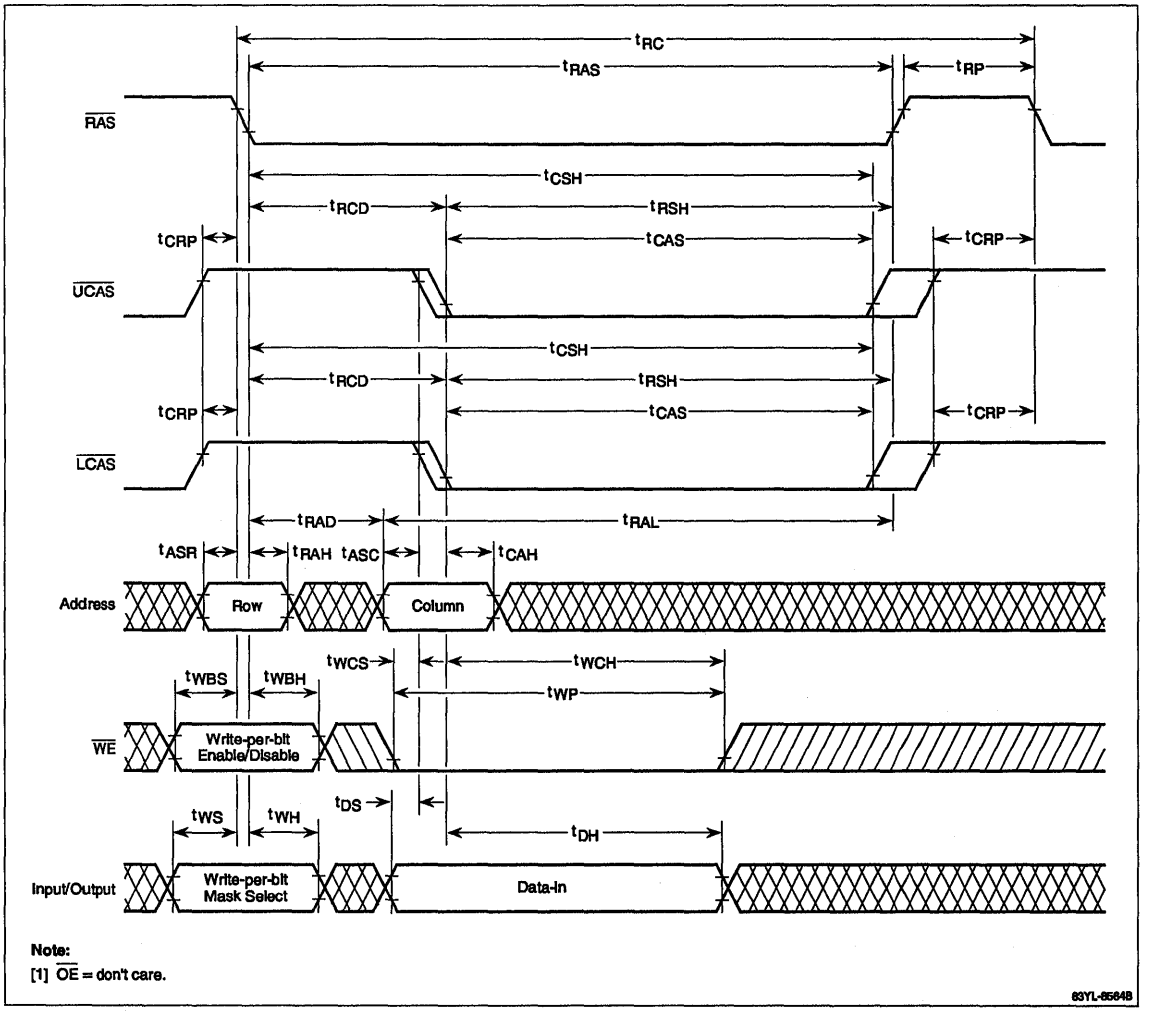
Byte Read Cycle



7d

Timing Waveforms (cont)

Word Early-Write Cycle

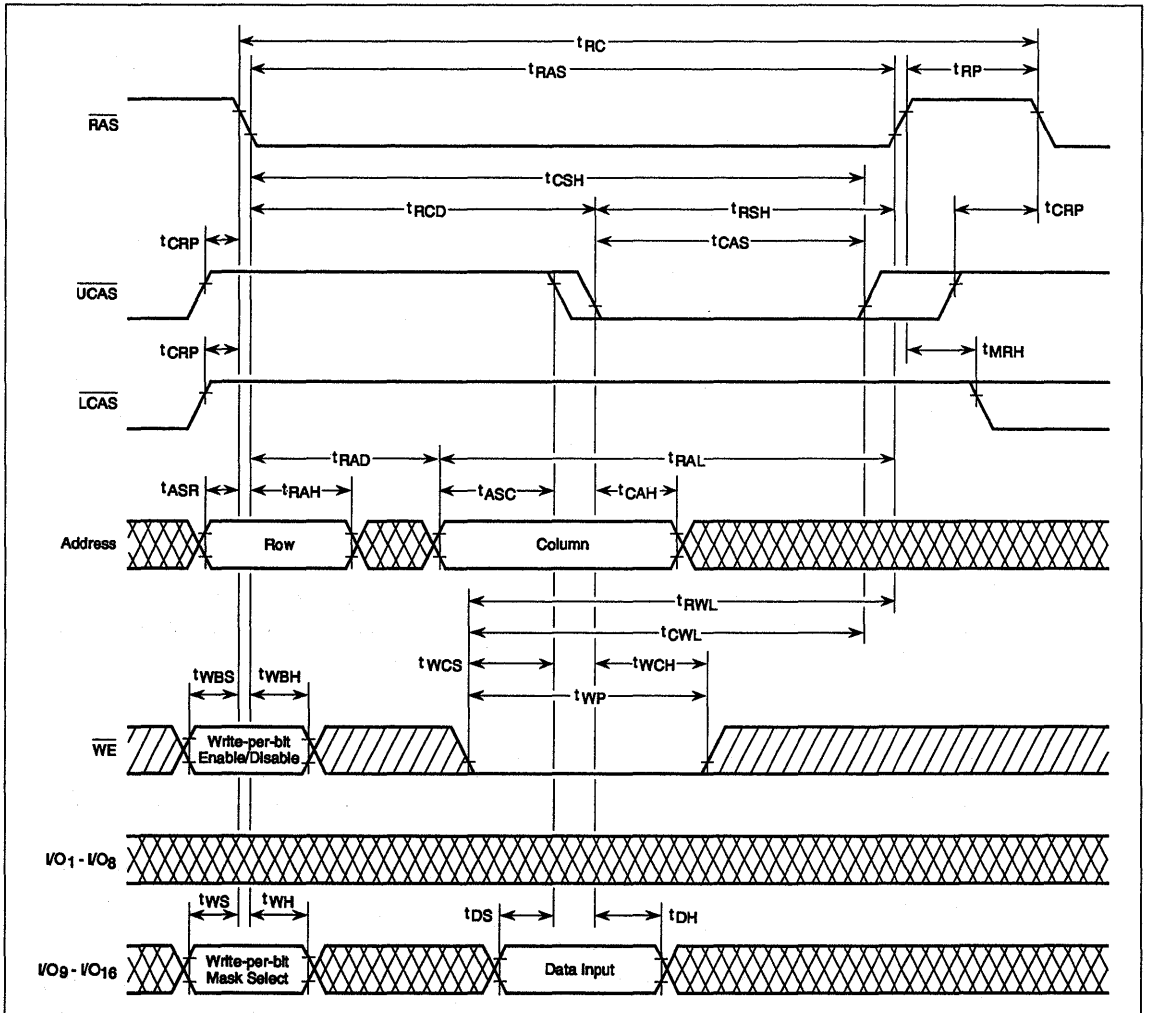


Note:
[1] $\overline{OE}$ = don't care.

83YL-8564B

Timing Waveforms (cont)

Byte Early-Write Cycle



Notes:

[1] Nonactive $\overline{CAS}$ = V_{IH}.

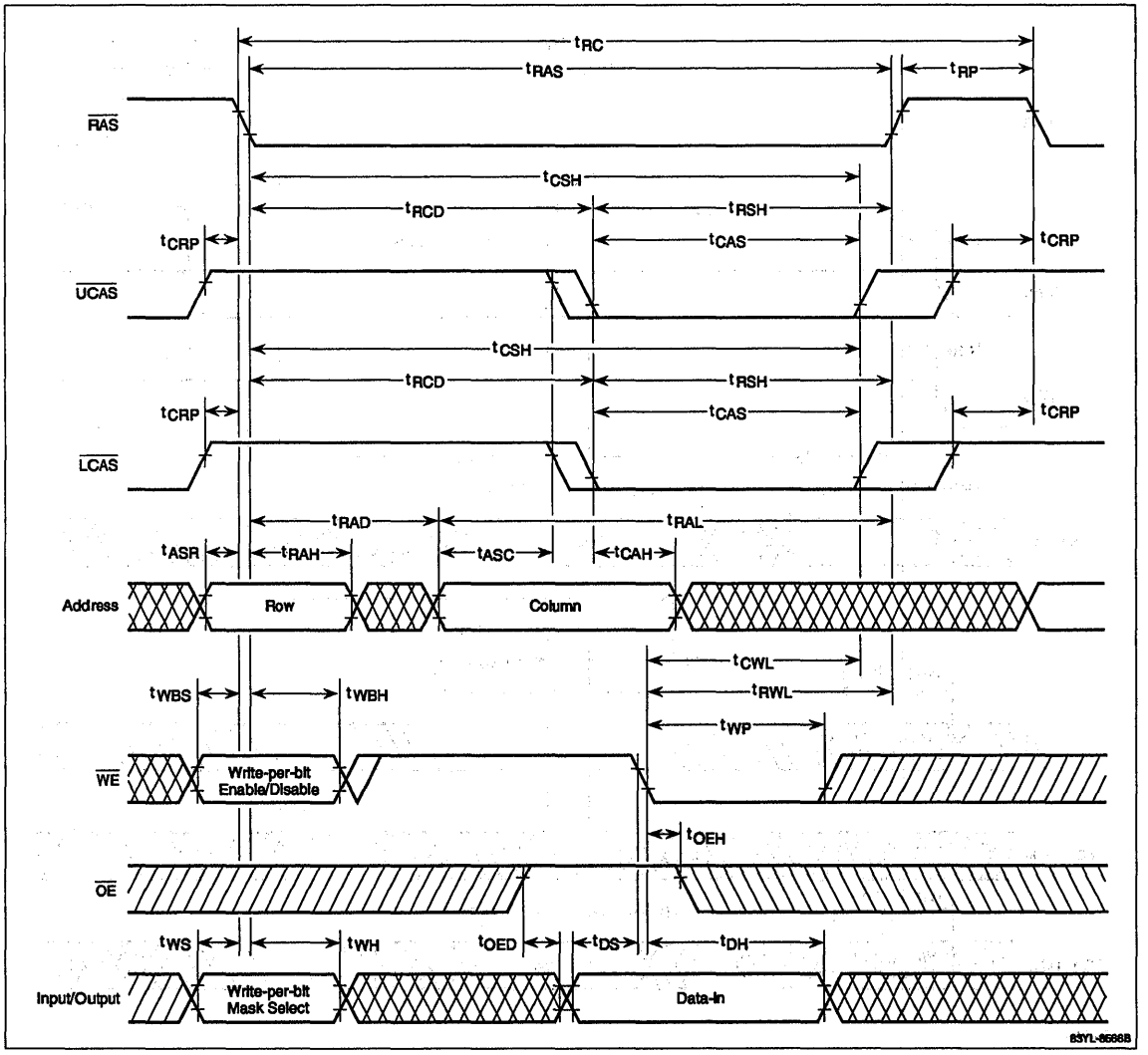
[2] $\overline{OE}$ = don't care.

83YL-85668

7d

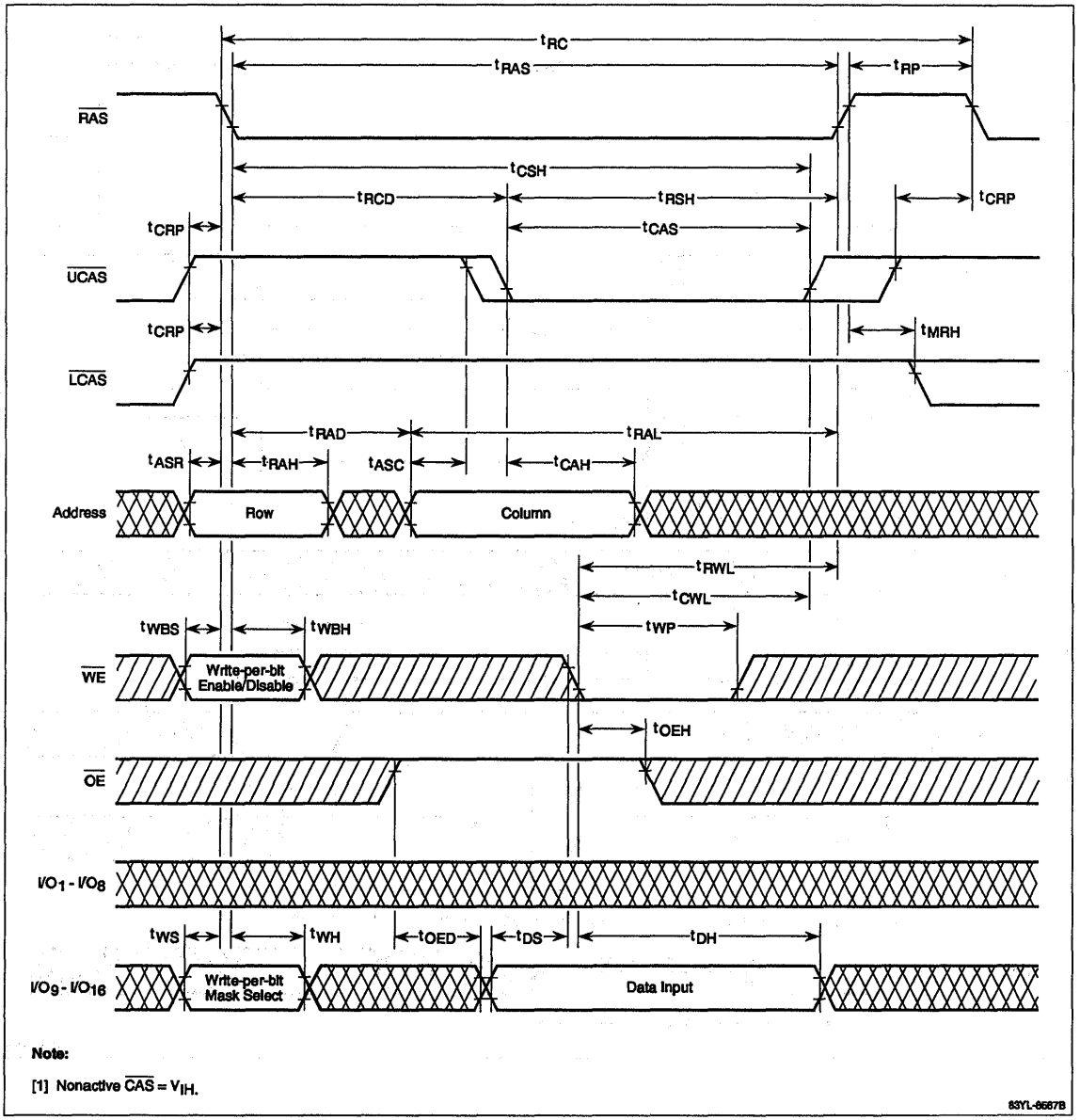
Timing Waveforms (cont)

Word Late-Write Cycle



Timing Waveforms (cont)

Byte Late-Write Cycle



Note:

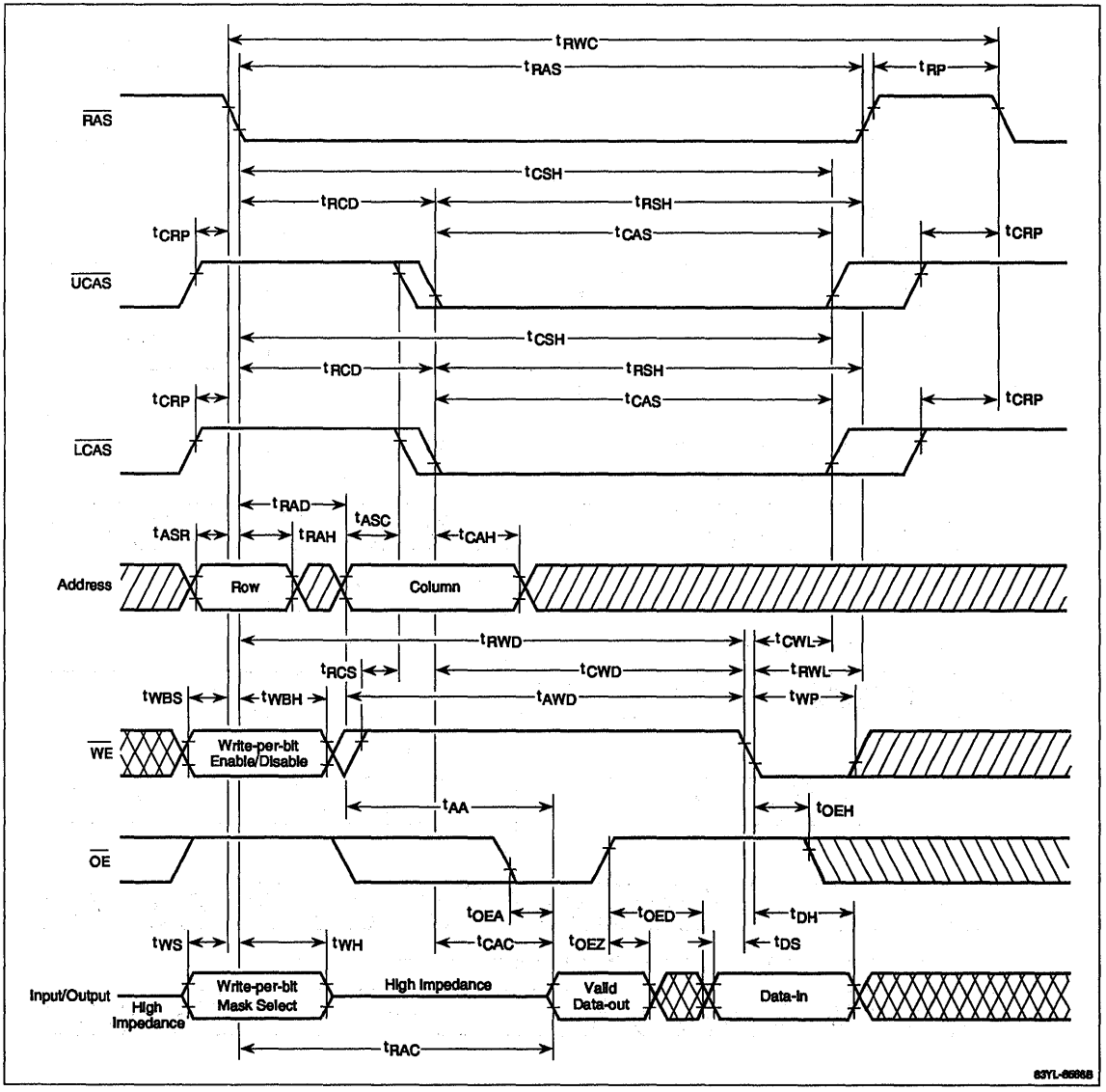
[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-8667B

7d

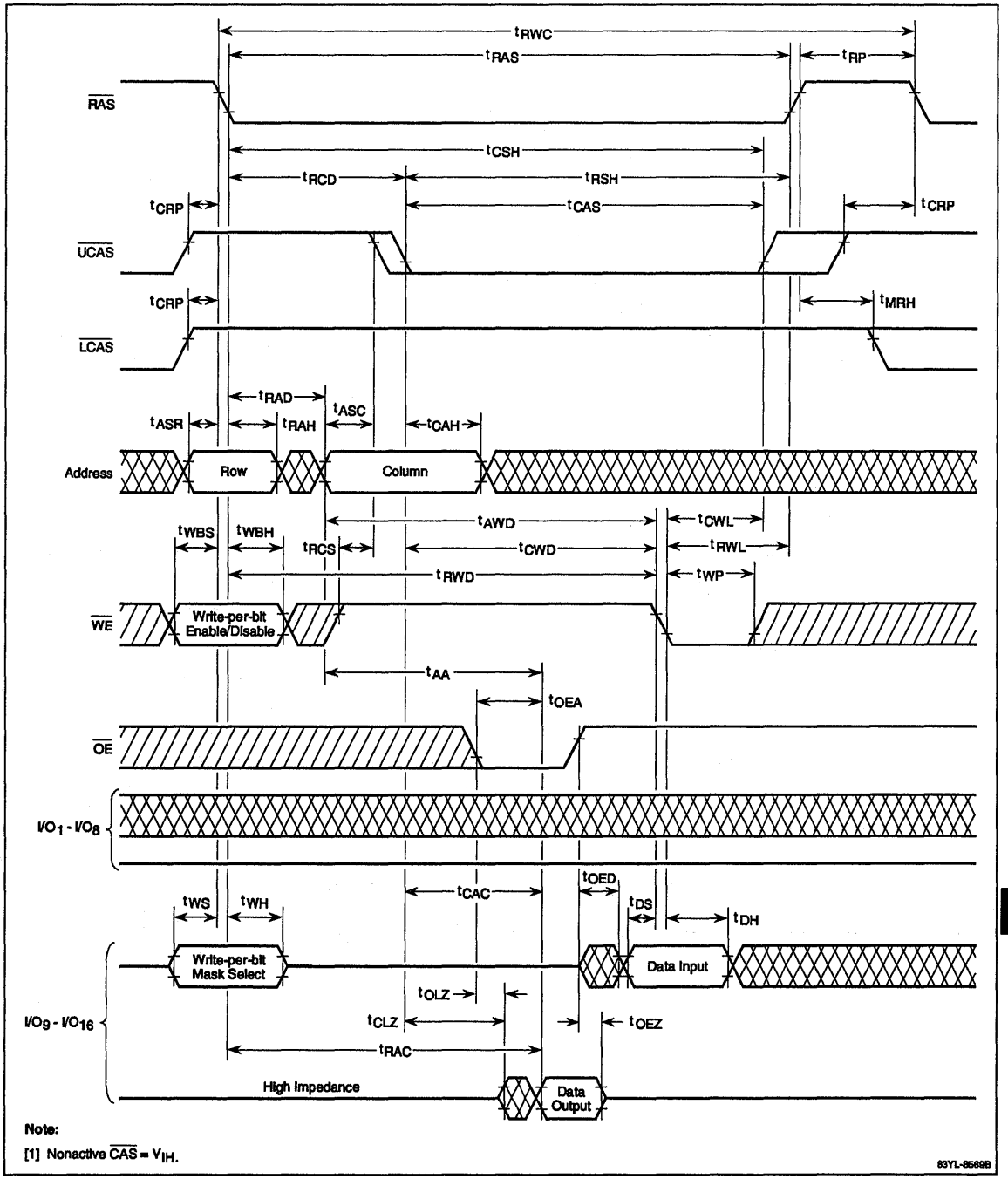
Timing Waveforms (cont)

Word Read-Modify-Write Cycle



Timing Waveforms (cont)

Byte Read-Modify-Write Cycle



Note:

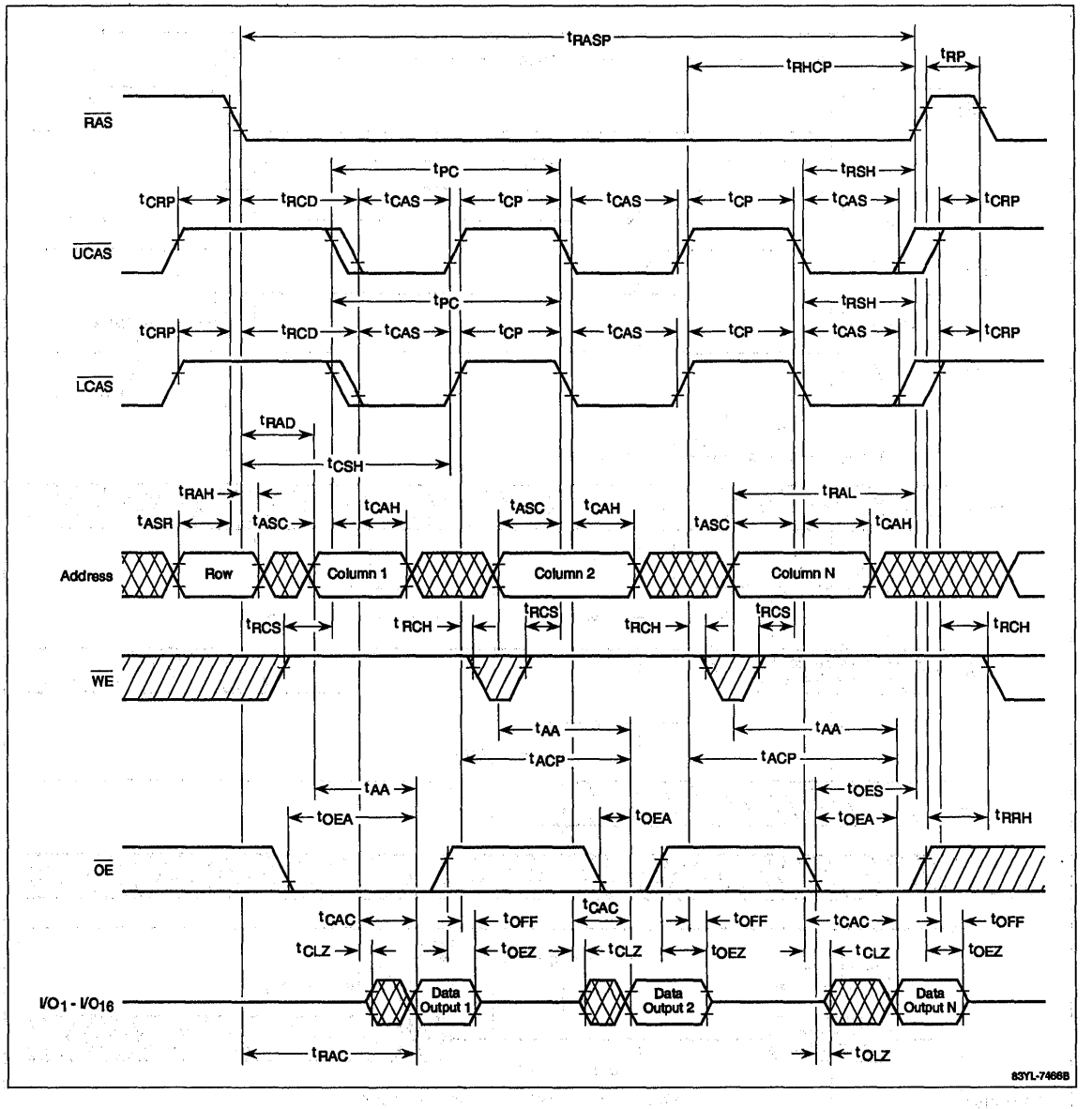
[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-8569B

7d

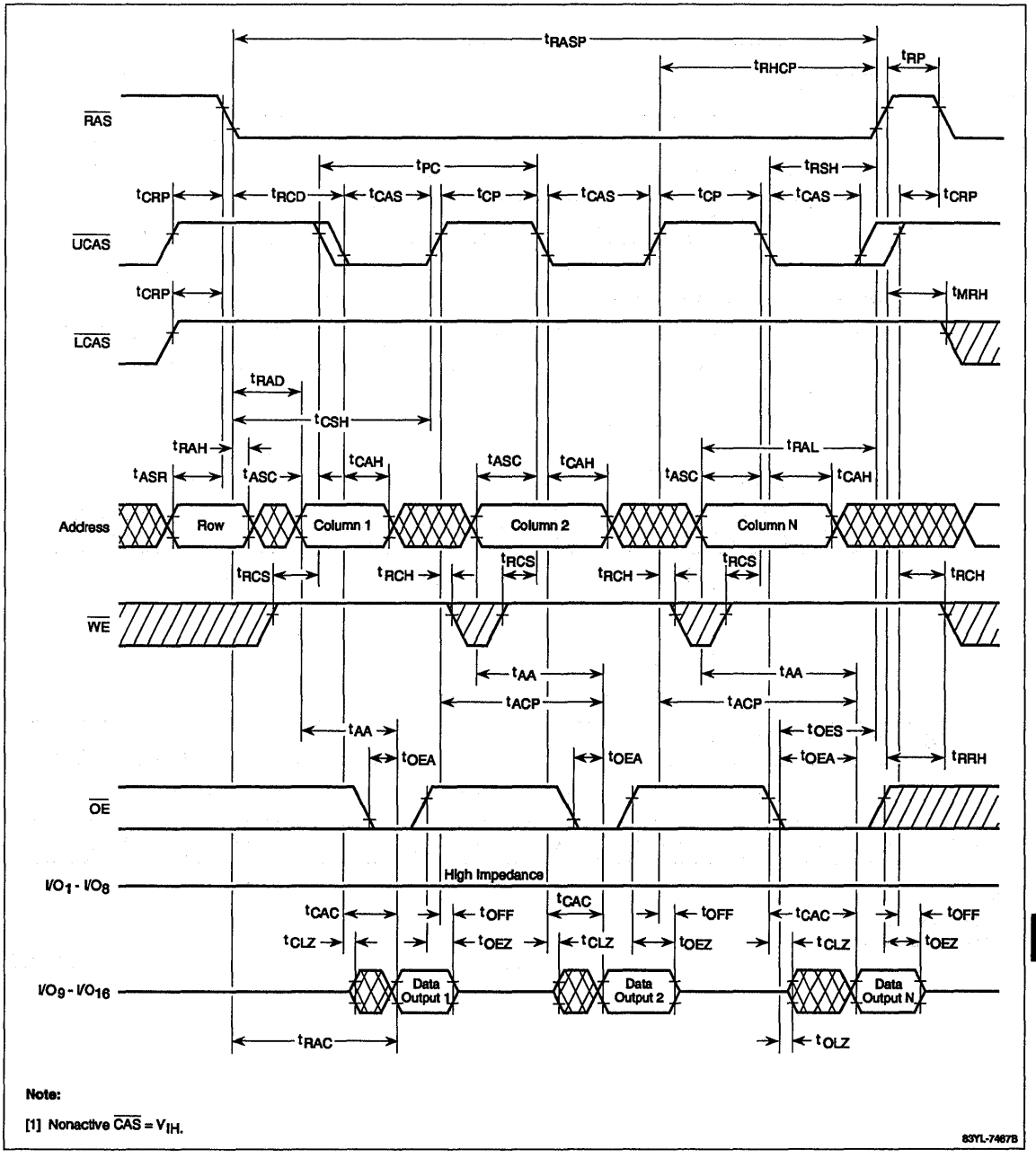
Timing Waveforms (cont)

Word Fast-Page Read Cycle



Timing Waveforms (cont)

Byte Fast-Page Read Cycle



Note:

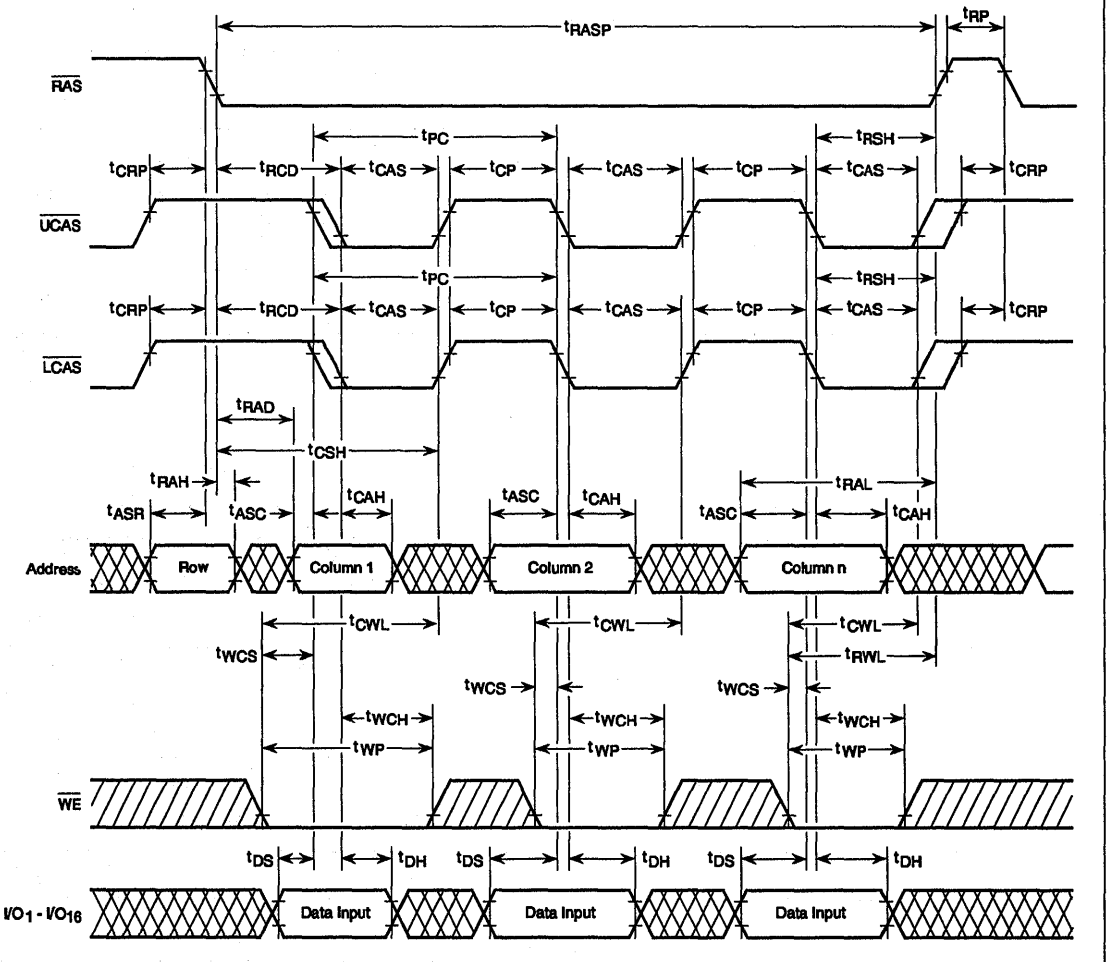
[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-7467B

7d

Timing Waveforms (cont)

Word Fast-Page Early-Write Cycle



Note:

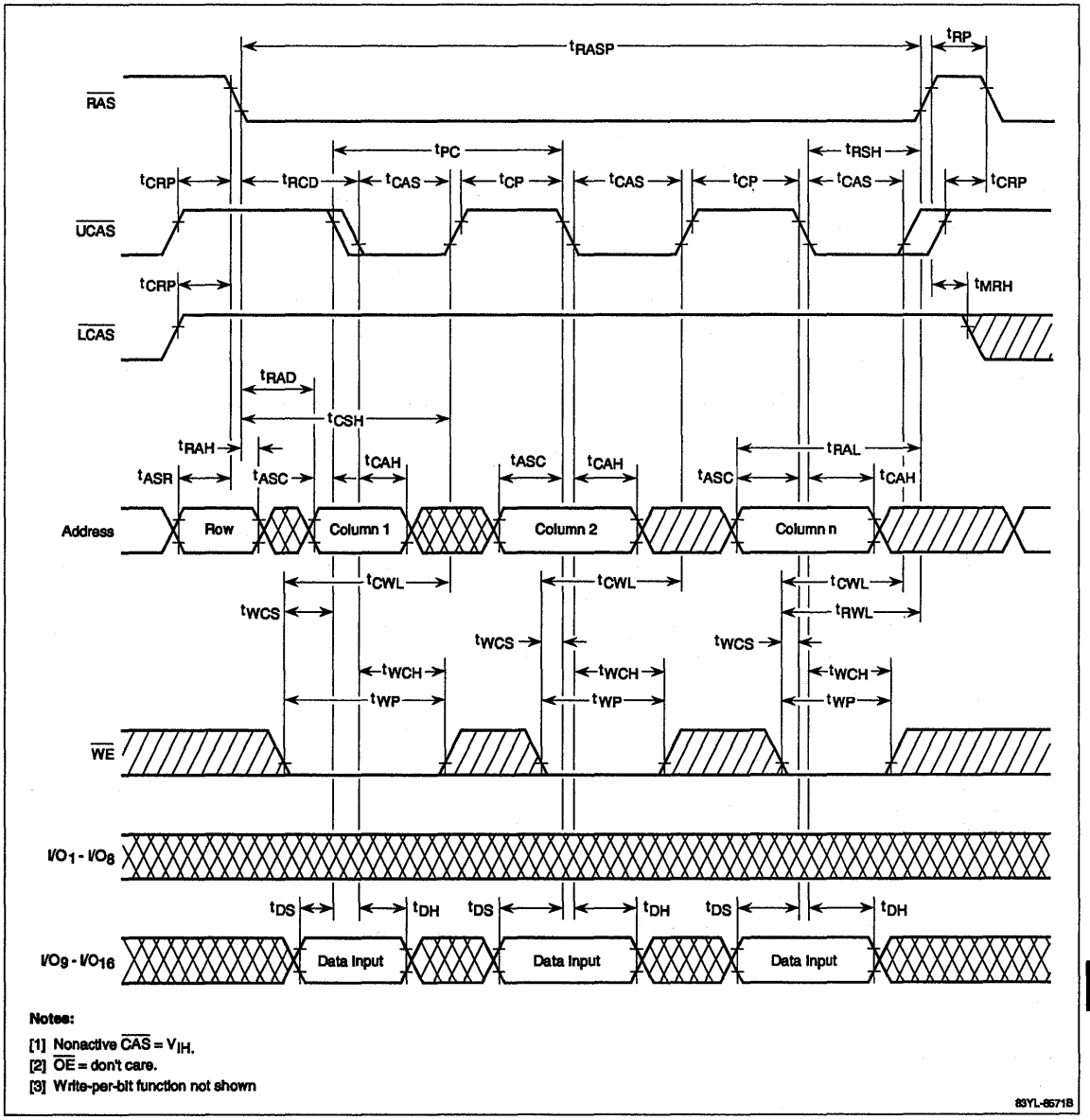
[1] $\overline{OE}$ = don't care.

[2] Write-per-bit function not shown

83YL-6570B

Timing Waveforms (cont)

Byte Fast-Page Early-Write Cycle



Notes:

[1] Nonactive $\overline{CAS}$ = V_{IH}.

[2] $\overline{OE}$ = don't care.

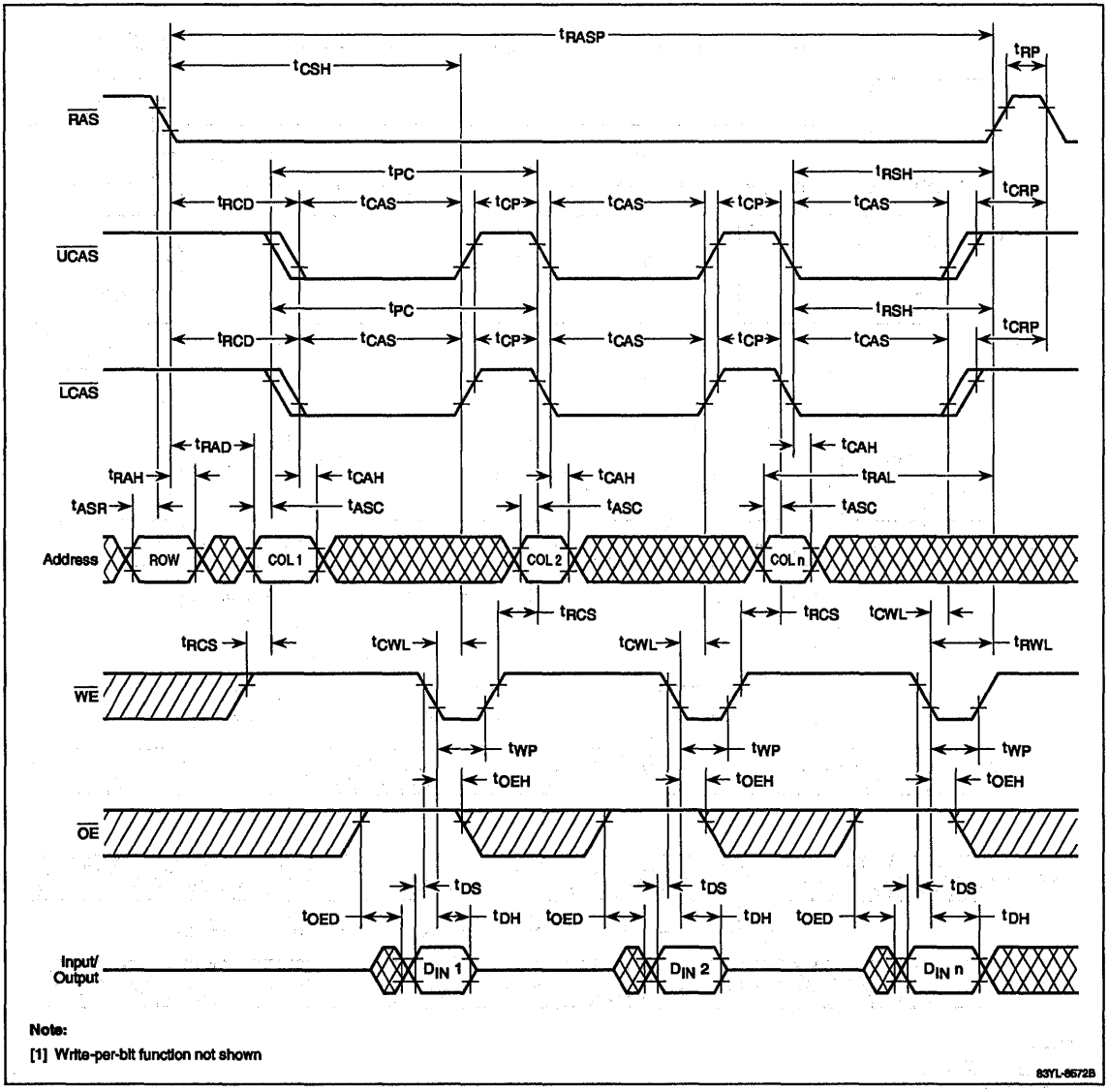
[3] Write-per-bit function not shown

83YL-8571B

7d

Timing Waveforms (cont)

Word Fast-Page Late-Write Cycle



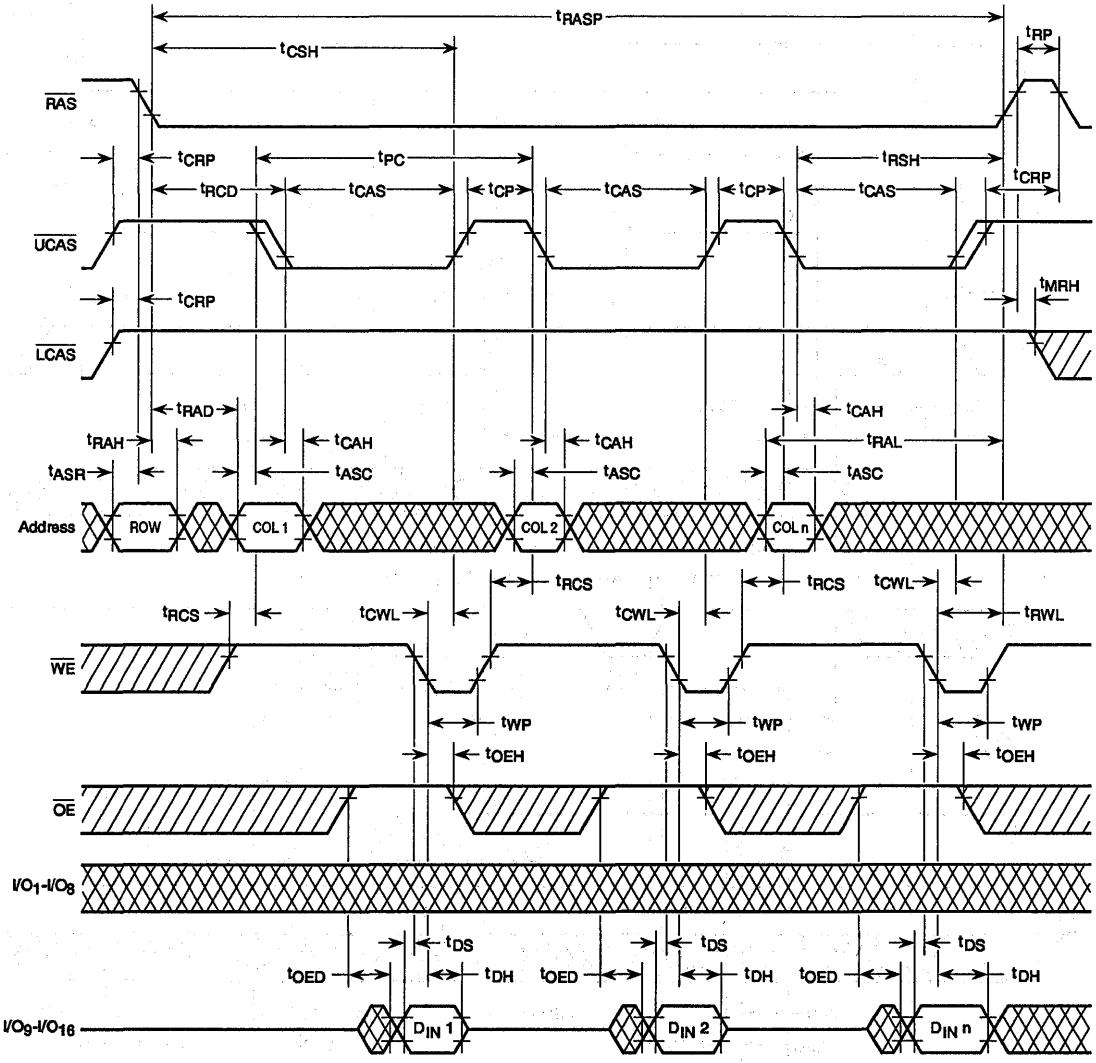
Note:

[1] Write-per-bit function not shown

83YL-8572B

Timing Waveforms (cont)

Byte Fast-Page Late-Write Cycle



Notes:

[1] Nonactive $\overline{CAS} = V_{IH}$.

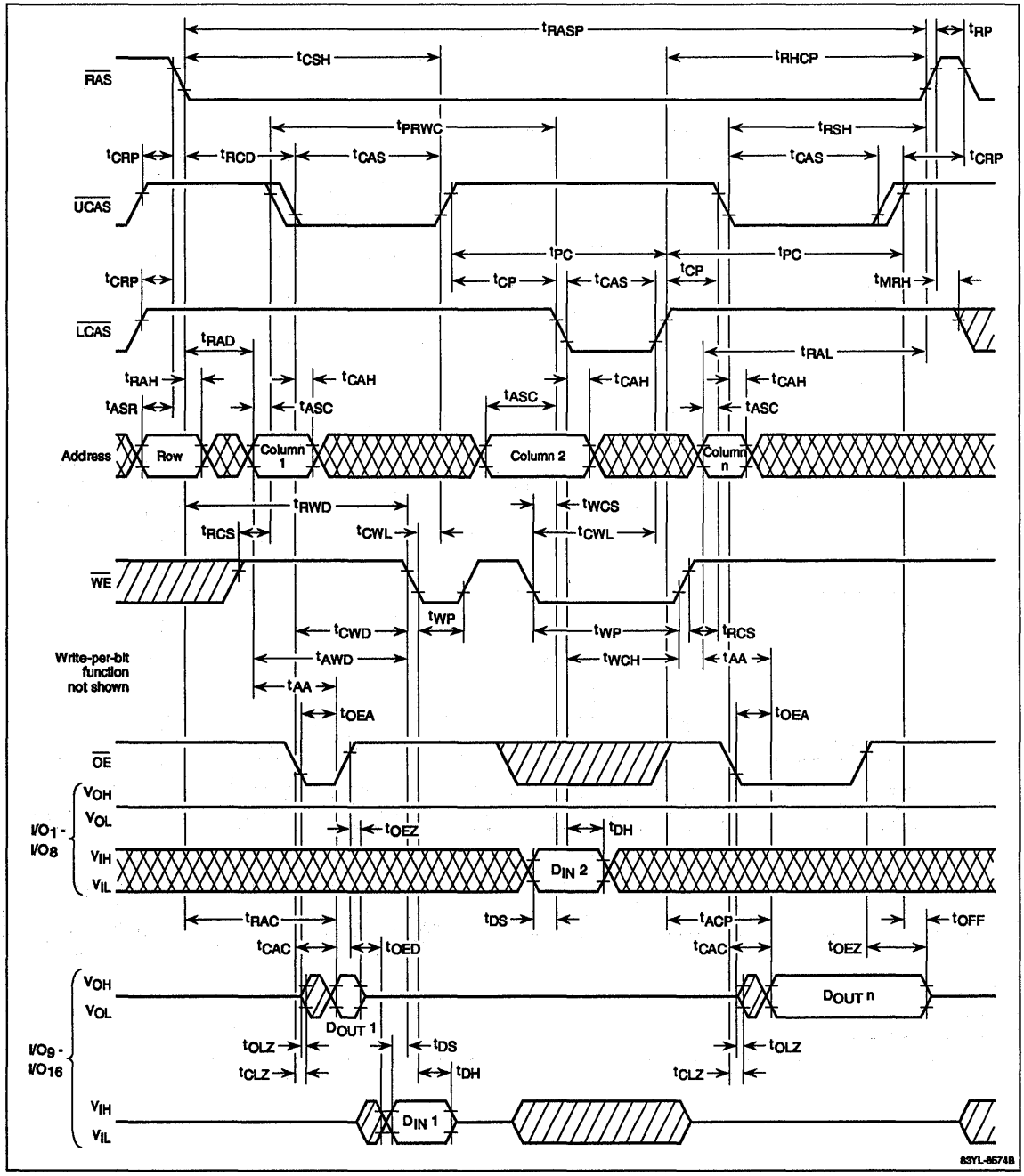
[2] Write-per-bit function not shown

83YL-8573B

7d

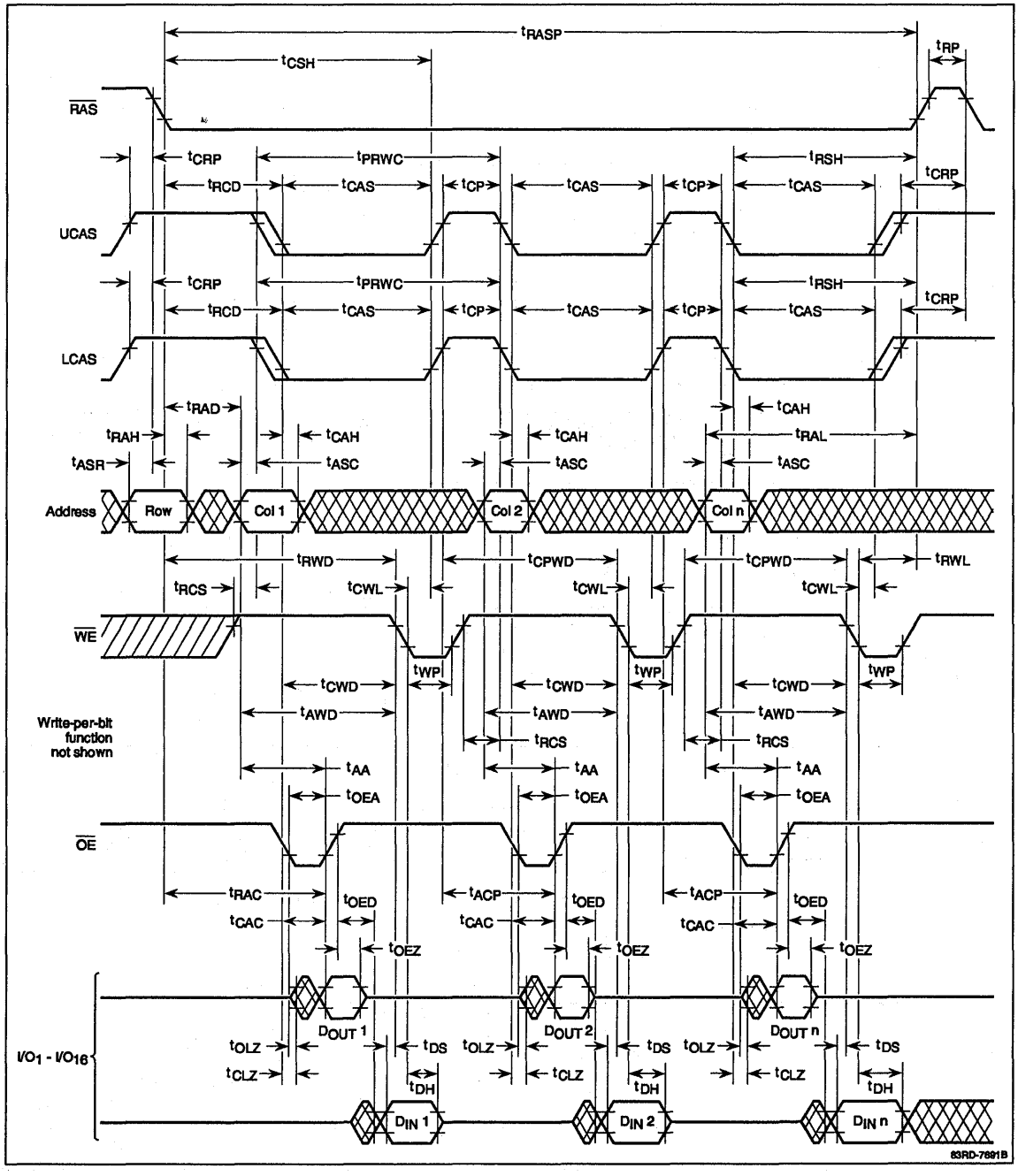
Timing Waveforms (cont)

Byte Fast-Page Read/Write Cycle



Timing Waveforms (cont)

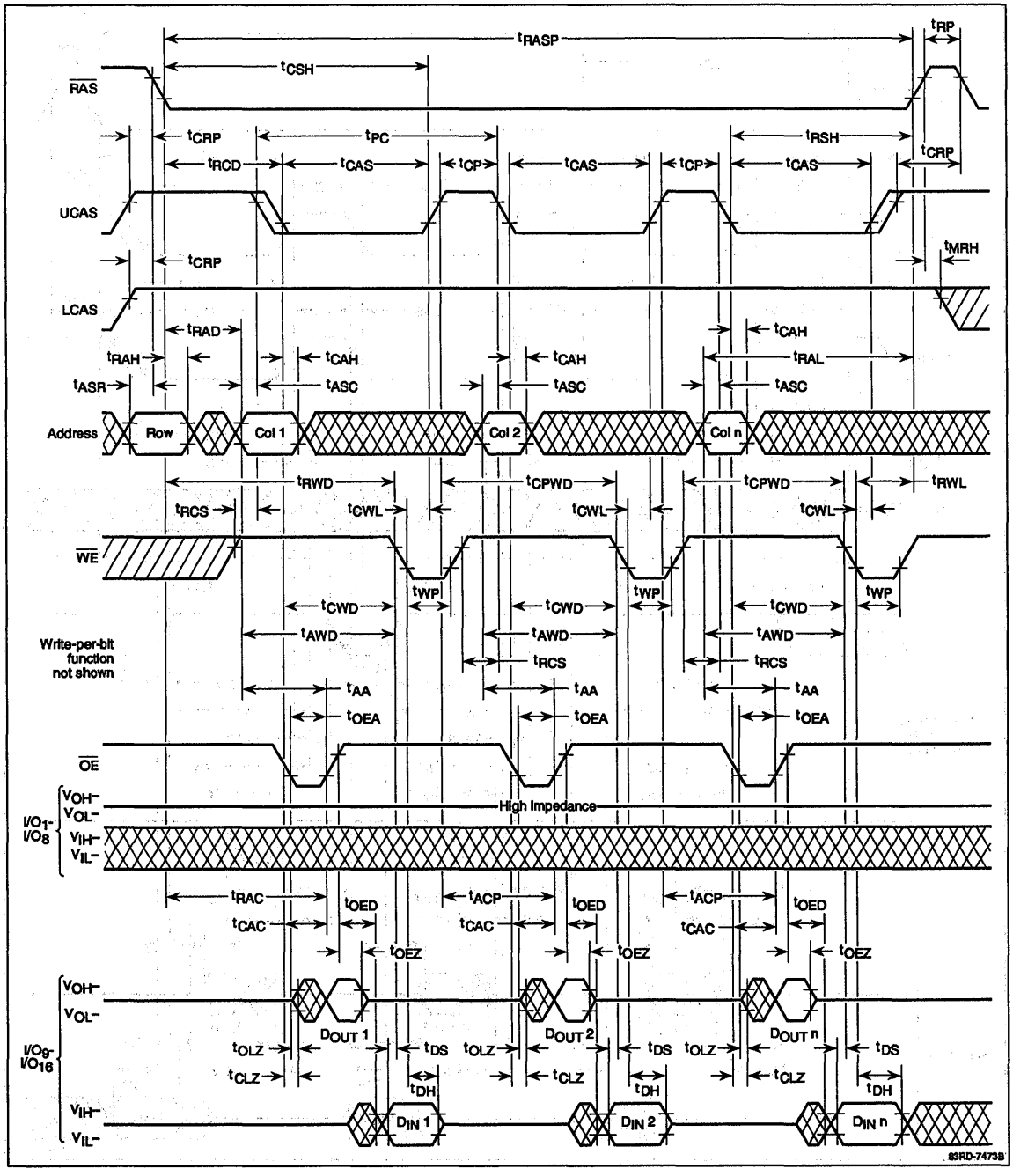
Word Fast-Page Read-Modify-Write Cycle



7d

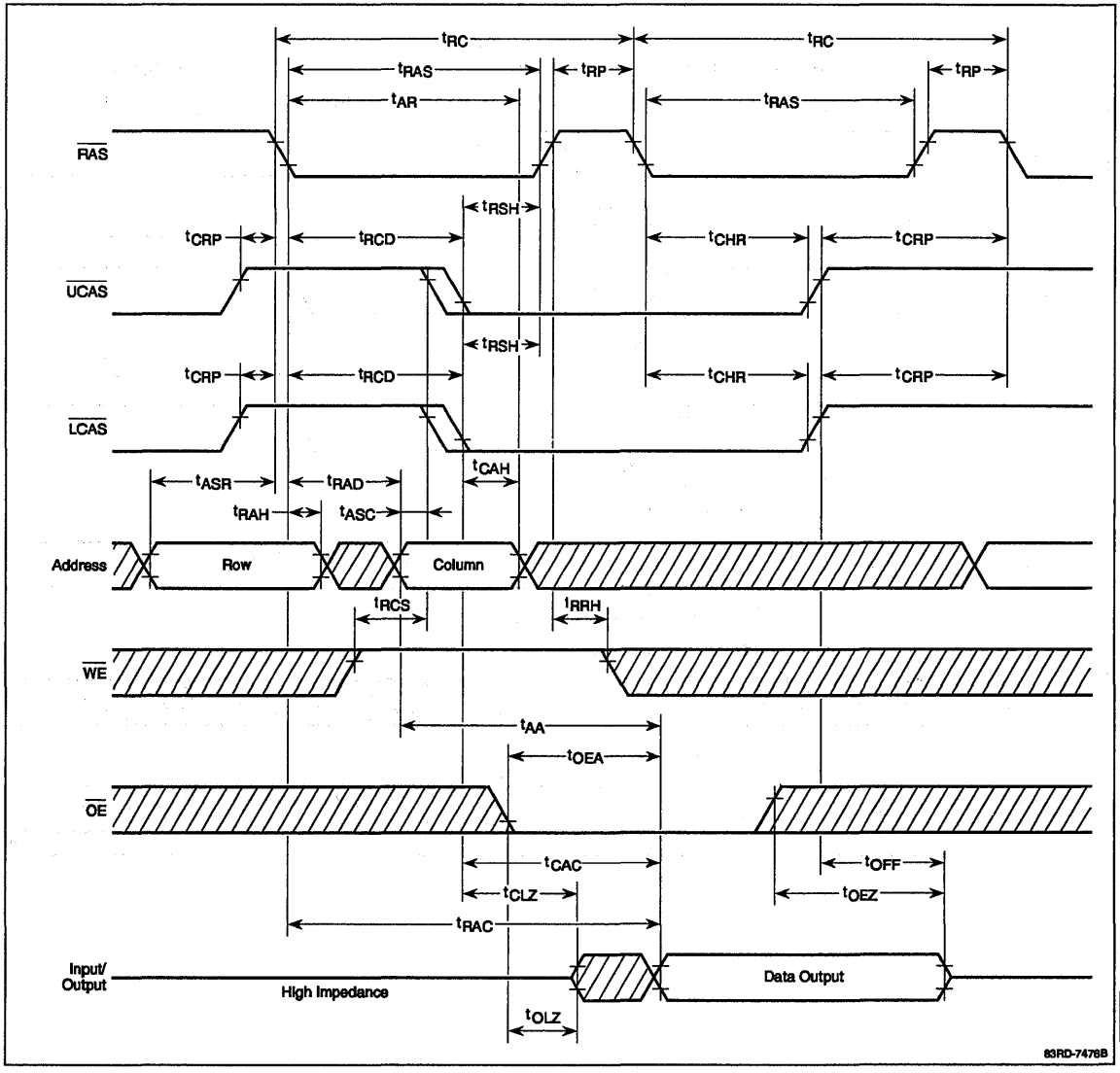
Timing Waveforms (cont)

Byte Fast-Page Read-Modify-Write Cycle



Timing Waveforms (cont)

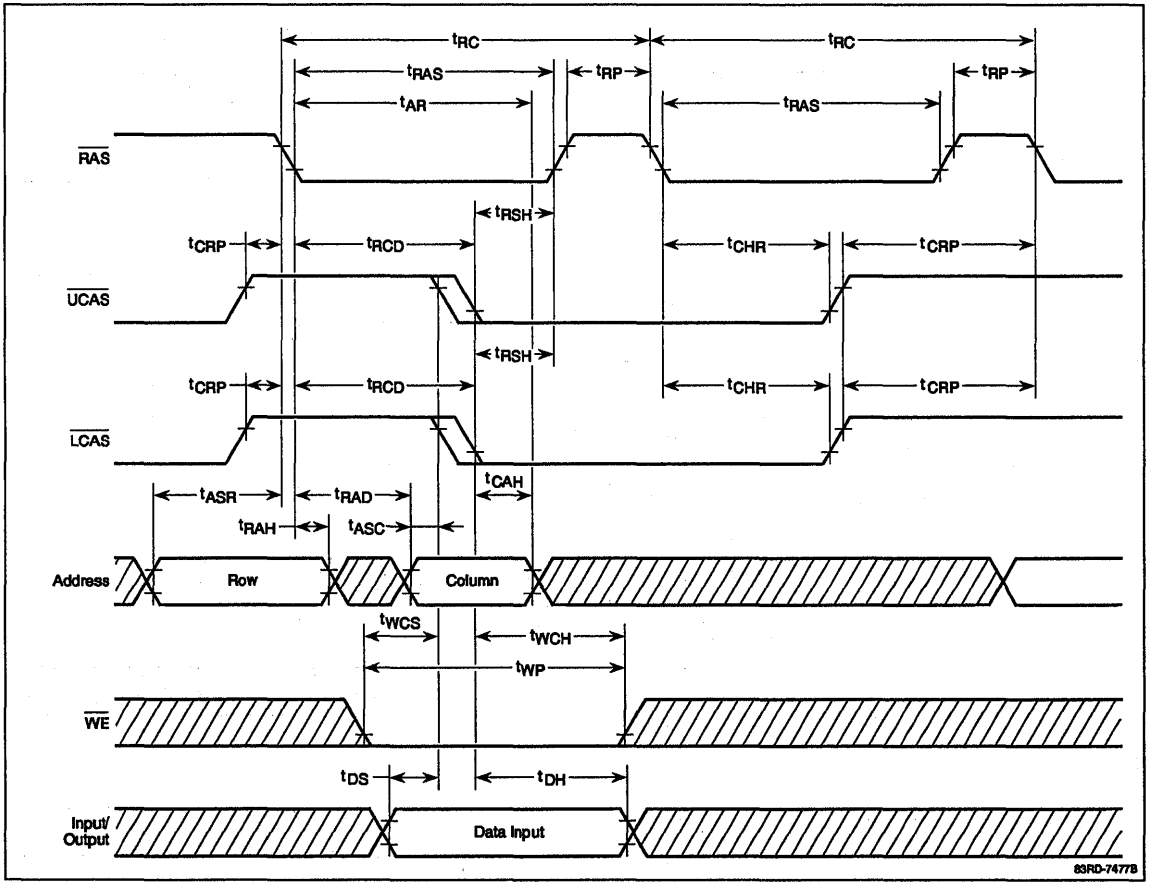
Hidden Refresh Cycle (Word Read Cycle)



7d

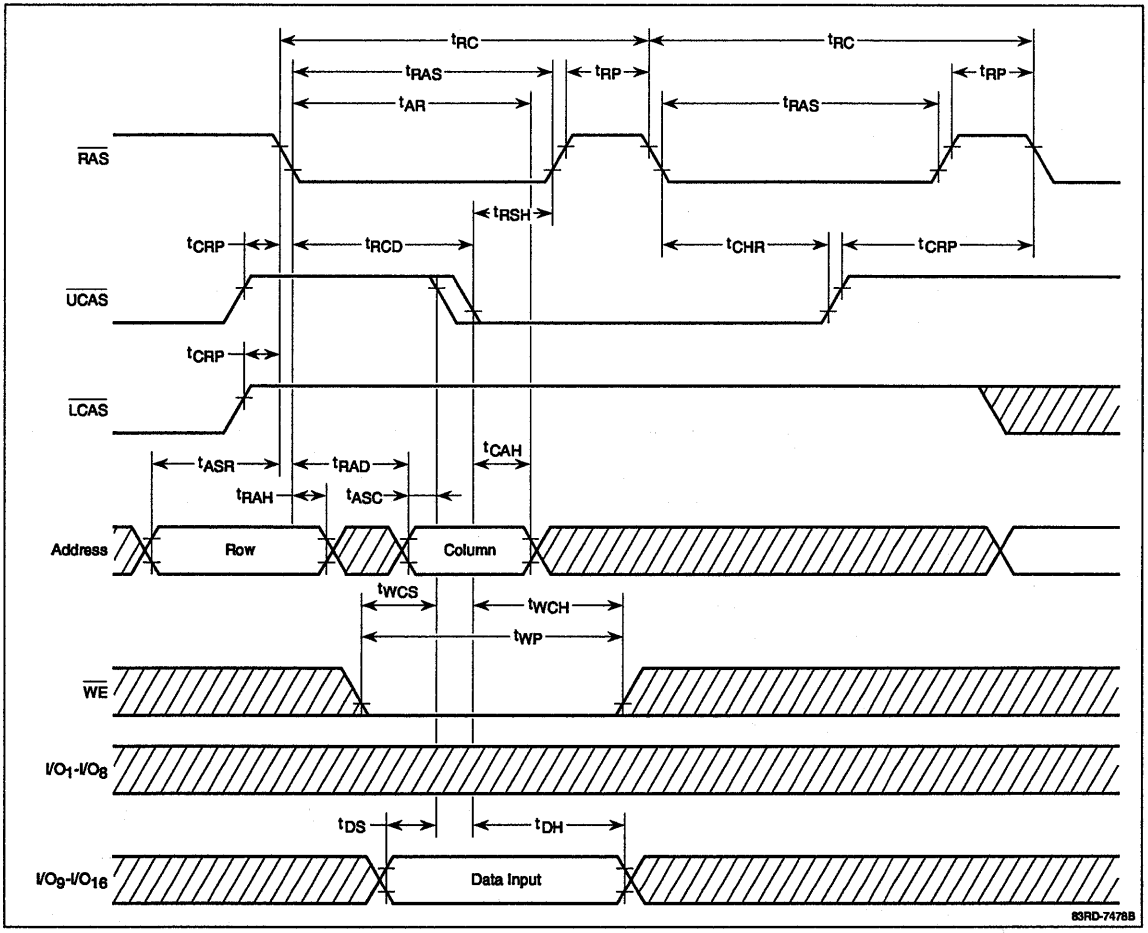
Timing Waveforms (cont)

Hidden Refresh Cycle (Word Write Cycle)



Timing Waveforms (cont)

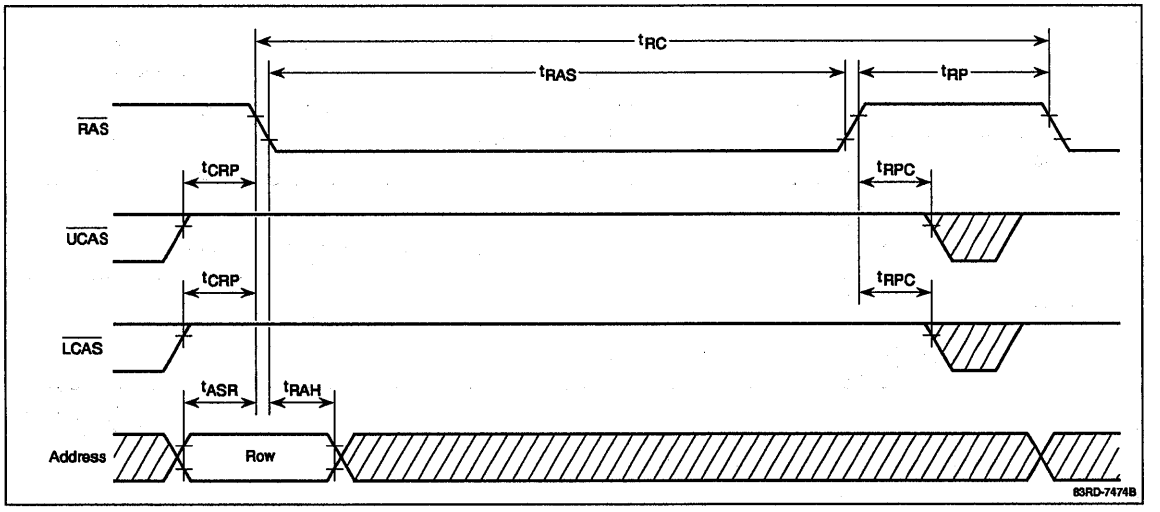
Hidden Refresh Cycle (Byte Write Cycle)



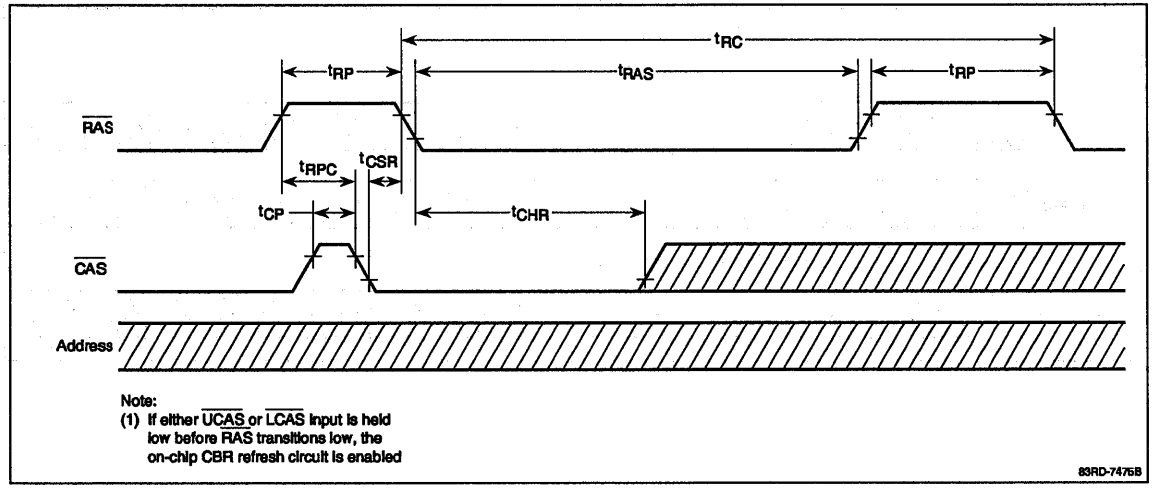
7d

Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



μPD424280A/L, 42S4280A/L
262,144 x 18-Bit
Dynamic CMOS RAM

Description

The μPD424280A/L and μPD42S4280A/L are fast-page dynamic RAMs organized as 262,144 words by 18 bits and designed to operate from a single power supply.

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
424280A	+5 V
424280L	+3.3 V
42S4280A	+5 V; self-refresh mode
42S4280L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{UCAS}$ and $\overline{LCAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, upper or lower byte data is held on the outputs by maintaining $\overline{UCAS}$ or $\overline{LCAS}$ low. Data outputs return to high impedance when either $\overline{UCAS}$ or $\overline{LCAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{UCAS}$ or $\overline{LCAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh address. $\overline{RAS}$-only refresh cycles will also refresh all memory locations.

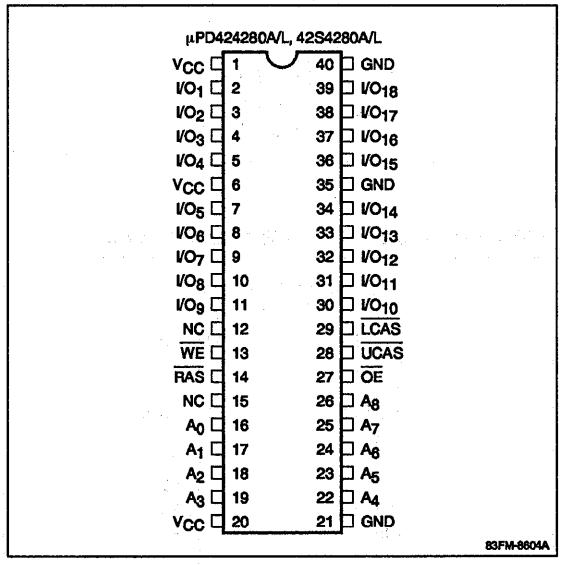
The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

- 262,144 by 18-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option
- Byte read/write control with UCAS and LCAS
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 512 refresh cycles every 8 ms
- 40-pin SOJ, 40-pin ZIP, and 44/40-pin TSOP plastic packaging

Pin Configurations

40-Pin Plastic SOJ



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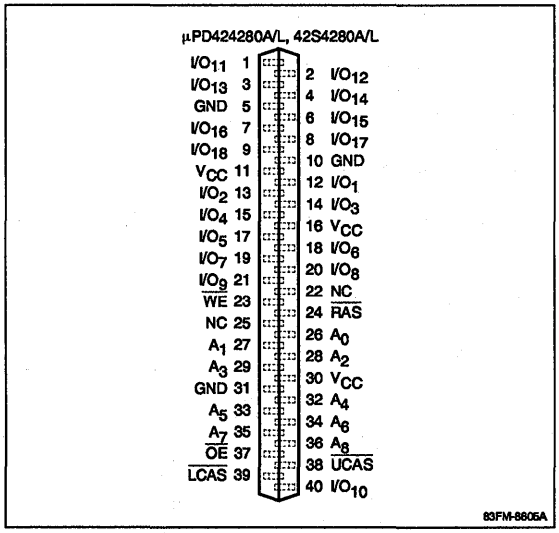
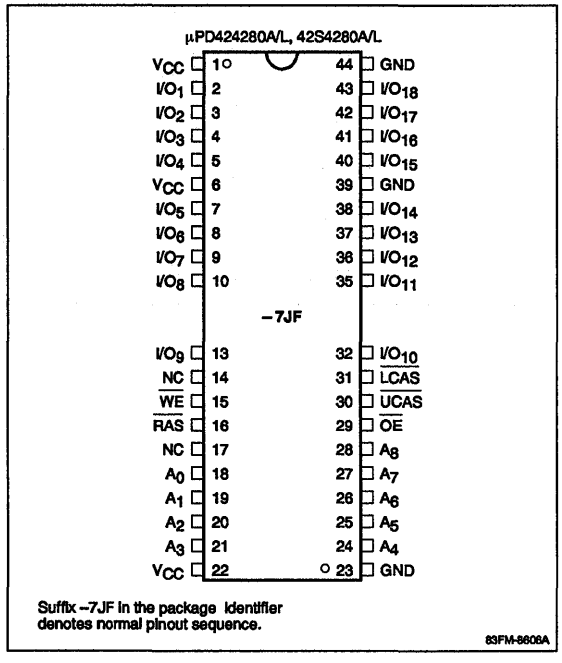
Pin Configurations (cont)

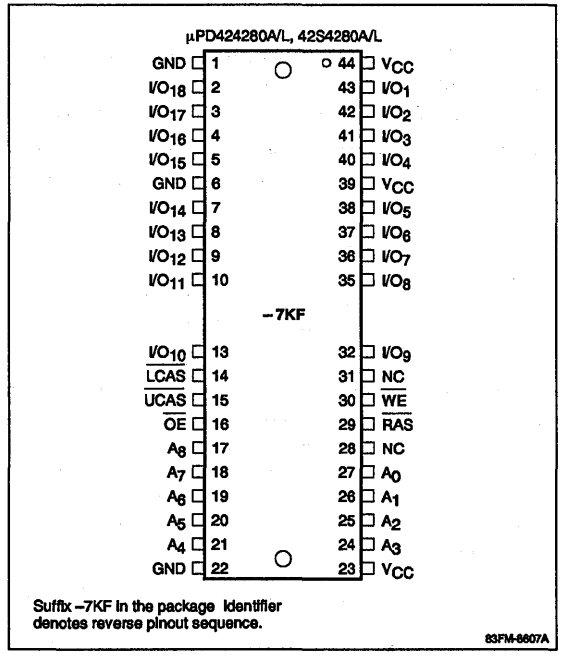
40-Pin Plastic ZIP



44/40-Pin Plastic TSOP (Normal Pinouts)



44/40-Pin Plastic TSOP (Reverse Pinouts)



Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_{18}	Data inputs and outputs
$\overline{LCAS}$, $\overline{UCAS}$	Column address strobes
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

Ordering Information, μPD424280A (+ 5-volt power)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Package
μPD424280ALE-60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD424280AV-60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-70	70 ns	45 ns		
V-80	80 ns	50 ns		
μPD424280AG5-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD424280AG5M-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD424280L (+ 3.3-volt power)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Package
μPD424280LLE-A60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD424280LV-A60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-A70	70 ns	45 ns		
V-A80	80 ns	50 ns		
μPD424280LG5-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD424280LG5M-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

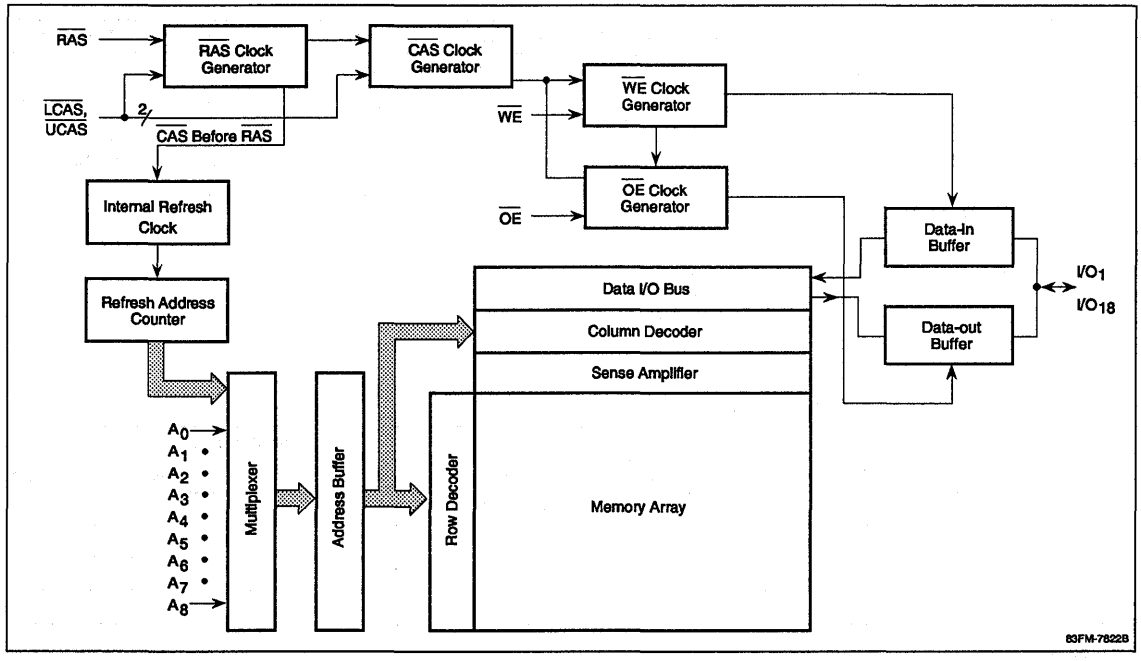
Ordering Information, μPD42S4280A (+ 5-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4280ALE-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4280AV-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic ZIP
V-70	70 ns	45 ns			
V-80	80 ns	50 ns			
μPD42S4280AG5-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns			
G5-80	80 ns	50 ns			
μPD42S4280AG5M-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns			
G5M-80	80 ns	50 ns			

Ordering Information, μPD42S4280L (+ 3.3-volt power; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4280LLE-A60	60 ns	40 ns	20 ns	100 μA	40-pin plastic SOJ
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			
μPD42S4280LV-A60	60 ns	40 ns	20 ns	100 μA	40-pin plastic ZIP
V-A70	70 ns	45 ns			
V-A80	80 ns	50 ns			
μPD42S4280LG5-A60	60 ns	40 ns	20 ns	100 μA	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns			
G5-A80	80 ns	50 ns			
μPD42S4280LG5M-A60	60 ns	40 ns	20 ns	100 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns			
G5M-A80	80 ns	50 ns			

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	I/O_1 - I/O_9	I/O_{10} - I/O_{18}
Standby	H	X	X	X	X	High-Z	High-Z
Refresh cycle	L	H	H	X	X	High-Z	High-Z
Byte read cycle	L	L	H	H	L	Data output	High-Z
	L	H	L	H	L	High-Z	Data output
Word read cycle	L	L	L	H	L	Data output	Data output
Byte write cycle	L	L	H	L	H	Data input	—
	L	H	L	L	H	—	Data input
Word write cycle	L	L	L	L	H	Data input	Data input
——	L	L	L	H	H	High-Z	High-Z

X = don't care.

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Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
5-volt devices	50 mA
3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_{16}

Recommended Operating Conditions

		5-Volt Devices			3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} +0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.5		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

Self-Refresh Current

T_A = 0 to +70°C; V_{CC} = +5 V ±10% (42S4280A) or +3.3 V ±0.3 V (42S4280L)

Symbol	42S4280A	42S4280L	Conditions
I_{CC7}	300 μA max	100 μA max	I/O pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. Other input pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. $t_{RAS} \geq 100$ μs

DC Characteristics; 5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				300	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

DC Characteristics; 3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			500	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				100	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–5		5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–5		5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

AC Characteristics

T_A = 0 to +70°C

μPD424280A, 42S4280A: V_{CC} = +5.0 V ±10%

μPD424280L, 42S4280L: V_{CC} = +3.3 V ±0.3 V

		-60		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5)		160		150		140	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
	I_{CC1} (+3.3)		150		140		130		
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5)		160		150		140	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
	I_{CC3} (+3.3)		150		140		130		
Operating current, fast-page cycle, average	I_{CC4} (+5)		110		100		90	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
	I_{CC4} (+3.3)		110		100		90		
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5)		160		150		140	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
	I_{CC5} (+3.3)		160		150		140		
Access time from column address	t_{AA}		30		35		40	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 3, 4, 7, 8, 16)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		ns	(Note 15)
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	–35		–40		–50		ns	For 42S4280A/L only

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	(Notes 4, 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		75		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		50		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 13)
Masked write hold time referenced to $\overline{RAS}$	t_{MRH}	0		0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	(Note 9)
Output disable from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t_{PC}	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with exended data output	t_{PRWC}	85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 3, 4, 7, 8)

AC Characteristics (cont)

Parameter	Symbol	-60		-70		-80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		10		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		μs	For 42S4280A/L
Random read or write cycle time	t_{RC}	120		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	120		130		150		ns	For 42S4280A/L
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Read-modify-write cycle time	t_{RWC}	165		175		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Rise and fall times	t_T	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		ns	(Note 14)

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Write command pulse width	t_{WP}	15		15		15		ns	(Note 12)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF. For 3.3-volt devices, V_{OH} = 2.0 V and V_{OL} = 0.8 V (ac reference levels).

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max).
If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of one of the $\overline{CAS}$ signals for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

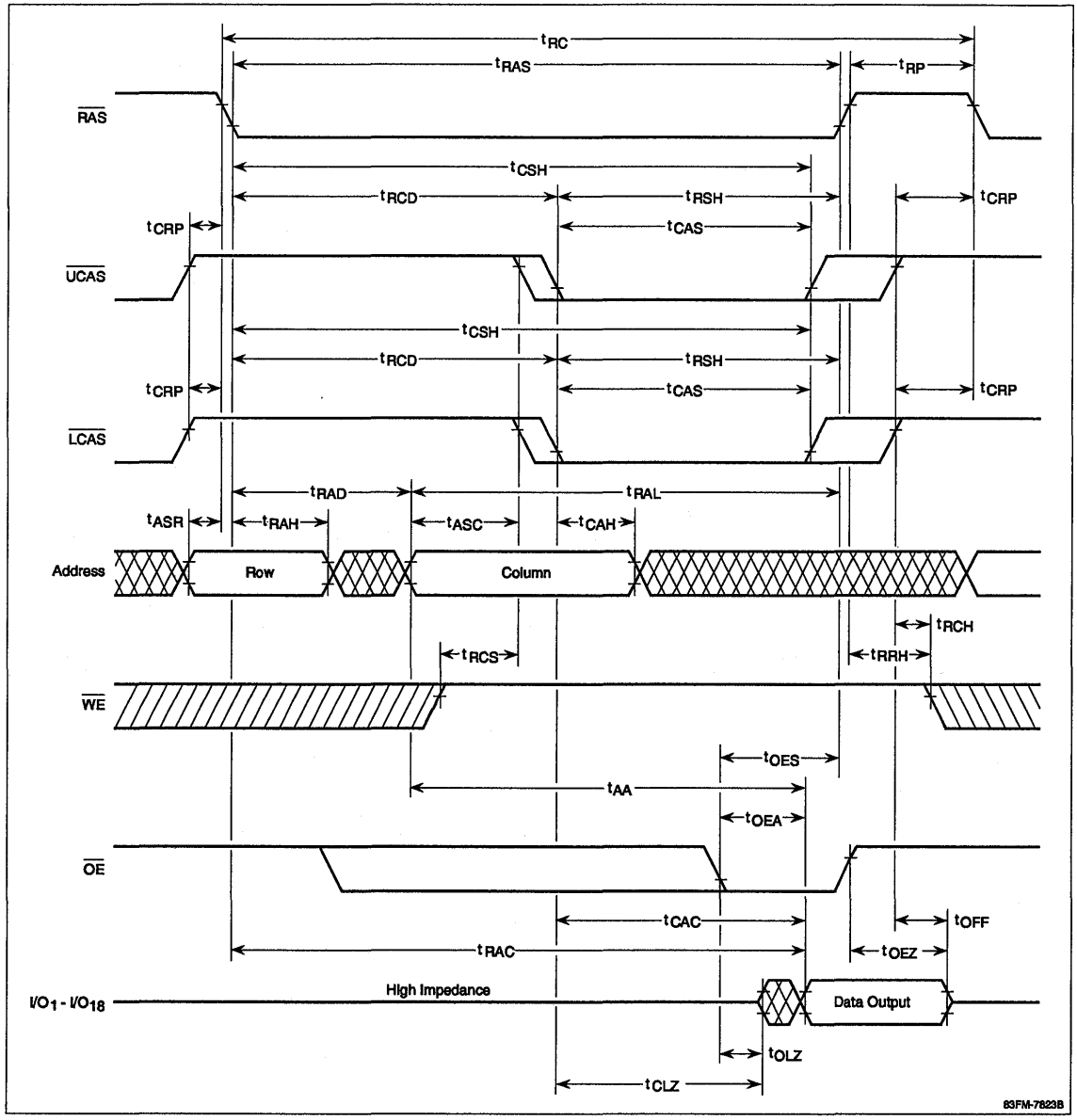
(14) t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD} and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) Holding $\overline{LCAS}$ or $\overline{UCAS}$ low prior to $\overline{RAS}$ going negative will initiate a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (t_{CSR} and t_{CHR} must be satisfied).

(16) The first $\overline{CAS}$ falling edge is used as a reference for the start of t_{ACP} ($\overline{CAS}$ precharge access time).

Timing Waveforms

Word Read Cycle



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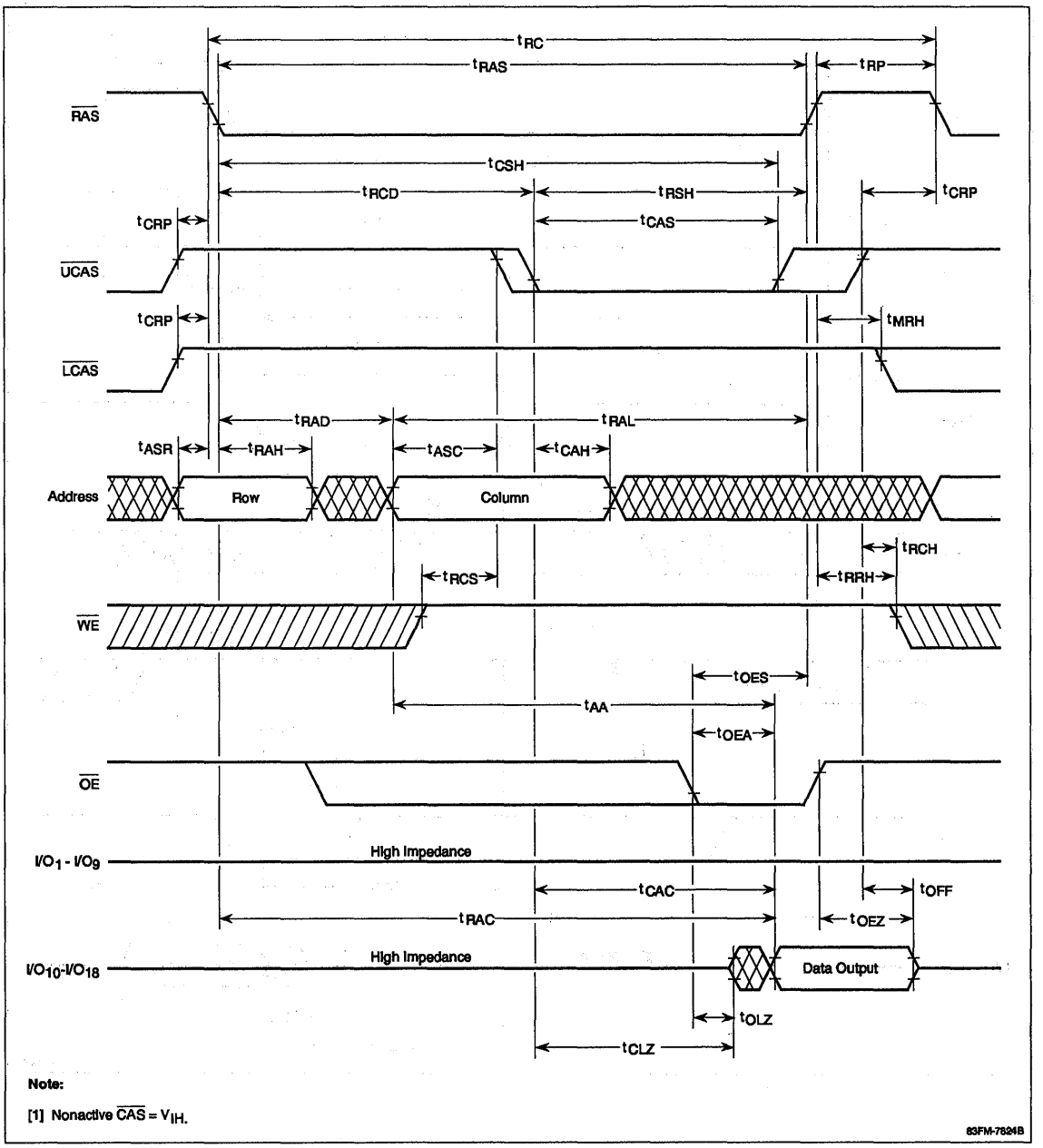
Timing Waveforms (cont)

Byte Read Cycle



Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

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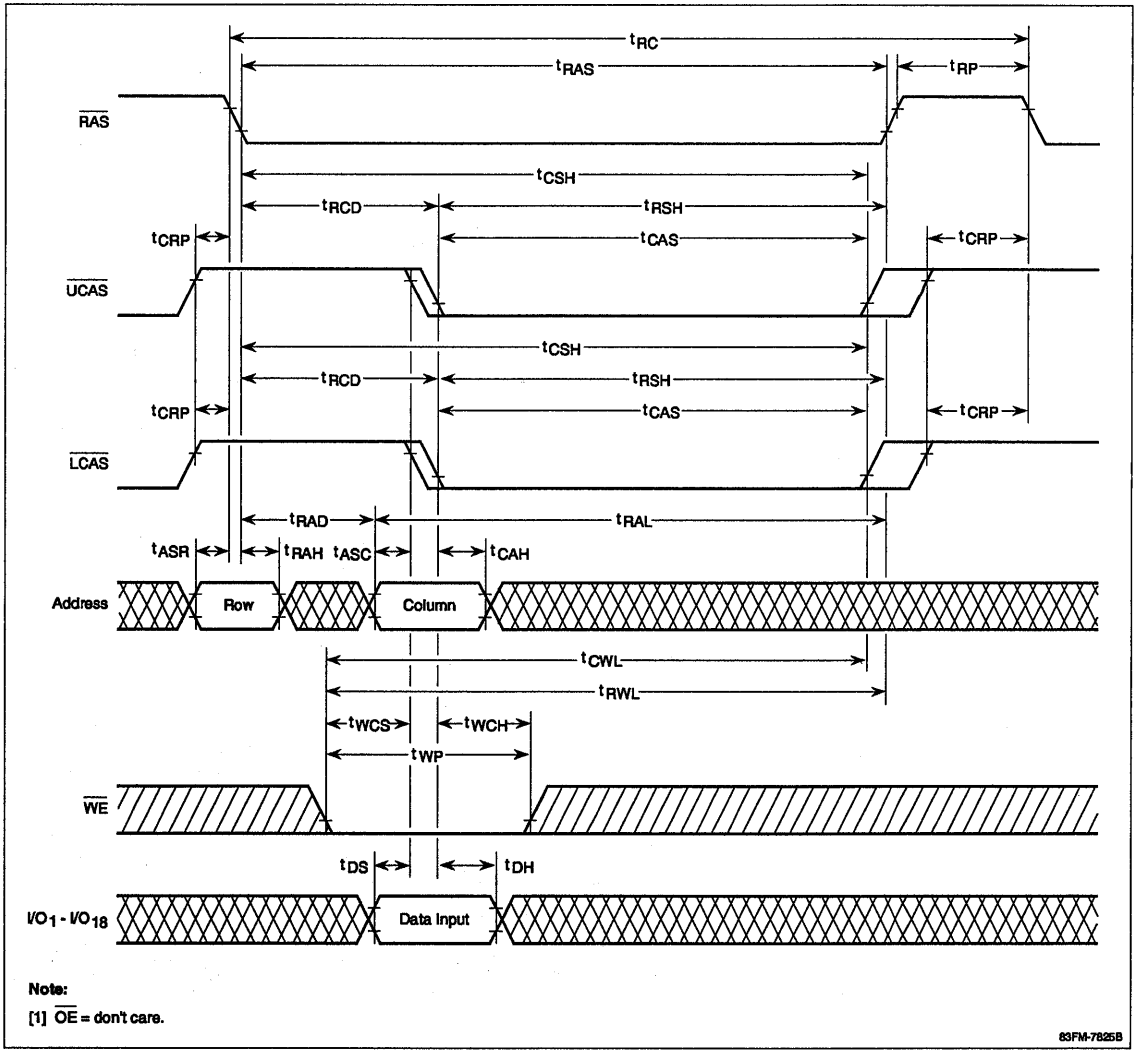
Timing Waveforms (cont)

Word Early-Write Cycle



Note:

[1] $\overline{OE}$ = don't care.

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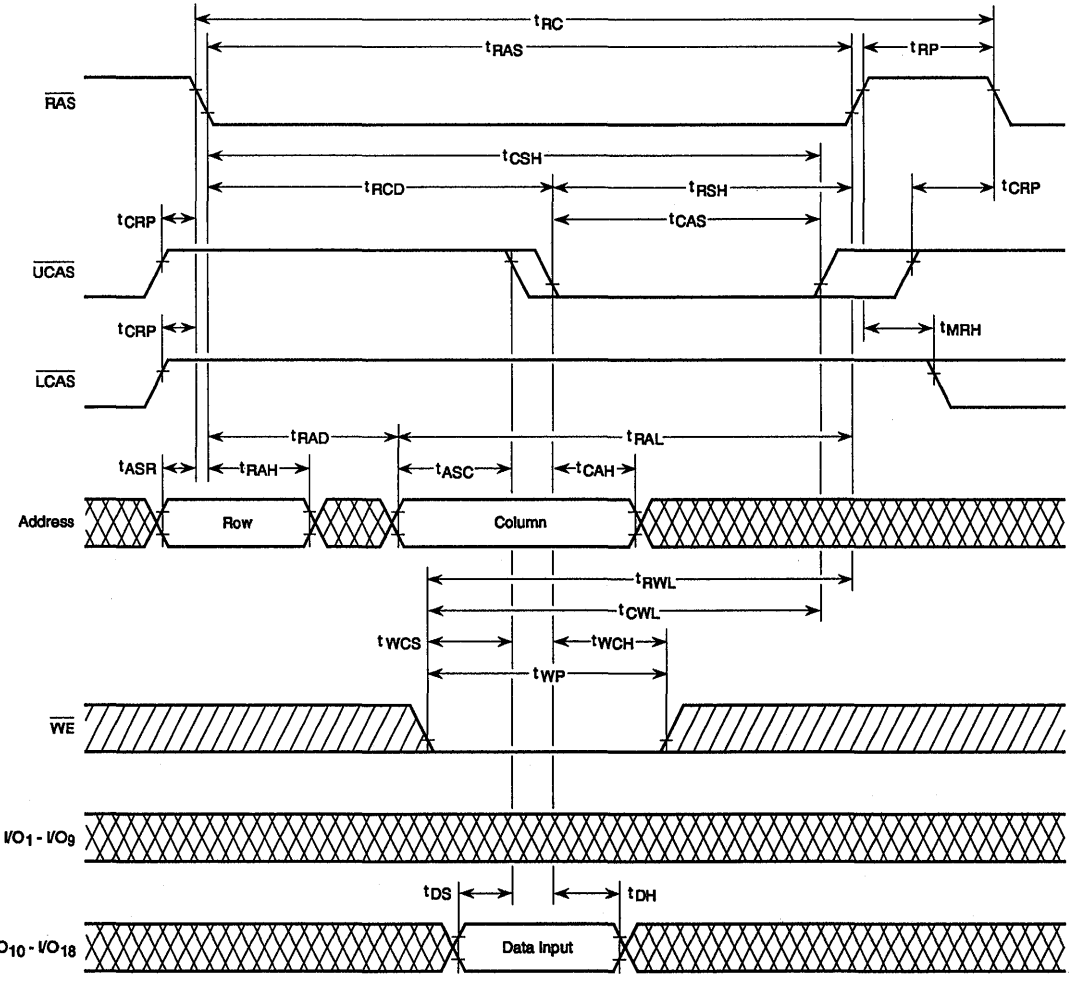
Timing Waveforms (cont)

Byte Early-Write Cycle



Notes:

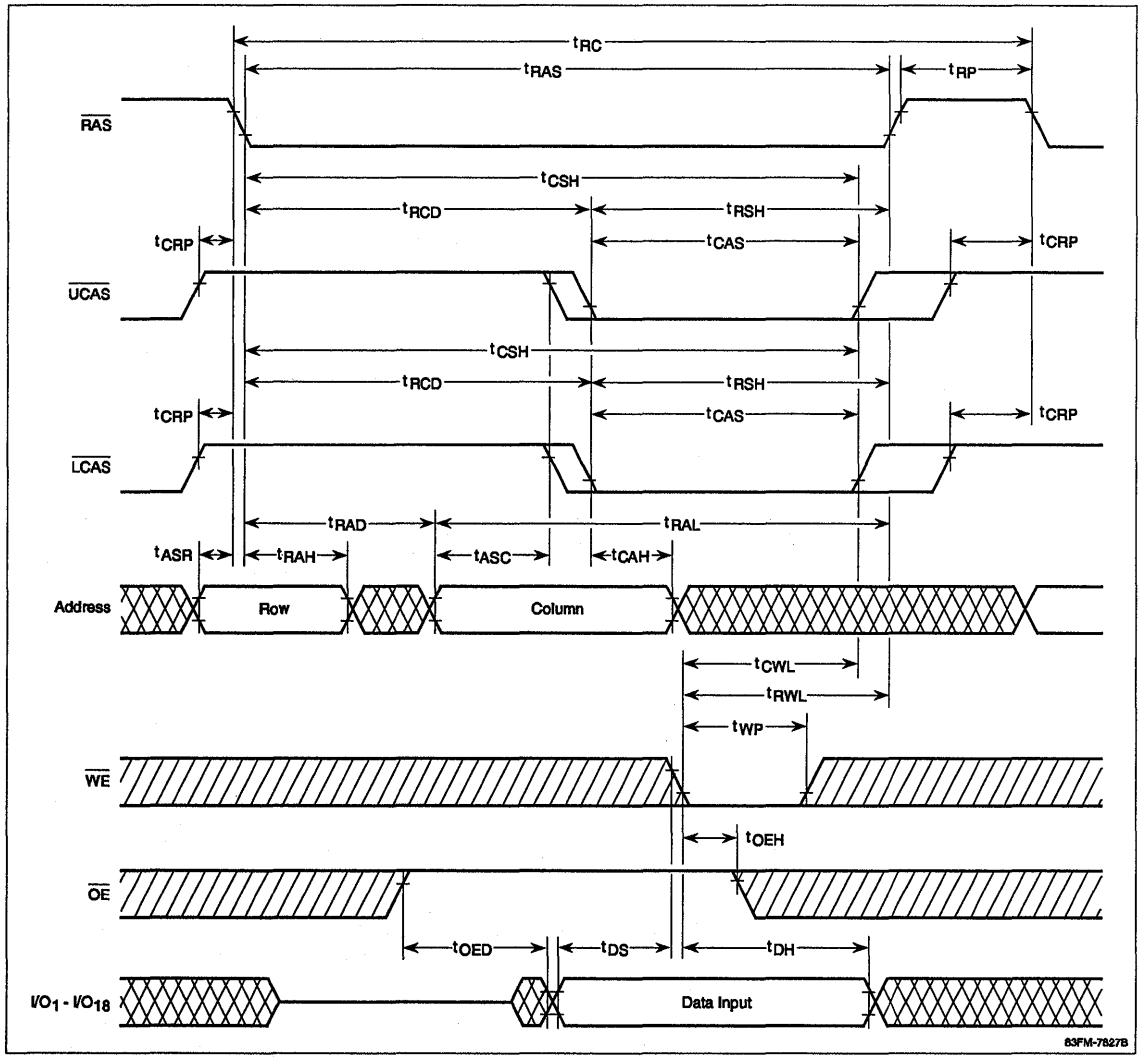
[1] Nonactive $\overline{CAS}$ = V_{IH}.

[2] $\overline{OE}$ = don't care.

83FM-7828B

Timing Waveforms (cont)

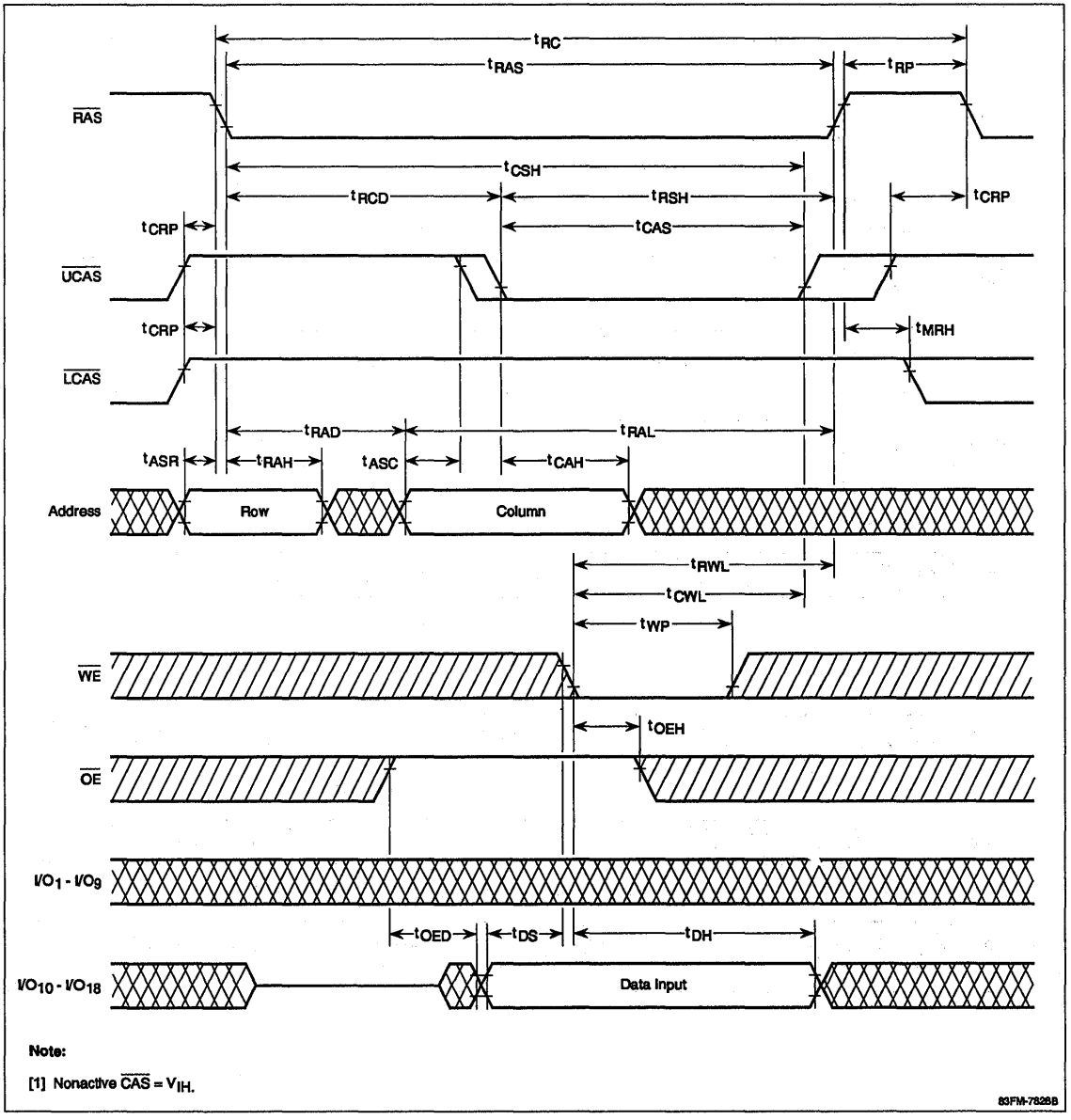
Word Late-Write Cycle



7e

Timing Waveforms (cont)

Byte Late-Write Cycle



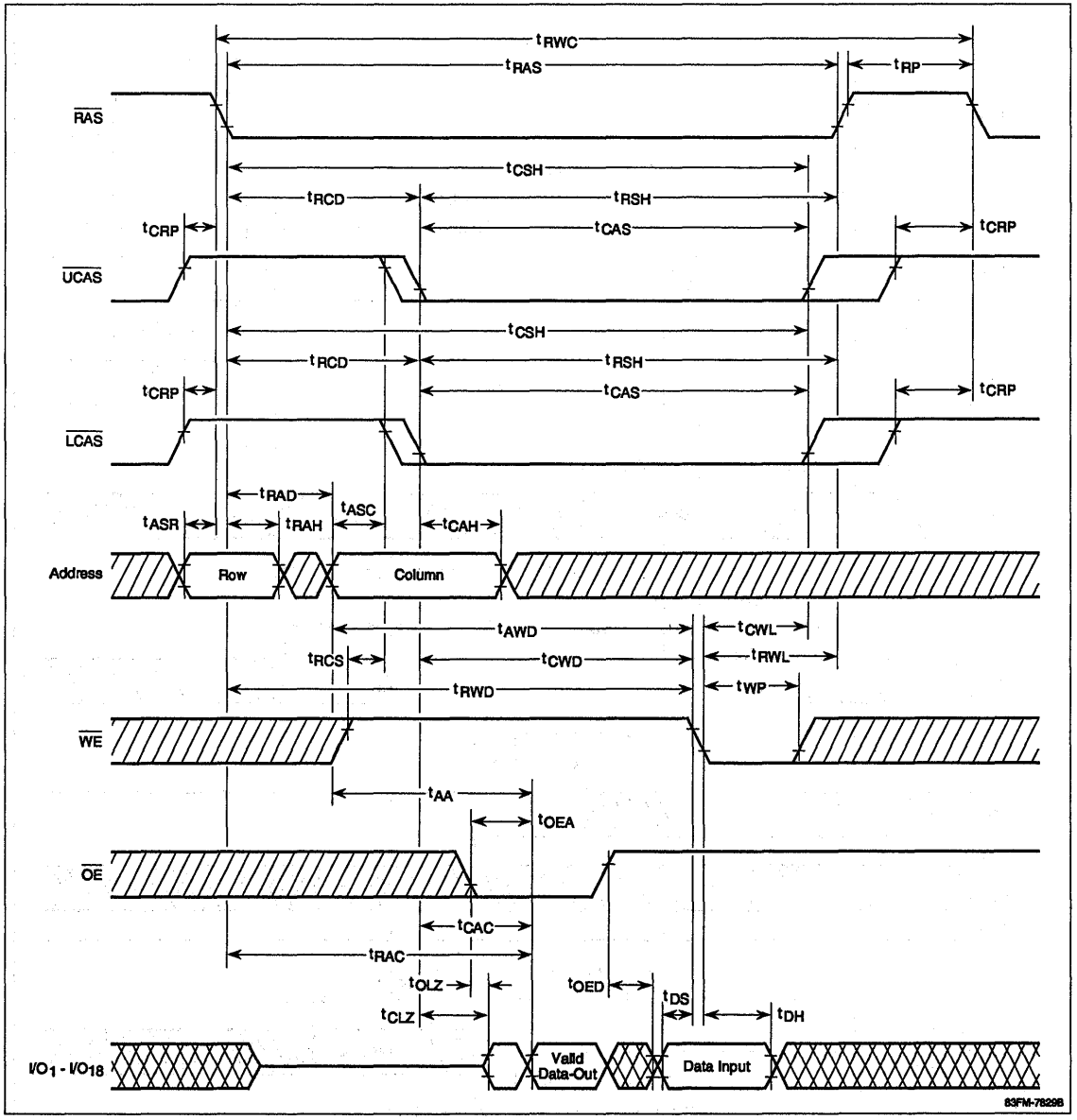
Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

83FM-7828B

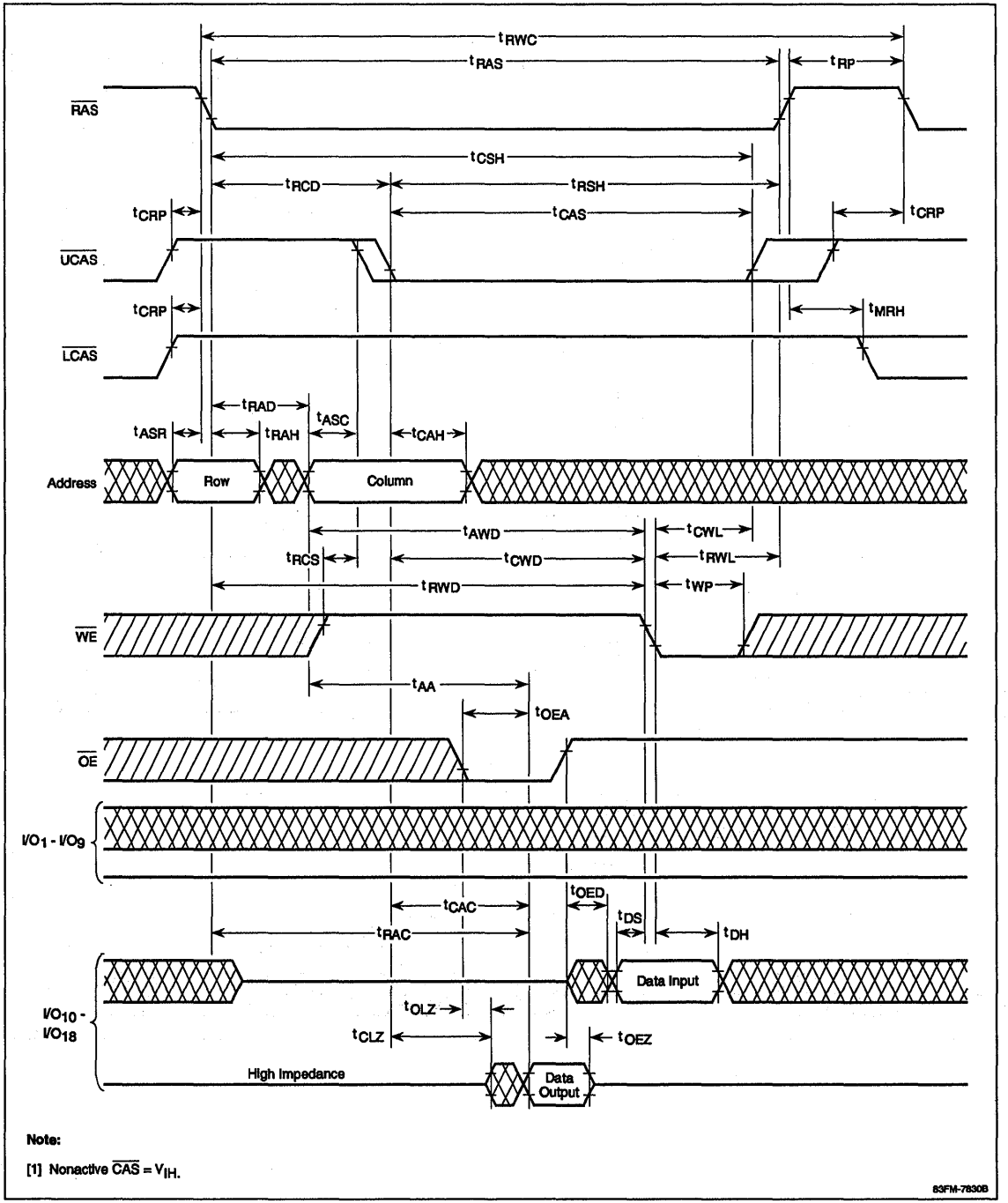
Timing Waveforms (cont)

Word Read-Modify-Write Cycle



Timing Waveforms (cont)

Byte Read-Modify-Write Cycle



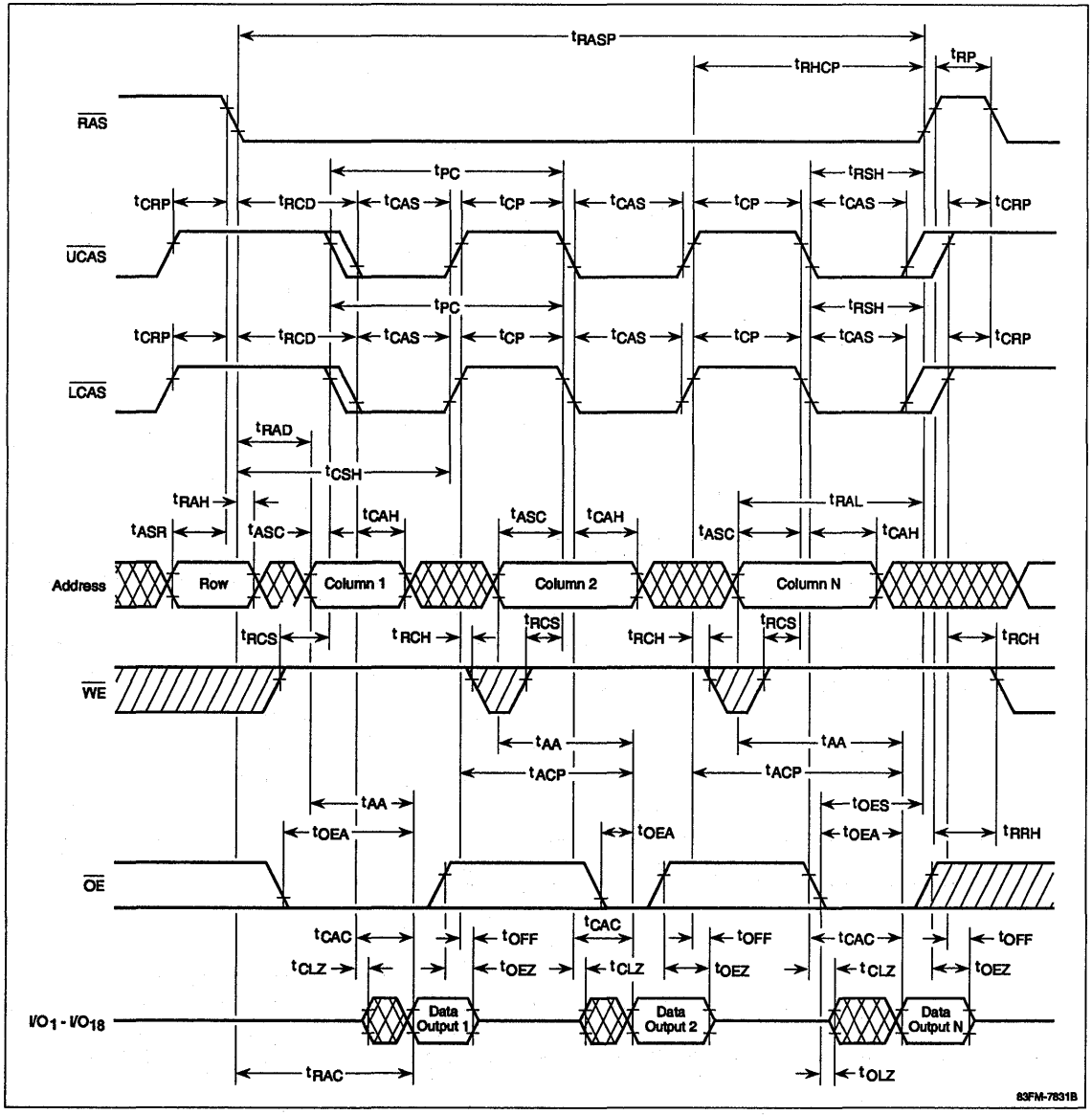
Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

83FM-7830B

Timing Waveforms (cont)

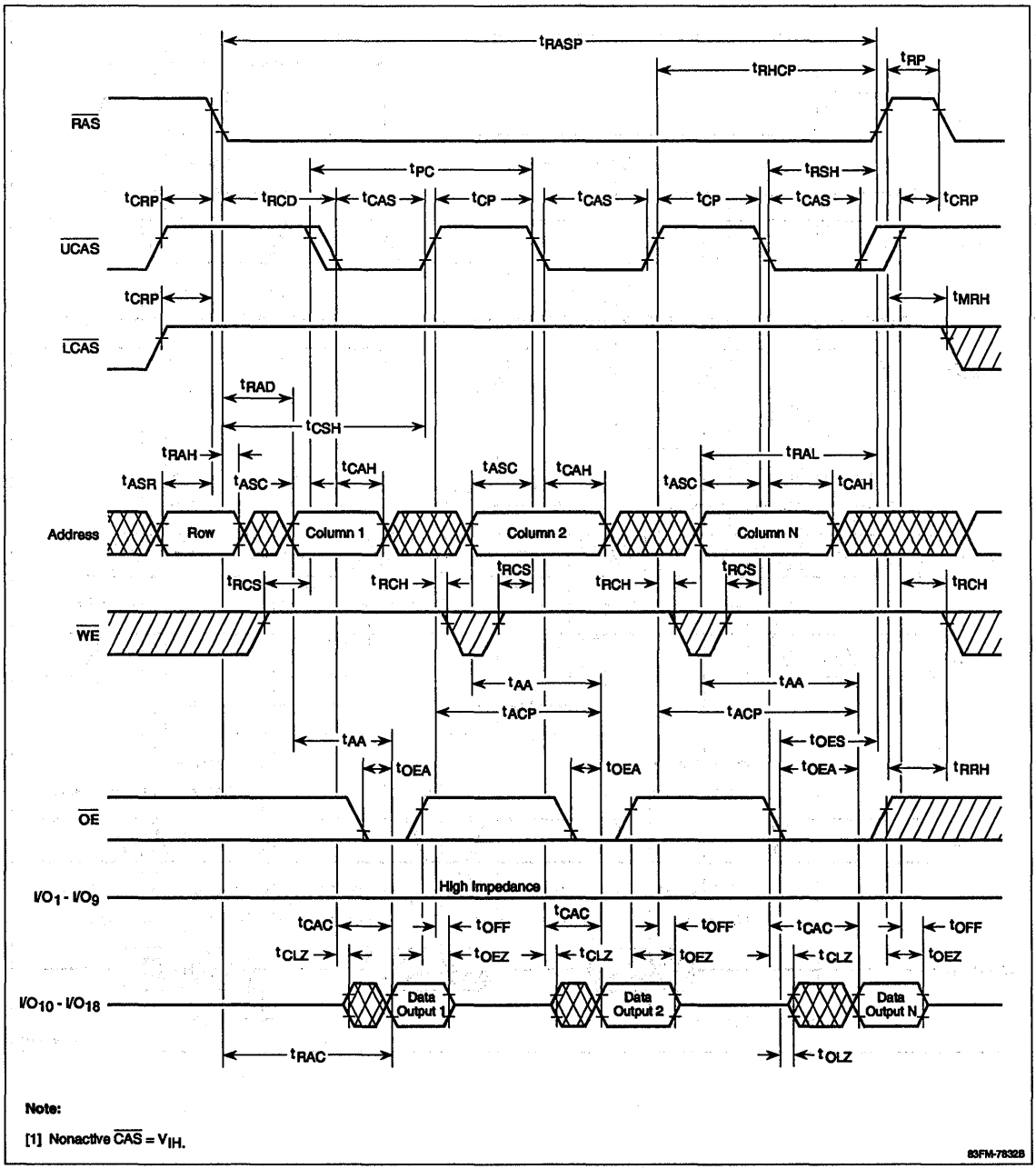
Word Fast-Page Read Cycle



7e

Timing Waveforms (cont)

Byte Fast-Page Read Cycle



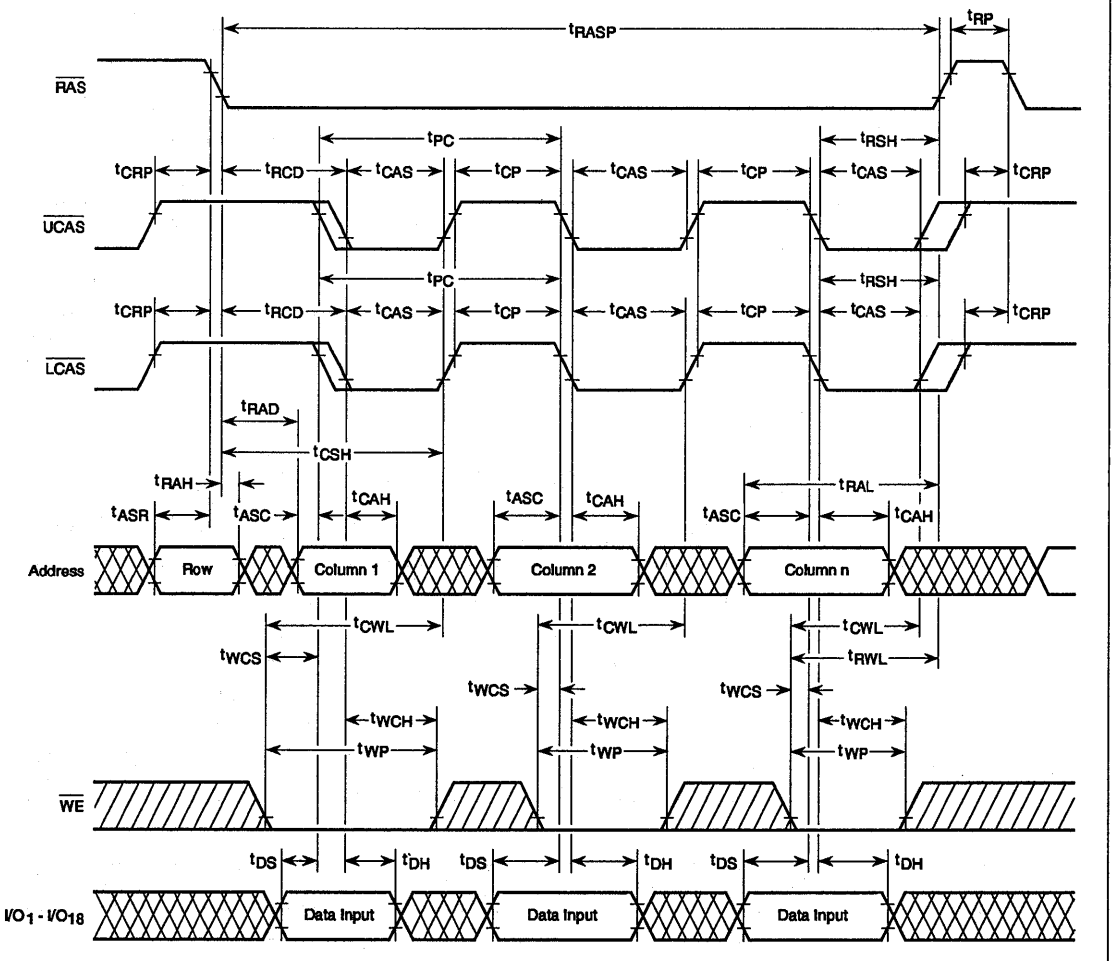
Note:

[1] Nonactive $\overline{CAS}$ = V_{IH}.

83FM-7832B

Timing Waveforms (cont)

Word Fast-Page Early-Write Cycle



Note:

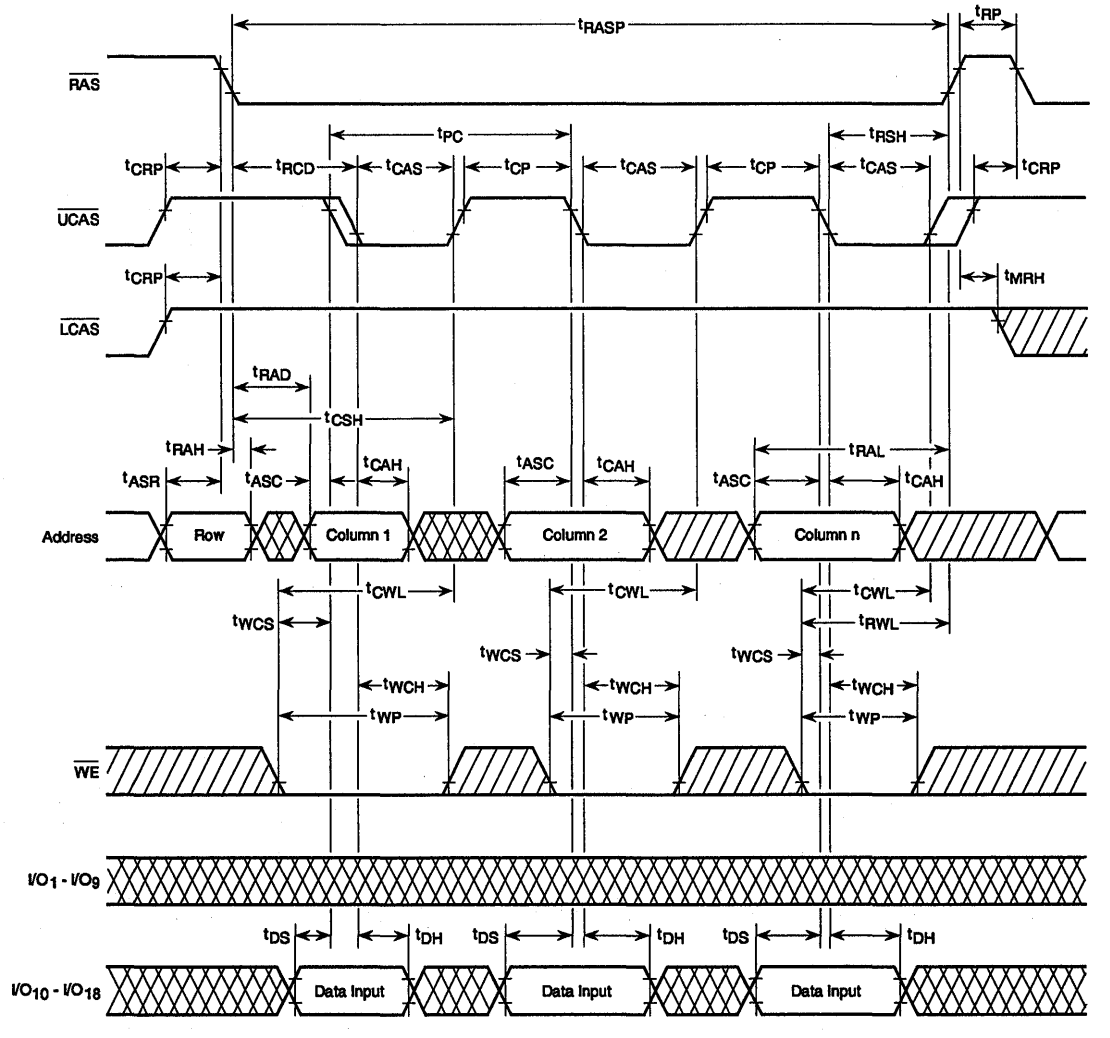
[1] $\overline{OE}$ = don't care.

89FM-7833B

7e

Timing Waveforms (cont)

Byte Fast-Page Early-Write Cycle



Notes:

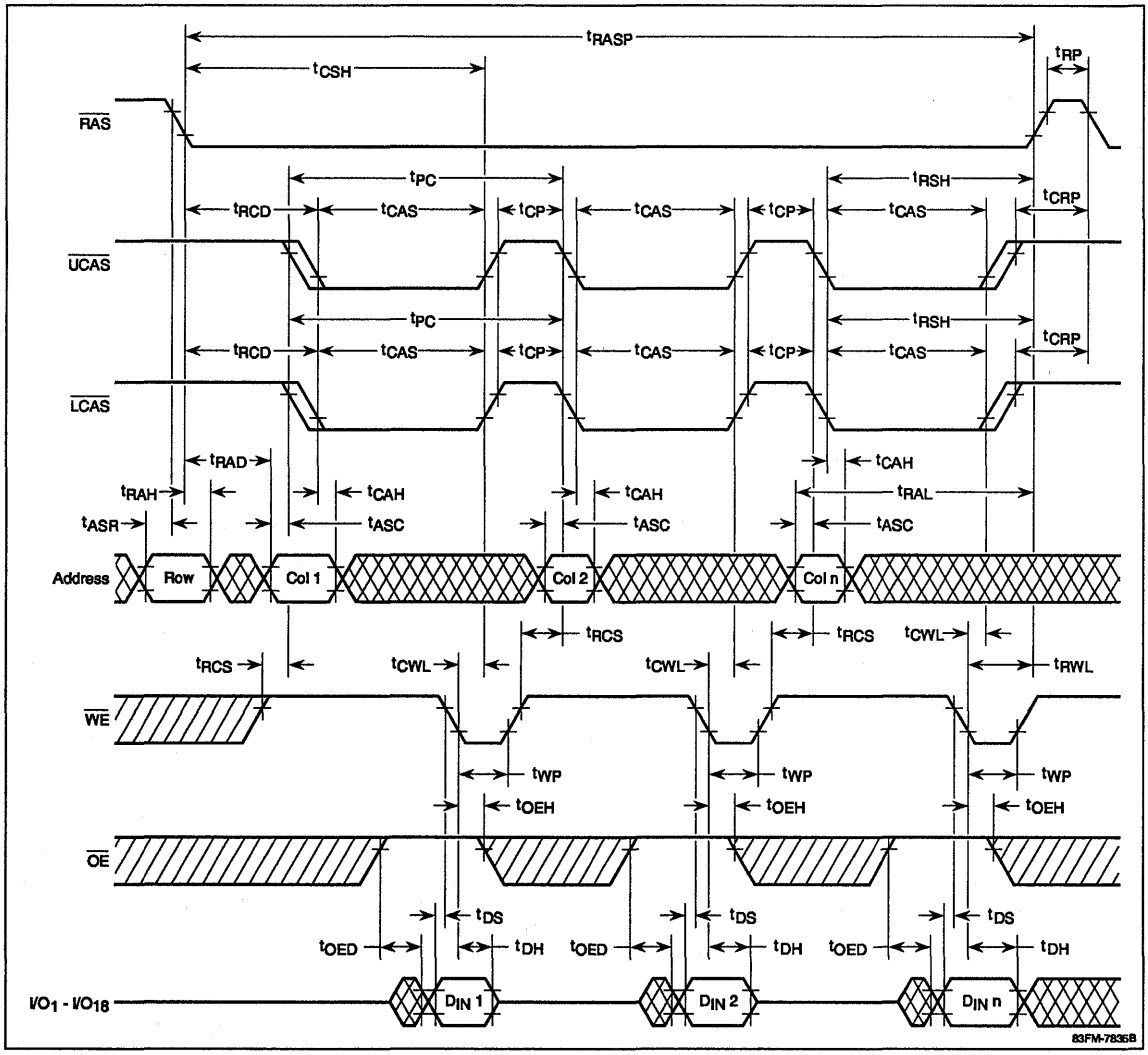
[1] Nonactive $\overline{CAS} = V_{IH}$.

[2] $\overline{OE}$ = don't care.

83FM-7834B

Timing Waveforms (cont)

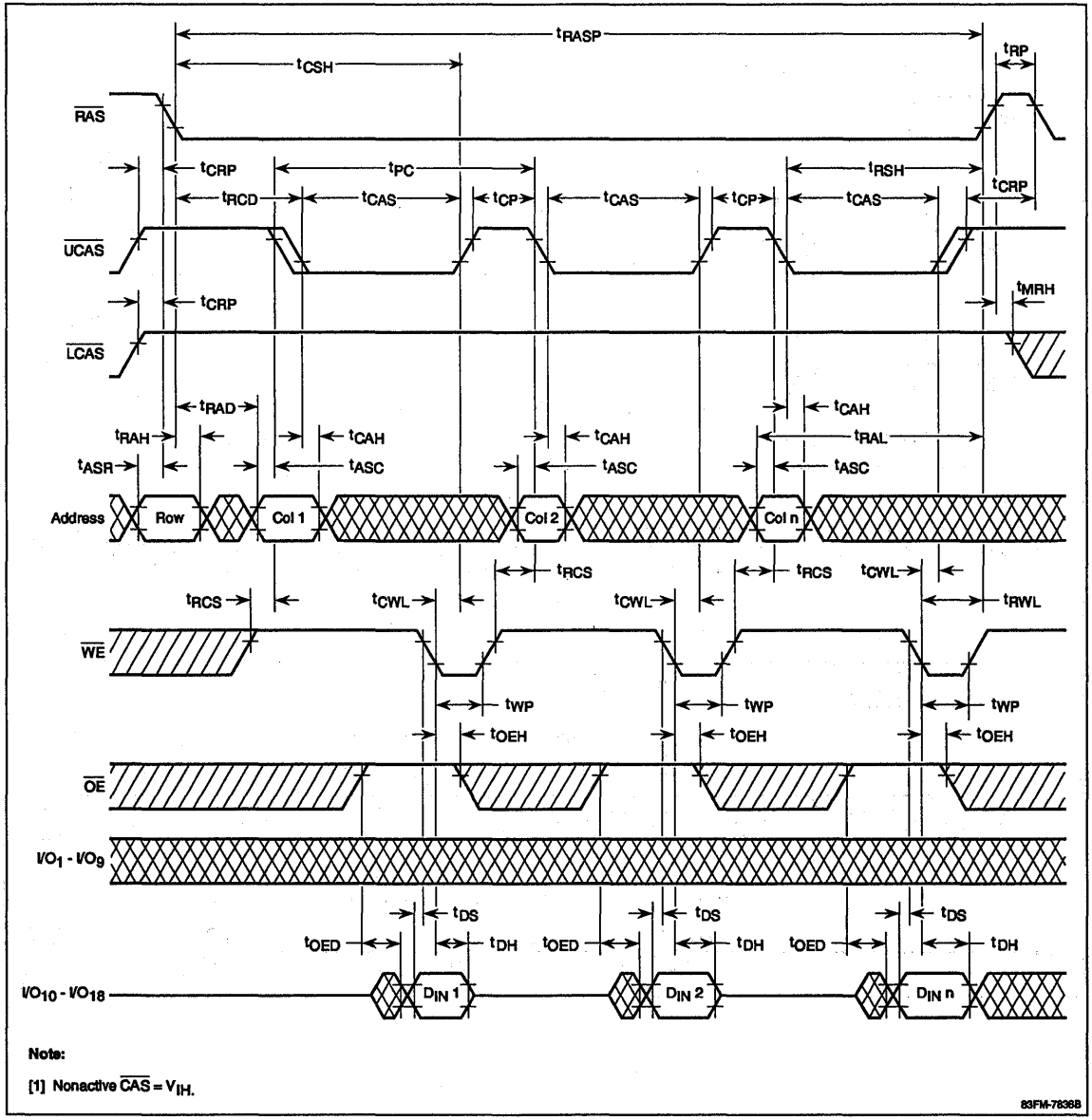
Word Fast-Page Late-Write Cycle



7e

Timing Waveforms (cont)

Byte Fast-Page Late-Write Cycle



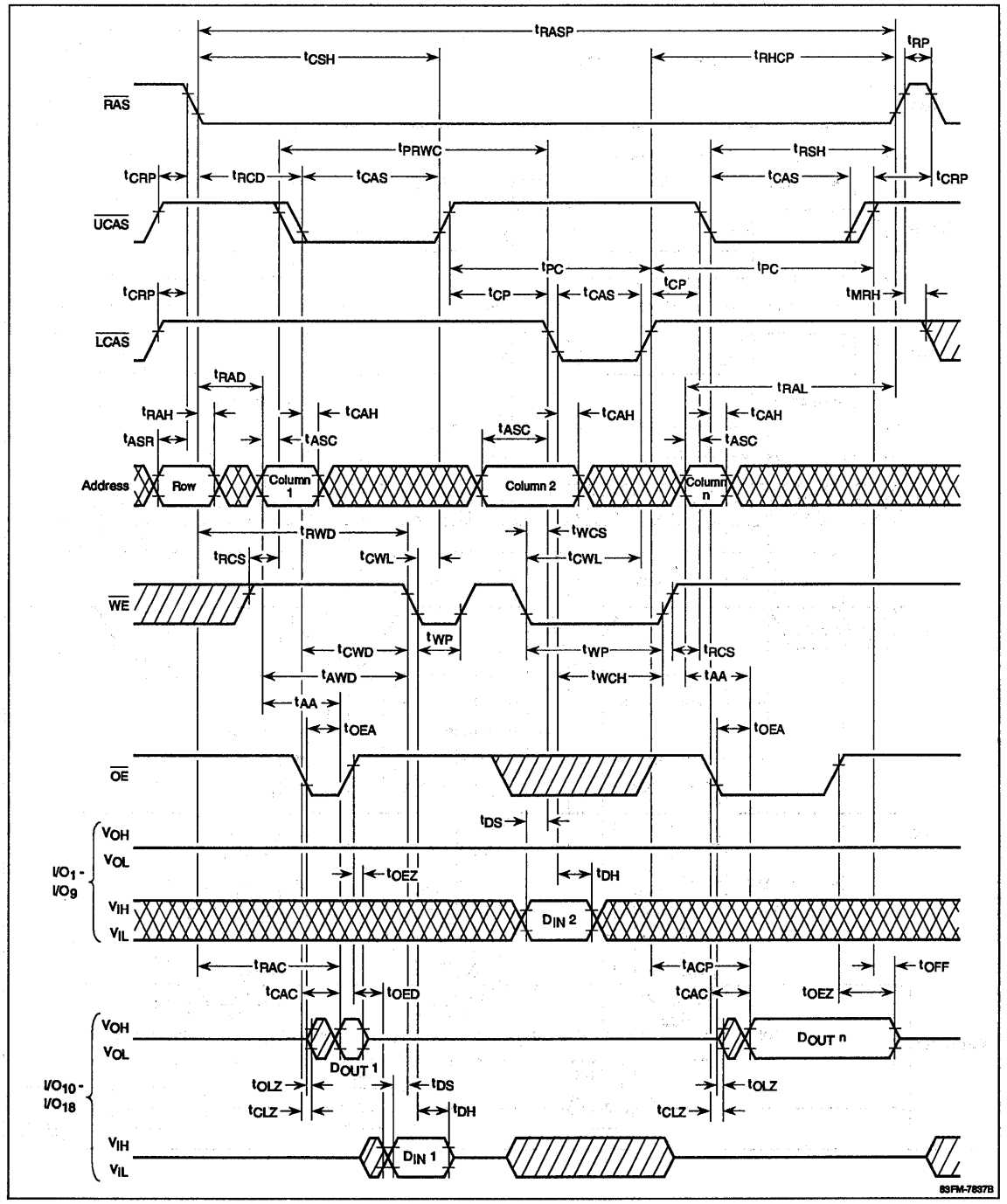
Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

83FM-7838B

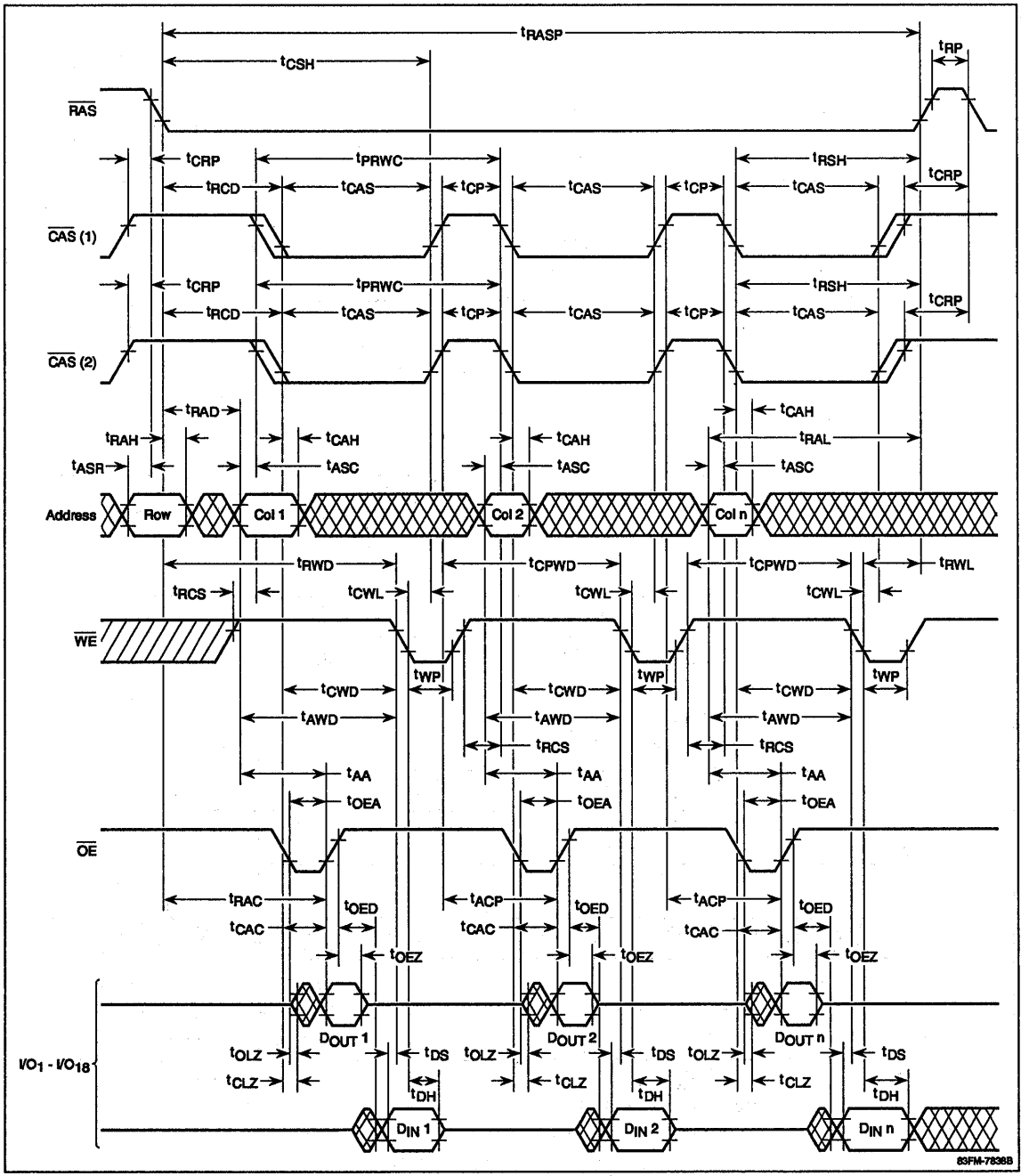
Timing Waveforms (cont)

Byte Fast-Page Read/Write Cycle



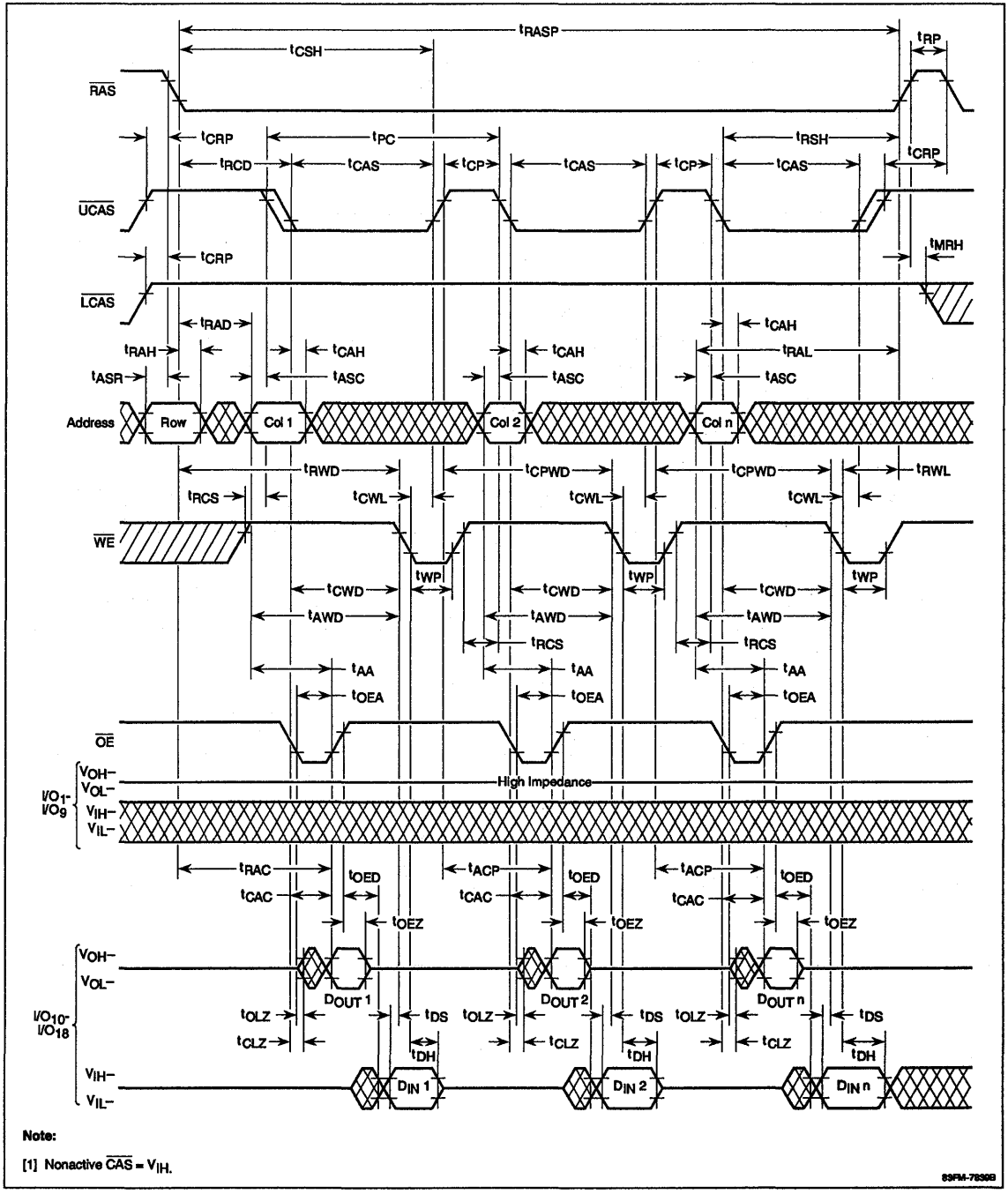
Timing Waveforms (cont)

Word Fast-Page Read-Modify-Write Cycle



Timing Waveforms (cont)

Byte Fast-Page Read-Modify-Write Cycle

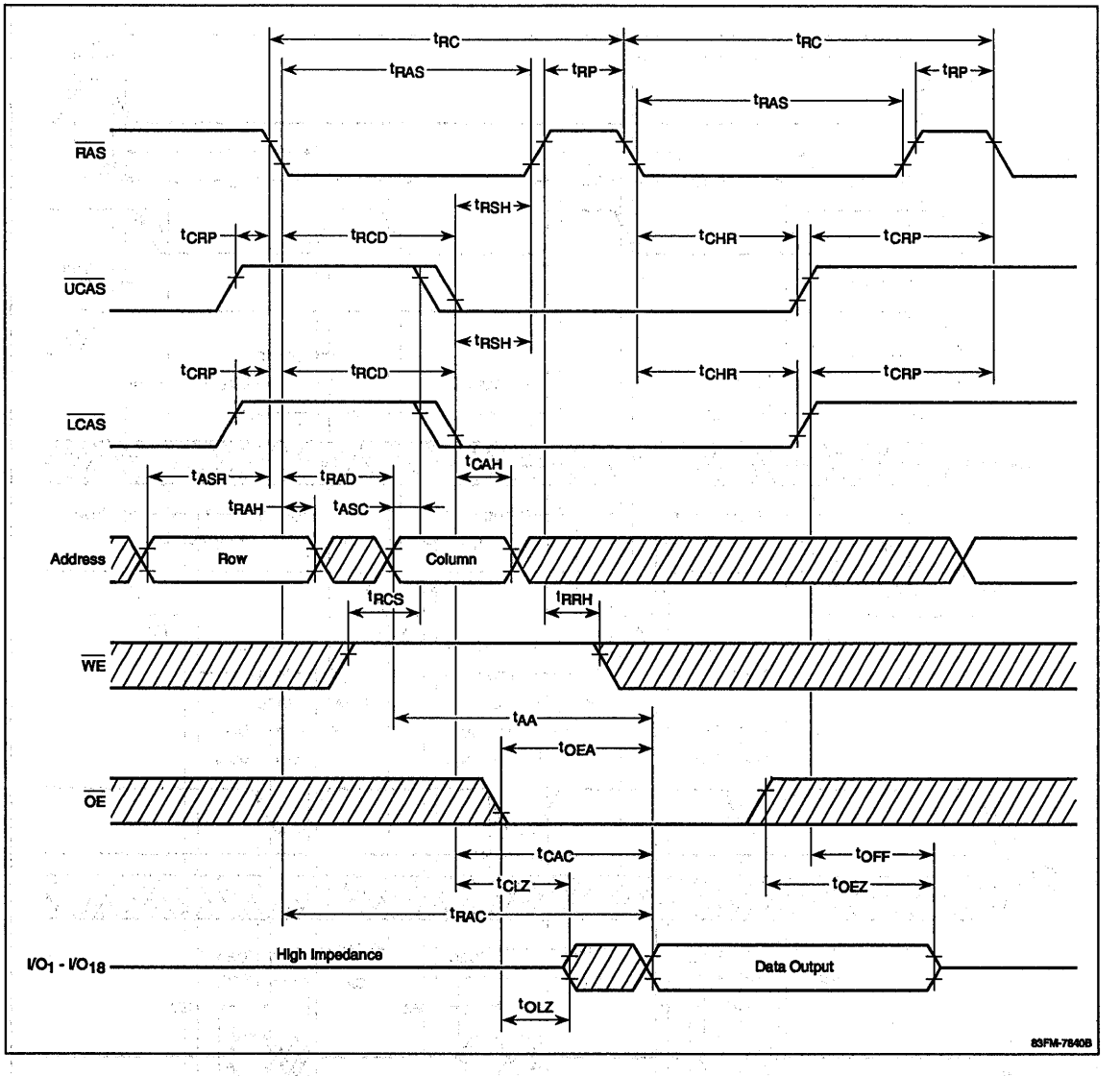


Note:

[1] Nonactive $\overline{CAS}$ = V_{IH}.

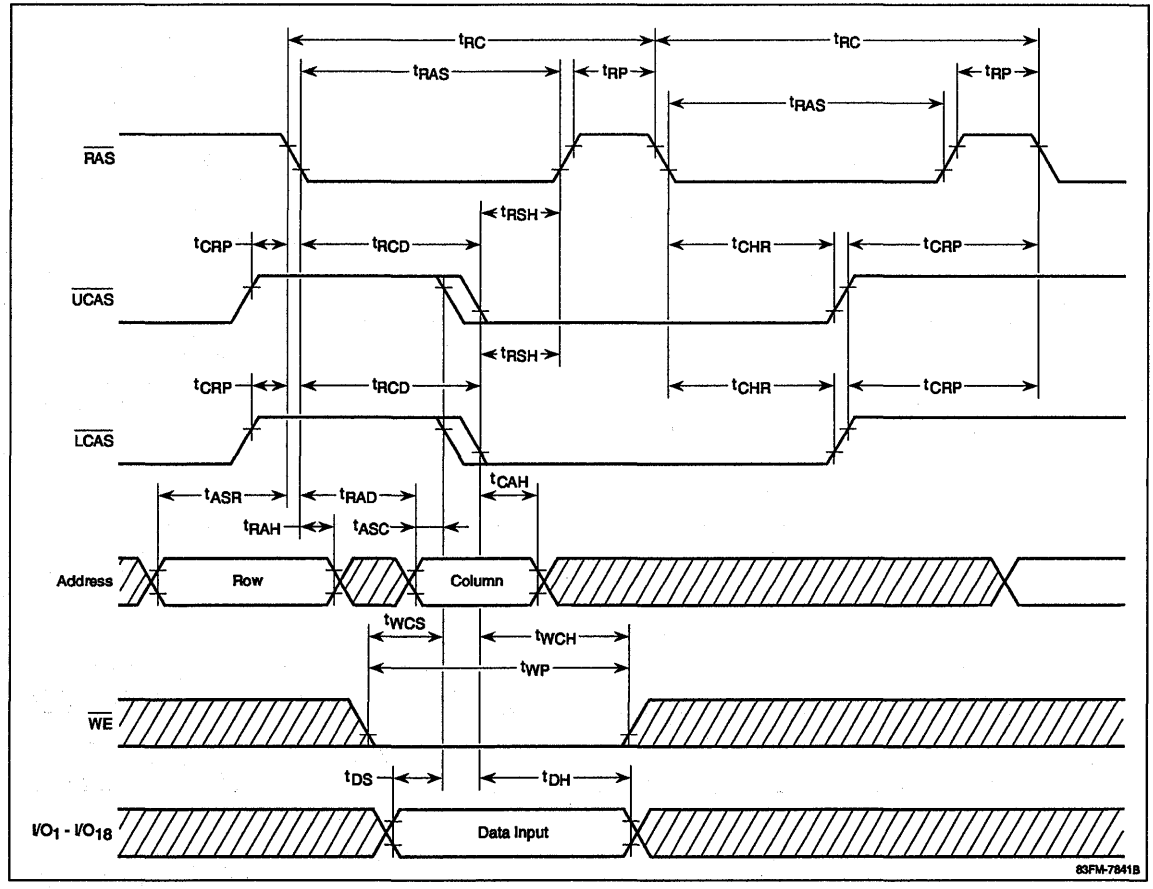
Timing Waveforms (cont)

Hidden-Refresh Cycle (Word Read Cycle)



Timing Waveforms (cont)

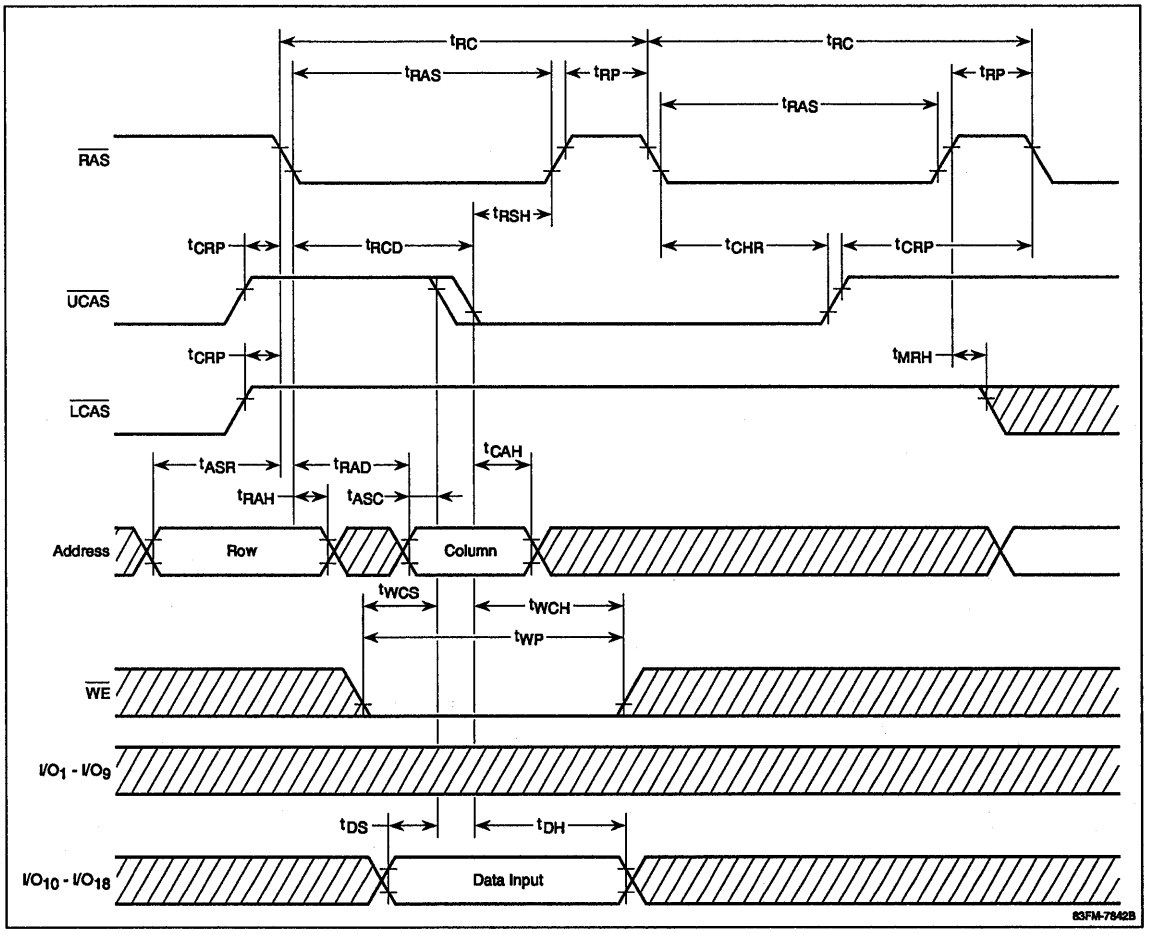
Hidden-Refresh Cycle (Word Write Cycle)



7e

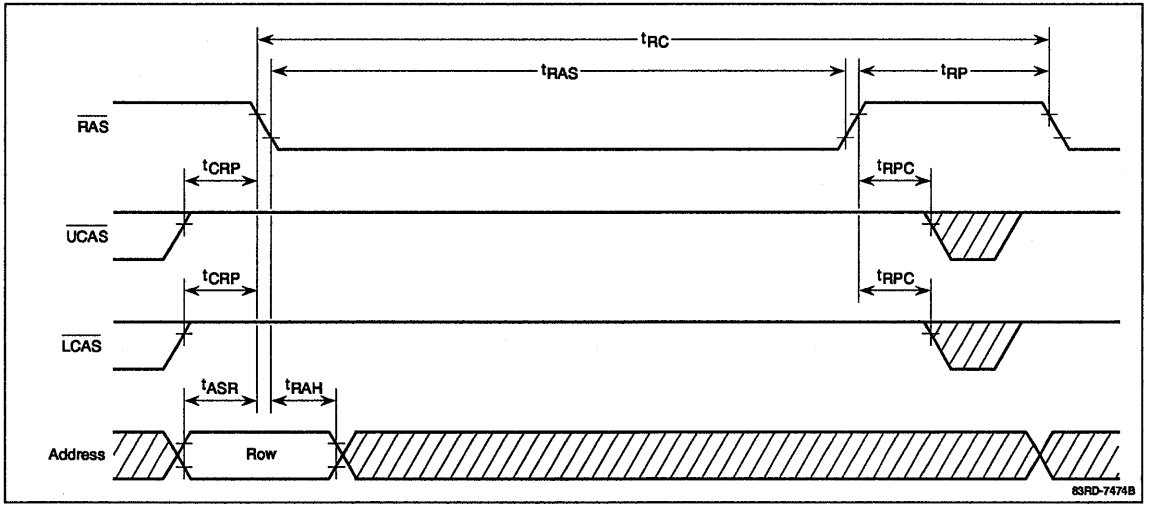
Timing Waveforms (cont)

Hidden-Refresh Cycle (Byte Write Cycle)

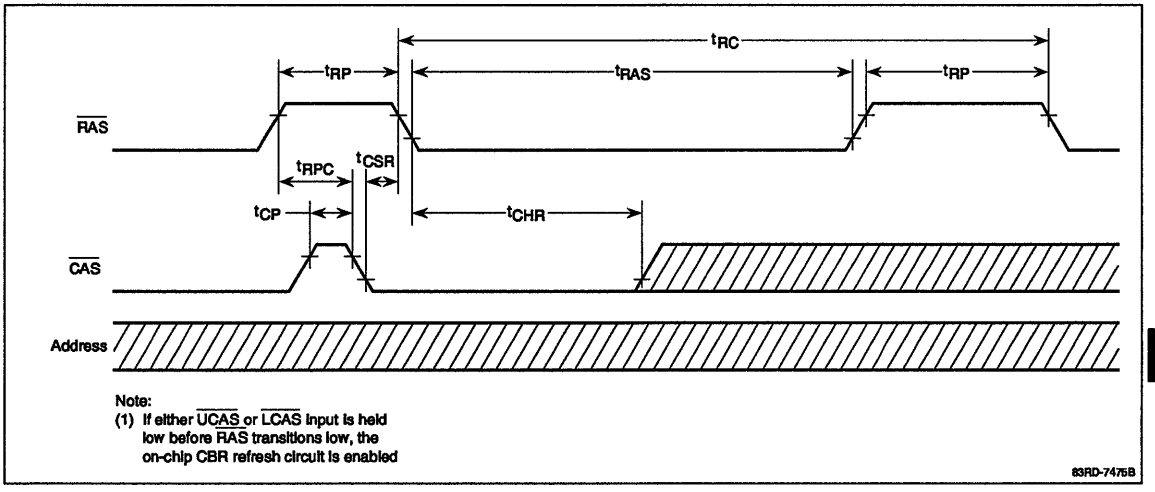


Timing Waveforms (cont)

$\overline{\text{RAS}}$-Only Refresh Cycle



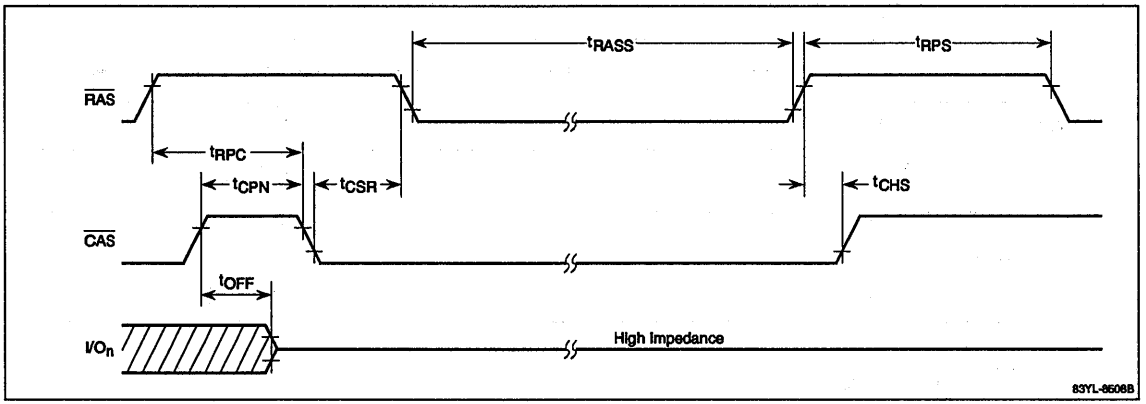
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



7e

Timing Waveforms (cont)

CBR Self-Refresh Cycle



NEC

Section 8. 16M DRAMs

μPD	Org.	Features	
4216100	16M x 1	FP; 4K refresh	8a
4217100	16M x 1	FP; 2K refresh	
4216101	16M x 1	Nibble; 4K refresh	8b
4217101	16M x 1	Nibble; 2K refresh	
4216102	16M x 1	Static-column; 4K refresh	8c
4217102	16M x 1	Static-column; 2K refresh	
4216400	4M x 4	FP; 4K refresh	8d
4217400	4M x 4	FP; 2K refresh	
4216402	4M x 4	Static-column; 4K refresh	8e
4217402	4M x 4	Static-column; 2K refresh	
4216410	4M x 4	FP; 4K refresh; write-per-bit	8f
4217410	4M x 4	FP; 2K refresh; write-per-bit	
4216412	4M x 4	Static-column; 4K refresh; write-per-bit	8g
4217412	4M x 4	Static-column; 2K refresh; write-per-bit	
4216800	2M x 8	FP; 4K refresh	8h
4216800L	2M x 8	FP; 4K refresh; 3.3-V	
42S16800	2M x 8	FP; 4K refresh; SR	
42S16800L	2M x 8	FP; 4K refresh; SR; 3.3-V	
4217800	2M x 8	FP; 2K refresh	
4217800L	2M x 8	FP; 2K refresh; 3.3-V	
42S17800	2M x 8	FP; 2K refresh; SR	
42S17800L	2M x 8	FP; 2K refresh; SR; 3.3-V	
4216802	2M x 8	Static-column	8i
4216900	2M x 9	FP; 4K refresh	8j
4216900L	2M x 9	FP; 4K refresh; 3.3-V	
42S16900	2M x 9	FP; 4K refresh; SR	
42S16900L	2M x 9	FP; 4K refresh; SR; 3.3-V	
4217900	2M x 9	FP; 2K refresh	
4217900L	2M x 9	FP; 2K refresh; 3.3-V	
42S17900	2M x 9	FP; 2K refresh; SR	
42S17900L	2M x 9	FP; 2K refresh; SR; 3.3-V	
4216902	2M x 9	Static-column	8k

μPD	Org.	Features	
4216160	1M x 16	FP; 4K refresh	8l
4216160L	1M x 16	FP; 4K refresh; 3.3-V	
42S16160	1M x 16	FP; 4K refresh; SR	
42S16160L	1M x 16	FP; 4K refresh; SR; 3.3-V	
4217160	1M x 16	FP; 2K refresh	
4217160L	1M x 16	FP; 2K refresh; 3.3-V	
42S17160	1M x 16	FP; 2K refresh; SR	
42S17160L	1M x 16	FP; 2K refresh; SR; 3.3-V	
4218160	1M x 16	FP; 1K refresh	
4218160L	1M x 16	FP; 1K refresh; 3.3-V	
42S18160	1M x 16	FP; 1K refresh; SR	
42S18160L	1M x 16	FP; 1K refresh; SR; 3.3-V	
4216180	1M x 18	FP; 4K refresh	8m
4216180L	1M x 18	FP; 4K refresh; 3.3-V	
42S16180	1M x 18	FP; 4K refresh; SR	
42S16180L	1M x 18	FP; 4K refresh; SR; 3.3-V	
4217180	1M x 18	FP; 2K refresh	
4217180L	1M x 18	FP; 2K refresh; 3.3-V	
42S17180	1M x 18	FP; 2K refresh; SR	
42S17180L	1M x 18	FP; 2K refresh; SR; 3.3-V	
4218180	1M x 18	FP; 1K refresh	
4218180L	1M x 18	FP; 1K refresh; 3.3-V	
42S18180	1M x 18	FP; 1K refresh; SR	
42S18180L	1M x 18	FP; 1K refresh; SR; 3.3-V	

FP = Fast-page
SR = Self-refresh

μPD4216100, 4217100
16,777,216 x 1-Bit
Dynamic CMOS RAM

Description

The μPD4216100 and the μPD4217100 are fast-page dynamic RAMs organized as 16,777,216 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles.

Two versions of the 16,777,216 x 1-bit DRAM are available. The μPD4216100 version uses 4096 address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period. The μPD4217100 version uses 2048 address combinations of A_0 - A_{10} to refresh the memory during a 32-ms period.

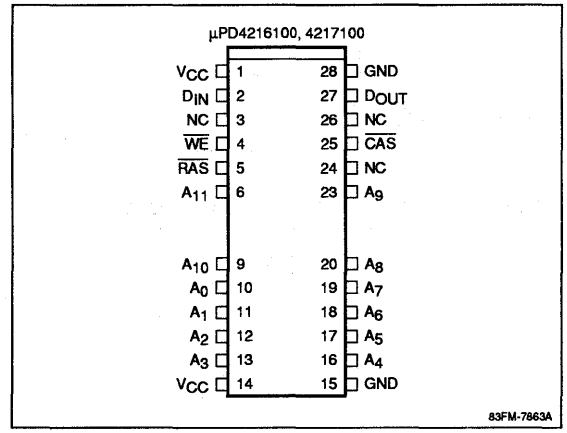
Both versions use row and column address combinations of A_0 - A_{11} for accessing the memory during read, write, and read-modify-write cycles.

Features

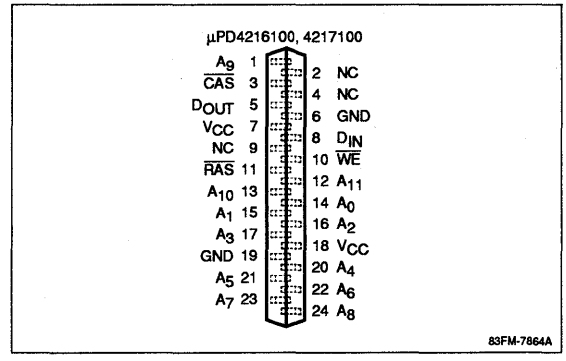
- 16,777,216 by 1-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 4K refresh cycles every 64 ms (4216100); 2K refresh cycles every 32 ms (4217100)
- 28/24-pin plastic SOJ (400 mil), 24-pin plastic ZIP (475 mil), and 28/24-pin plastic TSOP packaging

Pin Configurations

28/24-Pin Plastic SOJ



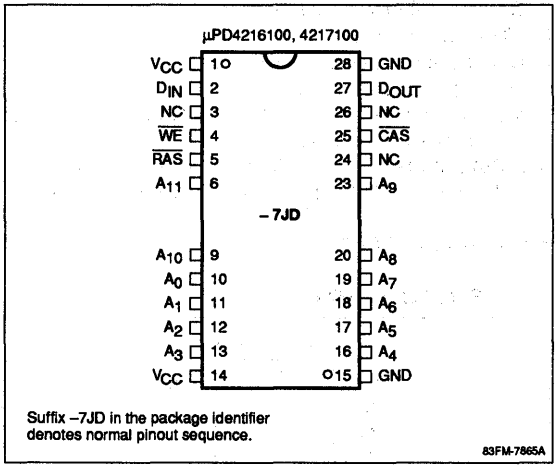
24-Pin Plastic ZIP



8a

Pin Configurations

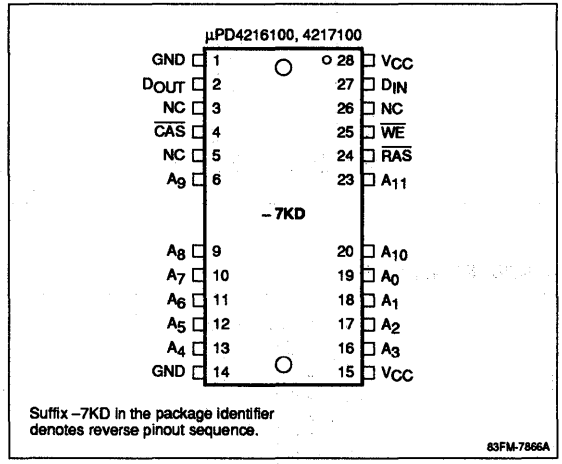
28/24-Pin Plastic TSOP (Normal Pinouts)



Suffix –7JD in the package identifier denotes normal pinout sequence.

83FM-7865A

28/24-Pin Plastic TSOP (Reverse Pinouts)



Suffix –7KD in the package identifier denotes reverse pinout sequence.

83FM-7866A

Pin Identification

Name	Function
A_0 - A_{11}	Address inputs
$\overline{CAS}$	Column address strobe
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	–1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	–55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	–1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Sym	*Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5 (7)	pF	Address, D_{IN}
	C_{I2}	7 (9)	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_O	7 (9)	pF	D_{OUT}

*Values in parentheses are for the ZIP package.

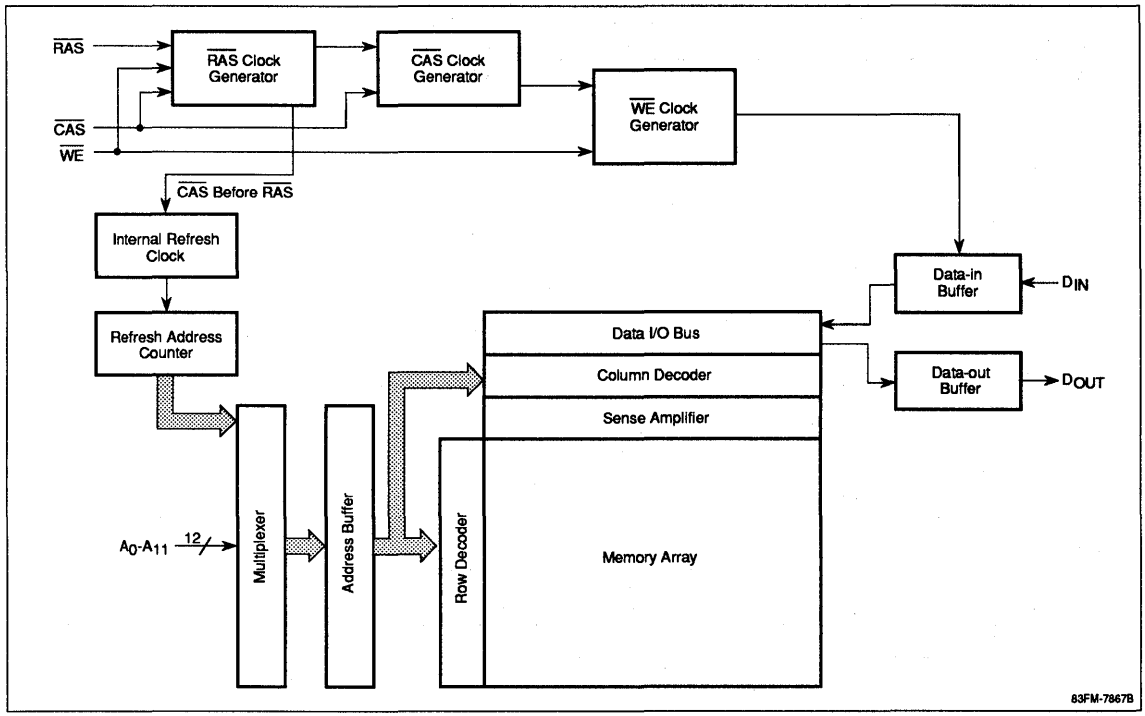
Ordering Information, μPD4216100 (4K Refresh Cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD4216100LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4216100V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4216100G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4216100G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	

Ordering Information, μPD4217100 (2K Refresh Cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD4217100LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4217100V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4217100G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4217100G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1} (4216100)		90		80		70		60	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; $t_{RC} \geq t_{RC}$ min; I_O = 0 mA (Note 5)
	I_{CC1} (4217100)		110		100		90		80	mA	
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (4216100)		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} \geq t_{RC}$ min; I_O = 0 mA (Note 5)
	I_{CC3} (4217100)		110		100		90		80	mA	
Operating current, fast-page cycle, average	I_{CC4} (4216100)		70		60		50		40	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} \geq t_{RC}$ min; I_O = 0 mA (Note 5)
	I_{CC4} (4217100)		70		60		50		40	mA	
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (4216100)		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; $t_{RC} \geq t_{RC}$ min; I_O = 0 mA (Note 5)
	I_{CC5} (4217100)		110		100		90		80	mA	
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		40		50		ns	(Note 16)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		15		18		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	18	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	10		10		10		10		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		0		ns	(Note 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		5		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	15		18		20		25		ns	(Note 16)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	10		15		15		20		ns	(Note 15)

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AC Characteristics (cont)

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	60		65		75		85		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	110		130		150		180		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 10)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		64		64		64		64	ms	(Note 18)
	t_{REF}		32		32		32		32	ms	(Note 19)
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		55		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5		5		5		5		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	15		18		20		25		ns	
Read-write cycle time	t_{RWC}	135		155		175		210		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	10		10		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		20		ns	
Write command pulse width	t_{WP}	10		10		15		20		ns	(Note 14)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

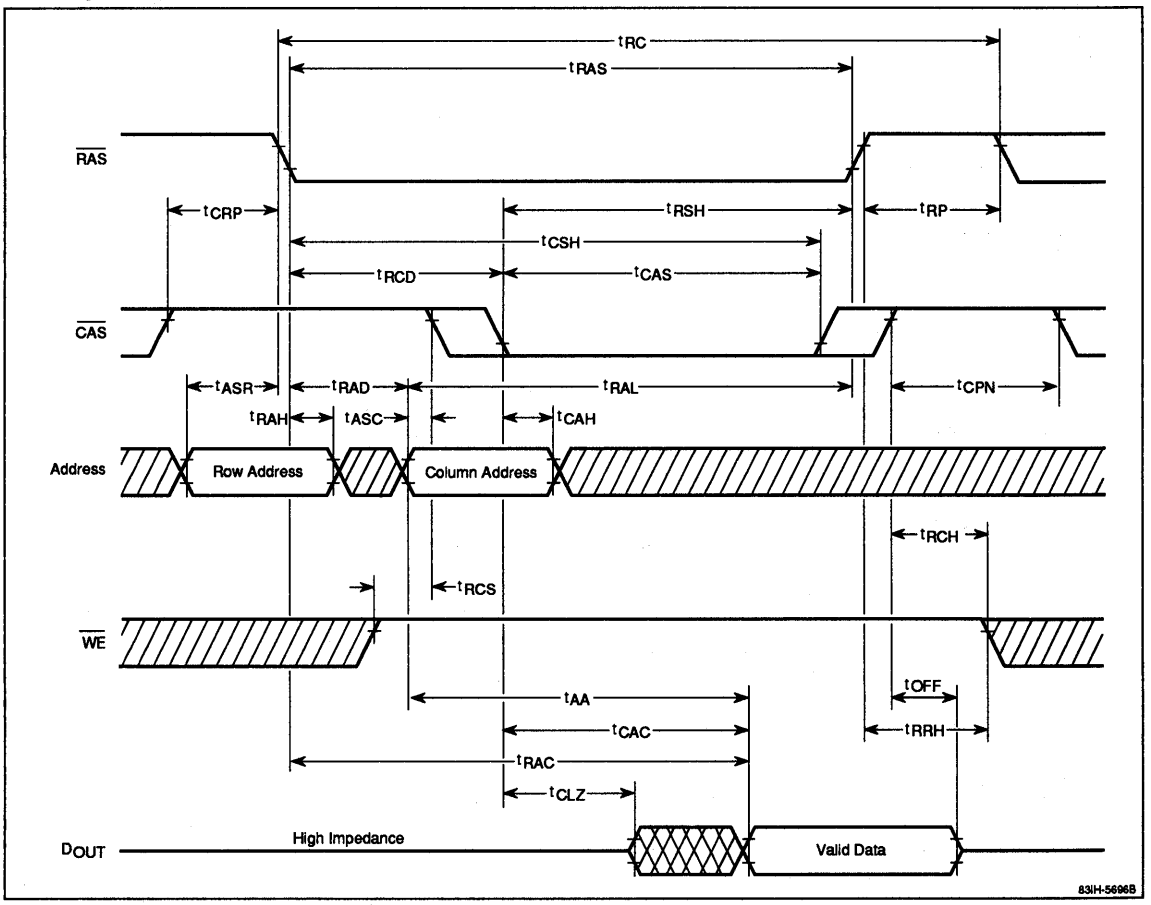
(17) Assumes that the test mode has been set. A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may be inadvertently initiated during power up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power up sequence to ensure normal device operation. Contact your NEC Electronics sales representative for more details.

(18) The μPD4216100 RAS-only refresh (ROR) cycle uses 4096 external row address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period (t_{REF}). Row and column address combinations of A_0 - A_{11} are used to access the memory during read, write, and read-modify-write cycles. CBR ($\overline{CAS}$ before $\overline{RAS}$) and hidden CBR refresh cycles use 4096 internal row address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period (t_{REF}).

(19) The μPD4217100 RAS-only refresh (ROR) cycle uses 2048 external row address combinations of A_0 - A_{10} to refresh the memory during a 32-ms refresh period (t_{REF}). Row and column address combinations of A_0 - A_{10} are used to access the memory during read, write, and read-modify-write cycles. CBR ($\overline{CAS}$ before $\overline{RAS}$) and hidden CBR refresh cycles use 2048 internal row address combinations of A_0 - A_{10} to refresh the memory during a 32-ms refresh period (t_{REF}).

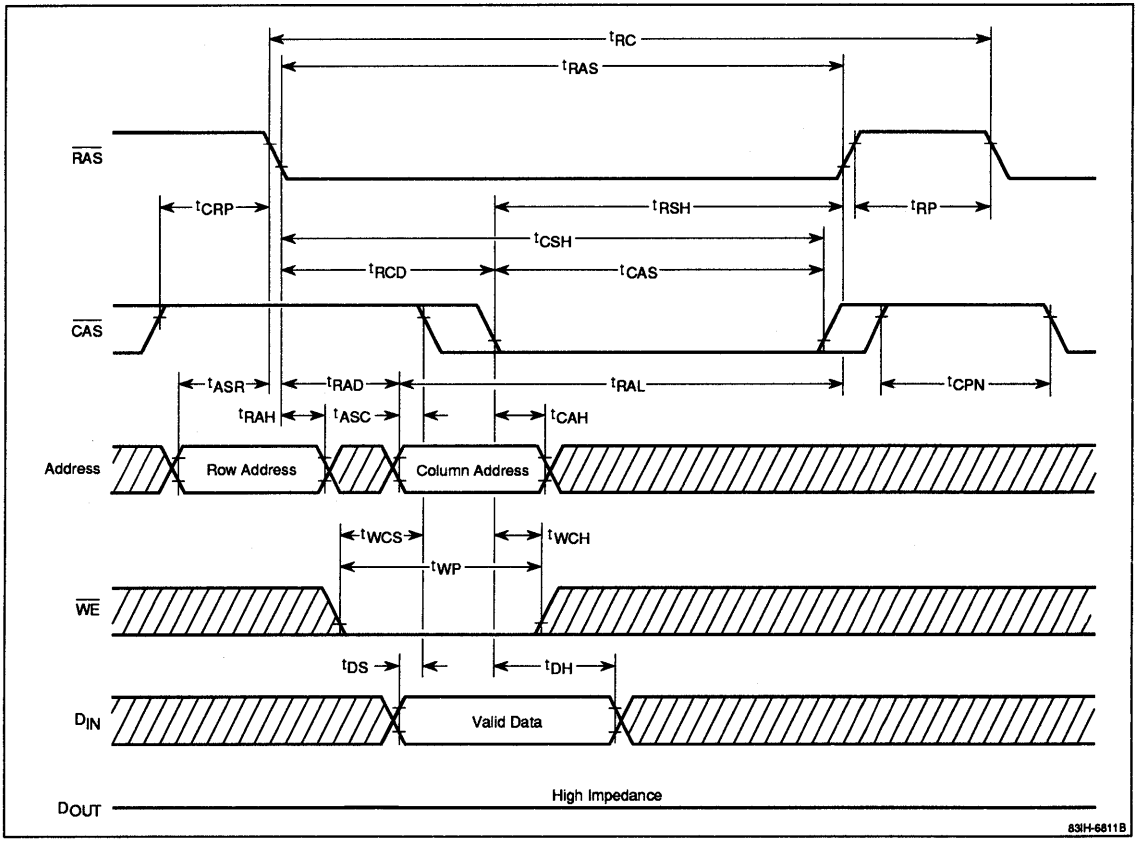
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



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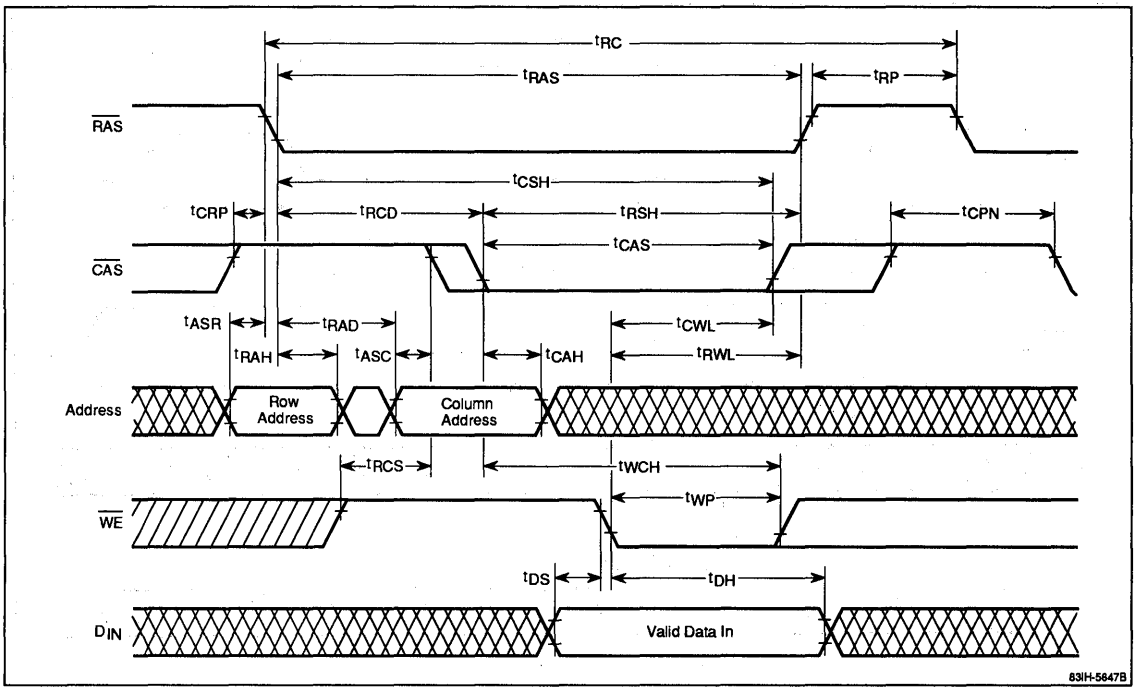
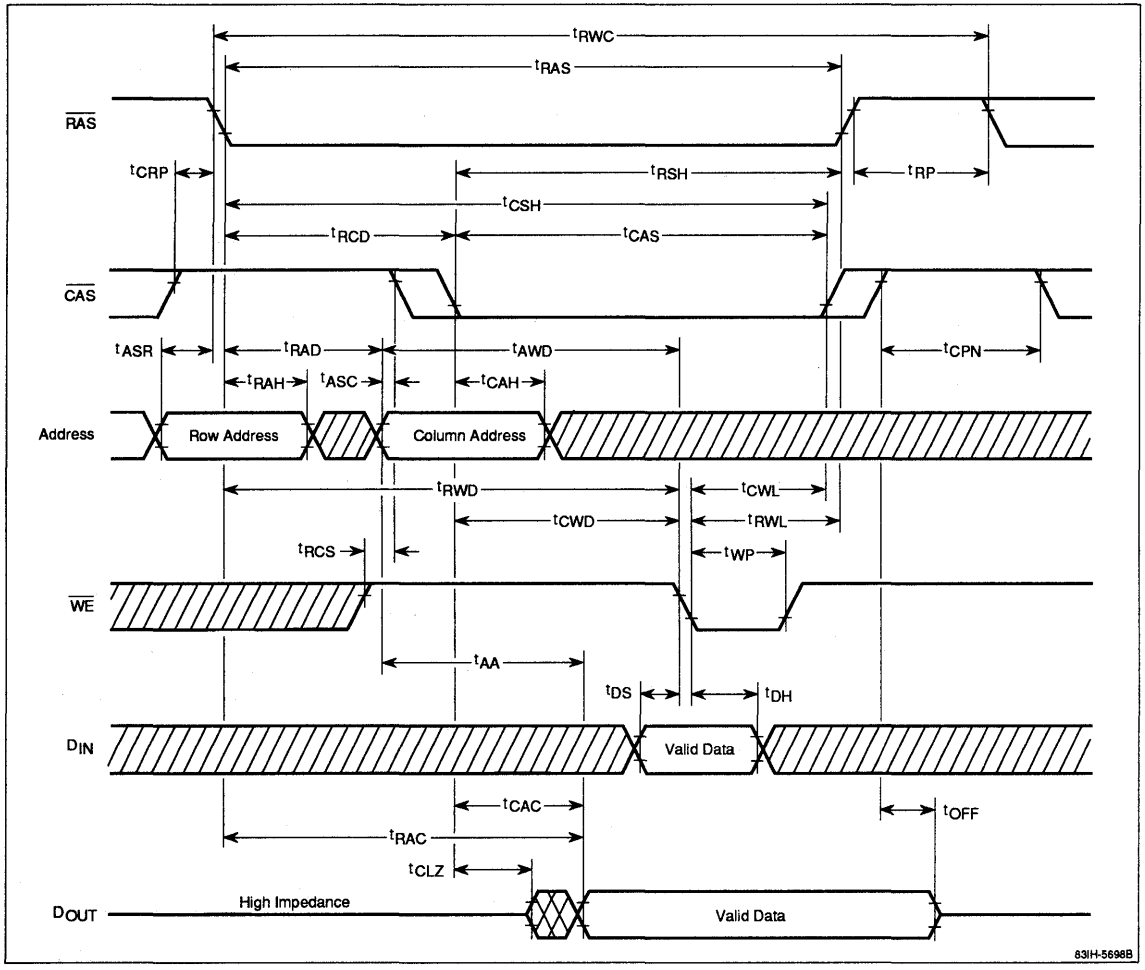
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

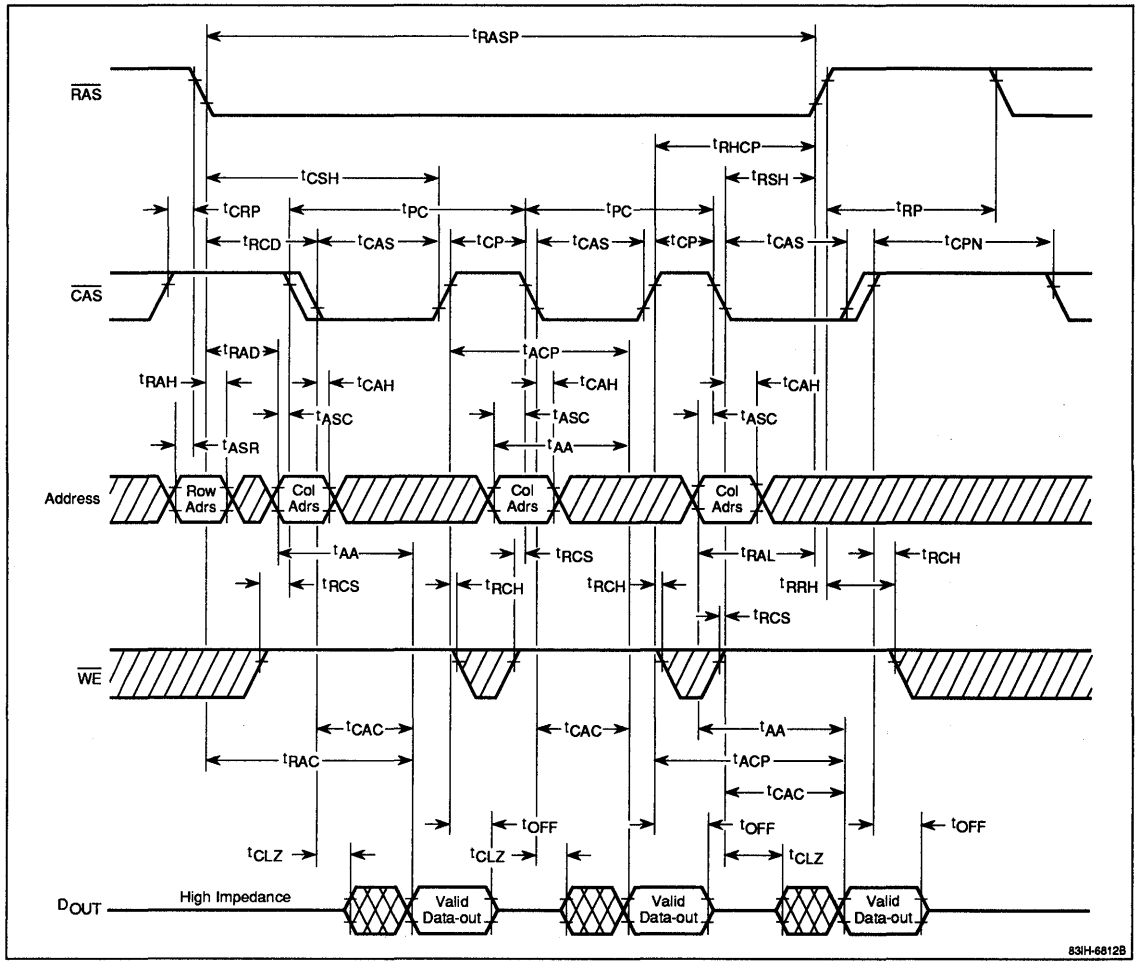
Read-Write/Read-Modify-Write Cycle



8a

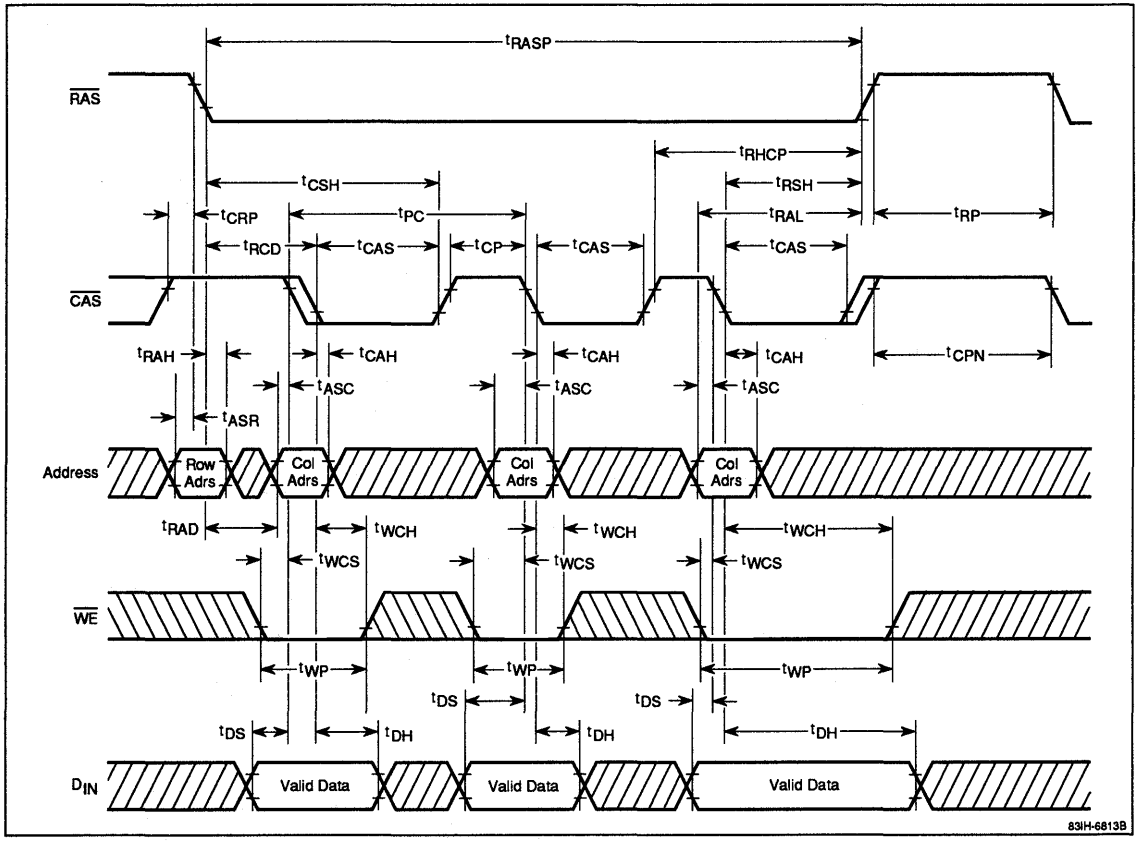
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

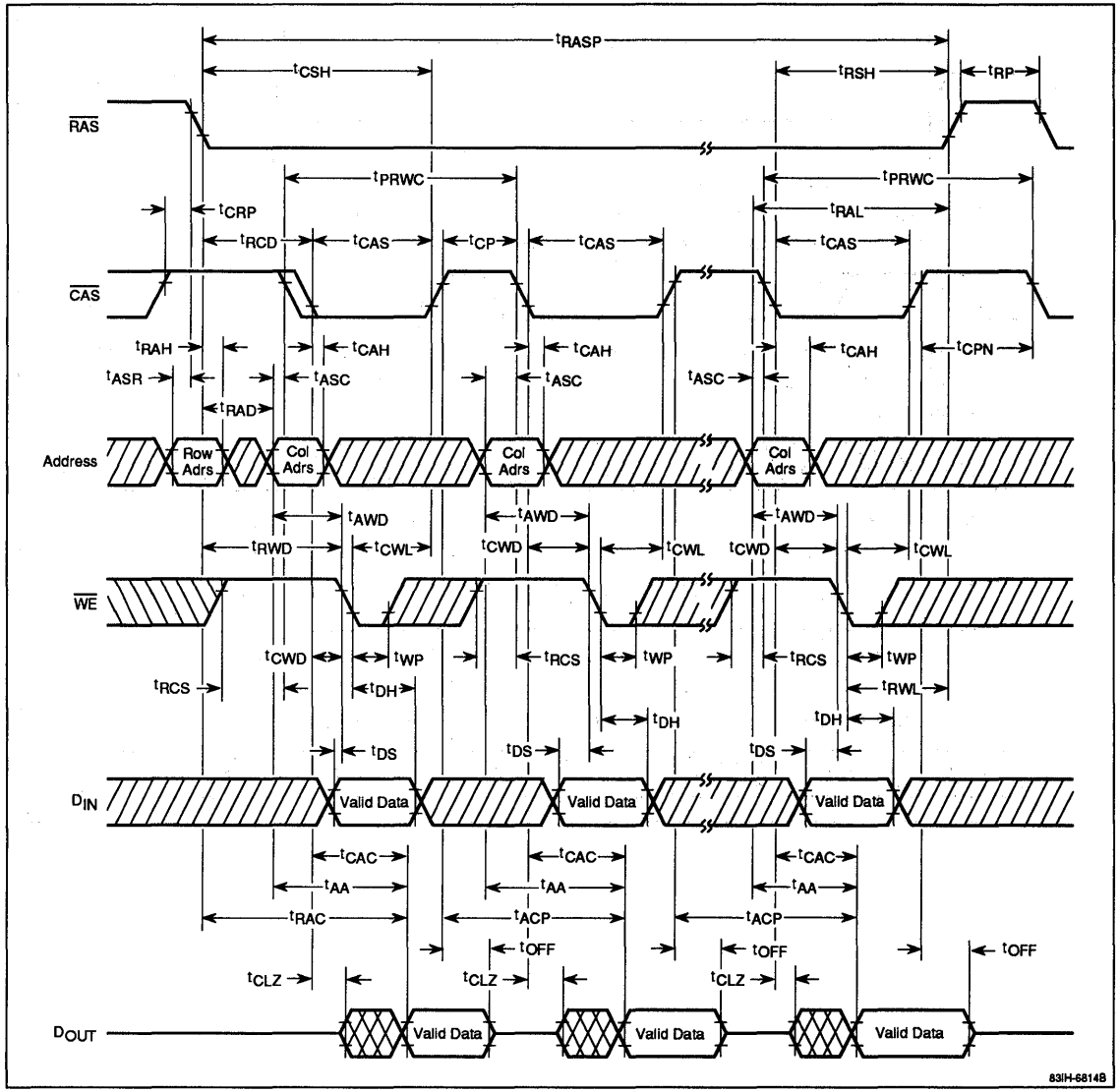
Fast-Page Early Write Cycle



8a

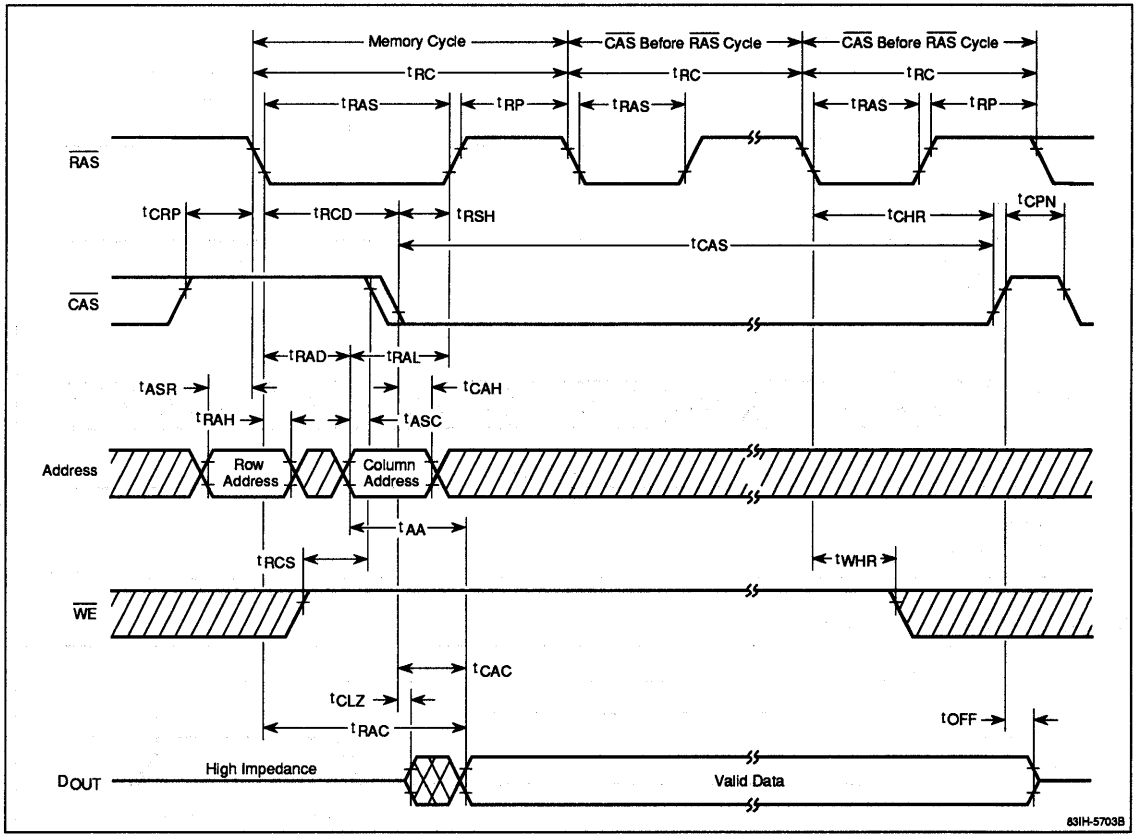
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



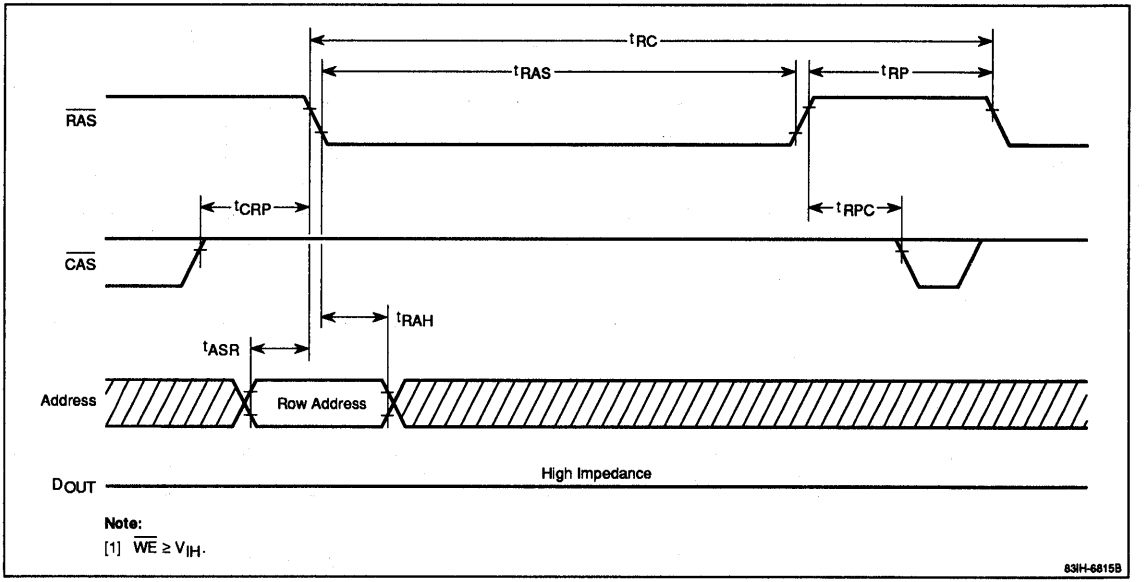
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

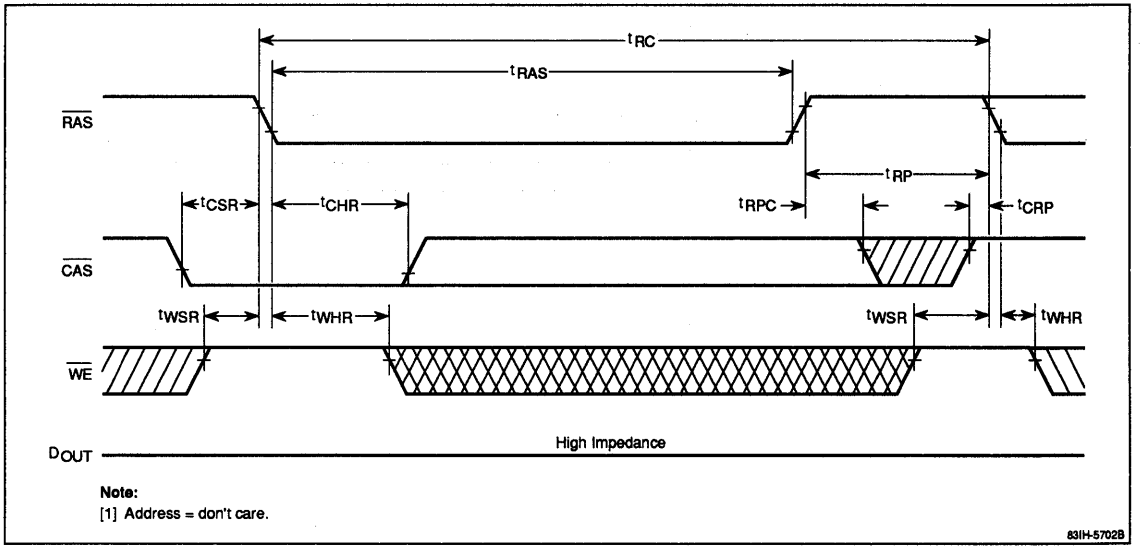
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

83IH-5702B

μPD4216101, 4217101
16,777,216 x 1-Bit
Dynamic CMOS RAM

Advance Information

Description

The μPD4216101 and the μPD4217101 are nibble-mode dynamic RAMs organized as 16,777,216 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. Nibble-mode read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by $\overline{RAS}$-only refresh cycles or by normal read or write cycles.

Two versions of the 16,777,216 by 1-bit nibble-mode dynamic RAM are available. The μPD4216101 version uses 4096 address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period. The μPD4217101 version uses 2048 address combinations of A_0 - A_{10} to refresh the memory during a 32-ms refresh period.

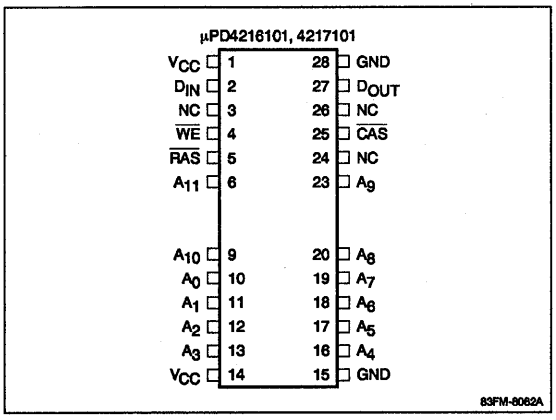
Both versions use row and column address combinations of A_0 - A_{11} for accessing the memory during read, write, and read-modify-write cycles.

Features

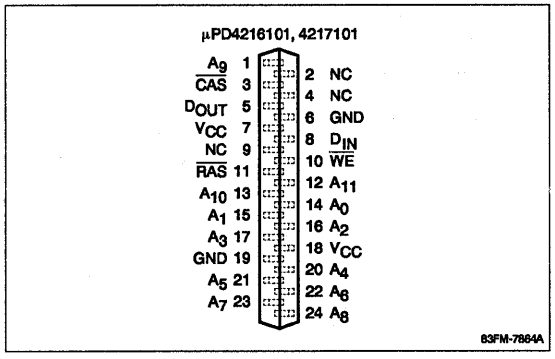
- 16,777,216 by 1-bit organization
- Single +5-volt power supply
- Nibble-mode option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 4K refresh cycles every 64 ms (4216101); 2K refresh cycles every 32 ms (4217101)
- 28/24-pin SOJ (400 mil), 24-pin ZIP (475 mil), and 28/24-pin TSOP plastic packaging

Pin Configurations

28/24-Pin Plastic SOJ



24-Pin Plastic ZIP



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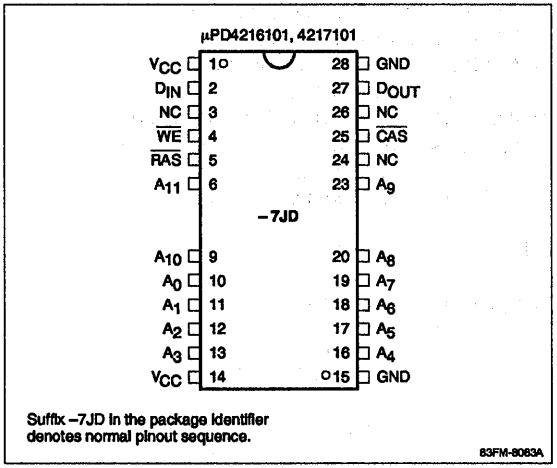
Contact your NEC sales representative for complete data sheet and product availability.

Pin Configurations (cont)

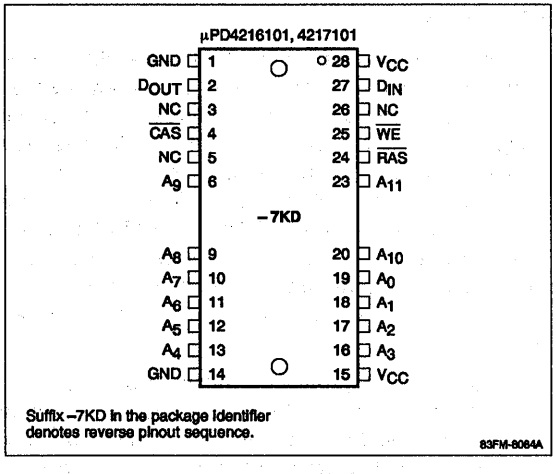
28/24-Pin Plastic TSOP (Normal Pinouts)



Suffix –7JD in the package identifier denotes normal pinout sequence.

83FM-8083A

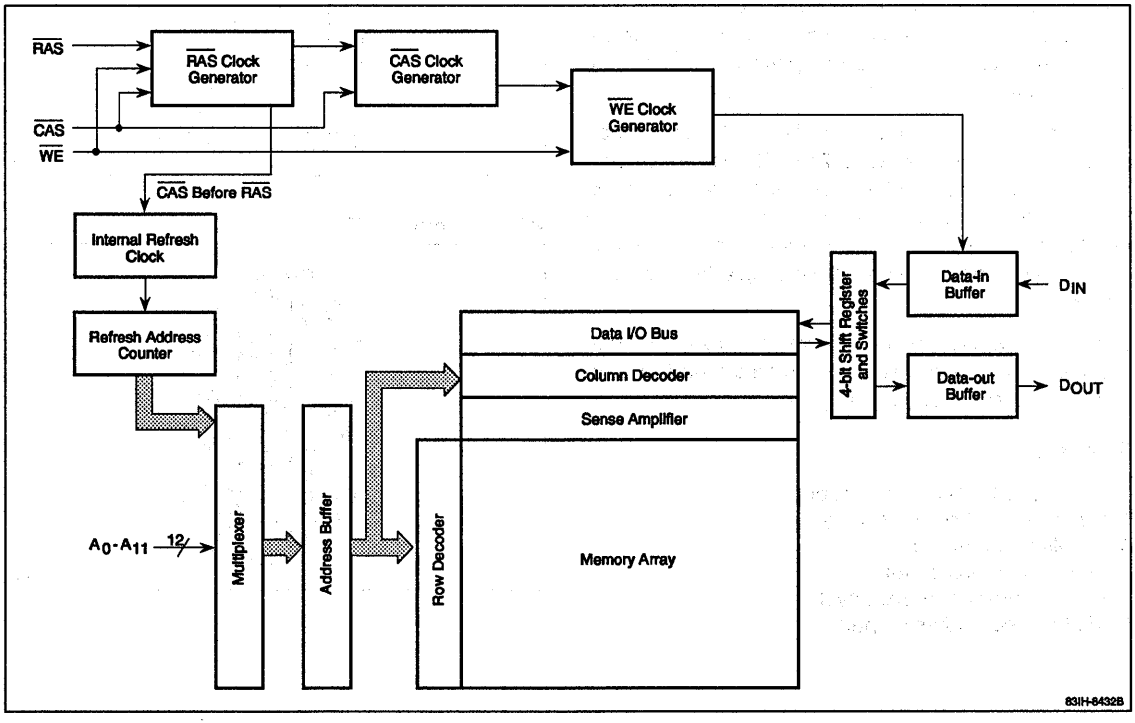
28/24-Pin Plastic TSOP (Reverse Pinouts)



Suffix –7KD in the package identifier denotes reverse pinout sequence.

83FM-8084A

Block Diagram



83IH-8432B

Ordering Information, μPD4216101 (4K refresh cycles)

Part Number		$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Nibble-Mode Cycle (max)	Package
μPD4216101	LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
	LE-70	70 ns	130 ns	40 ns	
	LE-80	80 ns	150 ns	40 ns	
	LE-10	100 ns	180 ns	45 ns	
μPD4216101	V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
	V-70	70 ns	130 ns	40 ns	
	V-80	80 ns	150 ns	40 ns	
	V-10	100 ns	180 ns	45 ns	
μPD4216101	G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
	G5-70	70 ns	130 ns	40 ns	
	G5-80	80 ns	150 ns	40 ns	
	G5-10	100 ns	180 ns	45 ns	
μPD4216101	G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
	G5M-70	70 ns	130 ns	40 ns	
	G5M-80	80 ns	150 ns	40 ns	
	G5M-10	100 ns	180 ns	45 ns	

Ordering Information, μPD4217101 (2K refresh cycles)

Part Number		$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Nibble-Mode Cycle (max)	Package
μPD4217101	LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
	LE-70	70 ns	130 ns	40 ns	
	LE-80	80 ns	150 ns	40 ns	
	LE-10	100 ns	180 ns	45 ns	
μPD4217101	V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
	V-70	70 ns	130 ns	40 ns	
	V-80	80 ns	150 ns	40 ns	
	V-10	100 ns	180 ns	45 ns	
μPD4217101	G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
	G5-70	70 ns	130 ns	40 ns	
	G5-80	80 ns	150 ns	40 ns	
	G5-10	100 ns	180 ns	45 ns	
μPD4217101	G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
	G5M-70	70 ns	130 ns	40 ns	
	G5M-80	80 ns	150 ns	40 ns	
	G5M-10	100 ns	180 ns	45 ns	

NEC Electronics Inc.

μPD4216102, 4217102
16,777,216 x 1-Bit
Dynamic CMOS RAM

Advance Information

Description

The μPD4216102 and the μPD4217102 are static-column dynamic RAMs organized as 16,777,216 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CS}$ low. The data output is returned to high impedance by returning $\overline{CS}$ high. Static-column read and write cycles can be executed by cycling $\overline{CS}$.

Refreshing may be accomplished by a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by $\overline{RAS}$-only refresh cycles or by normal read or write cycles.

Two versions of the 16,777,216 by 1-bit static-column dynamic RAM are available. The μPD4216102 version uses 4096 address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period. The μPD4217102 version uses 2048 address combinations of A_0 - A_{10} to refresh the memory during a 32-ms refresh period.

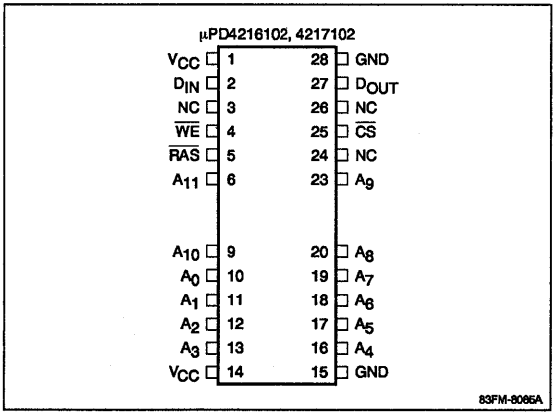
Both versions use row and column address combinations of A_0 - A_{11} to access the memory during read, write, and read-modify-write cycles.

Features

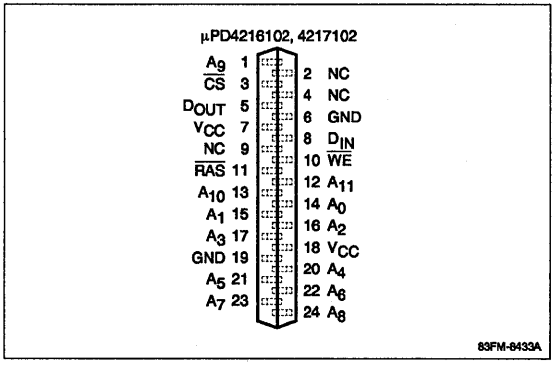
- 16,777,216 by 1-bit organization
- Single +5-volt power supply
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 4K refresh cycles every 64 ms (4216102); 2K refresh cycles every 32 ms (4217102)
- 28/24-pin plastic SOJ (400-mil), 24-pin plastic ZIP (475 mil), and 28/24-pin plastic TSOP packaging

Pin Configurations

28/24-Pin Plastic SOJ



24-Pin Plastic ZIP

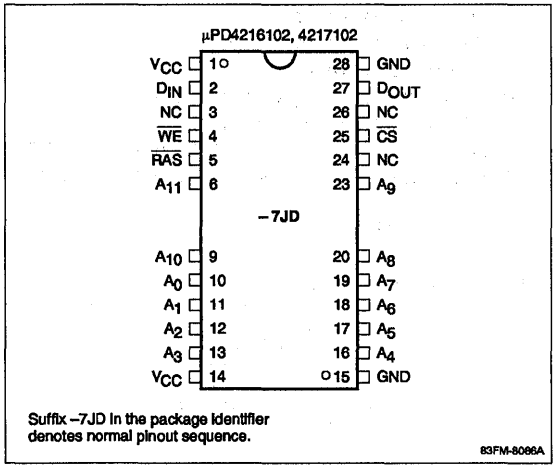


8c

Contact your NEC sales representative for a complete data sheet and product availability.

Pin Configurations (cont)

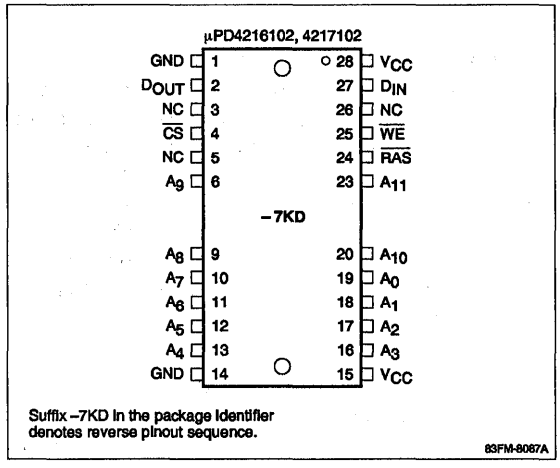
28/24-Pin Plastic TSOP (Normal Pinouts)



Suffix –7JD in the package identifier denotes normal pinout sequence.

83FM-8066A

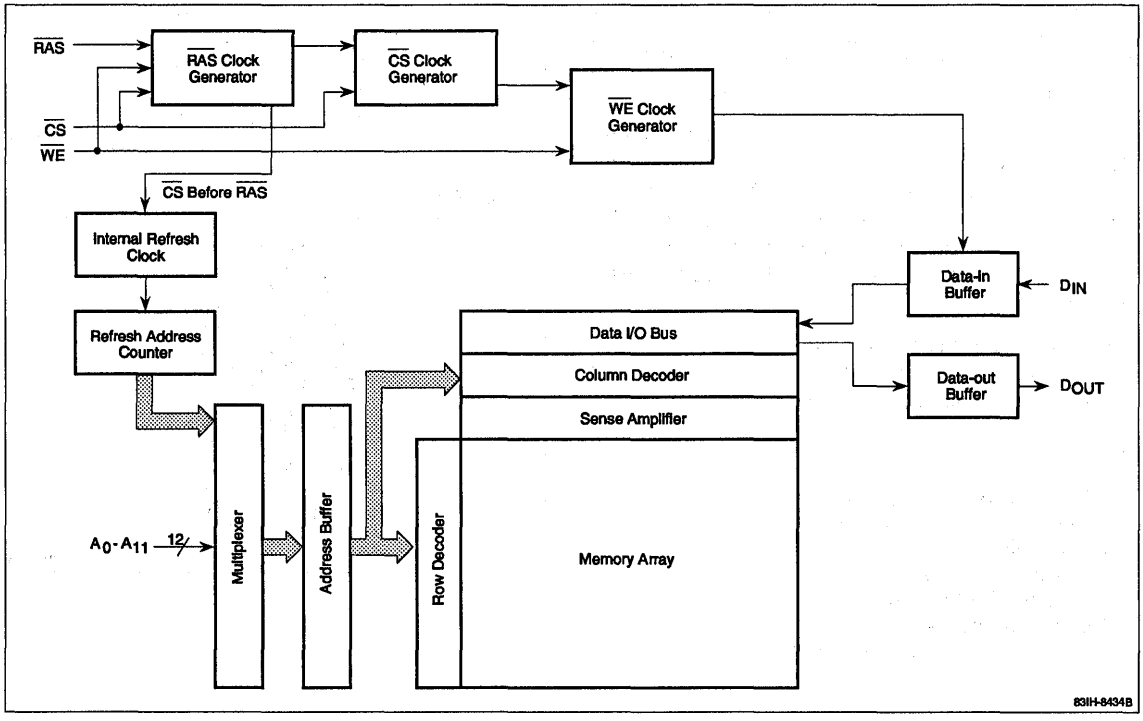
28/24-Pin Plastic TSOP (Reverse Pinouts)



Suffix –7KD in the package identifier denotes reverse pinout sequence.

83FM-8067A

Block Diagram



83IH-8434B

Ordering Information, μPD4216102 (4K refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Static-Column Cycle (max)	Package
μPD4216102LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	40 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4216102V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	40 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4216102G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	40 ns	
G5-80	80 ns	150 ns	50 ns	
G5-10	100 ns	180 ns	60 ns	
μPD4216102G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	40 ns	
G5M-80	80 ns	150 ns	50 ns	
G5M-10	100 ns	180 ns	60 ns	

Ordering Information, μPD4217102 (2K refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Static-Column Cycle (max)	Package
μPD4217102LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	40 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4217102V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	40 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4217102G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	40 ns	
G5-80	80 ns	150 ns	50 ns	
G5-10	100 ns	180 ns	60 ns	
μPD4217102G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	40 ns	
G5M-80	80 ns	150 ns	50 ns	
G5M-10	100 ns	180 ns	60 ns	

μPD4216400, 4217400
4,194,304 x 4-Bit
Dynamic CMOS RAM

Description

The μPD4216400 and the μPD4217400 are fast-page dynamic RAMs organized as 4,194,304 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles.

Two versions of the 4,194,304 x 4-bit DRAM are available. The μPD4216400 version uses 4096 address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period. Row address combinations A_0 - A_{11} and column address combinations A_0 - A_9 are used for accessing the memory during read, write, and read-modify-write cycles.

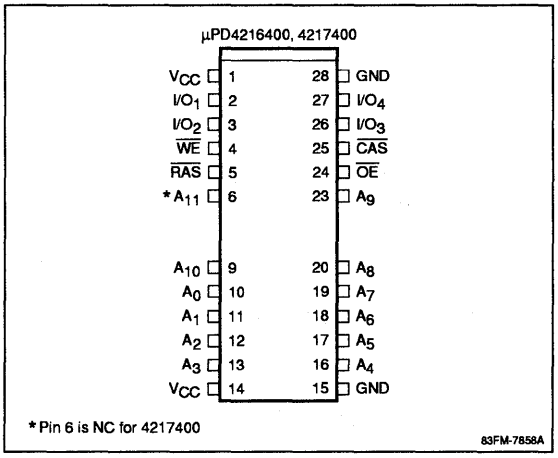
The μPD4217400 version uses 2048 address combinations of A_0 - A_{10} to refresh the memory during a 32-ms period. Row and column address combinations A_0 - A_{10} are used for accessing the memory during read, write, and read-modify-write cycles.

Features

- 4,194,304 by 4-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 4K refresh cycles every 64 ms (4216400); 2K refresh cycles every 32 ms (4217400)
- 28/24-pin plastic SOJ (400 mil), 24-pin plastic ZIP, and 28/24-pin plastic TSOP packaging

Pin Configurations

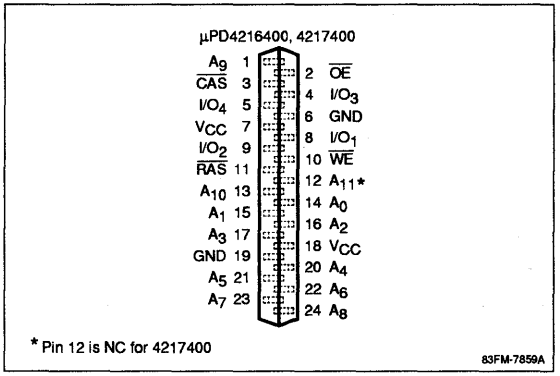
28/24-Pin Plastic SOJ



*Pin 6 is NC for 4217400

83FM-7858A

24-Pin Plastic ZIP



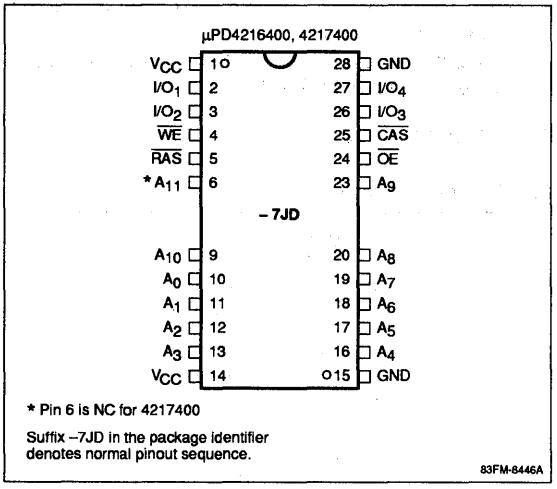
*Pin 12 is NC for 4217400

83FM-7859A

8d

Pin Configurations

28/24-Pin Plastic TSOP (Normal Pinouts)

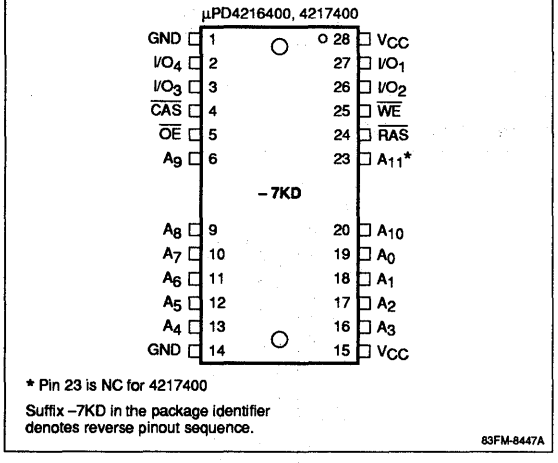


* Pin 6 is NC for 4217400

Suffix –7JD in the package identifier denotes normal pinout sequence.

83FM-8446A

28/24-Pin Plastic TSOP (Reverse Pinouts)



* Pin 23 is NC for 4217400

Suffix –7KD in the package identifier denotes reverse pinout sequence.

83FM-8447A

Pin Identification

Name	Function
A_0 - A_{11}	Address inputs (μPD4216400)
A_0 - A_{10}	Address inputs (μPD4217400)
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Absolute Maximum Ratings

Voltage on any pin relative to GND	–1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	–55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	–1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Sym	*Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5 (7)	pF	Addresses
	C_{I2}	7 (9)	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7 (9)	pF	I/O_1 - I/O_4

* Values in parentheses are for the ZIP package.

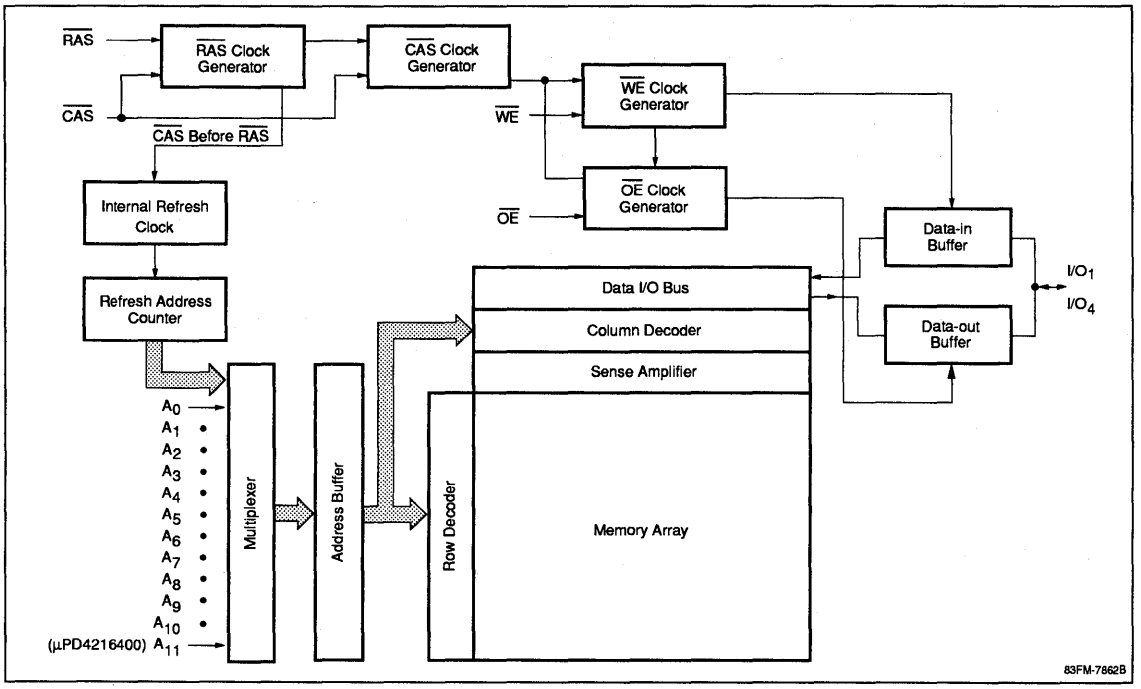
Ordering Information, μPD4216400 (4K Refresh Cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD4216400LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4216400V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4216400G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4216400G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	180 ns	50 ns	

Ordering Information, μPD4217400 (2K Refresh Cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD4217400LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4217400V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4217400G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4217400G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1} (4216400)		90		80		70		60	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; $t_{RC} \geq t_{RC}$ min; I_O = 0 mA (Note 5)
	I_{CC1} (4217400)		110		100		90		80	mA	
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (4216400)		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} \geq t_{RC}$ min; I_O = 0 mA (Note 5)
	I_{CC3} (4217400)		110		100		90		80	mA	
Operating current, fast-page cycle, average	I_{CC4} (4216400)		70		60		50		40	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} \geq t_{RC}$ min; I_O = 0 mA (Note 5)
	I_{CC4} (4217400)		70		60		50		40	mA	
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (4216400)		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; $t_{RC} \geq t_{RC}$ min; I_O = 0 mA (Note 5)
	I_{CC5} (4217400)		110		100		90		80	mA	
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	55		60		70		85		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		15		18		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	18	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	10		10		10		10		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		0		ns	(Notes 4, 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		5		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		43		50		60		ns	(Note 14)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	

AC Characteristics (cont)

		-60		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Data-in hold time	t_{DH}	10		15		15		20		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		15		18		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ delay data time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 9)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		0		ns	(Notes 4, 6, 7)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	85		90		105		120		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	110		130		150		180		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		64		64		64		64	ms	(Note 16)
	t_{REF}		32		32		32		32	ms	(Note 17)
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		55		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5		5		5		5		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	15		18		20		25		ns	
Read-write cycle time	t_{RWC}	160		180		205		245		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	85		95		110		135		ns	(Note 14)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	10		10		15		20		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 14)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		20		ns	
Write command pulse width	t_{WP}	10		10		15		20		ns	(Note 12)
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) If $t_{RCD} \leq t_{RCS}$ (max) and $t_{RAD} \leq t_{RAD}$ (max) access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max) access time is defined by t_{CAC} (max) and if $t_{RAD} \geq t_{RAD}$ (max) access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

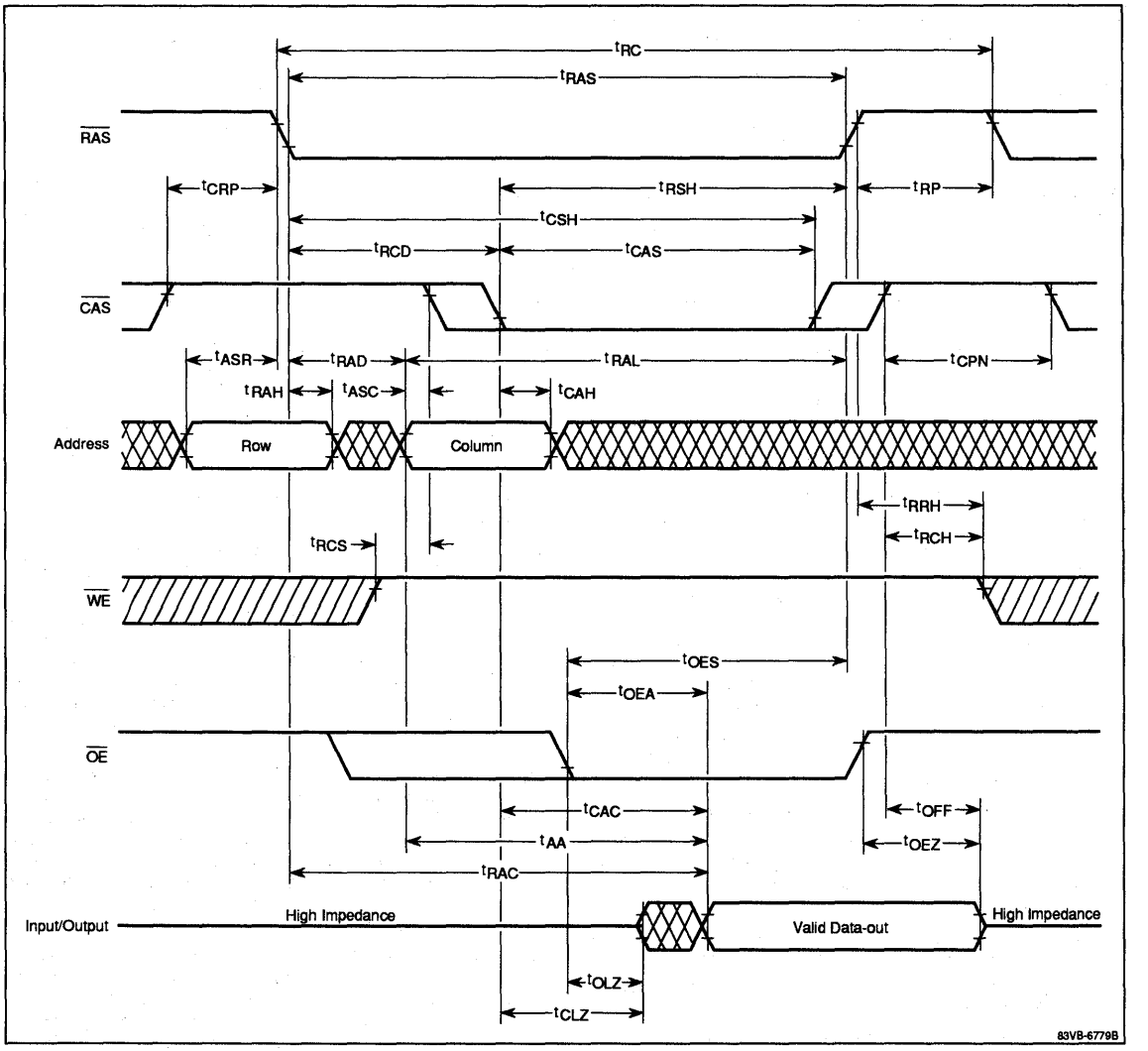
(15) Assumes that the test mode has been set. A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may be inadvertently initiated during power up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power up sequence to ensure normal device operation. Contact your NEC Electronics sales representative for more details.

(16) The μPD4216400 RAS-only refresh (ROR) cycle uses 4096 external row address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period (t_{REF}). Row address combinations of A_0 - A_{11} and column address combinations of A_0 - A_9 are used to access the memory during read, write, and read-modify-write cycles. CBR ($\overline{CAS}$ before $\overline{RAS}$) and hidden CBR refresh cycles use 4096 internal row address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period (t_{REF}).

(17) The μPD4217400 RAS-only refresh (ROR) cycle uses 2048 external row address combinations of A_0 - A_{10} to refresh the memory during a 32-ms refresh period (t_{REF}). Row and column address combinations of A_0 - A_{10} are used to access the memory during read, write, and read-modify-write cycles. CBR ($\overline{CAS}$ before $\overline{RAS}$) and hidden CBR refresh cycles use 2048 internal row address combinations of A_0 - A_{10} to refresh the memory during a 32-ms refresh period (t_{REF}).

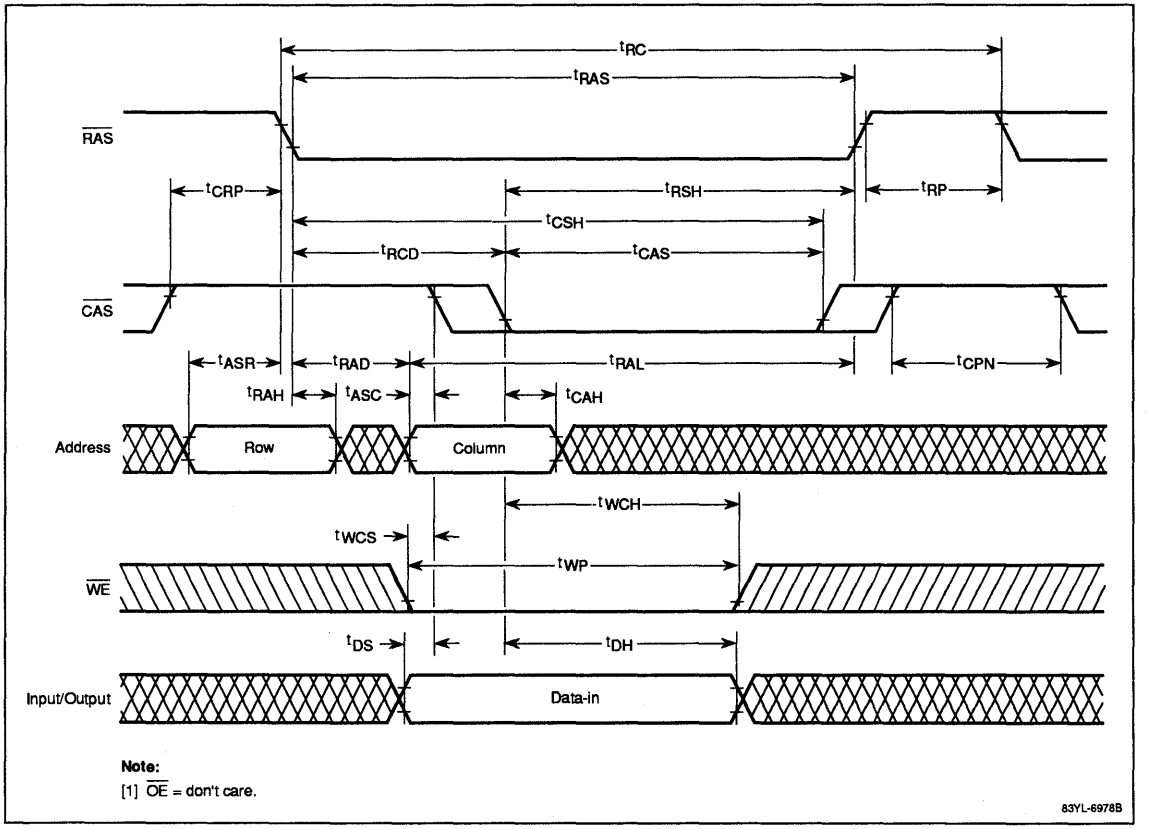
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle

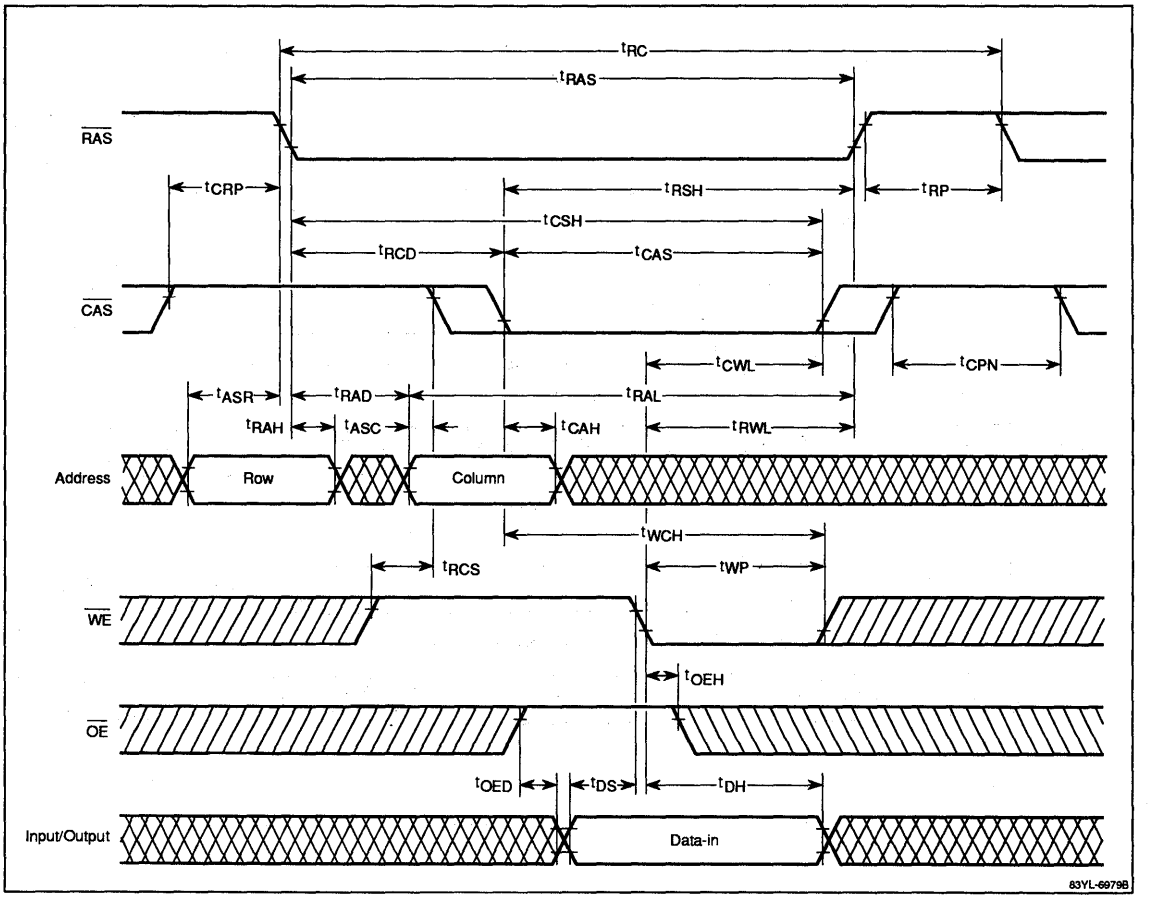


Note:
[1] $\overline{OE}$ = don't care.

83YL-6978B

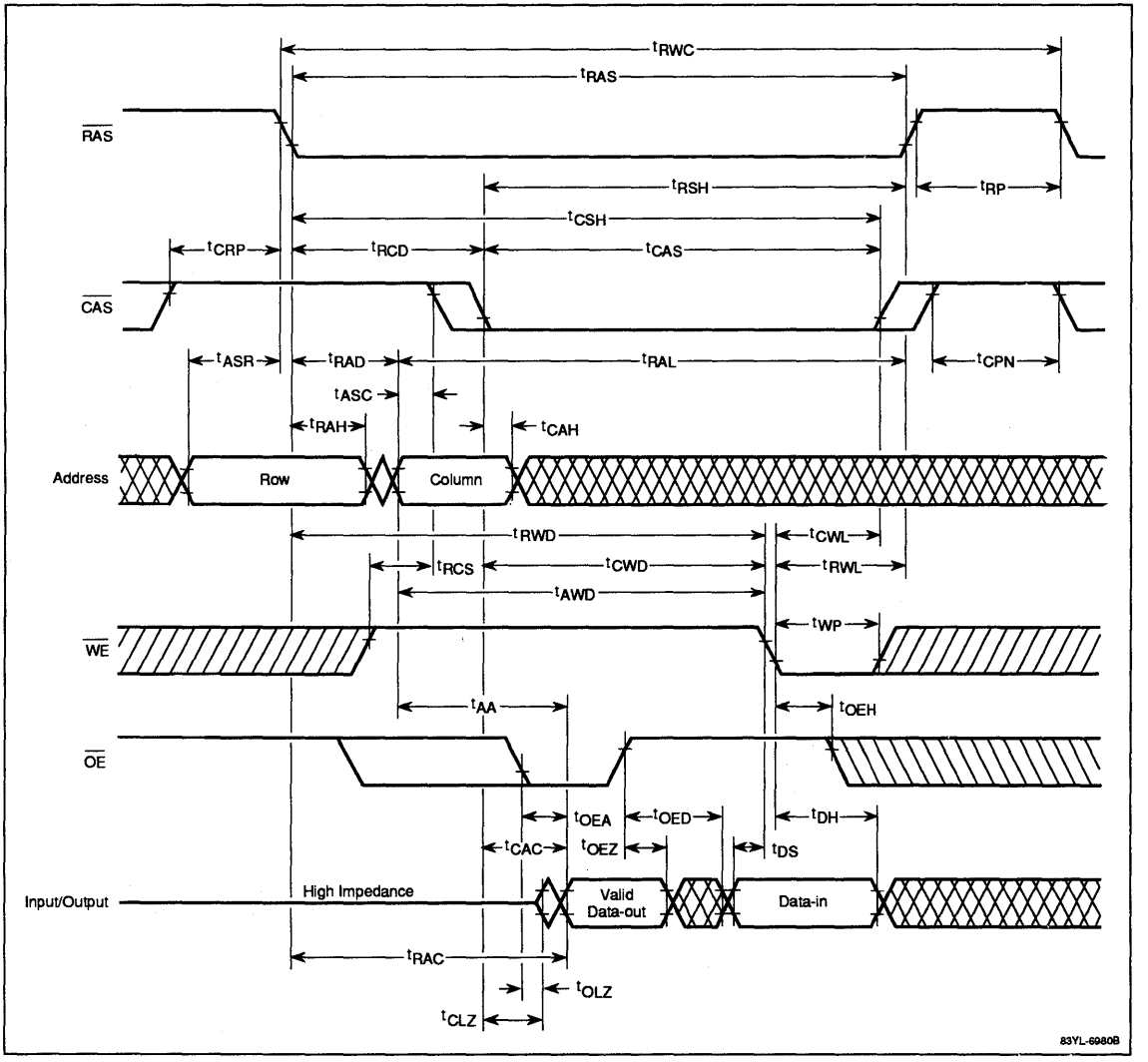
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

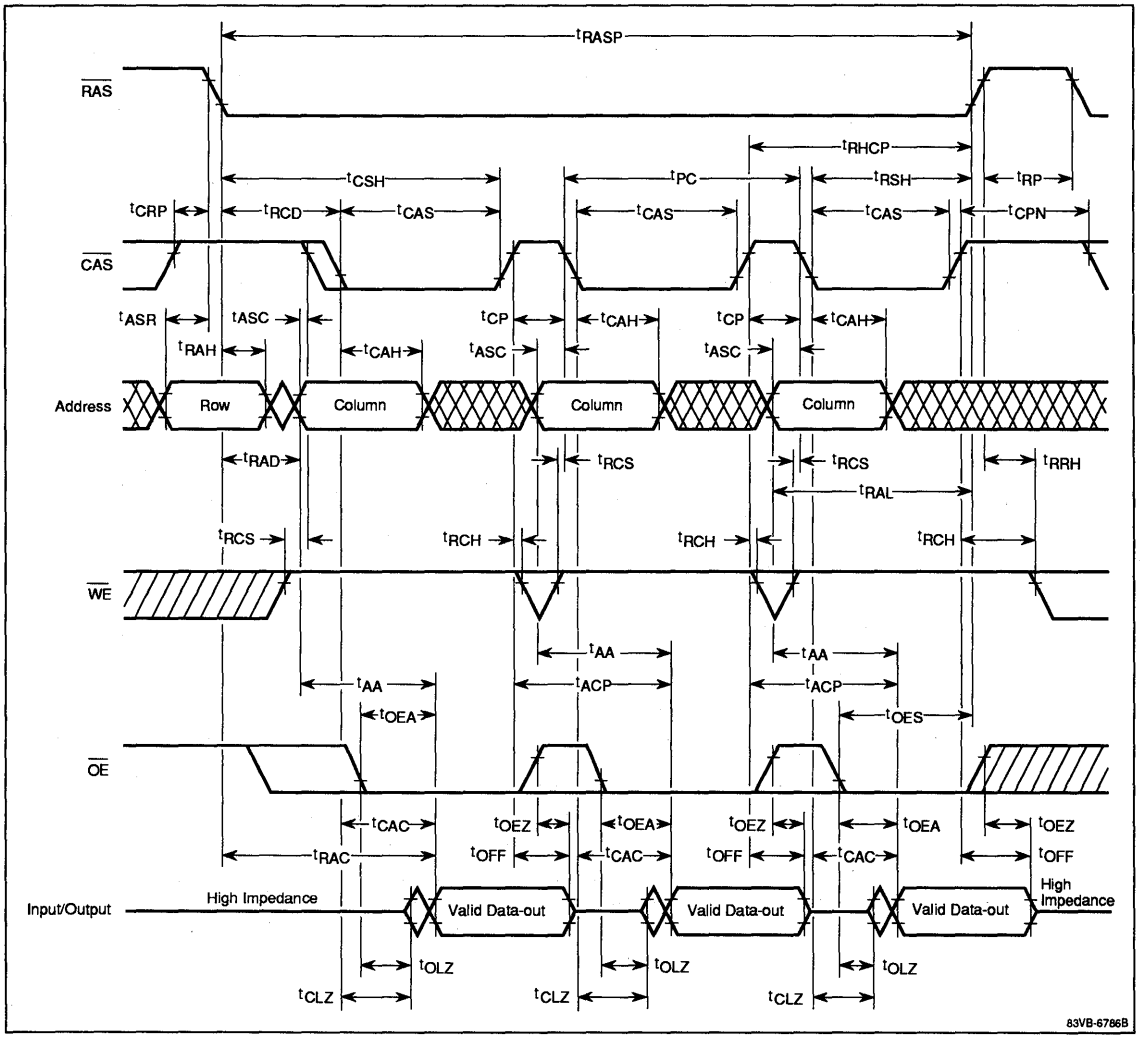
Read-Write/Read-Modify-Write Cycle



8d

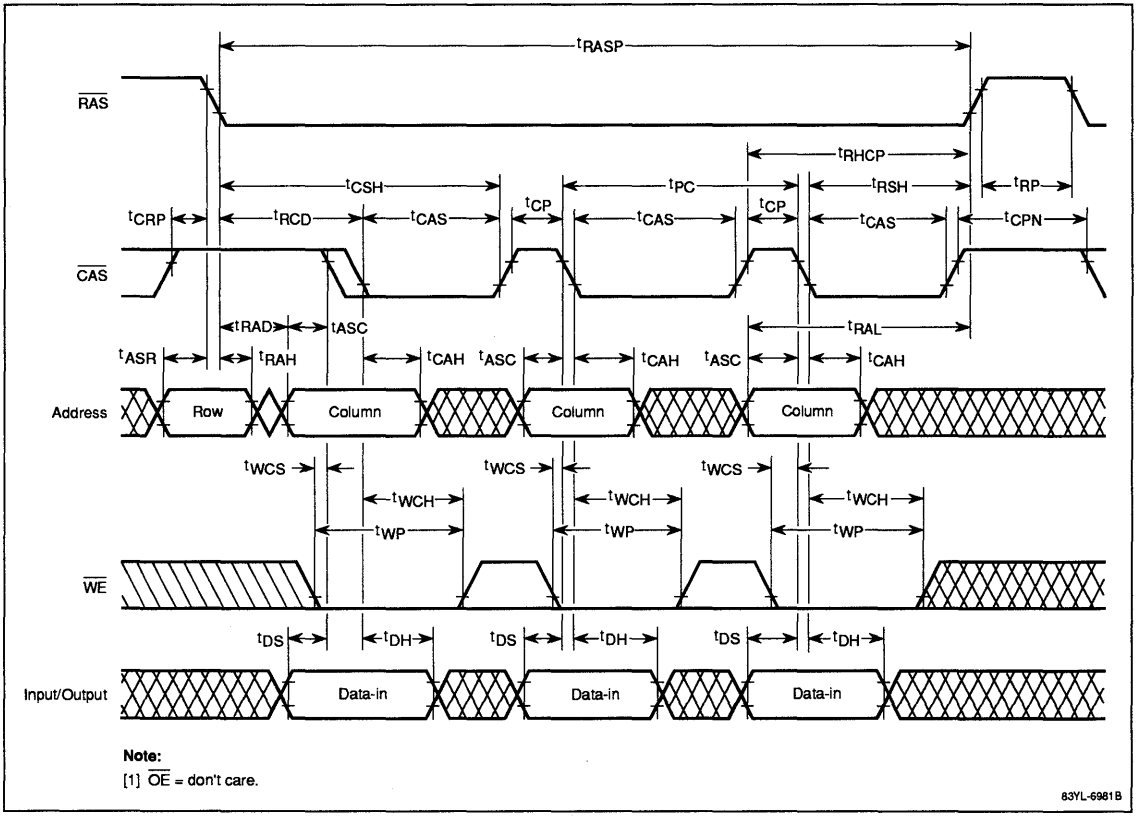
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



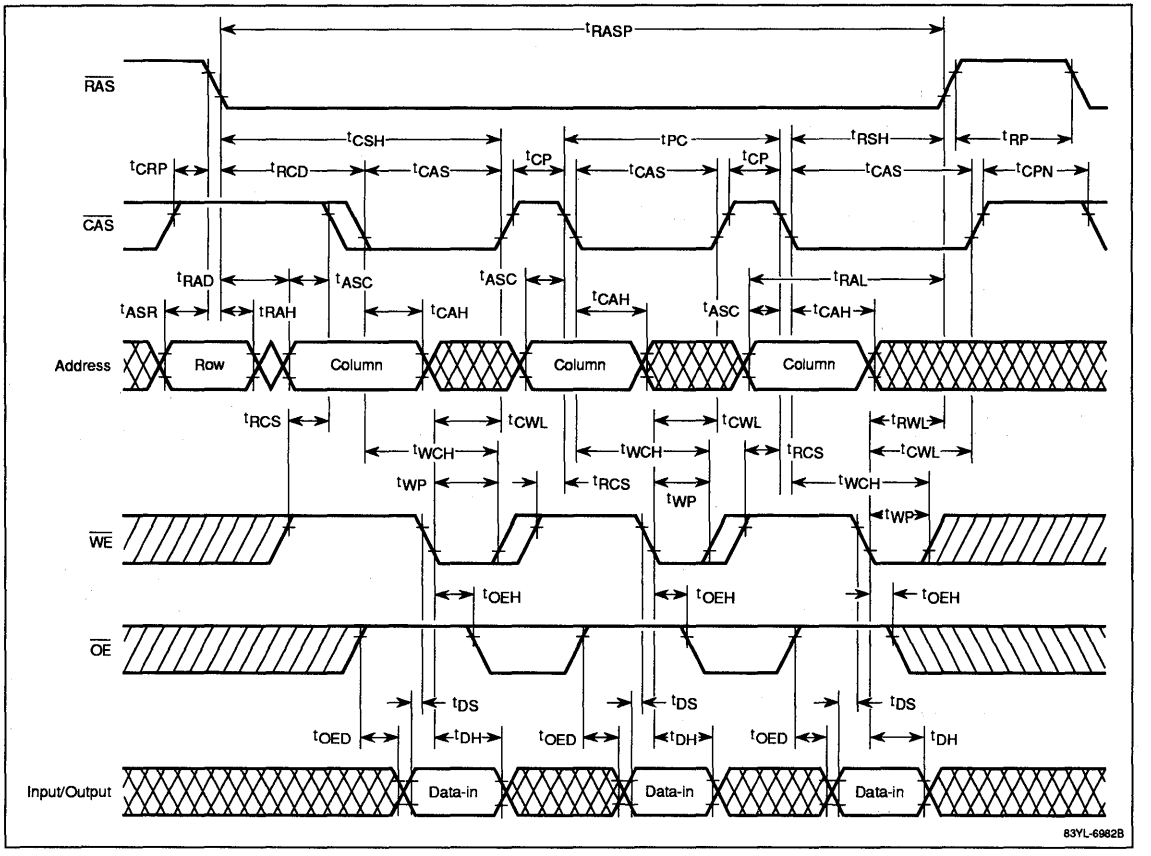
Note:

[1] $\overline{OE}$ = don't care.

83YL-6981B

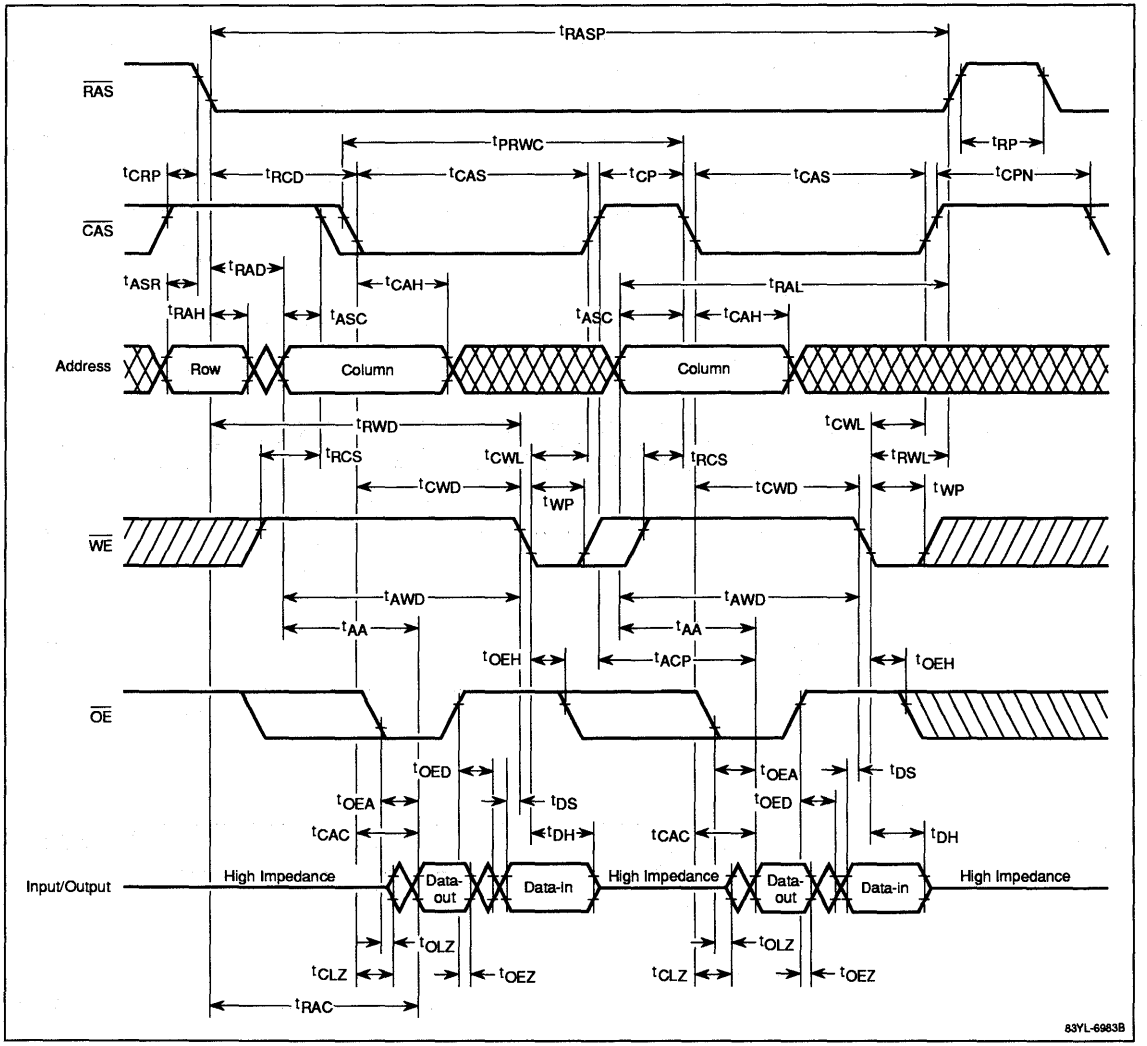
Timing Waveforms (cont)

Fast-Page Late Write Cycle



Timing Waveforms (cont)

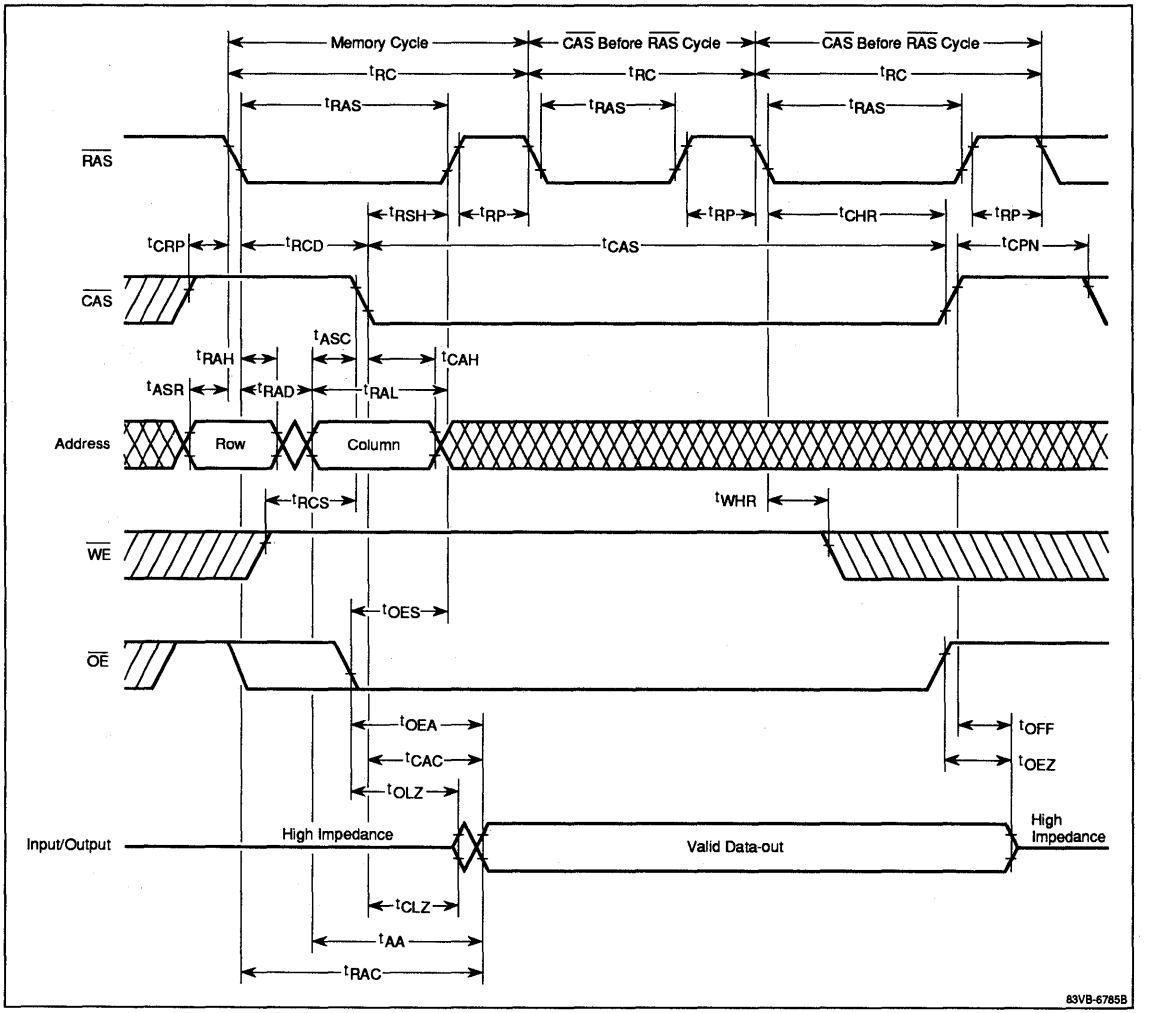
Fast-Page Read-Write/Read-Modify-Write Cycle



8d

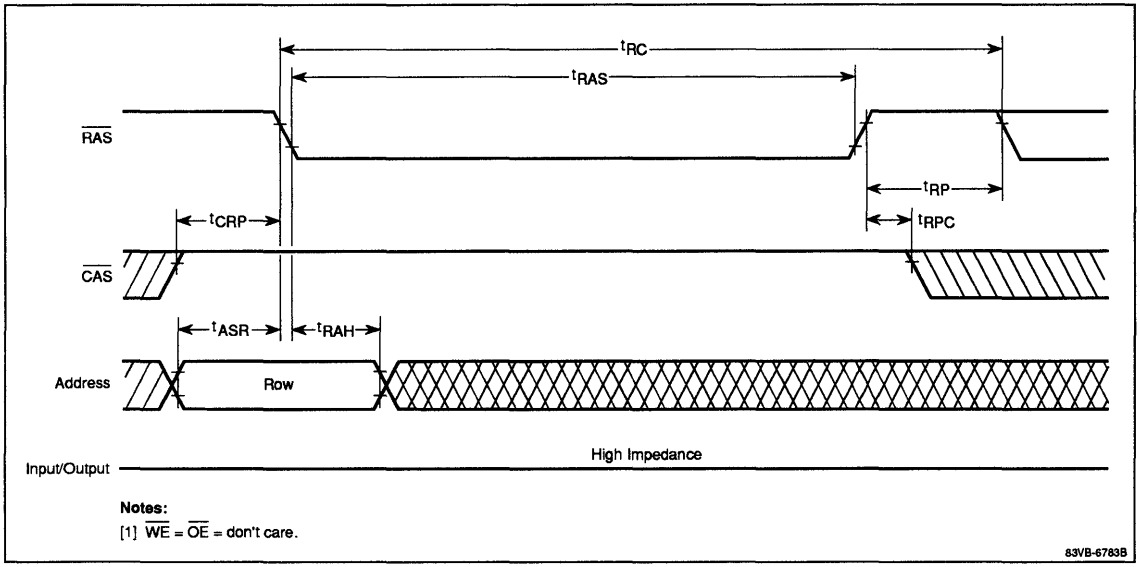
Timing Waveforms (cont)

Hidden Refresh Cycle



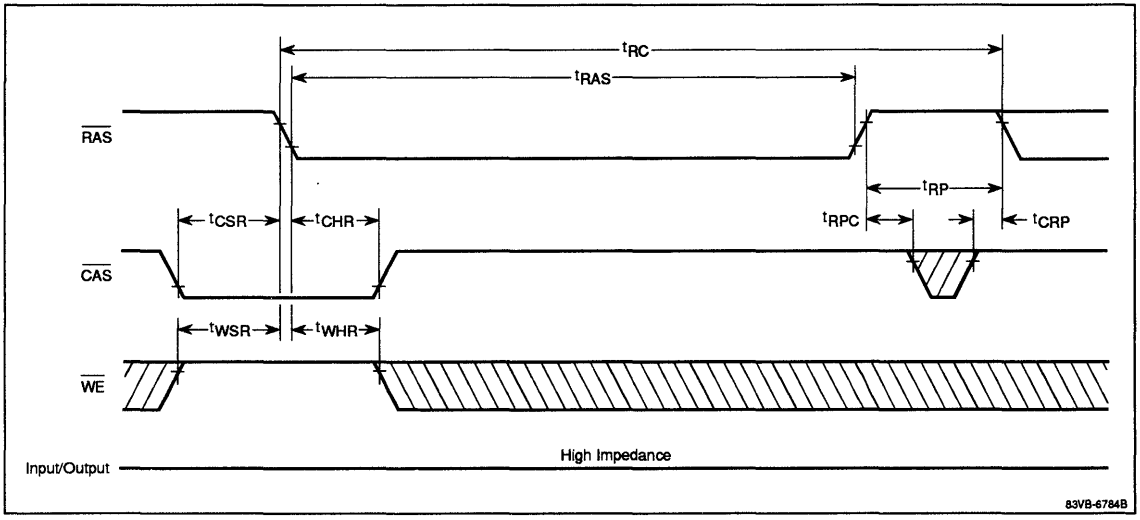
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Notes:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



8d

NEC Electronics Inc.

μPD4216402, 4217402
4,194,304 x 4-Bit Dynamic CMOS RAM

Advance Information

Description

The μPD4216402 and the μPD4217402 are static-column dynamic RAMs organized as 4,194,304 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. Data outputs return to high impedance when $\overline{CS}$ goes high. Static-column read and write cycles can be executed by cycling $\overline{CS}$.

Refreshing may be accomplished by a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by $\overline{RAS}$-only refresh cycles or by normal read or write cycles.

Two versions of the 4,194,304 by 4-bit static-column dynamic RAM are available. The μPD4216402 version uses 4096 address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period. The μPD4217402 version uses 2048 address combinations of A_0 - A_{10} to refresh the memory during a 32-ms refresh period.

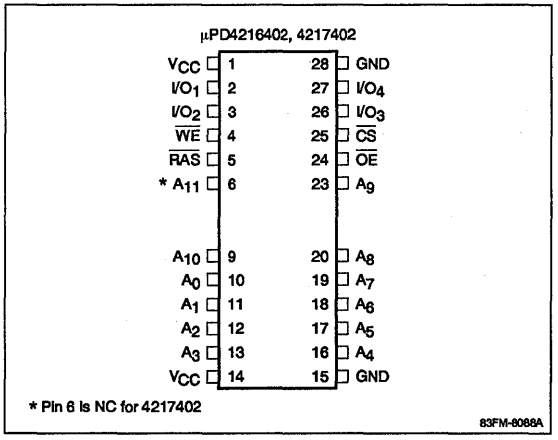
To access the memory during read, write, and read-modify-write cycles, the μPD4216402 uses row address combinations of A_0 - A_{11} and column address combinations of A_0 - A_9. The μPD4217402 uses row and colum address combinations of A_0 - A_{10}.

Features

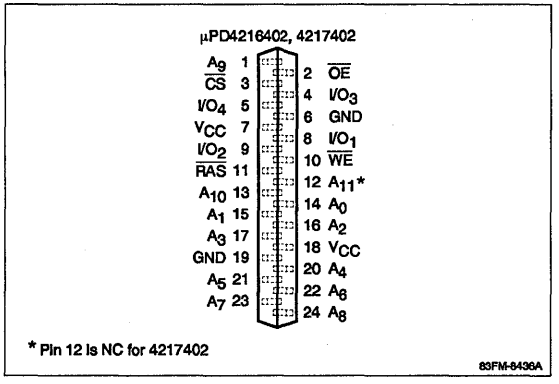
- 4,194,304 by 4-bit organization
- Single +5-volt power supply
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 4096 refresh cycles every 64 ms (4216402); 2048 refresh cycles every 32 ms (4217402)
- 28/24-pin SOJ (400-mil), 24-pin ZIP (475-mil), and 28/24-pin TSOP plastic packaging

Pin Configurations

28/24-Pin Plastic SOJ



24-Pin Plastic ZIP

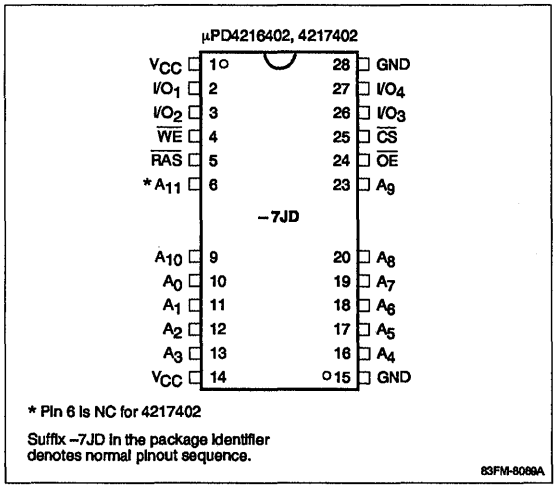


8e

Contact your NEC sales representative for a complete data sheet and product availability.

Pin Configurations (cont)

28/24-Pin Plastic TSOP (Normal Pinouts)

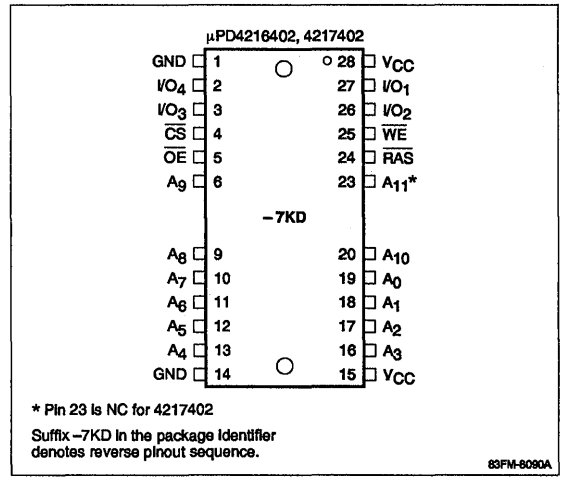


* Pin 6 is NC for 4217402

Suffix –7JD in the package identifier denotes normal pinout sequence.

83FM-8088A

28/24-Pin Plastic TSOP (Reverse Pinouts)

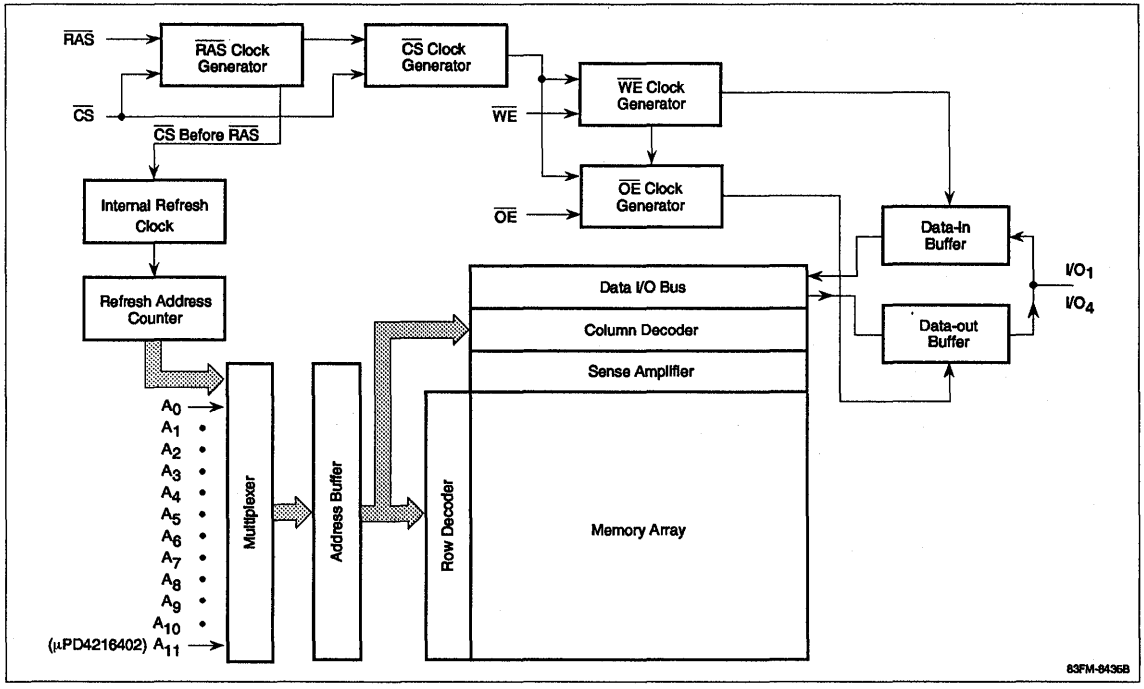


* Pin 23 is NC for 4217402

Suffix –7KD in the package identifier denotes reverse pinout sequence.

83FM-8090A

Block Diagram



83FM-8436B

Ordering Information, μPD4216402

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Number of Refresh Cycles	Package
μPD4216402LE-60	60 ns	110 ns	40 ns	4096	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns		
LE-80	80 ns	150 ns	50 ns		
LE-10	100 ns	180 ns	60 ns		
μPD4216402V-60	60 ns	110 ns	40 ns	4096	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns		
V-80	80 ns	150 ns	50 ns		
V-10	100 ns	180 ns	60 ns		
μPD4216402G5-60	60 ns	110 ns	40 ns	4096	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns		
G5-80	80 ns	150 ns	50 ns		
μPD4216402G5M-60	60 ns	110 ns	40 ns	4096	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns		
G5M-80	80 ns	150 ns	50 ns		

Ordering Information, μPD4217402

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Number of Refresh Cycles	Package
μPD4217402LE-60	60 ns	110 ns	40 ns	2048	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns		
LE-80	80 ns	150 ns	50 ns		
LE-10	100 ns	180 ns	60 ns		
μPD4217402V-60	60 ns	110 ns	40 ns	2048	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns		
V-80	80 ns	150 ns	50 ns		
V-10	100 ns	180 ns	60 ns		
μPD4217402G5-60	60 ns	110 ns	40 ns	2048	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns		
G5-80	80 ns	150 ns	50 ns		
μPD4217402G5M-60	60 ns	110 ns	40 ns	2048	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns		
G5M-80	80 ns	150 ns	50 ns		

NEC Electronics Inc.

μPD4216410, 4217410
4,194,304 x 4-Bit
Dynamic CMOS RAM

Advance Information

Description

The μPD4216410 and the μPD4217410 are fast-page dynamic RAMs with write per-bit organized as 4,194,304 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by $\overline{RAS}$-only refresh cycles or by normal read or write cycles.

Two versions of the 4,194,304 by 4-bit fast-page dynamic RAM with write-per-bit are available. The μPD4216410 version uses 4096 address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period. The μPD4217410 version uses 2048 address combinations of A_0 - A_{10} to refresh the memory during a 32-ms refresh period.

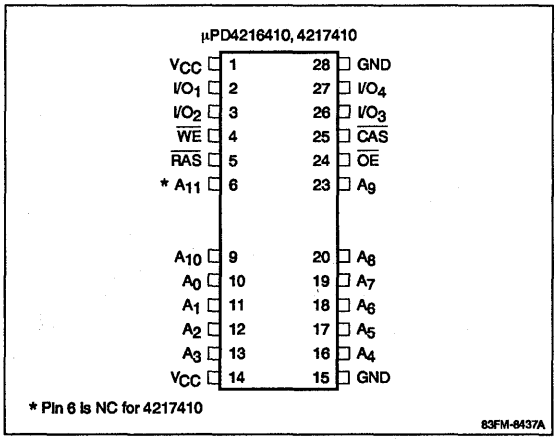
To access the memory during read, write, and read-modify-write cycles, the μPD4216410 uses row address combinations of A_0 - A_{11} and column address combinations of A_0 - A_9. The μPD4217410 uses row and colum address combinations of A_0 - A_{10}.

Features

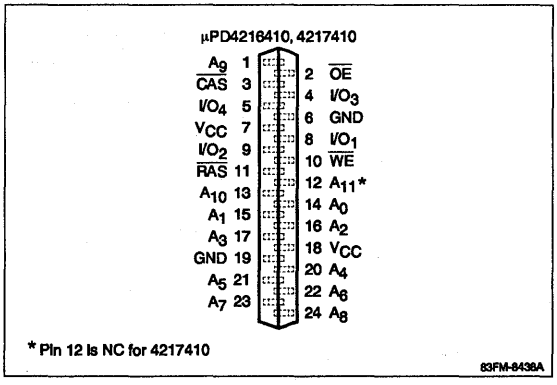
- 4,194,304 by 4-bit organization
- Single +5-volt power supply
- Fast-page option with write-per-bit
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 4096 refresh cycles every 64 ms (4216410); 2048 refresh cycles every 32 ms (4217410)
- 28/24-pin plastic SOJ (400 mil), 24-pin plastic ZIP (475 mil), and 28/24-pin plastic TSOP packaging

Pin Configurations

28/24-Pin Plastic SOJ



24-Pin Plastic ZIP



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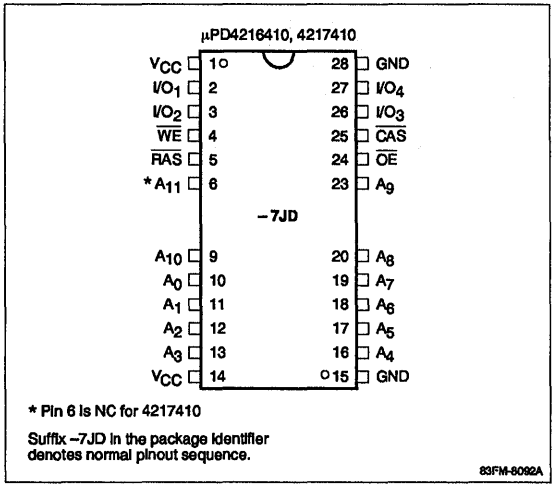
Contact your NEC sales representative for complete data sheet and product availability.

Pin Configurations (cont)

28/24-Pin Plastic TSOP (Normal Pinouts)

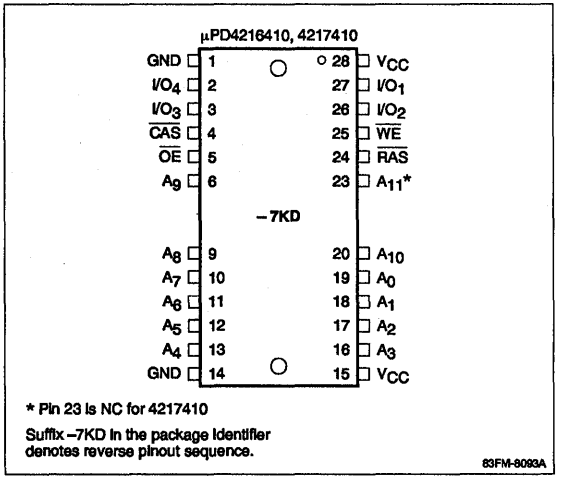


* Pin 6 is NC for 4217410

Suffix –7JD in the package identifier denotes normal pinout sequence.

83FM-8092A

28/24-Pin Plastic TSOP (Reverse Pinouts)

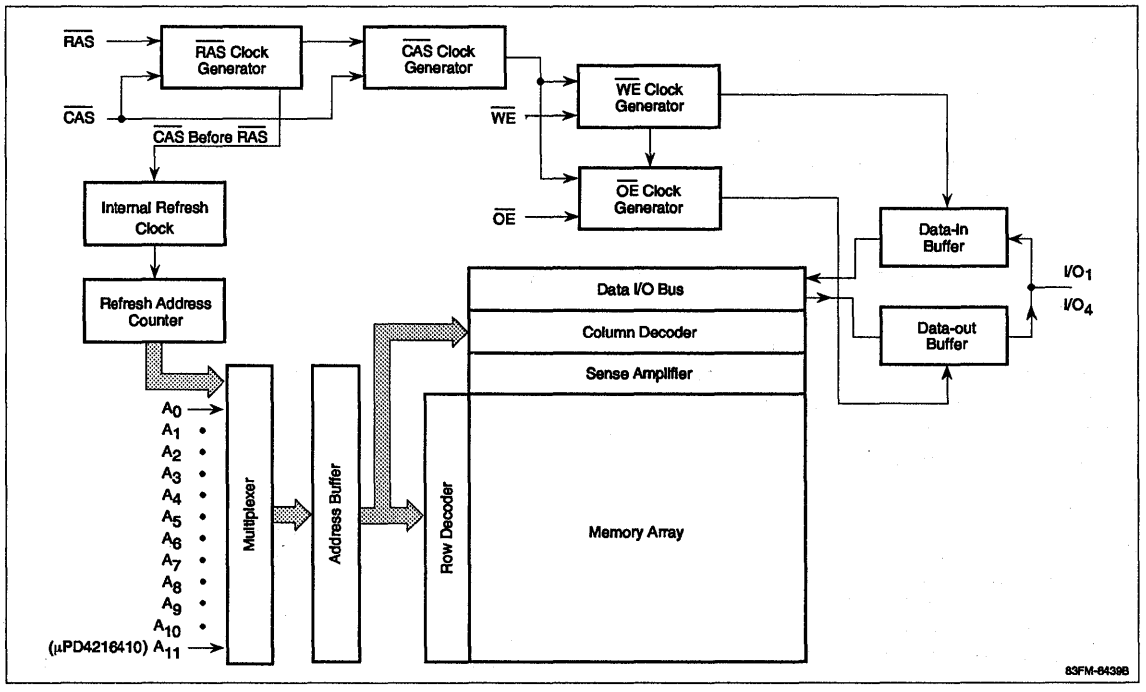


* Pin 23 is NC for 4217410

Suffix –7KD in the package identifier denotes reverse pinout sequence.

83FM-8093A

Block Diagram



83FM-8439B

Ordering Information, μPD4216410 (4096 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD4216410LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4216410V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4216410G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4216410G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	

Ordering Information, μPD4217410 (2048 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD4217410LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4217410V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4217410G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4217410G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	

NEC Electronics Inc.

μPD4216412, 4217412
4,194,304 x 4-Bit
Dynamic CMOS RAM

Advance Information

Description

The μPD4216412 and the μPD4217412 are static-column dynamic RAMs with write-per-bit organized as 4,194,304 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. Data outputs return to high impedance when $\overline{CS}$ goes high. Static-column read and write cycles can be executed by cycling $\overline{CS}$.

Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles.

Two versions of the 4,194,304 by 4-bit static-column dynamic RAM with write-per-bit are available. The μPD4216412 version uses 4096 address combinations of A_0 - A_{11} to refresh the memory during a 64-ms refresh period. The μPD4217412 version uses 2048 address combinations of A_0 - A_{10} to refresh the memory during a 32-ms refresh period.

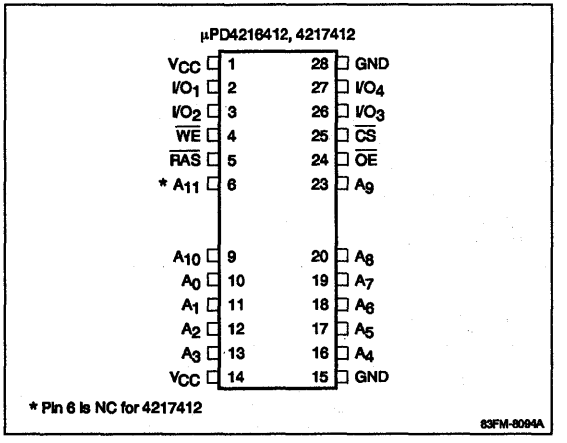
To access the memory during read, write, and read-modify-write cycles, the μPD4216412 uses row address combinations of A_0 - A_{11} and column address combinations of A_0 - A_9. The μPD4217412 uses row and colum address combinations of A_0 - A_{10}.

Features

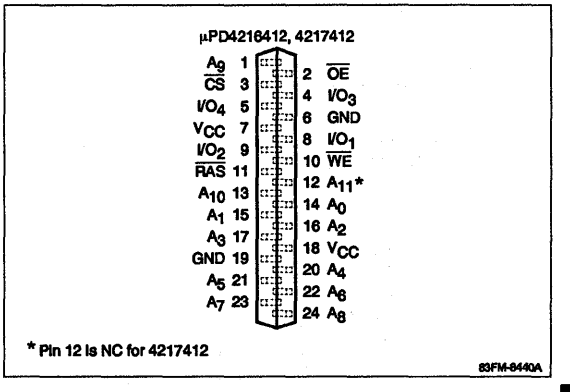
- 4,194,304 by 4-bit organization
- Single +5-volt power supply
- Static-column option with write-per-bit
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 4,096 refresh cycles every 64 ms (4216412); 2048 refresh cycles every 32 ms (4217412)
- 28/24-pin plastic SOJ (400 mil), 24-pin plastic ZIP (475 mil), and 28/24-pin plastic TSOP packaging

Pin Configurations

28/24-Pin Plastic SOJ



24-Pin Plastic ZIP

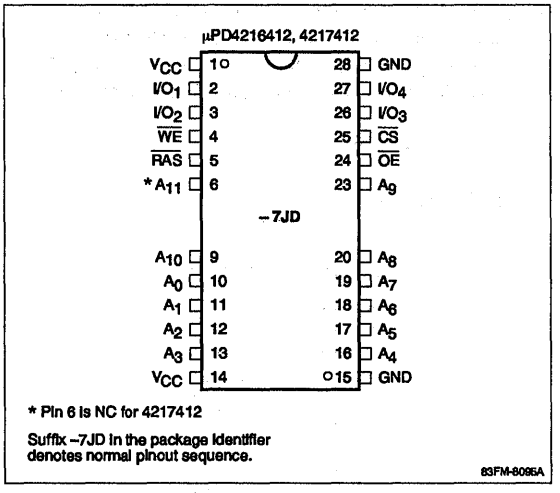


8g

Contact your NEC sales representative for a complete data sheet and product availability.

Pin Configurations (cont)

28/24-Pin Plastic TSOP (Normal Pinouts)

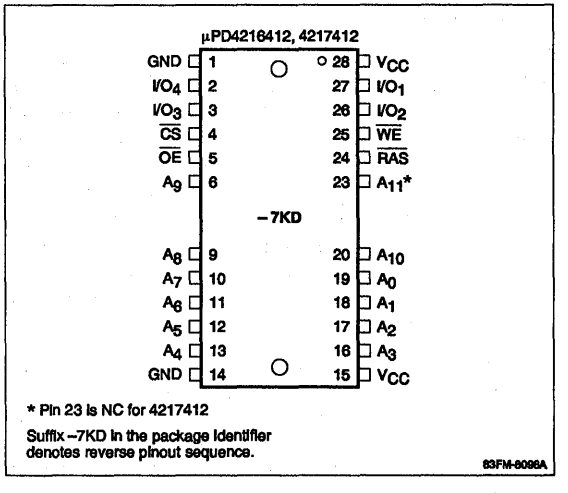


* Pin 6 is NC for 4217412

Suffix –7JD in the package identifier denotes normal pinout sequence.

83FM-8096A

28/24-Pin Plastic TSOP (Reverse Pinouts)

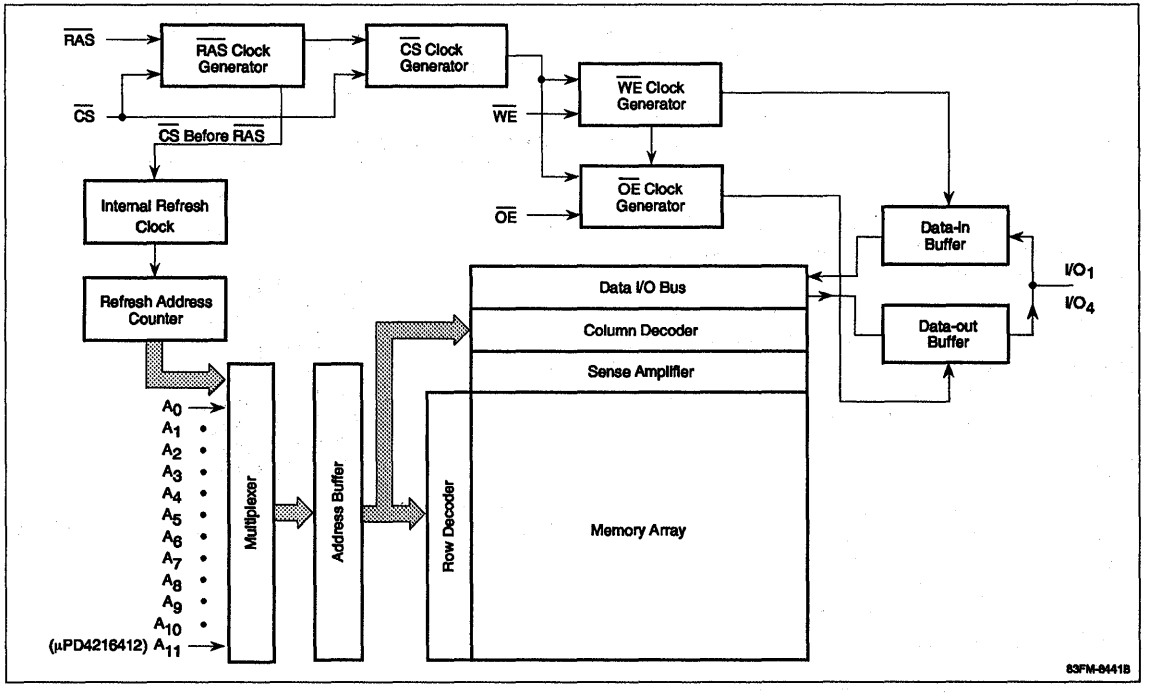


* Pin 23 is NC for 4217412

Suffix –7KD in the package identifier denotes reverse pinout sequence.

83FM-8096A

Block Diagram



83FM-8441B

Ordering Information, μPD4216412 (4096 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Static-Column Cycle (max)	Package
μPD4216412LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4216412V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4216412G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4216412G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	

Ordering Information, μPD4217412 (2048 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Static-Column Cycle (max)	Package
μPD4217412LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4217412V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4217412G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4217412G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	

μPD421x800/L, 42S1x800/L (x = 6, 7) 2,097,152 x 8-Bit Dynamic CMOS RAM

Description

The devices listed below are fast-page dynamic RAMs organized as 2M words by 8 bits and designed to operate from a single power supply. Optional features are power supply voltage (+5 V or +3.3 V), a new refresh mode called "self-refresh," and the number of cycles in a refresh period.

μPD	Power	Self-Refresh	Refresh Cycles
4216800	+5 V	—	4096 in 64 ms
800L	+3.3 V	—	
42S16800	+5 V	√	4096 in 256 ms
800L	+3.3 V	√	
4217800	+5 V	—	2048 in 32 ms
800L	+3.3 V	—	
42S17800	+5 V	√	2048 in 256 ms
800L	+3.3 V	√	

Note: Letters L and S denote 3.3-volt and self-refresh devices, respectively.

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation while an on-chip circuit internally generates the negative voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh addresses.

For the 4216/42S16, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 4096 address combinations of A_0 - A_{11} will refresh all memory locations. Bits A_0 - A_{11} are used for row and refresh addresses, A_0 - A_8 for column addresses.

For the 4217/42S17, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 2048 address combinations of A_0 - A_{10} will refresh all memory locations. Bits A_0 - A_{10} are used for row and refresh addresses, A_0 - A_9 for column addresses.

The self-refresh mode is entered by holding $\overline{RAS}$ and $\overline{CAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 μA (+5 V) or 80 μA (+3.3 V). Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

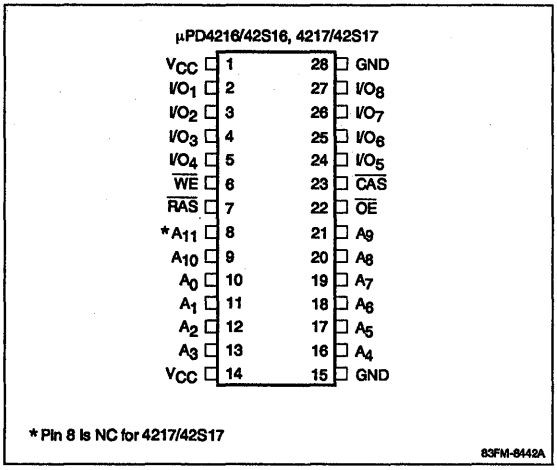
Battery backup current I_{CC6} is defined as the current consumption when the device is in standby mode ($\overline{RAS} \geq V_{CC} - 0.2$ V) and very-slow (extended) CBR cycles are being performed.

Features

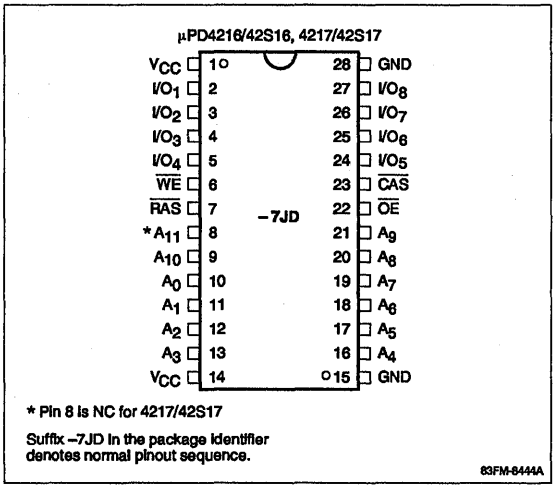
- 2,097,152 by 8-bit organization
- Single power supply: +5-volt or +3.3 volt
- Fast-page option
- Low-power operation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Self-refresh option (slow internal automatic refresh)
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 28-pin 400-mil SOJ and TSOP plastic packages

Pin Configurations

28-Pin Plastic SOJ



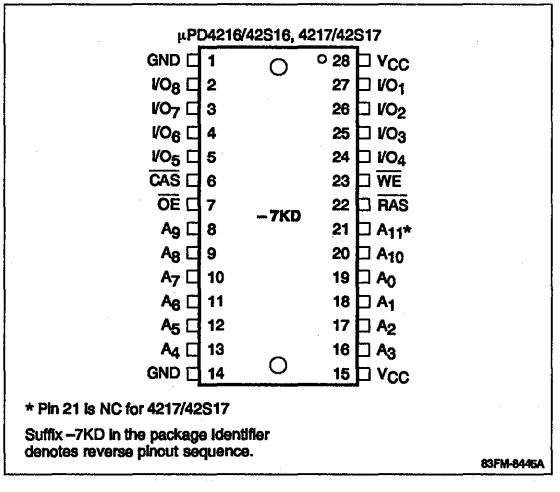
28-Pin Plastic TSOP (Normal Pinouts)



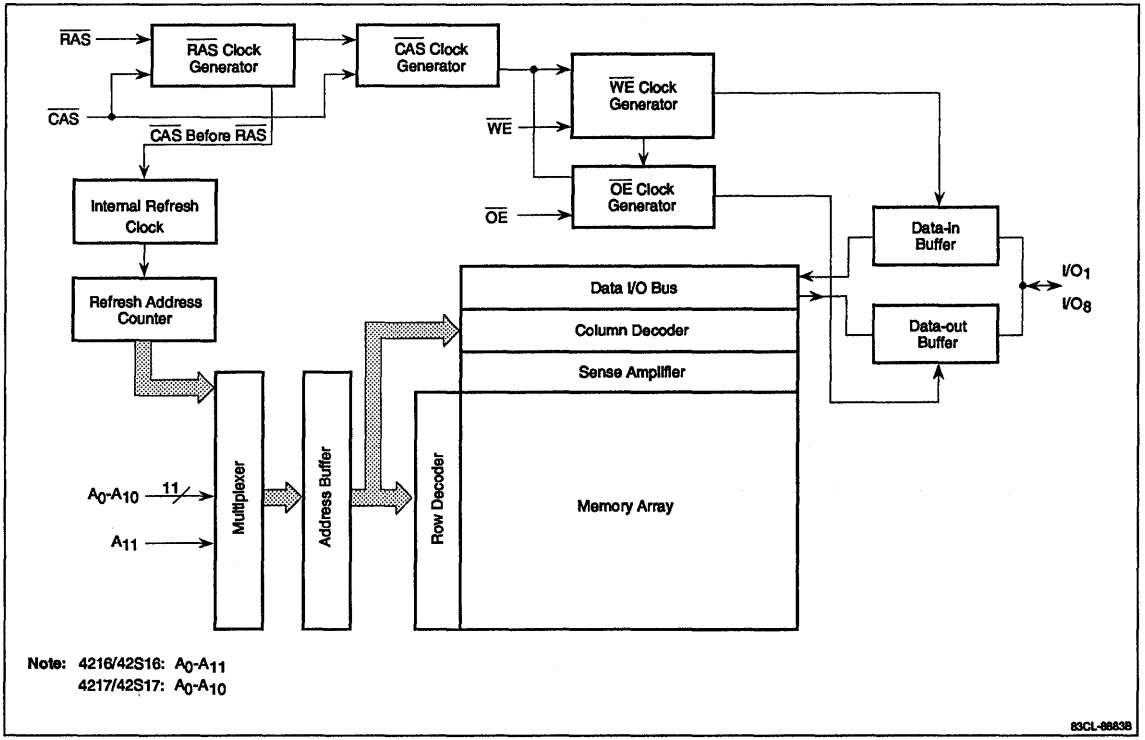
Pin Identification

Name	Function
A_0 - A_{11}	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

28-Pin Plastic TSOP (Reverse Pinouts)



Block Diagram



Truth Table

Function	RAS	CAS	WE	OE	I/O_1 - I/O_8
Standby	H	X	X	X	High-Z
Refresh cycle	L	H	X	X	High-Z
Byte read cycle	L	L	H	L	Data output
	L	H	H	L	High-Z
Byte write cycle	L	L	L	H	Data input
	L	H	L	H	—
——	L	L	H	H	High-Z

X = don't care.

8h

Ordering Information, μPD4216800 (+ 5-volt power; 4096 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4216800LE-50	50 ns	35 ns	350 μA	28-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD4216800G5-50	50 ns	35 ns	350 μA	28-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD4216800G5M-50	50 ns	35 ns	350 μA	28-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD4216800L (+ 3.3-volt power; 4096 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4216800LLE-A60	60 ns	40 ns	140 μA	28-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD4216800LG5-A60	60 ns	40 ns	140 μA	28-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD4216800LG5M-A60	60 ns	40 ns	140 μA	28-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD42S16800 (+ 5-volt power; 4096 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S16800LE-50	50 ns	35 ns	350 μA	28-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD42S16800G5-50	50 ns	35 ns	350 μA	28-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD42S16800G5M-50	50 ns	35 ns	350 μA	28-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD42S16800L (+ 3.3-volt power; 4096 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S16800LLE-A60	60 ns	40 ns	140 μA	28-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD42S16800LG5-A60	60 ns	40 ns	140 μA	28-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD42S16800LG5M-A60	60 ns	40 ns	140 μA	28-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD4217800 (+5-volt power; 2048 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4217800LE-50	50 ns	35 ns	300 μA	28-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD4217800G5-50	50 ns	35 ns	300 μA	28-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD4217800G5M-50	50 ns	35 ns	300 μA	28-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD4217800L (+3.3-volt power; 2048 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4217800LLE-A60	60 ns	40 ns	120 μA	28-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD4217800LG5-A60	60 ns	40 ns	120 μA	28-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD4217800LG5M-A60	60 ns	40 ns	120 μA	28-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD42S17800 (+ 5-volt power; 2048 refresh cycles; self-refresh mode)

Part Number	RAS Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S17800LE-50	50 ns	35 ns	300 μA	28-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD42S17800G5-50	50 ns	35 ns	300 μA	28-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD42S17800G5M-50	50 ns	35 ns	300 μA	28-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD42S17800L (+ 3.3-volt power; 2048 refresh cycles; self-refresh mode)

Part Number	RAS Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S17800LLE-A60	60 ns	40 ns	120 μA	28-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD42S17800LG5-A60	60 ns	40 ns	120 μA	28-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD42S17800LG5M-A60	60 ns	40 ns	120 μA	28-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to + 4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_8

Recommended Operating Conditions

		5-Volt Devices			3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		70	0		70	°C

Self-Refresh Current; 42S1x Devices

T_A = 0 to +70°C; V_{CC} = +5 V ±10% or +3.3 V ±0.3 V

Symbol	5-Volt Devices	3.3-Volt Devices	Conditions
I_{CC7}	200 μA max	80 μA max	I/O pins: $V_{IH} \geq V_{CC}$ −0.2 V; $V_{IL} \leq$ 0.2 V or open. Other input pins: $V_{IH} \geq V_{CC}$ −0.2 V; $V_{IL} \leq$ 0.2 V or open; $t_{RAS} \geq$ 100 μs

DC Characteristics; 5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				400	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

DC Characteristics; 3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				400	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

DC Current Requirements; 5-Volt Devices

Parameter	Symbol	-50	-60	-70	-80	Unit	Test Conditions
Operating current	I_{CC1}						
4216/42S16		100	90	80	70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} (min); I_O = 0 mA
4217/42S17		120	110	100	90	mA	
Refresh current ($\overline{RAS}$ only refresh)	I_{CC3}						
4216/42S16		100	90	80	70	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} (min); t_{RC} = t_{RC} (min); I_O = 0 mA
4217/42S17		120	110	100	90	mA	
Operating current (Fast-page mode)	I_{CC4}						
4216/42S16		80	70	60	50	mA	$\overline{CAS}$ cycling; $\overline{RAS}$ ≤ V_{IL} (max); t_{PC} = t_{PC} (min); I_O = 0 mA
4217/42S17		80	70	60	50	mA	
Refresh current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}						
4216/42S16		100	90	80	70	mA	$\overline{RAS}$ cycling; t_{RC} = t_{RC} (min); I_O = 0 mA
4217/42S17		120	110	100	90	mA	
Battery backup current (Standby with $\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RAS} ≤ 300 ns		t_{RAS} ≤ 1 μs			Standby: $\overline{RAS}$ ≥ V_{CC} – 0.2 V; $\overline{RAS}$, $\overline{CAS}$: 0 V ≤ V_{IL} ≤ 0.2 V, V_{CC} – 0.2 V ≤ V_{IH} ≤ V_{IH} (max); $\overline{WE}$, $\overline{OE}$: V_{IH}; Address: don't care; Output: open
42S16		350		500		μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 4096 cycles, 256 ms
42S17		300		400		μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 2048 cycles, 256 ms

DC Current Requirements; 3.3-Volt Devices

Parameter	Symbol	-A60	-A70	-A80	Unit	Test Conditions
Operating current	I_{CC1}					
4216/42S16		80	70	60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ (min); I_O = 0 mA
4217/42S17		100	90	80	mA	
Refresh current ($\overline{RAS}$ only refresh)	I_{CC3}					
4216/42S16		80	70	60	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$ (min); $t_{RC} = t_{RC}$ (min); I_O = 0 mA
4217/42S17		100	90	80	mA	
Operating current (Fast-page mode)	I_{CC4}					
4216/42S16		60	50	40	mA	$\overline{CAS}$ cycling; $\overline{RAS} \leq V_{IL}$ (max); $t_{PC} = t_{PC}$ (min); I_O = 0 mA
4217/42S17		60	50	40	mA	
Refresh current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}					
4216/42S16		80	70	60	mA	$\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ (min); I_O = 0 mA
4217/42S17		100	90	80	mA	
Battery backup current (Standby with $\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$t_{RAS} \leq 300$ ns		$t_{RAS} \leq 1$ μs		Standby: $\overline{RAS} \geq V_{CC} - 0.2$ V; $\overline{RAS}$, $\overline{CAS}$: 0 V ≤ V_{IL} ≤ 0.2 V, $V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH}$ (max); $\overline{WE}$, $\overline{OE}$: V_{IH}; Address: don't care; Output: open
42S16		140		140	μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 4096 cycles, 256 ms
42S17		120		120	μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 2048 cycles, 256 ms

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10% (-50, -60, -70, -80) or +3.3 V ±0.3 V (-A60, -A70, -A80)

		-50		-60, -A60		-70, -A70		-80, -A80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Access time from column address	t_{AA}		25		30		35		40	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		30		35		40		45	ns	(Note 7)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	45		53		60		65		ns	(Note 15)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		13		15		18		20	ns	(Notes 7, 8)
Column address hold time	t_{CAH}	13		15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	10		10		10		10		ns	
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	−50		−50		−50		−50		ns	(Note 16)
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		0		ns	(Note 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	8		10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	8		10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		65		70		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		5		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	33		38		43		45		ns	(Note 15)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	13		15		15		15		ns	
Data-in hold time	t_{DH}	10		10		15		15		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		13		15		18		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	10		13		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	0	15	ns	(Note 9)

8h

AC Characteristics (cont)

		-50		-60, -A60		-70, -A70		-80, -A80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Output disable from $\overline{CAS}$ high	t_{OFF}	0	10	0	13	0	15	0	15	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		0		ns	(Note 7)
Fast-page read or write cycle time	t_{PC}	35		40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with extended data output	t_{PRWC}	80		85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	15	35	17	40	ns	(Note 8)
Row address hold time	t_{RAH}	8		10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	25		30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		100		μs	(Note 16)
Random read or write cycle time	t_{RC}	90		110		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	20	45	20	50	25	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}										
4216			64		64		64		64	ms	
4217			32		32		32		32	ms	
42S16			256		256		256		256	ms	
42S17			256		256		256		256	ms	
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5		5		5		5		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	90		110		130		150		ns	(Note 16)
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	13		15		18		20		ns	
Read-modify-write cycle time	t_{RWC}	140		160		180		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	70		83		95		105		ns	(Note 15)

AC Characteristics (cont)

Parameter	Symbol	-50		-60, -A60		-70, -A70		-80, -A80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	18		20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	
Write command hold time	t_{WCH}	8		10		10		15		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 14)
Write command pulse width	t_{WP}	8		10		10		15		ns	(Note 12)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by eight refresh cycles ($\overline{RAS}$ only or CBR) before proper device operation is achieved.

(3) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(4) Ac measurements assume t_T = 5 ns.

(5) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max).
If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a late write cycle. For early write cycles, t_{WCH} must be met.

(13) These parameters are referenced to the leading edge of $\overline{CAS}$ in early write cycles and to the leading edge of $\overline{WE}$ in late write or read-modify-write cycles.

(14) If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle.

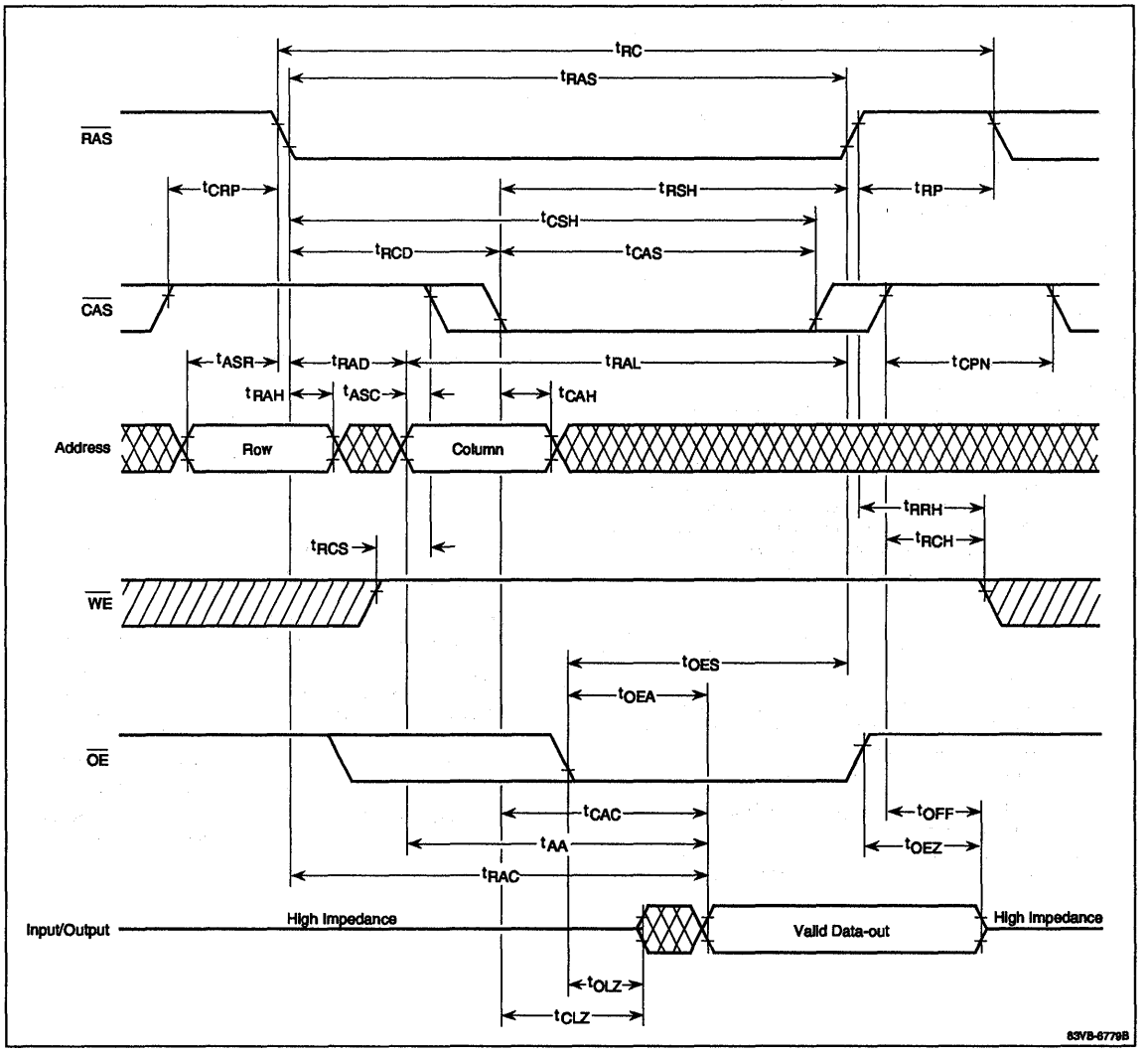
(15) If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(16) Parameter is applicable only to self-refresh versions.

(17) With burst CBR, $\overline{RAS}$ only, or external $\overline{RAS}/\overline{CAS}$, all addresses must be refreshed before entering self-refresh mode and after exiting.

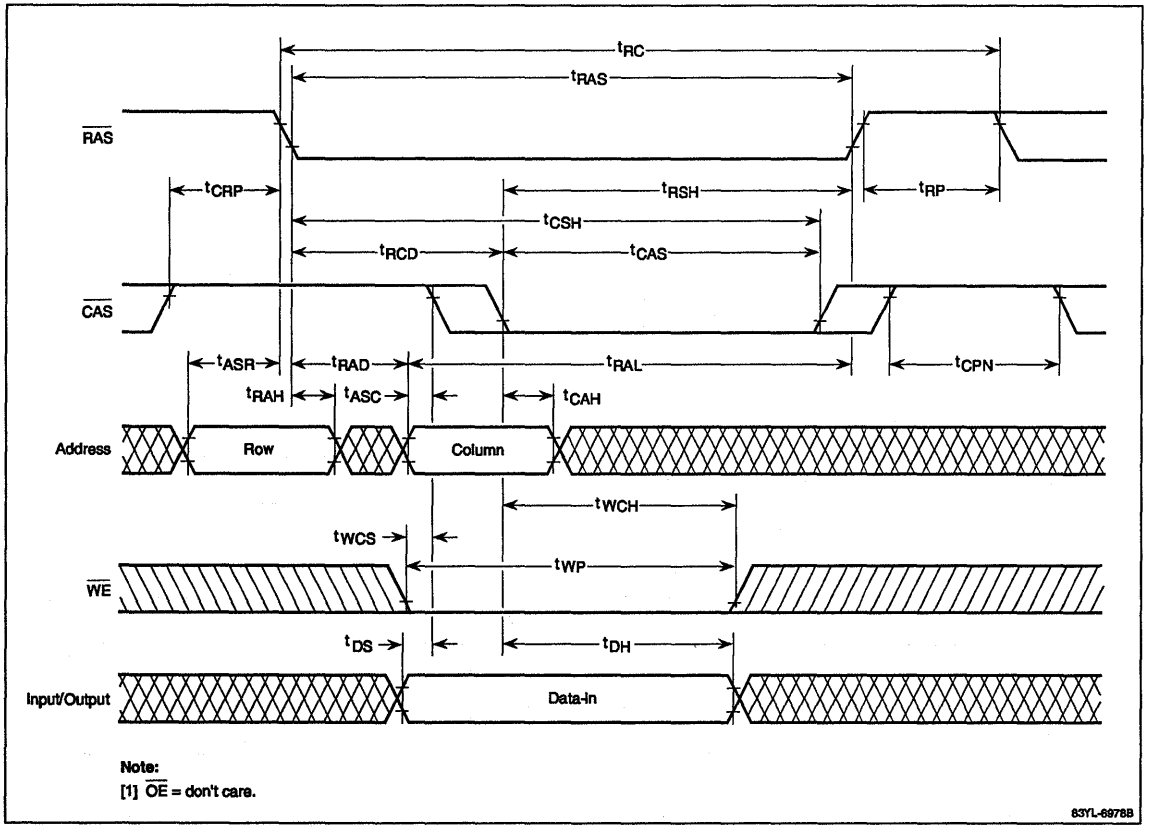
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early-Write Cycle

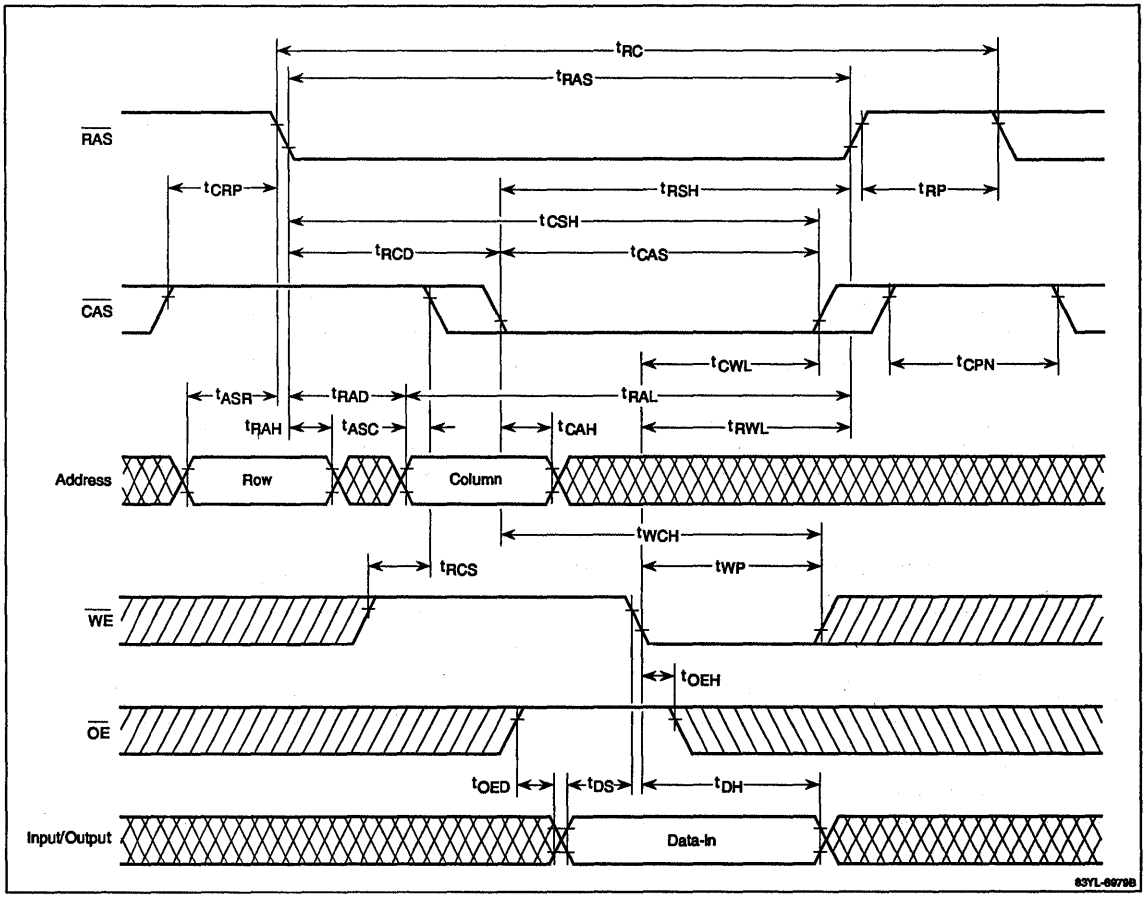


Note:
[1] $\overline{OE}$ = don't care.

83YL-6978B

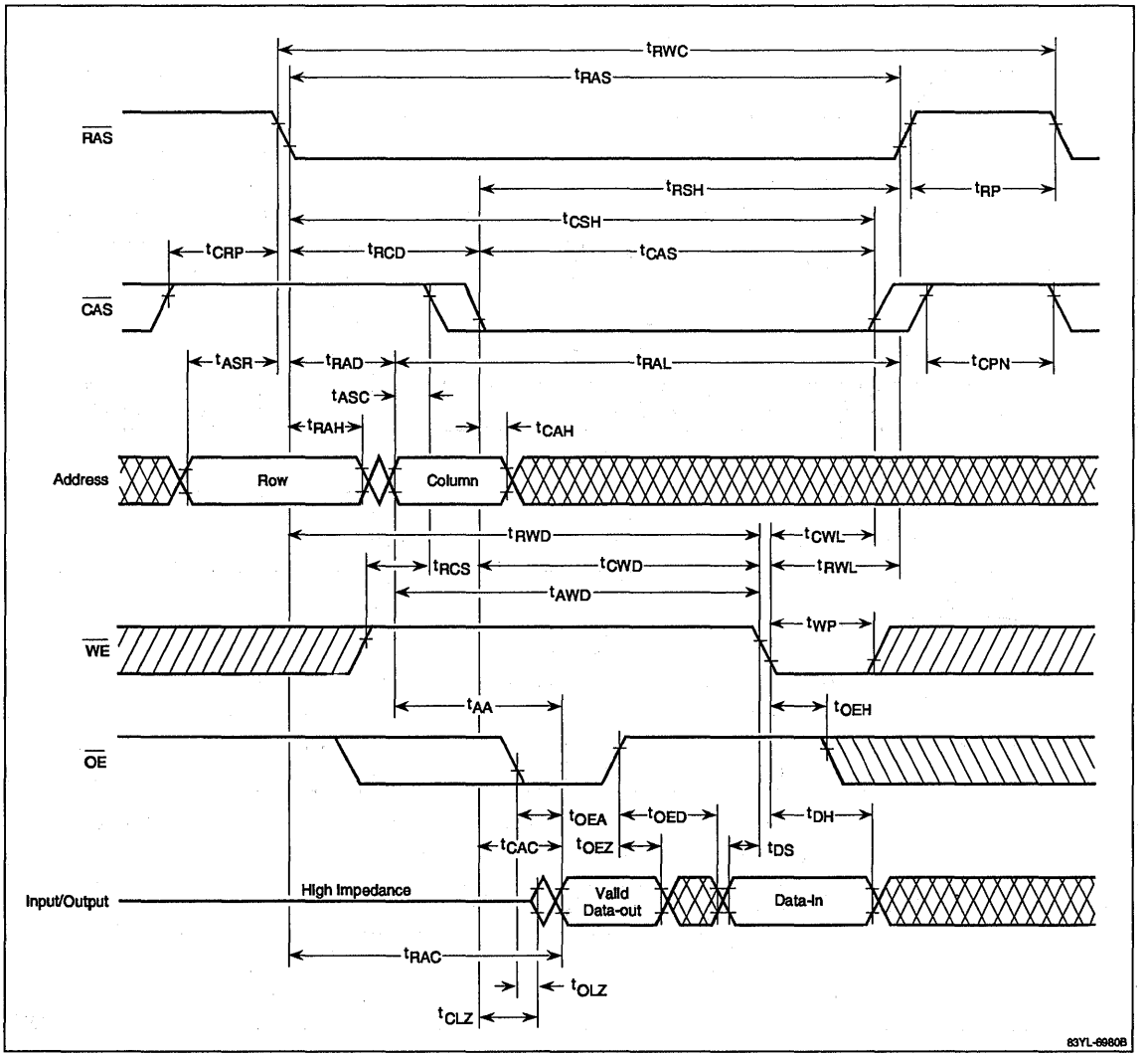
Timing Waveforms (cont)

Late-Write Cycle



Timing Waveforms (cont)

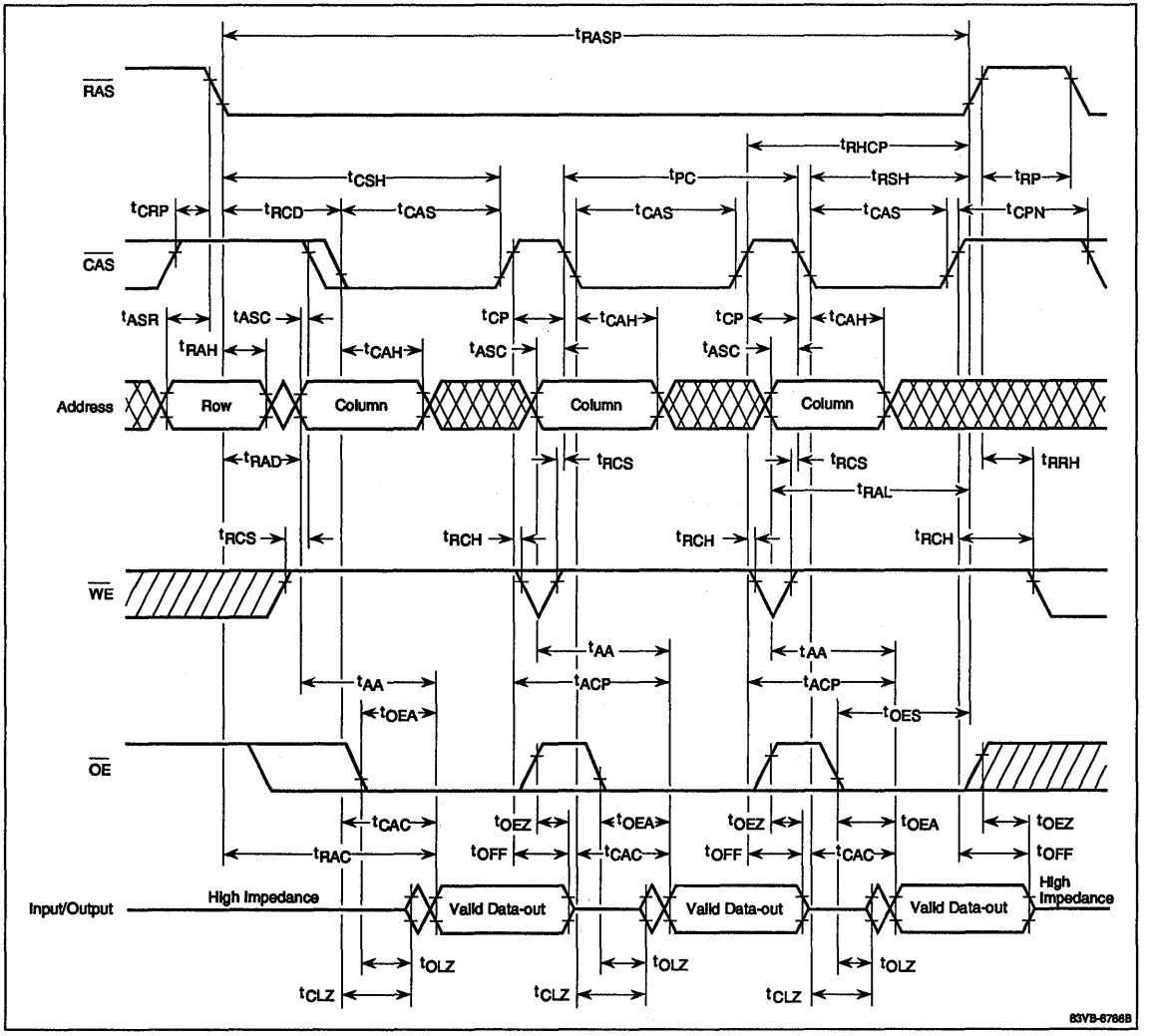
Read-Write/Read-Modify-Write Cycle



8h

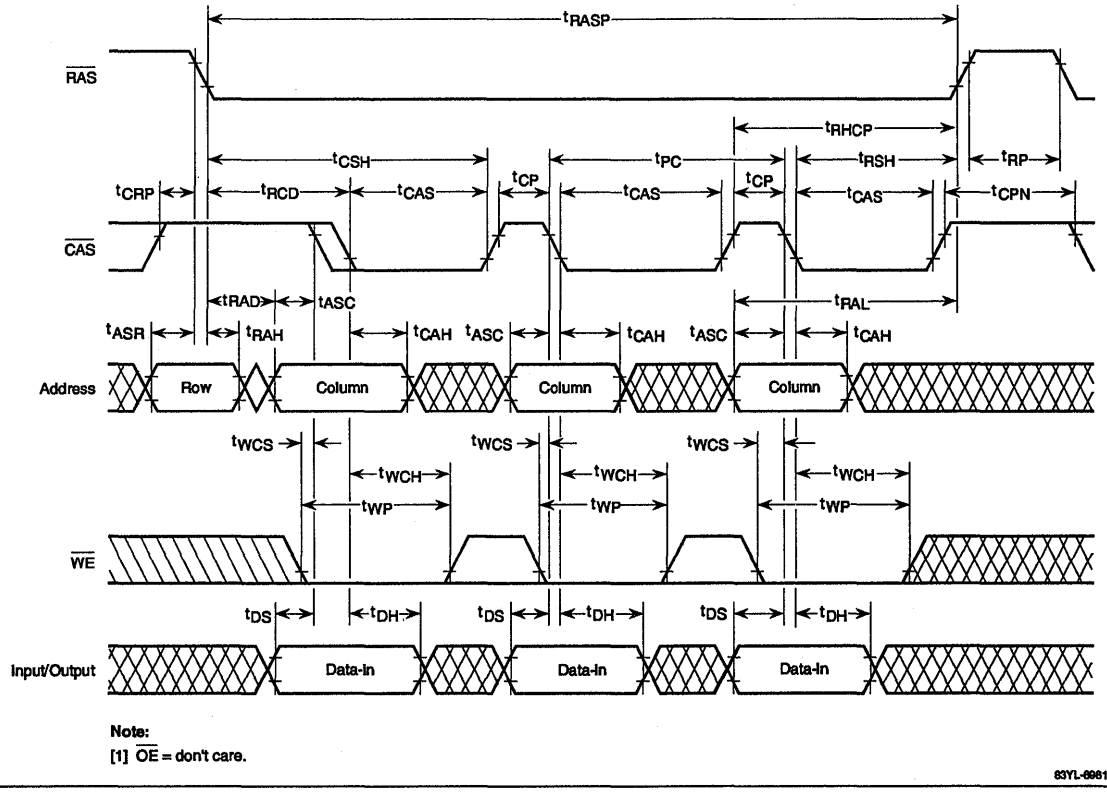
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early-Write Cycle



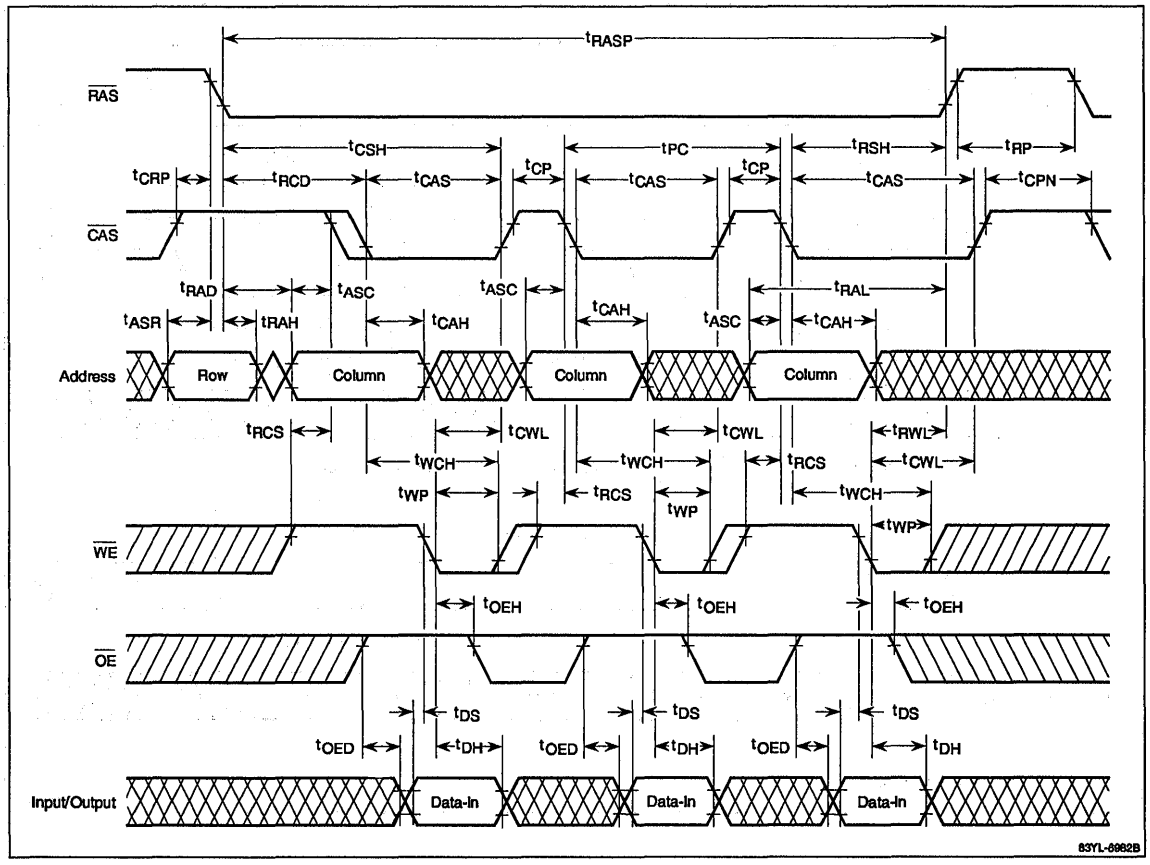
Note:
[1] $\overline{OE}$ = don't care.

83YL-8981B

8h

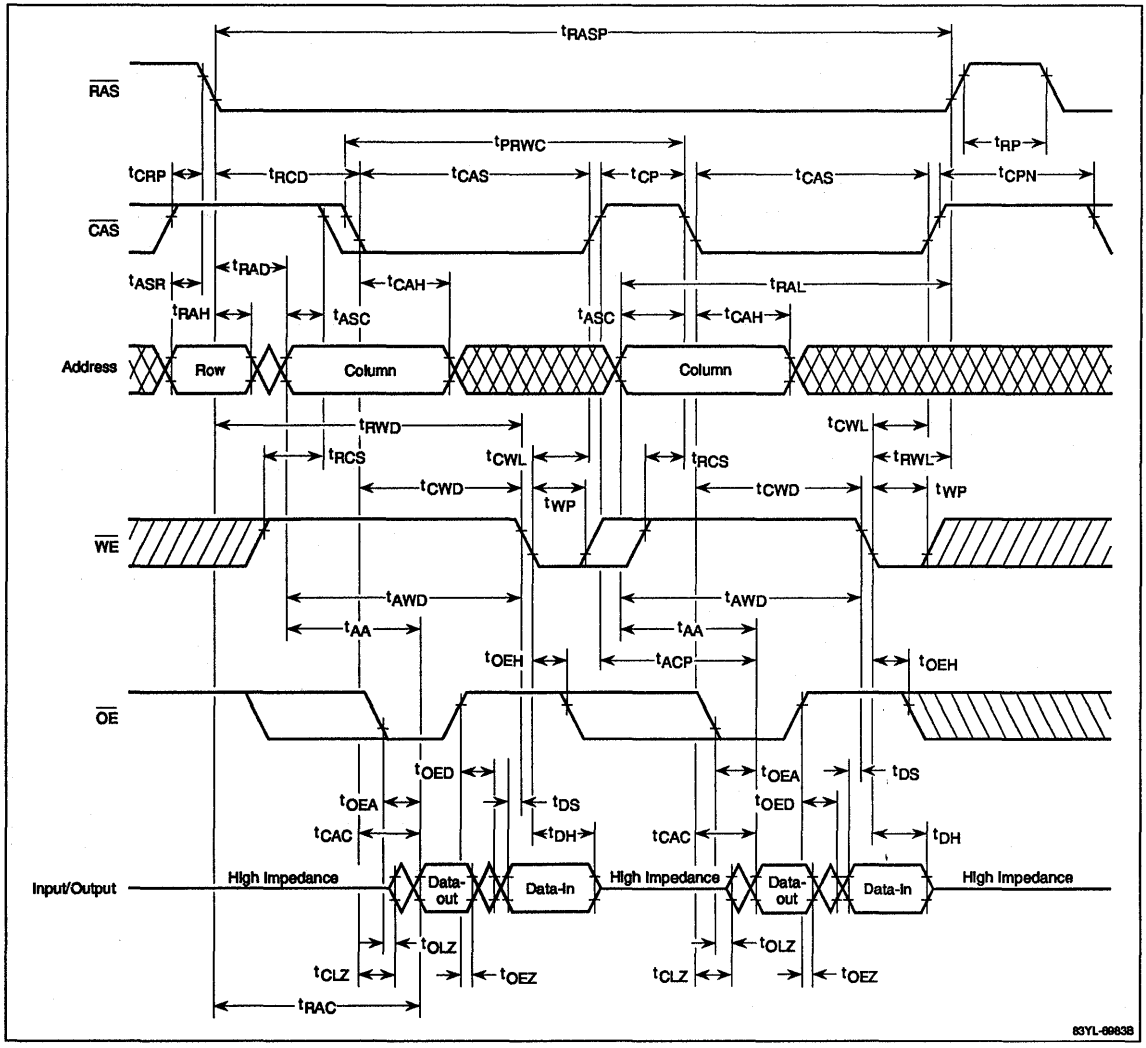
Timing Waveforms (cont)

Fast-Page Late-Write Cycle



Timing Waveforms (cont)

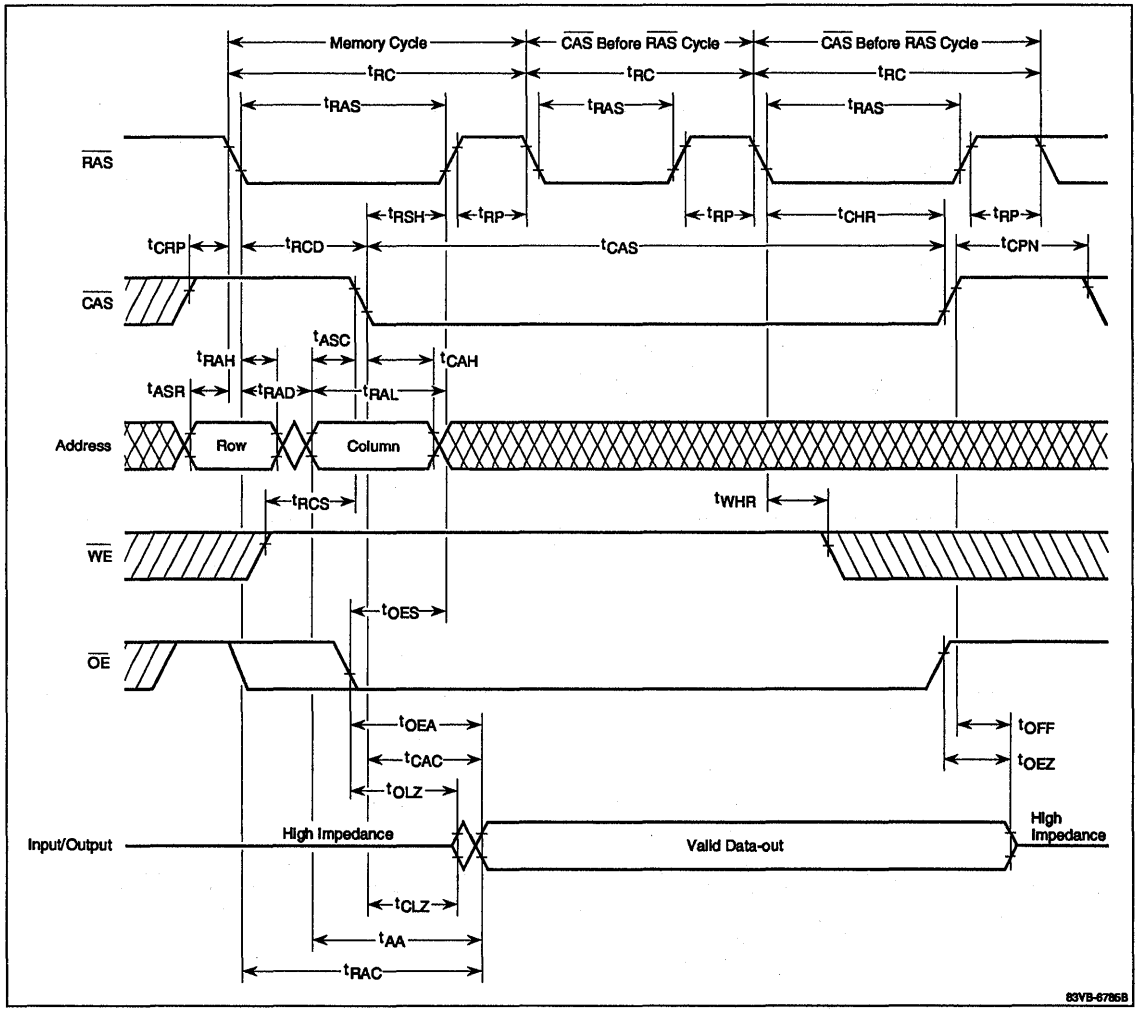
Fast-Page Read-Write/Read-Modify-Write Cycle



8h

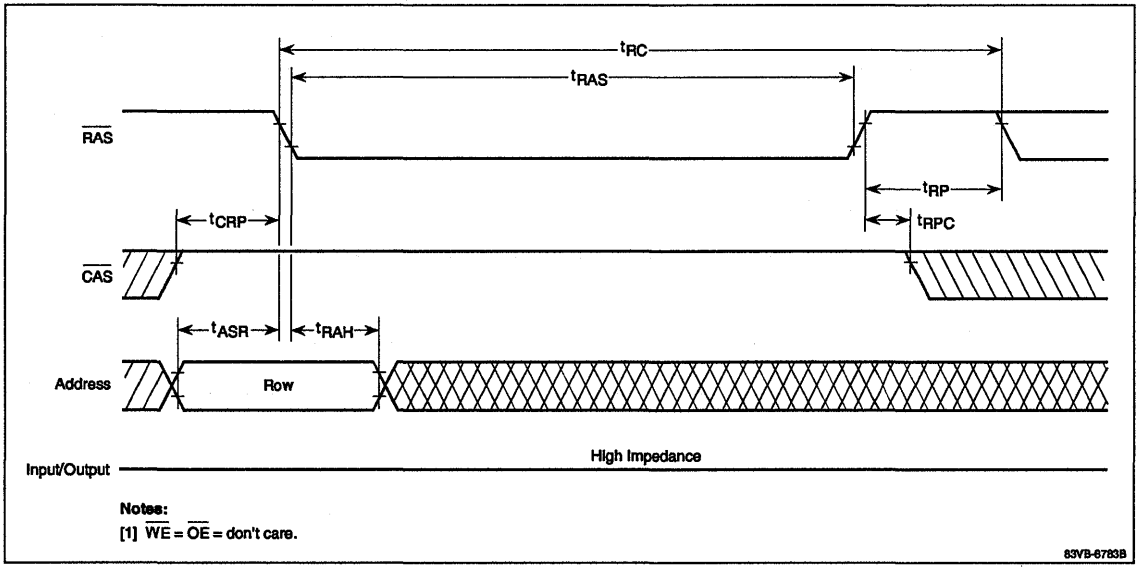
Timing Waveforms (cont)

Hidden Refresh Cycle

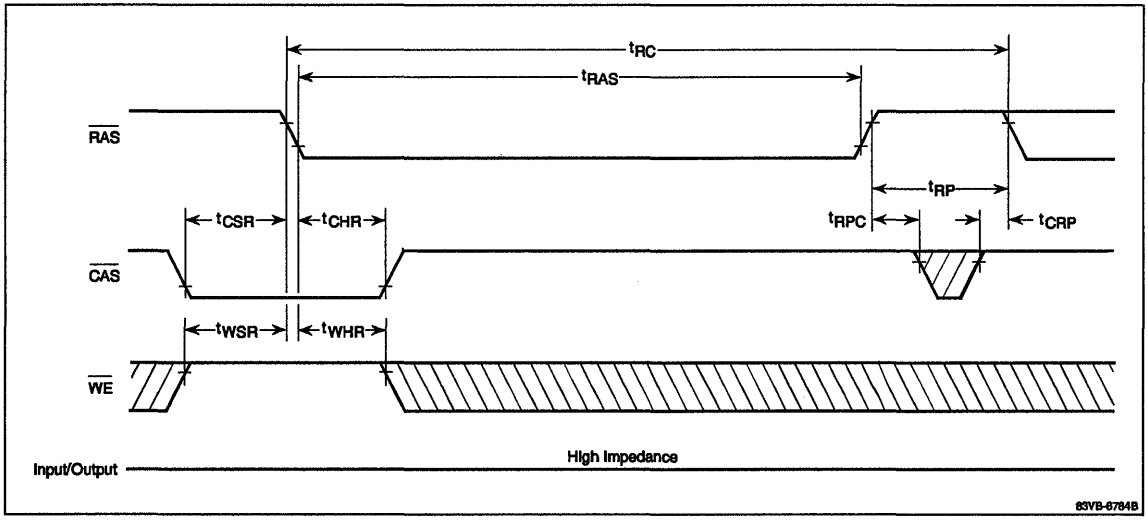


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



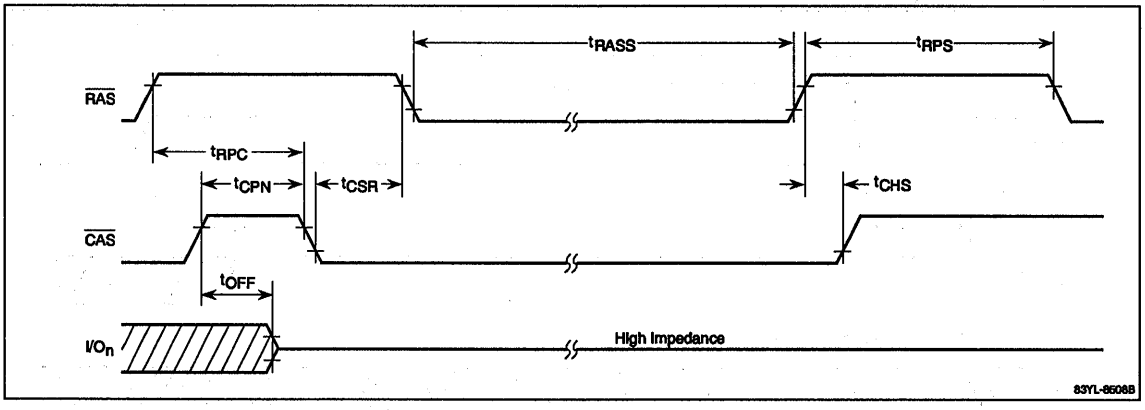
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



8h

Timing Waveforms (cont)

CBR Self-Refresh Cycle



NEC Electronics Inc.

μPD4216802
2,097,152 x 8-Bit
Dynamic CMOS RAM

Advance Information

Description

The devices listed below are static-column dynamic RAMs organized as 2M words by 8 bits and designed to operate from a single power supply. Optional features are power supply voltage (+5 V or +3.3 V), a new refresh mode called "self-refresh," and the number of cycles in a refresh period.

μPD	Power	Self-Refresh	Refresh Cycles
4216802	+5 V	—	4096 in 64 ms
802L	+3.3 V	—	
42S16802	+5 V	√	4096 in 256 ms
802L	+3.3 V	√	
4217802	+5 V	—	2048 in 32 ms
802L	+3.3 V	—	
42S17802	+5 V	√	2048 in 256 ms
802L	+3.3 V	√	

Note: Letters L and S denote 3.3-volt and self-refresh devices, respectively.

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation while an on-chip circuit internally generates the negative voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. Data outputs return to high impedance when $\overline{CS}$ goes high. Static-column read and write cycles can be executed by cycling $\overline{CS}$.

Refreshing may be accomplished by a $\overline{CS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh addresses.

For the 4216/42S16, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 4096 address combinations of A_0 - A_{11} will refresh all memory locations. Bits A_0 - A_{11} are used for row and refresh addresses, A_0 - A_8 for column addresses.

For the 4217/42S17, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 2048 address combinations of A_0 - A_{10} will refresh all memory locations. Bits A_0 - A_{10} are used for row and refresh addresses, A_0 - A_9 for column addresses.

The self-refresh mode is entered by holding $\overline{RAS}$ and $\overline{CS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 μA (+5 V) or 80 μA (+3.3 V). Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Battery backup current I_{CC6} is defined as the current consumption when the device is in standby mode ($\overline{RAS} \geq V_{CC} - 0.2$ V) and very-slow (extended) CBR cycles are being performed.

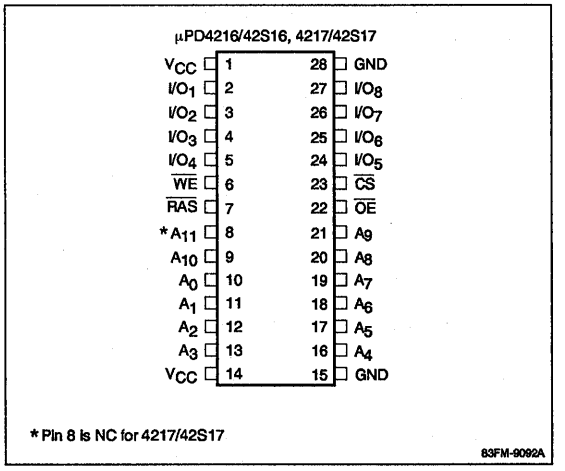
Features

- 2,097,152 by 8-bit organization
- Single power supply: +5-volt or +3.3-volt
- Static-column option
- Low-power operation
- $\overline{CS}$ before $\overline{RAS}$ refreshing
- Self-refresh option (slow internal automatic refresh)
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 28-pin, 400-mil SOJ and TSOP plastic packages

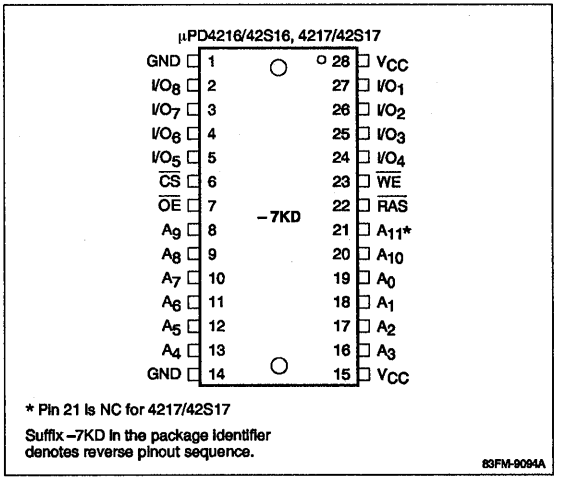
Contact your NEC sales representative for a complete data sheet.

Pin Configurations

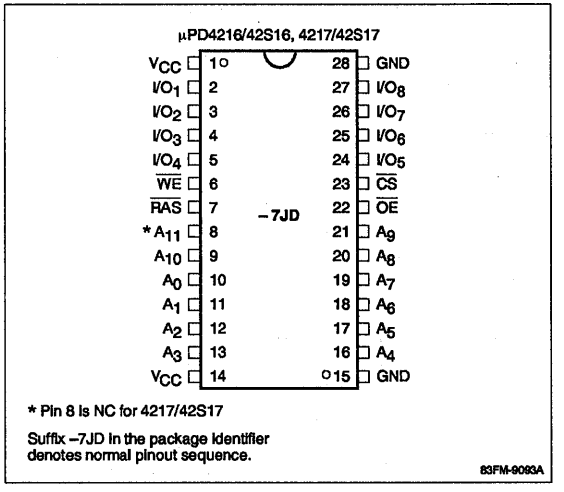
28-Pin Plastic SOJ



28-Pin Plastic TSOP (Reverse Pinouts)



28-Pin Plastic TSOP (Normal Pinouts)



Pin Identification

Name	Function
A_0 - A_{11}	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

NEC Electronics Inc.

μPD421x900/L, 42S1x900/L (x = 6, 7) 2,097,152 x 9-Bit Dynamic CMOS RAM

Description

The devices listed below are fast-page dynamic RAMs organized as 2M words by 9 bits and designed to operate from a single power supply. Optional features are power supply voltage (+5 V or +3.3 V), a new refresh mode called "self-refresh," and the number of cycles in a refresh period.

μPD	Power	Self-Refresh	Refresh Cycles
4216900	+5 V	—	4096 in 64 ms
900L	+3.3 V	—	
42S16900	+5 V	√	4096 in 256 ms
900L	+3.3 V	√	
4217900	+5 V	—	2048 in 32 ms
900L	+3.3 V	—	
42S17900	+5 V	√	2048 in 256 ms
900L	+3.3 V	√	

Note: Letters L and S denote 3.3-volt and self-refresh devices, respectively.

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation while an on-chip circuit internally generates the negative voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh addresses.

For the 4216/42S16, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 4096 address combinations of A_0 - A_{11} will refresh all memory locations. Bits A_0 - A_{11} are used for row and refresh addresses, A_0 - A_8 for column addresses.

For the 4217/42S17, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 2048 address combinations of A_0 - A_{10} will refresh all memory locations. Bits A_0 - A_{10} are used for row and refresh addresses, A_0 - A_9 for column addresses.

The self-refresh mode is entered by holding $\overline{RAS}$ and $\overline{CAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 μA (+5 V) or 80 μA (+3.3 V). Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

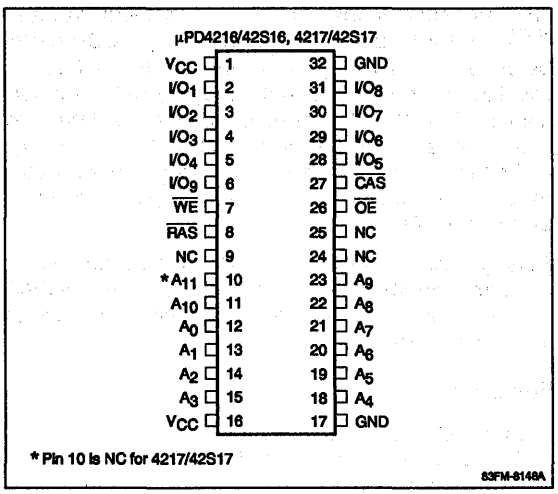
Battery backup current I_{CC6} is defined as the current consumption when the device is in standby mode ($\overline{RAS} \geq V_{CC} - 0.2$ V) and very-slow (extended) CBR cycles are being performed.

Features

- 2,097,152 by 9-bit organization
- Single power supply: +5-volt or +3.3 volt
- Fast-page option
- Low-power operation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Self-refresh option (slow internal automatic refresh)
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 32-pin, 400-mil SOJ and TSOP plastic packages

Pin Configurations

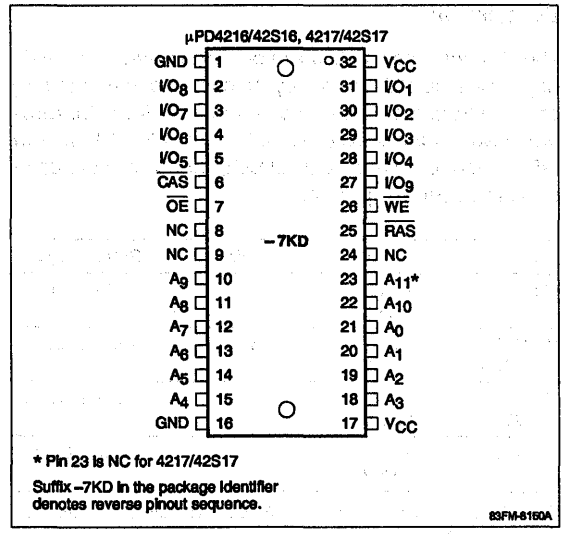
32-Pin Plastic SOJ



* Pin 10 is NC for 4217/42S17

83FM-8148A

32-Pin Plastic TSOP (Reverse Pinouts)

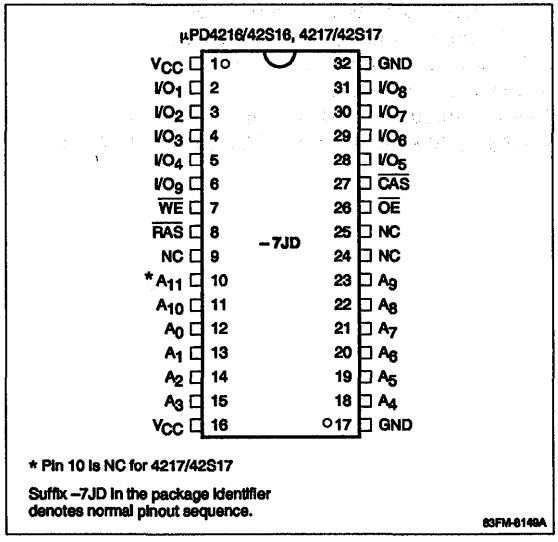


* Pin 23 is NC for 4217/42S17

Suffix –7KD in the package identifier denotes reverse pinout sequence.

83FM-8150A

32-Pin Plastic TSOP (Normal Pinouts)



* Pin 10 is NC for 4217/42S17

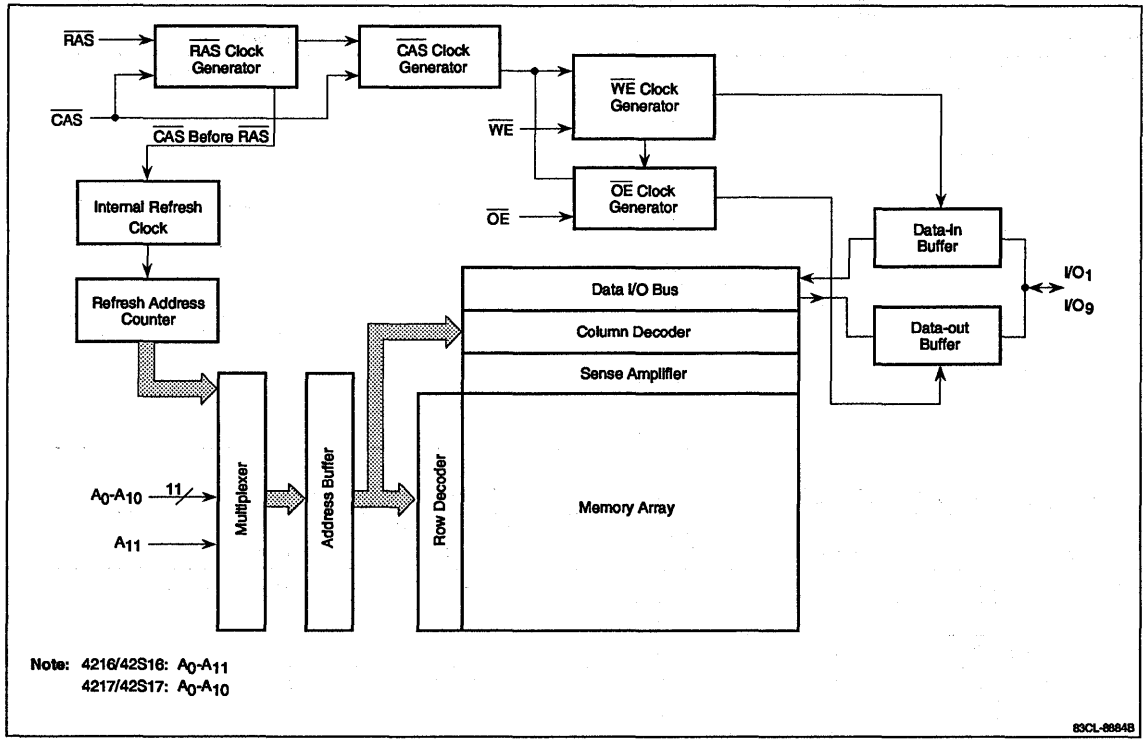
Suffix –7JD in the package identifier denotes normal pinout sequence.

83FM-8149A

Pin Identification

Name	Function
A_0 - A_{11}	Address inputs
I/O_1 - I/O_9	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

Block Diagram



Truth Table

Function	RAS	CAS	WE	OE	I/O_1 - I/O_9
Standby	H	X	X	X	High-Z
Refresh cycle	L	H	X	X	High-Z
Byte read cycle	L	L	H	L	Data output
	L	H	H	L	High-Z
Byte write cycle	L	L	L	H	Data input
	L	H	L	H	—
——	L	L	H	H	High-Z

X = don't care.

8j

Ordering Information, μPD4216900 (+ 5-volt power; 4096 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4216900LE-50	50 ns	35 ns	350 μA	32-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD4216900G5-50	50 ns	35 ns	350 μA	32-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD4216900G5M-50	50 ns	35 ns	350 μA	32-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD4216900L (+ 3.3-volt power; 4096 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4216900LLE-A60	60 ns	40 ns	140 μA	32-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD4216900LG5-A60	60 ns	40 ns	140 μA	32-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD4216900LG5M-A60	60 ns	40 ns	140 μA	32-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD42S16900 (+ 5-volt power; 4096 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S16900LE-50	50 ns	35 ns	350 μA	32-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD42S16900G5-50	50 ns	35 ns	350 μA	32-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD42S16900G5M-50	50 ns	35 ns	350 μA	32-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD42S16900L (+ 3.3-volt power; 4096 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S16900LLE-A60	60 ns	40 ns	140 μA	32-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD42S16900LG5-A60	60 ns	40 ns	140 μA	32-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD42S16900LG5M-A60	60 ns	40 ns	140 μA	32-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD4217900 (+ 5-volt power; 2048 refresh cycles)

Part Number	RAS Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4217900LE-50	50 ns	35 ns	300 μA	32-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD4217900G5-50	50 ns	35 ns	300 μA	32-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD4217900G5M-50	50 ns	35 ns	300 μA	32-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD4217900L (+ 3.3-volt power; 2048 refresh cycles)

Part Number	RAS Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4217900LLE-A60	60 ns	40 ns	120 μA	32-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD4217900LG5-A60	60 ns	40 ns	120 μA	32-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD4217900LG5M-A60	60 ns	40 ns	120 μA	32-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD42S17900 (+ 5-volt power; 2048 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S17900LE-50	50 ns	35 ns	300 μA	32-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD42S17900G5-50	50 ns	35 ns	300 μA	32-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD42S17900G5M-50	50 ns	35 ns	300 μA	32-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD42S17900L (+ 3.3-volt power; 2048 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S17900LLE-A60	60 ns	40 ns	120 μA	32-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD42S17900LG5-A60	60 ns	40 ns	120 μA	32-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD42S17900LG5M-A60	60 ns	40 ns	120 μA	32-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to + 4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_9

Recommended Operating Conditions

		5-Volt Devices			3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		70	0		70	°C

Self-Refresh Current; 42S1x Devices

T_A = 0 to +70°C; V_{CC} = +5 V ±10% or +3.3 V ±0.3 V

Symbol	5-Volt Devices	3.3-Volt Devices	Conditions
I_{CC7}	200 μA max	80 μA max	I/O pins: $V_{IH} \geq V_{CC}$ −0.2 V; $V_{IL} \leq$ 0.2 V or open. Other input pins: $V_{IH} \geq V_{CC}$ −0.2 V; $V_{IL} \leq$ 0.2 V or open; $t_{RAS} \geq$ 100 μs

DC Characteristics; 5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				400	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

DC Characteristics; 3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				400	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

DC Current Requirements; 5-Volt Devices

Parameter	Symbol	-50	-60	-70	-80	Unit	Test Conditions
Operating current	I_{CC1}						
4216/42S16		110	100	90	80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} (min); I_O = 0 mA
4217/42S17		130	120	110	100	mA	
Refresh current ($\overline{RAS}$ only refresh)	I_{CC3}						
4216/42S16		110	100	90	80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} (min); t_{RC} = t_{RC} (min); I_O = 0 mA
4217/42S17		130	120	110	100	mA	
Operating current (Fast-page mode)	I_{CC4}						
4216/42S16		80	70	60	50	mA	$\overline{CAS}$ cycling; $\overline{RAS}$ ≤ V_{IL} (max); t_{PC} = t_{PC} (min); I_O = 0 mA
4217/42S17		80	70	60	50	mA	
Refresh current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}						
4216/42S16		110	100	90	80	mA	$\overline{RAS}$ cycling; t_{RC} = t_{RC} (min); I_O = 0 mA
4217/42S17		130	120	110	100	mA	
Battery backup current (Standby with $\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RAS} ≤ 300 ns		t_{RAS} ≤ 1 μs			Standby: $\overline{RAS}$ ≥ V_{CC} – 0.2 V; $\overline{RAS}$, $\overline{CAS}$: 0 V ≤ V_{IL} ≤ 0.2 V, V_{CC} – 0.2 V ≤ V_{IH} ≤ V_{IH} (max); $\overline{WE}$, $\overline{OE}$: V_{IH}; Address: don't care; Output: open
42S16		350		500		μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 4096 cycles, 256 ms
42S17		300		400		μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 2048 cycles, 256 ms

8j

DC Current Requirements; 3.3-Volt Devices

Parameter	Symbol	-A60	-A70	-A80	Unit	Test Conditions
Operating current	I_{CC1}					
4216/42S16		90	80	70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ (min); I_O = 0 mA
4217/42S17		110	100	90	mA	
Refresh current ($\overline{RAS}$ only refresh)	I_{CC3}					
4216/42S16		90	80	70	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$ (min); $t_{RC} = t_{RC}$ (min); I_O = 0 mA
4217/42S17		110	100	90	mA	
Operating current (Fast-page mode)	I_{CC4}					
4216/42S16		60	50	40	mA	$\overline{CAS}$ cycling; $\overline{RAS} \leq V_{IL}$ (max); $t_{PC} = t_{PC}$ (min); I_O = 0 mA
4217/42S17		60	50	40	mA	
Refresh current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}					
4216/42S16		90	80	70	mA	$\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ (min); I_O = 0 mA
4217/42S17		110	100	90	mA	
Battery backup current (Standby with $\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$t_{RAS} \leq 300$ ns		$t_{RAS} \leq 1$ μs		Standby: $\overline{RAS} \geq V_{CC} - 0.2$ V; $\overline{RAS}$, $\overline{CAS}$: 0 V ≤ V_{IL} ≤ 0.2 V, $V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH}$ (max); $\overline{WE}$, $\overline{OE}$: V_{IH}; Address: don't care; Output: open
42S16		140		140	μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 4096 cycles, 256 ms
42S17		120		120	μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 2048 cycles, 256 ms

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10% (-50, -60, -70, -80) or +3.3 V ±0.3 V (-A60, -A70, -A80)

		-50		-60, -A60		-70, -A70		-80, -A80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Access time from column address	t_{AA}		25		30		35		40	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		30		35		40		45	ns	(Note 7)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	45		53		60		65		ns	(Note 15)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		13		15		18		20	ns	(Notes 7, 8)
Column address hold time	t_{CAH}	13		15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	10		10		10		10		ns	
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	−50		−50		−50		−50		ns	(Note 16)
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		0		ns	(Note 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	8		10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	8		10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		65		70		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		5		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	33		38		43		45		ns	(Note 15)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	13		15		15		15		ns	
Data-in hold time	t_{DH}	10		10		15		15		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		13		15		18		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	10		13		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	0	15	ns	(Note 9)

AC Characteristics (cont)

		-50		-60, -A60		-70, -A70		-80, -A80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Output disable from $\overline{CAS}$ high	t_{OFF}	0	10	0	13	0	15	0	15	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		0		ns	(Note 7)
Fast-page read or write cycle time	t_{PC}	35		40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with extended data output	t_{PRWC}	80		85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	15	35	17	40	ns	(Note 8)
Row address hold time	t_{RAH}	8		10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	25		30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		100		μs	(Note 16)
Random read or write cycle time	t_{RC}	90		110		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	20	45	20	50	25	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}										
4216			64		64		64		64	ms	
4217			32		32		32		32	ms	
42S16			256		256		256		256	ms	
42S17			256		256		256		256	ms	
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5		5		5		5		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	90		110		130		150		ns	(Note 16)
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	13		15		18		20		ns	
Read-modify-write cycle time	t_{RWC}	140		160		180		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	70		83		95		105		ns	(Note 15)

AC Characteristics (cont)

Parameter	Symbol	-50 Min	-50 Max	-60, -A60 Min	-60, -A60 Max	-70, -A70 Min	-70, -A70 Max	-80, -A80 Min	-80, -A80 Max	Unit	Test Conditions
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	18		20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	
Write command hold time	t_{WCH}	8		10		10		15		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 14)
Write command pulse width	t_{WP}	8		10		10		15		ns	(Note 12)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by eight refresh cycles ($\overline{RAS}$ only or CBR) before proper device operation is achieved.

(3) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(4) Ac measurements assume t_T = 5 ns.

(5) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max).
If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a late write cycle. For early write cycles, t_{WCH} must be met.

(13) These parameters are referenced to the leading edge of $\overline{CAS}$ in early write cycles and to the leading edge of $\overline{WE}$ in late write or read-modify-write cycles.

(14) If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle.

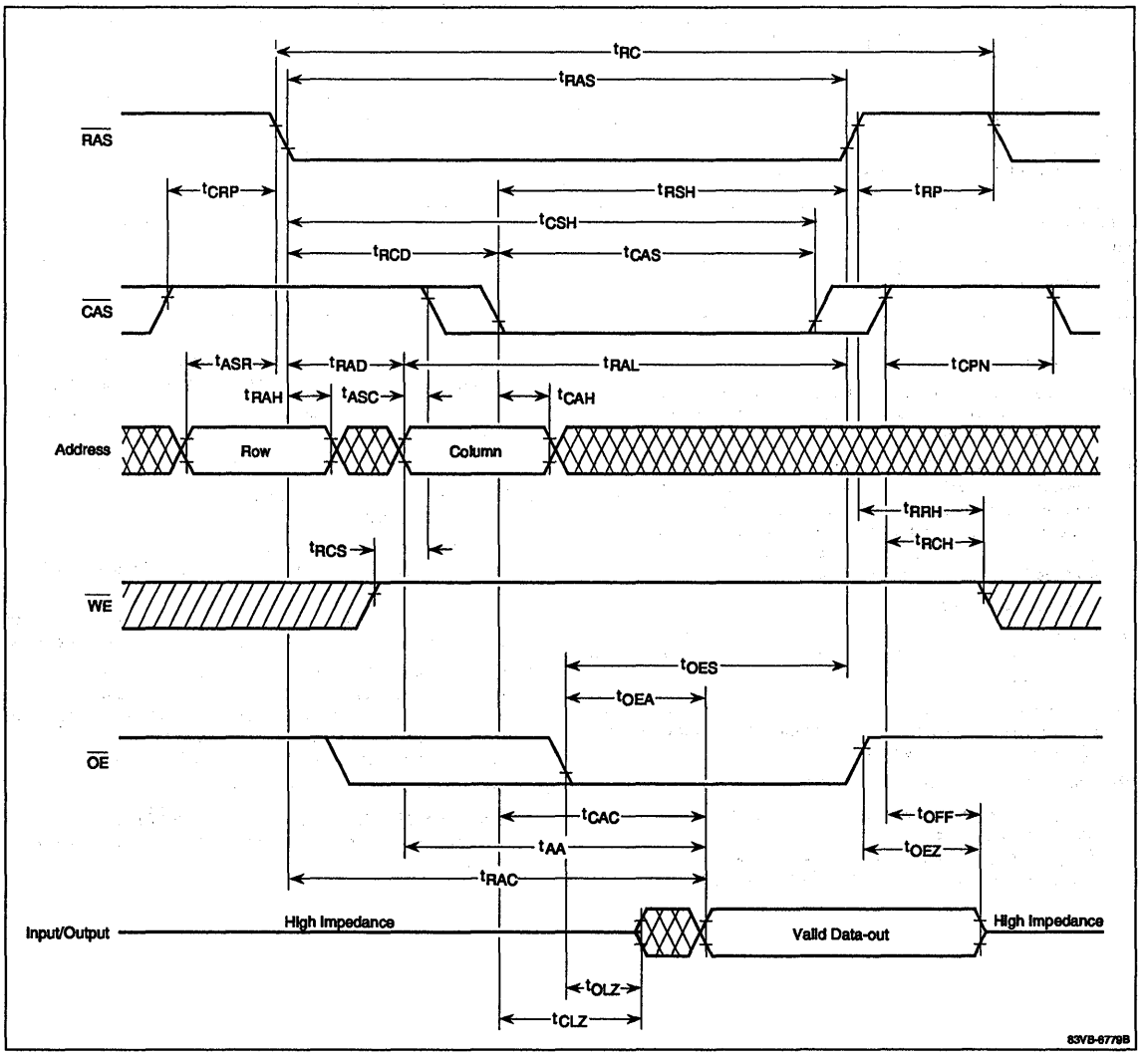
(15) If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(16) Parameter is applicable only to self-refresh versions.

(17) With burst CBR, $\overline{RAS}$ only, or external $\overline{RAS}/\overline{CAS}$, all addresses must be refreshed before entering self-refresh mode and after exiting.

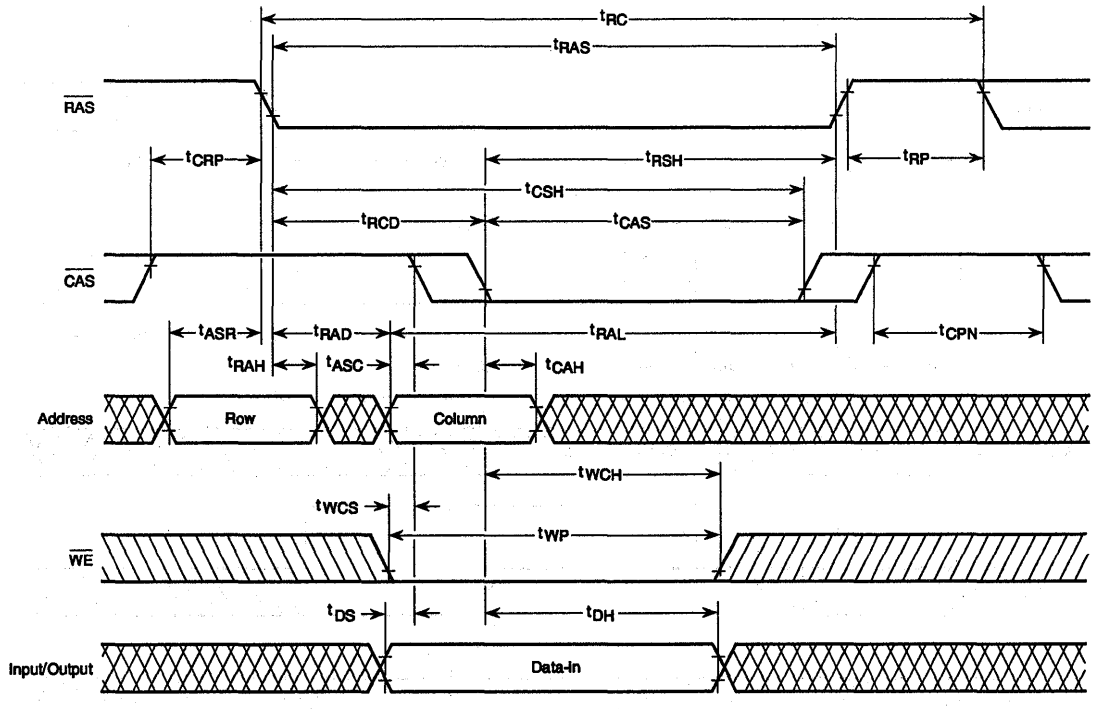
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early-Write Cycle

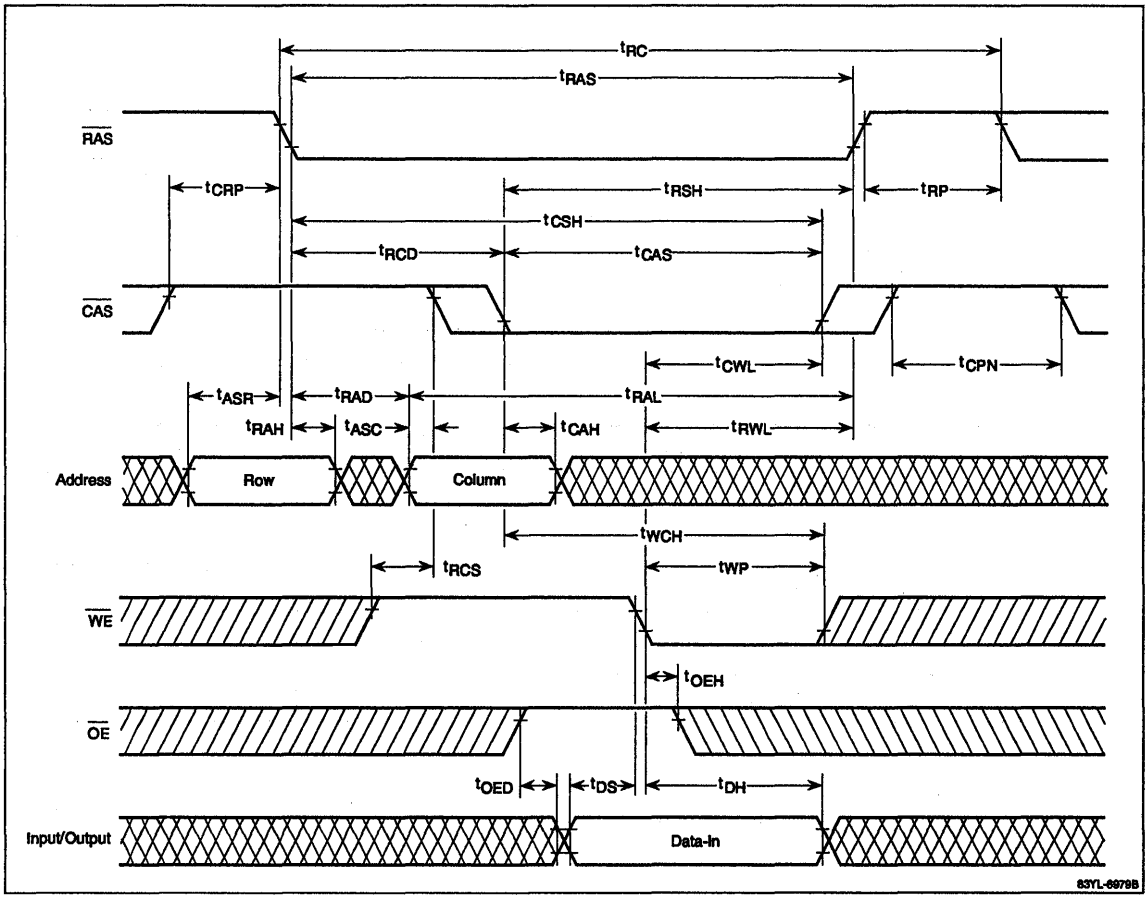


Note:
[1] $\overline{OE}$ = don't care.

83YL-6978B

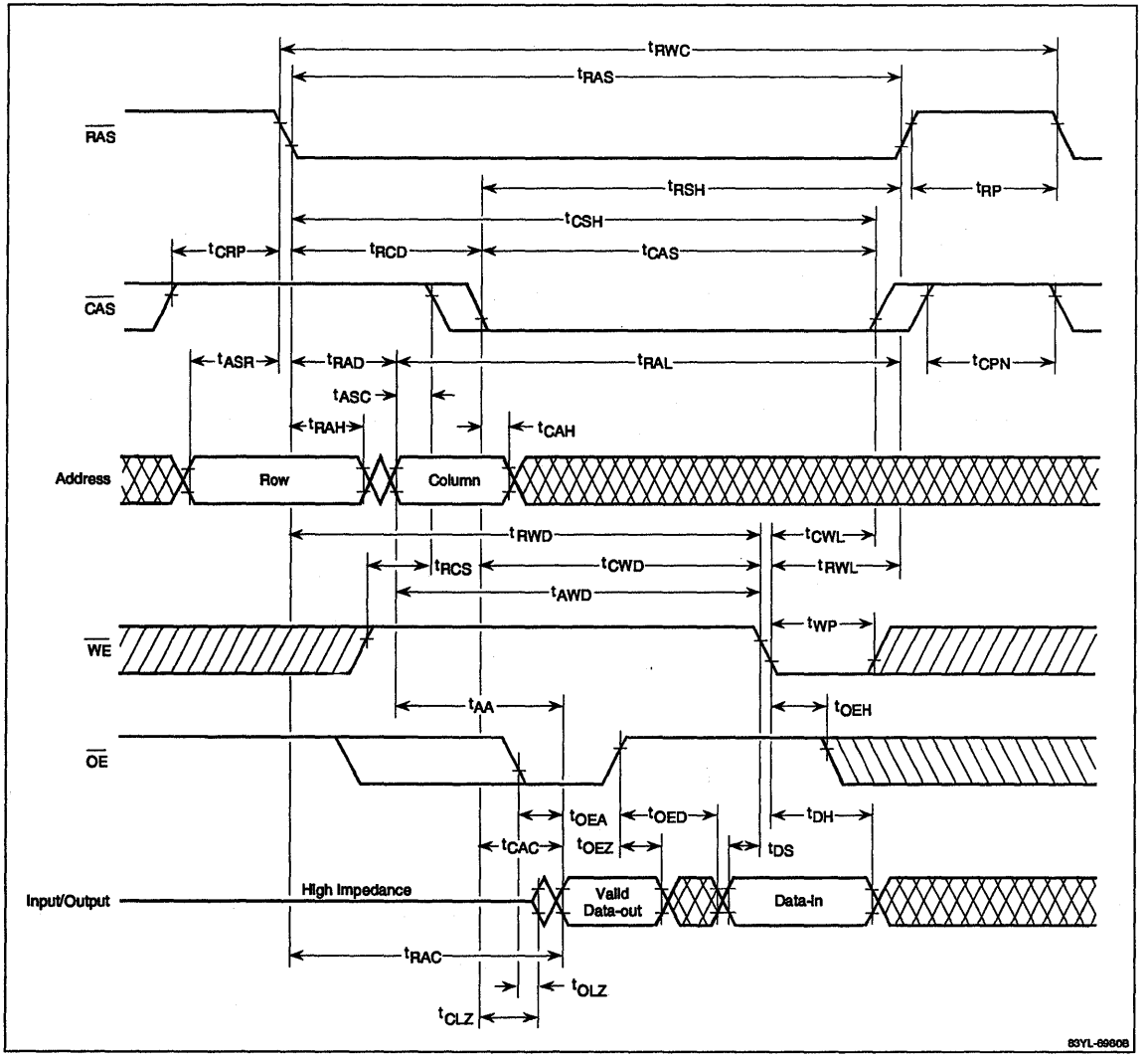
Timing Waveforms (cont)

Late-Write Cycle



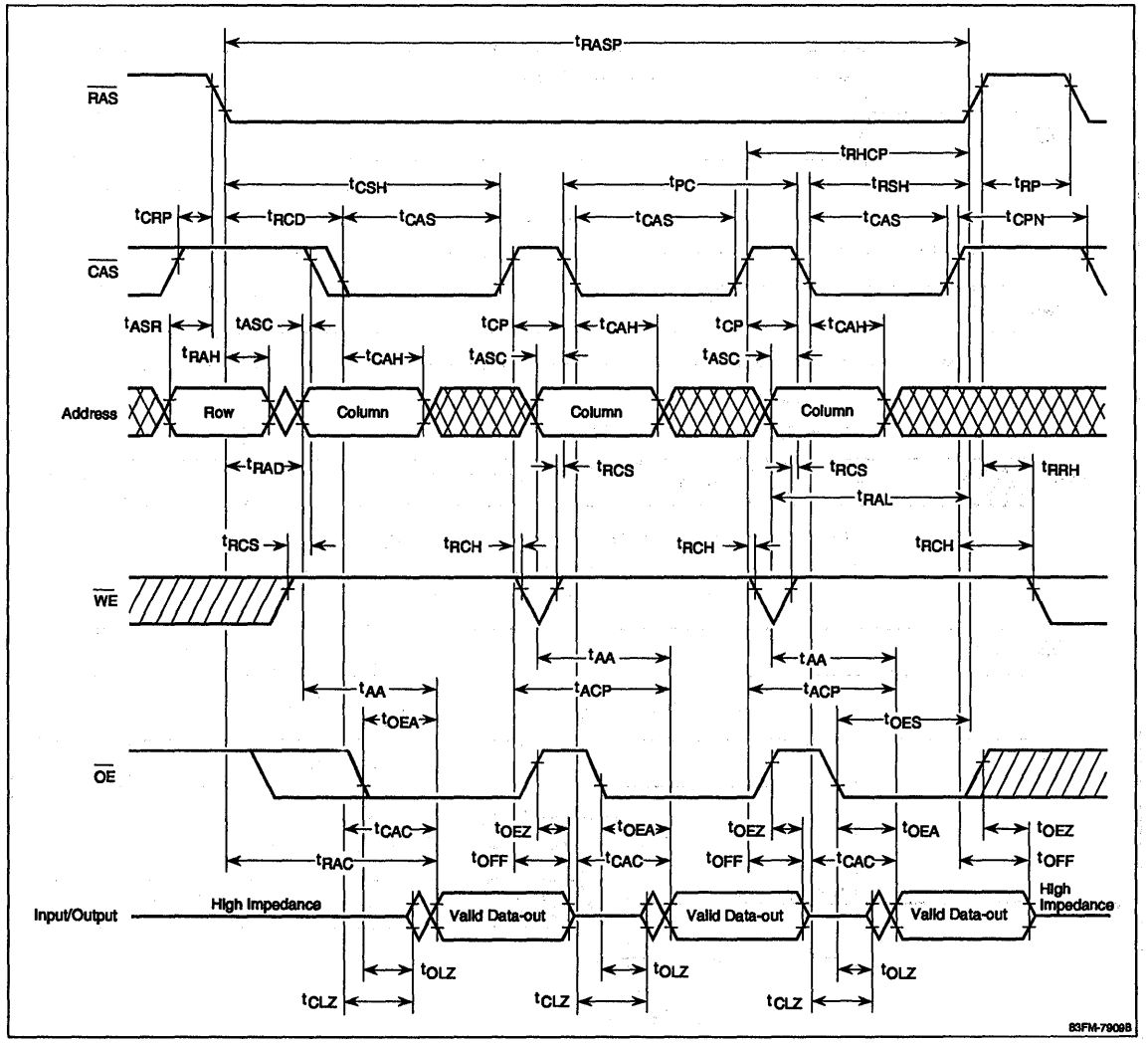
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



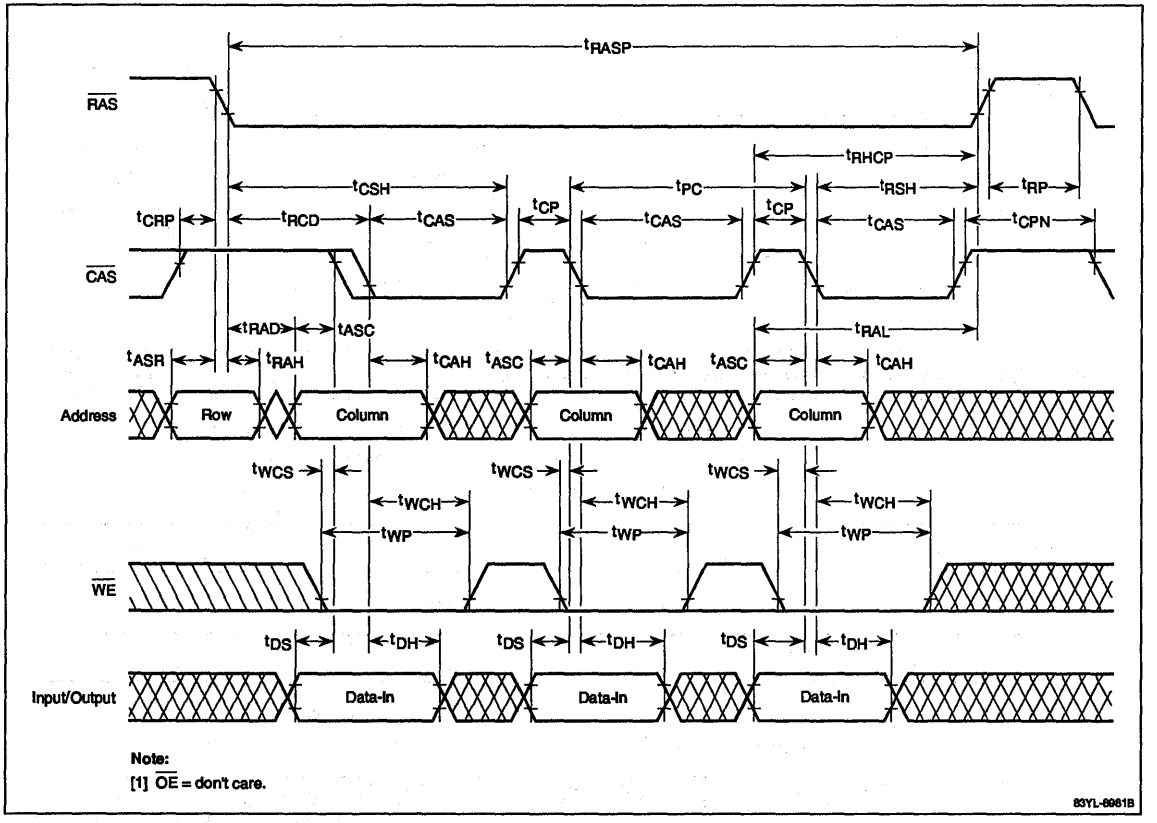
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early-Write Cycle

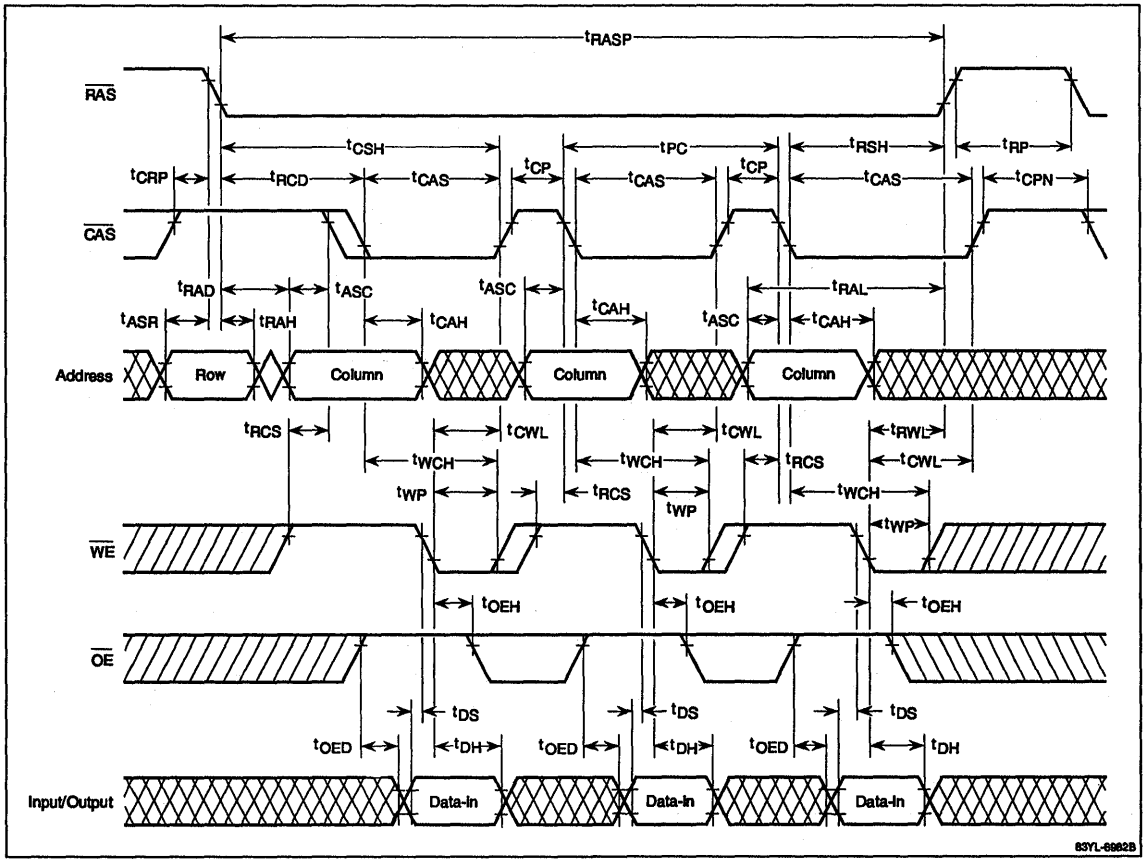


Note:
[1] $\overline{OE}$ = don't care.

83YL-8981B

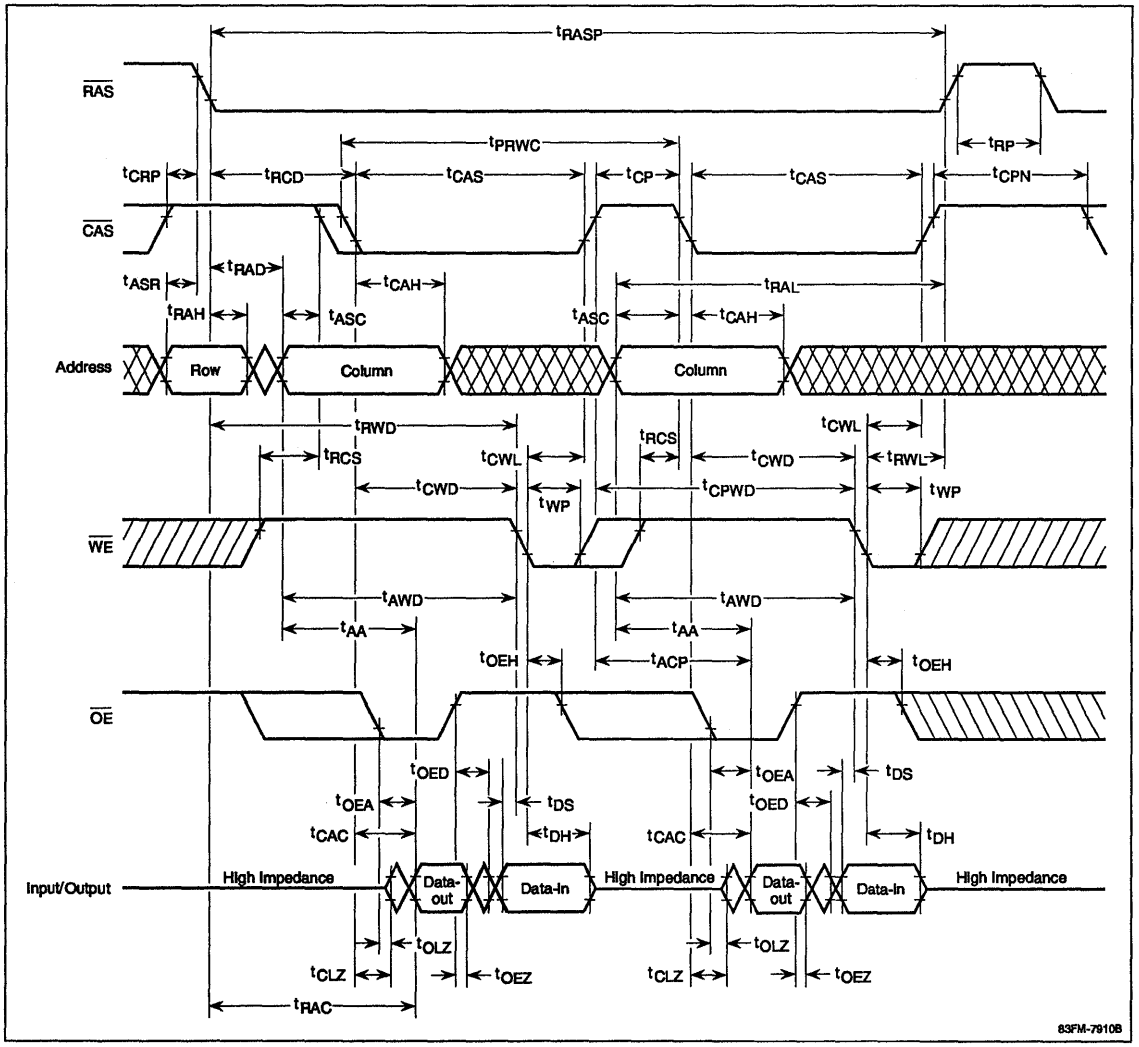
Timing Waveforms (cont)

Fast-Page Late-Write Cycle



Timing Waveforms (cont)

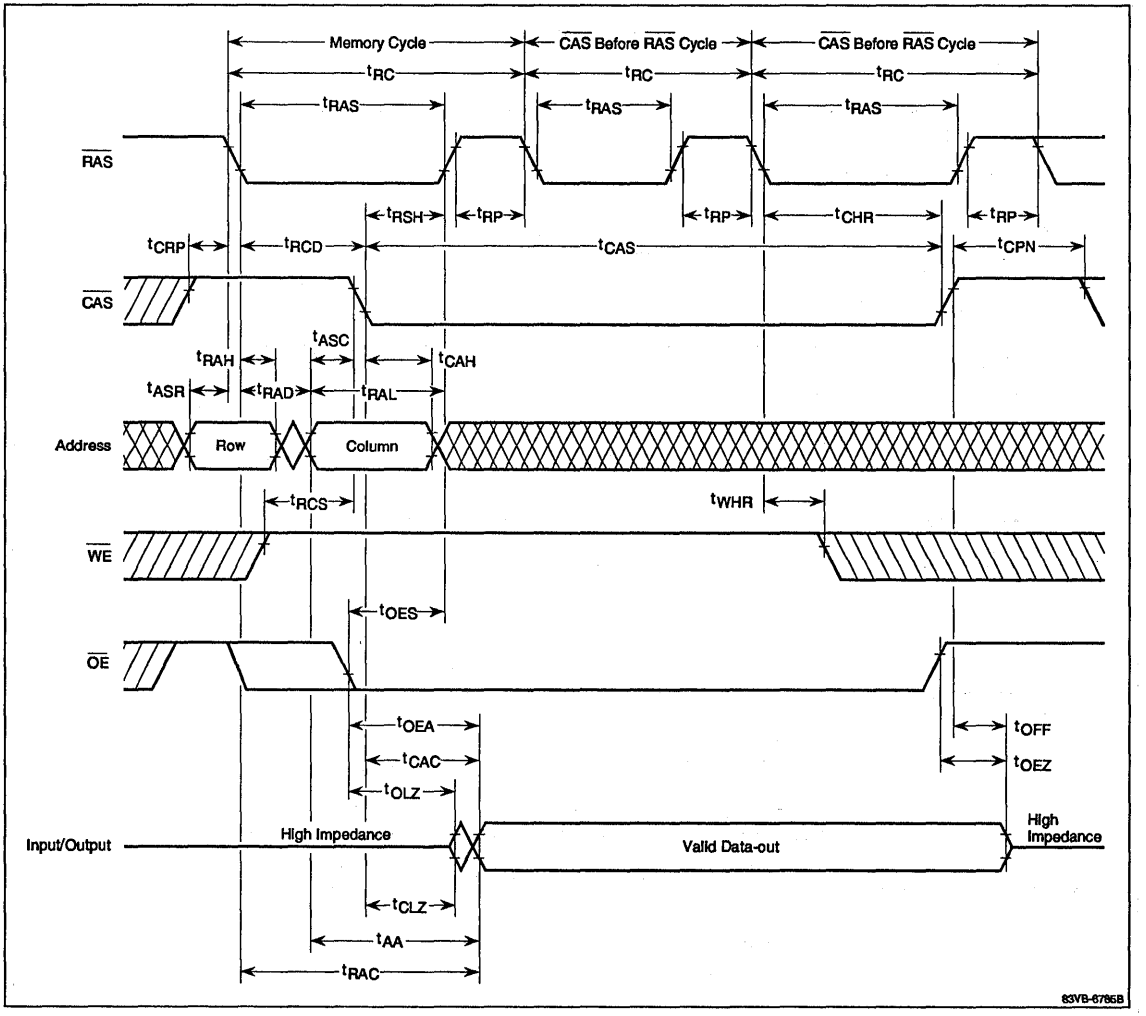
Fast-Page Read-Write/Read-Modify-Write Cycle



8j

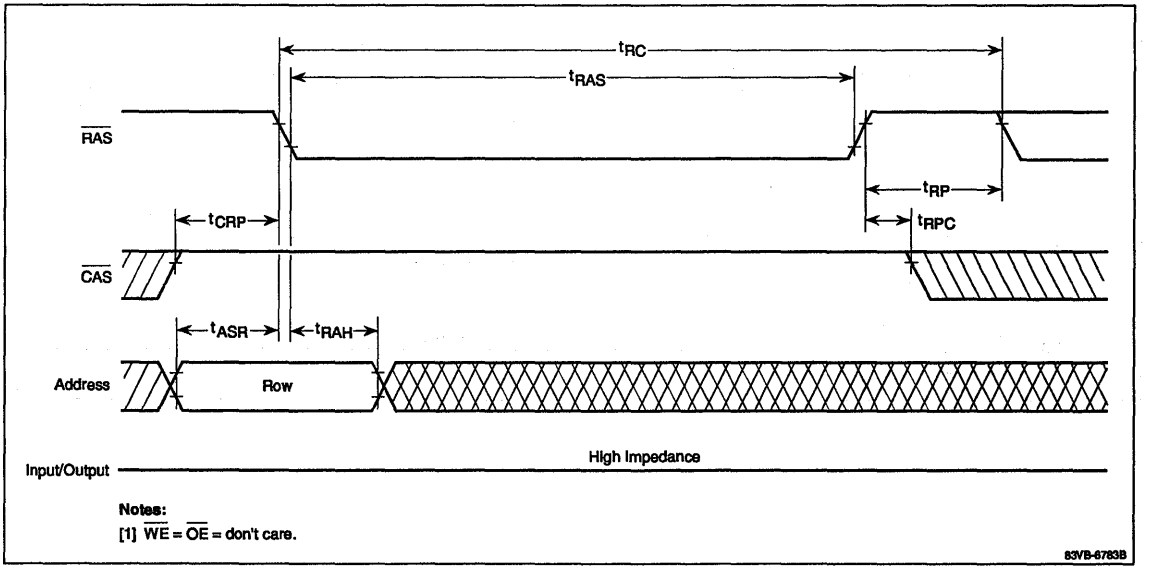
Timing Waveforms (cont)

Hidden Refresh Cycle

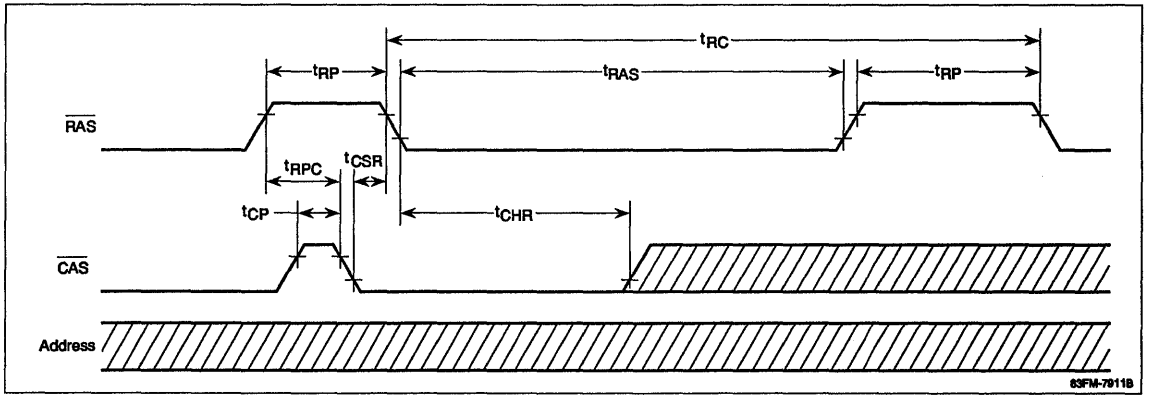


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



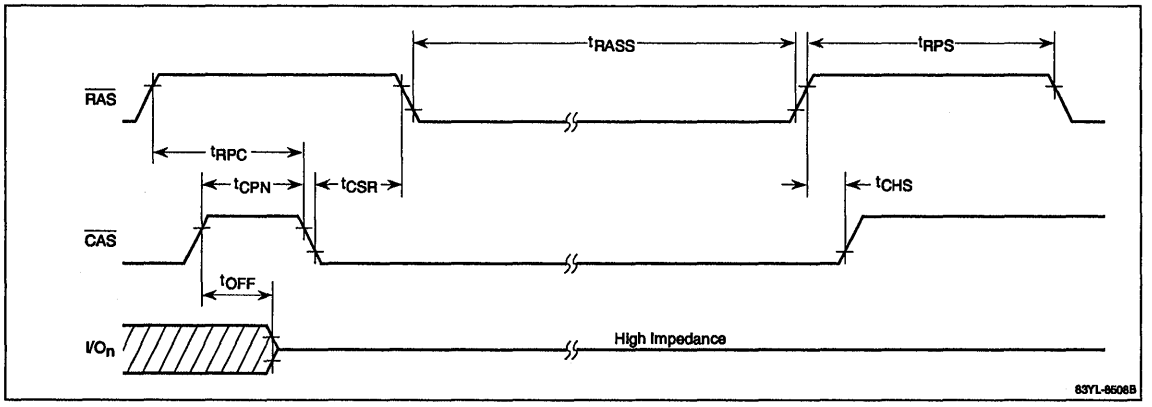
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



8j

Timing Waveforms (cont)

CBR Self-Refresh Cycle



NEC Electronics Inc.

μPD4216902
2,097,152 x 9-Bit
Dynamic CMOS RAM

Advance Information

Description

The devices listed below are static-column dynamic RAMs organized as 2M words by 9 bits and designed to operate from a single power supply. Optional features are power supply voltage (+5 V or +3.3 V), a new refresh mode called "self-refresh," and the number of cycles in a refresh period.

μPD	Power	Self-Refresh	Refresh Cycles
4216902	+5 V	—	4096 in 64 ms
902L	+3.3 V	—	
42S16902	+5 V	√	4096 in 256 ms
902L	+3.3 V	√	
4217902	+5 V	—	2048 in 32 ms
902L	+3.3 V	—	
42S17902	+5 V	√	2048 in 256 ms
902L	+3.3 V	√	

Note: Letters L and S denote 3.3-volt and self-refresh devices, respectively.

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation while an on-chip circuit internally generates the negative voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. Data outputs return to high impedance when $\overline{CS}$ goes high. Static-column read and write cycles can be executed by cycling $\overline{CS}$.

Refreshing may be accomplished by a $\overline{CS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh addresses.

For the 4216/42S16, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 4096 address combinations of A_0 - A_{11} will refresh all memory locations. Bits A_0 - A_{11} are used for row and refresh addresses, A_0 - A_8 for column addresses.

For the 4217/42S17, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 2048 address combinations of A_0 - A_{10} will refresh all memory locations. Bits A_0 - A_{10} are used for row and refresh addresses, A_0 - A_9 for column addresses.

The self-refresh mode is entered by holding $\overline{RAS}$ and $\overline{CS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 μA (+5 V) or 80 μA (+3.3 V). Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Battery backup current I_{CC6} is defined as the current consumption when the device is in standby mode ($\overline{RAS} \geq V_{CC} - 0.2$ V) and very-slow (extended) CBR cycles are being performed.

Features

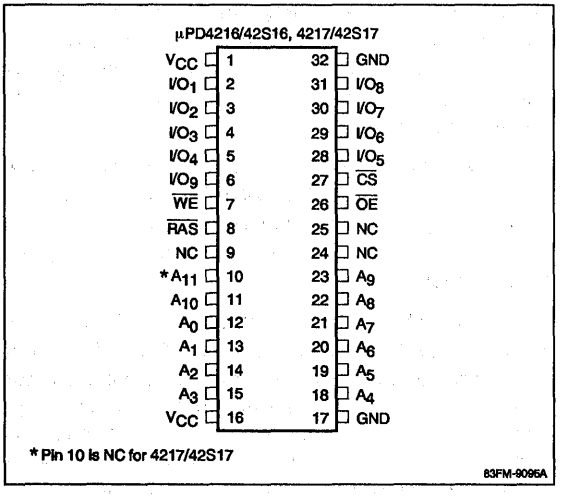
- 2,097,152 by 9-bit organization
- Single power supply: +5-volt or +3.3-volt
- Static-column option
- Low-power operation
- $\overline{CS}$ before $\overline{RAS}$ refreshing
- Self-refresh option (slow internal automatic refresh)
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 32-pin, 400-mil SOJ and TSOP plastic packages

8k

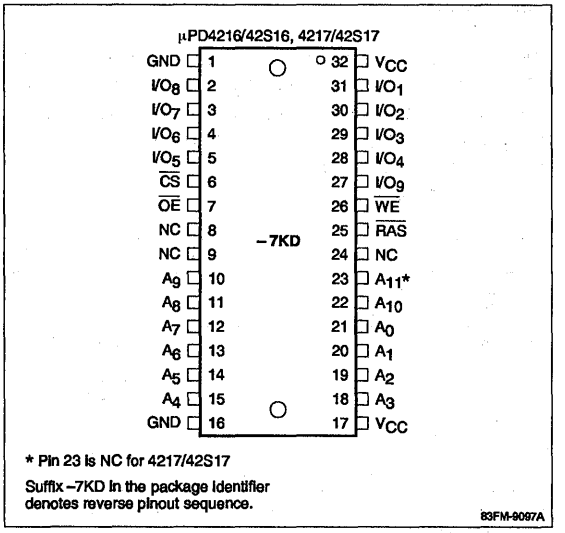
Contact your NEC sales representative for a complete data sheet.

Pin Configuration

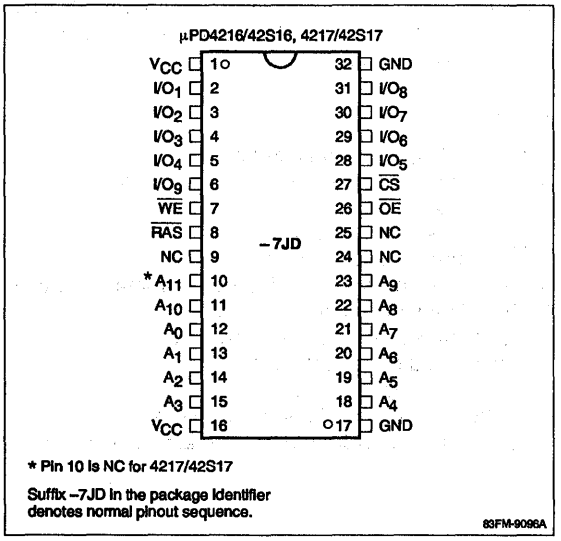
32-Pin Plastic SOJ



32-Pin Plastic TSOP (Reverse Pinouts)



32-Pin Plastic TSOP (Normal Pinouts)



Pin Identification

Name	Function
A_0 - A_{11}	Address inputs
I/O_1 - I/O_9	Data inputs and outputs
$\overline{CS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

μPD421x160/L, 42S1x160/L (x = 6, 7, 8) 1,048,576 x 16-Bit Dynamic CMOS RAM

Description

The devices listed below are fast-page dynamic RAMs organized as 1M words by 16 bits and designed to operate from a single power supply. Optional features are power supply voltage (+5 V or +3.3 V), a new refresh mode called "self-refresh," and the number of cycles in a refresh period.

μPD	Power	Self-Refresh	Refresh Cycles
4216160	+5 V	—	4096 in 64 ms
160L	+3.3 V	—	
42S16160	+5 V	√	4096 in 256 ms
160L	+3.3 V	√	
4217160	+5 V	—	2048 in 32 ms
160L	+3.3 V	—	
42S17160	+5 V	√	2048 in 256 ms
160L	+3.3 V	√	
4218160	+5 V	—	1024 in 16 ms
160L	+3.3 V	—	
42S18160	+5 V	√	1024 in 256 ms
160L	+3.3 V	√	

Note: Letters L and S denote 3.3-volt and self-refresh devices, respectively.

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation while an on-chip circuit internally generates the negative voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{UCAS}$ and $\overline{LCAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, upper or lower byte data is held on the outputs by maintaining $\overline{UCAS}$ or $\overline{LCAS}$ low. Data outputs return to high impedance when $\overline{UCAS}$ or $\overline{LCAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{UCAS}$ or $\overline{LCAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh addresses.

For the 4216/42S16, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 4096 address combinations of A_0 - A_{11} will refresh all memory locations. Bits A_0 - A_{11} are used for row and refresh addresses, A_0 - A_7 for column addresses.

For the 4217/42S17, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 2048 address combinations of A_0 - A_{10} will refresh all memory locations. Bits A_0 - A_{10} are used for row and refresh addresses, A_0 - A_8 for column addresses.

For the 4218/42S18, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 1024 address combinations of A_0 - A_9 will refresh all memory locations. Bits A_0 - A_9 are used for row, refresh, and column addresses.

The self-refresh mode is entered by holding $\overline{RAS}$ and $\overline{CAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 μA (+5 V) or 80 μA (+3.3 V). Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

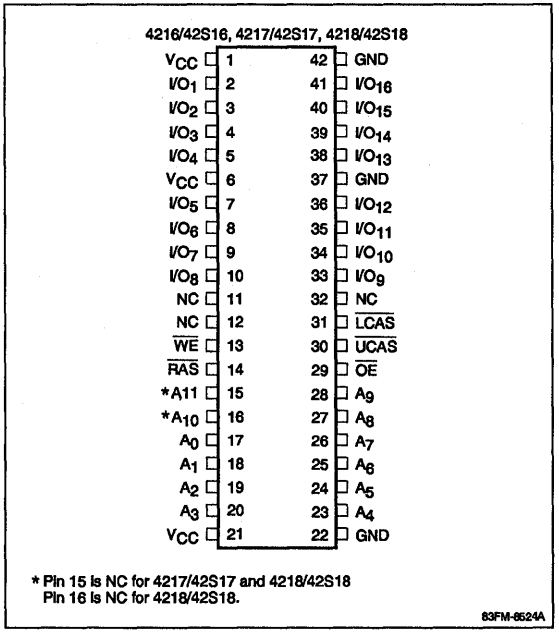
Battery backup current I_{CC6} is defined as the current consumption when the device is in standby mode ($\overline{RAS} \geq V_{CC} - 0.2$ V) and very-slow (extended) CBR cycles are being performed.

Features

- 1,048,576 by 16-bit organization
- Single power supply: +5-volt or +3.3-volt
- Fast-page option
- Low-power operation
- Byte read/write control with $\overline{UCAS}$ and $\overline{LCAS}$
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Self-refresh option (slow internal automatic refresh)
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 42-pin SOJ and 50/44-pin TSOP plastic packages

Pin Configurations

42-Pin Plastic SOJ



* Pin 15 is NC for 4217/42S17 and 4218/42S18
Pin 16 is NC for 4218/42S18.

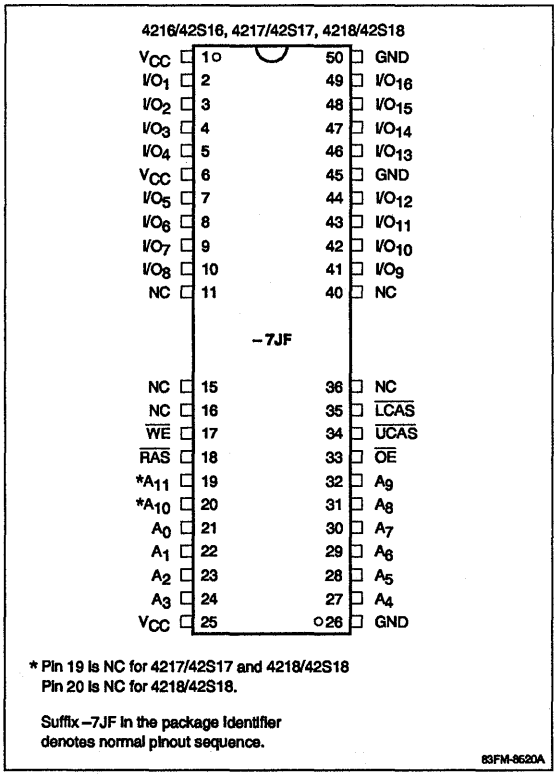
83FM-8524A

Pin Identification

Name	Function
A_0 - A_{11}	Address inputs
I/O_1 - I/O_{16}	Data inputs and outputs
$\overline{LCAS}$, $\overline{UCAS}$	Column address strobes
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

Pin Configurations (cont)

50/44-Pin Plastic TSOP (Normal Pinouts)

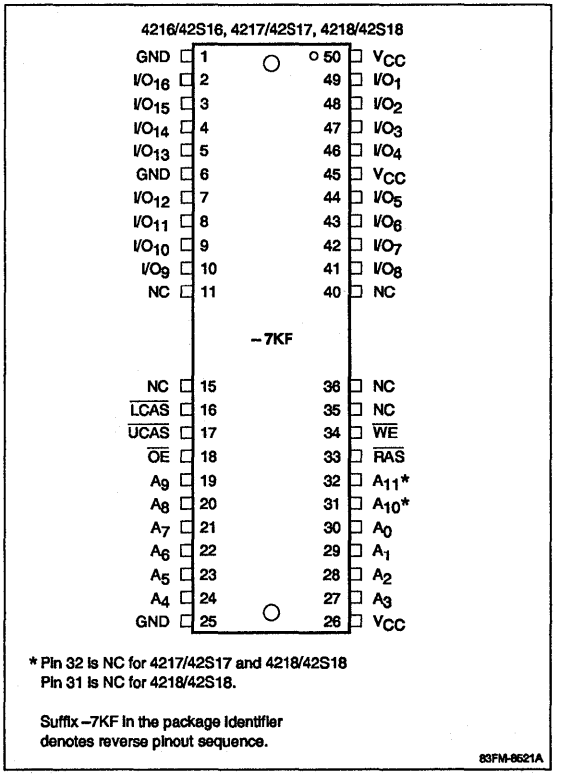


* Pin 19 is NC for 4217/42S17 and 4218/42S18
Pin 20 is NC for 4218/42S18.

Suffix -7JF in the package identifier denotes normal pinout sequence.

83FM-8520A

50/44-Pin Plastic TSOP (Reverse Pinouts)

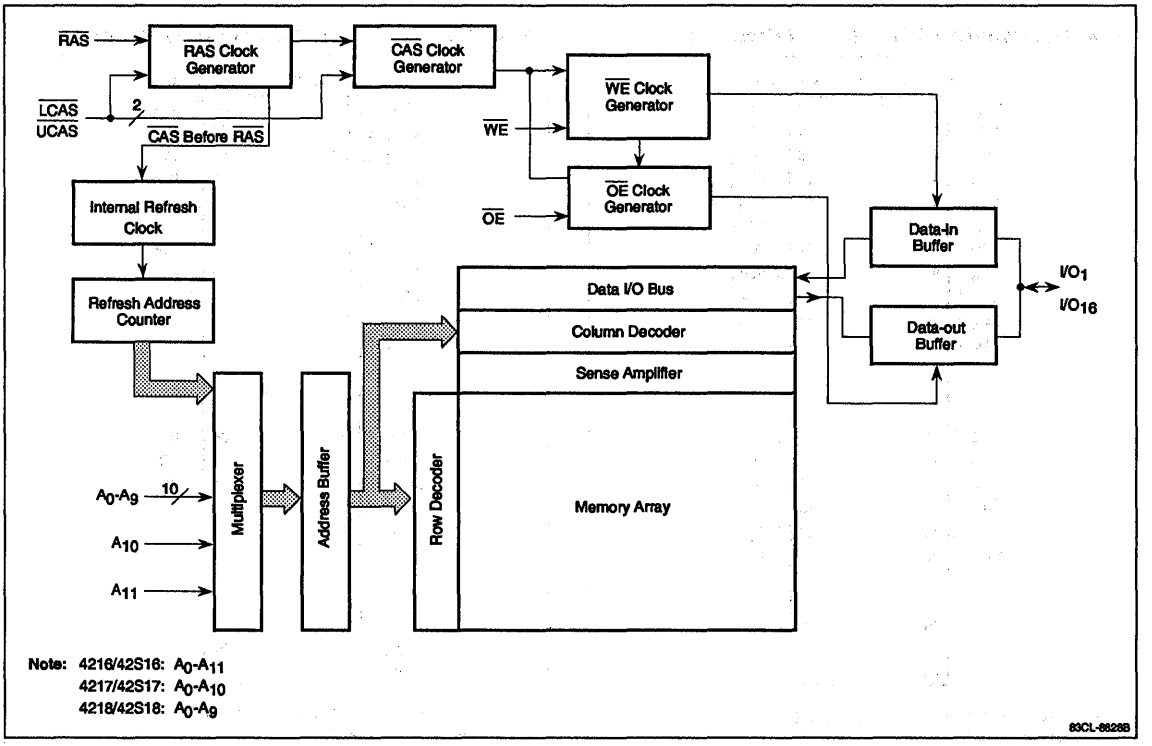


* Pin 32 is NC for 4217/42S17 and 4218/42S18
Pin 31 is NC for 4218/42S18.

Suffix -7KF in the package identifier denotes reverse pinout sequence.

83FM-8521A

Block Diagram



Truth Table

Function	RAS	LCAS	UCAS	WE	OE	I/O_1 - I/O_8	I/O_9 - I/O_{16}
Standby	H	X	X	X	X	High-Z	High-Z
Refresh cycle	L	H	H	X	X	High-Z	High-Z
Byte read cycle	L	L	H	H	L	Data output	High-Z
	L	H	L	H	L	High-Z	Data output
Word read cycle	L	L	L	H	L	Data output	Data output
Byte write cycle	L	L	H	L	H	Data input	—
	L	H	L	L	H	—	Data input
Word write cycle	L	L	L	L	H	Data input	Data input
——	L	L	L	H	H	High-Z	High-Z

X = don't care.

Ordering Information, μPD4216160 (+5-volt power; 4096 refresh cycles)

Part Number	RAS Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4216160LE-50	50 ns	35 ns	350 μA	42-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD4216160G5-50	50 ns	35 ns	350 μA	50/44-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD4216160G5M-50	50 ns	35 ns	350 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD4216160L (+3.3-volt power; 4096 refresh cycles)

Part Number	RAS Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4216160LLE-A60	60 ns	40 ns	140 μA	42-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD4216160LG5-A60	60 ns	40 ns	140 μA	50/44-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD4216160LG5M-A60	60 ns	40 ns	140 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD42S16160 (+ 5-volt power; 4096 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S16160LE-50	50 ns	35 ns	350 μA	42-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD42S16160G5-50	50 ns	35 ns	350 μA	50/44-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD42S16160G5M-50	50 ns	35 ns	350 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD42S16160L (+ 3.3-volt power; 4096 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S16160LLE-A60	60 ns	40 ns	140 μA	42-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD42S16160LG5-A60	60 ns	40 ns	140 μA	50/44-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD42S16160LG5M-A60	60 ns	40 ns	140 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD4217160 (+ 5-volt power; 2048 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4217160LE-50	50 ns	35 ns	300 μA	42-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD4217160G5-50	50 ns	35 ns	300 μA	50/44-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD4217160G5M-50	50 ns	35 ns	300 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD4217160L (+ 3.3-volt power; 2048 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4217160LLE-A60	60 ns	40 ns	120 μA	42-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD4217160LG5-A60	60 ns	40 ns	120 μA	50/44-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD4217160LG5M-A60	60 ns	40 ns	120 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD42S17160 (+5-volt power; 2048 refresh cycles; self-refresh mode)

Part Number	RAS Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S17160LE-50	50 ns	35 ns	300 μA	42-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD42S17160G5-50	50 ns	35 ns	300 μA	50/44-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD42S17160G5M-50	50 ns	35 ns	300 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD42S17160L (+3.3-volt power; 2048 refresh cycles; self-refresh mode)

Part Number	RAS Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S17160LLE-A60	60 ns	40 ns	120 μA	42-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD42S17160LG5-A60	60 ns	40 ns	120 μA	50/44-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD42S17160LG5M-A60	60 ns	40 ns	120 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD4218160 (+ 5-volt power; 1024 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4218160LE-50	50 ns	35 ns	250 μA	42-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD4218160G5-50	50 ns	35 ns	250 μA	50/44-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD4218160G5M-50	50 ns	35 ns	250 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD4218160L (+ 3.3-volt power; 1024 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4218160LLE-A60	60 ns	40 ns	110 μA	42-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD4218160LG5-A60	60 ns	40 ns	110 μA	50/44-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD4218160LG5M-A60	60 ns	40 ns	110 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD42S18160 (+ 5-volt power; 1024 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S18160LE-50	50 ns	35 ns	250 μA	42-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD42S18160G5-50	50 ns	35 ns	250 μA	50/44-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD42S18160G5M-50	50 ns	35 ns	250 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD42S18160L (+ 3.3-volt power; 1024 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S18160LLE-A60	60 ns	40 ns	110 μA	42-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD42S18160LG5-A60	60 ns	40 ns	110 μA	50/44-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD42S18160LG5M-A60	60 ns	40 ns	110 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to + 4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_{16}

Recommended Operating Conditions

		5-Volt Devices			3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		70	0		70	°C

Self-Refresh Current; 42S1x Devices

T_A = 0 to +70°C; V_{CC} = +5 V ±10% or +3.3 V ±0.3 V

Symbol	5-Volt Devices	3.3-Volt Devices	Conditions
I_{CC7}	200 μA max	80 μA max	I/O pins: $V_{IH} \geq V_{CC}$ −0.2 V; $V_{IL} \leq$ 0.2 V or open. Other input pins: $V_{IH} \geq V_{CC}$ −0.2 V; $V_{IL} \leq$ 0.2 V or open; $t_{RAS} \geq$ 100 μs

DC Characteristics; 5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS} \geq V_{IH}$ (min); I_O = 0 mA
				400	μA	$\overline{RAS}$ = $\overline{CAS} \geq V_{CC}$ − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

DC Characteristics; 3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				400	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

DC Current Requirements; 5-Volt Devices

Parameter	Symbol	-50	-60	-70	-80	Unit	Test Conditions
Operating current	I_{CC1}						
4216/42S16		110	100	90	80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} (min); I_O = 0 mA
4217/42S17		130	120	110	100	mA	
4218/42S18		170	160	150	140	mA	
Refresh current ($\overline{RAS}$ only refresh)	I_{CC3}						
4216/42S16		110	100	90	80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} (min); t_{RC} = t_{RC} (min); I_O = 0 mA
4217/42S17		130	120	110	100	mA	
4218/42S18		170	160	150	140	mA	
Operating current (Fast-page mode)	I_{CC4}						
4216/42S16		100	90	80	70	mA	$\overline{CAS}$ cycling; $\overline{RAS}$ ≤ V_{IL} (max); t_{PC} = t_{PC} (min); I_O = 0 mA
4217/42S17		100	90	80	70	mA	
4218/42S18		100	90	80	70	mA	
Refresh current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}						
4216/42S16		110	100	90	80	mA	$\overline{RAS}$ cycling; t_{RC} = t_{RC} (min); I_O = 0 mA
4217/42S17		130	120	110	100	mA	
4218/42S18		170	160	150	140	mA	
Battery backup current (Standby with $\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RAS} ≤ 300 ns		t_{RAS} ≤ 1 μs			Standby: $\overline{RAS}$ ≥ V_{CC} – 0.2 V; $\overline{RAS}$, $\overline{CAS}$: 0 V ≤ V_{IL} ≤ 0.2 V, V_{CC} – 0.2 V ≤ V_{IH} ≤ V_{IH} (max); $\overline{WE}$, $\overline{OE}$: V_{IH}; Address: don't care; Output: open
42S16		350		500		μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 4096 cycles, 256 ms
42S17		300		400		μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 2048 cycles, 256 ms
42S18		250		300		μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 1024 cycles, 256 ms

DC Current Requirements; 3.3-Volt Devices

Parameter	Symbol	-A60	-A70	-A80	Unit	Test Conditions
Operating current	I_{CC1}					
4216/42S16		90	80	70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ (min); I_O = 0 mA
4217/42S17		110	100	90	mA	
4218/42S18		150	140	130	mA	
Refresh current ($\overline{RAS}$ only refresh)	I_{CC3}					
4216/42S16		90	80	70	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$ (min); $t_{RC} = t_{RC}$ (min); I_O = 0 mA
4217/42S17		110	100	90	mA	
4218/42S18		150	140	130	mA	
Operating current (Fast-page mode)	I_{CC4}					
4216/42S16		80	70	60	mA	$\overline{CAS}$ cycling; $\overline{RAS} \leq V_{IL}$ (max); $t_{PC} = t_{PC}$ (min); I_O = 0 mA
4217/42S17		80	70	60	mA	
4218/42S18		80	70	60	mA	
Refresh current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}					
4216/42S16		90	80	70	mA	$\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ (min); I_O = 0 mA
4217/42S17		110	100	90	mA	
4218/42S18		150	140	130	mA	
Battery backup current (Standby with $\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$t_{RAS} \leq 300$ ns		$t_{RAS} \leq 1$ μs		Standby: $\overline{RAS} \geq V_{CC} - 0.2$ V; $\overline{RAS}$, $\overline{CAS}$: 0 V ≤ V_{IL} ≤ 0.2 V, $V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH}$ (max); $\overline{WE}$, $\overline{OE}$: V_{IH}; Address: don't care; Output: open
42S16		140		140	μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 4096 cycles, 256 ms
42S17		120		120	μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 2048 cycles, 256 ms
42S18		110		110	μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 1024 cycles, 256 ms

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10% (-50, -60, -70, -80) or +3.3 V ±0.3 V (-A60, -A70, -A80)

		-50		-60, -A60		-70, -A70		-80, -A80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Access time from column address	t_{AA}		25		30		35		40	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		30		35		40		45	ns	(Note 7)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	45		53		60		65		ns	(Note 15)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		13		15		18		20	ns	(Notes 7, 8)
Column address hold time	t_{CAH}	13		15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	10		10		10		10		ns	
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	−50		−50		−50		−50		ns	(Note 16)
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		0		ns	(Note 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	8		10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	8		10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		65		70		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		5		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	33		38		43		45		ns	(Note 15)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	13		15		15		15		ns	
Data-in hold time	t_{DH}	10		10		15		15		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 13)
Masked write hold time referenced to $\overline{RAS}$	t_{MRH}	0		0		0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		13		15		18		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	10		13		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	0	15	ns	(Note 9)

AC Characteristics (cont)

Parameter	Symbol	-50		-60, -A60		-70, -A70		-80, -A80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Output disable from $\overline{CAS}$ high	t_{OFF}	0	10	0	13	0	15	0	15	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		0		ns	(Note 7)
Fast-page read or write cycle time	t_{PC}	35		40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with extended data output	t_{PRWC}	80		85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	15	35	17	40	ns	(Note 8)
Row address hold time	t_{RAH}	8		10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	25		30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		100		μs	(Note 16)
Random read or write cycle time	t_{RC}	90		110		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	20	45	20	50	25	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}										
4216			64		64		64		64	ms	
4217			32		32		32		32	ms	
4218			16		16		16		16	ms	
42S16			256		256		256		256	ms	
42S17			256		256		256		256	ms	
42S18			256		256		256		256	ms	
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5		5		5		5		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	90		110		130		150		ns	(Note 16)
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	13		15		18		20		ns	
Read-modify-write cycle time	t_{RWC}	140		160		180		200		ns	(Note 6)

AC Characteristics (cont)

Parameter	Symbol	-50 Min	-50 Max	-60, -A60 Min	-60, -A60 Max	-70, -A70 Min	-70, -A70 Max	-80, -A80 Min	-80, -A80 Max	Unit	Test Conditions
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	70		83		95		105		ns	(Note 15)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	18		20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	
Write command hold time	t_{WCH}	8		10		10		15		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 14)
Write command pulse width	t_{WP}	8		10		10		15		ns	(Note 12)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by eight refresh cycles ($\overline{RAS}$ only or CBR) before proper device operation is achieved.

(3) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(4) Ac measurements assume t_T = 5 ns.

(5) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max).
If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a late write cycle. For early write cycles, t_{WCH} must be met.

(13) These parameters are referenced to the leading edge of $\overline{CAS}$ in early write cycles and to the leading edge of $\overline{WE}$ in late write or read-modify-write cycles.

(14) If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle.

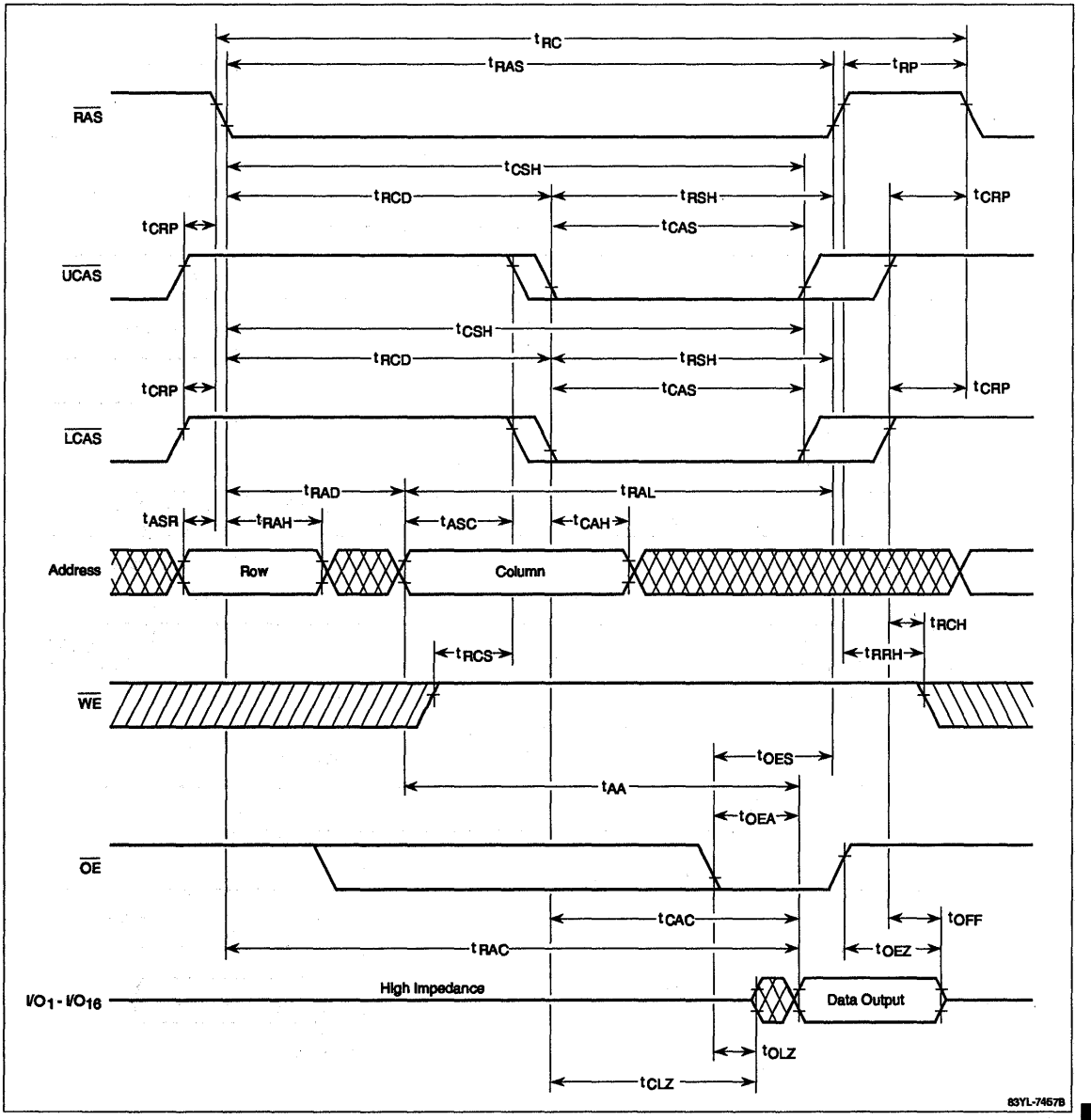
(15) If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(16) Parameter is applicable only to self-refresh versions.

(17) With burst CBR, $\overline{RAS}$ only, or external $\overline{RAS}$/$\overline{CAS}$, all addresses must be refreshed before entering self-refresh mode and after exiting.

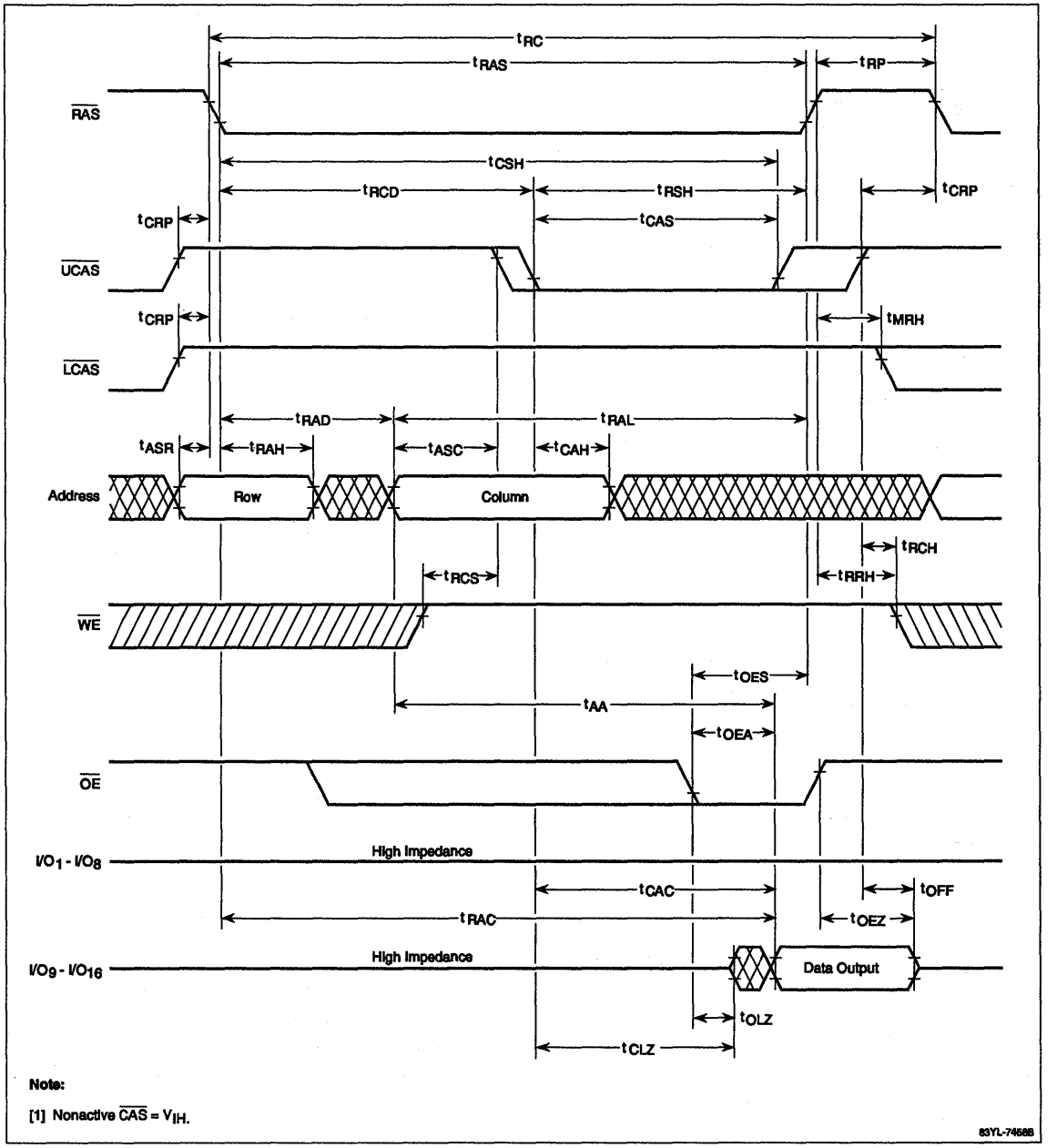
Timing Waveforms

Word Read Cycle



Timing Waveforms (cont)

Byte Read Cycle



Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

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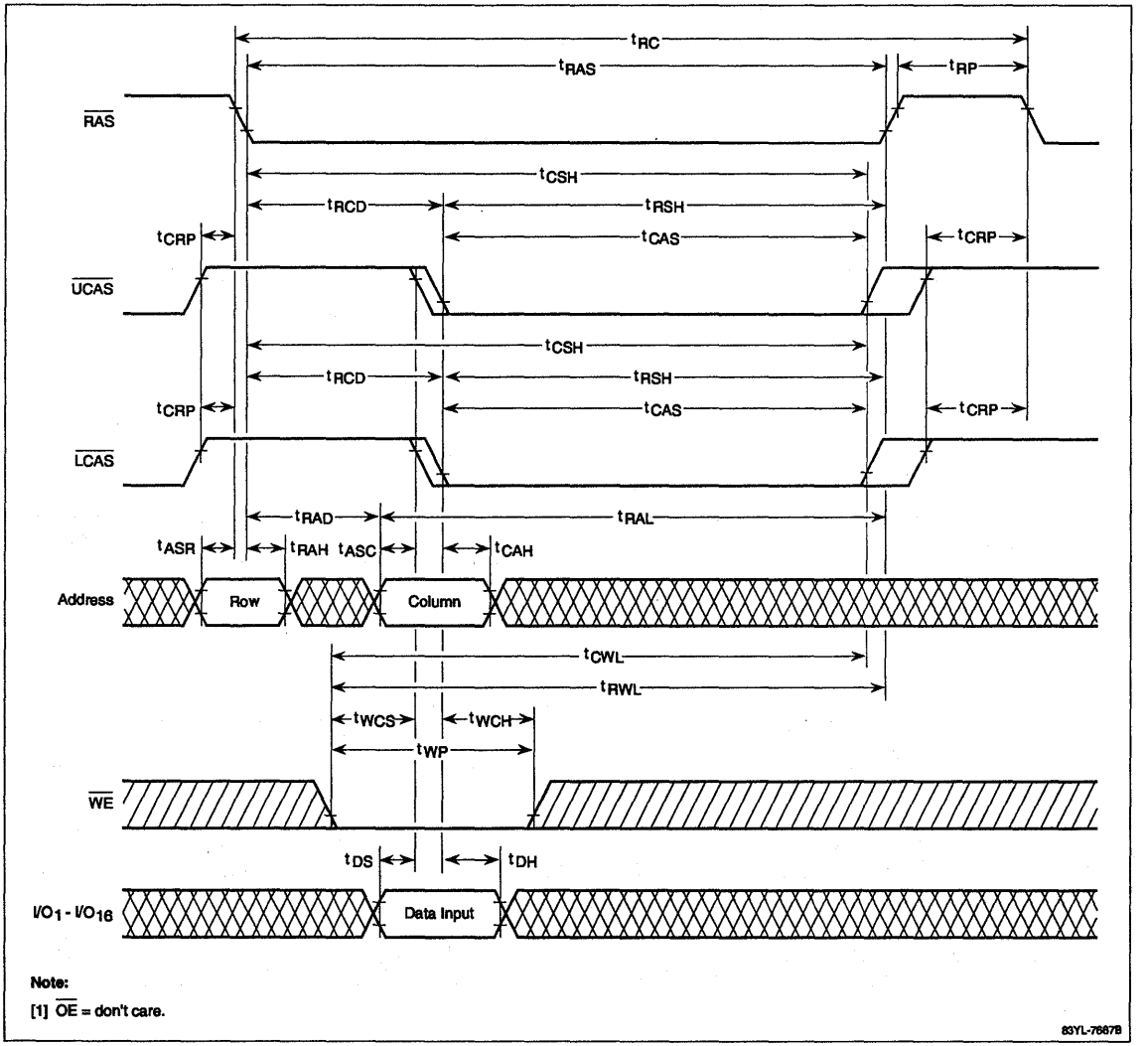
Timing Waveforms (cont)

Word Early-Write Cycle



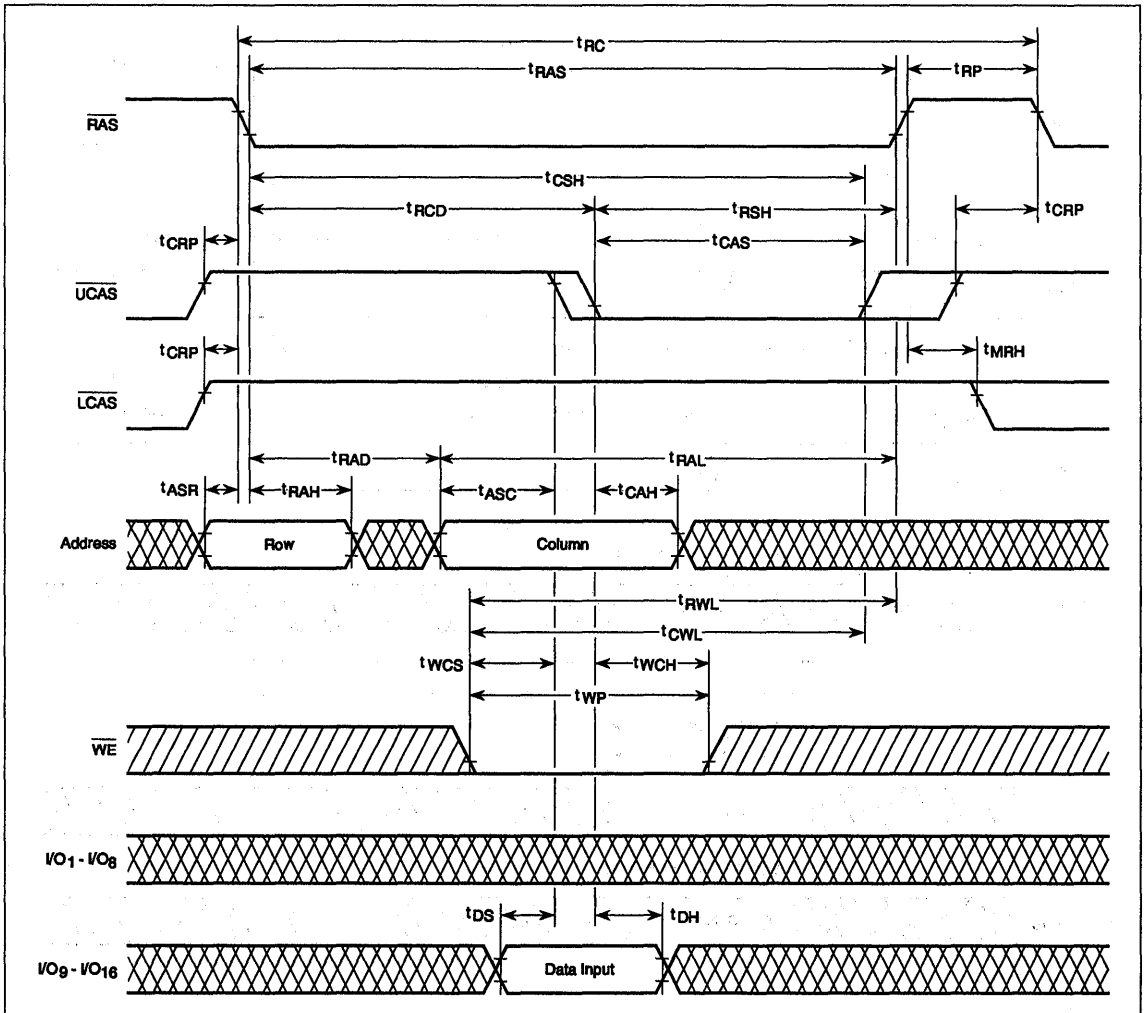
Note:

[1] $\overline{OE}$ = don't care.

83YL-76678

Timing Waveforms (cont)

Byte Early-Write Cycle



Notes:

[1] Nonactive $\overline{CAS}$ = V_{IH}.

[2] $\overline{OE}$ = don't care.

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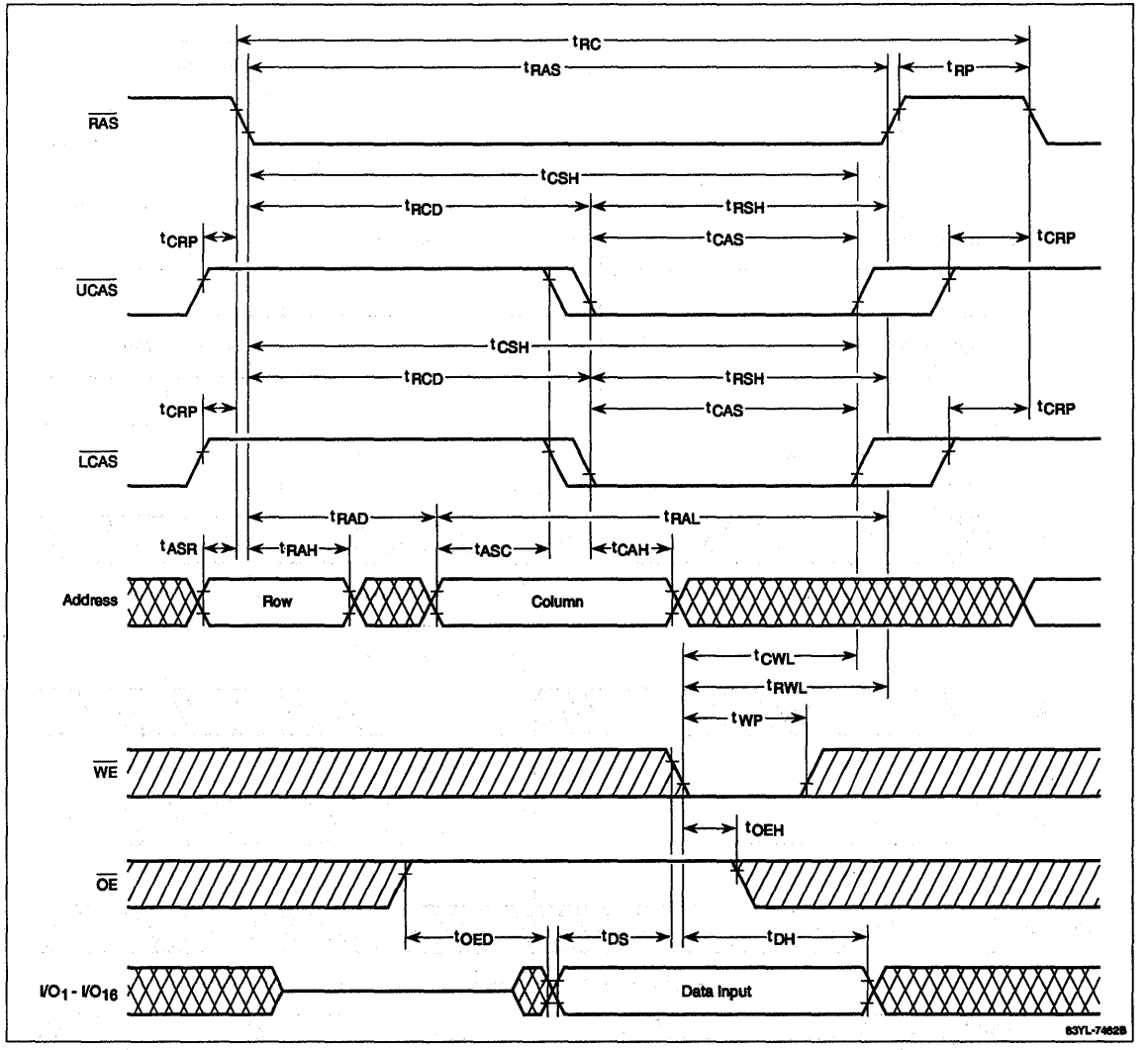
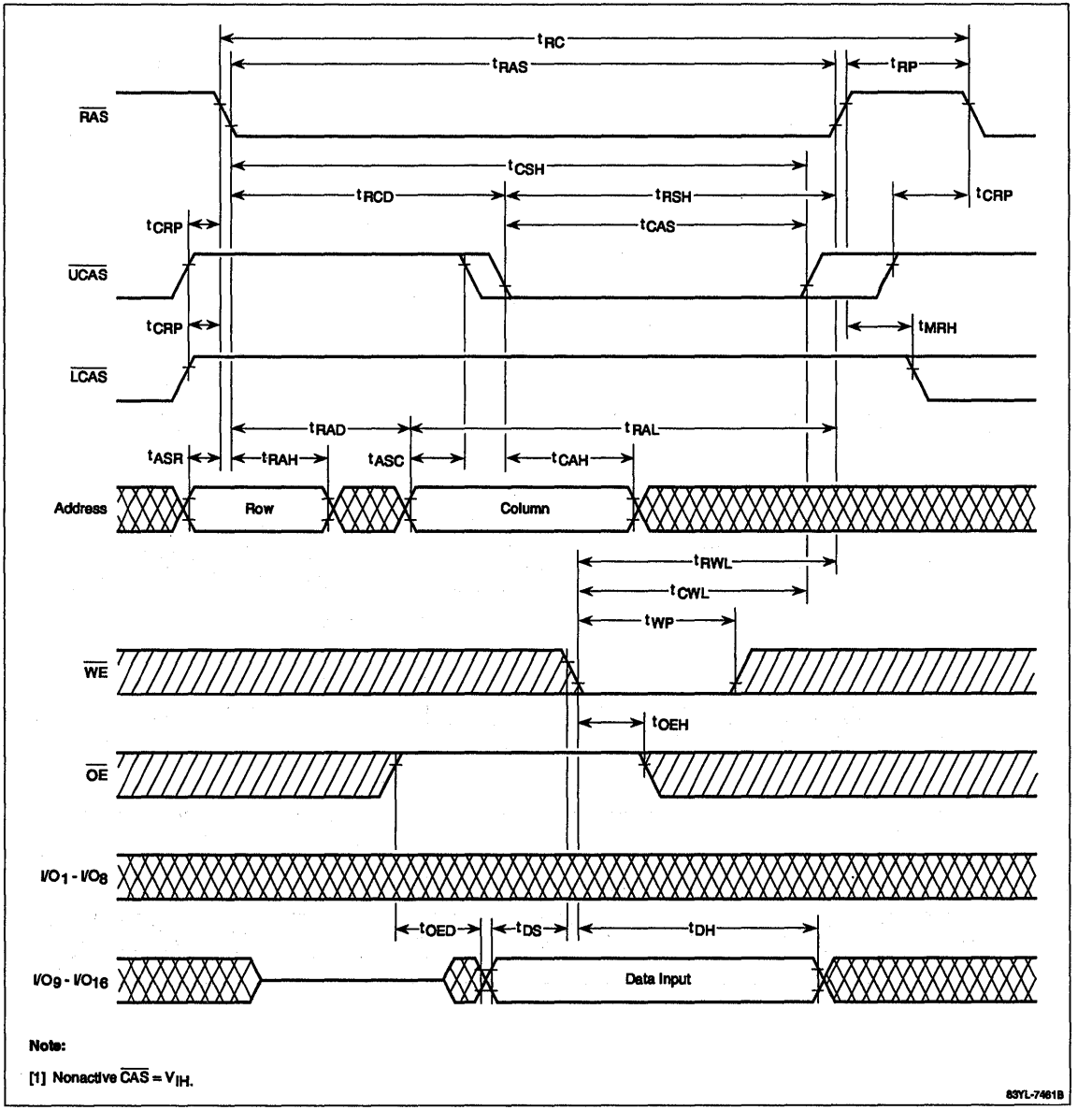
Timing Waveforms (cont)

Word Late-Write Cycle



Timing Waveforms (cont)

Byte Late-Write Cycle



Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

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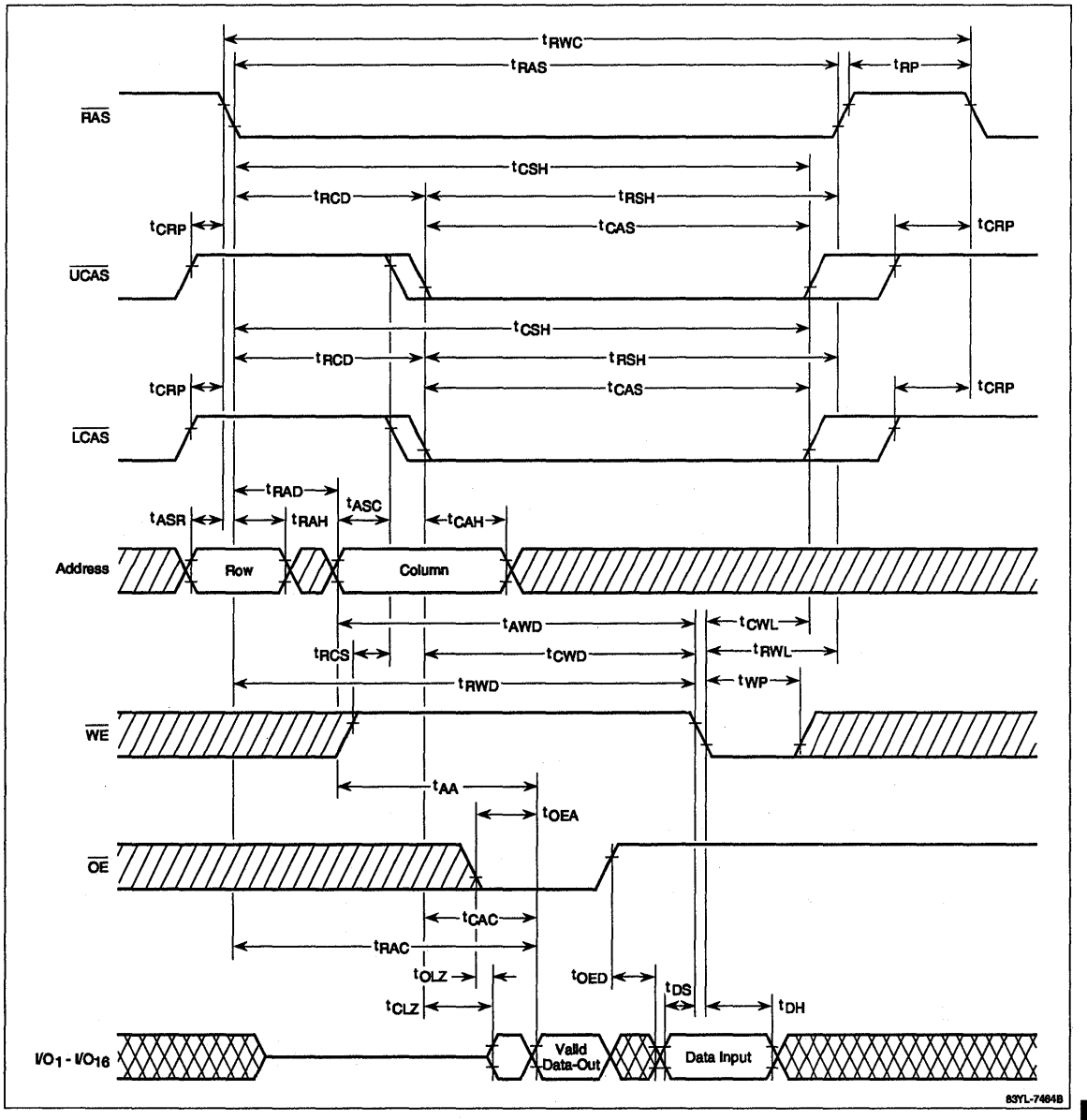
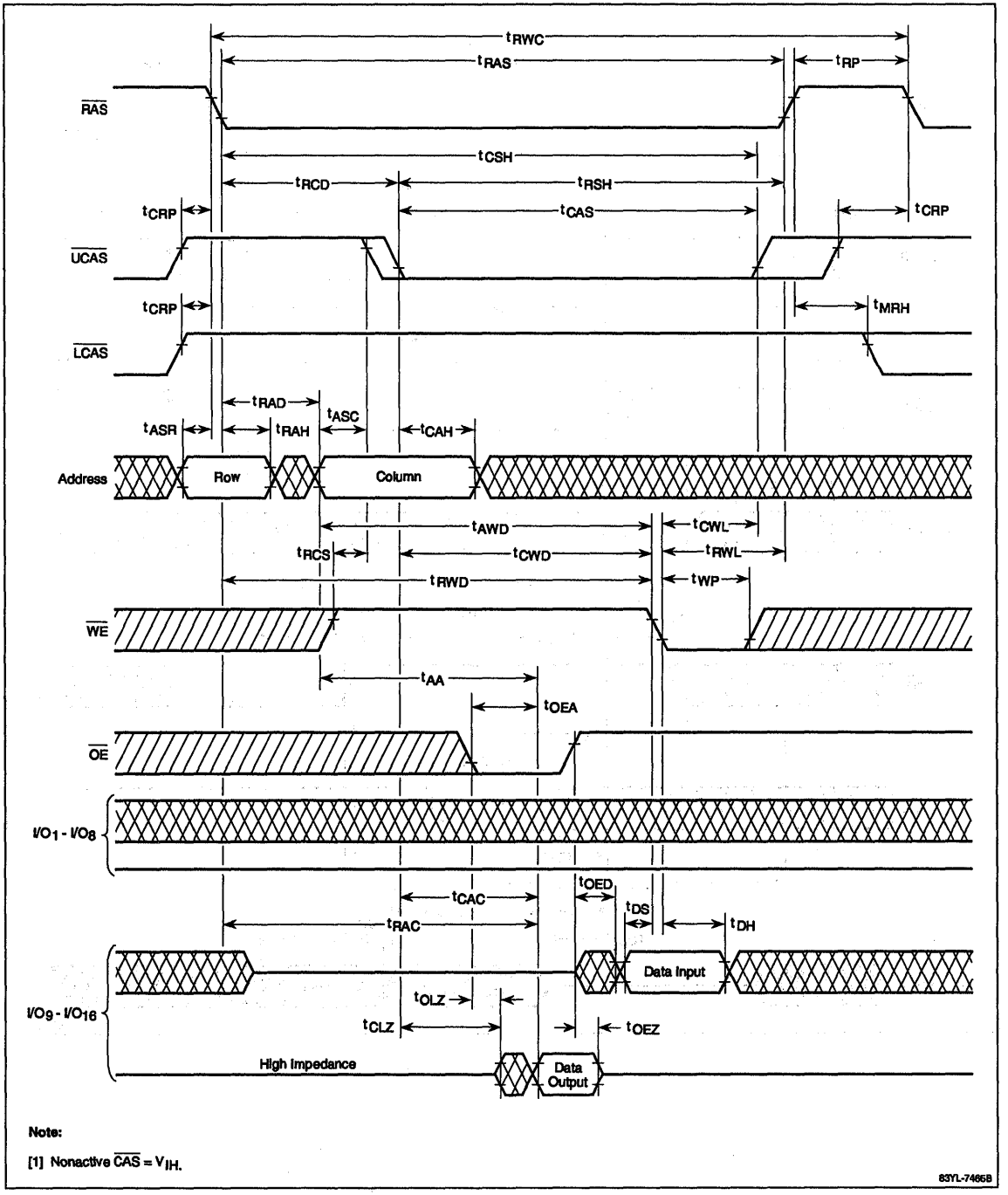
Timing Waveforms (cont)

Word Read-Modify-Write Cycle



Timing Waveforms (cont)

Byte Read-Modify-Write Cycle



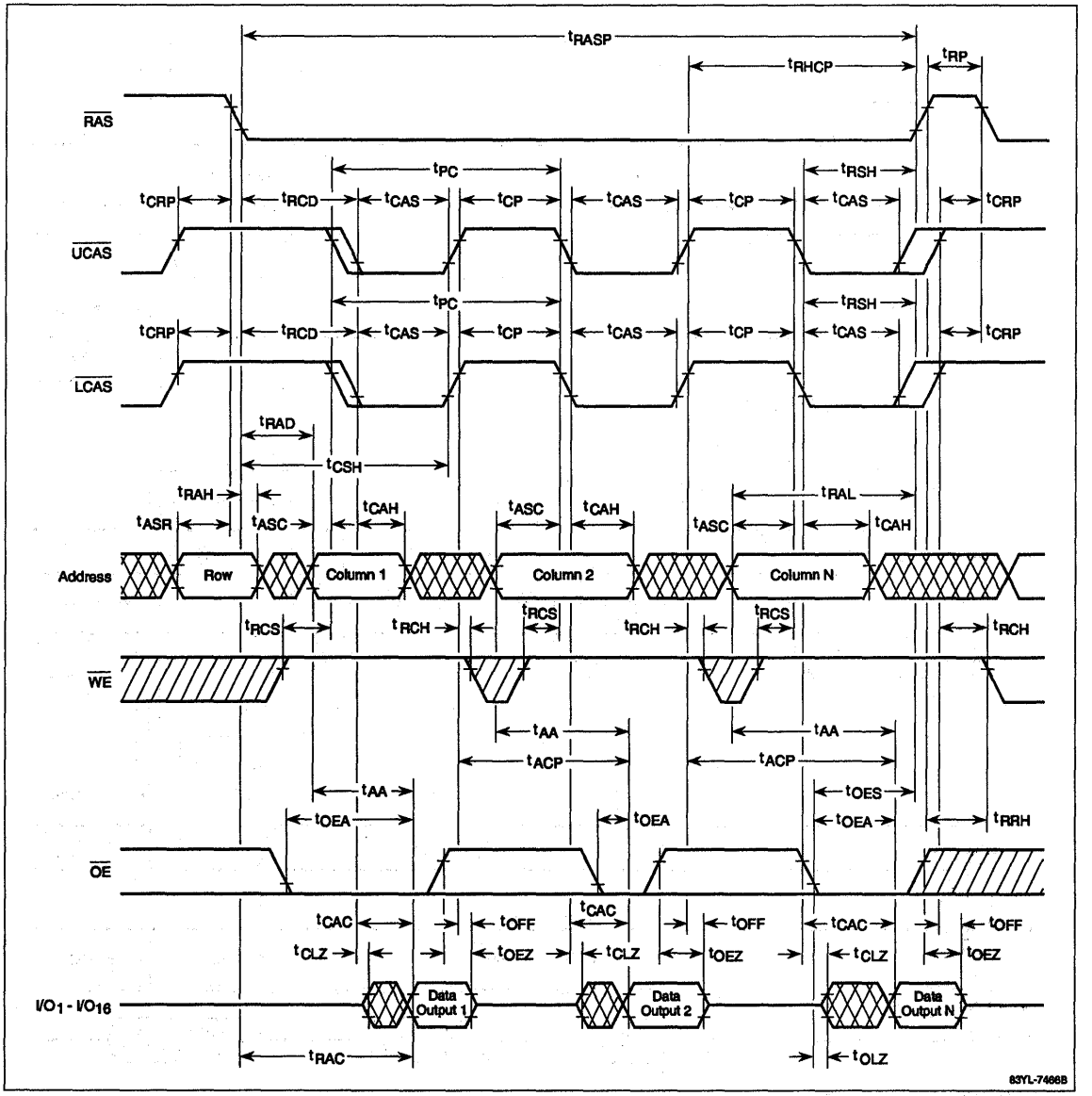
Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-7466B

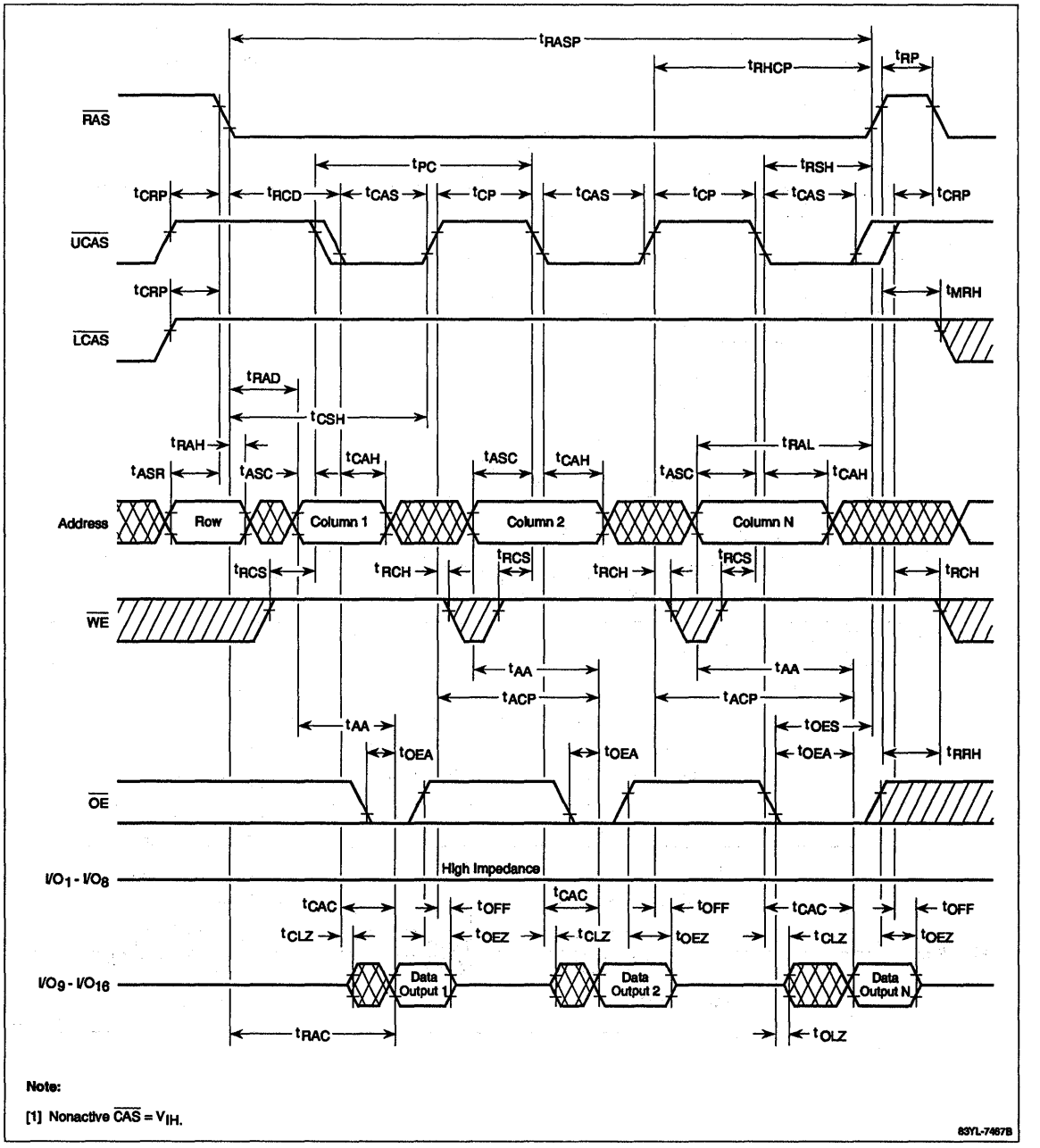
Timing Waveforms (cont)

Word Fast-Page Read Cycle



Timing Waveforms (cont)

Byte Fast-Page Read Cycle



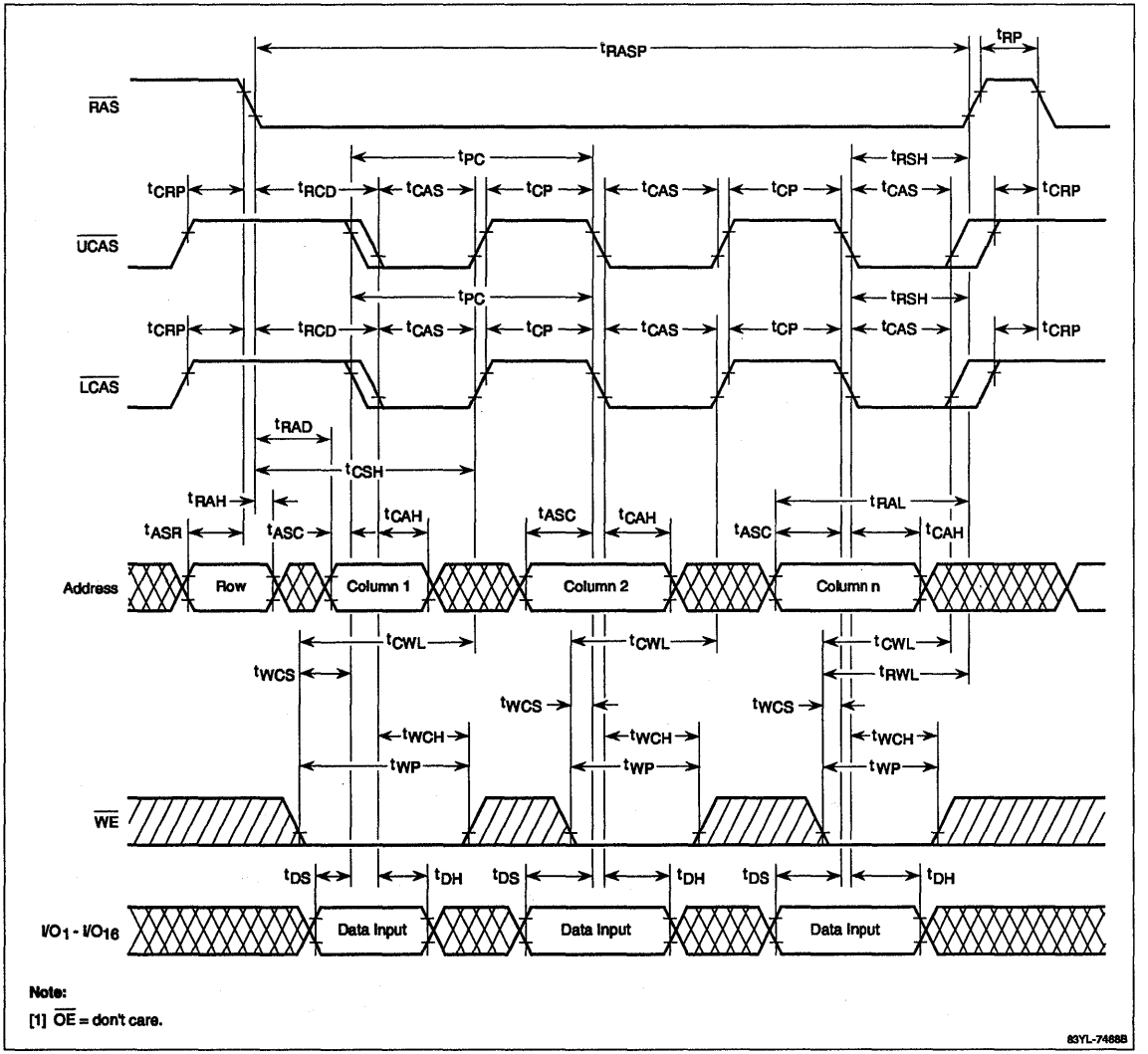
Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-7467B

Timing Waveforms (cont)

Word Fast-Page Early-Write Cycle



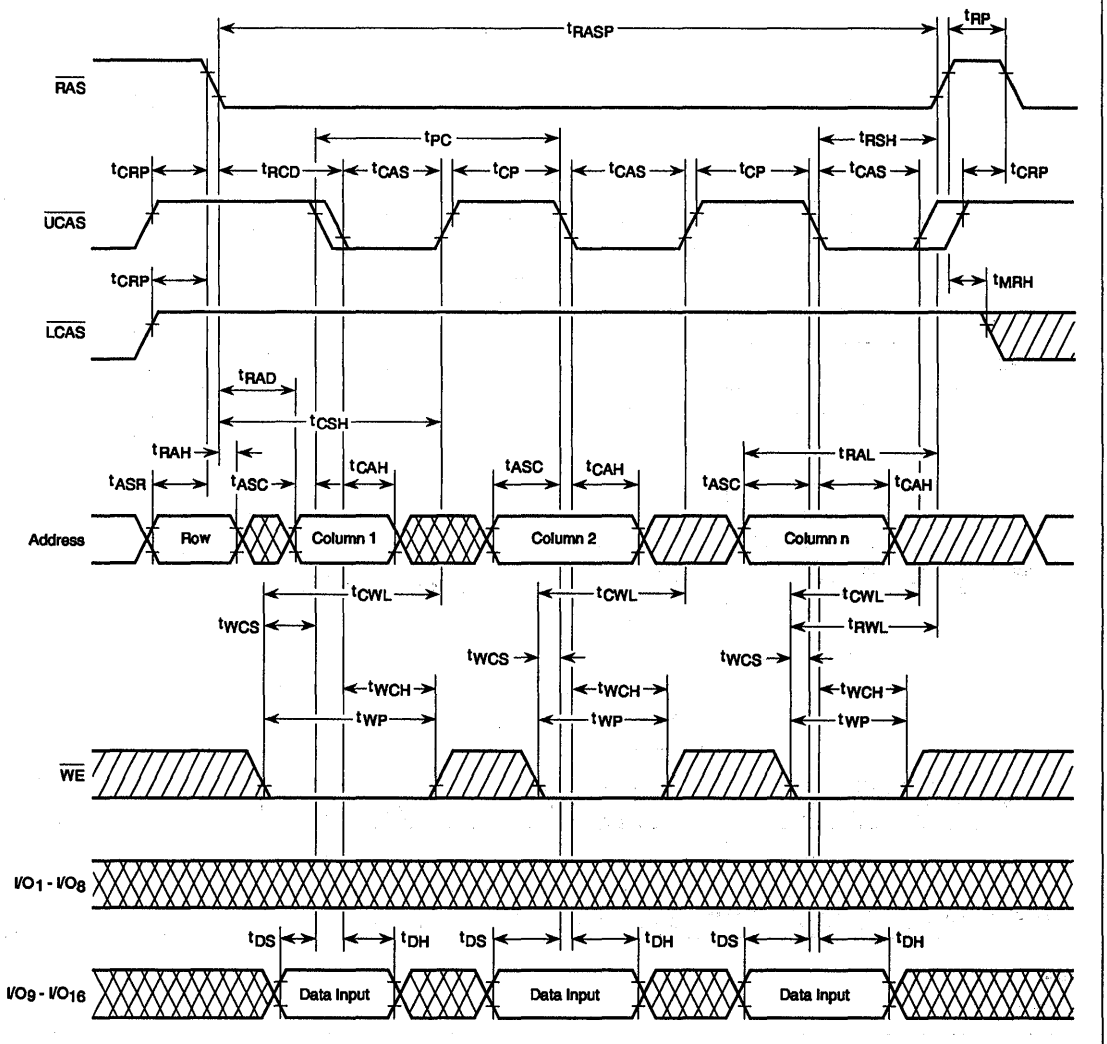
Note:

[1] $\overline{OE}$ = don't care.

83YL-7468B

Timing Waveforms (cont)

Byte Fast-Page Early-Write Cycle



Notes:

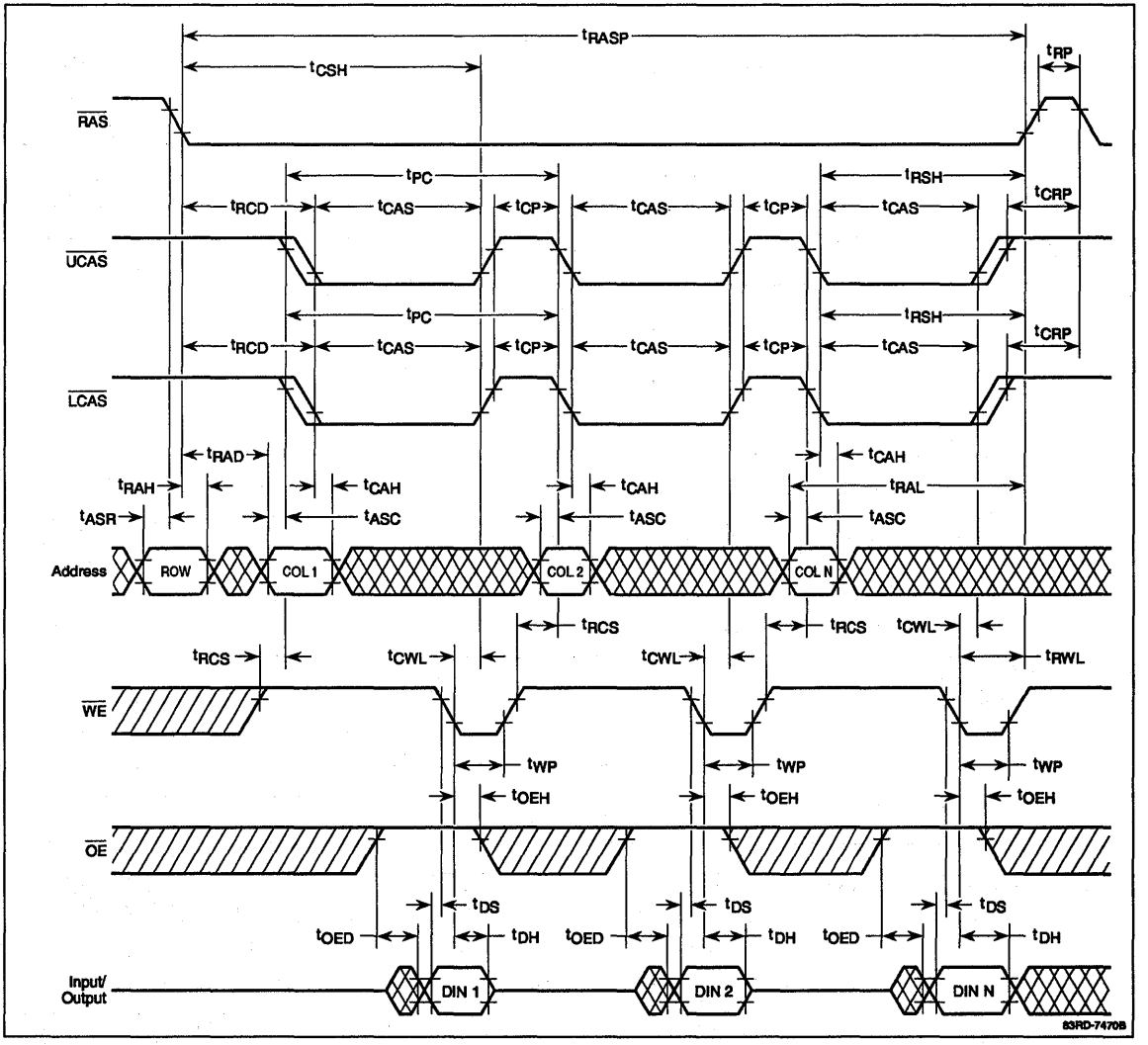
[1] Nonactive $\overline{CAS}$ = V_{IH}.

[2] $\overline{OE}$ = don't care.

83YL-7469B

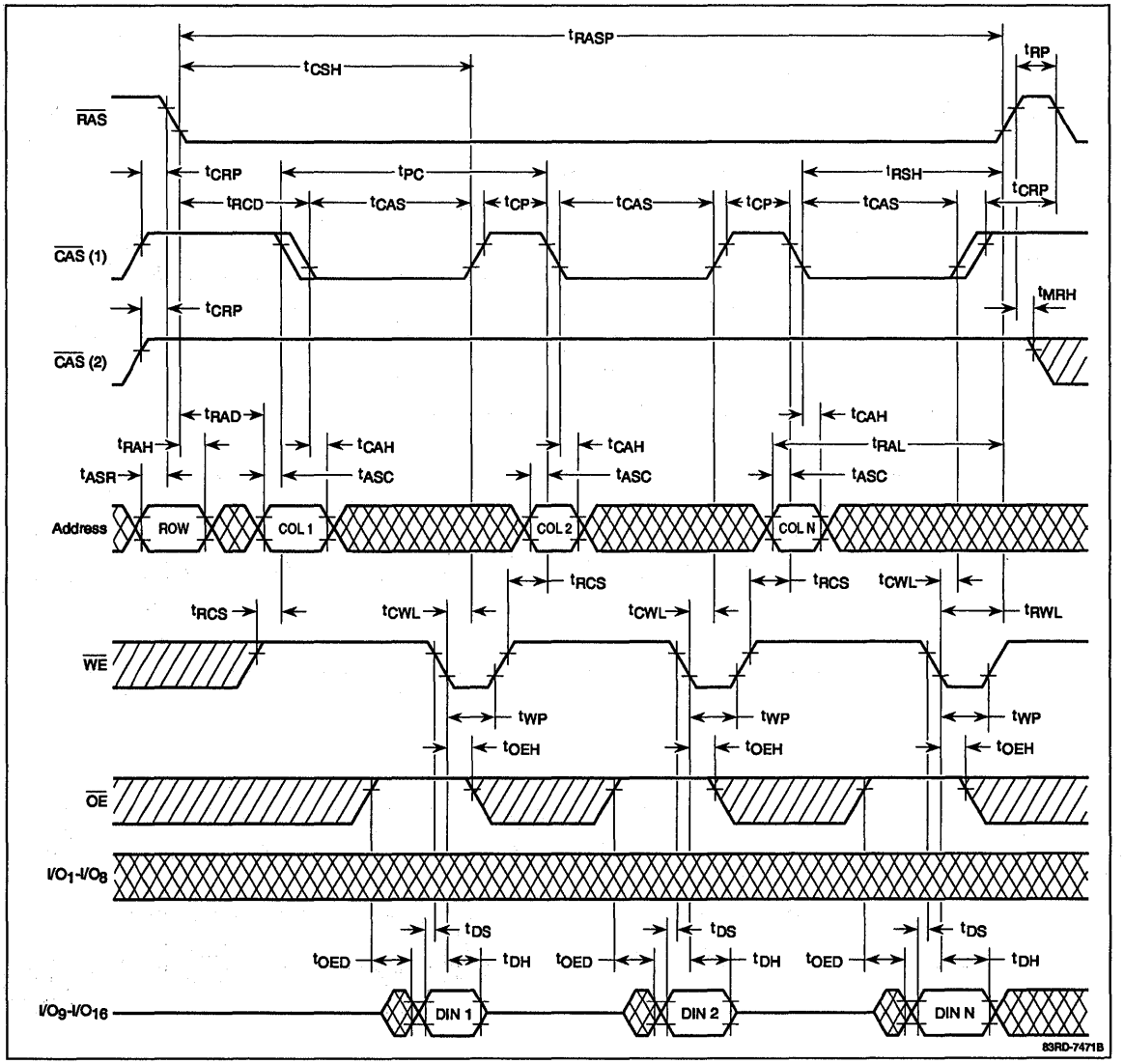
Timing Waveforms (cont)

Word Fast-Page Late-Write Cycle



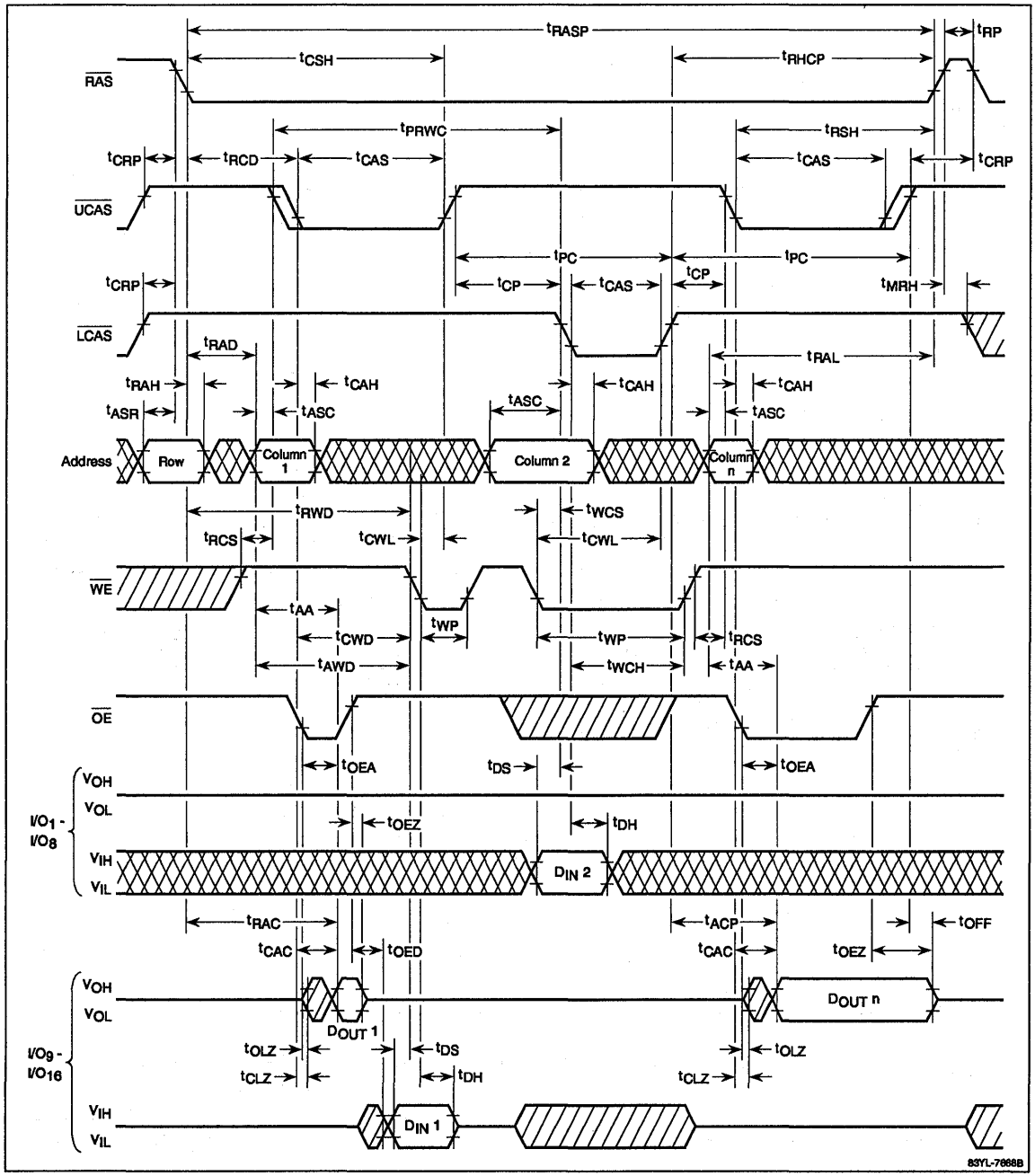
Timing Waveforms (cont)

Byte Fast-Page Late-Write Cycle



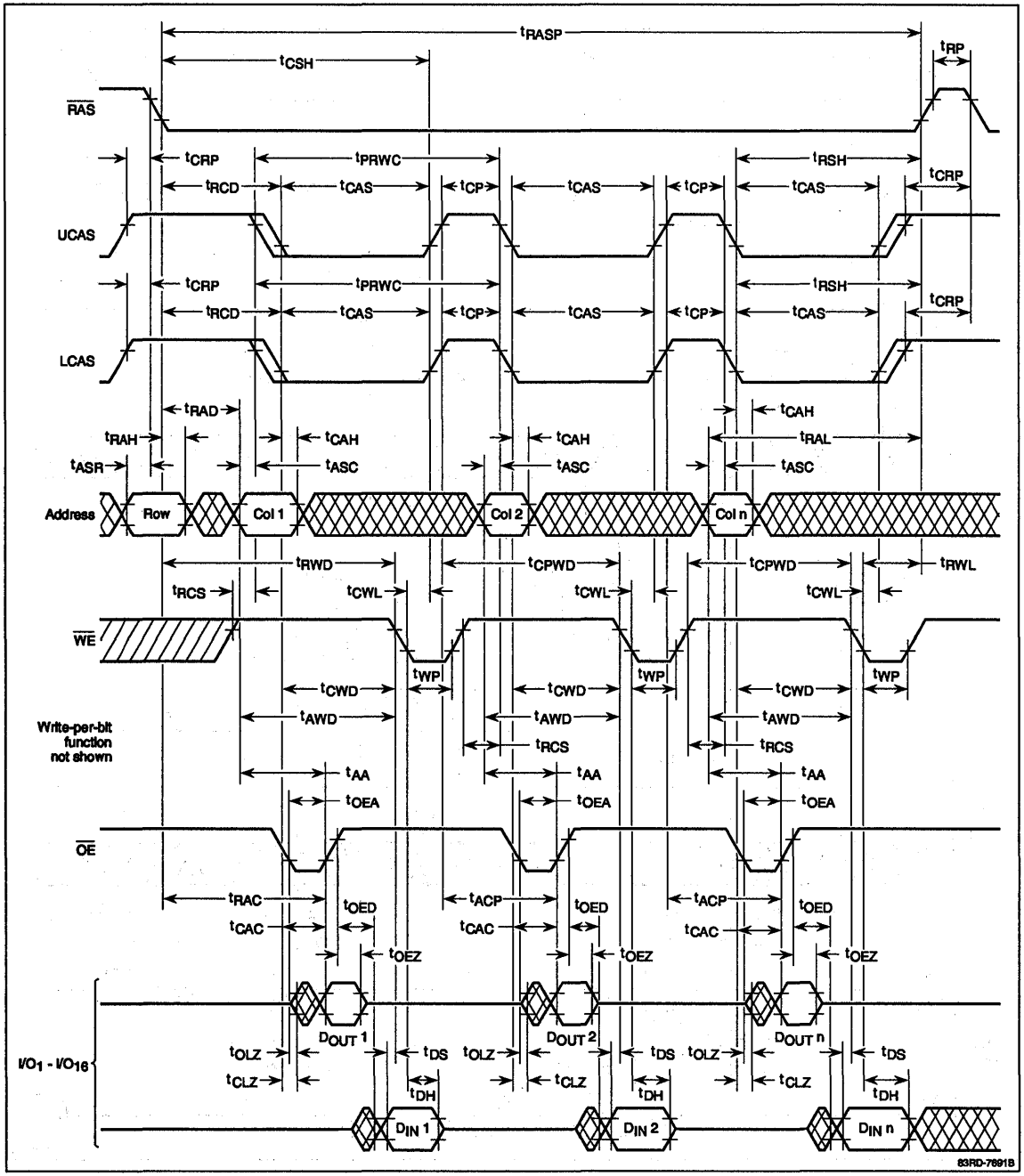
Timing Waveforms (cont)

Byte Fast-Page Read/Write Cycle



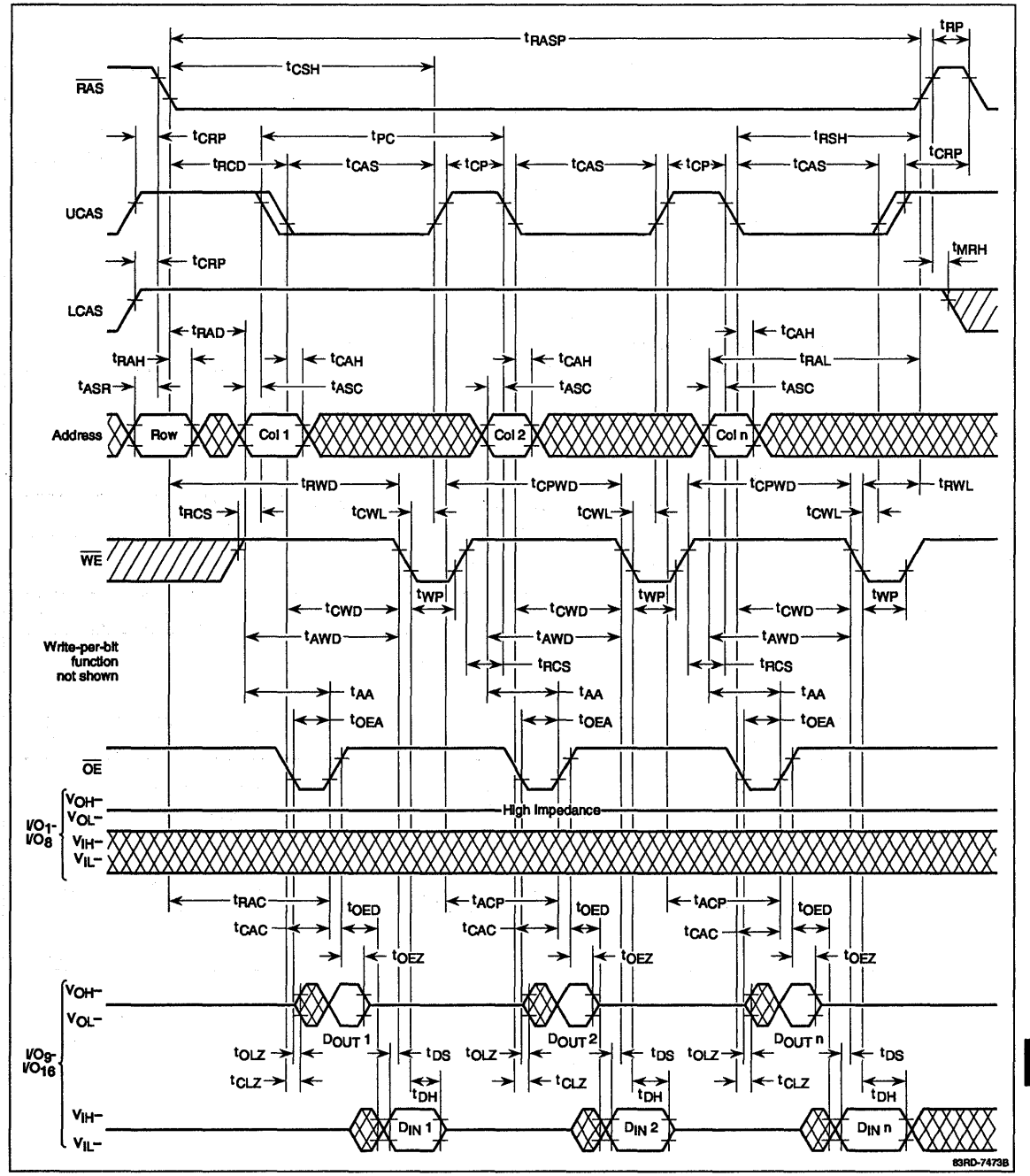
Timing Waveforms (cont)

Word Fast-Page Read-Modify-Write Cycle



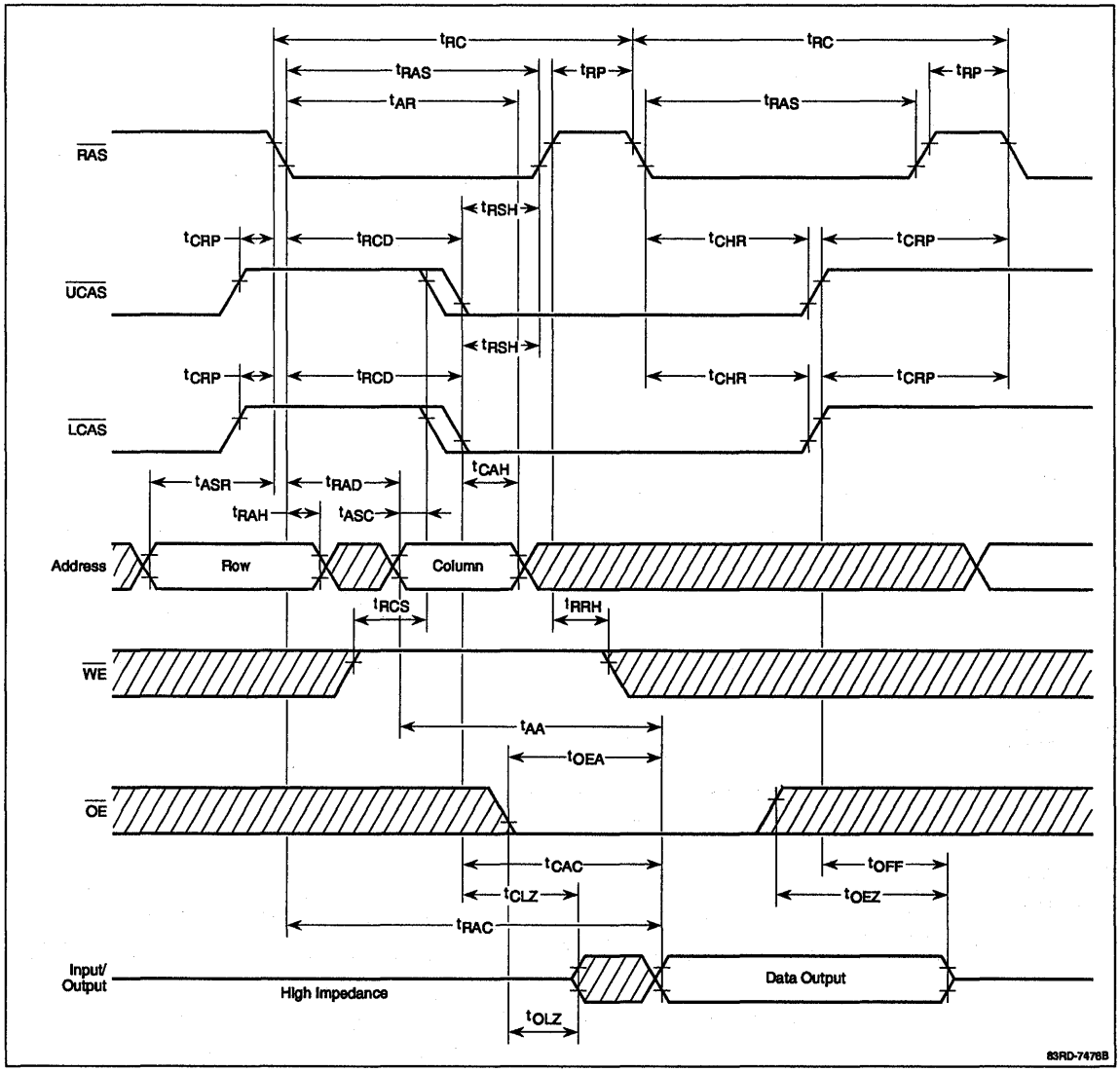
Timing Waveforms (cont)

Byte Fast-Page Read-Modify-Write Cycle



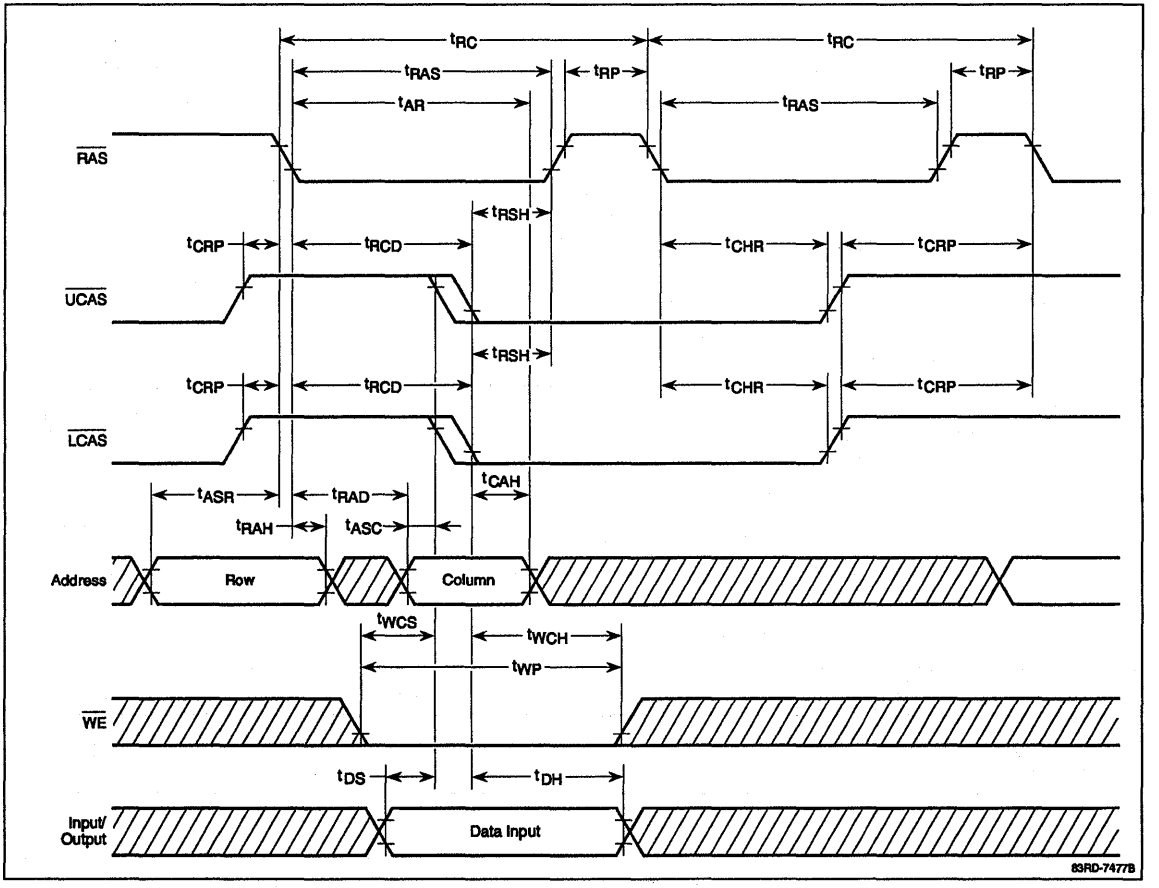
Timing Waveforms (cont)

Hidden-Refresh Cycle (Word Read Cycle)



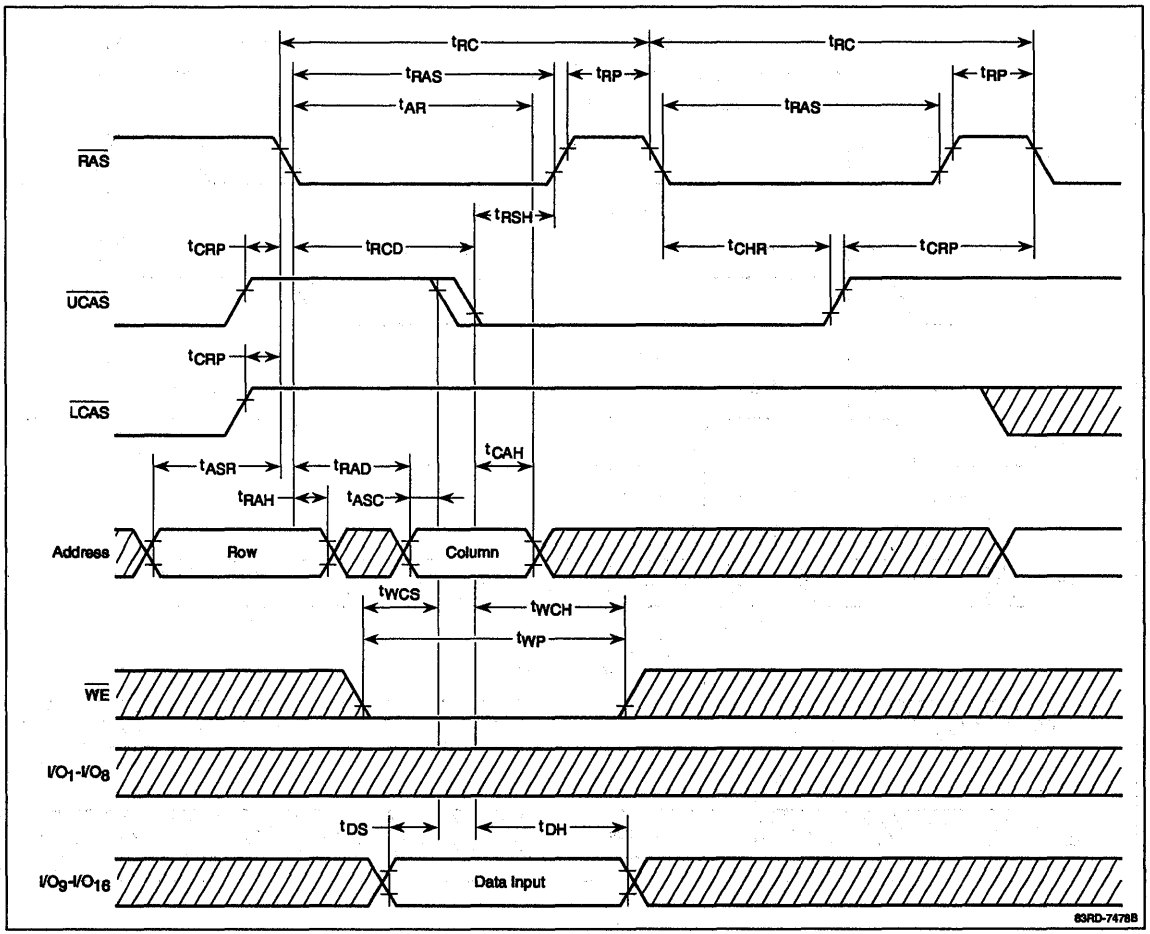
Timing Waveforms (cont)

Hidden-Refresh Cycle (Word Write Cycle)



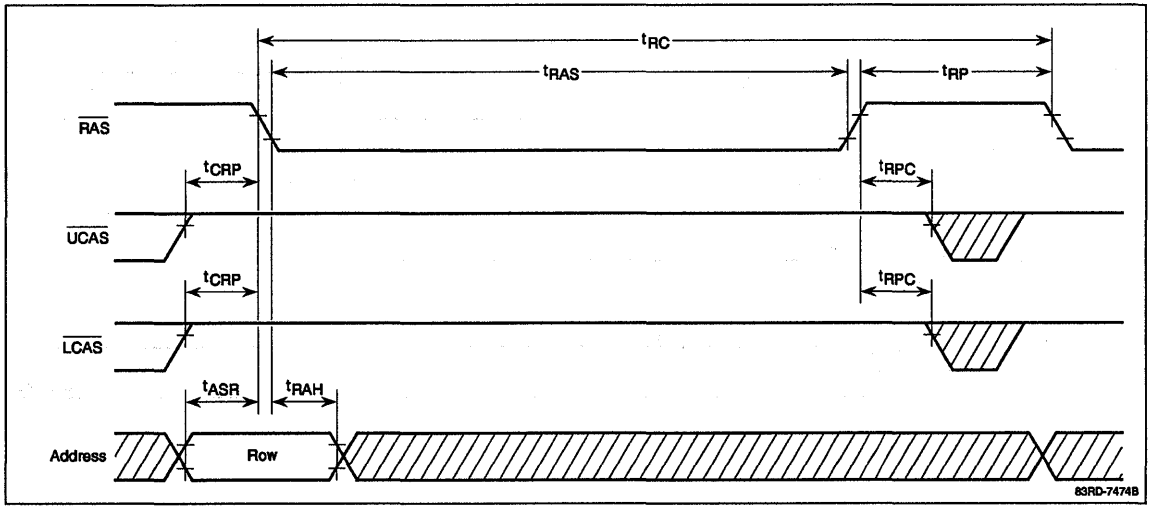
Timing Waveforms (cont)

Hidden-Refresh Cycle (Byte Write Cycle)

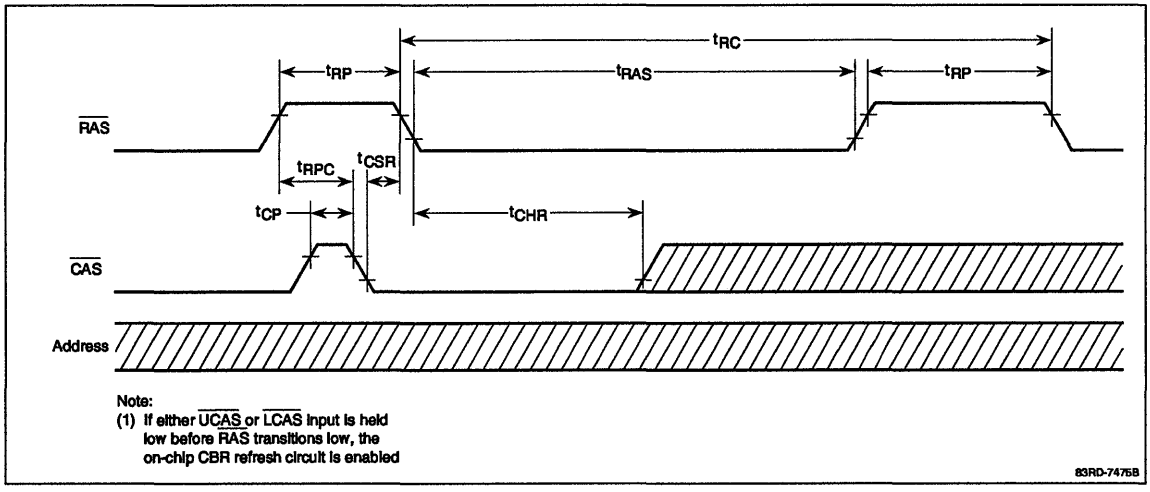


Timing Waveforms (cont)

$\overline{\text{RAS}}$-Only Refresh Cycle



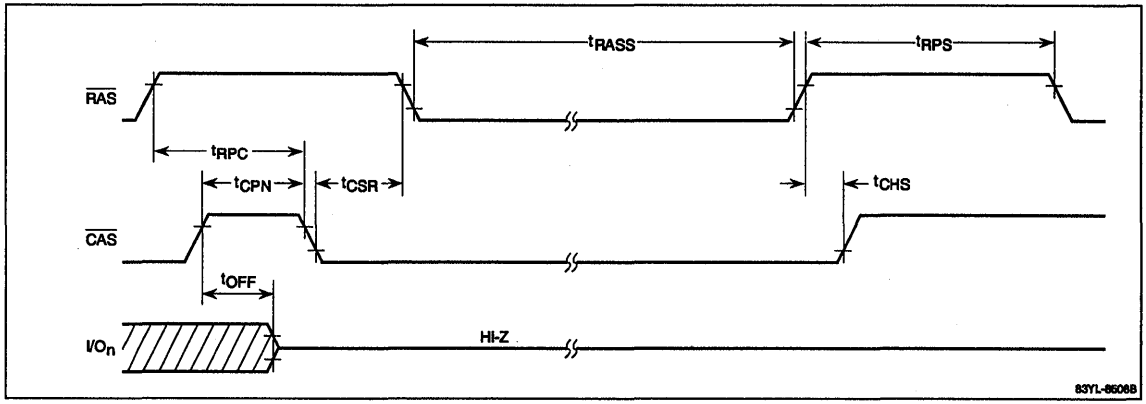
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



81

Timing Waveforms (cont)

CBR Self-Refresh Cycle



NEC Electronics Inc.

μPD421x180/L, 42S1x180/L (x = 6, 7, 8) 1,048,576 x 18-Bit Dynamic CMOS RAM

Description

The devices listed below are fast-page dynamic RAMs organized as 1M words by 18 bits and designed to operate from a single power supply. Optional features are power supply voltage (+5 V or +3.3 V), a new refresh mode called "self-refresh," and the number of cycles in a refresh period.

μPD	Power	Self-Refresh	Refresh Cycles
4216180	+5 V	—	4096 in 64 ms
180L	+3.3 V	—	
42S16180	+5 V	√	4096 in 256 ms
180L	+3.3 V	√	
4217180	+5 V	—	2048 in 32 ms
180L	+3.3 V	—	
42S17180	+5 V	√	2048 in 256 ms
180L	+3.3 V	√	
4218180	+5 V	—	1024 in 16 ms
180L	+3.3 V	—	
42S18180	+5 V	√	1024 in 256 ms
180L	+3.3 V	√	

Note: Letters L and S denote 3.3-volt and self-refresh devices, respectively.

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation while an on-chip circuit internally generates the negative voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{UCAS}$ and $\overline{LCAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, upper or lower byte data is held on the outputs by maintaining $\overline{UCAS}$ or $\overline{LCAS}$ low. Data outputs return to high impedance when $\overline{UCAS}$ or $\overline{LCAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{UCAS}$ or $\overline{LCAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh addresses.

For the 4216/42S16, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 4096 address combinations of A_0 - A_{11} will refresh all memory locations. Bits A_0 - A_{11} are used for row and refresh addresses, A_0 - A_7 for column addresses.

For the 4217/42S17, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 2048 address combinations of A_0 - A_{10} will refresh all memory locations. Bits A_0 - A_{10} are used for row and refresh addresses, A_0 - A_8 for column addresses.

For the 4218/42S18, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 1024 address combinations of A_0 - A_9 will refresh all memory locations. Bits A_0 - A_9 are used for row, refresh, and column addresses.

The self-refresh mode is entered by holding $\overline{RAS}$ and $\overline{CAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 μA (+5 V) or 80 μA (+3.3 V). Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Battery backup current I_{CC6} is defined as the current consumption when the device is in standby mode ($\overline{RAS} \geq V_{CC} - 0.2$ V) and very-slow (extended) CBR cycles are being performed.

Features

- 1,048,576 by 18-bit organization
- Single power supply: +5-volt or +3.3 volt
- Fast-page option
- Low-power operation
- Byte read/write control with $\overline{UCAS}$ and $\overline{LCAS}$
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Self-refresh option (slow internal automatic refresh)
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 42-pin SOJ and 50/44-pin TSOP plastic packages

Pin Identification

Name	Function
A_0 - A_{11}	Address inputs
I/O_1 - I/O_{18}	Data inputs and outputs
$\overline{LCAS}$, $\overline{UCAS}$	Column address strobes
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

Pin Configurations

42-Pin Plastic SOJ

μPD4216/42S16, 4217/42S17, 4218/42S18

V_{CC}	1	42	GND
I/O_1	2	41	I/O_{18}
I/O_2	3	40	I/O_{17}
I/O_3	4	39	I/O_{16}
I/O_4	5	38	I/O_{15}
V_{CC}	6	37	GND
I/O_5	7	36	I/O_{14}
I/O_6	8	35	I/O_{13}
I/O_7	9	34	I/O_{12}
I/O_8	10	33	I/O_{11}
I/O_9	11	32	I/O_{10}
NC	12	31	$\overline{LCAS}$
$\overline{WE}$	13	30	$\overline{UCAS}$
$\overline{RAS}$	14	29	$\overline{OE}$
*A11	15	28	A_9
*A_{10}	16	27	A_8
A_0	17	26	A_7
A_1	18	25	A_6
A_2	19	24	A_5
A_3	20	23	A_4
V_{CC}	21	22	GND

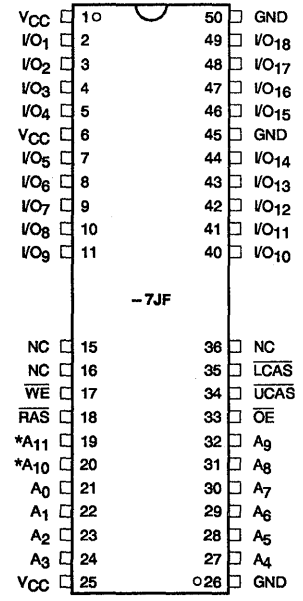
* Pin 15 is NC for 4217/42S17, 4218/42S18
Pin 16 is NC for 4218/42S18.

83FM-8154A

Pin Configurations (cont)

50/44-Pin Plastic TSOP (Normal Pinouts)

μPD4216/42S16, 4217/42S17, 4218/42S18



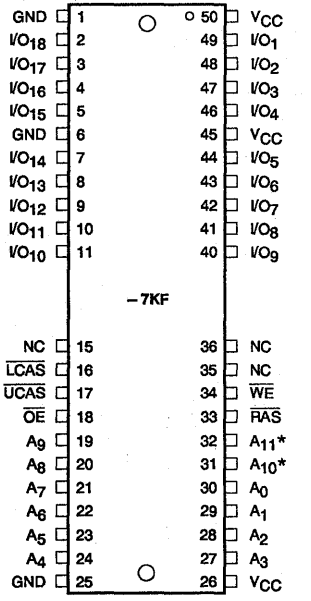
* Pin 19 is NC for 4217/42S17, 4218/42S18
Pin 20 is NC for 4218/42S18.

Suffix -7JF in the package identifier denotes normal pinout sequence.

83FM-8522A

50/44-Pin Plastic TSOP (Reverse Pinouts)

μPD4216/42S16, 4217/42S17, 4218/42S18



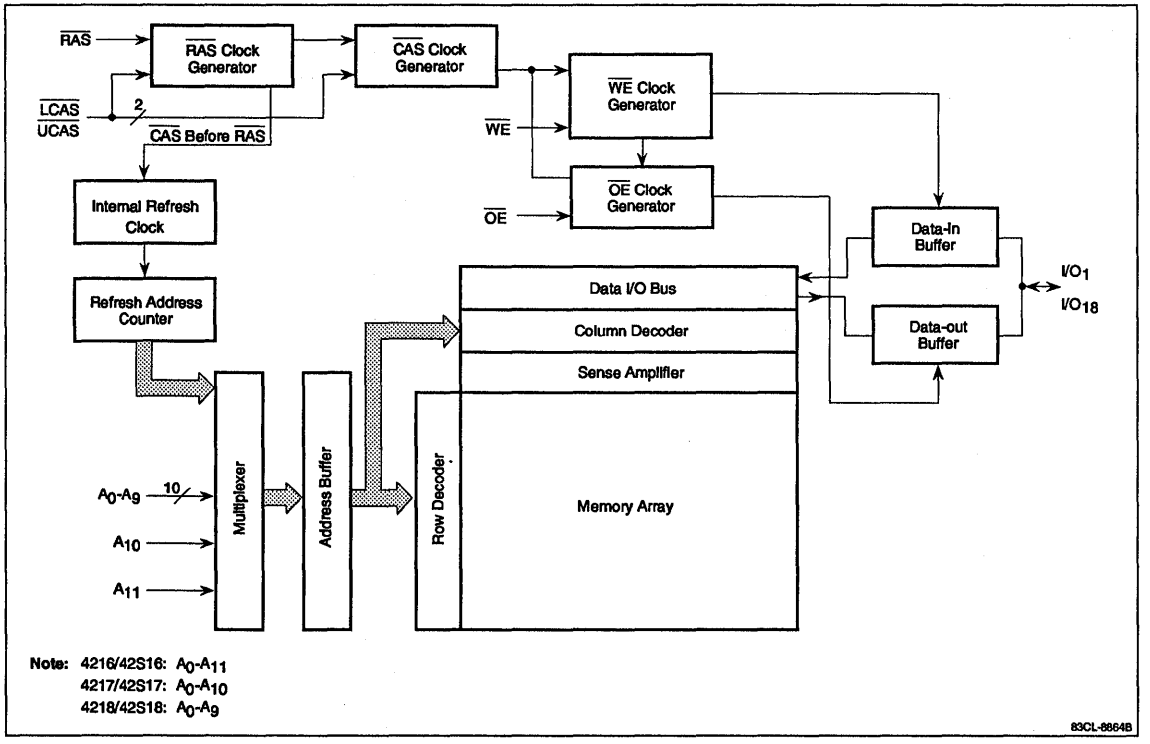
* Pin 32 is NC for 4217/42S17, 4218/42S18
Pin 31 is NC for 4218/42S18.

Suffix -7KF in the package identifier denotes reverse pinout sequence.

83FM-8523A

8m

Block Diagram



Truth Table

Function	RAS	LCAS	UCAS	WE	OE	I/O_1 - I/O_9	I/O_{10} - I/O_{18}
Standby	H	X	X	X	X	High-Z	High-Z
Refresh cycle	L	H	H	X	X	High-Z	High-Z
Byte read cycle	L	L	H	H	L	Data output	High-Z
	L	H	L	H	L	High-Z	Data output
Word read cycle	L	L	L	H	L	Data output	Data output
Byte write cycle	L	L	H	L	H	Data input	—
	L	H	L	L	H	—	Data input
Word write cycle	L	L	L	L	H	Data input	Data input
——	L	L	L	H	H	High-Z	High-Z

X = don't care.

Ordering Information, μPD4216180 (+ 5-volt power; 4096 refresh cycles)

Part Number	RAS Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4216180LE-50	50 ns	35 ns	350 μA	42-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD4216180G5-50	50 ns	35 ns	350 μA	50/44-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD4216180G5M-50	50 ns	35 ns	350 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD4216180L (+ 3.3-volt power; 4096 refresh cycles)

Part Number	RAS Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4216180LLE-A60	60 ns	40 ns	140 μA	42-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD4216180LG5-A60	60 ns	40 ns	140 μA	50/44-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD4216180LG5M-A60	60 ns	40 ns	140 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD42S16180 (+ 5-volt power; 4096 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S16180LE-50	50 ns	35 ns	350 μA	42-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD42S16180G5-50	50 ns	35 ns	350 μA	50/44-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD42S16180G5M-50	50 ns	35 ns	350 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD42S16180L (+ 3.3-volt power; 4096 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S16180LLE-A60	60 ns	40 ns	140 μA	42-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD42S16180LG5-A60	60 ns	40 ns	140 μA	50/44-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD42S16180LG5M-A60	60 ns	40 ns	140 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD4217180 (+ 5-volt power; 2048 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4217180LE-50	50 ns	35 ns	300 μA	42-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD4217180G5-50	50 ns	35 ns	300 μA	50/44-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD4217180G5M-50	50 ns	35 ns	300 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD4217180L (+ 3.3-volt power; 2048 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4217180LLE-A60	60 ns	40 ns	120 μA	42-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD4217180LG5-A60	60 ns	40 ns	120 μA	50/44-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD4217180LG5M-A60	60 ns	40 ns	120 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD42S17180 (+ 5-volt power; 2048 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S17180LE-50	50 ns	35 ns	300 μA	42-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD42S17180G5-50	50 ns	35 ns	300 μA	50/44-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD42S17180G5M-50	50 ns	35 ns	300 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD42S17180L (+ 3.3-volt power; 2048 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S17180LLE-A60	60 ns	40 ns	120 μA	42-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD42S17180LG5-A60	60 ns	40 ns	120 μA	50/44-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD42S17180LG5M-A60	60 ns	40 ns	120 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD4218180 (+ 5-volt power; 1024 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4218180LE-50	50 ns	35 ns	250 μA	42-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD4218180G5-50	50 ns	35 ns	250 μA	50/44-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD4218180G5M-50	50 ns	35 ns	250 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD4218180L (+ 3.3-volt power; 1024 refresh cycles)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD4218180LLE-A60	60 ns	40 ns	110 μA	42-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD4218180LG5-A60	60 ns	40 ns	110 μA	50/44-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD4218180LG5M-A60	60 ns	40 ns	110 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Ordering Information, μPD42S18180 (+ 5-volt power; 1024 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S18180LE-50	50 ns	35 ns	250 μA	42-pin plastic SOJ
LE-60	60 ns	40 ns		
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD42S18180G5-50	50 ns	35 ns	250 μA	50/44-pin plastic TSOP (normal pinouts)
G5-60	60 ns	40 ns		
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD42S18180G5M-50	50 ns	35 ns	250 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-60	60 ns	40 ns		
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD42S18180L (+ 3.3-volt power; 1024 refresh cycles; self-refresh mode)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle (max)	Battery Backup Current (max)	Package
μPD42S18180LLE-A60	60 ns	40 ns	110 μA	42-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD42S18180LG5-A60	60 ns	40 ns	110 μA	50/44-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD42S18180LG5M-A60	60 ns	40 ns	110 μA	50/44-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to + 4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_{18}

Recommended Operating Conditions

		5-Volt Devices			3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		70	0		70	°C

Self-Refresh Current; 42S1x Devices

T_A = 0 to +70°C; V_{CC} = +5 V ±10% or +3.3 V ±0.3 V

Symbol	5-Volt Devices	3.3-Volt Devices	Conditions
I_{CC7}	200 μA max	80 μA max	I/O pins: $V_{IH} \geq V_{CC}$ −0.2 V; $V_{IL} \leq$ 0.2 V or open. Other input pins: $V_{IH} \geq V_{CC}$ −0.2 V; $V_{IL} \leq$ 0.2 V or open; $t_{RAS} \geq$ 100 μs

DC Characteristics; 5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				400	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

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DC Characteristics; 3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				400	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

DC Current Requirements; 5-Volt Devices

Parameter	Symbol	-50	-60	-70	-80	Unit	Test Conditions
Operating current	I_{CC1}						
4216/42S16		120	110	100	90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} (min); I_O = 0 mA
4217/42S17		140	130	120	110	mA	
4218/42S18		190	180	170	160	mA	
Refresh current ($\overline{RAS}$ only refresh)	I_{CC3}						
4216/42S16		120	110	100	90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} (min); t_{RC} = t_{RC} (min); I_O = 0 mA
4217/42S17		140	130	120	110	mA	
4218/42S18		190	180	170	160	mA	
Operating current (Fast-page mode)	I_{CC4}						
4216/42S16		100	90	80	70	mA	$\overline{CAS}$ cycling; $\overline{RAS}$ ≤ V_{IL} (max); t_{PC} = t_{PC} (min); I_O = 0 mA
4217/42S17		100	90	80	70	mA	
4218/42S18		100	90	80	70	mA	
Refresh current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}						
4216/42S16		120	110	100	90	mA	$\overline{RAS}$ cycling; t_{RC} = t_{RC} (min); I_O = 0 mA
4217/42S17		140	130	120	110	mA	
4218/42S18		190	180	170	160	mA	
Battery backup current (Standby with $\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RAS} ≤ 300 ns		t_{RAS} ≤ 1 μs			Standby: $\overline{RAS}$ ≥ V_{CC} – 0.2 V; $\overline{RAS}$, $\overline{CAS}$: 0 V ≤ V_{IL} ≤ 0.2 V, V_{CC} – 0.2 V ≤ V_{IH} ≤ V_{IH} (max); $\overline{WE}$, $\overline{OE}$: V_{IH}; Address: don't care; Output: open
42S16		350		500		μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 4096 cycles, 256 ms
42S17		300		400		μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 2048 cycles, 256 ms
42S18		250		300		μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 1024 cycles, 256 ms

DC Current Requirements; 3.3-Volt Devices

Parameter	Symbol	-A60	-A70	-A80	Unit	Test Conditions
Operating current	I_{CC1}					
4216/42S16		100	90	80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ (min); I_O = 0 mA
4217/42S17		120	110	100	mA	
4218/42S18		170	160	150	mA	
Refresh current ($\overline{RAS}$ only refresh)	I_{CC3}					
4216/42S16		100	90	80	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$ (min); $t_{RC} = t_{RC}$ (min); I_O = 0 mA
4217/42S17		120	110	100	mA	
4218/42S18		170	160	150	mA	
Operating current (Fast-page mode)	I_{CC4}					
4216/42S16		80	70	60	mA	$\overline{CAS}$ cycling; $\overline{RAS} \leq V_{IL}$ (max); $t_{PC} = t_{PC}$ (min); I_O = 0 mA
4217/42S17		80	70	60	mA	
4218/42S18		80	70	60	mA	
Refresh current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}					
4216/42S16		100	90	80	mA	$\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ (min); I_O = 0 mA
4217/42S17		120	110	100	mA	
4218/42S18		170	160	150	mA	
Battery backup current (Standby with $\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$t_{RAS} \leq 300$ ns		$t_{RAS} \leq 1$ μs		Standby: $\overline{RAS} \geq V_{CC} - 0.2$ V; $\overline{RAS}$, $\overline{CAS}$: 0 V ≤ V_{IL} ≤ 0.2 V, $V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH}$ (max); $\overline{WE}$, $\overline{OE}$: V_{IH}; Address: don't care; Output: open
42S16		140		140	μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 4096 cycles, 256 ms
42S17		120		120	μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 2048 cycles, 256 ms
42S18		110		110	μA	$\overline{CAS}$ before $\overline{RAS}$ refresh: 1024 cycles, 256 ms

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10% (-50, -60, -70, -80) or +3.3 V ±0.3 V (-A60, -A70, -A80)

		-50		-60, -A60		-70, -A70		-80, -A80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Access time from column address	t_{AA}		25		30		35		40	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		30		35		40		45	ns	(Note 7)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	45		53		60		65		ns	(Note 15)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		13		15		18		20	ns	(Notes 7, 8)
Column address hold time	t_{CAH}	13		15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	10		10		10		10		ns	
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	−50		−50		−50		−50		ns	(Note 16)
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		0		ns	(Note 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	8		10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	8		10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		65		70		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		5		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	33		38		43		45		ns	(Note 15)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	13		15		15		15		ns	
Data-in hold time	t_{DH}	10		10		15		15		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 13)
Masked write hold time referenced to $\overline{RAS}$	t_{MRH}	0		0		0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		13		15		18		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	10		13		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	0	15	ns	(Note 9)

AC Characteristics (cont)

Parameter	Symbol	-50		-60, -A60		-70, -A70		-80, -A80		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Output disable from $\overline{CAS}$ high	t_{OFF}	0	10	0	13	0	15	0	15	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		0		ns	(Note 7)
Fast-page read or write cycle time	t_{PC}	35		40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with extended data output	t_{PRWC}	80		85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	15	35	17	40	ns	(Note 8)
Row address hold time	t_{RAH}	8		10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	25		30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		100		μs	(Note 16)
Random read or write cycle time	t_{RC}	90		110		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	20	45	20	50	25	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}										
4216			64		64		64		64	ms	
4217			32		32		32		32	ms	
4218			16		16		16		16	ms	
42S16			256		256		256		256	ms	
42S17			256		256		256		256	ms	
42S18			256		256		256		256	ms	
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	30		35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5		5		5		5		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	90		110		130		150		ns	(Note 16)
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	13		15		18		20		ns	
Read-modify-write cycle time	t_{RWC}	140		160		180		200		ns	(Note 6)

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AC Characteristics (cont)

Parameter	Symbol	-50 Min	-50 Max	-60, -A60 Min	-60, -A60 Max	-70, -A70 Min	-70, -A70 Max	-80, -A80 Min	-80, -A80 Max	Unit	Test Conditions
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	70		83		95		105		ns	(Note 15)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	18		20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	
Write command hold time	t_{WCH}	8		10		10		15		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 14)
Write command pulse width	t_{WP}	8		10		10		15		ns	(Note 12)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by eight refresh cycles ($\overline{RAS}$ only or CBR) before proper device operation is achieved.

(3) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(4) Ac measurements assume t_T = 5 ns.

(5) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max).
If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a late write cycle. For early write cycles, t_{WCH} must be met.

(13) These parameters are referenced to the leading edge of $\overline{CAS}$ in early write cycles and to the leading edge of $\overline{WE}$ in late write or read-modify-write cycles.

(14) If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle.

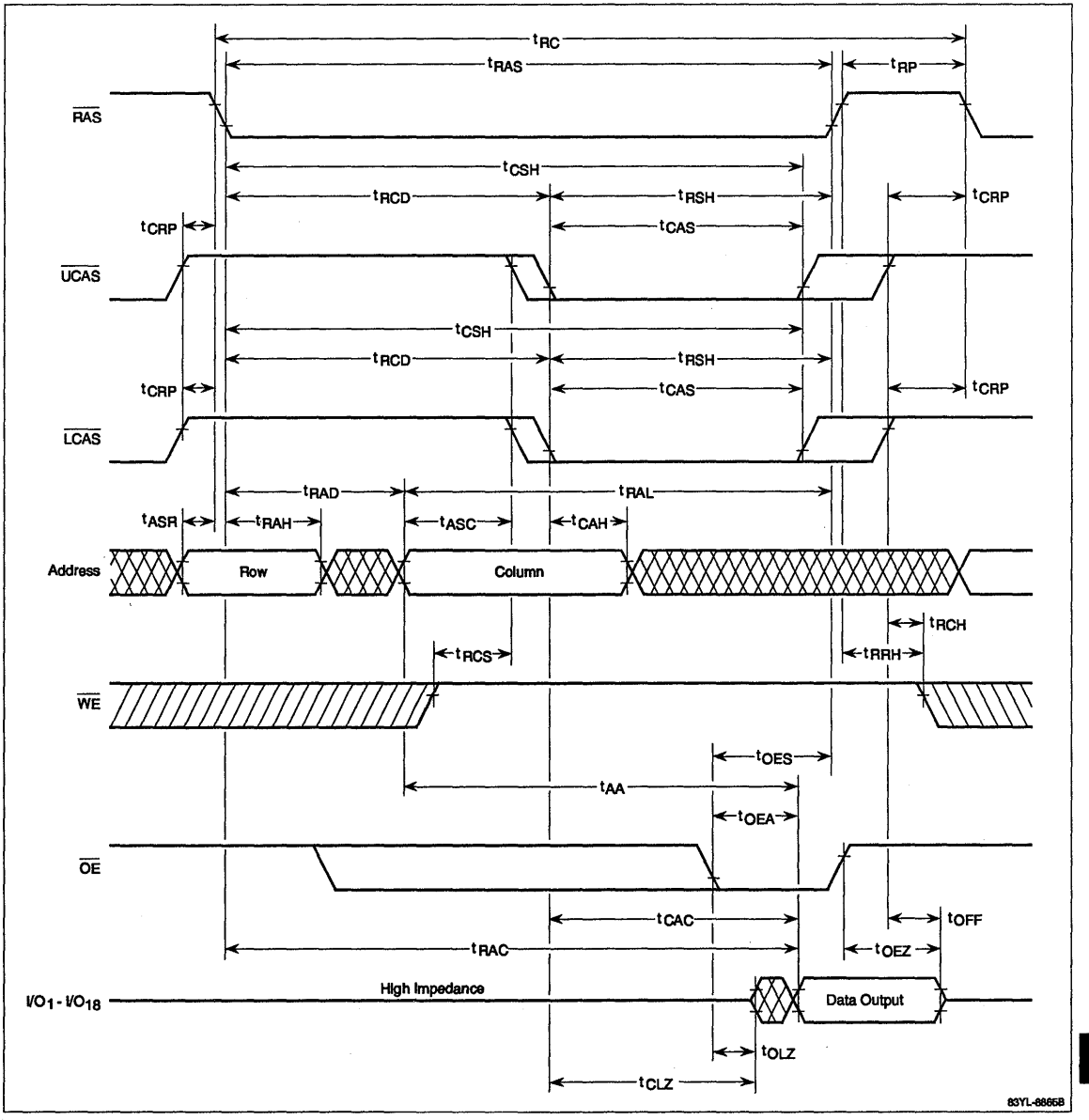
(15) If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(16) Parameter is applicable only to self-refresh versions.

(17) With burst CBR, $\overline{RAS}$ only, or external $\overline{RAS}$/$\overline{CAS}$, all addresses must be refreshed before entering self-refresh mode and after exiting.

Timing Waveforms

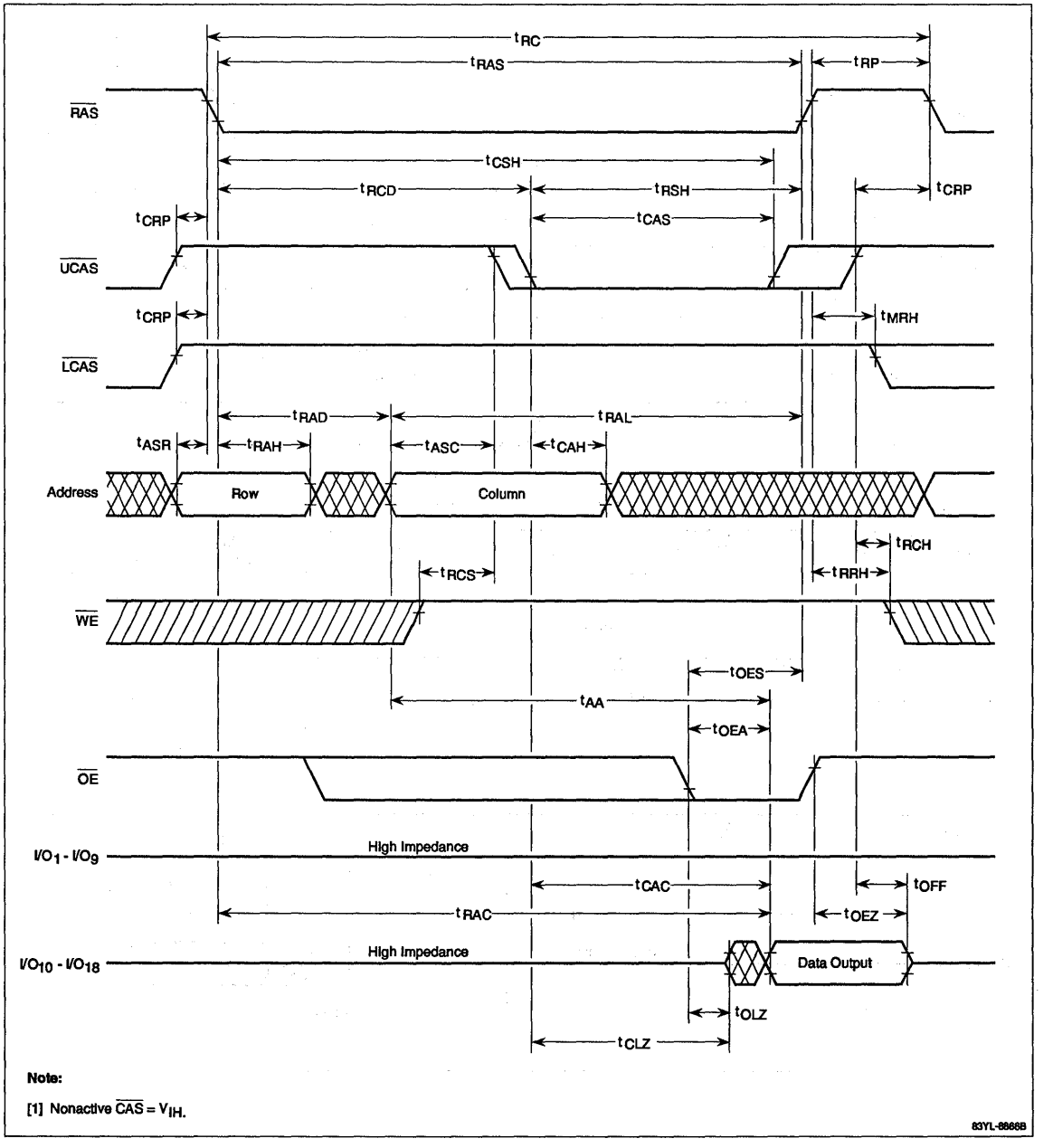
Word Read Cycle



8m

Timing Waveforms (cont)

Byte Read Cycle



Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

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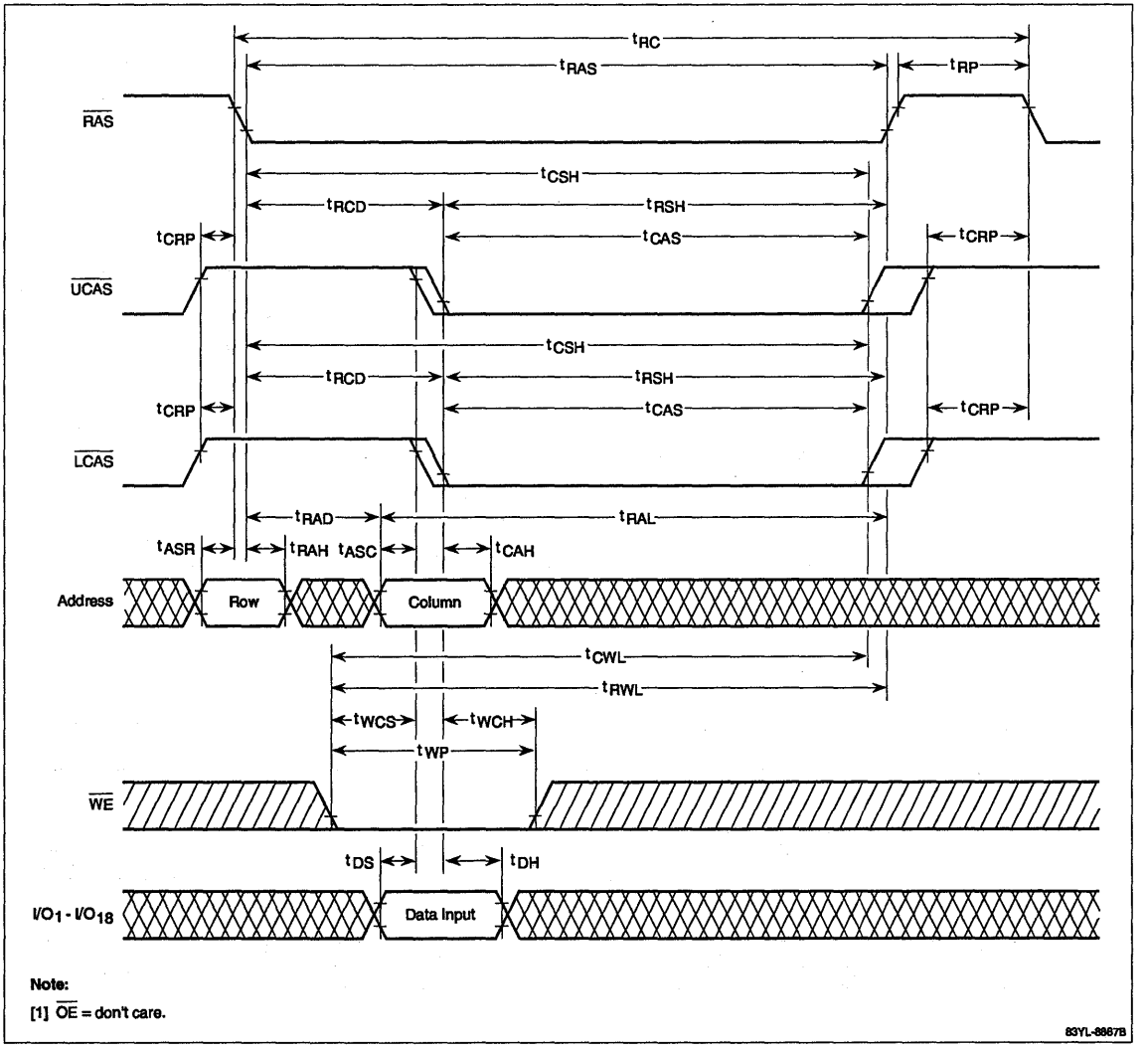
Timing Waveforms (cont)

Word Early-Write Cycle



Note:

[1] $\overline{OE}$ = don't care.

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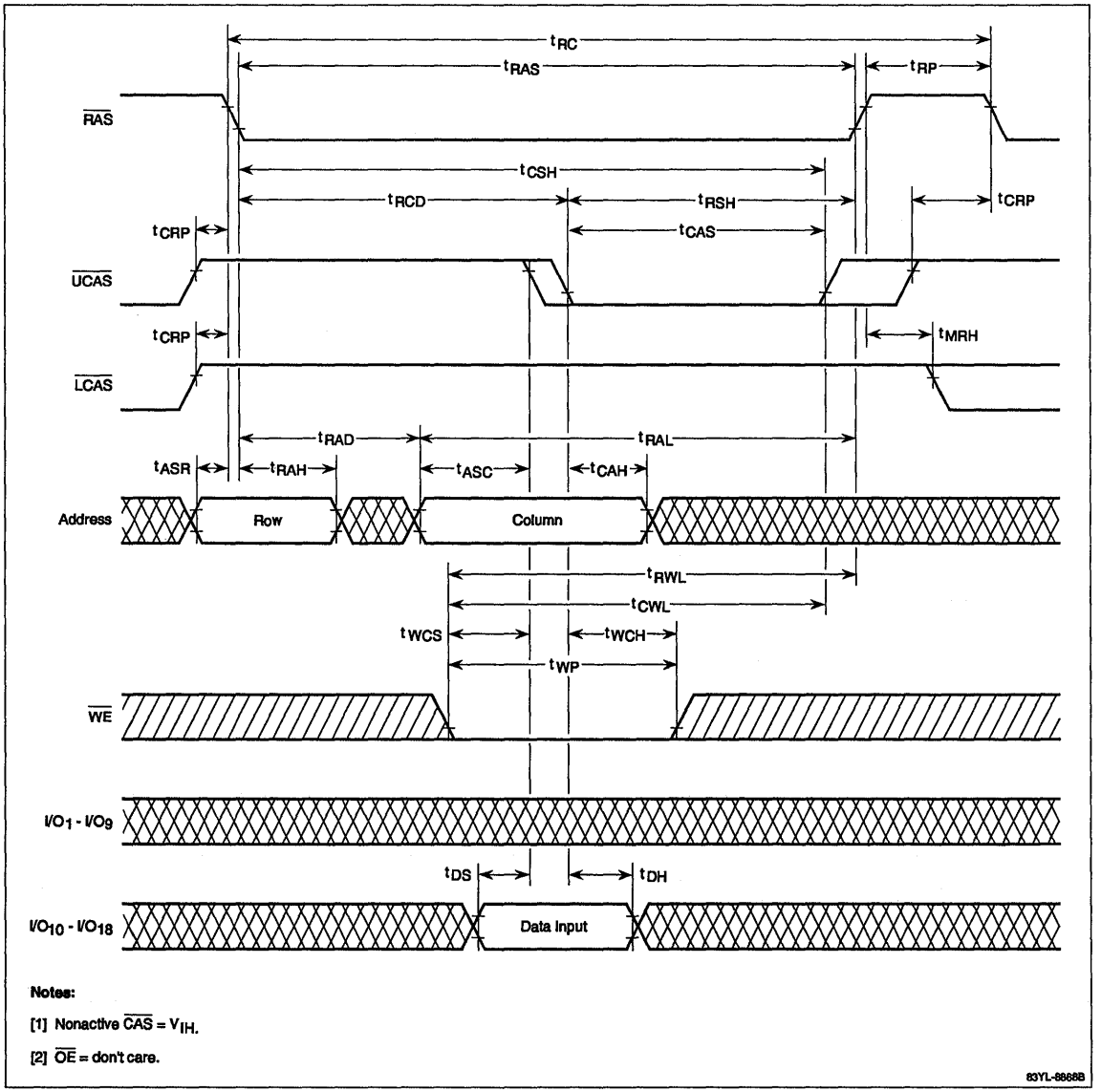
8m

Timing Waveforms (cont)

Byte Early-Write Cycle



Notes:

[1] Nonactive $\overline{CAS} = V_{IH}$.

[2] $\overline{OE}$ = don't care.

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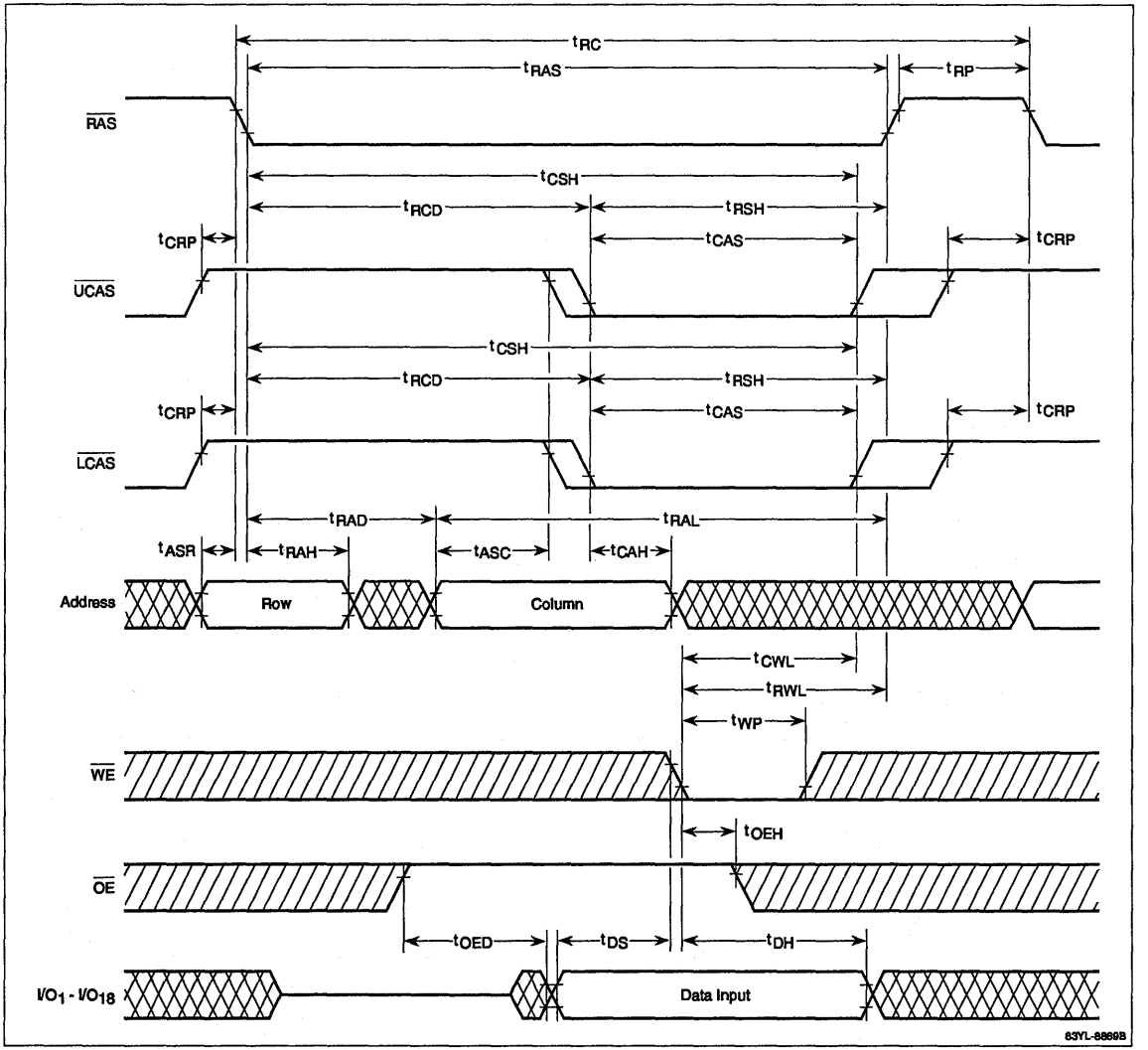
Timing Waveforms (cont)

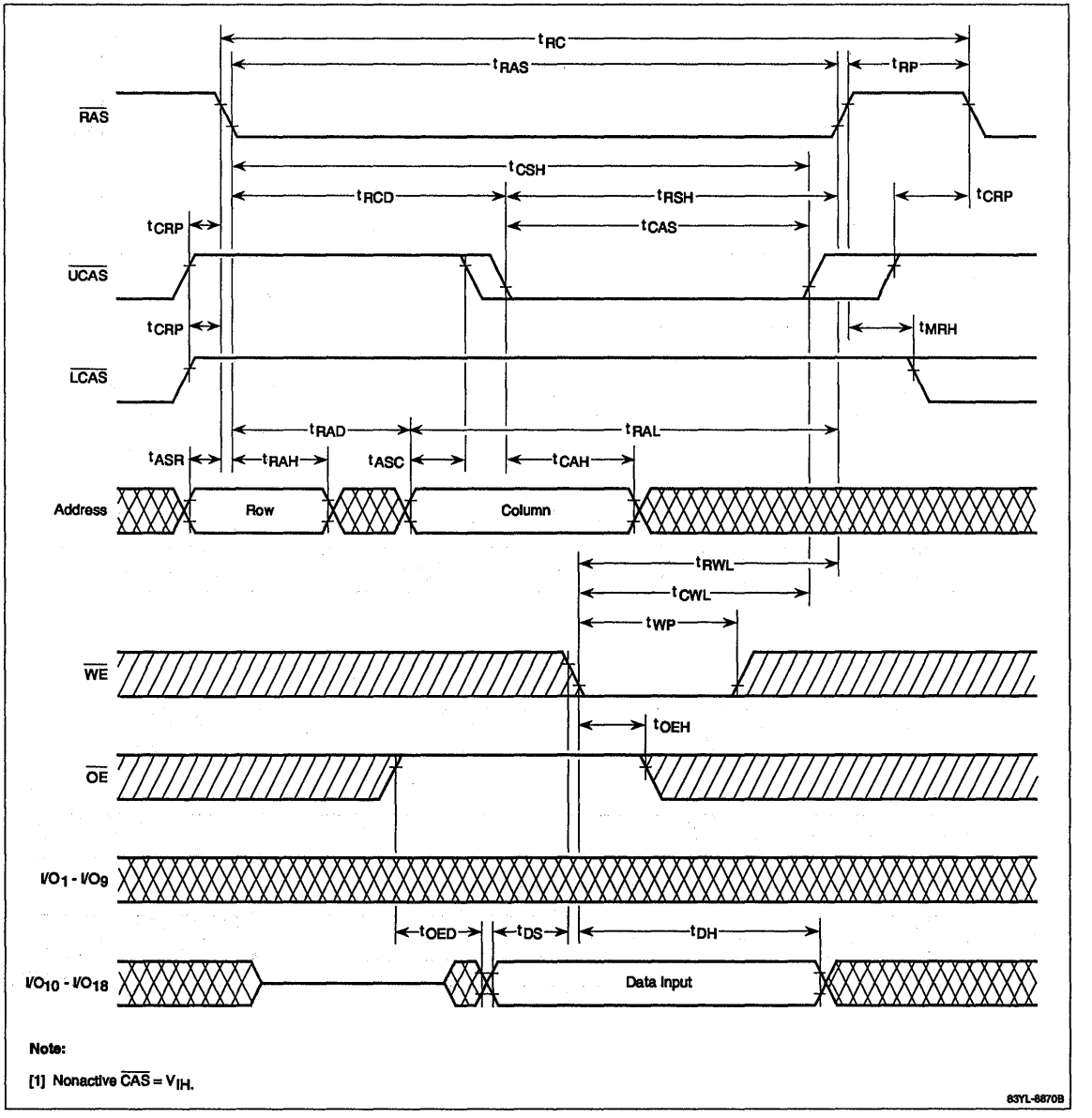
Word Late-Write Cycle



8m

Timing Waveforms (cont)

Byte Late-Write Cycle



Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

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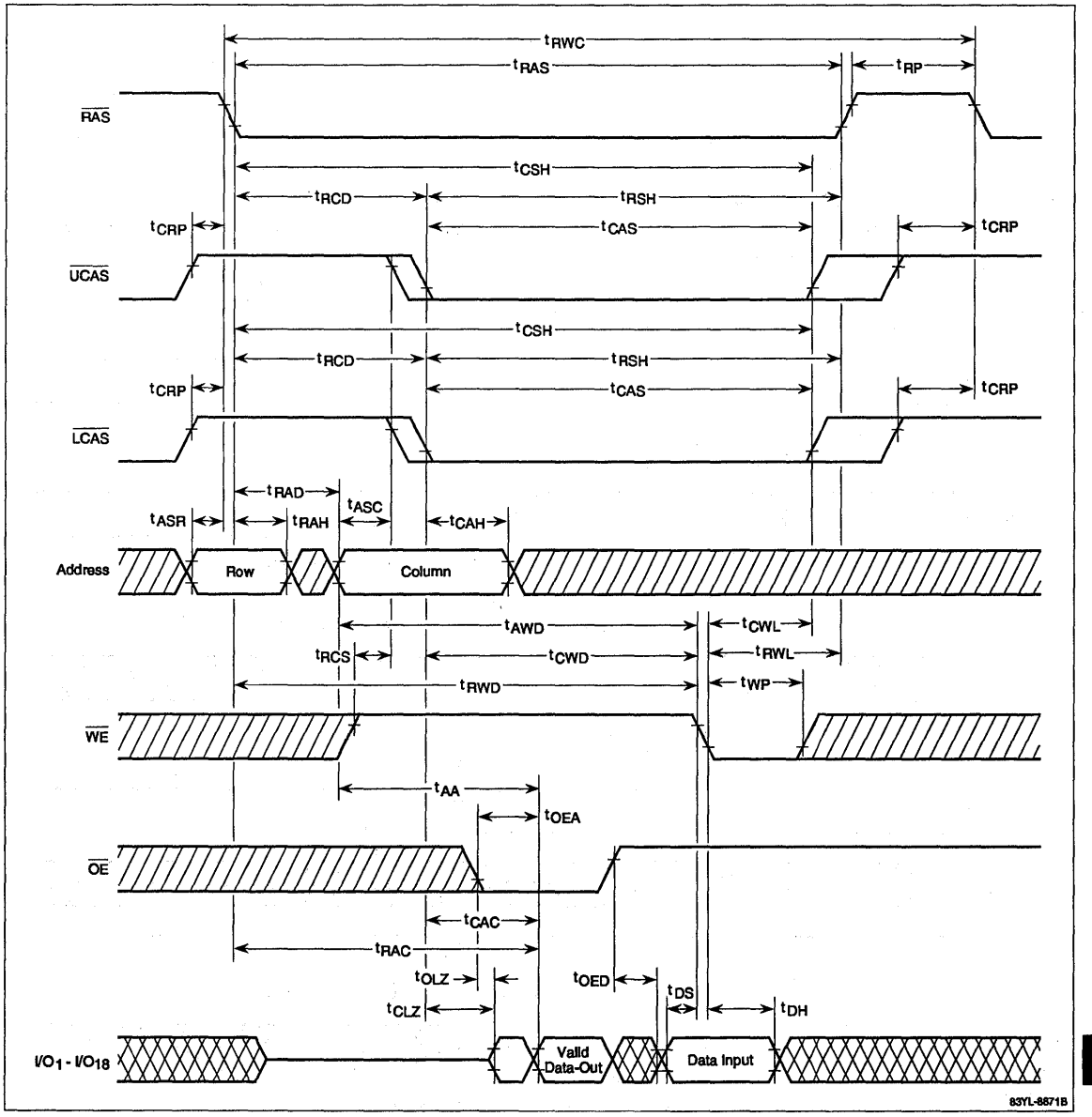
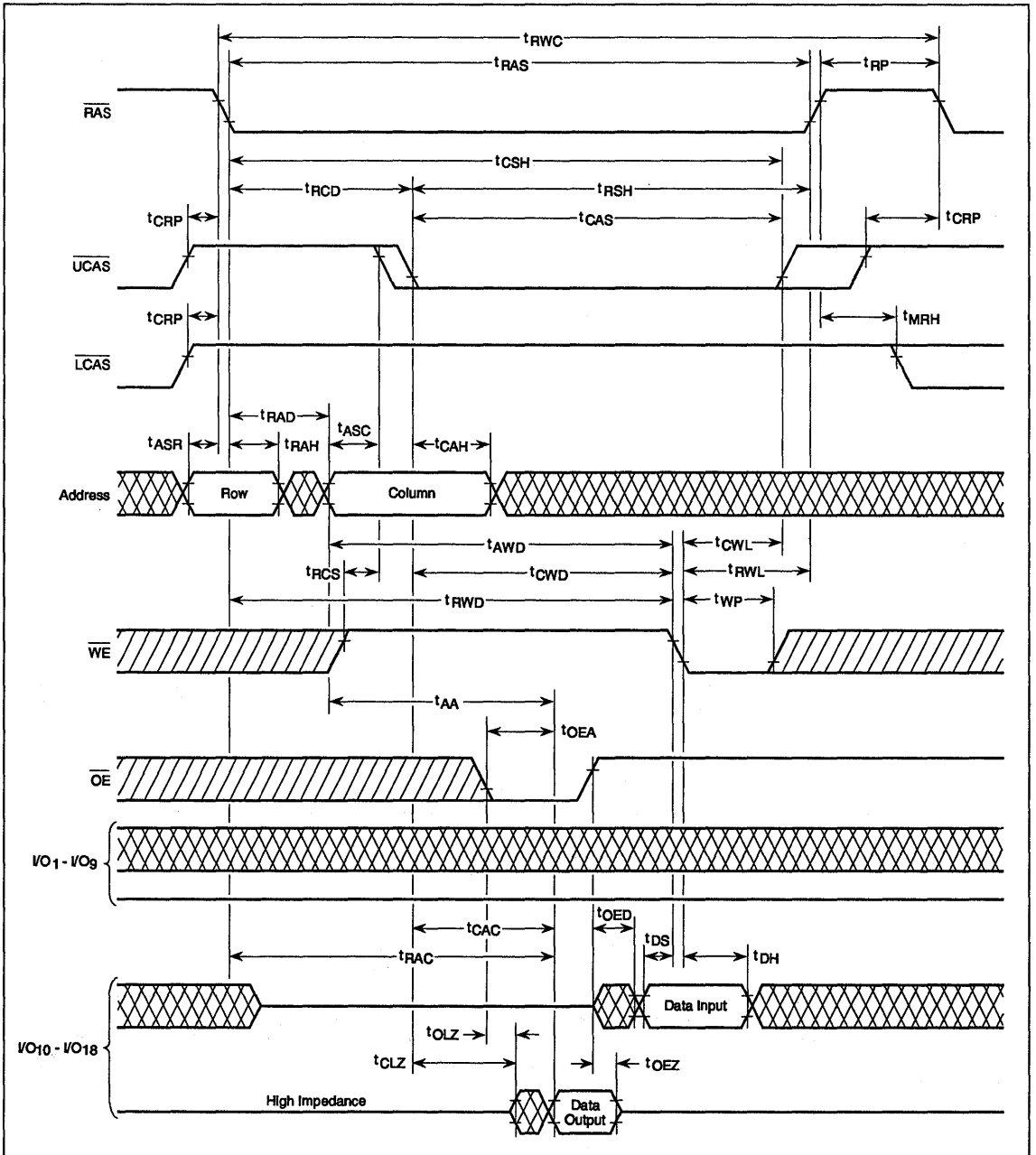
Timing Waveforms (cont)

Word Read-Modify-Write Cycle



Timing Waveforms (cont)

Byte Read-Modify-Write Cycle



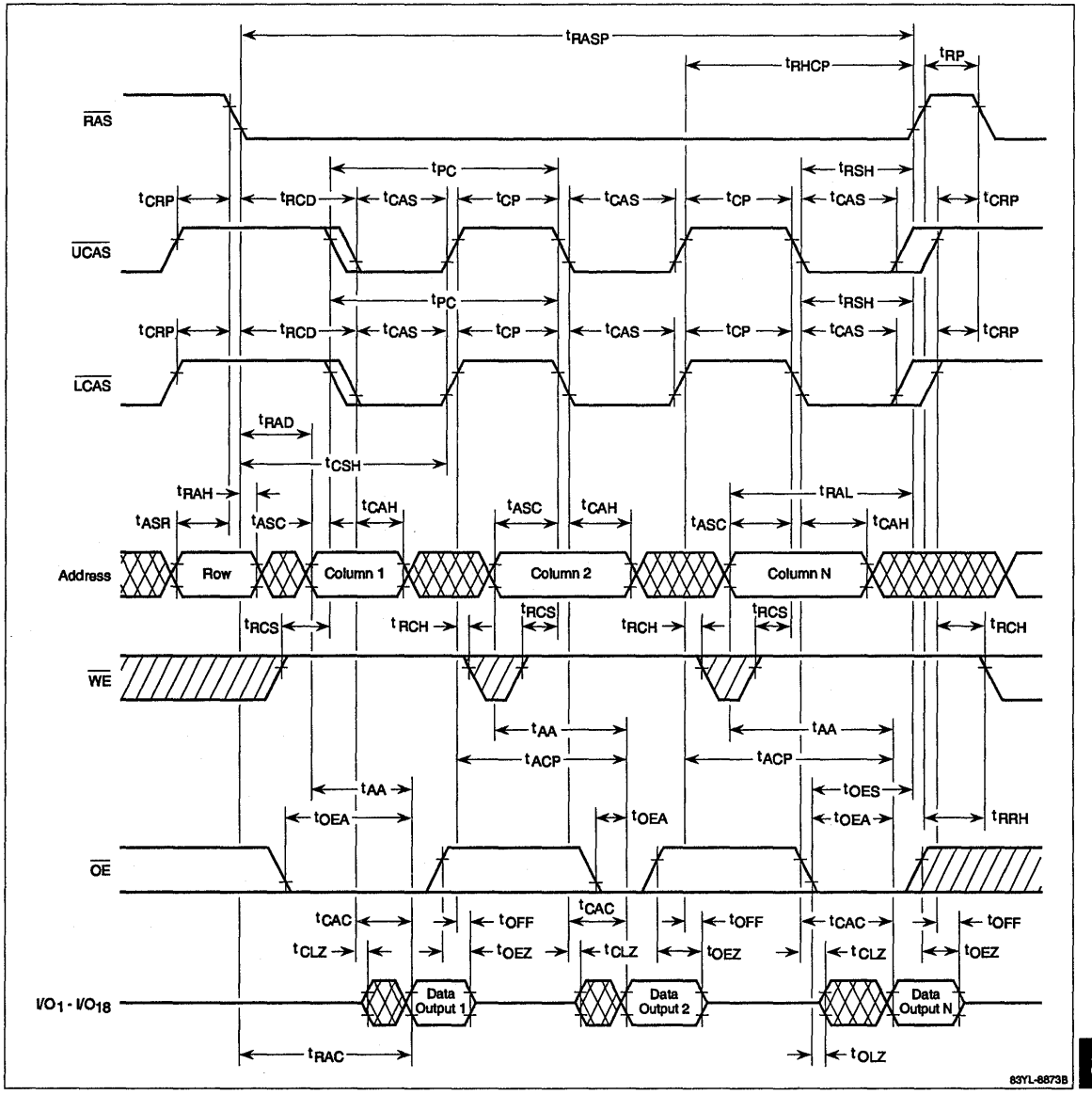
Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-8872B

Timing Waveforms (cont)

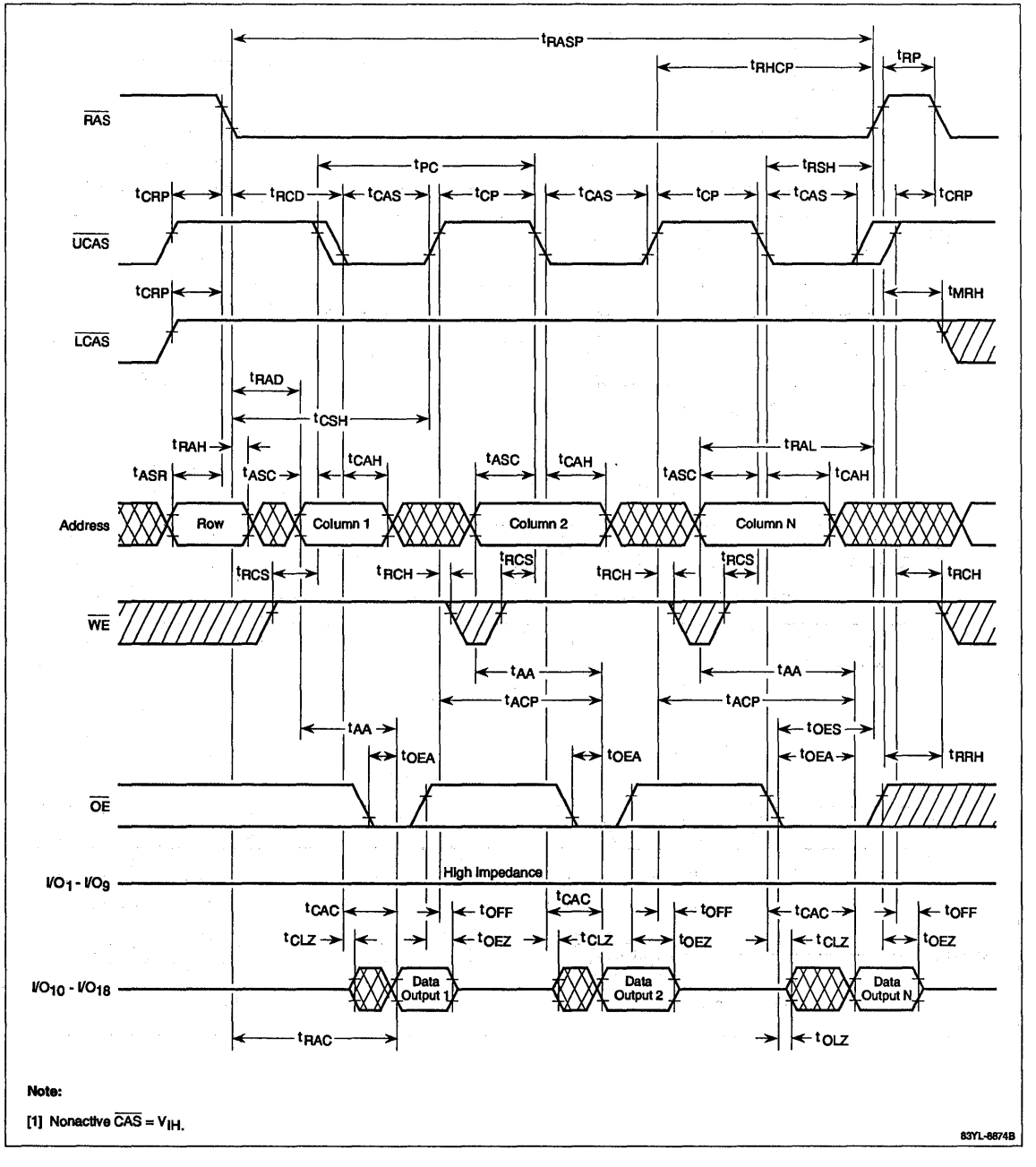
Word Fast-Page Read Cycle



8m

Timing Waveforms (cont)

Byte Fast-Page Read Cycle



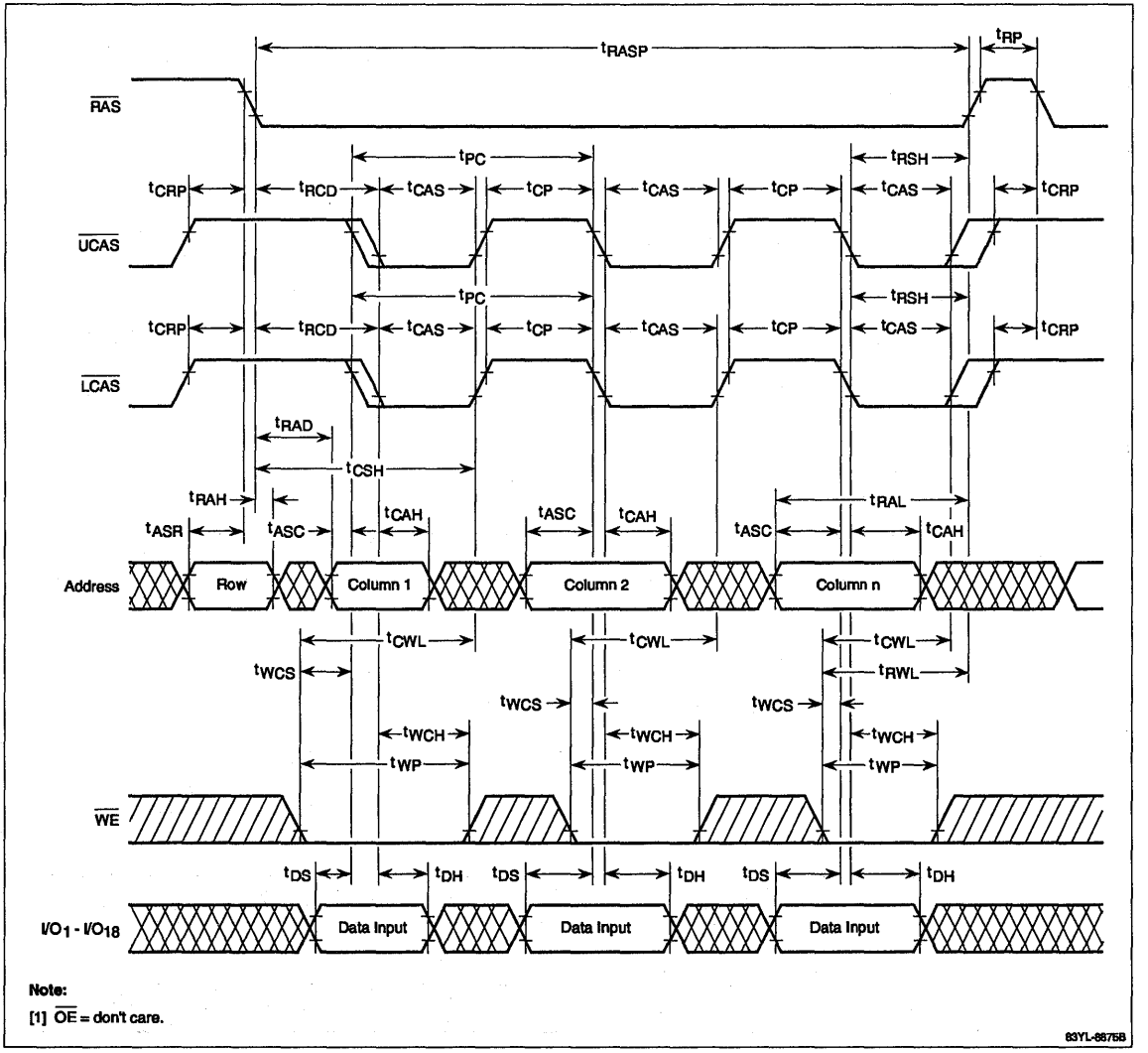
Note:

[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-8874B

Timing Waveforms (cont)

Word Fast-Page Early-Write Cycle



Note:

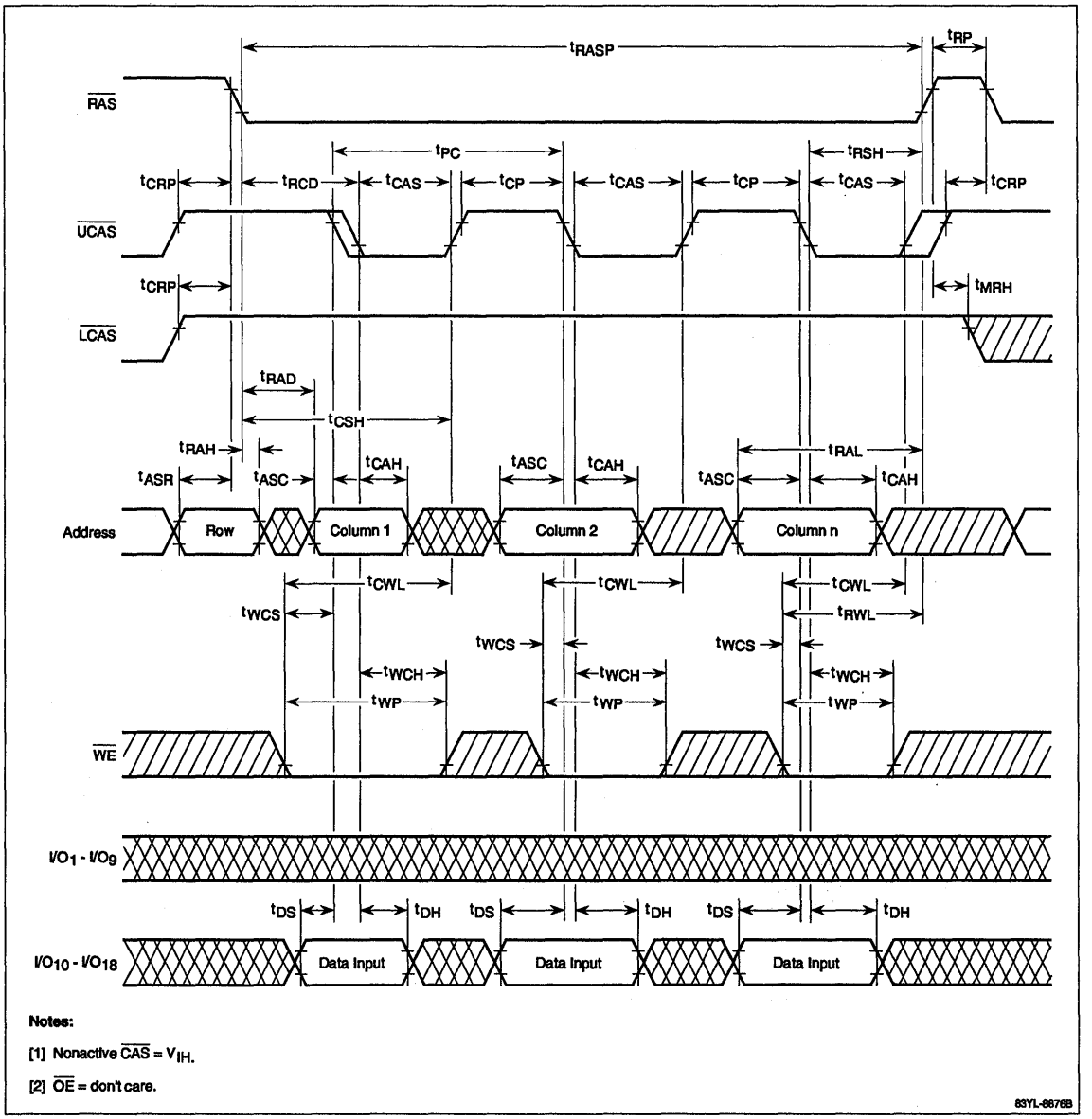
[1] $\overline{OE}$ = don't care.

83YL-8875B

8m

Timing Waveforms (cont)

Byte Fast-Page Early-Write Cycle



Notes:

[1] Nonactive $\overline{CAS} = V_{IH}$.

[2] $\overline{OE}$ = don't care.

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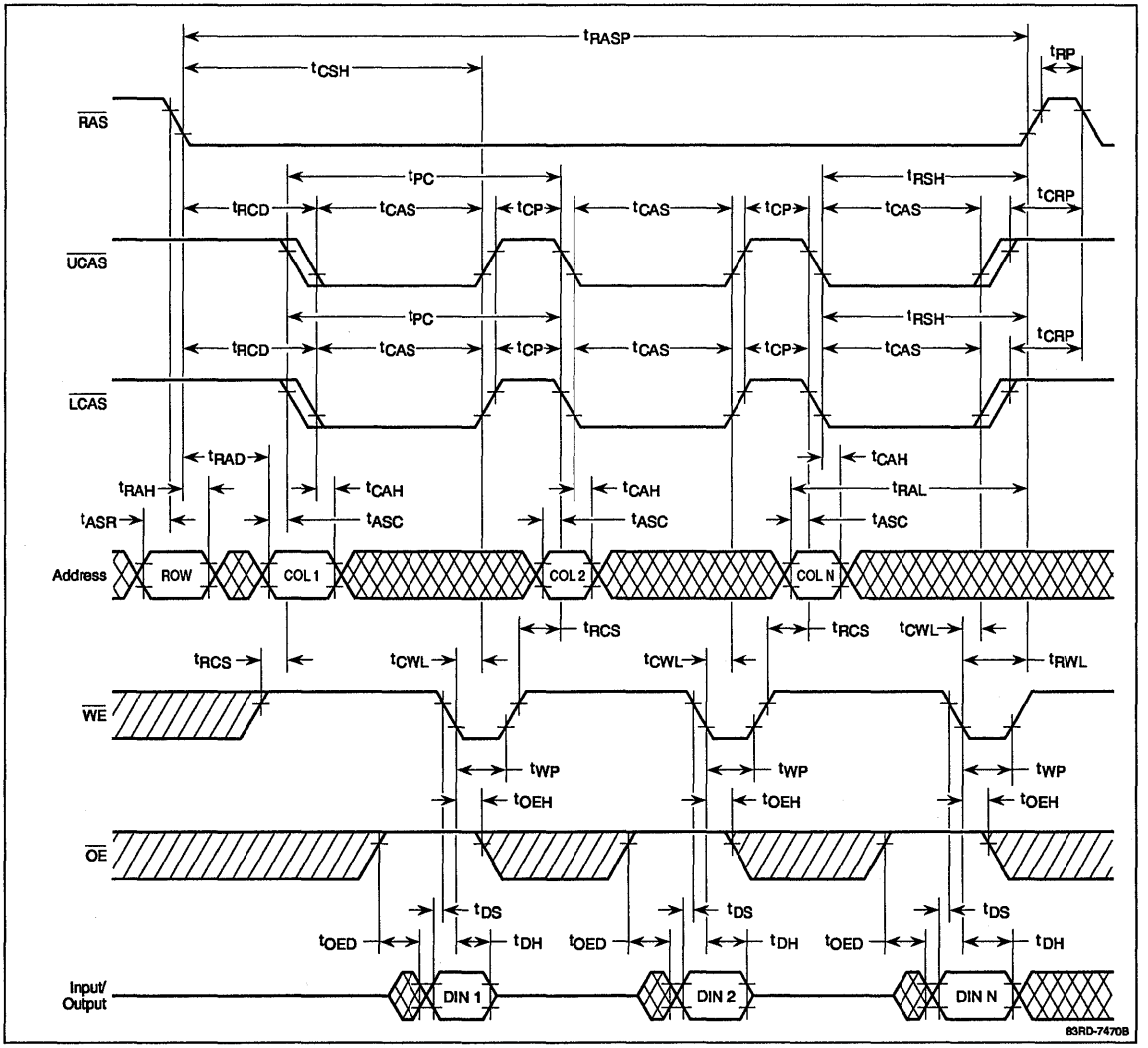
Timing Waveforms (cont)

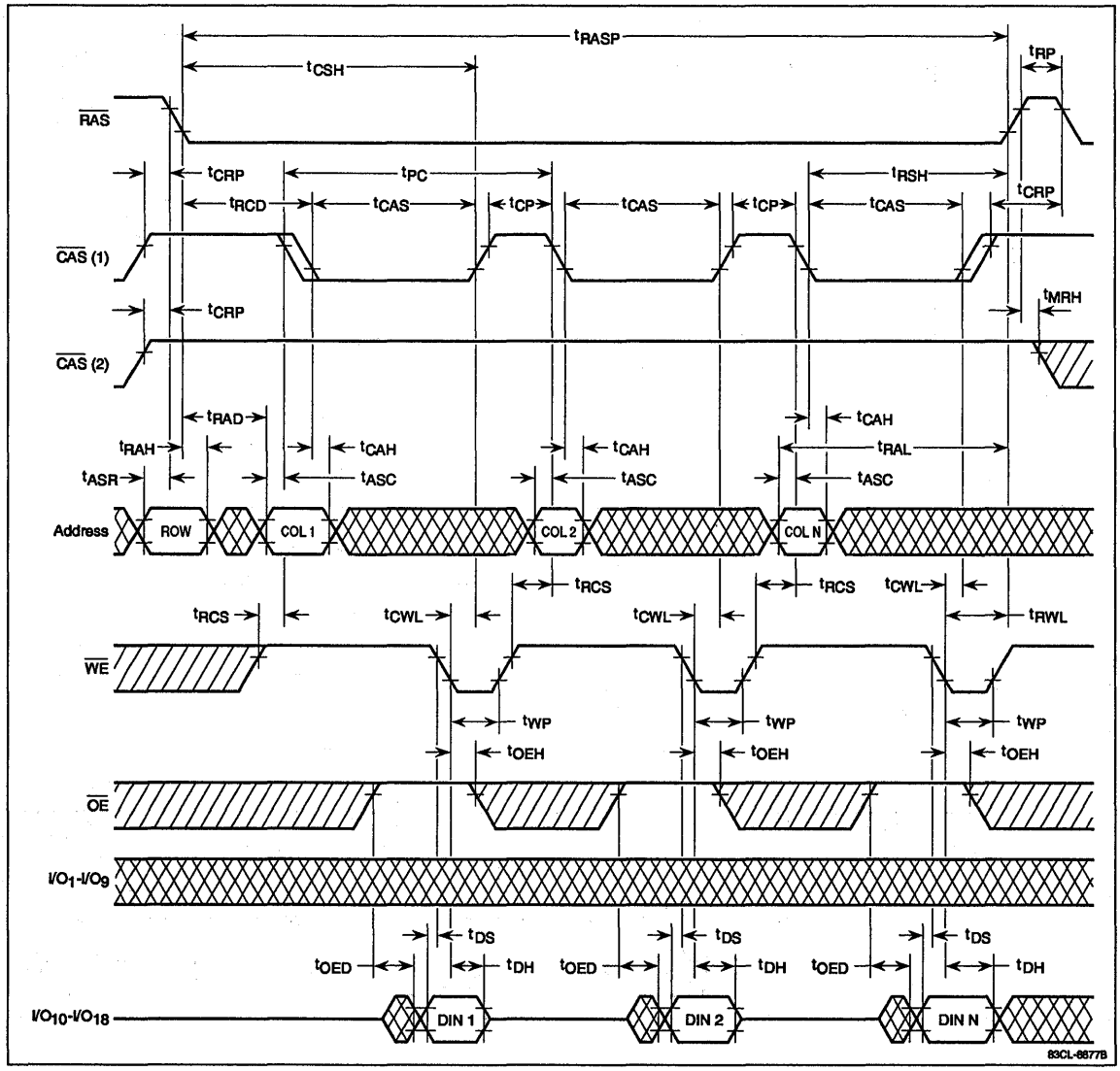
Word Fast-Page Late-Write Cycle



8m

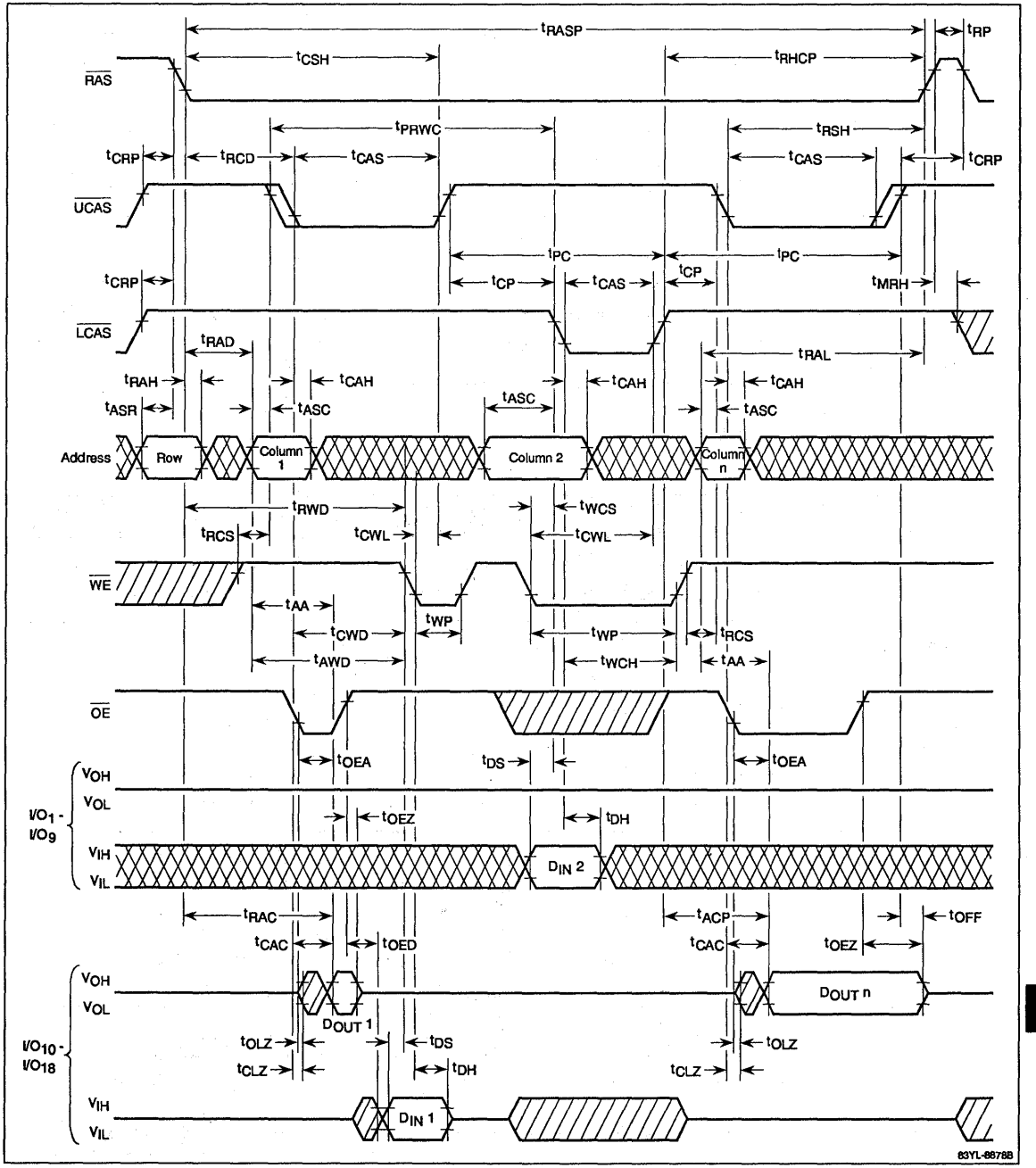
Timing Waveforms (cont)

Byte Fast-Page Late-Write Cycle



Timing Waveforms (cont)

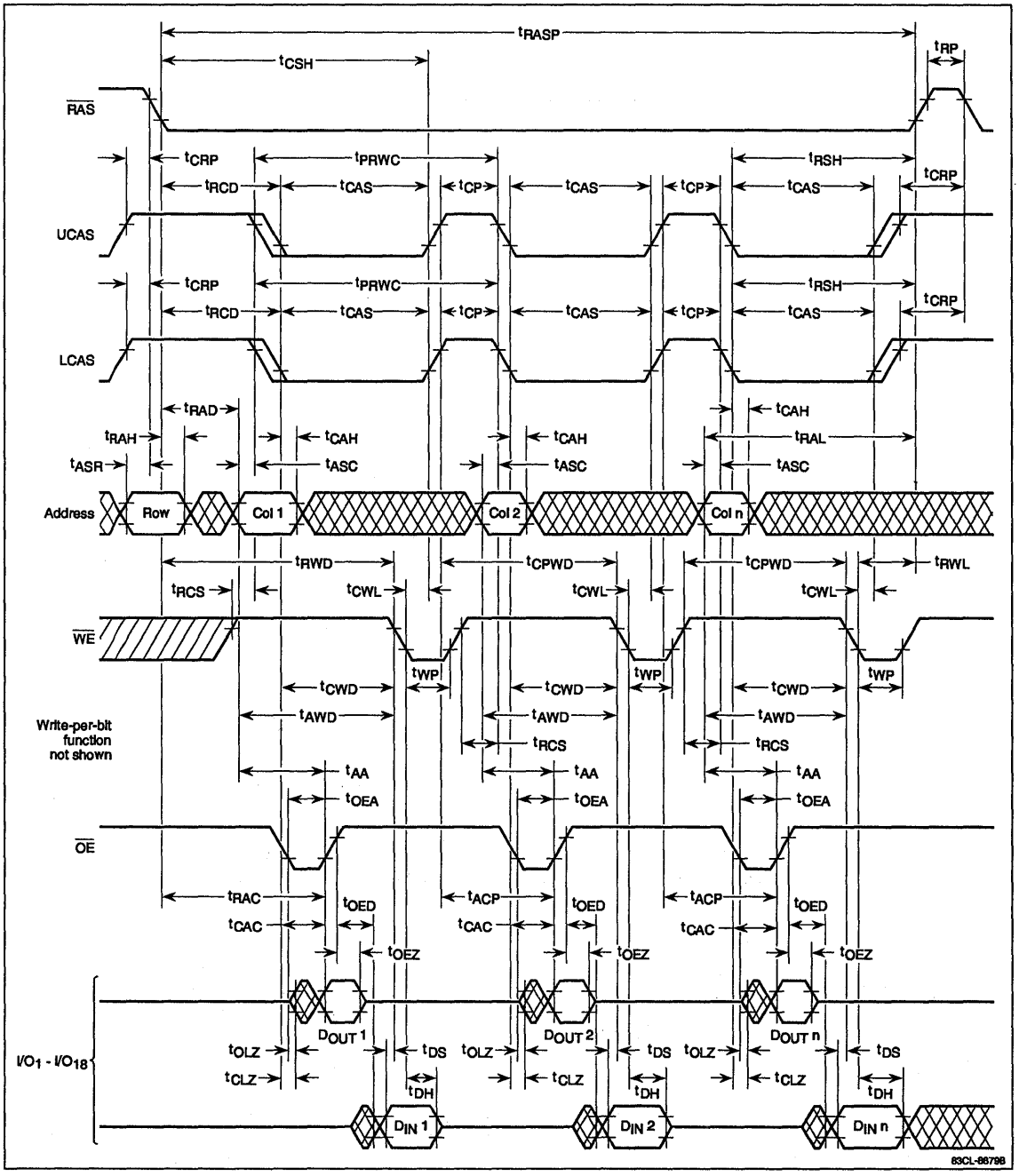
Byte Fast-Page Read/Write Cycle



8m

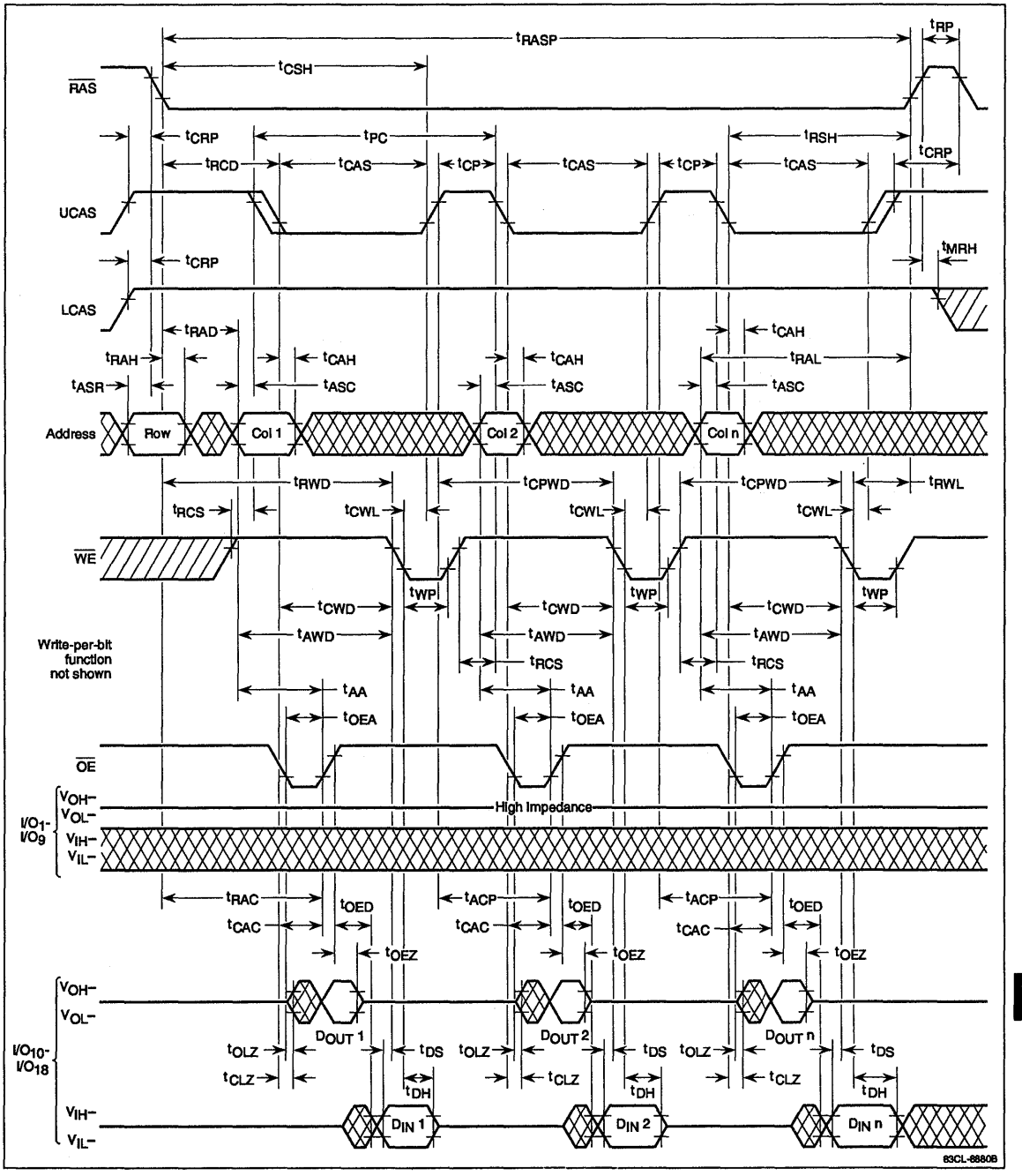
Timing Waveforms (cont)

Word Fast-Page Read-Modify-Write Cycle



Timing Waveforms (cont)

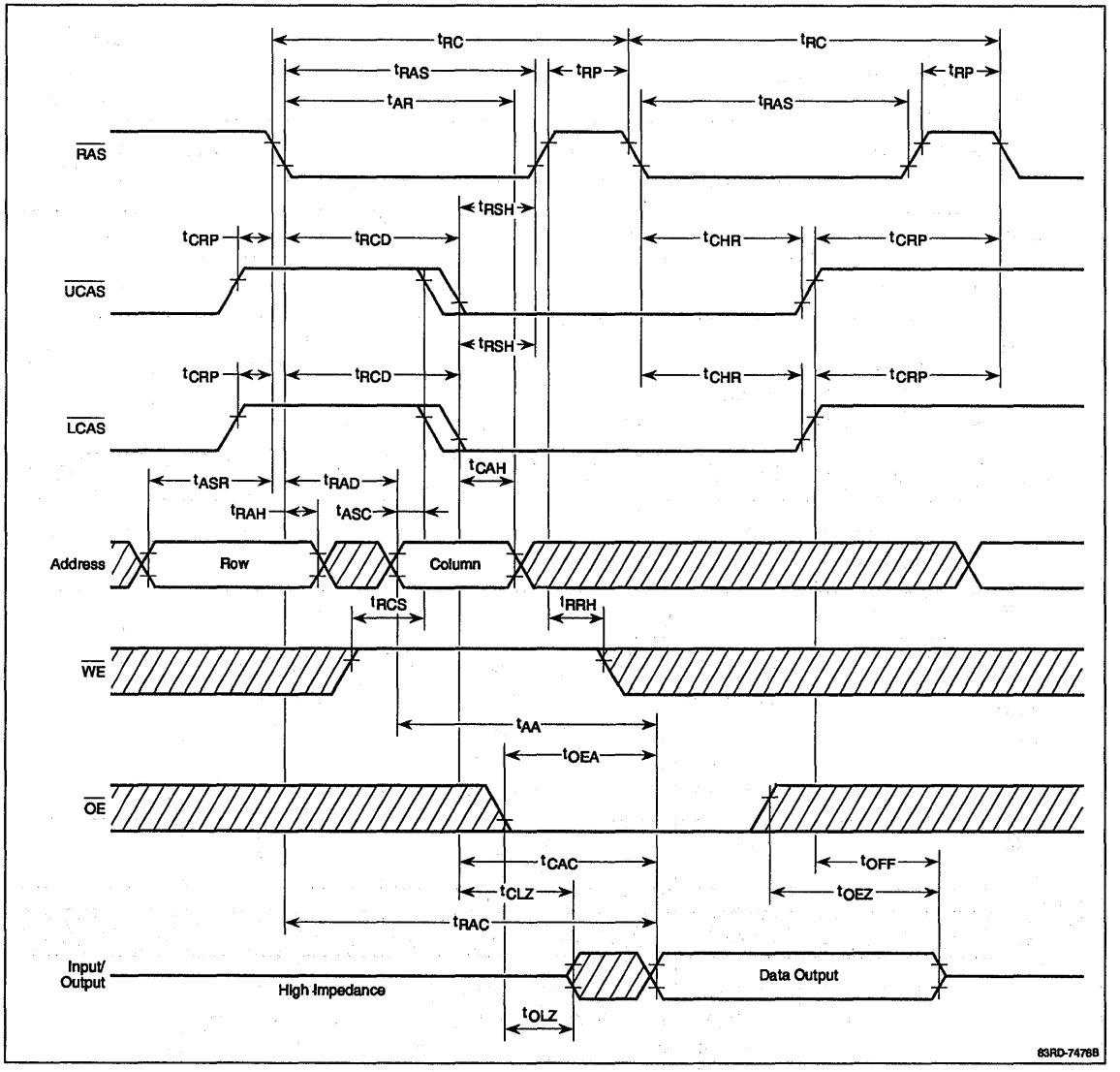
Byte Fast-Page Read-Modify-Write Cycle



8m

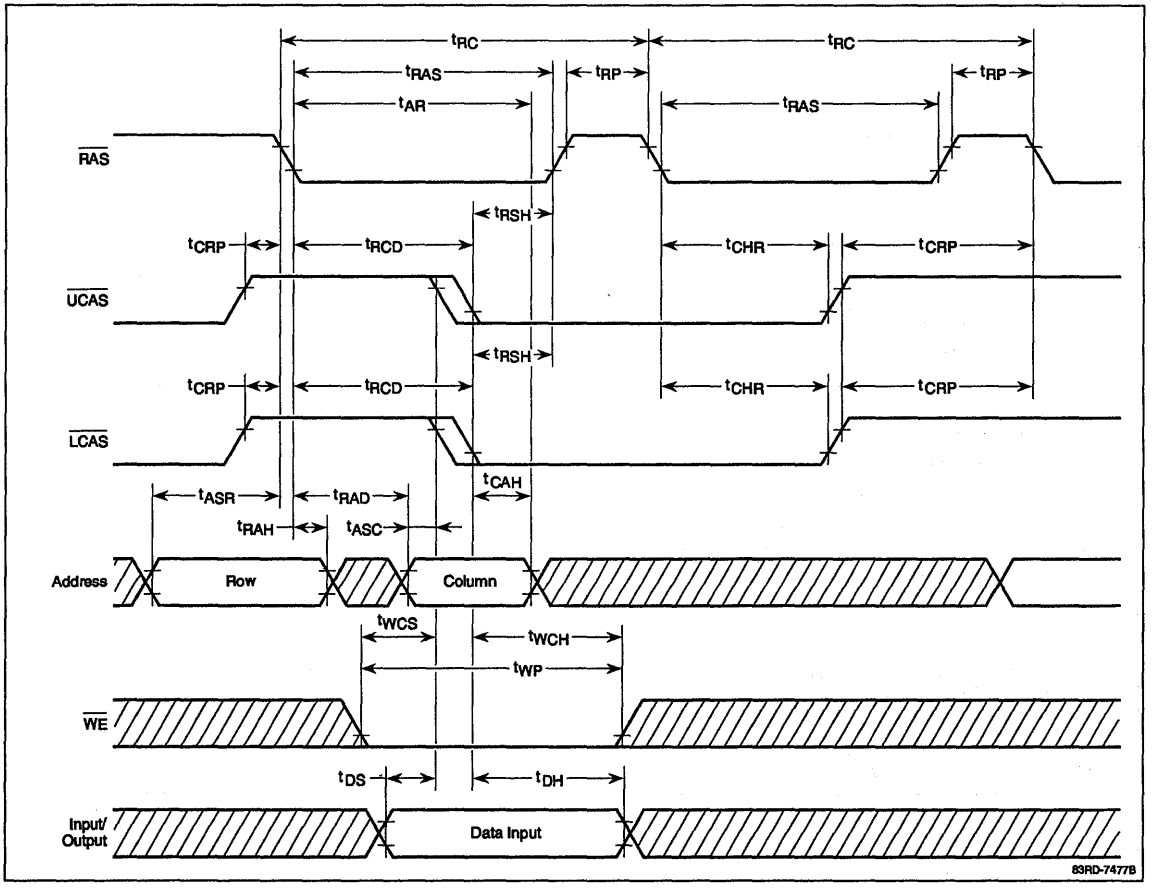
Timing Waveforms (cont)

Hidden-Refresh Cycle (Word Read Cycle)



Timing Waveforms (cont)

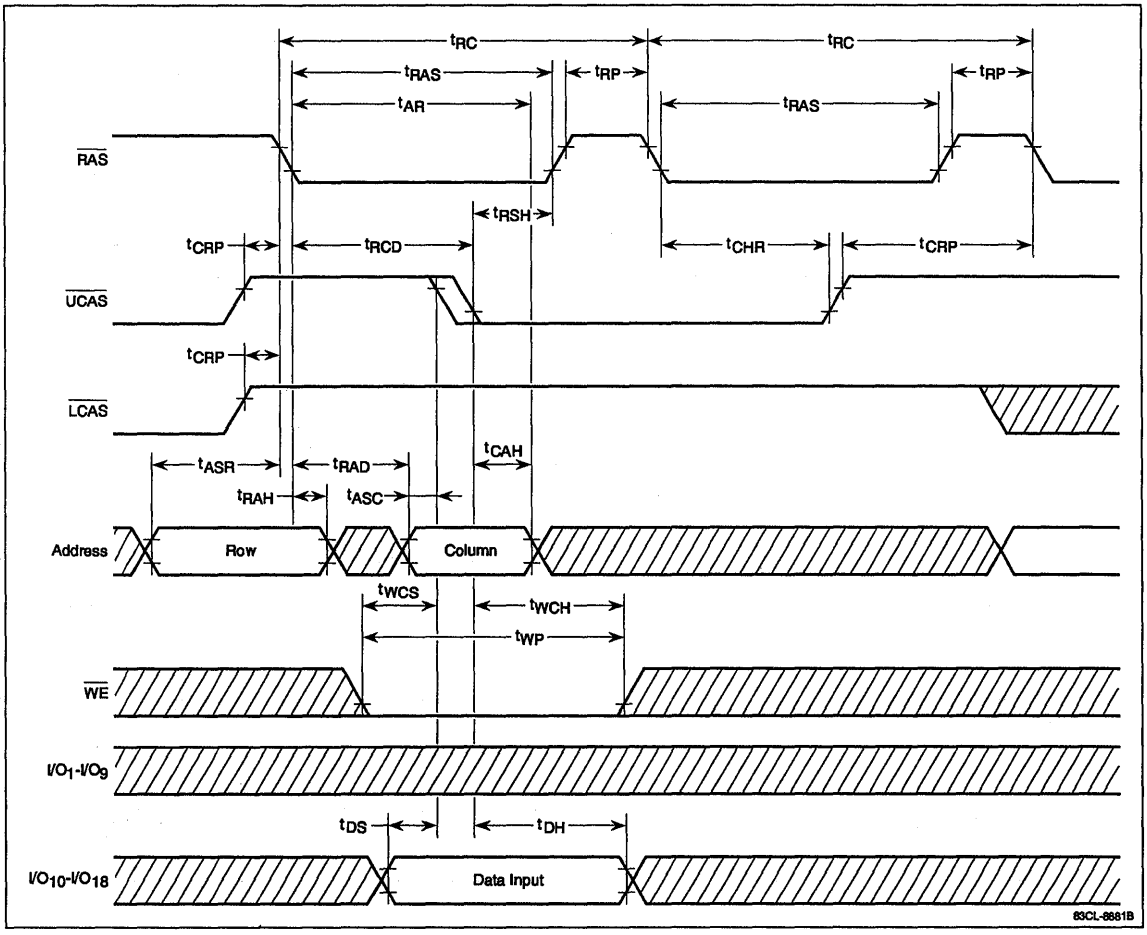
Hidden-Refresh Cycle (Word Write Cycle)



8m

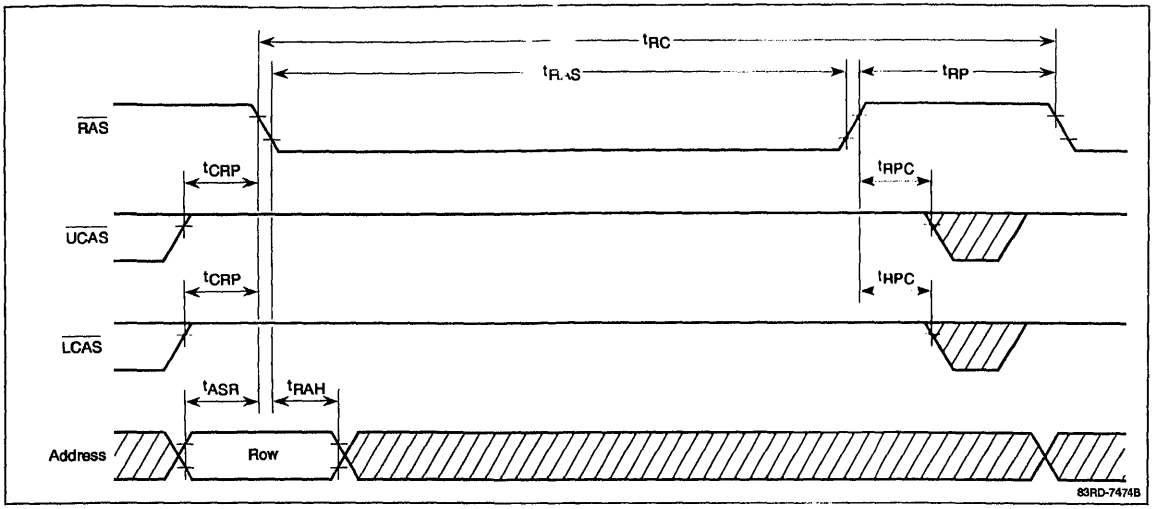
Timing Waveforms (cont)

Hidden-Refresh Cycle (Byte Write Cycle)

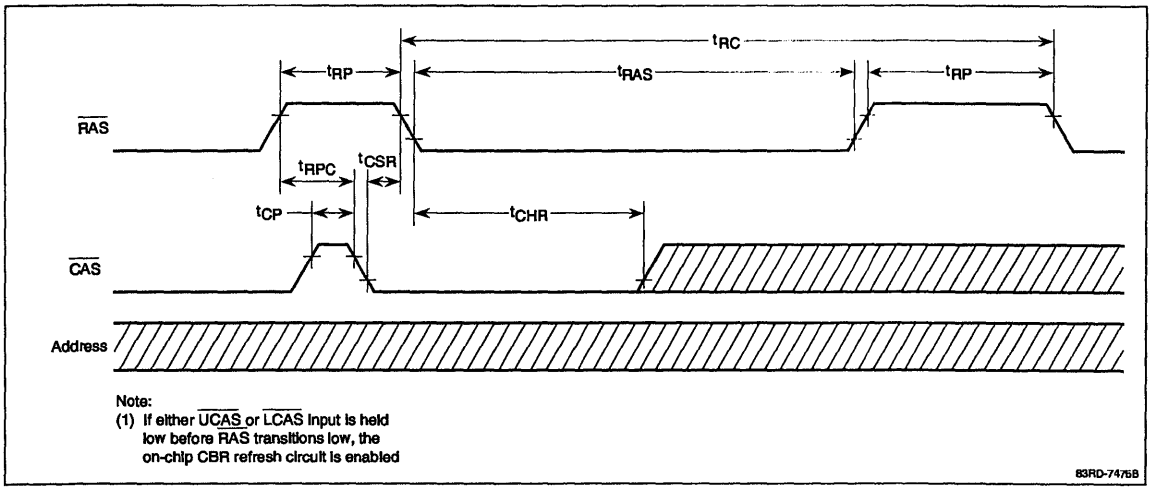


...ing Waveforms (cont)

RAS-Only Refresh Cycle



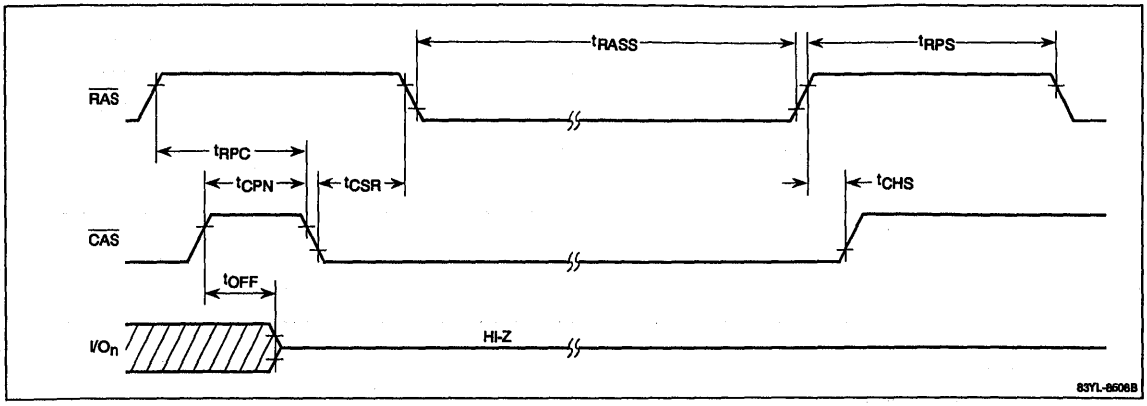
CAS Before RAS Refresh Cycle



8m

Timing Waveforms (cont)

CBR Self-Refresh Cycle



NEC

Section 9
DRAM Modules (256K/512K x n)

MC	Organization	Features	
-42256AB8	256K x 8	Fast-page	9a
-42256AB9	256K x 9	Fast-page	9b
-42256A32	256K x 32	Fast-page	9c
-42256A36	256K x 36	Fast-page	9d
-42256AA40	256K x 40	Fast-page	9e
-42512A32	512K x 32	Fast-page	9f
-42512A36	512K x 36	Fast-page	9g
-42512AA40, -42512AB40	512K x 40	Fast-page	9h

NEC Electronics Inc.

MC-42256AB8
262,144 x 8-Bit
Dynamic CMOS RAM Module

9a

Description

The MC-42256AB8 is a 262,144-word by 8-bit DRAM module designed to operate from a single +5-volt power supply. The module is a 30-pin socket-mountable Single Inline Memory Module (SIMM™) containing two μPD424256LA DRAMs (256K x 4).

The MC-42256AB8 is functionally equivalent to eight μPD42256 standard 256K x 1 DRAMs. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 - A_8 during a 4-ms period.

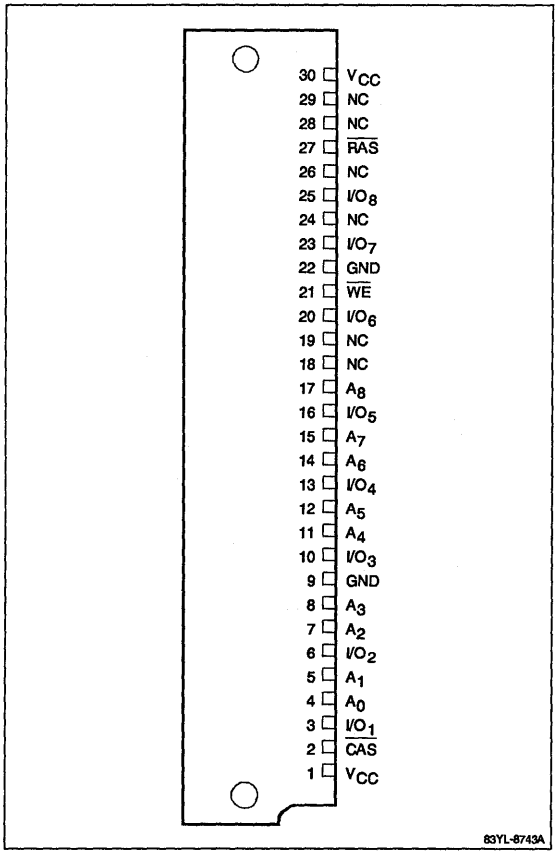
Features

- 262,144-word by 8-bit organization
- Single +5-volt power supply
- Standard 30-pin SIMM packaging
- Two 256K x 4 DRAMs
- Two power supply decoupling capacitors
- Low power dissipation of 16.5 mW max (standby)
- TTL-compatible inputs and outputs
- 256 refresh cycles every 4 ms
- Fast-page mode capability

SIMM is a trademark of Wang Laboratories.

Pin Configurations

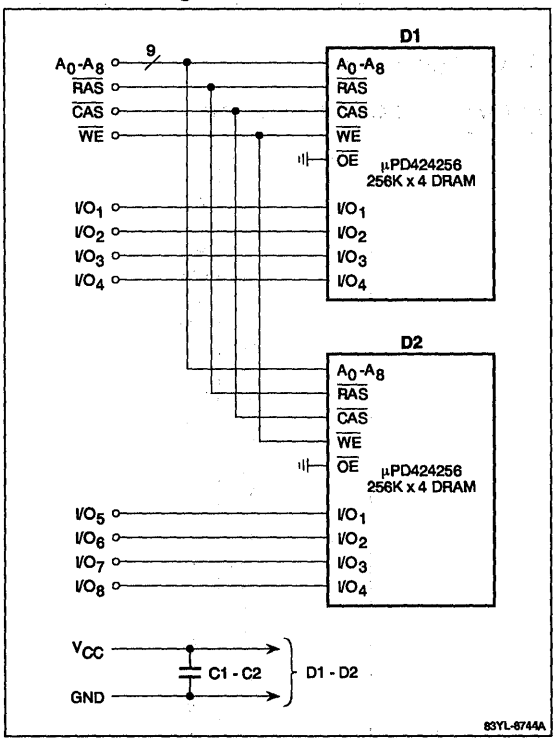
30-Pin Socket-Mountable SIMM



Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-42256AB8BA-60	60 ns	30-pin socket-mountable SIMM (solder plating)	16.8 mm (0.661 inch)	5.08 mm (0.200 inch)	Two μPD424256LA
BA-70	70 ns				
BA-80	80 ns				
BA-10	100 ns				
MC-42256AB8FA-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
FA-70	70 ns				
FA-80	80 ns				
FA-10	100 ns				

Connection Diagram



Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}$	Column address strobe
I/O_1 - I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	2.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	70	pF	A_0 - A_8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Input/output capacitance	$C_{I/O}$	10	pF	I/O_1 - I/O_8

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			4	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}
				2	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	I_{IL}	−20		20	μA	For A_0 - A_8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1 - I/O_8 and D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		−60		−70		−80		−10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		180		160		140		120	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		180		160		140		120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		160		140		120		100	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		180		160		140		120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 11)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		70		ns	
Column address setup time	t_{ASC}	0		0		0	20	0	20	ns	(Note 11)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		45		50		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10, 11)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	

AC Characteristics (cont)

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10	20	10	25	ns	(Note 11)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 14)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 17)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 12)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	10,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 15)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		4		4		4		4	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 15)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	145		155		190		225		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 18)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 18)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 16)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(13) For fast-page read operation, the definition of access time is as follows:

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{CAC}

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

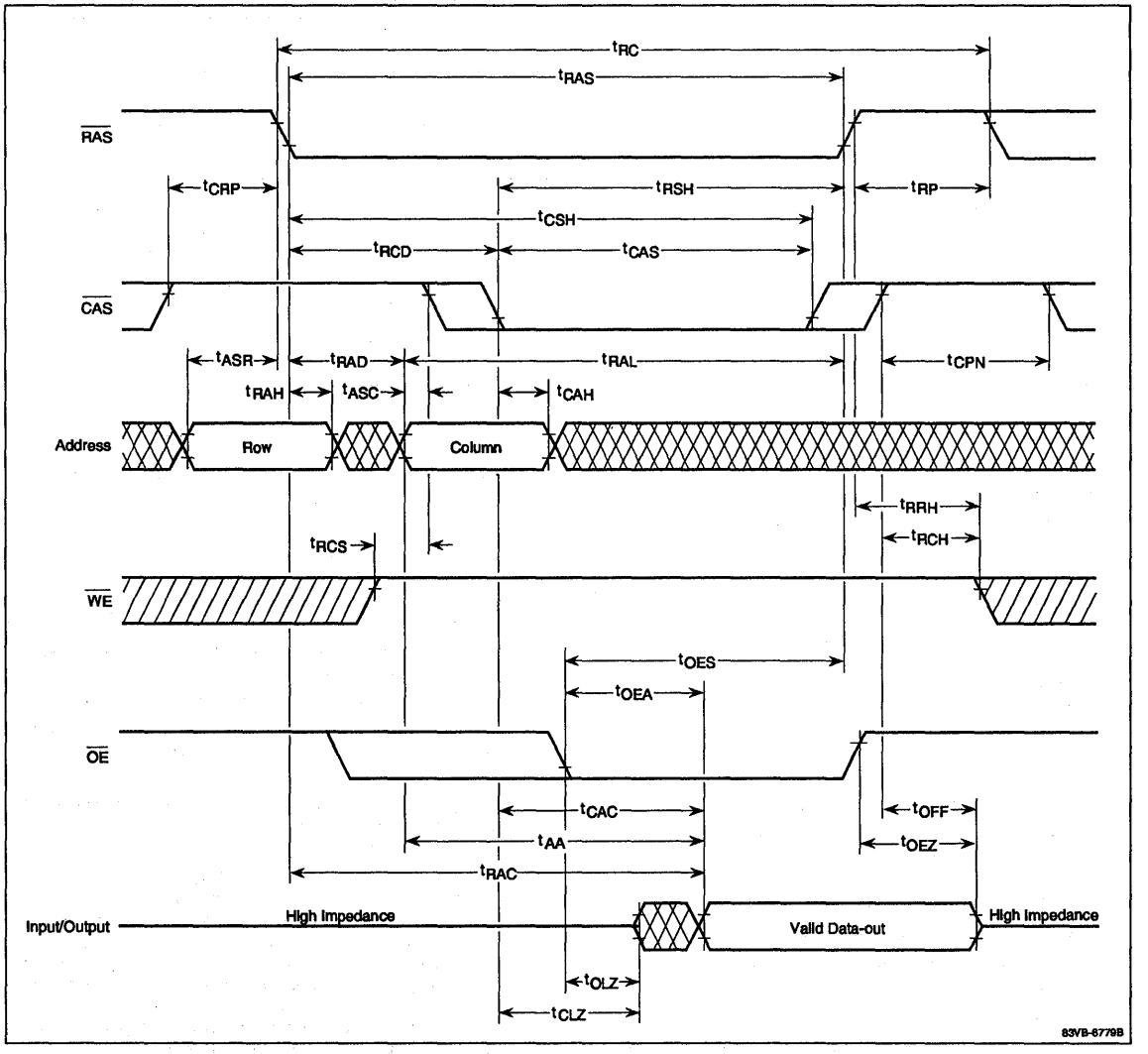
(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) For D_{OUT9} parameters t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of D_{OUT9} (at access time and until $\overline{CAS_9}$ returns to V_{IH}) is indeterminate.

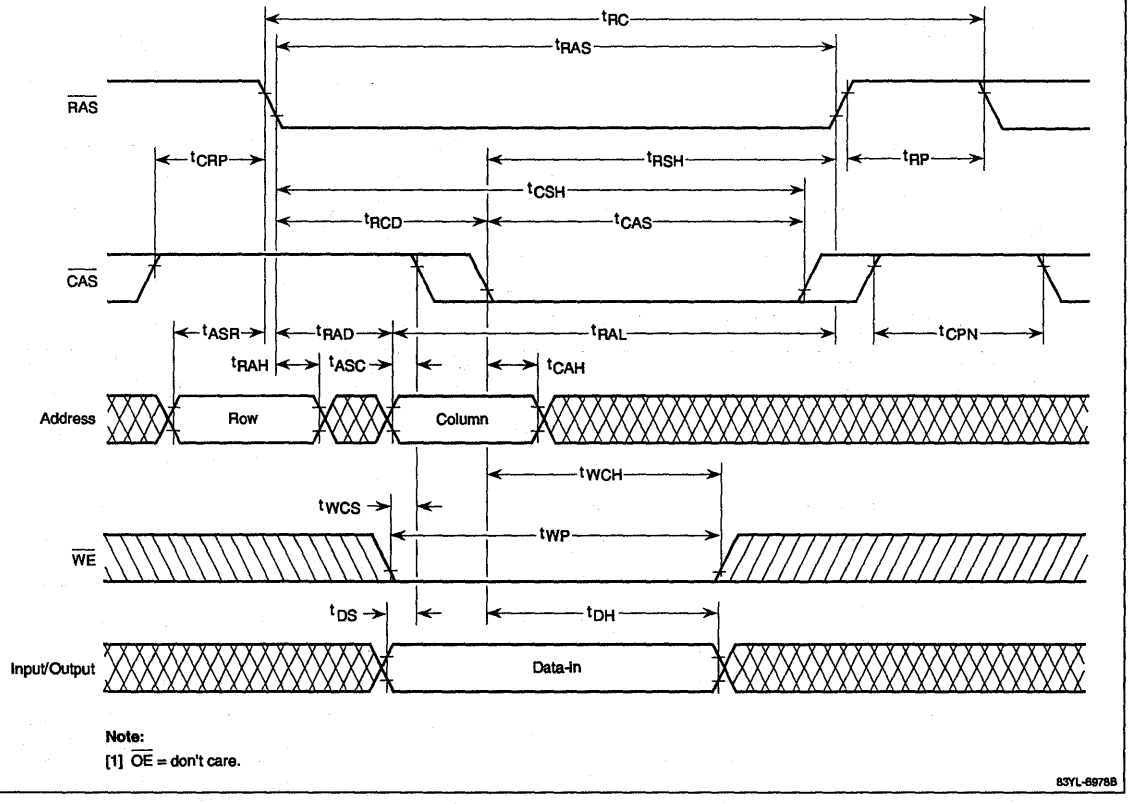
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle

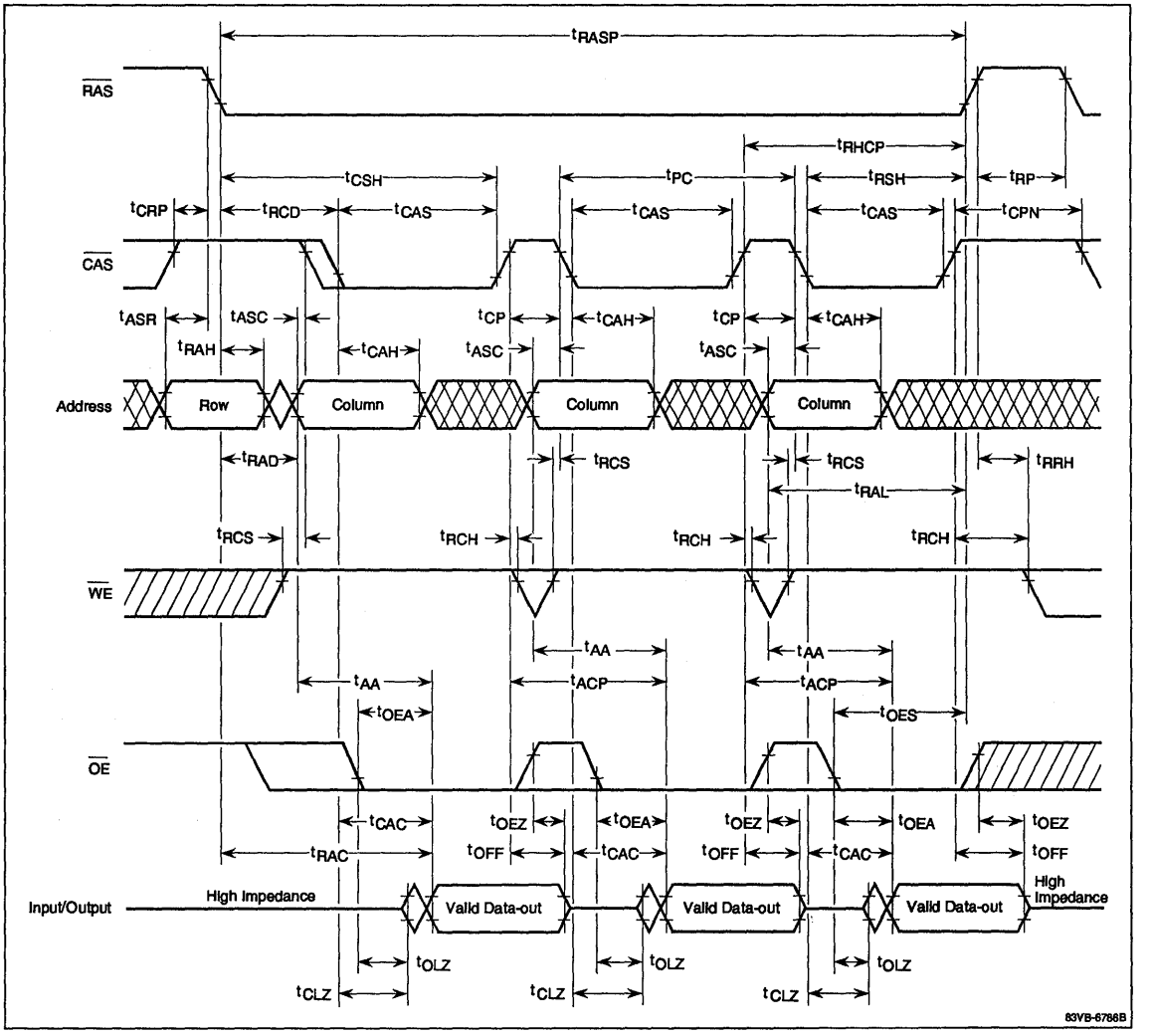


Note:
[1] $\overline{OE}$ = don't care.

83YL-6978B

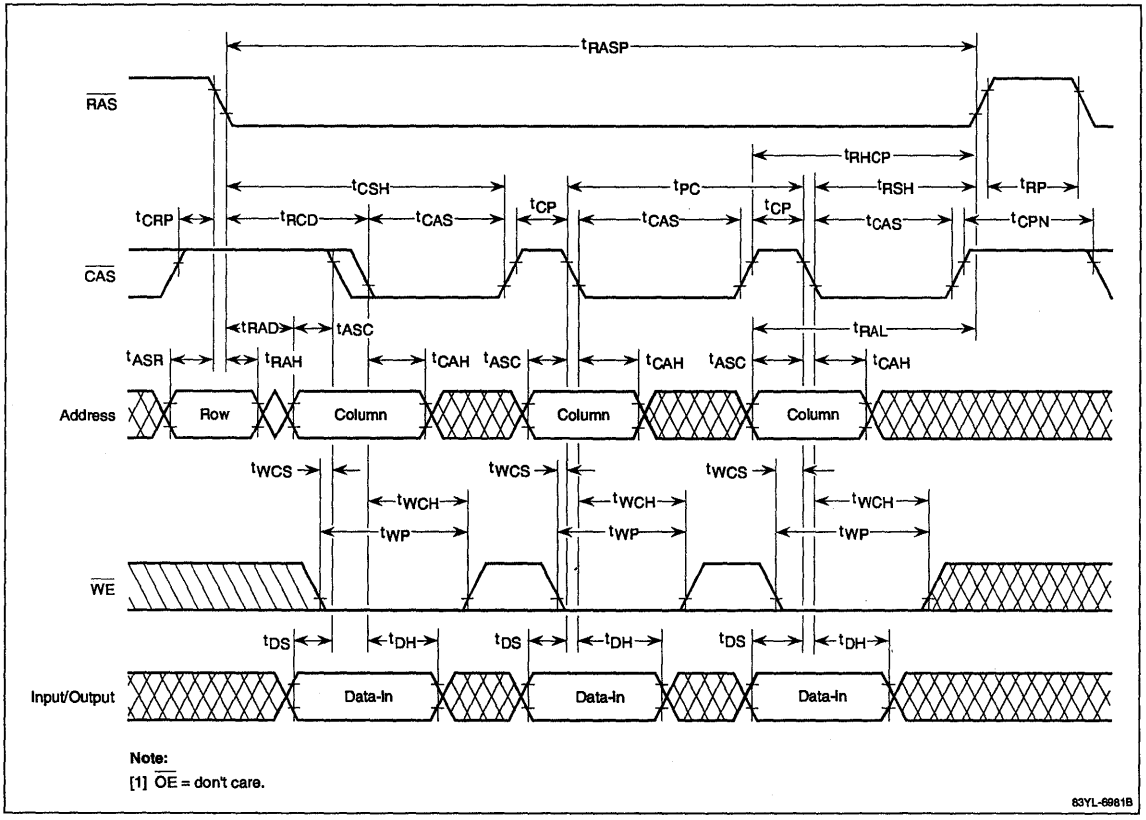
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



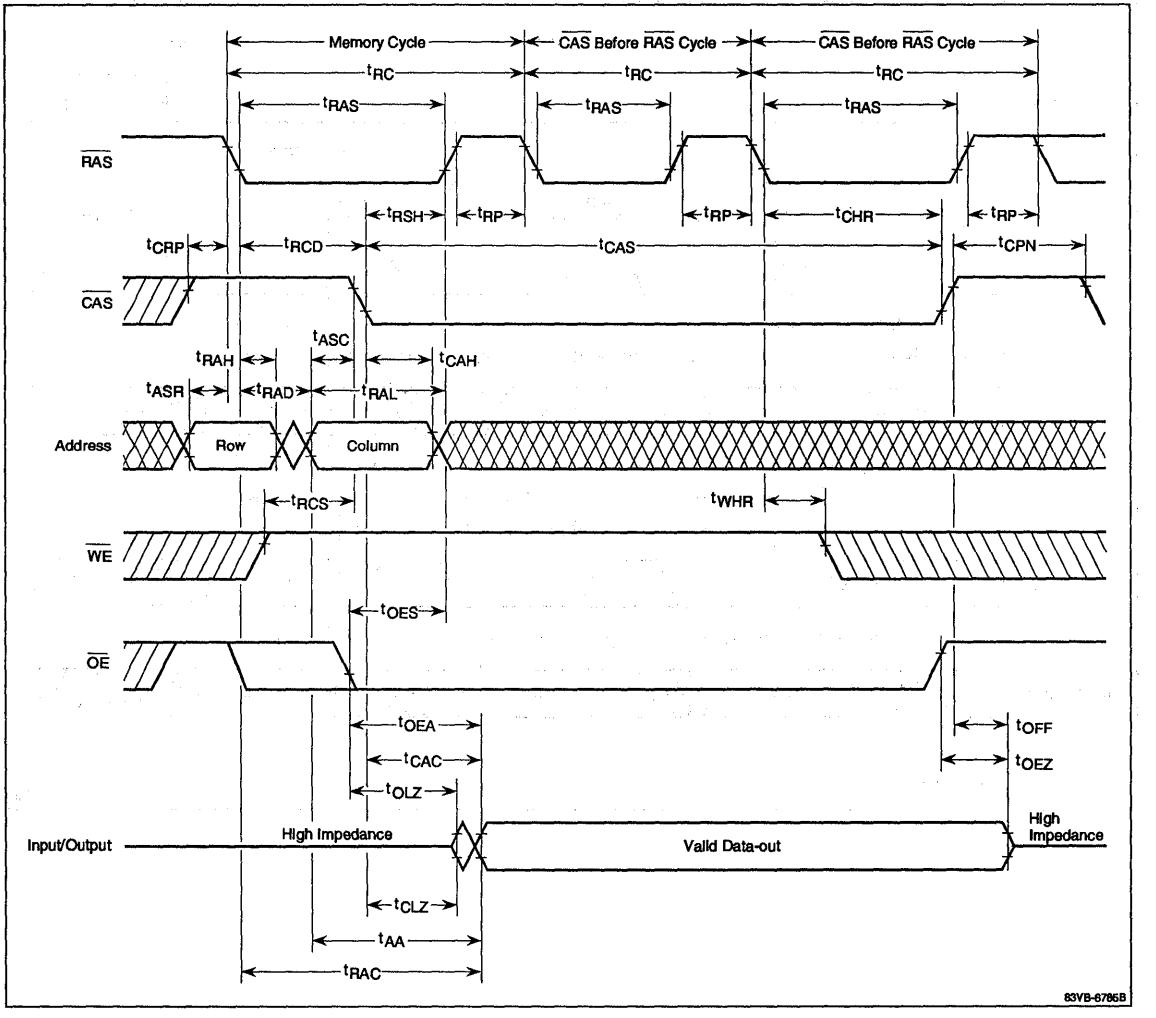
Note:

[1] $\overline{OE}$ = don't care.

63YL-6961B

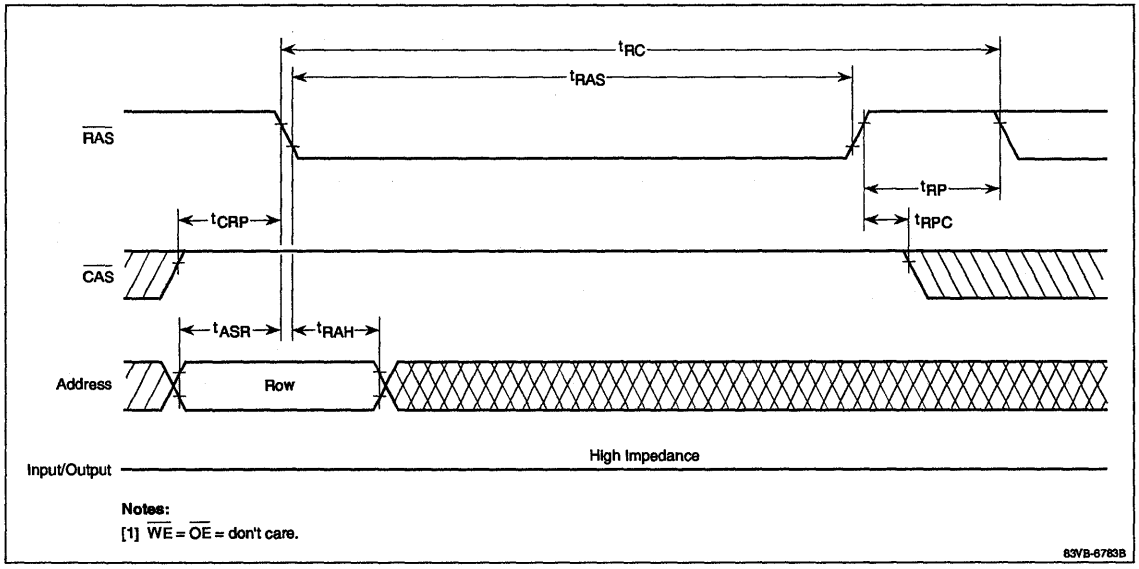
Timing Waveforms (cont)

Hidden Refresh Cycle

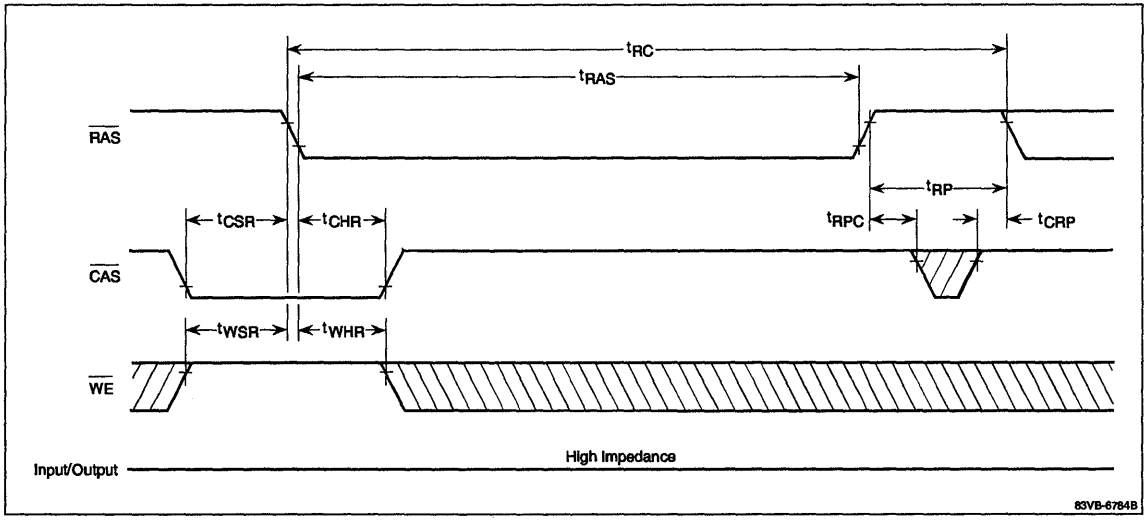


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



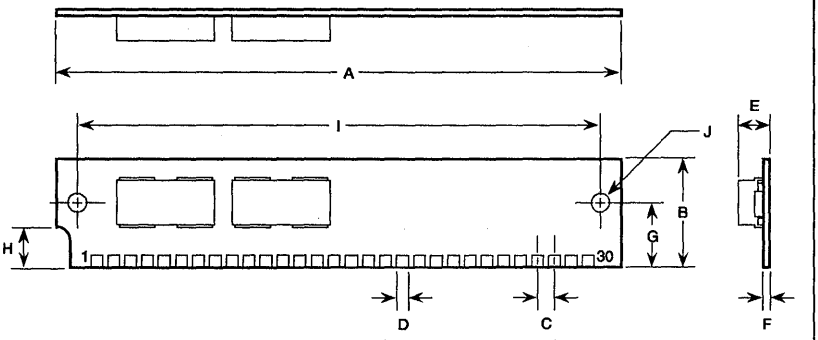
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Package Drawing

30-Pin Socket-Mountable SIMM (MC-42256AB8, Suffix BA or FA)

Item	Millimeters	Inches
A	88.90	3.500
B	16.80 max	.661 max
C	2.54	.100
D	1.78	.070
E	5.08 max	.200 max
F	1.27 ± .08	.050 ± .0032
G	10.16	.400
H	6.35	.250
I	82.10	3.232
J	3.175 dia	.125 dia



MC-42256AB8BA/FA

83YL-67458

MC-42256AB9
262,144 x 9-Bit
Dynamic CMOS RAM Module

Description

The MC-42256AB9 is a 262,144-word by 9-bit DRAM module designed to operate from a single +5-volt power supply. The module is a 30-pin socket-mountable Single Inline Memory Module (SIMM™) containing two μPD424256LA DRAMs (256K x 4) and one μPD42256L DRAM (256K x 1).

The MC-42256AB9 is functionally equivalent to eight μPD42256 standard 256K x 1 DRAMs with a parity bit. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 - A_8 during a 4-ms period.

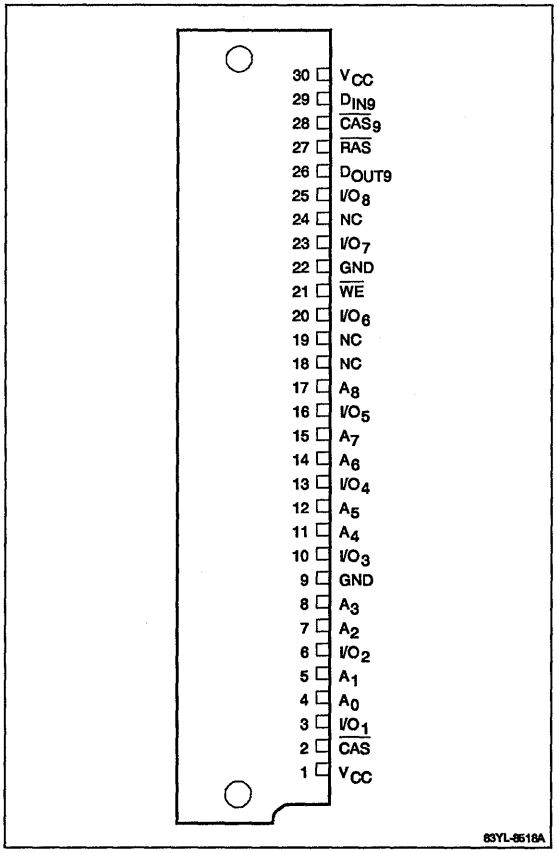
Features

- 262,144-word by 9-bit organization
- Single +5-volt power supply
- Standard 30-pin SIMM packaging
- Three 256K DRAMs
- Three power supply decoupling capacitors
- Low power dissipation of 16.5 mW max (standby)
- TTL-compatible inputs and outputs
- 256 refresh cycles every 4 ms
- Page-mode capability

SIMM is a trademark of Wang Laboratories.

Pin Configurations

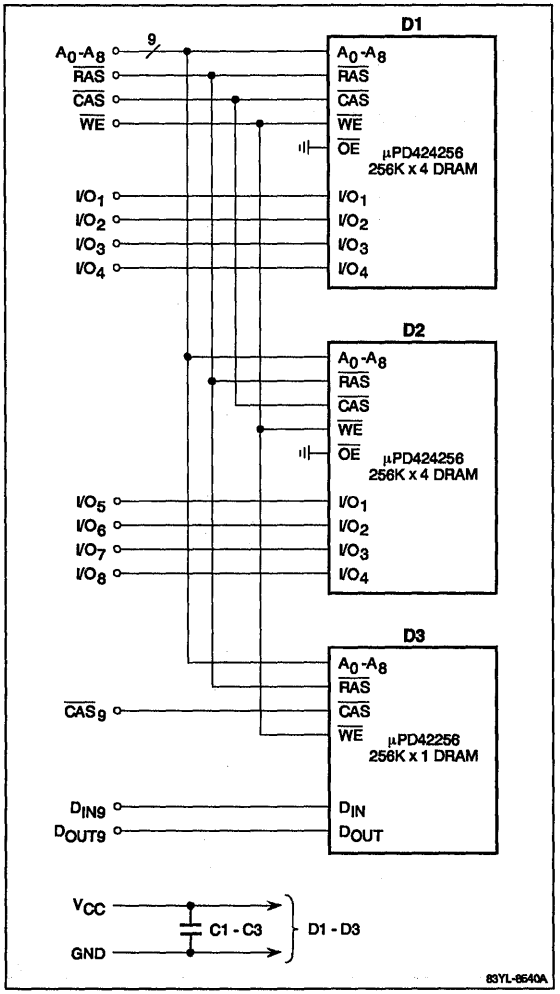
30-Pin Socket-Mountable SIMM



Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-42256AB9BA-60	60 ns	30-pin socket-mountable SIMM (solder plating)	16.8 mm (0.661 inch)	5.08 mm (0.200 inch)	Two μPD424256LA One μPD42256L
BA-70	70 ns				
BA-80	80 ns				
BA-10	100 ns				
MC-42256AB9FA-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
FA-70	70 ns				
FA-80	80 ns				
FA-10	100 ns				

Connection Diagram



Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}$	Column address strobe
$\overline{CAS_9}$	Column address strobe for data output 9
D_{IN9}	Data input 9
D_{OUT9}	Data output 9
I/O_1 - I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	3.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage*	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

* V_{CC} = +5.0 V ±5% for the −80 version.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	75	pF	A_0 - A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
	C_{I2}	13	pF	$\overline{CAS_9}$, D_{IN9}
Input/output capacitance	$C_{I/O}$	17	pF	I/O_1 - I/O_8
Output capacitance	C_O	12	pF	D_{OUT9}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			6	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}
				3	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	I_{IL}	−30		30	μA	For A_0 - A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
Input leakage current	I_{IL9}	−10		10	μA	For $\overline{CAS}_9$, D_{IN9}; V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1 - I/O_8 and D_{OUT9} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		−60		−70		−80		−10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		270		240		210		180	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		270		240		210		180	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		240		210		180		150	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		270		240		210		180	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 11)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		70		ns	
Column address setup time	t_{ASC}	0		0		0	20	0	20	ns	(Note 11)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		45		50		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10, 11)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	

AC Characteristics (cont)

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10	20	10	25	ns	(Note 11)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 14)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 17)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 12)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	10,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 15)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		4		4		4		4	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 15)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	145		155		190		225		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 18)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 18)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 16)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(13) For fast-page read operation, the definition of access time is as follows:

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{CAC}

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

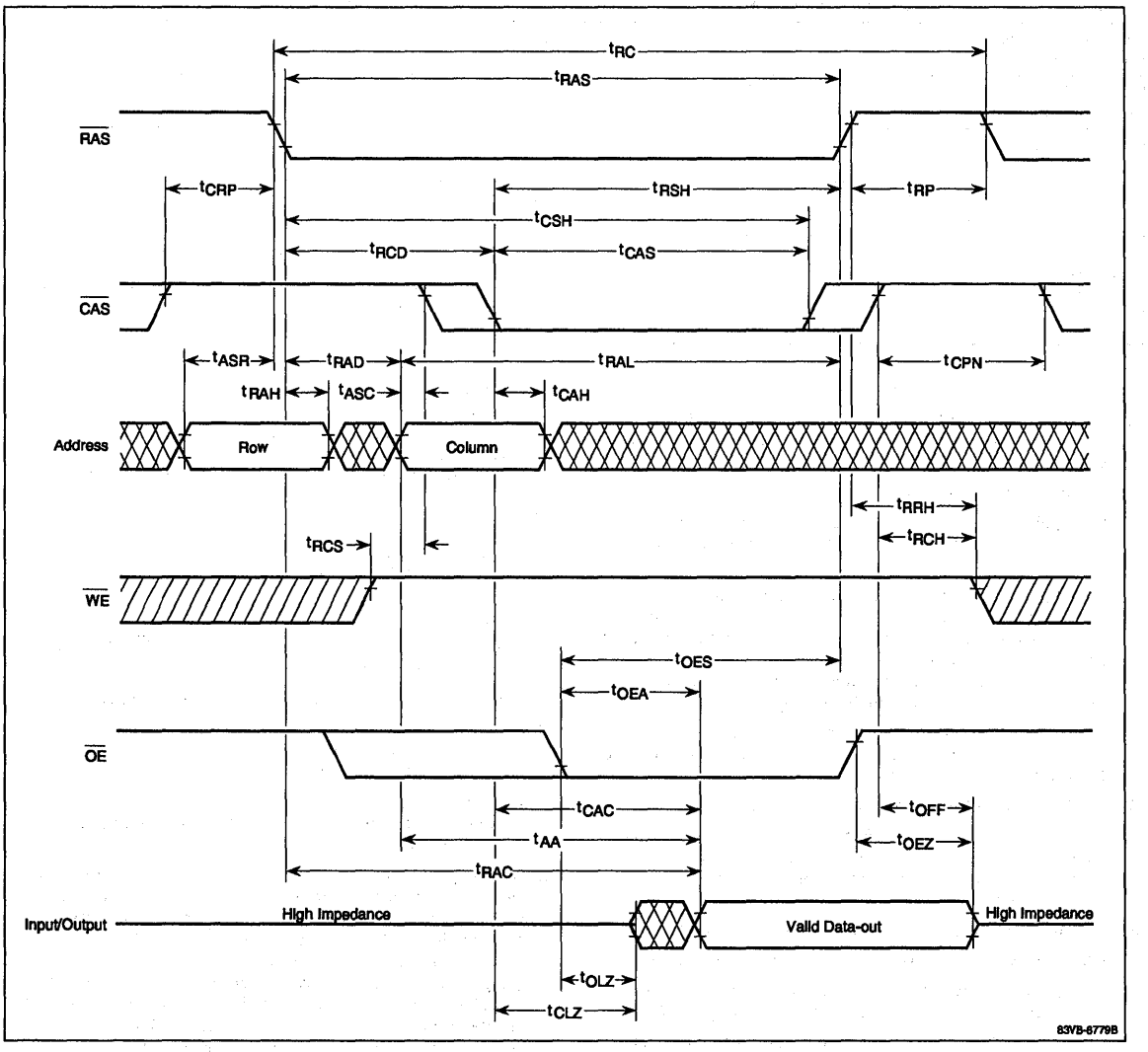
(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) For D_{OUT9} parameters t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of D_{OUT9} (at access time and until $\overline{CAS_9}$ returns to V_{IH}) is indeterminate.

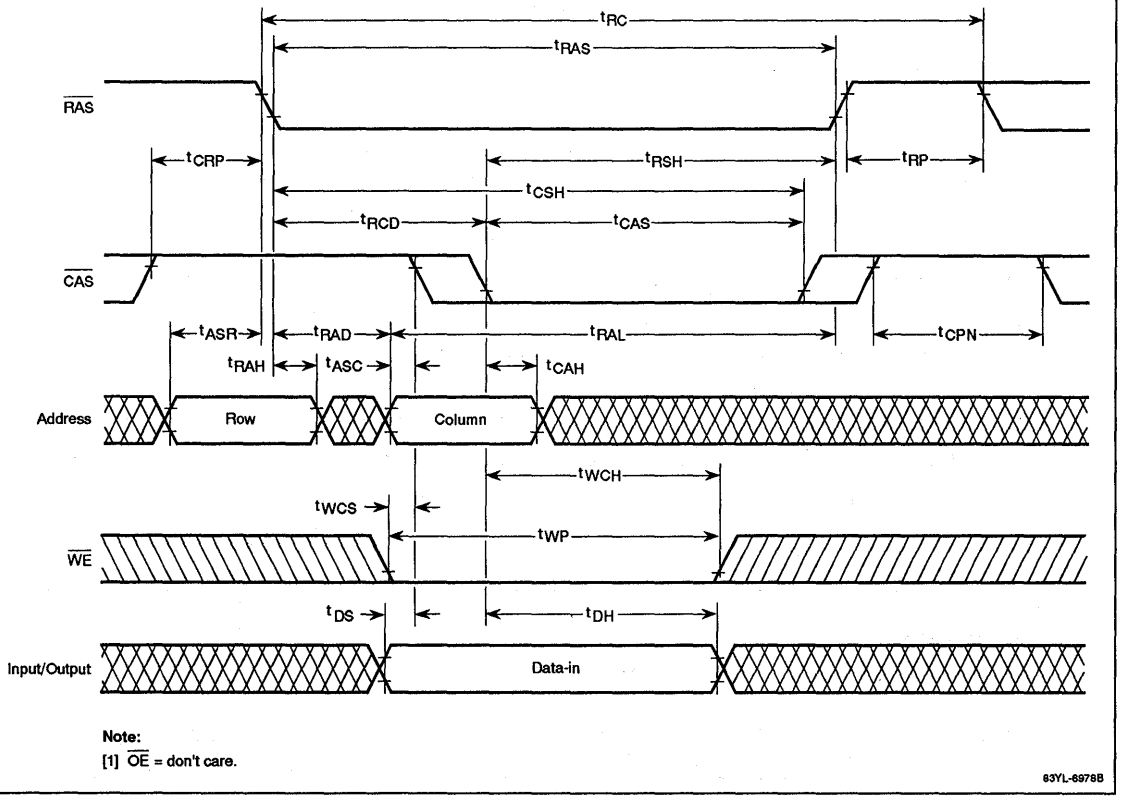
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle

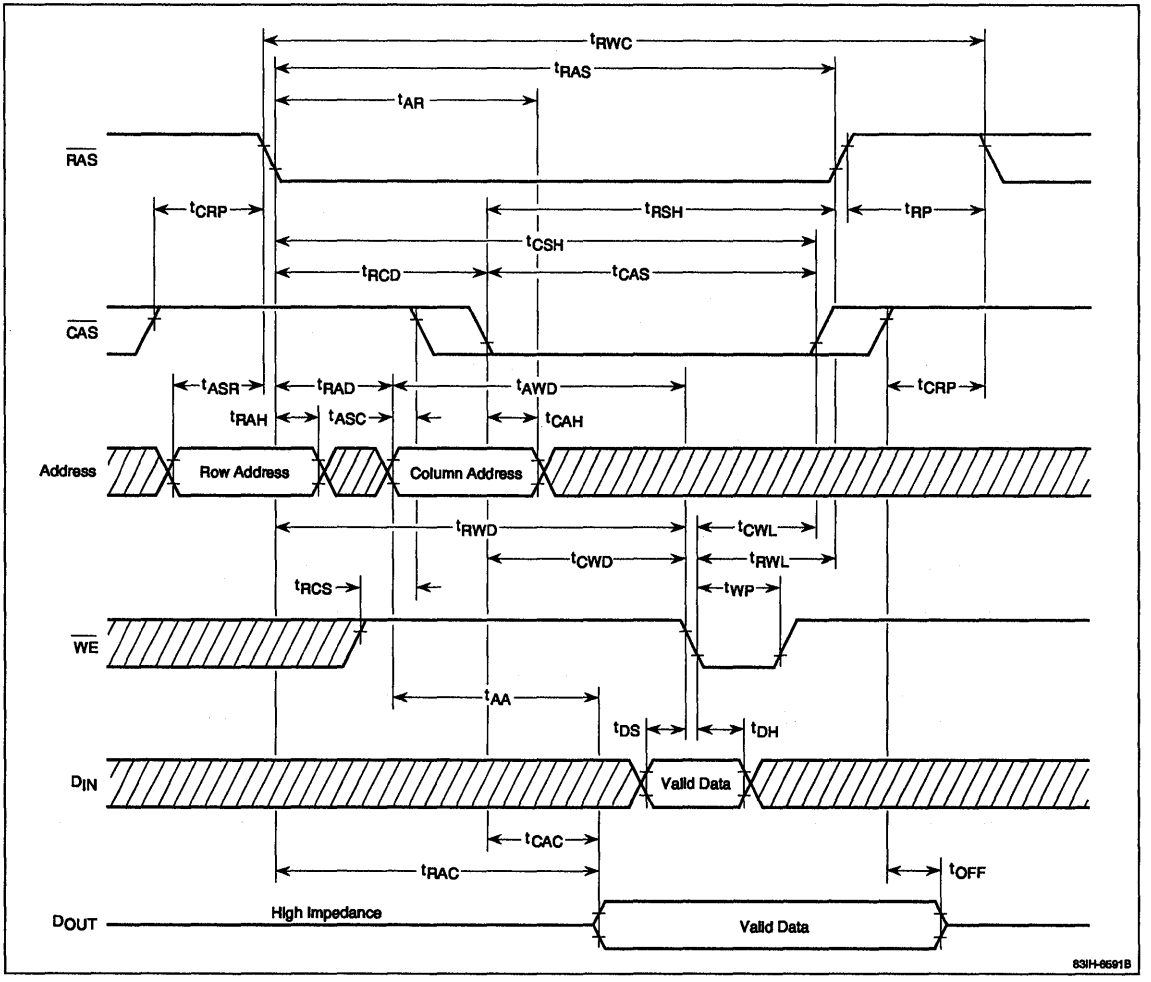


Note:
[1] $\overline{OE}$ = don't care.

83YL-6978B

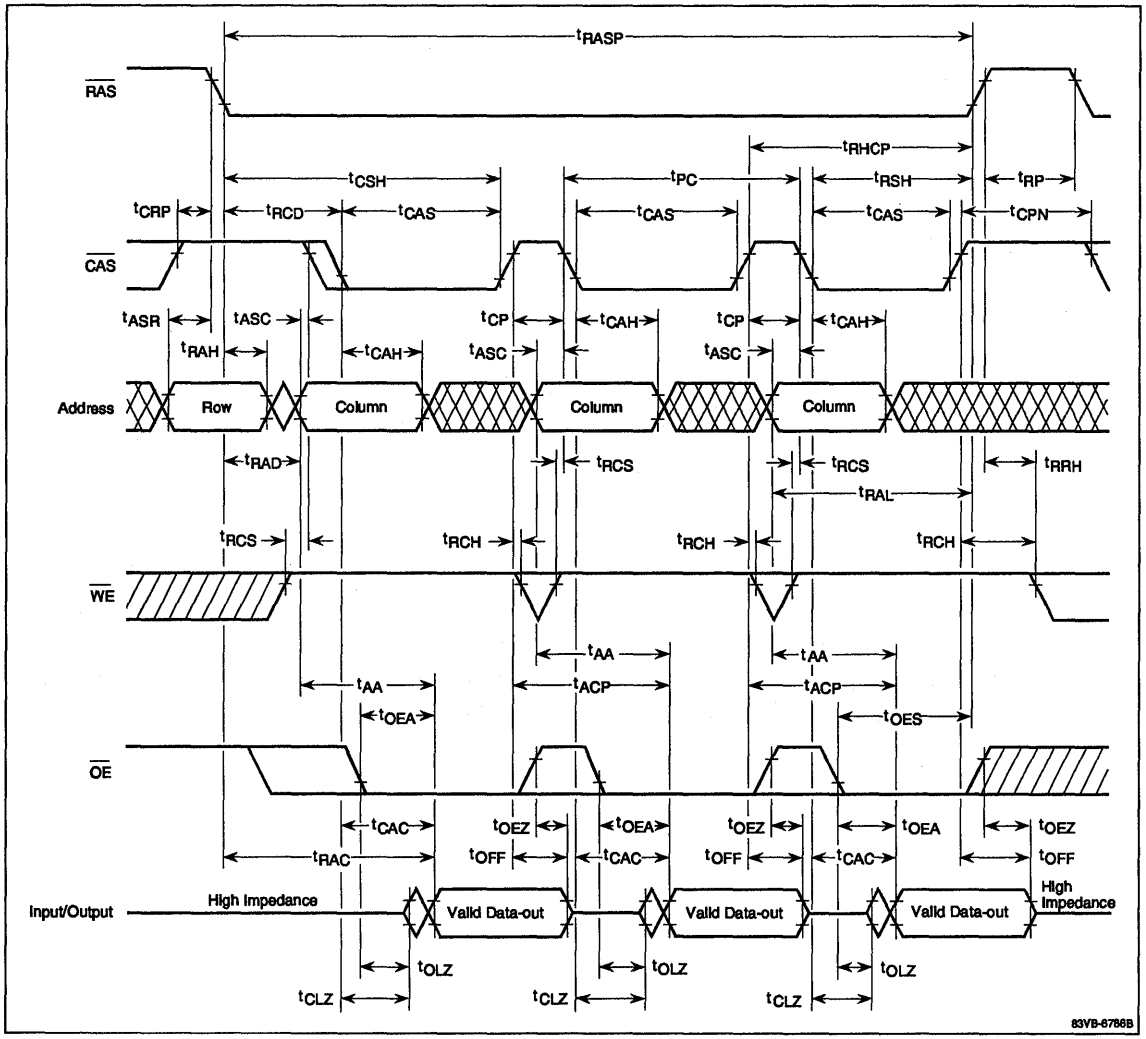
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle (D_{OUT9} only)



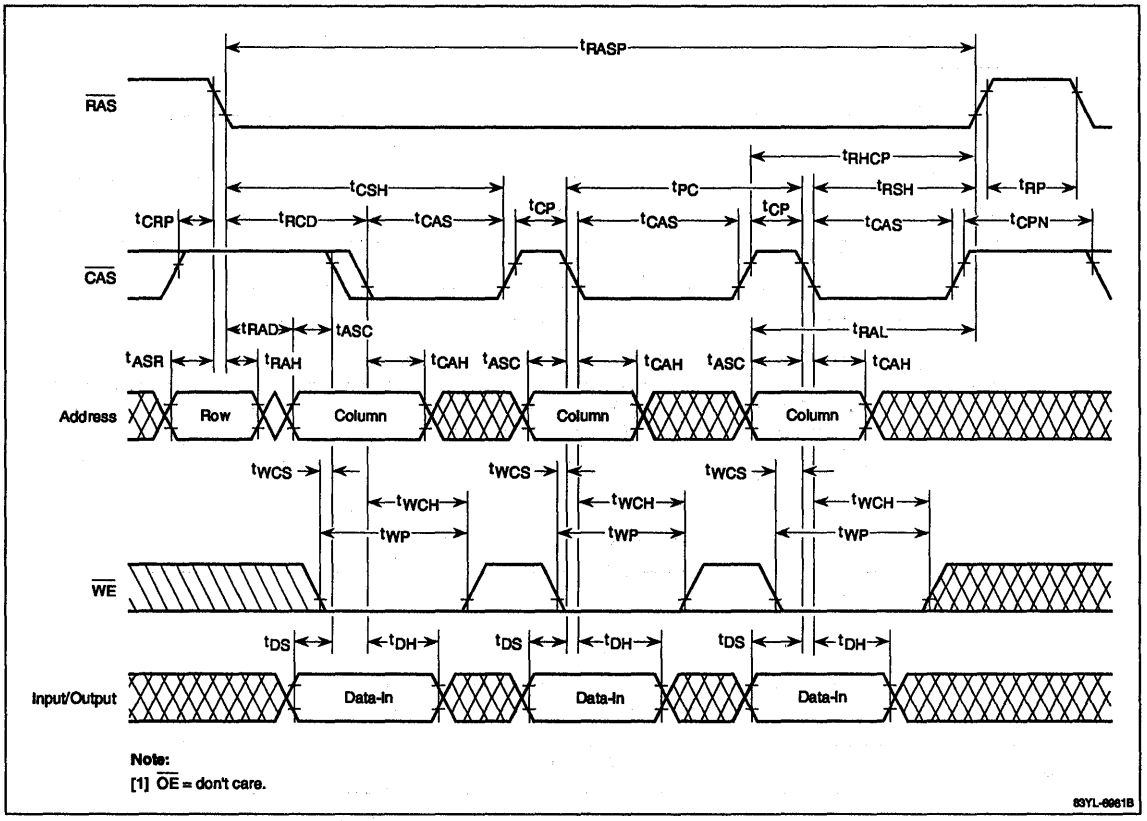
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle

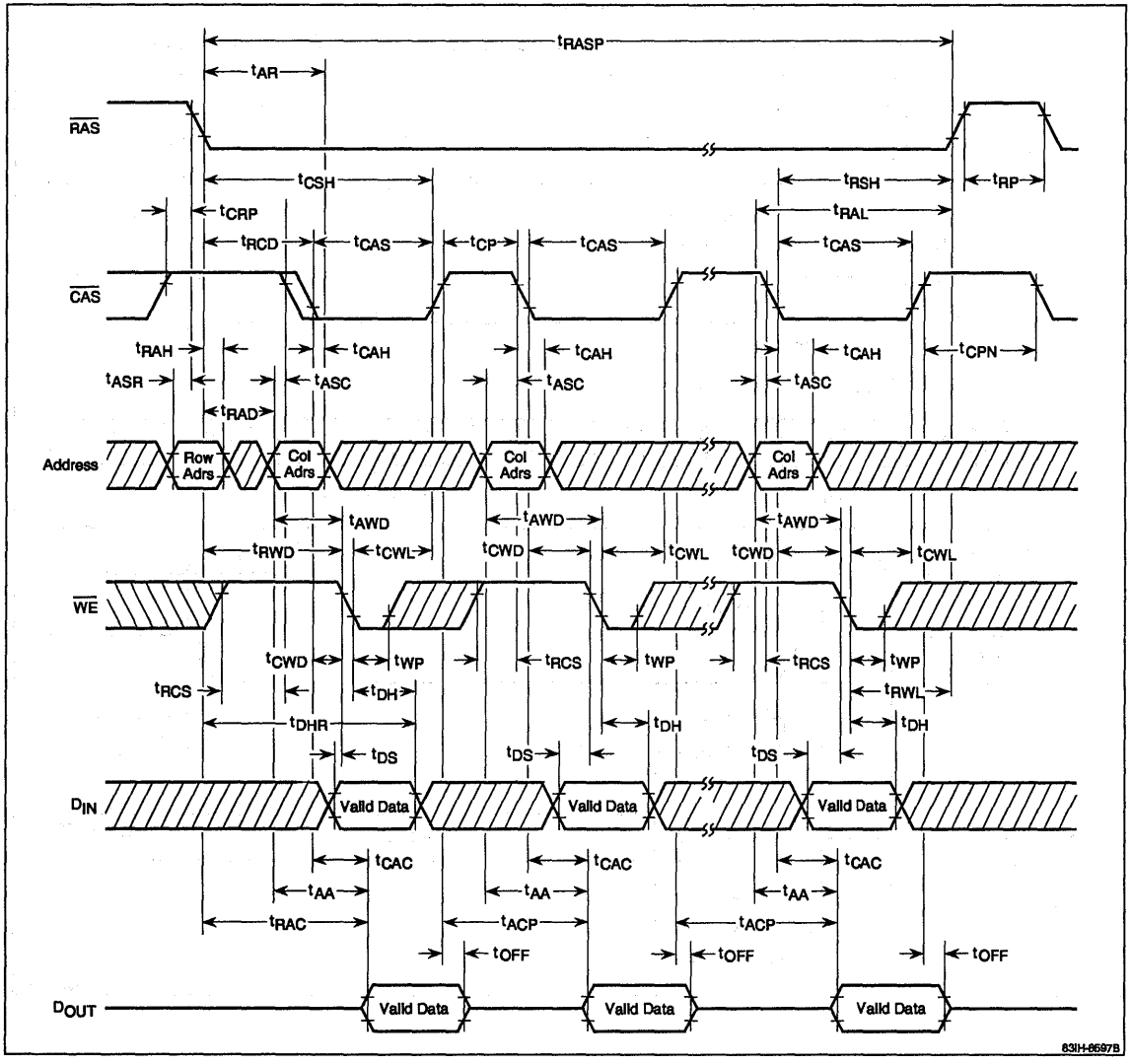


Note:
[1] $\overline{OE}$ = don't care.

83YL-6961B

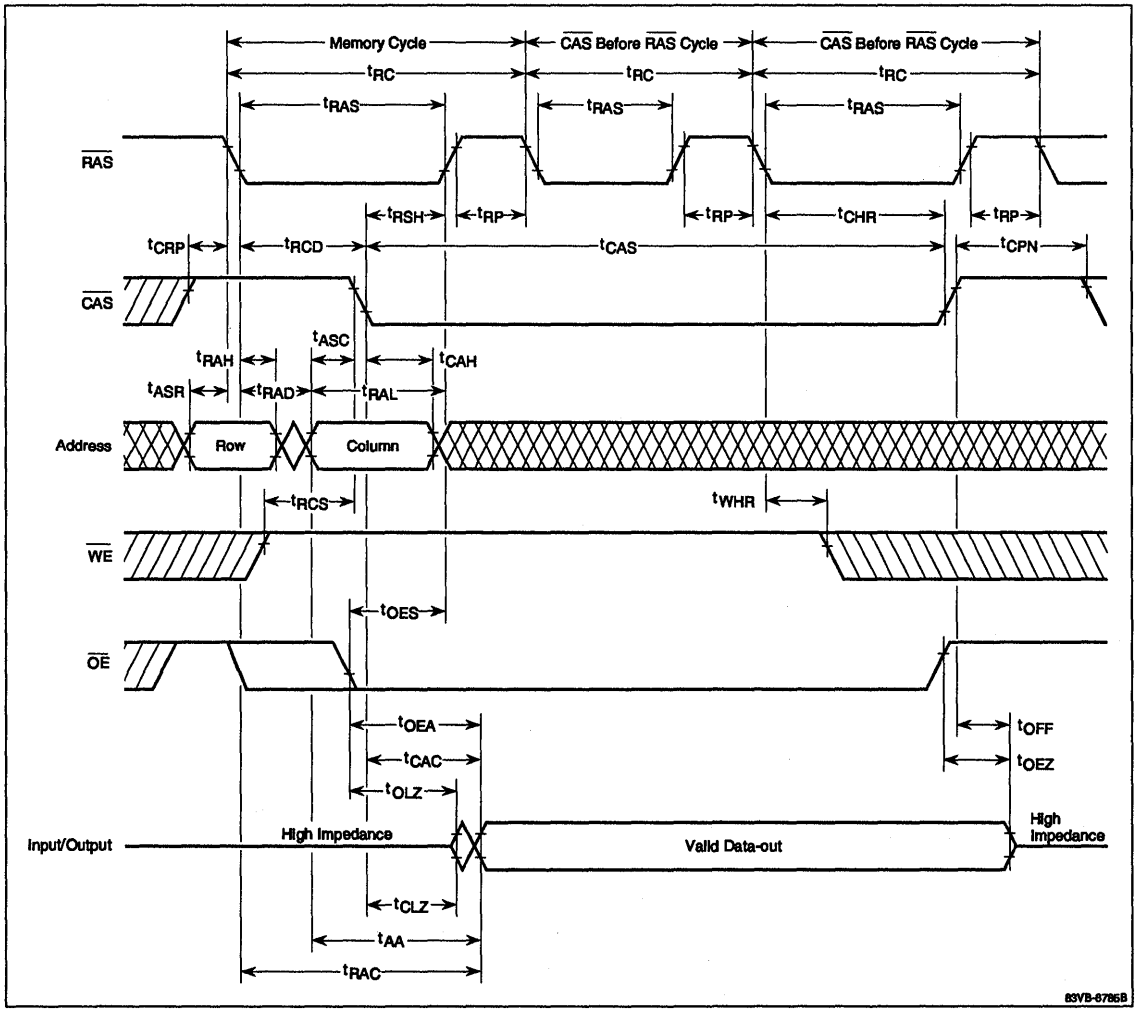
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle (D_{OUT9} only)



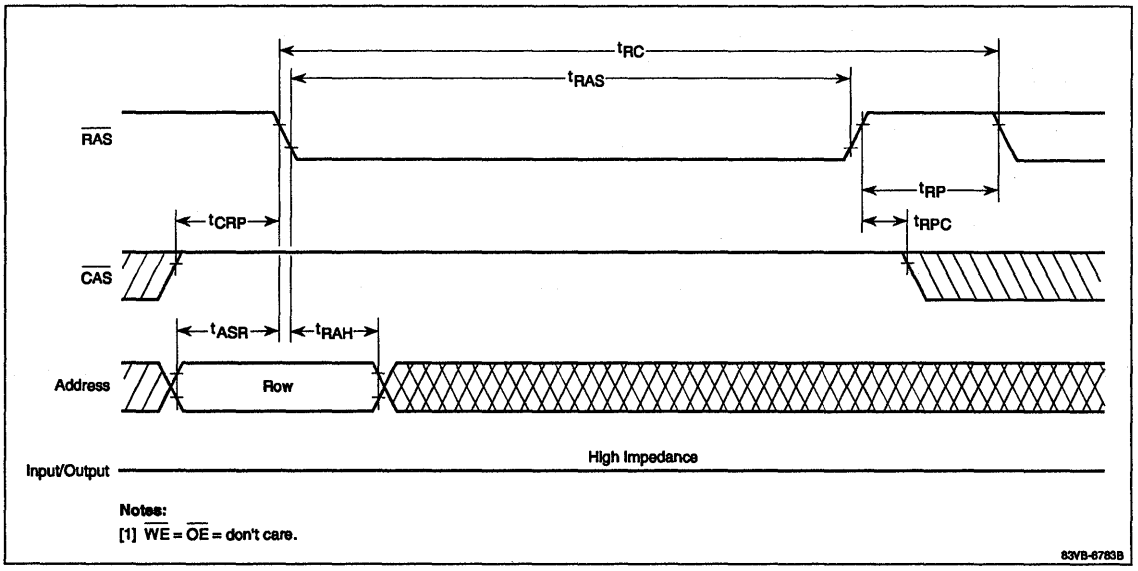
Timing Waveforms (cont)

Hidden Refresh Cycle

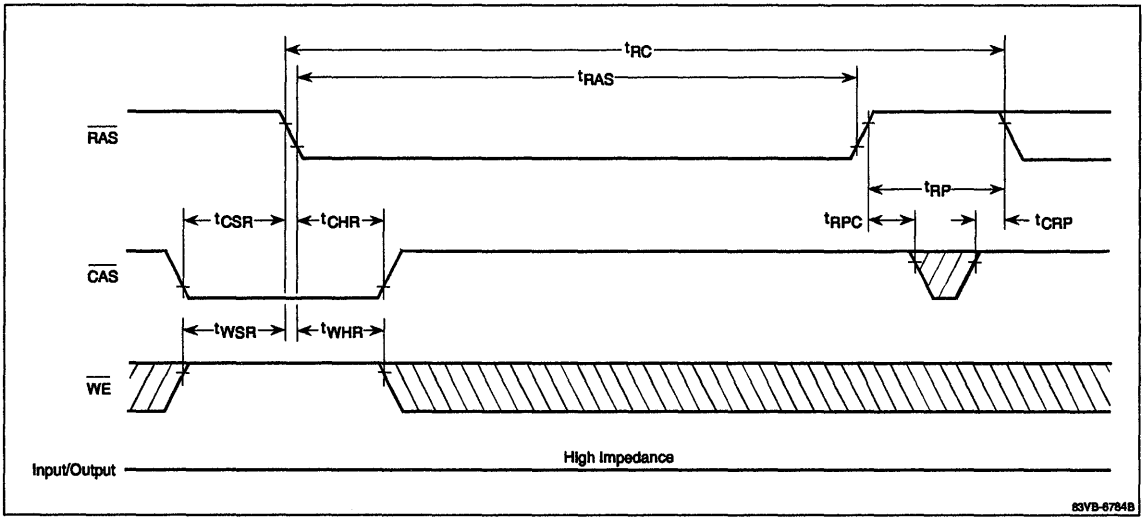


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



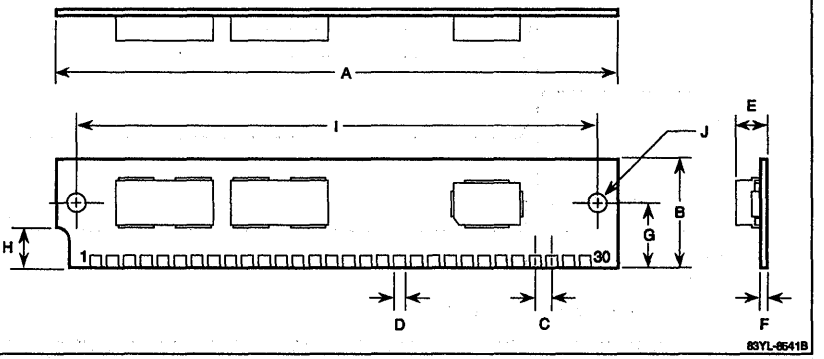
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Package Drawing

30-Pin Socket-Mountable SIMM (MC-42256AB9BA/FA)

Item	Millimeters	Inches
A	88.90	3.500
B	16.80 max	.661 max
C	2.54	.100
D	1.78	.070
E	5.08 max	.200 max
F	1.27 ± .08	.050 ± .0032
G	10.16	.400
H	6.35	.250
I	82.10	3.232
J	3.175 dia	.125 dia



MC-42256AB9BA/FA

83YL-6541B

MC-42256A32
262,144 x 32-Bit
Dynamic CMOS RAM Module

Description

The MC-42256A32 is a fast-page dynamic RAM module organized as 262,144 words by 32 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 512 address combinations of A_0 - A_8 during an 8-ms period.

The MC-42256A32 is packaged in a variety of Single Inline Memory Modules (SIMM™). Each SIMM contains eight 262,144 x 4-bit μPD424256 DRAMs and eight power supply decoupling capacitors for noise reduction. DQ_1 - DQ_{32} are common input/output pins.

Features

- 262,144-word by 32-bit organization
- Single +5-volt power supply
- Fast-page cycles
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 512 refresh cycles every 8 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

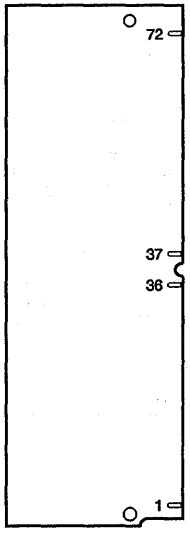
SIMM is a trademark of Wang Laboratories.

Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobes
DQ_1 - DQ_{32}	Common data inputs/outputs
$\overline{RAS}_0$, $\overline{RAS}_2$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol
1	GND
2	DQ_1
3	DQ_{17}
4	DQ_2
5	DQ_{18}
6	DQ_3
7	DQ_{19}
8	DQ_4
9	DQ_{20}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	NC
20	DQ_5
21	DQ_{21}
22	DQ_6
23	DQ_{22}
24	DQ_7
25	DQ_{23}
26	DQ_8
27	DQ_{24}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	NC
33	NC
34	$\overline{RAS}_2$
35	NC
36	NC

Pin	Symbol
37	NC
38	NC
39	GND
40	$\overline{CAS}_0$
41	$\overline{CAS}_2$
42	$\overline{CAS}_3$
43	$\overline{CAS}_1$
44	$\overline{RAS}_0$
45	NC
46	NC
47	$\overline{WE}$
48	NC
49	DQ_9
50	DQ_{25}
51	DQ_{10}
52	DQ_{26}
53	DQ_{11}
54	DQ_{27}

Pin	Symbol
55	DQ_{12}
56	DQ_{28}
57	DQ_{13}
58	DQ_{29}
59	V_{CC}
60	DQ_{30}
61	DQ_{14}
62	DQ_{31}
63	DQ_{15}
64	DQ_{32}
65	DQ_{16}
66	NC
67	[Note 1]
68	[Note 1]
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes [1]: Pins 67 through 70 are defined by access time:

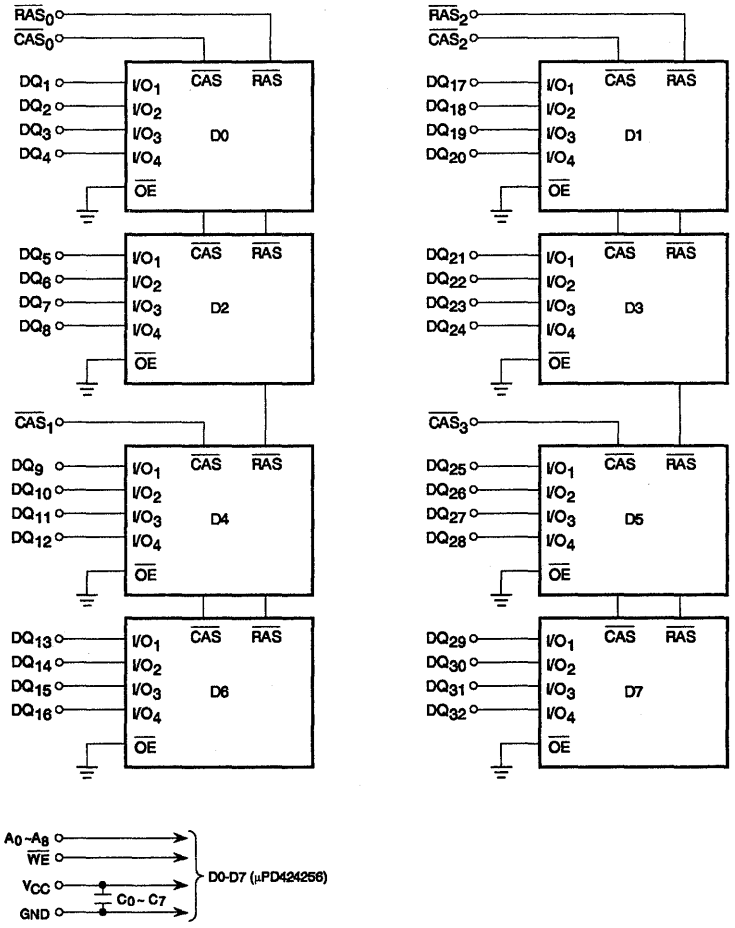
Pin	60 ns	70 ns	80 ns	100 ns
67	GND	GND	GND	GND
68	NC	NC	NC	NC
69	NC	GND	NC	GND
70	NC	NC	GND	GND

83YL-8609A

Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-42256A32B-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.00 inch)	5.08 mm (0.200 inch)	Eight μPD424256LA
B-70	70 ns				
B-80	80 ns				
B-10	100 ns				
MC-42256A32F-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				
F-10	100 ns				
MC-42256A32BT-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.00 inch)	2.68 mm (0.106 inch)	Eight μPD424256GX
BT-70	70 ns				
BT-80	80 ns				
BT-10	100 ns				
MC-42256A32FT-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FT-70	70 ns				
FT-80	80 ns				
FT-10	100 ns				

Connection Diagram



83YL-8510B

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		+70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	68	pF	A_0 - A_8
	C_{I2}	76	pF	$\overline{WE}$
	C_{I3}	43	pF	$\overline{RAS}$
	C_{I4}	29	pF	$\overline{CAS}$
Input/output capacitance	C_{I0}/C_{O0}	17	pF	DQ_1 - DQ_{32}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		16	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			8	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−80	80	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	DQ_1 to DQ_{32} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-60		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		720		640		560		480	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		720		640		560		480	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, page cycle, average	I_{CC4}		640		560		480		400	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		720		640		560		480	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40		55	ns	(Notes 7, 9)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		60		60		70		ns	
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	10		10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
Data-in hold time	t_{DH}	15		15		20		25		ns	(Note 15)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		60		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 10)
Page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	45	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		55		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, page cycle	t_{RASP}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		55		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

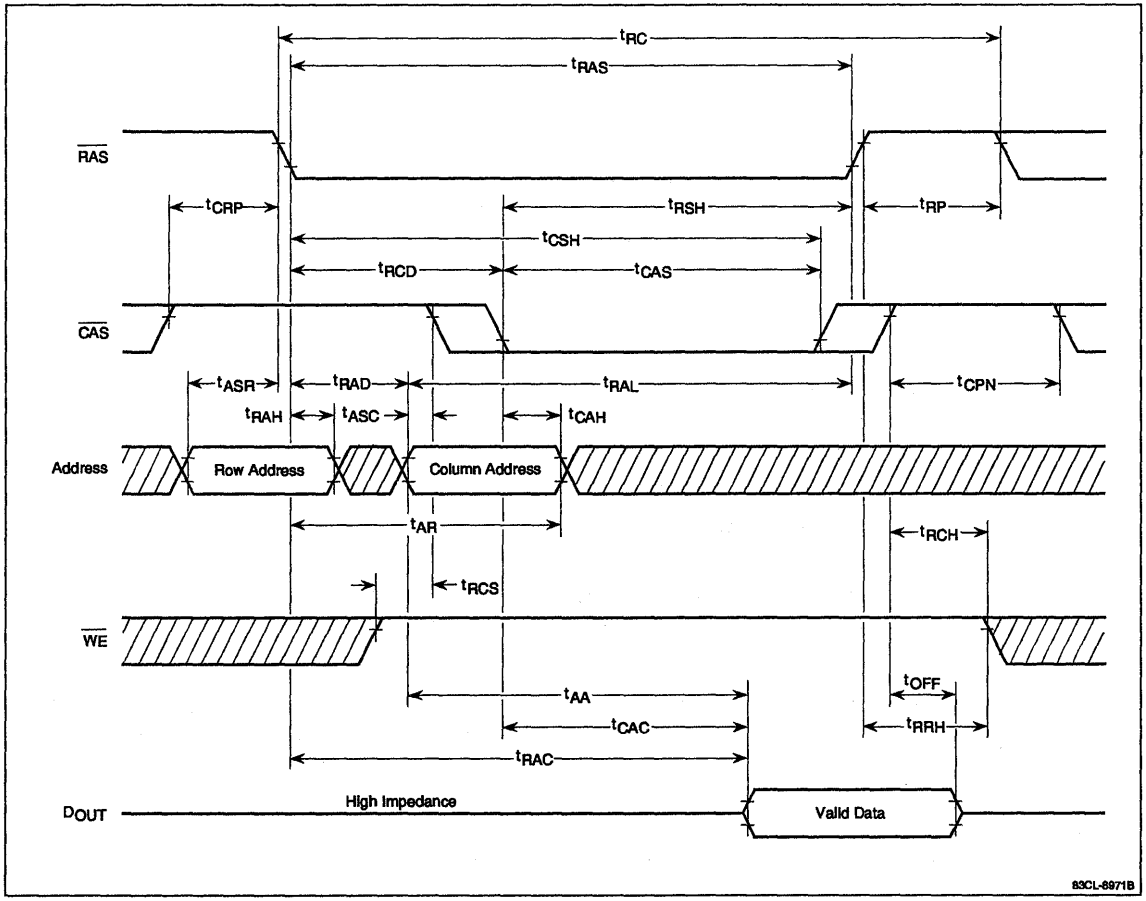
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

9c

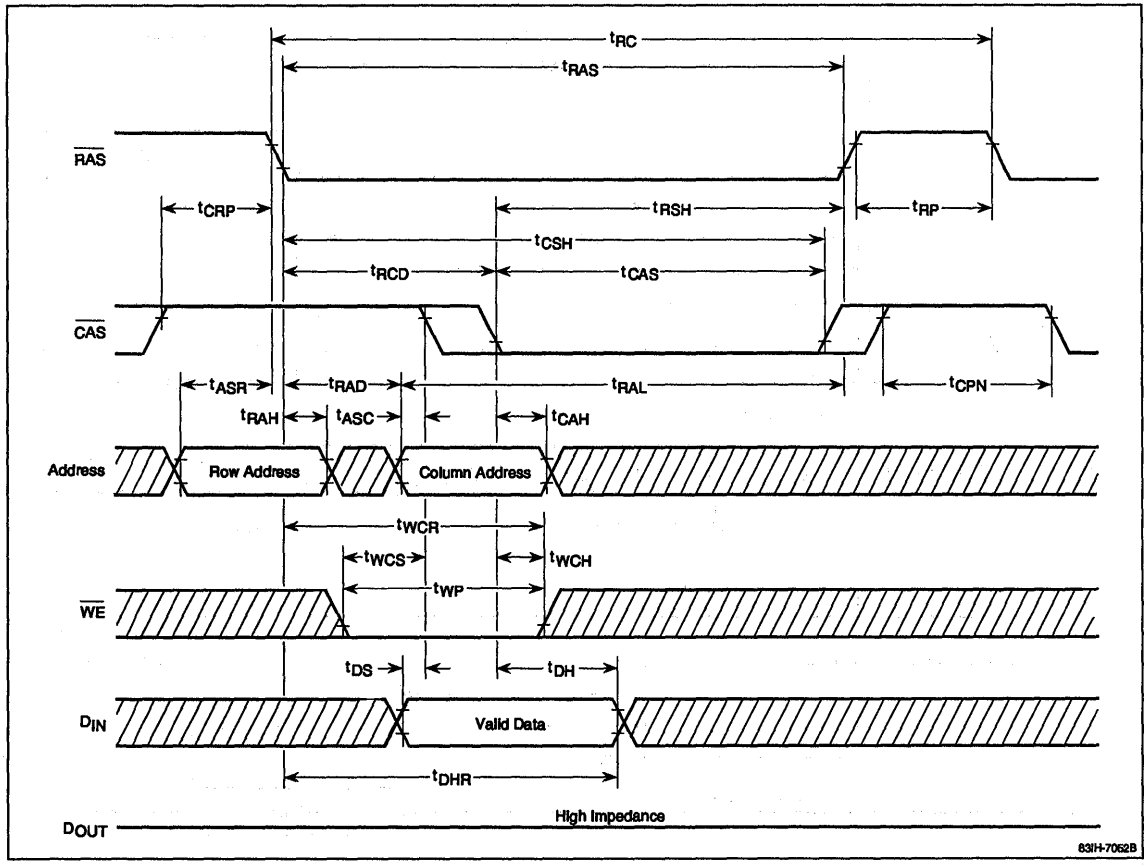
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



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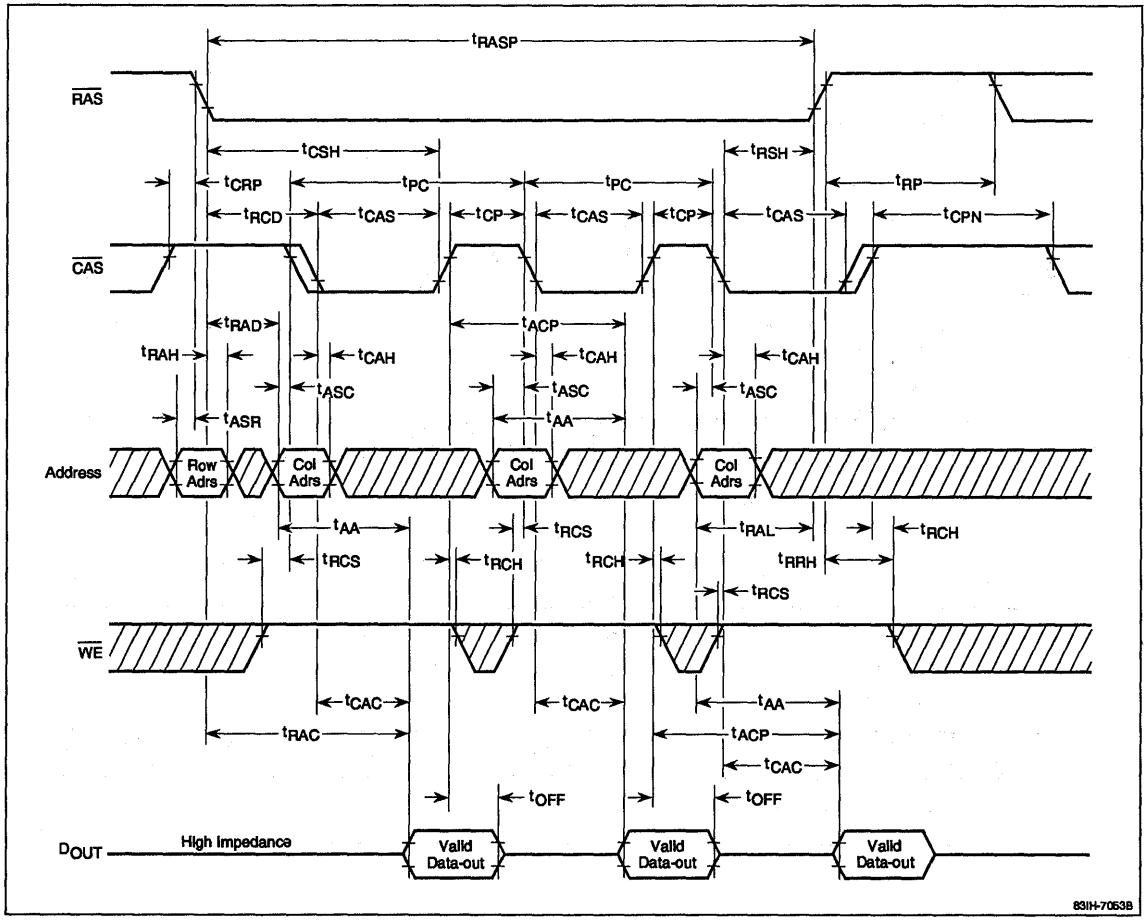
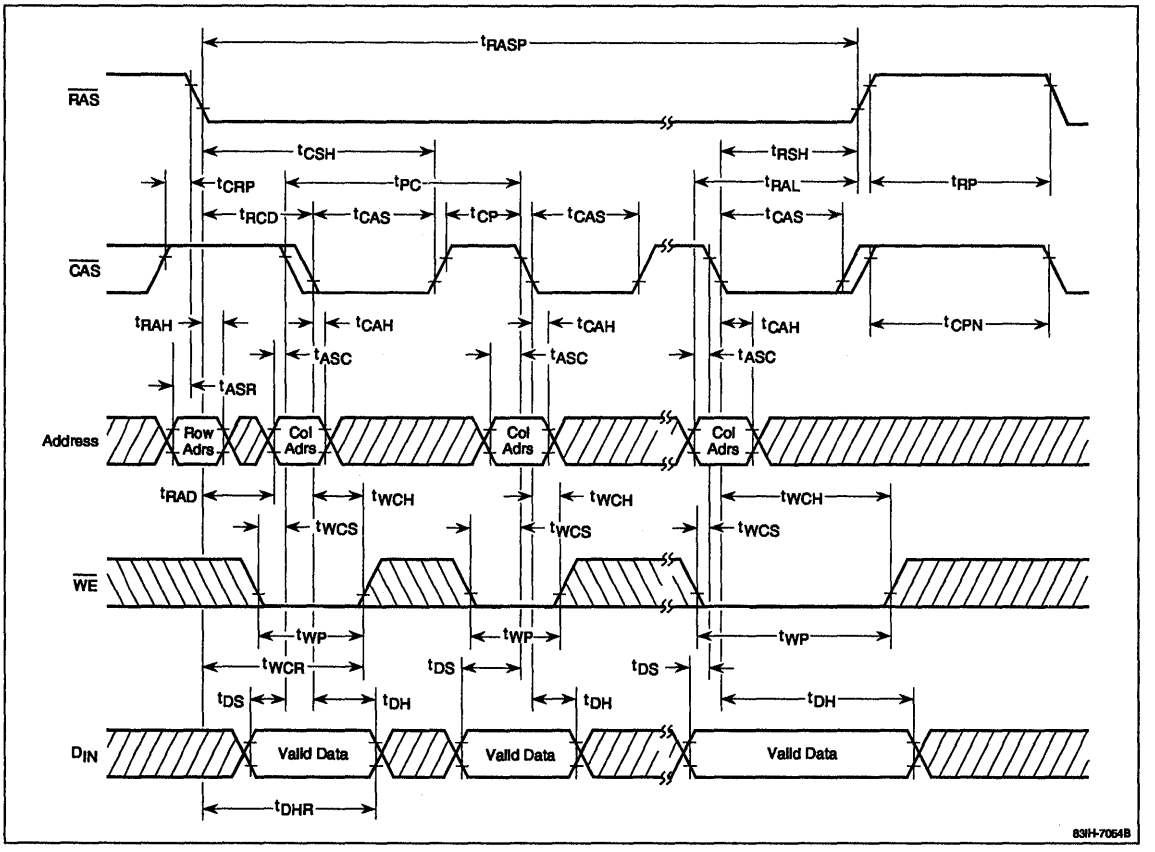
Timing Waveforms (cont)

Fast-Page Read Cycle



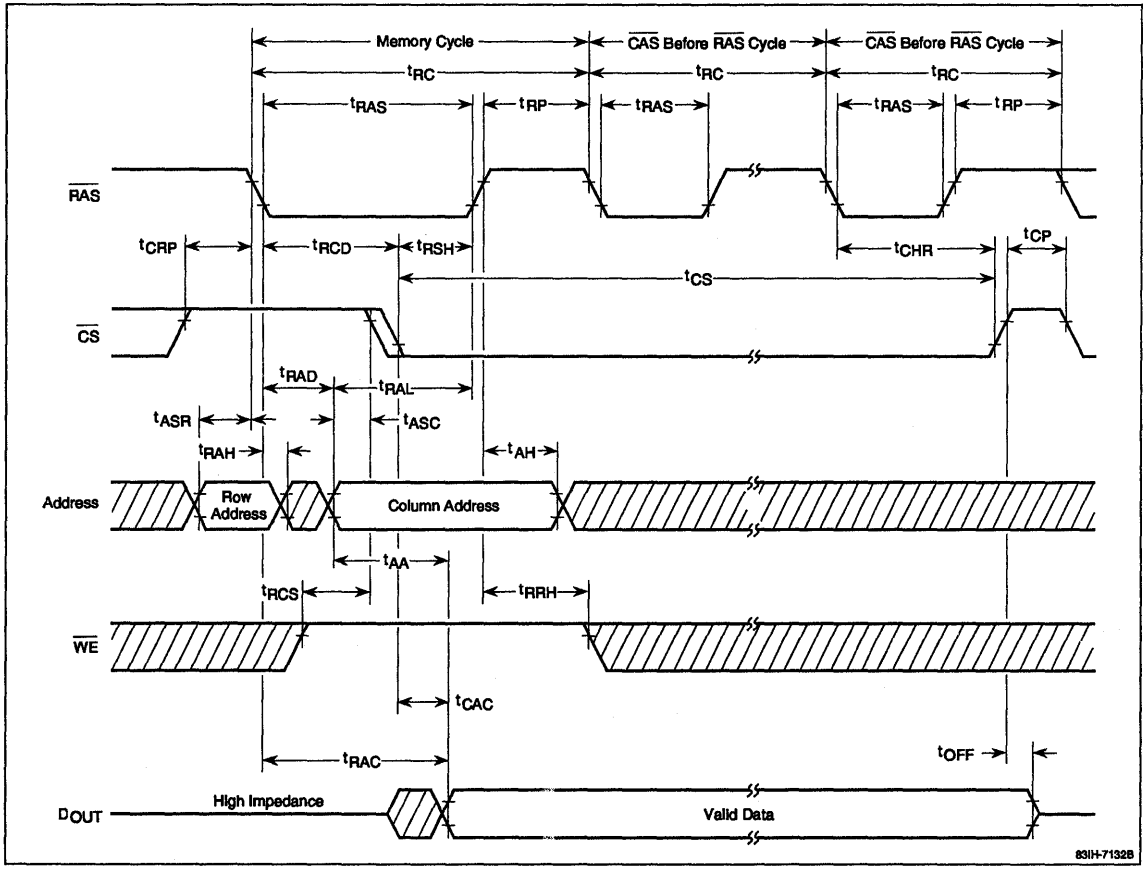
Timing Waveforms (cont)

Fast-Page Early Write Cycle



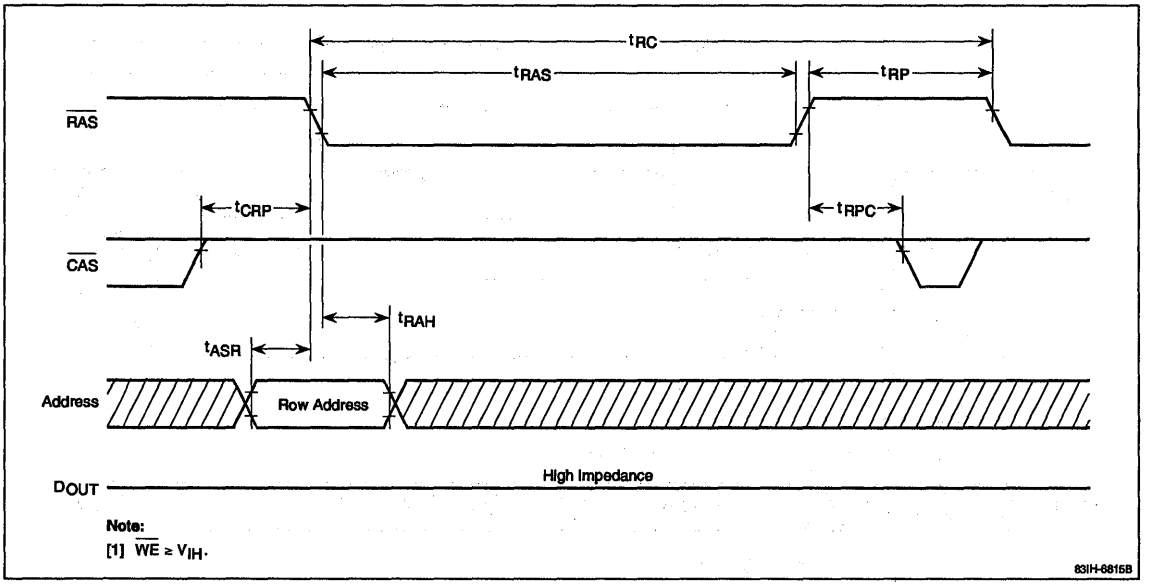
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

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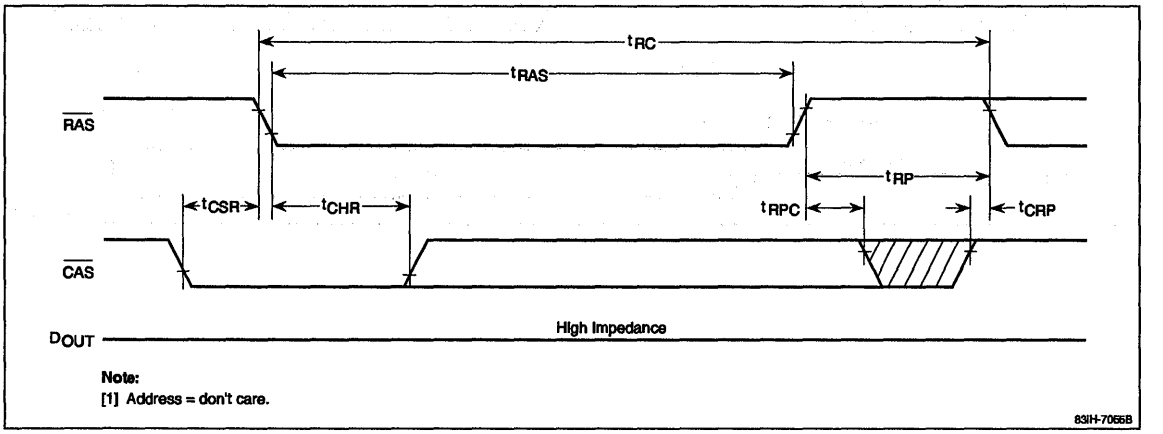
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

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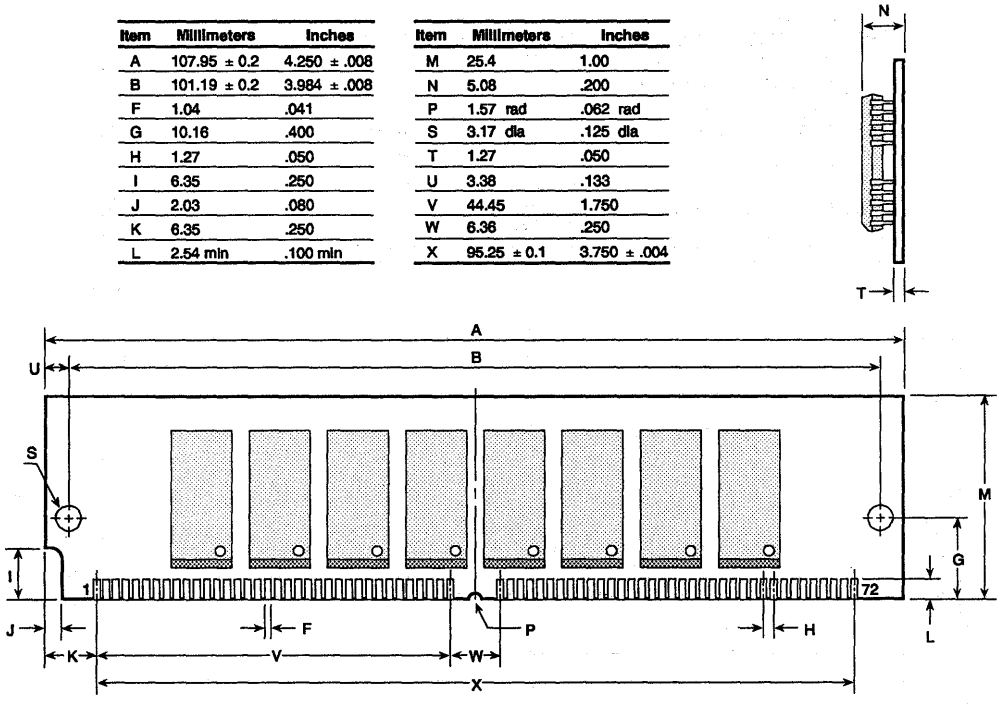
Package Drawings

72-Pin Socket-Mountable SIMM (MC-42256A32B/F)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	25.4	1.00
N	5.08	.200
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-42256A32B/F

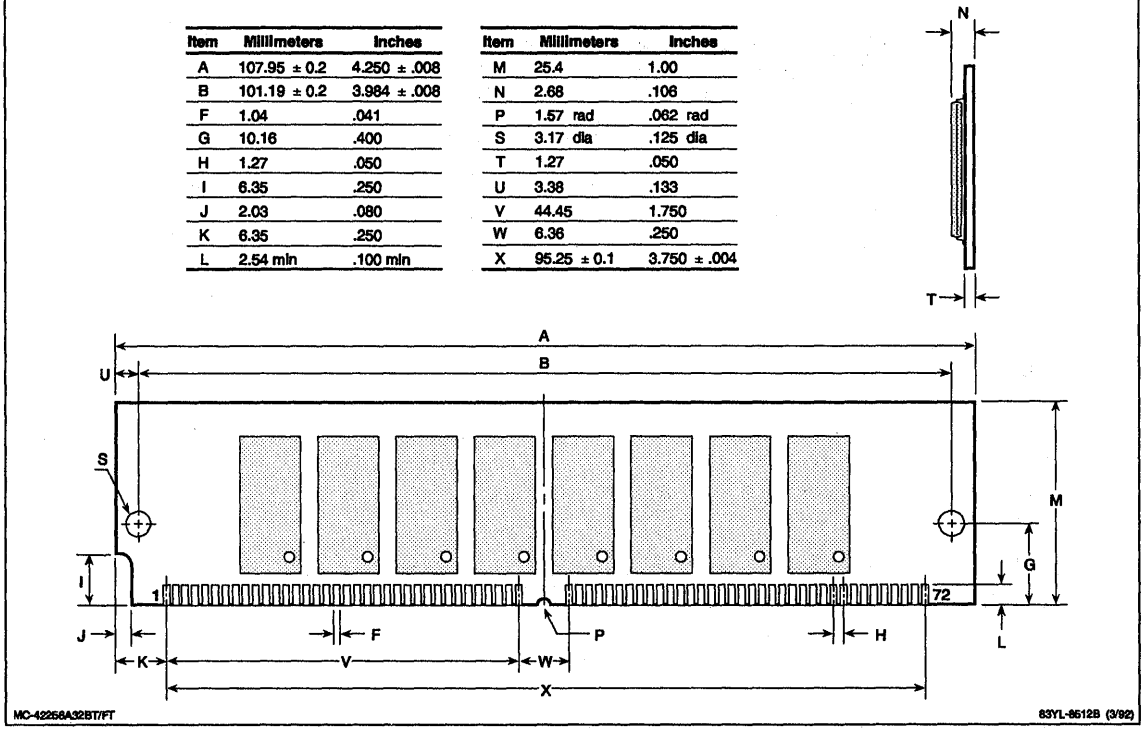
83YL-8611B (3/92)

Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-42256A32BT/FT)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	25.4	1.00
N	2.68	.106
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-42256A36, -424256A36
262,144 x 36-Bit
Dynamic CMOS RAM Module

Description

The MC-42256A36 and the MC-424256A36 are dynamic RAM modules organized as 264,144 words by 36 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 - A_8 during a 16-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight, and cost of a system. Each SIMM contains 12 DRAMs and 12 power supply decoupling capacitors. The complement of DRAMs (μPD424256, 41256, 42256, 421000) and the operating mode (fast-page, page) are summarized below.

Module	DRAMs (Qty) 256K x 4	256K x 1	1M x 1
MC-42256A36 B/F (fast-page)	(8) μPD424256	(4) μPD42256	
MC-424256A36 BH/FH (fast-page)	(8) μPD424256		(4) μPD421000
MC-424256A36 B/F (page)	(8) μPD424256	(4) μPD41256	

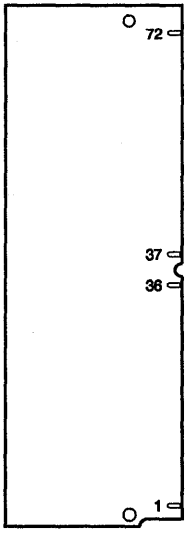
Features

- 262,144-word by 36-bit organization
- Single +5-volt power supply
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging
- Fast-page mode operation (MC-42256A36B/F and MC-424256A36BH/FH)
- Page mode operation (MC-424256A36B/F)

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{18}
4	DQ_1
5	DQ_{19}
6	DQ_2
7	DQ_{20}
8	DQ_3
9	DQ_{21}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	NC
20	DQ_4
21	DQ_{22}
22	DQ_5
23	DQ_{23}
24	DQ_6
25	DQ_{24}
26	DQ_7
27	DQ_{25}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	NC
33	NC
34	$\overline{RAS}_2$
35	DQ_{26}
36	DQ_8

Pin	Symbol
37	DQ_{17}
38	DQ_{35}
39	GND
40	$\overline{CAS}_0$
41	$\overline{CAS}_2$
42	$\overline{CAS}_3$
43	$\overline{CAS}_1$
44	$\overline{RAS}_0$
45	NC
46	NC
47	$\overline{WE}$
48	NC
49	DQ_9
50	DQ_{27}
51	DQ_{10}
52	DQ_{28}
53	DQ_{11}
54	DQ_{29}

Pin	Symbol
55	DQ_{12}
56	DQ_{30}
57	DQ_{13}
58	DQ_{31}
59	V_{CC}
60	DQ_{32}
61	DQ_{14}
62	DQ_{33}
63	DQ_{15}
64	DQ_{34}
65	DQ_{16}
66	NC
67	GND
68	NC
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

[1] Pins 69 and 70 are defined by access time:

Pin	70 ns	80/85 ns	100 ns
69	GND	NC	GND
70	NC	GND	GND

83FM-6344A

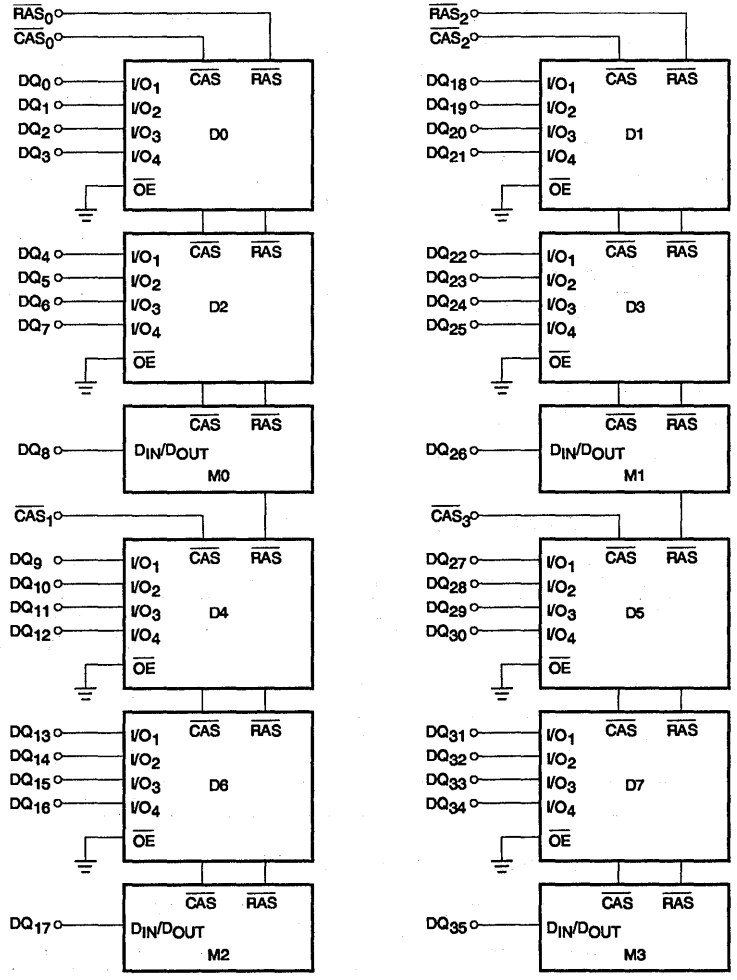
Ordering Information

Part Number	Access Time (max)	Package	Operation	Height	Thickness	DRAMs
MC-42256A36B-70	70 ns	72-pin socket-mountable SIMM (solder plating)	Fast-page	25.4 mm (1.00 inch)	5.28 mm (0.208 inch)	Eight μPD424256LA Four μPD42256L
B-80	80 ns					
B-10	100 ns					
MC-42256A36F-70	70 ns	72-pin socket-mountable SIMM (gold plating)				
F-80	80 ns					
F-10	100 ns					
MC-424256A36BH-70	70 ns	72-pin socket-mountable SIMM (solder plating)	Fast-page	31.75 mm (1.25 inch)	5.28 mm (0.208 inch)	Eight μPD424256LA Four μPD421000LA
BH-80	80 ns					
BH-10	100 ns					
MC-424256A36FH-70	70 ns	72-pin socket-mountable SIMM (gold plating)				
FH-80	80 ns					
FH-10	100 ns					
MC-424256A36B-80	80 ns	72-pin socket-mountable SIMM (solder plating)	Page	25.4 mm (1.00 inch)	5.28 mm (0.208 inch)	Eight μPD424256LA Four μPD41256L
B-85	85 ns					
B-10	100 ns					
MC-424256A36F-80	80 ns	72-pin socket-mountable SIMM (gold plating)				
F-85	85 ns					
F-10	100 ns					

Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobes
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS}_0$, $\overline{RAS}_2$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Connection Diagram; MC-42256A36, -424256A36



Desig	DRAM	Used On
D0-D7	μPD424256LA	All
M0-M3	μPD421000LA	MC-424256A36BH/FH
	μPD42256LA	MC-42256A36B/F
	μPD41256L	MC-424256A36B/F

83IH-8346B

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	24 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	88	pF	A_0 - A_8
	C_{I2}	104	pF	$\overline{WE}$
	C_{I3}	57	pF	$\overline{RAS}$
	C_{I4}	36	pF	$\overline{CAS}$
Input/output capacitance	C_{I0}/C_{O0}	17	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	22	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

DC Characteristics 1 (MC-42256A36B/F, -424256A36BH/FH)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			12	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−120	120	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics 1 (MC-42256A36B/F, -424256A36BH/FH)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (Note 17)		960		840		720	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC1} (Note 18)		920		800		680	mA	
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (Note 17)		960		840		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC3} (Note 18)		920		800		680	mA	
Operating current, fast-page cycle, average	I_{CC4} (Note 17)		840		720		600	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
	I_{CC4} (Note 18)		800		680		560	mA	
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (Note 17)		960		840		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC5} (Note 18)		920		800		560	mA	
Access time from column address	t_{AA}		35		45		50	ns	(Notes 7, 9)

AC Characteristics 1 (MC-42256A36B/F, -424256A36BH/FH) (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		60		70		ns	
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10	20	10	20	10	25	ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		20		20		ns	(Note 15)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	35	17	45	ns	(Note 9)
Row address hold time	t_{RAH}	10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	35		45		55		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	

AC Characteristics 1 (MC-42256A36B/F, -424256A36BH/FH) (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		20		ns	
Write command pulse width	t_{WP}	15		15		20		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle.

If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) MC-424256A36BH/FH

(18) MC-42256A36B/F

DC Characteristics 2 (MC-424256A36B/F)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		36	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$ (min)
			8	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V
Input leakage current	$I_{I(L)}$	–120	120	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics 2 (MC-424256A36B/F)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-80		-85		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		960		808		680	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		960		808		680	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		916		764		660	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		960		808		680	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		55		65		ns	
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		40		40		50	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	20		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10,000	40	10,000	50	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{CAS}$ precharge time	t_{CP}	20		20		40		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	80		85		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	20		20		25		ns	(Note 15)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		65		75		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	20	0	20	0	25	ns	(Note 10)
Access time from $\overline{RAS}$	t_{RAC}		80		85		100	ns	(Notes 7, 8)
Row address hold time	t_{RAH}	12		12		12		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	85	10,000	100	10,000	ns	
Random read or write cycle time	t_{RC}	160		165		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	45	20	50	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	70		70		90		ns	

AC Characteristics 2 (MC-424256A36B/F) (cont)

Parameter	Symbol	-80 Min	-80 Max	-85 Min	-85 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	40		40		50		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	20		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		65		75		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

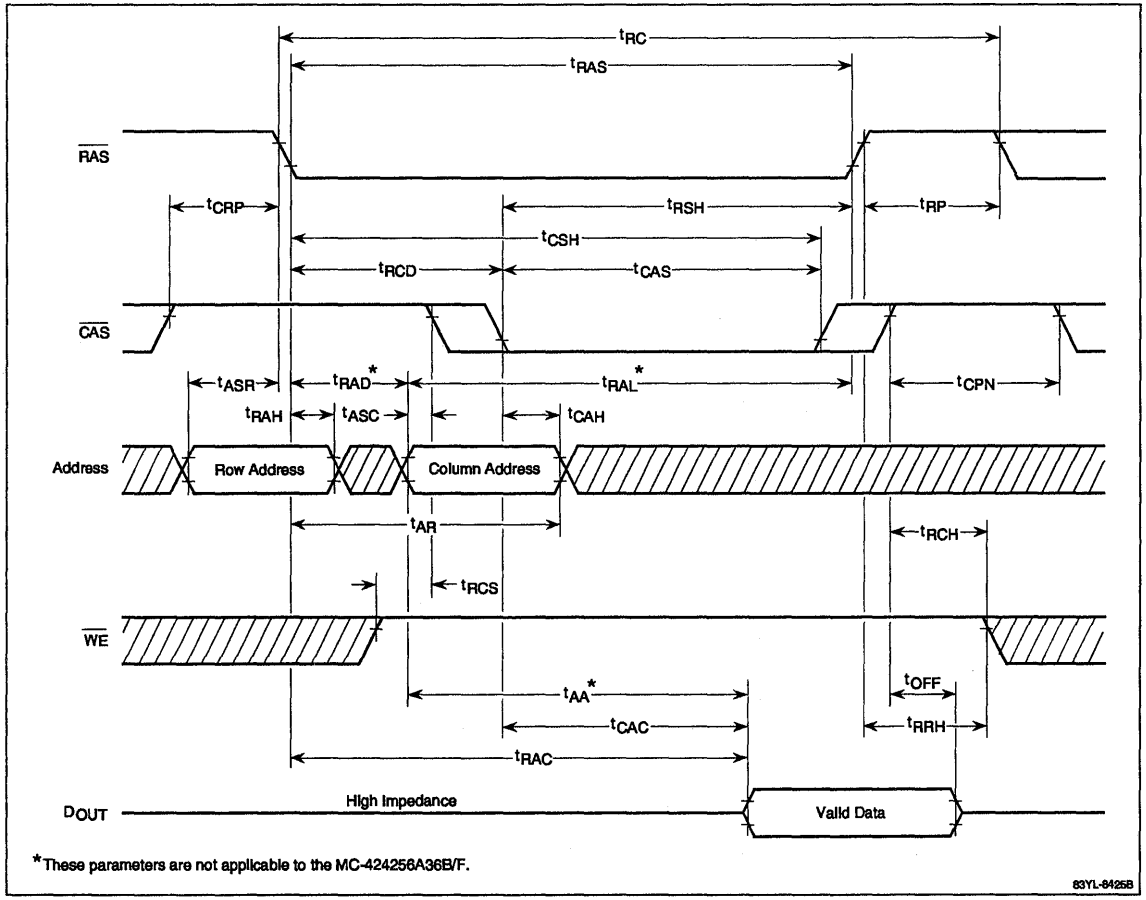
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle.

If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

Timing Waveforms

Read Cycle

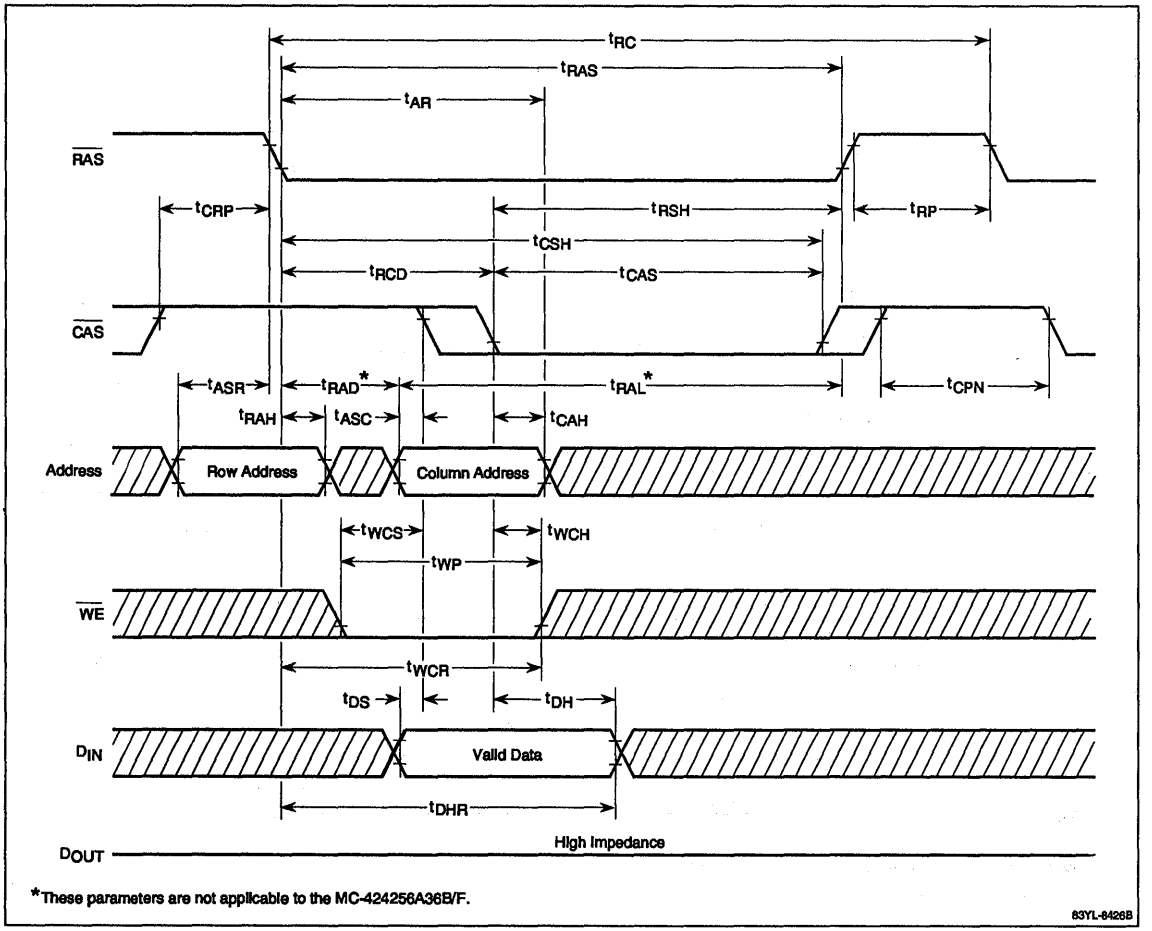


*These parameters are not applicable to the MC-424256A36B/F.

83YL-84258

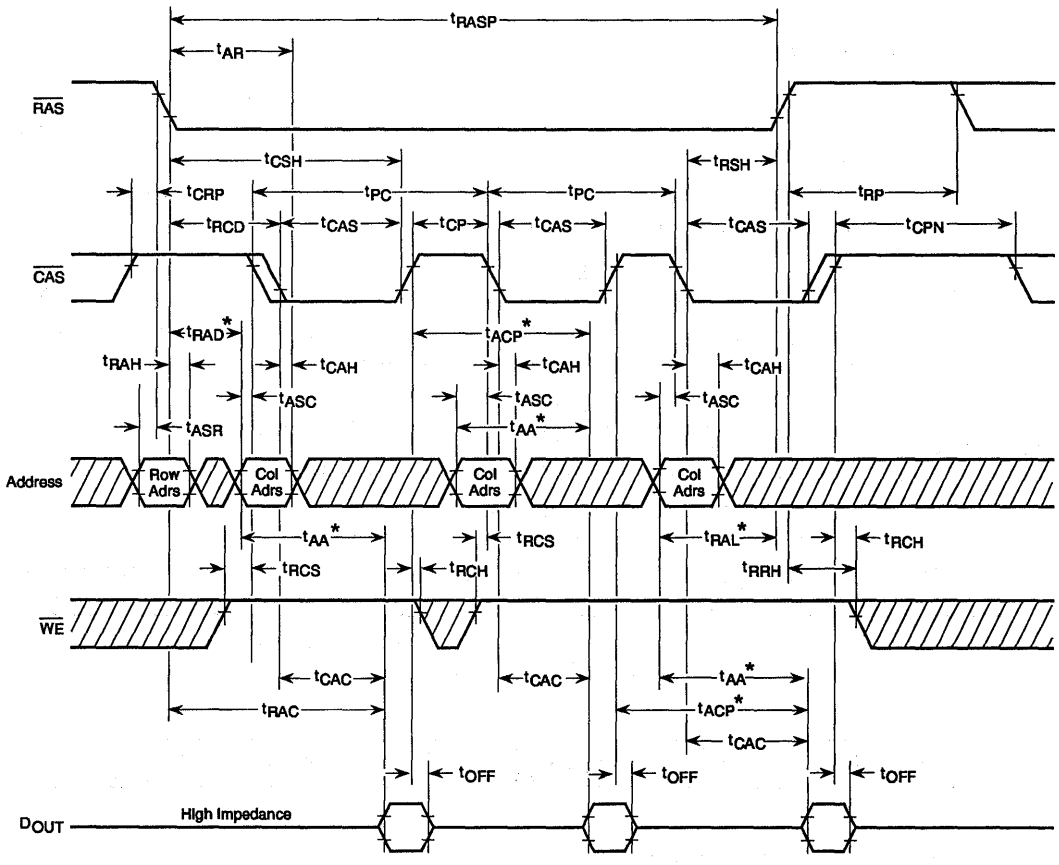
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Page/Fast-Page Read Cycle



*These parameters are not applicable to the MC-424256A36B/F.

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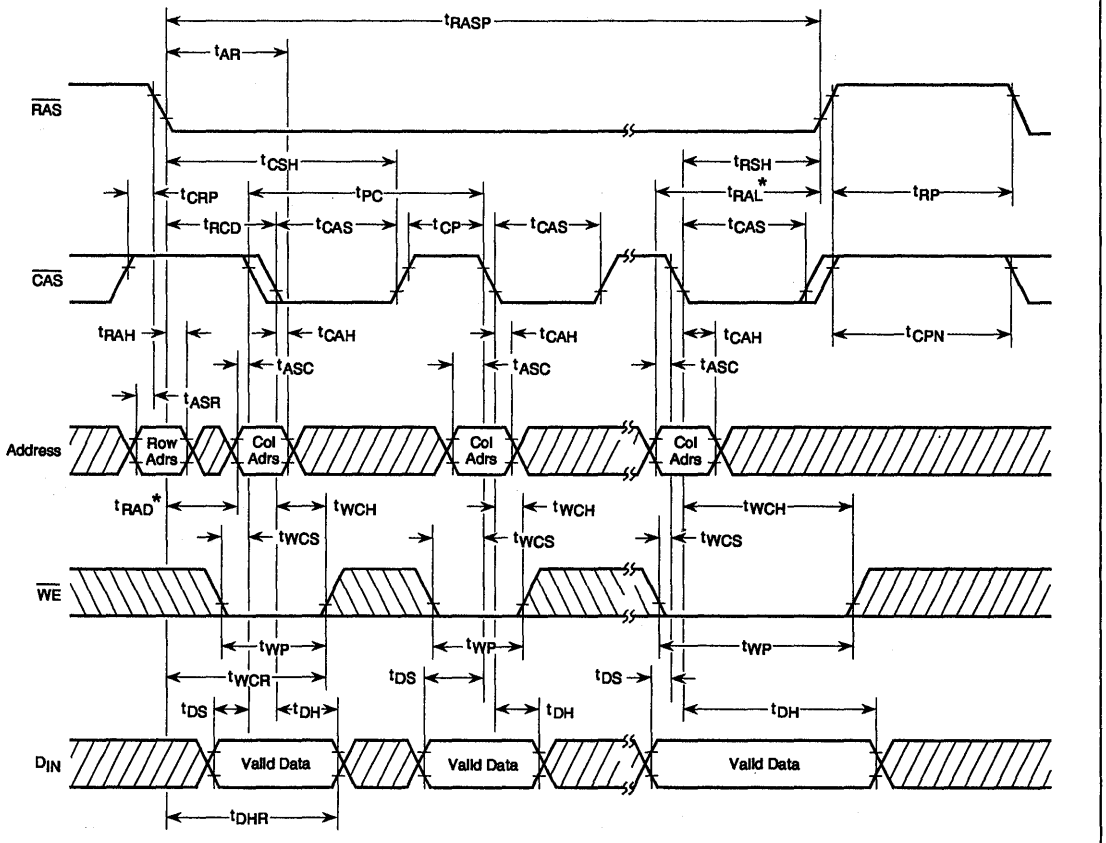
Timing Waveforms (cont)

Page/Fast-Page Early Write Cycle

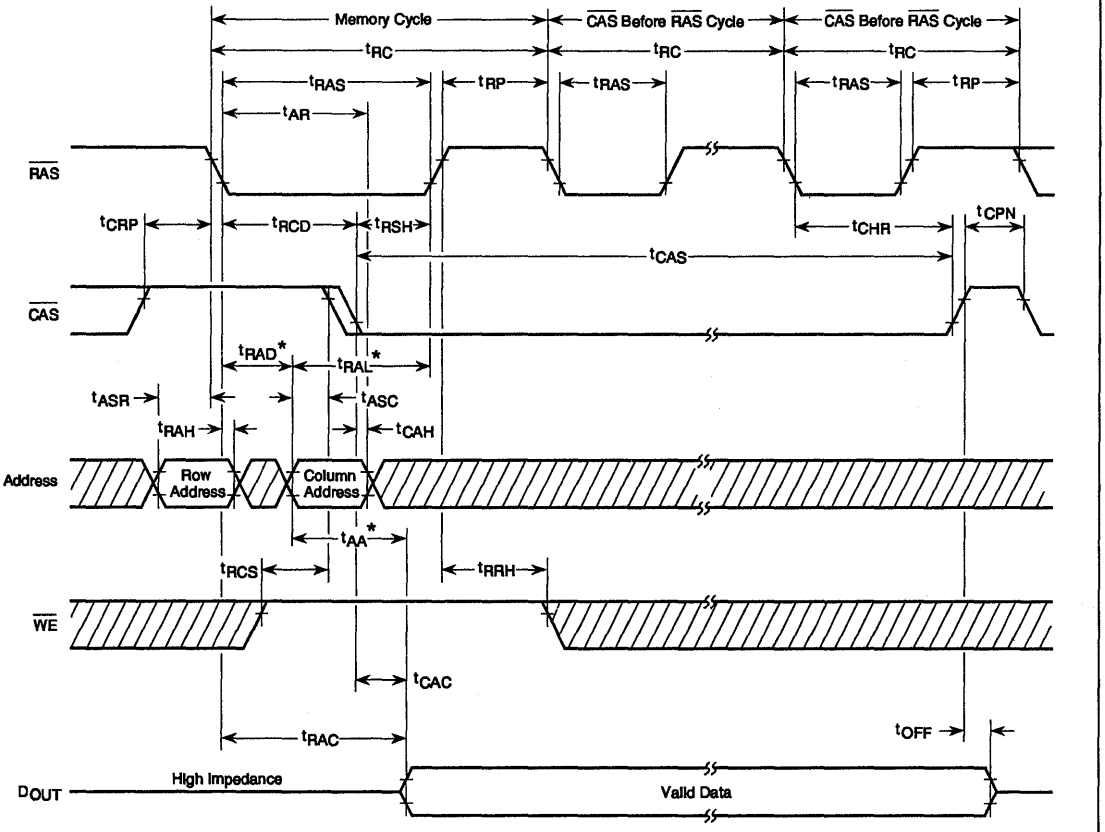


*These parameters are not applicable to the MC-424256A36B/F.

83YL-8428B

Timing Waveforms (cont)

Hidden Refresh Cycle

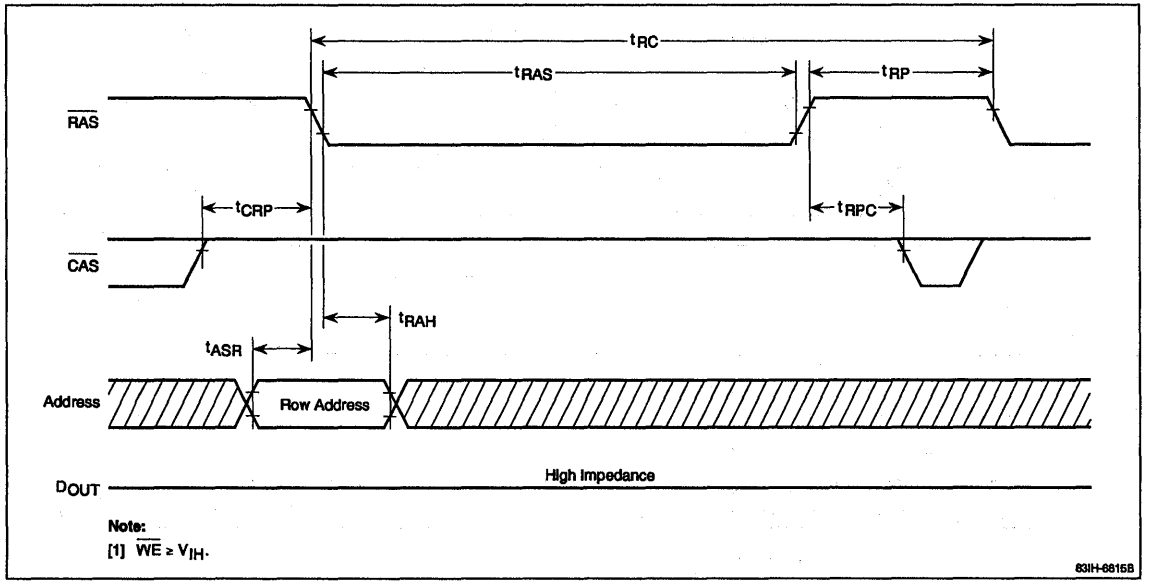


*These parameters are not applicable to the MC-424256A36.

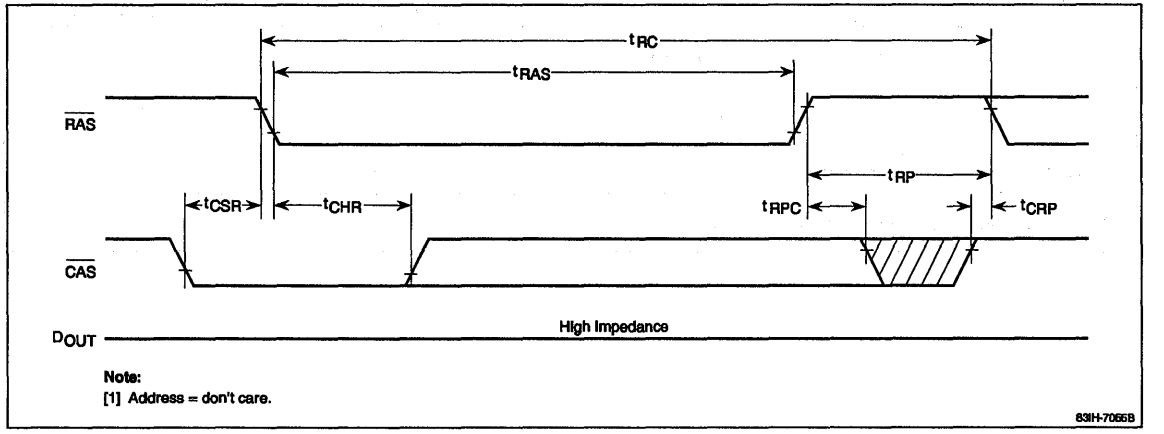
83YL-6429B

Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



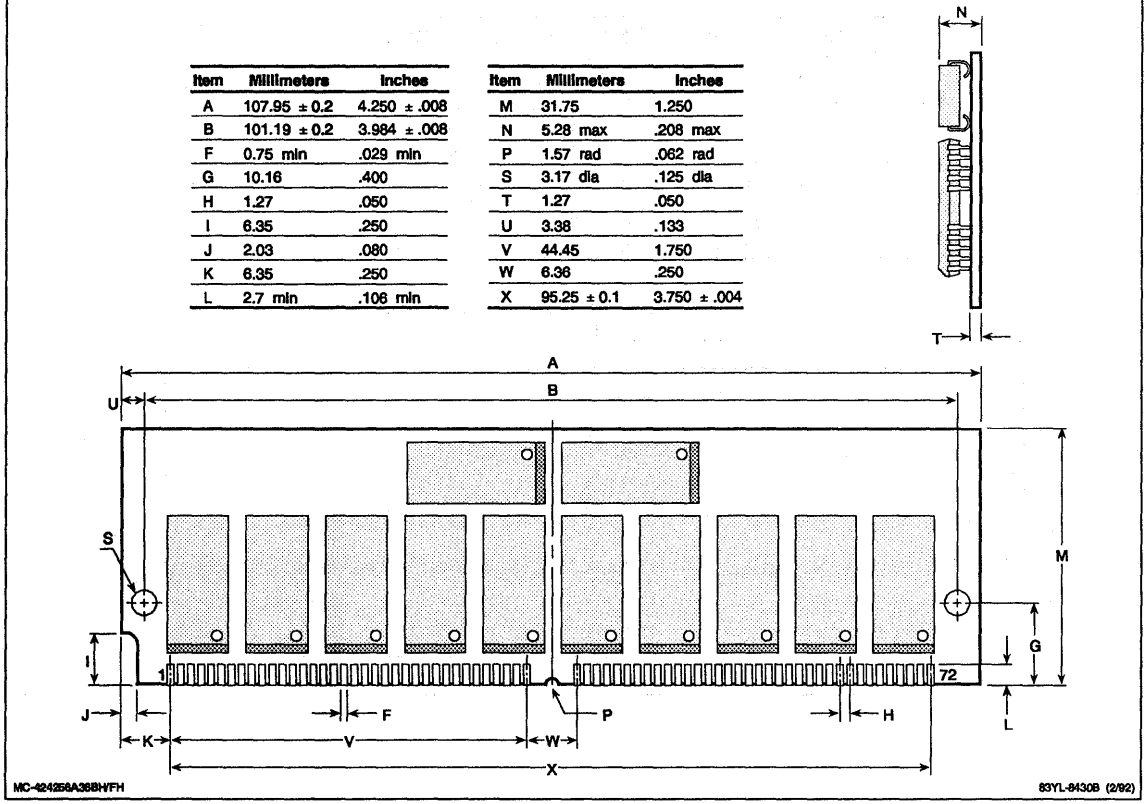
9d

Package Drawings

72-Pin Socket-Mountable SIMM (MC-424256A36BH/FH)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	31.75	1.250
N	5.28 max	.208 max
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004

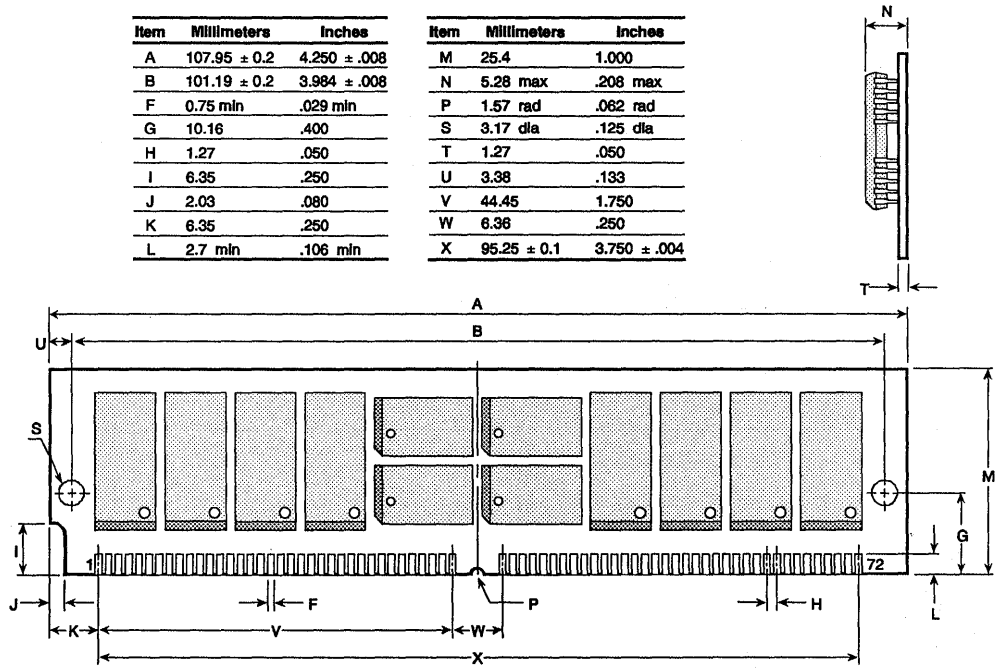


Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-42256A36B/F and MC-424256A36B/F)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	5.28 max	.208 max
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-42256A36B/F, -424256A36B/F

83YL-8431B (2/92)

MC-42256AA40
262,144 x 40-Bit
Dynamic CMOS RAM Module

Description

The MC-42256AA40 is a fast-page dynamic RAM module organized as 262,144 words by 40 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 512 address combinations of A_0 - A_8 during an 8-ms period.

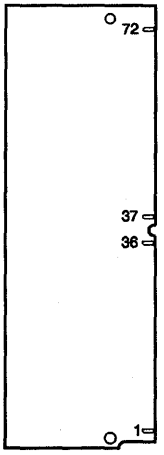
Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. Each SIMM contains ten 262,144 x 4-bit μPD424256 DRAMs in SOJ packages, and ten power supply decoupling capacitors for noise reduction. DQ_0 through DQ_{39} are common input/output pins.

Features

- 262,144-word by 40-bit organization
- Single +5-volt power supply
- Fast-page cycles
- Low power dissipation (55 mW max in standby)
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 512 refresh cycles every 8 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

Pin Configuration

72-Pin SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{16}
4	DQ_1
5	DQ_{17}
6	DQ_2
7	DQ_{18}
8	DQ_3
9	DQ_{19}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	$\overline{OE}$
20	DQ_4
21	DQ_{20}
22	DQ_5
23	DQ_{21}
24	DQ_6
25	DQ_{22}
26	DQ_7
27	DQ_{23}
28	A_7
29	DQ_{36}
30	V_{CC}
31	A_8
32	NC
33	NC
34	NC
35	DQ_{34}
36	DQ_{32}

Pin	Symbol
37	DQ_{33}
38	DQ_{35}
39	GND
40	$\overline{CAS}_0$
41	NC
42	NC
43	NC
44	$\overline{RAS}_0$
45	NC
46	DQ_{37}
47	$\overline{WE}$
48	GND
49	DQ_8
50	DQ_{24}
51	DQ_9
52	DQ_{25}
53	DQ_{10}
54	DQ_{26}

Pin	Symbol
55	DQ_{11}
56	DQ_{27}
57	DQ_{12}
58	DQ_{28}
59	V_{CC}
60	DQ_{29}
61	DQ_{13}
62	DQ_{30}
63	DQ_{14}
64	DQ_{31}
65	DQ_{15}
66	DQ_{38}
67	NC
68	GND
69	Note 1
70	Note 1
71	DQ_{39}
72	GND

Notes:

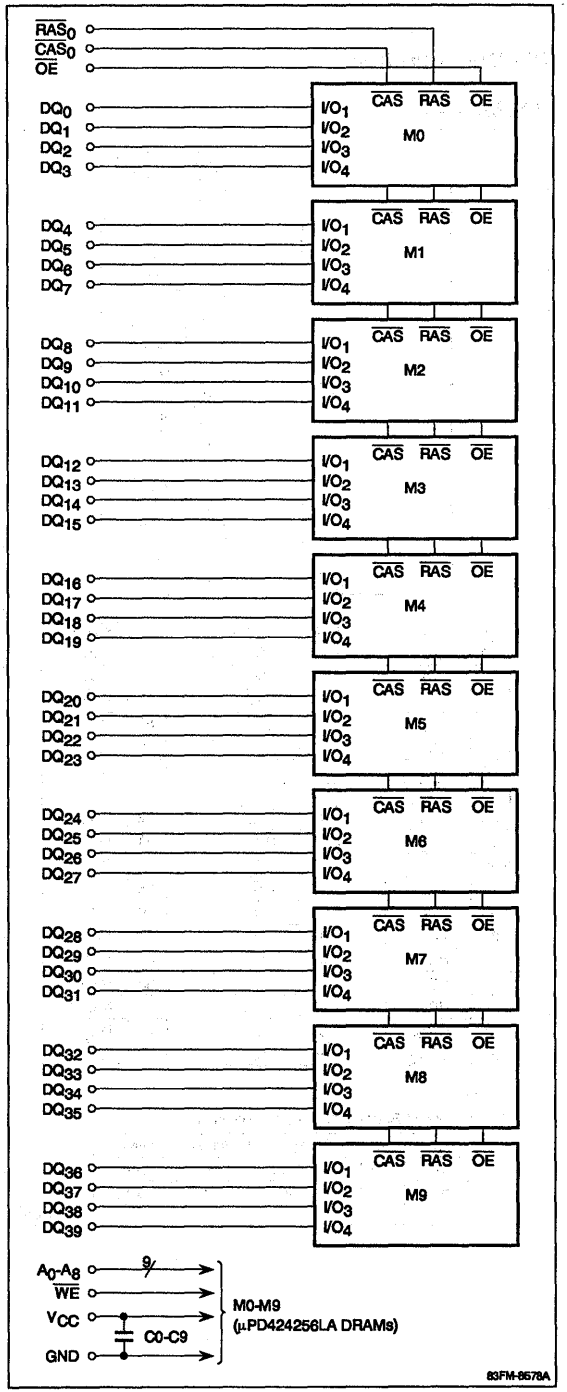
[1] Pins 69 and 70 are defined by access time:

Pin	60 ns	70 ns	80 ns	100 ns
69	NC	GND	NC	GND
70	NC	NC	GND	GND

83FM-8579A

SIMM is a trademark of Wang Laboratories.

Connection Diagram



Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}_0$	Column address strobe
DQ_0 - DQ_{39}	Common data inputs/outputs
$\overline{OE}$	Output enable
$\overline{RAS}_0$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-42256AA40B-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.000 inch)	5.08 mm (0.200 inch)	Ten μPD424256LA
B-70	70 ns				
B-80	80 ns				
B-10	100 ns				
MC-42256AA40F-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				
F-10	100 ns				

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	10 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	65	pF	A_0 - A_8
	C_{I2}	70	pF	$\overline{WE}$, $\overline{OE}$
	C_{I3}	60	pF	$\overline{RAS}$
	C_{I4}	60	pF	$\overline{CAS}$
Input/output capacitance	C_{IO}/C_{OO}	12	pF	DQ_0 - DQ_{39}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		20	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			10	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–100	100	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	DQ_0 to DQ_{39} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		900		800		700		600	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		900		800		700		600	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		800		700		600		500	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		900		800		700		600	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IL}; t_{RC} = t_{RC} min; (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10, 13)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		40		55	ns	(Notes 7, 13)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		60		60		70		ns	
Column address setup time	t_{ASC}	0	20	0	20	0	20	0	20	ns	(Note 13)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		65		80		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10, 13)
Column address hold time	t_{CAH}	15		16		16		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10	15	10	20	10	25	ns	(Note 13)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 14)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		55		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		60		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 17)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Fast-page read-write cycle time	t_{PRWC}	85		90		105		125		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	45	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		55		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 15)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8; 64 ms for -L versions
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 15)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	165		175		215		255		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		130		ns	(Note 18)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	50		55		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 18)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 16)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(12) Operation with the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(13) For fast-page read operation, the definition of access time is as follows:

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq$ CP (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq$ CP (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq$ CP (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

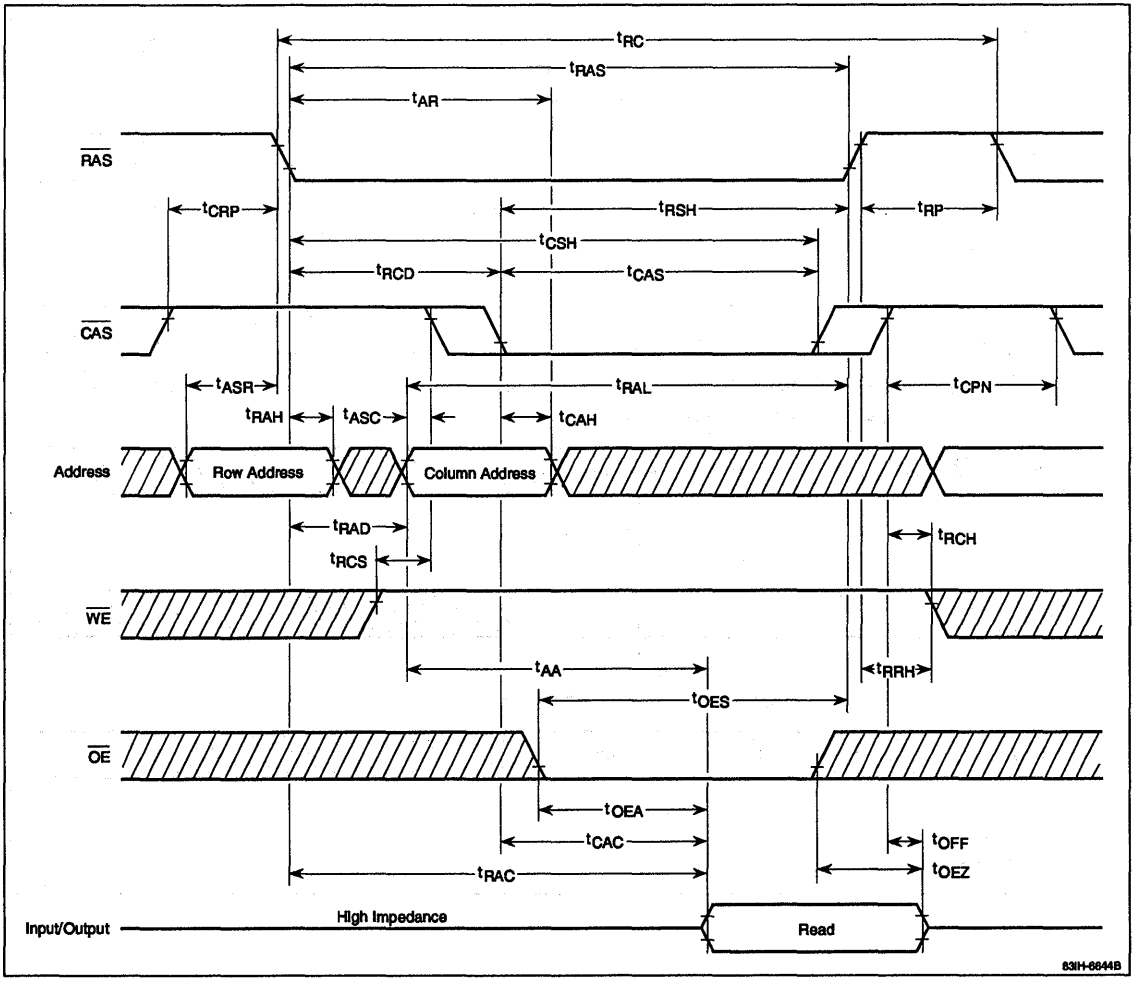
(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until CAS returns to V_{IH}) is indeterminate.

9e

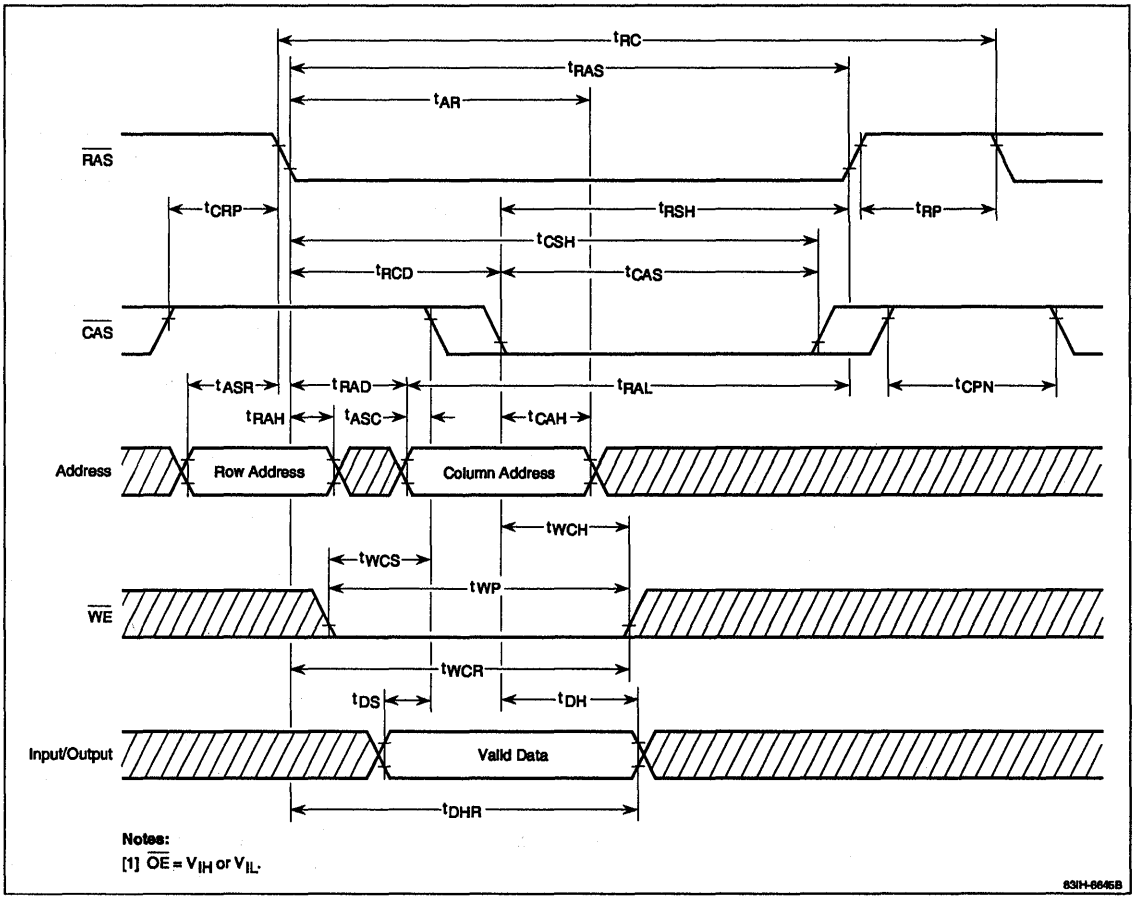
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

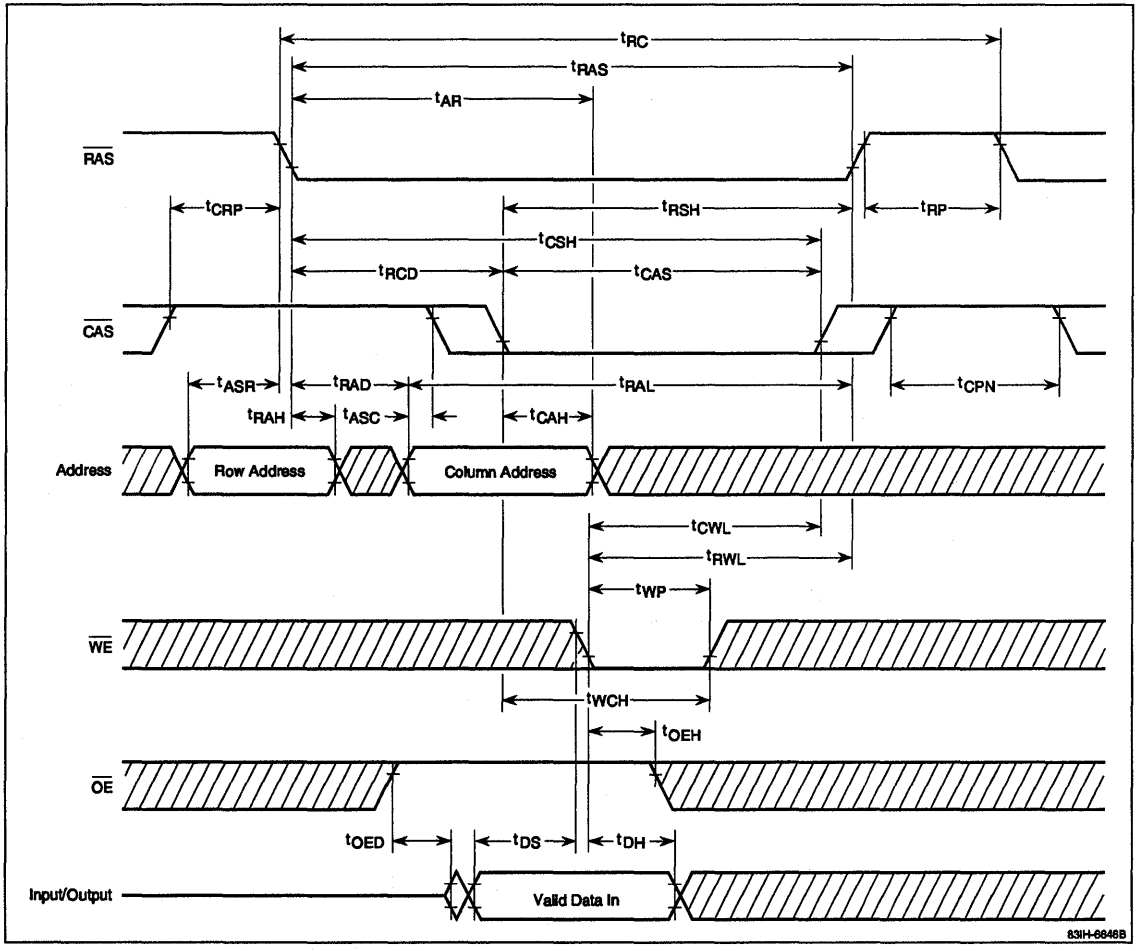
Early Write Cycle



9e

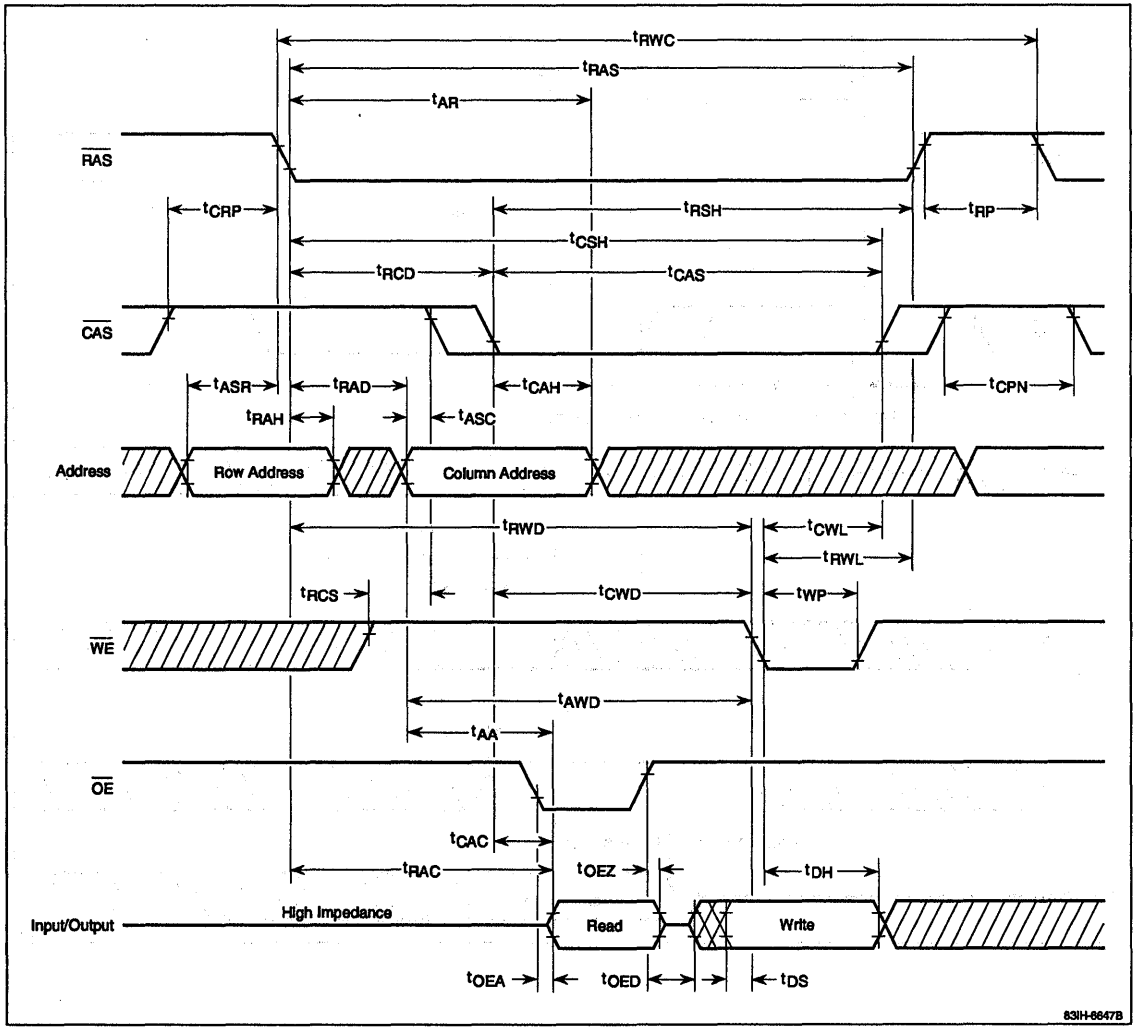
Timing Waveforms (cont)

$\overline{OE}$-Controlled Write Cycle



Timing Waveforms (cont)

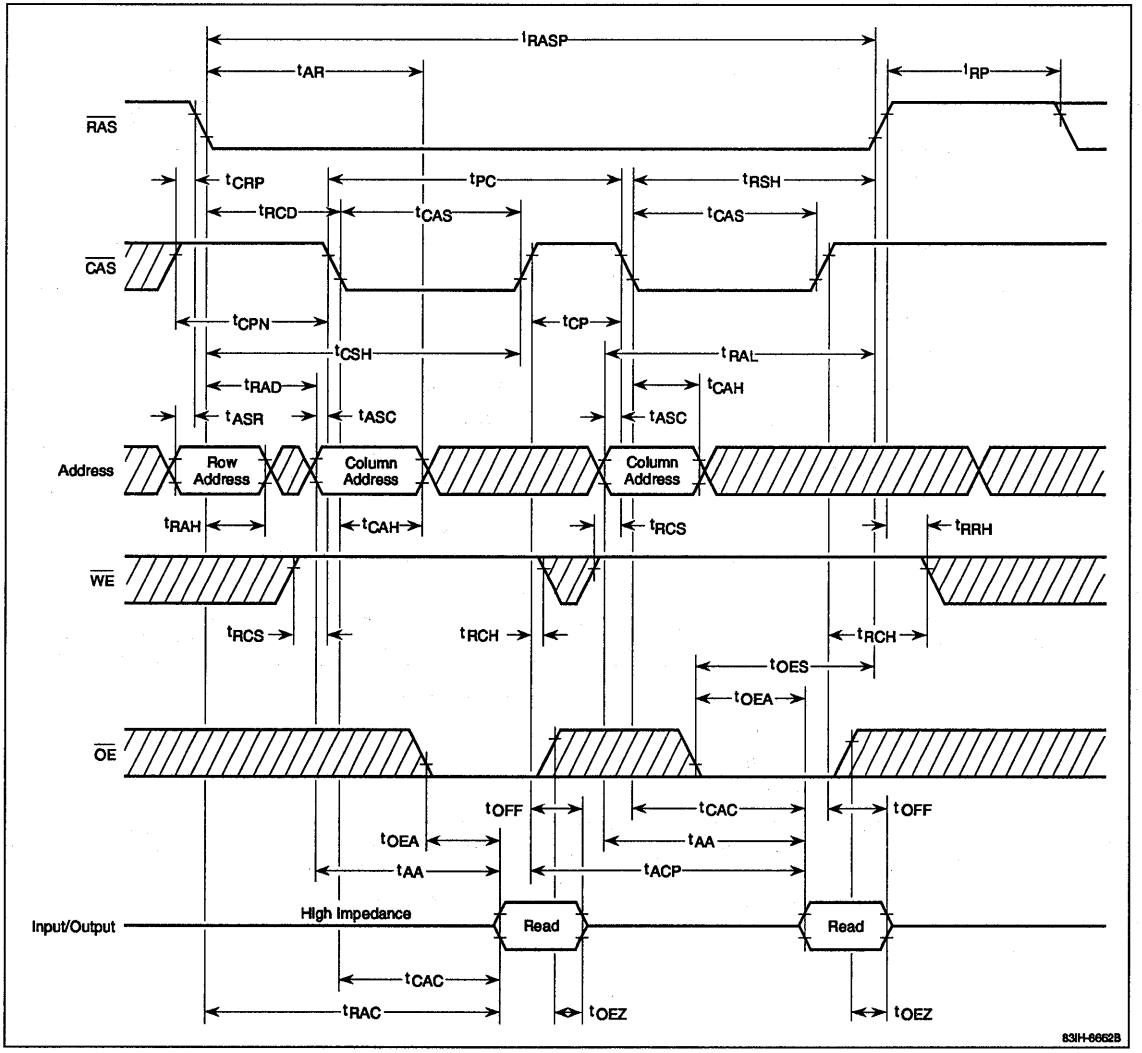
Read-Write/Read-Modify-Write Cycle



9e

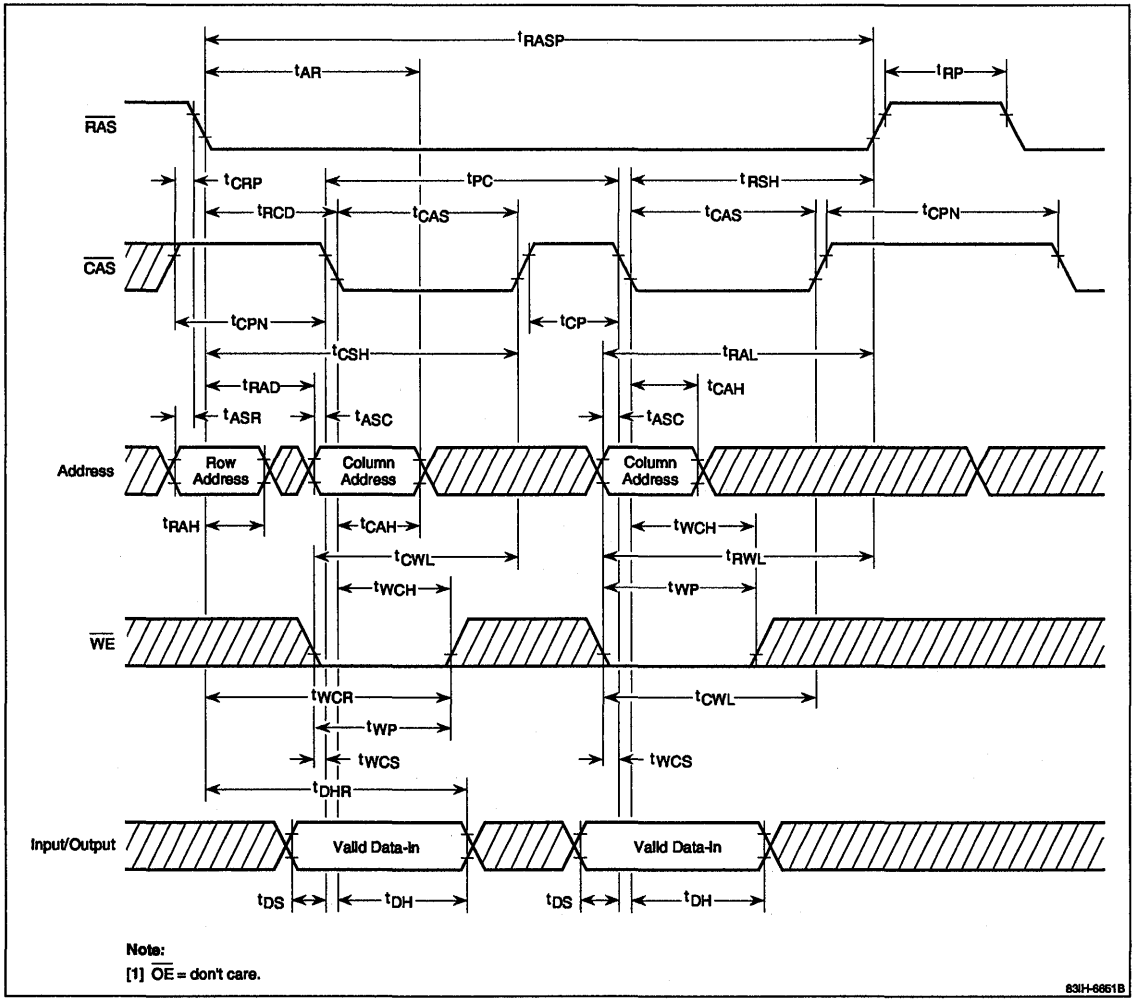
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



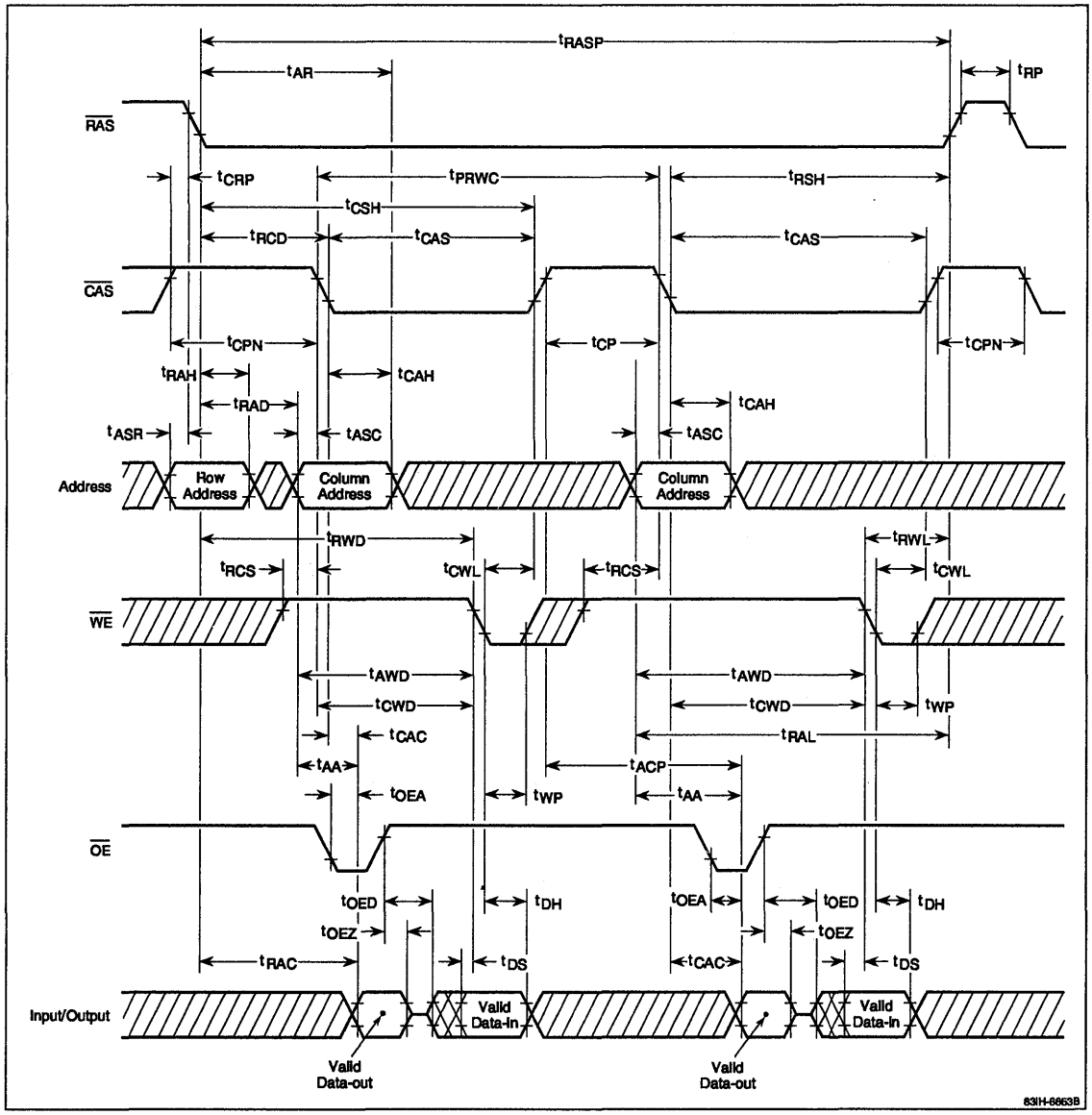
Note:
[1] $\overline{OE}$ = don't care.

83IH-6661B

9e

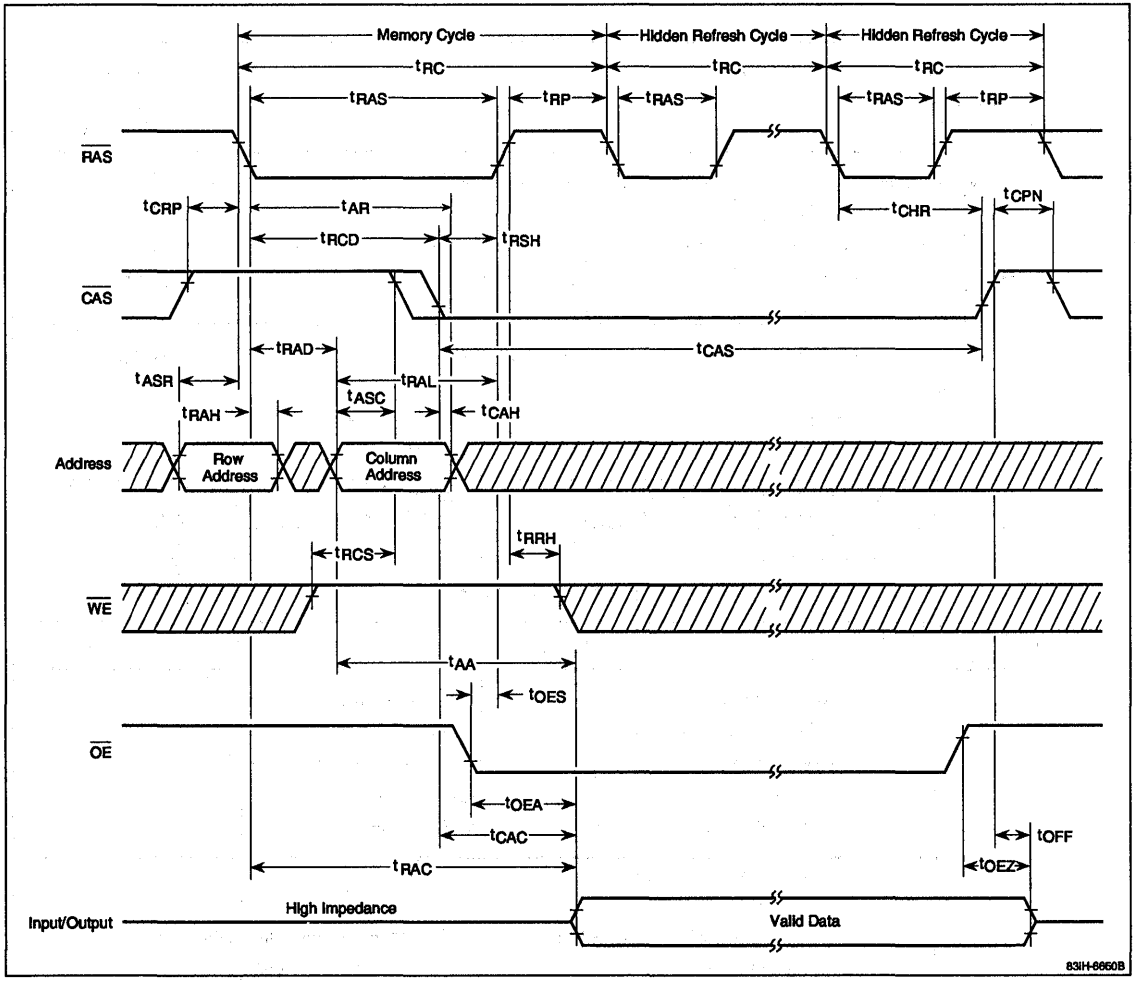
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

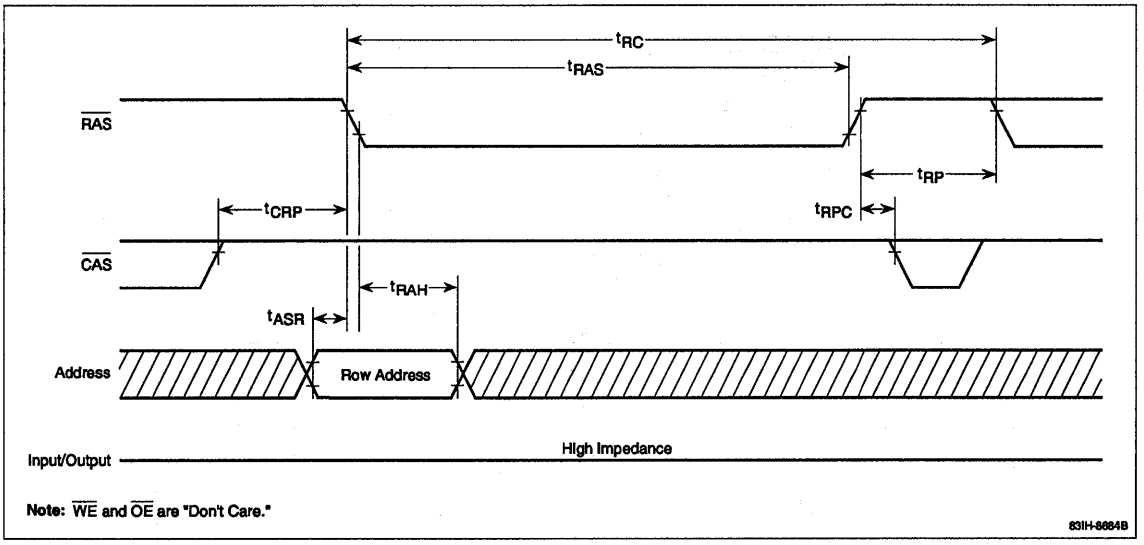
Hidden Refresh Cycle



9e

Timing Waveforms (cont)

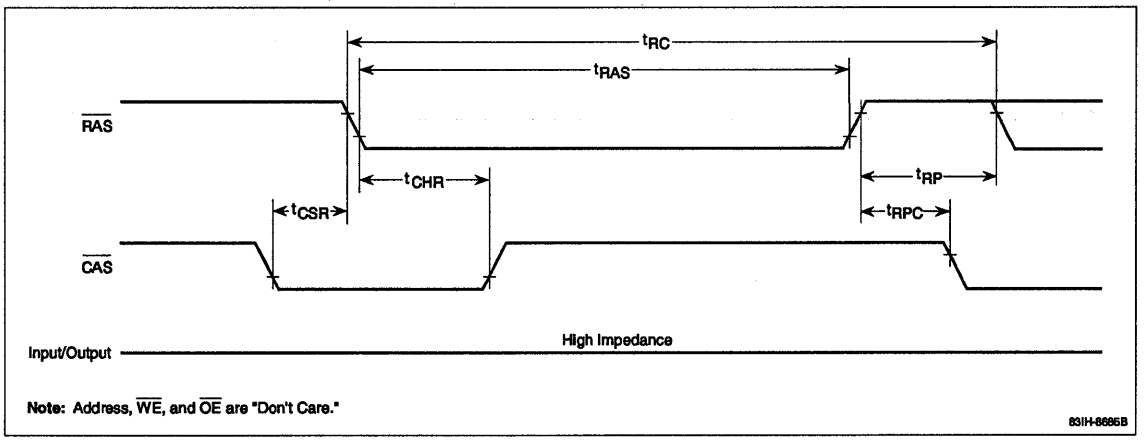
$\overline{RAS}$-Only Refresh Cycle



Note: $\overline{WE}$ and $\overline{OE}$ are "Don't Care."

83IH-8664B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



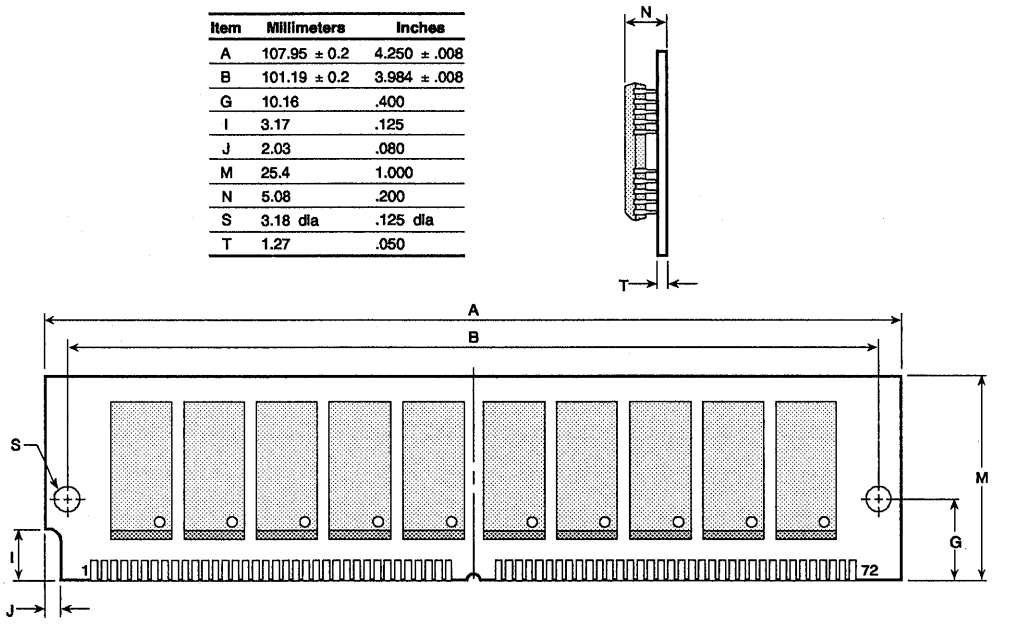
Note: Address, $\overline{WE}$, and $\overline{OE}$ are "Don't Care."

83IH-8666B

Package Drawing

72-Pin Socket-Mountable SIMM (MC-42256AA40B/F)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
G	10.16	.400
I	3.17	.125
J	2.03	.080
M	25.4	1.000
N	5.08	.200
S	3.18 dia	.125 dia
T	1.27	.050



MC-42256AA40 B/F

83FM-8677B (4/92)

MC-42512A32
524,288 x 32-Bit
Dynamic CMOS RAM Module

Description

The MC-42512A32 is a fast-page dynamic RAM module organized as 524,288 words by 32 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 512 address combinations of A_0-A_8 during an 8-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. Each SIMM contains sixteen 262,144 x 4-bit μPD424256s in SOJ packages and sixteen power supply decoupling capacitors for noise reduction. DQ_1 through DQ_{32} are common input/output pins.

Features

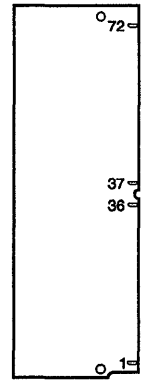
- 524,288-word by 32-bit organization
- Single +5-volt power supply
- Fast-page cycles
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 512 refresh cycles every 8 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS_0}$ - $\overline{CAS_3}$	Column address strobes
DQ_1 - DQ_{32}	Common data inputs/outputs
$\overline{RAS_0}$ - $\overline{RAS_3}$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configuration

72-Pin SIMM



Pin	Symbol
1	GND
2	DQ_1
3	DQ_{17}
4	DQ_2
5	DQ_{18}
6	DQ_3
7	DQ_{19}
8	DQ_4
9	DQ_{20}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	NC
20	DQ_5
21	DQ_{21}
22	DQ_6
23	DQ_{22}
24	DQ_7
25	DQ_{23}
26	DQ_8
27	DQ_{24}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	NC
33	$\overline{RAS_3}$
34	$\overline{RAS_2}$
35	NC
36	NC

Pin	Symbol
37	NC
38	NC
39	GND
40	$\overline{CAS_0}$
41	$\overline{CAS_2}$
42	$\overline{CAS_3}$
43	$\overline{CAS_1}$
44	$\overline{RAS_0}$
45	$\overline{RAS_1}$
46	NC
47	$\overline{WE}$
48	NC
49	DQ_9
50	DQ_{25}
51	DQ_{10}
52	DQ_{26}
53	DQ_{11}
54	DQ_{27}

Pin	Symbol
55	DQ_{12}
56	DQ_{28}
57	DQ_{13}
58	DQ_{29}
59	V_{CC}
60	DQ_{30}
61	DQ_{14}
62	DQ_{31}
63	DQ_{15}
64	DQ_{32}
65	DQ_{16}
66	NC
67	NC
68	GND
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

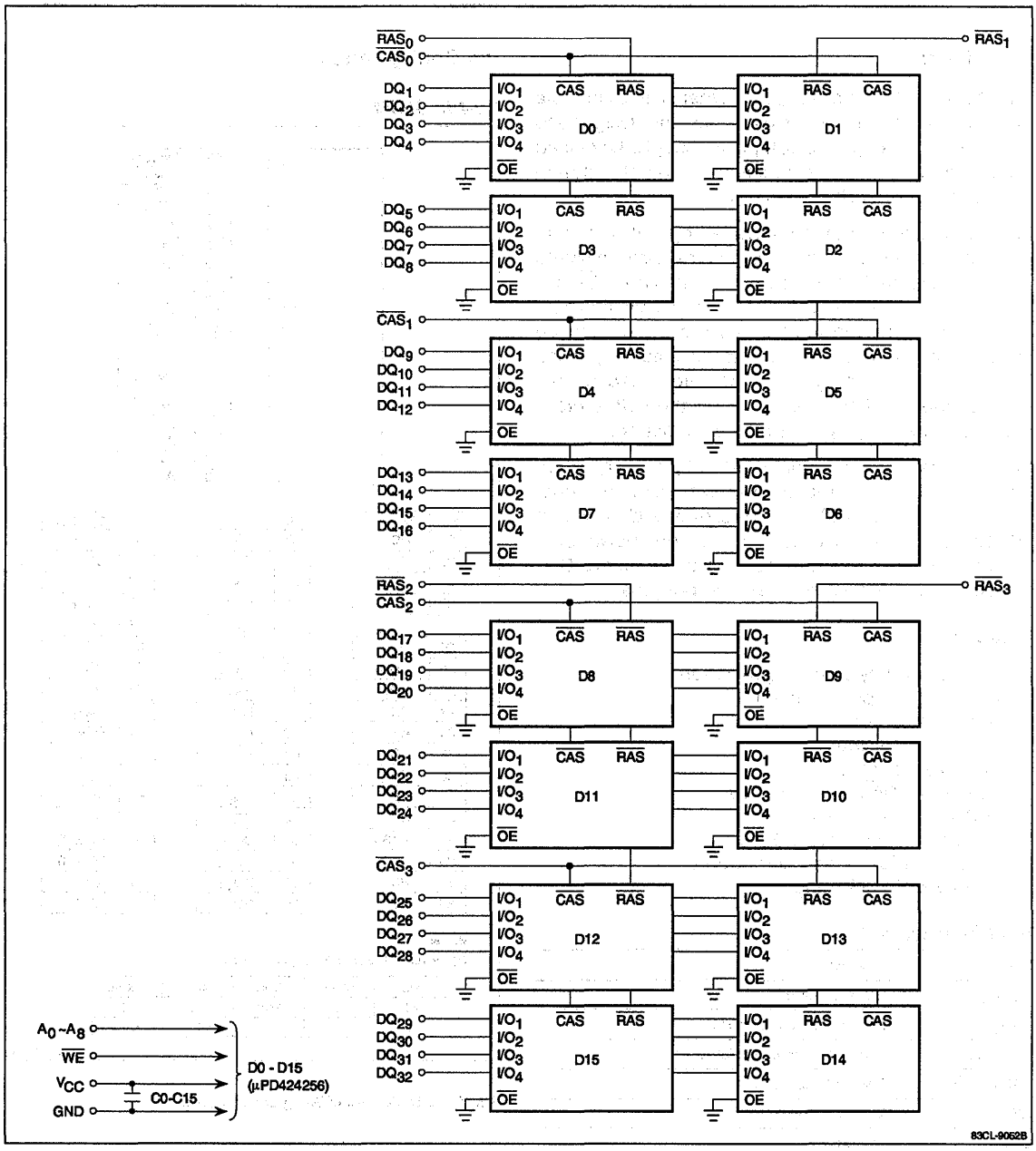
[1] Pins 69 and 70 are defined by access time:

Pin	60 ns	70 ns	80 ns	100 ns
69	NC	GND	NC	GND
70	NC	NC	GND	GND

83CL-9051A

SIMM is a trademark of Wang Laboratories.

MC-42152A32 Connection Diagram



Ordering Information

Part Number	Access Time (max)	Package	Height (typ)	Thickness (typ)	DRAMs
MC-42512A32B-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.000 inch)	9.0 mm (0.354 inch)	Sixteen μPD424256LA
B-70	70 ns				
B-80	80 ns				
B-10	100 ns				
MC-42512A32F-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				
F-10	100 ns				
MC-42512A32BT-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.000 inch)	4.1 mm (0.161 inch)	Sixteen μPD424256GX
BT-70	70 ns				
BT-80	80 ns				
BT-10	100 ns				
MC-42512A32FT-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FT-70	70 ns				
FT-80	80 ns				
FT-10	100 ns				

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	16 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	161	pF	A_0 - A_8
	C_{I2}	193	pF	$\overline{WE}$
	C_{I3}	62	pF	$\overline{RAS}$
	C_{I4}	62	pF	$\overline{CAS}$
Input/output capacitance	C_{I0}/C_{O0}	29	pF	DQ_1 - DQ_{32}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		32	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			16	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–160	160	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	DQ_1 to DQ_{32} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-60		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		780		700		620		540	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		780		700		620		540	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, page cycle, average	I_{CC4}		640		620		540		460	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		780		700		620		540	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40		55	ns	(Notes 7, 9)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		60		60		70		ns	
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		10		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
Data-in hold time	t_{DH}	15		15		20		25		ns	(Note 15)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		60		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0		0	15	0	20	0	25	ns	(Note 10)
Page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	35	17	40	17	45	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		55		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, page cycle	t_{RASP}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	50	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		55		55		70		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

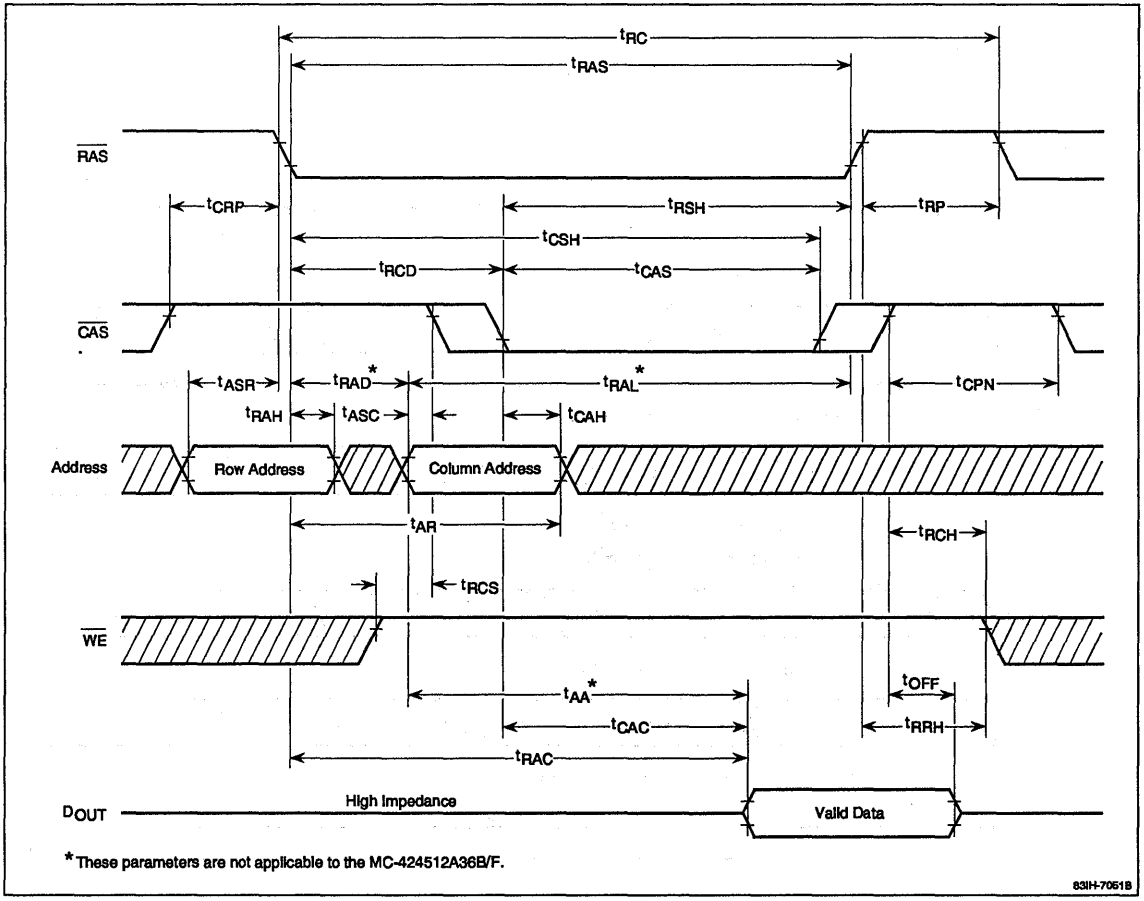
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

9f

Timing Waveforms

Read Cycle

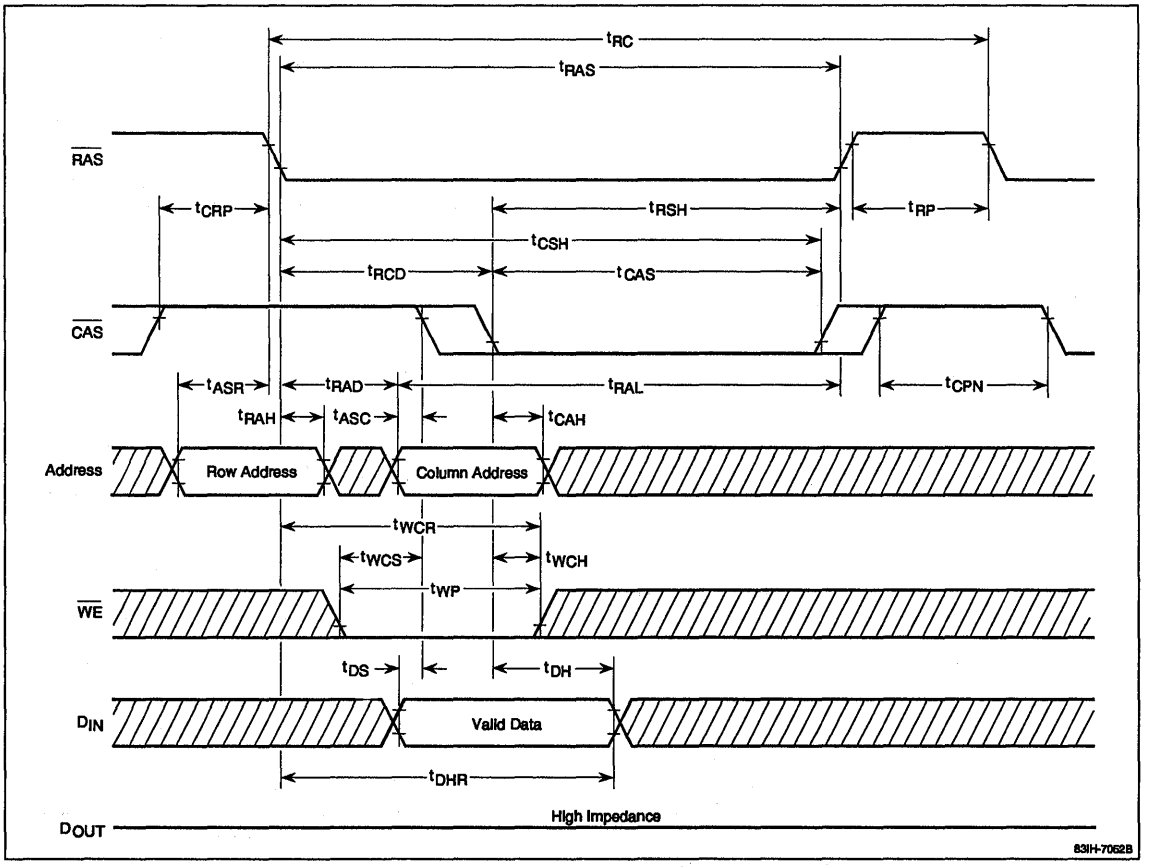


*These parameters are not applicable to the MC-424512A36B/F.

83IH-7051B

Timing Waveforms (cont)

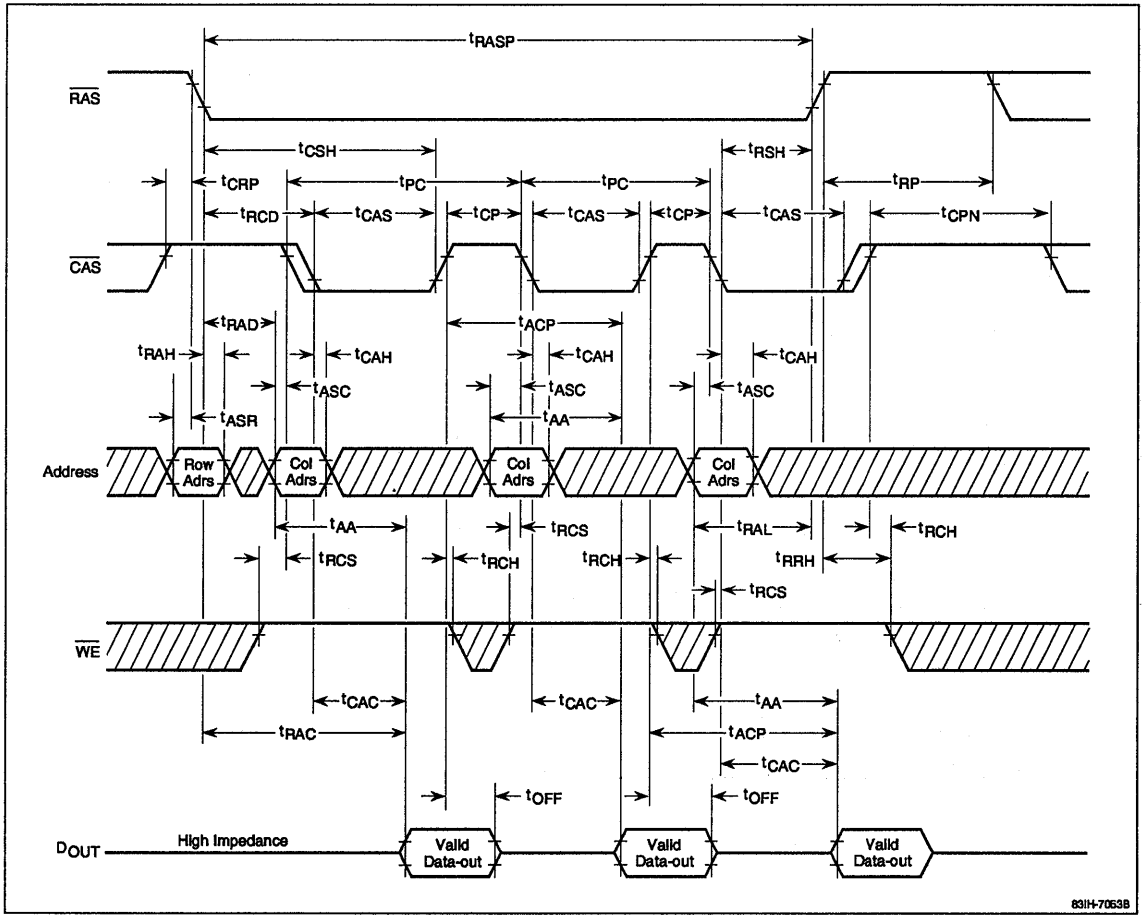
Early Write Cycle



9f

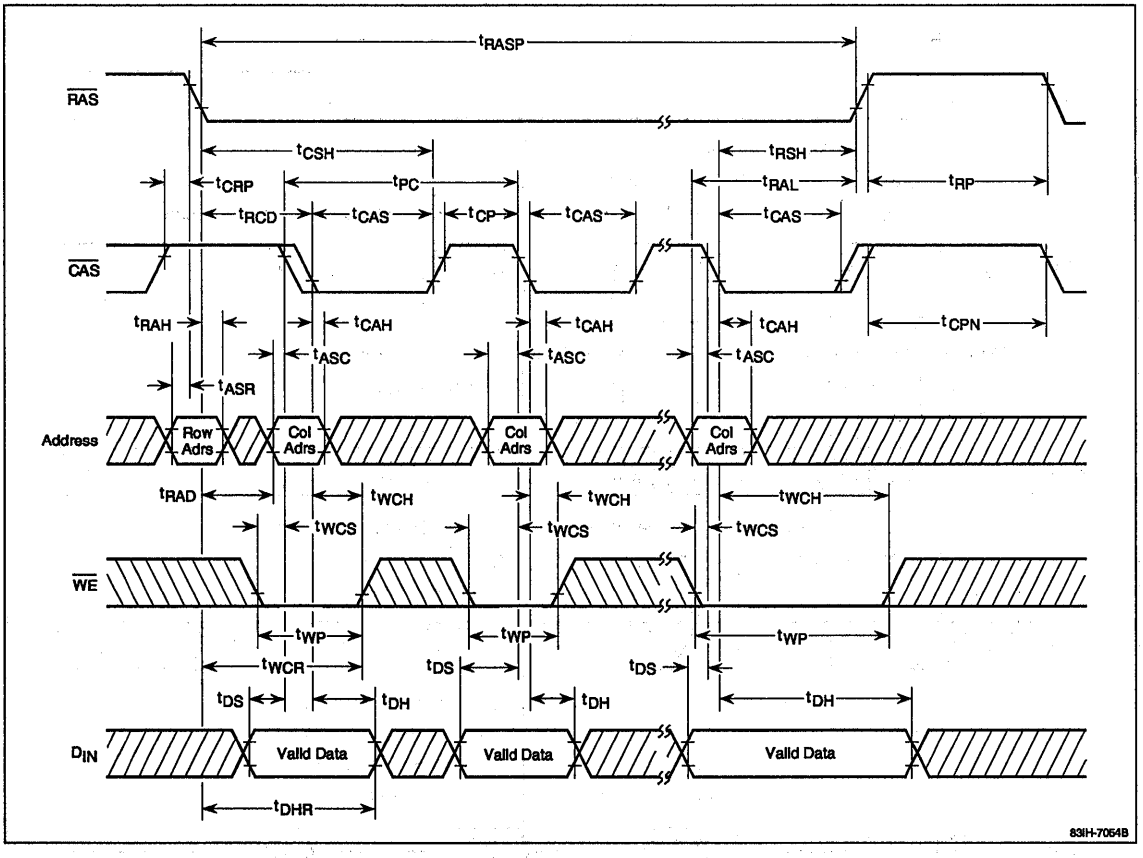
Timing Waveforms (cont)

Fast-Page Read Cycle



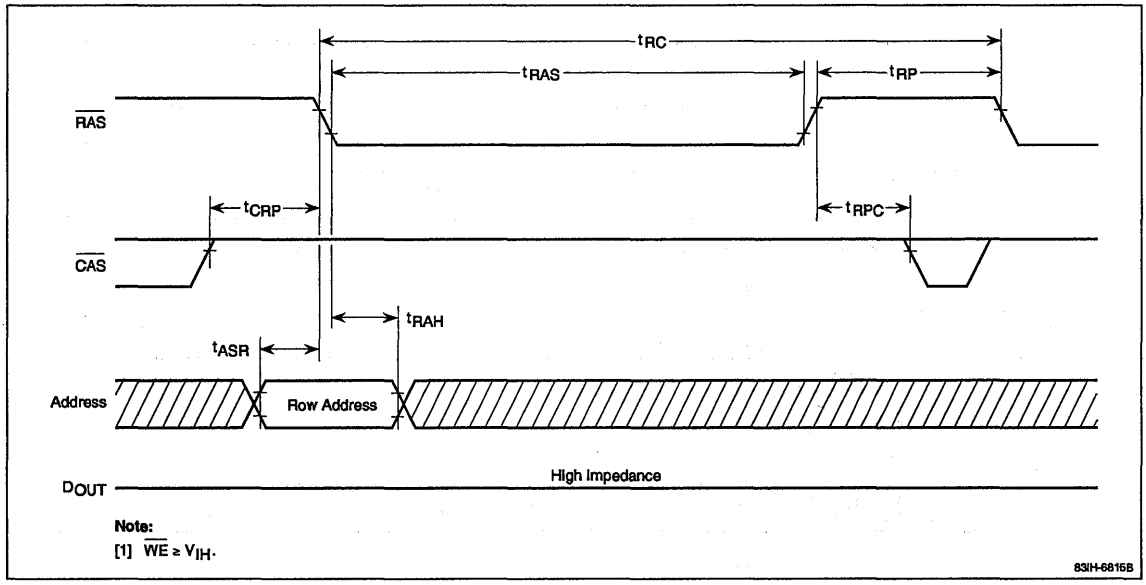
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

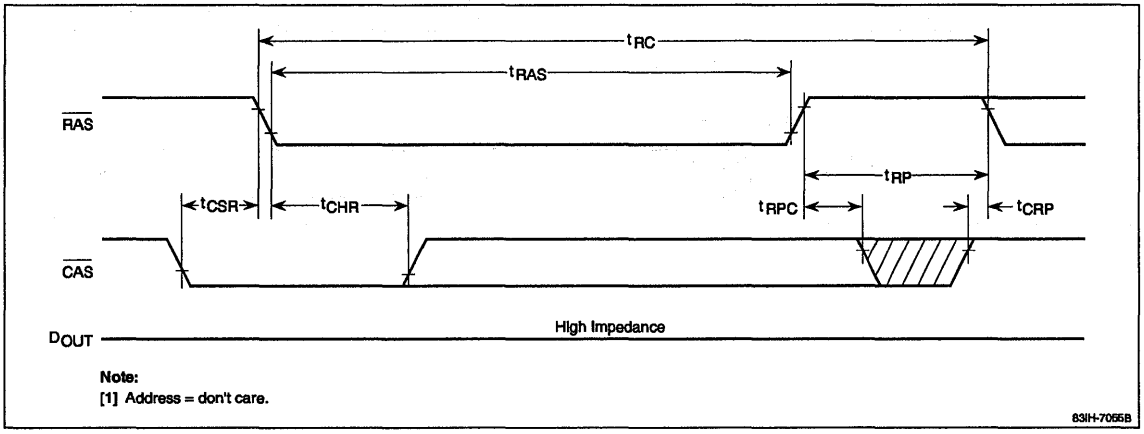
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

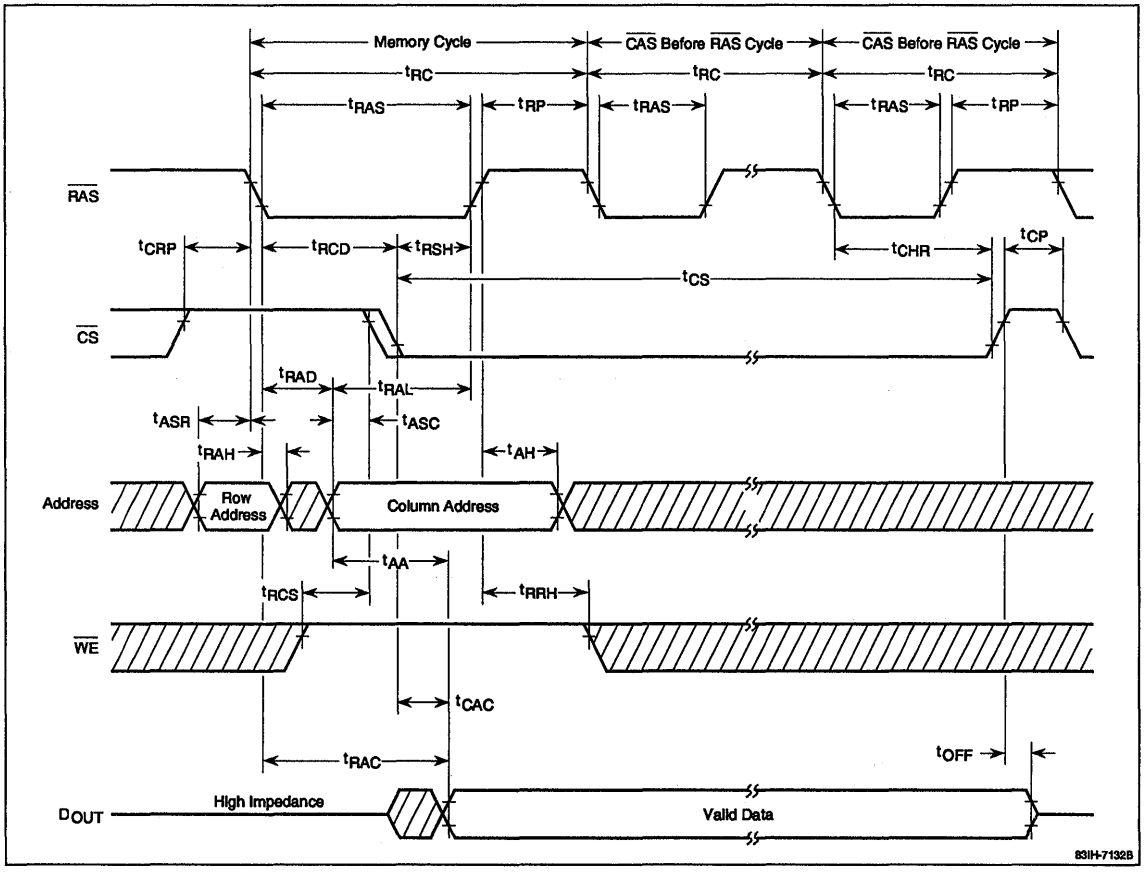


Note:
[1] Address = don't care.

83IH-7055B

Timing Waveforms (cont)

Hidden Refresh Cycle



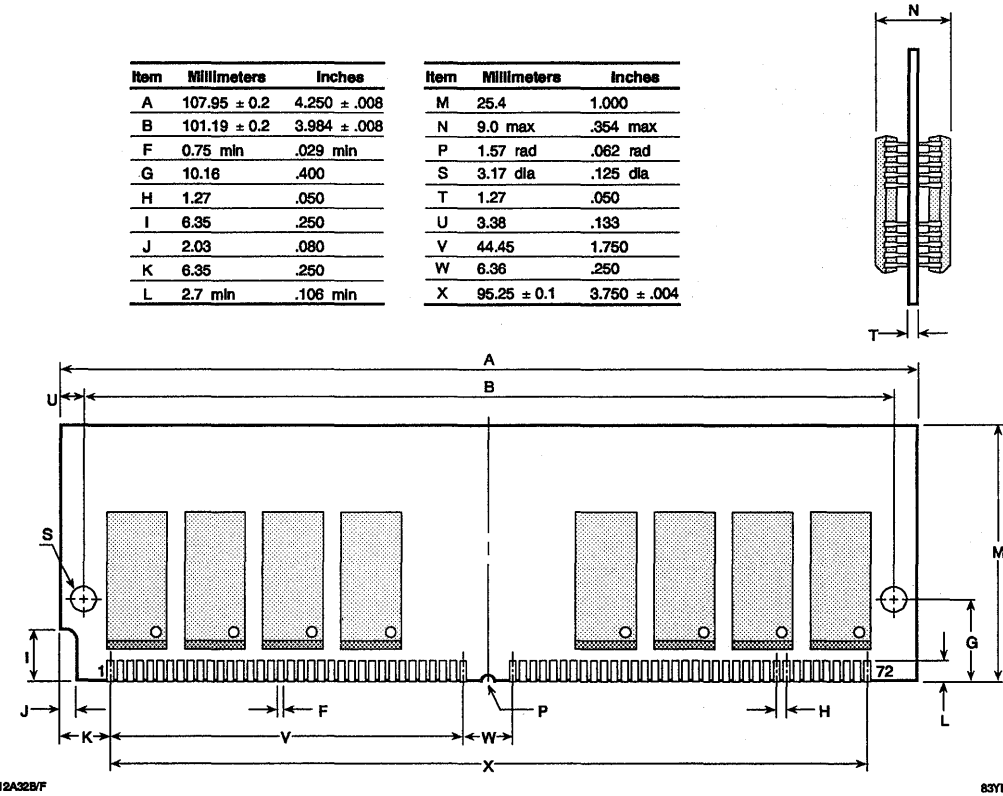
9f

Package Drawing

72-Pin Socket-Mountable SIMM (MC-42512A32B/F)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	9.0 max	.354 max
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004

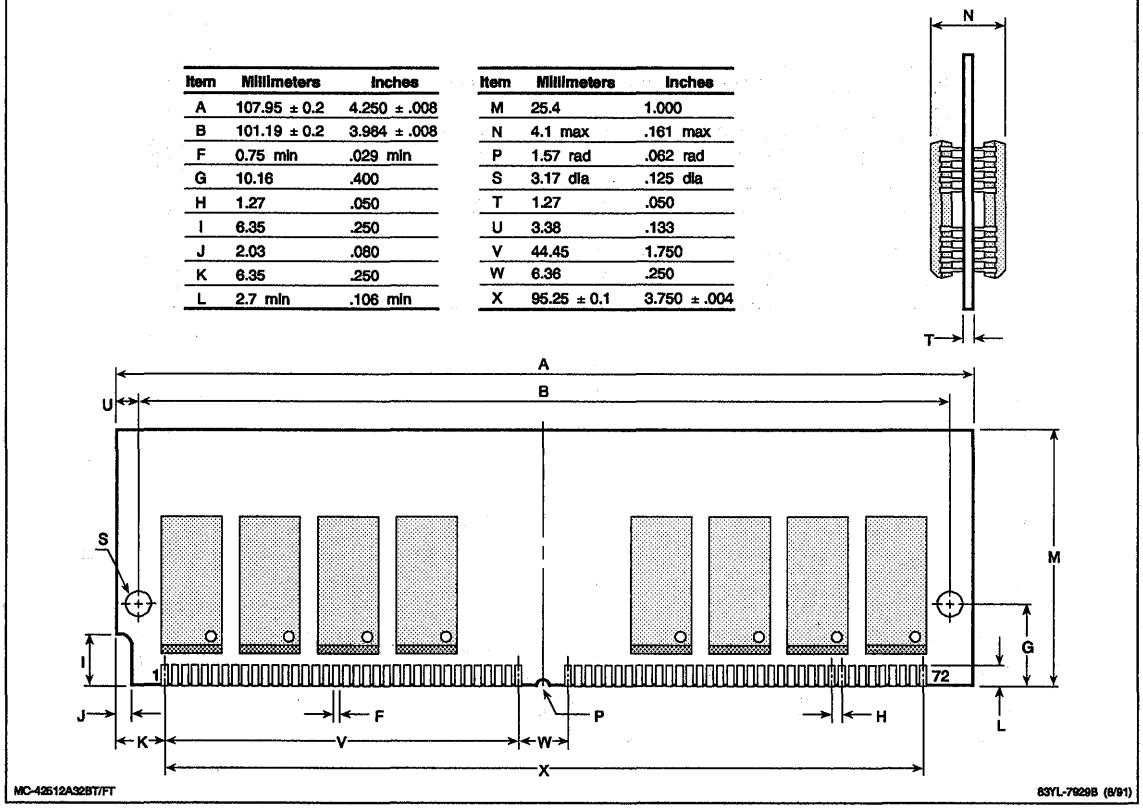


Package Drawing (cont)

72-Pin Socket-Mountable SIMM (MC-42512A32BT/FT)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	4.1 max	.161 max
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-42512A36, -424512A36
524,288 x 36-Bit
Dynamic CMOS RAM Module

Description

The MC-42512A36 and the MC-424512A36 are dynamic RAM modules organized as 524,288 words by 36 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 512 address combinations of A_0 through A_8 during an 8-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight, and cost of a system. Each SIMM contains 24 DRAMs and 24 power supply decoupling capacitors. The complement of DRAMs (μPD424256, 41256, 42256, 421000) and the operating mode (fast-page, page) are summarized below.

Module	DRAMs (Qty) 256K x 4	256K x 1	1M x 1
MC-42512A36 B/F (fast-page)	(16) 424256	(8) 42256	
MC-424512A36 B/F (page)	(16) 424256	(8) 41256	
MC-424512A36 BH/FH (fast-page)	(16) 424256		(8) 421000

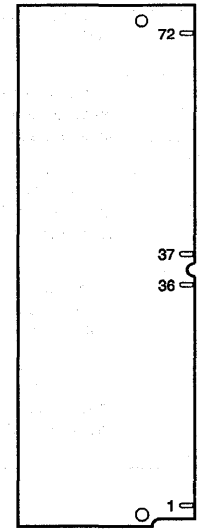
Features

- 524,288-word by 36-bit organization
- Single +5-volt power supply
- Low power dissipation (252 mW max in standby)
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 512 refresh cycles every 8 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging
- Fast-page mode operation (MC-42512A36B/F and MC-424512A36BH/FH)
- Page mode operation (MC-424512A36B/F)

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{18}
4	DQ_1
5	DQ_{19}
6	DQ_2
7	DQ_{20}
8	DQ_3
9	DQ_{21}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	NC
20	DQ_4
21	DQ_{22}
22	DQ_5
23	DQ_{23}
24	DQ_6
25	DQ_{24}
26	DQ_7
27	DQ_{25}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	NC
33	$\overline{RAS_3}$
34	$\overline{RAS_2}$
35	DQ_{26}
36	DQ_8

Pin	Symbol
37	DQ_{17}
38	DQ_{35}
39	GND
40	$\overline{CAS_0}$
41	$\overline{CAS_2}$
42	$\overline{CAS_3}$
43	$\overline{CAS_1}$
44	$\overline{RAS_0}$
45	$\overline{RAS_1}$
46	NC
47	$\overline{WE}$
48	NC
49	DQ_9
50	DQ_{27}
51	DQ_{10}
52	DQ_{28}
53	DQ_{11}
54	DQ_{29}

Pin	Symbol
55	DQ_{12}
56	DQ_{30}
57	DQ_{13}
58	DQ_{31}
59	V_{CC}
60	DQ_{32}
61	DQ_{14}
62	DQ_{33}
63	DQ_{15}
64	DQ_{34}
65	DQ_{16}
66	NC
67	NC
68	GND
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

[1] Pins 69 and 70 are defined by access time:

Pin	70 ns	80/85 ns	100 ns
69	GND	NC	GND
70	NC	GND	GND

83FM-8080A

Ordering Information

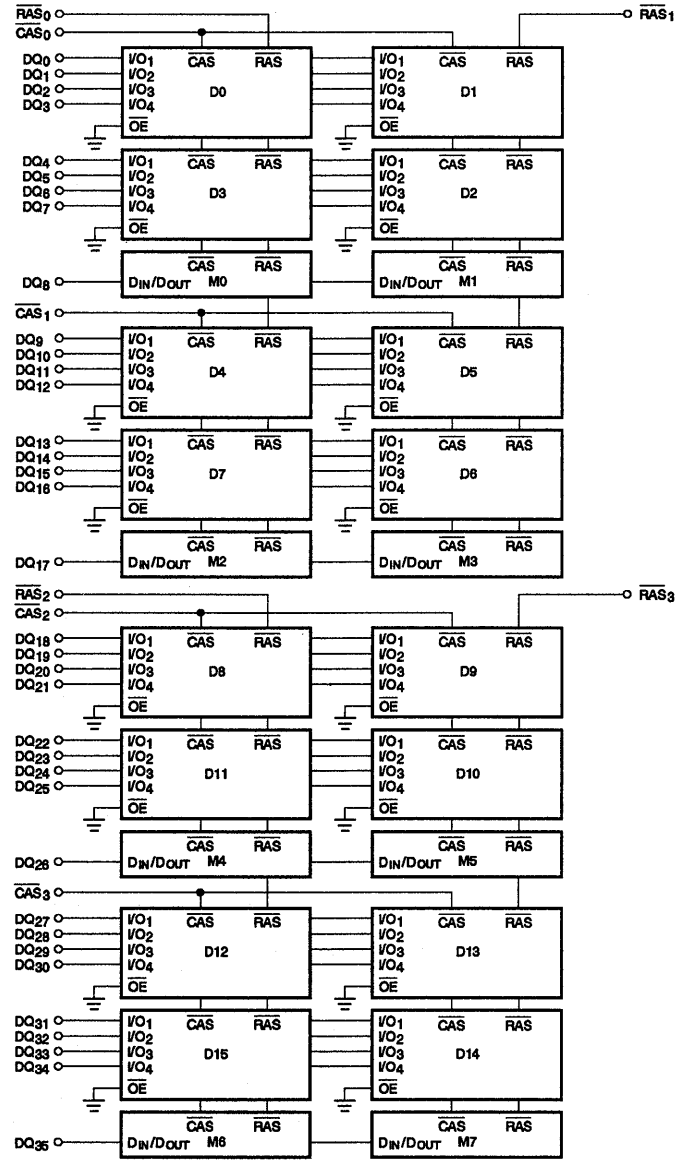
Part Number	Access Time (max)	Package	Operation	Height	Thickness	DRAMs
MC-424512A36BH-70	70 ns	72-pin socket-mountable SIMM (solder plating)	Fast-page	31.75 mm (1.25 inch)	9.3 mm (0.366 inch)	Sixteen μPD424256LA Eight μPD421000LA
BH-80	80 ns					
BH-10	100 ns					
MC-424512A36FH-70	70 ns	72-pin socket-mountable SIMM (gold plating)				
FH-80	80 ns					
FH-10	100 ns					
MC-42512A36B-70	70 ns	72-pin socket-mountable SIMM (solder plating)	Fast-page	25.4 mm (1.00 inch)	9.3 mm (0.366 inch)	Sixteen μPD424256LA Eight μPD42256L
B-80	80 ns					
B-10	100 ns					
MC-42512A36F-70	70 ns	72-pin socket-mountable SIMM (gold plating)				
F-80	80 ns					
F-10	100 ns					
MC-424512A36B-80	80 ns	72-pin socket-mountable SIMM (solder plating)	Page	25.4 mm (1.00 inch)	9.3 mm (0.366 inch)	Sixteen μPD424256LA Eight μPD41256L
B-85	85 ns					
B-10	100 ns					
MC-424512A36F-80	80 ns	72-pin socket-mountable SIMM (gold plating)				
F-85	85 ns					
F-10	100 ns					

Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobes
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS}_0$ - $\overline{RAS}_3$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

9g

Connection Diagram; MC-42512A36, -424512A36



Desig	DRAM	Used On
D0-D15	μPD424256LA	All
M0-M7	μPD421000LA	MC-424512A36BH/FH
	μPD42256LA	MC-42512A36B/F
	μPD41256L	MC-424512A36B/F

83YL-8061B

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	24 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	161	pF	A_0 - A_9
	C_{I2}	193	pF	$\overline{WE}$
	C_{I3}	62	pF	$\overline{RAS}$
	C_{I4}	62	pF	$\overline{CAS}$
Input/output capacitance	C_{I0}/C_{O0}	29	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	39	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

DC Characteristics 1 (MC-42512A36B/F, -424512A36BH/FH)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		48	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−240	240	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics 1 (MC-42512A36B/F, -424512A36BH/FH)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (Note 17)		1040		910		780	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC1} (Note 18)		980		860		740	mA	
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (Note 17)		1040		910		780	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC3} (Note 18)		980		860		740	mA	
Operating current, fast-page cycle, average	I_{CC4} (Note 17)		910		780		650	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
	I_{CC4} (Note 18)		860		740		620	mA	
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (Note 17)		1040		910		780	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
	I_{CC5} (Note 18)		980		860		740	mA	
Access time from column address	t_{AA}		35		45		50	ns	(Notes 7, 9)

AC Characteristics 1 (MC-42512A36B/F, -424512A36BH/FH) (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		60		70		ns	
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10	20	10	20	10	25	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		20		20		ns	(Note 15)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	35	17	45	ns	(Note 9)
Row address hold time	t_{RAH}	10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	35		45		55		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	

AC Characteristics 1 (MC-42512A36B/F, -424512A36BH/FH) (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		20		ns	
Write command pulse width	t_{WP}	15		15		20		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle.

If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) MC-424512A36BH/FH

(18) MC-42512A36B/F

DC Characteristics 2 (MC-424512A36B/F)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		72	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$ (min)
			16	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V
Input leakage current	$I_{I(L)}$	–240	240	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics 2 (MC-424512A36B/F)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-80		-85		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		1024		872		744	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1024		872		744	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		996		828		724	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1024		872		744	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		55		65		ns	
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		40		40		50	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	20		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10,000	40	10,000	50	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	20		20		40		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	80		85		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	20		20		25		ns	(Note 15)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		65		75		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	20	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	70		70		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		85		100	ns	(Notes 7, 8)
Row address hold time	t_{RAH}	12		12		12		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	85	10,000	100	10,000	ns	
Random read or write cycle time	t_{RC}	160		165		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	45	20	50	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	

AC Characteristics 2 (MC-424512A36B/F) (cont)

Parameter	Symbol	-80 Min	-80 Max	-85 Min	-85 Max	-10 Min	-10 Max	Unit	Test Conditions
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	70		70		90		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	40		40		50		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	20		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		65		75		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

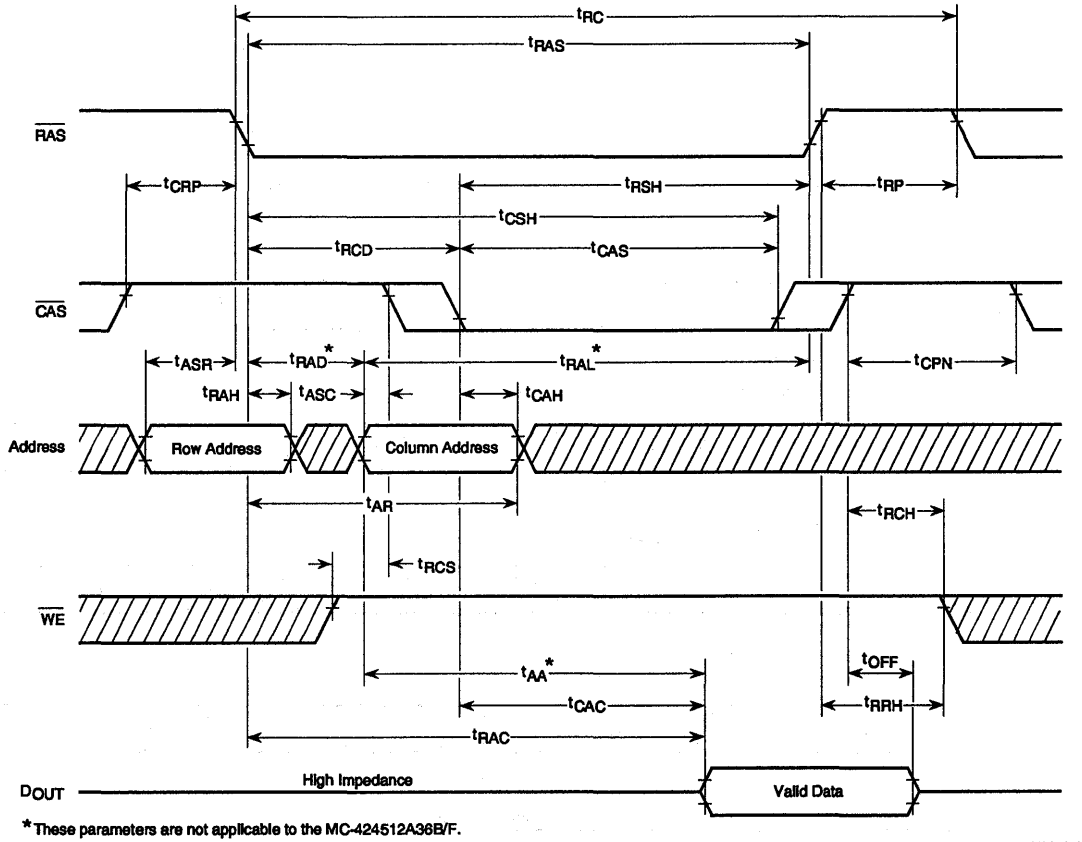
(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle.

If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

9g

Timing Waveforms

Read Cycle

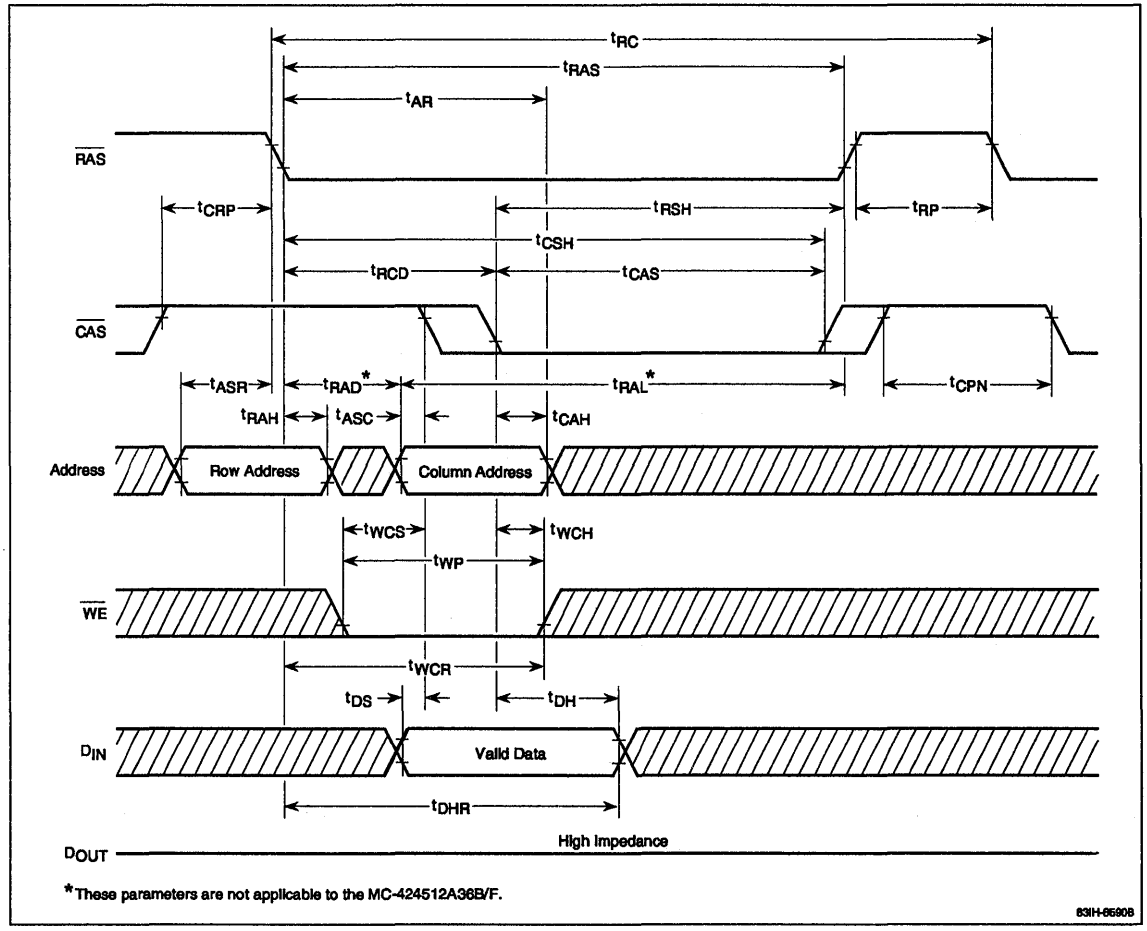


*These parameters are not applicable to the MC-424512A36B/F.

83IH-7051B

Timing Waveforms (cont)

Early Write Cycle



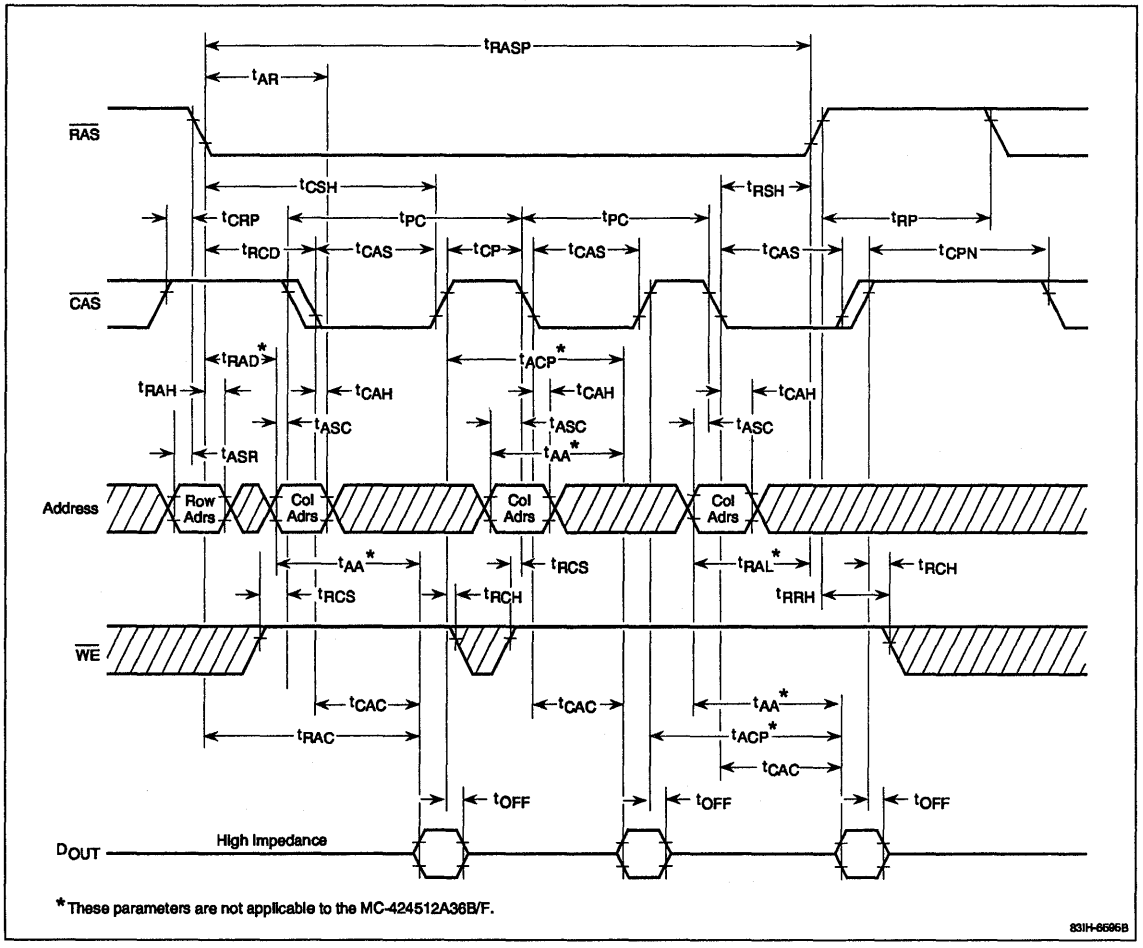
*These parameters are not applicable to the MC-424512A36B/F.

83IH-6590B

9g

Timing Waveforms (cont)

Page/Fast-Page Read Cycle

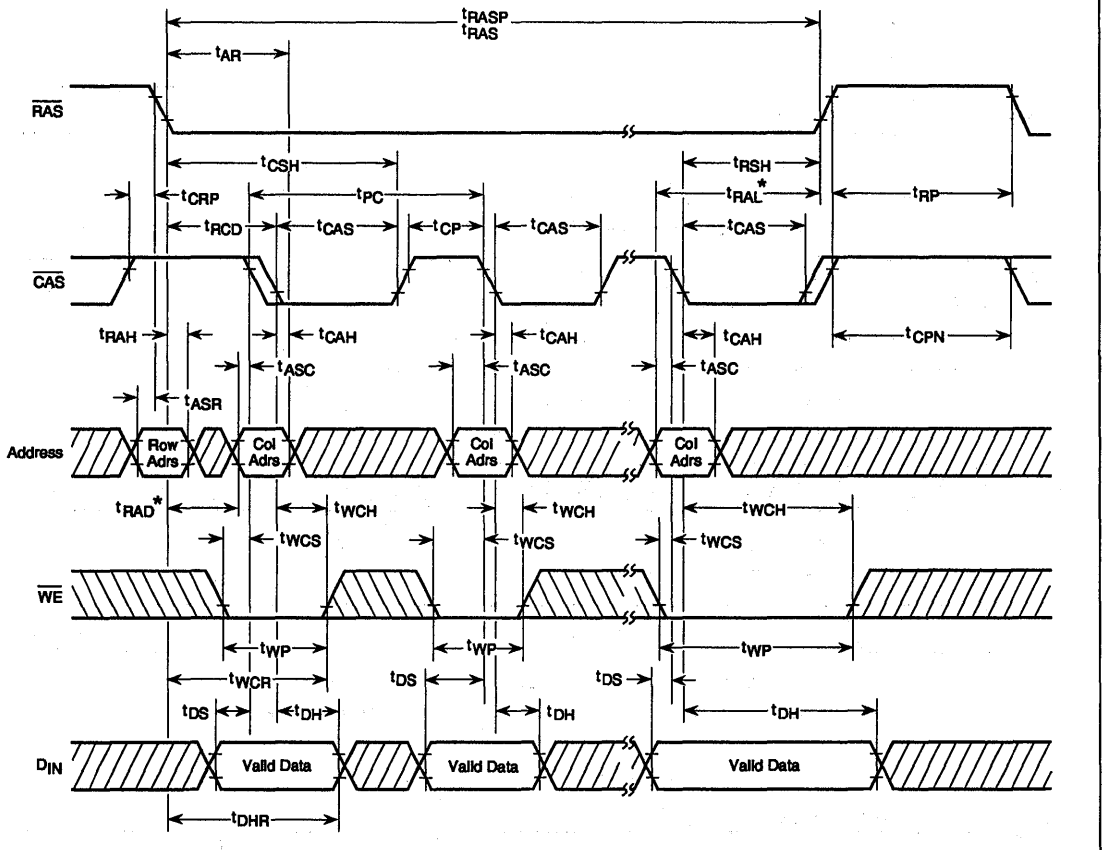


*These parameters are not applicable to the MC-424512A36B/F.

83IH-6696B

Timing Waveforms (cont)

Page/Fast-Page Early Write Cycle



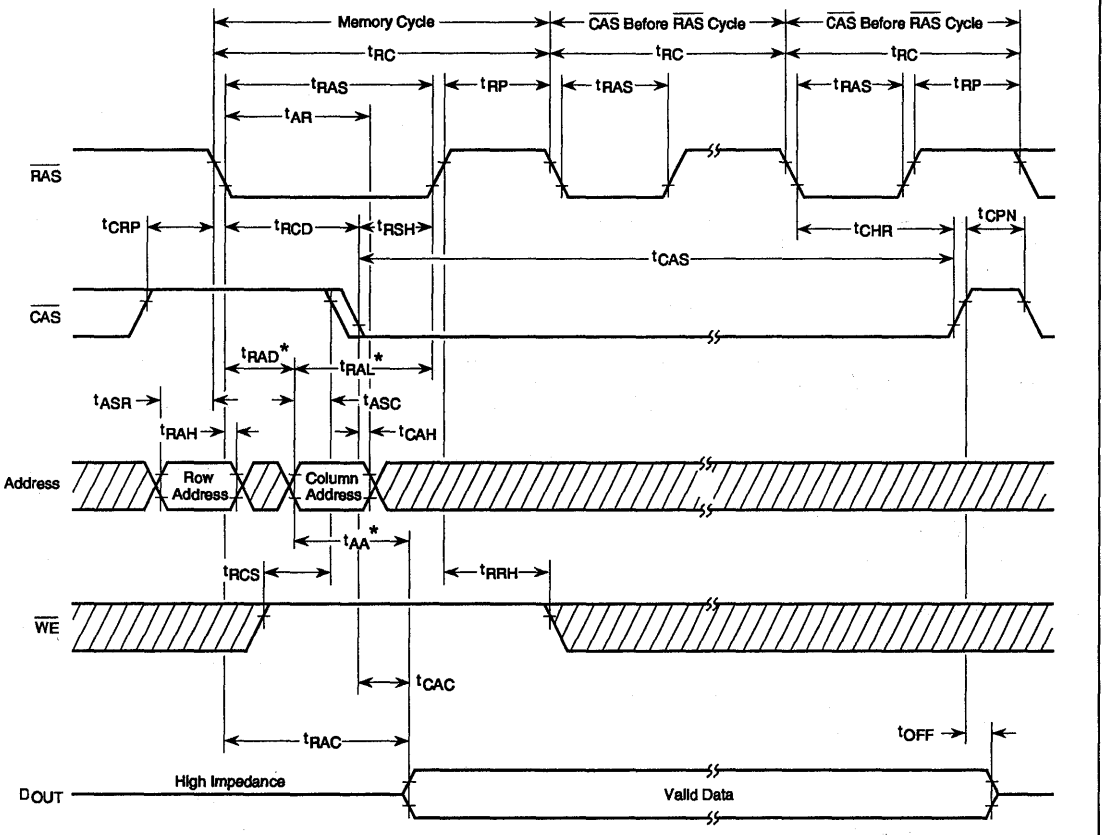
*These parameters are not applicable to the MC-424512A36B/F.

83IH-6696B

9g

Timing Waveforms (cont)

Hidden Refresh Cycle

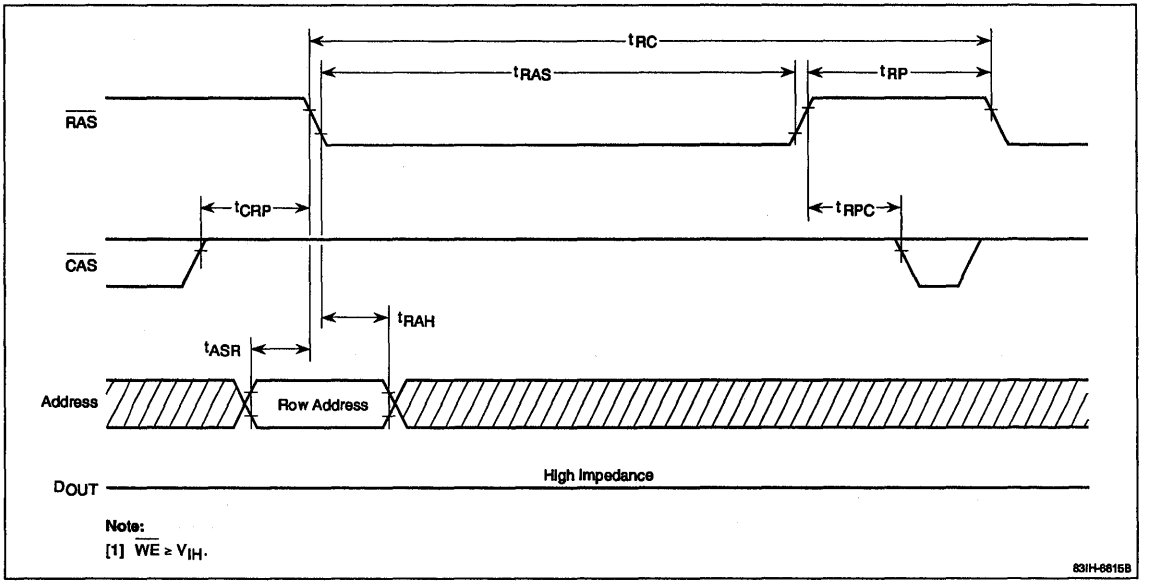


*These parameters are not applicable to the MC-424512A36.

83IH-8693B

Timing Waveforms (cont)

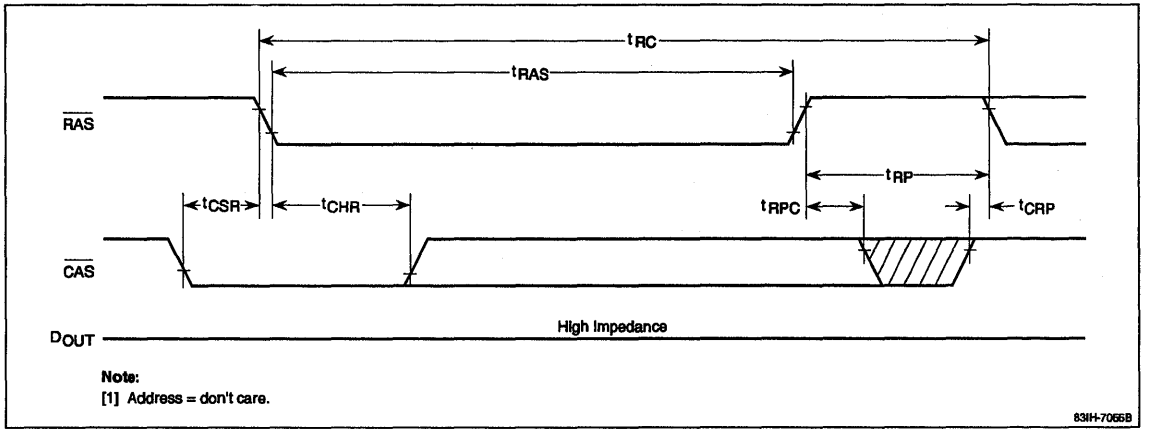
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

83IH-7066B

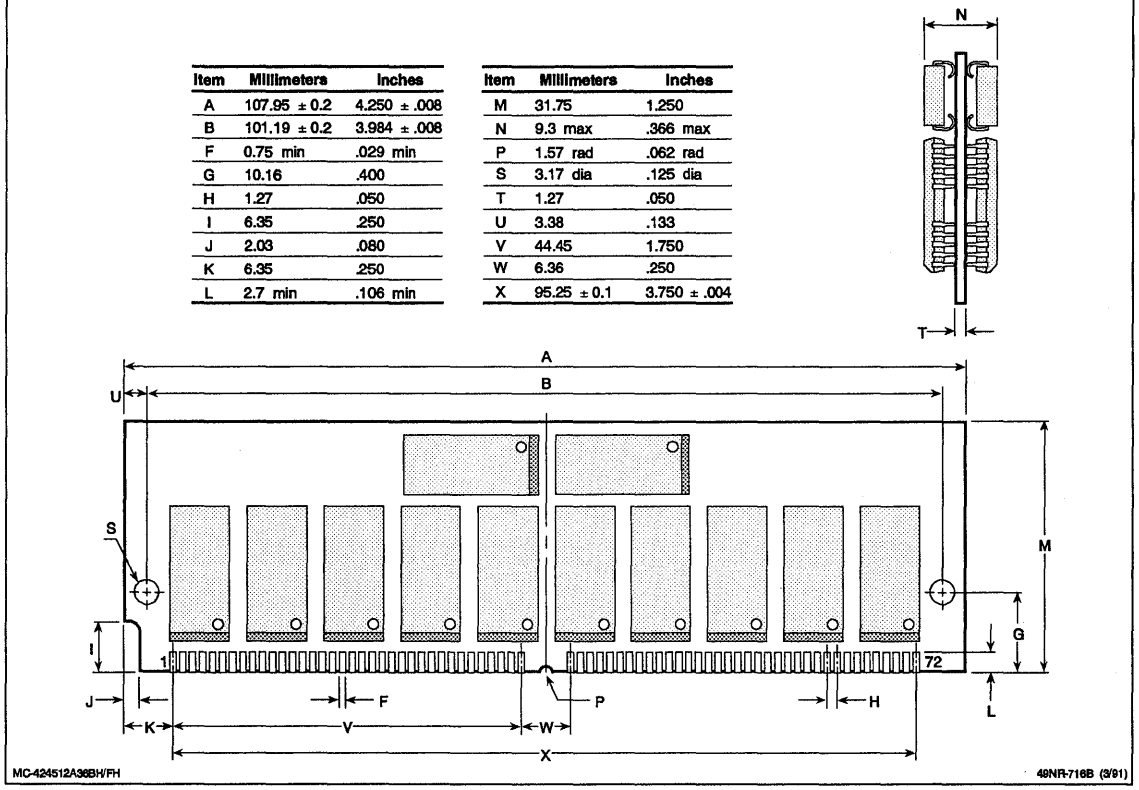
9g

Package Drawings

72-Pin Socket-Mountable SIMM (MC-424512A36BH/FH)

Item	Millimeters	Inches
A	107.95 ±0.2	4.250 ± .008
B	101.19 ±0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	31.75	1.250
N	9.3 max	.366 max
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ±0.1	3.750 ± .004

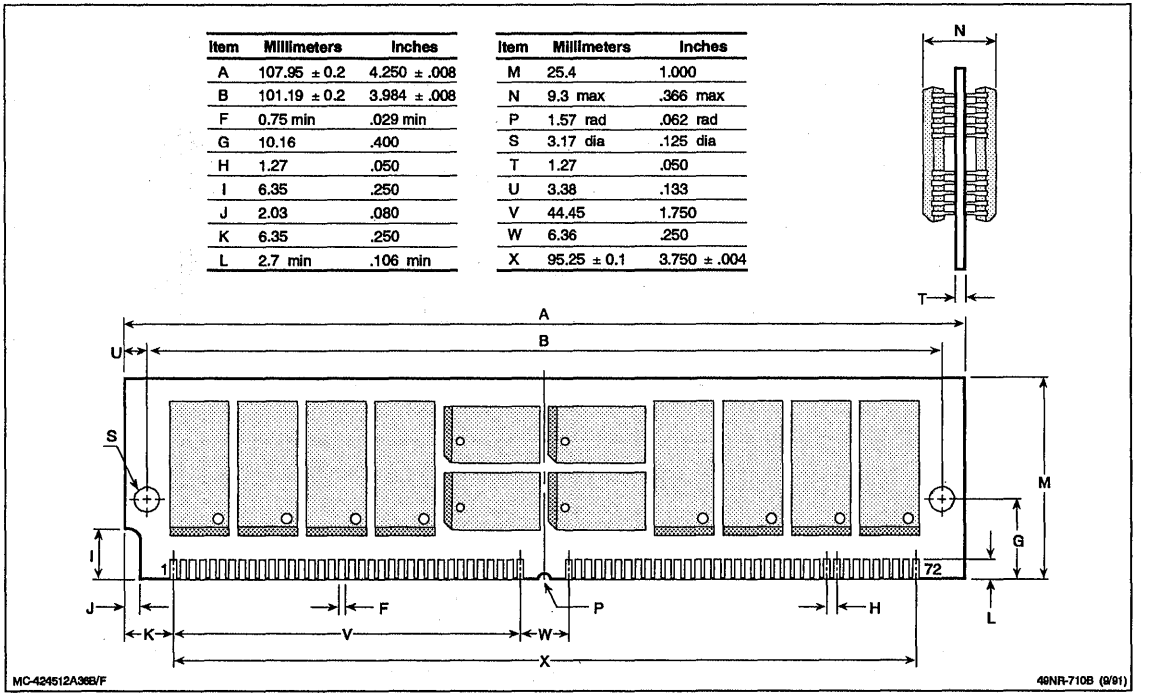


Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-42512A36B/F and MC-424512A36B/F)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	9.3 max	.366 max
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



NEC Electronics Inc.

MC-42512AA40, -42512AB40
524,288 x 40-Bit
Dynamic CMOS RAM Module

Description

The MC-42512AA40 and MC-42512AB40 are fast-page dynamic RAM modules organized as 524,288 words by 40 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 512 address combinations of A_0 - A_8 during an 8-ms period for the MC-42512AA40. The MC-42512AB40 requires 1024 address combinations of A_0 - A_9 during a 16-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight, and cost of a system.

Two versions of this SIMM module are available. The MC-42512AA40 is designed with twenty 262,144 x 4-bit μPD424256s in SOJ packages and 20 power supply decoupling capacitors for noise reduction.

The MC-41512AB40 is designed with five 524,288 x 8-bit μPD424800s in SOJ packages and five power supply decoupling capacitors for noise reduction.

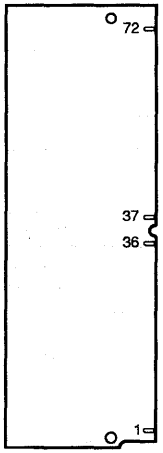
Features

- 524,288-word by 40-bit organization
- Single +5-volt power supply
- Fast-page cycles
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 512 refresh cycles every 8 ms (MC-42512AA40); 1024 refresh cycles every 16 ms (MC-42512AB40)
- TTL-compatible inputs and outputs
- 72-pin SIMM™ packaging

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{16}
4	DQ_1
5	DQ_{17}
6	DQ_2
7	DQ_{18}
8	DQ_3
9	DQ_{19}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	$\overline{OE}$
20	DQ_4
21	DQ_{20}
22	DQ_5
23	DQ_{21}
24	DQ_6
25	DQ_{22}
26	DQ_7
27	DQ_{23}
28	A_7
29	DQ_{36}
30	V_{CC}
31	A_8
32	Note 2
33	NC
34	NC
35	DQ_{34}
36	DQ_{32}

Pin	Symbol
37	DQ_{33}
38	DQ_{35}
39	GND
40	$\overline{CAS_0}$
41	NC
42	NC
43	Note 2
44	$\overline{RAS_0}$
45	Note 2
46	DQ_{37}
47	$\overline{WE}$
48	GND
49	DQ_8
50	DQ_{24}
51	DQ_9
52	DQ_{25}
53	DQ_{10}
54	DQ_{26}

Pin	Symbol
55	DQ_{11}
56	DQ_{27}
57	DQ_{12}
58	DQ_{28}
59	V_{CC}
60	DQ_{29}
61	DQ_{13}
62	DQ_{30}
63	DQ_{14}
64	DQ_{31}
65	DQ_{15}
66	DQ_{38}
67	Note 1
68	Note 1
69	Note 1
70	Note 1
71	DQ_{39}
72	GND

Notes:

[1] Pins 67-70 are defined by access time:

Pin	70 ns	80 ns	100 ns
67	NC	NC	NC
68	GND	GND	GND
69	GND	NC	GND
70	NC	GND	GND

[2] Signal assignments to pins 32, 43, and 45:

Pin	MC-42512AA40	MC-42512AB40
32	NC	A_9
43	$\overline{CAS1}$	NC
45	$\overline{RAS1}$	NC

83FM-8118A

Pin Identification

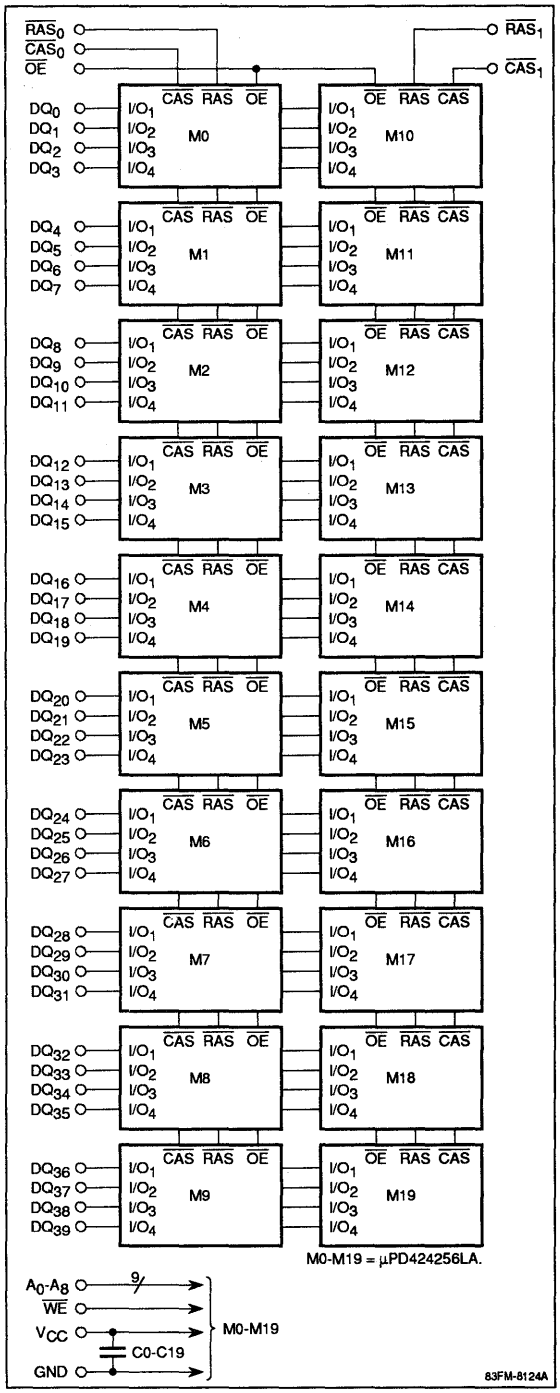
Name	Function
A_0 - A_9	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_1$	Column address strobes
DQ_0 - DQ_{39}	Common data inputs/outputs
$\overline{RAS}_0$ - $\overline{RAS}_1$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Ordering Information

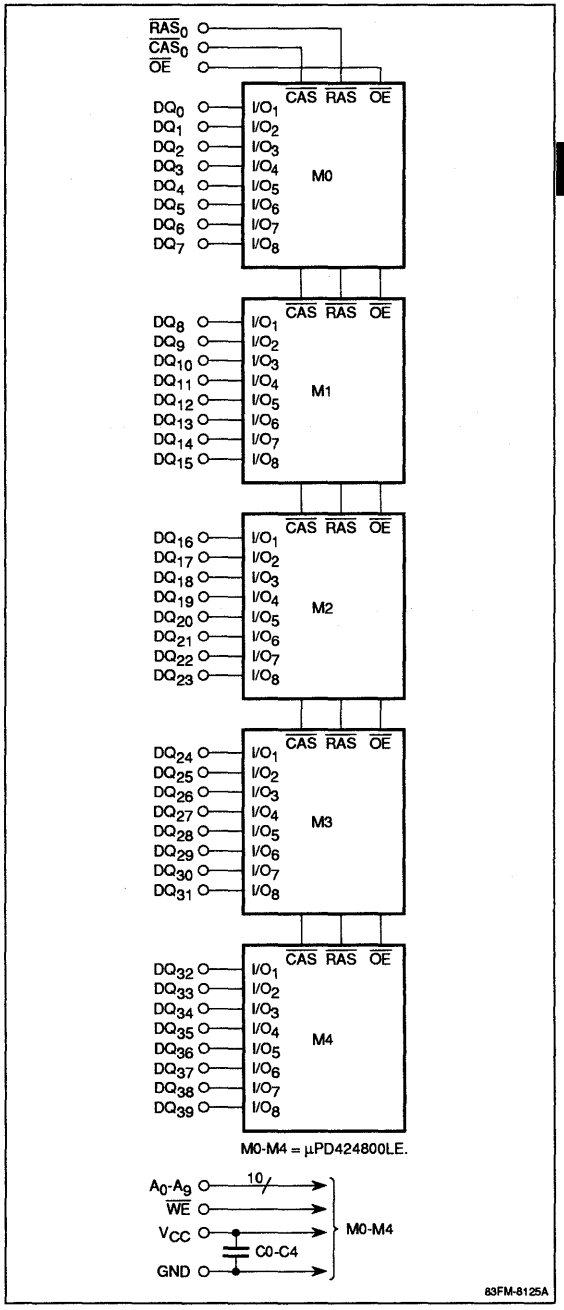
Part Number		Access Time (max)	Package	Height	Thickness	DRAMs
MC-42512AA40	B-70	70 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	9.3 mm (0.366 inch)	Twenty μPD424256LA
	B-80	80 ns				
	B-10	100 ns				
MC-42512AA40	F-70	70 ns	72-pin socket-mountable SIMM (gold plating)			
	F-80	80 ns				
	F-10	100 ns				
MC-42512AB40	B-70	70 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	5.08 mm (0.2 inch)	Five μPD424800LE
	B-80	80 ns				
	B-10	100 ns				
MC-42512AB40	F-70	70 ns	72-pin socket-mountable SIMM (gold plating)			
	F-80	80 ns				
	F-10	100 ns				

9h

MC-42512AA40 Connection Diagram



MC-42512AB40 Connection Diagram



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Supply voltage	V_{CC}	4.5	5.0	5.5	V	MC-42512AA40
Supply voltage	V_{CC}	4.75	5.0	5.25	V	MC-42512AB40
Ambient temperature	T_A	0		70	°C	

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D (MC-42512AA40)	20 W
Power dissipation, P_D (MC-42512AB40)	5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	MC-42512AA40 (max)	MC-42512AB40 (max)	Unit	Pins Under Test
Input capacitance	C_{I1}	110	35	pF	A_0 - A_9
	C_{I2}	130	45	pF	$\overline{WE}$, $\overline{OE}$
	C_{I3}	60	40	pF	$\overline{RAS}$
	C_{I4}	60	40	pF	$\overline{CAS}$
Input/output capacitance	C_{IO}/C_{OO}	20	12	pF	DQ_0 - DQ_{39}

DC Characteristics, MC-42512AA40

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		960		840		720	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; (Note 5)
Standby current	I_{CC2}		40		40		40	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
			20		20		20	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		960		840		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		820		720		620	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		960		840		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IL}; t_{RC} = t_{RC} min; (Note 5)
Input leakage current	$I_{I(L)}$	–200	200	–200	200	–200	200	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	–10	10	–10	10	μA	D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}		0.4		0.4		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		2.4		2.4		V	I_{OH} = –5 mA

DC Characteristics, MC-42512AB40

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		525		475		400	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; (Note 5)
Standby current	I_{CC2}		10		10		10	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
			5		5		5	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		525		475		400	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		400		350		300	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		525		475		400	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IL}; t_{RC} = t_{RC} min; (Note 5)
Input leakage current	$I_{I(L)}$	–50	50	–50	50	–50	50	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	–10	10	–10	10	μA	D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}		0.4		0.4		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		2.4		2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0V ±10% (AA40) or ±5% (AB40)

		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Access time from column address	t_{AA}		35		40		50	ns	(Notes 7, 8, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		40		55	ns	(Notes 7, 11, 18)
			40		45		45	ns	(Notes 7, 11, 19)
Column address setup time	t_{ASC}	0	10	0	15	0	20	ns	(Note 9)
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	55		65		80		ns	(Note 16)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		25	ns	(Notes 7, 8, 11)
Column address hold time	t_{CAH}	16		16		20		ns	(Note 18)
		15		15		20		ns	(Note 19)
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	(Notes 4, 19)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10	15	10	15	10	20	ns	(Note 9)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		45		55		ns	(Note 16)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	(Note 18)
		15		15		20		ns	(Note 19)
Data-in hold time	t_{DH}	15		20		20		ns	(Notes 15, 18)
		15		15		20		ns	(Notes 15, 19)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		60		70		ns	(Note 18)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Access time from $\overline{OE}$	t_{OEA}		20		20		25	ns	
$\overline{OE}$ data delay time	t_{OED}	15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	25	ns	(Note 10)
Output buffer turnoff delay	t_{OFF}	0	15	0	20	0	25	ns	(Note 10)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Notes 4, 19)
Fast-page cycle time	t_{PC}	45		50		60		ns	(Note 6)
Fast-page read-write cycle time	t_{PRWC}	90		105		125		ns	(Note 18)
		90		100		120		ns	(Note 19)
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	40	17	45	ns	(Notes 9, 18)
		15	35	17	40	17	50	ns	(Notes 9, 19)

AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Row address hold time	t_{RAH}	10		10		12		ns	(Note 18)
		10		12		12		ns	(Note 19)
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	35		45		55		ns	(Note 18)
		35		40		50		ns	(Note 19)
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	(Note 18)
		70	125,000	80	125,000	100	125,000	ns	(Note 19)
Random read or write cycle time	t_{RC}	130		160		190		ns	(Notes 6, 18)
		140		160		190		ns	(Notes 6, 19)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 9)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8 (Note 18)
			16		16		16	ms	Addresses A_0 - A_9 (Note 19)
$\overline{RAS}$ precharge time	t_{RP}	50		60		80		ns	(Note 18)
		60		70		80		ns	(Note 19)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		10		ns	(Notes 13, 18)
		10		10		10		ns	(Notes 13, 19)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Read-write cycle time	t_{RWC}	175		215		255		ns	(Notes 6, 18)
		185		210		250		ns	(Notes 6, 19)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	90		105		130		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		30		ns	(Note 18)
		20		20		25		ns	(Note 19)
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		55		70		ns	(Note 18)
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
Write command pulse width	t_{WP}	15		15		20		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. It is recommended that when using the MC-42512AB40, either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

AC Characteristics (cont)

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) For random read cycles, access time is defined as follows:

Input Conditions	Access Time
$t_{RAD} \leq t_{RAD}$ (max) and $t_{RCD} \leq t_{RCD}$ (max)	t_{RAC}
$t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

The above access times assume that $\overline{OE}$ has been active t_{OEA} (min) prior to when data is expected on the output.

(9) t_{ASC} (max), t_{CP} (max), t_{RAD} (max), and t_{RCD} (max) are specified as reference points for determination of access time. They are not restrictive operating parameters.

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) For fast-page read operation, the definition of access time is as follows:

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

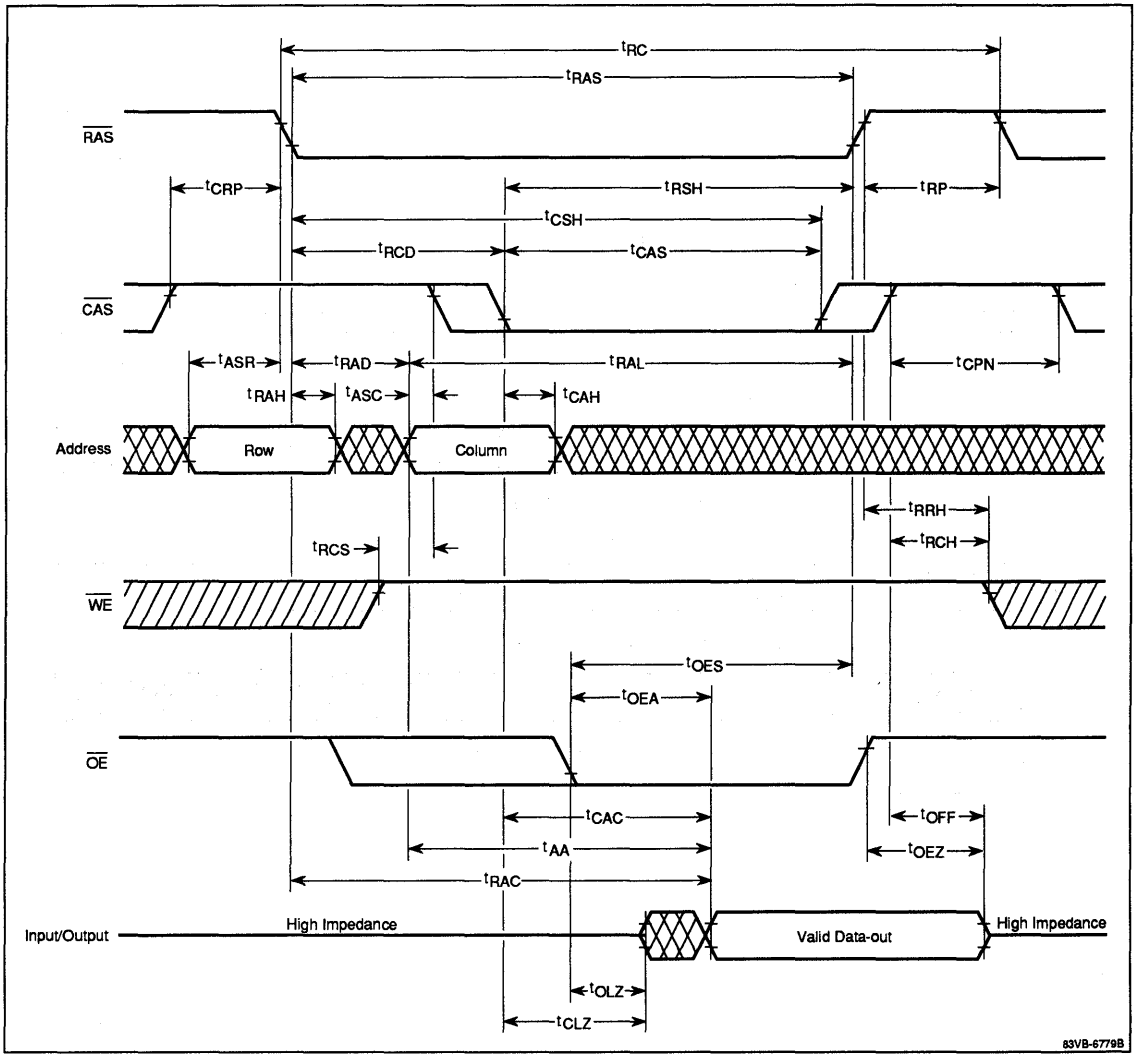
(17) A test mode may be inadvertently initiated during power-up because external control of signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed any time after the end of the initial power-up sequence to ensure normal device operation.

(18) Applicable to the MC-42512AA40 only.

(19) Applicable to the MC-42512AB40 only.

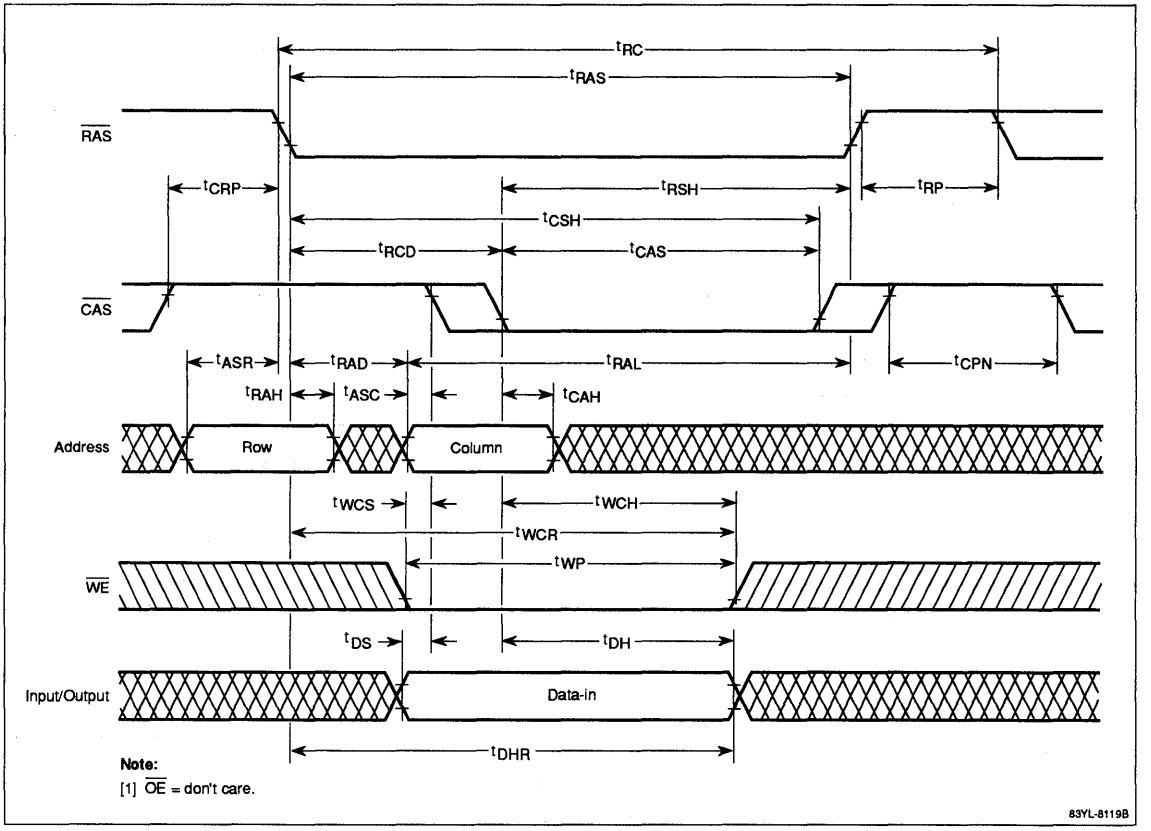
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

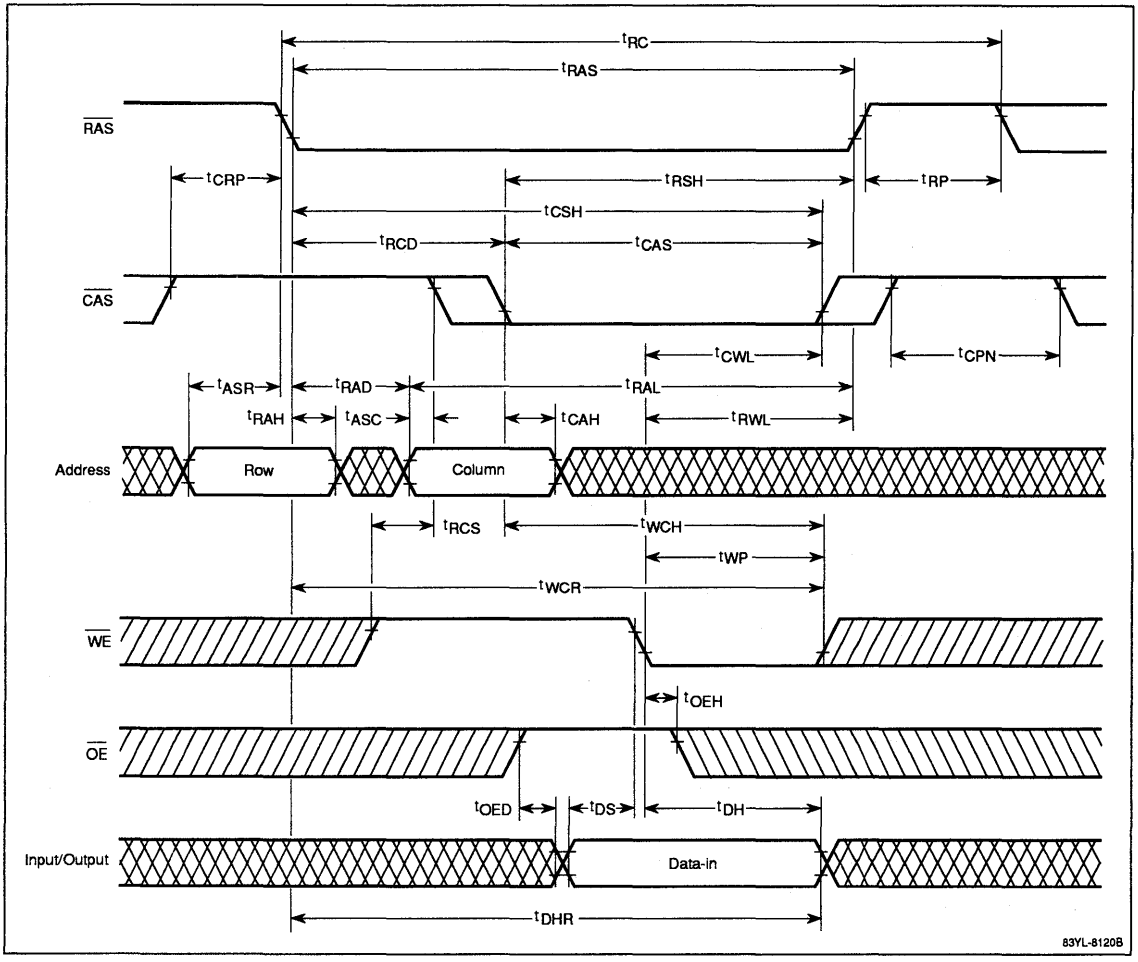
Early Write Cycle



9h

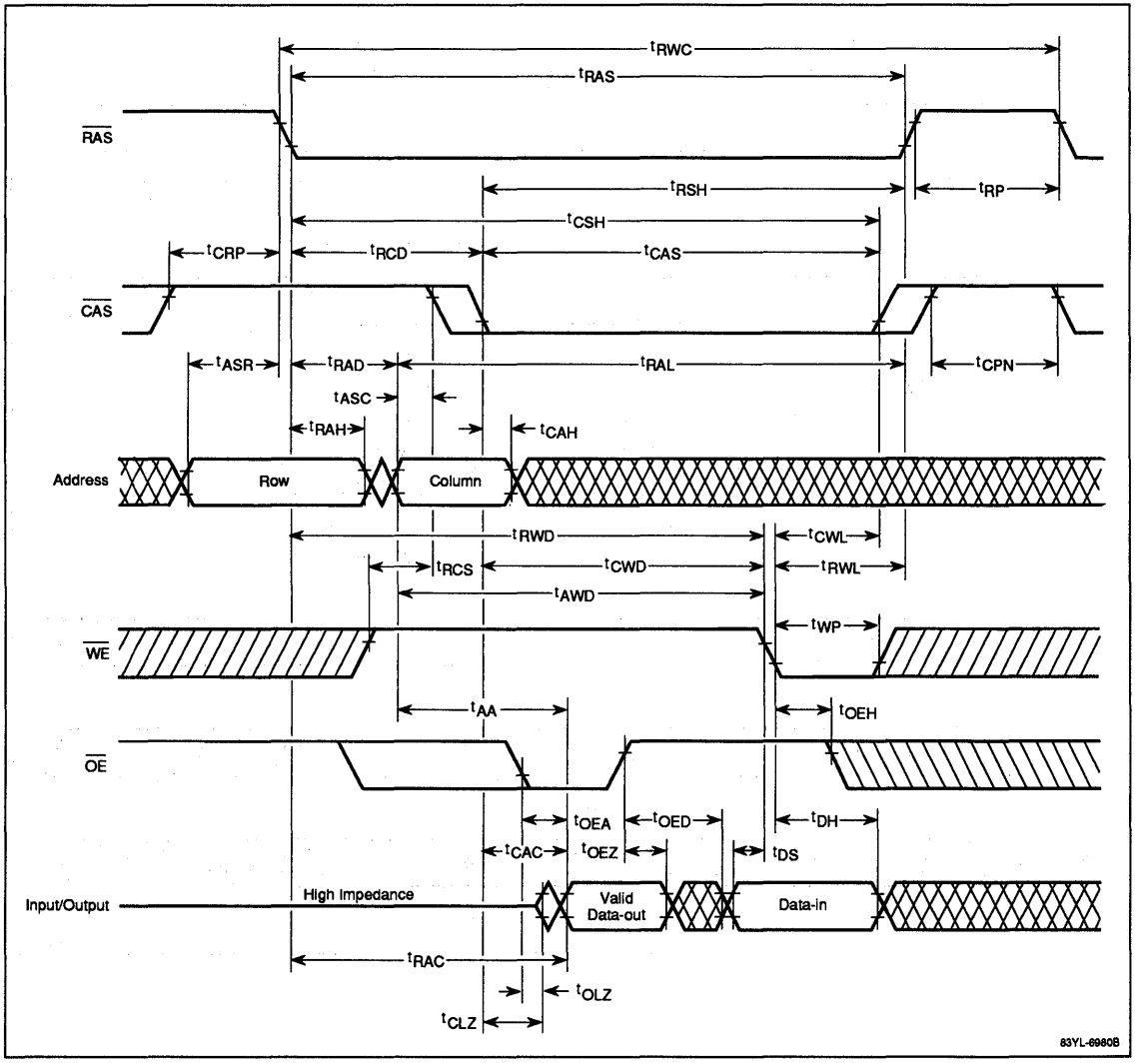
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

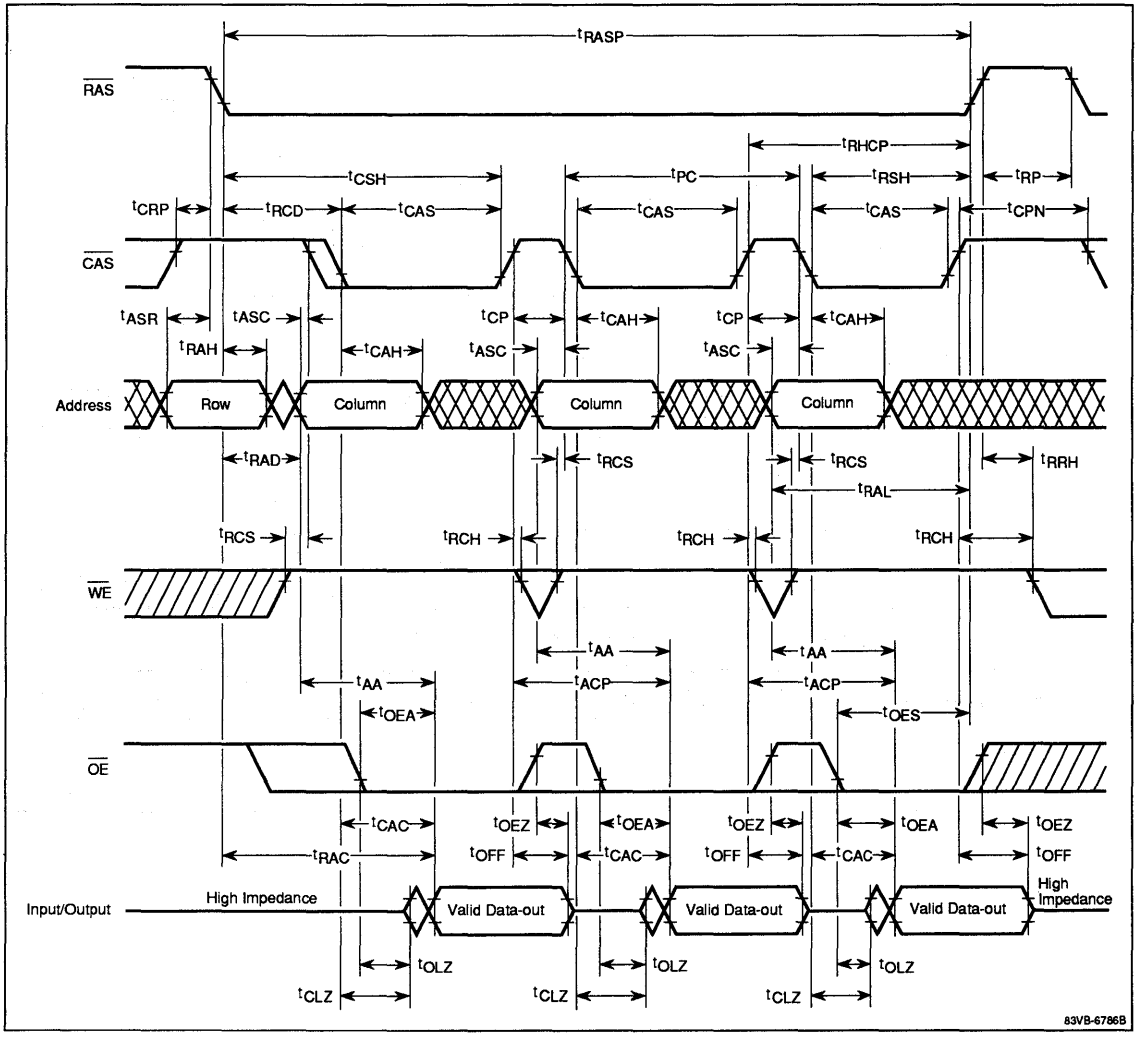
Read-Write/Read-Modify-Write Cycle



9h

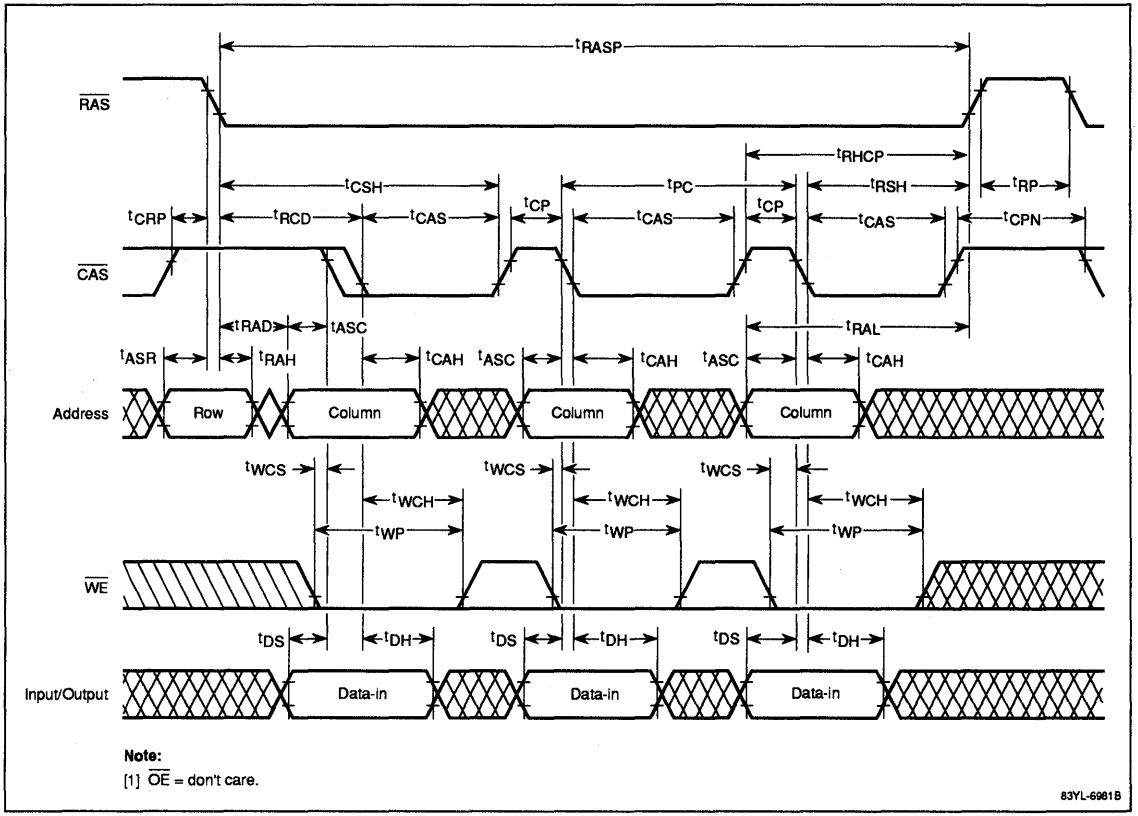
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle

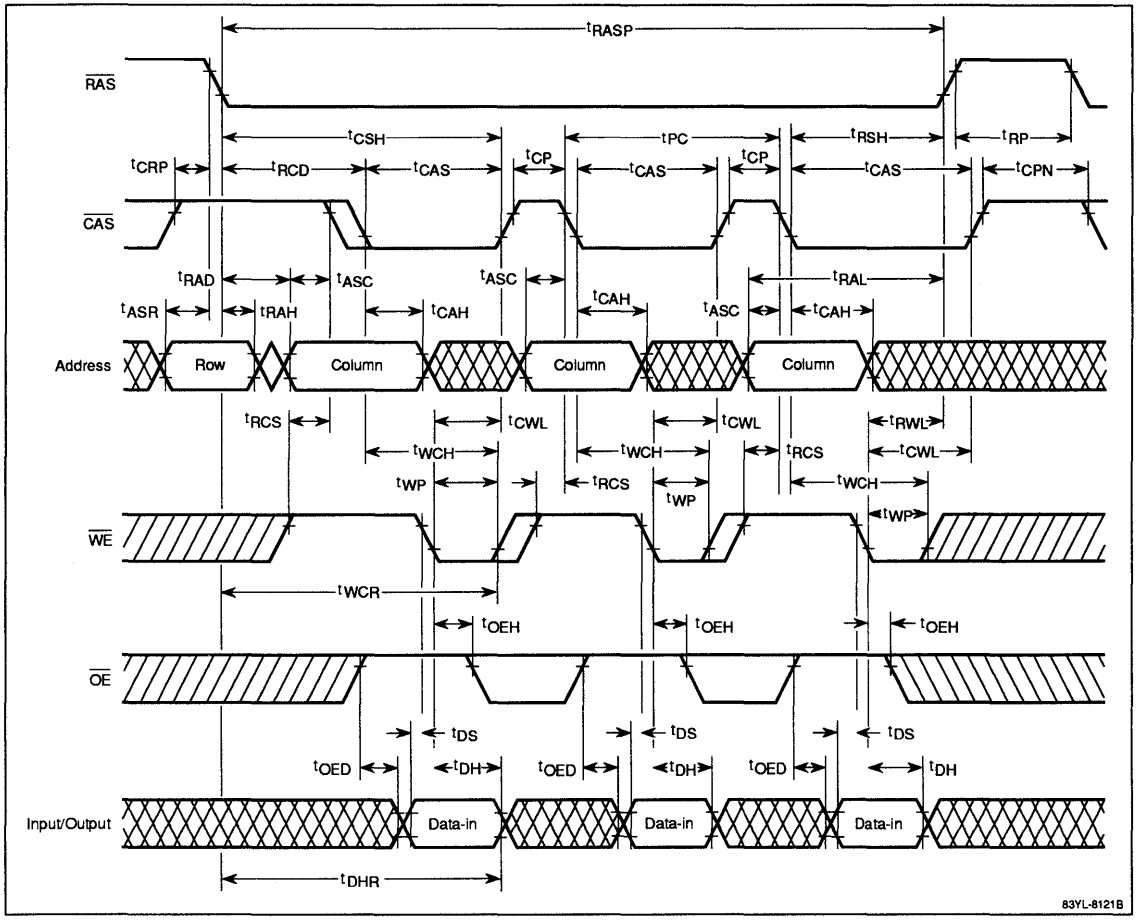


Note:
[1] $\overline{OE}$ = don't care.

83YL-6981B

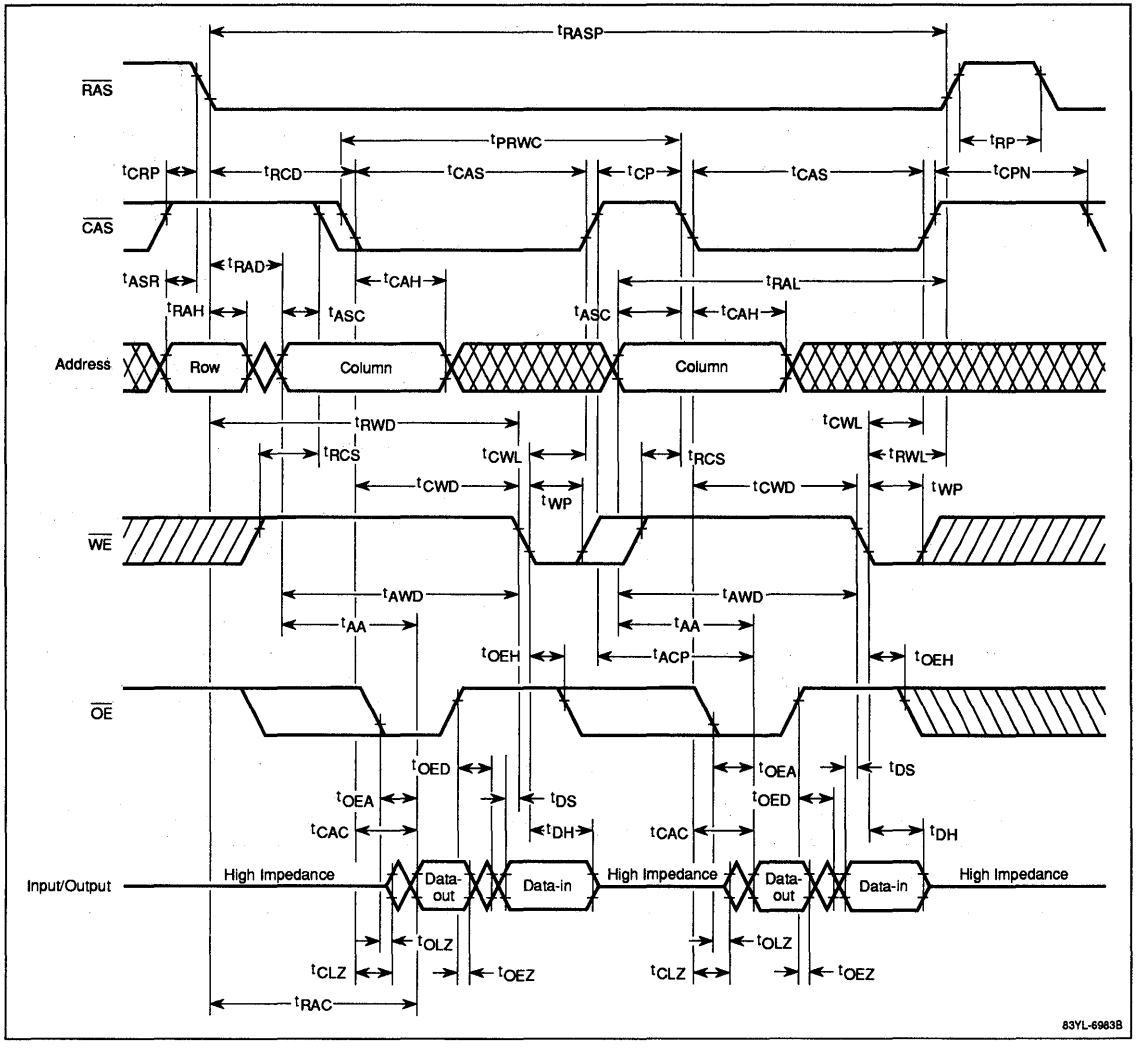
Timing Waveforms (cont)

Fast-Page Late Write Cycle



Timing Waveforms (cont)

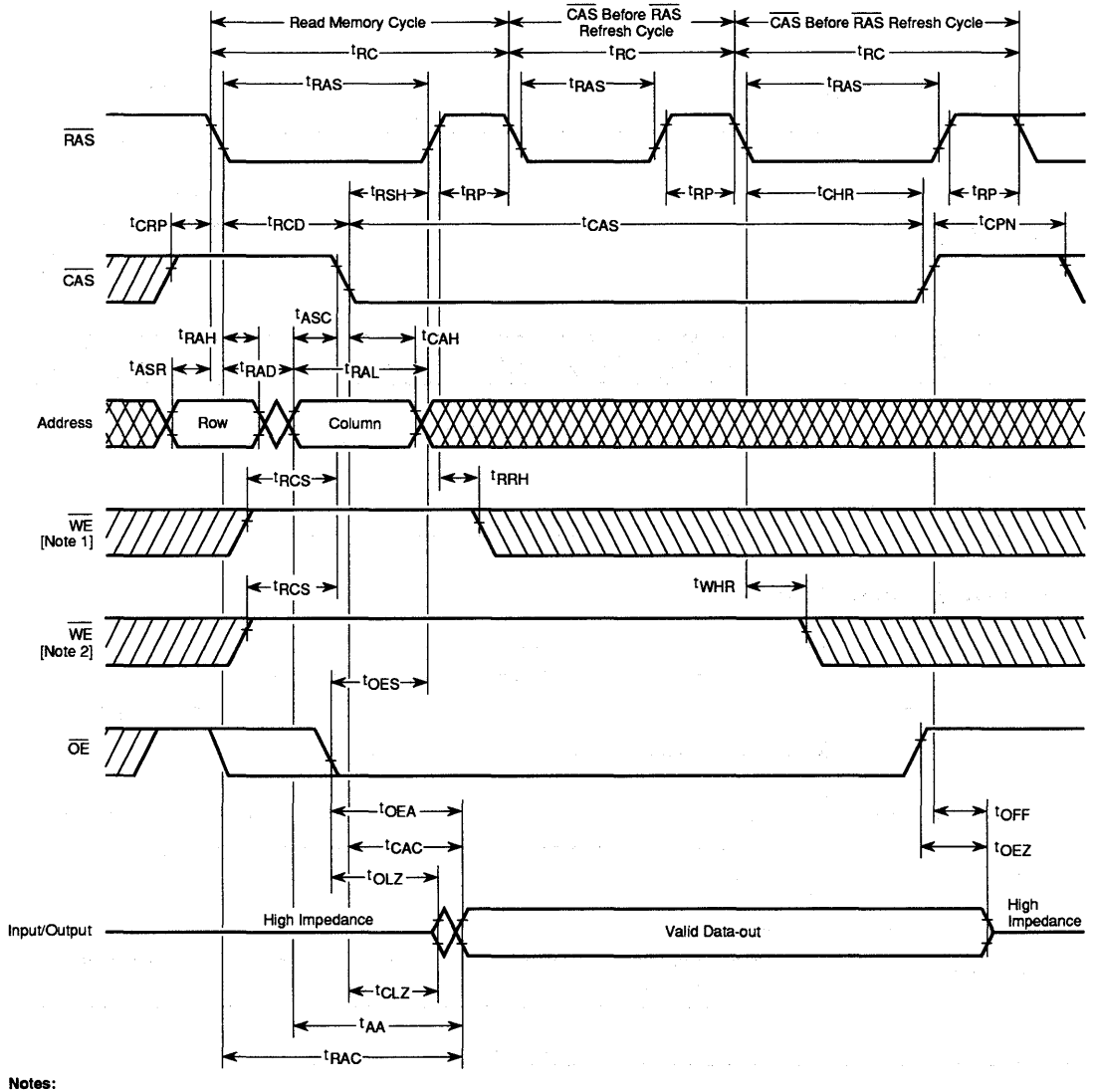
Fast-Page Read-Write/Read-Modify-Write Cycle



9h

Timing Waveforms (cont)

Hidden Refresh Cycle

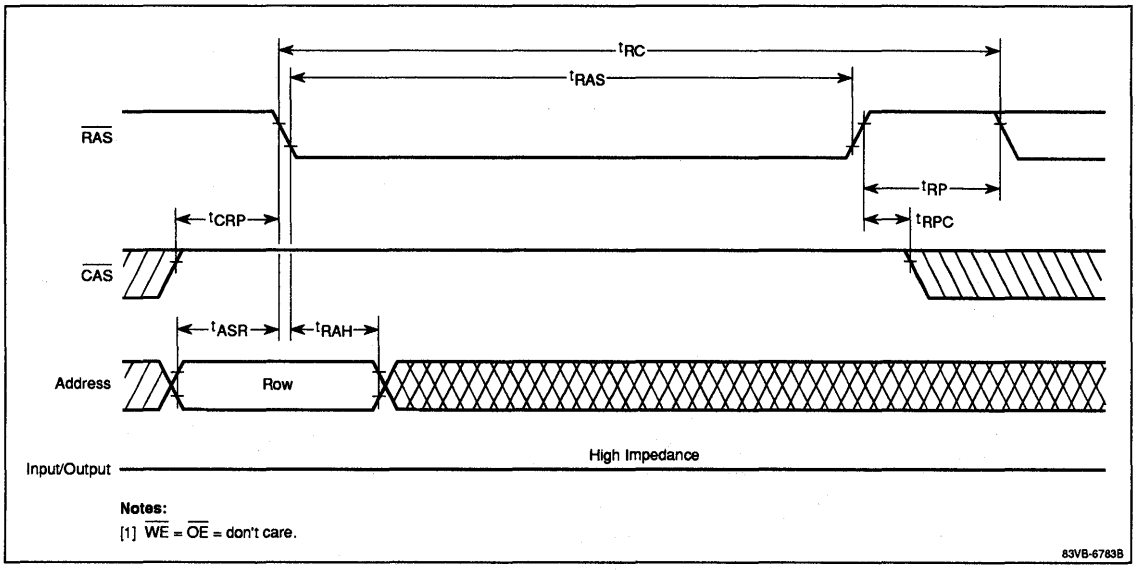


Notes:
[1] Applies only to MC-42512AA40.
[2] Applies only to MC-42512AB40.

83VB-8123B

Timing Waveforms (cont)

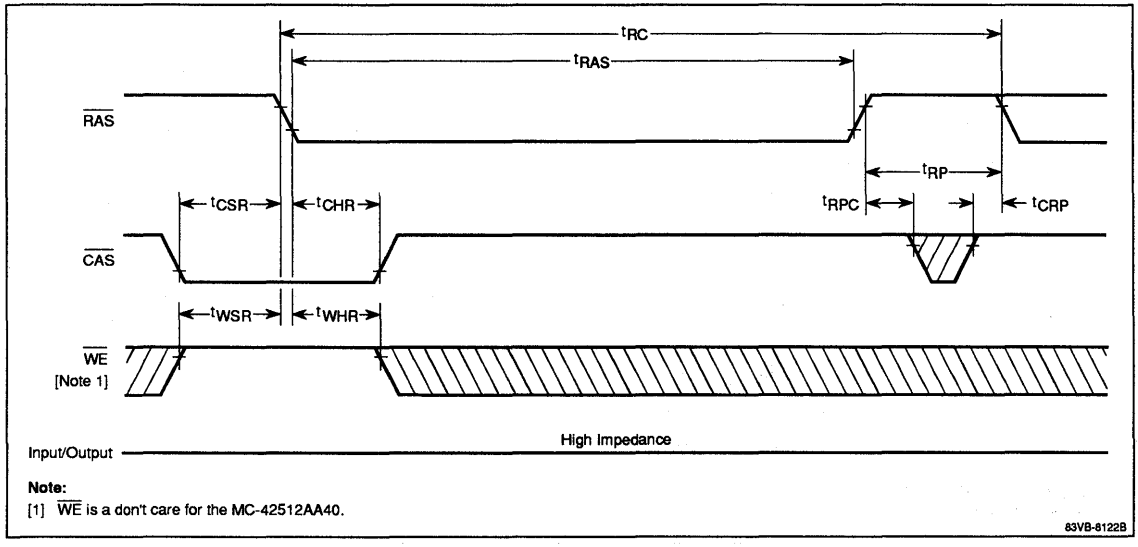
$\overline{RAS}$-Only Refresh Cycle



Notes:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

83VB-6783B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$ is a don't care for the MC-42512AA40.

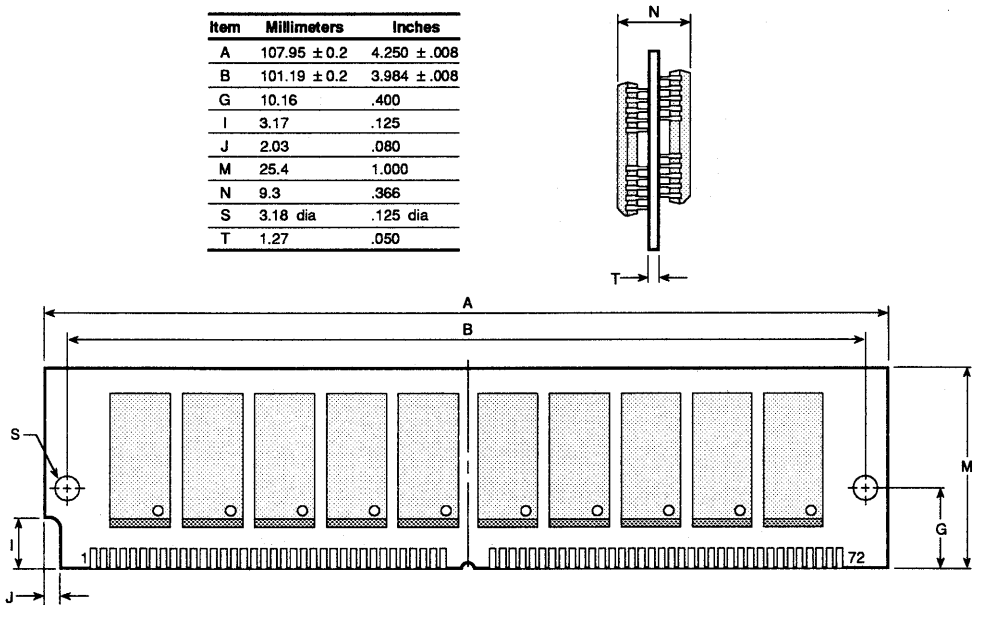
83VB-8122B

9h

Package Drawings

72-Pin Socket-Mountable SIMM (MC-42512AA40)

Item	Millimeters	Inches
A	107.95 ±0.2	4.250 ±.008
B	101.19 ±0.2	3.984 ±.008
G	10.16	.400
I	3.17	.125
J	2.03	.080
M	25.4	1.000
N	9.3	.366
S	3.18 dia	.125 dia
T	1.27	.050



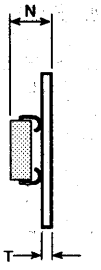
MC-42512AA40

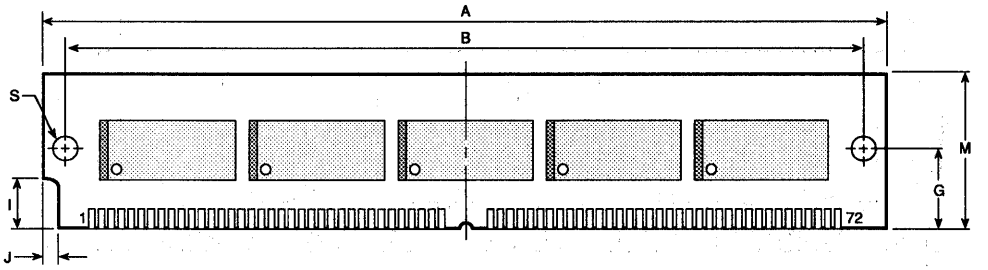
83FM-8126B (9/91)

Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-42512AB40)

Item	Millimeters	Inches
A	107.95 ±0.2	4.250 ± .008
B	101.19 ±0.2	3.984 ± .008
G	10.16	.400
I	6.35	.250
J	2.03	.080
M	25.4	1.000
N	5.08 max	.200 max
S	3.18 dia	.125 dia
T	1.27	.050





MC-42512AB40

83FM-8127B (9/91)

NEC

Section 10
DRAM Modules (1M/2M x n)

MC	Organization	Features	
-421000A8	1M x 8	Fast-page	10a
-421000A9	1M x 9	Fast-page	10b
-421000A32	1M x 32	Fast-page	10c
-421000A36	1M x 36	Fast-page	10d
-421000AA40, -421000AB40	1M x 40	Fast-page	10e
-422000A32	2M x 32	Fast-page	10f
-422000A36	2M x 36	Fast-page	10g
-422000AA40	2M x 40	Fast-page	10h

MC-421000A8
1,048,576 x 8-Bit
Dynamic CMOS RAM Module

Description

The MC-421000A8 is a fast-page 1,048,576-word by 8-bit dynamic RAM module designed to operate from a single +5-volt power supply. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles.

The MC-421000A8 is available with eight μPD421000 DRAMs (1M x 1) or two μPD424400 DRAMs (1M x 4) in a variety of 30-pin Single Inline Memory Modules (SIMMs™).

Features

- 1,048,576-word by 8-bit organization
- Single +5-volt power supply
- Eight 1M DRAMs or two 4M DRAMs in a 30-pin SIMM package
- Low power dissipation
- TTL-compatible inputs and outputs
- Fast-page option

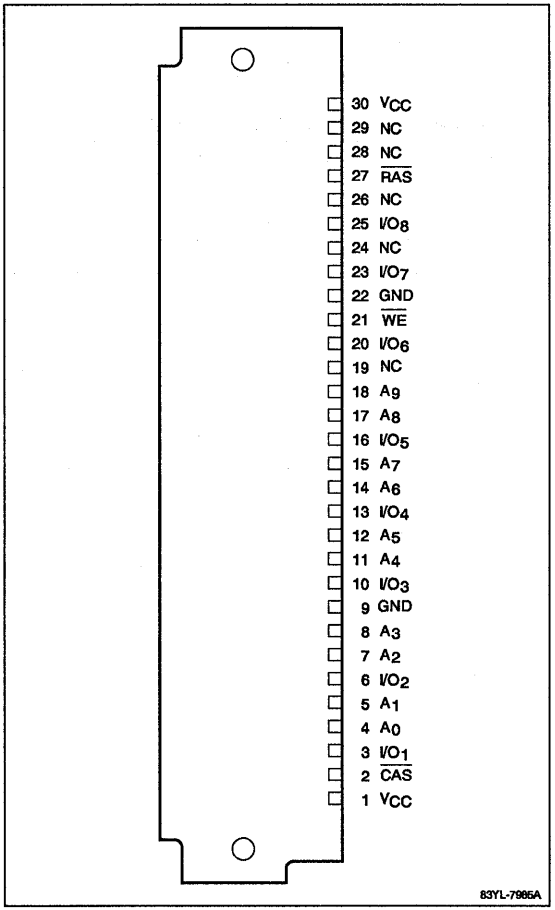
Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

SIMM is a trademark of Wang Laboratories.

Pin Configurations

30-Pin Socket-Mountable SIMM (MC-421000A8: Suffix B, F, BA, FA, BB, FB)



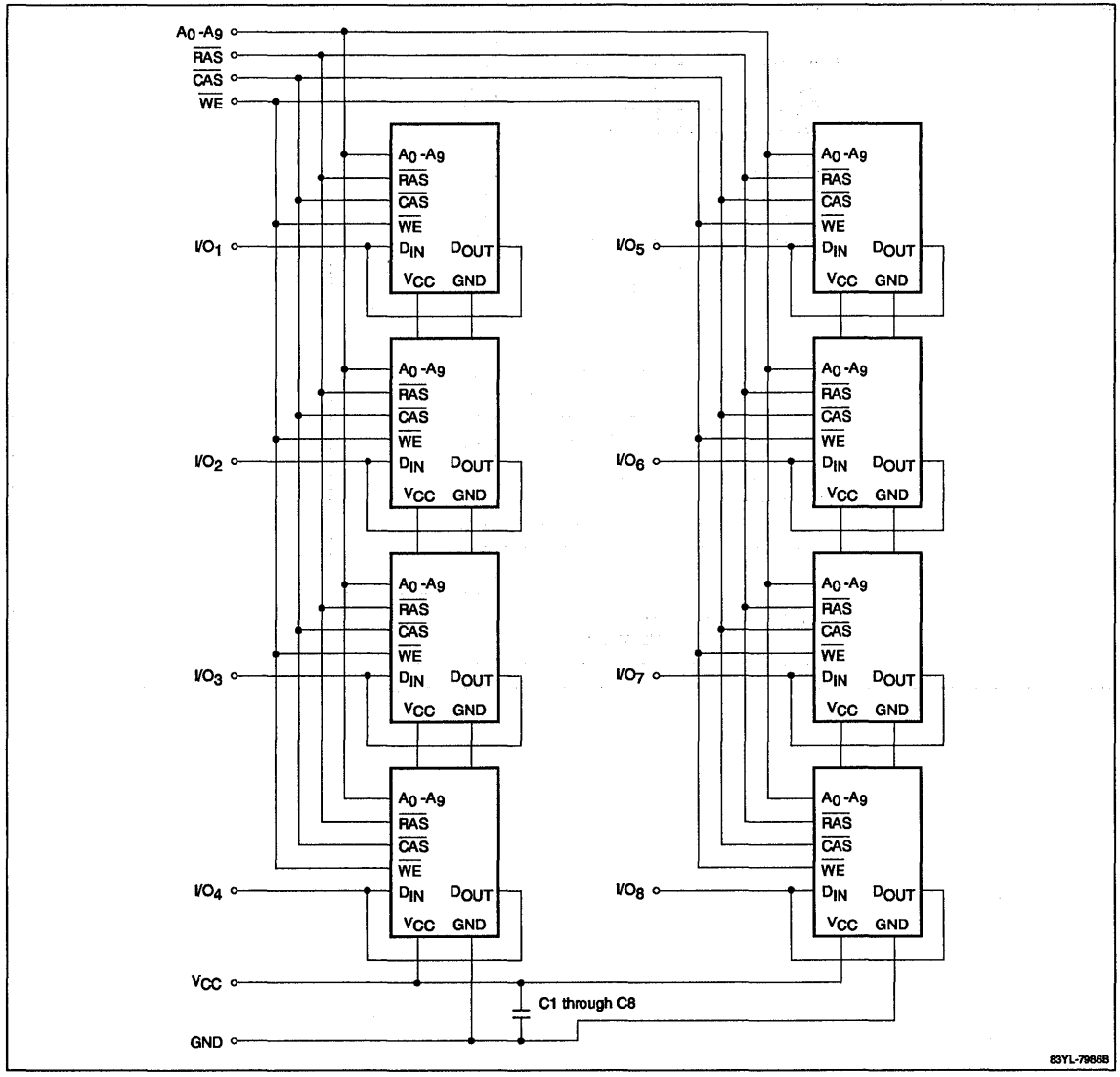
Ordering Information, Modules With Eight 1M x 1 DRAMs

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-421000A8B-60	60 ns	30-pin socket-mountable SIMM (solder plating)	20 mm (0.787 inch)	5.28 (0.208 inch)	Eight μPD421000LA
B-70	70 ns				
B-80	80 ns				
MC-421000A8F-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				

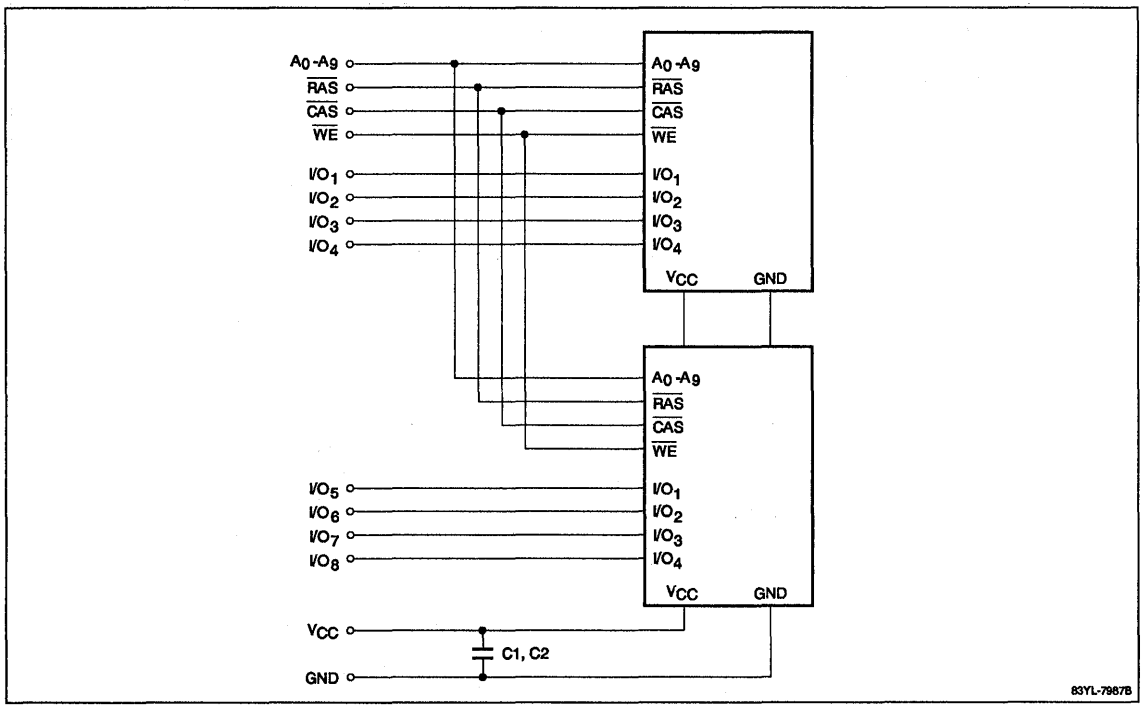
Ordering Information, Modules With Two 1M x 4 DRAMs

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-421000A8BA-60	60 ns	30-pin socket-mountable SIMM (solder plating)	16.67 mm (0.656 inch)	5.28 mm (0.208 inch)	Two μPD424400LA
BA-70	70 ns				
BA-80	80 ns				
MC-421000A8FA-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
FA-70	70 ns				
FA-80	80 ns				
MC-421000A8BB-60	60 ns	30-pin socket-mountable SIMM (solder plating)			
BB-70	70 ns				
BB-80	80 ns				
MC-421000A8FB-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
FB-70	70 ns				
FB-80	80 ns				

Connection Diagram; Modules With Eight 1M x 1 DRAMs



Connection Diagram; Modules With Two 1M x 4 DRAMs



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	
Modules with eight 1M x 1 DRAMs	8.0 W
Modules with two 1M x 4 DRAMs	2.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Ambient temperature	T_A	0		70	°C	
Input leakage current						
Modules with eight 1M x 1 DRAMs	I_{IL}	−80		80	μA	For Addresses, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: V_{IN} = 0 V to V_{CC}; other pins = 0 V
Modules with two 1M x 4 DRAMs	I_{IL}	−20		20	μA	
Output leakage current	I_{OL}	−10		10	μA	For I/O_1 - I/O_8: D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

Capacitance

T_A = 25°C; f = 1 MHz

		Modules With Eight 1M x 1 DRAMs		Modules With Two 1M x 4 DRAMs			
Parameter	Symbol	Min	Max	Min	Max	Unit	Pins Under Test
Input capacitance	C_{I1}		60		24	pF	Addresses, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Input/output capacitance	$C_{I/O}$		15		12	pF	I/O_1 - I/O_8

DC Characteristics; Modules With Eight 1M x 1 DRAMs

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		720		640		560	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Standby current	I_{CC2}		24		24		24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			8		8		8	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Refresh operating current, average	I_{CC3}		720		640		560	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Fast-page operating current, average	I_{CC4}		640		560		480	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		720		640		560	mA	t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)

DC Characteristics; Modules With Two 1M x 4 DRAMs

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		240		200		180	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Standby current	I_{CC2}		4		4		4	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			2		2		2	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Refresh operating current, average	I_{CC3}		240		200		180	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Fast-page operating current, average	I_{CC4}		180		160		140	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		240		200		180	mA	t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Access time from column address	t_{AA}		30		35		45	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 7, 11)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		ns	(Note 19)
Column address setup time	t_{ASC}	0		0		0	20	ns	(Note 11)
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		45		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 7, 9, 10, 11)
Column address hold time	t_{CAH}	15		17		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		ns	(Note 18)
Data setup time	t_{CLZ}	0		0		0		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	20	10	20	10	20	ns	(Note 11)
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 14)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	(Note 19)
Data-in hold time	t_{DH}	15		15		20		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		ns	(Note 19)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 17)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	ns	(Note 12)
Fast-page cycle time	t_{PC}	40		45		50		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	50	25	60	ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 15)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period Modules with eight 1M x 1 DRAMs	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
Modules with two 1M x 4 DRAMs	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 15)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		ns	(Note 19)
Write command setup time	t_{WCS}	0		0		0		ns	
$\overline{WE}$ hold time	t_{WHR}	15		15		15		ns	
Write command pulse width	t_{WP}	15		15		15		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max)

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(12) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(13) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) For early write operation, both t_{WCS} and t_{WCH} must be met.

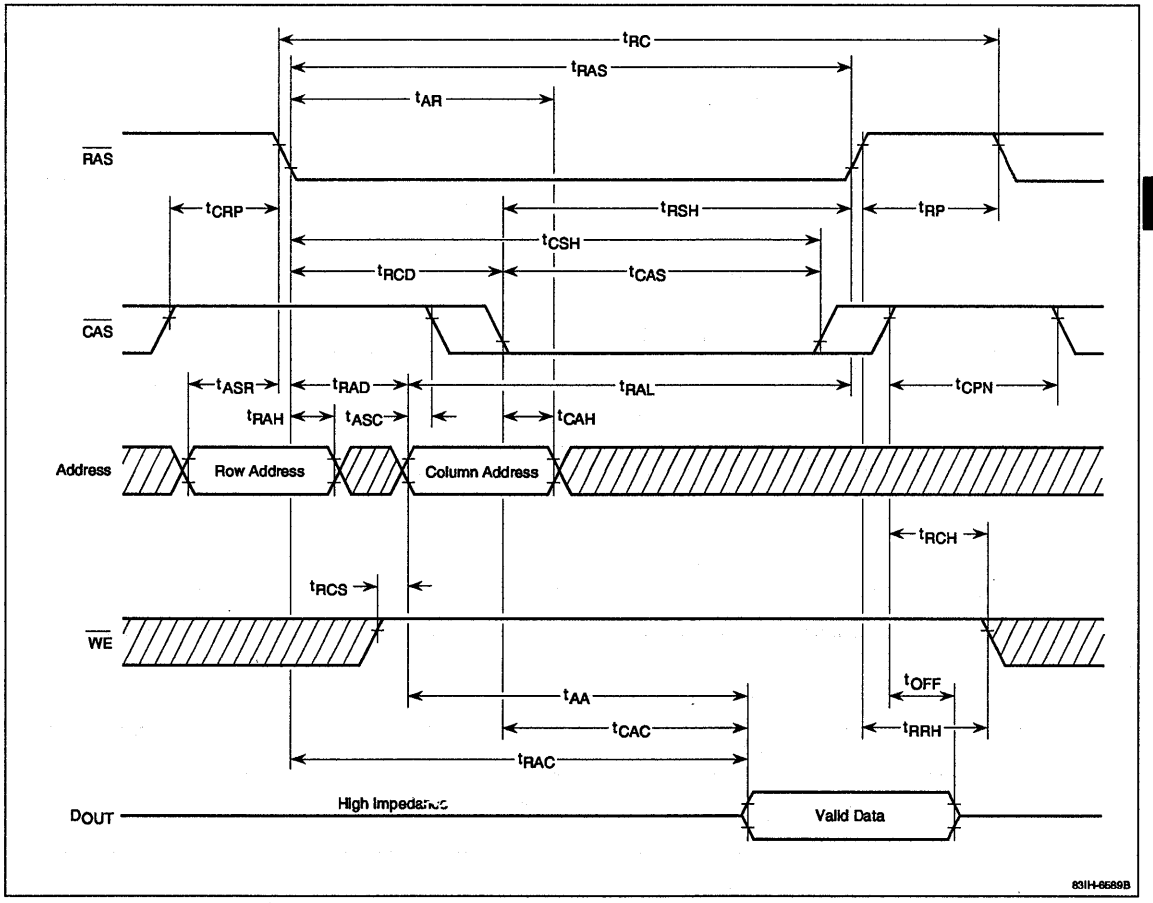
(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles.

(18) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

(19) This parameter is not needed for MC-421000A8-60/-70

Timing Waveforms

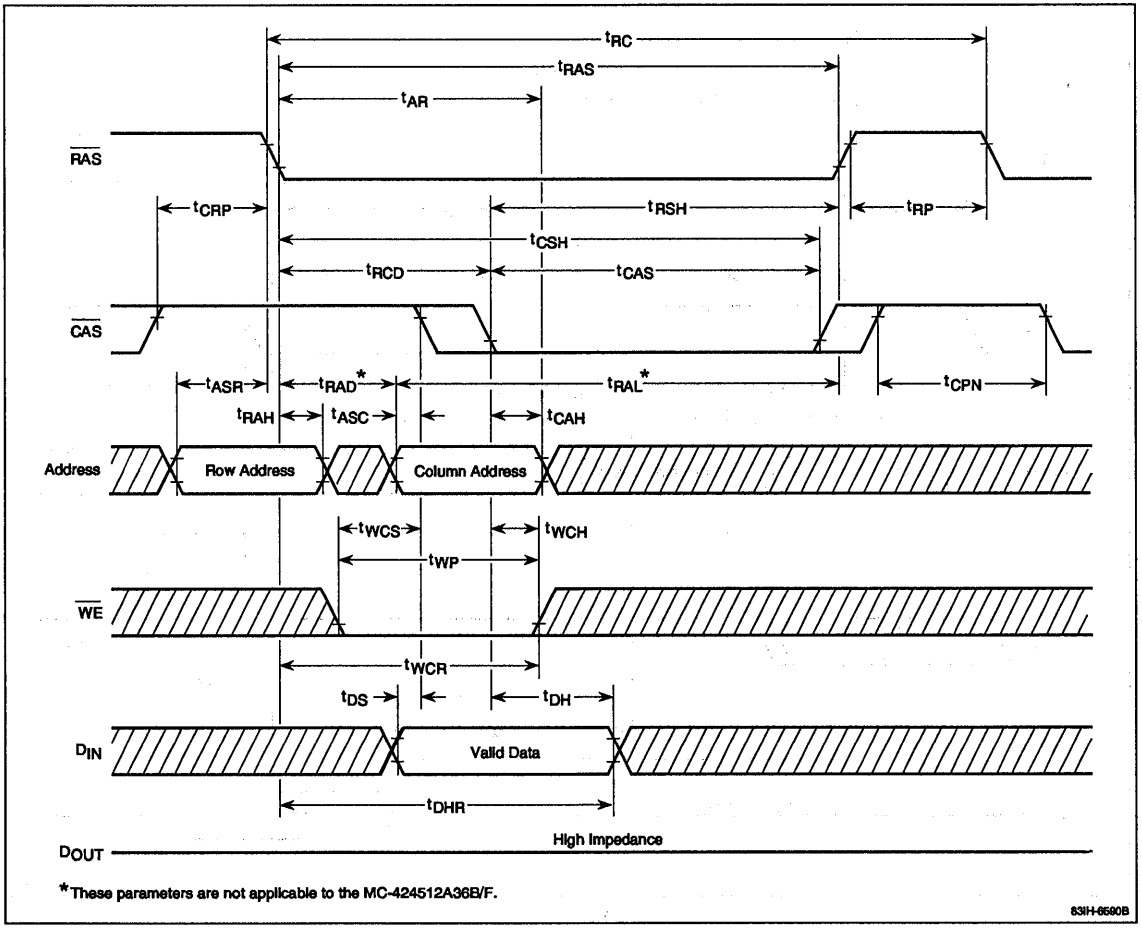
Read Cycle



10a

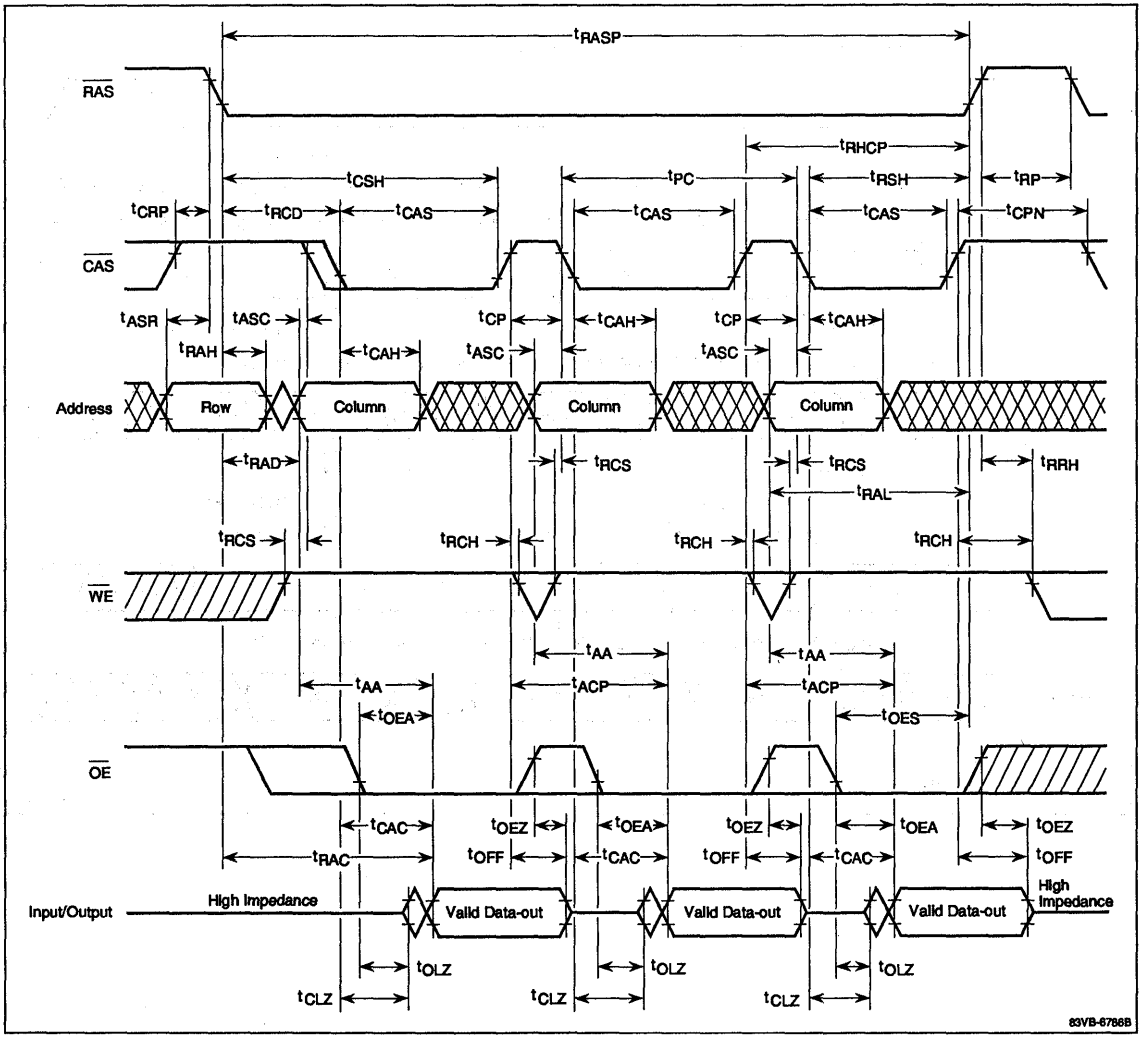
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

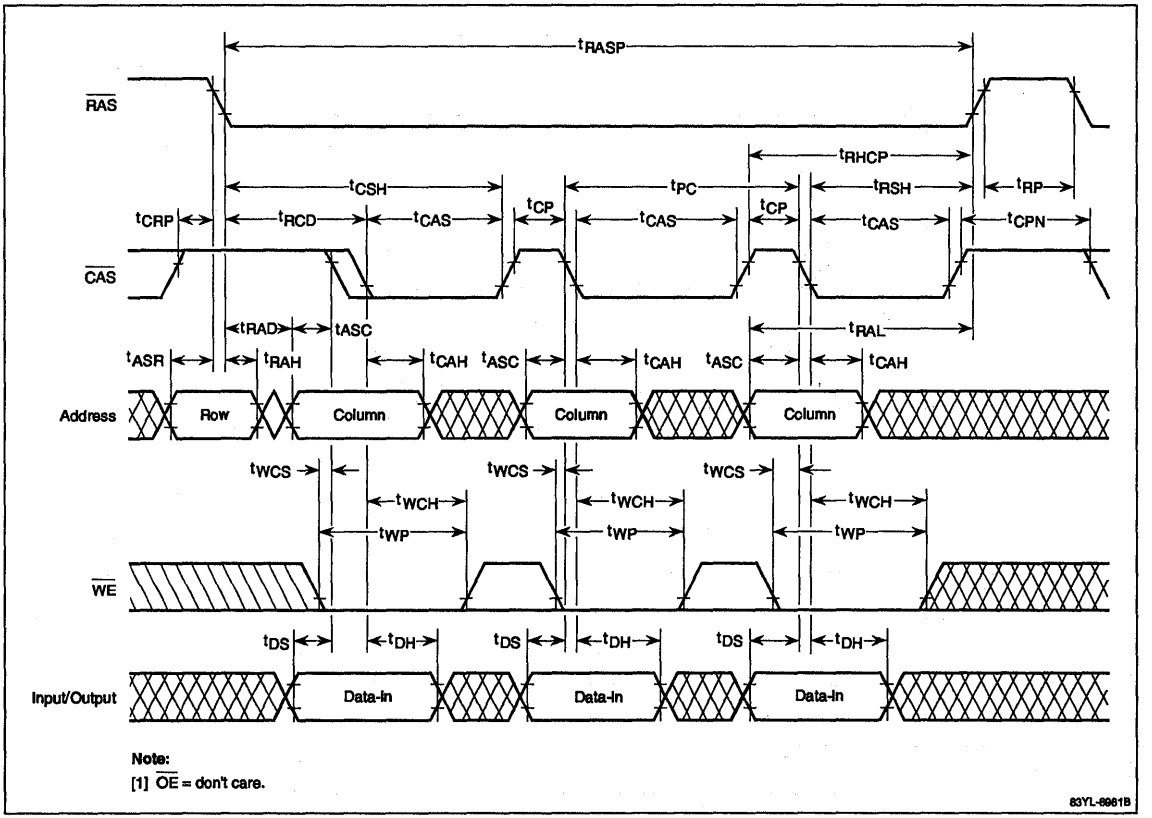
Fast-Page Read Cycle



10a

Timing Waveforms (cont)

Fast-Page Early Write Cycle

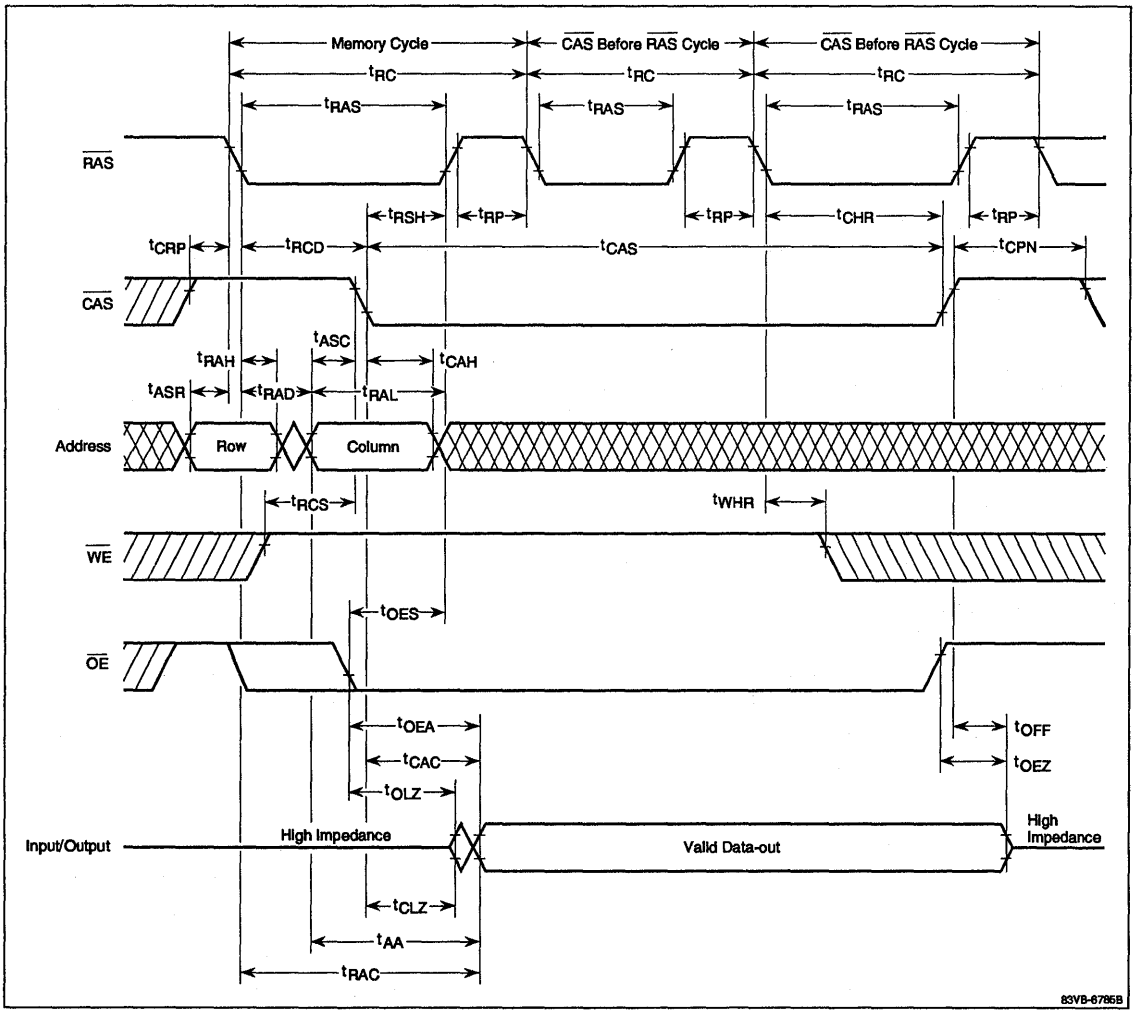


Note:
[1] $\overline{OE}$ = don't care.

83YL-6981B

Timing Waveforms (cont)

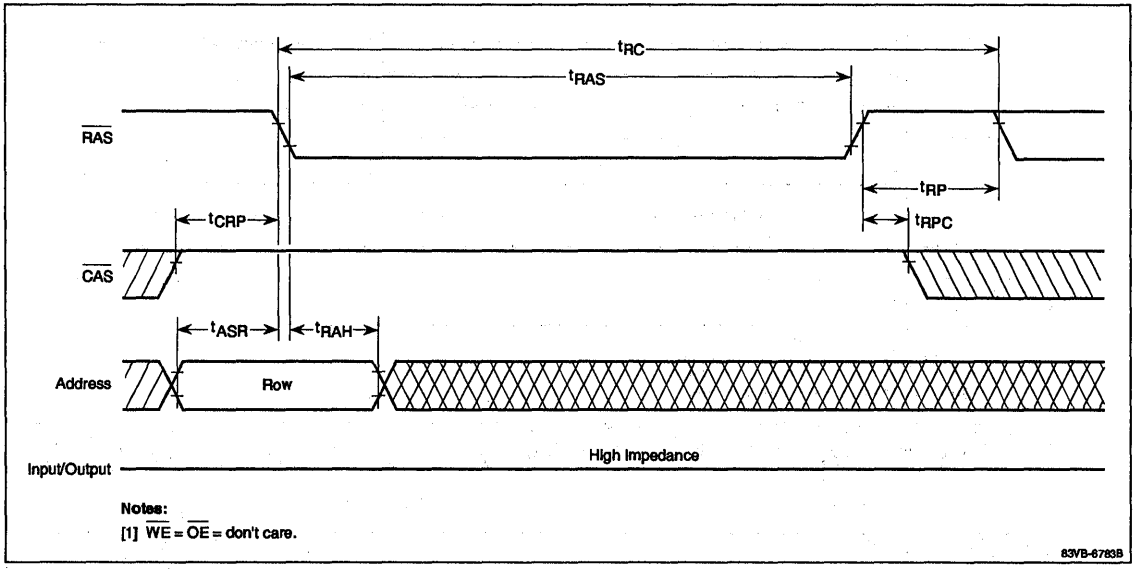
Hidden Refresh Cycle



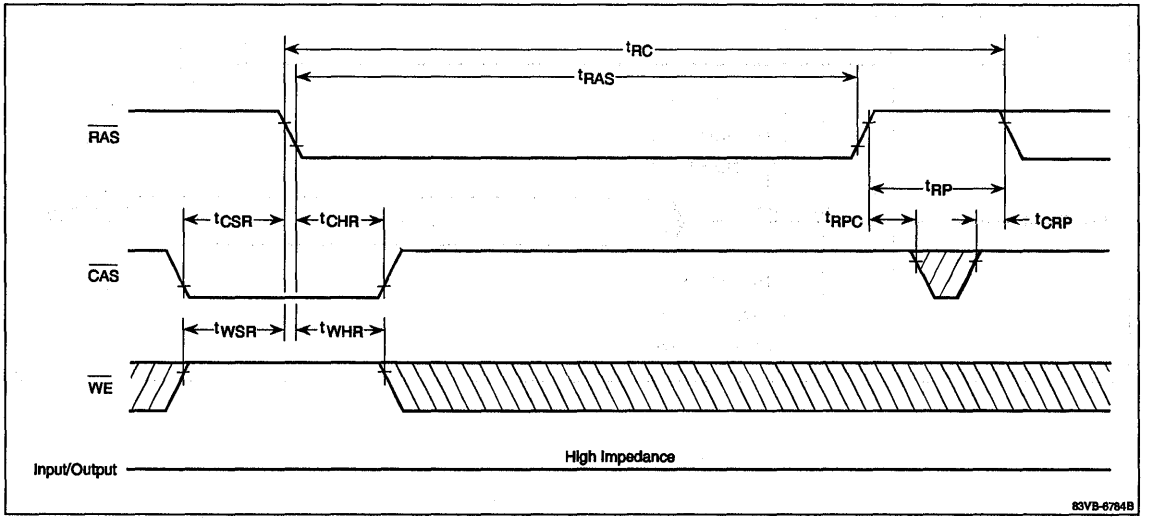
10a

Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



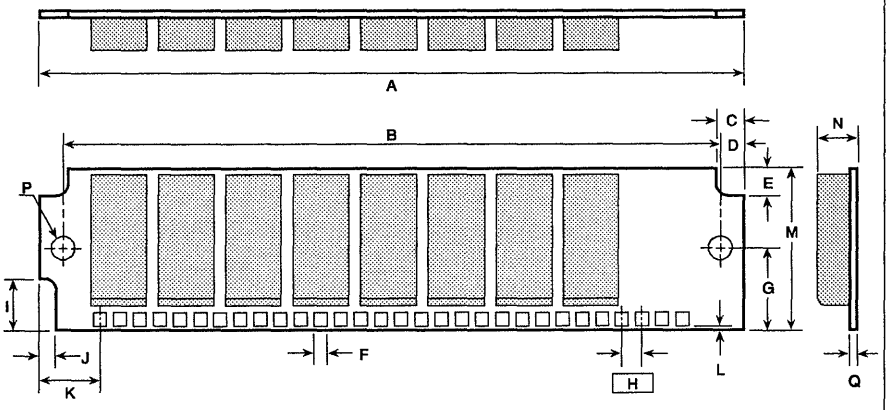
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Package Drawings

30-Pin Socket-Mountable SIMM (MC-421000A8: Suffix B, F)

Item	Millimeters	Inches
A	88.9 ± 0.5	3.500 ± .020
B	82.14	3.234
C	3.56	.140
D	3.38	.133
E	3.5	.138
F	1.77	.070
G	10.16	.400
H	2.54 (T.P.)	.100 (T.P.)
I	6.35	.250
J	2.03	.080
K	7.62	.300
L	0.2	.008
M	20.0	.787
N	5.28 max	.208 max
P	3.18 dia	.125 dia
Q	1.27 ± 0.15	.050 ± .006

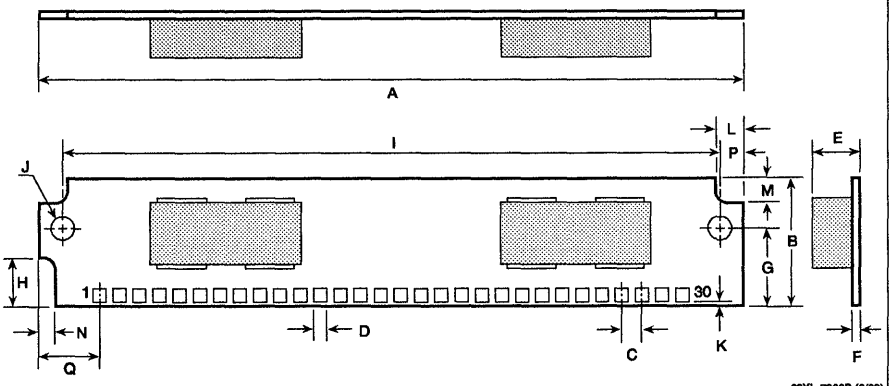


MC-421000A8: B, F

83YL-7991B (8/92)

30-Pin Socket-Mountable SIMM (MC-421000A8: Suffix BA, FA, BB, FB)

Item	Millimeters	Inches
A	88.9 ± 0.5	3.500 ± .020
B	16.67	.656
C	2.54 [TP]	.100 [TP]
D	1.77	.070
E	5.28 max	.208 max
F	1.27 ± 0.15	.050 ± .006
G	10.16	.400
H	6.35	.250
I	82.14	3.234
J	3.18 dia	.125 dia
K	0.2	.008
L	3.56	.140
M	3.5	.138
N	2.03	.080
P	3.38	.133
Q	7.62	.300



MC-421000A8: BA, FA, BB, FB

83YL-7989B (8/92)

10a

NEC Electronics Inc.

MC-421000A9
1,048,576 x 9-Bit
Dynamic CMOS RAM Module

Description

The MC-421000A9 is a fast-page 1,048,576-word by 9-bit dynamic RAM module designed to operate from a single +5-volt power supply.

The module is functionally equivalent to nine standard 1M DRAMs plus a parity bit. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles

The MC-421000A9 consists of nine 1M x 1 DRAMs (μPD421000) or two 1M x 4 DRAMs (μPD424400) and one 1M x 1 DRAM (μPD421000). Packaging is in a variety of 30-pin Single Inline Memory Modules (SIMM ™).

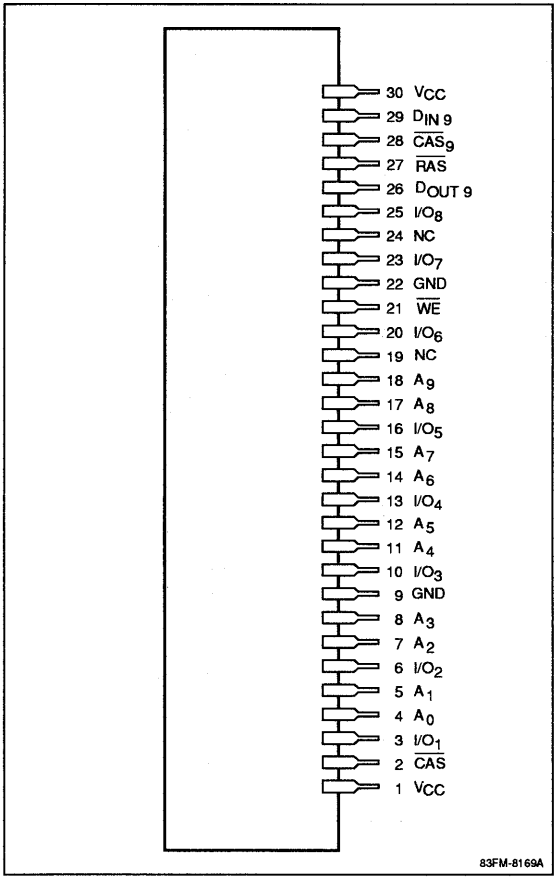
Features

- 1,048,576-word by 9-bit organization
- Single +5-volt power supply
- Standard 30-pin Single Inline Memory Module (SIMM) packaging
- Version 1: nine 1M x 1 DRAMs
- Version 2: two 1M x 4 DRAMs and one 1M x 1 DRAM
- Includes power supply decoupling capacitors
- Low power dissipation
- TTL-compatible inputs and outputs
- Fast-page capability

SIMM is a trademark of Wang Laboratories.

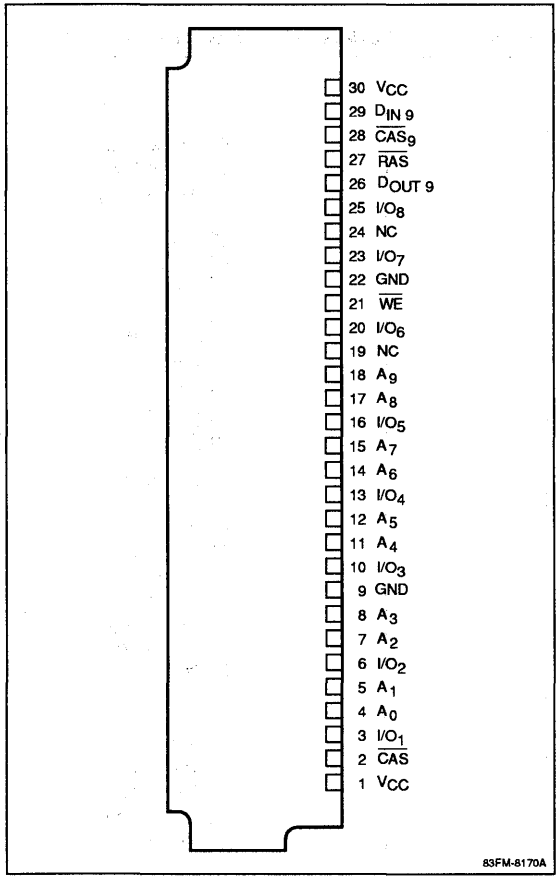
Pin Configurations

30-Pin Leaded SIMM (MC-421000A9A/AA/AB)



Pin Configurations (cont)

30-Pin Socket-Mountable SIMM (MC-421000A9B/BA/BB/F/FA/FB)



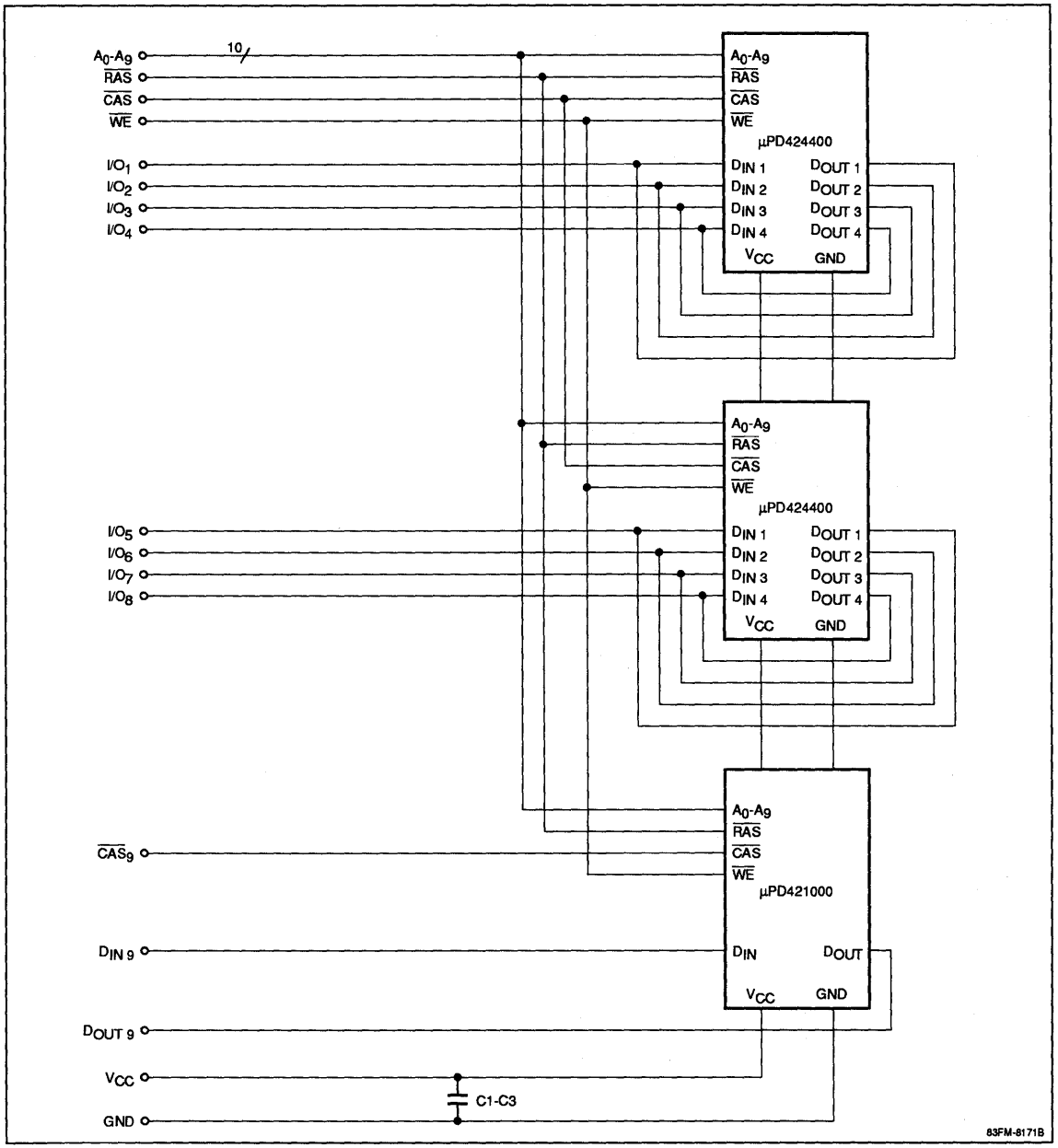
Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
$\overline{CAS}$	Column address strobe
$\overline{CAS}_9$	Column address strobe for data output 9
$D_{IN\ 9}$	Data input 9
$D_{OUT\ 9}$	Data output 9
I/O_1 - I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

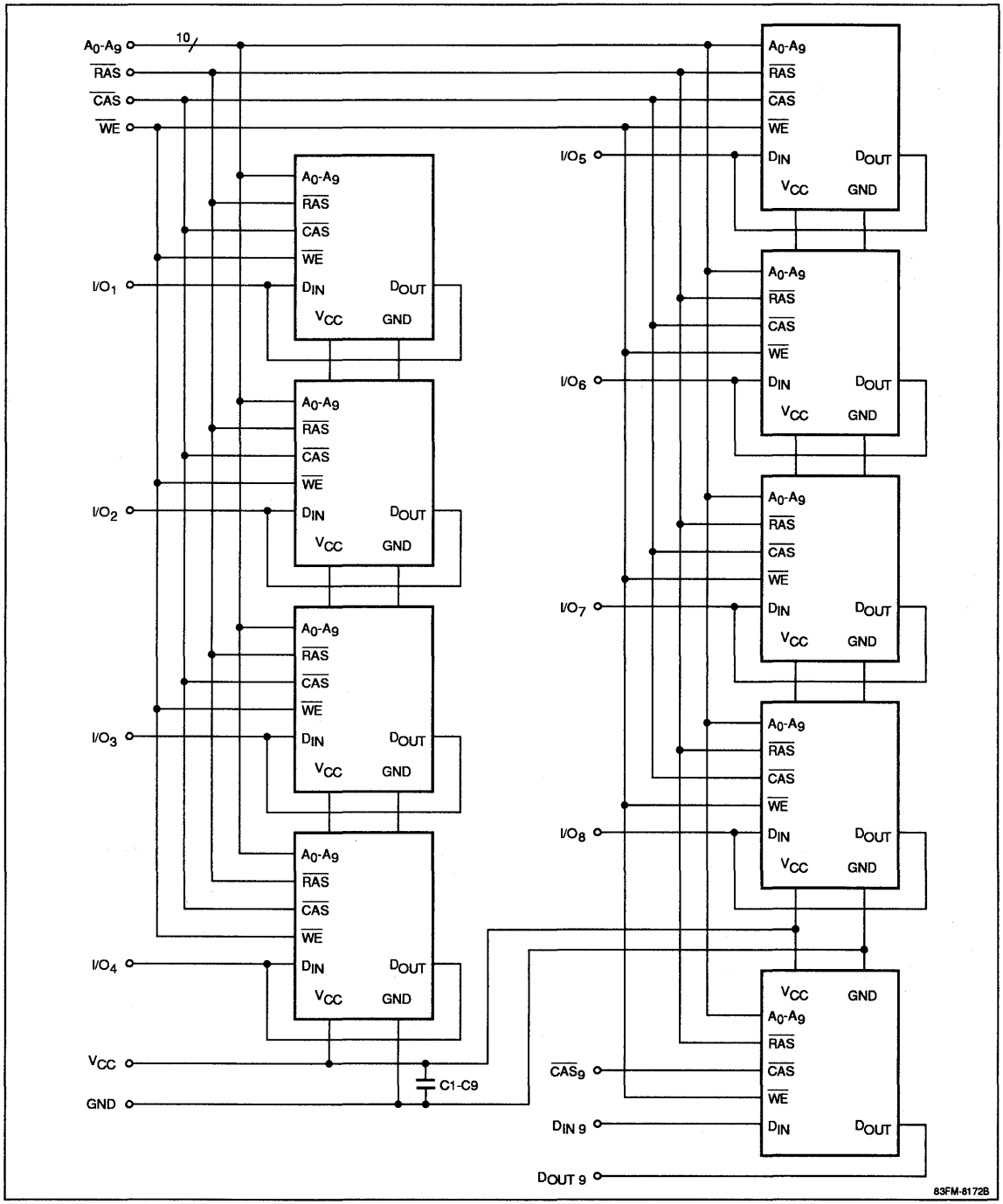
Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-421000A9A-60	60 ns	30-pin leaded SIMM (solder plating)	20.0 mm (0.787 inch)	5.28 mm (0.208 inch)	Nine μPD421000LA
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9B-60	60 ns	30-pin socket-mountable SIMM (solder plating)			
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9F-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9AA-60	60 ns	30-pin leaded SIMM (solder plating)	16.8 mm (0.661 inch)	5.08 mm (0.200 inch)	Two μPD424400LA One μPD421000LA
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9BA-60	60 ns	30-pin socket-mountable SIMM (solder plating)			
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9FA-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9AB-60	60 ns	30-pin leaded SIMM (solder plating)	16.8 mm (0.661 inch)	5.08 mm (0.200 inch)	Two μPD424400LB One μPD421000LA
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9BB-60	60 ns	30-pin socket-mountable SIMM (solder plating)			
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9FB-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
-70	70 ns				
-80	80 ns				
-10	100 ns				

Connection Diagram, MC-421000A9AA/BA/FA/AB/BB/FB



Connection Diagram, MC-421000A9A/B/F



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D MC-421000A9A/B/F	9.0 W
Power dissipation, P_D MC-421000A9AA/BA/FA/AB/BB/FB	3.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	MC-421000A9A/B/F	MC-421000A9AA/BA/FA/AB/BB/FB	Unit	Pins Under Test
Input capacitance, max	C_{I1}	70	31	pF	A_0 - A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
	C_{I2}	7	17	pF	$\overline{CAS}_9$, $D_{IN\ 9}$
Input/output capacitance, max	C_D	15	12	pF	I/O_1 - I/O_8
Output capacitance, max	C_O	10	17	pF	$D_{OUT\ 9}$

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current (Note 1)	I_{CC2}			18	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}
				9	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Standby current (Note 2)	I_{CC2}			6	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}
				3	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current (Note 1)	I_{IL}	−90		90	μA	For A_0 - A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
	I_{IL9}	−10		10	μA	For $\overline{CAS}_9$ and $D_{IN\ 9}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
Input leakage current (Note 2)	I_{IL}	−30		30	μA	For A_0 - A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
	I_{IL9}	−10		10	μA	For $\overline{CAS}_9$ and $D_{IN\ 9}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1 - I/O_8 and $D_{OUT\ 9}$: D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

Notes:

(1) Applicable to MC-421000A9A/B/F, which consists of nine 1M x 1 DRAMs (μPD421000).

(2) Applicable to MC-421000A9AA/BA/FA/AB/BB/FB, which consists of two 1M x 4 DRAMs (μPD424400) and one 1M x 1 DRAM (μPD421000).

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1} (Note 21)		810		720		630		540	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
	I_{CC1} (Note 22)		330		280		250		220	mA	
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (Note 21)		810		720		630		540	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
	I_{CC3} (Note 22)		330		280		250		220	mA	
Operating current, fast-page cycle, average	I_{CC4} (Note 21)		720		630		540		450	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
	I_{CC4} (Note 22)		260		230		200		170	mA	
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (Note 21)		810		720		630		540	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min (Note 5)
	I_{CC5} (Note 22)		330		280		250		220	mA	
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 11)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		70		ns	
Column address setup time	t_{ASC}	0		0		0		0		ns	(Note 11)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		40		50		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10, 11)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}		0		0		0		0	ns	(Note 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		10		ns	(Note 11)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 14)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 17)

10b

AC Characteristics (cont)

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 17)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	10,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 15)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_9 (Note 21)
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9 (Note 22)
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 15)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	145		165		185		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	
Write command	t_{WHR}	15		15		15		20			

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 16)
Write command	t_{WSR}	10		10		10		10			

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) For fast-page read operation, the definition of access time is as follows:

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{CAC}

(12) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(13) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) For D_{OUT9}, parameters t_{WCS}, t_{CWD}, t_{RWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of $D_{OUT\,9}$ (at access time and until $\overline{CAS_9}$ returns to V_{IH}) is indeterminate.

(19) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

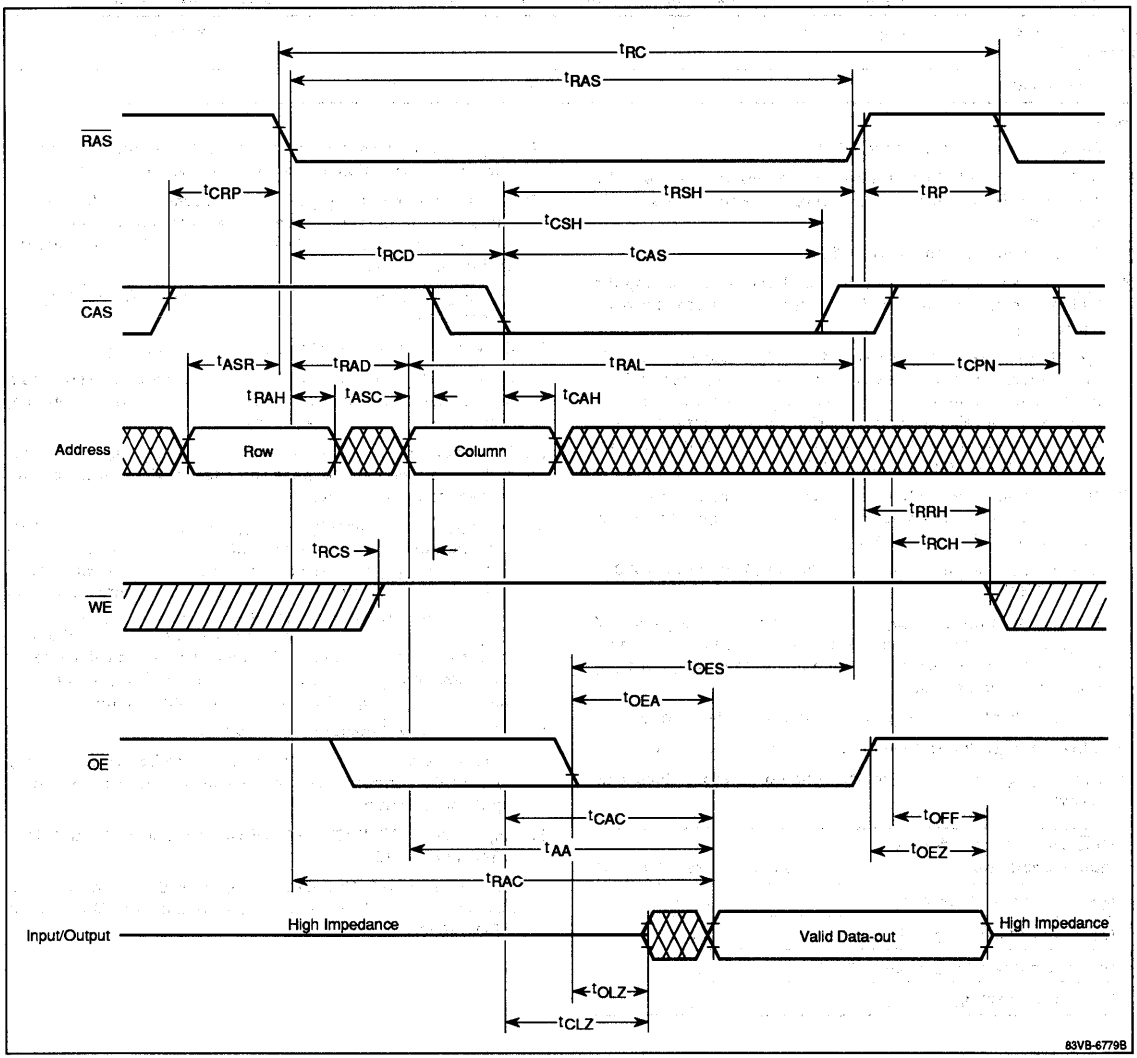
(20) Read-write/read-modify-write operation can be performed only by the SOJ controlled by $\overline{CAS_9}$ because of its separate data input and output pins.

(21) Applicable to MC-421000A9A/B/F, which consists of nine 1M x 1 DRAMs (μPD421000).

(22) Applicable to MC-421000A9AA/BA/FA/AB/BB/FB, which consists of two 1M x 4 DRAMs (μPD424400) and one 1M x 1 DRAM (μPD421000).

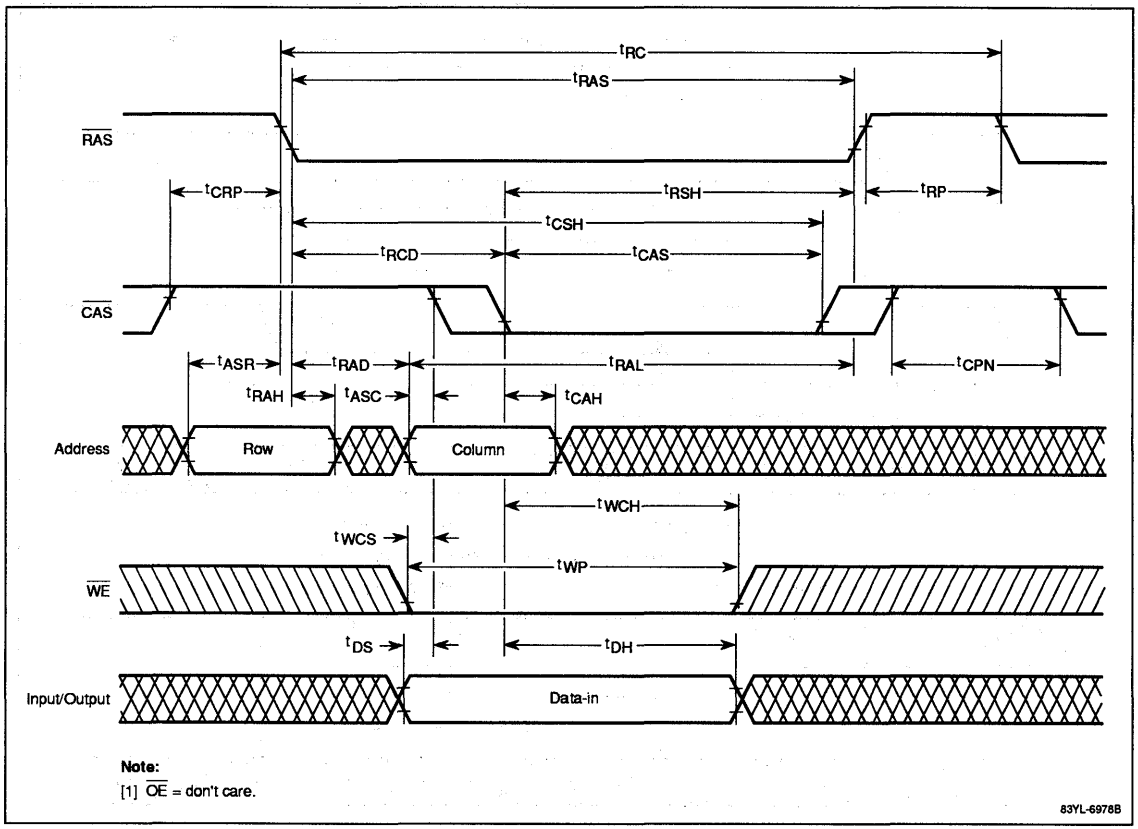
Timing Waveforms

Read Cycle



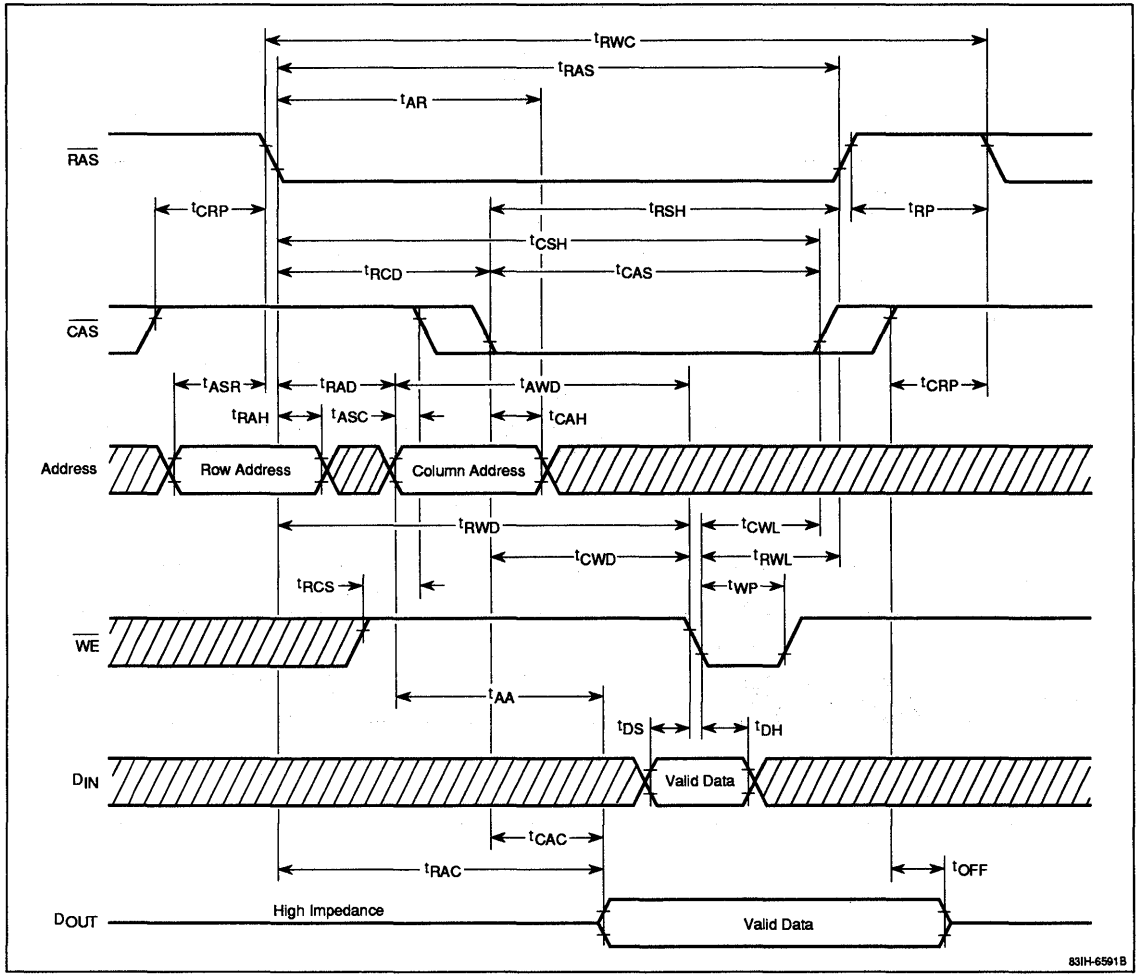
Timing Waveforms (cont)

Early Write Cycle



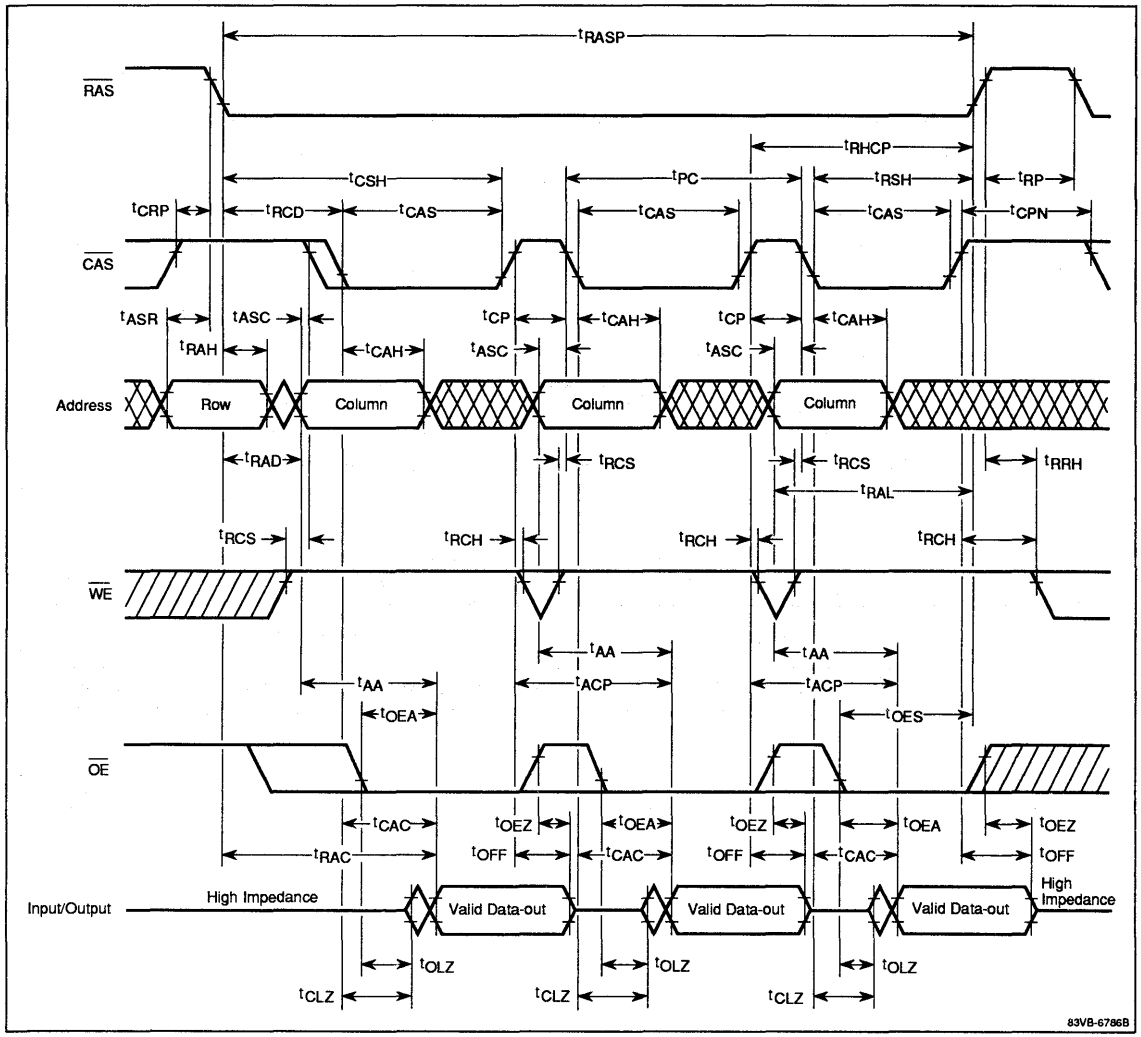
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle (D_{OUT9} only)



Timing Waveforms (cont)

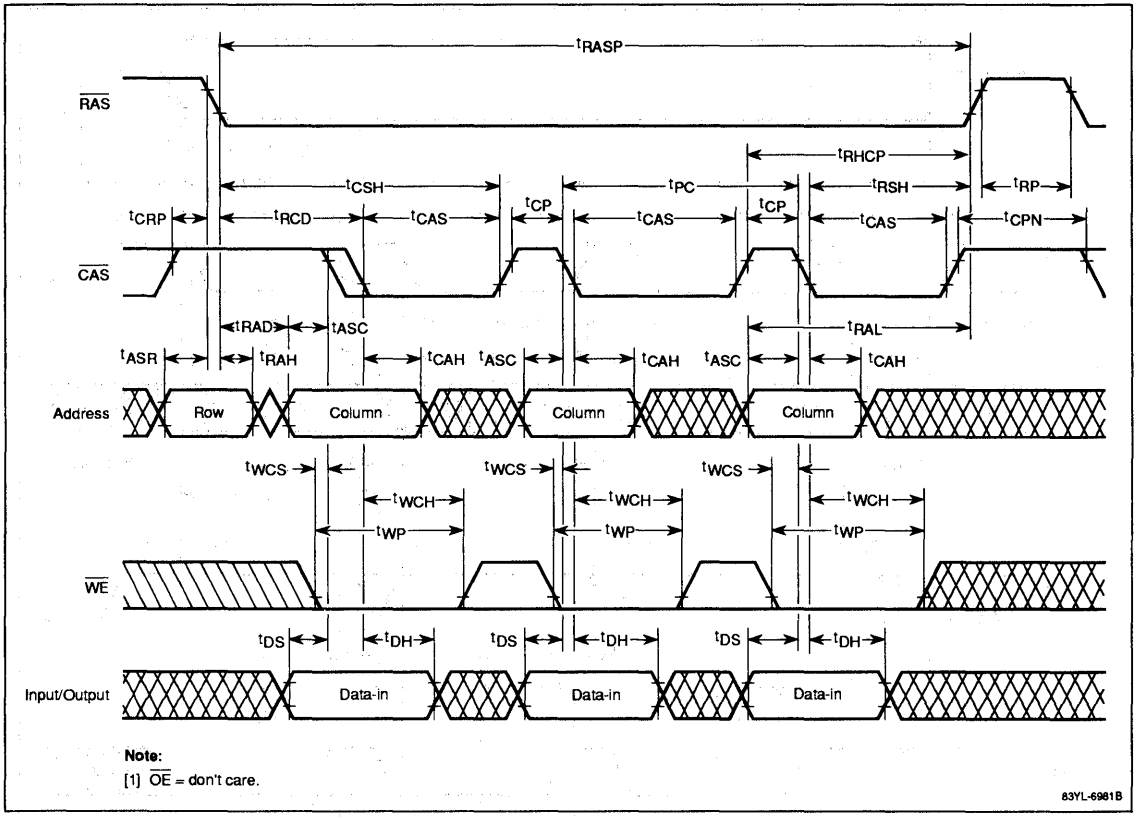
Fast-Page Read Cycle



10b

Timing Waveforms (cont)

Fast-Page Early Write Cycle

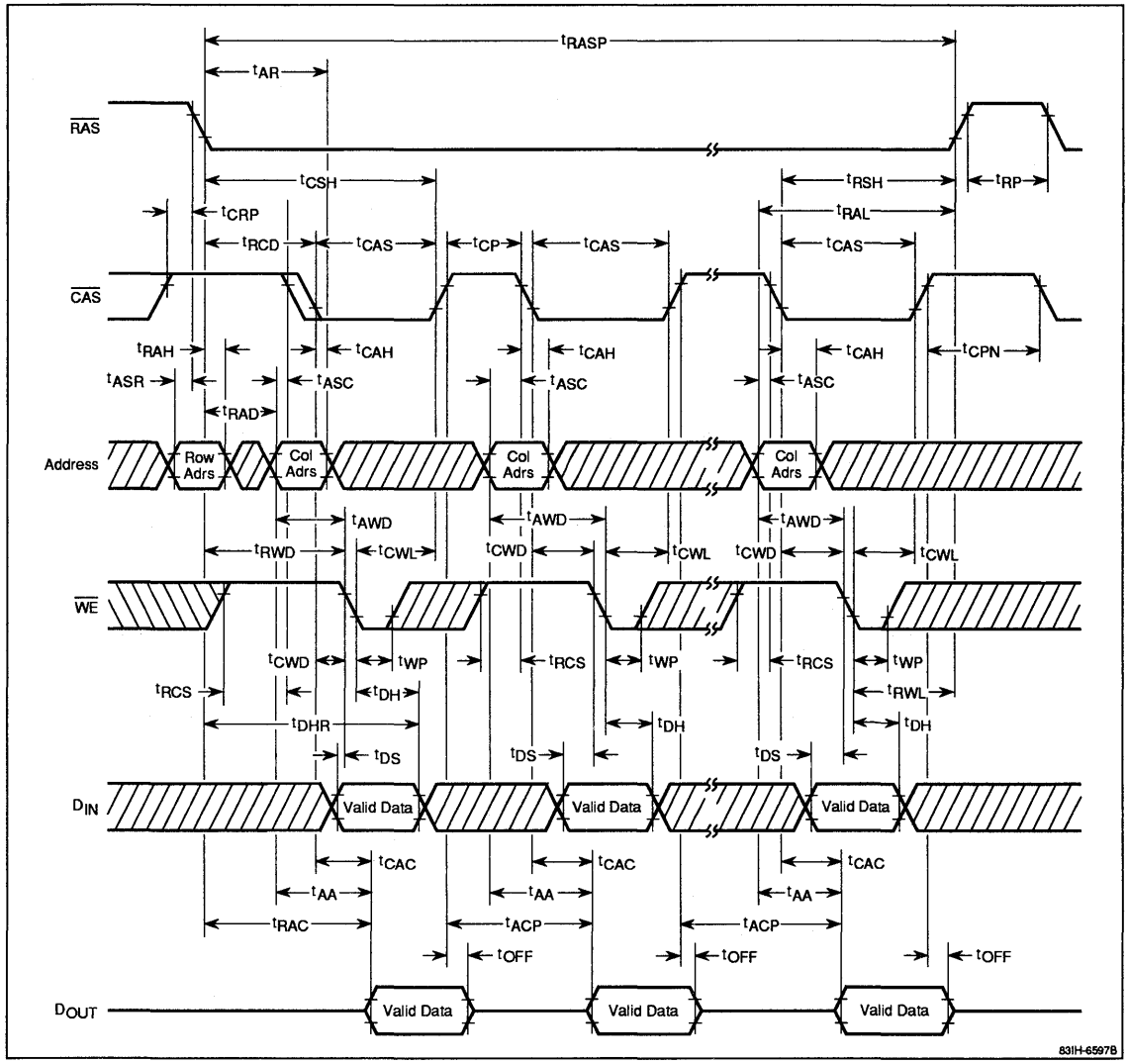


Note:
[1] $\overline{OE}$ = don't care.

83YL-6981B

Timing Waveforms (cont)

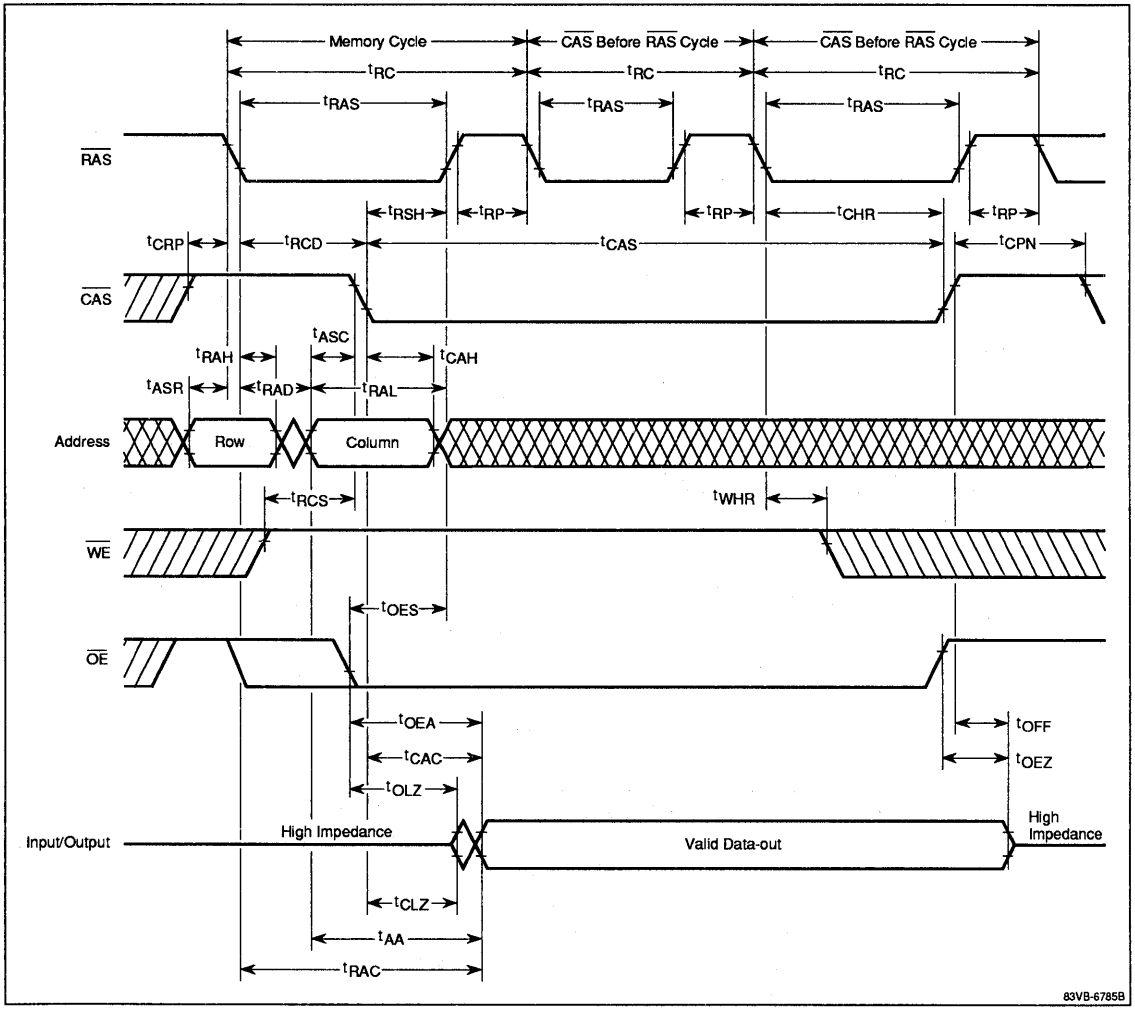
Fast-Page Read-Write/Read-Modify-Write Cycle (D_{OUT} only)



10b

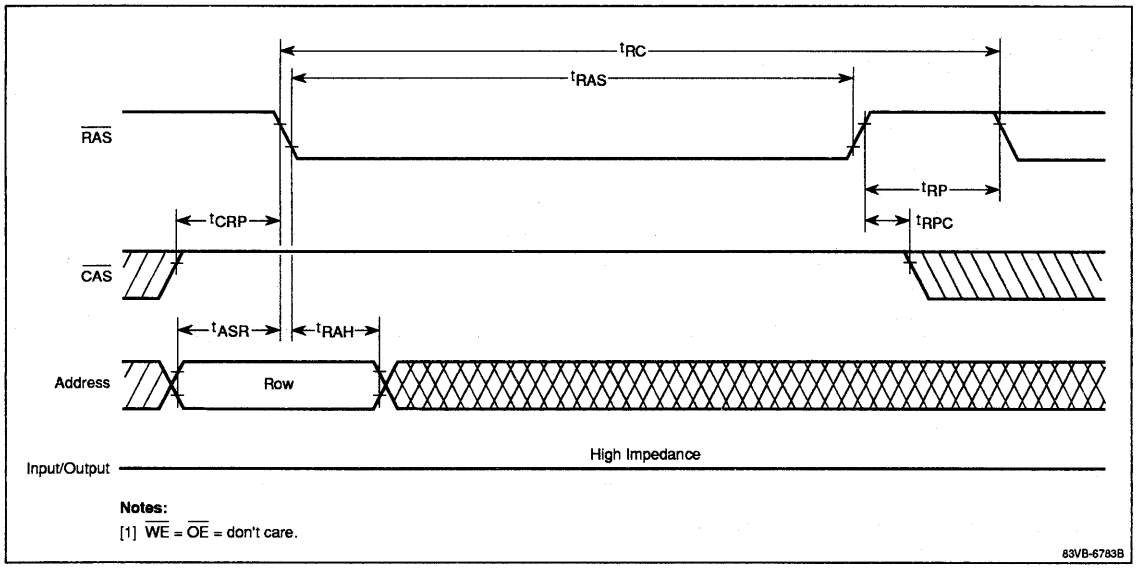
Timing Waveforms (cont)

Hidden Refresh Cycle

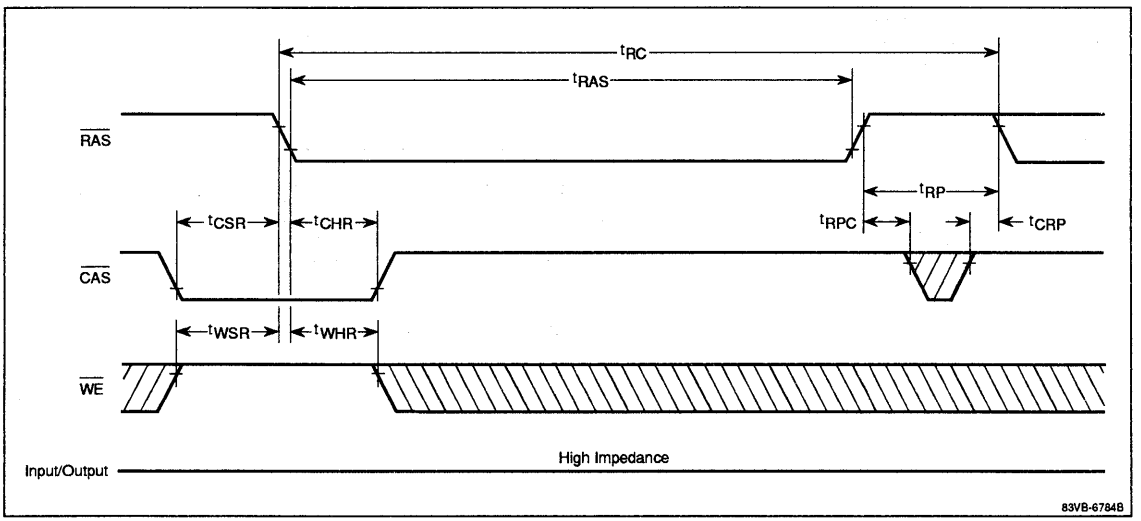


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



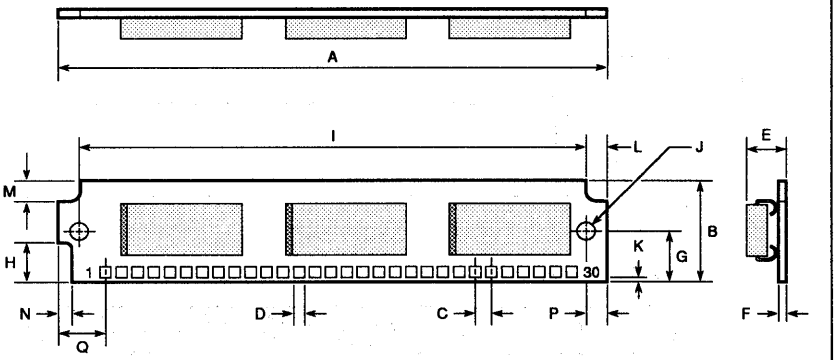
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Package Drawings

30-Pin Socket-Mountable SIMM (MC-421000A9BA/FA/BB/FB)

Item	Millimeters	Inches
A	88.9 ±0.5	3.5 ±.020
B	16.67	.656
C	2.54 [TP]	.100 [TP]
D	1.77	.070
E	5.28 max	.208 max
F	1.27 ±0.15	.050 ±.006
G	10.16	.400
H	6.35	.250
I	82.14	3.234
J	3.18 dia	.125 dia
K	0.2	.008
L	3.56	.140
M	3.5	.138
N	2.03	.080
P	3.38	.133
Q	7.62	.300

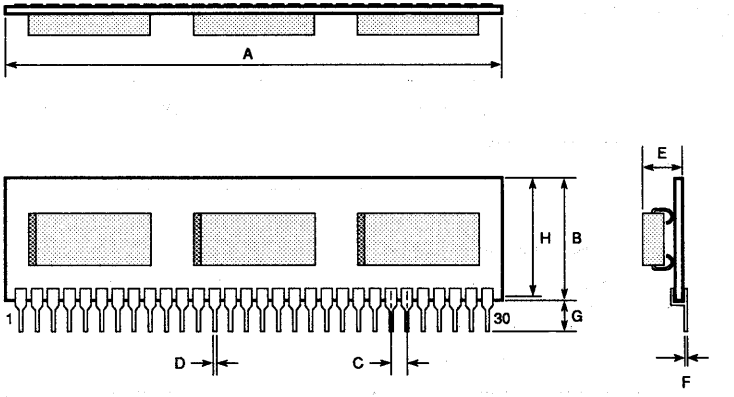


MC-421000A9/BA/FA/BB/FB

83FM-8173B (10/91)

30-Pin Leaded SIMM (MC-421000A9AA/AB)

Item	Millimeters	Inches
A	80.3 ± 0.5	3.161 $^{+.021}_{-.020}$
B	18.27 max	.719 max
C	2.54 [TP]	.100 [TP]
D	0.50	.020
E	5.5 max	.208 max
F	0.25	.010
G	3.4 ± 0.7	.134 ± .028
H	16.67	.656



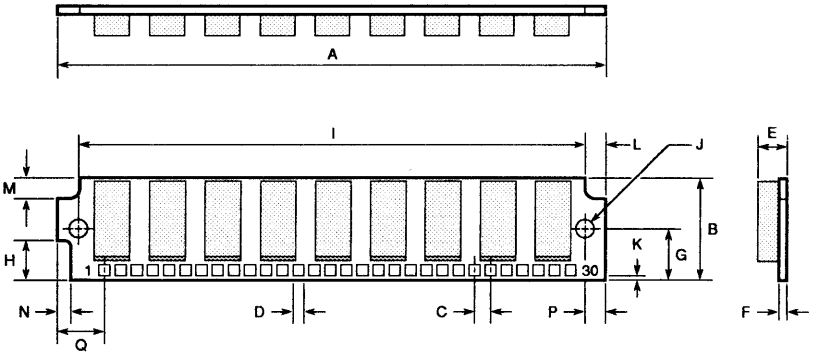
MC-421000A9AA/A9AB

83FM-8175B (10/91)

Package Drawings (cont)

30-Pin Socket-Mountable SIMM (MC-421000A9B/F)

Item	Millimeters	Inches
A	88.9 ±0.5	3.500 ± .020
B	20.0	.787
C	2.54 [TP]	.100 [TP]
D	1.77	.070
E	5.28 max	.208 max
F	1.27 ±0.15	.050 ± .006
G	10.16	.400
H	6.35	.250
I	82.14	3.234
J	3.18 dia	.125 dia
K	0.2	.008
L	3.56	.140
M	3.5	.138
N	2.03	.080
P	3.38	.133
Q	7.62	.300

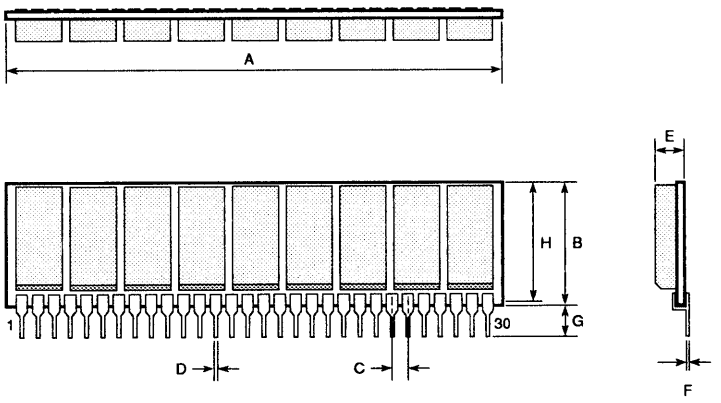


MC-421000A9B

83FM-8174B (10/91)

30-Pin Leaded SIMM (MC-421000A9A)

Item	Millimeters	Inches
A	80.3 ± 0.5	3.161 $^{+.021}_{-.020}$
B	21.6 max	.851 max
C	2.54 [TP]	.100 [TP]
D	0.50	.020
E	5.5 max	.217 max
F	0.25	.010
G	3.4 ± 0.7	.134 ± .028
H	20.0	.787



MC-421000A9A

83FM-8176B (10/91)

10b

MC-421000A32
1,048,576 x 32-Bit
Dynamic CMOS RAM Module

Description

The MC-421000A32 is a fast-page dynamic RAM module organized as 1,048,576 words by 32 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 - A_9 during a 16-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight, and cost of a system.. Each SIMM contains eight 1,048,576 x 4-bit DRAMs (μPD424400) and eight power supply decoupling capacitors for noise reduction. DQ_0 - DQ_{31} are common input/output pins.

Features

- 1,048,576-word by 32-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

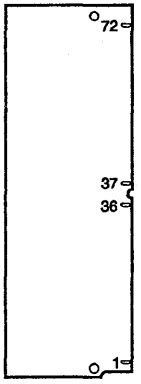
SIMM is a trademark of Wang Laboratories.

Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobes
DQ_0 - DQ_{31}	Common data inputs/outputs
$\overline{RAS}_0$, $\overline{RAS}_2$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{16}
4	DQ_1
5	DQ_{17}
6	DQ_2
7	DQ_{18}
8	DQ_3
9	DQ_{19}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	NC
20	DQ_4
21	DQ_{20}
22	DQ_5
23	DQ_{21}
24	DQ_6
25	DQ_{22}
26	DQ_7
27	DQ_{23}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	A_9
33	NC
34	$\overline{RAS}_2$
35	NC
36	NC

Pin	Symbol
37	NC
38	NC
39	GND
40	$\overline{CAS}_0$
41	$\overline{CAS}_2$
42	$\overline{CAS}_3$
43	$\overline{CAS}_1$
44	$\overline{RAS}_0$
45	NC
46	NC
47	$\overline{WE}$
48	NC
49	DQ_8
50	DQ_{24}
51	DQ_9
52	DQ_{25}
53	DQ_{10}
54	DQ_{26}

Pin	Symbol
55	DQ_{11}
56	DQ_{27}
57	DQ_{12}
58	DQ_{28}
59	V_{CC}
60	DQ_{29}
61	DQ_{13}
62	DQ_{30}
63	DQ_{14}
64	DQ_{31}
65	DQ_{15}
66	NC
67	GND
68	GND
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

[1] Pins 69 and 70 are defined by access time:

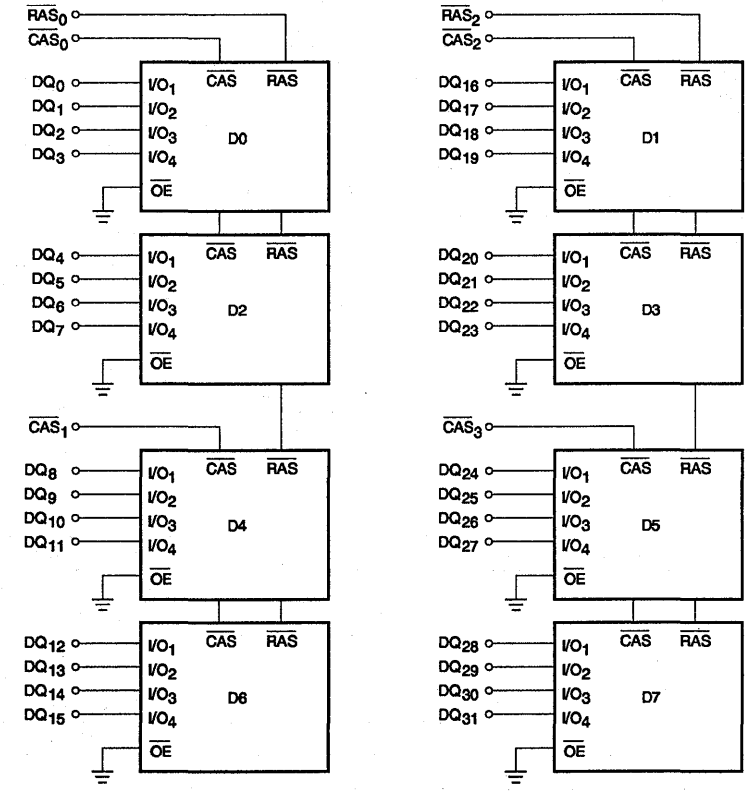
Pin	60 ns	70 ns	80 ns	100 ns
69	NC	GND	NC	GND
70	NC	NC	GND	GND

83YL-8626A

Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-421000A32B-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.000 inch)	5.28 mm (0.208 inch)	Eight μPD424400LA
B-70	70 ns				
B-80	80 ns				
MC-421000A32F-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				
MC-421000A32BT-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.000 inch)	4.1 mm (0.161 inch)	Eight μPD424400GS
BT-70	70 ns				
BT-80	80 ns				
MC-421000A32FT-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FT-70	70 ns				
FT-80	80 ns				

MC-421000A32 Connection Diagram



10c

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	68	pF	A_0 - A_9
	C_{I2}	76	pF	$\overline{WE}$
	C_{I3}	43	pF	$\overline{RAS}$
	C_{I4}	29	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{O1}	17	pF	DQ_0 - DQ_{31}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		16	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			8	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−80	80	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	DQ_0 to DQ_{31} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		960		800		720	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		960		800		720	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		720		640		560	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		960		800		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		17		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		ns	(Note 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		15		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	ns	(Note 10)
Fast-page cycle time	t_{PC}	40		45		50		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Random read or write cycle time	t_{RC}	120		140		160		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

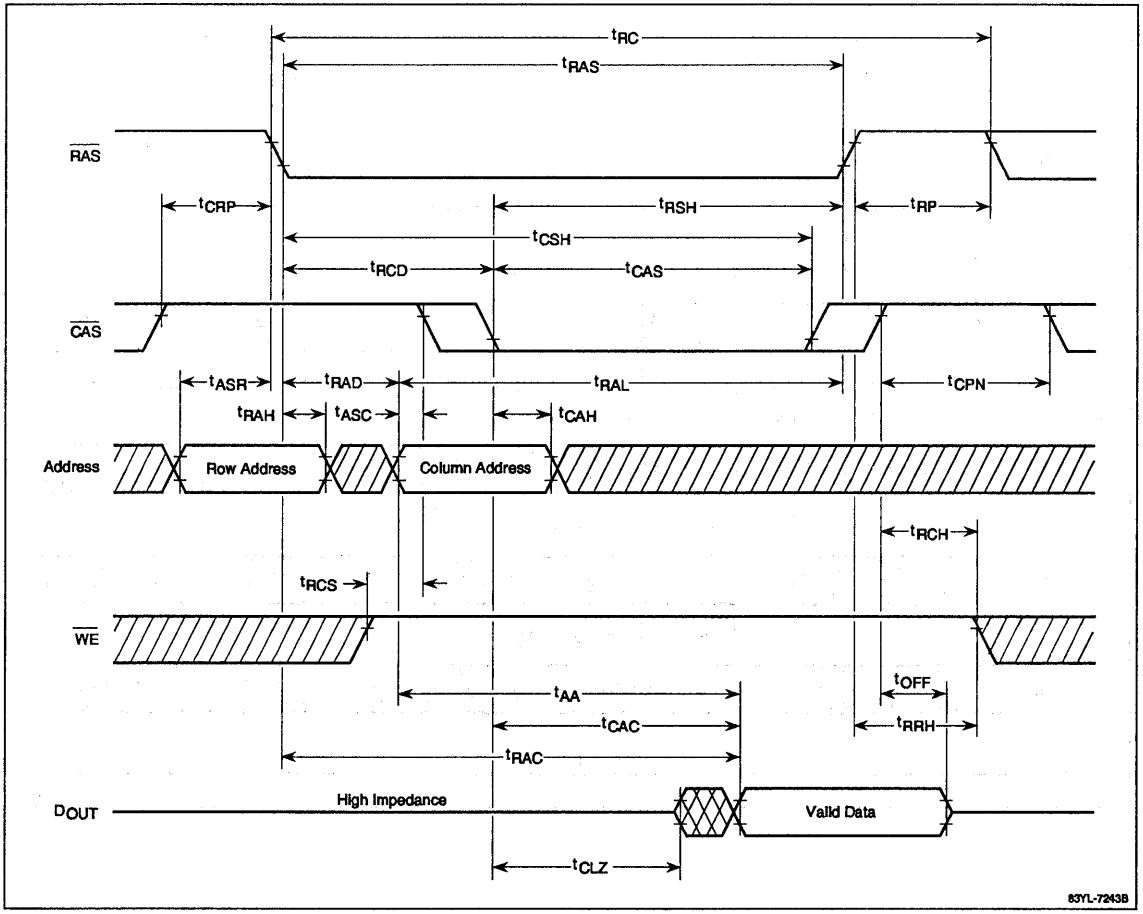
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

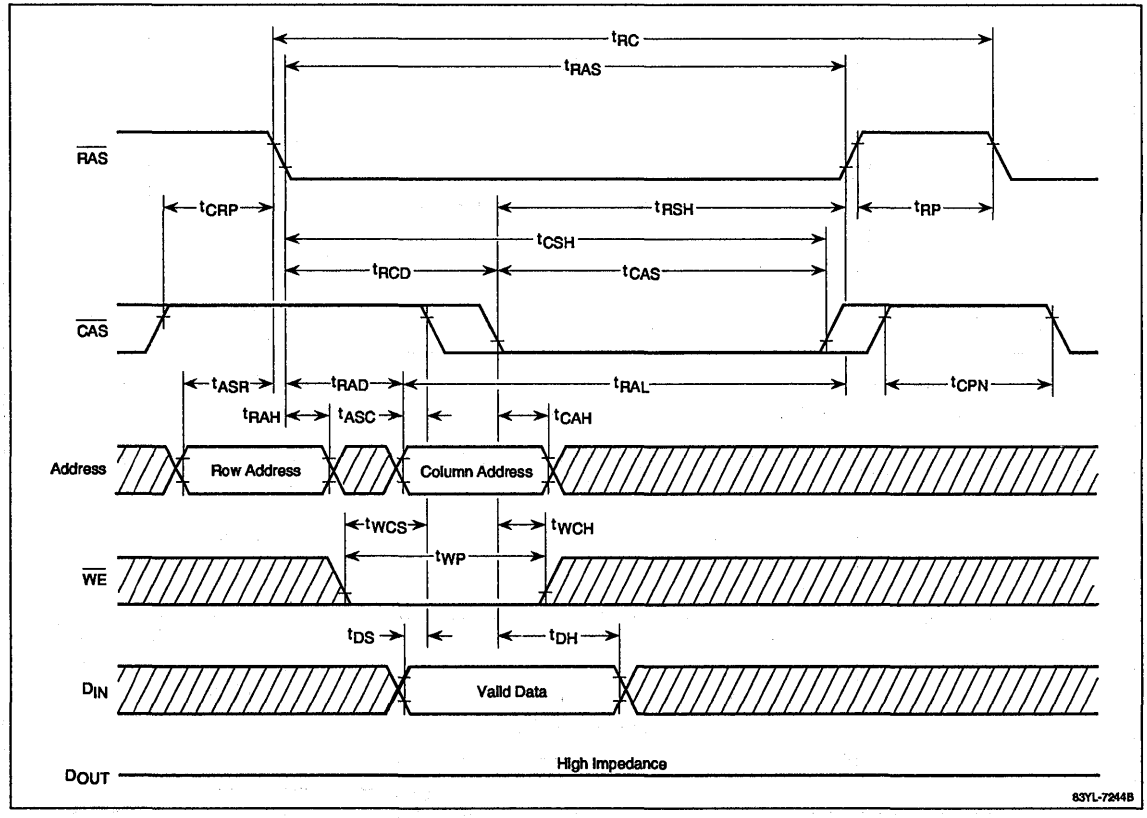
Timing Waveforms

Read Cycle



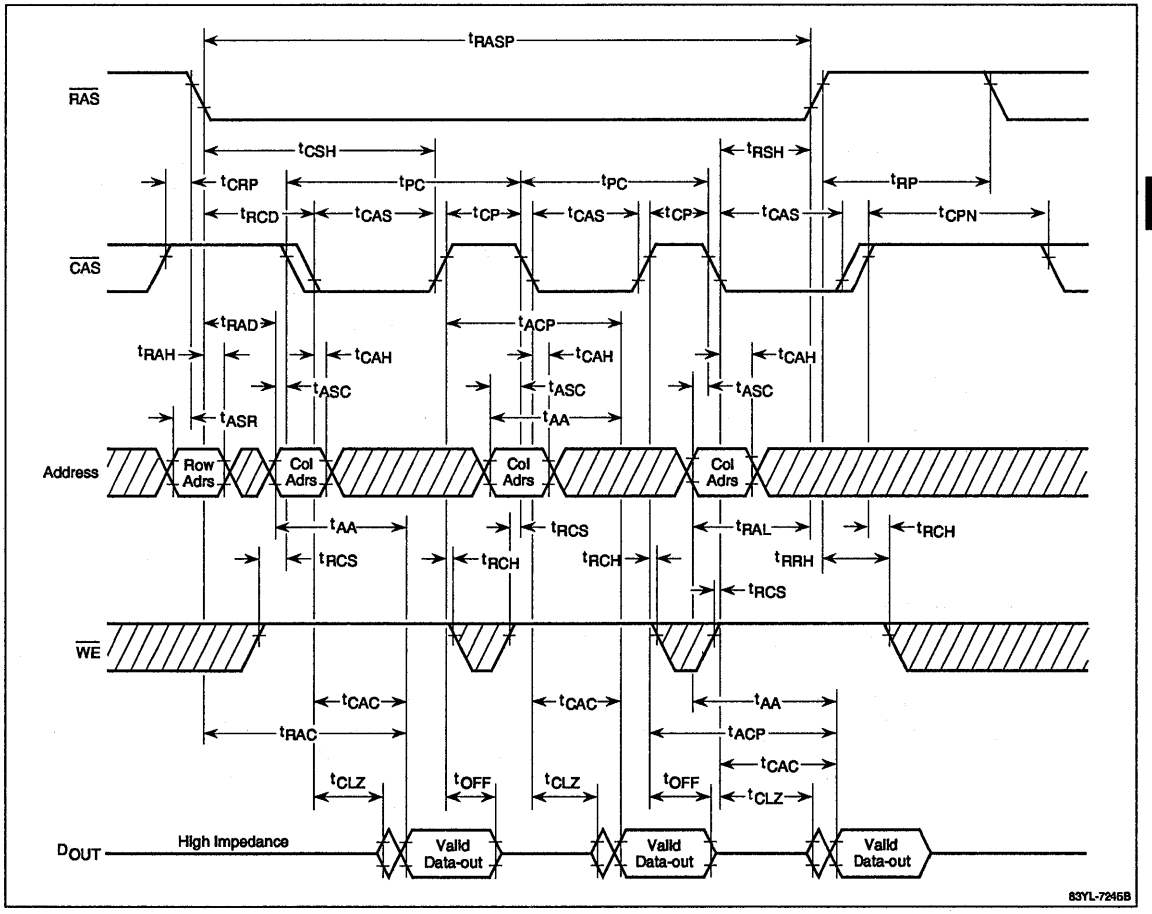
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Fast-Page Read Cycle



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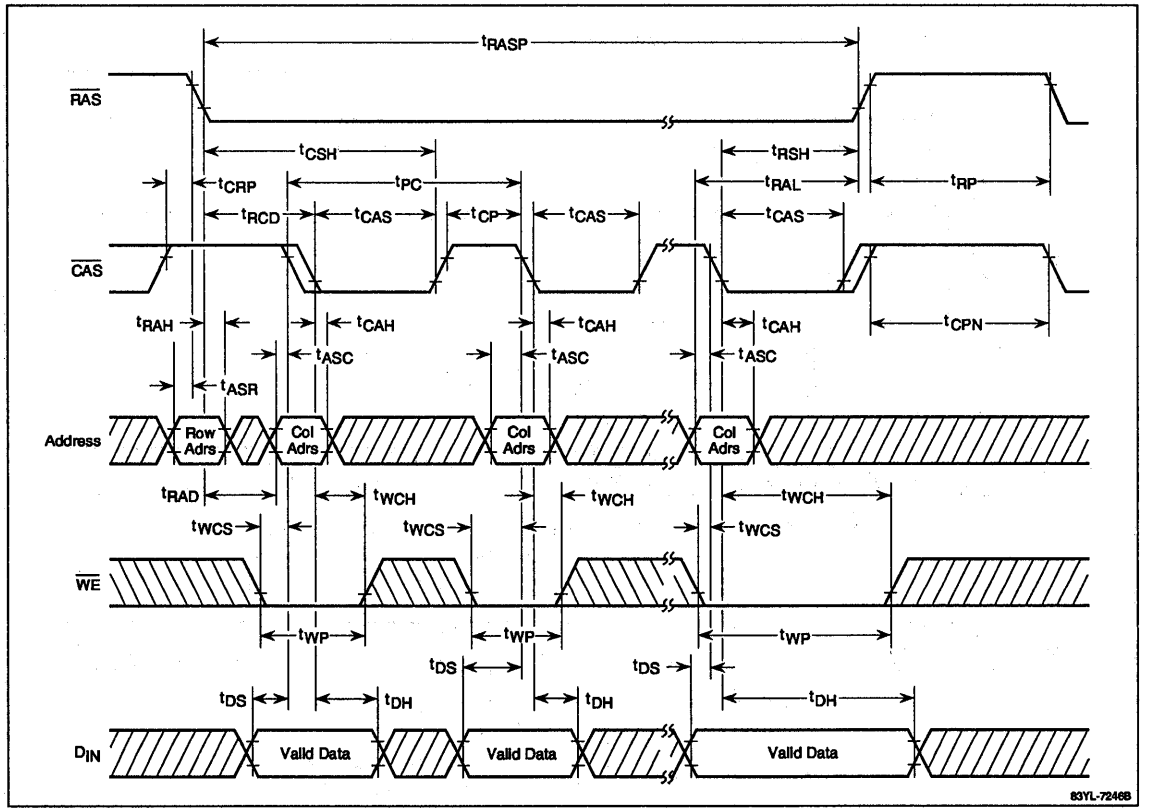
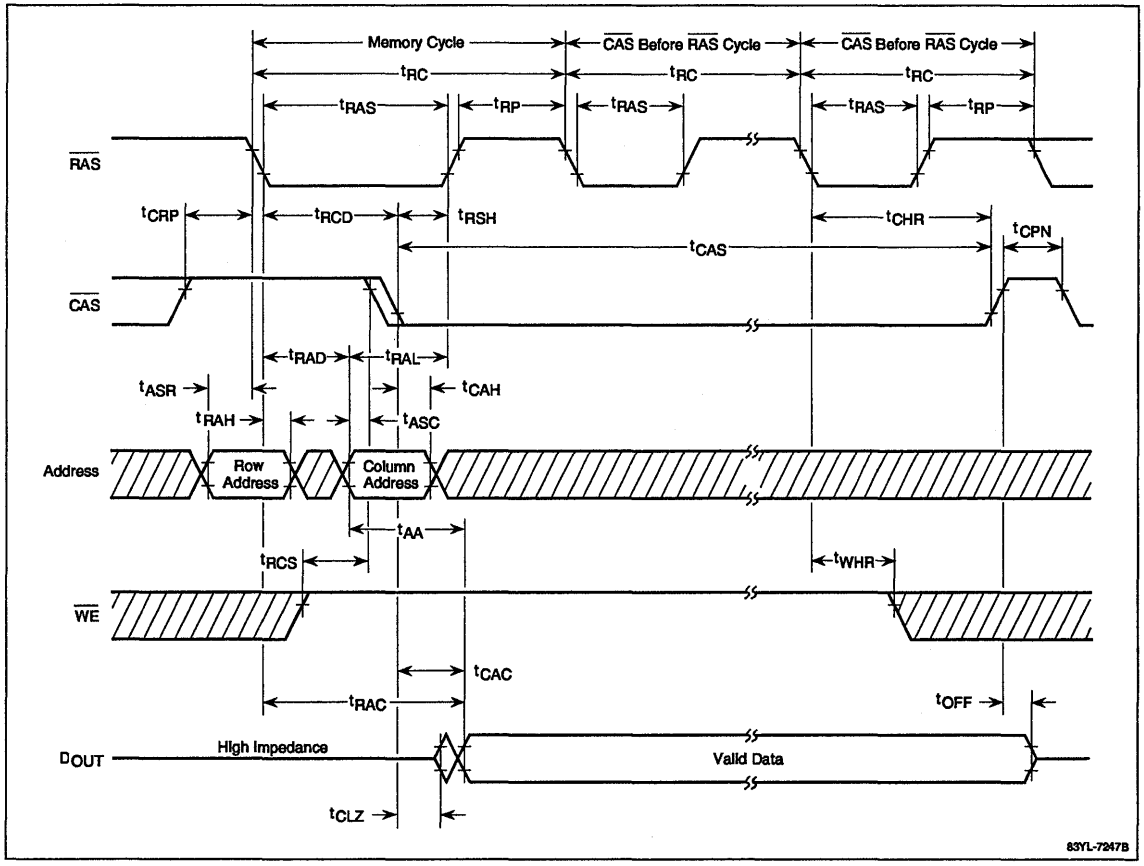
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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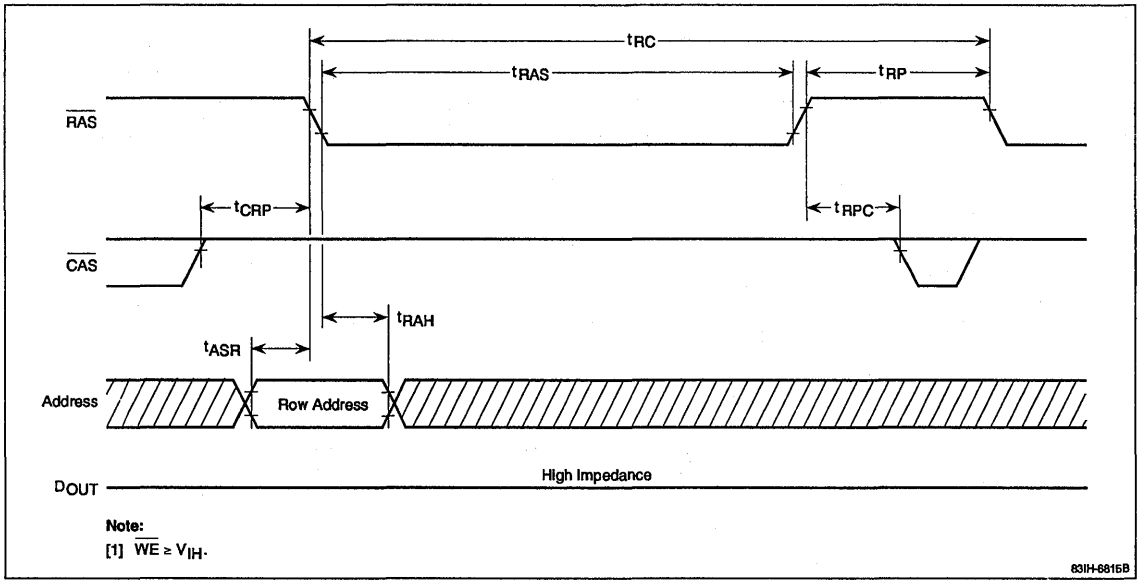
Timing Waveforms (cont)

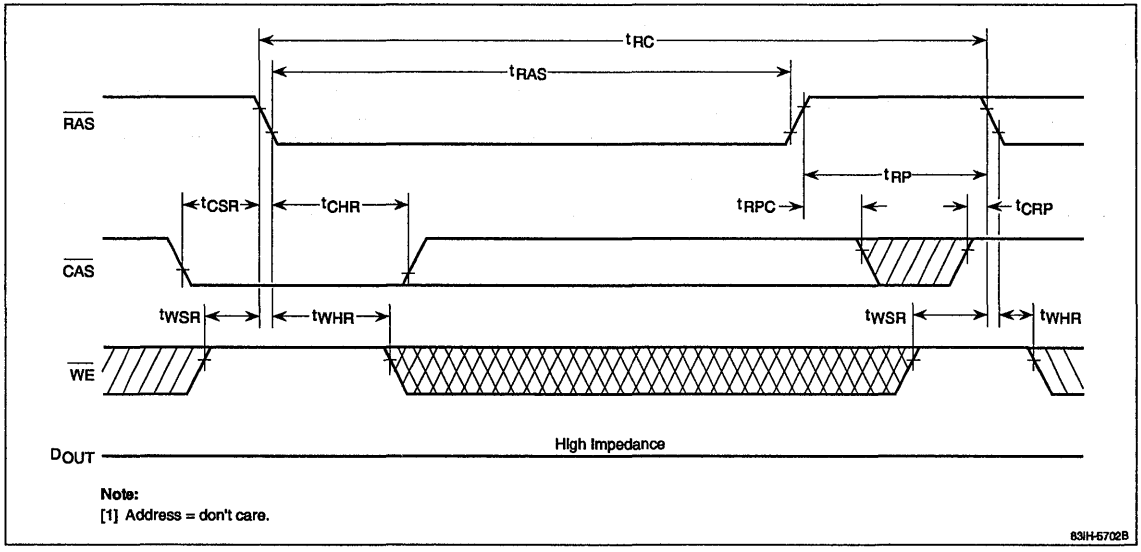
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

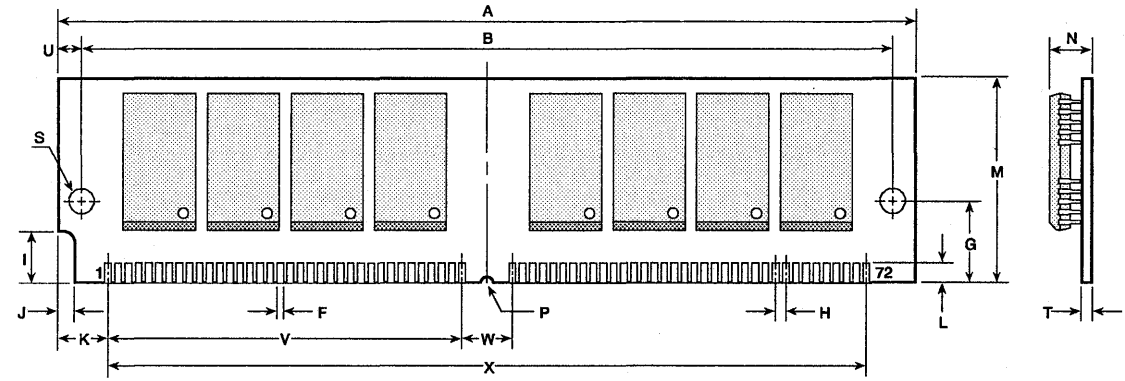
83IH-5702B

Package Drawings

72-Pin Socket-Mountable SIMM (MC-421000A32: Suffix B, F)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04 min	.041 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	25.4	1.000
N	5.28	.208
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004

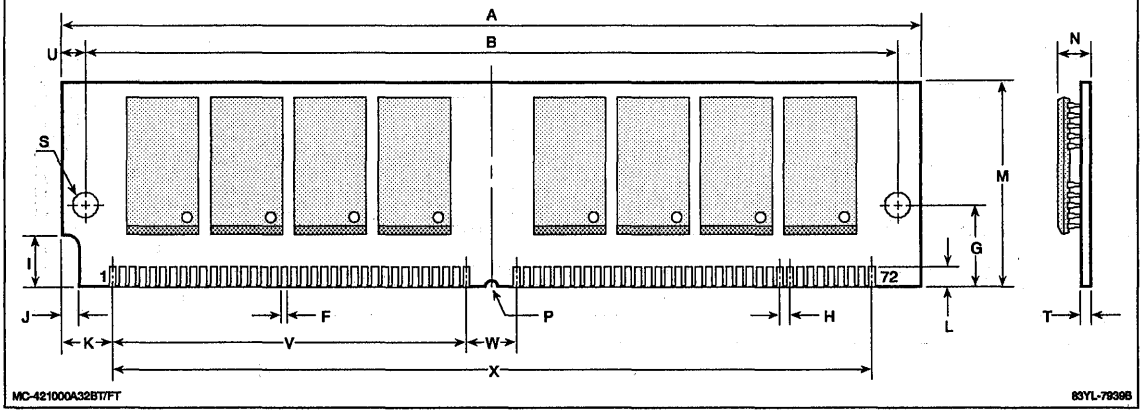


Package Drawing (cont)

72-Pin Socket-Mountable SIMM (MC-421000A32: Suffix BT, FT)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04 min	.041 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	25.4	1.000
N	4.1	.161
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-421000A36
1,048,576 x 36-Bit
Dynamic CMOS RAM Module

Description

The MC-421000A36 is a fast-page dynamic RAM module organized as 1,048,576 words by 36 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 - A_9 during a 16-ms period.

The MC-421000A36 is packaged in a variety of 72-pin Single Inline Memory Modules (SIMM™). Each SIMM contains eight 1,048,576 x 4-bit DRAMs (μPD424400), four 1,048,576 x 1-bit DRAMs (μPD421000), and 12 power supply decoupling capacitors for noise reduction.

Features

- 1,048,576-word by 36-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

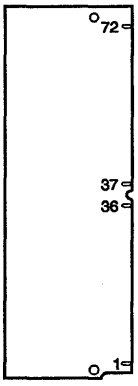
SIMM is a trademark of Wang Laboratories.

Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS_0}$ - $\overline{CAS_3}$	Column address strobes
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS_0}$, $\overline{RAS_2}$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configuration

72-Pin SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{18}
4	DQ_1
5	DQ_{19}
6	DQ_2
7	DQ_{20}
8	DQ_3
9	DQ_{21}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	NC
20	DQ_4
21	DQ_{22}
22	DQ_5
23	DQ_{23}
24	DQ_6
25	DQ_{24}
26	DQ_7
27	DQ_{25}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	A_9
33	NC
34	$\overline{RAS_2}$
35	DQ_{26}
36	DQ_8

Pin	Symbol
37	DQ_{17}
38	DQ_{35}
39	GND
40	$\overline{CAS_0}$
41	$\overline{CAS_2}$
42	$\overline{CAS_3}$
43	$\overline{CAS_1}$
44	$\overline{RAS_0}$
45	NC
46	NC
47	$\overline{WE}$
48	NC
49	DQ_9
50	DQ_{27}
51	DQ_{10}
52	DQ_{28}
53	DQ_{11}
54	DQ_{29}

Pin	Symbol
55	DQ_{12}
56	DQ_{30}
57	DQ_{13}
58	DQ_{31}
59	V_{CC}
60	DQ_{32}
61	DQ_{14}
62	DQ_{33}
63	DQ_{15}
64	DQ_{34}
65	DQ_{16}
66	NC
67	[Note 1]
68	[Note 1]
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

[1] Pins 67-70 are defined by access time:

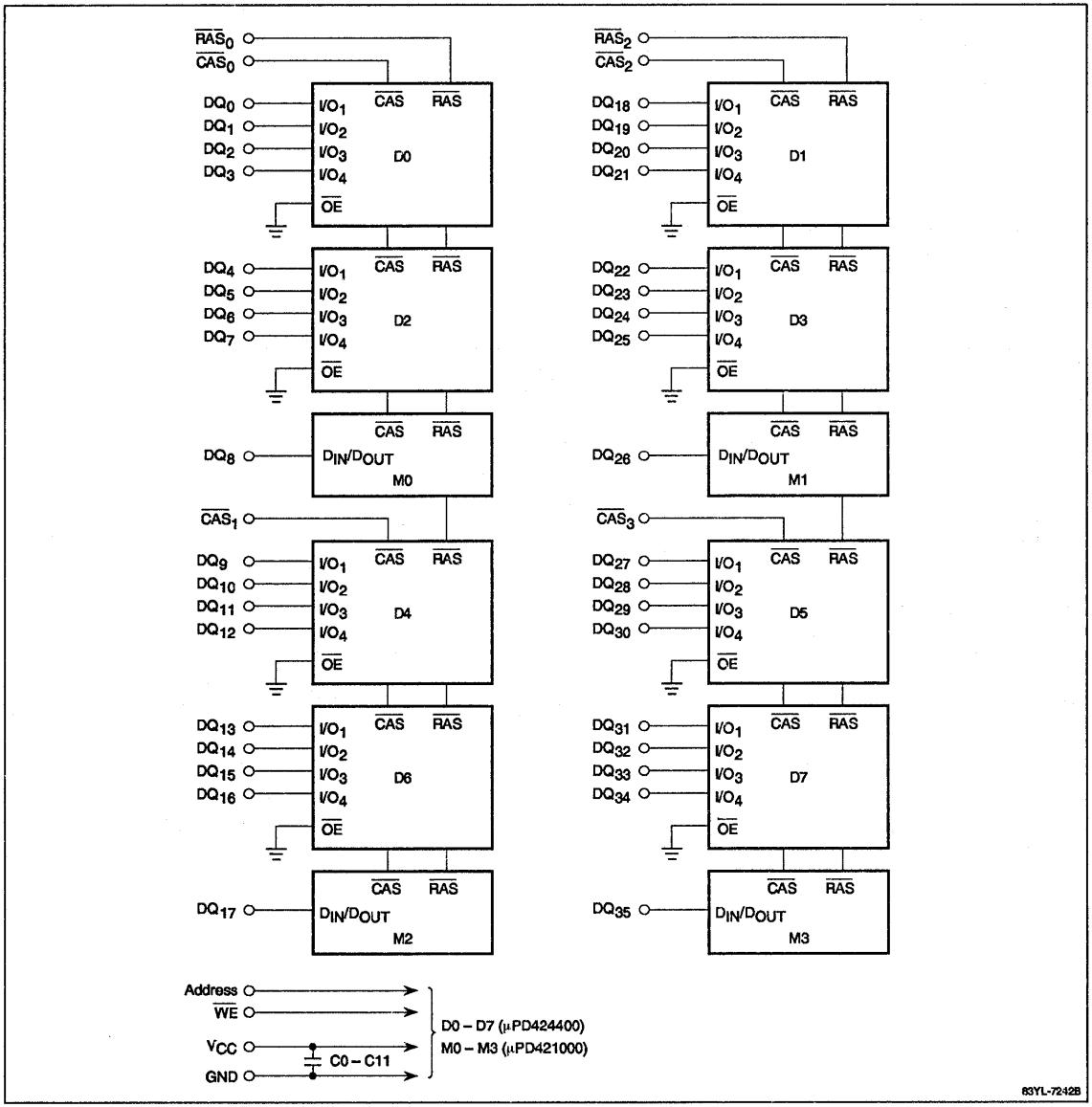
Pin	60 ns	70 ns	80 ns	100 ns
67	GND	GND	GND	GND
68	GND	GND	GND	GND
69	NC	GND	NC	GND
70	NC	NC	GND	GND

83FM-8163A

Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-421000A36B-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	5.28 mm (0.208 inch)	Eight μPD424400LA Four μPD421000GX
B-70	70 ns				
B-80	80 ns				
MC-421000A36F-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				
MC-421000A36BD-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	9.3 mm (0.366 inch)	Eight μPD424400LB Four μPD421000LA
BD-70	70 ns				
BD-80	80 ns				
MC-421000A36FD-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FD-70	70 ns				
FD-80	80 ns				
MC-421000A36BE-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	9.3 mm (0.366 inch)	Eight μPD424400LA Four μPD421000LA
BE-70	70 ns				
BE-80	80 ns				
MC-421000A36FE-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FE-70	70 ns				
FE-80	80 ns				
MC-421000A36BH-60	60 ns	72-pin socket-mountable SIMM (solder plating)	31.75 mm (1.250 inch)	5.28 mm (0.208 inch)	Eight μPD424400LB Four μPD421000LA
BH-70	70 ns				
BH-80	80 ns				
MC-421000A36FH-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FH-70	70 ns				
FH-80	80 ns				
MC-421000A36BJ-60	60 ns	72-pin socket-mountable SIMM (solder plating)	31.75 mm (1.250 inch)	5.28 mm (0.208 inch)	Eight μPD424400LA Four μPD421000LA
BJ-70	70 ns				
BJ-80	80 ns				
MC-421000A36FJ-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FJ-70	70 ns				
FJ-80	80 ns				
MC-421000A36BT-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	2.68 mm (0.106 inch)	Eight μPD424400GS Four μPD421000GX
BT-70	70 ns				
BT-80	80 ns				
MC-421000A36FT-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FT-70	70 ns				
FT-80	80 ns				

MC-421000A36 Connection Diagram



10d

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	12 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	88	pF	A_0 - A_9
	C_{I2}	104	pF	$\overline{WE}$
	C_{I3}	57	pF	$\overline{RAS}$
	C_{I4}	36	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{O1}	17	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	22	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			12	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−120	120	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		1320		1120		1000	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1320		1120		1000	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		1040		920		800	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1320		1120		1000	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		17		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		ns	(Note 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
Nonpage $\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		15		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	ns	(Note 10)
Fast-page cycle time	t_{PC}	40		45		50		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Random read or write cycle time	t_{RC}	120		140		160		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

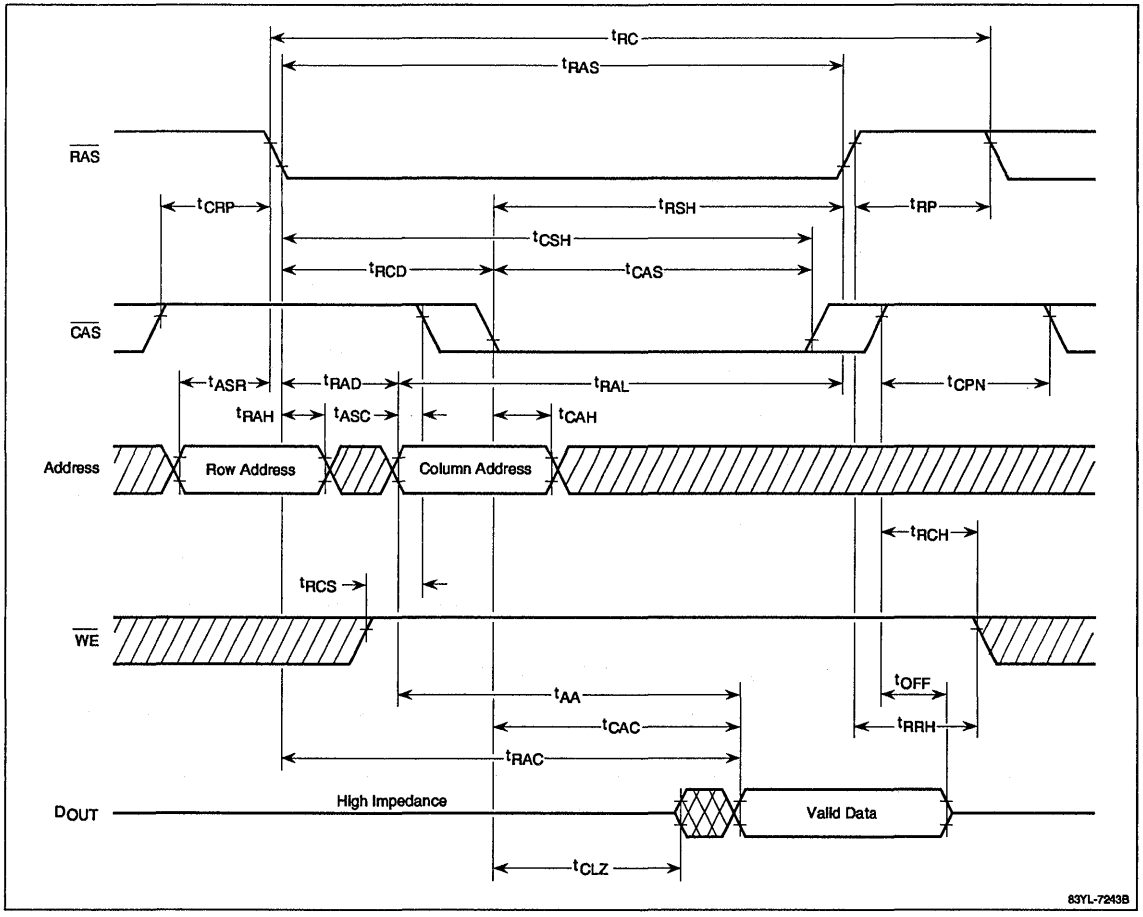
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Timing Waveforms

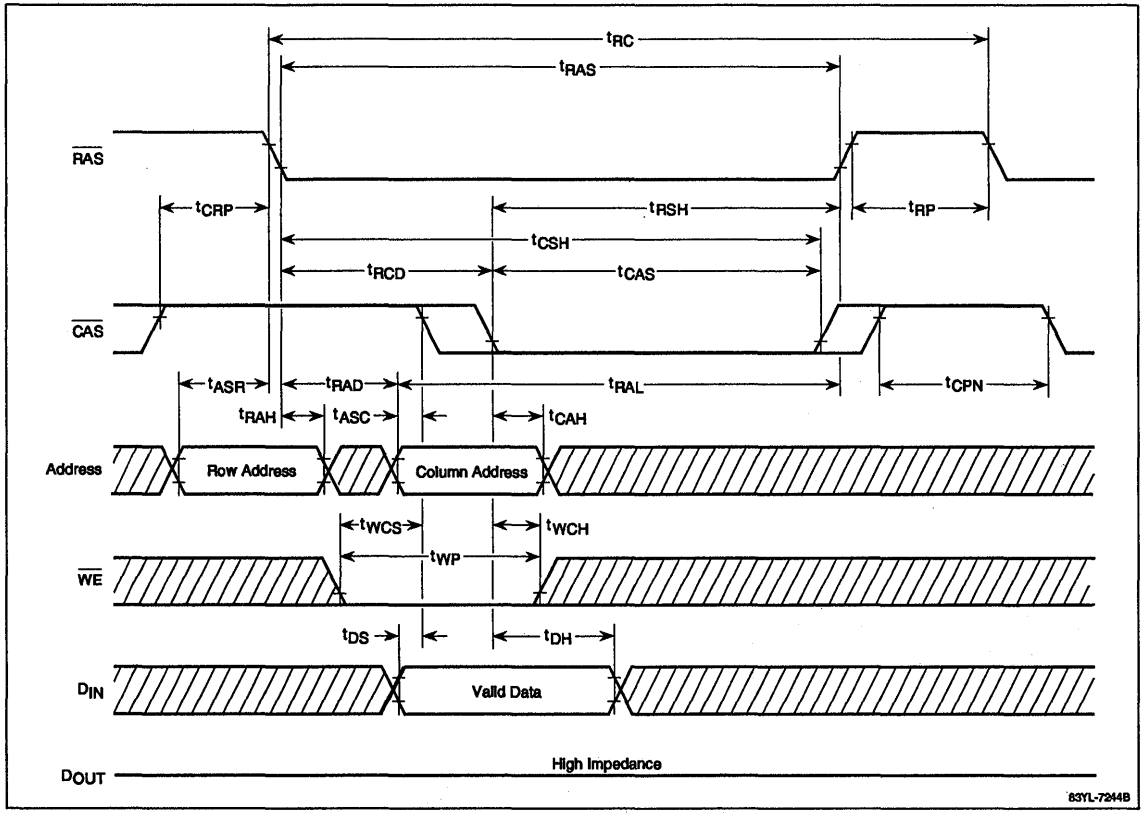
Read Cycle



10d

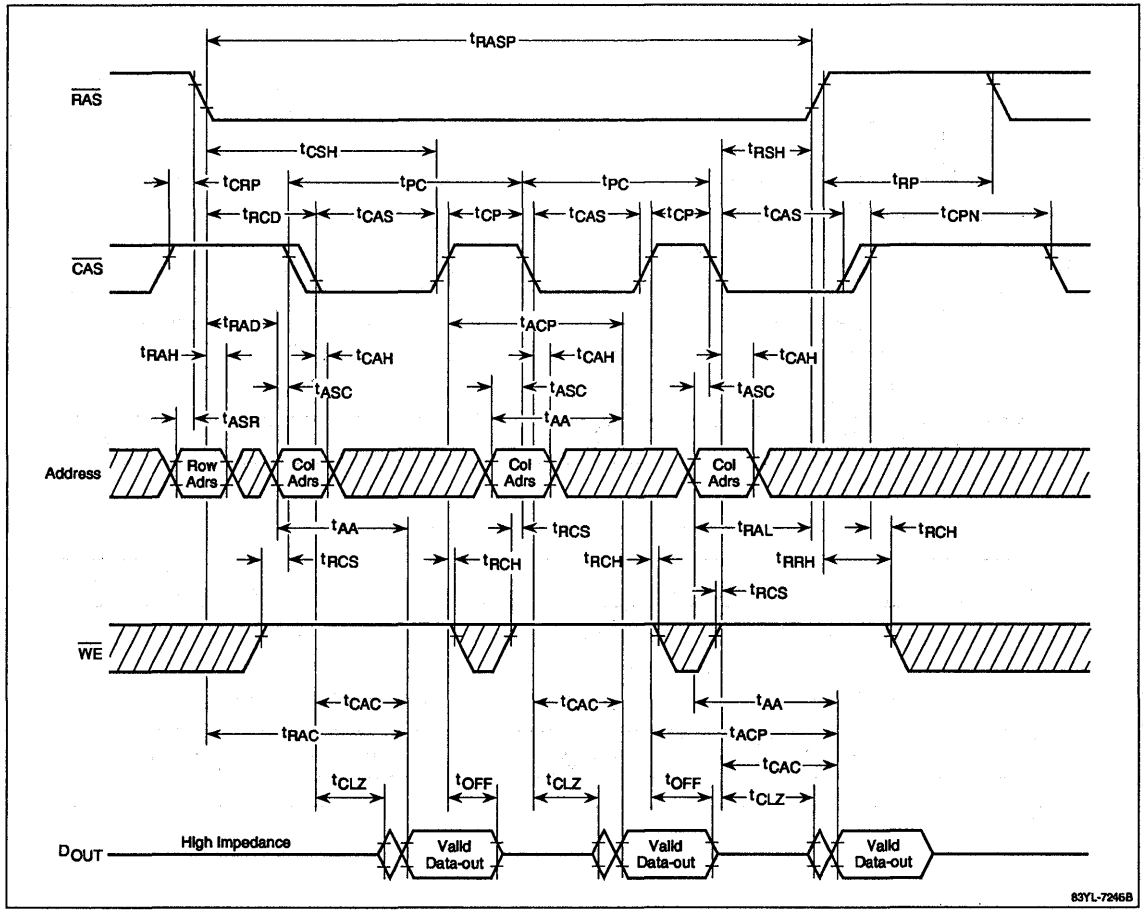
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

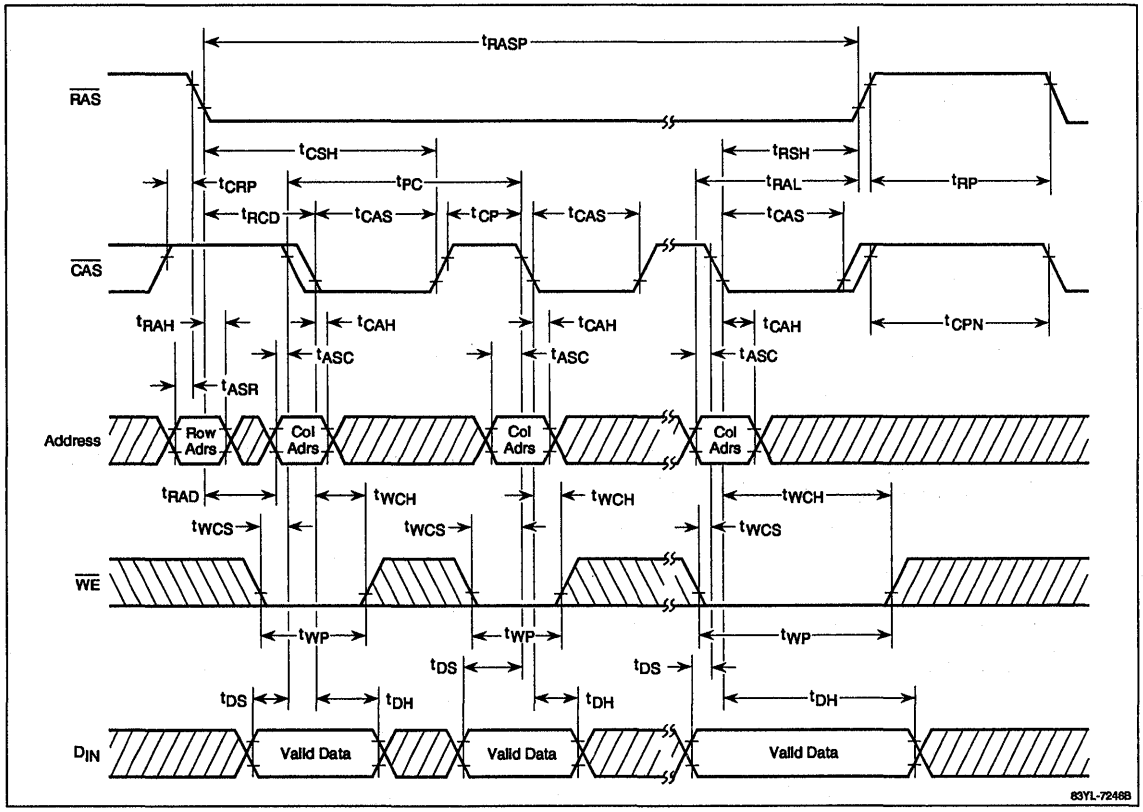
Fast-Page Read Cycle



10d

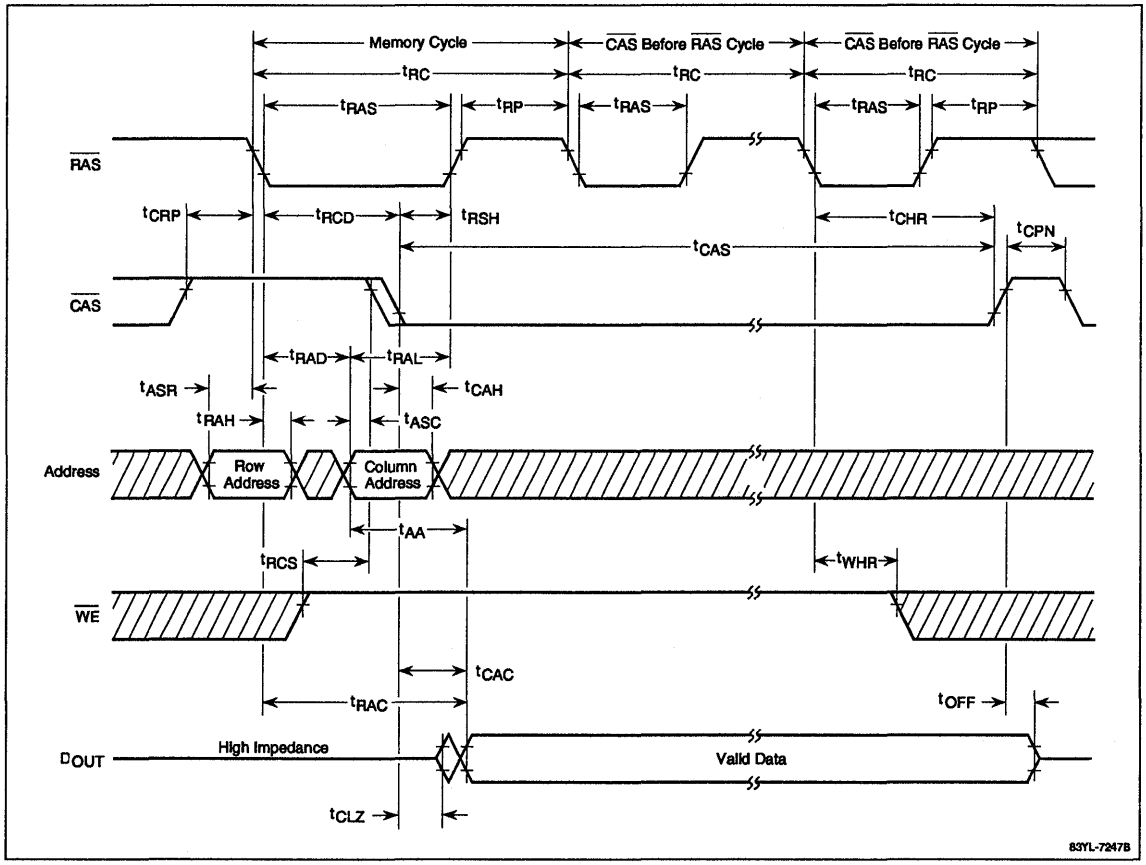
Timing Waveforms (cont)

Fast-Page Early Write Cycle



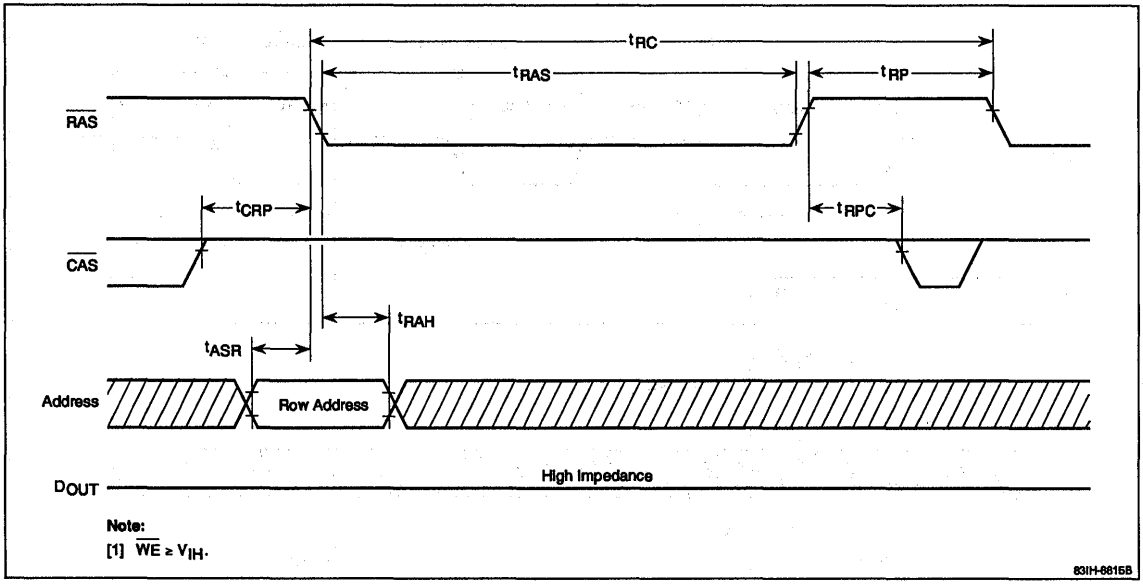
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

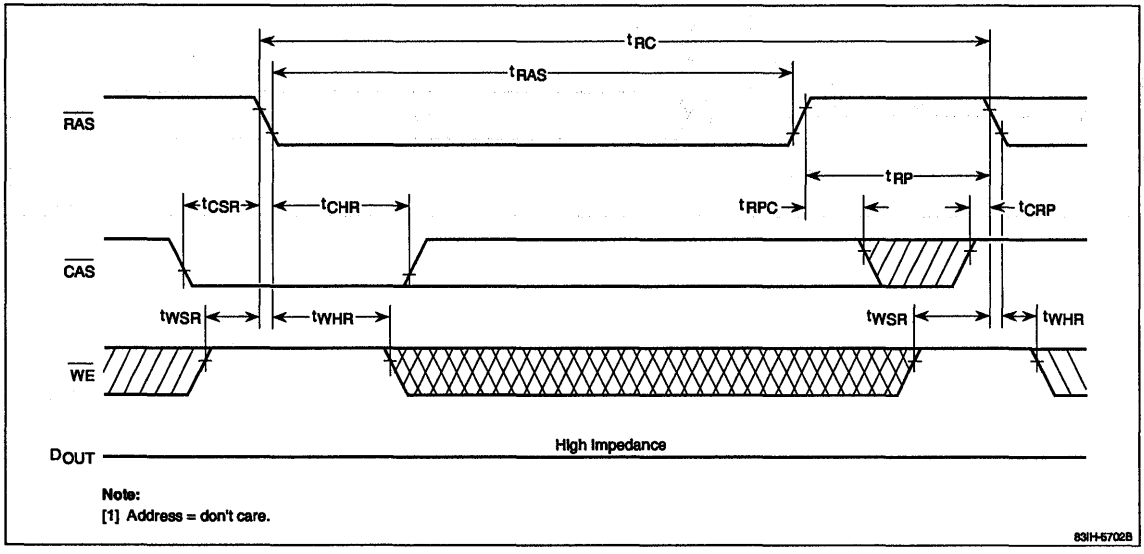
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

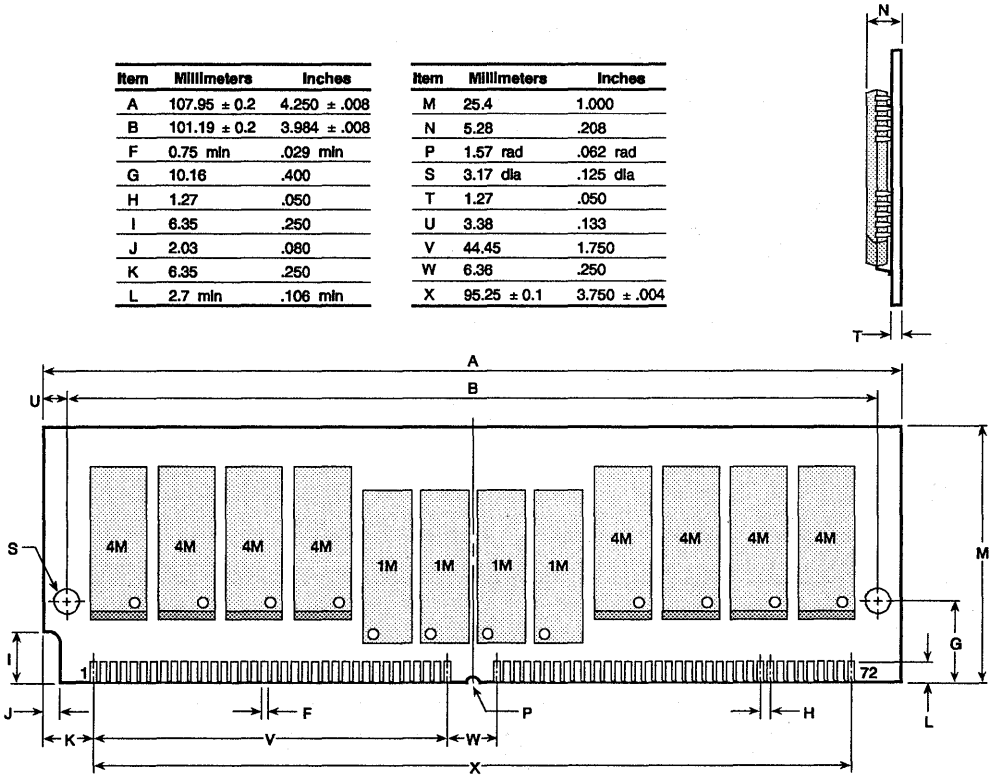
83IH-5702B

Package Drawings

72-Pin Socket-Mountable SIMM (MC-421000A36B/F)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	5.28	.208
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



1M = μPD421000GX 1M x 1 DRAM (TSOP)
4M = μPD424400LA 1M x 4 DRAM (300-mil SOJ)

MC-421000A36B/F

83NR-8166B (8/92)

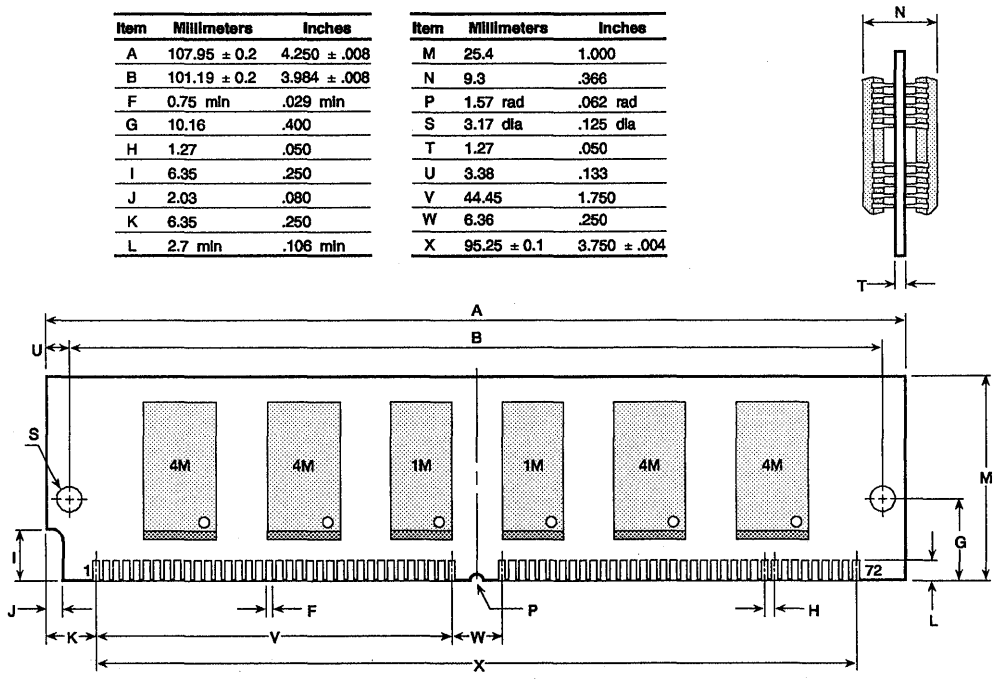
10d

Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-421000A36BD/FD, BE/FE)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	9.3	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-421000A36	4M	1M
BD	μPD424400LB, 1M x 4 DRAM (350-mil SOJ)	μPD421000LA, 1M x 1 DRAM (300-mil SOJ)
FD		
BE	μPD424400LA, 1M x 4 DRAM (300-mil SOJ)	
FE		

MC-421000A36BD/FD

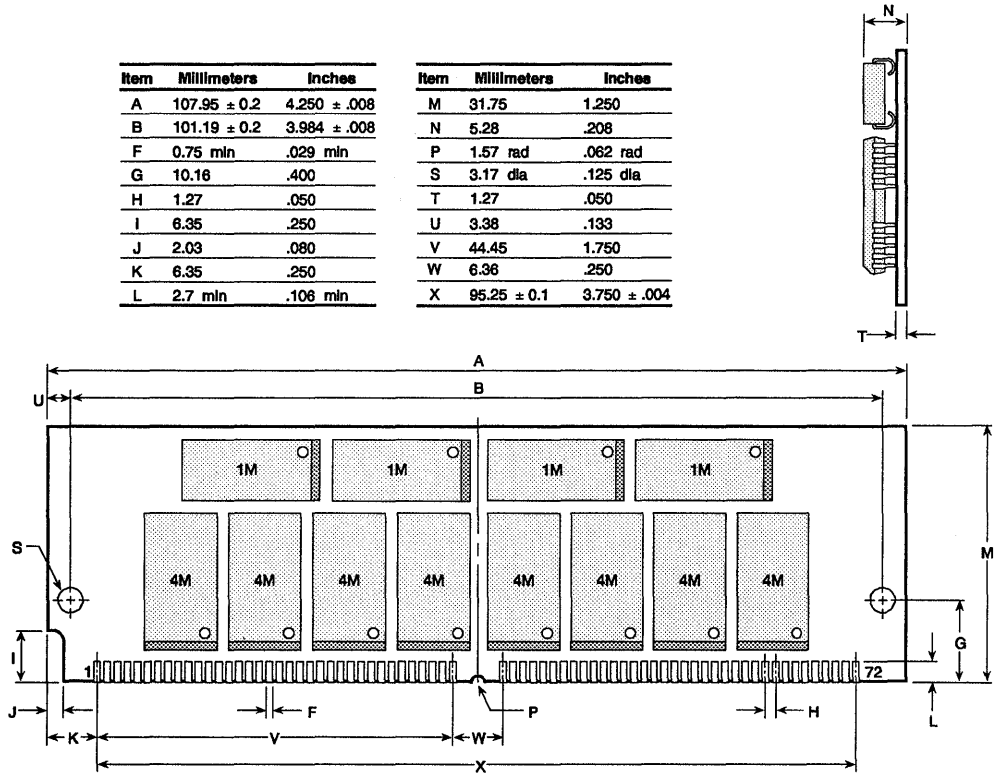
83NR-8177B (9/92)

Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-421000A36BH/FH)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	31.75	1.250
N	5.28	.208
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



1M = μPD421000LA 1M x 1 DRAM (300-mil SOJ)
4M = μPD424400LB 1M x 4 DRAM (350-mil SOJ)

MC-421000A36BH/FH

49NR-713B (10/91)

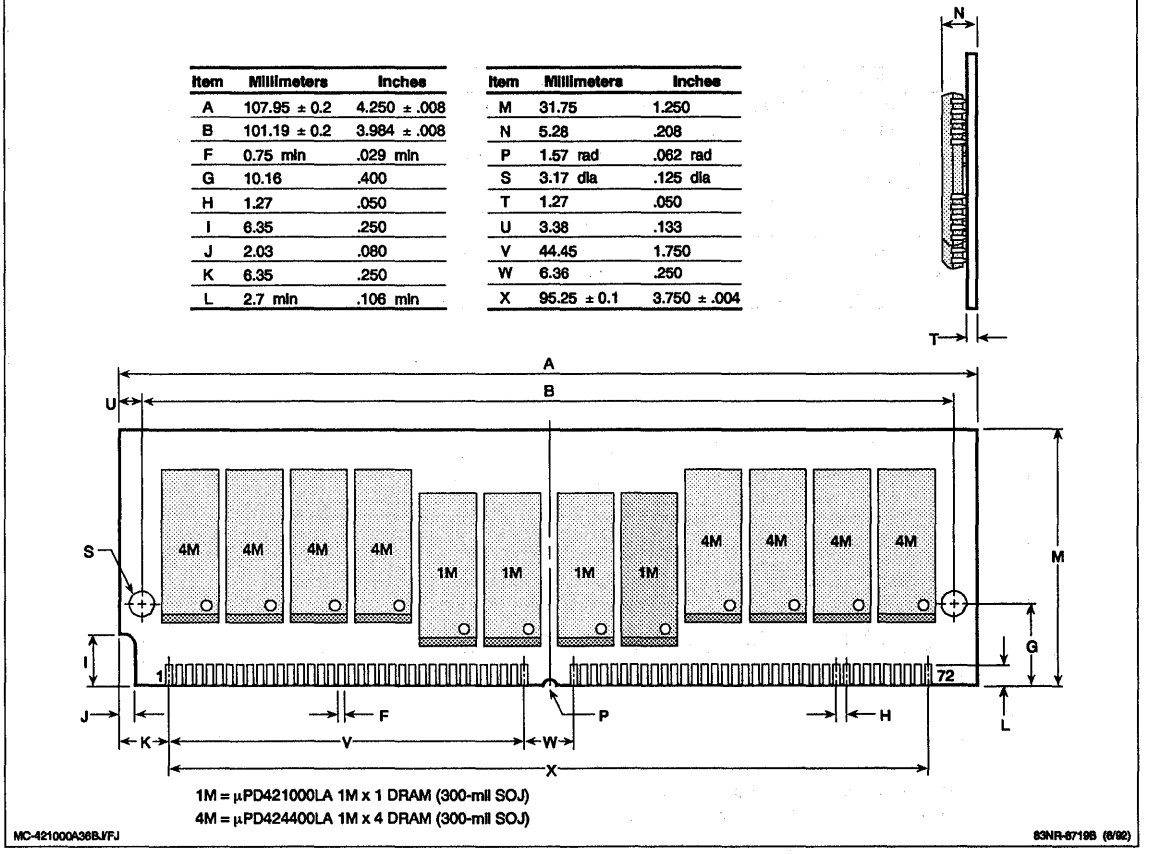
10d

Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-421000A36BJ/FJ)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	31.75	1.250
N	5.28	.208
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



1M = μPD421000LA 1M x 1 DRAM (300-mil SOJ)
4M = μPD424400LA 1M x 4 DRAM (300-mil SOJ)

MC-421000A36BJ/FJ

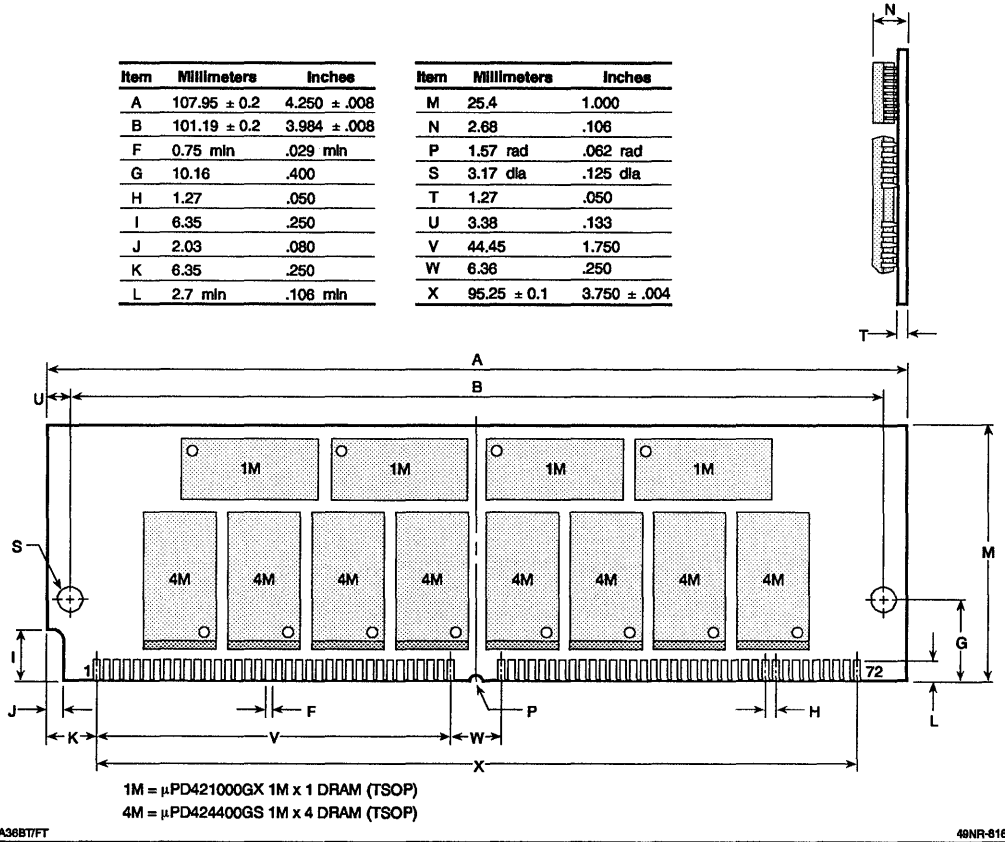
83NR-6719B (6/92)

Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-421000A36BT/FT)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	2.68	.106
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



1M = μPD421000GX 1M x 1 DRAM (TSOP)
4M = μPD424400GS 1M x 4 DRAM (TSOP)

MC-421000A36BT/FT

49NR-8166B (10/91)

10d

NEC Electronics Inc.

MC-421000AA40, -421000AB40
1,048,576 x 40-Bit
Dynamic CMOS RAM Module

10e

Description

The MC-421000AA40 and MC-421000AB40 are fast-page dynamic RAM modules organized as 1,048,576 words by 40 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 - A_9 during a 16-ms period.

The MC-421000AA40 is formed by ten 1M x 4 DRAMs (μPD424400). The MC-421000AB40 is formed by ten 512K x 8 DRAMs (μPD424800). Both modules have 10 power supply decoupling capacitors for noise reduction and are packaged in 72-pin Single Inline Memory Modules (SIMM™).

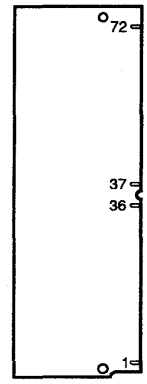
Features

- 1,048,576-word by 40-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{16}
4	DQ_1
5	DQ_{17}
6	DQ_2
7	DQ_{18}
8	DQ_3
9	DQ_{19}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	$\overline{OE}$
20	DQ_4
21	DQ_{20}
22	DQ_5
23	DQ_{21}
24	DQ_6
25	DQ_{22}
26	DQ_7
27	DQ_{23}
28	A_7
29	DQ_{36}
30	V_{CC}
31	A_8
32	A_9
33	NC
34	NC
35	DQ_{34}
36	DQ_{32}

Pin	Symbol
37	DQ_{33}
38	DQ_{35}
39	GND
40	$\overline{CAS}_0$
41	NC
42	NC
43	Note 1
44	$\overline{RAS}_0$
45	Note 1
46	DQ_{37}
47	$\overline{WE}$
48	GND
49	DQ_8
50	DQ_{24}
51	DQ_9
52	DQ_{25}
53	DQ_{10}
54	DQ_{26}

Pin	Symbol
55	DQ_{11}
56	DQ_{27}
57	DQ_{12}
58	DQ_{28}
59	V_{CC}
60	DQ_{29}
61	DQ_{13}
62	DQ_{30}
63	DQ_{14}
64	DQ_{31}
65	DQ_{15}
66	DQ_{38}
67	GND
68	GND
69	Note 2
70	Note 2
71	DQ_{39}
72	GND

Notes:

[1] Signal assignments to pins 43 and 45.

Pin	MC-421000AA40	MC-421000AB40
43	NC	$\overline{CAS}_1$
45	NC	$\overline{RAS}_1$

[2] Pins 69 and 70 are defined by access time.

Pin	60 ns	70 ns	80 ns	100 ns
69	NC	GND	NC	GND
70	NC	NC	GND	GND

83YL-8184A

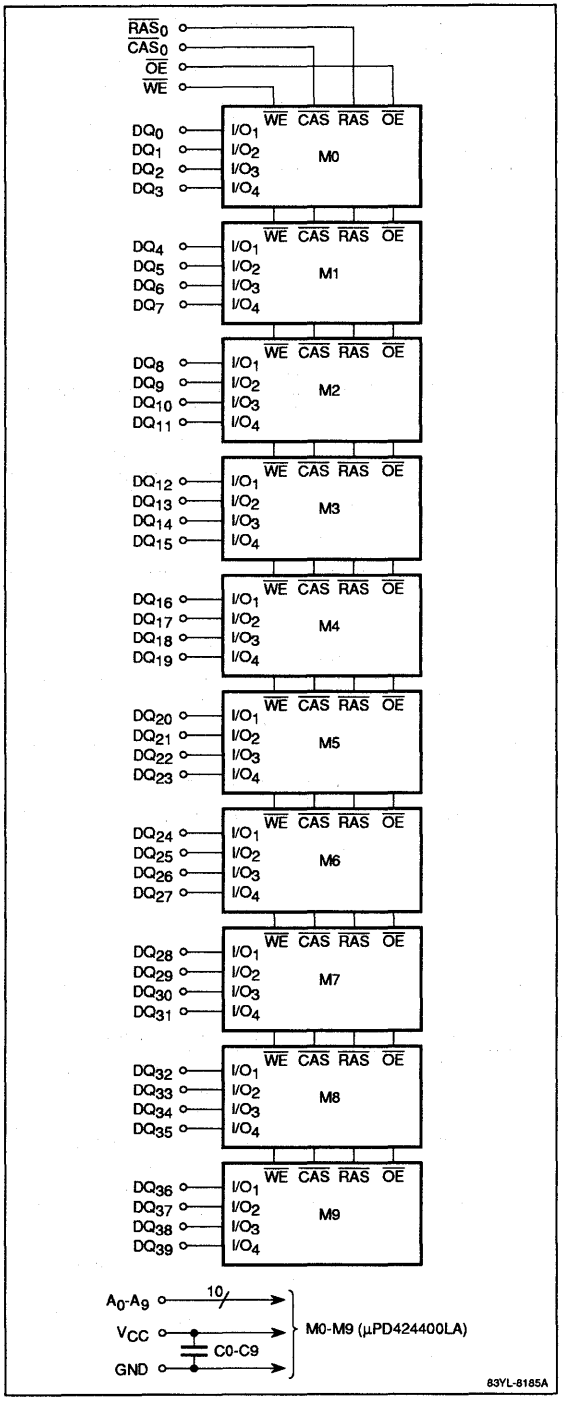
Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_1$	Column address strobes
DQ_0 - DQ_{39}	Common data inputs/outputs
$\overline{OE}$	Output enable
$\overline{RAS}_0$, $\overline{RAS}_1$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

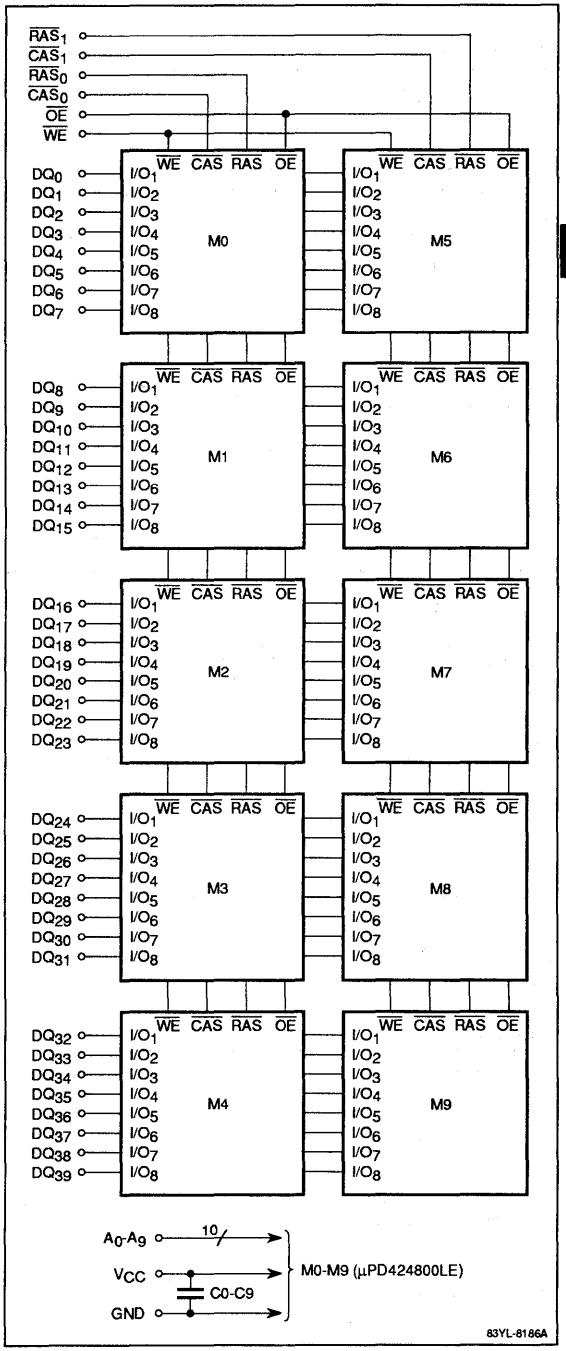
Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-421000AA40B-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	5.08 mm (0.2 inch)	Ten μPD424400LA
B-70	70 ns				
B-80	80 ns				
B-10	100 ns				
MC-421000AA40F-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				
F-10	100 ns				
MC-421000AB40B-60	60 ns	72-pin socket-mountable SIMM (solder plating)	20.0 mm (0.787 inch)	9.3 mm (0.366 inch)	Ten μPD424800LE
B-70	70 ns				
B-80	80 ns				
B-10	100 ns				
MC-421000AB40F-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				
F-10	100 ns				

MC-421000AA40 Connection Diagram



MC-421000AB40 Connection Diagram



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Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	10 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under Recommended Operating Conditions.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	MC-421000AA40 (max)	MC-421000AB40 (max)	Unit	Pins Under Test
Input capacitance	C_{I1}	65	60	pF	A_0 - A_9
	C_{I2}	70	85	pF	$\overline{WE}$, $\overline{OE}$
	C_{I3}	60	40	pF	$\overline{RAS}$
	C_{I4}	60	40	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{01}	12	20	pF	DQ_0 - DQ_{39}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		20	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			10	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−100	100	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	DQ_0 to DQ_{39} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		1250		1050		950		800	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1250		1050		950		800	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		900		800		700		600	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1250		1050		950		800	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		65		80		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		0		ns	(Notes 4, 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		55		ns	(Note 14)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ delay data time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 9)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		0		ns	(Notes 6, 7)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	70	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	165		185		210		250		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		130		ns	(Note 14)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 14)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		20		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 12)
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V and V_{OL} = 0.8 V).

(8) If $t_{RCD} \leq t_{RCS}$ (max) and $t_{RAD} \leq t_{RAD}$ (max) access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max) access time is defined by t_{CAC} (max) and if $t_{RAD} \geq t_{RAD}$ (max) access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

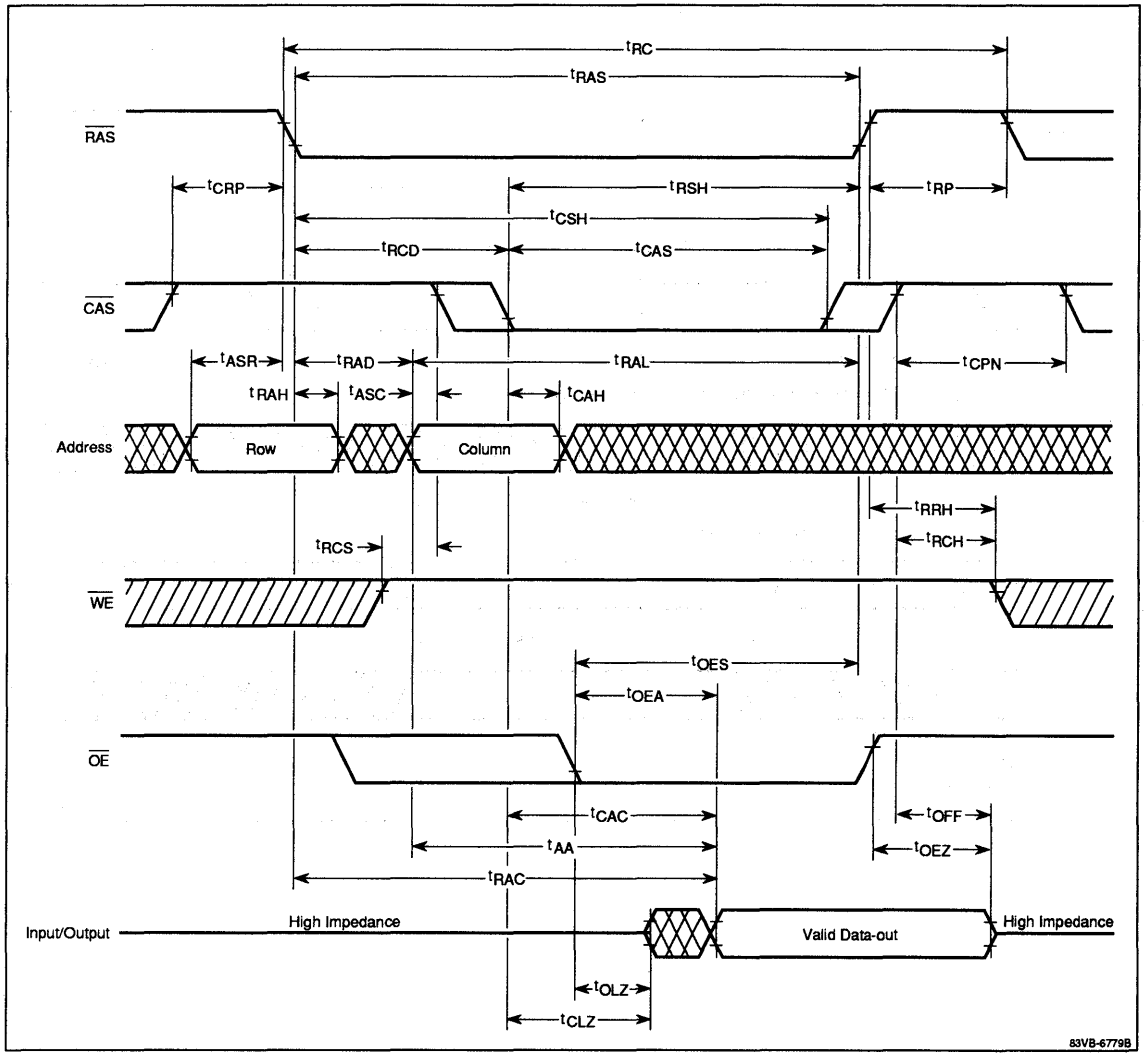
(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertantly be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Timing Waveforms

Read Cycle



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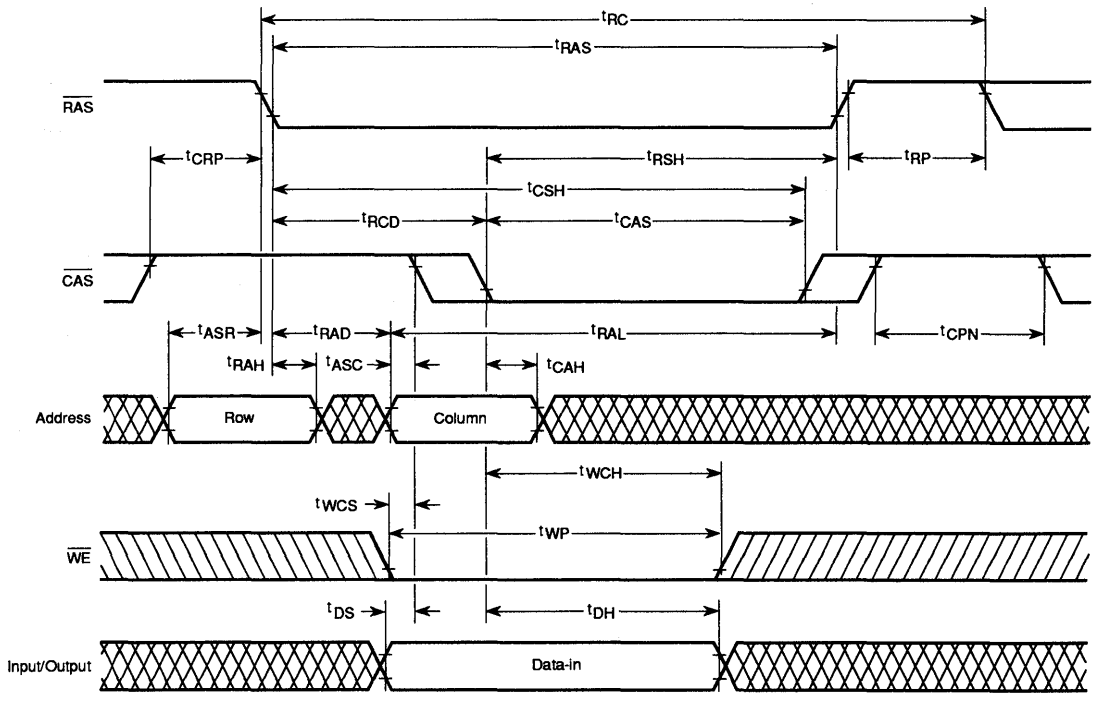
Timing Waveforms (cont)

Early Write Cycle

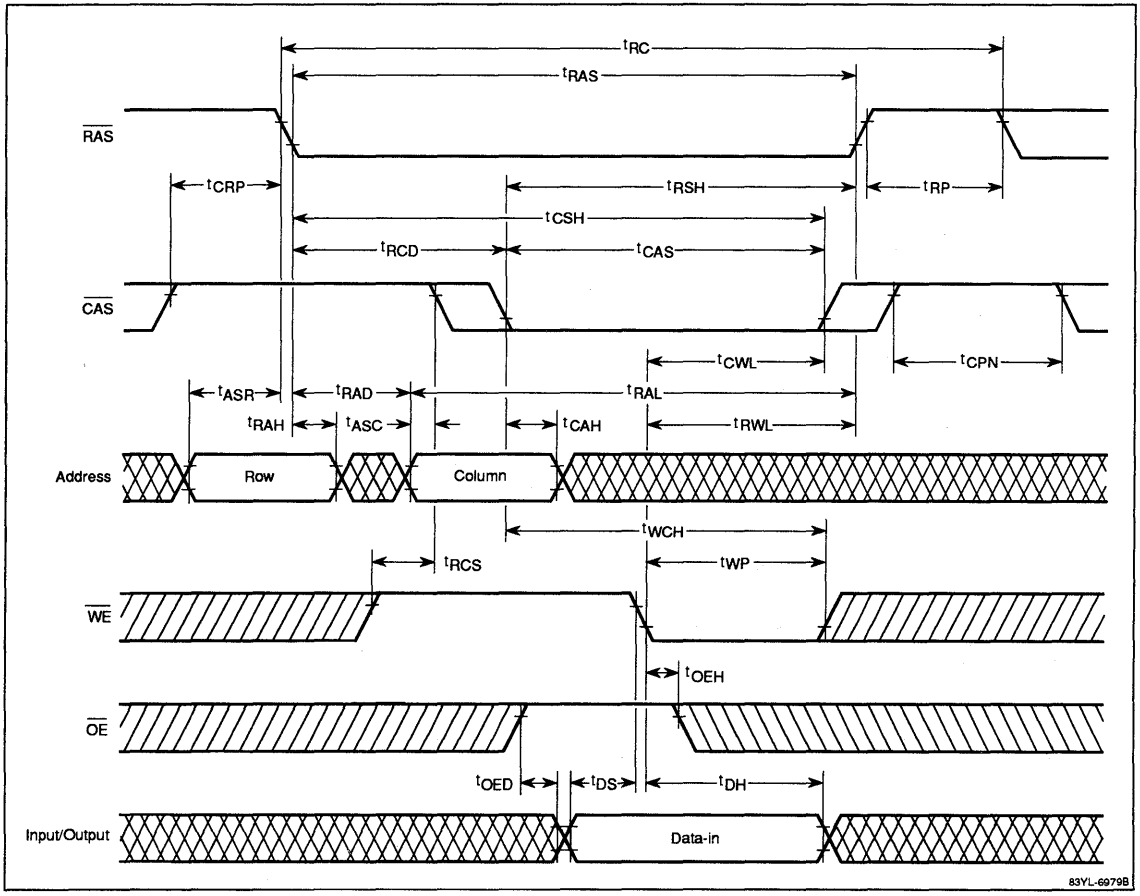


Note:
[1] $\overline{OE}$ = don't care.

83YL-6978B

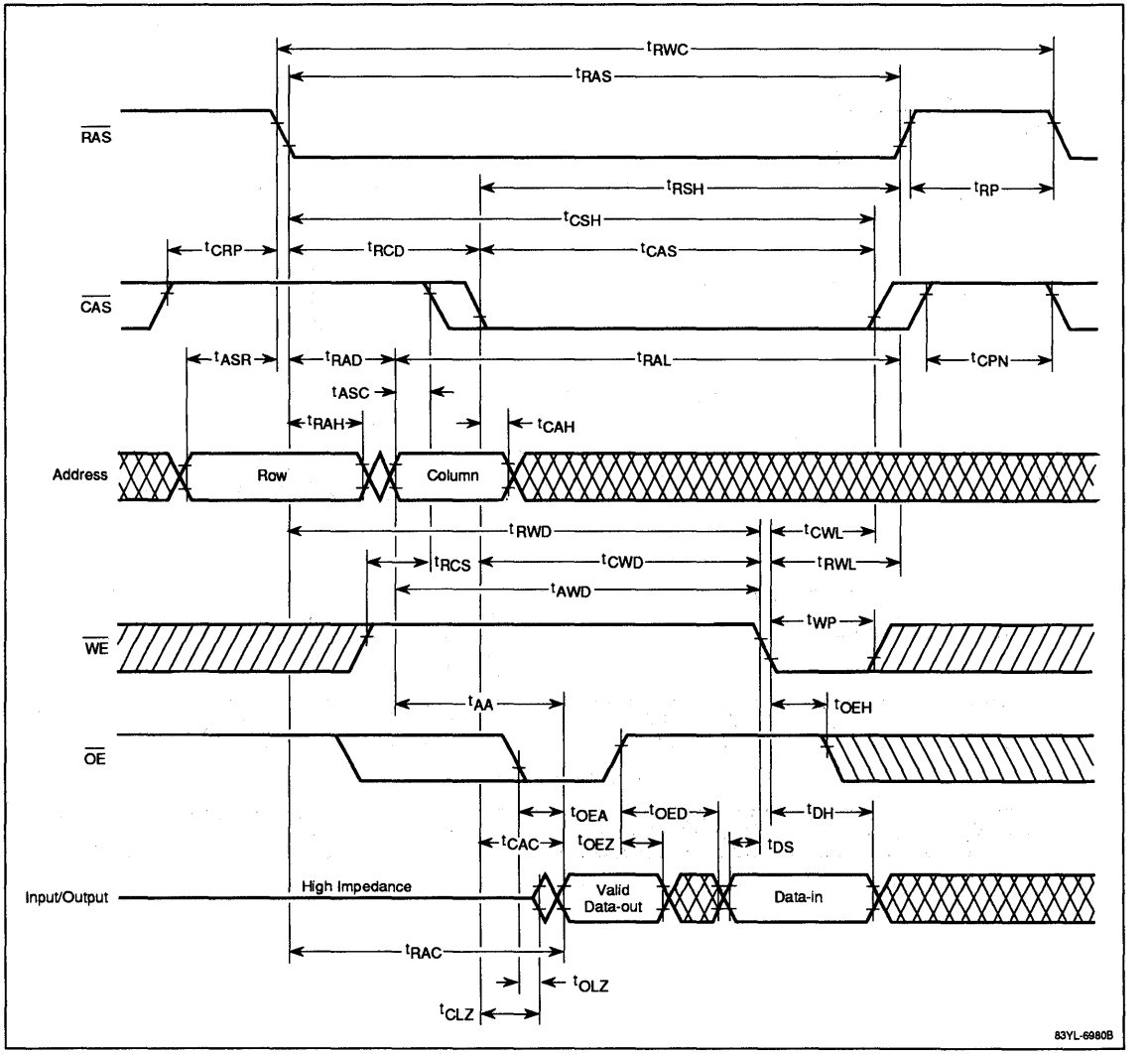
Timing Waveforms (cont)

Late Write Cycle



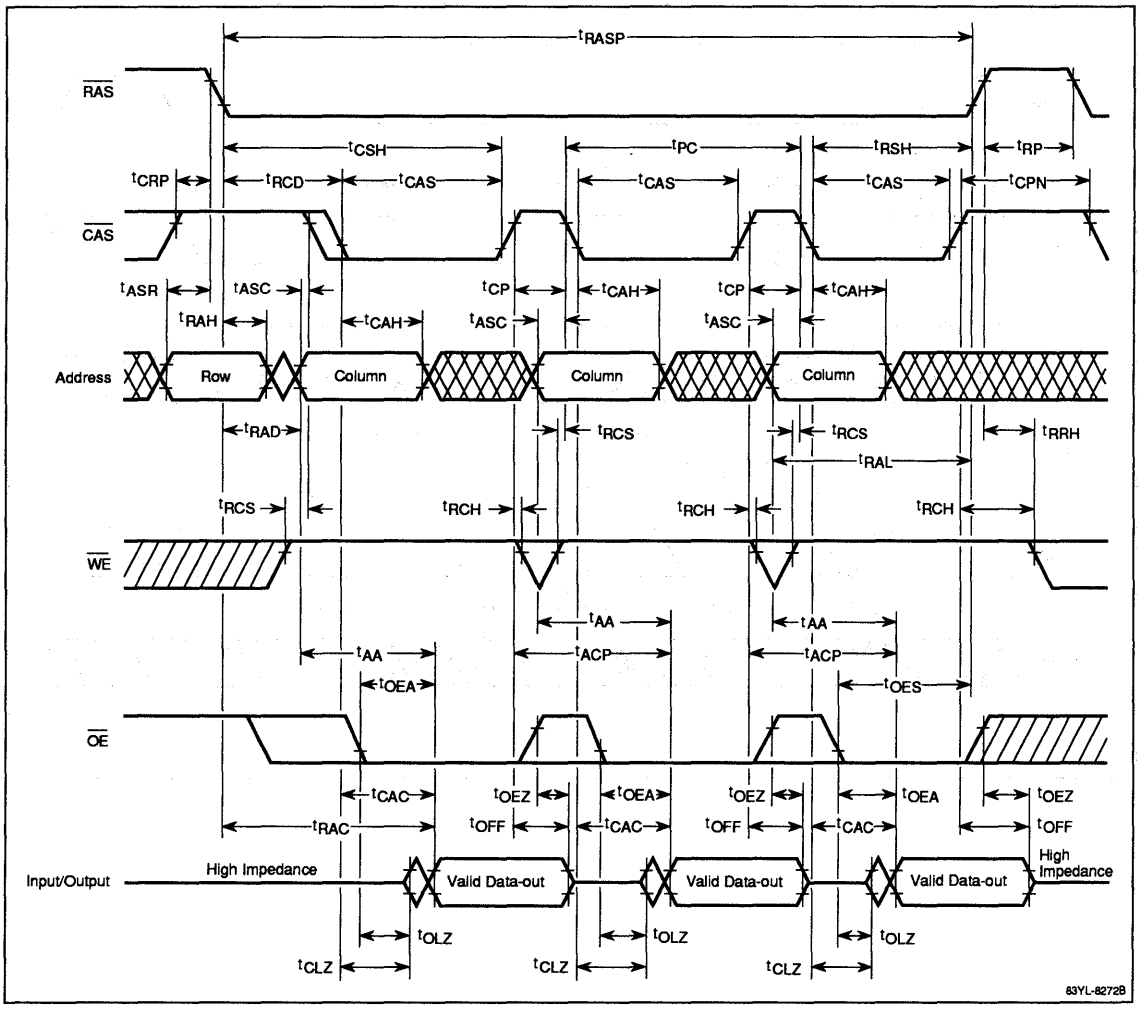
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



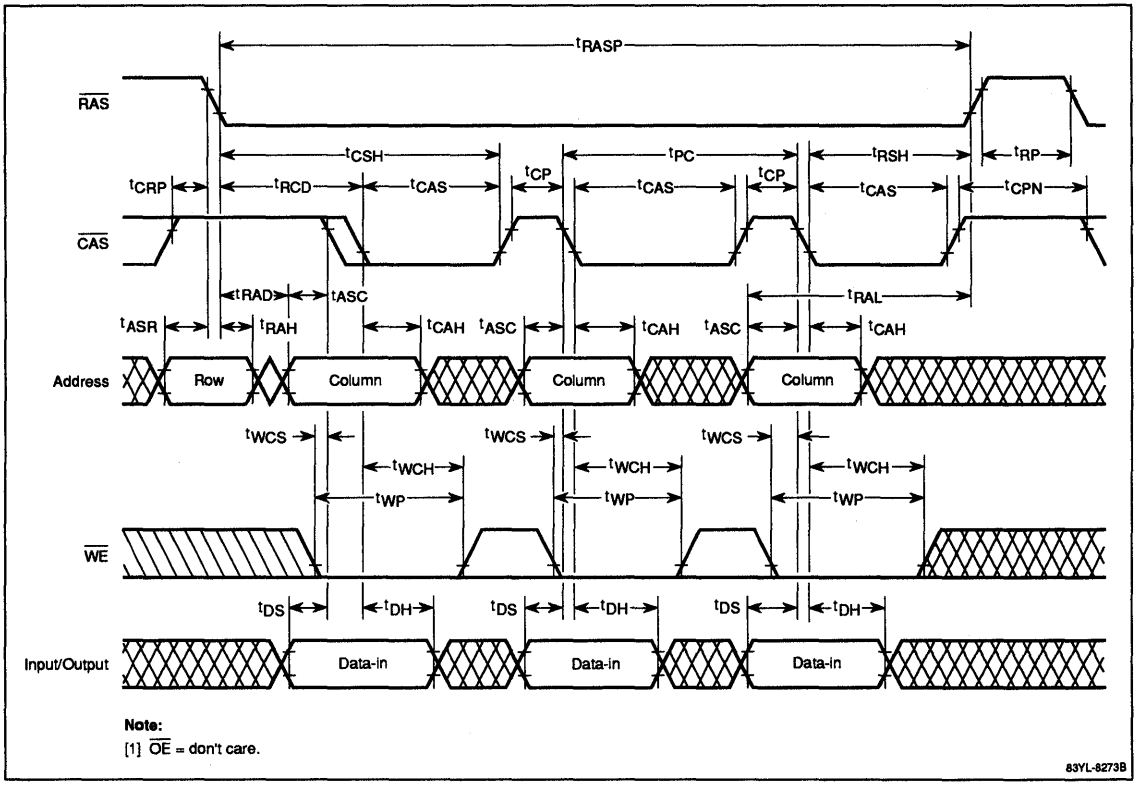
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

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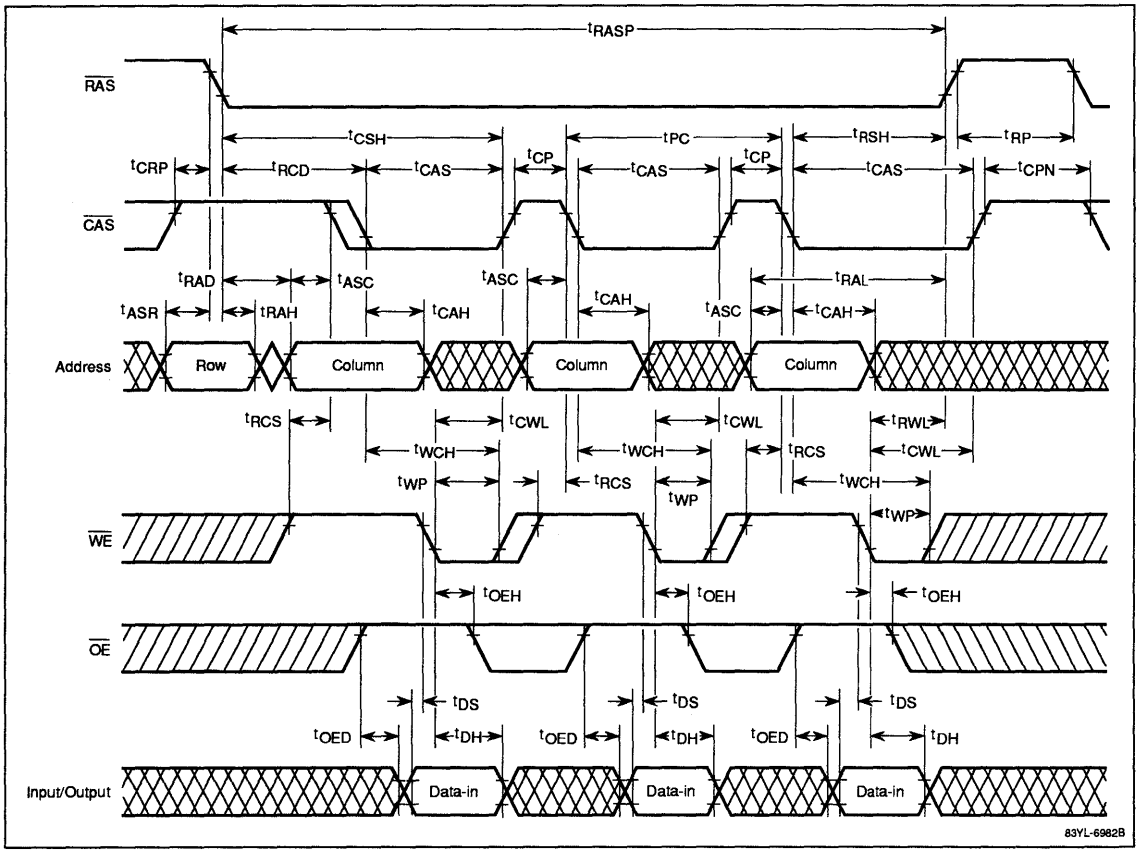
Timing Waveforms (cont)

Fast-Page Late Write Cycle



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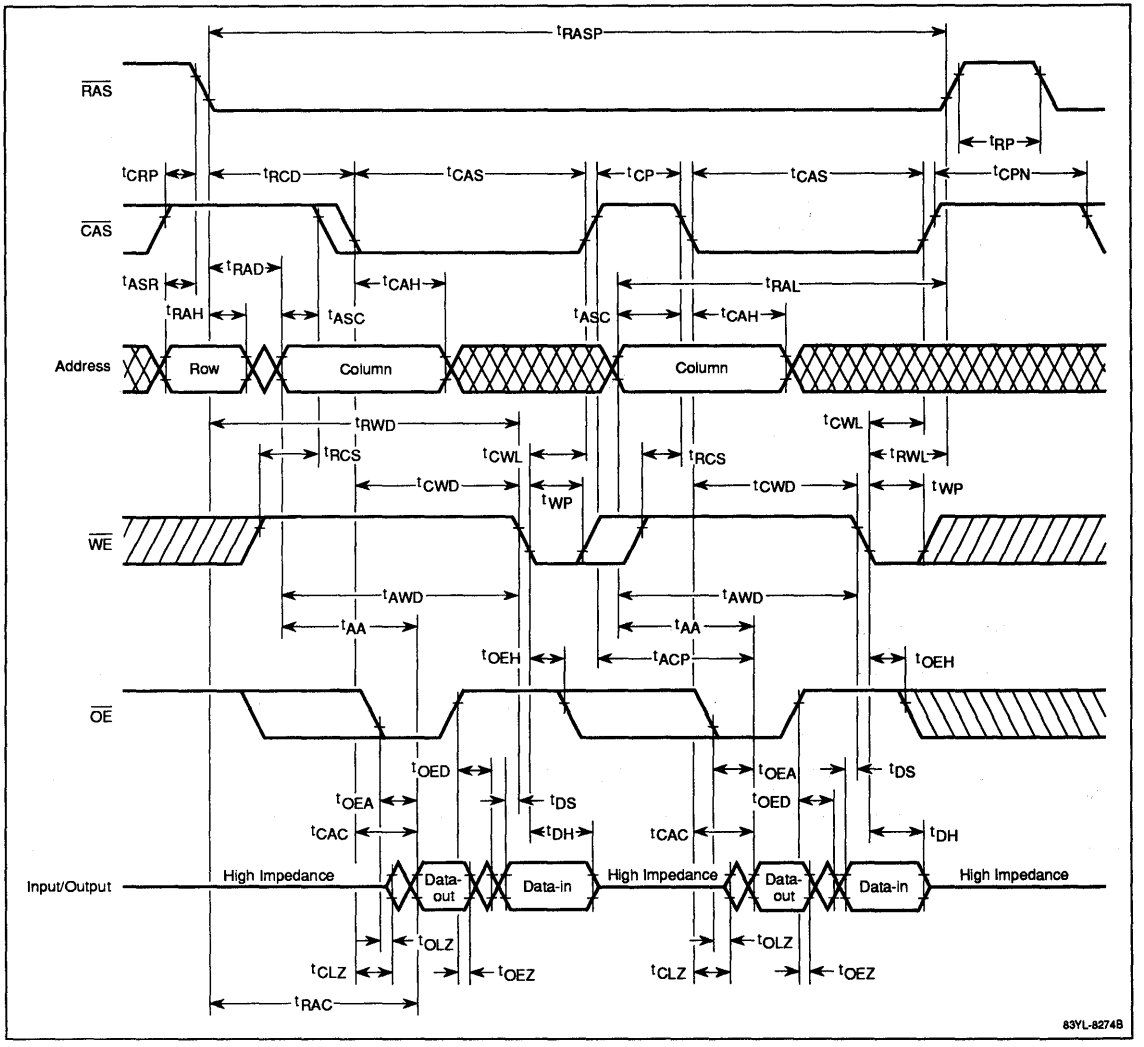
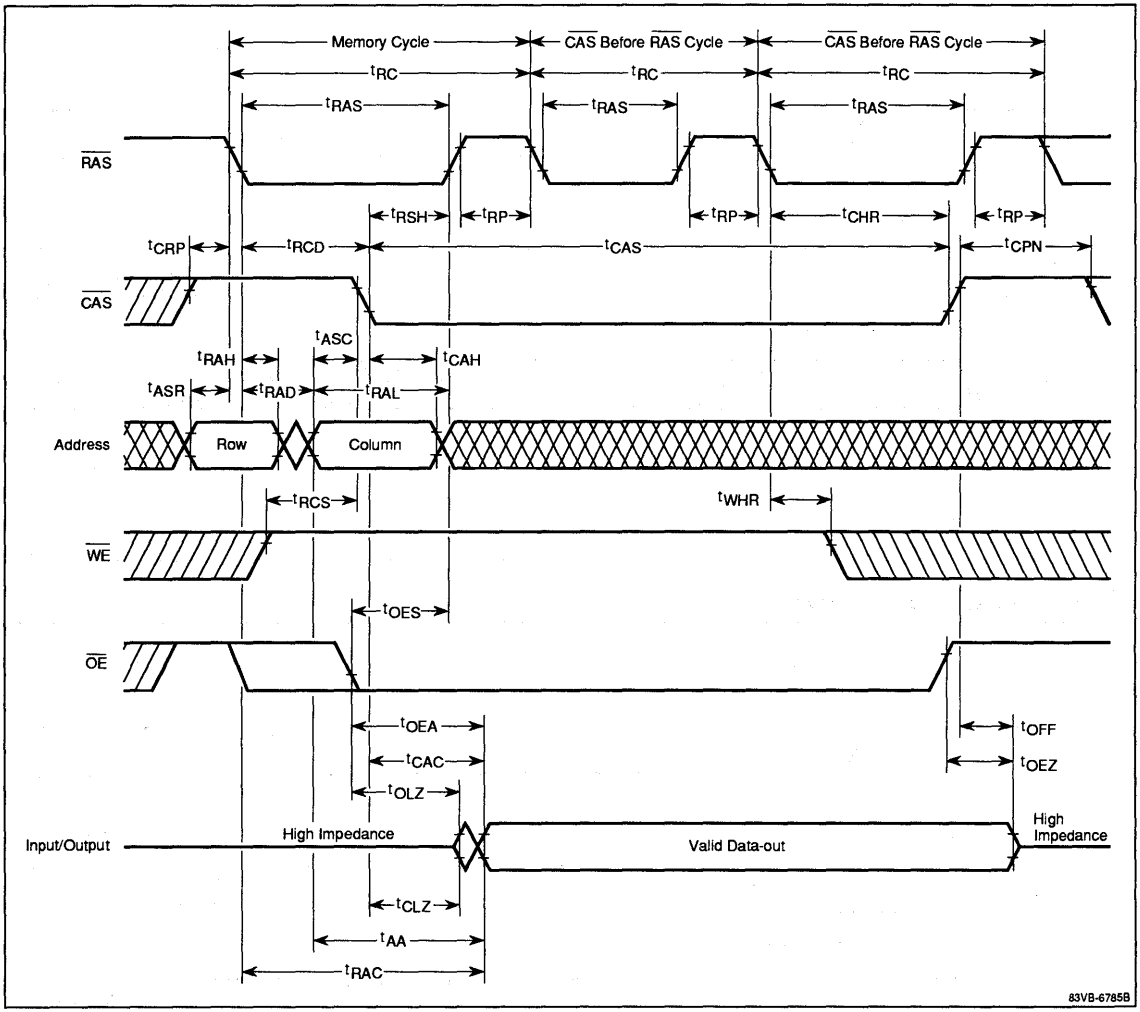
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



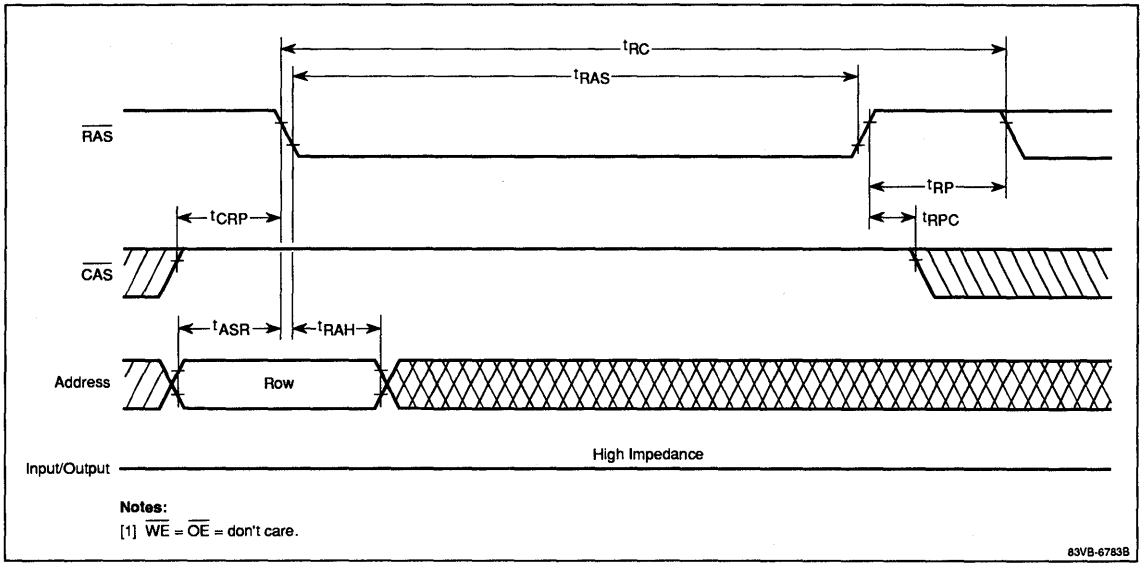
Timing Waveforms (cont)

Hidden Refresh Cycle

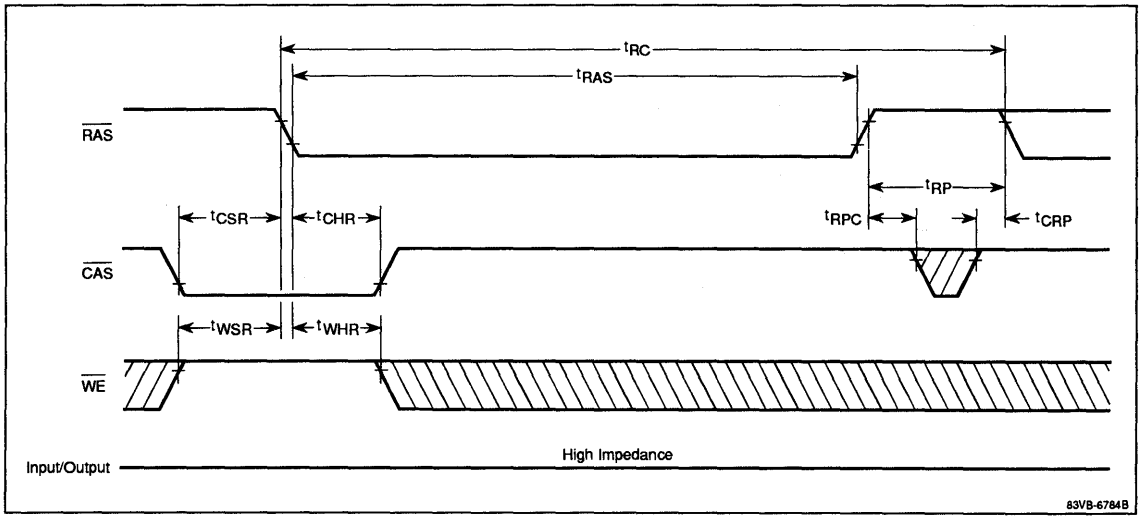


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

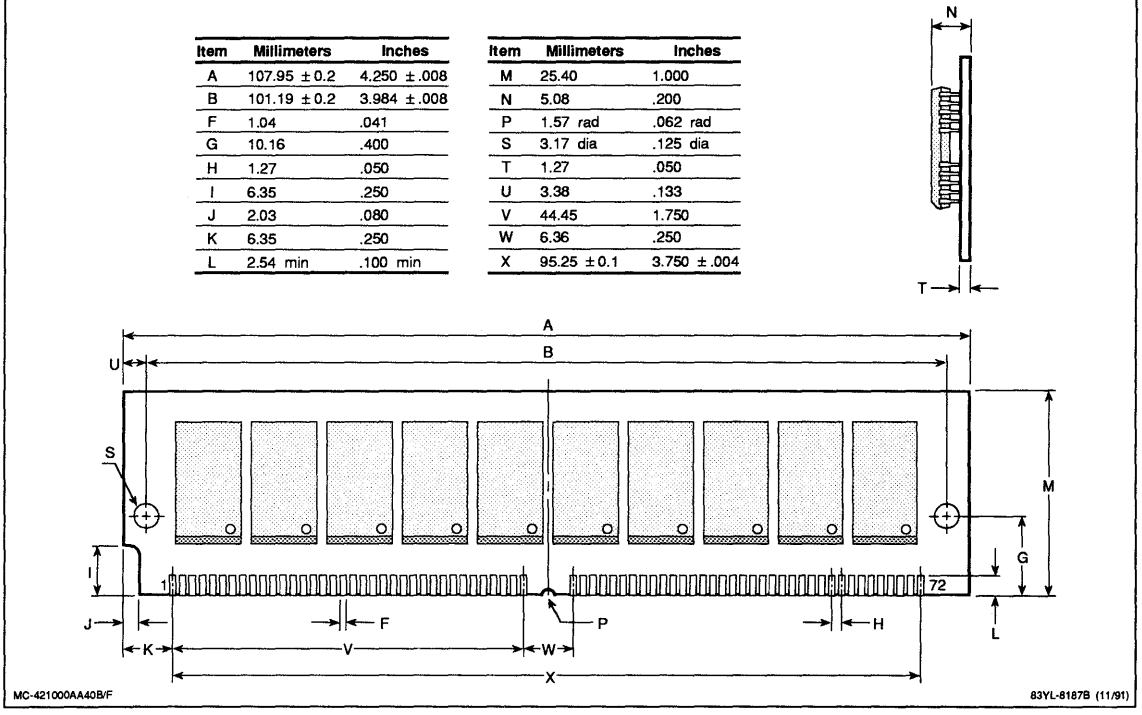


Package Drawings

72-Pin Socket-Mountable SIMM (MC-421000AA40B/F)

Item	Millimeters	Inches
A	107.95 ±0.2	4.250 ±.008
B	101.19 ±0.2	3.984 ±.008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	25.40	1.000
N	5.08	.200
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ±0.1	3.750 ±.004



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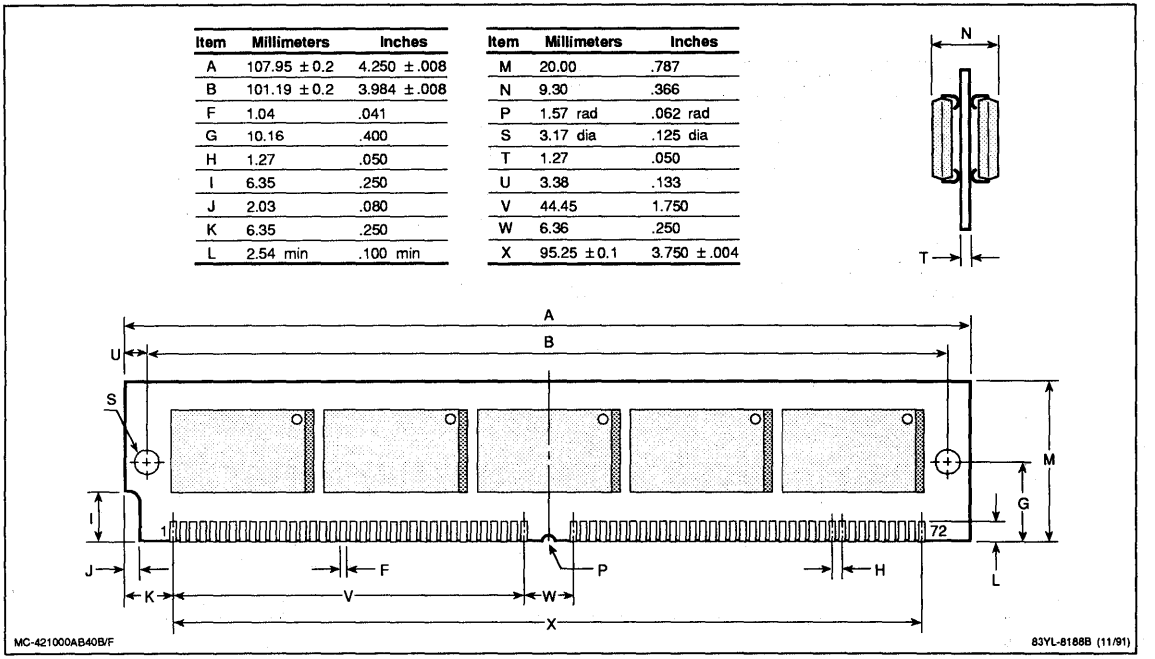
Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-421000AB40B/F)

Item	Millimeters	Inches
A	107.95 ±0.2	4.250 ±.008
B	101.19 ±0.2	3.984 ±.008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	20.00	.787
N	9.30	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ±0.1	3.750 ±.004



MC-422000A32
2,097,152 x 32-Bit
Dynamic CMOS RAM Module

Description

The MC-422000A32 is a fast-page dynamic RAM module organized as 2,097,152 words by 32 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 - A_9 during a 16-ms period.

The MC-422000A36 is packaged in a variety of Single Inline Memory Modules (SIMM™). Each SIMM contains sixteen 1,048,576 x 4-bit μPD424400 DRAMs, and 16 power supply decoupling capacitors for noise reduction. DQ_0 - DQ_{31} are common input/output pins.

Features

- 2,097,152-word by 32-bit organization
- Single +5-volt power supply
- Fast-page cycles
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

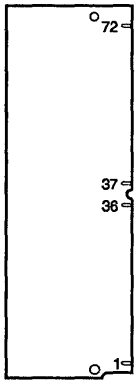
Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobes
DQ_0 - DQ_{31}	Common data inputs/outputs
$\overline{RAS}_0$ - $\overline{RAS}_3$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{16}
4	DQ_1
5	DQ_{17}
6	DQ_2
7	DQ_{18}
8	DQ_3
9	DQ_{19}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	NC
20	DQ_4
21	DQ_{20}
22	DQ_5
23	DQ_{21}
24	DQ_6
25	DQ_{22}
26	DQ_7
27	DQ_{23}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	A_9
33	$\overline{RAS}_3$
34	$\overline{RAS}_2$
35	NC
36	NC

Pin	Symbol
37	NC
38	NC
39	GND
40	$\overline{CAS}_0$
41	$\overline{CAS}_2$
42	$\overline{CAS}_3$
43	$\overline{CAS}_1$
44	$\overline{RAS}_0$
45	$\overline{RAS}_1$
46	NC
47	$\overline{WE}$
48	NC
49	DQ_8
50	DQ_{24}
51	DQ_9
52	DQ_{25}
53	DQ_{10}
54	DQ_{26}

Pin	Symbol
55	DQ_{11}
56	DQ_{27}
57	DQ_{12}
58	DQ_{28}
59	V_{CC}
60	DQ_{29}
61	DQ_{13}
62	DQ_{30}
63	DQ_{14}
64	DQ_{31}
65	DQ_{15}
66	NC
67	[Note 1]
68	[Note 1]
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

[1] Pins 67-70 are defined by access time:

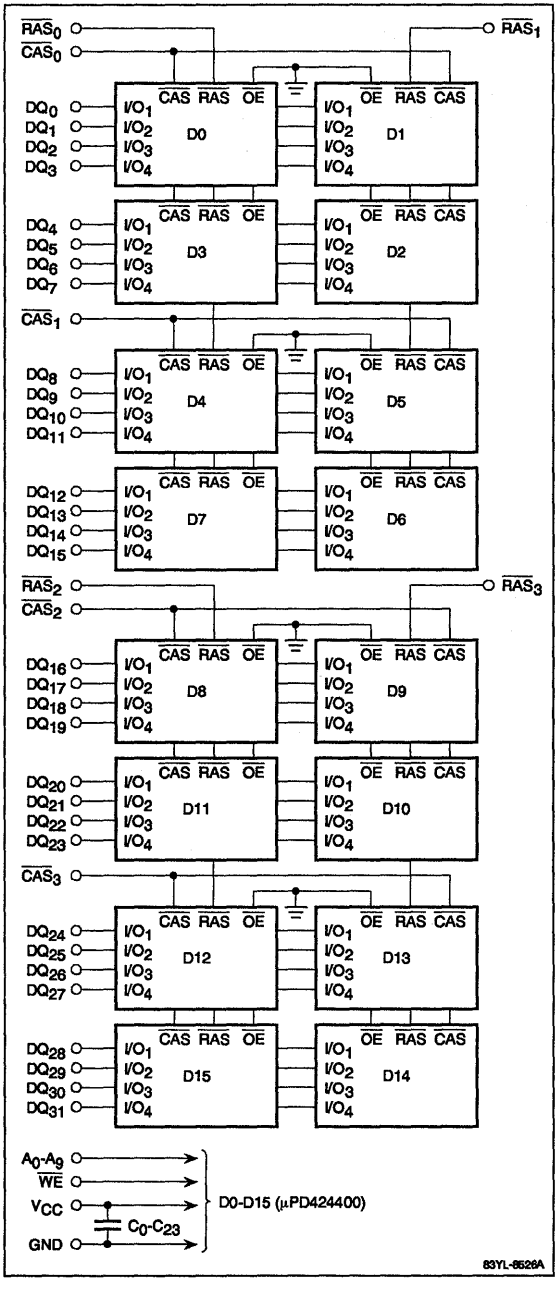
Pin	60 ns	70 ns	80 ns	100 ns
67	NC	NC	NC	NC
68	NC	NC	NC	NC
69	NC	GND	NC	GND
70	NC	NC	GND	GND

83FM-8525A

Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-422000A32B-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	9.3 mm (0.366 inch)	Sixteen μPD424400LA
B-70	70 ns				
B-80	80 ns				
B-10	100 ns				
MC-422000A32F-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				
F-10	100 ns				
MC-422000A32BJ-60	60 ns	72-pin socket-mountable SIMM (solder plating)	31.75 mm (1.250 inch)	9.3 mm (0.366 inch)	Sixteen μPD424400LA
BJ-70	70 ns				
BJ-80	80 ns				
BJ-10	100 ns				
MC-422000A32FJ-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FJ-70	70 ns				
FJ-80	80 ns				
FJ-10	100 ns				

Connection Diagram



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Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	16 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	121	pF	A_0 - A_9
	C_{I2}	137	pF	$\overline{WE}$
	C_{I3}	48	pF	$\overline{RAS}$
	C_{I4}	48	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{O1}	29	pF	DQ_0 - DQ_{31}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		32	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			16	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−160	160	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	DQ_0 to DQ_{31} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		1020		860		780		700	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1020		860		780		700	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		780		700		620		540	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1020		860		780		700	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0	20	0	20	0	20	0	25	ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		15		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	17		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
Data setup time	t_{CLZ}	0		0		0		0		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 10)

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AC Characteristics (cont)

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		20		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 14)

AC Characteristics (cont)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

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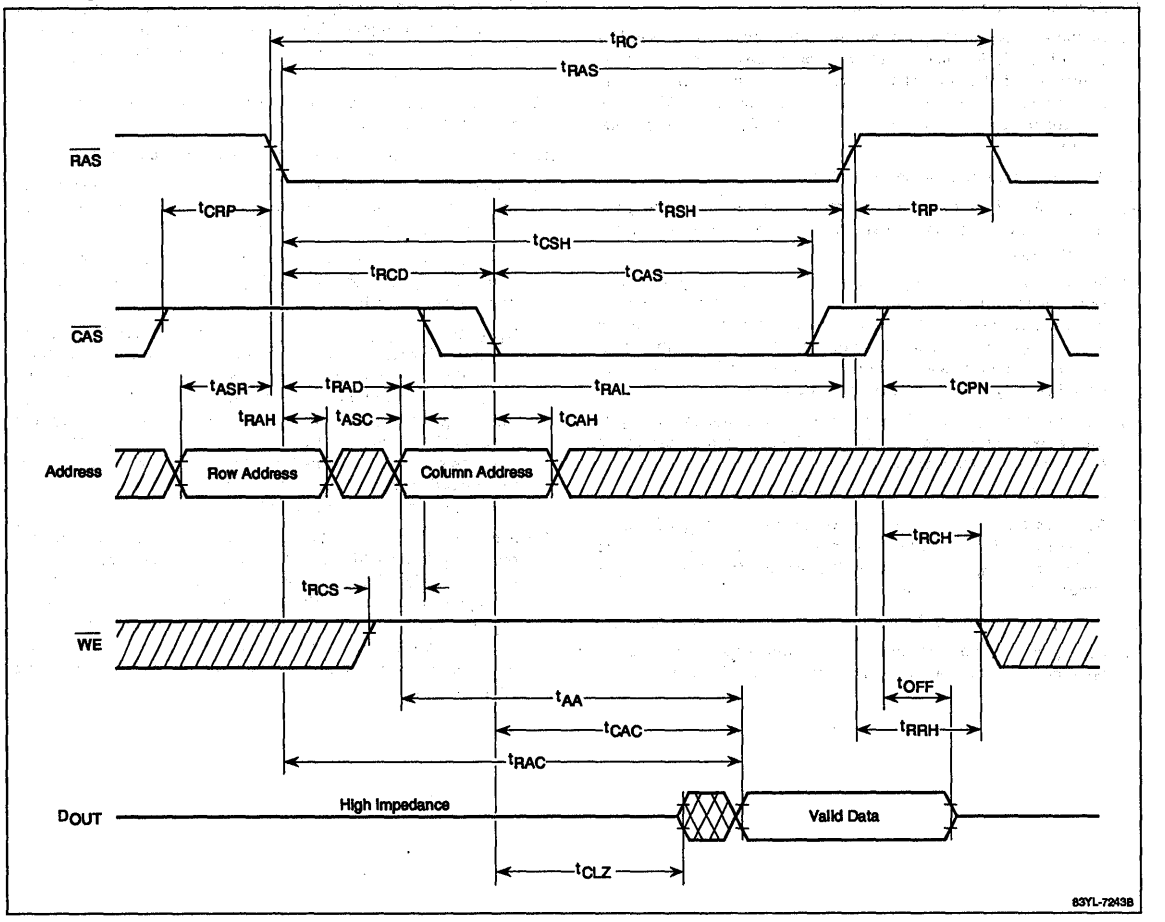
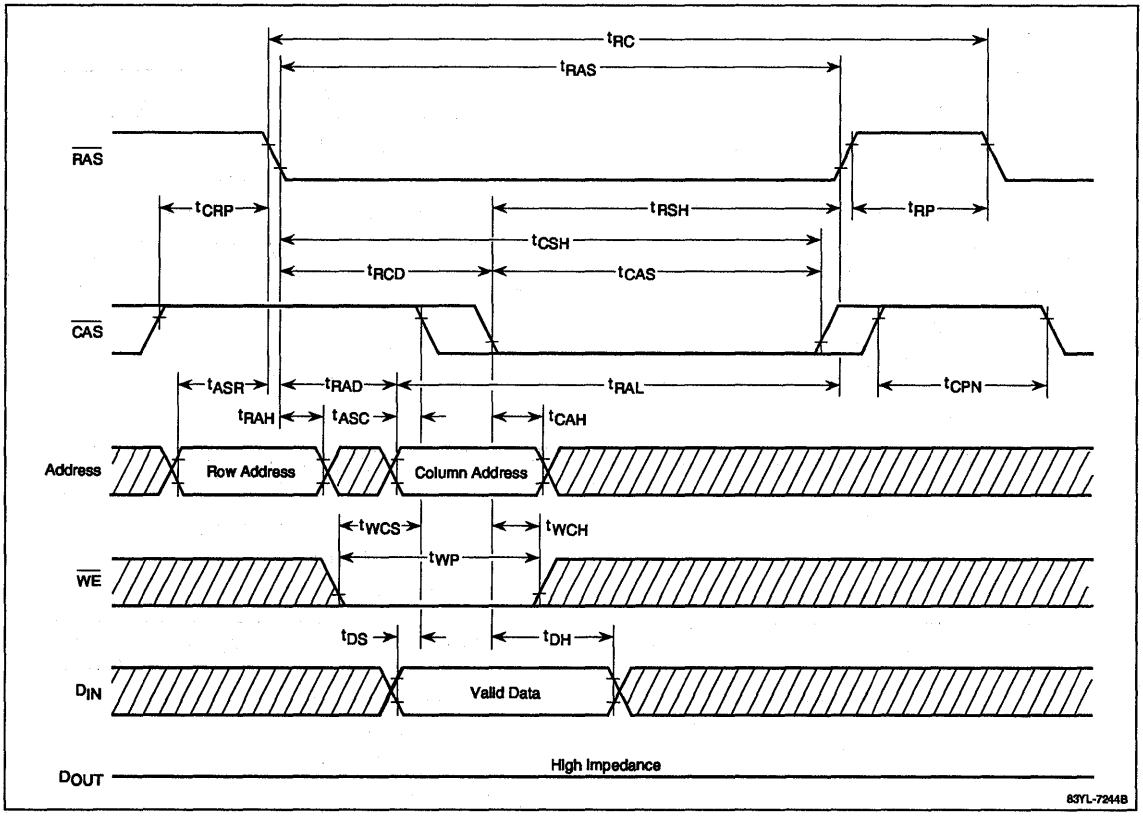
Timing Waveforms

Read Cycle



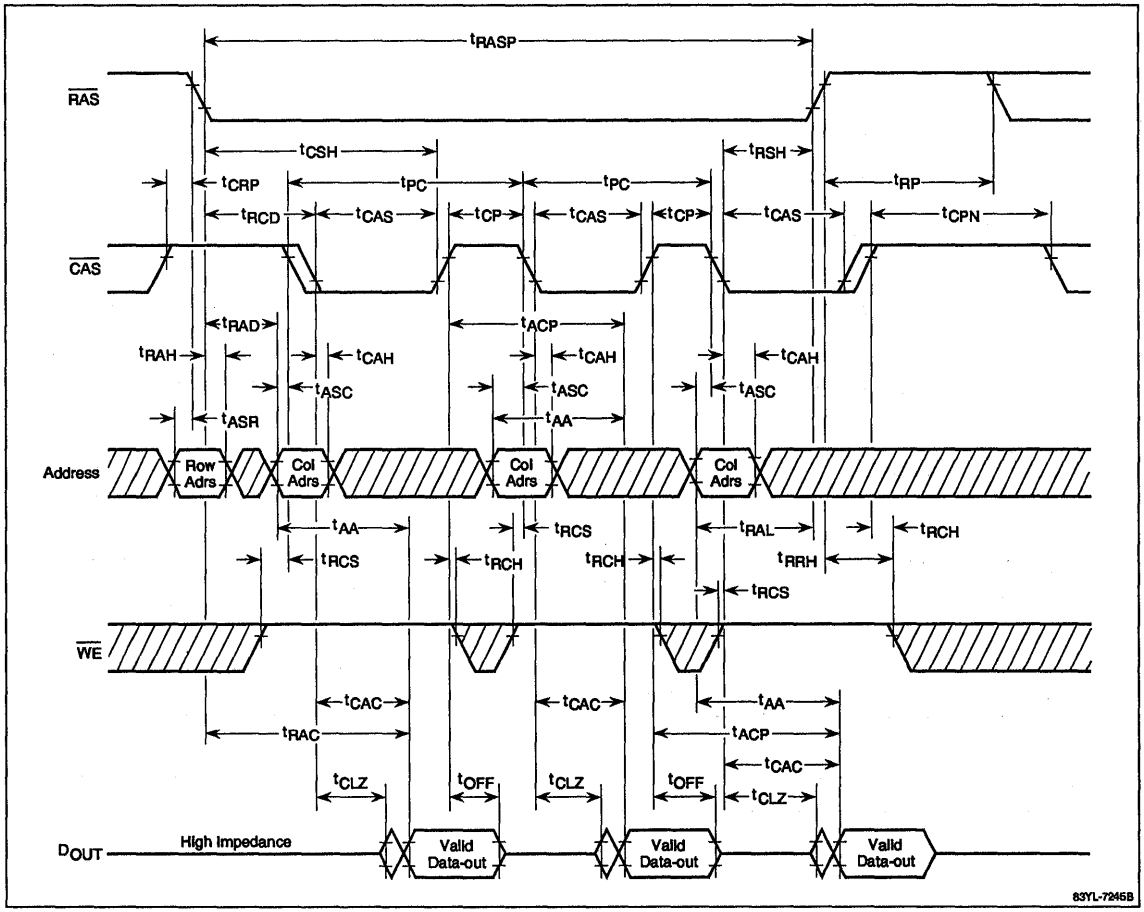
Timing Waveforms (cont)

Early Write Cycle



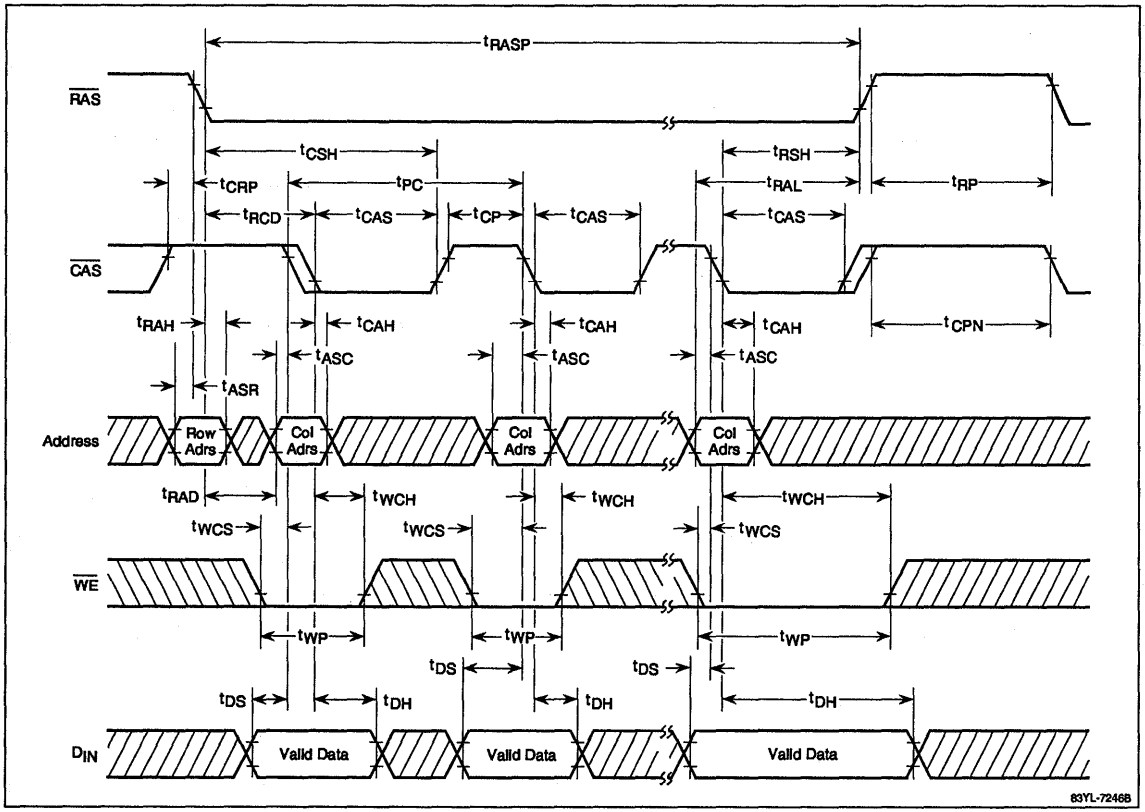
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



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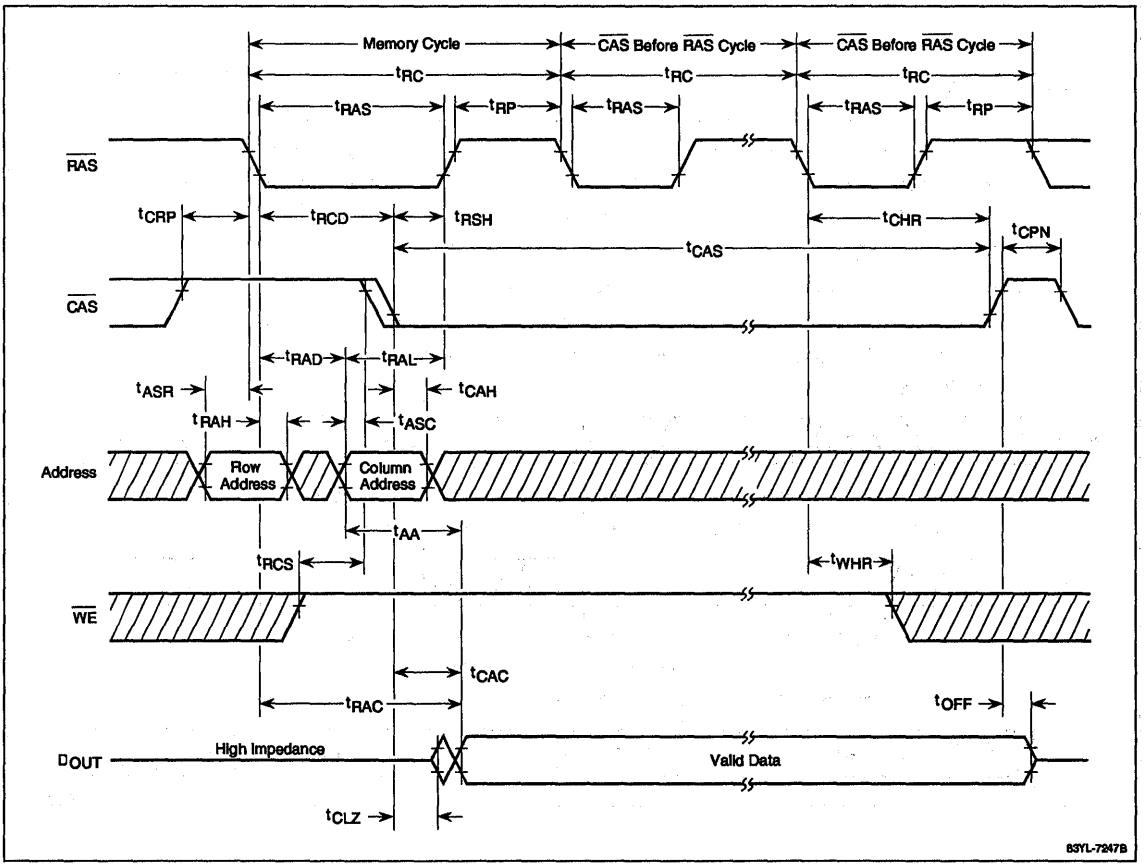
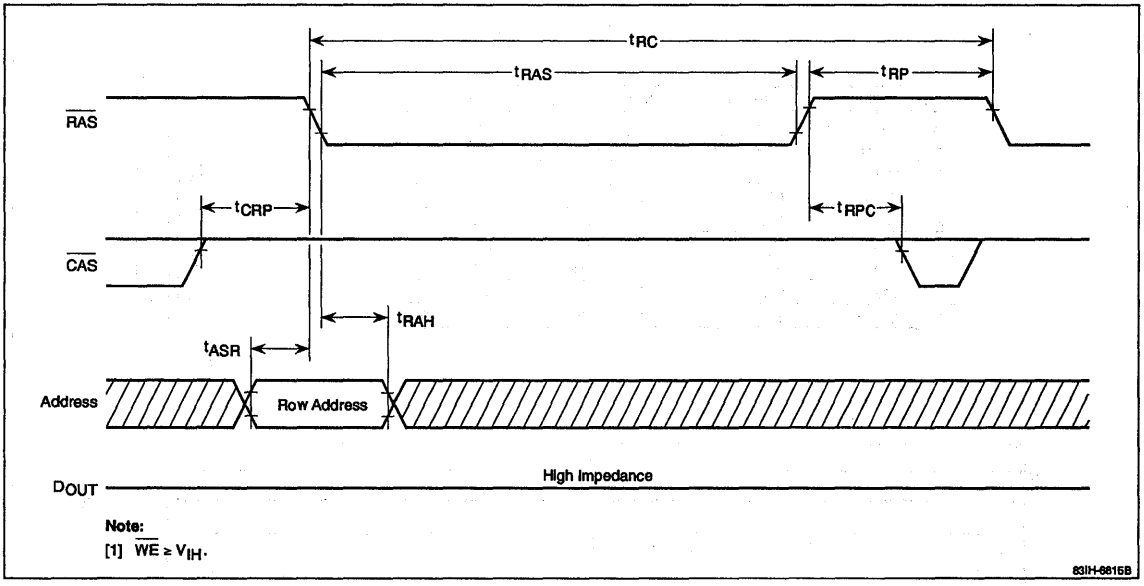
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

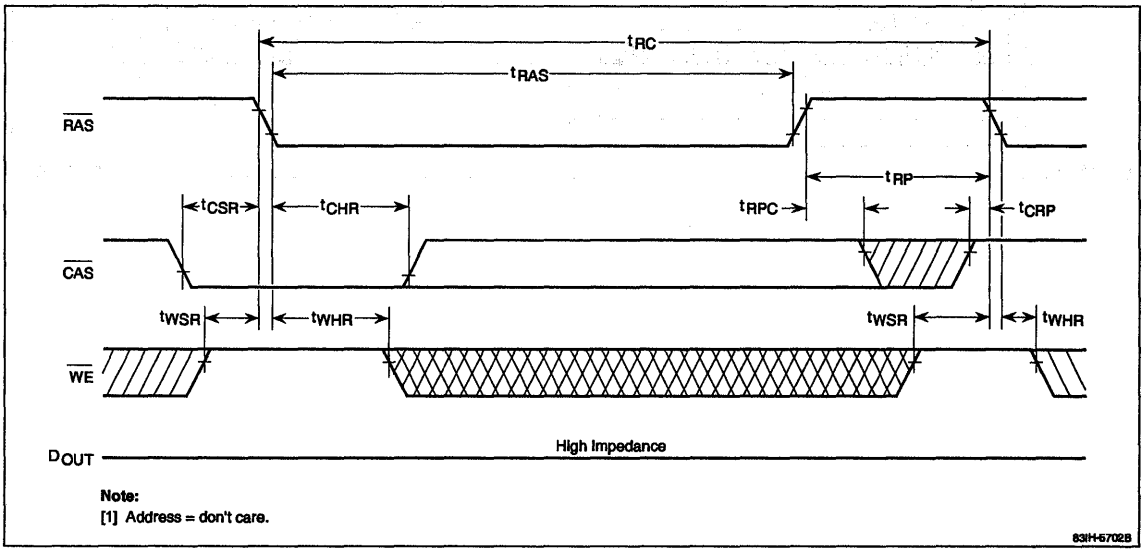
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

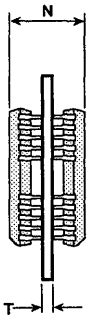
83IH-6702B

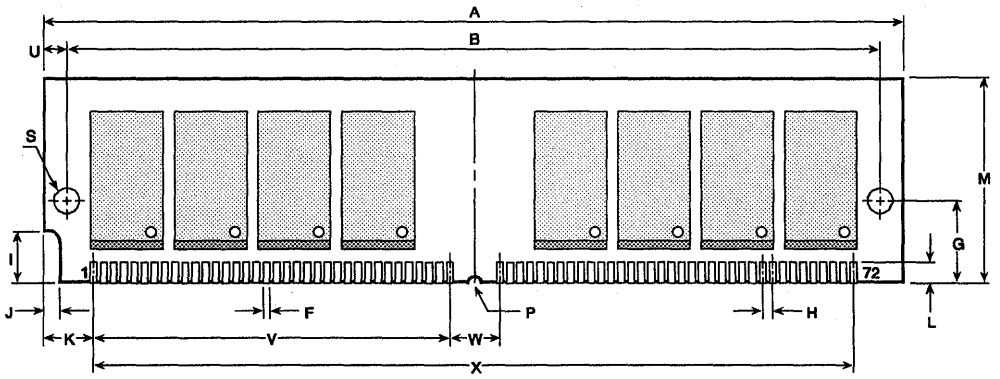
Package Drawings

72-Pin Socket Mountable SIMM (MC-422000A32B/F)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	25.4	1.000
N	9.3	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004





MC-422000A32B/F

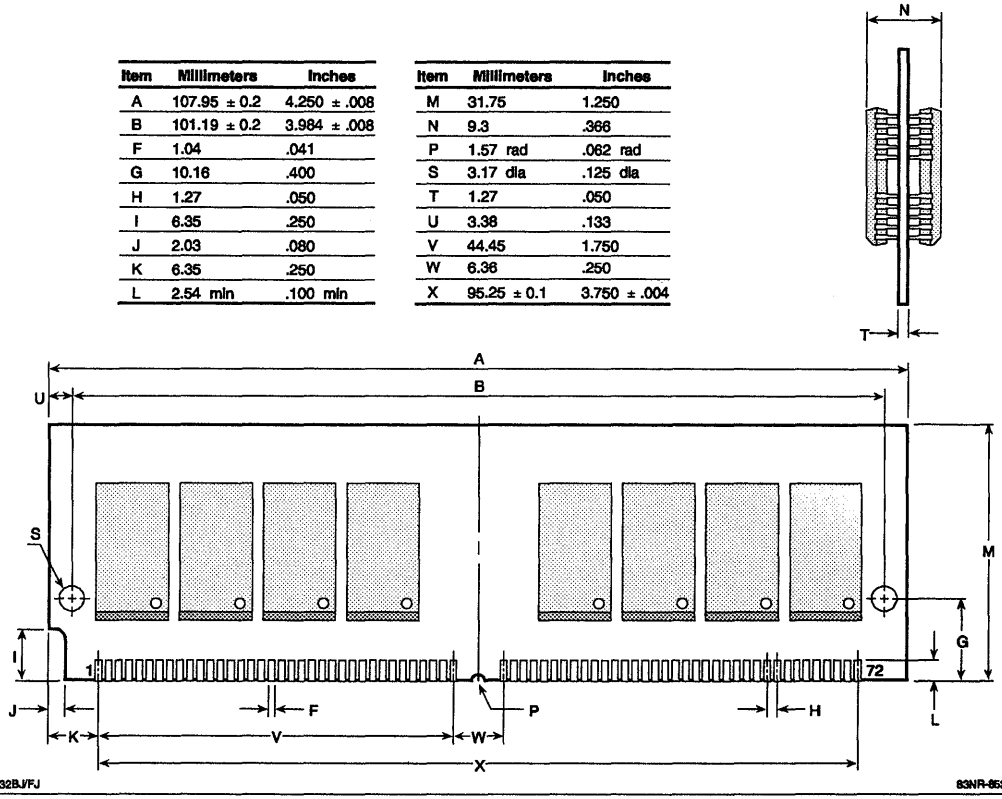
83NR-8528B (3/92)

Package Drawings (cont)

72-Pin Socket Mountable SIMM (MC-422000A32/BJ/FJ)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	31.75	1.250
N	9.3	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-422000A32BJFJ

83NR-8527B (7/92)

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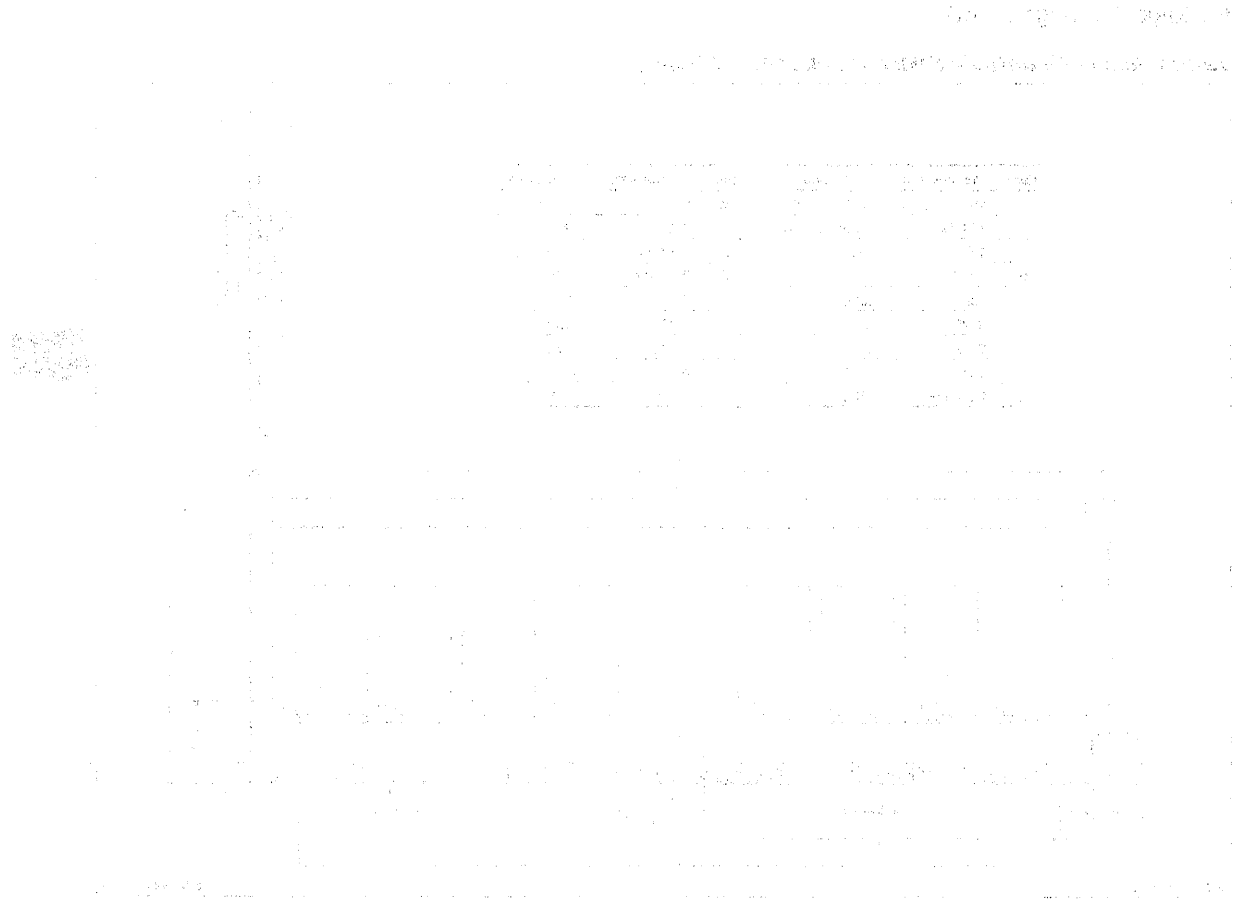


MC-422000A36
2,097,152 x 36-Bit
Dynamic CMOS RAM Module

Description

The MC-422000A36 is a fast-page dynamic RAM module organized as 2,097,152 words by 36 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 - A_9 during a 16-ms period.

The MC-422000A36 is packaged in a variety of Single Inline Memory Modules (SIMM™). Each SIMM contains sixteen 1,048,576 x 4-bit μPD424400 DRAMs, eight 1,048,576 x 1-bit μPD421000 DRAMs, and 24 power supply decoupling capacitors for noise reduction. DQ_0 - DQ_{35} are common input/output pins.

Features

- 2,097,152-word by 36-bit organization
- Single +5-volt power supply
- Fast-page cycles
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

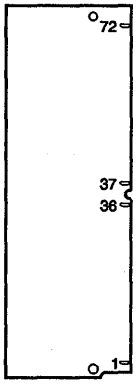
Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobes
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS}_0$ - $\overline{RAS}_3$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol	Pin	Symbol	Pin	Symbol
1	GND	19	NC	37	DQ_{17}
2	DQ_0	20	DQ_4	38	DQ_{35}
3	DQ_{18}	21	DQ_{22}	39	GND
4	DQ_1	22	DQ_5	40	$\overline{CAS}_0$
5	DQ_{19}	23	DQ_{23}	41	$\overline{CAS}_2$
6	DQ_2	24	DQ_6	42	$\overline{CAS}_3$
7	DQ_{20}	25	DQ_{24}	43	$\overline{CAS}_1$
8	DQ_3	26	DQ_7	44	$\overline{RAS}_0$
9	DQ_{21}	27	DQ_{25}	45	$\overline{RAS}_1$
10	V_{CC}	28	A_7	46	NC
11	NC	29	NC	47	$\overline{WE}$
12	A_0	30	V_{CC}	48	NC
13	A_1	31	A_8	49	DQ_9
14	A_2	32	A_9	50	DQ_{27}
15	A_3	33	$\overline{RAS}_3$	51	DQ_{10}
16	A_4	34	$\overline{RAS}_2$	52	DQ_{28}
17	A_5	35	DQ_{26}	53	DQ_{11}
18	A_6	36	DQ_8	54	DQ_{29}

Pin	Symbol
55	DQ_{12}
56	DQ_{30}
57	DQ_{13}
58	DQ_{31}
59	V_{CC}
60	DQ_{32}
61	DQ_{14}
62	DQ_{33}
63	DQ_{15}
64	DQ_{34}
65	DQ_{16}
66	NC
67	[Note 1]
68	[Note 1]
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

[1] Pins 67-70 are defined by access time:

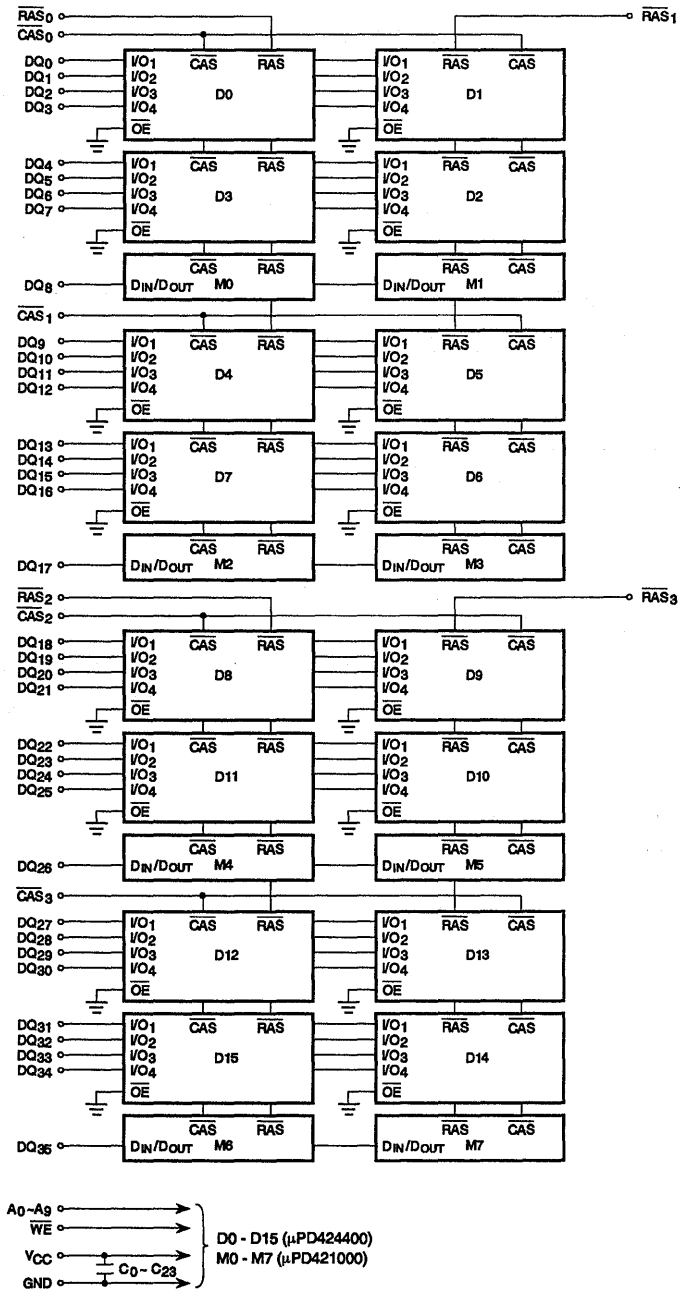
Pin	60 ns	70 ns	80 ns	100 ns
67	NC	NC	NC	NC
68	NC	NC	NC	NC
69	NC	GND	NC	GND
70	NC	NC	GND	GND

83YL-8515A

Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-422000A36B-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.000 inch)	9.3 mm (0.366 inch)	Sixteen μPD424400LA Eight μPD421000GX
B-70	70 ns				
B-80	80 ns				
MC-422000A36F-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				
MC-422000A36BJ-60	60 ns	72-pin socket-mountable SIMM (solder plating)	31.75 mm (1.250 inch)	9.3 mm (0.366 inch)	Sixteen μPD424400LA Eight μPD421000LA
BJ-70	70 ns				
BJ-80	80 ns				
MC-422000A36FJ-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FJ-70	70 ns				
FJ-80	80 ns				
MC-422000A36BT-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.000 inch)	9.3 mm (0.161 inch)	Sixteen μPD424400GS Eight μPD421000GX
BT-70	70 ns				
BT-80	80 ns				
MC-422000A36FT-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FT-70	70 ns				
FT-80	80 ns				

Connection Diagram



10g

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	24 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	161	pF	A_0 - A_9
	C_{I2}	193	pF	$\overline{WE}$
	C_{I3}	62	pF	$\overline{RAS}$
	C_{I4}	62	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{O1}	29	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	39	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		48	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	240	240	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-60		-70		-80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		1380		1180		1060	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1380		1180		1060	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		1100		980		860	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1380		1180		1060	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0	20	0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		17		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		ns	
Data setup time	t_{CLZ}	0		0		0		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10	20	10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		15		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	ns	(Note 10)
Fast-page cycle time	t_{PC}	40		45		50		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	60	25	60	ns	(Note 11)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

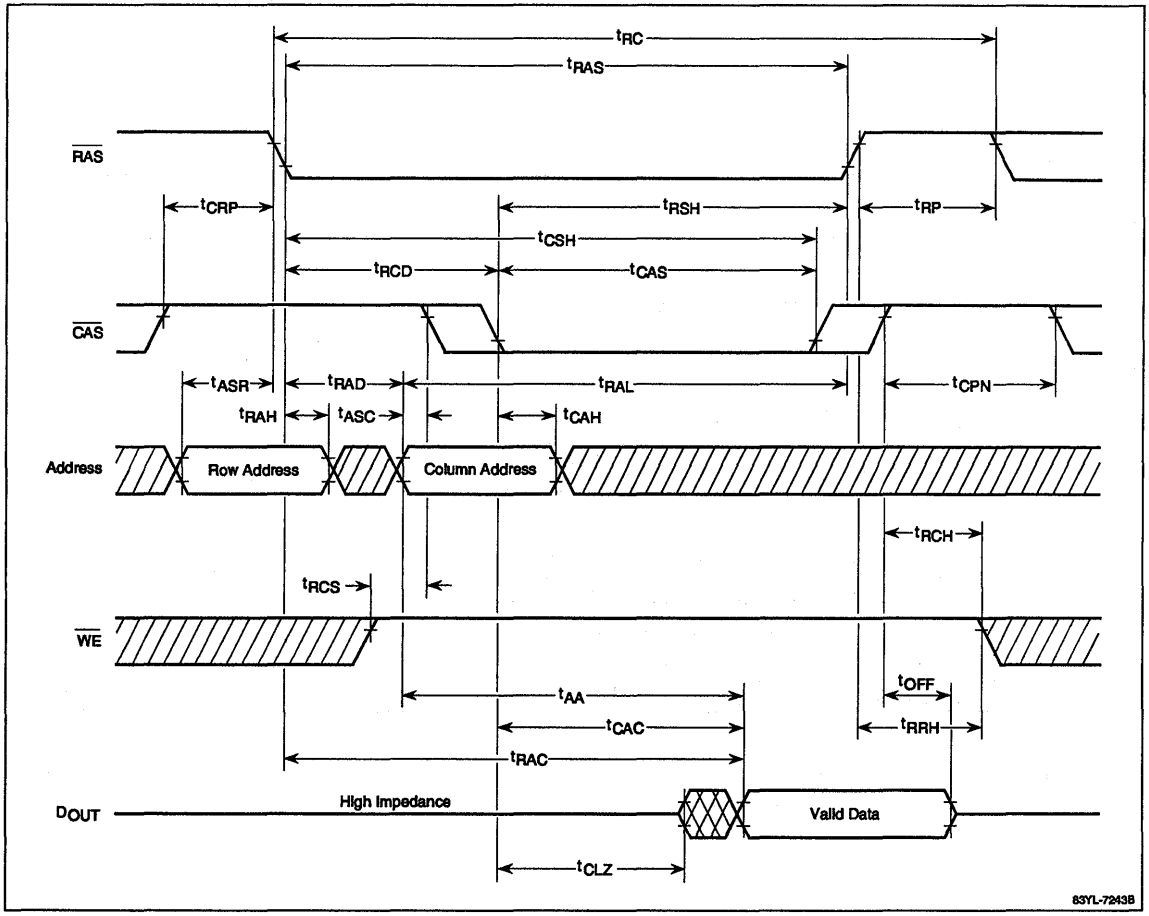
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Timing Waveforms

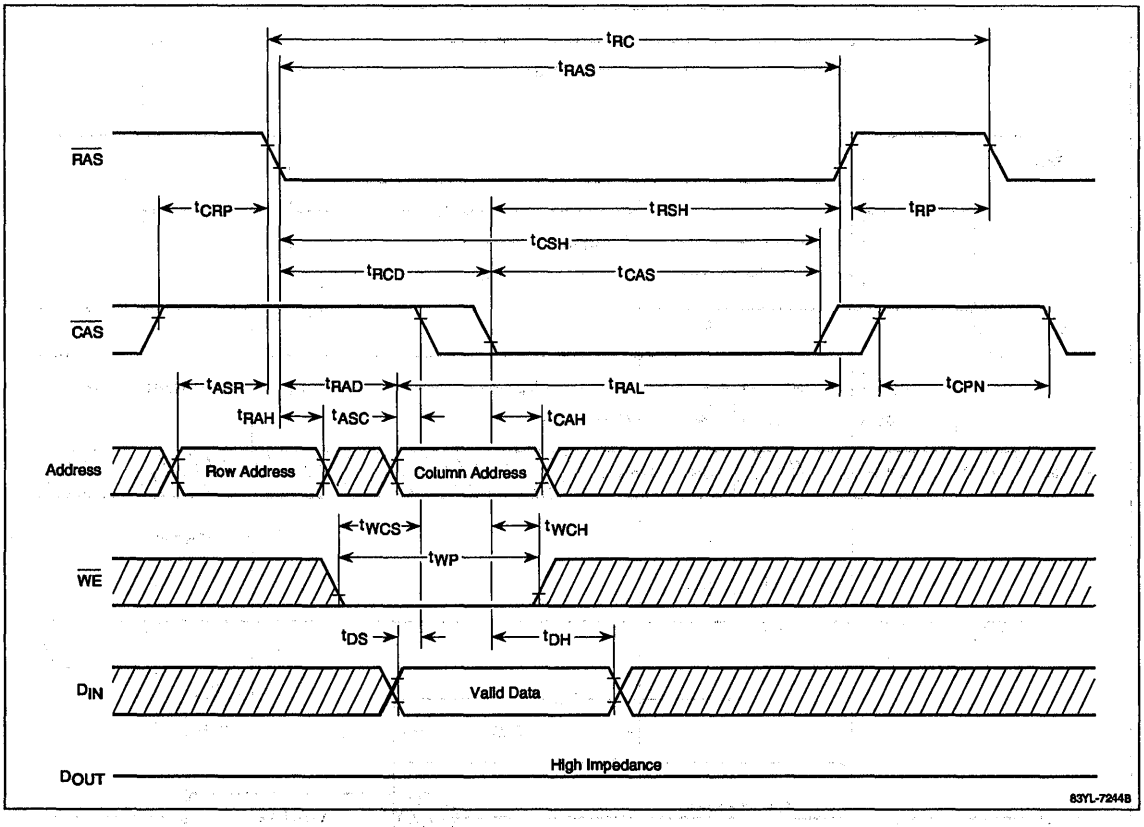
Read Cycle



10g

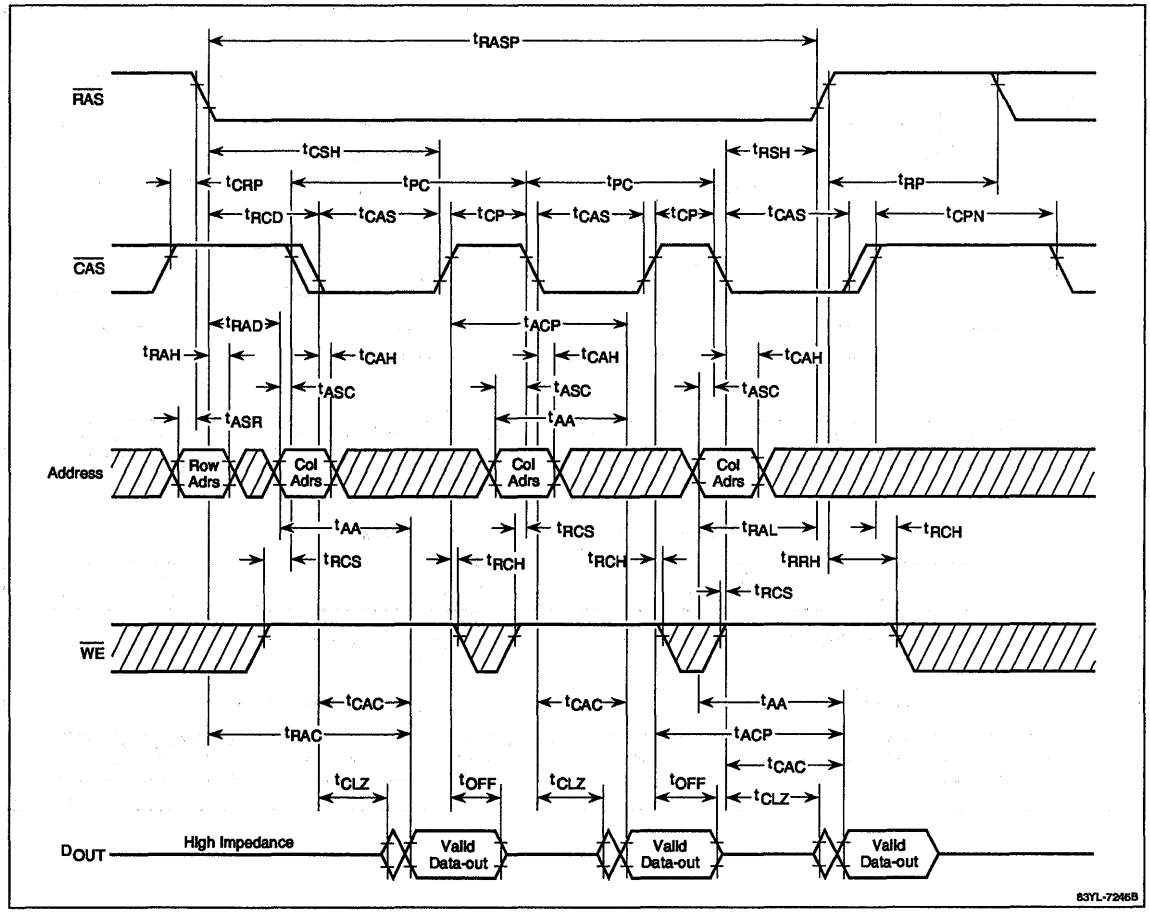
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Fast-Page Read Cycle



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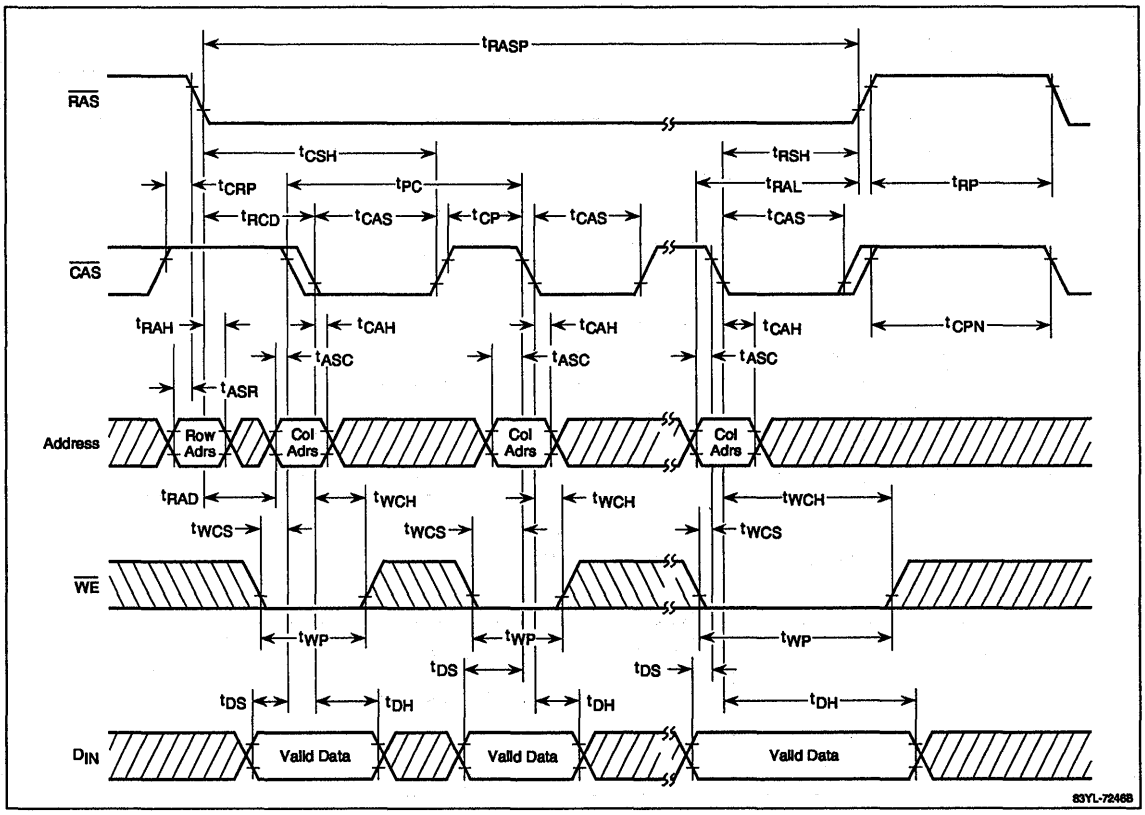
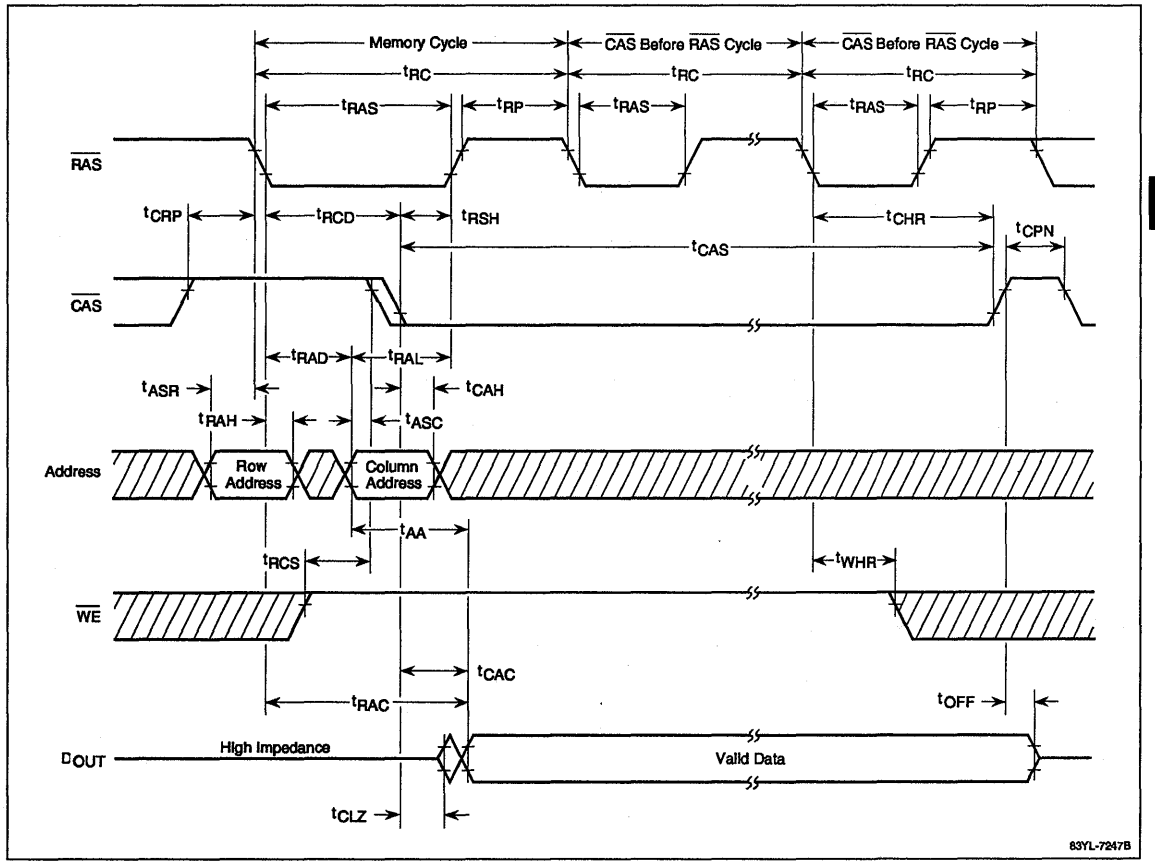
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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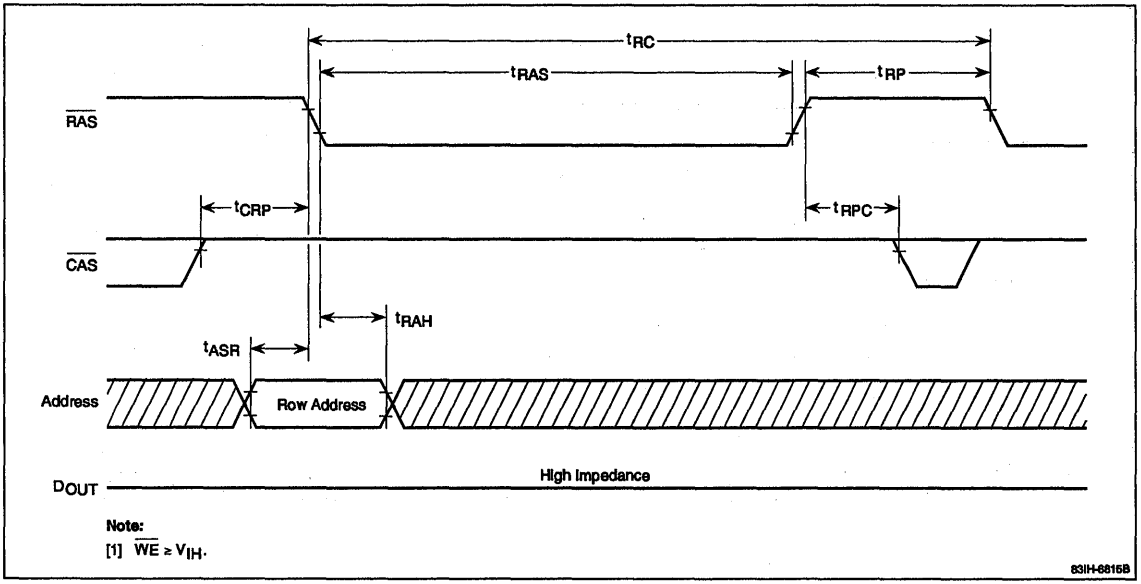
Timing Waveforms (cont)

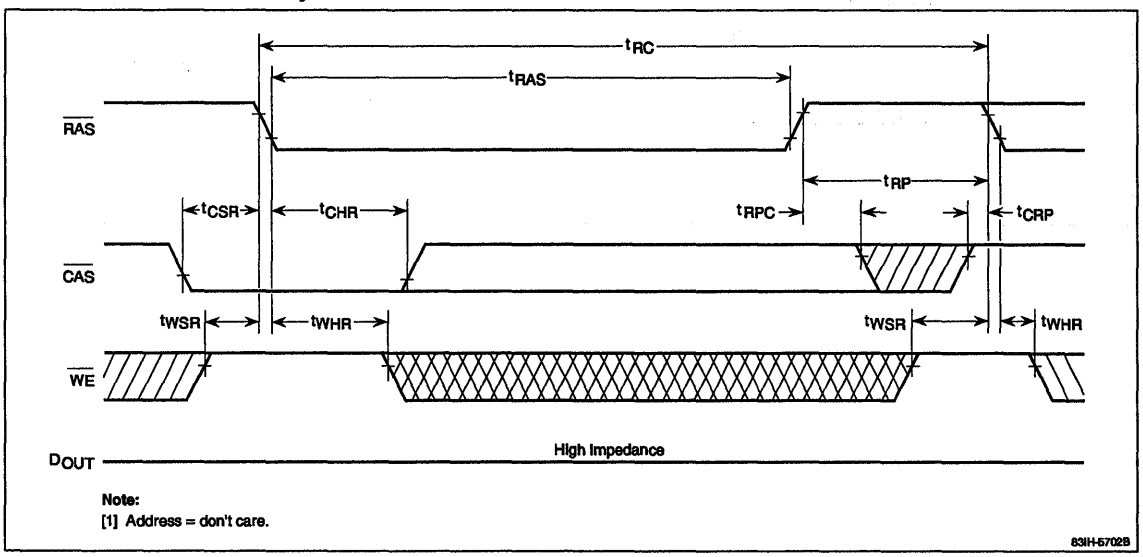
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

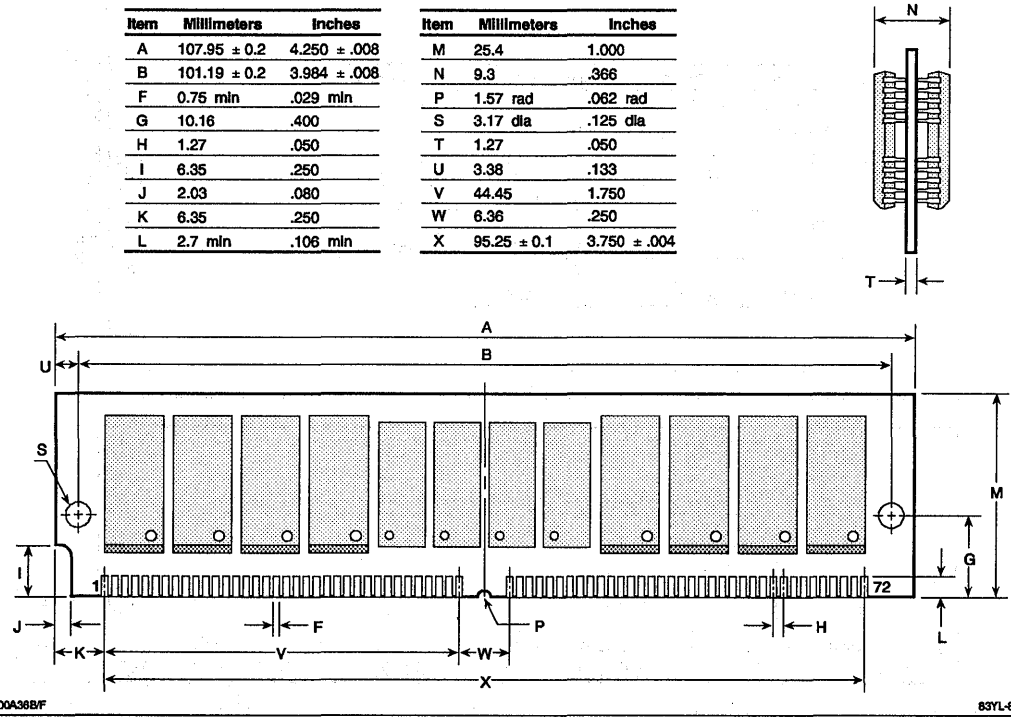
83IH-5702B

Package Drawings

72-Pin Socket-Mountable SIMM (MC-422000A36: Suffix B, F)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	9.3	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



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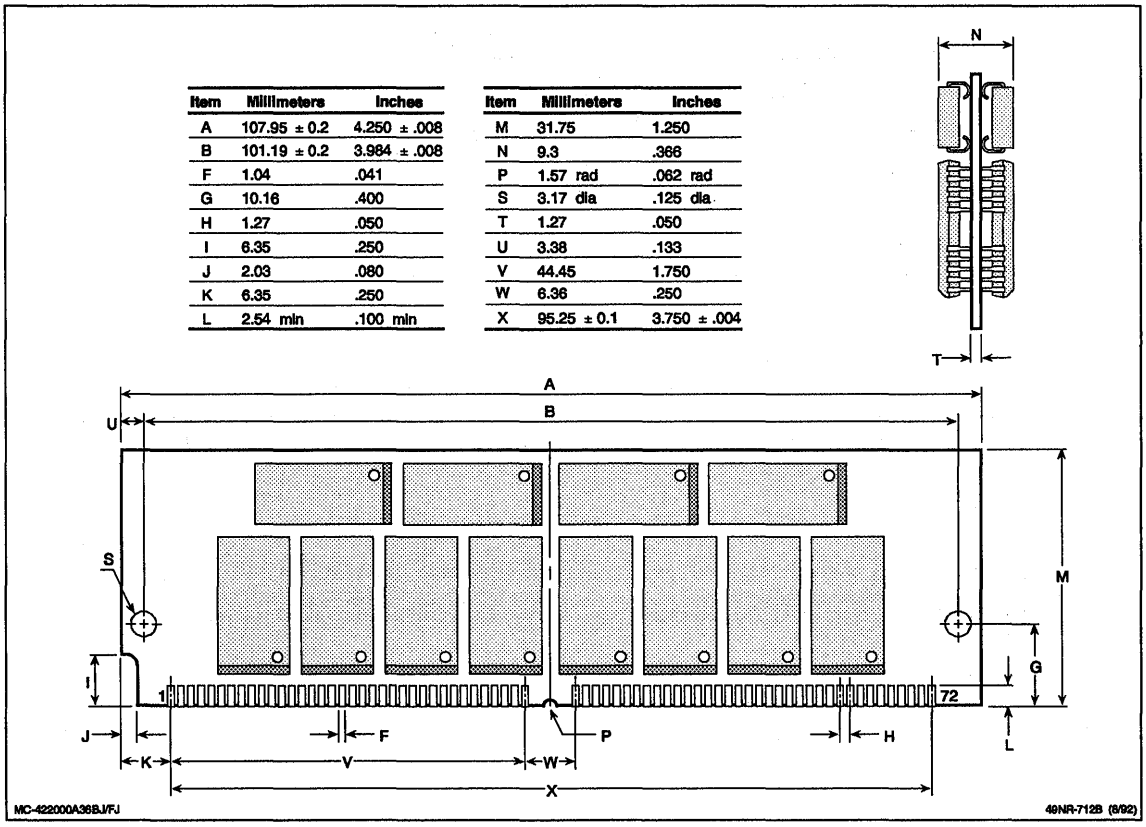
Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-422000A36: Suffix BJ, FJ)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	31.75	1.250
N	9.3	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004

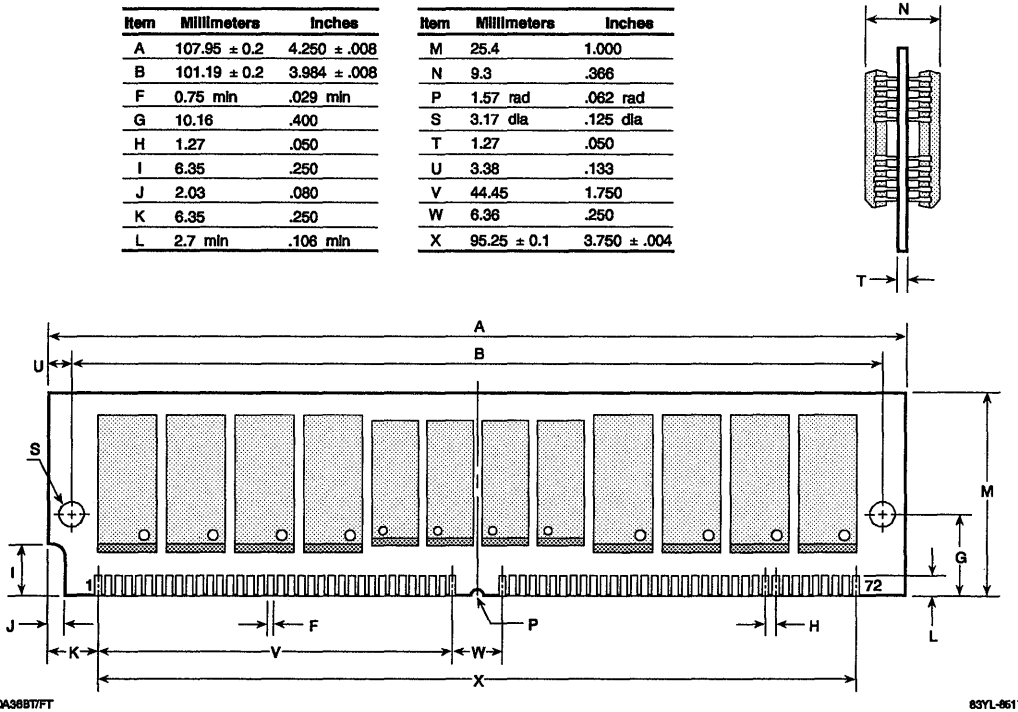


Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-422000A36: Suffix BT, FT)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	9.3	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-422000A36BT/FT

83YL-8617B (8/92)

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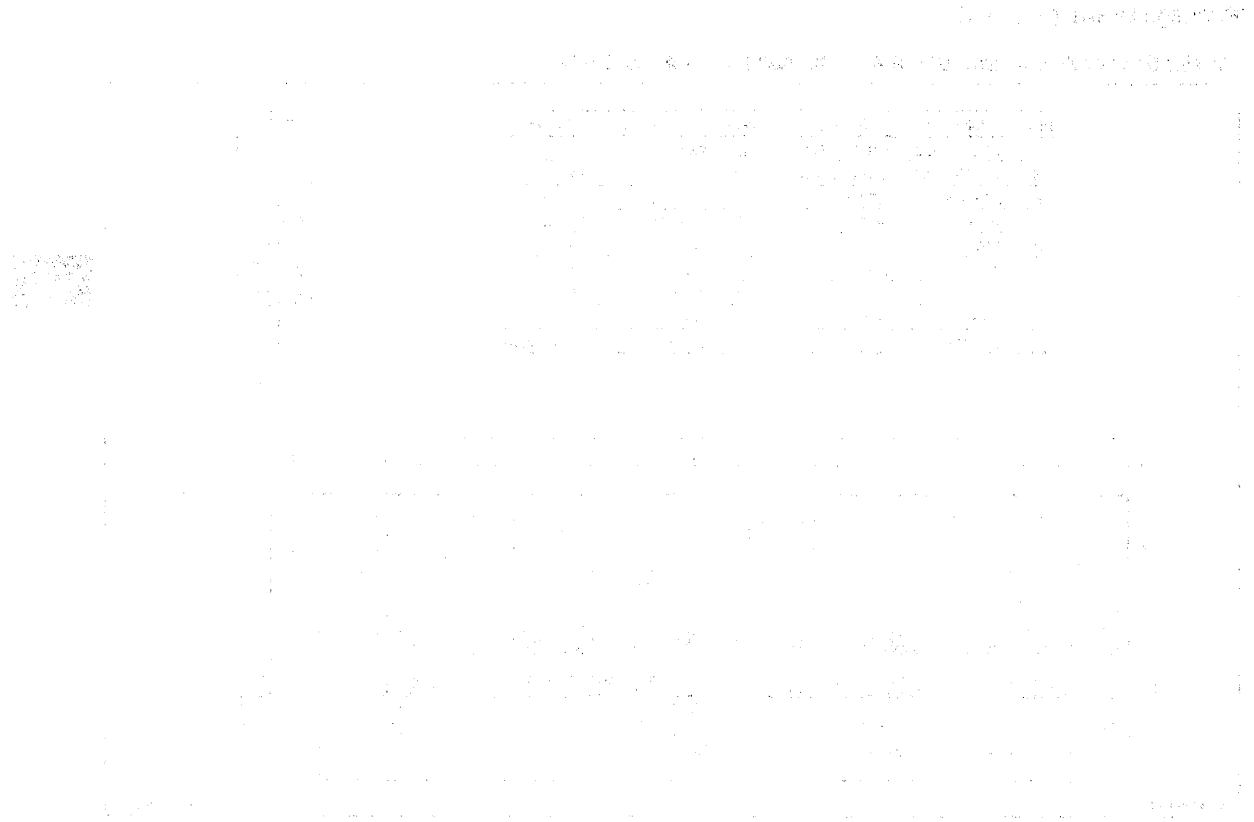


MC-422000AA40
2,097,152 x 40-Bit
Dynamic CMOS RAM Module

Description

The MC-422000AA40 is a fast-page dynamic RAM module organized as 2,097,152 words by 40 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 through A_9 during a 16-ms period.

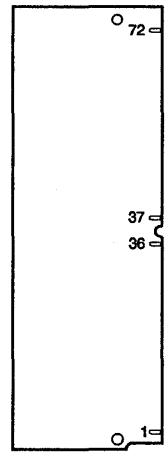
Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. Each SIMM contains twenty 1,048,576 x 4-bit DRAMs (μPD424400) in SOJ packages and 20 power supply decoupling capacitors for noise reduction. DQ_0 through DQ_{39} are common input/output pins.

Features

- 2,097,152-word by 40-bit organization
- Single +5-volt power supply
- Fast-page cycles
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

Pin Configuration

72-Pin SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{16}
4	DQ_1
5	DQ_{17}
6	DQ_2
7	DQ_{18}
8	DQ_3
9	DQ_{19}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	$\overline{OE}$
20	DQ_4
21	DQ_{20}
22	DQ_5
23	DQ_{21}
24	DQ_6
25	DQ_{22}
26	DQ_7
27	DQ_{23}
28	A_7
29	DQ_{36}
30	V_{CC}
31	A_8
32	A_9
33	NC
34	NC
35	DQ_{34}
36	DQ_{32}

Pin	Symbol
37	DQ_{33}
38	DQ_{35}
39	GND
40	$\overline{CAS}_0$
41	NC
42	NC
43	$\overline{CAS}_1$
44	$\overline{RAS}_0$
45	$\overline{RAS}_1$
46	DQ_{37}
47	$\overline{WE}$
48	GND
49	DQ_8
50	DQ_{24}
51	DQ_9
52	DQ_{25}
53	DQ_{10}
54	DQ_{26}

Pin	Symbol
55	DQ_{11}
56	DQ_{27}
57	DQ_{12}
58	DQ_{28}
59	V_{CC}
60	DQ_{29}
61	DQ_{13}
62	DQ_{30}
63	DQ_{14}
64	DQ_{31}
65	DQ_{15}
66	DQ_{38}
67	Note 1
68	Note 1
69	Note 1
70	Note 1
71	DQ_{39}
72	GND

Notes:

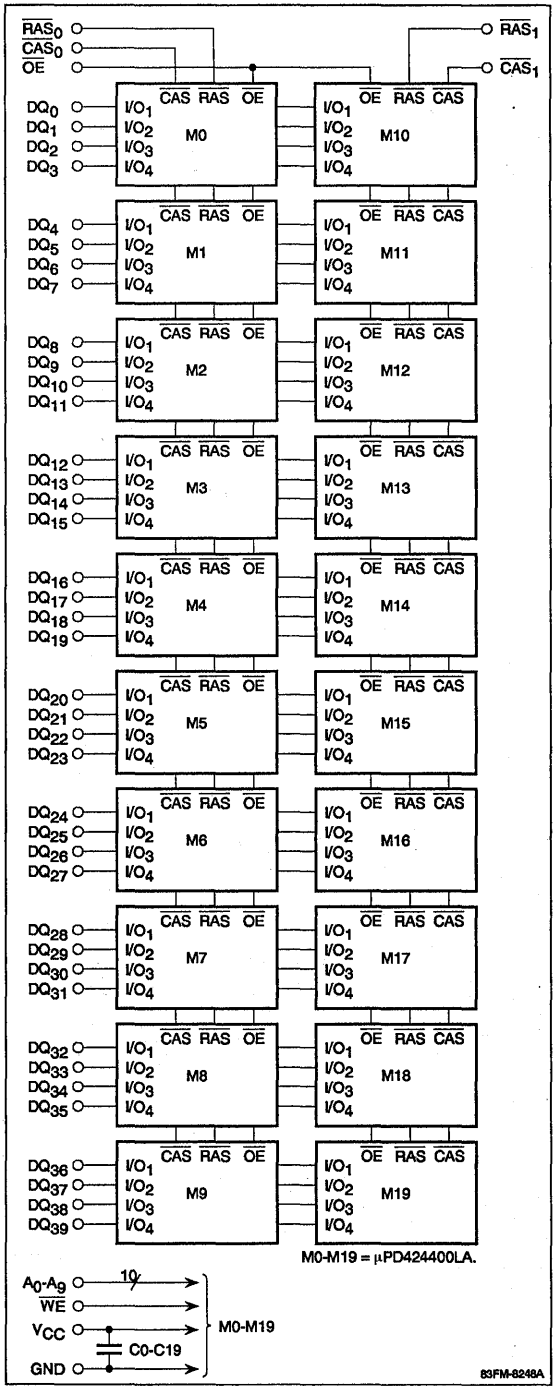
[1] Pins 67-70 are defined by access time:

Pin	70 ns	80 ns	100 ns
67	NC	NC	NC
68	NC	NC	NC
69	GND	NC	GND
70	NC	GND	GND

83FM-8247A

SIMM is a trademark of Wang Laboratories.

MC-422000AA40 Connection Diagram



Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_1$	Column address strobes
DQ_0 - DQ_{39}	Common data inputs/outputs
$\overline{OE}$	Output enable
$\overline{RAS}_0$ - $\overline{RAS}_1$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	20 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	110	pF	A_0 - A_9
	C_{I2}	130	pF	$\overline{WE}$, $\overline{OE}$
	C_{I3}	60	pF	$\overline{RAS}$
	C_{I4}	60	pF	$\overline{CAS}$
Input/output capacitance	C_{IO}/C_{OO}	20	pF	DQ_0 - DQ_{39}

Ordering Information

Part Number	Access Time (max)	Height (typ)	Thickness (typ)	Package	DRAMs
MC422000AA40B-70	70 ns	25.4 mm (1.000 inch)	9.3 mm (0.366 inch)	72-pin socket-mountable SIMM (solder plating)	Twenty μPD424400LA
B-80	80 ns				
MC422000AA40F-70	70 ns	25.4 mm (1.000 inch)	9.3 mm (0.366 inch)	72-pin socket-mountable SIMM (gold plating)	
F-80	80 ns				

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		40	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			20	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–200	200	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–20	20	μA	DQ_0 to DQ_{39} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

10h

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		1060		960	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1060		960	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		860		760	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1060		960	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		35		40	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		45	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	55		65		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		ns	(Notes 4, 7)

AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		45		ns	(Note 14)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		ns	
Data-in hold time	t_{DH}	15		15		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		20		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ delay data time	t_{OED}	15		20		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		ns	
$\overline{OE}$ to inactive setup time	t_{OES}	0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	20	ns	(Note 9)
Output buffer turnoff delay	t_{OFF}	0	15	0	20	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		ns	(Notes 6, 7)
Fast-page cycle time	t_{PC}	45		50		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		70		80	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	40	ns	(Note 8)
Row address hold time	t_{RAH}	10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	70	125,000	80	125,000	ns	
Random read or write cycle time	t_{RC}	140		160		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	60		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Read-write cycle time	t_{RWC}	185		210		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	90		105		ns	(Note 14)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		ns	(Note 14)
$\overline{WE}$ hold time	t_{WHR}	15		15		ns	
Write command pulse width	t_{WP}	15		15		ns	(Note 12)
$\overline{WE}$ setup time	t_{WSR}	10		10		ns	

10h

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max), and if $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

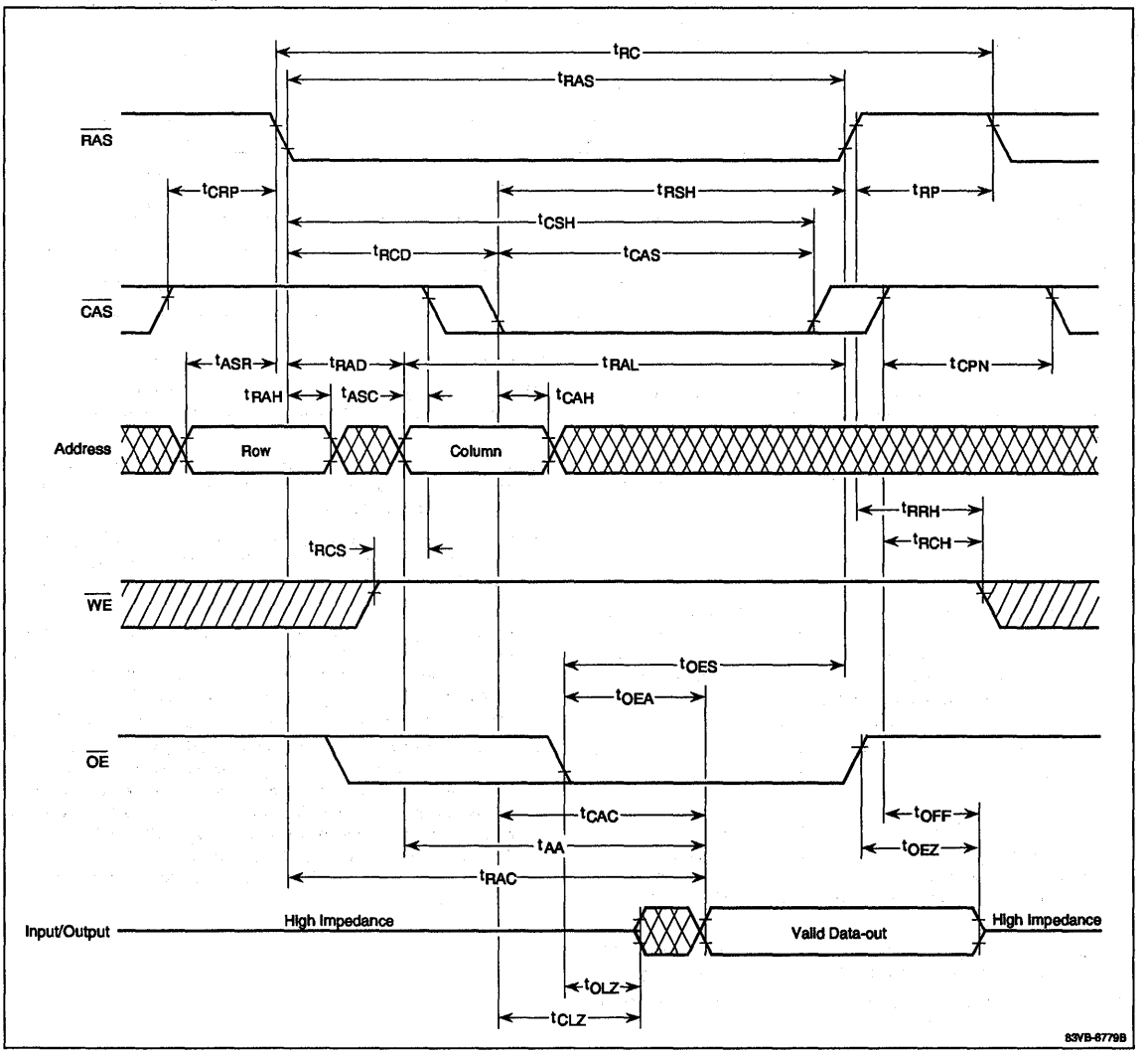
(14) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle.

If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

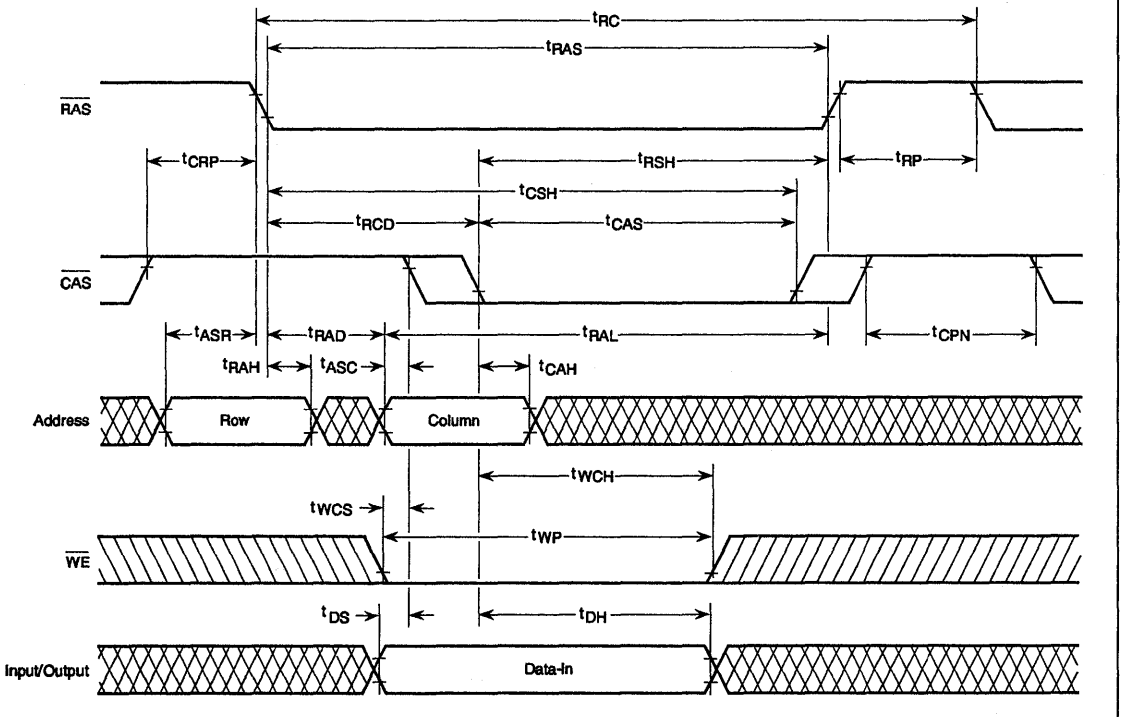
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle

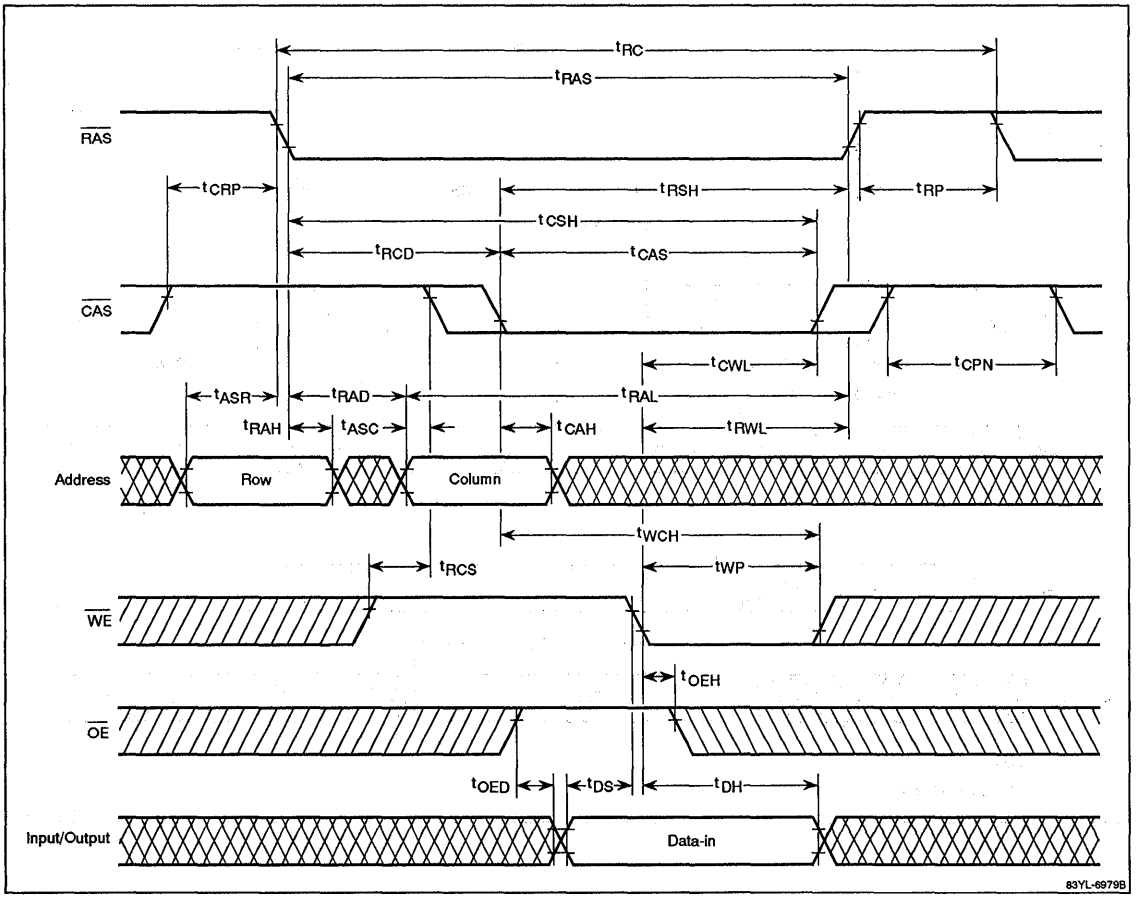


Note:
[1] $\overline{OE}$ = don't care.

83YL-6978B

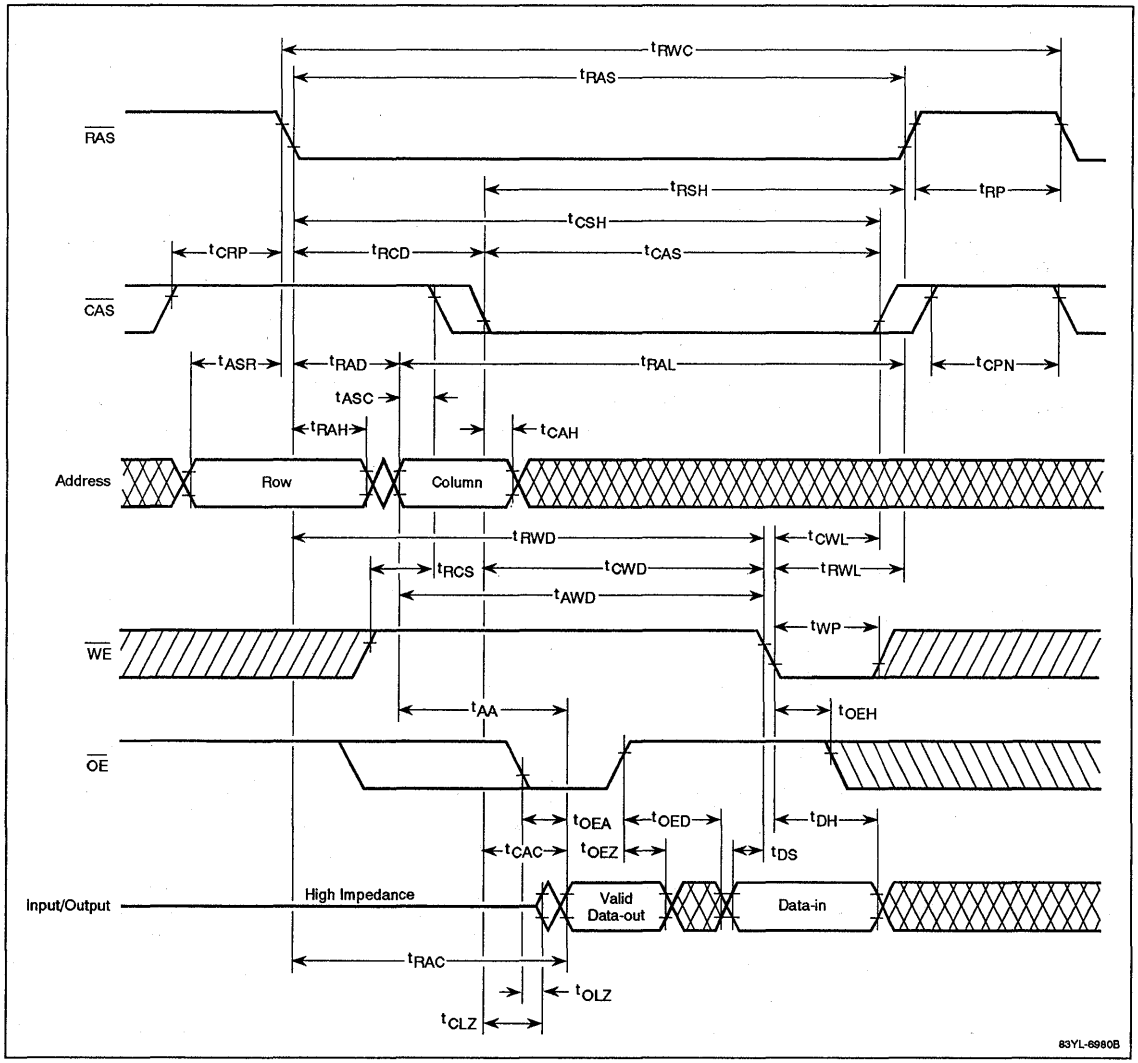
Timing Waveforms (cont)

Late Write Cycle



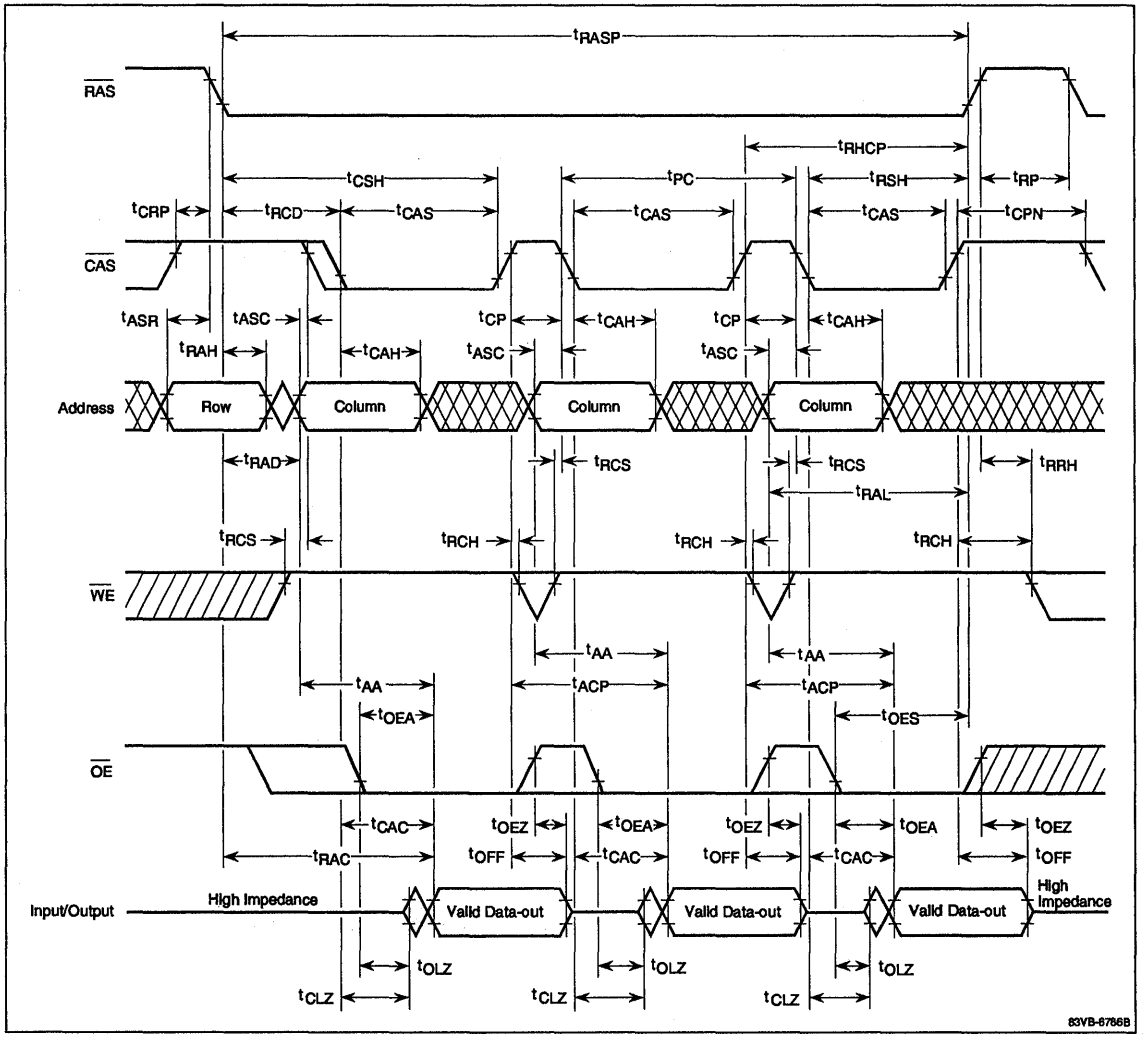
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



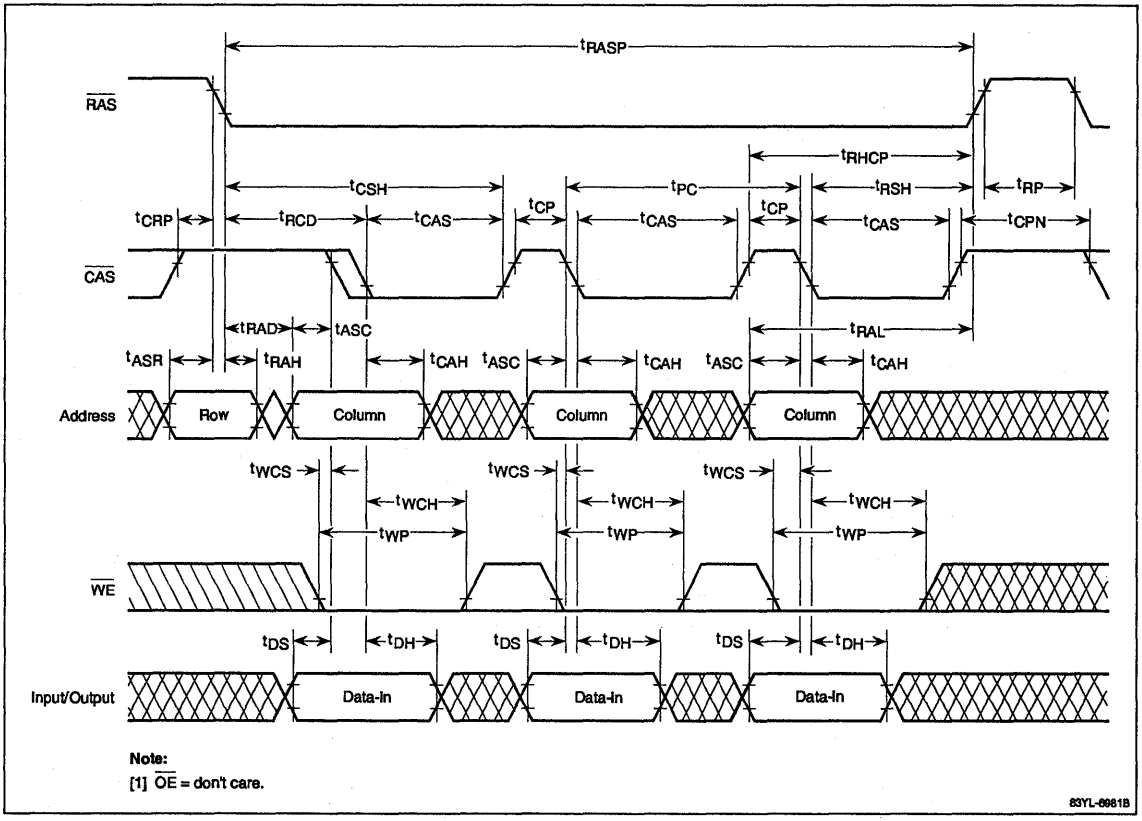
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



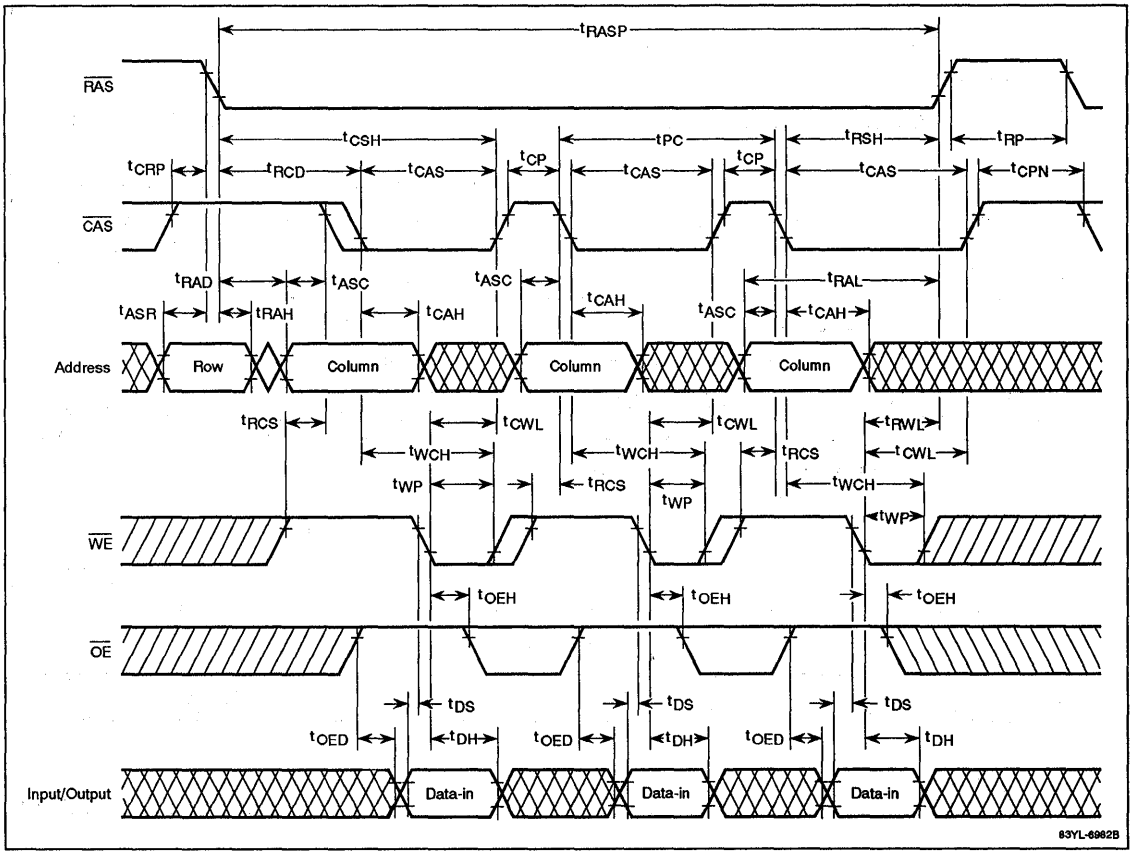
Note:
[1] $\overline{OE}$ = don't care.

83YL-6981B

10h

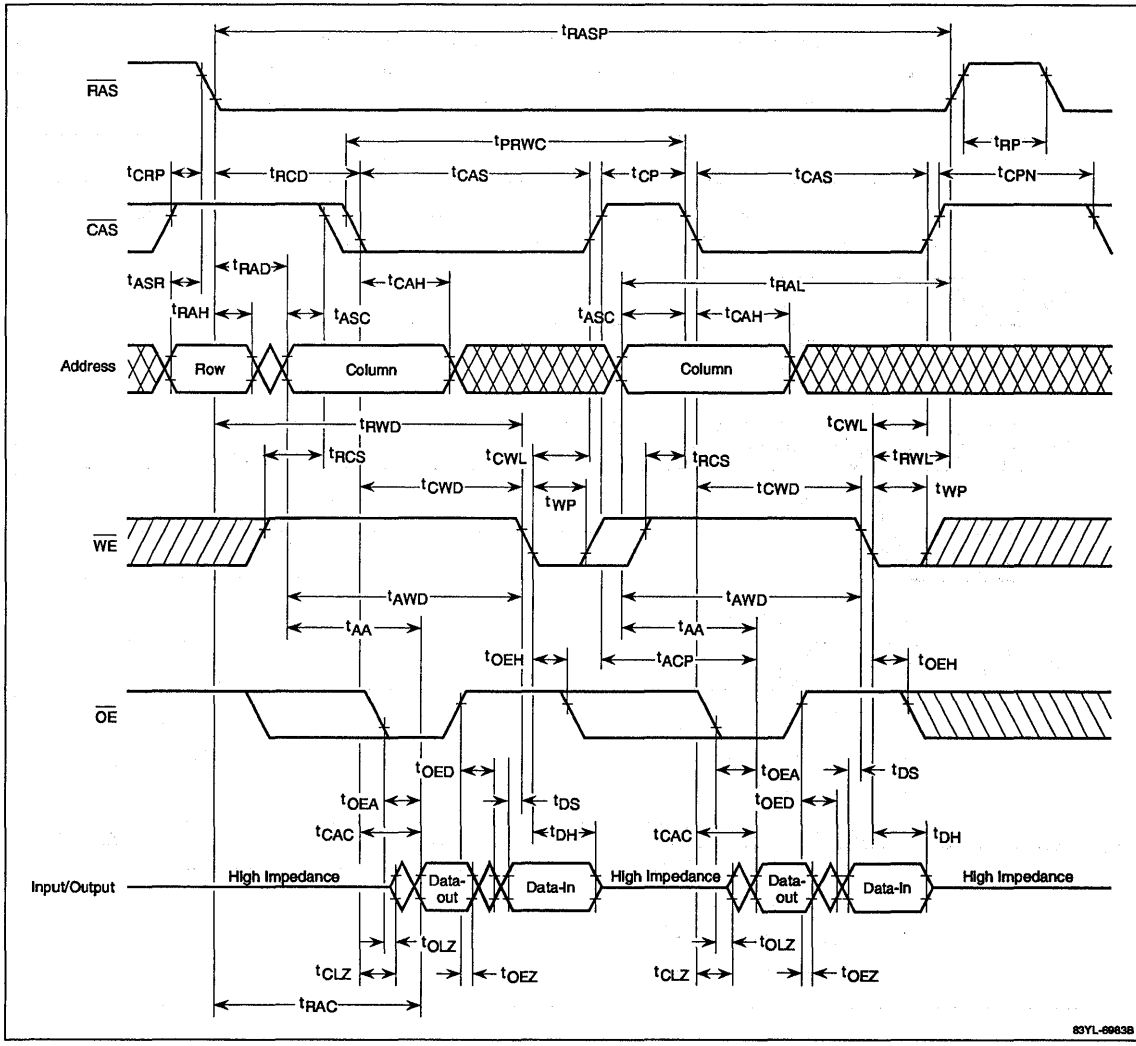
Timing Waveforms (cont)

Fast-Page Late Write Cycle



Timing Waveforms (cont)

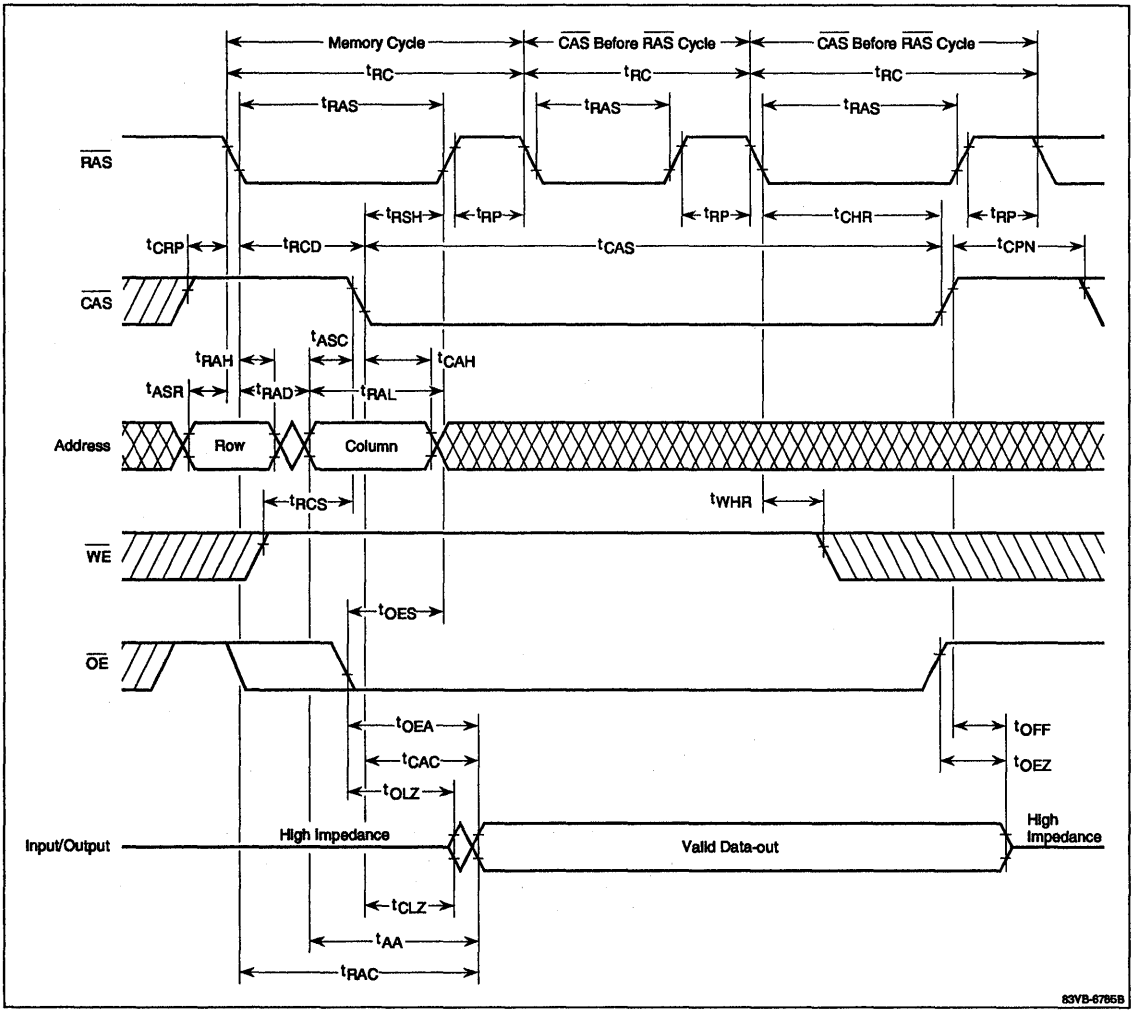
Fast-Page Read-Write/Read-Modify-Write Cycle



10h

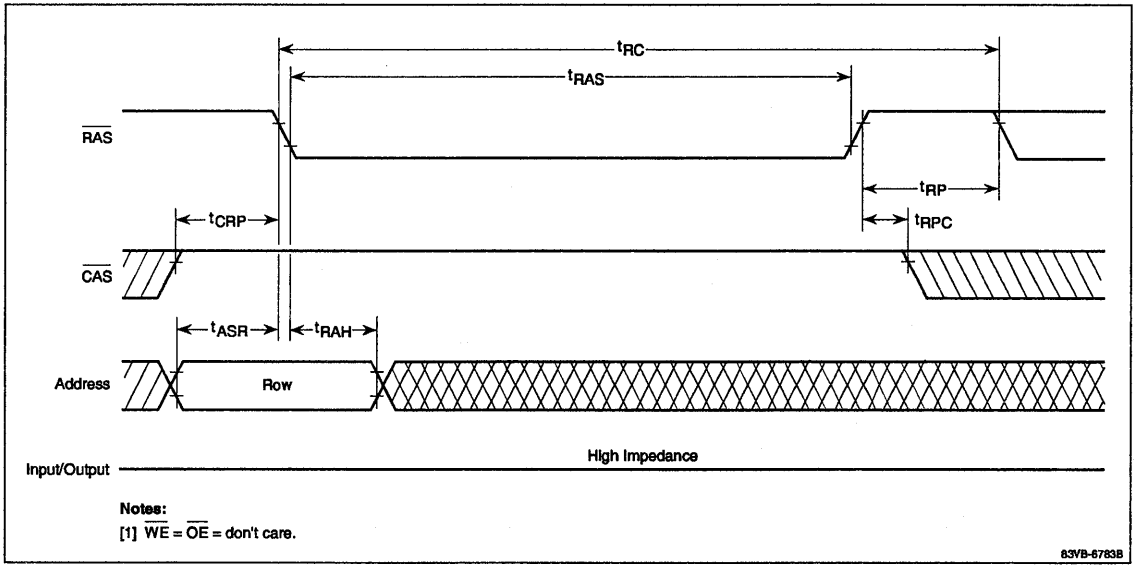
Timing Waveforms (cont)

Hidden Refresh Cycle

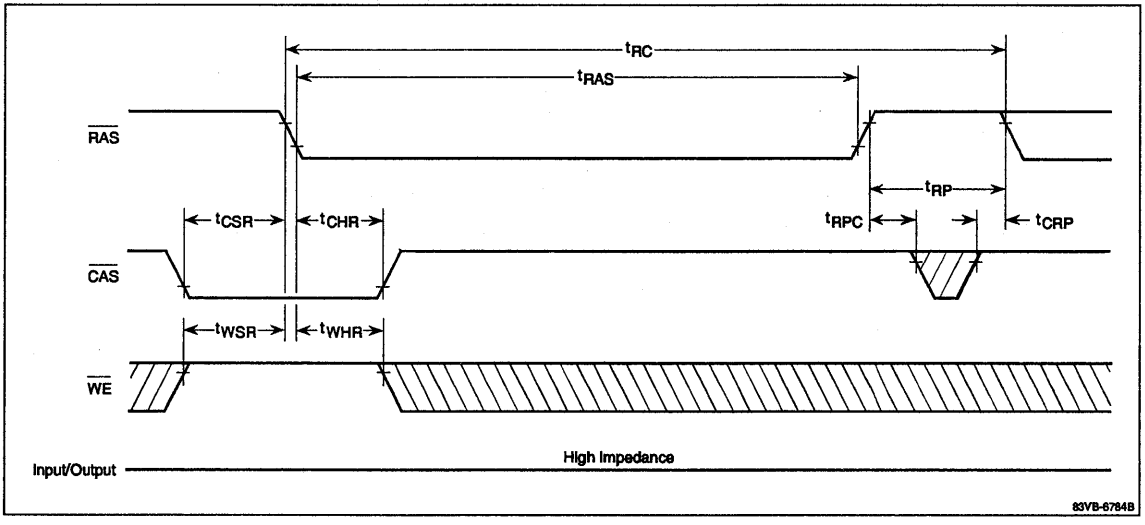


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

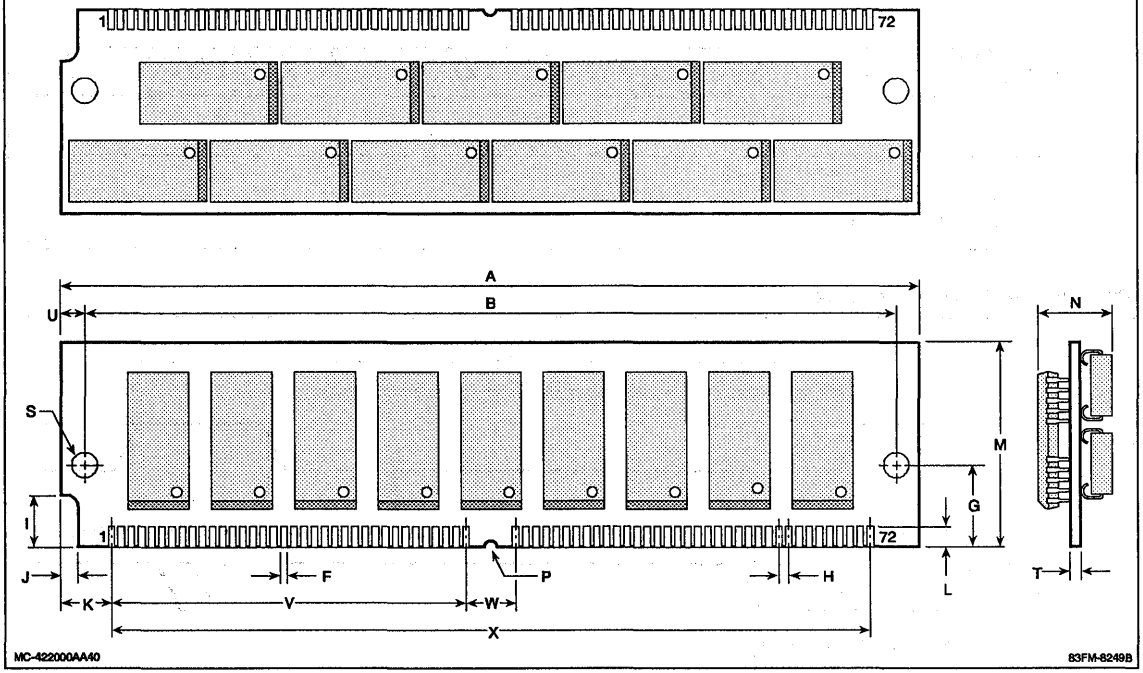


Package Drawing

72-Pin Socket-Mountable SIMM

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	25.4	1.000
N	9.3	.366
P	1.57 rad	.062 rad
S	3.18 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



NEC

Section 11
DRAM Modules (4M/8M x n)

MC	Organization	Features	
-424000A8	4M x 8	Fast-page	11a
-424000A9	4M x 9	Fast-page	11b
-424000A32	4M x 32	Fast-page	11c
-424000A36	4M x 36	Fast-page	11d
-428000A32	8M x 32	Fast-page	11e
-428000A36	8M x 36	Fast-page	11f

Upcoming Products

Description	Device Number	Comments
4M x 8 DRAM Module	MC-424000A8B B/FB	Uses 16M devices
4M x 9 DRAM Module	MC-424000A9B B/FB	Uses 16M devices
16M x 8 DRAM Module	MC-4216000A8BH/FA/AA	Uses 16M devices
16M x 9 DRAM Module	MC-4216000A9BH/FA/AA	Uses 16M devices
4M x 40 DRAM Module	MC-424000AA40BH/FH	Uses 16M devices
8M x 40 DRAM Module	MC-428000AA40BH/FH	Uses 16M devices

NEC Electronics Inc.

MC-424000A8
4,194,304 x 8-Bit
Dynamic CMOS RAM Module

Description

The MC-424000A8 is a fast-page 4,194,304-word by 8-bit dynamic RAM module designed to operate from a single +5-volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

Each module is functionally equivalent to eight standard 4M x 1 DRAMs. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 1024 address combinations of A_0 - A_9 during a 16-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. The SIMM includes eight μPD424100 DRAMs in SOJ packages and eight power supply decoupling capacitors.

Features

- 4,194,304-word by 8-bit organization
- Single +5-volt power supply
- Standard 30-pin Single Inline Memory Module (SIMM) packaging
- Eight μPD424100 4M x 1 DRAMs in high-density SOJ packaging
- Eight power supply decoupling capacitors
- Low power dissipation: 44 mW standby (max)
- TTL-compatible inputs and outputs
- 1024 refresh cycles every 16 ms
- Fast-page capability

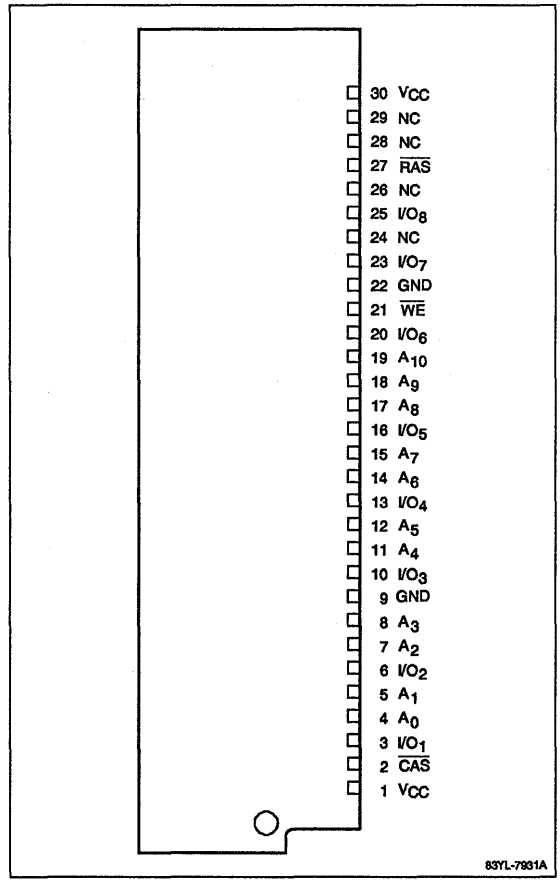
Pin Identification

Name	Function
A_0 - A_{10}	Address inputs
$\overline{CAS}$	Column address strobe
I/O_1 - I/O_8	Common data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

SIMM is a trademark of Wang Laboratories.

Pin Configuration

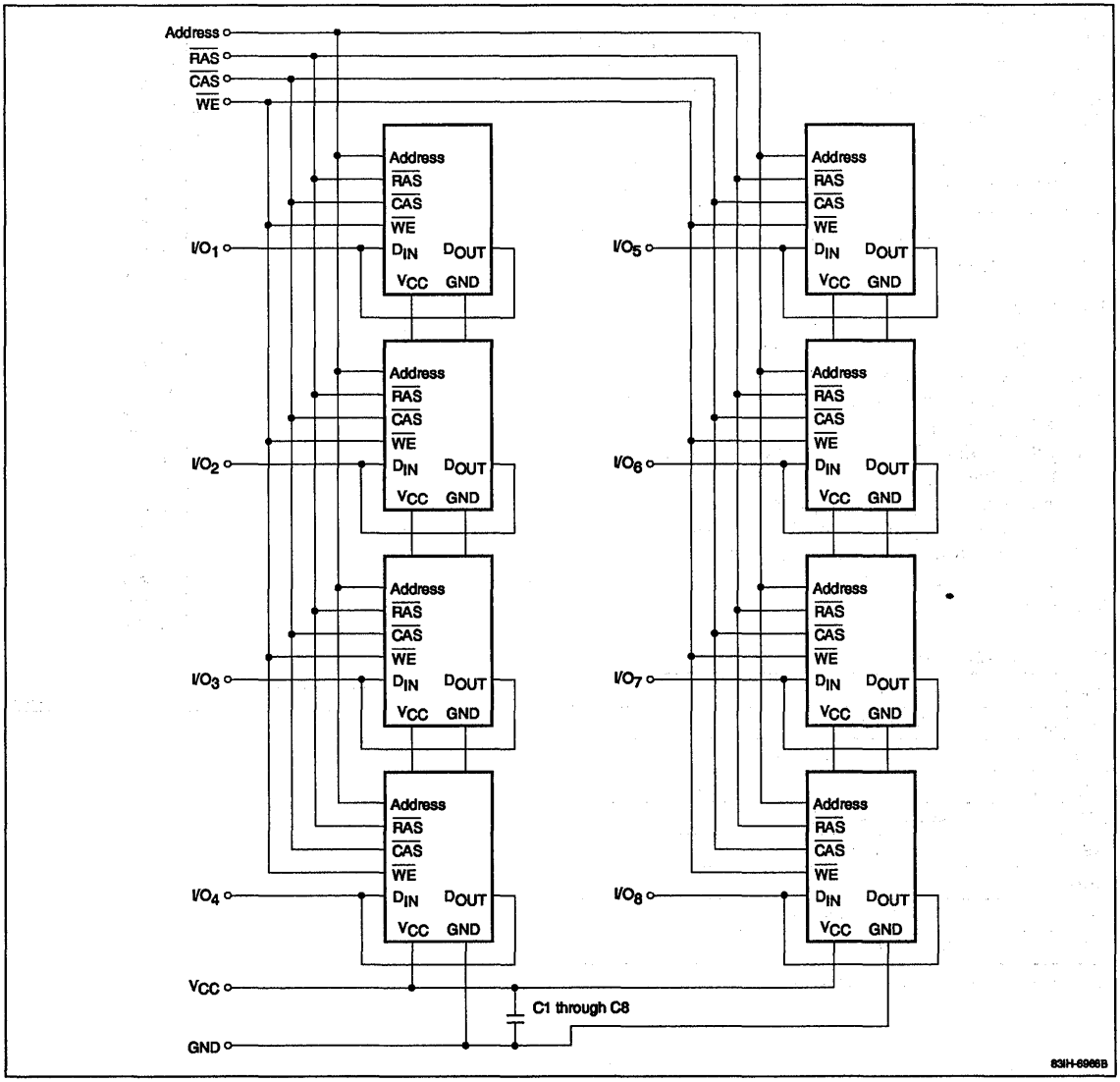
30-Pin Socket-Mountable SIMM



Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-424000A8BA-60	60 ns	30-pin socket-mountable SIMM (solder plating)	20.3 mm (0.799 inch)	5.08 mm (0.200 inch)	Eight μPD424100LA
BA-70	70 ns				
BA-80	80 ns				
MC-424000A8FA-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
FA-70	70 ns				
FA-80	80 ns				

Connection Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		+70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	60	pF	Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Input/output capacitance	C_{IO}	15	pF	I/O_1 through I/O_8

11a

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		16	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			8	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−80	80	μA	For addresses, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$: V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		960		800		720	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		960		800		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		720		640		560	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		960		800		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		ns	(Note 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	ns	(Note 10)
Fast-page cycle time	t_{PC}	40		45		50		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		ns	
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)
$\overline{WE}$ setup time	t_{WSR}	10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

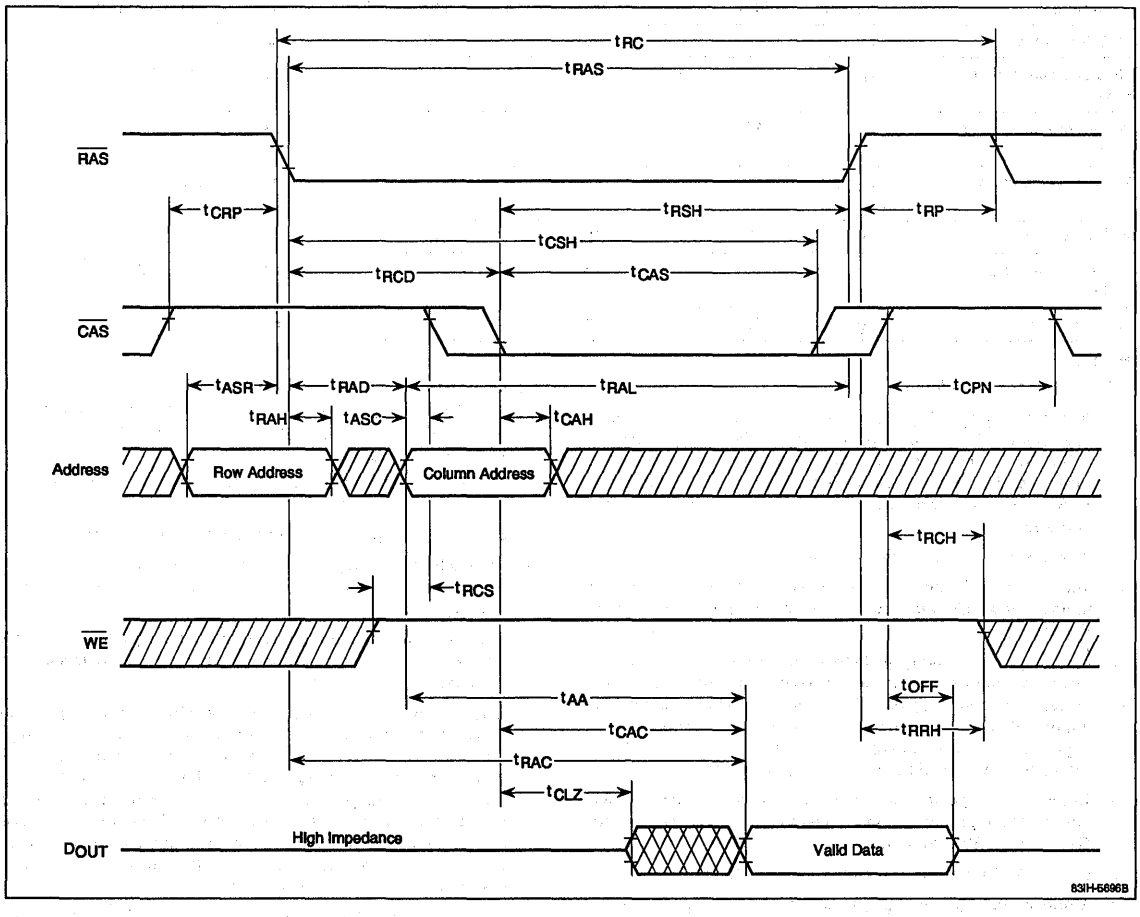
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

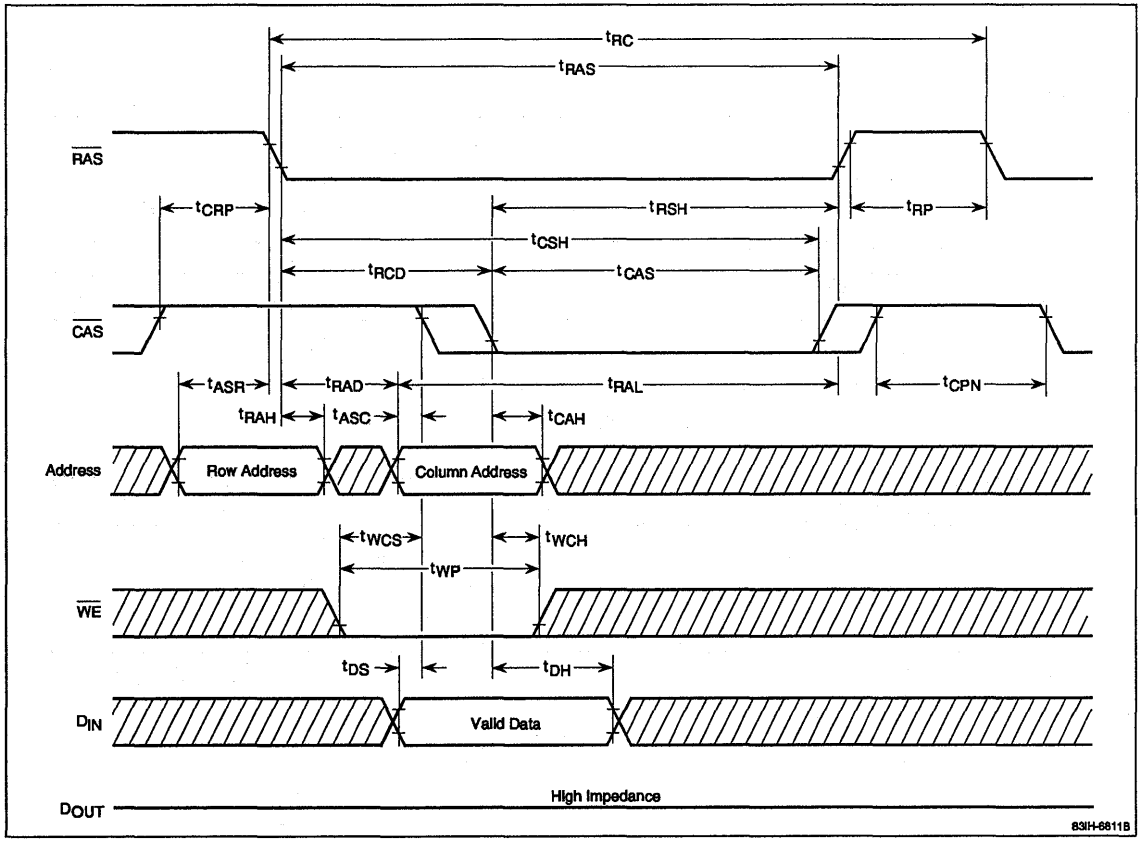
Timing Waveforms

Read Cycle



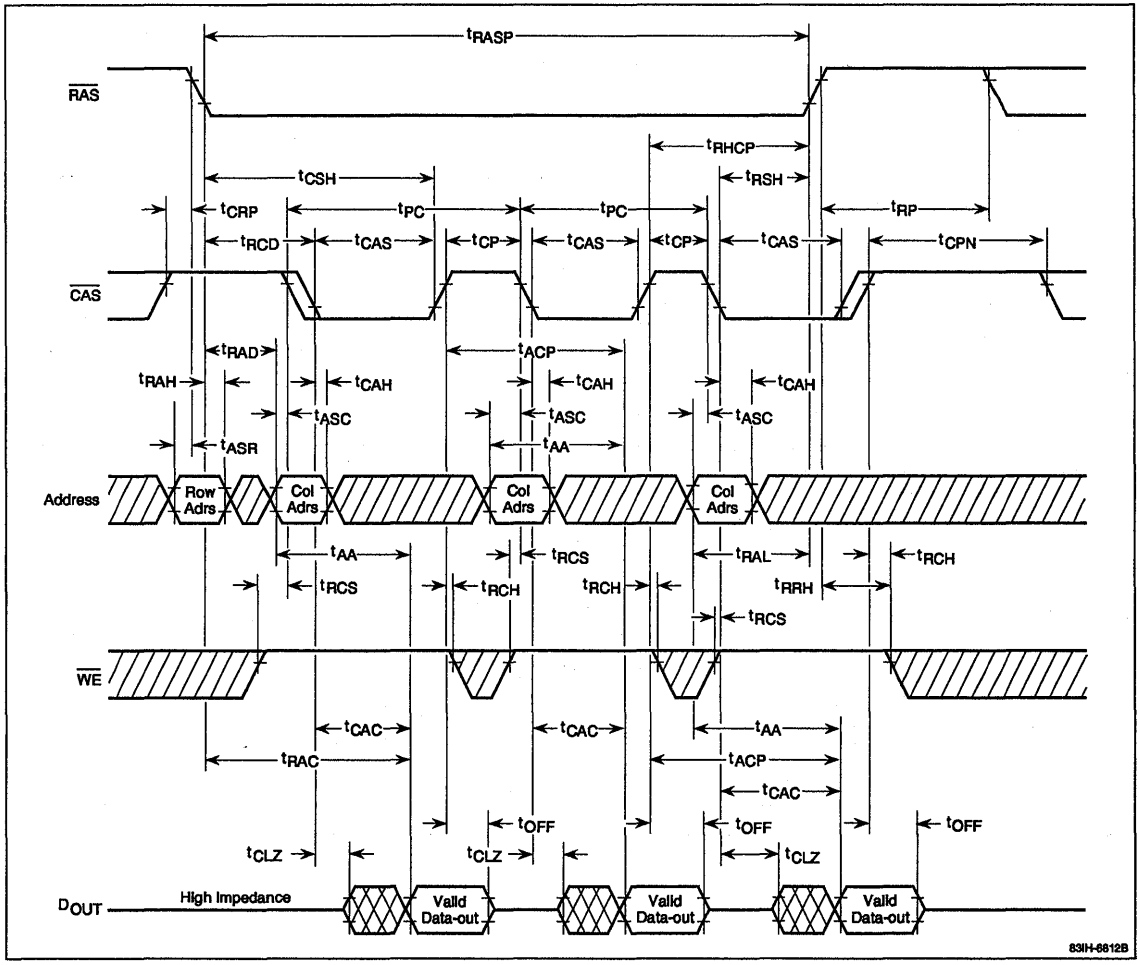
Timing Waveforms (cont)

Early Write Cycle



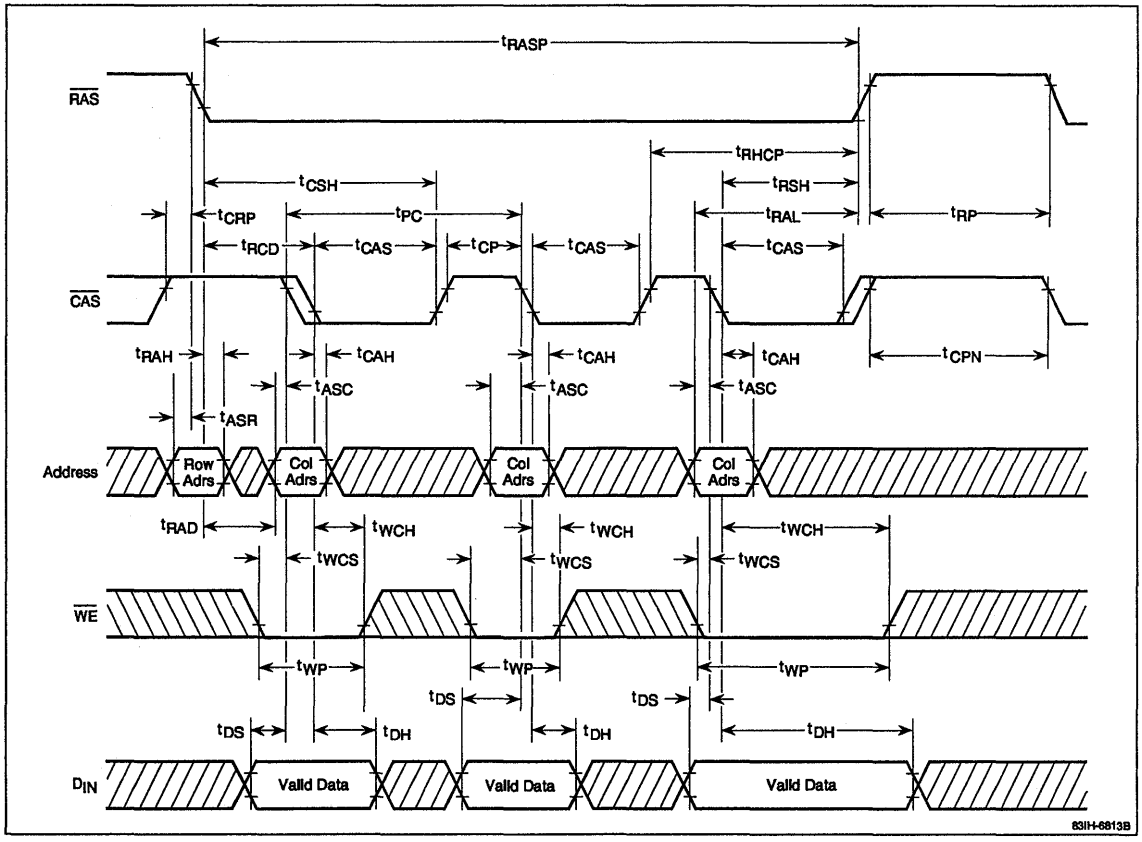
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

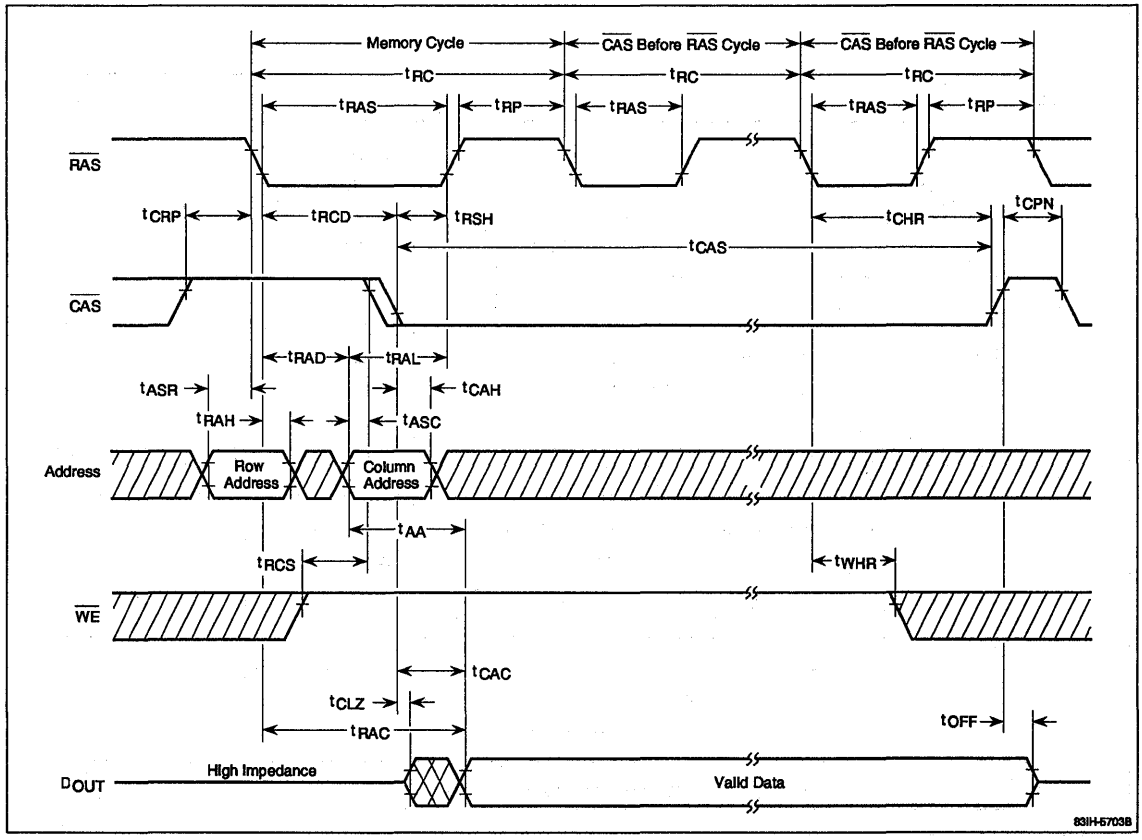
Fast-Page Early Write Cycle



11a

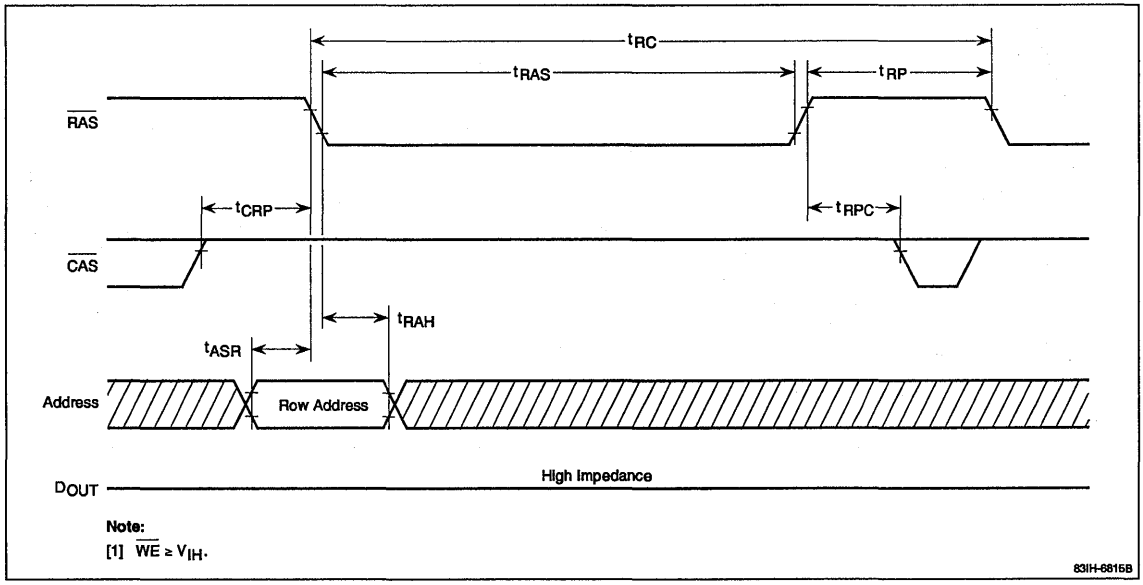
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

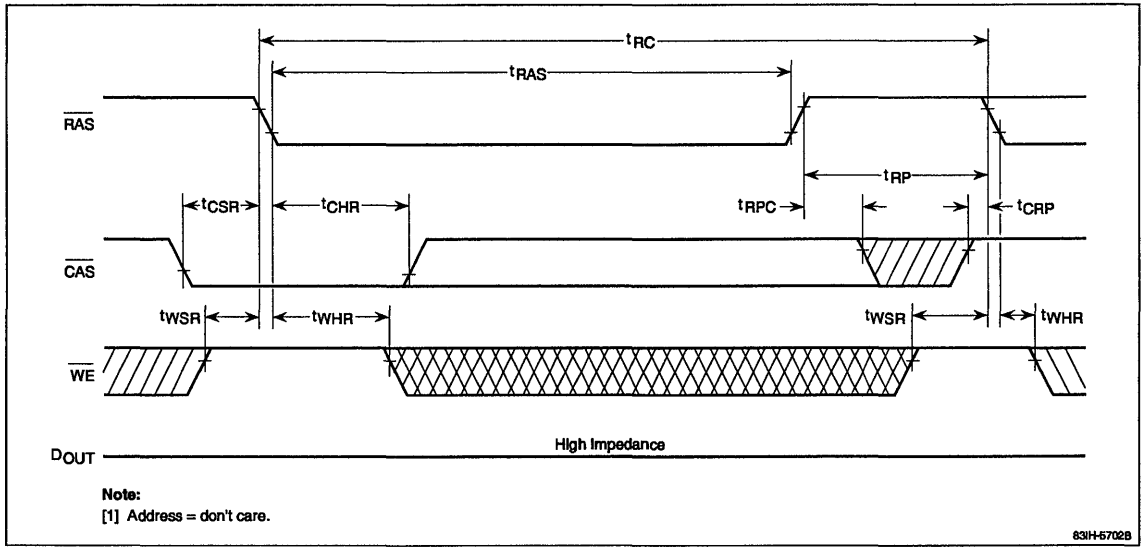
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

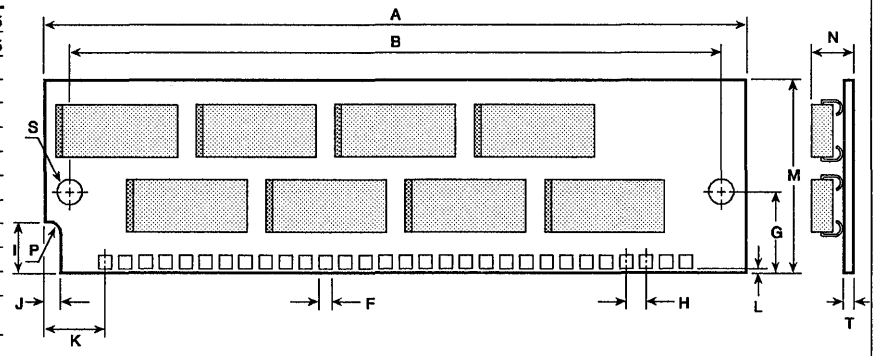
83IH-5702B

11a

Package Drawings

30-Pin Socket-Mountable SIMM (MC-424000A8: Suffix BA or FA)

Item	Millimeters	Inches
A	88.9 ± 0.13	3.500 ± .005
B	82.14 ± 0.13	3.234 ± .005
F	1.78	.070
G	10.16 ± 0.13	.400 ± .005
H	2.54	.100
I	6.35 ± 0.13	.250 ± .005
J	2.03 ± 0.13	.080 ± .005
K	7.62 ± 0.13	.300 ± .005
L	0.25 max	.010 max
M	20.3	.799
N	5.08	.200
P	1.57 rad	.062 rad
S	3.18 ± 0.13 dia	.125 ± .005 dia
T	1.27 $^{+0.10}_{-0.08}$	.050 $^{+.004}_{-.003}$



MC-424000A8BA/FA

83CL-8833B (7/92)

MC-424000A9, -424100A9
4,194,304 x 9-Bit
Dynamic CMOS RAM Module

Description

The MC-424000A9 and the MC-424100A9 are fast-page 4,194,304-word by 9-bit dynamic RAM modules designed to operate from a single +5-volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, multiplexed address buffers, and flexible refresh controls, provides good system operating margins.

The modules are functionally equivalent to eight μPD424100 standard 4M DRAMs plus a parity bit. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 1024 address combinations of A_0 - A_9 during a 16-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight, and cost of a system. The SIMM includes nine μPD424100 DRAMs in SOJ packages and nine power supply decoupling capacitors.

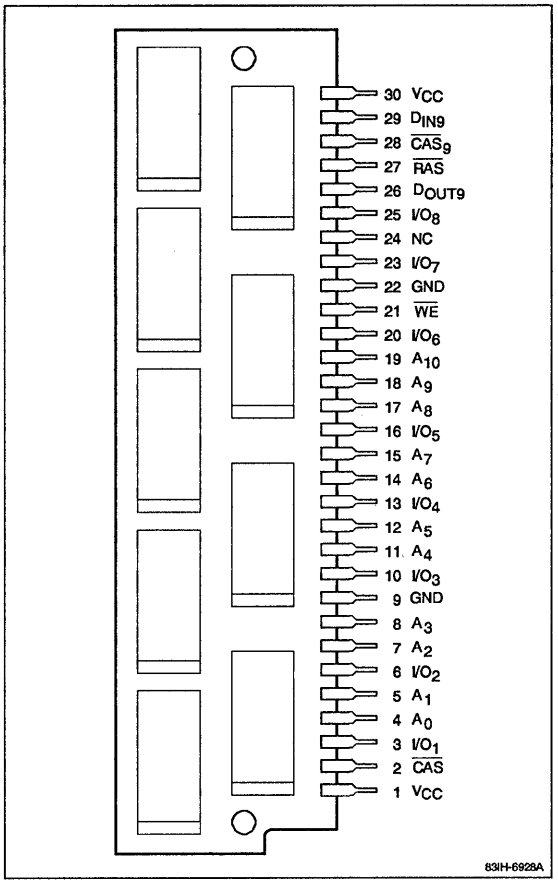
SIMM is a trademark of Wang Laboratories.

Features

- 4,194,304-word by 9-bit organization
- Single +5-volt power supply
- Standard 30-pin SIMM packaging
- Nine 4M dynamic RAMs incorporated in high-density SOJ packaging (μPD424100)
- Nine power supply decoupling capacitors
- Low power dissipation of 49.5 mW standby (max)
- TTL-compatible inputs and outputs
- 1024 refresh cycles every 16 ms
- Fast-page capability

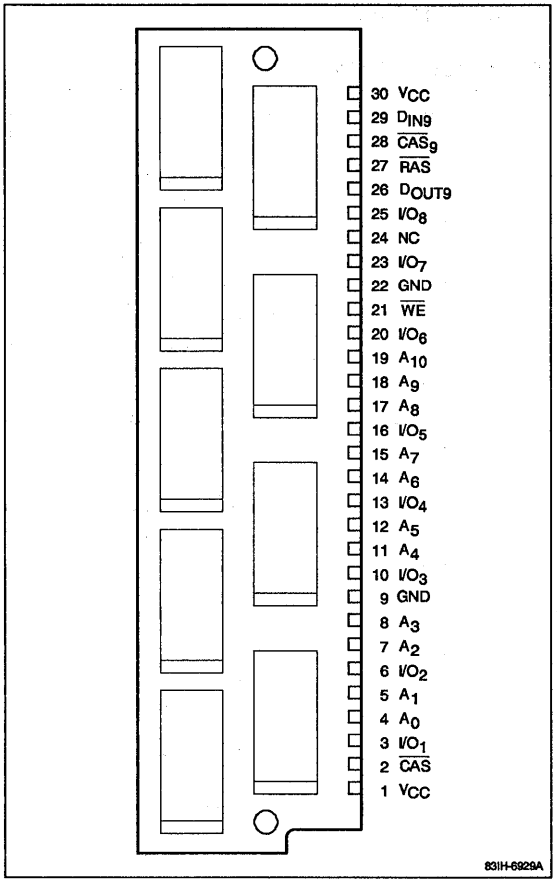
Pin Configurations

30-Pin Leaded SIMM



Pin Configurations (cont)

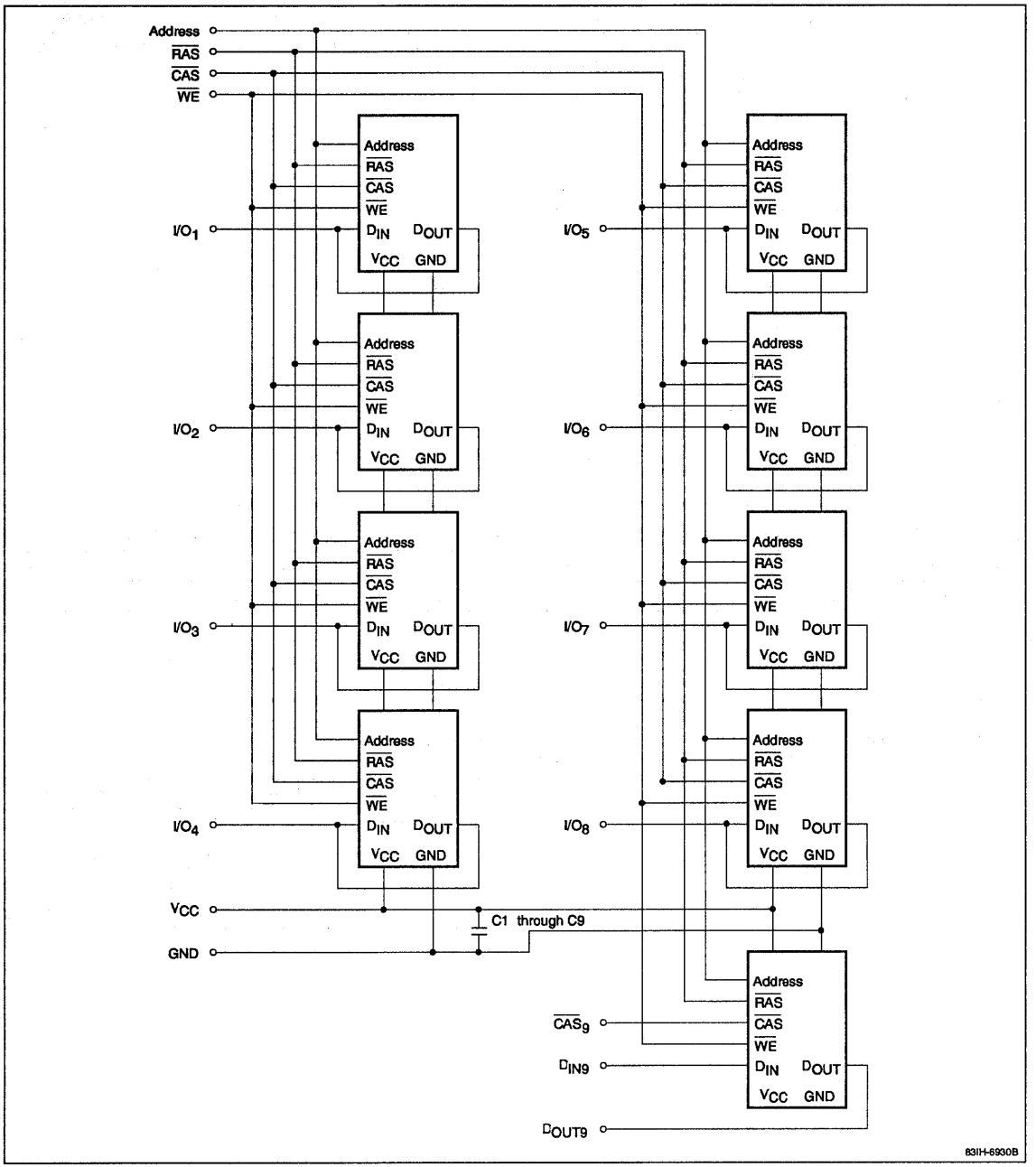
30-Pin Socket-Mountable SIMM



Pin Identification

Symbol	Function
A_0 - A_{10}	Address inputs
$\overline{CAS}$	Column address strobe
$\overline{CAS}_9$	Column address strobe for data output 9
D_{IN9}	Data input 9
D_{OUT9}	Data output 9
I/O_1 - I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Connection Diagram



Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-424000A9AA-60	60 ns	30-pin leaded SIMM (solder plating)	20.3 mm (.799 inch)	5.08 mm (.200 inch)	Nine μPD424100LA
AA-70	70 ns				
AA-80	80 ns				
AA-10	100 ns				
MC-424000A9BA60	60 ns	30-pin socket-mountable SIMM (solder plating)			
BA-70	70 ns				
BA-80	80 ns				
BA-10	100 ns				
MC-424100A9A-60	60 ns	30-pin leaded SIMM (solder plating)	24.03 mm (.946 inch)	5.28 mm (.208 inch)	Nine μPD424100LB
A-70	70 ns				
A-80	80 ns				
A-10	100 ns				
MC-424100A9B-60	60 ns	30-pin socket-mountable SIMM (solder plating)			
B-70	70 ns				
B-80	80 ns				
B-10	100 ns				

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	9.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	70	pF	Address, D_{IN}
	C_{I2}	7	pf	$\overline{CAS}_9$, D_{IN9}
Input/output capacitance	C_D	10	pF	D_{OUT9}
	C_{IO}	15	pF	I/O_1 through I/O_8

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		18	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			9	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–90	90	μA	For addresses, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$: V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
		–10	10	μA	For $\overline{CAS}_9$ and D_{IN9}: V_{IN} = 0 to 5.5 V; all other pins = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		1080		900		810		720	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1080		900		810		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		810		720		630		540	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		990		900		810		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		40		50		ns	(Notes 16, 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		20		15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		15		20		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		0		ns	(Note 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		10		ns	

AC Characteristics (cont)

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		25		20		25		ns	(Notes 16, 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		15		20		ns	(Note 18)
Data-in hold time	t_{DH}	15		20		15		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	80		95		80		95		ns	(Notes 6, 18)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 through A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		25		20		25		ns	
Read-write cycle time	t_{RWC}	145		165		185		220		ns	(Notes 6, 18)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Notes 16, 18)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		20		25		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		20		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		20		15		20		ns	
Write command pulse width	t_{WP}	15		20		15		20		ns	(Note 14)
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

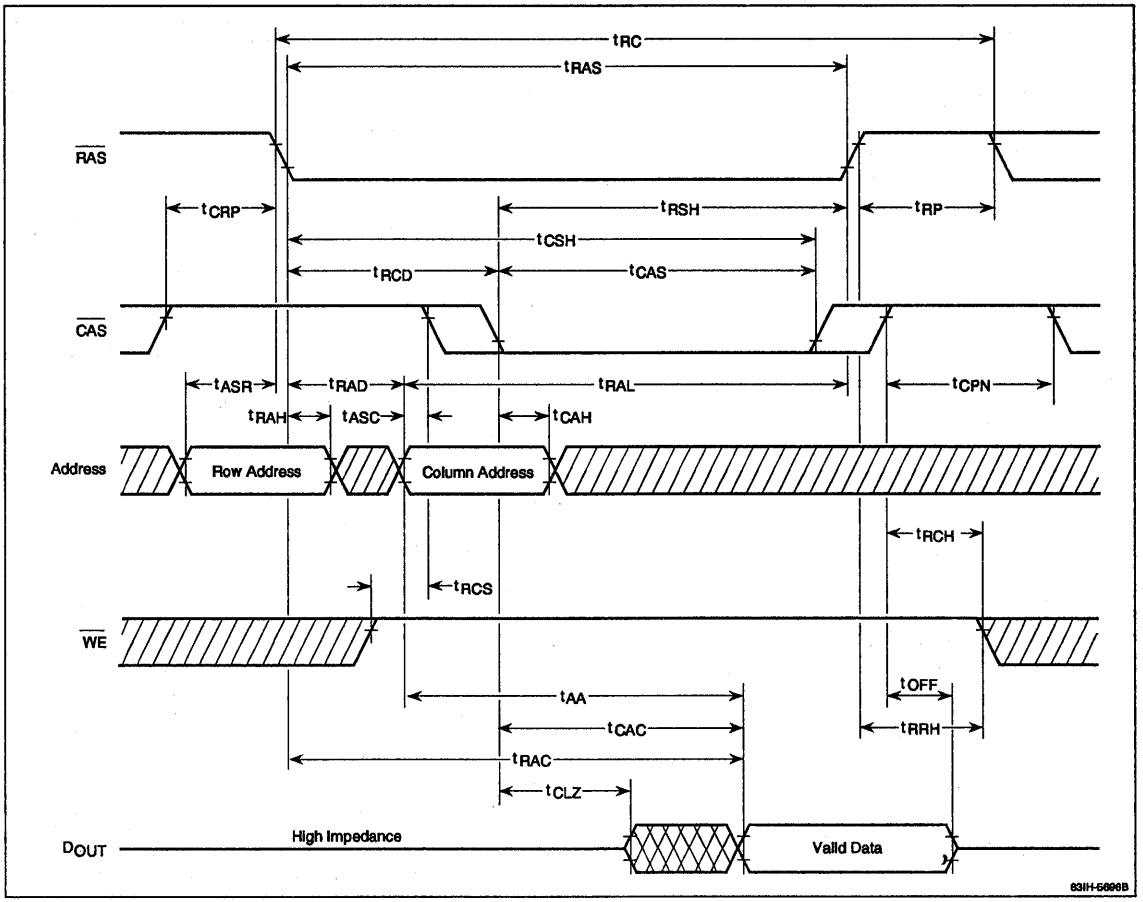
(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

(18) Read-write/read-modify-write cycles can be executed only by $\overline{CAS}_9$, D_{IN9} and D_{OUT9} because of the separate data input and output pins. See block diagram.

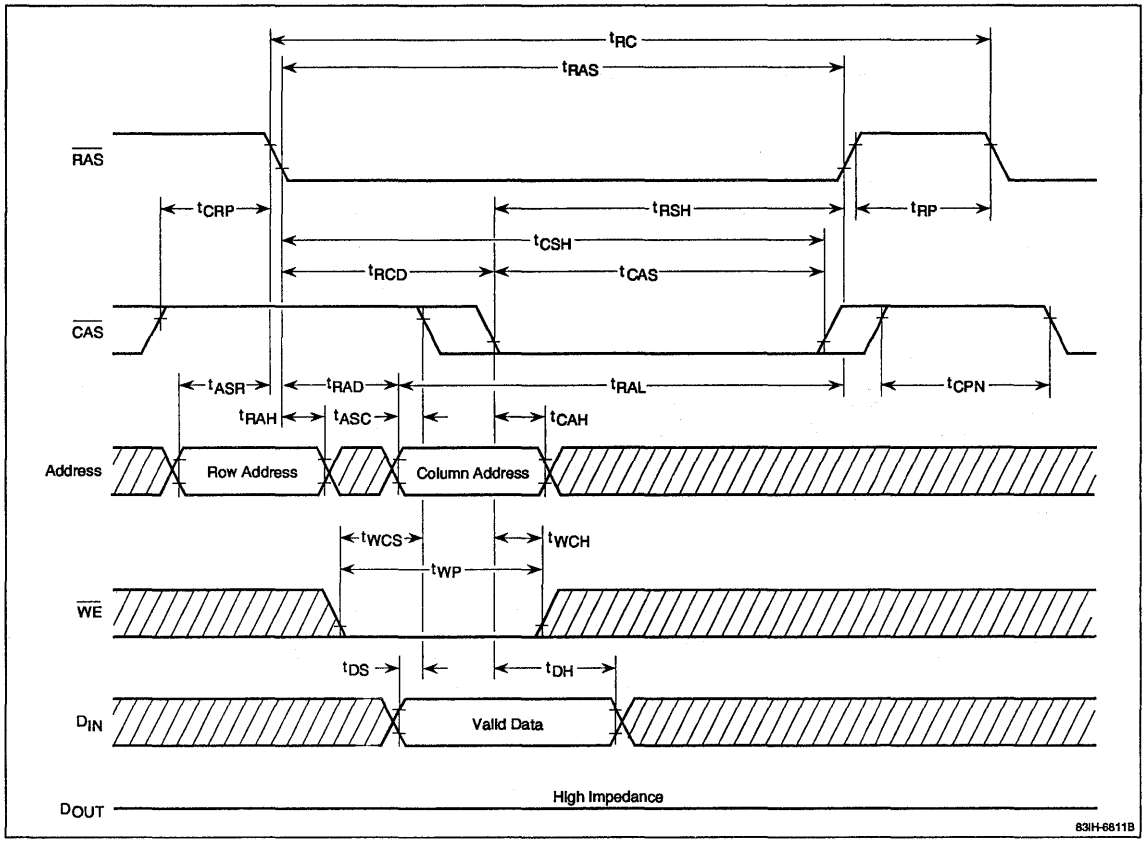
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



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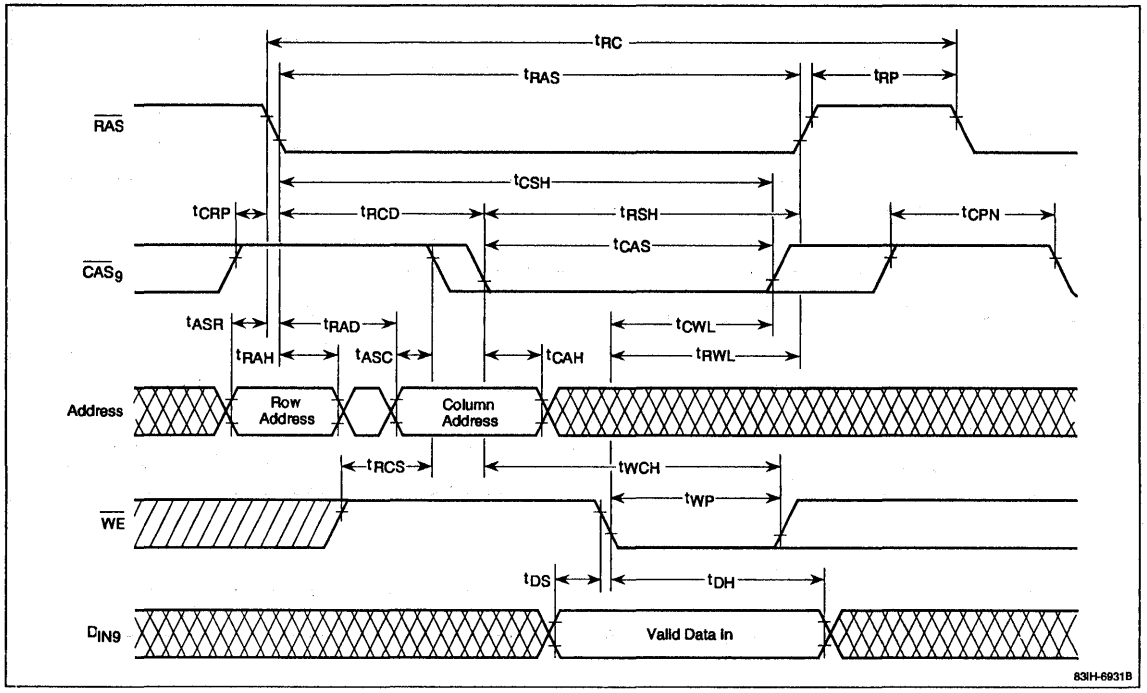
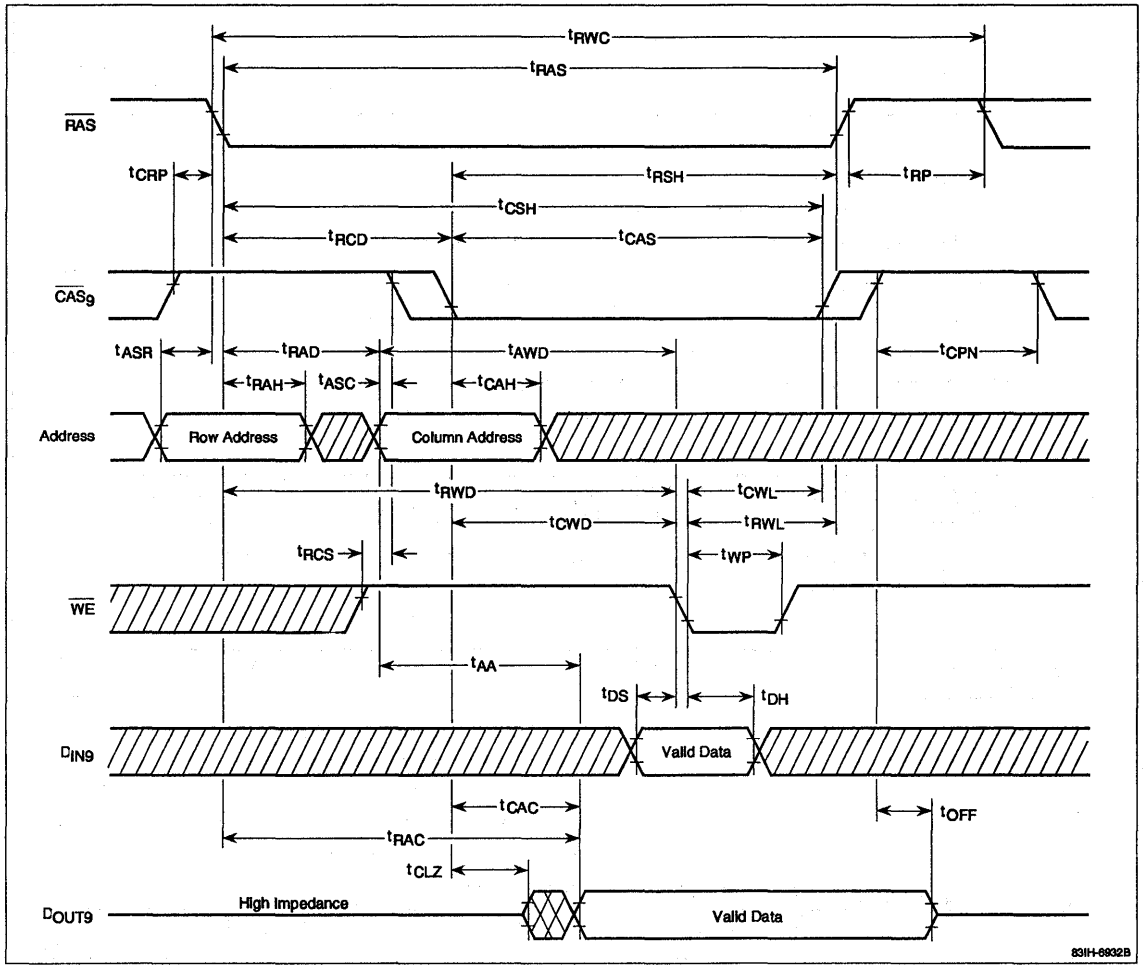
Timing Waveforms (cont)

Late Write Cycle (D_{IN9}, D_{OUT9}, and $\overline{CAS}_9$ Only)



Timing Waveforms (cont)

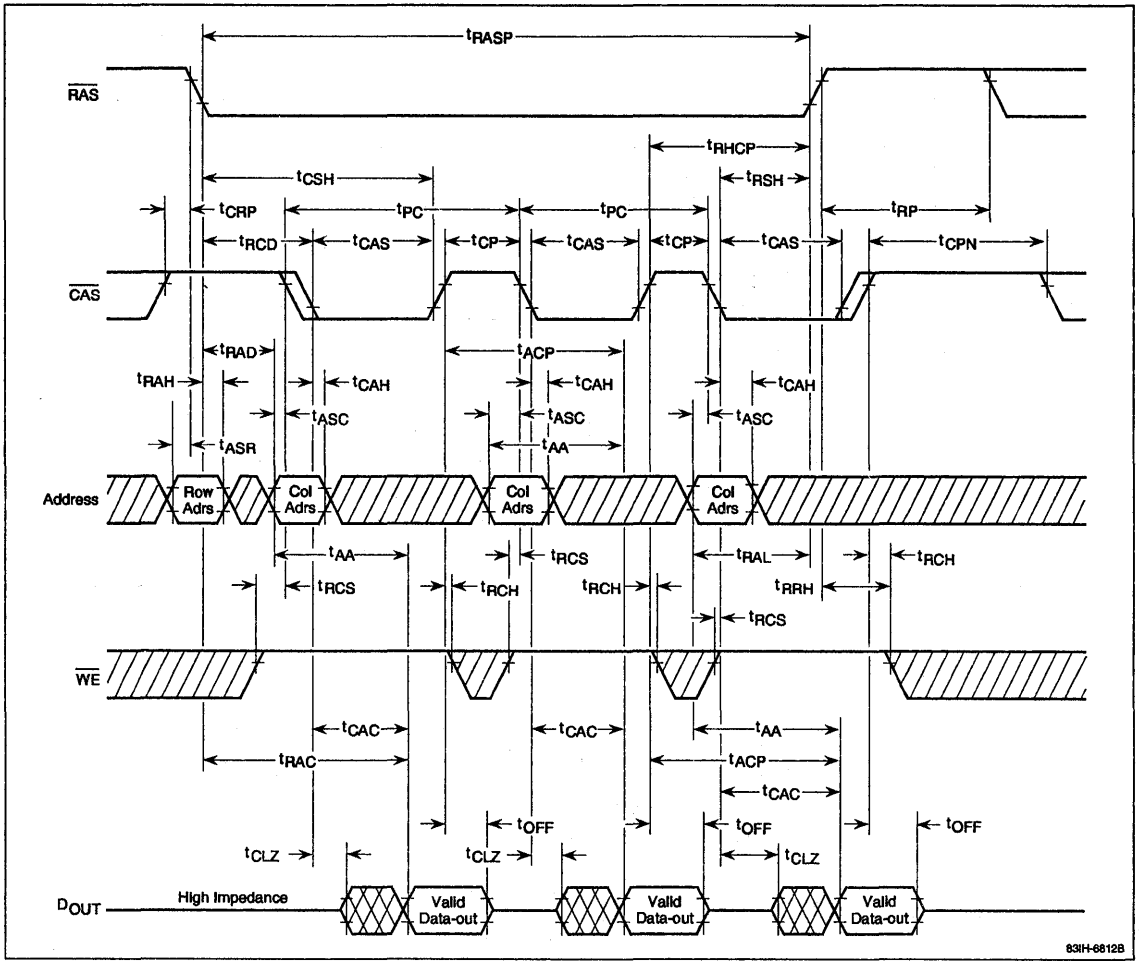
Read-Write/Read-Modify-Write Cycle (D_{IN9}, D_{OUT9}, and $\overline{CAS}_9$ Only)



11b

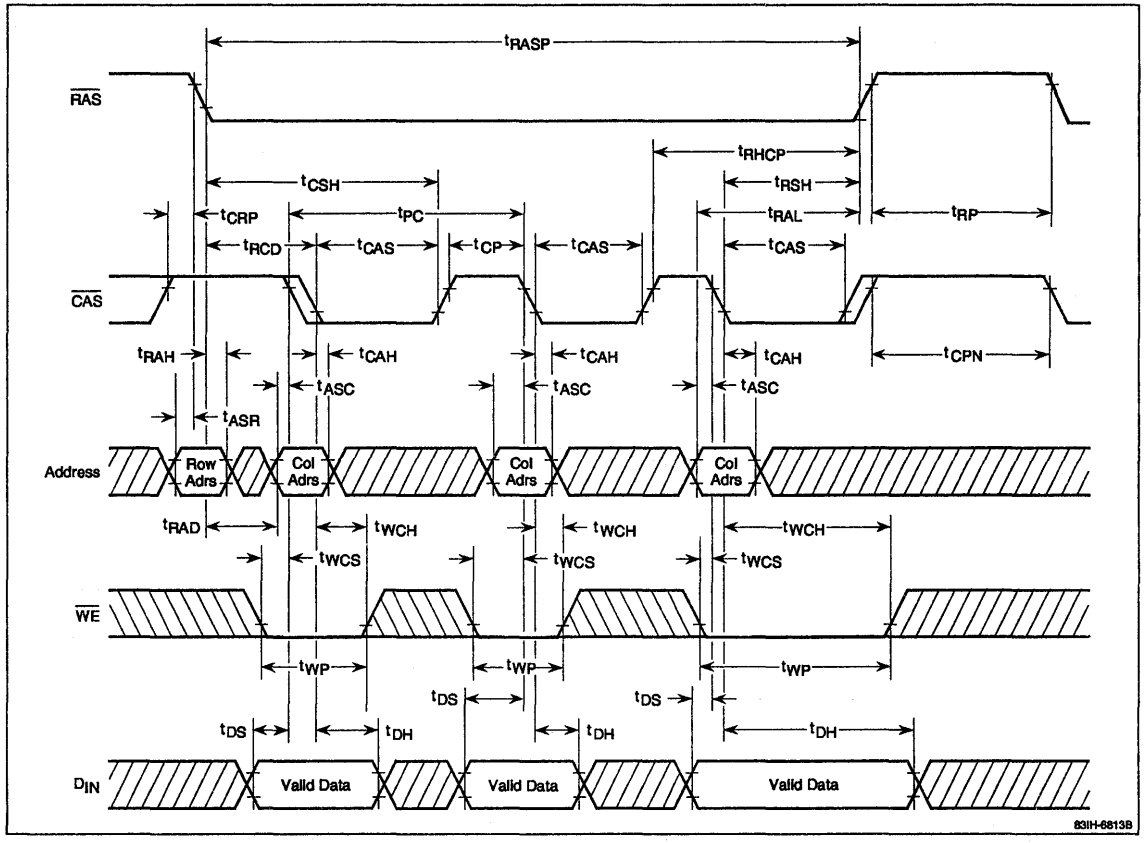
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

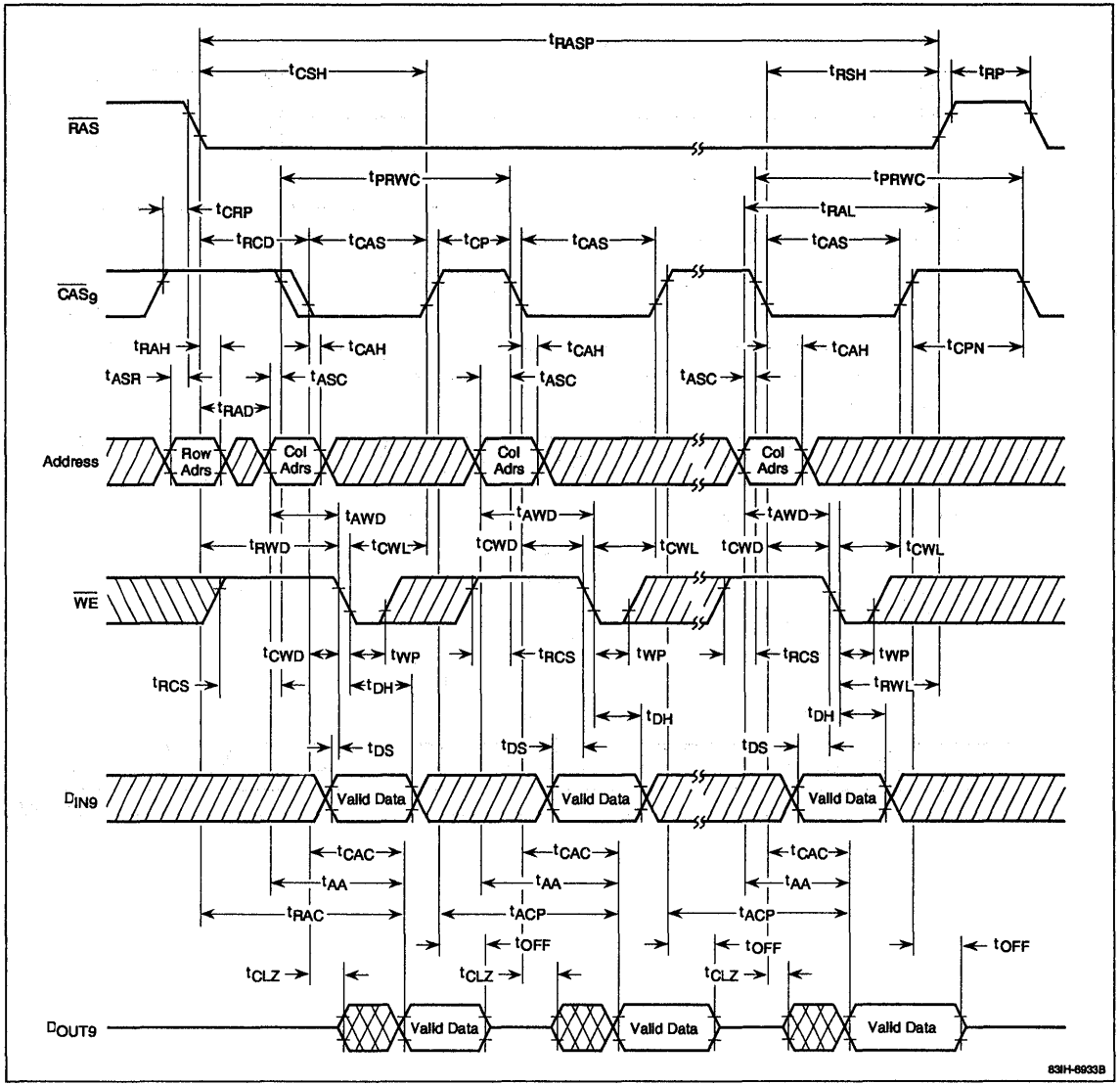
Fast-Page Early Write Cycle



11b

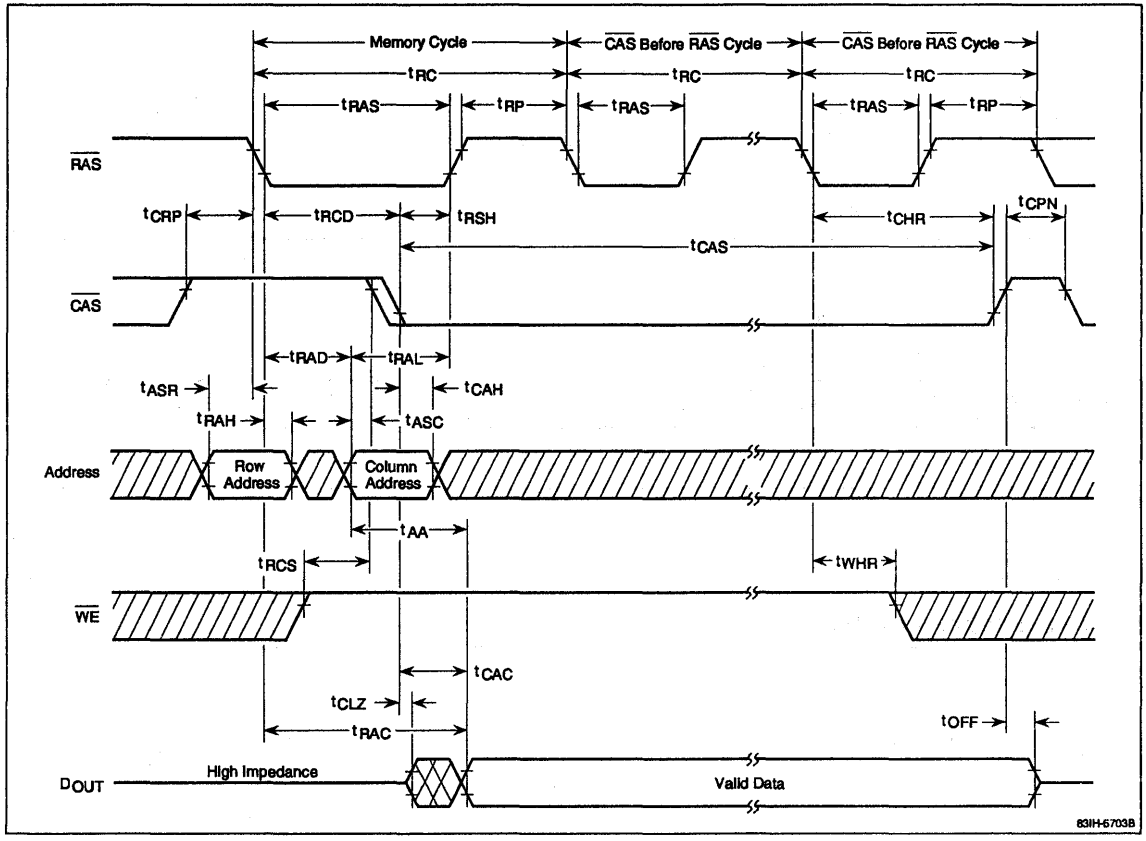
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle (D_{IN9}, D_{OUT9}, and $\overline{CAS}_9$ Only)



Timing Waveforms (cont)

Hidden Refresh Cycle



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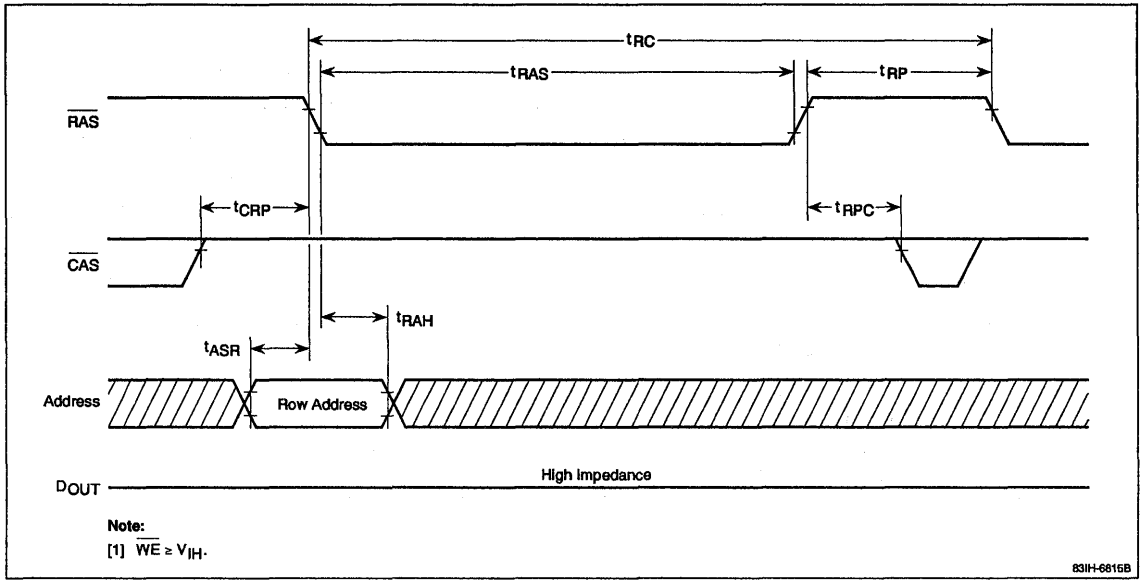
Timing Waveforms (cont)

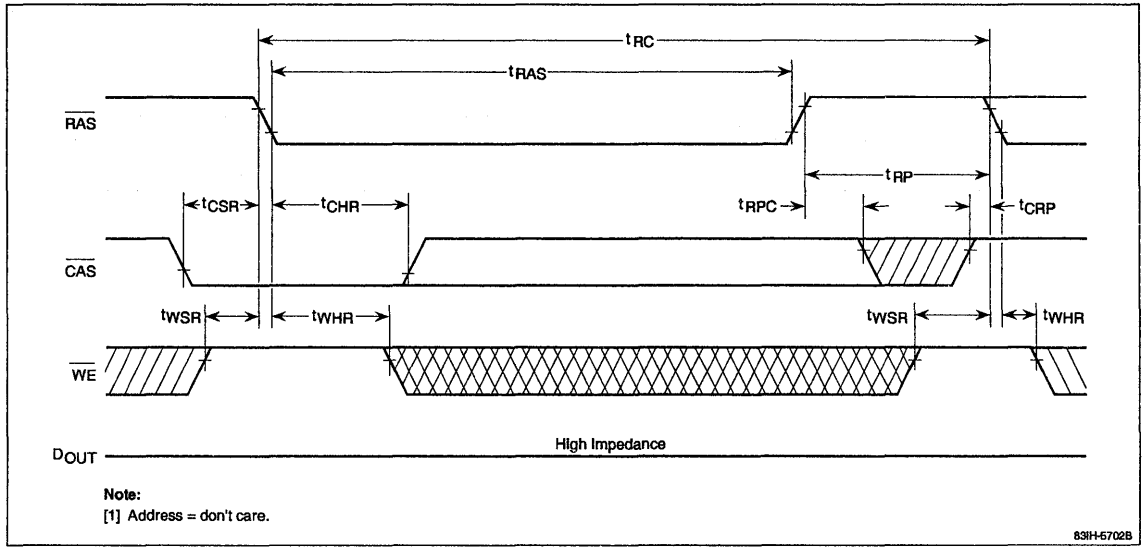
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6816B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



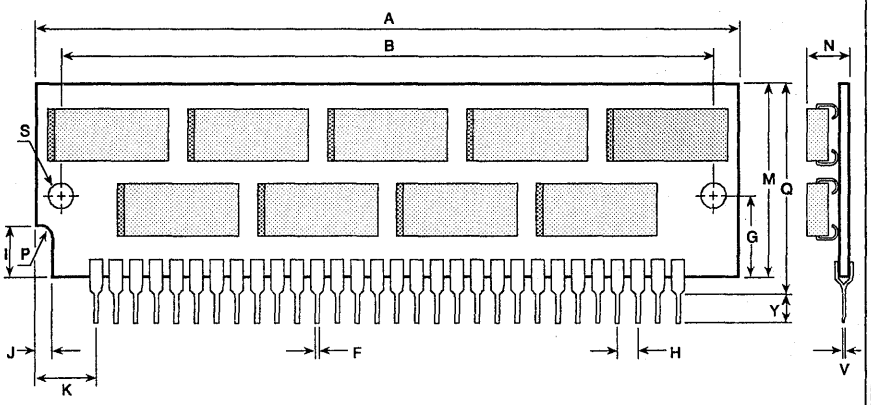
Note:
[1] Address = don't care.

83IH-6702B

Package Drawings

30-Pin Leaded SIMM (MC-424000A9AA)

Item	Millimeters	Inches
A	88.9 ± 0.13	3.500 ± .005
B	82.14 ± 0.13	3.234 ± .005
F	0.5	.020
G	10.16 ± 0.13	.400 ± .005
H	2.54	.100
I	6.35 ± 0.13	.250 ± .005
J	2.03 ± 0.13	.080 ± .005
K	7.62 ± 0.13	.300 ± .005
M	20.3 max	.799 max
N	5.08 max	.200 max
P	1.57 rad	.062 rad
Q	26.28 max	1.035 max
S	3.18 ± 0.13 dia	.125 ± .005 dia
V	0.25	.010
Y	3.4 ± 0.7	.134 ± .028



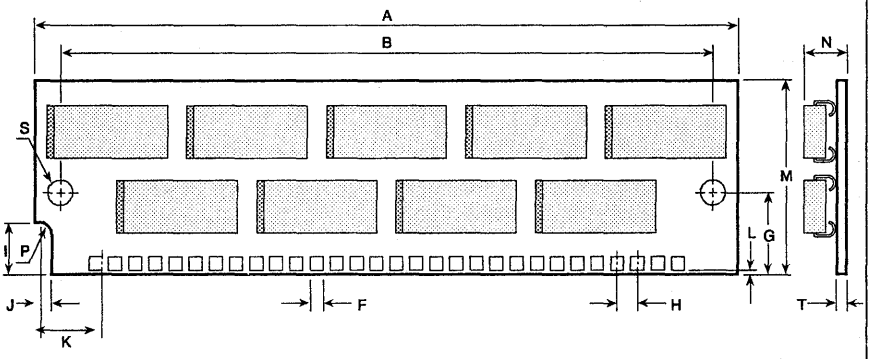
MC-424000A9AA

83YL-8423B (2/92)

11b

30-Pin Socket-Mountable SIMM (MC-424000A9BA)

Item	Millimeters	Inches
A	88.9 ± 0.13	3.500 ± .005
B	82.14 ± 0.13	3.234 ± .005
F	1.78	.070
G	10.16 ± 0.13	.400 ± .005
H	2.54	.100
I	6.35 ± 0.13	.250 ± .005
J	2.03 ± 0.13	.080 ± .005
K	7.62 ± 0.13	.300 ± .005
L	0.25 max	.010 max
M	20.3 max	.799 max
N	5.08 max	.200 max
P	1.57 rad	.062 rad
S	3.18 ± 0.13 dia	.125 ± .005 dia
T	1.27 $^{+0.10}_{-0.08}$	.050 $^{+.004}_{-.003}$



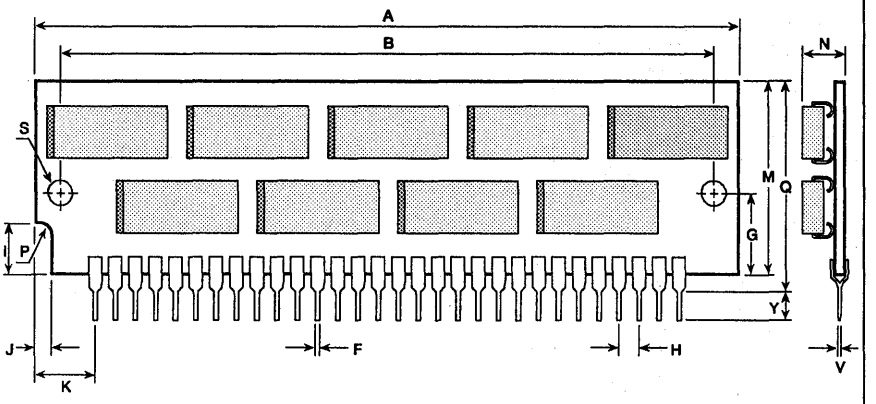
MC-424000A9BA

83YL-8424B (2/92)

Package Drawings (cont)

30-Pin Leaded SIMM (MC-424100A9A)

Item	Millimeters	Inches
A	88.9 ± 0.13	3.500 ± .005
B	82.14 ± 0.13	3.234 ± .005
F	0.5	.020
G	10.16 ± 0.13	.400 ± .005
H	2.54	.100
I	6.35 ± 0.13	.250 ± .005
J	2.03 ± 0.13	.080 ± .005
K	7.62 ± 0.13	.300 ± .005
M	24.03 ± 0.13	.946 ± .005
N	5.28 max	.208 max
P	1.57 rad	.062 rad
Q	26.28 max	1.035 max
S	3.18 ± 0.13 dia	.125 ± .005 dia
V	0.25	.010
Y	3.4 ± 0.7	.134 ± .028

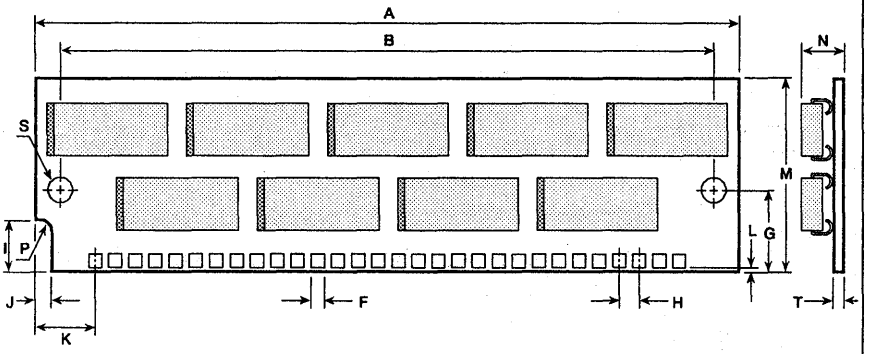


MC-424100A9A

83YL-8285B (1/92)

30-Pin Socket-Mountable SIMM (MC-424100A9B)

Item	Millimeters	Inches
A	88.9 ± 0.13	3.500 ± .005
B	82.14 ± 0.13	3.234 ± .005
F	1.78	.070
G	10.16 ± 0.13	.400 ± .005
H	2.54	.100
I	6.35 ± 0.13	.250 ± .005
J	2.03 ± 0.13	.080 ± .005
K	7.62 ± 0.13	.300 ± .005
L	0.25 max	.010 max
M	24.03 ± 0.13	.946 ± .005
N	5.28 max	.208 max
P	1.57 rad	.062 rad
S	3.18 ± 0.13 dia	.125 ± .005 dia
T	1.27 $^{+0.10}_{-0.08}$	.050 $^{+.004}_{-.003}$



MC-424100A9B

83YL-8286B (1/92)

MC-424000A32
4,194,304 x 32-Bit
Dynamic CMOS RAM Module

Description

The MC-424000A32 is a fast-page dynamic RAM module organized as 4,194,304 words by 32 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 2048 address combinations of A_0 - A_{10} during a 32-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight, and cost of a system.. Each SIMM contains eight 4M x 4-bit DRAMs (μPD4217400) and eight power supply decoupling capacitors for noise reduction. DQ_0 - DQ_{31} are common input/output pins.

Features

- 4,194,304-word by 32-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 2048 refresh cycles every 32 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

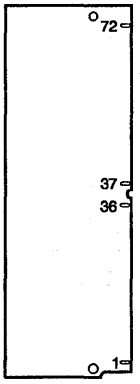
SIMM is a trademark of Wang Laboratories.

Pin Identification

Name	Function
A_0 - A_{10}	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobes
DQ_0 - DQ_{31}	Common data inputs/outputs
$\overline{RAS}_0$, $\overline{RAS}_2$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{16}
4	DQ_1
5	DQ_{17}
6	DQ_2
7	DQ_{18}
8	DQ_3
9	DQ_{19}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	A_{10}
20	DQ_4
21	DQ_{20}
22	DQ_5
23	DQ_{21}
24	DQ_6
25	DQ_{22}
26	DQ_7
27	DQ_{23}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	A_9
33	NC
34	$\overline{RAS}_2$
35	NC
36	NC

Pin	Symbol
37	NC
38	NC
39	GND
40	$\overline{CAS}_0$
41	$\overline{CAS}_2$
42	$\overline{CAS}_3$
43	$\overline{CAS}_1$
44	$\overline{RAS}_0$
45	NC
46	NC
47	$\overline{WE}$
48	NC
49	DQ_8
50	DQ_{24}
51	DQ_9
52	DQ_{25}
53	DQ_{10}
54	DQ_{26}

Pin	Symbol
55	DQ_{11}
56	DQ_{27}
57	DQ_{12}
58	DQ_{28}
59	V_{CC}
60	DQ_{29}
61	DQ_{13}
62	DQ_{30}
63	DQ_{14}
64	DQ_{31}
65	DQ_{15}
66	NC
67	[Note 1]
68	[Note 1]
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

[1] Pins 67 through 70 are defined by access time:

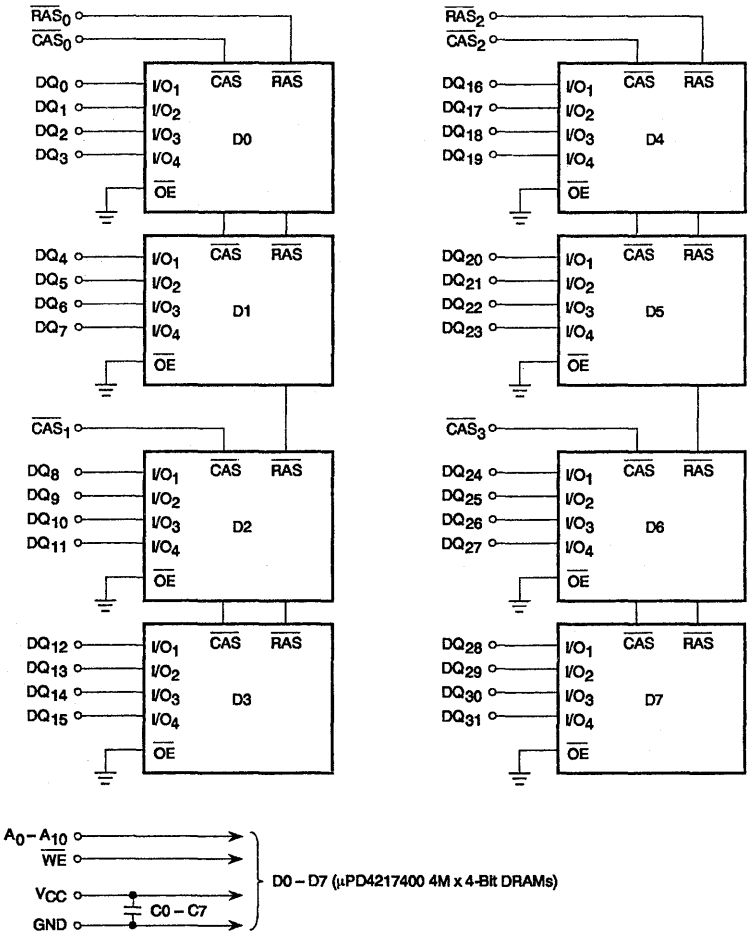
Pin	60 ns	70 ns	80 ns	100 ns
67	NC	NC	NC	NC
68	GND	GND	GND	GND
69	NC	GND	NC	GND
70	NC	NC	GND	GND

83CL-6838A

Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-424000A32BD-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.000 inch)	9.3 mm (0.366 inch)	Eight μPD4217400LE
BD-70	70 ns				
BD-80	80 ns				
MC-424000A32FD-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FD-70	70 ns				
FD-80	80 ns				
MC-424000A32BH-60	60 ns	72-pin socket-mountable SIMM (solder plating)	31.75 mm (1.250 inch)	5.08 mm (0.200 inch)	Eight μPD4217400LE
BH-70	70 ns				
BH-80	80 ns				
MC-424000A32FH-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FH-70	70 ns				
FH-80	80 ns				

MC-424000A32 Connection Diagram



11c

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	68	pF	A_0 - A_{10}
	C_{I2}	76	pF	$\overline{WE}$
	C_{I3}	43	pF	$\overline{RAS}$
	C_{I4}	29	pF	$\overline{CAS}$
Input/output capacitance	C_{IO}/C_{OO}	17	pF	DQ_0 - DQ_{31}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		16	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			8	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−80	80	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	DQ_0 to DQ_{31} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		880		800		720	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		880		800		720	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		640		560		480	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		880		800		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		ns	(Note 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	ns	(Note 10)
Fast-page cycle time	t_{PC}	40		45		50		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	60	25	60	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		32		32		32	ms	Addresses A_0 - A_{10}
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

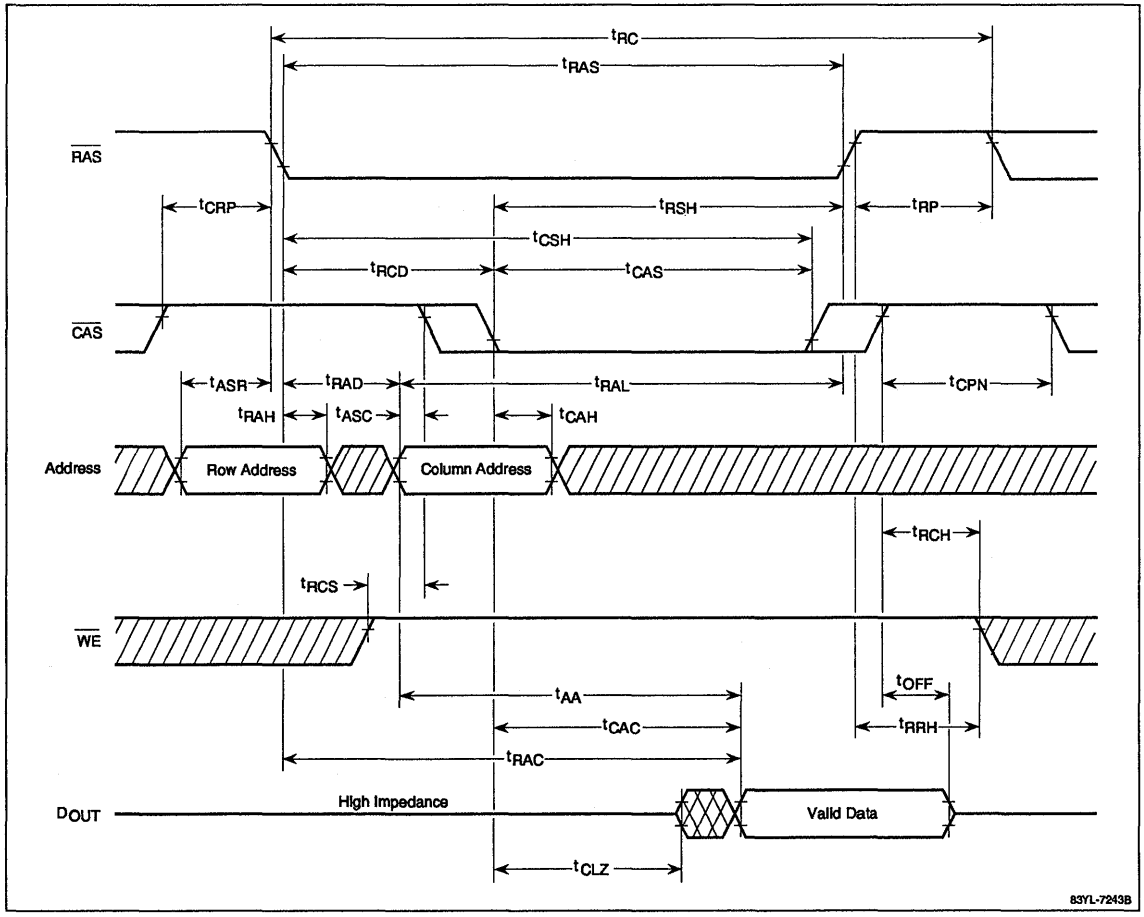
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Timing Waveforms

Read Cycle



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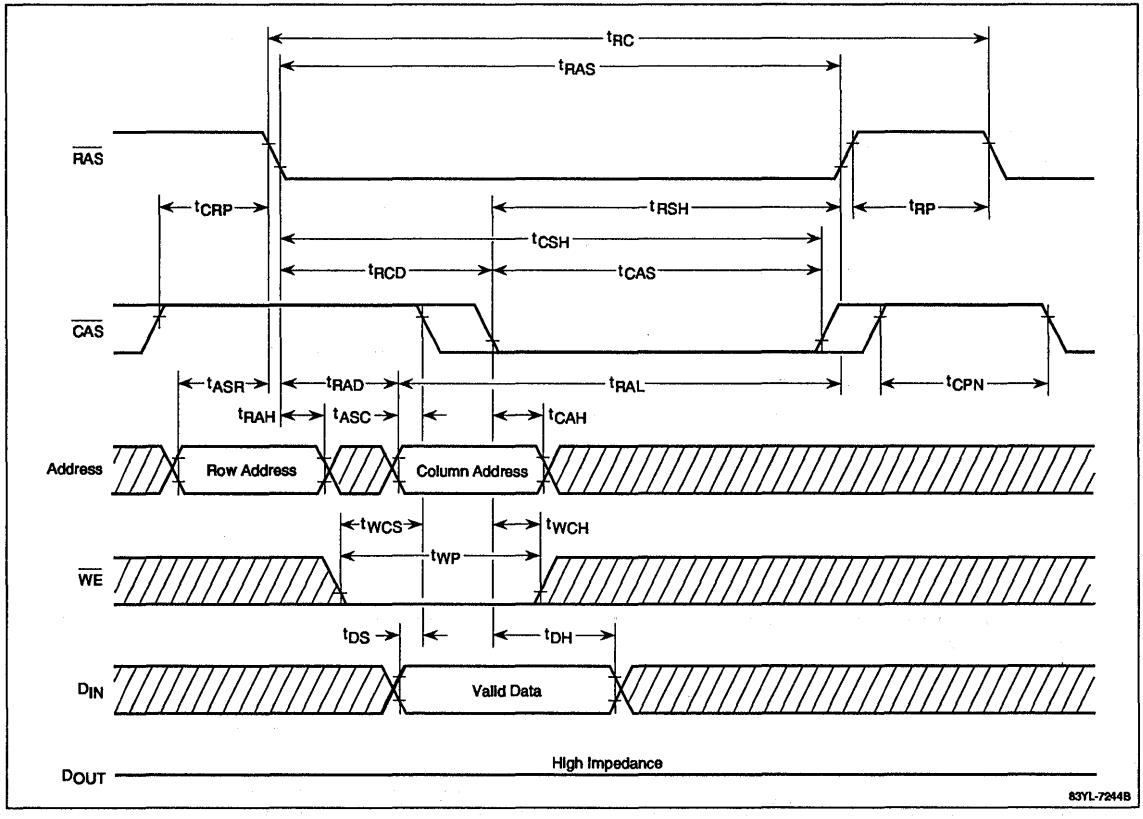
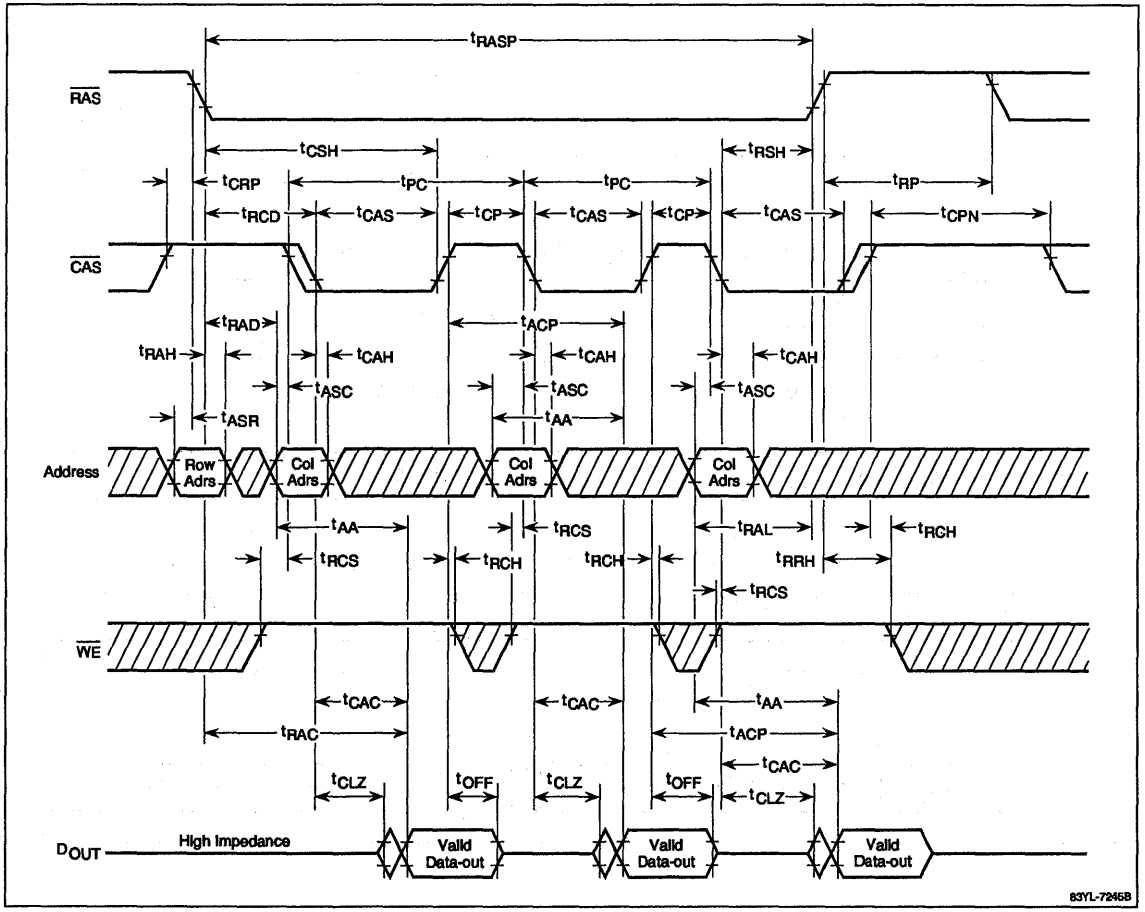
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Fast-Page Read Cycle



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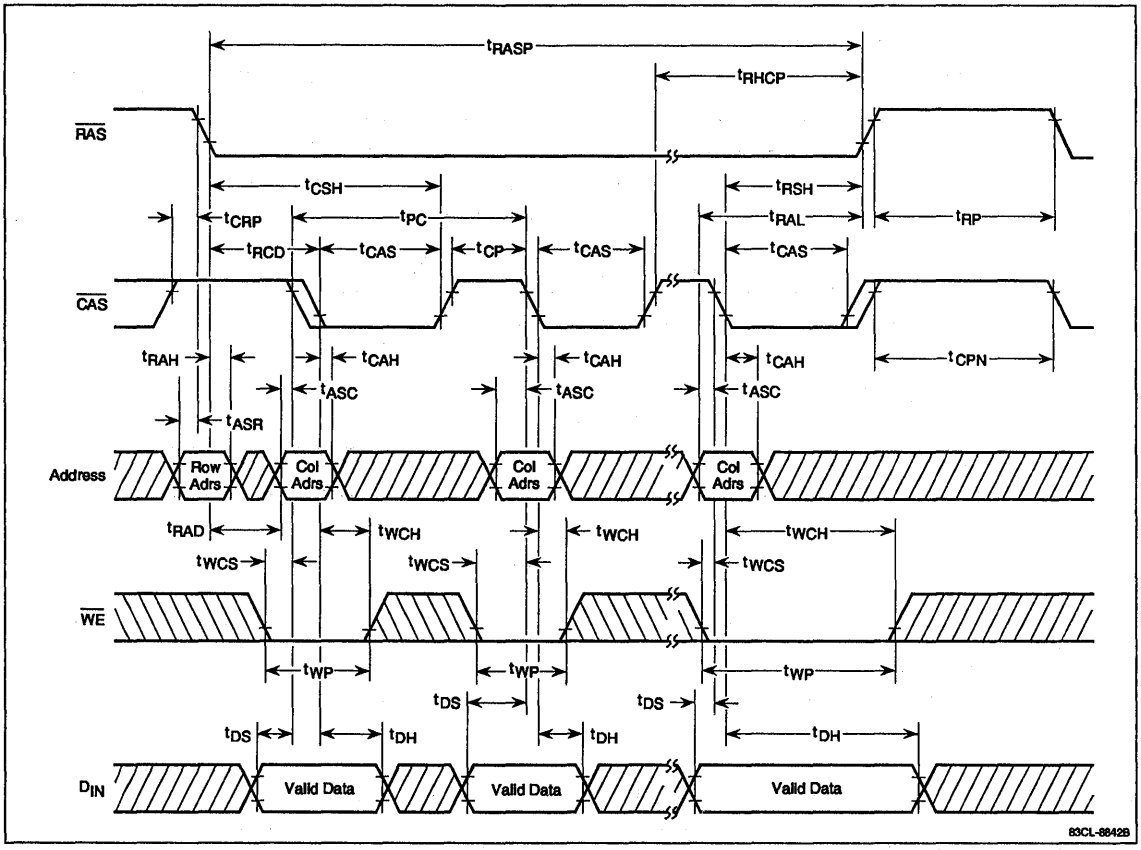
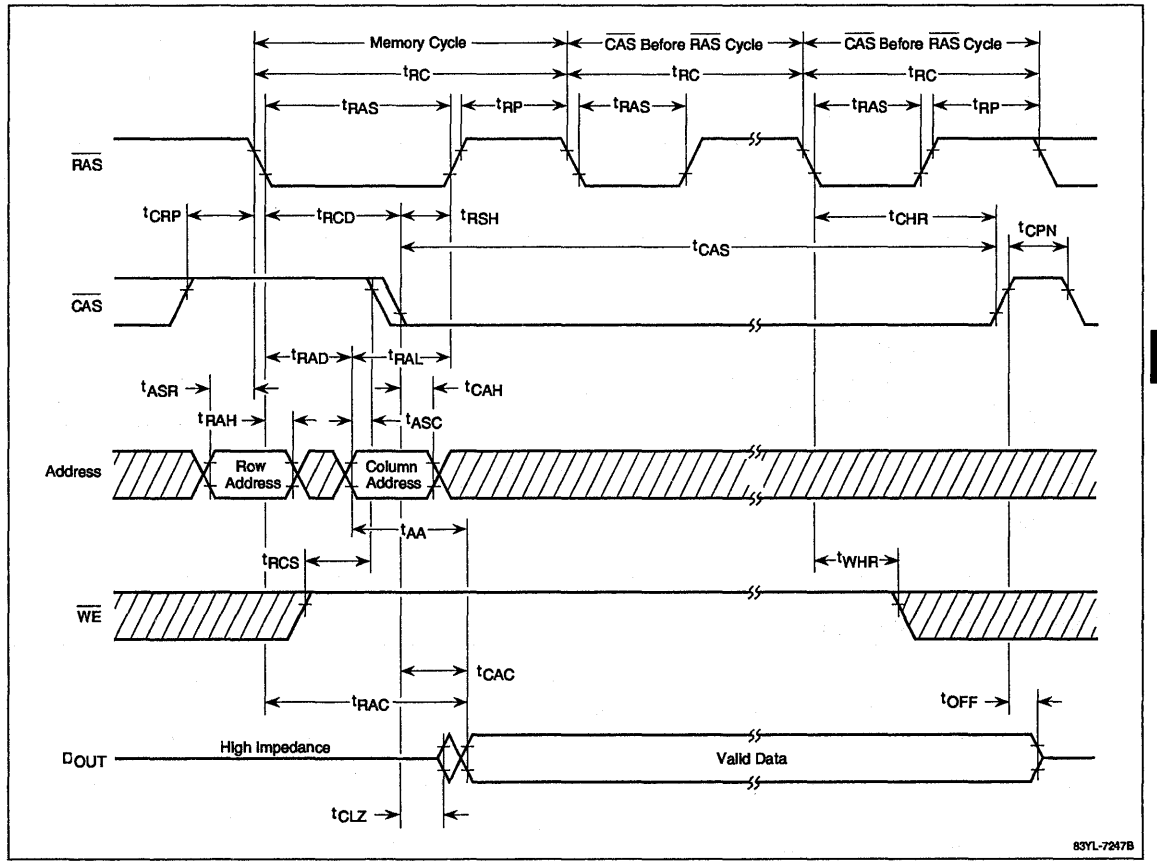
Timing Waveforms (cont)

Fast-Page Early Write Cycle



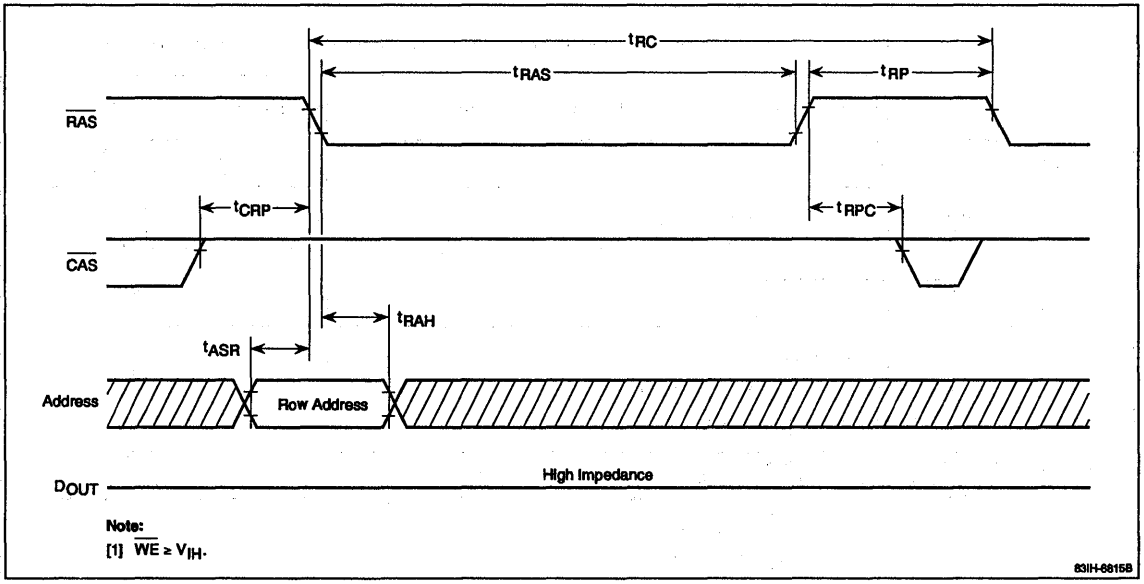
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

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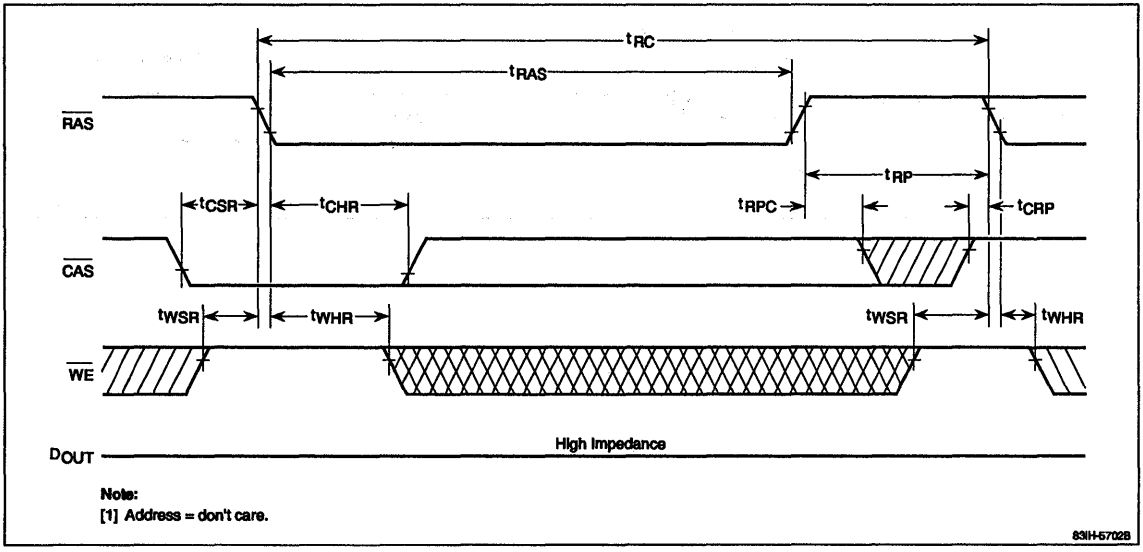
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

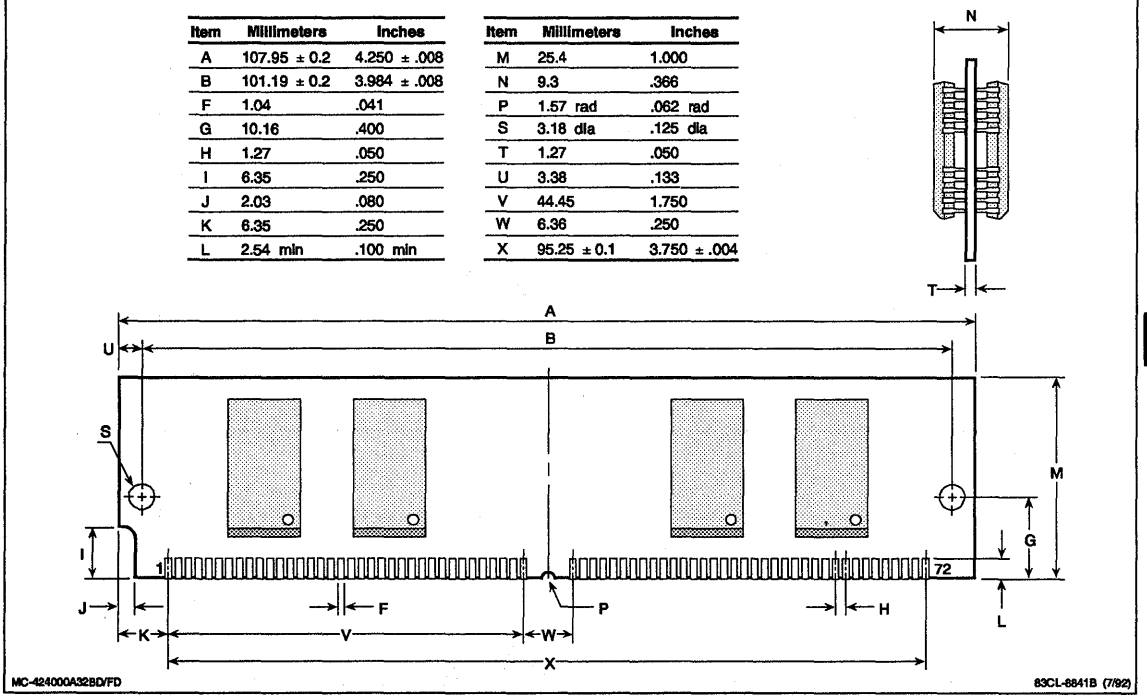
83IH-5702B

Package Drawings

72-Pin Socket-Mountable SIMM (MC-424000A32, Suffix BD or FD)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	25.4	1.000
N	9.3	.366
P	1.57 rad	.062 rad
S	3.18 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



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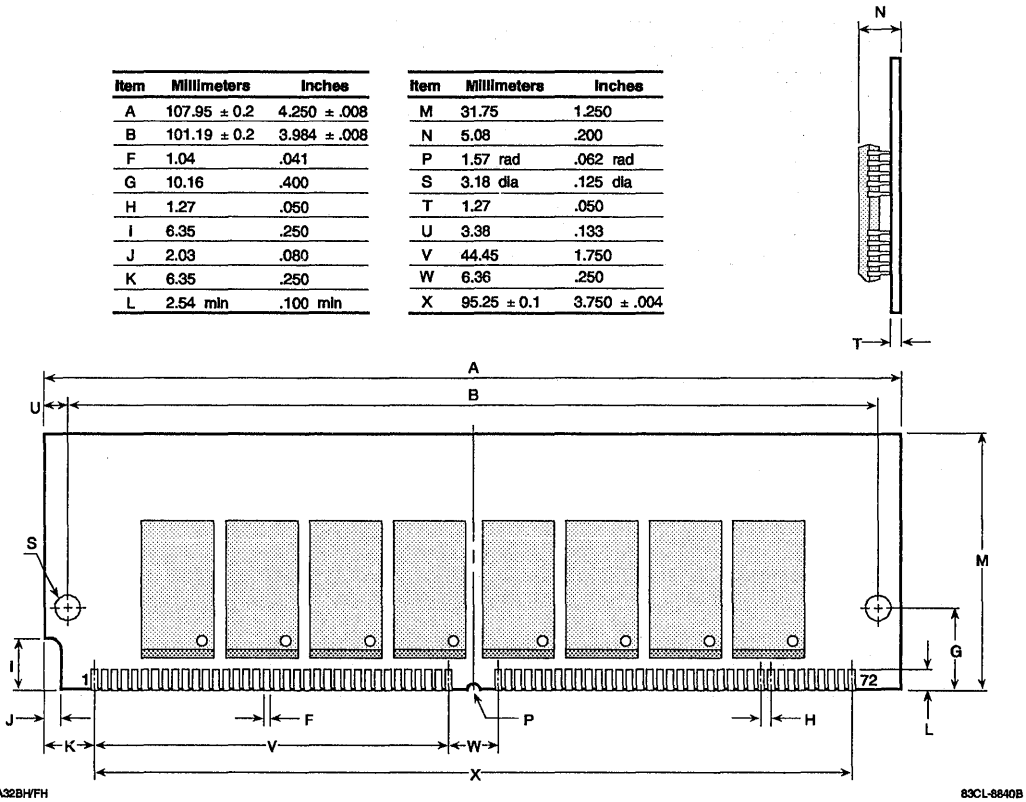
Package Drawing (cont)

72-Pin Socket-Mountable SIMM (MC-424000A32, Suffix BH or FH)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	31.75	1.250
N	5.08	.200
P	1.57 rad	.062 rad
S	3.18 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-424000A36
4,194,304 x 36-Bit
Dynamic CMOS RAM Module

Description

The MC-424000A36 is a fast-page dynamic RAM module organized as 4,194,304 words by 36 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 2048 address combinations of A_0 - A_{10} during a 32-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight, and cost of a system. Each SIMM contains eight 4M x 4-bit DRAMs (μPD4217400), four 4M x 1-bit DRAMs (μPD424100), and 12 power supply decoupling capacitors for noise reduction. DQ_0 - DQ_{35} are common input/output pins.

Features

- 4,194,304-word by 36-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 2048 refresh cycles every 32 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

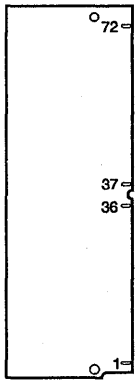
Pin Identification

Name	Function
A_0 - A_{10}	Address inputs
$\overline{CAS_0}$ - $\overline{CAS_3}$	Column address strobes
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS_0}$, $\overline{RAS_2}$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{18}
4	DQ_1
5	DQ_{19}
6	DQ_2
7	DQ_{20}
8	DQ_3
9	DQ_{21}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	A_{10}
20	DQ_4
21	DQ_{22}
22	DQ_5
23	DQ_{23}
24	DQ_6
25	DQ_{24}
26	DQ_7
27	DQ_{25}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	A_9
33	NC
34	$\overline{RAS_2}$
35	DQ_{26}
36	DQ_8

Pin	Symbol
37	DQ_{17}
38	DQ_{35}
39	GND
40	$\overline{CAS_0}$
41	$\overline{CAS_2}$
42	$\overline{CAS_3}$
43	$\overline{CAS_1}$
44	$\overline{RAS_0}$
45	NC
46	NC
47	$\overline{WE}$
48	NC
49	DQ_9
50	DQ_{27}
51	DQ_{10}
52	DQ_{28}
53	DQ_{11}
54	DQ_{29}

Pin	Symbol
55	DQ_{12}
56	DQ_{30}
57	DQ_{13}
58	DQ_{31}
59	V_{CC}
60	DQ_{32}
61	DQ_{14}
62	DQ_{33}
63	DQ_{15}
64	DQ_{34}
65	DQ_{16}
66	NC
67	[Note 1]
68	[Note 1]
69	[Note 1]
70	[Note 1]
71	NC
72	GND

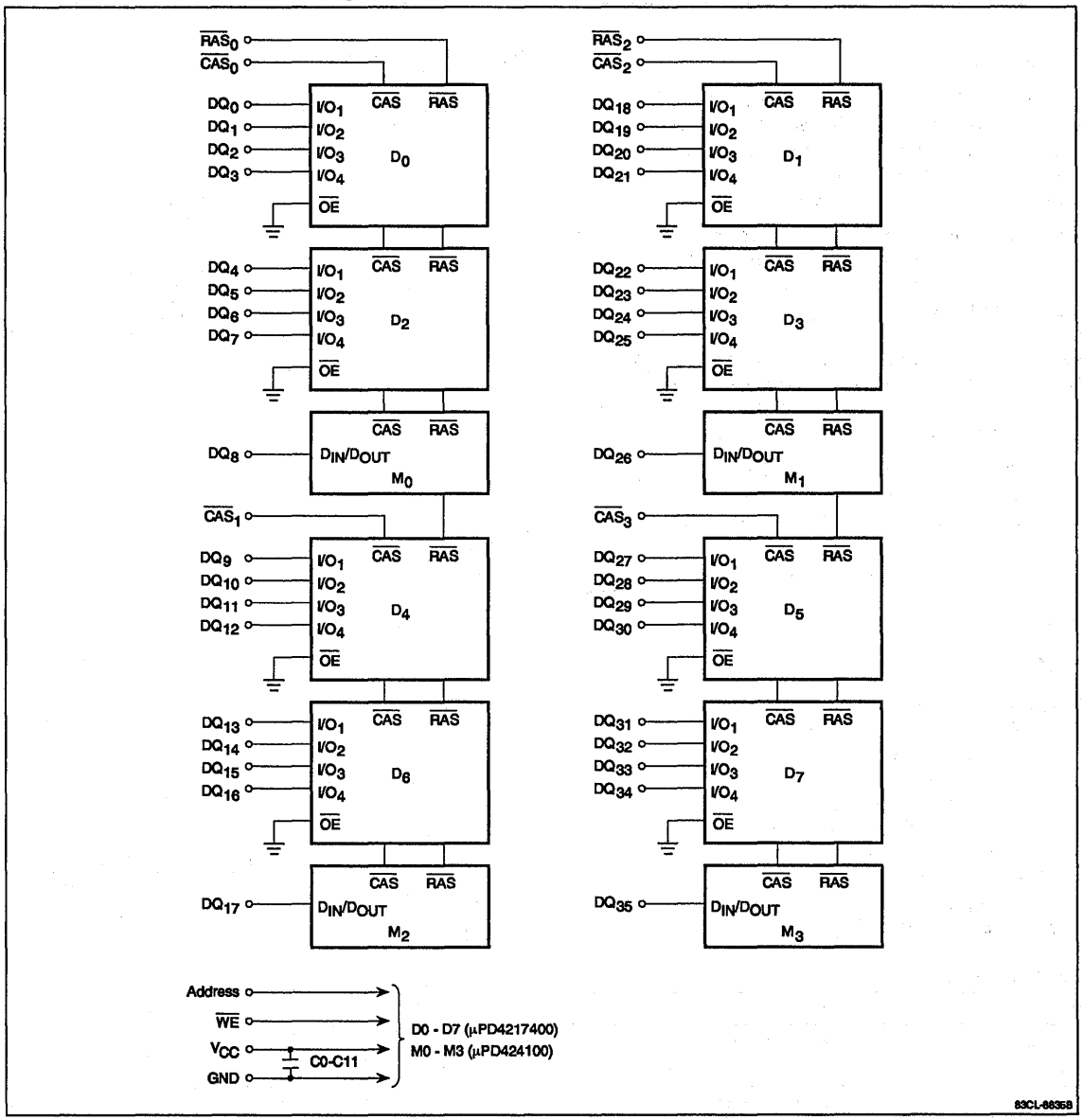
Notes:

[1] Pins 67 through 70 are defined by access time:

Pin	60 ns	70 ns	80 ns	100 ns
67	NC	NC	NC	NC
68	GND	GND	GND	GND
69	NC	GND	NC	GND
70	NC	NC	GND	GND

83CL-8834A

MC-424000A36 Connection Diagram



Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-424000A36BD-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.000 inch)	9.3 mm (0.366 inch)	Eight μPD4217400LE Four μPD424100LA
BD-70	70 ns				
BD-80	80 ns				
MC-424000A36FD-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FD-70	70 ns				
FD-80	80 ns				
MC-424000A36BH-60	60 ns	72-pin socket-mountable SIMM (solder plating)	31.75 mm (1.250 inch)	5.08 mm (0.200 inch)	Eight μPD4217400LE Four μPD424100LA
BH-70	70 ns				
BH-80	80 ns				
MC-424000A36FH-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FH-70	70 ns				
FH-80	80 ns				

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	12 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	88	pF	A_0 - A_{10}
	C_{I2}	104	pF	$\overline{WE}$
	C_{I3}	57	pF	$\overline{RAS}$
	C_{I4}	36	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{O1}	17	pF	DQ_0 - DQ_{35} except pins listed below
	C_{I2}/C_{O2}	22	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			12	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−120	120	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−20	20	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		1360		1200		1080	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1360		1200		1080	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		1000		880		760	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1360		1200		1080	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		40		45	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		ns	(Note 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	ns	(Note 10)
Fast-page cycle time	t_{PC}	40		45		50		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	60	25	60	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		32		32		32	ms	Addresses A_0 - A_{10}
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

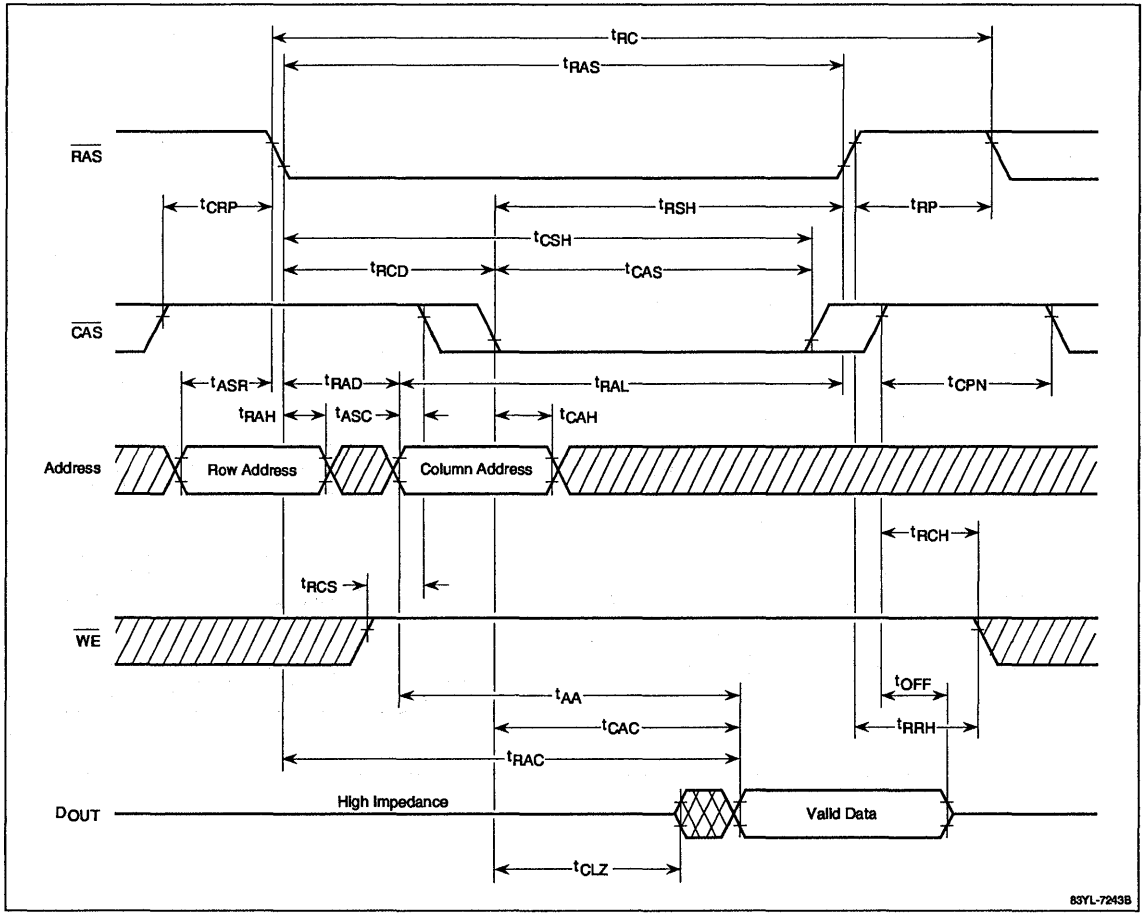
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Timing Waveforms

Read Cycle



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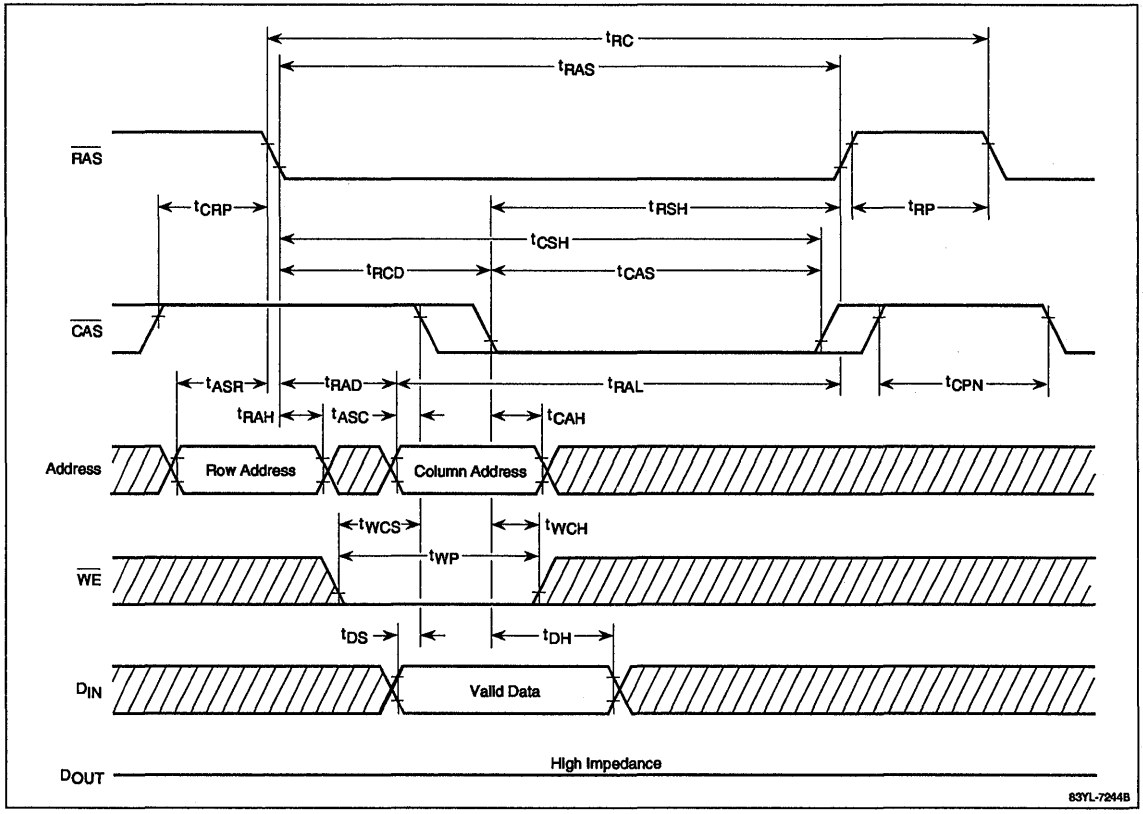
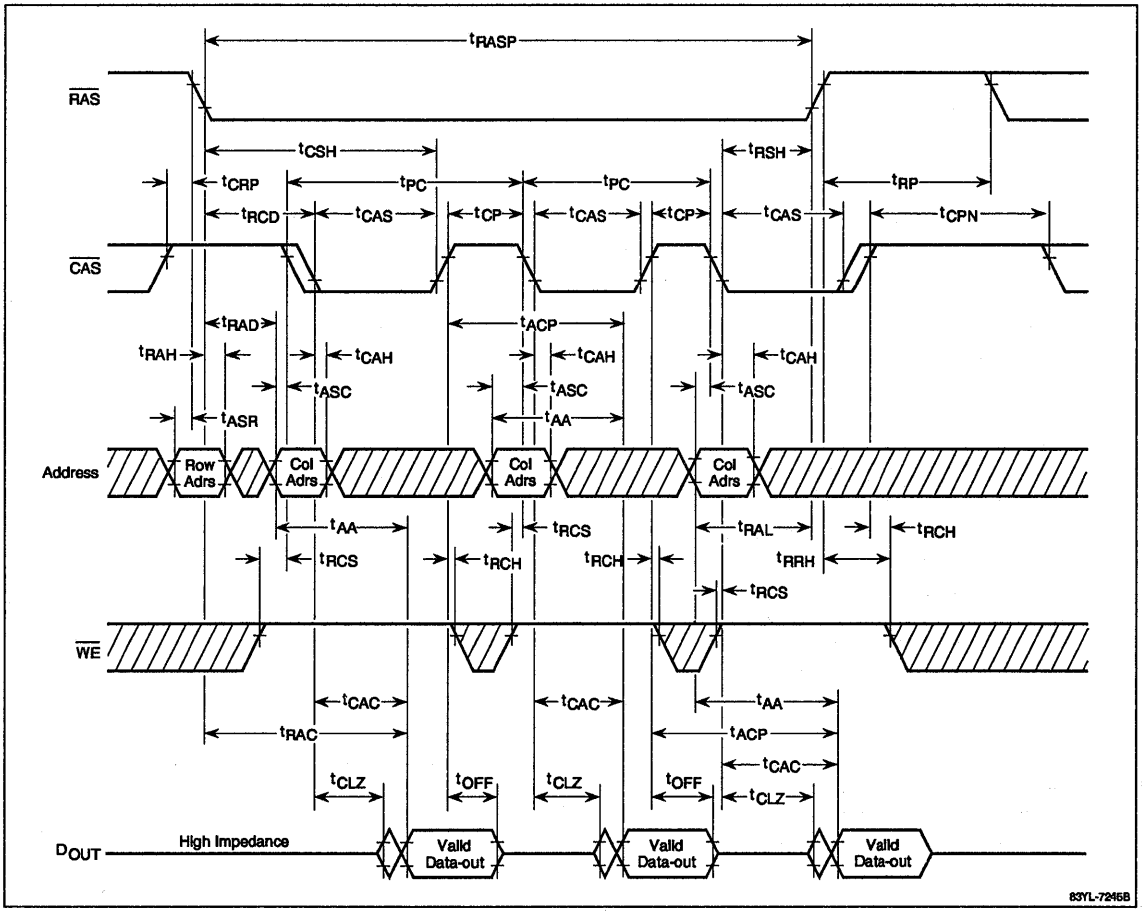
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Fast-Page Read Cycle



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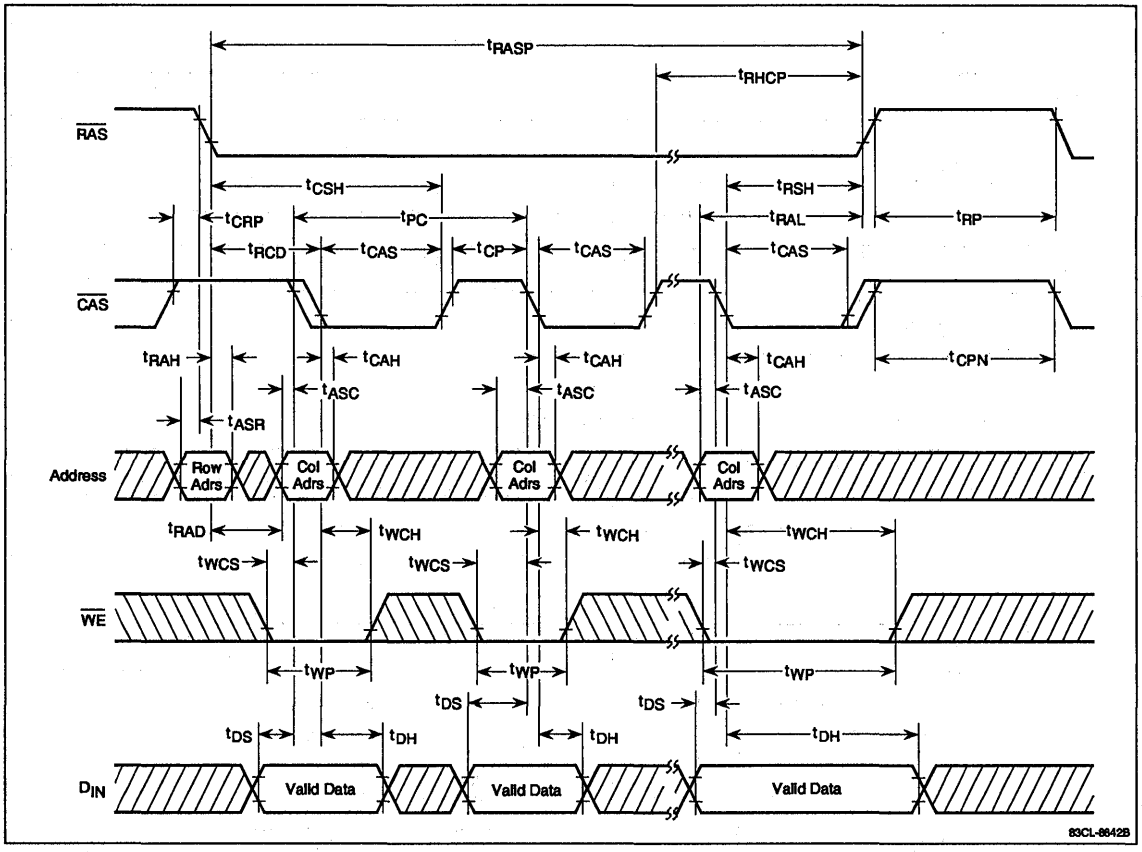
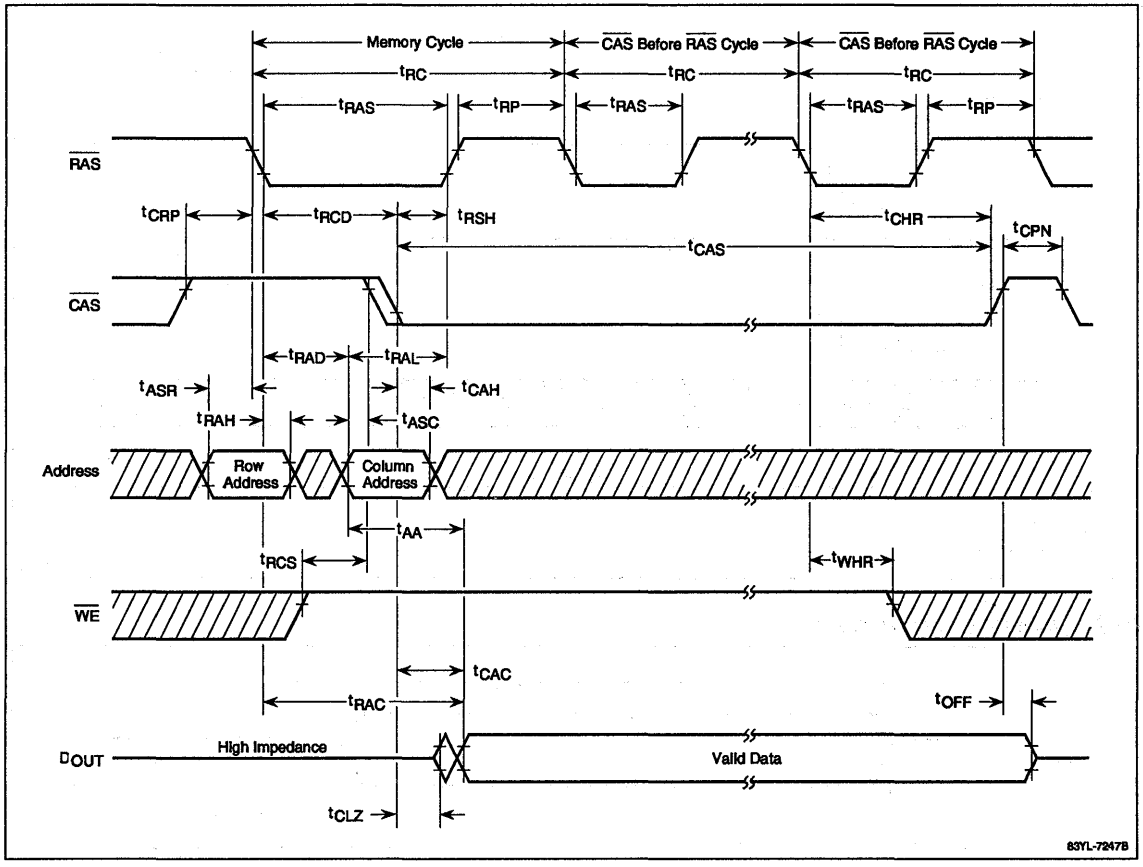
Timing Waveforms (cont)

Fast-Page Early Write Cycle



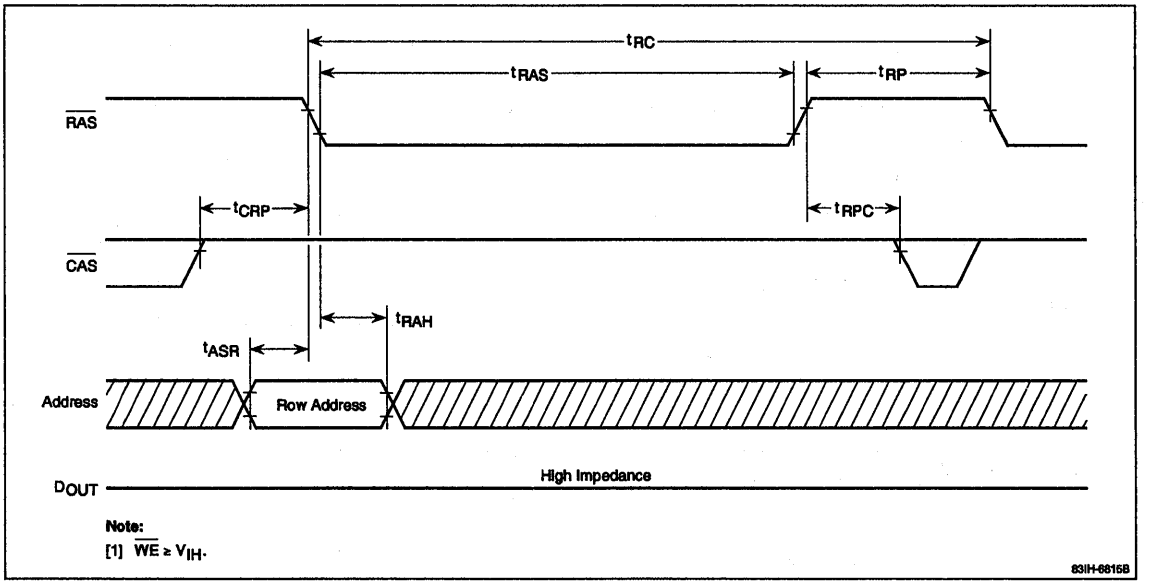
Timing Waveforms (cont)

Hidden Refresh Cycle

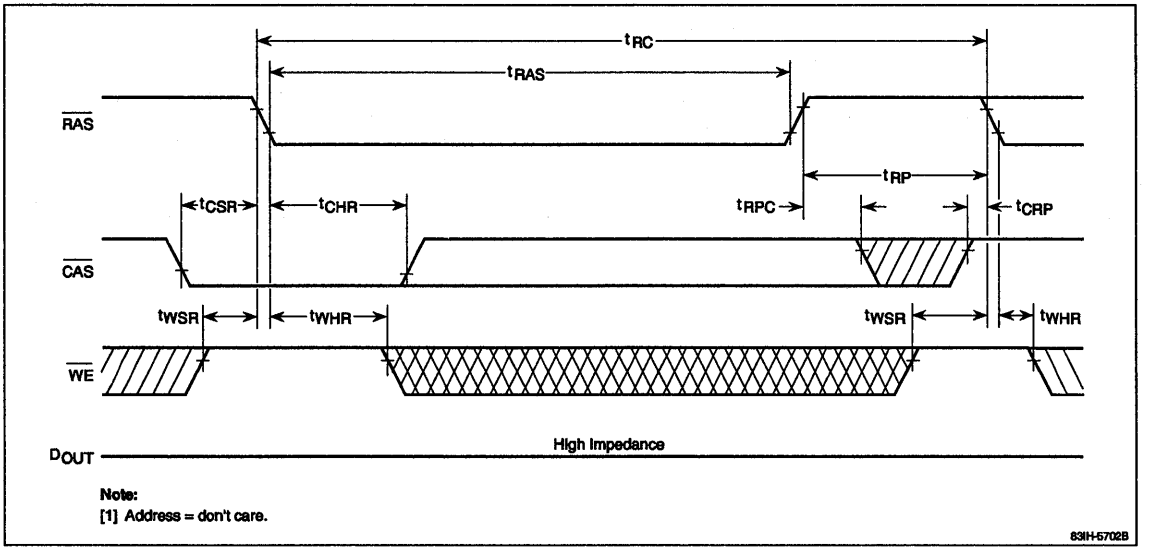


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

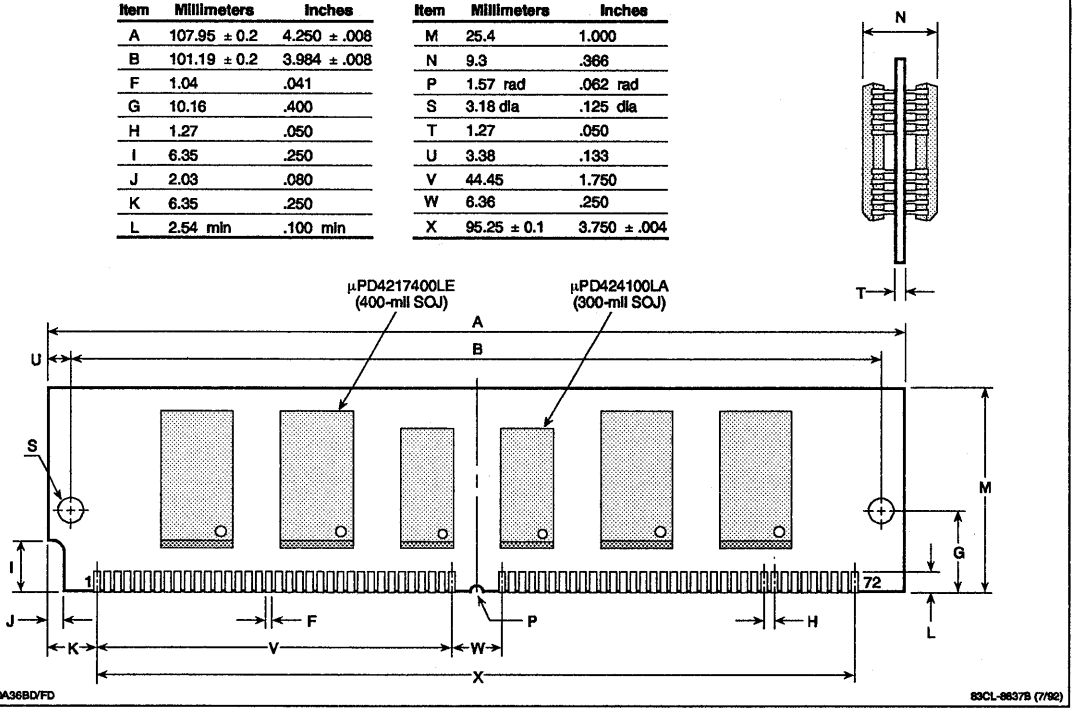


Package Drawings

72-Pin Socket-Mountable SIMM (MC-424000A36. Suffix BD or FD)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	25.4	1.000
N	9.3	.366
P	1.57 rad	.062 rad
S	3.18 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



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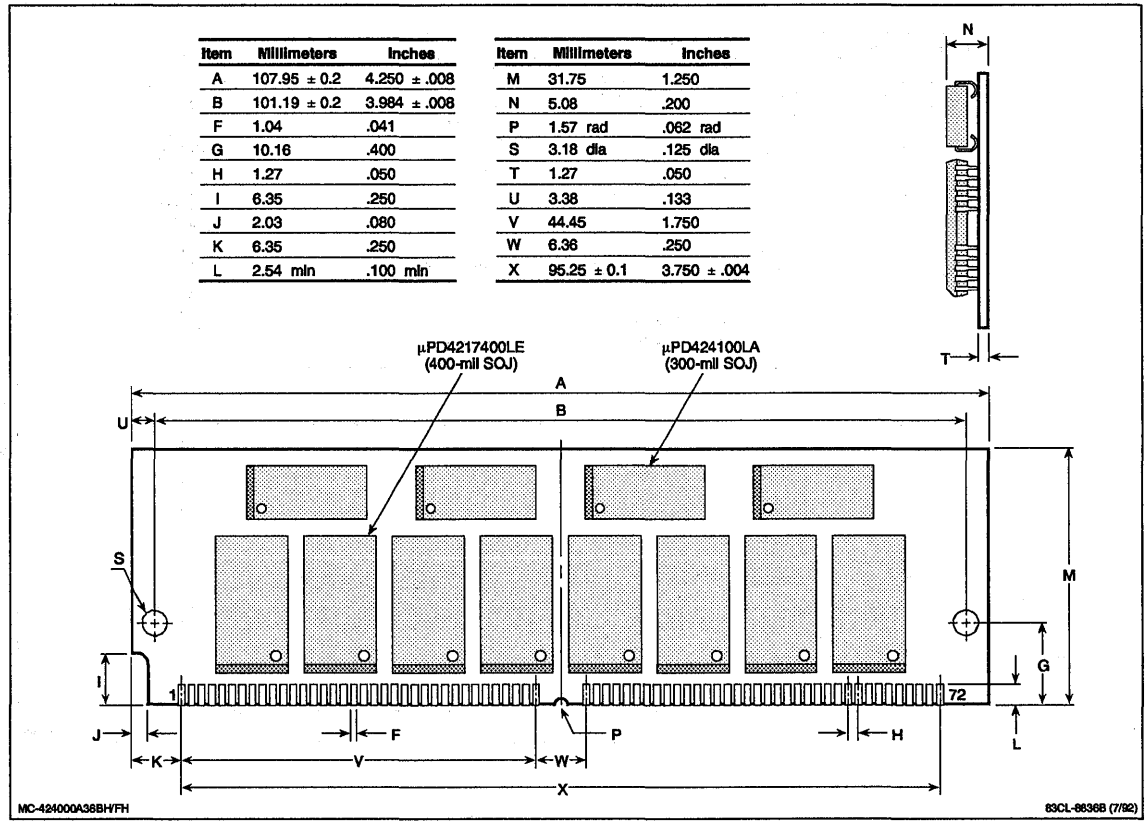
Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-424000A36, Suffix BH or FH)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	31.75	1.250
N	5.08	.200
P	1.57 rad	.062 rad
S	3.18 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-428000A32
8,388,608 x 32-Bit
Dynamic CMOS RAM Module

Description

The MC-428000A32 is a fast-page dynamic RAM module organized as 8,388,608 words by 32 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 2048 address combinations of A_0 - A_{10} during a 32-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight, and cost of a system.. Each SIMM contains sixteeen 4,194,304 x 4-bit DRAMs (μPD4217400) and 16 power supply decoupling capacitors for noise reduction. DQ_0 - DQ_{31} are common input/output pins.

Features

- 8,388,608-word by 32-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 2048 refresh cycles every 32 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

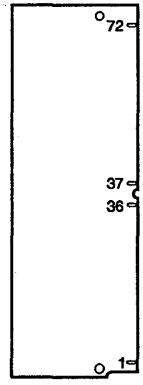
SIMM is a trademark of Wang Laboratories.

Pin Identification

Name	Function
A_0 - A_{10}	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobes
DQ_0 - DQ_{31}	Common data inputs/outputs
$\overline{RAS}_0$ - $\overline{RAS}_3$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{16}
4	DQ_1
5	DQ_{17}
6	DQ_2
7	DQ_{18}
8	DQ_3
9	DQ_{19}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	A_{10}
20	DQ_4
21	DQ_{20}
22	DQ_5
23	DQ_{21}
24	DQ_6
25	DQ_{22}
26	DQ_7
27	DQ_{23}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	A_9
33	$\overline{RAS}_3$
34	$\overline{RAS}_2$
35	NC
36	NC

Pin	Symbol
37	NC
38	NC
39	GND
40	$\overline{CAS}_0$
41	$\overline{CAS}_2$
42	$\overline{CAS}_3$
43	$\overline{CAS}_1$
44	$\overline{RAS}_0$
45	$\overline{RAS}_1$
46	NC
47	$\overline{WE}$
48	NC
49	DQ_8
50	DQ_{24}
51	DQ_9
52	DQ_{25}
53	DQ_{10}
54	DQ_{26}

Pin	Symbol
55	DQ_{11}
56	DQ_{27}
57	DQ_{12}
58	DQ_{28}
59	V_{CC}
60	DQ_{29}
61	DQ_{13}
62	DQ_{30}
63	DQ_{14}
64	DQ_{31}
65	DQ_{15}
66	NC
67	[Note 1]
68	[Note 1]
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

[1] Pins 67 through 70 are defined by access time:

Pin	60 ns	70 ns	80 ns	100 ns
67	GND	GND	GND	GND
68	NC	NC	NC	NC
69	NC	GND	NC	GND
70	NC	NC	GND	GND

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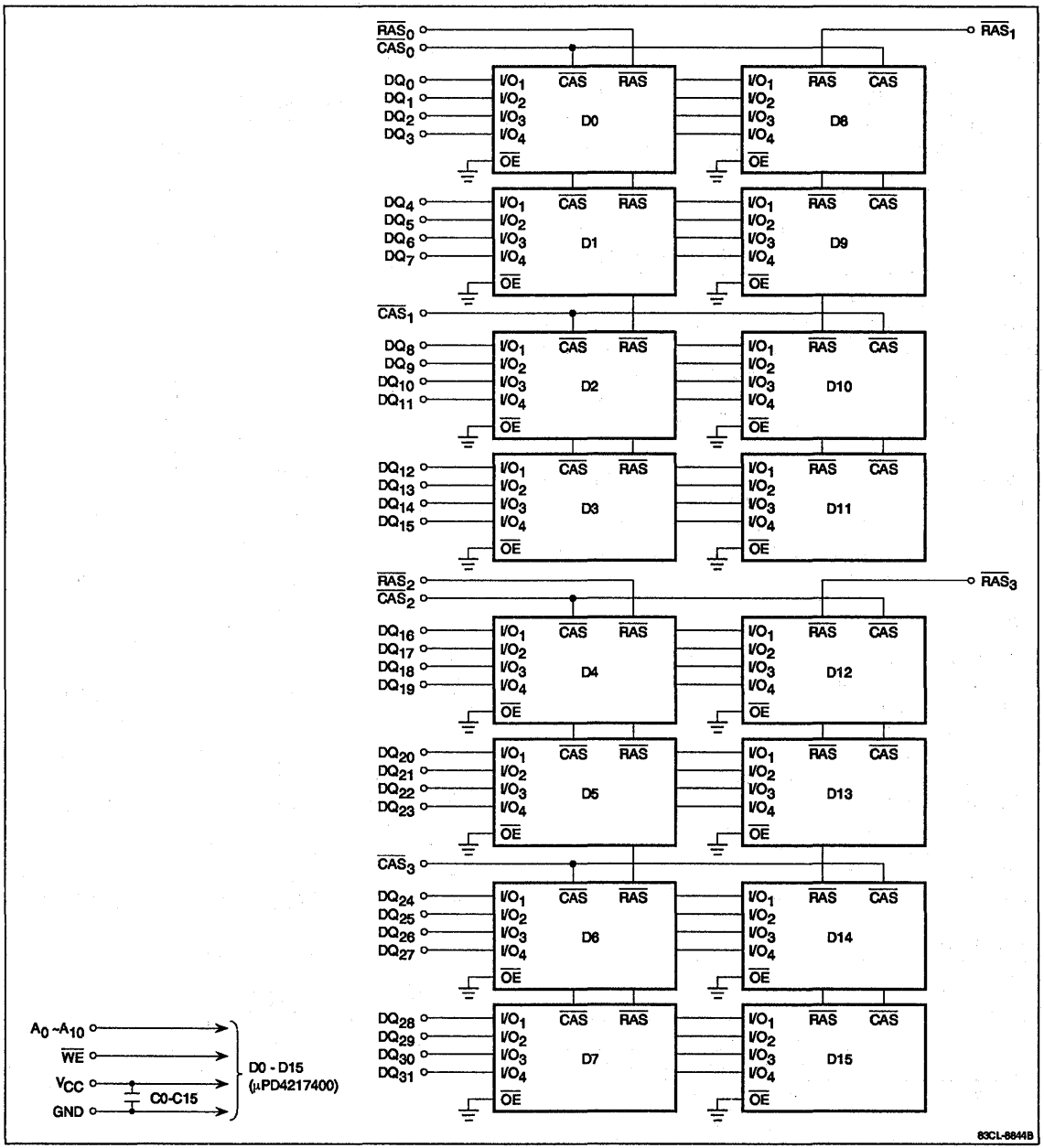
MC-428000A32 Connection Diagram



Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-428000A32BH-60	60 ns	72-pin socket-mountable SIMM (solder plating)	31.75 mm (1.250 inch)	9.3 mm (0.366 inch)	16 μPD4217400LE
BH-70	70 ns				
BH-80	80 ns				
MC-428000A32FH-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FH-70	70 ns				
FH-80	80 ns				

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	24 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

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Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	121	pF	A_0 - A_{10}
	C_{I2}	137	pF	$\overline{WE}$
	C_{I3}	48	pF	$\overline{RAS}$
	C_{I4}	48	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{O1}	29	pF	DQ_0 - DQ_{31}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		32	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			16	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−160	160	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−20	20	μA	DQ_0 to DQ_{31} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-60		-70		-80			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		940		860		780	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		940		860		780	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		700		620		540	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		940		860		780	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		35		35		45	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		40		45	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0	20	0	20	0	20	ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		15		20		20	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	17		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	ns	(Note 10)
Fast-page cycle time	t_{PC}	40		45		50		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	60	25	60	ns	(Note 11)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		32		32		32	ms	Addresses A_0 - A_{10}
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

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Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

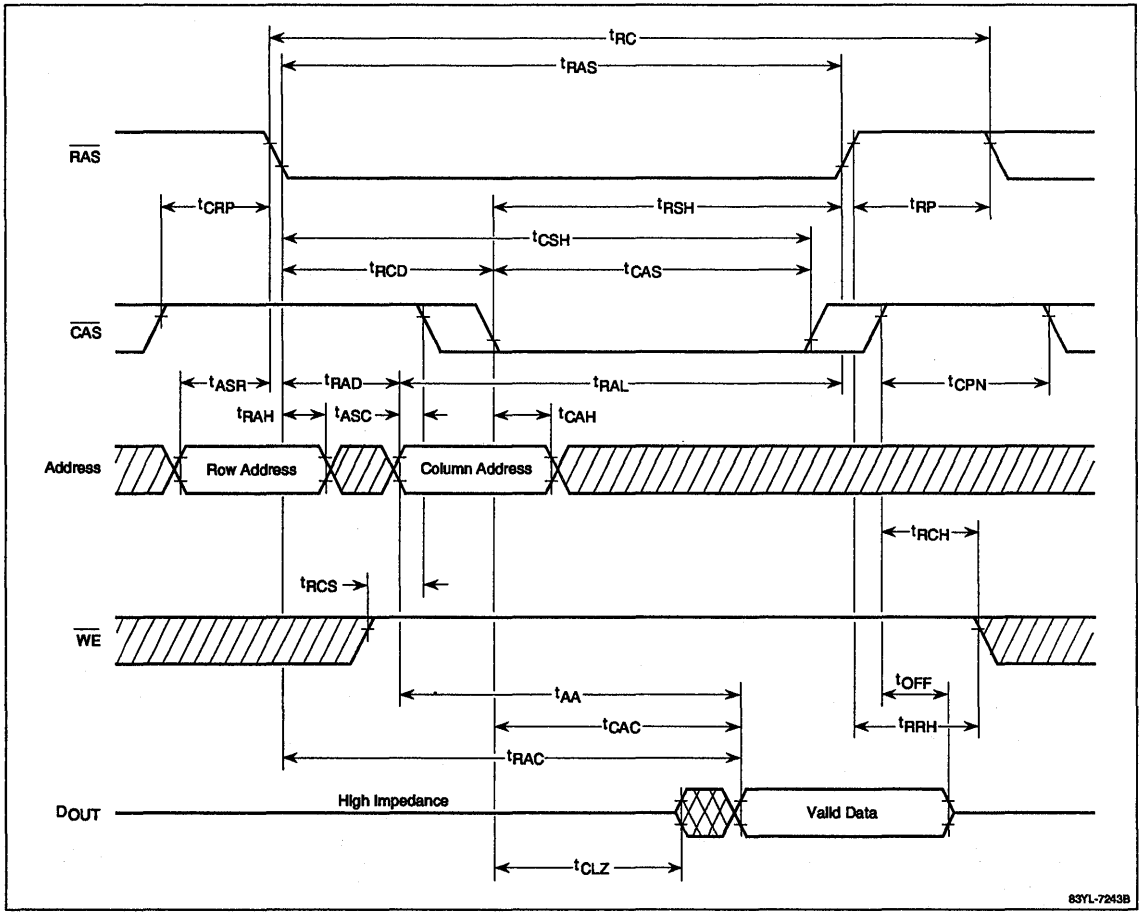
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

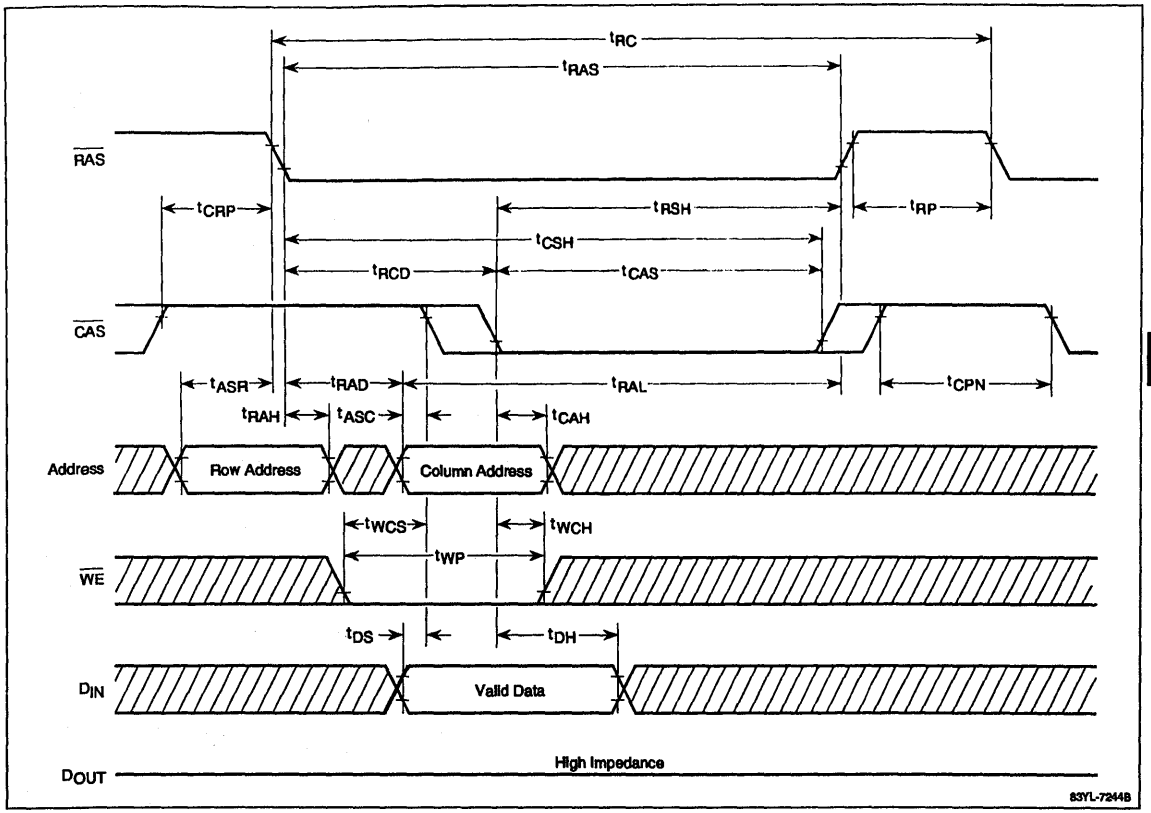
Timing Waveforms

Read Cycle



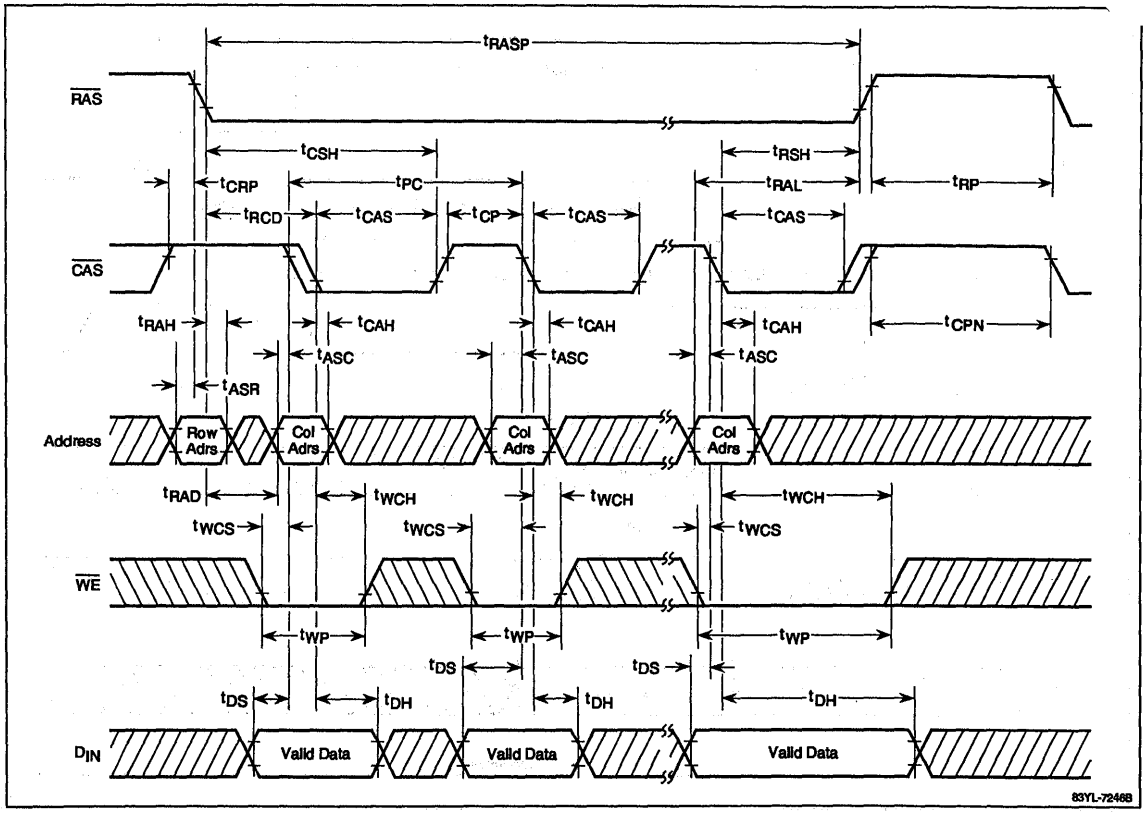
Timing Waveforms (cont)

Early Write Cycle



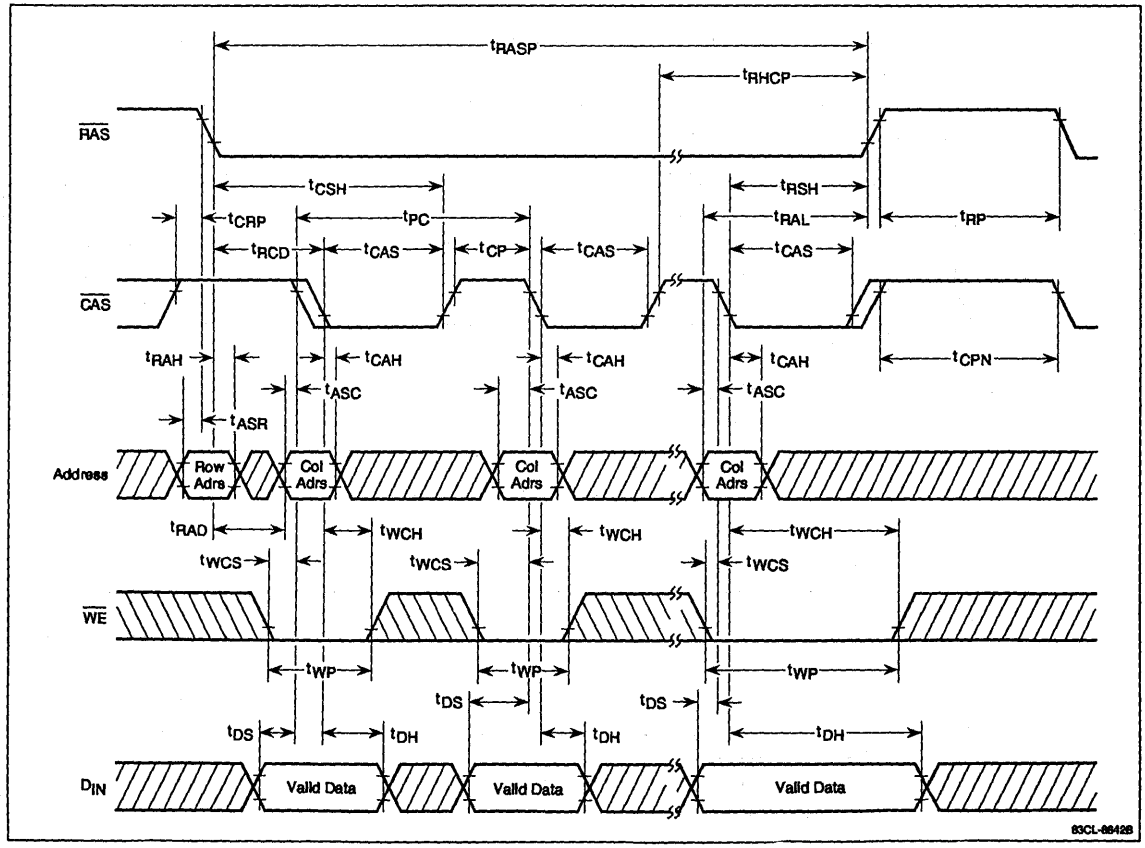
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



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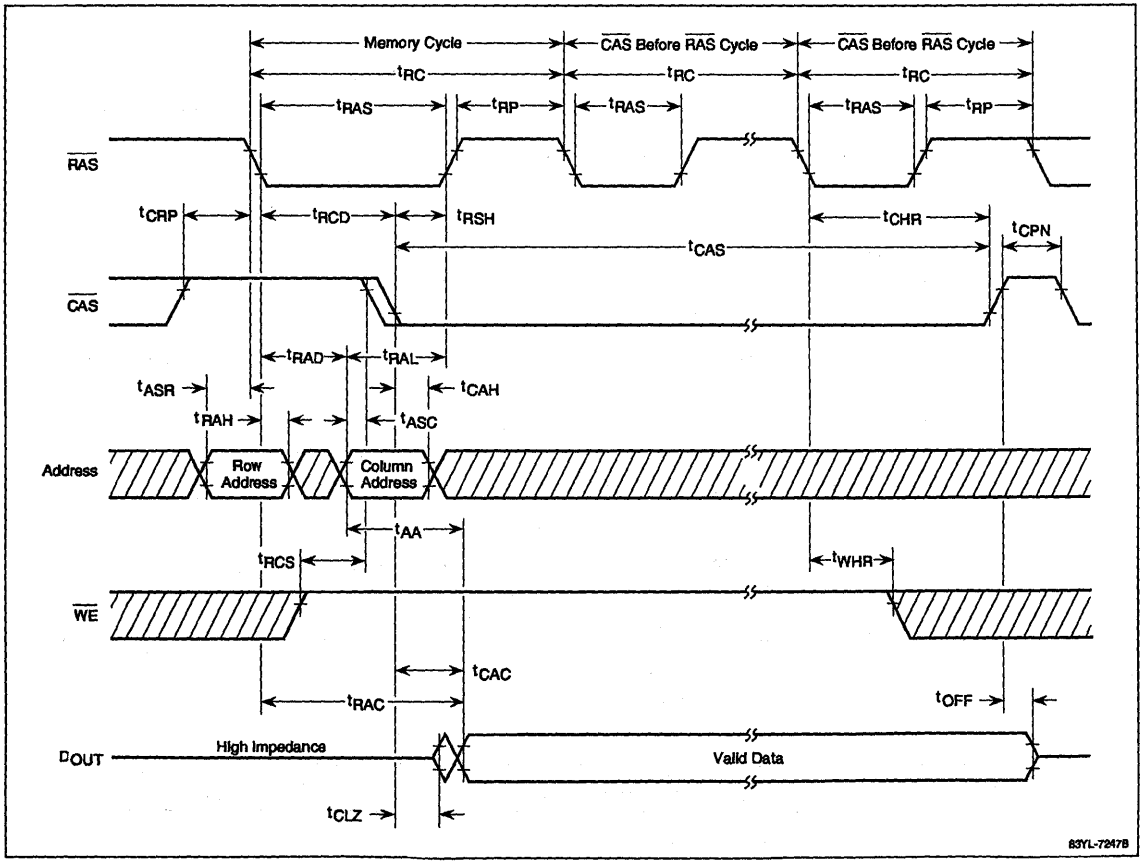
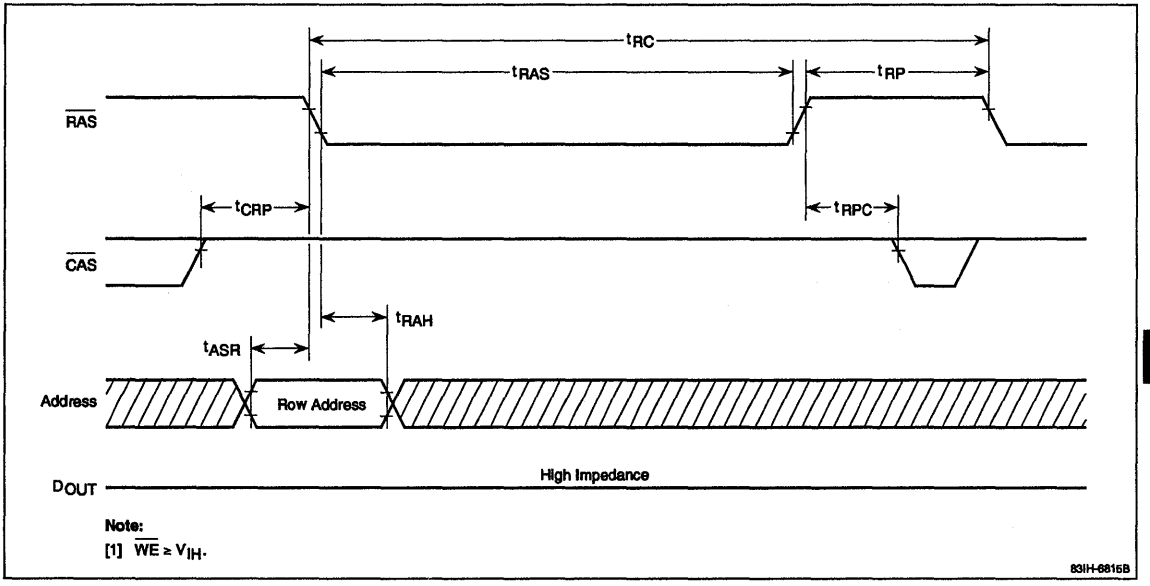
Timing Waveforms (cont)

Hidden Refresh Cycle

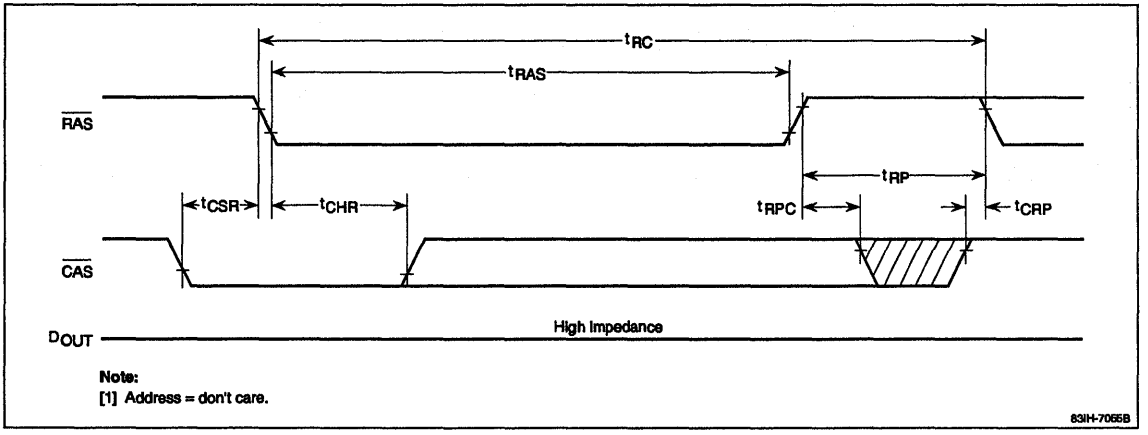


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



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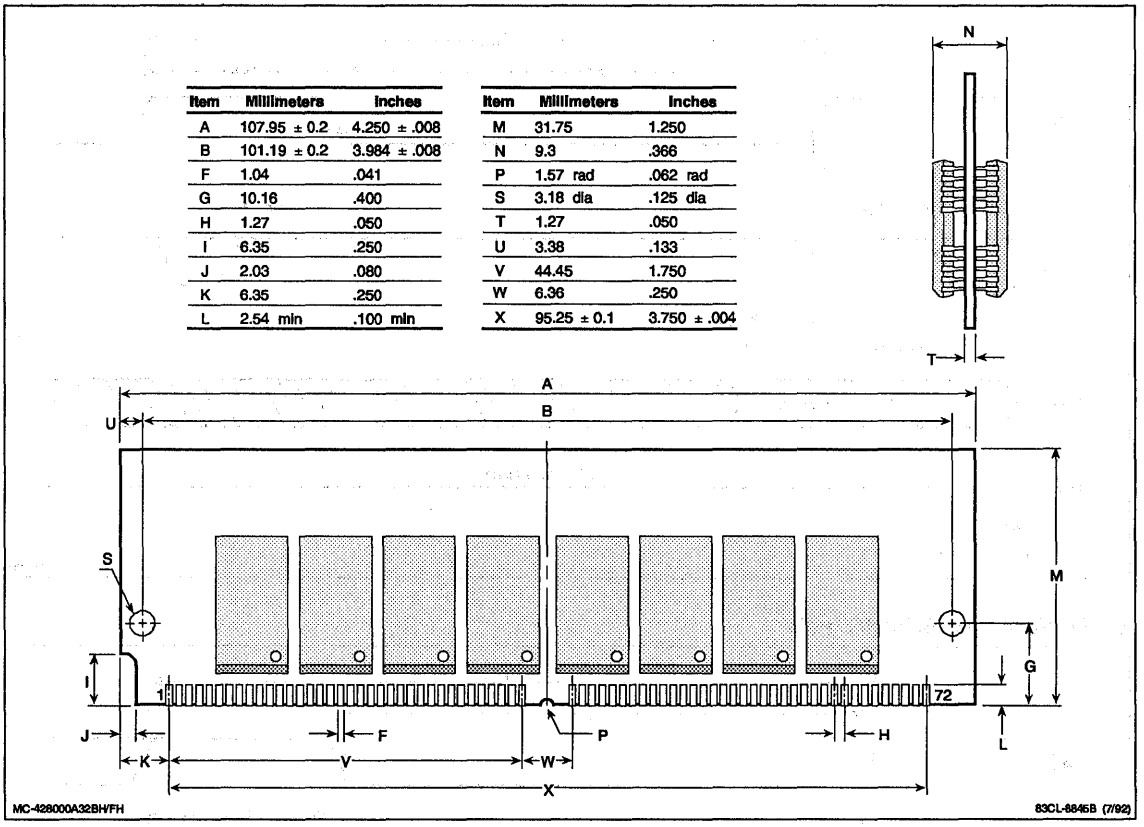
Package Drawings

72-Pin Socket-Mountable SIMM (MC-428000A32BH/FH)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	31.75	1.250
N	9.3	.366
P	1.57 rad	.062 rad
S	3.18 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



MC-428000A36
8,388,608 x 36-Bit
Dynamic CMOS RAM Module

Description

The MC-428000A36 is a fast-page dynamic RAM module organized as 8,388,608 words by 36 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 2048 address combinations of A_0 - A_{10} during a 32-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight, and cost of a system. Each SIMM contains sixteen μPD4217400 DRAMs (4M x 4-bit), eight μPD424100 DRAMs (4M x 1-bit), and 24 power supply decoupling capacitors for noise reduction. DQ_0 - DQ_{35} are common input/output pins.

Features

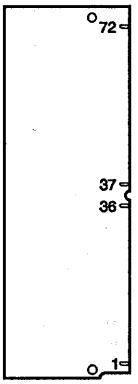
- 8,388,608-word by 36-bit organization
- Single +5-volt power supply
- Fast-page cycles
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 2048 refresh cycles every 32 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

Pin Identification

Name	Function
A_0 - A_{10}	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobes
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS}_0$ - $\overline{RAS}_3$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{18}
4	DQ_1
5	DQ_{19}
6	DQ_2
7	DQ_{20}
8	DQ_3
9	DQ_{21}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6

Pin	Symbol
19	A_{10}
20	DQ_4
21	DQ_{22}
22	DQ_5
23	DQ_{23}
24	DQ_6
25	DQ_{24}
26	DQ_7
27	DQ_{25}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	A_9
33	$\overline{RAS}_3$
34	$\overline{RAS}_2$
35	DQ_{26}
36	DQ_8

Pin	Symbol
37	DQ_{17}
38	DQ_{35}
39	GND
40	$\overline{CAS}_0$
41	$\overline{CAS}_2$
42	$\overline{CAS}_3$
43	$\overline{CAS}_1$
44	$\overline{RAS}_0$
45	$\overline{RAS}_1$
46	NC
47	$\overline{WE}$
48	NC
49	DQ_9
50	DQ_{27}
51	DQ_{10}
52	DQ_{28}
53	DQ_{11}
54	DQ_{29}

Pin	Symbol
55	DQ_{12}
56	DQ_{30}
57	DQ_{13}
58	DQ_{31}
59	V_{CC}
60	DQ_{32}
61	DQ_{14}
62	DQ_{33}
63	DQ_{15}
64	DQ_{34}
65	DQ_{16}
66	NC
67	[Note 1]
68	[Note 1]
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

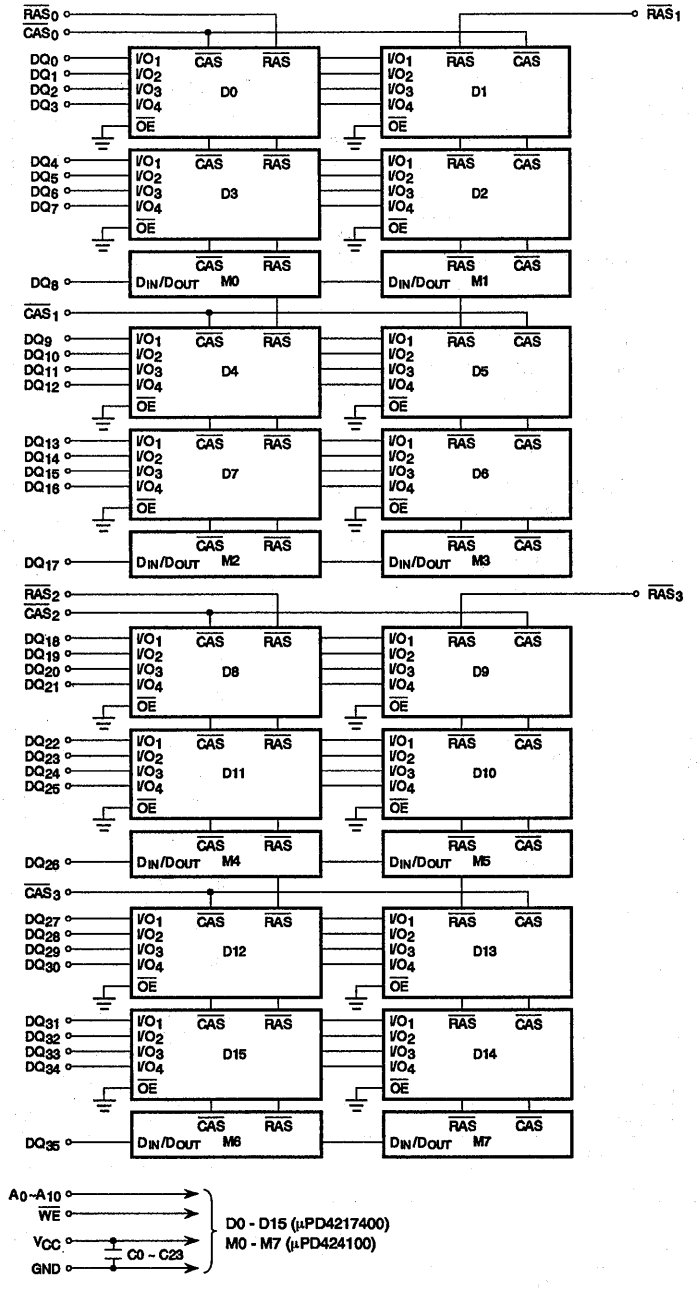
[1] Pins 67-70 are defined by access time:

Pin	60 ns	70 ns	80 ns	100 ns
67	GND	GND	GND	GND
68	NC	NC	NC	NC
69	NC	GND	NC	GND
70	NC	NC	GND	GND

83YL-8581A

SIMM is a trademark of Wang Laboratories.

Connection Diagram



Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-428000A36BH-60	60 ns	72-pin socket-mountable SIMM (solder plating)	31.75 mm (1.250 inch)	9.3 mm (0.366 inch)	Sixteen μPD4217400LE Eight μPD424100LA
BH-70	70 ns				
BH-80	80 ns				
BH-10	100 ns				
MC-428000A36FH-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FH-70	70 ns				
FH-80	80 ns				
FH-10	100 ns				

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	24 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	161	pF	A_0 - A_{10}
	C_{I2}	193	pF	$\overline{WE}$
	C_{I3}	62	pF	$\overline{RAS}$
	C_{I4}	62	pF	$\overline{CAS}$
Input/output capacitance	C_{IO}/C_{OO}	29	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	39	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

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DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		48	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−240	240	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−20	20	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		1420		1260		1140		1020	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1420		1260		1140		1020	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		1060		940		820		700	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1420		1260		1140		1020	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		35		35		45		55	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0	20	0	20	0	20	0	25	ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
Data setup time	t_{CLZ}	0		0		0		0		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 10)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	60	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		32		32		32		32	ms	Addresses A_0 - A_{10}
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		55		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		20		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 14)

AC Characteristics (cont)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

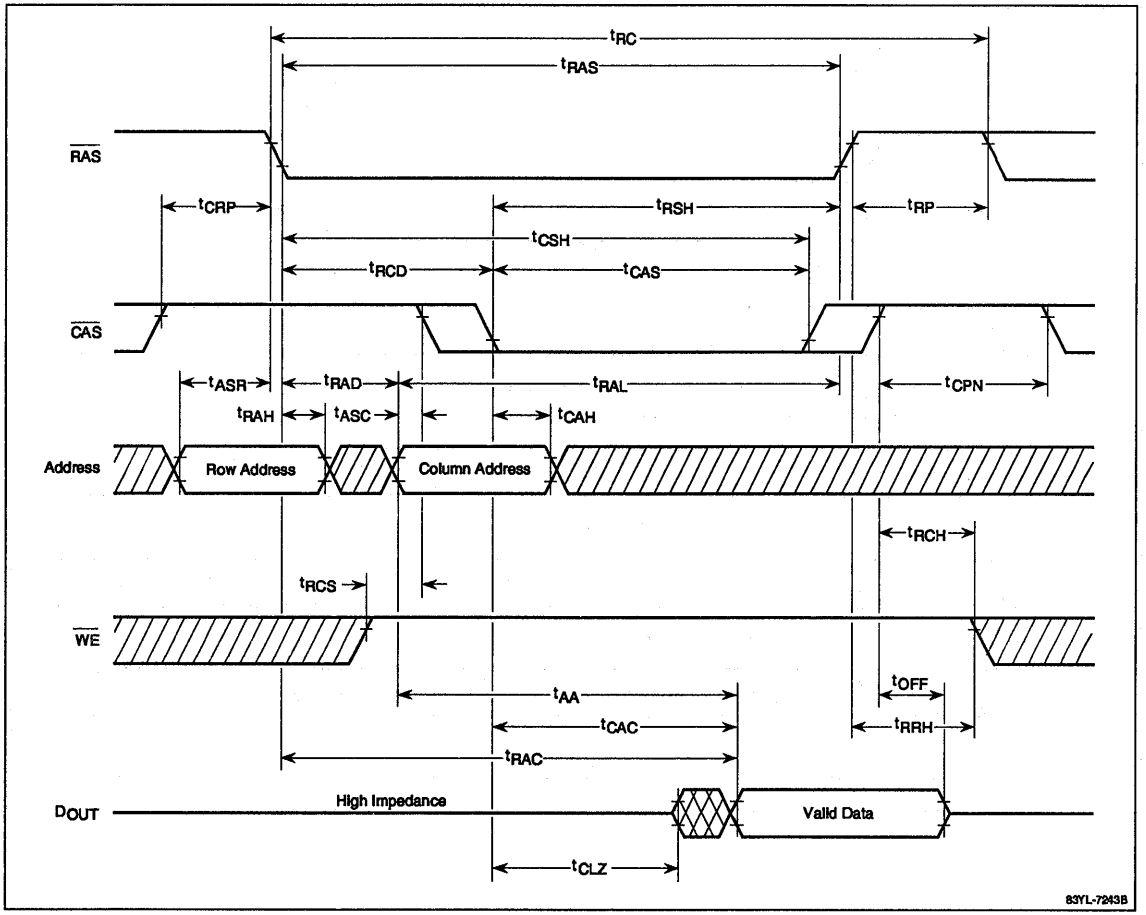
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Timing Waveforms

Read Cycle



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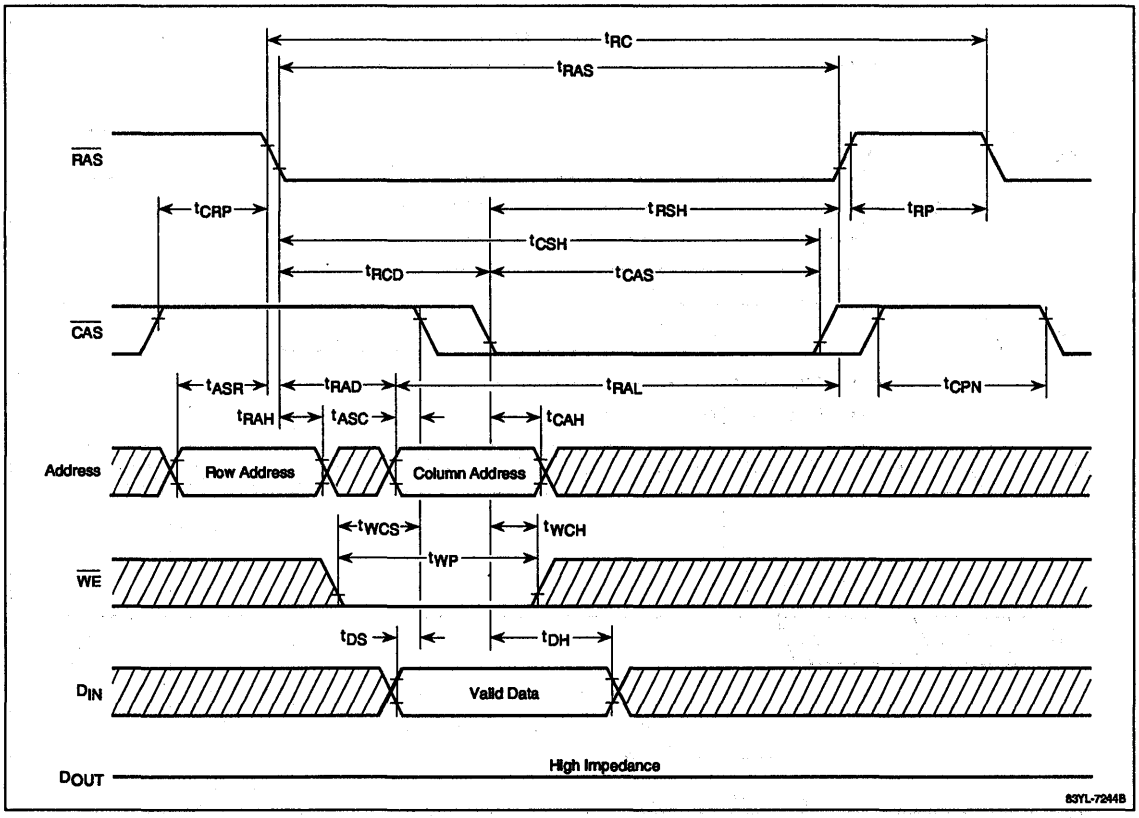
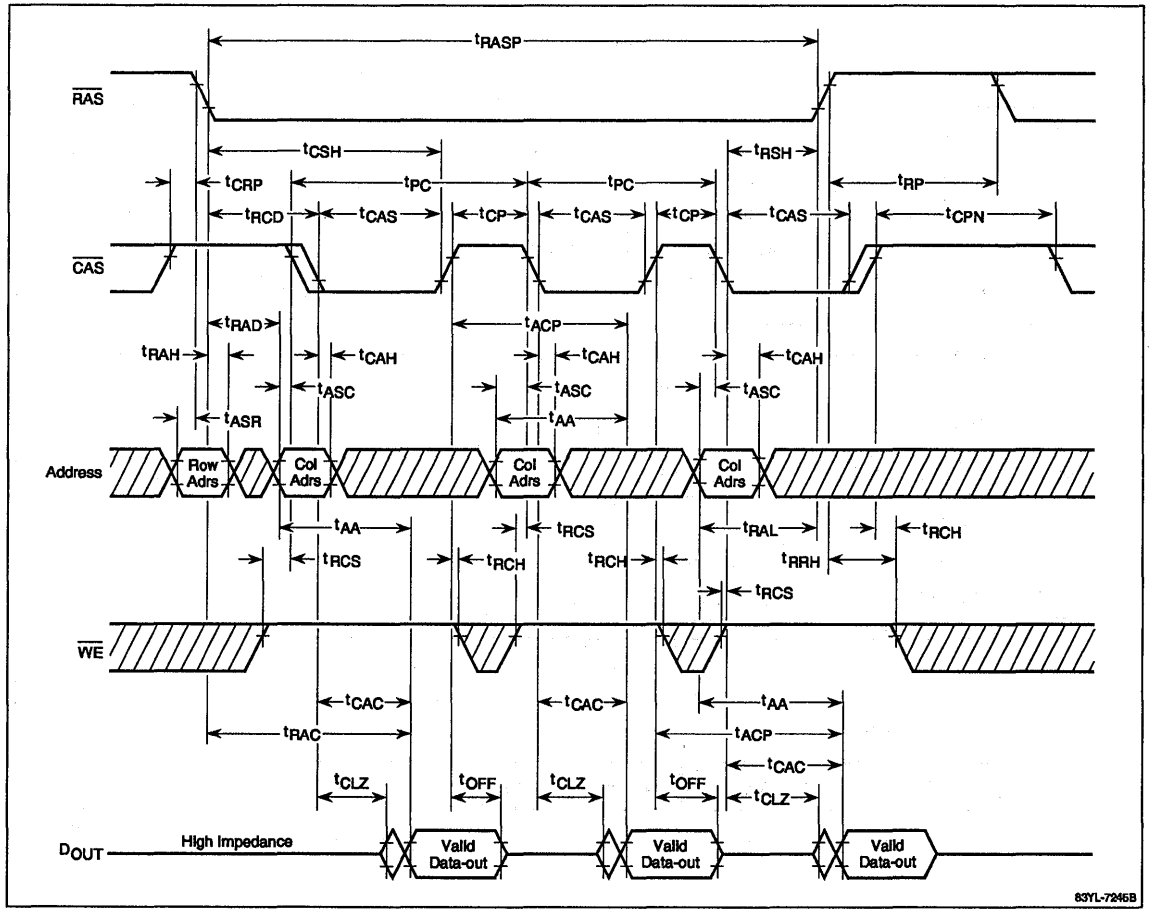
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Fast-Page Read Cycle



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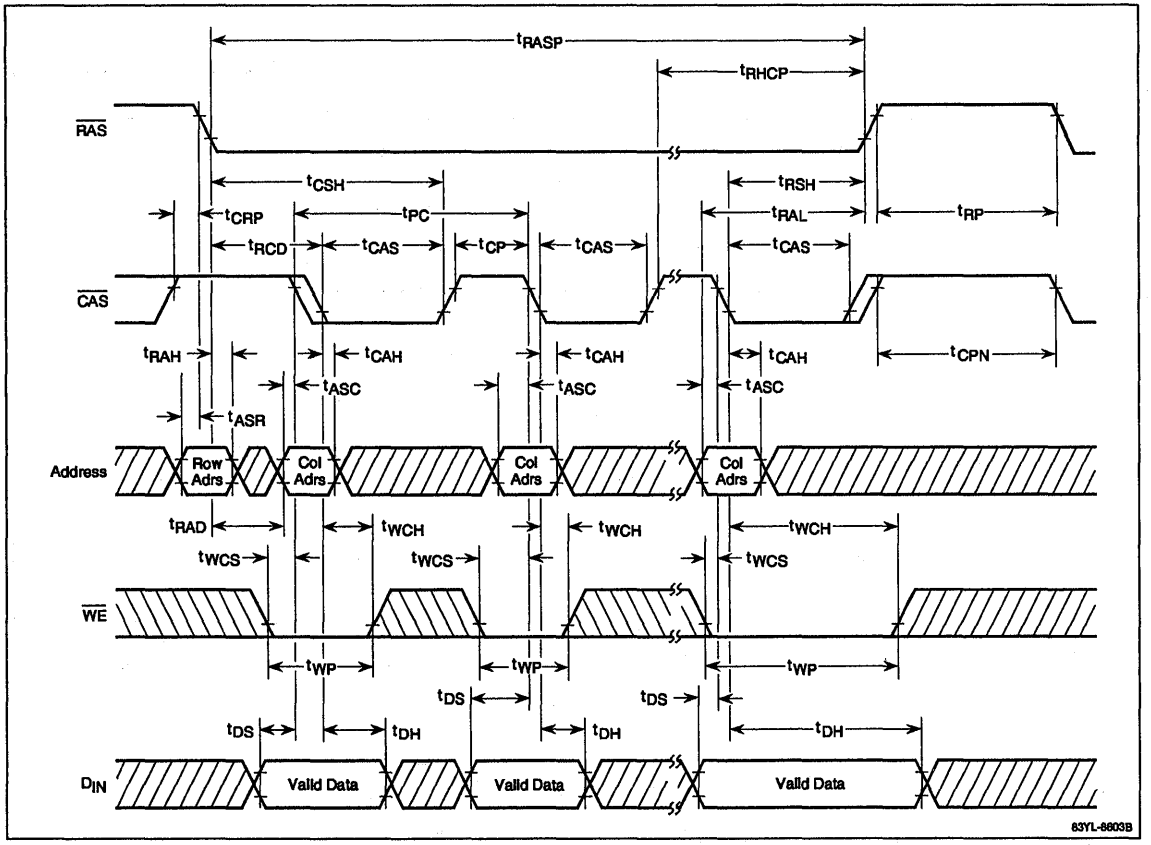
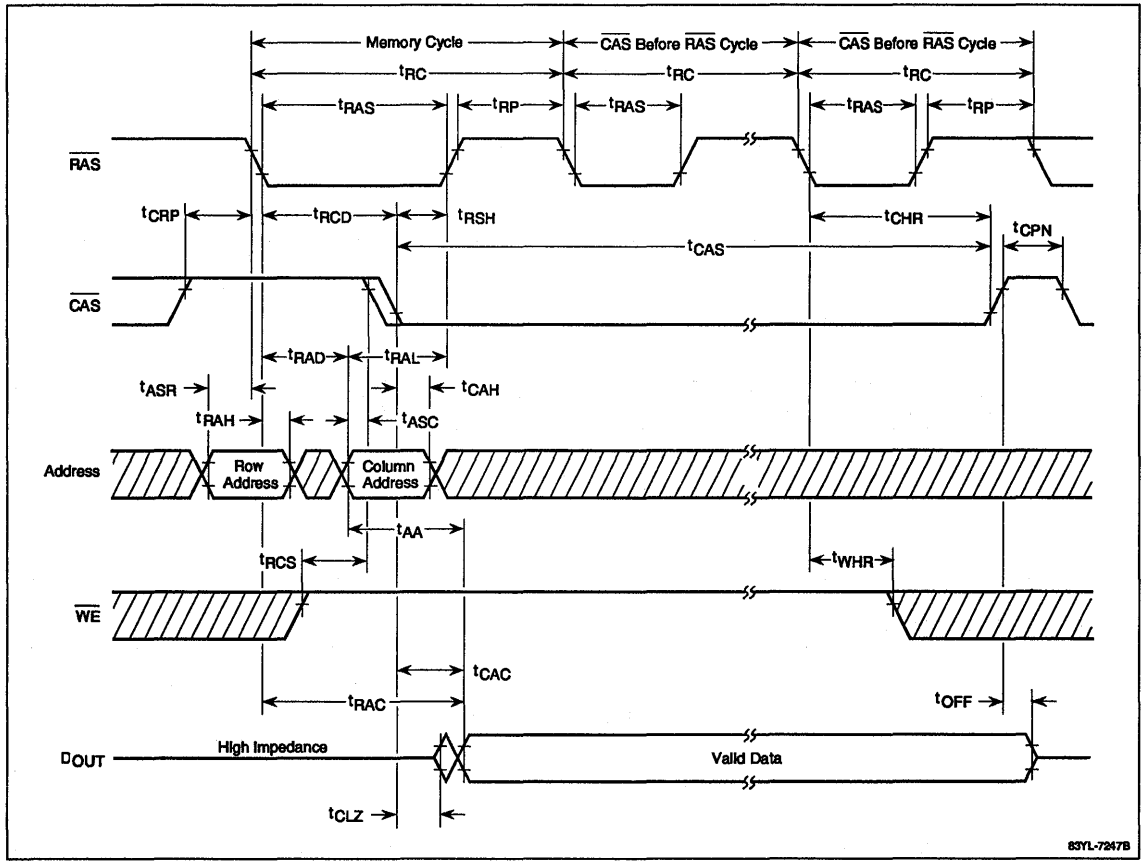
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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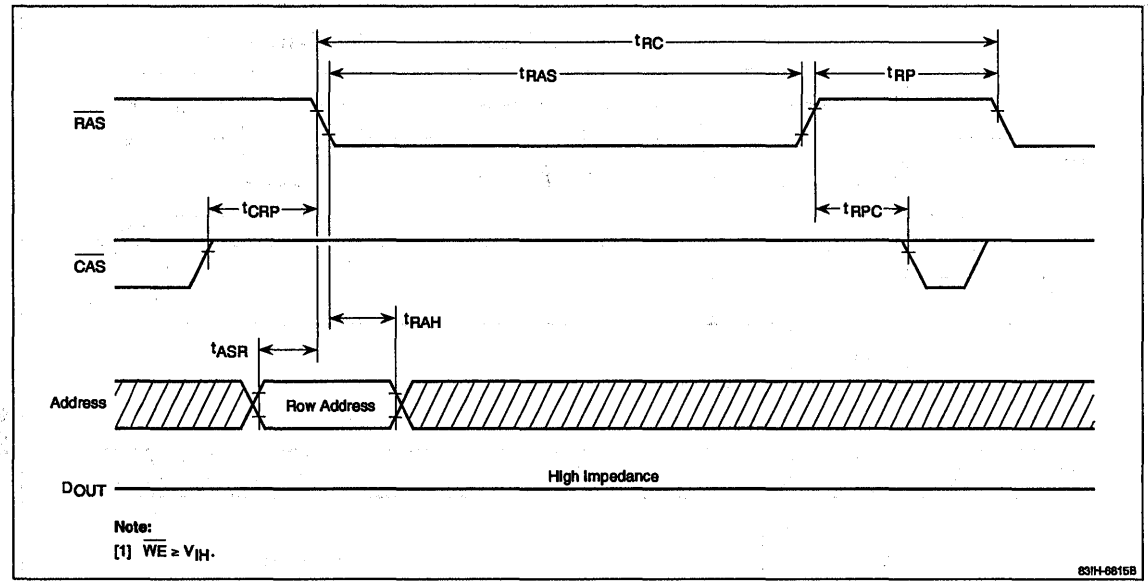
Timing Waveforms (cont)

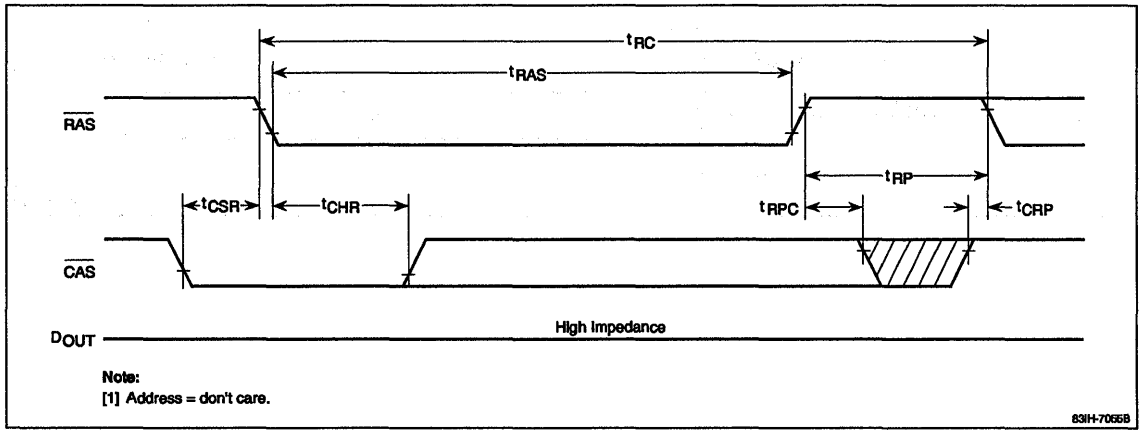
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

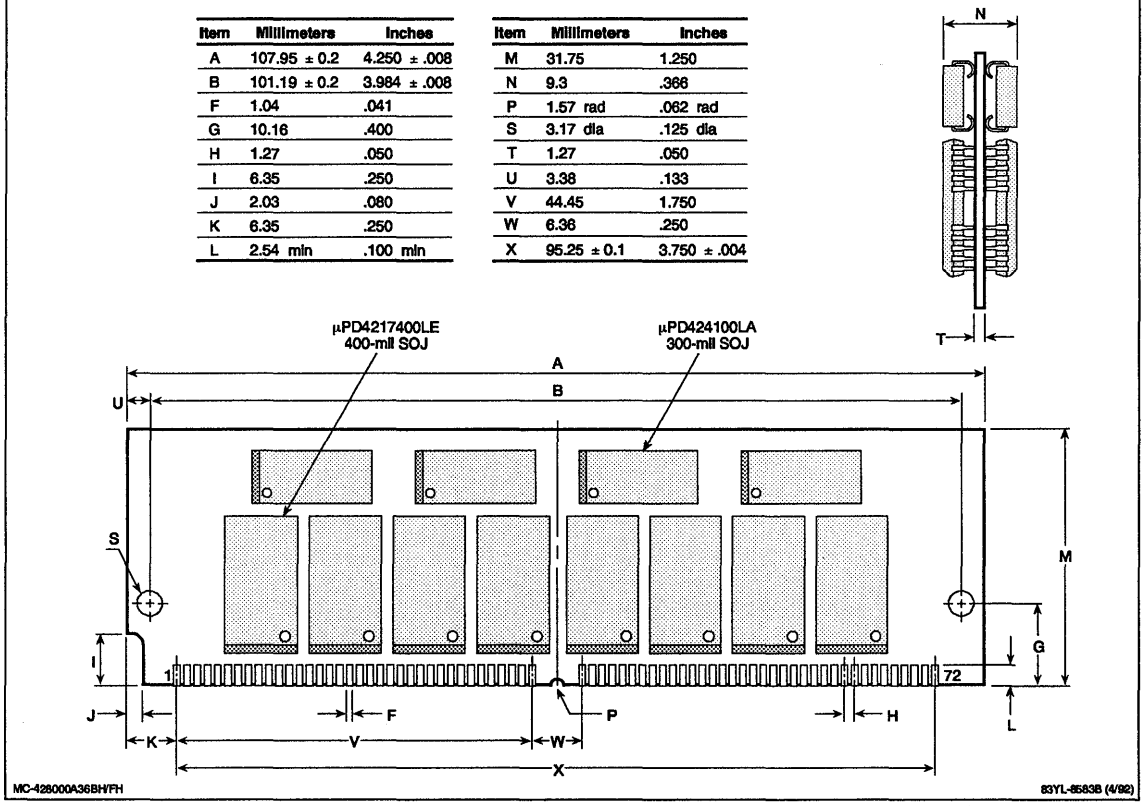
83IH-7066B

Package Drawings

72-Pin Socket-Mountable SIMM (MC-428000A36BH/FH)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	31.75	1.250
N	9.3	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



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NEC

Section 12
Video RAMs

(See App Notes 89-15, 89-16, 90-01.)

μPD	Organization	Features	
41264	64K x 4	Page; NMOS	12a
42264	64K x 4	Page; CMOS	12b
42273	256K x 4		12c
42274	256K x 4	Flash-write	12d
42274-80	256K x 4	Flash-write; high-performance	12e
42275	128K x 8		12f
482234	256K x 8	Fast-page	12g
482235	256K x 8	Hyper-page (extended data out)	

Upcoming Products

Description	Device Number	Comments
4M Video RAM	μPD482445	256K x 16; RAM port access times to 60 ns; serial port access times to 15 ns; 64-pin SSOP, 70-pin TSOP

μPD41264
Dual-Port Graphics Buffer

Description

The μPD41264 is a dual-port graphics buffer equipped with a 64K x 4-bit random access port and a 256 x 4-bit serial read port. The serial read port is connected to an internal 1024-bit data register through a 256 x 4-bit serial read output circuit. The random access port is used by the host CPU to read or write data addressed in any desired order and has a write-per-bit option that allows each of the four data bits to be individually selected or masked for a write cycle.

The μPD41264 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock, while the serial read port continues to operate normally. Following the clock transition of a data transfer, serial read output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

The μPD41264 is fabricated with a double polylayer, N-channel, silicon gate process that provides high storage cell density, high performance, and high reliability. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility. The μPD41264 is available in a 24-pin plastic DIP, or 24-pin plastic ZIP, and is guaranteed for operation at 0 to +70°C.

Features

- Three functional blocks
  - 64K x 4-bit random access storage array
  - 1024-bit data register
  - 256 x 4-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- Single +5-volt ± 10% power supply
- On-chip substrate bias generator
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - Refresh interval: 256 cycles/4 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and page mode capabilities
  - Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - Hidden refreshing by means of $\overline{CAS}$-controlled output
  - Write-per-bit capability
  - Write bit selection multiplexed on IO_0-IO_3
- $\overline{RAS}$-activated data transfer
  - Same cycle time as for random access
  - Row data transferred to data register as specified by row address inputs
  - Starting location of following serial read operation specified by column address inputs
  - Transfer of 1024 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
  - Serial data presented on SO_0-SO_3
  - Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- 24-pin plastic DIP and 24-pin plastic ZIP packaging

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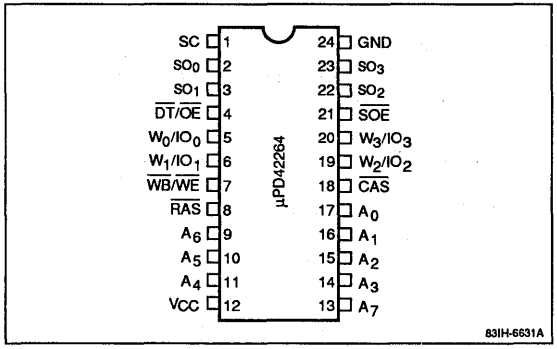
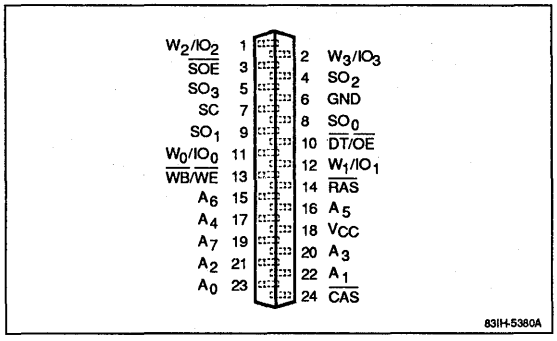
Pin Configurations

24-Pin Plastic DIP and SOJ



24-Pin Plastic ZIP



Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD41264C-12	120 ns	40 ns	24-pin plastic DIP
C-15	150 ns	60 ns	
μPD41264V-12	120 ns	40 ns	24-pin plastic ZIP
V-15	150 ns	60 ns	

Pin Identification

Symbol	Function
A_0 - A_7	Address inputs
$\overline{CAS}$	Column address strobe
$\overline{DT/OE}$	Data transfer/output enable
$\overline{RAS}$	Row address strobe
SC	Serial control
SO_0 - SO_3	Serial read outputs
$\overline{SOE}$	Serial output enable
W_0/IO_0 - W_3/IO_3	Write-per-bit inputs/data inputs and outputs
GND	Ground
$\overline{WB/WE}$	Write-per-bit/write enable
V_{CC}	+5-volt power supply

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Operating temperature	T_A	0		70	°C

Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 V to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 - A_7
	$C_{I(\overline{DT}/\overline{OE})}$	6	pF	$\overline{DT}/\overline{OE}$
	$C_{I(\overline{WB}/\overline{WE})}$	8	pF	$\overline{WB}/\overline{WE}$
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 - W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 - SO_3

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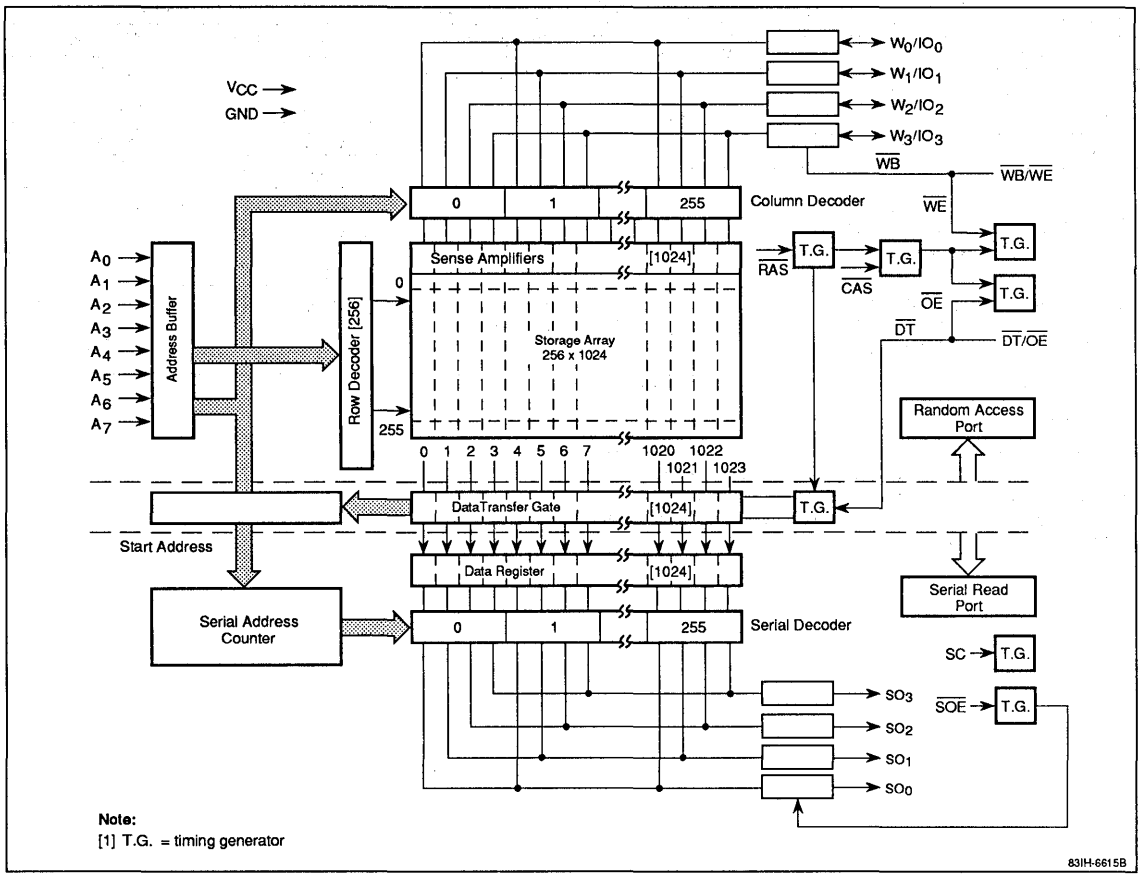
Block Diagram



Note:
[1] T.G. = timing generator

83IH-6615B

Device Operation

The μPD41264 has a random access port and a serial read port. The random access port executes standard read/write cycles as well as data transfer cycles, all of which are based on conventional $\overline{RAS}/\overline{CAS}$ timing. In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to the corresponding register location. The serial read port shows the contents of the data register in serial order. The random access and serial read ports can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is a 256-row by 1024-column matrix. Each of 4 data bits in the random access port corresponds to 65,536 storage cells, and 16 address bits are required to decode one cell location. Eight row address bits are set up on pins A_0 through A_7 and latched onto the chip by $\overline{RAS}$. Eight column address bits then are set up on pins A_0 through A_7 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ is similar to a chip enable signal; whenever it is activated, 1024 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ is a chip selection signal that activates the column decoder and input/output buffers.

Through 1 of 256 column decoders, 4 storage cells on a row are connected to 4 data buses, respectively. In a data transfer cycle, 8 row address bits are used to select 1 of the 256 possible rows involved in the transfer of data to the data register. Eight column address bits are then used to select the 1 of 256 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 4 data bits in the 1024-bit data register are transferred to 4 serial data buses and read out. Activating SC repeatedly causes a serial read cycle (starting from the location specified in the data transfer) to be executed within the 1024 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following functions are multi-plexed in the random access port:

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

The $\overline{OE}$, $\overline{WE}$ and IO_i functions represent standard operations while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$. The $\overline{DT}$ level determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit option is used. W_i defines data bits to be written with the write-per-bit capability. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD41264 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 1024-bit data register from the corresponding 1024-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 1024 data transfer gates and transfer data from one of the rows to the data register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and maintaining $(\overline{WB}/)\overline{WE}$ high while $\overline{CAS}$ is active. The $(W_i/)IO_i$ data pin (i = 0, 1, 2, 3) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, is the longest of the following three calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$ to $\overline{CAS}$ and $\overline{RAS}$ to $\overline{OE}$ delays are system-dependent timing parameters.

Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ high returns the output to high impedance.

Write Cycle. A write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes the data on (W_i/)IO_i into the on-chip data latch. To make use of the write-per-bit capability, $\overline{WB}$/($\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case, data bits targeted for write operation can be specified by keeping W_i(/IO_i) high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

For those data bits of W_i(/IO_i) that are kept low as $\overline{RAS}$ falls, write operation is inhibited on the chip. If $\overline{WB}$/($\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit option is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low before $\overline{CAS}$. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, ($\overline{DT}$/)$\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$, but otherwise ($\overline{DT}$/)$\overline{OE}$ does not affect any circuit operation while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. Bringing the ($\overline{WB}$/)$\overline{WE}$ signal low with $\overline{RAS}$ and $\overline{CAS}$ low executes this cycle. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i is returned to high impedance by a high ($\overline{DT}$/)$\overline{OE}$. The data to be written is strobed by ($\overline{WB}$/)$\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of ($\overline{DT}$/)$\overline{OE}$, which can be activated just after ($\overline{WB}$/)$\overline{WE}$ falls, even when ($\overline{WB}$/)$\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 256 row addresses (A_0 through A_7) will refresh all storage cells. Any cycle in the random access port (i.e., read, write, refresh, or data transfer) refreshes the 1024 bits selected by the $\overline{RAS}$ addresses or by the on-chip refresh address counter.

$\overline{RAS}$-only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep (W_i/)IO_i in a state of high impedance. This cycle is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal address counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This function performs hidden refreshing after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharging. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held low instead of high) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. By maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed, data is transferred at a faster rate because $\overline{RAS}$ addresses are maintained internally and do not have to be reapplied. During this operation, it is also possible to execute read, write and read-write/read-modify-write cycles. Additionally, the write-per-bit control specified in the entry write cycle is maintained through the following fast-page write cycle.

Data Transfer Cycle. A data transfer cycle is executed by bringing $\overline{DT}(/\overline{OE})$ low as $\overline{RAS}$ falls. The specified 1 of the possible 256 rows involved in the data transfer, aswell as the starting location of the following serial read cycle in the serial read port, are defined by address inputs. $\overline{DT}(/\overline{OE})$ must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$, so that the data transfer condition may be satisfied . The low-to-high transition of $\overline{DT}$ causes two transfer operations through the data transfer gates: column address buffer outputs are transferred to the serial address counters, and storage cell data amplified on digit lines is transferred to the data register. At least one SC cycle is required to hold the data in the register. Otherwise, the beginning of the next transfer cycle destroys the newly transferred data. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the transferred data in the random access port.

Serial Read Port

The serial read port is used only to read serially the contents of the data register starting from a specified location. The entire operation, therefore, follows a data transfer cycle. Data stored in the serial register remains valid for a minimum of 4 ms after the transfer cycle. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}(/\overline{OE})$ must occur within a specified period in an SC cycle. Except for this SC cycle, the serial read port can operate asynchronously with the random access port. The output data appears at SO_i after an access time of t_{SCA}, measured from SC high, only when $\overline{SOE}$ is maintained low. The SC cycle that includes the positive transition of $\overline{DT}(/\overline{OE})$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD41264 graphics buffers into the same external circuitry. When $\overline{SOE}$ is low, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is at a high logic level, SO_i is disabled and in a state of high impedance.

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DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −2 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −2 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 4.2 mA

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Random Access Port	Serial Read Port	Symbol	-12 Max	-15 Max	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	95	85	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; IO = 0 mA; SC = $\overline{SOE}$ = V_{IH} (Note 1)
Standby	Standby	I_{CC2}	12	12	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance; SC = $\overline{SOE}$ = V_{IH}
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	75	65	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; SC = $\overline{SOE}$ = V_{IH}
Page cycle	Standby	I_{CC4}	65	55	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; SC = $\overline{SOE}$ = V_{IH} (Note 1)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	75	65	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; SC = $\overline{SOE}$ = V_{IH} (Note 1)
Data transfer	Standby	I_{CC6}	120	100	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; SC = $\overline{SOE}$ = V_{IH}
Read/write cycle	Active	I_{CC7}	155	130	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
Standby	Active	I_{CC8}	60	45	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	135	110	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
Page cycle	Active	I_{CC10}	125	100	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	135	110	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
Data transfer	Active	I_{CC12}	180	145	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, and I_{CC6}, real values depend on output loading and cycle rates.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V±10%

Parameter	Symbol	μPD41264-12 Min	μPD41264-12 Max	μPD41264-15 Min	μPD41264-15 Max	Unit	Test Conditions
Column address hold time after $\overline{RAS}$ low	t_{AR}	80		100		ns	
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 2, 5)
Column address hold time	t_{CAH}	20		25		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	ns	

AC Characteristics (cont)

Parameter	Symbol	μPD41264-12 Min	μPD41264-12 Max	μPD41264-15 Min	μPD41264-15 Max	Unit	Test Conditions
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{CDH}	40		55		ns	(Note 12)
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	25		30		ns	
$\overline{CAS}$ precharge time (page cycle only)	t_{CP}	50		60		ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	25		30		ns	
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	100		120		ns	(Note 10)
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in hold time	t_{DH}	35		45		ns	(Note 11)
$\overline{DT}$ high hold time	t_{DHH}	20		25		ns	
Data-in hold time after $\overline{RAS}$ low	t_{DHR}	95		120		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		ns	
$\overline{DT}$ low setup time	t_{DLS}	0		0		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 11)
$\overline{DT}$ high to $\overline{CAS}$ high delay	t_{DTC}	10		10		ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	20		25		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	10		10		ns	
$\overline{OE}$ pulse width	t_{OE}	35		40		ns	
Access time from $\overline{OE}$	t_{OEA}		30		40	ns	(Note 2)
$\overline{OE}$ to data-in setup delay	t_{OED}	35		40		ns	
$\overline{OE}$ hold time after $\overline{WE}$ low	t_{OEH}	30		40		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		ns	
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	30	0	40	ns	(Note 6)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	30	0	40	ns	(Note 6)
Page cycle time	t_{PC}	120		145		ns	
Access time from $\overline{RAS}$	t_{RAC}		120		150	nc	(Notes 2, 4)
Row address hold time	t_{RAH}	15		20		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	ns	
Random read or write cycle time	t_{RC}	220		270		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	30	75	ns	(Note 4)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns	(Note 9)
Read command setup time	t_{RCS}	0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low (serial port active)	t_{RDH}	100		130		ns	
Refresh interval	t_{REF}		4		4	ms	
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		ns	
Read command hold after $\overline{RAS}$ high	t_{RRH}	20		20		ns	(Note 9)
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	

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AC Characteristics (cont)

Parameter	Symbol	μPD41264-12 Min	μPD41264-12 Max	μPD41264-15 Min	μPD41264-15 Max	Unit	Test Conditions
Read-write/read-modify-write cycle time	t_{RWC}	300		355		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	160		195		ns	(Note 10)
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
SC pulse width	t_{SCH}	10		20		ns	
Serial output access time from SC	t_{SCA}		40		60	ns	(Notes 2, 7)
Serial clock cycle time	t_{SCC}	40	50,000	60	50,000	ns	
SC precharge time	t_{SCL}	10		20		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	10		20		ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	10		20		ns	
Serial output access time from $\overline{SOE}$	t_{SOA}		35		50	ns	
$\overline{SOE}$ pulse width	t_{SOE}	15		20		ns	
Serial output hold time after SC high	t_{SOH}	10		10		ns	
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		ns	
$\overline{SOE}$ precharge time	t_{SOP}	15		20		ns	
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	30	0	40	ns	(Note 6)
Rise and fall transition time	t_T	3	50	3	50	ns	
Write-per-bit hold time	t_{WBH}	20		25		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	
Write command hold time	t_{WCH}	35		45		ns	
Write command hold time after $\overline{RAS}$ low	t_{WCR}	95		120		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 10)
Write bit selection hold time	t_{WH}	20		25		ns	
Write command pulse width	t_{WP}	35		45		ns	
Write bit selection setup time	t_{WS}	0		0		ns	

Notes:

(1) See input/output timing waveforms for timing reference voltages.

(2) See figures 1 and 2 for output loads.

(3) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles (except $\overline{CAS}$-before-$\overline{RAS}$ cycles), before proper device operation is achieved.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.

(5) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(6) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(7) Data in the serial output register remains valid for 4 ms (min) after a data transfer cycle.

(8) V_{IH} (min) and V_{IL} (min) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(9) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(10) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(11) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of (WB/)$\overline{WE}$ in delayed write or read-modify-write cycles.

(12) Use t_{RDH} and t_{CDH} when the serial port is active and t_{RDH1}, t_{RSD}, t_{CSD} and t_{SSC} if it is in standby.

(13) $\overline{SOE}$ may be tied to GND if the output enable function of the serial port is not needed.

Figure 1. Input Timing

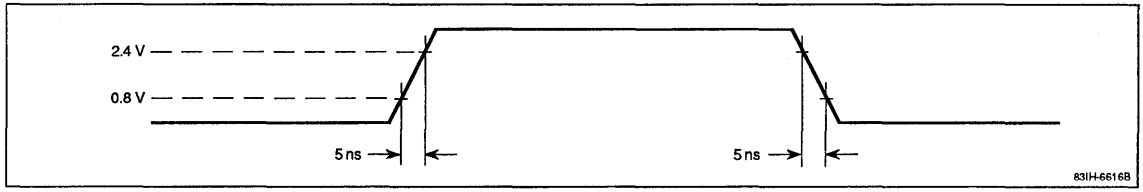


Figure 2. Output Timing

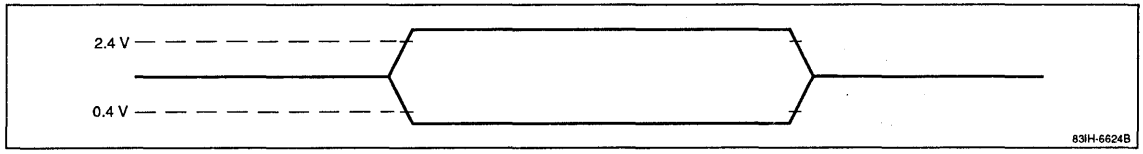


Figure 3. Output Loading in Random Access Port

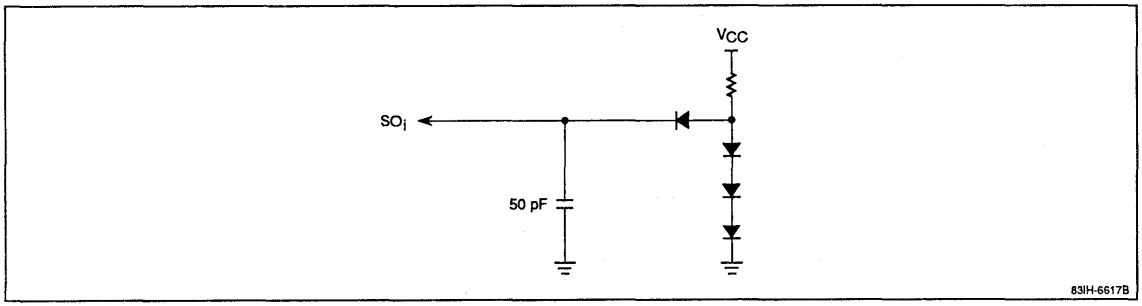
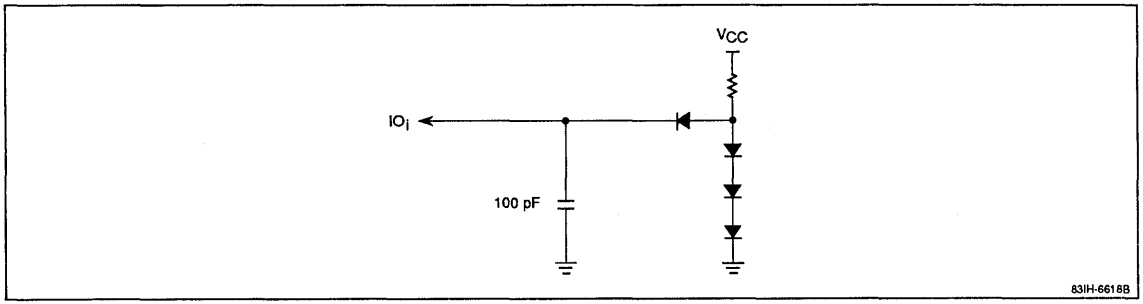


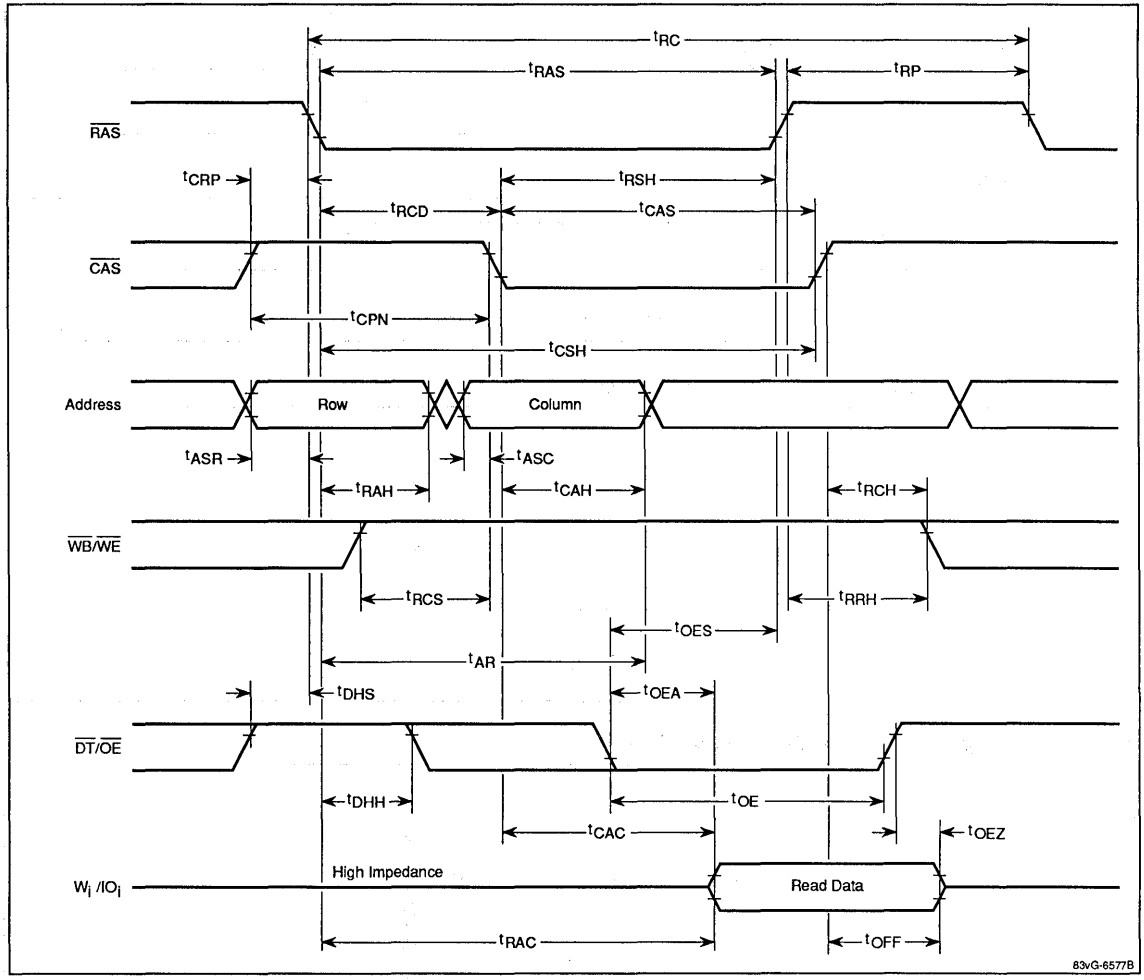
Figure 4. Output Loading in Serial Read Port



12a

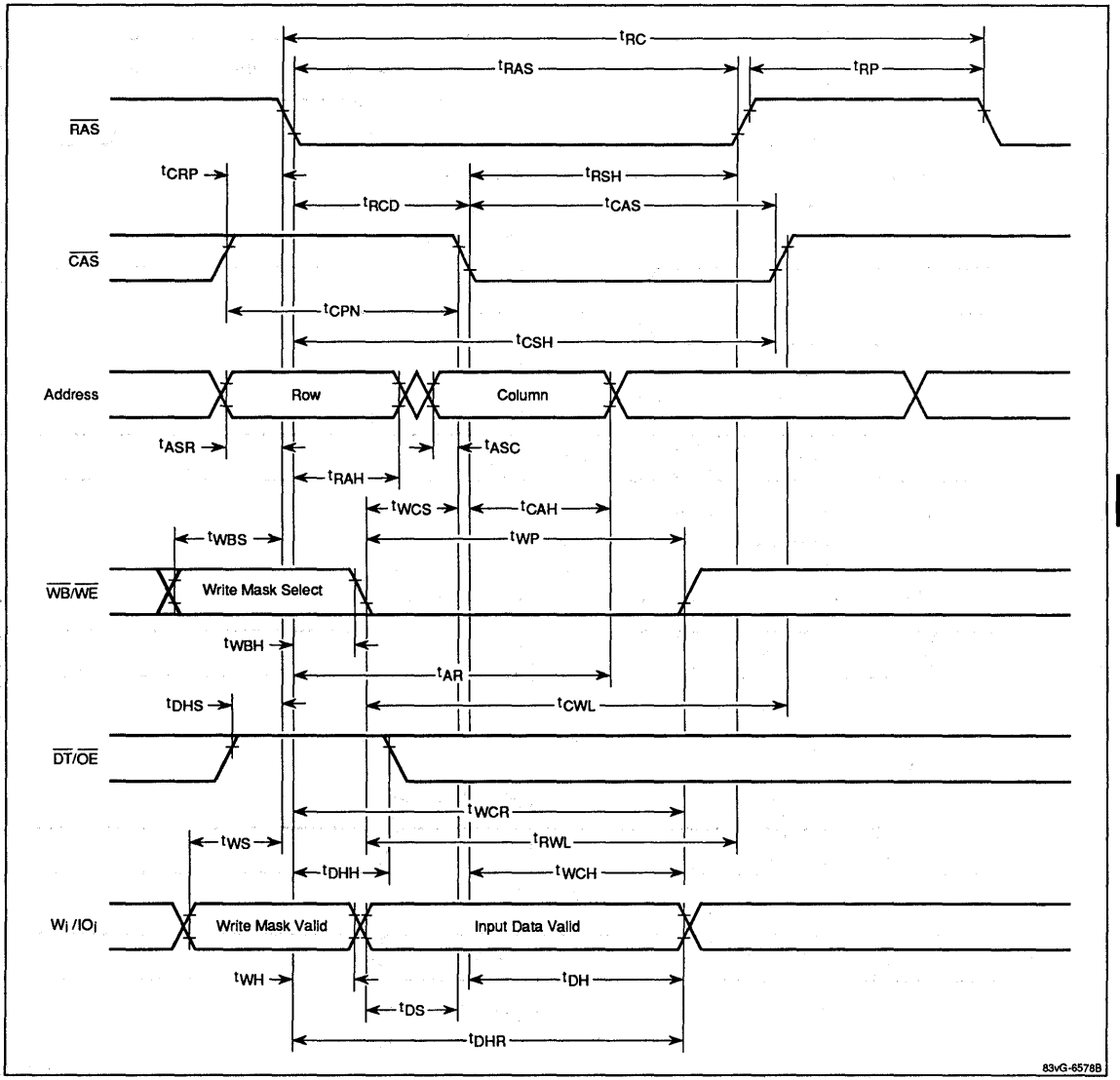
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

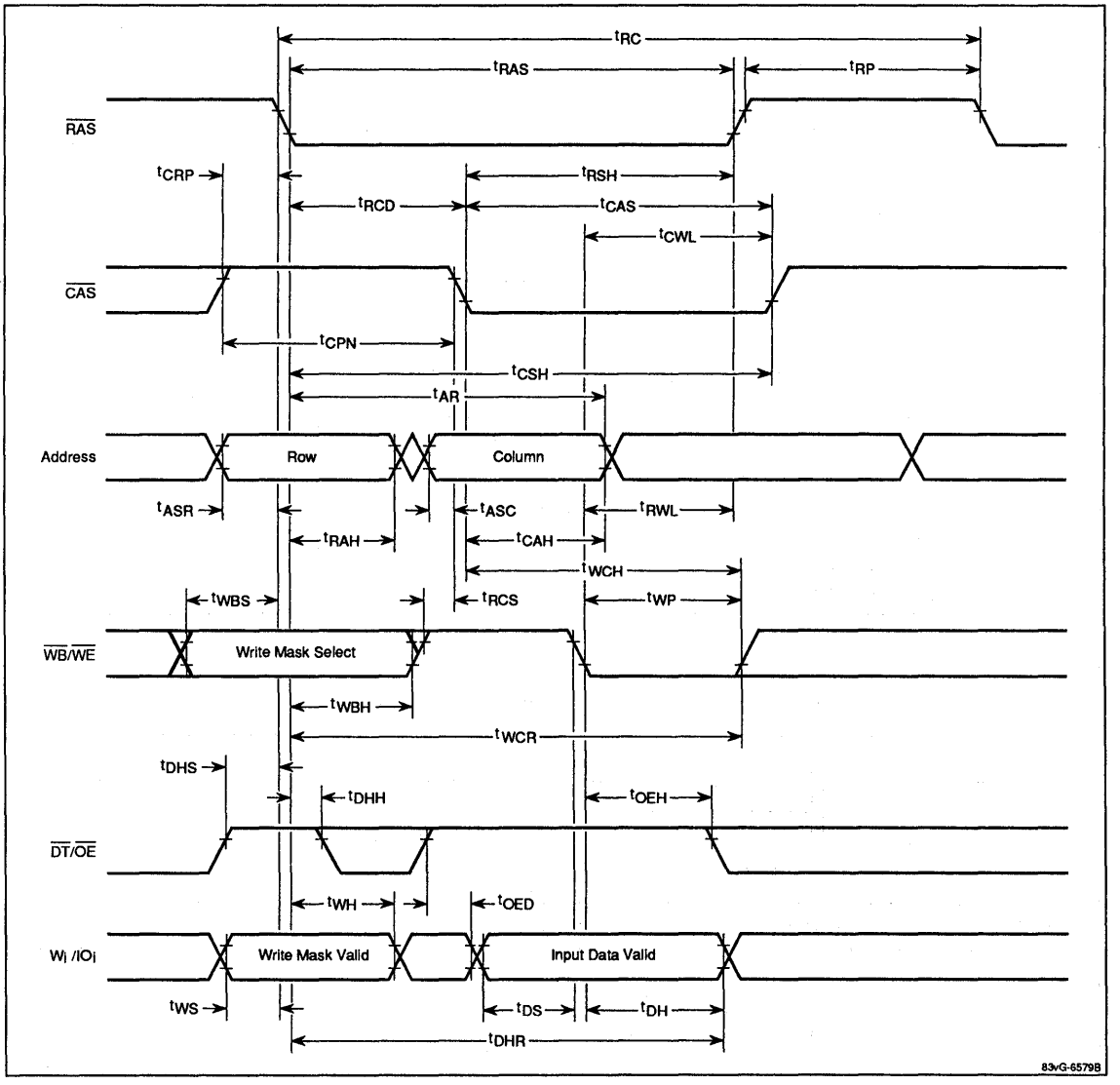
Early Write Cycle



12a

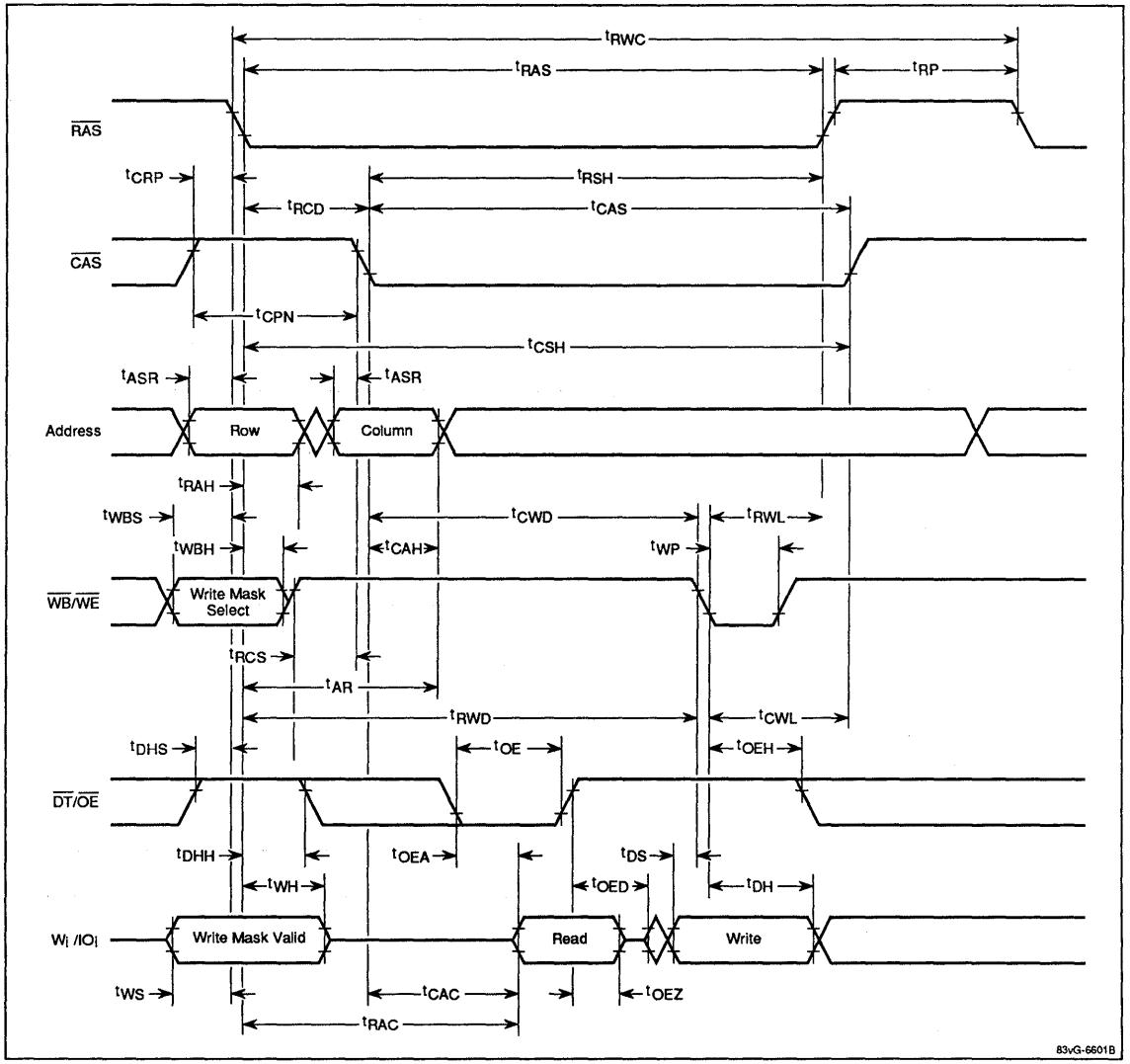
Timing Waveforms (cont)

Late Write Cycle



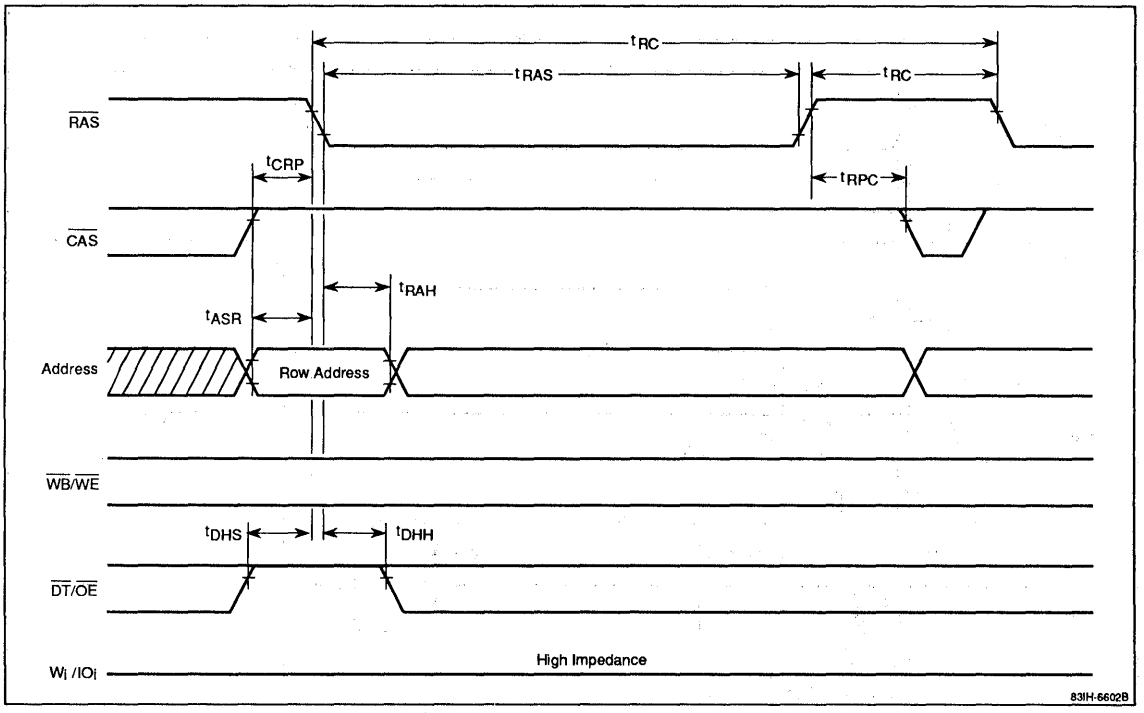
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle

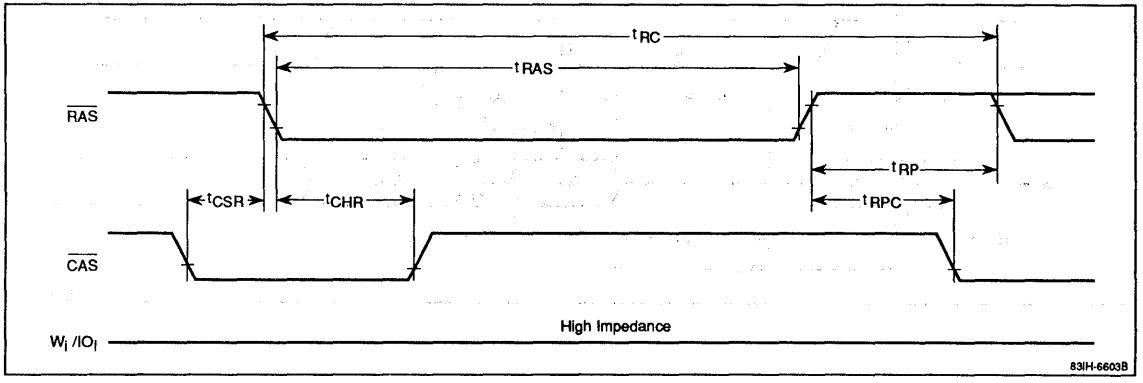


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle

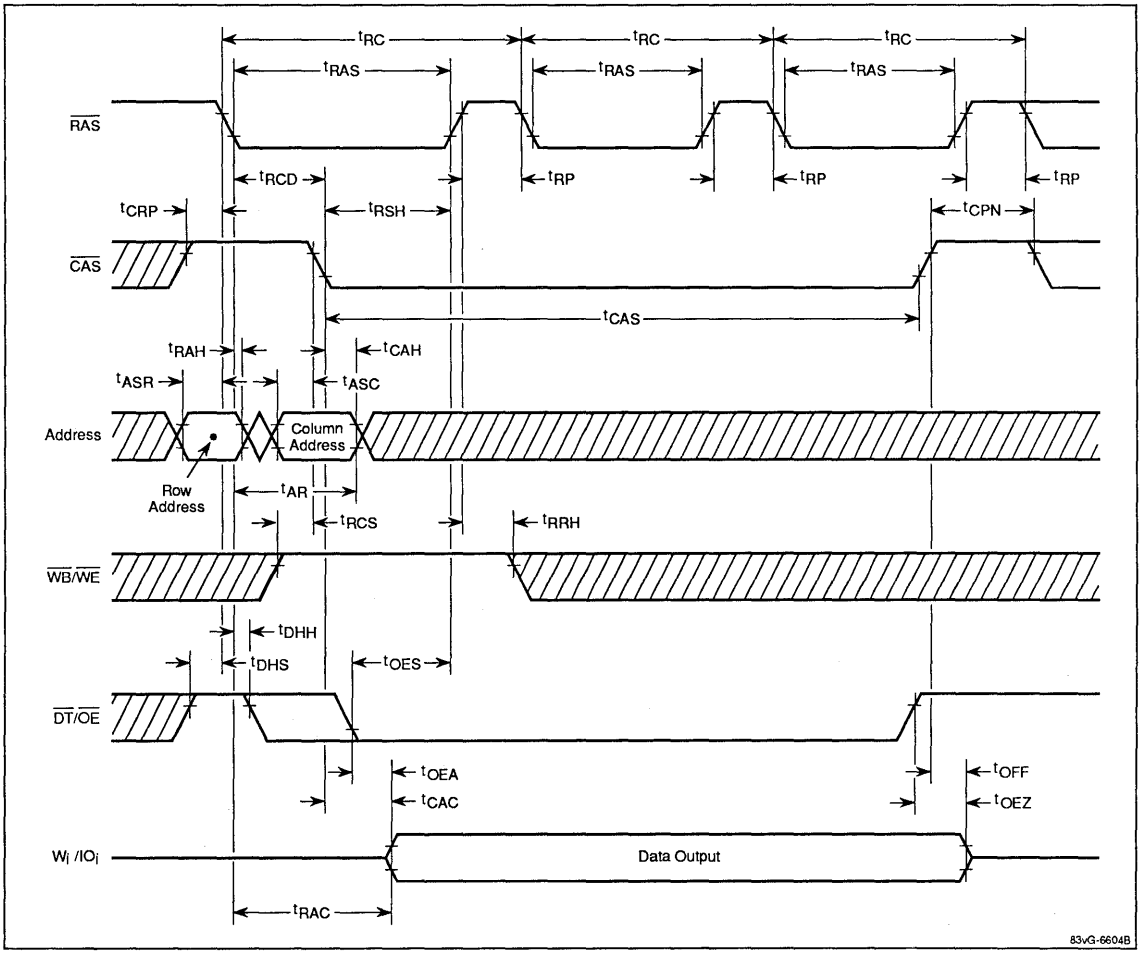


$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



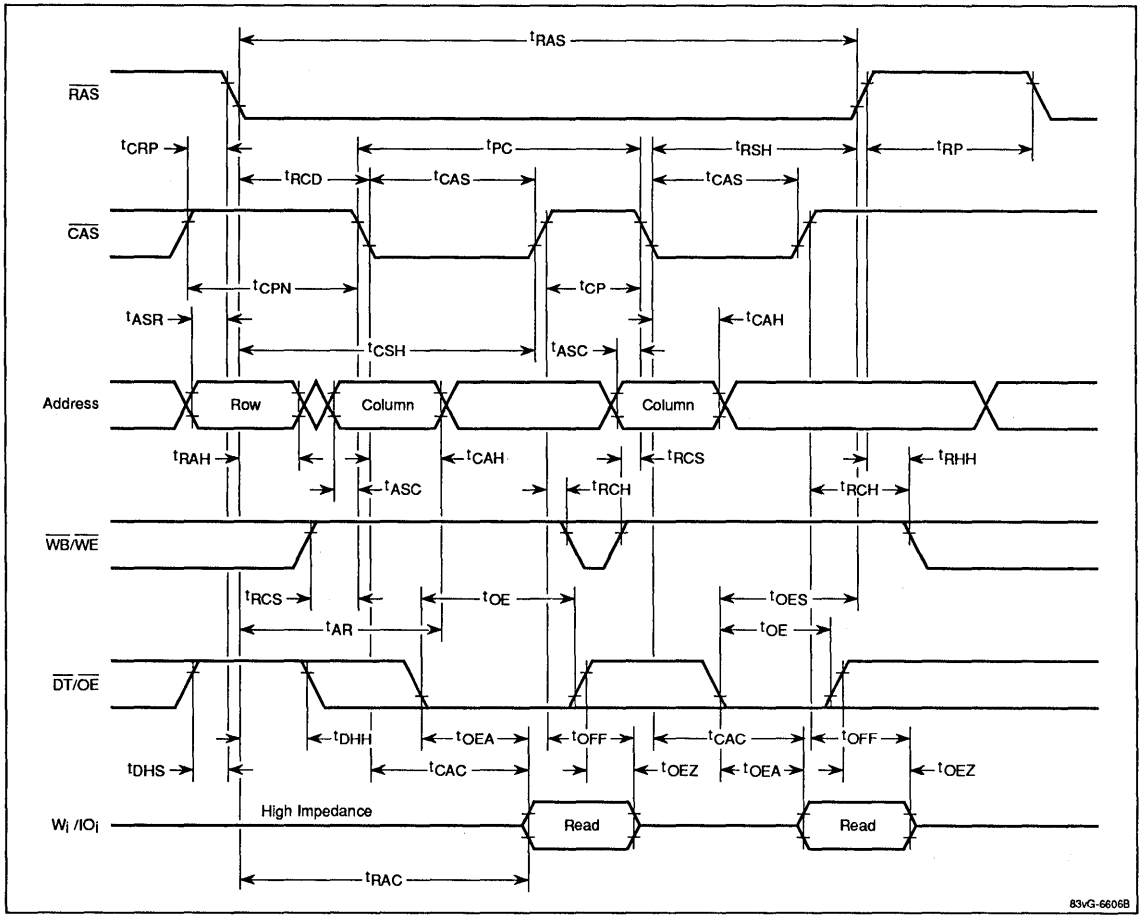
Timing Waveforms (cont)

Hidden Refresh Cycle



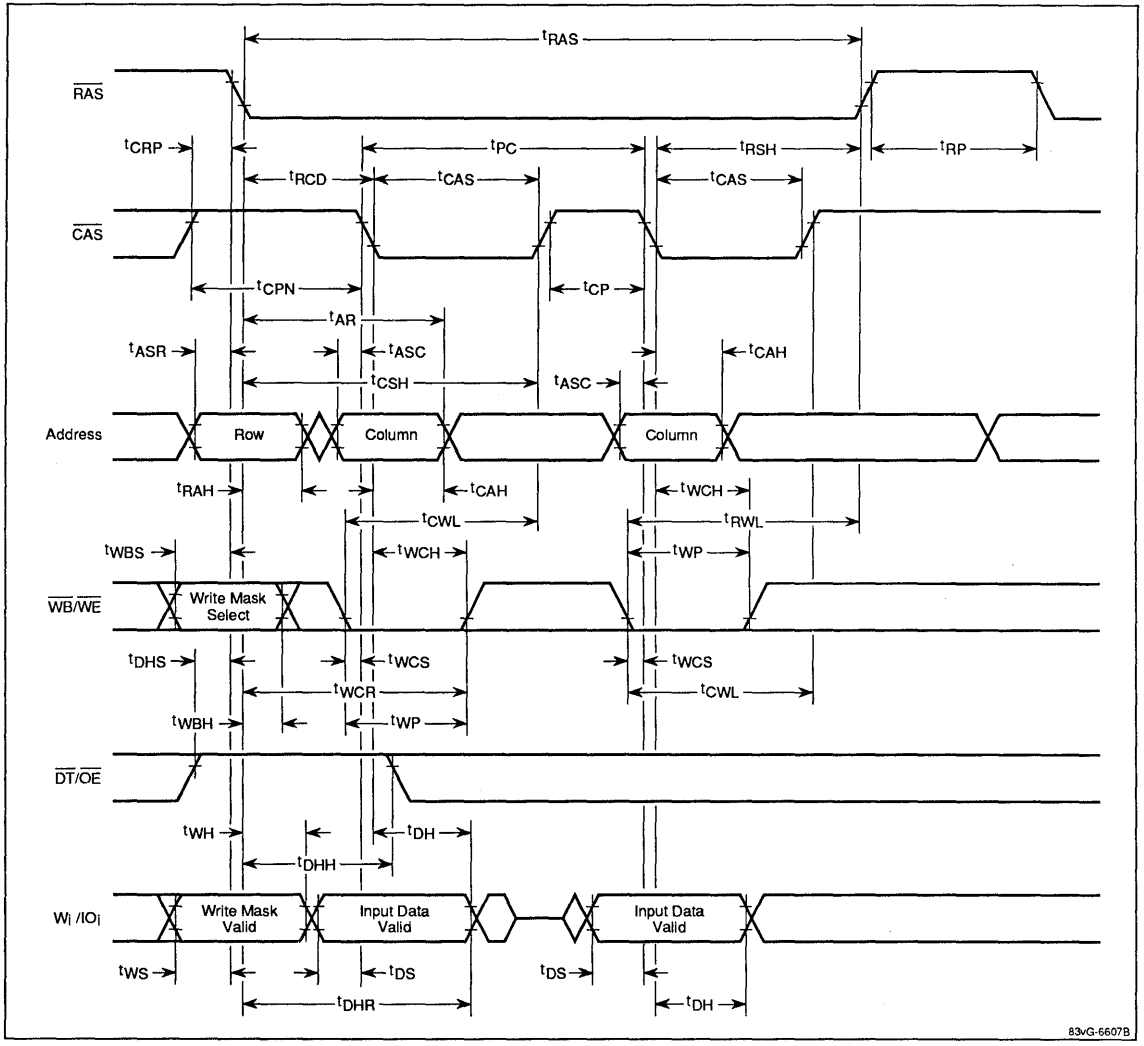
Timing Waveforms (cont)

Page Read Cycle



Timing Waveforms (cont)

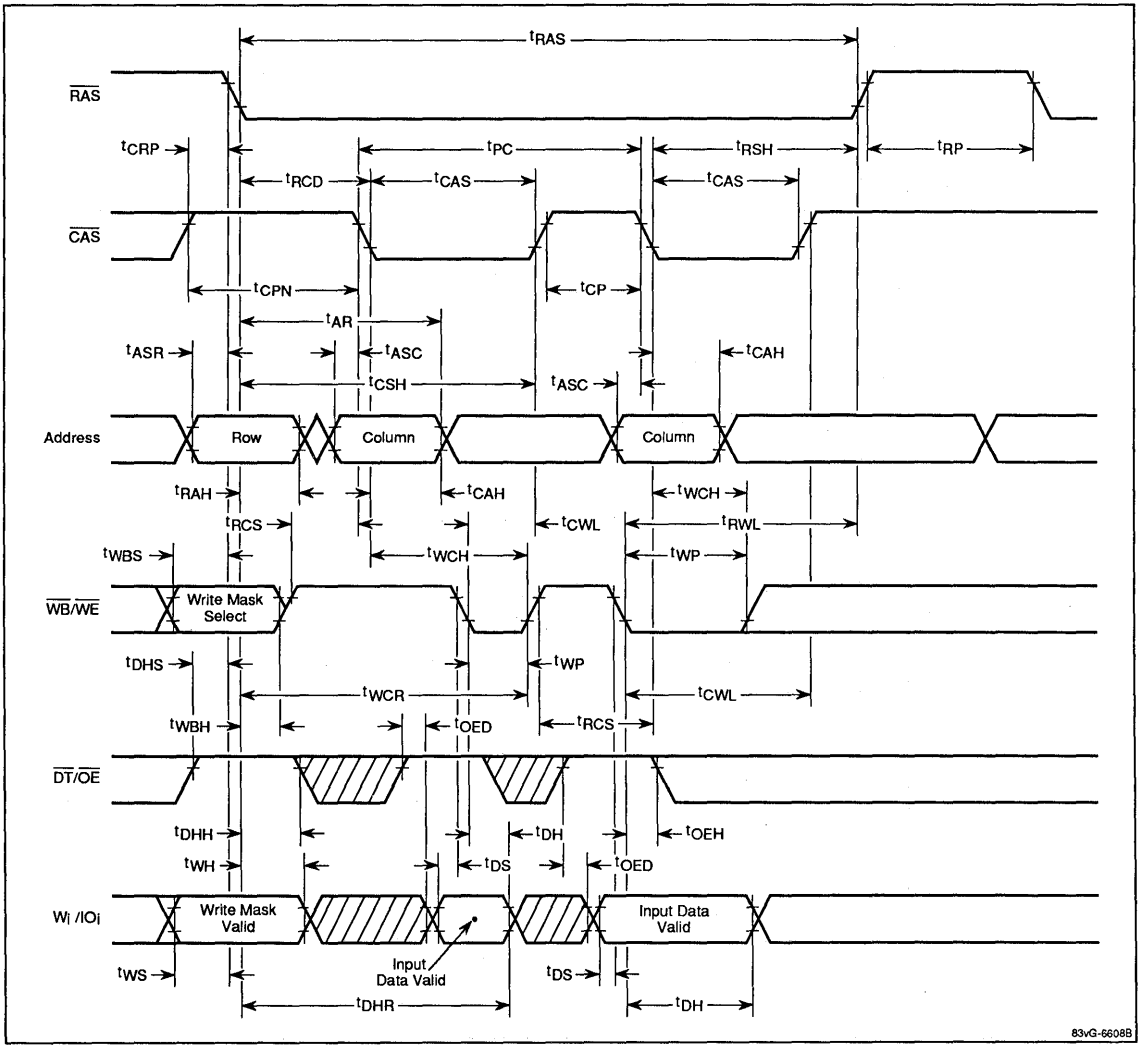
Page Early Write Cycle



12a

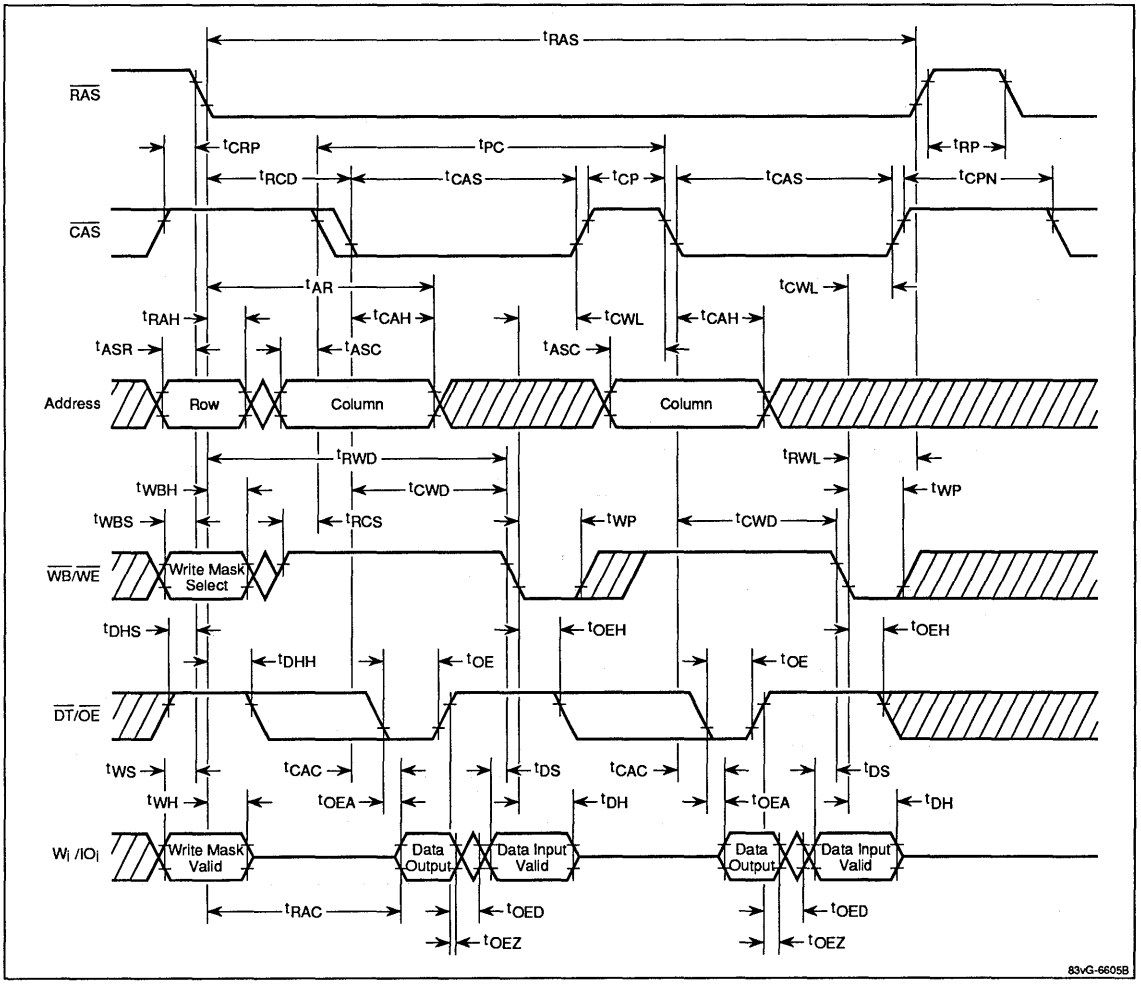
Timing Waveforms (cont)

Page Late Write Cycle



Timing Waveforms (cont)

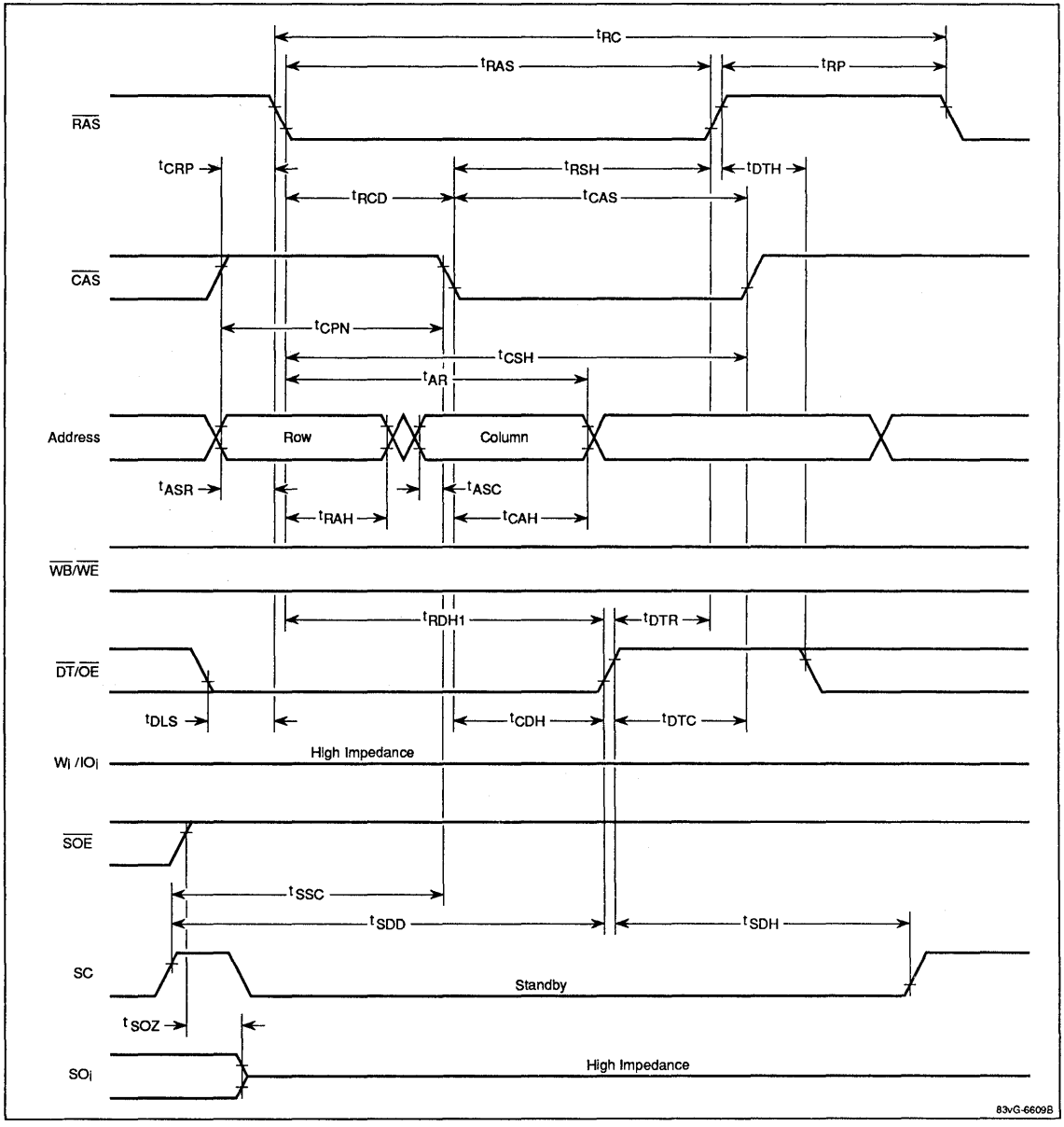
Page Read-Modify-Write Cycle



12a

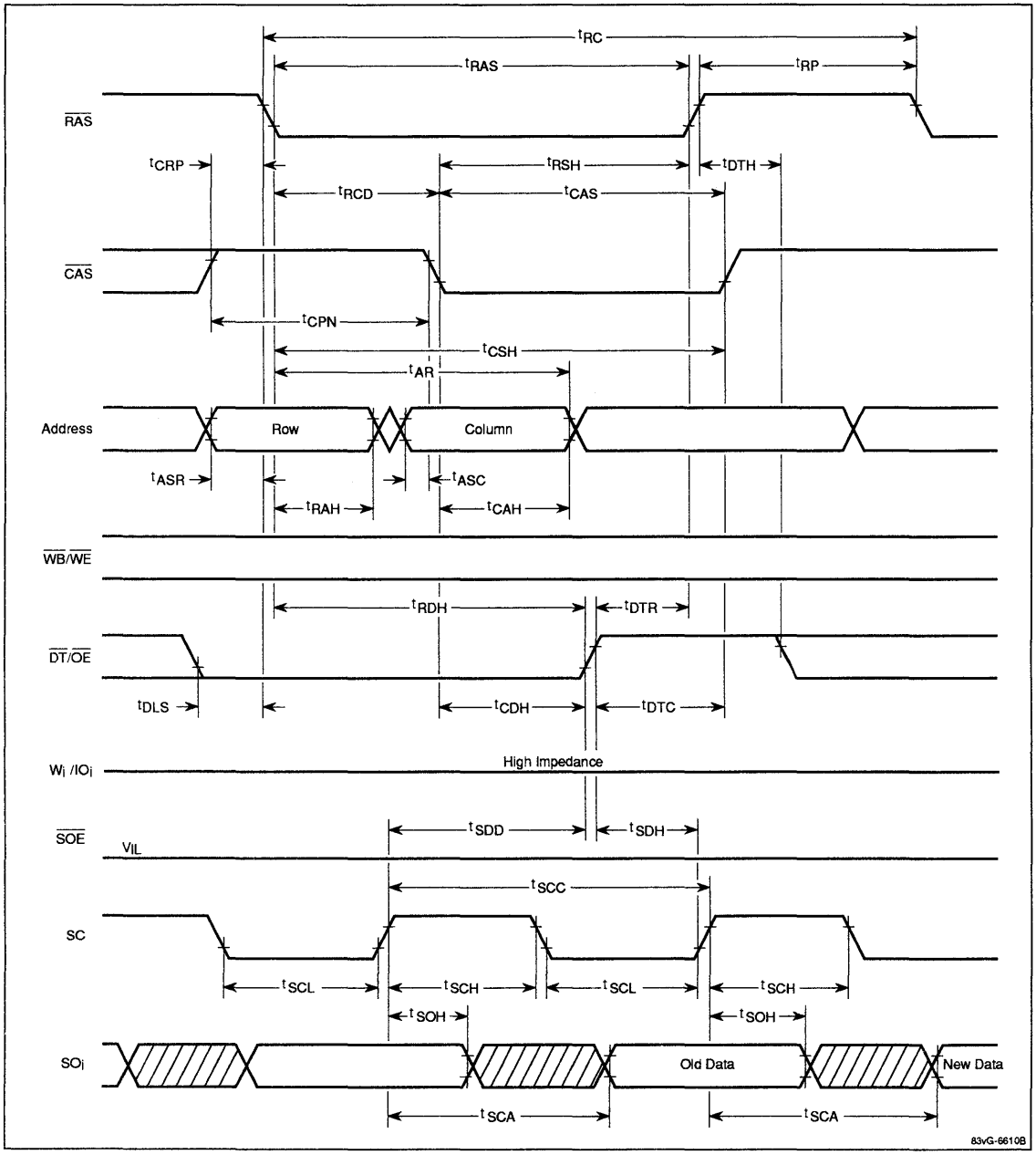
Timing Waveforms (cont)

Data Transfer Cycle (Serial Port in Standby)



Timing Waveforms (cont)

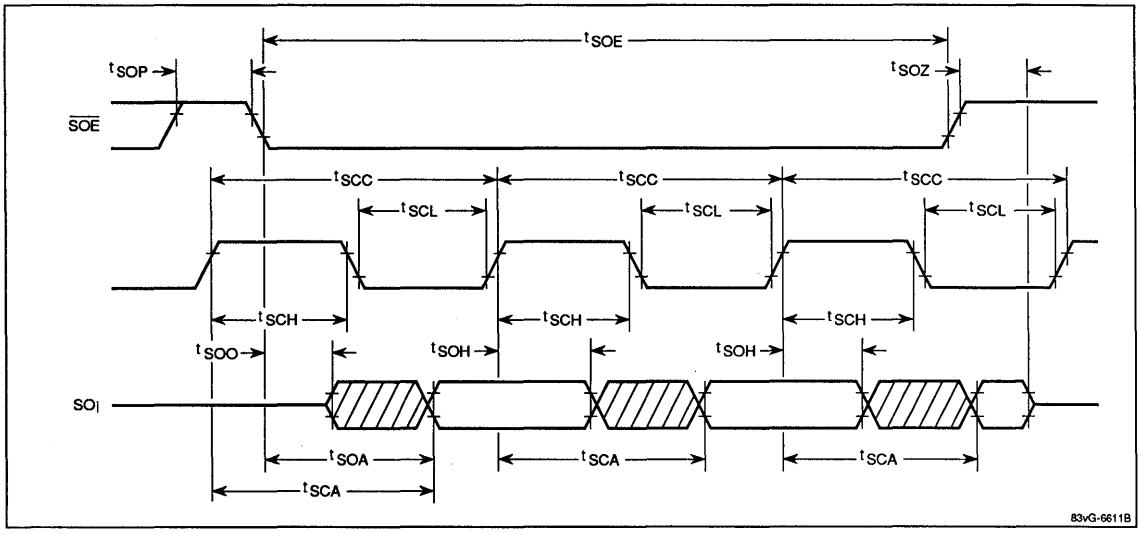
Data Transfer Cycle (Serial Port Active)



12a

Timing Waveforms (cont)

Serial Read Cycle



μPD42264
Dual-Port Graphics Buffer

Description

The μPD42264 is a dual-port graphics buffer equipped with a 64K x 4-bit random access port and a 256 x 4-bit serial read port. The serial read port is connected to an internal 1024-bit data register through a 256 x 4-bit serial read output circuit. The random access port is used by the host CPU to read or write data addressed in any desired order and has a write-per-bit option that allows each of the four data bits to be individually selected or masked for a write cycle.

The μPD42264 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock, while the serial read port continues to operate normally. Following the clock transition of a data transfer, serial read output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

The μPD42264 is fabricated with CMOS technology that provides high storage cell density, high performance, and high reliability. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility. The μPD42264 is available in a 24-pin plastic DIP, 24-pin plastic SOJ, and 24-pin plastic ZIP, and is guaranteed for operation at 0 to +70°C.

Ordering Information

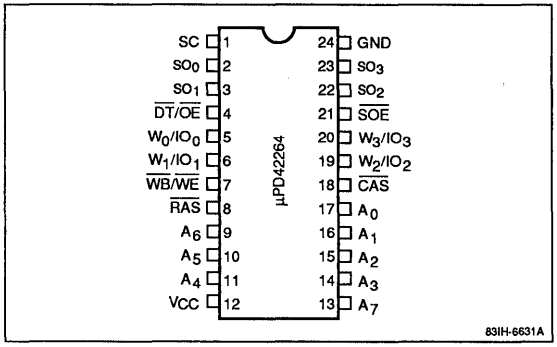
Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42264C-10	100 ns	25 ns	24-pin plastic DIP
μPD42264LA-10	100 ns	25 ns	24-pin plastic SOJ
μPD42264V-10	100 ns	25 ns	24-pin plastic ZIP

Features

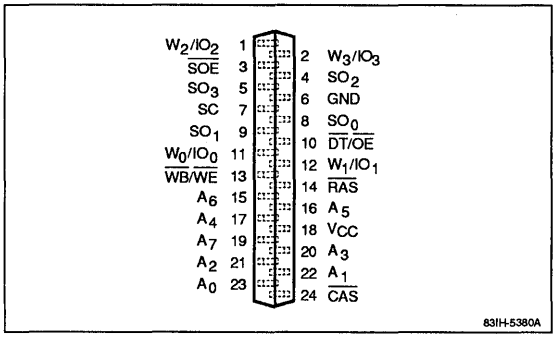
- Three functional blocks
  - 64K x 4-bit random access storage array
  - 1024-bit data register
  - 256 x 4-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- Single +5-volt ± 10% power supply
- On-chip substrate bias generator
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - Refresh interval: 256 cycles/4 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and page mode capabilities
  - Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - Hidden refreshing by means of $\overline{CAS}$-controlled output
  - Write-per-bit capability
  - Write bit selection multiplexed on IO_0-IO_3
- $\overline{RAS}$-activated data transfer
  - Same cycle time as for random access
  - Row data transferred to data register as specified by row address inputs
  - Starting location of following serial read operation specified by column address inputs
  - Transfer of 1024 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
  - Serial data presented on SO_0-SO_3
  - Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- 24-pin plastic DIP, 24-pin plastic SOJ, and 24-pin plastic ZIP packaging

Pin Configurations

24-Pin Plastic DIP and SOJ



24-Pin Plastic ZIP



Pin Identification

Symbol	Function
A_0 - A_7	Address inputs
$\overline{CAS}$	Column address strobe
$\overline{DT/OE}$	Data transfer/output enable
$\overline{RAS}$	Row address strobe
SC	Serial control
SO_0 - SO_3	Serial read outputs
$\overline{SOE}$	Serial output enable
W_0/IO_0 - W_3/IO_3	Write-per-bit inputs/data inputs and outputs
GND	Ground
$\overline{WB/WE}$	Write-per-bit/write enable
V_{CC}	+5-volt 10% power supply

Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	− 1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	− 1.0 V to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	− 55 to +125°C
Short-circuit output current, I_{OS}	50 mA

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

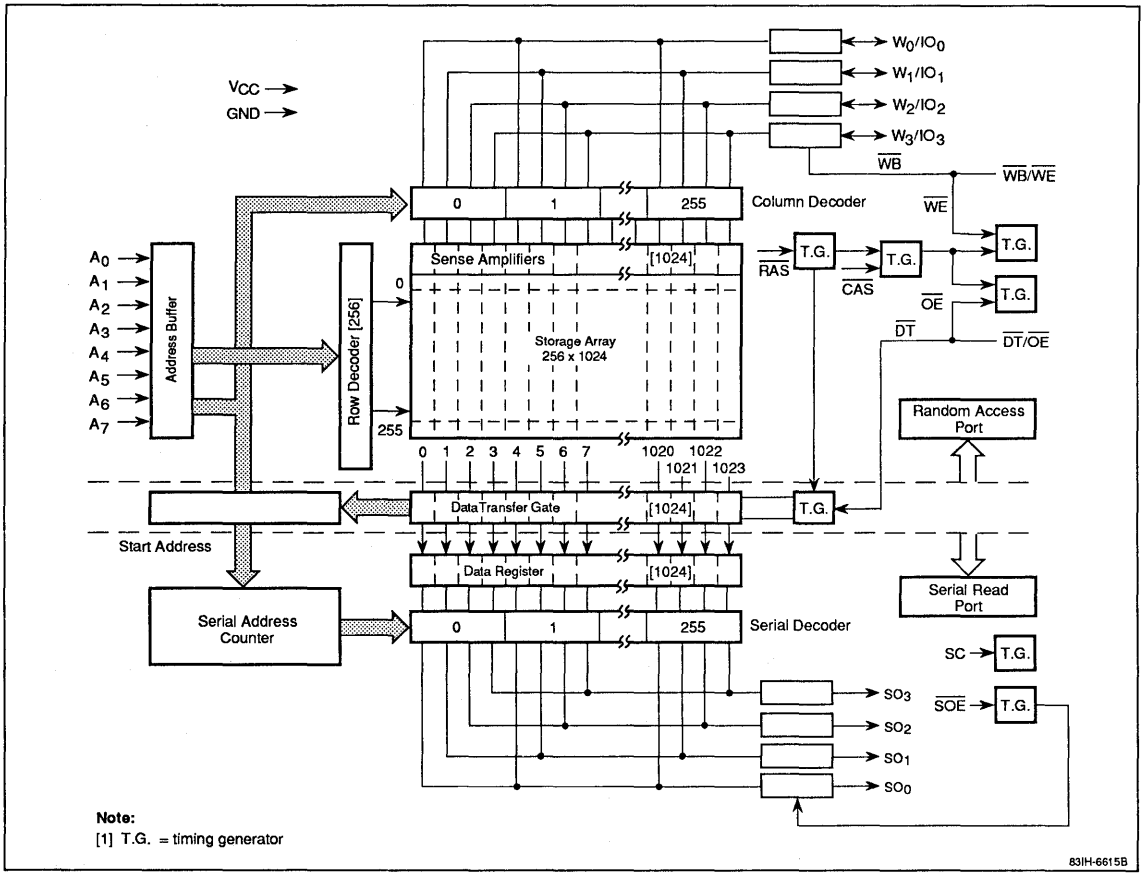
T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 - A_7
	$C_{I(\overline{DT/OE})}$	8	pF	$\overline{DT/OE}$
	$C_{I(\overline{WB/WE})}$	8	pF	$\overline{WB/WE}$
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 - W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 - SO_3

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	− 1.0		0.8	V
Operating temperature	T_A	0		70	°C

Block Diagram



DEVICE OPERATION

The μPD42264 consists of a random access port and a serial read port. The random access port executes standard read and write cycles as well as data transfer cycles, all of which are based on conventional $\overline{RAS}$/$\overline{CAS}$ timing. In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to the corresponding register location. The serial read port shows the contents of the data register in serial order. The random access port and the serial read port can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is arranged in a 256-row by 1024-column matrix. Each of 4 data bits in the random access port corresponds to 65,536 storage cells. Therefore, 16 address bits are required to decode one cell location. Eight row address bits are set up on pins A_0 through A_7 and latched onto the chip by $\overline{RAS}$. Eight column address bits then are set up on pins A_0 through A_7 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ is similar to a chip enable signal; whenever it is activated, 1024 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through 1 of 256 column decoders, 4 storage cells on the row are connected to 4 data buses, respectively. In the data transfer cycle, 8 row address bits are used to select 1 of the 256 possible rows involved in the transfer of data to the data register. Eight column address bits are

then used to select the 1 of 256 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 4 data bits in the 1024-bit data register are transferred to 4 serial data buses and read out. Activating SC repeatedly causes a serial read cycle (starting from the location specified in the data transfer cycle) to be executed within the 1024 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following functions are multiplexed in the random access port:

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

The $\overline{OE}$, $\overline{WE}$ and IO_i functions represent standard operations while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$. The $\overline{DT}$ level determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit option is used. W_i defines data bits to be written with the write-per-bit capability. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD42264 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 1024-bit data register from the corresponding 1024-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 1024 data transfer gates and transfer data from one of the rows to the data register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and maintaining $(\overline{WB}/)\overline{WE}$ high while $\overline{CAS}$ is active. The $(W_i/)IO_i$ data pin (i = 0, 1, 2, 3) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following three calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$ to $\overline{CAS}$ and $\overline{RAS}$ to $\overline{OE}$ delays are system-dependent timing parameters.

Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ high returns the output to high impedance.

Write Cycle. A write cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low during the $\overline{RAS}/\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or $(\overline{WB}/)\overline{WE}$ strobes the data on $(W_i/)IO_i$ into the on-chip data latch. To make use of the write-per-bit capability, $\overline{WB}(/\overline{WE})$ must be low as $\overline{RAS}$ falls. In this case, data bits targeted for write operation can be specified by keeping $W_i(/IO_i)$ high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

For those data bits of $W_i(/IO_i)$ that are kept low as $\overline{RAS}$ falls, write operation is inhibited on the chip. If $\overline{WB}(/\overline{WE})$ is high as $\overline{RAS}$ falls, the write-per-bit option is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low before $\overline{CAS}$. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, $(\overline{DT}/)\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$, but otherwise $(\overline{DT}/)\overline{OE}$ does not affect any circuit operation while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. Bringing the $(\overline{WB}/)\overline{WE}$ signal low with $\overline{RAS}$ and $\overline{CAS}$ low executes this cycle. $(W_i/)IO_i$ shows read data at access time. Afterward, in preparation for the upcoming write cycle, $(W_i/)IO_i$ is returned to high impedance by a high $(\overline{DT}/)\overline{OE}$. The data to be written is strobed by $(\overline{WB}/)\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of $(\overline{DT}/)\overline{OE}$, which can be activated just after $(\overline{WB}/)\overline{WE}$ falls, even when $(\overline{WB}/)\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 256 row addresses (A_0 through A_7) will refresh all storage cells. Any cycle in the random access port (i.e., read, write, refresh, or data transfer) refreshes the 1024 bits selected by the $\overline{RAS}$ addresses or by the on-chip refresh address counter.

$\overline{RAS}$-only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep $(W_i/)IO_i$ in a state of high impedance. This cycle is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal address counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This function performs hidden refreshing after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharging. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held low instead of high) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. By maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed, data is transferred at a faster rate because $\overline{RAS}$ addresses are maintained internally and do not have to be reapplied. During this operation, it is also possible to execute read, write and read-write/read-modify-write cycles. Additionally, the write-per-bit control specified in the entry write cycle is maintained through the following fast-page write cycle.

Data Transfer Cycle. A data transfer cycle is executed by bringing $\overline{DT}/\overline{OE}$ low as $\overline{RAS}$ falls. The specified 1 of the possible 256 rows involved in the data transfer, as well as the starting location of the following serial read cycle in the serial read port, are defined by address inputs. $\overline{DT}/\overline{OE}$ must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$, so that the data transfer condition may be satisfied. The low-to-high transition of $\overline{DT}$ causes two transfer operations through the data transfer gates: column address buffer outputs are transferred to the serial address counters, and storage cell data amplified on digit lines is transferred to the data register. At least one SC cycle is required to hold the data in the register. Otherwise, the beginning of the next transfer cycle destroys the newly transferred data. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the transferred data in the random access port.

Serial Read Port

The serial read port is used only to read serially the contents of the data register starting from a specified location. The entire operation, therefore, follows a data transfer cycle. Data stored in the serial register remains valid for a minimum of 4 ms after the transfer cycle. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}/\overline{OE}$ must occur within a specified period in an SC cycle. Except for this SC cycle, the serial read port can operate asynchronously with the random access port. The output data appears at SO_i after an access time of t_{SCA}, measured from SC high, only when $\overline{SOE}$ is maintained low. The SC cycle that includes the positive transition of $\overline{DT}/\overline{OE}$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD42264 graphics buffers into the same external circuitry. When $\overline{SOE}$ is low, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is at a high logic level, SO_i is disabled and in a state of high impedance.

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DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −2 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −2 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 4.2 mA

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Random Access Port	Serial Read Port	Symbol	Max	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	70	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; IO = 0 mA; SC = $\overline{SOE}$ = V_{IH} (Note 1)
Standby	Standby	I_{CC2}	5	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance; SC = $\overline{SOE}$ = V_{IH}
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; SC = $\overline{SOE}$ = V_{IH}
Page cycle	Standby	I_{CC4}	50	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; SC = $\overline{SOE}$ = V_{IH} (Note 1)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	60	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; SC = $\overline{SOE}$ = V_{IH} (Note 1)
Data transfer	Standby	I_{CC6}	75	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; SC = $\overline{SOE}$ = V_{IH}
Read/write cycle	Active	I_{CC7}	120	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; IO = 0 mA; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
Standby	Active	I_{CC8}	50	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	110	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
Page cycle	Active	I_{CC10}	100	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	110	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
Data transfer	Active	I_{CC12}	125	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, and I_{CC6}, real values depend on output loading and cycle rates.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Column address hold time after $\overline{RAS}$ low	t_{AR}	70			ns	
Column address setup time	t_{ASC}	0			ns	
Row address setup time	t_{ASR}	0			ns	
Access time from $\overline{CAS}$	t_{CAC}			50	ns	(Notes 2, 5)
Column address hold time	t_{CAH}	20			ns	
$\overline{CAS}$ pulse width	t_{CAS}	50		10,000	ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{CDH}	30			ns	(Note 12)
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	20			ns	
$\overline{CAS}$ precharge time (page cycle only)	t_{CP}	40			ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	20			ns	
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10			ns	
SC delay time from $\overline{CAS}$	t_{CSD}	45			ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	100			ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	10			ns	

AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	85			ns	(Note 10)
Write command to $\overline{CAS}$ lead time	t_{CWL}	35			ns	
Data-in hold time	t_{DH}	30			ns	(Note 11)
$\overline{DT}$ high hold time	t_{DHH}	15			ns	
Data-in hold time after $\overline{RAS}$ low	t_{DHR}	80			ns	
$\overline{DT}$ high setup time	t_{DHS}	0			ns	
$\overline{DT}$ low setup time	t_{DLS}	0			ns	
Data-in setup time	t_{DS}	0			ns	(Note 11)
$\overline{DT}$ high to $\overline{CAS}$ high delay	t_{DTC}	10			ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	15			ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	10			ns	
$\overline{OE}$ pulse width	t_{OE}	25			ns	
Access time from $\overline{OE}$	t_{OEA}			25	ns	(Note 2)
$\overline{OE}$ to data-in setup delay	t_{OED}	25			ns	
$\overline{OE}$ hold time after $\overline{WE}$ low	t_{OEH}	10			ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10			ns	
Output disable time from $\overline{OE}$ high	t_{OEZ}	0		25	ns	(Note 6)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0		25	ns	(Note 6)
Page cycle time	t_{PC}	100			ns	
Access time from $\overline{RAS}$	t_{RAC}			100	nc	(Notes 2, 4)
Row address hold time	t_{RAH}	15			ns	
$\overline{RAS}$ pulse width	t_{RAS}	100		10,000	ns	
Random read or write cycle time	t_{RC}	190			ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25		50	ns	(Note 4)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0			ns	(Note 9)
Read command setup time	t_{RCS}	0			ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low (serial port active)	t_{RDH}	80			ns	(Note 12)
$\overline{DT}$ low hold time after $\overline{RAS}$ low (serial port in standby)	t_{RDH1}	15			ns	(Note 12)
Refresh interval	t_{REF}			4	ms	
$\overline{RAS}$ precharge time	t_{RP}	80			ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0			ns	
Read command hold after $\overline{RAS}$ high	t_{RRH}	10			ns	(Note 9)
SC delay from $\overline{RAS}$	t_{RSD}	95			ns	(Note 12)
$\overline{RAS}$ hold time	t_{RSH}	50			ns	
Read-write/read-modify-write cycle time	t_{RWC}	260			ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	135			ns	(Note 10)
Write command to $\overline{RAS}$ lead time	t_{RWL}	35			ns	
SC pulse width	t_{SCH}	10			ns	
Serial output access time from SC	t_{SCA}			30	ns	(Notes 2, 7)
Serial clock cycle time	t_{SCC}	30		50,000	ns	

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AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SC precharge time	t_{SCL}	10			ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	10			ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	10			ns	
Serial output access time from $\overline{SOE}$	t_{SOA}			25	ns	
$\overline{SOE}$ pulse width	t_{SOE}	10			ns	(Note 13)
Serial output hold time after SC high	t_{SOH}	5			ns	
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5			ns	
$\overline{SOE}$ precharge time	t_{SOP}	10			ns	(Note 13)
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0		25	ns	(Note 6)
SC setup time to $\overline{CAS}$	t_{SSC}	10			ns	(Note 12)
Rise and fall transition time	t_T	3		50	ns	
Write-per-bit hold time	t_{WBH}	15			ns	
Write-per-bit setup time	t_{WBS}	0			ns	
Write command hold time	t_{WCH}	25			ns	
Write command hold time after $\overline{RAS}$ low	t_{WCR}	75			ns	
Write command setup time	t_{WCS}	0			ns	(Note 10)
Write bit selection hold time	t_{WH}	15			ns	
Write command pulse width	t_{WP}	15			ns	
Write bit selection setup time	t_{WS}	0			ns	

Notes:

(1) See input/output timing waveforms for timing reference voltages.

(2) See figures 1 and 2 for output loads.

(3) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles (except $\overline{CAS}$-before-$\overline{RAS}$ cycles), before proper device operation is achieved.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.

(5) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(6) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(7) Data in the serial output register remains valid for 4 ms (min) after a data transfer cycle.

(8) V_{IH} (min) and V_{IL} (min) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(9) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(10) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(11) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of $\overline{(WB/)WE}$ in delayed write or read-modify-write cycles.

(12) Use t_{RDH} and t_{CDH} when the serial port is active and t_{RDH1}, t_{RSD}, t_{CSD} and t_{SSC} if it is in standby.

(13) $\overline{SOE}$ may be tied to GND if the output enable function of the serial port is not needed.

Figure 1. Input Timing

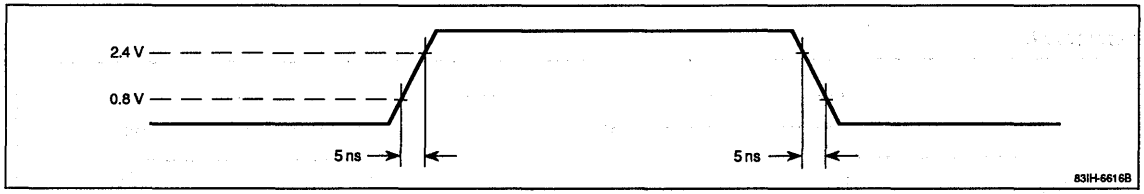


Figure 2. Output Timing

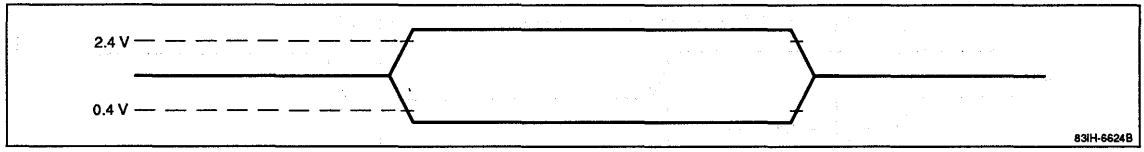


Figure 3. Output Loading in Random Access Port

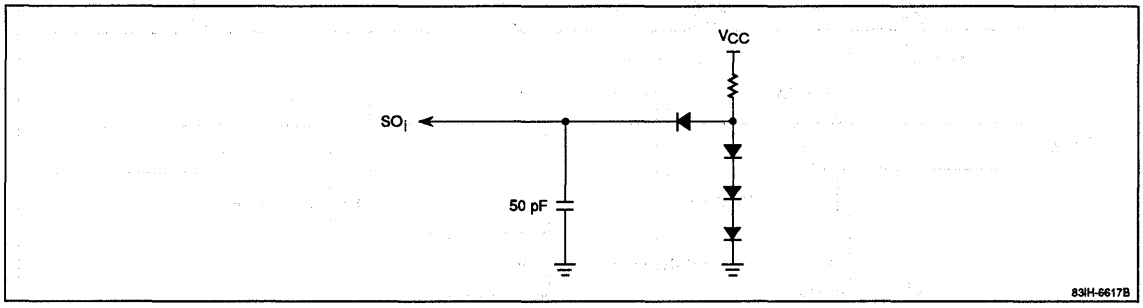
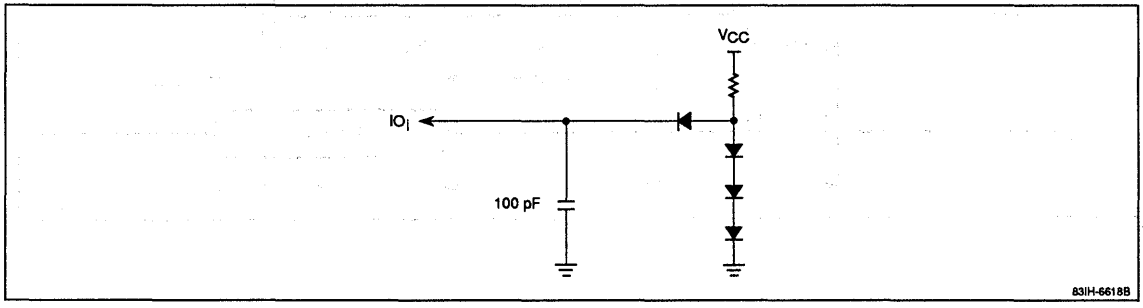
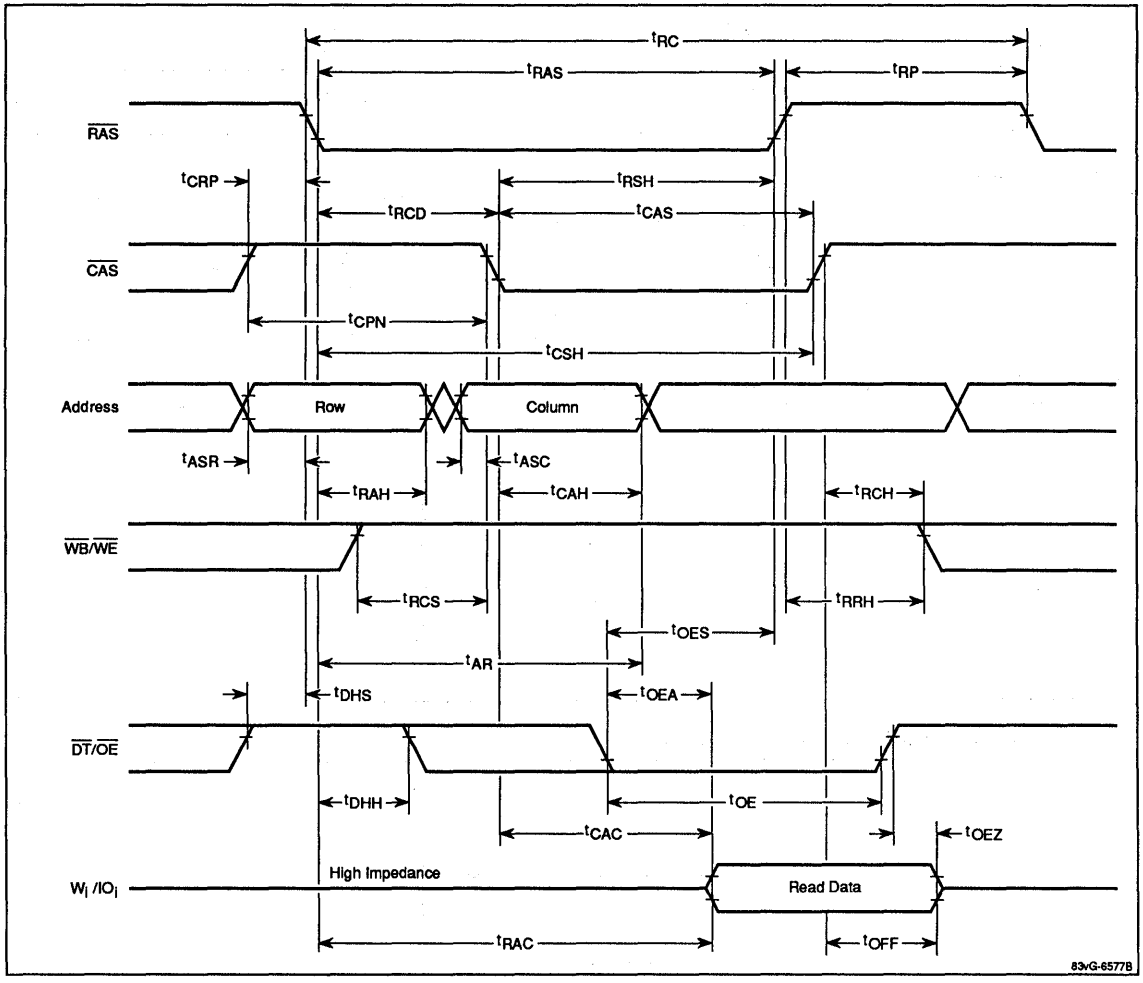


Figure 4. Output Loading in Serial Read Port



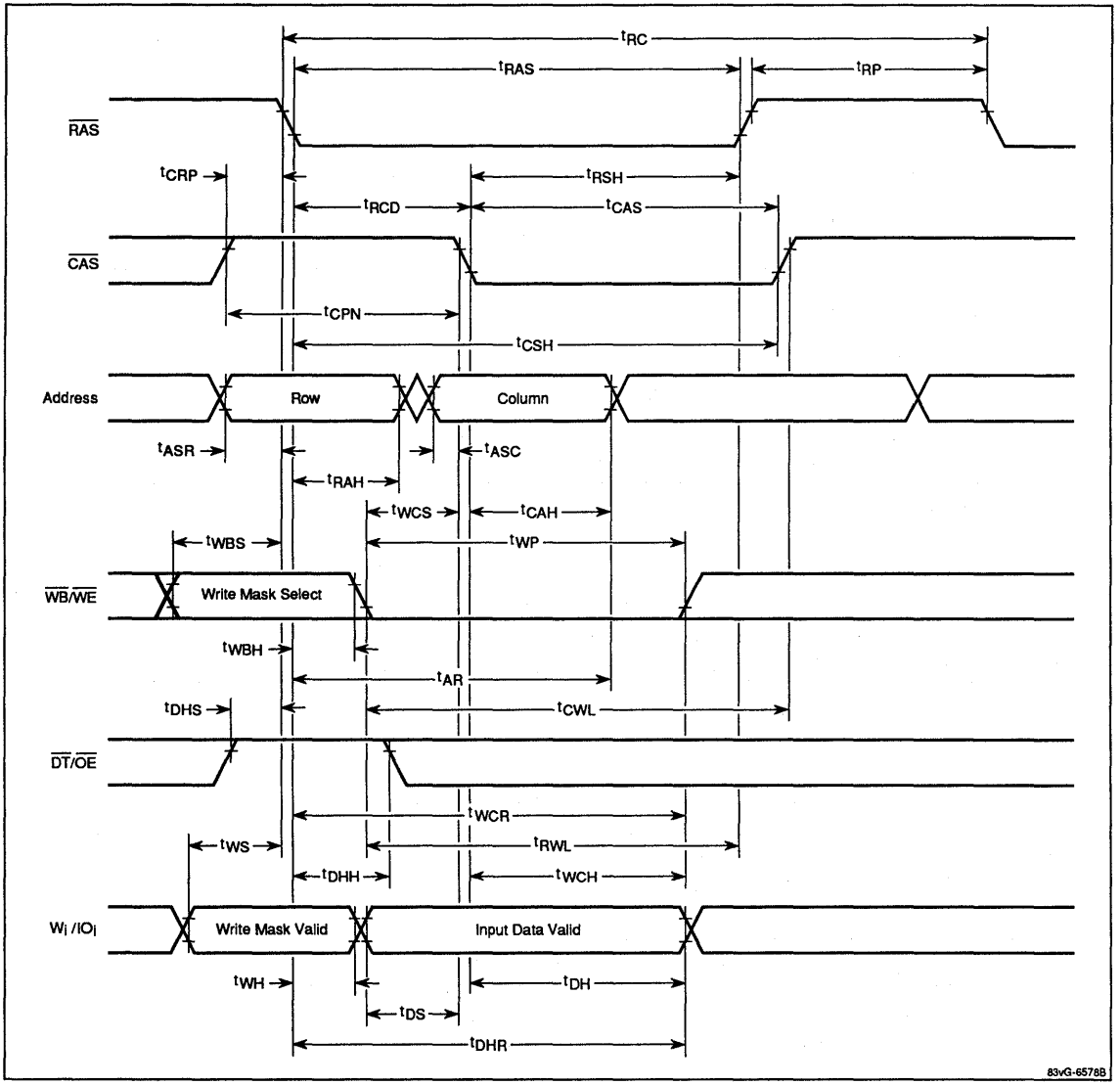
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



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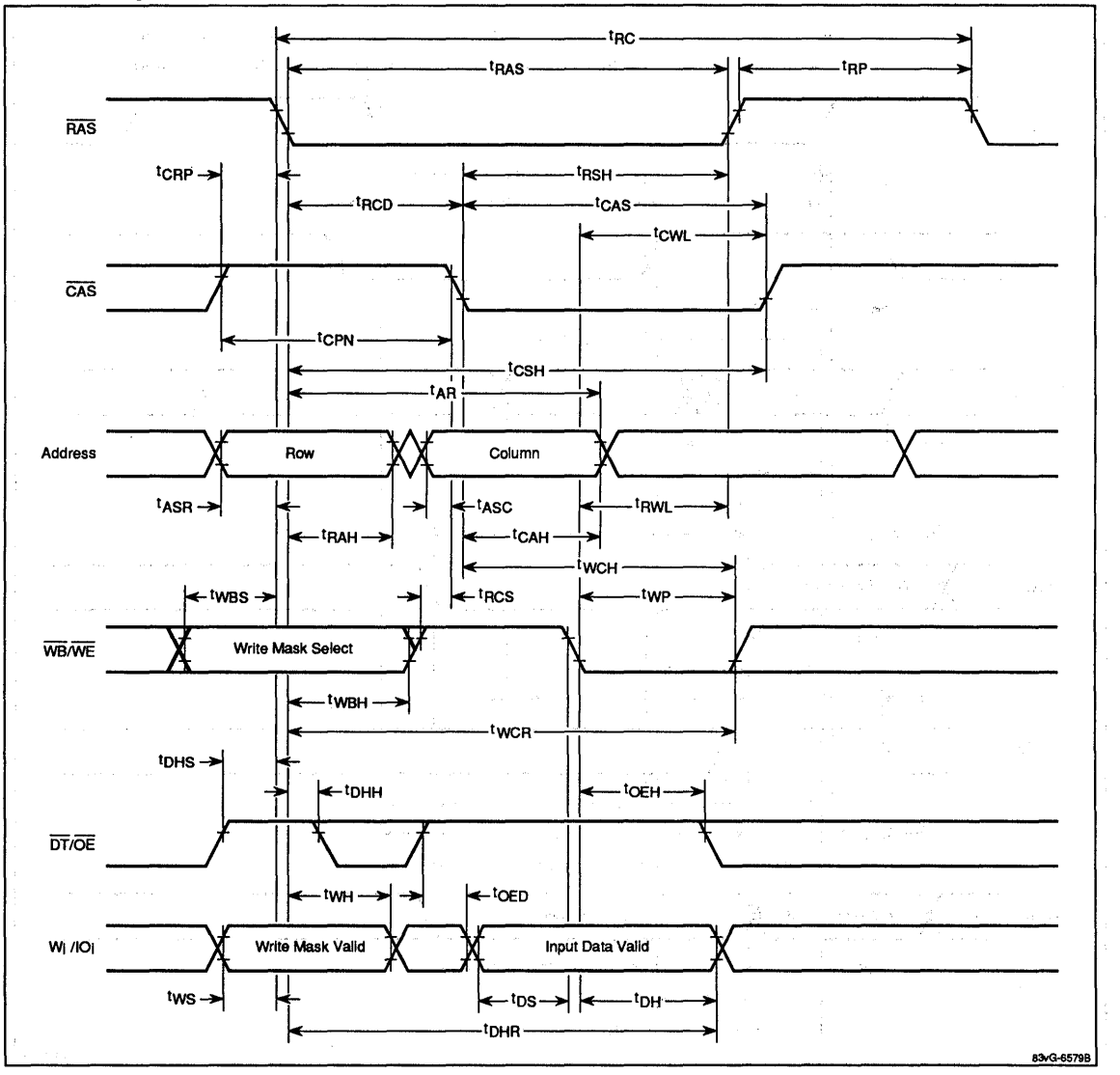
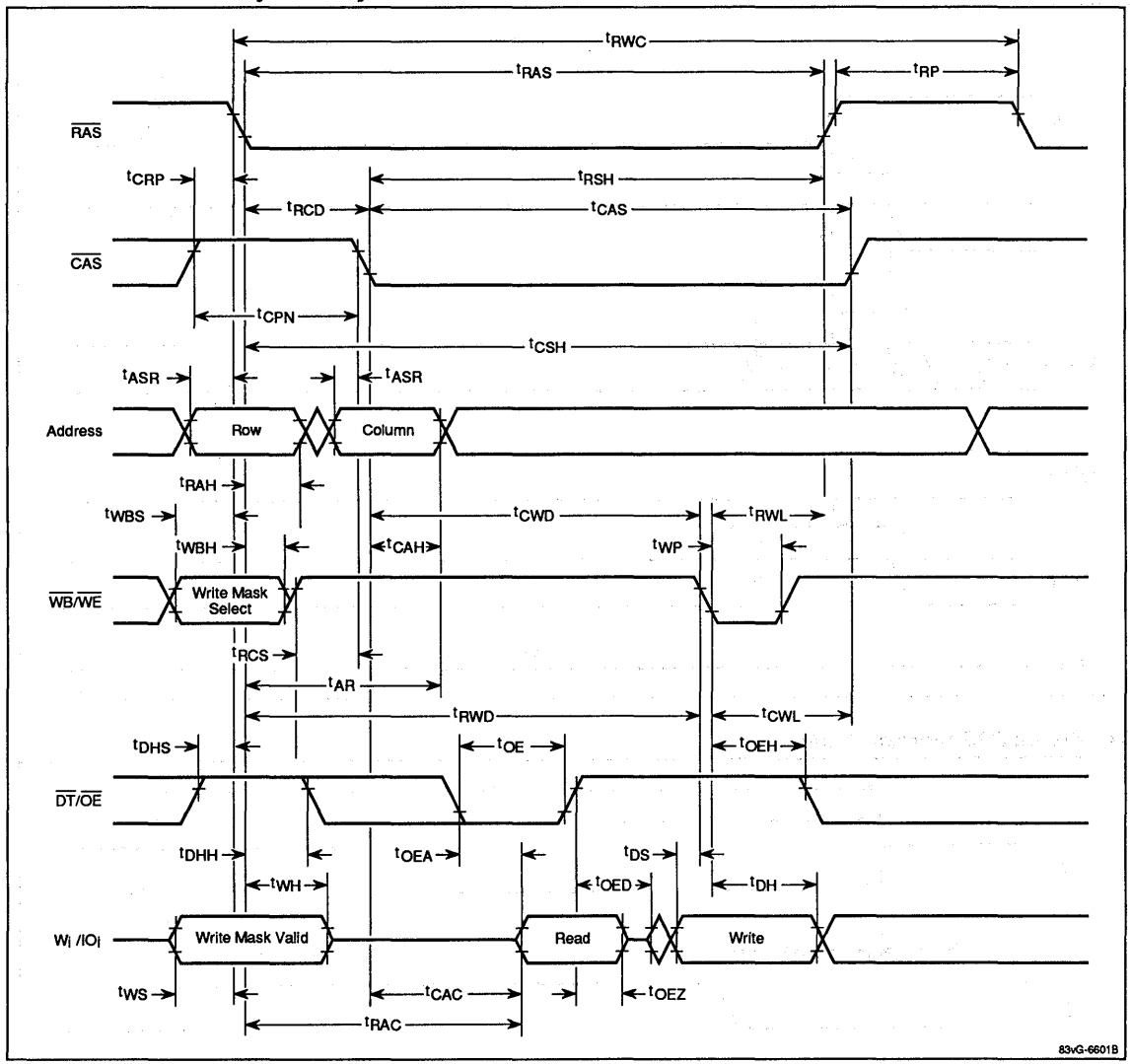
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



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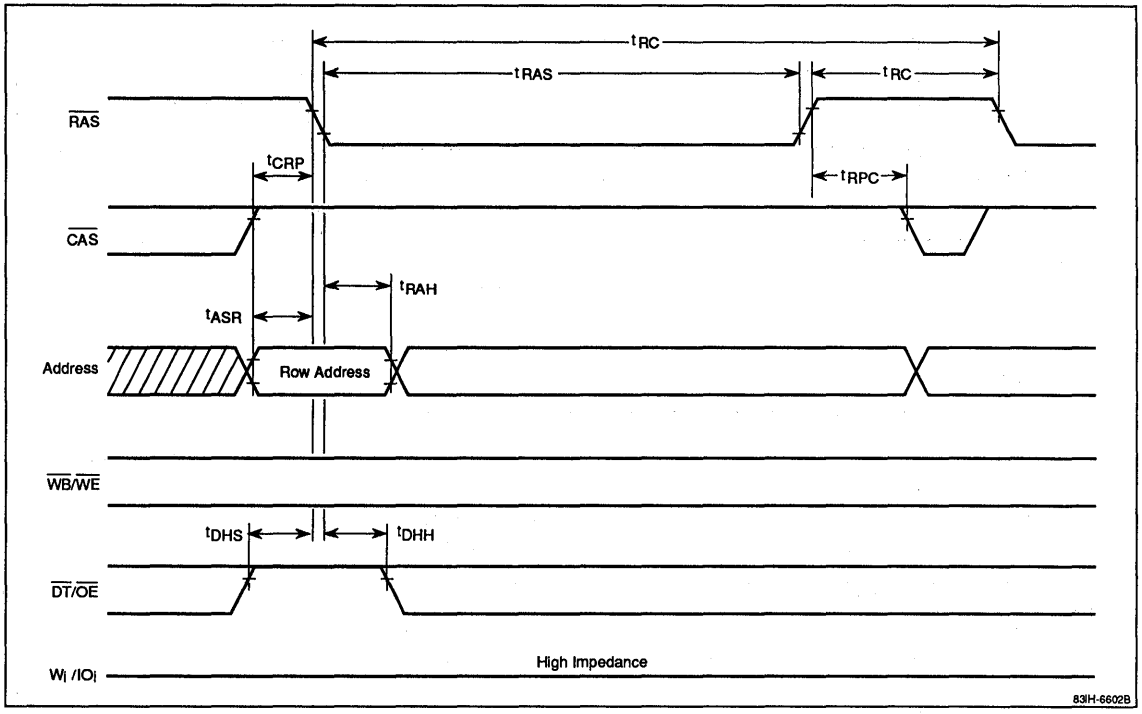
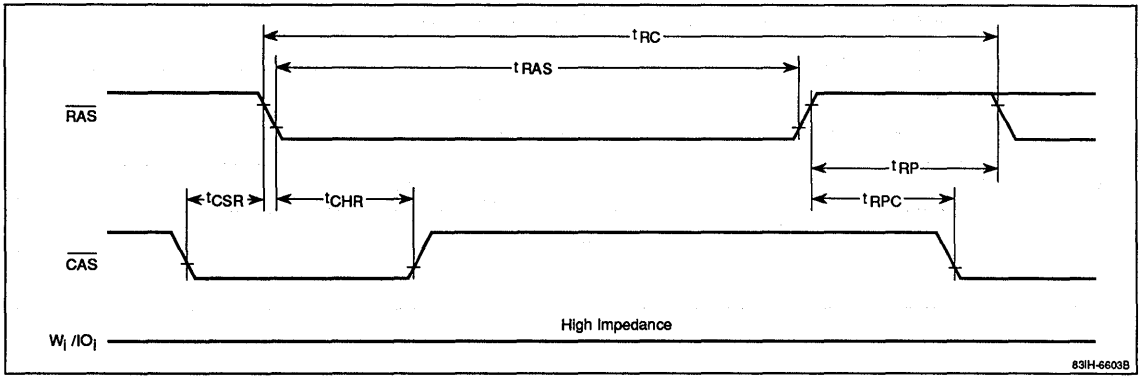
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle

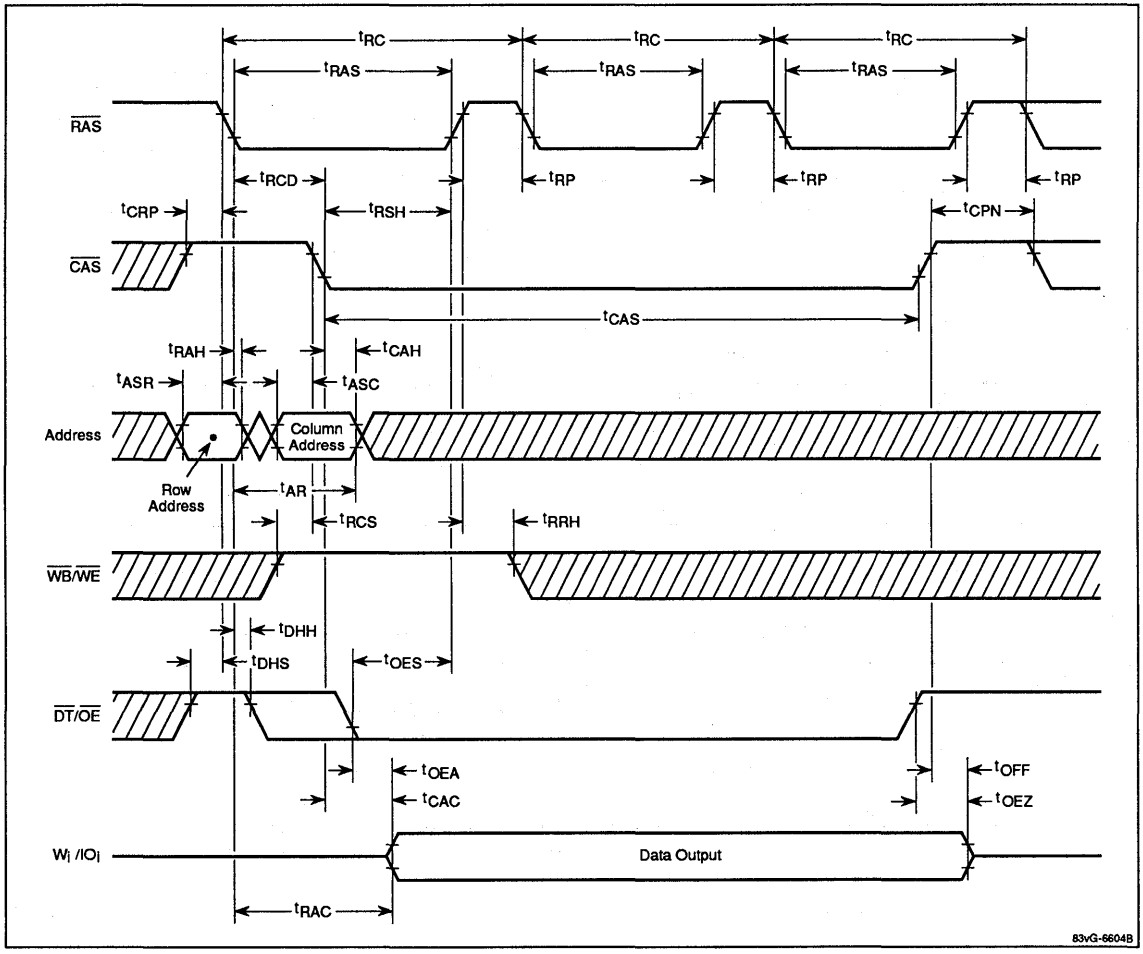


$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

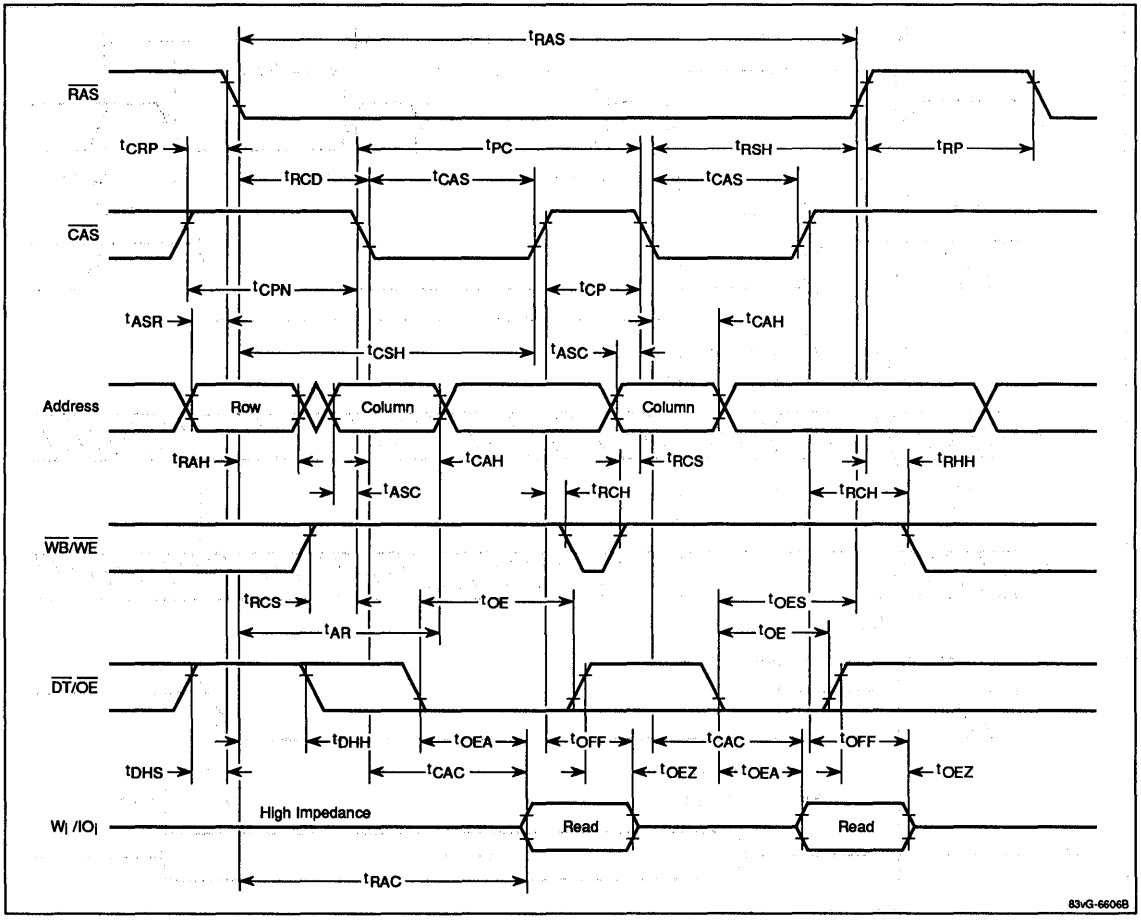
Hidden Refresh Cycle



12b

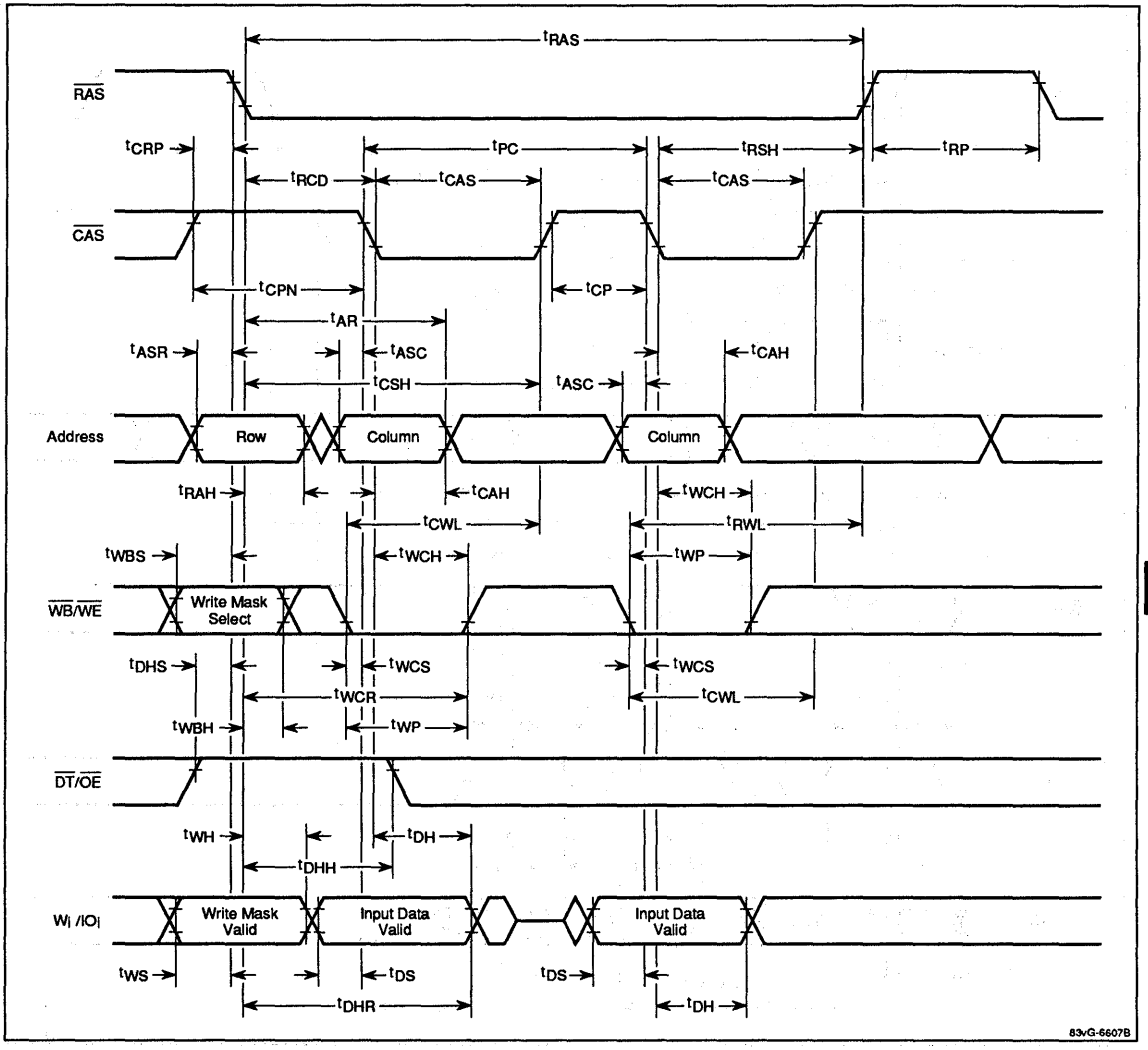
Timing Waveforms (cont)

Page Read Cycle



Timing Waveforms (cont)

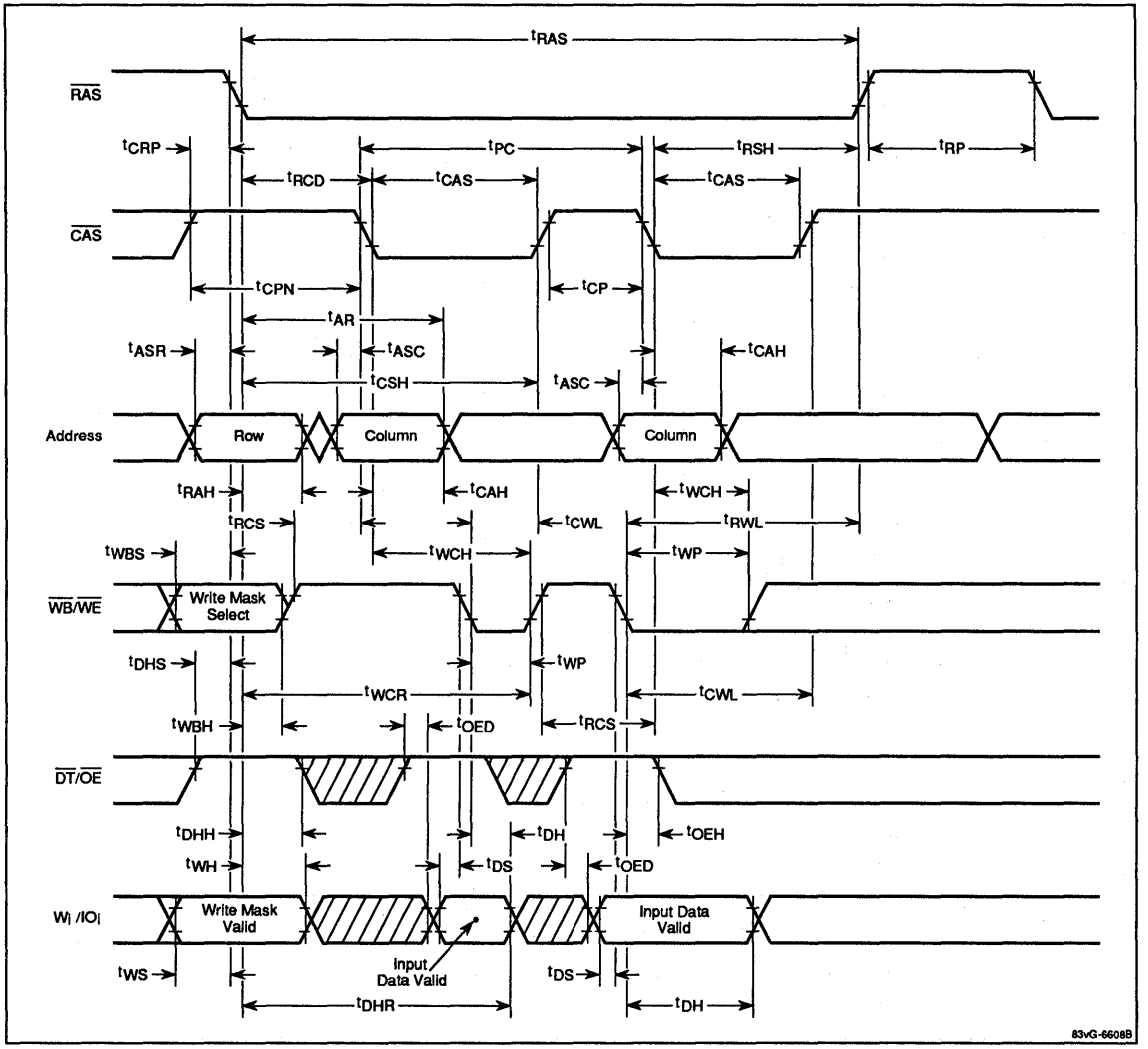
Page Early Write Cycle



12b

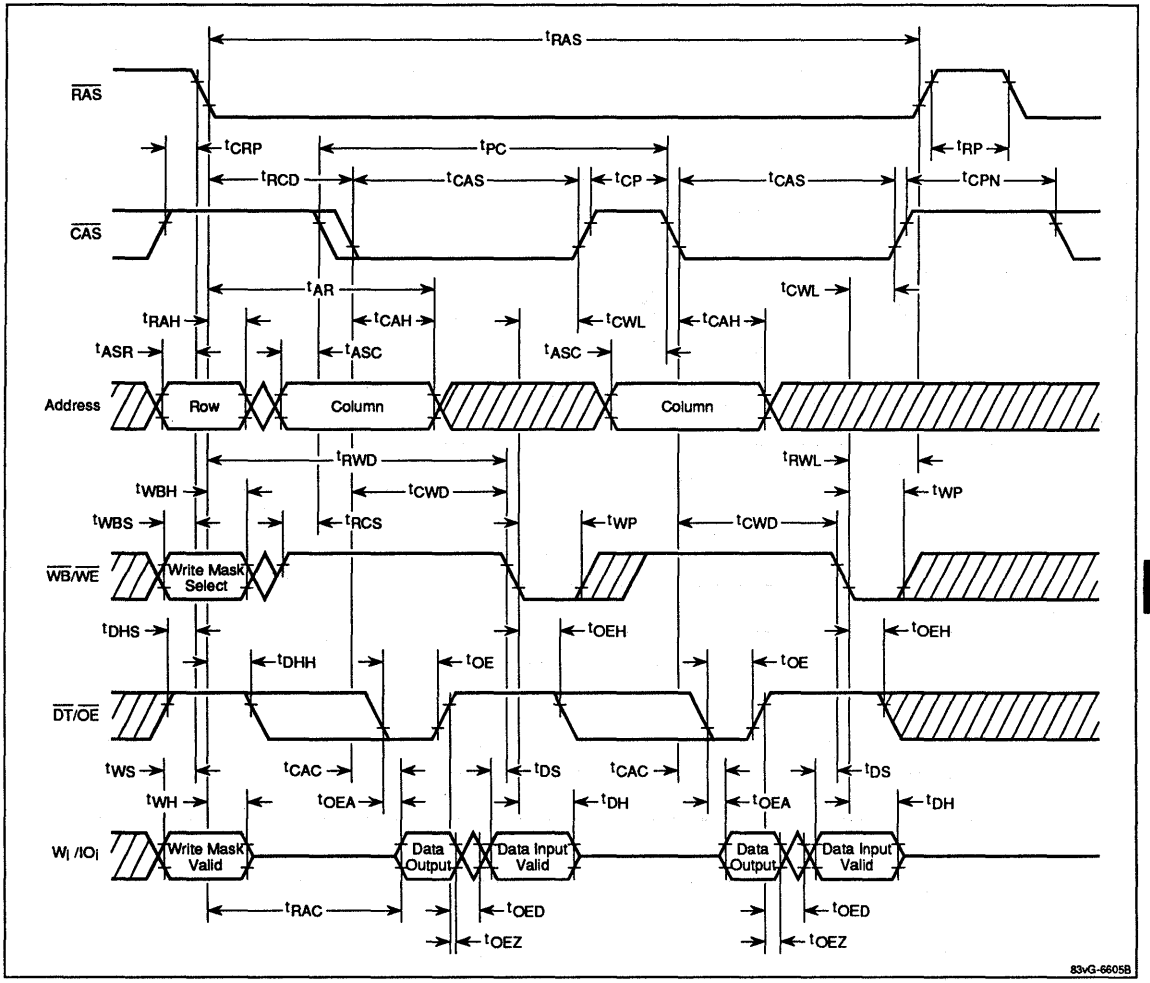
Timing Waveforms (cont)

Page Late Write Cycle



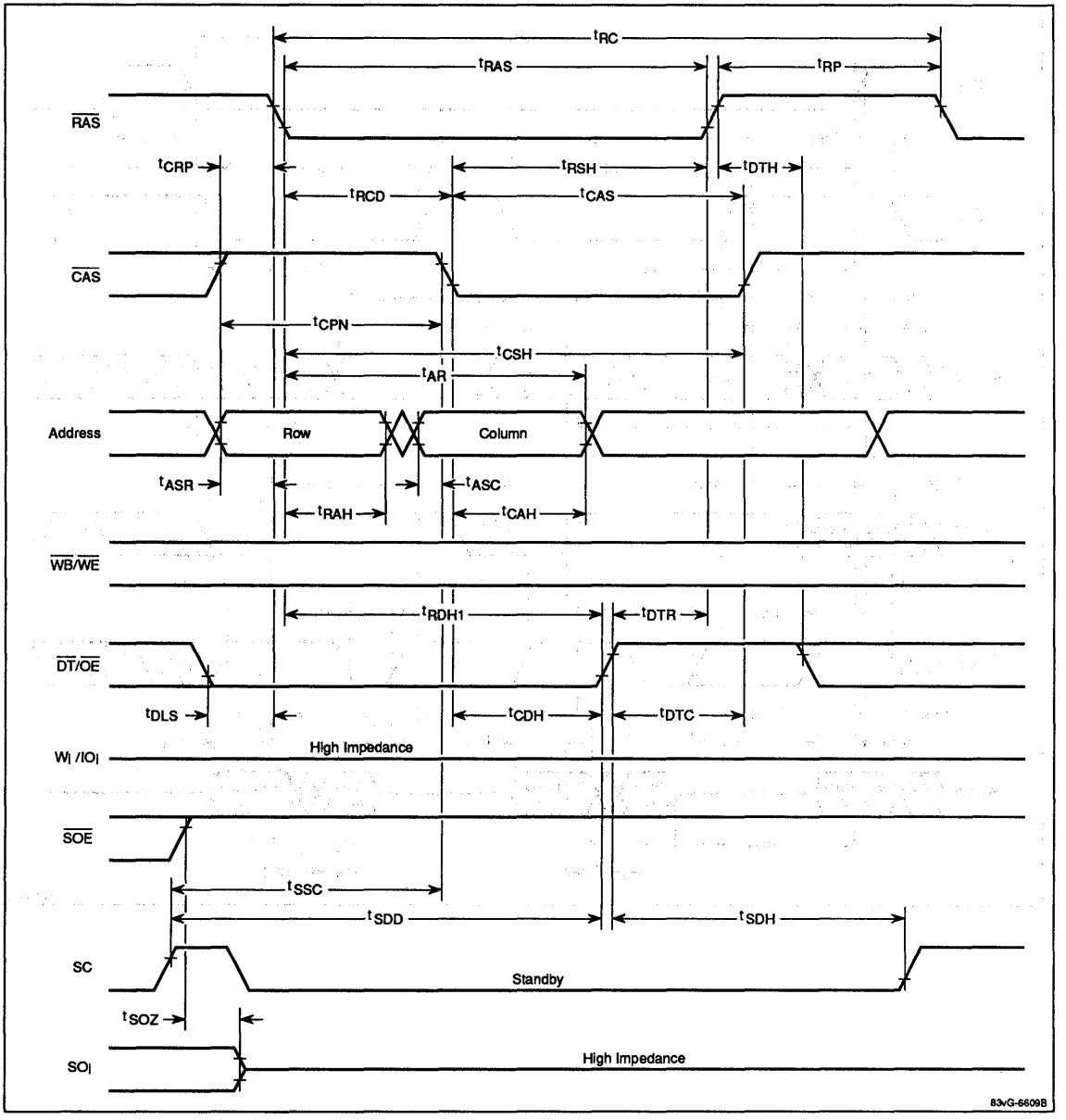
Timing Waveforms (cont)

Page Read-Modify-Write Cycle



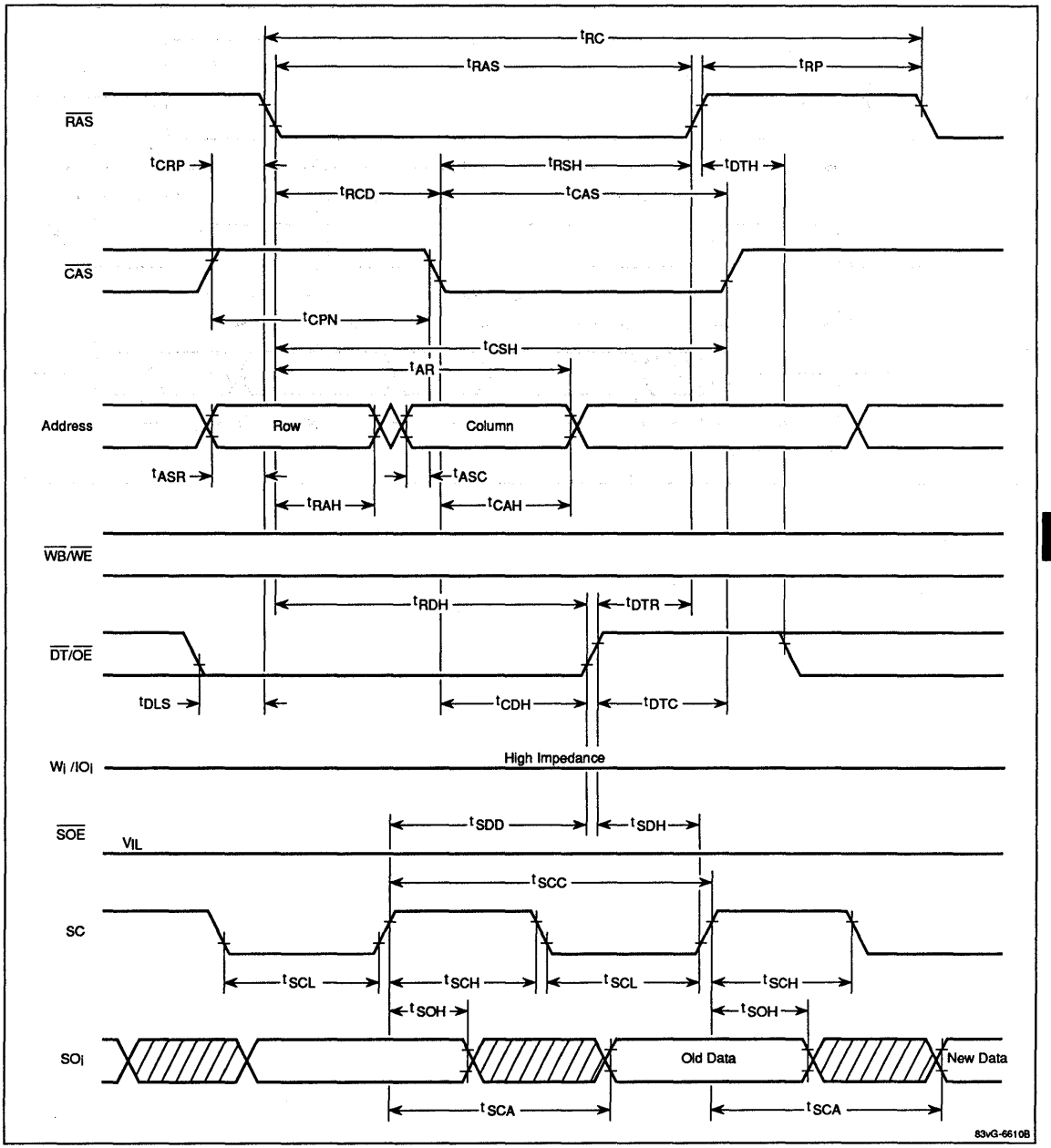
Timing Waveforms (cont)

Data Transfer Cycle (Serial Port in Standby)



Timing Waveforms (cont)

Data Transfer Cycle (Serial Port Active)



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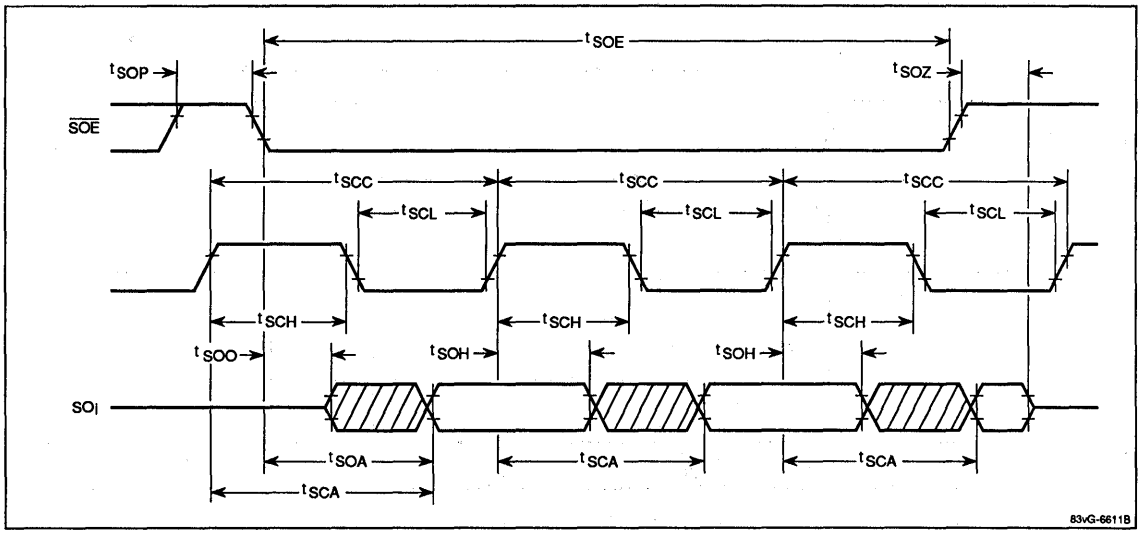
Timing Waveforms (cont)

Serial Read Cycle



μPD42273
Dual-Port Graphics Buffer

Description

The μPD42273 is a dual-port graphics buffer equipped with a 256K x 4-bit random access port and a 512 x 4-bit serial read port. The serial read port is connected to an internal 2048-bit data register through a 512 x 4-bit serial read output circuit. The random access port is used by the host CPU to read or write data addressed in any desired order. A write-per-bit capability allows each of the four data bits to be individually selected or masked for a write cycle.

The μPD42273 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock; the serial read port continues to operate normally. Following the clock transition of a data transfer, serial output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

An advanced CMOS silicon-gate process using polycide technology and trench capacitors provides high storage cell density, high performance, and high reliability.

Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

The μPD42273 is an alternative to the μPD42274 for applications that do not require the flash write function.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The μPD42273 is available in a 28-pin plastic ZIP or 28-pin plastic SOJ and is guaranteed for operation at 0 to + 70°C.

Features

- Three functional blocks
  - 256K x 4-bit random access storage array
  - 2048-bit data register
  - 512 x 4-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- Single + 5-volt ±10% power supply
- On-chip substrate bias generator
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - 512 refresh cycles every 8 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page cycles
  - Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - $\overline{CAS}$-controlled hidden refreshing
  - Write-per-bit option regarding four I/O bits
  - Write bit selection multiplexed on IO_0-IO_3
- $\overline{RAS}$-activated data transfer
  - Same cycle time as for random access
  - Row data transferred to data register as specified by row address inputs
  - Starting location of following serial read cycle specified by column address inputs
  - Transfer of 2048 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
- Serial data output on SO_0-SO_3
- Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- CMOS silicon-gate process with trench capacitors

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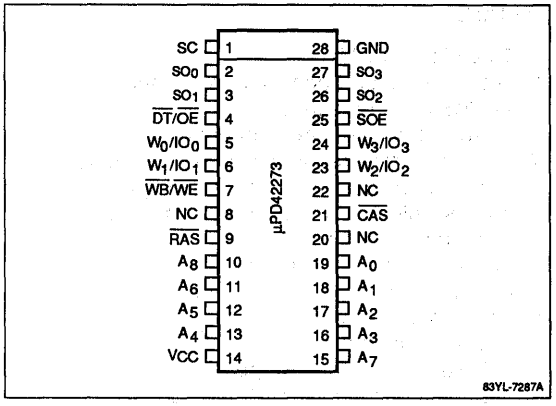
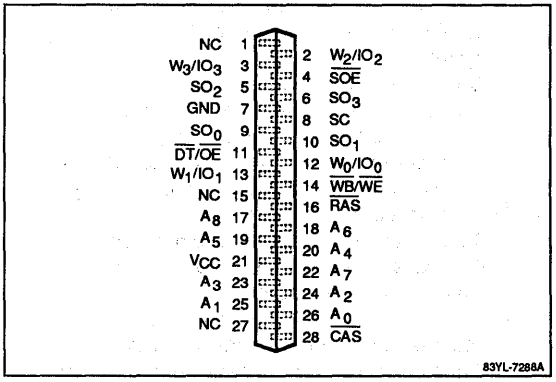
Pin Configurations

28-Pin Plastic SOJ



28-Pin Plastic ZIP



Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
W_0/IO_0 - W_3/IO_3	Write-per-bit selects/data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB/WE}$	Write-per-bit/write enable
$\overline{DT/OE}$	Data transfer/output enable
SO_0 - SO_3	Serial read outputs
SC	Serial control
$\overline{SOE}$	Serial output enable
GND	Ground
V_{CC}	+5-volt ±10% power supply
NC	No connection

Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42273LE-10	100 ns	30 ns	28-pin plastic SOJ
LE-12	120 ns	40 ns	
μPD42273V-10	100 ns	30 ns	28-pin plastic ZIP
V-12	120 ns	40 ns	

Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

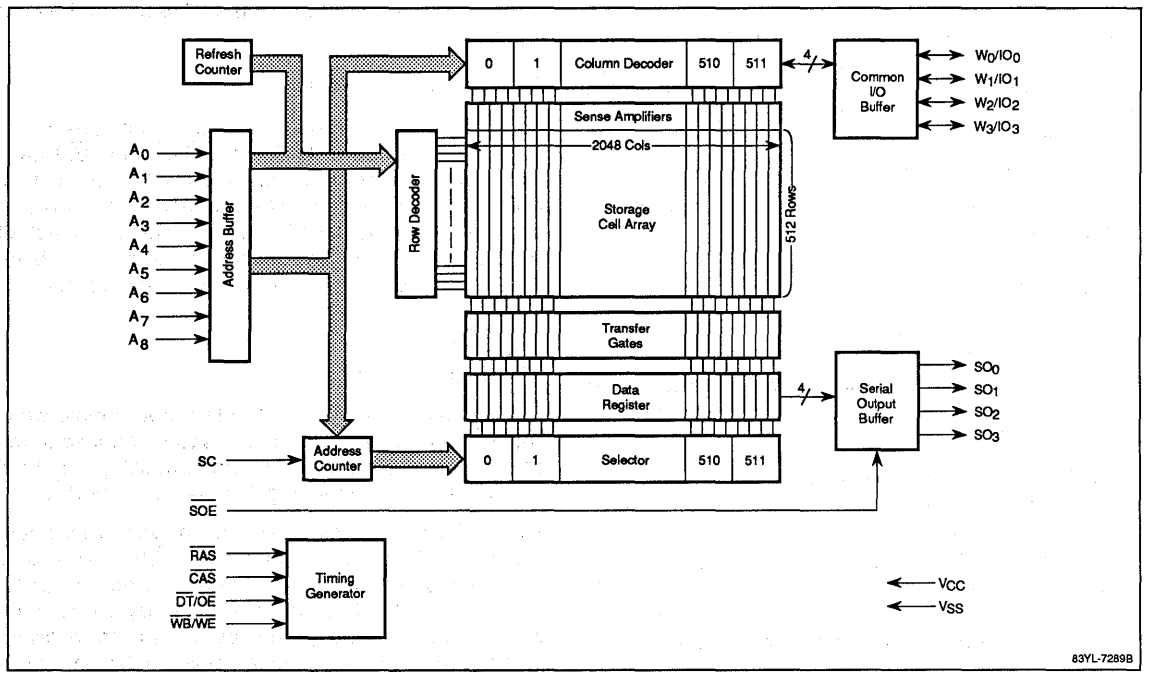
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Limit (max)	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 through A_8
	$C_{I(\overline{DT/OE})}$	8	pF	$\overline{DT/OE}$
	$C_{I(\overline{WB/WE})}$	8	pF	$\overline{WB/WE}$
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 through W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 through SO_3

Block Diagram



Pin Functions

A_0-A_8 (Address Inputs). These pins are multiplexed as row and column address inputs. Each of four data bits in the random access port corresponds to 262,144 storage cells, which means that nine row addresses and nine column addresses are required to decode one cell location. Nine row addresses are first used to select one of the 512 possible rows for a read, write, data transfer, or refresh cycle. Nine column addresses are then used to select the one of 512 possible column decoders for a read or write cycle or the one of 512 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{RAS}$-only refresh or flash write cycles.)

W_0/IO_0-W_3/IO_3 (Write-Per-Bit Inputs/Common Data Inputs and Outputs). Each of the four data bits can be individually latched by these inputs at the falling edge of $\overline{RAS}$ in a write cycle, and then updated at the next falling edge of $\overline{RAS}$. In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$ or $\overline{WE}$.

$\overline{RAS}$ (Row Address Strobe). This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 2,048 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The nine row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{DT/OE}$ and $\overline{WB/WE}$ are simultaneously latched to determine device operation.

$\overline{CAS}$ (Column Address Strobe). This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The nine column address bits are latched at the falling edge of $\overline{CAS}$.

$\overline{WB/WE}$ (Write-Per-Bit Control/Write Enable). At the falling edge of $\overline{RAS}$ the $\overline{WB/WE}$ input must be low and $\overline{CAS}$ and $\overline{DT/OE}$ high to enable the write- per-bit option. A high $\overline{WB/WE}$ can be used at the beginning of a standard write or read cycle.

$\overline{DT/OE}$ (Data Transfer/Output Enable). At the falling edge of $\overline{RAS}$, $\overline{CAS}$ high and FWE and $\overline{DT/OE}$ low initiate a data transfer, regardless of the level of $\overline{WB/WE}$. $\overline{DT/OE}$ high initiates conventional read or write cycles and controls the output buffer in the random access port.

SO_0-SO_3 (Serial Data Output). Four-bit data is read from these pins. Data remains valid until the next SC signal is activated.

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SC (Serial Control). Repeatedly activating this signal causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2,048 bits in the data register. The rising edge of SC activates serial read operation, in which four of the 2,048 data bits are transferred to four serial data buses, respectively, and read out. Whenever SC is low, the serial port is in standby.

$\overline{SOE}$ (Serial Output Enable). This signal controls the serial data output buffer.

OPERATION

The μPD42273 consists of a random access port and a serial read port. The random access port executes standard read and write cycles as well as data transfer and flash write cycles, all of which are based on conventional $\overline{RAS}/\overline{CAS}$ timing.

In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to its corresponding register location. The serial read port shows the contents of the data register in serial order. The random access and serial read ports can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is arranged in a 512-row by 2048-column matrix, whereby each of 4 data bits in the random access port corresponds to 262,144 storage cells and 18 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 through A_8 and latched onto the chip by $\overline{RAS}$. Nine column address bits then are set up on pins A_0 through A_8 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 2048 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through 1 of 512 column decoders, 4 storage cells on the row are connected to 4 data buses, respectively. In a data transfer cycle, 9 row address bits are used to select 1 of the 512 possible rows involved in the transfer of data to the data register. Nine column address bits are then used to select the 1 of 512 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 4 data bits in the 2048-bit data register are transferred to 4 serial data buses and read out. Activating SC repeatedly causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2048 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following are multiplexed.

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

$\overline{OE}$, $\overline{WE}$ and IO_i represent standard operations, while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

The level of $\overline{DT}$ determines whether a cycle is a random access or data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_i defines data bits to be written with the write-per-bit option. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD42273 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls to disconnect the 2048-bit register from the corresponding 2048-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 2048 transfer gates and transfer data from one of the rows to the register.

Truth Table for the Random Access Port

$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Cycle
H	H	H	Read or write (Note 1)
H	H	L	Mask write (Note 2)
H	L	X	Read data transfer (Note 3)
L	X	X	$\overline{CAS}$ before $\overline{RAS}$ refresh (Note 4)

Notes:

(1) Initiates a normal read or write cycle and disables the write-per-bit capability.

(2) Enables individual bits to be selected or masked for a write cycle. Four-bit masked data is latched at the falling edge of $\overline{RAS}$ and reset at the rising edge of $\overline{RAS}$.

(3) Initiates a read data transfer cycle.

(4) Initiates a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. As $\overline{RAS}$ falls, $\overline{WB}/\overline{WE}$ and $\overline{DT}/\overline{OE}$ = don't care.

(5) X = don't care.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining ($\overline{WB}$/)$\overline{WE}$ while $\overline{CAS}$ is active. The (W_i/)IO_i pin (i = 0, 1, 2, 3) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to ±CAS delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance.

Write Cycle. A write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes the data on (W_i/)IO_i into the on-chip data latch. To make use of the write-per-bit option, $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case, write data bits can be specified by keeping W_i(/IO_i) high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

For those data bits of W_i(/IO_i) that are kept low as $\overline{RAS}$ falls, write operation is inhibited on the chip. If $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit option is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low before $\overline{CAS}$ falls. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, ($\overline{DT}$/)$\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$, but otherwise ($\overline{DT}$/)$\overline{OE}$ does not affect anything while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. This cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i returns to high impedance when ($\overline{DT}$/)$\overline{OE}$ goes high. The data to be written is strobed by ($\overline{WB}$/)$\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of ($\overline{DT}$/)$\overline{OE}$, which can be activated just after ($\overline{WB}$/)$\overline{WE}$ falls, even when ($\overline{WB}$/)$\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 through A_8) will refresh all storage cells. Any read, write, refresh, or data transfer cycle executed in the random access port refreshes the 2048 bits selected by the $\overline{RAS}$ addresses or by the on-chip address counter.

$\overline{RAS}$-Only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes all cells in one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep (W_i/)IO_i in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, the row addresses specified by the internal counter are automatically refreshed and the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This cycle is executed after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

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Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed causes data to be transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. In fast-page operation, read, write and read-write/read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the next fast-page write cycle.

During a fast-page read cycle, (W_i/)IO_i remains in high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be one of the following calculated intervals:

Fast-Page Access Time

Calculated Interval	Conditions
t_{ACP}	$t_{ASC} \geq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
t_{AA}	$t_{ASC} \leq t_{ASC}$ (max) and $t_{CP} \geq t_{CP}$ (max)
	$t_{ASC} \leq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
t_{CAC}	$t_{ASC} \geq t_{ASC}$ (max) and $t_{CP} \leq t_{CP}$ (max)

Data Transfer Cycle. A data transfer is executed by bringing $\overline{DT}(/\overline{OE})$ low as $\overline{RAS}$ falls. $\overline{DT}(/\overline{OE})$ must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$. The specified 1 of the possible 512 rows involved in the data transfer, as well as the starting location of the following serial read cycle, are defined by address inputs. The low-to-high transition of $\overline{DT}$ causes column address buffer outputs to be transferred to the serial address counters, and storage cell data amplified on digit lines to be transferred to the data register. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the data in the random access port.

Serial Read Port

After the data transfer cycle, the serial read port is only used to serially read the contents of the data register starting from a specified location. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}(/\overline{OE})$ must occur within a specified period in an SC cycle. Otherwise, the serial read port can operate asynchronously. Output data appears at SO_i after an access time of t_{SCA}, measured from SC high, only when $\overline{SOE}$ is maintained low. The SC cycle which includes the positive transition of $\overline{DT}(/\overline{OE})$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD42273 graphics buffers into the same external circuitry. When $\overline{SOE}$ is at a low logic level, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is high, SO_i is disabled and in a state of high impedance.

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Port Operation			μPD42273-10	μPD42273-12		
Random Access	**Serial Read**	**Parameter**	**(max)**	**(max)**	**Unit**	**Test Conditions**
Read/write cycle	Standby	I_{CC1}	95	85	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Standby	Standby	I_{CC2}	4	4	mA	$\overline{CAS}$ = $\overline{RAS}$ = V_{IH}; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	95	85	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 2)
Fast-page cycle	Standby	I_{CC4}	90	80	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	95	85	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Data transfer cycle	Standby	I_{CC6}	135	120	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Read/write cycle	Active	I_{CC7}	120	105	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Standby	Active	I_{CC8}	30	25	mA	$\overline{CAS}$ = $\overline{RAS}$ = V_{IH}; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	120	105	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Fast-page cycle	Active	I_{CC10}	115	100	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	120	105	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Data transfer cycle	Active	I_{CC12}	160	140	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, I_{CC6}, and I_{CC14}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked, but is kept at a stable high level. Column addresses are also assumed to be at a stable high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −2 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −1 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 2.1 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

		μPD42273-10		μPD42273-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Switching Characteristics							
Access time from $\overline{RAS}$	t_{RAC}		100		120	ns	(Notes 3, 4 and 12)
Access time from falling edge of $\overline{CAS}$	t_{CAC}		25		30	ns	(Notes 3, 4, 13, 14 and 15)
Access time from column address	t_{AA}		55		65	ns	(Notes 3, 4, 14 and 15)
Access time from rising edge of $\overline{CAS}$	t_{ACP}		55		65	ns	(Notes 3 and 4)
Access time from $\overline{OE}$	t_{OEA}		25		30	ns	(Notes 3 and 4)
Serial output access time from SC	t_{SCA}		30		40	ns	(Notes 3 and 18)
Serial output access time from $\overline{SOE}$	t_{SOA}		25		30	ns	(Note 3)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	25	0	30	ns	(Note 5)
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	25	0	30	ns	(Note 5)
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	15	0	20	ns	(Note 5)
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		ns	
Serial output hold time after SC high	t_{SOH}	5		5		ns	
Timing Requirements							
Random read or write cycle time	t_{RC}	190		220		ns	(Note 11)
Read-write/read-modify-write cycle time	t_{RWC}	255		295		ns	(Note 11)
Fast-page cycle time	t_{PC}	60		70		ns	(Note 11)
Fast-page read-write/read-modify-write cycle time	t_{PRWC}	125		145		ns	(Note 11)
Rise and fall transition time	t_T	3	50	3	50	ns	(Notes 3, 10 and 18)
$\overline{RAS}$ precharge time	t_{RP}	80		90		ns	(Note 18)
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	10		15		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	25	15	30	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}	25	75	25	90	ns	(Note 4)
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		ns	(Note 16)

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AC Characteristics (cont)

Parameter	Symbol	μPD42273-10 Min	μPD42273-10 Max	μPD42273-12 Min	μPD42273-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	12		15		ns	
Column address setup time	t_{ASC}	0	25	0	30	ns	(Note 15)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	45	20	55	ns	(Notes 9 and 14)
Column address to $\overline{RAS}$ lead time	t_{RAL}	55		65		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns	(Note 6)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns	(Note 6)
Write command setup time	t_{WCS}	0		0		ns	(Note 7)
Write command hold time	t_{WCH}	20		30		ns	
Write command pulse width	t_{WP}	20		25		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		35		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 8)
Data-in hold time	t_{DH}	20		25		ns	(Note 8)
Column address to $\overline{WE}$ delay	t_{AWD}	85		100		ns	(Note 7)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	55		65		ns	(Note 7)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130		155		ns	(Note 7)
$\overline{OE}$ high to data-in setup delay	t_{OED}	30		35		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	25		30		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	0		0		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	15		20		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		ns	
Refresh interval	t_{REF}		8		8	ms	Addresses A_0 through A_8
$\overline{DT}$ low setup time	t_{DLS}	0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{RDH}	80		90		ns	(Note 18)
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	30		35		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	10		15		ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	10		15		ns	
Serial clock cycle time	t_{SCC}	30		40		ns	(Note 11)
SC pulse width	t_{SCH}	10		15		ns	
SC precharge time	t_{SCL}	10		15		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		ns	
$\overline{DT}$ high hold time	t_{DHH}	15		20		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	10		10		ns	
$\overline{DT}$ high to $\overline{CAS}$ high delay	t_{DTC}	5		5		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42273-10 Min	μPD42273-10 Max	μPD42273-12 Min	μPD42273-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	
Write-per-bit hold time	t_{WBH}	15		20		ns	
Write bit selection setup time	t_{WS}	0		0		ns	
Write bit selection hold time	t_{WH}	15		20		ns	
$\overline{SOE}$ pulse width	t_{SOE}	10		15		ns	
$\overline{SOE}$ precharge time	t_{SOP}	10		15		ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	15		20		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles and four data transfer (DT) cycles, before proper device operation is achieved.

(3) See input/output timing waveforms for timing reference voltages. See figures 3 and 4 for output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}, t_{OEA}, or t_{AA}.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(7) t_{WCS}, t_{AWD}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{AWD} \geq t_{AWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of $\overline{WB}/\overline{WE}$ in delayed write or read-modify-write cycles.

(9) Assumes that t_{RAD} (min) = t_{RAH} (min) + typical t_T of 5 ns.

(10) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(11) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(12) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(13) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(14) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(15) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(16) The t_{CRP} requirement is applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(17) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(18) Improvement in parameters t_{RDH}, t_{RP} and t_{SCA} are planned for process versions "x" and "m". Please contact your NEC sales office for details.

(19) Ac measurements assume t_T = 5 ns.

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Figure 1. Input Timing

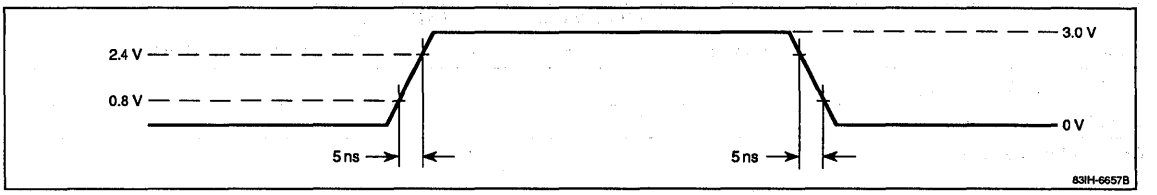


Figure 2. Output Timing

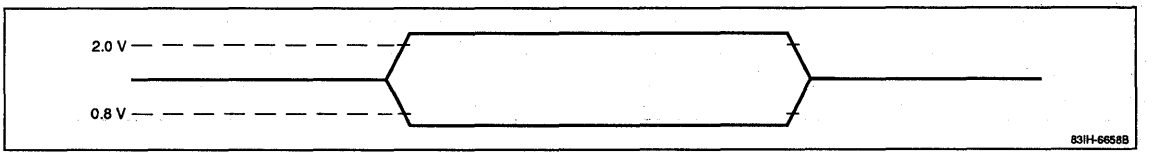


Figure 3. Output Load in Random Access Port

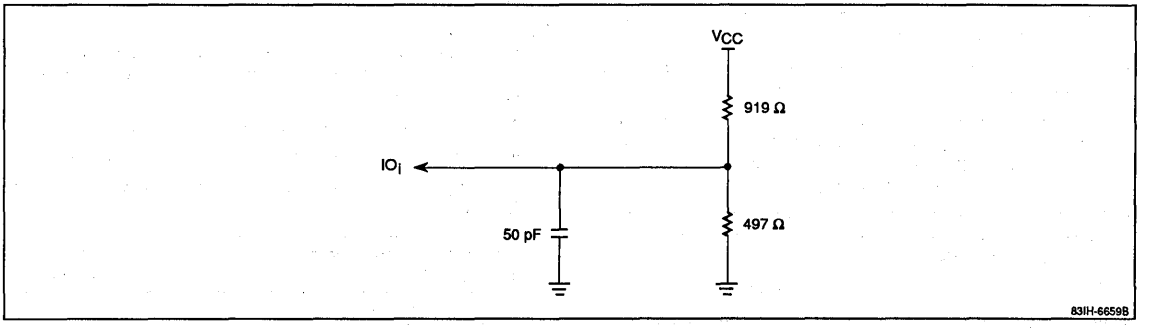
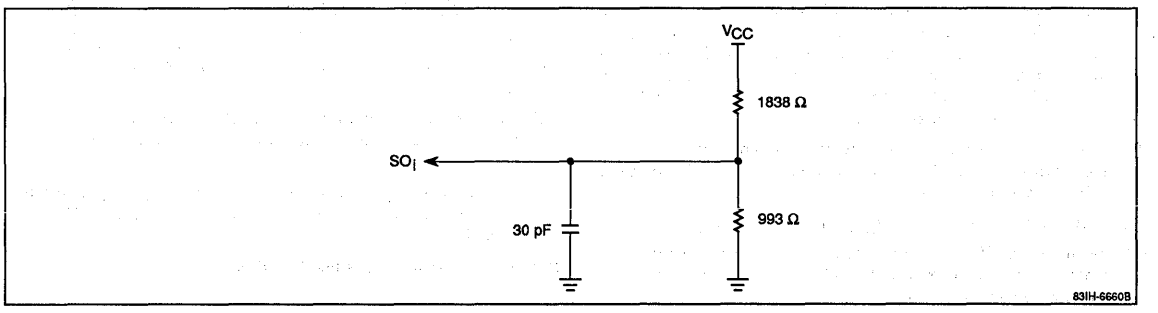
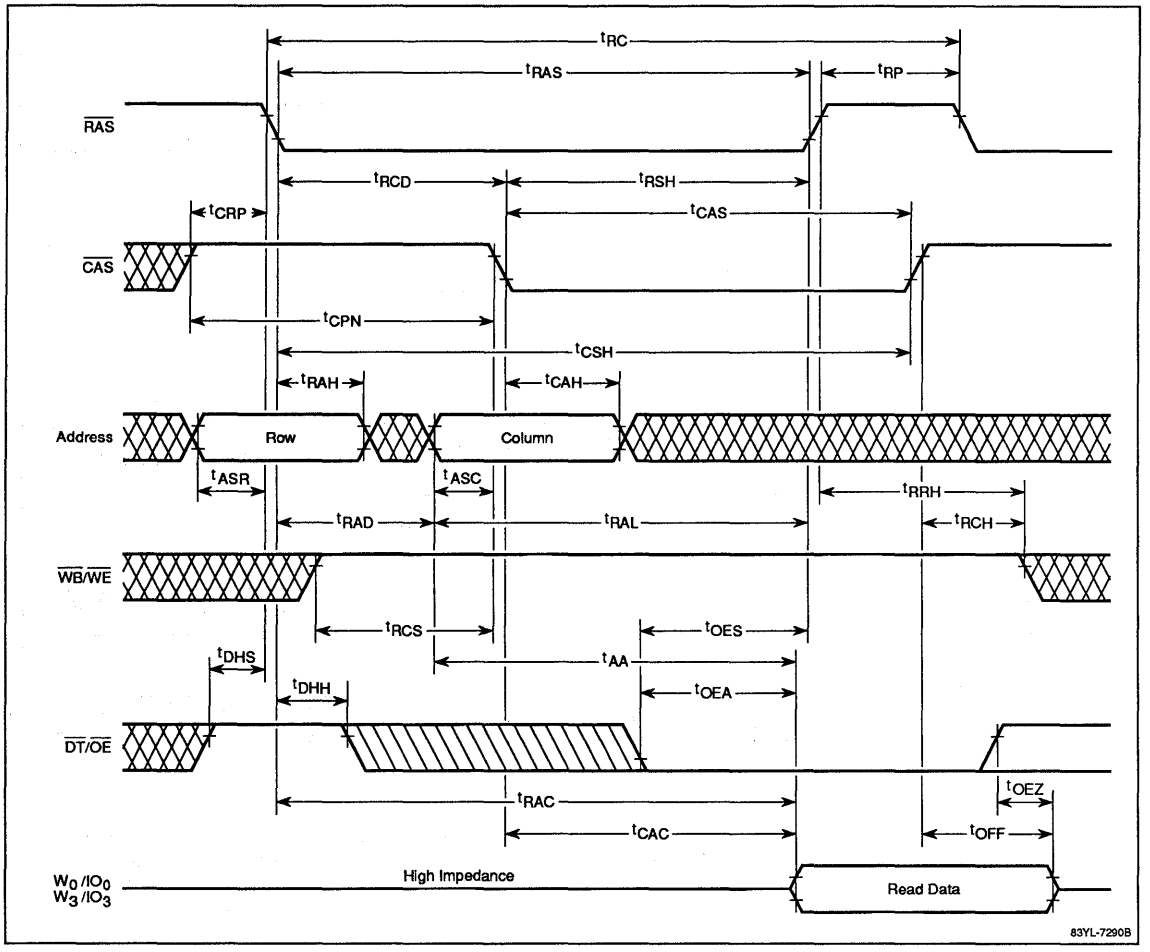


Figure 4. Output Load in Serial Read Port



Timing Waveforms

Read Cycle



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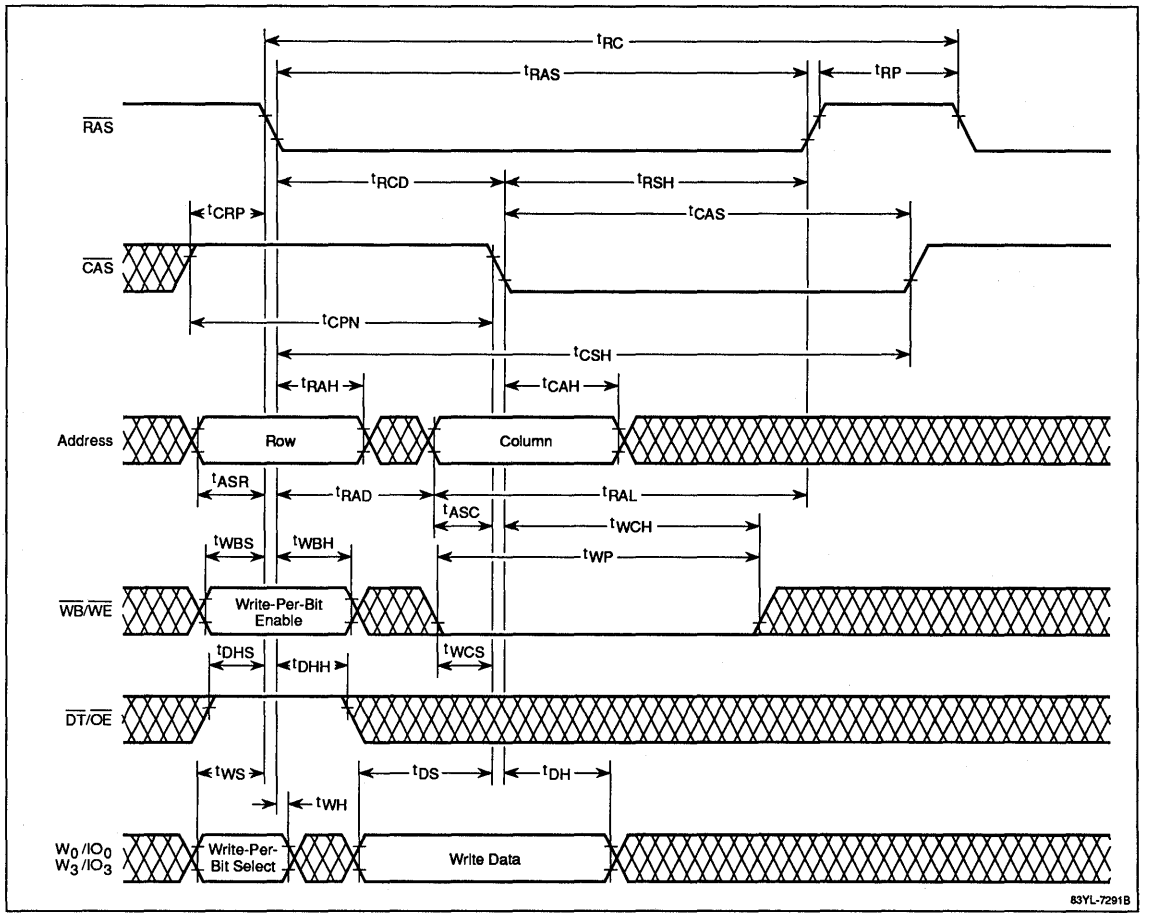
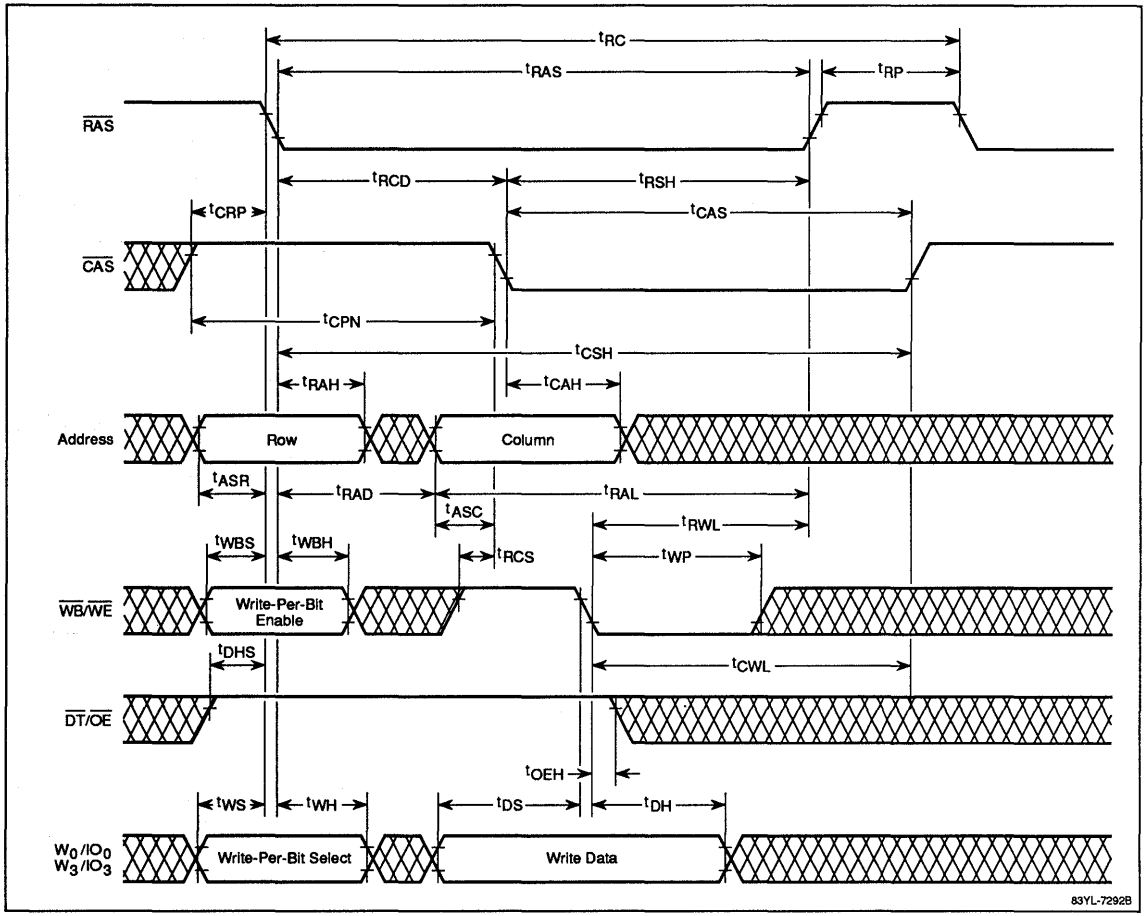
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Late Write Cycle



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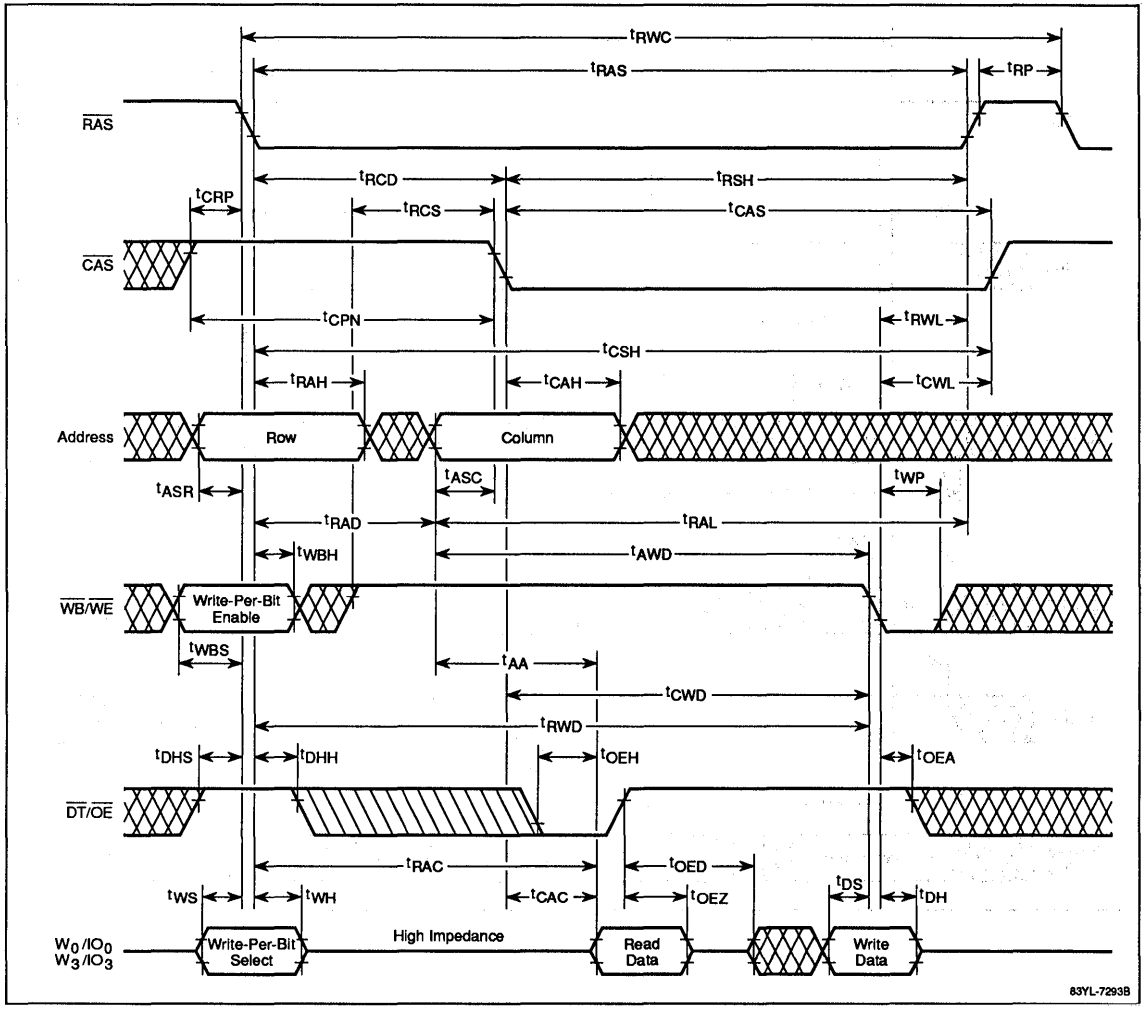
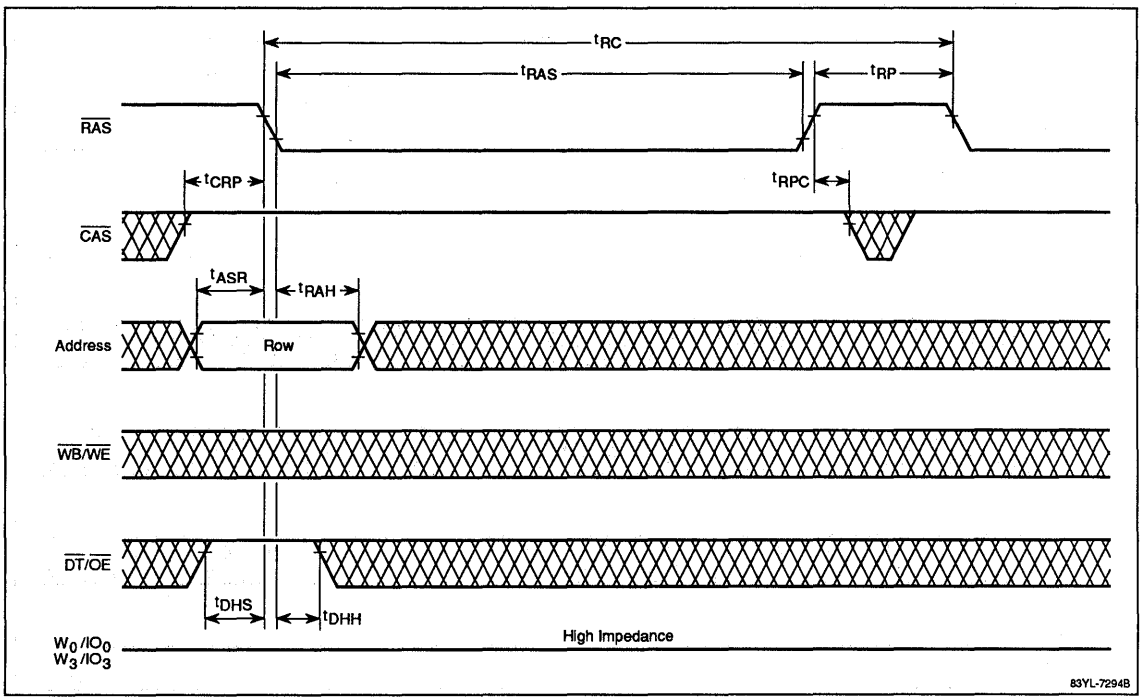
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



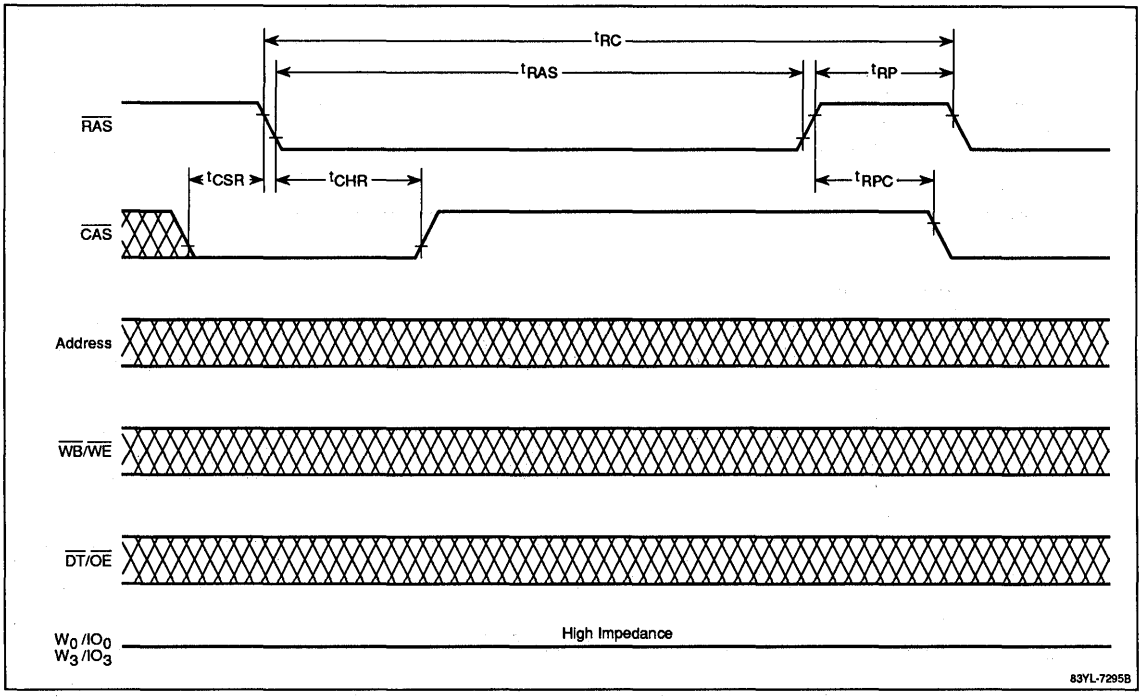
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



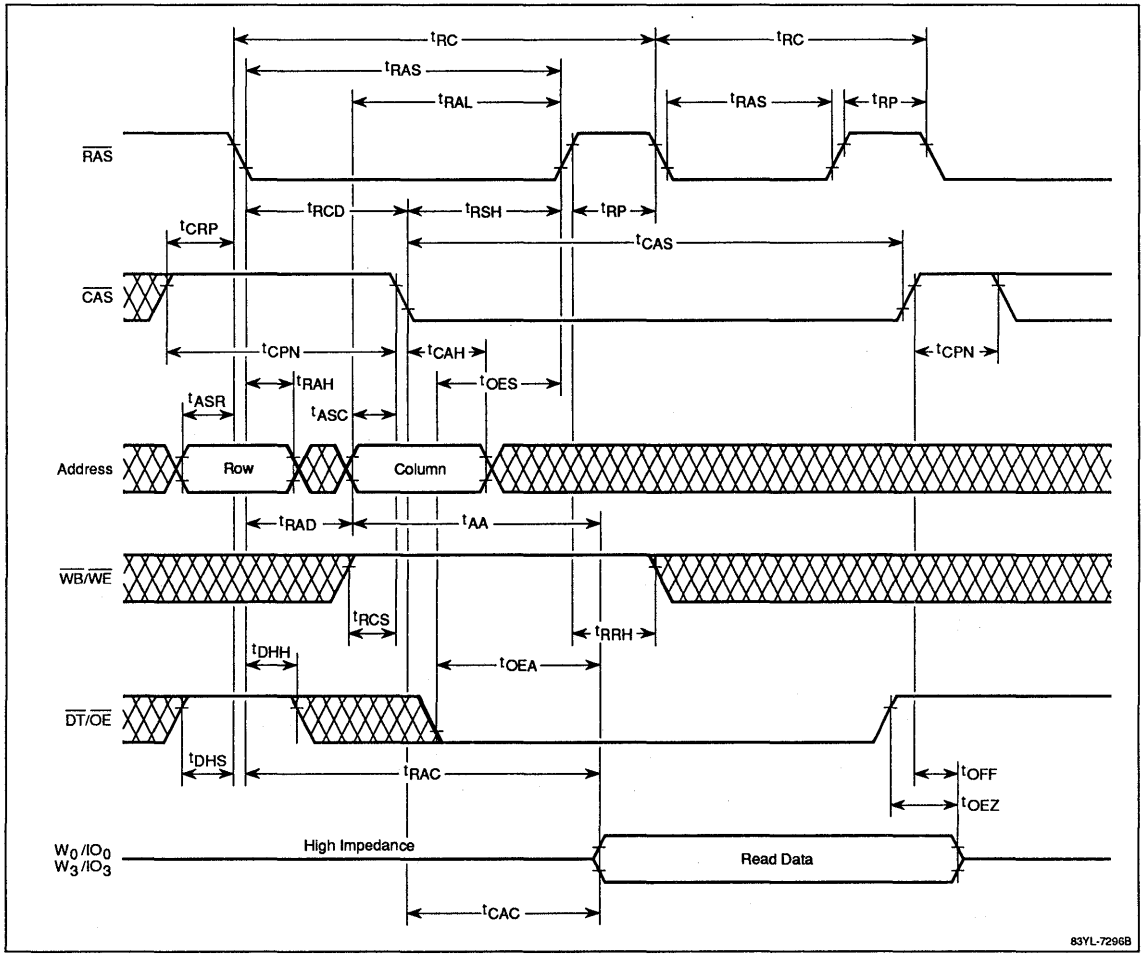
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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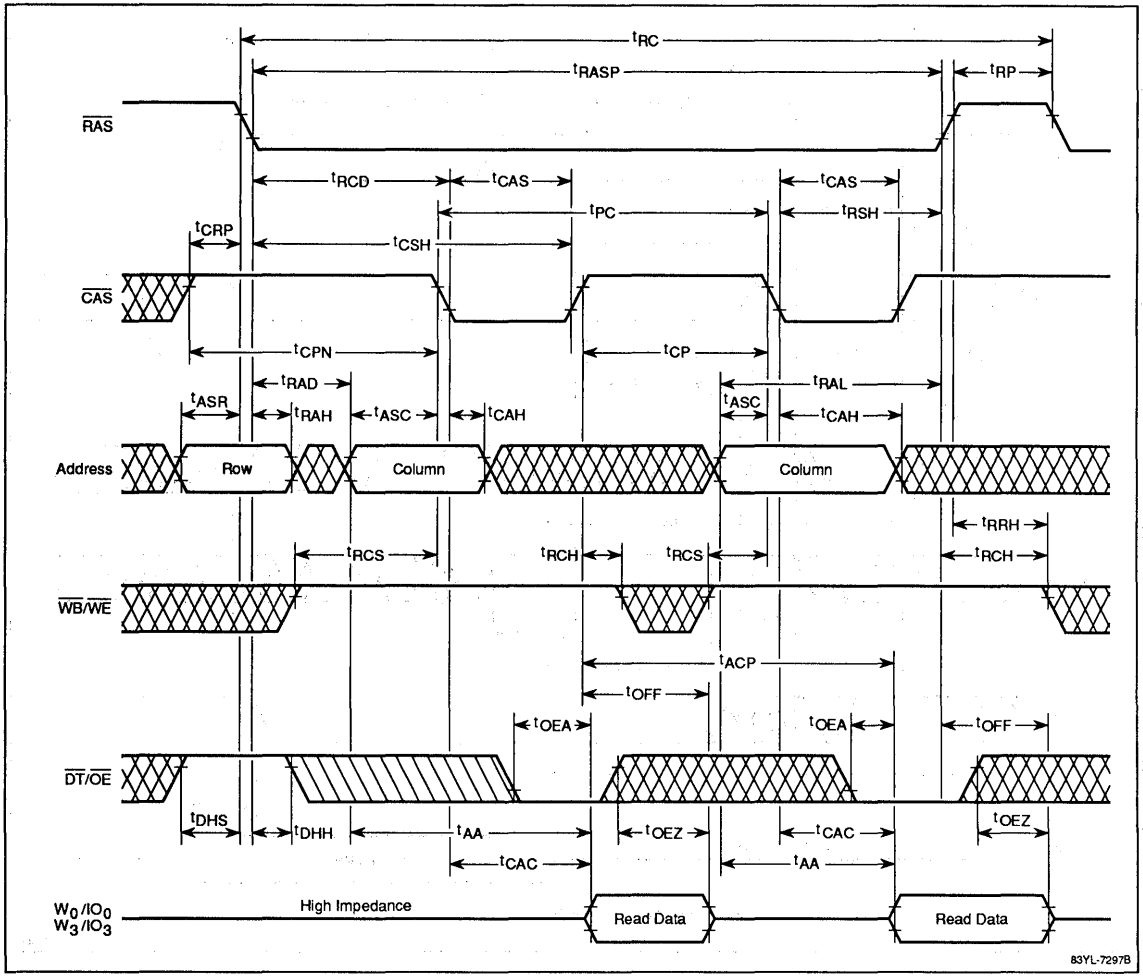
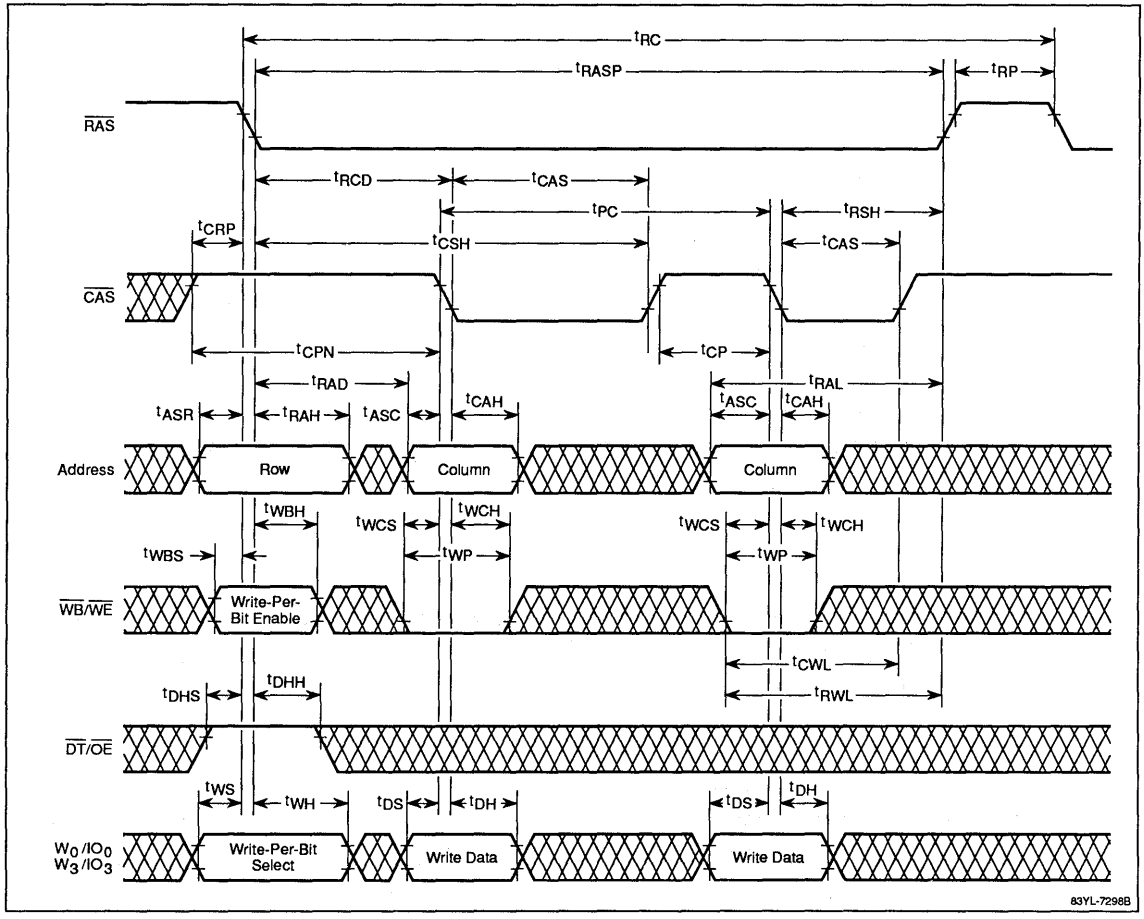
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Write Cycle



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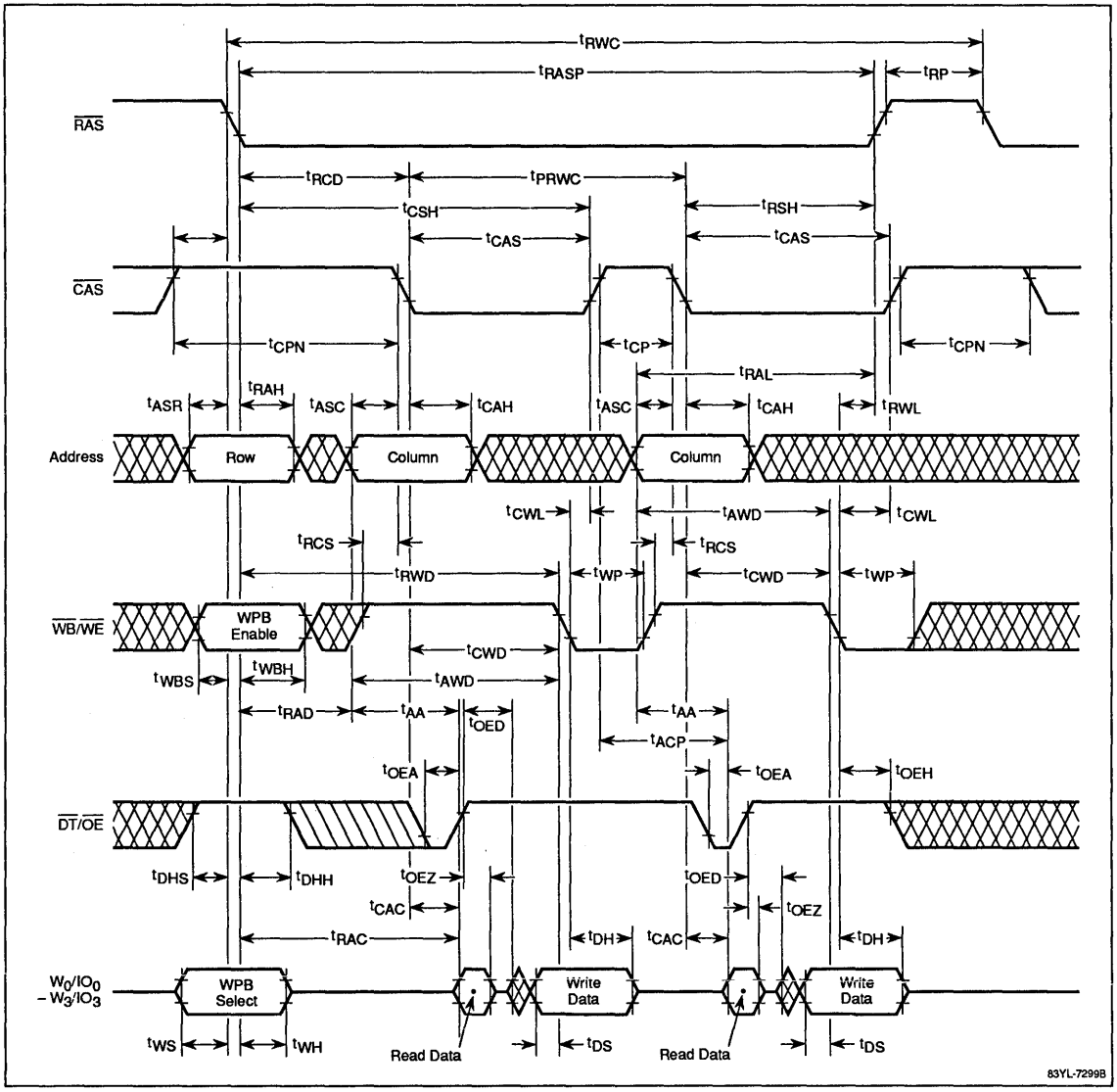
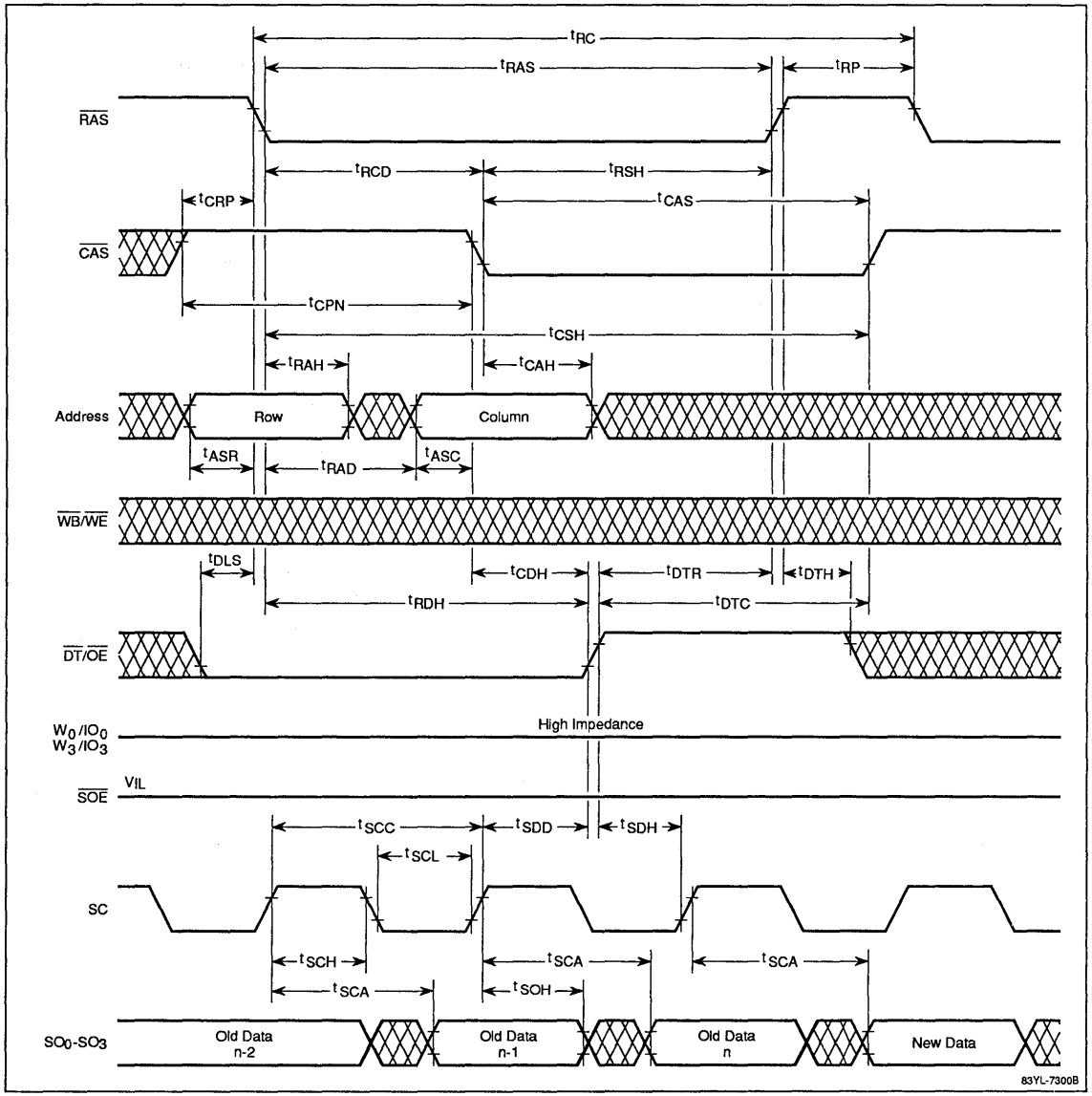
Timing Waveforms (cont)

Fast-Page Read-Modify-Write Cycle



Timing Waveforms (cont)

Data Transfer Cycle with Serial Port Active



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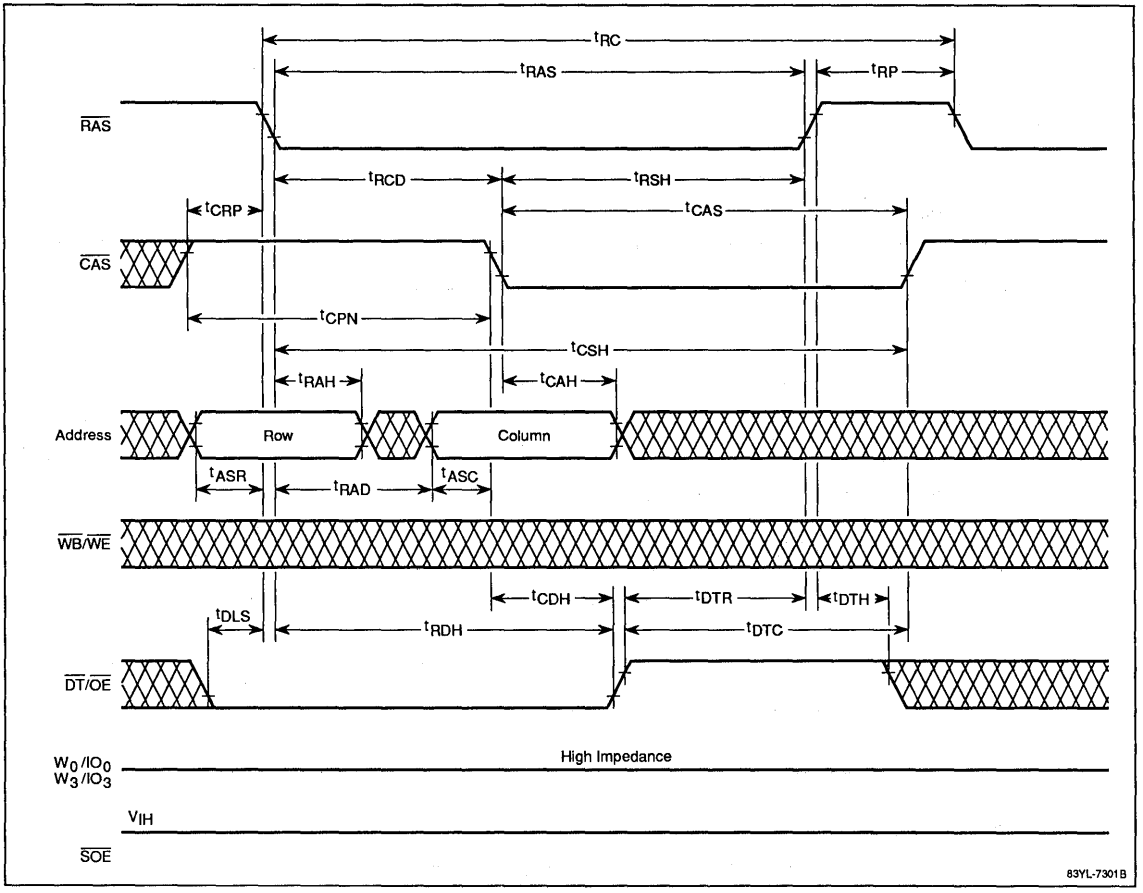
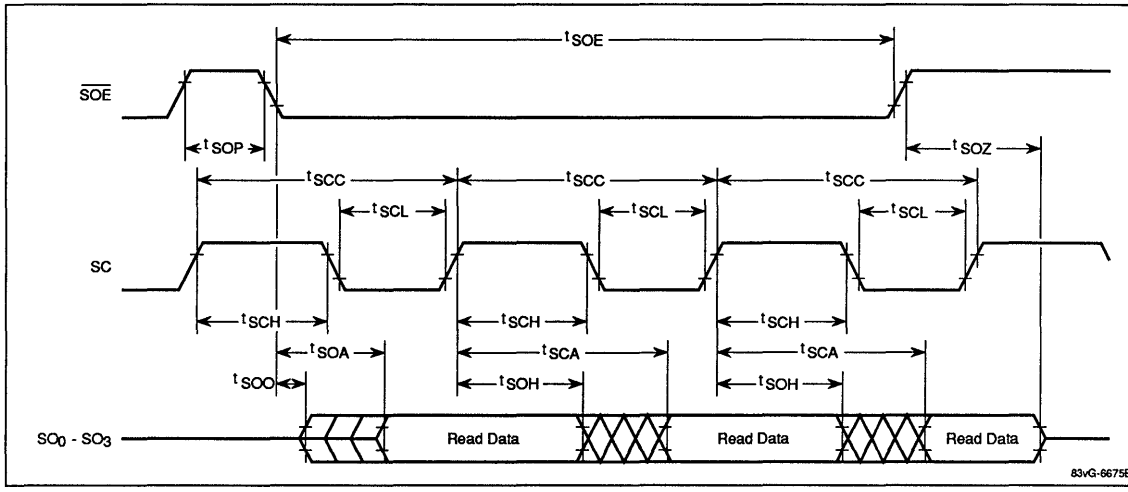
Timing Waveforms (cont)

Data Transfer Cycle with Serial Port in Standby



Timing Waveforms (cont)

Serial Read Cycle



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μPD42274
Dual-Port Graphics Buffer

Description

The μPD42274 is a dual-port graphics buffer equipped with a 256K x 4-bit random access port and a 512 x 4-bit serial read port. The serial read port is connected to an internal 2048-bit data register through a 512 x 4-bit serial read output circuit. The random access port is used by the host CPU to read or write data addressed in any desired order. A write-per-bit capability allows each of the four data bits to be individually selected or masked for a write cycle. Furthermore, a flash write option with write-per-bit control enables data in the color register to be written to a selected row in the random access port.

The μPD42274 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock; the serial read port continues to operate normally. Following the clock transition of a data transfer, serial output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

An advanced CMOS silicon-gate process using polycide technology and trench capacitors provides high storage cell density, high performance, and high reliability.

Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The μPD42274 is available in a 28-pin plastic ZIP or 28-pin plastic SOJ and is guaranteed for operation at 0 to + 70°C.

Features

- Three functional blocks
  - — 256K x 4-bit random access storage array
  - — 2048-bit data register
  - — 512 x 4-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- Single + 5-volt ±10% power supply
- On-chip substrate bias generator
- Random access port
  - — Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - — Multiplexed address inputs
  - — Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - — 512 refresh cycles every 8 ms
  - — Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page cycles
  - — Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - — $\overline{CAS}$-controlled hidden refreshing
  - — Write-per-bit option regarding four I/O bits
  - — Write bit selection multiplexed on IO_0-IO_3
- Flash write option with write-per-bit control
- $\overline{RAS}$-activated data transfer
  - — Same cycle time as for random access
  - — Row data transferred to data register as specified by row address inputs
  - — Starting location of following serial read cycle specified by column address inputs
  - — Transfer of 2048 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - — Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
- Serial data output on SO_0-SO_3
- Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- CMOS silicon-gate process with trench capacitors

Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42274LE-10	100 ns	30 ns	28-pin plastic SOJ
LE-12	120 ns	40 ns	
μPD42274V-10	100 ns	30 ns	28-pin plastic ZIP
V-12	120 ns	40 ns	

Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
W_0/IO_0 - W_3/IO_3	Write-per-bit selects/data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB/WE}$	Write-per-bit/write enable
$\overline{DT/OE}$	Data transfer/output enable
FWE	Flash write enable
SO_0 - SO_3	Serial read outputs
SC	Serial control
$\overline{SOE}$	Serial output enable
GND	Ground
V_{CC}	+5-volt ±10% power supply
NC	No connection

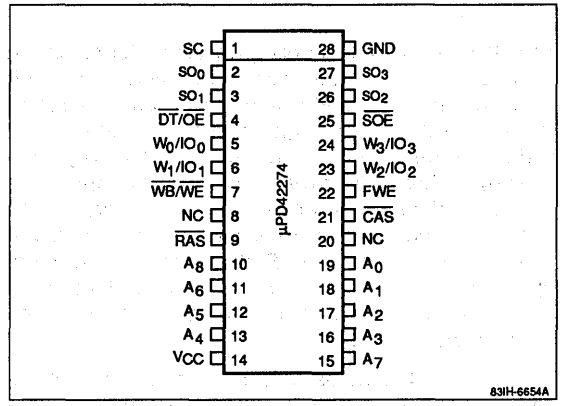
Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

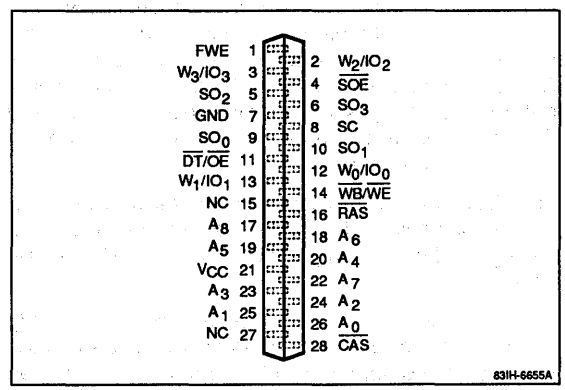
Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Pin Configurations

28-Pin Plastic SOJ



28-Pin Plastic ZIP



Pin Functions

A_0-A_8 (Address Inputs). These pins are multiplexed as row and column address inputs. Each of four data bits in the random access port corresponds to 262,144 storage cells, which means that nine row addresses and nine column addresses are required to decode one cell location. Nine row addresses are first used to select one of the 512 possible rows for a read, write, data transfer, or refresh cycle. Nine column addresses are then used to select the one of 512 possible column decoders for a read or write cycle or the one of 512 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{RAS}$-only refresh or flash write cycles.)

W_0/IO_0-W_3/IO_3 (Write-Per-Bit Inputs/Common Data Inputs and Outputs). Each of the four data bits can be individually latched by these inputs at the falling edge of $\overline{RAS}$ in a write or flash write cycle, and then updated at the next falling edge of $\overline{RAS}$.

In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$ or $\overline{WE}$.

$\overline{RAS}$ (Row Address Strobe). This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 2,048 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The nine row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$, and FWE are simultaneously latched to determine device operation.

$\overline{CAS}$ (Column Address Strobe). This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The nine column address bits are latched at the falling edge of $\overline{CAS}$.

$\overline{WB/WE}$ (Write-Per-Bit Control/Write Enable). At the falling edge of $\overline{RAS}$, the $\overline{WB/WE}$ and FWE inputs must be low and $\overline{CAS}$ and $\overline{DT/OE}$ high to enable the write- per-bit option. When $\overline{CAS}$, $\overline{DT/OE}$ and FWE are high at the falling edge of $\overline{RAS}$, the level of this signal indicates either a color register set cycle or flash write cycle. A high $\overline{WB/WE}$ can be used at the beginning of a standard write or read cycle.

$\overline{DT/OE}$ (Data Transfer/Output Enable). At the falling edge of $\overline{RAS}$, $\overline{CAS}$ high and FWE and $\overline{DT/OE}$ low initiate a data transfer, regardless of the level of $\overline{WB/WE}$. $\overline{DT/OE}$ high initiates conventional read or write cycles and controls the output buffer in the random access port.

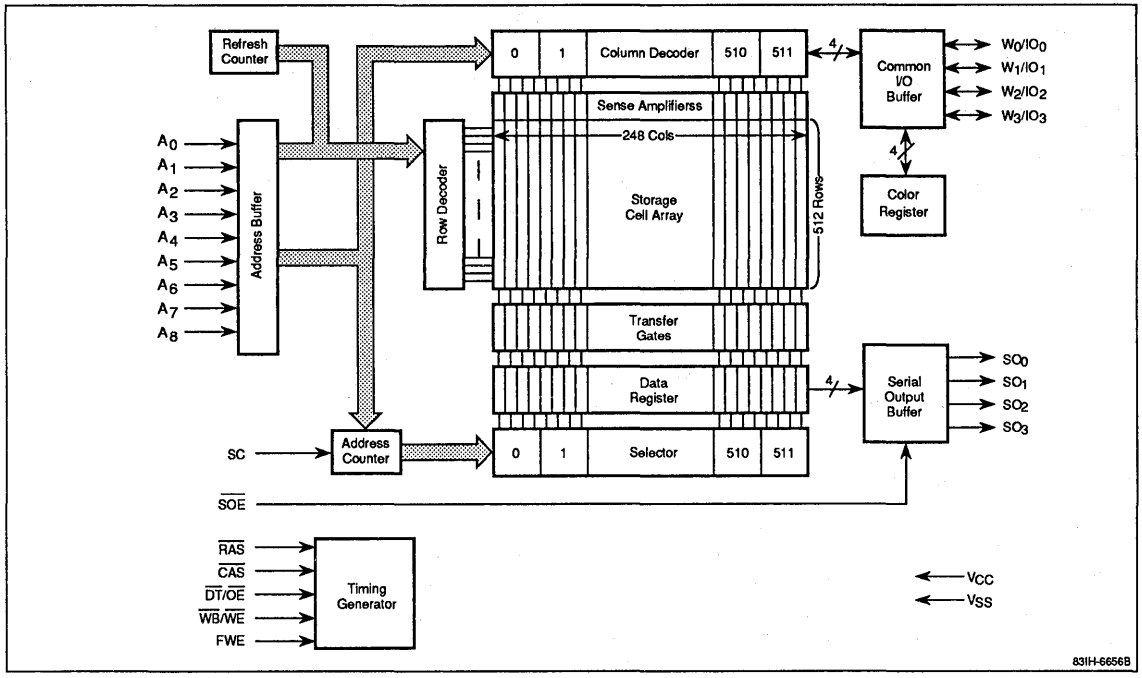
FWE (Flash Write Enable). If this signal is low and $\overline{CAS}$ and $\overline{DT/OE}$ are high at the falling edge of $\overline{RAS}$, a read or write cycle is initiated. If FWE, $\overline{CAS}$ and $\overline{DT/OE}$ are high at the falling edge of $\overline{RAS}$, either a color register set cycle or flash write cycle is initiated, depending on the level of $\overline{WB/WE}$.

SO_0-SO_3 (Serial Data Output). Four-bit data is read from these pins. Data remains valid until the next SC signal is activated.

SC (Serial Control). Repeatedly activating this signal causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2,048 bits in the data register. The rising edge of SC activates serial read operation, in which four of the 2,048 data bits are transferred to four serial data buses, respectively, and read out. Whenever SC is low, the serial port is in standby.

$\overline{SOE}$ (Serial Output Enable). This signal controls the serial data output buffer.

Block Diagram



OPERATION

The μPD42274 consists of a random access port and a serial read port. The random access port executes standard read and write cycles as well as data transfer and flash write cycles, all of which are based on conventional $\overline{RAS}$/$\overline{CAS}$ timing.

In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to its corresponding register location (unless the flash write option is used to write an entire row of data to predetermined values). The serial read port shows the contents of the data register in serial order. The random access and serial read ports can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is arranged in a 512-row by 2048-column matrix, whereby each of 4 data bits in the random access port corresponds to 262,144 storage cells and 18 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 through A_8 and latched onto the chip by $\overline{RAS}$. Nine column address bits then are set up on pins A_0 through A_8 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 2048 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through 1 of 512 column decoders, 4 storage cells on the row are connected to 4 data buses, respectively. In a data transfer cycle, 9 row address bits are used to select 1 of the 512 possible rows involved in the transfer of data to the data register. Nine column address bits are then used to select the 1 of 512 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 4 data bits in the 2048-bit data register are transferred to 4 serial data buses and read out. Activating SC repeatedly causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2048 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following are multiplexed.

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

The $\overline{OE}$, $\overline{WE}$ and IO_i functions represent standard operations, while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

The level of $\overline{DT}$ determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_i defines data bits to be written with the write-per-bit option. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD42274 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 2048-bit register from the corresponding 2048-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 2048 transfer gates and transfer data from one of the rows to the register.

Truth Table for the Random Access Port

$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	FWE	Cycle
H	H	H	L	Read or write (Note 1)
H	H	L	L	Mask write (Note 2)
H	L	X	L	Read data transfer (Note 3)
H	L	H	H	
L	X	X	X	$\overline{CAS}$ before $\overline{RAS}$ refresh (Note 4)
H	H	H	H	Color register set (Note 5)
H	H	L	H	Flash write/write-per-bit (Note 6)

Notes:

(1) Initiates a normal read or write cycle and disables the write-per- bit capability.

(2) Enables the write-per-bit capability, where individual bits can be selected or masked for a write cycle. Four-bit masked data is latched at the falling edge of $\overline{RAS}$ and reset at the rising edge of $\overline{RAS}$.

(3) Initiates a read data transfer cycle.

(4) Initiates a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. As $\overline{RAS}$ falls, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and FWE = don't care.

(5) Defines a color register set cycle, where data in the register can be accessed in a read or write cycle.

(6) Initiates a flash write cycle, where the storage cells on an entire selected row can be set with write-per-bit control to the same data stored in the color register. As $\overline{RAS}$ falls, $\overline{DT}/\overline{OE}$ = don't care. To avoid un-intended flash write operation, the FWE pin should be grounded. If grounding the FWE pin is not possible, use the non-flash write version μPD42273.

(7) X = don't care.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining $(\overline{WB}/)\overline{WE}$ while $\overline{CAS}$ is active. The $(W_i/)IO_i$ pin (i = 0, 1, 2, 3) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\pm\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance.

Write Cycle. A write cycle is executed by bringing (WB/)WE low during the RAS/CAS cycle. The falling edge of CAS or (WB/)WE strobes the data on (W_i/)IO_i into the on-chip data latch. To make use of the write-per-bit option, WB(/WE) must be low as RAS falls. In this case, write data bits can be specified by keeping W_i(/IO_i) high, with setup and hold times referenced to the negative transition of RAS.

For those data bits of W_i(/IO_i) that are kept low as RAS falls, write operation is inhibited on the chip. If WB(/WE) is high as RAS falls, the write-per-bit option is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing (WB/)WE low before CAS falls. Data is strobed by CAS, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As RAS falls, (DT/)OE must meet the setup and hold times of a high DT, but otherwise (DT/)OE does not affect any circuit operation while CAS is active.

Read-Write/Read-Modify-Write Cycle. This cycle is executed by bringing (WB/)WE low with the RAS and CAS signals low. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i returns to high impedance when (DT/)OE goes high. The data to be written is strobed by (WB/)WE, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of (DT/)OE, which can be activated just after (WB/)WE falls, even when (WB/)WE is brought low after CAS.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 through A_8) will refresh all storage cells. Any cycle executed in the random access port (i.e., read, write, refresh, data transfer, color register set, or flash write) refreshes the 2048 bits selected by the RAS addresses or by the on-chip refresh address counter.

RAS-Only Refresh Cycle. A cycle having only RAS active refreshes all cells in one row of the storage array. A high CAS is maintained while RAS is active to keep (W_i/)IO_i in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when RAS-only refresh cycles are executed.

CAS Before RAS Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever CAS is low as RAS falls, this circuitry automatically refreshes the row addresses specified by the internal counter. In this cycle, the circuit operation based on CAS is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next CAS before RAS cycle.

Hidden Refresh Cycle. This cycle is executed after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by CAS and OE. After the read cycle, CAS is held low while RAS goes high for precharge. A RAS-only cycle is then executed (except that CAS is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as CAS before RAS refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining RAS low while successive CAS cycles are executed causes data to be transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. In fast-page operation, read, write and read-write/read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the next fast-page write cycle.

During a fast-page read cycle, the (W_i/)IO_i data pin (i = 0, 1, 2, or 3) remains in a state of high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be one of the following calculated intervals:

Fast-Page Access Time

Calculated Interval	Conditions
t_{ACP}	$t_{ASC} \geq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
t_{AA}	$t_{ASC} \leq t_{ASC}$ (max) and $t_{CP} \geq t_{CP}$ (max)
	$t_{ASC} \leq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
t_{CAC}	$t_{ASC} \geq t_{ASC}$ (max) and $t_{CP} \leq t_{CP}$ (max)

Data Transfer Cycle. A data transfer is executed by bringing $\overline{DT}(/\overline{OE})$ and FWE low as $\overline{RAS}$ falls. The specified 1 of the possible 512 rows involved in the data transfer, as well as the starting location of the following serial read cycle in the serial read port, are defined by address inputs. $\overline{DT}(/\overline{OE})$ must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$, so that the data transfer condition may be satisfied. The low-to-high transition of $\overline{DT}$ causes two operations through the data transfer gates: column address buffer outputs are transferred to the serial address counters, and storage cell data amplified on digit lines is transferred to the data register. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the data in the random access port.

Color Register Set Cycle. A color register set cycle is executed in the same fashion as a conventional read or write cycle, with the level of $\overline{WE}$ high as $\overline{RAS}$ falls. In this cycle, read or write operation is available to the color register under the control of $\overline{WE}$. In read operation, color register data is read out on the common IO_i pins. In write operation, common IO_i data can be written into the color register. $\overline{RAS}$-only refreshing is internally performed on the row selected by A_0 through A_8 in this cycle.

Flash Write Cycle. A flash write cycle can clear or set each of the four 512-bit data sets on the one row selected from among the 512 possible rows according to data stored in the color register. Bit mask inputs are latched as $\overline{RAS}$ falls. This cycle is useful in graphics processing applications when the screen should be cleared or set to some uniform value as quickly as possible.

Serial Read Port

The serial read port is only used to serially read the contents of the data register starting from a specified location. The entire operation, therefore, follows the data transfer cycle. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}(/\overline{OE})$ must occur within a specified period in an SC cycle. Except for this cycle, the serial read port can operate asynchronously. The output data appears at SO_i after an access time of t_{SCA}, measured from SC high, only when $\overline{SOE}$ is maintained low. The SC cycle which includes the positive transition of $\overline{DT}(/\overline{OE})$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD42274 graphics buffers into the same external circuitry. When $\overline{SOE}$ is at a low logic level, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is at a high logic level, SO_i is disabled and in a state of high impedance.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 0 to +70 °C; V_{CC} = +5.0 V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Limit (max)	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 through A_8
	$C_{I(\overline{DT}/\overline{OE})}$	8	pF	$\overline{DT}/\overline{OE}$
	$C_{I(\overline{WB}/\overline{WE})}$	8	pF	$\overline{WB}/\overline{WE}$
	$C_{I(FWE)}$	8	pF	FWE
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 through W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 through SO_3

12d

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Port Operation						
Random Access	Serial Read	Parameter	μPD42274-10 (max)	μPD42274-12 (max)	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	95	85	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; FWE low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Standby	Standby	I_{CC2}	4	4	mA	$\overline{CAS}$ = $\overline{RAS}$ = V_{IH}; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	95	85	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; FWE low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 2)
Fast-page cycle	Standby	I_{CC4}	90	80	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min ; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	95	85	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Data transfer cycle	Standby	I_{CC6}	135	120	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Read/write cycle	Active	I_{CC7}	120	105	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; FWE low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Standby	Active	I_{CC8}	30	25	mA	$\overline{CAS}$ = $\overline{RAS}$ = V_{IH}; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	120	105	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; FWE low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Fast-page cycle	Active	I_{CC10}	115	100	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min ; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	120	105	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Data transfer cycle	Active	I_{CC12}	160	140	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Color register set cycle	Standby	I_{CC13}	95	85	mA	FWE and $\overline{WB}/\overline{WE}$ high as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Flash write cycle	Standby	I_{CC14}	95	85	mA	FWE high and $\overline{WB}/\overline{WE}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Color register set cycle	Active	I_{CC15}	120	105	mA	FWE and $\overline{WB}/\overline{WE}$ high as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Flash write cycle	Active	I_{CC16}	120	105	mA	FWE high and $\overline{WB}/\overline{WE}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, I_{CC6}, and I_{CC14}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked, but is kept at a stable high level. The column addresses are also assumed to be kept stable, at either a high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −2 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −1 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 2.1 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

		μPD42274-10		μPD42274-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Switching Characteristics							
Access time from $\overline{RAS}$	t_{RAC}		100		120	ns	(Notes 3, 4 and 12)
Access time from falling edge of $\overline{CAS}$	t_{CAC}		25		30	ns	(Notes 3, 4, 13, 14 and 15)
Access time from column address	t_{AA}		55		65	ns	(Notes 3, 4, 14 and 15)
Access time from rising edge of $\overline{CAS}$	t_{ACP}		55		65	ns	(Notes 3 and 4)
Access time from $\overline{OE}$	t_{OEA}		25		30	ns	(Notes 3 and 4)
Serial output access time from SC	t_{SCA}		30		40	ns	(Notes 3 and 18)
Serial output access time from $\overline{SOE}$	t_{SOA}		25		30	ns	(Note 3)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	25	0	30	ns	(Note 5)
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	25	0	30	ns	(Note 5)
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	15	0	20	ns	(Note 5)
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		ns	
Serial output hold time after SC high	t_{SOH}	5		5		ns	
Timing Requirements							
Random read or write cycle time	t_{RC}	190		220		ns	(Note 11)
Read-write/read-modify-write cycle time	t_{RWC}	255		295		ns	(Note 11)
Fast-page cycle time	t_{PC}	60		70		ns	(Note 11)
Fast-page read-write/read-modify-write cycle time	t_{PRWC}	125		145		ns	(Note 11)
Rise and fall transition time	t_T	3	50	3	50	ns	(Notes 3, 10 and 18)
$\overline{RAS}$ precharge time	t_{RP}	80		90		ns	(Note 18)
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	10		15		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	25	15	30	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}	25	75	25	90	ns	(Note 4)
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		ns	(Note 16)

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AC Characteristics (cont)

Parameter	Symbol	μPD42274-10 Min	μPD42274-10 Max	μPD42274-12 Min	μPD42274-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	12		15		ns	
Column address setup time	t_{ASC}	0	25	0	30	ns	(Note 15)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	45	20	55	ns	(Notes 9 and 14)
Column address to $\overline{RAS}$ lead time	t_{RAL}	55		65		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns	(Note 6)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns	(Note 6)
Write command setup time	t_{WCS}	0		0		ns	(Note 7)
Write command hold time	t_{WCH}	20		30		ns	
Write command pulse width	t_{WP}	20		25		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		35		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 8)
Data-in hold time	t_{DH}	20		25		ns	(Note 8)
Column address to $\overline{WE}$ delay	t_{AWD}	85		100		ns	(Note 7)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	55		65		ns	(Note 7)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130		155		ns	(Note 7)
$\overline{OE}$ high to data-in setup delay	t_{OED}	30		35		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	25		30		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	0		0		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	15		20		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		ns	
Refresh interval	t_{REF}		8		8	ms	Addresses A_0 through A_8
$\overline{DT}$ low setup time	t_{DLS}	0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{RDH}	80		90		ns	(Note 18)
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	30		35		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	10		15		ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	10		15		ns	
Serial clock cycle time	t_{SCC}	30		40		ns	(Note 11)
SC pulse width	t_{SCH}	10		15		ns	
SC precharge time	t_{SCL}	10		15		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		ns	
$\overline{DT}$ high hold time	t_{DHH}	15		20		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	10		10		ns	
$\overline{DT}$ high to $\overline{CAS}$ high delay	t_{DTC}	5		5		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42274-10 Min	μPD42274-10 Max	μPD42274-12 Min	μPD42274-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
Write-per-bit hold time	t_{WBH}	15		20		ns	
Flash write enable setup time	t_{FWS}	0		0		ns	
Flash write enable hold time	t_{FWH}	15		20		ns	
Write bit selection setup time	t_{WS}	0		0		ns	
Write bit selection hold time	t_{WH}	15		20		ns	
$\overline{SOE}$ pulse width	t_{SOE}	10		15		ns	
$\overline{SOE}$ precharge time	t_{SOP}	10		15		ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	15		20		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles and four data transfer (DT) cycles, before proper device operation is achieved.

(3) See input/output timing waveforms for timing reference voltages. See figures 3 and 4 for output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}, t_{OEA}, or t_{AA}.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(7) t_{WCS}, t_{AWD}, t_{CWD}, and t_{RWD} are restrictive operating parameter in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{AWD} \geq t_{AWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of (WB/)$\overline{WE}$ in delayed write or read-modify-write cycles.

(9) Assumes that t_{RAD} (min) = t_{RAH} (min) + typical t_T of 5 ns.

(10) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(11) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(12) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(13) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(14) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(15) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(16) The t_{CRP} requirement is applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(17) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(18) Improvement in parameters t_{RDH}, t_{RP} and t_{SCA} are planned for process versions "x" and "m". Please contact your NEC sales office for details.

(19) Ac measurements assume t_T = 5 ns.

Figure 1. Input Timing

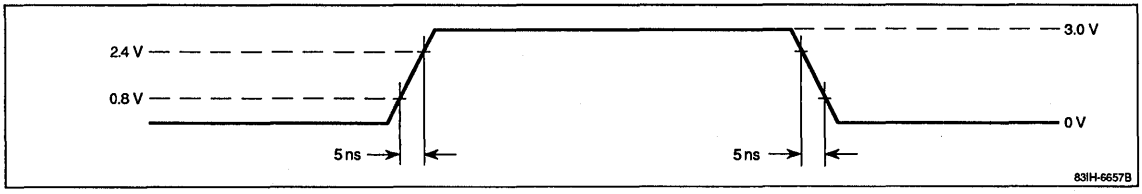


Figure 2. Output Timing

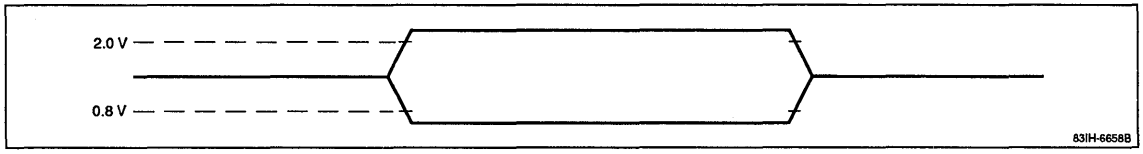


Figure 3. Output Load in Random Access Port

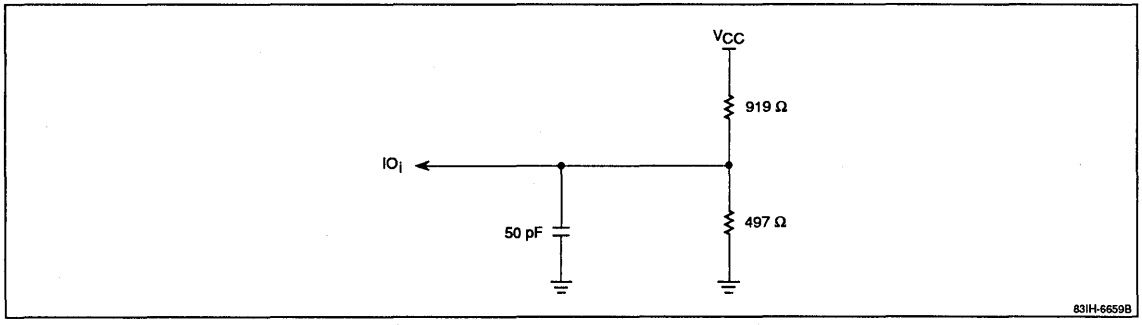
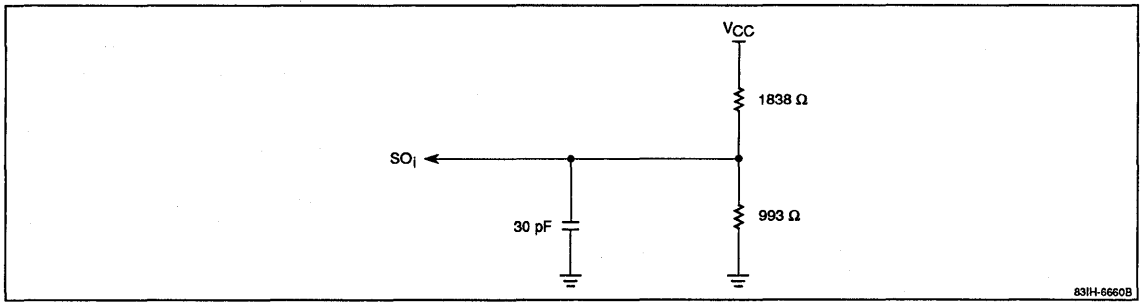
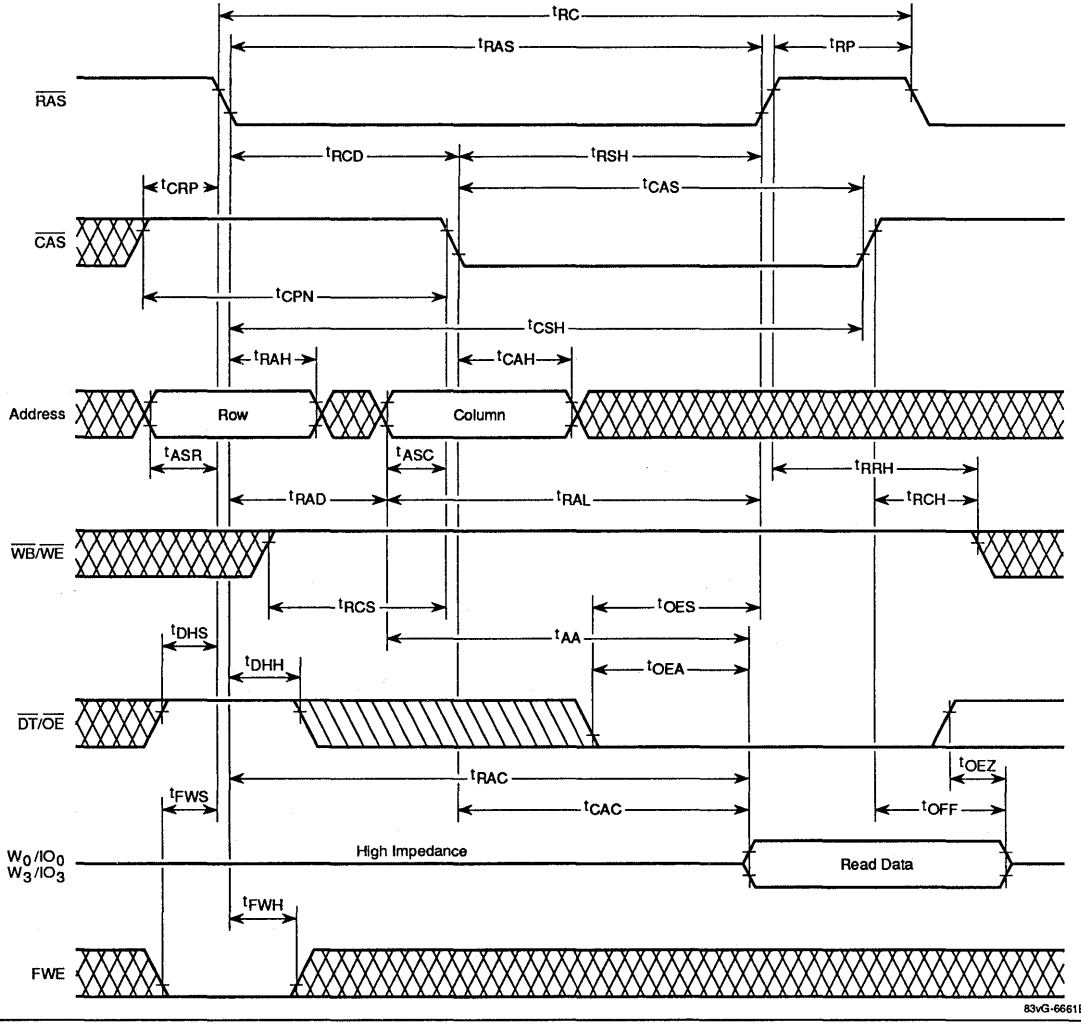


Figure 4. Output Load in Serial Read Port



Timing Waveforms

Read Cycle



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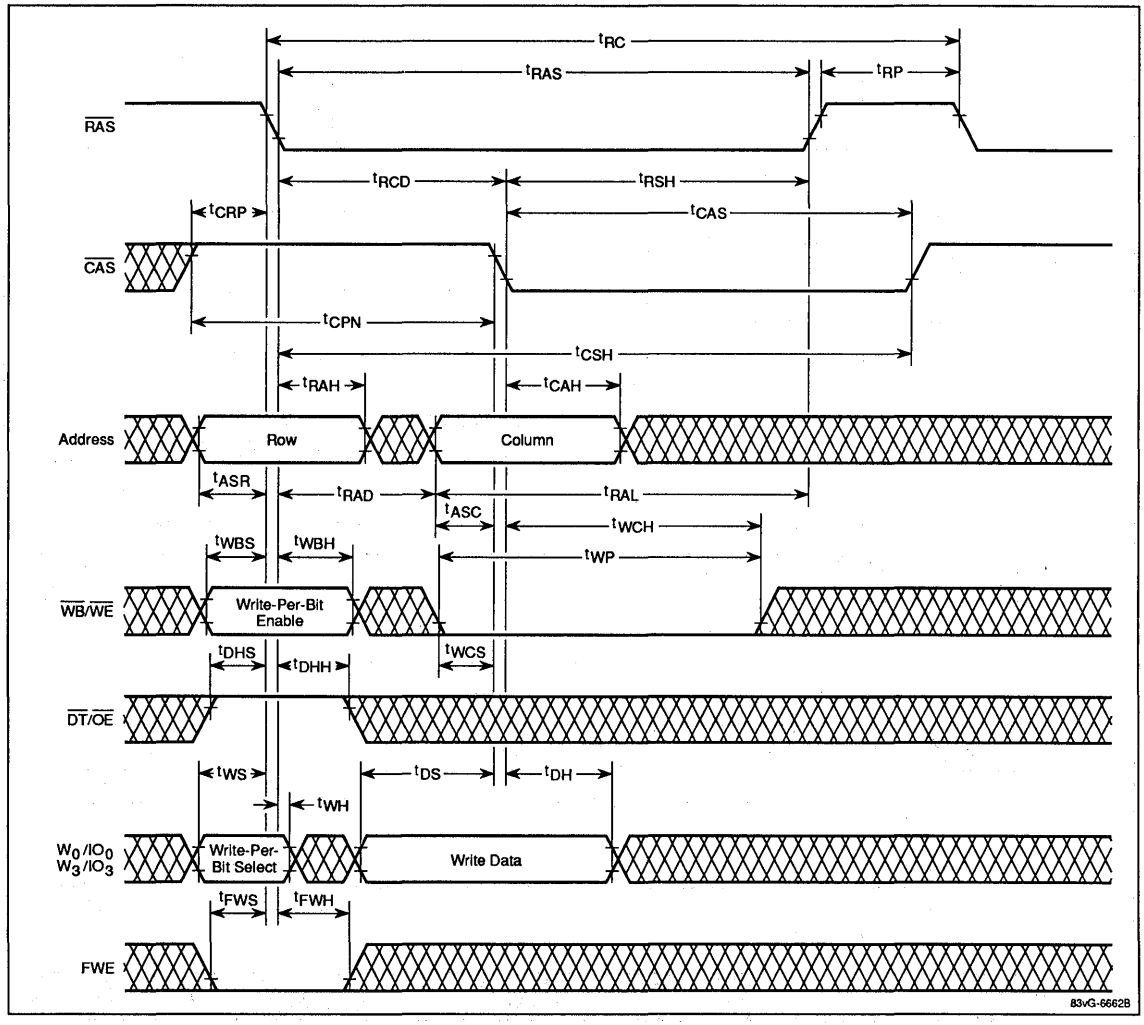
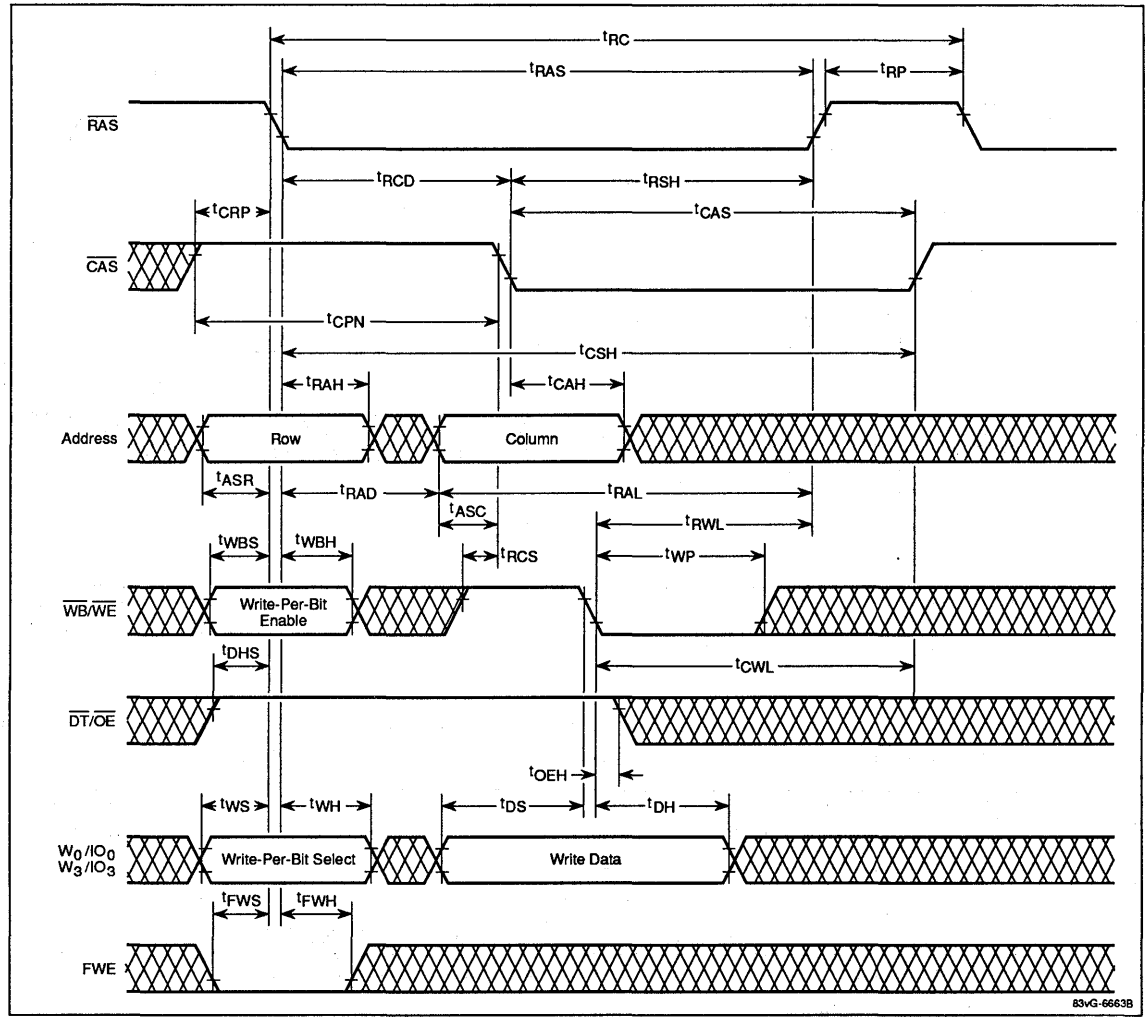
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

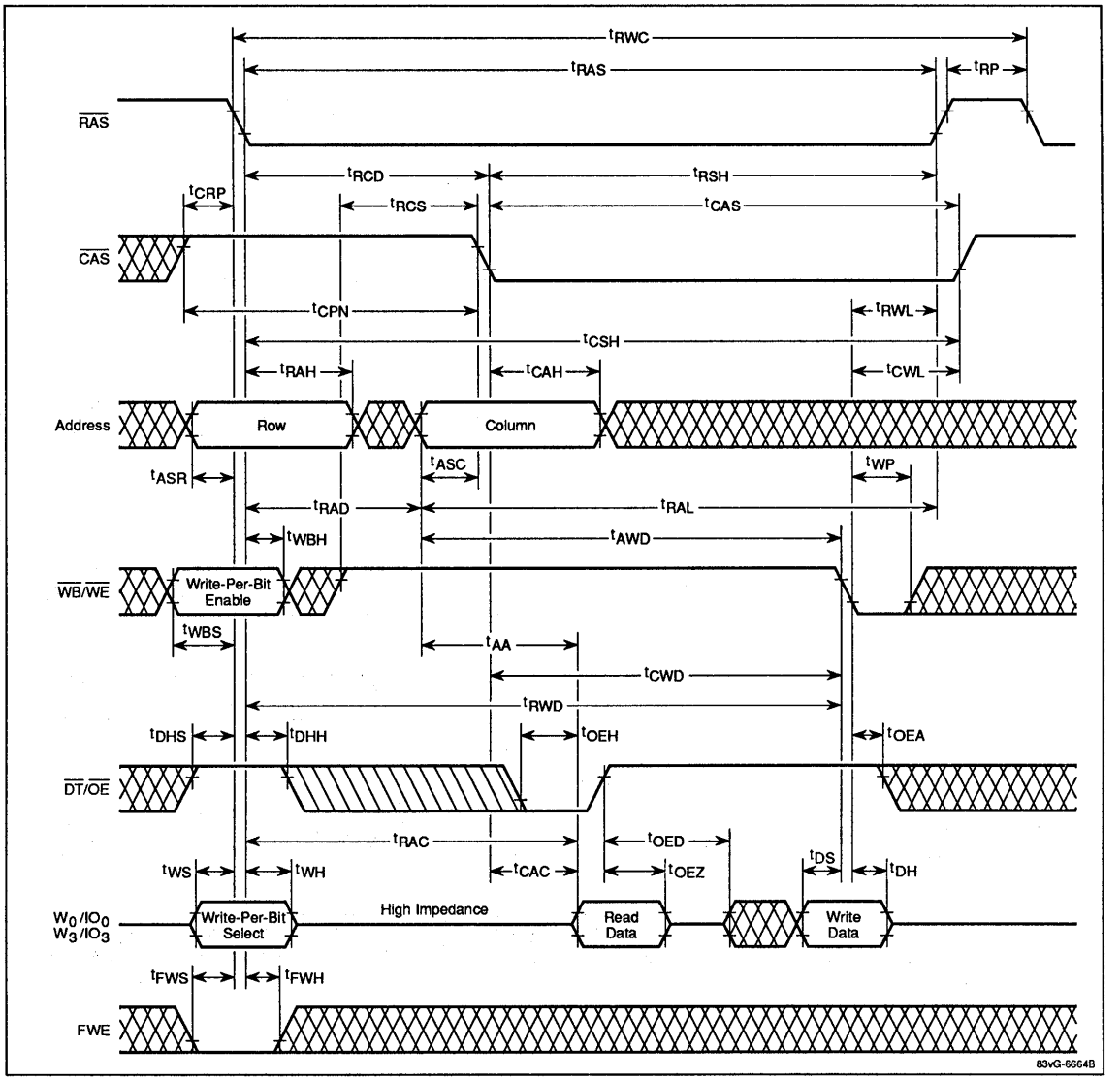
Late Write Cycle



12d

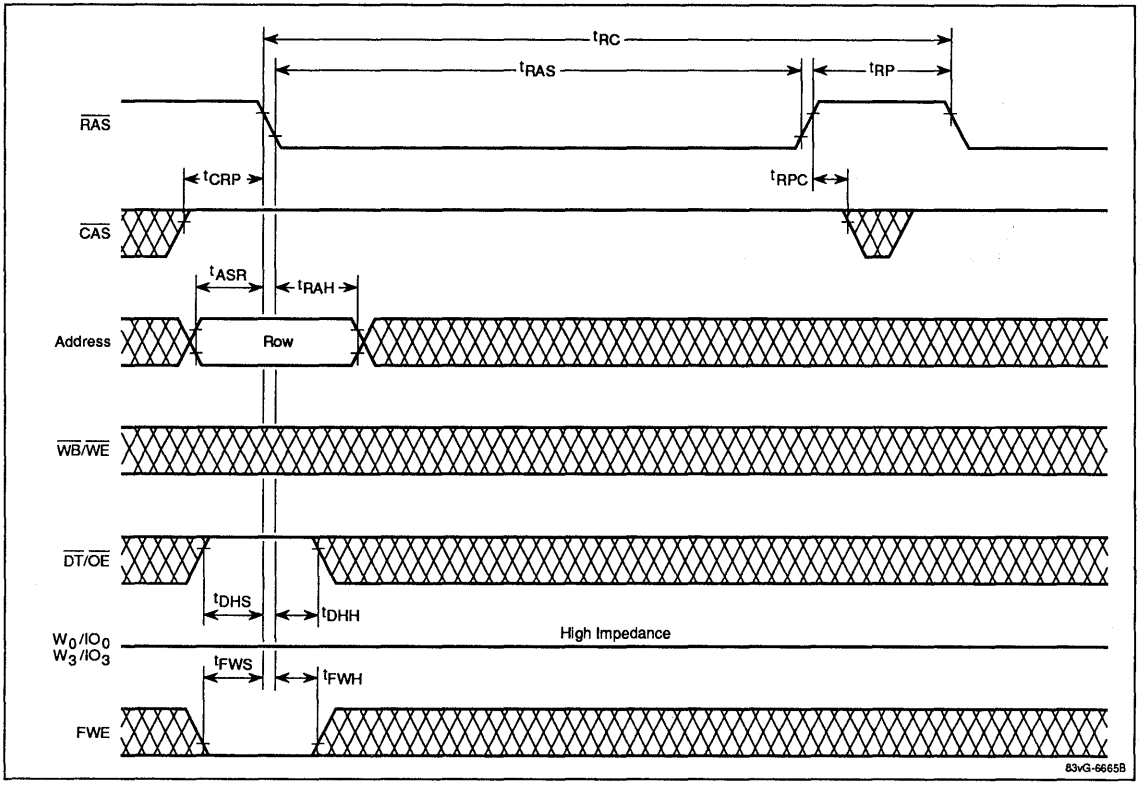
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



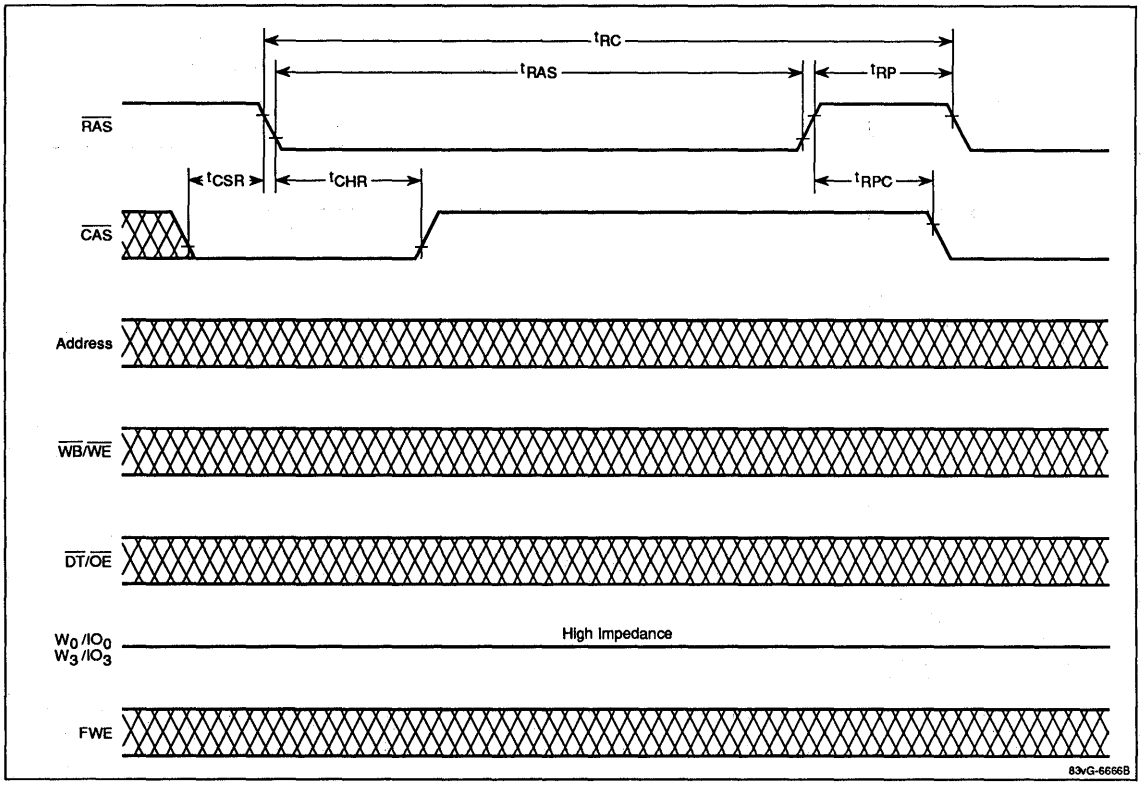
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



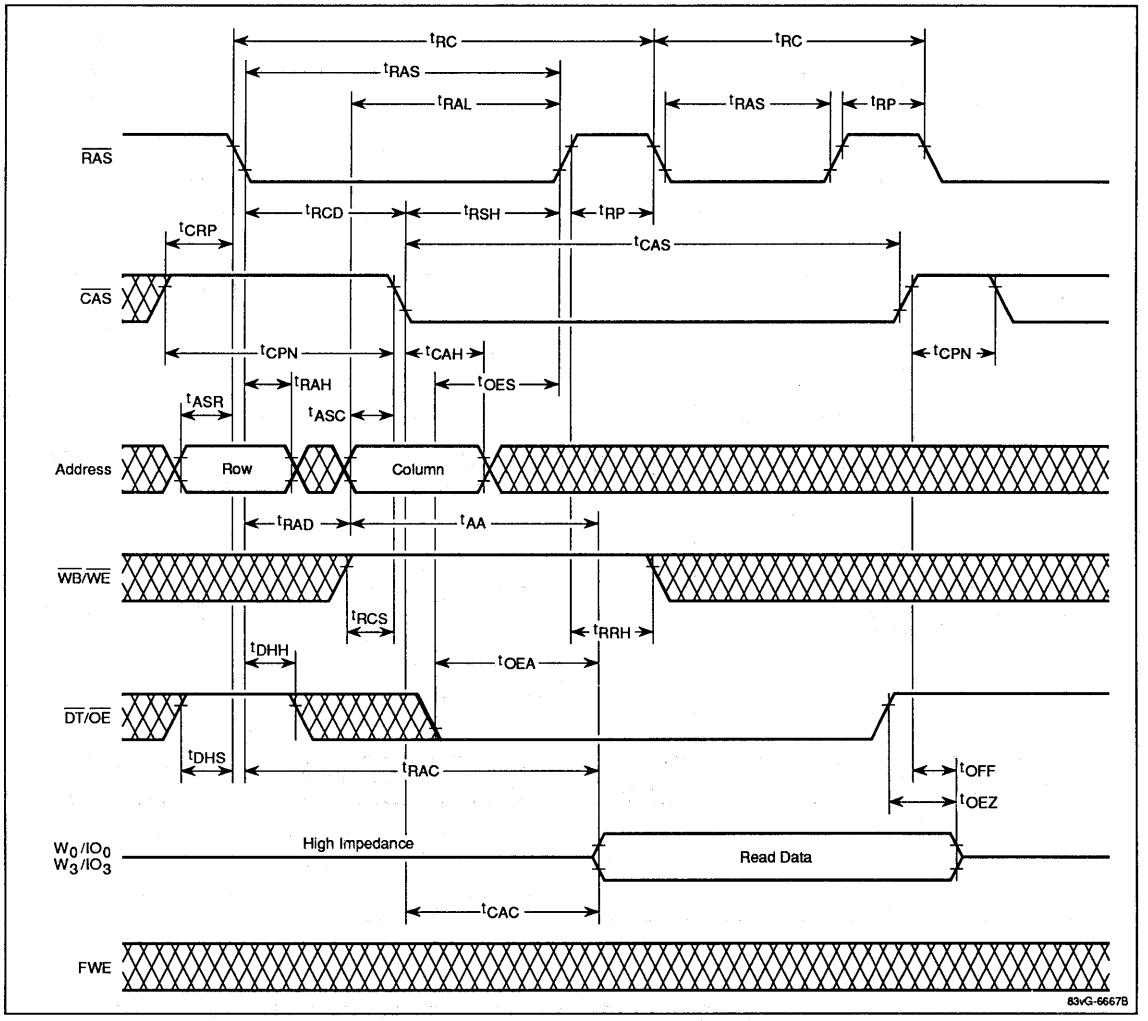
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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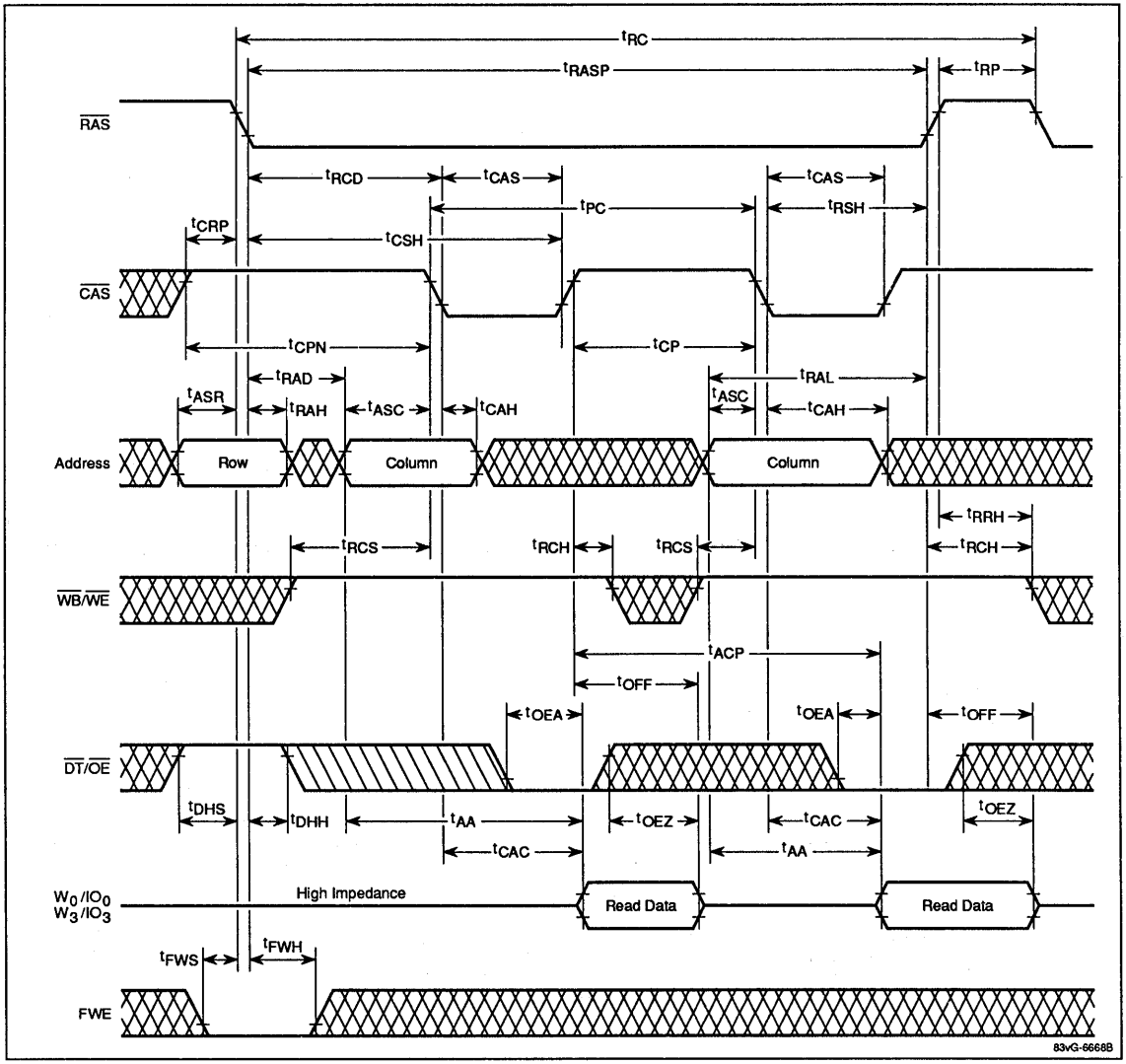
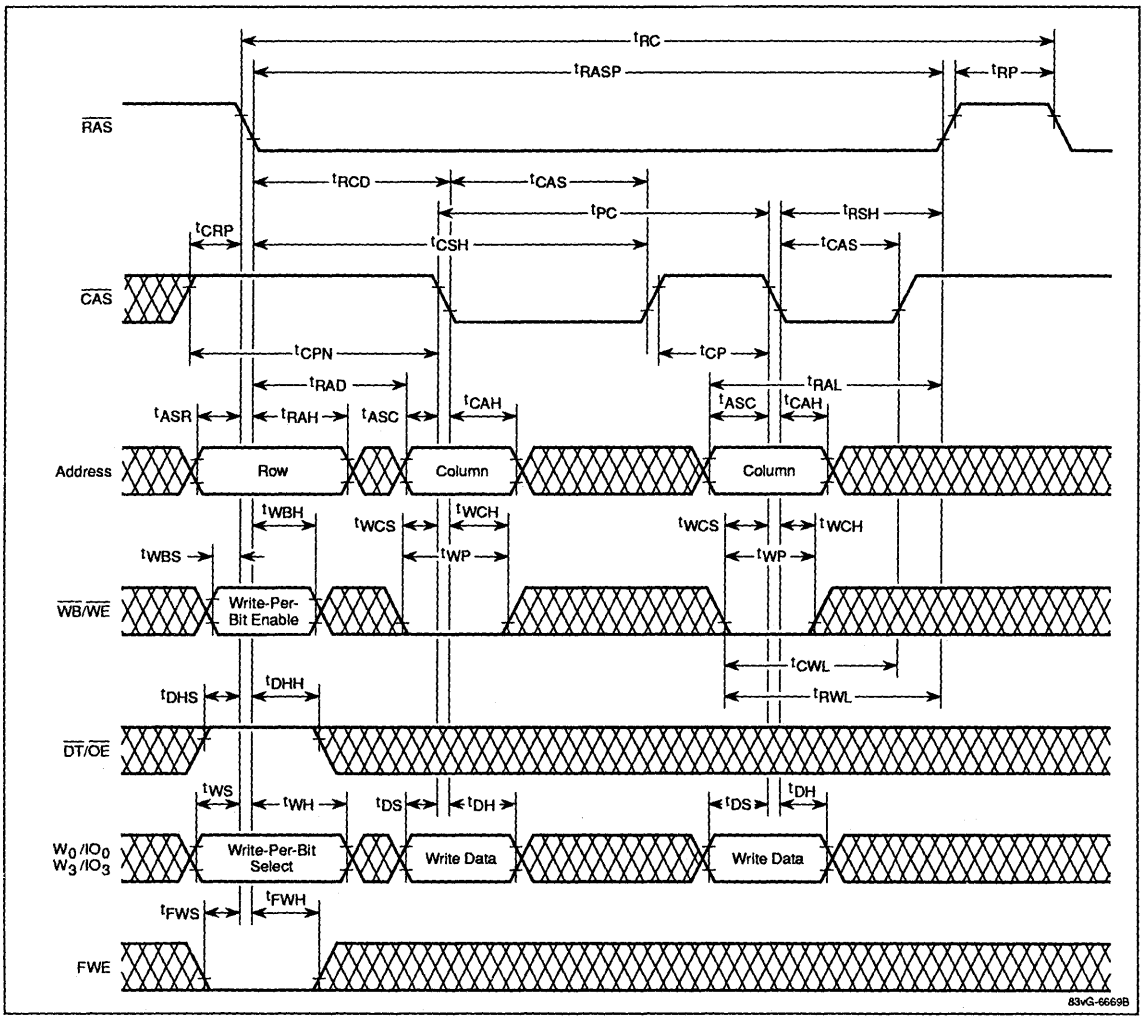
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Write Cycle



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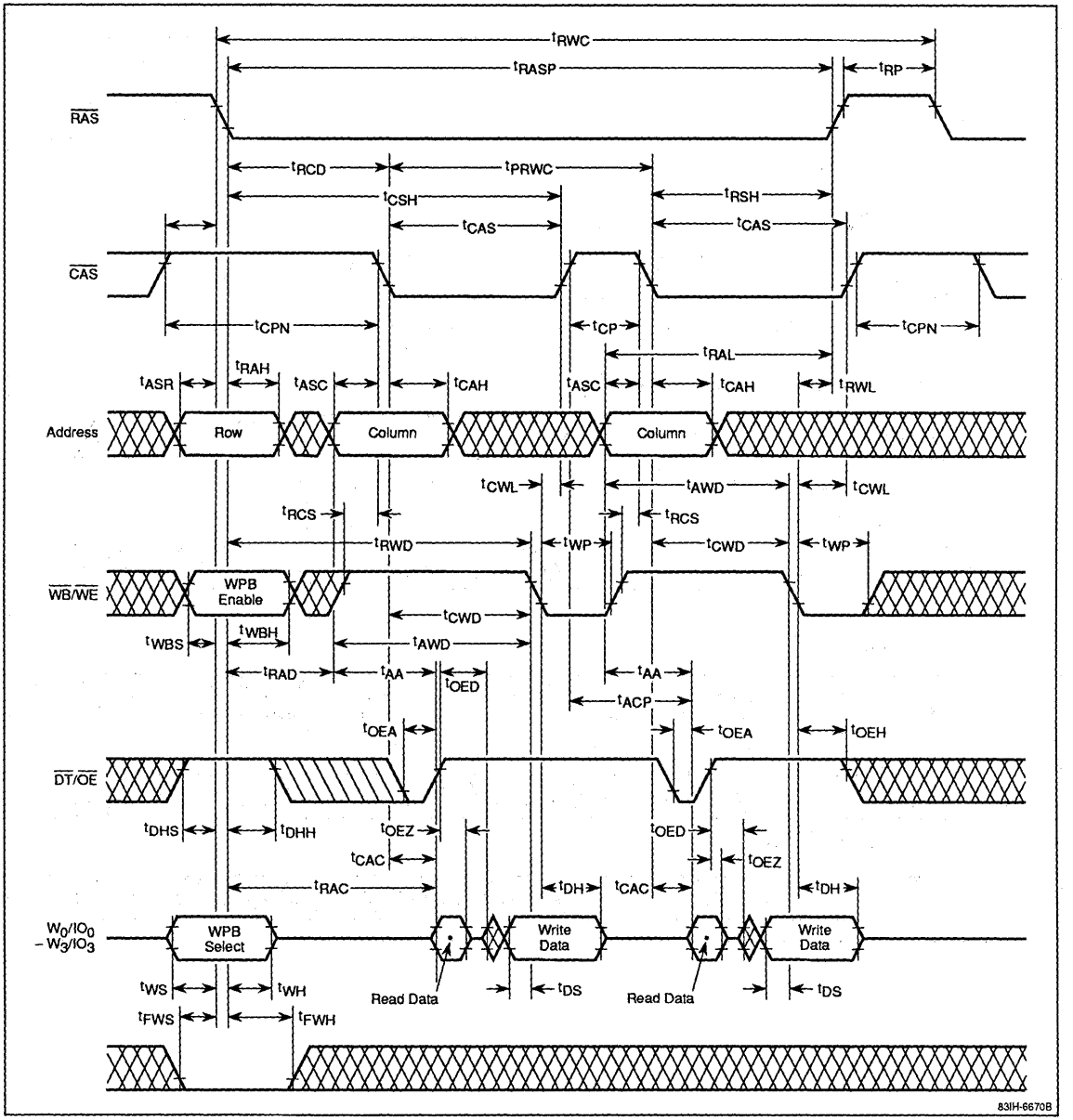
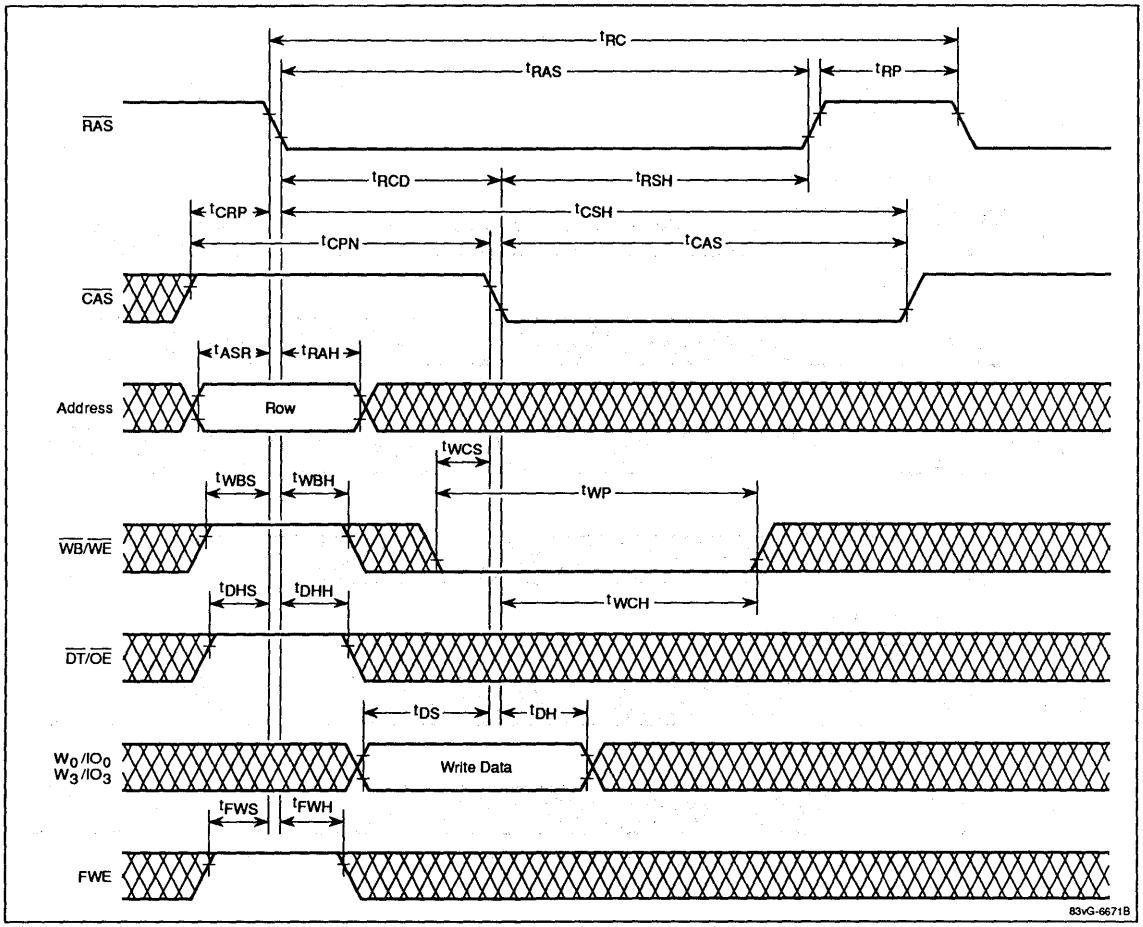
Timing Waveforms (cont)

Fast-Page Read-Modify-Write Cycle



Timing Waveforms (cont)

Color Register Set Cycle



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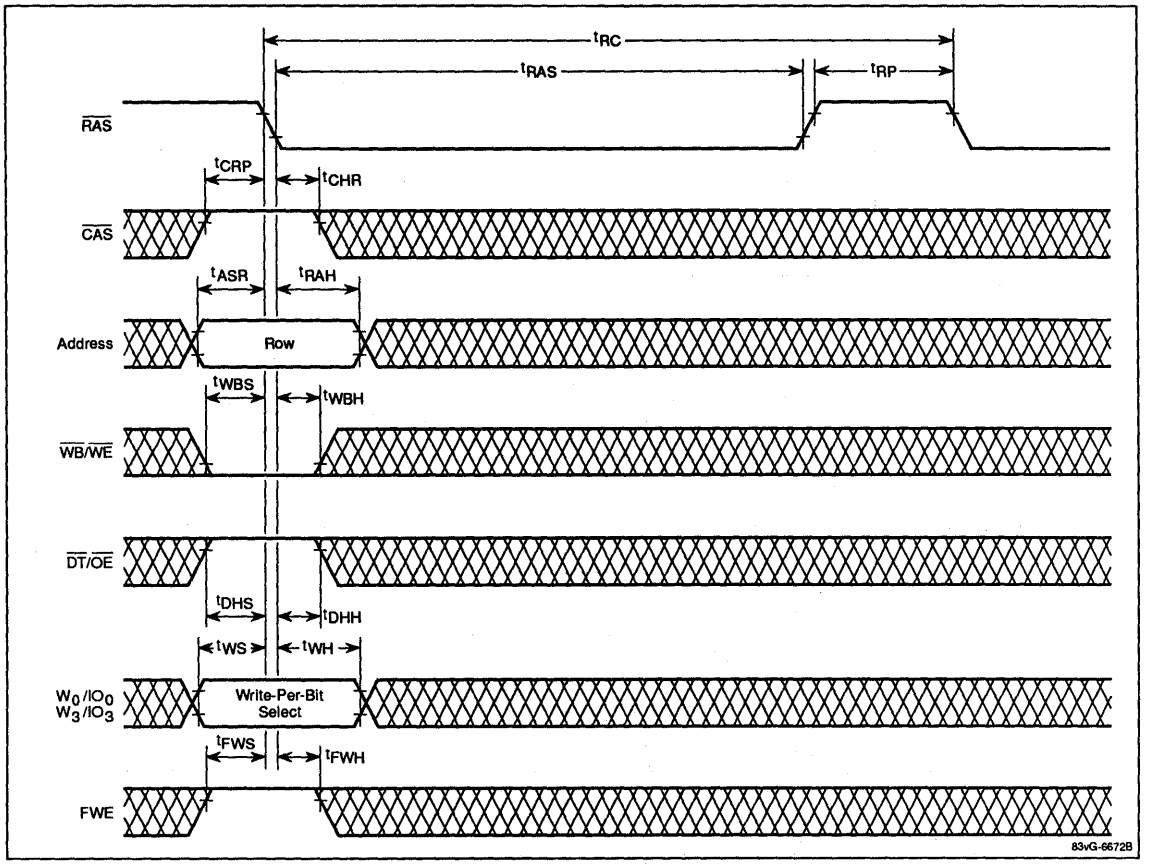
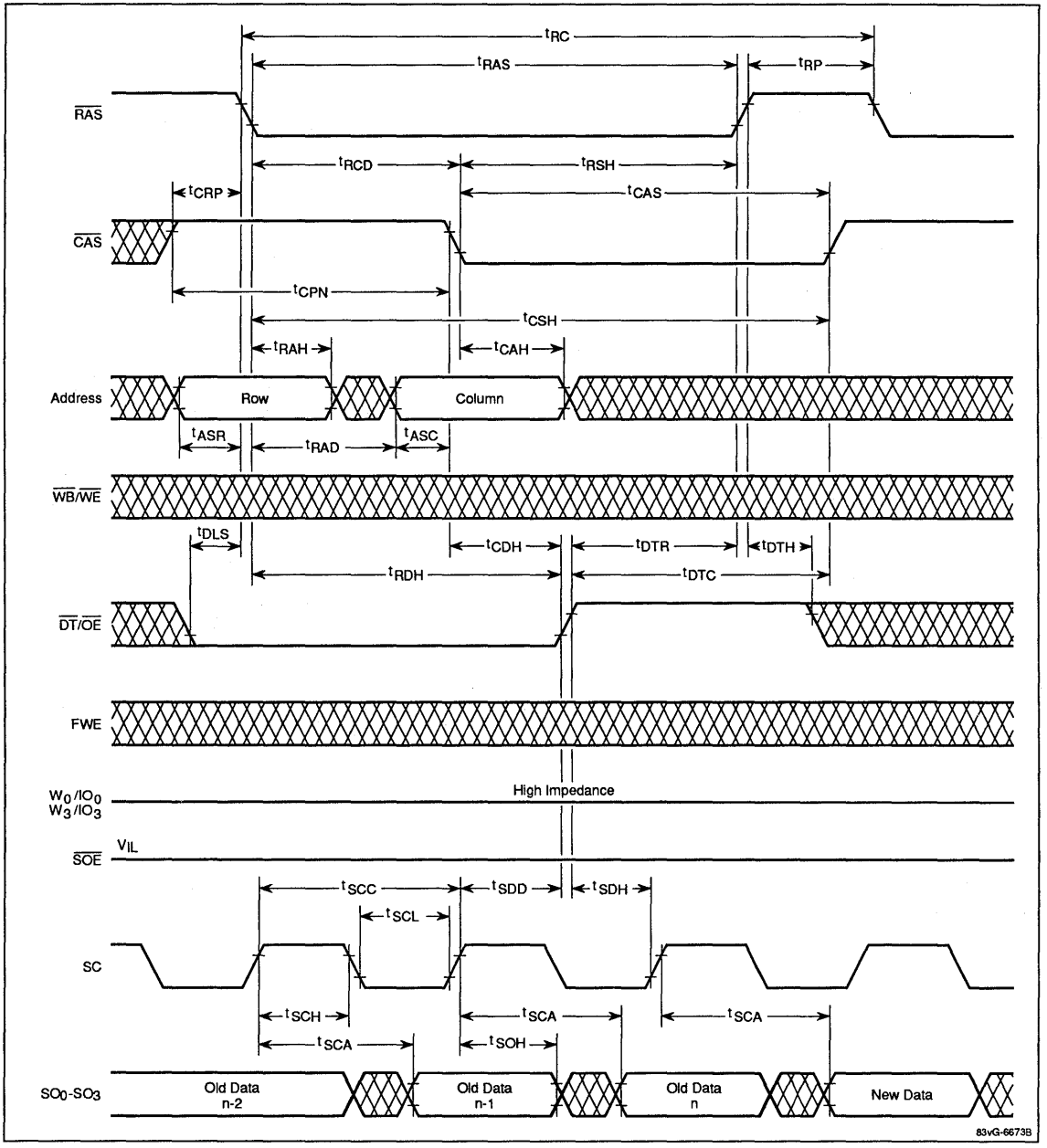
Timing Waveforms (cont)

Flash Write Cycle



Timing Waveforms (cont)

Data Transfer Cycle with Serial Port Active



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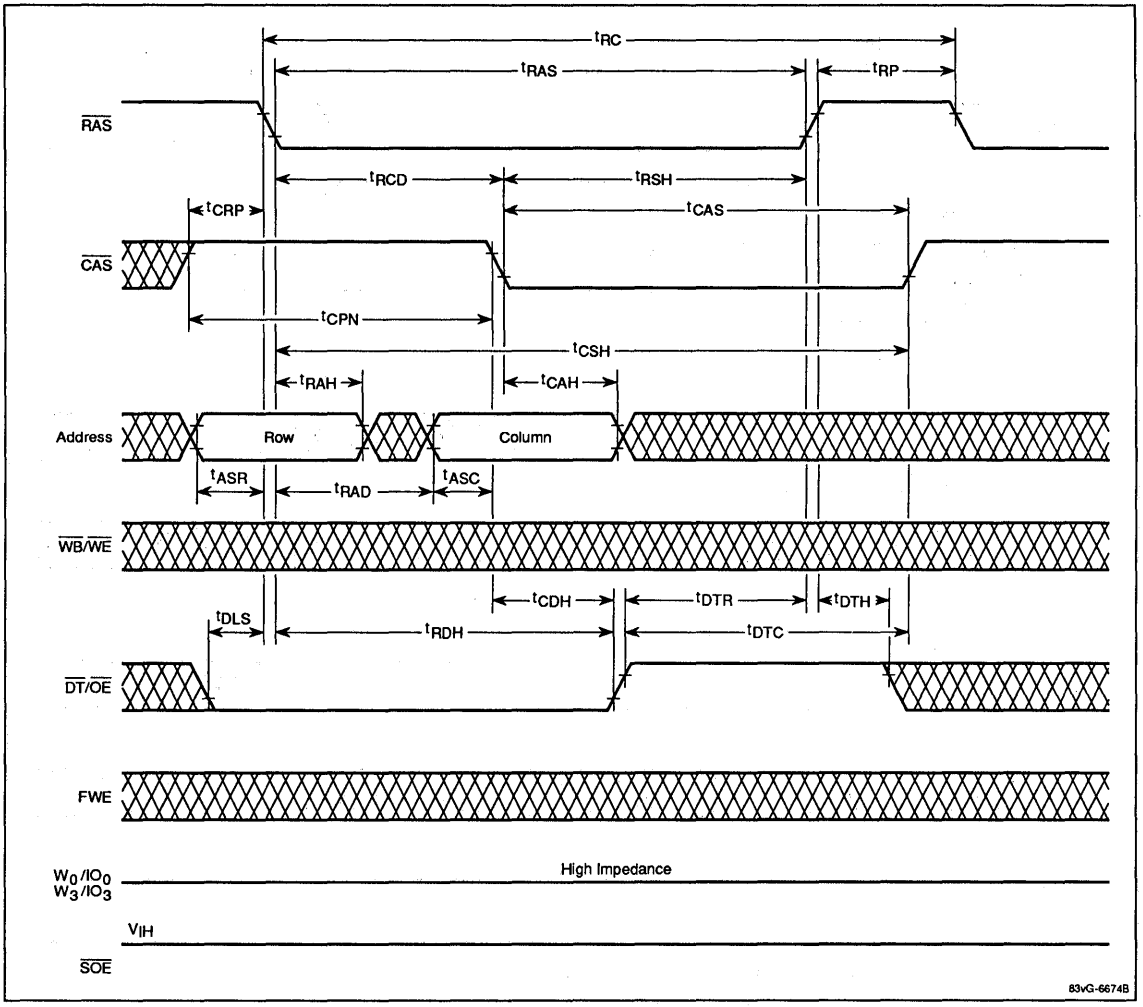
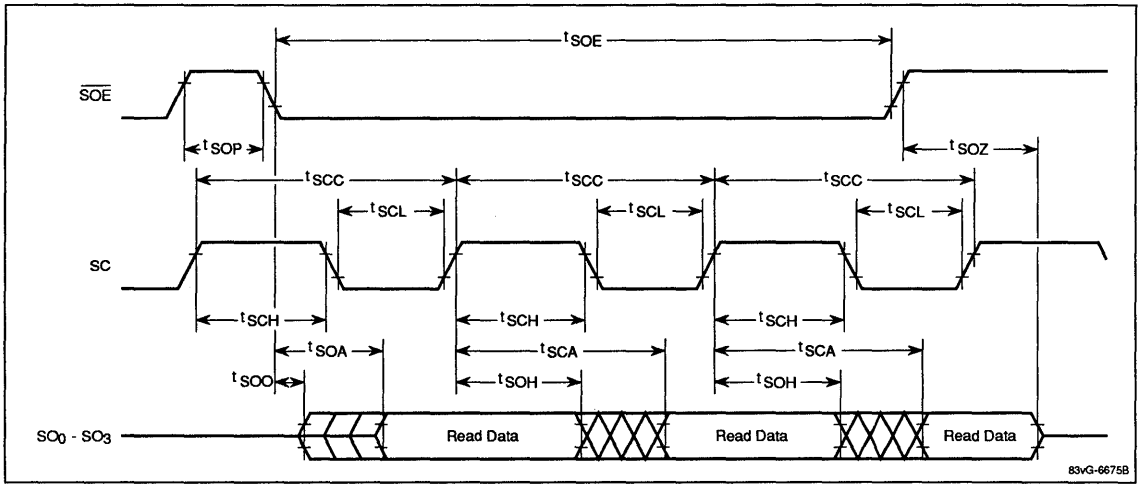
Timing Waveforms (cont)

Data Transfer Cycle with Serial Port in Standby



Timing Waveforms (cont)

Serial Read Cycle



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μPD42274-80
Dual-Port Graphics Buffer

Description

The μPD42274-80 is a dual-port graphics buffer equipped with a 256K x 4-bit random access port and a 512 x 4-bit serial read port. The serial read port is connected to an internal 2048-bit data register through a 512 x 4-bit serial read output circuit. The random access port is used by the host CPU to read or write data addressed in any desired order. A write-per-bit capability allows each of the four data bits to be individually selected or masked for a write cycle. Furthermore, a flash write option with write-per-bit control enables data in the color register to be written to a selected row in the random access port.

The μPD42274-80 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock; the serial read port continues to operate normally. Following the clock transition of a data transfer, serial output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

An advanced CMOS silicon-gate process using polycide technology and trench capacitors provides high storage cell density, high performance, and high reliability.

Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period. Automatic refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data input signals are latched on-chip to simplify system design. Data output is unlatched to allow greater system flexibility.

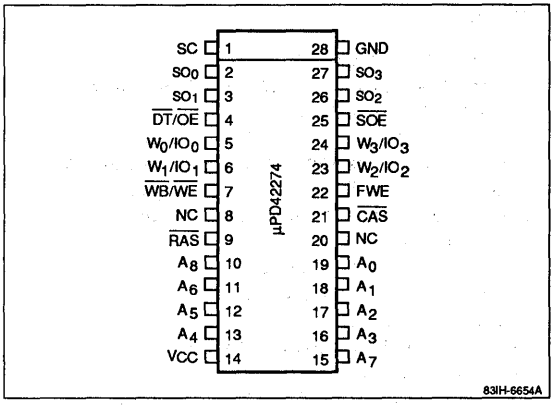
The μPD42274-80 is available in a 28-pin plastic ZIP or 28-pin plastic SOJ and is guaranteed for operation at 0 to + 70°C.

Features

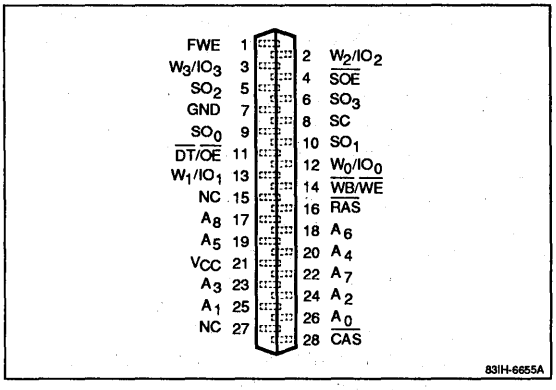
- Three functional blocks
  - 256K x 4-bit random access storage array
  - 2048-bit data register
  - 512 x 4-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- Single + 5-volt power supply
- On-chip substrate bias generator
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - 512 refresh cycles every 8 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page cycles
  - Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - $\overline{CAS}$-controlled hidden refreshing
  - Write-per-bit option regarding four I/O bits
  - Write bit selection multiplexed on IO_0-IO_3
- Flash write option with write-per-bit control
- $\overline{RAS}$-activated data transfer
  - Same cycle time as for random access
  - Row data transferred to data register as specified by row address inputs
  - Starting location of following serial read cycle specified by column address inputs
  - Transfer of 2048 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
- Serial data output on SO_0-SO_3
- Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- CMOS silicon-gate process with trench capacitors

Pin Configurations

28-Pin Plastic SOJ



28-Pin Plastic ZIP



Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42274LE-80	80 ns	25 ns	28-pin plastic SOJ
μPD42274V-80	80 ns	25 ns	28-pin plastic ZIP

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
W_0/IO_0 - W_3/IO_3	Write-per-bit selects/data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB/WE}$	Write-per-bit/write enable
$\overline{DT/OE}$	Data transfer/output enable
FWE	Flash write enable
SO_0 - SO_3	Serial read outputs
SC	Serial control
$\overline{SOE}$	Serial output enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage all pins relative to GND, V_R	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

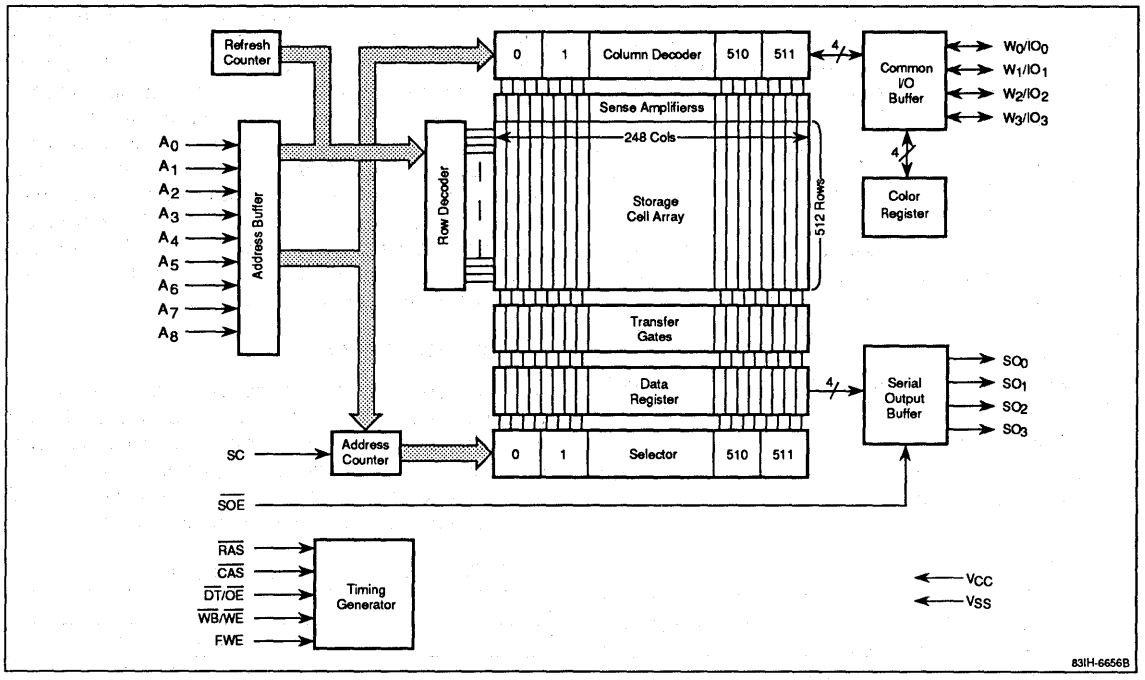
Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Limit (max)	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 through A_8
	$C_{I(\overline{DT/OE})}$	8	pF	$\overline{DT/OE}$
	$C_{I(\overline{WB/WE})}$	8	pF	$\overline{WB/WE}$
	$C_{I(FWE)}$	8	pF	FWE
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 through W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 through SO_3

Block Diagram



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Pin Descriptions

A_0-A_8 (Address Inputs). These pins are multiplexed as row and column address inputs. Each of four data bits in the random access port corresponds to 262,144 storage cells, which means that nine row addresses and nine column addresses are required to decode one cell location. Nine row addresses are first used to select one of the 512 possible rows for a read, write, data transfer, or refresh cycle. Nine column addresses are then used to select the one of 512 possible column decoders for a read or write cycle or the one of 512 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{RAS}$-only refresh or flash write cycles.)

W_0/IO_0-W_3/IO_3 (Write-Per-Bit Inputs/Common Data Inputs and Outputs). Each of the four data bits can be individually latched by these inputs at the falling edge of $\overline{RAS}$ in a write or flash write cycle, and then updated at the next falling edge of $\overline{RAS}$. In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$ or $\overline{WE}$.

$\overline{RAS}$ (Row Address Strobe). This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 2,048 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The nine row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{DT/OE}$ $\overline{WB/WE}$, and FWE are simultaneously latched to determine device operation.

$\overline{CAS}$ (Column Address Strobe). This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The nine column address bits are latched at the falling edge of $\overline{CAS}$.

$\overline{WB/WE}$ (Write-Per-Bit Control/Write Enable). At the falling edge of $\overline{RAS}$, the $\overline{WB/WE}$ and FWE inputs must be low and $\overline{CAS}$ and $\overline{DT/OE}$ high to enable the write-per-bit option. When $\overline{CAS}$, $\overline{DT/OE}$, and FWE are high at the falling edge of $\overline{RAS}$, the level of this signal indicates either a color register set cycle or flash write cycle. A high $\overline{WB/WE}$ can be used at the beginning of a standard write or read cycle.

$\overline{DT/OE}$ (Data Transfer/Output Enable). At the falling edge of $\overline{RAS}$, $\overline{CAS}$ high and FWE and $\overline{DT/OE}$ low initiate a data transfer, regardless of the level of $\overline{WB/WE}$. $\overline{DT/OE}$ high initiates conventional read or write cycles and controls the output buffer in the random access port.

FWE (Flash Write Enable). If this signal is low and $\overline{CAS}$ and $\overline{DT/OE}$ are high at the falling edge of $\overline{RAS}$, a read or write cycle is initiated. If FWE, $\overline{CAS}$ and $\overline{DT/OE}$ are high at the falling edge of $\overline{RAS}$, either a color register set cycle or flash write cycle is initiated, depending on the level of $\overline{WB/WE}$.

SO_0-SO_3 (Serial Data Output). Four-bit data is read from these pins. Data remains valid until the next SC signal is activated.

SC (Serial Control). Repeatedly activating this signal causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2,048 bits in the data register. The rising edge of SC activates serial read operation, in which four of the 2,048 data bits are transferred to four serial data buses, respectively, and read out. Whenever SC is low, the serial port is in standby.

$\overline{SOE}$ (Serial Output Enable). This signal controls the serial data output buffer.

OPERATION

The μPD42274-80 consists of a random access port and a serial read port. The random access port executes standard read and write cycles as well as data transfer and flash write cycles, all of which are based on conventional $\overline{RAS}/\overline{CAS}$ timing.

In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to its corresponding register location (unless the flash write option is used to write an entire row of data to predetermined values). The serial read port shows the contents of the data register in serial order. The random access and serial read ports can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is arranged in a 512-row by 2048-column matrix, whereby each of 4 data bits in the random access port corresponds to 262,144 storage cells and 18 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 through A_8 and latched onto the chip by $\overline{RAS}$. Nine column address bits then are set up on pins A_0 through A_8 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 2048 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through 1 of 512 column decoders, 4 storage cells on the row are connected to 4 data buses, respectively. In a data transfer, 9 row address bits are used to select 1 of the 512 possible rows involved in the transfer of data to the data register. Nine column address bits are then used to select the 1 of 512 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 4 data bits in the 2048-bit data register are transferred to 4 serial data buses and read out. Activating SC repeatedly causes serial read cycles (starting from the location specified in the data transfer) to be executed within the 2048 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, that must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time.

Truth Table for the Random Access Port

$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	FWE	Cycle
H	H	H	L	Read or write (Note 1)
H	H	L	L	Mask write (Note 2)
H	L	X	L	Read data transfer
H	L	H	H	
L	X	X	X	$\overline{CAS}$ before $\overline{RAS}$ refresh (Note 3)
H	H	H	H	Color register set (Note 4)
H	H	L	H	Flash write/write-per-bit (Note 5)

Notes:

(1) Initiates a normal read or write cycle and disables the write-per-bit capability.

(2) Enables the write-per-bit capability, where individual bits can be selected or masked for a write cycle. Four-bit masked data is latched at the falling edge of $\overline{RAS}$ and reset at its rising edge.

(3) Initiates a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. As $\overline{RAS}$ falls, $\overline{WB/WE}$ and $\overline{DT/OE}$ and FWE = don't care.

(4) Defines a color register set cycle, where data in the register can be accessed in a read or write cycle.

(5) Initiates a flash write cycle, where the storage cells on an entire selected row can be set with write-per-bit control to the same data stored in the color register. As $\overline{RAS}$ falls, $\overline{DT/OE}$ = don't care. To avoid unintended flash write operation, the FWE pin should be grounded. If grounding the FWE pin is not possible, use the non-flash write version of this part, the μPD42273.

(6) X = don't care.

To miminize the number of pins, some are multiplexed.

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

$\overline{OE}$, $\overline{WE}$ and IO_i affect standard operations, while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

The level of $\overline{DT}$ determines whether a cycle is a random access operation or data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_i defines data bits to be written with the write-per-bit option. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD42274-80 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 2048-bit register from the corresponding 2048-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 2048 transfer gates and transfer data from one of the rows to the register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining $(\overline{WB}/)\overline{WE}$ while $\overline{CAS}$ is active. The $(W_i/)IO_i$ pin (i = 0, 1, 2, 3) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to ±CAS delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance.

Write Cycle. A write cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low during the $\overline{RAS}/\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or $(\overline{WB}/)\overline{WE}$ strobes the data on $(W_i/)IO_i$ into the on-chip data latch. To make use of the write-per-bit option, $\overline{WB}(/\overline{WE})$ must be low as $\overline{RAS}$ falls. In this case, write data bits can be specified by keeping $W_i(/IO_i)$ high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

For those data bits of $W_i(/IO_i)$ that are kept low as $\overline{RAS}$ falls, write operation is inhibited on the chip. If $\overline{WB}(/\overline{WE})$ is high as $\overline{RAS}$ falls, the write-per-bit option is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low before $\overline{CAS}$ falls. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, $(\overline{DT}/)\overline{OE}$ must meet the setup and hold times of $\overline{DT}$ high, but otherwise $(\overline{DT}/)\overline{OE}$ does not affect any circuit operation while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. This cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. $(W_i/)IO_i$ shows read data at access time. Afterward, in preparation for the upcoming write cycle, $(W_i/)IO_i$ returns to high impedance when $(\overline{DT}/)\overline{OE}$ goes high. The data to be written is strobed by $(\overline{WB}/)\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of $(\overline{DT}/)\overline{OE}$, which can be activated just after $(\overline{WB}/)\overline{WE}$ falls, even when $(\overline{WB}/)\overline{WE}$ is brought low after $\overline{CAS}$.

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Refresh Cycle. A cycle at each of the 512 row addresses (A_0 through A_8) will refresh all storage cells. Any cycle executed in the random access port (i.e., read, write, refresh, data transfer, color register set, or flash write) refreshes the 2048 bits selected by the $\overline{RAS}$ addresses or by the on-chip refresh address counter.

$\overline{RAS}$-Only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes all cells in one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep $(W_i/)IO_i$ in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This cycle is executed after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed

(except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed causes data to be transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. In fast-page operation, read, write and read-write/read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the next fast-page write cycle.

During a fast-page read cycle, the $(W_i)IO_i$ data pin (i = 0, 1, 2, or 3) remains in a state of high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be one of the following calculated intervals:

Fast-Page Access Time

Calculated Interval	Conditions
t_{ACP}	$t_{ASC} \geq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
t_{AA}	$t_{ASC} \leq t_{ASC}$ (max) and $t_{CP} \geq t_{CP}$ (max)
	$t_{ASC} \leq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
t_{CAC}	$t_{ASC} \geq t_{ASC}$ (max) and $t_{CP} \leq t_{CP}$ (max)

Data Transfer Cycle. A data transfer is executed by bringing $\overline{DT}(/\overline{OE})$ and FWE low as $\overline{RAS}$ falls. The specified 1 of the possible 512 rows involved in the data transfer, as well as the starting location of the following serial read cycle in the serial read port, are defined by address inputs. $\overline{DT}(/\overline{OE})$ must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$, so that the data transfer condition may be satisfied. The low-to-high transition of $\overline{DT}$ causes two operations through the data transfer gates: column address buffer outputs are transferred to the serial address counters, and storage cell data amplified on digit lines is transferred to the data register. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the data in the random access port.

Color Register Set Cycle. A color register set cycle is executed in the same fashion as a conventional read or write cycle, with the level of $\overline{WE}$ high as $\overline{RAS}$ falls. In this cycle, read or write operation is available to the color-register under the control of $\overline{WE}$. In read operation, color register data is read out on the common IO_i pins. In write operation, common IO_i data can be written into the color register. $\overline{RAS}$-only refreshing is internally performed on the row selected by A_0 through A_8 in this cycle.

Flash Write Cycle. A flash write cycle can clear or set each of the four 512-bit data sets on the one row selected from among the 512 possible rows according to data stored in the color register. Bit mask inputs are latched as $\overline{RAS}$ falls. This cycle is useful in graphics processing applications when the screen should be cleared or set to some uniform value as quickly as possible.

Serial Read Port

The serial read port is only used to serially read the contents of the data register starting from a specified location. The entire operation, therefore, follows the data transfer cycle. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}(/\overline{OE})$ must occur within a specified period in an SC cycle. Except for this cycle, the serial read port can operate asynchronously . The output data appears at SO_i after an access time of t_{SCA}, measured from SC high, only when $\overline{SOE}$ is maintained low. The SC cycle which includes the positive transition of $\overline{DT}(/\overline{OE})$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD42274-80 graphics buffers into the same external circuitry. When $\overline{SOE}$ is at a low logic level, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is at high logic level, SO_i is disabled and in a state of high impedance.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 V to V_{CC}
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −2 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −1 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 2.1 mA

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Port Operation					
Random Access	Serial Read	Parameter	Max	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	100	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; FWE low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Standby	Standby	I_{CC2}	4	mA	$\overline{CAS}$ = $\overline{RAS}$ = V_{IH}; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	100	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; FWE low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 2)
Fast-page cycle	Standby	I_{CC4}	75	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	100	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Data transfer cycle	Standby	I_{CC6}	125	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Read/write cycle	Active	I_{CC7}	135	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; FWE low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Standby	Active	I_{CC8}	35	mA	$\overline{CAS}$ = $\overline{RAS}$ = V_{IH}; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	135	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; FWE low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Fast-page cycle	Active	I_{CC10}	110	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	135	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Data transfer cycle	Active	I_{CC12}	160	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Color register set cycle	Standby	I_{CC13}	80	mA	FWE and $\overline{WB}/\overline{WE}$ high as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Flash write cycle	Standby	I_{CC14}	80	mA	FWE high and $\overline{WB}/\overline{WE}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Color register set cycle	Active	I_{CC15}	115	mA	FWE and $\overline{WB}/\overline{WE}$ high as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Flash write cycle	Active	I_{CC16}	115	mA	FWE high and $\overline{WB}/\overline{WE}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, I_{CC6}, and I_{CC14}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked, but is kept at a stable high level. Column addresses are also assumed to be at a stable high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Switching Characteristics					
Access time from $\overline{RAS}$	t_{RAC}		80	ns	(Notes 3, 4 and 12)
Access time from falling edge of $\overline{CAS}$	t_{CAC}		20	ns	(Notes 3, 4, 13, 14 and 15)
Access time from column address	t_{AA}		45	ns	(Notes 3, 4, 14 and 15)
Access time from rising edge of $\overline{CAS}$	t_{ACP}		45	ns	(Notes 3 and 4)
Access time from $\overline{OE}$	t_{OEA}		20	ns	(Notes 3 and 4)
Serial output access time from SC	t_{SCA}		25	ns	(Note 3)
Serial output access time from $\overline{SOE}$	t_{SOA}		20	ns	(Note 3)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	20	ns	(Note 5)
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	20	ns	(Note 5)
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	10	ns	(Note 5)
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		ns	
Serial output hold time after SC high	t_{SOH}	5		ns	
Timing Requirements					
Random read or write cycle time	t_{RC}	160		ns	(Note 11)
Read-write/read-modify-write cycle time	t_{RWC}	215		ns	(Note 11)
Fast-page cycle time	t_{PC}	50		ns	(Note 11)
Fast-page read-write/read-modify-write cycle time	t_{PRWC}	105		ns	(Note 11)
Rise and fall transition time	t_T	3	50	ns	(Notes 3 and 10)
$\overline{RAS}$ precharge time	t_{RP}	70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	10		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	20	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}	22	60	ns	(Note 4)
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		ns	(Note 16)
Row address setup time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	12		ns	
Column address setup time	t_{ASC}	0	20	ns	(Note 15)
Column address hold time	t_{CAH}	15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	ns	(Notes 9 and 14)
Column address to $\overline{RAS}$ lead time	t_{RAL}	45		ns	
Read command setup time	t_{RCS}	0		ns	
Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns	(Note 6)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns	(Note 6)
Write command setup time	t_{WCS}	0		ns	(Note 7)

AC Characteristics (cont)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Timing Requirements (cont)					
Write command hold time	t_{WCH}	15		ns	
Write command pulse width	t_{WP}	15		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25		ns	
Data-in setup time	t_{DS}	0		ns	(Note 8)
Data-in hold time	t_{DH}	15		ns	(Note 8)
Column address to $\overline{WE}$ delay	t_{AWD}	70		ns	(Note 7)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	45		ns	(Note 7)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		ns	(Note 7)
$\overline{OE}$ high to data-in setup delay	t_{OED}	25		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	20		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	0		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	12		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		ns	
Refresh interval	t_{REF}		8	ms	Addresses A_0 through A_8
$\overline{DT}$ low setup time	t_{DLS}	0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low (serial port in standby)	t_{RDH}	70		ns	
$\overline{DT}$ hold time after $\overline{RAS}$ low (serial port active)	t_{RDHS}	25		ns	
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	25		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	7		ns	
	t_{SDDR}	12		ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	7		ns	
	t_{SDHR}	12		ns	
SC high to $\overline{CAS}$ low delay	t_{SSC}	10		ns	
Serial clock cycle time	t_{SCC}	25		ns	(Note 11)
SC pulse width	t_{SCH}	7		ns	
SC precharge time	t_{SCL}	7		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		ns	
$\overline{DT}$ high hold time	t_{DHH}	12		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	0		ns	
$\overline{DT}$ high pulse width	t_{DTP}	10		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		ns	
Write-per-bit setup time	t_{WBS}	0		ns	
Write-per-bit hold time	t_{WBH}	12		ns	
Flash write enable setup time	t_{FWS}	0		ns	
Flash write enable hold time	t_{FWH}	12		ns	
Write bit selection setup time	t_{WS}	0		ns	
Write bit selection hold time	t_{WH}	12		ns	
$\overline{SOE}$ pulse width	t_{SOE}	7		ns	

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AC Characteristics (cont)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Timing Requirements (cont)					
$\overline{SOE}$ precharge time	t_{SOP}	7		ns	
$\overline{CAS}$ low to SC high delay	t_{CSD}	35		ns	
$\overline{RAS}$ low to SC high delay	t_{RSD}	80		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles and four data transfer (DT) cycles, before proper device operation is achieved.

(3) See input/output timing waveforms for timing reference voltages. See figures 3 and 4 for output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}, t_{OEA}, or t_{AA}.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(7) t_{WCS}, t_{AWD}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{AWD} \geq t_{AWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of (WB/)WE in delayed write or read-modify-write cycles.

(9) Assumes that t_{RAD} (min) = t_{RAH} (min) + typical t_T of 5 ns.

(10) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(11) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(12) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(13) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(14) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(15) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(16) The t_{CRP} requirement is applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(17) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(18) Ac measurements assume t_T = 5 ns.

Figure 1. Input Timing

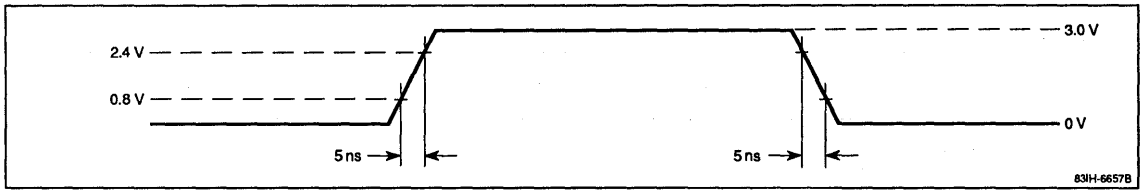

Figure 2. Output Timing

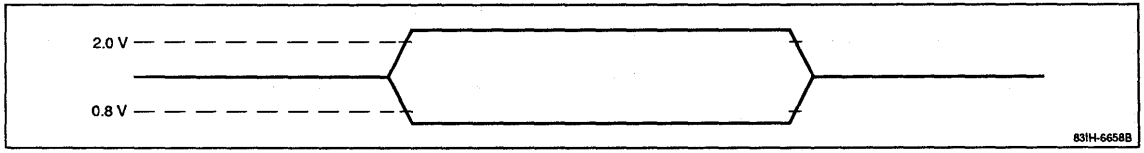

Figure 3. Output Load in Random Access Port

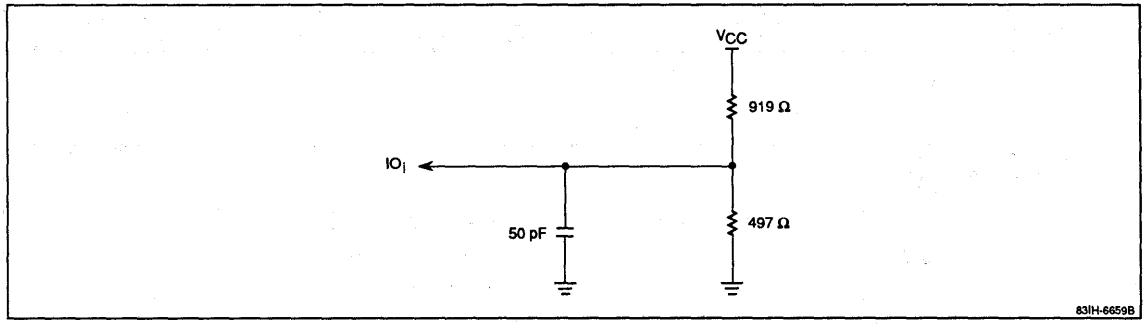

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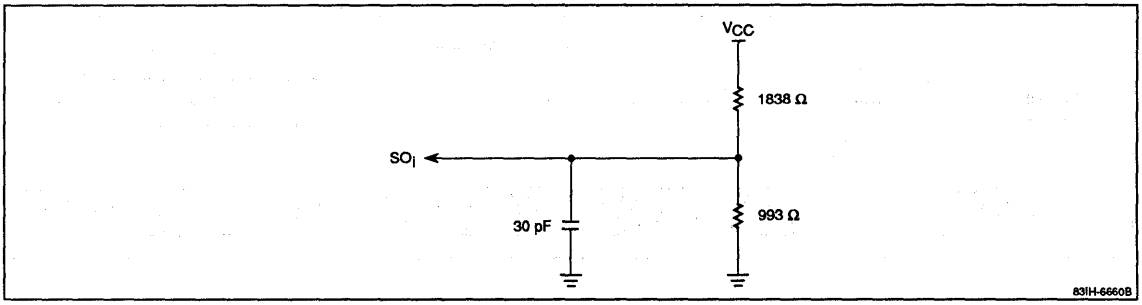
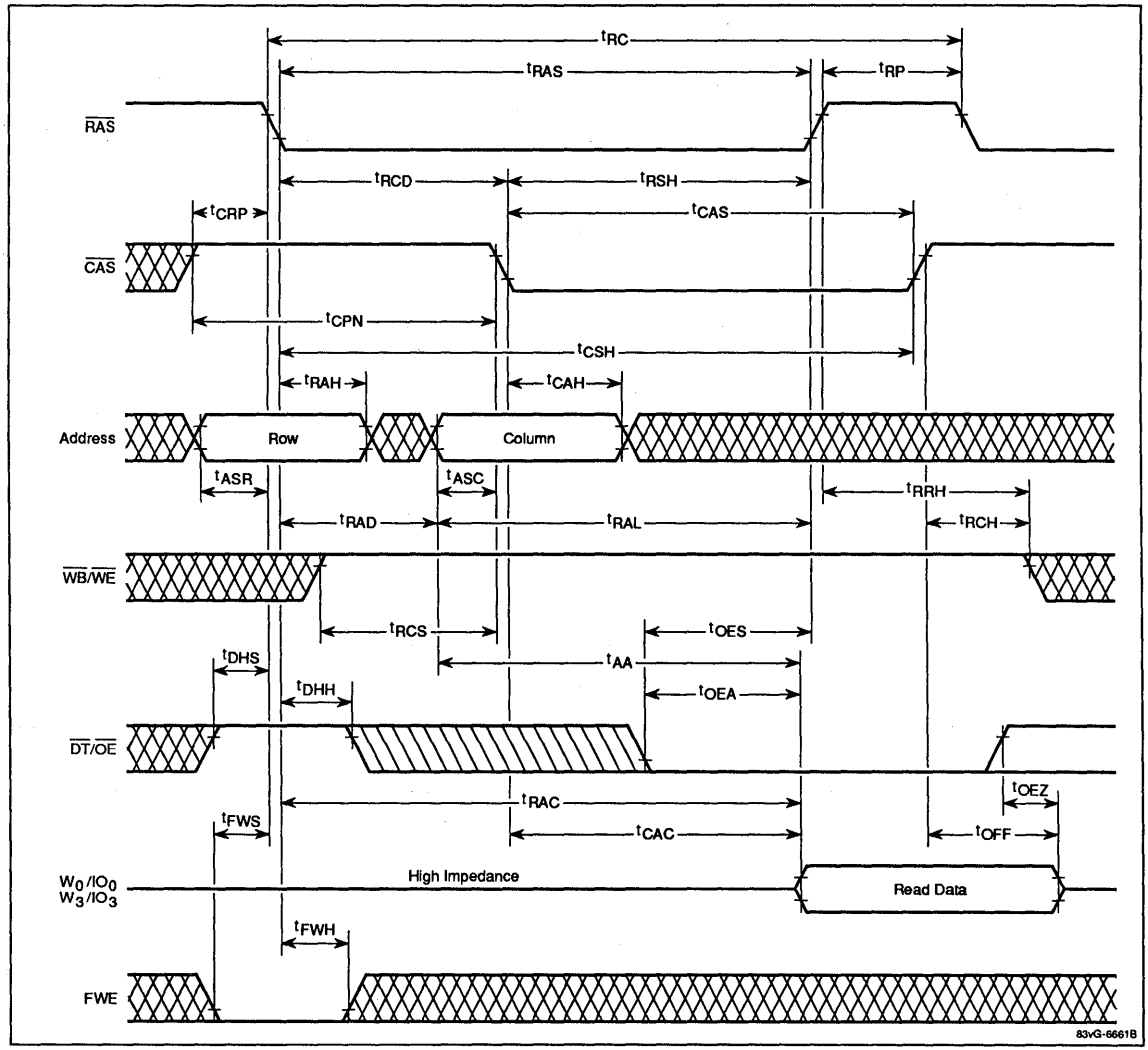
Figure 4. Output Load in Serial Read Port



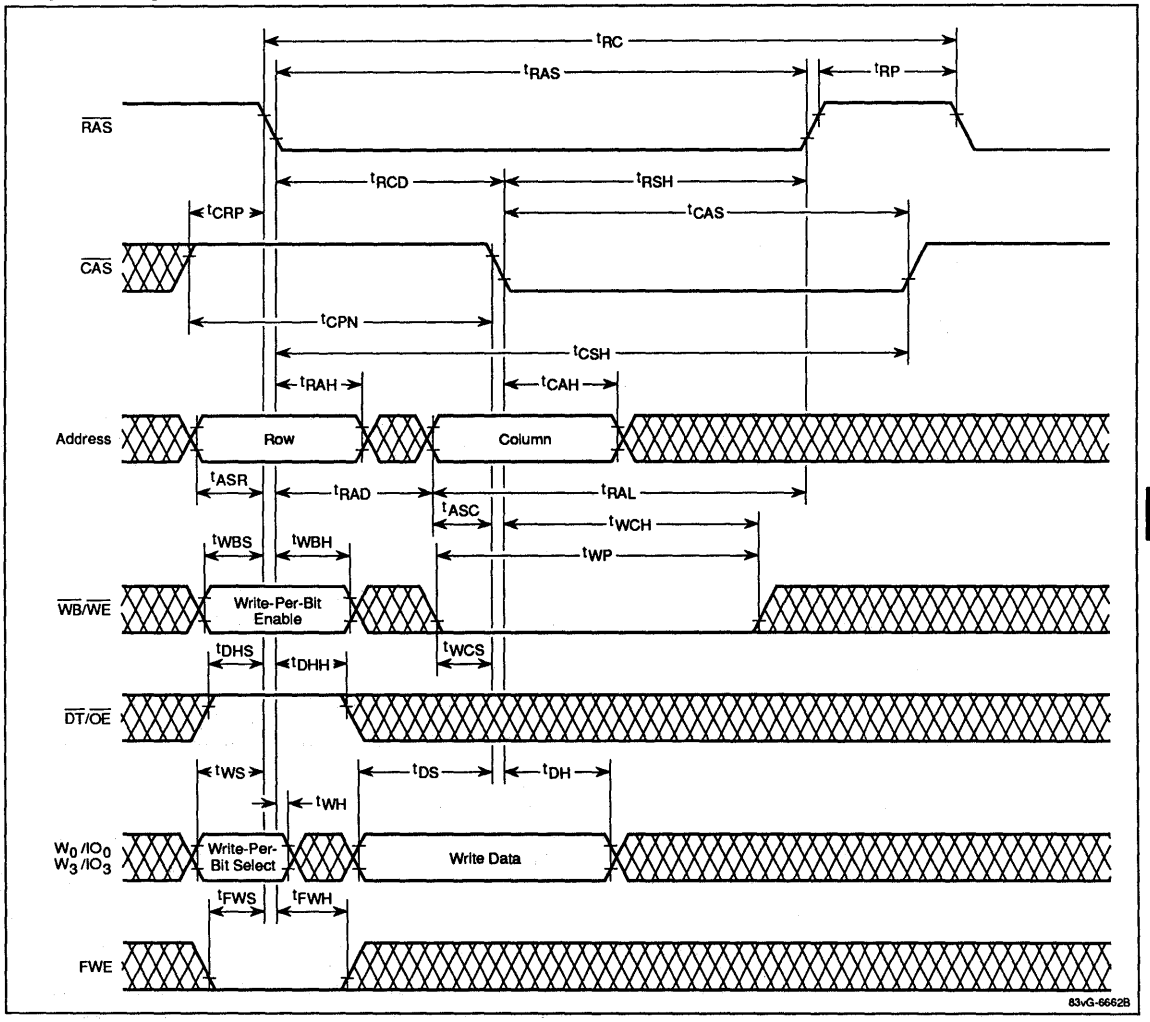
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



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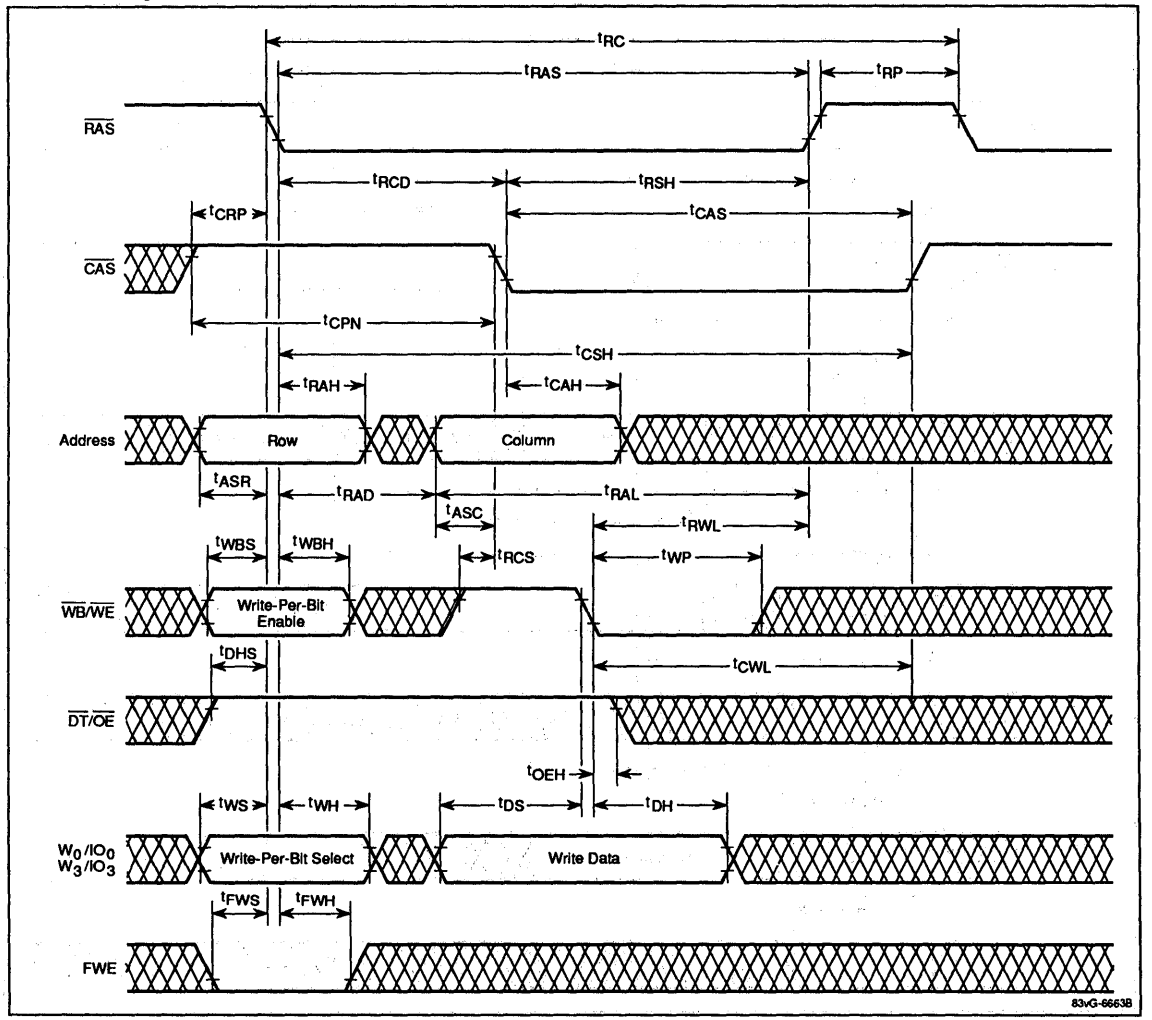
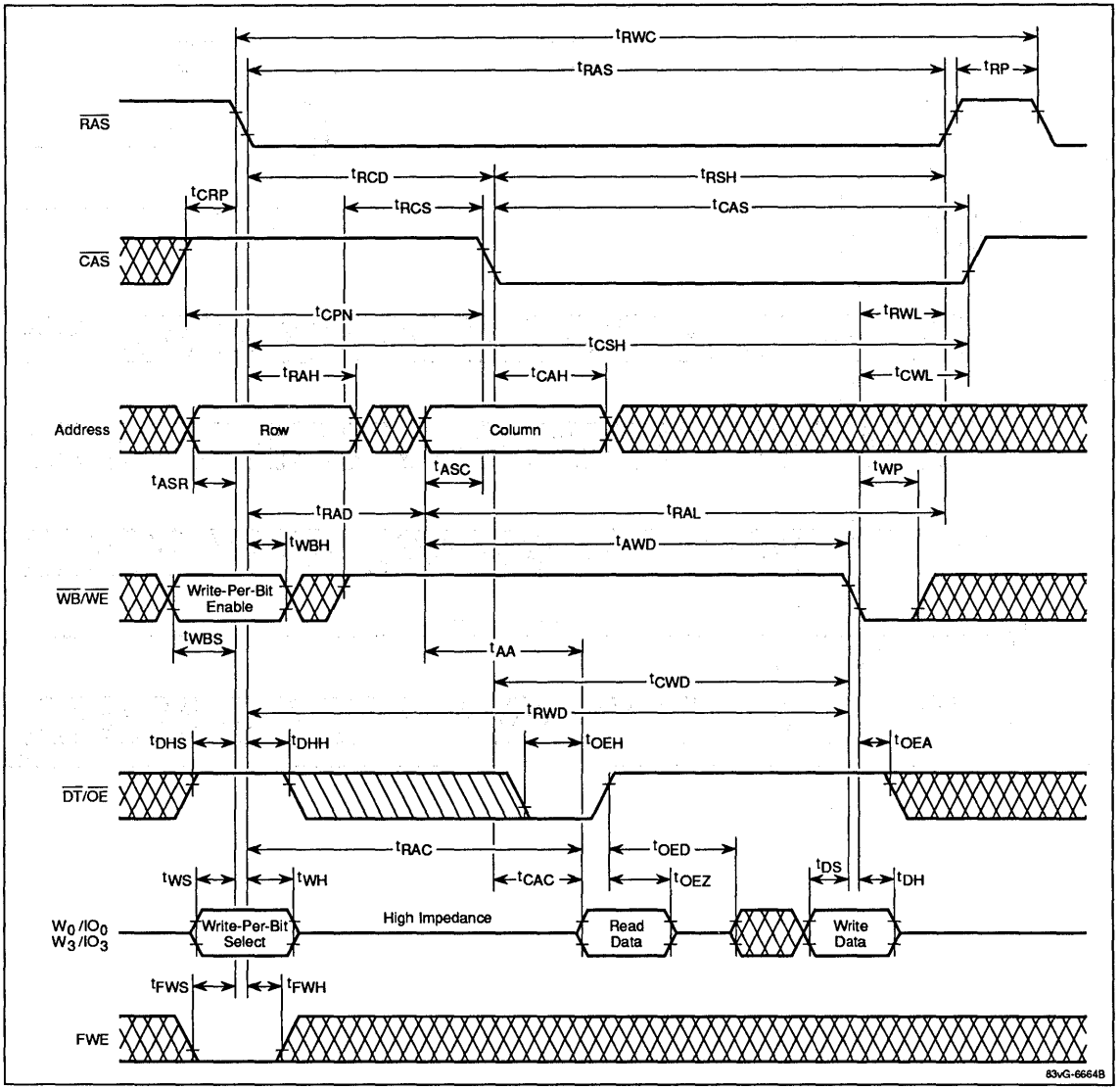
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



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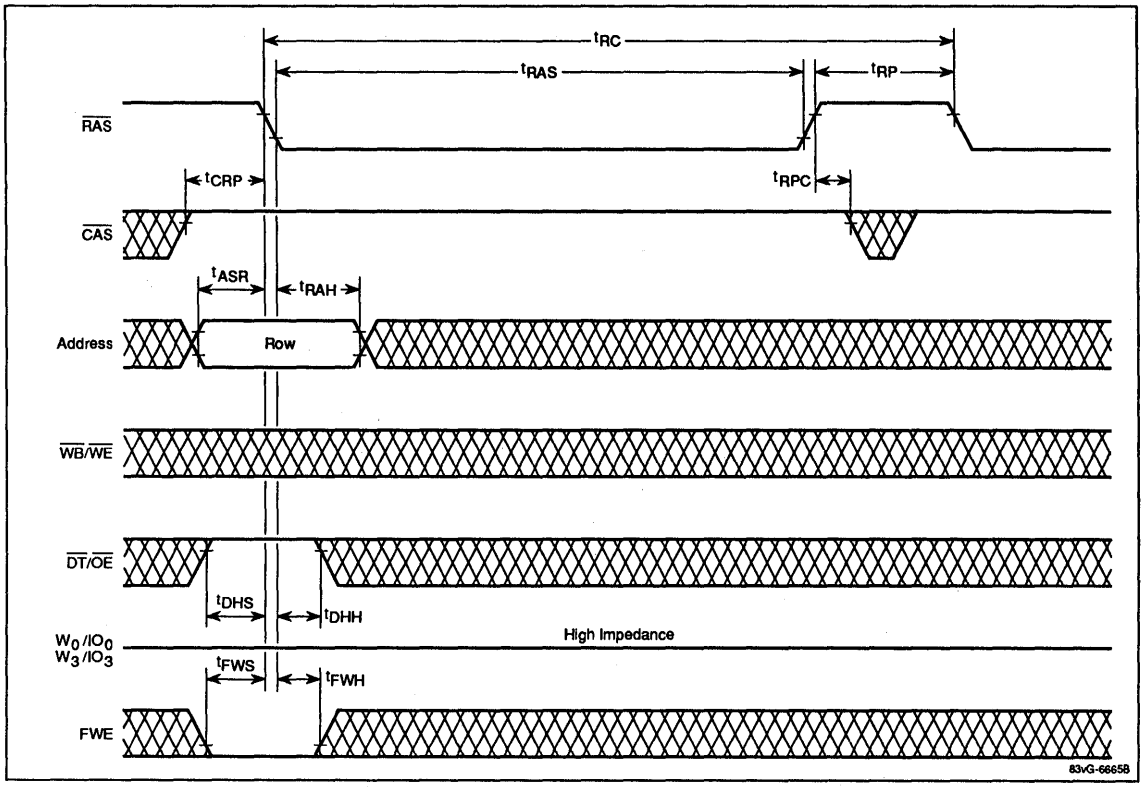
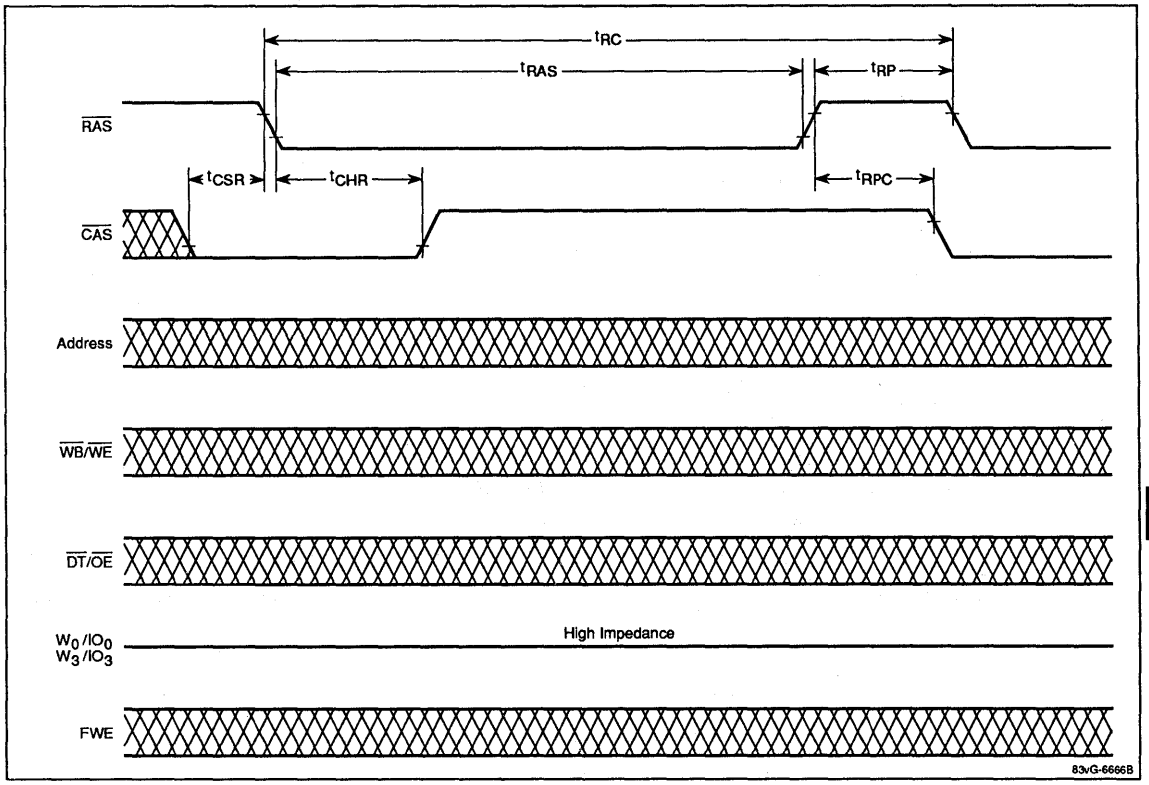
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



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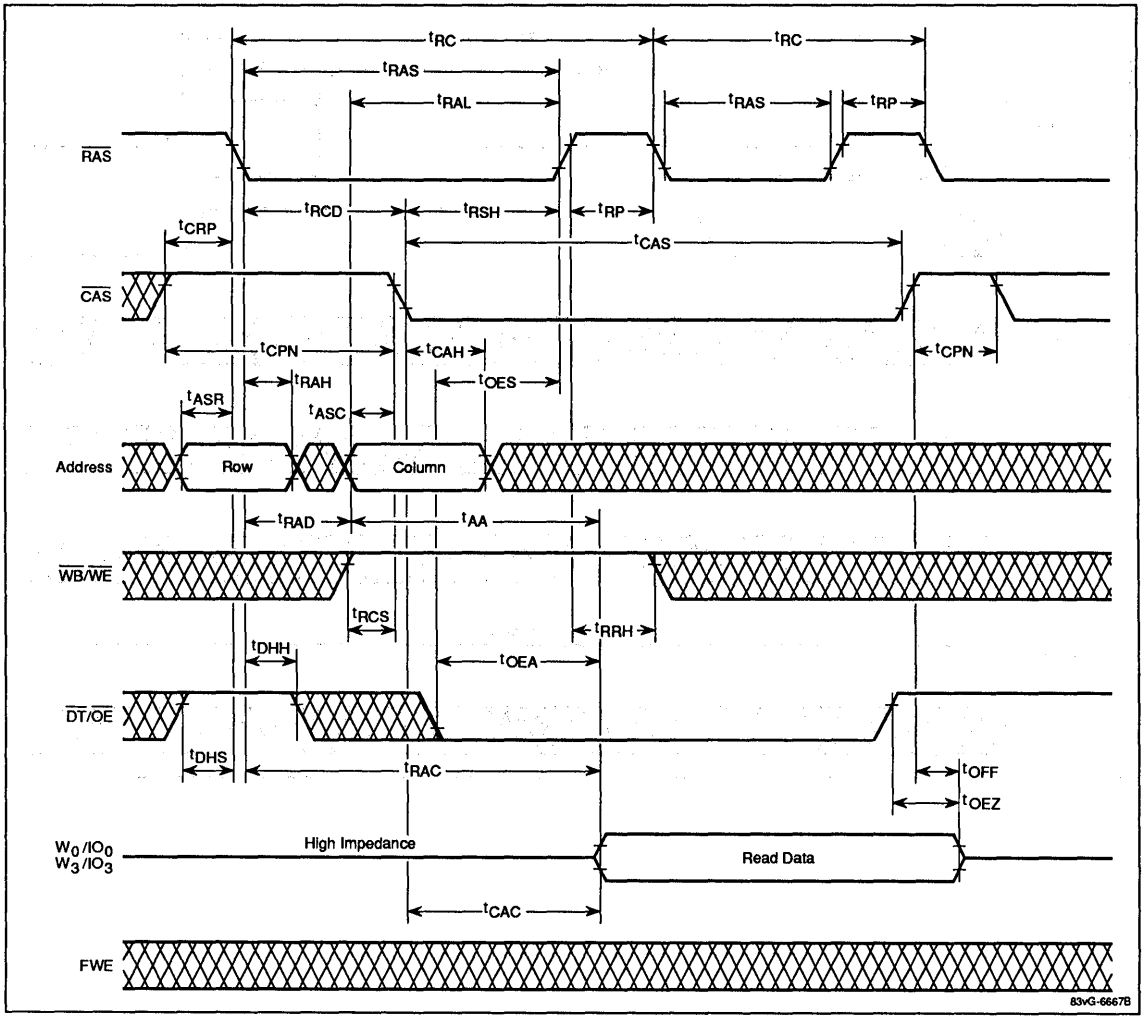
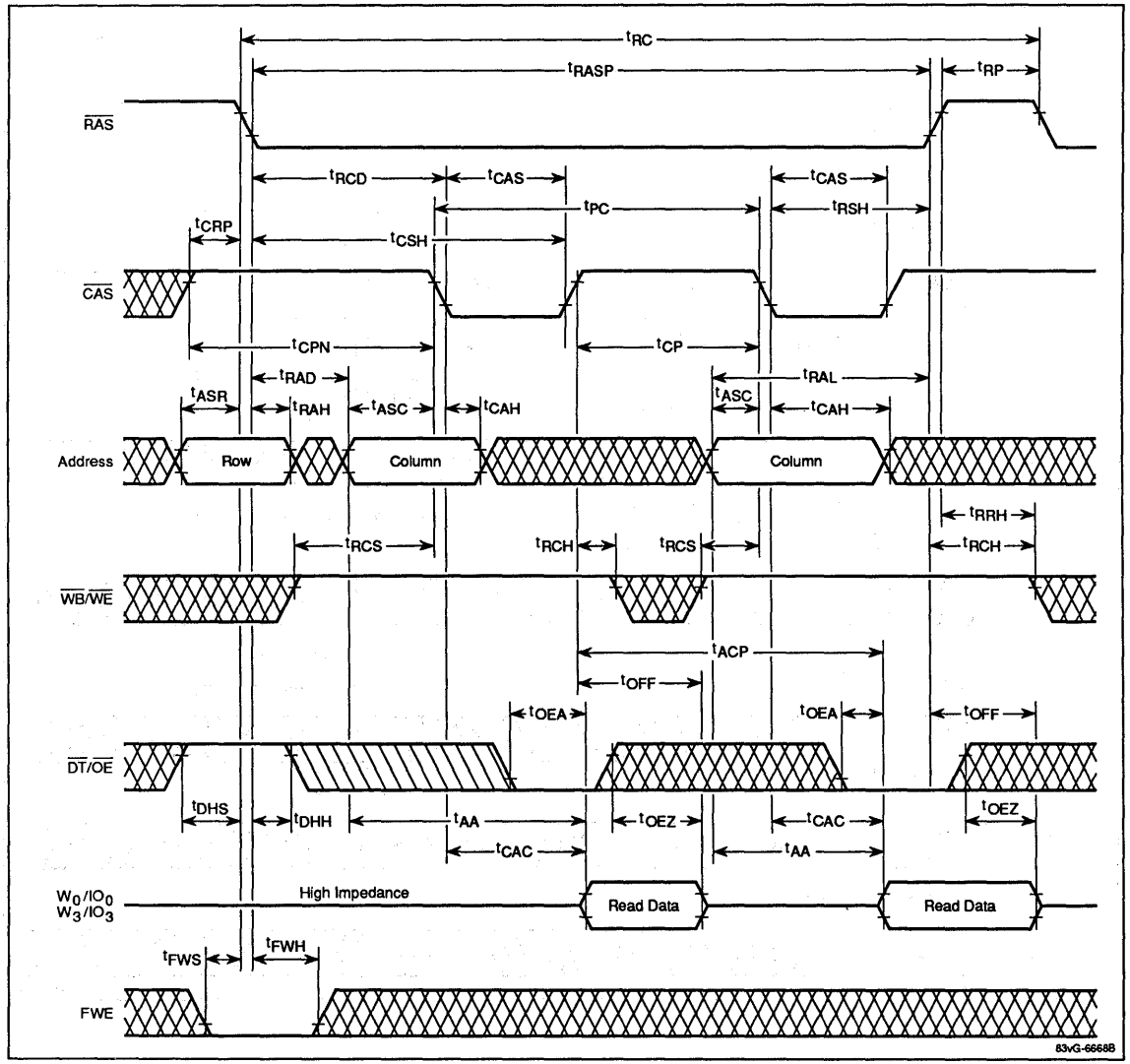
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

Fast-Page Read Cycle



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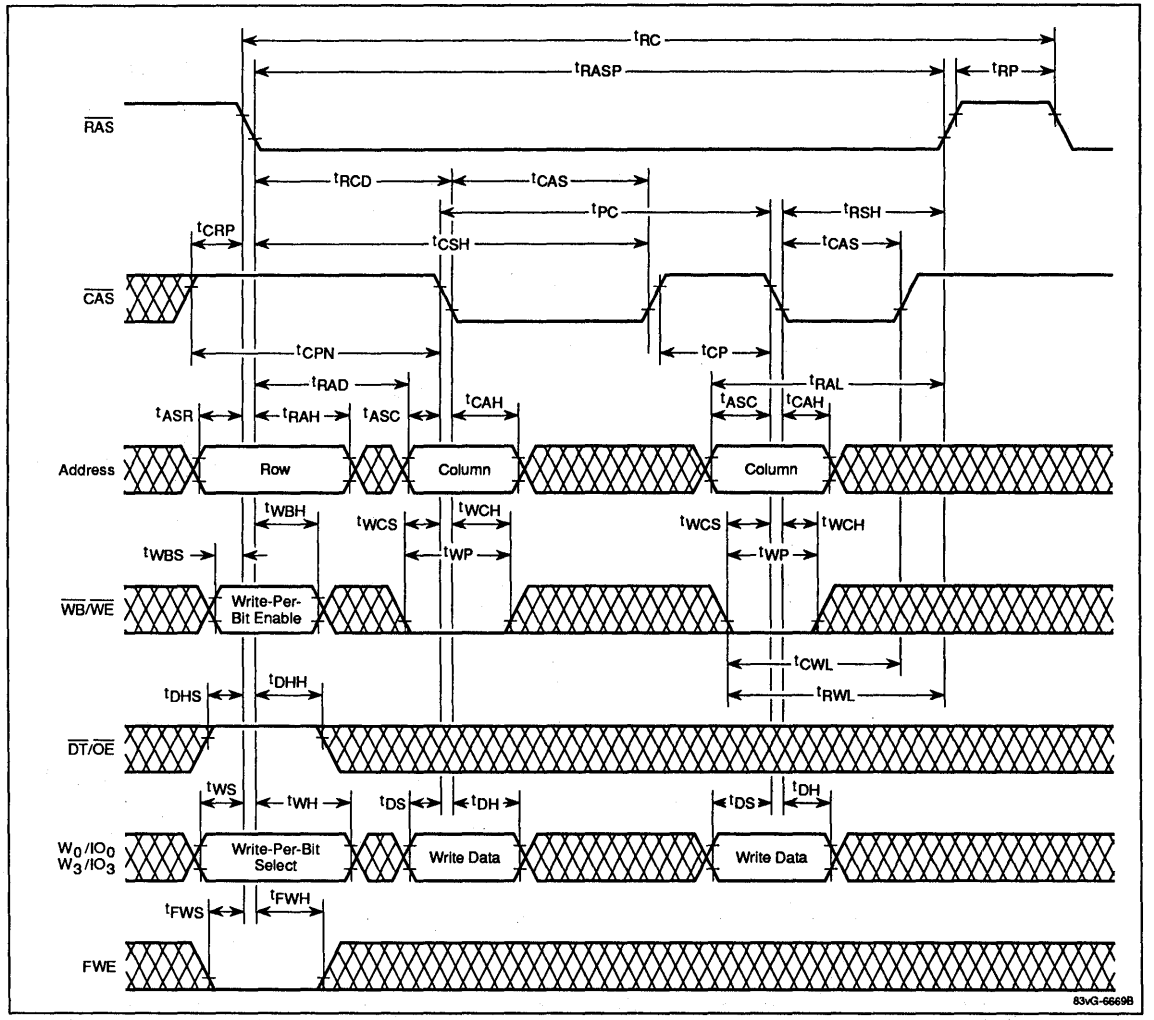
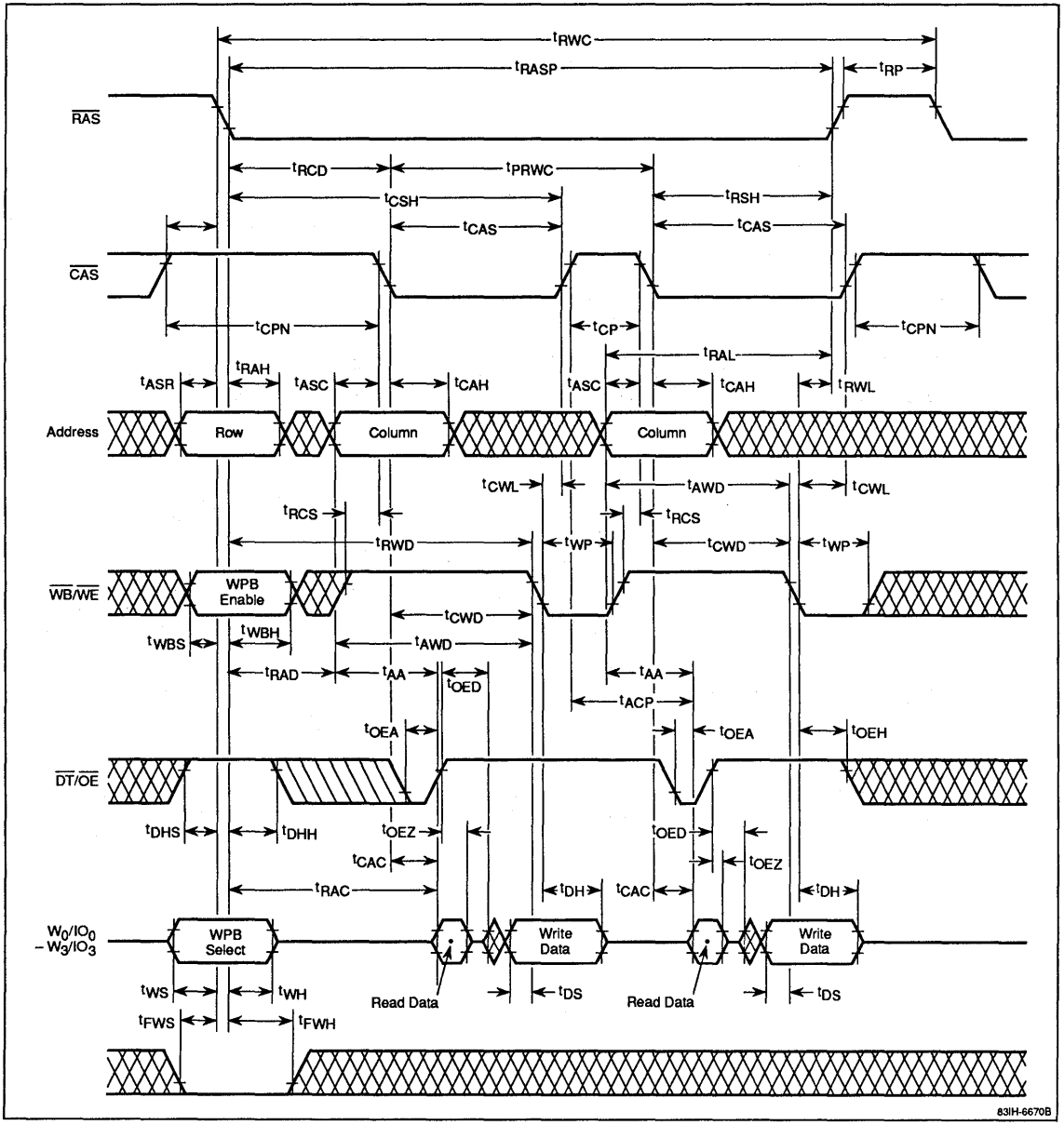
Timing Waveforms (cont)

Fast-Page Write Cycle



Timing Waveforms (cont)

Fast-Page Read-Modify-Write Cycle



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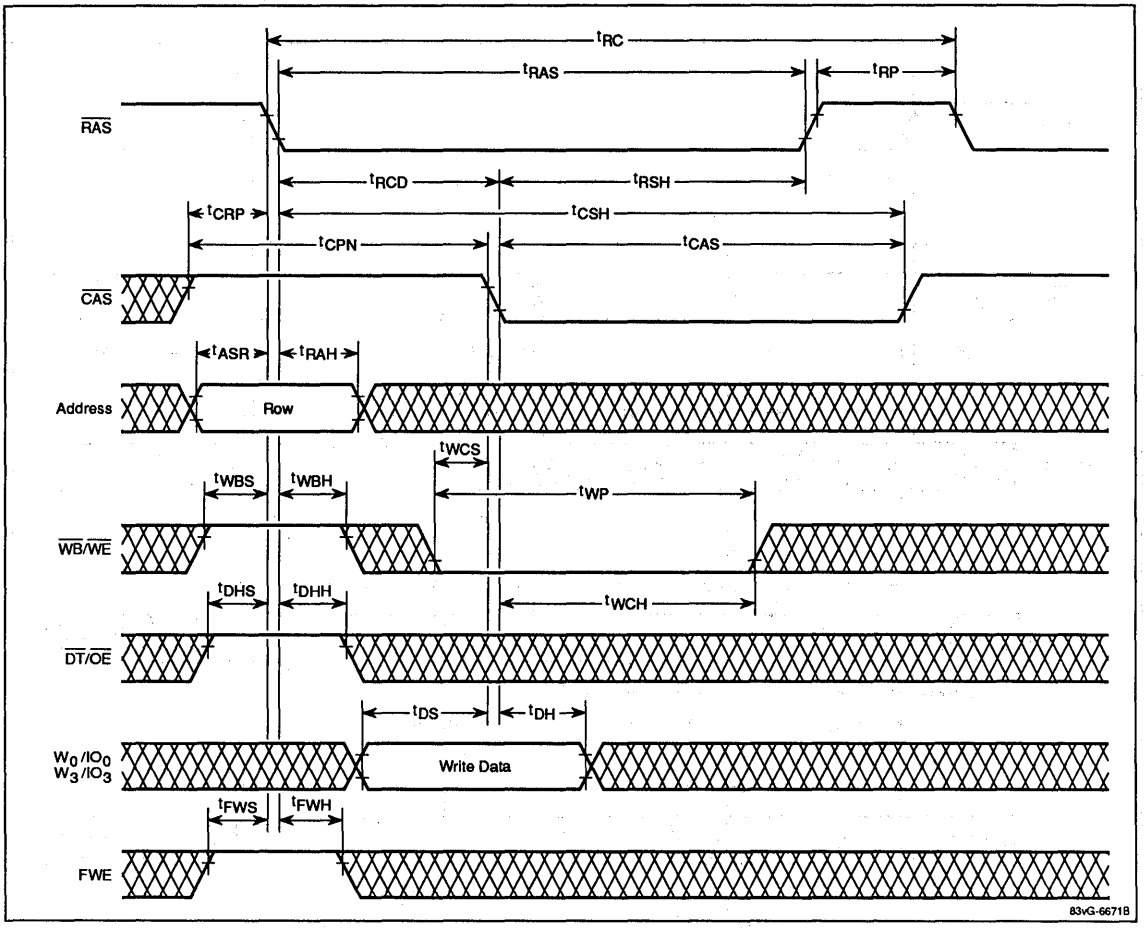
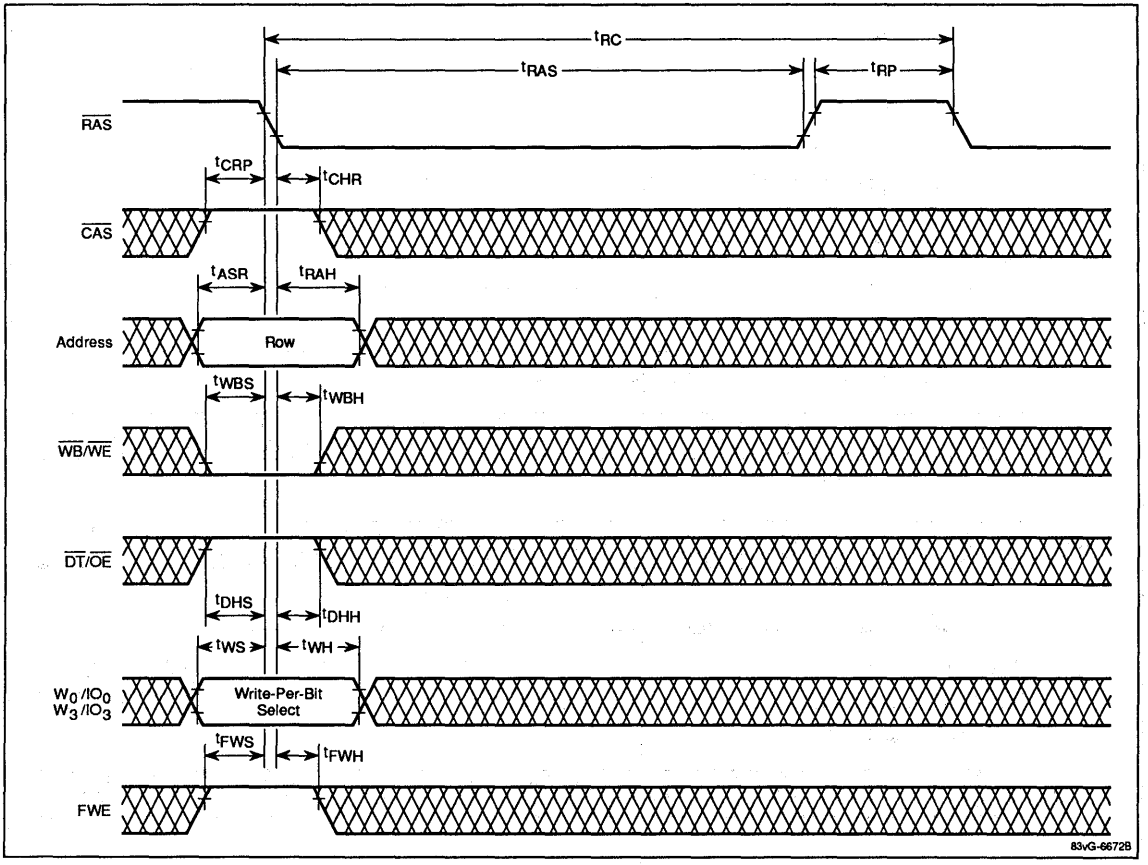
Timing Waveforms (cont)

Color Register Set Cycle



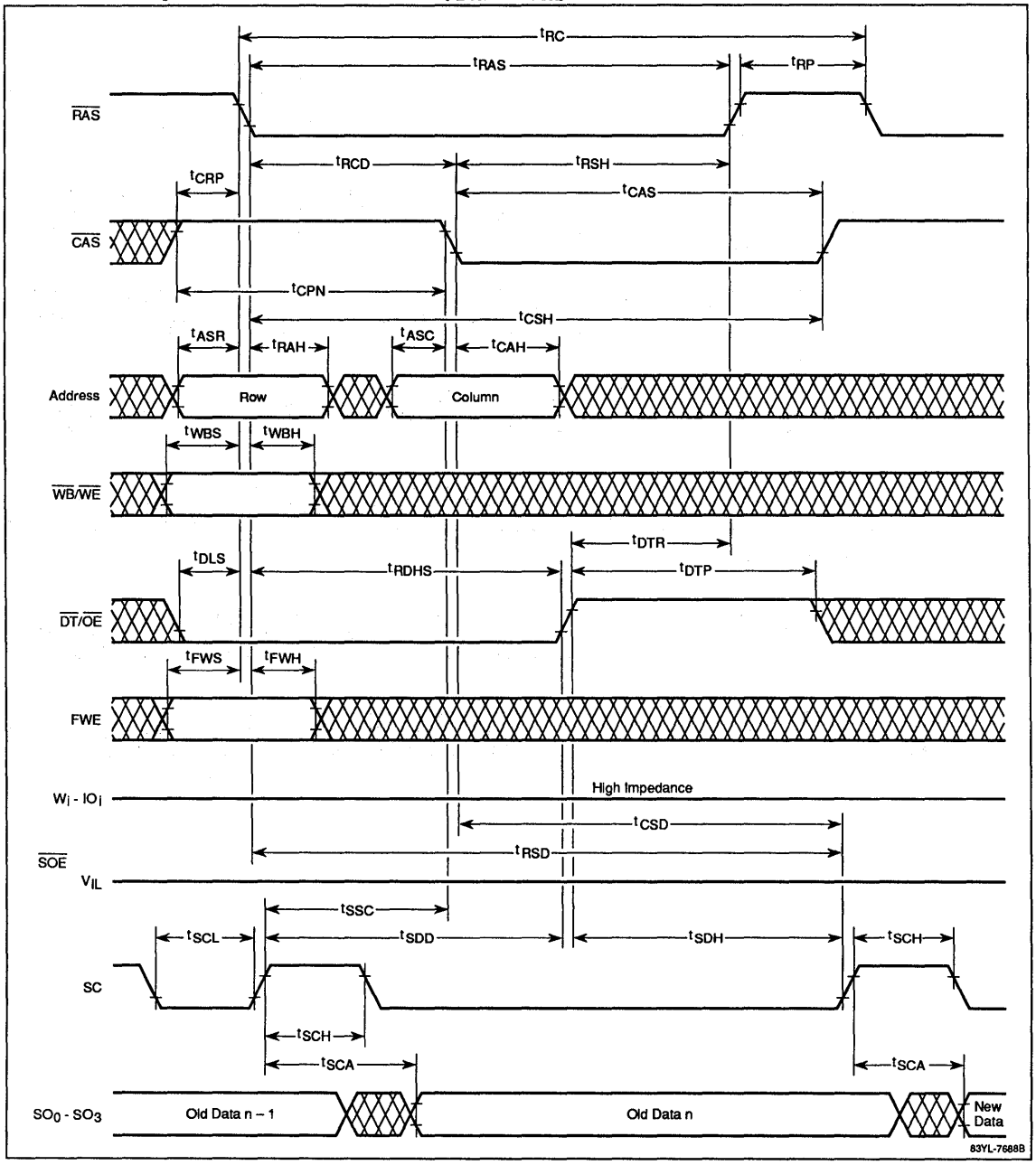
Timing Waveforms (cont)

Flash Write Cycle



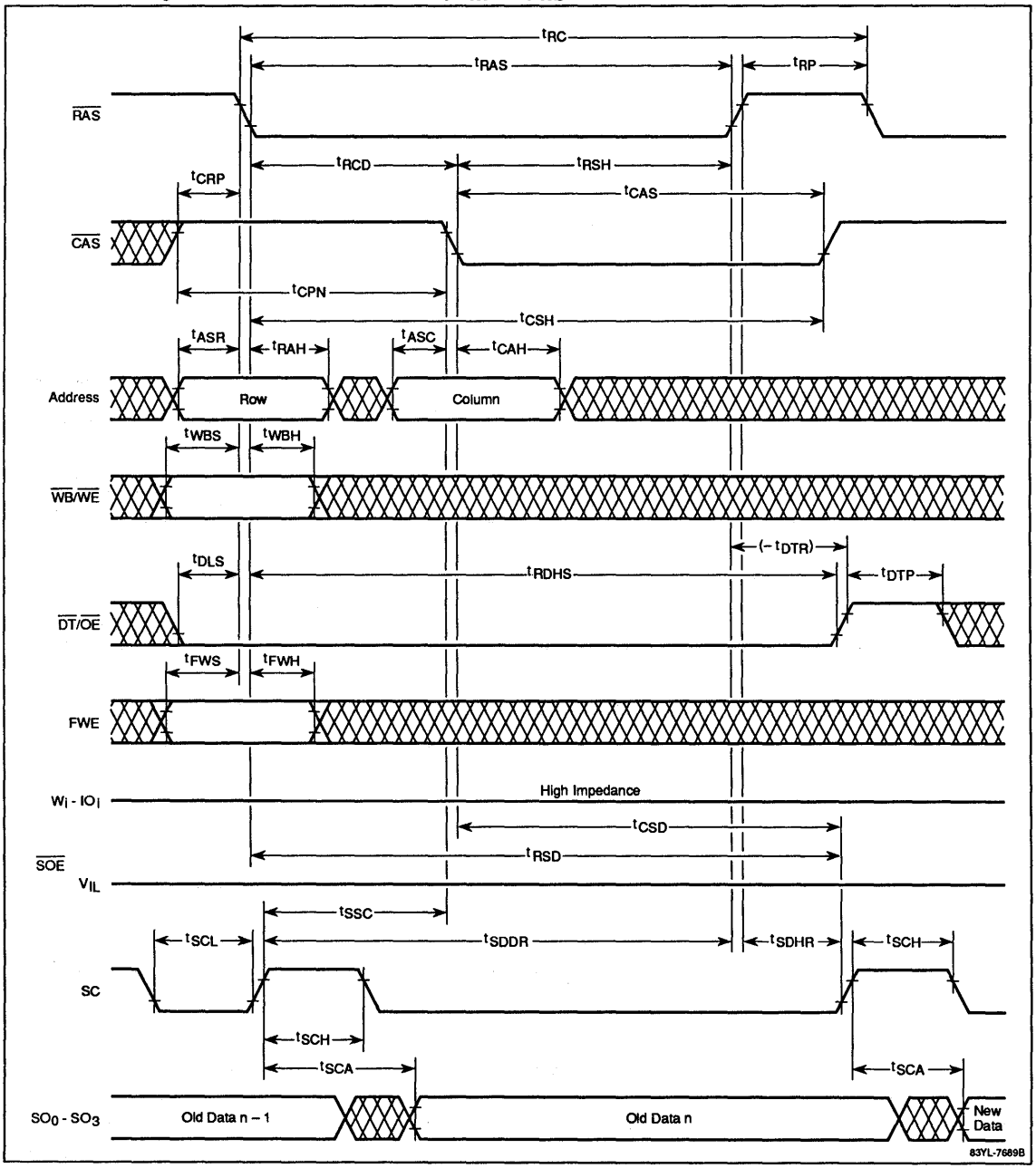
Timing Waveforms (cont)

Data Transfer Cycle with Serial Port Active ($t_{DTR} \geq t_{DTR}$)



Timing Waveforms (cont)

Data Transfer Cycle with Serial Port Active ($t_{DTR} \leq t_{DTR}$)



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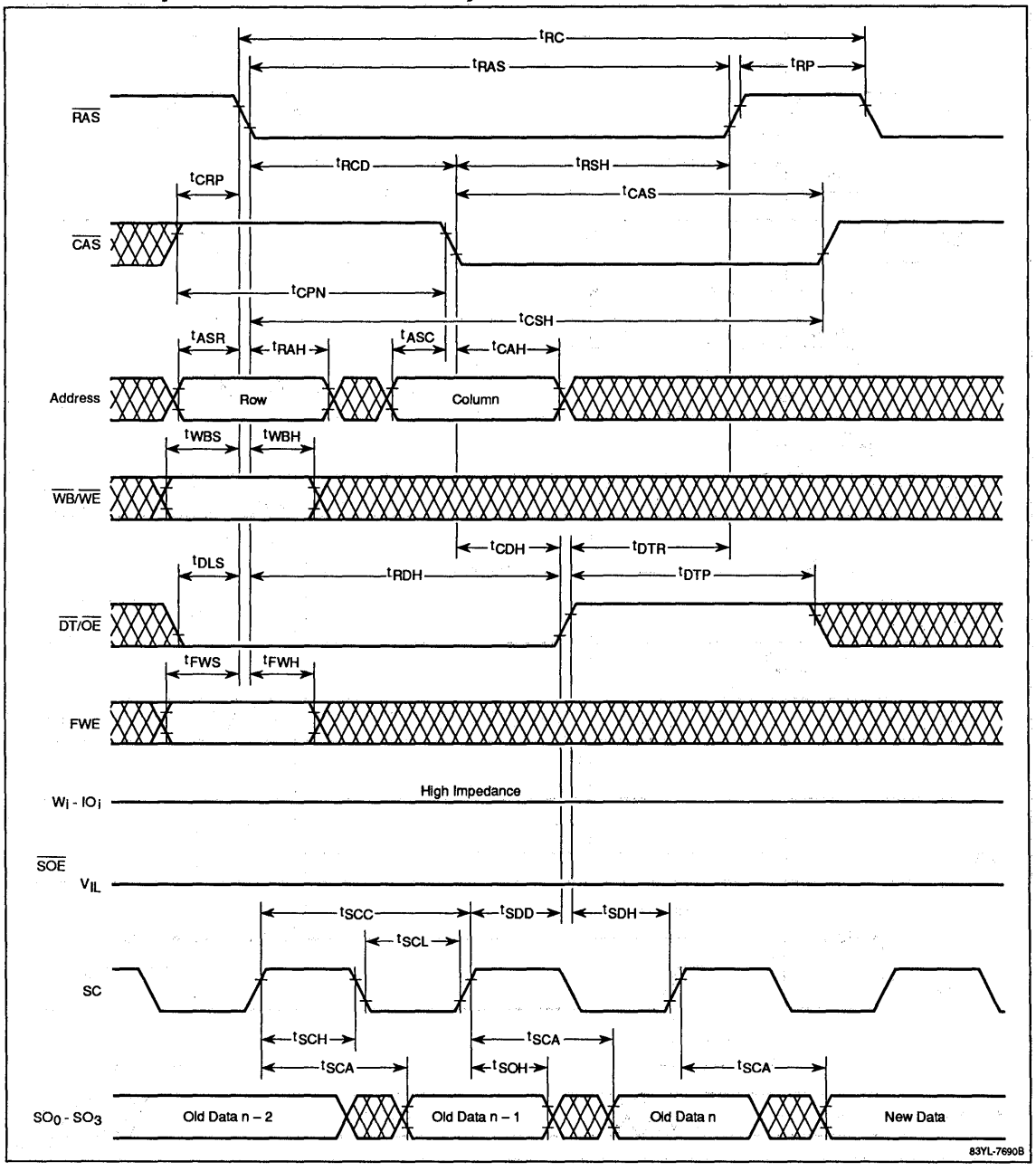
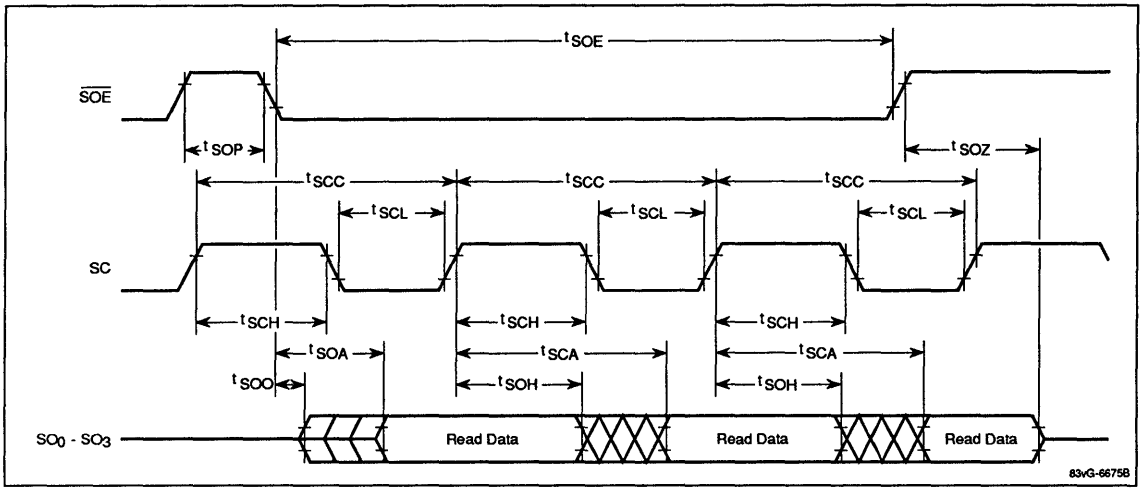
Timing Waveforms (cont)

Data Transfer Cycle with Serial Port in Standby



Timing Waveforms (cont)

Serial Read Cycle



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Description

The μPD42275 is a dual-port graphics buffer equipped with a random access port and a serial read port. The serial read port is connected to an internal 2048-bit data register through a 256 x 8-bit serial read output circuit. The 128K x 8-bit random access port is used by the host CPU to read or write data addressed in any desired order.

A write-per-bit capability allows each of the eight data bits to be individually selected or masked for a write cycle. Block write cycles can also be used to write the eight data bits to four consecutive column addresses. Selection and masking of the eight data bits and four column addresses is provided. A flash write option with write-per-bit control enables data in the color register to be written to a selected row in the random access port.

The μPD42275 features fully asynchronous dual access, except when transferring graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special cycle using a transfer clock; the serial port continues to operate normally. Following the clock transition of a data transfer, serial output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

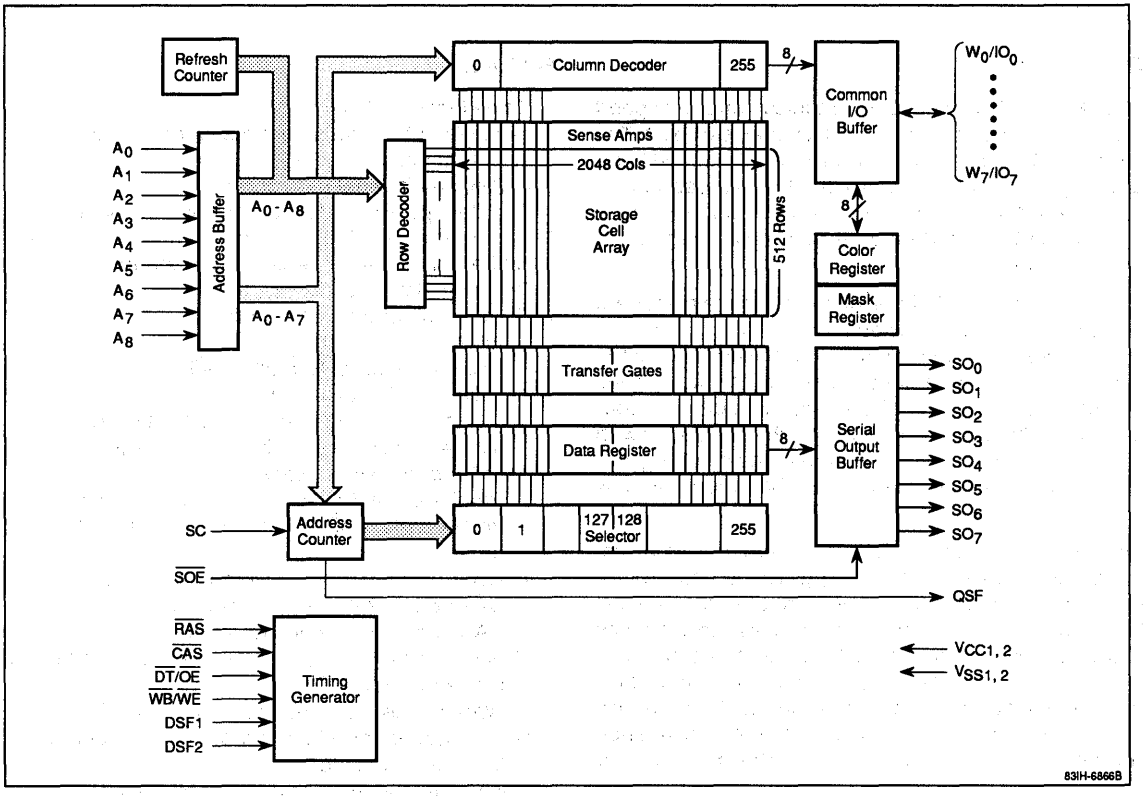
An advanced CMOS silicon-gate process using polycide technology and trench capacitors provides high storage cell density, high performance, and high reliability. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility. The μPD42275 is available in a 400-mil, 40-pin plastic SOJ and is guaranteed for operation at 0 to +70°C.

Features

- Three functional blocks
  - 128K x 8-bit random access storage array
  - 2048-bit data register
  - 256 x 8-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- On-chip substrate bias generator
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - 512 refresh cycles every 8 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page cycles
  - Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - $\overline{CAS}$-controlled hidden refreshing
  - Persistent and nonpersistent write-per-bit option regarding eight I/O bits
  - Write bit selection multiplexed on IO_0 - IO_7
- Block write option with write-per-bit control and column mask function
- Flash write option with write-per-bit control
- Split serial data register to allow shifting from lower half while simultaneously loading upper half
- $\overline{RAS}$-activated data transfer
  - Same cycle time as for random access
  - Row data transferred to data register as specified by row address inputs
  - Starting location of following serial read cycle specified by column address inputs
  - Transfer of 2048 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
- Serial data output on SO_0 - SO_7
- Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- CMOS silicon-gate process with trench capacitors

Block Diagram



Pin Identification

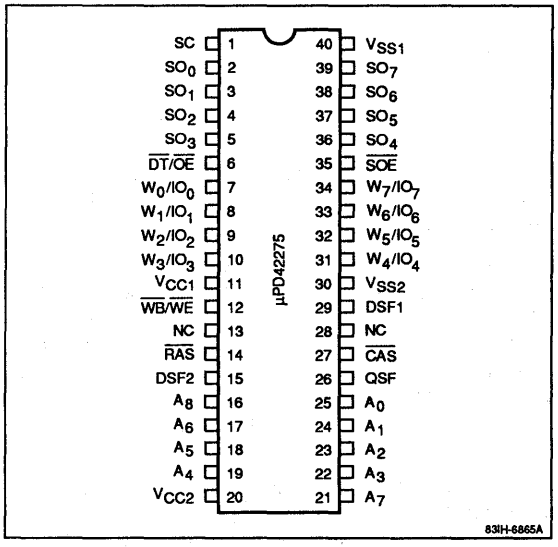
Symbol	Function
A_0 - A_8	Address inputs
W_0/IO_0 - W_7/IO_7	Write-per-bit selects/data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB/WE}$	Write-per-bit/write enable
$\overline{DT/OE}$	Data transfer/output enable
DSF_1 and DSF_2	Special function enable
SO_0 - SO_7	Serial read outputs
SC	Serial control
$\overline{SOE}$	Serial output enable
QSF	Special function output
V_{SS1} and V_{SS2}	Ground
V_{CC1} and V_{CC2}	+5-volt ±10% power supply
NC	No connection

Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42275LE-80	80 ns	25 ns	40-pin plastic SOJ
LE-10	100 ns	25 ns	
LE-12	120 ns	40 ns	

Pin Configuration

40-Pin Plastic SOJ



Pin Functions

A_0-A_8 (Address Inputs). These pins are multiplexed as row and column address inputs. Each of eight data bits in the random access port corresponds to 131,072 storage cells, which means that nine row addresses and eight column addresses are required to decode one cell location. Nine row addresses are first used to select one of the 512 possible rows for a read, write, data transfer, or refresh cycle. Eight column addresses are then used to select the one of 256 possible column decoders for a read or write cycle or the one of 256 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{RAS}$-only refresh cycles.)

W_0/IO_0-W_7/IO_7 (Write-Per-Bit Inputs/Common Data Inputs and Outputs). Each of the eight data bits can be individually latched by these inputs at the falling edge of $\overline{RAS}$ in any write cycle, and then updated at the next falling edge of $\overline{RAS}$. In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$ or $\overline{WE}$.

$\overline{RAS}$ (Row Address Strobe). This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 2048 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The nine row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$, DSF_1 and DSF_2 are simultaneously latched to determine device operation.

$\overline{CAS}$ (Column Address Strobe). This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The eight column address bits are latched at the falling edge of $\overline{CAS}$.

QSF (Special Function Output). This pin indicates which side of the split register is active. QSF high shows that the upper half (addresses 128 through 255) is active, while QSF low indicates the lower half (addresses 0 through 127).

DSF_1 and DSF_2 (Special Function Control). At the leading edge of $\overline{RAS}$ and $\overline{CAS}$, the high or low level of these pins is latched to initiate one of the operations shown in the Truth Table. Holding both pins low causes the device to operate without any special functions.

$\overline{WB/WE}$ (Write-Per-Bit Control/Write Enable). At the falling edge of $\overline{RAS}$, the $\overline{WB/WE}$ and DSF_1 inputs must be low and $\overline{CAS}$ and $\overline{DT/OE}$ high to enable the write-per-bit option. When $\overline{CAS}$, $\overline{DT/OE}$, and DSF_1 are high at the falling edge of $\overline{RAS}$, the level of this signal indicates either a color register set cycle or flash write cycle. A high $\overline{WB/WE}$ can be used at the beginning of a standard write or read cycle.

$\overline{DT/OE}$ (Data Transfer/Output Enable). At the $\overline{RAS}$ falling edge, $\overline{CAS}$ and $\overline{WB/WE}$ high and $\overline{DT/OE}$ low initiate a data transfer. $\overline{DT/OE}$ high initiates conventional read or write cycles and controls the output buffer in the random access port. The level of DSF_1 determines whether this is a read or split read data transfer.

SO_0-SO_7 (Serial Data Outputs). Eight-bit data is read from these pins and remains valid until the next SC signal is activated.

SC (Serial Control). Repeatedly activating this signal causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2048 bits in the data register. The rising edge of SC activates serial read operation, in which 8 of the 2048 data bits are transferred to eight serial data buses, respectively, and read out. Whenever SC is low, the serial port is in standby.

$\overline{SOE}$ (Serial Output Enable). This signal controls the serial data output buffer.

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OPERATION

The μPD42275 consists of a random access port and a serial read port. The random access port executes standard read and write cycles, as well as data transfer, block write and flash write cycles, all of which are based on conventional $\overline{RAS}/\overline{CAS}$ timing.

In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to its corresponding register location. The serial read port shows the contents of the data register in serial order. The random access and serial read ports can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is arranged in a 512-row by 2048-column matrix, whereby each of 8 data bits in the random access port corresponds to 131,072 storage cells and 17 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 through A_8 and latched onto the chip by $\overline{RAS}$. Eight column address bits then are set up on pins A_0 through A_7 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 2048 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through one of 256 column decoders, eight storage cells on the row are connected to eight data buses, respectively. In a data transfer cycle, 9 row address bits are used to select one of the 512 possible rows involved in the transfer of data to the data register. Eight column address bits are then used to select the one of 256 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 8 data bits in the 2048-bit data register are transferred to eight serial data buses and read out. Activating SC repeatedly causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2048 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following are multiplexed.

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3, 4, 5, 6, 7)

The $\overline{OE}$, $\overline{WE}$, and IO_i functions represent standard operations, while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs with setup and hold times referenced to the negative transition of $\overline{RAS}$.

The level of $\overline{DT}$ determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_i defines data bits to be written with the write-per-bit option. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD42275 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 2048-bit register from the corresponding 2048-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 2048 transfer gates and transfer data from one of the rows to the register.

Glossary of Special Functions

Masked Write Cycle with New Mask. When the write-per-bit function is enabled as shown in the following table, mask data on the W/IO_i pins is latched by $\overline{RAS}$ and loaded directly into the write mask register. A masked write cycle is then executed using $\overline{CAS}$ or $\overline{WB}/\overline{WE}$ to strobe the W/IO_i data into the on-chip data latch.

Write-Per-Bit Function

Mask Register Data	Action
1	Write
0	Do not write

Write Mask Register Set Cycle. In this cycle, data on W_i/IO_i is written to an 8-bit write mask register, where it is retained and used by subsequent masked write and masked block write cycles.

Masked Write Cycle with Old Mask. This write-per-bit cycle, commonly referred to as a persistent mask write cycle, uses the mask data previously set by the last write mask register set cycle.

Truth Table for Random Access Port

Cycle	Must Be Valid at Falling Edge of $\overline{RAS}$					Must be Valid at Falling Edge of $\overline{CAS}$	
	$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	DSF_1	DSF_2	DSF_1	Mnemonic Code
Read/write cycle	H	H	H	L	X	L	RW
Block write cycle	H	H	H	L	X	H	BW
Write mask register set cycle	H	H	H	H	X	L	LWR
Color register set cycle	H	H	H	H	X	H	LCR
Write cycle with new mask	H	H	L	L	X	L	RWNM
Block write cycle with new mask	H	H	L	L	X	H	BWNM
Write cycle with old mask	H	H	L	H	L	L	RWOM
Block write cycle with old mask	H	H	L	H	L	H	BWOM
Read data transfer cycle	H	L	H	L	X	X	RT
Split read data transfer cycle	H	L	H	H	X	X	SRT
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	L	X	H	X	X	X	CBR
Flash write cycle with new mask	H	H	L	H	H	X	FWT

Notes:

(1) X = don't care.

(2) Combinations not shown are used for refresh operation.

Block Write Addresses

Column Select By I/O Data	Result	Corresponding Column Address
$I/O_3 = 1$	Write	$A_1 = 1, A_0 = 1$
$I/O_3 = 0$	No write	
$I/O_2 = 1$	Write	$A_1 = 1, A_0 = 0$
$I/O_2 = 0$	No Write	
$I/O_1 = 1$	Write	$A_1 = 0, A_0 = 1$
$I/O_1 = 0$	No write	
$I/O_0 = 1$	Write	$A_1 = 0, A_0 = 0$
$I/O_0 = 0$	No write	

Notes:

(1) Data on I/O_7 - I/O_4 are don't care at the falling edge of $\overline{CAS}$.

Color Register Set Cycle. This cycle is executed in the same fashion as a conventional read or write cycle, with a read or write cycle available to the color register under the control of $\overline{WE}$. In read operation, color register data is read on the common W_i/IO_i pins. In write operation, common W_i/IO_i data can be written into the color register. $\overline{RAS}$-only refreshing is internally performed on the row selected by A_0 through A_8. This setup cycle precedes the first flash write or block write cycle supplying the 8 write data bits.

Block Write Cycle. In a block write cycle, A_1 and A_0 are ignored. I/O_0 - I/O_3 are used to select one or a combination of four column addresses for writing in an early write, late write, page early write, or page late write cycle. Block write data is previously stored in the color register using a set color register cycle. Column select data is latched by the W/IO_i pins at the falling edge of $\overline{CAS}$ or $\overline{WE}$. Block write cycles are useful for clearing windows and for accelerating polygon fill operations.

Masked Block Write Cycle with New Mask. This cycle allows for $W/I/O_0$ - $W/I/O_7$ masking during a block write cycle. The masking function is identical to a standard masked write cycle with new mask, except that four consecutive columns are written.

Masked Block Write Cycle with Old Mask. This cycle uses the masked data previously set by the last write mask register set cycle to write four consecutive columns.

Flash Write Cycle. A flash write cycle can clear or set each of the eight 256-bit data sets on the selected one of 512 possible rows according to data stored in the previously set color register. Bit mask inputs are latched as $\overline{RAS}$. This cycle is useful in graphics processing applications when the screen should be cleared or set to some uniform value as quickly as possible.

Read Data Transfer Cycle. In a full row read data transfer cycle, one of the possible 512 rows, as well as the starting location of the following serial read cycle, is defined by address inputs. The low-to-high transition of DT/($\overline{OE}$) causes the 2048 bits of cell data to be transferred to the serial data register.

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Split Read Transfer Cycle. This cycle is a half-row data transfer in which one of the 512 rows, the starting location of the following serial read cycle, and either of the split registers are specified by the address inputs. On-chip control circuitry causes the previously specified half row to be transferred to the selected upper or lower split register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining ($\overline{WB}$/)$\overline{WE}$ while $\overline{CAS}$ is active. The (W_i/)IO_i pin (i = 0 through 7) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance.

Write Cycle. A write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes the data on (W_i/)IO_i into the on-chip data latch. To make use of the write-per-bit option, $\overline{WB}$/($\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case, write data bits can be specified by keeping W_i/(IO_i) high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

Write-Per-Bit Cycle. The falling edge of $\overline{RAS}$ latches the write-per-bit mask data input on W_0 through W_7. If DSF_1 is low at the falling edge of $\overline{RAS}$, mask data must be reloaded every write-per-bit mask cycle. If DSF_1 is high and DSF_2 is low at the falling edge of $\overline{RAS}$, mask data is not reloaded from W_0 through W_7 but is retained from the previous write mask set cycle. The latter is called a persistent write-per-bit cycle.

Early Write Cycle. An early write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low before $\overline{CAS}$ falls. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, ($\overline{DT}$/)$\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$, but otherwise ($\overline{DT}$/)$\overline{OE}$ does not affect any circuit operation while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. This cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i returns to high impedance when ($\overline{DT}$/)$\overline{OE}$ goes high. The data to be written is strobed by ($\overline{WB}$/)$\overline{WE}$ with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of ($\overline{DT}$/)$\overline{OE}$, which can be activated just after ($\overline{WB}$/)$\overline{WE}$ falls, even when ($\overline{WB}$/)$\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 through A_8) will refresh all storage cells. Any cycle executed in the random access port (i.e., read, write, refresh, data transfer, color register set, flash write or block write) refreshes the 2048 bits selected by the $\overline{RAS}$ addresses or by the on-chip address counter.

$\overline{RAS}$-Only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes all cells in one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep (W_i/)IO_i in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This cycle is executed after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed causes data to be transferred at a faster rate because

row addresses are maintained internally and do not have to be reapplied. In fast-page operation, read, write, and read-write/read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the next fast-page write cycle.

During a fast-page read cycle, the $(W_i)IO_i$ data pin (i = 0 through 7) remains in a state of high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be the longest of the following intervals:

- t_{ACP}
- $t_{CP} + t_T + t_{CAC}$
- $\overline{CAS}$ high to column address delay + t_{AA}

Serial Read Port

The serial read port is used to serially read the previously loaded contents of the data register starting from a specified location. Other graphics buffers require very tight timing to synchronize this port with the random access port, but the μPD42275 has been designed with a split register to eliminate the need for synchronized timing between the two ports.

Split Register Data Transfer. A review of the split register architecture shows that the lower register (addresses 0 - 127) and upper register (addresses 128 - 255) are selected by the most significant bit of the column addresses (A_7). With the serial port split in half, data transfers can be executed to the inactive side (no SC clocks) while SC clocks are input to access data from the active side. This sequence allows for a longer time window to perform the transfer, i.e., 128 x t_{SCC}, or 3.84 μs. Column address bits A_0 through A_6 are latched on-chip to provide the tap address pointer for each split register.

QSF Special Function Output. This pin outputs a signal indicating which half of the data register is active and is synchronized with the SC clock.

Split Data Transfer Cycle

Portion of Split Register	QSF
0 through 127	Low
128 through 255	High

Notes:

(1) A full data transfer cycle must precede all split register operations.

(2) Column address A_7 must be specified for a split data transfer cycle.

Data in the data register is clocked serially by SC, starting from the first specified address of either register. After the last specified address has been transferred, QSF changes its level at the next rising edge of SC, and serial data transfer switches to the other (formerly inactive) register. Serial data output is maintained until the next SC clock.

SC clocks at the transition point, i.e., the end of one half and the beginning of the new half of the split registers, are restricted. Rising edges of the SC clock are not allowed for the last serial address (either 127 or 255) of the active register and for the first address (any address depending on current address pointer) of the next active register (figure 2).

$\overline{SOE}$ controls impedance of the serial output to allow multiplexing of more than one bank of μPD42275s on the same bus and has no effect on SC. When $\overline{SOE}$ is low, SO_i is disabled and in a state of high impedance.

Figure 1. Example of Split Register Transfer

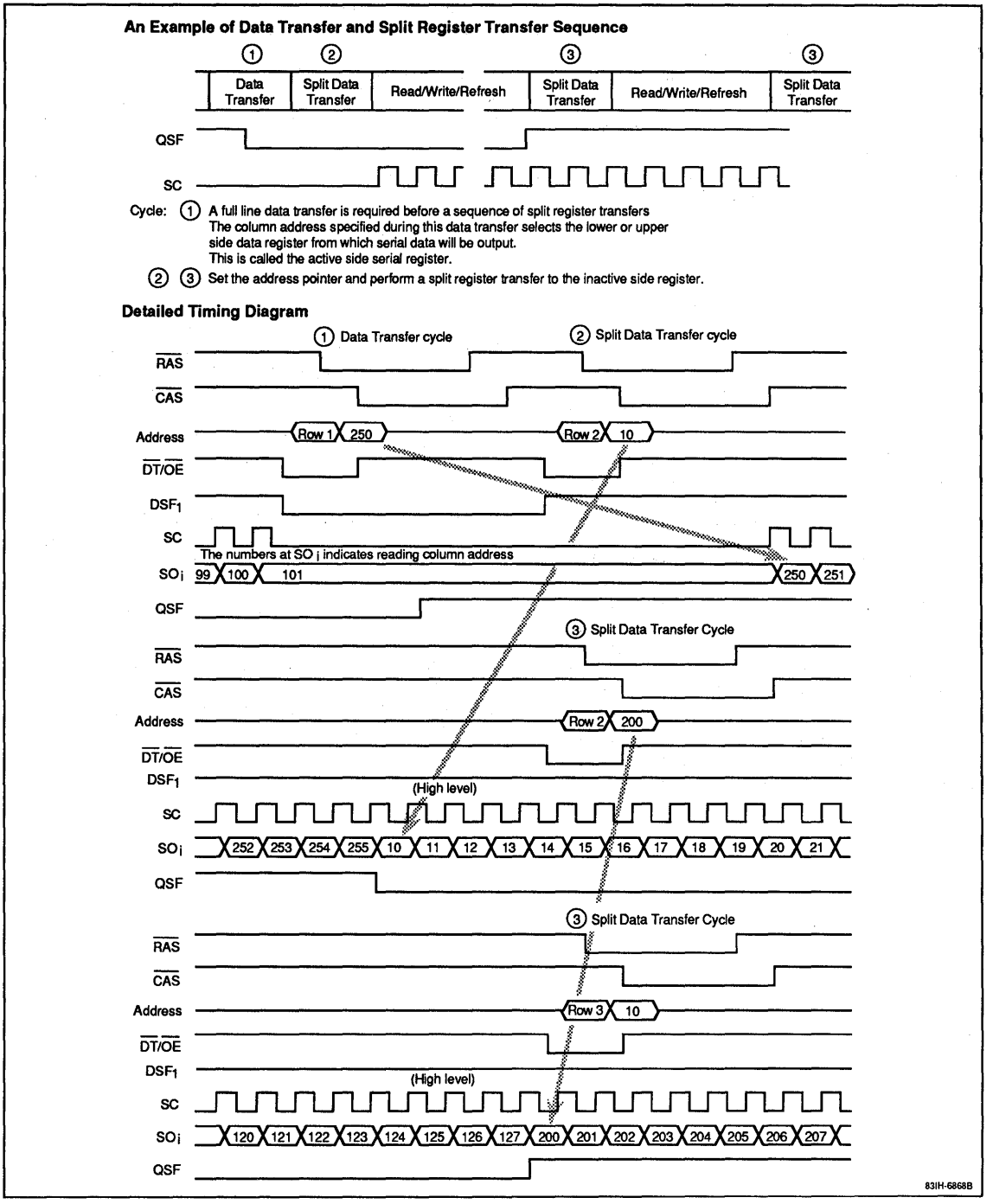
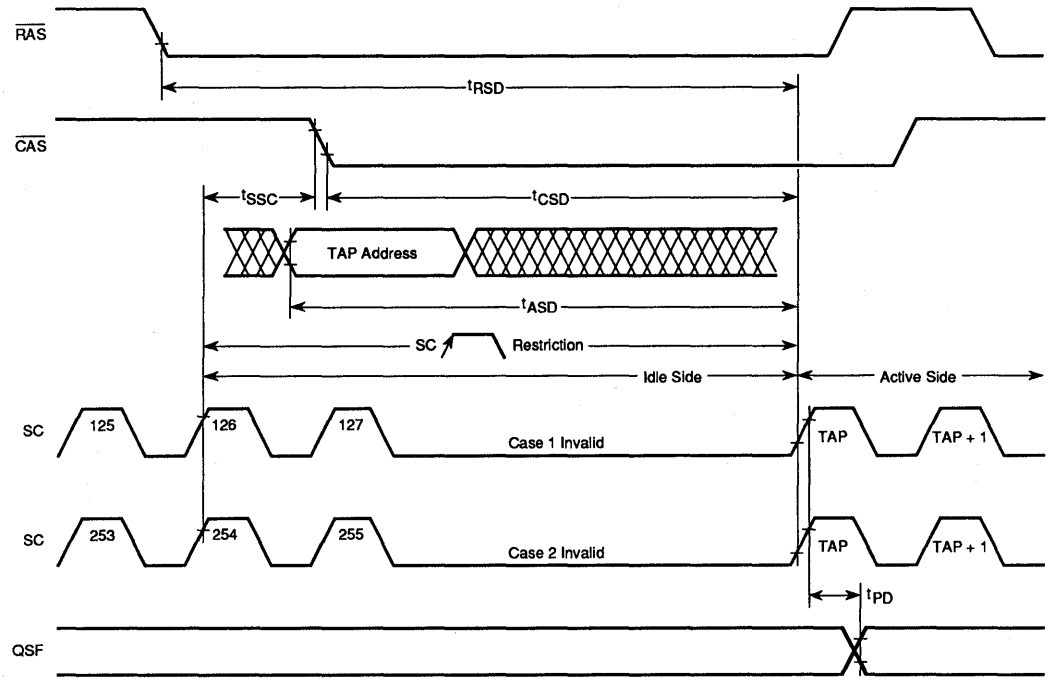


Figure 2. Restrictions on Rising Edges of SC



Note:

[1] For split register transfers, there is a restriction on the SC clocks at the transition point from the end of one half to the beginning of the other half split register. Rising edges of the SC clock are not allowed for the last serial address of the idle split register (127 or 255).

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Absolute Maximum Ratings

Voltage on any pin relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Max (pF)	Pins Under Test
Input capacitance	$C_{I(A)}$	5	A_0 - A_8
	$C_{I(\overline{DT}/\overline{OE})}$	8	$\overline{DT}/\overline{OE}$
	$C_{I(\overline{WB}/\overline{WE})}$	8	$\overline{WB}/\overline{WE}$
	$C_{I(DSF)}$	8	DSF_1 and DSF_2
	$C_{I(\overline{RAS})}$	8	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	$\overline{SOE}$
	$C_{I(SC)}$	8	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	W_0/IO_0 - W_7/IO_7
Output capacitance	$C_{O(SO)}$	7	SO_0 - SO_7
	$C_{O(QSF)}$	7	QSF

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Port Operation							
Random Access	**Serial Read**	**Parameter**	**-80 (max)**	**-10 (max)**	**-12 (max)**	**Unit**	**Test Conditions**
Read/write cycle	Standby	I_{CC1}	95	85	70	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; DSF_1 and DSF_2 low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Standby	Standby	I_{CC2}	10	10	10	mA	D_{OUT} = high impedance; address cycling; $t_{RC} = t_{RC}$ min; $\overline{CAS} = \overline{RAS} = V_{IH}$; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 4)
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	85	80	65	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; DSF_1 and DSF_2 low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 2)
Fast-page cycle	Standby	I_{CC4}	85	80	65	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	85	75	60	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Data transfer cycle	Standby	I_{CC6}	115	100	85	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Read/write cycle	Active	I_{CC7}	125	110	90	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; DSF_1 and DSF_2 low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Standby	Active	I_{CC8}	40	35	30	mA	D_{OUT} = high impedance; address cycling; $t_{RC} = t_{RC}$ min; $\overline{CAS} = \overline{RAS} = V_{IH}$; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 4)
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	115	105	85	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; DSF_1 and DSF_2 low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Fast-page cycle	Active	I_{CC10}	105	90	75	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	115	100	80	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Data transfer cycle	Active	I_{CC12}	145	125	105	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Color register set cycle	Standby	I_{CC13}	80	70	55	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Flash write cycle	Standby	I_{CC14}	80	70	55	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Color register set cycle	Active	I_{CC15}	110	95	75	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min

Power Supply Current (cont)

Port Operation							
Random Access	**Serial Read**	**Parameter**	**-80 (max)**	**-10 (max)**	**-12 (max)**	**Unit**	**Test Conditions**
Flash write cycle	Active	I_{CC16}	110	95	75	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Block write cycle	Standby	I_{CC17}	95	85	75	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Block write cycle	Active	I_{CC18}	125	110	95	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, I_{CC6}, and I_{CC14}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked, but is kept at a stable high level. The column addresses are also assumed to be kept stable, at either a high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

(4) A change in row addresses must not occur more than once in a read or write cycle.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	-10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	-10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = -1 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 2.1 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = -1 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 2.1 mA

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

		μPD42275-80		μPD42275-10		μPD42275-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Access time from column address	t_{AA}		45		50		65	ns	(Notes 3 and 4)
Access time from rising edge of $\overline{CAS}$	t_{ACP}		45		55		65	ns	(Notes 3 and 4)
$\overline{DT}$ low hold time after address	t_{ADD}	35		35		45		ns	(Note 15)
Column address setup time	t_{ASC}	0		0		0		ns	
Address to SC high delay	t_{ASD}	55		60		75		ns	(Notes 16 and 18)
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay	t_{AWD}	70		85		100		ns	(Note 7)
Access time from falling edge of $\overline{CAS}$	t_{CAC1}		20		25		30	ns	(Notes 3 and 4
Access time from $\overline{CAS}$, mask register read cycle	t_{CAC2}		30		35		40	ns	(Note 14)
Column address hold time	t_{CAH}	15		15		25		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	35	10,000	ns	
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	25		30		35		ns	(Note 15)
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	12		12		15		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42275-80		μPD42275-10		μPD42275-12		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		15		ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	10		10		15		ns	
$\overline{CAS}$ to QSF delay time	t_{CQD}		70		70		100	ns	(Notes 16 and 19)
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ low to SC high delay	t_{CSD}	45		55		65		ns	(Notes 16 and 18)
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	0		0		0		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	45		55		65		ns	(Note 7)
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		30		35		ns	
Data-in hold time	t_{DH}	15		20		25		ns	(Note 8)
$\overline{DT}$ high hold time	t_{DHH}	12		12		15		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		0		ns	
$\overline{DT}$ low setup time	t_{DLS}	0		0		0		ns	
Propagation delay time from $\overline{DT}/\overline{OE}$ to QSF	t_{DQD}		35		35		55	ns	(Note 20)
Propagation delay time from $\overline{RAS}$ to QSF	t_{DQR}		45		55		70	ns	(Note 20)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 8)
$\overline{DT}$ high pulse width	t_{DTP}	25		30		35		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	0		0		0		ns	(Note 15)
DSF_1 hold time from $\overline{CAS}$	t_{FCH1}	15		15		25		ns	
DSF_1 setup time from $\overline{CAS}$	t_{FCS1}	0		0		0		ns	
DSF_1 hold time from $\overline{RAS}$	t_{FRH1}	12		12		15		ns	
DSF_2 hold time from $\overline{RAS}$	t_{FRH2}	12		12		15		ns	
DSF_1 setup time from $\overline{RAS}$	t_{FRS1}	0		0		0		ns	
DSF_2 setup time from $\overline{RAS}$	t_{FRS2}	0		0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		20		25		30	ns	(Notes 3 and 4)
$\overline{OE}$ high to data-in setup delay	t_{OED}	20		25		30		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	20		20		30		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		10		ns	
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	20	0	25	0	30	ns	(Note 5)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	20	0	20	0	30	ns	(Note 5)
Fast-page cycle time	t_{PC}	50		60		70		ns	(Note 11)
Propagation delay time from SC to QSF	t_{PD}		25		25		40	ns	
Fast-page read-write/read-modify-write cycle time	t_{PRWC}	105		125		145		ns	(Note 11)
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 3 and 4)
$\overline{RAS}$ to column address delay time	t_{RAD}	17		17		20		ns	(Note 9)
Row address hold time	t_{RAH}	12		12		15		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42275-80		μPD42275-10		μPD42275-12		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Column address to $\overline{RAS}$ lead time	t_{RAL}	45		55		65		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	80	100,000	100	100,000	120	100,000	ns	
Random read or write cycle time	t_{RC}	160		180		220		ns	(Note 11)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD1}	22	60	25	75	25	90	ns	(Note 4)
$\overline{RAS}$ to $\overline{CAS}$ delay time, mask register read cycle	t_{RCD2}	22	50	25	65	25	80	ns	(Note 14)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		0		ns	(Note 6)
Read command setup time	t_{RCS}	0		0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low, serial port active	t_{RDH}	65		80		95		ns	(Note 15)
$\overline{DT}$ low hold time after $\overline{RAS}$ low, serial port in standby, split data transfer	t_{RDHS}	12		12		15		ns	(Notes 16 and 18)
Refresh interval	t_{REF}		8		8		8	ms	Addresses A_0 through A_8
$\overline{RAS}$ precharge time	t_{RP}	70		70		90		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ to QSF delay time	t_{RQD}		105		120		155	ns	(Notes 16 and 19)
Read command hold time after $\overline{RAS}$ high	t_{RRH}	0		0		0		ns	(Note 6)
$\overline{RAS}$ low to SC high delay	t_{RSD}	85		105		125		ns	(Note 18)
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
Read-write/read-modify-write cycle time	t_{RWC}	220		245		295		ns	(Note 11)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		155		ns	(Note 7)
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		30		35		ns	
Serial output access time from SC	t_{SCA}		25		25		40	ns	(Note 3)
Serial clock cycle time	t_{SCC}	25		30		40		ns	(Note 11)
SC pulse width	t_{SCH}	7		10		15		ns	
SC precharge time	t_{SCL}	7		10		15		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	5		5		5		ns	(Note 15)
SC low hold time after $\overline{DT}$ high	t_{SDH}	10		15		20		ns	(Note 15)
SC low hold time after $\overline{RAS}$ high	t_{SDHR}	25		30		40		ns	(Note 16)
Serial output access time from $\overline{SOE}$	t_{SOA}		20		25		30	ns	(Note 3)
$\overline{SOE}$ pulse width	t_{SOE}	7		10		15		ns	
Serial output hold time after SC high	t_{SOH}	5		7		7		ns	
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		5		ns	
$\overline{SOE}$ precharge time	t_{SOP}	7		10		15		ns	

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AC Characteristics (cont)

Parameter	Symbol	μPD42275-80 Min	μPD42275-80 Max	μPD42275-10 Min	μPD42275-10 Max	μPD42275-12 Min	μPD42275-12 Max	Unit	Test Conditions
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	10	0	15	0	20	ns	(Note 5)
SC high to $\overline{CAS}$ low delay	t_{SSC}	10		10		10		ns	(Notes 16 and 18)
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Notes 3 and 10)
Write-per-bit hold time	t_{WBH}	12		12		15		ns	
Write-per-bit setup time	t_{WBS}	0		0		0		ns	
Write command hold time	t_{WCH}	15		20		25		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 7)
Write bit selection hold time	t_{WH}	12		12		15		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 13)
Write bit selection setup time	t_{WS}	0		0		0		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) See figures 3 and 4 for reference voltages and figures 5 and 6 for output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(7) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of ($\overline{WB}$/)$\overline{WE}$ in delayed write or read-modify-write cycles.

(9) Assumes that t_{RAD} (min) = t_{RAH} (min) + typical t_T of 5 ns.

(10) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(11) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(12) The t_{CRP} requirement is applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(14) Only for mask register read operation during register read cycles.

(15) For real-time data transfer operation (data transfer with $\overline{SC}$ active).

(16) For read data transfers with serial port in standby.

(17) Ac measurements assume t_T = 5 ns.

(18) For split data transfer cycles.

(19) If $t_{CDH} \leq t_{CDH}$ (min) or $t_{RDHS} \leq t_{RDH}$ (min), then the delay time for the switching of QSF is determined by t_{RQD} or t_{CQD}, whichever occurs later.

(20) If $t_{CDH} \geq t_{CDH}$ (min) and $t_{RDHS} \geq t_{RDH}$ (min), then the switching delay time of QSF is determined by t_{DQD} or t_{DQR}, whichever occurs first.

Figure 3. Input Timing

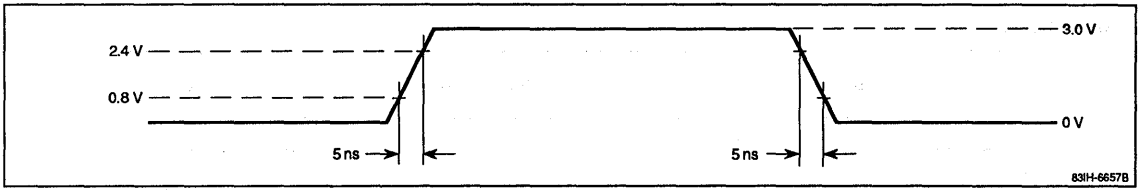


Figure 4. Output Timing

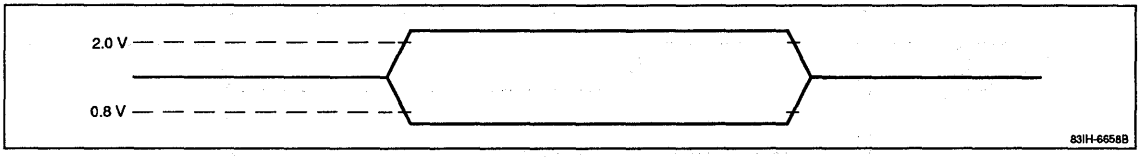


Figure 5. Output Load in Random Access Port

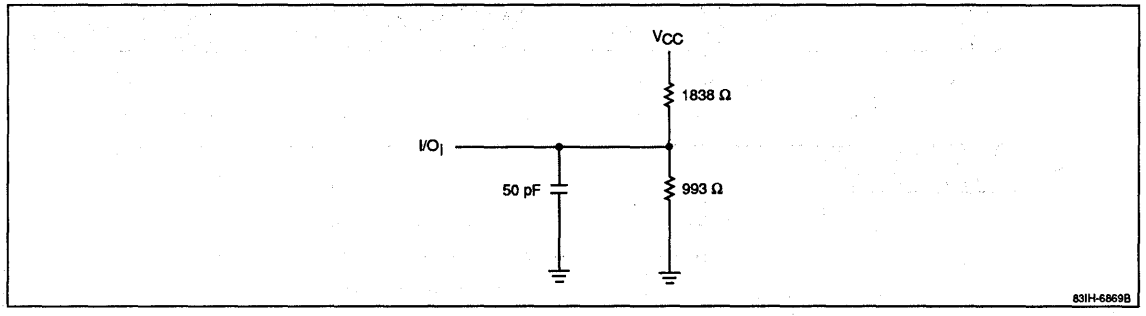
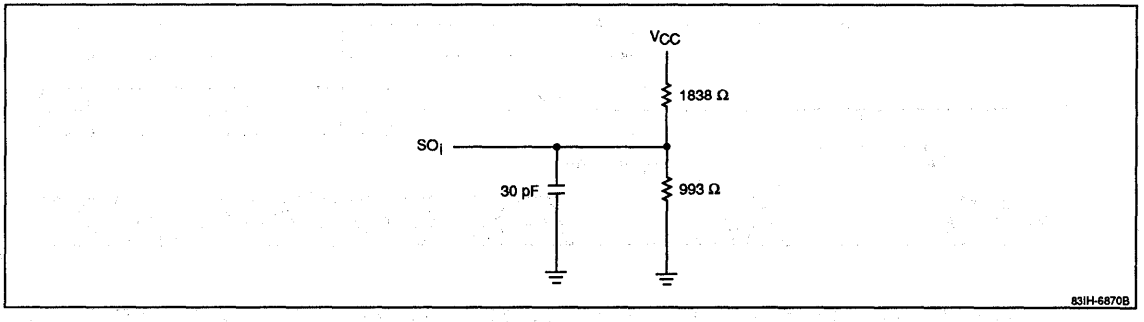


Figure 6. Output Load in Serial Read Port



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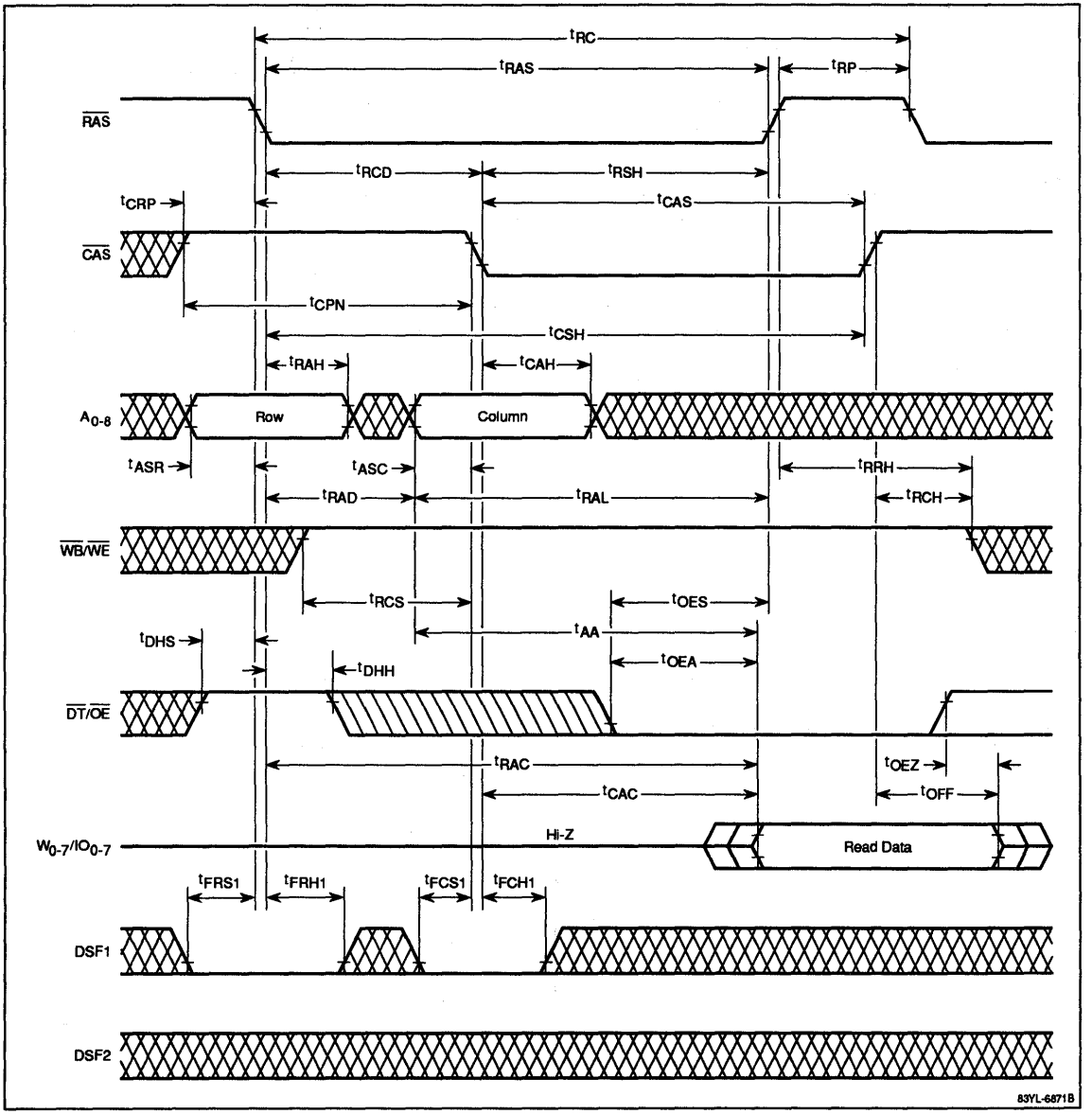
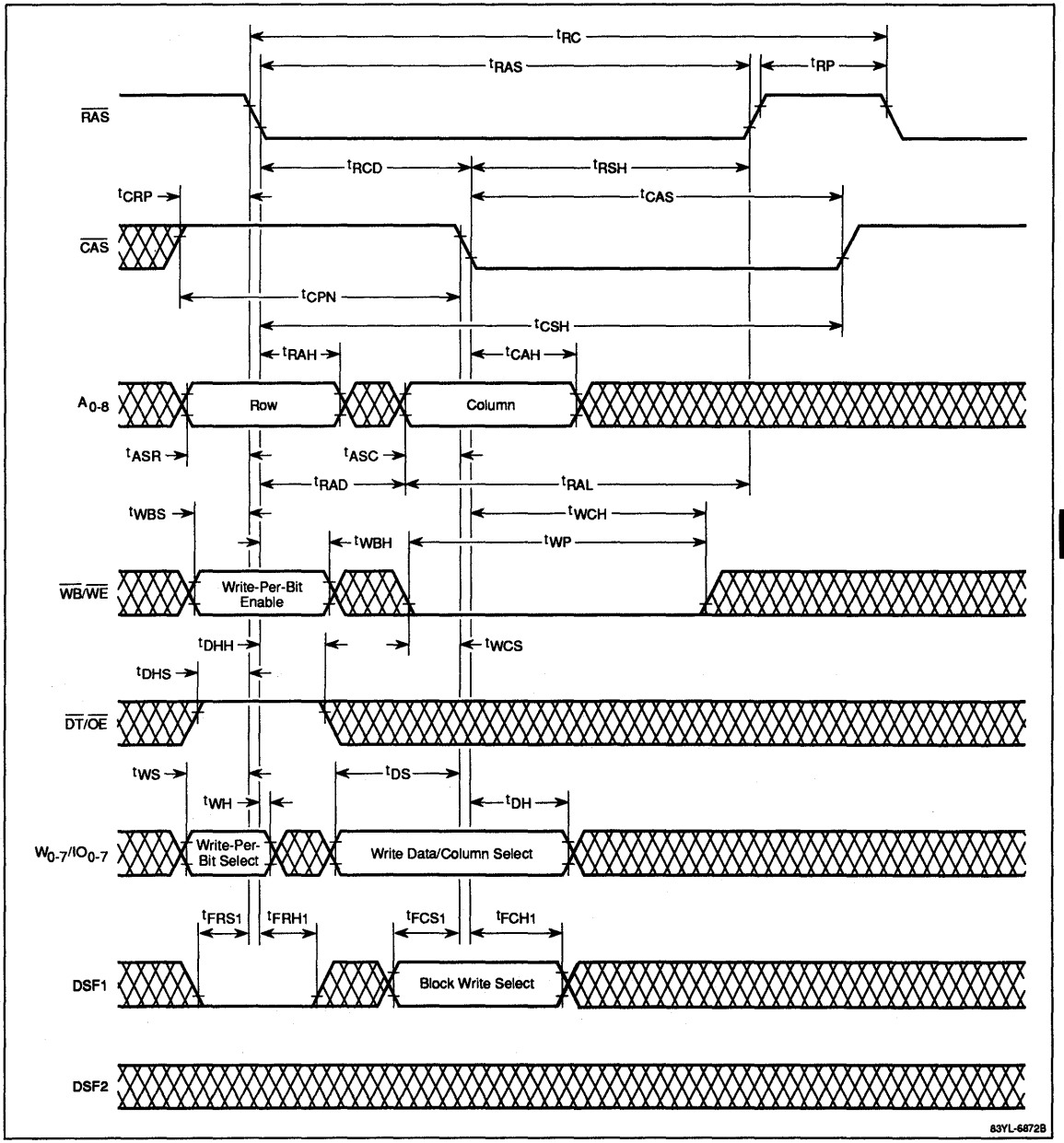
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle and Early Block Write Cycle



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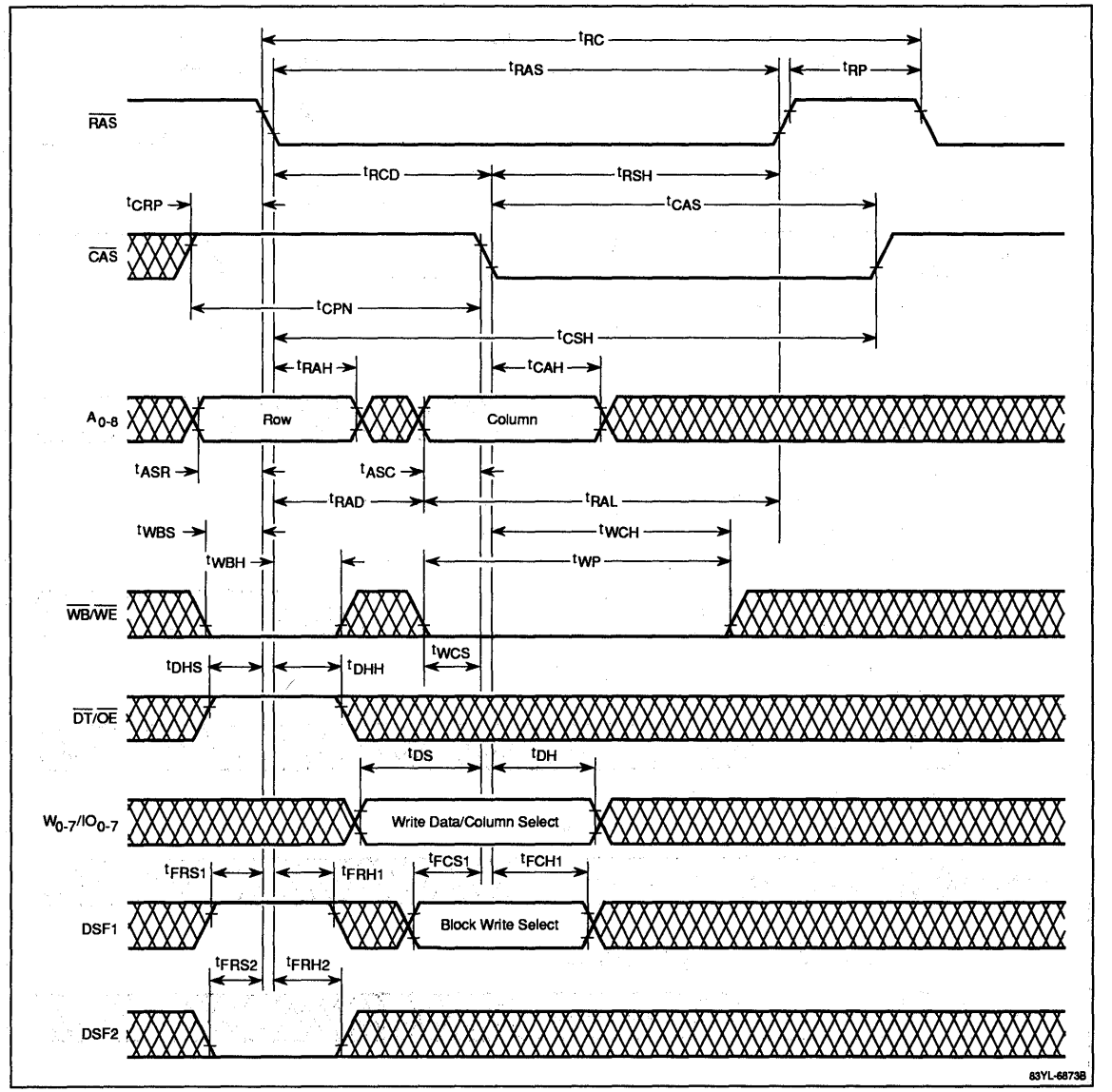
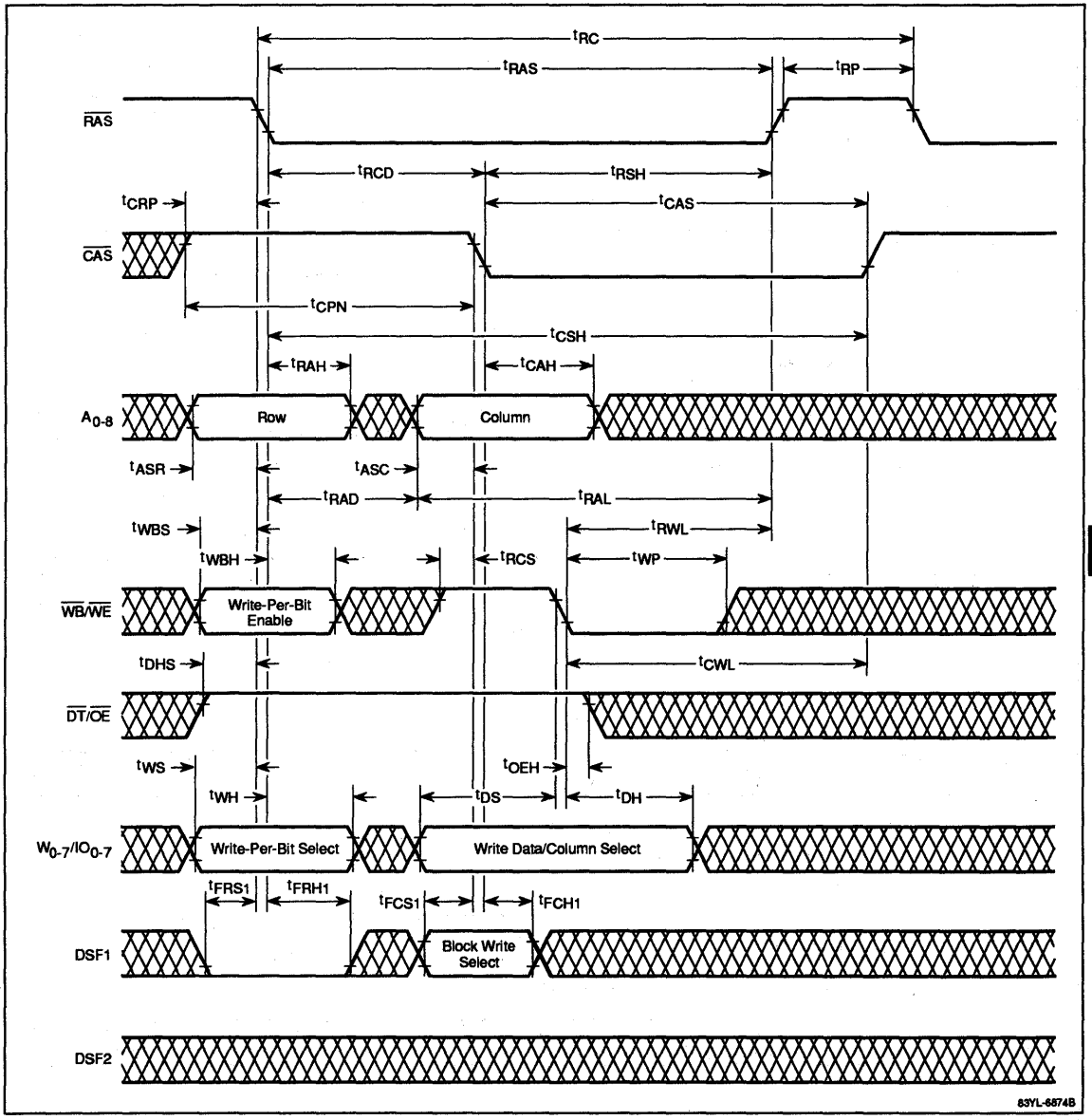
Timing Waveforms (cont)

Early Write Cycle and Early Block Write Cycle With Old Mask



Timing Waveforms (cont)

Late Write Cycle and Late Block Write Cycle



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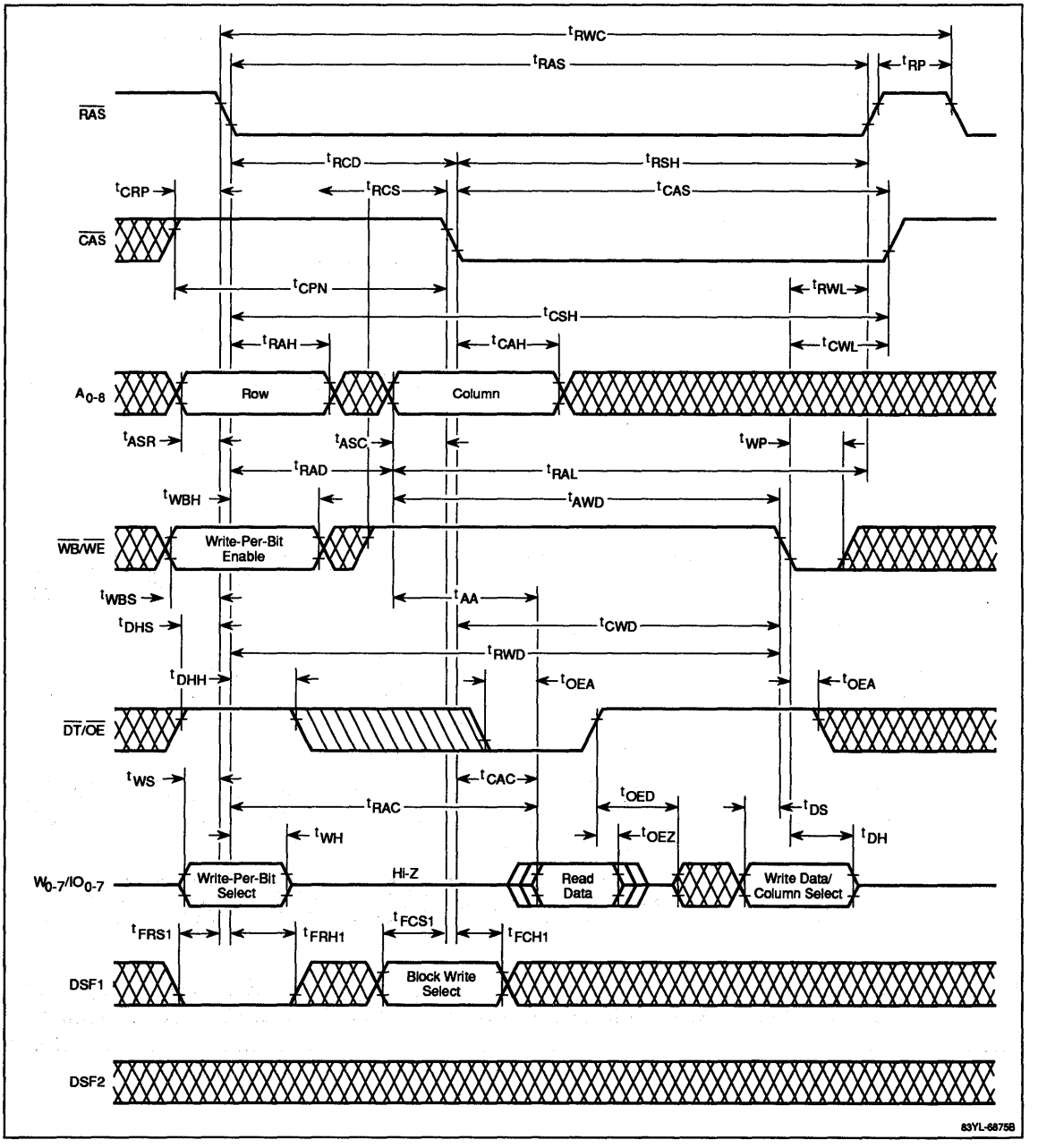
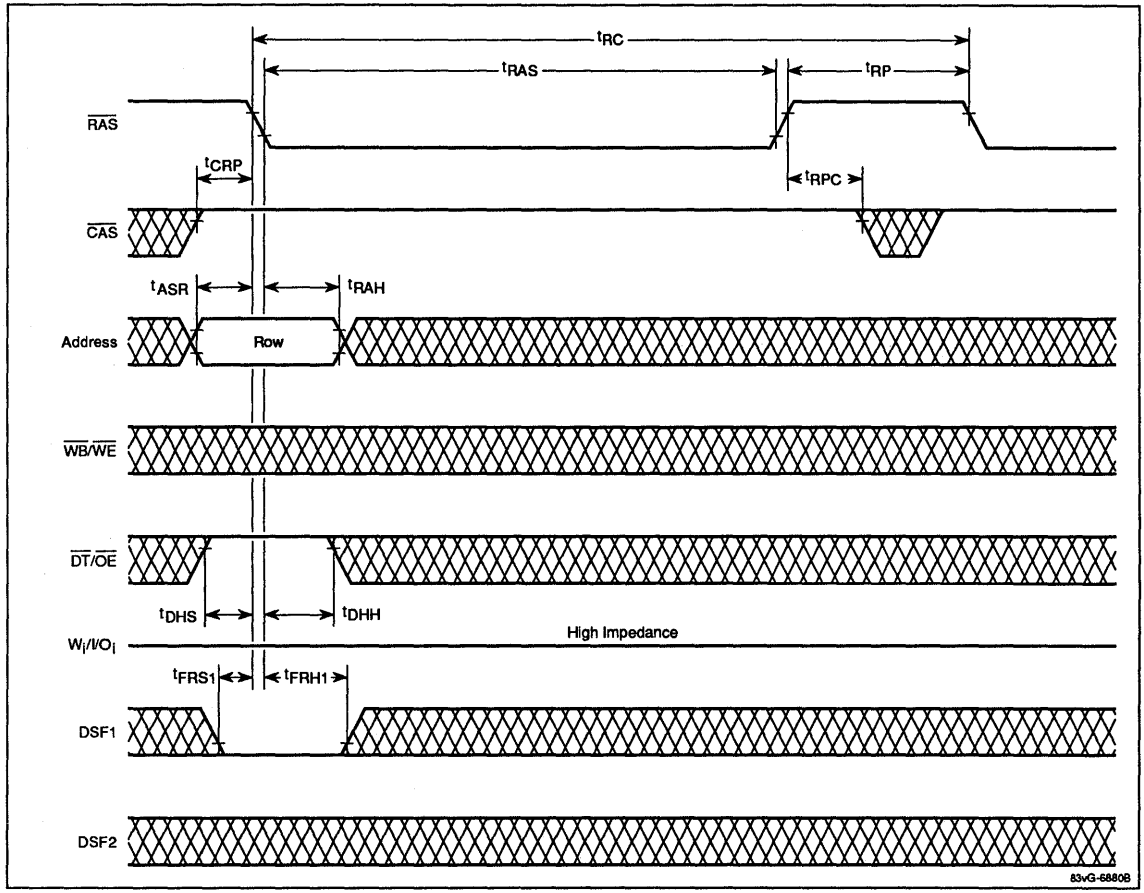
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



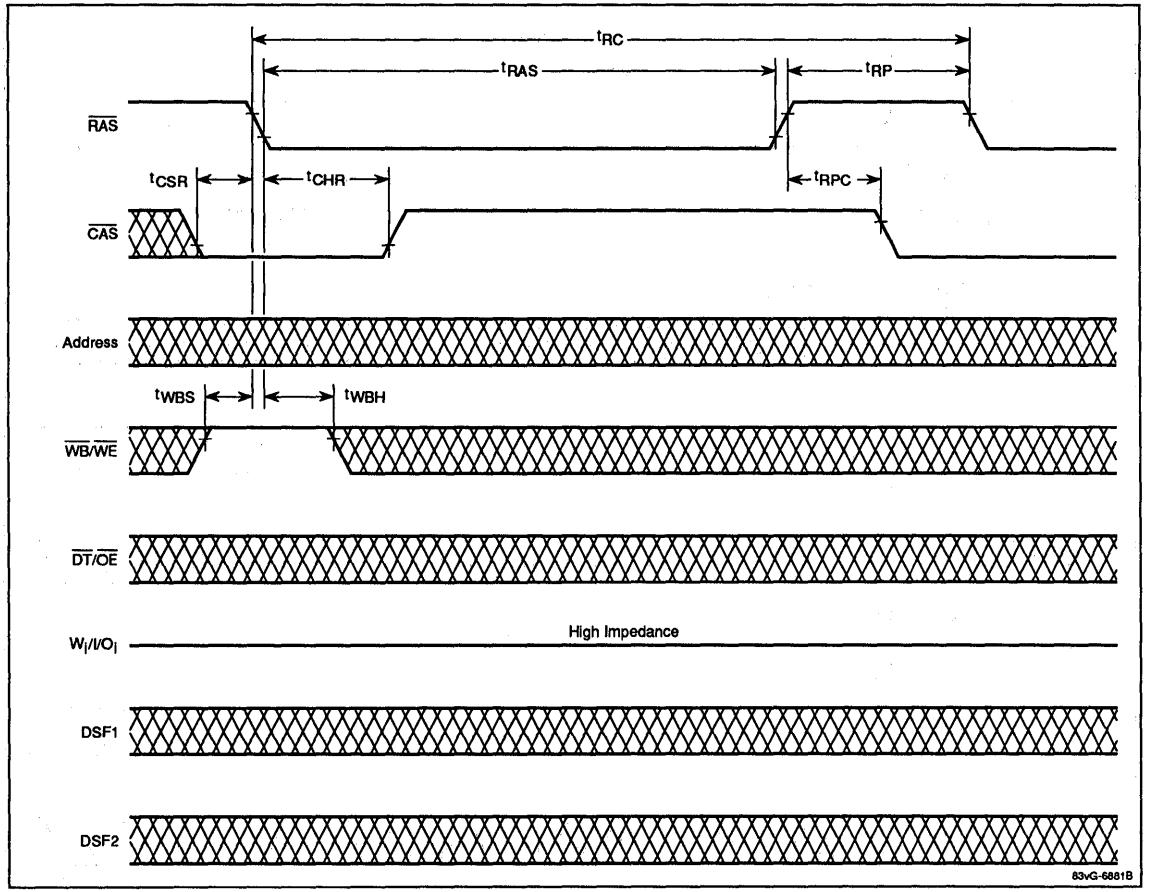
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



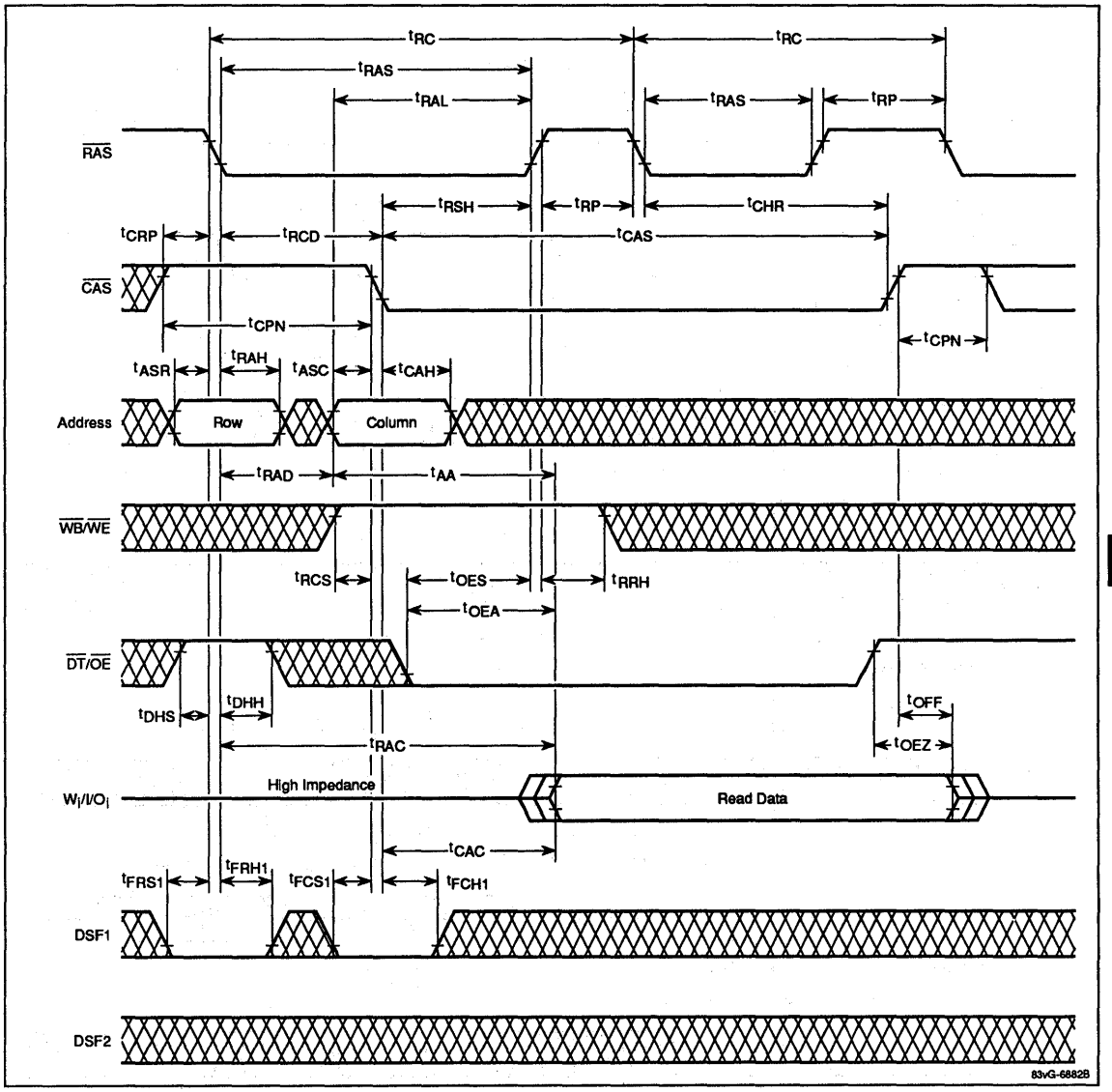
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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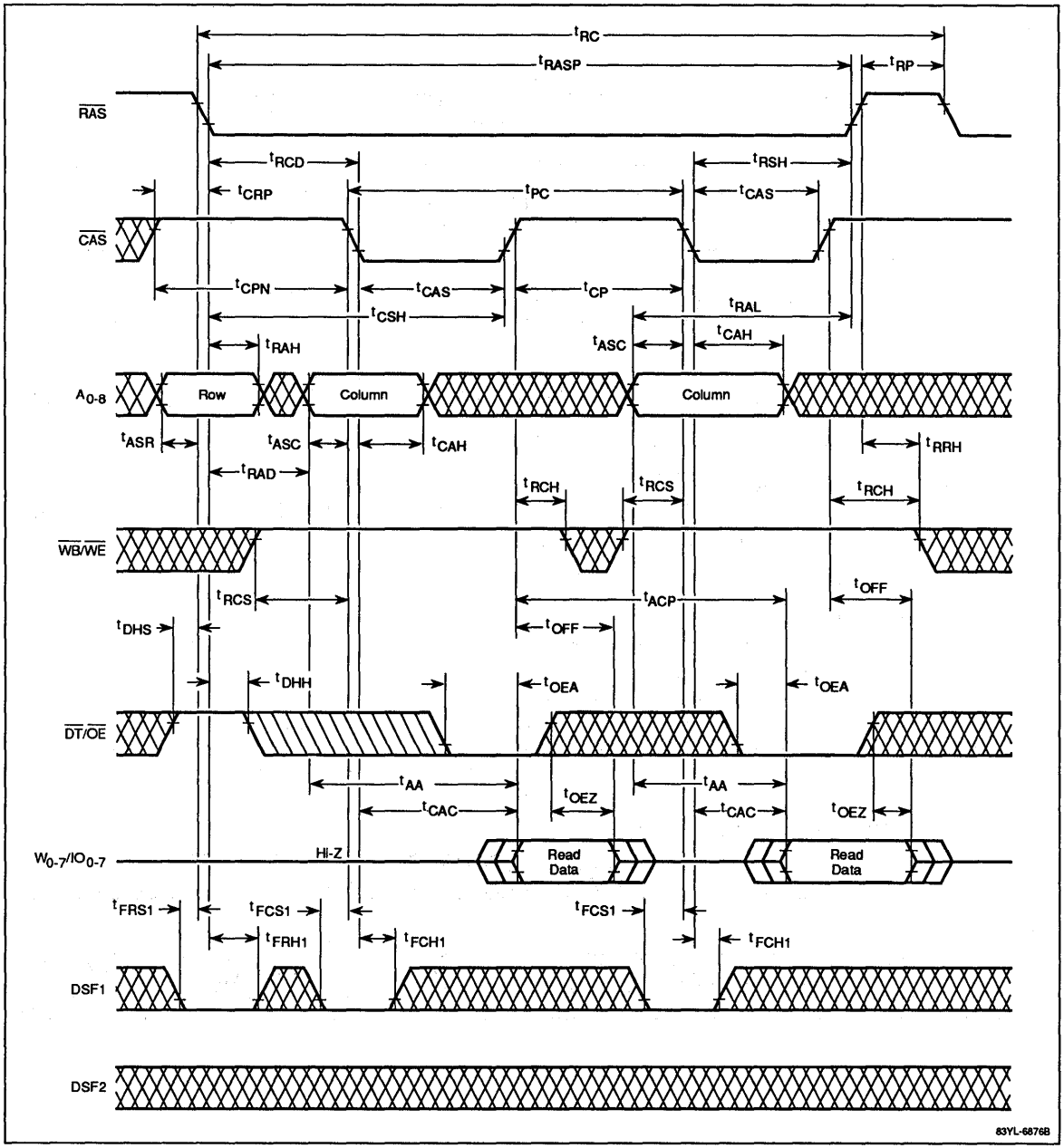
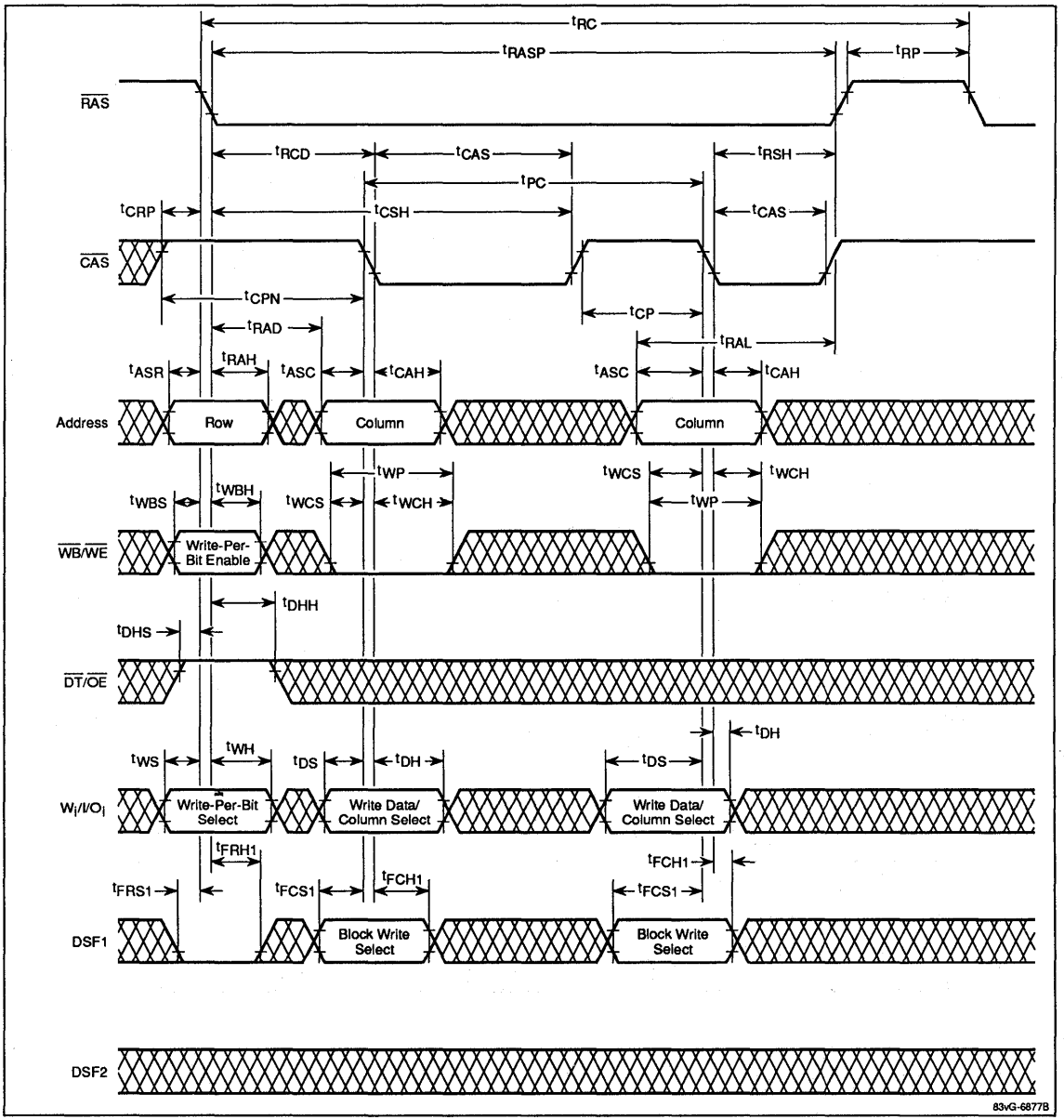
Timing Waveforms (cont)

Fast-Page Read Cycle



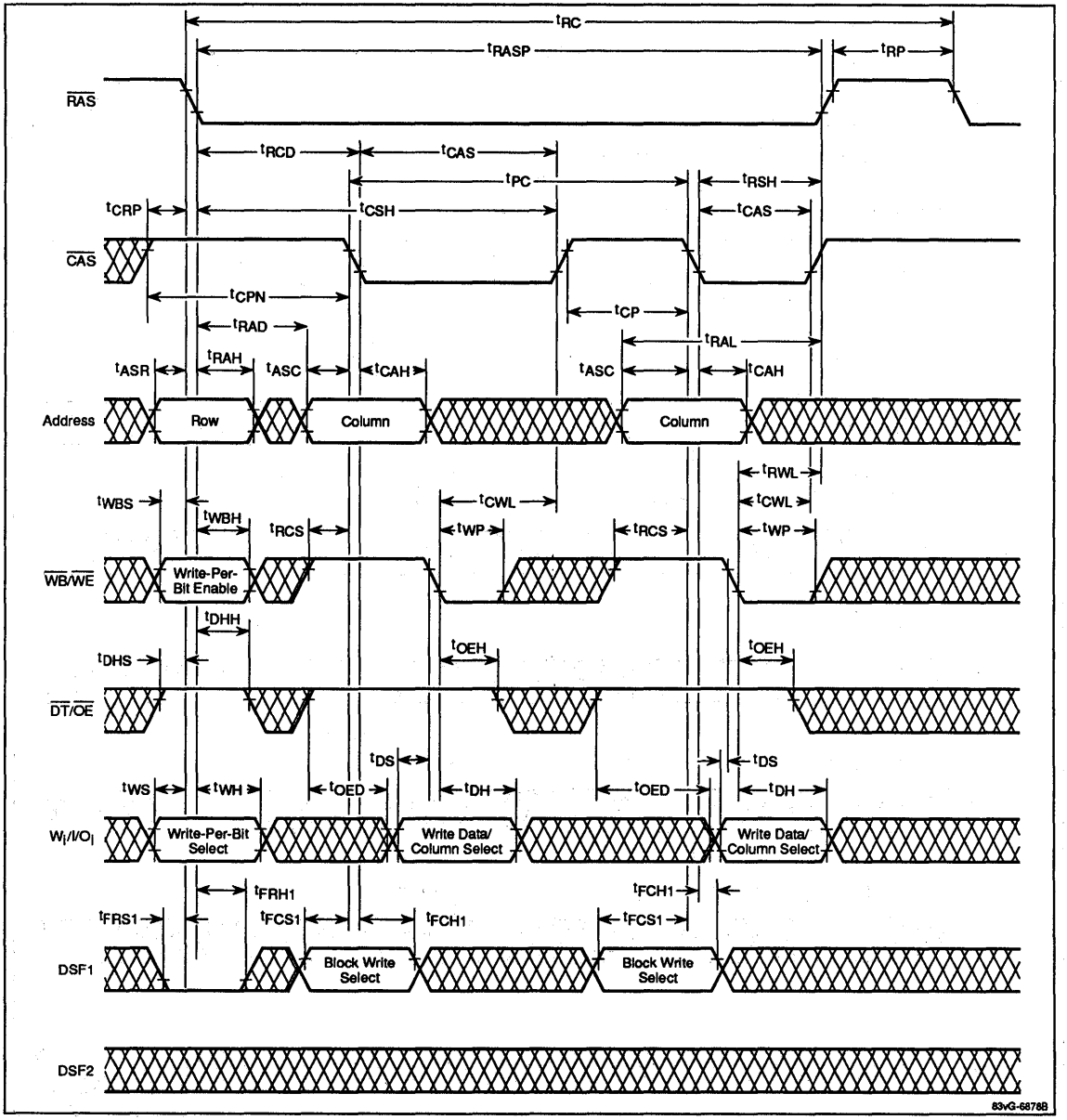
Timing Waveforms (cont)

Fast-Page Early Write Cycle and Fast-Page Early Block Write Cycle



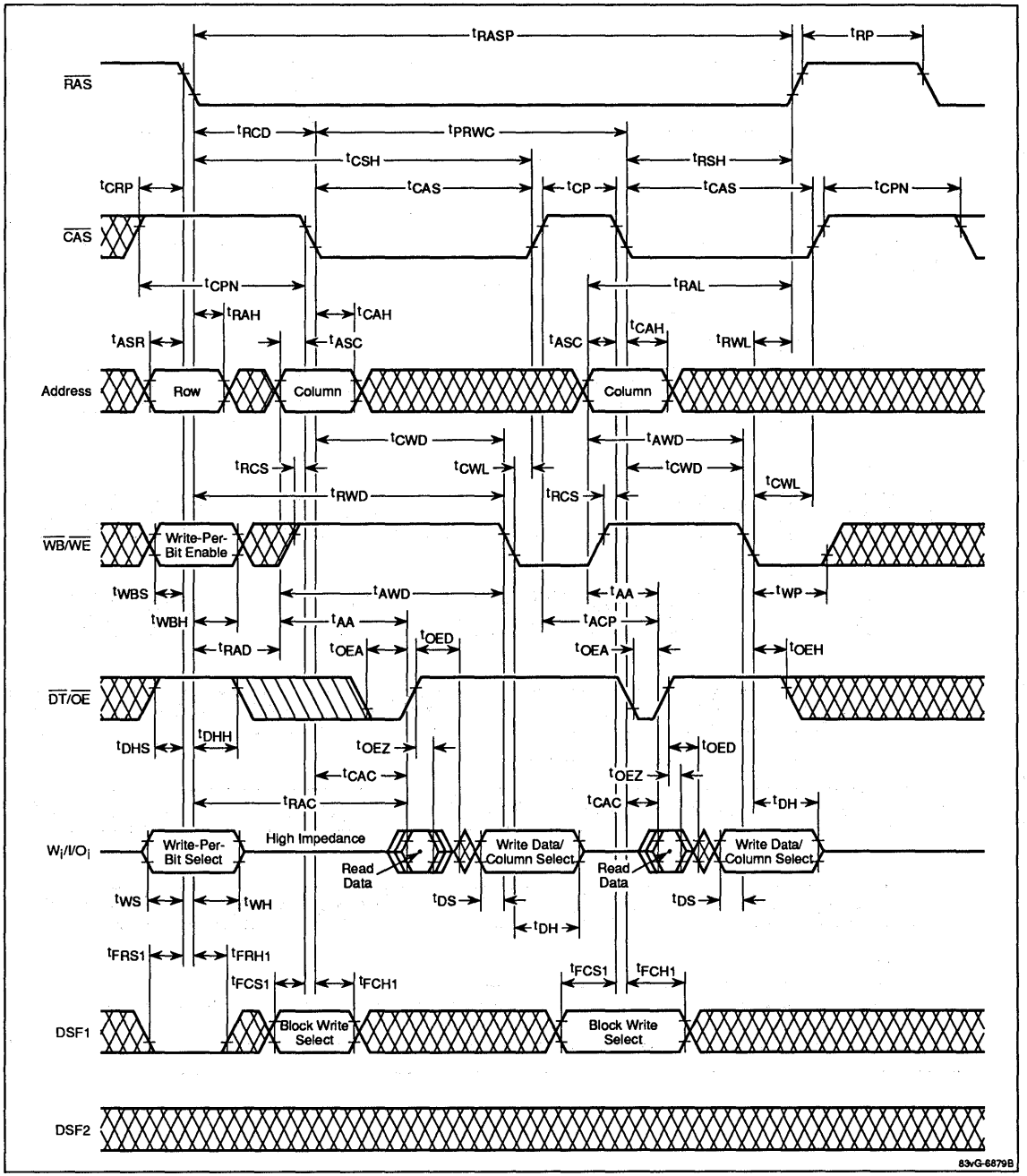
Timing Waveforms (cont)

Fast-Page Late Write Cycle and Fast-Page Late Block Write Cycle



Timing Waveforms (cont)

Fast-Page Read-Modify-Write Cycle



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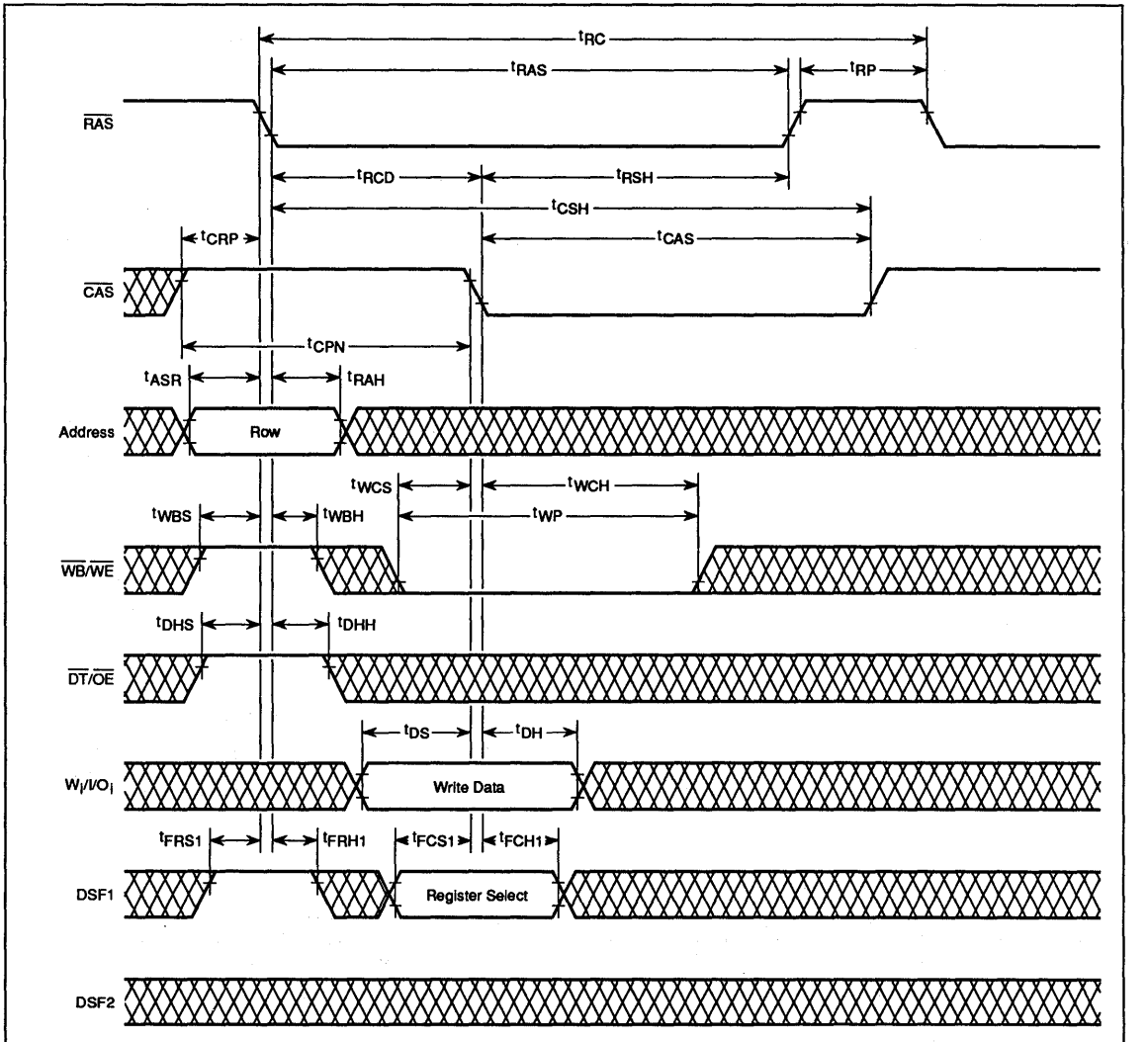
Timing Waveforms (cont)

Color Register Set Cycle



Notes:

[1] Read, late write, RMW, and hidden refresh cycles are also available.

[2] Specifications are exactly the same as read, late write, RMW, and hidden refresh cycles except DSF1 is high at $\overline{RAS}$ leading edge for register set cycles

[3] At $\overline{CAS}$ leading edge, set DSF1 to low level for a write mask register, or set DSF1 to high level for a color register.

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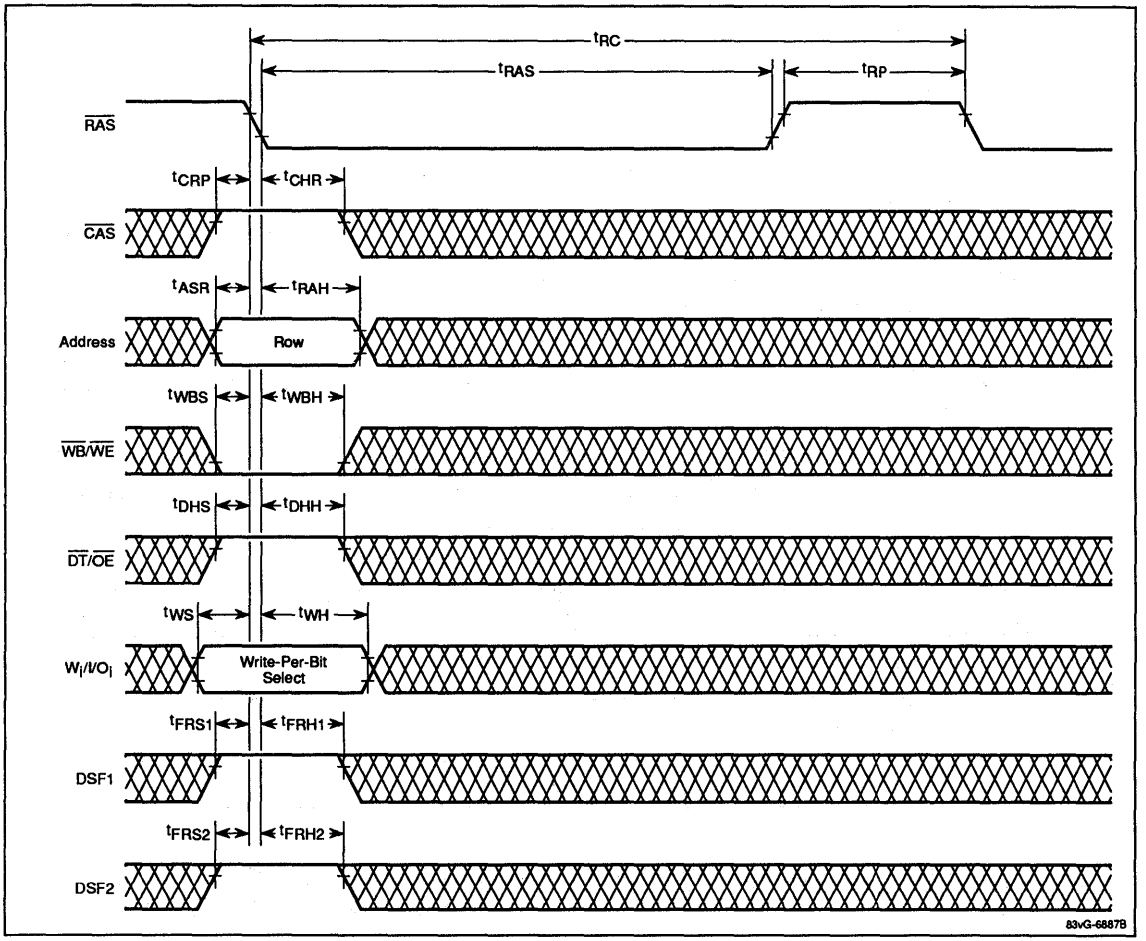
Timing Waveforms (cont)

Flash Write Cycle



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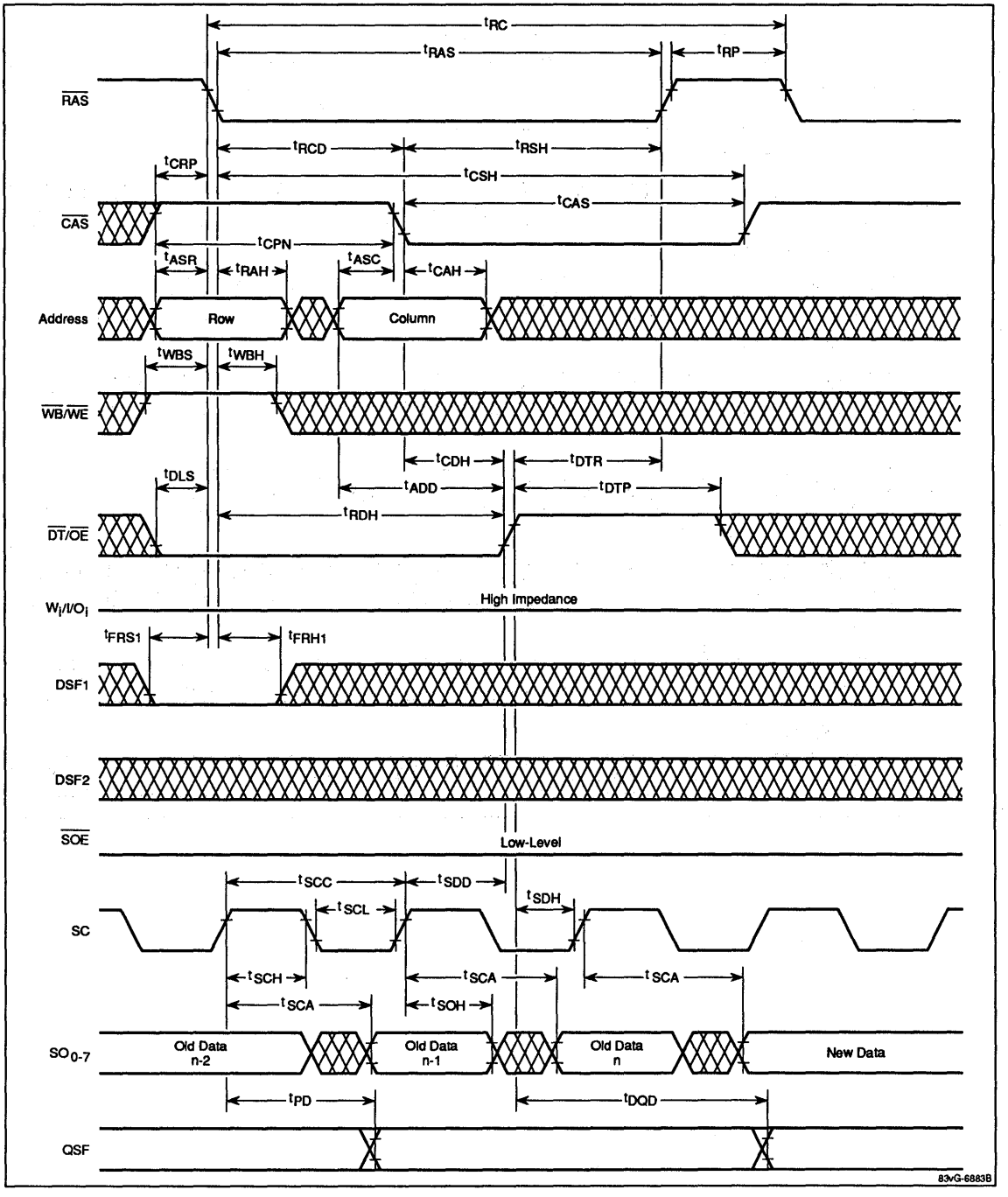
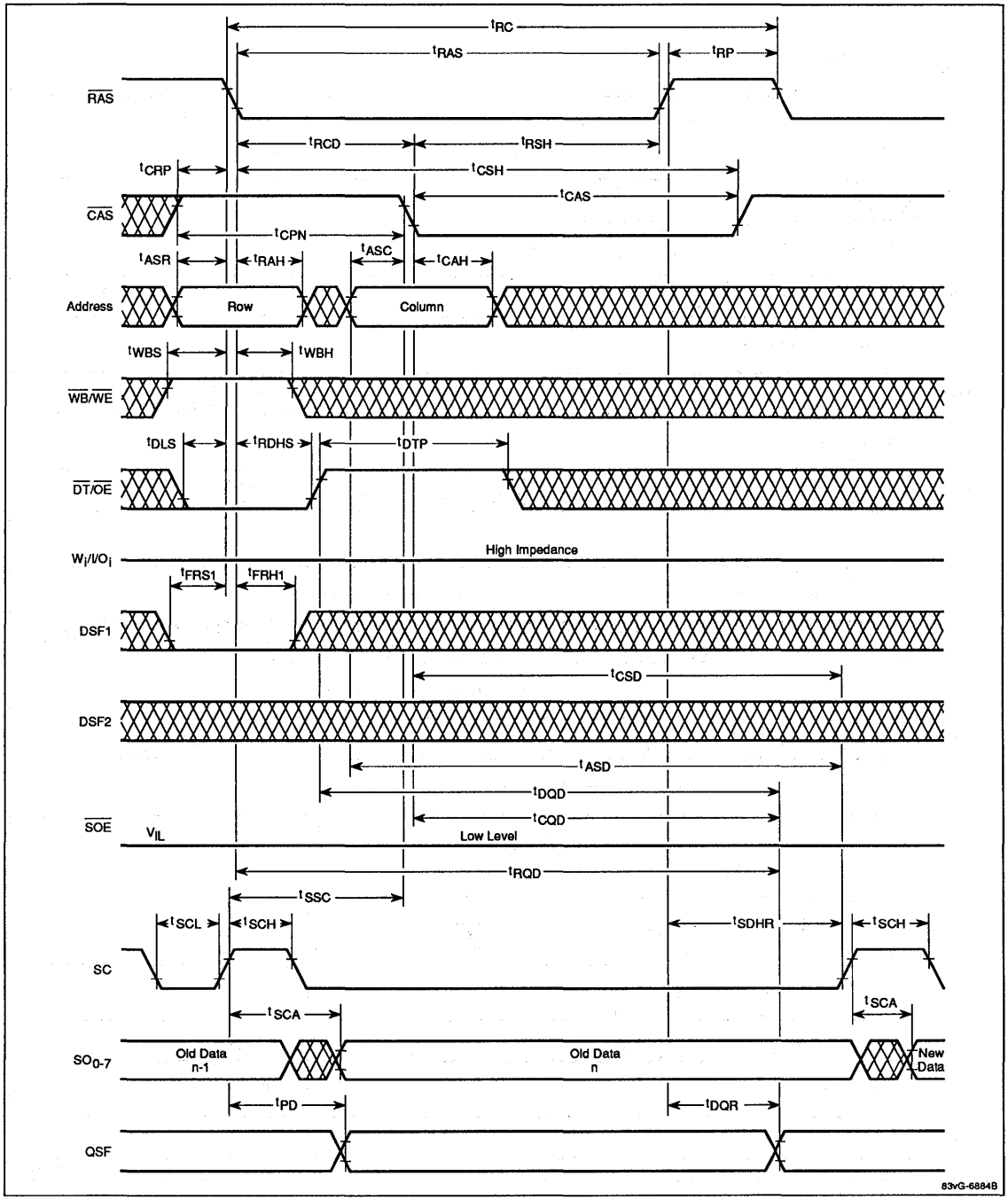
Timing Waveforms (cont)

Data Transfer Cycle with Serial Port Active



Timing Waveforms (cont)

Data Transfer Cycle with Serial Port in Standby



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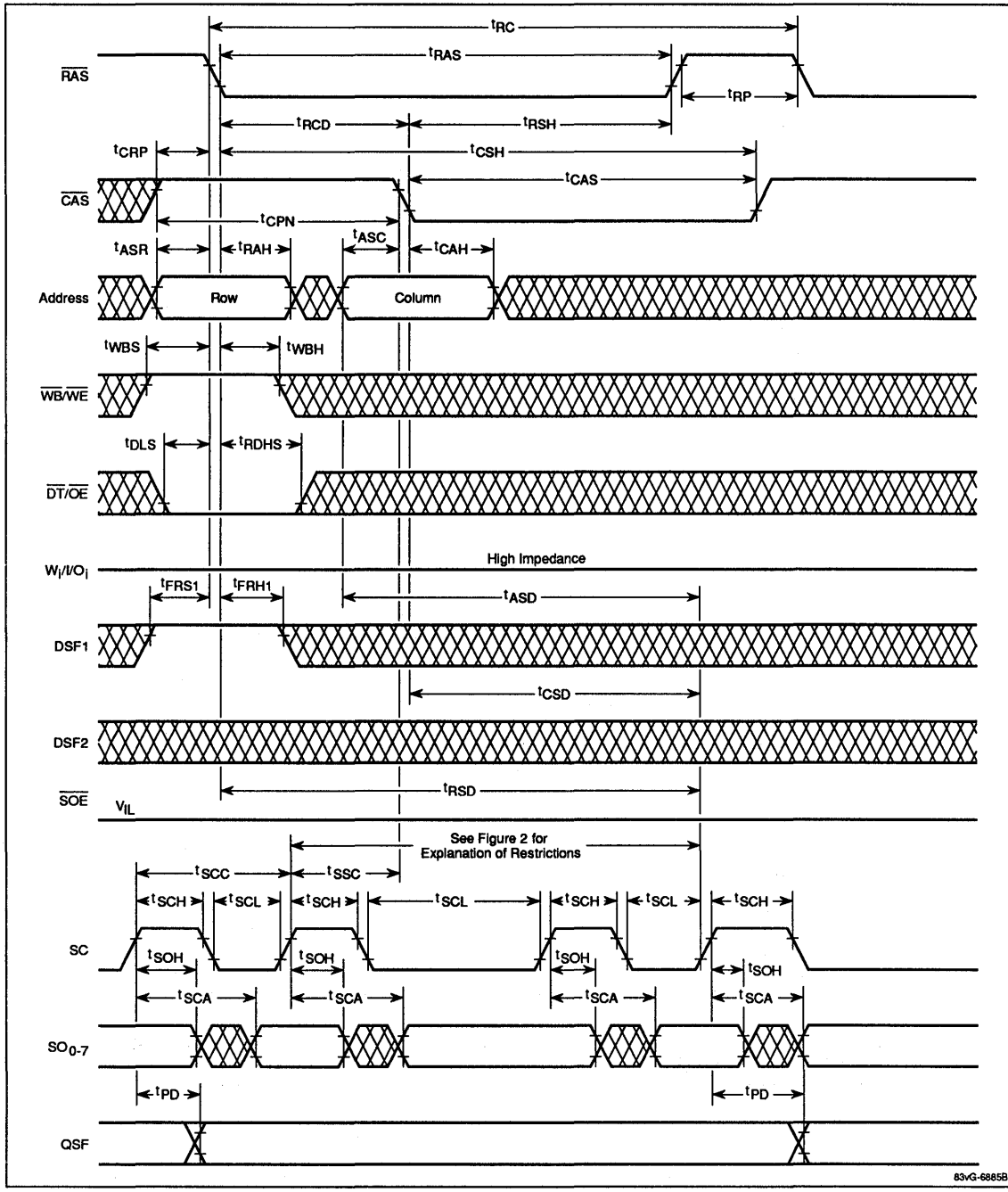
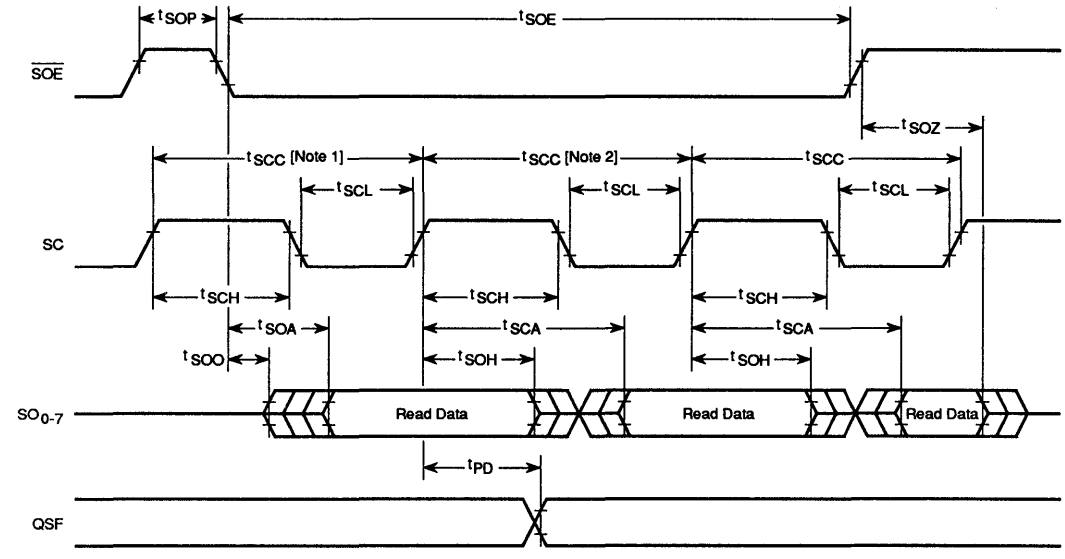
Timing Waveforms (cont)

Split Read Data Transfer Cycle



Timing Waveforms (cont)

Serial Read Cycle



Notes:

[1] Last location of split register (Loc: 127 or 255)

[2] The starting location of newly activated register

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Description

Each of the μPD482234 (fast-page) and μPD482235 (hyper-page) video RAMs has a random access port and a serial read/write port. The serial read/write port is connected to an internal 4096-bit data register through a 512 x 8-bit serial read input/output circuit. The 256K x 8-bit random access port is used by the host CPU to read or write data addressed in any desired order.

A write-per-bit capability allows each of the 8 data bits to be individually selected or masked for a write cycle. Block write cycles can also be used to write the 8 data bits to four consecutive column addresses. Selection and masking of the 8 data bits and four column addresses is provided. A flash write option with write-per-bit control enables data in the color register to be written to a selected row in the random access port.

Both the μPD482234 and μPD482235 feature fully asynchronous dual access between the RAM and serial ports. During a data transfer, the random access port requires a special cycle using a transfer clock; the serial port continues to operate normally. Following the clock transition of a data transfer, serial output data changes from an old line to a new line, and the new starting location is addressable in the data transfer cycle.

An advanced CMOS silicon-gate process using polycide technology and stacked capacitors provides high storage cell density, high performance, and high reliability. Refreshing is by $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 - A_8 during an 8-ms period. Automatic internal refreshing is by hidden refreshing or $\overline{CAS}$ before $\overline{RAS}$ timing, which uses on-chip refresh circuitry. The transfer of a row of data from the storage array to the data register refreshes that row. Data transfer from register to RAM array also refreshes the row.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. The μPD482234 and μPD482235 are available in 40-pin SOJ (400-mil), 40-pin shrink ZIP (475-mil), and 44/40-pin TSOP plastic packages, guaranteed for operation at 0 to +70°C.

Features

- Three functional blocks
  - 256K x 8-bit random access storage array
  - 4096-bit data register
  - 512 x 8-bit serial read/write output circuit
- Random access and serial read/write data ports
- Fast-page operation (μPD482234)
- Hyper-page operation (μPD482235)
- Addressable start of serial read and serial write operation
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - 512 refresh cycles every 8 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page cycles
  - Automatic $\overline{CAS}$ before $\overline{RAS}$ refreshing
  - $\overline{CAS}$-controlled hidden refreshing
  - Persistent and nonpersistent write-per-bit option regarding eight I/O bits
  - Write bit selection multiplexed on IO_0 - IO_7
- Block write option with write-per-bit control and column mask function
- Flash write option with write-per-bit control
- Split serial data register to allow shifting from the active half while simultaneously loading the inactive half
- Boundary jump function on the serial data register
- $\overline{RAS}$-activated data transfer
  - Row data transferred to data register as specified by row address inputs
- Either full or split data register transfer to the row specified by the row address inputs. Split write transfer is always performed from the inactive side of the data register
  - Starting location of following serial read cycle specified by column address inputs
  - Transfer of 4096 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$ or $\overline{RAS}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read/write operation by means of the SC pin
- Serial data input and output on SIO_0 - SIO_7
- Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access

Ordering Information, μPD482234

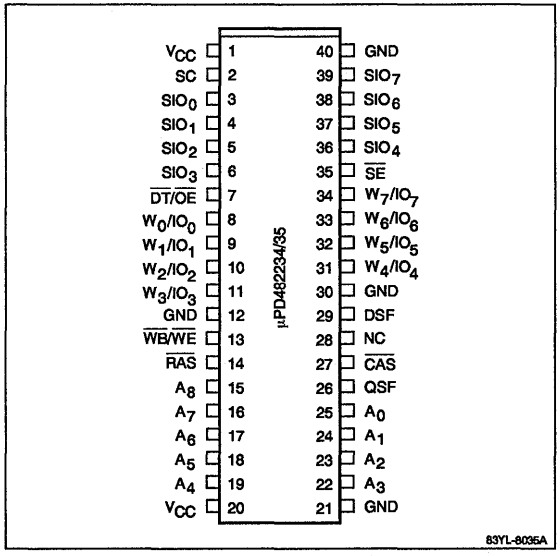
Part Number	$\overline{RAS}$ Access Time (max)	Serial Access Time (max)	Fast-Page Cycle (max)	Package
μPD482234LE-70	70 ns	17 ns	45 ns	40-pin plastic SOJ
LE-80	80 ns	20 ns	50 ns	
μPD482234VF-70	70 ns	17 ns	45 ns	40-pin plastic shrink ZIP
VF-80	80 ns	20 ns	50 ns	
μPD482234G5-70	70 ns	17 ns	45 ns	44/40-pin plastic TSOP (normal pinouts)
G5-80	80 ns	20 ns	50 ns	
μPD482234G5M-70	70 ns	17 ns	45 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-80	80 ns	20 ns	50 ns	

Ordering Information, μPD482235

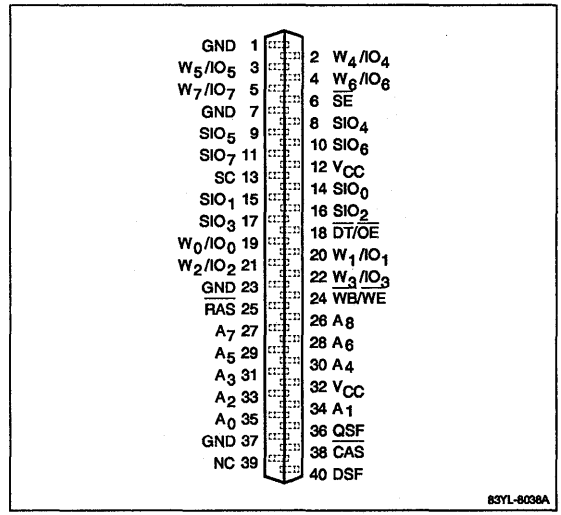
Part Number	$\overline{RAS}$ Access Time (max)	Serial Access Time (max)	Fast-Page Cycle (max)	Package
μPD482235LE-70	70 ns	17 ns	35 ns	40-pin plastic SOJ
LE-80	80 ns	20 ns	40 ns	
μPD482235VF-70	70 ns	17 ns	35 ns	40-pin plastic shrink ZIP
VF-80	80 ns	20 ns	40 ns	
μPD482235G5-70	70 ns	17 ns	35 ns	44/40-pin plastic TSOP (normal pinouts)
G5-80	80 ns	20 ns	40 ns	
μPD482235G5M-70	70 ns	17 ns	35 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-80	80 ns	20 ns	40 ns	

Pin Configurations

40-Pin Plastic SOJ



40-Pin Plastic Shrink ZIP



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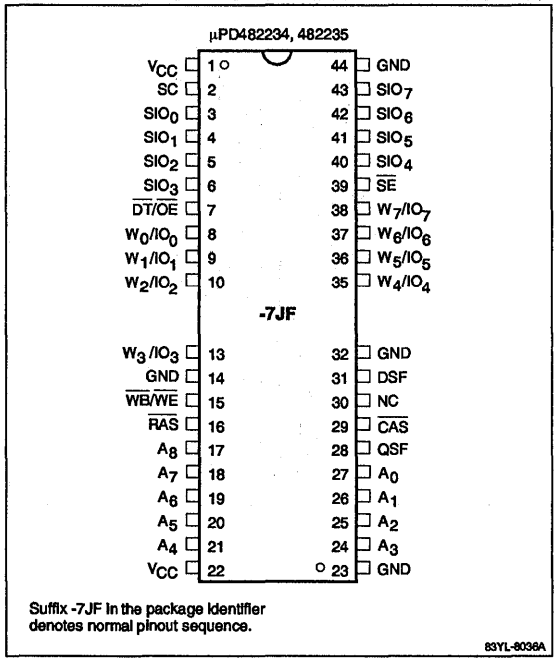
Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
$\overline{CAS}$	Column address strobe
DSF	Special function enable
$\overline{DT/OE}$	Data transfer/Output enable
QSF	Special function output
$\overline{RAS}$	Row address strobe
SC	Serial control
SIO_0 - SIO_7	Serial data inputs and outputs
$\overline{SE}$	Serial enable
W_0/IO_0 - W_7/IO_7	Write-per-bit selects/Data inputs and outputs
$\overline{WB/WE}$	Write-per-bit/Write enable
GND	Ground
V_{CC}	+5-volt ±10% power supply
NC	No connection

Pin Configurations (cont)

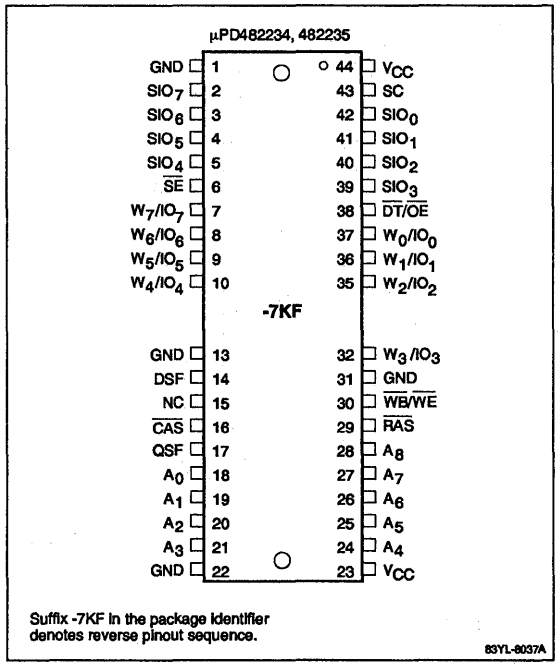
44/40-Pin Plastic TSOP (Normal Pinouts)



Suffix -7JF in the package identifier denotes normal pinout sequence.

83YL-8036A

44/40-Pin Plastic TSOP (Reverse Pinouts)



Suffix -7KF in the package identifier denotes reverse pinout sequence.

83YL-8037A

Pin Functions

A_0-A_8 (Address Inputs). These pins are multiplexed as row and column address inputs. Each of 8 data bits in the random access port corresponds to 262,144 storage cells, which means that 9-bit row addresses and 9-bit column addresses are required to decode one cell location. Row addresses are first used to select one of the 512 possible rows for a read, write, data transfer, or refresh cycle. Column addresses are then used to select the one of 512 possible column decoders for a read or write cycle or the one of 512 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{RAS}$-only refresh cycles.)

W_0/IO_0-W_7/IO_7 (Write-Per-Bit Inputs/Common Data Inputs and Outputs). Each of the 8 mask bits can be individually latched at the falling edge of $\overline{RAS}$ in any write cycle and then updated at the next falling edge of $\overline{RAS}$. In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$ or $\overline{WE}$.

$\overline{RAS}$ (Row Address Strobe). This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 4096 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The 9 row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$, and DSF are simultaneously latched to determine device operation.

$\overline{CAS}$ (Column Address Strobe). This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The 9 column address bits are latched at the falling edge of $\overline{CAS}$.

QSF (Special Function Output). This pin indicates which side of the split register is active. QSF high shows that the upper half (addresses 256 through 511) is active; QSF low indicates the lower half (addresses 0 through 255).

DSF (Special Function Control). At the leading edge of $\overline{RAS}$ and $\overline{CAS}$, the high or low level of DSF is latched to initiate one of the operations shown in table 1.

$\overline{WB/WE}$ (Write-Per-Bit Control/Write Enable). At the falling edge of $\overline{RAS}$, the $\overline{WB/WE}$ and DSF inputs must be low and $\overline{CAS}$ and $\overline{DT/OE}$ high to enable the write-per-bit option. When $\overline{CAS}$, $\overline{DT/OE}$, and DSF are high at the falling edge of $\overline{RAS}$, the level of this signal indicates either a color register set cycle or flash write cycle. A

high $\overline{WB}/\overline{WE}$ can be used at the beginning of a standard write or read cycle.

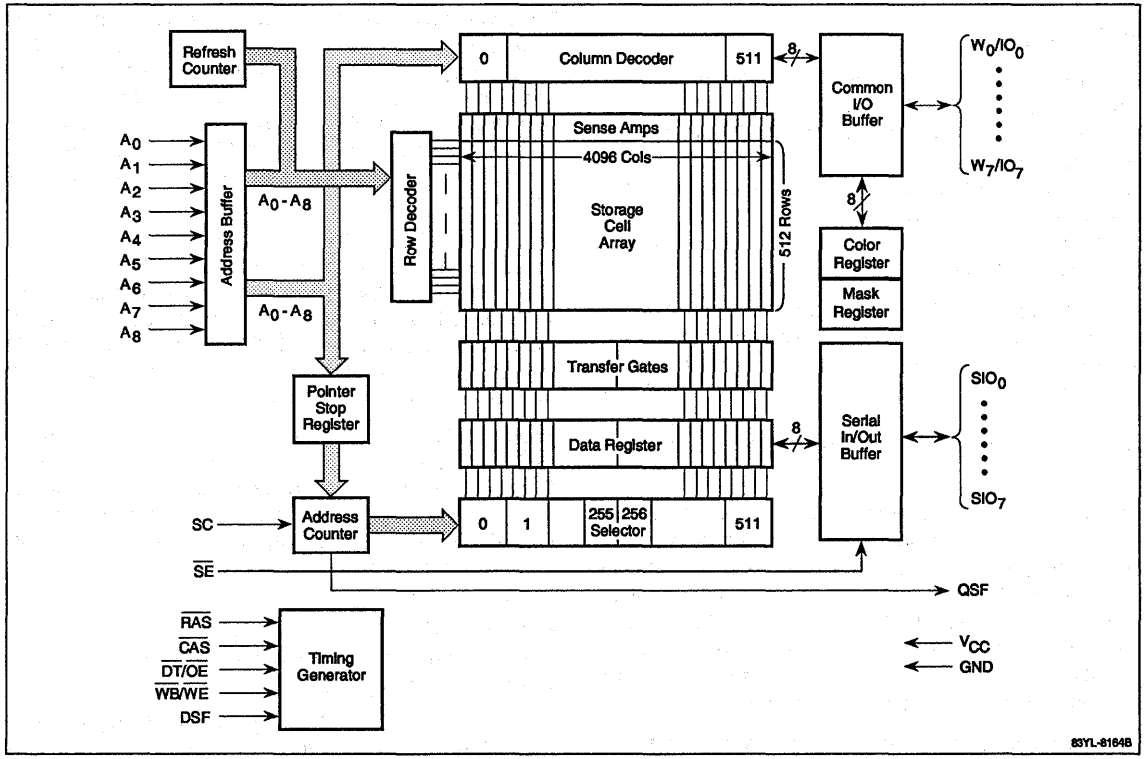
$\overline{DT}/\overline{OE}$ (Data Transfer/Output Enable). At the falling edge of $\overline{RAS}$, $\overline{CAS}$ and $\overline{WB}/\overline{WE}$ high and $\overline{DT}/\overline{OE}$ low initiate a data transfer. $\overline{DT}/\overline{OE}$ high initiates conventional read or write cycles and controls the output buffer in the random access port. The level of DSF determines whether this is a read or split read data transfer.

SIO_0 - SIO_7 (Serial Data Inputs/Outputs). Eight-bit data can be written or read from these pins, and during a serial read, data remains valid until the next SC signal is activated.

SC (Serial Control). Repeatedly activating this signal causes serial read/write cycles (starting from the location specified in the data transfer cycle) to be executed within the 4096 bits in the data register. The rising edge of SC activates either a serial read or write operation. In the serial read mode, 8 of the 4096 data bits are transferred to eight serial data buses, respectively, and read out. In the serial write operation, input data is latched on the rising edge of SC. Whenever SC is low, the serial port is in standby.

$\overline{SE}$ (Serial Enable). This signal controls the serial input/output buffer.

Block Diagram



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OPERATION

The μPD482234 and μPD482235 both incorporate a random access port and a serial read or write port. The random access port executes standard read and write cycles as well as data transfer, block write, and flash write cycles, all of which are based on conventional $\overline{RAS}/\overline{CAS}$ timing.

In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to its corresponding register location. The serial read port shows the contents of the data register in serial order. The random access and serial ports can operate asynchronously when split read or split write operation is used.

Addressing

The storage array is arranged in a 512-row by 4096-column matrix, whereby each of 8 data bits in the random access port corresponds to 262,144 storage cells, and 18 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 - A_8 and latched onto the chip by $\overline{RAS}$. Nine column address bits then are set up on pins A_0 - A_8 and latched onto the chip by $\overline{CAS}$.

All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 4096 cells on the selected row are sensed simultaneously, and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through one of 512 column decoders, eight storage cells on the row are connected to eight data buses, respectively. In a data transfer cycle, 9 row address bits are used to select one of the 512 possible rows involved in the transfer of data to the data register. Nine column address bits are then used to select the one of 512 possible serial decoders that corresponds to the starting location of the next serial read cycle.

In the serial read port, when SC is activated, 8 data bits in the 4096-bit data register are transferred to eight serial data buses and read out. Activating SC repeatedly causes serial read or serial write cycles (starting from the location specified in the previous data transfer cycle) to be executed within the 4096 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following are multiplexed: $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, W_n/IO_n (n = 0 through 7).

The $\overline{OE}$, $\overline{WE}$, and IO_n functions represent standard operations; $\overline{DT}$, $\overline{WB}$, and W_n are special inputs to be applied in the same way as row address inputs with setup and hold times referenced to the negative transition of $\overline{RAS}$.

The level of $\overline{DT}$ determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_n defines data bits to be written with the write-per-bit option. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD482234/5 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 4096-bit register from the corresponding 4096 digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 4096 transfer gates and transfer data from one of the rows to the register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining $(\overline{WB}/)\overline{WE}$ while $\overline{CAS}$ is active. The $(W_n/)IO_n$ pin remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance (μPD482234 only). See explanation of "Extended Data Output."

Write Cycle. A write cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low during the $\overline{RAS}/\overline{CAS}$ cycle. The falling

edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes the data on (W_n/)IO_n into the on-chip data latch. To make use of the write-per-bit option, $\overline{WB}$($\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case, write data bits can be specified by keeping W_n(IO_n) high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

Write-per-Bit-Cycle. A write-per-bit-cycle uses an I/O masking function to allow the system designer the flexibility of writing or not writing any combinations of W_0/IO_0 through W_7/IO_7. Two types of masking are possible: (1) new mask or the non-persistent mask that requires the user to provide the mask data each cycle and (2) old mask or the persistent mask. With the persistent mask option, an LMR or load mask register cycle is performed and the mask data is used during write, block write, and flash write cycles.

Early Write Cycle. An early write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low before $\overline{CAS}$ falls. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, ($\overline{DT}$/)$\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$, but otherwise ($\overline{DT}$/)$\overline{OE}$ does not affect any circuit operation while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. This cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. (W_n/)IO_n shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_n/)IO_n returns to high impedance when ($\overline{DT}$/)$\overline{OE}$ goes high. The data to be written is strobed by ($\overline{WB}$/)$\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of ($\overline{DT}$/)$\overline{OE}$, which can be activated just after ($\overline{WB}$/)$\overline{WE}$ falls, even when ($\overline{WB}$/)$\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 - A_8) will refresh all storage cells. Any cycle executed in the random access port (i.e., read, write, refresh, data transfer, color register set, flash write, or block write) refreshes the 2048 bits selected by the $\overline{RAS}$ addresses or by the on-chip address counter.

$\overline{RAS}$-Only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes all cells in one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep (W_n/)IO_n in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (CBRN). This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle. CBRS and CBR also performed internal refresh, stopping column control.

Hidden Refresh Cycle. This cycle is executed after a read cycle without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed causes data to be transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. In fast-page operation, read, write, and read-write/read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the next fast-page write cycle.

During a fast-page read cycle, the (W_n)/IO_n data pin (n = 0 - 7) remains in a state of high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be the longest of the following intervals.

- t_{ACP}
- $t_{CP} + t_T + t_{CAC}$
- $\overline{CAS}$ high to column address delay + t_{AA}

Glossary of Special Functions

Table 1 is a truth table for implementing the functions described below.

Masked Write Cycle With New Mask (RWM new mask). When the write-per-bit function is enabled as shown below, mask data on the W_n/IO_n pins is latched by $\overline{RAS}$ and loaded directly into the write mask register. A masked write cycle is then executed using $\overline{CAS}$ or $\overline{WB}/\overline{WE}$ to strobe the W_n/IO_n data into the on-chip data latch.

Mask Register Data	Action
1	Write
0	Do not write

Load Mask Register Cycle (LMR). In this cycle, data on W_n/IO_n is written to an 8-bit write mask register, where it is retained and used by subsequent masked write and masked block write cycles.

Masked Write Cycle With Old Mask (RWM old mask). This write-per-bit cycle, commonly referred to as a persistent mask write cycle, uses the mask data previously set by the last load mask register cycle.

Table 1. μPD482234/5 Function Truth Table (JEDEC Standard) for Random Access Port

Mnemonic Code	$\overline{RAS}$				$\overline{CAS}$	Address		DQ_n Input		Write Mask	Register		Function
	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	DSF	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}/\overline{WE}$		WM	Color	
CBRS (Notes 1, 3)	0	x	0	1	—	STOP (Note 4)	—	x	—	—	—	—	CBR refresh/STOP (no reset)
CBRN (Note 1)	0	x	1	1	—	x	—	x	—	—	—	—	CBR refresh (no reset)
CBR (Note 1)	0	x	1	0	—	x	—	x	—	—	—	—	CBR refresh (option reset)
MWT	1	0	0	0	x	Row	Tap	WM1 (Note 5)	—	Yes	Load/ Use	—	Masked write transfer (new/old)
MSWT	1	0	0	1	x	Row	Tap	WM1 (Note 5)	—	Yes	Load/ Use	—	Masked split write transfer (new/old)
RT	1	0	1	0	x	Row	Tap	x	—	—	—	—	Read transfer
SRT	1	0	1	1	x	Row	Tap	x	—	—	—	—	Split read transfer
RWM	1	1	0	0	0	Row	Col	WM1 (Note 5)	Data	Yes	Load/ Use	—	Read write (new/old mask)
BWM	1	1	0	0	1	Row	Col	WM1 (Note 5)	Col	Yes	Load/ Use	Use	Block write (new/old mask)
FWM	1	1	0	1	x	Row	x	WM1 (Note 5)	—	Yes	Load/ Use	Use	Flash write (new/old mask)
RW	1	1	1	0	0	Row	Col	x	Data	No	—	—	Read write (no mask)
BW	1	1	1	0	1	Row	Col	x	Col	No	—	Use	Block write (no mask)
LMR (Note 2)	1	1	1	1	0	Row	x	x	WM1	0	Load	—	Load (old) mask register set cycle
LCR	1	1	1	1	1	Row	x	x	Color	0	—	Load	Load color register

x = Don't care

— = Not applicable

$\overline{RAS}$ only refresh does not reset STOP or LMR functions.

Notes:

(1) CBRS, CBRN, and CBR all perform $\overline{CAS}$ before $\overline{RAS}$ refresh cycles. CBR is used to reset all options and either CBRS or CBRN is used to continue to refresh the RAM without clearing any of the options.

(2) After LMR, RWM and BWM use old mask. (CBR resets to new mask. Use CBRS or CBRN to perform $\overline{CAS}$ before $\overline{RAS}$ refresh while using old mask.)

(3) With CBRS, all SAM operations use STOP register.

(4) STOP defines the column on which shift out moves to the other half of the SAM.

(5) After LMR, WM1 is only changed by LMR (CBR resets).

Table 2. Block Write Addresses

Column Select By IO Data	Result	Corresponding Column Address
$IO_3 = 1$	Write	$A_1 = 1, A_0 = 1$
$IO_3 = 0$	No write	
$IO_2 = 1$	Write	$A_1 = 1, A_0 = 0$
$IO_2 = 0$	No write	
$IO_1 = 1$	Write	$A_1 = 0, A_0 = 1$
$IO_1 = 0$	No write	
$IO_0 = 1$	Write	$A_1 = 0, A_0 = 0$
$IO_0 = 0$	No write	

Notes:

(1) Data on IO_7 - IO_4 are don't care at the falling edge of $\overline{CAS}$.

Flash Write Cycle (FWM old mask). This flash write cycle is the same as the FWM new mask except that the bit mask inputs are supplied by the mask register set by the previous LMR cycle.

Flash Write Cycle (FWM new mask). A flash write cycle can clear or set each of the eight 512-bit data sets on the selected one of 512 possible rows according to data stored in the previously set color register. Bit mask inputs are latched as $\overline{RAS}$ falls. This cycle is useful in graphics processing applications when the screen should be cleared or set to some uniform value as quickly as possible.

Load Color Register Cycle (LCR). This cycle is executed in the same fashion as a conventional read or write cycle, with a read or write cycle available to the color register under the control of $\overline{WE}$. In read operation, color register data is read on the common W_n/IO_n pins. In write operation, common W_n/IO_n data can be written into the color register. $\overline{RAS}$-only refreshing is internally performed on the row selected by A_0 - A_8. This setup cycle precedes the first flash write or block write cycle supplying the 8 write data bits.

Block Write Cycle (BW no mask). In a block write cycle, A_1 and A_0 are ignored. IO_0 - IO_3 are used to select one or a combination of four column addresses for writing in an early write, late write, page early write, or page late write cycle. See table 2.

Block write data is previously stored in the color register using a set color register cycle. Column select data is latched by the W_n/IO_n pins at the falling edge of $\overline{CAS}$ or $\overline{WE}$. Block write cycles are useful for clearing windows and for accelerating polygon fill operations.

Block Write Cycle (BWM new mask). This cycle allows for W_0/IO_0 - W_7/IO_7 masking during a block write cycle. The masking function is identical to a standard masked write cycle with new mask, except that four consecutive columns are written.

Block Write Cycle (BWM old mask). This cycle uses the masked data previously set by the last LMR cycle to write four consecutive columns.

Read Data Transfer Cycle (RT). In a full-row read data transfer cycle, one of the possible 512 rows, as well as the starting location of the following serial read cycle, is defined by row and column address inputs. The low-to-high transition of $\overline{DT}/(\overline{OE})$ causes the 4096 bits of cell data to be transferred to the serial data register.

Split Read Transfer Cycle. This cycle is a half-row data transfer in which one of the 512 rows, the starting location of the following serial read cycle, and either of the split registers are specified by the address inputs. On-chip control circuitry causes the previously specified half-row to be transferred to the selected upper or lower split register.

Hyper-Page Mode With Extended Data Output. In operation, hyper-page mode is the same as standard fast-page mode. As in fast-page mode, a faster data rate is possible by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining $\overline{RAS}$ low while $\overline{CAS}$ cycles are executed causes data to be transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. During hyper-page mode, read, write, and read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the successive fast-page write cycle.

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Extended Data Output

The introduction of the extended data output feature causes the output data to remain valid even after $\overline{CAS}$ goes high. This is made possible by the addition of a transparent latch to the data amplifier circuit. Extended data output eliminates the t_{OFF} parameter. The resulting longer data valid time allows for the speedup of the fast-page cycle time. Fast-page mode applications that try to run at minimum cycle times find that timing skews and propagation delays make the data valid time so narrow that reliable sampling is impossible. Extended data output is intended to solve this problem and permit faster page-mode cycle times, hence the term "hyper-page mode."

Speed Grade	Fast-Page Mode	Hyper-Page Mode
-70	t_{PC} = 45 ns	t_{HPC} = 35 ns

In this operation, data pins W_0/IO_0 through W_7/IO_7 remain in the low-impedance state and the valid data appears after the device access time. Device access time, t_{PAC} (page-mode access time), is the longest of the following intervals:

- t_{ACP}
- t_{AA}
- t_{CAC}
- t_{AWE}†
- t_{ACE}†

† Page write to page read switch or continuous page RMW cycles.

Serial Read Port

The serial read port is used to serially read the previously loaded contents of the data register starting from a specified location. Other graphics buffers require very tight timing to synchronize this port with the random access port, but the μPD482234/5 has been designed with a split register to eliminate the need for synchronized timing between the two ports.

Read Data Transfer (RT). A data transfer is executed to both split registers, and the serial port direction is switched to the serial read mode. During this cycle, the row address selects the row, and the column address sets the start address of the next serial read sequence. The transfer trigger is $\overline{DT}/\overline{OE}$ or $\overline{RAS}$ low-to-high transition, whichever occurs first. The read data transfer cycle disables the boundary jump function in the serial port but keeps the stop register value. QSF will change depending on the column address specified during the RT cycle.

Split Read Data Transfer (SRT). A review of the split register architecture shows that the lower register (addresses 0 - 255) and upper register (addresses 256 - 511) are selected by *the most significant bit of the column addresses (A_8)*. Bit A_8 must be specified low level for transfer to the lower register and high level for transfer to the upper register. With the serial port split in half, data transfers can be executed to the inactive side while SC clocks are input to access data from the active side. This sequence allows for a longer time window to perform the transfer, i.e., 256 x t_{SCC}. Column address bits A_0 - A_7 are latched on-chip to provide the tap address pointer for each split register.

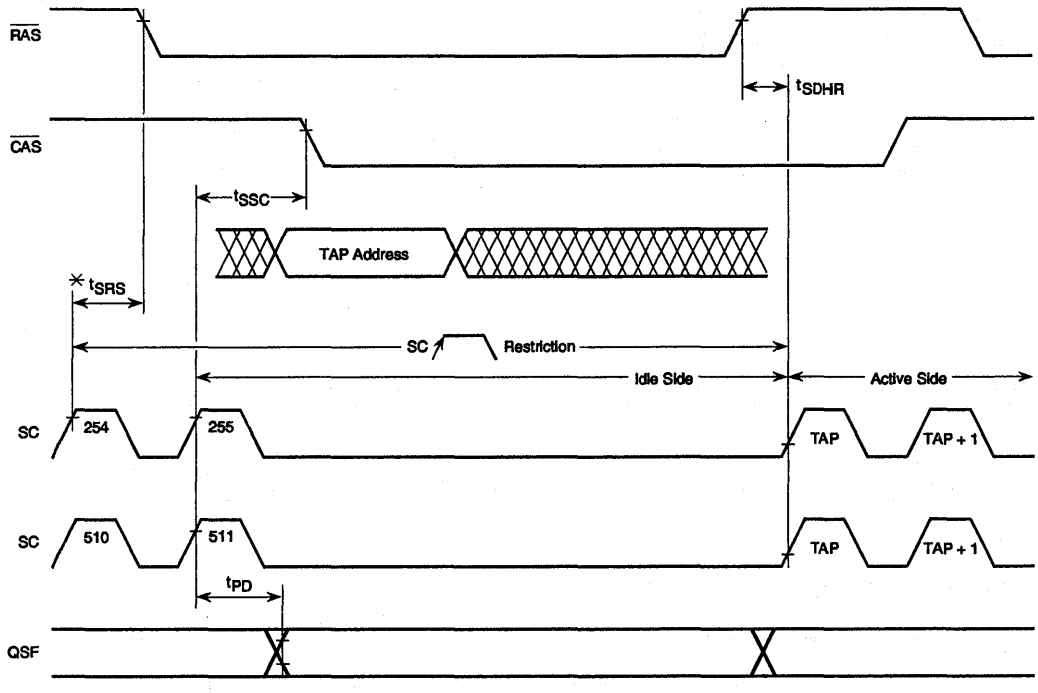
During a split read data transfer cycle, a half row of memory data is transferred to one of the split half serial registers. The row addresses select the half row to be transferred and the column addresses (A_7 - A_0) set the tap or pointer for the start of the serial read operation and boundary jump operation. A split read transfer does not change the direction of the serial port I/O.

Data in the data register is clocked serially by SC, starting from the first specified address of either register. After the last specified address has been transferred, QSF changes its level at the next rising edge of SC, and serial data transfer switches to the other (formerly inactive) register. Serial data output is maintained until the next SC clock.

SC clocks at the transition point; that is, the end of one half and the beginning of the new half of the split registers are restricted. Rising edges of the SC clock are not allowed for the last serial address (either 255 or 511) of the active register and for the first address (any address depending on current address pointer) of the next active register (figure 1).

$\overline{SE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD482234/5 on the same bus and has no effect on SC. When $\overline{SE}$ is low, SO_n is disabled and in a state of high impedance. During serial write, the $\overline{SE}$ level is latched by SC rising edge to control the serial input buffer. SC continues to increment serial addresses independent of $\overline{SE}$.

Figure 1. Restrictions on Rising Edges of SC for Split Read and Split Write Data Transfer Cycles



Notes:

[1] For split register transfers, there is a restriction on the SC clocks at the transition point from the end of one half to the beginning of the other half split register. Rising edges of the SC clock for the last serial address of the idle split register (255 or 511) and the first tap address are not allowed.

[2] The restrictions apply to split read transfers, split write transfers, split read transfers with stopping column control, full read data transfers and write data transfers.

* The same restrictions for split write transfers except t_{SRS} apply.

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Serial Port Write Operation

Serial writes can also be performed to the serial data register starting at the location (column address) specified by the previous write or split write transfer cycle. After writing to the serial register, the contents can be transferred to the specified row address in the DRAM array. This operation provides a fast screen clear function. Both a split write and full register write transfer are possible. Refer to figure 2.

Masked Write Data Transfer (MWT). The MWT cycle, under write-per-bit control, transfers the contents of both halves of the serial data register to the selected row in the DRAM array. Row addresses are used to select the row to receive the data and the column addresses set the start location of the following serial write operation. If the previous serial port operation was a serial read, then an MWT cycle is required to change the direction of the serial I/O from serial read to serial write. During all MWT cycles, SC clocks are not allowed and system timing must meet the conditions of t_{SRS} and t_{SDHR}.

In this type of transfer, the contents of the DRAM will be changed unless the masking or write-per-bit function is employed. Keeping $\overline{WE}$ and all eight I/Os low as $\overline{RAS}$ falls will perform a write-per-bit mask and inhibit data from being transferred to the RAM array. The MWT cycle disables the boundary jump function of the serial port but does not reset the stop register value. QSF will change in accordance with the value set by the column address specified during the MWT cycle.

Masked Split Write Data Transfer (MSWT). A data transfer cycle is performed from the selected split-half serial register to the specified half row in the DRAM array. Data from the serial port is always transferred from the inactive side (A_8 is a "don't care") of the split register to the corresponding half row in the RAM array. The direction of the serial port I/O (serial read or write) remains unchanged. The same write-per-bit masking function is used as described in the MWT cycle.

QSF Special Function Output

This pin outputs a signal synchronized with the SC clock and indicating which half of the serial data register is active. A high level of QSF indicates that an upper half address (256 - 511) will be read from or written to by the next SC clock. Read and write addresses 0 - 255 are indicated by a low QSF level. QSF changes on the rising edge of the SC clock for serial addresses 255, 511, and BJX (boundary jump).

Advanced Serial Write Operation

If the design objective is to write data into selected blocks without disturbing the background data, the sequence of operations in figure 3 should be followed.

Figure 2. Example of Split Read and Split Write Data Transfers (Sheet 1 of 3)

		①	②	③	③	④	⑤	⑤	⑥	⑦
Power up	8 RAS Cycles	CBRS or CBR	Read Data Transfer	Split Read Data Xfer	Split Read Data Xfer	Masked Write Data Transfer	Split Write Data Transfers	Split Write Data Transfers	Read Data Transfer	Split Read Data Xfer

Notes:

(1) A CBRS or CBR is required to set up the serial register boundaries. A CBR alone or a CBRS with A_7 - A_0 set to (11111111) sets the serial register to 255 and 511 splits.

(2) A full line data transfer is required before a sequence of split read or write transfers.

(3) Rising edges of SC clocks are not allowed in this restricted window for serial addresses 255 and 511. The restricting parameters are t_{SSC} and t_{SDHR}.

(4) No SC clocks are allowed during the period specified by t_{SRS} and t_{SDHR}.

(5) Rising edges of SC clocks are not allowed in this restricted window for serial addresses 255 and 511. The restricting parameters are t_{SRS} and t_{SDHR}.

(6) No SC clocks are allowed during the period specified by t_{SSC} and t_{SDHR}.

(7) The numbers at SIO_n indicate the serial read or write address.

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Figure 2. Example of Split Read and Split Write Data Transfers (Sheet 2 of 3)

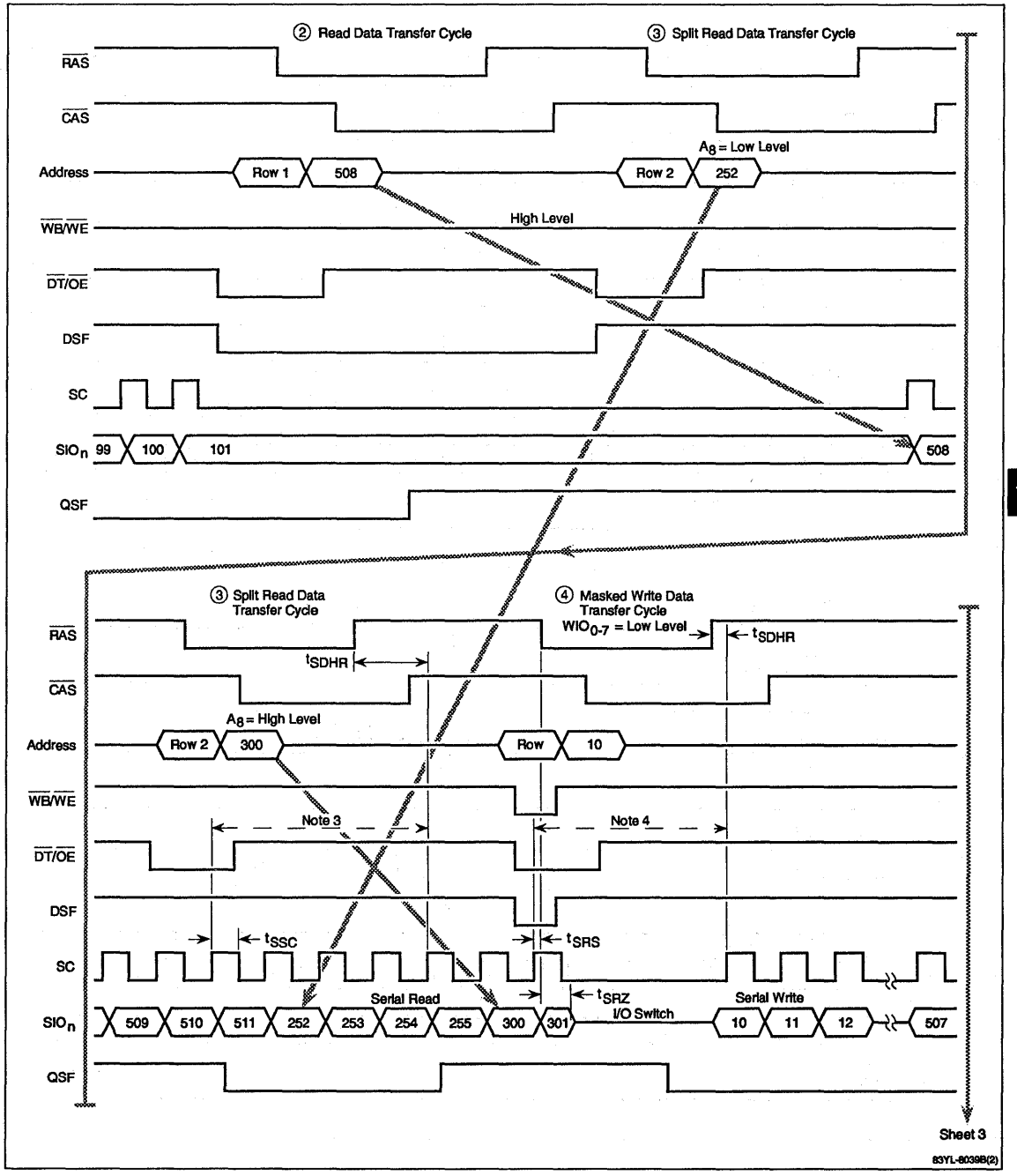

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Figure 2. Example of Split Read and Split Write Data Transfers (Sheet 3 of 3)

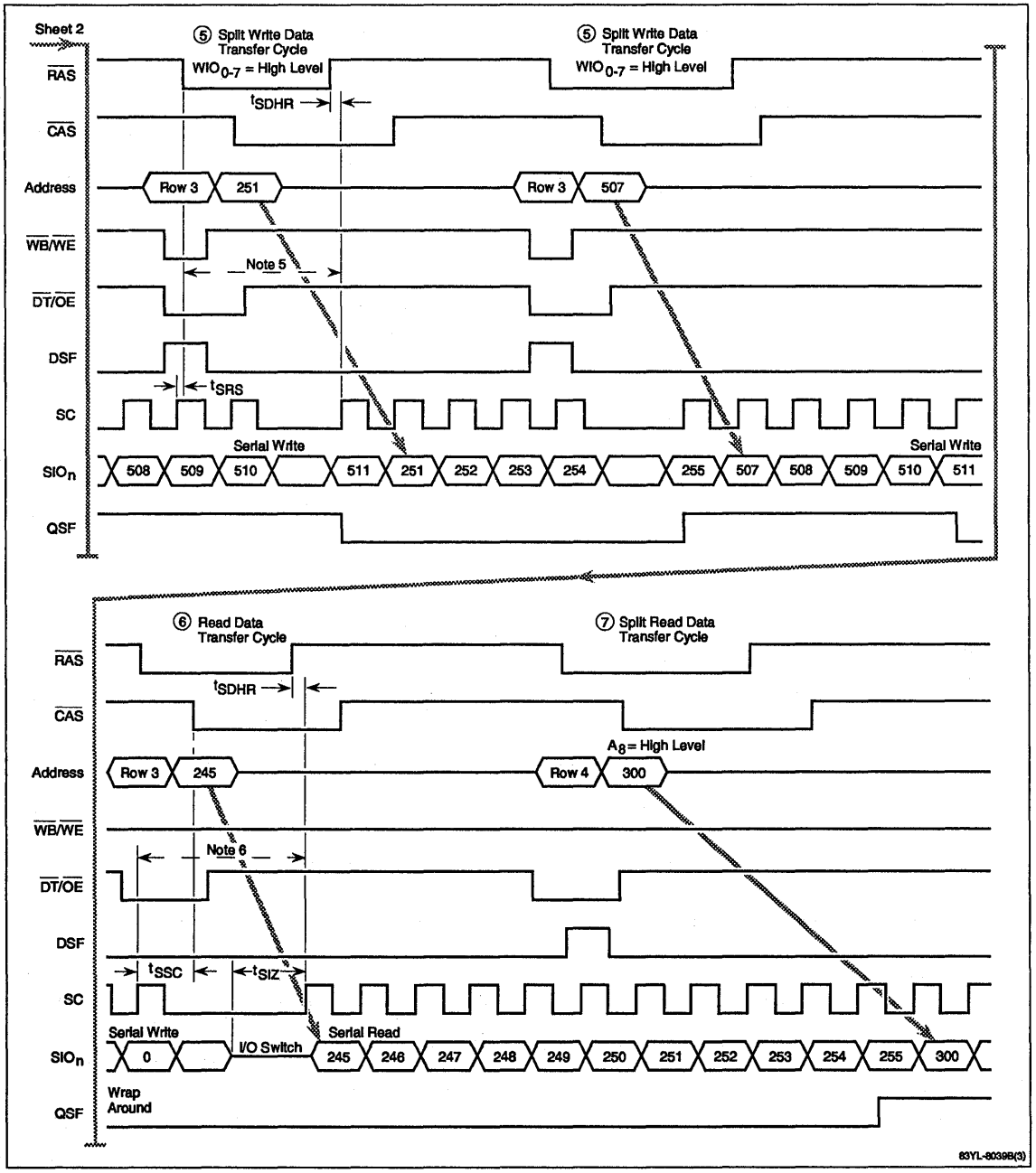
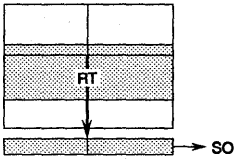
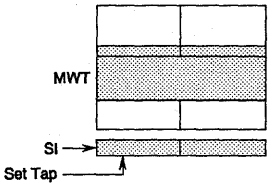
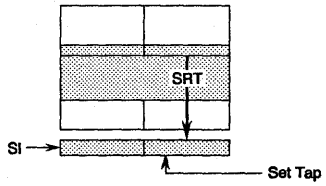
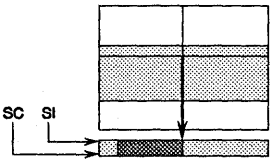
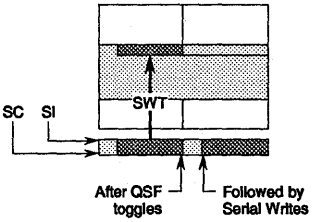
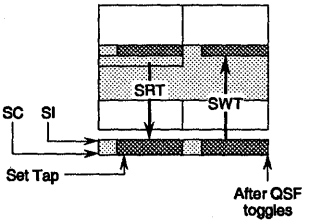


Figure 3. Advanced Serial Write Operation

Step	Operation	
1	The SC clock should be held inactive (low level).	
2	Perform a read data transfer (RT), copying the contents of the first row of data in the selected block to the data register.	
3	Perform a masked write transfer (MWT) to change the serial port to the serial write mode and set the start address for the next serial write operation. For this MWT, the bit mask data on all I/Os will be set to 0, preventing the memory array data from being changed.	
4	Perform a split read transfer (SRT) to set the data and tap address. (The serial port remains in the serial-in mode.)	
5	$\overline{SE}$ goes low (active) and the SC clock starts writing data to the lower half of the serial register.	
6	First, perform a split write transfer (SWT) cycle after the serial address moves from the lower to the upper half-register (QSF toggles).	
7	During the previous serial write to the upper half-register, a split read transfer was performed to the lower half-register, setting the tap for serial write to the lower half-register. When the serial write is completed to the upper half-register, a split write transfer is executed to transfer the new data to the memory array. This process is continued until the entire new block of data is written to the memory array.	

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Stopping Column Control

On previous dual-ported memories, after setting the pointer control (column start address in the serial register), there was no way to jump to the other half split register without serially clocking through the mid-point 255/256) of the 512-bit serial data register. Another way of stating this is that only a start position could be specified, not a stopping point.

The μPD482234/5 includes an 8-bit stop register, which corresponds to a boundary location in each split half register. The stop register value is latched during a special $\overline{CAS}$ before $\overline{RAS}$ cycle (CBRS) using address inputs A_0 - A_7. Sixteen different stop positions or boundaries can be specified for each half register using a stop register set cycle. With this feature, a mid-register to mid-register jump is possible. Refer to figure 4.

Application for Stopping Column Control. Since the page tiles are not organized for the display in scanline sequence, a method is needed to reassemble the segmented or tiled data from the memory array so that it flows out of the serial port in a scanline sequence. Stopping control provides the data transfer mechanism for moving pieces of data from the paged tiles through the serial port and out to the screen in a raster format.

By using stopping column control, the serial port can now clock out selected pieces of data, allowing the transfer of data corresponding to sequential pixels on a scanline. This feature provides for a flexible segmentation of memory and permits an efficient transfer of these segments from the memory to the screen.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle With Stop Register Set (CBRS). This special $\overline{CAS}$ before $\overline{RAS}$ cycle writes boundary locations to a stop register. The boundary value is supplied by addresses A_7 - A_0 and is latched at the falling edge of $\overline{RAS}$. (Note: This is a real-time stop register set cycle; that is, the new stop register value is changed during this CBRS cycle.)

After power-up, initializing this register by performing a CBRS or a CBR (option reset CBR register) is required. The value in the stop register and its bit boundary location are shown in table 3. This CBRS cycle will also refresh the specified row in the DRAM.

Table 3. Stop Register Set

Stop Register Value A_7 - A_0	Boundary Location (Jumps to tap after accessing this boundary)
1111 1111	255, 511 (default)
0111 1111	127, 255, 383, 511
0011 1111	63, 127, 191, 255, 319, 383, 447, 511
0001 1111	31, 63, 95, 127, 159, 191, 223, 255, 287, 319, 351, 383, 415, 447, 479, 511
0000 1111	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255, 271, 287, 303, 319, 335, 351, 367, 383, 399, 415, 431, 447, 463, 479, 495, 511

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle With Option Reset (CBR). After executing this option reset cycle, the write-per-bit mask register and the stop register will reset to the default condition. For example, the write-per-bit masking will be new mask and the stop register will be reset to 1111 1111. This CBR cycle will refresh the specified row in the DRAM.

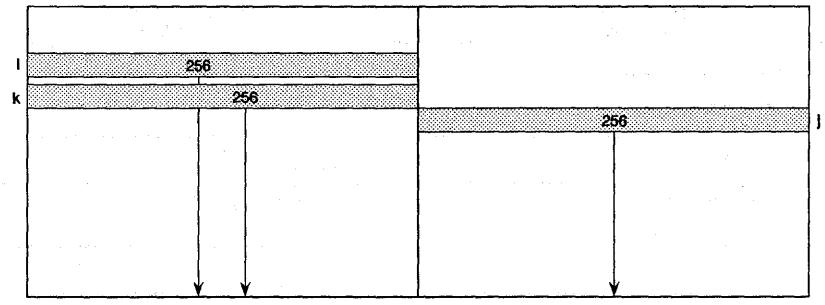
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle With No Reset (CBRN). This $\overline{CAS}$ before $\overline{RAS}$ cycle refreshes the specified row without clearing or changing any of the options and register values.

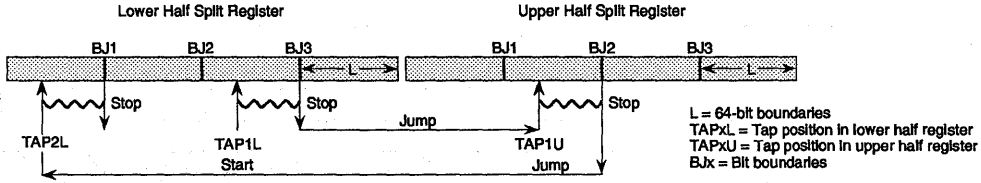
Recommended CBR, CBRS, and CBRN Cycles

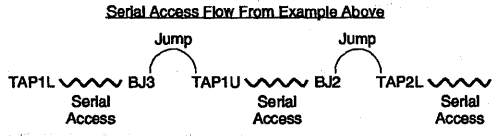
To ensure that the device has not entered unwanted register modes, at least one CBR (option reset) after power has stabilized is recommended. Eight CBR cycles or combination of RAS and CBR cycles satisfies the initialization sequence.

A CBR after each vertical retrace is recommended. This fail-safe routine is for cases where a system misoperation causes entry into an unwanted mode. If the stop register function is used, then a CBRS would follow every CBR cycle. If the stop register function is not required and persistent write masking is employed, then use a CBRN. This keeps the old mask function.

Figure 4. Example of Split Read Transfer With Boundary Jump (Sheet 1 of 2)







① Perform a Stop Register Set Cycle CBRS CBR with $\overline{WE}$ = low level and DSF = high level A_7-A_0 = 00111111

② Split Data Transfer Cycle

③ Split Data Transfer Cycle

④ Split Data Transfer Cycle

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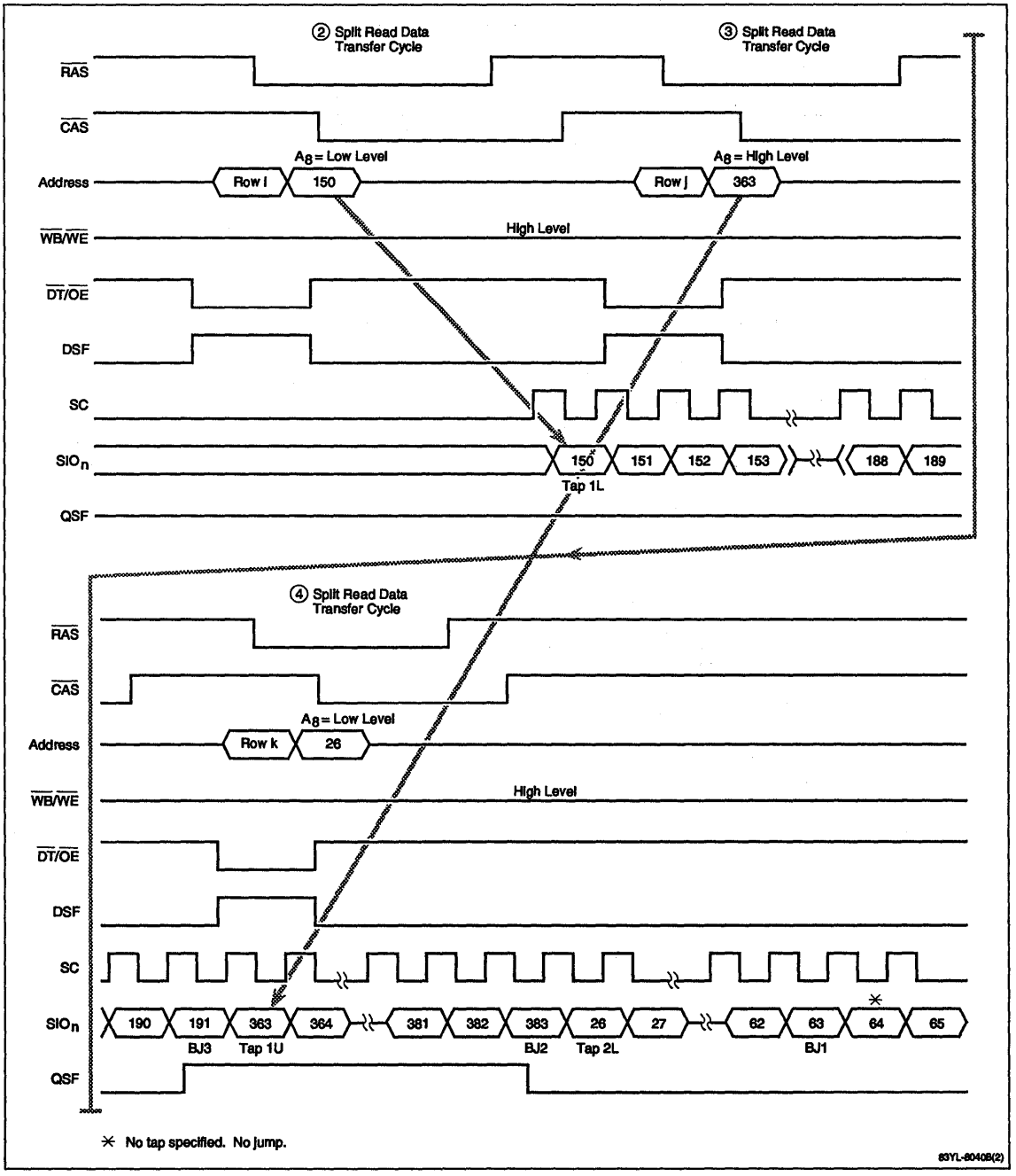
Figure 4. Example of Split Read Transfer With Boundary Jump (Sheet 2 of 2)



Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temp	T_A	0		+70	°C

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Limit (max)	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 - A_8
	$C_{I(\overline{DT}/\overline{OE})}$	8	pF	$\overline{DT}/\overline{OE}$
	$C_{I(\overline{WB}/\overline{WE})}$	8	pF	$\overline{WB}/\overline{WE}$
	$C_{I(DSF)}$	8	pF	DSF
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SE})}$	8	pF	$\overline{SE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 - W_7/IO_7
Output capacitance	$C_{O(SIO)}$	7	pF	SIO_0 - SIO_7
	$C_{O(QSF)}$	7	pF	QSF

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Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Port Operation						
Random Access	Serial Read	Parameter	−70 (max)	−80 (max)	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	130	130	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; DSF low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Standby	Standby	I_{CC2}	10	10	mA	D_{OUT} = high impedance; address cycling; t_{RC} = t_{RC} min; $\overline{CAS}$ = $\overline{RAS}$ = V_{IH}; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 4)
			1.0	1.0	mA	$\overline{RAS}$, $\overline{CAS}$, and $\overline{SE}$ ≥ V_{CC} − 0.2 V; A_0 - A_8, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, DSF, SC stay at V_{IH} ≥ V_{CC} − 0.2 V or V_{IL} ≤ GND + 0.2 V
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	115	115	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; DSF low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 2)
Fast-page cycle	Standby	I_{CC4}	100	90	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 3)
Hyper-page cycle	Standby	I_{CC4}	130	120	mA	
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	90	90	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Data transfer cycle	Standby	I_{CC6}	140	140	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SE}$ = V_{IH}; SC = V_{IH} or V_{IL}

Power Supply Current (cont)

Port Operation						
Random Access	**Serial Read**	**Parameter**	**-70 (max)**	**-80 (max)**	**Unit**	**Test Conditions**
Read/write cycle	Active	I_{CC7}	195	190	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; DSF low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Standby	Active	I_{CC8}	70	65	mA	D_{OUT} = high impedance; address cycling; $t_{RC} = t_{RC}$ min; $\overline{CAS} = \overline{RAS} = V_{IH}$; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 4)
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	180	175	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; DSF low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Fast-page cycle	Active	I_{CC10}	165	150	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 3)
Hyper-page cycle	Active	I_{CC10}	195	180	mA	
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	155	150	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Data transfer cycle	Active	I_{CC12}	205	200	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Color register set cycle	Standby	I_{CC13}	120	120	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IH}$; SC = V_{IH} or V_{IL}
Color register set cycle	Active	I_{CC14}	185	180	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Flash write cycle	Standby	I_{CC15}	120	120	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IH}$; SC = V_{IH} or V_{IL}
Flash write cycle	Active	I_{CC16}	185	180	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Block write cycle	Standby	I_{CC17}	130	130	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IH}$; SC = V_{IH} or V_{IL}
Block write cycle	Active	I_{CC18}	195	190	mA	$t_{RC} = t_{RC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Block write in fast-page cycle	Standby	I_{CC19}	110	100	mA	$t_{PC} = t_{PC}$ min; $\overline{SE} = V_{IH}$; SC = V_{IH} or V_{IL}
Block write in hyper-page cycle	Standby	I_{CC19}	135	125	mA	
Block write in fast-page cycle	Active	I_{CC20}	175	160	mA	$t_{PC} = t_{PC}$ min; $\overline{SE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Block write in hyper-page cycle	Active	I_{CC20}	200	185	mA	

Notes:

(1) No load on IO, SO, and QSF. Except for I_{CC2}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked but is kept at a stable high level. The column addresses are also assumed to be kept stable at either a high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

(4) A change in row addresses must not occur more than once in a read or write cycle.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO, SIO) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −1 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 2.1 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −1 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 2.1 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Access time from column address	t_{AA}		35		40	ns	(Note 4)
Access time from previous $\overline{CAS}$	t_{ACE}		65		75	ns	(Note 14)
Access time from $\overline{CAS}$ trailing edge	t_{ACP}		40		45	ns	
$\overline{DT}$ low hold time after address	t_{ADD}	25		30		ns	(Note 9)
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	55		65		ns	(Note 7)
Access time from previous $\overline{WE}$	t_{AWE}		60		70	ns	(Note 14)
Acces time from $\overline{CAS}$	t_{CAC}		20		25	ns	(Note 4)
Column address hold time	t_{CAH}	10		12		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	20		25		ns	(Note 9)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	10		12		ns	
$\overline{CAS}$ precharge time	t_{CP}	10		10		ns	
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	10		10		ns	
Propagation delay time from $\overline{CAS}$ to QSF	t_{CQD}	0	65	0	75	ns	
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	0		0		ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40		50		ns	(Note 7)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		ns	
Data in hold time	t_{DH}	12		15		ns	(Note 8)
Output hold time from $\overline{CAS}$	t_{DHC}	5		5		ns	(Note 14)
$\overline{DT}$ high hold time	t_{DHH}	10		12		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		ns	
$\overline{DT}$ low setup time	t_{DLS}	0		0		ns	
Propagation delay time from $\overline{DT/OE}$ to QSF	t_{DQD}	0	30	0	35	ns	
Propagation delay time from $\overline{RAS}$ high to QSF	t_{DQR}	0	40	0	45	ns	
Data in setup time	t_{DS}	0		0		ns	(Note 8)

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AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{DT}$ high pulse width	t_{DTP}	20		25		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	0		0		ns	(Note 9)
DSF hold time from $\overline{CAS}$	t_{FCH}	12		15		ns	
DSF setup time from $\overline{CAS}$	t_{FCS}	0		0		ns	
DSF hold time from $\overline{RAS}$	t_{FRH}	10		12		ns	
DSF setup time from $\overline{RAS}$	t_{FRS}	0		0		ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	12	10,000	ns	(Note 14)
Hyper-page mode cycle time	t_{HPC}	35		40		ns	(Note 14)
Read-write/Read-modify-write cycle time	t_{PRWC}	90		105		ns	
OE hold time after $\overline{CAS}$ high	t_{OCH}	10		10		ns	
Access time from $\overline{OE}$	t_{OEA}		20		25	ns	
$\overline{OE}$ high to data in setup delay	t_{OED}	15		20		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		ns	
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	15	0	20	ns	(Note 5)
Output disable time from $\overline{CAS}$ high	t_{OFC}	0	15	0	20	ns	(Note 5, 10, 14)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	15	0	20	ns	(Note 5, 11)
Output disable time from $\overline{RAS}$ high	t_{OFR}	0	15	0	20	ns	(Note 5, 10, 14)
$\overline{OE}$ hold time after $\overline{RAS}$ high	t_{ORH}	10		10		ns	
Fast-page mode cycle	t_{PC}	45		50		ns	
Propagation delay time from SC to QSF	t_{PD}		20		25	ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80	ns	(Note 4)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	40	ns	(Note 4)
Row address hold time	t_{RAH}	10		12		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		ns	
$\overline{RAS}$ pulse width (non-page mode)	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width in page mode/hyper-page mode	t_{RASP}	70	100,000	80	100,000	ns	
Random read or write cycle time	t_{RC}	140		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	22	55	ns	(Note 4)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns	(Note 6)
Read command setup time	t_{RCS}	0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{RDH}	65		70		ns	(Note 9)
	t_{RDHS}	15		15		ns	(Note 9)
Refresh period	t_{REF}		8		8	ms	
$\overline{RAS}$ precharge time	t_{RP}	50		60		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	10		10		ns	
Propagation delay time from $\overline{RAS}$ to QSF	t_{RQD}		95		105	ns	
Read command hold time after $\overline{RAS}$ high	t_{RRH}	0		0		ns	(Note 6)
$\overline{RAS}$ hold time	t_{RSH}	20		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Read-write/Read-modify-write cycle time	t_{RWC}	185		205		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	90		105		ns	(Note 7)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	
Serial output access time from SC	t_{SCA}		17		20	ns	
Serial clock cycle time	t_{SCC}	22		25		ns	
SC pulse width	t_{SCH}	5		7		ns	
SC precharge time	t_{SCL}	5		7		ns	
SC high to $\overline{DT}$ high	t_{SDD}	0		0		ns	(Note 9)
SC low hold time after $\overline{DT}$ high	t_{SDH}	40		50		ns	(Note 9)
	t_{SDHR}	45		55		ns	(Note 9)
Serial output access time from $\overline{SE}$	t_{SEA}		17		20	ns	
$\overline{SE}$ pulse width	t_{SEE}	5		7		ns	
$\overline{SE}$ hold time from SC	t_{SEH}	10		12		ns	
$\overline{SE}$ precharge time	t_{SEP}	5		7		ns	
$\overline{SE}$ setup time	t_{SES}	0		0		ns	
Output disable time from $\overline{SE}$ high	t_{SEZ}	0	15	0	20	ns	(Note 5)
Serial data in hold time	t_{SIH}	10		12		ns	
Serial data in setup time	t_{SIS}	0		0		ns	
Serial input disable time from SC	t_{SIZ}	0		0		ns	
Serial output hold time after SC high	t_{SOH}	5		5		ns	
$\overline{SE}$ low to serial output setup delay	t_{SOO}	5		5		ns	
SC hold time from $\overline{RAS}$	t_{SRH}	10		10		ns	(Note 12)
SC setup time from $\overline{RAS}$	t_{SRS}	10		10		ns	(Note 12)
Serial output disable time from $\overline{RAS}$	t_{SRZ}	0		0		ns	
SC high to $\overline{CAS}$ low	t_{SSC}	10		10		ns	(Note 9, 12)
Serial input enable time from $\overline{RAS}$	t_{SZH}	20		25		ns	
Transition time (rise/fall)	t_T	3	35	3	35	ns	
Write-per-bit hold time	t_{WBH}	10		12		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	
Write command hold time	t_{WCH}	12		15		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 7)
Output disable time from $\overline{WE}$ low	t_{WEZ}	0	15	0	20	ns	(Note 5, 10)
Write bit selection hold time	t_{WH}	10		12		ns	
Write command pulse width	t_{WP}	12		15		ns	
Write command pulse width	t_{WPZ}	12		15		ns	(Note 10)
Write bit selection setup time	t_{WS}	0		0		ns	

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AC Characteristics (cont)

Notes:

(1) All applied voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up ($V_{CC} \geq 4.5$ V), followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) See figures 5 for reference voltages and output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
Assumed: t_{RAD} (min) = t_{RAH} (min) + t_T.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} (min) or t_{RCH} (min) must be satisfied for a read cycle.

(7) t_{WCS}, t_{CWD}, t_{AWD} and t_{RWD} are restrictive operating parameters in early-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle.

If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a read modify-write cycle and the data output will contain data read from the selected cell. If none of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the leading edge of $\overline{CAS}$ in early write cycles and to the leading edge of (WB/)$\overline{WE}$ in delayed write or read-modify-write cycles.

(9) t_{RDH}, t_{CDH}, t_{ADD}, t_{SDD}, t_{SDH}, and t_{DTR} is an alternative parameter set of t_{RDHS}, t_{SSC}, and t_{SDHR} especially for real-time data transfer condition.

(10) Hyper-Page Mode Only: IO_0 - IO_7 turn to Hi-Z state when
- Both $\overline{RAS}$ and $\overline{CAS}$ go high; later one of t_{OFR} and t_{OFC} is valid.
- $\overline{WE}$ goes low; t_{WEZ} and t_{WPZ} are valid.
- $\overline{OE}$ goes high; t_{OEZ} is valid.

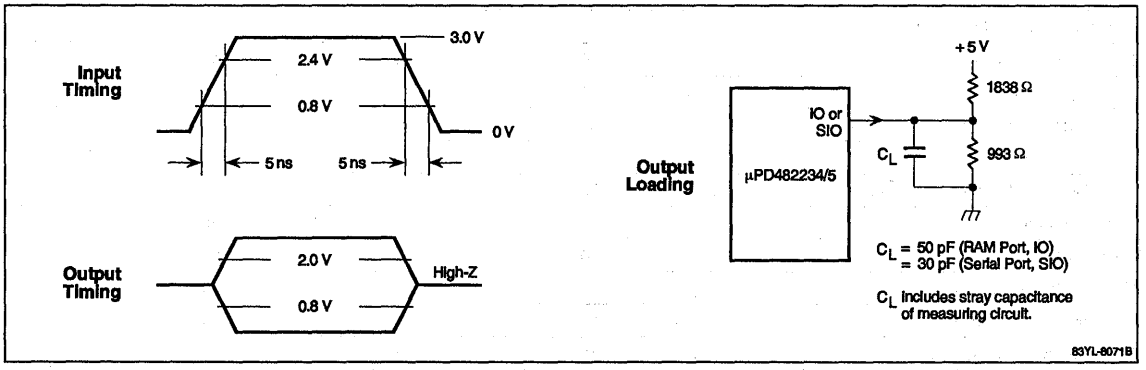
(11) Fast-Page Mode Only: $\overline{CAS}$ goes high; t_{OFF} is valid.

(12) If the stop register value is changed by a CBRS cycle, the $\overline{CAS}$ before $\overline{RAS}$ cycle must meet t_{SRS} and t_{SRH} to guarantee a following serial port boundary jump operation. Otherwise, t_{SRS} and/or t_{SRH} are "don't care" for those cycles.

(13) In a split read data transfer cycle and split write data transfer cycle, t_{SSC} and t_{SRS} are measured from the SC rising edge which reads/writes an address specified as boundary or tap location. These SC rising edges are not allowed during t_{SSC} or t_{SRS} through t_{SDHR}.

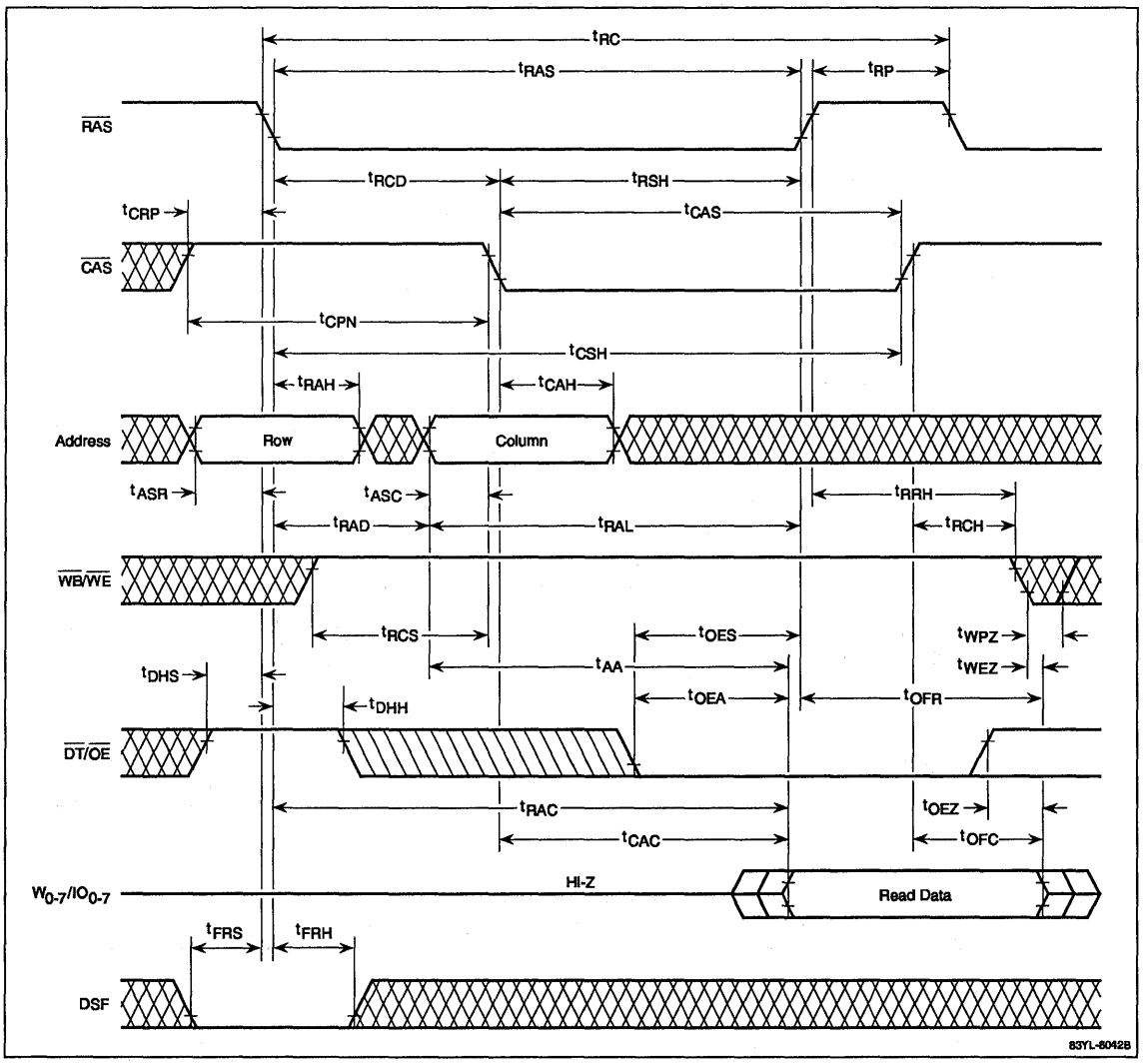
(14) These parameters apply only for the hyper-page mode devices (μPD482235).

Figure 5. Voltages and Loads for Timing Measurements



Timing Waveforms

Read Cycle (Hyper-Page Mode)



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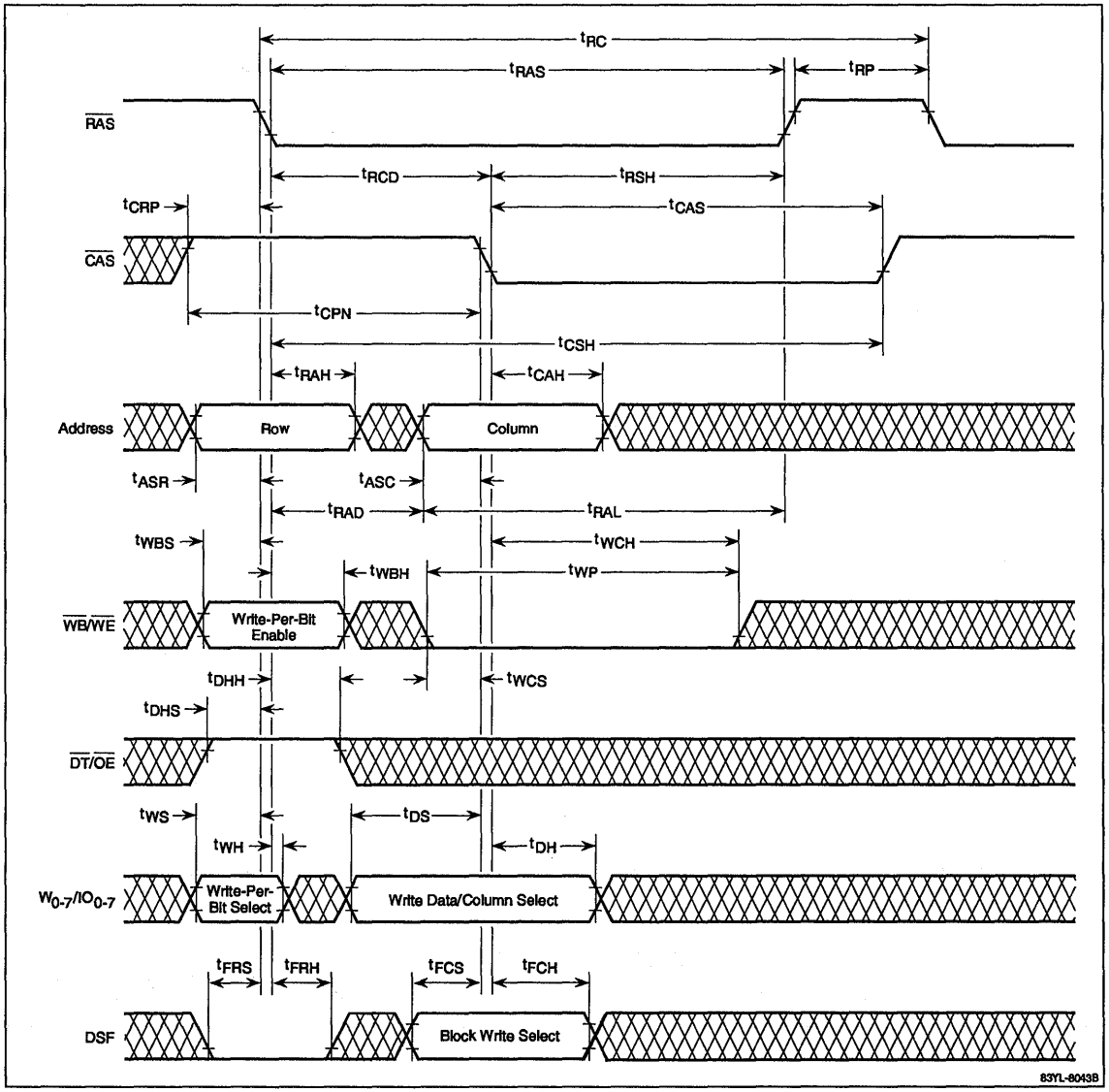
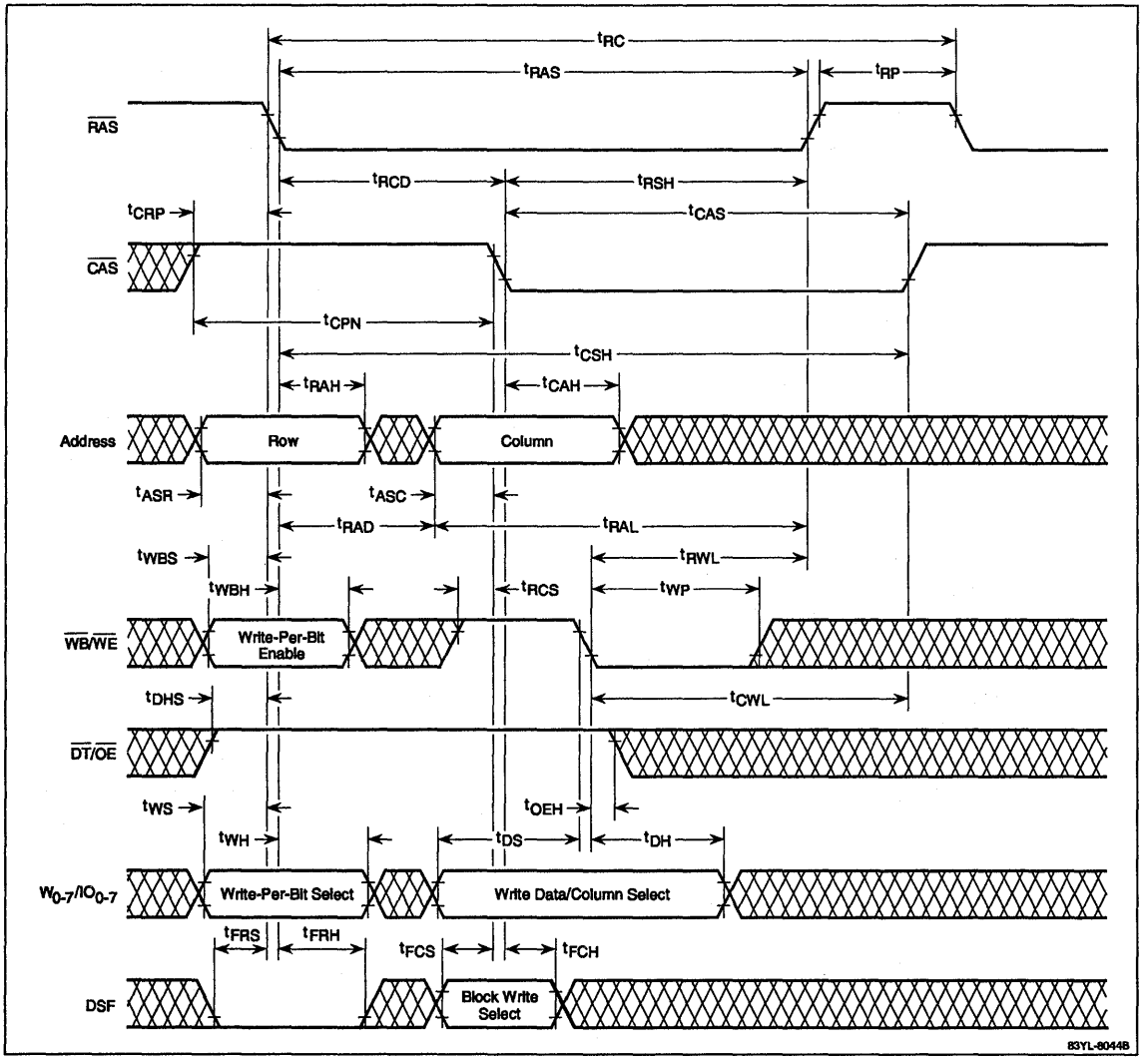
Timing Waveforms (cont)

Early Write Cycle and Early Block Write Cycle



Timing Waveforms (cont)

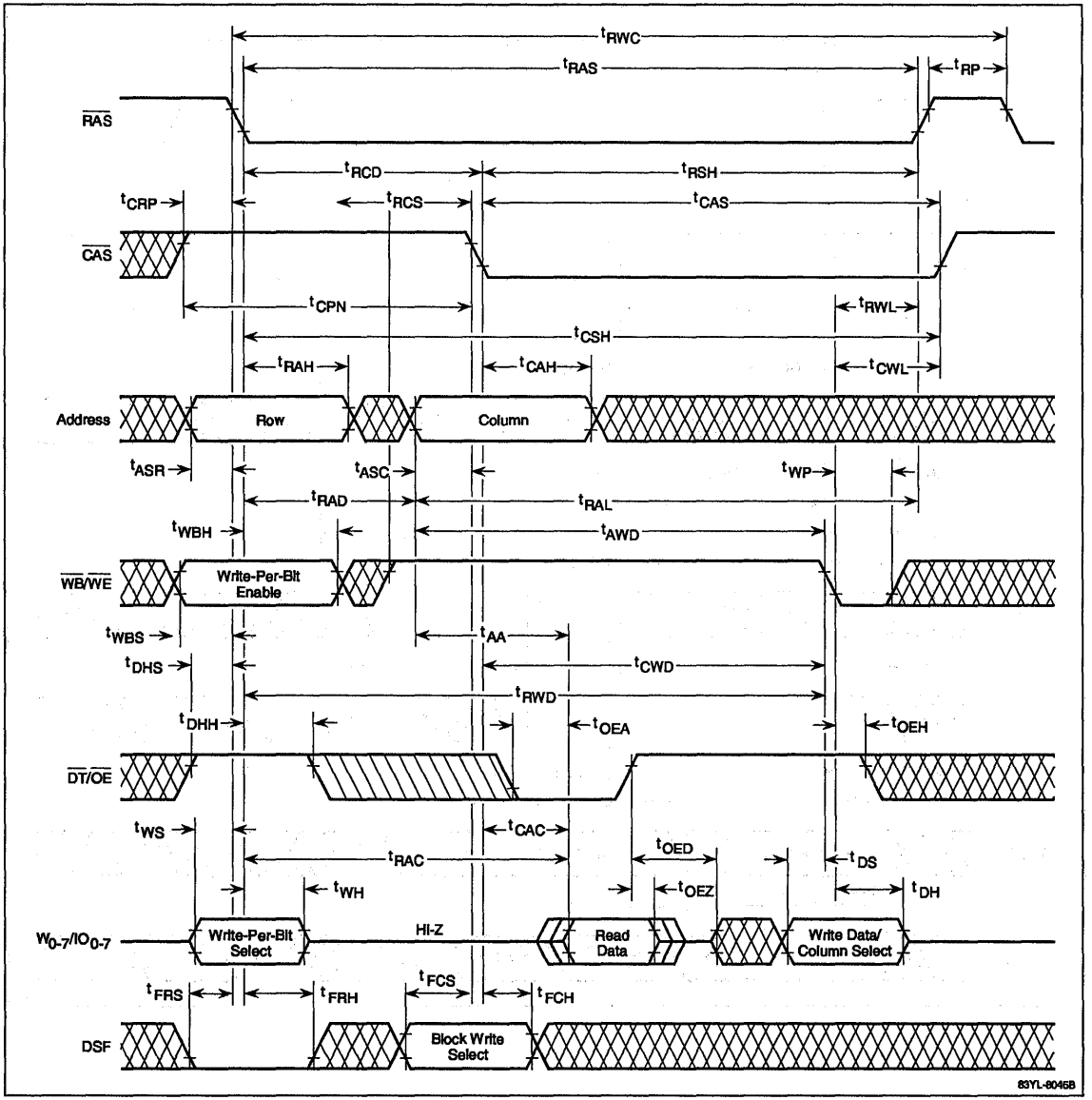
Late Write Cycle and Late Block Write Cycle



12g

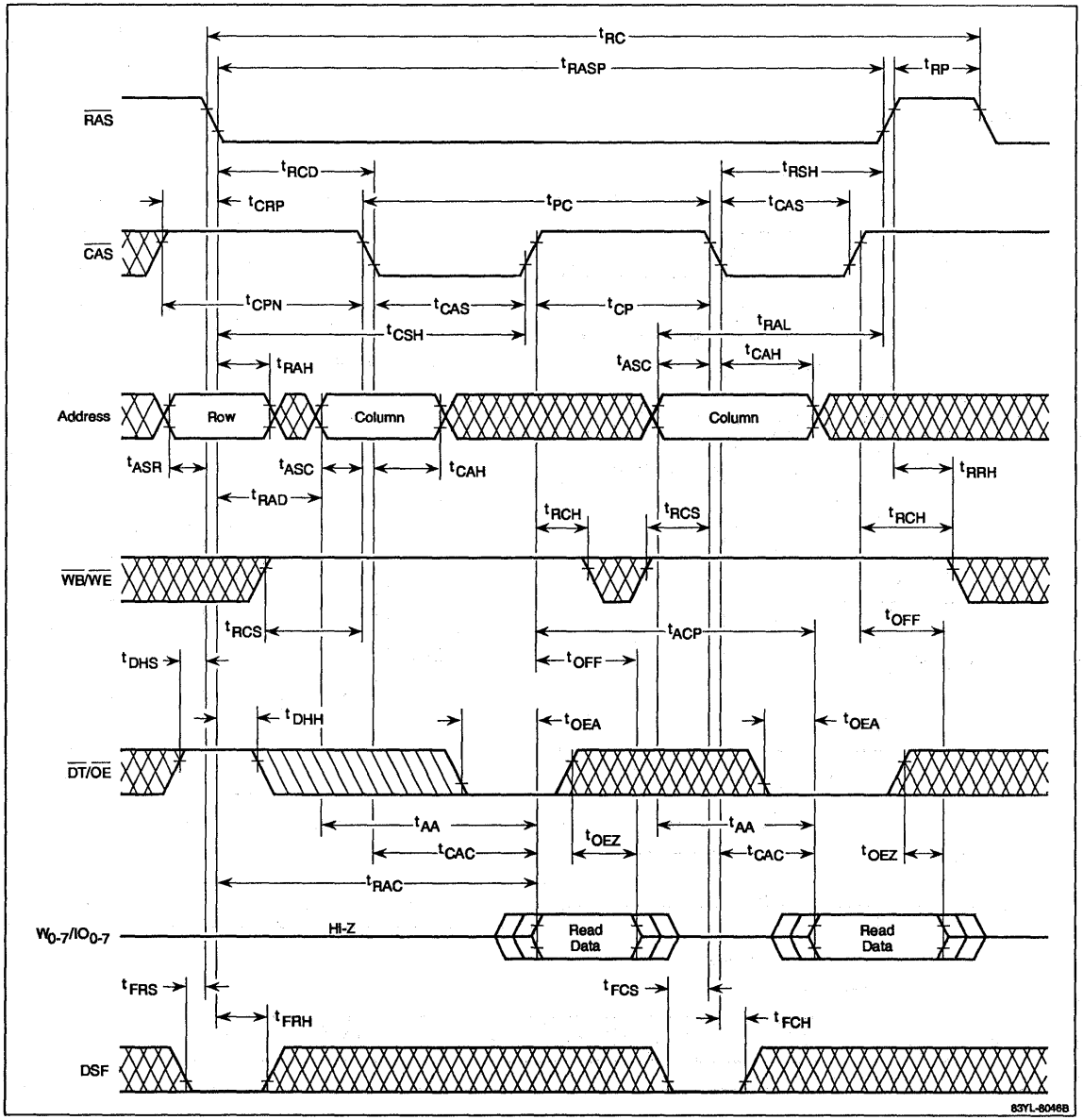
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Fast-Page Read Cycle



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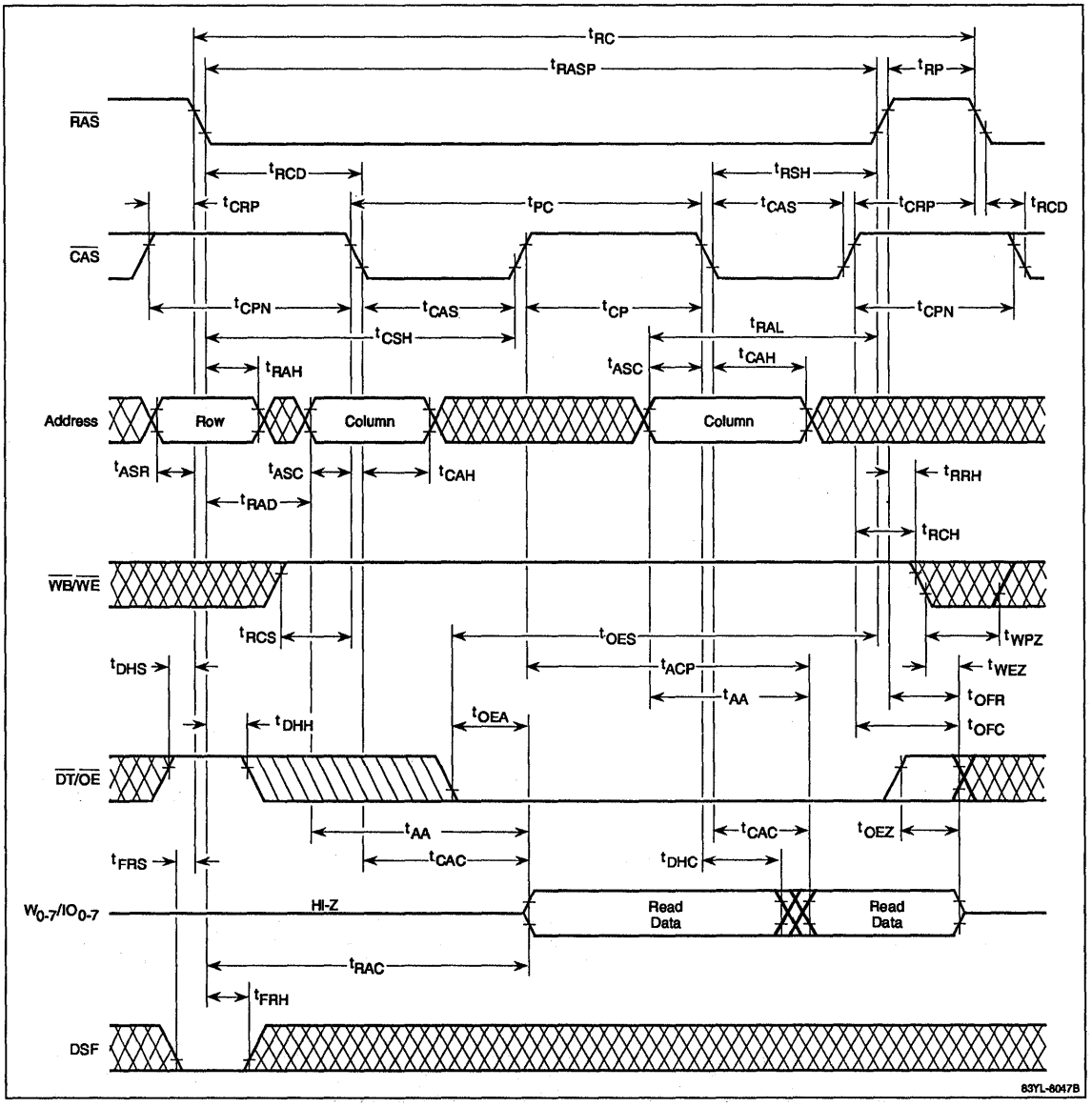
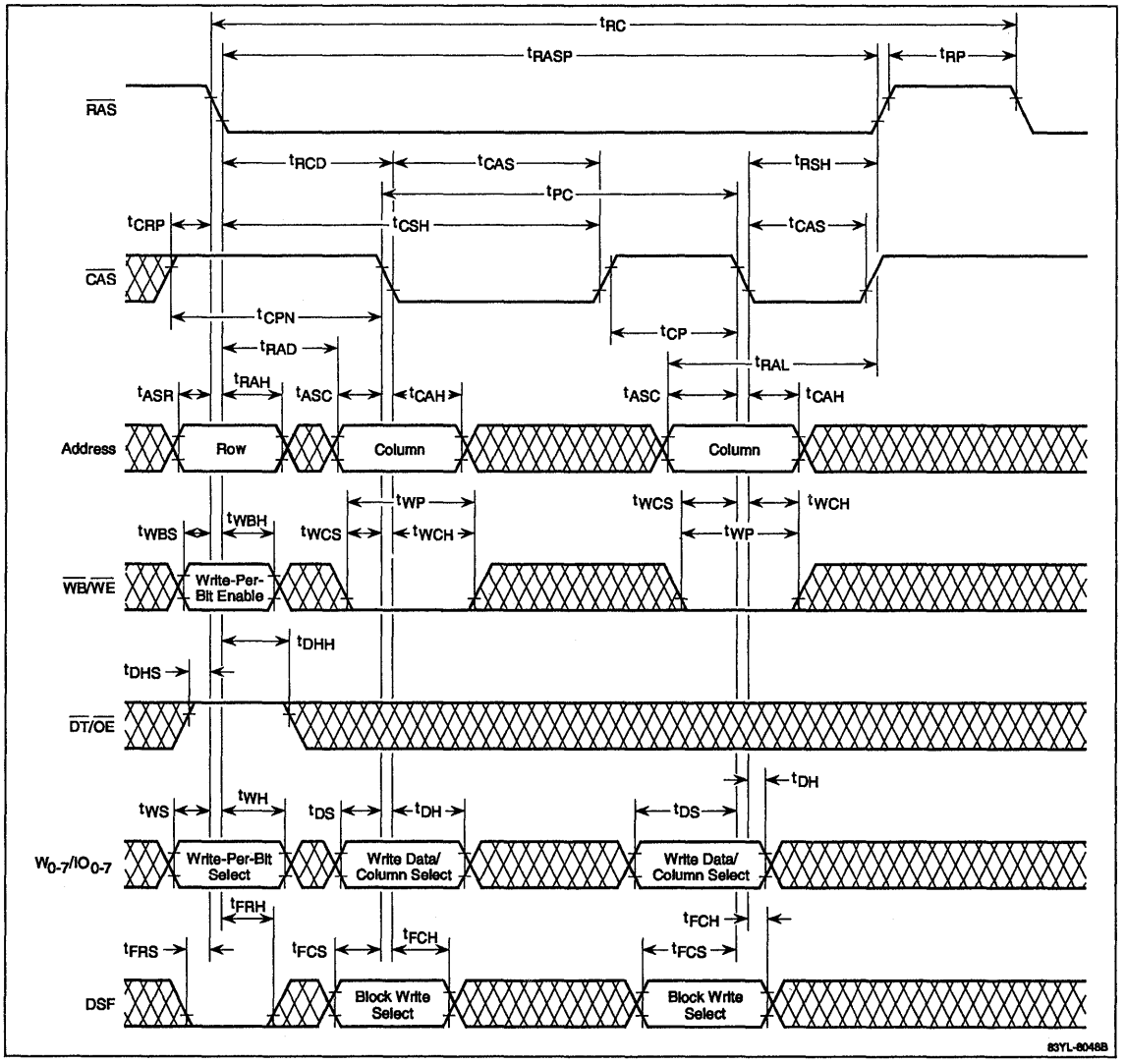
Timing Waveforms (cont)

Hyper-Page Read Cycle



Timing Waveforms (cont)

Fast-Page/Hyper-Page Early Write Cycle and Fast-Page/Hyper-Page Early Block Write Cycle



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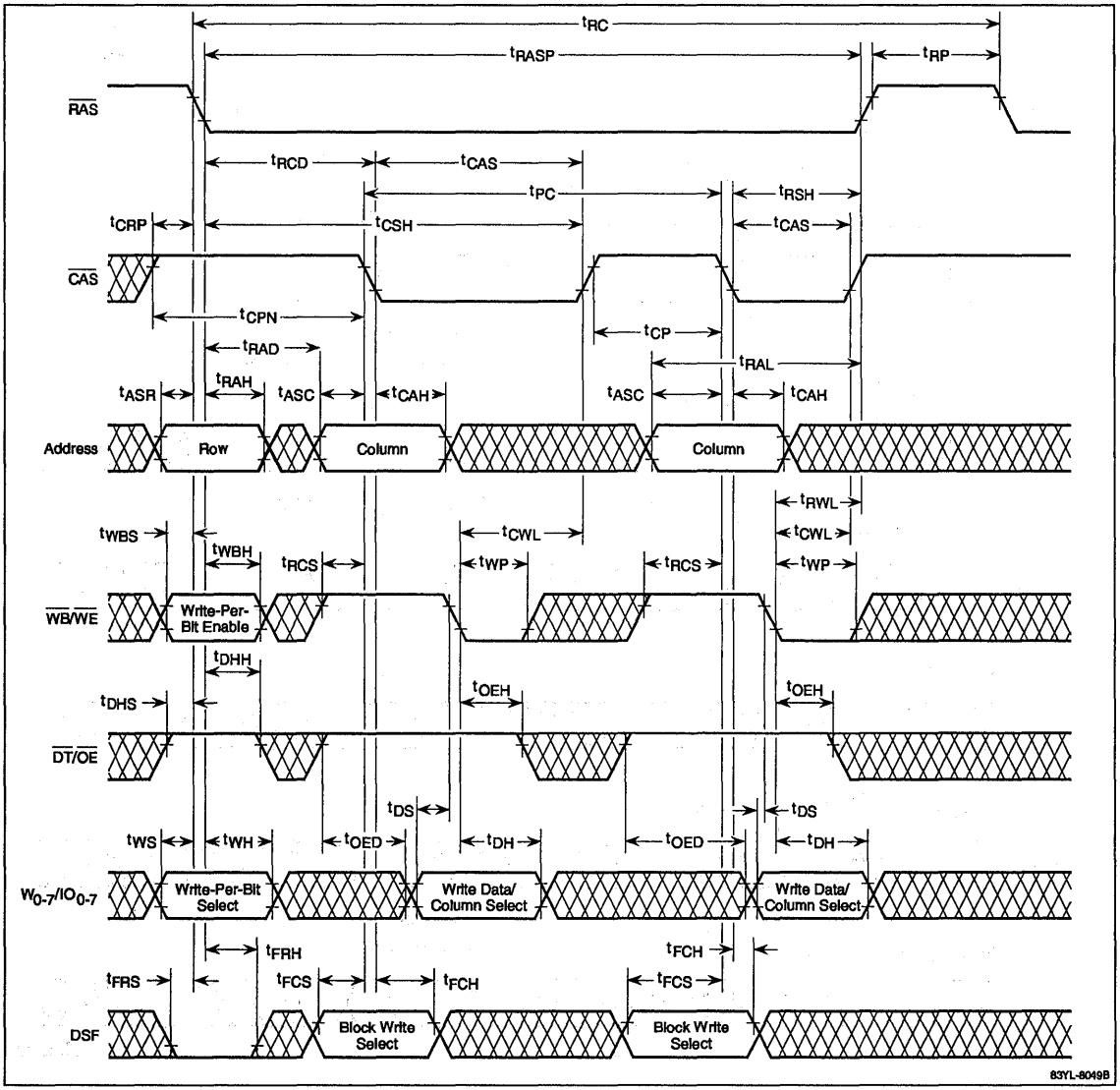
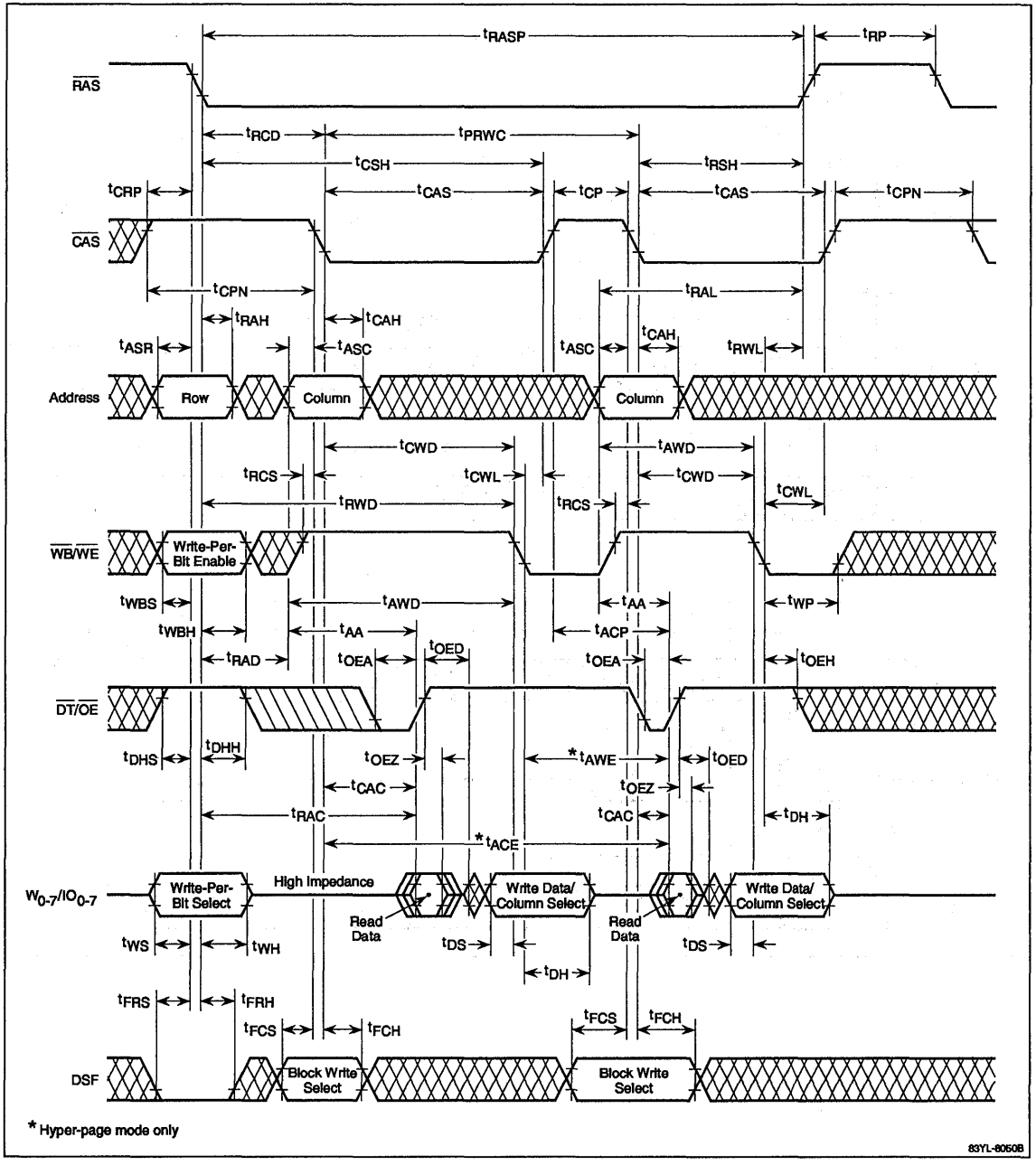
Timing Waveforms (cont)

Fast-Page/Hyper-Page Late Write Cycle and Fast-Page/Hyper-Page Late Block Write Cycle



Timing Waveforms (cont)

Fast-Page/Hyper-Page Read-Modify-Write Cycle



* Hyper-page mode only

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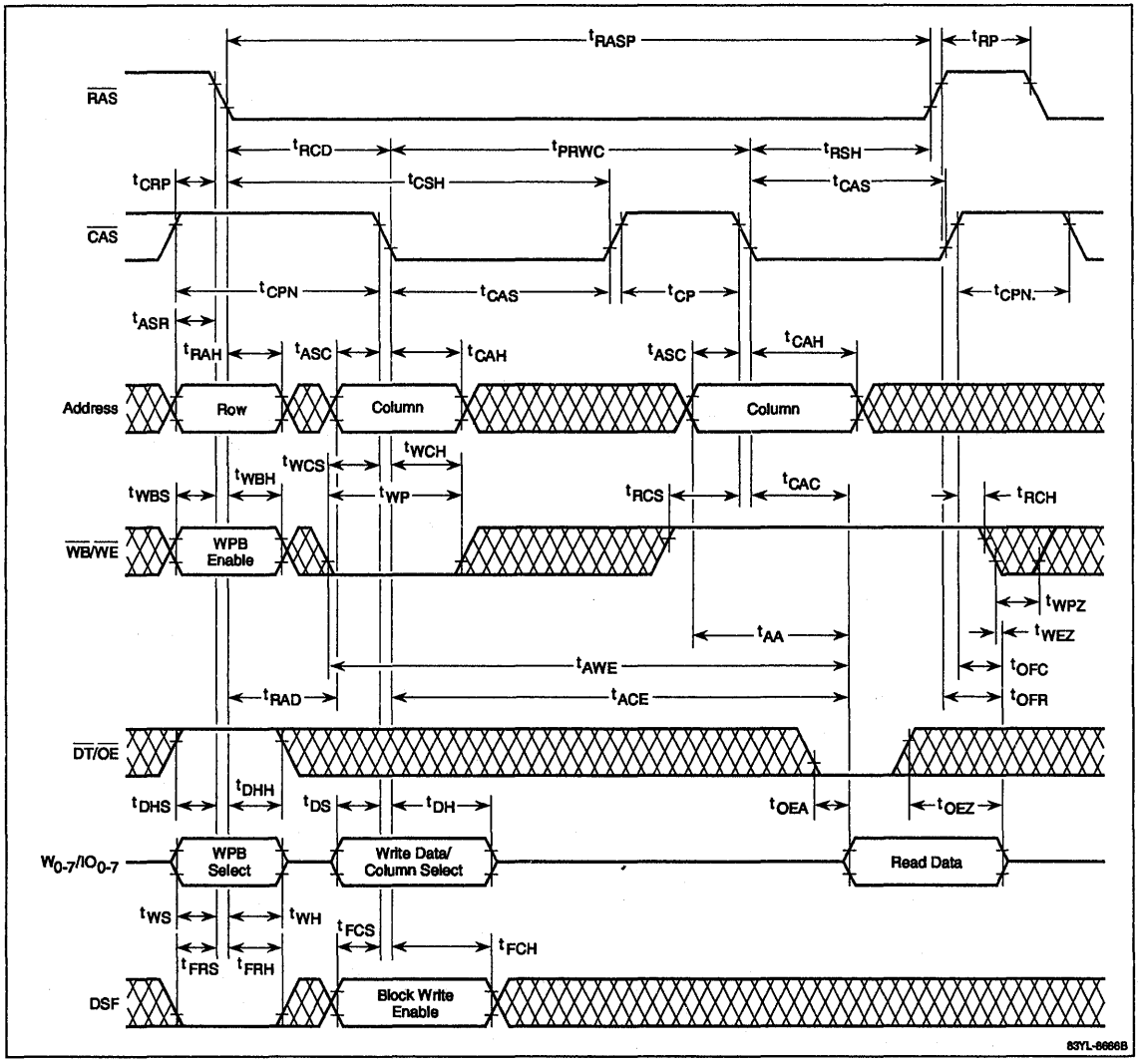
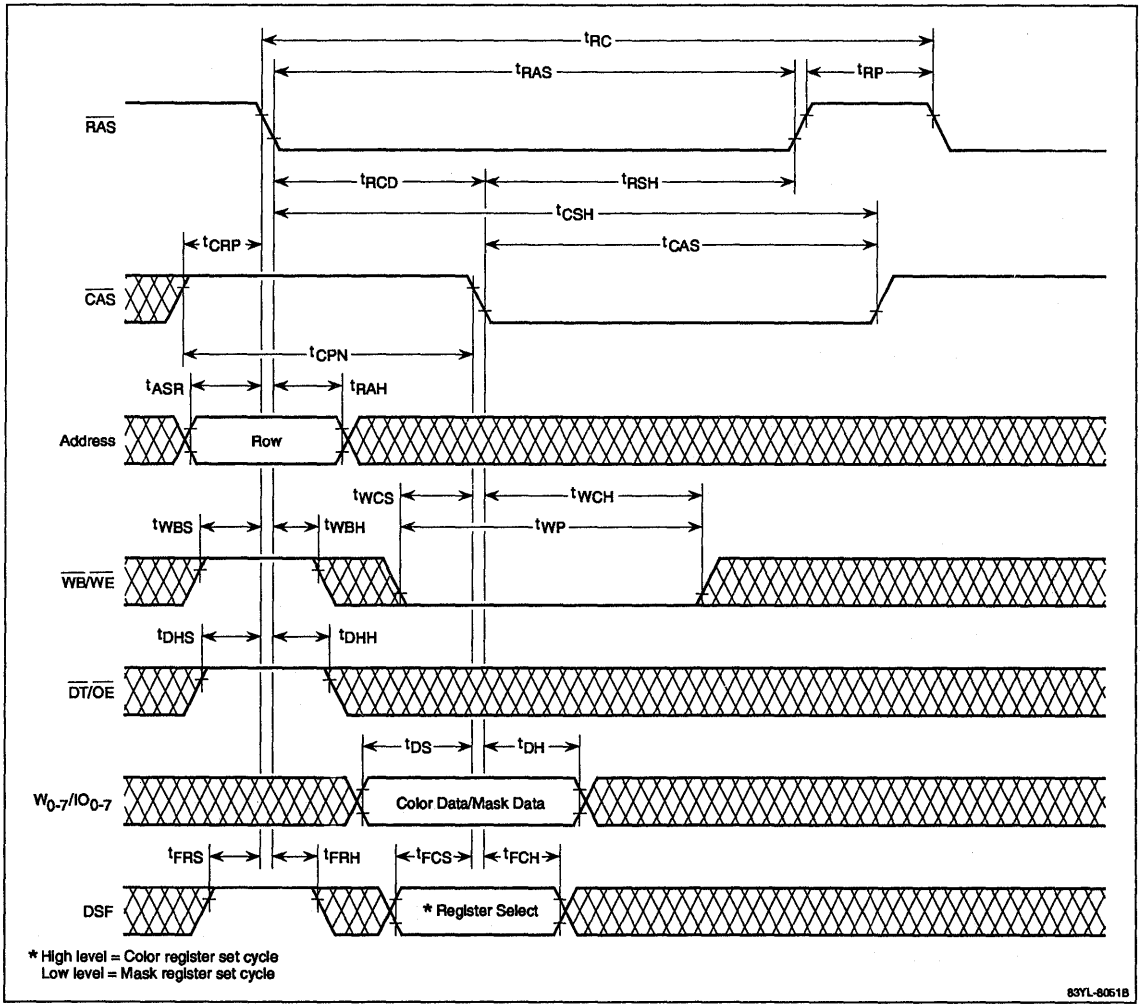
Timing Waveforms (cont)

Hyper-Page Write/Read Cycle



Timing Waveforms (cont)

Register Set LMR and LCR Cycles (Early Write)



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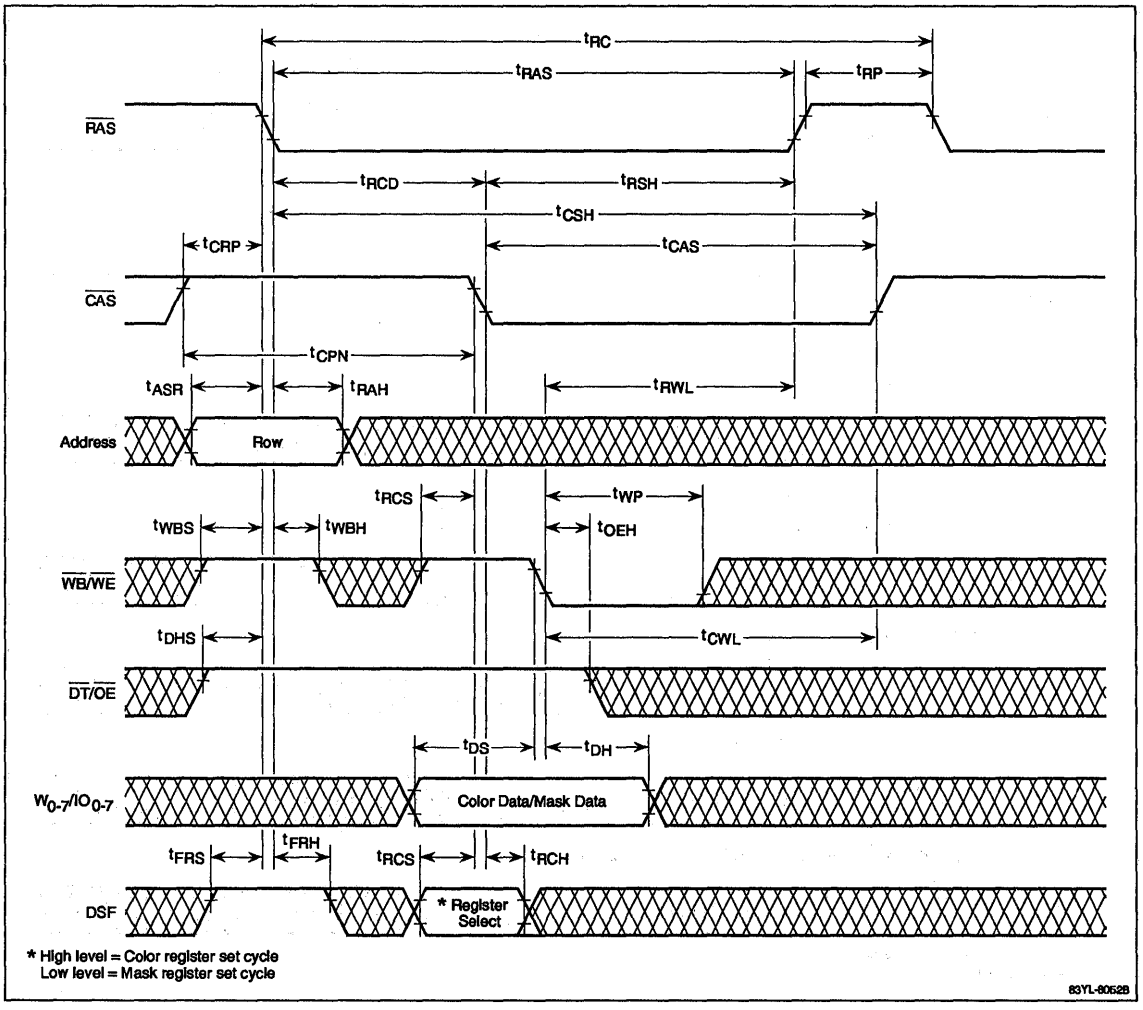
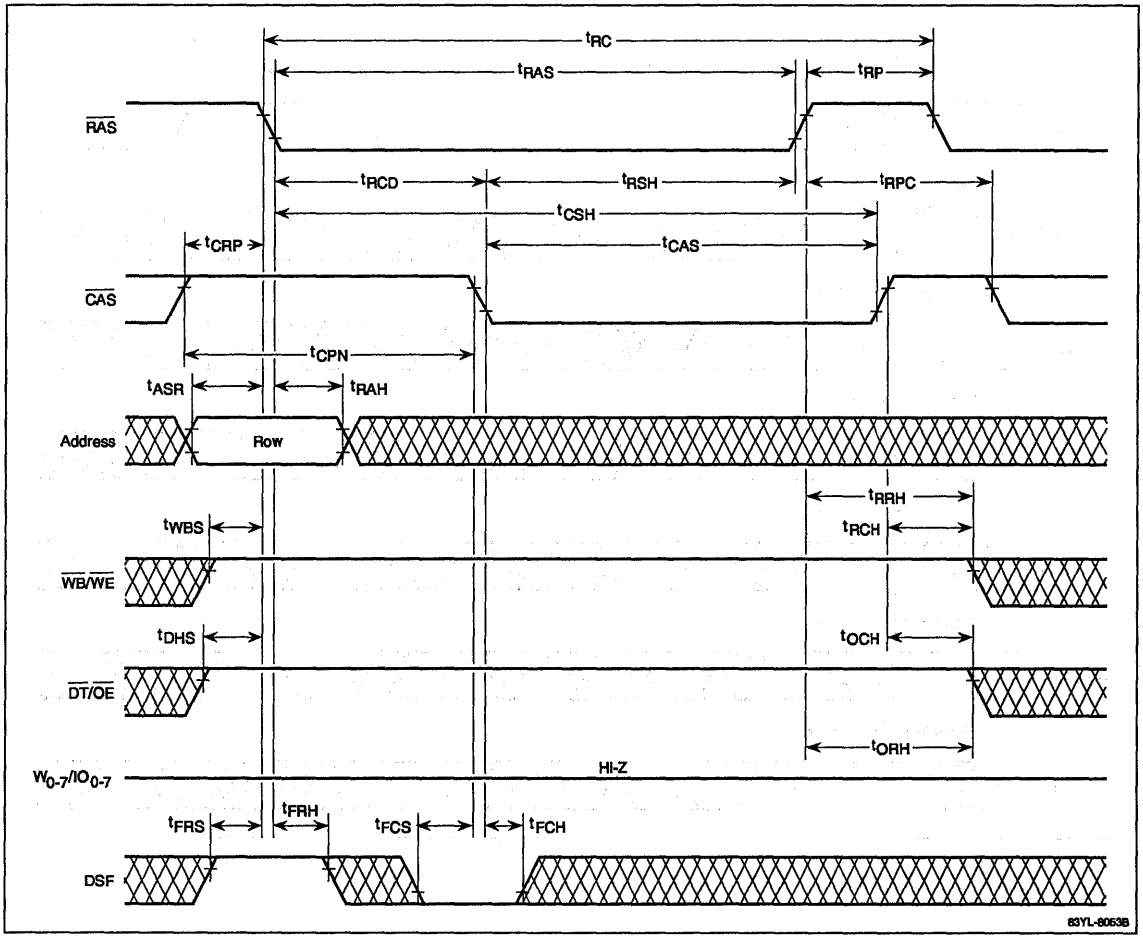
Timing Waveforms (cont)

Register Set LMR and LCR Cycles (Late Write)



Timing Waveforms (cont)

Reset Mask Register to New Mask Mode Cycle (non-JEDEC Standard)



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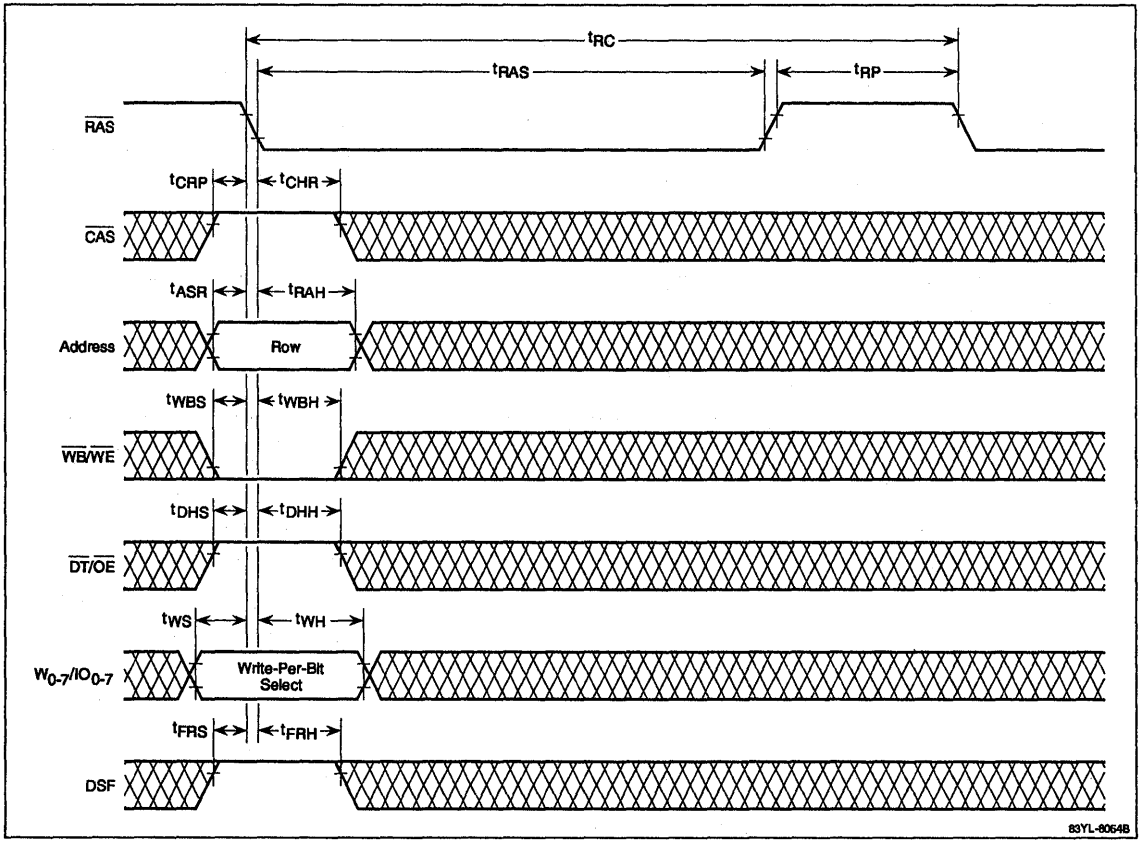
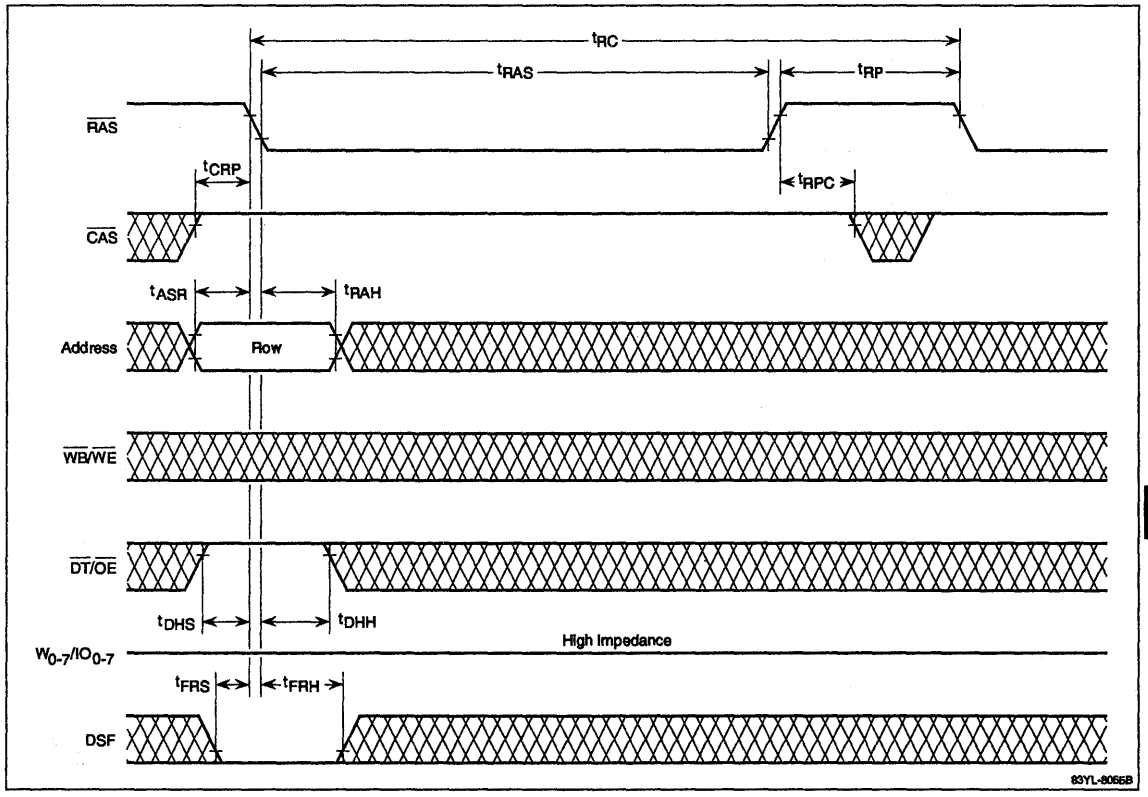
Timing Waveforms (cont)

Flash Write Cycle



Timing Waveforms (cont)

RAS-Only Refresh Cycle



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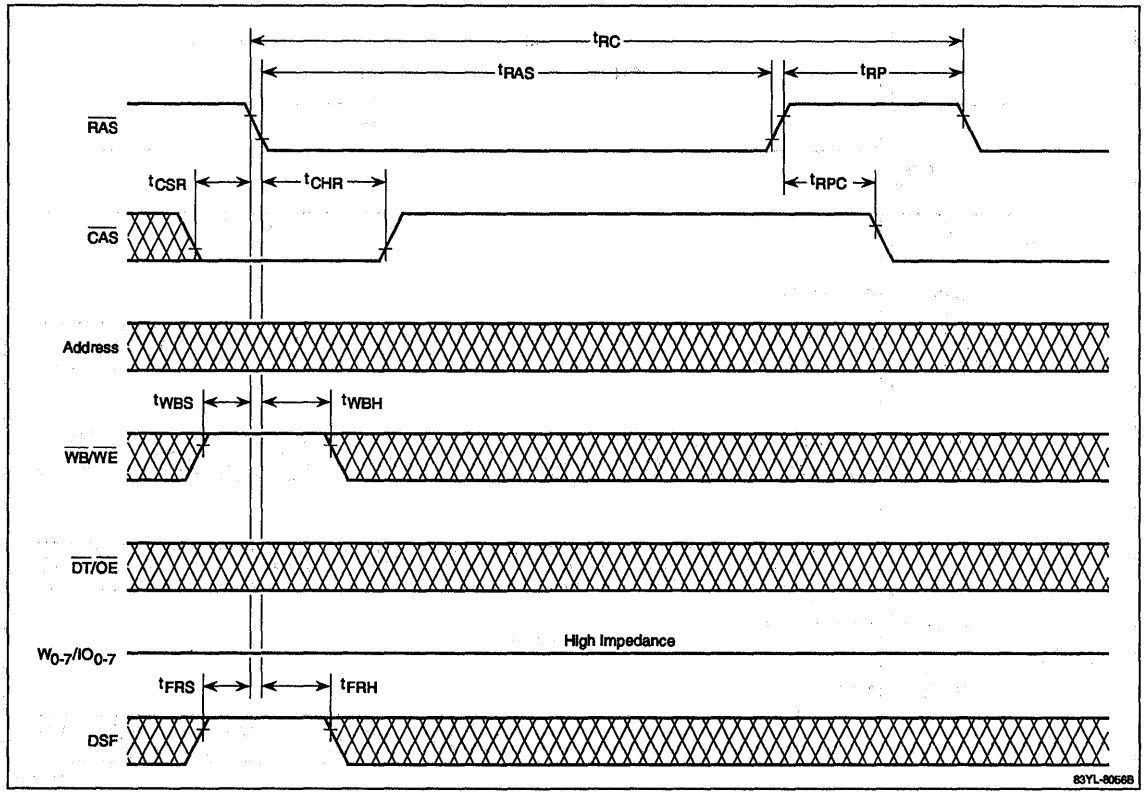
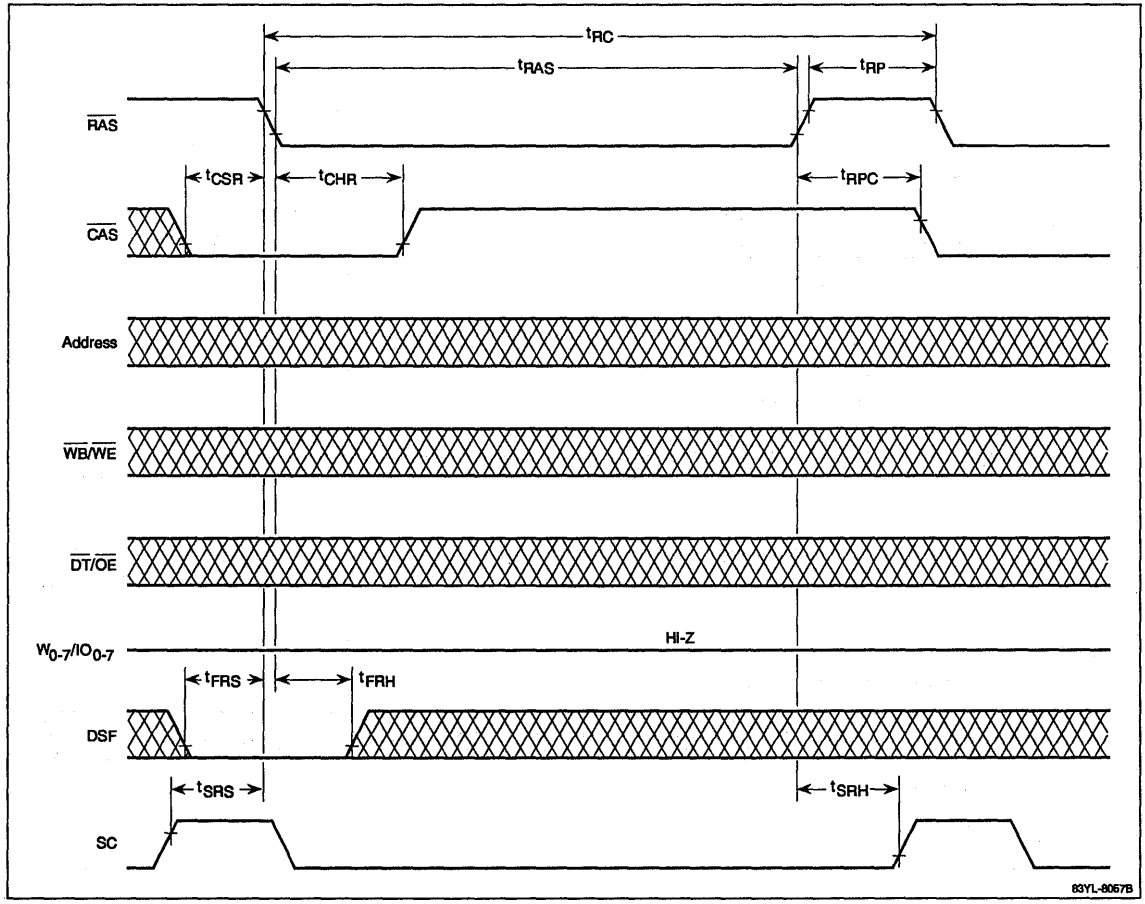
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle With No Option Reset (CBRN)



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle With Option Reset (CBR)



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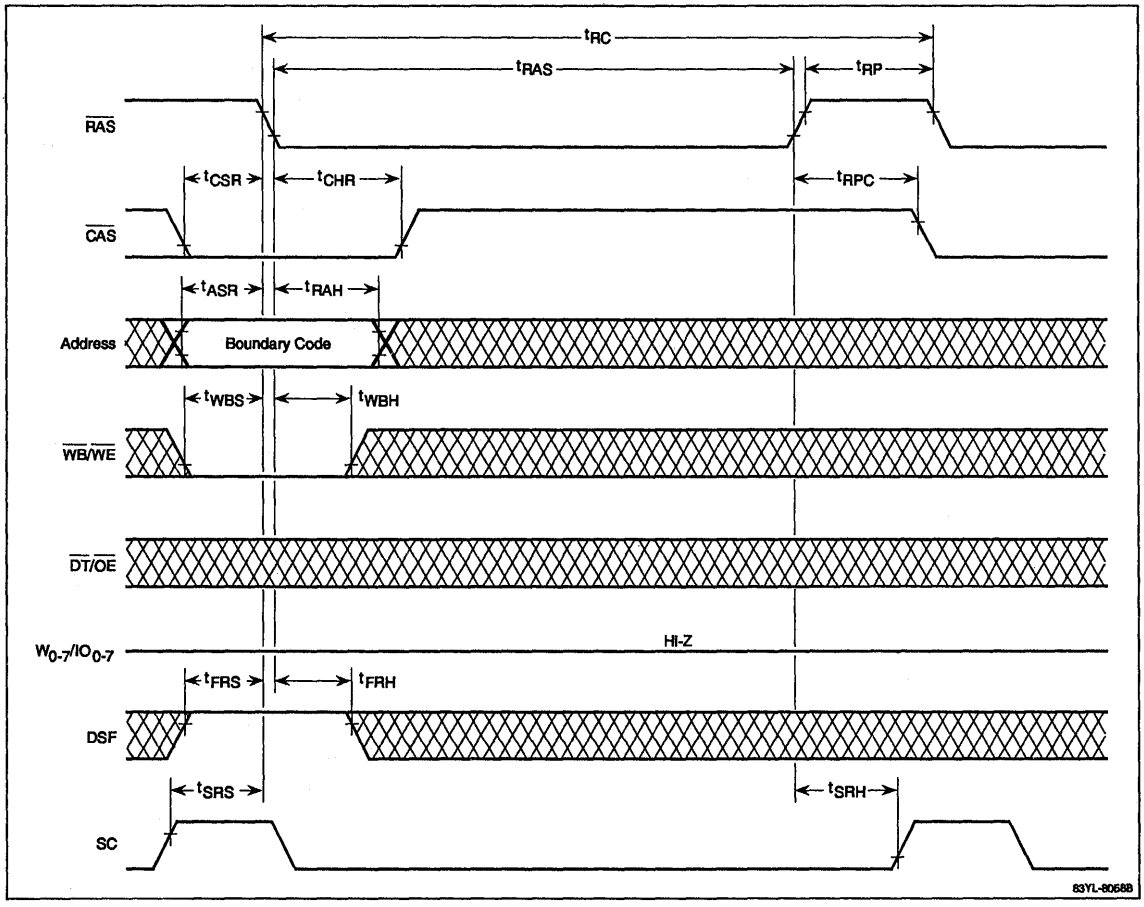
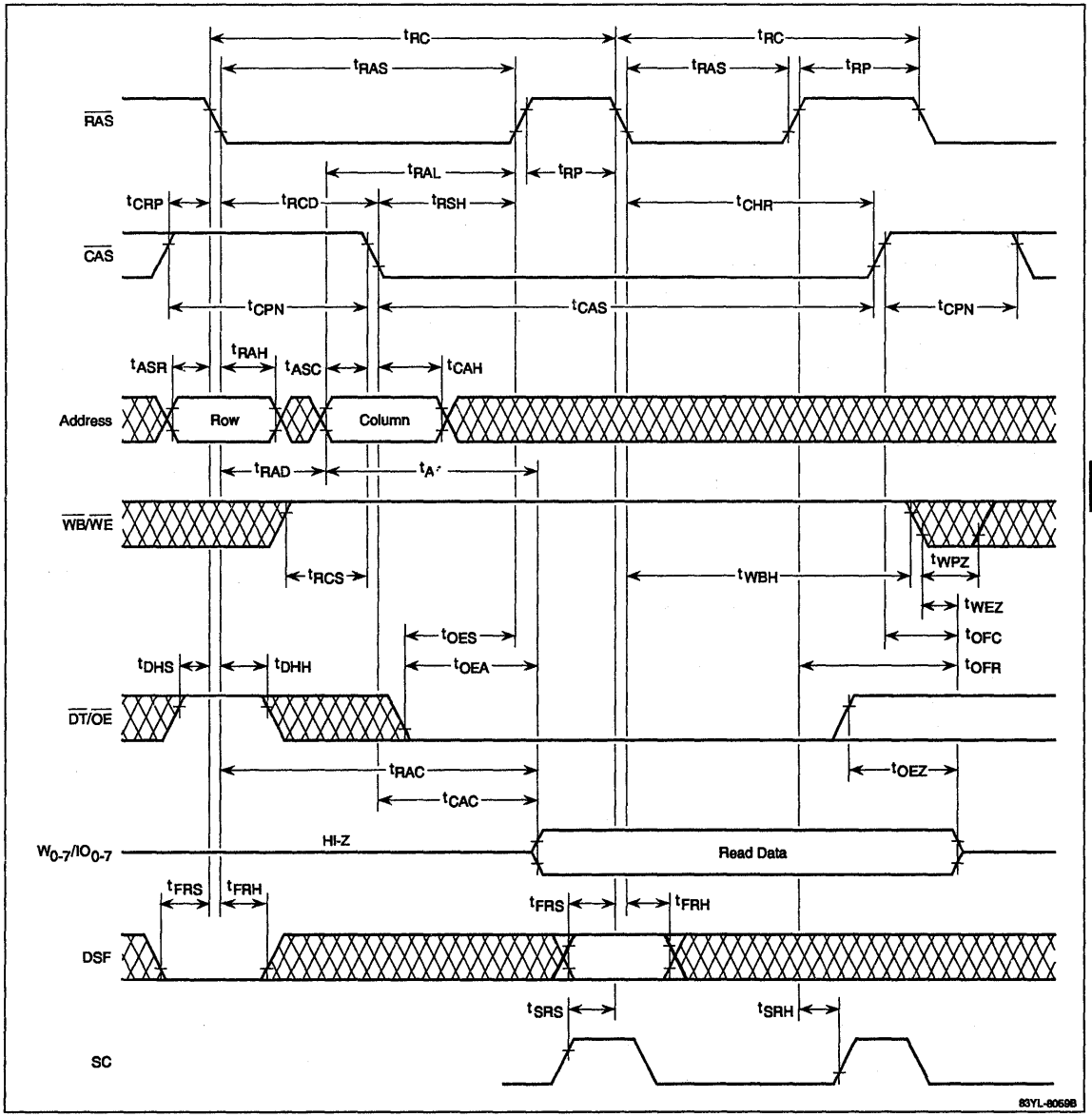
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle With Stop Register Set (CBRS)



Timing Waveforms (cont)

Hidden Refresh Cycle



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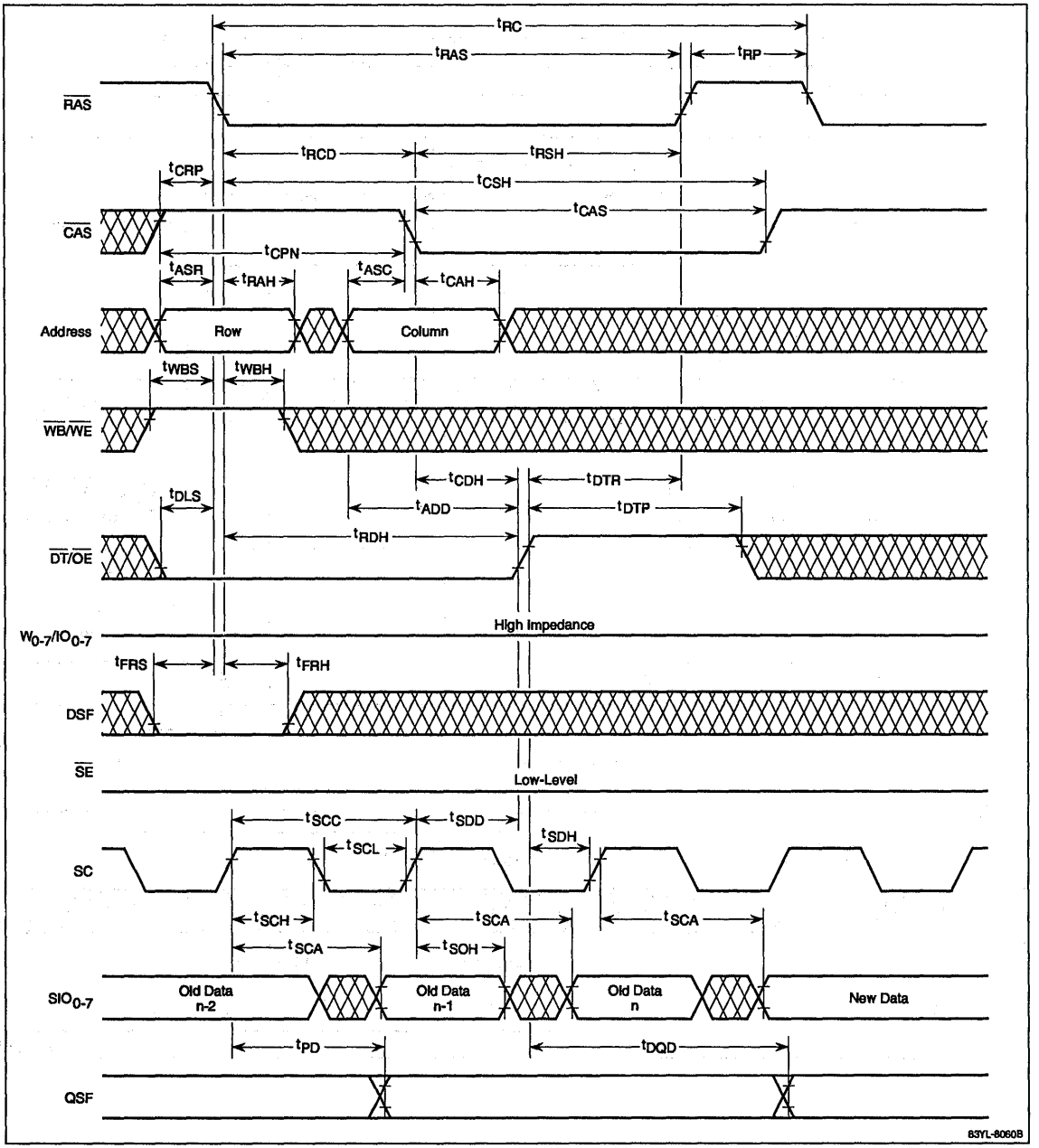
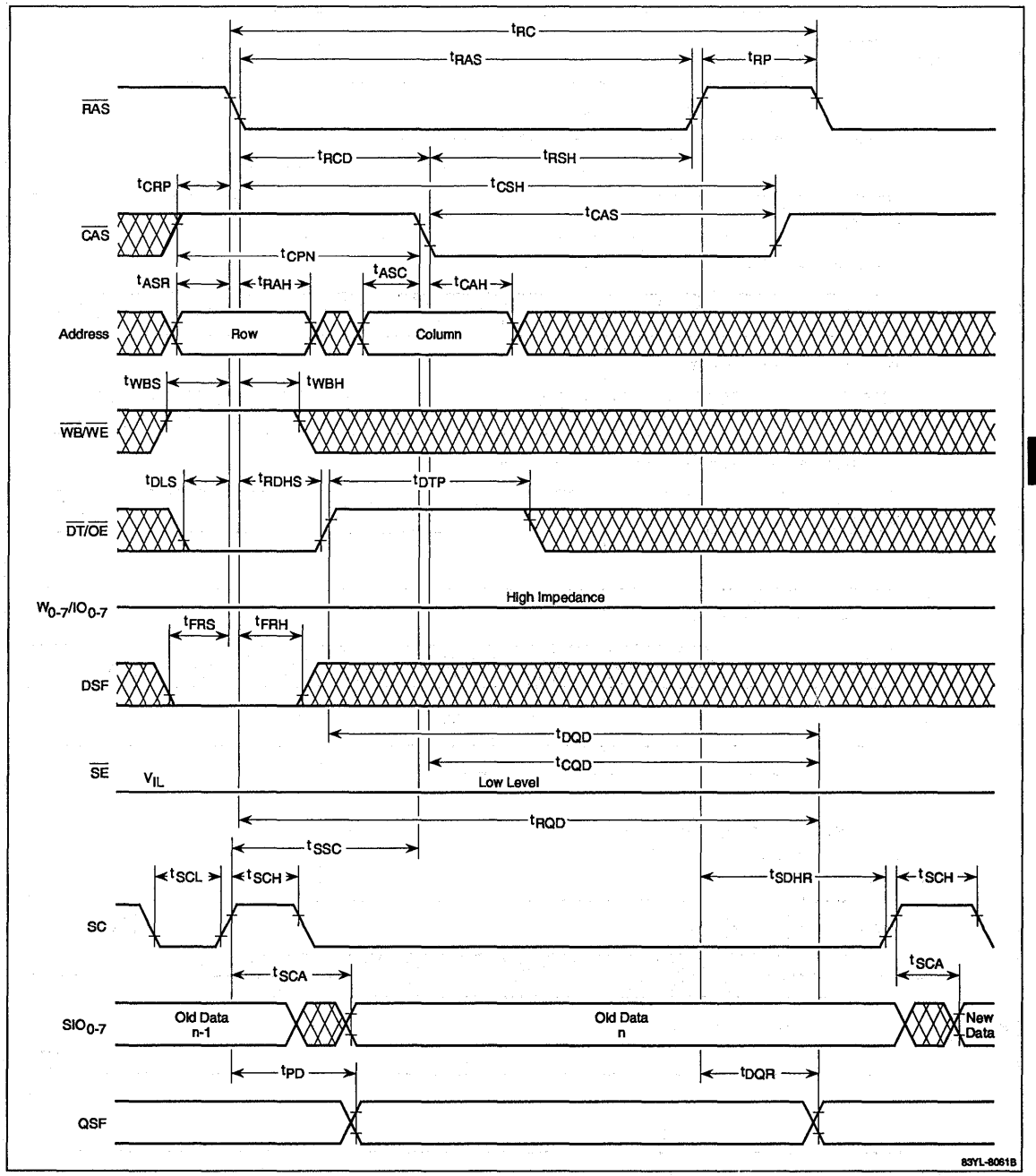
Timing Waveforms (cont)

Data Transfer Cycle With Serial Port Active

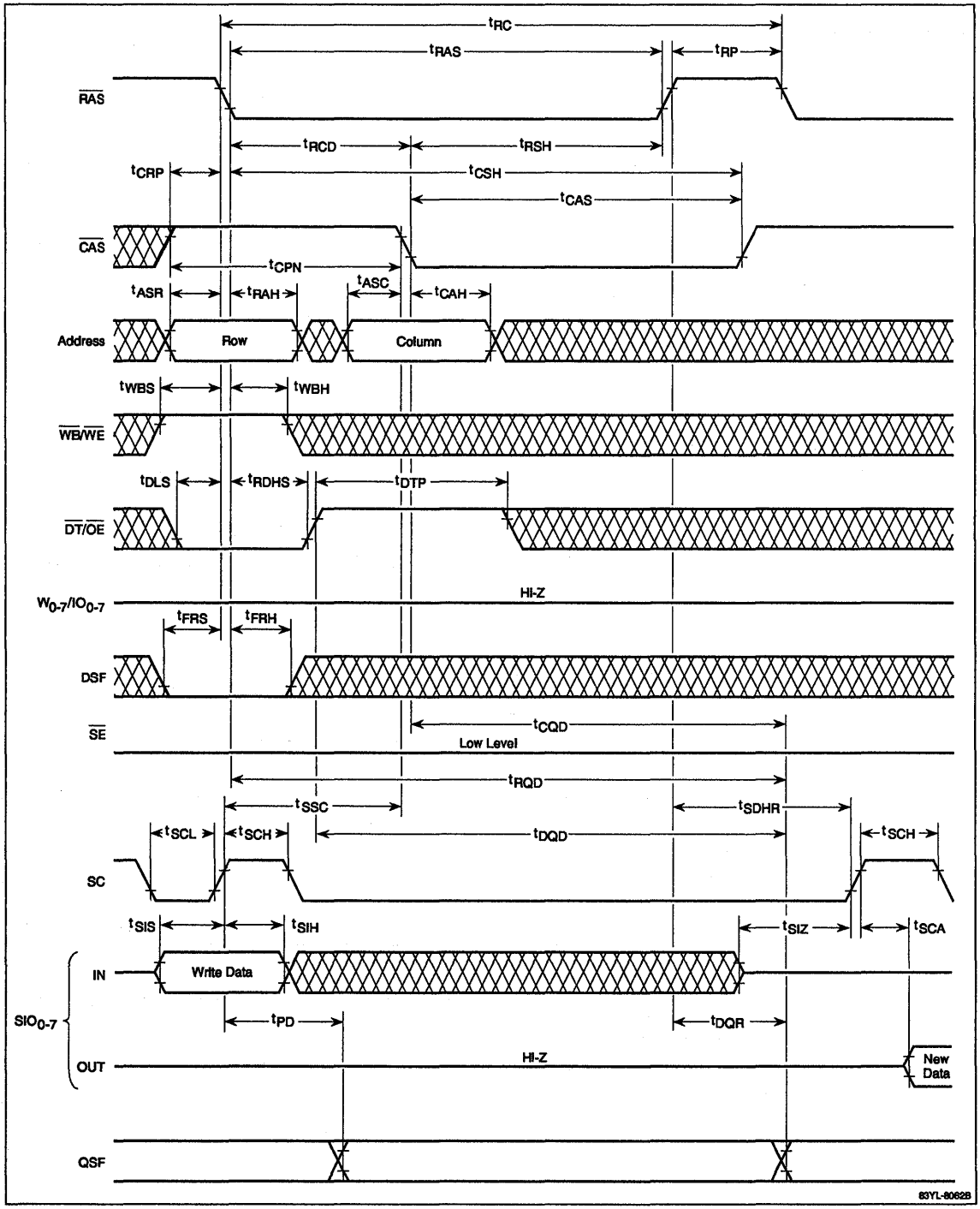


Timing Waveforms (cont)

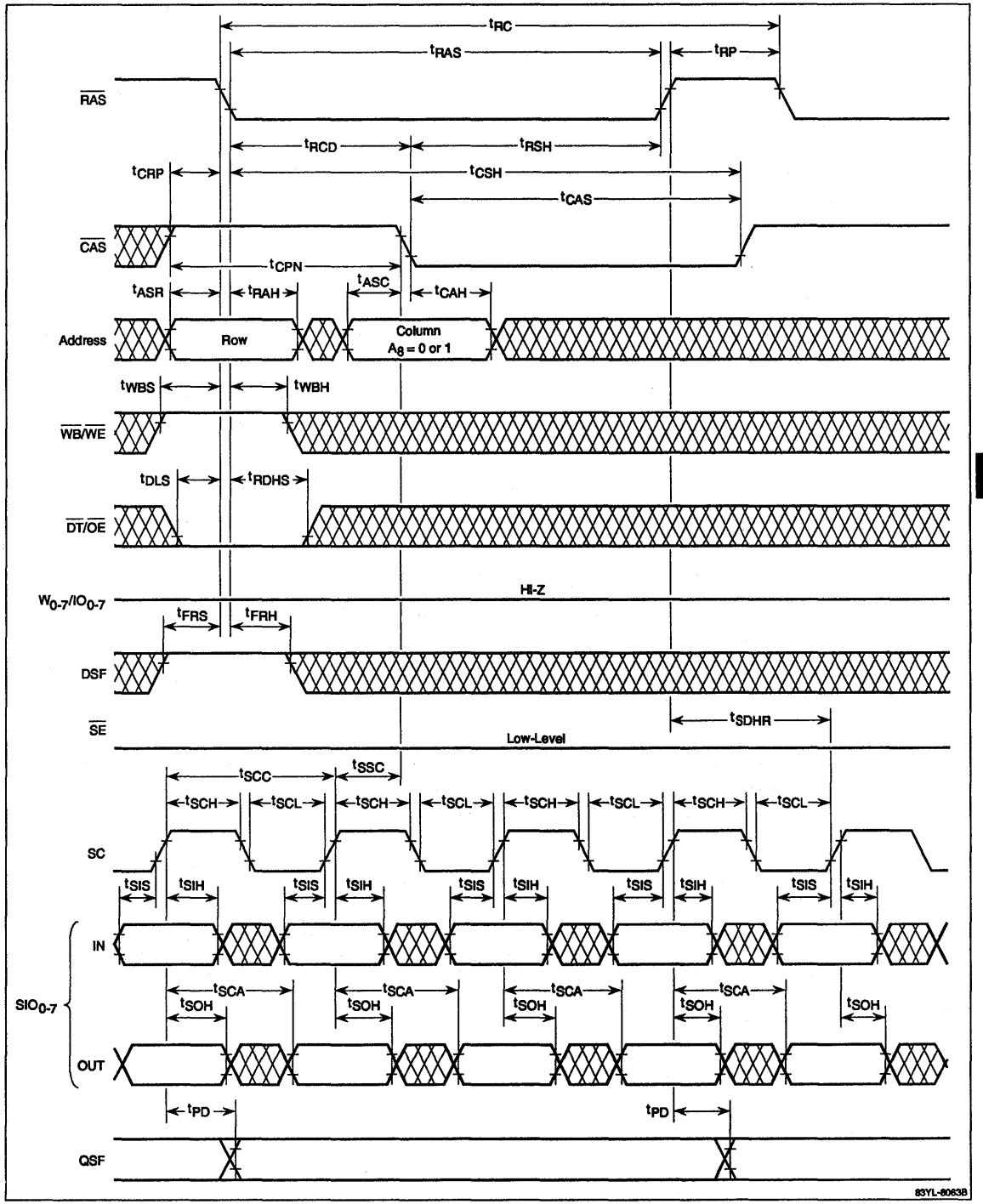
Data Transfer Cycle With Serial Port in Standby



Read Data Transfer Cycle (Serial Write to Read Mode Switch)

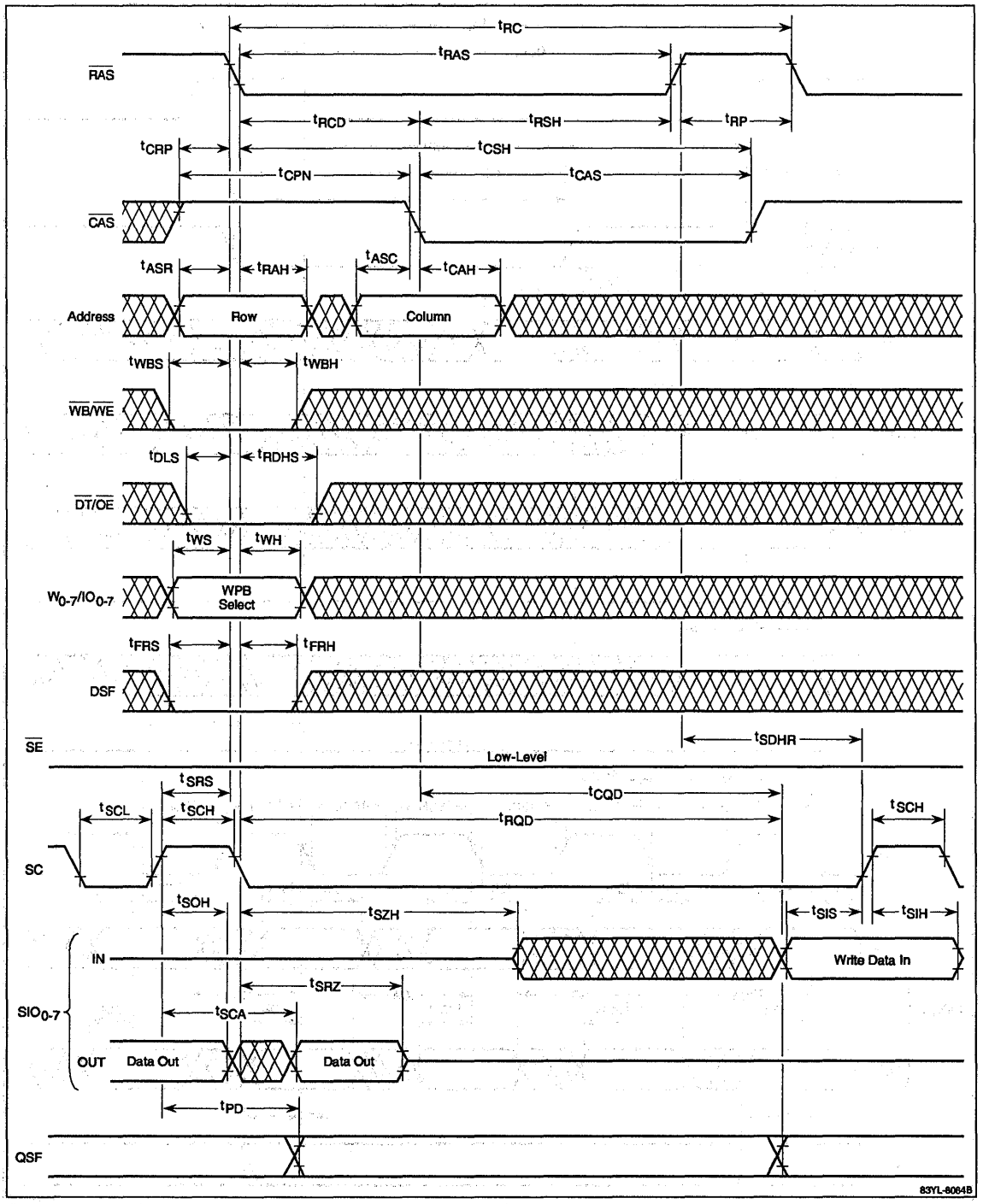


Split Read Data Transfer Cycle



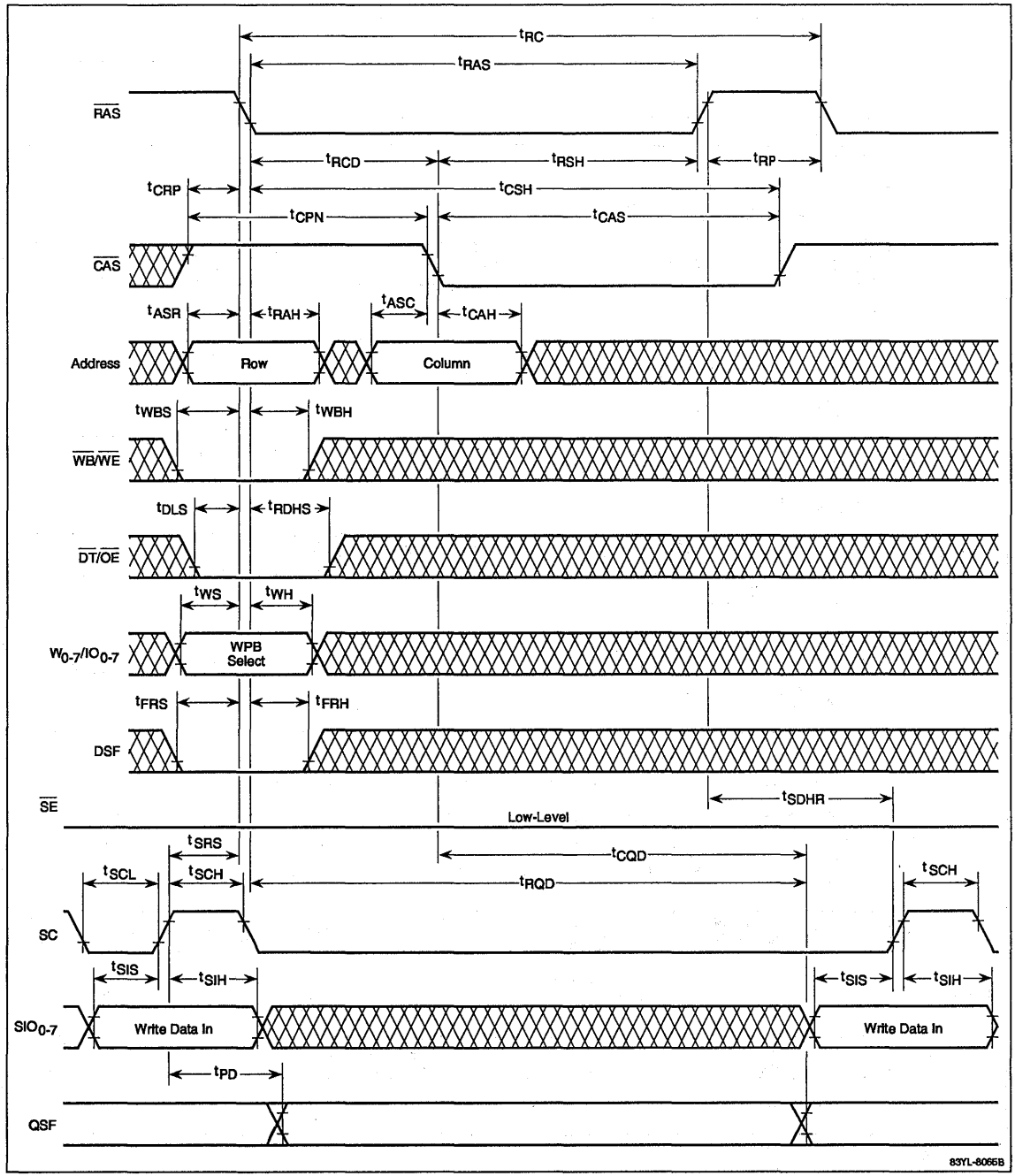
12g

Write Data Transfer Cycle (Serial Read to Write Mode Switch)



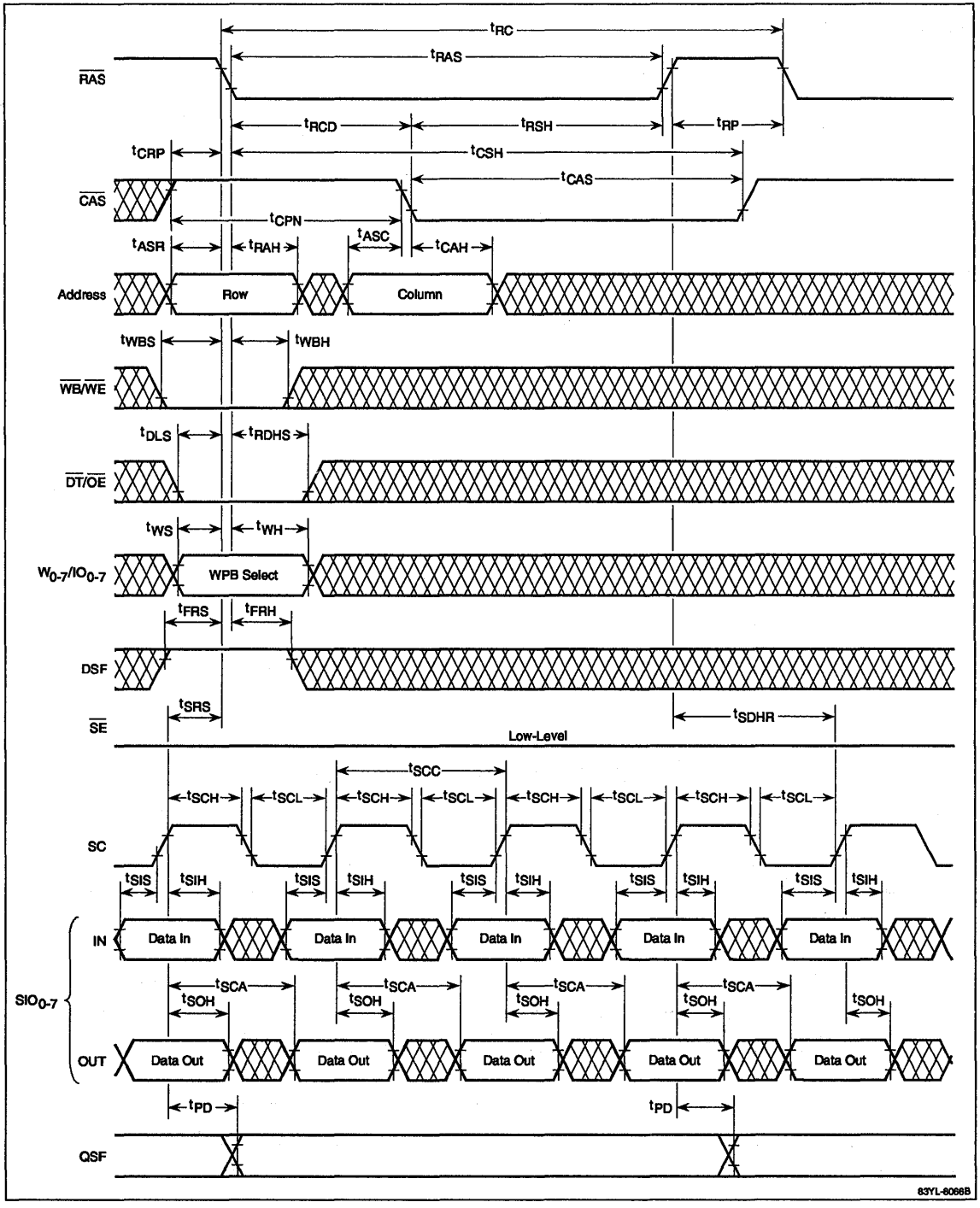
Timing Waveforms (cont)

Write Data Transfer Cycle



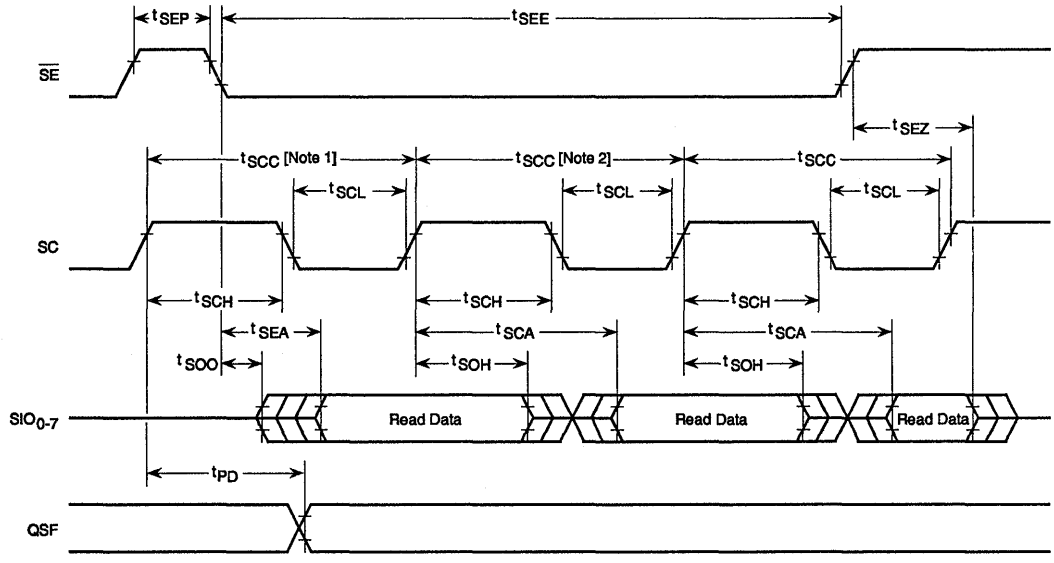
12g

Split Write Data Transfer Cycle



Timing Waveforms (cont)

Serial Read Cycle



Notes:

[1] Last location of split register (Loc: 127 or 255) and boundary address

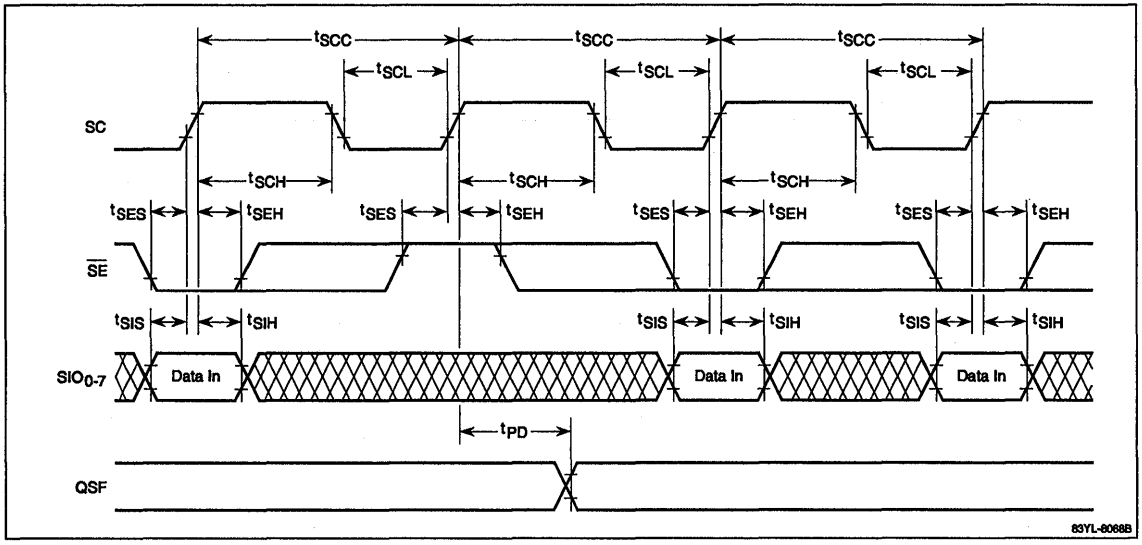
[2] The starting location of newly activated register

83YL-8067B

12g

Timing Waveforms (cont)

Serial Write Cycle



NEC

Section 13
Synchronous DRAM

μPD	Organization	Features	
42116420	4M x 4	3.3-volt	13a
42116820	2M x 8	3.3-volt	
42116920	2M x 9	3.3-volt	
42116162	1M x 16	3.3-volt	
42116182	1M x 18	3.3-volt	

NEC

NEC Electronics Inc.

μPD42116x (x = 420, 820, 920, 162, 182) 16-Megabit Synchronous Dynamic CMOS RAM

Advance Information

Description

The μPD42116x is a synchronous DRAM (SDRAM) using a single 3.3-volt power supply and with all input signals synchronized to an external clock. Commands are given to the SDRAM by a combination of input signals $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, and DQM. The state of these signals is read on the rising edge of the clock. Typical commands are activate, read, write, precharge, and refresh.

The synchronous DRAM family has the following optional memory organizations:

Part Number	Organization
μPD42116420	4M x 4
μPD42116820	2M x 8
μPD42116920	2M x 9
μPD42116162	1M x 16
μPD42116182	1M x 18

Refreshing may be accomplished by any of the following methods: (1) a $\overline{CAS}$ before $\overline{RAS}$ command that internally generates the refresh address; (2) self-refresh, which internally generates both the refresh address and the timing to automatically execute the cycle; (3) a precharge command followed by the activate command with the row address to be refreshed; and (4) normal read and write cycles on the 4096 row address combinations of A_0 - A_{11} during a 32-ms period.

Features

- Fully synchronous DRAM with all signals referenced to a positive clock edge
- Automatic precharge and user-controlled precharge commands
- Ping-pong operation between the two internal memory banks
- 3.3-volt power supply
- LVTTL-compatible inputs and outputs
- Programmable burst-length (1, 2, 4, 8, full-page)
- Sequential or interleave programmable burst sequence
- Programmable $\overline{CAS}$ latency
- Suspend operation
- CBR and self-refresh
- Random column address selectable on every clock cycle

Pin Identification

Symbol	Function
A_0-A_{11}	Address inputs
A_0-A_{11}	Row address inputs
	Column address inputs
A_0-A_9	4M x 4
A_0-A_8	2M x 8, 2M x 9
A_0-A_7	1M x 16, 1M x 18
A_{10}	Enable/disable autoprecharge
A_{11}	Bank select
	Data inputs/outputs
DQ_0-DQ_3	4M x 4
DQ_0-DQ_7	2M x 8
DQ_0-DQ_8	2M x 9
DQ_0-DQ_{15}	1M x 16
DQ_0-DQ_{17}	1M x 18
$\overline{CAS}$	Column address strobe
CKE	Clock enable
CLK	System clock input
$\overline{CS}$	Chip select
DQM	DQ mask enable
LDQM, UDQM	DQ mask enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
V_{CC}	Supply voltage
V_{CCQ}	Supply voltage for DQ
V_{SS}	Ground
V_{SSQ}	Ground for DQ
NC	No connection

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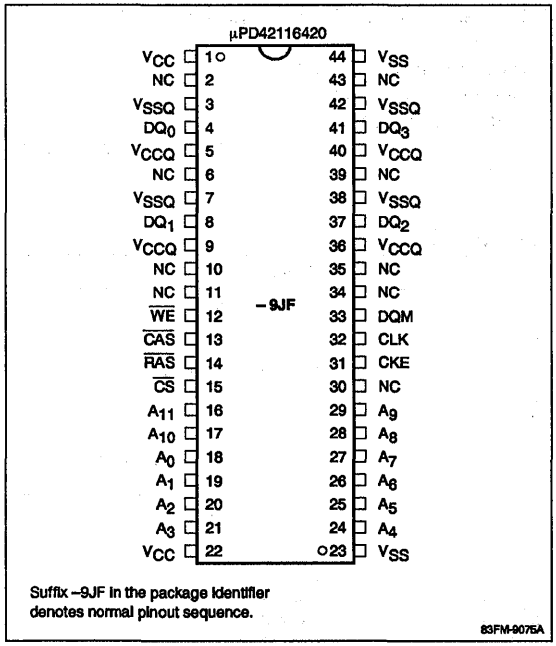
Contact your NEC sales representative for a copy of the complete data sheet.

Pin Configurations

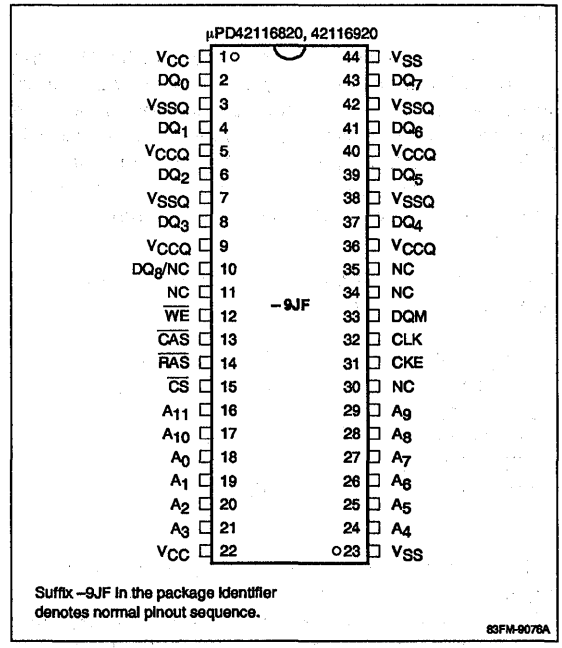
44-Pin TSOP (0.8-mm pitch); 4M x 4 SDRAM



Suffix –9JF in the package identifier denotes normal pinout sequence.

83FM-9075A

44-Pin TSOP (0.8-mm pitch); 2M x 8/9 SDRAM

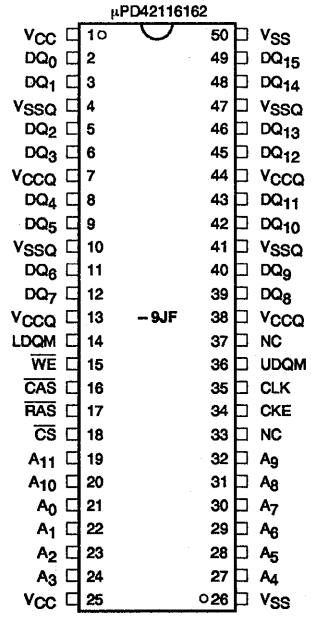


Suffix –9JF in the package identifier denotes normal pinout sequence.

83FM-9076A

Pin Configurations (cont)

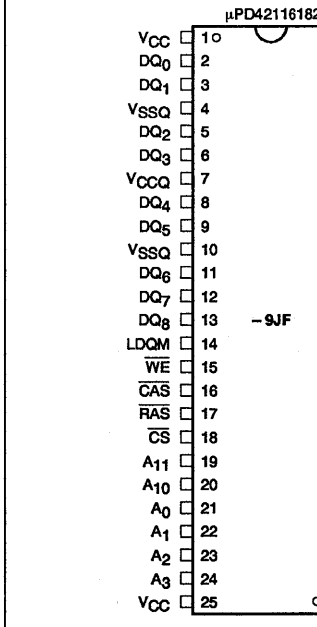
50-Pin TSOP (0.8-mm pitch); 1M x 16 SDRAM



Suffix –9JF in the package identifier denotes normal pinout sequence.

83FM-9077A

50-Pin TSOP (0.8-mm pitch); 1M x 18 SDRAM



Suffix –9JF in the package identifier denotes normal pinout sequence.

83FM-9102A

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Signal Description

Name	Function
A	Address lines
A_{10}	Address bit A_{10}, when $\overline{CAS}$ is active, enables/disables autoprecharge.
A_{11}	Address bit A_{11} selects which of the two memory banks is to be used.
$\overline{CAS}$	$\overline{CAS}$ is part of the input command to the SDRAM. See truth table for details.
CKE	Clock enable disables the clock internally, thus allowing data to remain on the output for several clock cycles. Clock enable is also used as part of the input command to specify self-refresh.
CLK	The positive edge of the clock input strobes the commands placed on the input lines. It is also used by the system to strobe output data from the SDRAM.
$\overline{CS}$	Command select indicates that the command on the input lines is for this device. If command select is inactive, the input command will be ignored.
DQ	Data input/output lines transfer data between the memory array and the system bus.
DQM	Data output mask turns off the output buffers during a read. During a write, DQM active prevents a write to the current memory location.
LDQM	Data output mask turns off the lower byte of the output buffers during a read (x16 and x18 devices only). During a write, DQM active prevents a write to the lower byte of the current memory location.
UDQM	Data output mask turns off the upper byte of the output buffers during a read (x16 and x18 devices only). During a write, DQM active prevents a write to the upper byte of the current memory location.
$\overline{RAS}$	$\overline{RAS}$ is part of the input command to the SDRAM. See truth table for details.
$\overline{WE}$	Write enable is part of the input command. See truth table for details

Commands (figure 3)

Activate. This command is very similar to activating $\overline{RAS}$ in a standard DRAM. The activate command selects a row in either memory bank A or bank B (selected by address bit A_{11}); the data in all memory cells in that row is read by the sense amplifiers. This operation destroys the data in the memory cells. Before another row in the same memory bank is selected, a precharge command must be executed to restore the data in memory cells.

Burst Stop. When a full-page burst length is specified, the synchronous DRAM will continuously output data on each clock. The burst stop command allows the data stream to be terminated. The burst will terminate after one additional piece of data has been output. The command for burst stop is $\overline{CS}$ and $\overline{WE}$ low; CKE, $\overline{RAS}$, and $\overline{CAS}$ high.

Precharge. This command is similar to transitioning $\overline{RAS}$ from an active state to an inactive state in a standard DRAM. Precharge causes the data in the sense amplifiers to be rewritten into the memory cells. It also initializes the sense amplifiers in preparation for reading another row in the memory array. See figure 4.

Read. Transfers data from the selected sense amplifier to the output buffer as determined by the column address. During each succeeding clock, new data will be output without additional read commands. See figures 8, 9, and 10.

Refresh. Similar to $\overline{CAS}$ before $\overline{RAS}$ refresh in a standard DRAM. This command causes a row to be read in both memory banks as determined by the refresh row address counter. After being read, the row is automatically rewritten back into the memory cell. Before execution of this command, both memory banks must be in a precharged state.

Register Set. This command allows setting different options for the SDRAM. The options include (1) burst length and type, (2) enable or disable autoprecharge, and (3) number of latency cycles between a read command and data availability. See figures 5, 6, and 7.

Self-Refresh. Same as refresh except that it is used when the device will be in standby for a very long time, such as when system power is turned off. In this case, self-refresh will automatically generate internal refresh cycles to keep the data in both memory banks refreshed. Before execution of this command, both memory banks must be in a precharged state.

Write. Transfers data from the output buffer to the selected sense amplifier as determined by the column address. During each succeeding clock, new data will be input without additional write commands. See figure 9.

Glossary

Autoprecharge. At the end of a burst (either read or write), a precharge will be executed without the system having to execute a precharge command.

Bank of Memory. One or more memory arrays within a chip that can be controlled independently but share common control, address, and data lines. NEC's SDRAM has two banks of memory on each chip.

Burst Length. The amount of data that will be sequentially accessed for each read or write command prior to automatic termination of the command. The burst length is programmable. See figure 5.

Burst Wrap. The order in which data will be automatically accessed from a single bank during a burst by the device. This order can be either sequential or interleaved. Some microprocessor cache systems are optimized for sequential and others are optimized for interleaved. See figures 1and 5 for details.

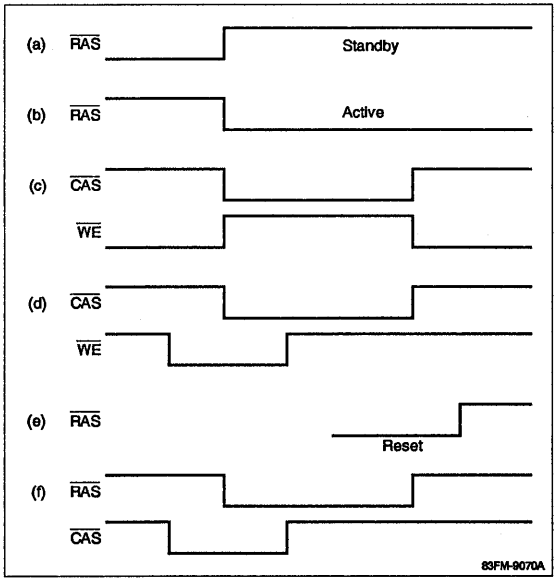
Latency. Number of clocks after the clock that initiates a command before the action takes place. For example, a $\overline{CAS}$ latency of 2 means that on the second clock after the $\overline{CAS}$ signal has been clocked in, data will be valid on the output.

Ping-Pong. Having two or more internal banks of memory active and being able to access data from any bank of memory without having to wait for both a $\overline{RAS}$ and a $\overline{CAS}$ latency to elapse before data is available. Figure 10 is an example of ping-ponging between the two memory banks.

Figure 1. Address Sequence Example

Burst Length (BL)	Burst Type: Sequential BT = 0	Burst Type: Interleave BT = 1
1 (000)	No burst	No burst
2 (001)	0-1 1-0	0-1 1-0
4 (010)	0-1-2-3 1-2-3-0 2-3-0-1 3-0-1-2	0-1-2-3 1-0-3-2 2-3-0-1 3-2-1-0
8 (011)	0-1-2-3-4-5-6-7 1-2-3-4-5-6-7-0 2-3-4-5-6-7-0-1 3-4-5-6-7-0-1-2 4-5-6-7-0-1-2-3 5-6-7-0-1-2-3-4 6-7-0-1-2-3-4-5 7-0-1-2-3-4-5-6	0-1-2-3-4-5-6-7 1-0-3-2-5-4-7-6 2-3-0-1-6-7-4-5 3-2-1-0-7-6-5-4 4-5-6-7-0-1-2-3 5-4-7-6-1-0-3-2 6-7-4-5-2-3-0-1 7-6-5-4-3-2-1-0
Full page (111)	Ys,Ys+1,Ys+2,... ,Yf,0,1,2,.. ,Ys,Ys+1,Ys+2,...	No support

Figure 2. DRAM Control Timing



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SDRAM Function Truth Table

Operation	CKE Pre	CKE Cur	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A_{11}	A_{10}	A_{9-0}	Mnemonic	DRAM Equiv (Fig 2)
Mode register set	H	X	L	L	L	L	X	Opcode + mode			MRS	
CBR refresh	H	H	L	L	L	H	X	X	X	X	REFR	(f)
Entry self-refresh	H	L	L	L	L	H	X	X	X	X	SRENT	(f)
Single-bank deactivate/precharge	H	X	L	L	H	L	X	BS	L	X	PRE	(e)
Precharge all banks	H	X	L	L	H	L	X	X	H	X	PALL	
Bank activate	H	X	L	L	H	H	X	Row address			ACTV	(b)
Write	H	X	L	H	L	L	X	BS	L	Col	WRITE	(d)
Write and autoprecharge	H	X	L	H	L	L	X	BS	H	Col	WRITEA	
Read	H	X	L	H	L	H	X	BS	L	Col	READ	(c)
Read and autoprecharge	H	X	L	H	L	H	X	BS	H	Col	READA	
Reserved (Burst stop in full-page)	H	X	L	H	H	L	V(X)	V(X)	V(X)	V(X)	R*(BST)	
No operation	H	X	L	H	H	H	X	X	X	X	NOP	
Device deselect	H	X	H	X	X	X	X	X	X	X	DESL	(a)
Clock suspend/ Standby mode	L	X	X	X	X	X	X	X	X	X	HOLD	
Data write/Output enable	H	X	X	X	X	X	L	X	X	X	ENBL	
Data mask/Output disable	H	X	X	X	X	X	H	X	X	X	MASK	

Legend

BS	Bank select	V	Valid
Col	Column address	H	Logic high
Cur	Current clock	L	Logic low
Pre	Previous clock	X	Don't care

Notes:

(1) All inputs are latched on the rising edge of CLK.

(2) MRS and REFR commands should be issued only after both banks are deactivated (PRE command).

(3) The ACTV command should be issued only after the corresponding bank has been deactivated (PRE command).

(4) WRITE and READ commands should be issued only after the corresponding bank has been activated (ACTV command).

(5) The BST command is valid only in the Full Page mode.

Absolute Maximum Ratings

Voltage on power supply pin relative to GND	−1.0 to +4.6 V
Voltage on input pin relative to GND	−1.0 to +7.0 V
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	5	pF	CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, LDQM, UDQM
Data input/output capacitance	C_O	7	pF	DQ_0 - DQ_{17}

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input voltage, high	V_{IH}	2.0		5.5	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Ambient temperature	T_A	0		70	°C

DC Characteristics

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$I_{I(L)}$	−1		1	μA	V_{IN} = 0 to 3.6 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−1		1	μA	D_{OUT} disabled; V_{OUT} = 0 to 3.6 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −2 mA

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DC Current Requirements

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	-10	-15	-20	Unit	Test Conditions
Operating current	I_{CC1}	80	70	60	mA	Burst length = 1; $t_{RAS} \geq t_{RAS}$ (min); $t_{RP} \geq t_{RP}$ (min); I_O = 0 mA (Note 1)
Precharge standby current in power-down mode	I_{CC2P}	3	3	3	mA	CKE ≤ V_{IH} (max); t_{CK} = 15 ns
	I_{CC2PS}	2	2	2	mA	CKE ≤ V_{IH} (max); t_{CK} = ∞
Precharge standby current in non-power-down mode	I_{CC2N}	15	15	15	mA	CKE ≥ V_{IL} (min); t_{CK} = 15 ns Input signals are changed once during 30 ns.
	I_{CC2NS}	6	6	6	mA	CKE ≥ V_{IL} (min); t_{CK} = ∞ Input signals are stable.
Active standby current in power-down mode	I_{CC3P}	4	4	4	mA	CKE ≤ V_{IH} (max); t_{CK} = 15 ns
	I_{CC3PS}	3	3	3	mA	CKE ≤ V_{IH} (max); t_{CK} = ∞
Active standby current in non-power-down mode	I_{CC3N}	16	16	16	mA	CKE ≥ V_{IL} (min); t_{CK} = 15 ns Input signals are changed once during 30 ns.
	I_{CC3NS}	7	7	7	mA	CKE ≥ V_{IL} (min); t_{CK} = ∞ Input signals are stable.
Operating current in burst mode	I_{CC4}	120	80	60	mA	$t_{CK} \geq t_{CK}$ (min); I_O = 0 mA (Note 1)
Refresh current	I_{CC5}	80	70	60	mA	$t_{RC} \geq t_{RC}$ (min)
Self-refresh current	I_{CC6}			2	mA	CKE ≤ V_{CC} - 0.2 V (Standard device)
				0.1	mA	CKE ≤ V_{CC} - 0.2 V (Low-power device)

Note:

(1) I_{CC1} and I_{CC4} depend on output loading and cycle rates. Specified values are obtained with the output open. Address inputs are assumed to be switched only once during each clock cycle.

AC Characteristics

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	-10 Min	-10 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit	Test Conditions
Access time (DQ) from CLK ↑	t_{IAC}		8		13		18	ns	(Note 5)
Address, BS hold time	t_{AH}	2		3		4		ns	
Address, BS setup time	t_{AS}	2		2		2		ns	
CLK high-level width	t_{CH}	3		4		5		ns	
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	2		3		4		ns	
System clock (read, write) cycle time	t_{CK}	10		15		20		ns	
CKE hold time	t_{CKH}	2		3		4		ns	
CKE setup time	t_{CKS}	2		2		2		ns	
CLK low-level width	t_{CL}	3		4		5		ns	
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2		2		2		ns	
Data-in hold time	t_{DH}	2		3		4		ns	
Data-in to Pre command period	t_{DPL}	$\overline{CAS}$ latency		$\overline{CAS}$ latency		$\overline{CAS}$ latency		ns	
Data-in setup time	t_{DS}	2		2		2		ns	
Data-out high-impedance time	t_{HZ}	4		4		4		ns	
Data-out low-impedance time	t_{LZ}	5		5		5		ns	
Data-out hold time	t_{OH}	4		4		4		ns	
Active to Pre-command period	t_{RAS}	70	120,000	75	120,000	80	120,000	ns	
Ref to Ref/Active command period	t_{RC}	100		115		140		ns	
Refresh period	t_{REF}		32		32		32	ms	
Pre to Active command period	t_{RP}	30		40		60		ns	
Active (A) to Active (B) command period	t_{RRD}	20		30		40		ns	
Transition time	t_T	1	30	1	30	1	30	ns	

Notes:

(1) All voltages referenced to V_{SS} (ground)

(2) An initial pause of 100 μs is required after power-up followed by eight refresh cycles before proper device operation is achieved.

(3) Ac measurements assume t_T = 1 ns.

(4) Reference level for measuring timing of input signals is 1.50 V. Transition times are measured between V_{IH} and V_{IL}.

(5) Access time is measured at 1.50 V and loading condition is 2TTL + 100 pF (at less than 50 MHz), 2TTL + 50 pF (50 to 75 MHz), or 2TTL + 30 pF (above 75 MHz).

Figure 3. Commands

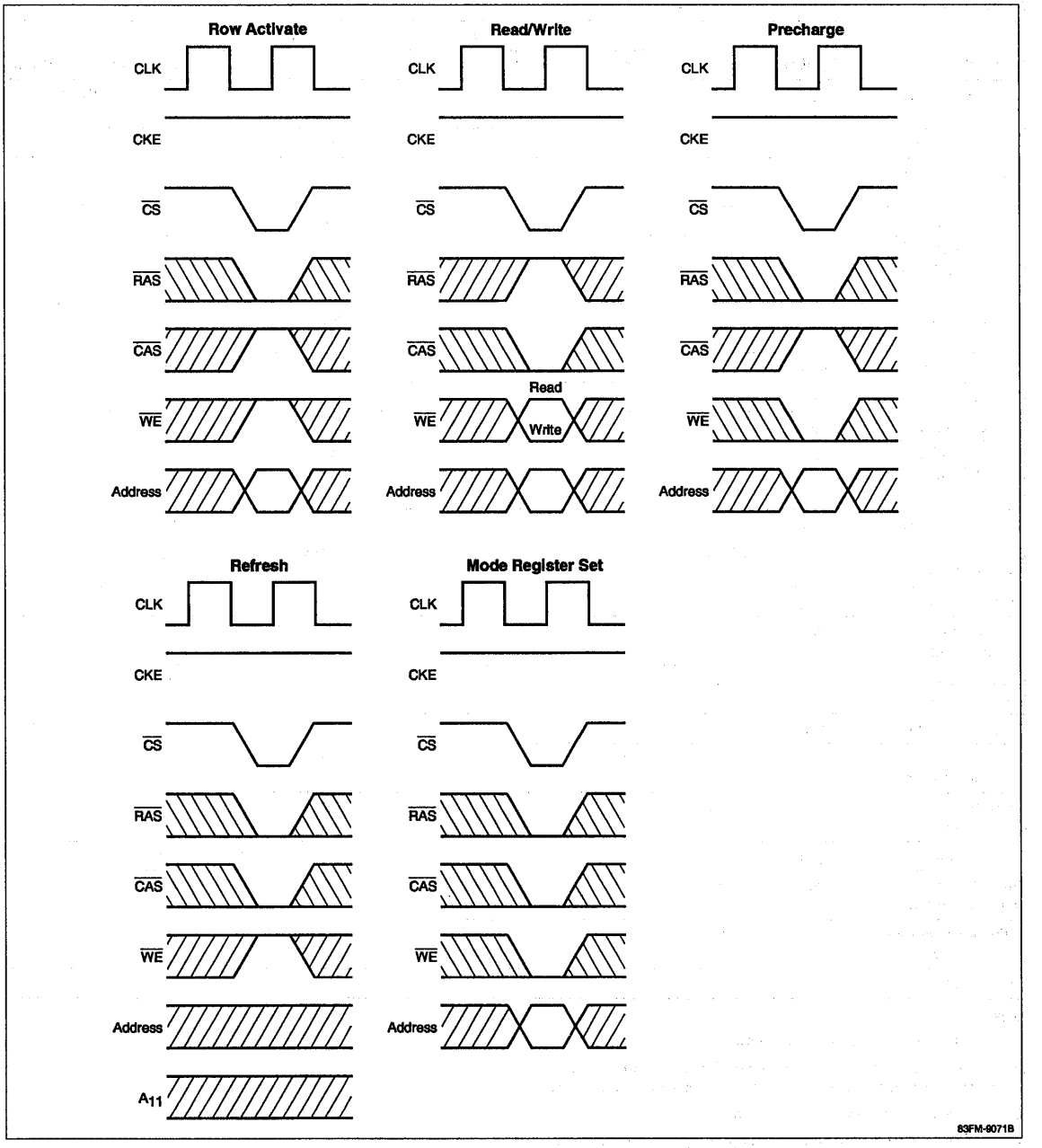
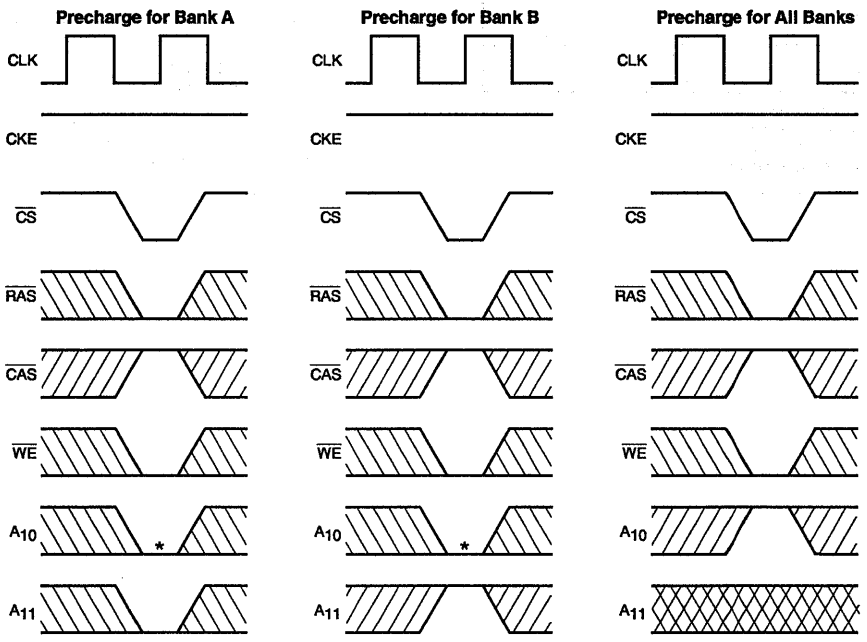


Figure 4. Precharge Options

	X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7	X_8	X_9	X_{10}	X_{11}
Row												
Column	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}

X_{10}	0	Disable	Precharge command for all banks
	1	Enable	
X_{11}	0	Bank A	Enables activate/precharge/refresh commands for bank
	1	Bank B	
Y_{10}	0	Disable	Autoprecharge (end of burst)
	1	Enable	
Y_{11}	0	Bank A	Enables read/write commands for bank
	1	Bank B	



*A_{10} = Low is standard

83FM-9074B

Figure 5. Mode Register Options

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	LTMODE			BT	BL		

Latency Mode

LTMODE	CAS Latency
000	R
001	1
010	2
011	3
100	R
101	R
110	R
111	R

Burst Type

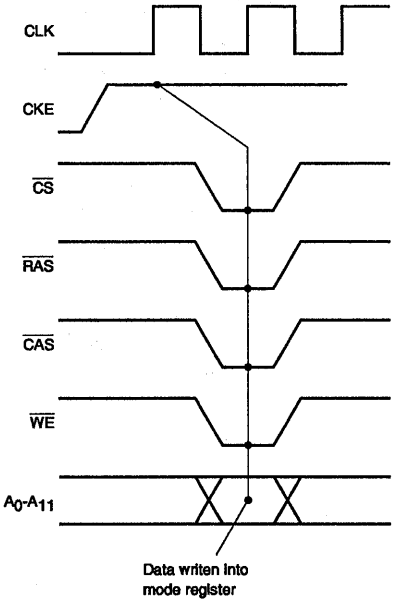
BT	Burst Type
0	Sequential
1	Interleave

Burst Length

BL	BT=0	BT=1
000	1	R
001	2	R
010	4	4
011	8	8
100	R	R
101	R	R
110	R	R
111	Full page	R

R = Reserved
BL = Burst length
BT = Burst type
LTMODE = Latency mode

Mode-Register Write Timing



Note: A_0-A_{11} are used as data input lines when writing the mode register

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Figure 6. Mode Register Options (Additional)

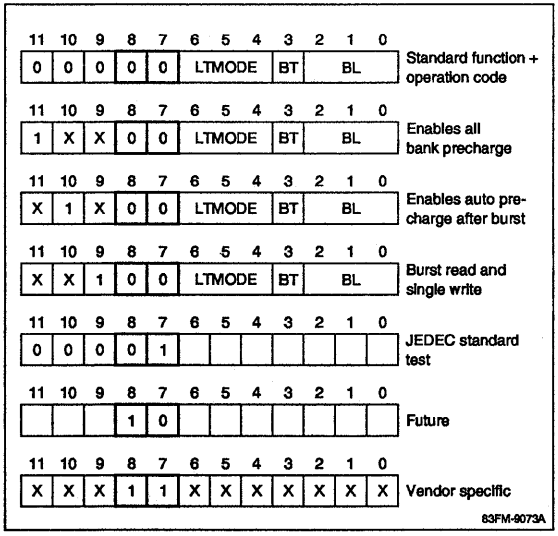

Figure 7. Frequency vs. Latency

Speed Version	-10				-15				-20			
Frequency (MHz)	100	66	50	33	100	66	50	33	100	66	50	33
Clock cycle time (ns)	10	15	20	30	10	15	20	30	10	15	20	30
$\overline{CAS}$ latency	3	2	2	1		3	2	2		3	2	2
(t_{RCD})	3	2	2	1		2	2	1		3	2	2
$\overline{RAS}$ latency ($\overline{CAS}$ latency + (t_{RCD}))	6	4	4	2		5	4	3		6	4	4
(t_{RC})	10	7	6	4		8	6	5		10	7	5
(t_{RAS})	7	5	4	3		5	4	3		6	4	3
(t_{RP})	3	2	2	1		3	2	2		4	3	2
(t_{DPL})	3	2	2	1		3	2	2		3	2	2

13a

Figure 8. Random Column Read Cycle

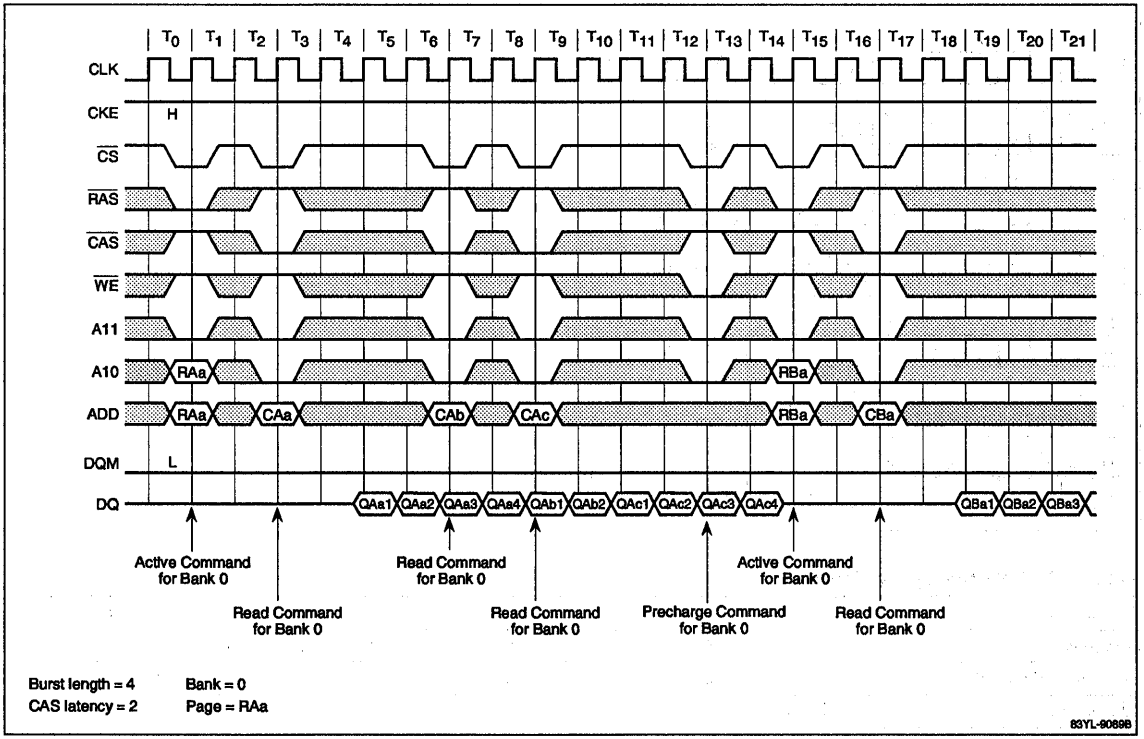

Figure 9. Read and Write Cycle

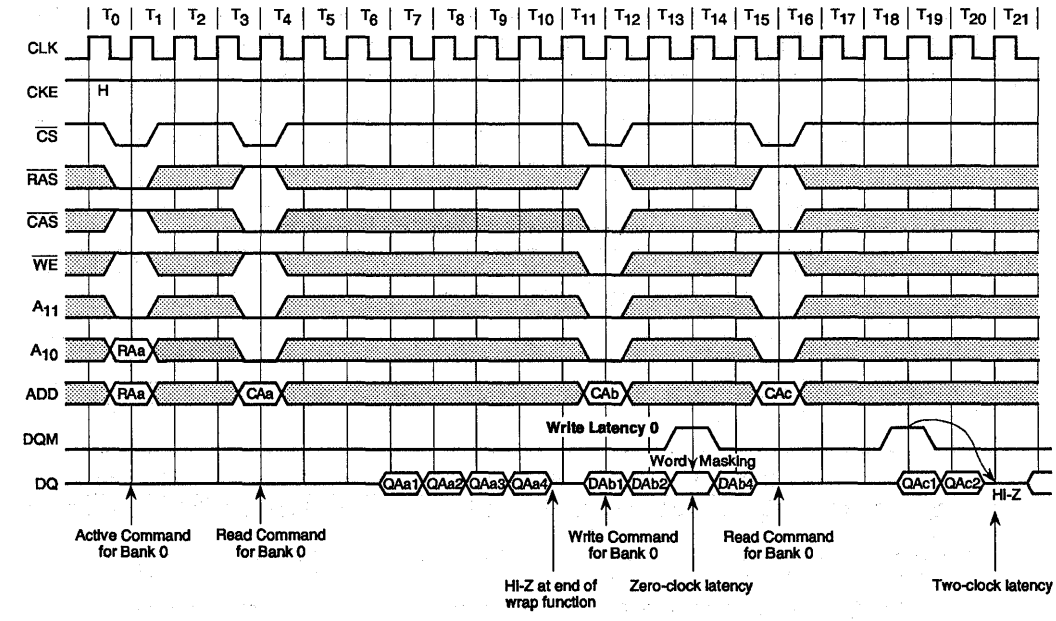

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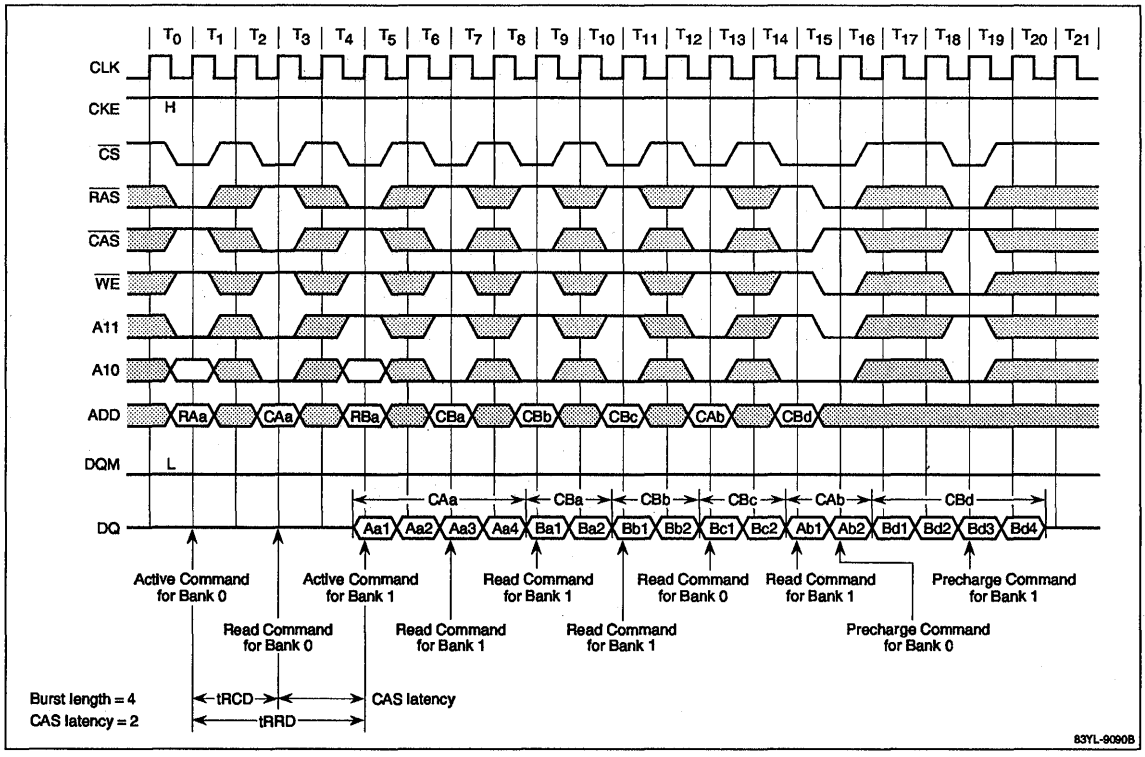
Figure 10. Interleaved Column Read Cycle



NEC

Section 14
Rambus DRAM

μPD	Organization	Features	
488130	2M x 8	3.3-volt	14a
488170	2M x 9	3.3-volt	

NEC Electronics Inc.

μPD488130, 488170
18-Megabit Rambus DRAM

Advance Information

Description

The μPD488130 and μPD488170 Rambus™ DRAMs (RDRAM™) are extremely-high-speed dynamic CMOS RAMs organized as 2M words by 8 or 9 bits. Using its sense amplifiers as a cache, the RDRAM bursts up to 256 bytes at a 500-megabyte/second rate. The RDRAM is ideal for main memory and graphics applications that require high performance at low cost.

Features

- Rambus interface
  - — 500-megabits/second peak bandwidth per RDRAM per bus
  - — Innovative, small-signal-swing interface
  - — Synchronous, block-oriented protocol
  - — Direct interface to Rambus ASICs, MPUs, and peripherals
- 28 ns from end of read request to first byte; 2 ns/byte thereafter
- Caches in RDRAM contribute to low latency
- Entirely self-contained—no external memory controller required
- Conventional plastic surface-mount package and PC board technology
- On-board registers for flexible addressing

System Benefits

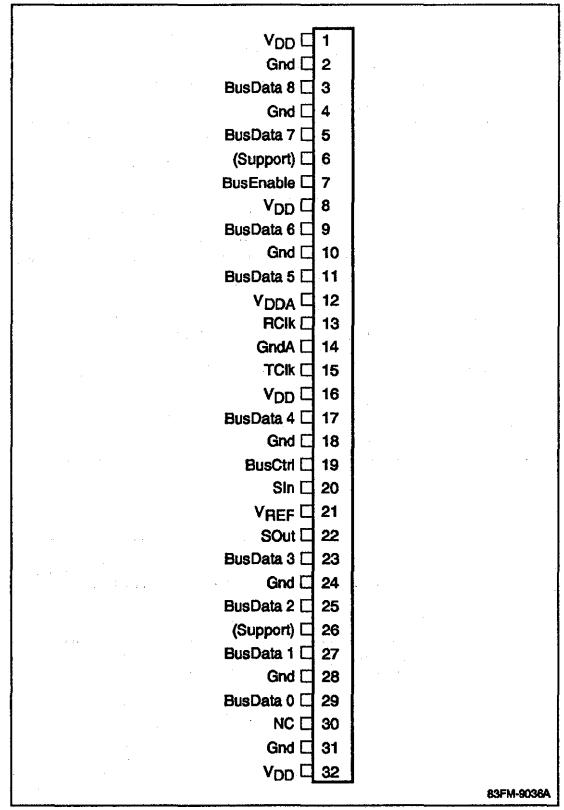
- Can eliminate second-level caches in uniprocessor designs
- Vastly improves graphics at lower cost
- Decreases parts count; eliminates memory controller, buffers, address decoders, etc.
- Same pinout as a 4.5-megabit RDRAM
- Incremental memory granularity is 2 megabits
- Alleviates need for expensive multichip modules at high system clock rates
- Systems can be modular; faster MPUs and larger Rambus memories can be installed without changing board layout or logic design
- Write-per-bit function available

Ordering Information

Part Number	Organization	Package
μPD488130	2M x 8 bits	32-pin SVP
μPD488170	2M x 9 bits	

Pin Configuration

32-Pin Surface Vertical Package



14a

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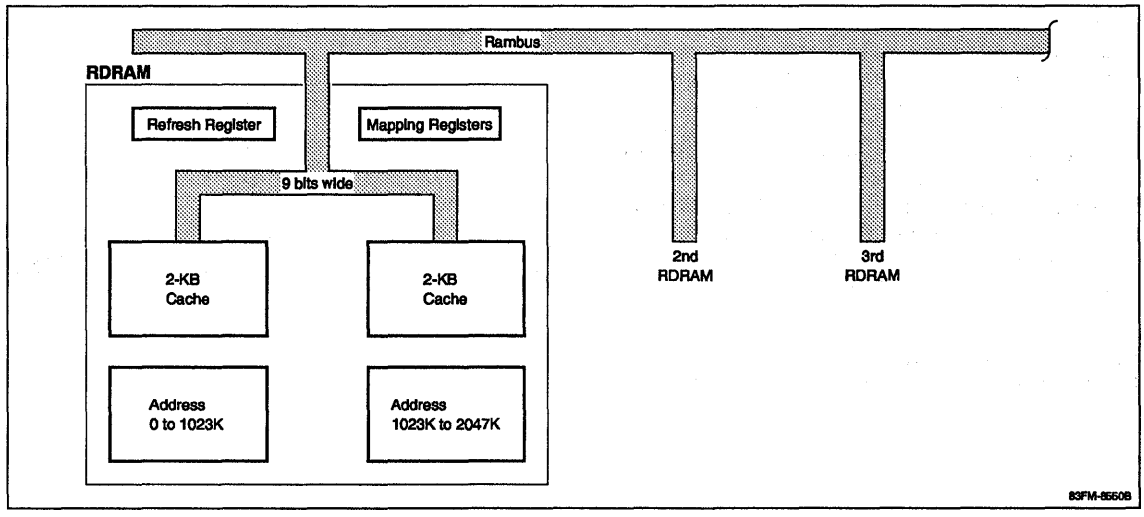
Rambus interface is used under license from Rambus Inc.

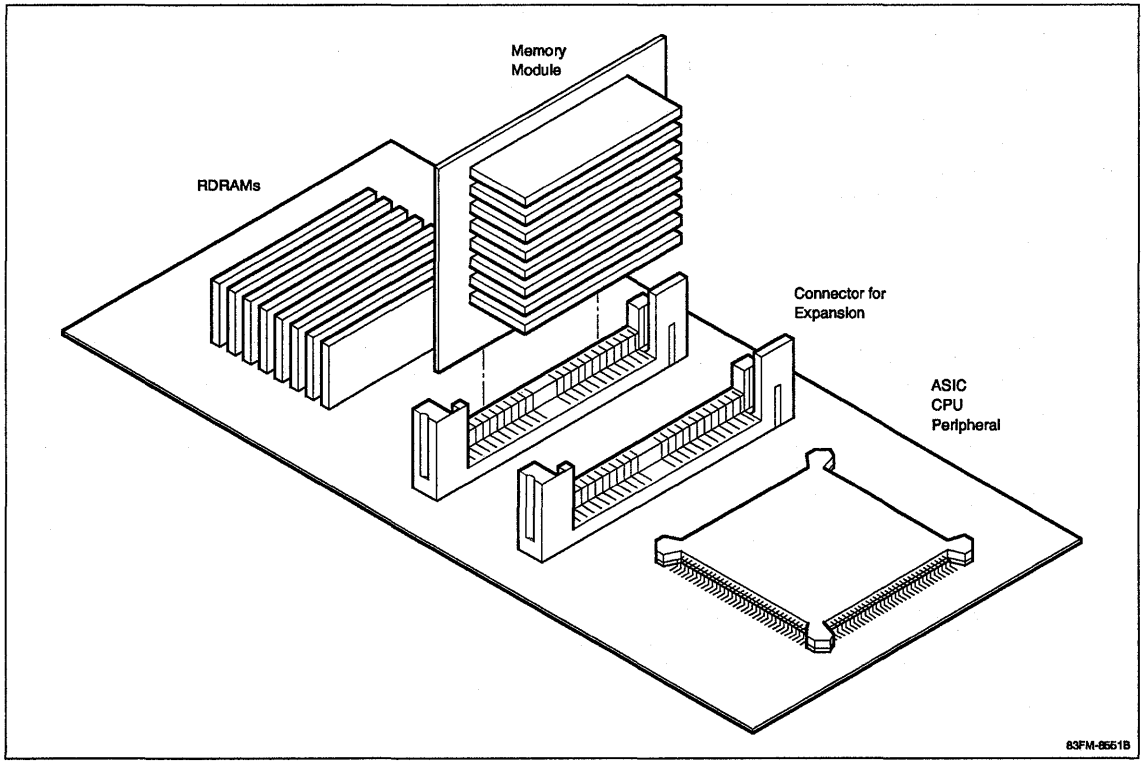
Pin Identification

Signal	I/O	Description
BusData0 - BusData8	I/O	Bus data for request, write, and read protocols. These are low-swing signals referenced to V_{REF}. The data lines carry the request packet with the address, operation codes, and the count of the bytes to be transferred.
RClk	In	Receive clock. RClk is aligned with incoming request and write data packets. The clock is completely synchronized with the request and data sent out on the Rambus interface.
TClk	Out	Transmit clock. TClk is aligned with the data being sent out on reads as well as the acknowledge packets. The clock is a low-swing signal referenced to V_{REF}.
V_{REF}	In	This is the logic threshold voltage for low-swing signals.
$\overline{\text{BusCtrl}}$	In	Control signal to frame packets, transmit opcode, and acknowledge requests. Signal is active low.
$\overline{\text{BusEnable}}$	In	Control signal to enable the bus. The signal is pulsed to power up the bus. Long assertions of this active low signal will reset all devices on the bus.
V_{DD}, V_{DDA}		+3-volt power supply. V_{DDA} is a separate supply for clock receivers.
Gnd, GndA		Circuit ground. GndA is a separate ground for clock receivers.
SIn, SOut	I/O	Reset daisy chain. CMOS levels and active high.

Block Diagram



Assembly Drawing



Protocol

The Rambus interface uses a simple, synchronous, block-oriented protocol. This is a transaction-based protocol with the data transport time determined by the master. RDRAMs do not arbitrate for the bus, eliminating the need for arbitration in single-master systems.

A Rambus device must be initialized before it takes part in bus transactions. One device, the configuration master, initializes the others. The configuration master begins by assigning a unique device identification (ID) to each device. Then, the configuration master polls each device's type register and initializes all control registers as appropriate to the number and types of devices.

A full initialization continues by assigning device ID values using the SIn and SOut pins. SIn and SOut are normal CMOS signals used only during configuration and power down. SOut of the configuration master connects to SIn of the first device and so on through each bus device in daisy chain fashion. SOut of the last device connects to SIn of the configuration master.

Transactions

Transactions are composed of three packets: request, acknowledge, and data. Each packet is a sequence of bits presented continuously on a set of wires. Determining the point in time at which each packet begins is referred to as framing. The framing of the acknowledge and data packets of a transaction is referenced to the end of the request packet. To initiate a bus transfer, a master sends out a request packet that contains an address and control information.

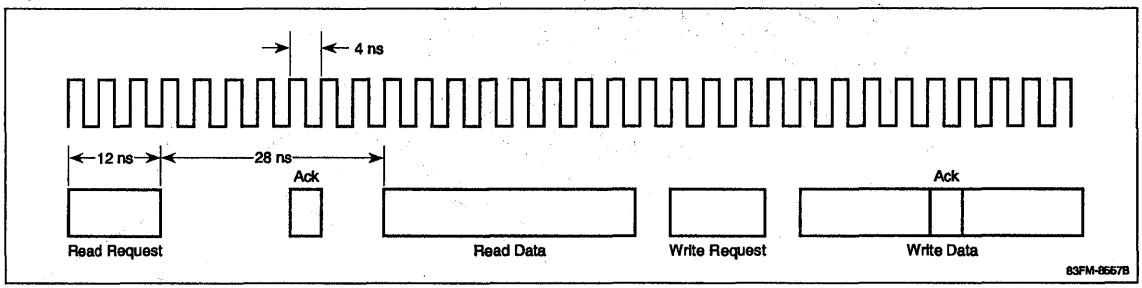
All RDRAM devices constantly monitor the bus looking for requests. When a request is received, they extract the requested device identification, determine whether it matches their own device identification, and, if so, drive an acknowledge packet back to the master.

The RDRAM also drives the data back to the master in the case of a read request or accepts the data from the master in the case of a write request. Also specified in the request packet is the number of bytes to transfer (4-256 bytes), making this a block-oriented protocol. The length of response time from a request to either an acknowledgment or an operation is always known and is based upon the clock frequency. Figure 1 is an example of a 16-byte read followed by a 16-byte write.

Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Receive clock frequency	RClk	100	250	MHz
Transmit clock frequency	TClk	100	250	MHz

Figure 1. Data Transactions



Recommended DC Operating Conditions

Parameter	Symbol	Min	Max	Unit
Junction operating temperature	T_j	0	100	°C
Supply voltage	V_{DD}, V_{DDA}	4.5	5.5	V
TTL input voltage, low	V_{IL}, TTL	−1.0	0.8	V
TTL input voltage, high	V_{IH}, TTL	2.0	V_{DD} + 1.0	V
TTL output voltage	V_{OL}, TTL	0.0	0.4	V
TTL output voltage, high	V_{OH}, TTL	2.4	V_{DD}	V
Termination voltage	V_{TERM}	2.2	2.7	V
Reference voltage	V_{REF}	1.7	2.4	V
Input voltage, high	V_{IH}	V_{REF} + 0.2		V
Input voltage, low	V_{IL}		V_{REF} − 0.2	V
Output voltage, high	V_{OH}	V_{REF} + 0.3		V
Output voltage, low	V_{OL}		V_{REF} − 0.3	V
Output current, (programmable)	I_{OL}	−35	−10	mA
Output current, high	I_{OH}	−10	10	μA
V_{REF} current	I_{REF}	−10	10	μA

Figure 2. Read Hit Timing Diagram

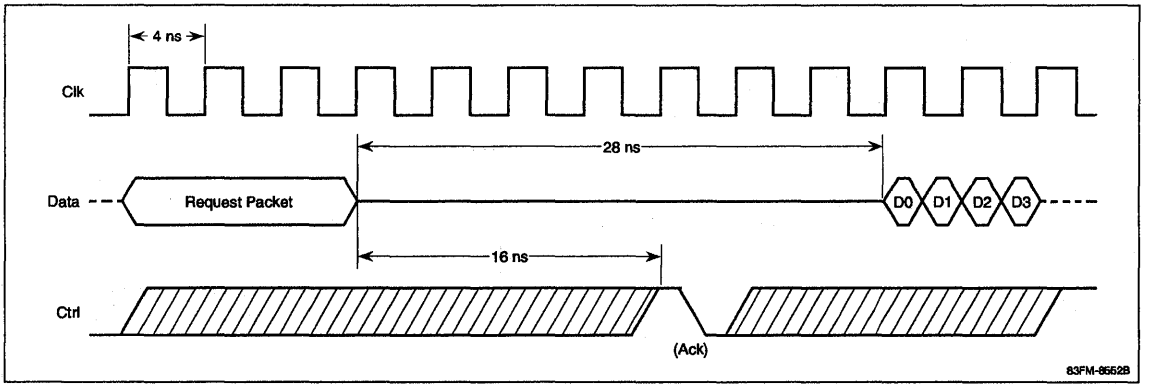


Figure 3. Write Hit Timing Diagram

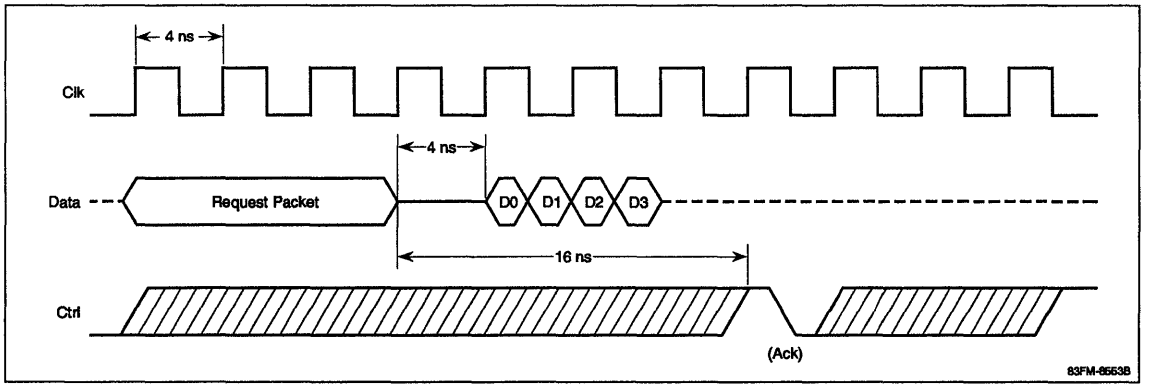


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Figure 4. Read Miss Timing Diagram

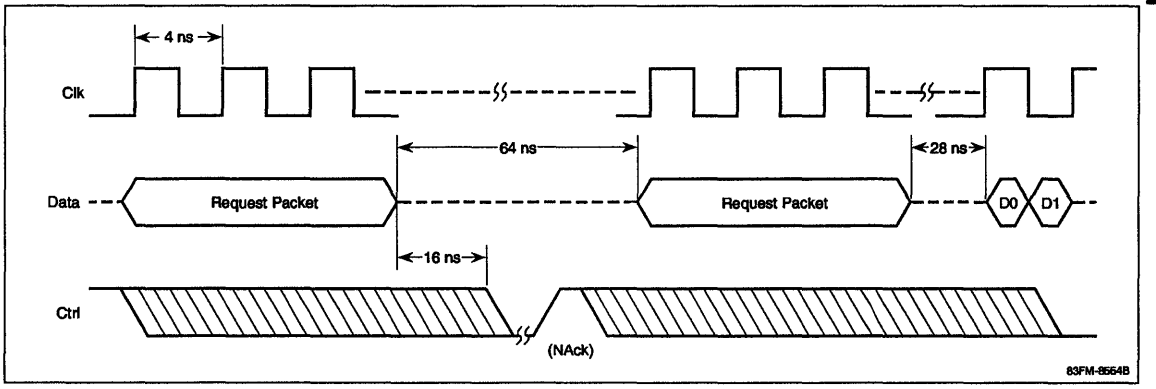
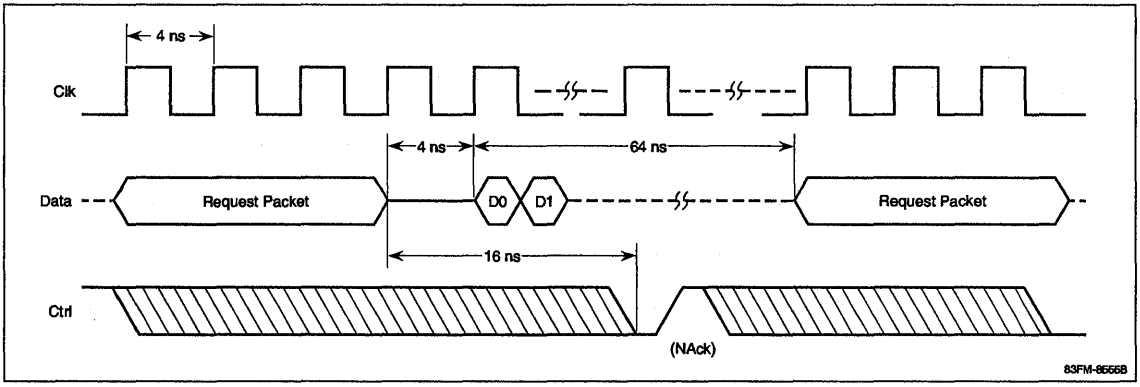


Figure 5. Write Miss Timing Diagram



NEC

Section 15
Application Notes

Description

NEC's μPD421000, μPD421001, and μPD421002 are 1-megabit dynamic RAMs (DRAMs) manufactured with the CMOS 1-μm fine-pattern process and configured as 1,048,576 x 1 bit. As shown in table 1, this family of DRAMs has been developed in a variety of speeds and packages. The package pin layouts appear in figure 1.

Configurations

The μPD421000, μPD421001, and μPD421002 (figures 2, 3, and 4) consist of memory cell arrays, input and output buffers, clock generators, refresh address counters, and row and column decoders.

The basic layout of the chips is shown in figure 5. As can be seen from the diagram, the whole memory cell array is divided into 16 smaller 64-kilobit arrays that are accessed separately.

Memory Cell Structure

Dynamic RAMs generally feature one-transistor memory cells, which require only about one-fourth of the area used by four-transistor and six-transistor (flip-flop) memory cells in static RAMs. Although a one-transistor cell provides a big advantage in reducing chip size, data must be rewritten (refreshed) at regular intervals for proper data storage on the memory cell capacitor. A cross-sectional view of the trench-type, one-transistor memory cell used in the μPD421000-series DRAMs is shown in figure 6.

This trench design uses three-dimensional rather than planar capacitors, thereby achieving a larger capacitance in a smaller surface area than in conventional circuits. The capacitance of this type of cell is determined by total trench area, the dielectric constant, and the thickness of the insulating film. To reduce soft errors caused by α-particles, an effective capacitance in excess of 50 femtofarads (fF) is used in the μPD421000, μPD421001, and μPD421002.

Figure 1. Pin Layouts

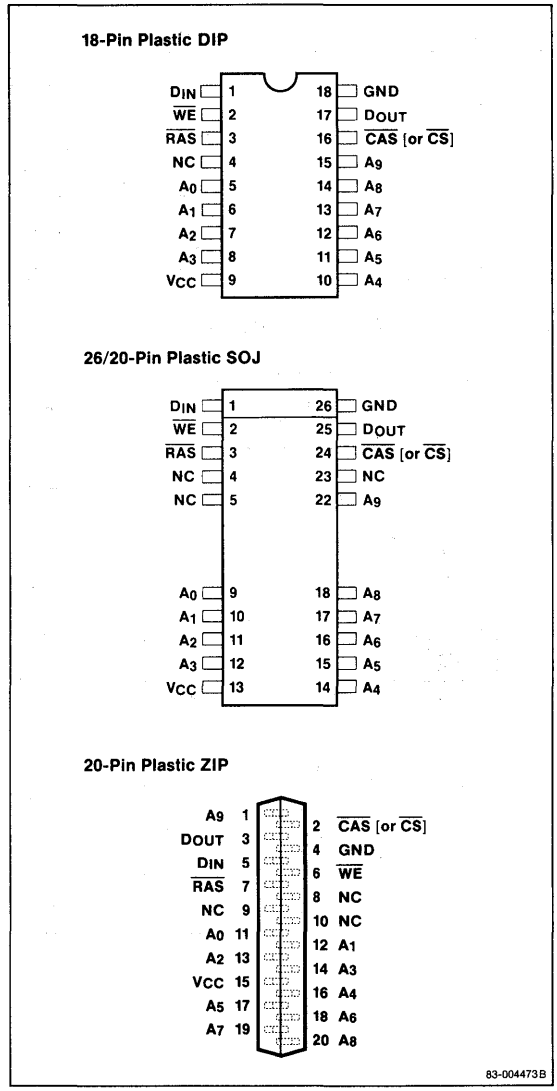


Table 1. 1,048,576 x 1-Bit DRAM Family

Device	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (min)	Operating Current (max)	Standby Current (max)	High-Speed Mode	Packages
μPD421000-80	80 ns	160 ns	70 mA	1 mA	Fast Page	C = 18-pin plastic DIP
-10	100 ns	190 ns	60 mA	1 mA		V = 20-pin plastic ZIP
-12	120 ns	220 ns	50 mA	1 mA		LA = 26/20-pin plastic SOJ
μPD421001-80	80 ns	160 ns	70 mA	1 mA	Nibble	
-10	100 ns	190 ns	60 mA	1 mA		
-12	120 ns	220 ns	50 mA	1 mA		
μPD421002-80	80 ns	160 ns	70 mA	1 mA	Static Column	
-10	100 ns	190 ns	60 mA	1 mA		
-12	120 ns	220 ns	50 mA	1 mA		

Figure 2. μPD421000 Block Diagram

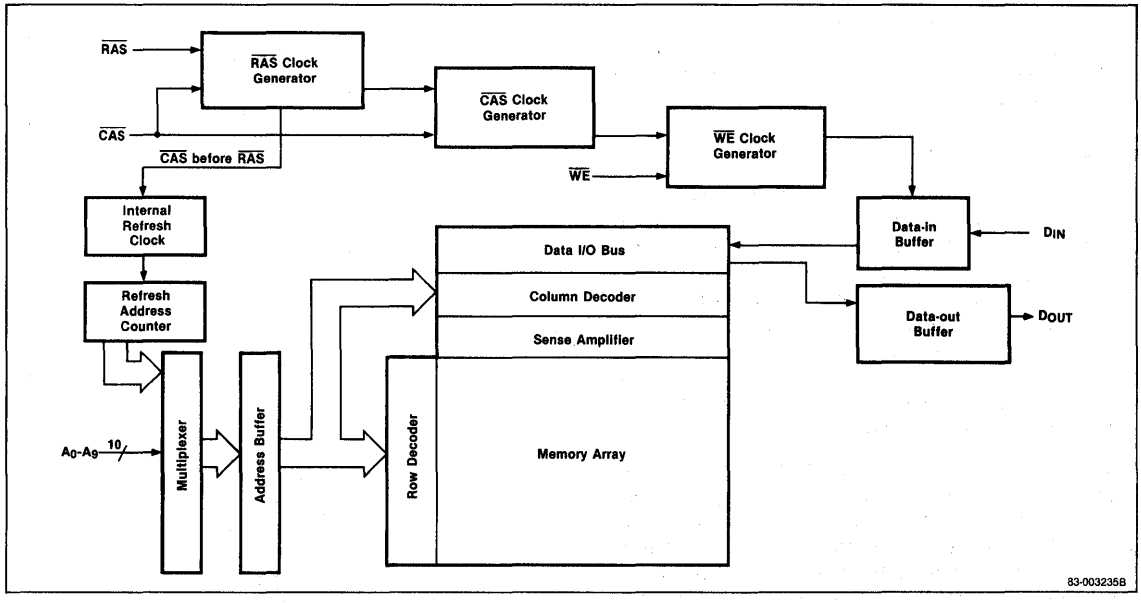


Figure 3. μPD421001 Block Diagram

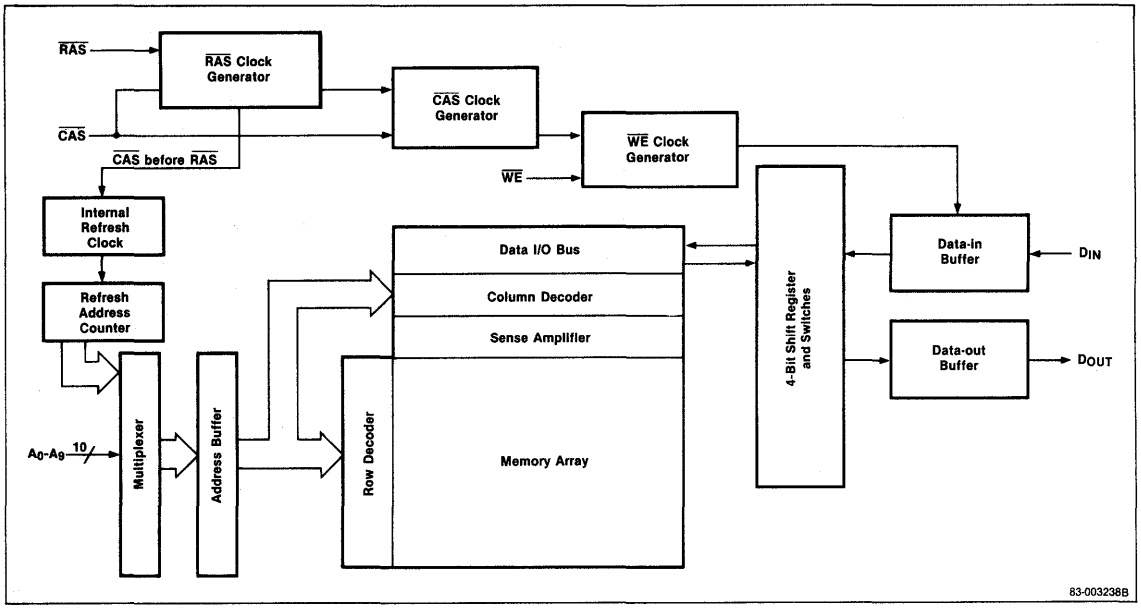


Figure 4. μPD421002 Block Diagram

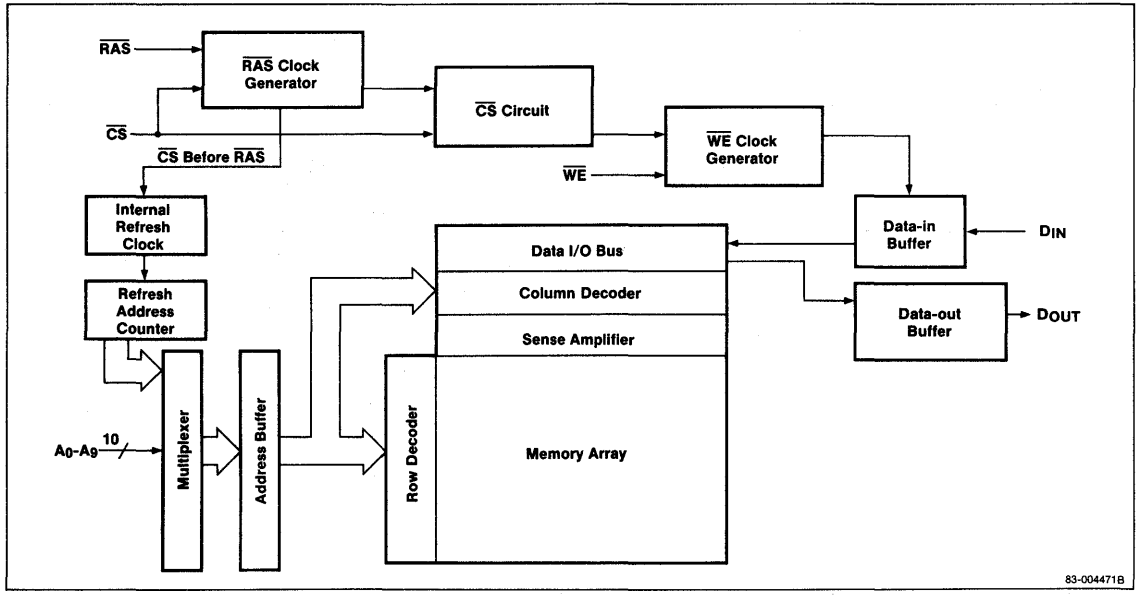


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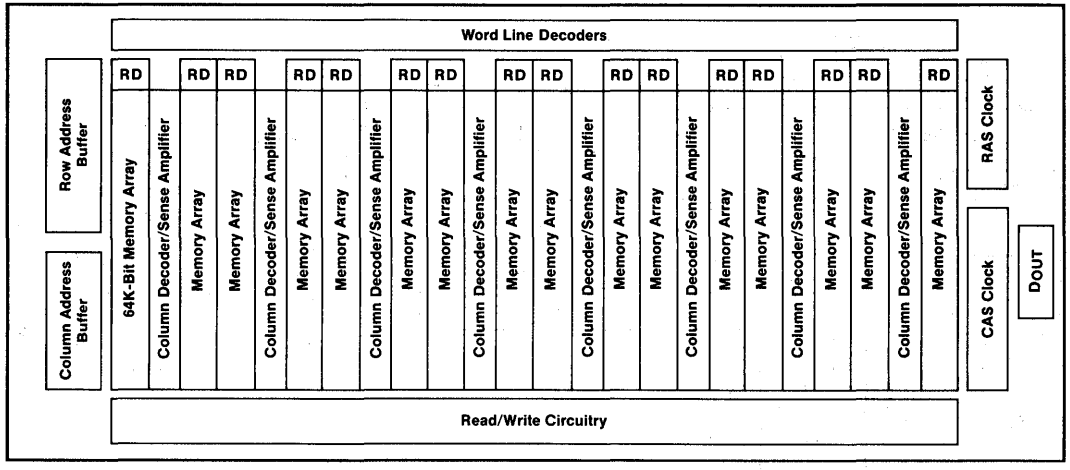
Figure 5. Chip Layout of μPD421000-Series DRAMs



Notes:
[1] The memory is divided into sixteen 64-kbit memory cell arrays.
[2] RD = row decoder/word driver.

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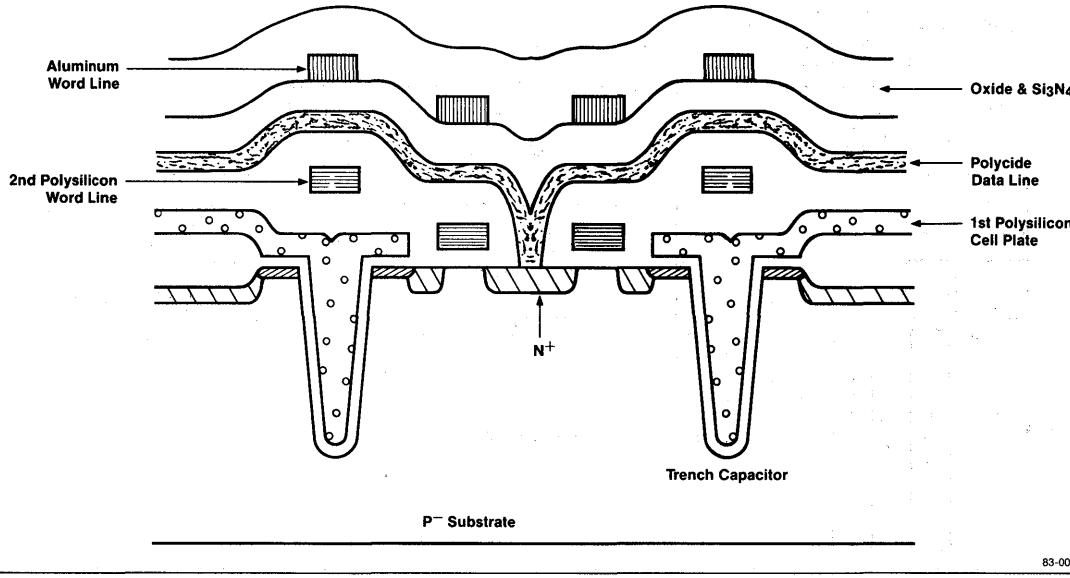
Figure 6. Cross Section of 1-Transistor Memory Cell



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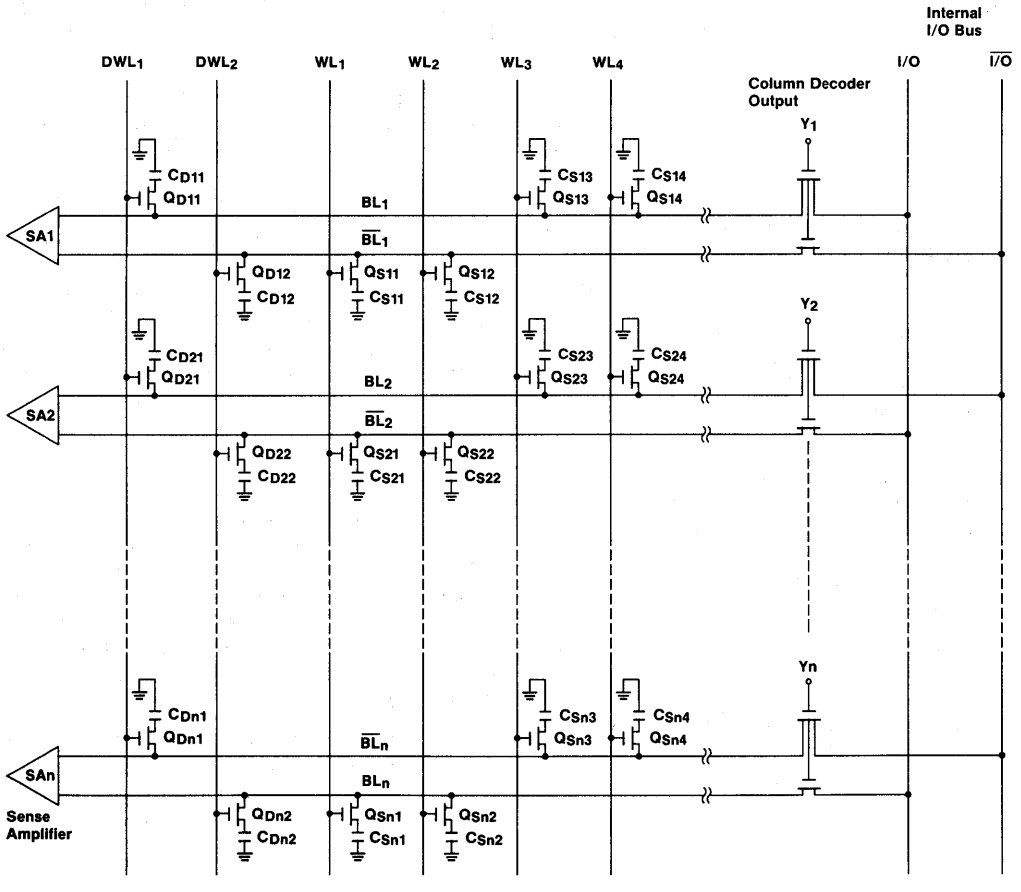
Read/Write Operation

In dynamic RAMs, changes in bit line potential caused by the minute charging and discharging of memory cells are amplified by a sense amplifier to be read as either 1 or 0. Memory cell and sense amplifier equivalent circuits are shown in figure 7.

To read the data from storage cell C_{S11}, the row address selects word line WL_1, and data from memory cells C_{S11}, C_{S21}, . . . , C_{Sn1} connected to WL_1 is passed to bit lines BL_1, BL_2, . . . , BL_n. These data signals are passed to the sense amplifiers, where they first are compared with data from dummy cells C_{D11}, C_{D21}, . . . , C_{Dn1}, connected simultaneously with the memory cells, and then amplified. At the same time, the original data is rewritten to memory cells C_{S11}, C_{S21}, . . ., C_{Sn1}. Switch Y_1 is then selected by the column address, and the C_{S11} data on the BL_1 line is passed via the I/O bus and a data amplifier to external circuits.

Write and read operations are identical, up to amplification and rewriting of memory cell data selected by a row address. After being passed to the bit line selected by the column address, write data is written into a target memory cell (such as C_{S11}). Since the number of memory cells selected by one row address in the devices is 2048, 2048 memory cells are refreshed simultaneously in each memory or refresh cycle.

Figure 7. Memory Cell and Sense Amplifier Equivalent Circuits



WL, [DWL]	Word Line [Dummy Word Line]
BL, $\overline{BL}$	Bit Line
C_S, [C_D]	Storage Cell Capacitor [Dummy Cell Capacitor]
SA	Sense Amplifier

83-004411B

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Pin Functions

$\overline{RAS}$ and $\overline{CAS}$ [or $\overline{CS}$]. The μPD421000-series DRAMs include two chip activator inputs: $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$), row address strobe and column address strobe (or chip select). In addition to reading row addresses A_0 through A_9, selecting the relevant word line, and activating the sense amplifiers for read and write operation, the $\overline{RAS}$ input also refreshes the 2048 bits selected by row addresses A_0 through A_8. The $\overline{CAS}$ input latches in column addresses (on the μPD421000 and the μPD421001) and connects the chip's internal I/O bus to the sense amplifiers activated by the $\overline{RAS}$ clock, thereby executing data input or output operations.

A_0 through A_9. Selection of an individual cell from the 1,048,576-word x 1-bit memory cell array requires a 20-bit address input. The three devices all feature an address multiplexing method in which an address is divided into two parts, the lower 10 bits (row address) and the upper 10 bits (column address).

The row address is latched into memory at the falling edge of the $\overline{RAS}$ clock. After an internal timing delay, the column address input circuits become active. Flow-through latches (voltage-level activated, not edge-triggered) for column addresses are enabled on the μPD421000 or μPD421001, and the column addresses immediately begin propagating through the latches to the column decoders. A column address is held in the latches by the falling edge of $\overline{CAS}$. For read cycles on the μPD421002, the column address input circuitry is not controlled by $\overline{CS}$, and column addresses must be held valid until data is read out.

Setup times (t_{ASR} and t_{ASC}) and hold times (t_{RAH} and t_{CAH}) for address inputs are defined in relationship to the falling edges of $\overline{RAS}$ and $\overline{CAS}$ ($\overline{CS}$ or $\overline{WE}$ for write cycles on the μPD421002). In actual operation, a row address is specified before the $\overline{RAS}$ input is activated; once the address bus switches to column addresses, $\overline{CAS}$ (or $\overline{CS}$) is activated.

$\overline{WE}$ [Write Enable]. Read and write cycles are executed by activating the $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) inputs and controlling $\overline{WE}$. An early write cycle is executed if $\overline{WE}$ is activated before the falling edge of $\overline{CAS}$ (or $\overline{CS}$) during a write cycle, and a late write (read-modify-write) cycle is executed if the $\overline{WE}$ input is activated later.

Read and Write Cycles

Read cycles are executed by activating $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) with the $\overline{WE}$ input at a high level (inactive). The $\overline{RAS}$ access time of t_{RAC} is valid if the delay from $\overline{RAS}$ to $\overline{CAS}$ (or $\overline{CS}$) is less than t_{RCD} (max), and the delay from $\overline{RAS}$ to the column address is less than t_{RAD} (max). The $\overline{CAS}$ (or $\overline{CS}$) access time of t_{CAC} is valid if the delay from $\overline{RAS}$ to $\overline{CAS}$ (or $\overline{CS}$) is greater than t_{RCD} (max), and the delay from the column address to $\overline{CAS}$ (or $\overline{CS}$) is greater than t_{ASC} (max). The address access time of t_{AA} is valid if the delay from $\overline{RAS}$ to the column address is greater than t_{RAD} (max), and the delay from the column address to $\overline{CAS}$ (or $\overline{CS}$) is less than t_{ASC} (max). Output data is held valid until $\overline{CAS}$ (or $\overline{CS}$) becomes inactive again (figure 8).

Write cycles are executed by activating the $\overline{RAS}$, $\overline{CAS}$ (or $\overline{CS}$), and $\overline{WE}$ inputs. Write data is latched by the falling edge of $\overline{CAS}$ (or $\overline{CS}$) or $\overline{WE}$, whichever occurs later.

A $\overline{WE}$ input applied before the $\overline{CAS}$ (or $\overline{CS}$) input initiates an early write cycle, whereby write data is latched by the falling edge of $\overline{CAS}$ (or $\overline{CS}$).

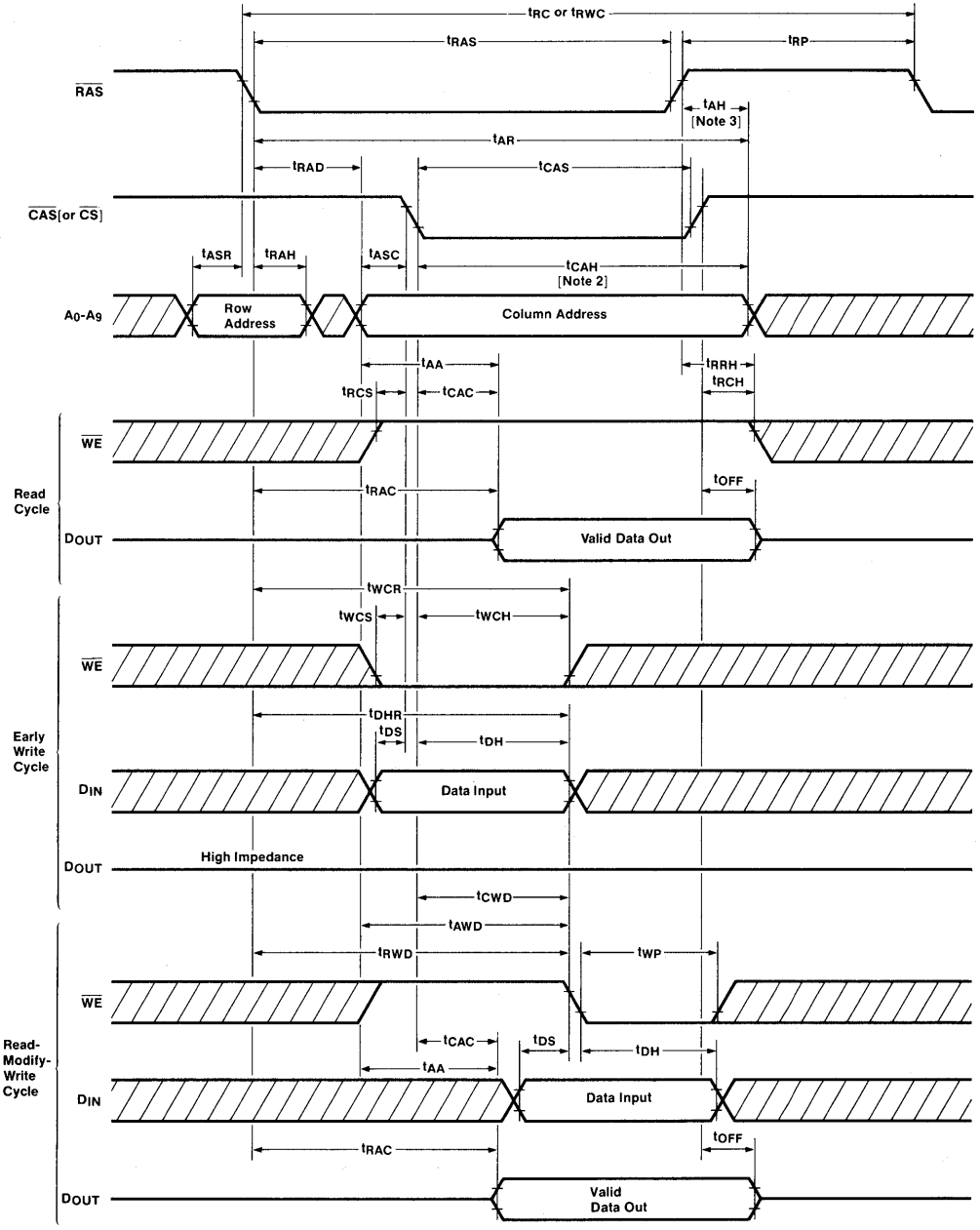
Conversely, a $\overline{WE}$ input applied after the $\overline{CAS}$ (or $\overline{CS}$) input initiates a late write cycle (read-modify-write cycle), whereby write data is latched into the chip by the falling edge of $\overline{WE}$. The status of D_{OUT} is not guaranteed in this case, but depends on the timing of $\overline{WE}$ with respect to $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$). If $\overline{WE}$ is activated at least t_{CWD} after the $\overline{CAS}$ (or $\overline{CS}$) input, and at least t_{RWD} after the $\overline{RAS}$ input, write operation is enabled in the same memory cycle during which the read data is valid.

Refresh Cycles

The process of rewriting data held in a memory cell, refreshing, is performed by a sense amplifier in the μPD421000-series DRAMs. The three devices are capable of executing the same $\overline{RAS}$-only and $\overline{CAS}$ (or $\overline{CS}$)-before-$\overline{RAS}$ refresh cycles as are executed in other conventional, general-purpose DRAMs. All 512 rows of memory cells must be refreshed within any 8-ms period.

Since in image memory applications, row addresses A_0 through A_8 are read or written sequentially within 8 ms, the accessing itself initiates refreshing and no additional refresh cycles are required.

Figure 8. Access Timing



Notes:

[1] In a read-modify-write cycle, cycle time is defined as $t_{RWC} = t_{RWD} + t_{RWL} + 3\,t_T + t_{RP}$.

[2] Timing t_{CAH} applies to the μPD421000 and the μPD421001.

[3] Timing t_{AH} applies to the μPD421002.

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$\overline{RAS}$-Only Refresh Cycle. $\overline{RAS}$-only refreshing is executed simply by leaving the $\overline{CAS}$ (or $\overline{CS}$) input inactive (high level) during a $\overline{RAS}$ clock cycle. This cycle uses the 512 lower addresses specified by row addresses A_0 through A_8 to ensure that all memory cell bits are refreshed. Hence, 2048 bits of memory are refreshed in a single cycle (figure 9).

$\overline{CAS}$ [or $\overline{CS}$]-Before-$\overline{RAS}$ Refresh Cycle. This type of refreshing is executed using the addresses generated by the chip's internal address counter when $\overline{CAS}$ (or $\overline{CS}$) is activated (low level) in advance of the $\overline{RAS}$ input (figure 10).

Even in systems without an address output from the microprocessor, no additional external address counter or refresh address selector is required. $\overline{CAS}$ (or $\overline{CS}$)-before-$\overline{RAS}$ refreshing allows refreshing to be accomplished with a minimum of peripheral circuits (figure 11).

High-Speed Access Cycles

In addition to being capable of standard access, the μPD421000 is equipped with fast-page access, the μPD421001 with nibble access, and the μPD421002 with static-column access (table 2).

Figure 9. $\overline{RAS}$-Only Refresh Cycle

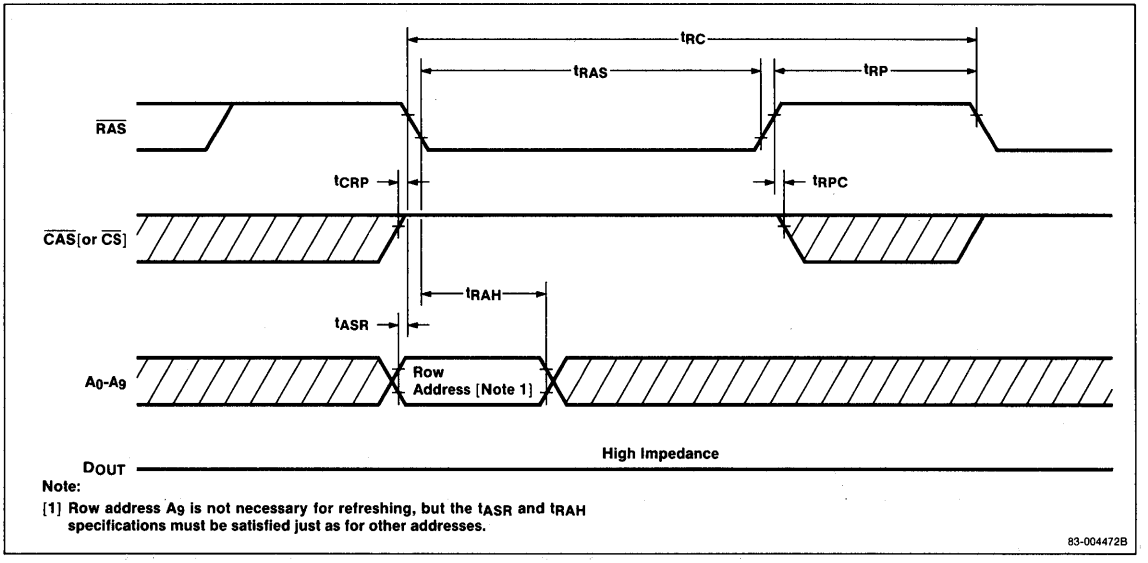

Figure 10. $\overline{CAS}$ (or $\overline{CS}$)-Before-$\overline{RAS}$ Refresh Cycle

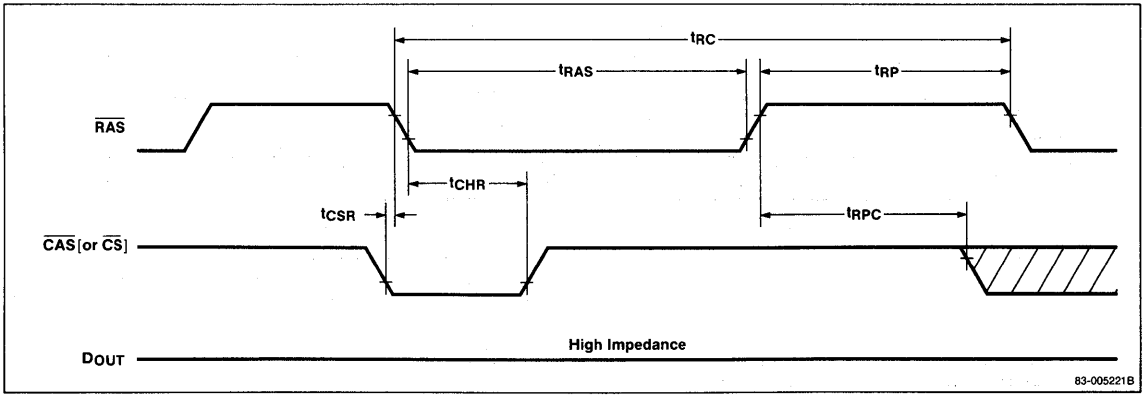

Figure 11. Address Multiplexing

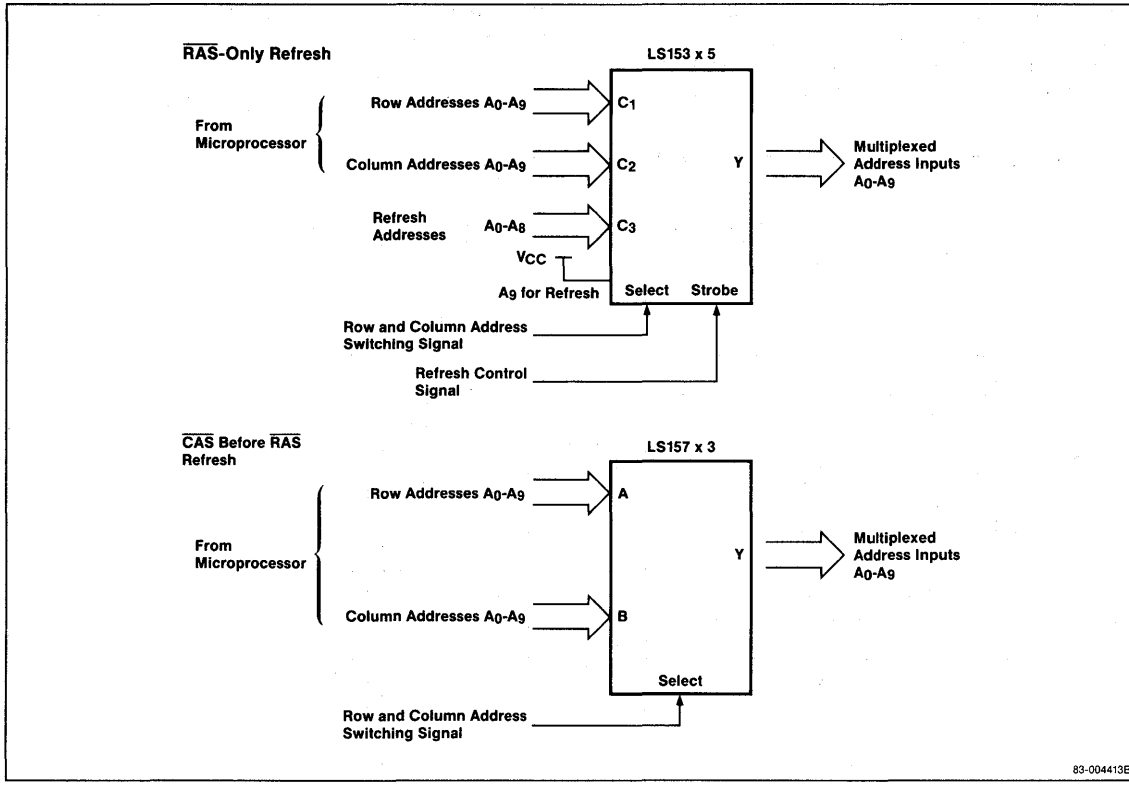

Table 2. Major Characteristics of Fast-Page, Nibble, and Static-Column Modes

Device	Access Time (max)	Cycle Time (min)	Internal Address Usage	High-Speed Access
μPD421000-80	45 ns	50 ns	Row: Page selection Column: Individual cell access on one page	Random access on one page selected by A_0 through A_9
-10	50 ns	60 ns		
-12	60 ns	70 ns		
μPD421001-80	20 ns	40 ns	Row, Column: A_9 inputs set starting location for nibble-mode access	Serial access (4 bits maximum)
-10	25 ns	45 ns		
-12	30 ns	55 ns		
μPD421002-80	45 ns	50 ns	Row: Row selection Column: Individual cell access on one row	Random access on one row selected by A_0 through A_9
-10	50 ns	60 ns		
-12	60 ns	70 ns		

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Fast-Page Mode. Fast-page mode makes it possible to randomly access data in the same row address (figures 12 and 13). The 1024 bits of memory are obtained from the combinations of column address inputs A_0 through A_9 within one row address in the μPD421000. Up to 1998 continuous accesses can be executed on the 80-ns version before the maximum interval for t_{RASP} (100 μs) is reached.

The t_{PC} cycle time for random fast-page read or write cycles is equivalent to $t_{CAS} + t_{CP} + 2t_T$.

Figure 12. Memory Cell/Sense Amplifier Block of the μPD421000

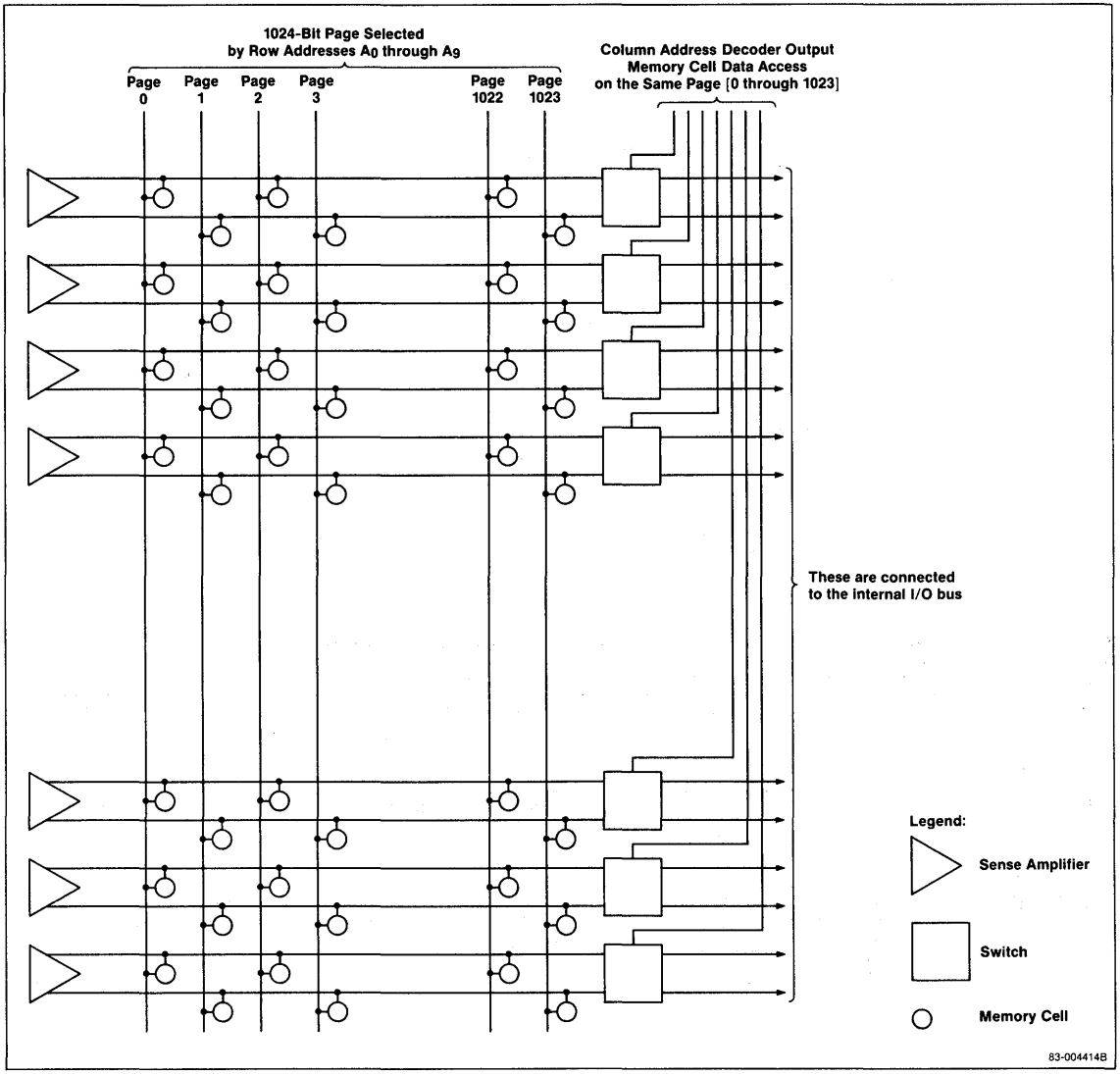
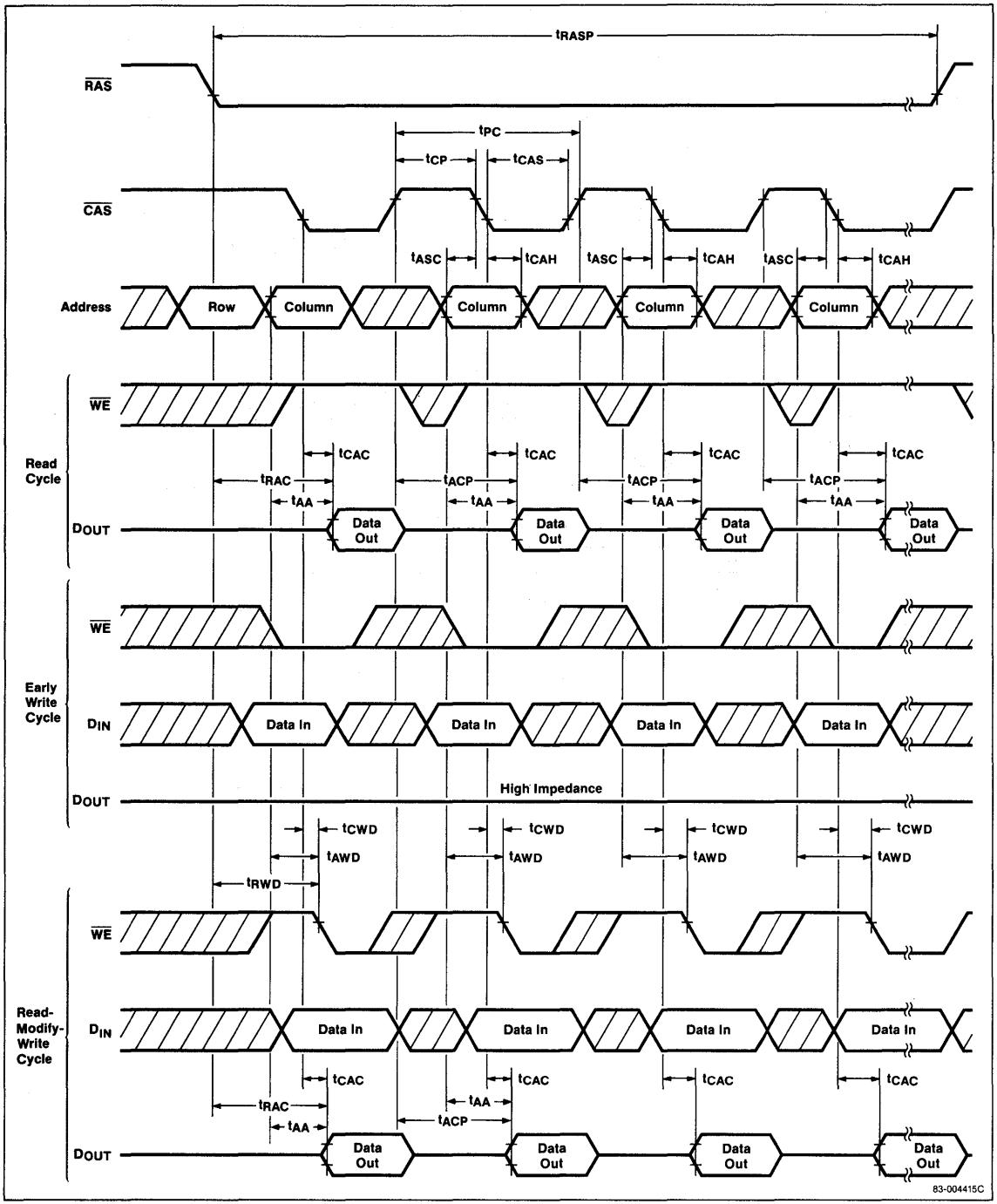
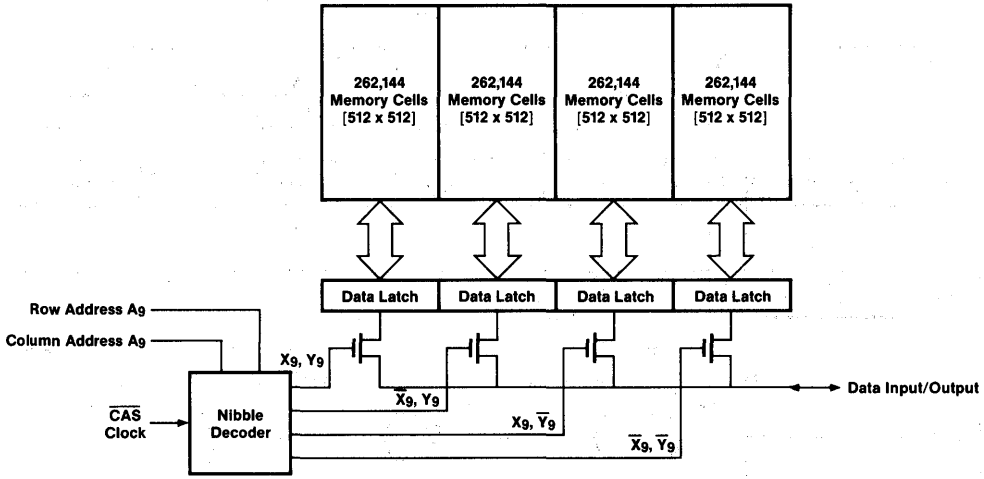


Figure 13. Fast-Page Timing



Nibble Mode. In nibble-mode cycles, the first data location is specified by row and column addresses A_0 through A_9 during a read or write cycle (table 2 and figures 14 and 15). When the μPD421001 internally sequences the two highest-order addresses (A_9) during the next $\overline{CAS}$ clock cycle, read and write cycles can be executed in less time than in fast-page operation.

Figure 14. Nibble-Mode Block Diagram and Example of Access Sequence



Sequence	Nibble Bit	Row Address A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Comment
$\overline{RAS}/\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	External address
$\overline{CAS}$ Cycling	2	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
$\overline{CAS}$ Cycling	3	0	1	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	Internal address
$\overline{CAS}$ Cycling	4	1	1	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	
$\overline{CAS}$ Cycling	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	Repeated sequence

Notes:

[1] X_9 = Row address A_9

[2] Y_9 = Column address A_9

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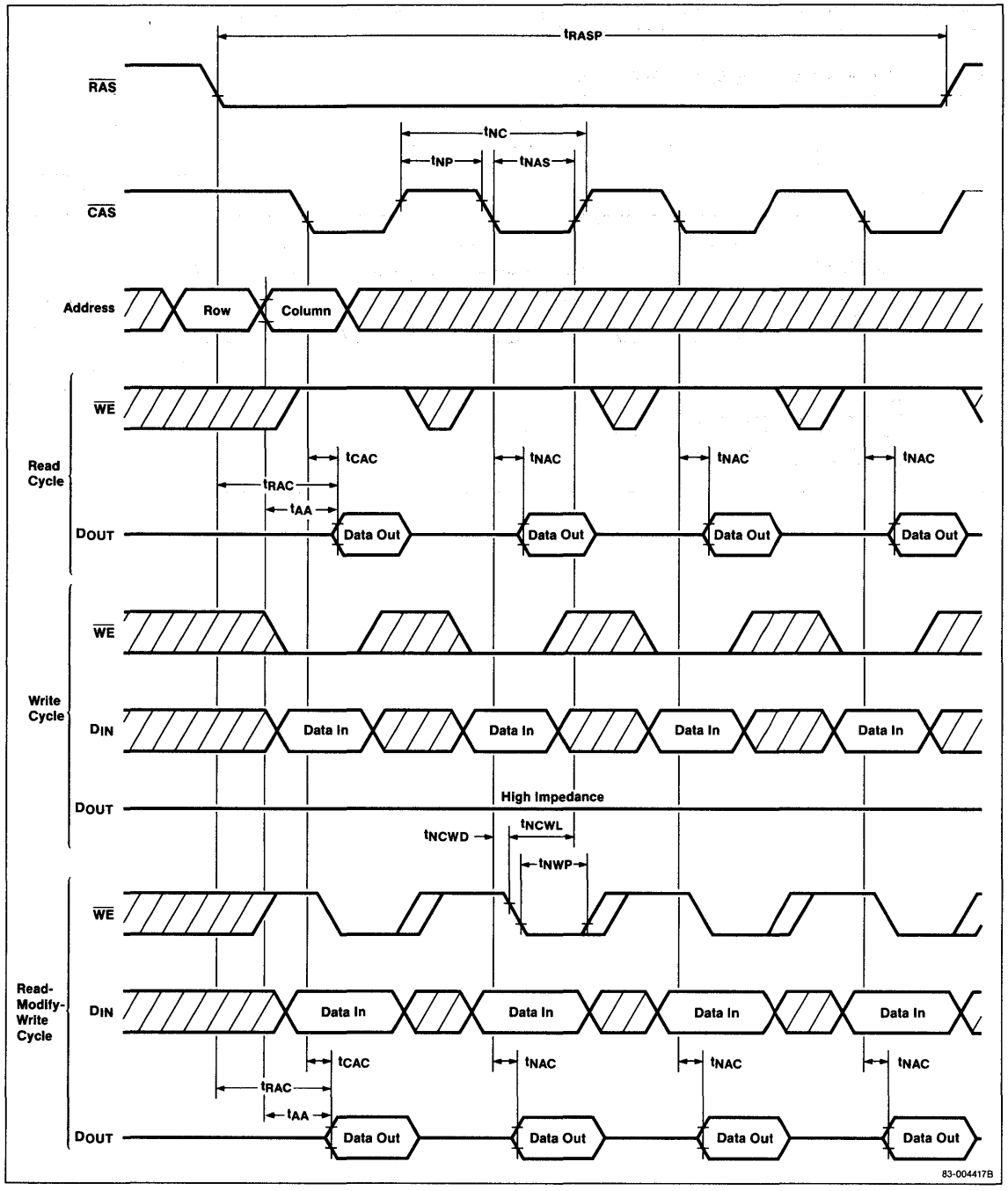
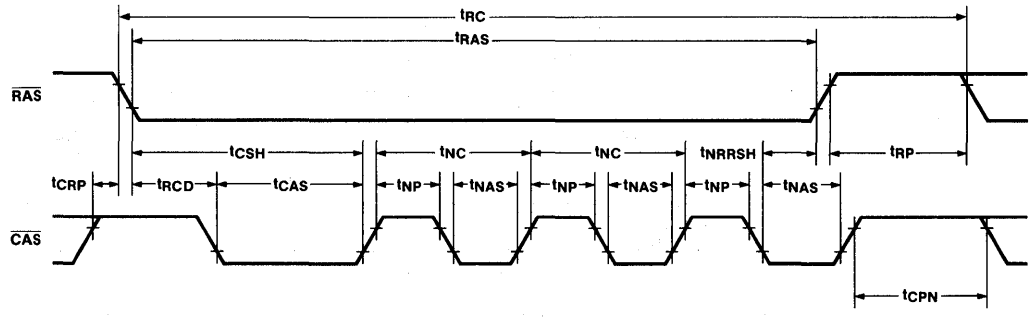
Figure 15. Nibble-Mode Timing



For the 80-ns version, the average cycle time per bit in nibble mode is 70 ns, when 4 bits are accessed during a long t_{RAS} cycle (figure 16). By using multiple μPD421001 devices, high-speed cache and frame buffer applications are possible (figure 17).

Figure 16. Average Data Rate in Nibble Access



Notes:

[1] Minimum t_{RC} [ns] in nibble mode:
$= t_{CSH} + t_{NC} \times 2 + t_{NP} + t_{NRRSH}$ or $t_{NWRSH} + t_{RP} + t_T \times 4$
$= 80 + 40 \times 2 + 10 + 20 + 70 + 20$
$= 280$ ns [for 4 bits]

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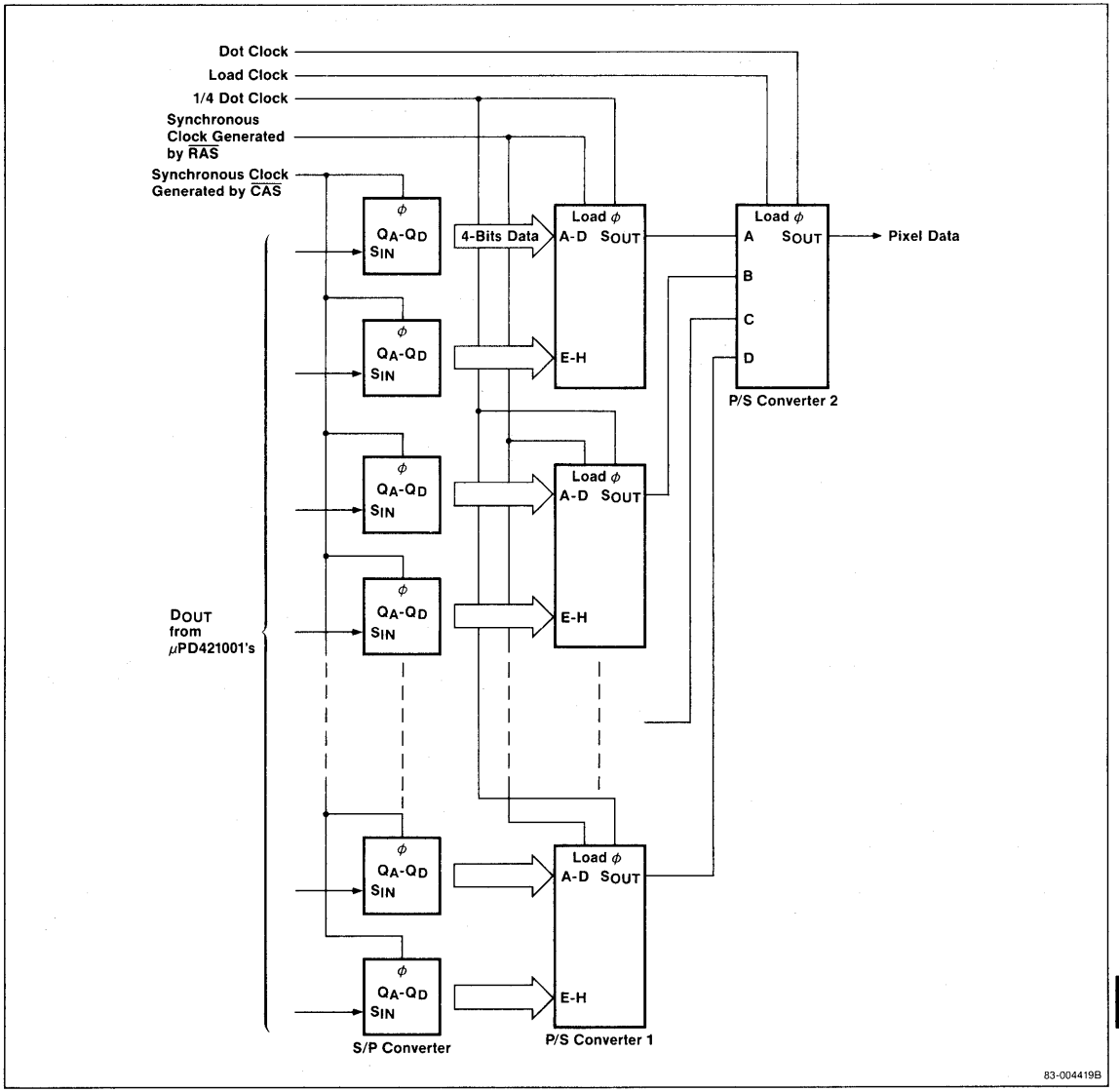
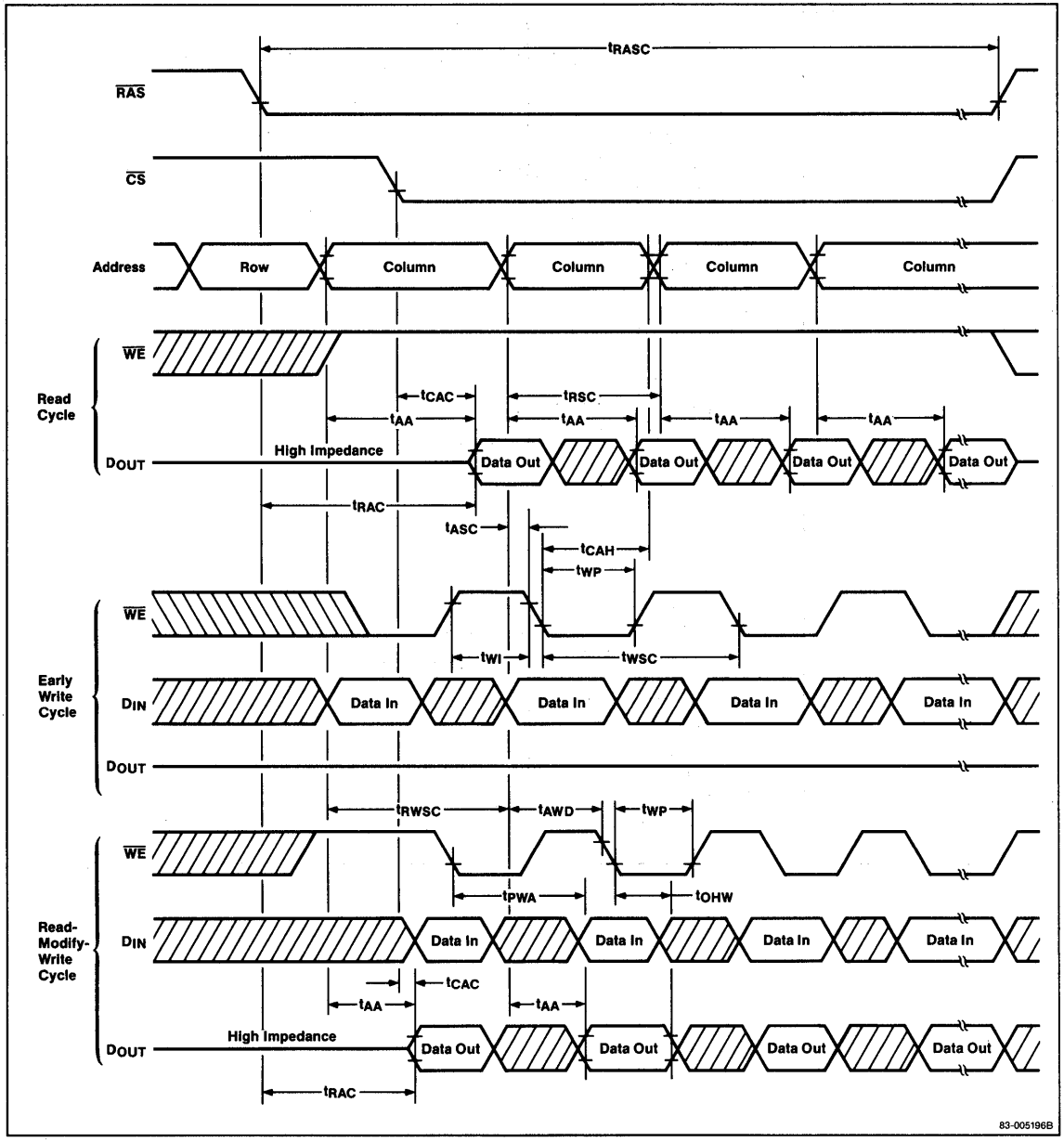
Figure 17. High-Speed Data Access Using Nibble Mode



Static-Column Mode. Row and column addresses are functionally equivalent in static-column and fast-page access. The available number of continuous accesses on one row, and the cycle timing, are also similar to fast-page operation.

In a static-column device, there are no setup or hold timing requirements for read addresses; $\overline{CS}$ may be held low continuously in the ON-state. To allow this feature, the column addresses must be maintained as valid inputs for the duration of each cycle. There are few other restrictions on timing (figure 18).

Figure 18. Static-Column Timing



Precautions

Precautions when using the μPD421000, μPD421001, μPD421002, and other DRAMs should be carefully observed in the areas listed below:

- Power-on and initialization
- Supply voltage fluctuations caused by peak currents
- Relationships between address/data inputs and drivers
- $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) generation

Power-On and Initialization. Dynamic RAMs operate by the charging and discharging of gate and internal circuit capacitances. Therefore, dummy $\overline{RAS}$ clock cycles must be executed to charge internal potentials to the prescribed levels when power is applied. Dummy $\overline{RAS}$ cycles are also necessary when there has been no accessing (reading, writing, or refreshing) for periods longer than the refresh interval (figure 19).

To control transistor threshold voltages and decrease internal stray capacitance, DRAMs are usually equipped with a substrate voltage generator circuit to supply the chip's interior with negative voltage. Approximately 100 μs is required to generate an adequate negative voltage level after power is applied and $V_{CC} \geq 4.5$ V.

When the power is switched on, a peak current dependent on the levels of $\overline{RAS}$, $\overline{CAS}$ (or $\overline{CS}$), and $\overline{WE}$ is reached during the rising of V_{CC}. This peak current—maximum when $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) are active and $\overline{WE}$ is inactive—can be minimized by using clock input pullups on $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) so that their rise times correspond to the rise time of the power supply.

Supply Voltage Fluctuations. Since 1 and 0 logic (storage) operations are executed by the charging and discharging of capacitances, including the memory cells, the peak current generated is dependent on charge and discharge timing.

This peak current is concentrated just after $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) transition intervals (figure 20) with a peak value of about 120 mA. Since this current is a source of noise (voltage drop) in the memory system supply voltage, decoupling by multilayer ceramic capacitors with excellent frequency response is necessary. If the average of the 120-mA peak current pulse lasts about 100 ns, the capacitance required to keep the drop in the supply voltage line at about 0.1 V will be calculated as follows:

$$C = \frac{120\ (mA) \times 100\ (ns)}{0.1\ (V)}$$

$$= 120 \times 10^3\ pF$$

$$= 0.12\ \mu F$$

Therefore, when designing the memory board, keep the power and ground leads as short as possible for low inductance. Decoupling capacitors of about 0.2 μF must be inserted between the power supply lines for each memory device. With careful board layout, the use of fewer but larger capacitors is possible. Capacitors used in one of every two memory device locations, with a value of perhaps 0.33 μF, can provide satisfactory decoupling in many cases.

Figure 19. Dummy Cycles after Power is Applied

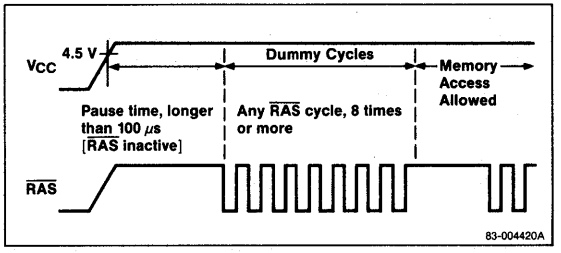
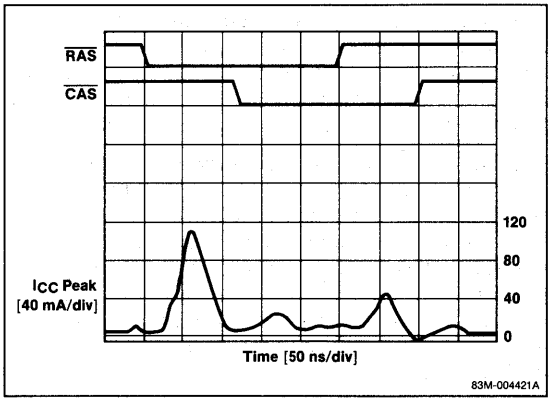


Figure 20. Operating Current Waveform



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Address/Data Inputs and Drivers. Probably the most important consideration in DRAM timing is the relationship between address/data inputs and the external drivers. In address-multiplexed DRAMs such as the μPD421000, μPD421001, and μPD421002 (where row and column addresses are supplied as two sets of inputs), addresses supplied externally have to be switched by a multiplexer.

The sequence of this timing must be designed very carefully. A timing sequence starts with the setting of row addresses. Next, $\overline{RAS}$ falls. After the specified hold time for row addresses is met, the addresses are switched to set up column address input. Once $\overline{CAS}$ (or $\overline{CS}$) falls, the specified hold time for column addresses must be satisfied.

When $\overline{CAS}$ (or $\overline{CS}$) is activated within the time specified for t_{RCD} (max), the setup time for column addresses is more difficult to guarantee than when t_{RCD} is longer than t_{RCD} (max), because one external address driver has to drive more than one address pin in an array of DRAMs. The address multiplexer's delay time is increased by load capacitances larger than the typical value.

For illustration, measurements of output delay times for certain drive load capacitances are shown in figure 21.

In the design of high-density memory boards having a large number of memory devices, partitioning of drivers becomes necessary because of wiring and through-hole capacitances. Special care must be taken to ensure that the setup and hold times for addresses conform with the specifications. Otherwise, invalid or undefined addresses may be latched into the chip, and data may be destroyed even if nothing is written.

$\overline{RAS}$ and $\overline{CAS}$ [or $\overline{CS}$] Generation. In addition to reading the address inputs, $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) also generate the basic timing for all DRAM circuit operations. The internal timing generators are connected in daisy-chain fashion, and are completely controlled by the basic $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) inputs. Because of this control, the memory system design must prevent noise glitches from being generated in the $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) inputs.

$\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) timing is specified in terms of minimum values. High- or low-level pulses that do not satisfy these minimum values can result in incorrect output data (because there is insufficient time for sense amplifier operation), and can also lead to destruction of write data. Therefore, the prevention of noise glitches must be carefully considered in logic and circuit design.

Figure 21. Effect of Load Capacitance on TTL (7404) Output

Delay and Transition Times

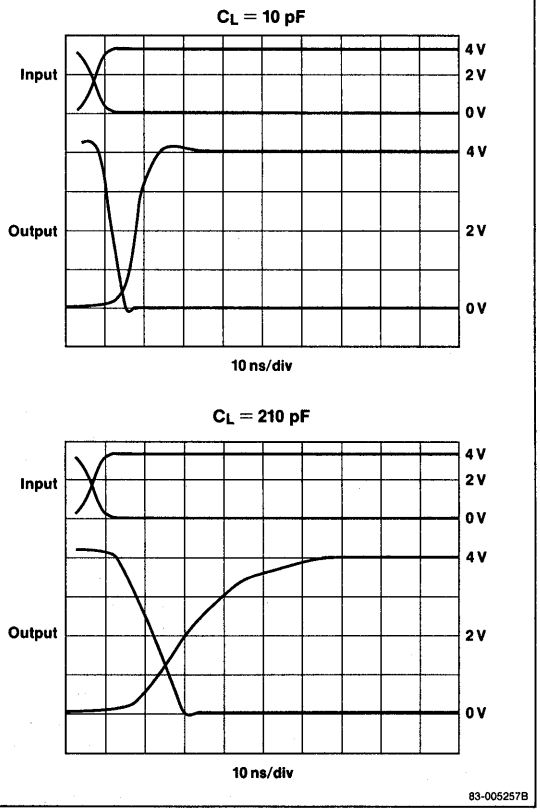
Parameter	Time [ns] C_L = 10 pF	C_L = 110 pF	C_L = 210 pF
t_{PLH}	9	16.5	26
t_{PHL}	5.5	12.5	17
t_R	3.2	7.8	15
t_F	1.5	3.8	5.5

Notes:

[1] t_{PLH}, t_{PHL} are defined as the delay time from V_{IN} = 1.5 V to V_{OUT} = 2.4 V or 0.8 V.

[2] t_R and t_F are defined as the transition time between V_{OH} [min] and V_{OL} [max].

[3] Load capacitance C_L includes the oscilloscope input capacitance.



V40™ MICROPROCESSOR APPLICATION

Features

The μPD70208 (also known as V40) is a high-performance 8-bit CMOS microprocessor featuring 16-bit architecture in the CPU, and including a number of other peripheral devices within the same chip. The CPU is equipped with a powerful set of instructions that cover bit processing and multiple-length, packed-BCD operations, high-speed multiplications and divisions, and variable-length bit and field manipulations.

This device combines high-speed processing with flexibility in a variety of applications. The on-chip peripherals include a clock generator with a timer/counter and programmable wait control, refresh control, serial control, interrupt control, and DMA control units. In addition to allowing more compact microcomputer systems, the V40 has a simplified system design.

When connected to the μPD421000-series DRAMs, the V40 does not require an external refresh timer or other peripherals, which means a big reduction in the number of external devices required.

Memory Mapping

In the V40, memories of up to 1 megaword can be accessed using address information (A_{19} through A_0) output from the 20-bit address bus (figure 22).

The first 1024 bytes, 0 through 3FFH, are allocated to interrupt vectors (although areas that cannot be used by the system can be used elsewhere). Addresses FFFF0H through FFFFBH are used for starting and resetting purposes; FFFFCH through FFFFFH are reserved for future use and cannot be used here. The remaining address space, 400H through FFFEFH, is not allocated and may be used as desired.

As shown in figure 23, with a data bus width of 8 bits in the V40, CPU connections to the memory require only that the 20-bit address output from the CPU be accepted in the 1-megabyte address space. Byte data is accessed in one bus cycle, and word data is accessed in two bus cycles.

V40 is a trademark of NEC Corporation.

Because of this simple connection requirement, it is only necessary to allocate the system control ROM to addresses of at least FFFF0H and disable the ROM-area RAM (since 1 megabyte is already taken up by eight 1-megabit DRAMs). The method used may involve either deselecting the ROM-area RAM by a decoder, or executing bank switching to use the entire area as RAM area. The example included for this application shows the former method because it is simpler.

Figure 22. V40 Memory Mapping

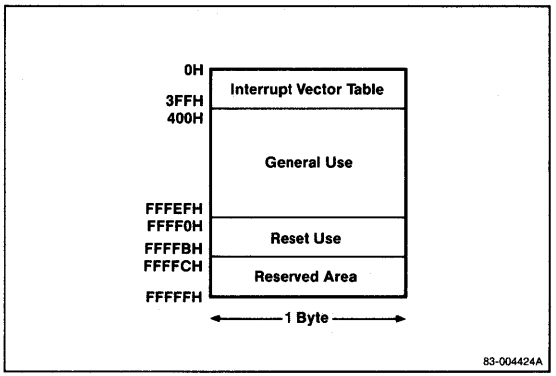
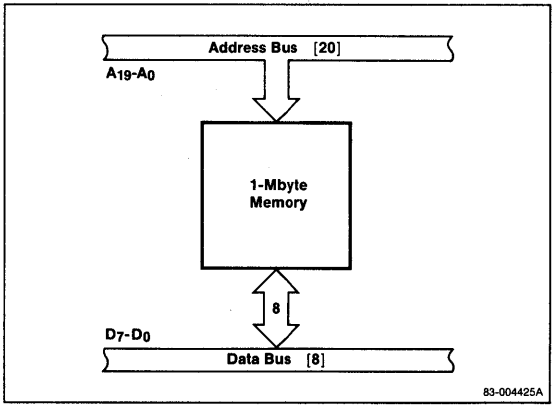


Figure 23. V40 Memory Interface



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Hardware Configuration

Since refresh addresses and the timing control outputs can be supported by programming on-chip circuits, the generation of $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) timing is the only major DRAM support not provided directly by the V40 (figure 24).

Memory Access Timing Generation

Although V40 memory access timing can be generated from either the bus status or MWR/$\overline{MRD}$, the μPD71088 system bus controller is used in this application example to enable connections to slightly slower-speed memories. The $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) signals are thus generated by decoding the bus status.

The $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) generator is shown in figure 25, and the operation timing in figure 26. To generate the control timing with this system controller, bus status signal BS_2 is sampled by the CPU clock output (ϕ_{OUT}) at the rising edge of the T_1 cycle, and $\overline{RAS}$ is generated from FF2 at the falling edge of ϕ_{OUT} at the end of T1. The multiplex control signal (MPX) used in address switching during memory cycles is generated by $\overline{RAS}$. After $\overline{RAS}$ is generated, it is delayed by the rising edge of the external 16-MHz clock to create MPX, which is then passed to the data selector input.

As can be seen from figure 26, memory access time is equal to $2/f(\phi_{OUT}) - (t_{SDK} + \text{TTL delay time})$. Even if an external clock of 16 MHz is used, a -12 device is sufficient ($\overline{RAS}$ access time in the -12 device is 120 ns).

Figure 24. Hardware Configuration for the Use of 1M DRAMs

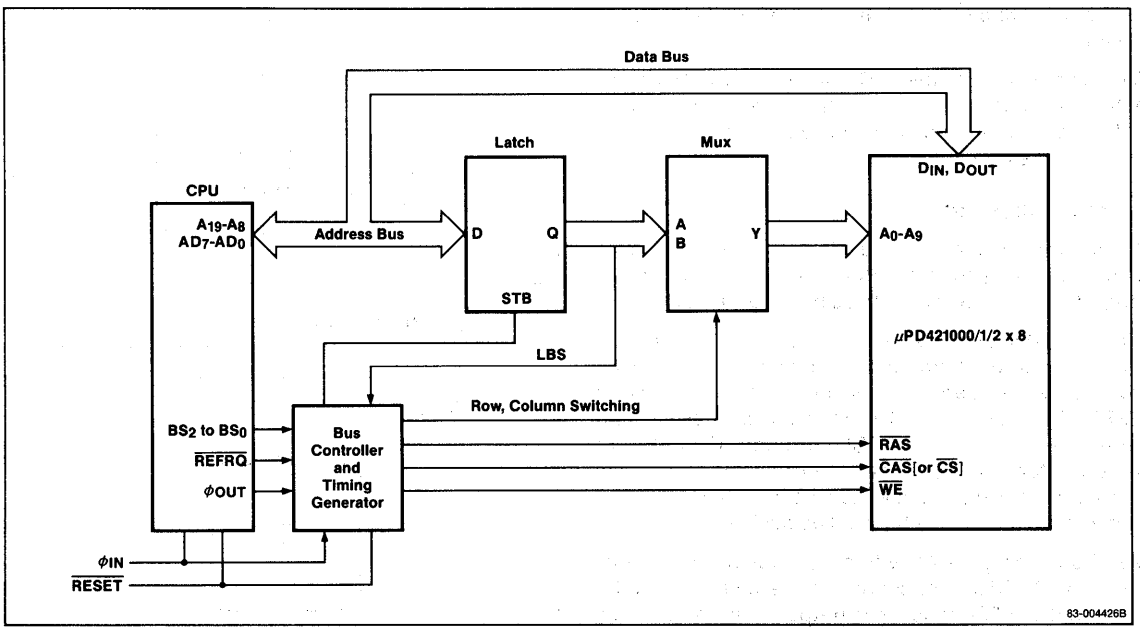


Figure 25. $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) Timing Generator

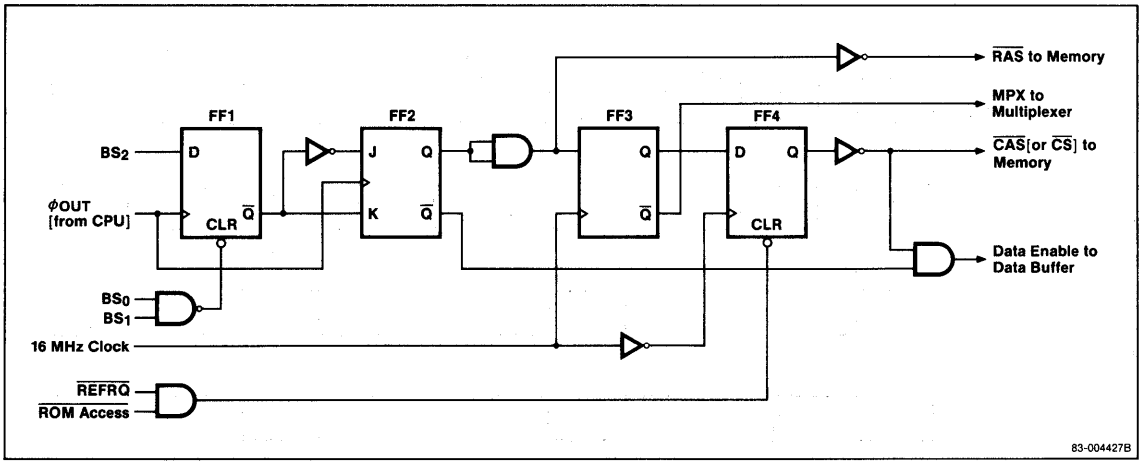
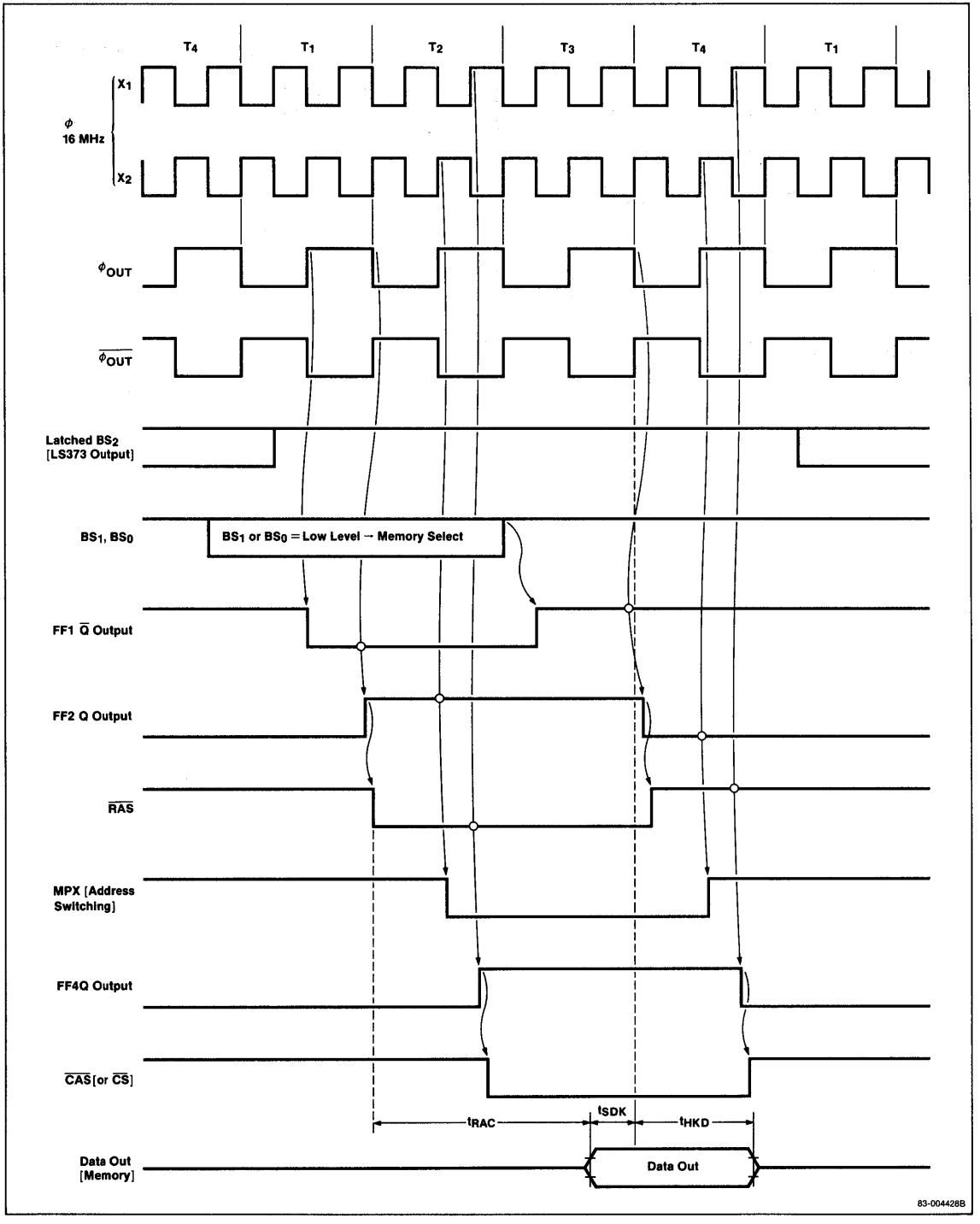


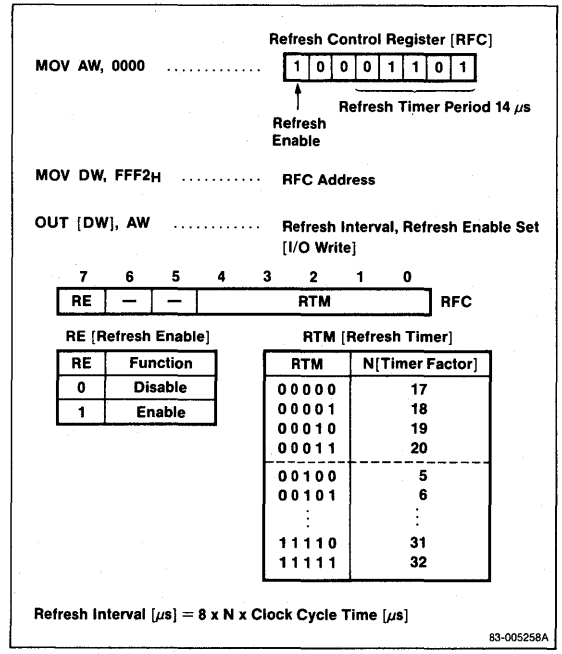
Figure 26. $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) Timing Sequence



Refresh Timing Generation

Refreshing for the μPD421000, μPD421001, and μPD421002 is executed by selecting 512 lines in 8 ms. In the V40, memory refreshing can be handled easily by outputting the $\overline{REFRQ}$ control signal and the A_0 through A_8 refresh addresses. These signals are controlled by programming the refresh control register (RFC), allocated to I/O address FFF2H (figure 27).

Figure 27. Programming of Refresh Control Register



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This function generates the $\overline{\text{REFRQ}}$ control signal in accordance with the programmed interval. In this application example, $\overline{\text{REFRQ}}$ is used to disable generation of the $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) clock during refresh cycles, thereby initiating $\overline{\text{RAS}}$-only refreshing. Figures 28 and 29 show how to generate memory addresses and how to control data input and output by using control signals generated by the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) timing generator. Figure 30 shows the timing for V40-generated refresh addresses.

The programmed values for the control register appear in figure 27 (also refer to the *μPD70208/μPD70216 User's Manual).*

Authorization for the μPD70208/μPD70216 refresh control unit to use the memory bus can be set either to top priority or lowest priority, depending on the hold status of the refresh request. Top priority is set if seven refresh requests are being held, and refreshing is executed consecutively until the number of requests is reduced to three.

Although a wait interval of maximum duration (three clocks) is inserted by the built-in wait control unit, if a reset input is applied after power is applied, no wait interval need be inserted in actual applications. Therefore, the wait control register has to be reset when the V40 is used at 8 MHz.

Wait control registers WCY2 (FFF6H), WCY1 (FFF5H), and WMB (FFF4H) write program data at these I/O addresses using an I/O write instruction (figure 31).

Figure 28. Memory Access Generation

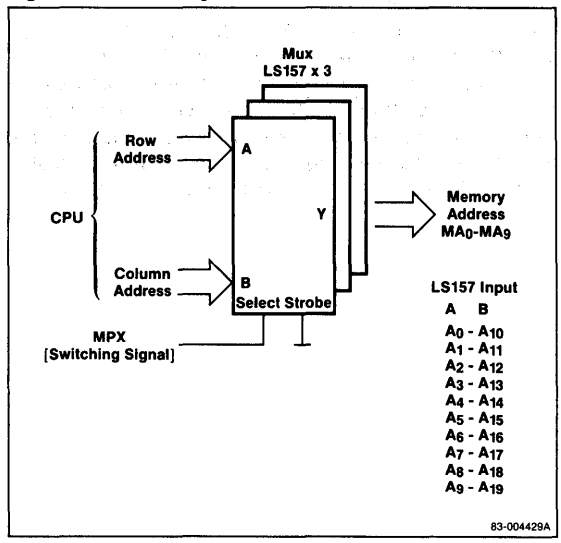


Figure 29. Data Input and Output Control

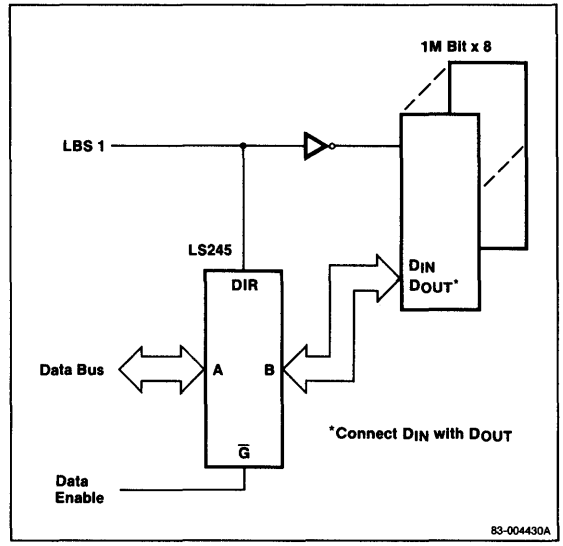
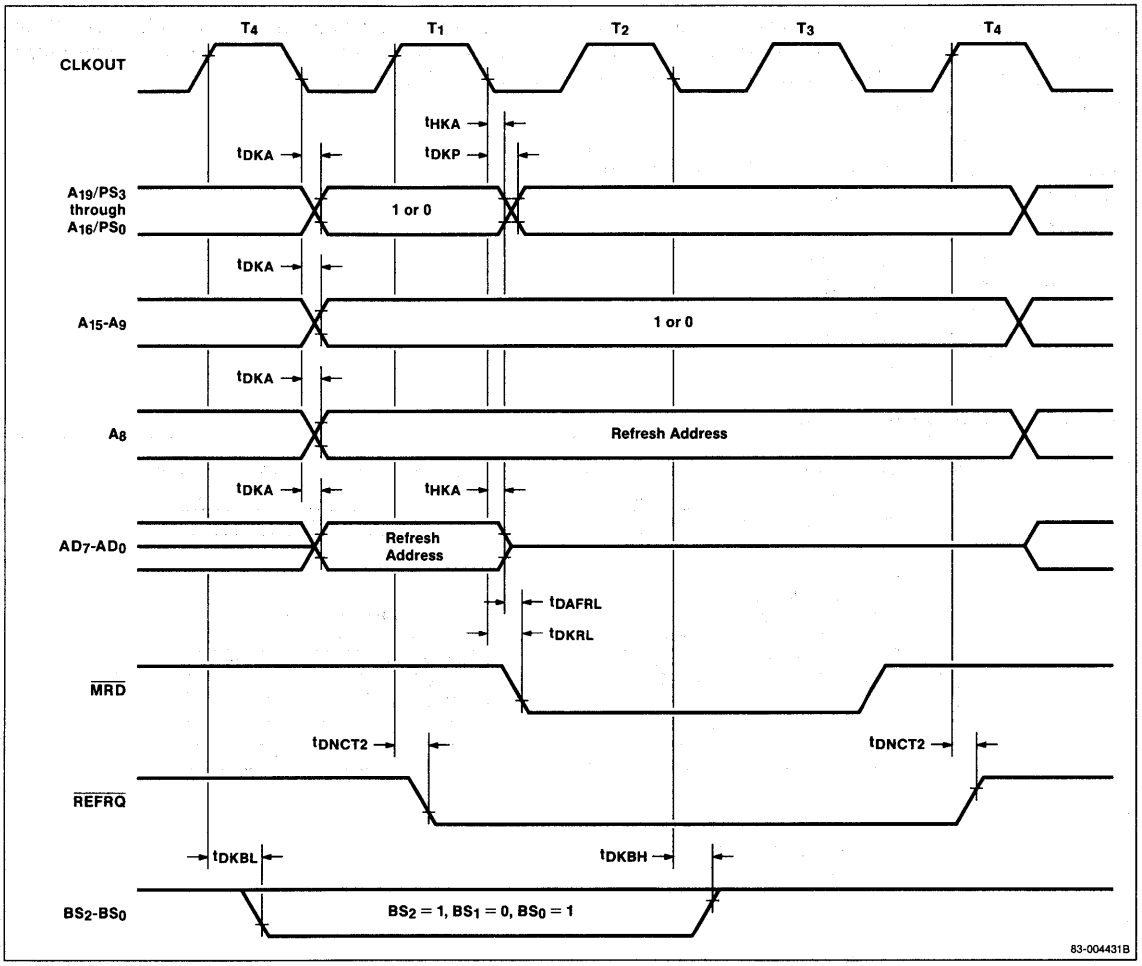


Figure 30. Refresh Timing Cycle



Dummy Cycles

As explained previously, dummy cycles are required to charge certain internal voltage potentials to proper operating levels in the DRAM's internal circuits after power has been applied.

In the following application example, these dummy cycles are implemented by executing eight write (or read) cycles, from 0000H to 00007H, in the memory .

```
        MOV     AL,0000H
LOOP:   MOV     (BL),0000H
        INC     AL
        CMP     AL,00007H
        JNZ     LOOP
```

Composite Schematic

Figure 32 shows the complete schematic. The V40 and 1M CMOS DRAMs are included, as well as circuits to control timing and refreshing.

Figure 31. Register Programming

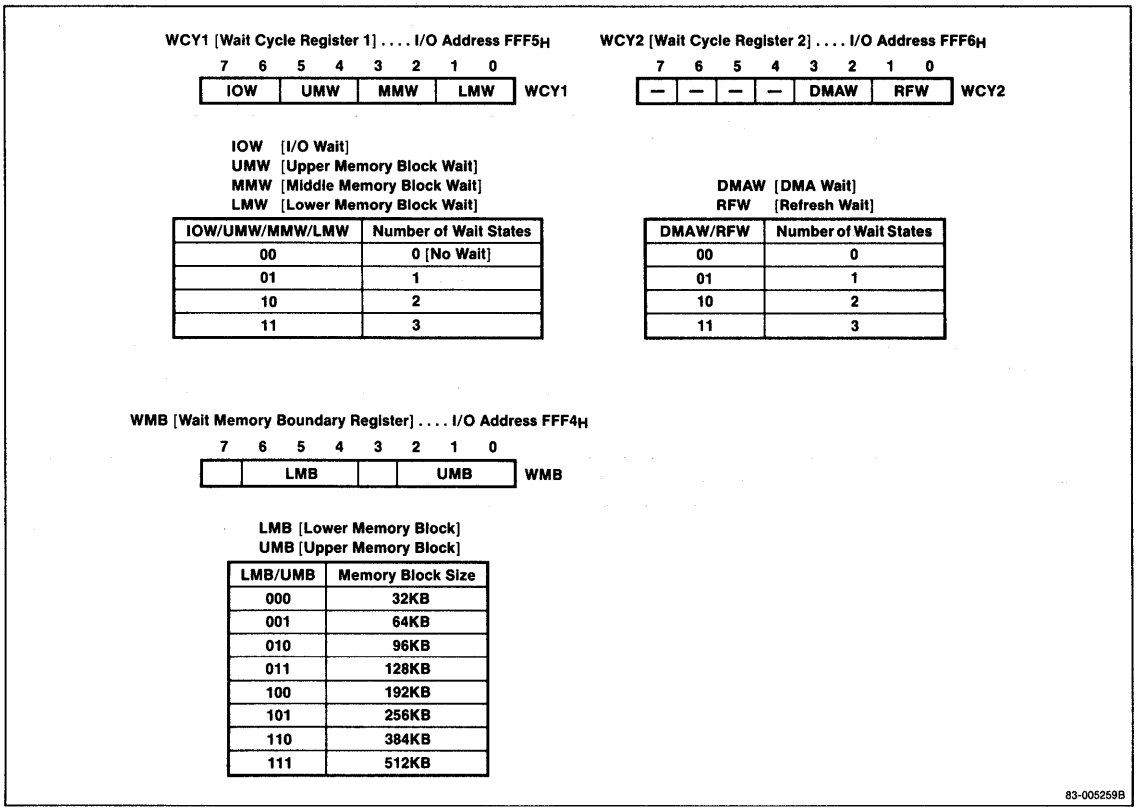
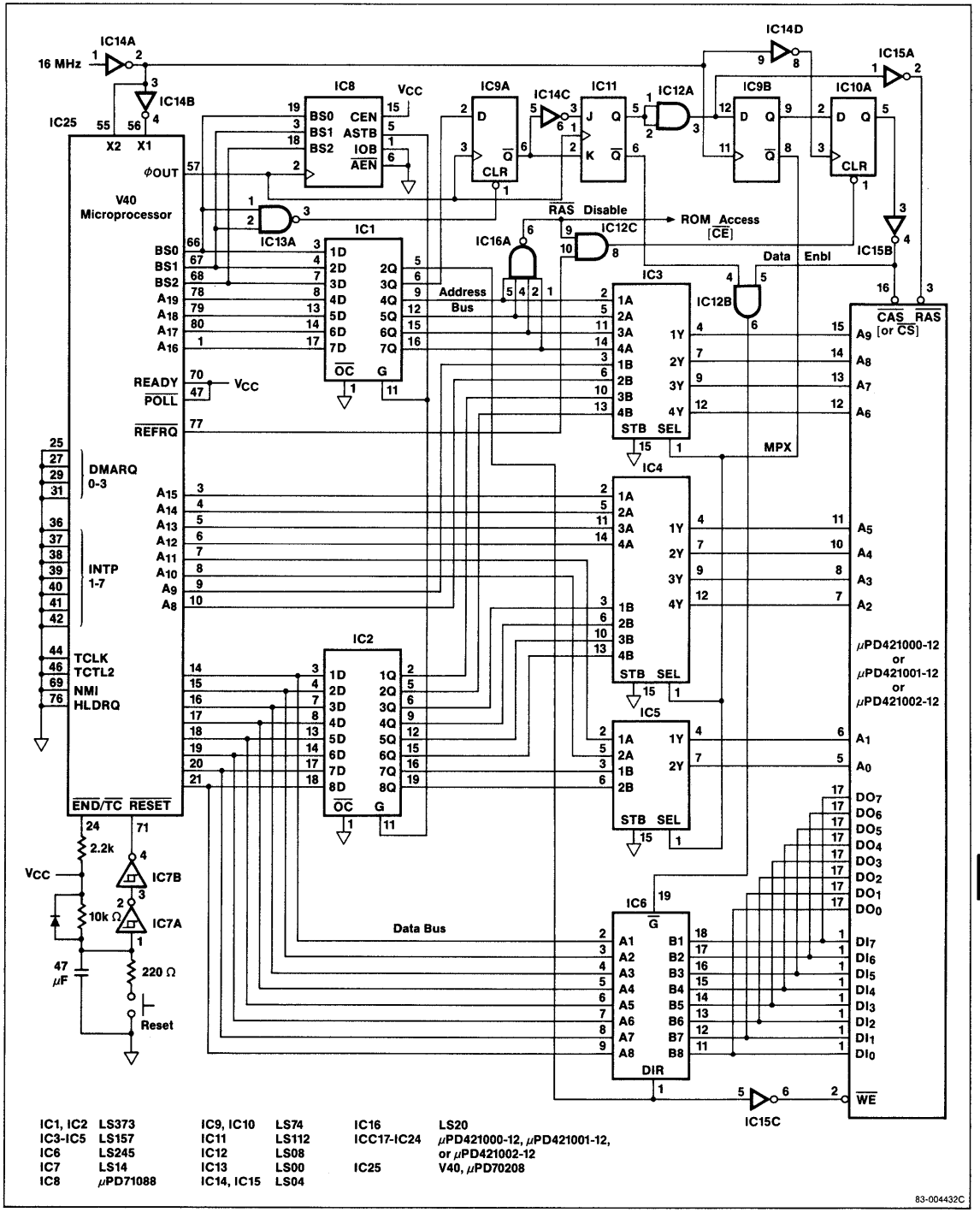


Figure 32. Composite Schematic



15a

INTRODUCTION

A computer graphics system is comprised of hardware and software, the organization of which depends upon the specific requirements of each application. While individual designs may differ from one application to another, the design objective essentially remains the same: to define a device-independent, general-purpose sequence of operations (or pipeline) that transforms the geometric model of an object into an image on a display screen.

This application note provides an overview of the concepts and methodologies used in the design of computer graphics systems. The intent here is to introduce the basics, building the foundation for more vigorous study later.

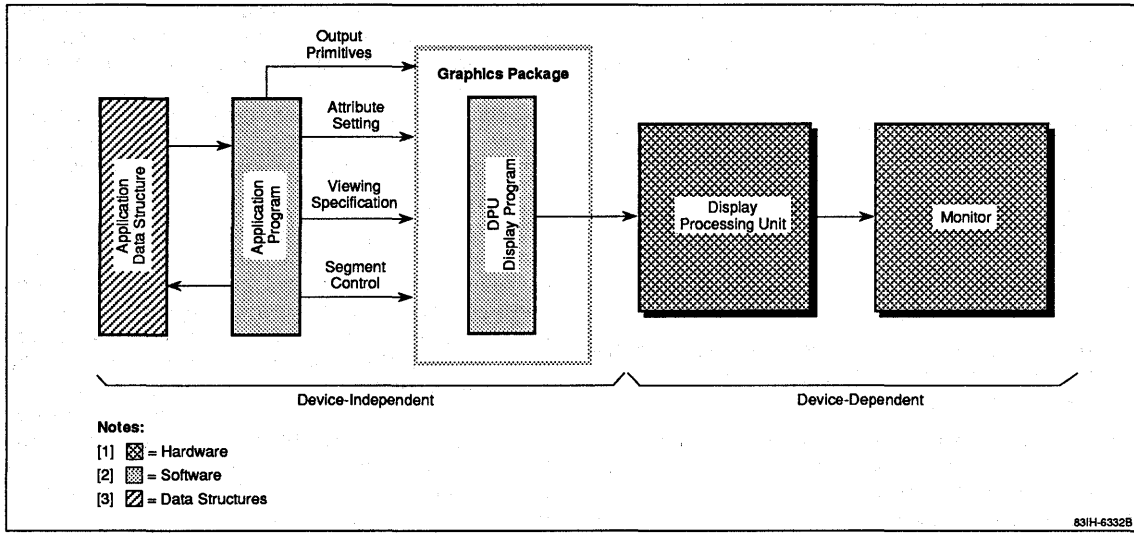
FUNDAMENTALS OF A GRAPHICS SYSTEM

The task of a graphics system is to transform real-world information into a perceptible image for display on an output device. While systems in the past typically used software designed for particular kinds of hardware, contemporary systems use device-independent software designed for compatibility with a variety of hardware.

This latter type involves a sequence of operations that begins with a model of the image to be rendered. As shown in figure 1, the program portion of the model has three elements—the application data structure (data base), the application program, and the display program. These are transmitted to the hardware component, in this case a host computer connected to a graphics display terminal, in terms that the computer can understand. At the same time, the original model structure is preserved. As a conceptual framework, this model is useful in showing how an abstract description of a two- or three-dimensional "world" having one or more objects is transformed into a view or picture of that world.

The functions represented by the conceptual model need to be more than device-independent; they also must be sufficiently general-purpose to support a variety of applications. No strict definition of this requirement exists. At one extreme, the system may be entirely incorporated into a host computer, with the graphics reduced to a single monitor. Another system might incorporate all graphics functions into a standalone workstation. The point is that the implementation of VLSI and concurrent technologies may differ, but the basic sequence of functions must remain the same.

Figure 1. Conceptual Model



One of the tasks of the application program is to support interactive input devices that allow the user to specify how objects are to be constructed and modified and which views are to be displayed. The application program decodes user-supplied input and uses it to direct the system to change the viewing specification or to alter the model in the data structure. Once the application program has developed the data structure, the objects contained therein are described to the graphics system so that it can calculate and display the particular view desired.

The application program describes in geometric terms that portion of the world in which the picture should appear. This data is presented in the form of output primitives such as points, lines, polygons, or character strings geometrically oriented in a two- or three-dimensional world. The application program also specifies the part of the object to be rendered, the vantage point to be displayed, and the part of the viewing surface on which the image should appear.

Problems inherent to the design of graphics software are solved by a graphics package that reinforces a general-purpose, device-independent approach to graphics design by providing basic subroutines or primitives that allow portability with the application program.

The graphics package is a small but functionally complete set of application-independent facilities for creating arbitrary views of two-dimensional objects and for supporting interaction between the application program and the user. The package also performs a number of roles crucial to supporting a range of physical devices controlled by a device-independent application program. These roles can include

- Providing the characteristics and performance capabilities of devices that can be driven by the application software
- Having responsibility for specifying a set of attributes and operations
- Serving as an interface between the applications program and the graphics display unit
- Serving as an interface between the demands of the graphics system and the true functionality of the real devices to be used by the system

The graphics package must therefore be designed not only as an abstract machine capable of supporting the tasks required by the application program, but also as a real machine for implementation on real devices. The key to device-independence is that only the implementation of the graphics package (and not the rest of the application program) is device-dependent.

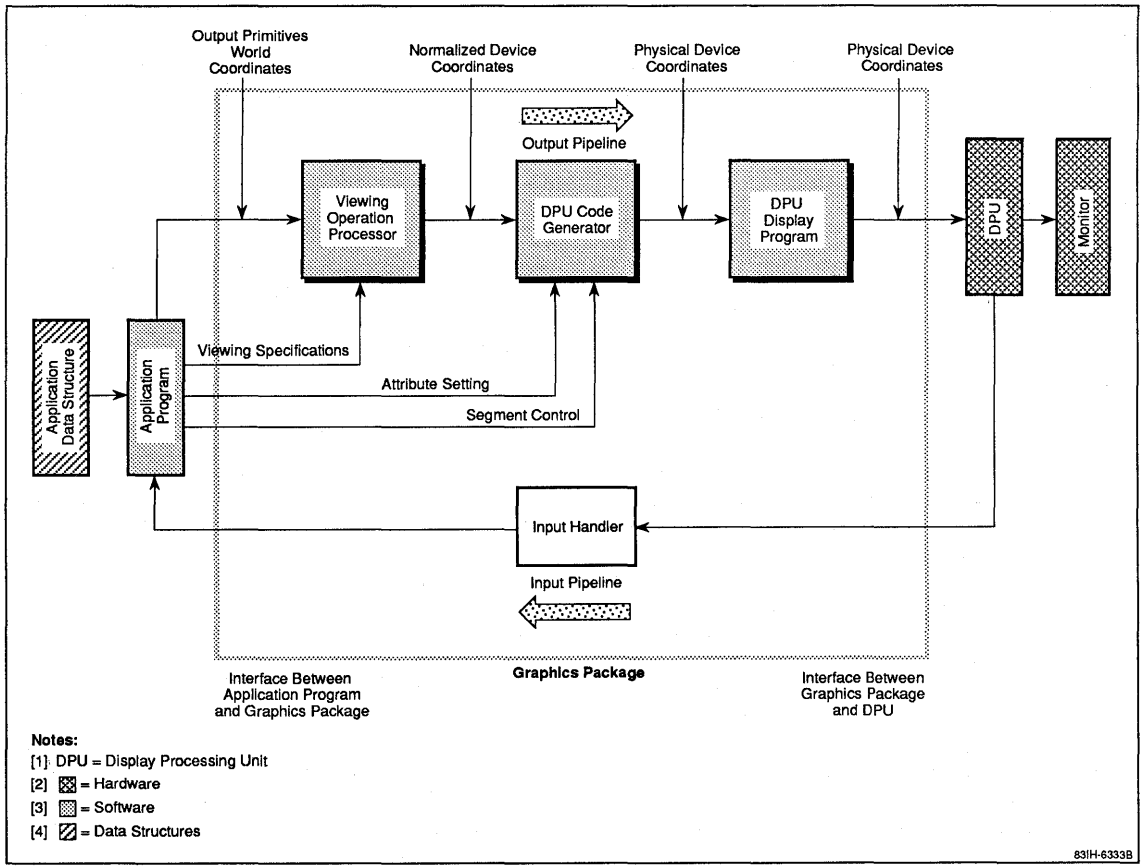
The two principal hardware components are the host computer and the display processing unit, or DPU. The two important data modules shown are both stored in shared memory (to simplify the diagram, the host's CPU and the memory shared by the CPU and DPU are not shown in figure 2). The first is the DPU display program (also called the display file or list), which is written by the graphics package and read by the DPU as it refreshes the image on the screen. The second is the application data structure, which contains a description of the objects whose images are to be displayed and is a tool to model the objects.

The three major stages shown as software modules in figure 2 could also be implemented as hardware or firmware modules in other systems. Their interaction is characterized by two major data flows moving in opposite directions within the system: one is from a data structure description of an object to its image on the screen, and the other is from user-supplied input to the data structure and/or display program.

The object-to-image transformation sequence begins at the output pipeline, a four-stage pipeline that transforms a description of the object into successively more machine-dependent representations, and finally, into an image on a screen. The portion of the data structure that models the geometry (layout) and topology (connectivity) of an object is transformed by the application program into a sequence of calls in a graphics package using parameters derived from the data structure. These calls describe the object in terms of its point, line, and text output primitives. Other calls specify how the object should be divided into logical units, i.e., segments, as well as which view of the object should be displayed.

The next stage, the viewing specification, is used first to clip the object's primitives against the user-supplied window boundaries and then to map the visible portion of the object into the current viewpoint. The DPU code generator transforms the device-independent specification of (clipped) primitives from normalized device coordinates of the DPU. The graphics package controls the segmentation of this DPU "machine code" and specifies to the DPU code generator which segments are to be added, made visible/invisible, translated, or deleted. The final stage involves the DPU itself, which transforms output primitives into the actual data needed for outputting an image onto the display screen.

Figure 2. Functional Block Diagram



The input pipeline has fewer stages. The DPU records input device usage and either interrupts the CPU or transfers data on request. Input data is collected from the DPU by the input handler, which typically passes it to the application program. This data changes the flow of the application program, and may also cause the application program to either modify the data structure or change the viewing operation parameters. The input may also be used directly by the code generator to manipulate segment operations.

THE VIEWING OPERATION

The viewing operation is a sequence of steps that transforms a device-independent description of an object into a device-dependent display program generating a particular view of an image. In the viewing operation processor and DPU code generator stages, functions such as clipping, window-to-viewpoint mapping, and display code generation in device-dependent physical screen coordinates are performed. The first two steps are usually considered part of the viewing operation, while the third step is part of the DPU code generation process.

OUTPUT PRIMITIVES

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Coordinate Systems

In a basic graphics system, the only graphical primitives needed by the application program are those to define points, lines, and displayed text strings. These are described in terms of positions and measurements in a Cartesian coordinate system. The coordinates are inherently dimensionless, and thus the application program can define objects in terms of units that are natural to the application and to the user.

The application program is constrained by the overall size of display space on the output device. Display space can be divided into a number of rectangular regions called "viewports," into which subpictures are mapped. Subpictures require the use of a suitable application coordinate system. Such a coordinate system is the world coordinate system, used by the application program to choose a rectangular "window." Any finite rectangular region of this infinite space, where the sides of the rectangle are parallel to the x and y axes, is a window in the world coordinate system. Because different window sizes can be used, the image is drawn in world coordinate space relative to a particular window and then clipped to that window. To be able to transform these windows into their allotted viewports on the screen, the application program must have procedures for specifying windows, viewports, and appropriate coordinate systems.

The window is defined in terms common to the world coordinate system, where the edges of the rectangle are parallel to the x and y coordinate axes. The viewport procedure also takes a rectangular boundary as its parameter; the system in which this boundary is expressed is called the device coordinate system, i.e., the one used for representing absolute positions on the display space. Since device coordinates map directly onto the display device, the range of coordinates will define display resolution.

Often a graphics system supports many different devices, and the application program must provide a means of controlling these in as uniform a manner as possible. Determination of the viewport using device coordinates is acceptable if only one graphics device is used, or if all graphics devices have exactly the same coordinate systems to represent their display spaces. A better solution to device disparity requires a uniform method of addressing different display spaces. The standard solution is to introduce an intermediate system called normalized device coordinates, where (0,0) is at the bottom left corner and (1,1) is at the top right, i.e., a unit square.

Windows and Clipping

The viewing operation, or pipeline, has been defined as a journey of a coordinate through the graphics system. It starts as a world coordinate point generated by a call to an output primitive procedure, continues through the normalized transformation stage, and finally passes through the device transformation stage, after which it is expressed in normalized device coordinates.

During this procedure, the graphics package must know what portion of the essentially unbound world coordinate space is to be displayed. This rectangular region, or window, is invoked by a graphics package procedure that maps the image of the window boundaries to coincide with the edges of the screen. A programmer can make the graphics package display only that portion of an object which is in view by surrounding the desired part with an appropriate window.

Any part of the object not in view inside the window is made invisible by the graphics package through a process known as clipping, whereby any primitive lying entirely outside the window boundary is not mapped to the screen, and any primitive lying partially inside and partially outside is cut off. Each output primitive defined by the application program is tested to see whether it is entirely inside the window, intersects the window, or lies entirely outside the window. The pieces that remain after testing and clipping are mapped to the screen.

The most basic form of clipping involves output primitives such as points, lines, and text (figure 3). Even with these simple primitives, it is essential that the clipping operation be done efficiently since hundreds or even thousands of lines must be processed as quickly as possible to provide the next view of the object as smoothly as possible.

Window-to-Viewport Mapping

In this context, window is a rectangular area that specifies the part of a scene—either graphics or text—to be displayed and is defined by means of coordinates in the lower right and upper left corners. (The type of window commonly associated with a page of text or graphics, or possibly the dynamic output from a process or program, does not apply to this discussion.)

A window defines what is to be displayed but not where it is to be displayed. Therefore, each window requires a corresponding viewport that defines the space into which the window is to be displayed. In figure 4, the window is clipped to its boundary in world coordinates, and then subsequently mapped to the viewport boundaries in device coordinates. A few windows appear whole, while some are obscured by other windows. A viewport obscures another viewport when it has a higher priority than the obscured viewport. Viewports may be moved around the display area without affecting their information content, except when they are moved relative to an obscuring viewport.

The movement of a window about the scene gives the effect of changing the observer's view of the picture. Adjusting the size of the window relative to the size of the objects being displayed produces arbitrary scaling effects. Thus, moving the window and selecting smaller

or larger window sizes creates the cinematic effect of panning in or zooming out. In theory, one can zoom in on a single primitive until it touches the boundaries, or zoom out until the entire scene blurs together as a single port.

If the graphics package supports only a single DPU, then it is most efficient to convert directly from world coordinates to physical coordinates. For packages that support multiple display devices, it is convenient to produce a low-level, machine-dependent, normalized device coordinate representation of the image that can then be translated by multiple DPU code generators to the appropriate physical device coordinates. Therefore, window-to-viewport mapping is a conversion process in which the window, defined in world coordinates, is converted into device or normalized device coordinates for input into the next phase of the viewing pipeline (figure 5).

Figure 3. Example of Two-Dimensional Clipping

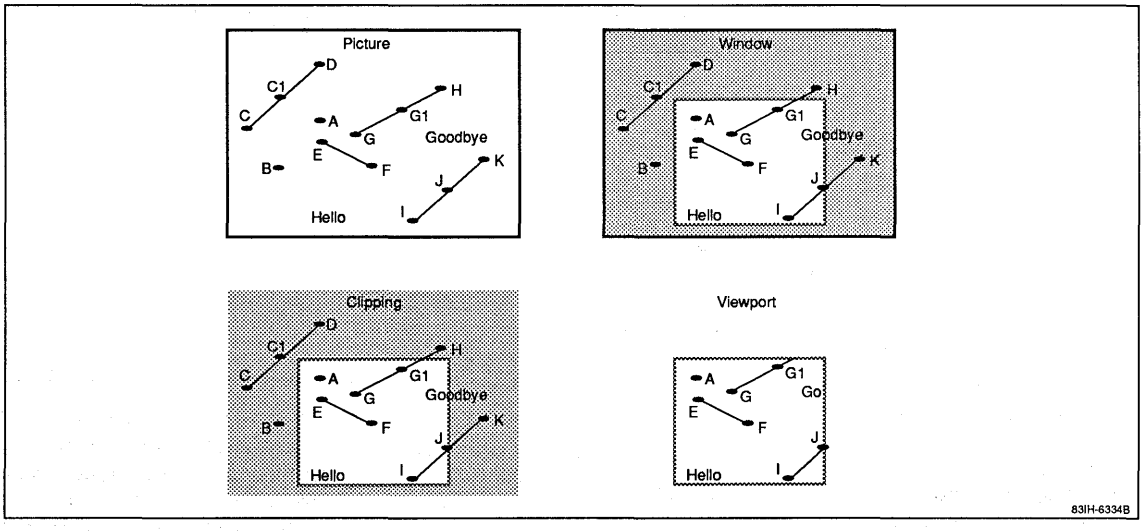

Figure 4. Window-to-Viewport Mapping

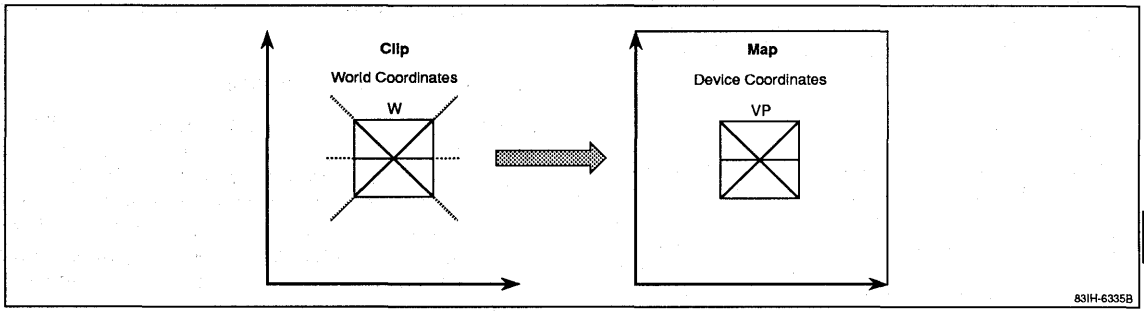

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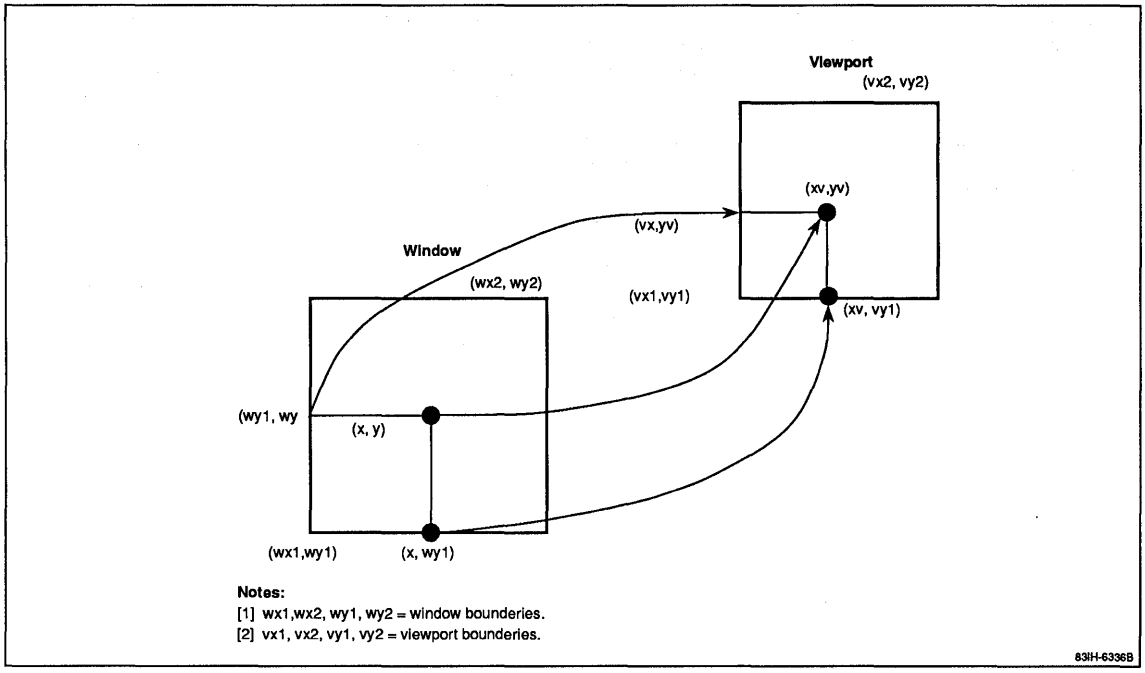
Figure 5. Window Boundaries Mapped to Viewport Boundaries



DPU Code Generation

This stage in the viewing pipeline converts the clipped and mapped output primitives to normalized device coordinate space, unless this conversion was already performed in the window-to-viewport mapping phase. Device-independent primitives are converted into actual DPU commands with operation codes, functions, and beam displacement fields in physical device coordinates.

Segmentation

The final stage, segmentation, involves organization of the output primitives into logically related segments for selective identification and modification of the image. Once a picture of an object has been created and drawn, changes to the drawing can be made by means of modifications to the data structure. Producing an updated view of the modified object(s) by having the application program redescribe everything to the graphics package, even though only a portion has been changed, would be very wasteful because of the computations required to clip and map world coordinates into device-dependent coordinates.

Segmentation, where the object's description is partitioned into segments that are individually displayed, provides the system with an extra dimension of flexibility, a way of creating a high-level representation of the total picture. Each segment consists of attributes determining the state of the segment, as well as a sequence of output primitives. Fast selective modification is a necessity of high-quality interactive graphics because it provides rapid response to the user for closely coupled feedback.

Geometric Transformations

A graphics system should also provide the ability to scale and rotate images in two- and three-dimensional space. These geometric transformations should be free from device-dependent issues such as screen coordinates so that different views of a picture at different scales may be selected, and repeated symbols in pictures may be drawn at various scales and angles of rotation.

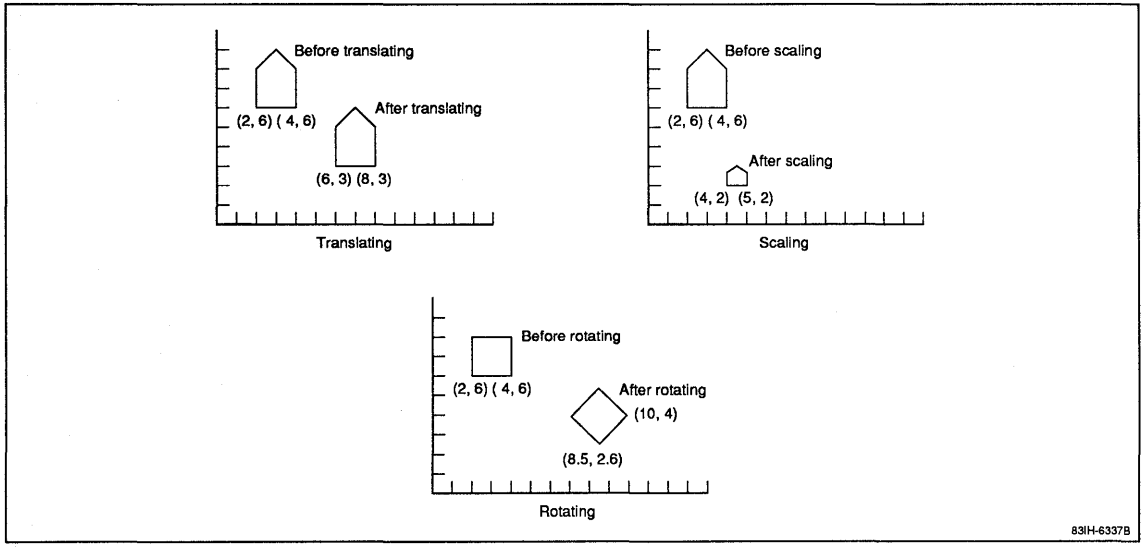
The most common way to view transformations is with 4 by 4 matrix multiplication. However, matrix multiplication requires many intermediate steps, making the transformation of object coordinates one of the most time-consuming steps in the entire graphics output sequence.

Arbitrary two- and three-dimensional transformations such as object rotations, translations, scaling, and per-

spective and orthographic projection may precede the clipping function in the graphics pipeline, and may also include the ability to transform the image into viewport coordinates (figure 6). Because matrix representations for translating, scaling and rotating differ (scaling requires an additional matrix and rotation uses a multiplication matrix), it is more efficient to treat these functions in a consistent way. For example, if they are expressed in homogeneous coordinates, all three transformations could be expressed as multiplications.

Homogeneous coordinates were developed in geometry and have subsequently been applied in graphics (figure 6). Numerous graphics subroutine packages and some display processors work with homogeneous coordinates and transformations. In some cases, they are used directly by the application program in passing parameters to the graphics package. In other cases, they are applied only within the package and are invisible to the programmer.

Figure 6. Transformations



INTERACTIVE GRAPHICS TECHNIQUES

One of the principal goals of interactive systems, graphics or otherwise, is the symbiosis between man and machine. When a user is able to interact with a computer, this interaction is said to be conversational. Working together on a single task merges the capabilities of the two partners, man and computer.

Of all the possibilities for graphics input hardware, the keyboard is certainly the most familiar. Many graphics systems have little more. There are five basic logical input devices: the locator to indicate a position and/or orientation, the pick to select a display entity, the valuator to input a single value in the space of real numbers, the keyboard to input a character string, and a button to select from a set of possible alternative actions or choices. Logical input devices are rather like logical files in an operating system. A sequential input file may be implemented physically by means of a card reader, a magnetic tape drive, a disk drive, or a terminal keyboard. The application program doesn't care because the operating system makes them functionally alike, despite their physical differences.

Many graphics systems simulate the logical functions of another class, although some of the simulations can be rather awkward. These implementations are sometimes part of the graphics package. For example, since a direct-view storage tube cannot be used with a light pen, the cross-hair cursor locator might be used as a pick.

In addition to interactive devices and device simulations, interaction techniques are used as the basic building blocks from which complete interactive dialogues are designed. Interactive techniques are higher-level functions implemented through the basic device simulations already discussed. These techniques, which are general application-independent ways of interfacing with a computer, are routinely used in many graphics packages and include the following:

- **Construction Techniques**—where the physical appearance of an object is indirectly manipulated by means of dragging or rubberbanding.
- **Command Techniques**—where menus and programmed function keyboards are used to input commands.
- **Picking Techniques**—where a hierarchical object structure allows the user to pick a basic object, a collection of basic objects, or perhaps a collection of collections.

When programming graphical input devices, a certain degree of device independence can be gained by providing individual high-level primitive functions for each basic form of interaction. The following list, based on this approach, is adequate for most graphics applications and can be implemented on a surprisingly large variety of terminals.

- **Positioning**—where the user defines a location on the screen. This location is passed back to the program, which uses it to position objects or endpoints of lines.
- **Pointing**—where the user identifies an object already displayed on the screen. This can be used to delete and copy objects or to implement light buttons and other means.
- **Inking**—which is used to specify a free-hand curve as a collection of screen points.
- **Character Recognition**—where the user draws a number of inked strokes that together can be recognized as a text character, an editing mark, or some other symbol.
- **Dragging**—where coordinates from a graphical input device are used to specify the location of some object on the screen. Repositioning is performed rapidly enough so that the user can "rag"the object around the screen until it is correctly positioned, at which time it is fixed again.

Device independence is just as troublesome here as it is in graphical output. The problem is not that input devices have such different characteristics, but that each input technique demands a specific form of immediate feedback on the screen. The popular rubberband line drawing technique, for example, depends on the dynamic display of a line with one endpoint fixed and the other following the coordinate input device. It is difficult to provide this sort of effect without modifying the graphical output process. Therefore, meddling with the output process should be avoided in the interest of device independence.

DISPLAY HARDWARE

Without special hardware for producing output, there would be little interest in computer graphics. Useful pictures can be produced using only a line printer or a normal hardcopy alphanumeric terminal, but what most people expect from a graphics system is something much more.

Most graphics hardware has options for moving in two dimensions, plotting or intensifying certain points on a surface, displaying characters, and providing gray-level variation or color shading. The number of such devices is increasing yearly and includes vector or raster CRTs, hardcopy drum and flatbed plotters, impact and ink-jet matrix printer/plotters, color copiers, LED displays, plasma panels, and laser printers. In this discussion, the focus will be on CRT technology for vector and raster scanning, with emphasis on the system architectures needed to implement such devices in a graphics system.

CRTs for Raster and Vector Scanning

The DPU is a special-purpose CPU with its own set of commands, data formats, and an instruction counter that executes a sequence of instructions called the display file to create an image on the display device. Individual DPU instructions typically are used to draw a point, a line, or a character string. Interactive devices attached to the DPU can also be used to input commands and other information.

The DPU can be organized to create an image, either by random or raster scanning. In a random scanning system (sometimes called a vector, stroke, or calligraphic scanning system), parts of the drawing can be depicted in any order on the display. For example, the house in figure 6 was drawn by moving (detecting) the beam to the starting point, turning it on, and continuously deflecting it between successive endpoints to trace the house outline. In a raster scanning (TV-type) system, all parts of the drawing in the first line are reproduced in left-to-right order, followed by all parts of the drawing in the second line, and so on. Hardcopy devices operate in either a random or raster scanning system. The printer, a simple hardcopy device, has a print head that moves from left to right and top to bottom. The pen plotter, which uses a pen that can be moved in any direction over a piece of paper, is a random scanning device.

Figure 7 shows basic display techniques. Starting in the upper left of the screen, the intensity is modulated during the left-to-right sweep to create different shades of gray. At the right edge, the beam is blanked (turned off), repositioned (indicated by the dashed line) at the left edge one unit down from the previous scan line, and

unblanked. After all scan lines have been drawn, the beam returns to the upper-left corner. Broadcast television in the United States operates with 525 scan lines, but common raster graphics systems use anywhere from 256 to 1024 lines. The more lines used, the higher the picture quality.

Display Processing Unit for Random Scanning

Figure 8 shows a very simple DPU capable of randomly plotting under CPU control individual discrete points on a grid of 1024 by 1024 lines. This feature requires that 10-bit x and y values be made available to the DPU. The computer uses input/output commands to load the x and y registers with coordinate values, while the analog (voltage) equivalents of the coordinate values go to the deflection system. The current amplifiers for the magnetic deflection coil produce the appropriate current. Once this current has stabilized, the electron beam is unblanked (turned on) for a few microseconds, and then blanked again to detect and draw the next point. The whole process can take from 5 to 20 μs per point with a fast deflection system, or as much as 50 μs per point with a slow deflection system. In a given system, the time between the display of successive points is usually nearly proportional to the distance between them. A refresh rate of 30 cycles per second allows 33,000 microseconds per refresh cycle, resulting in display capacities from 33,000/50 = 660 to 33,000/5 = 6600 points.

The system in figure 8 has no facilities for concurrent program execution and display of screen refresh capabilities. Most contemporary DPUs provide the same functions as a general-purpose CPU, functions such as an instruction counter, instruction register, and control logic that allow the DPU to execute instructions as well as to refresh the display.

Figure 7. Display Techniques

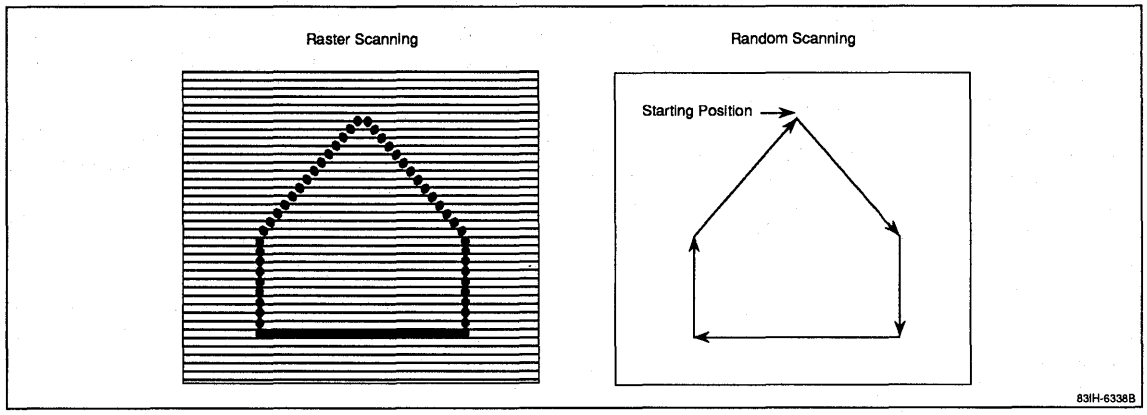
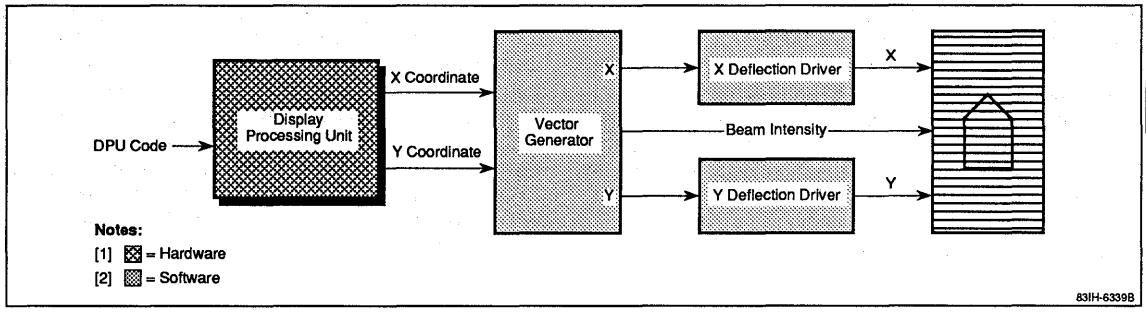


Figure 8. Random Scan Display Technology



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Display Processing Unit for Raster Scanning

The DPU illustrated in figure 9 provides a number of features to enhance operation. The CPU loads a DPU program into main memory, loads the DPU with the starting address, and tells the DPU to start the execution of the DPU program. The DPU cycle "steals" from the CPU's memory whenever it needs a new instruction. Thus, converting the display to an autonomous processor relieves the CPU of the refresh task.

Images to be displayed by a random scanning system are encoded as commands to draw each output primitive using endpoints of lines as coordinate data values. The encoding for raster scanning systems is much simpler: output primitives are separated into their constituent points for display.

The major differences in simple point plotters, random scanners, and raster scanners occur in their organization of stored bits. In point plotting displays, the component points of each successive output primitive are stored sequentially and are plotted in that order, one picture element at a time becaise the beam may be moved randomly on the screen. Conversely, the refresh memory in the raster display is arranged as a two-dimensional array. The entry at a particular row and column stores the brightness and/or color value of the corresponding (x,y) position on the screen in the simple one-to-one relationship shown in figure 9, i.e., each screen and memory location is referenced by an x coordinate (ranging from 0 to m–1) and a y coordinate (ranging from 0 to n–1). The top row of memory corresponds to the top scan line, the second row of memory to the second scan line, and so on. Image refreshing is performed by means of sequential raster scanning through the buffer, by scan line rather than by output primitive as in random scanning.

The job of the image refresh system is to cycle, row by row, through the refresh buffer, typically 30 to 60 times per second. Memory reference addresses are generated synchronously with the raster scanning device, and the contents of memory are used to control the CRT's beam intensity. The raster scanning generator provides deflection signals that generate the raster scanned image and also control the x and y address registers defining the location of the image to be fetched so as to control the CRT beam. At the start, the x address is set to 0 and the y register to n–1 (the top of the scan line). As the first scan line is generated, the x address increments from m–1. Each point is fetched and used to control the intensity of the CRT beam. After the first scan line, the x address is reset to 0 and the y address decrements by 1. The process continues until the last scan line (y = 0) is generated.

Display Resolution

The number of raster lines capable of being displayed on a monitor depends not only on the speed at which the electronic beam can be moved across the screen, but also on the quality of the electronics controlling the beam. Similarly, the number of horizontal points that can be plotted depends on the speed at which the beam can be switched on and off. The more raster lines and horizontal points that can be drawn, the greater the total number of points that can be displayed, and hence, the greater the resolution of the display.

Consider a CRT monitor with m pixels on each line and n raster lines. If the time required to draw one pixel is P_t and the time for horizontal retrace in H_t, then the total time to display one raster line is $L_t = MP_t + H_t$. If the time for one vertical retrace is V_t, the total time to draw one complete image is $t = N(MP_t + H_t) + V_t$. If there are to be raster frames per second, then rearranging the above for P_t means that the time to draw one pixel is $P_t = 1/MN_r - V_t/MN - H_t/M$. This value, usually expressed as a frequency, represents a measure of the monitor's resolution capability and defines the electronics performance required to achieve a particular display resolution, generally known as monitor bandwidth.

Typical bandwidth figures for refreshing of the whole image 60 times a second (60 Hz) are 28 MHz for a display of 512 by 768 pixels and 88 MHz for a display of 1024 by 1024 pixels.

SUMMARY

The aim of this application note has been to provide an overview of a graphics system, defining some of the fundamental operations required to render an image onto a display device. By no means comprehensive, the discussion should at least have provided a framework for understanding the common techniques and terminology used in a number of today's very sophisticated applications, whether implemented in state-of-the-art VLSI technology or organized into a higher performance parallel architecture.

Figure 9. Raster Scanning Display Technology

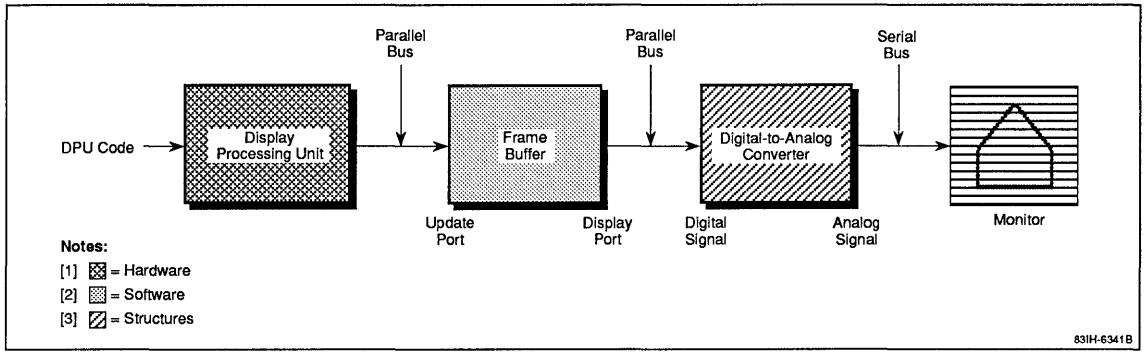
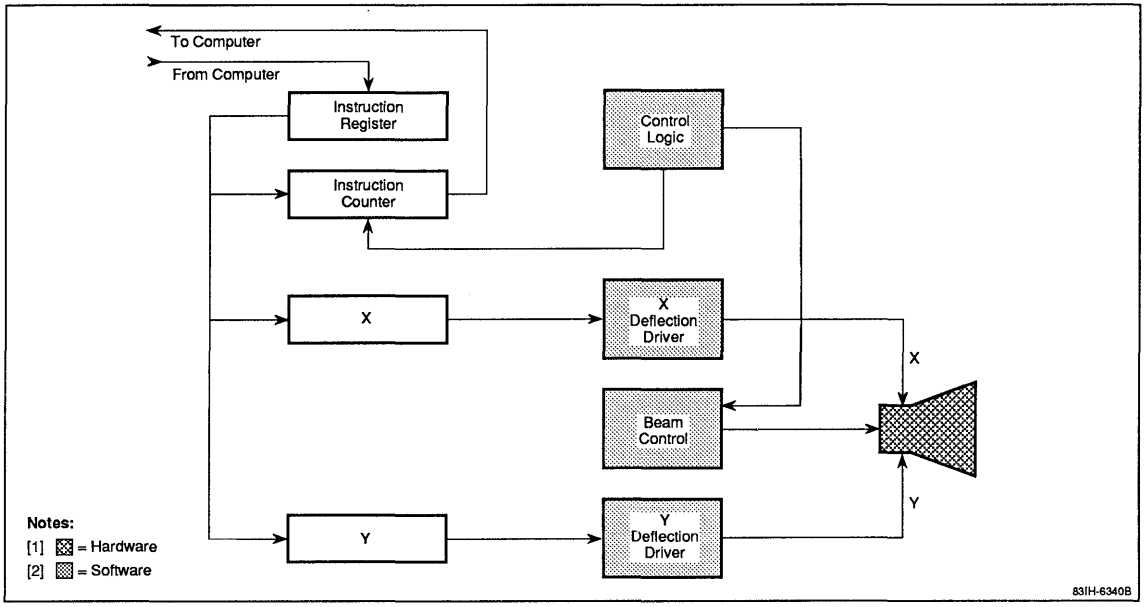


Figure 10. Raster Scan Instruction Counter



15b

Introduction

The growth of computer graphics is directly attributed to the availability of reasonably priced, high quality display hardware. The technology most successfully addressing this feature is called raster scanning, a type of graphics found in television applications and one that makes it possible for complex, flicker-free images to be displayed.

Frame buffer architecture is important in determining the performance of the entire raster display system. For example, although frame buffer architecture is restricted by the refresh requirements of the display (i.e., how fast a new image can be generated in response to user input), architecture of the entire graphics system is affected as well. This application note discusses some of the design techniques inherent to frame buffer architecture.

Raster Scanning

A raster display system constructs an image as a series of horizontal lines, each composed of picture elements (pixels) whose intensity is controlled by a bit map generated on the display processing unit (DPU) in accordance with graphics primitives defining the unit. The device buffering the bit-mapped image is called the frame buffer, or image memory, and is usually designed with dynamic RAMs (figure 1). Each storage cell in the frame buffer corresponds to a pixel that maps to a point on the display screen. Data stored in the frame buffer is systematically read by the DPU (video controller) and then used to refresh the CRT monitor displaying the image.

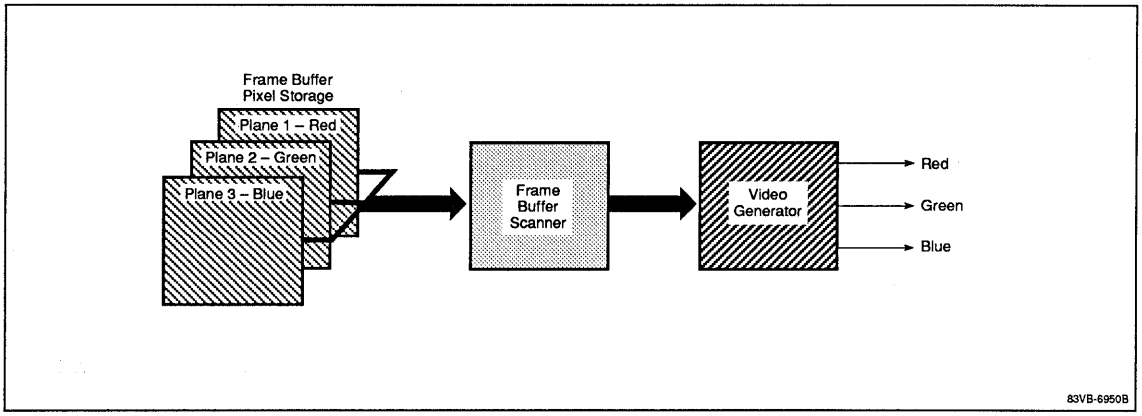
Frame buffers are usually sized in the horizontal and vertical directions as a power of 2, in particular 256 by 256 (2^8), 512 by 512 (2^9), or 1024 by 1024 (2^{10}) pixels. Sizes based on the aspect ratio of the screen (e.g., 768 by 512 or 1536 by 1024) are also common. These dimensions then become device coordinates of the raster scanning display system.

The bits in the frame buffer are scanned by the DPU in a left-to-right, top-to-bottom sequence. They are then read in parallel and serialized by a scanner that outputs the pixels to the video generator. The pixels modulate the CRT beam signal in proportion to the values in the frame buffer.

Refresh Requirements

The design of frame buffers is determined in large part by the requirements of the application. A stable display is generally the foremost requirement of a graphics system. Therefore, the first design consideration should focus on how the video's refresh controller will supply data to the output hardware when pixel time is less than a buffer cycle.

Figure 1. Frame Buffer Organization



The frame or image buffer stores a bit map representing the image to be displayed. The size of the frame buffer, often 512 by 512 or 1024 by 1024, is the resolution of the memory, with each element being one pixel. The DPU must update the frame buffer with the bit-mapped image and periodically refresh the display. Refresh requirements are determined by a number of factors, including the DPU's refresh rate, vertical and horizontal retrace time, screen resolution, and access time of the memory used in the frame buffer. When all of these factors are established, the architecture of the frame buffer can be determined.

Two standards developed by the Electronic Industries Association (EIA) define the timing of video signals. EIA standard RS-170-A specifies interlaced video signals at 30 frames of 525 lines per second each for typical television applications, RS-343-A specifies 30 frames of 1024 by 1024 noninterlaced images per second or 30 frames of 512 by 512 noninterlaced images per second for high-resolution television applications.

Knowing how often a new pixel must be supplied to the output device is crucial to determining how quickly image memory must be accessed to support the refresh requirement. Pixel time, the active line time divided by the number of visible pixels per line, can be derived from either the refresh rate, the vertical or horizontal blanking interval, the number of lines displayed per frame, or the number of pixels displayed per line (figure 2).

Table 1 gives the values used to derive pixel times for several popular display formats. Pixel times will vary from system to system, depending on the number of visible lines and the number of pixels per scan line. However, these figures are typical: (1) 100 ns for 512 x 512 at 30 Hz; (2) 45 ns for 512 x 512 at 60 Hz; (3) 25 ns for 1024 x 1024 at 30 Hz; and (4) 10 ns for 1024 x 1024 at 60 Hz.

The storage cell is the principal element in a frame buffer, which is why advances in frame buffer architectures have been paced by advances in the cost, performance and structure of these chips. Storage bandwidth is of primary concern in the design of frame buffers, and while dynamic devices have historically evolved to deeper and deeper organizations, the width of the access port (e.g., 1M x 1 or 256K x 4) has experienced almost no change.

The trend toward deeper organization meets the needs of main buffer designs, but doesn't provide a solution for potential bandwidth requirements. Furthermore, resolution isn't expected to grow significantly beyond the 1280 by 1024 now used in most applications, which means the need for higher density video buffers is limited (figure 3). Consequently, for a 1K x 1K display operating at 60 Hz, a pixel rate of 10 ns (as well as parallel accessing of the frame buffer) is required.

Figure 2. Pixel Time

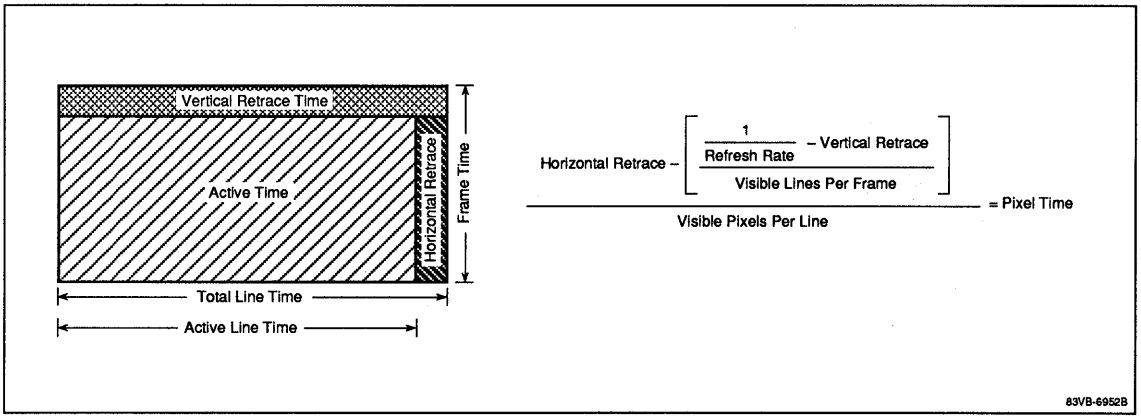


Table 1. Video Timing for Various Display Formats

Visible Area Pixels x Lines	Refresh Rate (Hz)	Interlaced	Vertical Retrace Time (μs)	Horizontal Retrace Time (μs)	Total Line Time (μs)	Pixel Time (μs)
512 x 485	30	Yes	1271	10.9	63.56	102.80
640 x 485	30	Yes	1271	10.9	63.56	82.30
512 x 512	30	Yes	1203	10.9	60.40	96.70
1024 x 768	30	Yes	1250 [1]	7.0 [1]	40.10	32.37
1024 x 1024	30	Yes	1250	7.0	30.11	22.57
1280 x 960	30	Yes	1250	7.0	32.12	19.62
512 x 485	60	No	1250	7.0	31.79	48.41
640 x 485	60	No	1250	7.0	31.79	38.73
512 x 512	60	No	1250	7.0	30.11	45.14
1024 x 0768	60	No	600 [2]	4.0 [2]	20.92	16.52
1024 x 1024	60	No	600	4.0	15.69	11.42
1280 x 960	60	No	600	4.0	16.74	9.95
1280 x 1024	60	No	600	4.0	15.69	9.13

Notes:

(1) Nominal RS-343-A specifications.

(2) Typical high-performance monitor specifications.

Figure 3. Color Monitor Standards

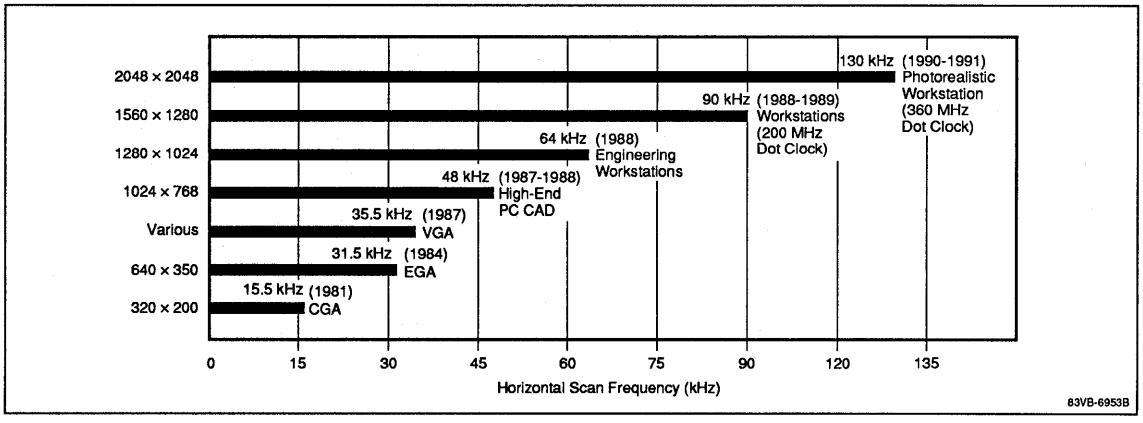


Table 2 shows the effect of using a device with a 4-bit organization, which can read and write four bits in a single cycle and provide four times the bandwidth of a 1-bit chip of equal capacity. This wider organization has figured prominently in frame buffer design, and as system performance requirements increase, ever wider organization may be required.

Table 2. Performance of Storage Chip

Organization	Time to Fill (ms)
4K x 1	1.6
16K x 1	6.6
64K x 1	26.2
256K x 1	105.0
16K x 4	6.6
64K x 4	26.2

Although an 8-bit organization is practical, the evolution toward 16-bit devices will be prohibitive because of pin configuration and package size. Therefore, in order to meet the required pixel rate of high performance graphics systems, the frame buffer must be designed with organizations and features that can best support the increasing performance requirements. Over the years, a number of different design solutions have been proposed. One is to separate the device into a double buffer, one for refreshing the display and the other for updating the image. Another approach is to incorporate the functions needed to update and refresh a display into a VLSI DRAM architecture. Both of these architectures are important in determining overall performance, but the organization of the frame buffer also plays an important role in optimizing its performance in various applications.

Organization

How pixel values are mapped into the update processor's address space has a substantial impact on the speed with which the processor can alter the memory. Two basic types of organization are commonly used to store and access pixels in display memory: pixel and plane organization.

Pixel Organization. In pixel organization, the storage cell is arranged so that all bits in a pixel are contained in the same word. When pixel length is shorter than word length, multiple pixels can be packed into each word. When the graphics processor accesses a word of display memory, all of a pixel's bits are available simultaneously. Therefore, in a pixel-based architecture, frame buffer data is handled one pixel at a time, providing a technique that can quickly access individual pixels (figure 4).

For multiple planes, the address to the plane buffer generates a data word composed of pixels at the same location across multiple planes. Because the pixel organization addresses individual pixels, there are no problems regarding word alignment during image transfers. This architecture is often found in image processing and solid modeling applications, where the value of each pixel is very computation-intensive because of color value or shading variations.

Plane Organization. In plane organization, the frame buffer may be viewed as a number of separate planes, where the number of planes in the frame buffer is equal to the number of bits in a pixel. In a two-dimensional display memory, each pixel consists of one bit, which can be either on or off, indicating the presence or absence of a dot. Such a display memory supports a monochrome, single-intensity display. In a color display, additional bits at each pixel add color and control the intensity. A four-bit pixel, for instance, can control the CRT's red, blue and green color guns, as well as the pixel's intensity. Each bit with the pixel corresponds to a separate plane.

Planes can provide information other than color. For example, one plane can show a static picture, while another displays an icon that the user can drag around the screen with a mouse. Alternatively, it is possible to use a one-bit plane to mask certain regions of another plane.

In plane organization, display memory is divided so that all the bits associated with one plane are stored in the same area of memory (figure 5). Each word, therefore, comprises bits associated with only one plane. The display memory data is accessed one word at a time. Since a word is usually 16 to 32 bits, the chip must access at least 15 unnecessary bits to be able to manipulate one bit with the pixel. Furthermore, because of the word boundary of 16 bits, a barrel shifter is required if image placement and movement accuracy are needed at the actual pixel level.

Figure 4. Pixel Access

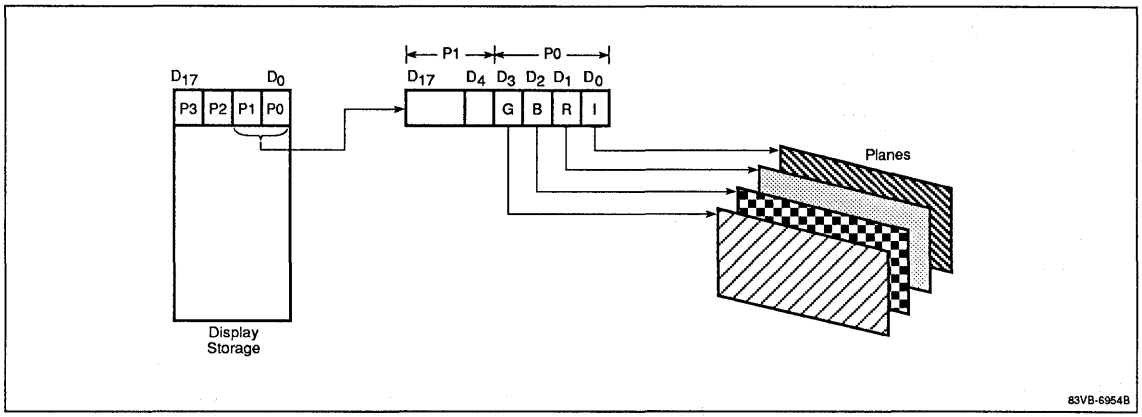
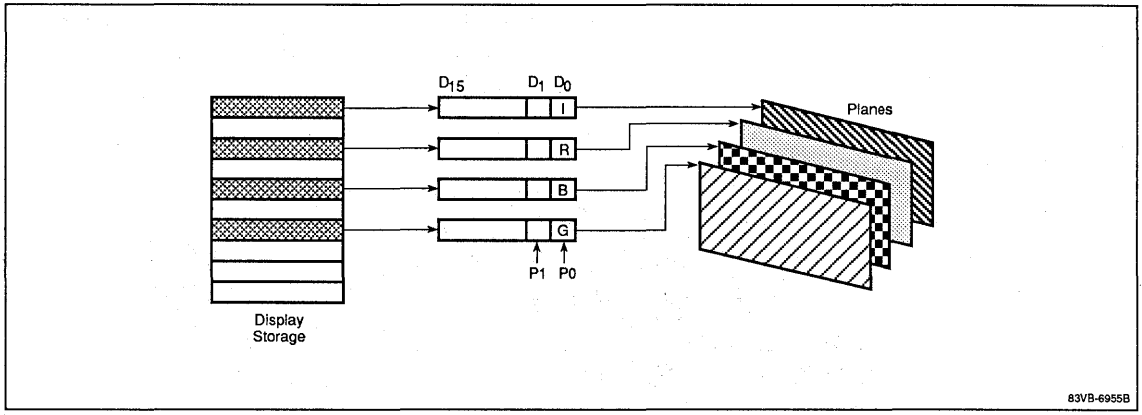


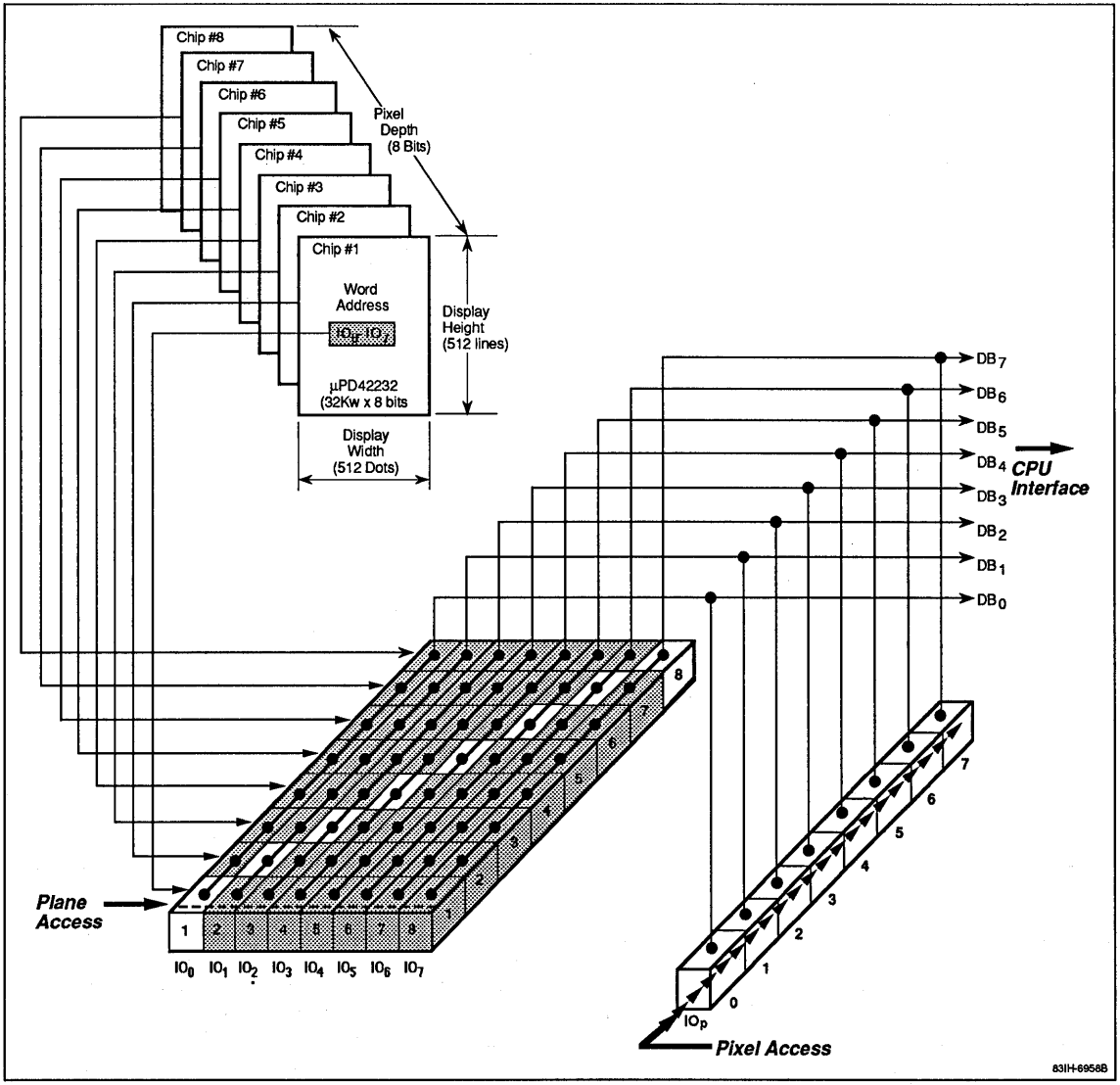
Figure 5. Plane Access



Plane organization is the most popular in engineering and business applications, because they require less intensive pixel computation but more intensive data creation and image movement computation. This architecture costs less and brings with it higher performance when large bit maps must be manipulated.

Pixel and Plane Organization. Some applications need both types of access, in which case the integrated organization shown in figure 6 may be implemented. Access to the frame buffer can be either at word width or pixel depth, providing the best of both types. For example, when pixel information such as a dot pattern for one plane is written to the frame buffer, a number of planes can be written at the same time using plane access. Because individual pixels can be accessed, word alignment when moving images is not an issue. Likewise, when the frame buffer is read, a number of planes can also be read in plane access and a number of pixels can be read simultaneously in pixel access. This enhances comparison functions such as color detection (pixel access) and pattern detection (plane access).

Figure 6. Plane and Pixel Access



Word Alignment

Although plane organization is implemented in a number of popular graphics systems, restrictions associated with word boundary constraints have limited the flexibility and performance of these systems. The pixel and plane combination solves this problem by providing the ability to first access each pixel individually and then switch to plane access.

At the graphic processor level, a number of manufacturers have provided the ability to switch between pixel and plane access or provide a function to align word boundaries. For example, NEC's μPD72120 Advanced Graphics Display Controller™ provides both plane and pixel access. National Semiconductor's graphics chip set uses a plane organization, but takes another approach to this issue by including a BITBLT (bit-boundary block transfer) processing unit chip that is a slave to the raster graphics processor and performs all the masking, word alignment, barrel shifting, data transfer, and Boolean logic necessary for BITBLT operations.

Access Modes

The plane and pixel organizations provide a means of organizing the frame buffer in such a way that its performance is optimized for a number of applications. Also, by providing logical and arithmetic functions that operate on arrays of data, the transfer of data between the graphics processor and the frame buffer can be optimized. These logical and arithmetic functions can be implemented in the instruction set of the graphics buffer or in the architecture of the frame buffer, depending on the application.

BITBLT Operation

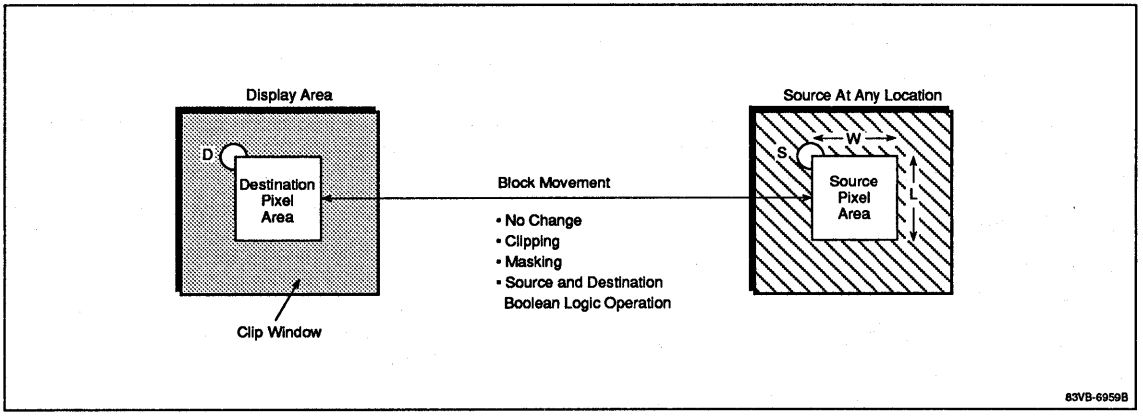
The BITBLT instruction, first developed on the Alto system, provides a powerful capability for bit operation on rectangular areas having the same heights and widths:

- Moves rectangular regions of pixels and is not restricted to contiguous linear arrays
- Operates at any pixel boundary and is not restricted to byte or word boundaries
- Is able to mix the source and destination pixels with a Boolean logical operation and is not restricted to a simple replace destination with source transfer

The instruction copies a source array into a destination array, where the destination array is derived by applying a given logical operation called the *combining rule* to pairs of bits in corresponding positions in the two arrays (figure 7).

The original concept of BITBLT entails a set of 16 specific combining rules that are one of the 16 Boolean operations defined in table 3. The AND function uses its source as a mask to selectively clear parts of the destination, while the OR function selectively sets parts of the destination. Thus the OR can be used to paint shapes into the refresh buffer, perhaps under control of a mouse or tablet. Another use of the OR function is to place text characters defined by bit arrays into a refresh buffer without changing the background pixels around those that form the character itself.

Figure 7. BITBLT Operation



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μPD72120 Advanced Graphics Display Controller is a trademark of NEC Corporation.

Table 3. BITBLT Combination Rules

Bit Pattern	Boolean Expression	Operation
0000	d := 0	CR_0
0001	d := s • d	CR_AND
0010	d := s • $\overline{(d)}$	CR_SND
0011	d := s	CR_S
0100	d := $\overline{(s)}$ • d	CR_DNS
0101	d := d	CR_D
0110	d := s ⊕ d	CR_XOR
0111	d := s + d	CR_OR
1000	d := $\overline{(s + d)}$	CR_NOR
1001	d := $\overline{(s \oplus d)}$	CR_NXOR
1010	d := $\overline{d}$	CR_ND
1011	d := $\overline{(s)}$ • d	CR_NDNS
1100	d := $\overline{s}$	CR_NS
1101	d := s • $\overline{(d)}$	CR_NSND
1110	d := $\overline{(s \cdot d)}$	CR_NAND
1111	d := 1	CR_1

Notes:

(1) s and d are the source and destination bits.

(2) •, $\overline{\ }$, ⊕, and + are Boolean AND, NOT, XOR, OR operators, respectively.

Some versions of BITBLT also use a 16 by 16 pixel halftone or pattern array that functions as an addition mask (figure 8). The halftone array can be used in place of the source or can be ANDed with the source prior to being combined with the destination. This same version of BITBLT also allows a clipping region to be associated with the destination. This can be used, for instance, to clip characters defined by bit arrays much more easily than if the clipping step where part of the viewing transformation process. This speed is crucial, especially for smooth scrolling of text by units of less than one character height. As the name indicates, the BITBLT is a block transfer operation, where the destination is stored as an array of bytes and where each byte represents eight successive bits.

PIXBIT Operation

The implementation of the BITBLT operation can be a tricky endeavor. Source and destination areas may overlap; therefore, the algorithm must be careful to operate in an order that ensures data will not be overwritten before it is used. The problem is further complicated by the arranged of the frame buffer, which is often arranged with 16 or 32 horizontally adjacent pixels in a single word. Because regions do not necessarily fall on word boundaries, corresponding pixels in source and destination words may fall at different bit positions with the words. In order to operate on several pixels within each memory word in parallel, two source words must be available to be aligned with the data within the destination data word. The logical operation is then applied to the aligned words, and the result written to the destination location. This must be repeated for each word containing a destination pixel.

The PIXBLT operation eliminates the need to align operands on word boundaries, because the PIXBLT operation accesses pixels and not words or bytes. The basic PIXBLT algorithm supports combination rules (similar to those found in BITBLT operation) and automatically aligns the source and destination arrays. PIXBLTs operate on multibit pixels, which gives them a speed advantage over BITBLTs in color systems because they perform the operation on all planes at once. They can perform logical and arithmetic operations, transparency detection, plane masking, and color expansion. Because PIXBLTs perform arithmetic operations that require the processor to have the ability to handle carries between bits, a PIXBLT can only be implemented with a frame buffer that has pixel organization. PIXBLTs are useful for performing the Bresenham anti-aliasing algorithm for line drawing primitives.

TILE Organization

Traditional frame buffers are designed so that sequential memory locations lie along a scan line. To refresh a raster scan display, the sequential pixels must be provided at a very high speed. In the past, display refreshing required a significant percentage of the available RAM bandwidth. Video RAMs that separate frame buffer update cycles from video refresh cycles recently became available, allowing almost all of the RAM bandwidth to be used for image updates.

Unlike video refresh cycles, generation of images into the frame buffer is not necessarily dependent on scan lines. In fact, many display operations manipulate groups of pixels having two-dimensional locality. This characteristic allows frame buffer input mechanisms to be organized not as scan lines but as two-dimensional or rectangular arrays called tiles. With this organization, more pixels are updated per memory cycle, thus increasing the data bandwidth between the scan converter and the frame buffer and increasing overall system performance.

The number of pixels updated per tile is also a function of tile organization and the type of operation being performed. In a pixel/plane architecture, tile organizations can be readily handled because packed pixels

can be sequentially accessed. For randomly oriented vectors, a square tile organization gives the highest average number of pixel updates per memory cycle. For horizontal vectors that include polygon fill, a tile organization linearly in the horizontal dimension gives the highest number of pixel updates per cycle.

- A tile is the maximum, simultaneous work area for the graphics processor.
- The more pixels updated per cycle, the higher the pixel performance.
- The number of pixels updated per cycle is a function of tile size.
- The number of pixels updated per tile is also a function of tile organization and the type of operation being performed.

Figure 9 shows an example of a one-plane buffer that supports 4 x 4 tiles and 16 x 1 tiles. The RAM has 16 data lines, with each of the four groups of data lines (A, B, C and D) able to receive a different address. The illustration shows how data lines in the storage array map into the display. Note that for any 16 consecutive pixels in the horizontal direction, each comes from a different data line. Also, in any 4 x 4 group of pixels, each of the 16 comes from a different data line in the array, allowing access of 16 pixels to originate from either a 16 x 1 or 4 x 4 tile, based on the addresses supplied to the different groups of RAM. To access a 16 x 1 tile, all groups of RAM receive the same address. To access a 4 x 4 tile, each group of RAM receives a different address, namely ADDR, ADDR+ M, ADDR+ 2M, and ADDR+ 3M (where M = consecutive memory addresses). Which group of RAM gets each of these addresses depends on the particular 4 x 4 tile being accessed. The fact that the four data lines within a group always have the same address fixes the tiles on four-bit boundaries.

Figure 8. Examples of Combination Rules

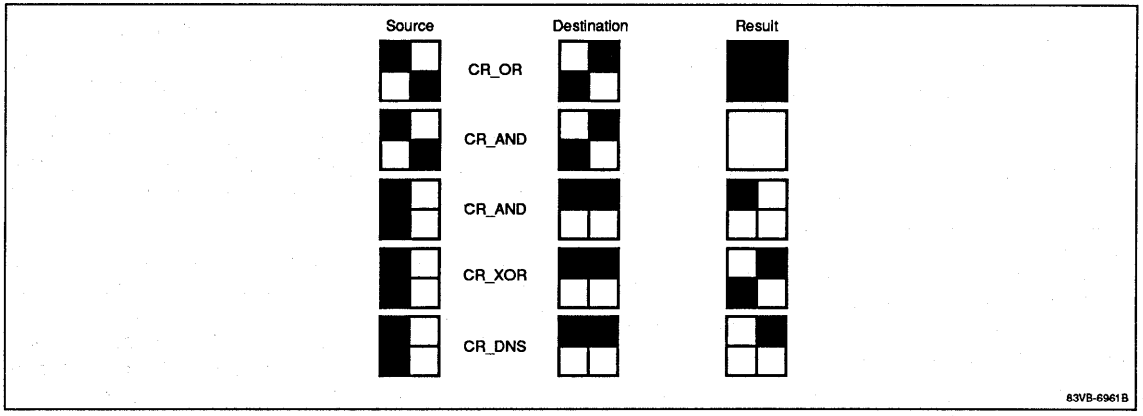

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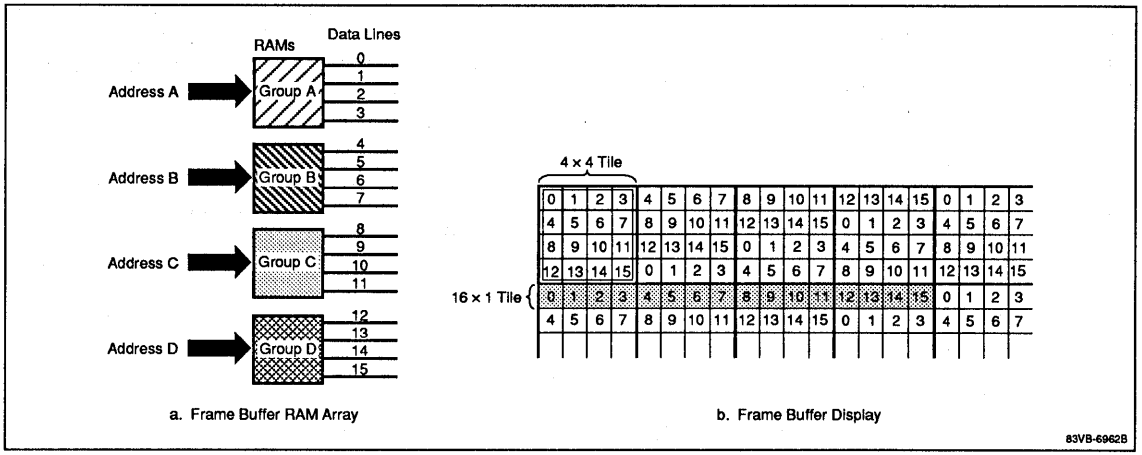
Figure 9. Tile Organization



FRAME BUFFER ARCHITECTURES

Double Buffer Architecture

One of the solutions is to divide the frame buffer into two separate storage arrays, where one is used to refresh the display and the other to update the image (figure 10). When the display controller decides to change the image on the screen, it switches the two buffers, substituting the new image into the refresh buffer and using the old refresh buffer to update a new image, and so forth. One of the disadvantages of this architecture is that it requires twice the amount of memory; however, it is essential to ensure a smooth transition between successive images. Even if the image can be written within one frame cycle, the display must be erased between frames, causing flicker.

Double buffering can be implemented with two methods: either by splitting the available memory in pixel depth and using two buffers with reduced color resolution, or by splitting the *x,y* resolution of the memory and retaining full pixel depth. When the two buffers use entirely separate sets of memory chips, the display processor and the video refresh processor have complete access to their respective memories. If the buffers must share memory chips, little or no access improvement results, but image transition is smoothed.

A 512 x 512 x 32-bit frame buffer can be treated as two 512 x 512 x 16-bit buffers. In some cases, the lost color resolution can be regained in the video output chain. The advantage of the pixel depth-splitting approach is that the system can be used as a single-buffer system for full color applications, and as a double-buffered system with reduced color resolution for applications that may not need full-color capability.

In systems with at least twice as much memory resolution as the desired output resolution, double buffering is accomplished by treating the memory as if it were two or more distinct buffers of the desired size. In some systems, *x,y* memory storage resolution is larger than the maximum displayed resolution, e.g., as in a 1024 x 1024 storage array in which only 512 x 512 can be displayed at any time.

Correctly designed addressing and window circuitry allow the use of different quadrants of the memory as multiple buffers. In a system that doesn't have a separate *z* buffer, an additional advantage is realized: one quadrant of memory that isn't displayed can be used to store *z* values for a *z* buffer hidden surface algorithm. The double-buffer architecture provides a solution to the display processor/frame buffer bandwidth problem, but at the expense of additional cost and complexity. A much more classical solution to this bandwidth problem is found in dual-port architectures. Such an architecture is provided by a dual-port graphics buffer, which consists of a random access port (similar to a typical DRAM) and a serial output port.

Dual-Port Graphics Buffer

The fundamental structure of a frame buffer is that of a dual-port memory in which one port is used to read memory values at high speed for displaying and the other port is used by an update processor to change the display image by changing the memory contents

(figure 11). To update the processor, the frame buffer behaves like all other memory in the system. It responds to each request to read or write a byte, a word, or multiple words as required. The display port is controlled by a video generator, which reads from memory the pixel values that correspond to the raster scanning pattern used on the display. The size and speed of the frame buffer must be chosen to match the properties of the display.

The display processor accesses the dual-port graphics buffer via the random access port, and it performs a data transfer from the random access port to the serial port when the display needs to be refreshed. The serial port consists of a large video shift register. The addressing of the memory is arranged so that a row of the memory chip contains bits that describe adjacent pixels on a scan line. The shift register is loaded at the beginning of the scan line, and then shifted to obtain the values of subsequent pixels. Because the shift register can only operate at 33 MHz, several chips are usually operated in parallel, and a final high-speed video multiplexer produces values at pixel rates.

Figure 10. Double-Buffer Architecture

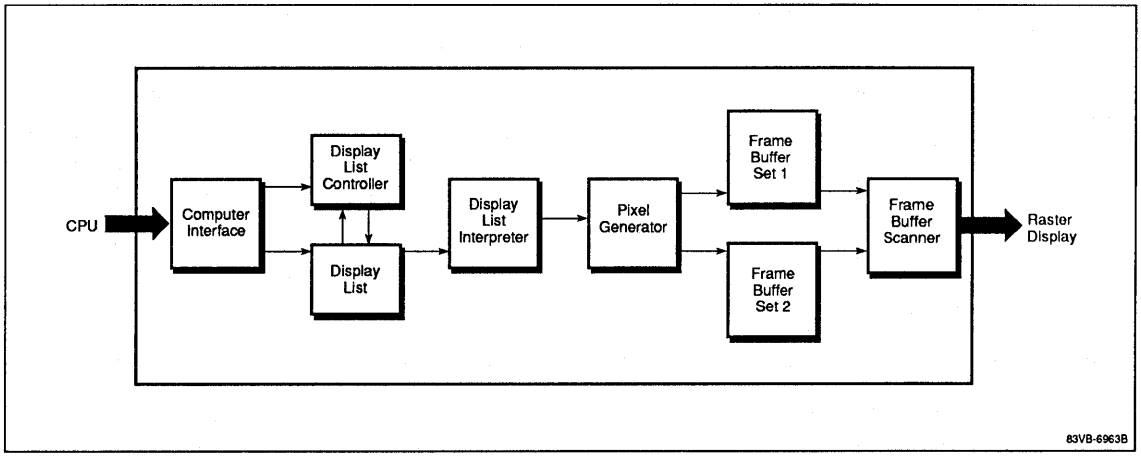
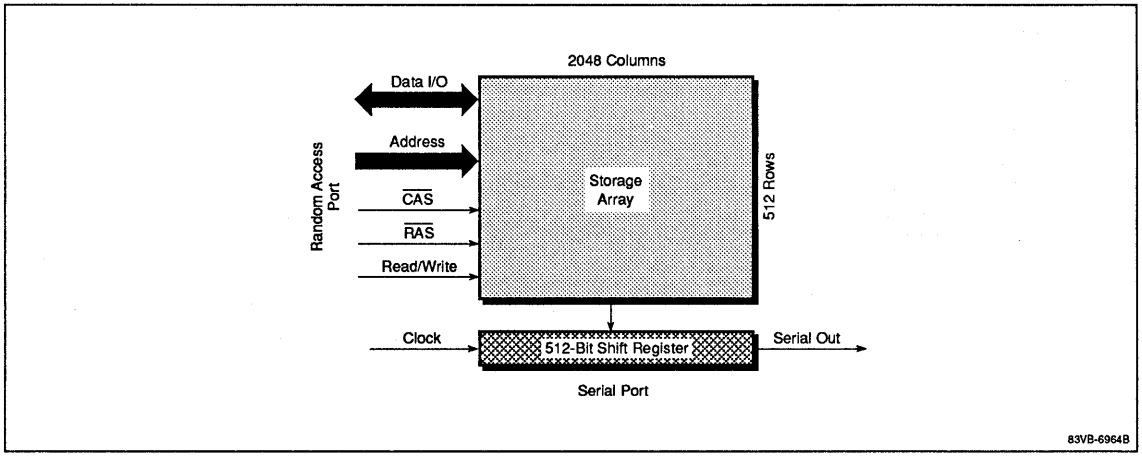


Figure 11. Dual-Port Graphics Buffer Architecture



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The shift register in a dual-port graphics buffer increases the bandwith available relative to a typical RAM chip by a factor of 6 to 8 in a way that directly benefits frame buffer display designs. For display refresh cycles, 512 bits are obtained with a single row access cycle, and therefore almost 100% of the normal row/column accesses can be devoted to the update port. Only infrequently must the update accesses be suspended so that a row address can reload the shift register.

Several system-oriented features were incorporated into the 64K x 4 dual-port graphics buffer architecture, including a mask function that provides the ability to alter some of the pixel values while leaving the remaining pixels unchanged. Current applications often require updating only one bit on a pixel. Conventional x4 memory devices must perform the same operation on all four bits. The system must execute a read cycle, update the desired data bits, and then execute a write cycle or provide an extended read-modify-write cycle.

The dual-port graphics buffer provides a write-per-bit option that can be set as part of a write cycle without any increase in cycle time over a standard read or write cycle (the write-per-bit feature is also being implemented on standard DRAM products). Standard dual-port graphics buffers also are able to load the serial register from the random access port without stopping the serial cycle. This feature is called real-time data transfer. Information can be transferred during mid-scan or during the retrace interval. A single memory device can now contain multiple segments of a scan line. This feature, combined with the ability to define the starting location of the serial port (pointer control) greatly simplifies the control logic required for scrolling and hardware windows.

Some general themes pertaining to the design of all frame buffers, although their implications for each application may differ.

- Organize the memory to provide sufficient bandwidth for both the display and update ports. While it is tempting to skimp, it generally leads to poor performance because the image cannot be changed fast. If the bandwidth for the two ports is equal, then the entire image can be changed in one frame cycle.
- Organize the update port to access the pixel data required. For example, if an application often alters only a single plane of memory at a time, a pixel access architecture is inefficient because each memory access yields all bits of a pixel rather than just the plane needing to be changed.
- Organize the memory so that the spatial organization of the update port accesses those pixels that often need to be changed. The conventional organization, which alters a horizontal group of pixels in one access, is inefficient for writing thin vertical lines in the frame buffer.
- Design the update port in conjunction with the processor that will use it.

Special Features of a Dual-Port Graphics Buffer

As the dual-port graphics buffer market has matured, manufacturers have created products that increased the number of on-chip features (table 4), thereby reducing display processor workload and increasing overall system performance. This trend has continued, as evidenced by designs for contemporary dual-port graphics buffers.

Flash Write Feature. Flash writing uses one of the dual-port graphics buffer's designated special feature pins. In the case of NEC's 256K x 4 μPD42274, pin 22 is defined as FWE for flash write enable. This feature allows the user to erase and/or write to the display in a much faster time than is required using the conventional method, thus enhancing applications that clear/write the entire display screen (figure 12). The flash write feature

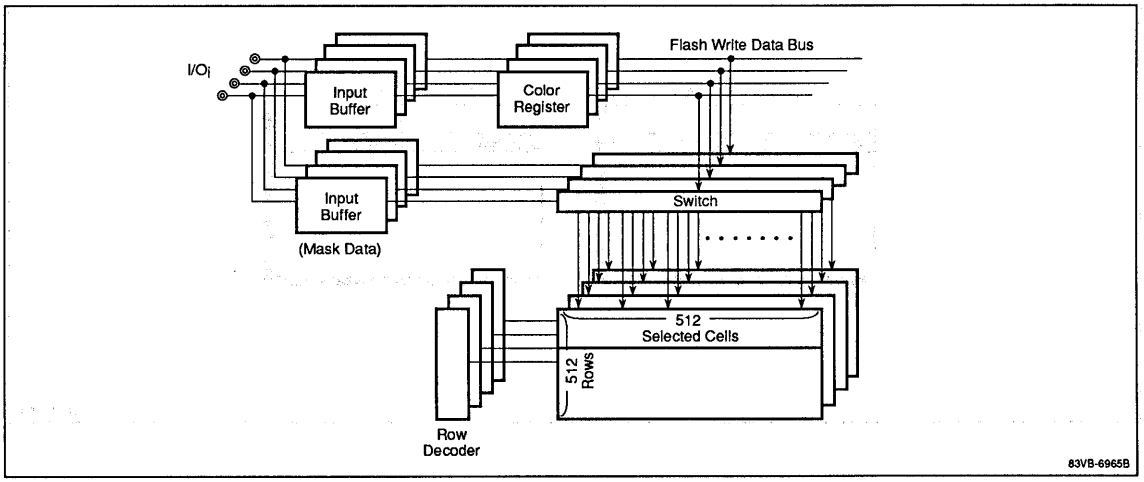
- Allows an entire row of scan line data to be written in one operation
- Is initiated by a special function FWE pin
- Updates screen data more quickly than in conventional write cycles

In a standard dual-port graphics buffer, a unique row and then a unique column are decoded from the address and a single memory cell is written. In this cycle, all the column decoder outputs are enabled, allowing all the bits in the selected row to be written.

Table 4. Feature Comparison

Device Features	μPD42273/ μPD42274	μPD42275	TC524256	TC524256A/258A TC528128A			TMX44C251	MB81C4251/3	HM534252	HM534253	M5M442256
Vendor	NEC	NEC	Toshiba	Toshiba			TI	Fujitsu	Hitachi	Hitachi	Mitsubishi
Configuration	x4	x8	x4	x4		x8	x4	x4	x4	x4	x4
				256A	258A	128A					
Fast-Page	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Flash Write	No/Yes	Yes	No	No	Yes	Yes	No	Yes	No	Yes	Yes
Serial Buffer	Single	Split	Single	Single	Split	Split	Split	Single	Single	Double	Split
Serial Input	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Block Write	No	Yes	No	No	Yes	Yes	Yes	No	No	No	Yes
Raster Operation	No	No	No	No	No	No	No	No	Yes	No	No
600-mil, 28-pin DIP	No	N/A	No	No		No	No	Yes	No	No	No
400-mil, 28-pin ZIP	Yes	N/A	Yes	Yes		N/A	Yes	Yes	Yes	Yes	Yes
400-mil, 28-pin SOJ	Yes	N/A	Yes	Yes		N/A	Yes	No	Yes	Yes	Yes
600-mil, 40-pin DIP	N/A	No	N/A	N/A		Yes	N/A	N/A	N/A	N/A	N/A
400-mil, 40-pin SOJ	N/A	Yes	N/A	N/A		Yes	N/A	N/A	N/A	N/A	N/A

Figure 12. Flash Write Operation



Bounded Flash Write Feature. Although flash writing provides a means for clearing/writing a screen very quickly, it can't be used in the window environment popular in today's graphics market. In conventional flash writing, no option exists to write to only a segment of the row that will be needed in a window environment. The bounded flash write feature can provide this function by allowing the user to specify the segment of the scan line to be accessed (figure 13). Bounded flash writing has not been implemented in dual-port graphics buffer architecture, but it deserves some consideration in today's x-window era.

Block Write Feature. Many frame buffer designs address specific performance requirements, but the problem lies in optimizing the architecture of the display processor with the kinds of features that may be needed for a general-purpose dual-port graphics buffer architecture. For example, the BITBLT operation that many graphics processors use to implement windowing applications is used to transfer blocks of data from a source array to a destination array of equal height and width. Because this operation moves a square block of data, system bus performance can be enhanced if the graphics buffer was able to store data in a block format, rather than in four separate sequential scan lines (figure 14). Unlike bounded flash writing, the block move feature has been implemented in several dual-port graphics buffer architectures.

Persistent Write-Per-Bit Feature. The write-per-bit feature is a standard option of dual-port graphics buffers, but in some applications, system timing considerations prohibit the use of this function because of the additional overhead required to supply the mask data on each write cycle. The persistent write-per-bit feature solves this problem by permitting mask data to be written only once (figure 15).

Extended Fast-Page Cycle. The display processor-to-frame buffer bandwidth is a key issue in determining performance of a graphics system. The trend in dual-port graphics buffers has been to follow standard DRAM evolution, expanding memory capacity with each new generation. In many cases, organization and not capacity determines bandwidth of the frame buffer. Therefore, a wider x8 organization would enhance system bandwidth and reduce the number of dual-port buffers needed in frame buffer design.

Another approach is to provide high-speed access such as the fast-page cycle implemented on the 256K x 4-bit generation of dual-port graphics buffers. Bandwidth requirements of fast-page cycles may be inadequate in some applications. The popularity of RISC architectures has created a demand for synchronous pipeline operation, for which extended fast-page access is being proposed. This feature interlaces the internal accesses of the dual-port graphics buffer and latches the data on-chip so that it can then be accessed synchronously, reducing the page access time from 60 ns to 30 ns. Extended fast-page access means that frame buffer designs will be able to increase bandwidth without increasing the size or cost of the device.

Figure 13. Bounded Flash Write Operation

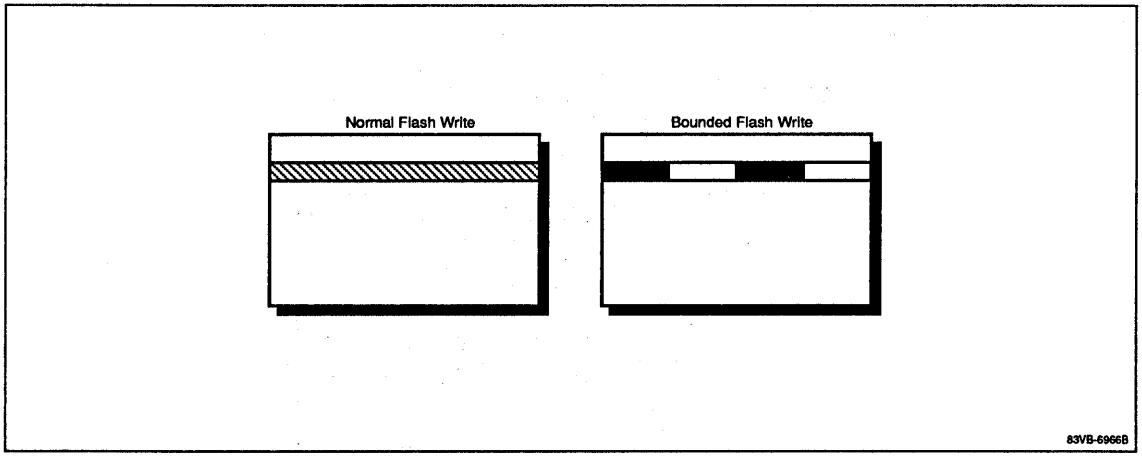


Figure 14. Block Write Feature

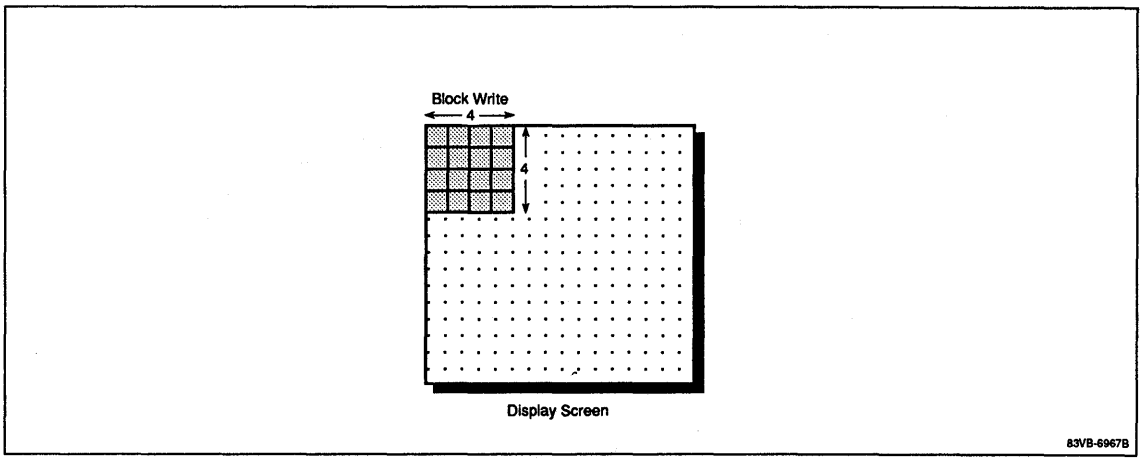
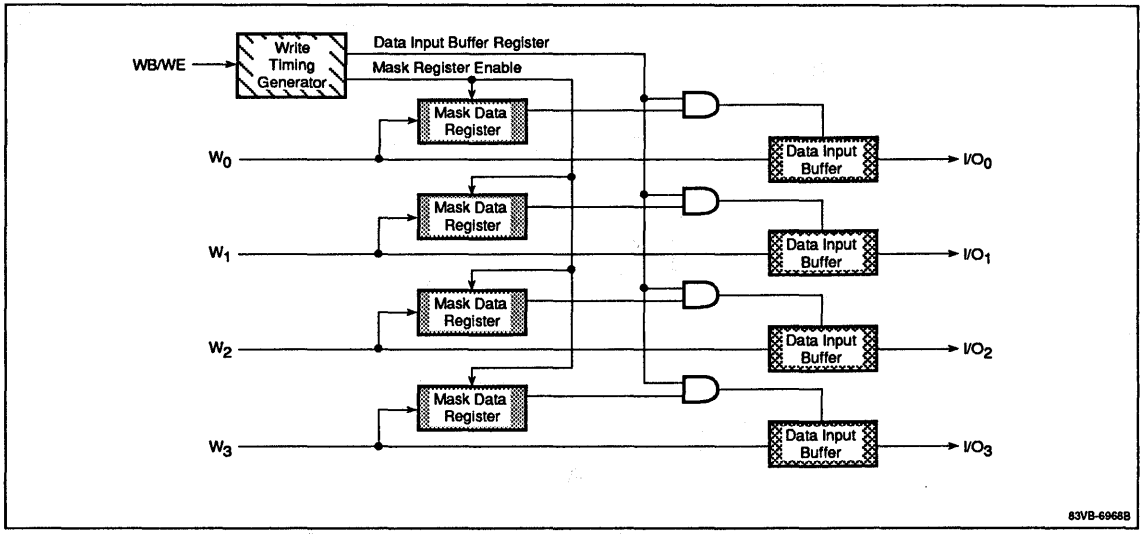


Figure 15. Persistent Write-Per-Bit



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Logic and Arithmetic Functions

The BITBLT operation has been defined as a means of copying an array of equal height and width from a source array to a destination array. Additionally, there are a number of combination rules that define how the source data is combined with the destination data to form the new values. There is also a third form called a pattern array that can be combined with the source toproduce a replicate pattern over the destination. Another name for BITBLT is RASTER-OP (figure 16). This nomenclature is pertinent to dual-port graphics buffers because it has been implemented in devices such as the NEC μPD42232™ and the Hitachi HM53462™ (in which it was first introduced).

μPD42232 is a trademark of NEC Corporation.
HM53462 is a trademark of Hitachi.

Figure 16. RASTER-OP Functions

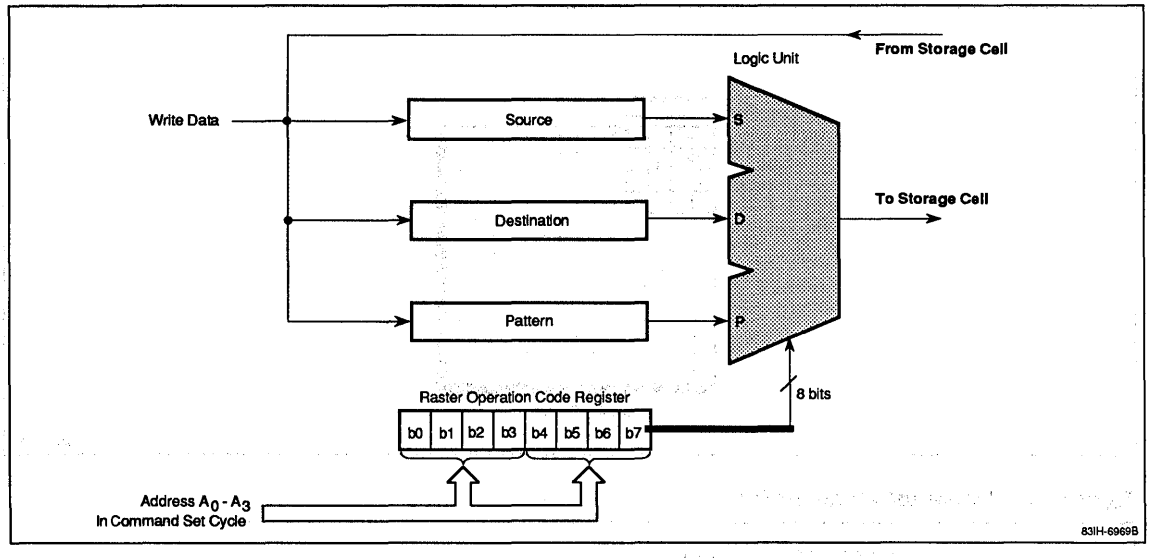
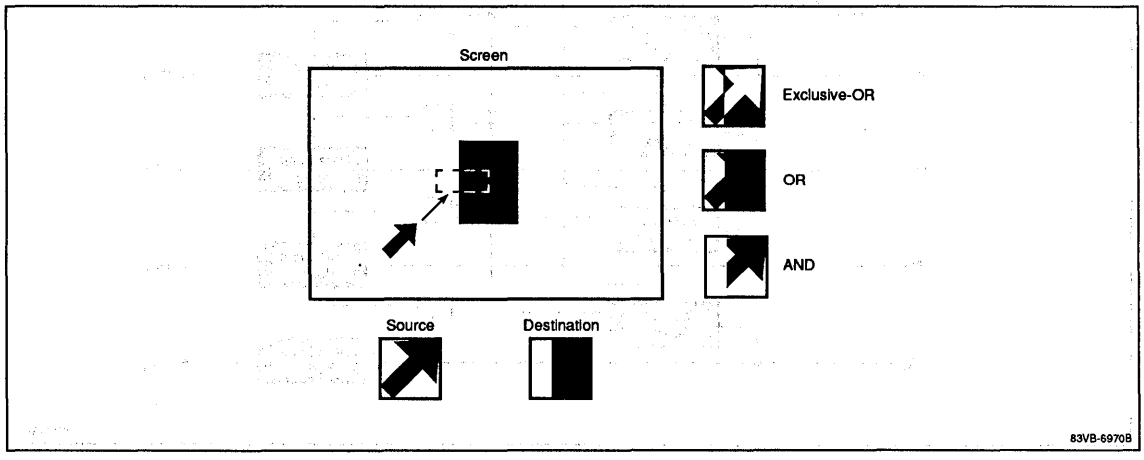


Figure 17. Example of RASTER-OP



The function can be implemented by inserting a logic unit between the input/output buffers and the internal input/output bus amplifier (figure 17). The logic unit is controlled by a 4-bit code that defines one of the 16 combination functions. NEC's μPD42232 approach to on-chip RASTER-OP involves the addition of a third input to the logic unit, a pattern function. This approach is compatible with the classical implementation of BITBLT, but the number of combination functions has been increased from 16 to 256 on the NEC device.Logic functions provided by the RASTER-OP operation are useful in two-dimensional graphics systems, but with the increasing development of three-dimensional systems that require hidden surface removal, three-dimensional polygon filling, etc., there is a requirement for much more powerful computational functions. Several contemporary graphics processors provide a number of pixel processing operations intended to address the requirements of three-dimensional systems.

One example is the pixel-planes graphics engine architecture, which replaces the rasterizer, frame buffer, and video controller of a conventional system. Its main

component is a "smart frame buffer" composed of custom VLSI enhanced memory chips that address the computational problem with a highly parallel processor that mimics a processor per pixel. The memory bandwidth bottleneck is overcome by intimately connecting processing circuitry and memory. Figure 18 shows a block diagram of the arithmetic logic unit, where logical operations are performed by a one-bit address with a multiplier on each of its three inputs. The pixel-planes architecture represents a trend in high-end graphics architectures that optimizes the graphics pipeline primitives by creating a smart frame buffer capable of performing computational functions and using concurrent operations.

Word Alignment in Dual-Port Graphics Buffers

An important issue in plane-organized graphics systems is aligning word boundaries. Although alignment functions exist in contemporary graphics processors, graphics systems designed for the low-end market may not be able to justify the cost of a high-end processor. One solution is to provide a dual-port graphics buffer with both plane and pixel access capabilities. An alternative solution is to include a barrel shifter function (figures 19 and 20). Both approaches are nonstandard but could be considered for an application-specific design that distributes some of the processor's functions to the frame buffer.

Figure 18. Smart Frame Buffer

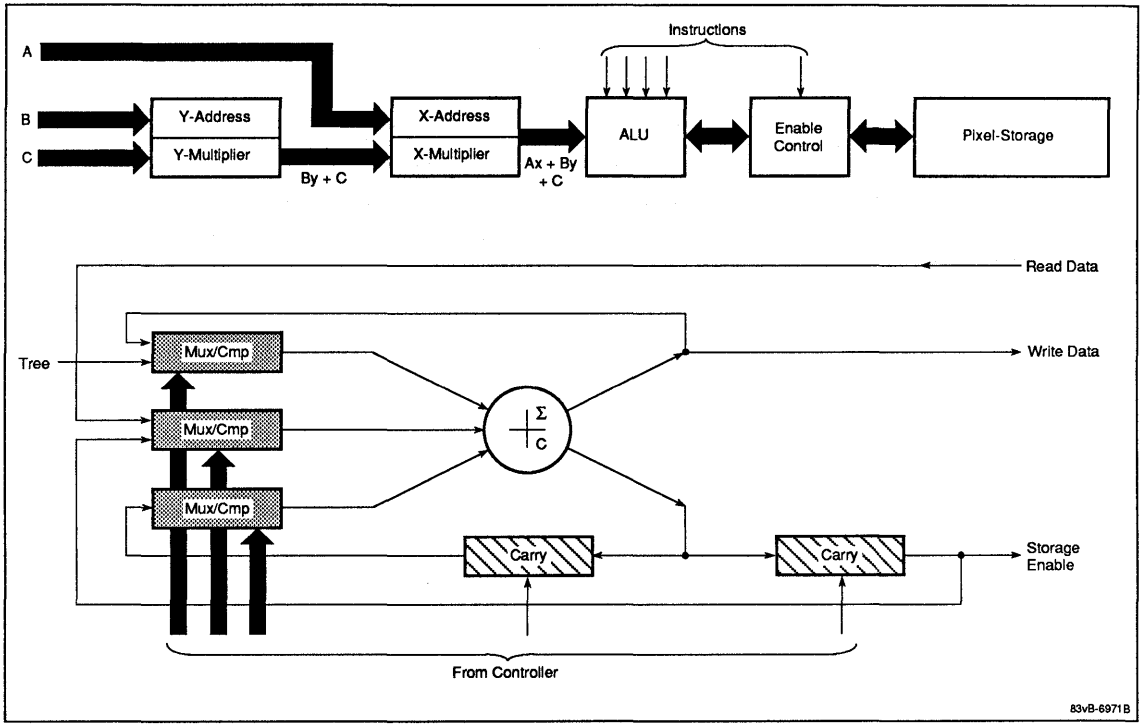


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Figure 19. Chip Addressing to Cross Word Boundaries

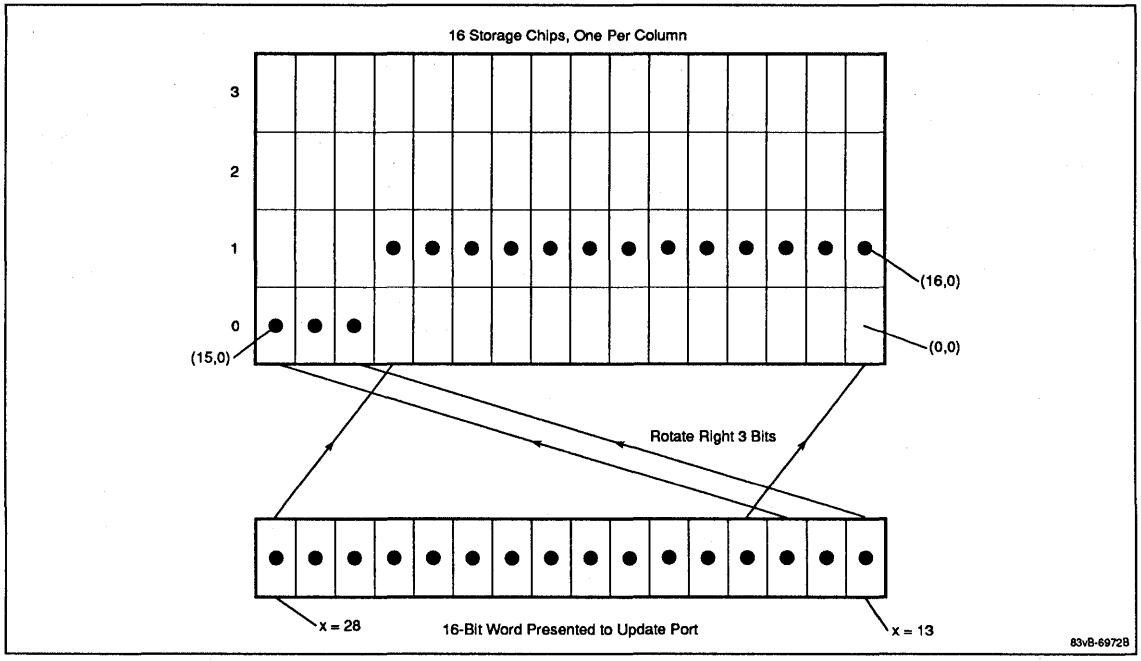
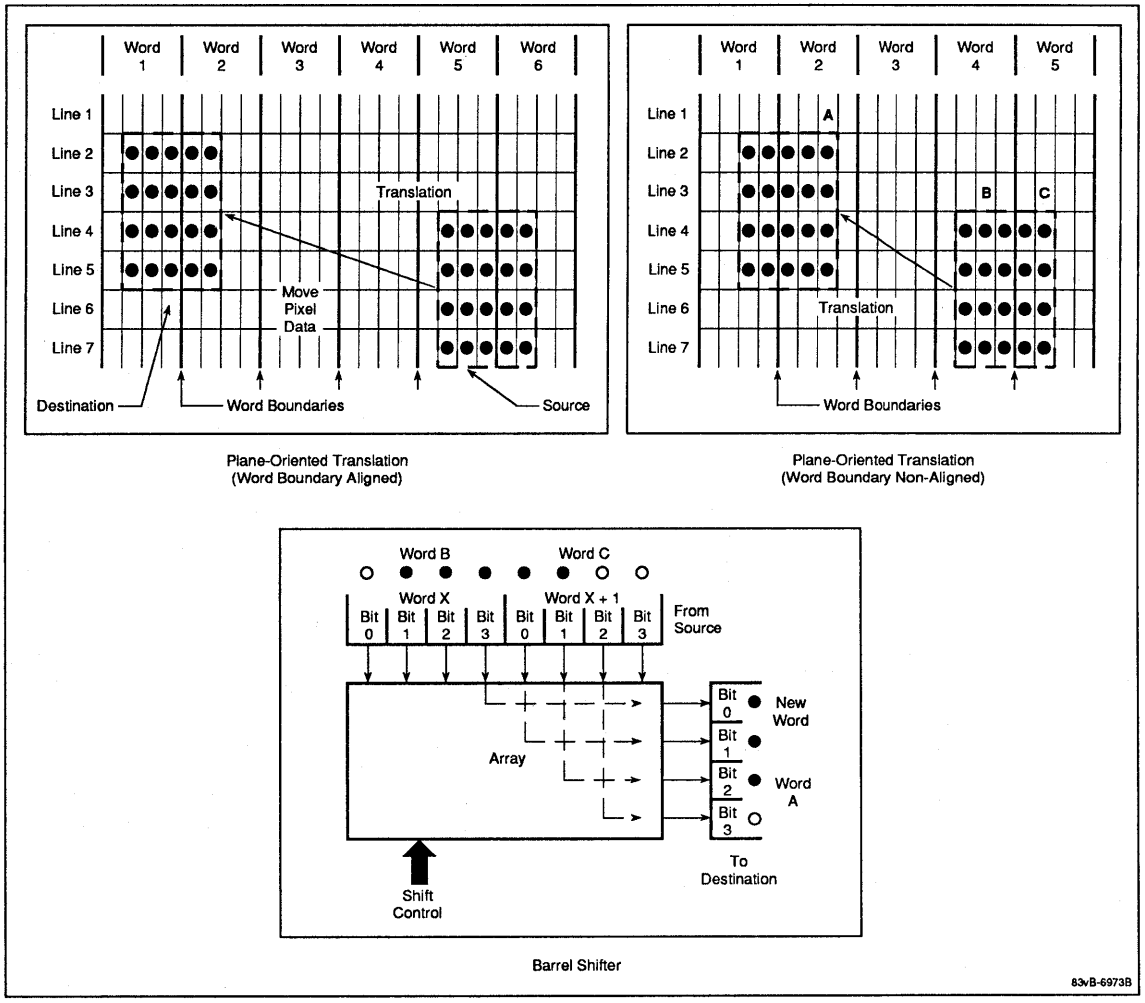


Figure 20. Barrel Shifter Function



Special Serial Port Features

High performance graphics applications require screen refresh rates in the range of 60 to 72 Hz; also full-resolution stereoscopic displays require twice this refresh rate, 120 Hz. In order to be able to accommodate these high rates, a very fast serial access cycle is required. A data transfer cycle to load data from the dual-port graphics buffer into its serial access memory requires use of the random access port. For example, a fast-page cycle must be in progress before a data transfer cycle can occur, which means it would be good to reduce the number of times that serial access memory must be loaded.

Alternatively, if the data from the random access port could be loaded into an idle part of the serial access port, the serial access port would not be interrupted. This could be accomplished with the use of a split-buffer serial port architecture, which separates the serial port into two equal halves, allowing concurrent data transfers from the random access port while the serial port transfers data to the display, thus increasing pixel bandwidth.

Another advantage of using a split-buffer architecture is that tile boundaries can be crossed in real time. For example, a frame buffer organized into 16 x 16 tile can be access by two dual-port graphics buffers. The left

half of the split buffers of devices 1 and 2 (figure 21) is used to fill tile A, and the right halves are used to fill tile B, and so forth. Because the data transfer is done on tile boundary, the unused or off-screen memory in the device is one linear array, allowing the system to use the memory of other functions such as *z* buffers.

Serial Input. Serial input has been offered as a standard feature in a number of 64K x 4 and 256K x 4 dual-port graphics buffers, and can be used in image processing applications as an input port to store serial pixel data. The serial port can also be used to transfer data between two planes while the display is not being updated, bypassing the random access port buffer. Although it wasn't considered an essential feature in the past, developing applications indicate a need for serial input.

When both serial input and output functions exist in a dual-port graphics buffer, the serial port can execute a pseudo-write transfer cycle, which switches the serial port from serial output to serial input with no actual data transfer taking place between the dynamic and static RAMs. This feature is useful in an alternating shift sequence where the dual-port graphics buffer is writing and reading data on the serial bus.

Serial Port Organization. The number of serial input/output pins has a direct relationship on the pixel bandwidth and number of dual-port graphics buffers needed to update the display. A typical system that displays an 8-bit word horizontally on the screen might need a final pixel rate of 120 MHz. If the serial port is organized with a x8 port operating at 30 MHz, NMOS and CMOS devices can be used together with an 8:1 multiplexer for updating the display. The disadvantage of using a wider serial port is larger package size, higher power requirements, and increased noise.

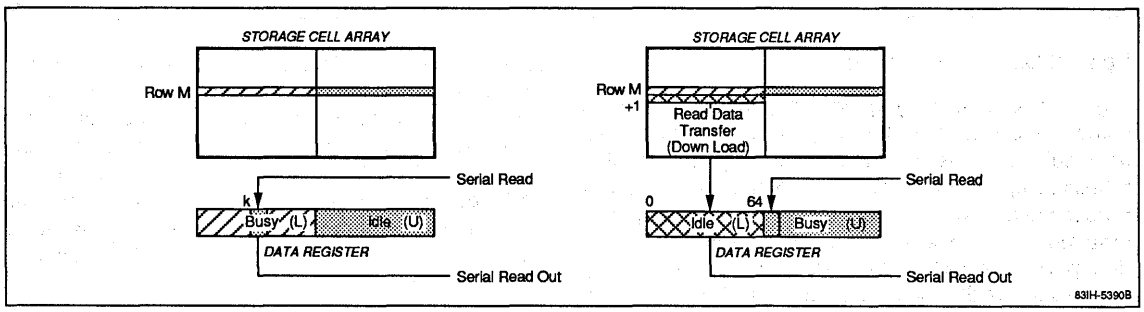
Video Generation

The job of the video generator is to fetch pixel values from the display port, convert them to analog voltages, and pass the results to the display monitor where they will control the intensity of one or more electronic beams. The video generator also creates synchronization signals used by the display monitor to coordinate the beam's sweep across the screen with the arrival of pixel data.

Video Lookup Tables. In addition to providing a digital-to-analog conversion function, the video generation circuit almost always provides a RAM-based lookup table that performs two functions: it allows greater precision in intensity or color values than can be represented in the frame buffer directly, and it allows certain kinds of dynamic displays because the table can be changed more rapidly than the contents of the entire frame buffer.

A pixel's color is determined by the bits stored at the pixel's address in the frame buffer. The pixel's contents don't drive the digital-to-analog converter directly; they are pointers to colors in a RAM lookup table. The width of the lookup table in a triple digital-to-analog converter formation is three times the resolution of the devices. The first third of the lookup table entry controls the red digital-to-analog converter, the second controls the blue, and the third controls the green. The number of bits in memory controls the total palette size. For example, three 6-bit digital-to-analog converters will result in an 18-bit wide lookup table, allowing a total palette size of 262,144 colors.

Figure 21. Split Buffer Configuration



Color resolution is determined by the number of bits per pixel. Eight bits per pixel gives a markedly better picture than four bits per pixel; however, 24 bits per pixel provides true color. More than 256 colors can be displayed on the screen at once by changing the color associated with each address in the lookup table. The colors can be changed as often as once every scan line. This technique is called "pseudocolor."

Lookup tables may have separate registers for generating overlays, which provide a means of generating an image separate from the frame buffer. The overlay registers are controlled by the system processor, and allow the system software to control the system graphics elements independently from the application software graphics. System software displays basic, relatively unchanging graphics elements such as cursors, screen frames, and system messages. Application software manipulates a variety of changing graphical information. By overlaying one or more separate graphics planes displaying system information, the time-consuming task of updating the frame buffer can be avoided (figure 22).

Digital-To-Analog Converters. The digital-to-analog conversion portion of the video generation circuit converts the digital output of the lookup table into analog circuits that are used to drive the display monitor. These converters are specified regarding their organization (e.g., triple 6-bit, single 8-bit, etc.) and the speed at which they can operate. Figure 23 shows the relationship between screen resolution and digital-to-analog converter bandwidth. A number of manufacturers produce both triple and single converters, up to a speed of 360 MHz. If greater speed is required, a discrete bipolar circuit needs to be designed.

References

Foley, J. D., and Van Dam, A., *Fundamentals of Interactive Computer Graphics,* Addison-Wesley.

Poulton, J., Fuchs H., Austin J. D., et al, "Pixel-Lanes: Building a VLSI-Based Graphics System," Proceedings of Chapel Hill Conference on VLSI, 1985.

Salmon, R., and Slater, M., *Computer Graphics-Systems and Concepts,* Addison-Wesley, 1987.

Sproull, R. F., "Frame-Buffer Display Architectures," Annual Review of Computer Science, 1986.

Whitton, M. C., "Memory Design for Raster Graphics Displays," IEEE Computer Graphics and Applications, Volume 4, Number 3, March 1984, pp 48-65.

Figure 22. Overlaying of One or More Planes

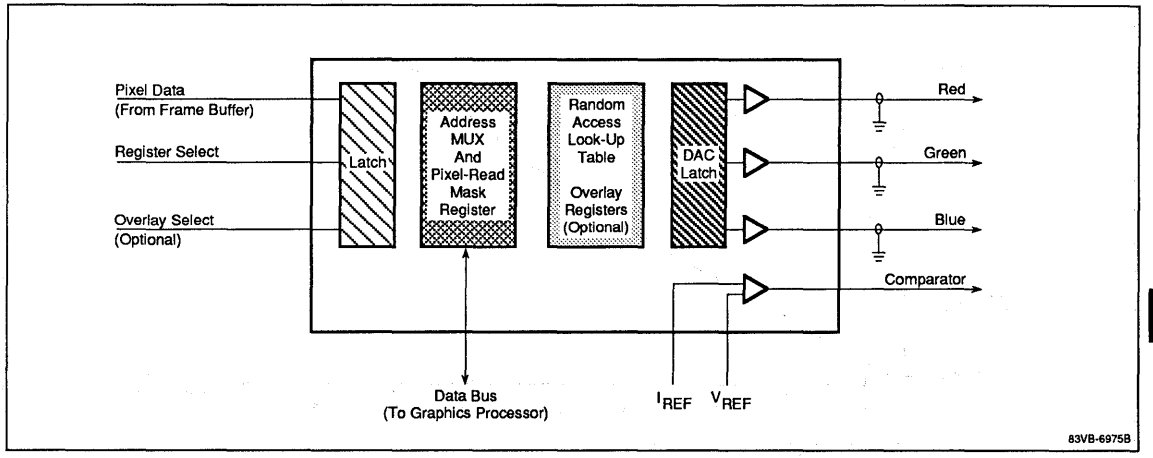


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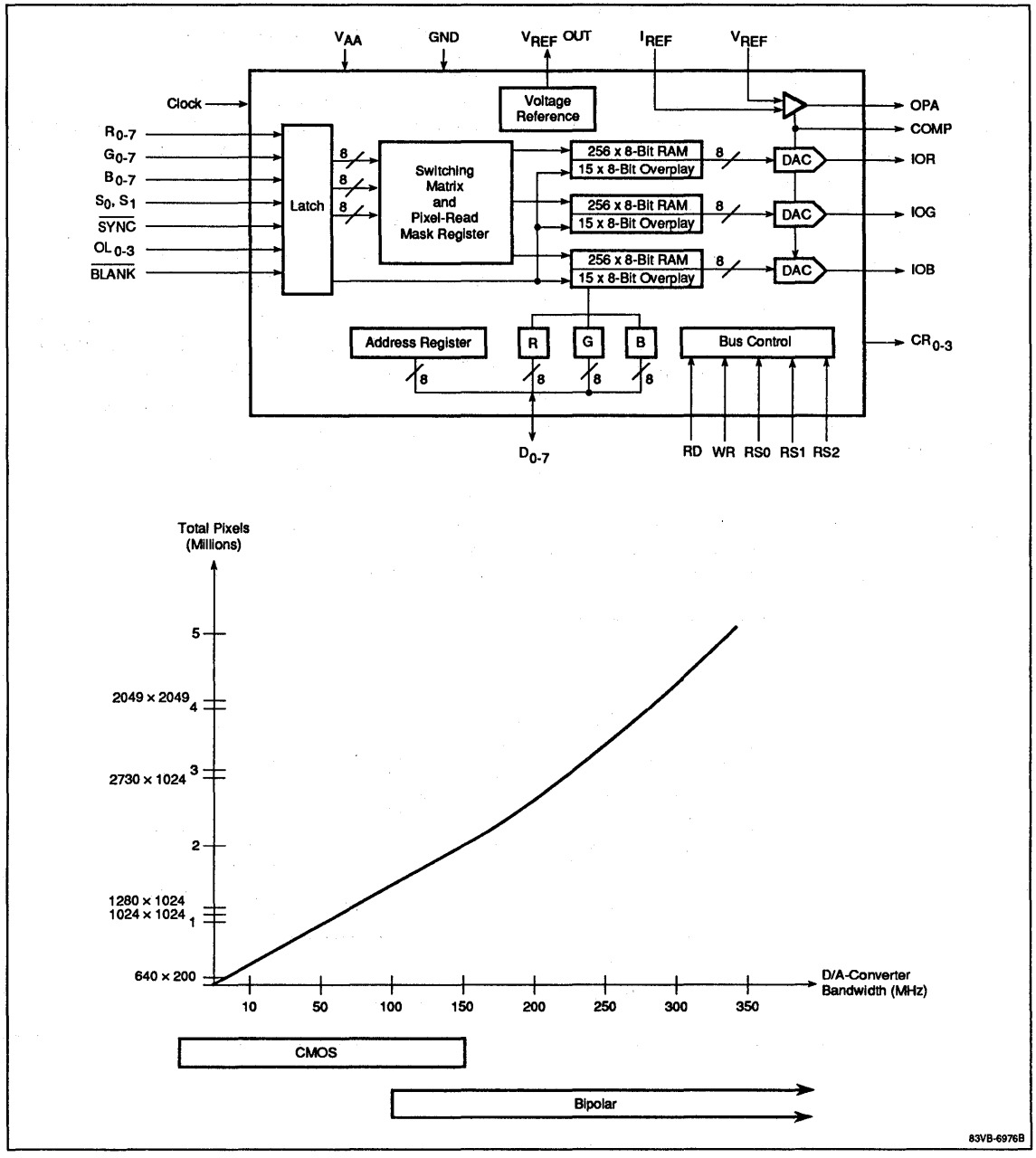
Figure 23. Relationship Between Screen Resolution and Bandwidth of the Digital-to-Analog Converter



Introduction

Computer-generated images that rival color photography in all of its nuances of color, shading, reflectance and translucency is in demand by a growing number of users. This application note will discuss the algorithms able to generate these effects, which have been integrated into a variety of systems with impressive results.

Three-Dimensional Graphics System

In a three-dimensional system, the object rendered is described as a mathematical model that holds primitives such as lines, polylines, and polygons in a display list. Traversing the display list produces a sequence of data in world coordinates. Often this data represents polygon vertices, but it can also represent control points for parametric surfaces and other data that must be converted to a polygonal approximation of the surface. Polygons expressed in three-dimensional world coordinates transform geometrically into a form suitable for display on a two-dimensional raster device. Transformations include three-dimensional to two-dimensional projection, translation, scaling, rotation, perspective projection, and clipping. The result is a series of polygon vertices supplied in coordinates for a specific CRT.

The polygon vertices and their associated color data are interpolated to determine the pixels to be illuminated and the color to be displayed, while depth (*z* axis) information is interpolated to determine which polygons are obscured from the observer's view. Color values are written to the frame buffer and depth values to the *z* buffer which, with its associated hardware, supplies hidden surface removal. Finally, each pixel from the frame buffer is sequenced in the line as required by the CRT and converted to an analog signal.

Although a basic three-dimensional system can render a realistic image, special functions are required to produce subtleties of color, shading, shape and translucency. These functions must be able to model the behavior of light with different levels of complexity, provide methods for creating realistic surface textures, compensate for the limitations of the display technology, and provide techniques for rendering natural effects such as terrain and clouds.

Two- and Three-Dimensional Image Processing

Three-dimensional graphics is an order of magnitude more complex than two-dimensional graphics, and while a detailed description of its specifics is beyond the scope of this paper, some aspects pertain to this discusssion.

The viewing pipeline in two-dimensional graphics involves transformations from two-dimensional coordinates, world coordinates, normalized device coordinates, and device coordinates. Moreover, the objects may be transformed at one of the stages by some combination of translation, scaling, and rotation.

In three-dimensional graphics, the pipeline is more complex because there is a projection stage, where the three-dimensional world coordinates in which the scene is described are projected onto a two-dimensional projection plane. Conceptually, objects in the three-dimensional world are clipped against the three-dimensional view volume and then projected. A view volume is specified in world coordinates, in a projection onto the projection plane, and in a viewport on the surface. The contents of the window, which is itself the projection of the view volume onto the projection plane, are then mapped into the viewport for display. Figure 1 shows this process, which is the model used in numerous three-dimensional graphics subroutine packages. As with two-dimensional viewing, a variety of models can be used for actual implementation of the viewing process.

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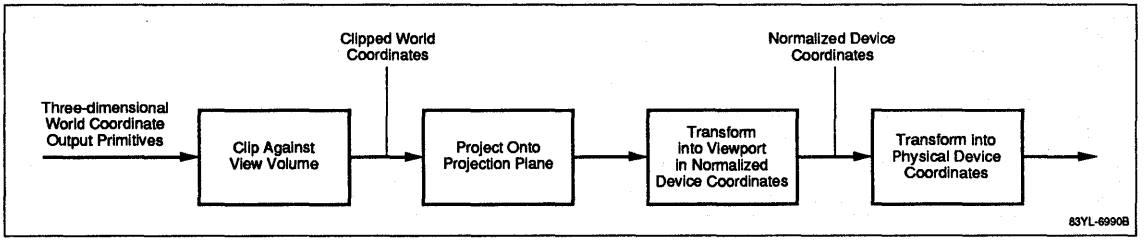
Figure 1. Basic Three-Dimensional Pipeline

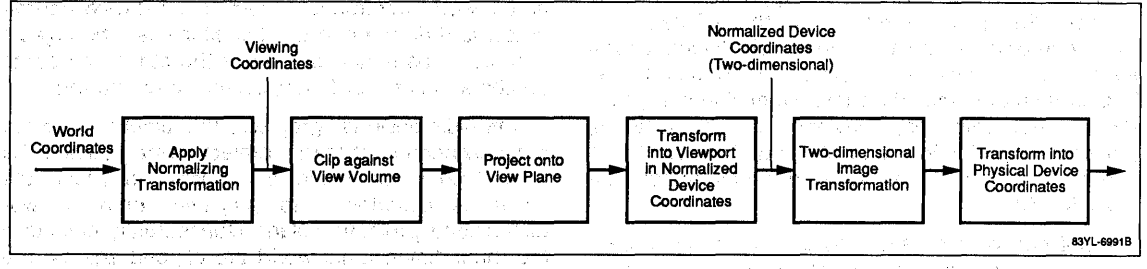


Given the specification of a view volume and a projection, there is a need to understand how the clipping actually is done and how the projection is applied. It is possible to clip lines against the view volume by first calculating their intersection with each of the six planes defining the view volume. Lines remaining after the clipping process would be projected onto the view plane by simultaneously calculating the intersection of the projectors through their end points with the view plane. The coordinates would then be transformed from three- into two-dimensional world coordinates.

To be able to include three-dimensional viewing operations in a standard graphics package, two sets of capabilities must be added: output primitives in three-dimensional coordinates, and specifications of planar geometric projections. Output primitives in three-dimensional world coordinates are straightforward extensions from the two-dimensional primitives. A third parameter, the *z* coordinate, is added to the procedure call. The perspective projections in a graphics package allow viewing from a number of perspectives, including from the center of a projection, from a view plane, from a window on the view plane, and from a viewport on the view surface.

The extra complexity introduced with three-dimensional viewing is caused by the fact that the display devices are only two-dimensional. The solution to the mismatch between three-dimensional objects and two-dimensional displays is solved by introducing projections, which transform three-dimensional objects onto a two-dimensional projection plane (figure 2). The large number of calculations required for this process, repeated for many lines, calls for considerable computing.

Figure 2. Three-Dimensional Viewing Process Extended to Include Two-Dimensional Image Transformations



Three-Dimensional Projections

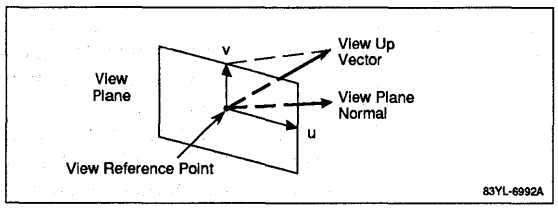
Table 1 identifies and defines the specifications for a three-dimensional projection. Figures 3, 4 and 5 are corresponding examples.

Table 1. Parameters for a Three-Dimensional Projection

Parameter	Description
uv Coordinate System	System by which a window is defined
u Axis Direction	The direction of *u*, *v* and the view plane normal when positioned to form a left-hand coordinate system
v Axis Direction	Coincident with the projection of the view up vector parallel to the view plane normal onto the view plane
Center of Projection	Helps define the view volume and is specified in world coordinates relative to the view reference point
View Plane	Plane on which the scene is to be projected
View Plane Distance	Distance of the view reference point to the view point along the view plane normal
View Plane Normal	Is used to specify the view plane
View Reference Point	Source of *u* axis and *v* axis in the *uv* coordinate system
View Up Vector	Determines the *v* axis direction; its projection parallel to the view plane normal is coincident with the *v* axis
View Volume	Bounds the portion of the world that will be clipped and projected, and is defined in part by the window

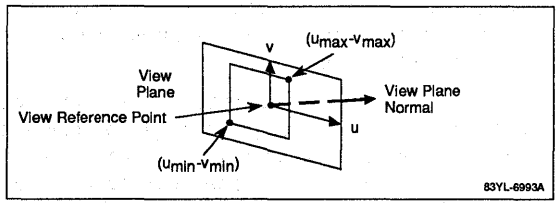
Figure 3 illustrates how the *v*-axis direction on the view plane is determined. The *v*-axis direction coincides with the projection of the view up vector parallel to the view plane normal.

Figure 3. uv System in the View Plane



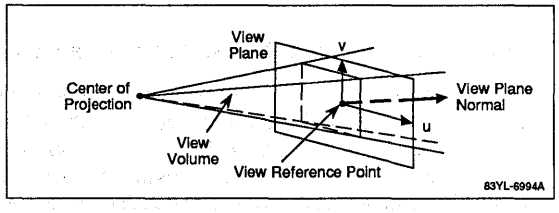
The view reference point, view up vector, and view plane normal are specified in the left-hand world coordinate system. With the *uv* system defined on the view plane, it is possible to specify the window's minimum and maximum *u* and *v* values, as shown in figure 4. Notice that the window need not be symmetrical about the view reference point.

Figure 4. Window in uv Coordinates



For perspective projections, the center of projection also helps to define the view volume. The center of projection is specified in world coordinates relative to the view reference point. The view volume is a semi-infinite pyramid that slides through the window, with its apex at the center of projection. Figure 5 shows the perspective projection view volumes. Positions behind the center of projection are not included in the view volume and will not be projected.

Figure 5. Semi-Infinite Pyramid View Volume for Perspective Projection



Anti-Aliasing

No matter how sophisticated the object model, it cannot overcome the consequences of sampling a continuous scene with a finite number of elements. Such sampling is an inevitable outcome of the very raster graphics technology that has made shaded image generation possible. A raster display consists of a rectangular array of spots, each of which can be controlled in intensity by the CPU. The actual image is a continuous intensity function of *x* and *y* on the screen; the pixels are regularly spaced samples of this continuous function. In any sampled data system, problems arise if the resolution of the continuous function is the same as or smaller than the spacing between samples. This phenomenon, known as aliasing, is visible on CRT screens as jagged lines, or jaggies. It is particularly apparent on lines and curves angled close to the horizontal and vertical axes, and often appears in images displayed on screens with low to moderate resolution (figures 6 and 7).

Figure 6. Vertical Aliasing

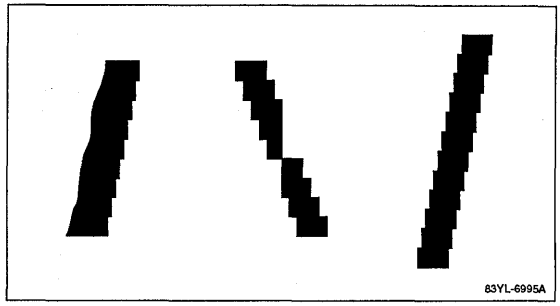
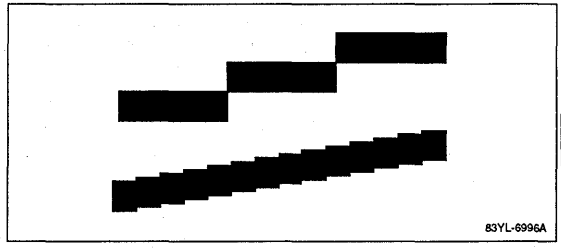


Figure 7. Horizontal Aliasing



Generally, aliasing can be found in at least three types of graphics: (1) in jagged edges of straight lines and polygon boundaries, (2) in objects smaller than pixel size or in objects containing very thin lines or polygons, or (3) in complex scenes containing a lot of fine detail. Unless special measures are taken, the fine detail is either totally lost or distorted beyond recognition.

The solution is to eliminate high frequency information before sampling the picture. Visually this means blurring the picture. Mathematically it means the intensity of a picture should be more than just the point to which it corresponds in the continuous picture; it should be some weighted average of the intensities surrounding the point. The anti-aliasing process requires the weighting function at each pixel to be multiplied by the ideal intensity function, the results integrated, and the result used as the displayed intensity. Perhaps the most obvious anti-aliasing technique is to sample the image at a resolution higher than the one used for display, and average down to the true pixel level. Elementary statistical theory shows that the average values contain more information about the true image than if the sampling had been performed at display resolution size.

Aliasing occurs especially when the intensities in the scene change sharply within a region, for it is in precisely such regions that the sampling rate is not high enough to capture the changes. The idea of filtering is directly based on the idea of a pixel covering a finite area of the scene. A filter applied to the scene definition has the effect of spreading, theoretically, the influence of the scene intensities to all pixels covering the scene. In this way, every part of every object makes some contribution to each of the pixel intensities of the final image.

Visibility

A three-dimensional scene is usually defined within a computer as a collection of objects, each of which may be described as a series of points and lines, or possibly as a set of polygons. Each of these by itself is easy to display. Using the transformation, perspective, and clipping algorithms described earlier, a system can plot these individual pieces on the display. However, in cases where there are a large number of objects, some may be positioned so as to obscure the eye point's view of others. This is referred to as the *hidden line* or *hidden surface* problem, depending on whether the eventual end product is a line drawing or a shaded rendering of the scene.

Solutions to this problem have typically required large amounts of computing time. Compared to the work involved in computing transformation, perspective and clipping algorithms, the hidden surface calculation is usually the dominant cost in such a program. The former calculations depend only on an individual object, not on its relationship to the other objects in a scene. Thus the amount of work is roughly proportional to the number of objects within the scene. However, hidden surface removal requires that each object be compared to every other object.

The various surfaces of an object to be shown in hidden surface or hidden line form must be sorted to find which ones are visible at various places on the screen. Surfaces may be sorted by lateral position in the picture (x,y), by depth (z), or by other criteria. To reduce the amount of sorting, each hidden surface algorithm must use some property of coherence of the objects represented. A picture is coherent not only because it consists of flat faces, but also because those faces relate to each other to form objects. A number of hidden surface algorithms have been developed by systematically looking for additional kinds of coherence and by sorting orders and types.

Hidden line or hidden surface removal algorithms have been separated into three categories. First, there are the algorithms operating in object space independent of the type of device used, whose different steps operate directly on the vertices of the face. The object space of an image is the set of primitives such as lines, polygons and spheres that compose the scene to be depicted. The object space methods attempt to solve the problem geometrically in the three-dimensional space of the scene definition.

The second category of algorithm assumes that the number of points composing the projection plane is finite and generally coincides with the raster display resolution. Image space of a scene, i. e., the set of raster elements (pixels) of the display, contains a fixed number of elements equaling the resolution of the display. Image space algorithms are specifically designed for modern raster graphics image generation and are more popular and widely used than the object space algorithms.

The last category, the so-called "list priority" algorithms, are generally characterized by a sorting step in object space and a display in image space. The simplest and fastest hidden surface algorithm is known as the z buffer algorithm. Other examples are the polygon scan conversion algorithm and the divide and conquer algorithm.

Z Buffer Algorithm and Hidden Surface Removal

Hidden surface removal is possible with an image space algorithm called the z buffer algorithm. Of all the complex algorithms addressing hidden line and surface removal, none are as straightforward as this one because it maintains color as well as depth (z) information at each pixel. A refresh buffer stores intensity

values, and the *z* buffer array stores depth values corresponding to the pixels currently set.

The *z* buffer must have the same dimensions as the display frame buffer. All locations in the *z* buffer are initialized to the value perceived by the viewer to be the farthest behind the screen, while the corresponding display pixels are set to the required background color. As each polygon is rasterized, the *z* values for the resulting pixels are compared individually with the previously stored *z* values. The new *z* value is written to the *z* buffer, and the new associated color is written to the frame buffer. If the new *z* value is larger (i.e., farther away), then neither buffer is modified.

The obvious advantage of this algorithm is that it is computationally simple, and its performance is independent of the complexity of the scene in terms of visibility. Its running time is proportional to the number of polygons to be processed, and not to the relationship between the polygons. A disadvantage of the method is that it requires a large amount of memory to maintain the *z* buffer. For example, for a 512 by 512 display, the *z* buffer size is a megabyte of memory if the *z* value precision of 16 to 20 bits would suffice. In any case, the relatively low cost of memory allows the realistic marketing of fast access *z* buffer hardware memory boards, which is perhaps the ideal solution.

Scan Line and Area Subdivision Algorithms

Scan line algorithms operate in image space to create an image one scan line at a time. This approach is an extension of the polygon scan conversion algorithm and thus uses scan line coherence and edge coherence. The difference between the two methods is that all the polygons that define an object are involved. The algorithm performs a *y* sort, and then an *x* sort, and finally a *z* depth search to establish the visible face. In the scan line method, the dimensions are first reduced to two at the intersection of the plane through the scan line, parallel to where the *z* axis intersects the scene, and then reduced to one by considering only the line segments on the plane with minimum *z* values. A *z* buffer based on polyhedral surfaces also makes use of depth coherence to improve speed of computation, whereas the scan line method is based on edge and scan line coherence.

Another method, the area subdivision or divide and conquer algorithm departs from strategies used in other algorithms in that it is based on area coherence and solves the general sorting problem by attempting to avoid it altogether. An area of the projection plane image is examined, and if it is easy to decide which polygon or polygons are visible in the area, the appropriate ones are displayed. Otherwise the area is subdivided into smaller areas and the decision logic is recursively applied to each of the smaller areas. As the areas become smaller, fewer and fewer polygons will overlap, and ultimately a decision will be possible.

This algorithm clearly takes an image space approach by exploiting area coherence, i.e., the tendency for at least the small areas of an image to be contained in a single polygon at most. Area coherence means that pixels close together are likely to correspond to the same object and have a similar color, which is the underlying assumption of the algorithm. This algorithm generally performs less efficiently than the scan line method, because it involves more work to sort things out when projections of polygons overlap.

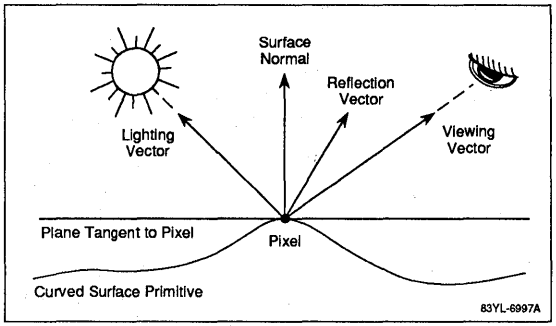
Shading

After hidden surfaces have been removed, the next step in creating a realistic image is to shade the visible surfaces, taking into account the light source, surface characteristics, and positions and orientations of the surfaces and sources. Graphics system designers have been developing lighting and shading models for rendering graphics images at different levels of realism. This involves some understanding of the fundamental properties of the humam vision system. Unlike a photograph of a real world scene, a computer-generated shaded picture is made from a numerical model stored in the computer as an objective model. The goal of the shading model is to provide realistic images of surfaces for which the illumination of a surface depends on its orientation. If it is normal to the incident light rays, the surface is brightly illuminated. The more oblique the surface is to the light rays, the less the illumination. This variation in illumination is a powerful cue to the three-dimensional structure of an object. It would be a waste of modern day computer graphics resources if color-generation techniques were not used to their full capacity. Shading is one of these techniques.

Light Models

In 1975, Bui-Tuong Phong proposed a light model for specular reflection that has since been termed *Phong shading*. This model specified how light reflects from glossy surfaces such as billiard balls, apples, china, and as an extreme, mirrors. Before this model, light was modeled on how it reflected from a perfectly diffused surface, i.e., one that reflects light equally in all directions (figure 8).

Figure 8. Basic Lighting Model for Shading



When planar polygons are used to approximate curved surfaces, greater realism can be achieved by an interpolation scheme introduced by Gouraud. This scheme is called *Gouraud smooth shading*, or *intensity-interpolation shading*. In flat shading, a single intensity value for shading the entire polygon face is calculated, a single surface-normal vector is defined for each represented polygon, and each polygon is shaded with a single color. This is a reasonable approach to shading flat surfaces where the intensity of the light reflected from the surface is held constant over the entire surface.

Gouraud shading provides smooth shading through a linear interpolation technique in which surface-normal vectors are computed at the vertices or corners of each face of a polyhedron. First, surface normals are calculated. Subsequently, vertex normals are computed by averaging the surface normals of all the polygon faces common to the vertex. Each of these vertex normals are used to compute a vertex shade, and then the shade inside the particular polygon face is interpolated from the vertex shades. Each polygon is shaded along each edge and then between edges along each scan line.

Phong shading is a complex algorithm that computes the intensity value of each pixel of a polygon face according to how that point is oriented to the light source(s). Phong's was the first shading model to achieve realistic highlights using interpolation of surface normals and an approximation of specular reflection. The Phong shading model entails interpolated surface-normal vectors across the polygon face—as opposed to Gouraud shading—and using the interpolated surface normal to calculate the intensity values for each pixel on the polygon surface. The intensity contribution for each light is modeled as the sum of diffuse and specular components. Because the Phong technique requires extensive computer power to execute the complex calculations needed to shade each pixel of an object's surface, it is usually performed only on supercomputers or superminicomputers. Phong and Gouraud shading models also support the full range of lighting controls, including multiple, colored point, spot and directional light sources. The special advantage of these schemes is that they fit well with scan line algorithms for filling polygons.

The Phong model yields a surface with a specific normal based solely on the curvature of the surface, which causes a shiny, plastic look. To make this surface appear more realistic, a textured surface must be mapped over the first surface. This technique is called procedural textured mapping and provides a means of defining constant, matte, metal and plastic surfaces.

Ray Casting and Ray Tracing

Ray tracing algorithms simulate the interaction of light with the environment, simply determining such optical effects as reflection, refraction, and shadowing. Ray tracing is a computer graphics technique in which the path of all the individual light rays contributing to the image are traced explicitly. These techniques are direct and somewhat brute force methods for solving the visibility problem. Nevertheless, ray tracing algorithms have produced some of the most spectacular results in graphics images. Many visual and lighting effects such as refraction and reflection, motion blur, depth-of-field, penumbrae, and nonuniform interradiation can be modeled with ray tracing. Despite its simplicity and robustness, ray tracing is seldom used in practical applications because of its high computational requirements.

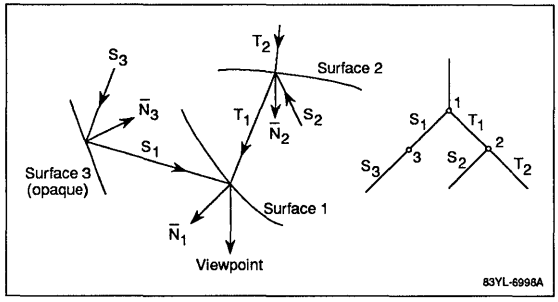
The idea of ray casting is a very simple one: for each pixel, trace a ray from the eye position (in image space) through the pixel and find the intersections with all the objects in the scene. The intersection having the smallest z value determines the color of the pixel. Ray tracing is more complex, because once the first intersection is found, the ray is reflected off the object surface and traced back farther—and so on recursively—until it passes out of the scene or is traced to one of the original light sources. Similarly, if the surface is transparent, then an additional ray is refracted through the surface and traced. In this way, a number of features that are extremely difficult to implement in other methods can be easily introduced into the rendering. Problems with visibility and transparency, as well as with shadows and the reflection of objects on each other, can be easily solved.

The fundamental idea is to trace light rays and to determine which one ends up at the view point. Unfortunately, an infinite number of rays emanate from each

point light source, and most of them never reach the view point. Thus, the tracing starts at the view point and traces rays backward through each pixel to their origin. A ray of light striking the surface of an object breaks into three parts: diffusely reflected light, specularly reflected light, and transmitted light. Similarly, a ray of light leaving the surface of an object is in general the sum of contributions of the three sources. This means that each time a ray leaves an object, up to three new rays should be traced.

Figure 9 shows the tree grown in the process of tracing a particular ray backward. S_1 is the light ray that comes into surface 1 at such an angle that it is specularly reflected and leaves as part of the outgoing ray. Similarly, T_1 is the light ray incident on surface 1 such that it is transmitted and leaves as part of the outgoing ray. Each node of the tree corresponds to a surface. After the tree is completely grown, the intensities at each leaf node are computed and then used to compute the intensity at the parent node, until the root node is reached.

Figure 9. Tree Grown From Tracing a Single Ray to Viewer



An infinite number of rays could be traced backward, but only those rays passing through the view point and the corner of the pixels are actually traced. T_1's permit anti-aliasing to be performed, because the intensities can be averaged to calculate the intensity of the pixel. If the four rays through the corners of a pixel subtend a volume in space that contains a lot of fine detail, the pixel is subdivided and additional rays are traced to help the anti-aliasing process. As ray tracing is developed further, speed increases will undoubtedly come from the application of coherence or other properties of the objects being displayed. Ray tracing also lends itself to parallel processing, because rays can be traced independently of one another. VLSI implementations may therefore be expected.

Surface Detail

The shading algorithms described to this point all produce very smooth and uniform surfaces. In the real world, most surfaces have details of color and texture. Texture mapping is one of the most common techniques used to model surface patterns. The patterns are mapped onto the object surface or modeled on the surface patch itself. Color detail is applied to a smooth surface without appearing to change its geometry, while texture details give the appearance of roughness. Perturbing the surface normal will produce bumpy surfaces, brushed copper, and so forth. A wood grain or marble surface could also be achieved by applying a real-world image to a geometrically defined curved surface.

Although this method works well with smooth surfaces, it does not work well with terrains, coastlines, and jagged mountains, which require a fractal surface method. Hidden surfaces are removed, and an appropriate shading model applied.

Procedural definitions of textures, light sources, volumes, and atmospheres are collectively called "shaders." There are predefined lighting shaders for ambient, distant and point light sources, as well as for spotlights. Atmosphere shaders include depth cue and fog. Volume shaders describe volumes through which light passes and is refracted and attenuated. Atmosphere shaders are based on the principle that light is attenuated over distance, be it through clear or foggy air, and that such attenuation gives the eye a cue to spatial relationships. The syntax of these predefined shaders can be used to define custom shaders of all kinds.

References

Foley, J. D., and Van Dam, A., *Fundamentals of Interactive Computer Graphics,* Addison-Wesley, July 1984.

Newman, W. M., and Sproul, R. F., "An Approach to Graphics System Design," Proceedings of the IEEE, April 1974.

Phong, B. T., "Illumination for Computer-Generated Pictures," Communications of the ACM, Vol. 18, No. 6, June 1975, pp. 311-317.

Salmon, R., and Slater, M., *Computer Graphics-Systems and Concepts,* Addison-Wesley, 1987.

NEC

Section 16
Package Drawings

Device/Package Cross-Reference

Part Number	Ordering Designation	Package	Page
MC-434000	D	32-Pin Ceramic DIP (600-mil)	43
	E	32-Pin Plastic (FR-4) DIP (600-mil)	44
μPB100422	B	24-Pin Ceramic Flatpack	29
	D	24-Pin Ceramic DIP (400-mil)	25
μPB100470	D	18-Pin Cerdip (300-mil)	17
μPB100474	B	24-Pin Ceramic Flatpack	29
	D	24-Pin Ceramic DIP (400-mil)	25
	K	24-Pin Ceramic LCC	28
μPB100474A	BH	24-Pin Ceramic Flatpack	29
	D	24-Pin Cerdip (400-mil) #2	25
μPB100474E	DH	24-Pin Cerdip (400-mil) #1	24
	BH	24-Pin Ceramic Flatpack	29
μPB100476LL	DH	28-Pin Cerdip (400-mil) #2	36
	BH	28-Pin Ceramic Flatpack	37
μPB100480	B	20-Pin Ceramic Flatpack	20
	D	20-Pin Cerdip (300-mil)	19
μPB100484	B	28-Pin Ceramic Flatpack	37
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μPB10470	D	18-Pin Cerdip (300-mil)	17
μPB10474	D	24-Pin Cerdip (400-mil) #2	25
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μPD10500	D	24-Pin Cerdip (300-mil)	24

Device/Package Cross-Reference (cont)

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	G	24-Pin Plastic SOP (Miniflat) (450-mil)	27
μPD28C05	C	24-Pin Plastic DIP (600-mil)	23
	G	24-Pin Plastic SOP (Miniflat) (450-mil)	27
μPD28C256	CZ	28-Pin Plastic DIP (600-mil)	34
μPD28C64	C	28-Pin Plastic DIP (600-mil)	34
μPD41256	C	16-Pin Plastic DIP (300-mil)	16
	L	18-Pin Plastic Leaded Chip Carrier	18
μPD41264	C	24-Pin Plastic DIP (400-mil)	22
	V	24-Pin Plastic ZIP (350-mil)	27
μPD41464	C	18-Pin Plastic DIP (300-mil) #1	16
	L	18-Pin Plastic Leaded Chip Carrier	18
μPD421000	C	18-Pin Plastic DIP (300-mil) #2	17
	GX	24/20-Pin Plastic TSOP I	26
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
μPD42101	C	24-Pin Plastic DIP (300-mil) #2	21
	G	24-Pin Plastic SOP (Miniflat) (450-mil)	27
μPD42102	C	24-Pin Plastic DIP (300-mil) #2	21
	G	24-Pin Plastic SOP (Miniflat) (450-mil)	27
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μPD42116182		50-Pin Plastic TSOP II (400-mil)	55
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μPD42116820		44-Pin Plastic TSOP II (400-mil) #2	54
μPD42116920		44-Pin Plastic TSOP II (400-mil) #2	54
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	V	24-Pin Plastic ZIP (425-mil)	28
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Device/Package Cross-Reference (cont)

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	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD4216802	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD4216802L	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD4216900	G5	32-Pin Plastic TSOP II (400-mil)	47
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
μPD4216900L	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD4216902	G5	32-Pin Plastic TSOP II (400-mil)	47
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
μPD4216902L	G5	32-Pin Plastic TSOP II (400-mil)	47
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
μPD4217100	G5	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
μPD4217101	G5	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
μPD4217102	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
μPD4217160	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4217160L	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4217180	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4217180L	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4217400	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	G5	28/24-Pin Plastic TSOP II (400-mil)	39

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD4217402	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
μPD4217410	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
μPD4217412	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
μPD4217800	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD4217800L	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD4217802	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD4217802L	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD4217900	G5	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
μPD4217900L	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD4217902	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD4217902L	G5M	32-Pin Plastic TSOP II (400-mil)	47
	G5	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
μPD4218160	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD4218160L	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4218180	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4218180L	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
μPD42264	C	24-Pin Plastic DIP (400-mil)	22
	V	24-Pin Plastic ZIP (350-mil)	27
	LA	24-pin Plastic SOJ (300-mil)	26
μPD42270	C	28-Pin Plastic DIP (400-mil)	33
μPD42271	GF	64-Pin Plastic QFP	58
μPD42272	GF	64-Pin Plastic QFP	58
μPD42273	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
μPD42274	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
μPD42274-80	V	28-Pin Plastic ZIP (350-mil)	41
	LE	28-Pin Plastic SOJ (400-mil)	38
μPD42275	LE	40-Pin Plastic SOJ (400-mil)	49
μPD42280	GU	28-Pin Plastic SOP (Miniflat) (450-mil) #1	40
	V	28-Pin Plastic ZIP (350-mil)	41
μPD424100	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
μPD424100A	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
μPD424100L	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
μPD424101	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD424102	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD424170A	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424170L	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424190A	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424190L	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400- il)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424256	C	20-Pin Plastic DIP (300-mil)	18
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
	GX	24/20-Pin Plastic TSOP I	26
μPD424260A	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424260L	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424263A	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424263L	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD424280A	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424280L	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424400	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD424400A	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
μPD424400L	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
μPD424402	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD424410	V	20-Pin Plastic ZIP (350-mil)	19
	LB	26/20-Pin Plastic SOJ (350-mil)	30
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD424412	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD424440	LE	26/24-Pin Plastic SOJ (350-mil)	31
μPD424440L	LE	26/24-Pin Plastic SOJ (350-mil)	31
μPD424800A	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD424800L	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
	G5M	28-Pin Plastic TSOP II (400-mil)	39

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD424810A	LE	28-Pin Plastic SOJ (400-mil)	38
	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	V	28-Pin Plastic ZIP (350-mil)	41
μPD424810L	LE	28-Pin Plastic SOJ (400-mil)	38
	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	V	28-Pin Plastic ZIP (350-mil)	41
μPD424900A	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD424900L	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD42505	C	24-Pin Plastic DIP (300-mil) #2	21
	V	28-Pin Plastic ZIP (350-mil)	41
μPD42532	C	40-Pin Plastic DIP (600-mil)	49
μPD42601	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
μPD42641	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
μPD42644	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD42S16160	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD42S16160L	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD42S16180	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD42S16180L	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD42S16800	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
μPD42S16800L	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD42S16802	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
μPD42S16802L	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
μPD42S16900	G5	32-Pin Plastic TSOP II (400-mil)	47
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
μPD42S16900L	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD42S16902	G5	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
μPD42S16902L	G5	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
μPD42S17160	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD42S17160L	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD42S17180	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD42S17180L	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD42S17800	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD42S17800L	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD42S17802	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD42S17802L	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD42S17900	G5	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
μPD42S17900L	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD42S17902	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD42S17902L	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD42S18160	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
μPD42S18160L	LE	42-Pin Plastic SOJ (400-mil)	51
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
μPD42S18180	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD42S18180L	LE	42-Pin Plastic SOJ (400-mil)	51
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
μPD42S4100A	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
μPD42S4100L	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD42S4170A	V	40-Pin Plastic ZIP (400-mil)	50
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
μPD42S4170L	V	40-Pin Plastic ZIP (400-mil)	50
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
μPD42S4190A	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
μPD42S4190L	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
μPD42S4260A	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
μPD42S4260L	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
μPD42S4263A	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
μPD42S4263L	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
μPD42S4280A	V	40-Pin Plastic ZIP (400-mil)	50
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
μPD42S4280L	V	40-Pin Plastic ZIP (400-mil)	50
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD42S4400A	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD42S4400L	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD42S4440	LE	26/24-Pin Plastic SOJ (350-mil)	31
μPD42S4440L	LE	26/24-Pin Plastic SOJ (350-mil)	31
μPD42S4800A	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
μPD42S4800L	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
μPD42S4810A	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD42S4810L	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD42S4900A	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
μPD42S4900L	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
μPD431000A	GZM	32-Pin Plastic TSOP I #1	46
	CZ	32-Pin Plastic DIP (600-mil)	43
	GW	32-Pin Plastic SOP (Miniflat) (525-mil)	47
	GZ	32-Pin Plastic TSOP I #1	46
μPD431001	LE	28-Pin Plastic SOJ (400-mil)	38
μPD431004	LE	28-Pin Plastic SOJ (400-mil)	38
μPD431008	LE	32-Pin Plastic SOJ (400-mil) #1	45

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD431009	LE	36-Pin Plastic SOJ (400-mil)	48
μPD431016	LE	44-Pin Plastic SOJ (400-mil)	51
	G5	44-Pin Plastic TSOP II (400-mil) #3	55
μPD431018	G5	44-Pin Plastic TSOP II (400-mil) #3	55
	LE	44-Pin Plastic SOJ (400-mil)	51
μPD43251B	LA	24-Pin Plastic SOJ (300-mil)	26
	CR	24-Pin Plastic DIP (300-mil) #1	21
μPD43253B	LA	28-Pin Plastic SOJ (300-mil)	37
	CR	28-Pin Plastic DIP (300-mil) #2	33
μPD43254B	LA	24-Pin Plastic SOJ (300-mil)	26
	CR	24-Pin Plastic DIP (300-mil) #1	21
μPD43256A	GU	28-Pin Plastic SOP (Miniflat) (450-mil) #2	40
	C	28-Pin Plastic DIP (600-mil)	34
	GXM	32-Pin Plastic TSOP I #2	46
	GX	32-Pin Plastic TSOP I #2	46
μPD43256B	GU	28-Pin Plastic SOP (Miniflat) (450-mil) #2	40
	CZ	28-Pin Plastic DIP (600-mil)	34
μPD43258A	LA	28-Pin Plastic SOJ (300-mil)	37
	CR	28-Pin Plastic DIP (300-mil) #2	33
μPD43259A	CR	32-Pin Plastic DIP (300-mil)	42
	LA	32-Pin Plastic SOJ (300-mil)	44
μPD434000	CZ	32-Pin Plastic DIP (600-mil)	43
	GW	32-Pin Plastic SOP (Miniflat) (525-mil)	47
	G5	32-Pin Plastic TSOP II (400-mil)	47
	G5M	32-Pin Plastic TSOP II (400-mil)	47
μPD434001	LE	32-Pin Plastic SOJ (400-mil) #1	45
μPD434004	LE	32-Pin Plastic SOJ (400-mil) #1	45
μPD434008	LE	36-Pin Plastic SOJ (400-mil)	48
μPD4361B	CR	22-Pin Plastic DIP (300-mil)	20
	LA	24-Pin Plastic SOJ (300-mil)	26
μPD4362B	LA	24-Pin Plastic SOJ (300-mil)	26
	CR	22-Pin Plastic DIP (300-mil)	20
μPD4363B	CR	24-Pin Plastic DIP (300-mil) #1	21
	LA	24-Pin Plastic SOJ (300-mil)	26
μPD4368	CR	28-Pin Plastic DIP (300-mil) #2	33
	LA	28-Pin Plastic SOJ (300-mil)	37
μPD4369	CR	28-Pin Plastic DIP (300-mil) #1	32
	LA	28-Pin Plastic SOJ (300-mil)	37
μPD46710A	LN	52-Pin Plastic LCC	57
μPD46741A	LP	68-Pin Plastic LCC	59
μPD481440	LE	40-Pin Plastic SOJ (400-mil)	49

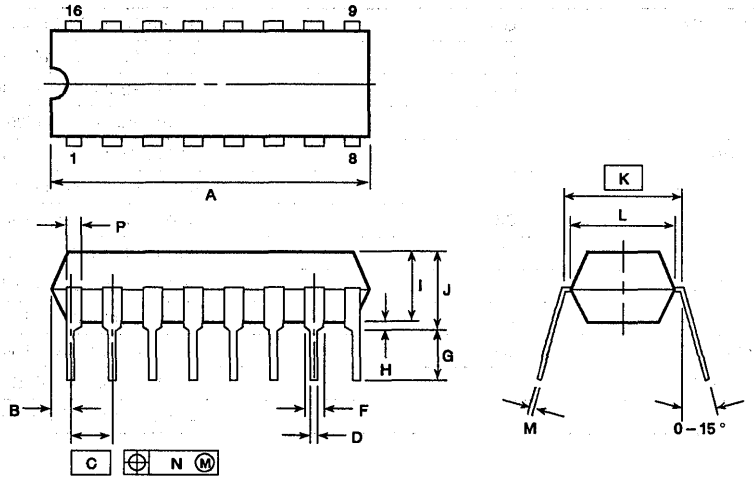
Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD482234	G5M	44-Pin Plastic TSOP II (400-mil) #1	53
	VF	40-Pin Plastic Shrink ZIP (450-mil)	50
	G5	44-Pin Plastic TSOP II (400-mil) #1	53
	LE	40-Pin Plastic SOJ (400-mil)	49
μPD482235	G5M	44-Pin Plastic TSOP II (400-mil) #1	53
	VF	40-Pin Plastic Shrink ZIP (450-mil)	50
	G5	44-Pin Plastic TSOP II (400-mil) #1	53
	LE	40-Pin Plastic SOJ (400-mil)	49
μPD485505	GU	24-Pin Plastic SOP (Miniflat) (450-mil)	27-
	V	24-Pin Plastic ZIP (350-mil)	27
μPD485506	G5	44-Pin Plastic TSOP II (400-mil) #1	53
μPD488130		32-Pin Surface Vertical Package (SVP)	48
μPD488170		32-Pin Surface Vertical Package (SVP)	48

16-Pin Plastic DIP (300-mil)

Item	Millimeters	Inches
A	20.32 max	.800 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	6.7	.264
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



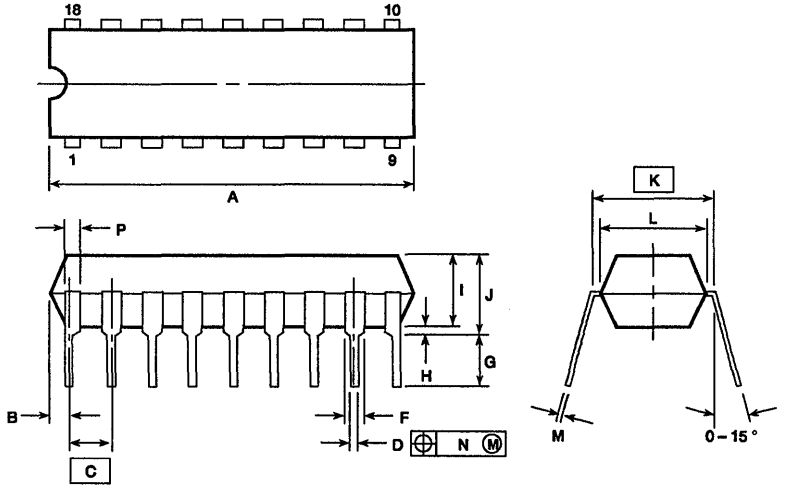
P16C-100-300SA

49NR-674B (2/90)

18-Pin Plastic DIP (300-mil) #1

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	6.7	.264
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



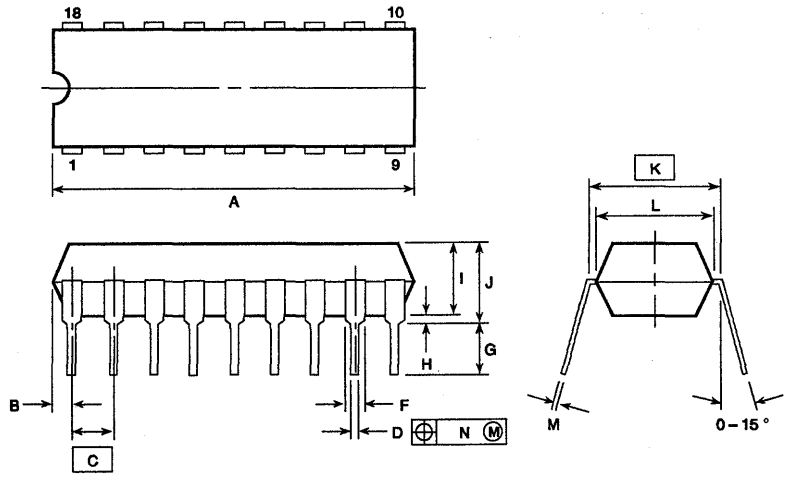
P18C-100-300SA

49NR-507B (2/92)

18-Pin Plastic DIP (300-mil) #2

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	7.35	.289
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

* Item K to center of leads when formed parallel.

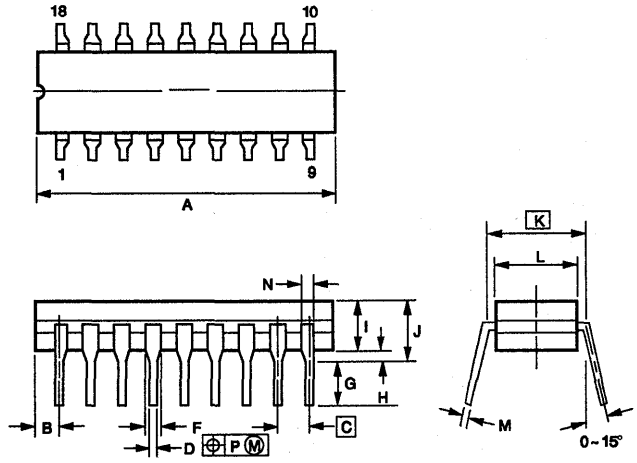


P18C-100-300WA

49NR-657B (11/91)

18-Pin Cerdip (300-mil)

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 [TP]	.100[TP]
D	0.46 ± .05	.018 $^{+.003}_{-.002}$
F	1.42 min	.055 min
G	3.50 ±.30	.138 ±.012
H	0.51 min	.020 min
I	3.95	.156
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.60	.260
M	0.25 ±.05	.010 $^{+.002}_{-.003}$
N	0.89 min	.035 min
P	0.25	.010

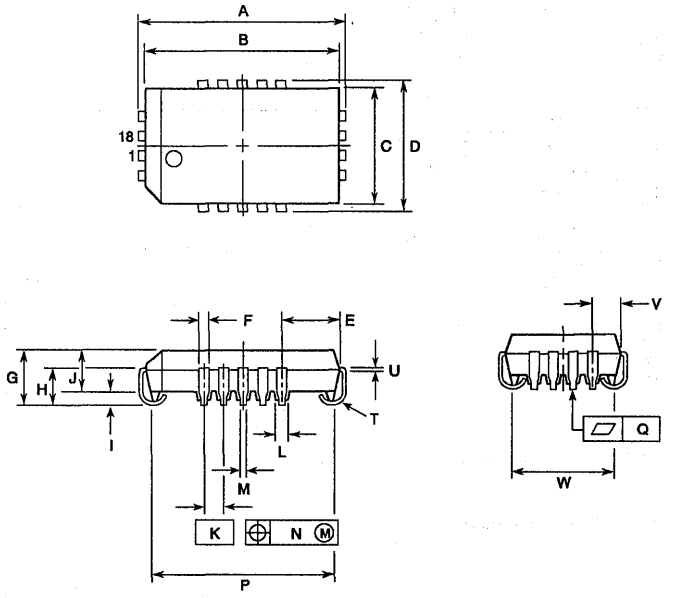


P18DH-100-300A

83H-6063B (6/89)

18-Pin Plastic Leaded Chip Carrier

Item	Millimeters	Inches
A	13.4 ± 0.2	.528 $^{+.008}_{-.009}$
B	12.5	.492
C	7.4	.291
D	8.3 ± 0.2	.327 $^{+.008}_{-.009}$
E	3.71 ± 0.15	.146 $^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ± 0.2	.138 $^{+.008}_{-.009}$
H	2.4 ± 0.2	.094 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
L	0.7	.028
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P	11.68 ± 0.20	.460 $^{+.008}_{-.009}$
Q	0.15	.006
T	0.8 rad	.031 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$
V	1.80 ± 0.15	.071 $^{+.006}_{-.007}$
W	6.60 ± 0.20	.260 $^{+.008}_{-.009}$



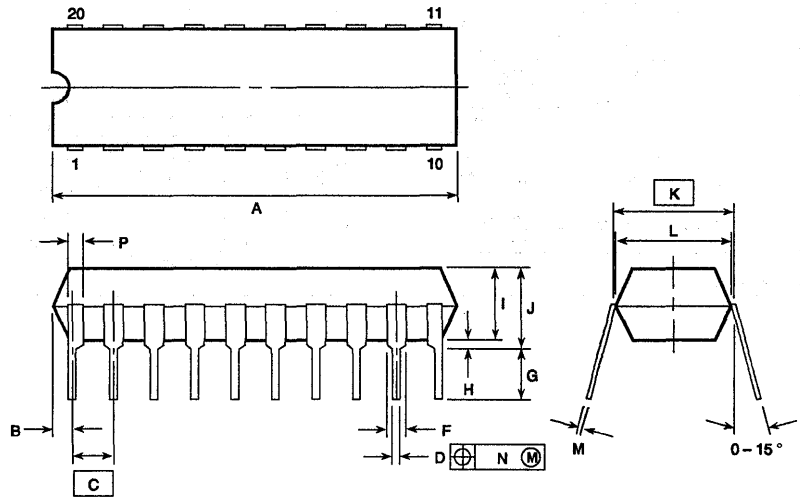
P18L-50A

49NR-675B (2/90)

20-Pin Plastic DIP (300-mil)

Item	Millimeters	Inches
A	25.4 max	1.000 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	7.35	.289
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.

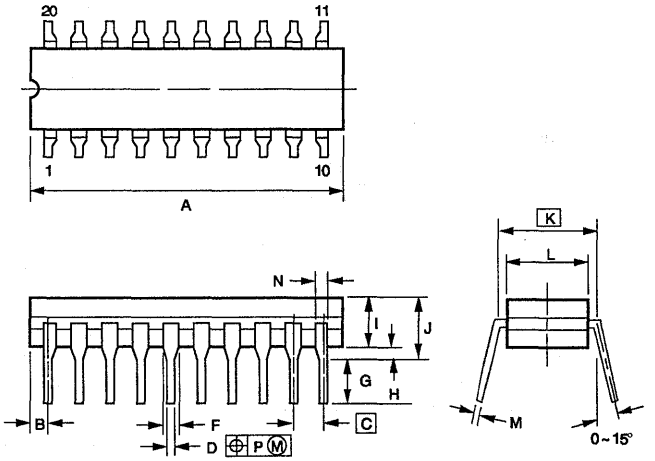


P20C-100-300WA

49NR-511B (11/91)

20-Pin Cerdip (300-mil)

Item	Millimeters	Inches
A	25.4 max	1.00 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.46 ± 0.05	.018 ± .002
F	1.42 min	.055 min
G	3.50 ± 0.30	.138 ±.012
H	0.51 min	.020 min
I	3.95	.156
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.32	.288
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.89 min	.035 min
P	0.25	.010

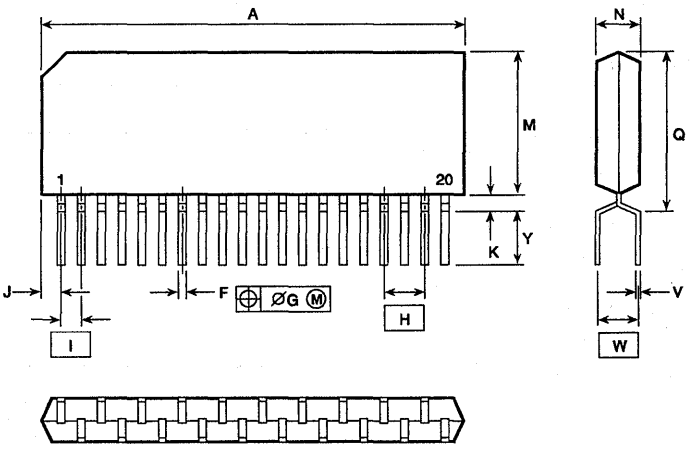


P20DH-100-300A

83IH-6194B

20-Pin Plastic ZIP (350-mil)

Item	Millimeters	Inches
A	26.67 max	1.050 max
F	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
G	Ø0.25	.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	8.9 max	.350 max
N	2.8 ± 0.2	.110 $^{+.009}_{-.008}$
Q	10.16 max	.400 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ± 0.5	.130 ± .020



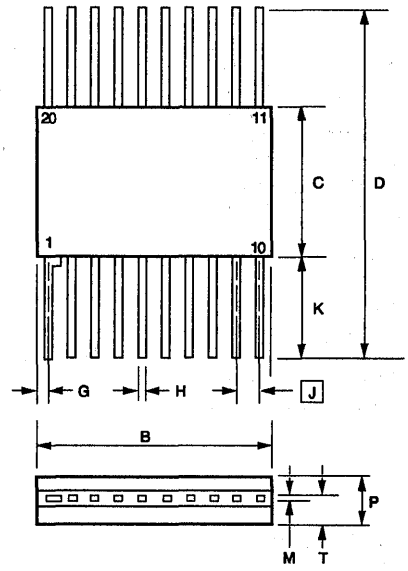
P20V-254-400A-1

49NR-620B (9/91)

16

20-Pin Ceramic Flatpack

Item	Millimeters	Inches
B	12.6 $^{+0.4}_{-0.1}$	.496 $^{+.016}_{-.004}$
C	9.8 $^{+0.4}_{-0.1}$	.388 $^{+.016}_{-.005}$
D	29.0	1.142
G	0.6	.024
H	0.43	.169
J	1.27	.050
K	9.6	.378
M	0.13	.005
P	2.18 max	.086 max
T	1.14 max	.045 max



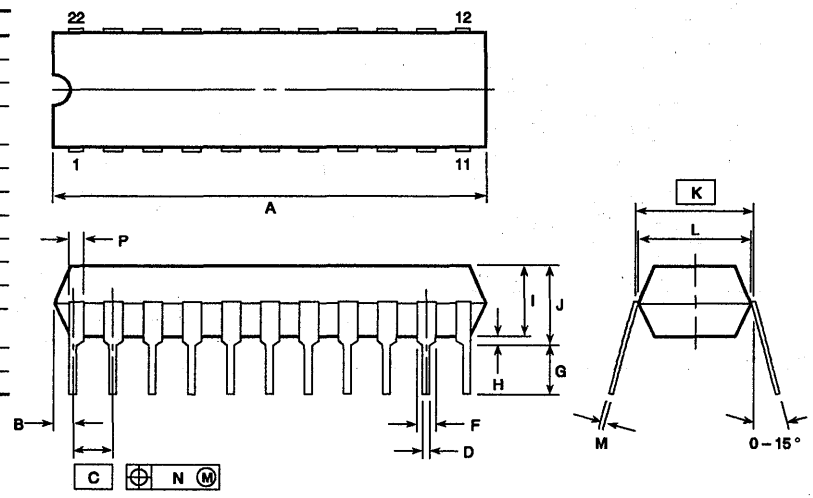
X20B-100A

83IH-5014B (7/89)

22-Pin Plastic DIP (300-mil)

Item	Millimeters	Inches
A	27.94 max	1.100 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	7.35	.289
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	0.9 min	.035 min

* Item K to center of leads when formed parallel.



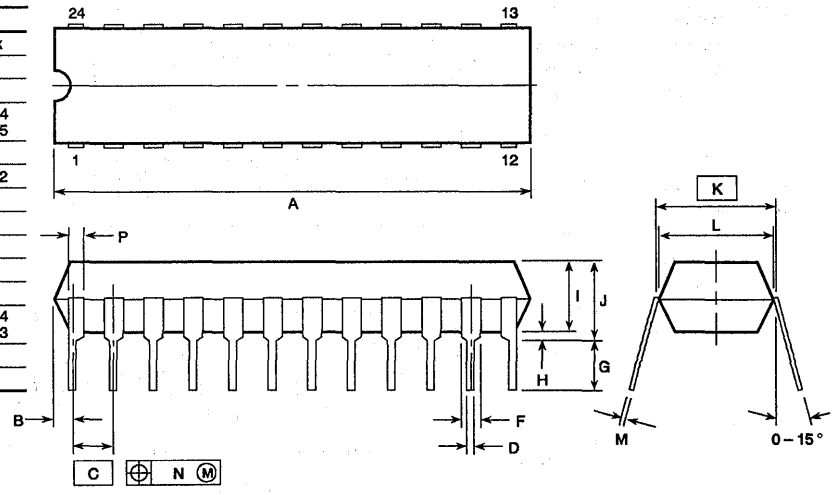
P22C-100-300WA

49NR-614B (10/89)

24-Pin Plastic DIP (300-mil) #1

Item	Millimeters	Inches
A	30.48 max	1.200 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.1 min	.043 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	7.35	.289
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	0.9 min	.035 min

* Item K to center of leads when formed parallel.



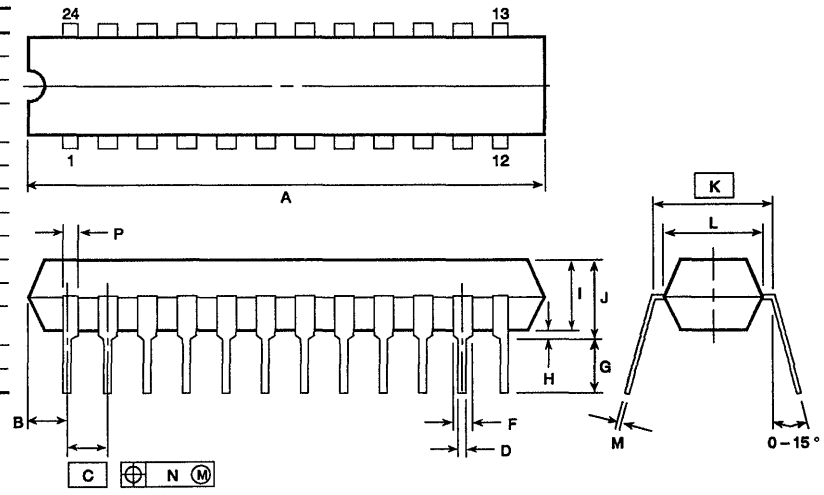
P24C-100-300WA

40NR-590B (9/89)

24-Pin Plastic DIP (300-mil) #2

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	6.4	.252
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



P24C-100-300A

40NR-619B (11/89)

16

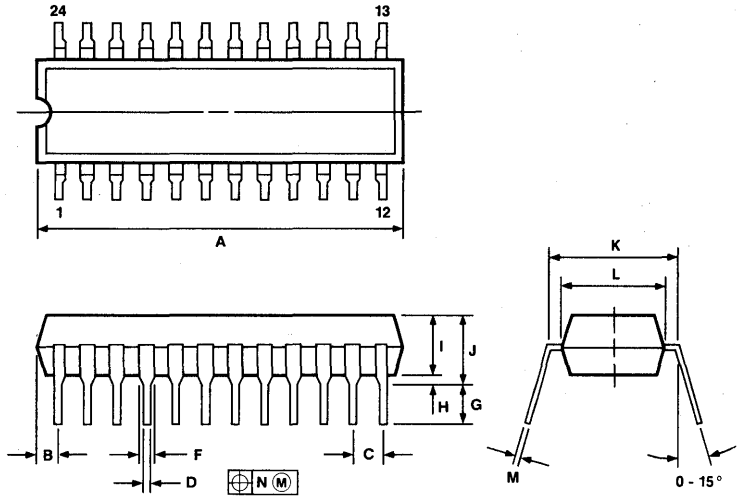
24-Pin Plastic DIP (400-mil)

Item	Millimeters	Inches
A	30.48 max	1.200 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	8.6	.339
M	.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



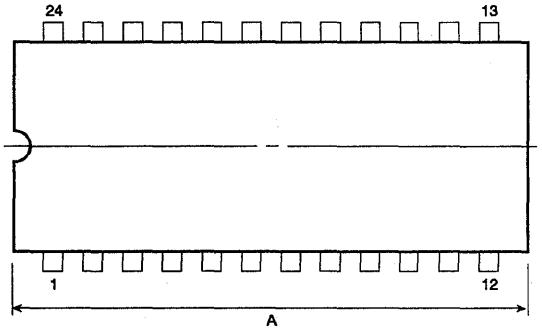
P24C-100-400A1

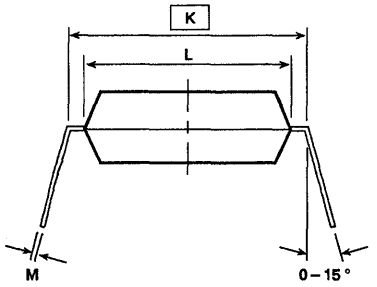
83-003627B

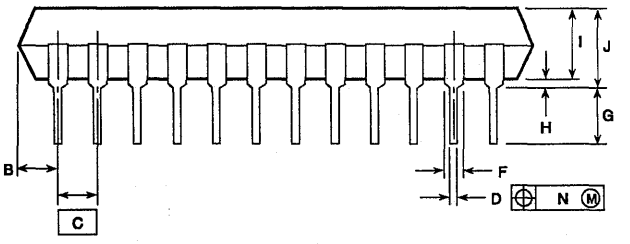
24-Pin Plastic DIP (600-mil)

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K*	15.24 (TP)	.600 (TP)
L	13.2	.520
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

* Item K to center of leads when formed parallel.





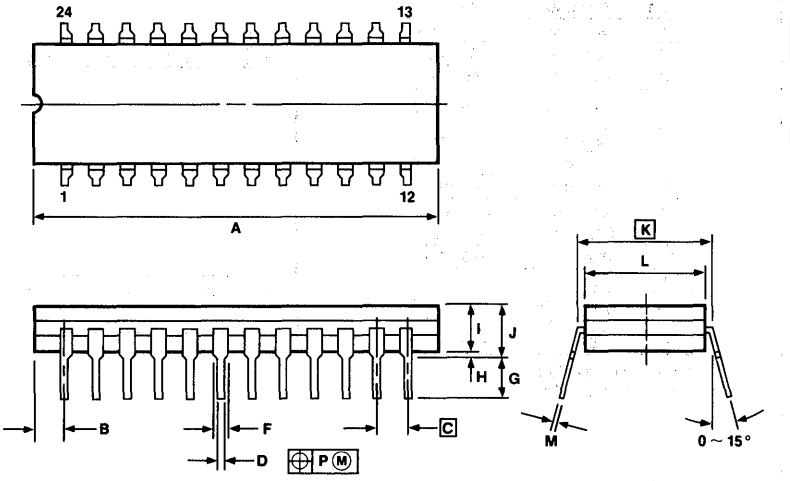


P24C-100-600

49NR-592B (6/91)

24-Pin Cerdip (300-mil)

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.46 ± 0.05	.018 ±.002
F	1.42 min	.055 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.32	.288
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
P	0.25	.010



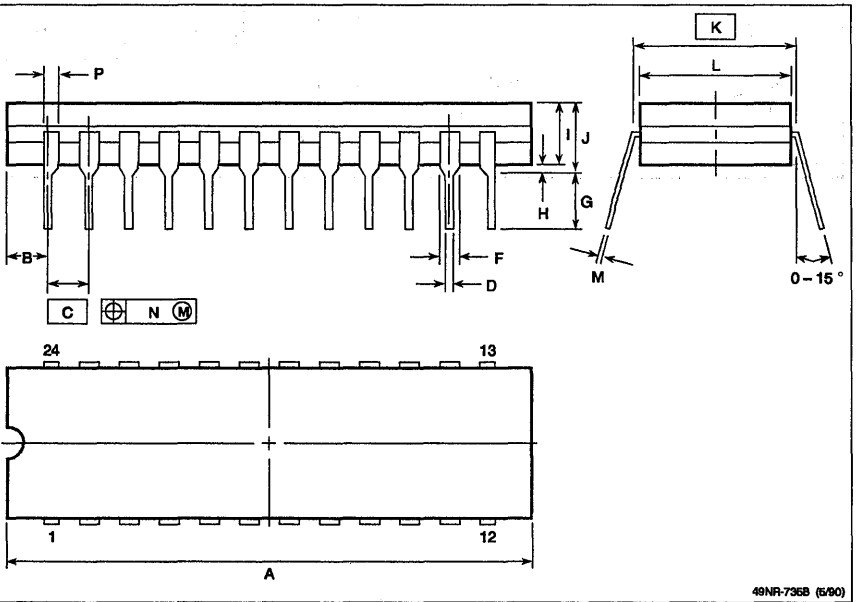
P24DH-100-300A

83-006012B

24-Pin Cerdip (400-mil) #1

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.20 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K*	10.16 (TP)	.400 (TP)
L	9.70	.382
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.25	.010
P	0.89 min	.035 min

* Item K to center of leads when formed parallel.



P24DH-100-400A

49NR-736B (5/90)

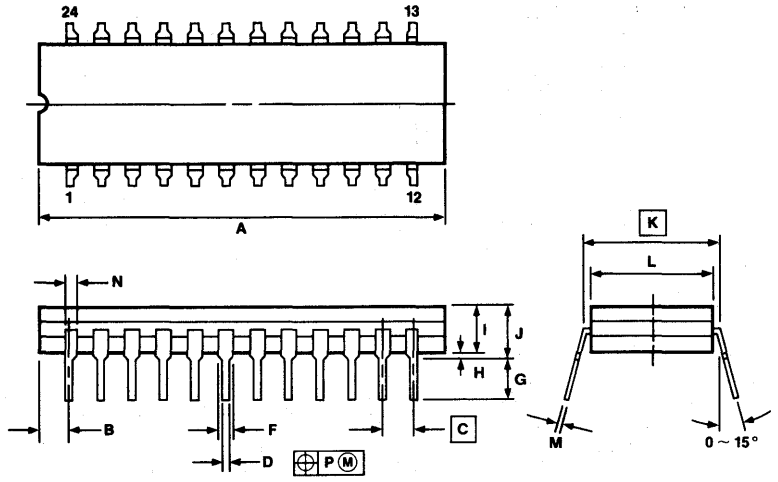
24-Pin Cerdip (400-mil) #2

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	9.70	.382
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.89 min	.035 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



P24DH-100-400A

83-005012B

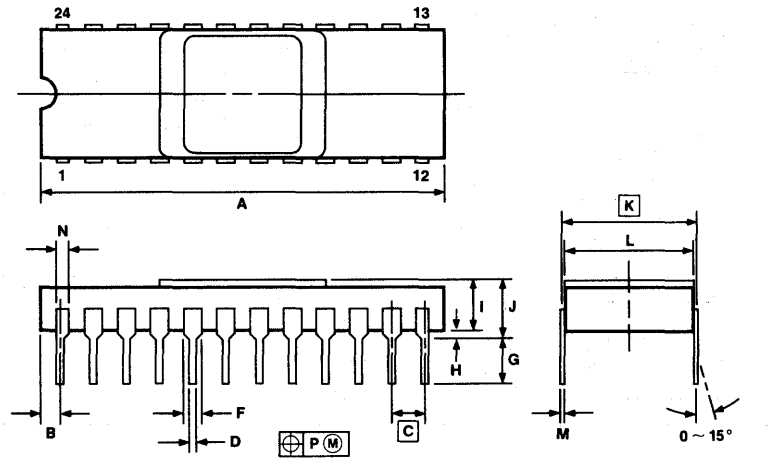
24-Pin Ceramic DIP (400-mil)

Item	Millimeters	Inches
A	33.02 max	1.30 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.46 ± 0.05	.018 ± .002
F	1.25 min	.049 min
G	3.50 ± 0.30	.138 ± .012
H	0.51 min	.020 min
I	2.74	.108
J	4.57 max	.180 max
K	10.16 [TP]	.400 [TP]
L	10.0	.394
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	1.00 min	.039 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.

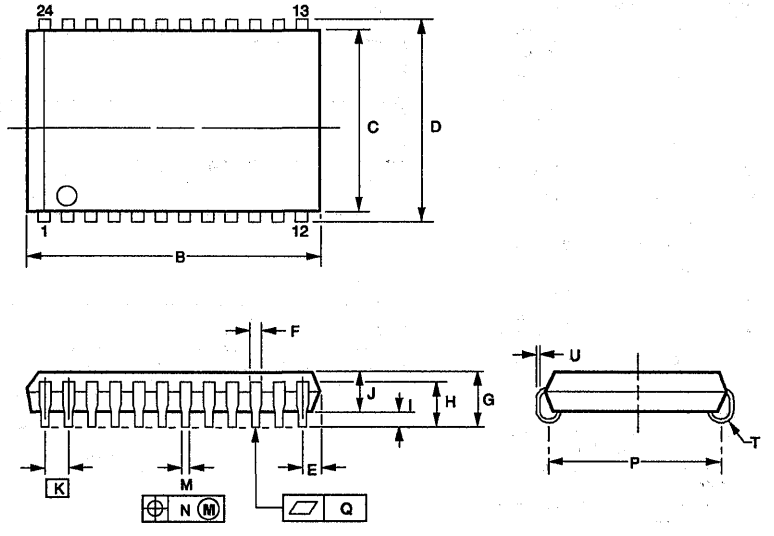


83-003579B

16

24-Pin Plastic SOJ (300-mil)

Item	Millimeters	Inches
B	$16.13^{+0.20}_{-0.35}$	$.635^{+.008}_{-.013}$
C	7.57	.298
D	8.47 ± 0.20	$.333^{+.009}_{-.008}$
E	1.08 ± 0.15	$.043^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ± 0.20	.138 ± .008
H	2.4 ± 0.20	$.094^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 [TP]	.050 [TP]
M	0.40 ± 0.10	$.016^{+.004}_{-.005}$
N	0.12	.005
P	6.73 ± 0.20	.265 ± .008
Q	0.15	.006
T	R 0.85	R .033
U	$0.20^{+0.10}_{-0.05}$	$.008^{+.004}_{-.002}$

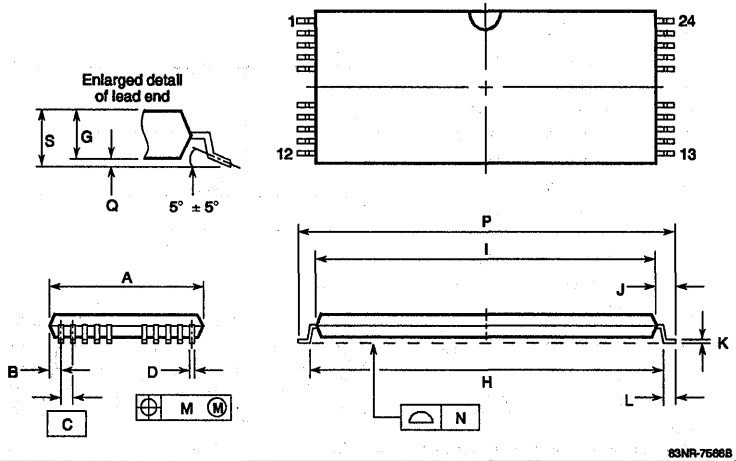


P24LA-60A

83IH-6851B

24/20-Pin Plastic TSOP I

Item	Millimeters	Inches
A	6.0 ± 0.2	.236 ± .008
B	0.45 max	.018 max
C	0.5 (TP)	.020 (TP)
D	0.20 ± 0.10	.008 ± .004
G	1.02 max	.041 max
H	15.0 ± 0.2	$.591^{+.008}_{-.009}$
I	14.4 ± 0.2	.567 ± .008
J	0.8 ± 0.2	$.031^{+.009}_{-.008}$
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	$.020^{+.004}_{-.005}$
M	0.08	.003
N	0.10	.004
P	16.0 ± 0.2	.630 ± .008
Q	0.05 ± 0.05	.002 ± .002
S	1.1 max	.044 max

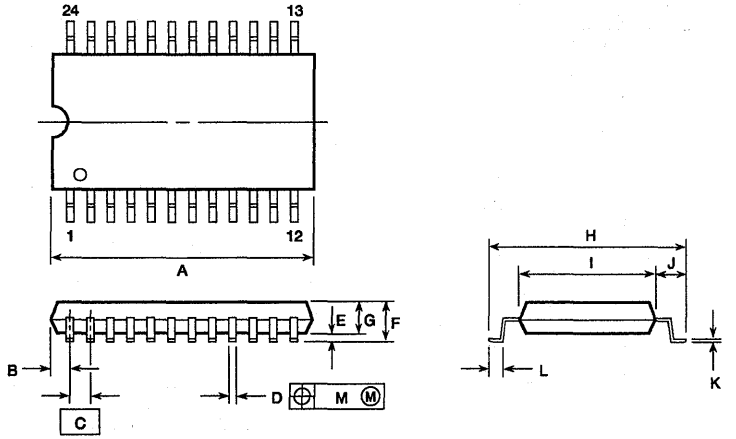


S24GX-50-UH

83NR-7566B (8/92)

24-Pin Plastic SOP (Miniflat) (450-mil)

Item	Millimeters	Inches
A	16.51 max	.650 max
B	1.27 max	.050 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	0.1 $^{+0.2}_{-0.1}$	.004 $^{+.008}_{-.004}$
F	2.5 max	.099 max
G	2.00	.079
H	12.2 ± 0.3	.480 $^{+.013}_{-.012}$
I	8.4	.331
J	1.9	.075
K	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
L	0.9 ± 0.2	.035 $^{+.009}_{-.008}$
M	0.12	.005

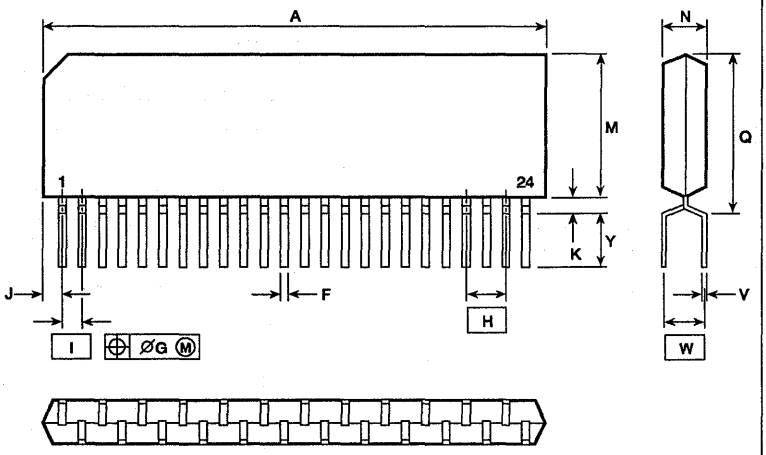


P24GM-50-450A

49NR-513B (6/91)

24-Pin Plastic ZIP (350-mil)

Item	Millimeters	Inches
A	31.75 max	1.250 max
F	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
G	∅0.25	.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	8.9 max	.350 max
N	2.8 ± 0.2	.110 $^{+.009}_{-.008}$
Q	10.16 max	.400 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ± 0.5	.130 ± .020



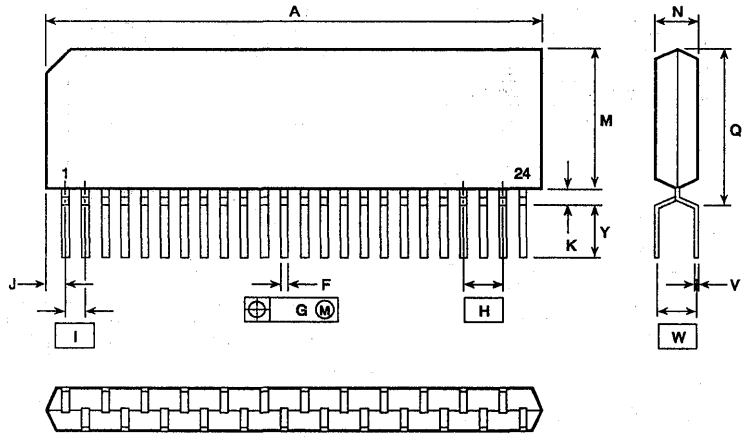
P24V-254-400A

49NR-642B (11/89)

16

24-Pin Plastic ZIP (425-mil)

Item	Millimeters	Inches
A	31.75 max	1.250 max
F	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
G	Ø0.25	Ø.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	10.8 max	.425 max
N	2.8 ± 0.2	.110 $^{+.009}_{-.008}$
Q	12.07 max	.475 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ± 0.5	.130 ± .020

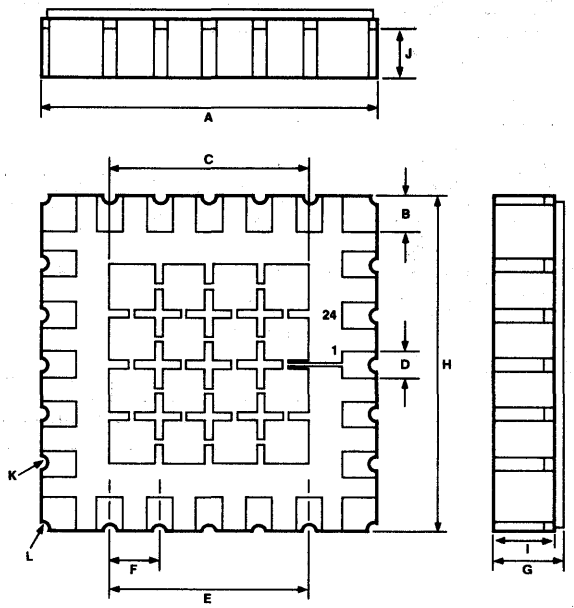


P24V-100-475A

83NR-8160B (10/91)

24-Pin Ceramic LCC

Item	Millimeters	Inches
A	8.51 ±0.4	.335 ±.016
B	.89 ±0.2	.035 ±.008
C	5.14	.202
D	.64 ±0.1	.025 $^{+.005}_{-.004}$
E	5.08	.200
F	1.27	.050
G	2.0 max	.079 max
H	8.51 ±0.4	.335 ±.016
I	1.4	.055
J	1.02	.040
K	0.2R	.008R
L	0.3R	.012R



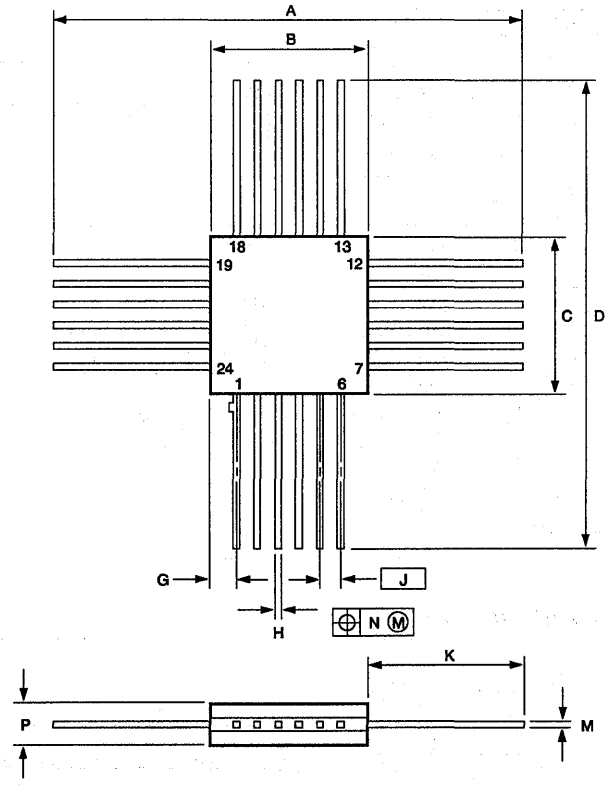
83-003582B

24-Pin Ceramic Flatpack

Item	Millimeters	Inches
A	28.5 ± 1.0	1.122 ± .040
B	9.6	.378
C	9.6	.378
D	28.5 ± 1.0	1.122 ± .040
G	1.62	.064
H	0.4 ± 0.1	$.016^{+.004}_{-.005}$
J	1.27 (TP)	.050 (TP)
K	9.45 ± 1.0	.372 ±.040
M	$0.15^{+0.10}_{-0.05}$	$.006^{+.004}_{-.002}$
N	0.25	.010
P	2.6 max	.103 max

Note:

(1) Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (TP) at maximum material condition.



X24B-127A1

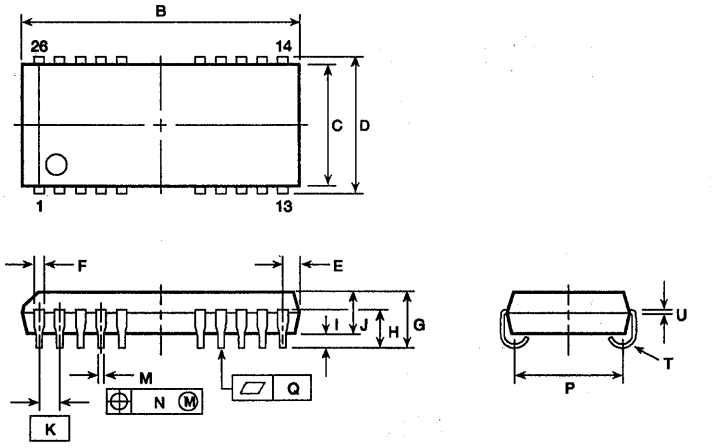
83YL-6407B

16

26/20-Pin Plastic SOJ (300-mil)

Item	Millimeters	Inches
B	17.4 $^{+0.2}_{-0.35}$	.685 $^{+.008}_{-.013}$
C	7.57	.298
D	8.47 ± 0.2	.333 $^{+.009}_{-.008}$
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ± 0.2	.138 ± .008
H	2.4 ± 0.2	.094 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P*	6.73 ± 0.20	.265 ± .008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



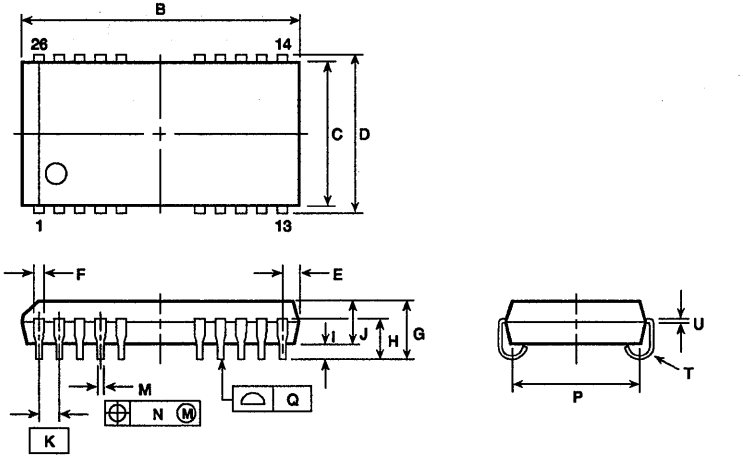
P28LA-50A

49NR-651B (9/91)

26/20-Pin Plastic SOJ (350-mil)

Item	Millimeters	Inches
B	17.4 $^{+0.2}_{-0.35}$	.685 $^{+.008}_{-.013}$
C	8.89	.350
D	9.78 ± 0.2	.385 ± .008
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.6 ± 0.2	.142 $^{+.008}_{-.007}$
H	2.45 ± 0.2	.096 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.7	.106
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P*	8.06 ± 0.20	.317 $^{+.008}_{-.007}$
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



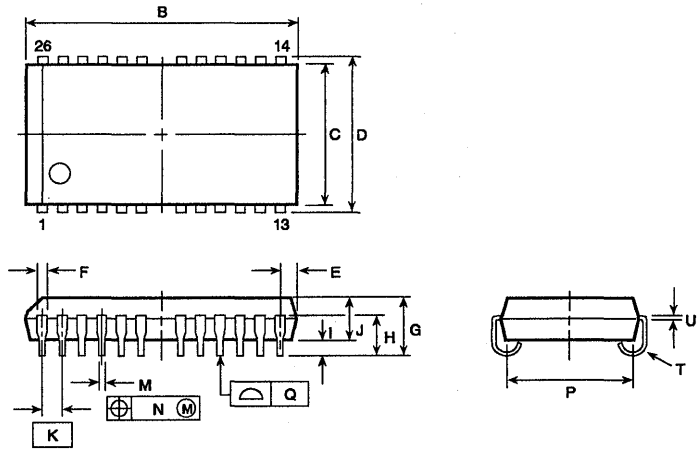
P28LB-350A

49NR-673B (9/91)

26/24-Pin Plastic SOJ (350-mil)

Item	Millimeters	Inches
B	17.4 $^{+0.2}_{-0.35}$	.685 $^{+.008}_{-.013}$
C	8.89	.350
D	9.78 ± 0.2	.385 ± .008
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.6 ± 0.2	.142 $^{+.008}_{-.007}$
H	2.45 ± 0.2	.096 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.7	.106
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P*	8.06 ± 0.20	.317 $^{+.008}_{-.007}$
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

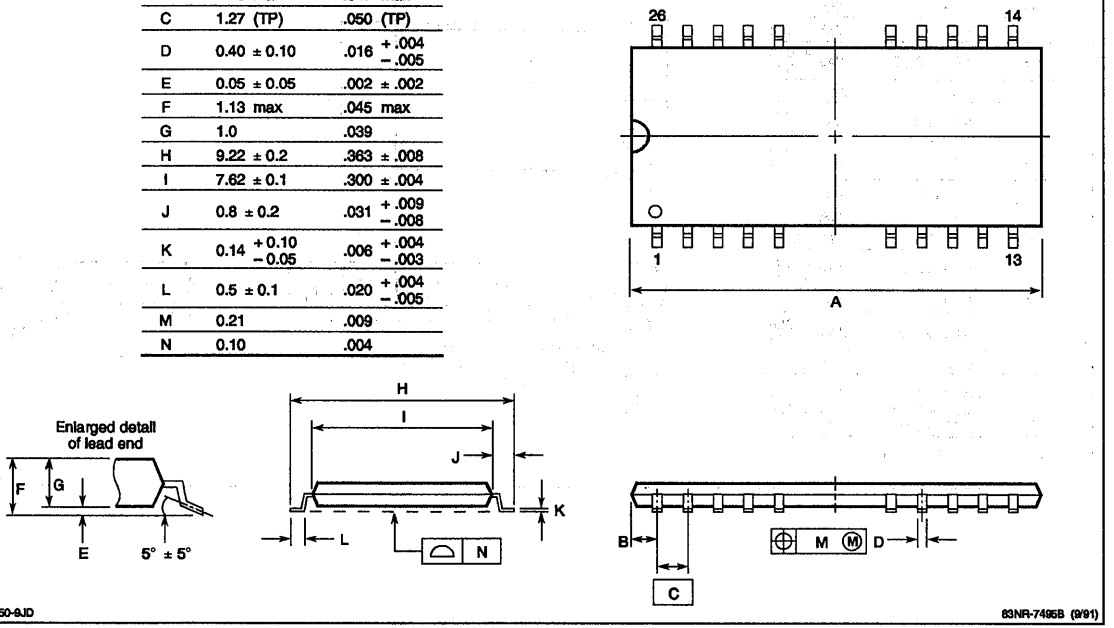
* Item P to center of leads.



83CL-6086B (10/92)

26/20-Pin Plastic TSOP II (300-mil)

Item	Millimeters	Inches
A	17.54 max	.691 max
B	1.18 max	.047 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	0.05 ± 0.05	.002 ± .002
F	1.13 max	.045 max
G	1.0	.039
H	9.22 ± 0.2	.363 ± .008
I	7.62 ± 0.1	.300 ± .004
J	0.8 ± 0.2	.031 $^{+.009}_{-.008}$
K	0.14 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
L	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
M	0.21	.009
N	0.10	.004



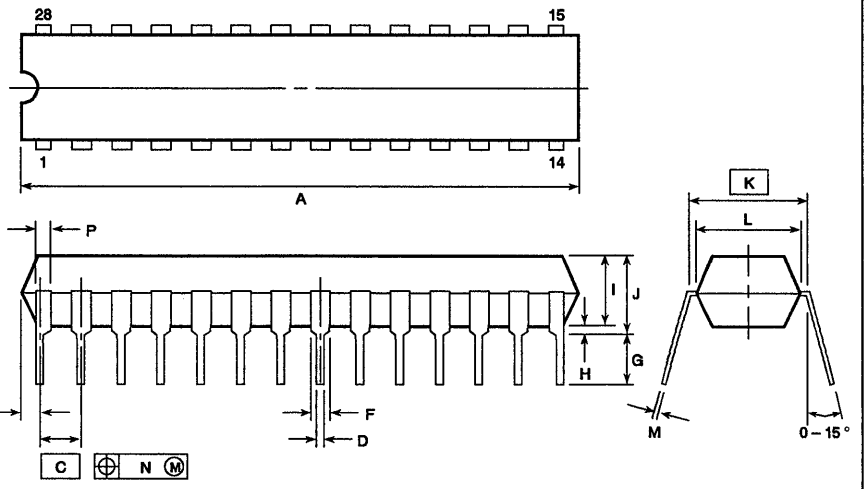
S26GS-50-9JD

83NR-7495B (9/91)

28-Pin Plastic DIP (300-mil) #1

Item	Millimeters	Inches
A	35.56 max	1.400 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	6.7	.264
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



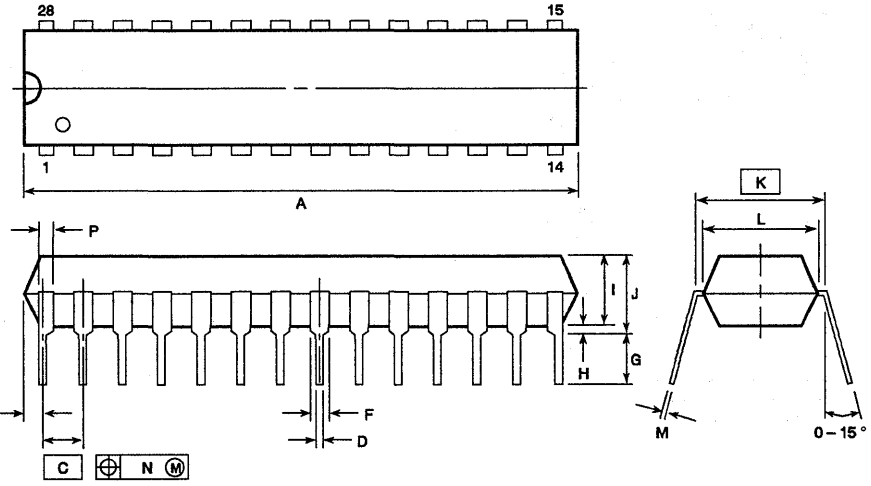
P28C-100-300SA

49NR-621B (11/89)

28-Pin Plastic DIP (300-mil) #2

Item	Millimeters	Inches
A	35.56 max	1.400 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	7.25	.286
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



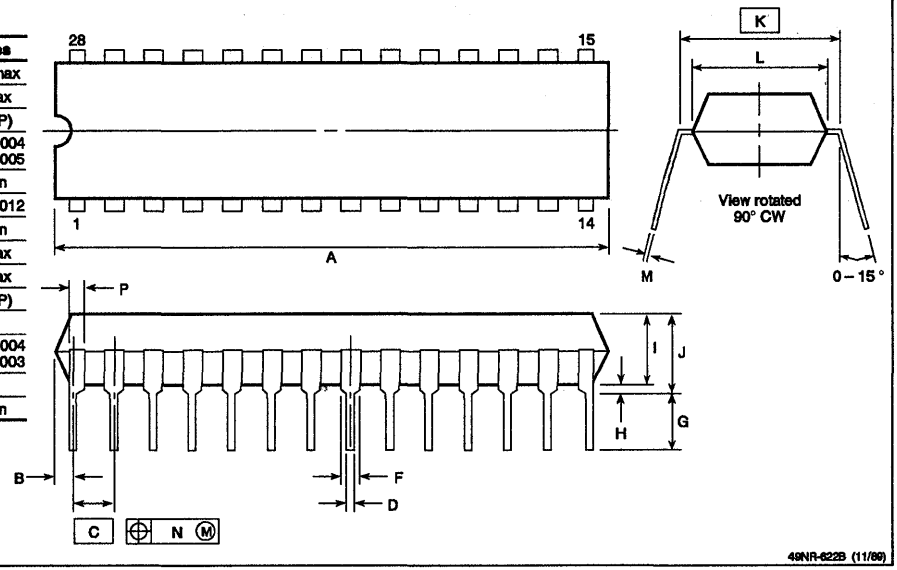
P28C-100-300WA

83NR-7521B (12/90)

28-Pin Plastic DIP (400-mil)

Item	Millimeters	Inches
A	35.56 max	1.400 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.1 min	.043 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K*	10.16 (TP)	.400 (TP)
L	8.6	.339
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	0.9 min	.035 min

* Item K to center of leads when formed parallel.



P28C-100-400

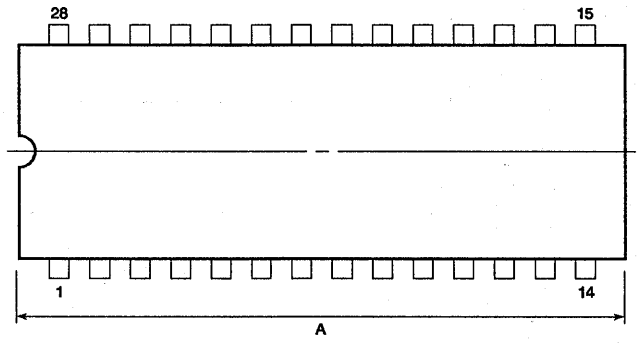
49NR-622B (11/89)

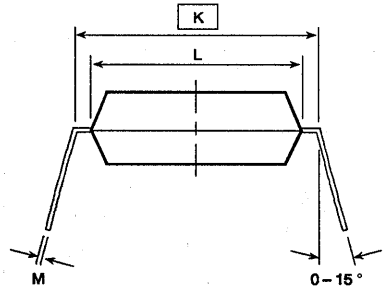
16

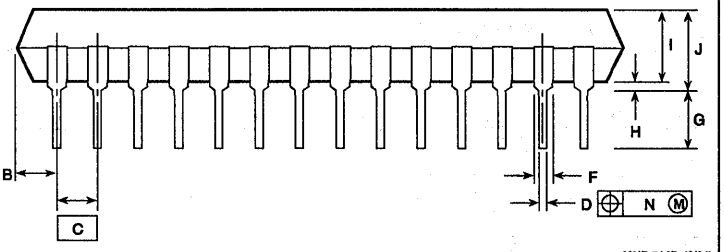
28-Pin Plastic DIP (600-mil)

Item	Millimeters	Inches
A	38.10 max	1.500 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.6 ± 0.3	.142 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K*	15.24 (TP)	.600 (TP)
L	13.2	.520
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

* Item K to center of leads when formed parallel.







P28C-100-600A1

49NR-514B (6/91)

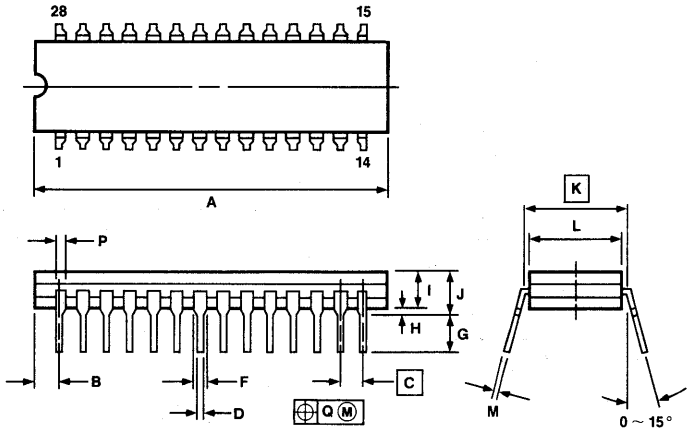
28-Pin Cerdip (400-mil) #1

Item	Millimeters	Inches
A	38.10 max	1.50 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020^{+.004}_{-.005}$
F	1.20 min	.047 min
G	3.50 ± 0.30	.138 ± .012
H	0.51 min	.020 min
I	4.00	.157
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	9.65	.380
M	0.25 ± 0.05	$.010^{+.002}_{-.003}$
P	0.89 min	.035 min
Q	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



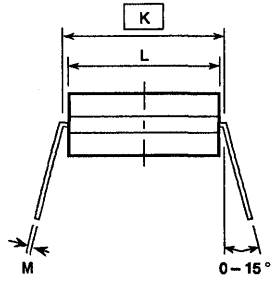
P28DH-100-400A

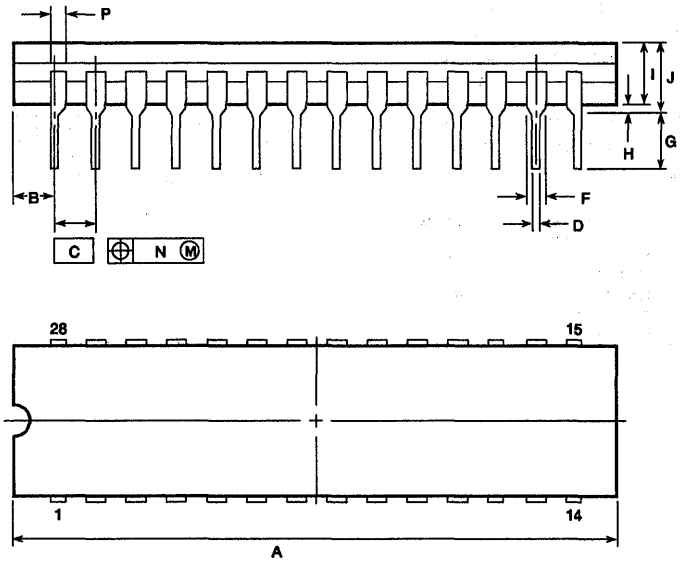
83-005015B

28-Pin Cerdip (400-mil) #2

Item	Millimeters	Inches
A	38.10 max	1.500 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.20 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	4.00	.157
J	5.08 max	.200 max
K*	10.16 (TP)	.400 (TP)
L	9.65	.380
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.25	.010
P	0.89 min	.035 min

* Item K to center of leads when formed parallel.



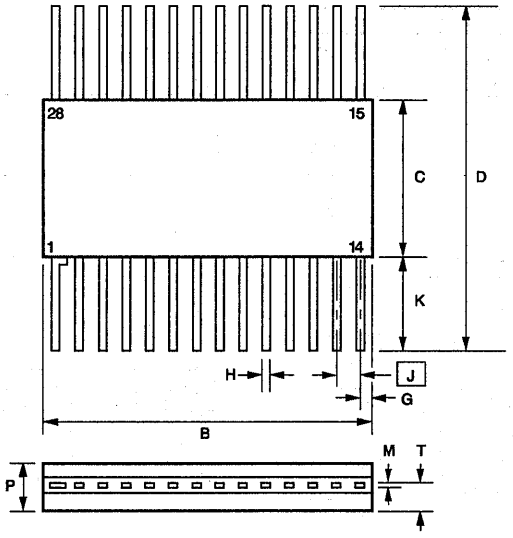


P28DH-100-400A

83CL-8883B (7/92)

28-Pin Ceramic Flatpack

Item	Millimeters	Inches
B	17.5	.689
C	9.84	.387
D	29.0	1.142
G	0.50	.020
H	0.43	.017
J	1.27 [TP]	.050 [TP]
K	9.58	.377
M	0.15	.006
P	2.18 max	.086 max
T	1.14 max	.045 max



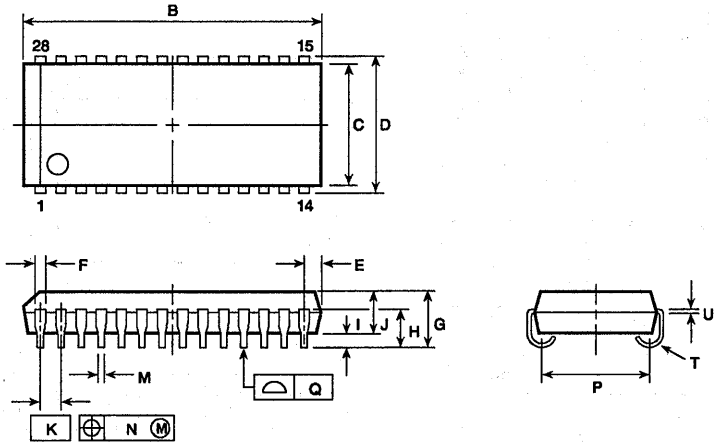
X28B-100A

83IH-4510B (5/89)

28-Pin Plastic SOJ (300-mil)

Item	Millimeters	Inches
B	18.67 $^{+0.2}_{-0.35}$	.735 $^{+.008}_{-.014}$
C	7.57	.298
D	8.47 ± 0.2	.333 $^{+.009}_{-.008}$
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.74	.029
G	3.5 ± 0.2	.138 ± .008
H	2.4 ± 0.2	.094 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.55	.100
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P *	6.73 ± 0.20	.265 ± .008
Q	0.1	.004
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



P28LA-300A

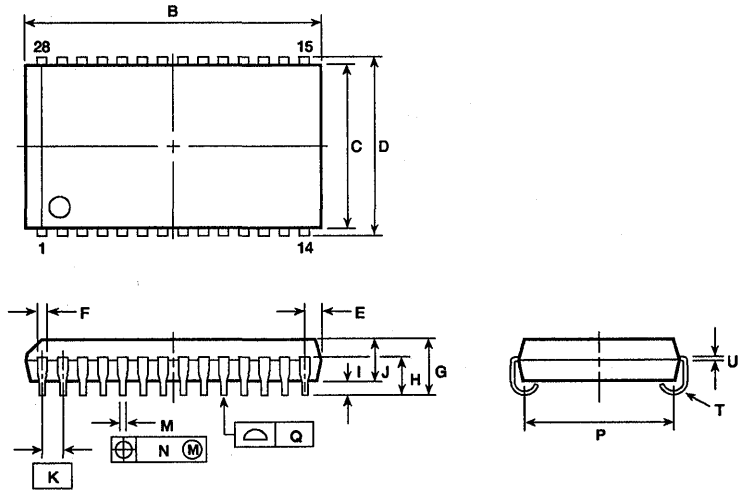
83NR-7520B (12/90)

16

28-Pin Plastic SOJ (400-mil)

Item	Millimeters	Inches
B	18.67 $^{+0.20}_{-0.35}$	.735 $^{+.008}_{-.013}$
C	10.16	.400
D	11.18 ± 0.20	.440 $^{+.006}_{-.007}$
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ± 0.2	.138 $^{+.006}_{-.007}$
H	2.4 ± 0.2	.094 $^{+.006}_{-.007}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P *	9.40 ± 0.20	.370 $^{+.006}_{-.007}$
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



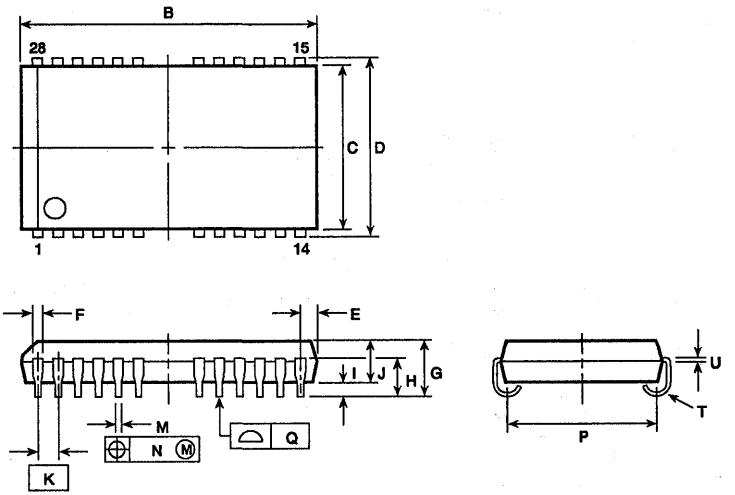
P28LA-400A-1

49NR-690B (1/92)

28/24-Pin Plastic SOJ (400-mil)

Item	Millimeters	Inches
B	18.67 $^{+0.20}_{-0.35}$	.735 $^{+.008}_{-.013}$
C	10.16	.400
D	11.18 ± 0.20	.440 $^{+.006}_{-.007}$
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.7	.028
G	3.5 ± 0.2	.138 $^{+.006}_{-.007}$
H	2.4 ± 0.2	.094 $^{+.006}_{-.007}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P *	9.40 ± 0.20	.370 $^{+.006}_{-.007}$
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.

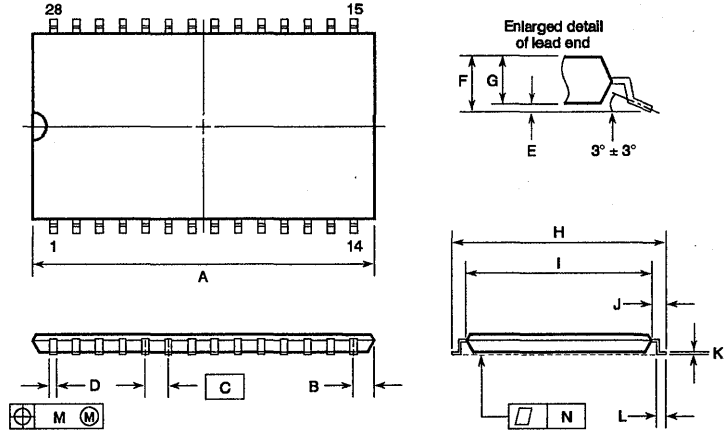


P28LB-400A1

83NR-8156B (4/92)

28-Pin Plastic TSOP II (400-mil)

Item	Millimeters	Inches
A	18.81 max	.741 max
B	1.15 max	.046 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.044 max
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	0.14 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
L	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
M	0.21	.009
N	0.10	.004

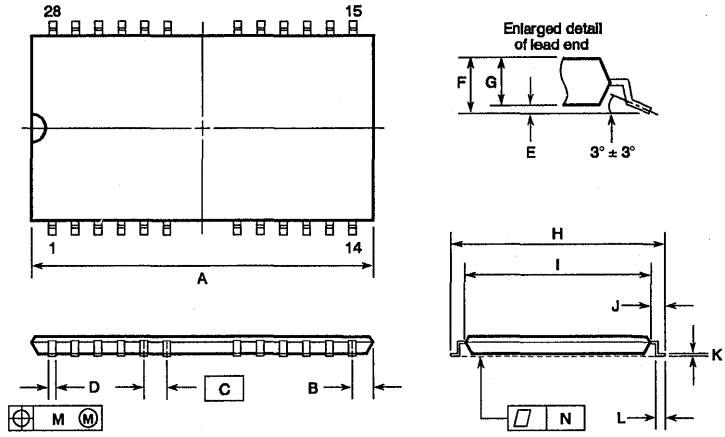


S28G5-50-7JD

83RD-8340B (1/92)

28/24-Pin Plastic TSOP II (400-mil)

Item	Millimeters	Inches
A	18.81 max	.741 max
B	1.15 max	.045 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.043 max
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.2	.400 ± .008
J	0.8 ± 0.2	.031 ± .008
K	0.125 $^{+0.10}_{-0.05}$	.005 $^{+.004}_{-.002}$
L	0.5 ± 0.1	.020 ± .004
M	0.21	.008
N	0.10	.004



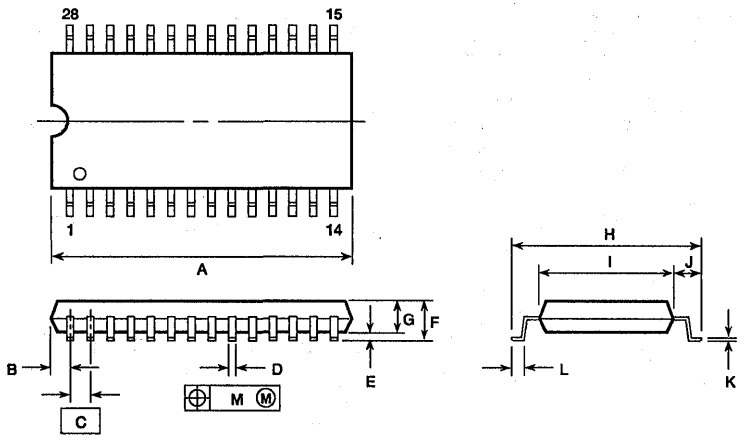
S28G5-50-7JD1

83RD-8157B (10/91)

16

28-Pin Plastic SOP (Miniflat) (450-mil) #1

Item	Millimeters	Inches
A	19.05 max	.750 max
B	1.27 max	.050 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	0.1 $^{+0.2}_{-0.1}$	.004 $^{+.008}_{-.004}$
F	2.5 max	.099 max
G	2.00	.079
H	11.8 ± 0.3	.465 $^{+.012}_{-.013}$
I	8.4	.331
J	1.7	.067
K	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
L	0.7 ± 0.2	.028 $^{+.008}_{-.009}$
M	0.12	.005

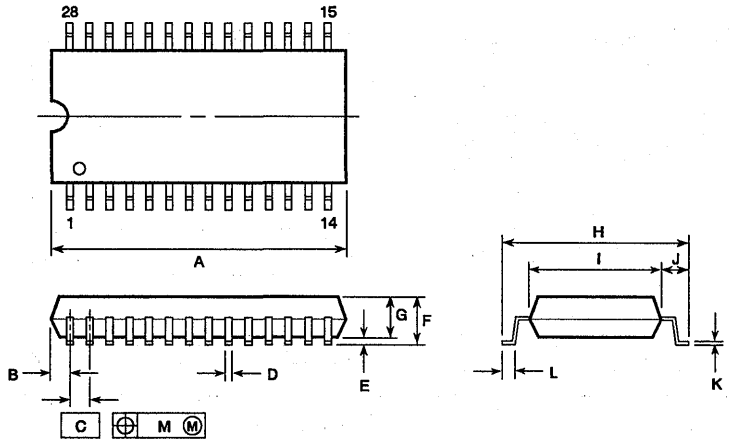


P28GM-50-450A1

49NR-623B (12/91)

28-Pin Plastic SOP (Miniflat) (450-mil) #2

Item	Millimeters	Inches
A	19.05 max	.750 max
B	1.27 max	.050 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	0.1 ± 0.1	.004 $^{+.005}_{-.004}$
F	3.0 max	.119 max
G	2.55	.100
H	11.8 ± 0.3	.465 $^{+.012}_{-.013}$
I	8.4	.331
J	1.7	.067
K	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
L	0.7 ± 0.2	.028 $^{+.008}_{-.009}$
M	0.12	.005

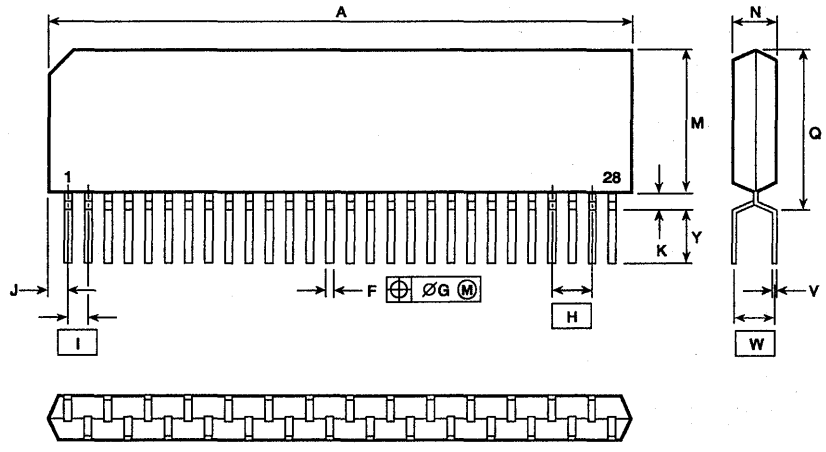


P28GM-50-450A2

49NR-635B (11/89)

28-Pin Plastic ZIP (350-mil)

Item	Millimeters	Inches
A	36.83 max	1.450 max
F	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
G	Ø0.25	.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	8.9 max	.350 max
N	2.8 ± 0.2	.110 $^{+.009}_{-.008}$
Q	10.16 max	.400 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ± 0.5	.130 ± .020



P28V-254-400A

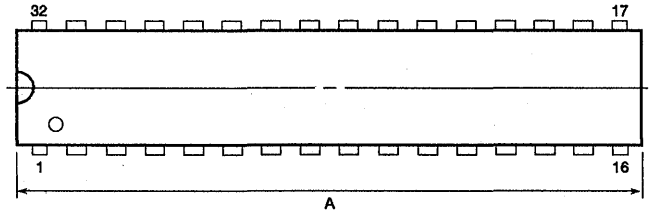
49NR-702B (4/92)

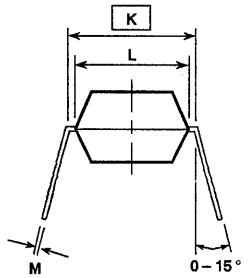
16

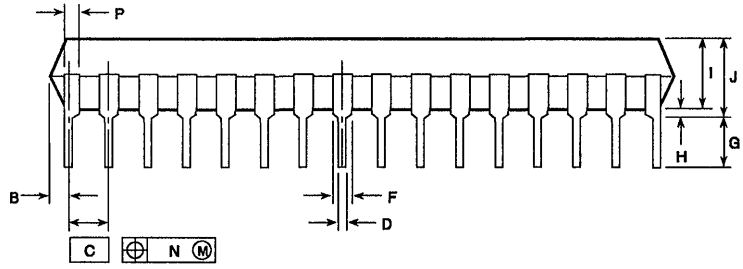
32-Pin Plastic DIP (300-mil)

Item	Millimeters	Inches
A	40.64 max	1.600 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	7.25	.285
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.01
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.





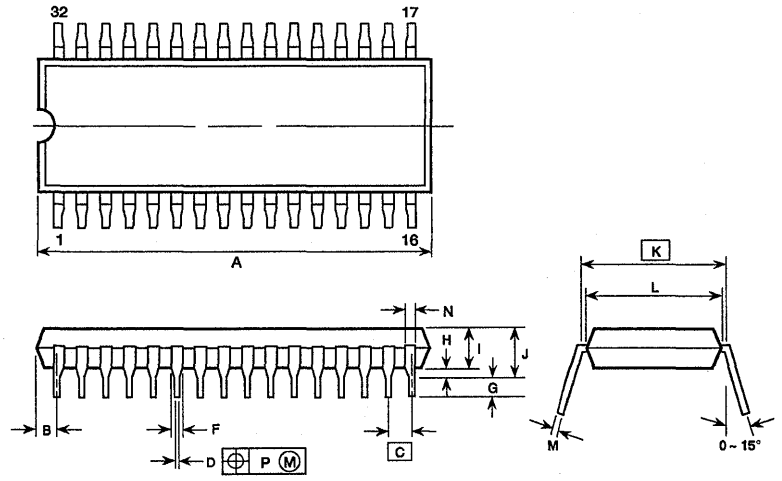


P32C-100-300WA

83NR-7543B (1/91)

32-Pin Plastic DIP (600-mil)

Item	Millimeters	Inches
A	40.64 max	1.60 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020^{+.004}_{-.005}$
F	1.1 min	.043 min
G	3.2 ± 0.30	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	$0.25^{+0.10}_{-0.05}$	$.010^{+.004}_{-.003}$
N	0.9 min	.035 min
P	0.25	.010

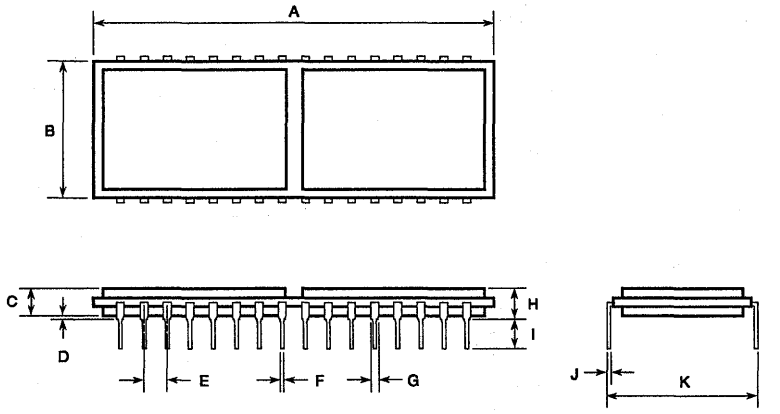


P32C-100-600A

83IH-5818B (9/89)

32-Pin Ceramic DIP (600-mil)

Item	Millimeters	Inches
A	43.053 ± .127	1.7 ± 0.01
B	14.99 ± .254	.59 ± 0.10
C	9.78 max	.385 max
D	0.254 ± .127	.010 ± .005
E	2.54 [TP]	.100 [TP]
F	0.508 ± .127	.02 ± .005
G	1.27 ± .381	.05 ± .015
H	10.287 max	.405 max
I	3.81 ± .635	.15 ± .025
J	0.254 ± .076	.01 ± .003
K	15.37 ± .381	.605 ± .015

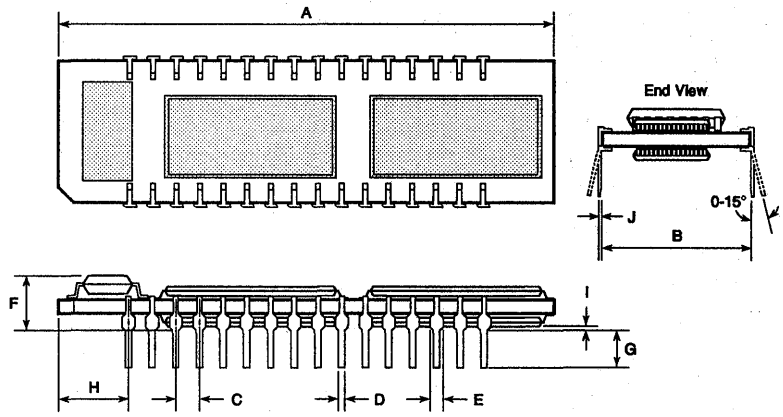


83FM-8966B (8/92)

16

32-Pin Plastic (FR-4) DIP (600-mil)

Item	Millimeters	Inches
A	53.47 ± 0.13	2.105 ± .005
B	15.24	.600
C	2.54 [TP]	.100 [TP]
D	0.47 ± 0.12	.019 ± .005
E	1.02	.040
F	5.84 max	.230 max
G	2.54 min	.100 min
H	7.62	.300
I	0.38 min	.015 min
J	0.28 ± 0.08	.011 ± .003

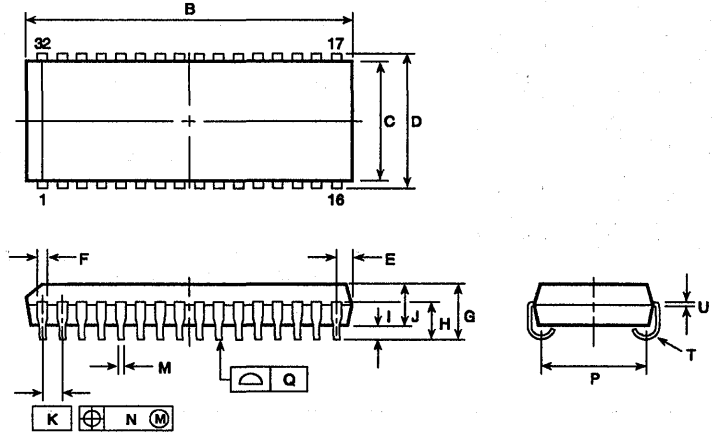


83FM-8905B (8/92)

32-Pin Plastic SOJ (300-mil)

Item	Millimeters	Inches
B	21.21 $^{+0.3}_{-0.35}$	.835 $^{+.009}_{-.014}$
C	7.57	.298
D	8.47 ± 0.2	.333 $^{+.009}_{-.008}$
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.74	.029
G	3.5 ± 0.2	.138 ± .008
H	2.4 ± 0.2	.094 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.55	.100
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P*	6.73 ± 0.20	.265 ± .008
Q	0.1	.004
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



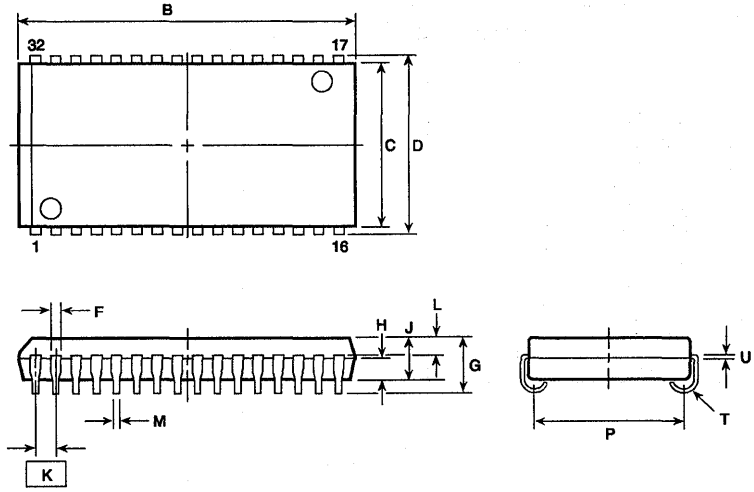
P32LA-300A

83NR-7544B (1/91)

32-Pin Plastic SOJ (400-mil) #1

Item	Millimeters	Inches
B	21.01 ± 0.15	.827 ± .006
C	10.16 ± 0.05	.400 ± .002
D	11.18 ± 0.10	.440 ± .004
F	0.74 ± 0.10	.029 ± .004
G	3.5 ± 0.10	.138 ± .004
H	1.445 ± 0.025	.057 ± .001
J	2.6	.102
K	1.27 (TP)	.050 (TP)
L	0.955 ± 0.025	.038 ± .001
M	0.40 ± 0.05	.016 ± .002
P*	9.40 ± 0.15	.370 ± .006
T	0.85 ± 0.10 rad	.033 ± .004 rad
U	0.22 ± 0.05	.009 ± .002

* Item P to center of leads.

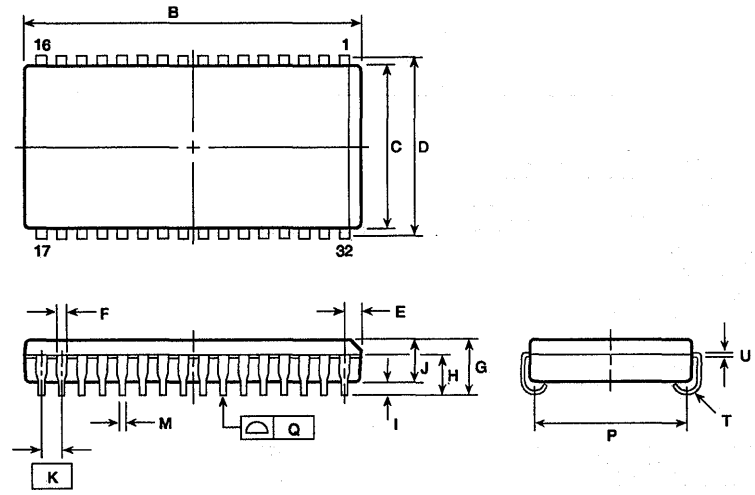


83YL-8647B (6/92)

32-Pin Plastic SOJ (400-mil) #2

Item	Millimeters	Inches
B	21.21 $^{+0.20}_{-0.35}$	.835 $^{+.008}_{-.014}$
C	10.16	.400
D	11.18 ± 0.20	.440 ± .008
E	1.08 ± 0.15	.043 ± .006
F	0.6	.024
G	3.5	.138
H	2.545 ± 0.2	.100 ± .008
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 ± .004
P*	9.40 ± 0.20	.370 ± .008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.

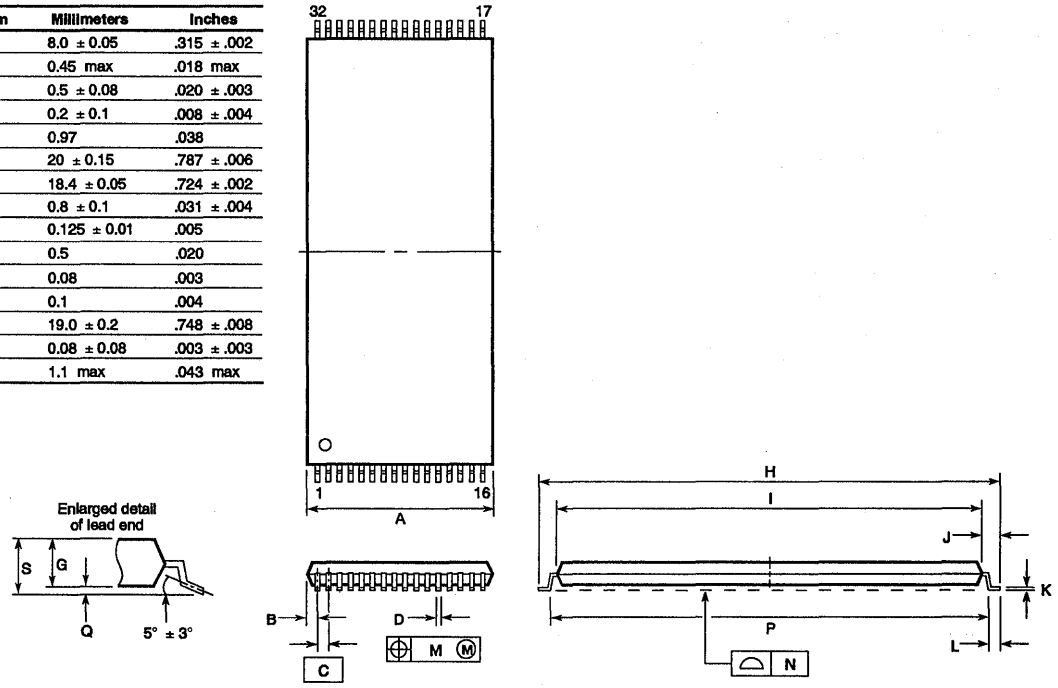


83YL-9023B (9/92)

16

32-Pin Plastic TSOP I #1

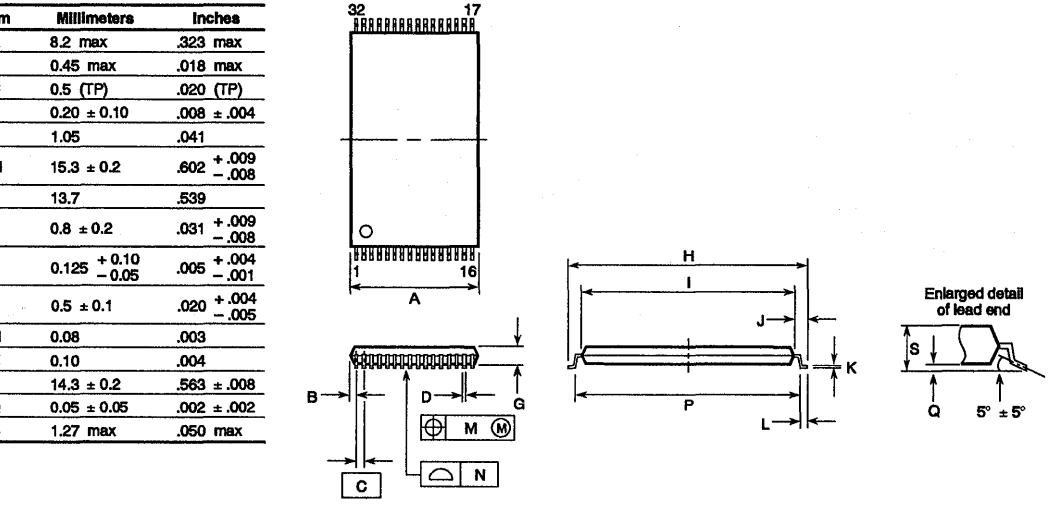
Item	Millimeters	Inches
A	8.0 ± 0.05	.315 ± .002
B	0.45 max	.018 max
C	0.5 ± 0.08	.020 ± .003
D	0.2 ± 0.1	.008 ± .004
G	0.97	.038
H	20 ± 0.15	.787 ± .006
I	18.4 ± 0.05	.724 ± .002
J	0.8 ± 0.1	.031 ± .004
K	0.125 ± 0.01	.005
L	0.5	.020
M	0.08	.003
N	0.1	.004
P	19.0 ± 0.2	.748 ± .008
Q	0.08 ± 0.08	.003 ± .003
S	1.1 max	.043 max



49NR-737B (11/91)

32-pin Plastic TSOP I #2

Item	Millimeters	Inches
A	8.2 max	.323 max
B	0.45 max	.018 max
C	0.5 (TP)	.020 (TP)
D	0.20 ± 0.10	.008 ± .004
G	1.05	.041
H	15.3 ± 0.2	.602 $^{+.009}_{-.008}$
I	13.7	.539
J	0.8 ± 0.2	.031 $^{+.009}_{-.008}$
K	0.125 $^{+0.10}_{-0.05}$	.005 $^{+.004}_{-.001}$
L	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
M	0.08	.003
N	0.10	.004
P	14.3 ± 0.2	.563 ± .008
Q	0.05 ± 0.05	.002 ± .002
S	1.27 max	.050 max

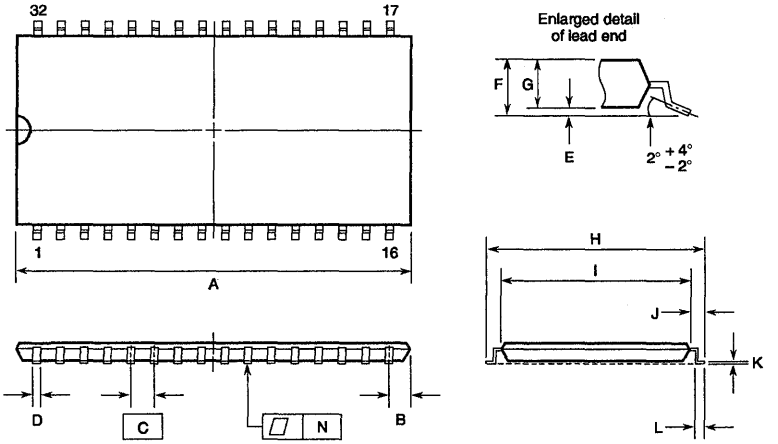


S32GX-50-EJA

49NR-601B (11/91)

32-Pin Plastic TSOP II (400-mil)

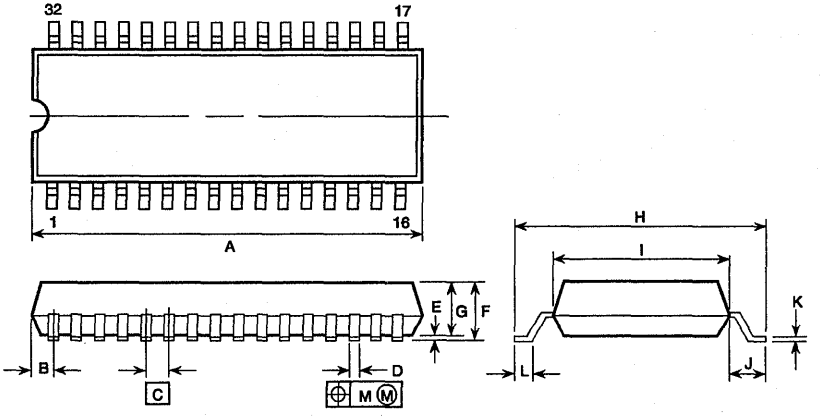
Item	Millimeters	Inches
A	21.16 max	.833 max
B	1.06 max	.042 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.043 max
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	$.020^{+.004}_{-.005}$
N	0.10	.004



83YL-9026B (9/92)

32-Pin Plastic SOP (Miniflat) (525-mil)

Item	Millimeters	Inches
A	20.61 max	.812 max
B	0.78 max	.031 max
C	1.27 [TP]	.050 [TP]
D	$0.40^{+0.10}_{-0.05}$	$.016^{+.004}_{-.003}$
E	0.05 ±0.05	.002 ±.002
F	2.85 max	.113 max
G	2.7	.106
H	14.1 ±0.3	.555 ±.012
I	11.3	.445
J	1.4	.055
K	$0.20^{+0.10}_{-0.05}$	$.008^{+.004}_{-.002}$
L	0.8 ±0.2	$.031^{+.009}_{-.008}$
M	0.12	.005



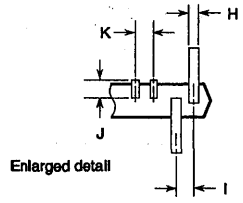
S32GM-50-525A-1

83IH-6227B (10/90)

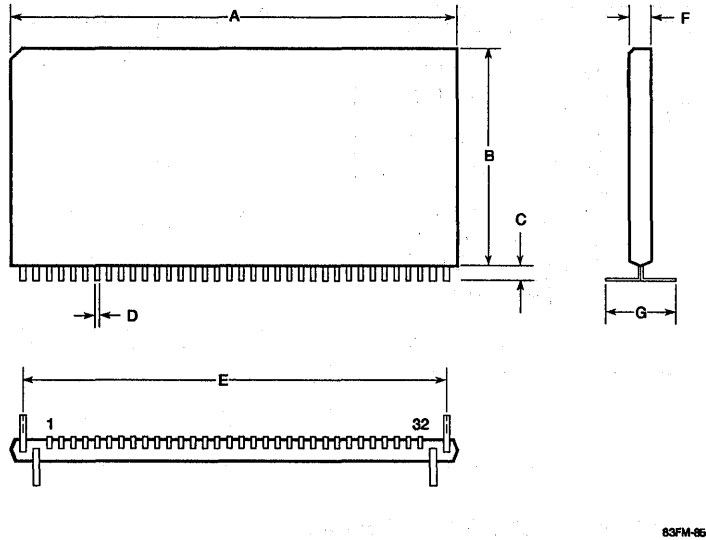
16

32-Pin Surface Vertical Package (SVP)

Item	Millimeters	Inches
A	25.0	.984
B	11.0	.433
C	0.5	.020
D	0.32	.013
E	24.10	.949
F	1.25	.049
G	3.80	.150
H	0.52	.020
I	0.90	.035
J	0.75	.030
K	0.65	.026



Enlarged detail

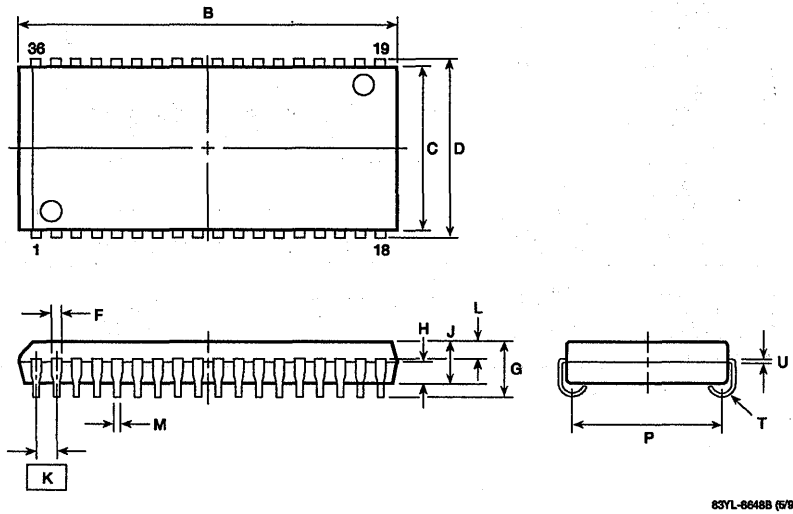


83FM-8556B

36-Pin Plastic SOJ (400-mil)

Item	Millimeters	Inches
B	23.55 ± 0.15	.927 ± .006
C	10.16 ± 0.05	.400 ± .002
D	11.18 ± 0.10	.440 ± .004
F	0.74 ± 0.10	.029 ± .004
G	3.5 ± 0.10	.138 ± .004
H	1.445 ± 0.025	.057 ± .001
J	2.6	.102
K	1.27 (TP)	.05 (TP)
L	0.955 ± 0.025	.0376 ± .001
M	0.40 ± 0.05	.0157 ± .002
P*	9.40 ± 0.15	.37 ± .006
T	0.85 ± 0.10 rad	.033 ± .004 rad
U	0.22 ± 0.05	.009 ± .002

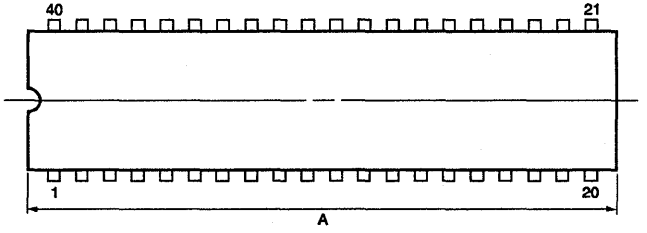
* Item P to center of leads.

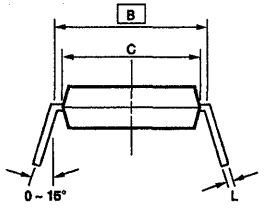


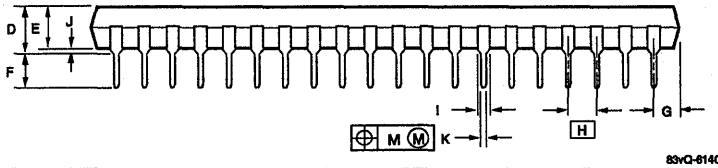
83YL-6648B (5/92)

40-Pin Plastic DIP (600-mil)

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	15.24 [TP]	.600 [TP]
C	13.2	.520
D	5.72 max	.225 max
E	4.31 max	.170 max
F	3.6 ±0.3	.142 ±.012
G	2.54 max	.100 max
H	2.54 [TP]	.100 [TP]
I	1.2 min	.047 min
J	0.51 min	.020 min
K	0.50 ±0.10	.020 ±.004
L	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.002}$
M	0.25	.010







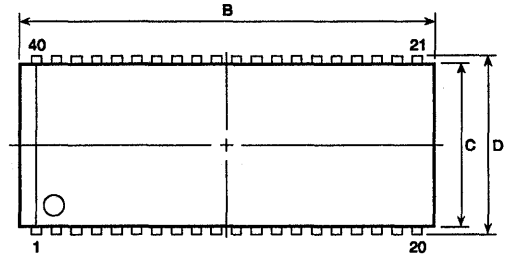
P40C-100-600A

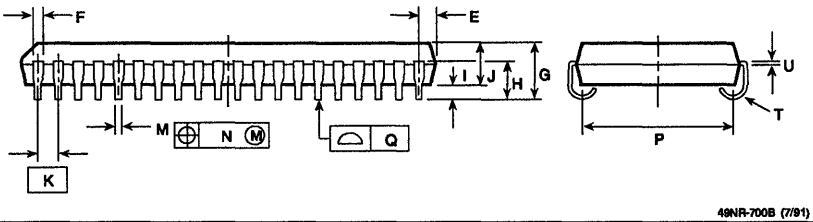
83vQ-61408 (6/89)

40-Pin Plastic SOJ (400-mil)

Item	Millimeters	Inches
B	26.29 $^{+.02}_{-.035}$	1.035 $^{+.008}_{-.014}$
C	10.16	.400
D	11.18 ± 0.2	.440 ± .008
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.7	.028
G	3.5 ± 0.2	.138 ± .008
H	2.4 ± 0.2	.094 $^{+.007}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P *	9.40 ± 0.20	.370 ± .008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



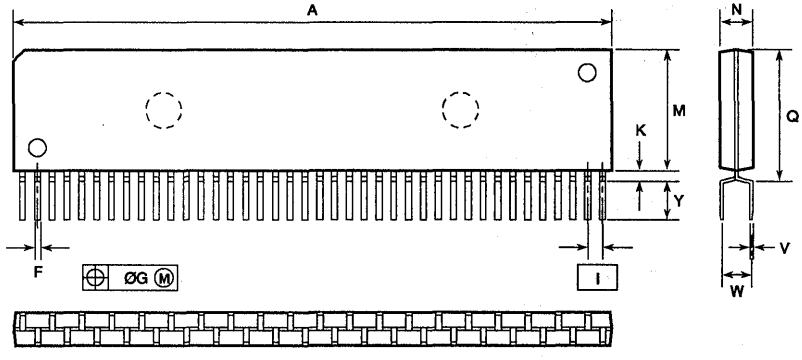


P40LE-400A

49NR-700B (7/91)

40-Pin Plastic ZIP (400-mil)

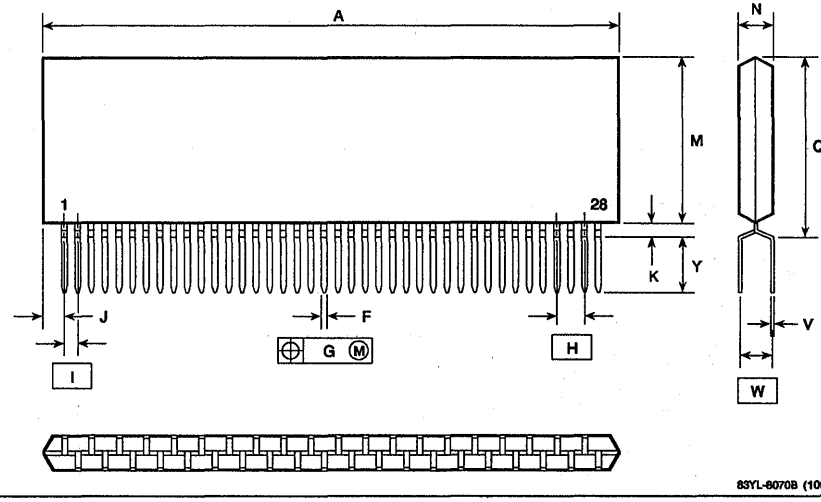
Item	Millimeters	Inches
A	$50.98^{+0.05}_{-0.35}$	$2.007^{+0.002}_{-0.014}$
F	14.0 ± 0.2	0.20 ± 0.002
G	Ø0.25	Ø0.010
I	1.27 ± 0.1	0.050 ± 0.004
K	0.9 min	0.035 min
M	10.29 ± 0.05	0.405 ± 0.002
N	2.8 ± 0.05	0.110 ± 0.002
Q	11.5 ± 0.15	0.453 ± 0.006
V	$.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$
W	2.50 ± 0.1	0.098 ± .004
Y	3.25 ± 0.15	0.128 ± .006



83RD-7780B (5/91)

40-Pin Plastic Shrink ZIP (450-mil)

Item	Millimeters	Inches
A	36.83 max	1.450 max
F	0.4 ± 0.1	.016 ± .004
G	0.2	.008
H	1.778	.070
I	0.889	.035
J	1.016	.040
K	1.0 min	.039 min
M	10.50 max	.413 max
N	2.2 ± 0.2	.087 ± .008
Q	11.70 max	.461 max
V	$0.25^{+0.10}_{-0.05}$	$.010^{+.004}_{-.002}$
W	1.778	.070
Y	3.108	.122

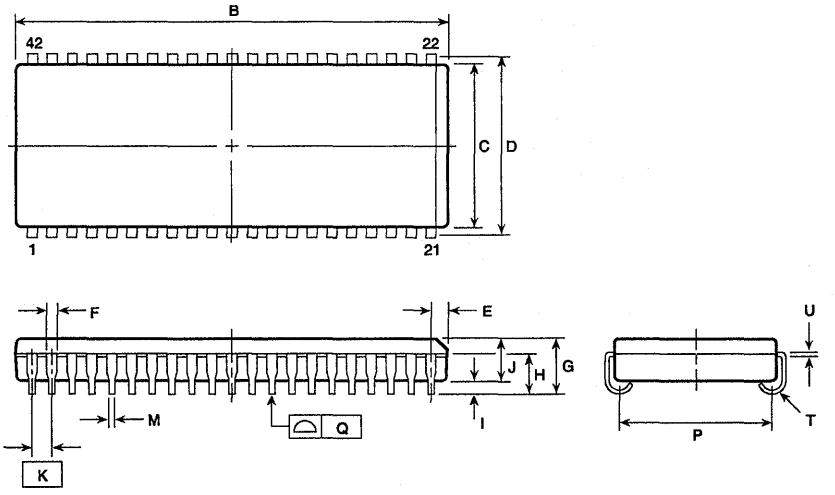


83YL-8070B (1091)

42-Pin Plastic SOJ (400-mil)

Item	Millimeters	Inches
B	27.41 $^{+0.20}_{-0.35}$	1.08 $^{+.008}_{-.014}$
C	10.16	.400
D	11.18 ± 0.20	.440 ± .008
E	1.08 ± 0.15	.043 ± .006
F	0.6	.024
G	3.5 ± 0.20	.138 ± .008
H	2.545 ± 0.2	.100 ± .008
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 ± .004
P*	9.40 ± 0.20	.370 ± .008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.

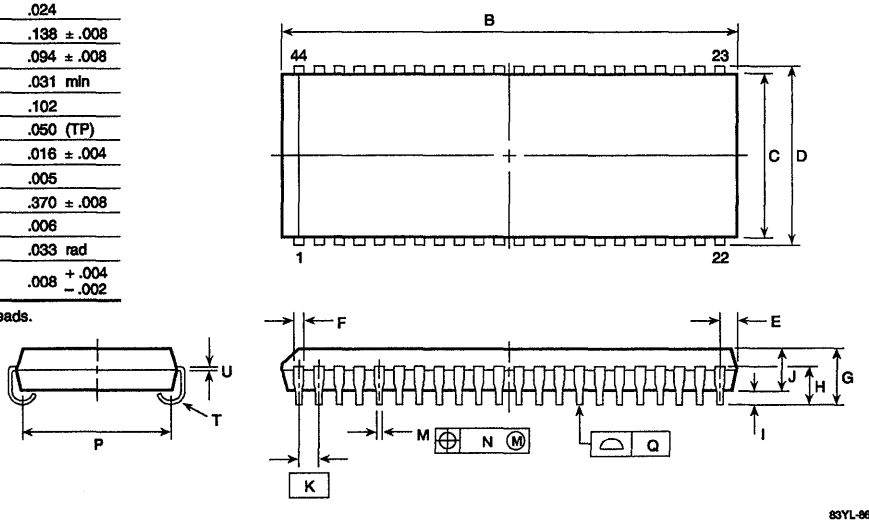


83YL-9024B (9/92)

44-Pin Plastic SOJ (400-mil)

Item	Millimeters	Inches
B	28.83 $^{+0.20}_{-0.35}$	1.135 $^{+.008}_{-.014}$
C	10.16	.400
D	11.18 ± 0.2	.440 ± .008
E	1.08 ± 0.15	.043 ± .006
F	0.6	.024
G	3.5 ± 0.2	.138 ± .008
H	2.4 ± 0.2	.094 ± .008
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 ± .004
N	0.12	.005
P*	9.40 ± 0.20	.370 ± .008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



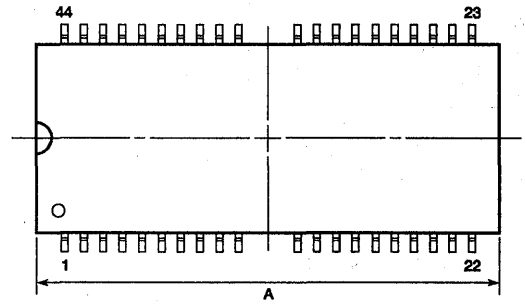
83YL-8649B (5/92)

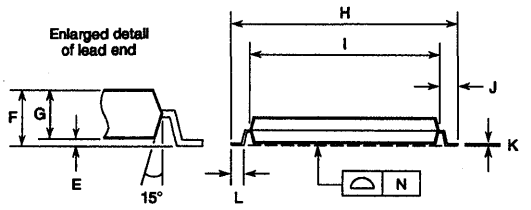
16

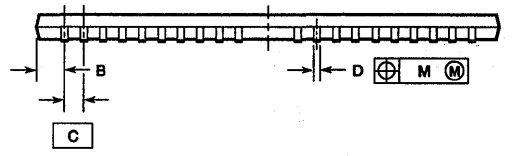
NEC

44/40-Pin Plastic TSOP II (300-mil)

Item	Millimeters	Inches
A	18.81 max	.741 max
B	1.04 max	.041 max
C	0.8 typ.	.031 typ.
D	0.3 ± 0.1	.012 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.13 max	.044
G	1.0 typ.	.039
H	9.22 ± 0.2	.363 ± .008
I	7.62 ± 0.2	.300 ± .008
J	0.8 ± 0.2	.031 ± .008
K	$0.14^{+0.1}_{-0.05}$	$.006^{+.004}_{-.002}$
L	0.5 ± 0.1	.020 ± .004
M	0.21	.008
N	0.1	.004



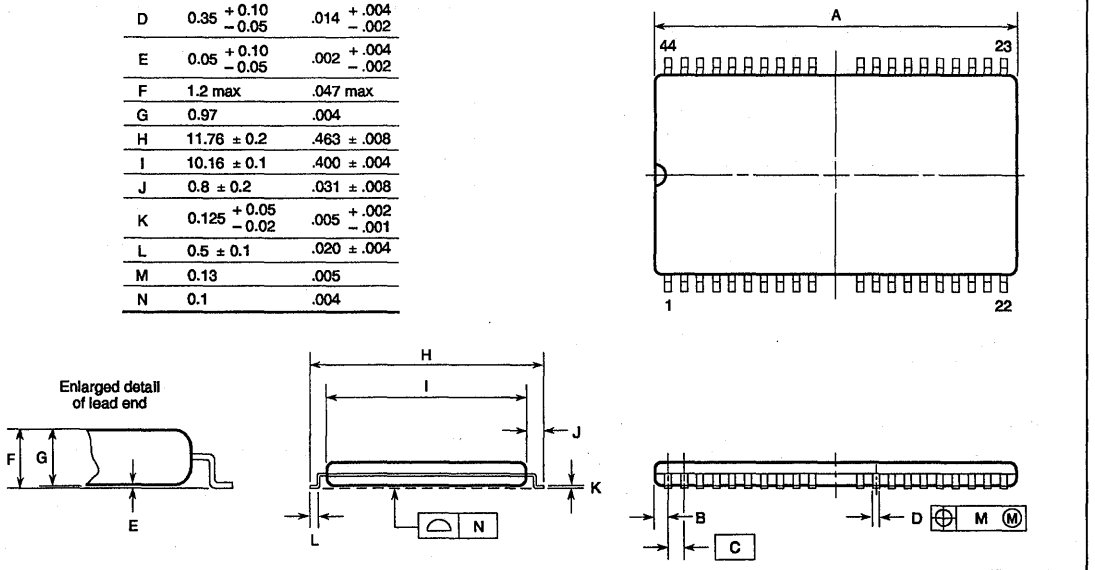




83YL-7697B (2/92)

44-Pin Plastic TSOP II (400-mil) #1

Item	Millimeters	Inches
A	18.41 ± 0.1	.725 ± .004
B	1.0 max	.039 max
C	0.8 ± 0.1	.031 ± .004
D	$0.35^{+0.10}_{-0.05}$	$.014^{+.004}_{-.002}$
E	$0.05^{+0.10}_{-0.05}$	$.002^{+.004}_{-.002}$
F	1.2 max	.047 max
G	0.97	.004
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	$0.125^{+0.05}_{-0.02}$	$.005^{+.002}_{-.001}$
L	0.5 ± 0.1	.020 ± .004
M	0.13	.005
N	0.1	.004

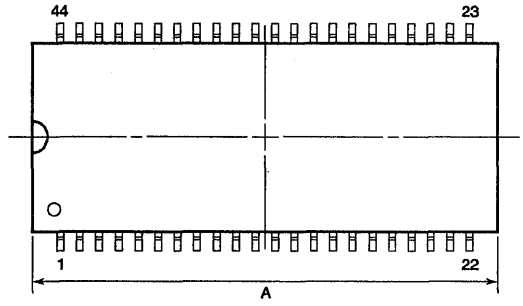


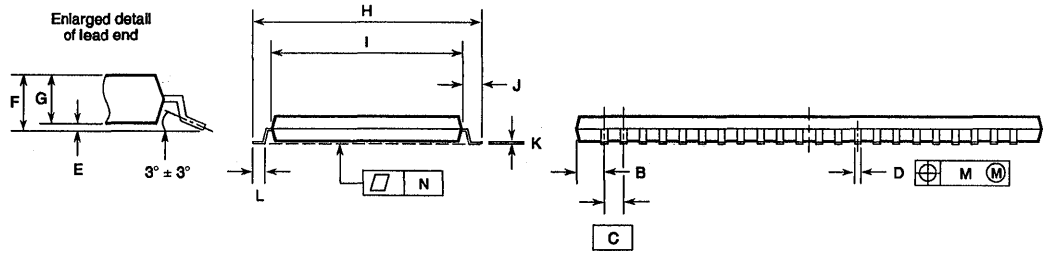
83YL-8069B (10/91)

16

44-Pin Plastic TSOP II (400-mil) #2

Item	Millimeters	Inches
A	18.81 max	.741 max
B	1.00 max	.039 max
C	0.8 (TP)	.031 (TP)
D	0.30 ± 0.10	.012 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.043
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	.020 ± .004
M	0.13	.005
N	0.1	.004

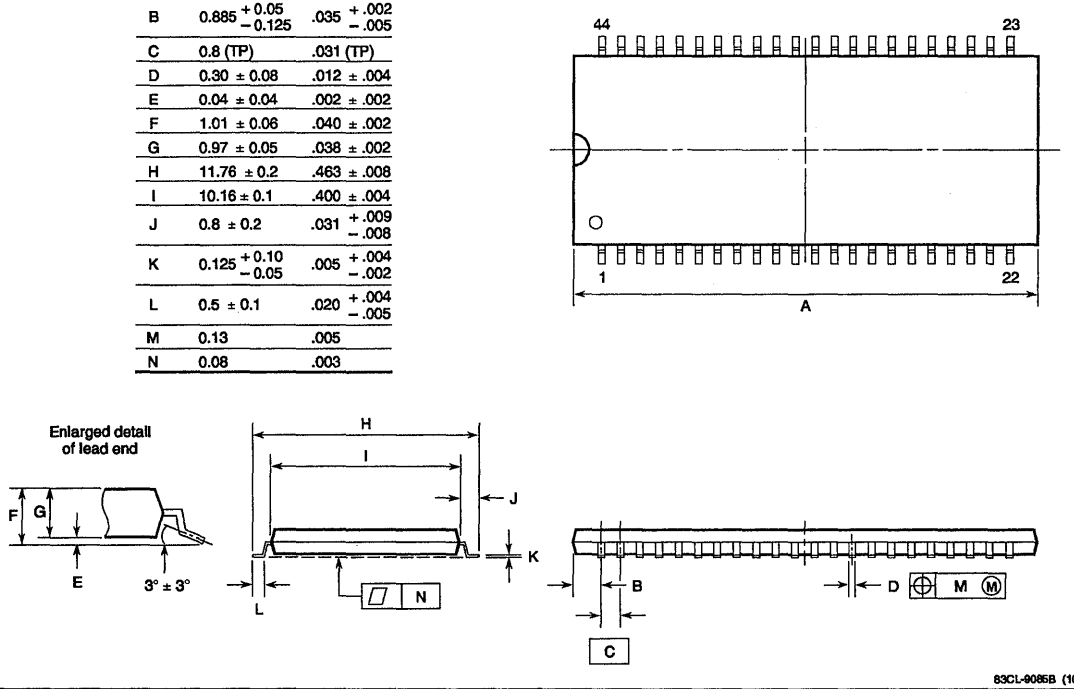




83CL-9080B (9/92)

44-Pin Plastic TSOP II (400-mil) #3

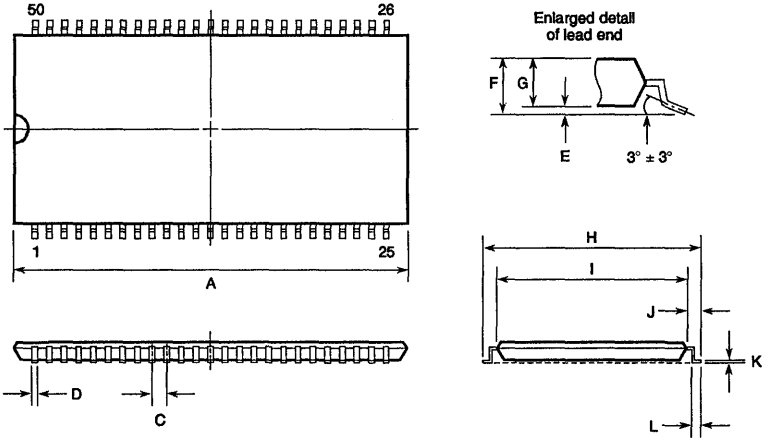
Item	Millimeters	Inches
A	18.37 ± 0.05	.723 ± .002
B	$0.885^{+0.05}_{-0.125}$	$.035^{+.002}_{-.005}$
C	0.8 (TP)	.031 (TP)
D	0.30 ± 0.08	.012 ± .004
E	0.04 ± 0.04	.002 ± .002
F	1.01 ± 0.06	.040 ± .002
G	0.97 ± 0.05	.038 ± .002
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	$.031^{+.009}_{-.008}$
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	$.020^{+.004}_{-.005}$
M	0.13	.005
N	0.08	.003



83CL-9085B (10/92)

50-Pin Plastic TSOP II (400-mil)

Item	Millimeters	Inches
A	21.11 ± .05	.831 ± .002
C	0.8 ± 0.05	.031 ± .002
D	0.3 ± 0.08	.012 ± .003
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.043 max
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	$.020^{+.004}_{-.005}$

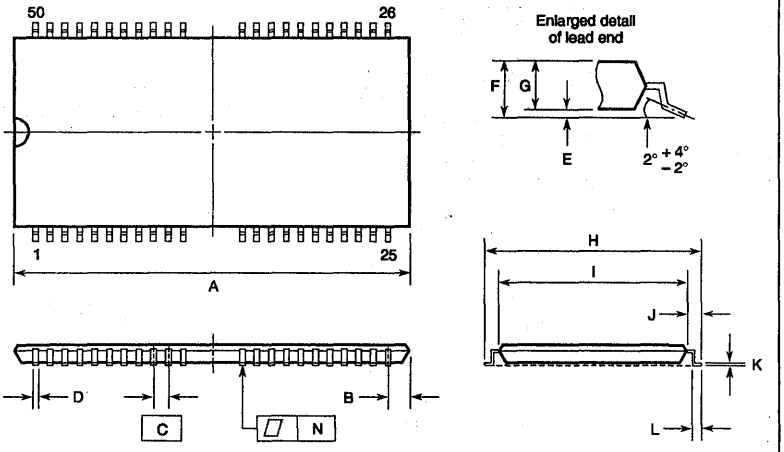


83CL-9081B (9/92)

16

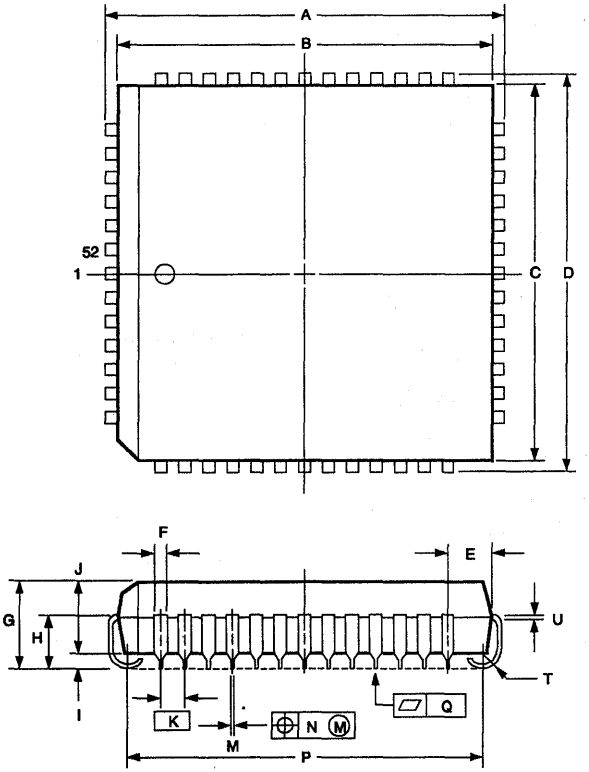
50/44-Pin Plastic TSOP II (400-mil)

Item	Millimeters	Inches
A	21.45 max	.844 max
B	1.06 max	.042 max
C	0.8 (TP)	.031 (TP)
D	0.30 ± 0.10	.012 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.043 max
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	$.020^{+.004}_{-.005}$
N	0.10	.004



52-Pin Plastic LCC

Item	Millimeters	Inches
A	20.1 ±0.2	.791 ±.008
B	19.12	.753
C	19.12	.753
D	20.1 ±0.2	.791 ±.008
E	1.94 ±0.15	.076 ±.006
F	0.6	.024
G	4.4 ±0.2	.173 ±.008
H	2.8 ±0.2	.110 ±.008
I	0.9 min	.035 min
J	3.4	.134
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 ±.004
N	0.12	.005
P	18.04 ±0.20	.710 ±.008
Q	0.15	.006
T	0.8 radius	.031 radius
U	$0.20^{+0.10}_{-0.05}$	$.008^{+.004}_{-.002}$



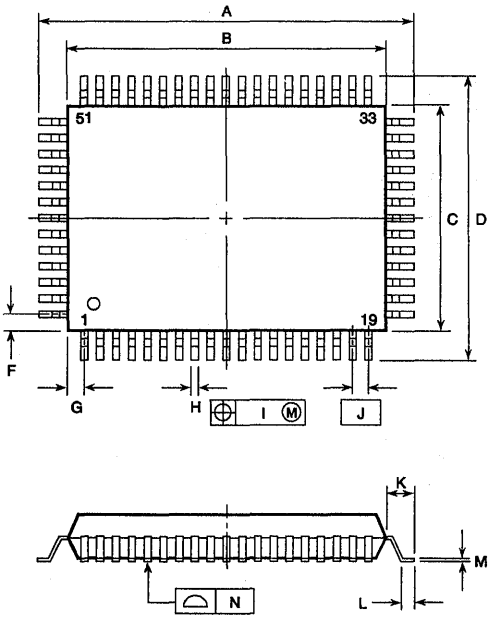
P52L-50A1

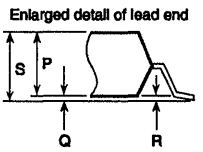
83YL-5805B

16

64-Pin Plastic QFP

Item	Millimeters	Inches
A	23.6 ± 0.4	.929 ± .016
B	20.0 ± 0.2	.795 $^{+.009}_{-.008}$
C	14.0 ± 0.2	.551 $^{+.009}_{-.008}$
D	17.6 ± 0.4	.693 ± .016
F	1.0	.039
G	1.0	.039
H	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
I	0.20	.008
J	1.0 (TP)	.039 (TP)
K	1.8 ± 0.2	.071 $^{+.008}_{-.009}$
L	0.8 ± 0.2	.031 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
N	0.15	.006
P	2.7	.106
Q	0.1 ± 0.1	.004 ± .004
R	0.1 ± 0.1	.004 ± .004
S	3.0 max	.119 max



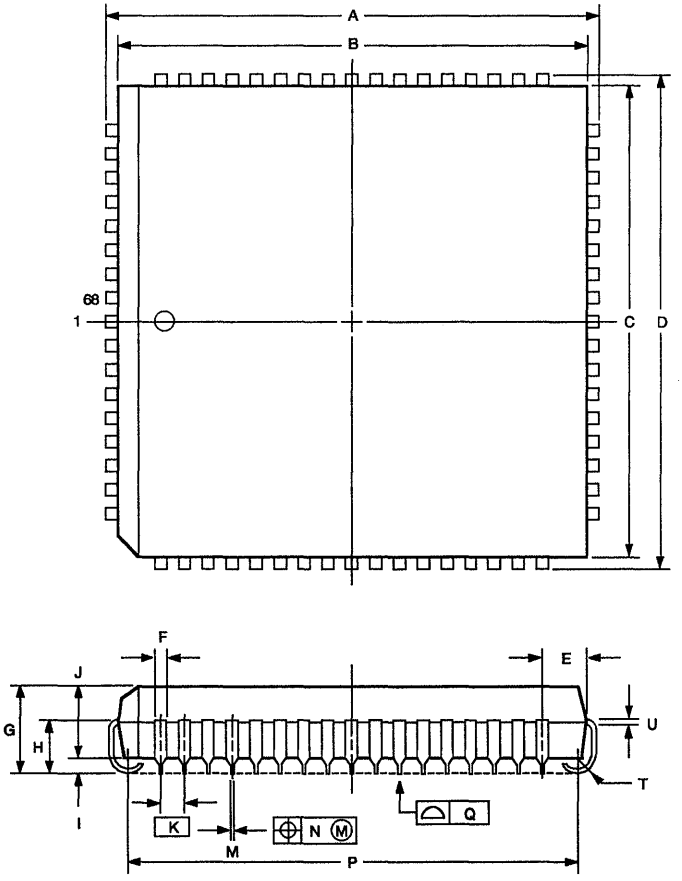


P64GF-100-3B8, 3BE-1

49NR-699B (6/91)

68-Pin Plastic LCC

Item	Millimeters	Inches
A	25.2 ±0.2	.992 ±.008
B	24.20	.953
C	24.20	.953
D	25.2 ±0.2	.992 ±.008
E	1.94 ±0.15	.076 $^{+.007}_{-.006}$
F	0.6	.024
G	4.4 ±0.2	.173 $^{+.009}_{-.008}$
H	2.8 ±0.2	.110 $^{+.009}_{-.008}$
I	0.9 min	.035 min
J	3.4	.134
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P	23.12 ±0.20	.910 $^{+.009}_{-.008}$
Q	0.15	.006
T	0.8 radius	.031 radius
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$



P68L-50A1-1

(2/90)

83YL-6561B

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