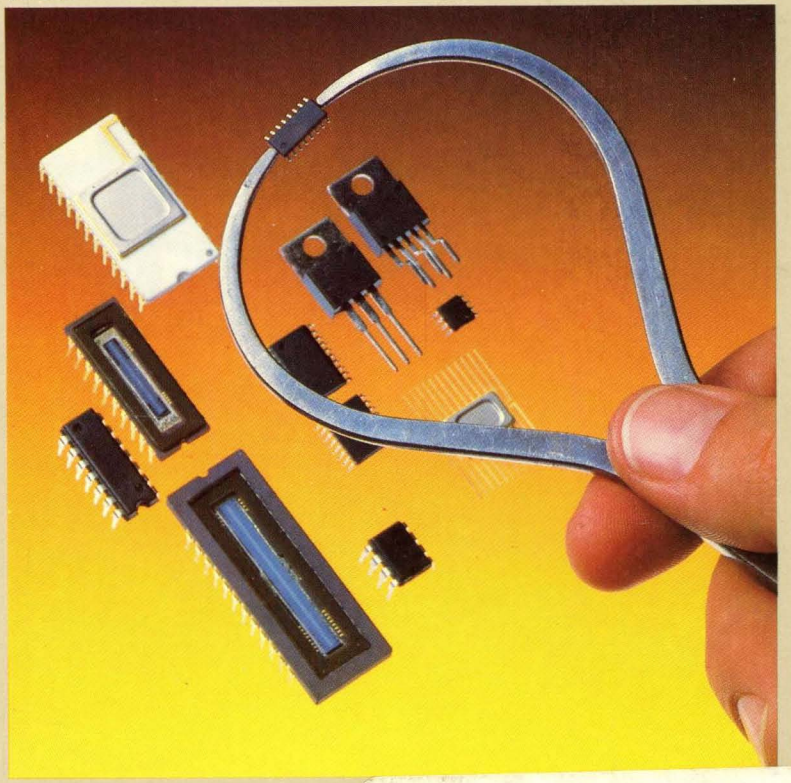
NEC Electronics Inc.

NEC

LINEAR PRODUCTS

1986 DATA BOOK



NEC Electronics Inc.

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1986 LINEAR DATA BOOK

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GENERAL INFORMATION

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Section 1 — General Information

Introduction

NEC's Linear Catalog illustrates the extensive line of components available to designers and manufacturers. The variety of devices allows greater design alternatives and the ability to choose parts that truly fit your product needs. NEC's components are designed to satisfy industrial, communication, instrumentation, and consumer applications.

Designed for easy reference, NEC's Linear Catalog is divided into the following sections.

General Information - This section includes product selection guides, cross reference, ordering information, and handling precautions.

Quality and Reliability - An explanation and detailed specifications of NEC's stringent Q&R product testing.

Operational Amplifiers - Popular second-source operational amplifiers, and state-of-the-art J-FET input originals, complement a complete line of op-amps. Most are available in surface mount packaging.

Voltage Comparators - Some of the most popular comparators are available in either DIP or surface mount packaging.

A/D-D/A Converters - A full line of D/A converters are available with 6-, 8-, 10-, and 12- bits; also, 8- and 10-bit CMOS A/D converters with full microprocessing capabilities.

Voltage Regulators - All standard 3-terminal regulators are available in the 7800 and 7900 series, as well as the μPC305 DIP.

Functional Blocks - A wide variety of special products are offered including, SMPS controllers, timers, precision voltage references, and Charge Coupled Devices (CCD Sensors).

Ordering Information

NEC integrated circuits may be ordered by contacting either the local NEC sales office, representative, or authorized distributor.

Numbering System

μPC 1234 C

- C — Package
  - B — Ceramic flatpack
  - C — Plastic molded DIP
  - D — Ceramic DIP/CERDIP
  - G2 — Plastic miniflat
  - H — TO-220
  - HA — Plastic SIP
  - J — TO-92
- 1234 — Device Number
- μPC — Product Family
  - μPC — Bipolar Linear Circuits
  - μPD — MOS Circuits

Temperature Range

Operating Temperature	High Reliability Industrial	Commercial
Ceramic Flatpack		0°C to 70°C
Plastic DIP	−40°C to +85°C*	−20°C to +70°C
Ceramic DIP	−40°C to +85°C*	−20°C to +70°C
Plastic Miniflat	−40°C to +85°C*	0°C to +70°C
TO-220	−40°C to +85°C*	−20°C to +85°C
Plastic SIP	−40°C to +85°C*	−20°C to +80°C
TO-92	−40°C to +85°C*	−20°C to +85°C

Storage Temperature	High Reliability Industrial	Commercial
Ceramic Flatpack		−65°C to +150°C
Plastic DIP	−55°C to +125°C	−55°C to +125°C
Ceramic DIP	−55°C to +150°C	
Plastic Miniflat	−55°C to +125°C	−55°C to +125°C
TO-220		−55°C to +150°C
Plastic SIP		−55°C to +125°C
TO-92		−65°C to +150°C

*Available For Most Linear Devices.

Selection Guide

Operational Amplifiers

Temperature Range: C Package (plastic molded DIP) 0°C to +70°C
G2 Package (plastic molded SO) 0°C to +70°C
D Package (ceramic cavity DIP) −20°C to +80°C

*Unless otherwise specified, $V^{\pm} = \pm 15$ V, $T_A = 25°C$

NEC No.	Package	Generic	V_{CC}[1] (+/−V) Rec.	I_{CC} (mA) Max.	V_{io} (mV) Max.	I_{io} (nA) Max.	I_b (nA) Max.	A_{VOL} (dB) Min.	e_n^2 (nV/√Hz) Typ.	f_{UNITY} (MHz) Typ.	Slew Rate (V/μs) Typ.
Single Operational Amplifiers											
μPC301A	C/8	LM301A	5-16	3	7.5	50	250	88	25	prog	prog
μPC318	C/8	LM318	5-16	10	10	200	500	88	15	10	70
μPC356	C/8	LF356	5-16	10	5	0.05	0.2	88	20	5	12
μPC357	C/8	LF357	5-16	10	5	0.05	0.2	88	20	20 ($A_V \geq 5$) (GBW at 10 kHz)	50 ($A_V \geq 5$)
μPC741	C/8 G2/8	μA741	7-16	2.8	6	200	500	88	25	0.6	0.5
μPC811[3]	C/8 G2/8	LF411	5-16	3.5	2.5	0.05	0.2	88	20	4	15
μPC813[3]	C/8 G2/8	LF412	5-16	3.5	2.5	0.05	0.2	88	20	8	25
μPC4061[3]	C/8 G2/8	TL061	2-16	0.25	10	0.05	0.1	69	30	1	3
μPC4071	C/8 G2/8	TL071	5-16	2.7	10	0.05	0.2	88	18	3	13
μPC4081	C/8 G2/8	TL081	5-16	2.8	15	0.1	0.4	88	25	3	13
μPC4250	C/8 G2/8	LM4250	1-16	prog	6	prog	prog	96	25	prog	prog

Notes: 1. Recommended supply voltage range.
2. Input equivalent noise density at 1 kHz ($R_S = 100\ \Omega$).
3. New product (Preliminary data).

Operational Amplifiers (cont)

Temperature Range: C Package (plastic molded DIP) 0°C to +70°C
G2 Package (plastic molded SO) 0°C to +70°C
D Package (ceramic cavity DIP) −20°C to +80°C
*Unless otherwise specified, $V^{\pm} = \pm 15$ V, $T_A = 25°C$

NEC No.	Package	Generic	V_{CC}[1] (+/−V) Rec.	I_{CC} (mA) Max.	V_{io} (mV) Max.	I_{io} (nA) Max.	I_b (nA) Max.	A_{VOL} (dB) Min.	e_n^2 (nV/√Hz) Typ.	f_{UNITY} (MHz) Typ.	Slew Rate (V/μs) Typ.
Dual Operational Amplifiers											
μPC358	C/8 G2/8	LM358	3-30 (Single Supply)	1.2	7.0	50	250	88	32	0.5	0.2
*Specified at $V^{\pm} = +5$ V.											
μPC812[3]	C/8, G2/8	ORIG	5-16	6.8	3.0	0.05	0.2	88	20	4	15
μPC814[3]	C/8	ORIG	5-16	6.8	3.0	0.05	0.2	88	20	8	25
μPC1458	C/8 G2/8	MC1458	7-16	5.6	6	200	500	88	25	0.6	0.5
μPC4062[3]	C/8 G2/8	TL062	2-16	0.50	10	0.05	0.1	69	30	1	3
μPC4072	C/8 G2/8	TL072	5-16	5.0	10	0.05	0.2	88	18	3	13
μPC4082	C/8 G2/8	TL082	5-16	5.6	15	0.1	0.4	88	25	3	13
μPC4359	C/14	LM339	5-22	22	—	—	1500	70	—	15	60
μPC4556	C/8 G2/8	ORIG	4-16	5.6	6.0	200	500	86	12	20 ($A_V \geq 10$) (GBW at 10 kHz)	5.0 ($A_V \geq 10$)
μPC4557	C/8	ORIG	4-16	5.6	6.0	200	500	86	12	2	1
μPC4558	C/8 G2/8	RC4558	4-16	5.6	6.0	200	500	86	12	2	1
μPC4559	C/8	RC4559	4-16	5.6	6.0	200	500	86	12	3	2
μPC4560	C/8 G2/8	ORIG	4-16	5.6	6.0	200	500	86	7	10 (GBW at 10 kHz)	2.8
μPC4570[3]	C/8 G2/8	ORIG	4-16	8.0	5.0	200	1000	90	4.5	15 (GBW at 10 kHz)	7

Notes: 1. Recommended supply voltage range.
2. Input equivalent noise density at 1 kHz ($R_S = 100\ \Omega$).
3. New product (Preliminary data).

Operational Amplifiers (cont)

Temperature Range: C Package (plastic molded DIP) 0°C to +70°C
G2 Package (plastic molded SO) 0°C to +70°C
D Package (ceramic cavity DIP) −20°C to +80°C

*Unless otherwise specified, $V^{\pm} = \pm 15$ V, $T_A = 25°C$

NEC No.	Package	Generic	V_{CC}[1] (+/−V) Rec.	I_{CC} (mA) Max.	V_{io} (mV) Max.	I_{io} (nA) Max.	I_b (nA) Max.	A_{VOL} (dB) Min.	e_n^2 (nV/√Hz) Typ.	f_{UNITY} (MHz) Typ.	Slew Rate (V/μs) Typ.
Quad Operational Amplifiers											
μPC324	C/14 G2/14	LM324	3-30 (Single Supply)	2.0	7.0	50	250	88	32	0.5	0.25
*Specified at $V^{\pm} = +5$ V.											
μPC3403	C/14 G2/14	MC3403	3-32 (Single Supply)	7.0	7.0	50	250	88	32	1	0.6
*Specified at $V^{\pm} = +5$ V.											
μPC4064	C/14 G2/14	TL064	2-16	1.0	10	0.05	0.1	69	30	1	3
μPC4074	C/14 G2/14	TL074	5-16	10.0	10	0.05	0.2	88	18	3	13
μPC4084	C/14	TL084	5-16	10.0	15	0.2	0.4	88	25	3	13
μPC4574	C/14 G2/14	ORIG	±15	12	5	200	1000	90	5	7	6
μPC4741	C/14 G2/14	HA4741	2-16	7.0	5.0	50	300	88	10	3	1.6

Notes: 1. Recommended supply voltage range.
2. Input equivalent noise density at 1 kHz ($R_S = 100\ \Omega$).
3. New product (preliminary data).

Comparators

Temperature Range: C Package 0°C to +70°C
G2 Package (plastic molded SO) 0°C to +70°C
*Unless otherwise specified, $V^{\pm} = \pm 15$ V, $T_A = 25°C$

NEC No.	Package	Generic	V_{CC}[1] (+/−V)	I_{CC} Max. (mA)	V_{io} Max. (mV)	I_{io} Max. (nA)	I_b Max. (nA)	A_{VOL} Typ. (dB)	I_{SINK}[2] Typ. (mA)	Response Time[3] (ns)
μPC311 (Single)	C/8 G2/8	LM311	4-18 5-36 (Single Supply)	7.5	7.5	50	250	106	8.0	200
μPC319 (Dual)	C/14 G2/14	LM319	5-18 5-18 (Single Supply)	12.5	8.0	200	1000	92	3.2	80
μPC339 (Quad)	C/14 G2/14	LM339	2-32 (Single Supply)	2.0	5.0	50	250	106	4.0	1300
*Specified at $V^+ = +5$ V.										
μPC393 (Dual)	C/8 G2/8	LM393	2-32 (Single Supply)	1.0	5.0	50	250	106	4.0	1300
*Specified at $V^+ = +5$ V.										

Notes: 1. Recommended supply voltage range.
2. $V^+ = +5$ V, $V_{OL} = 0.4$ V.
3. 100 mV input step with 5 mV overdrive.

Voltage Regulators

Device	Original	Operating Temperature Range (°C)	V_{OUT} (V)	V_{IN} (V)		I_O Max. (A)	P_T Max. (W)	Package
				Min.	Max.			
μPC305C	305	0~+70	4.5~30	8.0	40	0.05	0.35	8 pin DIP
μPC317	LM317	−20~+80	+1.3~+30	4.3	40	1.5	20	TO-220
μPC337	LM337	−20~+80	−1.3~−30	4.3	40	1.5	20	TO-220
μPC2600	—	−30~+85	5, 10	12	28	0.5	20	TO-220
μPC78L05J	78L05	−20~+150[1]	5[2]	7	30	0.1	0.8	TO-92
μPC78L08J	78L08	−20~+150[1]	8[2]	10.5	30	0.1	0.8	TO-92
μPC78L12J	78L12	−20~+150[1]	12[2]	14.5	35	0.1	0.8	TO-92
μPC78L15J	78L15	−20~+150[1]	15[2]	17.5	35	0.1	0.8	TO-92
μPC78M05	78M05	−20~+80	5[3]	7	35	0.5	20	TO-220
μPC78M08	78M05	−20~+80	8[3]	10.5	35	0.5	20	TO-220
μPC78M10	—	−20~+80	10[3]	12.5	35	0.5	20	TO-220
μPC78M12	78M12	−20~+80	12[3]	14.5	35	0.5	20	TO-220
μPC78M15	78M15	−20~+80	15[3]	17.5	35	0.5	20	TO-220
μPC78M18	78M18	−20~+80	18[3]	21	35	0.5	20	TO-220
μPC78M24	78M24	−20~+80	24[3]	27	40	0.5	20	TO-220
μPC7805	7805	−20~+80	5[3]	7	35	1.0	20	TO-220
μPC7808	7808	−20~+80	8[3]	10.5	35	1.0	20	TO-220
μPC7812	7812	−20~+80	12[3]	14.5	35	1.0	20	TO-220
μPC7815	7815	−20~+80	15[3]	17.5	35	1.0	20	TO-220
μPC7818	7818	−20~+80	18[3]	21	35	1.0	20	TO-220
μPC7824	7824	−20~+80	24[3]	27	40	1.0	20	TO-220
μPC79L05	7905	−20~+125[1]	−5[3]	−7	−20	0.07	0.7	TO-92
μPC79L08	7908	−20~+125[1]	−8[3]	−10.5	−23	0.07	0.7	TO-92
μPC79L12	7912	−20~+125[1]	−12[3]	−14.5	−27	0.07	0.7	TO-92
μPC79L15	7915	−20~+125[1]	−15[3]	−17.5	−30	0.07	0.7	TO-92
μPC79M05	7905	−20~+150[1]	−5[3]	−7	−25	0.35	20	TO-220
μPC79M08	7908	−20~+150[1]	−8[3]	−10.5	−25	0.35	20	TO-220
μPC79M12	7912	−20~+150[1]	−12[3]	−14.5	−30	0.35	20	TO-220
μPC79M18	7918	−20~+150[1]	−18[3]	−17.5	−30	0.35	20	TO-220
μPC79M24	7924	−20~+150[1]	−24[3]	−27	−38	0.35	20	TO-220
μPC7905	7905	−20~+80	−5[3]	−7	−35	1.0	20	TO-220
μPC7908	7908	−20~+80	−8[3]	−10.5	−35	1.0	20	TO-220
μPC7912	7912	−20~+80	−12[3]	−14.5	−35	1.0	20	TO-220
μPC7915	7915	−20~+80	−15[3]	−17.5	−35	1.0	20	TO-220
μPC7918	7918	−20~+80	−18[3]	−21	−35	1.0	20	TO-220
μPC7924	7924	−20~+80	−24[3]	−27	−40	1.0	20	TO-220

Notes: 1. Junction temperature.
2. Output voltage accuracy ±10%.
3. Output voltage accuracy ±5%.

Digital to Analog Converters

Part No.	Resolution	Non-Linearity	Conversion Speed	Supply Voltage	Features
μPC603	6 Bit	0.4%	3 μs	±15	Onboard V_{REF} — Output Buffer
μPC610	10 Bit	0.2%	6 μs	±15	Onboard V_{REF} — Output Buffer
μPC624	8 Bit	0.19%	150 ns	±5 ±15	Current Output
μPC6012	12 Bit	0.05%	400 ns	+5-+15 −12/−15	Current Output
μPC6900	8 Bit	1/2 LSB	20 x 10^6 samples/sec	+5	Current Output
μPD7011 μPD7011C-1	8 Bit	0.4% 0.2%	3 μs	+5	Current Output

Analog to Digital Converters

Part No.	Resolution	Non-Linearity	Conversion Speed	Supply Voltage	Output
μPC650	12 Bit	0.05%	45 μs	+5 −15	Parallel Output
μPC6950	8 Bit	±1/2 LSB	20 x 10^6 samples/sec	+5	Parallel Output
μPD7001	8 Bit	0.8%	140 μs	+5	Serial Output
μPD7002 μPD7002C-1	10 Bit	0.2% 0.1%	15 ms	+5	Three State Output
μPD7003	8 Bit	0.49%	4 μs	+5	Three State Output
μPD7004	10 Bit	0.15%	104 μs	+5	Serial/Parallel

Functional Blocks*

Device No.	Description
μPC398	Monolithic Sample and hold circuit
μPC494	Switching regulator (SMPS) controller
μPC751	Quad read/write amp for hard disk media
μPC752	Quad addressable read/write amplifier
μPC754	Magnetic servo head preamp
μPC1042	Switching regulator (SMPS) controller
μPC1060	2.5 V precision voltage reference, for use with D/A and A/D converters
μPC1555	Precision Timer (NE 555 direct replacement)
μPC3423	Overvoltage "Crowbar" sensing circuit
μPD5555/5556	CMOS 555 Timers

*Contact manufacturer for specifications.

Charge Coupled Devices (CCD Sensors)

Device No.	Description
μPD791D	4096 Bit Array
μPD795D	1024 Bit Array
μPD799D	2048 Bit Array

Part Number Index

Part Number Index (cont)

Industry Cross Reference

AMD	NEC
AM 6012	μPC6012
DAC 08	μPC624

Fairchild	NEC
UA 1458	μPC1458
UA 301A	μPC301A
UA 305	μPC305
UA 311	μPC311
UA 324	μPC324
UA 339	μPC339
LM 358	μPC358
UA 393	μPC393
UA 398	μPC398
UA 4558	μPC4558
UA 494	μPC494
UA 555	μPC1555
UA 733	μPC1663
UA 741	μPC741
UA 78XX	μPC78XX
UA 78LXX	μPC78LXX
UA 78MXX	μPC78MXX
UA 79XX	μPC79XX
UA 79LXX	μPC79LXX
UA 79MXX	μPC79MXX

Intersil	NEC
ICM 7555	μPD5555
ICM 7556	μPD5556

Motorola	NEC
DAC 08	μPC624
TL 071	μPC4071
TL 072	μPC4072
TL 074	μPC4074
TL 081	μPC4081
TL 082	μPC4082
TL 084	μPC4084
MC 1403	μPC1060
MC 1408-8	μPC624
MC 1455	μPC1555
MC 1458	μPC1458

Motorola (cont)	NEC
UA 301A	μPC301A
LM 305	μPC305
LM 311	μPC311
LM 317	μPC311
LM 324	μPC324
LM 339	μPC339
MC 3403	μPC3403
MC 34072	μPC842*
MC 34074	μPC844*
LM 358	μPC358
MC 4558	μPC4558
MC 4741	μPC4741
LM 741	μPC741
MC 78XX	μPC78XX
MC 78LXX	μPC78LXX
MC 78MXX	μPC78MXX
MC 79XX	μPC79XX

National	NEC
DAC 08	μPC624
LM 1458	μPC1458
LM 2930	μPC2250
LM 301A	μPC301A
LM 305	μPC305
LM 311	μPC311
LM 317	μPC317
LM 319	μPC319
LM 320TX	μPC79XX
LM 324	μPC324
LM 337	μPC337
LM 339	μPC339
LM 340T	μPC78XX
LF 356	μPC356
LM 358	μPC358
LM 359	μPC4359
LM 393	μPC393
LM 398	μPC398
LF 411	μPC811
LF 412	μPC812
LM 4250	μPC4250
LM 555	μPC1555

*New product - Data available May 86

Industry Cross Reference (cont)

National (cont)	NEC
LM 741	μPC741
LM 78XX	μPC78XX
LM 78LXX	μPC78LXX
LM 78MXX	μPC78MXX
LM 79XX	μPC79XX

PMI	NEC
DAC 01C	μPC603
DAC 02	μPC610
DAC 08	μPC624

RCA	NEC
CA 081	μPC4081
CA 082	μPC4082
CA 084	μPC4084
CA 1458	μPC1458
CA 301A	μPC301A
CA 311	μPC311
CA 324	μPC324
CA 339	μPC339
CA 358	μPC358
CA 393	μPC393
CA 555	μPC1555
CA 741	μPC741

SGS	NEC
MC 1458	μPC1458
L 2605	μPC2605
L 2610	μPC2610
LS 301A	μPC301A
LM 317	μPC317
LM 324	μPC324
LM 339	μPC339
LM 358	μPC358
LM 393	μPC393
LS 4558	μPC4558
NE 555	μPC1555
NE 571	μPC1571
LM 741	μPC741

SGS (cont)	NEC
L 78XX	μPC78XX
L 78MXX	μPC78MXX
L 79XX	μPC79XX

Signetics	NEC
AM 6012	μPC6012
DAC 08	μPC624
MC 1408-8	μPC624
MC 1458	μPC1458
LM 311	μPC311
LM 319	μPC319
LM 324	μPC324
LM 339	μPC339
MC 3403	μPC3403
LM 393	μPC393
LF 398	μPC398
NE 4558	μPC4558
NE 555	μPC1555
NE 5532	μPC4570
UA 741	μPC741

Texas Inst.	NEC
TL 061	μPC4061
TL 062	μPC4062
TL 064	μPC4064
TL 071	μPC4071
TL 072	μPC4072
TL 074	μPC4074
TL 081	μPC4081
TL 082	μPC4082
TL 084	μPC4084
TL 431	μPC1093
MC 1458	μPC1458
LM 301A	μPC301A
LM 311	μPC311
LM 319	μPC319
LM 324	μPC324
LM 339	μPC339
LM 358	μPC358
LM 393	μPC393
RC 4558	μPC4558
RC 4559	μPC4559

Industry Cross Reference (cont)

Texas Inst. (cont)	NEC
TL 494	μPC494
NE 555	μPC1555
UA 741	μPC741
UA 78XX	μPC78XX
UA 78LXX	μPC78LXX
UA 78MXX	μPC78MXX
UA 79XX	μPC79XX
UA 79LXX	μPC79LXX
UA 79MXX	μPC79MXX

Full Product Line Guide

SINGLE OP AMPS

Part No.	Package	Description
μPC301A	C - 8 pin	General Purpose OP Amp
μPC318	C - 8 pin	High Speed Op Amp
μPC356	C - 8 pin	J-FET Input Op Amp
μPC357	C - 8 pin	J-FET Input Low Power, Op Amp
μPC741	C/G2 - 8 pin	General Purpose Op Amp
μPC811	C/G2 - 8 pin	JFET Input High Performance Op Amp
μPC813	C/G2 - 8 pin	JFET Input High Performance Op Amp
μPC4061	C/G2 - 8 pin	J-FET Input, Low Power, Op Amp
μPC4071	C/G2 - 8 pin	J-FET Input, Low Noise, Op Amp
μPC4081	C/G2 - 8 pin	J-FET Input, Low Offset/Bias Current
μPC4250	C/G2 - 8 pin	Programmable Op Amp

DUAL OP AMPS

μPC358	C/G2 - 8 pin	Low Power Op Amp
μPC812	C - 8 pin	J-FET Input Low Offset Voltage, High Stability, Op Amp
μPC814	C - 8 pin	High Performance
μPC1458	C/G2 - 8 pin	General Purpose Op Amp
μPC4062	C/G2 - 8 pin	J-FET Input, Low Power, Op Amp
μPC4072	C/G2 - 8 pin	J-FET Input, Low Noise, Op Amp
μPC4082	C/G2 - 8 pin	J-FET Input, Low Offset/Bias Current
μPC4359	C - 8 pin	High Performance
μPC4556	C/G2 - 8 pin	High Performance, Decompensated, Op Amp
μPC4557	C - 8 pin	High Performance Op Amp
μPC4558	C/G2 - 8 pin	High Performance Op Amp
μPC4559	C - 8 pin	High Performance Op Amp
μPC4560	C/G2 - 8 pin	High Performance Op Amp
μPC4570	C/G2 - 8 pin	Ultra Low Noise, Wide Bandwidth Op Amp

QUAD OP AMPS

μPC324	C/G2 - 14 pin	Low Power Op Amp
μPC3403	C/G2 - 14 pin	Low Power Op Amp
μPC4064	C/G2 - 14 pin	J-FET Input, Low Power Op Amp
μPC4074	C/G2 - 14 pin	J-FET Input, Low Power Op Amp
μPC4084	C - 14 pin	J-FET Input, Low Offset/Bias Current
μPC4574	C/G2 - 14 pin	Ultra Low Noise, High Bandwidth
μPC4741	C/G2 - 14 pin	High Performance Op Amp

COMPARATORS

Part No.	Package	Description
μPC311	C/G2 - 8 pin	Precision Comparator (Single)
μPC319	C/G2 - 14 pin	High Speed Comparator (Dual)
μPC339	C/G2 - 14 pin	Low Power Comparator (Quad)
μPC393	C/G2 - 8 pin	Low Power Comparator (Dual)

CCD = CHARGED COUPLED DEVICES FOR IMAGE SENSING

μPC603	D - 14 pin	High Performance, 6-Bit D/A
μPC610	D - 18 pin	Polarized, 10-Bit D/A
μPC624	D - 16 pin	Multiplying, High Speed, 8-Bit D/A
μPC6012	C - 20 pin	Multiplying, High Speed, 12-Bit D/A
μPD6900	C - 22 pin	Video DAC, 20 mHz CMOS
μPD7011	C - 18 pin	Serial/Parallel I/O, NMOS 8-Bit D/A

DIGITAL TO ANALOG CONVERTERS

μPD791	D - 24 pin	4096-Bit Linear Image Sensor, CCD, 7 μm by 5 μm Photo Element Size
μPD795	D - 20 pin	1024-Bit Linear Image Sensor, CCD, 14 μm by 9 μm Photo Element Size
μPD799	D - 24 pin	2048-Bit Linear Image Sensor, CCD, 14 μm by 9 μm Photo Element Size

ANALOG TO DIGITAL CONVERTERS [CMOS]

μPD6950	C - 24 pin	Video ADC, 20 mHz Flash CMOS
μPD7001	C - 16 pin	Serial Output, 4 Channel Input, CMOS, 8-Bit Succesive Approximation A/D
μPD7002	C - 28 pin	4 Channel Input, CMOS, 8/10-Bit Integrating A/D (Accuracy 0.2% FSR)
μPD7002(-1)	C - 28 pin	Same as μPD7002 with Higher Conversion accuracy (0.1% FSR)
μPD7003	C - 24 pin	High Speed, Parallel (FLASH), CMOS 8-Bit A/D (Conversion time 4 μs)
μPD7004	C - 28 pin	8 Channel Input, Serial or Parallel Output, CMOS 10-Bit A/D

Full Product Line Guide (cont)

FUNCTIONAL BLOCKS

Part No.	Package	Description
μPC305	C - 8 pin	Voltage Regulator Controller
μPC398	C - 8 pin	Monolithic Sample and Hold Circuit
μPC494	C/G2 - 16 pin	Switching Regulator (SMPS) Controller
μPC751	B/D - 22 pin	Quad Read/Write Amp for Hard Disk
μPC752	B - 22 pin	4 Input/Output, Hard Disk Amplifier
μPC1042	C - 16 pin	Switching Regulator Control Circuit
μPC1060	C - 8 pin	2.5 Volt Precision Voltage Reference, for use with D/A and A/D Converters
μPC1555	C/G2 - 8 pin	Precision Timer
μPC1571	C - 16 pin	Compander
μPC1663	C - 8 pin	Ultra Wide Bandwidth Differential Amp
μPC1664	C - 14 pin	Ultra Wide Bandwidth Differential Amp
μPC3423	C - 8 pin	Precision Timer
μPC5555/6	C/G2 - 8/14 pin	CMOS Precision Timers

VOLTAGE REGULATORS
Positive-3 Terminal Regulators-0.1 AMP

μPC78L05	TO-92	5 Volt, Fixed
μPC78L08	TO-92	8 Volt, Fixed
μPC78L10	TO-92	10 Volt, Fixed
μPC78L12	TO-92	12 Volt, Fixed
μPC78L15	TO-92	15 Volt, Fixed

VOLTAGE REGULATORS
Positive-3 Terminal Regulators-0.5 AMP

μPC2605	TO-220	5 Volt, Fixed Low Drop
μPC2610	TO-220	10 Volt, Fixed Low Drop
μPC78M05	TO-220	5 Volt, Fixed
μPC78M08	TO-220	8 Volt, Fixed
μPC78M10	TO-220	10 Volt, Fixed
μPC78M12	TO-220	12 Volt, Fixed
μPC78M15	TO-220	15 Volt, Fixed
μPC78M18	TO-220	18 Volt, Fixed
μPC78M24	TO-220	24 Volt, Fixed

Contact your local NEC sales office for more information

VOLTAGE REGULATORS
Positive-3 Terminal Regulators-1.0 AMP

Part No.	Package	Description
μPC317	TO-220	3 to 30 Volt, Variable
μPC7805	TO-220	5 Volt, Fixed
μPC7808	TO-220	8 Volt, Fixed
μPC7812	TO-220	12 Volt, Fixed
μPC7815	TO-220	15 Volt, Fixed
μPC7818	TO-220	18 Volt, Fixed
μPC7824	TO-220	24 Volt, Fixed

VOLTAGE REGULATORS
Negative-3 Terminal Regulators-0.1 AMP

μPC79L05	TO-92	5 Volt, Fixed
μPC79L08	TO-92	8 Volt, Fixed
μPC79L12	TO-92	12 Volt, Fixed
μPC79L15	TO-92	15 Volt, Fixed

VOLTAGE REGULATORS
Negative-3 Terminal Regulators-0.5 AMP

μPC79M05	TO-220	5 Volt, Fixed
μPC79M08	TO-220	8 Volt, Fixed
μPC79M12	TO-220	12 Volt, Fixed
μPC79M15	TO-220	15 Volt, Fixed
μPC79M24	TO-220	24 Volt, Fixed

VOLTAGE REGULATORS
Negative-3 Terminal Regulators-1.0 AMP

μPC7905	TO-220	5 Volt, Fixed
μPC7908	TO-220	8 Volt, Fixed
μPC7910	TO-220	10 Volt, Fixed
μPC7912	TO-220	12 Volt, Fixed
μPC7915	TO-220	15 Volt, Fixed
μPC7918	TO-220	18 Volt, Fixed
μPC7924	TO-220	24 Volt, Fixed

Notes: C = Plastic DIP G2 = Plastic Miniflat DIP
D = Ceramic DIP B= Ceramic Flat Pack

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Discontinued Products

Old Part Number	Replacement	Old Part Number	Replacement	Old Part Number	Replacement
μPC550	None	μPC254	None	μPC616	μPC3911
μPC141C	μPC305	μPC258	μPC4558	μPC617	μPC1555
μPC151	μPC741	μPC259	μPC4560	μPC646/647	None
μPC154	None	μPC271	μPC311	μPC648	μPC6012
μPC156	None	μPC272	μPC319	μPC649	μPC398
μPC157	μPC301	μPC277	μPC393	μPC801	μPC4081
μPC159	μPC318	μPC354	None	μPC802	μPC4250
μPC177	μPC339	μPC451	μPC324	μPC803	μPC4082
μPC209	μPC4359	μPC452	μPC3403	μPC804	μPC4084
μPC251	μPC1458	μPC454	None	μPC1251	μPC358
μPC253	None	μPC458	μPC4741		

QUALITY AND RELIABILITY

Section 2 — Quality and Reliability

Introduction

NEC Electronics is dedicated to producing the highest quality electronic components at competitive prices with on-time deliveries. In order to guarantee this high level of product reliability, it is essential to build quality into the product — at every phase of operation.

NEC has introduced the concept of Total Quality Control (TQC) across its entire semiconductor product line. By adopting TQC, NEC builds high quality into its products, thus assuring higher reliability. This concept and methodology of TQC are company-wide activities involving all levels of management, engineers, quality control staff, and support staff functions.

NEC's goal is to further improve the superior product that is synonymous with its name. That's why extensive failure analysis tests are performed and corrective actions taken prior to marketing products. At the same time, research and development efforts to achieve even higher standards are an ongoing process.

Quality Control Implementation

Building excellence into a product requires the earliest possible detection of failure in each phase. Immediate action must be taken to remove the cause of failure. Fixed-station quality inspection often precludes the ability to take immediate action. It is, therefore, necessary to perform quality control functions at each step — especially at the conceptual stage.

Significant quality stages include:

- Product Development
- Wafer Processing
- Assembly
- Electrical Testing and Screening
- Pre-Inventory Inspection
- Reliability Assurance Test

Product Development

The product development phase includes product conception, review of the device proposal, organization and physical element design, engineering evaluations, and transfer of the product to manufacturing.

In every step of the product development phase, quality and reliability requirements *must* be satisfied. Utilizing the TQC approach has shortened the product development cycle by two to three months. At NEC, building superiority into the product is essential.

Wafer Processing

During the wafer processing stage, the in-process quality inspections that occur are as follows:

Process	Inspection Item
Wafer	Resistivity, Dimension, and Appearance, Lot Sampling Inspection
Photo-Lithography	Alignment and Etching, 100 percent inspection
Diffusion and Oxidation	Oxide Thickness, Sheet Resistivity, Lot Sampling Inspection
Metallization and Passivation	Thickness, V_{th}, C-V Characteristics, and Lot Sampling
Wafer Sort and Scribe	DC Parameters, 100 Percent Inspection
Die Sort	100 Percent Visual Inspection

Assembly

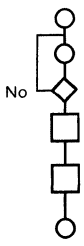
The in-process quality inspections performed during the chip-mounting and packaging stage are as follows:

Process	Inspection Item
Die	Incoming Material Inspection
Die Attach	Appearance, Lot Sampling Inspection
Wire Bonding	Bond Strength, Appearance, Lot Sampling
Packaging	100 Percent Appearance Inspection
Fine Leak*	Lot Sampling
Gross Leak*	100 Percent Inspection

Note: *For ceramic package devices only.

Electrical Testing and Screening

Electrical testing and infant mortality screening are performed at this stage. The flow chart below depicts the process. (Please note: The following diagram illustrates NEC's basic flow and is similar to most processes. Some product lines may have variations. However, in all cases NEC strives for zero defects.)



Flow	Process	Frequency
	1st Electrical	100%
	2nd Electrical	100%
No	PDA	100%
	Pre-Inventory Inspection	Every lot
	Reliability Assurance Tests	Every lot or every month
	Warehouse/Finished Goods	

During the first electrical test, DC parameters are tested in accordance with electrical specifications, on 100% of each lot. This prescreen performance is prior to the infant mortality testing.

In the second electrical test, AC functional as well as DC parameter tests are performed. If the percentage of defective units exceeds a set limit, the lot is subjected to an additional burn-in. During this second burn-in, the defective units undergo a failure analysis. The results of this analysis are then fed back for appropriate corrective action.

Pre-Inventory Inspection

Prior to warehouse storage, lots are subjected to an incoming inspection according to the following sampling plan:

Electrical test:	DC parameters	LTPD 3%
	Function test	LTPD 3%
Appearance		LTPD 3%

Reliability Assurance Testing

A large part of NEC's Total Quality Control program involves various types of reliability assurance tests performed to ensure the highest product quality and reliability possible.

The High Temperature Operating Life Test is used to accelerate failure mechanisms by operating the devices at an elevated temperature. The data obtained is then translated to a lower temperature.

Integrated circuits are highly sensitive to the general accelerating effect of humidity in causing electrolytic corrosion between biased lines. High Temperature and High Humidity Tests are performed to detect failure mechanisms which are accelerated by these conditions. It is especially effective in accelerating leakage-related failures and drifts in device parameters due to process instability.

Another common test is the High Temperature Storage Test. In this test, devices are subjected to elevated temperatures with no applied bias. This test is used to detect any mechanical problems or process instability.

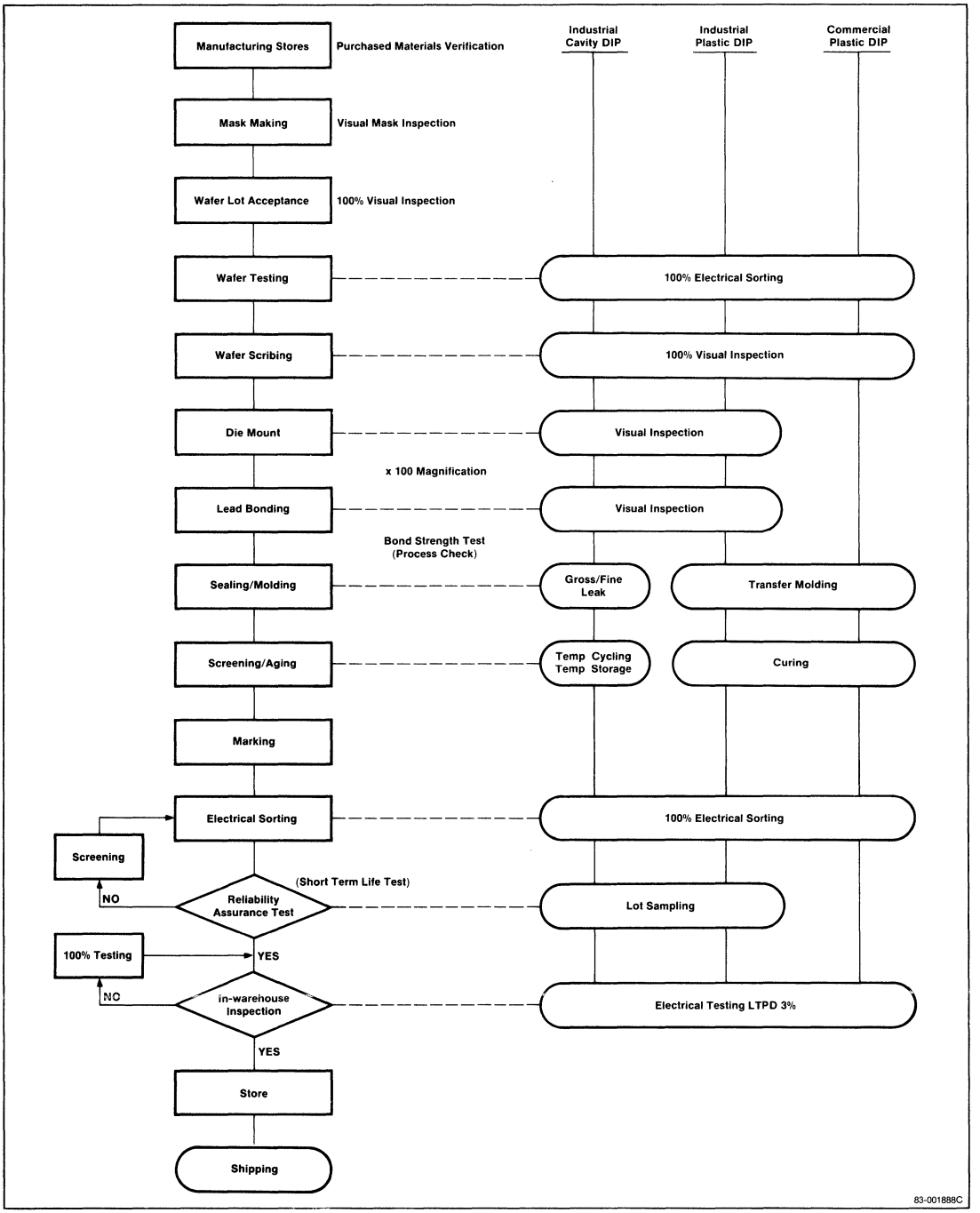
The Environmental Test is performed to detect problems related to packaging, material, susceptibility to environmental extremes, and problems related to usage of the devices.

Summary

Building quality and reliability into products is the most efficient way to ensure product excellence. NEC's adoption of quality control functions at each process step forms a consolidated quality control system, which guarantees a superior product.

With company-wide practice of Total Quality Control, NEC is committed to producing superior products. Through continuous research and development, extensive failure analysis and process improvements, higher standards of quality and reliability are continuously set and maintained.

Quality Control Flowchart



Periodical Reliability Test

Industrial Cavity DIP

	Test Items	Test Conditions
Environmental Test	Soldering Heat	260 °C, 10 sec, once
	Temperature Cycle	−65 °C to +150 °C, 10 cycles, 30 min each temp
	Thermal Shock	100 °C and 0 °C, 15 cycles, 5 min each temp
	Mechanical Shock	1500G, 0.5 ms, XYZ Axis, 5 times
	Variable Frequency Vibration	100 Hz to 2000 Hz, 20G, XYZ Axis, 4 times
	Constant Acceleration	2000G, XYZ Axis, 1 min each
	Lead Fatigue	250 g, 90 degrees, 3 times, 3 or 4 leads
	Solderability	230 °C, 5 sec, once, with rosin flux
Life Test	Bias Temperature Test	T_A = 125 °C, Maximum Rated Voltage, 1000 hours
	High Temperature Storage Test	T_A = 175 °C, 1000 hours

Industrial Plastic Molded DIP

	Test Items	Test Conditions
Environmental Test	Soldering Heat	260 °C, 10 sec, once
	Temperature Cycle	−65 °C to +150 °C, 10 cycles, 30 min each temp
	Thermal Shock	100 °C and 0 °C, 15 cycles, 5 min each temp
	Lead Fatigue	250 g, 90 degrees, 3 times, 3 or 4 leads
	Solderability	230 °C, 5 sec, once, with rosin flux
Life Test	Bias Temperature Test	T_A = 125 °C, Maximum Rated Voltage, 1000 hours
	High Temperature Storage Test	T_A = 150 °C, 1000 hours
	High Temperature, High Humidity Storage Test	T_A = 65 °C, R_H=95%, 1000 hours
	Pressure Cooker Test	T_A = 125 °C, R_H = 100%, 96 Hr

Industrial Miniflat IC

	Test Items	Test Conditions
Environmental Test	Solderability	230 °C, 5 sec, once
	Temperature Cycle	−65 °C to +150 °C, 10 cycles, 30 min each temp
	Thermal Shock	100 °C and 0 °C, 15 cycles, 5 min each temp.
Life Test	Bias Temperature Test	T_A = 125 °C, Maximum Rated Voltage, 1000 hours
	High Temperature Storage Test	T_A = 150 °C, 1000 hours
	High Temperature, High Humidity Storage Test	T_A = 65 °C, R_H=95%, 1000 hours
	Pressure Cooker Test	T_A = 125 °C, R_H = 100%, 48 Hr

Note: 1. Periodical reliability test is carried out every three months for each product.

OPERATIONAL AMPLIFIERS

3

Section 3 — Operational Amplifiers

NEC Electronics Inc.

μPC301A GENERAL PURPOSE OPERATIONAL AMPLIFIER

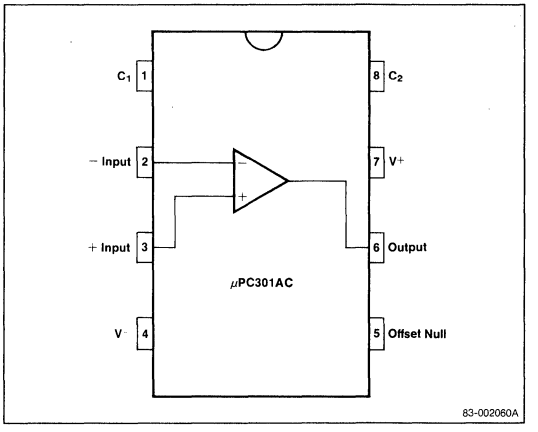
Description

The μPC301A is a general purpose amplifier offering higher performance than 709 type operational amplifiers. This amplifier offers virtually foolproof operation with overload protection on both input and output to prevent latch-up when the common mode range is exceeded. In addition, circuit stability is assured by use of a single 30-pF capacitor. Frequency compensation can also be tailored to meet the needs of individual circuits with a single external capacitor.

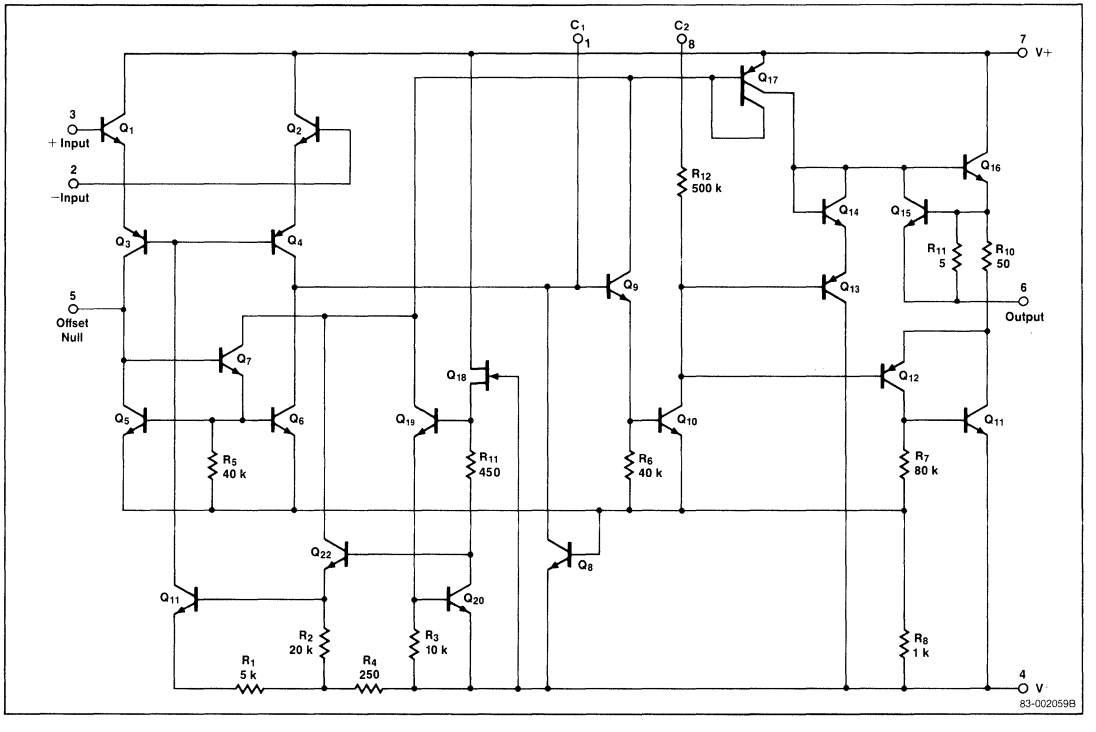
Features

- ☐ Wide common mode and differential voltage range
- ☐ Short-circuit protection
- ☐ No latch-up
- ☐ Offset voltage null capability
- ☐ Adjustable frequency and transient response characteristics
- ☐ LM301A direct replacement

Pin Configuration



Equivalent Circuit



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Electrical Characteristics

$T_A = 25°C$, $V^{\pm} = \pm5$ V to ±15 V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		2.0	7.5	mV	$R_S \leq 50$ kΩ
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		6.0	30	μV/°C	$R_S \leq 50$ kΩ, $V^{\pm} = \pm15$ V
Input Offset Current	I_{io}		3	50	nA	
Input Offset Current Drift	$\Delta V_{io}/\Delta T$		0.02	0.6	nA/°C	$V^{\pm} = \pm15$ V
Input Bias Current	I_b		70	250	nA	
Input Impedance			0.5	2	MΩ	
Large Signal Voltage Gain	A_{VOL}		88	104	dB	$V^{\pm} = \pm15$ V, $V_O = \pm10$ V, $R_L \geq 2$ kΩ
Supply Current	I_{CC}		1.8	3	mA	
Output Voltage Swing	V_{om}	±12	±14		V	$V^{\pm} = \pm15$ V, $R_L \geq 10$ kΩ
Output Voltage Swing	V_{om}	±10	±13		V	$V^{\pm} = \pm15$ V, $R_L \geq 2$ kΩ
Common Mode Input Voltage Range	V_{icm}	±12			V	$V^{\pm} = \pm15$ V
Common Mode Rejection Ratio	CMRR	70	90		dB	$R_S \leq 50$ kΩ
Supply Voltage Rejection Ratio	SVRR	70	90		dB	$R_S \leq 50$ kΩ

Ordering Information

Part Number	Package	Operating Temperature Range
μPC301AC	Plastic DIP	0°C to +70°C

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V^+ and V^-	36 V
Power Dissipation	350 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

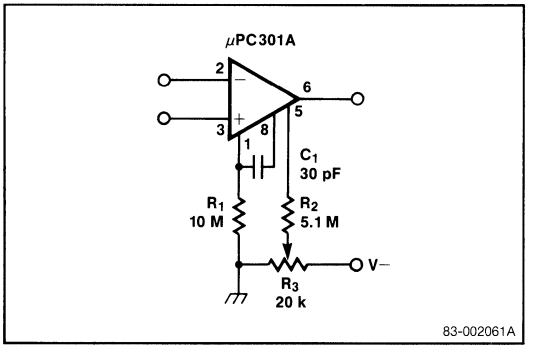
Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

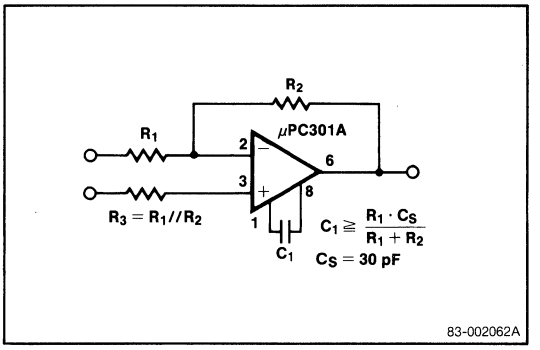
Typical Characteristics

$T_A = 25°C$

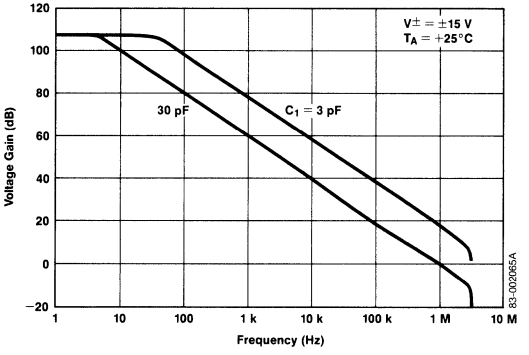
Standard Compensation and Offset Balance Circuit



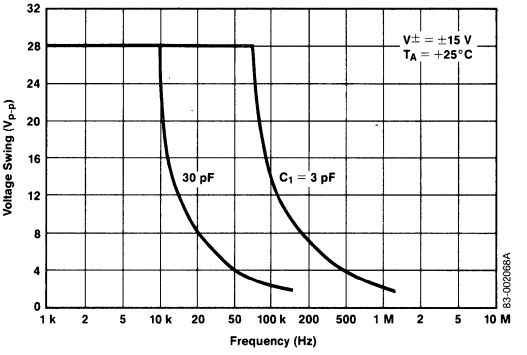
Single Pole Compensation



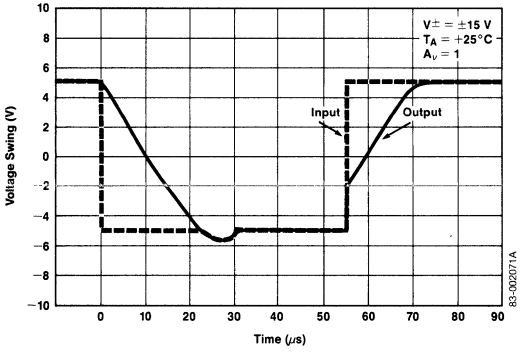
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



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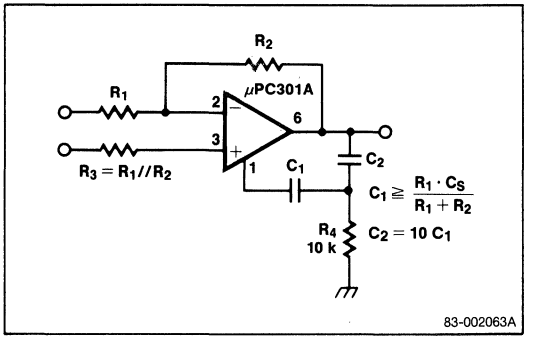
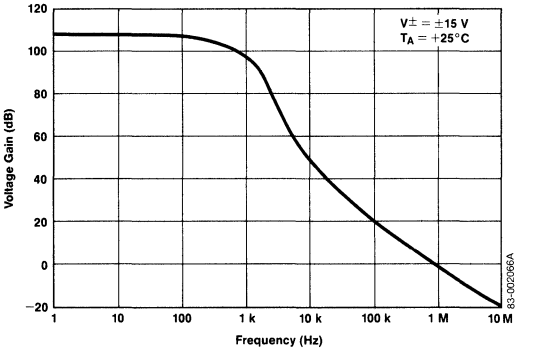
Typical Characteristics (Cont.)

$T_A = 25°C$

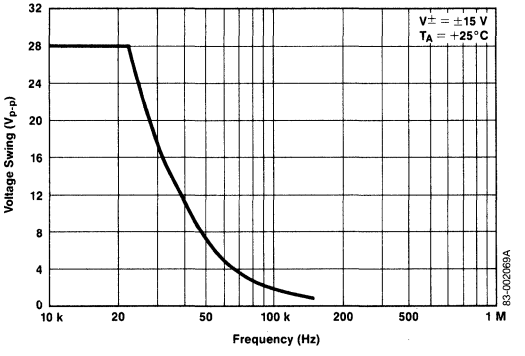
Two Pole Compensation



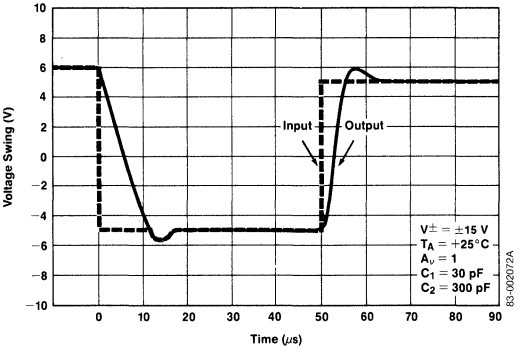
Open Loop Frequency Response



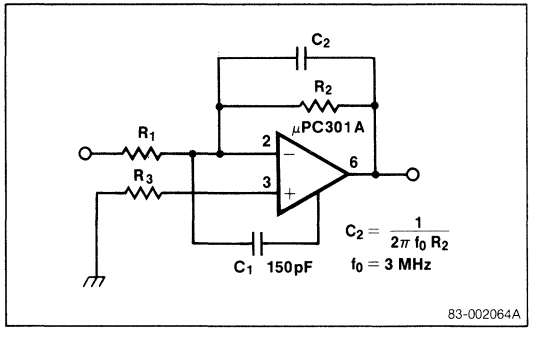
Large Signal Frequency Response



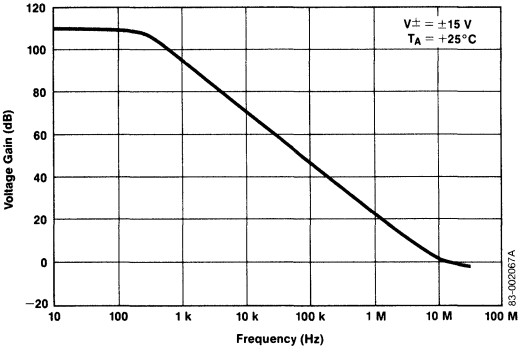
Voltage Follower Pulse Response



Feedforward Compensation



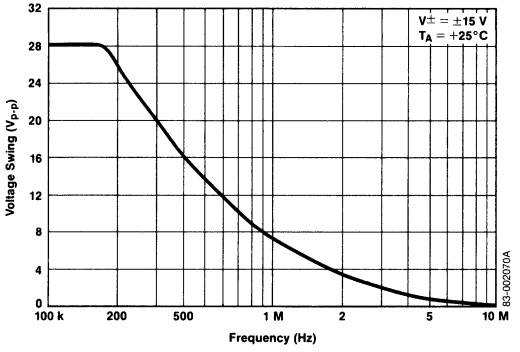
Open Loop Frequency Response



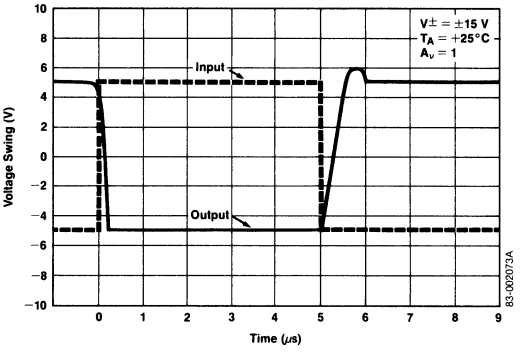
Typical Characteristics (Cont.)

$T_A = 25°C$

Large Signal Frequency Response



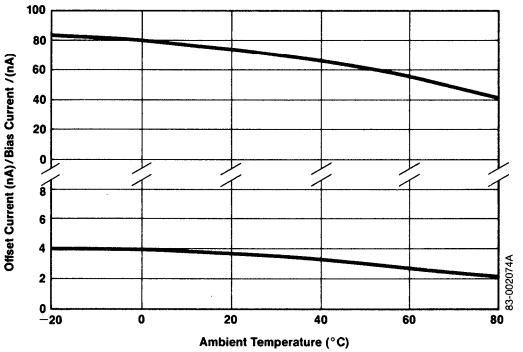
Inverter Pulse Response



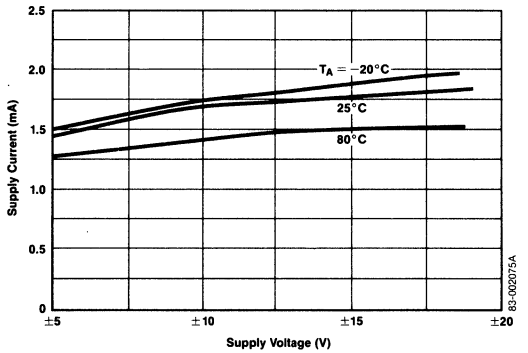
Operating Characteristics

$T_A = 25°C$

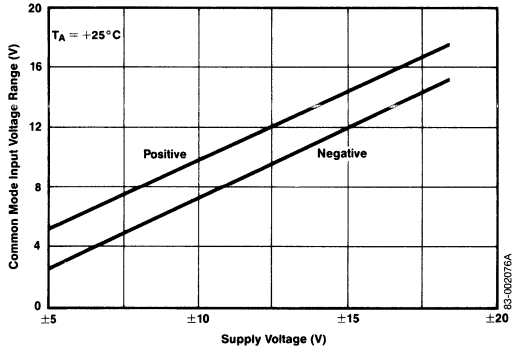
Input Current



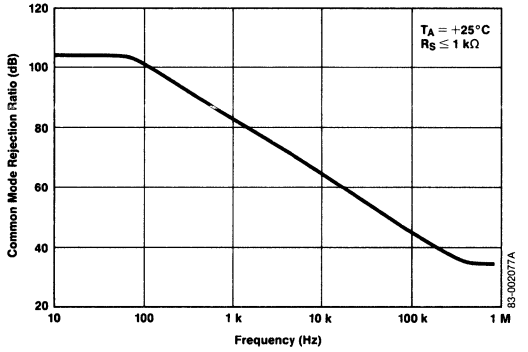
Supply Current



Common Mode Input Voltage Range



Common Mode Rejection Ratio

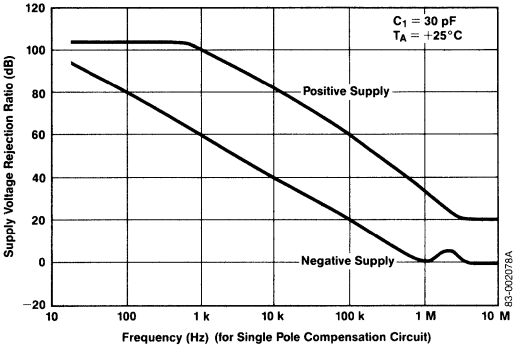


3

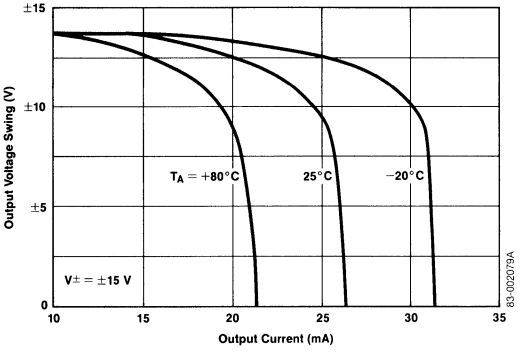
Operating Characteristics (Cont.)

$T_A = 25\,°C$

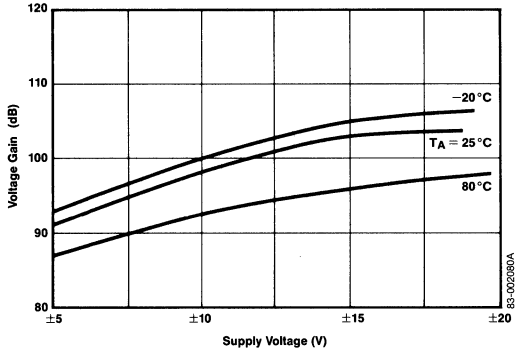
Supply Voltage Rejection Ratio



Current Limiting



Voltage Gain



μPC318
HIGH-SPEED OPERATIONAL AMPLIFIER

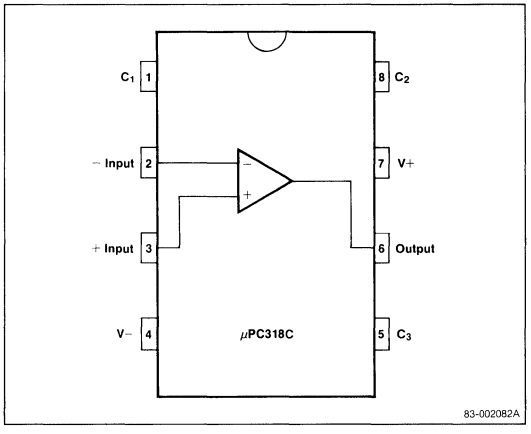
Description

The μPC318 is a precision high-speed operational amplifier designed for applications requiring wide bandwidth and high slew rate. It features a factor of ten increase in speed compared to general purpose operational amplifiers, without degrading the DC performance. By incorporating internal unity gain frequency compensation, external compensation components are eliminated. The high-speed and fast settling time of the μPC318 make it ideal for use in D/A converters, oscillators, sample and hold circuits.

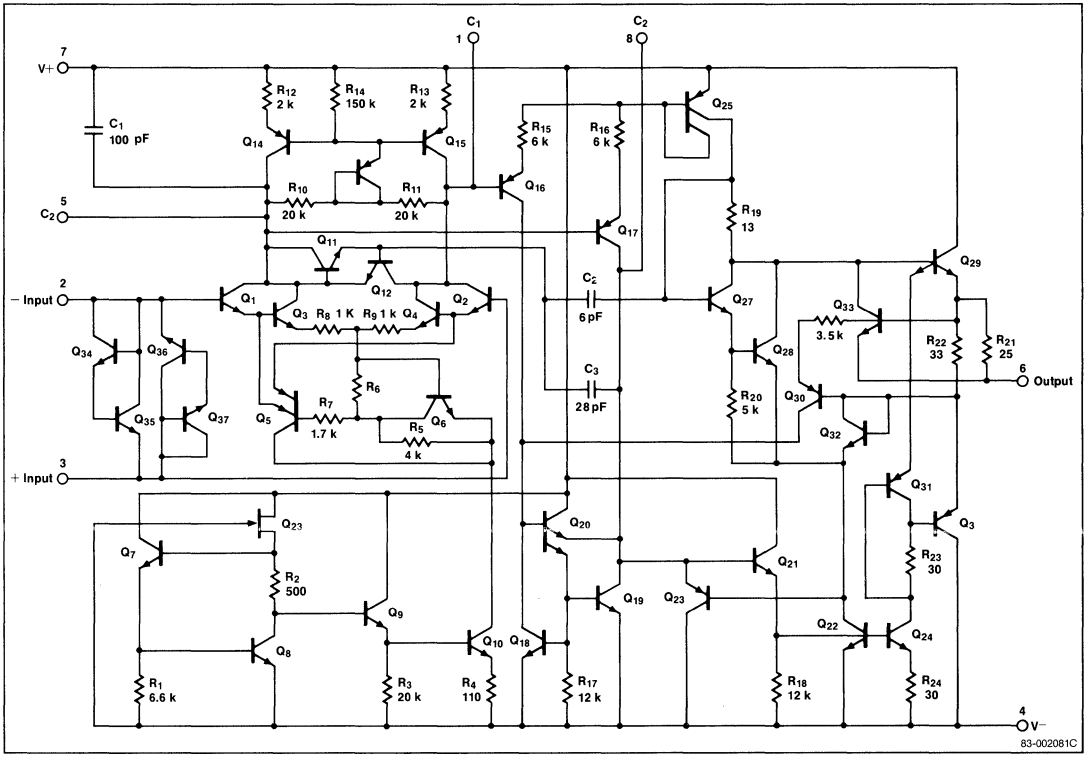
Features

- ☐ Very high slew rate
- ☐ Maximum bias current of 500 nA
- ☐ Operates from supplies of ±5 V to ±20 V
- ☐ Internal frequency compensation
- ☐ Input and output overload protected
- ☐ LM318 direct replacement

Pin Configuration



Equivalent Circuit



Ordering Information

Part Number	Package	Operating Temperature Range
μPC318C	Plastic DIP	0°C to +70°C

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V^+ and V^-	40 V
Power Dissipation	500 mW
Differential Input Current (Note 1)	±10 mA
Input Voltage (Note 2)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55 to +150°C

Notes: 1. The inputs are shunted with back-to-back diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

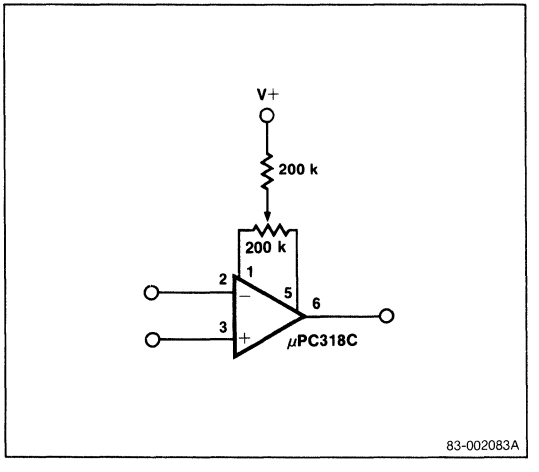
Electrical Characteristics

$T_A = 25°C$, $V^{\pm} = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		4	10	mV	$R_S = 100\ \Omega$
Input Offset Current	I_{io}		30	200	nA	
Input Bias Current	I_b		150	500	nA	
Input Impedance	R_{IN}	0.5	3		MΩ	
Large Signal Voltage Gain	A_{VOL}	88	106		dB	$V_O = \pm 10$ V, $R_L \geq 2$ kΩ
Slew Rate	SR	50	70		V/μs	$A_V = 1$
Output Voltage Swing	V_{OM}	±12	±13		V	$R_L \geq 2$ kΩ
Common Mode Input Voltage Range	V_{icm}	±11.5				
Common Mode Rejection Ratio	CMRR	70	100		dB	
Supply Voltage Rejection Ratio	SVRR	65	80		dB	
Supply Current	I_{CC}		5	10	mA	$R_L = \infty$, $V_O = 0$ V

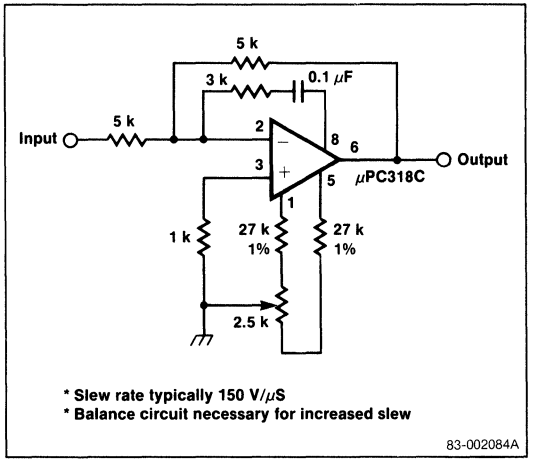
Typical Applications

Offset Balancing Circuit



83-002083A

Feedforward Compensation for Greater Inverting Slew Rate



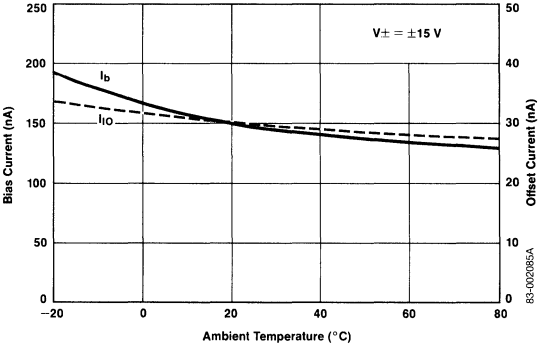
* Slew rate typically 150 V/μS
* Balance circuit necessary for increased slew

83-002084A

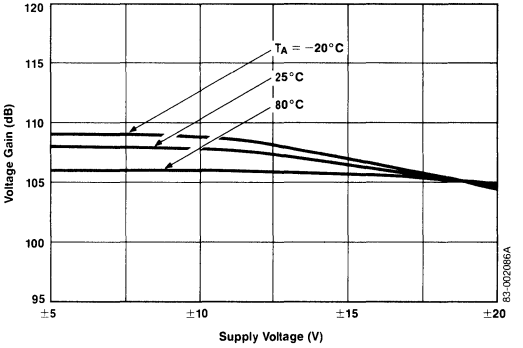
Operating Characteristics

$T_A = 25°C$

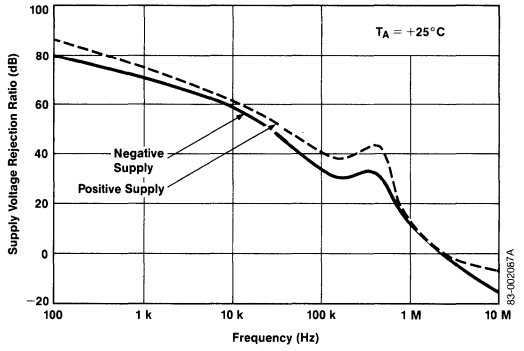
Input Current



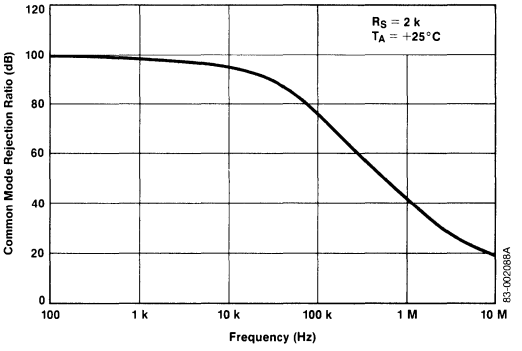
Voltage Gain



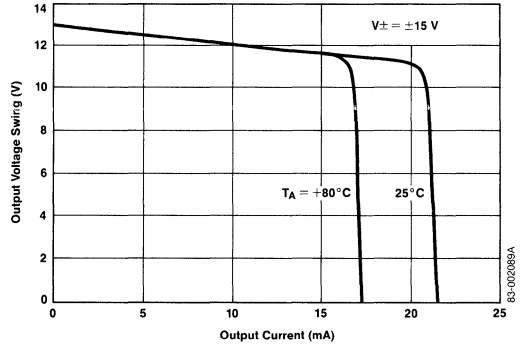
Supply Voltage Rejection Ratio



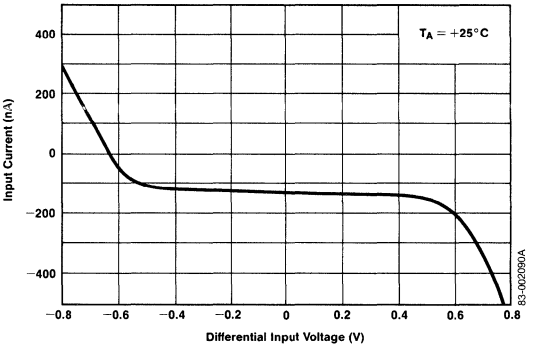
Common Mode Rejection Ratio



Current Limiting



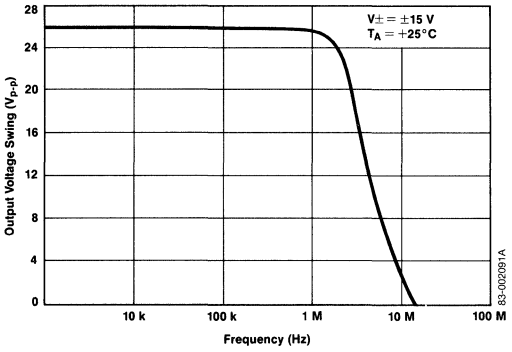
Input Current



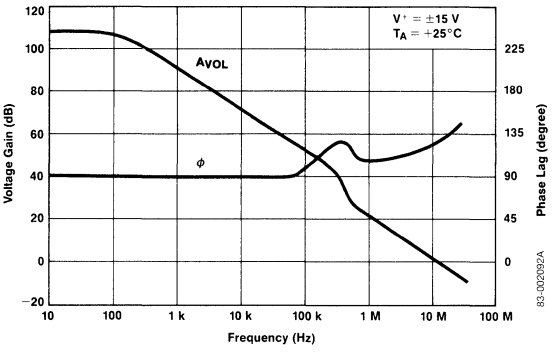
Operating Characteristics (Cont.)

$T_A = 25°C$

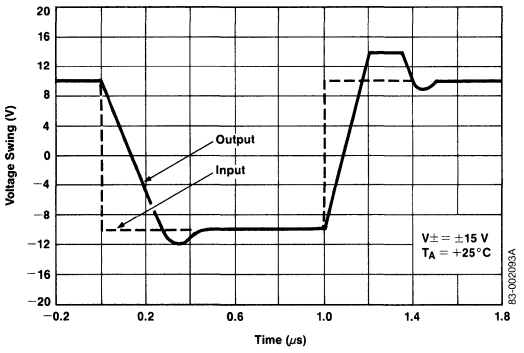
Large Signal Frequency Response



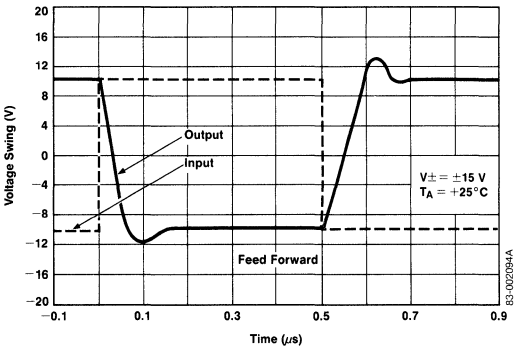
Open Loop Frequency Response



Voltage Follower Pulse Response



Inverter Pulse Response



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μPC356
J-FET INPUT OPERATIONAL AMPLIFIER

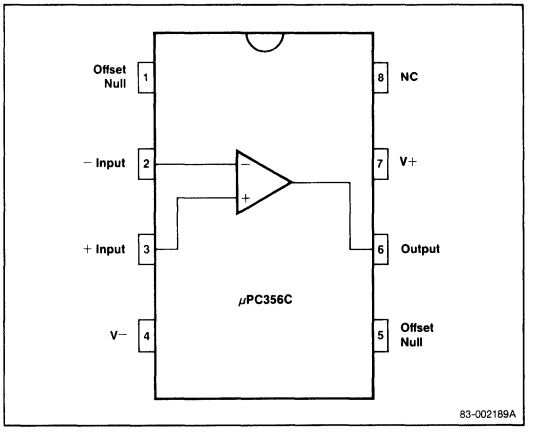
Description

The μPC356 is a J-FET input operational amplifier with matched P-channel ion implanted J-FETs. In addition to the obvious advantages of J-FET inputs, the μPC356 is designed for high slew rate, wide bandwidth, and extremely fast settling time.

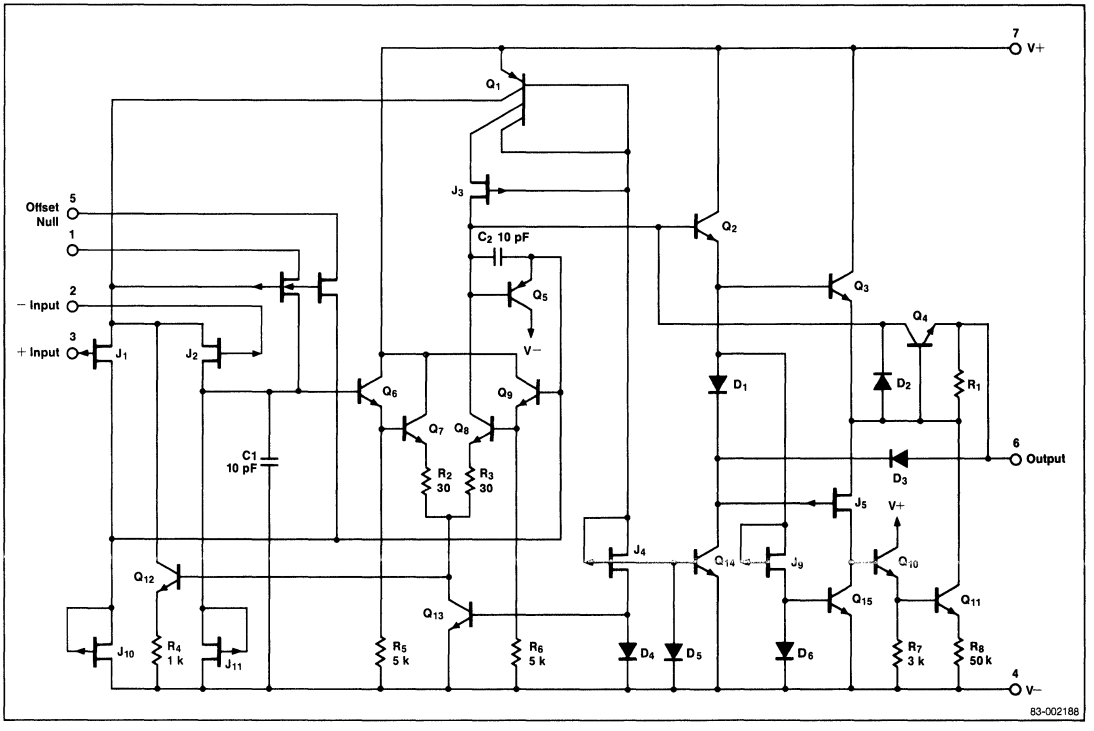
Features

- ☐ Low input offset voltage: 5 mV max (trimming technique used)
- ☐ Offset adjust does not degrade drift or CMRR
- ☐ The NPN sink output stage allows use of large capacitive loads (10,000 pF) without a stability problem
- ☐ Internal compensation and large differential input voltage capability
- ☐ LF356 equivalent

Pin Configuration



Equivalent Circuit



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Ordering Information

Part Number	Package	Operating Temperature Range
μPC356C	Plastic DIP	0°C to +70°C

Electrical Characteristics

$T_A = 25°C$, $V\pm = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		2	5	mV	$R_S \leq 50\ \Omega$
Input Offset Current	I_{io}		3	50	pA	
Input Bias Current	I_b		30	200	pA	
Large Signal Voltage Gain	A_{VOL}	88	106		dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Supply Current	I_{CC}		5	10	mA	
Common Mode Rejection Ratio	CMRR	80	100		dB	
Supply Voltage Rejection Ratio	SVRR	80	100		dB	
Output Voltage Swing	V_{OM}	±12	±13		V	$R_1 \geq 10$ kΩ
		±10	±12		V	$R_1 \geq 2$ kΩ
Common Mode Voltage	V_{ICM}	±10	± 15.1 -12		V	
Slew Rate	SR		12		V/μs	Rise
			20		V/μs	Fall
Input Noise Voltage	en		20		$nV/\sqrt{Hz}$	f = 1 kHz, $R_1 = 100\ \Omega$
Gain Bandwidth Products	GBW		5		MHz	
Over Operating Temperature Range						
Input Offset Voltage	V_{io}			7	mV	$R_S \leq 50\ \Omega$, $T_A = T_{OPT}$
Offset Voltage Drift	$\Delta V_{io}/\Delta T$		5		μV/°C	$T_A = T_{OPT}$
Input Bias Current	I_b			8	nA	$T_A = T_{OPT}$
Input Offset Current	I_{io}			2	nA	$T_A = T_{OPT}$

Absolute Maximum Ratings

$T_A = 25°C$

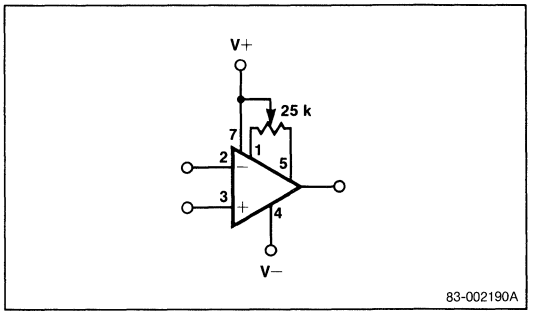
Voltage Between V^+ and V^-	36 V
Power Dissipation	350 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Typical Application

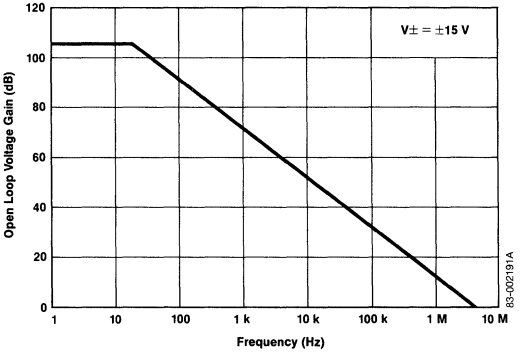
Offset Voltage Null Circuit



Operating Characteristics

$T_A = 25°C$

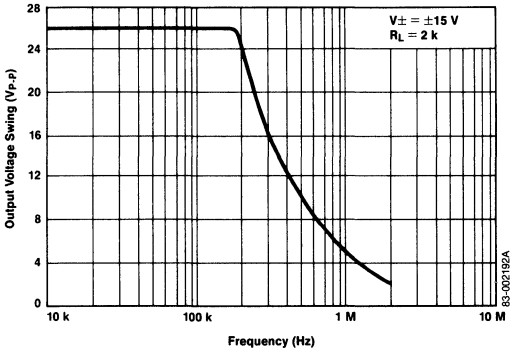
Open Loop Frequency Response



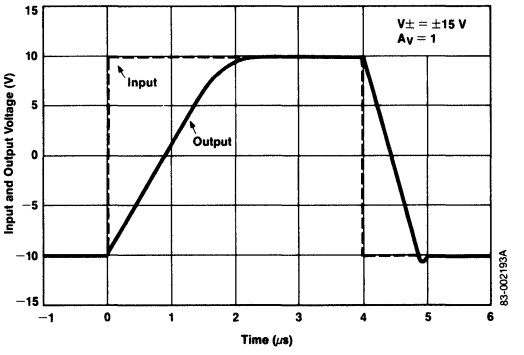
Operating Characteristics (Cont.)

$T_A = 25°C$

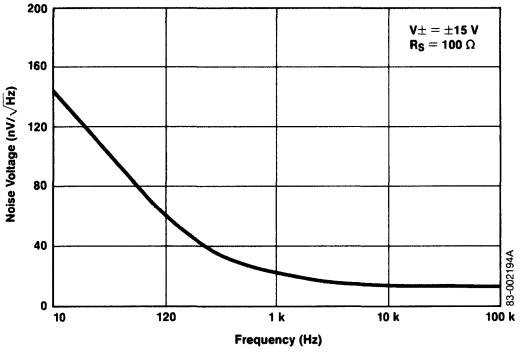
Undistorted Output Voltage Swing



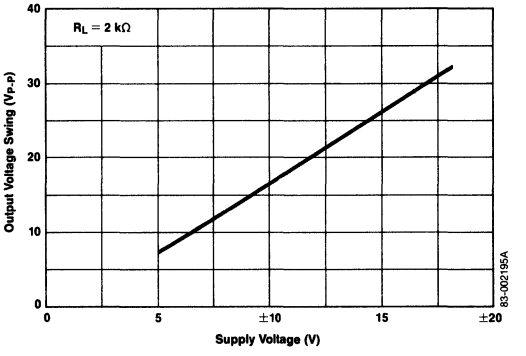
Voltage Follower Pulse Response



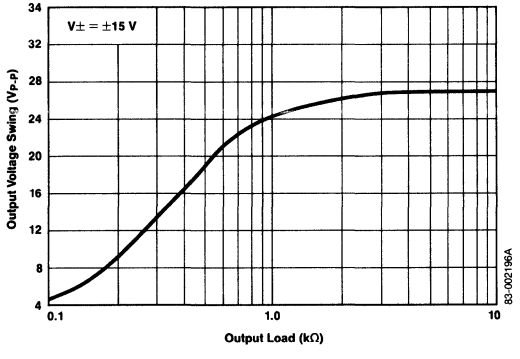
Input Equivalent Noise



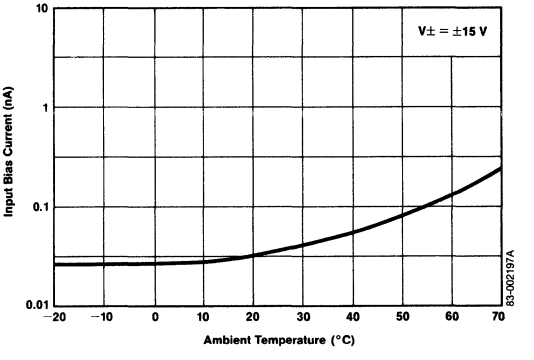
Voltage Swing



Voltage Swing



Input Bias Current

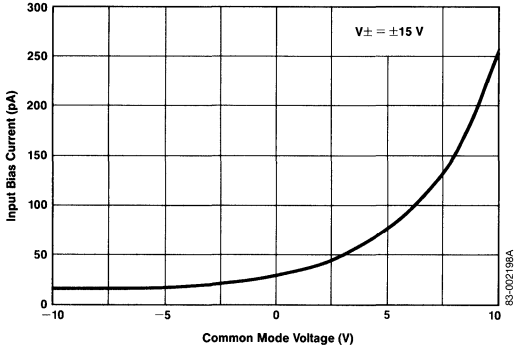


3

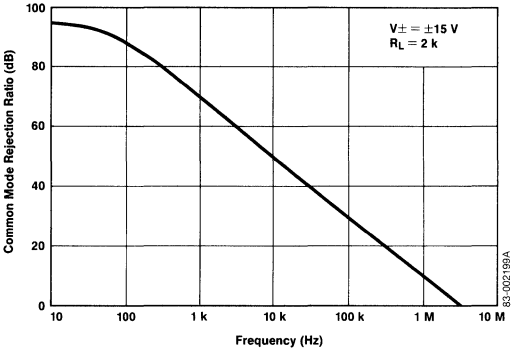
Operating Characteristics (Cont.)

$T_A = 25°C$

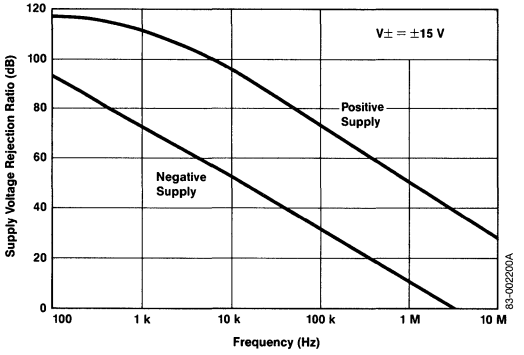
Input Bias Current



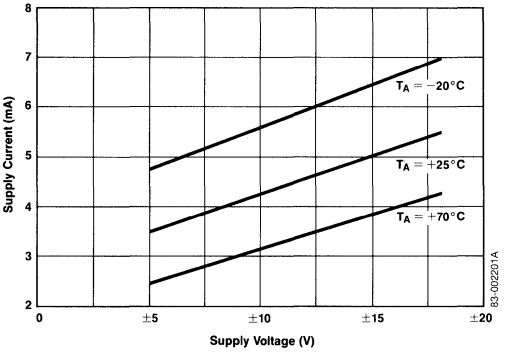
Common Mode Rejection Ratio



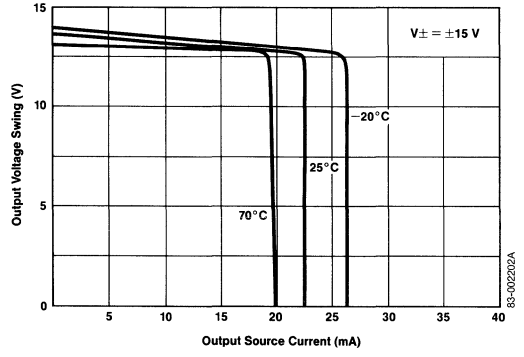
Supply Voltage Rejection Ratio



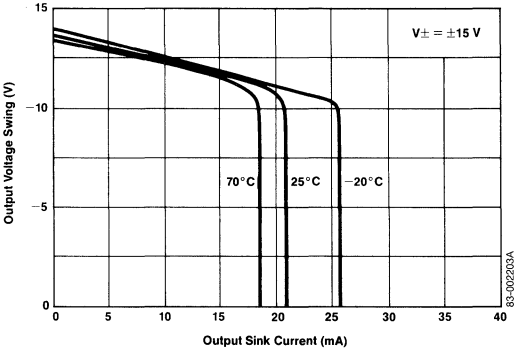
Supply Current



Output Source Current



Output Sink Current



NEC
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μPC357
J-FET INPUT DECOMPENSATED OPERATIONAL AMPLIFIER

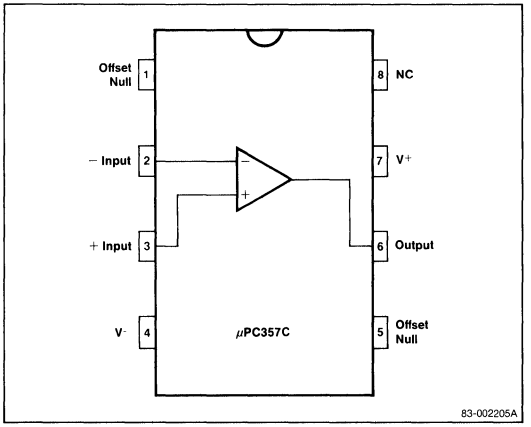
Description

The μPC357 is a decompensated operational amplifier with matched P-channel ion implanted J-FET inputs. When the closed loop gain is greater than five ($A_v > 5$) the μPC357 has a slew rate of 50 V per microsecond and a bandwidth of 20 MHz. This device is ideal for applications which require high-input impedance and high-frequency operation.

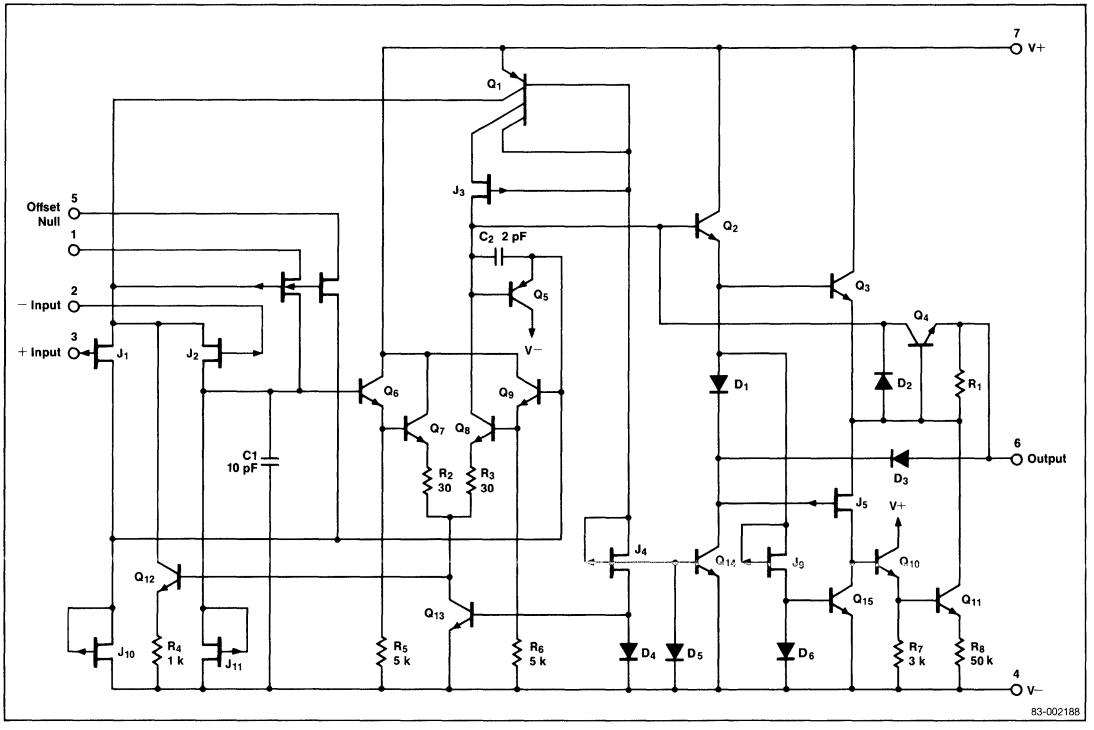
Features

- ☐ Low input offset voltage: 5 mV max
- ☐ Offset adjust does not degrade drift or CMRR
- ☐ High slew rate: 50 V/μs ($A_v > 5$)
- ☐ Wide bandwidth: 20 MHz
- ☐ Suitable for high-speed inverting amplifiers and active filter applications
- ☐ LF357 equivalent

Pin Configuration



Equivalent Circuit



3

Ordering Information

Part Number	Package	Operating Temperature Range
μPC357C	Plastic DIP	0°C to +70°C

Absolute Maximum Ratings

$T_A = 25°C$

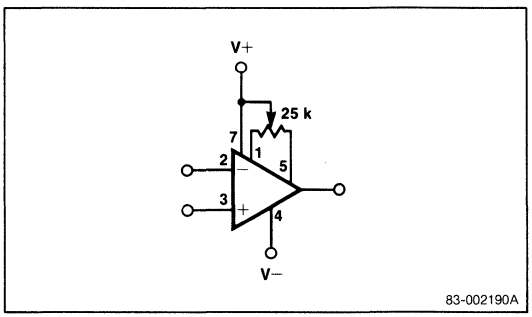
Voltage Between V+ and V−	36 V
Power Dissipation	350 mW
Differential Input Voltage	+30 V
Input Voltage (see note)	+15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Note: For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Typical Application

Offset Voltage Null Circuit



Electrical Characteristics

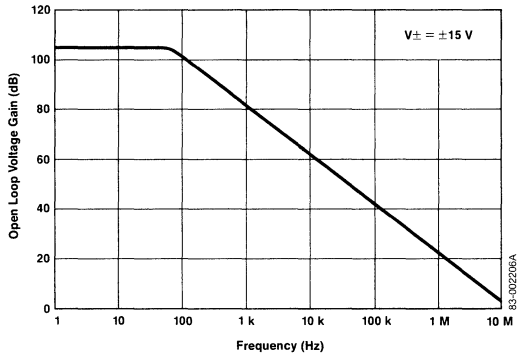
$T_A = 25°C$, $V^{\pm} = \pm 15$ V,

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{IO}		2	5	mV	$R_S \leq 50\ \Omega$
Input Offset Current	I_{IO}		3	50	pA	
Input Bias Current	I_b		30	200	pA	
Large Signal Voltage Gain	A_{VOL}	88	106		dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Supply Current	I_{CC}		5	10	mA	
Common Mode Rejection Ratio	CMRR	80	100		dB	
Supply Voltage Rejection Ratio	SVRR	80	100		dB	
Output Voltage Swing	V_{OM}	±12	±13		V	$R_1 \geq 10$ kΩ
		±10	±12		V	$R_1 \geq 2$ kΩ
Common Mode Voltage	V_{icm}	±10	+15.1 −12		V	
Slew Rate	SR		50		V/μs	Rise
			50		V/μs	Fall
Input Noise Voltage	en		20		nV/√Hz	f = 1 kHz, $R_1 = 100\ \Omega$
Gain Bandwidth Products	GBW		20		MHz	
Over Operating Temperature Range						
Input Offset Voltage	V_{IO}			7	mV	$R_S \leq 50\ \Omega$, $T_A = T_{OPT}$
Offset Voltage Drift	$\Delta V_{IO}/\Delta T$		5		μV/°C	$T_A = T_{OPT}$
Input Bias Current	I_b			8	nA	$T_A = T_{OPT}$
Input Offset Current	I_{IO}			2	nA	$T_A = T_{OPT}$

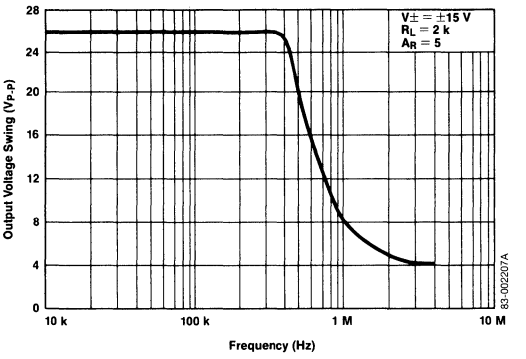
Operating Characteristics

$T_A = 25°C$

Open Loop Frequency Response



Undistorted Output Voltage Swing



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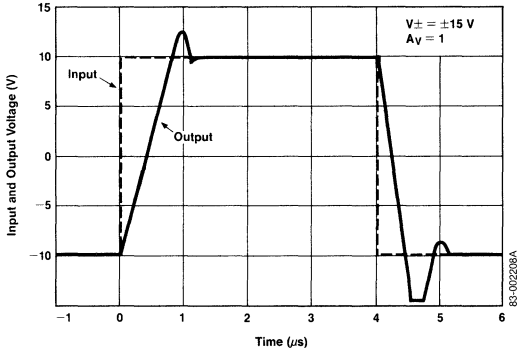
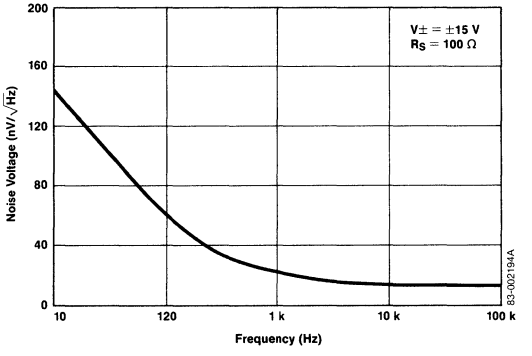
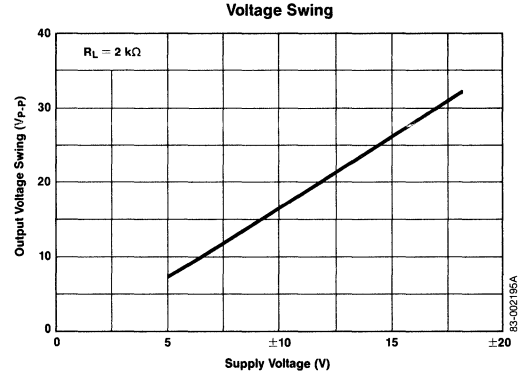
Voltage Follower Pulse Response



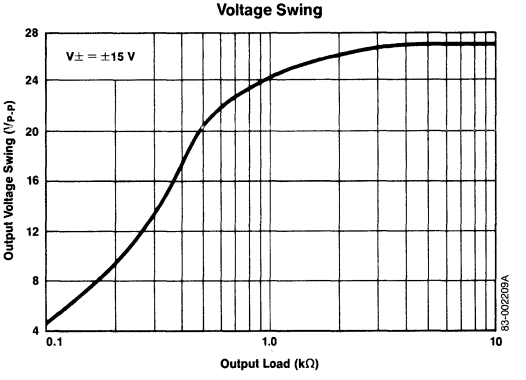
Input Equivalent Noise



Voltage Swing



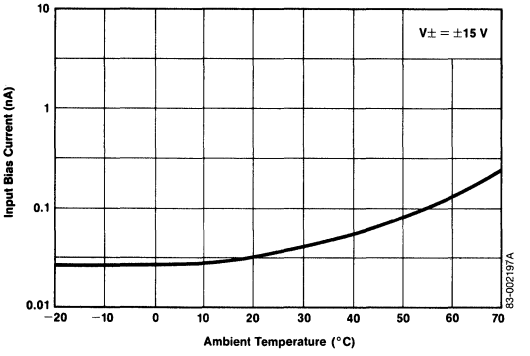
Voltage Swing



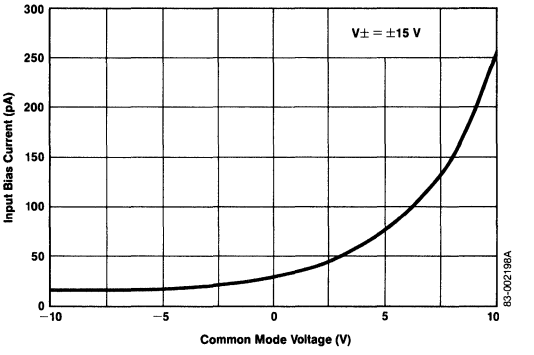
Operating Characteristics (Cont.)

$T_A = 25°C$

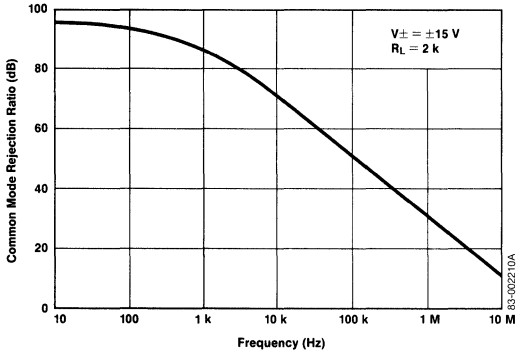
Input Bias Current



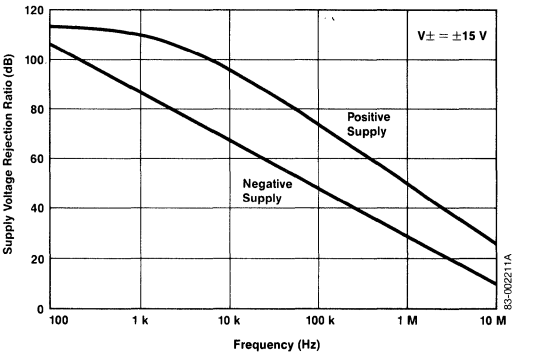
Input Bias Current



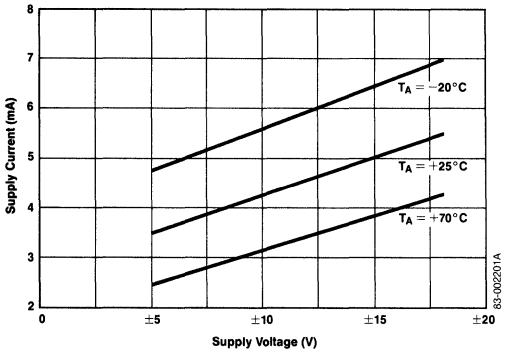
Common Mode Rejection Ratio



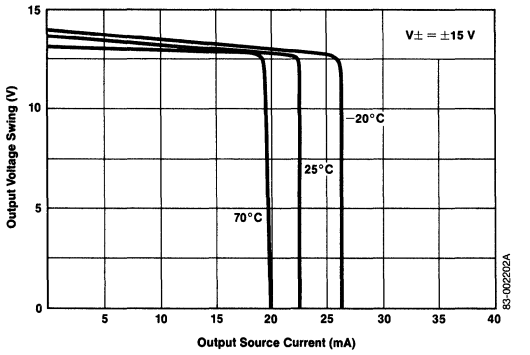
Supply Voltage Rejection Ratio



Supply Current

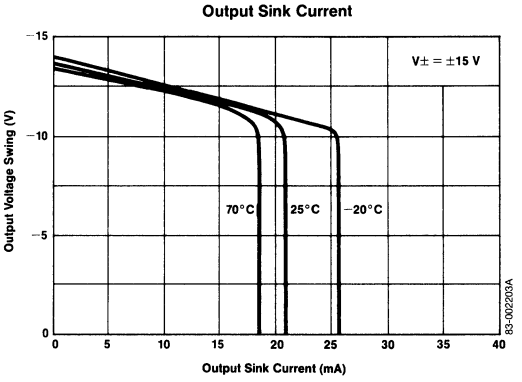


Output Source Current



Operating Characteristics (Cont.)

$T_A = 25°C$



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μPC741
GENERAL PURPOSE OPERATIONAL AMPLIFIER

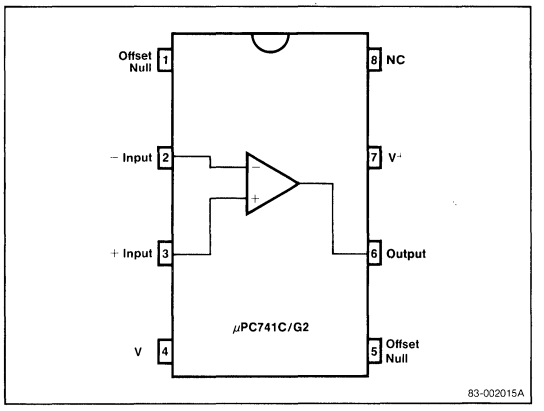
Description

The μPC741 is a general purpose operational amplifier which incorporates internal frequency compensation (C1 = 30 pF). It is intended for a wide range of analog applications where high quality and low cost are required. High common mode voltage range and latch-free operation make this amplifier ideal for use as a voltage follower.

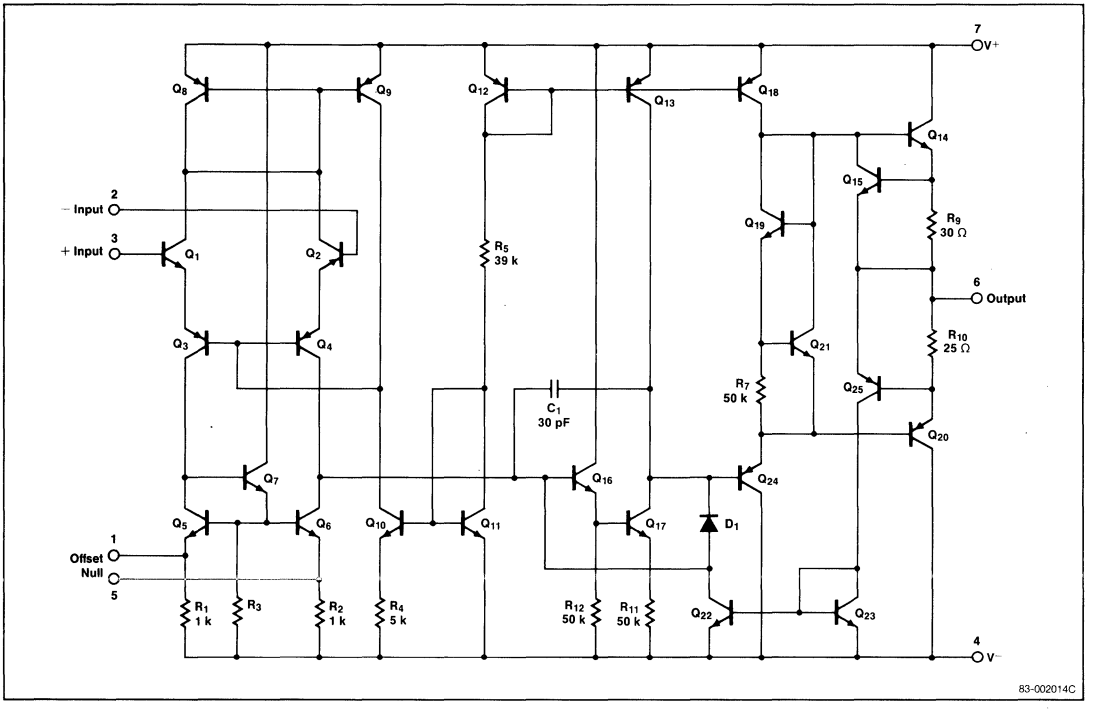
Features

- ☐ Internal frequency compensation
- ☐ Short-circuit protection
- ☐ Offset voltage null capability
- ☐ Large common mode and differential voltage range
- ☐ No latch-up
- ☐ μA741 direct replacement

Pin Configuration



Equivalent Circuit



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Ordering Information

Part Number	Package	Operating Temperature Range
μPC741C	Plastic DIP	0°C to +70°C
μPC741G2	Plastic Miniflat	0°C to +70°C

Absolute Maximum Ratings

$T_A = 25°C$

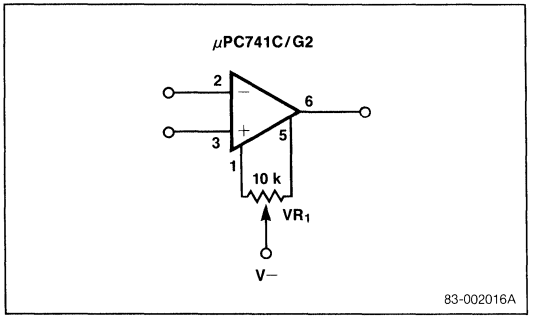
Voltage Between V^+ and V^-	36 V
Power Dissipation, C Package	350 mW
Power Dissipation, G2 Package	440 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Output Short Circuit Duration	Indefinite
Voltage Between Offset Null and V^-	±0.5 V
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Notes: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Typical Application

Offset Voltage Null Circuit



Electrical Characteristics

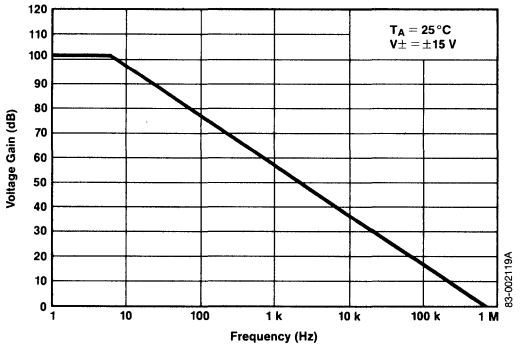
$T_A = 25°C$, $V^{\pm} = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		1.0	6.0	mV	$R_S \leq 10$ kΩ
Input Offset Current	I_{io}		20	200	nA	
Input Bias Current	I_b		80	500	nA	
Large Signal Voltage Gain	A_{VOL}	88	106		dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Offset Voltage Adjustable Range	ΔV_{io}		±15		mV	$VR_1 = 10$ kΩ
Supply Current	I_{CC}		1.5	2.8	mA	
Power Consumption	P_D		45	85	mW	
Common Mode Rejection Ratio	CMRR	70	90		dB	$R_S \leq 10$ kΩ
Supply Voltage Rejection Ratio	SVRR		89	103	dB	$R_S \leq 10$ kΩ
Output Voltage Swing	V_{OM}	±12	±14		V	$R_L \geq 10$ kΩ
Output Voltage Swing	V_{OM}	±10	±13		V	$R_L \geq 2$ kΩ
Output Short Circuit Current	I_{SHORT}	5	20		mA	$R_L = 0$

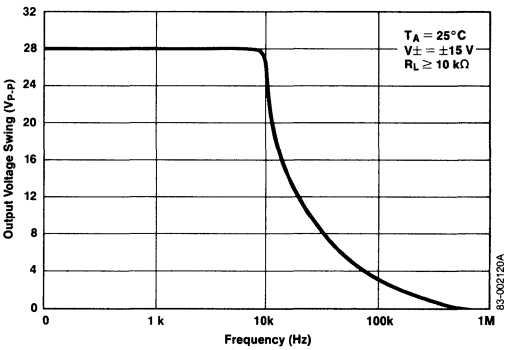
Operating Characteristics

$T_A = 25°C$

Open Loop Frequency Response



Large Signal Frequency Response



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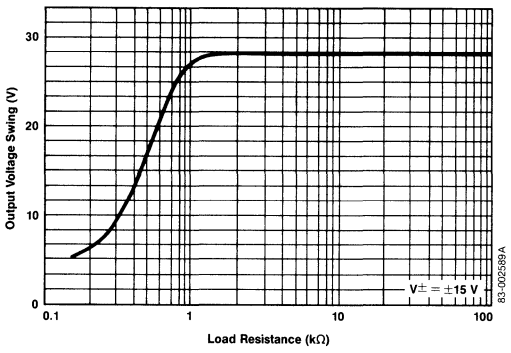
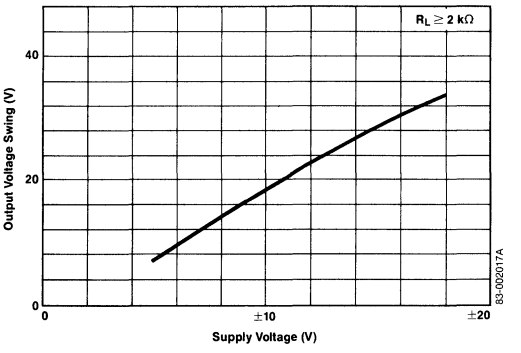
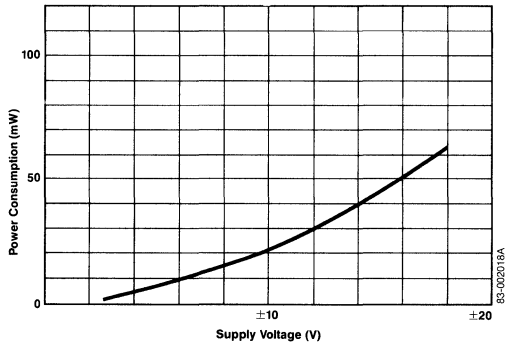
Output Voltage Swing



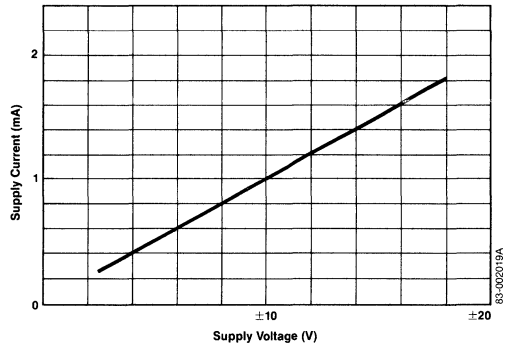
Output Voltage Swing



Power Consumption



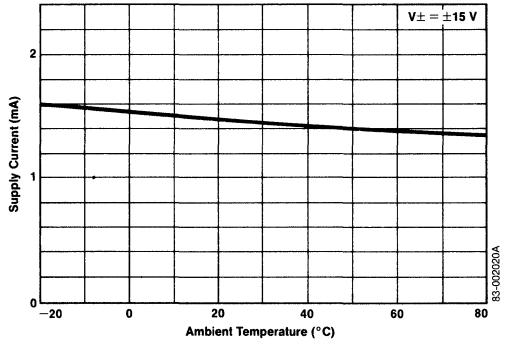
Supply Current



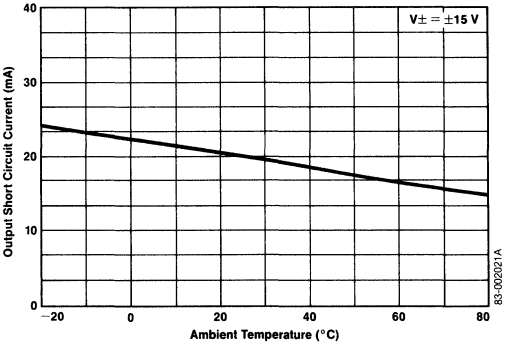
Operating Characteristics (Cont.)

$T_A = 25°C$

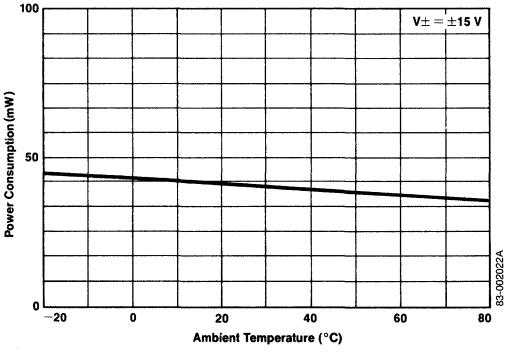
Supply Current



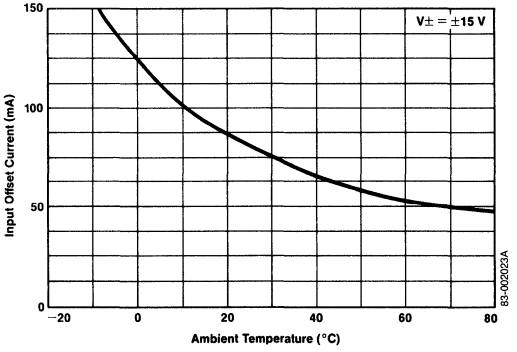
Output Short Circuit Current



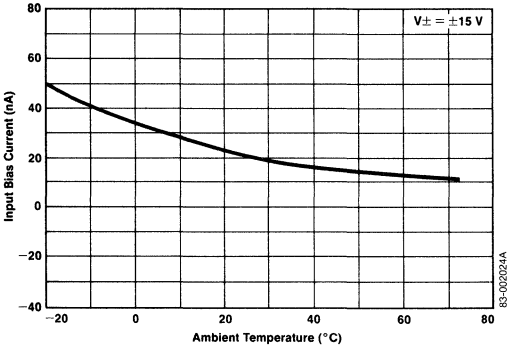
Power Consumption



Input Bias Current



Input Offset Current



NEC

NEC Electronics Inc.

μPC811
J-FET INPUT LOW-OFFSET OPERATIONAL AMPLIFIER

PRELIMINARY INFORMATION

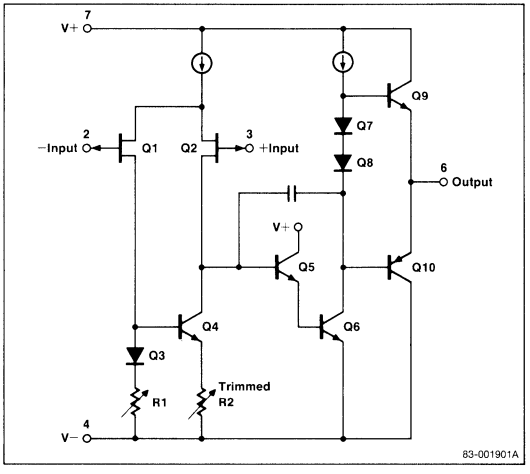
Description

The μPC811 operational amplifier offers high input impedance, low offset voltage, high slew rate, and stable ac operating characteristics. NEC's unique high-speed pnp transistor ($f_T = 300$ MHz) in the output stage solves the oscillation problem of current sinking with a large capacitive load. Zener-zap resistor trimming in the input stage produces excellent offset voltage and temperature drift characteristics.

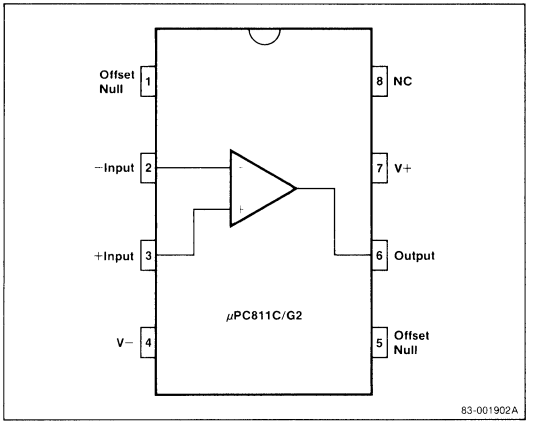
Features

- ☐ Stable operation with 10,000 pF capacitive load
- ☐ Low input offset voltage
  - —2.5 mV max
  - —7 μV/°C temperature drift
- ☐ Low input bias and offset currents
- ☐ Low noise: en = 20 nV/$\sqrt{Hz}$
- ☐ Output short-circuit protection
- ☐ High input impedance
- ☐ Internal frequency compensation
- ☐ High slew rate: 15 V/μs

Equivalent Circuit



Pin Configuration



Ordering Information

Part Number	Package	Operating Temperature Range
μPC811C	8-Pin Plastic DIP	−20 to +70°C
μPC811G2	8-Pin Plastic Miniflat	−20 to +70°C

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Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V±	±5		±16	V
Capacitive Load	C_L			10,000	pF
Output Current	I_O			10	mA

Electrical Characteristics

$T_A = 25°C$, V± = ±15 V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		1	2.5	mV	$R_S = 50\ \Omega$
Input Offset Current	I_{io}		25	100	pA	
Input Bias Current	I_b		50	200	pA	
Voltage Gain	A_{VOL}	88	106		dB	$R_L = 2\ k\Omega$, $V_O = \pm 10$ V
Supply Current	I_{CC}		2.5	3.4	mA	
Common Mode Rejection Ratio	CMRR	70	100		dB	
Supply Voltage Rejection Ratio	SVRR	70	100		dB	
Output Voltage Swing	V_{om}	±12	±13.5		V	$R_L = 10\ k\Omega$
Output Voltage Swing	V_{om}	±10	±12		V	$R_L = 2\ k\Omega$
Common Mode Input Voltage Range	V_{icm}	±11			V	
Slew Rate			15		V/μs	$A_V = +1$
Input Equivalent Noise Voltage	en		20		$nV/\sqrt{Hz}$	$R_S = 100\ \Omega$, f = 1 kHz
Unity Gain Frequency			4		MHz	
Over Operating Temperature						
Input Offset Voltage	V_{io}			5	mV	$R_S = 50\ \Omega$, $T_A = T_{opt}$
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		7		μV/°C	$T_A = T_{opt}$
Input Bias Current	I_b			7	nA	$T_A = T_{opt}$
Input Offset Current	I_{io}			2	nA	$T_A = T_{opt}$

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Power Dissipation, C Package (Note 1)	350 mW
Power Dissipation, G2 Package (Note 2)	440 mW
Differential Input Voltage	±30 V
Common Mode Input Voltage (Note 3)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−55 to +125°C

Notes: 1. Thermal derating factor is 5 mW/°C when ambient temperature is higher than 55°C.
2. Thermal derating factor is 4.4 mW/°C when ambient temperature is higher than 25°C.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NEC

NEC Electronics Inc.

μPC813
J-FET INPUT LOW-OFFSET OPERATIONAL AMPLIFIER

PRELIMINARY INFORMATION

Description

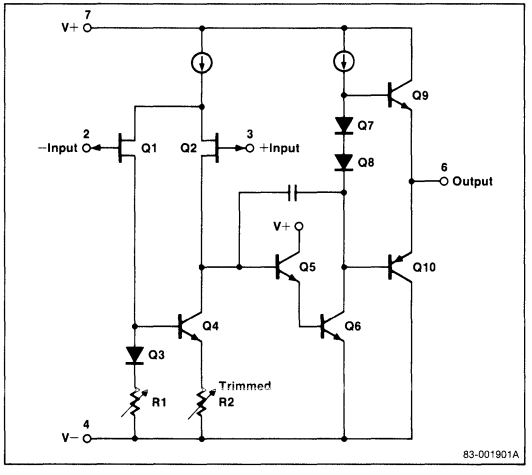
The μPC813 operational amplifier is a high-speed version of the μPC811. NEC's unique high-speed pnp transistor (f_T = 300 MHz) in the output stage yields a high slew rate of 25 V/μs under voltage-follower conditions without an oscillation problem. Zener-zap trimming in the input stage produces excellent offset voltage and temperature drift characteristics.

With ac performance characteristics that are two times better than conventional bi-FET op amps, the μPC813 is ideal for fast integrators, active filters, and other high-speed circuit applications.

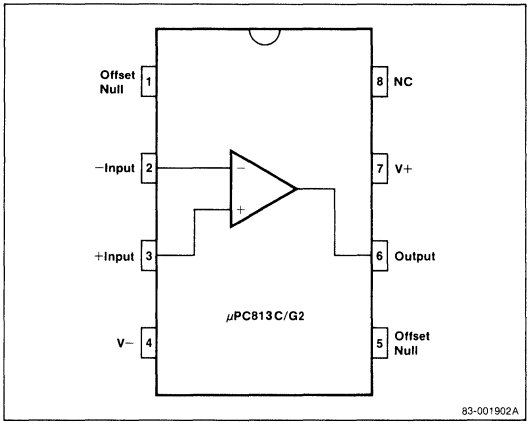
Features

- ☐ High slew rate: 25 V/μs
- ☐ Stable operation with 220 pF capacitive load
- ☐ Low input offset voltage
  - —2.5 mV max
  - —7 μV/°C temperature drift
- ☐ Low input bias and offset currents
- ☐ Low noise: en = 20 nV/$\sqrt{Hz}$
- ☐ Output short-circuit protection
- ☐ High input impedance
- ☐ Internal frequency compensation

Equivalent Circuit



Pin Configuration



Ordering Information

Part Number	Package	Operating Temperature Range
μPC813C	8-Pin Plastic DIP	0 to +70°C
μPC813G2	8-Pin Plastic Miniflat	0 to +70°C

3

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V±	±5		±16	V
Capacitive Load	C_L			220	pF
Output Current	I_O			10	mA

Electrical Characteristics

$T_A = 25°C$, V± = ±15 V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		1	2.5	mV	$R_S = 50\ \Omega$
Input Offset Current	I_{io}		25	100	pA	
Input Bias Current	I_b		50	200	pA	
Voltage Gain	A_{VOL}	88	106		dB	$R_L = 2\ k\Omega$, $V_O = \pm 10$ V
Supply Current	I_{CC}		2.5	3.4	mA	Both channels
Common Mode Rejection Ratio	CMRR	70	100		dB	
Supply Voltage Rejection Ratio	SVRR	70	100		dB	
Output Voltage Swing	V_{om}	±12	±13.5		V	$R_L = 10\ k\Omega$
Output Voltage Swing	V_{om}	±10	±12		V	$R_L = 2\ k\Omega$
Input Voltage Range	V_{icm}	±11			V	
Slew Rate			25		V/μs	$A_V = 1$
Input Noise Voltage	en		20		$nV/\sqrt{Hz}$	$R_S = 100\ \Omega$, f = 1 kHz
Unity Gain Frequency			6		MHz	
Over Operating Temperature Range						
Input Offset Voltage	V_{io}			5	mV	$R_S = 50\ \Omega$, $T_A = T_{opt}$
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		7		μV/°C	$T_A = T_{opt}$
Input Bias Current	I_b			7	nA	$T_A = T_{opt}$
Input Offset Current	I_{io}			2	nA	$T_A = T_{opt}$

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Power Dissipation, C Package (Note 1)	350 mW
Power Dissipation, G2 Package (Note 2)	440 mW
Differential Input Voltage	±30 V
Input Voltage (Note 3)	±15 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−55 to +125°C

Notes: 1. Thermal derating factor is 5 mW/°C when ambient temperature is higher than 55°C.
2. Thermal derating factor is 4.4 mW/°C when ambient temperature is higher than 25°C.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NEC

NEC Electronics Inc.

μPC4061
J-FET INPUT LOW-POWER OPERATIONAL AMPLIFIER

PRELIMINARY INFORMATION

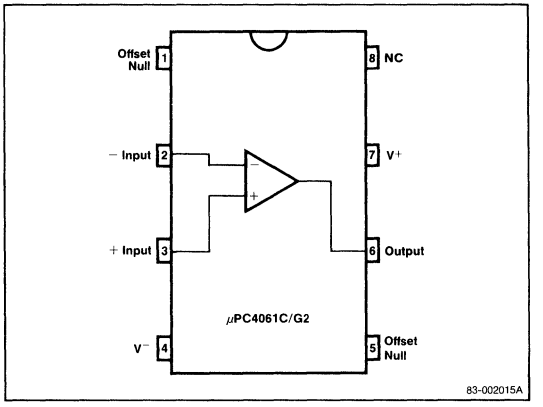
Description

The μPC4061 is a J-FET input low-power operational amplifier featuring low supply voltage operation from ±1.75 V. Supply current is ten times smaller than μPC4081 type J-FET input op-amp. With very low input bias current characteristics, the μPC4061 is an excellent choice for hand-held measurement equipment and other low-power application circuits.

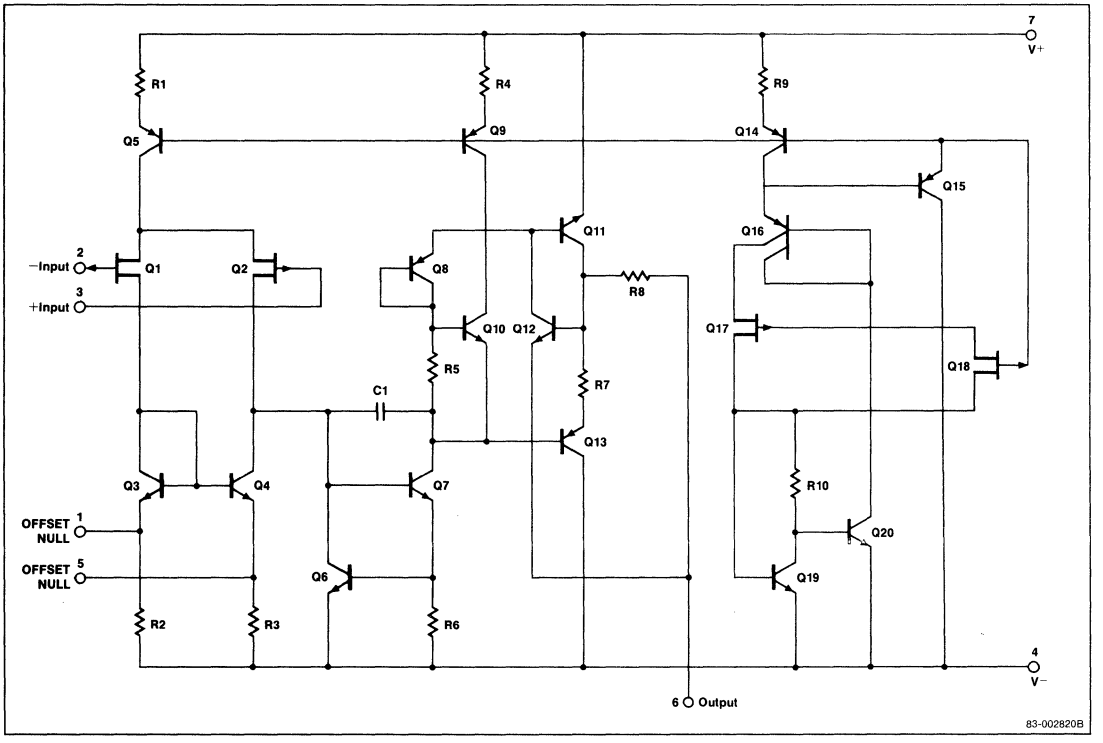
Features

- ☐ Low supply current: 230 μA
- ☐ Very low input bias and offset currents
- ☐ High slew rate: 3 V/μs
- ☐ High input impedance
- ☐ Low supply voltage operation
- ☐ Output short-circuit protection
- ☐ Internal frequency compensation
- ☐ TL061 direct replacement

Pin Configuration



Equivalent Circuit



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Ordering Information

Part Number	Package	Operating Temperature Range
μPC4061C	Plastic DIP	−20 to +70°C
μPC4061G2	Plastic Miniflat	−20 to +70°C

Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V±	±2		±16	V	
Output Current	I_O Source I_O Sink			5 3.5	mA	
Load Capacitance (Voltage Follower)	C_L			220	pF	

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Power Dissipation (Note 1), C Package	350 mW
Power Dissipation (Note 2), G2 Package	440 mW
Differential Input Voltage	±30 V
Input Voltage, (Note 3)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−55 to +125°C

Notes: 1. Derate at 5 mW/°C above 55°C.

2. Derate at 4.4 mW/°C above 25°C.

3. For $V\pm < \pm 15$ V, $V_{IN\ (max)} = V\pm$.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

$T_A = 25°C$, $V\pm = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{IO}		2	10	mV	$R_S = 50$
Input Offset Voltage	V_{IO}			15	mV	$R_S = 50$, $T_A = T_{OPT}$
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$		10		μV/°C	$R_S = 50$, $T_A = T_{OPT}$
Input Offset Current	I_{IO}		5	50	pA	
Input Offset Current	I_{IO}			1.5	nA	$T_A = T_{OPT}$
Input Bias Current	I_B		10	100	pA	
Input Bias Current	I_B			3	nA	
Large Signal Voltage Gain	A_{VOL}	69	75		dB	$R_{IN} = 10k$, $V_O = \pm 10$ V
Supply Current	I_{CC}		230	260	μA	
Common Mode Rejection Ratio	CMRR	70	95		dB	
Supply Voltage Rejection Ratio	SVRR	70	95		dB	
Output Voltage Swing	V_{om}	±12	±14		V	$R_{IN} = 10k$
Common Mode Input Voltage	V_{icm}	±12	+15, −13		V	
Output Current	I_O Source I_O Sink		+5 −3.5		mA	$V_{om} = \pm 10$ V
Slew Rate	SR		3		V/μs	$R_{IN} = 10k$
Input Noise Voltage	en		30		nV/√Hz	f = 1 kHz
Gain Bandwidth Products	GBW		1		MHz	
Over Operating Temperature Range						
Large Signal Voltage Gain	A_{VOL}	66			dB	$T_A = T_{OPT}$
Common Mode Rejection Ratio	CMRR	70	90		dB	$T_A = T_{OPT}$
Supply Voltage Rejection Ratio	SVRR	70	90		dB	$T_A = T_{OPT}$
Output Voltage Swing	V_{om}	±3.8	±4.1		V	$R_{IN} = 10k$, $T_A = T_{OPT}$
Common Mode Input Voltage	V_{icm}	+4.7 −2.8	+5.2 −3.5		V	$T_A = T_{OPT}$

μPC4071
J-FET INPUT LOW-NOISE OPERATIONAL AMPLIFIER

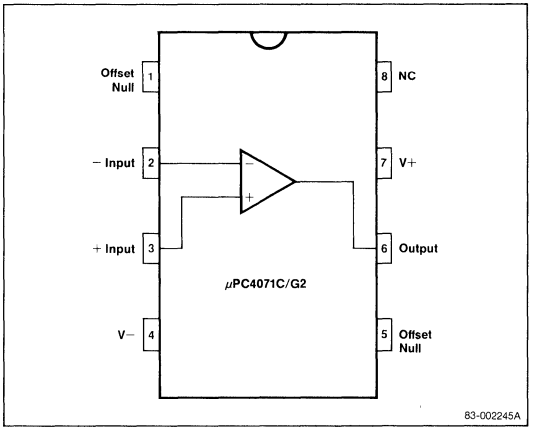
Description

The J-FET input operational amplifier of the μPC4071 is designed as low-noise versions of the μPC4081. The features of the μPC4071 have more improved input equivalent noise voltage, input offset voltage, and input bias current, than those of the μPC4081. The μPC4071 is an excellent choice for a wide variety of applications, including preamplifier and active filter circuits.

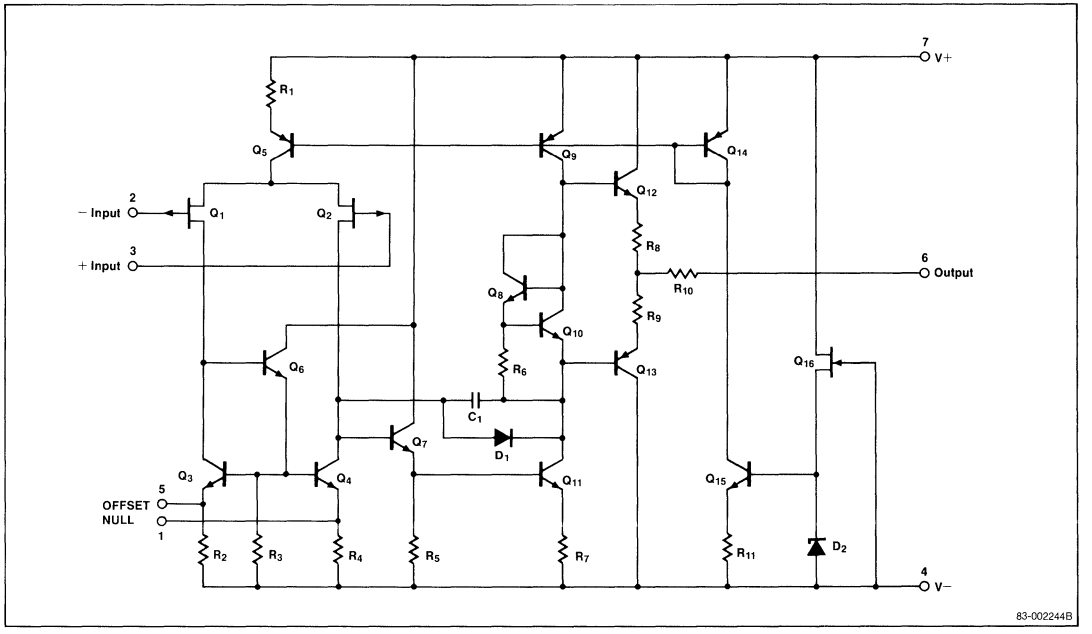
Features

- ☐ Low noise: $e_n = 18\ nV/\sqrt{Hz}$
- ☐ Low input bias and offset currents
- ☐ Output short-circuit protection
- ☐ High input impedance: J-FET input stage
- ☐ Internal frequency compensation
- ☐ High slew rate: $13\ V/\mu s$
- ☐ Latch-free operation
- ☐ TL071 direct replacement

Pin Configuration



Equivalent Circuit



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Ordering Information

Part Number	Package	Operating Temperature Range
μPC4071C	Plastic DIP	0° to +70°C
μPC4071G2	Plastic Miniflat	0° to +70°C

Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V±	±5		±16	V	
Capacitive Load ($A_V = +1$)	C_L			100	pF	
Output Current	I_O			10	mA	

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Differential Input Voltage	±30 V
Input Voltage (see Note 1)	±15 V
Power Dissipation, C Package	350 mW
Power Dissipation, G2 Package	440 mW
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

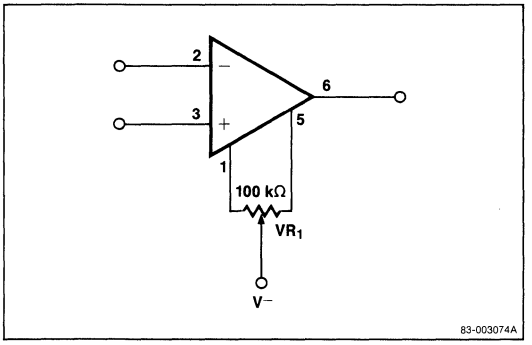
$T_A = 25°C$, $V± = ±15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		3	10.0	mV	$R_S \leq 50\ \Omega$
Input Offset Current	I_{io}		5	50	pA	$T_A = 25°C$ (see Note 1)
Input Bias Current	I_b		30	200	pA	$T_A = 25°C$ (see Note 1)
Large Signal Voltage Gain	A_{VOL}	88	106		dB	$R_L \geq 2\ k\Omega$, $V_O = ±10$ V
Supply Current	I_{CC}		2.0	2.7	mA	
Common Mode Rejection Ratio	CMRR	70	86		dB	
Supply Voltage Rejection Ratio	SVRR	70	86		dB	
Output Voltage Swing	V_{om}	±12	±13.5		V	$R_L \geq 10\ k\Omega$
Output Voltage Swing	V_{om}	±10	±12		V	$R_L \geq 2\ k\Omega$
Common Mode Input Voltage Range	V_{icm}	±10			V	
Slew Rate	SR		13		V/μs	$A_V = 1$
Input Noise Voltage	en		18		$nV/\sqrt{Hz}$	$R_S = 100\ \Omega$, f = 1 kHz
			4		μV_{RMS}	$R_S = 100\ \Omega$, f = 10 Hz to 10 kHz
Unity Gain Bandwidth	GBW		3		MHz	
Over Operating Temperature						
Input Offset Voltage	V_{io}			13	mV	$R_S \leq 50\ \Omega$, $T_A = T_{OPT}$
Average Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		10		μV/°C	$T_A = T_{OPT}$
Input Bias Current	I_b			7	nA	$T_A = T_{OPT}$
Input Offset Current	I_{io}			2	nA	$T_A = T_{OPT}$

Note: 1. Input bias currents are temperature sensitive. Short time measuring method is recommended to maintain the junction temperature close to the ambient temperature.

Typical Application

Offset Voltage Null Circuit



Operating Characteristics

$T_A = 25°C$

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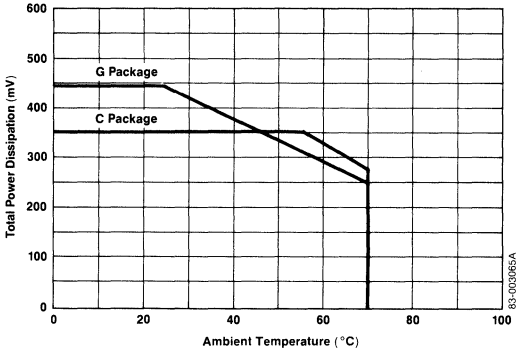
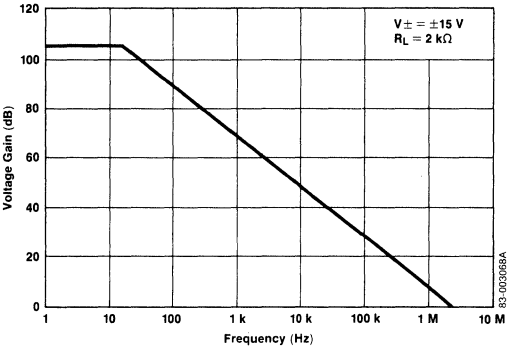
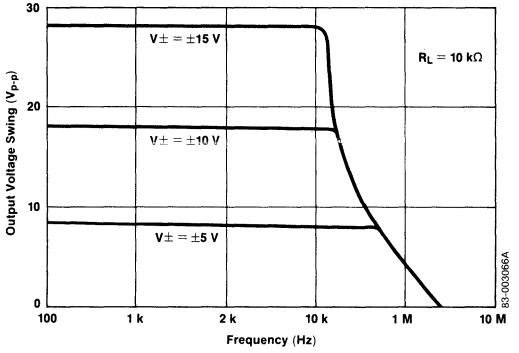
Power Dissipation



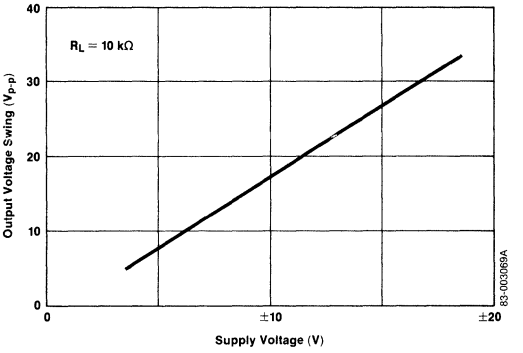
Open Loop Frequency Response



Large Signal Frequency Response



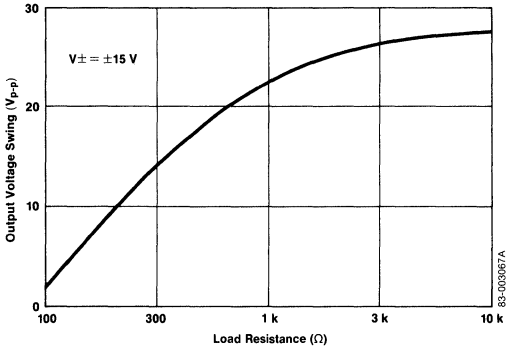
Output Voltage Swing



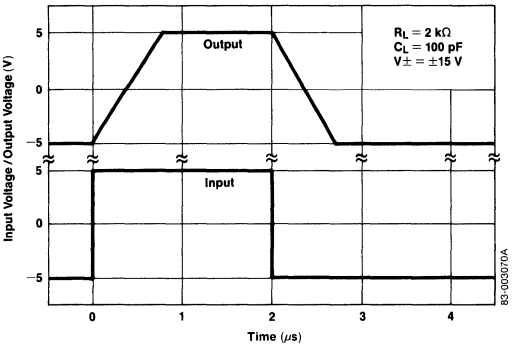
Operating Characteristics (Cont.)

$T_A = 25°C$

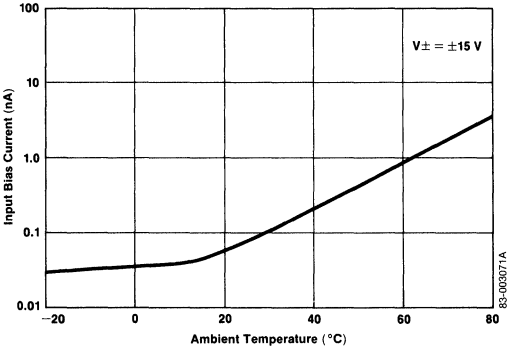
Output Voltage Swing



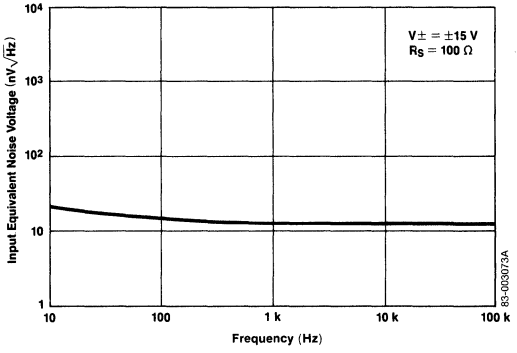
Voltage Follower Pulse Response



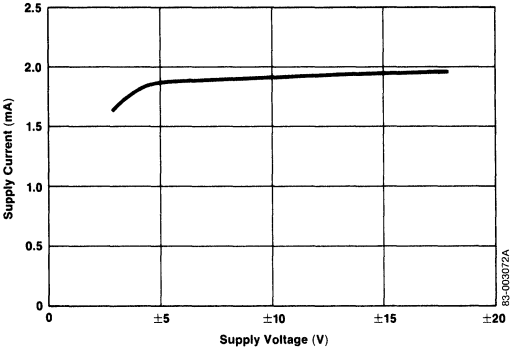
Input Bias Current



Input Equivalent Noise Voltage



Supply Current



μPC4081
J-FET INPUT OPERATIONAL AMPLIFIER

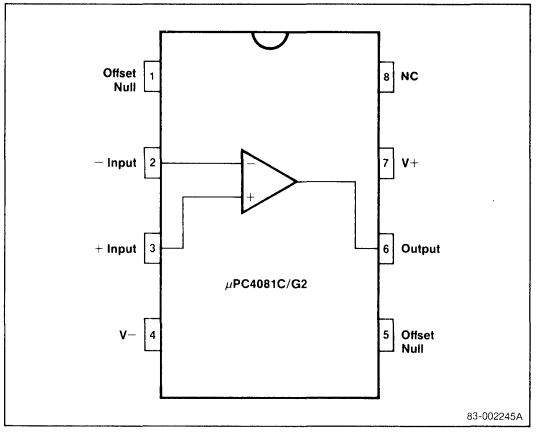
Description

The μPC4081 is a single operational amplifier with a combination of matched ion implanted P-channel J-FET inputs with standard bipolar transistor technology. The very low-input bias current and high slew rate (ten times that of general purpose operational amplifiers) makes this device an excellent choice for integrators, active filters, and pulse amplifier applications.

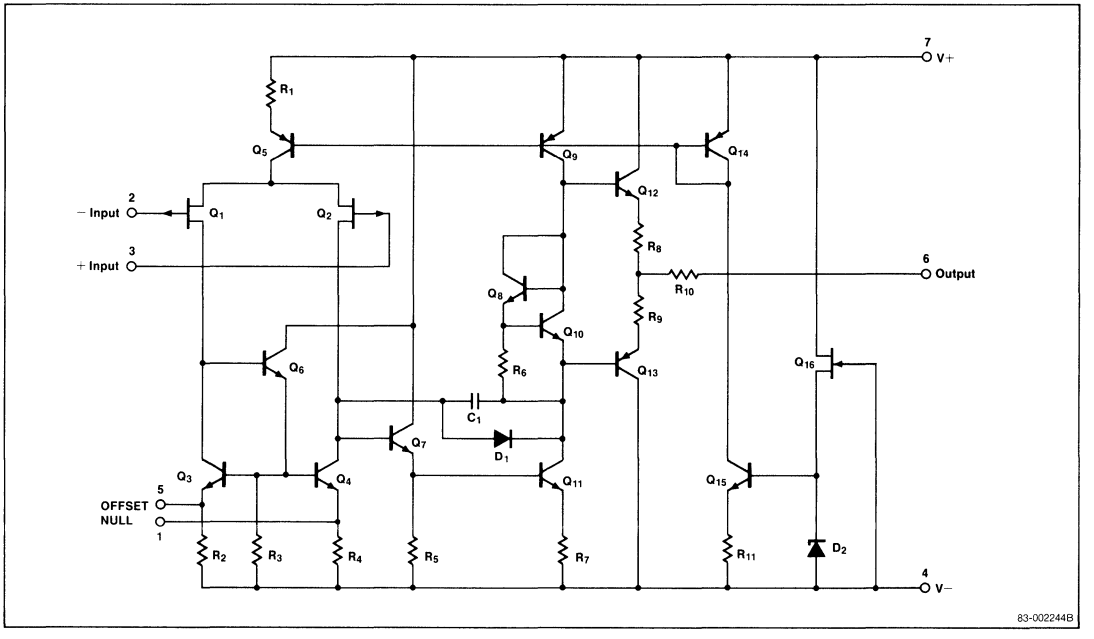
Features

- ☐ Wide common-mode and differential input voltage range
- ☐ Low input bias and offset currents
- ☐ Output short-circuit protection
- ☐ High input impedance: J-FET input stage
- ☐ Internal frequency compensation
- ☐ High slew rate: 11 V/μs typical
- ☐ Latch-free operation
- ☐ TL081 direct replacement

Pin Configuration



Equivalent Circuit



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Electrical Characteristics

$T_A = 25°C$, $V^{\pm} = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		5.0	15.0	mV	$R_S \leq 50\ \Omega$
Input Offset Current	I_{io}		5	200	pA	
Input Bias Current	I_b		30	400	pA	
Large Signal Voltage Gain	A_{VOL}	88	106		dB	$RL \geq 2$ kΩ, $V_O = \pm 10$ V
Supply Current	I_{CC}		2.0	2.8	mA	
Common Mode Rejection Ratio	CMRR		70	76	dB	
Supply Voltage Rejection Ratio	SVRR		70	76	dB	
Output Voltage Swing	V_{OM}	±12	±13.5		V	$R_L \geq 10$ kΩ
Output Voltage Swing	V_{OM}	±10	±12		V	$R_L \geq 2$ kΩ
Common Mode Input Voltage Swing	V_{icm}		±10		V	
Slew Rate	SR		11		V/μs	$Av = 1$
Input Equivalent Noise Voltage	en		25		$nV/\sqrt{Hz}$	f = 1 kHz, $R_S = 100\ \Omega$
Unity Gain Bandwidth	GBW		3		MHz	
Over Operating Temperature						
Input Offset Voltage	V_{io}			20	mV	$R_S \leq 50\ \Omega$, $T_A = T_{OPT}$
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		10		μV/°C	$T_A = T_{OPT}$
Input Bias Current	I_b			10	nA	$T_A = T_{OPT}$
Input Offset Current	I_{io}			5	nA	$T_A = T_{OPT}$

Ordering Information

Part Number	Package	Operating Temperature Range
μPC4081C	Plastic DIP	0°C to +70°C
μPC4081G2	Plastic Miniflat	0°C to +70°C

Absolute Maximum Ratings

$T_A = 25°C$

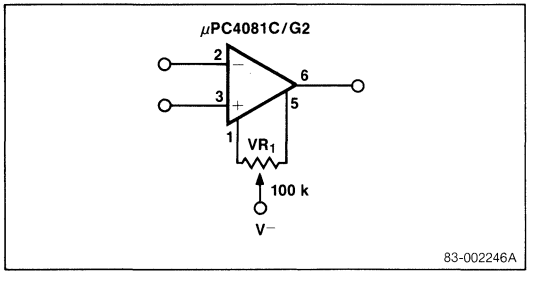
Voltage Between V^+ and V^-	36 V
Power Dissipation, C Package	350 mW
Power Dissipation (Note 1), G2 Package	440 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Notes: 1. For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Typical Applications

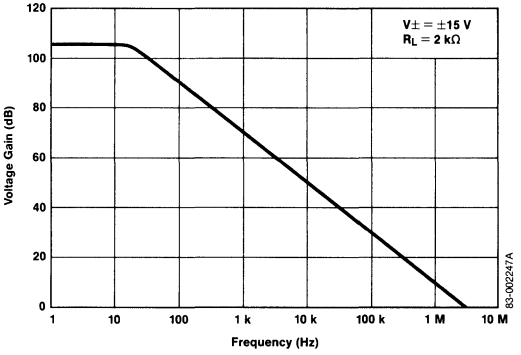
Offset Voltage Null Circuit



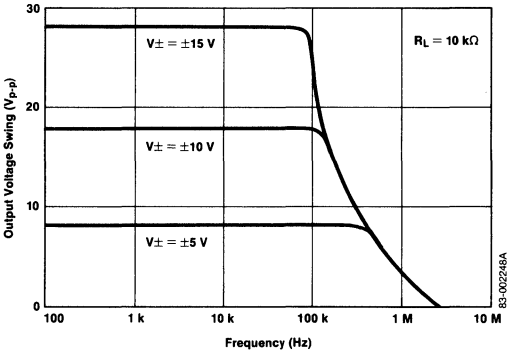
Operating Characteristics

$T_A = 25°C$

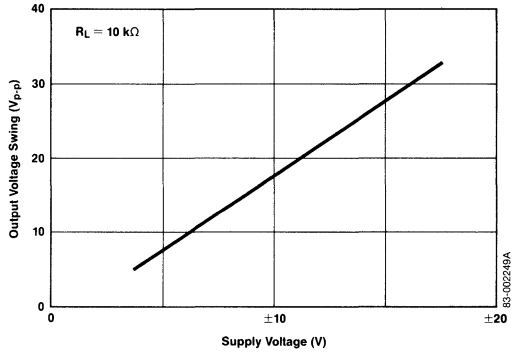
Open Loop Frequency Response



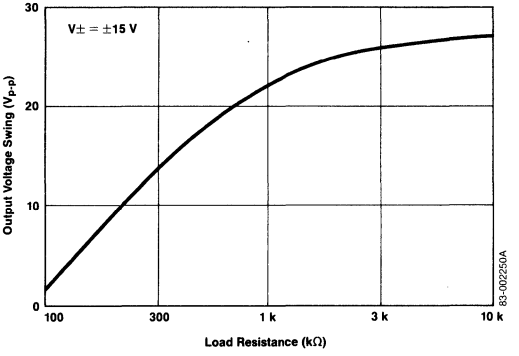
Large Signal Frequency Response



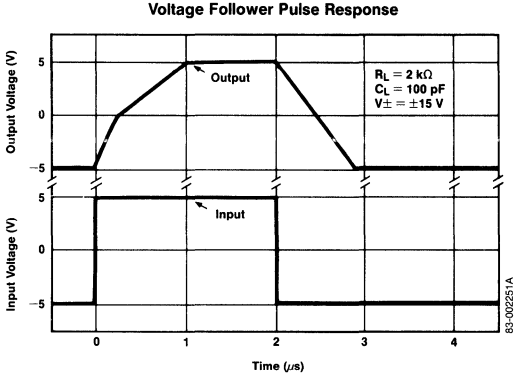
Output Voltage Swing



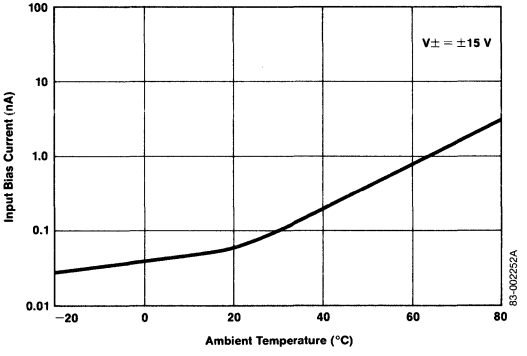
Output Voltage Swing



Voltage Follower Pulse Response



Input Bias Current



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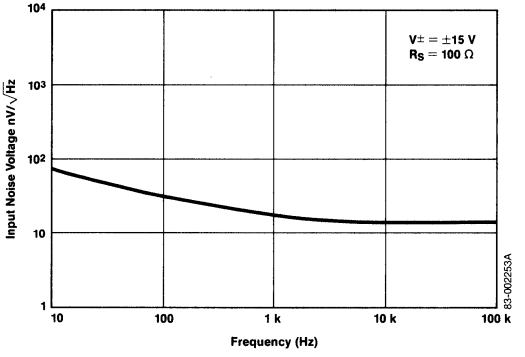
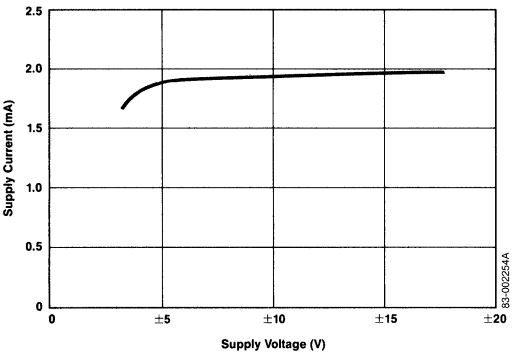
Operating Characteristics (Cont.)

$T_A = 25°C$

Input Equivalent Noise Voltage



Supply Current



NEC
NEC Electronics Inc.

μPC4250
PROGRAMMABLE OPERATIONAL AMPLIFIER

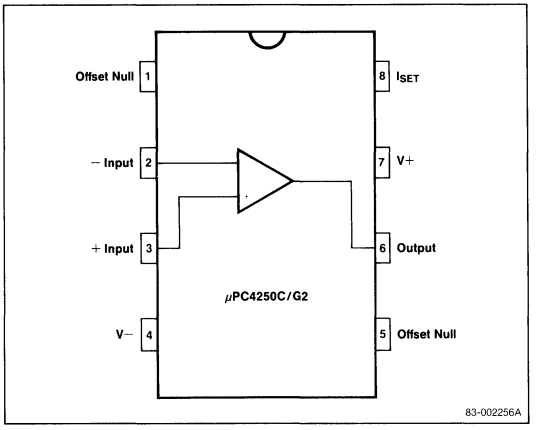
Description

The μPC4250 is a very versatile monolithic operational amplifier. The quiescent power dissipation, input offset and bias current, slew rate, and gain bandwidth product are determined by a single external programming resistor. Because this device is individually programmable, a large variety of circuit functions can be realized by stocking a single operational amplifier type. In addition, this device operates from as little as ±1 V, making it ideal for portable applications.

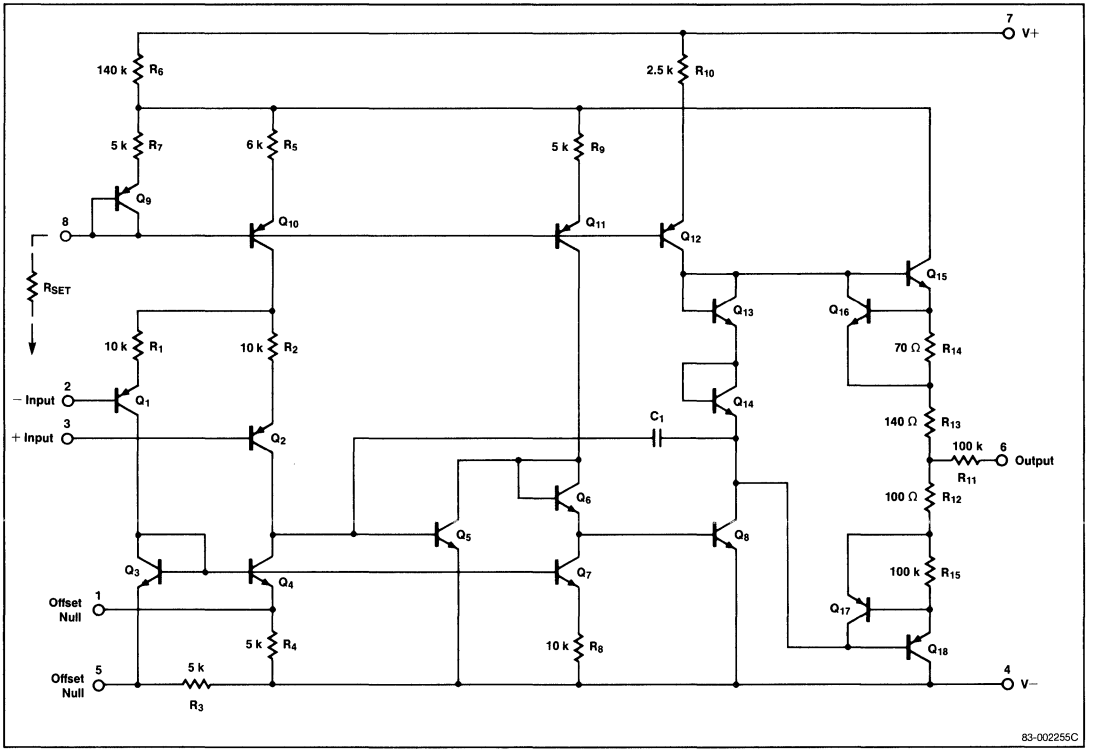
Features

- ☐ ±1 V to ±18 V power supply operation
- ☐ Standby power consumption as low as 500 nW
- ☐ Programmable electrical characteristics
- ☐ Internal frequency compensation
- ☐ Offset-voltage nulling capability
- ☐ Short-circuit protection
- ☐ LM4250 direct replacement

Pin Configuration



Equivalent Circuit



Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V^+ and V^-	36 V
Power Dissipation, C Package	350 mW
Power Dissipation, G2 Package	440 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
I_{SET} Current	150 μA
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ordering Information

Part Number	Package	Operating Temperature Range
μPC4250C	Plastic DIP	0°C to +70°C
μPC4250G2	Plastic Miniflat	0°C to +70°C

Electrical Characteristics

$T_A = 25°C$, $V^{\pm} = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{IO}			5	mV	$I_{SET} = 1$ μA, $R_S \leq 100$ kΩ
				5	mV	$I_{SET} = 1$ μA, $V^{\pm} = \pm 1.5$ V, $R_S \leq 100$ kΩ
				6	mV	$I_{SET} = 10$ μA, $R_S \leq 100$ kΩ
				6	mV	$I_{SET} = 10$ μA, $V^{\pm} = \pm 1.5$ V, $R_S \leq 100$ kΩ
Input Offset Current	I_{IO}			6	nA	$I_{SET} = 1$ μA
				20	nA	$I_{SET} = 10$ μA
Input Bias Current	I_B			10	nA	$I_{SET} = 1$ μA
				10	nA	$I_{SET} = 1$ μA, $V^{\pm} = \pm 1.5$ V
				75	nA	$I_{SET} = 10$ μA
				75	nA	$I_{SET} = 10$ μA, $V^{\pm} = \pm 1.5$ V
Voltage Gain	A_{VOL}	95			dB	$I_{SET} = 1$ μA, $V_O = \pm 10$ V, $R_L = 100$ kΩ
		95			dB	$I_{SET} = 10$ μA, $V_O = \pm 10$ V, $R_L = 10$ kΩ
Supply Current	I_{CC}			11	μA	$I_{SET} = 1$ μA
				8	μA	$I_{SET} = 1$ μA, $V^{\pm} = \pm 1.5$ V
				100	μA	$I_{SET} = 10$ μA
				90	μA	$I_{SET} = 10$ μA, $V^{\pm} = \pm 1.5$ V
Power Dissipation	P_D			330	μW	$I_{SET} = 1$ μA
				24	μW	$I_{SET} = 1$ μA, $V^{\pm} = \pm 1.5$ V
				3,000	μW	$I_{SET} = 10$ μA
				270	μW	$I_{SET} = 10$ μA, $V^{\pm} = \pm 1.5$ V

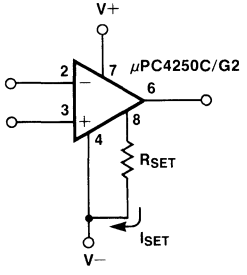
Electrical Characteristics (Cont.)

$T_A = 25°C$, $V^{\pm} = \pm 15$ V

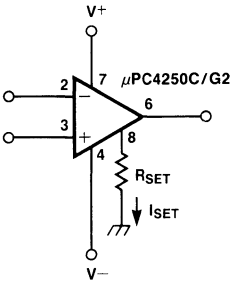
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage Range	V_{icm}	±13.5			V	$I_{SET} = 1\ \mu A$
		±0.6			V	$I_{SET} = 1\ \mu A$, $V^{\pm} = \pm 1.5$ V
		±13.5			V	$I_{SET} = 10\ \mu A$
		±0.6			V	$I_{SET} = 10\ \mu A$, $V^{\pm} = \pm 1.5$ V
Output Voltage Swing	V_{om}	±12			V	$I_{SET} = 1\ \mu A$, $R_L = 100\ k\Omega$
		±0.6			V	$I_{SET} = 1\ \mu A$, $V^{\pm} = \pm 1.5$ V, $R_L = 100\ k\Omega$
		±12			V	$I_{SET} = 10\ \mu A$, $R_L = 10\ k\Omega$
		±0.6			V	$I_{SET} = 10\ \mu A$, $V^{\pm} = \pm 1.5$ V, $R_L = 10\ k\Omega$
Common Mode Rejection Ratio	CMRR	70			dB	$I_{SET} = 1\ \mu A$, $R_S \leq 10\ k\Omega$
		70			dB	$I_{SET} = 10\ \mu A$, $R_S \leq 10\ k\Omega$
Supply Voltage Rejection Ratio	SVRR	74			dB	$I_{SET} = 1\ \mu A$, $R_S \leq 10\ k\Omega$
		74			dB	$I_{SET} = 10\ \mu A$, $R_S \leq 10\ k\Omega$

3

Typical Application



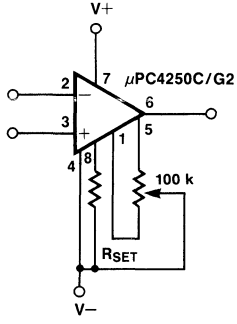
$$I_{SET} = \frac{V^+ + |V^-| - 0.5}{R_{SET}}$$



$$I_{SET} \approx \frac{V^+ - 0.5}{R_{SET}}$$

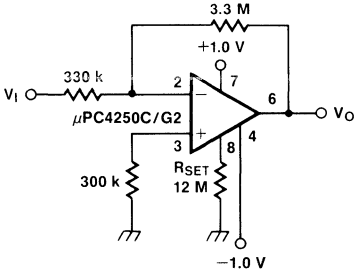
83-002257B

Offset Null Circuit



83-002258A

500 Nano-Watt x 10 Amplifier

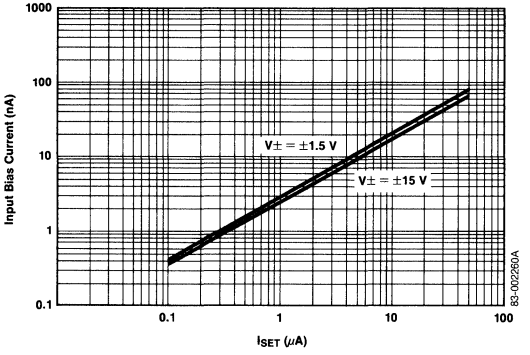


83-002259A

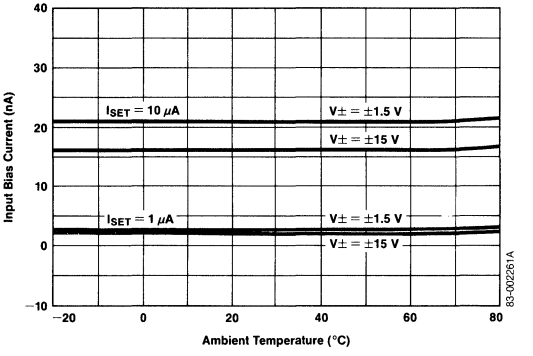
Operating Characteristics

$T_A = 25°C$

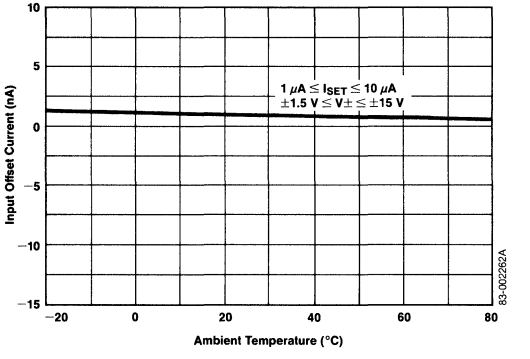
Input Bias Current



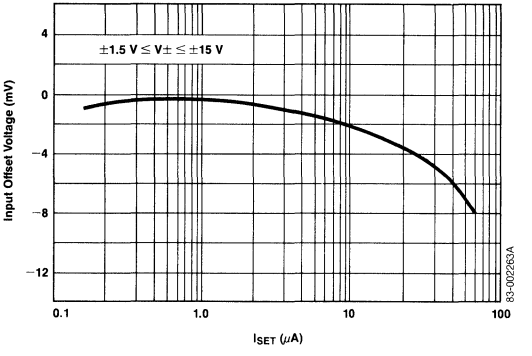
Input Bias Current



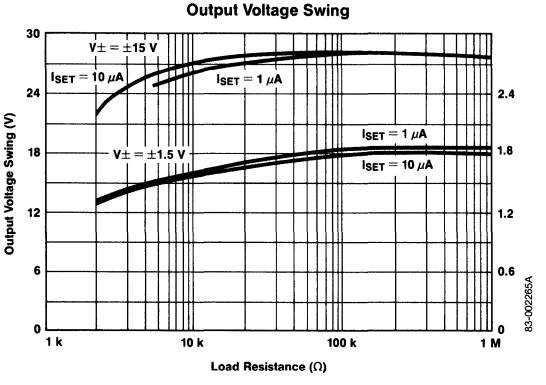
Input Offset Current



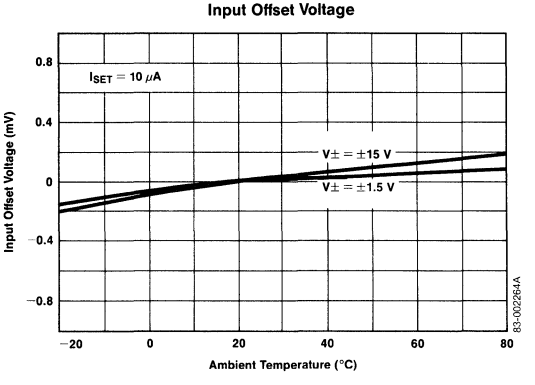
Input Offset Voltage



Output Voltage Swing



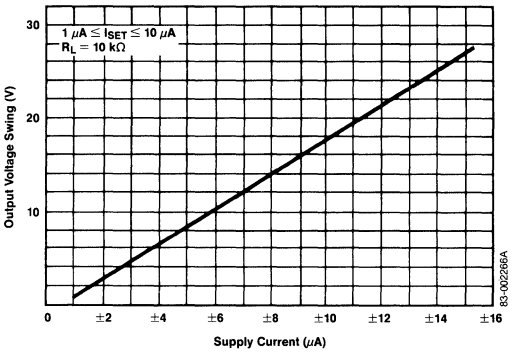
Input Offset Voltage



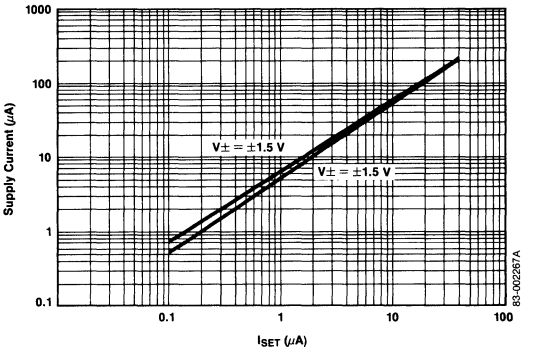
Operating Characteristics (Cont.)

$T_A = 25°C$

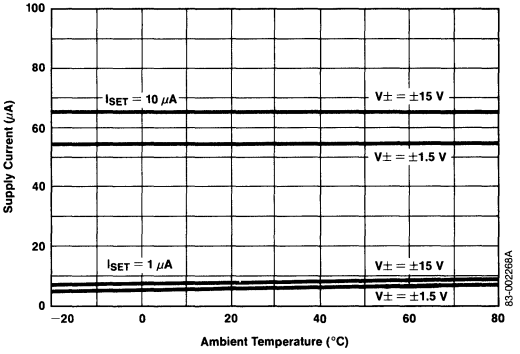
Output Voltage Swing



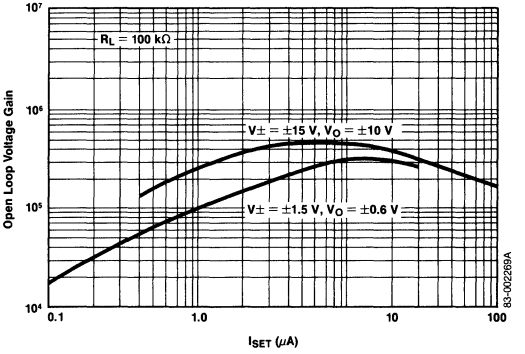
Supply Current



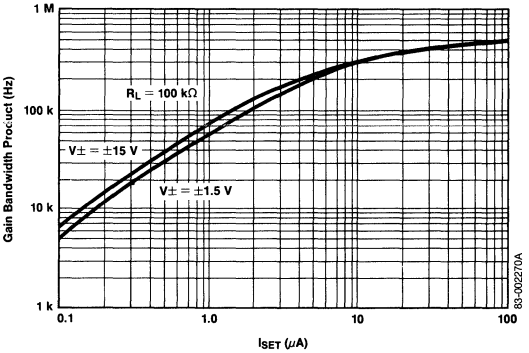
Supply Current



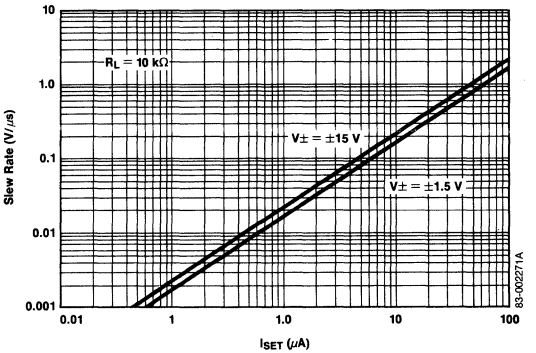
Open Loop Voltage Gain



Gain Bandwidth Product



Slew Rate



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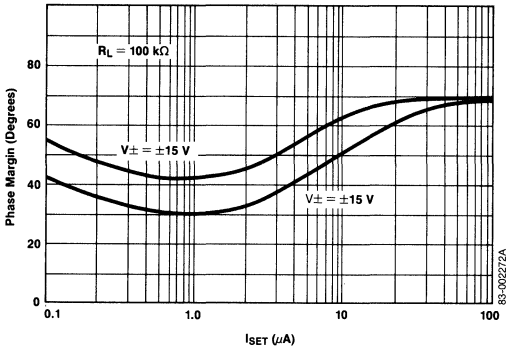
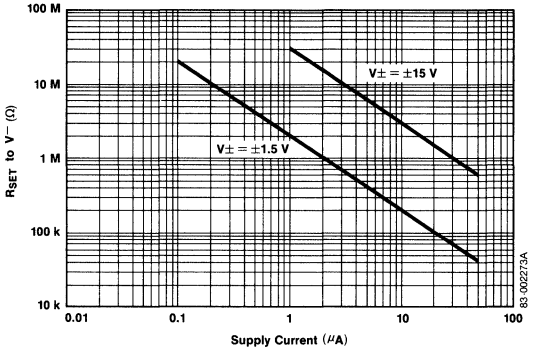
Operating Characteristics (Cont.)

$T_A = 25°C$

Phase Margin



R_{SET}



μPC358
DUAL LOW-POWER OPERATIONAL AMPLIFIER

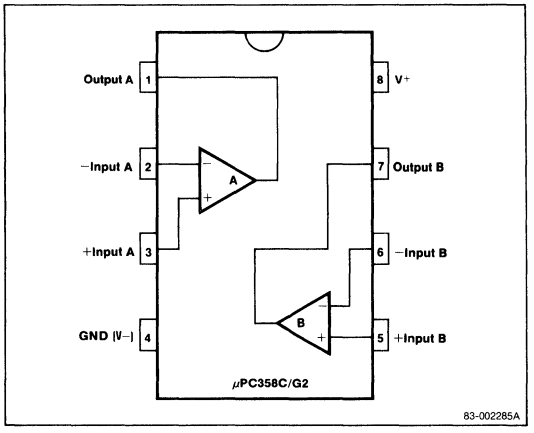
Description

The μPC358 is designed to operate from a single power supply, with the option to operate from split power supplies. This amplifier offers the circuit designer low power supply current drain, input common mode voltage, and large output voltage swing both of which include ground.

Features

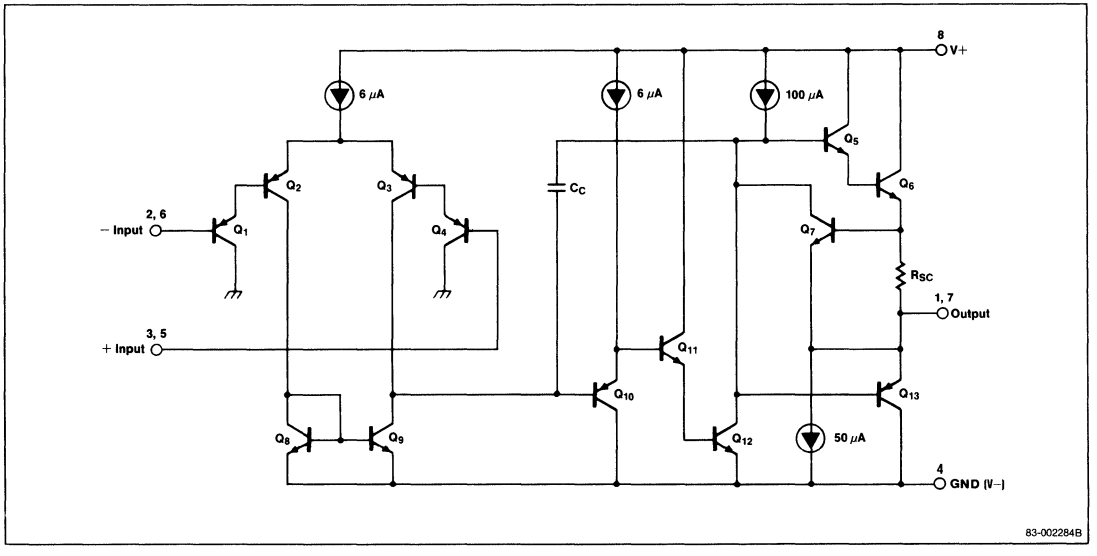
- ☐ Internal frequency compensation
- ☐ Large output voltage swing: 0 V to (V+ − 1.5 V)
- ☐ Input common-mode voltage range includes ground
- ☐ Wide power supply range: single supply 3 V to 30 V DC
- ☐ Dual supplies: ±1.5 V to ±15 V DC
- ☐ LM358 direct replacement

Pin Configuration



Equivalent Circuit

1/2 Circuit



3

Ordering Information

Part Number	Package	Operating Temperature Range
μPC358C	Plastic DIP	0°C to +70°C
μPC358G2	Plastic Miniflat	0°C to +70°C

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	32 V
Differential Input Voltage	32 V
Input Voltage	−0.3 to +32 V
Power Dissipation, C Package	350 mW
Power Dissipation, G2 Package	440 mW
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

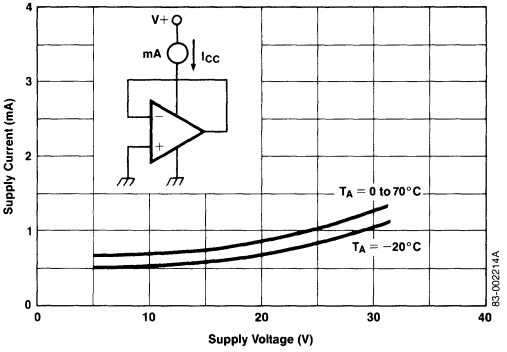
$T_A = 25°C$, $V\pm = \pm 15$ V,

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		2	7	mV	$R_S \leq 0\ \Omega$
Input Bias Current	I_b		45	250	nA	
Input Offset Current	I_{io}		5	50	nA	
Common Mode Input Voltage Range	V_{icm}	0		V+ − 1.5	V	
Supply Current	I_{CC}		0.7	1.2	mA	$R_L = \infty$
Voltage Gain	A_{VOL}	88	100		dB	$R_L \geq 2$ kΩ
Output Voltage Swing	V_{OM}	0		V+ − 1.5	V	$R_L \geq 2$ kΩ
Common Mode Rejection Ratio	CMRR	65	70		dB	
Supply Voltage Rejection Ratio	SVRR	65	100		dB	
Channel Separation	CS		120		db	f = 1 kHz to 20 kHz
Output Current (Source)	$I_{O\ SOURCE}$	20	40		mA	+Input = 1 V −Input = 0 V
Output Current (Sink)	$I_{O\ SINK}$	10	20		mA	+Input = 1 V −Input = 0 V
		12	50		μA	+Input = 1 V −Input = 0 V V_O = 200 mV

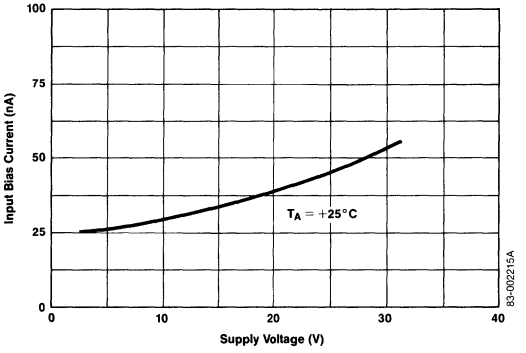
Operating Characteristics

$T_A = 25°C$

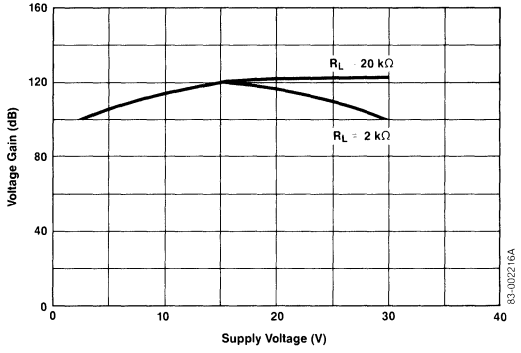
Supply Current



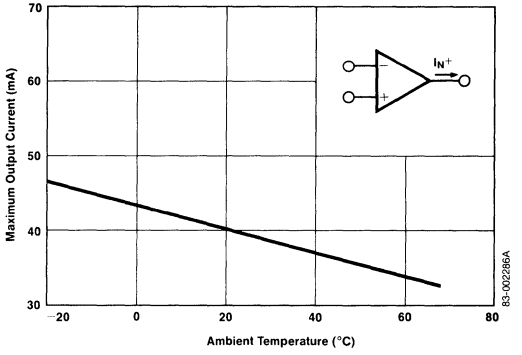
Input Bias Current



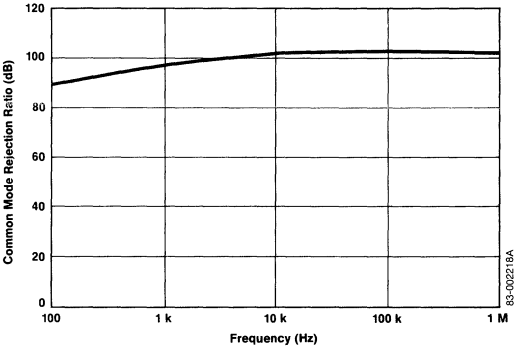
Voltage Gain



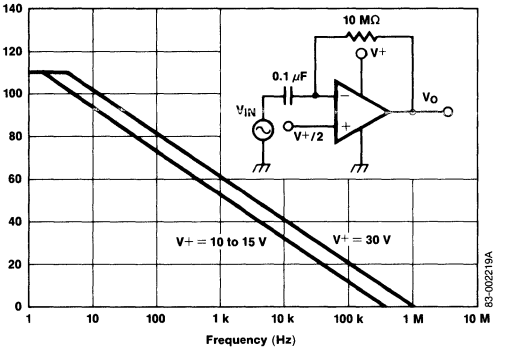
Current Limiting



Common Mode Rejection Ratio



Open Loop Frequency Response

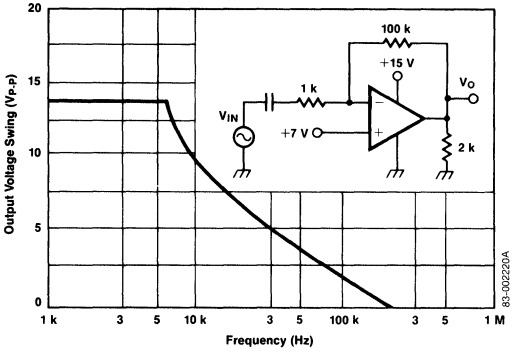


3

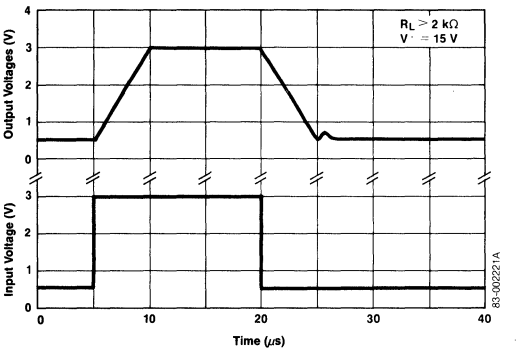
Operating Characteristics (Cont.)

$T_A = 25°C$

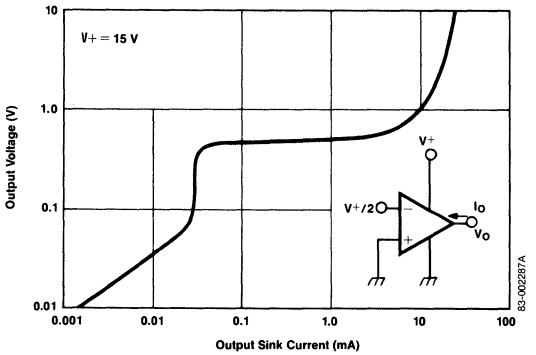
Large Signal Frequency Response



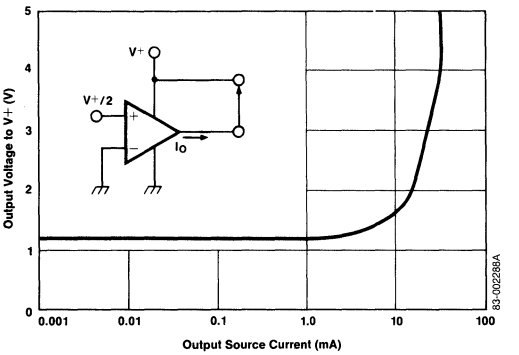
Voltage Follower Large Signal Pulse Response



Current Sinking



Current Sourcing



NEC

NEC Electronics Inc.

μPC812
DUAL J-FET INPUT LOW-OFFSET OPERATIONAL AMPLIFIER

PRELIMINARY INFORMATION

Description

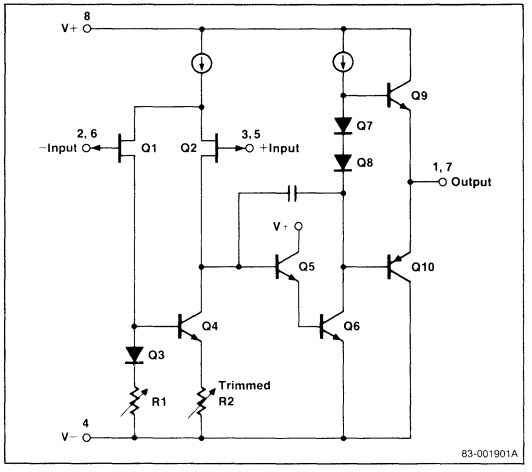
Dual operational amplifier μPC812 offers high input impedance, low offset voltage, high slew rate, and stable ac operating characteristics. NEC's unique high-speed pnp transistor ($f_T = 300$ MHz) in the output stage solves the oscillation problem of current sinking with a large capacitive load. Zener-zap resistor trimming in the input stage produces excellent offset voltage and temperature drift characteristics.

Features

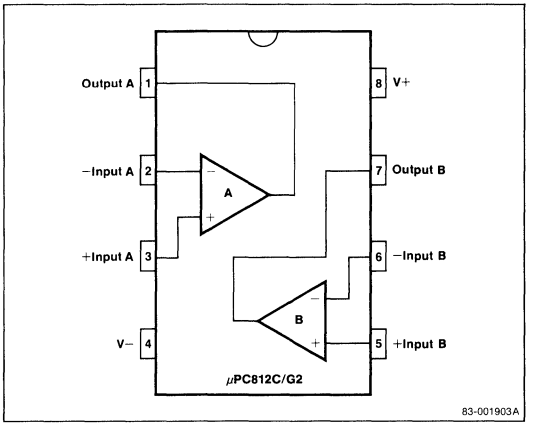
- ☐ Stable operation with 10,000pF capacitive load
- ☐ Low input offset voltage:
  - 3 mV max
  - 7 μV/°C temperature drift
- ☐ Low input bias and offset currents
- ☐ Low noise: en = 20 nV/$\sqrt{Hz}$
- ☐ Output short-circuit protection
- ☐ High input impedance
- ☐ Internal frequency compensation
- ☐ High slew rate: 15 V/μs

Equivalent Circuit

1/2 Circuit



Pin Configuration



Ordering Information

Part Number	Package	Operating Temperature Range
μPC812C	8-Pin Plastic DIP	−20 to +70 °C
μPC812G2	8-Pin Plastic Miniflat	−20 to +70 °C

3

Absolute Maximum Ratings

$T_A = 25°C$

Parameter	Symbol	μPC812C	μPC812G2	Unit
Voltage Between V+ and V−	V+ − V−	36	36	V
Power Dissipation	P_D	350 (Note 1)	440 (Note 2)	mW
Differential Input Voltage	V_{id}	±30	±30	V
Common Mode Input Voltage (Note 3)	V_{icm}	±15	±15	V
Output Short Circuit Duration		Indefinite	Indefinite	s
Operating Temperature Range	T_{opt}	−20 to +70	−20 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	−55 to +125	°C

Note: 1. Thermal derating factor is 5 mW/°C when ambient temperature is higher than 55°C.
2. Thermal derating factor is 4.4 mW/°C when ambient temperature is higher than 25°C.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V±	±5		±16	V
Capacitive Load	C_L			10,000	pF
Output Current	I_O			10	mA

Electrical Characteristics

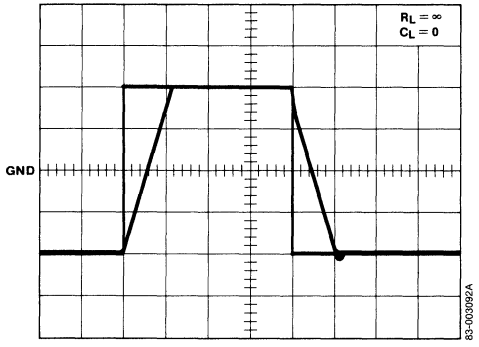
$T_A = 25°C$, $V± = ±15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		1	3.0	mV	$R_S = 50\ \Omega$
Input Offset Current	I_{io}		25	100	pA	$T_J = 25°C$
Input Bias Current	I_b		50	200	pA	$T_J = 25°C$
Voltage Gain	A_{VOL}	80	106		dB	$R_L = 2\ k\Omega$, $V_O = ±10$ V
Supply Current	I_{CC}		5	6.8	mA	Both channels
Common Mode Rejection Ratio	CMRR	70	100		dB	
Supply Voltage Rejection Ratio	SVRR	70	100		dB	
Output Voltage Swing	V_{om}	±12	±13.5		V	$R_L = 10\ k\Omega$
Output Voltage Swing	V_{om}	±10	±12		V	$R_L = 2\ k\Omega$
Input Voltage Range	V_{icm}	±11			V	
Slew Rate			15		V/μs	$A_V = +1$
Input Noise Voltage	en		20		$nV/\sqrt{Hz}$	$R_S = 100\ \Omega$, f = 1 kHz
Unity Gain Frequency			4		MHz	
Channel Separation	CS		120		dB	f = 1 Hz to 20 kHz
Over Operating Temperature						
Input Offset Voltage	V_{io}			5	mV	$R_S = 50\ \Omega$, $T_A = T_{opt}$
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		7		μV/°C	$T_A = T_{opt}$
Input Bias Current	I_b			7	nA	$T_A = T_{opt}$
Input Offset Current	I_{io}			2	nA	$T_A = T_{opt}$

Operating Characteristics

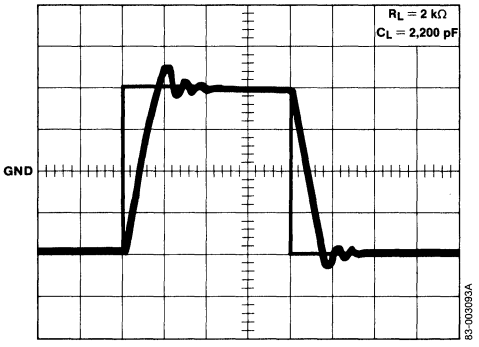
$T_A = 25°C$

Voltage Follower Pulse Response



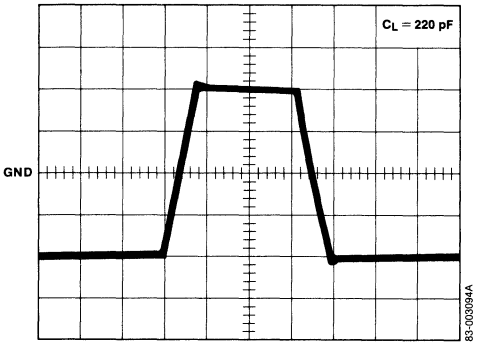
5 V/div Vertical
1 μs/div Horizontal

Voltage Follower Pulse Response



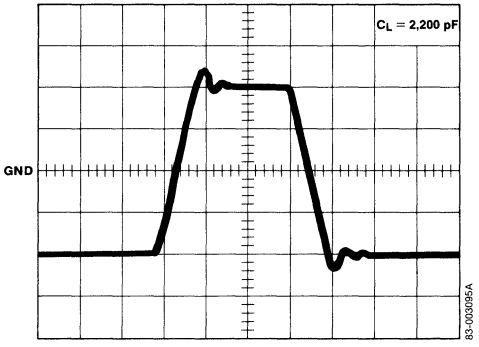
5 V/div Vertical
2 μs/div Horizontal

Voltage Follower Pulse Response



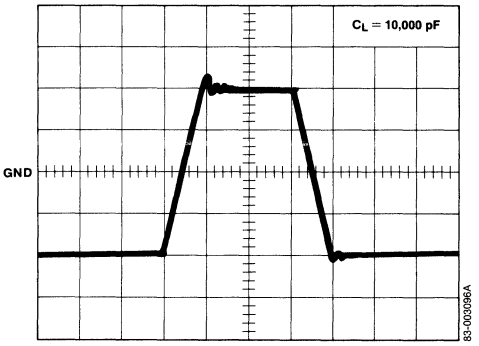
5 V/div Vertical
2 μs/div Horizontal

Voltage Follower Pulse Response



5 V/div Vertical
8 μs/div Horizontal

Voltage Follower Pulse Response



5 V/div Vertical
10 μs/div Horizontal

3

NEC

NEC Electronics Inc.

μPC814
DUAL J-FET INPUT LOW-OFFSET OPERATIONAL AMPLIFIER

PRELIMINARY INFORMATION

Description

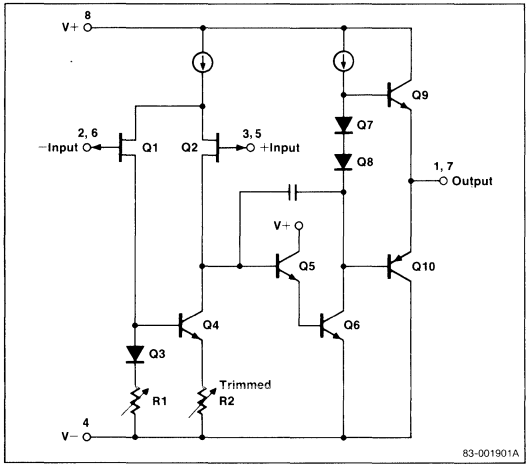
Dual operational amplifier μPC814 is a high-speed version of the μPC812. NEC's unique high-speed pnp transistor (f_T = 300 MHz) in the output stage yields a high slew rate of 25 V/μs under voltage-follower conditions without an oscillation problem. Zener-zap resistor trimming in the input stage produces excellent offset voltage and temperature drift characteristics.

Having ac performance characteristics that are two times better than conventional bi-FET op amps, the μPC814 is ideal for fast integrators, active filters, and other high-speed circuit applications.

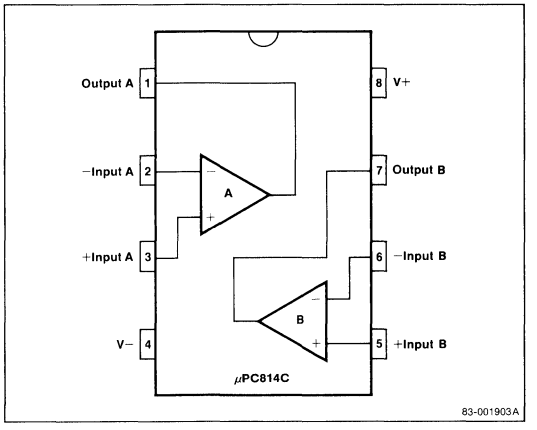
Features

- ☐ High slew rate: 25 V/μs
- ☐ Stable operation with 220-pF capacitive load
- ☐ Low input offset voltage:
  - —3 mV max
  - —7 μV/°C temperature drift
- ☐ Low input bias and offset currents
- ☐ Low noise: en = 20 nV/$\sqrt{Hz}$
- ☐ Output short-circuit protection
- ☐ High input impedance
- ☐ Internal frequency compensation

Equivalent Circuit *(1/2 Circuit)*



Pin Configuration



Ordering Information

Part Number	Package	Operating Temperature Range
μPC814C	8-Pin Plastic DIP	−20 to +70°C

3

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Power Dissipation	350 mW
Differential Input Voltage	±30 V
Common Mode Input Voltage (Note 1)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−55 to +125°C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Paramater	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V±	±5		±16	V
Capacitive Load	C_L			220	pF
Output Current	I_O			10	mA

Electrical Characteristics

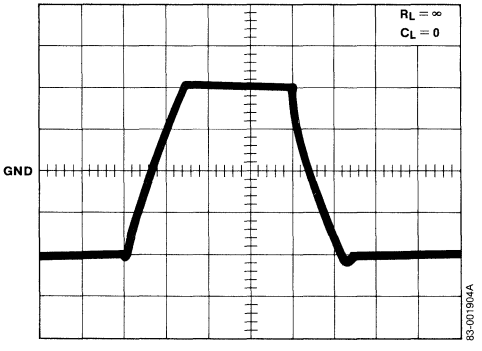
$T_A = 25°C$, V± = ±15 V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		1	3	mV	$R_S = 50\ \Omega$
Input Offset Current	I_{io}		25	100	pA	$T_A = 25°C$
Input Bias Current	I_b		50	200	pA	$T_A = 25°C$
Voltage Gain	A_{VOL}	88	106		dB	$R_L = 2\ k\Omega$, $V_O = \pm 10$ V
Supply Current	I_{CC}		5	6.8	mA	Both channels
Common Mode Rejection Ratio	CMRR	70	100		dB	
Supply Voltage Rejection Ratio	SVRR	70	100		dB	
Output Voltage Swing	V_{om}	±12	±13.5		V	$R_L = 10\ k\Omega$
Output Voltage Swing	V_{om}	±10	±12		V	$R_L = 2\ k\Omega$
Input Voltage Range	V_{icm}	±11			V	
Slew Rate			25		V/μs	$A_V = +1$
Input Noise Voltage	en		20		nV/√Hz	$R_S = 100\ \Omega$, f = 1 kHz
Unity Gain Frequency			6		MHz	
Channel Separation	CS		120		dB	f = 1 Hz to 20 kHz
Over Operating Temperature						
Input Offset Voltage	V_{io}			5	mV	$R_S = 50\ \Omega$, $T_A = T_{opt}$
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		7		μV/°C	$T_A = T_{opt}$
Input Bias Current	I_b			7	nA	$T_A = T_{opt}$
Input Offset Current	I_{io}			2	nA	$T_A = T_{opt}$

Operating Characteristics

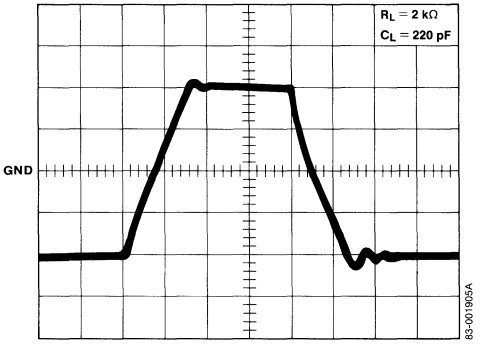
$T_A = 25°C$

Voltage Follower Pulse Response



5 V/div Vertical
500 ns/div Horizontal

Voltage Follower Pulse Response



5 V/div Vertical
500 ns/div Horizontal

NEC
NEC Electronics Inc.

μPC1458
DUAL GENERAL PURPOSE OPERATIONAL AMPLIFIER

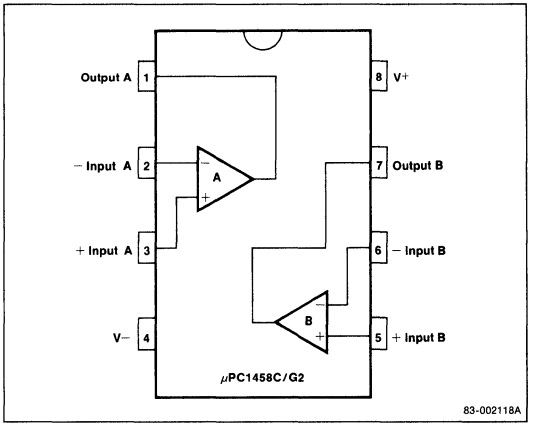
Description

The μPC1458 ia a dual general purpose operational amplifier which incorporates internal frequency compensation. This circuit was designed for a wide range of general applications. Large common mode voltage range and latch-free operation make this device ideal for voltage-follower applications where quality and cost are major concerns.

Features

- ☐ Internal frequency compensation
- ☐ Short-circuit protection
- ☐ Large common mode and differential input voltage
- ☐ No latch-up
- ☐ MC1458 direct replacement

Pin Configuration



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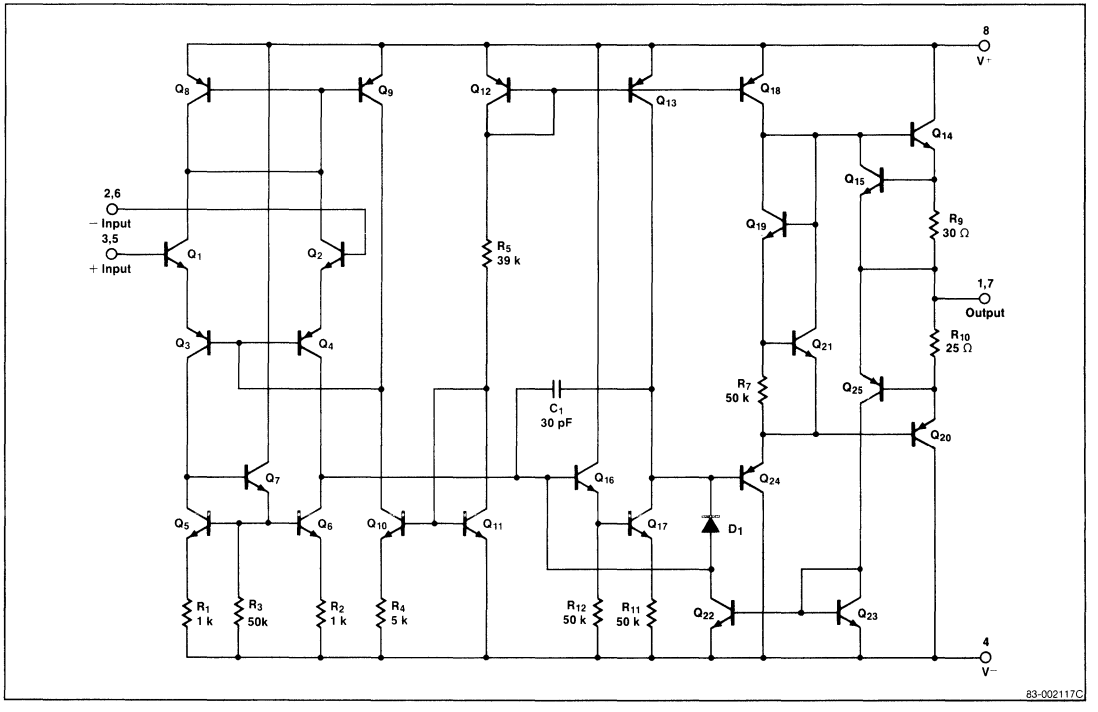
Equivalent Circuit

1/2 Circuit



Ordering Information

Part Number	Package	Operating Temperature Range
μPC1458C	Plastic DIP	0°C to +70°C
μPC1458G2	Plastic Miniflat	0°C to +70°C

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V^+ and V^-	36 V
Power Dissipation, C Package	350 mW
Power Dissipation, G2 Package	440 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

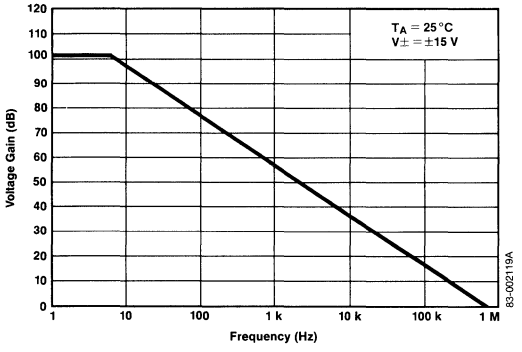
$T_A = 25°C$, $V^{\pm} = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		1.0	6.0	mV	$R_S \leq 10$ kΩ
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		3		μV/°C	$R_S \leq 10$ kΩ
Input Offset Current	I_{io}		20	200	nA	
Input Bias Current	I_b		80	500	nA	
Large Signal Voltage Gain	A_{VOL}	88	104		dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Channel Separation	CS		120		dB	f = 10 Hz, $R_L = 2$ kΩ
Supply Current	I_{CC}		3.0	5.6	mA	
Power Consumption	P_D		90	170	mW	
Common Mode Rejection Ratio	CMRR	70	90		dB	$R_S \leq 10$ kΩ
Supply Voltage Rejection Ratio	SVRR		89	103	dB	$R_S \leq 10$ kΩ
Output Voltage Swing	V_{om}	±12	±14		V	$R_L \geq 10$ kΩ
Output Voltage Swing	V_{om}	±10	±13		V	$R_L \geq 2$ kΩ
Input Impedance	R_{IN}	0.3	1		MΩ	

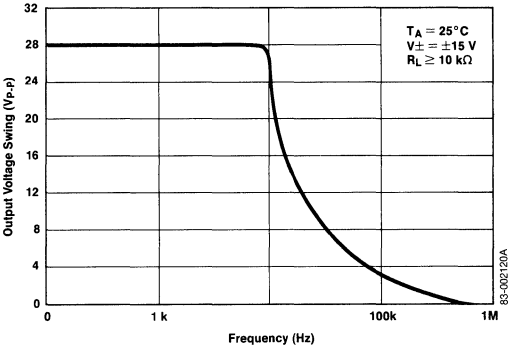
Operating Characteristics

$T_A = 25°C$

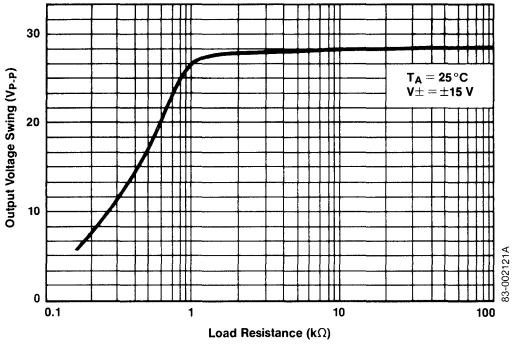
Open Loop Frequency Response



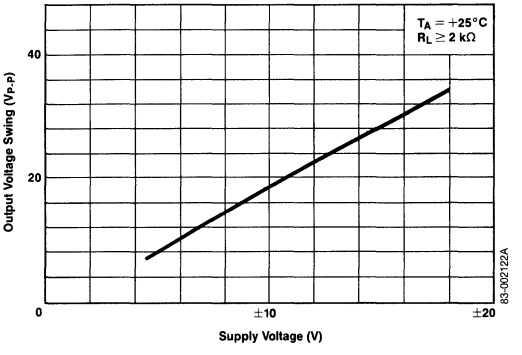
Large Signal Frequency Response



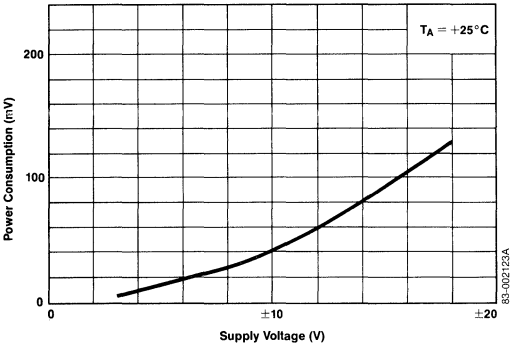
Output Voltage Swing vs Load Resistance



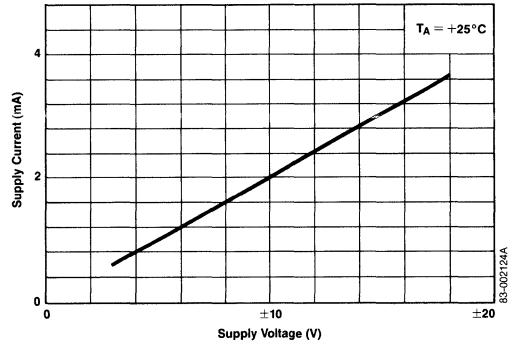
Output Voltage Swing



Power Consumption



Supply Current



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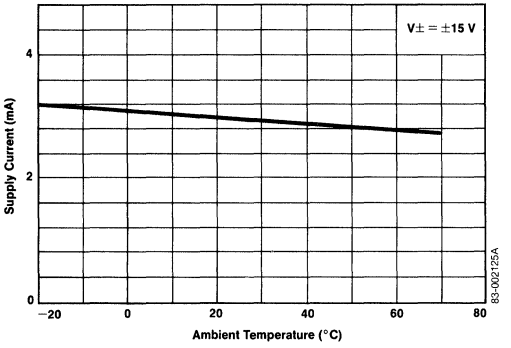
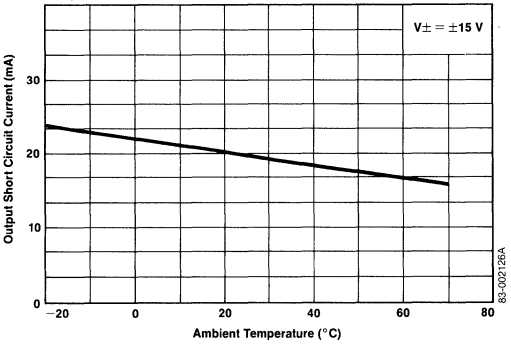
Operating Characteristics (Cont.)

$T_A = 25°C$

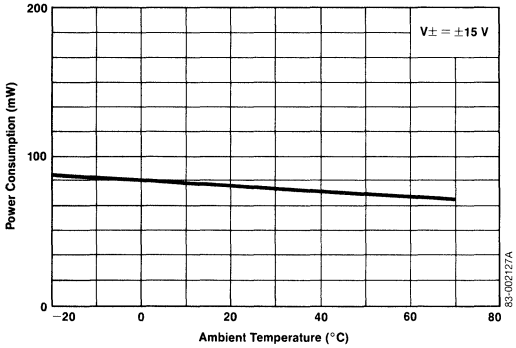
$T_{CC} - T_A$ Characteristics



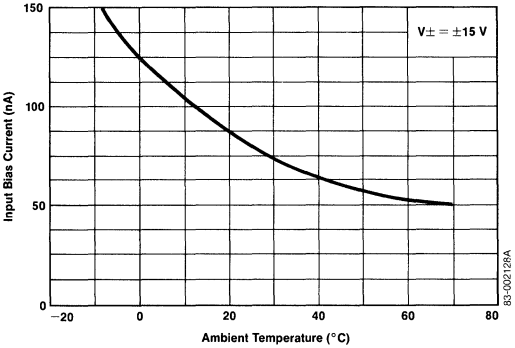
Output Short Circuit Current



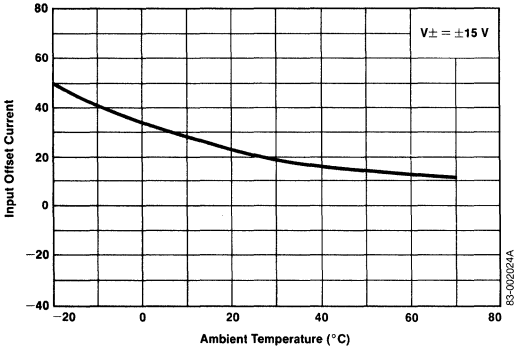
Power Consumption



Input Bias Current



Input Offset Current



NEC Electronics Inc.

μPC4062
DUAL J-FET INPUT LOW-POWER OPERATIONAL AMPLIFIER

PRELIMINARY INFORMATION

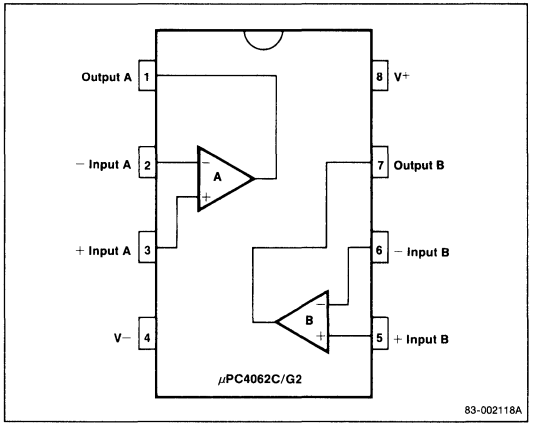
Description

The μPC4062 is a low-power, J-FET input, operational amplifier featuring low supply voltage operation from ±1.75 V. Supply current of μPC4062 is 1/10 the supply current of a μPC4083 op-amp. With very low input bias current characteristics, the μPC4062 is an excellent choice for hand-held measurement equipment and other low-power application circuits.

Features

- ☐ Low supply current: 400 μA
- ☐ Very low input bias and offset currents
- ☐ High slew-rate: 3 V/μs
- ☐ High input impedance
- ☐ Low supply voltage operation
- ☐ Output short-circuit protection
- ☐ Internal frequency compensation

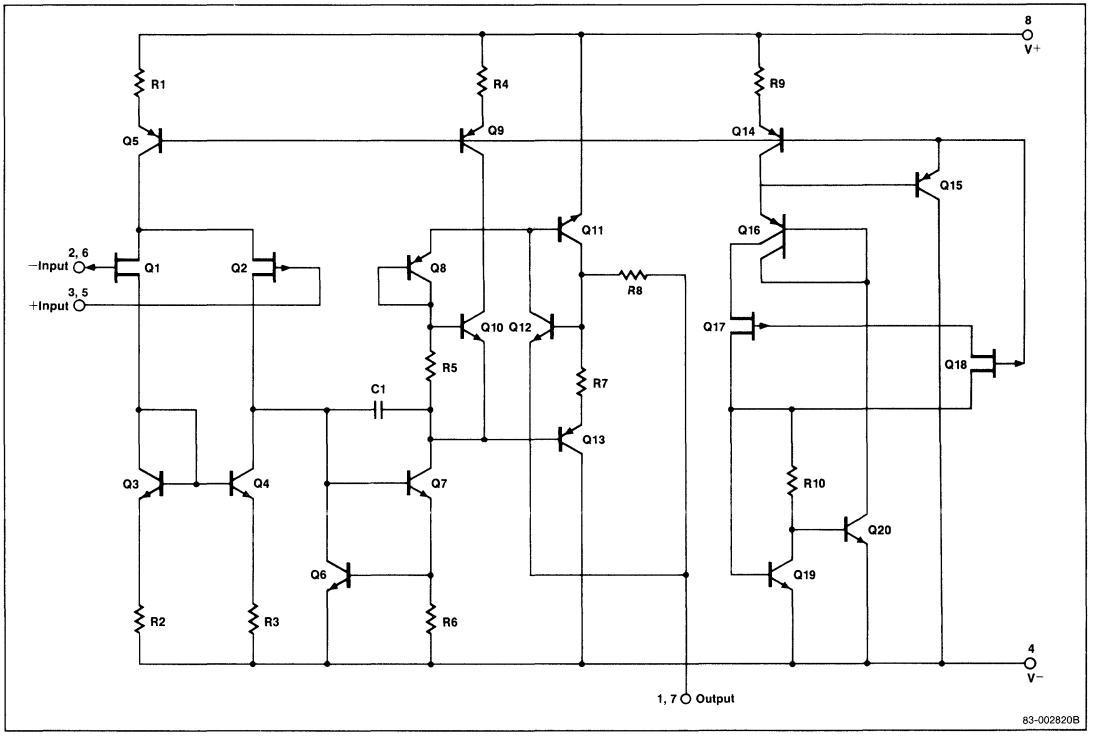
Pin Configuration



3

Equivalent Circuit

1/2 Circuit



Ordering Information

Part Number	Package	Operating Temperature Range
μPC4062C	Plastic DIP	0 to +70°C
μPC4062G2	Plastic Miniflat	0 to +70°C

Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	$V\pm$	±1.75		±16	V	
Output Current	I_O			5	mA	
Load Capacitance (Voltage Follower)	C_L			100	pF	

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Power Dissipation (Note 1), C Package	350 mW
Power Dissipation (Note 2), G2 Package	440 mW
Differential Input Voltage	±30 V
Input Voltage (Note 3)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Notes: 1. Thermal derating factor is 5 mW/°C for $T_A > +55°C$.
2. Thermal derating factor is 4.4 mW/°C for $T_A > +25°C$.
3. For supply voltages less than +15 V, the absolute maximum input voltage is equal to the supply voltage.

Electrical Characteristics

$T_A = 25°C$, $V\pm = \pm15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		2	15	mV	$R_S = 50$
Input Offset Voltage	V_{io}			20	mV	$R_S = 50$, $T_A = T_{OPT}$
Input Offset Voltage	$\Delta V_{io}/\Delta T$		7		μV/°C	$R_S = 50$, $T_A = T_{OPT}$
Input Offset Current	I_{io}		5	50	pA	
Input Offset Current	I_{io}			1.5	nA	$T_A = T_{OPT}$
Input Bias Current	I_b		10	100	pA	
Input Bias Current	I_b			3	nA	$T_A = T_{OPT}$
Large Signal Voltage Gain	A_{VOL}	69	75		dB	$R_L = 10$ kΩ, $V_O = \pm10$ V
Supply Current	I_{CC}		400	500	μA	
Common Mode Rejection Ratio	CMRR	70	95		dB	
Supply Voltage Rejection Ratio	SVRR	70	95		dB	
Output Voltage Swing	V_{om}	±12	±14		V	$R_L = 10$ kΩ
Common Mode Input Voltage	V_{icm}	±12	+15		V	
			−13		V	
Output Current	I_O	±5			mA	$V_{om} = \pm10$ V
Slew Rate	SR		3		V/μs	$R_L = 10$ kΩ
Input Noise Voltage	en		30		nV/√Hz	f = 1 kHz
Gain Bandwidth Products	GBW		1		MHz	
Channel Separation			120		dB	f = 1 to 20 kHz

NEC Electronics Inc.

μPC4072
DUAL J-FET INPUT LOW-NOISE OPERATIONAL AMPLIFIER

Description

The J-FET input operational amplifiers of the μPC4072 are designed as low-noise versions of the μPC4082. Features of the μPC4072 include improved input noise voltage, input offset voltage, and input bias current compared to the μPC4082. These features make the μPC4072 an excellent choice for a wide variety of applications including audio preamplifier and active filter circuits.

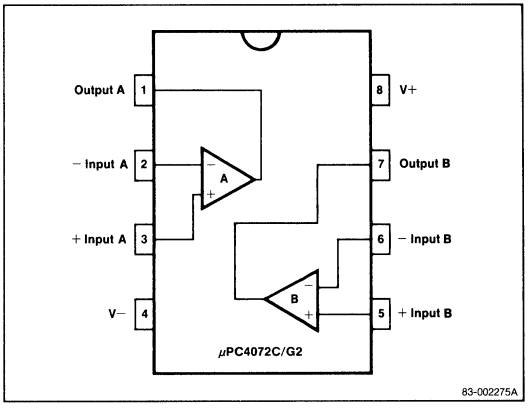
Features

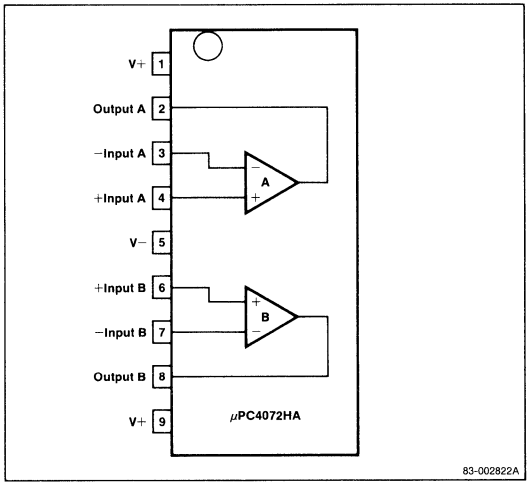
- ☐ Low noise: en = 18 nV/$\sqrt{Hz}$
- ☐ Low input bias and offset currents
- ☐ Output short-circuit protection
- ☐ High input impedance
- ☐ Internal frequency compensation
- ☐ High slew rate: 13 V/μs typical
- ☐ Latch-free operation

Ordering Information

Part Number	Package	Operating Temperature Range
μPC4072C	Plastic DIP	0 to +70°C
μPC4072G2	Plastic Miniflat	0 to +70°C
μPC4072HA	Plastic SIP	0 to +70°C

Pin Configurations

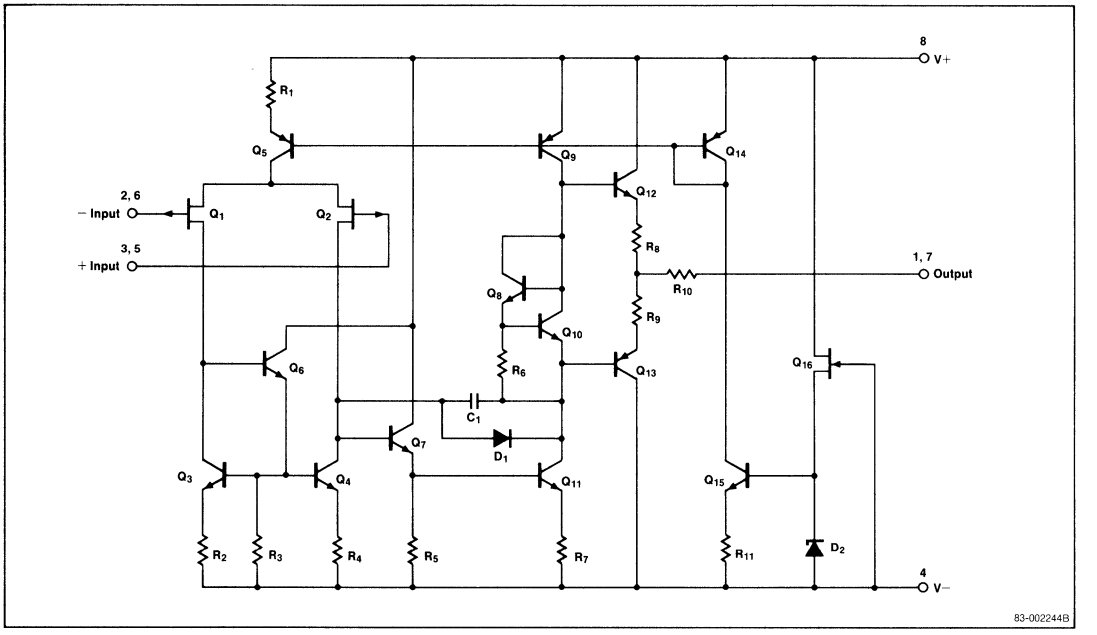




3

Equivalent Circuit

1/2 Circuit



Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Power Dissipation (C Package)	350 mW
Power Dissipation (G2 Package)	440 mW
Power Dissipation (HA Package)	350 mW
Output Short Circuit Duration	Indefinite
Operating Temperature Range (C or G2 Package)	0 to +70°C
Operating Temperature Range (HA Package)	0 to +70°C
Storage Temperature Range (C or G2 Package)	−55 to +125°C
Storage Temperature Range (HA Package)	−55 to +125°C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to supply voltages.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	$V\pm$	±5		±16	V	
Capacitive Load ($A_V = +1$)	C_L			100	pF	
Output Current	I_O			10	mA	

Electrical Characteristics

$T_A = 25°C$, $V\pm = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		3	10.0	mV	$R_S \leq 50\ \Omega$
Input Offset Current	I_{io}		5	50	pA	$T_A = 25°C$ (Note 1)
Input Bias Current	I_b		30	200	pA	$T_A = 25°C$ (Note 1)
Large Signal Voltage Gain	A_{VOL}	88	106		dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Supply Current	I_{CC}		4	5	mA	Both amplifiers
Common Mode Rejection Ratio	CMRR	70	86		dB	
Supply Voltage Rejection Ratio	SVRR	70	86		dB	
Output Voltage Swing	V_{om}	±12	±13.5		V	$R_L \geq 10$ kΩ
Output Voltage Swing	V_{om}	±10	±12		V	$R_L \geq 2$ kΩ
Common Mode Input Voltage Range	V_{icm}	±10			V	
Slew Rate	SR		13		V/μs	$A_V = 1$
Input Equivalent Noise Voltage	en		18		$nV/\sqrt{Hz}$	$R_S = 100\ \Omega$, f = 1 kHz
			4		μV_{RMS}	$R_S = 100\ \Omega$, f = 10 Hz to 10 kHz
Unity Gain Bandwidth	GBW		3		MHz	
Channel Separation	CS		120		dB	
Over Operating Temperature Range						
Input Offset Voltage	V_{io}			13	mV	$R_S \leq 50\ \Omega$, $T_A = T_{OPT}$
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		10		μV/°C	$T_A = T_{OPT}$
Input Bias Current	I_b			7	nA	$T_A = T_{OPT}$
Input Offset Current	I_{io}			2	nA	$T_A = T_{OPT}$

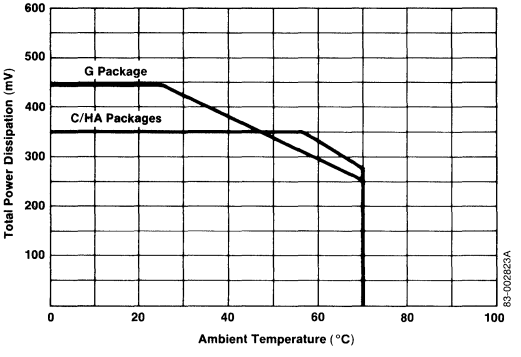
Note: 1. Input bias currents are temperature sensitive. Short time measuring method is recommended to maintain the junction temperature close to the ambient temperature.

3

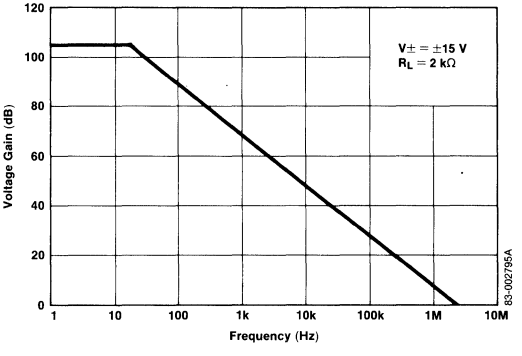
Operating Characteristics

$T_A = 25°C$

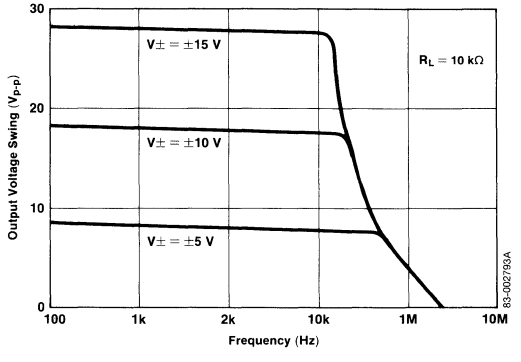
Power Dissipation



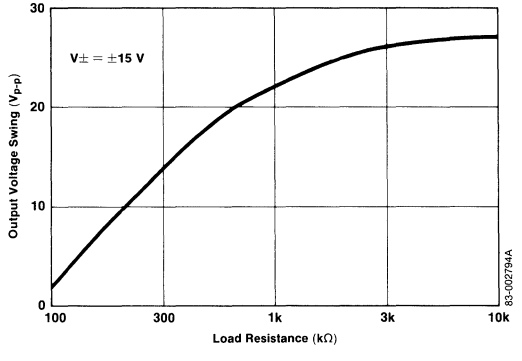
Open Loop Frequency Response



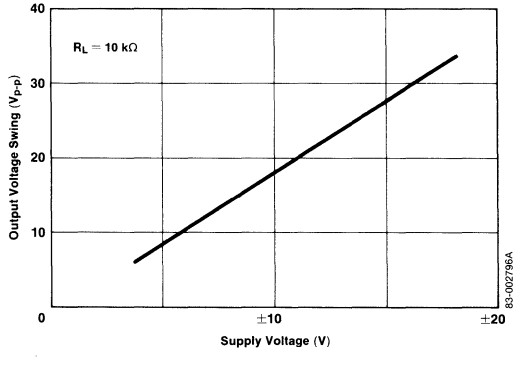
Large Signal Frequency Response



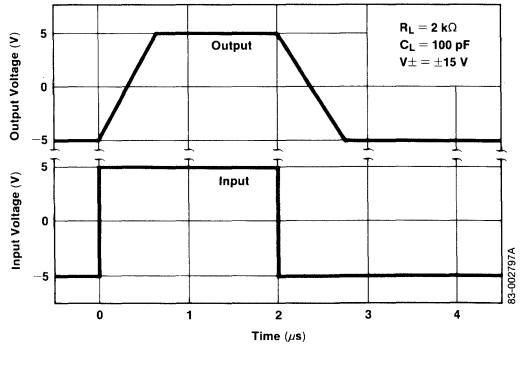
Output Voltage Swing



Output Voltage Swing



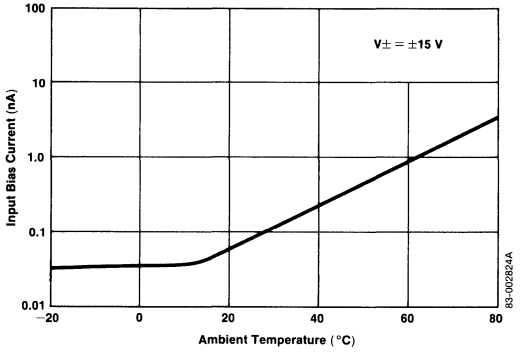
Voltage Follower Pulse Response



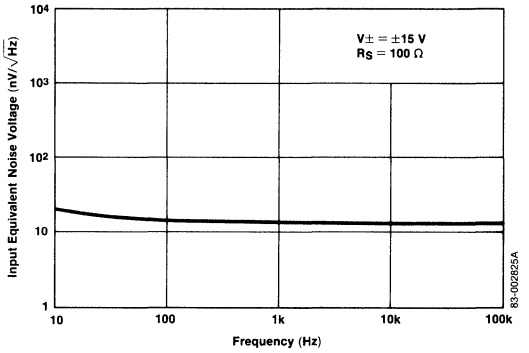
Operating Characteristics (Cont.)

$T_A = 25°C$

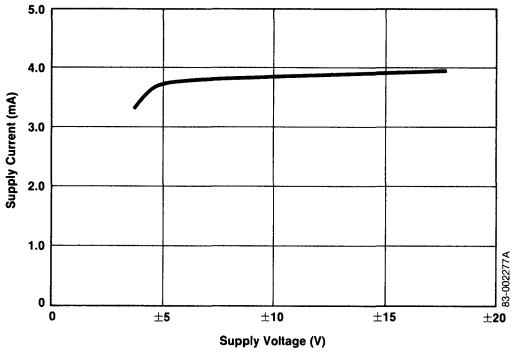
Input Bias Current



Input Equivalent Noise Voltage



Supply Current



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μPC4082
DUAL J-FET INPUT OPERATIONAL AMPLIFIER

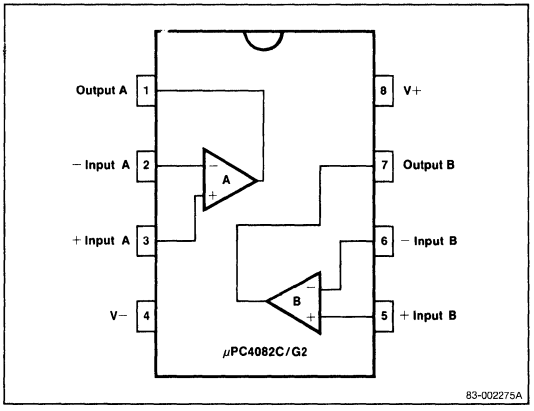
Description

The μPC4082 is designed around matched ion implant P-channel J-FET inputs, along with standard bipolar technology. Featuring very low input bias current and ten times the slew rate of general purpose operational amplifiers, this device is well suited for active filters, integrators, and pulse amplifier applications.

Features

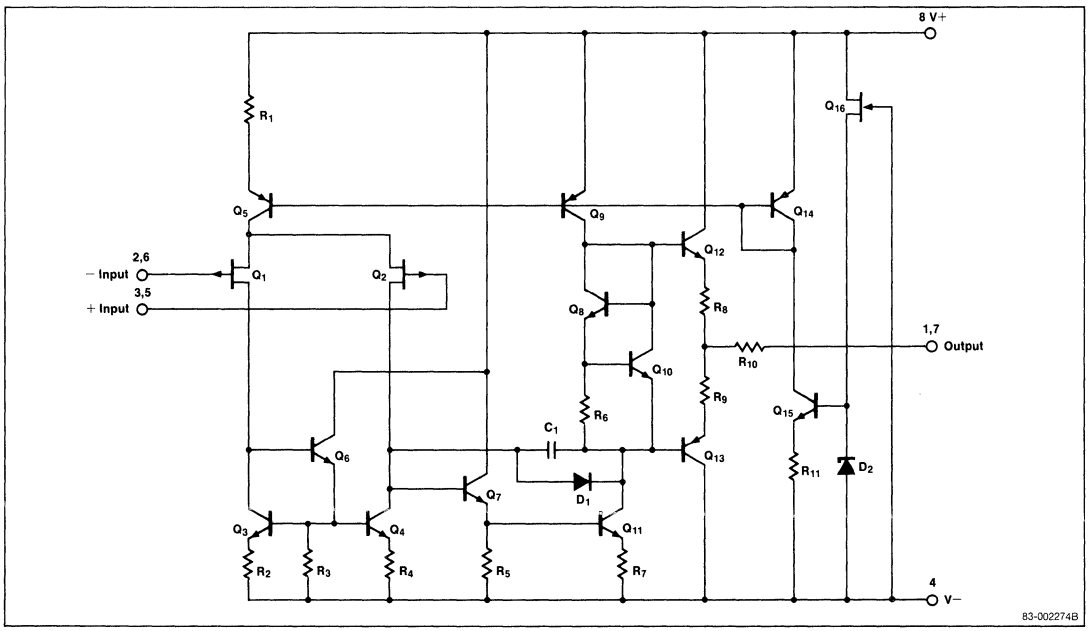
- ☐ Wide common-mode and differential input voltage ranges
- ☐ Low input bias and offset currents
- ☐ Output short-circuit protection
- ☐ High input impedance: J-FET input stage
- ☐ Internal frequency compensation
- ☐ High slew rate: 13 V/μs typical
- ☐ Latch-free operation
- ☐ TL082 direct replacement

Pin Configuration



Equivalent Circuit

1/2 Circuit



Ordering Information

Part Number	Package	Operating Temperature Range
μPC4082C	Plastic DIP	0°C to +70°C
μPC4082G2	Plastic Miniflat	0°C to +70°C

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V^+ and V^-	36 V
Power Dissipation, C Package	350 mW
Power Dissipation (Note 1), G2 Package	440 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

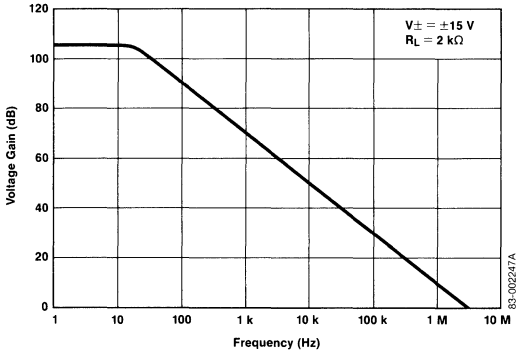
$T_A = 25°C$, $V^{\pm} = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		5.0	15.0	mV	$R_S \leq 50$
Input Offset Current	I_{io}		5	200	pA	
Input Bias Current	I_b		30	400	pA	
Large Signal Voltage Gain	A_{VOL}	88	106		dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Supply Current	I_{CC}		4.0	5.6	mA	Both amplifiers
Common Mode Rejection Ratio	CMRR	70	76		dB	
Supply Voltage Rejection Ratio	SVRR	70	76		dB	
Output Voltage Swing	V_{om}	±12	±13.5		V	$R_L \geq 10$ kΩ
Output Voltage Swing	V_{om}	±10	±12		V	$R_L \geq 2$ kΩ
Common Mode Input Voltage Range	V_{icm}	±10			V	
Slew Rate	SR		13		V/μs	$A_V = 1$
Input Equivalent Noise Voltage	en		25		nV/$\sqrt{Hz}$	f = 1 kHz, $R_S = 100$ Ω
Unity Gain Bandwidth	GBW		3		MHz	
Channel Separation	CS		120		dB	
Over Operating Temperature Range						
Input Offset Voltage	V_{io}			20	mV	$R_S \leq 50$ Ω, $T_A = T_{OPT}$
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		10		μV/°C	$T_A = T_{OPT}$
Input Bias Current	I_b			10	nA	$T_A = T_{OPT}$
Input Offset Current	I_{io}			5	nA	$T_A = T_{OPT}$

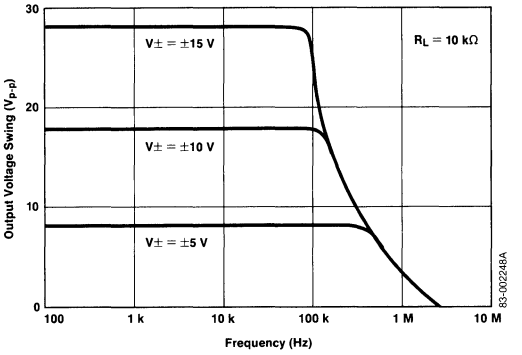
Operating Characteristics

$T_A = 25°C$

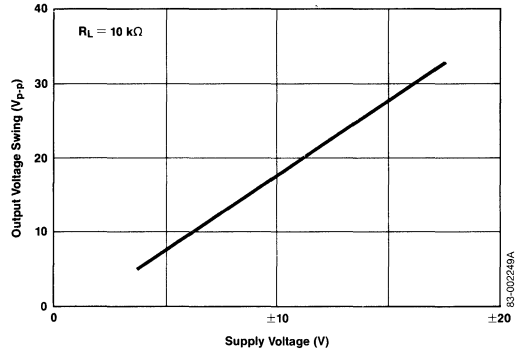
Open Loop Frequency Response



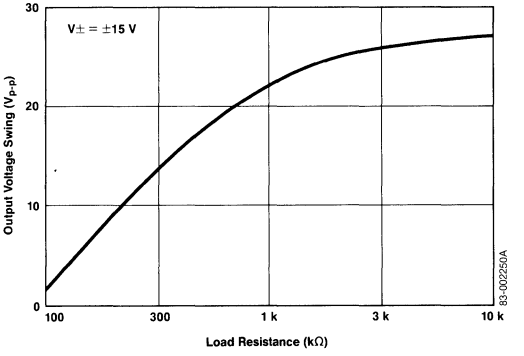
Large Signal Frequency Response



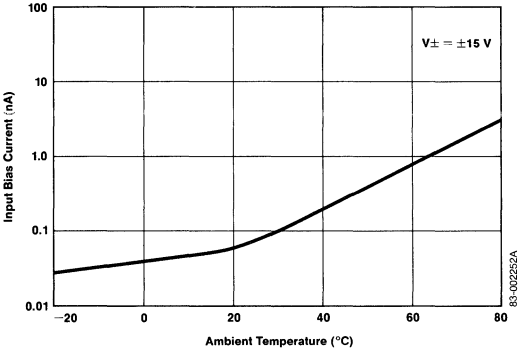
Output Voltage Swing



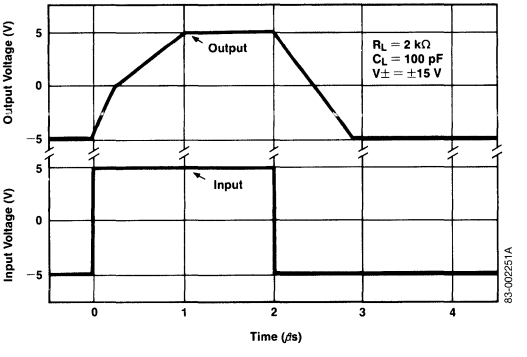
Output Voltage Swing



Input Bias Current



Voltage Follower Pulse Response



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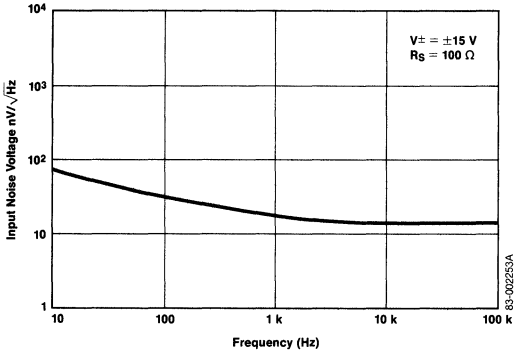
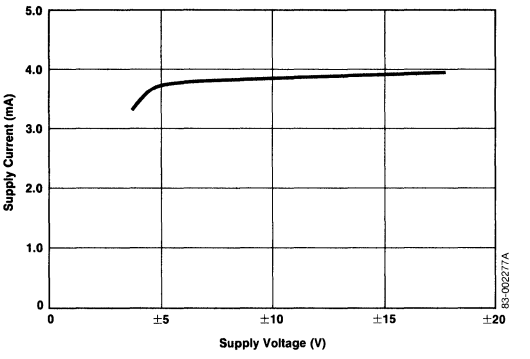
Operating Characteristics (Cont.)

$T_A = 25°C$

Input Equivalent Noise Voltage



Supply Current



NEC
NEC Electronics Inc.

μPC4359
DUAL HIGH-SPEED PROGRAMMABLE CURRENT MODE OPERATIONAL AMPLIFIER

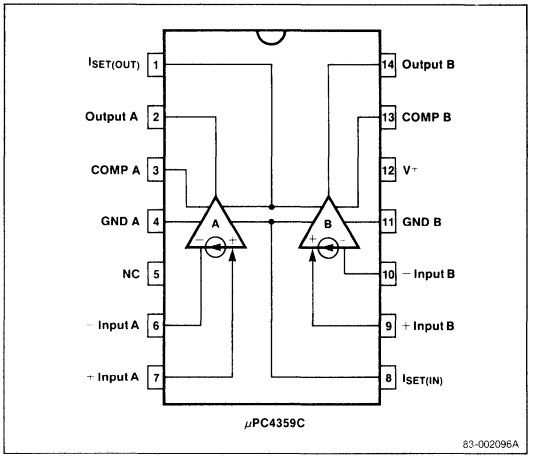
Description

The μPC4359 consists of two current differencing input amplifiers. Design emphasis has been placed on obtaining high frequency performance while providing user programmability. Each amplifier provides high gain-bandwidth product, high slew rate, and stable inverting operation in closed loop designs with a gain of ten or greater.

Features

- ☐ User programmable gain bandwidth product, slew rate, input bias current, output stage current
- ☐ High gain bandwidth product:
  300 MHz for $A_v = 10$ to 100
  30 MHz for $A_v = 1$
- ☐ High slew rate:
  60 V/μs for $A_v = 10$ to 100
  30 V/μs for $A_v = 1$
- ☐ Operates from a single 5 V to 22 V supply
- ☐ Current differencing inputs allow high common-mode input voltages
- ☐ LM359 direct replacement

Pin Configuration

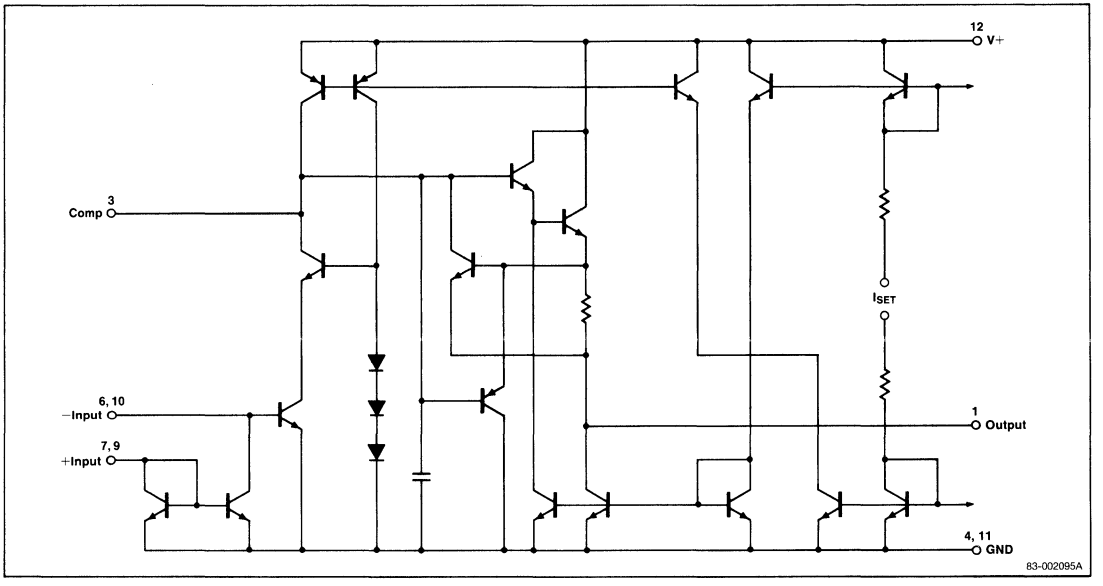


Ordering Information

Part Number	Package	Operating Temperature Range
μPC4359C	Plastic DIP	0°C to +70°C

Equivalent Circuit

1/2 Circuit



Absolute Maximum Ratings

$T_A = 25°C$

Supply Voltage Range V+	22 V
Input Current I_{IN}	20 mA
Set Current I_{SET}	2 mA
Power Dissipation P_D	570 mW
Operating Temperature Range, T_{opt}	0 to +70°C
Storage Temperature Range, T_{stg}	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

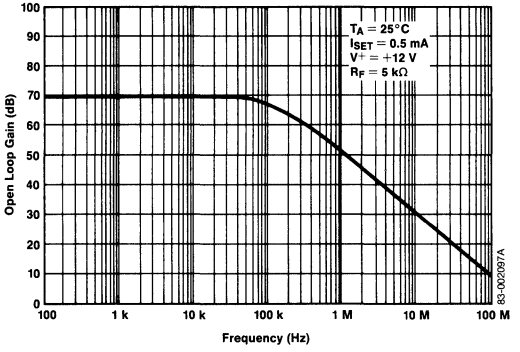
$T_A = 25°C$, $I_{SET} = 0.5$ mA, $V\pm = \pm 12$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Open Loop Voltage Gain	A_{VOL}	62	70		dB	$f = 100$ Hz, $R_L = 1$ kΩ
Gain Bandwidth	GBW	15	30		MHz	$R_{IN} = 1$ kΩ, $C_{COMP} = 10$ pF, $A_V = 1$
		200	300		MHz	$R_{IN} = 50$ to 200 Ω, $A_V = 10$ to 100
Slew Rate	SR		30		V/μs	$R_{IN} = 1$ kΩ, $C_{COMP} = 10$ pF, $A_V = 1$
			60		V/μs	$R_{IN} \leq 200$ Ω
Channel Separation	CS		80		dB	$f = 100$ Hz to 100 kHz, $R_L = 1$ kΩ
Mirror Gain	$\frac{-\text{Input}}{+\text{Input}}$	0.9	1.0	1.1	μA/μA	$I_{SET} = 5$ μA +Inputs = 2 mA $T_A = 25°C$
		0.9	1.0	1.1	μA/μA	$I_{SET} = 5$ μA +Inputs = 0.2 mA $T_A = T_{OPT}$
		0.9	1.0	1.1	μA/μA	$I_{SET} = 5$ μA +Inputs = 20 mA
Mirror Gain	$\Delta\left(\frac{-\text{Input}}{+\text{Input}}\right)$		3.0	5.0	%	$I_{SET} = 5$ μA +Inputs = 20 mA to 0.2 mA $T_A = T_{OPT}$
Input Bias Current	I_b		5.3	15	μA	−Inputs $T_A = 25°C$
			30		μA	−Inputs $T_A = T_{OPT}$
Input Resistance	R_{IN}		2.5		kΩ	−Inputs
Output Resistance	R_O		3.5		Ω	$I_O = 15$, mA_{rms}, $f = 1$ MHz
High Level Output Voltage	V_{OH}	9.5	10.3		V	$R_L = 600$ Ω, all inputs grounded
Low Level Output Voltage	V_{OL}		0.002	0.05	V	$R_L = 600$ Ω, −Inputs = 100 μA, +inputs grounded
Output Source Current	I_{SOURCE}	16	65		mA	$R_L = 100$ Ω, all inputs grounded
Output Sink Current	I_{SINK}		4.7		mA	$V_O = 1$ V, $V_{COMP} = 0.5$ V, +inputs grounded
		1.5	4.5			$V_O = 1$ V, −Inputs = 100 μA, +inputs grounded
Supply Current	I_{CC}		17	22	mA	$R_L = \infty$, +inputs grounded
Supply Voltage Rejection Ratio	SVRR	40	48		dB	$f = 120$ Hz, +inputs grounded

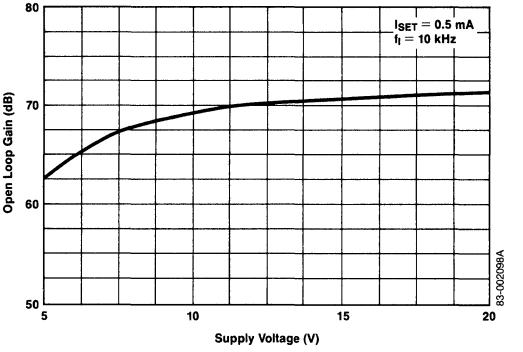
Operating Characteristics

$T_A = 25°C$

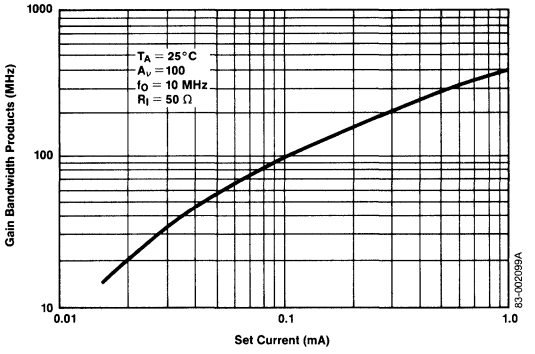
Open Loop Frequency Response



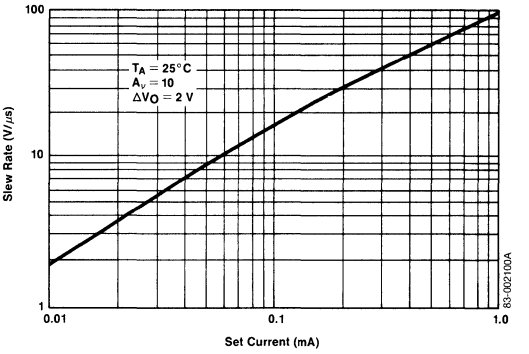
Open Loop Gain



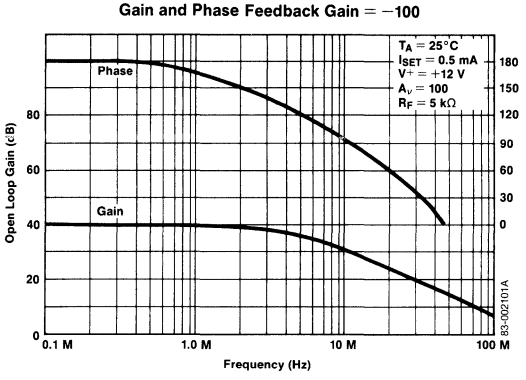
Gain Bandwidth Products



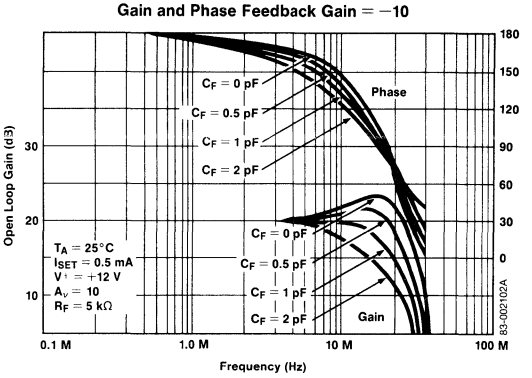
Slew Rate



Gain and Phase Feedback Gain = −100



Gain and Phase Feedback Gain = −10



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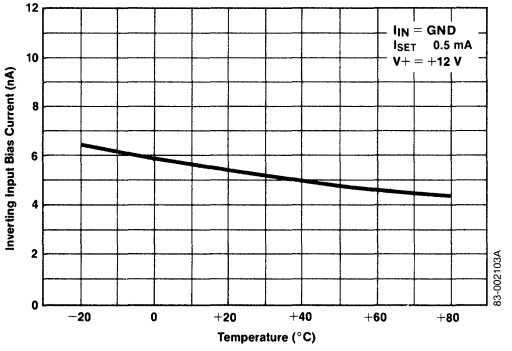
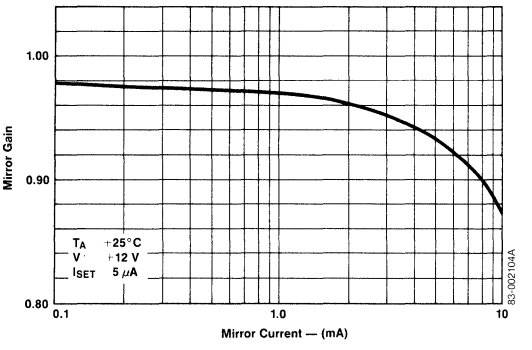
Operating Characteristics (Cont.)

$T_A = 25°C$

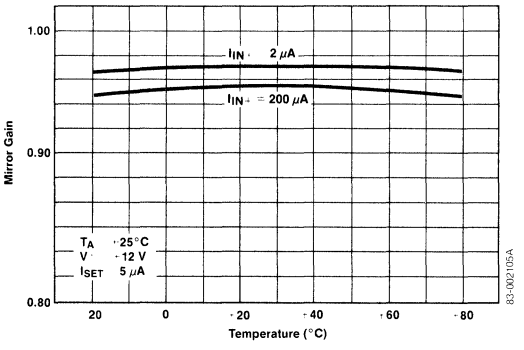
Inverting Input Bias Current



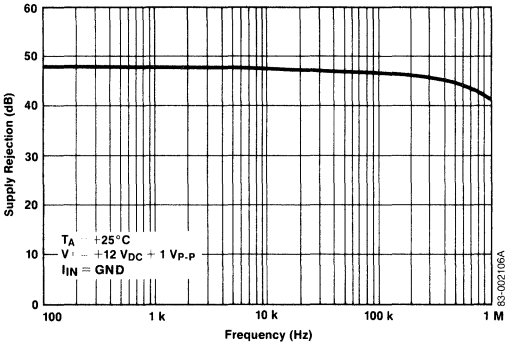
Mirror Gain



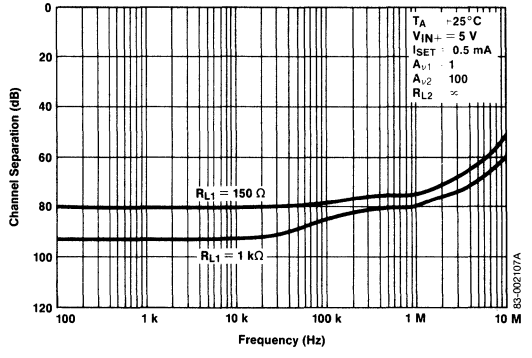
Mirror Gain



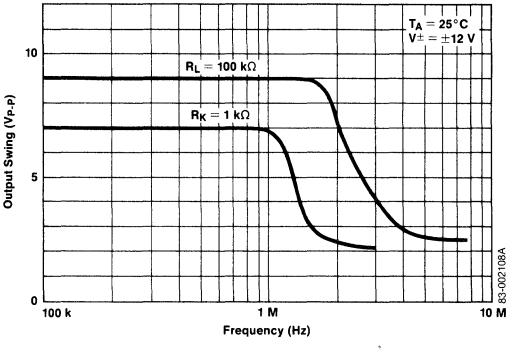
Supply Rejection



Channel Separation (Amp1 → Amp 2)



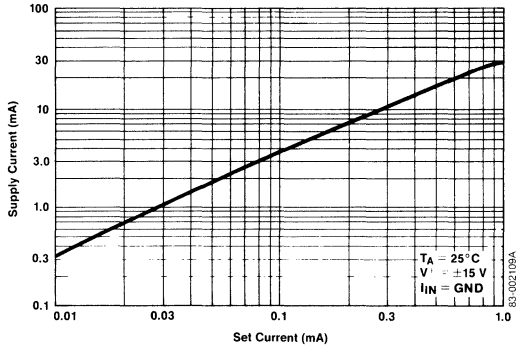
Output Swing



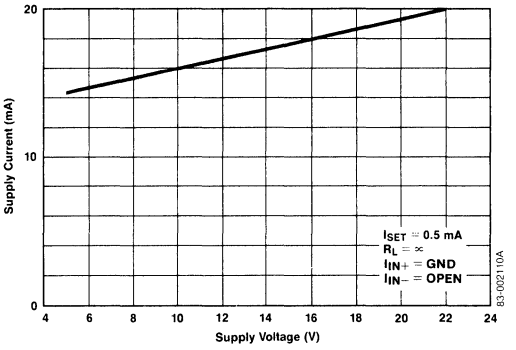
Operating Characteristics (Cont.)

$T_A = 25°C$

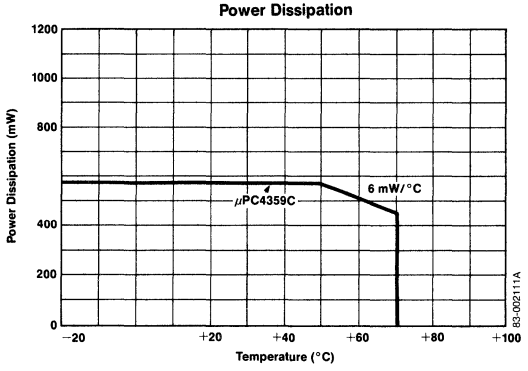
Supply Current



Supply Current



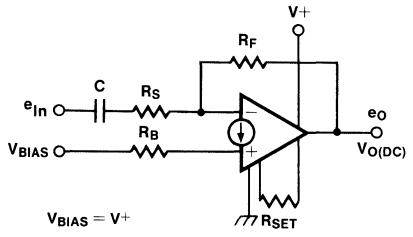
Power Dissipation



3

Typical Applications

Inverting AC Amplifier

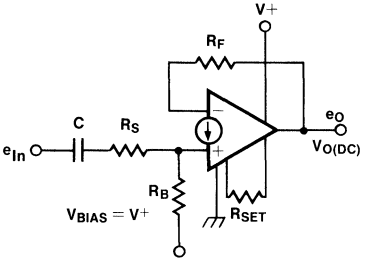


$A_{V(AC)} = R_F/R_S$

$V_{O(DC)} = V_{BE} + R_F\left[\frac{V+ - V_{BE}}{R_B} + I_{B(-)}\right]$

83-002112A

Non-Inverting AC Amplifier



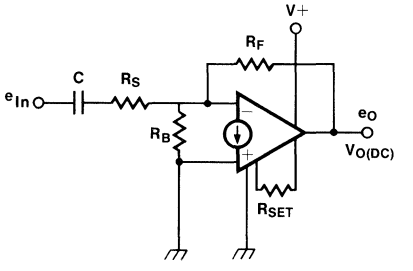
$A_{V(AC)} = R_F/(R_S + r_E)$ r_E: Emitter Resistance of Q1

$r_E = 0.026/I_{I+}$ ($I_{I(+)} = 0.2$ mA, $r_E = 130\ \Omega$)

$V_{O(DC)} = V_{BE}\left(1 + \frac{R_F}{R_B}\right) + I_{B(-)} \cdot R_F$

83-002113A

Inverting AC Amplifier (Self Biasing)



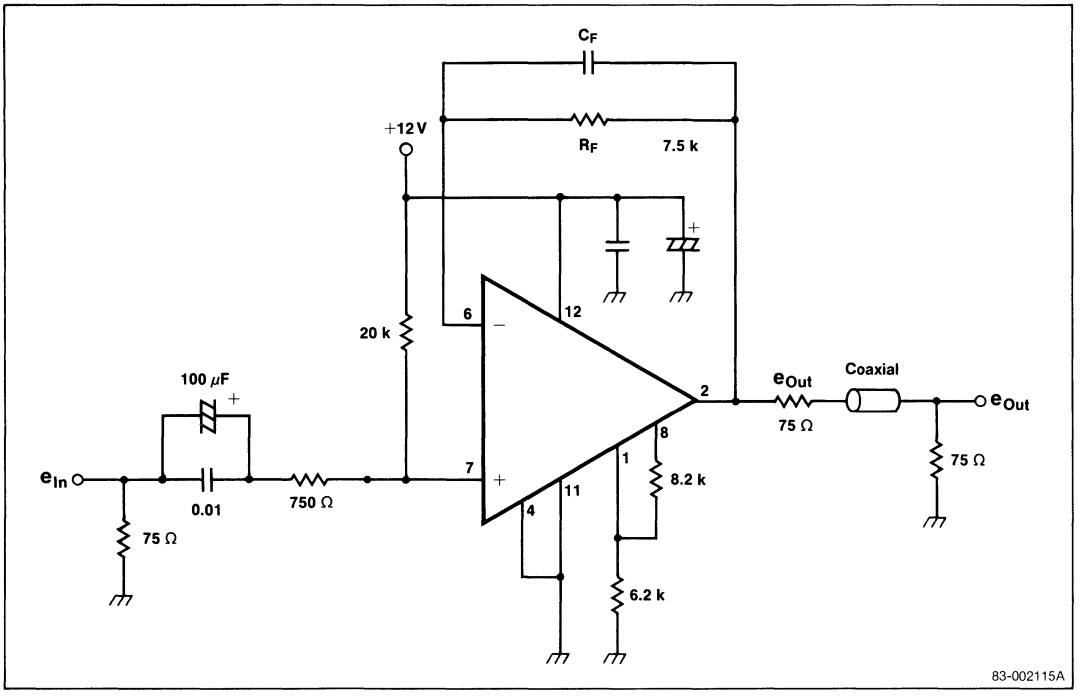
$A_{V(AC)} = R_F/(R_S + r_E)$ r_E: Emitter Resistance of Q1

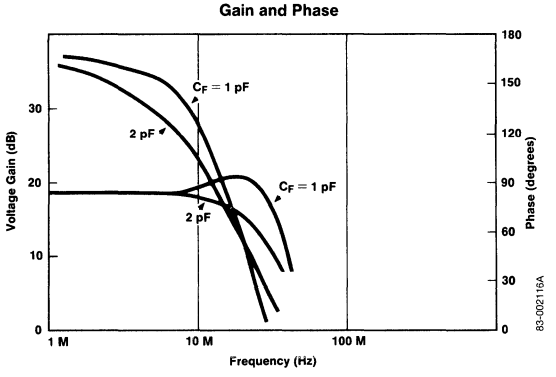
$V_{O(DC)} = V_{BE}\left(1 + \frac{R_F}{R_S}\right) + I_{B(-)} \cdot R_F$

83-002114A

Typical Applications (Cont.)

Video Line Driver Application





NEC

NEC Electronics Inc.

μPC4556
DUAL DECOMPENSATED HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

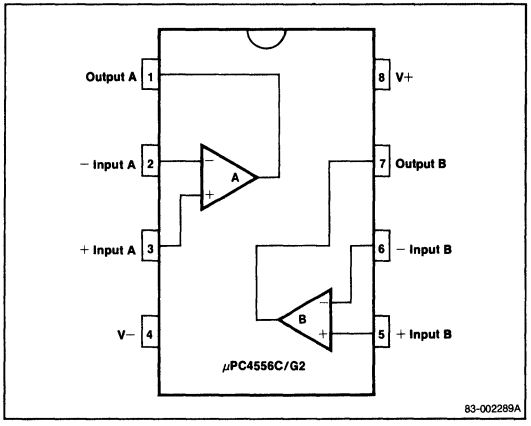
Description

The μPC4556 is a dual operational amplifier with advanced AC performance characteristics over the 4558 type operational amplifiers. The device features low input and high output current drive capability. The decompensation characteristic guarantees 20 MHz gain bandwidth product above 20 dB. The combined performance features of this device make it ideal for use in audio applications.

Features

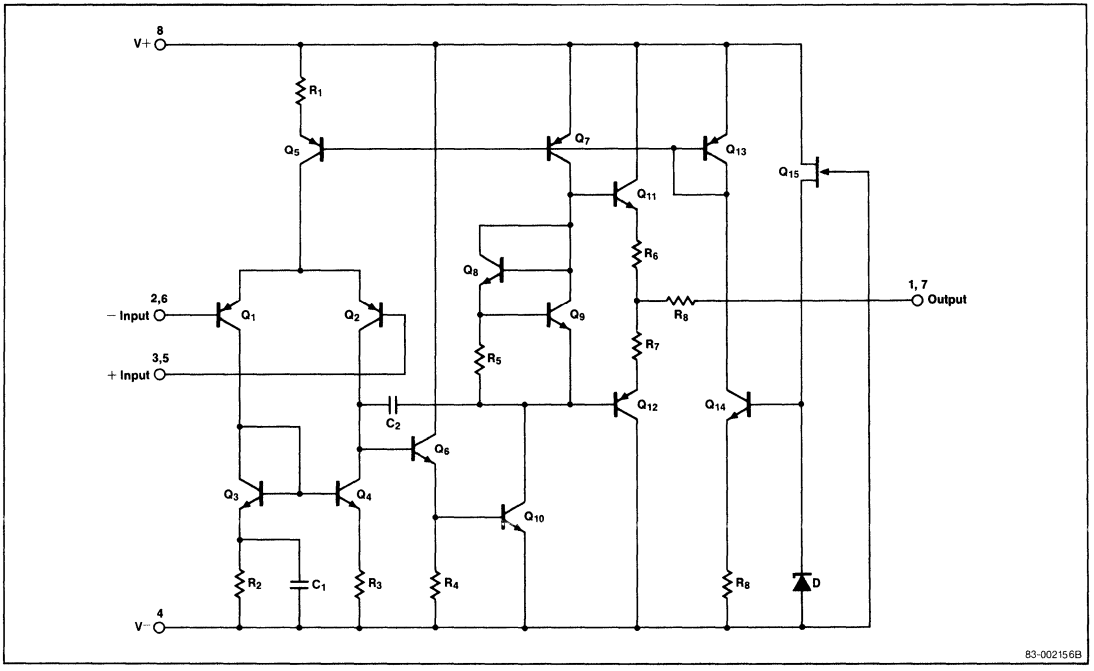
- ☐ Gain-bandwidth products: 20 MHz (Av ≥ 20 dB)
- ☐ High slew-rate: 5 V/μs
- ☐ Low input noise voltage: 6 μV_{P-P}
- ☐ Decompensated frequency characteristics
- ☐ Large common mode and differential input

Pin Configuration



Equivalent Circuit

1/2 Circuit



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Ordering Information

Part Number	Package	Operating Temperature Range
μPC4556C	Plastic DIP	0°C to +70°C
μPC4556G2	Plastic Miniflat	0°C to +70°C

Absolute Maximum Ratings

$T_A = 25°C$

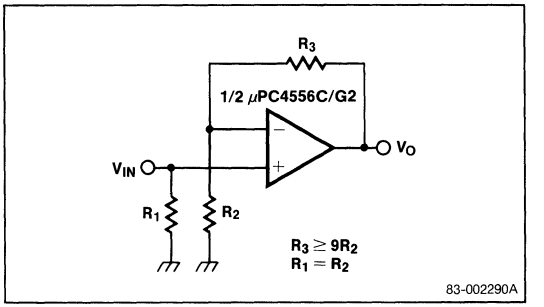
Voltage Between V^+ and V^-	36 V
Power Dissipation (Note 1), C Package	700 mW
Power Dissipation (Note 1), G2 Package	440 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Output Short Circuit Duration	5 s
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°

Notes: 1. When the ambient temperature is more than 25°C, derate linearly at 7mW/°C, ($T_{J\text{-}MAX} = 125°C$).
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

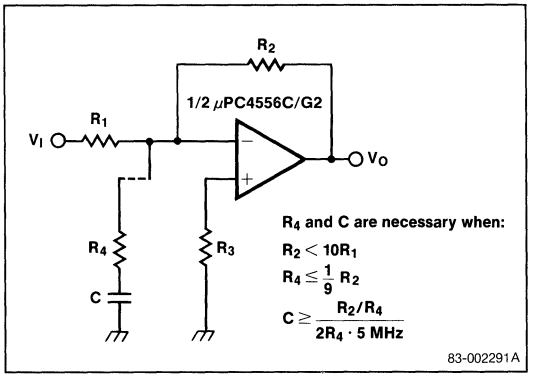
Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Typical Application

Non-Inverting Amplifier



Inverting Amplifier



Electrical Characteristics

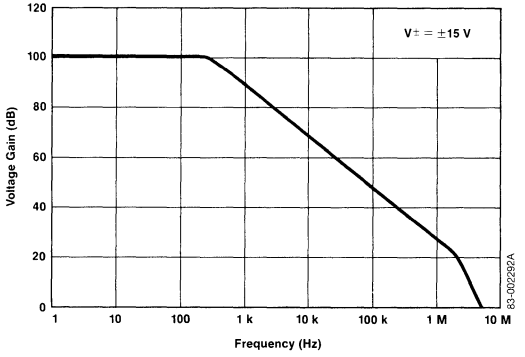
$T_A = 25°C$, $V^{\pm} = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{IO}		0.5	6.0	mV	$R_S \leq 10$ kΩ
Input Offset Current	I_{IO}		5	200	nA	
Input Bias Current	I_b		180	500	nA	
Voltage Gain	A_{VOL}		100	86	dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Power Dissipation	P_D		90	170	mW	Both channels
Common Mode Rejection Ratio	CMRR	70	90		dB	$R_S \leq 10$ kΩ
Supply Voltage Rejection Ratio	SVRR		89	103	dB	$R_S \leq 10$ kΩ
Output Voltage Swing	V_{OM}	±12	±14		V	$R_L \geq 2$ kΩ
Output Voltage Swing	V_{OM}	±10	±11.5		V	$I_O = \pm 25$ mA
Common Mode Input Voltage Range	V_{icm}	±12	±14		V	
Slew Rate	SR		5		V/μs	$A_V \geq 10$ (20 dB)
Input Noise Voltage	en		6		$\mu V_{P\text{-}P}$	$R_S = 1$ kΩ, f = 1 Hz to 1 kHz
Channel Separation	CS		105		dB	f = 1 kHz

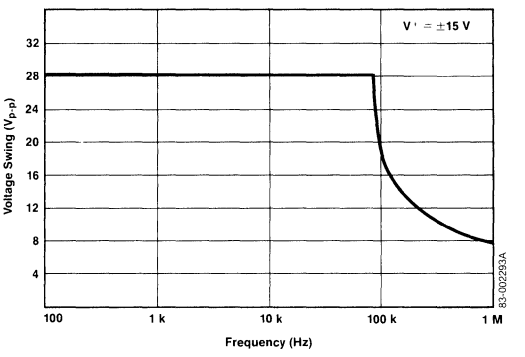
Operating Characteristics

$T_A = 25°C$

Open Loop Frequency Response



Large Signal Frequency Response



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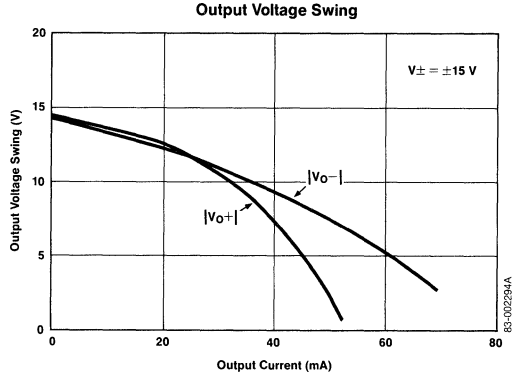
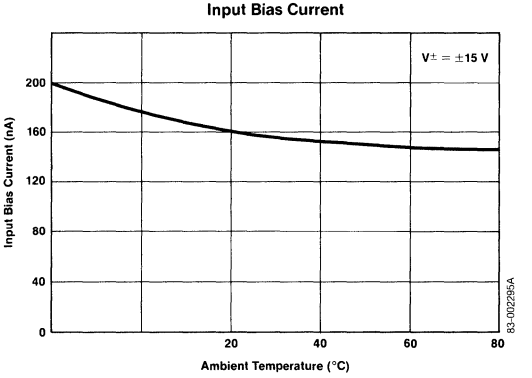
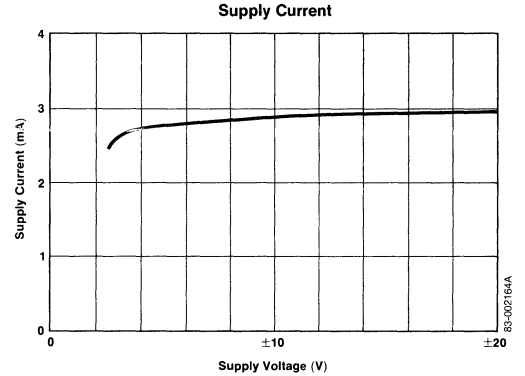
Output Voltage Swing



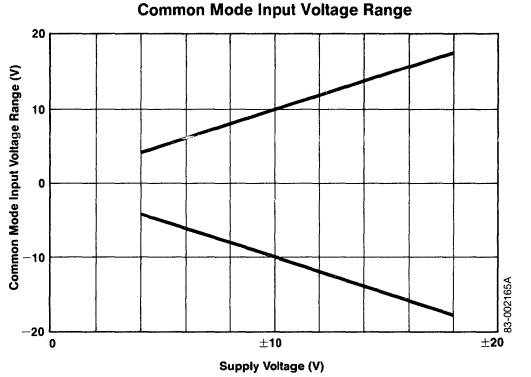
Input Bias Current



Supply Current



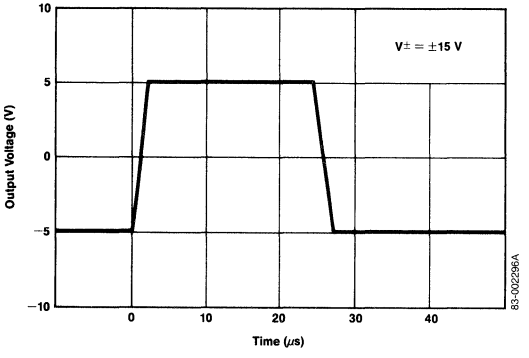
Common Mode Input Voltage Range



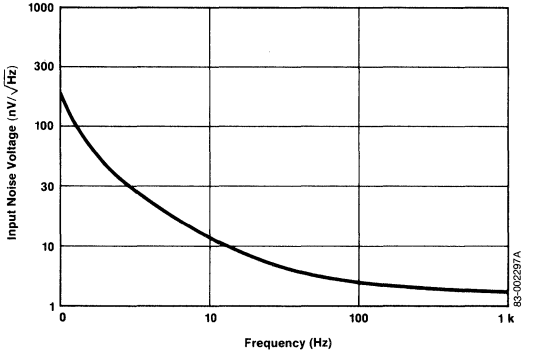
Operating Characteristics (Cont.)

$T_A = 25°C$

Pulse Response



Input Noise Voltage



μPC4557
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

Description

The μPC4557 is a dual operational amplifier which features higher output drive current than that of the μPC4558. This feature allows driving of headphone speakers directly. Other characteristics of this device are low noise and no crossover distortion, which make it the ideal choice for audio applications.

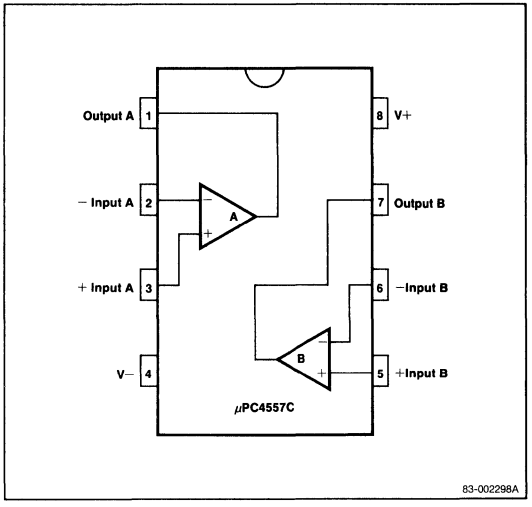
Features

- ☐ Internal frequency compensation
- ☐ Large common-mode and differential input voltage ranges
- ☐ No latch-up
- ☐ Low noise

Ordering Information

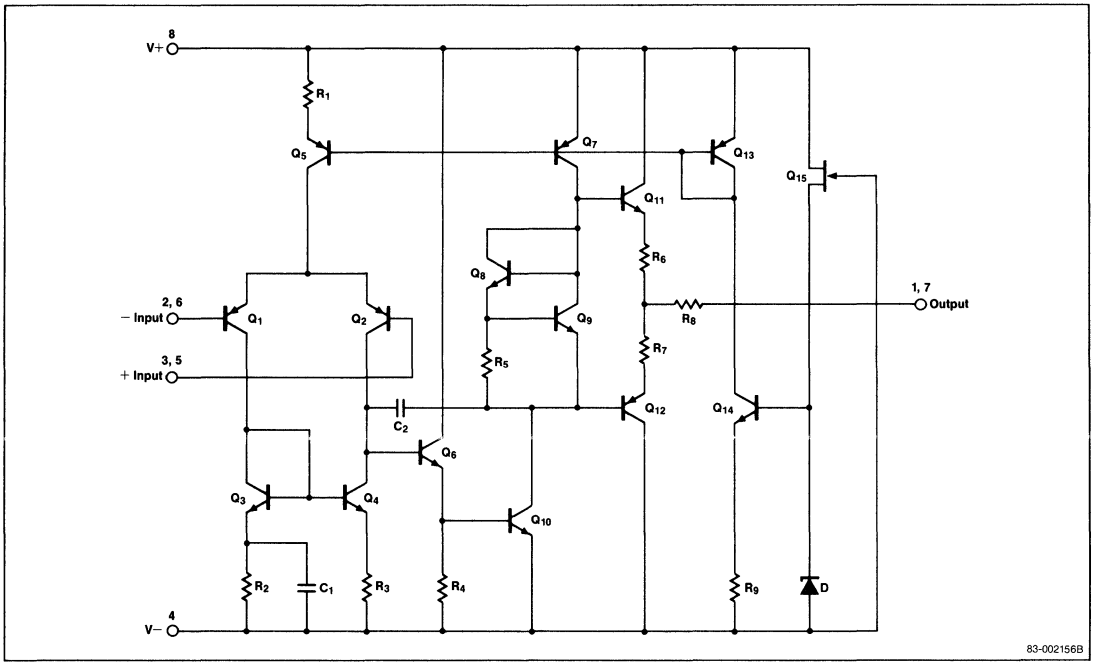
Part Number	Package	Operating Temperature Range
μPC4557C	Plastic DIP	0°C to +70°C

Pin Configuration



Equivalent Circuit

1/2 Circuit



Absolute Maximum Ratings

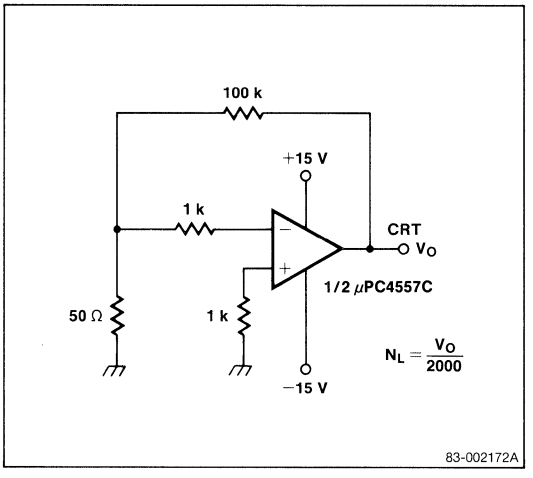
$T_A = 25°C$

Voltage Between V+ and V−	36 V
Power Dissipation (Note 1)	700 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Output Short Circuit Duration	5 s
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Notes: 1. When the ambient temperature is more than 25°C, derate linearly at 7 mW/°C, (T_{Jmax}) = 125°).
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Noise Measurement Circuit

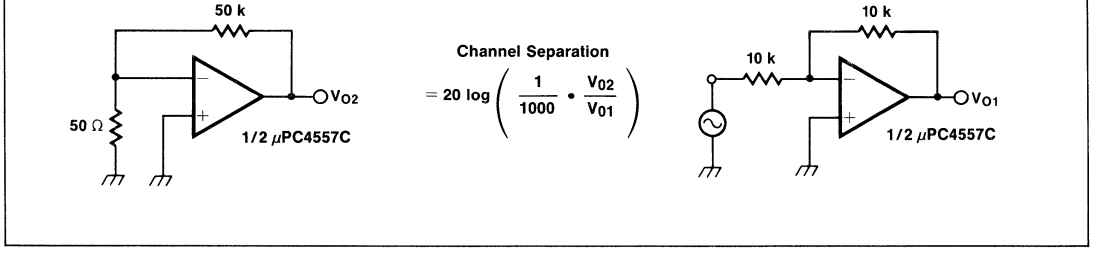


Electrical Characteristics

$T_A = 25°C$, $V\pm = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{IO}		0.5	6.0	mV	$R_S \leq 10$ kΩ
Input Offset Current	I_{IO}		5	200	nA	
Input Bias Current	I_b		180	500	nA	
Large Signal Voltage Gain	A_{VOL}	86	100		dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Power Dissipation	P_D		90	170	mW	Both channels
Common Mode Rejection Ratio	CMRR	70	90		dB	$R_S \leq 10$ kΩ
Supply Voltage Rejection Ratio	SVRR		30	150	μV/V	$R_S \leq 10$ kΩ
Output Voltage Swing	V_{om}	±12	±14		V	$R_L \geq 2$ kΩ
Output Voltage Swing	V_{om}	±10	±11.5		V	$I_O = \pm 25$ mA
Common Mode Input Voltage Range	V_{icm}	±12	±14		V	
Slew Rate	SR		1.0		V/μs	Av = 1
Input Noise Voltage	en		6		μV_{P-P}	$R_S = 1$ kΩ, f = 1 Hz to 1 kHz
Channel Separation	CS		105		dB	f = 1 kHz

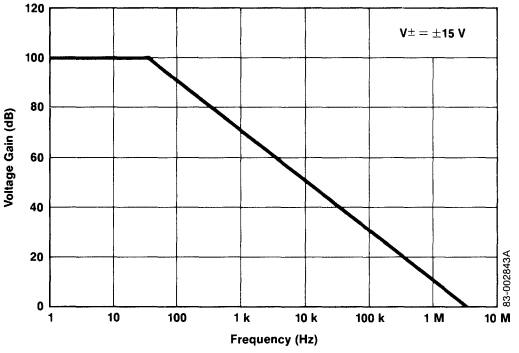
Channel Separation Measurement Circuit



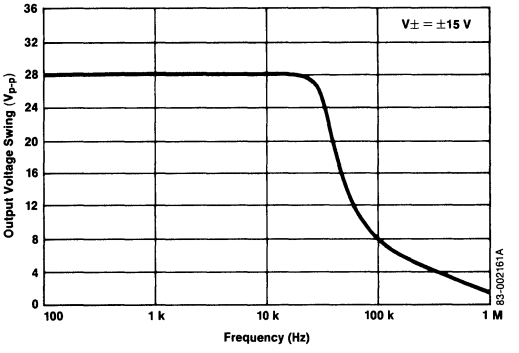
Operating Characteristics

$T_A = 25°C$

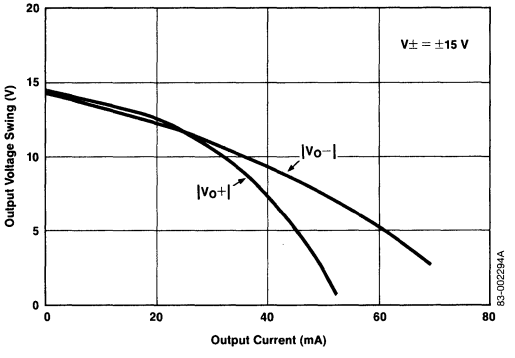
Open Loop Frequency Response



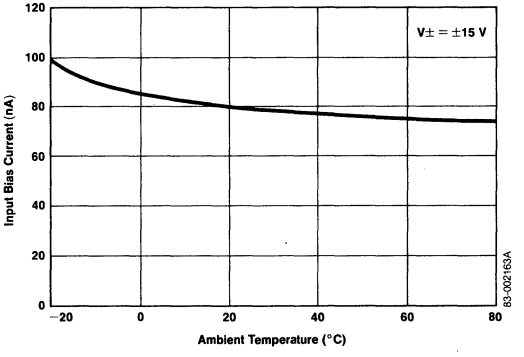
Large Signal Frequency Response



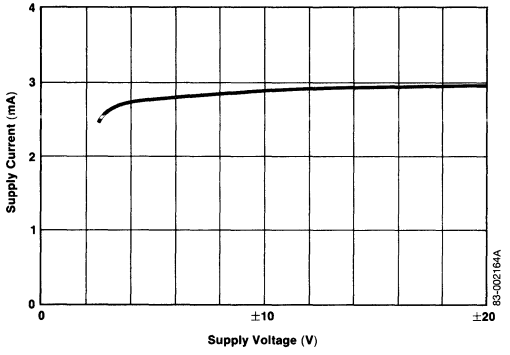
Output Voltage Swing



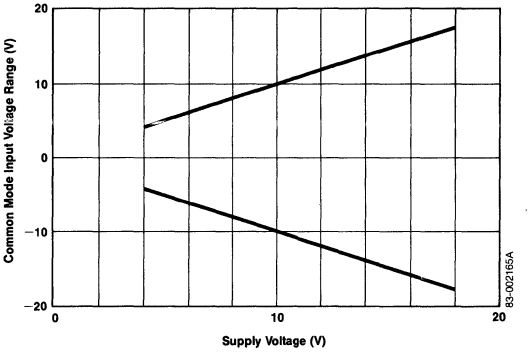
Input Bias Current



Supply Current



Common Mode Input Voltage Range

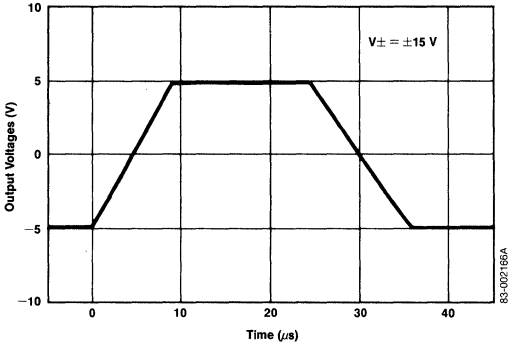


3

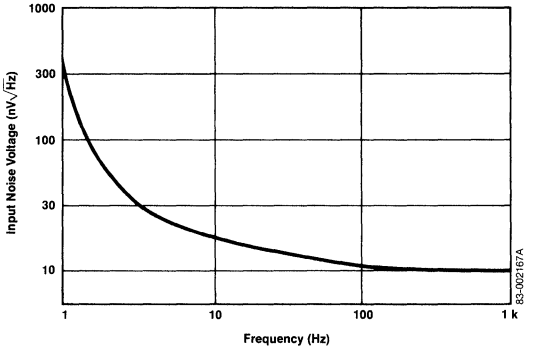
Operating Characteristics (Cont.)

$T_A = 25°C$

Voltage Follower Large Signal Pulse Response

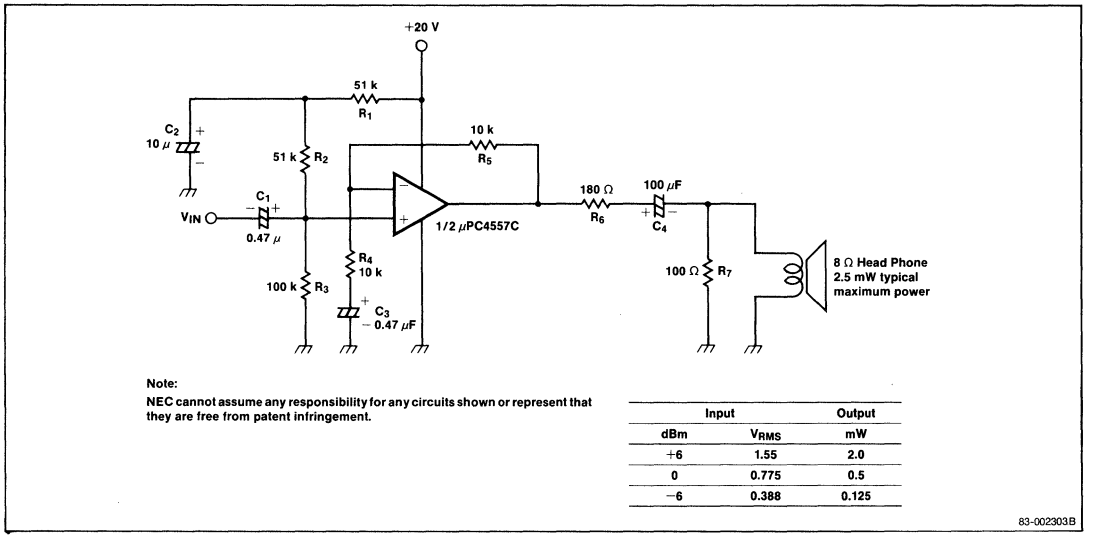


Input Noise Voltage Density



Application Circuit

Head Phone AMP



Note:
NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

Input		Output
dBm	V_{RMS}	mW
+6	1.55	2.0
0	0.775	0.5
−6	0.388	0.125

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μPC4558
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

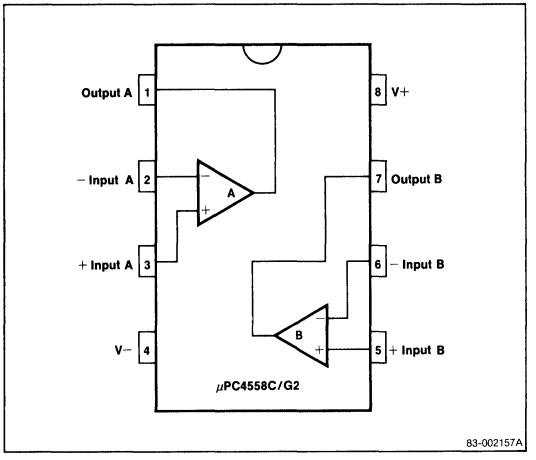
Description

The μPC4558 is a dual operational amplifier with internal frequency compensation. Using low noise lateral PNP input transistors on the amplifier inputs allows the use of this device for signal processing applications, such as low-noise audio preamplifiers and signal conditioning circuits. The simplified output stage eliminates crossover distortion under any normal load conditions.

Features

- ☐ Internal frequency compensation
- ☐ Short-circuit protection
- ☐ Large common mode and differential voltage range
- ☐ No latch-up
- ☐ Low noise
- ☐ RC4558 direct replacement

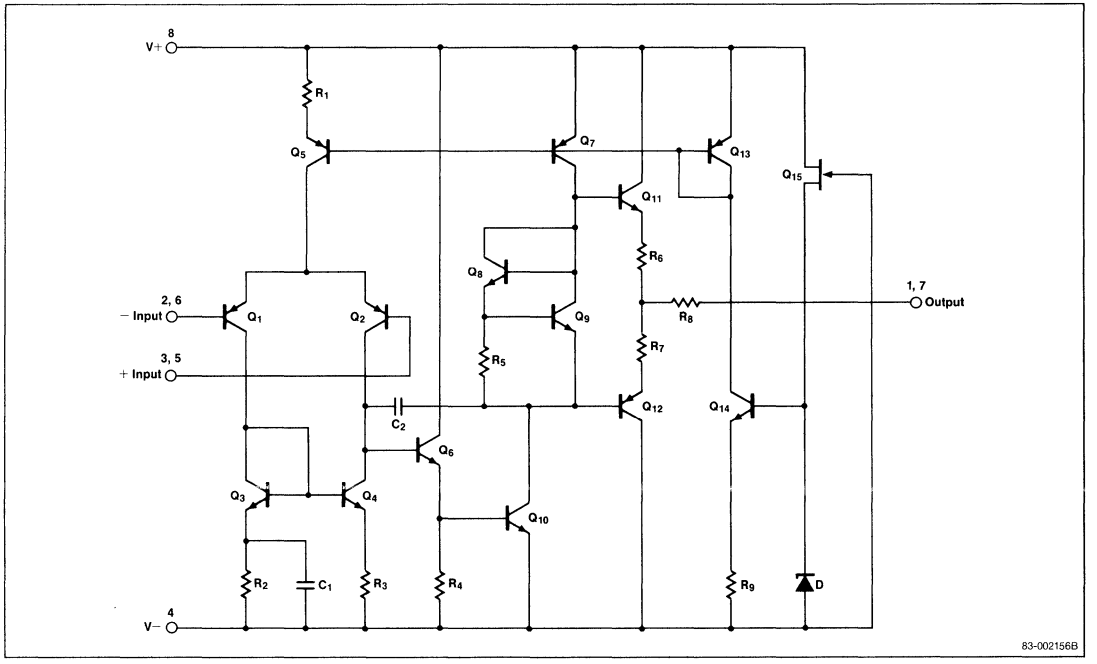
Pin Configuration



3

Equivalent Circuit

1/2 Circuit



Ordering Information

Part Number	Package	Operating Temperature Range
μPC4558C	Plastic DIP	0°C to +70°C
μPC4558G2	Plastic Miniflat	0°C to +70°C

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Power Dissipation, C Package	350 mW
Power Dissipation, G2 Package	440 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range, C or G2 Package	0 to +70°C
Storage Temperature Range, C or G2 Package	−55 to +125°C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

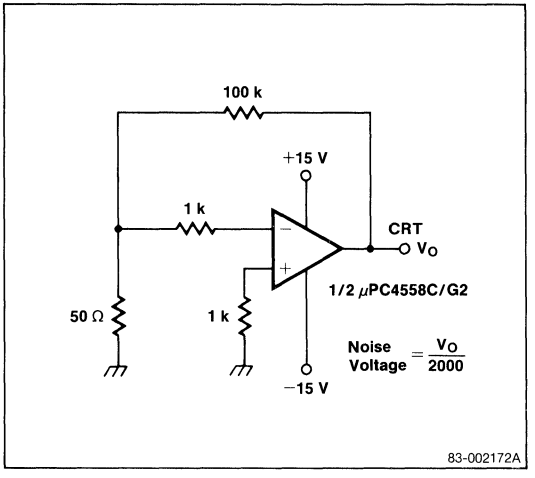
Electrical Characteristics

$T_A = 25°C$, $V\pm = \pm 15$ V

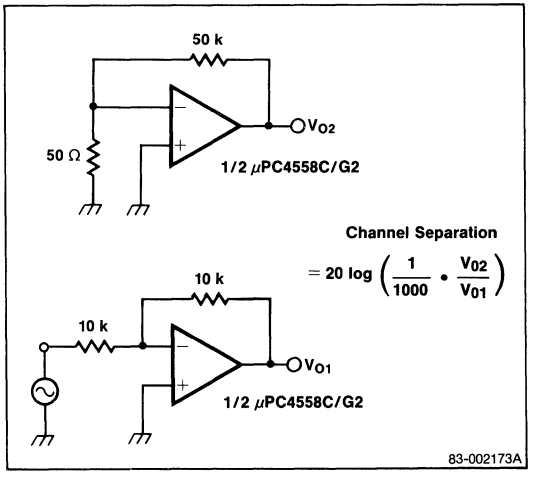
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		0.5	6.0	mV	$R_S \leq 10$ kΩ
Input Offset Current	I_{io}		5	200	nA	
Input Bias Current	I_b		60	500	nA	
Large Signal Voltage Gain	A_{VOL}	86			dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Power Consumption	P_D		90	170	mW	Both channels (see note)
Common Mode Rejection Ratio	CMRR	70	90		dB	$R_S \leq 10$ kΩ
Supply Voltage Rejection Ratio	SVRR		30	150	μV/V	$R_S \leq 10$ kΩ
Output Voltage Swing	V_{om}	±12	±14		V	$R_S \leq 10$ kΩ
		±10	±13		V	$R_S \leq 2$ kΩ
Common Mode Input Voltage Range	V_{icm}	±12	±14		V	
Slew Rate	SR		1.0		V/μs	Av = 1
Input Noise Voltage	en		6		μV_{p-p}	$R_S = 1$ kΩ, f = 1 Hz to 1 kHz
Channel Separation	CS		105		dB	f = 1 kHz

Note: The total of internal power dissipation.

Noise Measurement Circuit



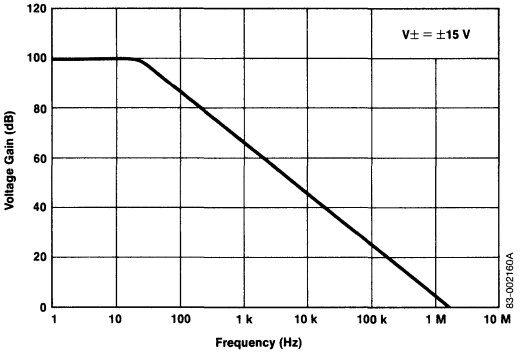
Channel Separation Measurement Circuit



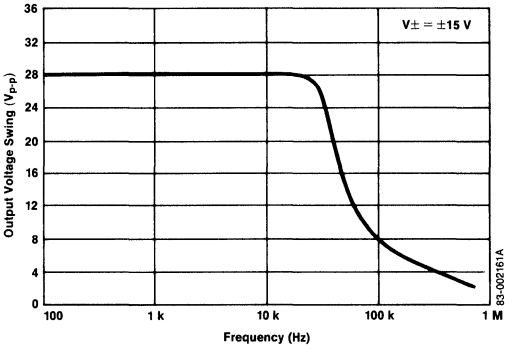
Operating Characteristics

$T_A = 25°C$

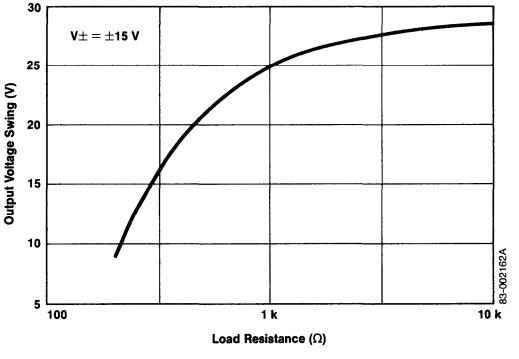
Open Loop Frequency Response



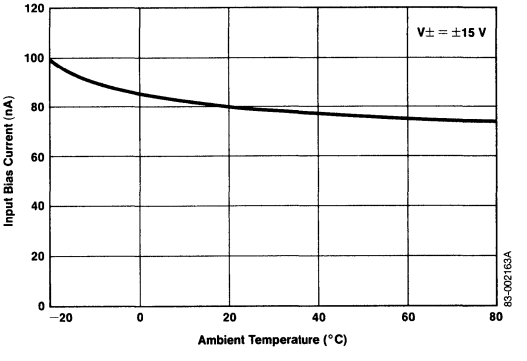
Large Signal Frequency Response



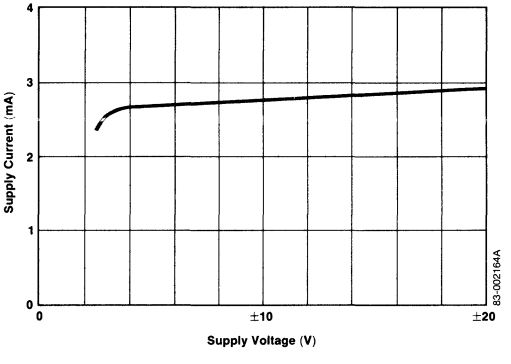
Output Voltage Swing



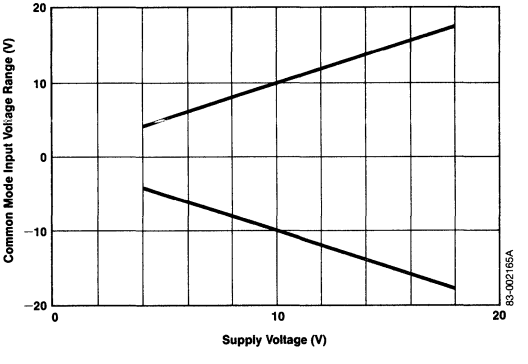
Input Bias Current



Supply Current



Common Mode Input Voltage Range

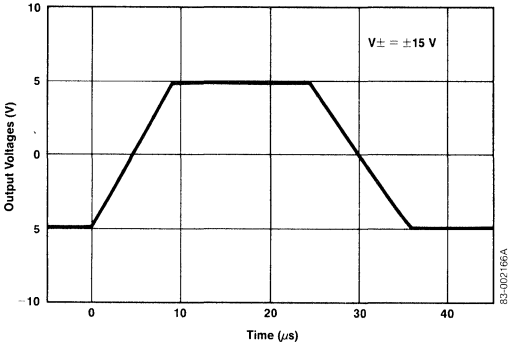


3

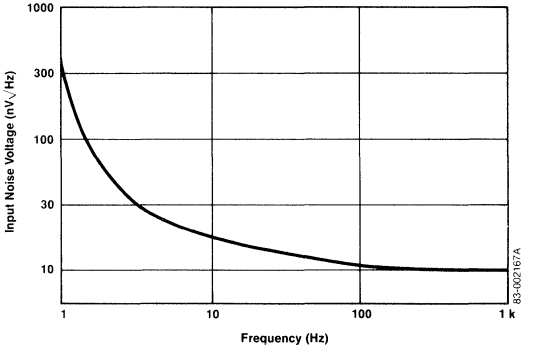
Operating Characteristics (Cont.)

$T_A = 25°C$

Voltage Follower Large Signal Pulse Response

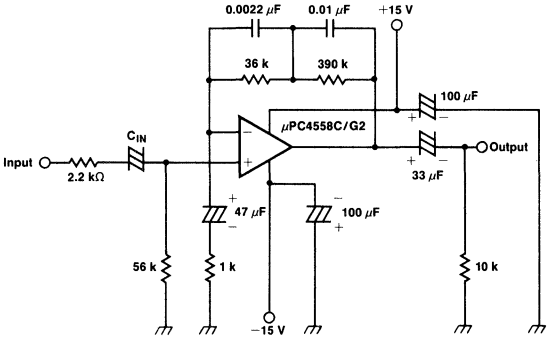


Input Noise Voltage Density



Application Circuit

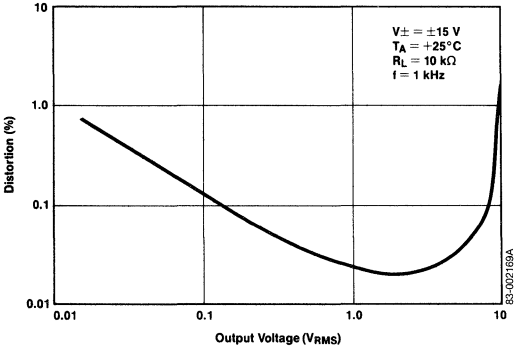
RIAA Preamp



RIAA Preamp A_U = 32.5 dB
Distortion 0.03% (V_O = 1 V_{RMS}, f = 1 kHz
Noise 1.0 μV_{RMS} (Input EQUIV, Input EQUIV
Short Peak Det. Average Indication)

83-002168B

V_O — Distortion Characteristics

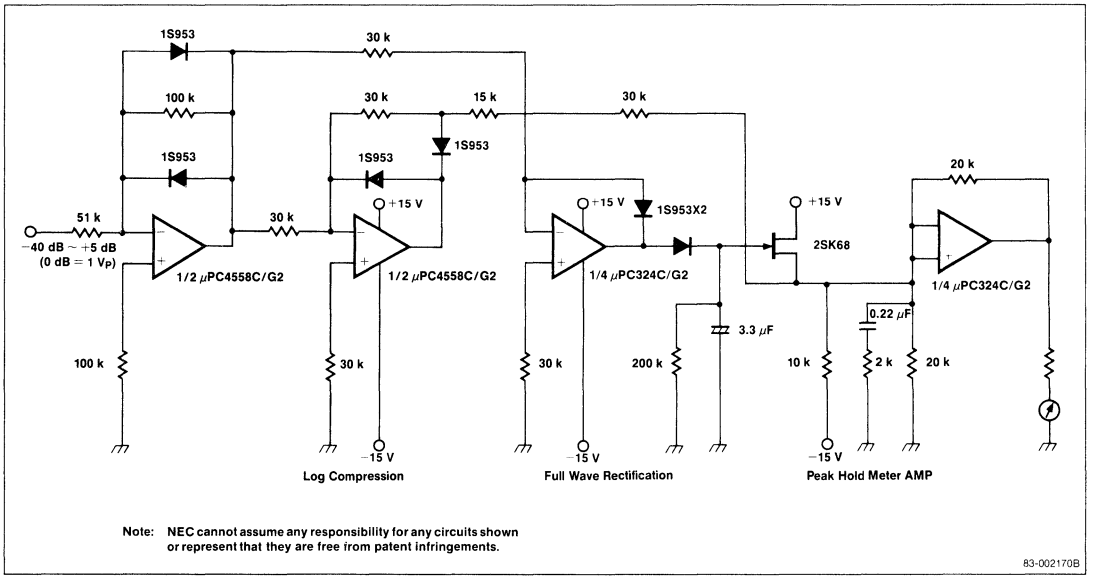


Peak Level Meter

This circuit converts the peak voltage (about ±10 mV to ±10 V) of the input signal to a DC voltage (about 0.2 V to 1.3 V) and drives the meter.

Since the output voltage is proportional to the logarithmic value of the peak voltage of the input signal, indication of a much wider dynamic range can be obtained compared to conventional linear indicating methods.

Peak Level Meter



Note: NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringements.

83-002170B

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μPC4559
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

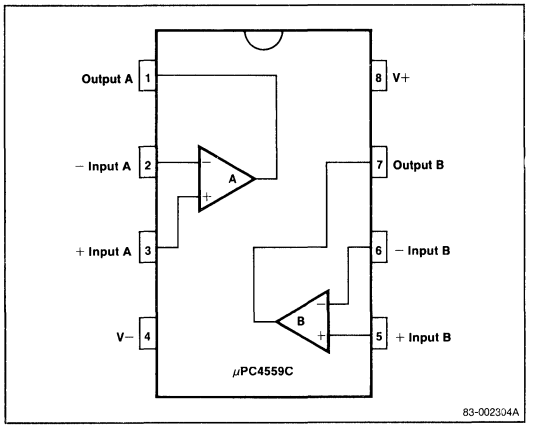
Description

The μPC4559 is a dual operational amplifier featuring improved slew rate and gain bandwidth product when compared to the μPC4558. With low noise and internal frequency compensation, this device is a good choice for active filter designs and audio applications.

Features

- ☐ Internal frequency compensation
- ☐ Large common mode and differential input voltage ranges
- ☐ No latch up
- ☐ Low noise
- ☐ Output short-circuit protection
- ☐ RS4559 direct replacement

Pin Configuration

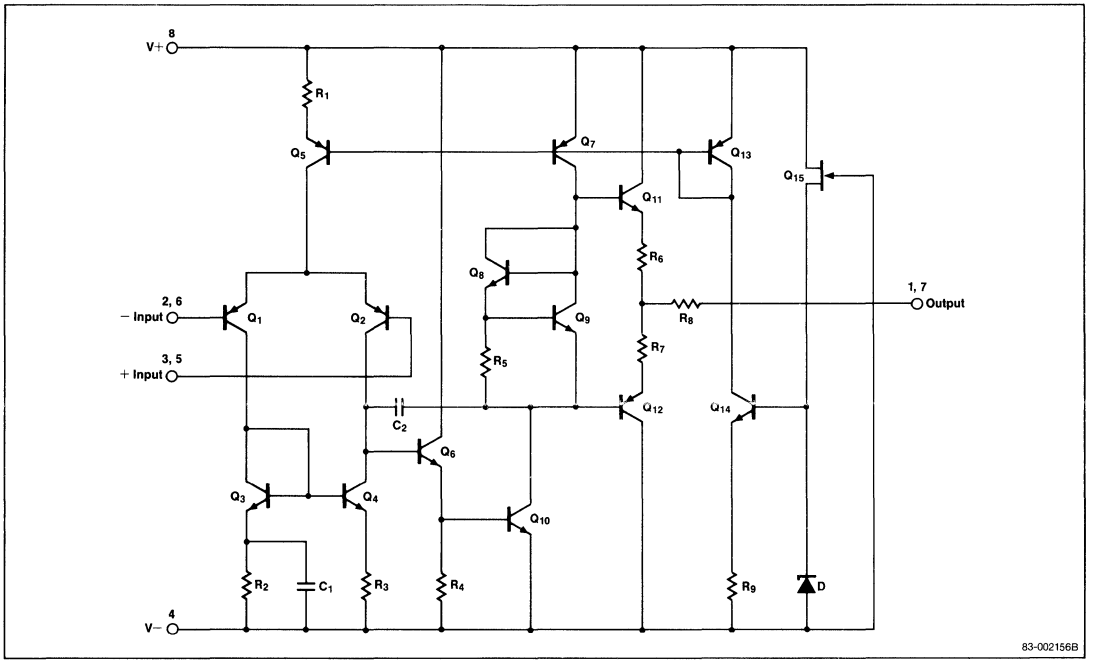


Ordering Information

Part Number	Package	Operating Temperature Range
μPC4559C	Plastic DIP	0° to +70°C

Equivalent Circuit

1/2 Circuit



Absolute Maximum Ratings

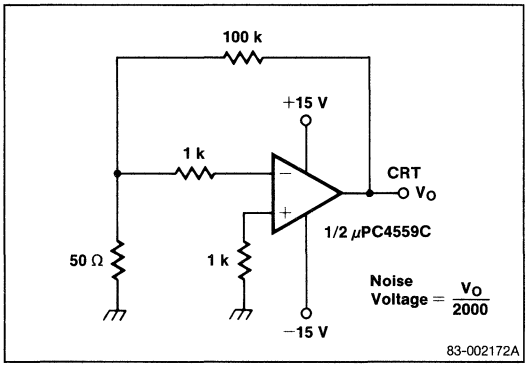
$T_A = 25°C$

Voltage Between V+ and V−	36 V
Power Dissipation	350 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

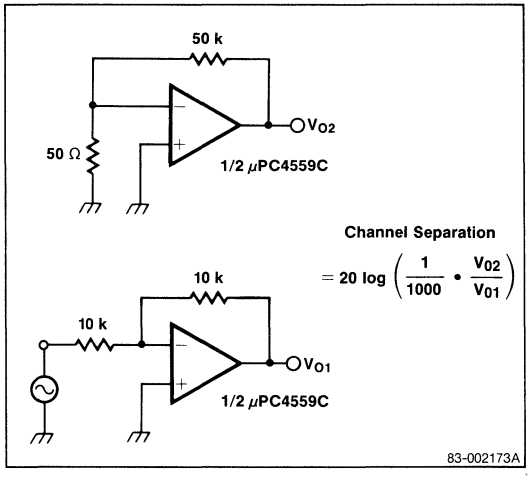
Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Noise Measurement Circuit



Channel Separation Measurement Circuit



Electrical Characteristics

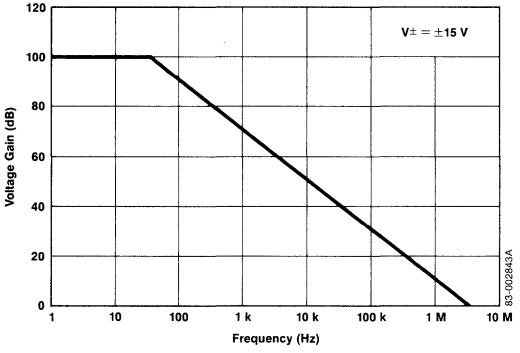
$T_A = 25°C$, $V^{\pm} = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{IO}		0.5	6.0	mV	$R_S \leq 10$ kΩ
Input Offset Current	I_{IO}		5	200	nA	
Input Bias Current	I_B		60	500	nA	
Large Signal Voltage Gain	A_{VOL}	86	100		dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Power Consumption	P_D		90	170	mW	
Common Mode Rejection Ratio	CMRR	70	90		dB	$R_S \leq 10$ kΩ
Supply Voltage Rejection Ratio	SVRR		89	103	dB	$R_S \leq 10$ kΩ
Output Voltage Swing	V_{om}	±12	±14		V	$R_S \geq 10$ kΩ
Output Voltage Swing	V_{om}	±10	±13		V	$R_S \geq 2$ kΩ
Common Mode Input Voltage Range	V_{icm}	±12	±14		V	
Slew Rate	SR		2.0		V/μs	$A_V = 1$
Input Noise Voltage	en		6		μV_{P-P}	$R_S = 1$ kΩ, f = 1 Hz to 1 kHz
Channel Separation	CS		105		dB	f = 1 kHz

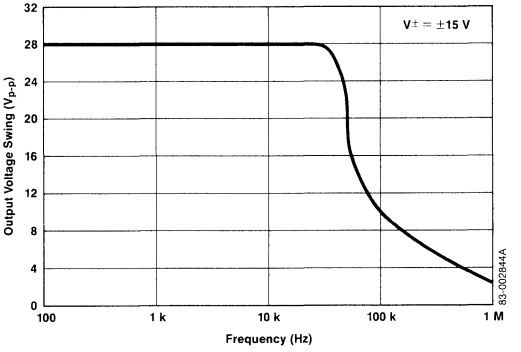
Operating Characteristics

$T_A = 25°C$

Open Loop Frequency Response

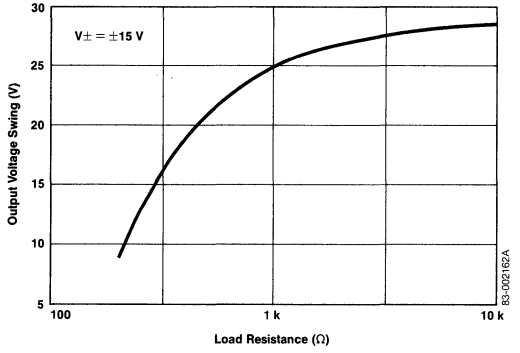


Large Signal Frequency Response

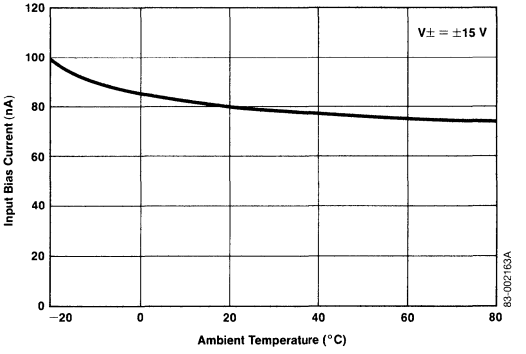


3

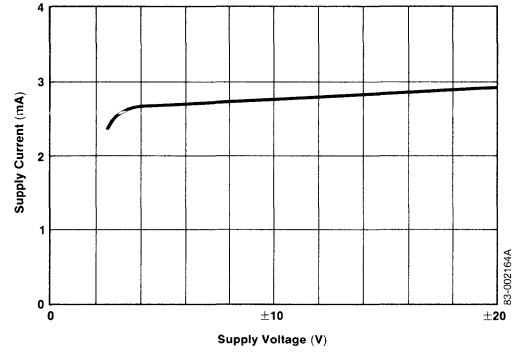
Output Voltage Swing



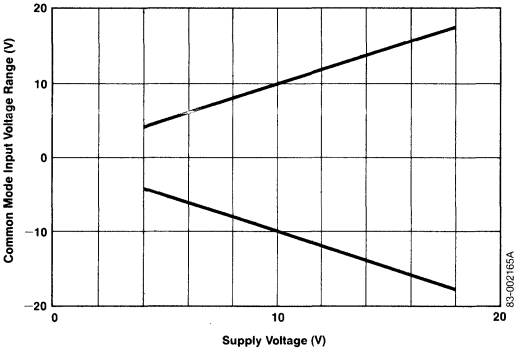
Input Bias Current



Supply Current



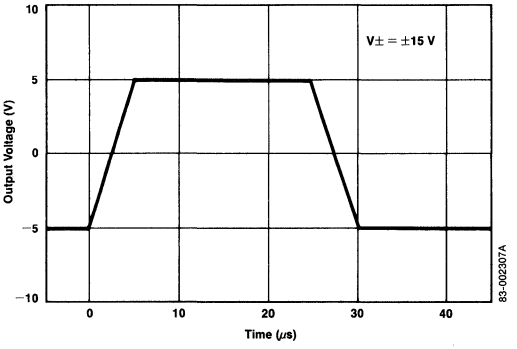
Common Mode Input Voltage Range



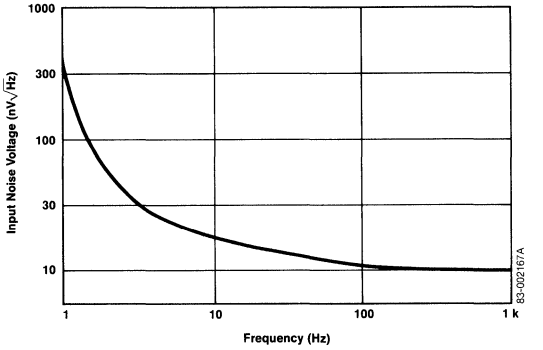
Operating Characteristics (Cont.)

$T_A = 25°C$

Voltage Follower Pulse Response



Input Noise Voltage Density



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μPC4560
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

Description

The μPC4560 is a dual operational amplifier with improved slew rate and gain-bandwidth product when compared to the μPC4559 with unity gain frequency compensation. Low input noise and high output current drive capability makes this device ideal for audio applications and active filters.

Features

- ☐ Internal frequency compensation
- ☐ Large common mode and differential voltage range
- ☐ No latch-up
- ☐ Gain-bandwidth products: 10 MHz typical
- ☐ Low input noise voltage: 6 μV_{p-p} typical

Ordering Information

Part Number	Package	Operating Temperature Range
μPC4560C	Plastic DIP	0° to +70°C
μPC4560G2	Plastic Miniflat	0° to +70°C

Absolute Maximum Ratings

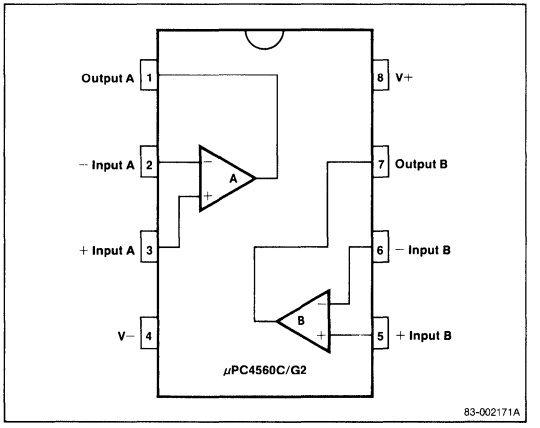
$T_A = 25°C$

Voltage Between V+ and V−	36 V
Power Dissipation (Note 1), C Package	700 mW
Power Dissipation (Note 1), G2 Package	440 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	0 V
Output Short Circuit Duration	0 s
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Note: 1. When the ambient temperature is more than 25°C, derate linearly at 7 mW/°C (T_{JMAX} = 125°C).
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



Electrical Characteristics

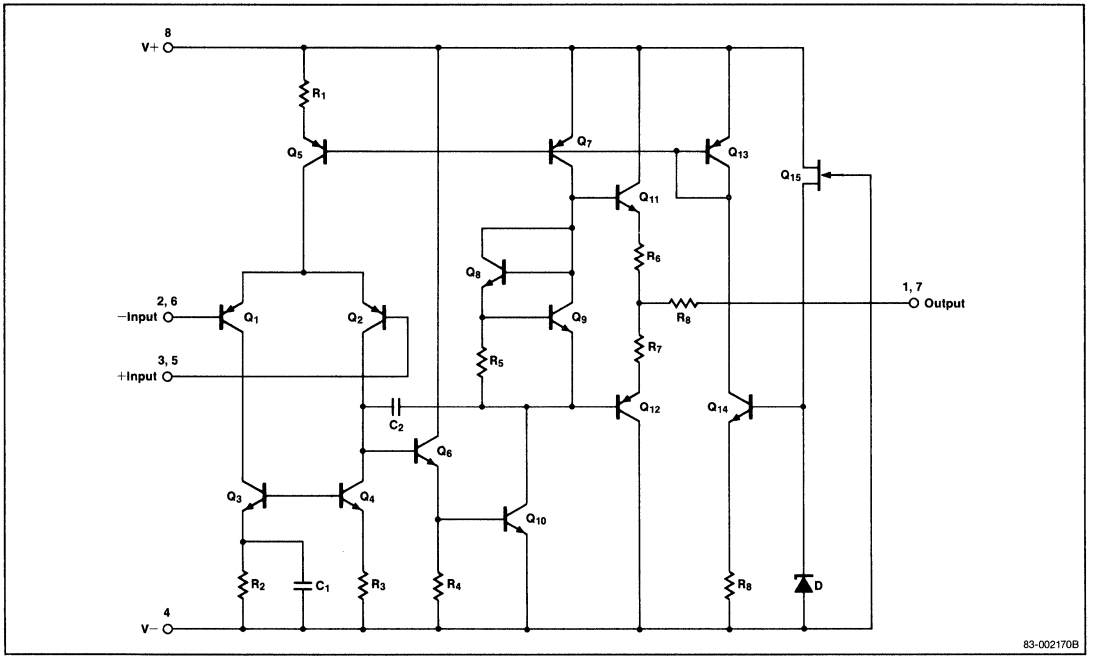
$T_A = 25°C$, $V\pm = \pm 15$ V

Parameter	Symbol	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		0.5	6.0	mV	$R_S \leq 10$ kΩ
Input Offset Current	I_{io}		5	200	nA	
Input Bias Current	I_b		60	500	nA	
Large Signal Voltage Gain	A_{VOL}	88	105		dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Power Consumption	P_D		120	170	mW	Both channels
Common Mode Rejection Ratio	CMRR	70	100		dB	$R_S \leq 10$ kΩ
Supply Voltage Rejection Ratio	SVRR		89	103	dB	$R_S \leq 10$ kΩ
Output Voltage Swing	V_{om}	±12	±14		V	$R_S \geq 2$ kΩ
		±10	±13		V	$I_O = \pm 25$ mA
Common Mode Voltage Range	V_{icm}	±12	±14		V	
Slew Rate	SR		2.8		V/μs	$A_V = 1$
Input Noise Voltage	en		6		μV_{p-p}	$R_S = 1$ kΩ, f = 1 Hz to 1 kHz
Channel Separation	CS		105		dB	f = 1 kHz

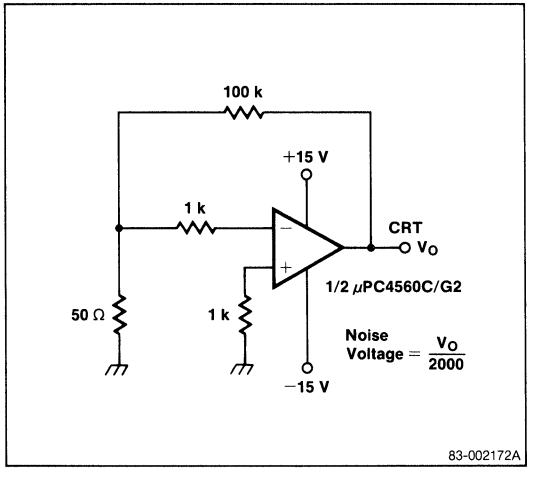
3

Equivalent Circuit

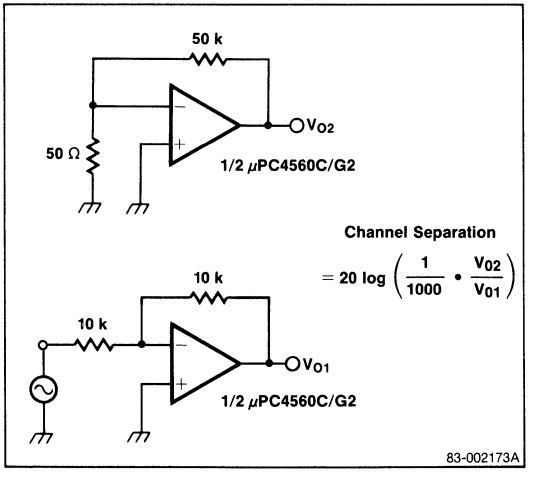
1/2 Circuit



Noise Measurement Circuit



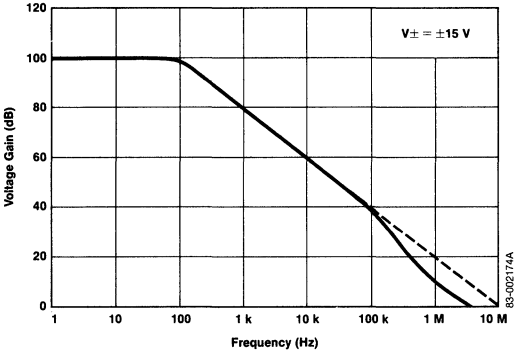
Channel Separation Measurement Circuit



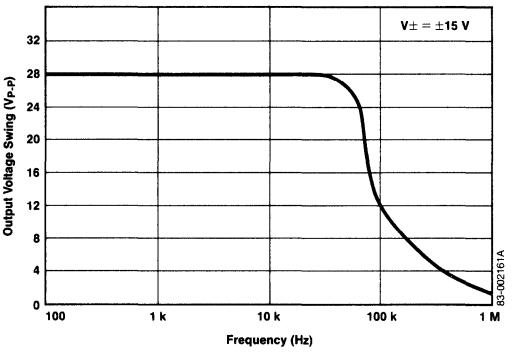
Operating Characteristics

$T_A = 25°C$

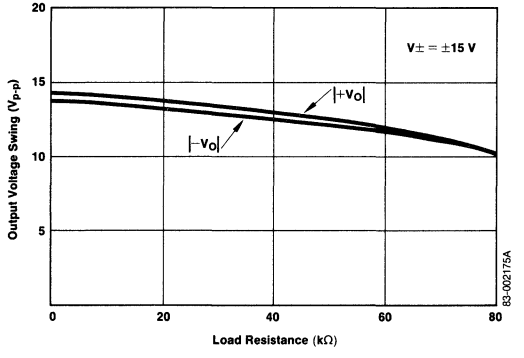
Open Loop Frequency Response



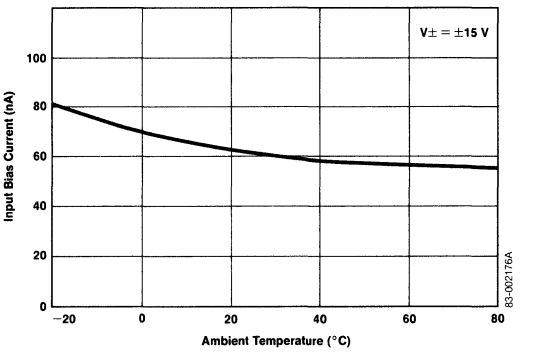
Large Signal Frequency Response



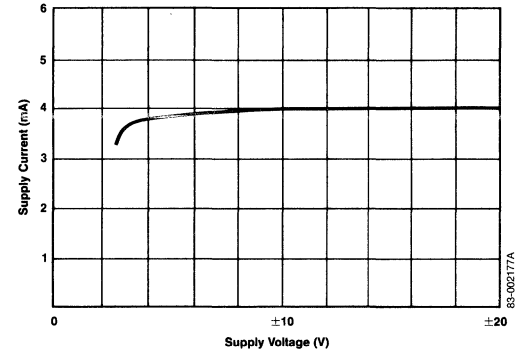
Output Voltage Swing



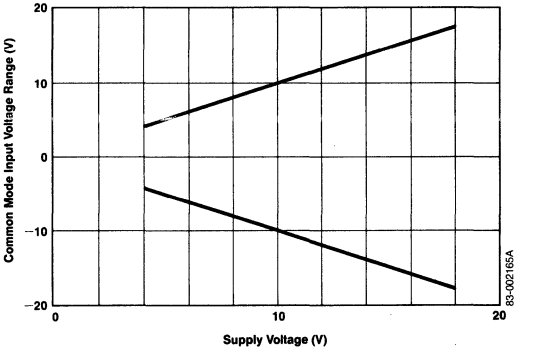
Input Bias Current



Supply Current



Common Mode Input Voltage Range

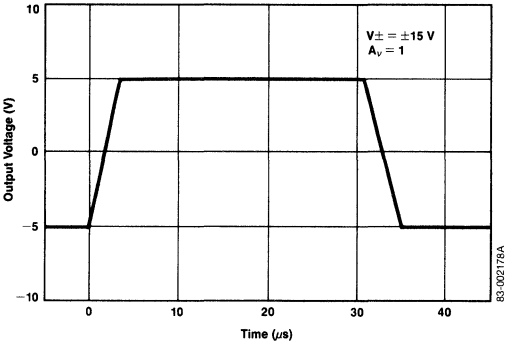


3

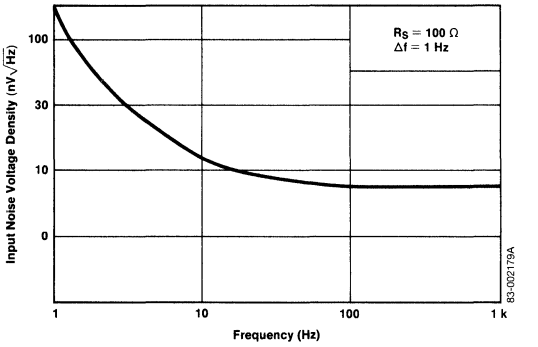
Operating Characteristics (Cont.)

$T_A = 25°C$

Pulse Response

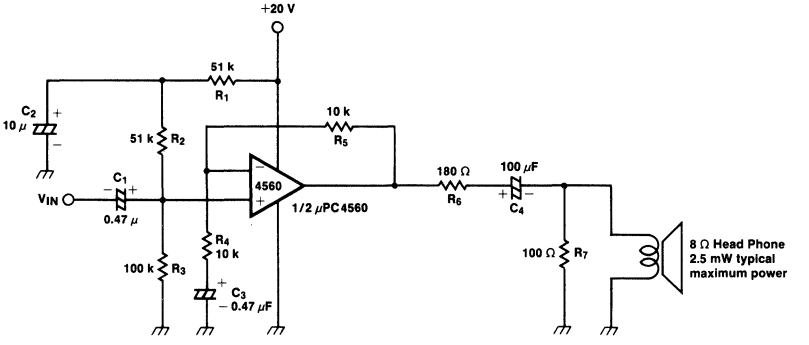


Input Noise Voltage Density



Application Circuit

Head Phone Amp

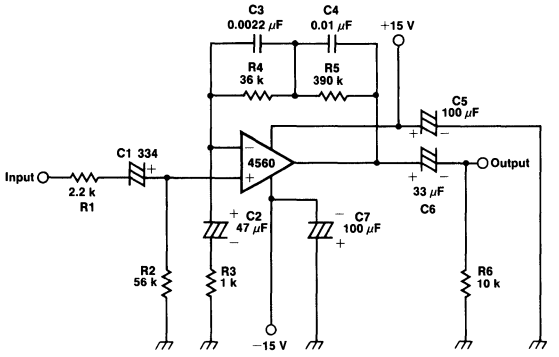


Note:
NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

Input		Output
dBm	V_{RMS}	mW
+6	1.55	2.0
0	0.775	0.5
−6	0.388	0.125

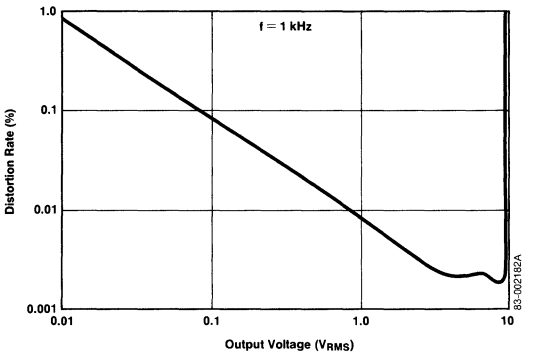
83-002303B

Application Circuit (Cont.)



83-002181B

Distortion Characteristics



3

NEC

NEC Electronics Inc.

μPC4570
DUAL ULTRA LOW-NOISE, WIDEBAND, OPERATIONAL AMPLIFIER

Description

The μPC4570 is an ultralow-noise, wideband, high slew-rate, dual operational amplifier. Input equivalent noise is three times better than the conventional 4558 type op-amp. The gain bandwidth product and the slew-rate are seven times better than 4558. In spite of fast ac performance, the μPC4570 is extremely stable under voltage-follower circuit conditions. Supply current is also improved compared with conventional wideband op-amps. The μPC4570 is an excellent choice for pre-amplifiers and active filters in audio, instrumentation, and communication circuits.

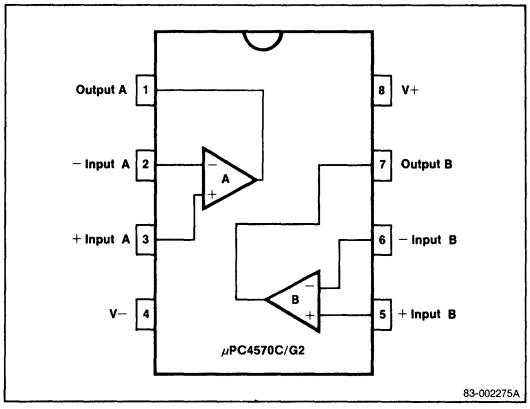
Features

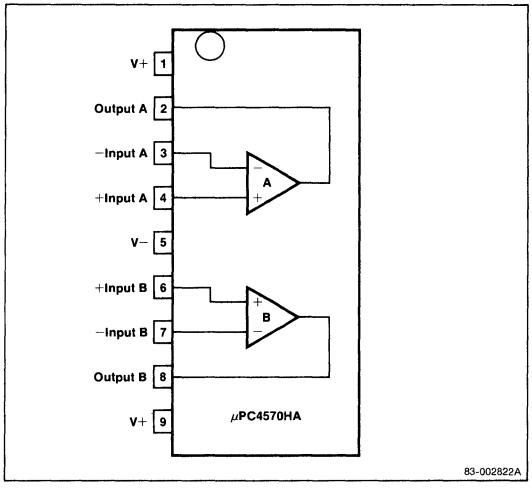
- ☐ Ultralow noise: en = 4.5 nV/$\sqrt{Hz}$
- ☐ High slew-rate: 7 V/μs
- ☐ Wide bandwidth: GBW = 15 MHz at 100 kHz
- ☐ Internal full-frequency compensation
- ☐ NE5532 equivalent

Ordering Information

Part Number	Package	Operating Temperature Range
μPC4570C	Plastic DIP	−20 to +70°C
μPC4570G2	Plastic Miniflat	−20 to +70°C
μPC4570HA	Plastic SIP	−20 to +70°C

Pin Configurations

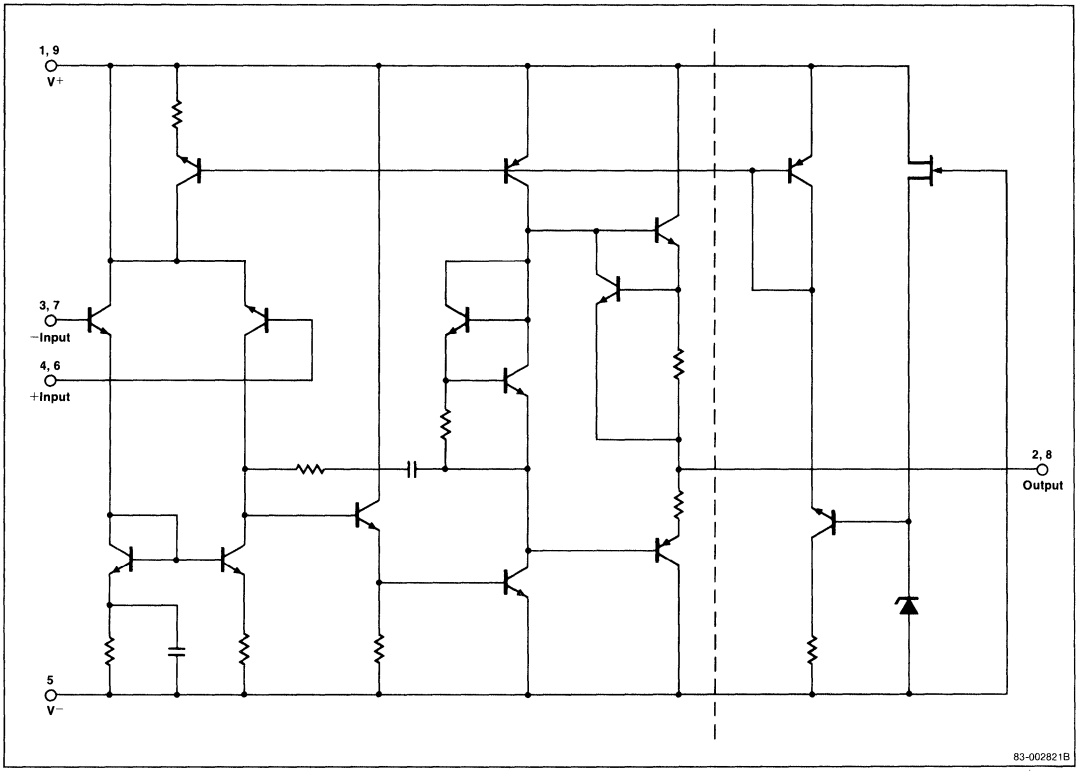




3

Equivalent Circuit

1/2 Circuit



Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Differential Input Voltage	±30 V
Power Dissipation, C and HA Packages (Note 1)	350 mW
Power Dissipation, G2 Package (Note 2)	440 mW
Input Voltage (Note 3)	±15 V
Output Short Circuit Duration	10 s
Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−55 to +125°C

Notes: 1. Thermal derating factor is 5 mW/°C when ambient temperature is higher than 55°C.

2. Thermal derating factor is 4.4 mW/°C when ambient temperature is higher than 25°C.

3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to supply voltages.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

$T_A = 25°C$, $V± = ±15$ V

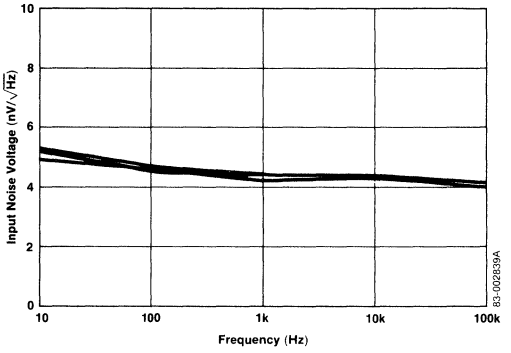
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input offset voltage	V_{io}		0.3	5	mV	$R_S = 50\ \Omega$
Input offset current	I_{io}		10	200	nA	
Input bias current	I_b		500	1000	nA	
Large signal voltage gain	A_{VOL}	90	110		dB	$R_L = 2$ kΩ, $V_O = ±10$ V
Supply current	I_{CC}		5	8	mA	
Common mode rejection ratio	CMRR	80	100		dB	
Supply voltage rejection ratio	SVRR	80	100		dB	
Output voltage swing	V_{om}	±12	±13.5		V	$R_L \geq 10$ kΩ
Output voltage swing	V_{om}	±12	±12.8		V	$R_L \geq 2$ kΩ
Common mode voltage	V_{icm}	±10	±14		V	
Slew rate	SR	57			V/μs	$R_L = 2$ kΩ
Gain bandwidth	GBW	10	15		MHz	
Power bandwidth	PBW	50	70		kHz	$V_O = 27\ V_{p-p}$, THD ≤ 1%
Unity gain frequency	f_{unity}		9		MHz	
Phase margin			60		°	
Total harmonic distortion	THD		0.002		%	$V_O = 3\ V_{RMS}$, 2 to 20 kHz
Channel separation	CS		120		dB	f = 20 Hz to 20 kHz
Input RMS noise voltage			1.2		μV_{RMS}	RIAA
			0.5	0.65	μV_{RMS}	Flat + JISA
Input noise voltage	e_n		4.5		$nV/\sqrt{Hz}$	f = 1 kHz
Input noise current	i_n		0.7		$pA/\sqrt{Hz}$	f = 1 kHz

3

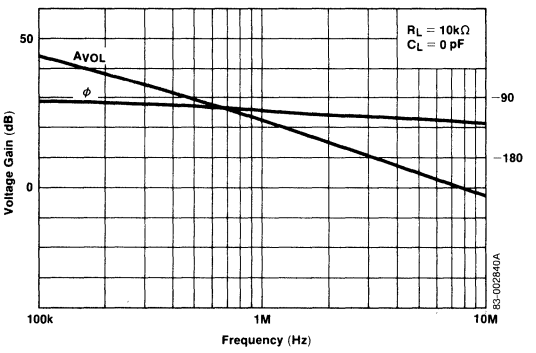
Operating Characteristics

$T_A = 25°C$

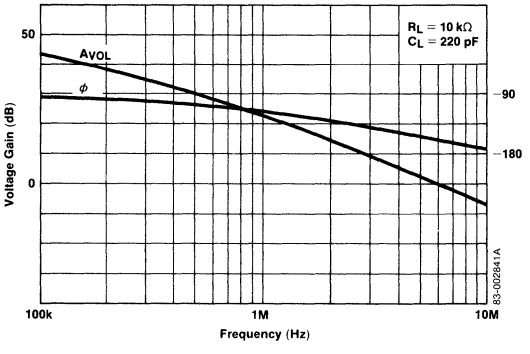
Input Noise vs Frequency Characteristics



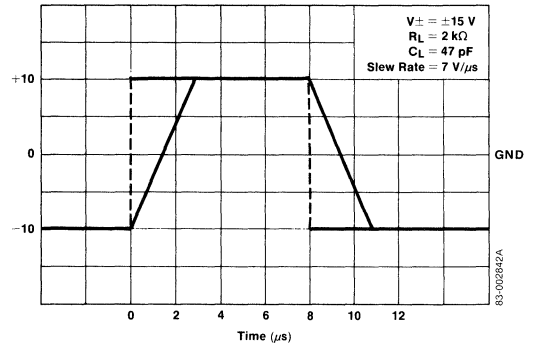
Phase Gain vs Frequency



Gain, Phase vs Frequency



Voltage Follower Pulse Response



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μPC324
QUAD LOW-POWER OPERATIONAL AMPLIFIER

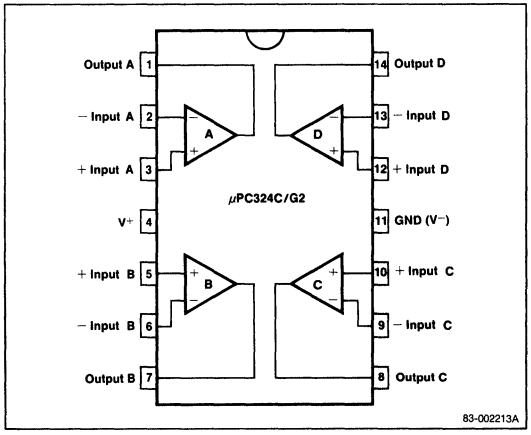
Description

The μPC324 is a quad operational amplifier designed to operate from either single or split power supplies, with very low current drain. The input common mode voltage of these amplifiers includes ground and they are internally frequency compensated for unity gain stability.

Features

- ☐ Internal frequency compensation
- ☐ Large output voltage swing: 0 V to V+ − 1.5 V DC
- ☐ Input common mode voltage range includes ground
- ☐ Wide power supply range:
  Single supply 3 V to 30 V DC
  Dual supplies ±1.5 V to ±15 V DC
- ☐ LM324 direct replacement

Pin Configuration

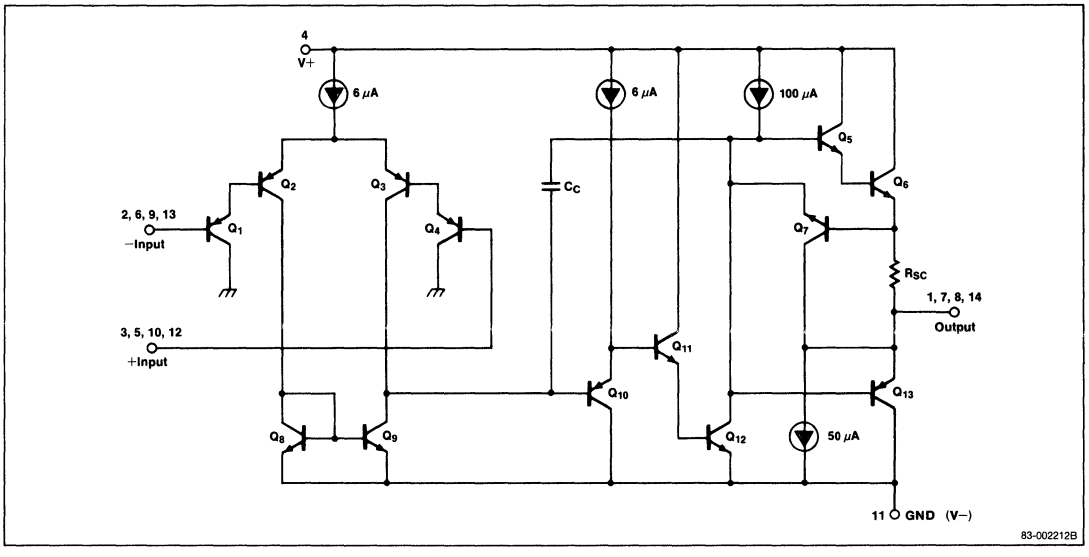


Ordering Information

Part Number	Package	Operating Temperature Range
μPC324C	Plastic DIP	0° to +70°C
μPC324G2	Plastic Miniflat	0° to +70°C

Equivalent Circuit

1/4 Circuit



3

Absolute Maximum Ratings

$T_A = 25°C$, $V\pm = \pm 5$ V

Voltage Between V+ and V−	32 V
Differential Input Voltage	32 V
Input Voltage	−0.3 to +32 V
Power Dissipation, C Package	570 mW
Power Dissipation, G Package	550 mW
Operating Temperature Range, C or G Package	0 to +70°C
Storage Temperature Range, C or G Package	−55 to +125°C

Electrical Characteristics

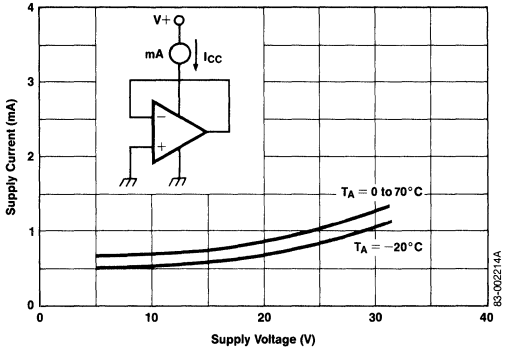
$T_A = 25°C$, $V\pm = \pm 5$ V

Parameter	Symbol	Limit Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		2	7	mV	$R_S = 0\ \Omega$
Input Bias Current	I_b		45	250	nA	
Input Offset Current	I_{io}		5	50	nA	
Common Mode Input Voltage Range	V_{icm}	0		V+ − 1.5	V	
Supply Current	I_{CC}		0.8	2	mA	$R_L = \infty$ on all op-amps
Large Signal Voltage Gain	A_{VOL}	88	100		dB	$R_L \geq 2$ kΩ
Output Voltage Swing	V_{OM}	0		V+ − 1.5	V	$R_L = 2$ kΩ
Common Mode Rejection Ratio	CMRR	65	85		dB	
Supply Voltage Rejection Ratio	SVRR	65	10		dB	
Channel Separation	CS		120		dB	f = 1 kHz to 20 kHz
Output Current (Source)	$I_{OSOURCE}$	20	40		mA	+ Input = 1 V, − Input = 0 V
Output Current (Sink)	I_{OSINK}	10	20		mA	− Input = 1 V, + Input = 0 V
Output Current (Sink)	I_{OSINK}	12	50		mA	− Input = 1 V, + Input = 0 V

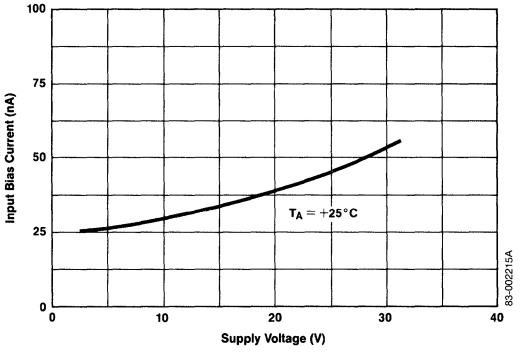
Operating Characteristics

$T_A = 25°C$

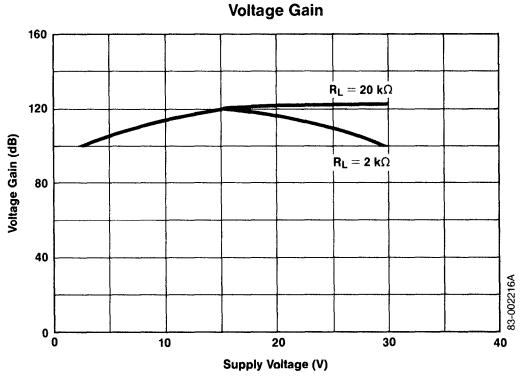
Supply Current



Input Bias Current



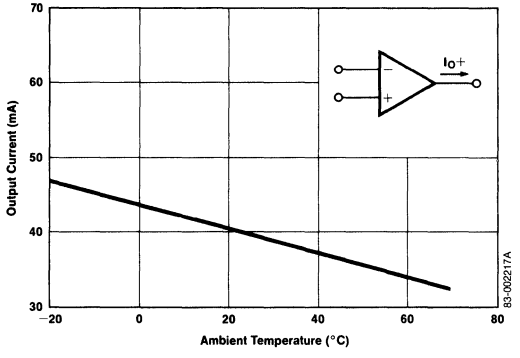
Voltage Gain



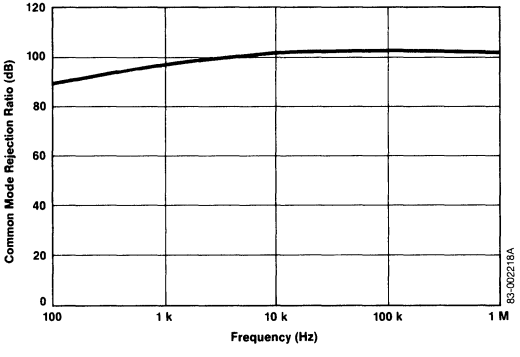
Operating Characteristics (Cont.)

$T_A = 25°C$

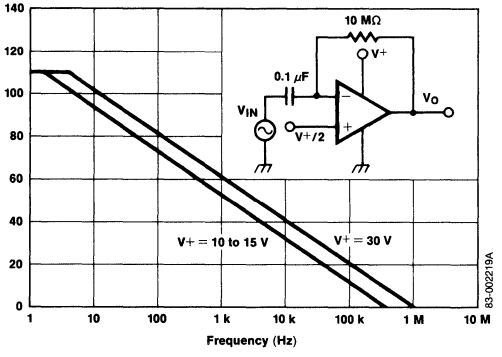
Current Limiting



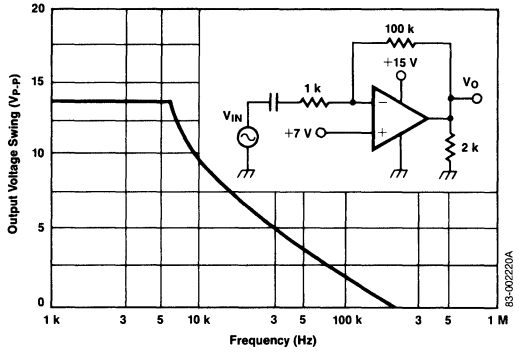
Common Mode Rejection Ratio



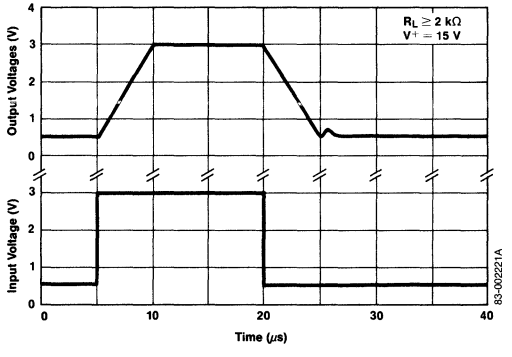
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Large Signal Pulse Response



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μPC3403
QUAD HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

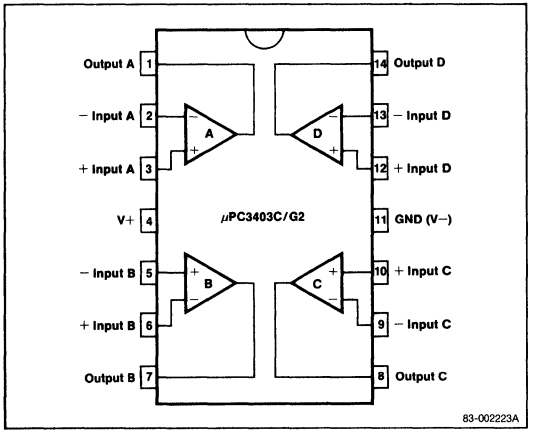
Description

The μPC3403 quad operational amplifier is designed with four independent high gain frequency compensated operational amplifiers. Featuring operations from either single or split power supplies from 3 V to ±18 V. The common mode input range includes the negative supply which eliminates the need for external biasing circuitry in most applications.

Features

- ☐ Input common mode voltage range includes ground or negative supply
- ☐ Output voltage can swing to ground or negative supply
- ☐ Wide power supply range:
  - Single supply of 3.0 to 36 V
  - Split supplies of ±1.5 to 18 V
- ☐ Class AB output stage for minimal crossover distortion
- ☐ Short-circuit protected outputs
- ☐ MC3403 direct replacement

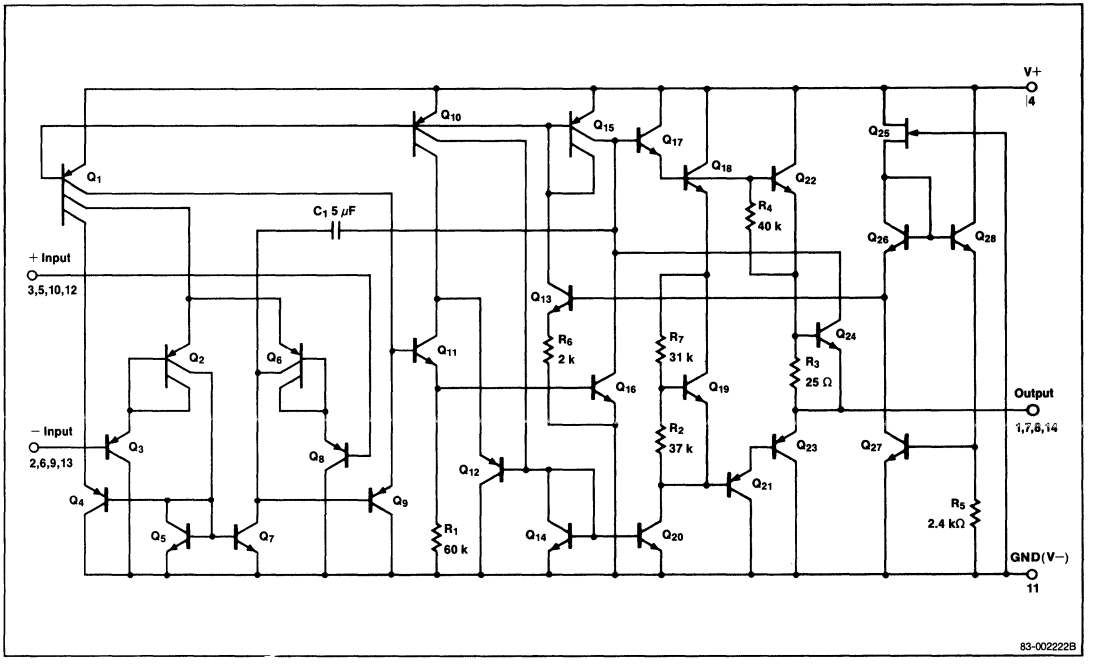
Pin Configuration



3

Equivalent Circuit

1/4 Circuit



Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Differential Input Voltage	±36 V
Input Voltage (Note 1)	±18 V
Power Dissipation, C Package	570 mW
Power Dissipation, G2 Package	550 mW
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Note: 1. The absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ordering Information

Part Number	Package	Operating Temperature Range
μPC3403C	Plastic DIP	0°C to +70°C
μPC3403G2	Plastic Miniflat	0°C to +70°C

Electrical Characteristics

$T_A = 25°C$, $V^{\pm} = \pm 15$ V

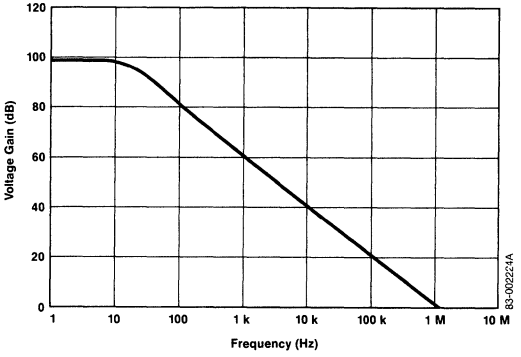
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{IO}		2.0	7.0	mV	V+ = +5 V, V− = GND
Input Offset Current	I_{IO}		5	50	nA	V+ = +5 V, V− = GND
Input Bias Current	I_b		45	250	nA	V+ = +5 V, V− = GND
Large Signal Voltage Gain	A_{VOL}	86	98		dB	$V_O = \pm 10$ V, $R_L = 2$ kΩ
		86	98		dB	V+ = +5 V, V− = GND, $R_L = 2$ kΩ
Input Voltage Range	V_{icm}	+13 to −15	+13.5 to −15		V	
Common Mode Rejection Ratio	CMRR	70	90		dB	
Supply Voltage Rejection Ratio	SVRR		89	103	dB	
				103	dB	V+ = +5 V, V− = GND
Supply Current	I_{CC}		2.8	7.0	mA	$V_O = 0$, $R_L = \infty$, all channels
			2.5	7.0	mA	V+ = +5 V, V− = GND, all channels
Output Short Circuit Current (see Note)	I_{OSHORT}	±10	±20	±45	mA	
Output Voltage Swing	V_{OM}	±12	±13.5			$R_L = 10$ kΩ
		±10	±13		V	$R_L = 2.0$ kΩ
		V+ − 1.7	V+ − 1.5		V	$R_L = 10$ kΩ, 5 V ≤ V+ ≤ 30 V, V− = GND
Channel Separation	CS		120		dB	f = 1 kHz to 20 kHz

Note: Do not exceed the maximum power dissipation rating.

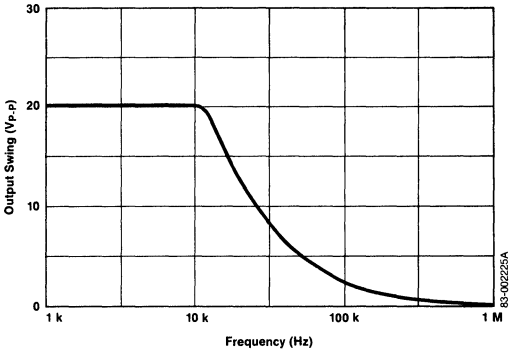
Operating Characteristics

$T_A = 25°C$

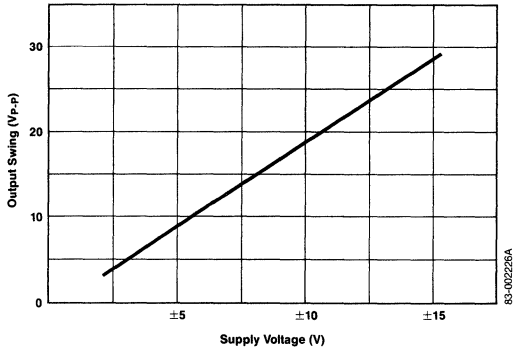
Open Loop Frequency Response



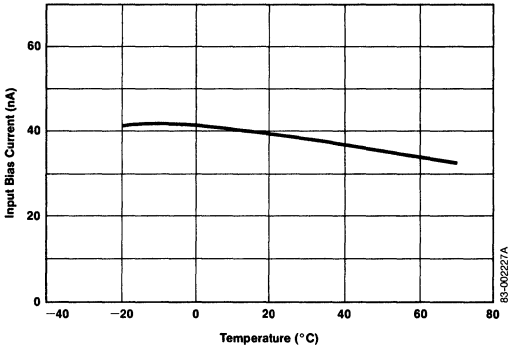
Power Bandwidth



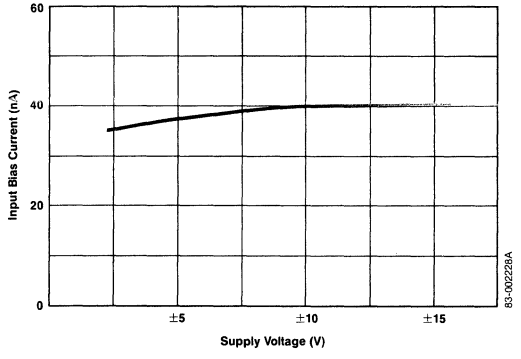
Output Swing



Input Bias Current



Input Bias Current



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μPC4064
QUAD J-FET INPUT LOW-POWER OPERATIONAL AMPLIFIER

Description

The μPC4064 is a low power J-FET input quad operational amplifier that will operate at voltage levels as low as ±2.0 V. Input current is typically less than 1 mA. With input bias and offset currents as low as a few pA, the μPC4064 is an excellent choice for hand-held measurement equipment.

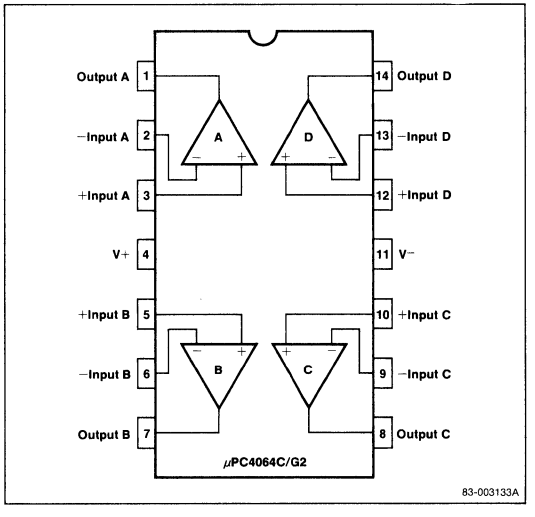
Features

- ☐ Low supply current
- ☐ Very low input bias and offset currents
- ☐ High slew rate
- ☐ High input impedance
- ☐ Output short circuit protection
- ☐ Internal frequency compensation
- ☐ TL064 direct replacement

Ordering Information

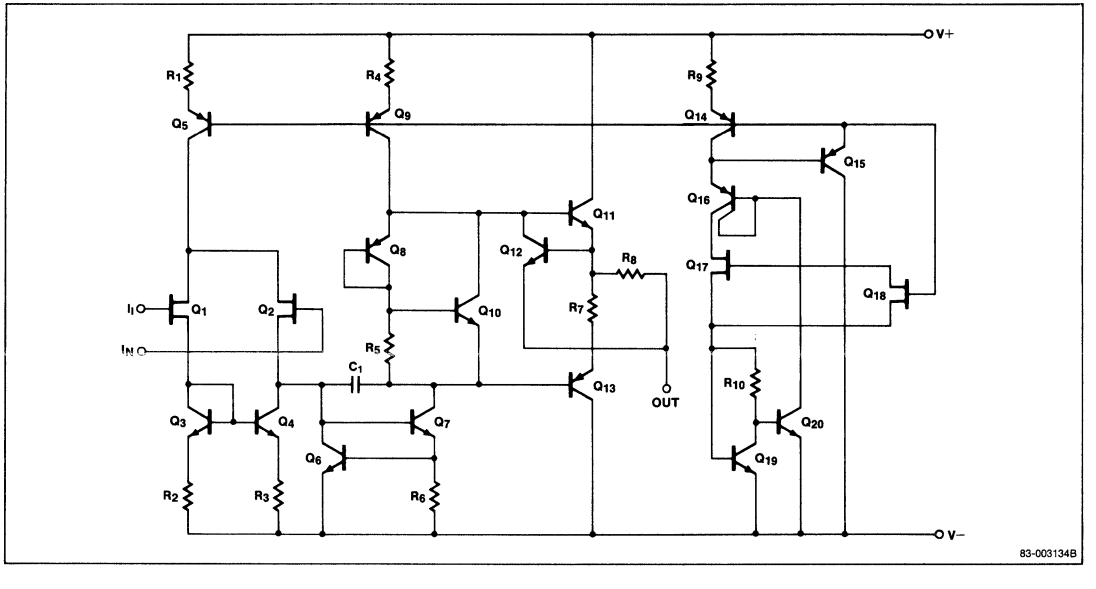
Part Number	Package	Operating Temperature Range
μPC4064C	14-pin plastic DIP	−20 to +70°C
μPC4064G2	14-pin Miniflat	−20 to +70°C

Pin Configuration



Equivalent Circuit

1/4 Circuit



3

Absolute Maximum Ratings

$T_A = 25°C$

Supply Voltage Differential	36 V
Power Dissipation, C Package (Note 1)	570 mW
Power Dissipation, G2 Package (Note 2)	550 mW
Differential Input Voltage (Note 3)	±30 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−20 to 70°C

Note:

1. Derate at 8 mW/°C when $T_A > 25°C$.
2. Derate at 5.5 mW/°C when $T_A > 25°C$.
3. For supply voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Recommended Operating Conditions

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply Voltage	V_{SUPP}	±2		±16	V
Output Current	I_O			5	mA
Load Capacitance	C_L			220	pF

Electrical Characteristics

$T_A = +25°C$, $V_{SUPP} = ±15$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Offset Voltage	V_{io}		2	10	mV	$R_S = 50Ω$
Input Offset Voltage	V_{io}			15	mV	$R_S = 50\ Ω$, $T_A = T_{opt}$
Input Offset Voltage Drift	$ΔV_{io}/ΔT$		10		μV/°C	$R_S = 50\ Ω$, $T_A = T_{opt}$
Input Offset Current	I_{io}		5	50	pA	
Input Offset Current	I_{io}			1.5	nA	$T_A = T_{opt}$
Input Bias Current	I_b		10	100	pA	
Input Bias Current	I_b			3	nA	$T_A = T_{opt}$
Large Signal Voltage Gain	A_{VOL}	70	76		dB	R1 = 10k, $V_O = 10$ V
Supply Current	I_{SUPP}		800	1000	μA	
Common Mode Rejection Ratio	CMRR	70	95		dB	
Power Supply Rejection Ratio	PSRR	70	95		dB	
Output Voltage Swing	$±V_O$	±12	±14		V	R1 = 10k
Common Mode Input Voltage	V_{cm}	±12	+15 −13		V	
Output Current	I_O	5 −3.5			mA	$±V_O = ±10$ V
Slew Rate	SR		3		V/μs	R1 = 10k
Input Noise Voltage	en		30		nV/√Hz	f = 1 kHz
Gain Bandwidth Product	GBW		1		MHz	
Channel Separation	CS		120		dB	f = 1 to 20 kHz

Electrical Characteristics

$T_A = +25°C$, $V_{SUPP} = ±5$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Large Signal Voltage Gain	A_{VOL}	20			dB	
Common Mode Rejection Ratio	CMRR	70	90		dB	
Power Supply Rejection Ratio	PSRR	70	90		dB	
Output Voltage Swing	$±V_O$	±3.8	±4.1		V	R1 = 10k
Common Mode Input Voltage	V_{cm}	+4.7 −2.8	+5.2 −3.5		V	

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μPC4074
QUAD J-FET INPUT LOW-NOISE OPERATIONAL AMPLIFIER

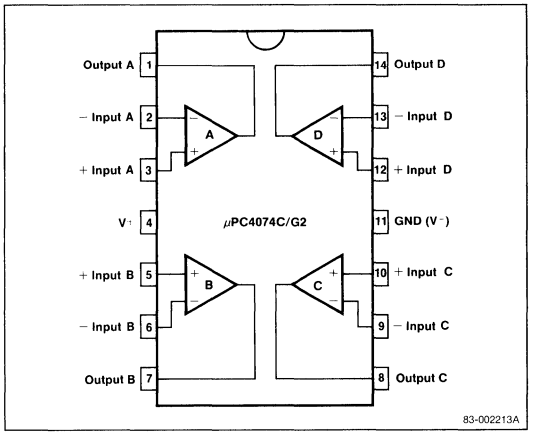
Description

The J-FET input operational amplifiers of the μPC4074 are designed as low-noise versions of the μPC4084. Features of the μPC4074 include improved input equivalent noise voltage, input offset voltage, and input bias current compared to the μPC4084. The μPC4074 is an excellent choice for a wide variety of applications, including audio preamplifier and active filter circuits.

Features

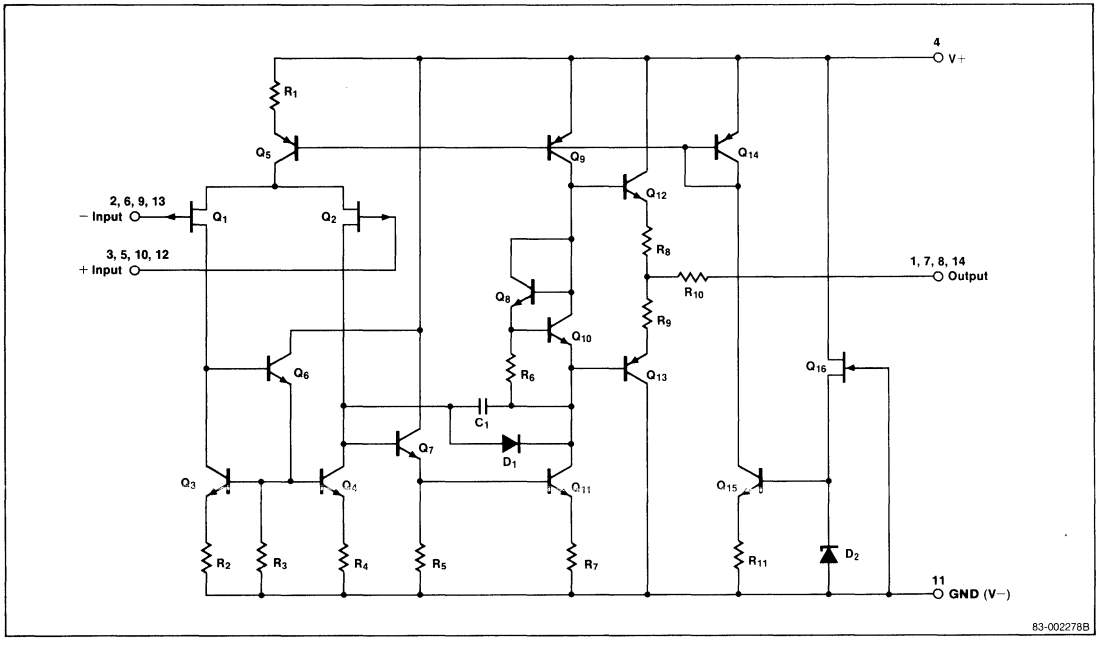
- ☐ Low-noise $e_n = 18\ nV/\sqrt{Hz}$
- ☐ Low-input bias and offset currents
- ☐ Output short-circuit protection
- ☐ High-input impedance: J-FET input stage
- ☐ Internal frequency compensation
- ☐ High slew-rate: 13 V/μs typical
- ☐ Latch-free operation
- ☐ TL074 direct replacement

Pin Configuration



Equivalent Circuit

1/4 Circuit



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Ordering Information

Part Number	Package	Operating Temperature Range
μPC4074C	Plastic DIP	0° to +70°C
μPC4074G2	Plastic Miniflat	0° to +70°C

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Power Dissipation (C Package)	350 mW
Power Dissipation (G2 Package)	440 mW
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	$V^{\pm}$	±5		±16	V	
Capacitive Load ($A_V = +1$)	C_L			100	pF	
Output Current	I_O			10	mA	

Electrical Characteristics

$T_A = 25°C$, $V\pm = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		3	10.0	mV	$R_S \leq 50\ \Omega$
Input Offset Current	I_{io}		5	50	pA	$T_A = 25°C$ (Note 1)
Input Bias Current	I_b		30	200	pA	$T_A = 25°C$ (Note 1)
Large Signal Voltage Gain	A_{VOL}	88	106		dB	$R_L \geq 2\ k\Omega$, $V_O = \pm 10$ V
Supply Current	I_{CC}		8	10	mA	Four amplifiers
Common Mode Rejection Ratio	CMRR	70	86		dB	
Supply Voltage Rejection Ratio	SVRR	70	86		dB	
Output Voltage Swing	V_{OM}	±12	±13.5		V	$R_L \geq 10\ k\Omega$
Output Voltage Swing	V_{OM}	±10	±12		V	$R_L \geq 2\ k\Omega$
Common Mode Input Voltage Range	V_{icm}	±10			V	
Slew Rate	SR		13		V/μs	$A_V = 1$
Input Equivalent Noise Voltage	en		18		$nV/\sqrt{Hz}$	$R_S = 100\ \Omega$, f = 1 kHz
			4		μV_{RMS}	$R_S = 100\ \Omega$, f = 10 Hz to 10 kHz
Unity Gain Bandwidth			3		MHz	
Channel Separation	CS		120		dB	
Over Operating Temperature Range						
Input Offset Voltage	V_{io}			13	mV	$R_S \leq 50\ \Omega$, $T_A = T_{OPT}$
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		10		μV/°C	$T_A = T_{OPT}$
Input Bias Current	I_b			7	nA	$T_A = T_{OPT}$
Input Offset Current	I_{io}			2	nA	$T_A = T_{OPT}$

Note: 1. Input bias currents are temperature sensitive. Short time measuring method is recommended to maintain the junction temperature close to the ambient temperature.

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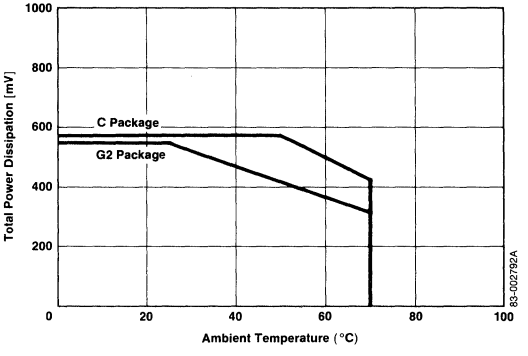
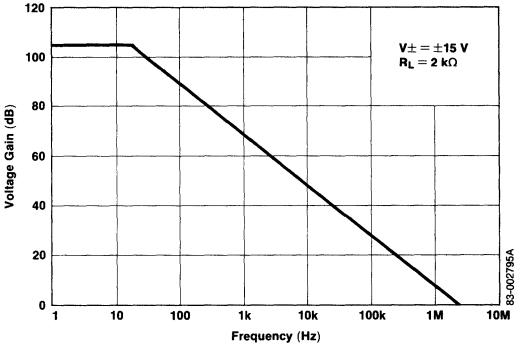
Operating Characteristics

$T_A = 25°C$

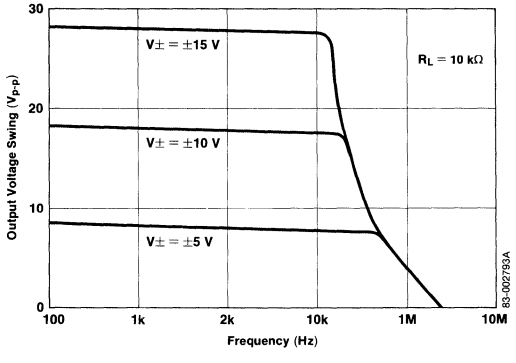
Power Dissipation



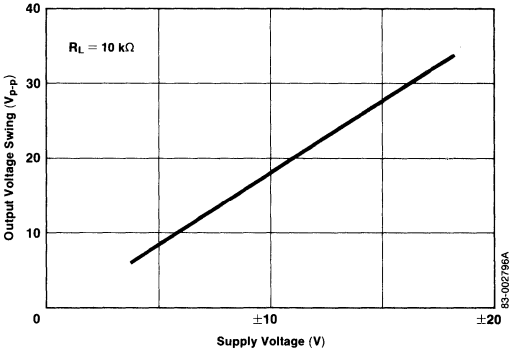
Open Loop Frequency Response



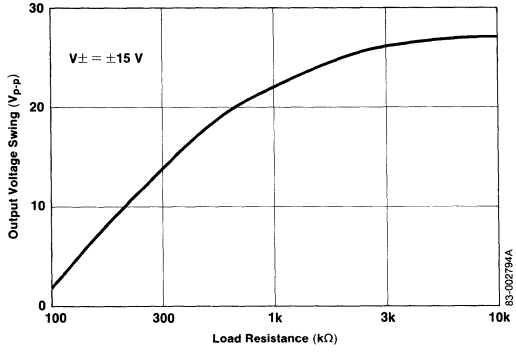
Large Signal Frequency Response



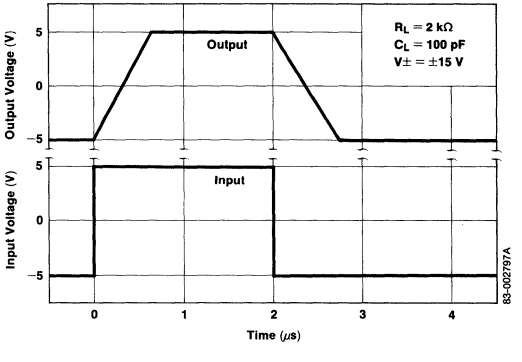
Output Voltage Swing



Output Voltage Swing



Voltage Follower Pulse Response



NEC
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μPC4084
QUAD J-FET INPUT OPERATIONAL AMPLIFIER

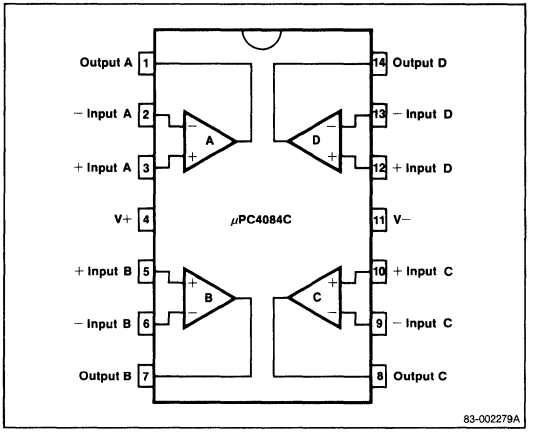
Description

The μPC4084 offers four operational amplifiers with matched ion implanted P-channel J-FET inputs with standard bipolar technology in a single 14 pin DIP. With low input bias current and slew rates ten times that of general purpose amplifiers, this device is ideally suited for pulse amplifiers, active filters and integrator designs.

Features

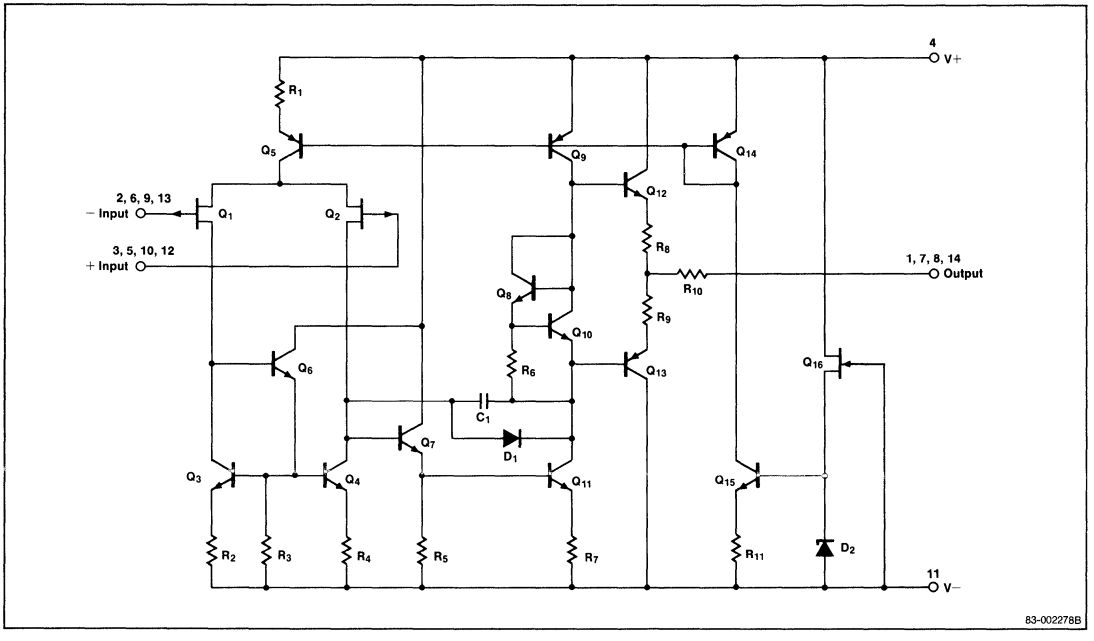
- ☐ Wide common-mode and differential input voltage range
- ☐ Low input bias and offset currents
- ☐ Output short-circuit protection
- ☐ High input impedance: J-FET input stage
- ☐ Internal frequency compensation
- ☐ High slew-rate: 11 V/μs typical
- ☐ Latch-free operation
- ☐ TL084 direct replacement

Pin Configuration



Equivalent Circuit

1/4 Circuit



3

Electrical Characteristics

$T_A = 25°C$, $V^{\pm} = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		5.0	15.0	mV	$R_S \leq 50\Omega$
Input Offset Current	I_{io}		5	200	pA	
Input Bias Current	I_b		30	400	pA	
Large Signal Voltage Gain	A_{VOL}	88	106		dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Supply Current	I_{CC}		8.0	11.2	mA	All amplifiers
Common Mode Rejection Ratio	CMRR	70	76		dB	
Supply Voltage Rejection Ratio	SVRR	70	76		dB	
Output Voltage Swing	V_{OM}	±12	±13.5		V	$R_L \geq 10$ kΩ
Output Voltage Swing	V_{OM}	±10	±12		V	$R_L \geq 2$ kΩ
Common Mode Input Voltage Range	V_{icm}	±10			V	
Slew Rate	SR		11		V/μs	$A_V = 1$
Input Equivalent Noise Voltage	e_n		25		nV/√Hz	f = 1 kHz, $R_S = 100\ \Omega$
Unity Gain Bandwidth	GBW		3		MHz	
Channel Separation	CS		120		dB	
Over Operating Temperature Range						
Input Offset Voltage	V_{io}			20	mV	$R_S \leq 50\ \Omega$, $T_A = T_{OPT}$
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		10		μV/°C	$T_A = T_{OPT}$
Input Bias Current	I_b			10	nA	$T_A = T_{OPT}$
Input Offset Current	I_{io}			5	nA	$T_A = T_{OPT}$

Ordering Information

Part Number	Package	Operating Temperature Range
μPC4084C	Plastic DIP	0°C to +70°C

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V^+ and V^-	36 V
Power Dissipation (Note 1)	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

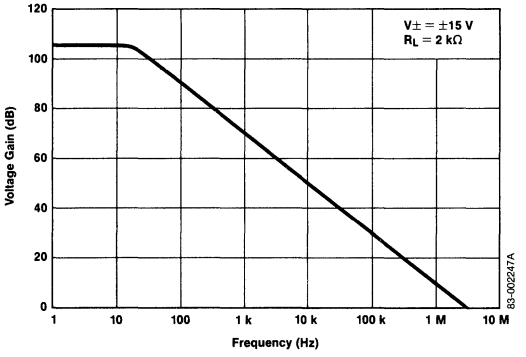
Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

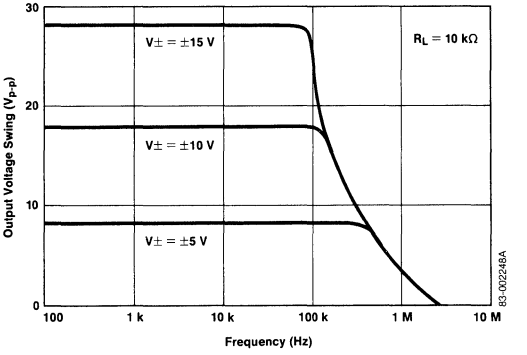
Operating Characteristics

$T_A = 25°C$

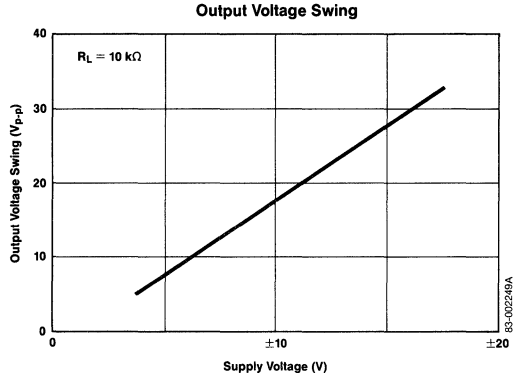
Open Loop Frequency Response



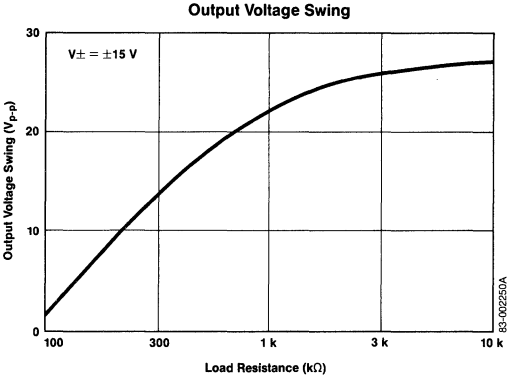
Large Signal Frequency Response



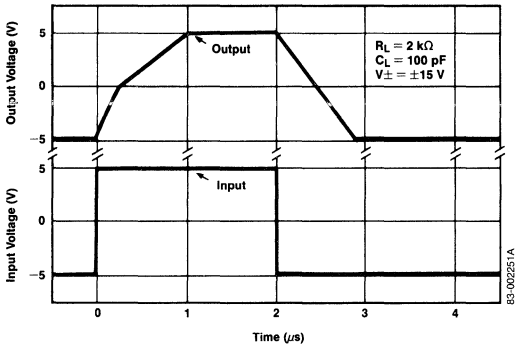
Output Voltage Swing



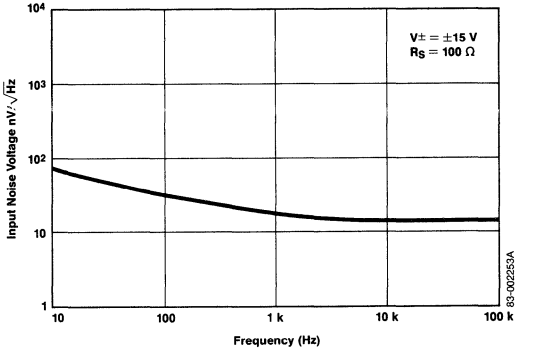
Output Voltage Swing



Voltage Follower Pulse Response



Input Equivalent Noise Voltage

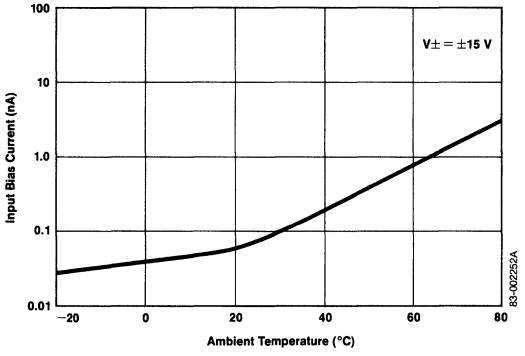


3

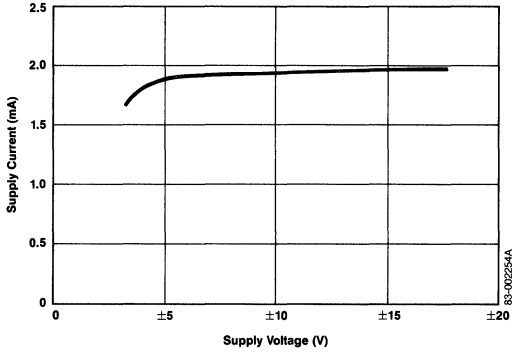
Operating Characteristics (Cont.)

$T_A = 25\,°C$

Input Bias Current



Supply Current



NEC
NEC Electronics Inc.

μPC4574
QUAD ULTRA LOW-NOISE, WIDEBAND, OPERATIONAL AMPLIFIER

Description

The μPC4574 is an ultra low noise, high slew rate quad operational amplifier specifically designed for audio, instrumentation, and communication circuits. The low noise and high frequency capabilities make it ideal for preamps and audio filters for instrumentation and professional audio.

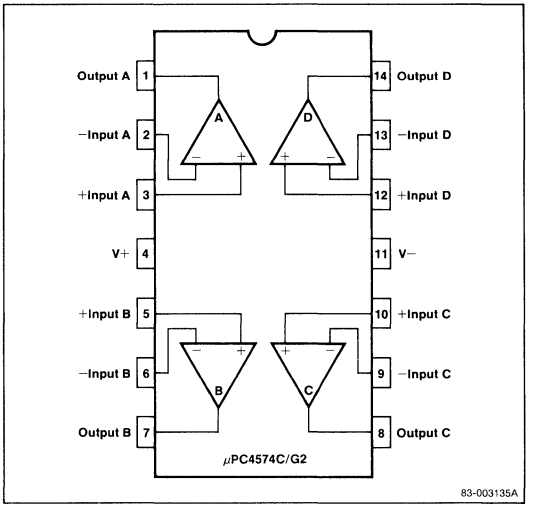
Features

- ☐ Ultra low noise
- ☐ High slew rate
- ☐ Wide bandwidth
- ☐ Internal full frequency compensation
- ☐ Quad equivalent to NE5532

Ordering Information

Part Number	Package	Operating Temperature Range
μPC4574C	14-pin plastic DIP	−20 to +80°C
μPC4574G2	14-pin plastic miniflat	−20 to +80°C

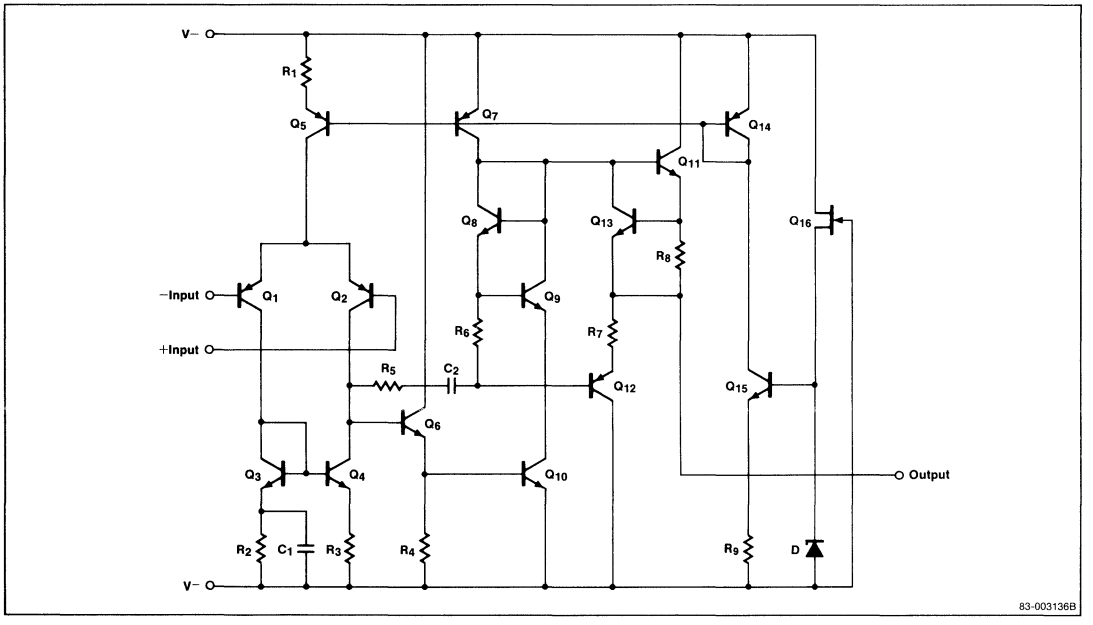
Pin Configuration



83-003135A

Equivalent Circuit

1/4 Circuit



83-003136B

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Power Dissipation, C Package	570 mW
Power Dissipation, G2 Package (Note 1)	550 mW
Differential Input Voltage (Note 2)	±30 V
Output Short Circuit Duration	10 s
Operating Temperature Range	−20 to 80°C
Storage Temperature Range	−55 to +125°C

Note:

1. Derate at 5.5 mW/°C when $T_A > 25°C$.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to supply voltage.

Electrical Characteristics

T_A +25°C, V± = 15 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Offset Voltage	V_{io}		0.3	5	mV	$R_S = 50\ \Omega$
Input Offset Current	I_{io}		10	200	nA	
Input Bias Current	I_b		430	1000	nA	
Large Signal Voltage Gain	A_{VOL}	90	110		dB	R1 = 2k, $V_O = \pm 10$ V
Supply Current	I_{supp}		8.5	12	mA	
Common Mode Rejection Ratio	CMRR	80	100		dB	
Power Supply Rejection Ratio	PSRR	80	100		dB	
Output Voltage Swing	$\pm V_O$	±12	±13.5		V	R1 ≥ 10k
Output Voltage Swing	$\pm V_O$	±10	±12.8		V	R1 ≥ 2k
Common Mode Voltage	V_{cm}	±10	±14		V	

AC and Noise Characteristics

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Slew Rate	SR	4	6		V/μs	R1 = 2k
Gain Bandwidth Product	GBW	10	14		MHz	
Power Bandwidth	PBW	50	70		kHz	V_O = 27 V p-p, THD ≤ 1%
Unity Gain Frequency	f_{unity}		7		MHz	
Phase Margin			50		degrees	
Total Harmonic Distortion	THD		0.002		%	V_O = 3 V rms, 2 to 20 kHz
Channel Separation	CS		120		dB	f = 20 to 20 kHz
Input Noise Voltage	e_n		1.2		μV rms	RIAA + 30 kHz LPF
			0.53	0.65	μV rms	Flat + JISA R_S = 100
Input Noise Voltage Density	e_n		5.0		nV/√Hz	f = 1 Hz
Input Noise Current Density	i_n		0.7		pA/√Hz	f = 1 Hz

NEC
NEC Electronics Inc.

μPC4741
QUAD HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

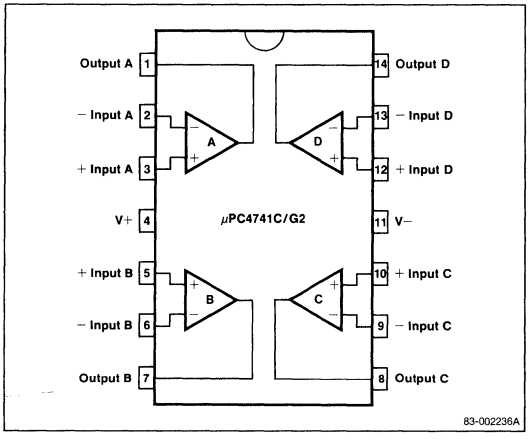
Description

The μPC4741 is a quad operational amplifier designed using four independent internally compensated high-performance 741-type operational amplifiers. The superior AC and DC characteristics of bandwidth, slew-rate, and noise make this device ideal for active filter and audio amplifier applications.

Features

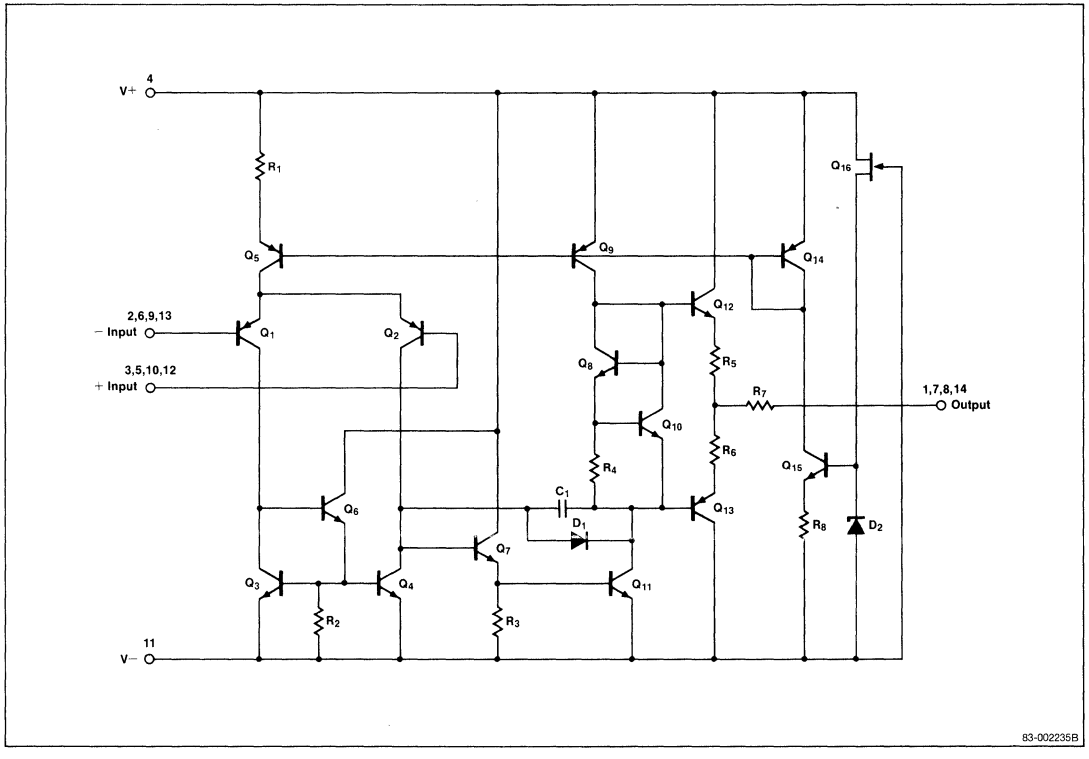
- ☐ Internal frequency compensation
- ☐ Output short-circuit protection
- ☐ Large common mode and differential input voltage range
- ☐ No latch-up
- ☐ No crossover distortion
- ☐ Wide power supply range: ±2 V to ±20 V
- ☐ HA4741 direct replacement

Pin Configuration



Equivalent Circuit

1/4 Circuit



3

Absolute Maximum Ratings

$T_A = 25°C$

Voltage between V+ and V–	40 V
Power Dissipation C Package	570 mW
Power Dissipation G2 Package	550 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Output Short Circuit Duration (Note 2)	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Notes: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Short-circuit to ground on one amplifier only.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ordering Information

Part Number	Package	Operating Temperature Range
μPC4741C	Plastic DIP	0° to 70°C
μPC4741G2	Plastic Miniflat	0° to 70°C

Electrical Characteristics

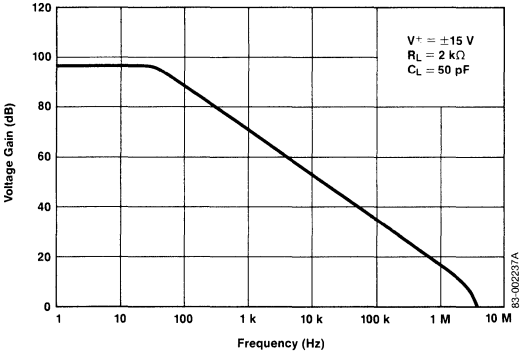
$T_A = 25°$, $V^{\pm} = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		1.0	5.0	mV	$R_S \leq 100\ \Omega$
Input Offset Current	I_{io}		30	50	nA	
Input Bias Current	I_b		100	300	nA	
Large Signal Voltage Gain	A_{VOL}	88	94		dB	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V
Power Consumption	P_D		150	210	mW	
Common Mode Rejection Ratio	CMRR	80	90		dB	
Supply Voltage Rejection Ratio	SVRR		94	100	dB	
Output Voltage Swing	V_{OM}	±12	±13.7		V	$R_L \geq 10$ kΩ
Output Voltage Swing	V_{OM}	±10	±12.5		V	$R_L \geq 2$ kΩ
Common Mode Input Voltage	V_{icm}	±12	±14		V	
Slew Rate	SR		1.6		V/μs	Av = 1
Input Noise Voltage	e_n		9		$nV/\sqrt{Hz}$	f = 1 kHz
Channel Separation	CS		108		dB	f = 10 kHz

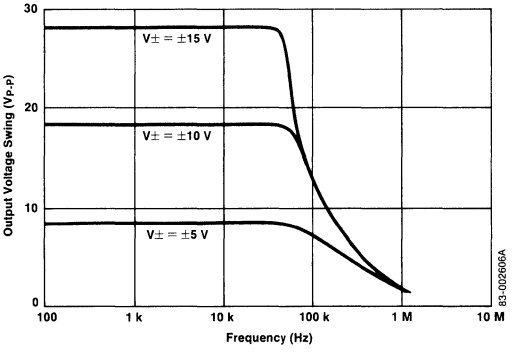
Operating Characteristics

$T_A = 25°C$

Open Loop Frequency Response

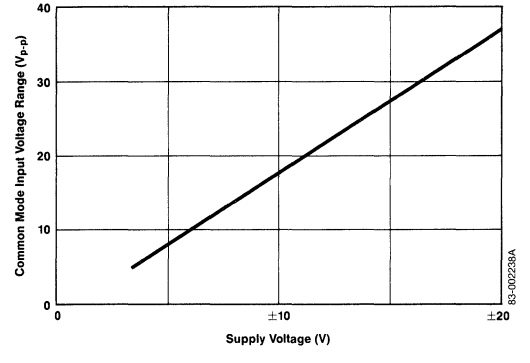


Large Signal Frequency Response

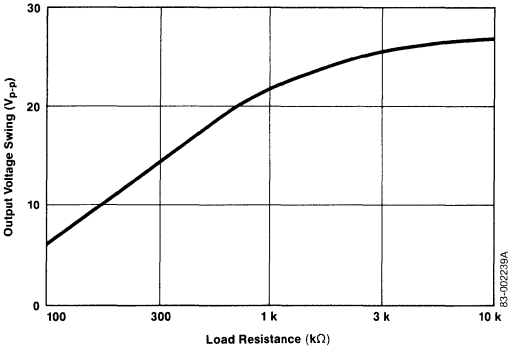


3

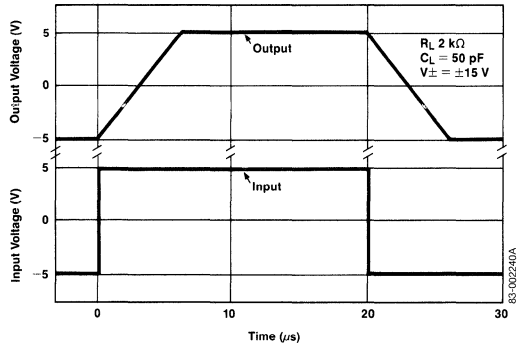
Output Voltage Swing



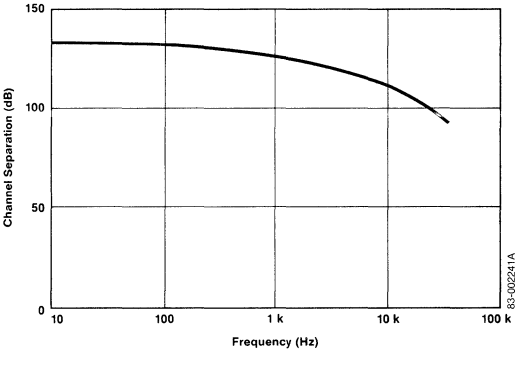
Output Voltage Swing



Pulse Response



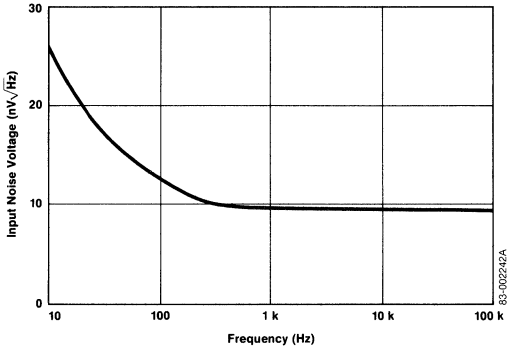
Channel Separation



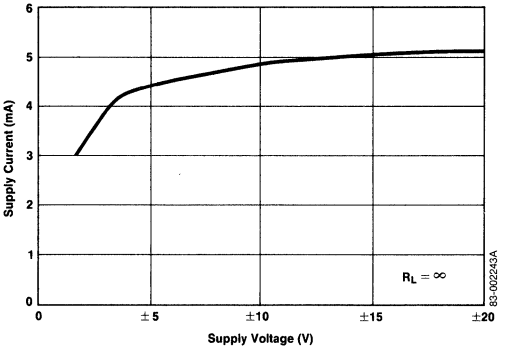
Operating Characteristics (Cont.)

$T_A = 25°C$

Input Noise Voltage Density



Supply Current



Input Offset Voltage: The input voltage required to zero the output with no load.

Input Bias Current: The base current of the input transistors or the gate leakage current of input J-FETS when the output is at zero volts with no load.

Input Offset Current: The difference between the two input bias currents when the output is at zero volts with no load.

Average Input Offset Voltage Drift: The ratio of the change in input offset voltage to the change in temperature.

Average Input Bias Current Drift: The ratio of the change in input bias current to the change in temperature.

Average Input Offset Current Drift: The ratio of the change in input offset current to the change in temperature.

Large Signal Voltage Gain: The ratio of the change in output voltage to the change in input voltage.

Common Mode Rejection Ratio [CMRR]: The ratio of the change in input offset voltage to the change in common mode voltage.

Supply Voltage Rejection Ratio [SVRR]: The ratio of the change in input offset voltage to a change in the supply voltage.

Input Voltage Range: The range of common mode voltage to the input terminals within which the device will operate linearly.

Input Resistance: The ratio in small signal input voltage change to the change in input current at either input terminal with the other input grounded.

Maximum Output Voltage Swing: The peak output voltage obtainable without clipping.

Supply Current: The current consummed by the device with the output at zero.

Input Noise Voltage: The peak to peak noise voltage within a specified frequency band.

Input Noise Voltage Density: The RMS noise voltage in a 1 Hz band surrounding a specified value of frequency.

Input Noise Current: The peak to peak noise current within a specified frequency band.

Input Noise Current Density: The RMS noise voltage in a 1 Hz band surrounding a specified value of frequency.

Slew Rate: The ratio of change in output voltage to the minimum time required to effect the change under large signal drive conditions.

COMPARATORS 4

Section 4 — Comparators

NEC

NEC Electronics Inc.

μPC311
SINGLE PRECISION VOLTAGE COMPARATOR

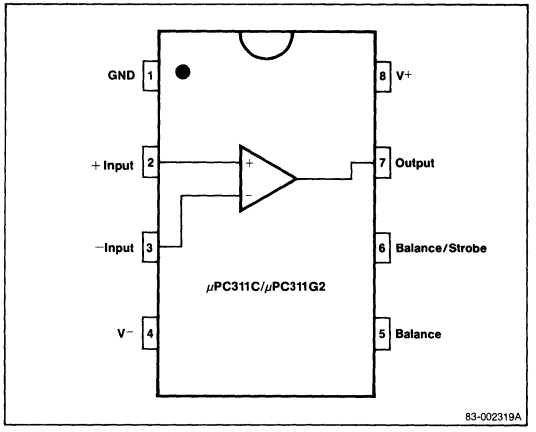
Description

The μPC311 is a single voltage comparator with extremely low input bias currents. This device can be operated with single or split power supplies from +5 V to ±15 V. The output is compatible to DTL, TTL, and CMOS circuits.

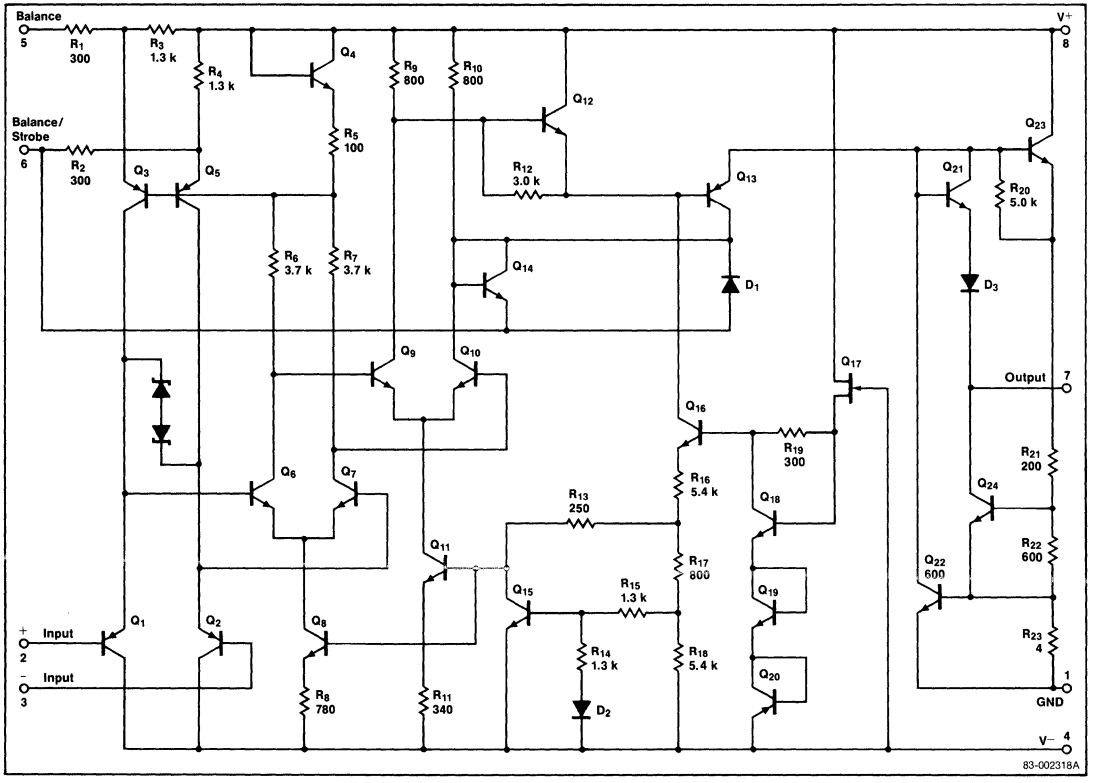
Features

- ☐ Operates from single 5 V supply
- ☐ Maximum input current: 250 nA
- ☐ Maximum offset current: 50 nA
- ☐ Fast transient response: 200 ns
- ☐ LM311 direct replacement

Pin Configuration



Equivalent Circuit



4

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V^+ and V^-	36 V
Output to Negative Supply Voltage	40 V
Ground to Negative Supply Voltage	30 V
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Power Dissipation, C Package	350 mW
Power Dissipation, G2 Package	440 mW
Output Short Circuit Duration	10s
Operating Temperature Range, C or G2 Package	0 to +70° C
Storage Temperature Range, C or G2 Package	−55 to +125° C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ordering Information

Part Number	Package	Operating Temperature Range
μPC311C	Plastic DIP	0°C to +70° C
μPC311G2	Plastic Miniflat	0°C to +70° C

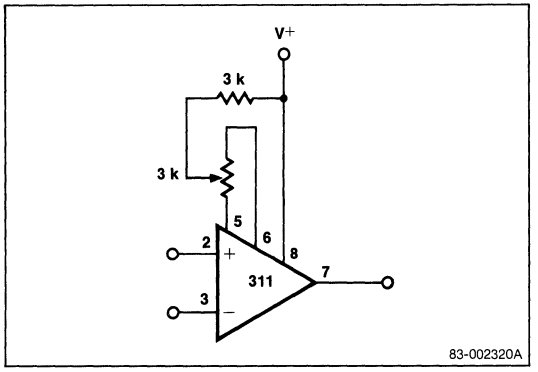
Electrical Characteristics

$T_A = 25°C$, $V\pm = \pm 15$ V

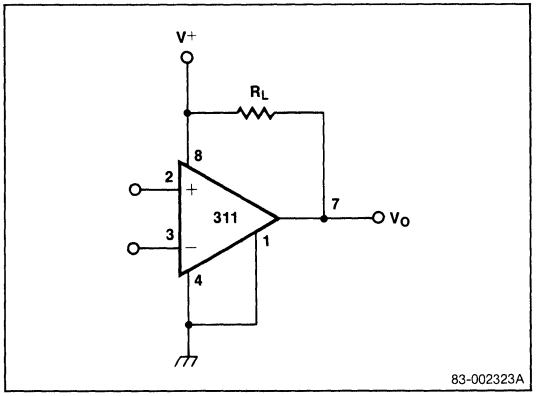
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		2.0	7.5	mV	$V^+ - V^- = 5$ V to 30 V, $R_S \leq 50$ kΩ
Input Offset Current	I_{io}		6.0	50	nA	$V^+ - V^- = 5$ V to 30 V, $R_S \leq 50$ kΩ
Input Bias Current	I_b		100	250	nA	$V^+ - V^- = 5$ V to 30 V, $R_S \leq 50$ kΩ
Voltage Gain	A_{VOL}		106		dB	$R_L = 1.0$ kΩ
Response Time	t_{RSP}		200		ns	Input step 100 mV, overdrive 5 mV
Saturation Voltage	V_{SAT}		0.75	1.5	V	$V_{IN} \geq 10$ mV, $I_O = 50$ mA
Strobe ON Current	$I_{STB\ ON}$		3.0		mA	
Output Leakage Current	I_{OLEAK}		0.2	50	nA	$V_{IN} \geq 10$ mV, $I_O = 35$ mA
Positive Supply Current	$I_{CC}+$		5.1	7.5	mA	
Negative Supply Current	$I_{CC}-$		4.1	5.0	mA	
Input Voltage Range	V_{icm}		±14		V	
Saturation Voltage	V_{SAT}		0.23	0.4	V	$V^+ \geq 4.5$ V, $V^- = 0$ V, $V_{IN} \leq -10$ mV, $I_O = 8$ mA
Over Operating Temperature Range						
Input Offset Voltage	V_{io}			10	mV	$V^+ - V^- = 5$ V to 30 V, $R_S \leq 50$ kΩ, $T_A = 0$ to 70°C
Input Offset Current	I_{io}			70	nA	$V^+ - V^- = 5$ V to 30 V, $R_S \leq 50$ kΩ, $T_A = 0$ to 70°C
Input Bias Current	I_b			300	nA	$V^+ - V^- = 5$ V to 30 V, $R_S \leq 50$ kΩ, $T_A = 0$ to 70°C

Typical Applications

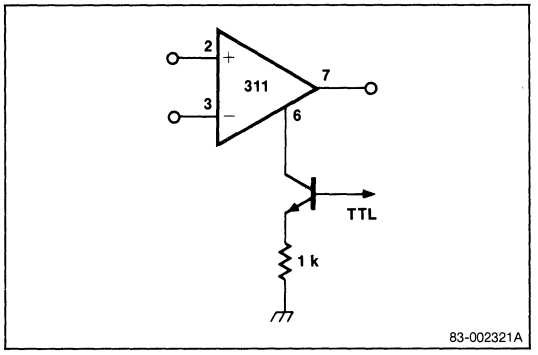
Offset Null



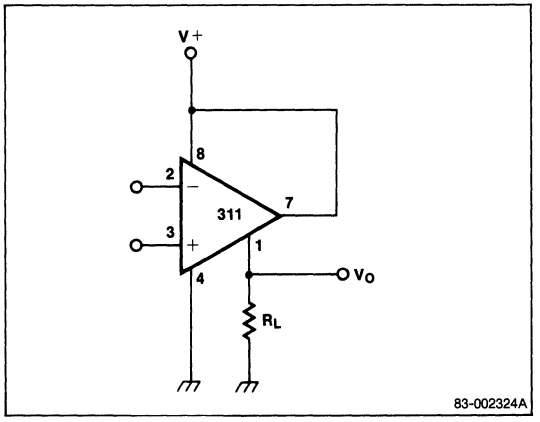
Open Collector Output



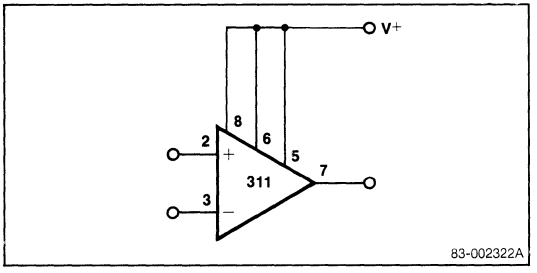
Strobing



Emitter Follower Output



Increasing Input Stage Current



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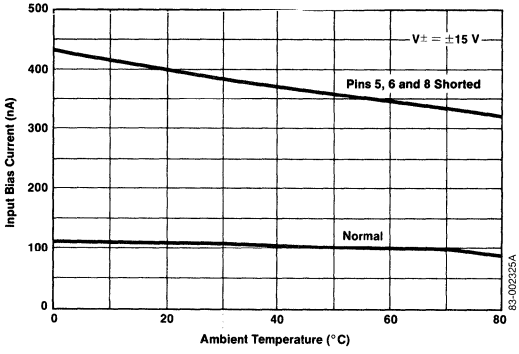
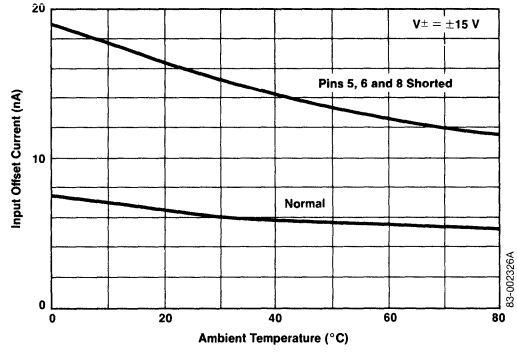
Operating Characteristics

$T_A = 25°C$

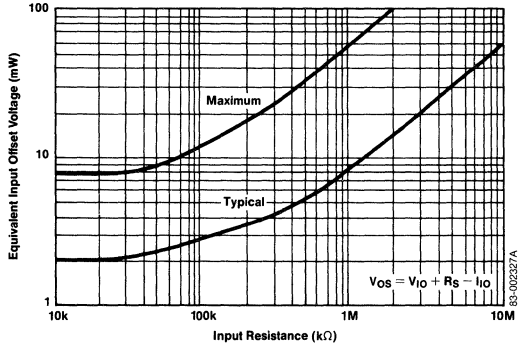
Input Bias Current



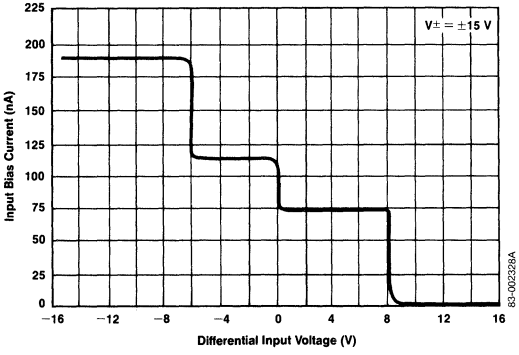
Input Offset Current



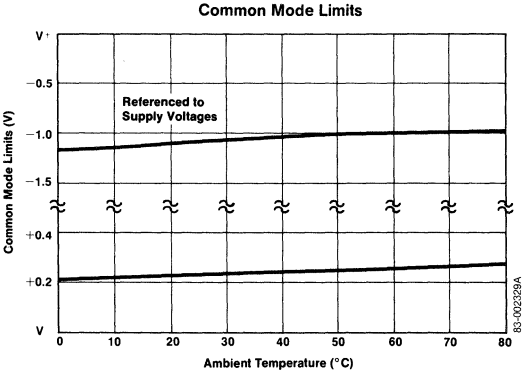
Offset Error



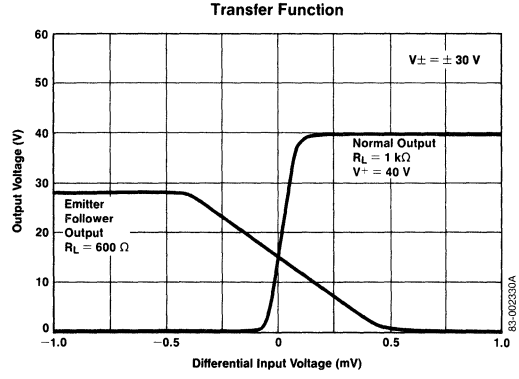
Input Characteristics



Common Mode Limits



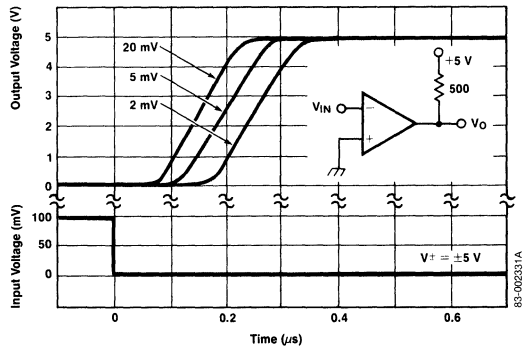
Transfer Function



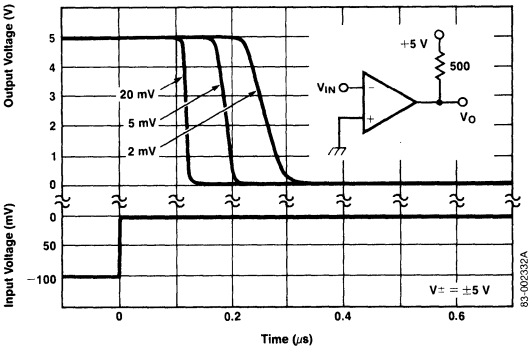
Operating Characteristics (Cont.)

$T_A = 25°C$

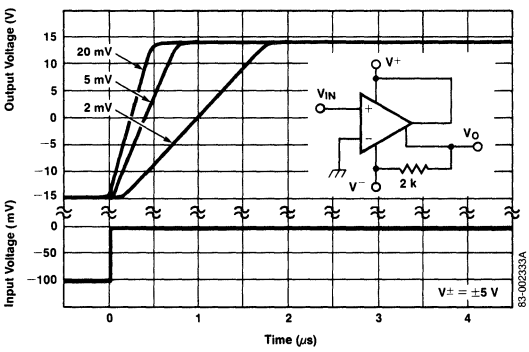
Response Time for Various Input Overdrives



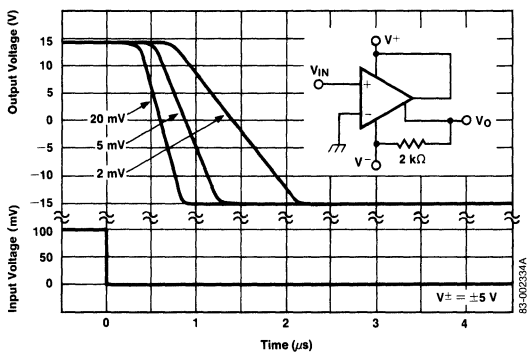
Response Time for Various Input Overdrives



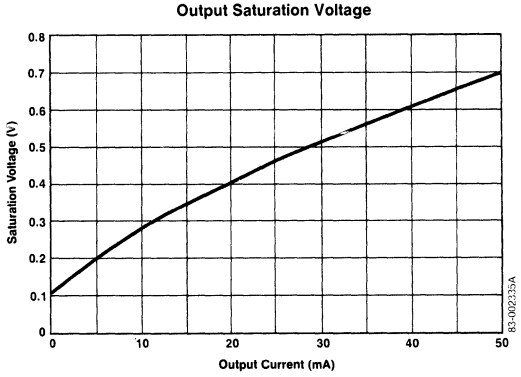
Response Time for Various Input Overdrives



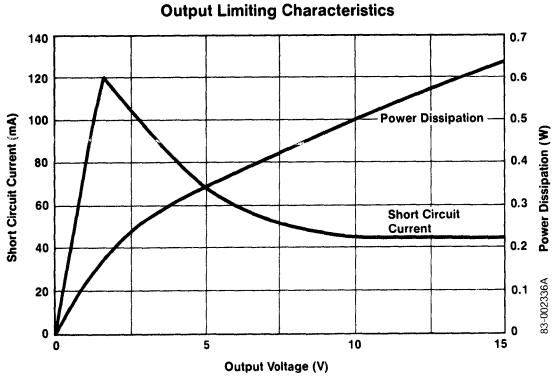
Response Time for Various Input Overdrives



Output Saturation Voltage



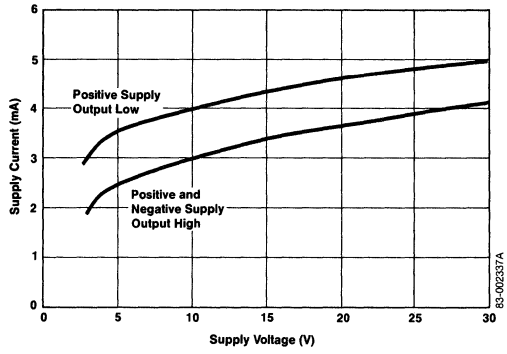
Output Limiting Characteristics



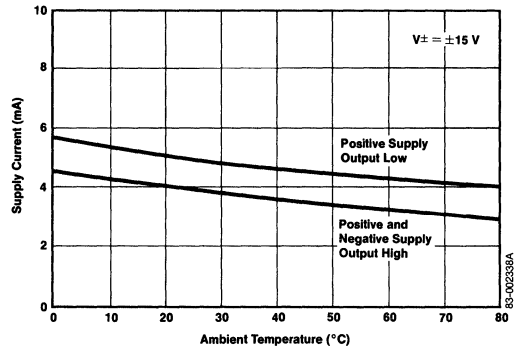
Operating Characteristics (Cont.)

$T_A = 25°C$

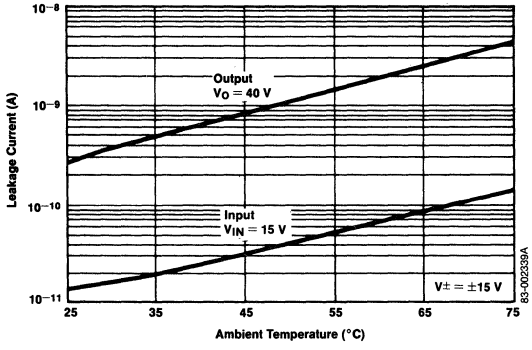
Supply Current



Supply Current



Leakage Currents



μPC319
DUAL HIGH-SPEED VOLTAGE COMPARATOR

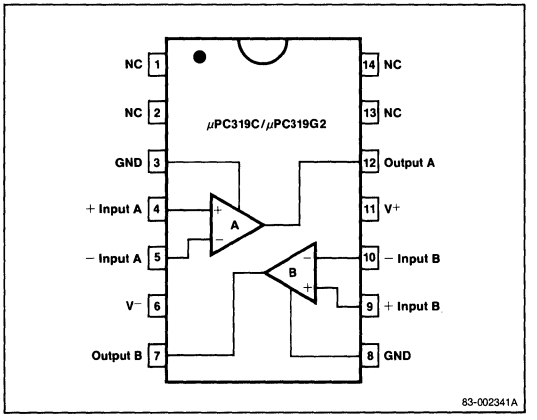
Description

The μPC319 is a precision high-speed comparator designed to operate from single or split power supplies from +5 V to ±15 V. It features excellent input characteristics and drive compatibilities to all popular logic families. The μPC319 is designed for commercial temperature ranges.

Features

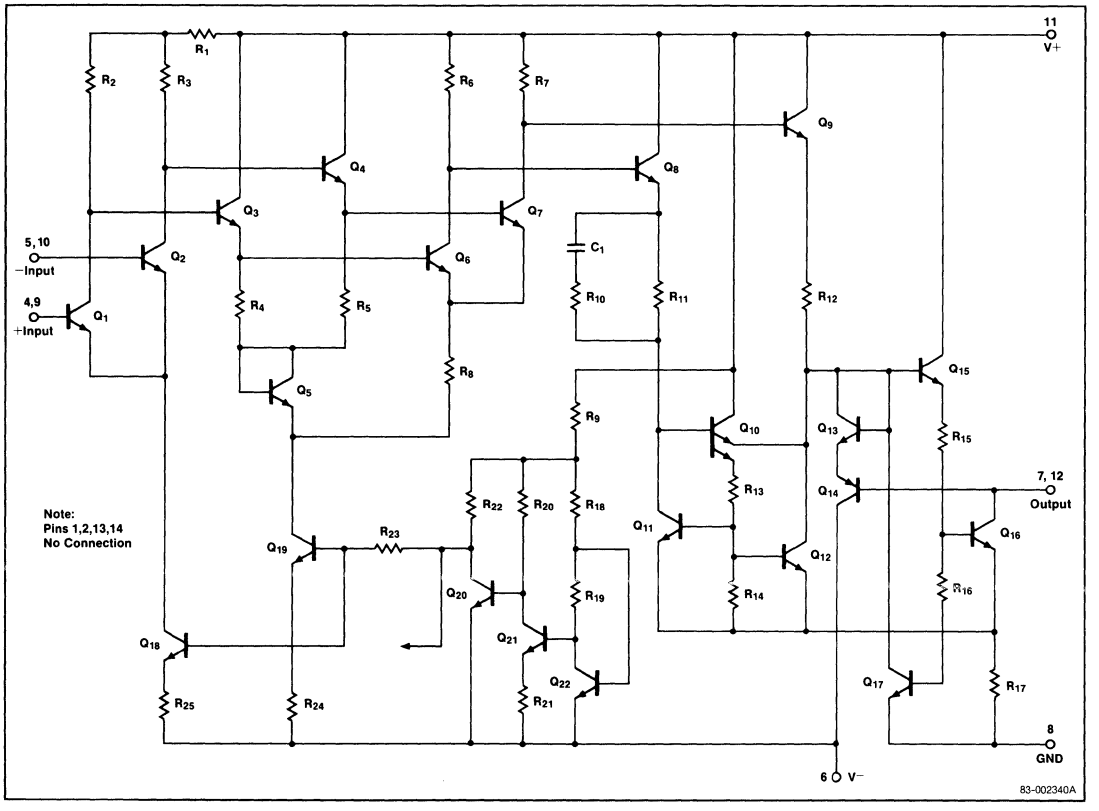
- ☐ Operates from single 5 V supply
- ☐ Typically 80 ns response time at ±15 V
- ☐ Open collector output
- ☐ Minimum fan-out of two each side (TTL)
- ☐ High common mode slew rate
- ☐ LM319 direct replacement

Pin Configuration



Equivalent Circuit

1/2 Circuit



4

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V^+ and V^-	36 V
Output in Negative Supply Voltage	36 V
Ground to Negative Supply Voltage	25 V
Ground to Positive Supply Voltage	18 V
Differential Input Voltage	±5 V
Input Voltage (Note 1)	±15 V
Power Dissipation, C Package	500 mW
Power Dissipation, G2 Package	550 mW
Output Short Circuit Duration	10 s
Operating Temperature Range, C or G2 Package	0 to +70°C
Storage Temperature Range, C or G2 Package	−55 to +125°C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ordering Information

Part Number	Package	Temperature Range
μPC319C	Plastic DIP	0°C to +70°C
μPC319G2	Plastic Miniflat	0°C to +70°C

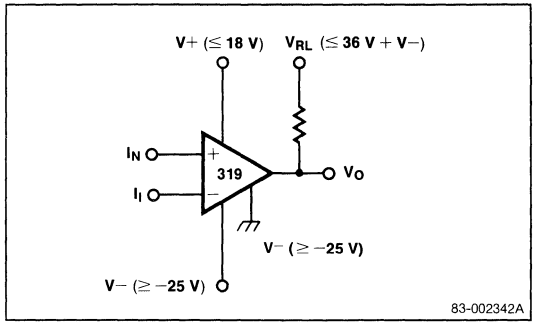
Electrical Characteristics

$T_A = 25°C$, $V\pm = \pm 15$ V

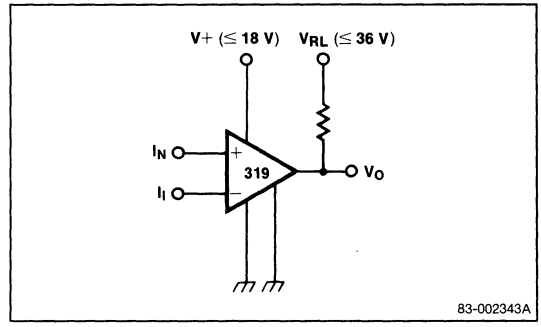
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		2.0	8.0	mV	$V\pm = \pm 5$ V to ±15 V, $R_S \leq 50\Omega$
Input Offset Current	I_{io}		80	200	nA	
Input Bias Current	I_b		400	1000	nA	
Voltage Gain	A_{VOL}	78	92		dB	
Response Time	t_{RSP}		80		ns	Input 100 mV, overdrive 5 mV
Saturation Voltage	V_{SAT}		0.75	1.5	V	$V_I \leq -10$ mV, $I_O = 25$ mA
Output Leakage Current	I_{OLEAK}		0.2	10	μA	$V_I \geq 10$ mV, $I_O = 35$ mA
Positive Supply Current	I_{CC+}		4.3		mA	$V^+ = +5$ V, $V^- = 0$ V
Positive Supply Current	I_{CC+}		8.0	12.5	mA	$V\pm = \pm 15$ V
Positive Supply Current	I_{CC+}		3.0	5.0	mA	$V\pm = \pm 5$ V
Input Voltage Range	V_{icm}		±13		V	$V\pm = \pm 15$ V
Saturation Voltage	V_{SAT}		0.23	0.4	V	$V^+ \geq 4.5$ V, $V^- = 0$ V, $V_I \leq -10$ mV, $I_O = 3.2$ mA
Over Operating Temperature Range						
Input Offset Voltage	V_{io}			10	mV	$V\pm = \pm 5$ V to ±15 V, $R_S \leq 5$ kΩ, $T_A = 0$ to +70°C
Input Offset Current	I_{io}			300	nA	$V\pm = \pm 5$ V to ±15 V, $R_S \leq 5$ kΩ, $T_A = 0$ to +70°C
Input Bias Current	I_b			1200	nA	$V\pm = \pm 5$ V to ±15 V, $R_S \leq 5$ kΩ, $T_A = 0$ to +70°C

Typical Applications

Split Supplies



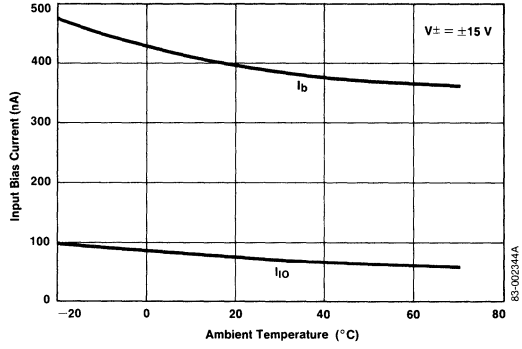
Single Supply



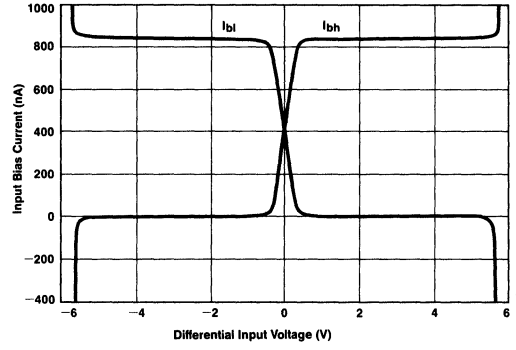
Operating Characteristics

$T_A = 25\,°C$

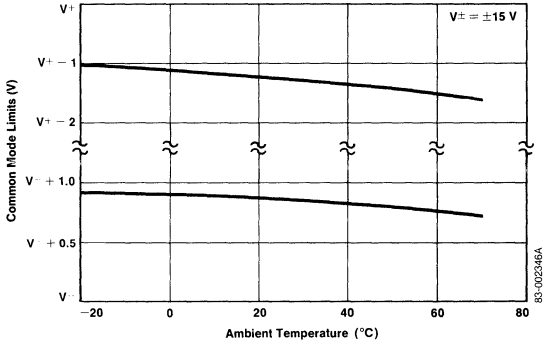
Input Currents



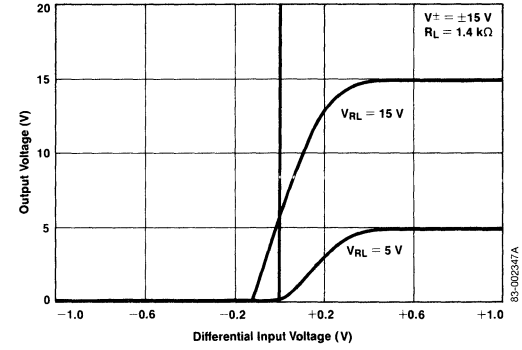
Input Characteristics



Common Mode Limits



Transfer Function

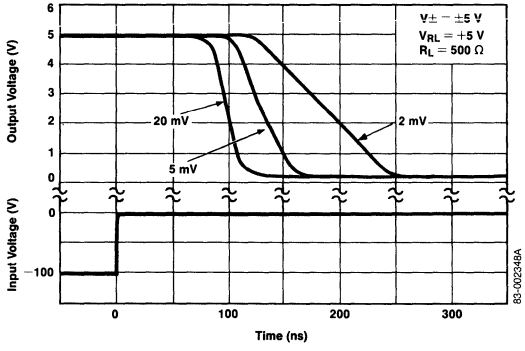


4

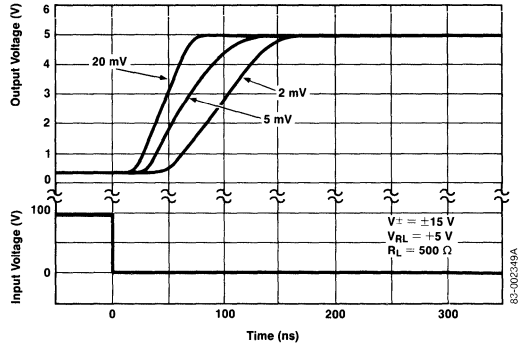
Operating Characteristics (Cont.)

$T_A = 25°C$

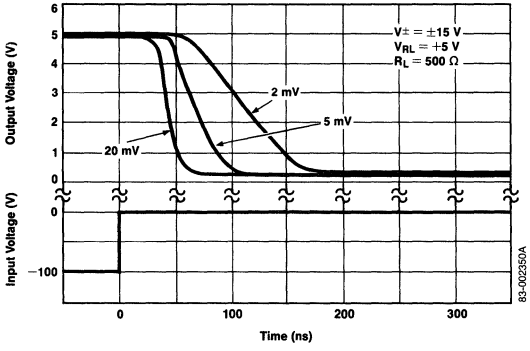
Response Time for Various Input Overdrives



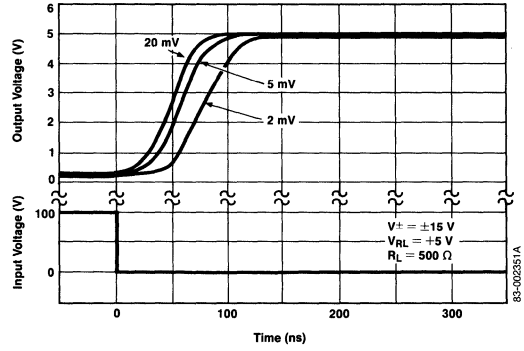
Response Time for Various Input Overdrives



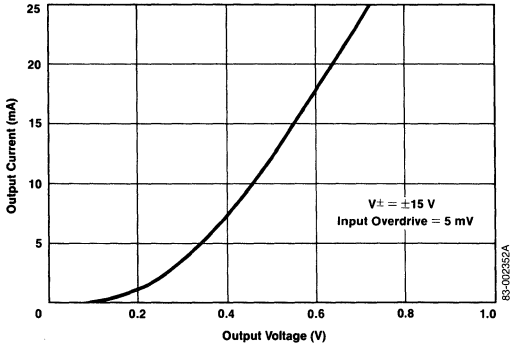
Response Time for Various Input Overdrives



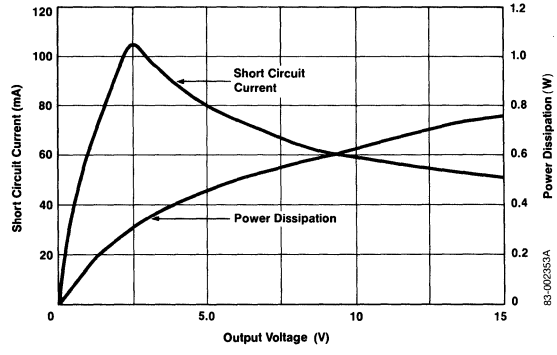
Response Time for Various Input Overdrives



Output Saturation Voltage



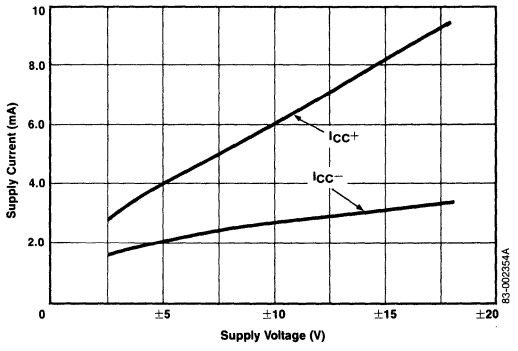
Output Limiting Characteristics



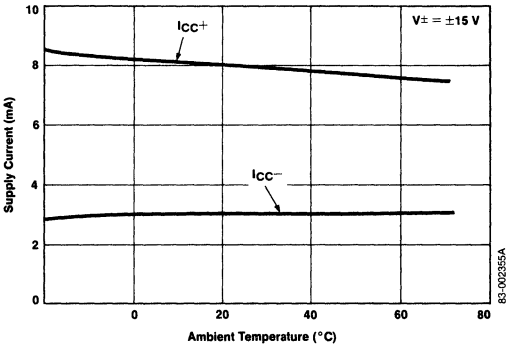
Operating Characteristics (Cont.)

$T_A = 25°C$

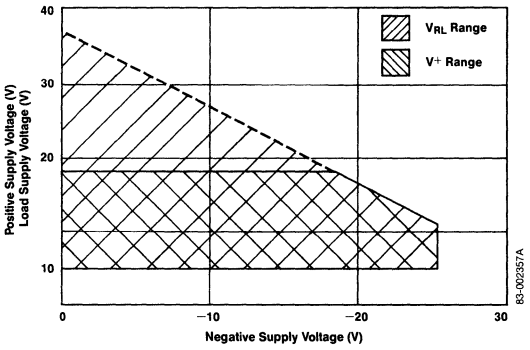
Supply Current



Supply Current



Supply Voltage Range



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μPC339
QUAD LOW-POWER VOLTAGE COMPARATOR

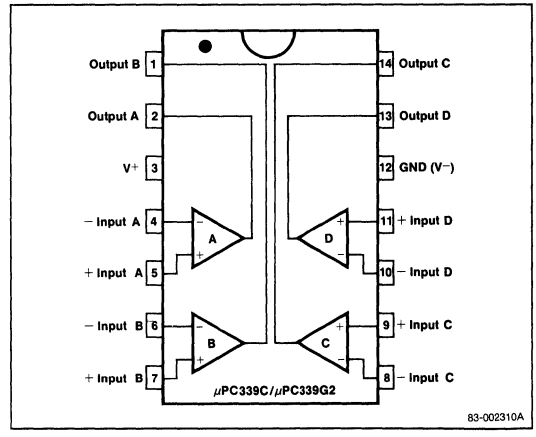
Description

The μPC339 is a quad comparator designed to operate from a single or split power supply over a wide range of voltages, with very low current consumption. Even when operating from a single power supply the input common mode voltage includes ground.

Features

- ☐ Input common-mode voltage range includes ground
- ☐ Wide power supply range:
  - Single supply 2 V to 36 V DC
  - Dual supplies ±1 V to ±18 V DC
- ☐ Low power consumption
- ☐ Compatible with all forms of logic
- ☐ Open collector output
- ☐ LM339 direct replacement

Pin Configuration

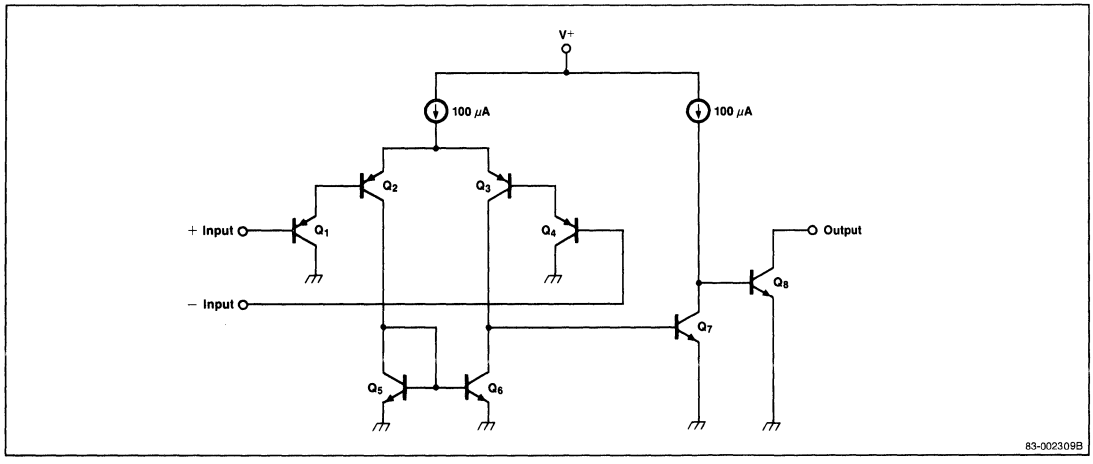


Ordering Information

Part Number	Package	Operating Temperature Range
μPC339C	Plastic DIP	0°C to +70°C
μPC339G2	Plastic Miniflat	0°C to +70°C

Equivalent Circuit

1/4 Circuit



Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	36 V
Differential Input Voltage	36 V
Common Mode Input Voltage	−0.3 to +36 V
Power Dissipation, C Package	570 mW
Power Dissipation, G2 Package	550 mW
Output Short Circuit to Ground	Indefinite
Operating Temperature Range, C or G2 Package	0 to +70°C
Storage Temperature Range, C or G2 Package	−55 to +125°C

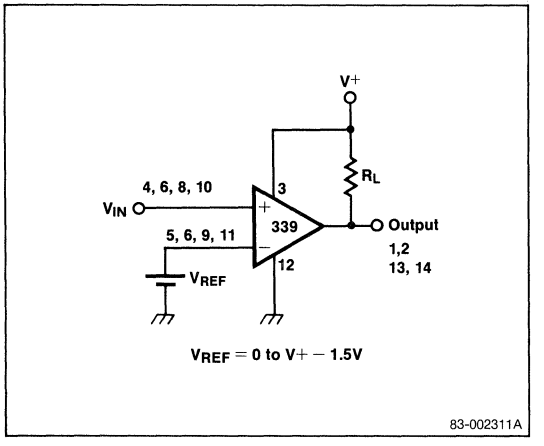
Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

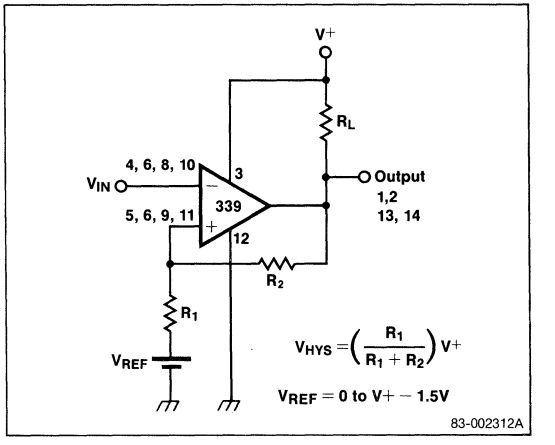
Electrical Characteristics

$T_A = 25°C$, $V+ = 5$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		2	5	mV	$V_O = 1.4$ V, $V_{REF} = 1.4$ V, $R_S = 0\ \Omega$
Input Bias Current	I_b		25	250	nA	$V_O \approx 1.4$ V
Input Offset Current	I_{io}		5	50	nA	$V_O \approx 1.4$ V
Common Mode Input Voltage Range	V_{icm}	0		V+ − 1.5	V	
Supply Current	I_{CC}		0.8	2	mA	$R_L = \infty$
Voltage Gain	A_{VOL}		106		dB	$R_L = 15$ kΩ
Large Signal Response Time	t_{RSP}		1.3		μs	R_L 5.1 kΩ, $V_{RL} = 5$ V
Output Sink Current	I_{OSINK}	6	16		mA	$V_{IN}(-) = 1$ V, $V_{IN}(+) = 0$ V, $V_O \leq 1.5$ V
Saturation Voltage	V_{SAT}		0.2	0.4	V	$V_{IN}(-) = 1$ V, $V_{IN}(+) = 0$ V, $I_{OSINK} = 3$ mA
Output Leakage Current	I_{OLEAK}		0.1		nA	$V_{IN}(+) = 1$ V, $V_{IN}(-) = 0$ V, $V_O = 5$ V

Typical Applications

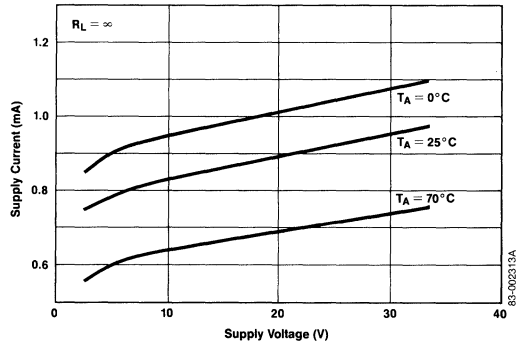




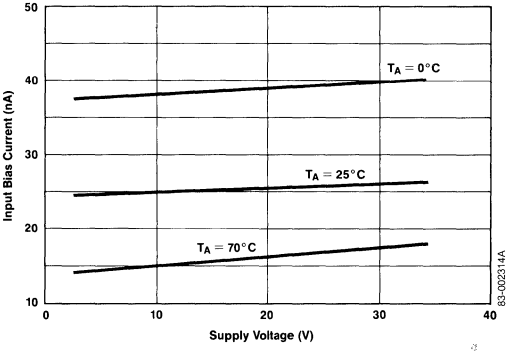
Operating Characteristics

$T_A = 25°C$

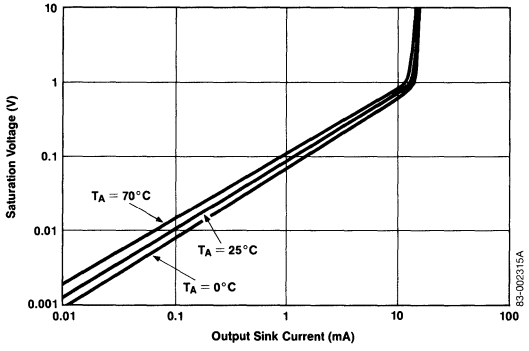
Supply Current



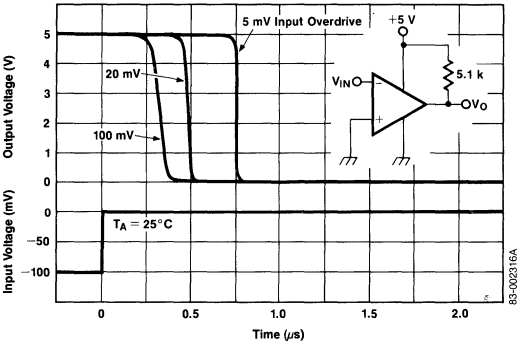
Input Bias Current



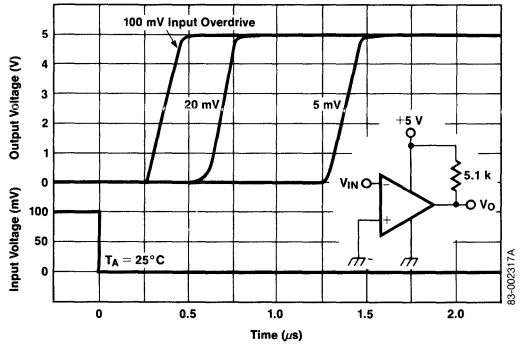
Output Saturation Voltage



Response Time for Various Input Overdrives



Response Time for Various Input Overdrives



4

μPC393
DUAL LOW-POWER VOLTAGE COMPARATOR

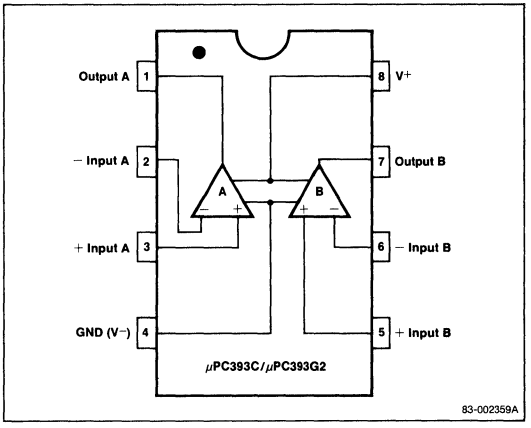
Description

The μPC393 is a dual comparator designed to operate from either single or split power supplies from + 2 V to ±18 V. It features low power supply current drain and input common mode voltage which includes ground, even when operated from a single supply. The μPC393 is designed for Commercial temperature ranges.

Features

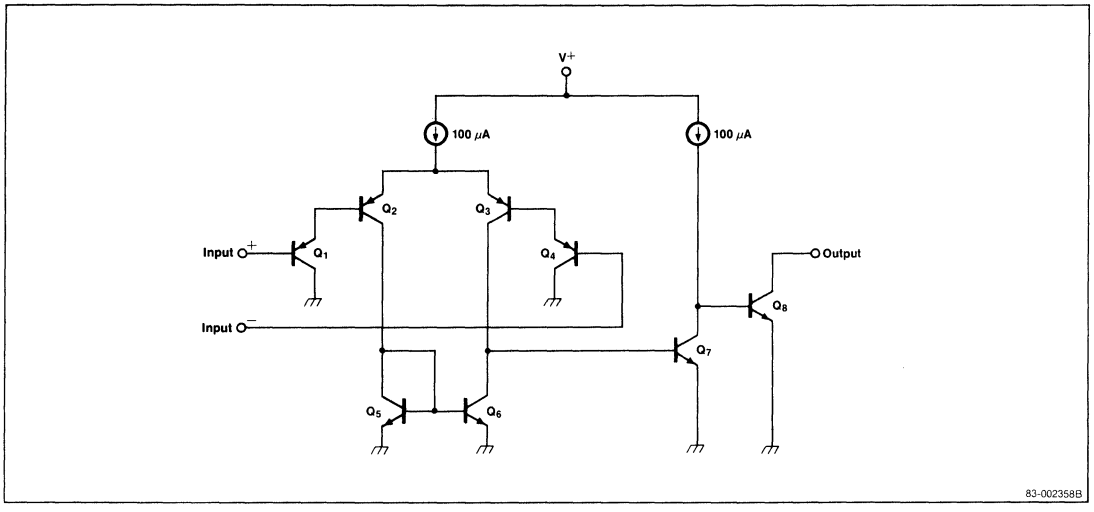
- ☐ Input common-mode voltage range includes ground
- ☐ Wide power supply range:
  - Single supply 2 V to 36 V DC
  - Dual supplies ±1 V to ±18 V DC
- ☐ Low power consumption
- ☐ Compatible with all forms of logic
- ☐ Open collector output
- ☐ LM393 direct replacement

Pin Configuration



Equivalent Circuit

1/2 Circuit



4

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V^+ and V^-	36 V
Differential Input Voltage	36 V
Common Mode Input Voltage	−0.3 to +36 V
Power Dissipation, C Package	350 mW
Power Dissipation, G2 Package	440 mW
Output Short Circuit to Ground	Indefinite
Operating Temperature Range, C or G2 Package	0 to +70°C
Storage Temperature Range, C or G2 Package	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ordering Information

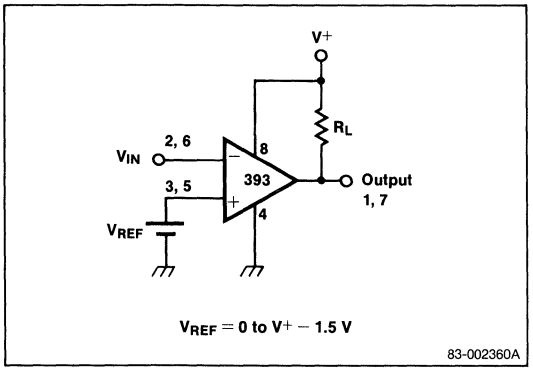
Part Number	Package	Operating Temperature Range
μPC393C	Plastic DIP	0°C to +70°C
μPC393G2	Plastic Miniflat	0°C to +70°C

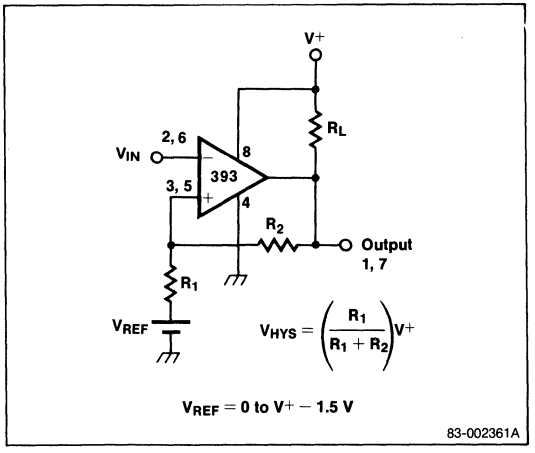
Electrical Characteristics

$T_A = 25°C$, $V^+ = 5$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}		2	5	mV	$V_O = 1.4$ V, $V_{REF} = 1.4$ V, $R_S = 0\Omega$
Input Bias Current	I_b		25	250	nA	$V_O = 1.4$ V
Input Offset Current	I_{io}		5	50	nA	$V_O = 1.4$ V
Common Mode Input Voltage Range	V_{icm}	0				
Supply Current	I_{CC}		0.6	1	mA	$R_L = \infty$
Voltage Gain	A_{VOL}		106		dB	$R_L = 15$ kΩ
Large Signal Response Time	t_{RLS}		1.3		μs	R_L 5.1 kΩ, $V_{RL} = 5$ V
Output Sink Current	I_{OSINK}	6	16		mA	− INPUT = 1 V, + INPUT = 0 V, $V_O \leq 1.5$ V
Saturation Voltage	V_{SAT}		0.2	0.4	V	− INPUT = 1 V, + INPUT = 0 V, $I_{OSINK} = 3$ mA
Output Leakage Current	I_{OLEAK}		0.1		nA	+ INPUT = 1 V, − INPUT = 0 V, $V_O \leq 5$ V

Typical Applications

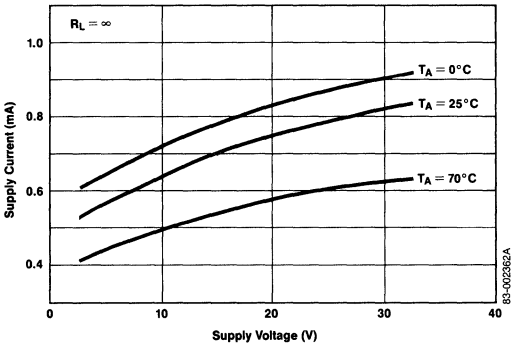




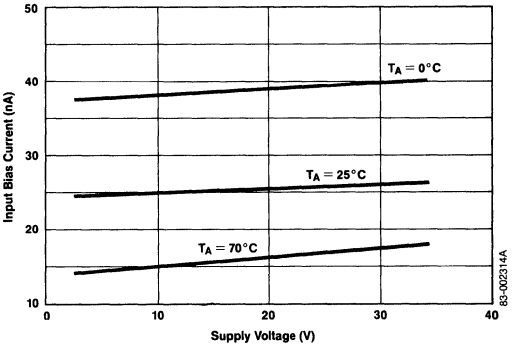
Operating Characteristics

$T_A = 25°C$

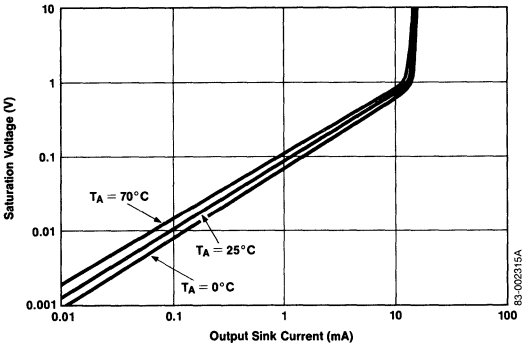
Supply Current



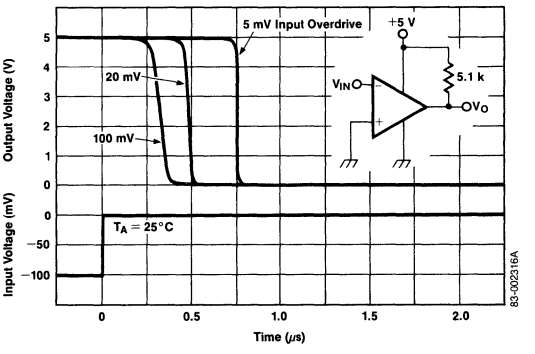
Input Bias Current



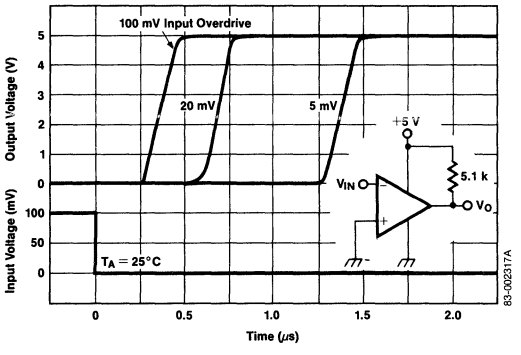
Output Saturation Voltage



Response Time for Various Input Overdrives



Response Time for Various Input Overdrives



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Input Offset Voltage: The voltage between the input terminals when the output is within a specified voltage range.

Input Bias Current: The bias current of the input transistors.

Input Offset Current: The difference in current in the two input terminals when the output is at a specified voltage.

Voltage Gain: The ratio of the change in output voltage to the change in input voltage.

Common Mode Rejection Ratio [CMRR]: The ratio of the input voltage range to the maximum change in input voltage over this range.

Supply Voltage Rejection Ratio [SVRR]: The ratio of change in input offset voltage to the change in supply voltage.

Input Voltage Range: The range of common mode voltage at the input terminals within which operating specifications are assured.

Output Leakage Current: The current into the output terminal, at a given output voltage and input drive, equal to or greater than a specified value.

Output Sink Current: The maximun negative current that can be output by the comparator.

Saturation Voltage: The low output voltage level at a specified current "sink" level.

Overdrive: The input step voltage required, at some predetermined input level, to change the output state to high or low from its initial state.

NEC

VOLTAGE REGULATORS

5

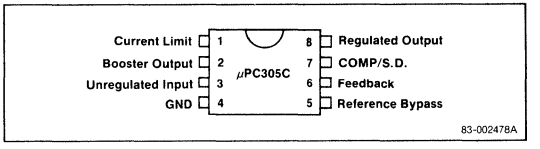
Section 5 — Voltage Regulators

μPC305
PRECISION POSITIVE VOLTAGE REGULATOR

Description

The μPC305 is a precision adjustable voltage regulator designed for a wide range of applications including digital and analog circuits. This device features fast response to both line and load transients, low standby power dissipation, and freedom from oscillation with variation in resistive or inductive loading. This device is ideal for use in general purpose power supply circuits.

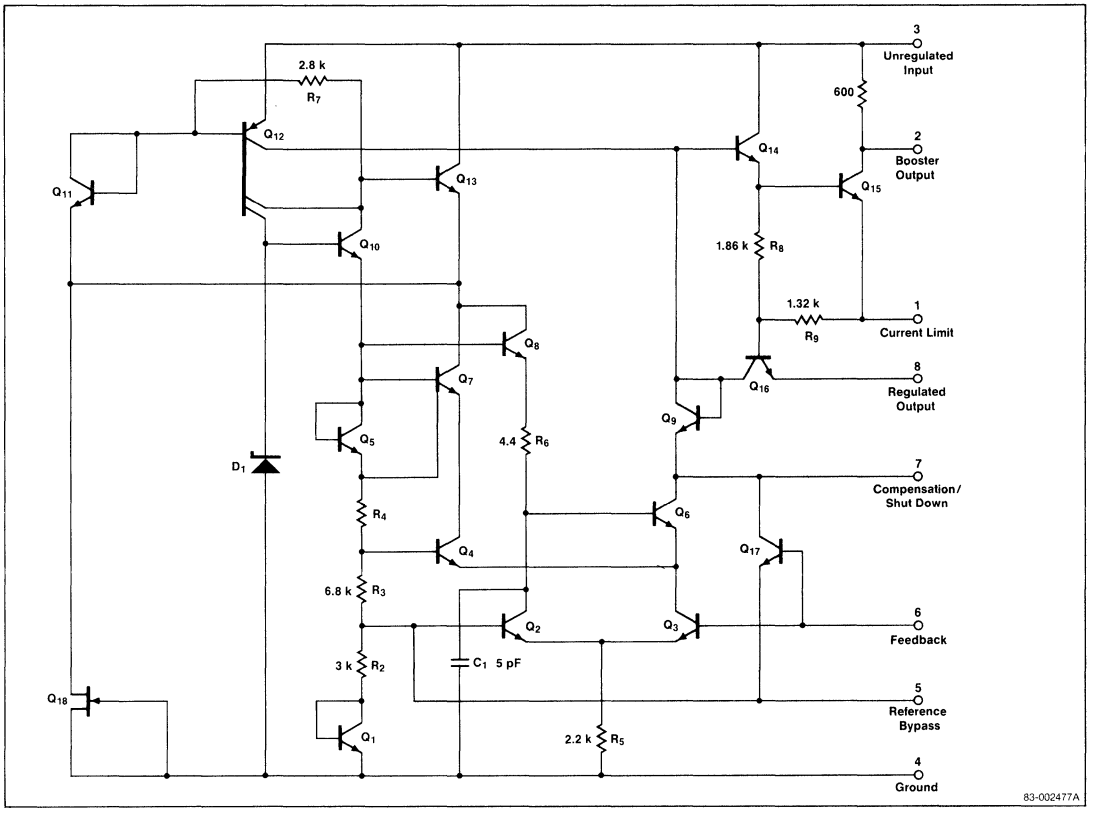
Pin Configuration



Features

- ☐ Output voltage adjustable from 4.5 V to 30 V
- ☐ Output currents in excess of 10 A possible by adding external transistors
- ☐ Load regulation better than 0.1% full load with current limiting
- ☐ DC line regulation guaranteed at 0.03%/V
- ☐ LM305 direct replacement

Equivalent Circuit



Absolute Maximum Ratings

$T_A = 25°C$

Input Voltage	40 V
Input Output Voltage Differential	40 V
Peak Output Current	50 mA
Power Dissipation	350 mW
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ordering Information

Part Number	Package	Operating Temperature Range
μPC305C	Plastic DIP	0 to +70°C

Electrical Characteristics

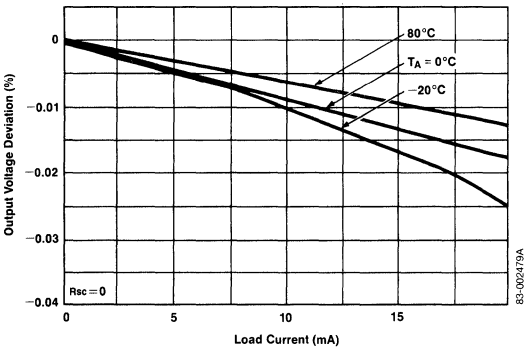
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage Range	V_{IN}	8.0		40	V	
Output Voltage Range	V_O	4.5		30	V	
Input Output Voltage Differential		3.0		30	V	
Load Regulation	REG_L		0.02	0.05	%	$0 \leq I_O \leq 12$ mA, $R_{SC} = 18\ \Omega$
Line Regulation	REG_{IN}		0.025	0.06	%/V	$V_{IN} - V_O \leq 5$ V
			0.015	0.03	%/V	$V_{IN} - V_O > 5$ V
Ripple Rejection			0.003		%/V	$C_{REF} = 10\ \mu F$, f = 120 Hz
Temperature Stability			0.3	1.0	%	$0°C \leq T_A \leq 70°C$
Feedback sense voltage		1.65	1.8	1.90	V	
Standby Current Drain			0.005		%	10 Hz ≤ f ≤ 10 kHz, $C_{REF} = 0$
			0.002		%	$C_{REF} = 0.1\ \mu F$
Long Term Stability			0.1		%	
Standby Current Drain			1.0	2.0	mA	$V_{IN} = 40$ V

C_{REF}: Bypass capacitor of pin 5.
R_{SC}: Output current sense resistor.

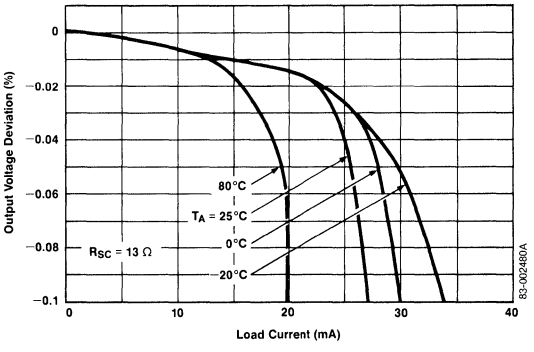
Operating Characteristics

$T_A = 25\,°C$

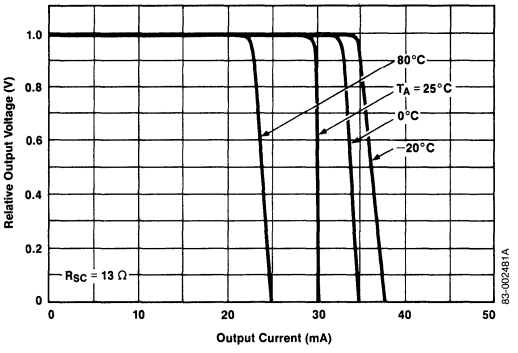
Load Regulation



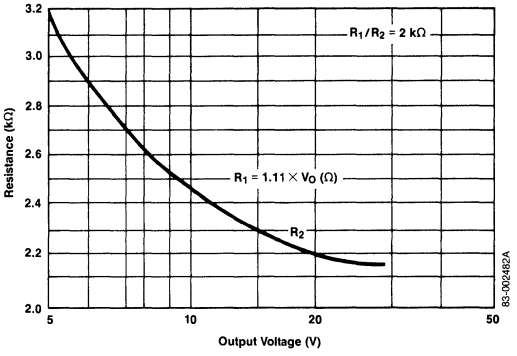
Load Regulation



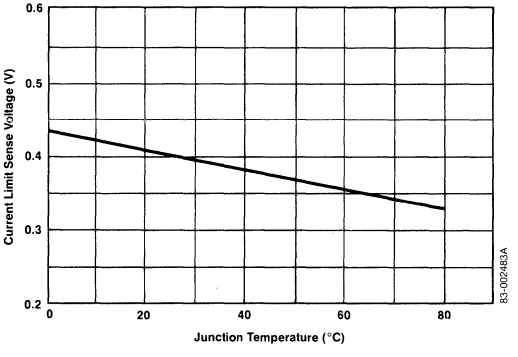
Current Limiting Characteristic



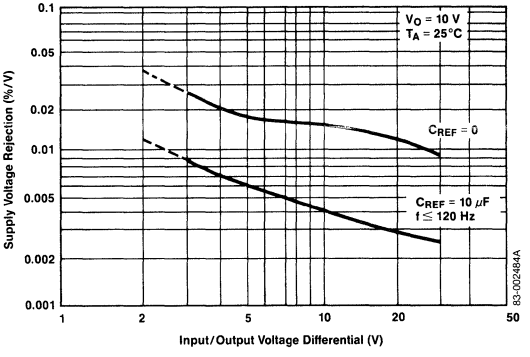
Optimum Divider Resistance Values



Current Limit, Sense Voltage



Supply Voltage Rejection

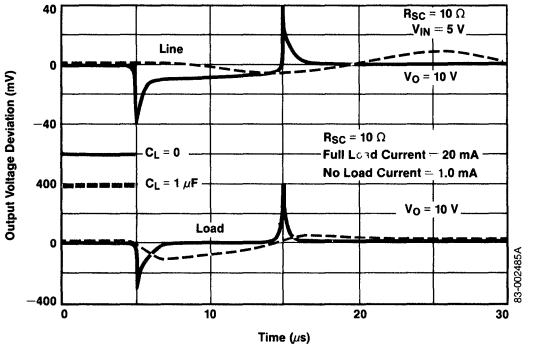


5

Operating Characteristics (Cont)

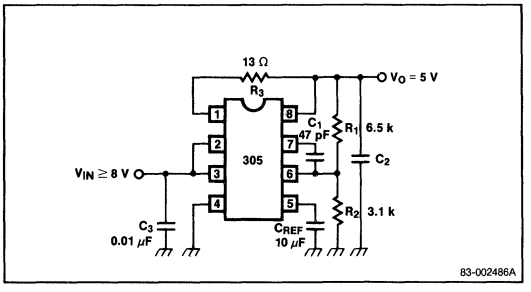
$T_A = 25°C$

Transient Response

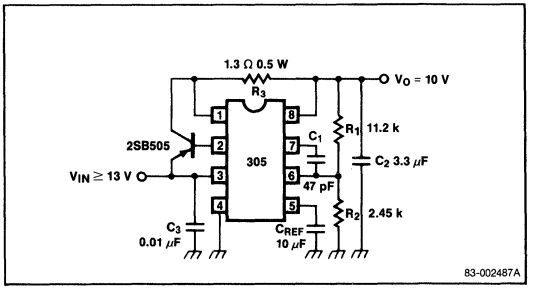


Applications

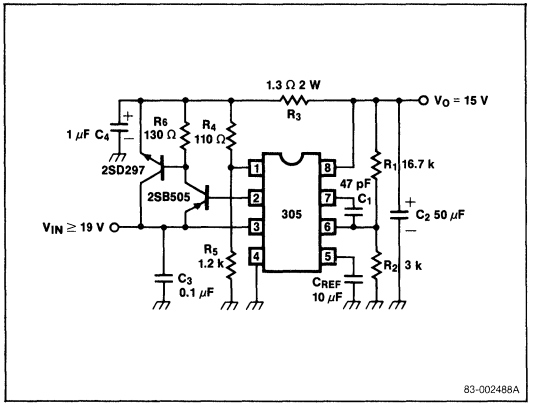
5 V — 15 mA Regulator



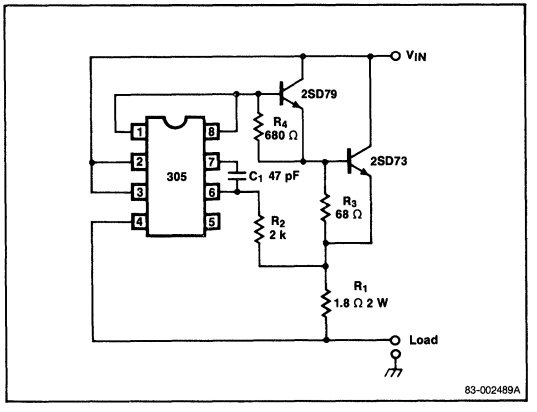
10 V — 200 mA Regulator



15 V — 1 A Foldback Current Limit



1 A Regulator



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μPC317
THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

Description

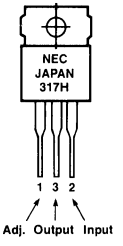
The μPC317 is an adjustable three-terminal positive voltage regulator capable of supplying in excess of 1.5 A over a 1.3 V to 30 V output voltage range.

Output voltage can be fixed by two external resistors.

Features

- ☐ Output current up to 1.5 A
- ☐ Current limit constant with temperature
- ☐ Internal thermal overload protection
- ☐ Equivalent to LM317

Pin Configuration

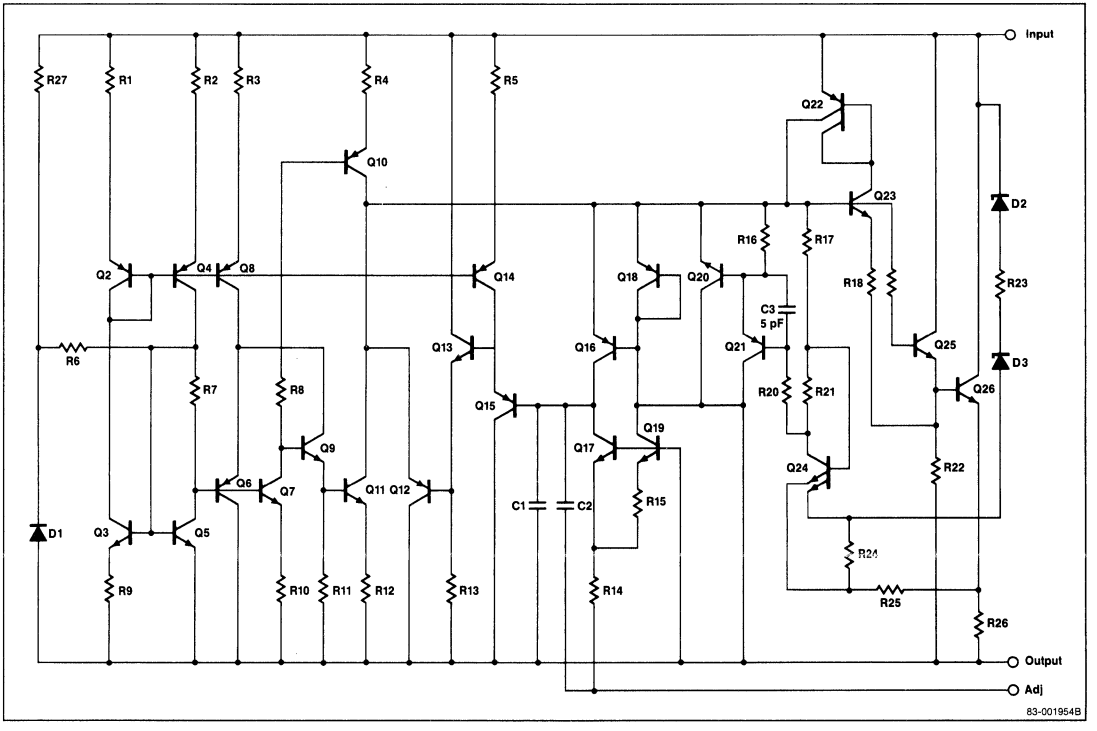


83-002523A

Ordering Information

Part Number	Package	Operating Temperature Range
μPC317H	3 pin SIP	−20°C to +80°C

Equivalent Circuit



83-001954B

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Absolute Maximum Ratings

$T_A = +25°C$

Input-Output Voltage Differential	40 V
Internal Power Dissipation (Note 1)	20 W
Operating Temperature Range	−20°C to +150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 s)	300°C
Thermal Resistance (junction to case)	4°C/W
Thermal Resistance (junction to ambient)	83°C/W

Note: 1. Internally limited.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input-Output Voltage Differential	$V_{IN} - V_O$	3		38.7	V	
Output Voltage	V_O	1.3		30	V	
Input Voltage	V_{IN}	4.3		40	V	
Output Current	I_O	0.01		1.5	A	
Operating Temperature Range	T_J	−20		+125	°C	

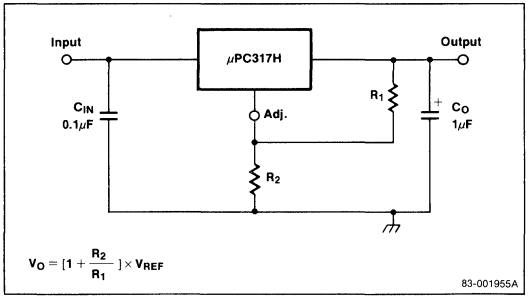
Electrical Characteristics

($V_{IN} - V_O = 5$ V, $I_O = 0.5$ A, $0°C \leq T_J \leq +125°C$)

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Line Regulation (Note 1)	REG_{IN}		0.01	0.04	%/V	$T_A = 25°C$, $3 V \leq (V_{IN} - V_O) \leq 40 V$
			0.02	0.07	%/V	$0°C \leq T_J \leq +125°C$, $3 V \leq (V_{IN} - V_O) \leq 40 V$
Load Regulation (Note 1)	REG_L		5	25	mV	$V_O \leq 5$ V, $T_J = 25°C$, $10 mA \leq I_O \leq 1.5 A$
			0.1	0.5	% V_O	$V_O \geq 5$ V, $T_J = 25°C$, $10 mA \leq I_O \leq 1.5 A$
			20	70	mV	$V_O \leq 5$ V, $0°C \leq T_J \leq +125°C$, $10 mA \leq I_O \leq 1.5 A$
			0.3	1.5	% V_O	$V_O \geq 5$ V, $0°C \leq T_J \leq +125°C$, $10 mA \leq I_O \leq 1.5 A$
Thermal Regulation	REG_{TH}		0.02	0.07	%/W	$T_J = 25°C$, $0.2 ms \leq t \leq 20 ms$
Adjustment Pin Current	I_{ADJ}		50	100	μA	
Adjustment Pin Current Change	ΔI_{ADJ}		0.4	5	μA	$10 mA \leq I_O \leq 1.5 A$, $3 V \leq (V_{IN}-V_O) \leq 40 V$, $P_D \leq 20 W$
Reference Voltage	V_{REF}	1.20	1.25	1.30	V	$10 mA \leq I_O \leq 1.5 A$, $3 V \leq (V_{IN}-V_O) \leq 40 V$, $P_D \leq 20 W$
V_{REF} Drift	$\Delta V_{REF}/\Delta T$		0.7		%	$0°C \leq T_J \leq +125°C$
Load Current	I_O		4.7	10	mA	$(V_{IN} - V_O) = 40 V$
Peak Output Current	I_{OPEAK}	1.5	2.2	2.9	A	$5 V \leq (V_{IN} - V_O) \leq 15 V$
		0.15	0.8			$(V_{IN} - V_O) \leq 40 V$
Output Noise Voltage	V_N		0.001		% V_O (RMS)	$T_J = 25°C$, $10 Hz \leq f \leq 10 kHz$
Ripple Rejection Ratio	RR		48		dB	$C_{ADJ} = 0$, $V_O = 10$ V, $f = 120$ Hz, $\Delta V_{IN} = 1$ V RMS
		56	65		dB	$C_{ADJ} = 10$ μF, 10 V, $f = 120$ Hz, $\Delta V_{IN} = 1$ V RMS

Notes: 1. Measured at constant junction temperature, using pulse testing with a low duty cycle. PW = 10 ms, duty cycle ≤ 2%.

Typical Applications



$$V_O = [1 + \frac{R_2}{R_1}] \times V_{REF}$$

NEC Electronics Inc.

μPC337
THREE-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

PRELIMINARY INFORMATION

Description

The μPC337 is an adjustable three terminal negative voltage regulator capable of supplying up to 1.5A over a voltage range of −1.3 to −30 V. Output voltage is set by only two external resistors.

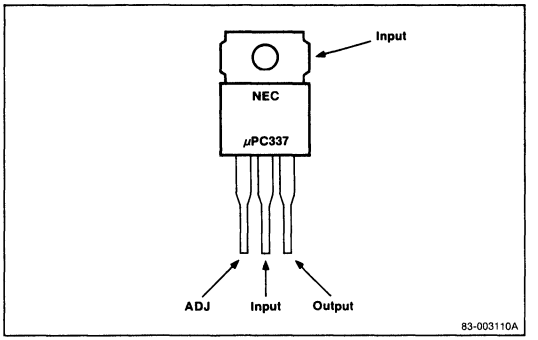
Features

- ☐ Output current up to 1.5A
- ☐ Current limit constant with temperature
- ☐ Internal thermal overload protection
- ☐ Output transistor safe area protection

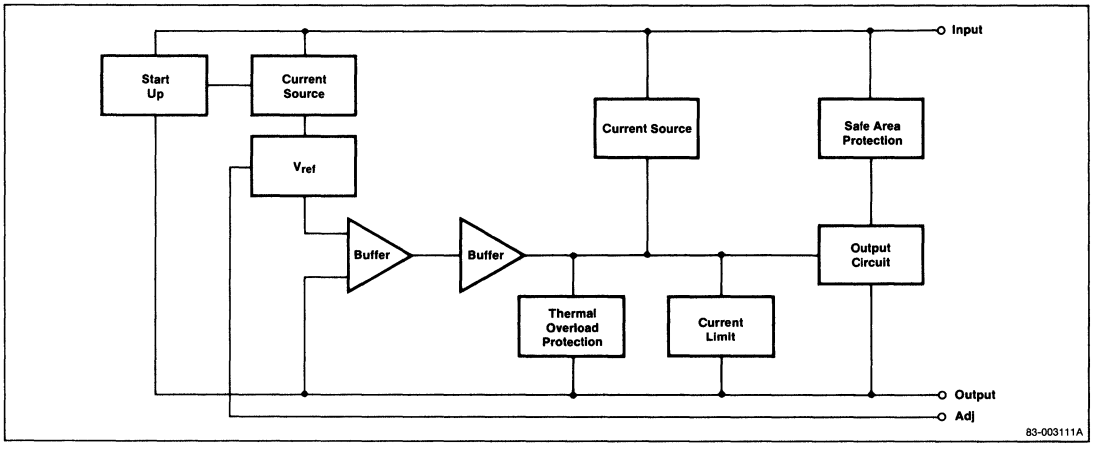
Ordering Information

Part Number	Package	Operating Temperature Range
μPC337H	TO-220	−20 °C to +85 °C

Pin Configuration



Block Diagram



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Absolute Maximum Ratings

($T_A = 25°C$)

Input Output Voltage Differential	−40 V
Total Power Dissipation	25 W (Note 1)
Operating Temperature Range	−20 to +85 °C
Operating Junction Temperature	−20 to +150 °C
Storage Temperature	−65 to +150 °C
Junction to Case Thermal Resistance	4 °C/W
Junction to Ambient Thermal Resistance	83 °C/W

Note: (1) Thermal overload protection circuit shuts off the output whenever $T_J \geq 150°C$.

Comment: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit
Input Output Voltage Differential	V_{IN}-V_O	−3	−5	−38.7	V
Input Voltage	V_{IN}	−4.3		−40	V
Output Voltage	V_O	−1.3		−30	V
Output Current	I_O	0.01		1.5	A
Operating Junction Temperature	T_J	−20		125	°C

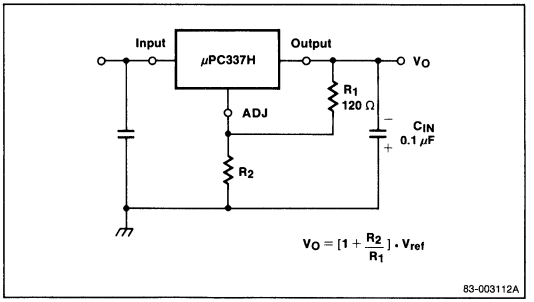
Electrical Characteristics

V_{IN}-V_O = −5 V, I_O = 0.5 A, 0 °C ≤ T_j ≤ + 125 °C

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Line Regulation	REG_{IN}		0.01	0.04	%/V	T_J = 25 °C, 3 V ≤ $\|V_{IN}$-$V_O\|$ ≤ 40 V (Note 1)
			0.02	0.07	%/V	0 °C ≦ T_J ≤ 125 °C, 3 V ≤ $\|V_{IN}$- $V_O\|$ ≤ 40 V
Load Regulation	REG_L		15	50	mV	T_J = 25 °C, (Note 1) $\|V_O\| \leq 5$ V
			0.3	1.0	%	10 mA ≤ I_O ≤ 1.5 A $\|V_O\| \geq 5$ V
			20	70	mV	0 ≤ T_J ≤ 125 °C (Note 1) $\|V_O\| \leq 5$ V
			0.3	1.5	%	10 mA ≤ I_O ≤ 1.5 A $\|V_O\| \geq 5$ V
Thermal Regulation	REG_{TH}		0.003	0.04	%/W	T_J = 25 °C, $\|V_{IN}$-$V_O\|$ = 40 V, V_O = −10 V, 0 ≤ I_O ≤ 0.25A, t = 10 ns
Adjustment Pin Current	I_{ADJ}		65	100	μA	
Adjustment Pin Current Change	ΔI_{ADJ}		2	5	μA	T_J = 25 °C, 3 V ≤ $\|V_{IN}$-$V_O\|$ ≤ 40 V, 10 mA ≤ I_O ≤ 1.5A (Note 2)
Reference Voltage	V_{REF}	−1.20	−1.25	−1.30	V	3 V ≤ $\|V_{IN}$-$V_O\|$ ≤ 40 V, 10 mA ≤ I_O ≤ 1.5A (Note 2)
V_{REF} Drift	$\Delta V_{REF}/\Delta T$		0.6		%	0 °C ≤ T_J ≤ 125 °C, I_O = 5 mA
Minimum Load Current	I_O Min		2.5	10	mA	$\|V_{IN}$-$V_O\|$ = 40 V
Peak Output Current	I_{OPEAK}	1.5	2.2	2.9	A	3 V ≤ $\|V_{IN}$-$V_O\|$ ≤ 15 V
		0.15	0.4		A	$\|V_{IN}$-$V_O\|$ = 40 V
Output Noise Voltage	e_n		0.003		%	T_J = 25 °C, 10 Hz ≤ f ≤ 10 kHz
Ripple Rejection	RR		60		dB	T_J = 25 °C, ΔV_O = 1 V_{rms} C_{ADJ} = 0
		66	70		dB	f = 120 Hz, V_O = 10 V C_{ADJ} = 10 μF

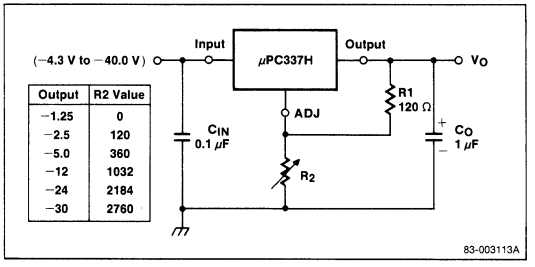
Note: 1. Pulse Measurement P_W = 10 ms, duty cycle ≦ 2%.
2. Internal Power Dissipation ≦ 20 W.

Typical Connection



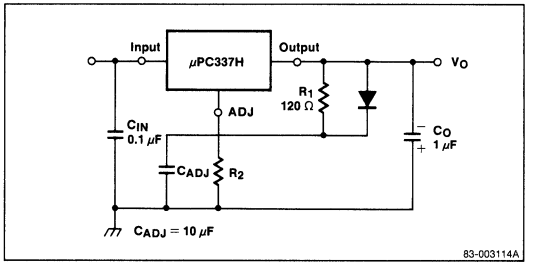
Typical Applications

1. *Variable Output Regulator*
VO = −1.3 V to −30 V

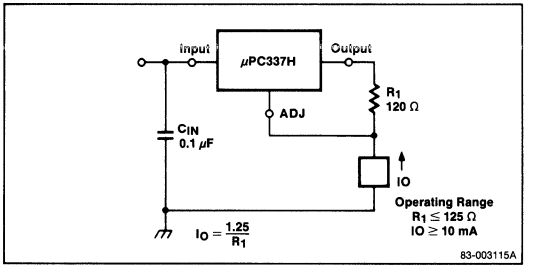


Output	R2 Value
−1.25	0
−2.5	120
−5.0	360
−12	1032
−24	2184
−30	2760

2. *Ripple Rejection Improvement*



3. *Current Regulator*



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NEC

NEC Electronics Inc.

μPC2600 SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

PRELIMINARY INFORMATION

Description

The μPC2600 series are monolithic three terminal positive regulators which employ protection circuits against the dangerous overvoltages always present on the battery rail of the car. They are intended as fixed-voltage regulators for car instrumentation in vehicles with 12 V battery and can supply an output current up to 500 mA.

Features

- ☐ Output voltages of 5 V and 10 V
- ☐ Output current up to 500 mA
- ☐ No external components
- ☐ Low dropout voltage
- ☐ Load dump voltage surge protection
- ☐ Reverse voltage protection
- ☐ Internal thermal overload protection
- ☐ Internal short circuit current limiting

Ordering Information

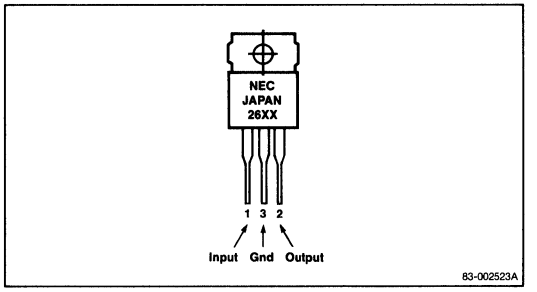
Part Number	Package	Operating Temperature Range
μPC2600H	Plastic SIP	−30 to +85 °C

Recommended Operating Conditions

$T_A = 25\,°C$

Item	Symbol	Limit Min.	Typ.	Max.	Unit	Test Conditions
Input voltage	V_{IN}		12	28	V	
Output Current	I_O	50		500	mA	
Operating Junction Temperature Range	T_j	−12		+125	°C	

Pin Configuration



Absolute Maximum Ratings

$T_A = 25\,°C$

DC Input Voltage, V_{IN} (DC)	−35 V
DC Input Reverse Voltage $-V_{IN}$ (DC)	−28 V
Positive Transient Voltage, V_{IN} (t = 40 ms, duty cycle = 1%) (surge)	120 V
Negative Transient Voltage, $-V_{IN}$ (t = 30 ms, duty cycle = 1%) (surge)	−90 V
Internal Power Dissipation, P_T ($T_C = 25\,°C$)	20 W (Note 1)
Operating Junction Temperature Range, $T_{opt\,(j)}$	−30 to +150 °C
Operating Temperature Range, T_{opt}	−30 to +85 °C
Storage Temperature Range, T_{stg}	−65 to +150 °C
Thermal Resistance (junction to case), $R_{th\,(j\text{-}c)}$	4 °C/W
Thermal Resistance (junction to ambient), $R_{th\,(j\text{-}a)}$	83 °C/W

Note: 1. Internally limited.

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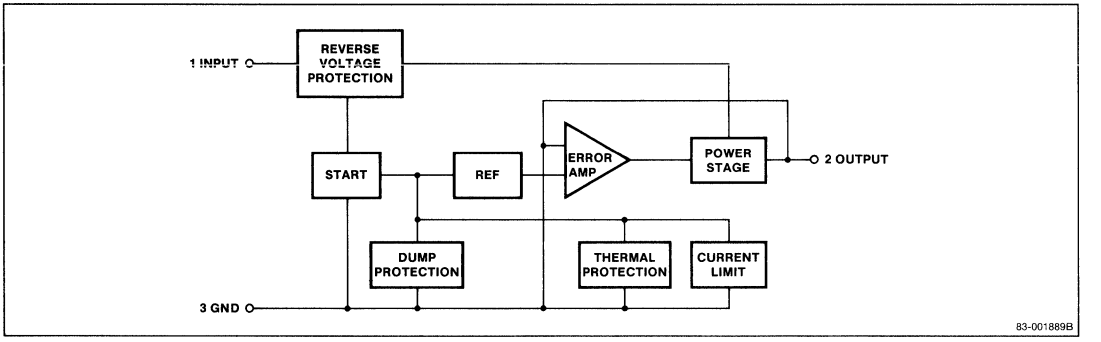
Block Diagram

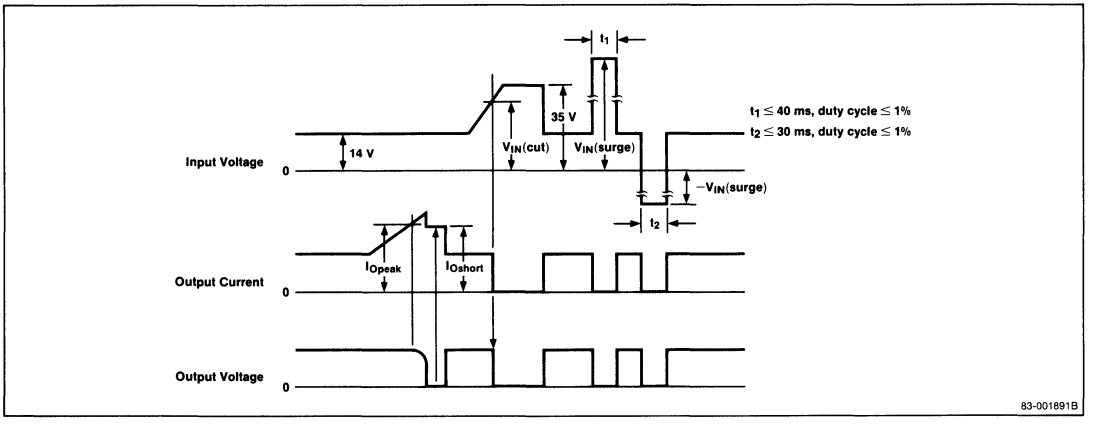


Electrical Characteristics

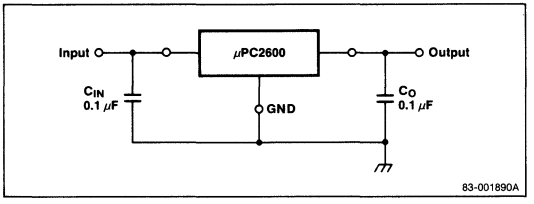
$T_A = 25°C$

Item		Symbol	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
Output Voltage	μPC2605	V_O	4.8	5.0	5.2	V	$12\ V \le V_{IN} \le 16\ V,\ I_O = 500\ mA$
	μPC2610	V_O	9.55	10.0	10.45	V	$12\ V \le V_{IN} \le 16\ V,\ I_O = 500\ mA$
Line Regulation		REG_{IN}		7	20	mV	$12\ V \le V_{IN} \le 16\ V,\ I_O = 50\ mA$
Load Regulation		REG_L		0.3	1.0	$\%V_O$	$V_{IN} = 14\ V,\ 50\ mA \le I_O \le 500\ mA$
Quiescent Current	μPC2605	I_{BIAS}		37		mA	$V_{IN} = 14\ V,\ I_O = 500\ mA$
	μPC2610	I_{BIAS}		150		mA	$V_{IN} = 14\ V,\ I_O = 500\ mA$
Ripple Rejection		RR	56			dB	$15\ V \le V_{IN} \le 17\ V,\ I_O = 500\ mA$ $f = 100\ Hz$
Output Noise Voltage	μPC2605	V_N		27		μV_{RMS}	$V_{IN} = 14\ V,\ I_O = 500\ mA$
	μPC2610	V_N		53		μV_{RMS}	$V_{IN} = 14\ V,\ I_O = 500\ mA$
Dropout Voltage		V_{DIF}		1.3	1.7	V	$I_O = 500\ mA$
Short Circuit Current		I_{Oshort}		900		mA	$V_{IN} = 14\ V$
Peak Output Current		I_{Opeak}	650	1,000		mA	$V_{IN} = 14\ V$
Output Resistance		R_O		0.07		Ω	$V_{IN} = 14\ V,\ 400\ mA \le I_O \le 500\ mA$ $f = 1\ kHz$
Lockout Input Voltage		V_{IN} (cut)	28	32	35	V	$V_O = 0$
Output Voltage Drift		$\Delta V_O/\Delta T$		0.4		mV/°C	$V_{IN} = 14\ V,\ I_O = 50\ mA,$ $-12°C \le T_A \le +80°C$

Timing Waveform



Typical Application



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NEC
NEC Electronics Inc.

μPC78L00H SERIES THREE-TERMINAL 0.1 A POSITIVE VOLTAGE REGULATORS

Description

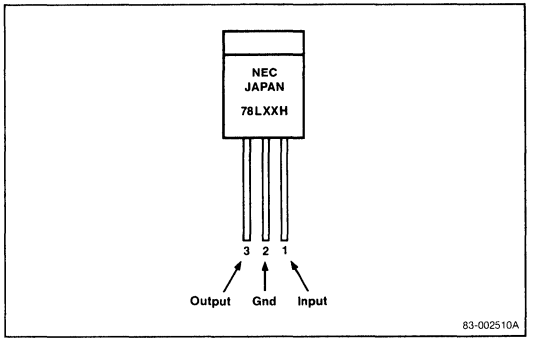
The μPC78L00H series of three terminal regulators are monolithic positive voltage regulators which feature internal current limiting and thermal shutdown. They are intended for use as fixed voltage regulators in a wide range of applications, including local on-card regulators where distribution with single point regulation is a problem.

This device is not recommended for new designs. Use μPC78L00J instead.

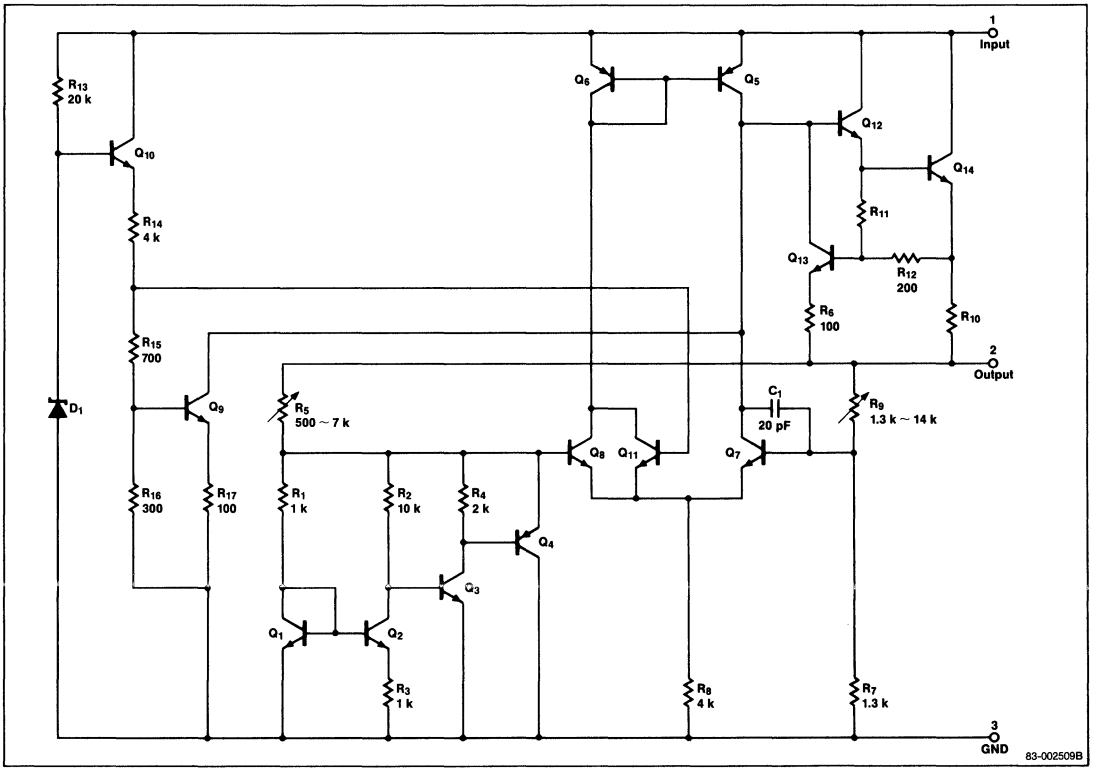
Features

- ☐ Output current in excess of 100 mA
- ☐ No external component required
- ☐ Internal thermal overload protection
- ☐ Internal short circuit current limiting

Pin Configuration



Equivalent Circuit



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Ordering Information

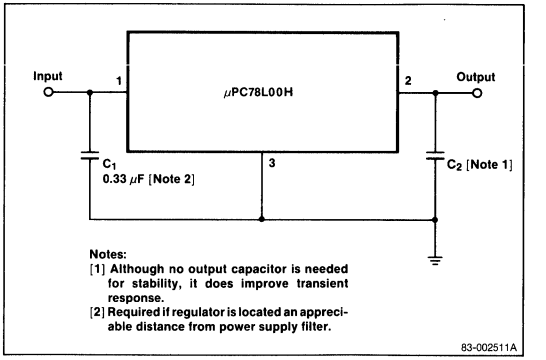
Part Number	Package	Operating Temperature Range
μPC78L05H	Plastic SIP	−20 °C to +80 °C
μPC78L08H	Plastic SIP	−20 °C to +80 °C
μPC78L10H	Plastic SIP	−20 °C to +80 °C
μPC78L12H	Plastic SIP	−20 °C to +80 °C
μPC78L15H	Plastic SIP	−20 °C to +80 °C
μPC78L10H	Plastic SIP	−20 °C to +80 °C

Absolute Maximum Ratings

Input Voltage (μPC78L05H/78L08H)	30 V
Input Voltage (μPC78L10H/78L12H/78L15H)	35 V
Internal Power Dissipation	800 mW
Operating Temperature Range	−20 to +80 °C
Storage Temperature	−55 to +150 °C
Operating Junction Temperature Range	−20 to + 150 °C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Typical Application



Notes:
[1] Although no output capacitor is needed for stability, it does improve transient response.
[2] Required if regulator is located an appreciable distance from power supply filter.

83-002511A

Electrical Characteristics — μPC78L05H

V_{IN} = 10 V, I_O = 40 mA, 0 °C ≤ T_J ≤ 125 °C, C_I = 0.33 μF, C_O = 0.1 μF

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	4.6	5.0	5.4	V	T_J = 25 °C
Line Regulation	REG_{IN}		55	200	mV	T_J = 25 °C, 7 V ≤ V_{IN} ≤ 20 V
			45	150	mV	T_J = 25 °C, 8 V ≤ V_{IN} ≤ 20 V
Load Regulation	REG_L		11	60	mV	T_J = 25 °C, 1 mA ≤ I_O ≤ 100 mA
			5.0	30	mV	T_J = 25 °C, 1 mA ≤ I_O ≤ 40 mA
Output Voltage	V_O	4.5		5.5	V	7 V ≤ V_{IN} ≤ 20 V, 1 mA ≤ I_O ≤ 40 mA
		4.5		5.5	V	V_{IN} = 10 V, 1 mA ≤ I_O ≤ 70 mA
Quiescent Current	I_{BIAS}		3.8	6.0	mA	T_J = 25 °C
				5.5	mA	T_J = 125 °C
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	8 V ≤ V_{IN} ≤ 20 V, I_O = 40 mA
				0.2	mA	V_{IN} = 10 V, 1 mA ≤ I_O ≤ 40 mA
Output Noise Voltage	V_N		30		μV	T_A = 25 °C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	40	50		dB	f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V, T_J = 25 °C
Temperature Coefficient of Output Voltage	$V_O/\Delta T$		−0.65		mV/°C	I_O = 5 mA
Dropout Voltage	V_{DO}		1.7		V	T_J = 25 °C
Short Circuit Current	I_{OSHORT}		150		mA	T_J = 25 °C

Electrical Characteristics — μPC78L08H

V_{IN} = 14 V, I_O = 40 mA, 0 °C ≤ T_J ≤ 125 °C, C_I = 0.33 μF, C_O = 0.1 μF

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	7.36	8.0	8.64	V	T_J = 25 °C
Line Regulation	REG_{IN}		80	200	mV	T_J = 25 °C, 10.5 V ≤ V_{IN} ≤ 23 V
			70	150	mV	T_J = 25 °C, 11 V ≤ V_{IN} ≤ 23 V
Load Regulation	REG_L		15	80	mV	T_J = 25 °C, 1 mA ≤ I_O ≤ 100 mA
			8.0	40	mV	T_J = 25 °C, 1 mA ≤ I_O ≤ 40 mA
Output Voltage	V_O	7.2		8.8	V	10.5 V ≤ V_{IN} ≤ 23 V, 1 mA ≤ I_O ≤ 40 mA
		7.2		8.8	V	V_{IN} = 14 V, 1 mA ≤ I_O ≤ 70 mA
Quiescent Current	I_{BIAS}		3.9	6.0	mA	T_J = 25 °C
				5.5	mA	T_J = 25 °C
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	12 V ≤ V_{IN} ≤ 23 V, I_O ≤ 40 mA
				0.2	mA	V_{IN} = 14 V, 1 mA ≤ I_O ≤ 40 mA
Output Noise Voltage	V_N		60		μV	T_A = 25 °C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	38	45		dB	f = 120 Hz, 12 V ≤ V_{IN} ≤ 22 V, T_J = 25 °C
Temperature Coefficient of Output Voltage	$V_O/\Delta T$		−0.8		mV/°C	I_O = 5 mA
Dropout Voltage			1.7		V	T_J = 25 °C
Short Circuit Current	I_{OSHORT}		150		mA	T_J = 25 °C

Electrical Characteristics — μPC78L10H

V_{IN} = 17 V, I_O = 40 mA, 0 °C ≤ T_J ≤ 125 °C, C_I = 0.33 μF, C_O = 0.1 μF

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	9.2	10	10.8	V	T_J = 25 °C
Line Regulation	REG_{IN}		100	230	mV	T_J = 25 °C, 12.5 V ≤ V_{IN} ≤ 25 V
			80	170	mV	T_J = 25 °C, 13 V ≤ V_{IN} ≤ 25 V
Load Regulation	REG_L		18	90	mV	T_J = 25 °C, 1 mA ≤ I_O ≤ 100 mA
			9	45	mV	T_J = 25 °C, 1 mA ≤ I_O ≤ 40 mA
Output Voltage	V_O	9.0		11.0	V	12.5 V ≤ V_{IN} ≤ 25 V, 1 mA ≤ I_O ≤ 40 mA
		9.0		11.0	V	V_{IN} = 17 V, 1 mA ≤ I_O ≤ 70 mA
Quiescent Current	I_{BIAS}		4.0	6.0	mA	T_J = 25 °C
				5.5	mA	T_J = 25 °C
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	13 V ≤ V_{IN} ≤ 25 V, I_O ≤ 40 mA
				0.2	mA	V_{IN} = 17 V, 1 mA ≤ I_O ≤ 40 mA
Output Noise Voltage	V_N		70		μV_{RMS}	T_A = 25 °C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	37	44		dB	f = 120 Hz, 14 V ≤ V_{IN} ≤ 24 V, T_J = 25 °C
Temperature Coefficient of Output Voltage	$V_O/\Delta T$		−0.9		mV/°C	I_O = 5 mA
Dropout Voltage			1.7		V	T_J = 25 °C
Short Circuit Current	I_{OSHORT}		150		mA	T_J = 25 °C

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Electrical Characteristics — μPC78L12H

V_{IN} = 19 V, I_O = 40 mA, 0°C ≤ T_J ≤ 125°C, C_I = 0.33 μF, C_O = 0.1 μF

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	11.1	12	12.9	V	T_J = 25°C
Line Regulation	REG_{IN}		120	250	mV	T_J = 25°C, 14.5 V ≤ V_{IN} ≤ 27 V
			100	200	mV	T_J = 25°C, 16 V ≤ V_{IN} ≤ 27 V
Load Regulation	REG_L		20	100	mV	T_J = 25°C, 1 mA ≤ I_O ≤ 100 mA
			10	50	mV	T_J = 25°C, 1 mA ≤ I_O ≤ 40 mA
Output Voltage	V_O	10.8		13.2	V	14.5 V ≤ V_{IN} ≤ 27 V, 1 mA ≤ I_O ≤ 40 mA
		10.8		13.2	V	V_{IN} = 19 V, 1 mA ≤ I_O ≤ 70 mA
Quiescent Current	I_{BIAS}		4.2	6.5	mA	T_J = 25°C
				6.0	mA	T_J = 125°C
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	16 V ≤ V_{IN} ≤ 27 V, I_O ≤ 40 mA
				0.2	mA	V_{IN} = 19 V, 1 mA ≤ I_O ≤ 40 mA
Output Noise Voltage	V_N		80		μV	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	36	42		dB	f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V, T_J = 25°C
Temperature Coefficient of Output Voltage	$V_O/\Delta T$		−1.0		mV/°C	I_O = 5 mA
Dropout Voltage			1.7		V	T_J = 25°C
Short Circuit Current	I_{OSHORT}		150		mA	T_J = 25°C

Electrical Characteristics — μPC78L15H

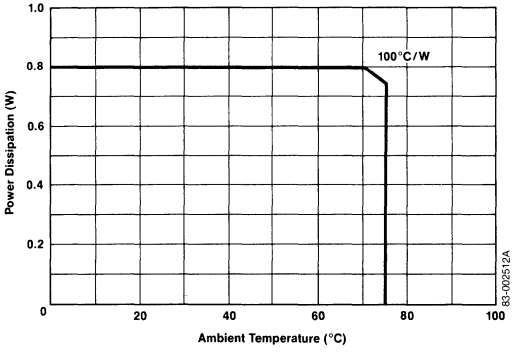
V_{IN} = 23 V, I_O = 40 mA, 0°C ≤ T_J ≤ 125°C, C_I = 0.33 μF, C_O = 0.1 μF

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	13.8	15	16.2	V	T_J = 25°C
Line Regulation	REG_{IN}		130	300	mV	T_J = 25°C, 17.5 V ≤ V_{IN} ≤ 30 V
			110	250	mV	T_J = 25°C, 20 V ≤ V_{IN} ≤ 30 V
Load Regulation	REG_L		25	150	mV	T_J = 25°C, 1 mA ≤ I_O ≤ 100 mA
			12	75	mV	T_J = 25°C, 1 mA ≤ I_O ≤ 40 mA
Output Voltage	V_O	13.5		16.5	V	17.5 V ≤ V_{IN} ≤ 30 V, 1 mA ≤ I_O ≤ 40 mA
		13.5		16.5	V	V_{IN} = 23 V, 1 mA ≤ I_O ≤ 70 mA
Quiescent Current	I_{BIAS}		4.4	6.5	mA	T_J = 25°C
				6.0	mA	T_J = 125°C
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	20 V ≤ V_{IN} ≤ 30 V, I_O ≤ 40 mA
				0.2	mA	V_{IN} = 23 V, 1 mA ≤ I_O ≤ 40 mA
Output Noise Voltage	V_N		90		μV	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	33	39		dB	f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V, T_J = 25°C
Temperature Coefficient of Output Voltage	$V_O/\Delta T$		−1.3		mV/°C	I_O = 5 mA
Dropout Voltage			1.7		V	T_J = 25°C
Short Circuit Current	I_{OSHORT}		150		mA	T_J = 25°C

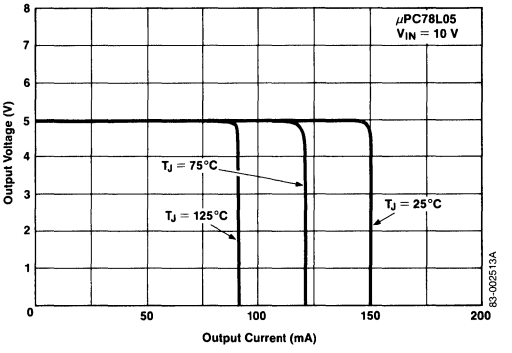
Operating Characteristics

$T_A = +25°C$

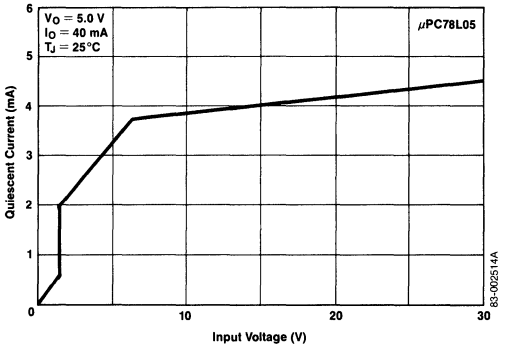
Worst Case Power Dissipation vs. Ambient Temperature



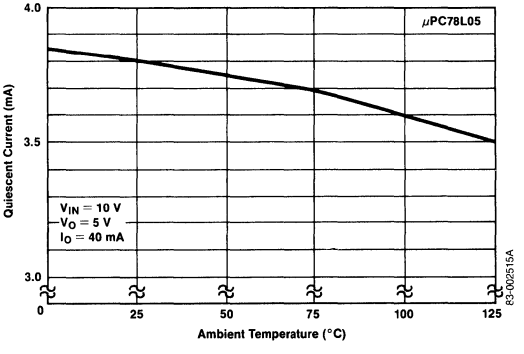
Current Limiting Characteristics



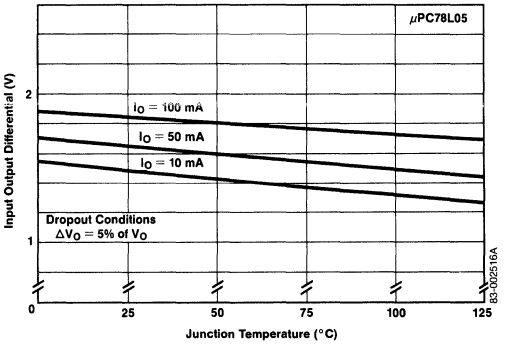
Quiescent Current as a Function of Input Voltage



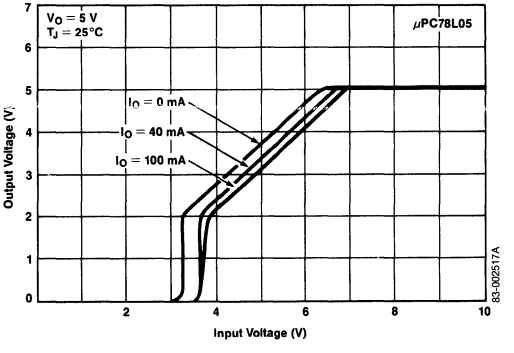
Quiescent Current as a Function of Temperature



Dropout Voltage as a Function of Junction Temperature



Dropout Characteristics



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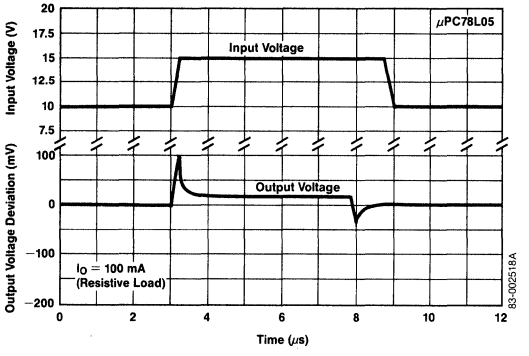
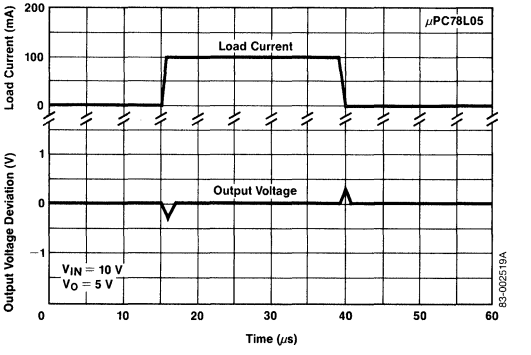
Operating Characteristics (Cont.)

$T_A = \pm 25\,°C$

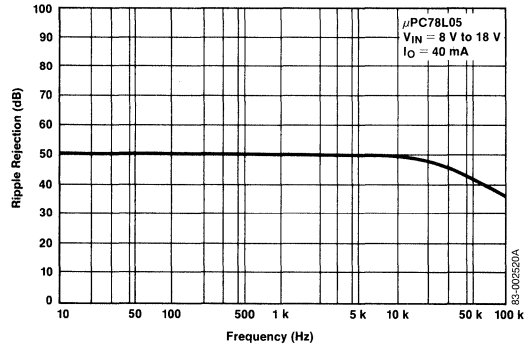
Line Transient Response



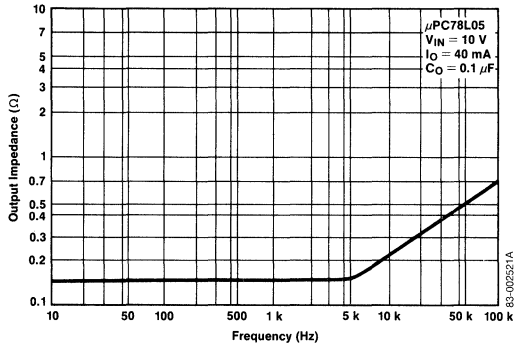
Load Transient Response



Ripple Rejection as a Function Frequency



Output Impedance as a Function of Frequency



μPC78L00J SERIES THREE-TERMINAL 0.1 A POSITIVE VOLTAGE REGULATORS

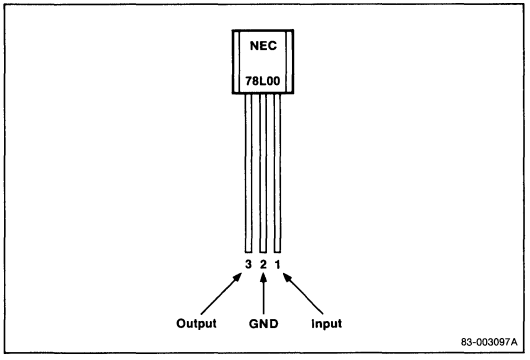
Description

The μPC78L00J series of three terminal regulators are monolithic positive voltage regulators which feature internal current limiting and thermal shutdown. They are intended for use as fixed voltage regulators in a wide range of applications, including local on-card regulators where distribution with single point regulation is a problem.

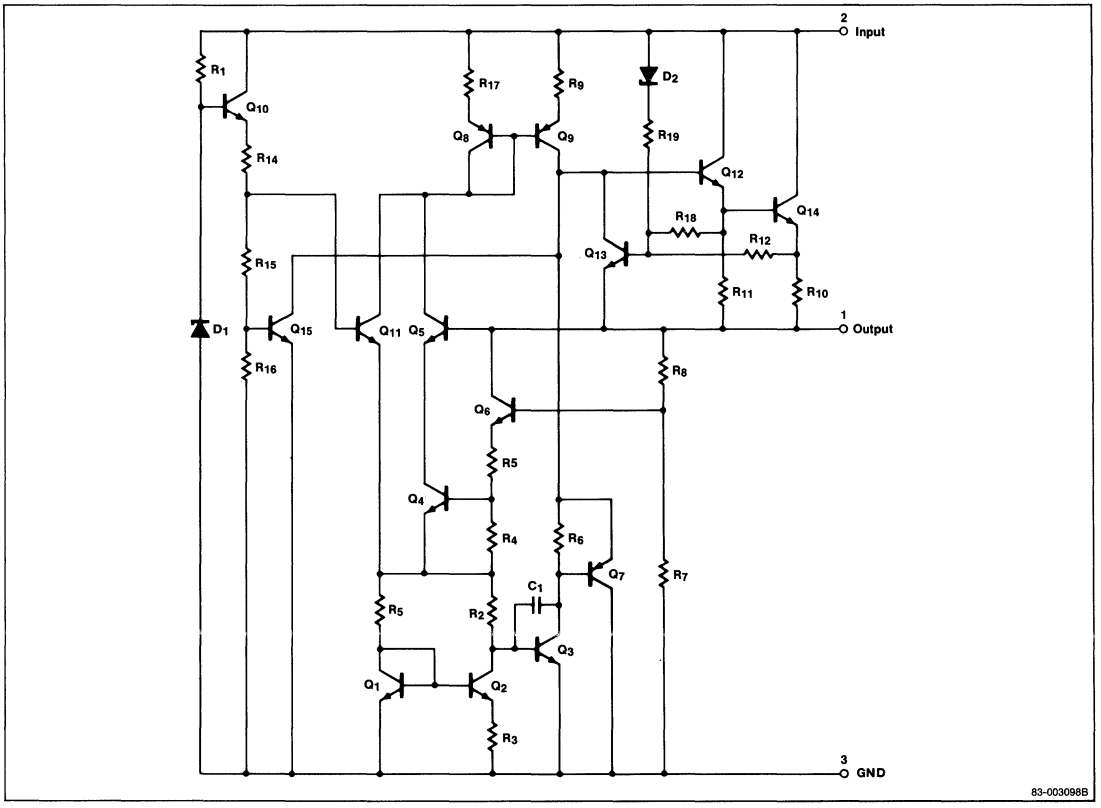
Features

- ☐ Output current in excess of 100 mA
- ☐ No external component required
- ☐ Internal thermal overload protection
- ☐ Internal short circuit current limiting

Pin Configuration



Equivalent Circuit



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Ordering Information

Part Number	Package	Operating Temperature Range
μPC78L05J	TO-92	−20 °C to +80 °C
μPC78L08J	TO-92	−20 °C to +80 °C
μPC78L12J	TO-92	−20 °C to +80 °C
μPC78L15J	TO-92	−20 °C to +80 °C
μPC78L18J	TO-92	−20 °C to +80 °C
μPC78L24J	TO-92	−20 °C to +80 °C

Absolute Maximum Ratings

Input Voltage (μPC78L05J/78L08J)	30 V
Input Voltage (μPC78L10J/78L12J/78L15J)	35 V
Internal Power Dissipation	800 mW
Operating Temperature Range	−20 to +80 °C
Storage Temperature	−55 to +150 °C
Operating Junction Temperature Range	−20 to + 150 °C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Type Number	Limits Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}	μPC78L05J	7	10	20	V
		μPC78L08J	10.5	14	23	
		μPC78L10J	12.5	17	25	
		μPC78L12J	14.5	19	27	
		μPC78L15J	17	23	30	
Output Current	I_O	All	0	40	70	mA
Internal Power Dissipation	P_D	All		200	220	mW
Operating Ambient Temperature	T_{opt}	All	−20		80	°C
Operating Junction Temperature	T_J	All	−20		125	°C

Electrical Characteristics — μPC78L05J

V_{IN} = 10 V, I_O = 40 mA, 0 °C ≤ T_J ≤ 125 °C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	4.8	5.0	5.2	V	T_J = 25 °C
		4.75		5.25	V	7 V ≤ V_{IN} ≤ 20 V, 1 mA ≤ I_O ≤ 40 mA
		4.75		5.25	V	V_{IN} ≤ 10 V, 1 mA ≤ I_O ≤ 70 mA
Line Regulation	REG_{IN}		6	150	mV	T_J = 25 °C, 7 V ≤ V_{IN} ≤ 20 V
			4	100	mV	T_J = 25 °C, 8 V ≤ V_{IN} ≤ 20 V
Load Regulation	REG_L		9	60	mV	T_J = 25 °C, 1 mA ≤ I_O ≤ 100 mA
			4	30	mV	T_J = 25 °C, 1 mA ≤ I_O ≤ 40 mA
Quiescent Current	I_{BIAS}		2.3	5.5	mA	T_J = 25 °C
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	8 V ≤ V_{IN} ≤ 20 V, I_O ≤ 40 mA
				0.1	mA	5 mA ≤ I_O ≤ 350 mA
Output Noise Voltage	V_N		45	120	μV rms	T_J = 25 °C, f = 10 Hz to 100 kHz
Ripple Rejection	RR	55	75		dB	T_J = 25 °C, 8 V ≤ V_{IN} ≤ 18 V, f = 120 Hz
Dropout Voltage	V_{DIF}		1.7		V	T_J = 25 °C
Short Circuit Current	I_{OSHORT}		88		mA	T_J = 25 °C, V_{IN} = 20 V
Peak Output Current	I_{OPEAK}	125	160	205	mA	T_J = 25 °C
Output Voltage Drift	$\Delta V_O/\Delta T$		0.4		mV/°C	0 °C ≤ T_J ≤ 150 °C, I_O = 5 mA

Electrical Characteristics — μPC78L08J

V_{IN} = 14 V, I_O = 40 mA, 0 °C ≤ T_J ≤ 125 °C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Output Voltage	V_O	7.7	8.0	8.3	V	T_J = 25 °C
		7.6		8.4	V	10.5 V ≤ V_{IN} ≤ 23 V, 1 mA ≤ I_O ≤ 40 mA
		7.6		8.4	V	V_{IN} ≤ 14 V, 1 mA ≤ I_O ≤ 70 mA
Line Regulation	REG_{IN}		10	175	mV	T_J = 25 °C, 10.5 V ≤ V_{IN} ≤ 23 V
			6	125	mV	T_J = 25 °C, 11 V ≤ V_{IN} ≤ 23 V
Load Regulation	REG_L		14	80	mV	T_J = 25 °C, 1 mA ≤ I_O ≤ 100 mA
			6	40	mV	T_J = 25 °C, 1 mA ≤ I_O ≤ 40 mA
Quiescent Current	I_{BIAS}		2.4	5.5	mA	T_J = 25 °C
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	12 V ≤ V_{IN} ≤ 23 V, I_O ≤ 40 mA
				0.1	mA	V_{IN} = 14 V, 1 mA ≤ I_O ≤ 40 mA
Output Noise Voltage	V_N		85	190	μV rms	T_J = 25 °C, f = 10 Hz to 100 kHz
Ripple Rejection	RR	51	73		dB	T_J = 25 °C, 12 V ≤ V_{IN} ≤ 22 V, f = 120 Hz
Dropout Voltage	V_{DIF}		1.7		V	T_J = 25 °C
Short Circuit Current	I_{OSHORT}		80		mA	T_J = 25 °C, V_{IN} = 23 V
Peak Output Current	I_{OPEAK}	125	160	205	mA	T_J = 25 °C
Output Voltage Drift	$\Delta V_O/\Delta T$		0.6		mV/°C	0 °C ≤ T_J ≤ 125 °C, I_O = 5 mA

Electrical Characteristics — μPC78L10J

V_{IN} = 17 V, I_O = 40 mA, 0 °C ≤ T_J ≤ 125 °C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Output Voltage	V_O	9.6	10.0	10.4	V	T_J = 25 °C
		9.5		10.5	V	12.5 V ≤ V_{IN} ≤ 25 V, 1 mA ≤ I_O ≤ 40 mA
		9.5		10.5	V	V_{IN} = 17 V, 1 mA ≤ I_O ≤ 70 mA
Line Regulation	REG_{IN}		12	200	mV	T_J = 25 °C, 12.5 V ≤ V_{IN} ≤ 25 V
			8	150	mV	T_J = 25 °C, 13 V ≤ V_{IN} ≤ 25 V
Load Regulation	REG_L		18	90	mV	T_J = 25 °C, 1 mA ≤ I_O ≤ 100 mA
			8	45	mV	T_J = 25 °C, 1 mA ≤ I_O ≤ 40 mA
Quiescent Current	I_{BIAS}		2.5	5.5	mA	T_J = 25 °C
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	13 V ≤ V_{IN} ≤ 25 V, I_O ≤ 40 mA
				0.1	mA	V_{IN} = 17 V, 1 mA ≤ I_O ≤ 40 mA
Output Noise Voltage	V_N		100	230	μV rms	T_J = 25 °C, f = 10 Hz to 100 kHz
Ripple Rejection	RR	49	69		dB	T_J = 25 °C, 14 V ≤ V_{IN} ≤ 24 V, f = 120 Hz
Dropout Voltage	V_{DIF}		1.7		V	T_J = 25 °C
Short Circuit Current	I_{OSHORT}		70		mA	T_J = 25 °C, V_{IN} = 25 V
Peak Output Current	I_{OPEAK}	125	160	205	mA	T_J = 25 °C
Output Voltage Drift	$\Delta V_O/\Delta T$		0.8		mV/°C	0 °C ≤ T_J ≤ 125 °C, I_O = 5 mA

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Electrical Characteristics — μPC78L12J

V_{IN} = 19 V, I_O = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF

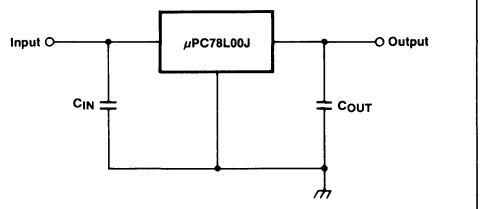
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	11.5	12.0	12.5	V	T_J = 25°C
		11.4		12.6	V	14 V ≤ V_{IN} ≤ 27 V, 1 mA ≤ I_O ≤ 40 mA
		11.4		12.6	V	V_{IN} = 19 V, 1 mA ≤ I_O ≤ 100 mA
Line Regulation	REG_{IN}		14	250	mV	T_J = 25°C, 14.5 V ≤ V_{IN} ≤ 27 V
			10	200	mV	T_J = 25°C, 16 V ≤ V_{IN} ≤ 27 V
Load Regulation	REG_L		20	100	mV	T_J = 25°C, 1 mA ≤ I_O ≤ 100 mA
			10	50	mV	T_J = 25°C, 1 mA ≤ I_O ≤ 40 mA
Quiescent Current	I_{BIAS}		2.6	5.5	mA	T_J = 25°C
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	16 V ≤ V_{IN} ≤ 27 V, I_O ≤ 40 mA
				0.1	mA	V_{IN} = 19 V, 1 mA ≤ I_O ≤ 40 mA
Output Noise Voltage	V_N		115	280	μV rms	T_J = 25°C, f = 10 Hz to 100 kHz
Ripple Rejection	RR	47	66		dB	T_J = 25°C, 15 V ≤ V_{IN} ≤ 25 V, f = 120 Hz
Dropout Voltage	V_{DIF}		1.7		V	T_J = 25°C
Short Circuit Current	I_{OSHORT}		64		mA	T_J = 25°C, V_{IN} = 27 V
Peak Output Current	I_{OPEAK}	125	160	205	mA	T_J = 25°C
Output Voltage Drift	$\Delta V_O/\Delta T$		1.1		mV/°C	0°C ≤ T_J ≤ 125°C, I_O = 5 mA

Electrical Characteristics — μPC78L15J

V_{IN} = 23 V, I_O = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	14.4	15.0	15.6	V	T_J = 25°C
		14.25		15.75	V	17.5 V ≤ V_{IN} ≤ 30 V, 1 mA ≤ I_O ≤ 40 mA
		14.25		15.75	V	V_{IN} = 23 V, 1 mA ≤ I_O ≤ 70 mA
Line Regulation	REG_{IN}		18	300	mV	T_J = 25°C, 17.5 V ≤ V_{IN} ≤ 30 V
			13	250	mV	T_J = 25°C, 20 V ≤ V_{IN} ≤ 30 V
Load Regulation	REG_L		25	150	mV	T_J = 25°C, 1 mA ≤ I_O ≤ 100 mA
			12	75	mV	T_J = 25°C, 1 mA ≤ I_O ≤ 40 mA
Quiescent Current	I_{BIAS}		2.7	5.5	mA	T_J = 25°C
Quiescent Current Change	ΔI_{BIAS}			1.5	mA	20 V ≤ V_{IN} ≤ 30 V, I_O ≤ 40 mA
				0.1	mA	V_{IN} = 23 V, 1 mA ≤ I_O ≤ 40 mA
Output Noise Voltage	V_N		135	350	μV rms	T_J = 25°C, f = 10 Hz to 100 kHz
Ripple Rejection	RR	45	61		dB	T_J = 25°C, 18 V ≤ V_{IN} ≤ 28.5 V, f = 120 Hz
Dropout Voltage	V_{DIF}		1.7		V	T_J = 25°C
Short Circuit Current	I_{OSHORT}		53		mA	T_J = 25°C, V_{IN} = 30 V
Peak Output Current	I_{OPEAK}	125	160	205	mA	T_J = 25°C
Output Voltage Drift	$\Delta V_O/\Delta T$		1.4		mV/°C	0°C ≤ T_J ≤ 125°C, I_O = 5 mA

Typical Connection



CIN: 0.1 to 0.47 μF [Required if regulator is located an appreciable distance from power supply filter.]

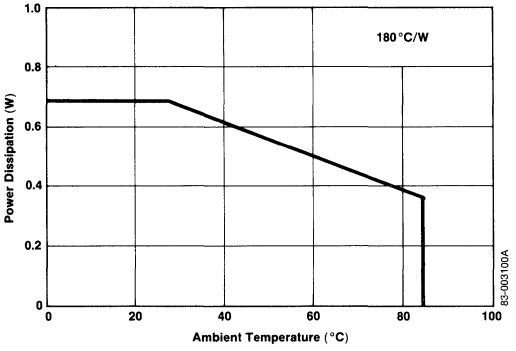
COUT: ≥ 0.22 μF [recommended mylar capacitor].

83-003099A

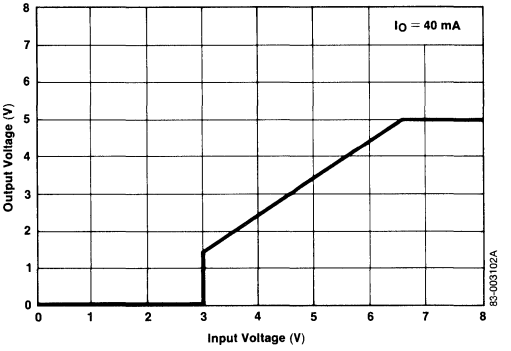
Operating Characteristics

$T_A = 25°C$

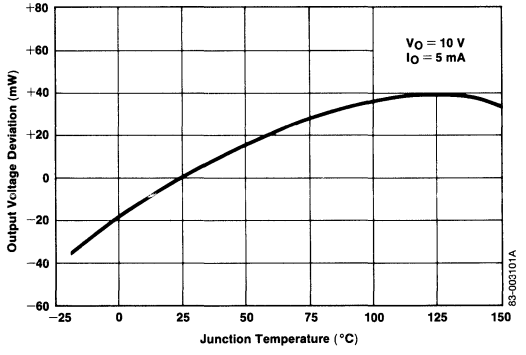
Worst Case Power Dissipation vs. Ambient Temperature



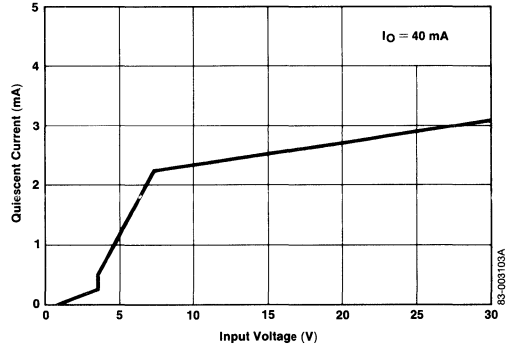
Dropout Characteristics



Output Voltage vs. Junction Temperature



Quiescent Current



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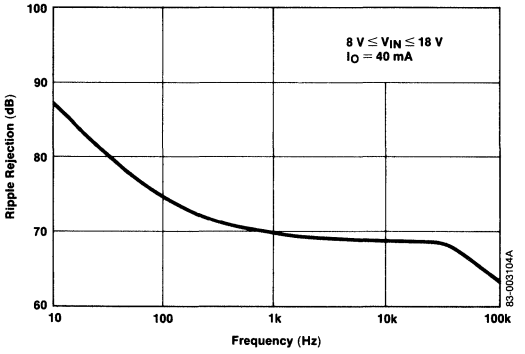
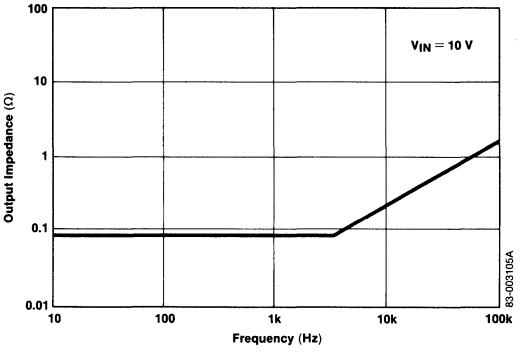
Operating Characteristics (Cont.)

$T_A = 25°C$

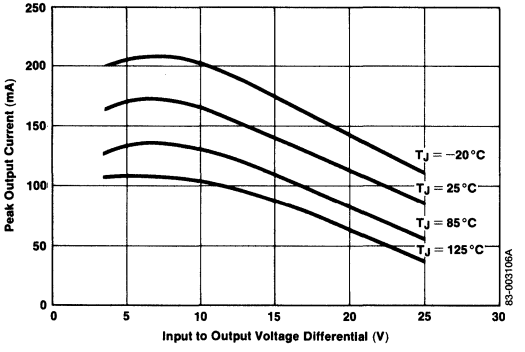
Ripple Rejection vs. Frequency



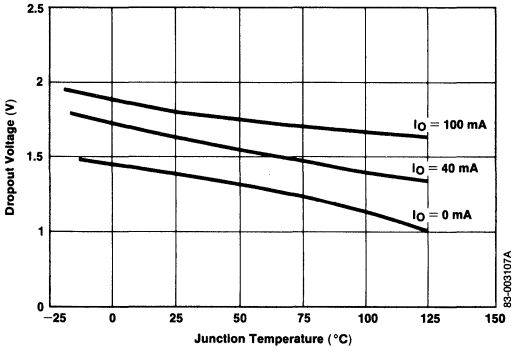
Output Impedance vs. Frequency



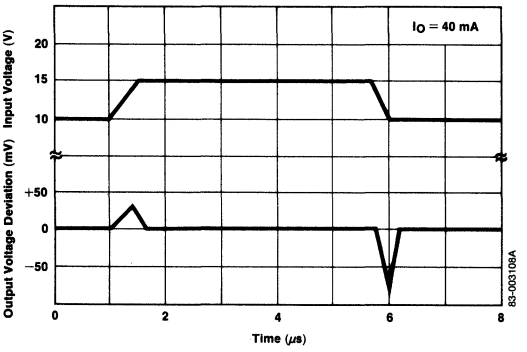
Peak Output Current as a Function of Input/Output Differential Voltage



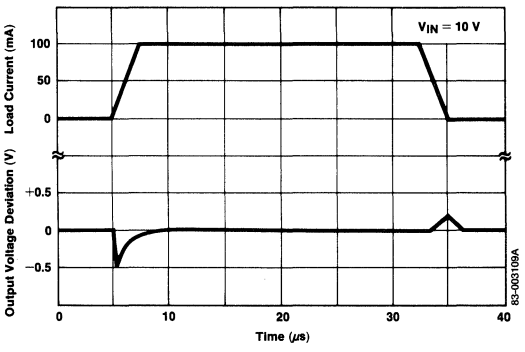
Dropout Voltage as a Function of Junction Temperature



Line Transient Response



Load Transient Response



NEC Electronics Inc.

μPC78M00 SERIES THREE-TERMINAL 0.5 A POSITIVE VOLTAGE REGULATORS

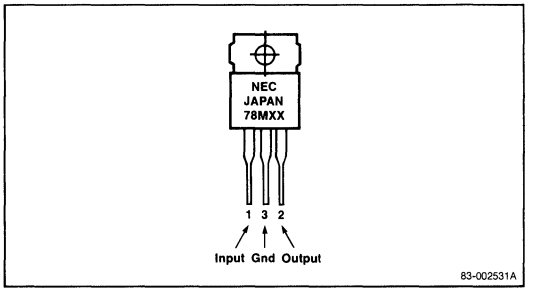
Description

The μPC78M00 series of three terminal regulators are monolithic positive voltage regulators which feature internal current limiting and thermal shutdown. They are intended for use as fixed voltage regulators in a wide range of applications, including local on-card regulators where distribution with single point regulation is a problem.

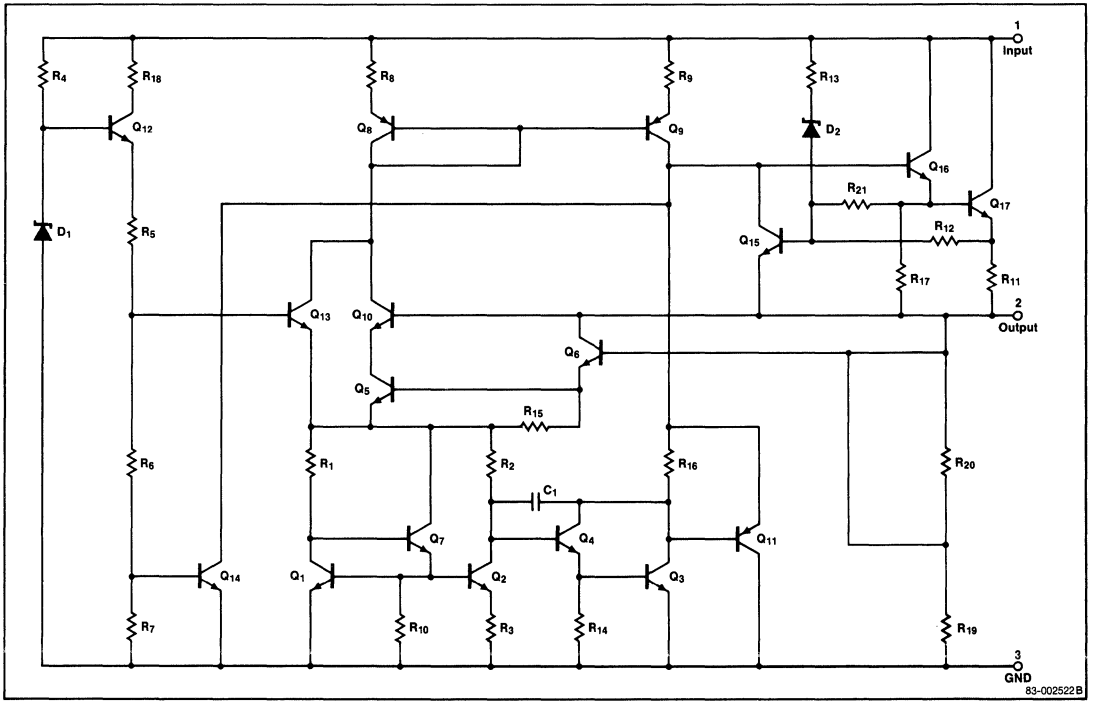
Features

- ☐ Output current in excess of 0.5 A
- ☐ No external components required
- ☐ Internal thermal overload protection
- ☐ Internal short circuit current limiting

Pin Configuration



Equivalent Circuit

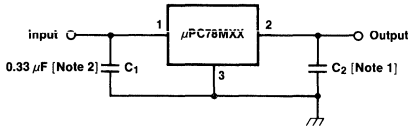


5

Ordering Information

Part Number	Package	Operating Temperature Range
μPC78M05H	Plastic SIP	−20°C to +80°C
μPC78M08H	Plastic SIP	−20°C to +80°C
μPC78M10H	Plastic SIP	−20°C to +80°C
μPC78M12H	Plastic SIP	−20°C to +80°C
μPC78M15H	Plastic SIP	−20°C to +80°C
μPC78M18H	Plastic SIP	−20°C to +80°C
μPC78M24H	Plastic SIP	−20°C to +80°C

Typical Application



Notes:
[1] Although no output capacitor is needed for stability, it does improve transient response.
[2] Required if regulator is located an appreciable distance from power supply filter.

83-002524A

Absolute Maximum Ratings

Input Voltage (μPC78M05/08/10/12/15/18)	35 V
Input Voltage (μPC78M24)	40 V
Internal Power Dissipation	Internally Limited
Operating Temperature Range	−20 to +80°C
Storage Temperature Range	−55 to +150°C
Operating Junction Temperature Range	−20 to 125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics — μPC78M05

V_{IN} = 10 V, I_O = 350 mA, 0°C ≤ T_J ≤ 125°C

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	4.8	5.0	5.2	V	T_J = 25°C
		4.75		5.25	V	7 V ≤ V_{IN} ≤ 20 V, 5 mA ≤ I_O ≤ 350 mA
Line Regulation	REG_{IN}		3	100	mV	T_J = 25°C, 7 V ≤ V_{IN} ≤ 25 V, I_O = 200 mA
			1	50	mV	T_J = 25°C, 8 V ≤ V_{IN} ≤ 25 V, I_O = 200 mA
Load Regulation	REG_L		20	100	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 500 mA
			10	50	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 200 mA
Quiescent Current	I_{BIAS}		4.5	6.0	mA	T_J = 25°C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	8 V ≤ V_{IN} ≤ 25 V, I_O = 200 mA
				0.5	mA	5 mA ≤ I_O ≤ 350 mA
Output Noise Voltage	V_N		40		μV	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	62	80		dB	T_J = 25°C, f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V, I_O = 300 mA
Dropout Voltage			2.0		V	T_A = 25°C
Short Circuit Current	I_{OSHORT}		250		mA	T_J = 25°C, V_{IN} ≤ 35 V
Peak Output Current	I_{OPEAK}		1.0		A	T_J = 25°C
Output Voltage Drift	$\Delta V_O/\Delta T$		−1.0		mV/°C	I_O = 5 mA

Electrical Characteristics — μPC78M08

V_{IN} = 14 V, I_O = 350 mA, 0°C ≤ T_J ≤ 125°C

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	7.7	8.0	8.3	V	T_J = 25°C
		7.6		8.4	V	10.5 V ≤ V_{IN} ≤ 23 V, 5 mA ≤ I_O ≤ 350 mA
Line Regulation	REG_{IN}		6.0	100	mV	T_J = 25°C, 10.5 V ≤ V_{IN} ≤ 25 V, I_O = 200 mA
			2.0	50	mV	T_J = 25°C, 11 V ≤ V_{IN} ≤ 25 V, I_O = 200 mA
Load Regulation	REG_L		25	160	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 500 mA
			10	80	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 200 mA
Quiescent Current	I_{BIAS}		4.6	6.0	mA	T_J = 25°C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	10.5 V ≤ V_{IN} ≤ 25 V, I_O = 200 mA
				0.5	mA	5 mA ≤ I_O ≤ 350 mA
Output Noise Voltage	V_N		52		μV	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	56	80		dB	T_J = 25°C, f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V, I_O = 300 mA
Dropout Voltage			2.0		V	T_A = 25°C
Short Circuit Current	I_{OSHORT}		250		mA	T_J = 25°C, V_{IN} = 35 V
Peak Output Current	I_{OPEAK}		1.0		A	T_J = 25°C
Output Voltage Drift	$\Delta V_O/\Delta T$		−1.0		mV/°C	I_O = 5 mA

Electrical Characteristics — μPC78M10

V_{IN} = 17 V, I_O = 350 mA, 0°C ≤ T_J ≤ 125°C

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	9.6	10	10.4	V	T_J = 25°C
		9.5		10.5	V	12.5 V ≤ V_{IN} ≤ 25 V, 5 mA ≤ I_O ≤ 350 mA
Line Regulation	REG_{IN}		1.0	100	mV	T_J = 25°C, 12.5 V ≤ V_{IN} ≤ 28 V, I_O = 200 mA
			2.0	50	mV	T_J = 25°C, 14 V ≤ V_{IN} ≤ 28 V, I_O = 200 mA
Load Regulation	REG_L		25	200	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 500 mA
			10	100	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 200 mA
Quiescent Current	I_{BIAS}		4.5	6.0	mA	T_J = 25°C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	12.5 V ≤ V_{IN} ≤ 28 V, I_O = 200 mA
				0.5	mA	5 mA ≤ I_O ≤ 350 mA
Output Noise Voltage	V_N		70		μV	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	55	80		dB	T_J = 25°C, f = 120 Hz, 13 V ≤ V_{IN} ≤ 23 V, I_O = 300 mA
Dropout Voltage			2.0		V	T_A = 25°C
Short Circuit Current	I_{OSHORT}		250		mA	T_J = 25°C, V_{IN} = 35 V
Peak Output Current	I_{OPEAK}		1.0		A	T_J = 25°C
Output Voltage Drift	$\Delta V_O/\Delta T$		−1.0		mV/°C	I_O = 5 mA

Electrical Characteristics — μPC78M12

V_{IN} = 19 V, I_O = 350 mA, 0°C ≤ T_J ≤ 125°C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Output Voltage	V_O	11.5	12.0	12.5	V	T_J = 25°C
		11.4		12.6	V	14.5 V ≤ V_{IN} ≤ 27 V, 5 mA ≤ I_O ≤ 350 mA
Line Regulation	REG_{IN}		8.0	100	mV	T_J = 25°C, 14.5 V ≤ V_{IN} ≤ 30 V, I_O = 200 mA
			2.0	50	mV	T_J = 25°C, 16 V ≤ V_{IN} ≤ 30 V, I_O = 200 mA
Load Regulation	REG_L		25	240	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 500 mA
			10	120	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 200 mA
Quiescent Current	I_{BIAS}		4.8	6.0	mA	T_J = 25°C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	14.5 V ≤ V_{IN} ≤ 30 V, I_O = 200 mA
				0.5	mA	5 mA ≤ I_O ≤ 350 mA
Output Noise Voltage	V_N		75		μV	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection		55	80		dB	T_J = 25°C, f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V, I_O = 300 mA
Dropout Voltage			2.0		V	T_A = 25°C
Short Circuit Current	I_{OSHORT}		250		mA	T_J = 25°C, V_{IN} = 35 V
Peak Output Current	I_{OPEAK}		1.0		A	T_J = 25°C
Output Voltage Drift	$\Delta V_O/\Delta T$		−1.0		mV/°C	I_O = 5 mA

Electrical Characteristics — μPC78M15

V_{IN} = 23 V, I_O = 350 mA, 0°C ≤ T_J ≤ 125°C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Output Voltage	V_O	14.4	15	15.6	V	T_J = 25°C
		14.25		15.75	V	17.5 V ≤ V_{IN} ≤ 30 V, 5 mA ≤ I_O ≤ 350 mA
Line Regulation	REG_{IN}		10	100	mV	T_J = 25°C, 17.5 V ≤ V_{IN} ≤ 30 V, I_O = 200 mA
			3.0	50	mV	T_J = 25°C, 20 V ≤ V_{IN} ≤ 30 V, I_O = 200 mA
Load Regulation	REG_L		25	300	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 500 mA
			10	150	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 200 mA
Quiescent Current	I_{BIAS}		4.8	6.0	mA	T_J = 25°C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	17.5 V ≤ V_{IN} ≤ 30 V, I_O = 200 mA
				0.5	mA	5 mA ≤ I_O ≤ 350 mA
Output Noise Voltage	V_N		90		μV	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	54	70		dB	T_J = 25°C, f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V, I_O = 300 mA
Dropout Voltage			2.0		V	T_A = 25°C
Short Circuit Current	I_{OSHORT}		250		mA	T_J = 25°C, V_{IN} = 35 V
Peak Output Current	I_{OPEAK}		1.0		A	T_J = 25°C
Output Voltage Drift	$\Delta V_O/\Delta T$		−1.0		mV/°C	I_O = 5 mA

Electrical Characteristics — μPC78M18

V_{IN} = 27 V, I_O = 350 mA, 0°C ≤ T_J ≤ 125°C

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	17.3	18.0	18.7	V	T_J = 25°C
		17.1		18.9	V	21 V ≤ V_{IN} ≤ 33 V, 5 mA ≤ I_O ≤ 350 mA
Line Regulation	REG_{IN}		10	100	mV	T_J = 25°C, 21 V ≤ V_{IN} ≤ 33 V, I_O = 200 mA
			4.0	50	mV	T_J = 25°C, 24 V ≤ V_{IN} ≤ 30 V
Load Regulation	REG_L		30	360	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 500 mA
			10	180	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 200 mA
Quiescent Current	I_{BIAS}		4.8	6.0	mA	T_J = 25°C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	27 V ≤ V_{IN} ≤ 38 V
				0.5	mA	5 mA ≤ I_O ≤ 350 mA
Output Noise Voltage	V_N		100		μV	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	53	70		dB	T_J = 25°C, f = 120 Hz, 22 V ≤ V_{IN} ≤ 32 V, I_O = 300 mA
Dropout Voltage			2.0		V	T_A = 25°C
Short Circuit Current	I_{OSHORT}		250		mA	T_J = 25°C, V_{IN} = 35 V
Peak Output Current	I_{OPEAK}		1.0		A	T_J = 25°C
Output Voltage Drift	$\Delta V_O/\Delta T$		−1.0		mV/°C	I_O = 5 mA

Electrical Characteristics — μPC78M24

V_{IN} = 27 V, I_O = 350 mA, 0°C ≤ T_J ≤ 125°C

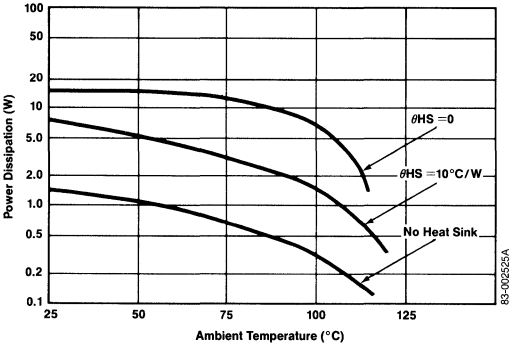
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	23	24	25	V	T_J = 25°C
		22.8		25.2	V	27 V ≤ V_{IN} ≤ 38 V, 5 mA ≤ I_O ≤ 350 mA
Line Regulation	REG_{IN}		10	100	mV	T_J = 25°C, 27 V ≤ V_{IN} ≤ 38 V, I_O = 200 mA
			5.0	50	mV	T_J = 25°C, 28 V ≤ V_{IN} ≤ 38 V
Load Regulation	REG_L		30	480	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 500 mA
			10	240	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 200 mA
Quiescent Current	I_{BIAS}		5.0	6.0	mA	T_J = 25°C
Quiescent Current Change	ΔI_{BIAS}			0.8	mA	27 V ≤ V_{IN} ≤ 38 V, I_O = 200 mA
				0.5	mA	5 mA ≤ I_O ≤ 350 mA
Output Noise Voltage	V_N		170		μV	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection		50	70		dB	T_J = 25°C, f = 120 Hz, 28 V ≤ V_{IN} ≤ 38 V, I_O = 300 mA
Dropout Voltage			2.0		V	T_A = 25°C
Short Circuit Current	I_{OSHORT}		250		mA	T_J = 25°C, V_{IN} = 35 V
Peak Output Current	I_{OPEAK}		1.0		A	T_J = 25°C
Output Voltage Drift	$\Delta V_O/\Delta T$		−1.2		mV/°C	I_O = 5 mA, 0°C ≤ T_J ≤ 125°C

5

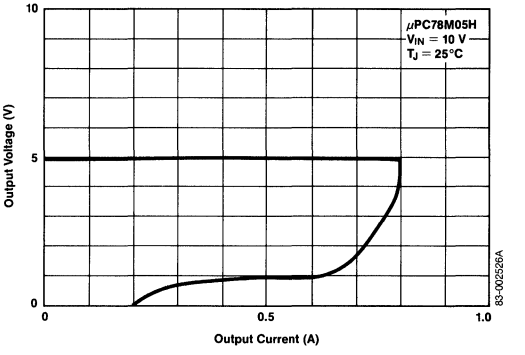
Operating Characteristics

$T_A = 25°C$

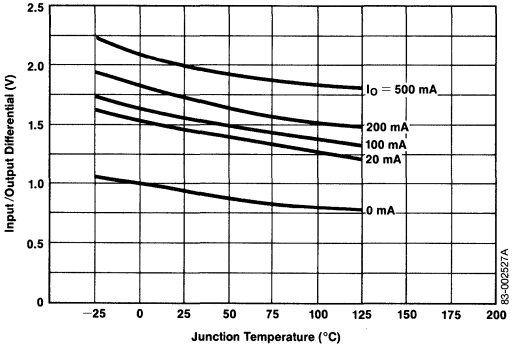
Power Dissipation vs. Ambient Temperature



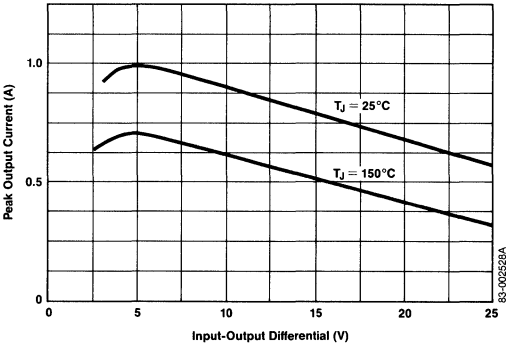
Current Limiting Characteristics



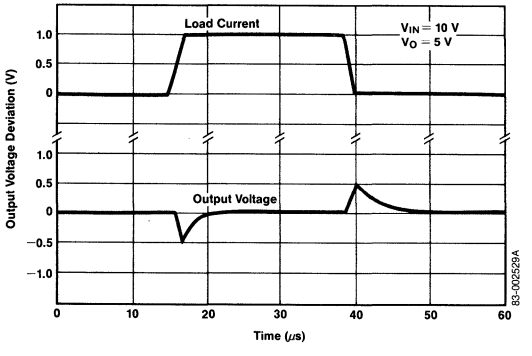
Dropout Voltage as a Function of Junction Temperature



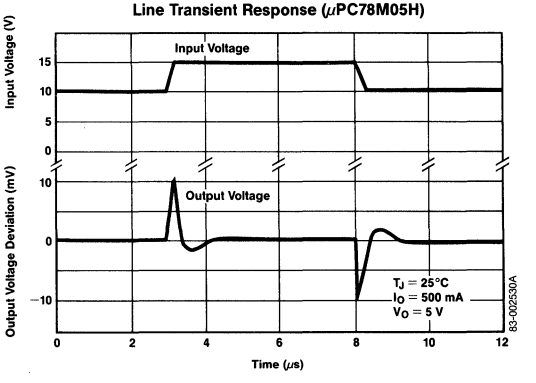
Peak Output Current as a Function of Input/Output Differential Voltage



Load Transient Response (μPC78M05H)



Line Transient Response (μPC78M05H)



NEC
NEC Electronics Inc.

μPC7800 SERIES
THREE-TERMINAL 1.0 A
POSITIVE VOLTAGE REGULATORS

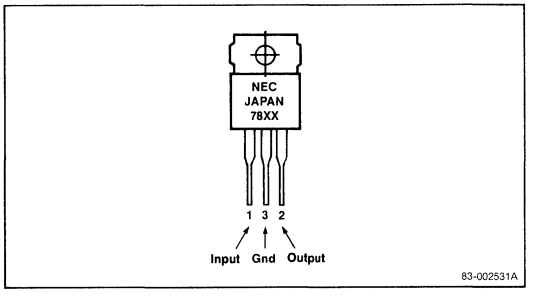
Description

The μPC7800 series of three terminal regulators are monolithic positive voltage regulators which feature internal current limiting and thermal shutdown. They are intended for use as fixed voltage regulators in a wide range of applications, including local on-card regulators where distribution with single point regulation is a problem.

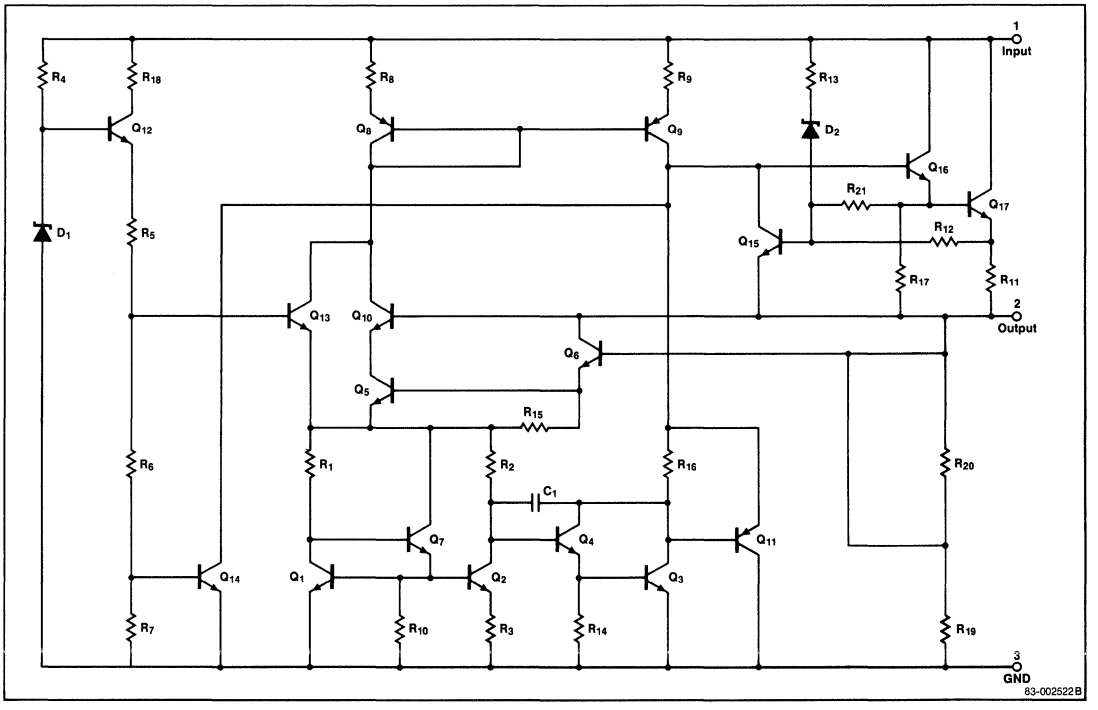
Features

- ☐ Output current in excess of 1.0 A
- ☐ No external components required
- ☐ Internal thermal overload protection
- ☐ Internal short circuit current limiting

Pin Configuration



Equivalent Circuit



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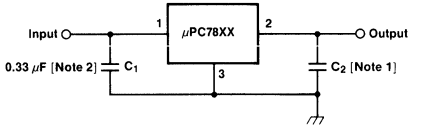
Ordering Information

Part Number	Package	Operating Temperature Range
μPC7805H	Plastic SIP	−20°C to +80°C
μPC7808H	Plastic SIP	−20°C to +80°C
μPC7812H	Plastic SIP	−20°C to +80°C
μPC7815H	Plastic SIP	−20°C to +80°C
μPC7818H	Plastic SIP	−20°C to +80°C
μPC7824H	Plastic SIP	−20°C to +80°C

Typical Application



Notes:
[1] Although no output capacitor is needed for stability, it does improve transient response.
[2] Required if regulator is located an appreciable distance from power supply filter.

83-002532A

Absolute Maximum Ratings

Input Voltage (μPC7805/08/12/15/18)	35 V
Input Voltage (μPC7824)	40 V
Internal Power Dissipation	Internally Limited
Operating Temperature Range	−20 to +80°C
Storage Temperature Range	−55 to +150°C
Operating Junction Temperature Range	−20 to 150°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics — μPC7805

V_{IN} = 10 V, I_O = 500 mA, 0°C ≤ T_J ≤ 125°C

Parameter	Symbol	Limits Min.	Limits Typ.	Limits Max.	Unit	Test Conditions
Output Voltage	V_O	4.8	5.0	5.2	V	T_J = 25°C
		4.75		5.25	V	7 V ≤ V_{IN} ≤ 20 V, 5 mA ≤ I_O ≤ 1.0 A, P_T ≤ 15 W
Line Regulation	REG_{IN}		15	100	mV	T_J = 25°C, 7 V ≤ V_{IN} ≤ 25 V
			4	50	mV	T_J = 25°C, 8 V ≤ V_{IN} ≤ 12 V
Load Regulation	REG_L		4	100	mV	T_J = 25°C, 5 mA ≤ I_O ≤ 1.5 A
			2	50	mV	T_J = 25°C, 250 mA ≤ I_O ≤ 750 mA
Quiescent Current	I_{BIAS}		5.3	8.0	mA	T_J = 25°C
Quiescent Current Change	ΔI_{BIAS}			1.3	mA	7 V ≤ V_{IN} ≤ 25 V
				0.5	mA	5 mA ≤ I_O ≤ 1.0 A
Output Noise Voltage	V_N		40	200	μV_{RMS}	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	62	69		dB	T_J = 25°C, f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V
Dropout Voltage			1.8		V	I_O = 1.0 A, T_J = 25°C
Short Circuit Current	I_{OSHORT}		1.1		A	T_J = 25°C, V_{IN} = 25 V
Peak Output Current	I_{OPEAK}	1.7	2.2	2.8	A	T_J = 25°C, V_{IN} = 10 V
Output Voltage Drift	$\Delta V_O/\Delta T$		−0.4		mV/°C	I_O = 5 mA, 0°C ≤ T_J ≤ 125°C

Electrical Characteristics — μPC7808

V_{IN} = 14 V, I_O = 500 mA, 0 °C ≤ T_J ≤ 125 °C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Output Voltage	V_O	7.7	8.0	8.3	V	T_J = 25 °C
		7.6		8.4	V	10.5 V ≤ V_{IN} ≤ 23 V, 5 mA ≤ I_O ≤ 1.0 A, P_T ≤ 15 W
Line Regulation	REG_{IN}		34	160	mV	T_J = 25 °C, 10.5 V ≤ V_{IN} ≤ 25 V
			18	80	mV	T_J = 25 °C, 11 V ≤ V_{IN} ≤ 17 V
Load Regulation	REG_L		24	160	mV	T_J = 25 °C, 5 mA ≤ I_O ≤ 1.5 A
			8	80	mV	T_J = 25 °C, 250 mA ≤ I_O ≤ 750 mA
Quiescent Current	I_{BIAS}		4.7	8.0	mA	T_J = 25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	10.5 V ≤ V_{IN} ≤ 25 V
				0.5	mA	5 mA ≤ I_O ≤ 1.0 A
Output Noise Voltage	V_N		50	250	μV_{RMS}	T_A = 25 °C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	56	63		dB	f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V
Dropout Voltage			1.8		V	I_O = 1.0 A, T_J = 25 °C
Short Circuit Current	I_{OSHORT}		1.0		A	T_J = 25 °C, V_{IN} = 25 V
Peak Output Current	I_{OPEAK}	1.7	2.3	2.8	A	T_J = 25 °C, V_{IN} = 14 V
Output Voltage Drift	$\Delta V_O/\Delta T$		0.4		mV/°C	I_O = 5 mA, 0 °C ≤ T_J ≤ 125 °C

Electrical Characteristics — μPC7812

V_{IN} = 19 V, I_O = 500 mA, 0 °C ≤ T_J ≤ 125 °C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Output Voltage	V_O	11.5	12.0	12.5	V	T_J = 25 °C
		11.4		12.6	V	14.5 V ≤ V_{IN} ≤ 27 V, 5 mA ≤ I_O ≤ 1.0 A, P_T ≤ 15 W
Line Regulation	REG_{IN}		44	240	mV	T_J = 25 °C, 14.5 V ≤ V_{IN} ≤ 30 V
			16	120	mV	T_J = 25 °C, 16 V ≤ V_{IN} ≤ 22 V
Load Regulation	REG_L		45	240	mV	T_J = 25 °C, 5 mA ≤ I_O ≤ 1.5 A
			16	120	mV	T_J = 25 °C, 250 mA ≤ I_O ≤ 750 mA
Quiescent Current	I_{BIAS}		4.7	8.0	mA	T_J = 25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	14.5 V ≤ V_{IN} ≤ 30 V
				0.5	mA	5 mA ≤ I_O ≤ 1.0 A
Output Noise Voltage	V_N		70	300	μV_{RMS}	T_A = 25 °C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	55	60		dB	f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V
Dropout Voltage			1.8		V	I_O = 1.0 A, T_J = 25 °C
Short Circuit Current	I_{OSHORT}		0.7		A	T_J = 25 °C, V_{IN} = 30 V
Peak Output Current	I_{OPEAK}	1.7	2.3	2.8	A	T_J = 25 °C, V_{IN} = 19 V
Output Voltage Drift	$\Delta V_O/\Delta T$		0.8		mV/°C	I_O = 5 mA, 0 °C ≤ T_J ≤ 125 °C

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Electrical Characteristics — μPC7815

V_{IN} = 23 V, I_O = 500 mA, 0 °C ≤ T_J ≤ 125 °C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Output Voltage	V_O	14.4	15.0	15.6	V	T_J = 25 °C
		14.25		15.75	V	17.5 V ≤ V_{IN} ≤ 30 V, 5 mA ≤ I_O ≤ 1.0 A, P_T ≤ 15 W
Line Regulation	REG_{IN}		46	300	mV	T_J = 25 °C, 17.5 V ≤ V_{IN} ≤ 30 V
			22	150	mV	T_J = 25 °C, 20 V ≤ V_{IN} ≤ 26 V
Load Regulation	REG_L		66	300	mV	T_J = 25 °C, 5 mA ≤ I_O ≤ 1.5 A
			24	150	mV	T_J = 25 °C, 250 mA ≤ I_O ≤ 750 mA
Quiescent Current	I_{BIAS}		4.7	8.0	mA	T_J = 25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	17.5 V ≤ V_{IN} ≤ 30 V
				0.5	mA	5 mA ≤ I_O ≤ 1.0 A
Output Noise Voltage	V_N		85	400	μV_{RMS}	T_A = 25 °C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	54	58		dB	f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V
Dropout Voltage			1.8		V	I_O = 1.0 A, T_J = 25 °C
Short Circuit Current	I_{OSHORT}		0.7		A	T_J = 25 °C, V_{IN} = 30 V
Peak Output Current	I_{OPEAK}	1.7	2.3	2.8	A	T_J = 25 °C, V_{IN} = 23 V
Output Voltage Drift	$\Delta V_O/\Delta T$		1.0		mV/°C	I_O = 5 mA, 0 °C ≤ T_J ≤ 125 °C

Electrical Characteristics — μPC7818

V_{IN} = 27 V, I_O = 500 mA, 0 °C ≤ T_J ≤ 125 °C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Output Voltage	V_O	17.3	18.0	18.7	V	T_J = 25 °C
		17.1		18.9	V	21 V ≤ V_{IN} ≤ 33 V, 5 mA ≤ I_O ≤ 1.0 A, P_T ≤ 15 W
Line Regulation	REG_{IN}		52	360	mV	T_J = 25 °C, 21 V ≤ V_{IN} ≤ 33 V
			26	180	mV	T_J = 25 °C, 24 V ≤ V_{IN} ≤ 30 V
Load Regulation	REG_L		100	360	mV	T_J = 25 °C, 5 mA ≤ I_O ≤ 1.5 A
			32	180	mV	T_J = 25 °C, 250 mA ≤ I_O ≤ 750 mA
Quiescent Current	I_{BIAS}		5.0	8.0	mA	T_J = 25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	21 V ≤ V_{IN} ≤ 33 V
				0.5	mA	5 mA ≤ I_O ≤ 1.0 A
Output Noise Voltage	V_N		95	450	μV_{RMS}	T_A = 25 °C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	53	56		dB	f = 120 Hz, 22 V ≤ V_{IN} ≤ 32 V
Dropout Voltage			1.8		V	I_O = 1.0 A, T_J = 25 °C
Short Circuit Current	I_{OSHORT}		0.7		A	T_J = 25 °C, V_{IN} = 33 V
Peak Output Current	I_{OPEAK}	1.7	2.3	2.8	A	T_J = 25 °C, V_{IN} = 27 V
Output Voltage Drift	$\Delta V_O/\Delta T$		1.2		mV/°C	I_O = 5 mA, 0 °C ≤ T_J ≤ 125 °C

Electrical Characteristics — μPC7824

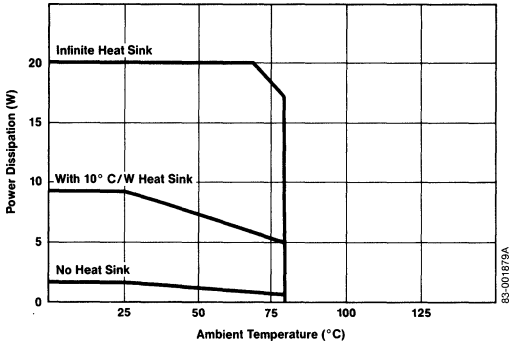
V_{IN} = 33 V, I_O = 500 mA, 0 °C ≤ T_J ≤ 125 °C

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	23.0	24.0	25.0	V	T_J = 25 °C
		22.8		25.2	V	27 V ≤ V_{IN} ≤ 38 V, 5 mA ≤ I_O ≤ 1.0 A, P_T ≤ 15 W
Line Regulation	REG_{IN}		64	480	mV	T_J = 25 °C, 27 V ≤ V_{IN} ≤ 38 V
			34	240	mV	T_J = 25 °C, 30 V ≤ V_{IN} ≤ 36 V
Load Regulation	REG_L		130	480	mV	T_J = 25 °C, 5 mA ≤ I_O ≤ 1.5 A
			44	240	mV	T_J = 25 °C, 250 mA ≤ I_O ≤ 750 mA
Quiescent Current	I_{BIAS}		5.0	8.0	mA	T_J = 25 °C
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	27 V ≤ V_{IN} ≤ 38 V
				0.5	mA	5 mA ≤ I_O ≤ 1.0 A
Output Noise Voltage	V_N		120	500	μV_{RMS}	T_A = 25 °C, 10 Hz ≤ f ≤ 100 kHz
Ripple Rejection	RR	50	54		dB	f = 120 Hz, 28 V ≤ V_{IN} ≤ 38 V
Dropout Voltage			2.0		V	I_O = 1.0 A, T_J = 25 °C
Short Circuit Current	I_{OSHORT}		0.4		A	T_J = 25 °C, V_{IN} = 38 V
Peak Output Current	I_{OPEAK}	1.7	2.4	2.8	A	T_J = 25 °C, V_{IN} = 33 V
Output Voltage Drift	$\Delta V_O/\Delta T$		1.4		mV/°C	I_O = 5 mA, 0 °C ≤ T_J ≤ 125 °C

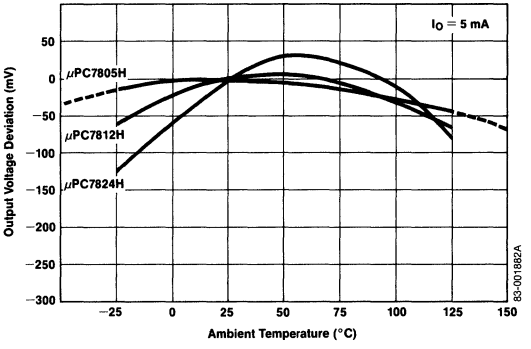
Operating Characteristics

T_A = +25 °C

Worst Case Power Dissipation vs. Ambient Temperature



Output Voltage vs. Ambient Temperature



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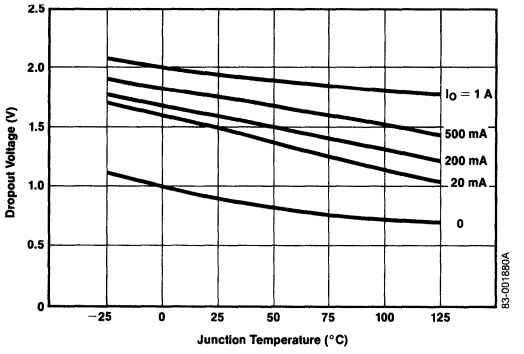
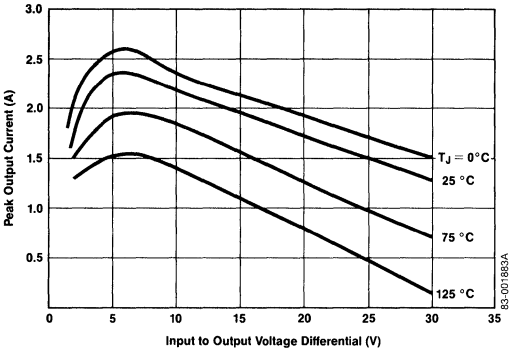
Operating Characteristics (Cont.)

$T_A = +25°C$

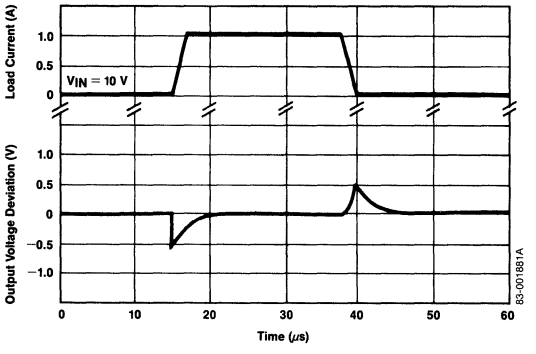
Dropout Voltage as a Function of Junction Temperature



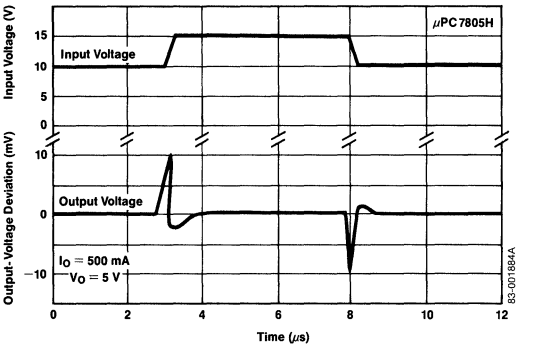
Peak Output Current as a Function of Input/Output Differential Voltage



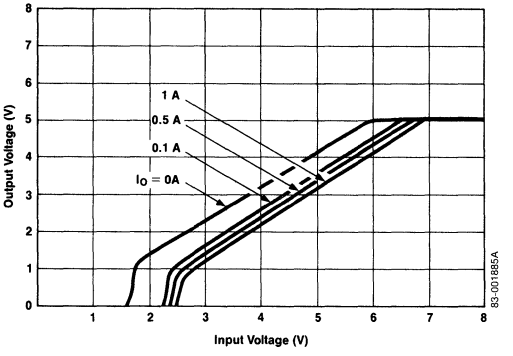
Load Transient Response (μPC7805H)



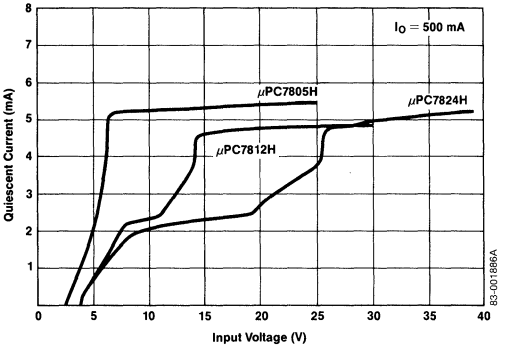
Line Transient Response



Dropout Characteristics (μPC7805H)



Quiescent Current



NEC

NEC Electronics Inc.

μPC79L00 SERIES THREE-TERMINAL 0.1 A NEGATIVE VOLTAGE REGULATORS

PRELIMINARY INFORMATION

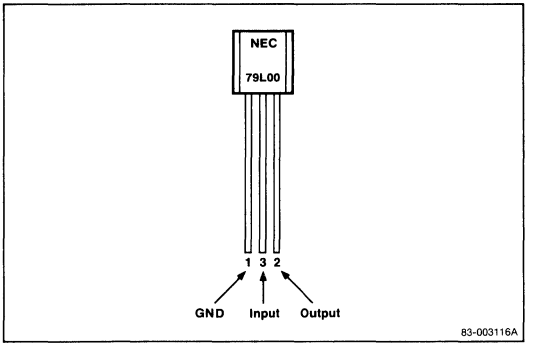
Description

The μPC79L00 series is composed of four monolithic three terminal negative voltage regulators that employ current limiting, thermal shutdown, and output transistor safe area protection. They are intended as fixed voltage regulators in a wide range of applications, including local or on-card regulation for elimination of noise and distribution problems associated with single-point regulation. The four devices in the μPC79L00 series (μPC79L05, 08, 12, and 15) have output voltage ratings of −5, −8, −12, and −15 volts, respectively.

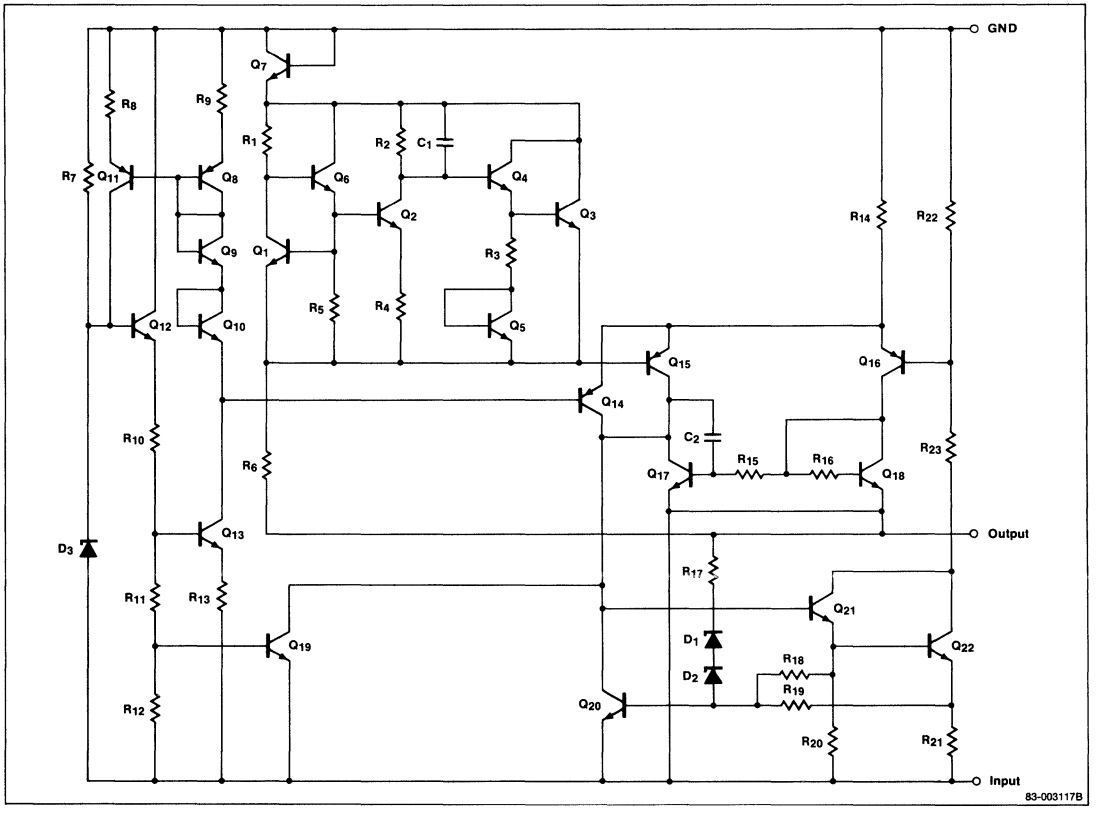
Features

- ☐ Output current up to 100 mA
- ☐ Internal thermal overload protection
- ☐ Internal short circuit current limiting
- ☐ Low noise

Pin Configuration



Equivalent Circuit



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Ordering Information

Part Number	Package	Operating Temperature Range
μPC79L05J	T092	−20 °C to +85 °C
μPC79L08J	T092	−20 °C to +85 °C
μPC79L12J	T092	−20 °C to +85 °C
μPC79L18J	T092	−20 °C to +85 °C

Recommended Operating Conditions

Parameter	Symbol	Type Number	Limits Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}	μPC79L05	−7	−10	−20	V
		μPC79L08	−10.5	−14	−23	
		μPC79L12	−14.5	−19	−27	
		μPC79L15	−17.5	−23	−30	
Output Current	I_O	All	0	40	70	mA
Operating Junction Temperature	T_J	All	−20	75	125	°C

Absolute Maximum Ratings

($T_A = 25$ °C)

Input Voltage	−30 or −35 V (Note 1)
Internal Power Dissipation	700 mW
Operating Ambient Temperature	−20 to +85 °C
Storage Temperature	−55 to +150 °C
Operating Junction Temperature Range	−20 to + 150 °C
Thermal Resistance	180 °C/W

Note:

(1) −30 V for μPC79L05, 08
−35 V for μPC79L12, 15

Comment: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics — μPC79L05

$V_{IN} = -10$ V, $I_O = 40$ mA, $0\,°C \leq T_J \leq 125\,°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	−4.8	−5.0	−5.2	V	$T_J = 25\,°C$
		−4.75		−5.25	V	$-7\,V \leq V_{IN} \leq -20\,V$, $1\,mA \leq I_O \leq 40\,mA$
Line Regulation	REG_{IN}		5	60	mV	$T_J = 25\,°C$, $-7\,V \leq V_{IN} \leq -20\,V$
Load Regulation	REG_L		10	50	mV	$T_J = 25\,°C$, $1\,mA \leq I_O \leq 100\,mA$
Quiescent Current	I_{BIAS}		4.2	6.0	mA	$T_J = 25\,°C$
Quiescent Current Change	ΔI_{BIAS}			0.5	mA	$-7\,V \leq V_{IN} \leq -20\,V$, $I_O \leq 40\,mA$
				0.1	mA	$V_{IN} = -10\,V$, $1\,mA \leq I_O \leq 40\,mA$
Output Noise Voltage	V_N		100		μV rms	$T_J = 25\,°C$, $10\,Hz \leq f \leq 100\,kHz$
Ripple Rejection	RR	50	70		dB	$f = 120\,Hz$, $-8\,V \leq V_{IN} \leq -18\,V$, $T_J = 25\,°C$
Dropout Voltage	V_{DIF}		1.1		V	$T_J = 25\,°C$
Short Circuit Current	I_{OSHORT}		120		mA	$T_J = 25\,°C$, $V_{IN} = -20\,V$
Peak Output Current	I_{OPEAK}		180		mA	$T_J = 25\,°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		0.4		mV/°C	$I_O = 5\,mA$

Electrical Characteristics — μPC79L08

$V_{IN} = -14$ V, $I_O = 40$ mA, $0°C \leq T_J \leq 125°C$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Output Voltage	V_O	−7.7	−8.0	−8.3	V	$T_J = 25°C$
		−7.6		−8.4	V	$-10.5\ V \leq V_{IN} \leq -23\ V$
Line Regulation	REG_{IN}		7	60	mV	$T_J = 25°C$, $-10.5\ V \leq V_{IN} \leq -23\ V$
Load Regulation	REG_L		12	80	mV	$T_J = 25°C$, $1\ mA \leq I_O \leq 100\ mA$
Quiescent Current	I_{BIAS}		4.2	6.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			0.5	mA	$-10.5\ V \leq V_{IN} \leq -23\ V$, $I_O \leq 40\ mA$
				0.1	mA	$V_{IN} = -14\ V$, $1\ mA \leq I_O \leq 40\ mA$
Output Noise Voltage	V_N		110		μV rms	$T_J = 25°C$, $10\ Hz \leq f \leq 100\ kHz$
Ripple Rejection	RR	50	70		dB	$f = 120\ Hz$, $-12\ V \leq V_{IN} \leq -22\ V$, $T_J = 25°C$
Dropout Voltage	V_{DIF}		1.1		V	$T_J = 25°C$
Short Circuit Current	I_{OSHORT}		85		mA	$T_J = 25°C$, $V_{IN} = -23\ V$
Peak Output Current	I_{OPEAK}		180		mA	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		0.6		mV/°C	$I_O = 5\ mA$

Electrical Characteristics — μPC79L12

$V_{IN} = -19$ V, $I_O = 40$ mA, $0°C \leq T_J \leq 125°C$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Output Voltage	V_O	−11.5	−12.0	−12.5	V	$T_J = 25°C$
		−11.4		−12.6	V	$-14\ V \leq V_{IN} \leq -27\ V$, $1\ mA \leq I_O \leq 40\ mA$
Line Regulation	REG_{IN}		9	45	mV	$T_J = 25°C$, $-14.5\ V \leq V_{IN} \leq -27\ V$
Load Regulation	REG_L		14	100	mV	$T_J = 25°C$, $1\ mA \leq I_O \leq 100\ mA$
Quiescent Current	I_{BIAS}		4.2	6.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			0.5	mA	$-14.5\ V \leq V_{IN} \leq -30\ V$, $I_O \leq 40\ mA$
				0.1	mA	$V_{IN} = -19\ V$, $1\ mA \leq I_O \leq 40\ mA$
Output Noise Voltage	V_N		140		μV rms	$T_J = 25°C$, $10\ Hz \leq f \leq 100\ kHz$
Ripple Rejection	RR	52	70		dB	$f = 120\ Hz$, $-15\ V \leq V_{IN} \leq -25\ V$, $T_J = 25°C$
Dropout Voltage	V_{DIF}		1.1		V	$T_J = 25°C$
Short Circuit Current	I_{OSHORT}		40		mA	$T_J = 25°C$, $V_{IN} = -27\ V$
Peak Output Current	I_{OPEAK}		180		mA	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		0.8		mV/°C	$I_O = 5\ mA$

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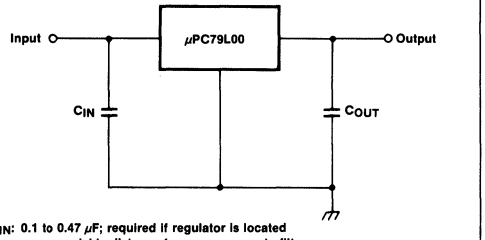
Electrical Characteristics — μPC79L15

$V_{IN} = -23$ V, $I_O = 40$ mA, $0°C \leq T_J \leq 125°C$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
Output Voltage	V_O	−14.4	−15.0	−15.6	V	$T_J = 25°C$
		−14.25		−15.75	V	$-17.5\ V \leq V_{IN} \leq -30\ V$, $1\ mA \leq I_O \leq 40\ mA$
Line Regulation	REG_{IN}		10	45	mV	$T_J = 25°C$, $-17.5\ V \leq V_{IN} \leq -30\ V$
Load Regulation	REG_L		15	125	mV	$T_J = 25°C$, $1\ mA \leq I_O \leq 100\ mA$
Quiescent Current	I_{BIAS}		4.2	6.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			0.5	mA	$-17.5\ V \leq V_{IN} \leq -30\ V$, $I_O \leq 40\ mA$
				0.1	mA	$V_{IN} = -23\ V$, $1\ mA \leq I_O \leq 40\ mA$
Output Noise Voltage	V_N		180		μV rms	$T_I = 25°C$, $10\ Hz \leq f \leq 100\ kHz$
Ripple Rejection	RR	50	67		dB	$f = 120\ Hz$, $-18.5\ V \leq V_{IN} \leq -28.5\ V$, $T_J = 25°C$
Dropout Voltage	V_{DIF}		1.1		V	$T_J = 25°C$
Short Circuit Current	I_{OSHORT}		5		mA	$T_J = 25°C$, $V_{IN} = -30\ V$
Peak Output Current	I_{OPEAK}		180		mA	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		1.0		mV/°C	$I_O = 5\ mA$

Typical Connection



C_{IN}: 0.1 to 0.47 μF; required if regulator is located an appreciable distance from power supply filter.

C_{OUT}: ≥ 0.22 μF [recommended mylar capacitor].

83-003118A

NEC
NEC Electronics Inc.

μPC79M00 SERIES THREE-TERMINAL 0.5 A NEGATIVE VOLTAGE REGULATORS

PRELIMINARY INFORMATION

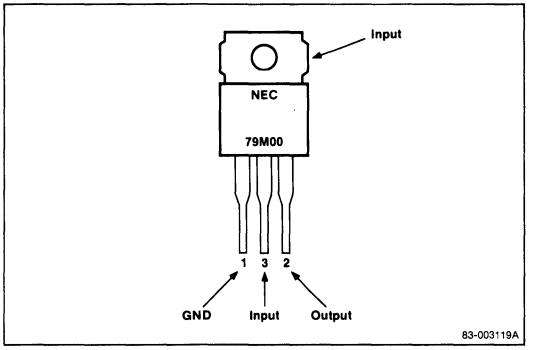
Description

The μPC79M00 series is comprised of five monolithic three terminal negative voltage regulators that employ current limiting, thermal shutdown, and output transistor safe area protection. They are intended as fixed voltage regulators in a wide range of applications, including local or on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Five output voltages are available: −5, −8, −12, −15, and −24 volts.

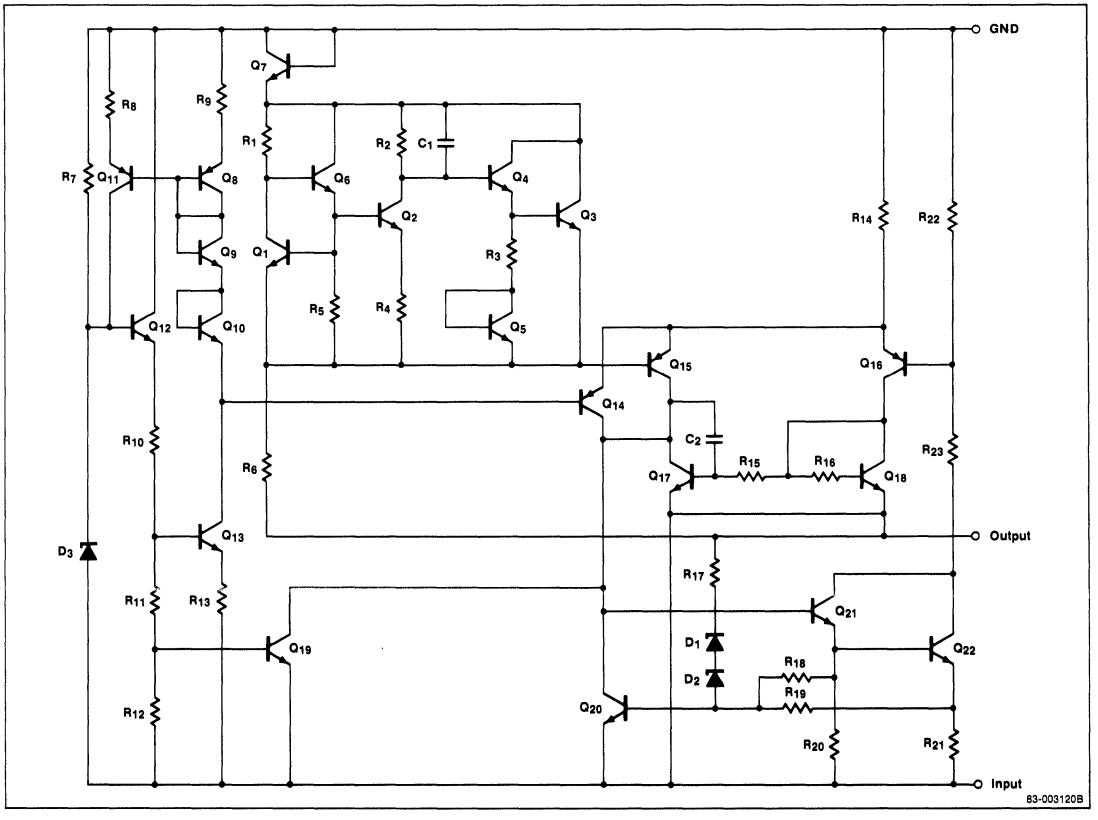
Features

- ☐ Output current up to 500 mA
- ☐ Internal thermal overload protection
- ☐ Internal short circuit current limiting
- ☐ Low noise

Pin Configuration



Equivalent Circuit



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Ordering Information

Part Number	Package	Operating Temperature Range
μPC79M05H	SIP	−20 °C to +85 °C
μPC79M08H	SIP	−20 °C to +85 °C
μPC79M12H	SIP	−20 °C to +85 °C
μPC79M15H	SIP	−20 °C to +85 °C
μPC79M18H	SIP	−20 °C to +85 °C

Recommended Operating Conditions

Parameter	Symbol	Type Number	Limits Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}	μPC79M05	−7	−10	−25	V
		μPC79M08	−10.5	−14	−25	
		μPC79M12	−14.5	−19	−30	
		μPC79M15	−17.5	−23	−30	
		μPC79M24	−27	−33	−38	
Output Current	I_O	All	5		350	mA
Operating Junction Temperature	T_J	All	−20		125	°C

Absolute Maximum Ratings

(T_A = 25 °C)

Input Voltage	−35 V
Internal Power Dissipation	20 W (Note 1)
Operating Ambient Temperature	−20 to +85 °C
Storage Temperature	−55 to +150 °C
Junction to Case Thermal Resistance	4.0 °C/W
Junction to Air Thermal Resistance	83 °C/W

Note: (1) Output automatically turns off if $T_J > 150$ °C.

Comment: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics — μPC79M05

V_{IN} = −10 V, I_O = 350 mA, 0 °C ≤ T_J ≤ 125 °C

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	−4.8		−5.2	V	T_J = 25 °C
		−4.75		−5.25	V	−7 V ≤ V_{IN} ≤ −25 V, 5 mA ≤ I_O ≤ 350 mA
Line Regulation	REG_{IN}		7.0	50	mV	T_J = 25 °C, −7 V ≤ V_{IN} ≤ −25 V
			3.0	30	mV	T_J = 25 °C, −8 V ≤ V_{IN} ≤ −18 V
Load Regulation	REG_L		30	100	mV	T_J = 25 °C, 5 mA ≤ I_O ≤ 500 mA
			20		mV	T_J = 25 °C, 5 mA ≤ I_O ≤ 350 mA
Quiescent Current	I_{BIAS}		4.2	6.0	mA	T_J = 25 °C
Quiescent Current Change	ΔI_{BIAS}			0.5	mA	−8 V ≤ V_{IN} ≤ −25 mA
				0.4	mA	5 mA ≤ I_O ≤ 350 mA
Output Noise Voltage	V_N		100	200	μV rms	T_J = 25 °C, f = 10 Hz to 100 kHz
Ripple Rejection	RR	54	60		dB	T_J = 25 °C, −8 V ≤ V_{IN} ≤ −18 V, f = 120 Hz, I_O = 300 mA
		50			dB	I_O = 100 mA
Dropout Voltage	V_{DIF}		1.1		V	T_J = 25 °C
Short Circuit Current	I_{OSHORT}		400		mA	T_J = 25 °C, V_{IN} = −25 V
Peak Output Current	I_{OPEAK}	620	800	1020	mA	T_J = 25 °C
Output Voltage Drift	$\Delta V_O/\Delta T$		0.4		mV/°C	I_O = 5 mA

Electrical Characteristics — μPC79M08

$V_{IN} = -14$ V, $I_O = 350$ mA, $0°C \leq T_J \leq 125°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	−7.7	−8.0	−8.3	V	$T_J = 25°C$
		−7.6		−8.4	V	$-10.5\ V \leq V_{IN} \leq -25\ V$, $5\ mA \leq I_O \leq 350\ mA$
Line Regulation	REG_{IN}		8.0	80	mV	$T_J = 25°C$, $-10.5\ V \leq V_{IN} \leq -25\ V$
			4.0	50	mV	$T_J = 25°C$, $-11\ V \leq V_{IN} \leq -21\ V$
Load Regulation	REG_L		30	160	mV	$T_J = 25°C$, $5\ mA \leq I_O \leq 500\ mA$
			20		mV	$T_J = 25°C$, $5\ mA \leq I_O \leq 350\ mA$
Quiescent Current	I_{BIAS}		4.2	6.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			0.5	mA	$-10.5\ V \leq V_{IN} \leq -25$ mA
				0.4	mA	$5\ mA \leq I_O \leq 350\ mA$
Output Noise Voltage	V_N		110	220	μV rms	$T_J = 25°C$, f = 10 Hz to 100 kHz
Ripple Rejection	RR	54	60		dB	$T_J = 25°C$, $-11\ V \leq V_{IN} \leq -21.5\ V$, f = 120 Hz; $I_O = 300$ mA
		50			dB	$I_O = 100$ mA
Dropout Voltage	V_{DIF}		1.1		V	$T_J = 25°C$
Short Circuit Current	I_{OSHORT}		400		mA	$T_J = 25°C$, $V_{IN} = -25$ V
Peak Output Current	I_{OPEAK}	620	800	1020	mA	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		0.6		mV/°C	$I_O = 5$ mA

Electrical Characteristics — μPC79M12

$V_{IN} = -19$ V, $I_O = 350$ mA, $0°C \leq T_J \leq 125°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	−11.5	−12.0	−12.5	V	$T_J = 25°C$
		−11.4		−12.6	V	$-14\ V \leq V_{IN} \leq -30\ V$, $5\ mA \leq I_O \leq 350\ mA$
Line Regulation	REG_{IN}		9.0	80	mV	$T_J = 25°C$, $-14.5\ V \leq V_{IN} \leq -30\ V$
			5.0	50	mV	$T_J = 25°C$, $-15\ V \leq V_{IN} \leq -25\ V$
Load Regulation	REG_L		30	240	mV	$T_J = 25°C$, $5\ mA \leq I_O \leq 500\ mA$
			20		mV	$T_J = 25°C$, $5\ mA \leq I_O \leq 350\ mA$
Quiescent Current	I_{BIAS}		4.2	6.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			0.5	mA	$-14.5\ V \leq V_{IN} \leq -30$ mA
				0.4	mA	$5\ mA \leq I_O \leq 350\ mA$
Output Noise Voltage	V_N		140	280	μV rms	$T_J = 25°C$, f = 10 Hz to 100 kHz
Ripple Rejection	RR	54	60		dB	$T_J = 25°C$, $-15\ V \leq V_{IN} \leq -25\ V$, f = 120 Hz; $I_O = 300$ mA
		50			dB	$I_O = 100$ mA
Dropout Voltage	V_{DIF}		1.1		V	$T_J = 25°C$
Short Circuit Current	I_{OSHORT}		200		mA	$T_J = 25°C$, $V_{IN} = -30$ V
Peak Output Current	I_{OPEAK}	620	800	1020	mA	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		0.8		mV/°C	$I_O = 5$ mA

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Electrical Characteristics — μPC79M15

$V_{IN} = -23$ V, $I_O = 350$ mA, $0°C \leq T_J \leq 125°C$

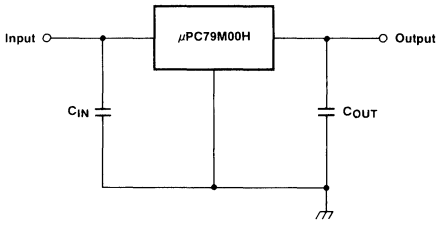
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	−14.4	−15.0	−15.6	V	$T_J = 25°C$
		−14.25		−15.75	V	$-17.5\ V \leq V_{IN} \leq -30\ V$, $5\ mA \leq I_O \leq 350\ mA$
Line Regulation	REG_{IN}		9.0	80	mV	$T_J = 25°C$, $-17.5\ V \leq V_{IN} \leq -30\ V$
			7.0	50	mV	$T_J = 25°C$, $-18\ V \leq V_{IN} \leq -28\ V$
Load Regulation	REG_L		30	240	mV	$T_J = 25°C$, $5\ mA \leq I_O \leq 500\ mA$
			20		mV	$T_J = 25°C$, $5\ mA \leq I_O \leq 350\ mA$
Quiescent Current	I_{BIAS}		4.2	6.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			0.5	mA	$-17.5\ V \leq V_{IN} \leq -30$ mA
				0.4	mA	$5\ mA \leq I_O \leq 350\ mA$
Output Noise Voltage	V_N		180	360	μV rms	$T_J = 25°C$, f = 10 Hz to 100 kHz
Ripple Rejection	RR	54	60		dB	$T_J = 25°C$, $I_O = 300$ mA
		50			dB	$-18.5\ V \leq V_{IN} \leq -28.5\ V$, f = 120 Hz, $I_O = 100$ mA
Dropout Voltage	V_{DIF}		1.1		V	$T_J = 25°C$
Short Circuit Current	I_{OSHORT}		200		mA	$T_J = 25°C$, $V_{IN} = -30$ V
Peak Output Current	I_{OPEAK}	620	800	1020	mA	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		1.0		mV/°C	$I_O = 5$ mA

Electrical Characteristics — μPC79M24

$V_{IN} = -33$ V, $I_O = 350$ mA, $0°C \leq T_J \leq 125°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	−23.0	−24.0	−25.0	V	$T_J = 25°C$
		−22.8		−25.2	V	$-27\ V \leq V_{IN} \leq -38\ V$, $5\ mA \leq I_O \leq 350\ mA$
Line Regulation	REG_{IN}		9.0	80	mV	$T_J = 25°C$, $-27\ V \leq V_{IN} \leq -38\ V$
			5.0	50	mV	$T_J = 25°C$, $-30\ V \leq V_{IN} \leq -36\ V$
Load Regulation	REG_L		30	360	mV	$T_J = 25°C$, $5\ mA \leq I_O \leq 500\ mA$
			20		mV	$T_J = 25°C$, $5\ mA \leq I_O \leq 350\ mA$
Quiescent Current	I_{BIAS}		4.2	6.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			0.5	mA	$-27\ V \leq V_{IN} \leq -38$ mA
				0.4	mA	$5\ mA \leq I_O \leq 350\ mA$
Output Noise Voltage	V_N		300	600	μV rms	$T_J = 25°C$, f = 10 Hz to 100 kHz
Ripple Rejection	RR	54	59		dB	$T_J = 25°C$, $I_O = 300$ mA
		50			dB	$-28\ V \leq V_{IN} \leq -38\ V$, f = 120 Hz, $I_O = 100$ mA
Dropout Voltage	V_{DIF}		1.1		V	$T_J = 25°C$
Short Circuit Current	I_{OSHORT}		10		mA	$T_J = 25°C$, $V_{IN} = -38$ V
Peak Output Current	I_{OPEAK}	620	800	1020	mA	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		1.4		mV/°C	$I_O = 5$ mA

Typical Connection



C_{IN}: 0.1 to 0.47 μF; required if regulator is located an appreciable distance from power supply filter.

C_{OUT}: ≥ 0.22 μF [recommended mylar capacitor].

83-003121A

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μPC7900 SERIES
THREE-TERMINAL 1.0 A
NEGATIVE VOLTAGE REGULATORS

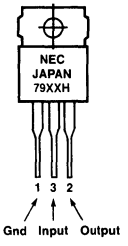
Description

The μPC7900 series of three terminal regulators are monolithic negative voltage regulators which feature internal current limiting and thermal shutdown. They are intended for use as fixed voltage regulators in a wide range of applications, including local on-card regulators where distribution with single point regulation is a problem.

Features

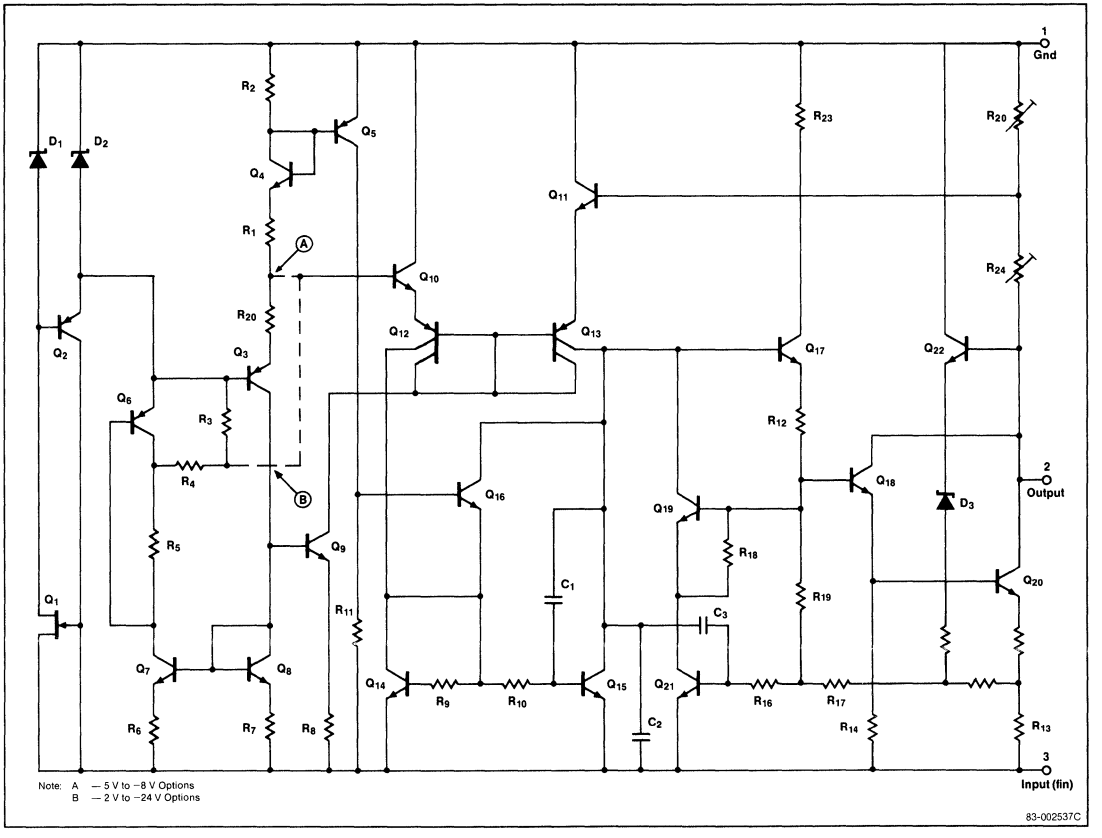
- ☐ Output current in excess of 1.0 A
- ☐ No external components required
- ☐ Internal thermal overload protection
- ☐ Internal short circuit current limiting

Pin Configuration



83-002523A

Equivalent Circuit



Note: A — 5 V to −8 V Options
B — 2 V to −24 V Options

83-002537C

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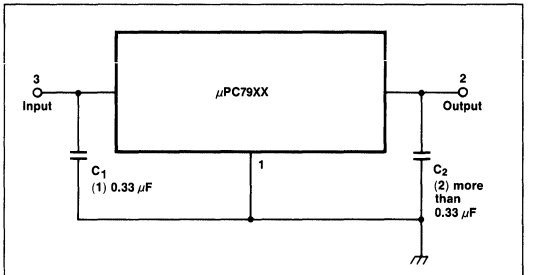
Ordering Information

Part Number	Package	Operating Temperature Range
μPC7905H	Plastic SIP	−20°C to +80°C
μPC7908H	Plastic SIP	−20°C to +80°C
μPC7912H	Plastic SIP	−20°C to +80°C
μPC7915H	Plastic SIP	−20°C to +80°C
μPC7918H	Plastic SIP	−20°C to +80°C
μPC7924H	Plastic SIP	−20°C to +80°C

Typical Application



Notes: (1) Mylar film type capacitors are recommended.
(2) Required if regulator is located an appreciable distance from power supply filter.

83-002539A

Absolute Maximum Ratings

Input Voltage (μPC7905/08/12/15/18)	−35 V
Input Voltage (μPC7924)	−40 V
Internal Power Dissipation	Internally Limited
Operating Temperature Range	−20 to +80°C
Storage Temperature Range	−55 to +150°C
Operating Junction Temperature Range	−20 to 125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics — μPC7905

$V_{IN} = -10$ V, $I_O = -500$ mA, $0°C \leq T_J \leq 125°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	−4.8	−5.0	−5.2	V	$T_J = 25°C$
		−4.75		−5.25	V	$-7\ V \leq V_{IN} \leq -20\ V$, $-5\ mA \leq I_O \leq -1.0\ A$, $P_T \leq 15\ W$
Line Regulation	REG_{IN}		3	100	mV	$T_J = 25°C$, $-7\ V \leq V_{IN} \leq -25\ V$
			1	50	mV	$T_J = 25°C$, $-8\ V \leq V_{IN} \leq -12\ V$
Load Regulation	REG_L		70	150	mV	$T_J = 25°C$, $-5\ mA \leq I_O \leq -1.5\ A$
			20	80	mV	$T_J = 25°C$, $-250\ mA \leq I_O \leq -750\ mA$
Quiescent Current	I_{BIAS}		1.0	2.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			1.3	mA	$-7\ V \leq V_{IN} \leq -25\ V$
				0.5	mA	$-5\ mA \leq I_O \leq -1.0\ A$
Output Noise Voltage	V_N		100		μV_{RMS}	$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$
Ripple Rejection	RR	54	62		dB	$f = 120\ Hz$, $-8\ V \leq V_{IN} \leq -18\ V$, $I_O = -500\ mA$
Dropout Voltage			1.1		V	$I_O = -1.0\ A$, $T_J = 25°C$
Peak Output Current	I_{OPEAK}		−2.1		A	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		−0.4		mV/°C	$I_O = -5\ mA$, $0°C \leq T_J \leq 125°C$

Electrical Characteristics — μPC7908

$V_{IN} = -14$ V, $I_O = -500$ mA, $0°C \leq T_J \leq 125°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	−7.7	−8.0	−8.3	V	$T_J = 25°C$
		−7.6		−8.4	V	$-10.5\ V \leq V_{IN} \leq -23\ V$, $-5\ mA \leq I_O \leq -1.0\ A$, $P_T \leq 15\ W$
Line Regulation	REG_{IN}		6.0	160	mV	$T_J = 25°C$, $-10.5\ V \leq V_{IN} \leq -25\ V$
			2.0	80	mV	$T_J = 25°C$, $-11\ V \leq V_{IN} \leq -17\ V$
Load Regulation	REG_L		80	200	mV	$T_J = 25°C$, $-5\ mA \leq I_O \leq -1.5\ A$
			30	100	mV	$T_J = 25°C$, $-250\ mA \leq I_O \leq -750\ mA$
Quiescent Current	I_{BIAS}		1.0	2.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	$-10.5\ V \leq V_{IN} \leq -25\ V$
				0.5	mA	$-5\ mA \leq I_O \leq -1.0\ A$
Output Noise Voltage	V_N		200		μV_{RMS}	$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$
Ripple Rejection	RR	54	62		dB	$f = 120\ Hz$, $-11.5\ V \leq V_{IN} \leq -21.5\ V$, $I_O = -500\ mA$
Dropout Voltage			1.1		V	$I_O = -1.0\ A$, $T_J = 25°C$
Peak Output Current	I_{OPEAK}		−2.1		A	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		−0.6		mV/°C	$I_O = -5\ mA$, $0°C \leq T_J \leq 125°C$

Electrical Characteristics — μPC7912

$V_{IN} = -19$ V, $I_O = -500$ mA, $0°C \leq T_J \leq 125°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	−11.5	−12.0	−12.5	V	$T_J = 25°C$
		−11.4		−12.6	V	$-14\ V \leq V_{IN} \leq -27\ V$, $-5\ mA \leq I_O \leq -1.0\ A$, $P_T \leq 15\ W$
Line Regulation	REG_{IN}		10	240	mV	$T_J = 25°C$, $-14.5\ V \leq V_{IN} \leq -30\ V$
			3.0	120	mV	$T_J = 25°C$, $-16\ V \leq V_{IN} \leq -22\ V$
Load Regulation	REG_L		85	240	mV	$T_J = 25°C$, $-5\ mA \leq I_O \leq -1.5\ A$
			30	120	mV	$T_J = 25°C$, $-250\ mA \leq I_O \leq -750\ mA$
Quiescent Current	I_{BIAS}		1.5	3.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	$-14.5\ V \leq V_{IN} \leq -30\ V$
				0.5	mA	$-5\ mA \leq I_O \leq -1.0\ A$
Output Noise Voltage	V_N		300		μV_{RMS}	$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$
Ripple Rejection	RR	54	62		dB	$f = 120\ Hz$, $-15\ V \leq V_{IN} \leq -25\ V$, $I_O = -500\ mA$
Dropout Voltage			1.1		V	$I_O = -1.0\ A$, $T_J = 25°C$
Peak Output Current	I_{OPEAK}		−2.1		A	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		0.8		mV/°C	$I_O = -5\ mA$, $0°C \leq T_J \leq 125°C$

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Electrical Characteristics — μPC7915

$V_{IN} = -23$ V, $I_O = -500$ mA, $0°C \leq T_J \leq 125°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	−14.4	−15.0	−15.6	V	$T_J = 25°C$
		−14.25		−15.75	V	$-17.5\ V \leq V_{IN} \leq -30\ V$, $-5\ mA \leq I_O \leq -1.0\ A$, $P_T \leq 15\ W$
Line Regulation	REG_{IN}		11	300	mV	$T_J = 25°C$, $-17.5\ V \leq V_{IN} \leq -30\ V$
			3.0	150	mV	$T_J = 25°C$, $-20\ V \leq V_{IN} \leq -26\ V$
Load Regulation	REG_L		90	300	mV	$T_J = 25°C$, $-5\ mA \leq I_O \leq -1.5\ A$
			30	150	mV	$T_J = 25°C$, $-250\ mA \leq I_O \leq -750\ mA$
Quiescent Current	I_{BIAS}		1.5	3.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	$-17.5\ V \leq V_{IN} \leq -30\ V$
				0.5	mA	$-5\ mA \leq I_O \leq -1.0\ A$
Output Noise Voltage	V_N		375		μV_{RMS}	$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$
Ripple Rejection	RR	54	60		dB	$f = 120\ Hz$, $-18.5\ V \leq V_{IN} \leq -28.5\ V$, $I_O = -500\ mA$
Dropout Voltage			1.1		V	$I_O = -1.0\ A$, $T_J = 25°C$
Peak Output Current	I_{OPEAK}		−2.1		A	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		−1.0		mV/°C	$I_O = -5\ mA$, $0°C \leq T_J \leq 125°C$

Electrical Characteristics — μPC7918

$V_{IN} = -27$ V, $I_O = -500$ mA, $0°C \leq T_J \leq 125°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	−17.3	−18.0	−18.7	V	$T_J = 25°C$
		−17.1		−18.9	V	$-21\ V \leq V_{IN} \leq -33\ V$, $-5\ mA \leq I_O \leq -1.0\ A$, $P_T \leq 15\ W$
Line Regulation	REG_{IN}		15	360	mV	$T_J = 25°C$, $-21\ V \leq V_{IN} \leq -33\ V$
			5.0	180	mV	$T_J = 25°C$, $-24\ V \leq V_{IN} \leq -30\ V$
Load Regulation	REG_L		90	360	mV	$T_J = 25°C$, $-5\ mA \leq I_O \leq -1.5\ A$
			30	180	mV	$T_J = 25°C$, $-250\ mA \leq I_O \leq -750\ mA$
Quiescent Current	I_{BIAS}		1.5	3.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	$-21\ V \leq V_{IN} \leq -33\ V$
				0.5	mA	$-5\ mA \leq I_O \leq -1.0\ A$
Output Noise Voltage	V_N		450		μV_{RMS}	$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$
Ripple Rejection	RR	54	60		dB	$f = 120\ Hz$, $-22\ V \leq V_{IN} \leq -32\ V$, $I_O = -500\ mA$
Dropout Voltage			1.1		V	$I_O = -1.0\ A$, $T_J = 25°C$
Peak Output Current	I_{OPEAK}		−2.1		A	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		−1.0		mV/°C	$I_O = -5\ mA$, $0°C \leq T_J \leq 125°C$

Electrical Characteristics — μPC7924

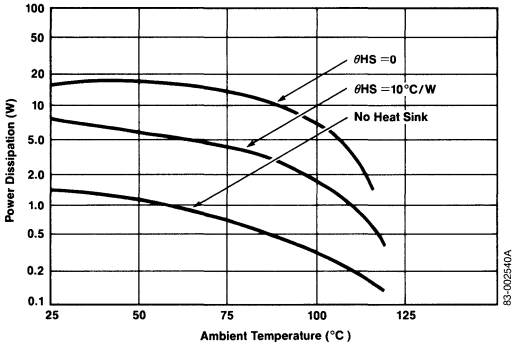
$V_{IN} = -33$ V, $I_O = -500$ mA, $0°C \leq T_J \leq 125°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	−23.0	−24.0	−25.0	V	$T_J = 25°C$
		−22.8		−25.2	V	$-27\ V \leq V_{IN} \leq -38\ V$, $-5\ mA \leq I_O \leq -1.0\ A$
Line Regulation	REG_{IN}		18	480	mV	$T_J = 25°C$, $-27\ V \leq V_{IN} \leq -38\ V$
			6	240	mV	$T_J = 25°C$, $-30\ V \leq V_{IN} \leq -36\ V$
Load Regulation	REG_L		90	480	mV	$T_J = 25°C$, $-5\ mA \leq I_O \leq -1.5\ A$
			30	240	mV	$T_J = 25°C$, $-250\ mA \leq I_O \leq -750\ mA$
Quiescent Current	I_{BIAS}		1.5	3.0	mA	$T_J = 25°C$
Quiescent Current Change	ΔI_{BIAS}			1.0	mA	$-27\ V \leq V_{IN} \leq -38\ V$
				0.5	mA	$-5\ mA \leq I_O \leq -1.0\ A$
Output Noise Voltage	V_N		600		μV_{RMS}	$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$
Ripple Rejection	RR	51	59		dB	$f = 120\ Hz$, $-28\ V \leq V_{IN} \leq -38\ V$, $I_O = -500\ mA$
Dropout Voltage			1.1		V	$I_O = -1.0\ A$, $T_J = 25°C$
Peak Output Current	I_{OPEAK}		−2.1		A	$T_J = 25°C$
Output Voltage Drift	$\Delta V_O/\Delta T$		−1.0		mV/°C	$I_O = -5\ mA$, $0°C \leq T_J \leq 125°C$

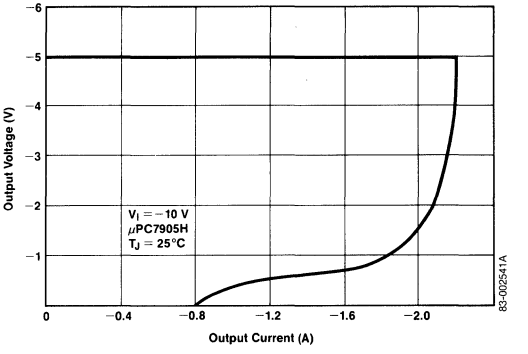
Operating Characteristics

$T_A = 25°C$

Power Dissipation vs. Ambient Temperature



Current Limiting Characteristics

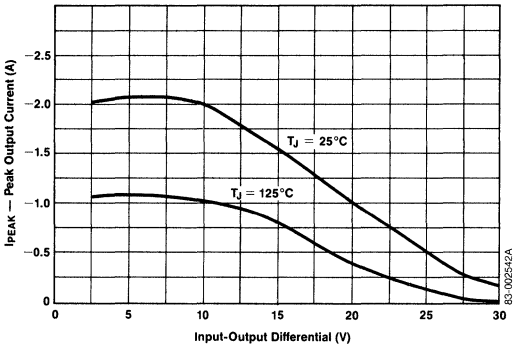


5

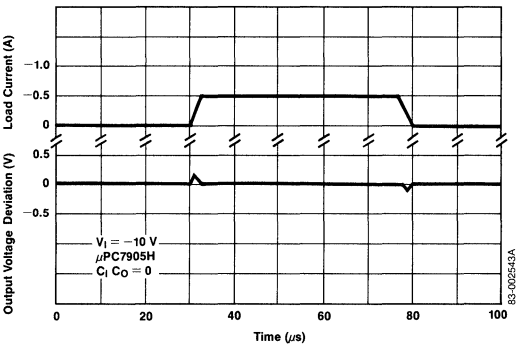
Operating Characteristics (Cont.)

$T_A = 25°C$

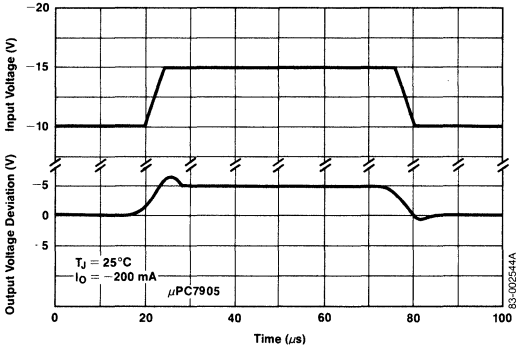
Peak Output Current as a Function of Input/Output Differential Voltage



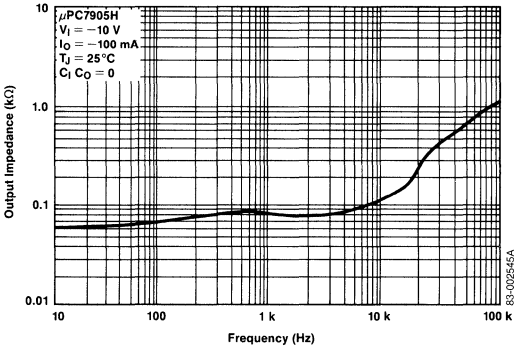
Load Transient Response



Line Transient Response



Output Impedance as a Function of Frequency



D/A AND A/D CONVERTERS

Section 6 — D/A and A/D Converters

NEC
NEC Electronics Inc.

μPC603
6-BIT HIGH-PERFORMANCE D/A CONVERTER

Description

The μPC603 is a monolithic digital-to-analog converter designed to convert 6-bit binary coded decimal signals to an analog output voltage signal. The reference voltage, weighted current source, current switch, and output op-amp, are all integrated on board the device.

Features

- ☐ Linearity error: 0.4% (1/4 LSB of 6-bit) max
- ☐ Response speed: 3 μs max
- ☐ Temperature coefficient at full speed: 160 ppm/°C max
- ☐ Input level TTL, DTL level, active low
- ☐ The output voltage range can be applied to any of the 3 following ranges: 0 to 10 V, −5 to +5 V, −10 to +10 V
- ☐ Built-in output short-circuit protection
- ☐ Possesses a linearity equivalent to that of a 7-bit converter, and can be used as a 7-bit D/A converter by the addition of external circuits
- ☐ Pin-for-pin compatible with PMI's "DAC-01C"

Ordering Information

Part Number	Package	Operating Temperature Range
μPC603D	Ceramic DIP	−20°C to +80°C

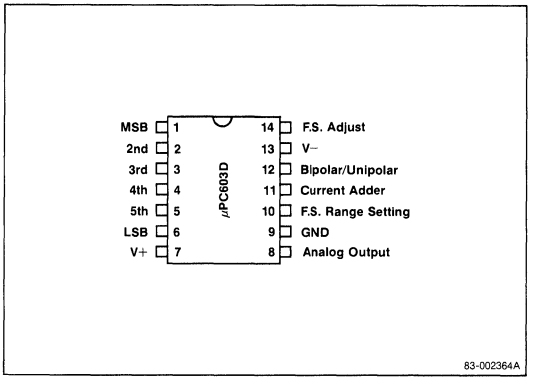
Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	±18 V
Power Dissipation	500 mW
Input Voltage	−0.7 to +6 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−20 to +80°C
Storage Temperature Range	−55 to +150°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration

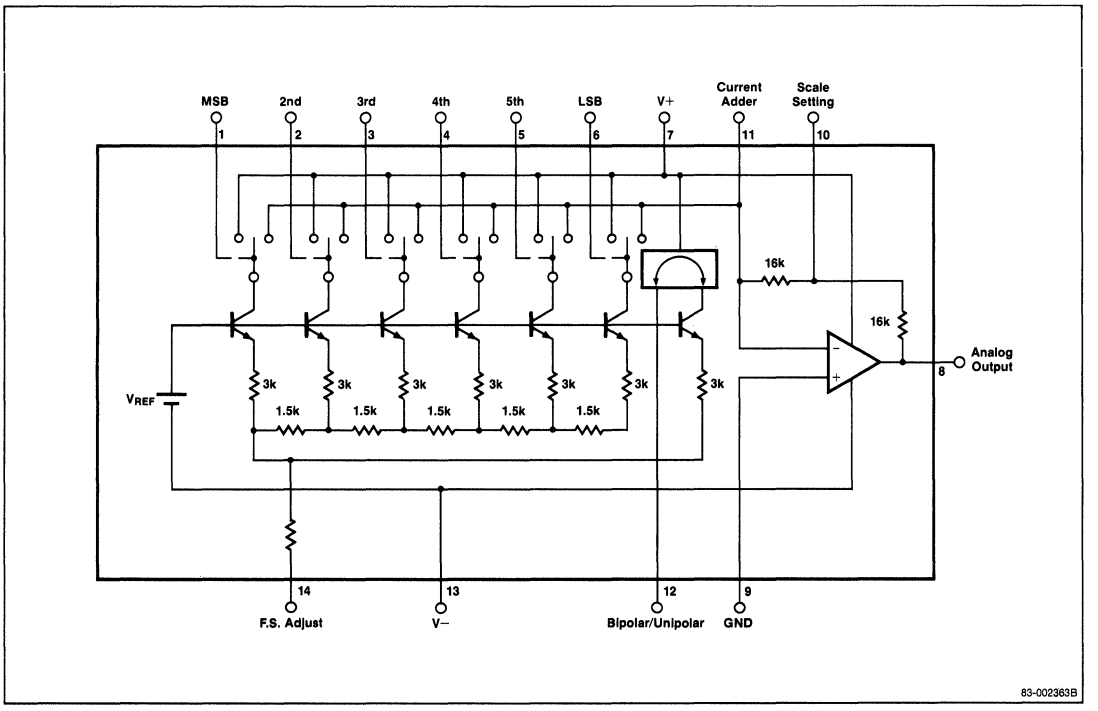


Pin Identification

Pin	Name	Function
1	MSB	Data Bit 1
2	2nd	Data Bit 2
3	3rd	Data Bit 3
4	4th	Data Bit 4
5	5th	Data Bit 5
6	LSB	Data Bit 6
7	V+	Power Supply Positive
8	Analog Output	
9	Ground	Power Supply Ground
10	F.S. Range	Full Scale Range Setting
11	Current Adder	
12	Bipolar/Unipolar	Bipolar/Unipolar Control
13	V−	Power Supply Negative
14	F.S. Adj.	Full Scale Adjust

6

Equivalent Circuit



Electrical Characteristics

$T_A = +25°C$, $V^{\pm} = \pm 15$ V

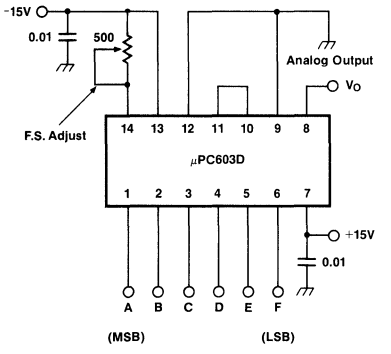
Parameter	Symbol	Limits Min.	Limits Typ.	Limits Max.	Unit	Test Conditions
Linearity Error	NL			0.4	%FSR	Fig. 1, 2, 3
				0.45	%FSR	Fig. 1, 2, 3; $T_A = -20$ to $+80°C$
Full Scale Temperature Coefficient (Note 2)	$\frac{\Delta I_{FS}}{I_{FS} - \Delta T}$		80	160	ppm/°C FSR	Fig. 1 each bit "ON" after FS adjust $T_A = -20$ to $+80°C$
Analog Output Offset Voltage:						
Unipolar				25	mV	Fig. 1 each bit "OFF" without FS adjust $T_A = -20$ to $+80°C$
Bipolar (Note 3)			50		mV	Fig. 2; ±5 V output without FS adjust
			100		mV	Fig. 3; ±10 V output without FS adjust
Low Level Input Voltage (Note 4)	V_{IL}			0.5	V	Bit "ON"
High Level Input Voltage (Note 4)	V_{IH}	2.1			V	Bit "OFF"
Input Terminal Current	I_{IN}			5.0	μA	$0 V \leq V_{IN} \leq 5$ V
Analog Output FS Voltage:						
Unipolar		+10.00		+11.75	V	$R_L = 2$ kΩ Fig. 1; without FS adjust
Bipolar		+4.93		+5.94	V	Fig. 2; ±5 V range; $R_L = 2$ kΩ without offset adjust and FS adjust
		−5.94		−4.93	V	
		+9.86		+11.89	V	Fig. 3; ±10 V range; $R_L = 2$ kΩ without offset adjust and FS adjust
		−11.89		−9.86	V	
Supply Voltage Rejection Ratio	SVRR			0.15	%FSR/V	$\pm 12 V \leq V^{\pm} \leq \pm 18$ V
Settling Time (Note 5)	T_S			3	μs	Error ≤ ½ LSB, $R_L = 5$ kΩ, $C_L = 30$ pF
Power Consumption	P_D			250	mW	

Notes: 1. %FSR and ppm FSR are the percentage and parts per million against full scale, respectively.
2. The average value of the differential coefficient at $T_C = -20$ to $+80°C$.
3. Care should be taken, since the temperature drift after bipolar offset adjustment has been made will become larger for ICs in which the offset voltage of the bipolar analog output is larger than the LSB value.
4. The input is active "Low."
5. When the load capacitance exceeds 30 pF there is a possibility of oscillation.

6

Typical Applications

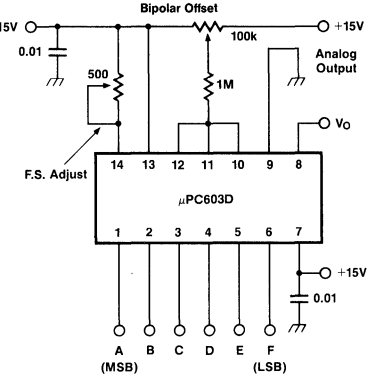
Unipolar Operation, Output 0 to 10 V Range



Digital Input 6 Bit Binary Code Active Low	Example Input	Output
	111111 =	0.00 V
	100000 ≒	4.92 V
	011111 ≒	5.08 V
	000000 =	10.00 V

83-002365A

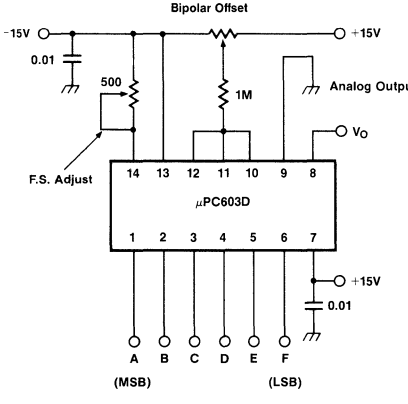
Bipolar Operation (2), −10 V to +10 V Output



Input 6 Bit Offset Binary code Active Low	Example Input	Output
	111111 =	−10.00 V
	100000 ≒	−0.16 V
	011111 ≒	+0.16 V
	000000 =	+10.00 V

83-002367A

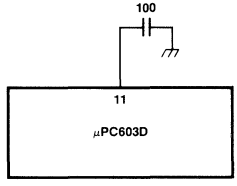
Bipolar Operation (1), Output −5 V to +5 V Range



Digital Input 6 Bit Offset Binary code Active Low	Example Input	Output
	111111 =	−5.00 V
	100000 ≒	−0.08 V
	011111 ≒	+0.08 V
	000000 =	+5.00 V

83-002366A

Compensation against Capacitive Loads (1)

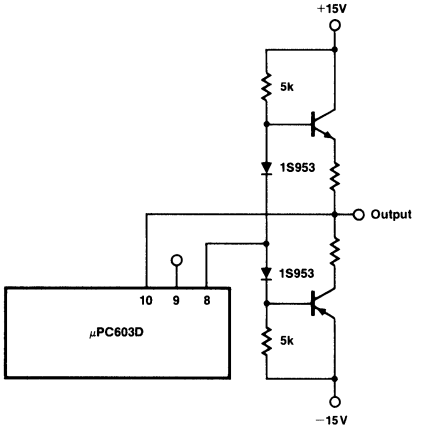


- ☐ The IC is stable against capacitive loads of less than 100 pF.
- ☐ Care should be taken, since the settling time will increase to about 5 μs.

83-002368A

Typical Applications (Cont.)

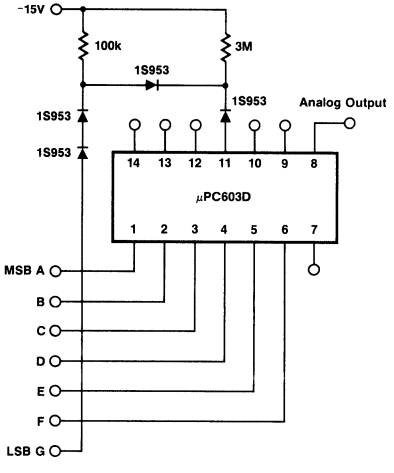
Compensation against Capacitive Loads (2)



- ☐ This method can be applied only to the 0 to 10 V and ±5 V output ranges.
- ☐ It is possible to connect such operational amplifiers as μPC318 etc. to the 8 pin as a voltage follower.

83-002369A

7-Bit D/A Converter

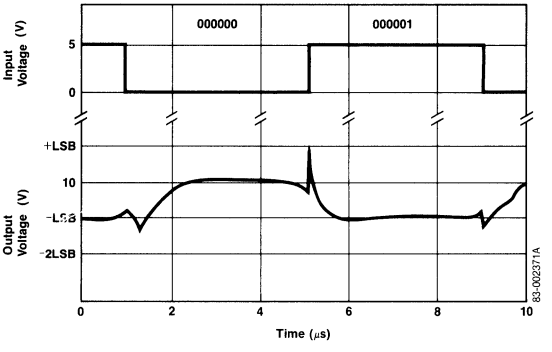


- ☐ The linearity error can be reduced by adjusting the 3 MΩ resistor.
- ☐ The output voltage may be set to any of the 3 ranges, with the circuits of figure 1, 2 and 3.

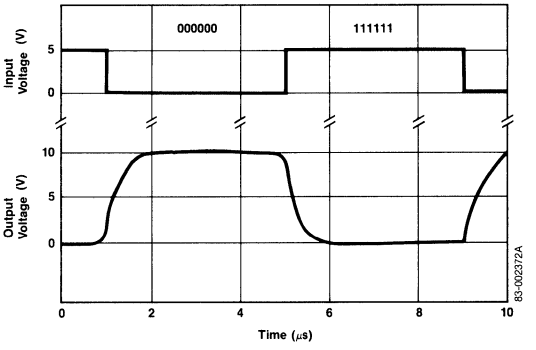
83-002370A

Operating Characteristics

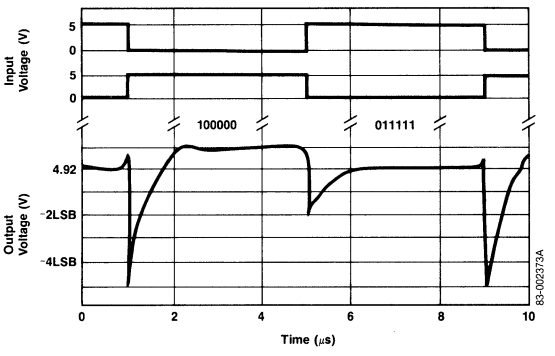
Output Response (1)



Output Response (2)



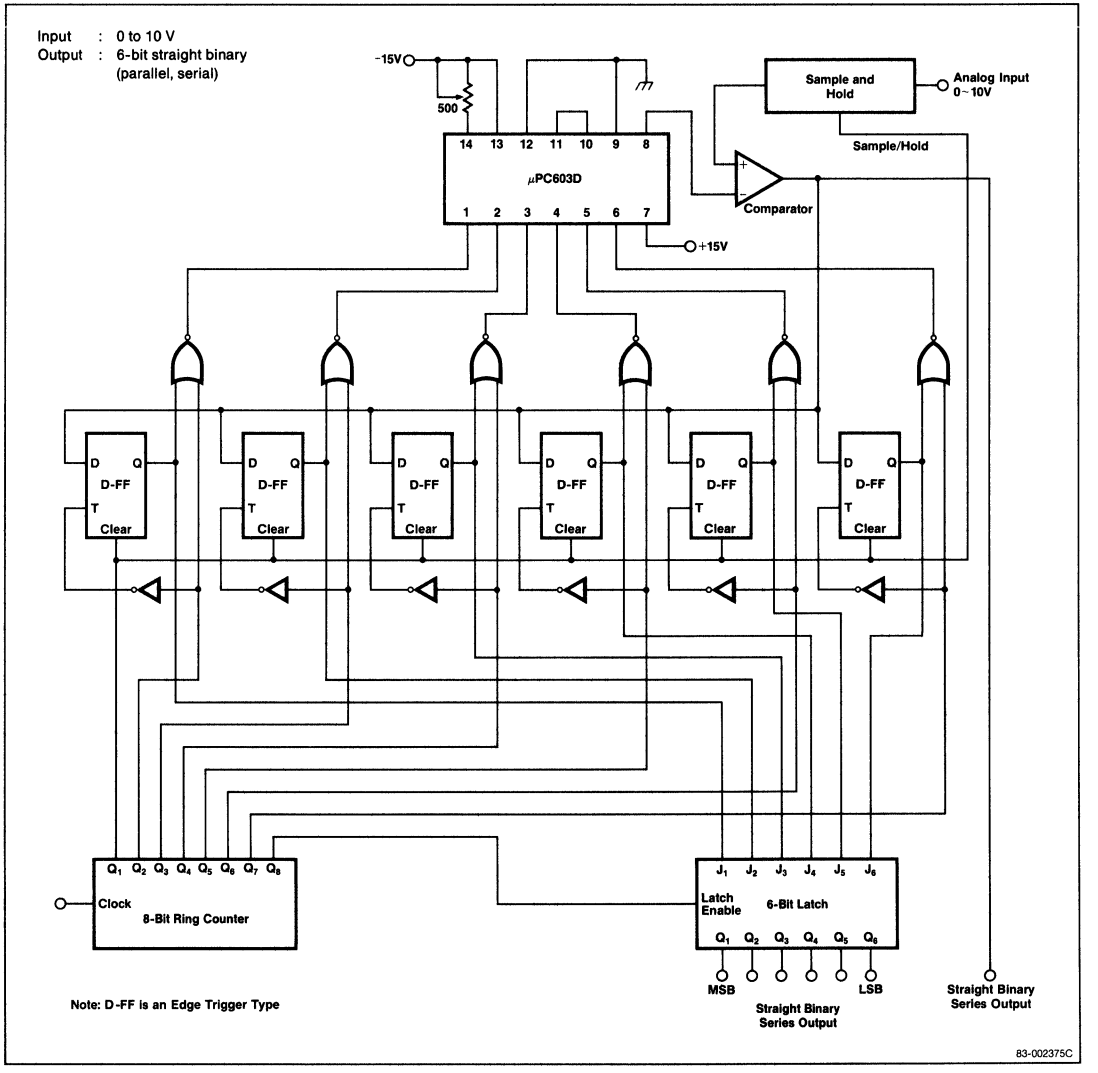
Glitch Waveform at 1/2 Scale



6

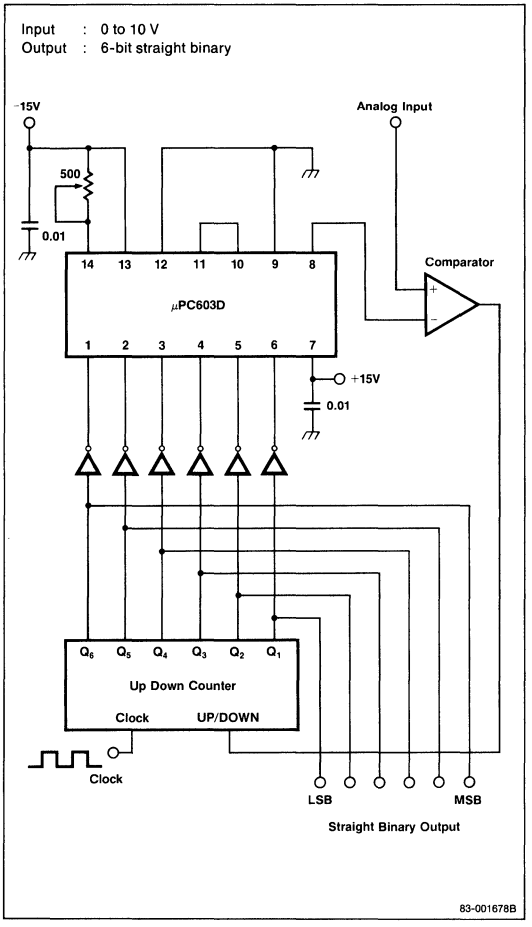
Application Circuits

Progressive comparison type A/D converter



Application Circuits (Cont.)

Tracking type A/D converter



6

μPC610
10-BIT POLARIZED D/A CONVERTER

Description

The μPC610 is a high performance precision monolithic digital-to-analog converter which converts 10-bit binary coded digital signals to an analog DC output voltage. All of the necessary circuit blocks are incorporated on board the converter to make designing simple. With the built-in voltage reference and reference input, multiplier operation is also possible.

Features

- ☐ Full Scale Temperature: 100 ppm/°C max
- ☐ Linearity error: 0.2% (1/2 LSB of 8th bit) max
- ☐ Settling Time: 1.5 μs typ
- ☐ Built-in band-gap reference voltage source
- ☐ Multiplying type
- ☐ Sign-Magnitude binary code
- ☐ Low noise
- ☐ Low power dissipation

Ordering Information

Part Number	Package	Operating Temperature Range
μPC610D	Ceramic DIP	−20°C to +80°C

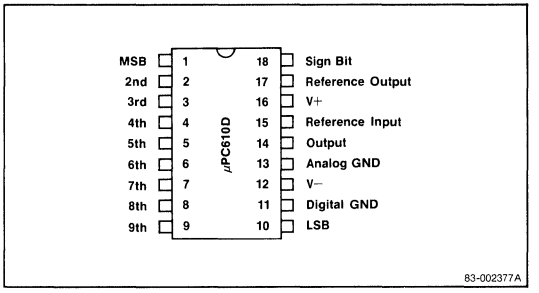
Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V^+ and V^-	±18 V
Power Dissipation	500 mW
Analog Ground to Digital Ground	±0.5 V
Logic Input Voltage	−5 to +15 V
Reference Input Voltage	0 to +7 V
Reference Voltage Source Output Current	1.0 mA
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−20 to +80°C
Storage Temperature Range	−55 to +150°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration

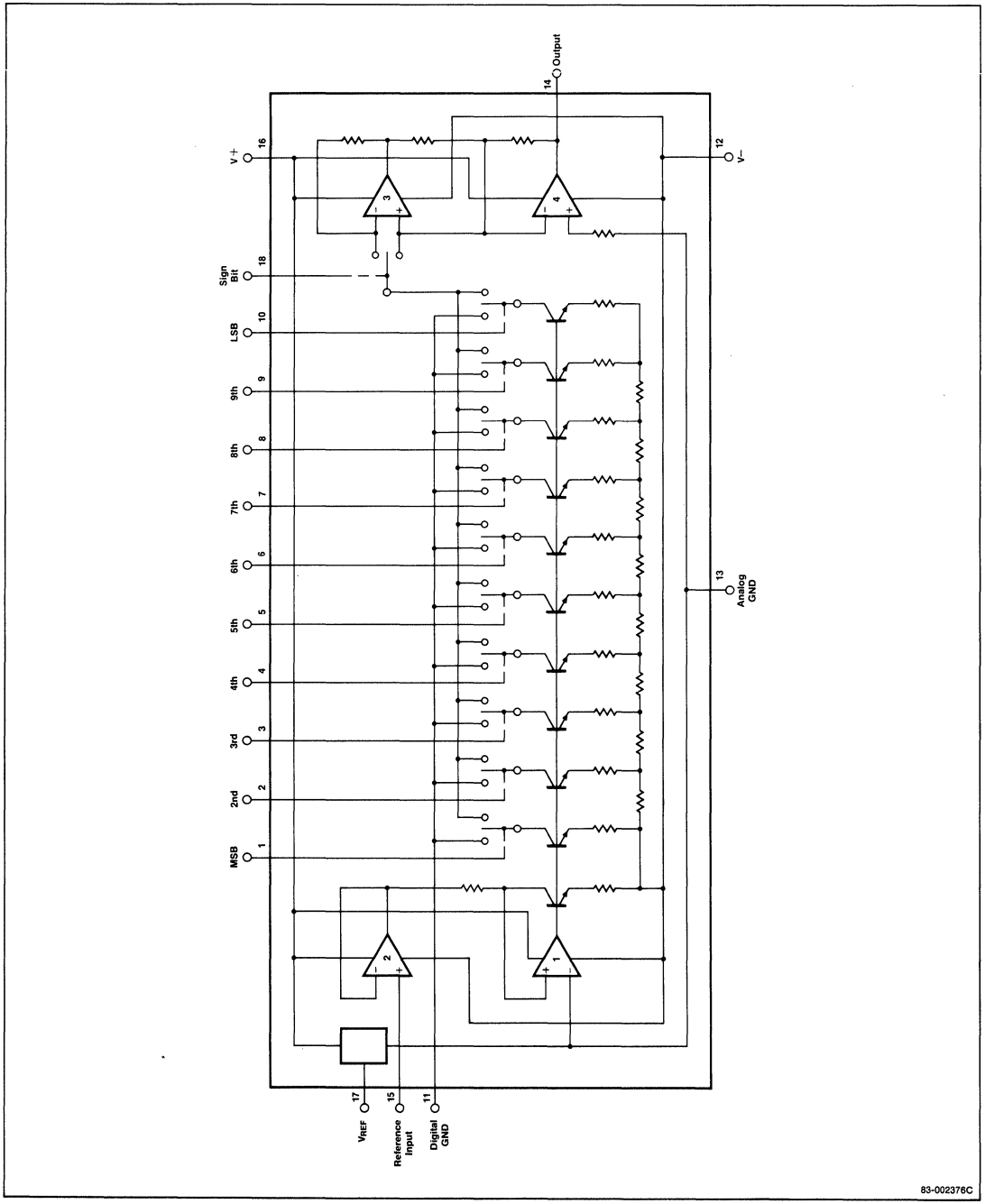


Pin Identification

Pin	Name	Function
1	MSB	Data Bit 1
2	2nd	Data Bit 2
3	3rd	Data Bit 3
4	4th	Data Bit 4
5	5th	Data Bit 5
6	6th	Data Bit 6
7	7th	Data Bit 7
8	8th	Data Bit 8
9	9th	Data Bit 9
10	LSB	Data Bit 10
11	Digital Ground	
12	V− Supply	Power Supply Negative
13	Analog Ground	
14	V_{OUT} − Output	Voltage Output
15	Reference Input	
16	V+ Supply	Power Supply Positive
17	Reference Output	
18	Sign Bit	Sign + or −

6

Equivalent Circuit



Electrical Characteristics

$T_A = +25°C$, $V^{\pm} = +15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution (Note 1)				11	Bit	Bipolar Operation
				10	Bit	Unipolar Operation
Linearity Error (Note 1)	NL		0.1	0.2	%FSR	$T_A = -20 \sim +80°C$
Settling Time	T_S		1.5	6.0	μs	Final Value ±20 mV
Full Scale Temperature Coefficient (Note 2)			50	100	ppm/°C	Using internal reference voltage source
			30	60	ppm/°C	Using external reference voltage source
Reference Input Bias Current	I_{IS}		100	500	nA	
Reference Input Slew Rate	SR		1.5		V/μs	
Reference Voltage	V_{REF}	2.2	2.4	2.6	V	$R_L \geq 20$ kΩ
Zero Scale Offset Voltage			±5	±10	mV	Signbit "ON", other bits "OFF"
Zero Scale Offset Symmetry			±1	±5	mV	
Full Scale Output Offset			±10	±80	mV	
Supply Voltage Rejection Ratio	SVRR		0.015	0.15	%FSR/V	$\pm 12\ V \leq V^{\pm} \leq \pm 18\ V$
Power Dissipation	P_D			300	mW	
Logic Input Terminal Current	I_{IN}			10	μA	$V_{IN} = -5\ V \sim +15\ V$
High Level Input Voltage (Note 3)	V_{IH}	2.0			V	
Low Level Input Voltage (Note 3)	V_{IL}			0.8	V	
Full Scale Output Voltage (Note 4)	V_O	10.0		11.0	V	All bits "ON", $R_L \geq 2$ kΩ
		−11.0		−10.0	V	Signbit "OFF", other bits "ON", $R_L \geq 2$ kΩ

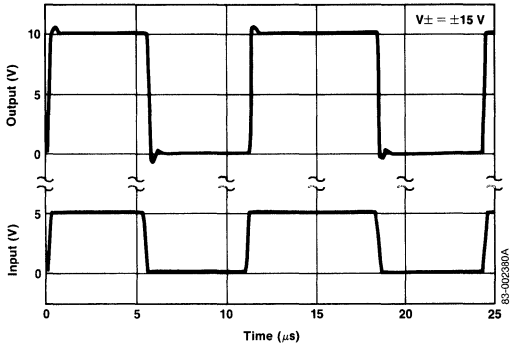
Notes: 1. Though the IC possesses a resolution of 10 or 11 bits, the linearity error is equivalent to 9 bits. In applications where perfect monotonicity is expected, employ the IC as an 8-bit D/A converter.
2. The average value of the differential coefficient at $T_A = -20°C$ to $+80°C$.
3. The digital input is active "High" binary code.
4. The value when the internal reference voltage is directly applied to the reference input terminals.

6

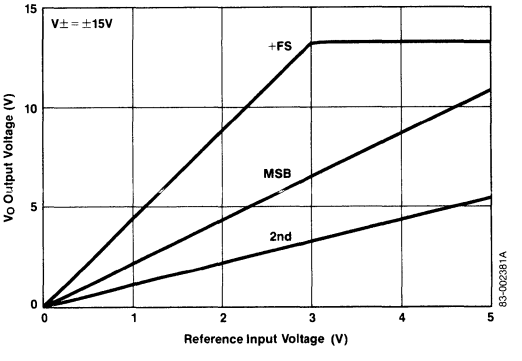
Typical Characteristics

($T_A = 25°C$)

Digital Input Response Characteristics

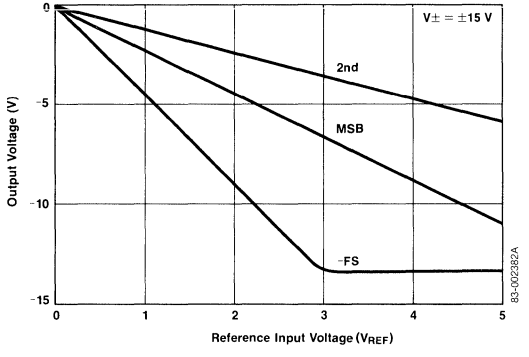


$V_{REF} - V_O+$ Characteristic

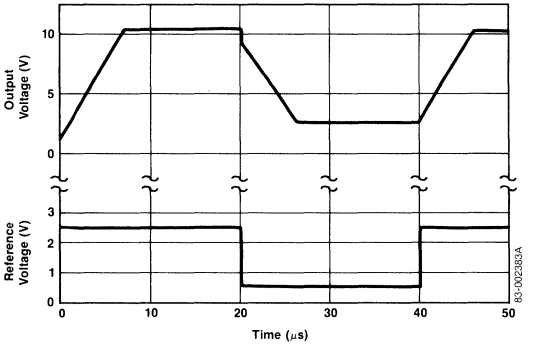


Typical Characteristics (Cont.)
($T_A = 25°C$)

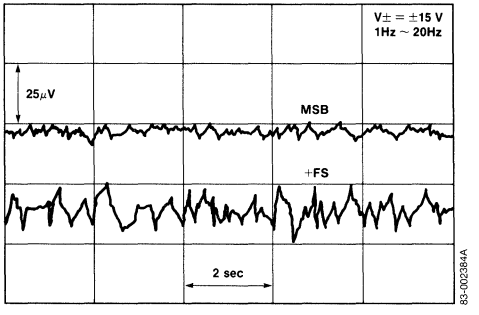
$V_{REF} - V_O -$ Characteristic



Reference Input Response Characteristic

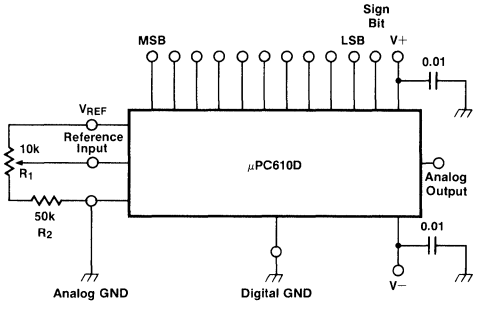


Output Noise Voltage



Typical Applications

Using internal reference voltage source



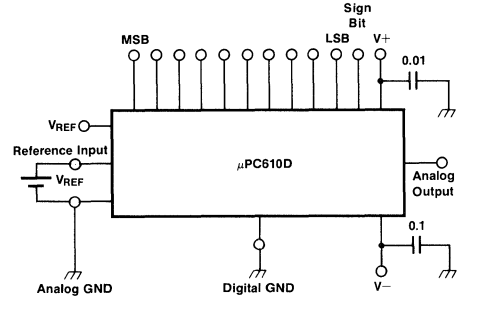
Note: Use resistors with good stability for R_1 and R_2.

☐ Sign + 10-Bit Binary code

Sign	Magnitude	
1	1111111111 =	
1	0000000000 =	0 V
0	0000000000 =	0 V
0	1111111111 =	0 V

83-002378A

External reference and multiplier type



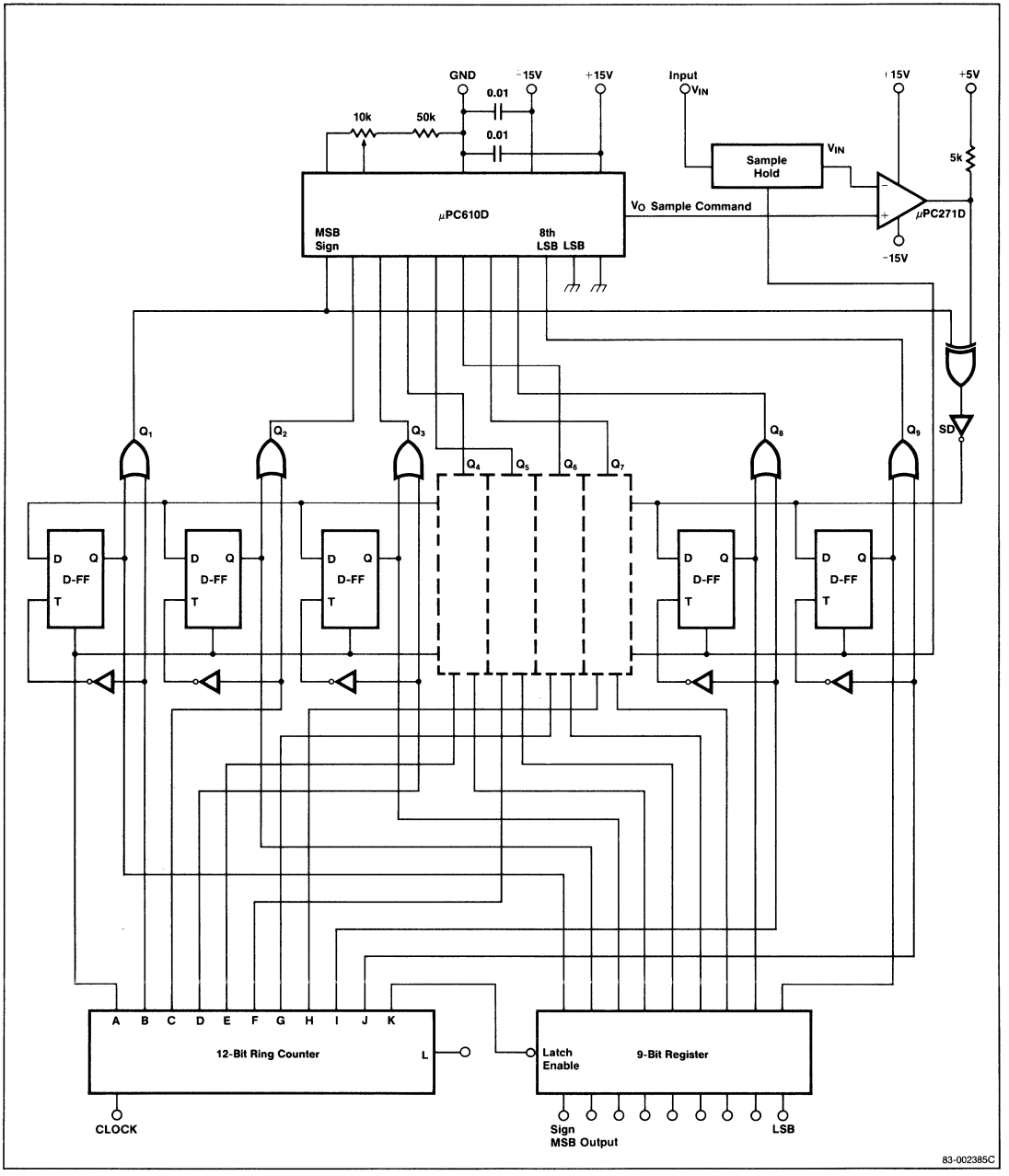
☐ Multiplying coefficient ≈ 4.4
$V_{FS} \approx 4.4 \times V_{REF}$,
$V_{MSB} \approx 2.2 \times V_{REF}$,
$V_{LSB} \approx 2.2 \times 2^{-9}$

83-002379A

Application Circuits

8-Bit + sign A/D converter

Successive approximation type (sheet 1 of 2)

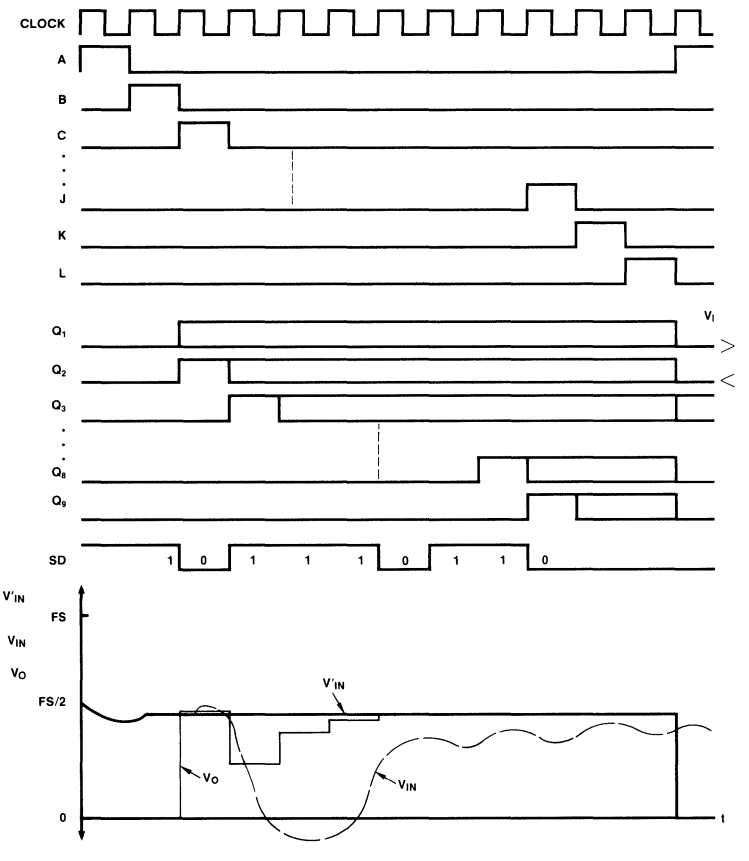


6

Application Circuits (Cont.)

8-bit + sign A/D converter

Successive approximation type (sheet 2 of 2)

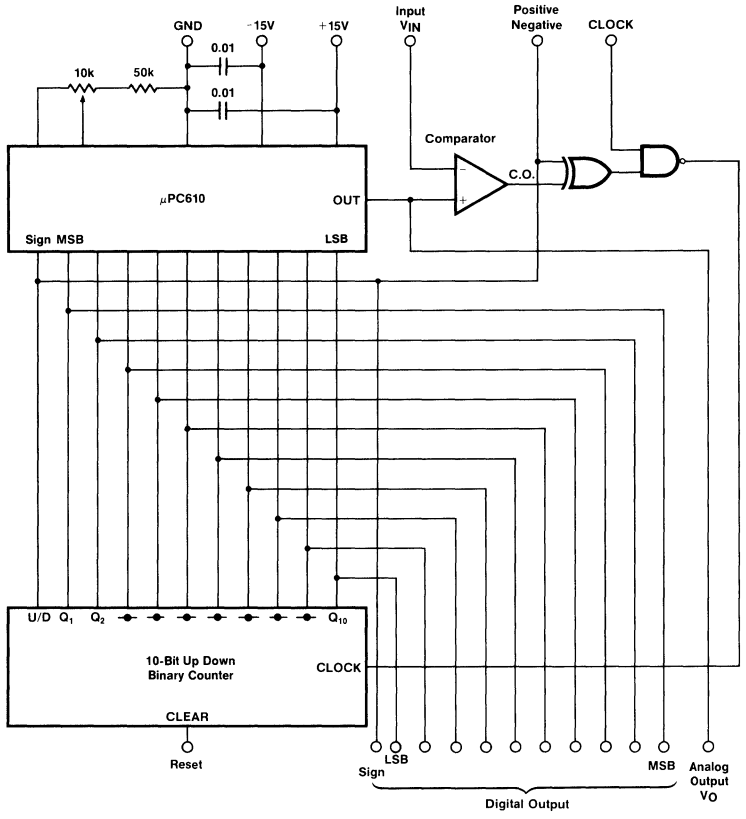


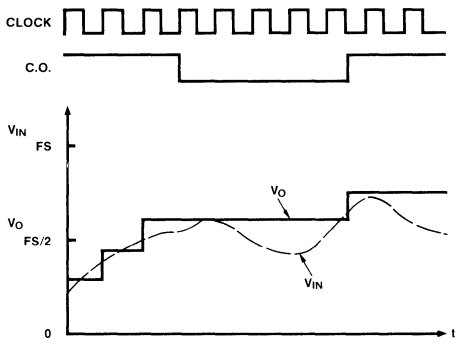
Note: D, V_{IN}, V'_{IN} and V_O show in case when an input equivalent to an output of "101110110".

83-002386C

Application Circuits (Cont.)

Peak detector (positive/negative)





83-002388C

6

Precautions for Usage

1. To absorb surges and prevent oscillation, bypass the power supply terminals with a capacitor of 0.01 μF.
2. To utilize the characteristics of the μPC610D in full, employ components of good stability for the full-scale adjustment resistor and the trimmer.
3. Since the settling time may increase or oscillation may occur in the case of capacitive loads, the μPC610D should be used with load capacitance of 100 pF or less.
4. The output amplifier will saturate at: $|V_{REF}| \geq 3$ V in the case of multiplier type operation. In this case the response time and power supply current will increase.
5. Since the reference potential inside the μPC610D is connected to the analog GND, common mode noise in regard to analog GND will present a direct error. Since analog GND and digital GND have independent circuits within the IC, these should be connected together outside the IC (if required).

μPC624
8-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER

Description

The μPC624 is a monolithic multiplying digital-to-analog converter designed for high speed performance and design/application flexibility. Advanced circuit design allows settling time of 85 ns. The outputs are high impedance dual complementary current types, which allow simple resistive loading, op-amp voltage conversion, and other configurations. The adjustable threshold logic input allows connection to all popular logic families.

Features

- ☐ Wide range multiplying capability
- ☐ Wide power supply range ±5 V to ±18 V
- ☐ High output impedance and compliance
- ☐ Variable logic threshold
- ☐ Direct interface to TTL, CMOS, PMOS
- ☐ Differential current outputs
- ☐ Pin to pin compatible with PMI'S DAC-08

Ordering Information

Part Number	Package	Operating Temperature Range
μPC624C	Plastic DIP	−20°C to +70°C
μPC624D	Ceramic DIP	−20°C to +80°C

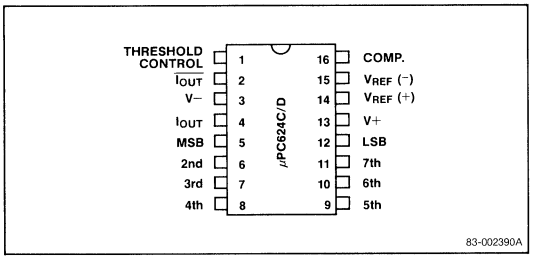
Absolute Maximum Ratings

$T_A = 25°C$

Supply Voltage	36 V
Logic Inputs	V^- to (V^- +36 V)
Logic Threshold Control Voltage	V^- to V^+
Analog Current Outputs	4.2 mA
Reference Inputs	V^- to V^+
Reference Input Differential Voltage	±18 V
Reference Input Current	5.0 mA
Power Dissipation, D or C Package	500 mW
Operating Temperature Range, D Package	−20 to +80°C
Operating Temperature Range, C Package	−20 to +70°C
Storage Temperature Range, D Package	−55 to +150°C
Storage Temperature Range, C Package	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration

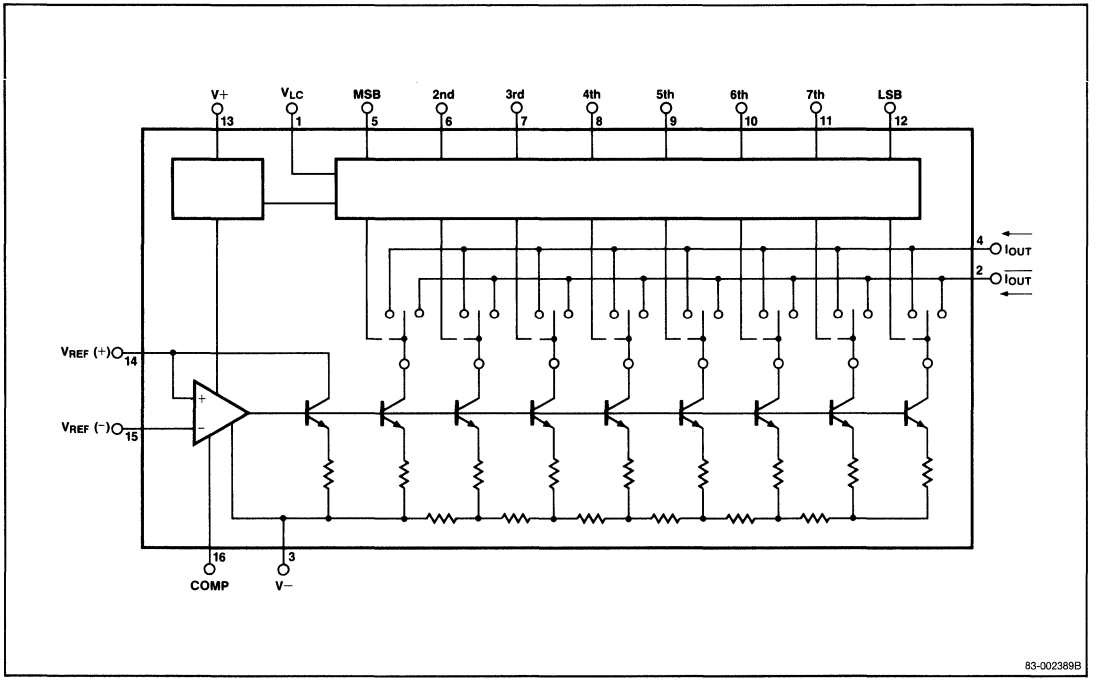


Pin Identification

Pin	Name	Function
1	Threshold Control	
2	I_{OUT}	Current Output
3	V−	Power Supply Negative
4	I_{OUT}	Current Output
5	MSB	Data Bit 1
6	2nd	Data Bit 2
7	3rd	Data Bit 3
8	4th	Data Bit 4
9	5th	Data Bit 5
10	6th	Data Bit 6
11	7th	Data Bit 7
12	LSB	Data Bit 8
13	V+	Power Supply Positive
14	$V_{REF}+$	Positive Reference Voltage
15	$V_{REF}-$	Negative Reference Voltage
16	Compensation	Amp Compensation

6

Equivalent Circuit



Electrical Characteristics

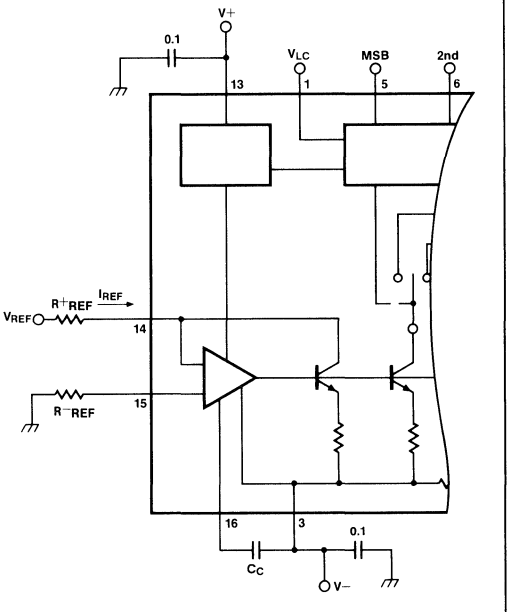
$T_A = +25°C$, $V^{\pm} = \pm 15$ V, $I_{REF} = 2.0$ mA

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	8	8	Bit	
Monotonicity		8	8	8	Bit	
Nonlinearity	NL			0.19	%FSR	
Settling Time	T_S		85	150	ns	$\pm$½ LSB, $R_L \leq 50\ \Omega$ All bits ON/OFF
Full Scale Temperature Coefficient			10	50	ppm/°C	
Output Voltage Compliance	V_{OC}	−10		+18	V	$\Delta I_{FS} \leq$ ½ LSB
Full Scale Current	I_{FS}	1.94	1.99	2.04	mA	$V_{REF} = 10.000$ V, $R^{+}_{REF} = 5.000$ kΩ
Full Scale Symmetry	$I_{FS} - I_{FS}$		±1.0	±8.0	μA	
Zero Scale Offset Current	I_{ZS}		0.2	2.0	μA	
Output Current Range	I_O	0	2.0	2.1	mA	$V^{-} = 5.0$ V
		0	2.0	4.2	mA	$V^{-} = 8.0$ V to −18 V
Low Level Input Voltage	V_{IL}			0.8	V	$V_{LC} = 0$ V, Bit "OFF"
High Level Input Voltage	V_{IH}	2.0			V	$V_{LC} = 0$ V, Bit "ON"
Low Level Input Current	I_{IL}		−2.0	−10	μA	$V_{LC} = 0$ V, $V_{IN} = -10$ V to +0.8 V
High Level Input Current	I_{IH}		0.002	10	μA	$V_{LC} = 0$ V, $V_{IN} = 2.0$ V to 18 V
Logic Input Swing	V_{IS}	−10		+18	V	
Logic Threshold Range	V_{TH}	−10		+13.5	V	$V_{TH} \approx V_{LC} + 1.3$ V
Reference Bias Current	I_{b+}			−3	μA	
Reference Input Slew Rate	$\Delta I_{REF}/\Delta T$	4.0	8.0		mA/μs	$R_{REF} \leq 200\ \Omega$, $C_C = 0$ pF
Power Supply Voltage Rejection Ratio	$SVRR^{+}$ V		0.0003	0.01	%FSR/%	$V^{+} = 4.5$ to 18 V, $I_{REF} = 1$ mA
	$SVRR^{-}$ V		0.002	0.01	%FSR/%	$V^{-} = -4.5$ to −18 V, $I_{REF} = 1$ mA
Power Supply Current	I^{+}		2.5	3.8	mA	
	I^{-}		−6.5	−7.8	mA	
	I^{+}		2.4	3.8	mA	$V^{+} = 5$ V, $V^{-} = -15$ V, $I_{REF} = 2$ mA
	I^{-}		−6.4	−7.8	mA	$V^{+} = 5$ V, $V^{-} = -15$ V, $I_{REF} = 2$ mA
	I^{+}		2.3	3.8	mA	$V^{\pm} = \pm 5$ V, $I_{REF} = 1$ mA
	I^{-}		−4.3	−5.8	mA	$V^{\pm} = \pm 5$ V, $I_{REF} = 1$ mA

6

Typical Applications

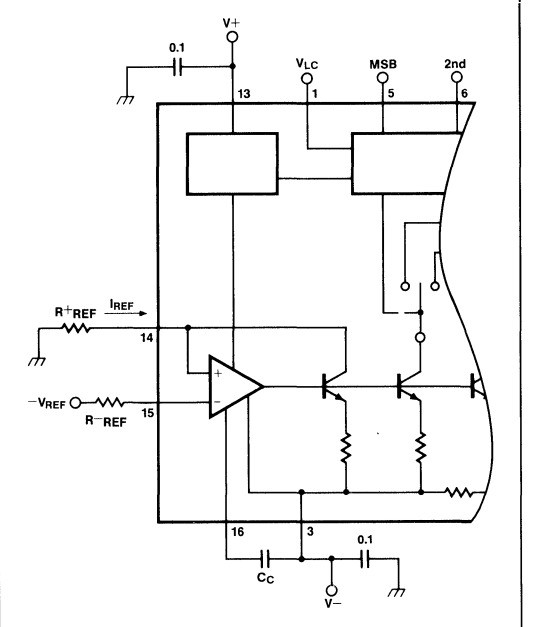
Basic Positive Reference Operation



Notes: 1. $R^{+}_{REF} = R^{-}_{REF}$
2. $C = 0.01\ \mu F$ (Standard Value)
3. Minimum capacitor value for stable operation is given by $C_C = R_{REF}\ (k\Omega) \times 15\ (pF)$.

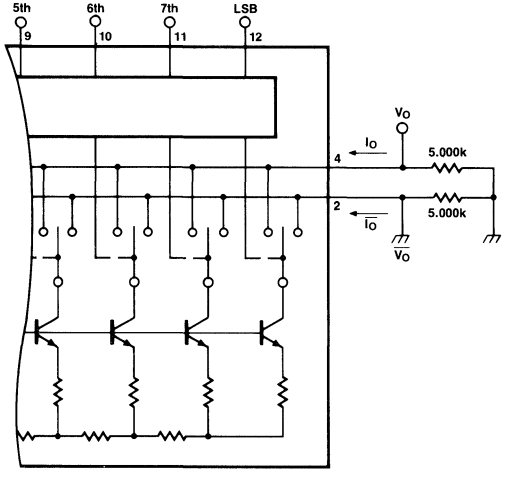
83-002391B

Basic Negative Reference Operation



83-002392B

Basic Unipolar Negative Operation



$I_{REF} = 2.000$ mA

Input	I_O (mA)	$\overline{I_O}$ (mA)	V_O (V)	$\overline{V_O}$ (V)
1 1 1 1 1 1 1 1	1.992	0.000	−9.96	0.00
1 1 1 1 1 1 1 0	1.984	0.008	−9.92	−0.04
1 0 0 0 0 0 0 1	1.008	0.984	−5.04	−4.92
1 0 0 0 0 0 0 0	1.000	0.992	−5.00	−4.96
0 1 1 1 1 1 1 1	0.992	1.000	−4.96	−5.00
0 0 0 0 0 0 0 1	0.008	1.984	−0.04	−9.92
0 0 0 0 0 0 0 0	0.000	1.992	0.00	−9.96

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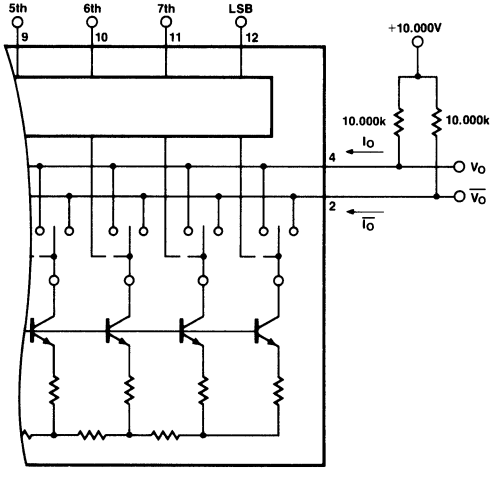
Typical Applications (Cont.)

Basic Bipolar Output Operation

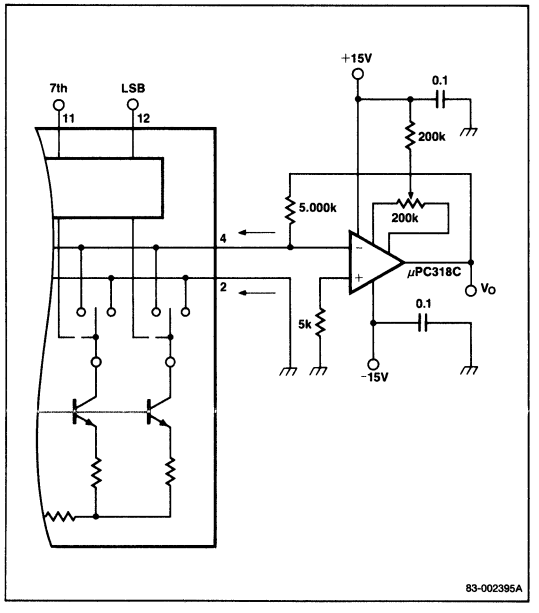


I_{REF} = 2.000 mA

Input	I_O (mA)	$\overline{I_O}$ (mA)	V_O (V)	$\overline{V_O}$ (V)
1 1 1 1 1 1 1 1	1.992	0.000	−9.92	+10.00
1 1 1 1 1 1 1 0	1.984	0.008	−9.84	+9.92
1 0 0 0 0 0 0 1	1.008	0.984	−0.08	+0.16
1 0 0 0 0 0 0 0	1.000	0.992	0.00	+0.08
0 1 1 1 1 1 1 1	0.992	1.000	+0.08	0.00
0 0 0 0 0 0 0 1	0.008	1.984	+9.92	−9.84
0 0 0 0 0 0 0 0	0.000	1.992	+10.00	−9.92

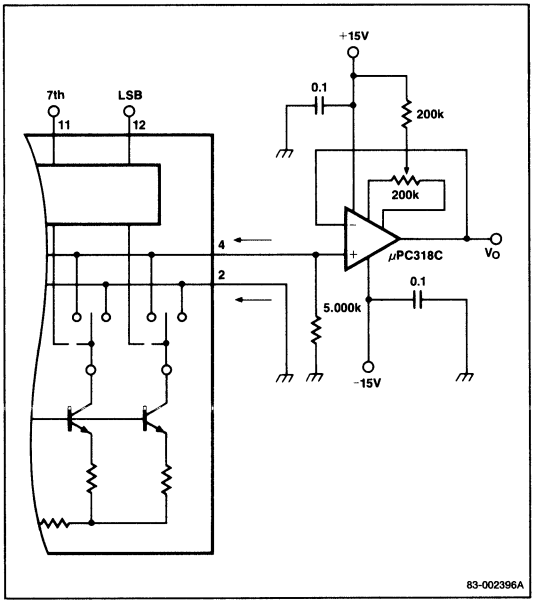
83-002394B

Positive Low Impedance Output Operation



83-002395A

Negative Low Impedance Output Operation

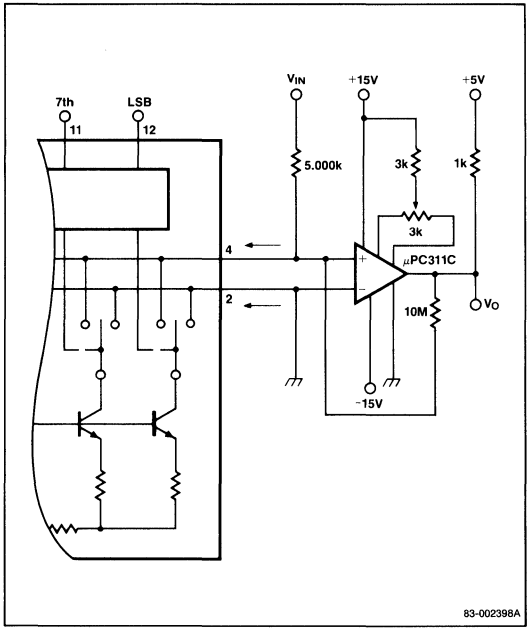


83-002396A

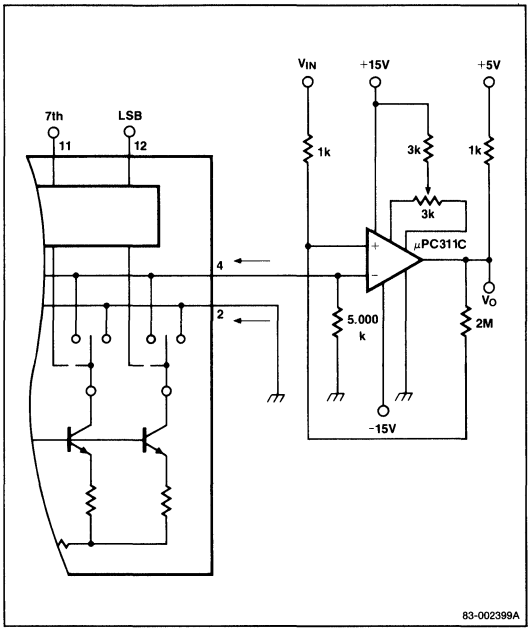
6

Typical Applications (Cont.)

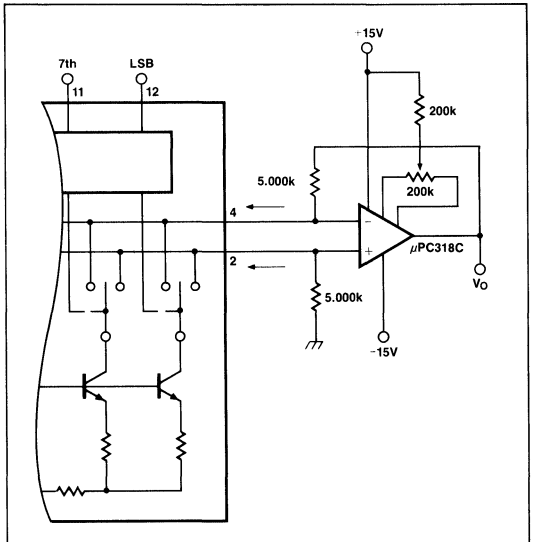
Comparator Connection Method for A/D Conversion
(Positive Analog Input)



Comparator Connection Method for A/D Conversion
(Negative Analog Input)



Low Impedance Output Operation (Both Outputs)



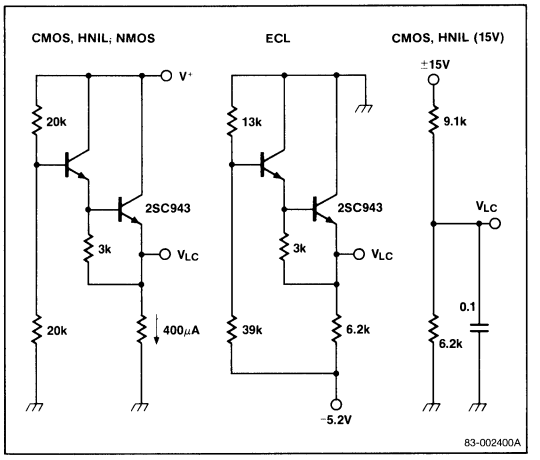
Note: For buffer amplifier, high slew rate op-amp is recommended to obtain fast settling time.

Interfacing with Various Logic Families

The logic threshold is set about 1.4 V above V_{LC}. This enables TTL level acceptance by simply grounding pin 1. By placing an appropriate voltage at the logic threshold control pin (pin 1), various threshold values are available for the other logic families.

TTL interface permission gives the interval logic threshold −4 mV/°C temperature coefficient. $V_{TH} = V_{LC} + 1.4\ V - 0.004\ V \times (T_A - 25°C)$.

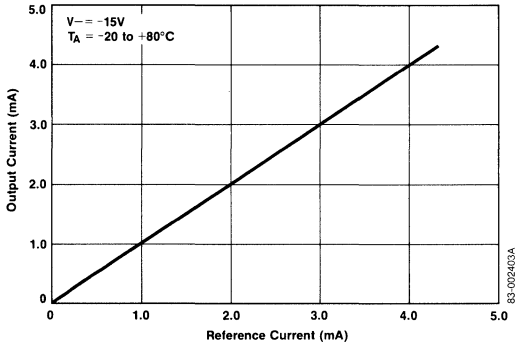
Anti-temperature coefficient circuits



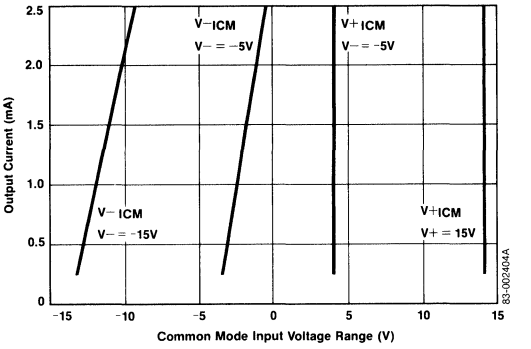
6

Operating Characteristics
($T_A = 25°C$)

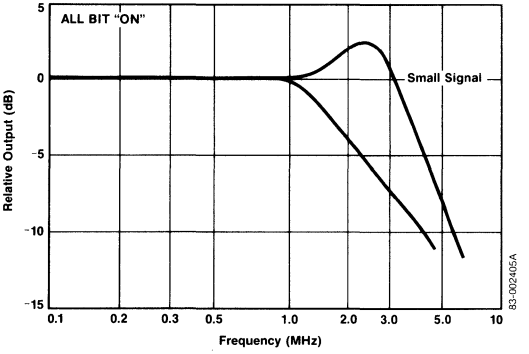
Full Scale Current



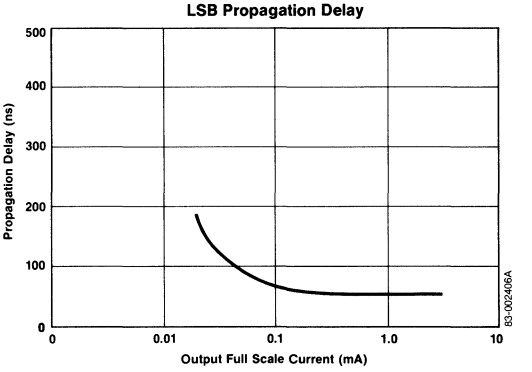
Full Scale Current



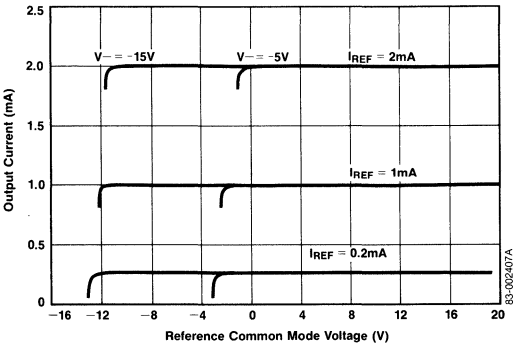
Reference Input Frequency Response



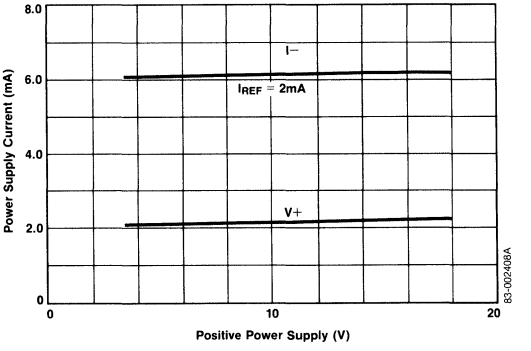
LSB Propagation Delay



Reference Amp Common Mode Range



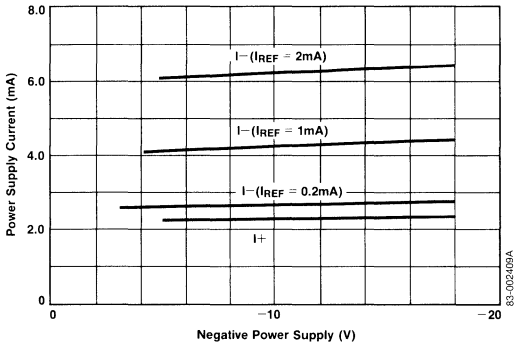
Power Supply Current



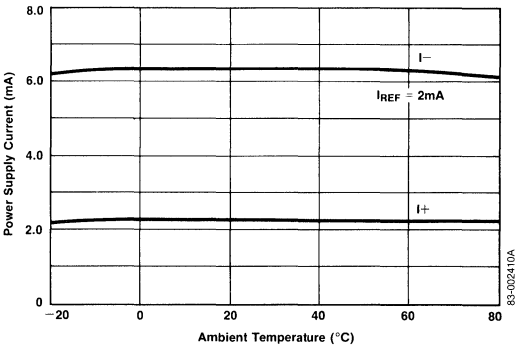
Operating Characteristics (Cont.)

($T_A = 25°C$)

Power Supply Current



Power Supply Current



A/D Conversion Program List

0000		MVI	A, 89H	: CONTROL WORD FOR 8255
0002		OUT	(8255)	: PROGRAM TO 8255
0004		MVI	B, 80H	: BIT POINTER INITIALIZE
0006		MOV	A, B	: BIT SET WORD
0007	BIT TEST	OUT	(PORT B)	: BIT SET OUTPUT TO PB OF 8255
0009		MOV	C, A	
000A		NOP		
000B		IN	(PORT C)	: READ COMPARATOR
000D		RRC		: $A_0 \rightarrow$ CARRY FLG
000E		JC	DEC POINTER	: COMPARATOR TEST
0011		MOV	A, C	
0012		SUB	B	: BIT RESET
0013		MOV	C, A	
0014	DEC POINTER	MOV	A, B	
0015		RRC		: DECREMENT BIT POINTER
0016		JC	RETURN	: LSB WAS TESTED?
0019		MOV	B,A	
001A		ORA	C	: NEW BIT SET WORD
001B		JMP	BIT TEST	
001E	RETURN	RET	(MAIN PROGRAM)	: CONVERSION END & RETURN TO MAIN PROGRAM
	PROGRAM MEMORY		: 31 BYTE	
	CONVERSION TIME		: 371 μs (741 STATE) MAX, 323 μs (645 STATE) MIN (@ ϕ + 2 MHz)	
	WORKING REGISTER		:B & C (C REGISTER; FINAL ANSWER MEMORY)	

6

μPC6012
12-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER

Description

The μPC6012 monolithic multiplying digital-to-analog converter is designed to set new standards of speed and accuracy for 12-bit converters. This device is the first 12-bit DAC to use standard processing without the need of thin film resistors and/or active trimming of individual devices. The μPC6012 features high voltage compliance, and high impedance dual complementary outputs, which enable differential operation to effectively double the peak-to-peak output swing. The outputs can be used without op-amps in many applications.

Features

- ☐ Differential nonlinearity to ±0.025% FS max
- ☐ Fast setting time: 400 ns typical
- ☐ Full scale current 4 mA
- ☐ High output impedance and compliance: −5 to +10 V
- ☐ Differential current output
- ☐ High speed multiplying capability
- ☐ Direct interface to TTL, CMOS, ECL, HTL, NMOS
- ☐ Am6012 direct replacement

Ordering Information

Part Number	Package	Operating Temperature Range
μPC6012C	Plastic DIP	0°C to +70°C

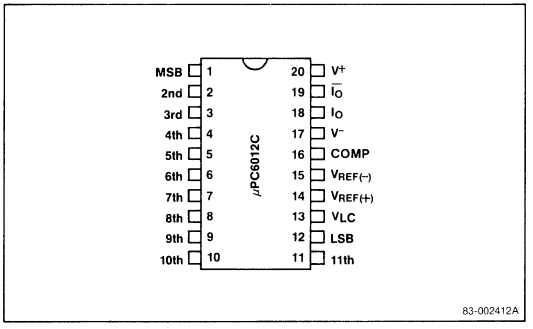
Absolute Maximum Ratings

$T_A = 25°C$

Power Supply Voltage Range, $V^+ - V^-$	36 V
Logic Input Voltage Range, $V^{\pm}$	−5 to +18 V
Output Voltage Range, V_O	−8 to +12 V
Reference Input Voltage Range, V^+_{REF}	V− to V+
Reference Input Differential Voltage Range, $V^+_{REF} - V^-_{REF}$	±18 V
Reference Input Current Range, I_{REF}	0 − 1.25 mA
Total Power Dissipation, P_T	500 mW
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration

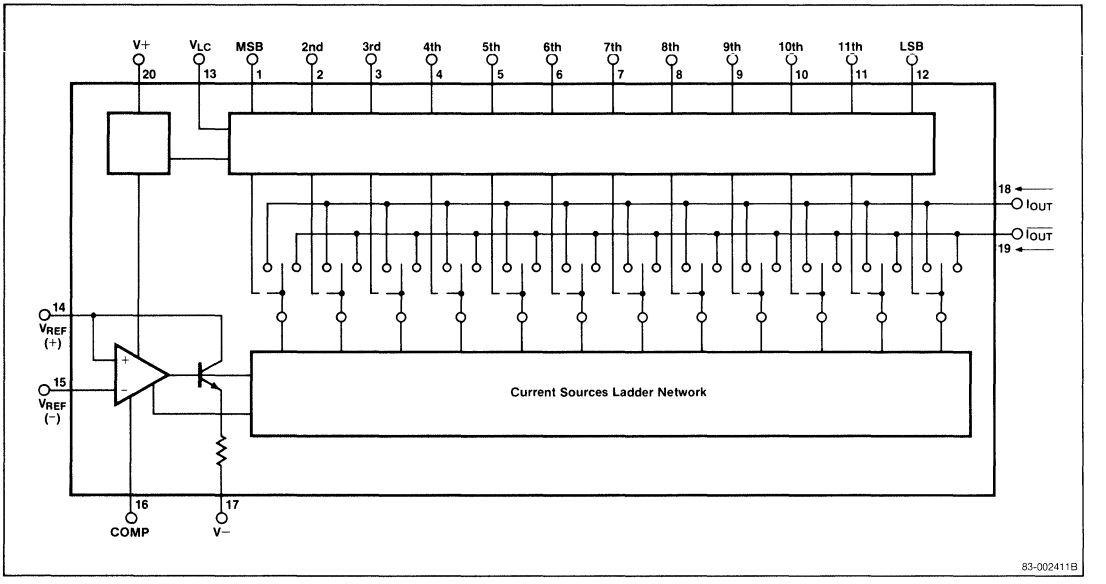


Pin Identification Table

Pin	Name	Function
1	MSB	Data Bit 1
2	2nd	Data Bit 2
3	3rd	Data Bit 3
4	4th	Data Bit 4
5	5th	Data Bit 5
6	6th	Data Bit 6
7	7th	Data Bit 7
8	8th	Data Bit 8
9	9th	Data Bit 9
10	10th	Data Bit 10
11	11th	Data Bit 11
12	LSB	Data Bit 12
13	V_{LC}	Threshold Control
14	$V_{REF}+$	Positive Reference Voltage
15	$V_{REF}-$	Negative Reference Voltage
16	Compensation	Amp Compensation
17	V− Supply	Negative Supply Voltage
18	I_O	Current Out +
19	$\overline{I_O}$	Current Out −
20	V+ Supply	Positive Supply Voltage

6

Block Diagram



Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Power Supply Voltage	V^+	+4.5	+15		V	
	V^-		−15	−10.8	V	
Ambient Temperature	T_A	0	+25	+70	°C	
Reference Input Current	I_{REF}	0.2	1.0	1.1	mA	
High Level Input Voltage	V_{IH}	+2.0		+18	V	V_{LC} = 0 V
Low Level Input Voltage	V_{IL}	−5.0		+0.8	V	V_{LC} = 0 V
Output Voltage Compliance	V_{OC}	−5.0	0	+10	V	DNL ≤ ±0.025% FSR

Electrical Characteristics

T_A = 0 to 70°C, $V^{\pm}$ = ±15 V, I_{REF} − 1.0000 mA

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Monotonicity		12	12	12	Bit	
Differential Nonlinearity	DNL			±0.025	%FSR	
Nonlinearity	NL			±0.05	%FSR	
Full Scale Output Current	I_{FS}	3.935	3.999	4.063	mA	V_{REF} = 10.000 V, T_A = 25°C, $R_{14} = R_{15}$ = 10.000 kΩ
Full Scale Temperature Coefficient	$\frac{\Delta I_{FS}}{I_{FS} - \Delta T}$			±40	ppm/°C	
Full Scale Symmetry	$I_{FS} - I_{FS}$			±2.0	μA	
Zero Scale Current	I_{ZS}			0.10	μA	
Settling Time	t_s		400		ns	½ LSB, T_A = 25°C, all bits ON or OFF
Propagation Delay	t_{PLH}, t_{PHL}			50	ns	50% to 50%
Output Capacitance	C_O		35		pF	
Logic Input Current	I_{IN}			40	μA	−5 V < V_I < +18 V
Reference Bias Current	I_{b+}			−2.0	μA	
Reference Input Slew Rate	$\lvert\Delta I_{REF}/\Delta t\rvert$	4.0	8.0		mA/μs	C_C = 0, R_{14} = 800 Ω
Supply Voltage Rejection Ratio	$\lvert SVRR^+\rvert$			±0.001	%FSR/%	V+ = +13.5 to +16.5 V, V− = −15 V
	$\lvert SVRR^-\rvert$			±0.001	%FSR/%	V− = +13.5 to −16.5 V, V+ = +15 V
Power Supply Current	I^+1			8.5	mA	V^+ = +5 V
	I^-1			−18.0	mA	V^- = −15 V
	I^+2			8.5	mA	V^+ = +15 V
	I^-2			−18.0	mA	V^- = −15 V
Power Dissipation	P_{D1}			312	mW	V^+ = +5 V, V^- = −15 V
	P_{D2}			397	mW	V^+ = +15 V, V^- = −15 V

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Typical Applications

There is a 1 to 4 scale factor between the reference current (I_{REF}) and the full scale output current (I_{FS}).

If $V_{REF} = +10$ V and $I_{FS} = 4$ mA, the value of the R_{REF} is:

$$R^{+}_{REF} = \frac{4 \times 10\ V}{4\ mA}$$

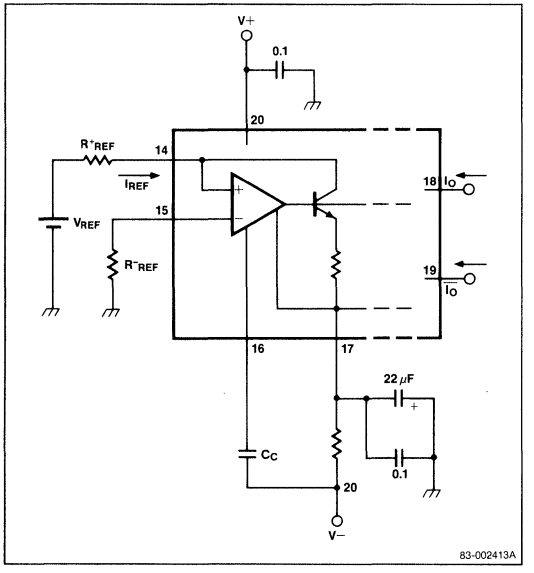
$$R^{+}_{REF} = R^{-}_{REF}$$

The compensation capacitor is a function of the impedance seen at the $+V_{RFF}$ input and is determined by the following expression:

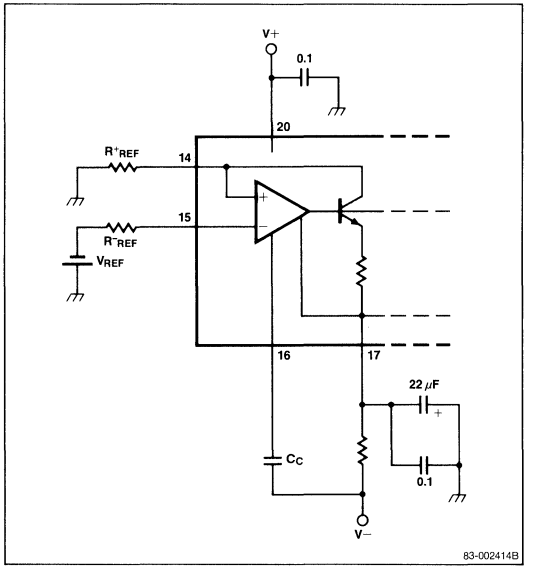
$C = (5\ pF)\ (R+_{REF\ (k\ \Omega)})$.

For $R_{14} < 800\Omega$, no capacitor is necessary.

Positive Reference Voltage

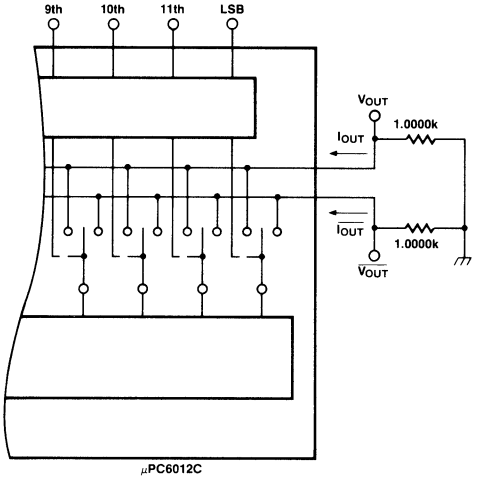


Negative Reference Voltage



Typical Applications (Cont.)

Unipolar Negative Output



I_{REF} = 1.0000 mA

Input Code MSB	LSB	I_O (mA)	$\overline{I_O}$ (mA)	V_O (V)	$\overline{V_O}$ (V)
1 1 1 1 1 1 1 1 1 1 1	1	3.999	0.000	−3.999	0.000
1 1 1 1 1 1 1 1 1 1 1	0	3.998	0.001	−3.998	−0.001
1 0 0 0 0 0 0 0 0 0 0	0	2.000	1.999	−2.000	−1.999
0 0 0 0 0 0 0 0 0 0 0	1	0.001	3.998	−0.001	−3.998
0 0 0 0 0 0 0 0 0 0 0	0	0.000	3.999	0.000	−3.999

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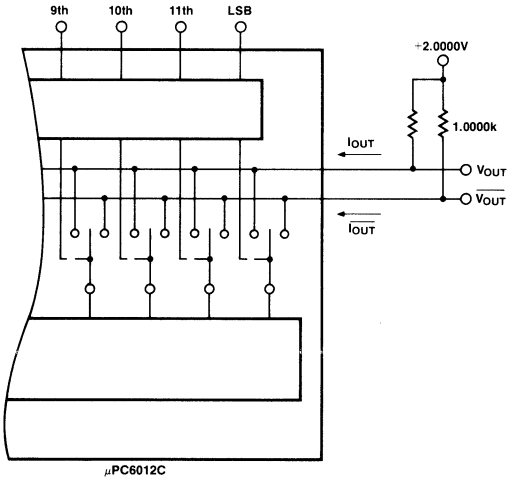
Bipolar Output



I_{REF} = 1.0000 mA

Input Code MSB	LSB	I_O (mA)	$\overline{I_O}$ (mA)	V_O (V)	$\overline{V_O}$ (V)
1 1 1 1 1 1 1 1 1 1 1	1	3.999	0.000	−1.999	+2.000
1 1 1 1 1 1 1 1 1 1 1	0	3.998	0.001	−1.998	+1.999
1 0 0 0 0 0 0 0 0 0 0	1	2.001	1.998	−0.001	+0.002
1 0 0 0 0 0 0 0 0 0 0	0	2.000	1.999	0.000	+0.001
0 1 1 1 1 1 1 1 1 1 1	1	1.999	2.000	+0.001	0.000
0 0 0 0 0 0 0 0 0 0 0	1	0.001	3.998	+1.999	−1.998
0 0 0 0 0 0 0 0 0 0 0	0	0.000	3.999	+2.000	−1.999

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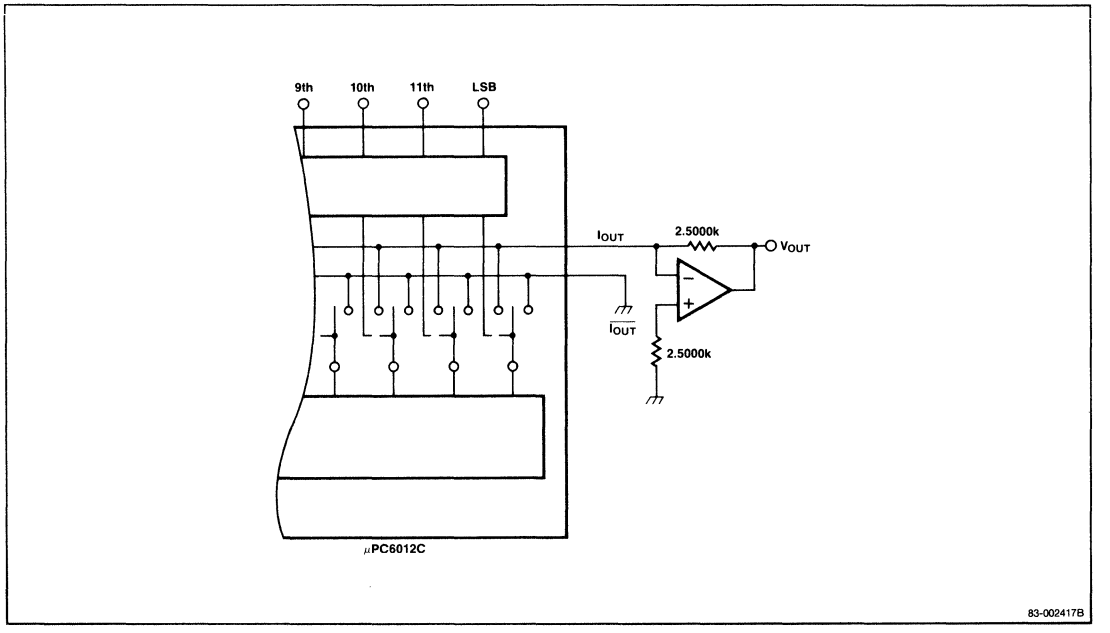
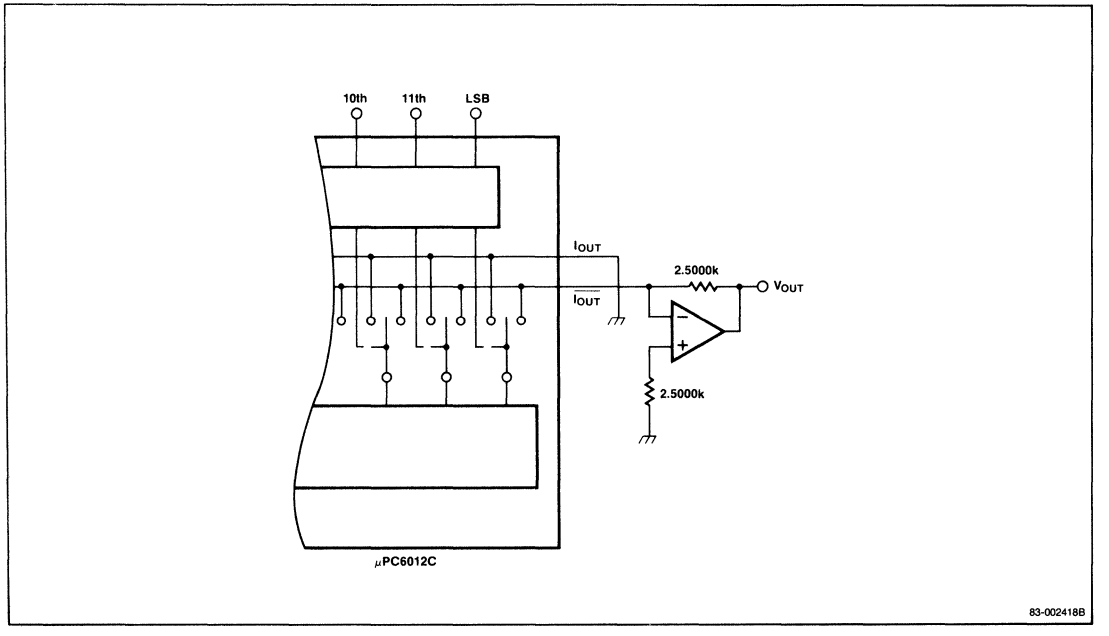
Typical Applications (Cont.)

Unipolar Positive Output (Straight Binary)

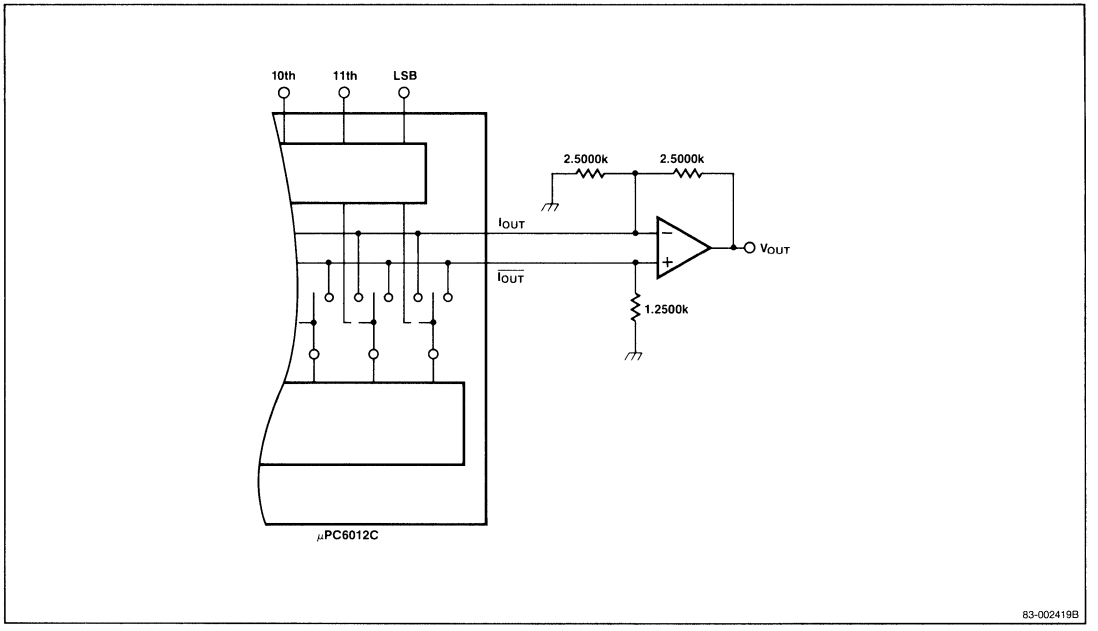


Unipolar Negative Output (Complementary Binary)



Typical Applications (Cont.)

Symmetrical Offset



6

NEC

NEC Electronics Inc.

μPD6900
8-BIT CMOS VIDEO D/A CONVERTER

PRELIMINARY INFORMATION

Description

The μPD6900 is an 8-bit D/A converter for video signals. Although it is a CMOS converter (V+ =5 V), its conversion rate is very high because a high-speed CMOS processing technique and matrix current cell method are used.

With its low power consumption and conversion rate of 20Msps, this converter can be applied to various units such as digital video processing systems and high-speed facsimiles.

Features

- ☐ Conversion rate: 20 Megasamples/sec
- ☐ Linearity: ±1/2 LSB typ
- ☐ Reference voltage: 2.0 V typ
- ☐ Single 5 V power supply
- ☐ Low power consumption: 150 mW typ.
- ☐ TTL compatible digital input

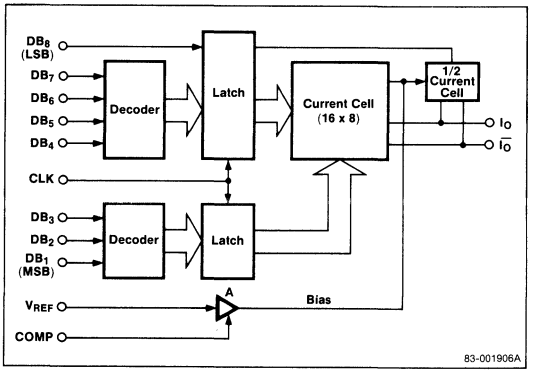
Absolute Maximum Ratings

$T_A = 25°C$

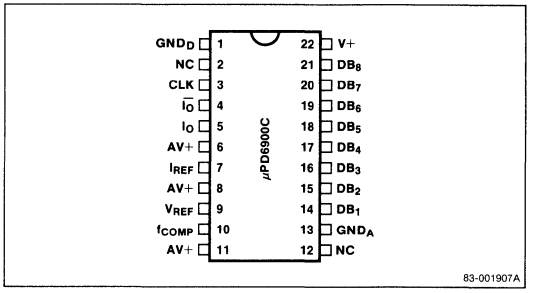
Power supply voltage	−0.3 to +7.0 V
Input/output terminal voltage	−0.3 to V+ +0.3 V
Operating temperature range	−10 to +75 °C
Storage temperature range	−40 to +125 °C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Configuration



Pin Identification

Pin	Symbol	Function
1	GND_D	Digital GND
2	NC	No connection
3	CLK	Clock input
4	$\overline{I_O}$	Complementary current output
5	I_O	Current (analog) output
6	AV+	Analog power supply
7	I_{REF}	Full-scale current adjustment
8	AV+	Analog power supply
9	V_{REF}	Reference voltage input
10	f_{COMP}	Frequency compensation
11	AV+	Analog power supply
12	NC	No connection
13	GND_A	Analog GND
14	DB_1	Digital input (MSB)
15	DB_2	Digital input (2nd)
16	DB_3	Digital input (3rd)
17	DB_4	Digital input (4th)
18	DB_5	Digital input (5th)
19	DB_6	Digital input (6th)
20	DB_7	Digital input (7th)
21	DB_8	Digital input (LSB)
22	V+	Digital power supply

Ordering Information

Part Number	Package	Operating Temperature Range
μPD6900C	Plastic DIP	−20 °C to +75 °C

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Pin Function

DB_1 to DB_8

DB_1 to DB_8 are the 8-bit digital signal input terminals. DB_1 corresponds to MSB, and DB_8 corresponds to LSB.

CLK

CLK is the sampling clock input terminal. An 8-bit digital signal is latched within the IC by the rising edge of the sampling clock and is converted into an analog signal.

I_O

I_O is the analog output terminal. This output is current output. It outputs the current of 10 mA (typ) at the full scale (Reference voltage = 2 V, R_{REF} = 800 Ω).

$\overline{I_O}$

$\overline{I_O}$ is the complementary current output terminal.

I_{REF}

I_{REF} is the full-scale current adjustment terminal. Normally, a resistance of 800 Ω is set between this terminal and GND_A. (When V_{REF} is 2.0 V, the full-scale current I_{FS} is 10 mA typ.)

V_{REF}

V_{REF} is the reference voltage input terminal. Normally, the input level is 2.0 V.

f_{COMP}

f_{COMP} is the terminal to which a frequency compensation capacitor should be connected. Normally, a capacitance of 1.0 μF is set between this terminal and GND_A.

AV+

AV+ is the power supply terminal (+5 V) for an analog system.

GND_A

GND_A is the ground terminal for an analog system.

V+

V+ is the power supply terminal (+5 V) for a digital system.

GND_D

GND_D is the ground terminal for a digital system.

NC

NC is a non-connection terminal, but normally it is connected to GND_A.

Recommended Operating Conditions

T_A = −20 to +75 °C

Parameter	Symbol	Limit Min.	Typ.	Max.	Unit	Test Conditions
Power supply voltage	V+, AV+	4.5	5.0	5.5	V	
Reference voltage	V_{REF}	1.8	2.0	2.2	V	
Reference resistance	R_{REF}		800		Ω	
Sampling clock	f_{SAMP}	DC		20	MHz	
Sampling clock low level pulse width	t_{PWL}	10			ns	
Sampling clock high level pulse width	t_{PWH}	10			ns	
Data set up time	t_S	20			ns	
Data hold time	t_H	10			ns	
Digital input high level	V_{IH}	2.7			V	
Digital input low level	V_{IL}			0.4	V	
Compensation capacitance	C_{COMP}	1.0			μF	

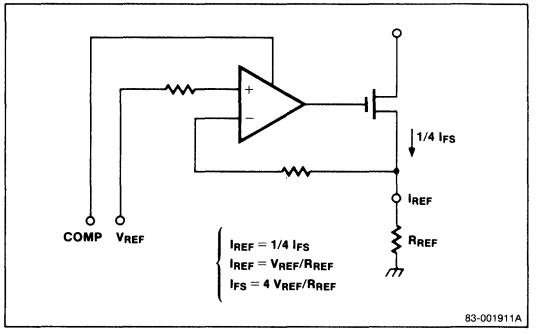
Electrical Characteristics

T_A = −20 to +75 °C, V+ = AV+ = 5 V ± 10%

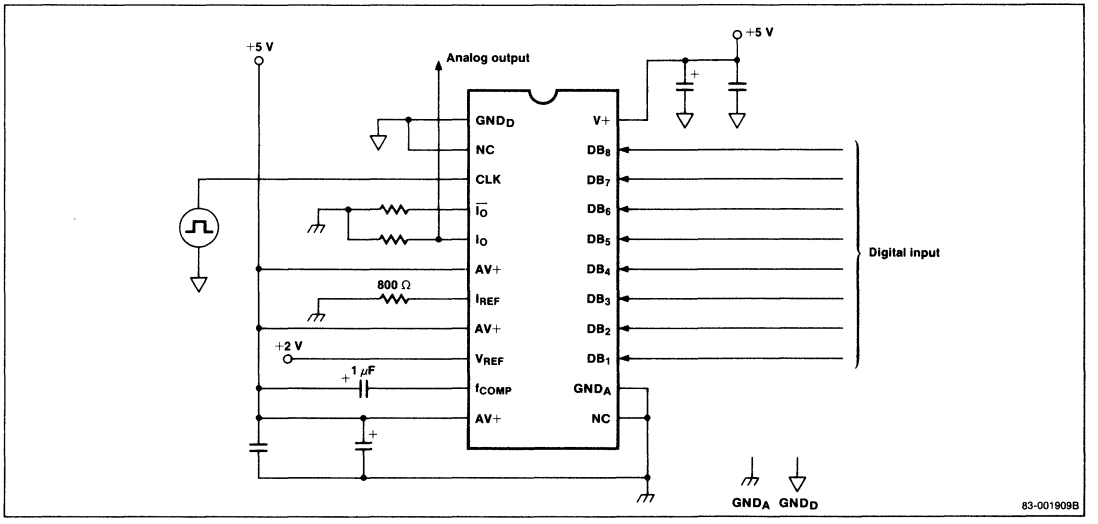
Parameter	Symbol	Limit Min.	Typ.	Max.	Unit	Test Conditions
Power supply current	I+		30	50	mA	
Resolution			8		bit	
Non-linearity error	NL		±1/2	±1	LSB	
Differential non-linearity	DNL		±1/2	±1	LSB	
Differential gain	DG		3	4	%	f_{SAMP} = 14.318 MHz
Differential phase	DP		1	3	°	f_{SAMP} = 14.318 MHz
Output compliance	V_O	2.5	3.0		V	V+ = 5.0 V
Analog output delay time	t_d		40		ns	
Settling time	t_{SET}		40		ns	
Full-scale current	I_{FS}	9	10	11	mA	
Zero-scale offset current	I_{ZS}			20	μA	
Digital input capacitance	C_{IN}			30	pF	
Digital input current	I_{IN}			10	μA	

Typical Applications

Full-Scale Current (I_{FS}) Setting Method



Test Circuit



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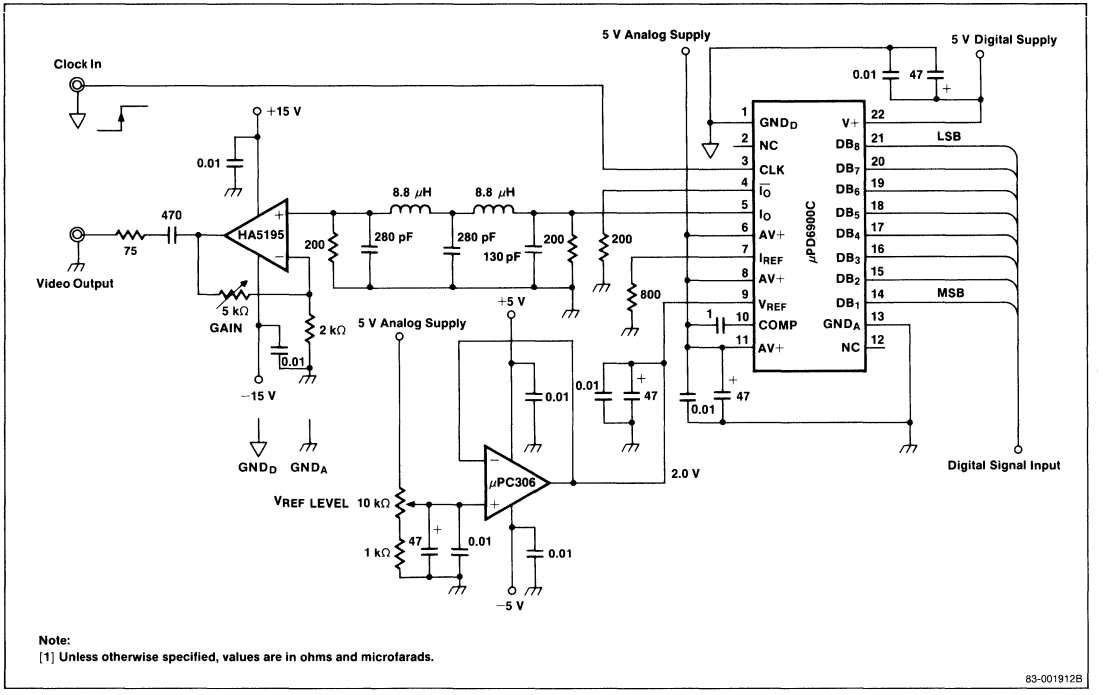
Typical Applications (Cont.)

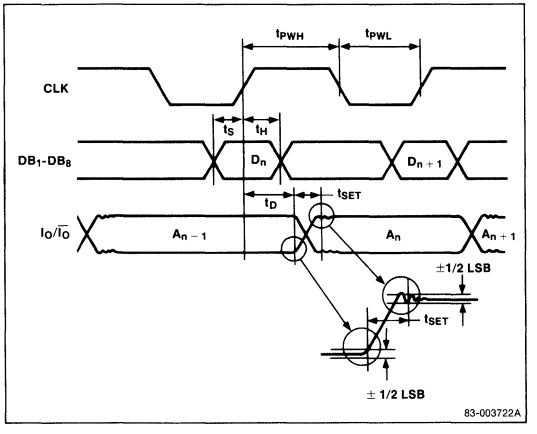
Application Circuit



Note:
[1] Unless otherwise specified, values are in ohms and microfarads.

83-001912B

Timing Waveforms



83-003722A

μPD7011
8-BIT NMOS D/A CONVERTER

Description

The μPD7011 is a low cost 8-bit NMOS digital-to-analog converter featuring single +5 V power supply operation and on board voltage reference. The serial interface option allows easy interface to the μCOM-43, -87, and -75 series of single chip microcomputers and the μPD7720 Signal Processing chip (SPI). In parallel mode the μPD7011 is easily connected to the 8080 and 8085 type bus structures by the bus interface facilities.

Features

- ☐ Single +5 V power supply
- ☐ Internal voltage reference
- ☐ Complementary current output
- ☐ Wide output compliance (2.4 V to 8 V)
- ☐ Serial interface with μCOM-43, -87, -75 and μPD7720 (SPI)
- ☐ Bus interface with 8080 and 8085A-2
- ☐ Pure binary and 2's complement code available in serial mode
- ☐ MSB 1st and LSB 1st serial input available
- ☐ Applications: CPU peripherals, toys, displays, instrumentation, speech synthesis
- ☐ Two performance ranges linearity error: μPD7011C, 1 LSB; μPD7011C-1, 1/2 LSB

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7011C	Plastic DIP	−20°C to +70°C

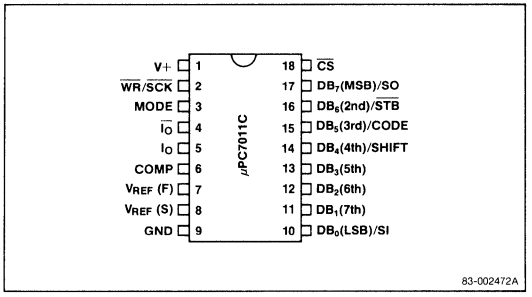
Absolute Maximum Ratings

$T_A = 25°C$

Operating Temperature	−20°C to +70°C
Storage Temperature	−65°C to +125°C
All Input Voltages	−0.3 to V_{DD} + 0.3 V
Power Supply	−0.3 V to +7.0 V
Power Dissipation	300 mW
SO Pin Pull-up Voltage	V_{DD} + 0.3 V
$I_O/\overline{I_O}$ Output Pull-up Voltage	+10 V

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration

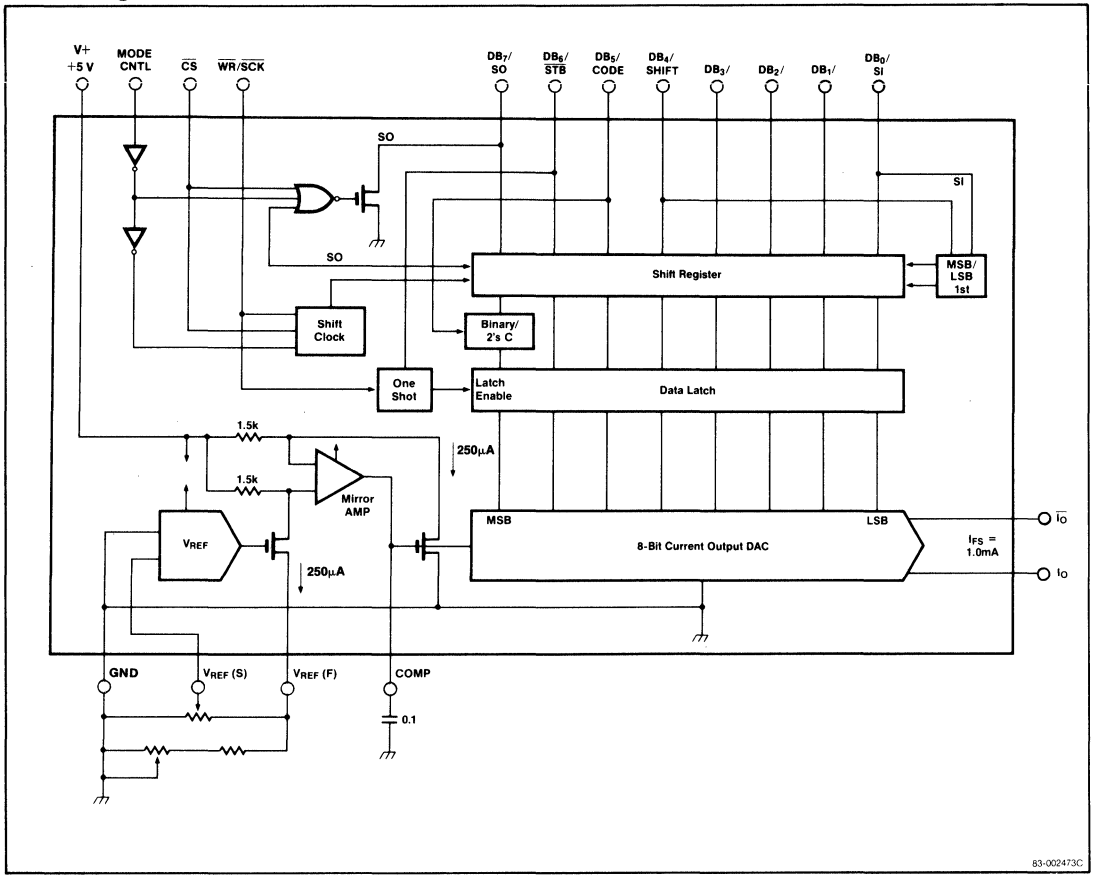


Pin Identification

Pin	Name	Function
1	V+	+5 V power supply
2	WR/SCK	WR: write SCK: serial shift clock
3	MODE	High: serial input mode Low: parallel bus input mode
4	$\overline{I_O}$	Complementary current outputs (open drain)
5	I_O	
6	COMP	Frequency compensation
7	$V_{REF}(F)$	Voltage reference output
8	$V_{REF}(S)$	Reference sense
9	GND	Digital analog common GND
10	DB_0/SI	Serial data input (serial) LSB input (bus)
11	DB_1	7th bit input (bus)
12	DB_2	6th bit input (bus)
13	DB_3	5th bit input (bus)
14	DB_4/SHIFT	Shift select; High: MSB 1st Low: LSB 1st 4th bit input (bus)
15	DB_5/CODE	High: 2s complement code Low: pure binary code 3rd bit input (bus)
16	$DB_6/\overline{STB}$	Strobe input 2nd bit input (bus)
17	DB_7/SO	Serial output (open drain) MSB input (bus)
18	$\overline{CS}$	Chip select

6

Block Diagram



DC Characteristics

$T_A = 25°C \pm 2°C$; $I_{FS} = 1$ mA;
$C_{COMP} = 0.1\ \mu F$; $V+ = 5\ V \pm 5\%$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	8	8	Bits	−20°C to +70°C
Nonlinearity, 7011C-1	NL		0.25	0.5	LSB	−20°C to +70°C
Nonlinearity, 7011C	NL		0.5	1	LSB	−20°C to +70°C
Differential Nonlinearity	DNL		0.1	0.1	LSB	−20°C to +70°C
Zero-Scale Error				0.5	LSB	−20°C to +70°C
Zero-Scale Symmetry		−1.5	−1.0	0.5	LSB	Note 1
Gain Error, 7011C-1				3	%FSR	Note 2
Gain Error, 7011C				5	%FSR	Note 2
Full-Scale Symmetry		−1.5	−1.0	−0.5	LSB	Note 3
Reference Voltage	V_{REF}	1.41	2.0	2.59	V	
Power Supply Current	I_{DD}		8	13	mA	
Logic Input Leakage	I_{ILK}		0.1	10	μA	$0 \le V_{IN} \le V+$
Low-Level Output Voltage	V_{OL}			0.5	V	SO (Pin 17) $I_{SINK} \le 2$ mA
Output Leakage	I_{OH}		0.1	10	μA	SO (pin 17) $V_O = V+$
Full-Scale Drift			70		PPM/°C	$\Delta I_{FS}/\Delta T$
Supply Voltage 7011C-1 Rejection Ratio	SVRR			0.8	%FSR/V	$\Delta I_{FS}/\Delta T$
Supply Voltage 7011C Rejection Ratio	SVRR			1.2	%FSR/V	$\Delta I_{FS}/\Delta V+$
Analog Output Compliance		2.4		8.0	V	$\Delta I_O(FS) \le$ 1 LSB

Notes: 1. Zero-scale symmetry is defined as follows: $255(I_O(ZS) - \overline{I_O(ZS)}/I_O(FS)$.
2. Gain error is defined as follows: $100(I_O(FS) \times 256/255 - 4I_{REF})/4I_{REF}$.
3. Full-scale symmetry is defined as follows: $255(I_O(ZS) - \overline{I_O(ZS)})/I_O(FS)$.

Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit
Supply Voltage	V+	4.75	5.0	5.25	V
Reference Current	I_{REF}	225	250	275	μA
Full-Scale Current	I_{FS}	0.9	1.0	1.1	mA
Reference Force Terminal Voltage	V_{REF}	2.65	2.7	2.75	V
Low-Level Logic Input	V_{IL}	0		0.8	V
High-Level Logic Input	V_{IH}	2.0		V+	V
Analog Output Pull-up Voltage	V_P	2.4		3.0	V
SO Pin 17 Output Pull-up Voltage	V_{OP}			V+	V
Frequency Compensation Capacitor (See Note)	C_{COMP}	0.01	0.1	1.0	μF

Note: Using a frequency compensation capacitor larger than 1 μF will promote low noise operation of the μPD7001C. However, the turn-on time at initial power on will increase.

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AC Recommended Conditions

$T_A = 25°C \pm 2°C$;
$V+ = 5\ V \pm 0.25\ V$; Note 1

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Serial Mode						
Serial Clock Setup Time	t_{SKCS}	30			ns	$\overline{SCK}\uparrow \rightarrow \overline{CS}\downarrow$
CS Setup Time	t_{SCSK}	300			ns	$\overline{CS}\downarrow \rightarrow \overline{SCK}\uparrow$
Data Setup Time	t_{SIK}	120			ns	$SI \rightarrow \overline{SCK}\uparrow$
Data Hold Time	t_{HKI}	50			ns	$\overline{SCK}\uparrow \rightarrow SI$
High-Level Serial Clock Pulse Width	t_{WHK}	300			ns	
Low-Level Serial Clock Pulse Width	t_{WLK}	300			ns	
Strobe Hold Time	t_{HKST}	100			ns	$\overline{SCK}\uparrow \rightarrow \overline{STB}\uparrow$
High-Level Strobe Pulse Width	t_{WHST}	200			ns	
Low-Level Strobe Pulse Width	t_{WLST}	200			ns	
Chip Select Hold Time	t_{HKCS}	0			ns	$\overline{SCK}\uparrow \rightarrow \overline{CS}\uparrow$
Serial Clock Hold Time	t_{HCSK}	100			ns	$\overline{CS}\uparrow \rightarrow \overline{SCK}\downarrow$
Strobe Setup Time	t_{SSTCS}	300			ns	$\overline{STB}\uparrow \rightarrow \overline{CS}\downarrow$
Parallel Mode						
Address Setup Time	t_{AW}	0			ns	$\overline{CS}\downarrow \rightarrow \overline{WR}\downarrow$
Low-Level WR Pulse Width	t_{WW}	200			ns	
Address Hold Time	t_{WA}	0			ns	$\overline{WR}\uparrow \rightarrow \overline{CS}\uparrow$
Data Setup Time	t_{DW}	180			ns	$DB \rightarrow \overline{WR}\uparrow$
Data Hold Time	t_{WD}	0			ns	$\overline{WR}\uparrow \rightarrow DB$

Note: t_r, $t_f \leq 50$ ns.

AC Characteristics

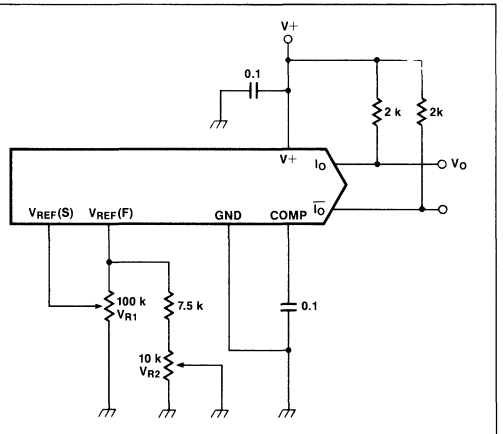
$T_A = 25°C \pm 2°C$; $V+ = +5\ V$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Analog Output Setting Time	t_{SET1}		1	3	μs	Parallel Mode, Note 1
	t_{SET2}		1	3	μs	Serial Mode, Note 2
Serial Data Delay Time	t_{DKO}			450	ns	SCK ↓ → SO, Note 2
Delay Time T_D Floating S_O	t_{FCSO}			250	ns	CS ↑ → SO, High Impedance

Notes: 1. $R_L \leq 2\ k\Omega$; $C_L \leq 20$ pF.
2. $R_L = 2\ k\Omega$; $C_L \leq 20$ pF.

Typical Applications

Connection Diagram



Notes: 1. Use resistors of 1% accuracy.
2. Capacitive load at $V_{REF}(F)$ pin should be less than 15 pF.
3. Adjustment Procedure
   a. Set $V_{REF}(F) = 2.7$ V by V_{R1}.
   b. After latching full-scale digital input, set $V_O = 2.0$V by V_{R2}.

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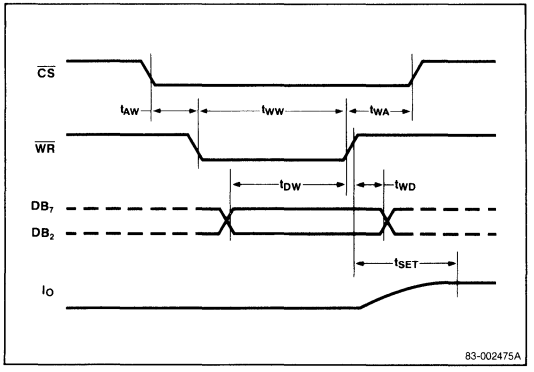
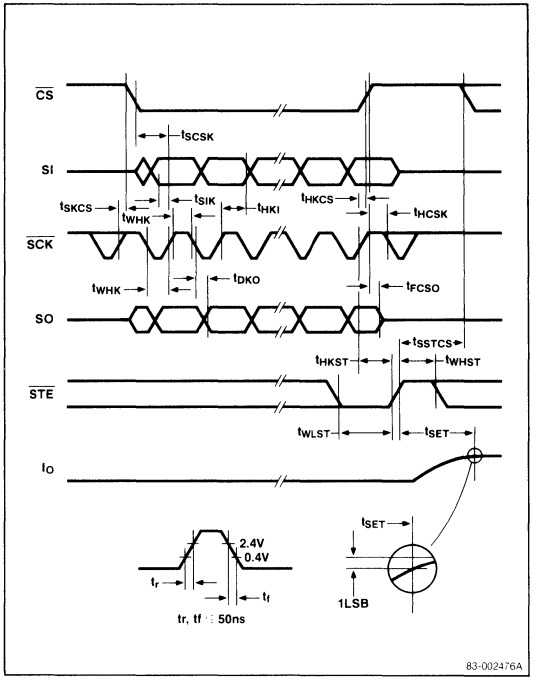
Timing Waveforms

Parallel Mode



Serial Mode



6

NEC

NEC Electronics Inc.

μPD6950
8-BIT CMOS VIDEO A/D CONVERTER

PRELIMINARY INFORMATION

Description

The μPD6950 is an 8-bit A/D converter for video signals. Although it is a CMOS converter (V+ = 5 V), its conversion rate is very high because a high-speed CMOS processing technique and full-parallel (flash) conversion method are used.

With its low power consumption and conversion rate of 20 Msps, this converter can be applied to various units such as digital video processing systems and high-speed fascimiles.

Features

- ☐ Resolution: 8 bits
- ☐ Conversion rate: 20 Msps (V+ = 5 V)
- ☐ Linearity: ±1/2 LSB typ
- ☐ Reference voltage: 3.5 V typ
- ☐ Power supply: 5 V single
- ☐ Low power consumption (350 mW typ)
- ☐ Available in 24 lead DIP

Absolute Maximum Ratings

$T_A = 25°C$

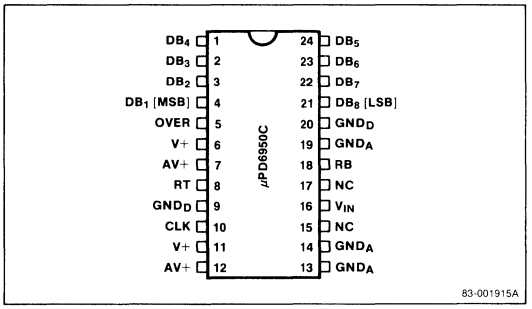
Power Supply Voltage	−0.3 to +7.0V
Input/Output Terminal Voltage	−0.3 to V_{DD}+0.3V
Analog GND Voltage	−0.3 to V_{IN} +0.3V
Reference GND Voltage	−0.3 to +0.3V
Operating Temperature Range	−20 to +75°C
Storage Temperature Range	−40 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ordering Information

Part Number	Package	Operating Temperature Range
μPD6950C	Plastic DIP	−20°C to +75°C

Pin Configuration

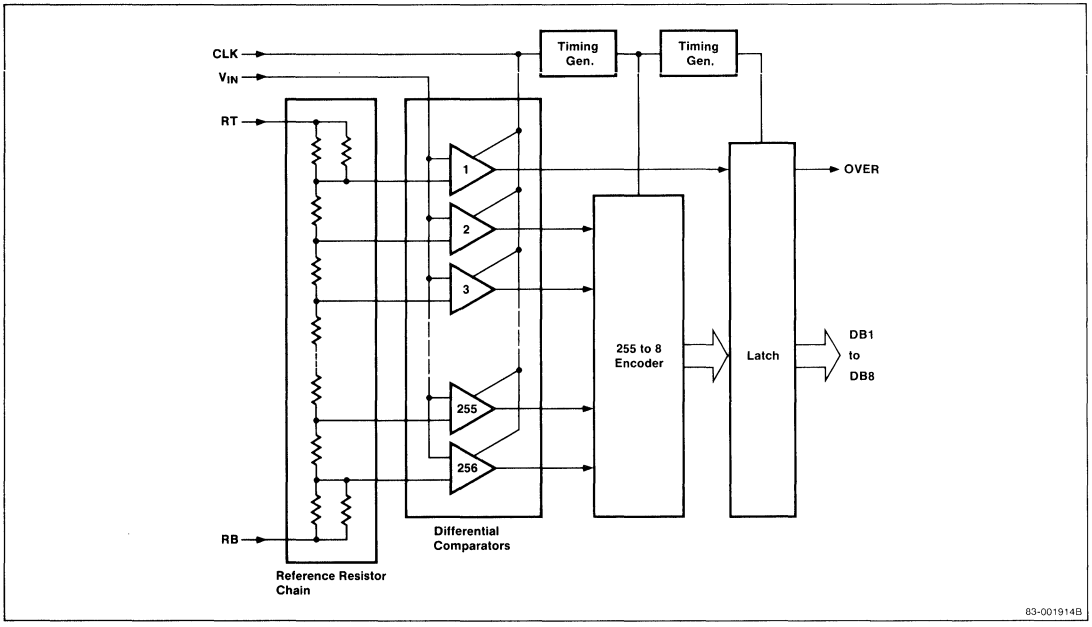


Pin Identification

Pin	Symbol	Function
1	DB_4	Digital output 4th
2	DB_3	Digital output 3rd
3	DB_2	Digital output 2nd
4	DB_1	Digital output MSB
5	OVER	Overrange
6	AV+	Analog power supply
7	V+	Power supply
8	RT	Reference voltage (high voltage side)
9	GND_D	Digital GND
10	CLK	Clock input
11	V+	Power supply
12	AV+	Analog power supply
13	GND_A	Analog GND
14	GND_A	Analog GND
15	NC	No connection
16	VIN	Analog input
17	NC	No connection
18	RB	Reference voltage (low voltage side)
19	GND_A	Analog GND
20	GND_D	Digital GND
21	DB_8	Digital output LSB
22	DB_7	Digital output 7th
23	DB_6	Digital output 6th
24	DB_5	Digital output 5th

6

Block Diagram



Electrical Characteristics

T_A = 25 °C, V+ = AV+ = 5V, sampling rate = 20 MHz

Item	Symbol	Limit Min.	Typ.	Max.	Unit	Test Conditions
Current Consumption	I_{DD}		50		mA	
Resolution	RES		8		bit	
Non-Linearity	NL			1.5	LSB	V_{REF} =3.5V
Differential Gain	DG			5	%	f_{SAMP}=14.318 MHz
Differential Phase	DP			5	°	f_{SAMP}=14.318 MHz
Reference Resistance	R_{ref}		1.5		kΩ	
Data Output High-Level Current	I_{OH}			1.0	mA	V_{OH} = 2.5V
Data Output Low-Level Current	I_{OL}	1.8			mA	V_{OL} = 0.4V

Recommended Operating Conditions

T_A = 25 °C

Item	Symbol	Limit Min.	Typ.	Max.	Unit	Test Conditions
Power Supply Voltage	V+, AV+	4.5	5.0	5.5	V	
Reference Voltage	V_{REF}	2.5	3.5	3.5	V	
Sampling Clock	f_{SAMP}			20	MHz	
CLK Input High Level	V_{IH}	2.7			V	
CLK Input Low Level	V_{IL}			0.4	V	
Output Code			Binary			

Pin Functions

DB_1 to DB_8

DB_1 to DB_8 are the 8-bit digital signal output terminals. The analog signal input to terminal 16 (analog input terminal) is converted and sent from these terminals as an 8-bit digital signal. DB_1 corresponds to MSB, and DB_8 corresponds to LSB.

OVER

OVER is the overflow output terminal. When the analog input level (terminal 16) exceed the value of V_{OVER}, a high level is sent from this terminal.

(V_{OVER} = (255 + 1/2) LSB, 1LSB = (V_{RT}-V_{RS})/256

CLK

CLK is the A/D conversion clock input terminal. The analog data is latched on the rising edge of this clock. The internal encoder and latch circuit operations are synchronized with the timing pulses generated by this clock.

VIN

VIN is the analog input terminal. The analog signal to this terminal is converted on the rising edge of the CLK input clock and is sent from terminals DB_1 to DB_8 as an 8-bit digital signal.

RT

RT is the reference voltage input terminal on the high voltage side. It is the V_{REF} input terminal.

RB

RB is the reference voltage input terminal on the low voltage side. Normally, 0V is applied to this terminal.

AV+

AV+ is the power supply terminal for an analog system.

V+

V+ is the power supply terminal for a digital system.

GND_A

GND_A is the ground terminal for an analog system.

GND_D

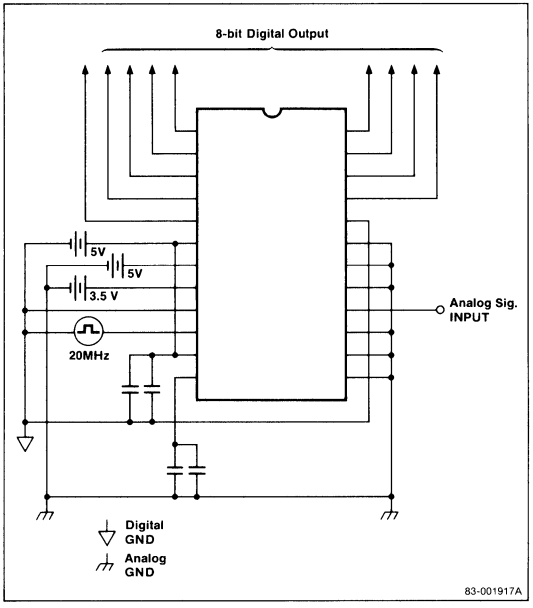
GND_D is the ground terminal for a digital system.

NC

NC is a non-connection terminal, but normally, it is connected to GND_A.

Typical Applications

Test Circuit



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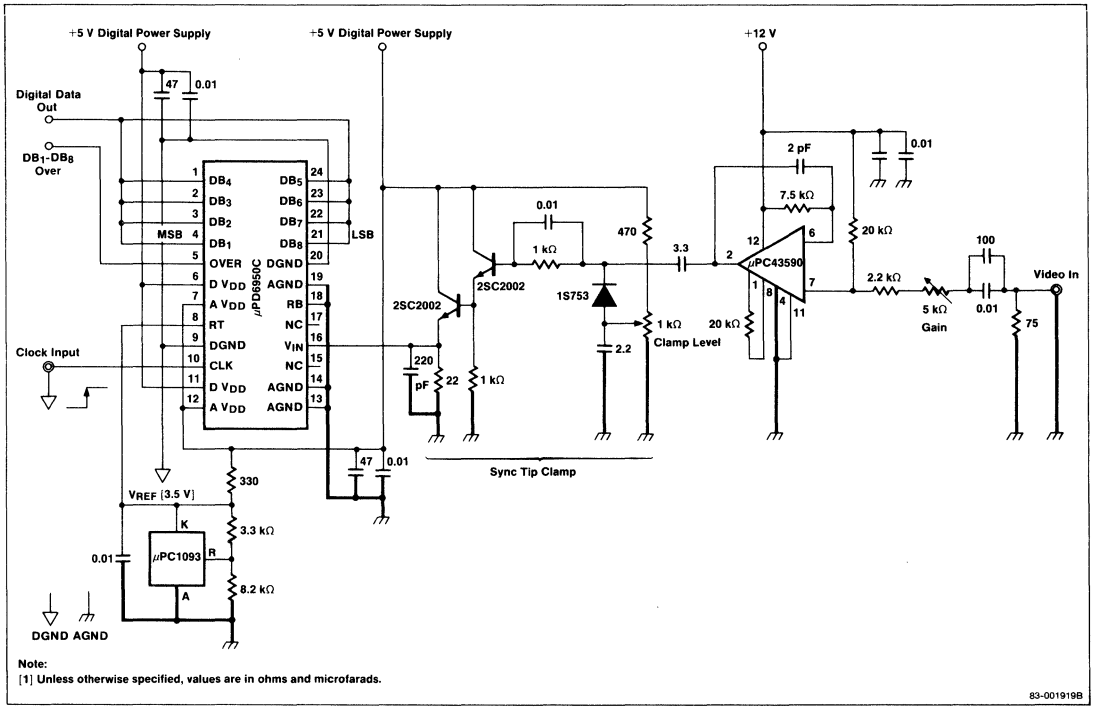
Typical Applications (Cont.)

Application Circuit



Note:
[1] Unless otherwise specified, values are in ohms and microfarads.

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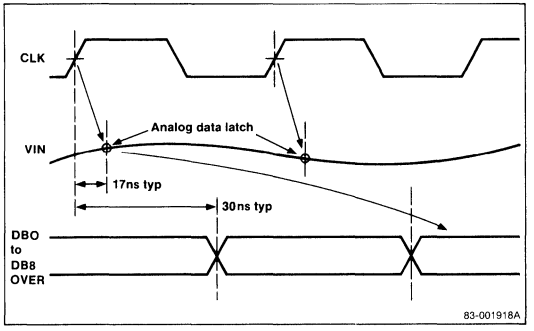
Timing Waveform



Output Data Format

Analog input	Digital output								
	OVER	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8
V_{RB} to 1/2 LSB	0	0	0	0	0	0	0	0	0
1/2 LSB to 1+1/2 LSB	0	0	0	0	0	0	0	0	1
254 + 1/2 LSB to 255 + 1/2 LSB	0	1	1	1	1	1	1	1	1
255 + 1/2 LSB to V_{RT}	1	1	1	1	1	1	1	1	1
V_{RT} to V+	1	1	1	1	1	1	1	1	1

$$LSB \fallingdotseq \frac{V_{RT} - V_{RB}}{256}$$

6

NEC
NEC Electronics Inc.

μPD7001
8-BIT CMOS SERIAL OUTPUT A/D CONVERTER

Description

The μPD7001 is a high performance, low power, 8-bit CMOS analog-to-digital converter. Using the Successive Approximation Register (SAR) technique, the 7001 offers the designer the convenience of serial data output and microprocessor interface, with the versatility of four addressable multiplexed analog inputs and low power CMOS operation.

Features

- ☐ 4 channel multiplexed analog input
- ☐ Auto zero and full scale correction without external components
- ☐ Serial data output
- ☐ High input impedance 1000 MΩ
- ☐ Operates from a single +5 V supply
- ☐ Low power operation (CMOS)
- ☐ 140 μs conversion speed
- ☐ Linearity: 0.8% FSR

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7001C	Plastic DIP	0°C to +70°C

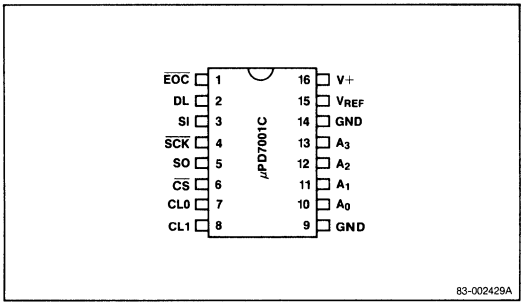
Absolute Maximum Ratings

$T_A = 25°C$

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to 125°C
Analog Input Voltage	−0.3 V to V+ + 0.3 V
Reference Input Voltage	−0.3 V to V+ + 0.3 V
Digital Input Voltage	−0.3 V to +12 V
Maximum Pull-up Voltage	+12 V
Supply Voltages	−0.3 V to +7 V
Power Dissipation	200 mW

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



Pin Identification

Pin	Name	Symbol	Function
1	End of Conversion	EOC	High impedance when $\overline{CS}$ = Low. Open drain output.
2	Data Latch	DL	MPX addresses are latched at the falling edge of DL input.
3	Serial Input	SI	Pin to accept MPX address data. Data read at the rising edge of $\overline{SCK}$ input.
4	Serial Clock	$\overline{SCK}$	$\overline{SCK}$ controls the shift operation of I/O interface 8-bit shift register. Input.
5	Serial Output	SO	Conversion data in shift register are output at the falling edge of $\overline{SCK}$. High impedance when $\overline{CS}$ = High. Open drain output.
6	Chip Select	$\overline{CS}$	$\overline{CS}$ = High: A/D conversion mode $\overline{CS}$ = Low: Interface mode. Input.
7	Clock	CL0	Pin for clock oscillation.
8	Clock	CL1	Pin for clock oscillation.
9	Digital Ground	V_{SS}	Ground terminal. Tie to GND with analog GND externally.
10-13	Analog Inputs	A_0 to A_3	Analog input terminals.
14	Analog GND	GND	Ground terminal for analog inputs and references.
15	Reference Input	V_{REF}	Pin to set full scale voltage. $V_{REF} \sim 2.5$ V.
16	Power Supply	V+	+5 V

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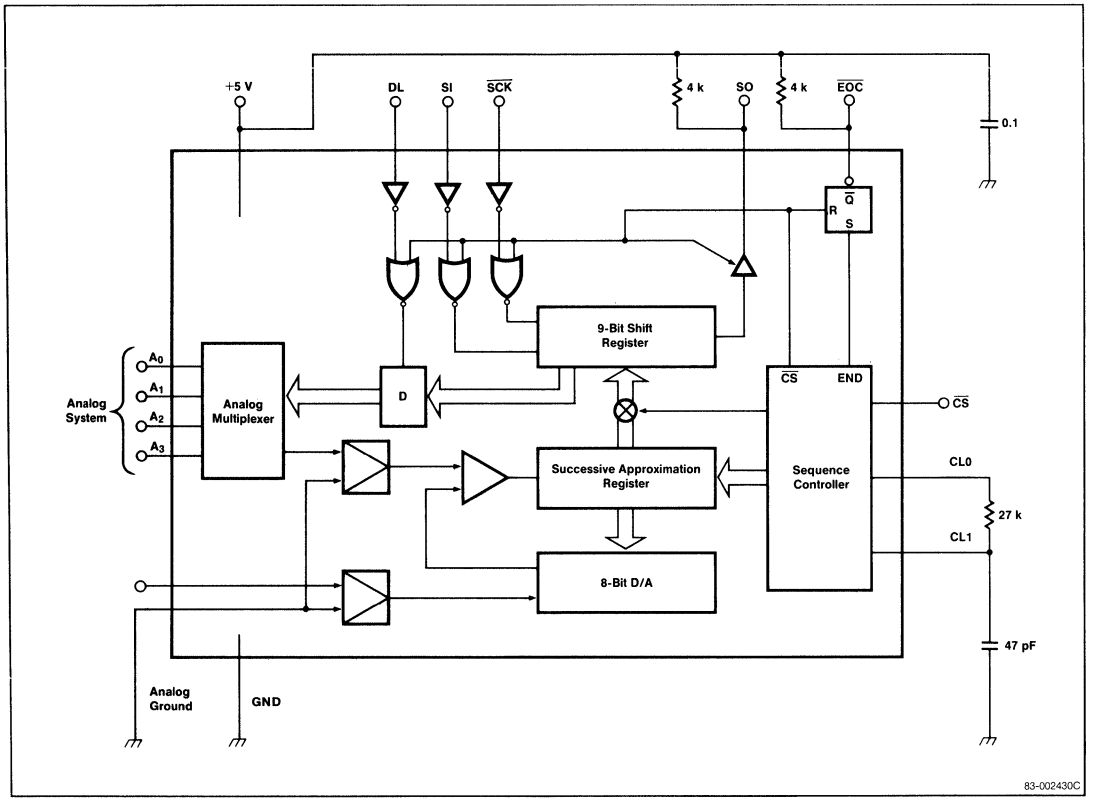
Block Diagram



DC Characteristics

$T_A = +25°C \pm 2°C$; $f_{clk} = 400$ kHz; V+ = 5 V, ±0.25 V, $V_{REF} = 2.500$ V, Note 1

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution				8	Bit	
Nonlinearity	NL			0.8	%FSR	
Full-Scale Error			1	2	LSB	
Full-Scale Error Temperature Coefficient			30		ppm/°C	
Zero Error				2	LSB	
Zero Error Temperature Coefficient			30		ppm/°C	
Total Unadjusted Error 1	TUE1			2	LSB	Note 4
Total Unadjusted Error 2	TUE2			2	LSB	Note 5
Analog Input Voltage	V_{IN}	0		V_{REF}	V	Note 1
Analog Input Resistance	R_{IN}		1000		MΩ	V_I = 0 to V
Conversion Time	t_{CONV}		140		μs	Note 2
Clock Frequency Range	f_{clk}	0.01	0.4	0.5	MHz	
Clock Frequency Distribution	Δf_{clk}		±5	±20	%	R = 27 KΩ, C = 47 pF, f_{CK} = 400 kHz
Serial Clock Frequency	t_{SCK}		0.5		MHz	Note 3
High Level Voltage	V_{IH}	3.6			V	
Low Level Voltage	V_{IL}			1.4	V	
Digital Input Leakage Current	I_{ILK}		1.0	10	μA	$V_I = V_{SS}$ to +10 V
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.7 mA
Output Leakage Current	I_{OLK}		1.0	10	μA	V_O = +10 V
Power Dissipation	P_D		5	15	mW	

Notes: 1. All digital outputs are put at a high level when $V_I > V_{REF}$.

2. A/D conversion is started with $\overline{CS}$ going high; at the final step of the first A/D conversion, $\overline{EOC}$ is low. The conversion time is:
$$t_{CONV} = 56/f_{CK}$$

3. For $f_{SCK} < 500$ kHz, the load capacitor (stray capacitance included) and the pull-up resistor, which are connected to serial output, are required to be not more than 30 pF and 4 kΩ respectively.

4. V+ = 5.0 V, $V_{REF} = 2.5 \pm 0.25$ V.

5. V+ = 4.5 to 5.5 V.

6

AC Characteristics

$T_A = +25°C \pm 2°C$; $f_{clk} = 400$ kHz; V+ = 5 V, Note 1

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
$\overline{EOC}$ Hold Time	t_{HECS}	0			μs	$\overline{EOC}$ to $\overline{CS}$
$\overline{CS}$ Setup Time	t_{SCSK}	12.5			μs	$\overline{CS}$ to $\overline{SCK}$ Note 1
Address Data Setup Time	t_{SIK}	150			ns	
Address Data Hold Time	t_{HKI}	100			ns	
High Level Serial Clock Pulse Width	t_{WHK}	400			ns	
Low Level Serial Clock Pulse Width	t_{WCK}	400			ns	
Data Latch Hold Time	t_{HKDL}	200			ns	$\overline{SCK}$ to DL
Data Latch Pulse Width	t_{DKO}	200			ns	
Serial Data Delay Time	t_{DKO}			500	ns	$\overline{SCK}$ to SO, $R_L = 3$ K (Note 2), $C_L = 30$ pF
Delay Time to Floating SO	t_{FCSO}			250	ns	$\overline{CS}$ to High Impedance SO
$\overline{CS}$ Hold Time	t_{HKCS}	200			ns	

Notes: 1. When $\overline{CS}$ is high, the μPD7001 performs A/D conversion and does not accept any external digital signal. It remains at the previous state continuously. When $\overline{CS}$ is low, the data is exchanged with the external digital circuits. However, 5 internal clock pulses are needed before digital data is output. The rating corresponds to the 5 clock signal pulses:

$$t_{SCSK}\ (\text{min}) = 5/f_{clk}$$

2. The serial data delay time depends on load capacitance and pull-up resistance: $t_{DKO} = 2.3 \times R_L \times C_L + 100$ ns.

Addressing the Inputs

One of the four analog inputs is selected by toggling the chip select line at pin 6 "low" and presenting a 2-bit serial code (from the host controller) to the Serial Input (SI) at pin 3.

The "channel select" data is sent to the upper 2 bits of the 9-bit shift register on the rising edge of the Serial Clock ($\overline{SCK}$) at pin 4 and loaded into the Data Latch on the falling edge of the Data Latch signal at pin 2.

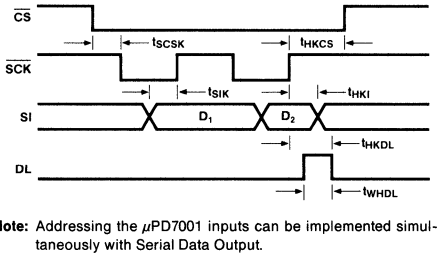
Referring to figure 1 the analog input addressing sequence is:

- ☐ Chip Select ($\overline{CS}$ pin 6) toggled "low" or 0
- ☐ 2-bit "channel select" data presented to SI and pin 3
- ☐ Data shifted in on $\overline{SCK}$ rising edge
- ☐ Data Latch signal present at pin 2 (pulse is 200 ns min.)
- ☐ Mux address data latched on falling edge of DL signal.

Multiplexer Channel Selection

Input	D0	D1
A0	Low	Low
A1	High	Low
A2	Low	High
A3	High	High

Figure 1. Analog Channel Selection



Note: Addressing the μPD7001 inputs can be implemented simultaneously with Serial Data Output.

Rise and Fall times of all signals should not exceed 50 ns.

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The Conversion Process

When Chip Select ($\overline{CS}$) at pin 6 is "high," all external inputs (except the selected analog input) and outputs are disabled and the internal Sequence Controller controls the conversion process on the selected analog input via the A/D converter section.

The A/D converter section is comprised of the comparator and buffer amplifier, the successive approximation register and an 8-bit digital to analog (D/A) converter. Because the SAR technique requires the input voltage be stable during the conversion process, it is recommended that a low pass filter and a sample and hold circuit precede the analog input. Failure to present stable input voltage will result in conversion errors.

A single conversion requires 56 internal clock periods, which are clock periods generated by the Sequence Controller Clock (CL0) and CL1 at pins 7 and 8 respectively. The internal clock speed is set by Rcl and Ccl and the values shown in figure 2 are recommended for proper timing.

The final step in the conversion process is the transfer of converted data to the shift register and signaling (to the external controlling device) that the converted data is available for reading, via the End of Conversion ($\overline{EOC}$) pulse at pin 1.

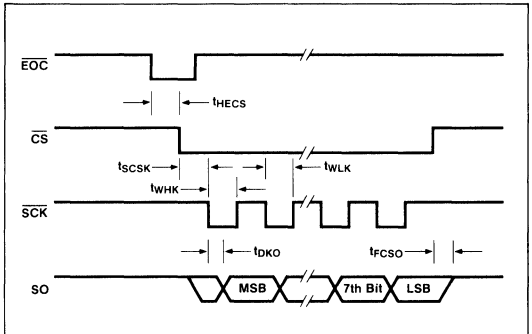
If the data is not to be read then the Chip Select ($\overline{CS}$) line is kept in the "high" state and the Sequence Controller begins the next conversion of the last selected analog channel. Note again that "channel select" data and "converted" data output can only be initiated while the Chip Select line is "low." The sequence of data conversion and output is shown in figure 2.

Sequence:

- ☐ Analog channel selection (1 of 4):
  $\overline{CS}$ = "low"
- ☐ Analog-to-digital conversion (internal):
  $\overline{CS}$ = "high"
- ☐ Internal load of "converted data" to shift register (56 internal clock cycles):
  $\overline{CS}$ = "high"
- ☐ $\overline{EOC}$ signals data ready to external controller:
  $\overline{CS}$ = "high"
- ☐ Output of serial data to controlling device and/or refresh of analog input select data:
  $\overline{CS}$ = "low"

Stability of the analog input voltage level is critical to the conversion accuracy of the μPD7001, as with any SAR type converter, during the conversion cycle. When $\overline{CS}$ is "high," the converter responds to whatever voltage level is present at the selected input. For DC level sampling from remote sensors a low pass filter (similar to that shown in figure 3) and a sample and hold circuit (such as the μPC398) is recommended.

Figure 2. Digital Data Output



Notes: Serial Data Output and Analog Channel Select Data input can be performed simultaneously.

Two bits of the 9-bit shift register are used to shift data into the multiplexer data latch between conversion/output cycles. Conflict between Address Data and Output Data is avoided by timing shown in Figures 1 and 2.

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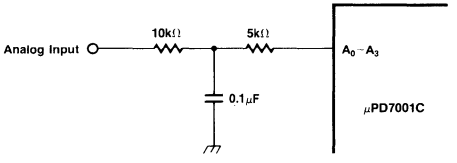
Figure 3. Low Pass Filter Circuit



Note: The data in the internal Data Latch and the internal Sequence Controller at "power on" is random. It is recommended that at "power on" the sequence controller be reset and the multiplex address setting be set prior to the first conversion read.

When long leads are used to connect external components to the μPD7001, noise and interference may alter the expected result. It is strongly recommended that trace and lead length be kept to a minimum for optimum performance.

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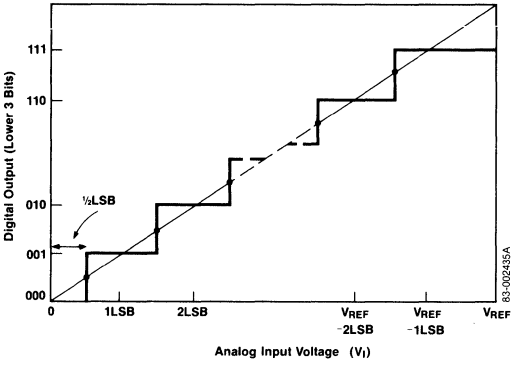
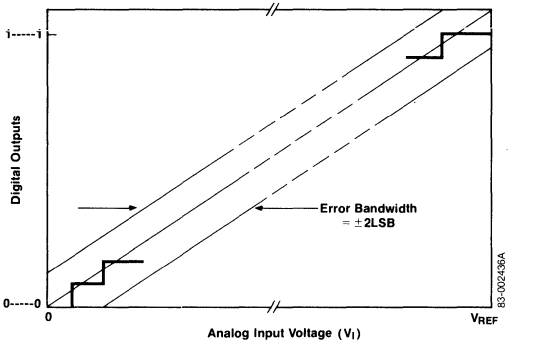
6

Operating Characteristics

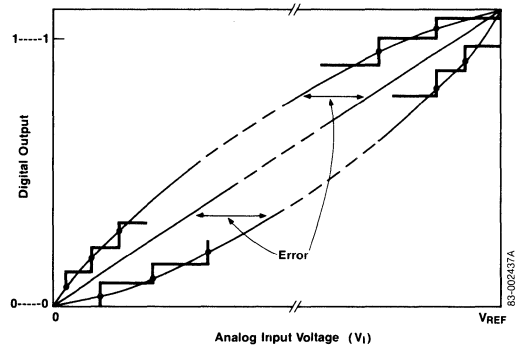
Ideal Input/Output Transfer Characteristics



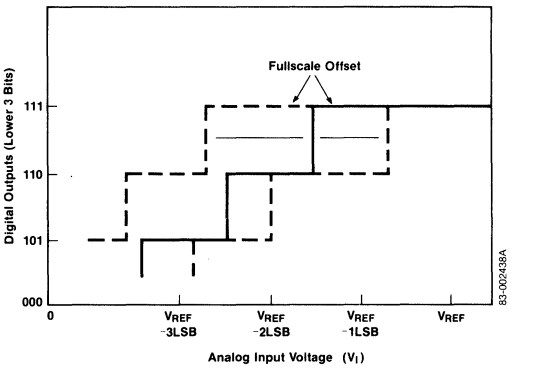
Total Unadjusted Error



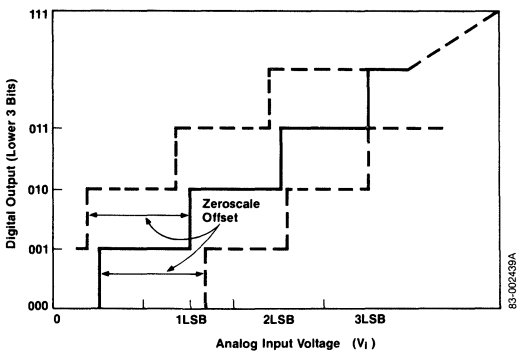
Linearity Error



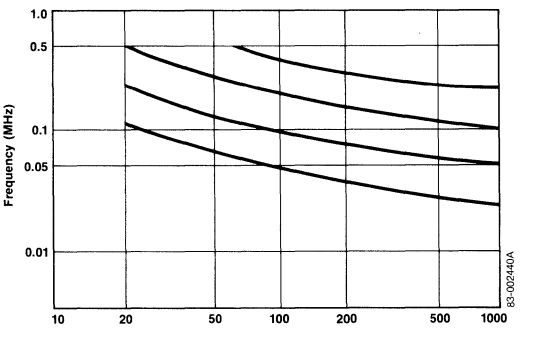
Full Scale Error



Zero Scale Error

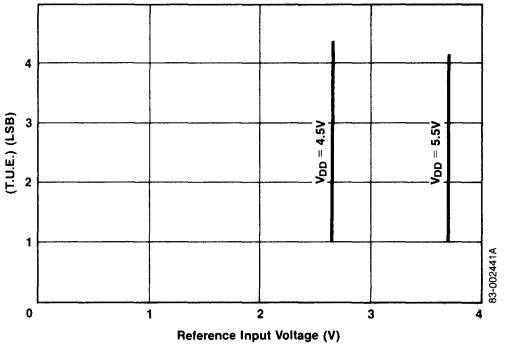


Clock Frequency Range

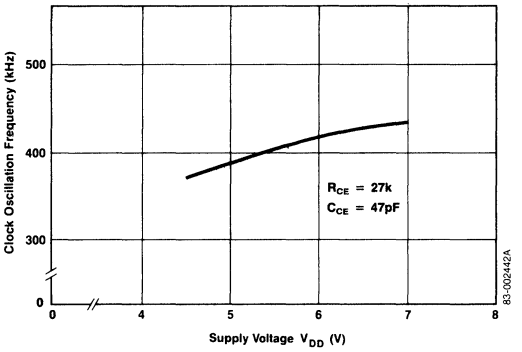


Operating Characteristics (Cont.)

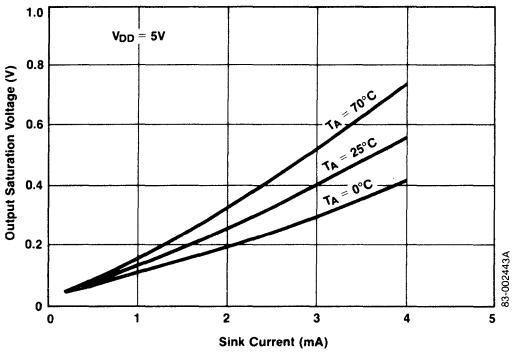
Total Unadjusted Error vs. V_{REF}



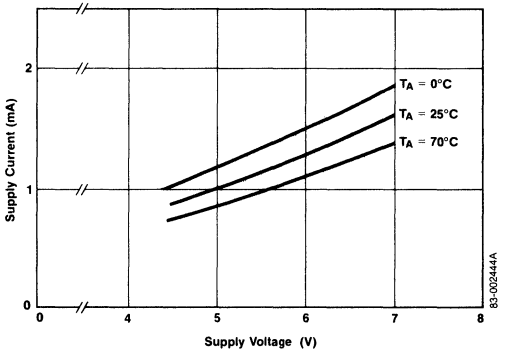
Clock Oscillation Frequency vs. Current Characteristics



Output Sink Current vs. Saturation Voltage Characteristics



Supply Voltage vs. Current Characteristics



6

μPD7002
10-BIT CMOS INTEGRATING A/D CONVERTER

Description

The μPD7002 is a high performance, low power, 10-bit CMOS analog-to-digital converter. Using the integrating technique the 7002 offers the designer full microprocessor interface, four multiplexed analog inputs, and low power CMOS construction.

Features

- ☐ 8- or 10-bit resolution (selectable)
- ☐ 4 channel multiplexed analog input
- ☐ Auto zero and full scale correction without external components
- ☐ High input impedance — 1000 MΩ
- ☐ Internal status register can be accessed by host controller
- ☐ Operates from single +5 V supply
- ☐ Interfaces to most 8-bit microprocessors
- ☐ Low power operation (CMOS)
- ☐ 5 ms conversion speed (10 bits with $f_{CK} = 2$ MHz)
- ☐ Available in two performance ranges:
  Conversion accuracy (maximum with $T_A = 0$ to +50°C):
  μPD7002C-1 ..... 0.1% FSR
  μPD7002C ..... 0.2% FSR

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7002C	Plastic DIP	−20°C to +70°C

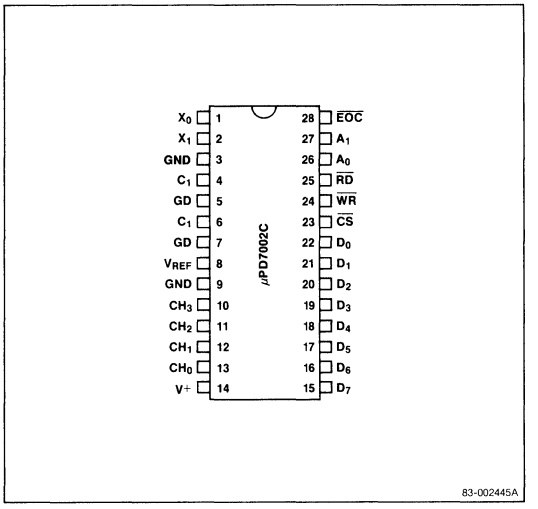
Absolute Maximum Ratings

$T_A = +25°C$

Operating Temperature	−20°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage	−0.3 V to +7.0 V
All Input Voltages	−0.3 V to V+ 0.3 V
Power Dissipation	300 mW
Analog GND Voltage	± 0.3 V

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



Pin Identification

Pin	Name	Function
1, 2	X_0, X_1	External clock input
3	GND	TTL ground
4, 6	CI	Integrating capacitor
5, 7	GD	Guard
8	V_{REF}	Reference voltage input
9	GND	Analog ground
10	CH_3	Analog channel 3
11	CH_2	Analog channel 2
12	CH_1	Analog channel 1
13	CH_0	Analog channel 0
14	V+	Voltage (+5 V)
15-22	D_7-D_0	Data bus
23	$\overline{CS}$	Chip select
24, 25	$\overline{WR}$, $\overline{RD}$	Control bus
26, 27	A_0, A_1	Address bus
28	$\overline{EOC}$	End of conversion interrupt

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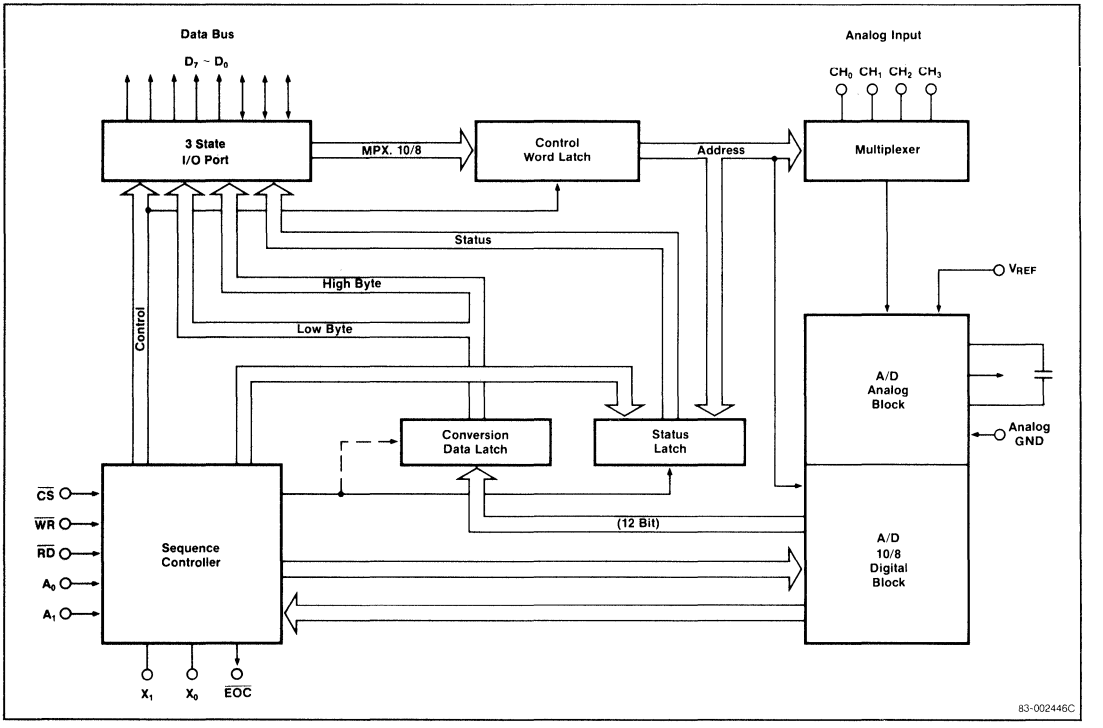
Block Diagram



Digital I/O Pin Function

Pin	Symbol	Name	I/O	Function
1, 2	X_0, X_1	Xtal	—	Xtal OSC. X_1 can be used as the input of external clock.
15–22	D_7–D_0	Data Bus	Three-state (1 TTL) I/O	A/D conversion data (High and Low Byte) and internal status output to 8-bit Data Bus. MPY Address, 8/10 select and flag data input from bus. High impedance when μPD7002 is not enabled ($\overline{CS}$ = High).
23	$\overline{CS}$	Chip Select	Input	Low level of $\overline{CS}$ makes other input pins ($\overline{WR}$, $\overline{RD}$, A_0, A_1) enable and data transmission and receiving are possible through data bus pins.
24	$\overline{WR}$	Write	Input	When $\overline{WR}$ = Low, μPD7002 receives new data from data bus.
25	$\overline{RD}$	Read	Input	When $\overline{RD}$ = Low, μPD7002 transmits conversion data and internal status to data bus.
26, 27	A_0, A_1	Address	Input	A_0, A_1 designate the data in data bus (High, Low, Status Byte).
28	$\overline{EOC}$	End of Conversion	Output (1 TTL)	$\overline{EOC}$ indicates the end of conversion to external chips. Read mode operation (high byte output) resetable $\overline{EOC}$.

DC Characteristics

$T_A = 0°C$ to $+50°C$; $V+ = +5\ V \pm 0.25\ V$
$V_{REF} = +2.50\ V$, $f_{clk} = 1\ MHz$, $C_{INT} = 0.033\ \mu F$, 10-Bit Mode

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution, 7002C-1		10	11	12	Bits	
Resolution, 7002C		9	11	12	Bits	
Nonlinearity, 7002C-1			0.05	0.1	%FSR	
Nonlinearity, 7002C			0.1	0.2	%FSR	
Full Scale Error, 7002C-1			0.05	0.1	%FSR	
Full Scale Error, 7002C			0.1	0.2	%FSR	
Zero Scale Error, 7002C-1			0.05	0.1	%FSR	
Zero Scale Error, 7002C			0.1	0.2	%FSR	
Full Scale Temperature Coefficient			10		ppm/°	
Zero Scale Temperature Coefficient			10		ppm/°C	
Analog Input Resistance	R_{IN}		1000		MΩ	$V_{IN} = 0$ to $V+$
Total Unadjusted Error 1, 7002C-1	TUE1		0.05	0.1	%FSR	
Total Unadjusted Error 1, 7002C	TUE1		0.1	0.2	%FSR	
Total Unadjusted Error 2, 7002C-1	TUE2		0.05	0.1	%FSR	
Total Unadjusted Error 2, 7002C	TUE2		0.1	0.2	%FSR	
Clock Input Current	I_{clk}		5	50	μA	X_I pin can be used as an external CMOS level clock input. When external clock is applied. X_O pin should be left open.
High Level Output Voltage	V_{OH}	$V+ - 1.5$			V	$I_O = -1.6\ mA$, $T_A = -20$ to $+70°C$
Low Level Output Voltage	V_{OL}			0.45	V	$I_O = 1.6\ mA$, $T_A = -20$ to $+70°C$
Digital Input Leakage Current	I_{ILK}		1	10	μA	$0 \le V_{IN} \le V+$
Output Leakage Current	I_{OLK}		1	10	μA	$0 \le V_{IN} \le V+$
Power Dissipation	P_D		15	25	mW	

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AC Characteristics

$T_A = +25°C$; $V+ = +5\ V \pm 0.25\ V$, $V_{REF} = +2.5\ V$, $f_{clk} = 1\ MHz$, $C_{INT} = 0.033\ \mu F$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Conversion Speed (10 bit)	t_{CONV}	8.5	10	15	ms	
Conversion Speed (8 bit)	t_{CONV}	2.4	4	5	ms	
Address Setup Time $\overline{CS}$, A_0, A_{11} to $\overline{WR}$	t_{AW}	50			ns	
Address Setup Time $\overline{CS}$, A_0, A11 to $\overline{RD}$	t_{AR}	50			ns	
Address Hold Time $\overline{WR}$ to $\overline{CS}$, A_0, A_1	t_{WA}	50			ns	
Address Hold Time $\overline{RD}$ to $\overline{CS}$, A_0, A_1	t_{RA}	50			ns	
Low Level $\overline{WR}$ Pulse Width	t_{WW}	400			ns	
Low Level $\overline{RD}$ Pulse Width	t_{RR}	400			ns	
Data Setup Time Input Data to $\overline{WR}$	t_{DW}	300			ns	
Data Hold Time $\overline{WR}$ to Input Data	t_{WD}	50			ns	
Output Delay Time $\overline{RD}$ to Output Data	t_{RD}			300	ns	Note 1
Delay Time to High Z Output $\overline{RD}$ to Floating Output	t_{DF}			150	ns	

Note: 1 TTL load + 100 pF.

Recommended Operating Conditions

$T_A = +25°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V+	4.75	5.00	5.25	V	
Reference Voltage	V_{REF}	2.25	2.50	2.75	V	
Analog Input Voltage	V_{IN}	0		V_{REF}	V	Note 1
Clock Frequency	f_{clk}	0.5	1	3	MHz	Note 2
Integrating Capacitor	C_{INT}	0.029	0.033		μF	
High Level Input	V_{IH}	2.2			V	Note 3
Low Level Input	V_{IL}			0.8	V	Note 3
High Level Clock Input	V_{XHL}	V+ − 1.4			V	Note 3
Low Level Clock Input	V_{XLL}			1.4	V	Note 3

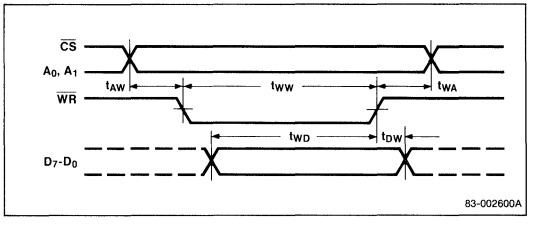
Notes: 1. Negative voltage input (< −0.2 V) decreases the input impedance. Furthermore, conversion error for the input through another MPX channel also increases.

Notes [Cont.]:

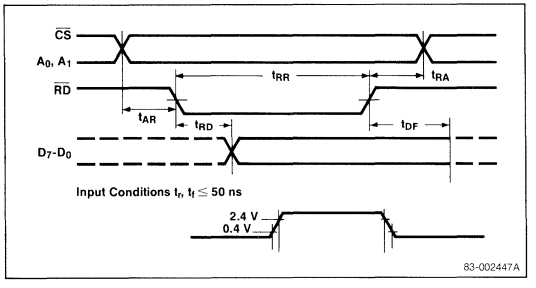
2. Integrating capacitor: C_{INT} depends on clock frequency and can be obtained as follows $C_{INT}(\mu F) = 0.033/f_{clk}$ (MHz). Note that conversion time is inversely proportional to the clock frequency.
3. $T_A = -20°C$ to $+70°C$, $V+ = +5\ V \pm 0.25\ V$.

Timing Waveforms

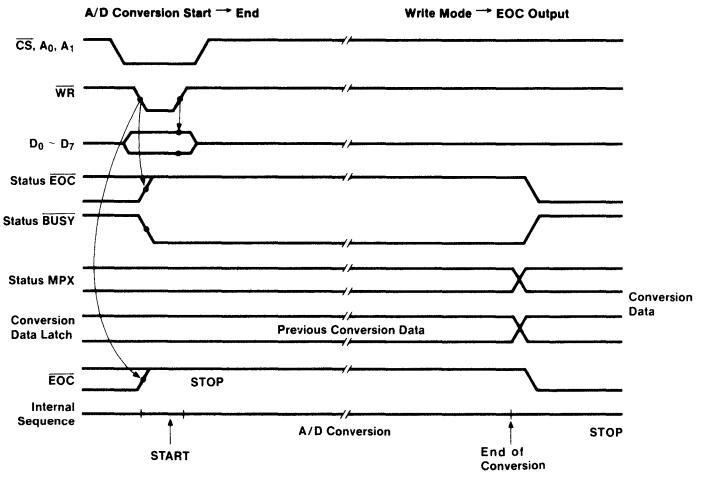
Write Mode



Read Mode

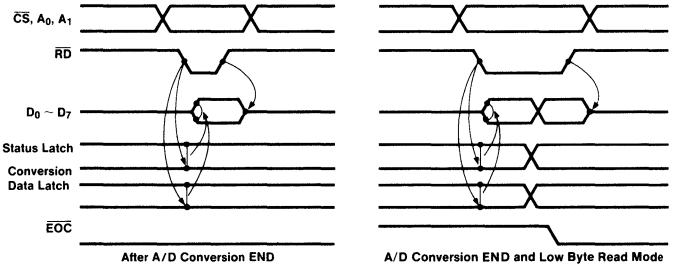


Timing Waveforms (Cont.)



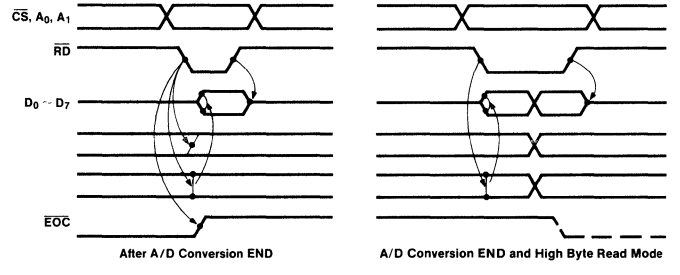
83-002601B

Read Mode (Status, Low Byte)



83-002602B

Read Mode (High Byte)



Read operation of High Byte resets the $\overline{EOC}$ (STATUS and $\overline{EOC}$ pin)

83-002451C

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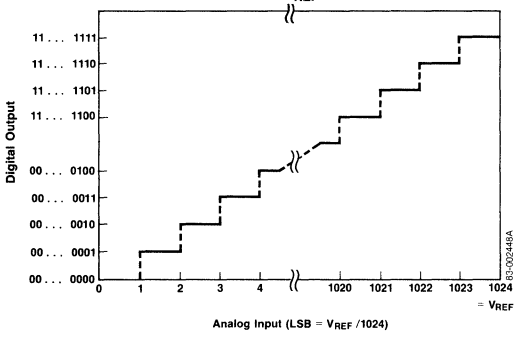
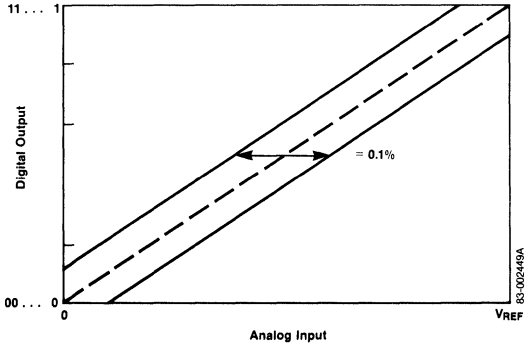
There is some uncertainty whether $\overline{EOC}$ is set or not, when data read operation is made simultaneously with the end of A/D conversion. Furthermore, the reading error occurs at this time, so in this case a dual read operation is recommended.

Operating Characteristics

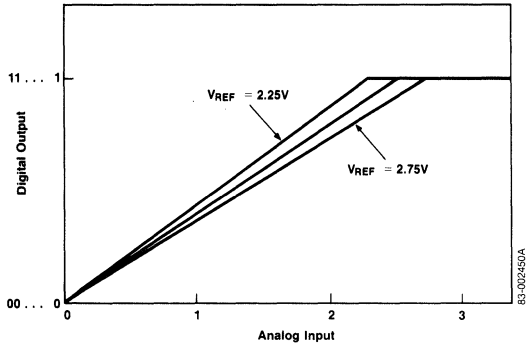
Full Scale vs V_{REF}



Total Unadjusted Error



Transfer Characteristics with Respect to V_{REF}



Addressing the Inputs

One of the four analog inputs is selected by initiating a write mode from the external controller with the control signals as follows: $\overline{CS}$ (pin 23) = "low," $\overline{RD}$ (pin 25) = "high," $\overline{WR}$ (pin 24) = "low," A1 (pin 27) and A0 (pin 26) = "low."

The analog input select data is presented to D0 (pin 22) and D1 (pin 21) and the desired channel (1 to 4) is selected. The conversion resolution mode is also selected during "write" mode by presenting a "high" for 10-bit mode or "low" for 8-bit mode, to D3 at pin 19.

Sequence

☐ Initiate "write" mode ($\overline{CS} = 0$, $\overline{RD} = 1$, $\overline{WR} = 0$, A1/A2 = 0).

☐ Present data for analog channel select to D0, D1.

	D0	D1
CH0 =	L	L
CH1 =	H	L
CH2 =	L	H
CH3 =	H	H

☐ Present conversion resolution data to D3.

10 BIT = H
8 BIT = L

During the write mode the only available function of the μPD7002 is data input from the controlling system. When the write function is terminated the A/D conversion process starts.

The Conversion Process

During the "write" mode the internal sequence controller is initialized and ready to take control of the conversion process on the rising edge of the write pulse. All conversion functions take place with the μPD7002 in the "not selected" mode with the control signals set at: $\overline{CS}$ = "low," $\overline{RD}$ and $\overline{WR}$ "high ... A0" and A1 "don't care." In the A/D section the analog signal is input via the multiplexer and compared to V_{REF} at pin 8 (V_{REF} sets the maximum full-scale input signal which can be converted). At this point the internal sample and hold for auto zero function and full scale correction are accomplished.

The processed analog signal is then passed to the analog section where the integrating capacitor is charged for a given time period controlled by the clock. In this case the period is 8192 clock periods. The capacitor is then terminated to ground and the falling slope is measured by the number of clock cycles to the zero crossing point. The number of clock cycles from peak to zero (falling slope) is proportional to the value of V_{IN}. The integrator is then set up for the next conversion cycle.

The digital section converts the pulses from the analog section to 12-bit code and sends the converted code to the conversion data register where the data is latched and ready for "reading" by the controlling device. The data is then "read" in two bytes by addressing A0 and A1 while in the read mode. A1 = "low" A0 = "high" reads the high data byte (D0 to D7), and A1 = "high" A0 = "either" reads the low data byte (D7 to D4). During the low data byte read D0 to D3 are low and the data on D4 and D5 (bits 11 and 12) may not be accurate data.

The internal status can also be checked while in the read mode by setting A0 and A1 both "low."

Operation of Individual Sections

Sequence Controller (See Sequence Chart)

The Sequence Controller controls the internal sequence of A/D conversion and the operation of the three-state I/O buffer. It is initialized by the write mode operation (analog MPX address and 10-/8-bit choice). After the write mode operation, the Sequence Controller starts the A/D conversion, and outputs an $\overline{EOC}$ signal when the conversion is completed. There is no power-on-reset circuitry.

A/D Conversion Block

In the A/D section, an analog signal is input through the MPX and is compared to V_{REF}, after which it is converted to a digital output signal. Full scale analog input is equal to V_{REF}. GND as an analog input is equal to zero scale. A/D conversion time depends on both analog input voltage and conversion mode (10/8 bit).

Three-State I/O Port Section

The three-state I/O port section is controlled by the Sequence Controller. It accepts the MPX address input and conversion mode input (10-/8-bit choice). The three-state I/O port section outputs the internal status and conversion data high/low bytes.

Conversion Data Latch

After the end of conversion, the A/D section outputs new data to the Data Latch. The output of the Data Latch is connected to the three-state I/O ports, and the data can be read at any time. When Data Read occurs simultaneously with an internal data transfer, a read error occurs. Therefore, two read operations should be made, unless Data Read occurs after the end of conversion.

Status Latch

The status latch stores the status data internal to the chip, and the internal operation state can be referenced by the status data. Status includes the following:

$\overline{BUSY}$, $\overline{EOC}$: Internal sequence state of μPD7002. Write mode operation sets $\overline{BUSY}$, and this is reset at the end of conversion. $\overline{EOC}$ is set at the end of conversion, and High Byte Read Operation resets $\overline{EOC}$.

MSB, 2nd; 10-/8-Bit Flag MPX

The data stored in the conversion Data Latch when the status reading operation is made can be output. Therefore, the data is refreshed at the end of conversion.

Access to the μPD7002 from the CPU can be made by both interrupt and polling methods. In the interrupt method use $\overline{EOC}$ as an interrupt signal. In the polling method, use $\overline{EOC}$ and $\overline{BUSY}$ in Status Byte.

After the A/D conversion, the data in the conversion Data Latch does not change, and can be read repeatedly. Therefore, fundamental instructions like Load, Store, Move, etc. can be used to access data (by placing the address of the μPD7002 in memory area). Note that the access time (t_{RD}) and the data setup time (t_{DW}) of the μPD7002 are longer than that of the 8080 and 8085. The following program example shows the accessing of the μPD7002 by polling method in an 8080-based system.

MPX Channel Address Functions

MPX Address Bit	Analog Input Channel			
	CH0	CH1	CH2	CH3
D_1	L	L	H	H
D_0	L	H	L	H

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Control Terminal Functions

Control Terminals					Mode	Internal Function	Data I/O Terminals
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_7			
H	x	x	x	x	Not selected		High impedance
L	H	H	x	x	Not selected	—	
L	H	L	L	L	Write mode	Data latch A/D start	Input status, D_1, D_0 = MPX address D_3 = 8-bit/10-bit conversion designation. Note 1. D_7 = Flag input.
L	H	L	L	H	Not selected	—	High impedance
L	H	L	H	L	Not selected	—	
L	H	L	H	H	Test mode	Test status	Input status, Note 2
L	L	H	L	L	Read mode	Internal status	$D_7 = \overline{EOC}$, D_6 = BUSY, D_5 = MSB, D_4 = 2nd MSB, D_3 = 8/10, D_2 = Flag Output, D_1 = MPX, D_0 = MPX
L	L	H	L	H	Read mode	High data byte	D_7–D_0 = MSB – 8th bit
L	L	H	H	L	Read mode	Low data byte	D_7–D_0 = 9th – 10th bit
L	L	H	H	H	Read mode	Low data byte	D_3–D_0 = L

Notes: 1. Designation of number of conversion bits: 8 bit = L; 10 bit = H.
2. Test Mode: used for inspecting the device. The data input-output terminals assume an input state and are connected to the A/D counter. Therefore, the A/D conversion data read out after this is meaningless.

Bit Function

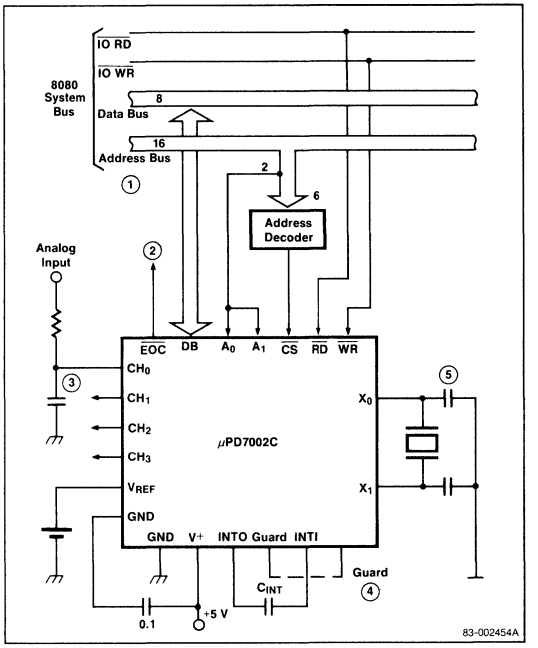
		Write Mode	Read Mode				
		Function	Status Output	High Byte Output		Low Byte Output	
Bit	I/O			10-Bit Note 2	8-Bit	10-Bit Note 2	8-Bit
D7	Output		EOC	MSB	MSB	9th	Note 3
D6	Output		Busy	2nd	2nd	LSB	Note 3
D5	Output		MSB Note 1	3rd	3rd	Q_{11}	Note 3
D4	Output		2nd Bit Note 1	4th	4th	Q_{12}	Note 3
D3	I/O	10/8-Bit	10/8-Bit Note 1	5th	5th	Low	Low
D2	I/O	Flag input	Flag Output Note 1	6th	6th	Low	Low
D1	I/O	MPX Address	MPX Note 1	7th	7th	Low	Low
D0	I/O	MPX Address	MPX Note 1	8th	8th	Low	Low

Notes: 1. Previous conversion data.
2. In 10-bit mode, the μPD7002 operates as a 12-bit converter. Therefore, 11th and 12th bit data appear at Q_{11} and Q_{12}, and the output of Q_{11} and Q_{12} varies with analog input; however, the data contain internal noise and are meaningless.
3. Not to be determined.

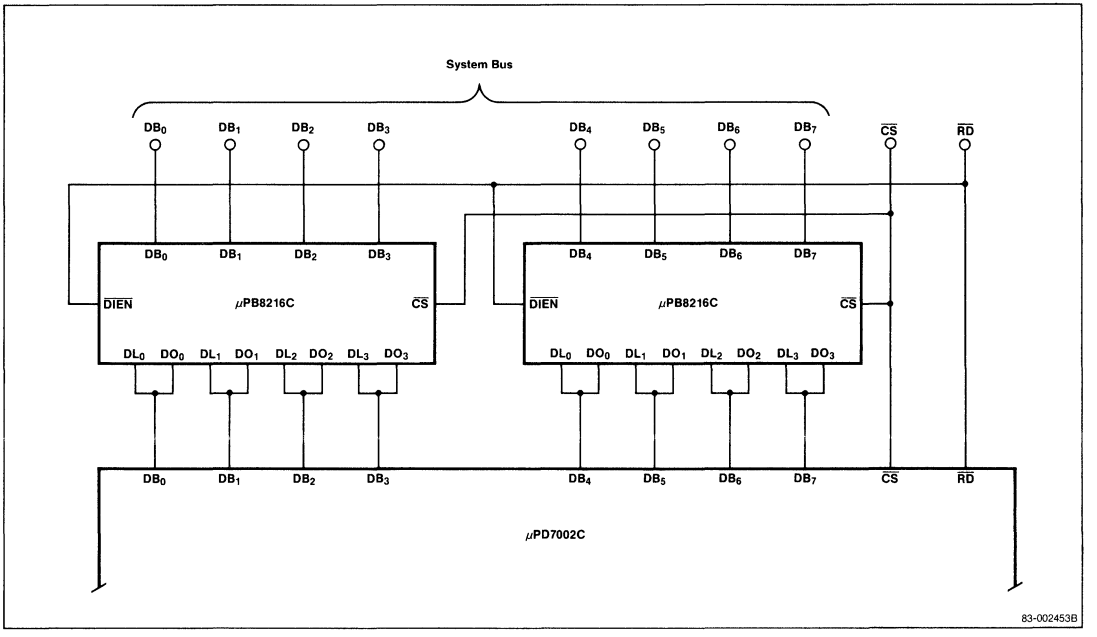
Typical Applications

1. The high level input voltage of the μPD7002C is 2.2 V. In a minimum component system configuration, tying 50 kΩ resistors to DB_0-DB_7, A_0, A_1, $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ is recommended. The fan-out of DB_0-DB_7 is 1 TTL level. In larger systems, use bus drivers as shown here.
2. Use $\overline{EOC}$ as an interrupt signal if you have an interrupt-driven system.
3. Use a 100 Hz low pass filter to decrease the conversion error. Using the diode protection circuit shown here is effective protection against high voltage surges.
4. The μPD7002 uses the integration technique for A/D conversion, and it operates at a very low current level. The external integrating capacitor (C_{INT}) is directly connected to the internal integrator. Using the guard pattern as shown below makes the operation less sensitive to leakage current.
5. Capacitors are tied to the X and X_0 pins to stabilize the oscillation, use a ceramic capacitor about 50 pF. About 50 ms is required for stable oscillation after initial power-on. Therefore, the first Write Mode Operation should occur after this interval.

Typical Microprocessor Interface



Use of Bus Drivers



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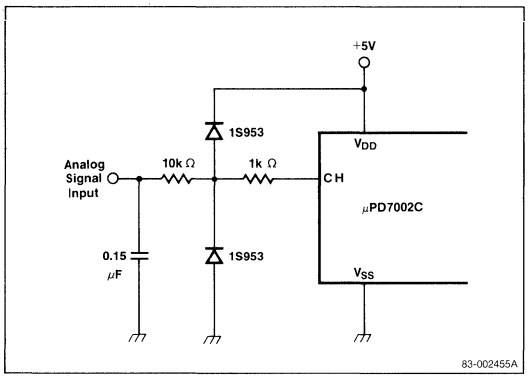
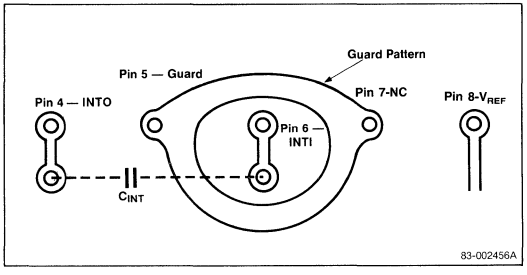
Typical Applications (Cont.)

Diode Protection Circuit



Guard Pattern

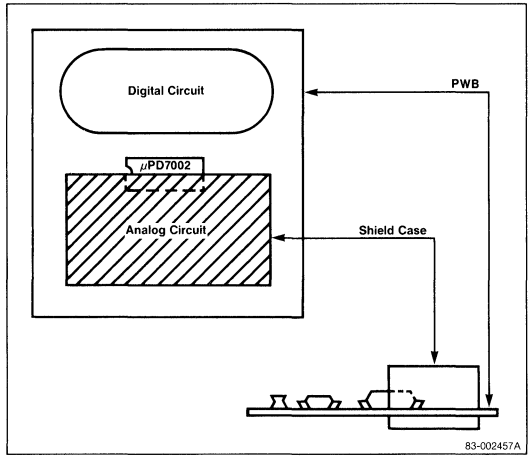


Noise Reduction

The μPD7002 is an integrating A/D converter; however, it operates at a relatively high speed and the normal mode noise rejection cannot be expected. Observance of the following points will minimize noise induction to the input of the analog circuit.

- ☐ Use lower impedance in GND connection
- ☐ Place the bypass capacitors for supply voltage and V_{REF} and analog input close to the μPD7002 (one point GND is also effective)
- ☐ Isolate analog circuitry from digital circuitry:
  - — Component layout
  - — GND wire layout
  - — Shielding of analog circuitry (pin configuration of the μPD7002 is suitable for the layout shown in the next figure)

Shield for Analog Circuitry



NEC Electronics Inc.

μPD7003
8-BIT CMOS HIGH-SPEED A/D CONVERTER

Description

The μPD7003 is a high speed, high performance, low power, 8-bit analog-to-digital Converter designed to be easily interfaced to the 8080 and 8086, 8- and 16-bit microprocessors. Using the parallel conversion technique, the μPD7003 features a conversion speed of 4 μs and eliminates the need of sample and hold circuits in most applications. The μPD7003 is also capable of running under DMA control using a DMA controller such as the μPD8257. Available in a 24-pin ceramic/plastic DIP, the μPD7003 is the ideal converter for high speed 8-bit designs.

Features

- ☐ High speed conversion (250 k samples/sec. max.)
- ☐ Input consists of 255/1 matched autozeroed comparators
- ☐ No missing codes over temperature range
- ☐ Linearity ±1.25 LSB max.
- ☐ Three-state outputs
- ☐ Overrange output
- ☐ Operates from single +5 V supply
- ☐ Low power consumption (50 mW)

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7003C	Plastic DIP	−20 °C to +70 °C
μPD7003D	Ceramic DIP	−20 °C to +80 °C

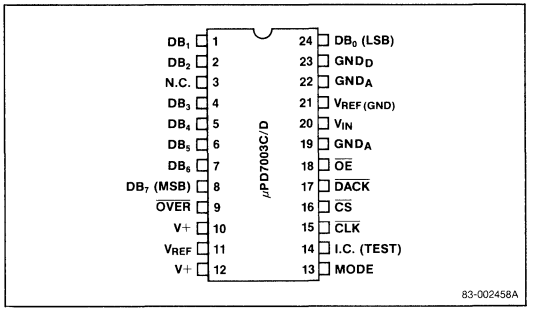
Absolute Maximum Ratings

$T_A = 25°C$

Operating Temperature, C Package	−20 to +70 °C
Operating Temperature, D Package	−20 to +70 °C
Storage Temperature	−65 to +125 °C
All Input Voltages	−0.3 to V+ +0.3 V
Power Supply	−0.3 to +7 V
Power Dissipation	300 mW
Analog GND Voltage	±0.3 V

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



Pin Identification

Pin	Name	Function
1	DB_1	7th bit output
2	DB_2	6th bit output
3	NC	Non connection
4	DB_3	5th bit output
5	DB_4	4th bit output
6	DB_5	3th bit output
7	DB_6	2th bit output
8	DB_7	MSB output
9	$\overline{OVER}$	Overrange output
10	V+	Power supply (+5 V)
11	V_{REF}	Reference voltage input (positive)
12	V+	Power supply (+5 V)
13	MODE	MODE control (note 1)
14	TEST	Low: Device test (used for inspecting the device) High: Conversion
15	$\overline{CLK}$	Low: Previous data output High: Quantizing
16	$\overline{CS}$	Chip select
17	$\overline{DACK}$	DMA Acknowledge
18	$\overline{OE}$	Low: Data output High: High impedance
19	AGND	Analog ground
20	V_{IN}	Voltage input
21	$V_{REF(GND)}$	GND for V_{REF}
22	AGND	Analog ground
23	GND	Digital ground
24	DB_0 (LSB)	LSB

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Pin Identification (Cont.)

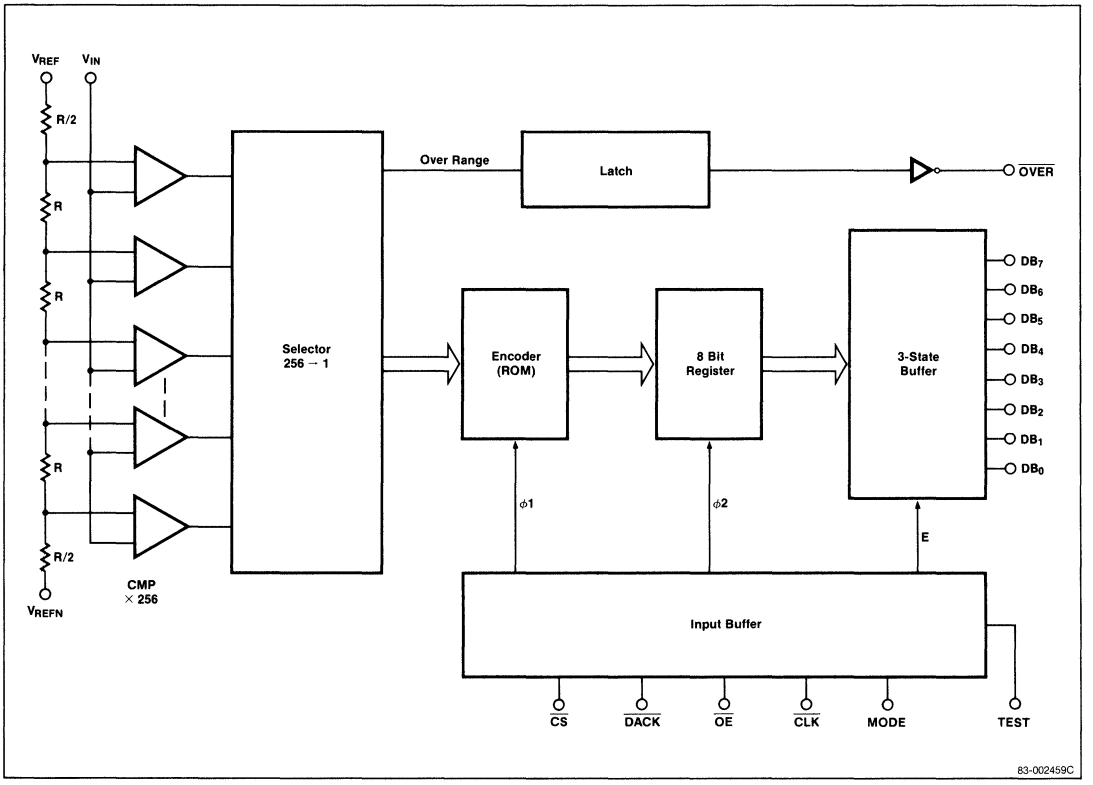
Pin	Name	Function
19	GND_A	Analog ground
20	V_{SIN}	Analog input
21	V_{REFN}	Reference voltage input (negative) (Note 2)
22	GND_A	Analog ground
23	GND_D	Digital Ground
24	DB0	LSB output

Notes: 1.

Inputs		8-Bit Register
Mode	$\overline{OE}$	
1	1	Data refreshed with every $\overline{CONV}$ ↓
	0	
.....		
0	1	.....
	0	No change

2. Tie to the analog ground unless external zero adjustment required.

Block Diagram



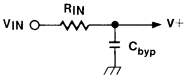
DC Characteristics

$T_A = +25°C$, $V+ = V_{REF} = 5.0 \pm 0.25$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Power Supply Current	I_{CC}		6.0	18.0	mA	$t_{CY} = 4.0\ \mu s$, $t_{WLC} = 2.0\ \mu s$ Note 1
High Level Output Voltage	V_{OH}	2.8			V	$I_O = -2.0$ mA
Low Level Output Voltage	V_{OL}			0.4	V	$I_O = -1.0$ mA
Digital Input Leakage Current	I_{ILK}		1	10	μA	$0\ V \leq V_{IN} \leq V+$
Digital Output Leakage Current	I_{OLK}		1	10	μA	$0\ V \leq V_O \leq V+$
Reference Input Current	I_{REF}	1.19	1.79	3.57	mA	$\overline{CLK}$ = H or L Note 1
Analog Input Resistance	R_{IN}	1	35		kΩ	$V_{EN} = 2.5$ V, $t_{CY} = 4\ \mu s$, $t_{WLC} = 2\ \mu s$ Note 2
Reference Input Capacitance	C_{REF}		100		pF	$f_{clk} = 1$ MHz; unmeasured pins returned to Ground
Analog Input Capacitance	C_{IN}		100		pF	$f_{clk} = 1$ MHz; unmeasured pins returned to Ground
Power Dissipation	P_D			50	mW	$t_{CY} = 4.0\ \mu s$, $t_{WLC} = 2.0\ \mu s$

Notes: 1. This means DC current. Tie the bypass capacitors (electrolytic capacitor ≥ 10 μF, ceramic capacitor ≈ 0.01 μF) to V+ and V_{REF} pins, in order to absorb rush current (≈ 10 mA).

2. DC input equivalent circuit is shown below.



Tie the bypass capacitor (> 0.01 μF) to the analog input pin. 3 mA peak current flows into this pin.

AC Characteristics

$T_A = 25 \pm 2°C$; $V+ = 5.0$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Delay Time	t_{DEO}		100	350	ns	$\overline{OE}$ ↓ → DO
	t_{DCO}		150	450	ns	$\overline{CONV}$ ↓ → DO
	t_{DSO}		100	350	ns	$\overline{CS}$ ↓ → DO
	t_{DCOVR}		100	350	ns	$\overline{CONV}$ ↑ → $\overline{OVER}$
Delay Time to Floating	t_{FEO}		70	200	ns	$\overline{OE}$ ↑ → DO
	t_{FSO}		150	450	ns	$\overline{CS}$ ↑ → DO

Conversion Characteristics

$T_A = 25 \pm 2°C$; $V+ = V_{REF} = 5.0$ V;
$t_{CY} = 4.0\ \mu s$; $t_{WLC} = 2.0\ \mu s$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution	RES	8	8	8	Bits	−20°C to +80°C
Nonlinearity	NL			±1.25	LSB	
Full Scale Error				±1.00	LSB	
Full Scale Error Temperature Coefficient			20		ppm/°C	
Zero Scale Error		−0.75		+0.75	LSB	
Zero Scale Error Temperature Coefficient			20		ppm/°C	

Note: μPD7003C: $T_A = 0°C$ to $+70°C$.

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Recommended Operating Conditions

$T_A = 0°C$ to $70°C$: μPD7003C,
$T_A = -20°C$ to $+80°C$: μPD7003D

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V+	4.75	5.0	5.25	V	
Reference Input Voltage	V_{REF}	4.0	V+	V+	V	
Analog Input Voltage	V_{IN}	−0.1		V+ +0.1	V	
High Level Logic Input	V_{IH}	2.4		V+	V	
Low Level Logic Input	V_{IL}	−0.1		0.8	V	
Sampling Rate		10		250k	times/s	
Conversion Cycle Time	t_{CY}	4.0		100	μs	
$\overline{CONV}$ High Level Width	t_{WHC}	2.0			μs	
$\overline{CONV}$ Low Level Width	t_{WLC}	2.0			μs	
$\overline{CONV}$ Setup Time	t_{SCE}	0		Note 1	ns	$\overline{CONV}\downarrow \rightarrow \overline{OE}\downarrow$
$\overline{CS}$ Setup Time	t_{SSE}	100			ns	$\overline{CS}\downarrow \rightarrow \overline{OE}\downarrow$
$\overline{CS}$ Hold Time	t_{HES}	0			ns	$\overline{OE}\uparrow \rightarrow \overline{CS}\uparrow$
$\overline{OE}$ Setup Time	t_{SEC}	600			ns	$\overline{OE}\downarrow \rightarrow \overline{CONV}\downarrow$
$\overline{OE}$ Hold Time	t_{HCE}	400			ns	$\overline{CONV}\uparrow \rightarrow \overline{OE}\downarrow$
$\overline{OE}$ Low Level Width	t_{WLE}	400		Note 2	ns	
Digital Input Rise and Fall Time	t_r, t_f			50	ns	

Notes: 1. t_{SCE} (ns) $\leq t_{CY}$ (ns) − t_{WLE} (ns) − 100 (ns).
2. t_{WLE} (ns) $\leq t_{CY}$ (ns) − t_{SCE} (ns) − 100 (ns).

Converter Operation

Referring to the block diagram, the reference voltage is set externally to some desired level which references the individual internal components such that V_{REF} is divided equally by 256 resistors in a ladder/divider configuration. The applied voltage to V_{IN} is then compared to the reference level and the individual samples are sent to the selector section where the individual signals are multiplexed to form an address data word. The data word is then further encoded to form the final 8-bit data byte by the encoder ROM, and stored in the 8-bit register until the Output Enable Command. Then the data is sent to the data bus via a three-state buffer.

Mode Select

There are two modes of operation for the μPD7003. Figure 1 shows the timing diagram for mode "0" where the converter is operating in continuous output mode. The analog input is sampled when the clock is in the "low" state. When the clock is in the "high" state the conversion from analog-to-digital takes place and the resultant data is output on the next falling edge of the clock pulse and the cycle is repeated.

The second mode (Mode 1) is shown in figure 2. In this mode of operation, one conversion takes place while the clock is in the "low" state and the resultant data is held as long as output enable and Chip Select ($\overline{CS}$) or DMA Acknowledge ($\overline{DACK}$) are "low." Data refresh is inhibited until $\overline{CS}$ and $\overline{DACK}$ are recycled.

MODE = "HIGH"

Data is refreshed on the falling edge of $\overline{CLK}$, loaded during the "low" clock state, and converted and output during the "high" clock state.

MODE = "LOW"

Data is loaded and converted when Output Enable is "low" and refreshed only when $\overline{OE}$ makes the transition from high to low again.

Note that in either case data will only be accepted and output when $\overline{OE}$ and $\overline{CS}$ or $\overline{DACK}$ are active ("low"). Output enable should not be changed during the intervals shown in figure 3. The timing for output enable change versus clock transition is 600 ns before and 500 ns after the rising or falling edge of $\overline{CLK}$ any attempt to change $\overline{OE}$ during these periods will be inhibited.

Timing Waveforms

Figure 1. (MODE;0)

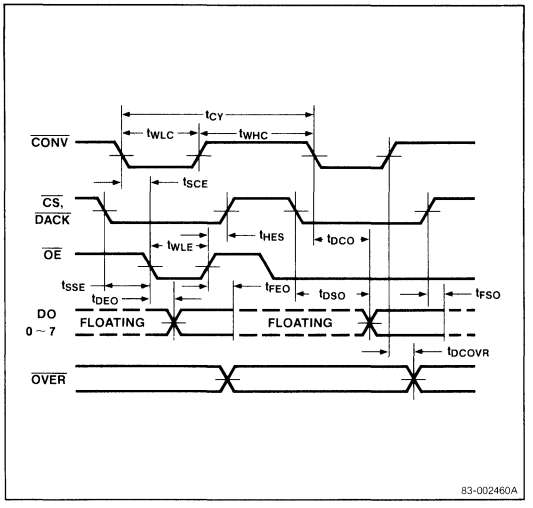


Figure 2. (MODE;1)

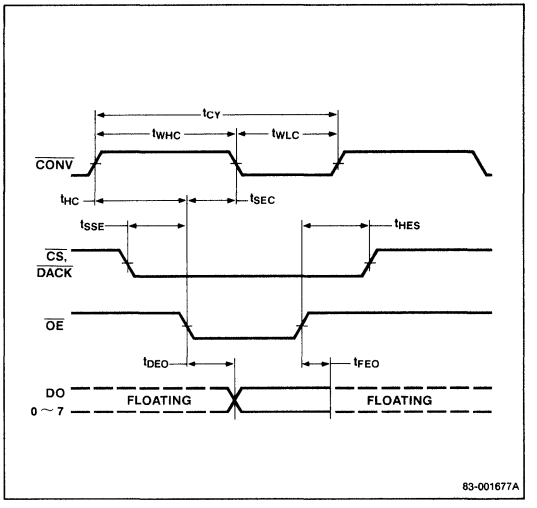
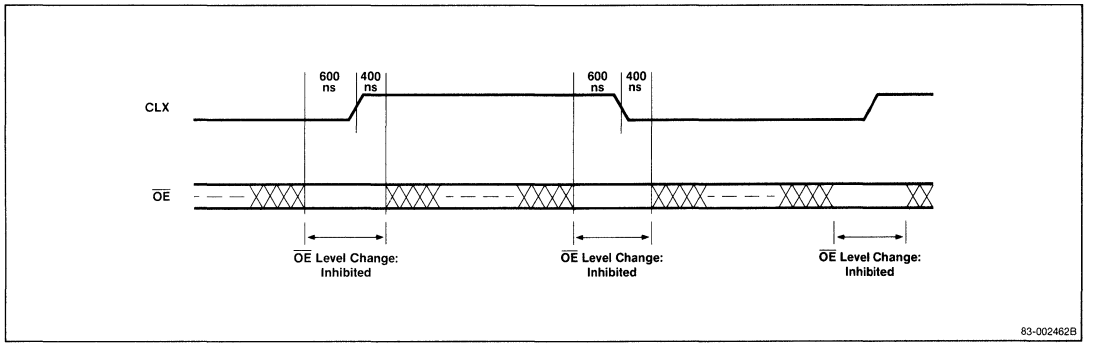


Figure 3. Timing Chart



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NEC
NEC Electronics Inc.

μPD7004
10-BIT CMOS SUCCESSIVE APPROXIMATION A/D CONVERTER

Description

The μPD7004 is a 10-bit monolithic CMOS analog-to-digital converter using the Successive Approximation Register (SAR) technique. The μPD7004 incorporates an 8-channel multiplexed analog input and full microprocessor interface to achieve a high degree of versatility. The designer has a choice of either serial or parallel output and interface to 8080 type microprocessors or advanced signal processors like the μPD7720.

Features

- ☐ 8-channel multiplexed analog input
- ☐ Serial or parallel interface
- ☐ 10-bit resolution
- ☐ Linearity: 1 LSB max. ($T_A = 25°C$)
- ☐ Conversion time: 100 μs ($f_{clk} = 1$ MHz)
- ☐ Input voltage range 0 to V+
- ☐ Temperature range from −40 to +85°C
- ☐ Operates from single +5 volt supply

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7004C	Plastic DIP	−40°C to +85°C

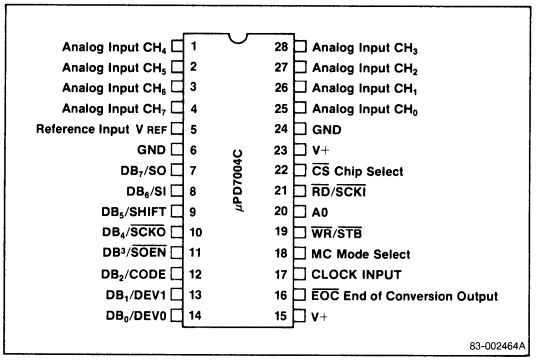
Absolute Maximum Ratings

$T_A = 25°C$

Supply Voltage, V_{DD}	−0.3 to +7.0 V
Input Voltage, V_I	−0.3 to V+ +0.3 V
Reference Voltage, V_{REF}	−0.3 to V+ +0.3 V
Operating Temperature, T_{OPT}	−40 to +85°C
Storage Temperature, T_{OPT}	−65 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



Conversion Characteristics

$T_A = 25°C$, $V+ = V_{REF} = 4.5$ to 5.5 V, $f_{clk} = 1$ MHz

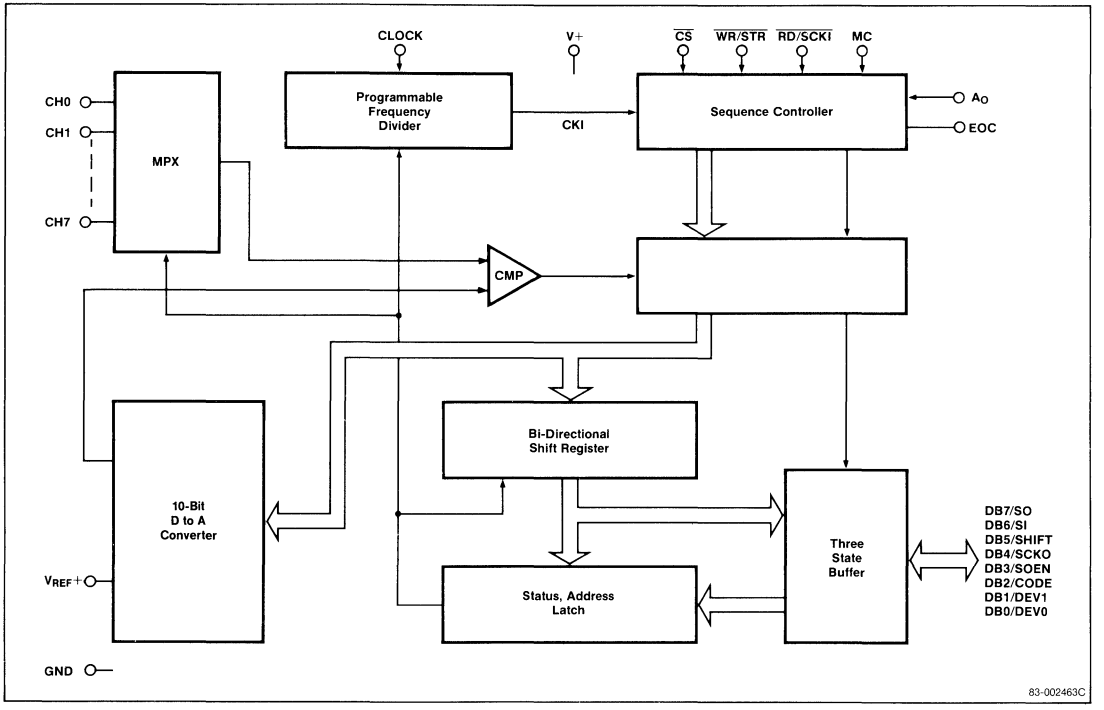
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution		10	10	10	Bit	−40 to +85°C
Nonlinearity	NL			±1.0	LSB	
Zero Scale Error				±0.5	LSB	
Zero Scale Temperature Coefficient			2		ppm/°C	−40 to +85°C
Full Scale Error		−0.5		0.5	LSB	
Full Scale Temperature Coefficient			2		ppm/°C	−40 to +85°C
Nonlinearity	NL			±2	LSB	−40 to +85°C ($T = T_{OPT}$)

6

Pin Identification

		Parallel Mode		Serial Mode	
Pin	Symbol	Direction	Function	Direction	Function
1	CH4		Analog input CH4		
2	CH5		Analog input CH5		
3	CH6		Analog input CH6		
4	CH7		Analog input CH7		
5	V^+_{REF}		Positive reference input		
6	GND		Ground		
7	DB7/SO	O	Data bus (MSB)	O	Serial output
8	DB6/SI	O	Data bus (2nd)	I	Serial input
9	DB5/SHIFT	O	Data bus (3rd)	I	LSB/MSB 1st select
10	DB4/$\overline{SCKO}$	O	Data bus (4th)	I/O	Serial clock output
11	DB3/$\overline{SOEN}$	O	Data bus (5th)	I/O	Serial output enable
12	DB2/CODE	I/O	Data bus (6th)	I	Code select
13	DB1/DEV1	I/O	Data bus (7th	I	Frequency divide ratio set
14	DB0/DEV0	I/O	Data bus (LSB)	I	Frequency divide ratio set
15	V+		Power supply		
16	$\overline{EOC}$	O	End of conversion (active low)		
17	CLOCK	I	Clock input		
18	MC	I	MODE select (H = Parallel, L = Serial)		
19	$\overline{WR}/\overline{STB}$	I	Write input	I	Strobe input
20	A0	I	Address input	I	Internal/external shift clock
21	$\overline{RD}/\overline{SCKI}$	I	Read input	I	Serial clock input
22	$\overline{CS}$	I	Chip select		
23	V+		Power supply		
24	GND		Ground		
25	CH0		Analog input CH0		
26	CH1		Analog input CH1		
27	CH2		Analog input CH2		
28	CH3		Analog input CH3		

Block Diagram



AC Characteristics

$T_A = -40°C$ to $+85°C$, $V+ = V_{REF} = 5\ V \pm 0.5\ V$, $f_{CKI} = 1\ MHz$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Delay Time	t_{RD}			250	ns	$\overline{RD}$ ↓ → DB (parallel mode)
	t_{DKO}			250	ns	$\overline{SCKI}$ ↓, $\overline{SCKO}$ ↓ → SO (serial mode)
Output Floating Delay Time	t_{DF}			150	ns	$\overline{RD}$ ↑ → DB floating (parallel mode)
	t_{FCSO}			150	ns	$\overline{CS}$ ↑ → SO floating (serial mode 1)
Serial Clock Output Delay Time	t_{SKS}	40		200	ns	$\overline{SCKO}$ ↑ → $\overline{SOEN}$ ↓ (serial mode 2)
Serial Output Enable Delay Time	t_{HKS}	0		200	ns	$\overline{SCKO}$ ↓ → $\overline{SOEN}$ ↑ (serial mode 2)
Serial Clock Output Cycle	t_{CYK}		$1/f_{clk}$		ns	(Serial mode 2)
High Level Serial Clock Pulse Width	t_{WHK}	400			ns	(Serial mode 2)
Low Level Serial Clock Pulse Width	t_{WLK}	400			ns	(Serial mode 2)
Serial Clock Rise Time	t_{RSC}		20		ns	(Serial mode 2)
Serial Clock Fall Time	t_{FSC}		20		ns	(Serial mode 2)

6

DC Characteristics

$T_A = -40°C$ to $+85°C$, $V_{REF} = 5\ V \pm 0.5\ V$, $f_{clk} = 1\ MHz$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
High Level Output Voltage	V_{OH}	3.5			V	$I_O = -1.6\ mA$
Low Level Output Voltage	V_{OL}			0.4	V	$I_O = 1.6\ mA$
Digital Input Leakage Current	I_{ILK}	−10		10	μA	$V_{IN} = GND$
High-Z Output Leakage Current	I_{OLK}	−10		10	μA	$V_O = GND$
Analog Input Resistance	R_{IN}		1000		MΩ	$V_{IN} = GND$
Equivalent Analog Input Resistance	R_{IN}		10		kΩ	Analog input impedance is equivalent to that of the series circuit of R_I and C_I
	C_{IN}		100		pF	
Reference Input Resistance	R_{REF}	5		50	kΩ	
Power Dissipation	P_D		5	15	mW	

Recommended Operating Conditions

$T_A = -20°C$ to $+80°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V+	4.5	5.0	5.5	V	
Reference Voltage	V_{REF}	4.0		V_{DD}	V	
Analog Input Voltage	V_{IN}	0.0		V_{REF}	V	
High Level Input Voltage	V_{IH}	2.4			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Clock Frequency	f_{clk}	0.4		8.8	MHz	
Internal Clock Frequency	f_{clki}	0.4	1.0	1.1	MHz	$f_{clki} = f_{clk} \times$ Divide Ratio
Parallel Mode (MC = High)						
Address Setup Time	t_{AW}	50			ns	$\overline{CS}\downarrow$, AO → $\overline{WR}\downarrow$
	t_{AR}	50			ns	$\overline{CS}\downarrow$, AO → $\overline{RD}\downarrow$
Address Hold Time	t_{WA}	50			ns	$\overline{WR}\uparrow$ → $\overline{CS}\uparrow$ AO
	t_{RA}	50			ns	$\overline{RD}\uparrow$ → $\overline{CS}\uparrow$, AO
$\overline{WR}$ Pulse Width	t_{WW}	400			ns	
$\overline{RD}$ Pulse Width	t_{RR}	400			ns	
Data Setup Time	t_{DW}	300			ns	DB → $\overline{WR}\uparrow$
Data Hold Time	t_{WD}	100			ns	$\overline{WR}\uparrow$ → DB
Serial Mode 1 (MC = Low, AO = Low; External Serial Clock)						
$\overline{EOC}$ Hold Time	t_{HECS}	0			μs	$\overline{EOC}\downarrow$ → $\overline{CS}\downarrow$
$\overline{CS}$ Setup Time	t_{SCSK}	1			μs	$\overline{CS}\downarrow$ → $\overline{SCKI}\downarrow$
Serial Input Setup Time	t_{SIK}	150			ns	$\overline{SI}$ → $\overline{SCKI}\uparrow$
Serial Input Hold Time	t_{HKI}	100			ns	$\overline{SCKI}\uparrow$ → $\overline{SI}$
Low Level Serial Clock Pulse Width	t_{WLK}	400			ns	
High Level Serial Clock Pulse Width	t_{WHK}	400			ns	
Strobe Pulse Width	t_{WLST}	200			ns	
Strobe Hold Time	t_{HKST}	200			ns	$\overline{SCK}\uparrow$ → $\overline{STB}\uparrow$
Chip Select Hold Time	t_{HKCS}	100			ns	$\overline{SCK}\uparrow$ → $\overline{CS}\uparrow$

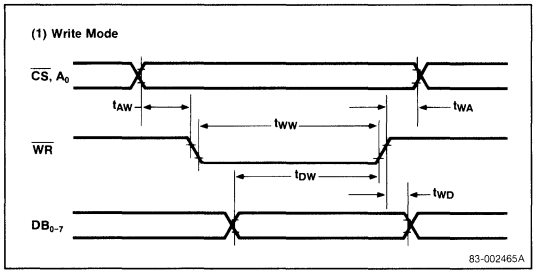
Addressing the Inputs

One of eight analog inputs can be selected with the μPD7004 in the "write" mode and A0 at pin 20 set "low." The "write" mode is selected by setting the Chip Select ($\overline{CS}$) at pin 22, and Write ($\overline{WR}$) at pin 19, "low" or 0. The multiplex channel select is accomplished by presenting a 3-bit binary code to DB0 to DB2 at pins 14, 13, and 12 where 000 = channel 0 and 111 = channel 7.

Referring to figure 1, the sequence is:

- ☐ Chip Select ($\overline{CS}$) and A0 set "low."
- ☐ Write ($\overline{WR}$) set "low." (Read ($\overline{RD}$) is left "high.")
- ☐ Analog input channel selected by presenting a 3-bit binary code on pins 14, 13, 12 (D0 to D2).
- ☐ The address is latched and the desired input channel is now selected.

Figure 1. Write Mode Timing Diagram



Initializing the Converter

The μPD7004 gives the designer a choice of the type of data output format, either a 2's complement or binary, and the speed of operation by providing a programmable frequency divider. These options may be selected by the controlling system at any time by the "initialize" mode.

The "initialize mode" is set with $\overline{CS}$ and $\overline{WR}$ both "low." $\overline{RD}$ and A0 are set "high." Code select is accomplished by presenting either a "high" for 2's complement or "low" for binary output at DB2 (pin 12). The divide ratio of 1/1 to 1/8 is set by presenting a 2-bit code to DB0 (pin 14) and DB1 (pin 13).

Ratio	DB0	DB1
1/1	L	L
1/2	H	L
1/4	L	H
1/8	H	H

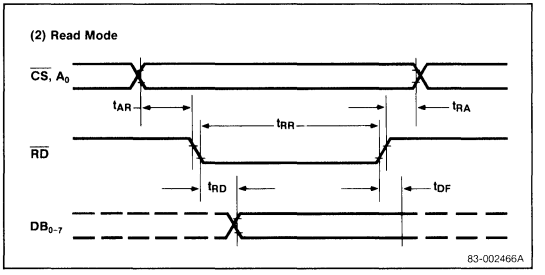
Data Output

Data can be read in 2 bytes from the data output at pins 7 through 14 (DB7 to DB0). To read the high byte, $\overline{CS}$ and $\overline{RD}$ are both "low." To read the low byte, A0 is set Low and data bit 9 and 10 are present at DB7 and DB6 respectively. During the low data byte read DB0 through DB5 are "low."

Referring to figure 2, the sequence is:

- ☐ Chip Select ($\overline{CS}$) "low" and A0 (pin 20) "high"
- ☐ Read ($\overline{RD}$) set "low" and Write ($\overline{WR}$) set "high"
- ☐ Output high byte (MSB to 8th bit)
- ☐ A0 set "low"
- ☐ Output low byte (9th bit and LSB)

Figure 2. Data Output Timing Diagram



The Conversion Sequence

The μPD7004C uses the Successive Approximation Register (SAR) technique to convert analog voltage levels to 10-bit digital code in either 2's complement or binary format. Regardless of the type of data output (either serial or parallel), the conversion process is the same.

Once the clock frequency and the output data format have been set, and the analog input selected, the conversion process begins with the analog level compared to the existing level from an internal 10-bit digital to analog converter. The D/A output level is proportional to the existing code output from the Successive Approximation Register which is proportional to the input level from the comparator.

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Data Bus I/O Operation (Parallel Mode MC = H)

Pin	Symbol			Function				
22	$\overline{CS}$	H	L	L	L	L	L	L
19	$\overline{WR}$	x	H	L	L	H	H	L
21	$\overline{RD}$	x	H	H	H	L	L	L
20	A0	x	x	H	L	H	L	X
—	Operation	No Operation		Initialize	MPX address setting	High byte read	Low byte read	Inhibit
7	DB7	—	—	DB2 = CODE select	DB2,1,0 = Analog	DB7 ~ DB0	DB7, DB6	
:	:	:	:	H = 2's comp	CH select	= MSB ~ 8th	=9th, LSB	
:	:	:	:	L = binary	0, 0, 0 ~ 1, 1, 1		DB5 ~ DB0	
:	:	:	:	DB1, DB0 = divide ratio	= CH0 ~ CH7		= LOW level	
:	:	:	:	0, 0 ~ 1, 1				
14	DB0	—	—	= 1/1 ~ 1/8				

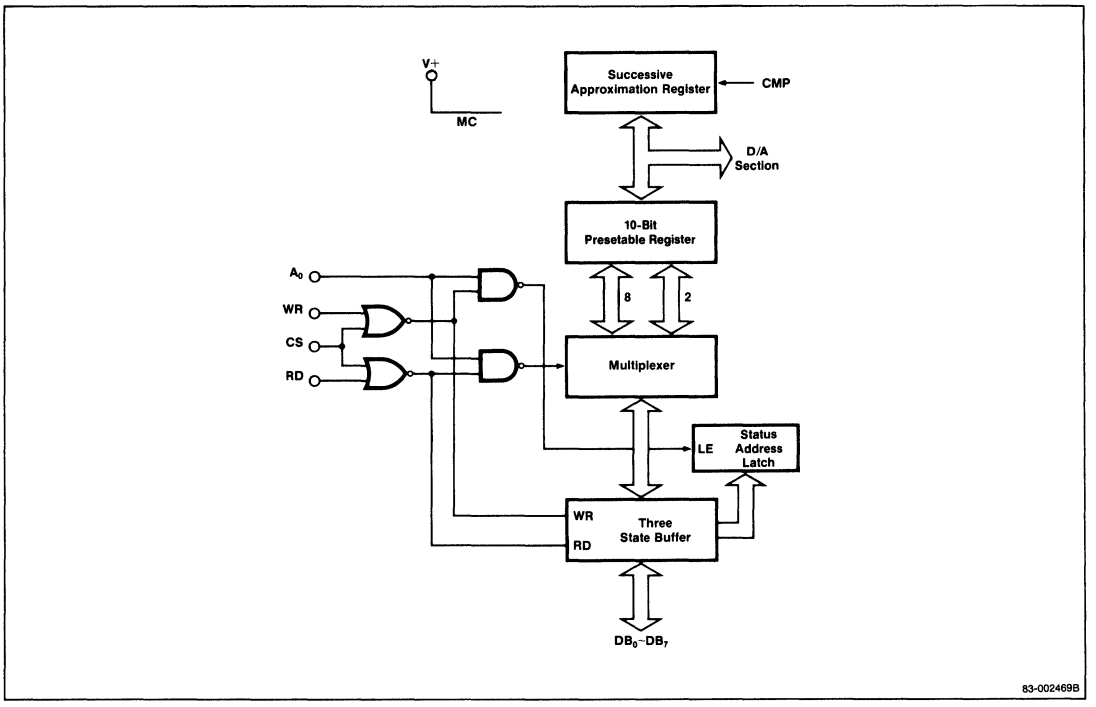
Serial I/O Operation (Serial Mode 1, 2, MC = L)

		Serial Mode 1 (External SCK, A0 = L)		Serial Mode 2 (Signal Processor Mode, A0 = H)	
Pin	Symbol	Direction	Function	Direction	Function
7	SO	O	Serial output (three state). Data are output at the falling edge of $\overline{SCKI}$ or $\overline{SCKO}$.		
8	SI	I	Serial Input. Data read at the rising edge of $\overline{SCKI}$ or $\overline{SCKO}$.	I	Tie to V+
9	SC	I	Shift select (H/L — LSB/MSB first)		
10	$\overline{SCKO}$	—	Tie to GND	O	Serial clock output (= internal clock)
11	$\overline{SOEN}$	—	Tie to GND	O	Serial output enable (active low)
12	CODE	I	Code select (H = 2's complement, L = binary)		
13	DIV1	I	Frequency Divide ratio setting		DIV1, 0 = 0, 0 1,1 = 1/1 1/8
14	DIV0	I			
19	$\overline{STB}$	I	Address strobe input MPX addresses are latched at the rising edge of $\overline{STB}$ input.	I	Tie to GND
21	$\overline{SCKI}$	I	$\overline{SCKI}$ controls the shift operation of I/O interface shift register. Data are output at the falling edge, and input at the rising edge.	—	Tie to V+
22	$\overline{CS}$	I	Chip select signal input. Low level of $\overline{CS}$ resets the internal sequence, and I/O interface is enabled.	I	Internal sequence reset signal input. Sequence controller are reset at the low level of $\overline{CS}$, and A/D conversion starts at the rising edge of $\overline{CS}$.

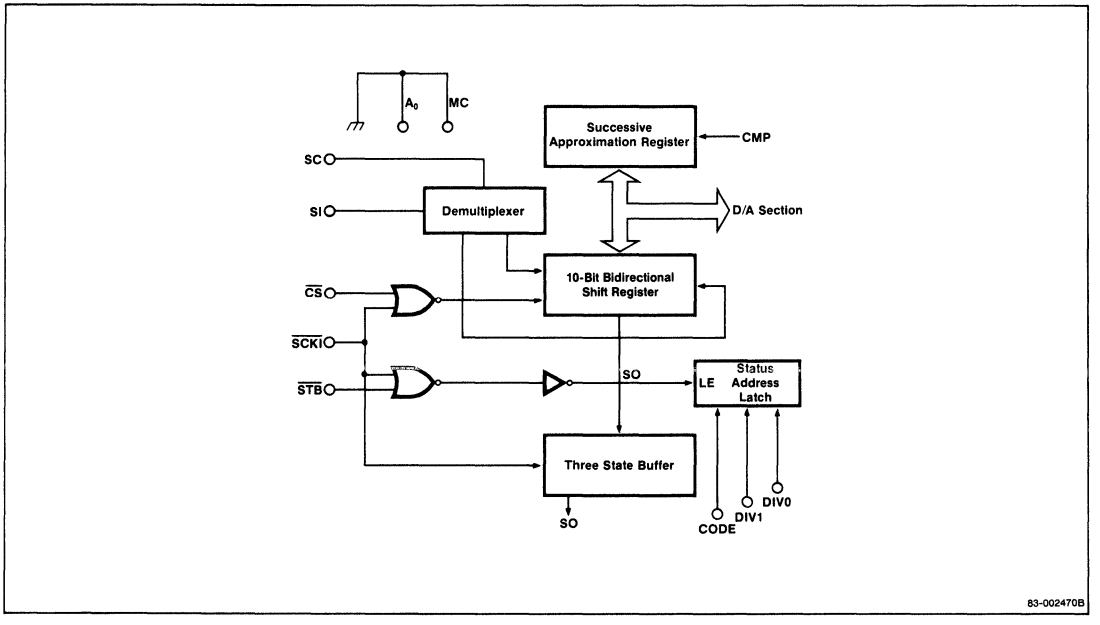
Notes: 1. In serial mode 1. I/O pins listed below are strobed by $\overline{CS}$ signal. Therefore, when $\overline{CS}$ = HIGH, input signals are ignored and output pins are left at high impedance state. Input terminal; SI, $\overline{STB}$, $\overline{SCKI}$ Output terminal; SO

2. In serial mode 2 (signal processor interface mode). By initialization, analog input MPX of CH7 is automatically selected.

Parallel Operation



Serial Operation



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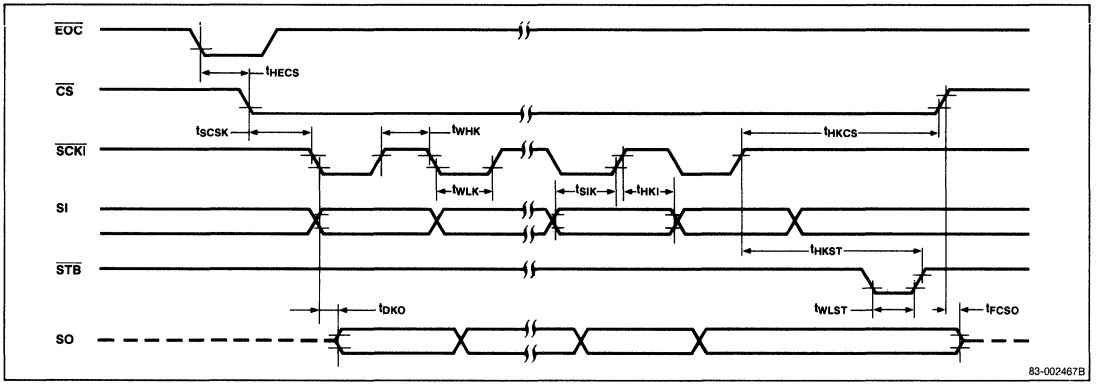
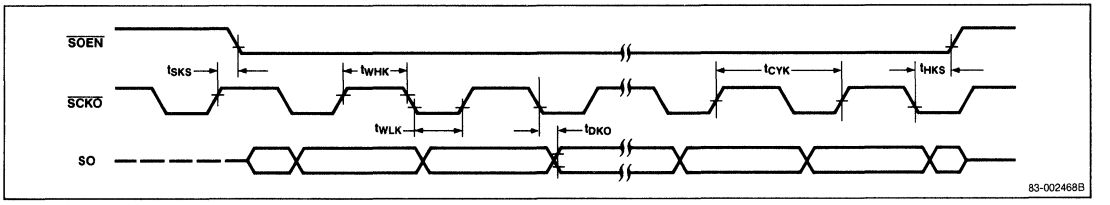
Timing Waveforms

Serial Mode 1

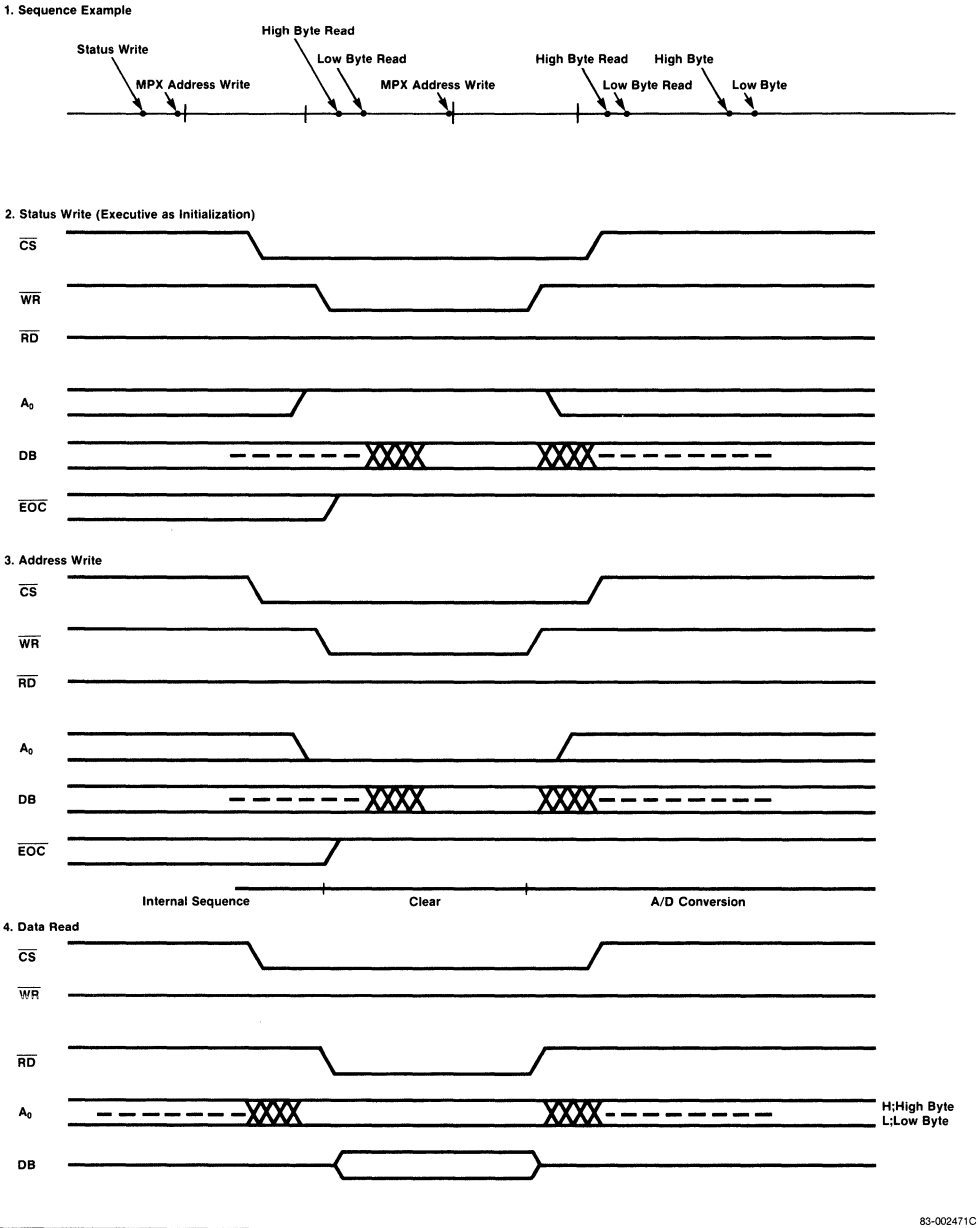


Serial Mode 2



Timing Waveforms (Cont.)

Parallel Mode Timing Chart (MC = H)



FUNCTIONAL BLOCKS

7

Section 7 — Functional Blocks

NEC
NEC Electronics Inc.

μPC398 MONOLITHIC SAMPLE-AND-HOLD CIRCUIT

Description

The μPC398 is a monolithic sample and hold circuit which combines J-FET and bipolar circuitry on the same substrate to provide a high input impedance input buffer and a high speed output buffer. Operating as a unity gain input buffer circuit, DC accuracy is typically 0.004% and acquisition time is as low as 6 μs with a maximum gain error of 0.01 %. This device is ideal for data acquisition circuits requiring high speed and high input impedance.

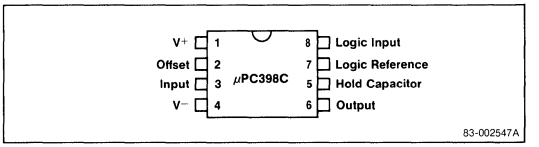
Features

- ☐ Fast acquisition time
- ☐ Gain accuracy: 0.004%
- ☐ Input offset voltage: 2 mV
- ☐ Direct interface to TTL/CMOS
- ☐ LF398 direct replacement

Ordering Information

Part Number	Package	Temperature Range
μPC398C	Plastic DIP	−20 °C to +70 °C

Pin Configuration



Absolute Maximum Ratings

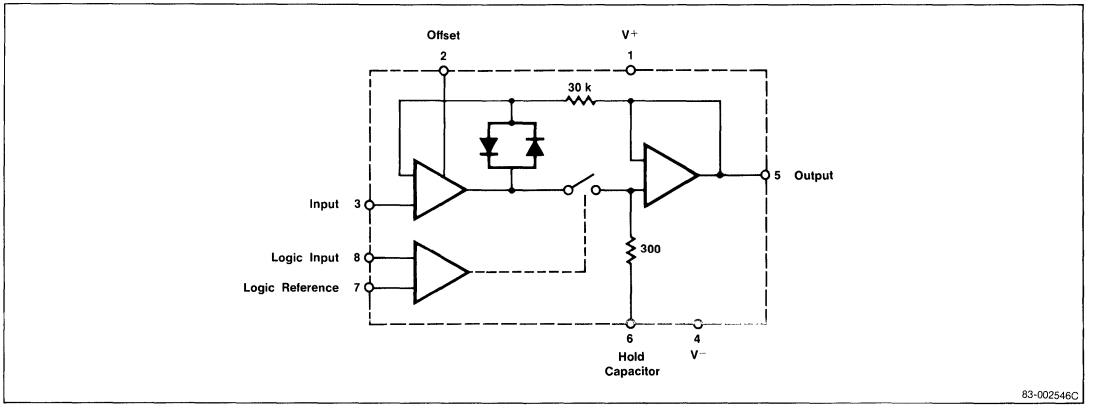
$T_A = 25\,°C$

Voltage Between V+ and V−	36 V
Input Voltage Range (Note 1)	±15 V
Logic to Logic Reference Differential Voltage	−0.3 to +7.0 V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 s
Power Dissipation	350 mW
Operating Temperature Range	−20 to +70 °C
Storage Temperature Range	−55 to +150 °C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Equivalent Circuit



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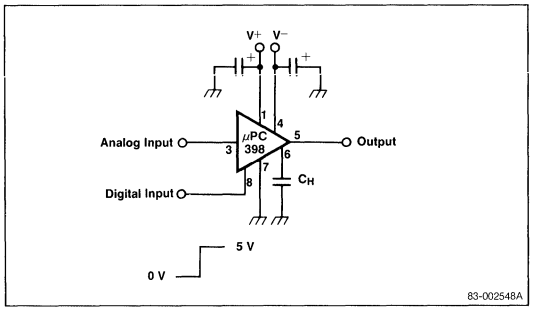
Recommended Operating Conditions

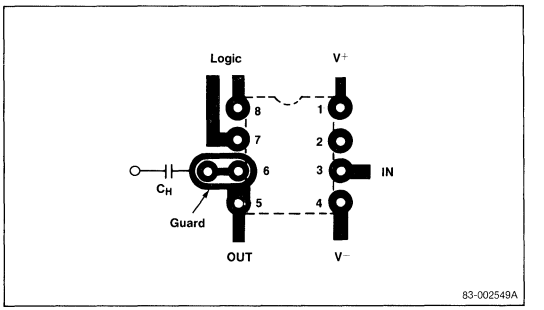
$T_A = 25°C$, $V\pm = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Power Supply Voltage	$V\pm$	±5	±15	±16.5	V	
Analog Input Voltage	V_{IN}	−11.5		+11.5	V	
Sample Mode Logic Input Voltage	V_{SH}	2.7		5.25	V	$V_{REF} = 0$
Hold Mode Logic Input Voltage	V_{SH}	−15		0.5	V	$V_{REF} = 0$
Logic Input Voltage Slew Rate	SR	0.2			V/μs	
Hold Capacitor	C_H	0.001		0.1	μF	

Typical Connection



Guarding Technique (Bottom View)



Electrical Characteristics

$T_A = 25°C$, $V\pm = \pm 15$ V, $-11.5\ V \le V_{IN} \le +11.5$ V, $C_H = 0.01\ \mu F$, $R_L = 10\ k\Omega$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}			7.0	mV	
Input Bias Current	I_b			50	nA	
Input Impedance	R_{IN}		10^{10}		Ω	
Gain Error				0.01	%	
Feedthrough Attenuation Ratio		80			dB	f = 1 kHz
Output Impedance	Z_o			4.0	Ω	
Hold Step Voltage	V_{HS}			2.5	mV	$V_O = 0$
Leakage Current into Hold Capacitor	I_{OLK}			200	pA	$V\pm = \pm 5$ V to ±18 V
Acquisition Time	t_{aq}		4		μs	$\Delta V_O = 10$ V, 0.1% Error, $C_H = 1000$ pF
	t_{sq}		20		μs	$\Delta V_O = 10$ V, 0.1% Error, $C_H = 0.01$ pF
Hold Capacitor Charging Current	I_{CH}		5		mA	$V_{IN} - V_O = 2$ V
Logic Input Current	I_{IN}			10	μA	
Logic Threshold	V_{TH}	0.8		2.4	V	
Supply Voltage Rejection Ratio	SVRR	80			dB	
Supply Current	I_{CC}			±6.5	mA	$V\pm = \pm 15$ V to ±18 V

μPC494
SWITCHING REGULATOR CONTROL CIRCUIT

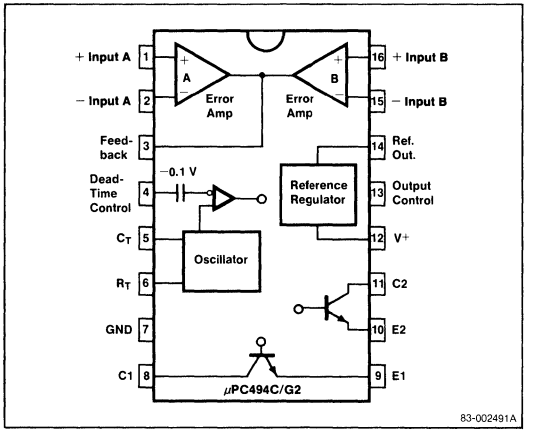
Description

The μPC494 is a switching regulator controller designed for use in switch mode power supplies (SMPS) using Pulse Width Modulator (PWM) technique. The on-board control circuitry includes a voltage reference, dual error amplifiers, oscillator, pulse width modulator, pulse steering flip-flop, dual output drivers and dead time control circuit. The μPC494 is available in the plastic DIP package and the G2 mini flat package.

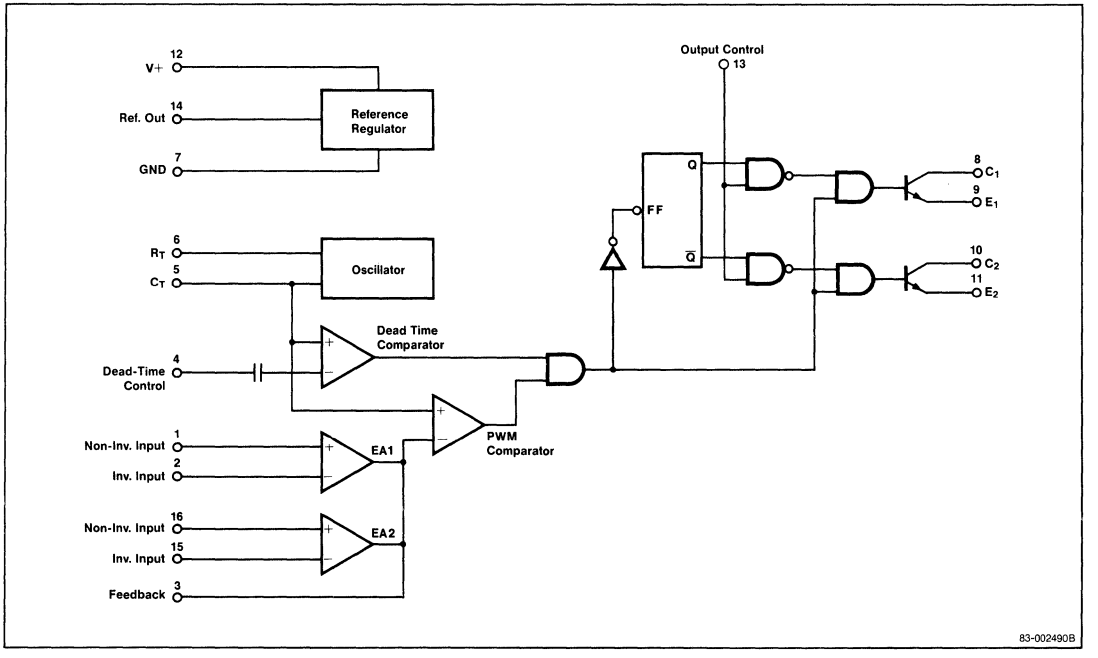
Features

- ☐ Complete PWM power control circuit
- ☐ Adjustable dead time (0 to 100%)
- ☐ No double pulsing of same output during load transient condition
- ☐ Dual error amplifiers have wide common mode input voltage capability (−0.3 V to V+ − 2 V)
- ☐ Circuit architecture provides easy synchronization
- ☐ Uncommitted outputs for 250 mA sink or source
- ☐ Equivalent to TL494

Pin Configuration



Equivalent Circuit



Ordering Information

Part Number	Package	Temperature Range
μPC494C	Plastic DIP	−20 °C to +85 °C
μPC494G2	Miniflat	−20 °C to +85 °C

Absolute Maximum Ratings

$T_A = 25°C$

Supply Voltage	41 V
Error Amplifier Input Voltage	V+ − 0.3 V
Output Voltage	41 V
Output Current	250 mA
Total Power Dissipation, C Package	1000 mW
Total Power Dissipation, G Package (Note 1)	780 mW
Operating Temperature Range	−20 to +85 °C
Storage Temperature Range	−65 to +125 °C

Note: 1. Mounted on 5x5 cm Glass-Epoxy PC board (thickness 1.6 mm)

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V+	7	12	40	V	
Output Voltage	V_O	−0.3		40	V	
Output Current	I_O			−0.3 200	mA	
Error Amplifier Sink Current	I_O			−0.3	mA	
Timing Capacitor	C_t	0.47		10,000	nF	
Timing Resistance	R_t	1.8		500	kΩ	
Oscillation Frequency	f_{osc}	1	40	500	kHz	
Operating Temperature	T_{OPT}	−20		+85	°C	

Electrical Characteristics

V+ = 15 V, f = 10 kHz, $-20 \leq T_{OPT} \leq +85°C$, unless otherwise noted

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Reference Section						
Output Voltage	V_{REF}	4.75	5	5.25	V	$I_{REF} = 1$ mA, $T_A = 25°C$
Line Regulation	REG_{IN}		2	25	mV	$7 V \leq V+ \leq 40 V$, $I_{REF} = 1$ mA, $T_A = 25°C$
Load Regulation	REG_L		1	15	mV	$1 mA \leq I_{REF} \leq 10$ mA, $T_A = 25°C$
Temperature Coefficient			0.01	0.03	%/°C	$-20°C \leq T_A \leq +85°C$, $I_{REF} = 1$ mA
Short Circuit Output Current	I_{SHORT}		35		mA	$V_{REF} = 0$
Oscillator Section						
Frequency	f_{osc}		10		kHz	$C_t = 0.01$ μF, $R_t = 12$ kΩ
Standard Deviation of Frequency			10		%	$7 V \leq V+ \leq 40 V$, C_t, R_t const., $T_A = 25°C$
Frequency Change with Temperature	$\Delta f/\Delta T$			2	%	$0°C \leq T_A \leq +85°C$, $C_t = 0.01$ μF, $R_t = 12$ kΩ
Frequency Change with Voltage	$\Delta f/\Delta V$			1	%	$7 V \leq V+ \leq 40 V$, $C_t = 0.01$ μF, $T_A = 25°C$, $R_T = 12$ kΩ
Dead-Time Control Section						
Input Bias Current	I_b		−2	−10	μA	$0 \leq V_{IN} \leq 5.25$ V
Maximum Duty Cycle (Each Output)		45			%	$V_I = 0$
Input Threshold Voltage	V_{TH}	0	3	3.3	V	Zero duty cycle, maximum duty cycle

Electrical Characteristics (Cont.)

V_{CC} = 12 V, T_A = 25°C, unless otherwise noted

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Error Amplifier Section						
Input Offset Voltage	V_{io}		2	10	mV	V_{OAMP} = 2.5 V
Input Offset Current	I_{io}		25	250	nA	V_{OAMP} = 2.5 V
Input Bias Current	I_b		0.2	1	μA	V_{OAMP} = 2.5 V
Common Mode Input Voltage, Low	V_{icm}	−0.3			V	7 V ≤ V+ ≤ 40 V
Common Mode Input Voltage, High	V_{icm}	V_{CC}−2			V	7 V ≤ V+ ≤ 40 V
Open Loop Voltage Amplification	A_{VOL}	60	74		dB	V_{OAMP} = 3 V
Unity Gain Bandwidth	GBW		500	650	kHz	
Common Mode Rejection Ratio	CMRR	65	80		dB	V+ = 40 V, T_A = 25°C
Output Sink Current	$I_{O\ SINK}$	0.3	0.6		mA	V_{OAMP} = 0.7 V
Output Source Current	$I_{O\ SOURCE}$	−2			mA	V_{OAMP} = 3.5 V
PWM Section						
Input Threshold Voltage			4	4.5	V	Zero Duty Cycle
Input Sink Current	$I_{O\ SINK}$	0.3	0.6		mA	$V_{(PIN3)}$ = 0.7 V
Output Section						
Collector Cutoff Current	I_{CBO}		2	100	μA	V_{CE} = 40 V, V+ = 40 V
Emitter Cutoff Current	I_{CEO}			−100	μA	V+ = V_{CO} = 40 V
Collector Saturation Voltage	$V_{CE(SAT)}$		1.1	1.3	V	I_C = 200 mA, V_E = 0, common emitter
	$V_{CE(ON)}$		1.5	2.5	V	I_E = 200 mA, V_C = 15 V, emitter follower
Output Voltage Rise Time, Common Emitter	t_r		100	200	ns	V+ = 15 V, R_L = 150 Ω, T_A = 25°C
Output Voltage Rise Time, Emitter Follower	t_r		100	200	ns	V+ = 15 V, R_L = 150 Ω, T_A = 25°C
Output Voltage Fall Time, Common Emitter	t_f		70	200	ns	V+ = 15 V, R_L = 150 Ω, T_A = 25°C
Output Voltage Fall Time, Emitter Follower	t_f		70	200	ns	V+ = 15 V, R_L = 150 Ω, T_A = 25°C
Total Device						
Standby Current	I_{CCSB}		8	12.5	mA	V+ = 15 V, all other inputs and outputs open
Bias Current	I_b		10		mA	$V_{(PIN4)}$ = 2 V, see figure 1

Note: Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \overline{X})^2}{N-1}}$$

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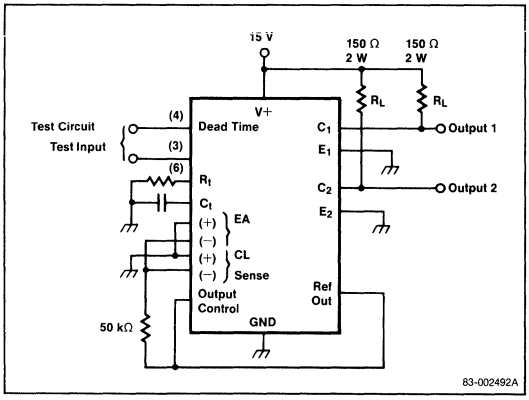
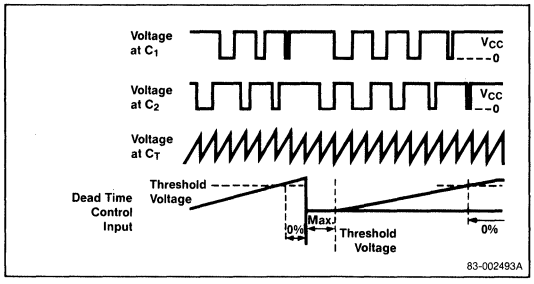
Test Circuit

Test Circuit



Typical Voltage Waveforms



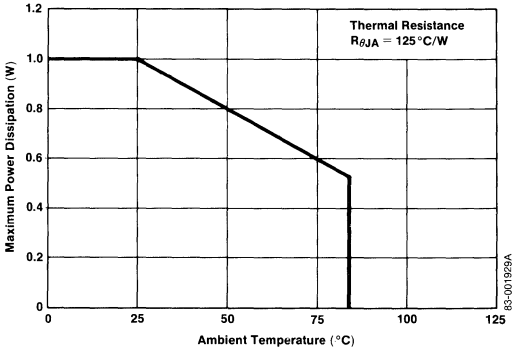
Function Table

Output Control Input (13 pin)	Output Function
At Ref-Out	Normal push-pull operation
Grounded	Single-ended or parallel output

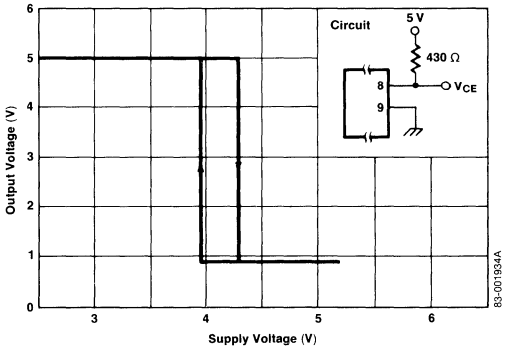
Operating Characteristics

$T_A = 25 \pm 2°C$, $V_{IN} = 15$ V

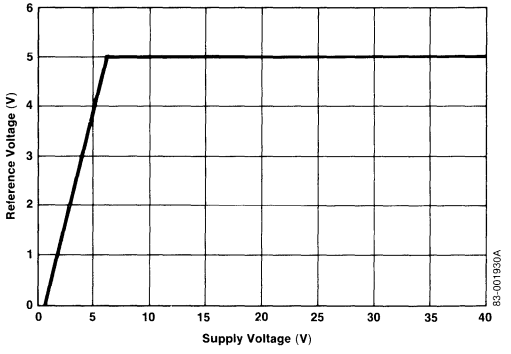
Maximum Power Dissipation



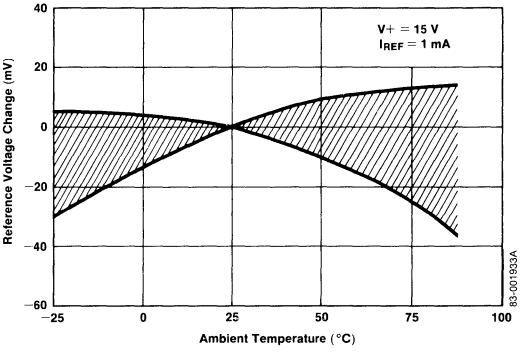
Mis-Operation Prevention Circuit Characteristics



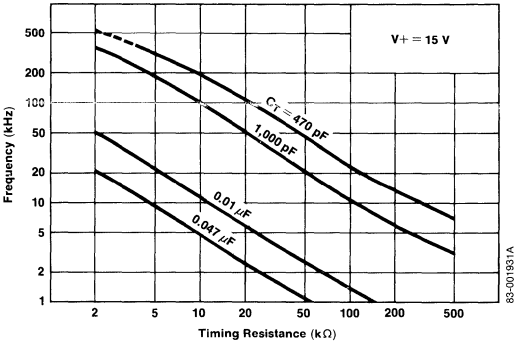
Reference Voltage vs. Supply Voltage



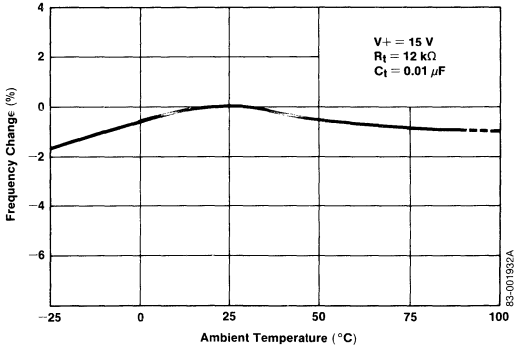
Reference Voltage vs. Temperature



Frequency vs. R_T and C_T



Frequency vs. Temperature



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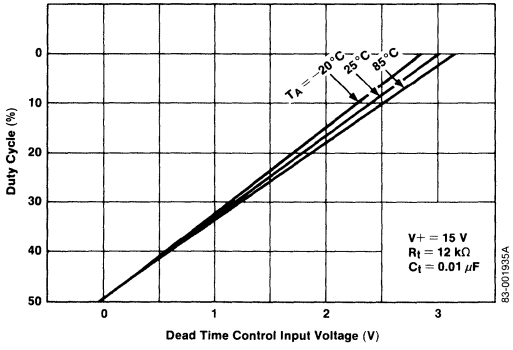
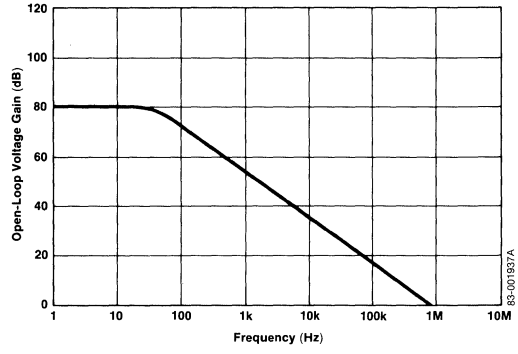
Operating Characteristics (cont.)

$T_A = 25 \pm 2°C$, $V_{IN} = 15$ V

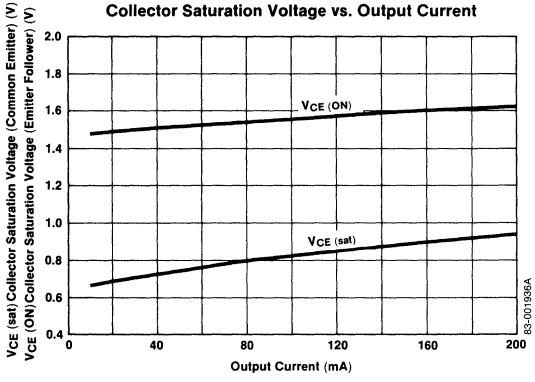
Duty Cycle vs. Dead Time Control Input Voltage



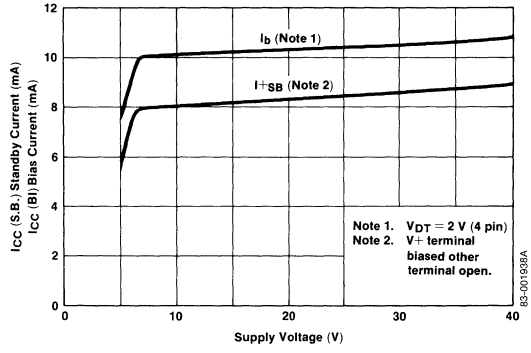
Open-Loop Voltage Gain vs. Frequency



Collector Saturation Voltage vs. Output Current

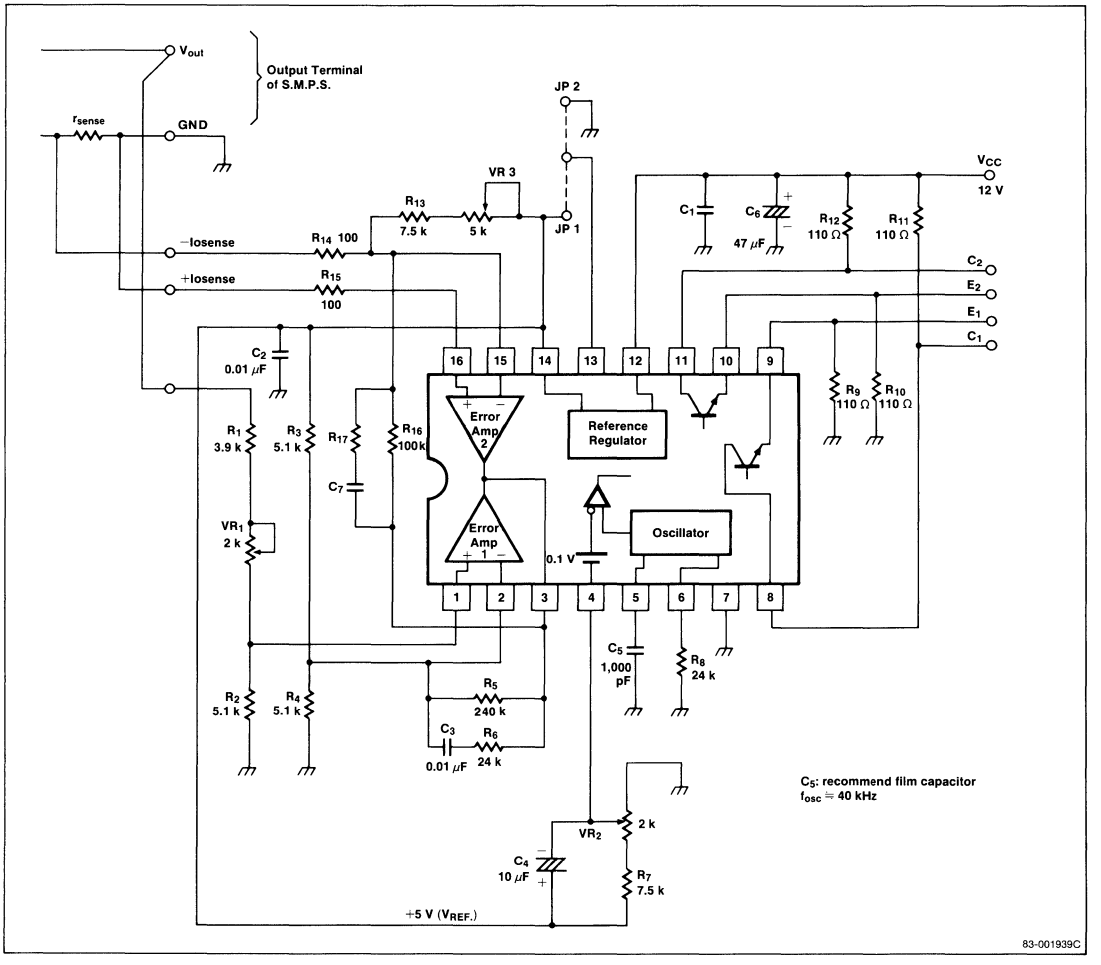


Standby and Bias Current vs. Supply Voltage



Typical Application Circuit (IC)

Circuit



Connection Diagram

Output Function	Output Control Input (13 pin)	Output Mode	Output Voltage Waveform
Push-Pull Operation	At Ref-Out (JP1 Wired)	Open Collector (R_9, R_{10} 0 Ω)	C1, C2
		Emitter Follower (R_{11}, R_{12} 0 Ω)	E1, E2
Single-Ended or Partial Output	Grounded (JP2 Wired)	Open Collector (R_9, R_{10} 0 Ω)	C1, C2
		Emitter Follower (R_{11}, R_{12} 0 Ω)	E1, E2

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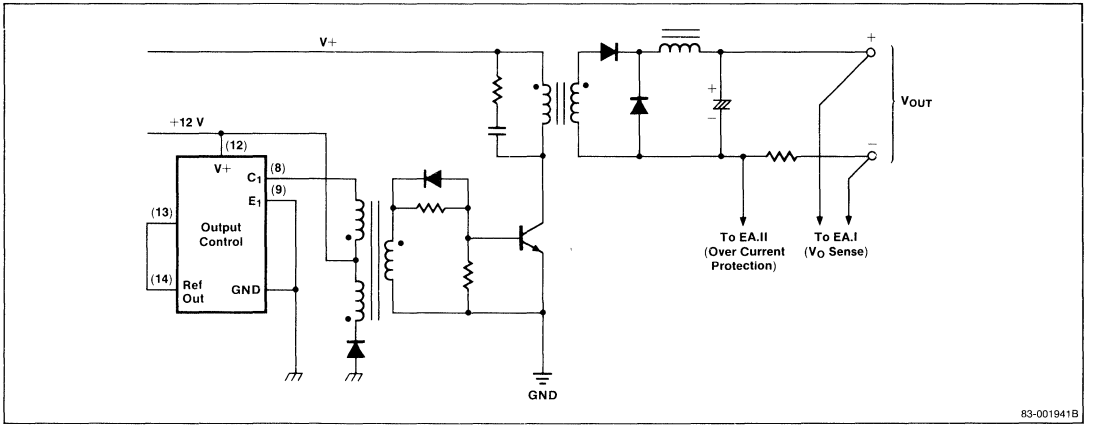
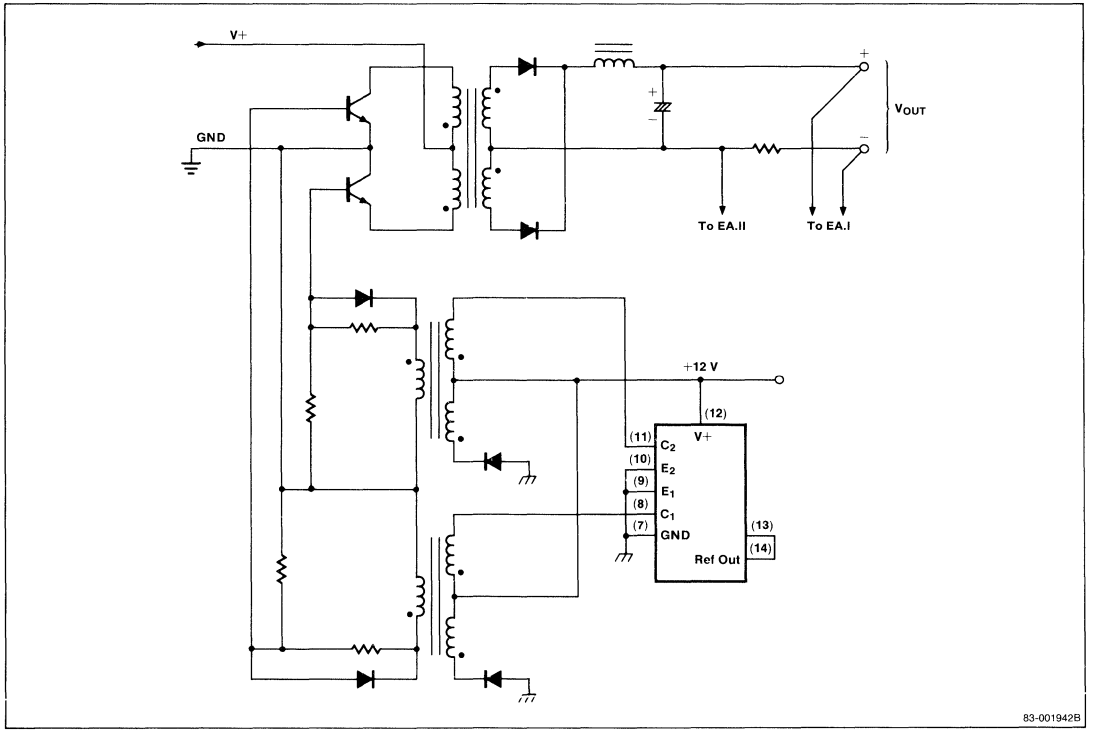
Typical Application Circuits

Forward Type

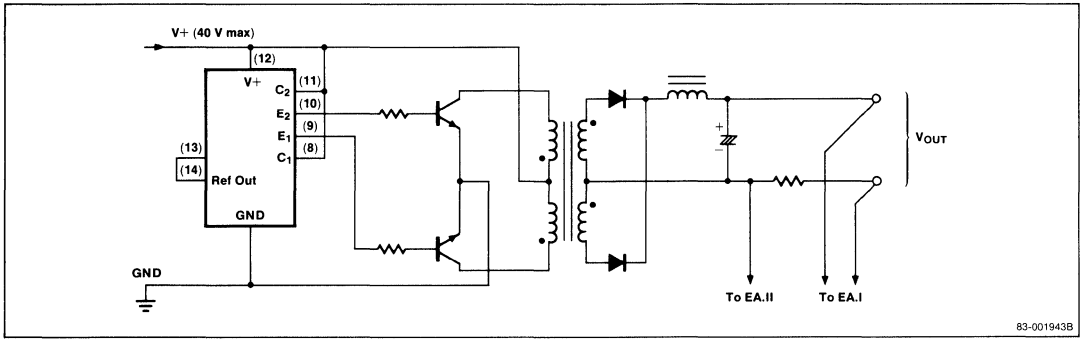


Push-Pull Type (Isolated)

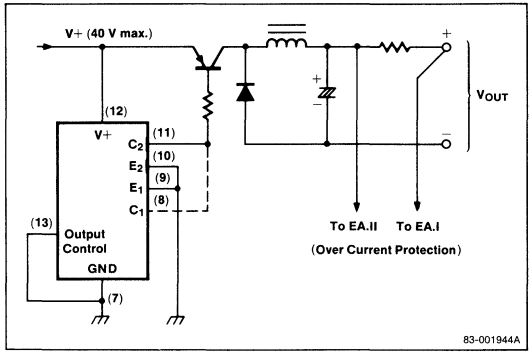


Typical Application Circuits (Cont.)

Push-Pull Type (Non Isolated)



Stepdown Chopper



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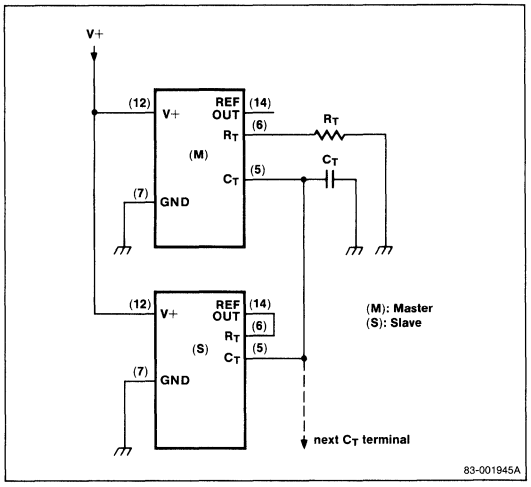
Synchronized Operation

If synchronized operation is needed, master-slave circuit can be used. This circuit is shown below. Initially, R_t terminal of slave IC is connected to Pin 14 (Ref Out) and internal oscillator is stopped.

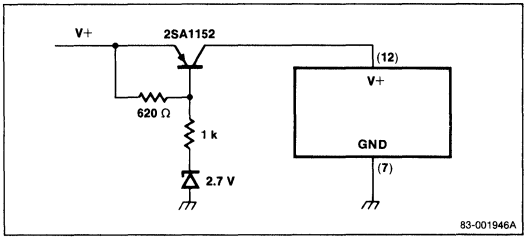
Synchronized Operation



Mis-operation Prevention Method

If the supply voltage drops below 2-2.5 V, the mis-operation prevention circuit is disabled. However, the internal flip-flop is still active and each output will be high. Thus, if prevention from this condition is desired, the following circuit may be used.

Mis-operation Prevention Method



μPC751/752
QUAD ADDRESSABLE READ/WRITE AMPLIFIER

Description

The μPC751 and the μPC752 are monolithic integrated circuits designed for reading and writing data in high performance magnetic disk storage systems, and are designed to mount on the head stack arm of hard disk units. Each IC contains four read preamplifiers, four write drivers, an output line driver, head select decoder circuitry, and fault monitoring circuits. These devices offer three modes of operation: Read, Write and Idle.

The μPC752 is similar to the μPC751 in function, but provides a lower differential gain in the read mode for higher inductance and higher output heads.

All signal levels and current specifications are fully IBM 3350 head and support arm compatible.

Ordering Information

Part Number	Package	Operating Temperature Range
μPC751B	Ceramic Flat	0°C to +70°C
μPC752B	Ceramic Flat	0°C to +70°C

Absolute Maximum Ratings

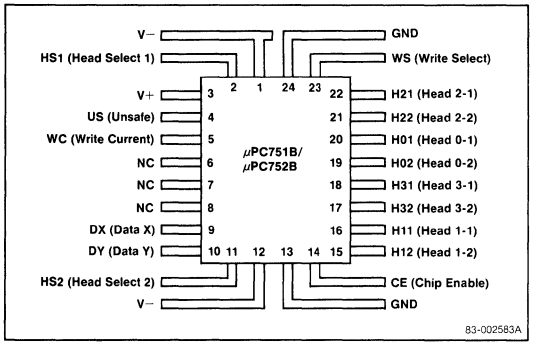
Positive Supply Voltage	−0.6 to 7.0 V
Negative Supply Voltage	−5.5 to 0.6 V
Input Voltage	V− − 0.3 to V+ +0.3
Storage Temperature Range	−65 to +150°C
Operating Moving-Air Temperature Range	0 to +70°C
Operating Junction Temperature Range	+150°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Limits

Parameter	Limits Min.	Limits Max.	Unit	Mode
V+	5.7	6.3	V	Read/Write/Idle
V−	−4.2	−3.8	V	Read/Write/Idle
Unsafe Voltage	4	V+ + 0.3	V	Read/Write/Idle
Head Center Tap Voltage	3.2	3.8	V	Write
Write Current (I_{WC})		45	mA	Write

Pin Configuration



Electrical Characteristics

Test Conditions (unless otherwise specified)

Parameter	Range	Unit	Mode
V+	6.00 ± 0.01	V	Read/Write/Idle
V−	−4.00 ± 0.01	V	Read/Write/Idle
V_{WS}	0.00 ± 0.01	V	Read
V_{WS}	3.50 ± 0.01	V	Write
V_{CE}	$0.00 \pm \begin{matrix}0.01\\0.00\end{matrix}$	V	Read/Write
L_h	Max. 0.1	μH	Read/Write/Idle
R_h	Max. 0.01	Ω	Read/Write/Idle
V_{CT}	0.00 ± 0.01	V	Read
V_{CT}	3.50 ± 0.01	V	Write
V_{US}	6.00 ± 0.01	V	Read/Write/Idle
R_{L1}	200 ± 1	Ω	Read/Write/Idle
R_{L2}	$101 \pm \begin{matrix}1\\0\end{matrix}$	V	Read/Write/Idle
I_{WC}	0	mA	Read
I_{WC}	40 ± 1	mA	Write
Ambient Temperature	25 ± 2	°C	Read/Write/Idle

Head Selection Table

Head Selected	VHS1	VHS2
0	V_{HHS}	V_{HHS}
1	V_{LHS}	V_{HHS}
2	V_{HHS}	V_{LHS}
3	V_{LHS}	V_{LHS}

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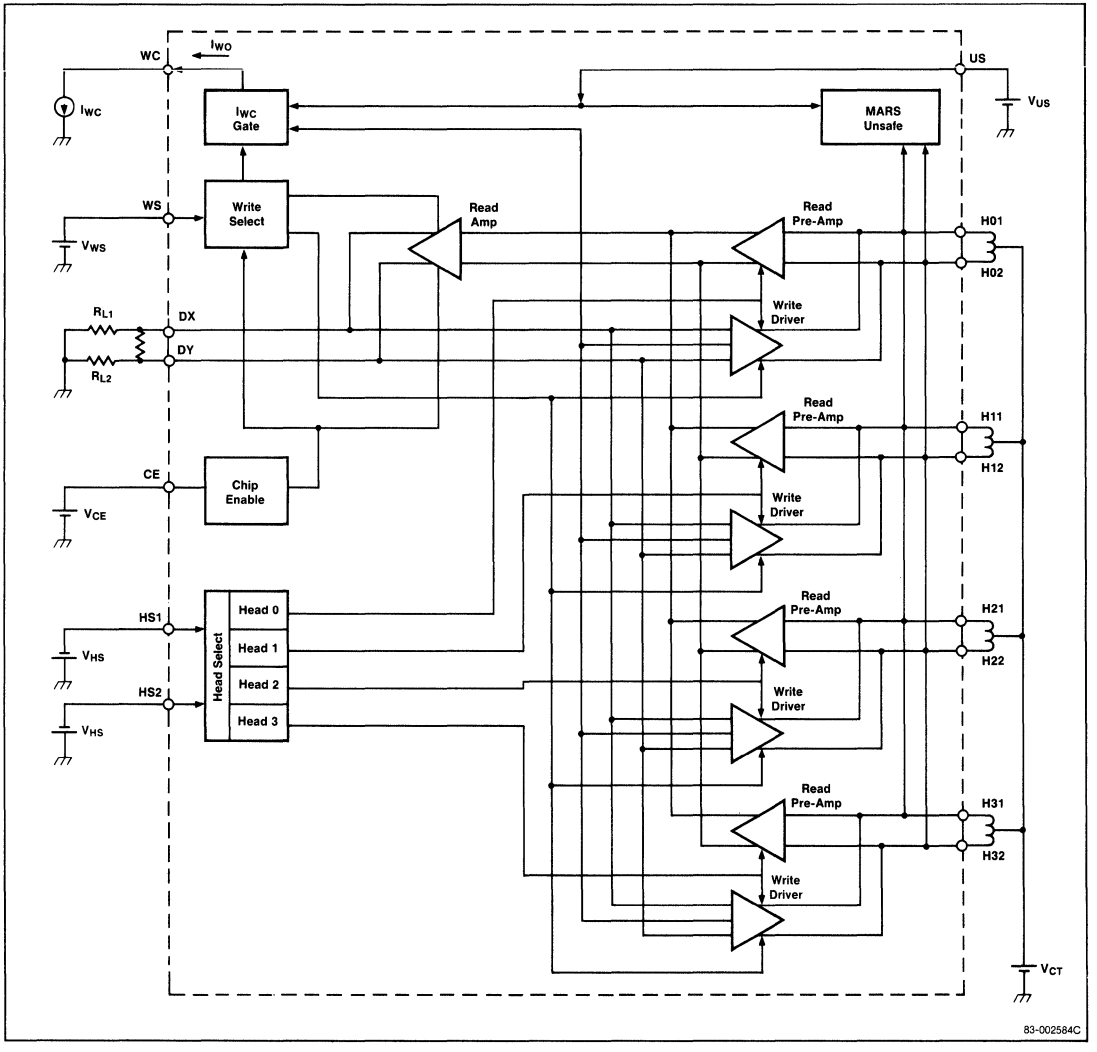
Connection Diagram



Mode Select

The circuit has three modes of operation: Read, Write and Idle. The state of the Chip Enable and Write Select determines the mode of operation as shown in the following tabie.

Mode Select

Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
Chip Enable				
V_{HCE}	5.5	6.3	V	Idle
V_{LCE}	0.0	0.7	V	Read/Write
I_{HCE}	−110	−50	μA	Idle, V_{CE} = V+ − 0.5 V
I_{LCE}	−1.3	−0.7	mA	Read/Write, V_{CE} = 0.0 V
Write Select				
V_{HWS}	3.2	3.8	V	Write/Idle
V_{LWS}	−0.1	0.1	V	Read/Idle
I_{HWS}	0.35	2.7	mA	Write/Idle (transition unsafe current off)
	0.7	3.5	mA	Write (transition unsafe current on)
I_{LWS}		0.1	mA	Read/Idle
Switching Delay		0.5	μs	All modes

Supply Current

Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
I_{CCRW}	12	20	mA	Read/Write
I_{CCID}		150	μA	Idle
I_{EERW}		70	mA	Read/Write
I_{EEID}		40	mA	Idle

Total Head Input Current

Sum of all head input currents with $I_{WC} = 0$

Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
$I_{HC(W)}$		3.0	mA	Write, V_{CT} = 3.5 V
$I_{HC(R)}$		0.16	mA	Read, V_{CT} = 0.0 V
$I_{HC(ID)}$		0.10	mA	Idle, V_{CT} = 3.5 or 0.0 V

Head Select

One of four heads may be selected by controlling the state of two head select inputs. The head is selected as specified below:

Head Select

Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
V_{HHS}	−0.97	−0.61	V	Temp = 0°C ~ 70°C
V_{LHS}	−2.38	−1.52	V	Temp = 0°C ~ 70°C
I_{HHS}		240	μA	
I_{LHS}		60	μA	
Switching Delay		50	ns	

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Read Mode (μPC751B)

In the Read mode the circuit functions as a low noise differential amplifier. The state of the head select inputs determines which amplifier is active.

Read Mode (μPC751B)

Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
Input Current		20	μA	$V_{IN} = 0$ V
Differential Input Capacity		18.8	pF	$V_{IN} = 0$ V
Differential Input Resistance (Damping Resistor)	585	915	Ω	$V_{IN} = 0$ V, 25°C
	565	915	Ω	$V_{IN} = 0$ V, 0°C
	585	984	Ω	$V_{IN} = 0$ V, 70°C
Output Offset Voltage		100	mV	$V_{IN} = 0$ V
Common Mode Output Voltage	−0.75	−0.50	V	$V_{IN} = 0$ V
Differential Gain	28	43	V/V	$V_{IN} = 1$ mVp-p, OVDC, f = 300 kHz, 25°C
	30	45	V/V	$V_{IN} = 1$ mVp-p, OVDC, f = 300 kHz, 0°C
	27	40	V/V	$V_{IN} = 1$ mVp-p, OVDC, f = 300 kHz, 70°C
Gain Linearity (DC)	0.9	1.1		$\dfrac{V_O (V_{IN} = 5\text{ mV}) - V_O (V_{IN} = 0\text{ mV})}{V_O (V_{IN} = 0.5\text{ mV}) - V_O (V_{IN} = 0\text{ mV})} \Big/ \dfrac{5.0\text{ mV}}{5.0\text{ mV}}$
Bandwidth	30		MHz	$Z_{IN} = 0\Omega$, $V_{IN} = 1 mV_{P-P}$ $\dfrac{\text{Gain @ } f_{BW}}{\text{Gain @ 300kHz}} = -3dB$
Input Noise		6.6	μVRMS	$V_{IN} = 0$ V, $Z_{IN} = 0\ \Omega$, 15 MHz power bandwidth
Common Mode Input to Differential Output Rejection Ratio	45		dB	$V_{IN} = 5$ mVp-p, OVDC, f ≤ 5 MHz
Power Supply Rejection Ratio (referred to the ΔV_{CC} or ΔV_{EE} = 0.1 Vp-p input)	45		dB	$V_{IN} = 0$ V, f ≤ 5 MHz
Channel Separation	40		dB	$V_{IN} = 1$ mVp-p, OVDC, f = 300 kHz, three channels driven
Unsafe Current		0.1	mA	Write Current = 0 mA
	40	45	mA	Write Current = 45 mA

Read Mode (μPC752B)

The same as μPC751B except for the following characteristics.

Read Mode (μPC752B)

Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
Output Offset Voltage		50	mV	$V_{IN} = 0$ V
Differential Gain	8.5	12.5	V/V	$V_{IN} = 1$ mVp-p, OVDC, f = 300 kHz, 25°C
	8.5	13.25	V/V	$V_{IN} = 1$ mVp-p, OVDC, f = 300 kHz, 0°C
	7.5	12.5	V/V	$V_{IN} = 1$ mVp-p, OVDC, f = 300 kHz, 70°C
Gain Linearity (DC)	0.9	1.1		$\dfrac{V_O (V_{IN} = 5\text{ mV}) - V_O (V_{IN} = 0\text{ mV})}{V_O (V_{IN} = 0.5\text{ mV}) - V_O (V_{IN} = 0\text{ mV})} \Big/ \dfrac{5.0\text{ mV}}{5.0\text{ mV}}$
Input Noise		25	μVRMS	$V_{IN} = 0$ V, $Z_{IN} = 0\ \Omega$, 15 MHz power bandwidth

Write Mode

In the Write mode the circuit functions as a current gate. Externally supplied Write current is gated by the state of the head select and data inputs to one side of one head.

Write Mode

Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
Differential Input Voltage	0.225		V	
Single Ended Input Voltage	−2.0	−0.45	V	
DX DY Input Current	−2.0	+2.0	mA	
Current Gain	0.95	1.0		I_{WC} = 45 mA
Write Current Voltage	−3.7	−3.0	V	I_{WC} = 45 mA
Head Current Transition Time		15	ns	I_{WC} = 45 ms, L_H = 0, f = 5 MHz
Head Current Switching Delay Time		15	ns	I_{WC} = 45 ms, L_H = 0, f = 5 MHz
Head Current Switching Hysteresis		2	ns	I_{WC} = 45 ms, L_H = 0, f = 5 MHz; data rise and fall time ≤ 1 ns
Unsafe Current		0.1	mA	I_{WC} = 30 mA, f = 2 MHz, L_H = 9 μH
	20		mA	I_{WC} = 30 mA, f = 2 MHz, L_H = 0 μH
	20		mA	I_{WC} = 45 mA, R_H = ∞ one side of head only
Unsafe Switching Delay Time		1.0	μs	I_{WC} = 30 mA, f = 2 MHz, L_H = 9 μH
	1.0	4.0	μs	I_{WC} = 30 mA, f = 2 MHz, L_H = 0 μH
	1.0	4.0	μs	I_{WC} = 45 mA, R_H = ∞
Unselected Head Current		1.5	mAo-p	I_{WC} = 45 mA, f = 2 MHz, L_H = 9.5 μH
Differential Head Voltage		9.0	Vo-p	I_{WC} = 45 mA, L_H = 10 μH

7

μPC754
MAGNETIC SERVO HEAD PREAMPLIFIER

Description

The μPC754 is a two stage wideband differential amplifier which features a very narrow gain range and 30 MHz bandwidth. This device is designed to be used primarily as the preamplifier for the servo head of the model 3348 head/arm assembly.

Features

- ☐ Very narrow gain range
- ☐ 30 MHz bandwidth

Ordering Information

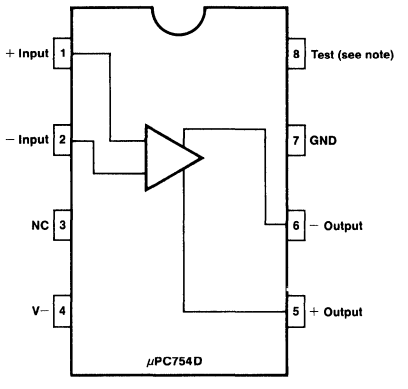
Part Number	Package	Operating Temperature Range
μPC754D	Ceramic DIP	0°C to +70°C

Absolute Maximum Ratings

Power Supply Voltage	−12 V
Differential Input Voltage	±1 V
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

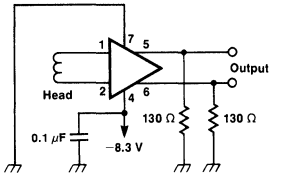
Pin Configuration



Note: Pin 8 cannot be connected to any circuit.

83-002585A

Connection Diagram



Note: A 0.1 μF ceramic capacitor is recommended for good power supply noise filtering.

83-002586A

7

Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V−	−7.45	−8.3	−9.15	V	
Input Signal	V_{IN}		2		mVpp	
Ambient Temperature	T_A	0		70	°C	

Electrical Characteristics

$T_A = 25°C$, V− = −8.3 V ±10%

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Differential Gain		77	93	110		$R_L = 130\ \Omega$
Bandwidth	BW	10	30		MHz	$V_{IN} = 2\ mV_{pp}$
Input Resistance	R_{IN}	800	1000	1250	Ω	
Input Capacitance	C_{IN}		3		pF	
Output Dynamic Range (Differential)		350			mVpp	$R_L = 130\ \Omega$
Power Supply Current	I_{CC}		26	35	mA	V− = −9.15 V
Output Offset	V_{OS}			±600	mV	$R_S = 0$, $R_L = 130\ \Omega$
Equivalent Input Noise	e_n		8	14	μV	$R_S = 0$, $R_L = 130\ \Omega$, BW = 4 MHz
PSPR, Input Referred	PSPR	50	65		dB	$R_S = 0$, $f \leq 5$ MHz
Gain Sensitivity (Supply)			±1.3		%	$R_L = 130\Omega$
Gain Sensitivity (Temperature)			−0.2		%/°C	$T_A = 25°C$ to 70°C, $R_L = 130\ \Omega$
CMRR, Input Referred	CMRR	55	70		dB	$f \leq 5$ MHz

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μPC1042
SWITCHING REGULATOR CONTROL CIRCUIT

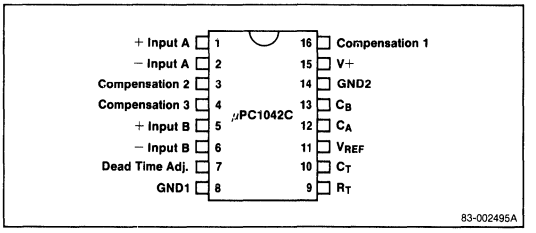
Description

The μPC1042 is a switching regulator control circuit designed for use in Switch Mode Power Supplies (SMPS). The μPC1042 uses the Pulse Width Modulator Technique (PWM) and features on chip voltage reference, dual error amplifiers, oscillator, pulse width modulator comparator, pulse steering flip flop, dual phase output drivers, and deadtime adjustment. The μPC1042 is ideal for forward and push-pull converters with minimum external circuitry.

Features

- ☐ Internal oscillator has symmetrical triangular waveform
- ☐ Adjustable dead time (0 to 100%)
- ☐ Includes a misoperation-preventing circuit at low input voltage
- ☐ No double pulsing of outputs
- ☐ Error amplifier II can operate with 0 V input voltage level

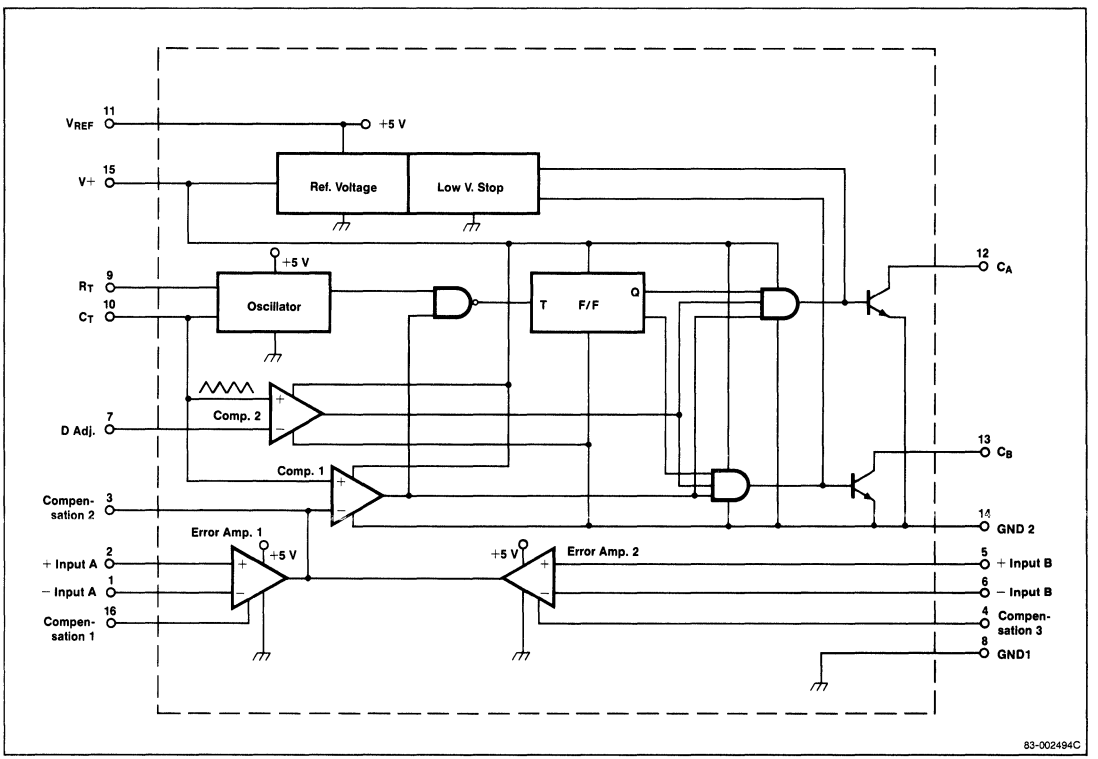
Pin Configuration



Ordering Information

Part Number	Package	Operating Temperature Range
μPC1042C	Plastic DIP	−20°C to +85°C

Equivalent Circuit



7

Absolute Maximum Ratings

$T_A = 25°C$

Supply Voltage	30 V
Output Voltage	40 V
Output Current (Each Output)	100 mA
Reference Output Current	40 mA
Total Power Dissipation	800 mW
Operating Temperature Range	−20 to +85°C
Storage Temperature Range	−40 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V+	8	12	16	V	
Output Voltage	V_O		24	32	V	
Output Current	I_O	5	20	40	mA	
Reference Output Current	I_{REF}	0	3	5	mA	
Oscillation Frequency	f_{osc}	20	40	100	kHz	

Electrical Characteristics

V+ = 12 V, $T_A = 25°C$ unless otherwise noted

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Reference Section						
Output Voltage	V_O	4.6	5.0	5.4	V	$I_O = 0$
Line Regulation	REG_{IN}		13	35	mV	$8\ V \le V+ \le 20\ V$, $I_{REF} = 0$
Load Regulation	REG_L		−2.5	−10	mV	$0 \le I_{REF} \le 20$ mA
Ripple Rejection	RR		60		dB	f = 120 Hz
V_{REF} Drift	$\Delta V_{REF}/\Delta T$		200	750	μV/°C	$-20°C \le T_{OPT} \le +85°C$
Low Voltage Stop Section						
Startup Voltage	V+(L to H)		7.5		V	$0 \le V+ \le 12$ V
Hysteresis Voltage	V_{HYS}		0.5		V	$0 \le V+ \le 12$ V
Oscillator Section						
Maximum Oscillation Frequency	f_{max}	100			kHz	
Initial Accuracy			±5	±10	%	R_T, C_T constant
Temperature Stability			−6	−10	%	$-20°C \le T_{OPT} \le +85°C$
Output Voltage (High)	V_{OH}		4		V	
Output Voltage (Low)	V_{OL}		2		V	
Line Frequency Stability			±1	±2	1%	$8\ V \le V+ \le 20$ V
Error Amplifier 1 Section						
Input Offset Voltage	V_{io}		±2	±10	mV	
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		±4	±10	μV/°C	$-20°C \le T_{OPT} \le +85°C$
Input Bias Current	I_B		+1.3	+10	μA	
Large Signal Voltage Gain	A_{VOL}	72	87		dB	
Common Mode Input Voltage	V_{icm}	1.2		4.0	V	
Common Mode Rejection Ratio	CMRR		70		dB	
Small Signal Bandwidth	GBW		2		MHz	$A_{V1} = 0$ dB, $C_1 = 560$ pF, $C_2 = 150$ pF

Electrical Characteristics (Cont.)

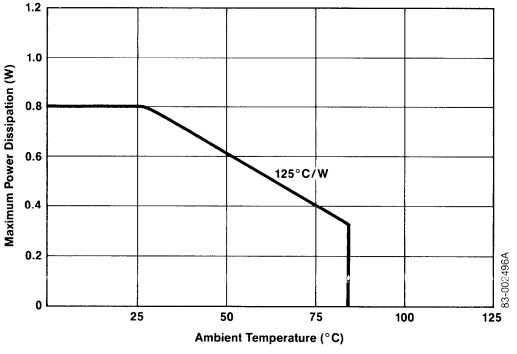
V+ = 12 V, T_A = 25°C unless otherwise noted

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Error Amplifier 2 Section						
Input Offset Voltage	V_{io}		±3	±10	mV	
Input Offset Voltage Drift	$\Delta V_{io}/\Delta T$		±3	±10	μV/°C	$-20°C \leq T_{OPT} \leq +85°C$
Input Bias Current	I_b		−1.5	−10	μA	
Large Signal Voltage Gain	A_{VOL}	72	100		dB	
Common Mode Input Voltage	V_{icm}	0		3	V	
Common Mode Rejection Ratio	CMRR		70		dB	
Small Signal Bandwidth	GBW		1.2		MHz	A_{V2} = 0 dB, C_3 = 220 pF, C_4 = 470 pF
Maximum Output Current				1.0	mA	
Dead Time Adjustment Section						
Input Bias Current	I_b		−4.5		μA	
Input Voltage (0% Duty)	V_{IN}		1.35		V	
Input Voltage (100% Duty)	V_{IN}		3.3		V	
Output Section						
Collector to Emitter Voltage	V_{CE}	40			V	I_C = 1 mA
Collector to Emitter Cutoff Current	I_{CEO}			10	μA	V_{CE} = 40 V
Collector Saturation Voltage	$V_{CE(SAT)}$		0.55	0.7	V	I_C = 20 mA
Rise Time	t_r		80		ns	I_C = 20 mA, V+ = 12 V, $R_L \fallingdotseq$ 560 Ω
Fall Time	t_f		70		ns	
Total Standby Current	I_{CCSB}		12	15	mA	V+ = 20 V, I_{REF} = 0

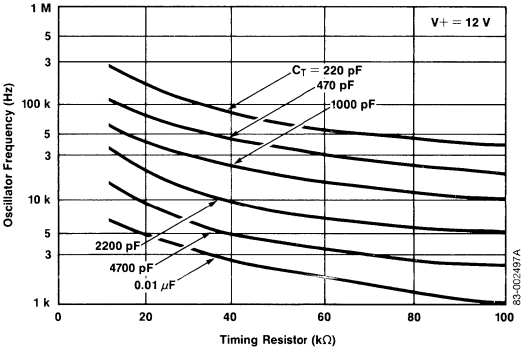
Operating Characteristics

T_A = 25°C

Maximum Power Dissipation



Oscillator Frequency vs. R_T and C_T



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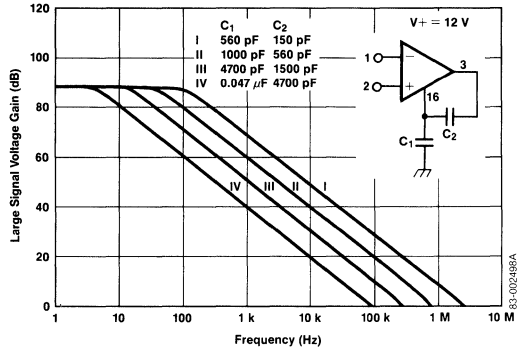
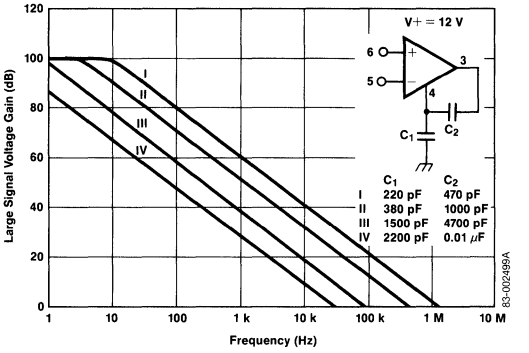
Operating Characteristics (Cont.)

$T_A = 25°C$

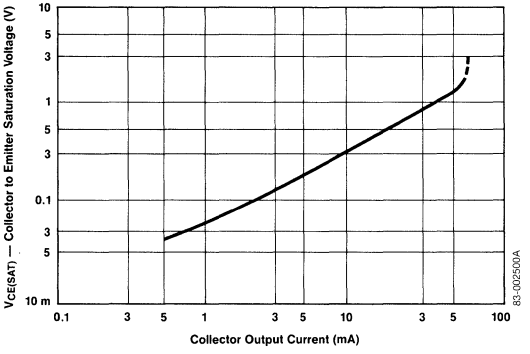
Error Amplifier I, A_{V1} vs. Frequency



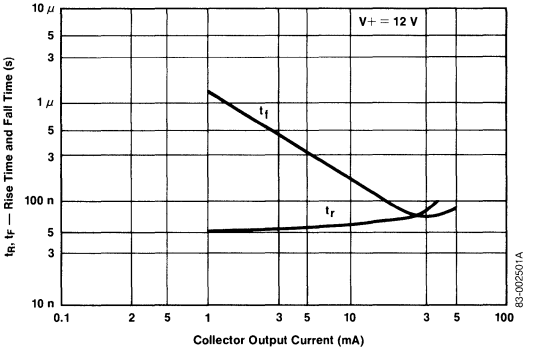
Error Amplifier II, A_{V2} vs. Frequency



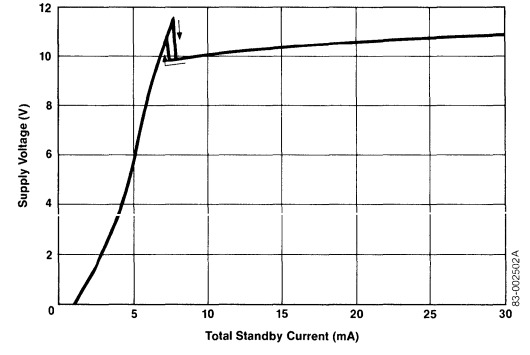
Correct Saturation Voltage vs. Collector Current



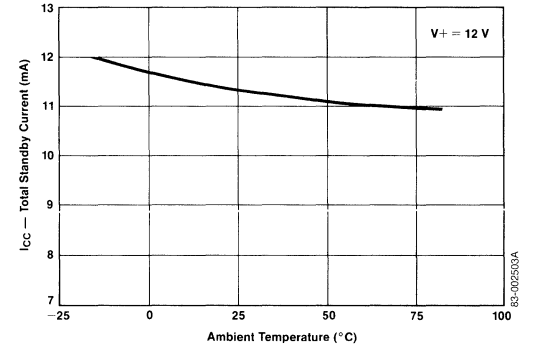
Output Section Rise Time and Fall Time vs. Collector Current



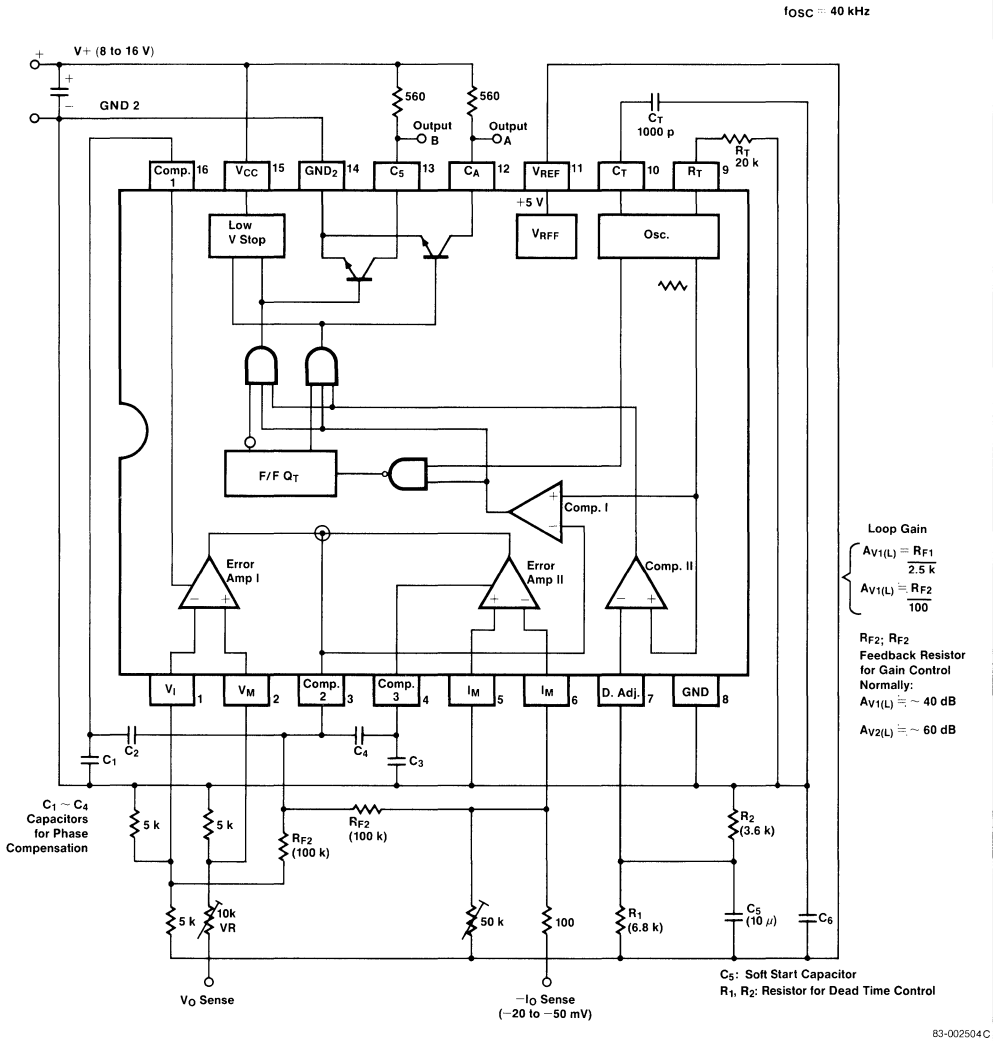
Total Standby Current vs. Supply Voltage



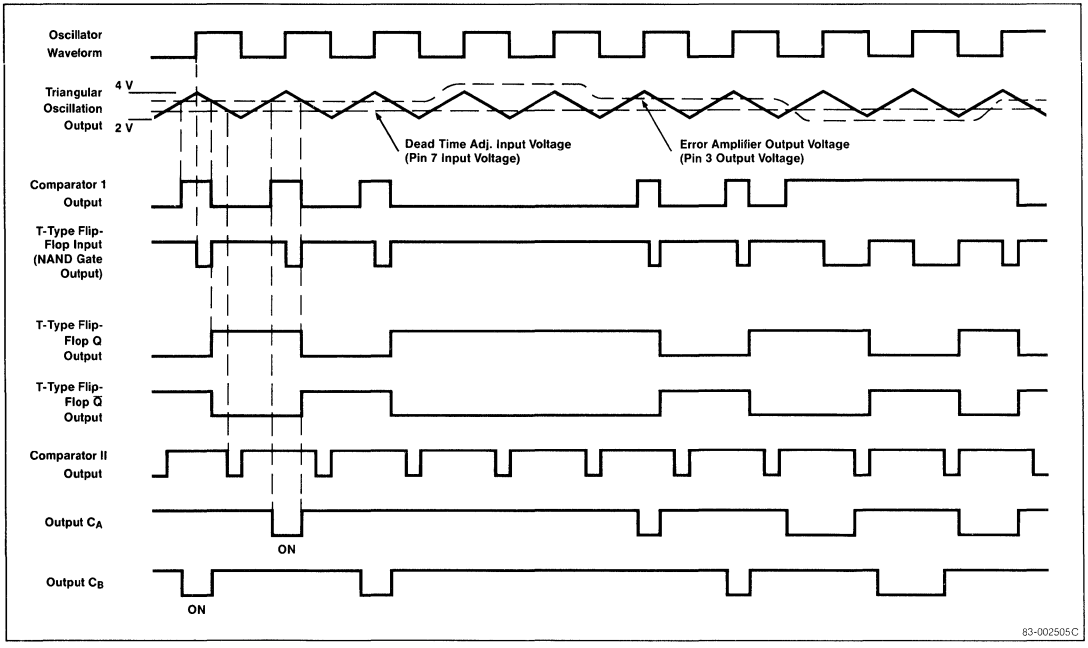
Total Standby Current vs. Ambient Temperature



Typical Application



Internal Waveforms (Timing Charts)



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μPC1060
PRECISION 2.5 VOLT REFERENCE REGULATOR

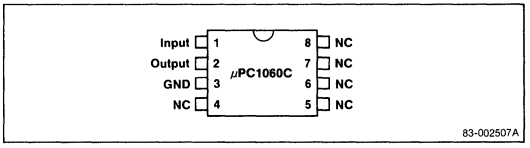
Description

The μPC1060 is a precision low voltage reference regulator which uses the band gap voltage reference technique. It features low temperature drift and low supply current drain. The μPC1060 is ideal for use in instrumentation and D/A converter applications.

Features

- ☐ High accuracy: $V_O = 2.5\ V \pm 1\%$
- ☐ Low temperature drift: $\Delta V_O/\Delta T \leq 40$ ppm/°C
- ☐ Low supply current: $I_{CC} \leq 1.5$ mA
- ☐ Equivalent to MC1403

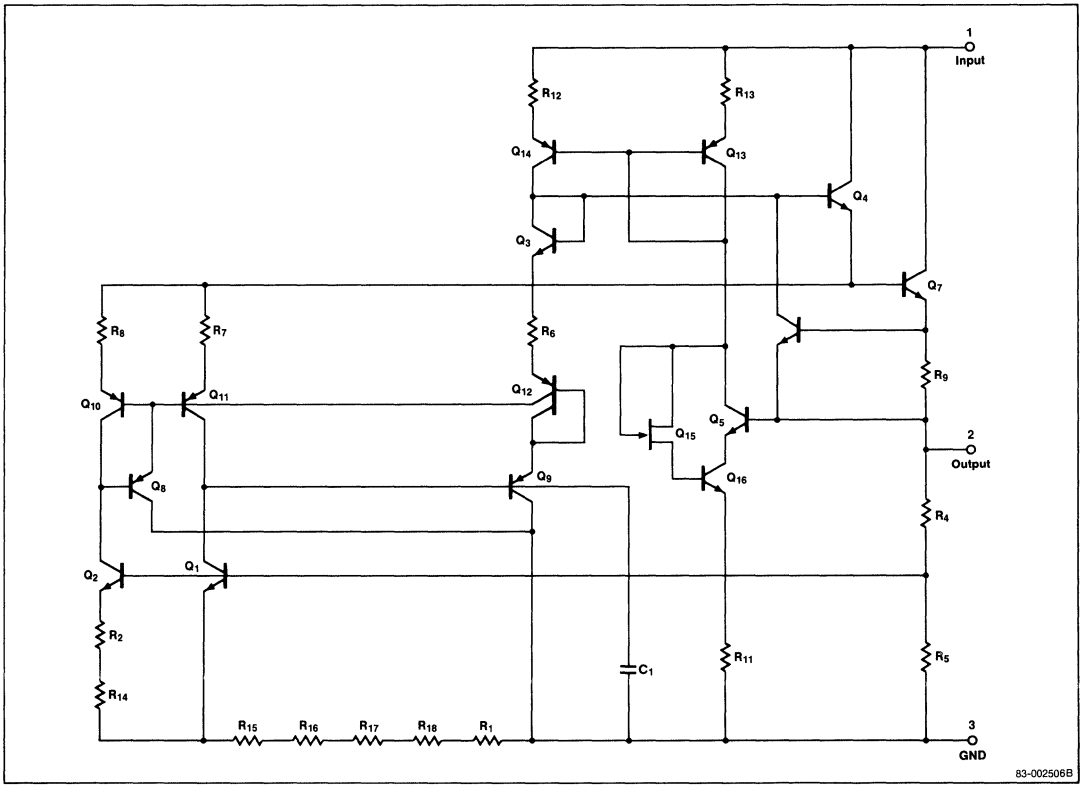
Pin Configuration



Ordering Information

Part Number	Package	Operating Temperature Range
μPC1060C	Plastic DIP	−20°C to +70°C

Equivalent Circuit



7

Absolute Maximum Ratings

Input Voltage	40 V
Power Dissipation	350 mW
Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

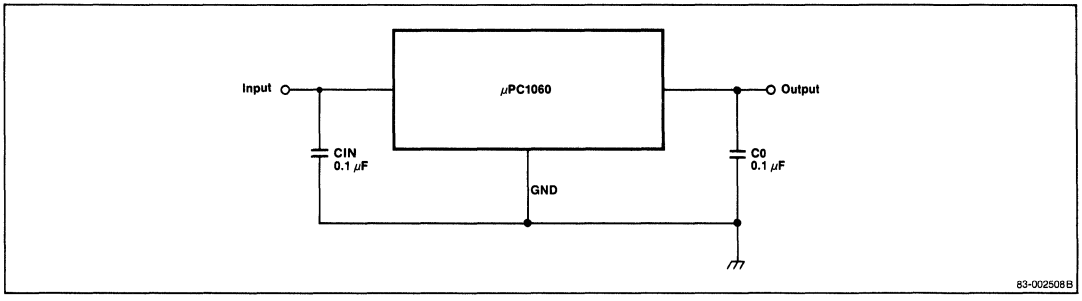
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit
Input Voltage Range	V_{IN}	4.5		40	V
Output Current	I_O	0		10	mA
Power Dissipation	P_D			350	mW
Operating Temperature	T_{OPT}	−20		+70	C°

Electrical Characteristics

$T_A = 25°C$, $V_{IN} = 15$ V, $I_O = 0$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_O	2.475	2.50	2.525	V	
Temperature Drift Output Voltage	$\Delta V_O/\Delta T$			40	ppm/°C	$-20°C \leq T_A \leq +70°C$
Output Voltage Change	V_O			7.0	mV	$-20°C \leq T_A \leq +70°C$
Line Regulation	REG_{IN}			4.5 3.0	mV	$15\ V \leq V_{IN} \leq 40\ V$ $4.5\ V \leq V_{IN} \leq 15\ V$
Load Regulation	REG_{LOAD}			10	mV	$6 \leq I_O \leq 10$ mA
Input Current	I_{IN}			1.5	mA	
Ripple Rejection Ratio	RR		90		dB	$5\ V \leq V_{IN} \leq 15\ V$, $I_O = 0$ f = 120 Hz
Output Noise Voltage	e_n		80		μV_{p-p}	$4.5\ V \leq V_{IN} \leq 40\ V$ $0 \leq I_O \leq 10$ mA
Output Short Circuit Current	I_{OSHORT}		17		mA	$V_O = 0$

Typical Circuit



μPC1555
PRECISION TIMER CIRCUIT

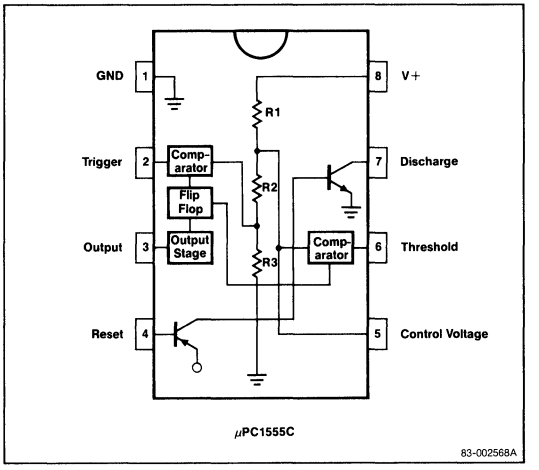
Description

The μPC1555 is a highly stable precision timer capable of producing oscillation in the astable mode and accurate time delays in the monostable mode. In the astable mode as an oscillator, the free running frequency and duty cycle are accurately controlled using two resistors and a capacitor. In the monostable or time delay mode, only one external resistor and capacitor is required. The totem pole output drivers can sink or source up to 200 mA making these devices ideal for driving small speakers, transducers, and single ended AC/DC converters.

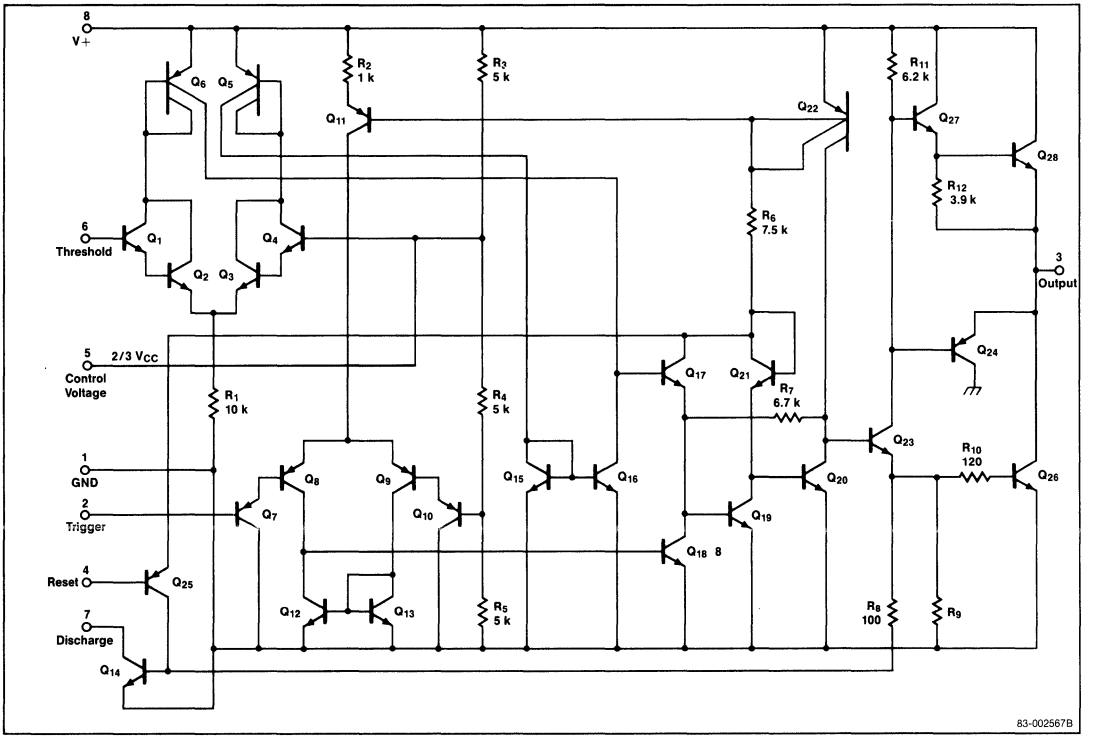
Features

- ☐ Operates in both astable and monostable mode
- ☐ Output can drive TTL loads
- ☐ Adjustable duty cycle
- ☐ NE555 direct replacement

Pin Configuration



Equivalent Circuit



7

Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and GND	18 V
Power Dissipation, C Package	600 mW
Power Dissipation, G2 Package	440 mW
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ordering Information

Part Number	Package	Operating Temperature Range
μPC1555C	Plastic DIP	0°C to +70°C
μPC1555G2	Plastic Miniflat	0°C to +70°C

Electrical Characteristics

$T_A = 25°C$, $V^+ = +5$ V to +15 V

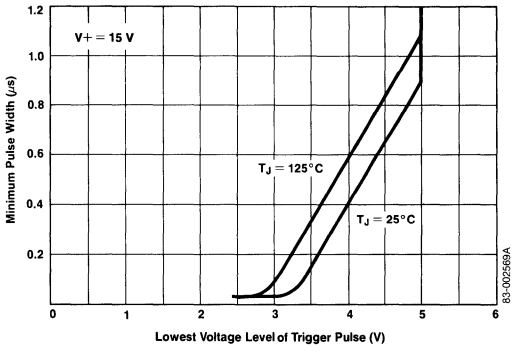
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V+	4.5		16	V	
Supply Current	I_{CC}		3	6	mA	V+ = 5 V, $R_L = \infty$, V_O = 0 V
			10	15	mA	V+ = 15 V, $R_L = \infty$, V_O = 0 V
Threshold Voltage	V_{th}		2/3 V+		V	
Threshold Current	I_{th}		0.1	0.25	μA	Note 1
Trigger Voltage	V_{TRIG}		5		V	V+ = 15 V
			1.67		V	V+ = 5 V
Trigger Current	I_{TRIG}		0.5		μA	
Reset Voltage	V_{RST}	0.4	0.7	1.0	V	
Reset Current	I_{RST}		0.1		mA	
Control Voltage Level		9.0	10	11	V	V+ = 15 V
		2.6	3.33	4	V	V+ = 5 V
Output Voltage Drop (Low)	V_{OL}		0.1	0.25	V	V+ = 15 V, I_{SINK} = 10 mA
			0.4	0.75	V	V+ = 15 V, I_{SINK} = 50 mA
			2.0	2.5	V	V+ = 15 V, I_{SINK} = 100 mA
			2.5		V	V+ = 15 V, I_{SINK} = 200 mA
			0.1	0.35	V	V+ = 5 V, I_{SINK} = 5 mA
Output Voltage Drop (High)	V_{OH}		12.5		V	V+ = 15 V, I_{SOURCE} = 200 mA
		12.75	13.3		V	V+ = 15 V, I_{SOURCE} = 100 mA
		2.75	3.3		V	V+ = 5 V, I_{SOURCE} = 100 mA
Rise Time Output	t_R		100		ns	
Fall Time Output	t_F		100		ns	
Timing Error, Astable: Initial Accuracy			1		%	R_A, R_B = 1 k to 100 kΩ, C = 0.1 μF
Drift with Temperature			50		ppm/°C	
Drift with Supply			0.01		%/V	

Notes: 1. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total resistance is 20 MΩ.

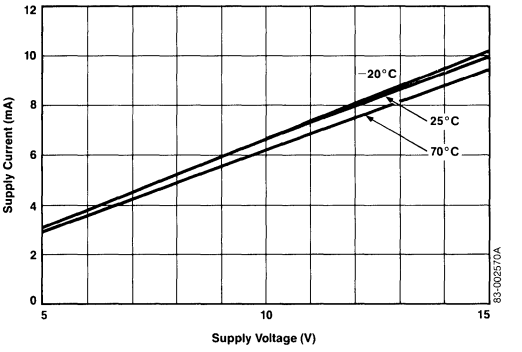
Operating Characteristics

$T_A = 25°C$

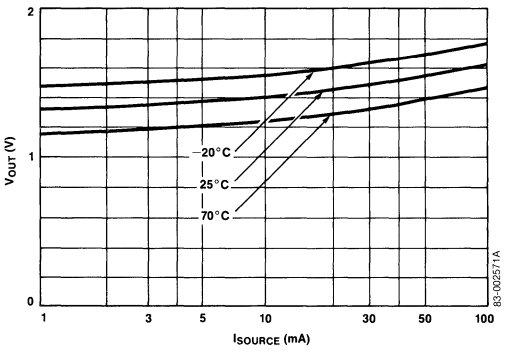
Minimum Pulse Width Required for Triggering



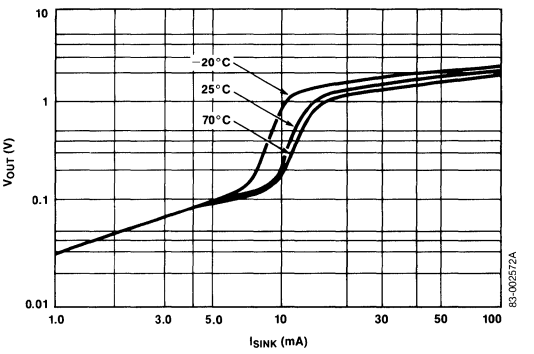
Supply Current vs. Supply Voltage



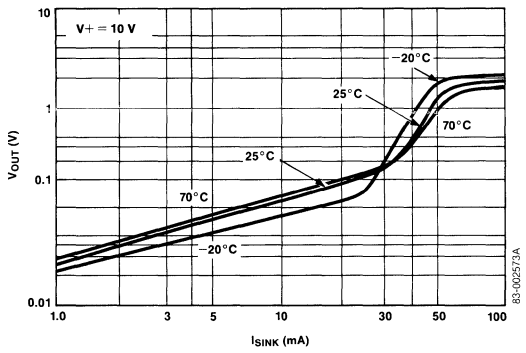
High Output Voltage Drop vs. Output Source Current



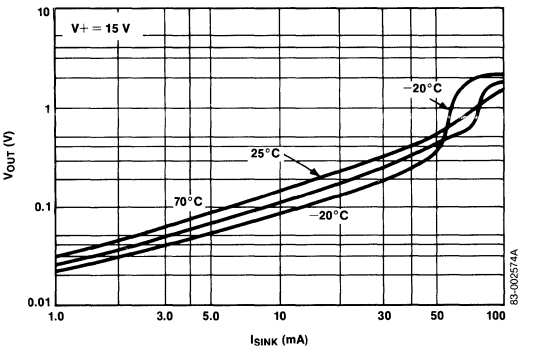
Low Output Voltage vs. Output Sink Current



Low Output Voltage vs. Output Sink Current



Low Output Voltage vs. Output Sink Current

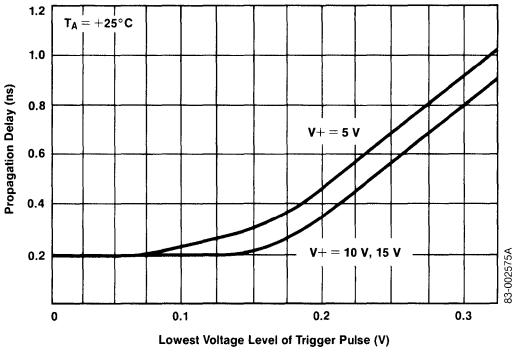


7

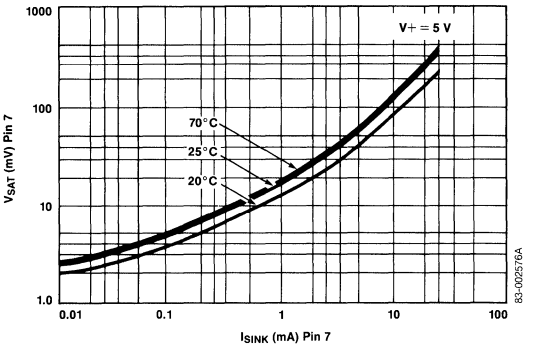
Operating Characteristics (Cont.)

$T_A = 25°C$

Output Propagation Delays vs. Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs. Sink Current



Applications

Monostable Operation

When the timer is operated as a monostable multivibrator, one external capacitor (C_1), and one external resistor (R_1), are used as shown in figure 1. When the trigger input is reduced below 1/3 V+, the timer internal flip-flop is set. This releases the short circuit across the external capacitor and the Q output goes HIGH. The voltage across the capacitor voltage reaches 2/3 V+, the internal comparator resets the flip-flop and the external capacitor (C_1), is rapidly discharged, provided the trigger voltage is returned above 1/3 V+ (figure 2). The output is now in LOW state and a new timing cycle may be initiated. The time that the output is in the HIGH state is given by 1.1 R.C., or can be taken directly from figure 3. Both the charge rate and internal threshold are directly proportional to the supply voltage. Thus, the timer output pulse width is independent of the power supply voltage. If a LOW is applied to the reset input, the output is forced LOW and the external capacitor discharged regardless of the other inputs.

Astable Operation

When the timer is operated in the astable mode, two external resistors (R_1 and R_2), and one external capacitor (C_1), are used as shown in figure 4. With this connection scheme, the external capacitor (C_1), charges and discharges between 1/3 V+ and 2/3 V+. The charge time (output HIGH) is:

$$t = 0.693(R_1 + R_2)C_1$$

The discharge time (output LOW) is:

$$t_2 = 0.693R_2C_1$$

The total period for one cycle of output HIGH and output LOW is:

$$t = t_1 + t_2 = 0.693\ (R_1 + R_2)C_1$$

The frequency for this period, T, is:

$$f = \frac{1}{t} = \frac{1}{0.693(R_1 + R_2)C_1}$$

The astable free-running frequency can also be found from the graph shown in figure 6. The duty cycle, the time the output is LOW divided by the period, is given by:

$$D = \frac{t_2}{t_1 + t_2} = \frac{R_2}{R_1 + R_2}$$

Figure 1. Monostable Circuit

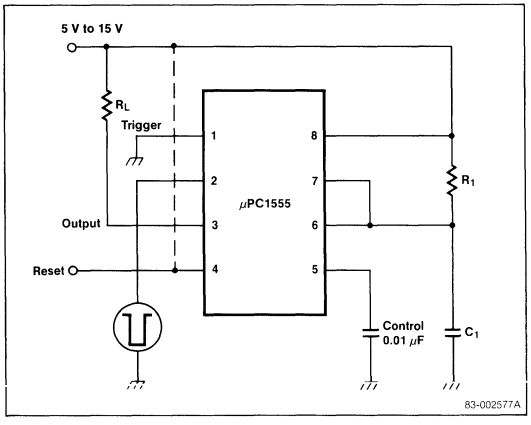
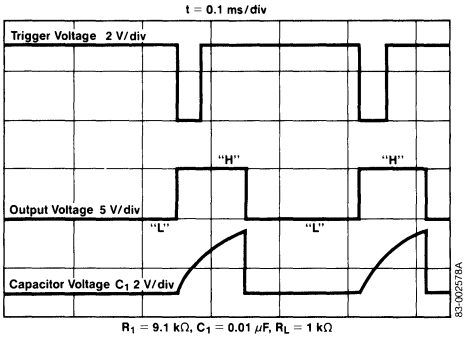


Figure 2. Monostable Waveforms



R_1 = 9.1 kΩ, C_1 = 0.01 μF, R_L = 1 kΩ

Figure 3. Time Delay

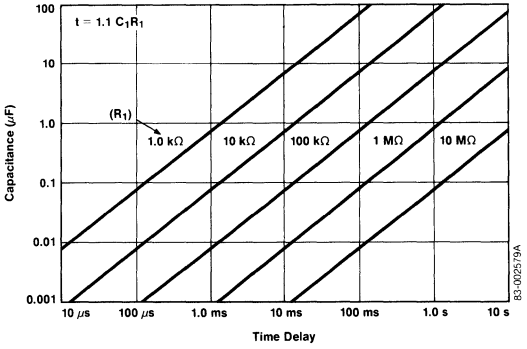


Figure 4. Astable Circuit

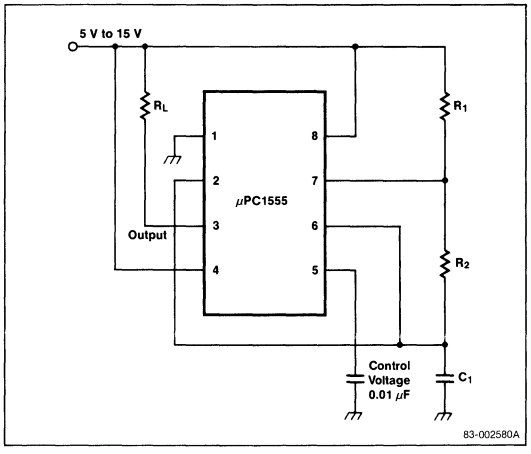
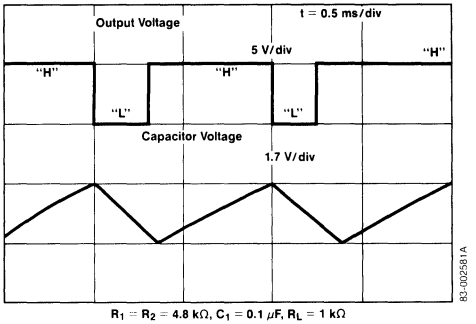
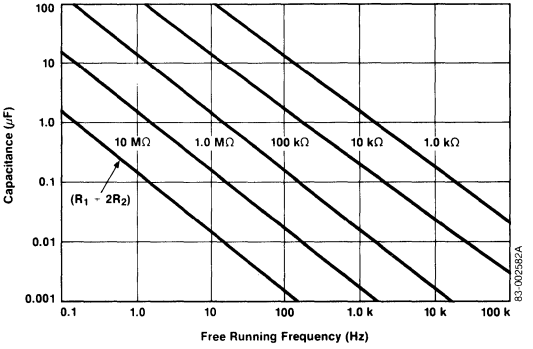


Figure 5. Astable Waveform



R_1 = R_2 = 4.8 kΩ, C_1 = 0.1 μF, R_L = 1 kΩ

Figure 6. Free Running Frequency



7

Description

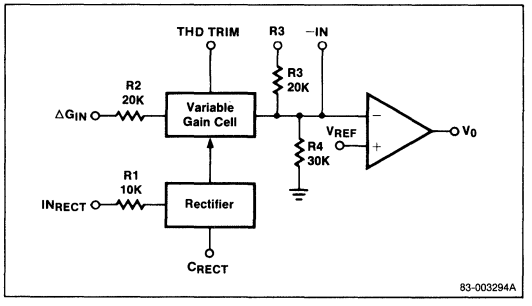
The μPC1571 is a dual gain control circuit in which either channel may be used as a dynamic range compressor or expander. Each channel contains a fullwave rectifier, a temperature compensated variable gain cell, and an operational amplifier.

This circuit is well suited for use in telephone systems, limiters, voltage control amplifiers, and noise reduction circuits.

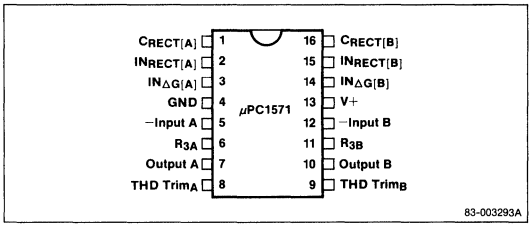
Features

- ☐ Single power supply operation
- ☐ Temperature compensated
- ☐ Complete compressor and expander in a single package
- ☐ Dynamic range greater than 70 dB
- ☐ Outputs fully protected against short circuits

Block Diagram



Pin Configuration



Ordering Information

Part Number	Package	Operating Temperature Range
μPC1571C	16 pin Plastic DIP	0°C to +70°C

Absolute Maximum Ratings

T_A = +25°C

Power Supply	16 V
Input Voltage (Note 1)	16 V
Power Dissipation	400 mW
Storage Temperature	−55 to +125°C

Note: 1. Applies to all input terminals.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits Min	Typ	Max	Unit
Operating Temperature	T_{op}	0		70	°C
Power Supply	V+	6	8	13.5	V
Rectifier Capacitor	C_{RECT}	2.0	2.2		μF

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Electrical Characteristics

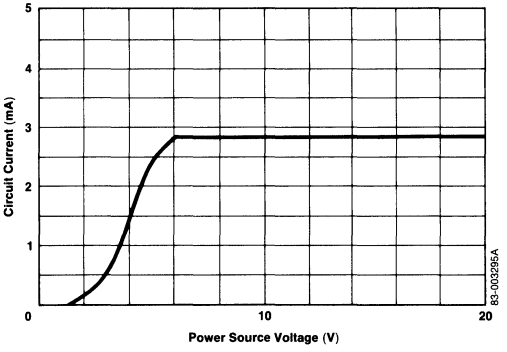
T_A = +25°C, V+ = 8 V, C_{RECT} = 2.2 μF

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Power Supply Current	I_{CC}		2.5	4.0	mA	V_{IN} = 0 V
Internal Reference Voltage	V_{ref}	1.7	1.8	1.9	V	T_A = 0°C to +70°C
V_{ref} Change with Temperature	$\Delta V_{ref}/\Delta T$		15	30	mV/°C	
Output Current	I_O	±10			mA	
Slew Rate	SR		0.2		V/μs	
Internal Resistor Tolerance		−20		+20	%	T_A = 0°C to +70°C
Change with Temperature			1200	1800	ppm/°C	
Unity Gain Level	f_{unity}	−1.5	0	+1.5	dBm	$V_{IN} = V_O$
Total Harmonic Distortion	THD		0.5	2	%	
Expander Output Noise	V_N		−100		dBm	Δf = 3 kHz
Gain Variation A	ΔG_A	−0.2	0	+0.2	dB	V_{IN} = −30 dBm, T_A = 0° to +70°C, f = 1 kHz to 5 kHz
Gain Variation B	ΔG_B	−0.5	0	+0.5	dB	
Compressor Output	V_O	−20.2	−20	−19.5	dB	V_{IN} = −20 dB
		−40.4	−40	−39.3	dB	V_{IN} = −40 dB
		−61.0	−60	−58.3	dB	V_{IN} = −60 dB
			−80		dB	V_{IN} = −80 dB
Expander Output	V_O	−10.5	−10	−9.8	dB	V_{IN} = −10 dB
		−20.7	−20	−19.6	dB	V_{IN} = −20 dB
		−31.5	−30	−29.0	dB	V_{IN} = −30 dB
			−40		dB	V_{IN} = −40 dB
Channel Separation	CS	60			dB	

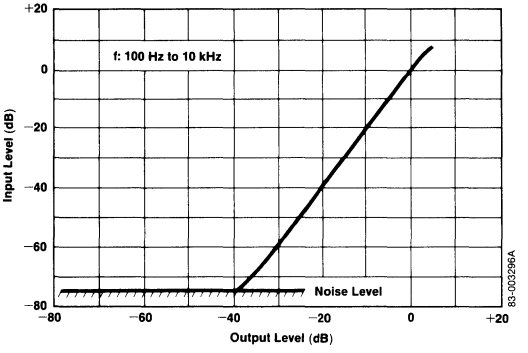
Operating Characteristics

$T_A = 25°C$

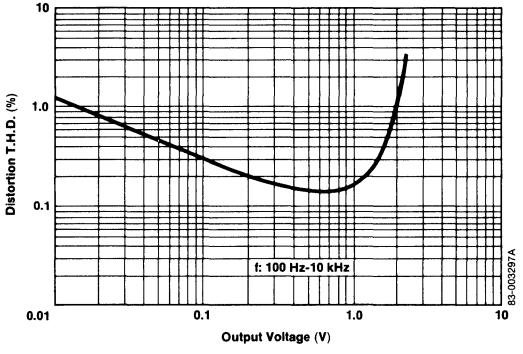
Power Supply Characteristics



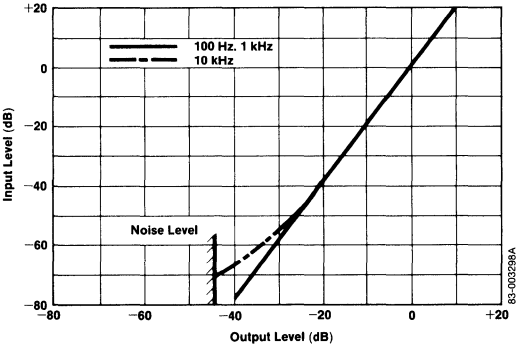
Expander Characteristics



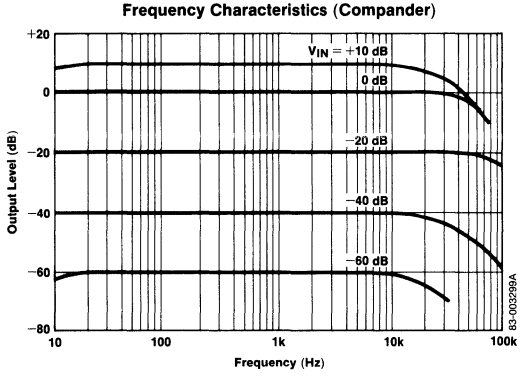
Distortion-Output Voltage Characteristics (Compander)



Compressor Characteristics



Frequency Characteristics (Compander)



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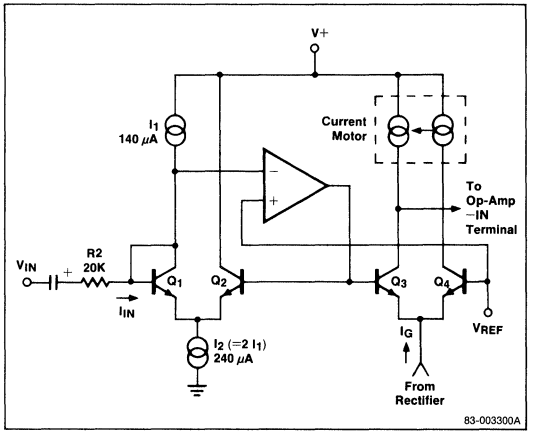
Gain Cell Operation

The gain cell is a multiplier comprised of two transistor pairs. I_1 and I_2 are fixed within the IC; I_G is a control current supplied by the rectifier. This current determines the amount of output amplification:

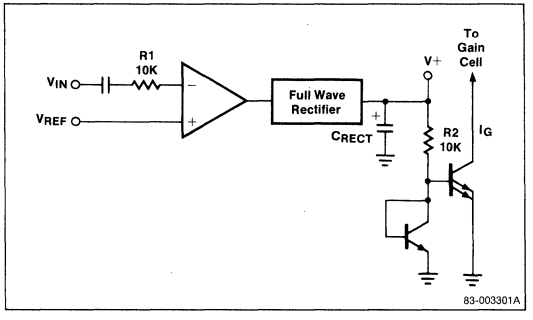
$$I_0 = \frac{I_G \cdot I_{IN}}{140\ \mu A} = \frac{I_G \cdot V_{IN}}{R_1}$$



Rectifier Operation

The output current of the op-amp is averaged by C_{RECT} R_2 then doubled to become I_G:

$$I_G = \frac{V_{IN\ (avg)}}{R_1}$$



Compressor Operation

Using the μPC1571 as a compressor involves placing an expander in the op-amp feedback circuit. For example, if the input increases by 6 dB, the output is limited to 3 dB. The 3 dB increase produces a 3 dB increase in the output of the gain cell, which results in a 6 dB increase in feedback current.

$$\text{Gain} = \frac{.84}{V_{IN\ (avg)}}$$

$$V_0 = (\text{gain})\ (V_{IN})$$

Note that op-amp feedback is AC only. C_{DC} and the two R_{DC} provide DC feedback to set the DC bias at the op-amp output:

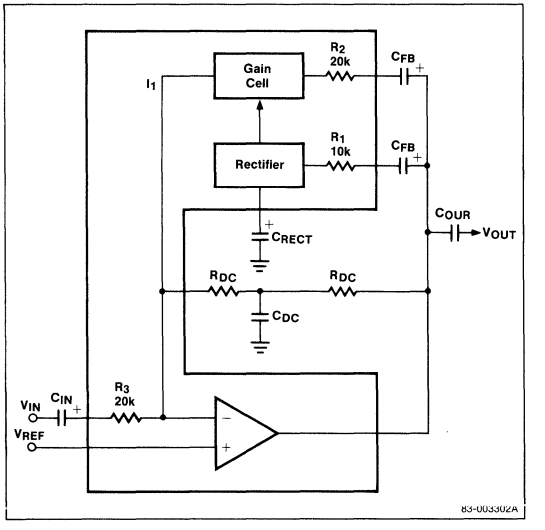
$$V_{OPO\ (DC)} = (1 + \frac{R_{DC\ (total)}}{R_4})\ V_{REF}$$

The output of the compressor will be biased at 3 V DC, assuming the internal resistors are used:

$$V_{O\ (DC)} = (1 + \frac{R_3}{R_4})\ V_{REF}$$

Note that external resistors may be placed in series with R_3 to change the gain, or with R_4 to change the output DC bias.

1/2 μPC1571

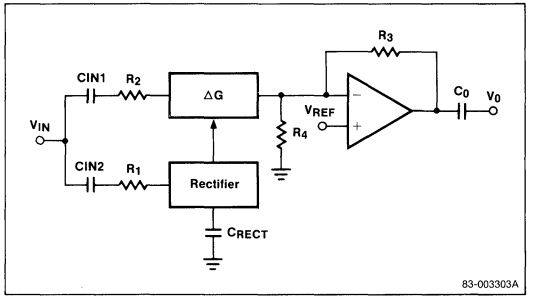


Expander Operation

When connected as an expander, the input signal is applied to both the rectifier and the gain cell. When the signal drops by 6 dB, the gain current drops by a factor of 2 so the overall gain drops by 6 dB. Thus the output level will drop by 12 dB.

Gain = (1.43) ($V_{IN\ (avg)}$)

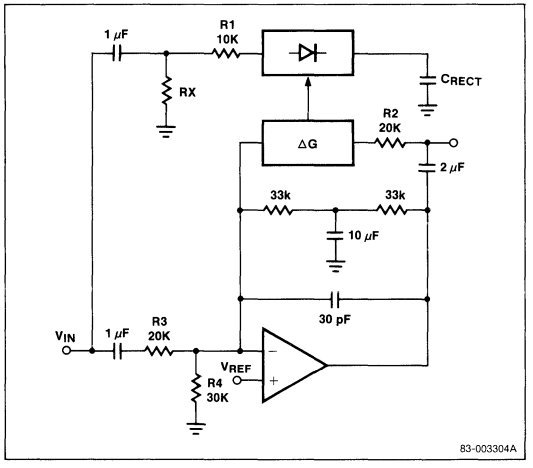
V_O = (gain) (V_{IN})



Applications

A. Automatic Level Control

With the rectifier input tied to V_{IN}, a very high performance ALC can be built. Gain is inversely proportional to input level, so a 20 dB drop in input produces a 20 dB increase in gain. Circuit shown will maintain a fixed output ±1 dB from −43 dBm to +14 dBm at 1 kHz.



7

NEC

NEC Electronics Inc.

μPC1663/1664 ULTRA-WIDEBAND DIFFERENTIAL AMPLIFIER

PRELIMINARY INFORMATION

Description

The μPC1663 and μPC1664 are video amplifiers with differential input and output stages. An ultrahigh-frequency process (f_T = 6 GHz) improves ac performance compared with industry-standard type 733 video amplifiers. The μPC1663 and μPC1664 are excellent as sense amplifiers for high-density CCDs, as video or pulse amplifiers in high-resolution displays, and in communications equipment.

Features

- ☐ Bandwidth and typical gain
  120 MHz at A_{VOL} = 300
  170 MHz at A_{VOL} = 90
  700 MHz at A_{VOL} = 8
- ☐ Very small phase delay
- ☐ Gain adjustable from 8 to 300
- ☐ Frequency compensation not required
- ☐ Pin compatible (μPC1664C) with type 733
- ☐ Pin compatible (μPC1663C) with type 592

Ordering Information

Part Number	Package	Operating Temperature Range
μPC1663C	8-Pin Plastic DIP	0 to +70°C
μPC1664C	14-Pin Plastic DIP	0 to +70°C

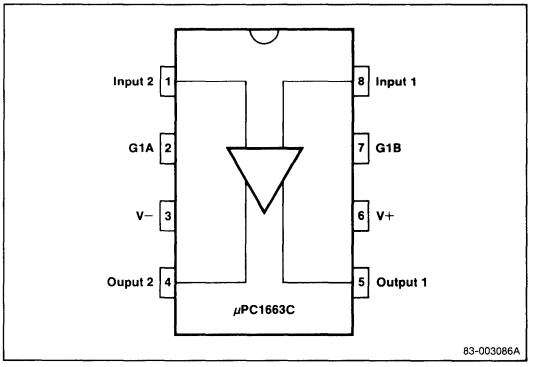
Absolute Maximum Ratings

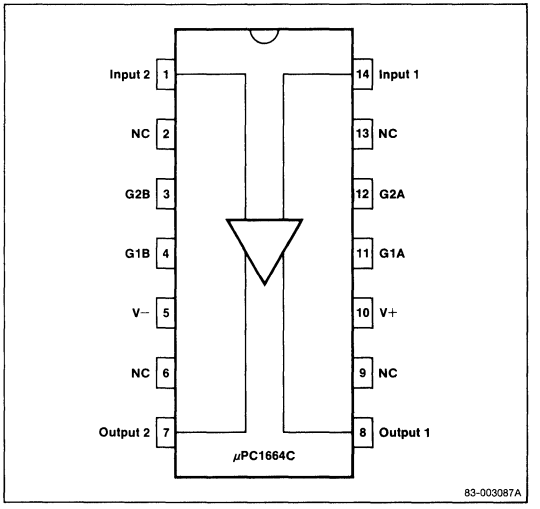
T_A = 25°C

Voltage Between V+ and V−	±8 V
Power Dissipation μPC1663C	500 mW
Power Dissipation μPC1664C	570 mW
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	35 mA
Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration





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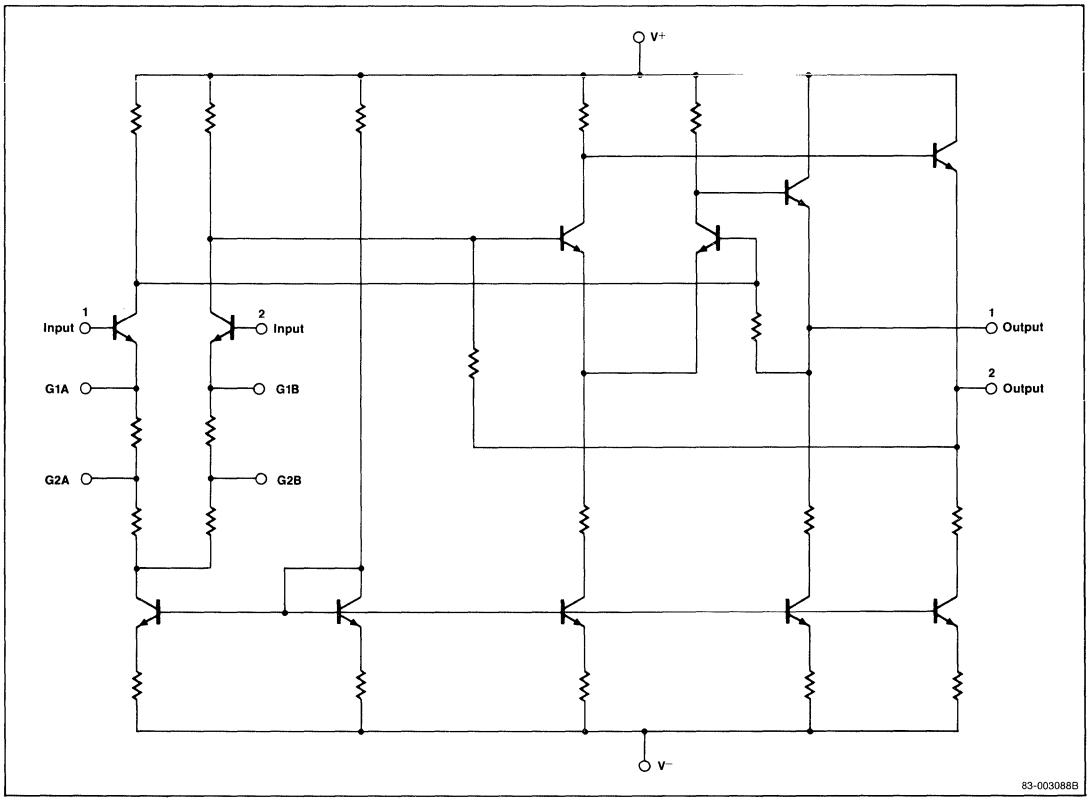
Equivalent Circuit



Electrical Characteristics

$T_A = 25°C$, $V\pm = \pm 6$ V

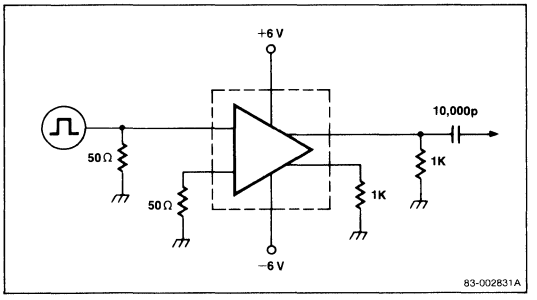
Parameter		Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Differential Voltage Gain	Gain 1	A_{VOL}		300			Note 1
	Gain 2			90			Note 2
	Gain 3			8			Note 3
Bandwidth	Gain 1	BW		120		MHz	$R_S = 50\ \Omega$; −3 dB point
	Gain 2			170			
	Gain 3			700			
Rise Time	Gain 1	t_r		2.9		ns	$R_S = 50\ \Omega$; V_{OUT} = 1 V_{p-p}
	Gain 2			2.7			
	Gain 3			2.9			
Propagation Delay	Gain 1	t_{pd}		2		ns	$R_S = 50\ \Omega$; V_{OUT} = 1 V_{p-p}
	Gain 2			1.6			
	Gain 3			1.2			
Input Offset Current		I_{io}		0.4	5.0	μA	
Input Bias Current		I_b		9.0	30	μA	
Input Voltage Range		V_{IN}		1.0		V	
Output Offset Voltage	Gain 1	$V_{O\ (OFF)}$		0.6	1.5	V	
	Gain 2			0.35	1.5	V	
Output Common Mode Voltage		$V_{O\ (CM)}$	2.4	2.9	3.4	V	
Output Voltage Swing		$V_{O\ (p-p)}$	3.0	4.0		V_{p-p}	
Output Sink Current		I_{SINK}	2.5	3.6		mA	
Supply Current		I_{CC}		15	24	mA	

Notes: 1. Gain select pins G1A and G1B are connected.
2. Gain select pins G2A and G2B are connected.
3. All gain select pins are open.
4. Insert adjustment resistor (0 to 10 kΩ) between G1A and G1B when variable gain is necessary.

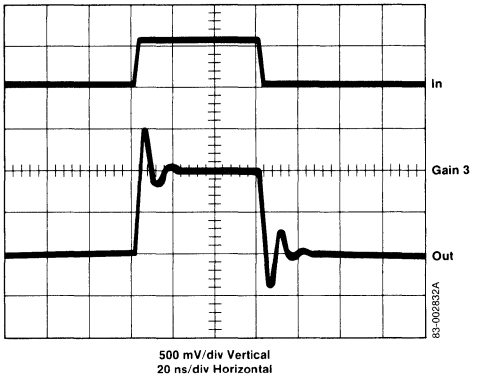
Attention: Due to ultrahigh-frequency characteristics, the physical circuit layout is very critical. Supply voltage line bypass, double-sided printed-circuit board, and wide-area ground line layout are necessary for stable operation. Two signal resistors connected to both inputs and two load resistors connected to both outputs should be balanced for stable operation.

Operating Characteristics

$T_A = 25°C$

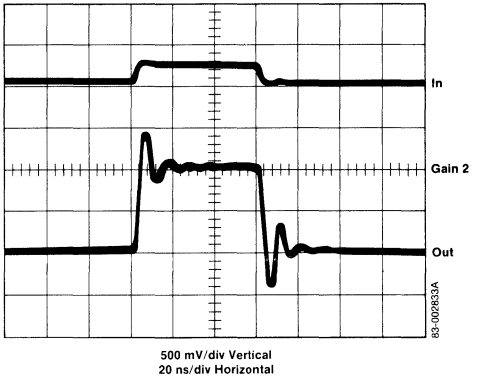


Pulse Response



500 mV/div Vertical
20 ns/div Horizontal

Pulse Response



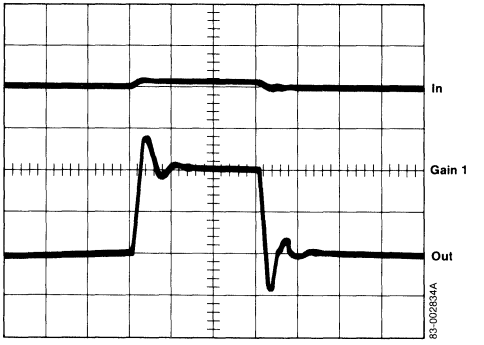
500 mV/div Vertical
20 ns/div Horizontal

7

Operating Characteristics (Cont.)

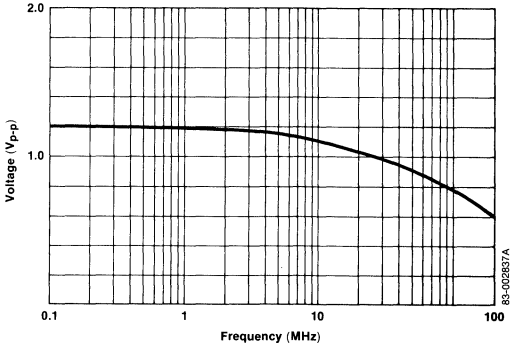
$T_A = 25°C$

Pulse Response

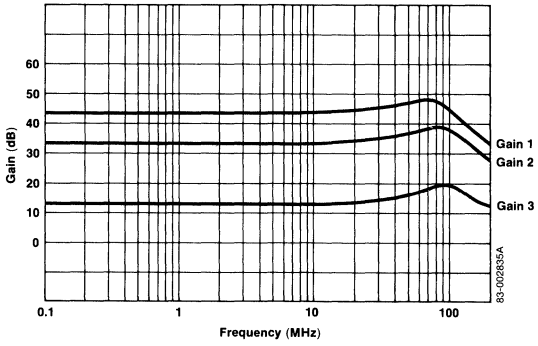


500 mV/div Vertical
20 ns/div Horizontal

Maximum Output Voltage Swing vs Frequency
[Single-Ended Video Line]

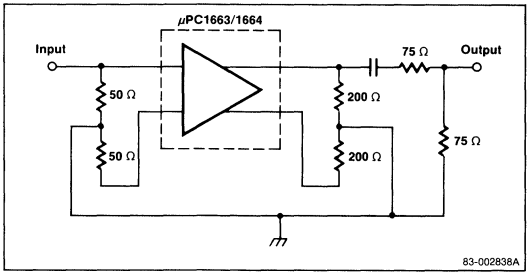


Single-Ended Gain vs Frequency

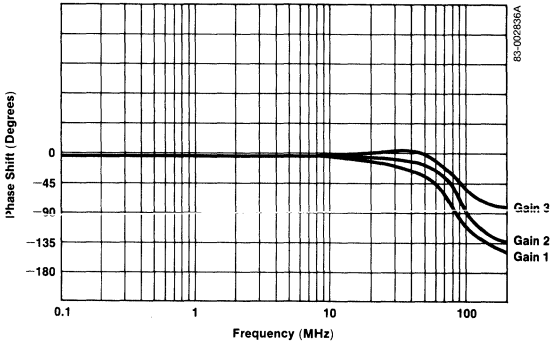


Measurement Circuit

V± = ±6 V



Phase Shift vs Frequency



NEC Electronics Inc.

μPC3423
OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

Description

The μPC3423 is an overvoltage protection circuit (OVP) that protects sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR.

Features

- ☐ Threshold voltage easily programmed by external resistors
- ☐ Programmable trip delay
- ☐ 300 mA output current
- ☐ Equivalent to MC3423

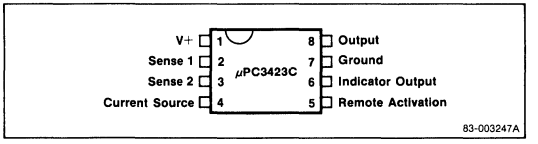
Ordering Information

Part Number	Package	Operating Temperature Range
μPC3423C	8-pin Plastic DIP	−20°C to +70°C

Recommended Operating Conditions

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply Voltage	V+	4.5		36	V
Output Current	I_O	0		300	mA
Indication Output Current	$I_{O(ind)}$	0		10	mA

Pin Configuration



Absolute Maximum Ratings

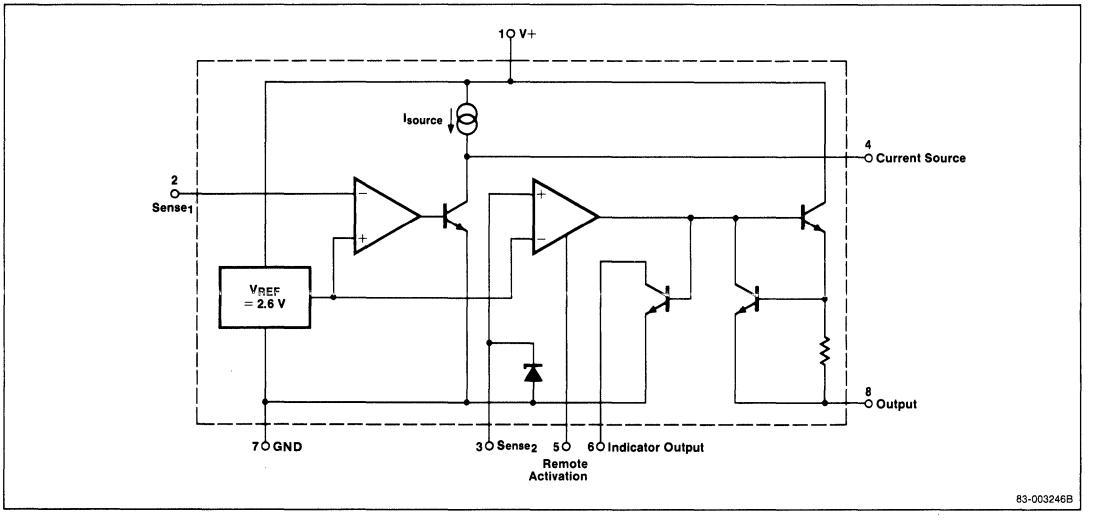
$T_A = 25°C$

Parameter	μPC3423	Unit
Supply Voltage	45	V
Sense Voltage	6.8	V
Remote Activation Input Voltage	7.0	V
Output Current	300	mA
Total Power Dissipation	600	mW
Operating Temperature Range	−20 to +70	°C
Storage Temperature Range	−40 to +125	°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Equivalent Circuit

1/4 Circuit



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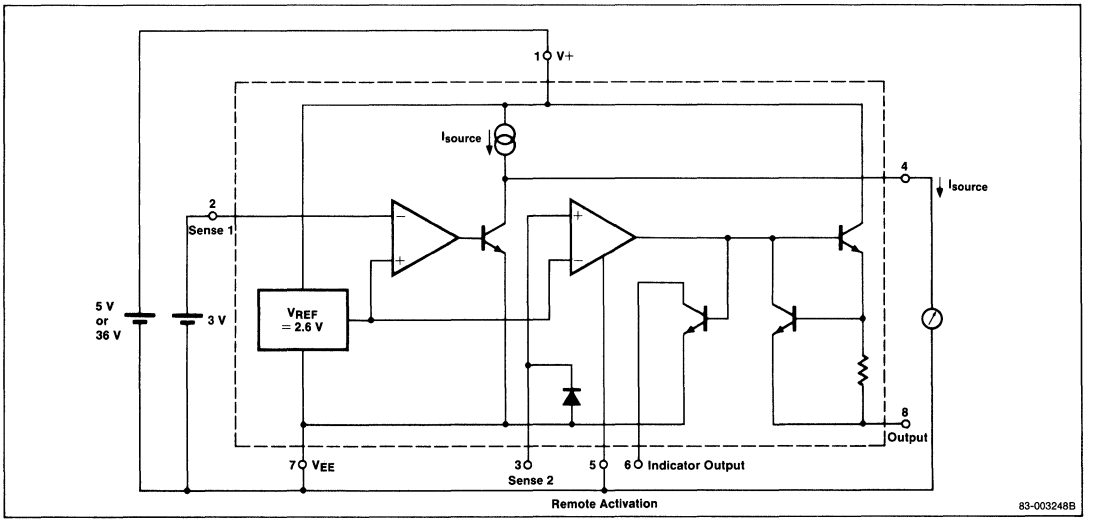
Electrical Characteristics

$V+ = 5.0\ V$, T_A +25°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output Voltage	V_O	V+ − 2.2	V+ − 1.8		V	$I_O = 100\ mA$
Indication Output Voltage	$V_{OL(Ind)}$		0.2	0.4		$I_{O(Ind)} = 8\ mA$
Sense Voltage (1), (2)	V_{sense1} V_{sense2}	2.4	2.6	2.8	V	
Sense Voltage Drift	$\Delta V_{sense}/\Delta T$		−0.04		%/°C	$-20°C \leq T_A \leq +70°C$
Remote Activation Input Current	I_{IH}		0.1	40	μA	$V_{IH} = 2.0\ V$
Remote Activation Input Current	I_{IL}		−250		μA	$V_{IL} = 0.8\ V$
Source Current	I_{source}		300		μA	See Test Circuit
Output Current Rise Time	t_r		400		mA/μs	$I_O = 100\ mA$
Propagation Delay	t_{pd}		0.5		μs	
Supply Current	I_{CC}		5.0	8.0	mA	pin 5 grounded, other terminals open

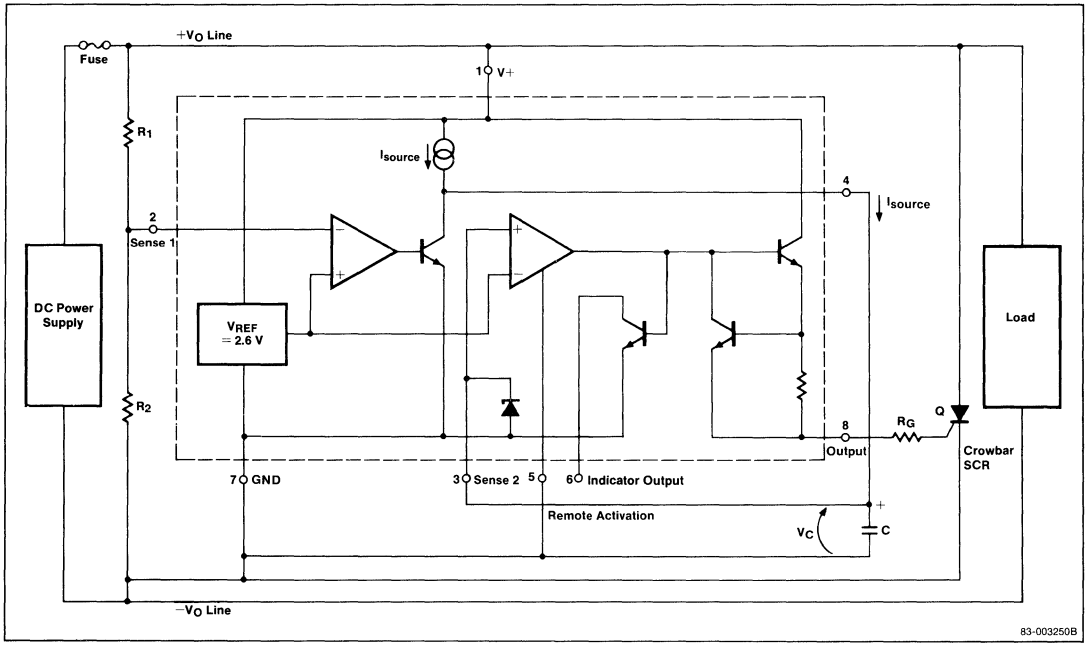
Test Circuit

I_{source} Test Circuit



Typical Applications

1. Basic Application



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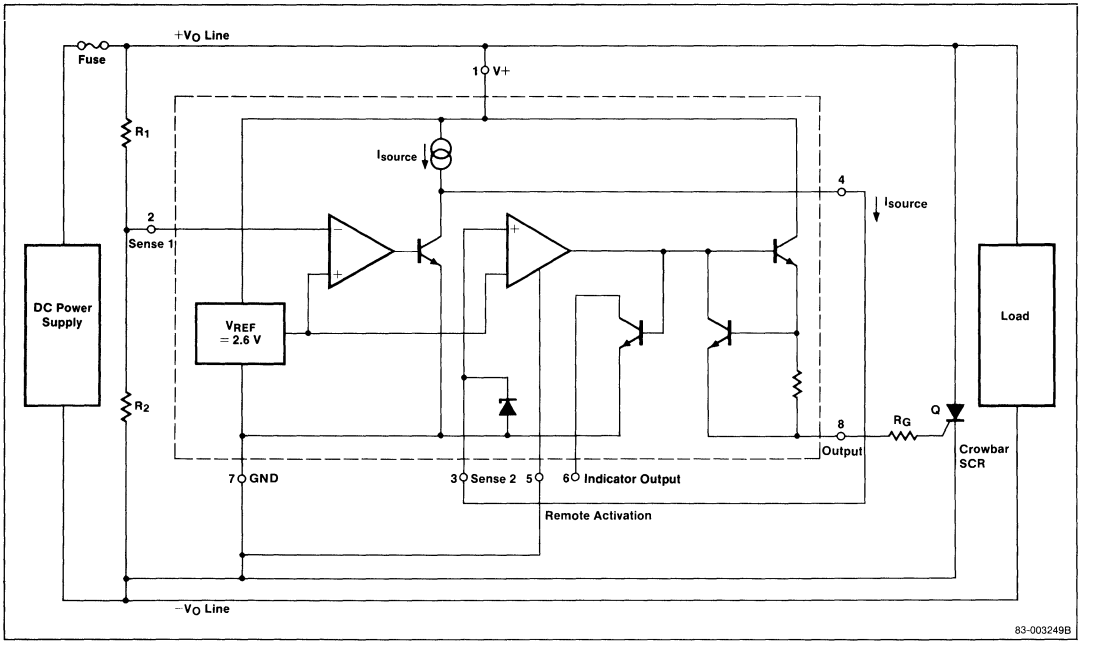
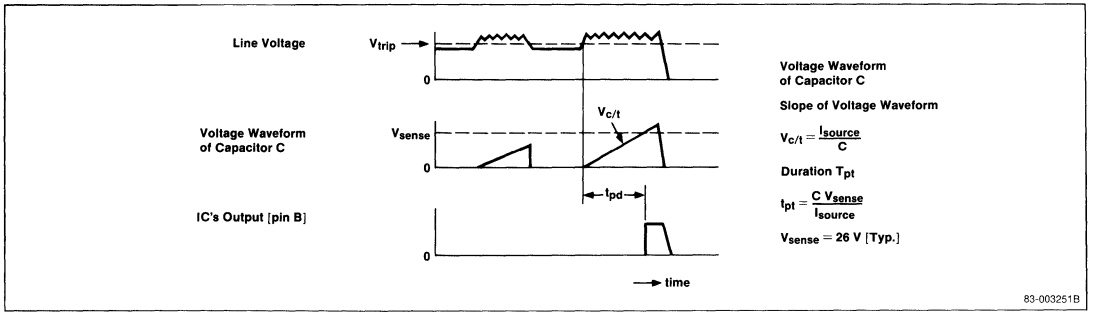
Typical Applications (Cont.)

2. Application when programmable duration of overvoltage condition before trip is needed



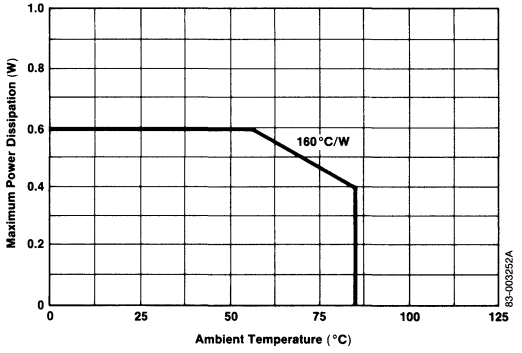
Timing Chart



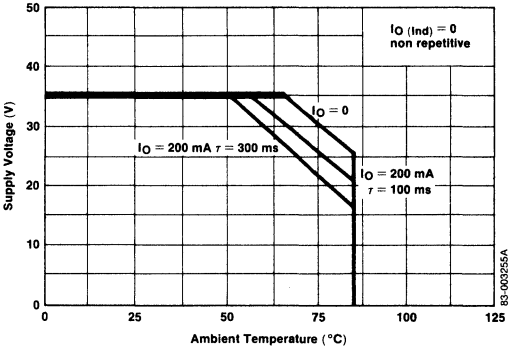
Operating Characteristics

$T_A = 25°C$

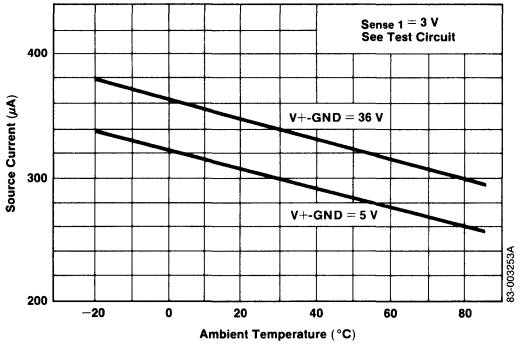
Maximum Power Dissipation



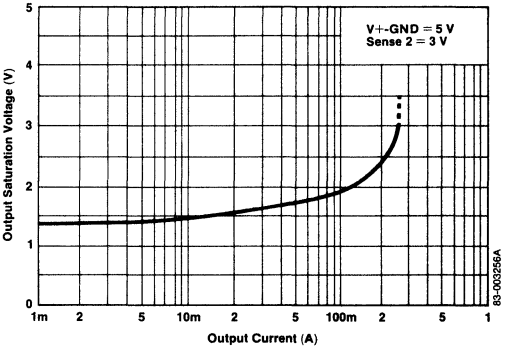
Supply Voltage vs. Ambient Temperature



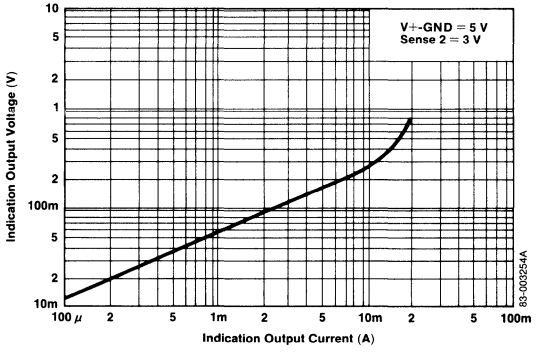
Source Current vs. Ambient Temperature



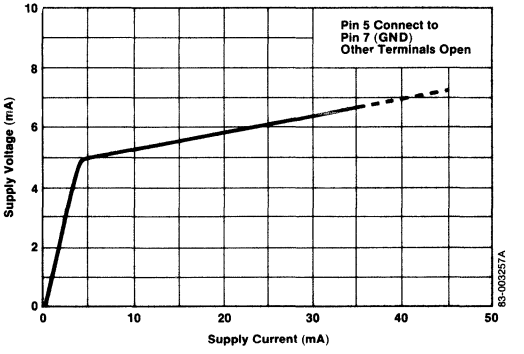
Output Saturation Voltage vs. Output Current



Indication Output Voltage vs. Output Current



Supply Current vs. Supply Voltage



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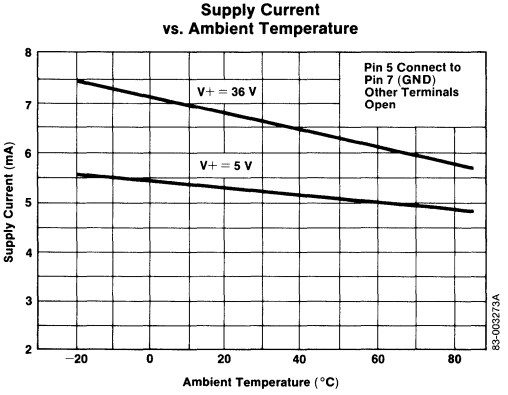
Operating Characteristics (Cont.)

$T_A = 25°C$



Description

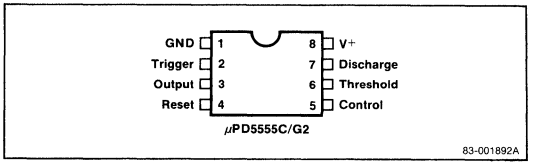
The μPD5555/56 are CMOS RC timers providing significantly improved performance over the standard bipolar 555/556 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, THRESHOLD, TRIGGER and RESET currents as low as 2 pA, no crowbarring of the power supply during output transitions, higher frequency performance, and no requirement to decouple control voltage for stable operation.

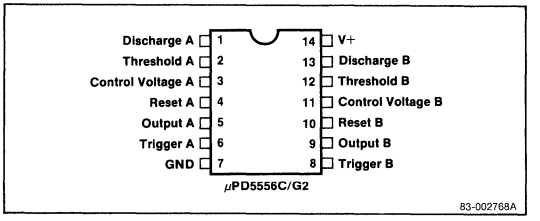
Specifically, the μPD5555/56 are stable controllers capable of producing accurate time delays or frequencies. The 5556 is a dual 5555, with the two timers operating independently of one another, sharing only V+ and GND. In the one-shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are controlled by two external resistors and one capacitor. The circuits can source or sink current large enough to drive TTL loads or provide minimal offsets to drive CMOS loads.

Features

- ☐ Exact equivalent in most cases for industry standard 555/556 timers
- ☐ Low supply current
- ☐ 3 to 16 V operating voltage range
- ☐ Timing from microseconds through hours

Pin Configurations

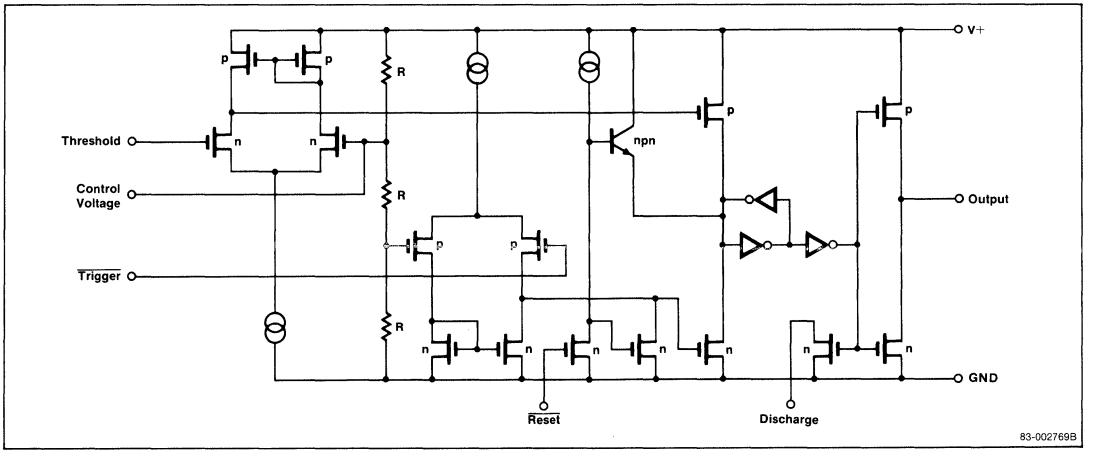




Ordering Information

Part Number	Package	Type
μPD5555C	Plastic DIP	Single
μPD5555G2	Plastic Miniflat	Single
μPD5556C	Plastic DIP	Dual
μPC5556G2	Plastic Miniflat	Dual

Equivalent Circuit



7

Applications

Figure 1. Monostable Operation

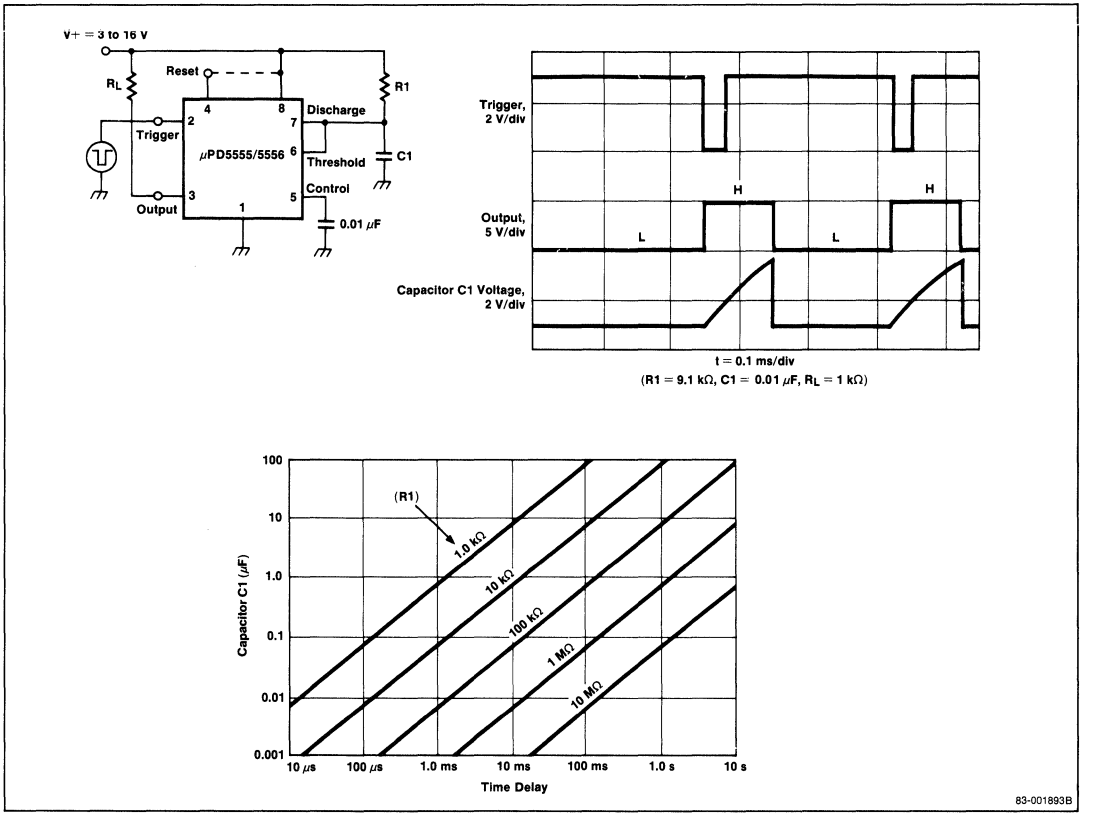


Figure 1 shows the μPD5555 operating as a monostable (one-shot) multivibrator. The sequence of operation is described below.

1. When the trigger input is reduced below 1/3 V+, the timer internal flip-flop is set.
2. This releases the short-circuit across C1 and the output goes high.
3. When the voltage across C1 reaches 2/3 V+, an internal comparator resets the flip-flop.
4. If the trigger voltage has returned above 1/3 V+, C1 discharges rapidly.
5. The output is now low and a new timing cycle may be initiated.

The time that the output is high can be taken from the graph in figure 1 or calculated by this formula:

$$t(\text{seconds}) = 1.1 \times R1\ (M\Omega) \times C1\ (\mu F)$$

If a low is applied to the reset input, the output is forced low and C1 is discharged regardless of the other inputs.

Applications (Cont.)

Figure 2. Astable Operation

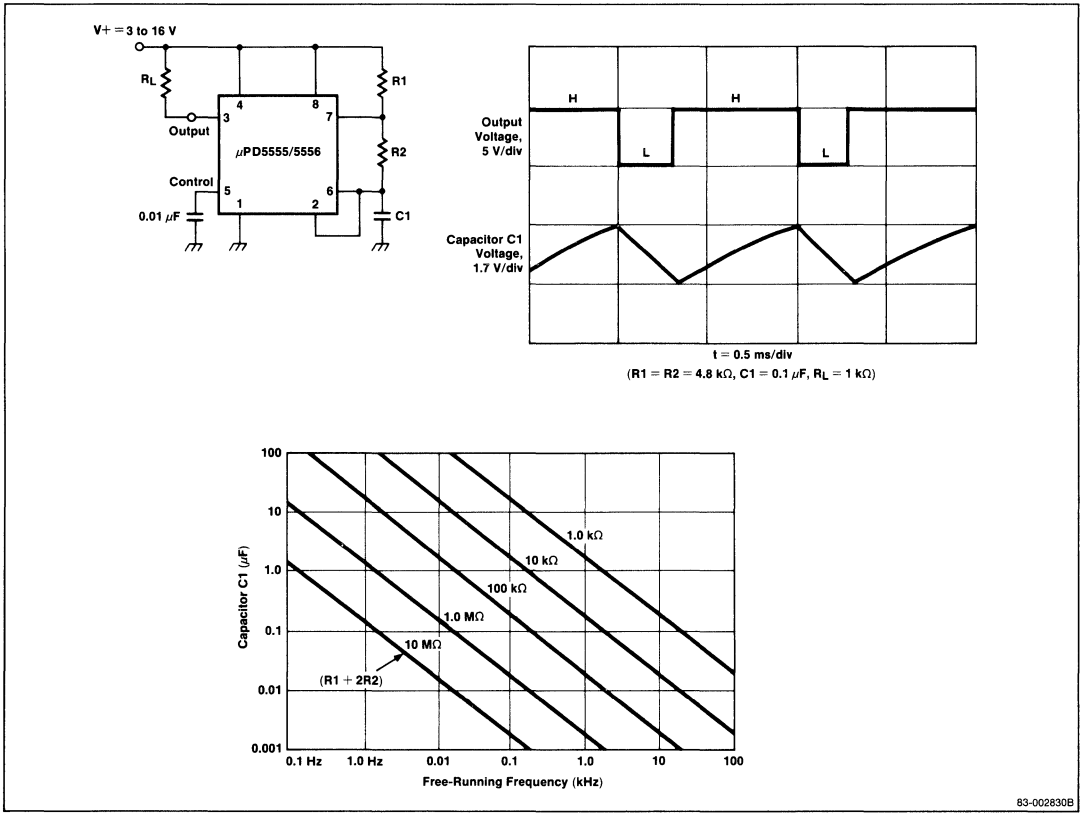


Figure 2 shows the μPD5555 operating as a free-running multivibrator. Capacitor C1 charges and discharges between 1/3 V+ and 2/3 V+. The free-running frequency can be obtained from the graph in figure 2 or calculated by the formula below.

Charge time (output high): $t_1 = 0.693\ (R1 + R2)\ C1$

Discharge time (output low): $t_2 = 0.693\ R2\ C1$

Period: $t = t_1 + t_2 = 0.693\ (R1 + 2R2)\ C1$

$$\text{Frequency} = \frac{1}{t} = \frac{1}{0.693\ (R1 + 2R2)\ C1}$$

$$\text{Duty cycle (output low): } D = \frac{t_2}{t} = \frac{R2}{R1 + 2R2}$$

In the formulas, the corresponding units in which time, frequency, resistance, and capacitance can be expressed are:

Time	Frequency	Resistance	Capacitance
s	Hz	MΩ	μF
ms	kHz	kΩ	μF
μs	MHz	Ω	μF

7

Electrical Characteristics

T_A = 25°C; V+ = 3 to 15 V unless otherwise specified.

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Current	I_{CC}		115	250	μA	V+ = 5 V
			140	350		V+ = 15 V
Threshold Voltage	V_{th}		2/3 V+		V	
Threshold Current	I_{th}		50		pA	V+ = 15 V
			10			V+ = 5 V
			1			V+ = 3 V
Trigger Voltage	V_{TRIG}		1/3 V+		V	
Trigger Current	I_{TRIG}		50		pA	V+ = 15 V
			10			V+ = 5 V
			1			V+ = 3 V
Reset Voltage (V_{OUT} becomes low.)	V_{RST}	0.4	1.1	2.0	V	V+ = 15 V
		0.4	1.1	2.0		V+ = 3 V
Reset Current	I_{RST}		100		pA	V_{reset} = V−, V+ = 15 V
			20			V+ = 5 V
			2			V+ = 3 V
Output Low Level	V_{OL}		0.06	0.4	V	V+ = 15 V, I_{sink} = 3.2 mA
			0.14	0.4		V+ = 5 V, I_{sink} = 3.2 mA
Output High Level	V_{OH}	14.25	14.85		V	V+ = 15 V, I_{source} = 1 mA
		4.0	4.7			V+ = 5 V, I_{source} = 1 mA
Output Rise Time	t_r		40		ns	V+ = 5 V, R_L = 10 MΩ, C_L = 7 pF
Output Fall Time	t_f		40		ns	V+ = 5 V, R_L = 10 MΩ, C_L = 7 pF
Max Osc Freq	f_{OSC}	500			kHz	Astable Operation
Propagation Delay (V+ = 5 V)	t_{pd}		350		ns	Monostable operation; trigger level = 0.1 V+
Min Trigger Pulse Width (V+ = 5 V)	t_{tr}		160		ns	Trigger level = 0.1 V+
Control Voltage			2/3 V+		V	
Timing Error initial Accuracy			2		%	R1, R2 = 1 to 10 kΩ, C1 = 0.1 μF, V+ = 5 to 15 V
Temperature Drift			50		ppm/°C	
Supply Voltage Drift			1		%/V	

Absolute Maximum Ratings

T_A = 25°C

Supply Voltage	18 V
Input Voltage	V+ ±0.3 V
Output Current	100 mA
Power Dissipation, μPD5555	
Plastic Miniflat	350 mW
Plastic DIP	440 mW
Power Dissipation, μPD5556	
Plastic Miniflat	550 mW
Plastic DIP	570 mW
Operating Temperature	−20 to +70°C
Storage Temperature	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

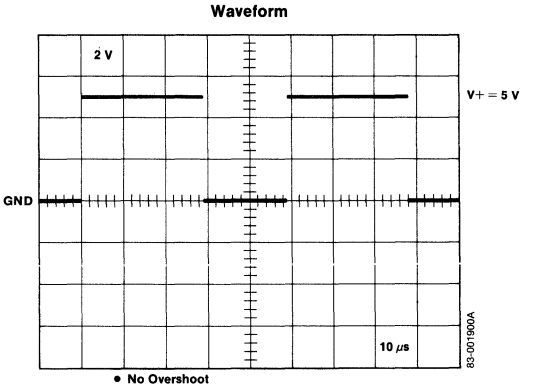
Recommended Operating Conditions

Paramater	Symbol	Min.	Typ.	Max.	Unit
Oscillation Frequency				500	kHz
Supply Voltage (Note 1)	V+	3		16	V
Input Voltage	V_{IN}	0			V
Output Sink Current	I_{SINK}			3.2	mA
Output Source Current	I_{SOURCE}			1	mA
Operating Temperature	T_{OPT}	−20		70	°C

Note: 1. To reduce transient switching noise on the supply voltage line, install a bypass capacitor from V+ to ground. Connect the capacitor, with value listed below, close to V+.

V+	C
< 10 V	0.047 μF
≥ 10 V	0.1 μF

Timing Waveform

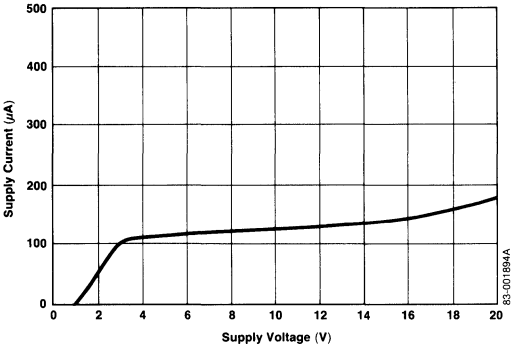


- No Overshoot
- V_{OH} can reach V+ without pull-up resistor

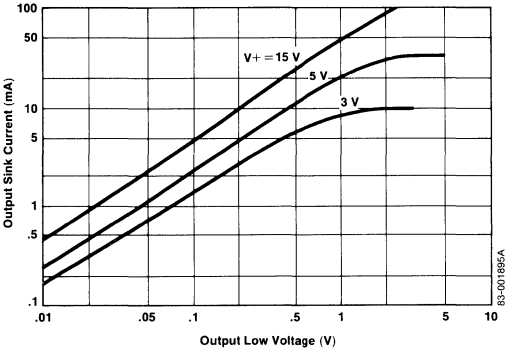
Operating Characteristics

$T_A = 25°C$

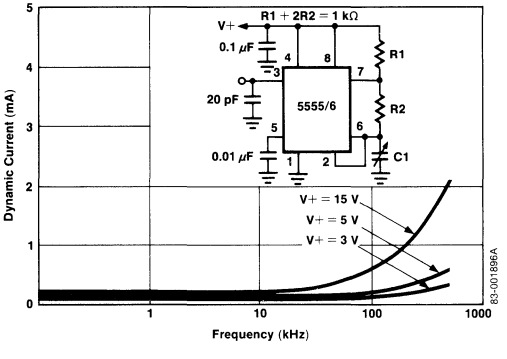
Supply Current (Static) vs. V+



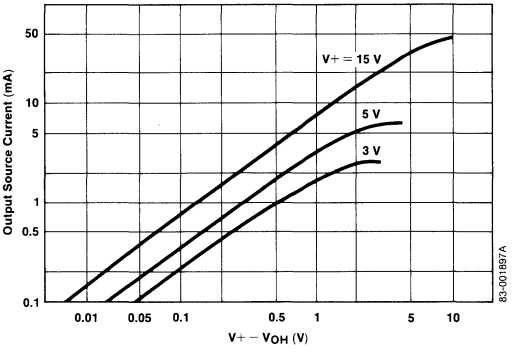
Output Sink Current vs V_{OL}



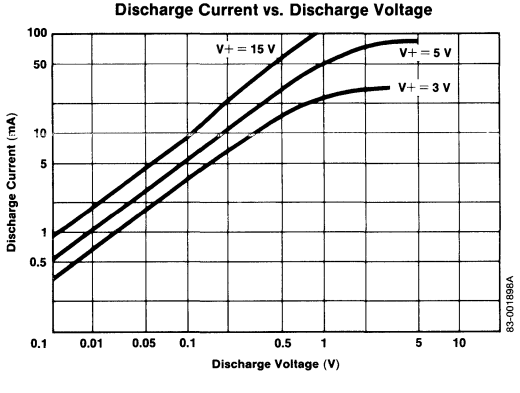
Dynamic Current vs Frequency



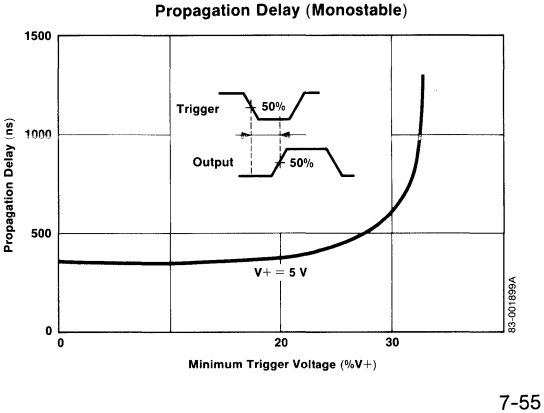
Output Source Current vs V_{OH}



Discharge Current vs. Discharge Voltage



Propagation Delay (Monostable)



7

NEC

CHARGE COUPLED DEVICES

8

Section 8 — Charge Coupled Devices

NEC

NEC Electronics Inc.

μPD791
4096-BIT CCD IMAGE SENSOR

PRELIMINARY INFORMATION

Description

The μPD791 is a CCD (charge-coupled device) linear image sensor that changes optical images to electrical signals. It has 4096 photo-elements, two lines of 2061-bit CCD charge transfer registers, two output amplifiers, and two compensation signal amplifiers.

The photo-elements have excellent response characteristics because of their PN junction construction. They are 7 by 5 μm separated by 2-μm channel stoppers.

The CCD charge transfer registers have very high transfer efficiency, above 99.996 percent.

Features

- ☐ Excellent photo-electrical characteristics
- ☐ Single 12-volt power supply
- ☐ Compensation amplifier signal can reduce output signal noise
- ☐ High resolution of 16 dots per mm across 25.6-cm page
- ☐ Transfer efficiency above 99.996 percent
- ☐ 24-pin ceramic DIP

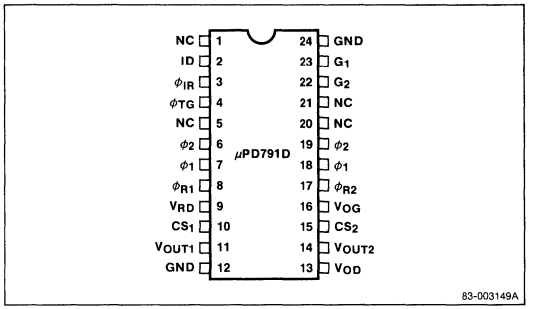
Applications

Facsimile
OCR (optical character reader)
Instrumentation

Ordering Information

Part Number	Package	Operating Ambient Temperature
μPD791D	24-pin ceramic DIP	−25 to +55 °C

Pin Configuration



Pin Identification

Pin	Name	*Function
1	NC	No connection
2	ID	Test input
3	ϕ_{IR}	Test input
4	ϕ_{TG}	Transfer gate clock input
5	NC	No connection
6, 7	ϕ_2, ϕ_1	Register clock input
8	ϕ_{R1}	Reset gate clock 1 input
9	V_{RD}	Reset part power supply input
10	CS_1	Compensation signal 1 output
11	V_{OUT1}	Output 1 (bit 1, 3, 5,...)
12	GND	Ground
13	V_{OD}	Output amplifier power supply input
14	V_{OUT2}	Output 2 (bit 2, 4, 6...)
15	CS_2	Compensation signal 2 output
16	V_{OG}	Output gate bias input
17	ϕ_{R2}	Reset gate clock 2 input
18, 19	ϕ_1, ϕ_2	Register clock input
20, 21	NC	No connection
22	G_2	Test input
23	G_1	Test input
24	GND	Ground

*All NC pins should be connected to ground.

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Block Diagram

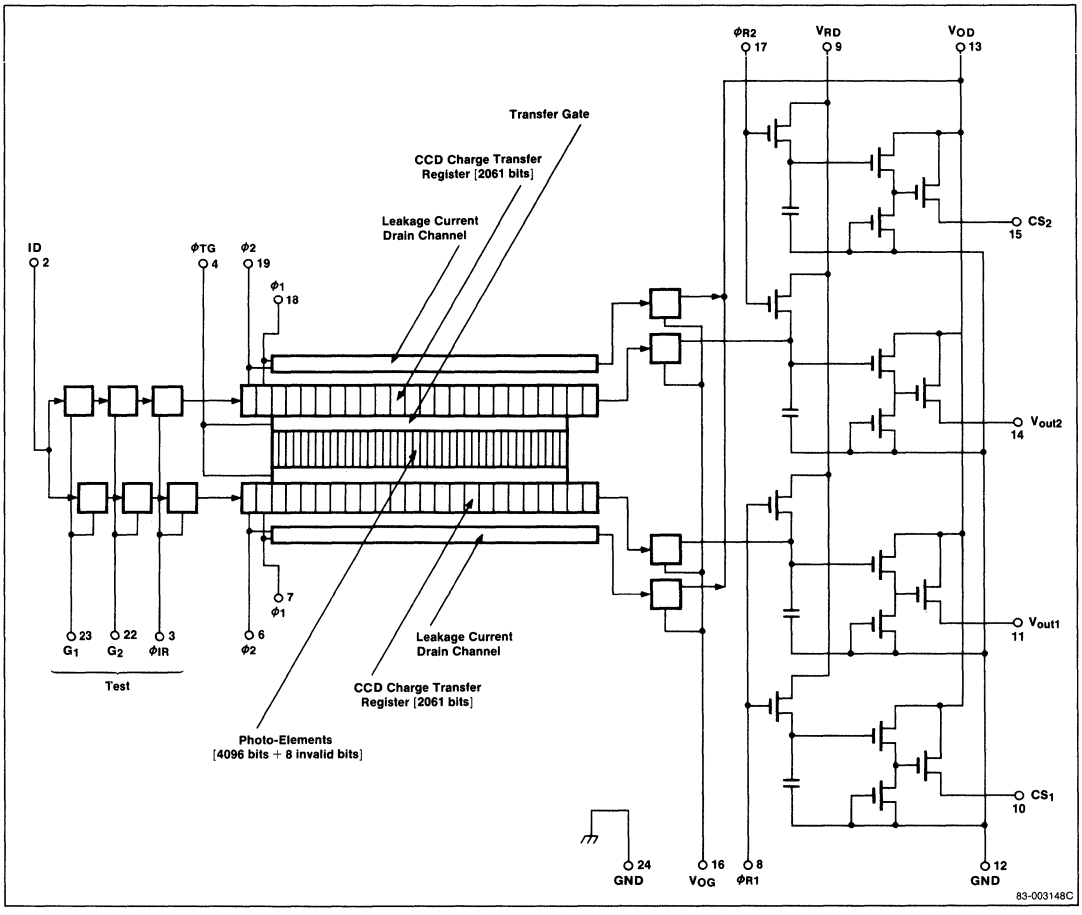
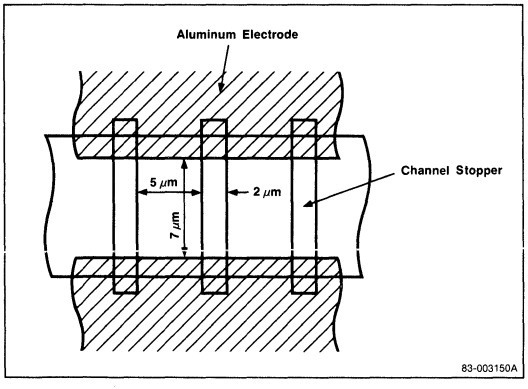


Photo-Element Construction



Electrical Characteristics

$T_A = +25°C$; source of light, 2856 K tungsten lamp; exposure period = 5.0 ms; $f_{\phi 1}$, $f_{\phi 2}$, and $f_{\phi R}$ = 1 MHz; external load resistance = 2 kΩ; V_{OD} and V_{RD} = 12.0 V; V_{OG} = 3.2 V; V_{G1} and V_{G2} = 0 V.

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Saturation Output Voltage	V_{SAT}	300	400		mV	
Saturation Exposure	SE		0.22		lx•s	
Photo-Response Nonuniformity	PRNU		±5	±10	%	V_{OUT} = 200 mV; infrared cut filter, Corning 1-75
Average Dark Signal	ADS		2	10	mV	No exposure
Dark Signal Nonuniformity	DSNU		10	20	mV	No exposure
Working Power Consumption	P_D	70	150	230	mW	Current of pins 9 and 13 x supply voltage
Spectral Response Range Limits	SR	0.3		1.1	μm	
Sensitivity	S	1300	1900	3000	mV/lx•s	
Offset Voltage	V_{IO}	4	6	8	V	0% level of V_{OUT} in timing waveforms
Output Delay Time	t_D		50	120	ns	See timing waveforms.
Difference between V_{OUT1} and V_{OUT2}	dV_{OUT}			±10	%	V_{OUT1} = 200 mV

Reference Characteristics

Parameter	Limits Min	Typ	Max	Unit
Input Capacitance at ϕ_1 or ϕ_2 (pins 6, 7, 18, 19)	400	800	1200	pF
Input Capacitance at ϕ_R (pins 8, 17)	5	10	15	pF
Input Capacitance at ϕ_{TG} (pin 4)	50	100	150	pF
Output Impedance at V_{OUT} or CS (pins 10, 11, 14, 15) with 2-kΩ external load resistor		1.0	2.0	kΩ

Absolute Maximum Ratings

$T_A = +25°C$

Output Amplifier Supply Voltage, V_{OD}	−0.3 to +18 V
Reset Part Supply Voltage, V_{RD}	−0.3 to +18 V
Output Gate Voltage, V_{OG}	−0.3 to +18 V
Register Clock Signal Voltage, $V_{\phi 1 \phi 2}$	−0.3 to +18 V
Transfer Gate Clock Signal Voltage, $V_{\phi TG}$	−0.3 to +18 V
Reset Gate Clock Signal Voltage, $V_{\phi R}$	−0.3 to +18 V
Operating Temperature, T_{OPT}	−25 to +55°C
Storage Temperature, T_{STG}	−40 to +100°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

$T_A = -25$ to $+55°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit
Output Amplifier Supply Voltage	V_{OD}	11.4	12.0	12.6	V
Reset Part Supply Voltage	V_{RD}	11.4	12.0	12.6	V
Output Gate Bias Voltage	V_{OG}	2.7	3.2	3.7	V
Test Terminal G_1 Voltage	V_{G1}		0		V
Test Terminal G_2 Voltage	V_{G2}		0		V
Test Terminal ID Voltage	V_{ID}	10	12.0	15	V
Test Terminal ϕ_{IR} Voltage	$V_{\phi IR}$		0		V
High Level of Register Clock Signal	$V_{\phi 1 \phi 2H}$	9.0	12.0	12.5	V
Low Level of Register Clock Signal	$V_{\phi 1 \phi 2L}$	−0.3	0	0.5	V
High Level of Transfer Gate Clock Signal	$V_{\phi TGH}$	9.0	12.0	12.5	V
Low Level of Transfer Gate Clock Signal	$V_{\phi TGL}$	−0.3	0	0.5	V
High Level of Reset Gate Clock Signal	$V_{\phi RH}$	9.0	12.0	12.5	V
Low Level of Reset Gate Clock Signal	$V_{\phi RL}$	−0.3	0	0.5	V
Register Clock Signal Frequency (see Note)	$f_{\phi 1 \phi 2}$		1	3.5	MHz
Reset Gate Clock Signal Frequency (see Note)	$f_{\phi R}$		1	3.5	MHz

Note: At lower frequencies, t_P of output signal is >100 ns. (See Timing Waveforms.)

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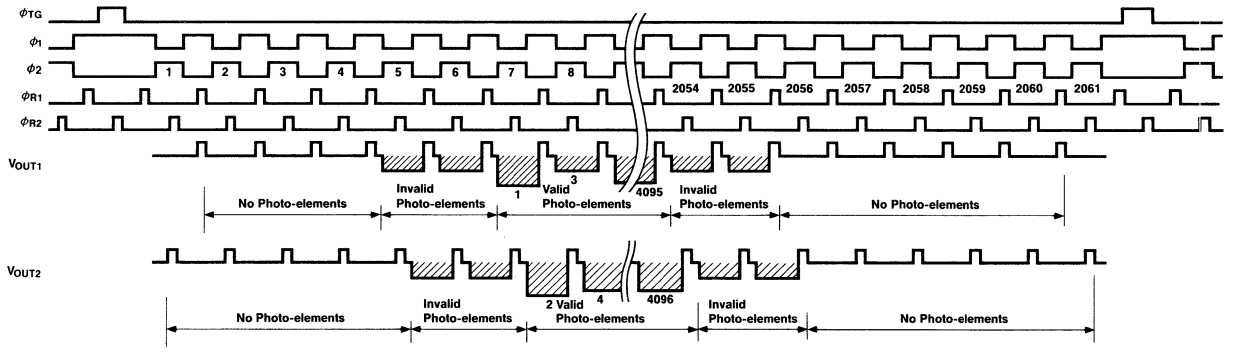
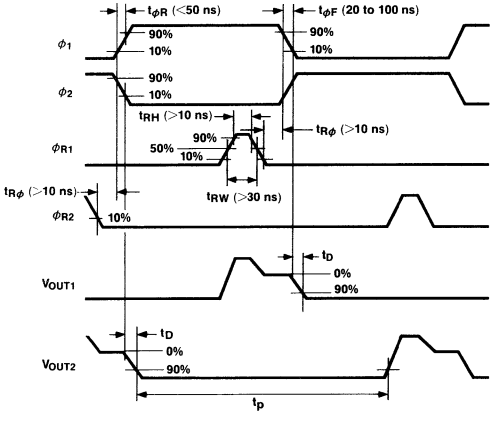
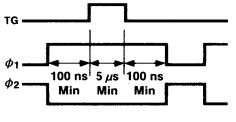
Timing Waveforms







- ϕ_1 and ϕ_2 are symmetrical.
- The crossing voltage of ϕ_1 and ϕ_2 should be kept above $V_{OG} + 1$ V.
- The register clock pulse should be not more than 2061 cycles.
- Width of the transfer gate pulse should be less than 20 μs.

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NEC

Definitions of Electrical Parameters

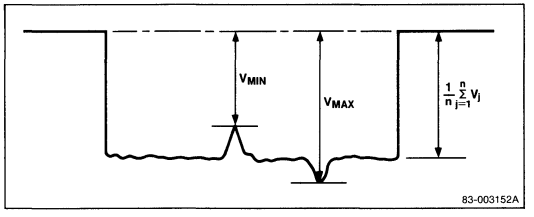
Saturation Output Voltage [V_{SAT}]. An output signal level above which the PRNU (photo-response nonuniformity) is ≥10% or the response is nonlinear.

Saturation Exposure [SE]. Product of illuminance (lx) and exposure period (s) in which the output is saturated.

Photo-Response Nonuniformity [PRNU]. Percentage of peak output level and bottom output level against average output level of all valid photo-elements in static and uniform light.

$$PRNU\ (\%) = \left(\frac{V_{MAX} \text{ or } V_{MIN}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1\right) \times 100$$

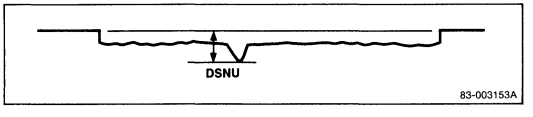
where
n = number of valid photo-elements
V_j = output voltage of each photo element



Average Dark Signal [ADS]. Average output level of valid photo-elements with no exposure.

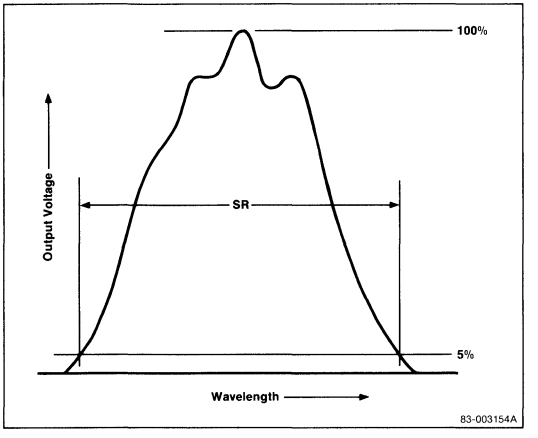
$$ADS\ (mV) = \frac{1}{n}\sum_{j=1}^{n} V_j$$

Dark Signal Nonuniformity [DSNU]. Peak output level with no exposure.



Working Power Consumption [P_W]. Product of supply voltage and current when supply voltage is 12.0 V.

Spectral Response Range Limits [SR]. Short side and long side limits of response spectral range having sensitivity above 5 percent of sensitivity of most sensitive wavelength.



Sensitivity [S]. Quotient of the output level divided by exposure (lx•s).

Offset Voltage [V_{OS}]. Output terminal potential with no exposure.

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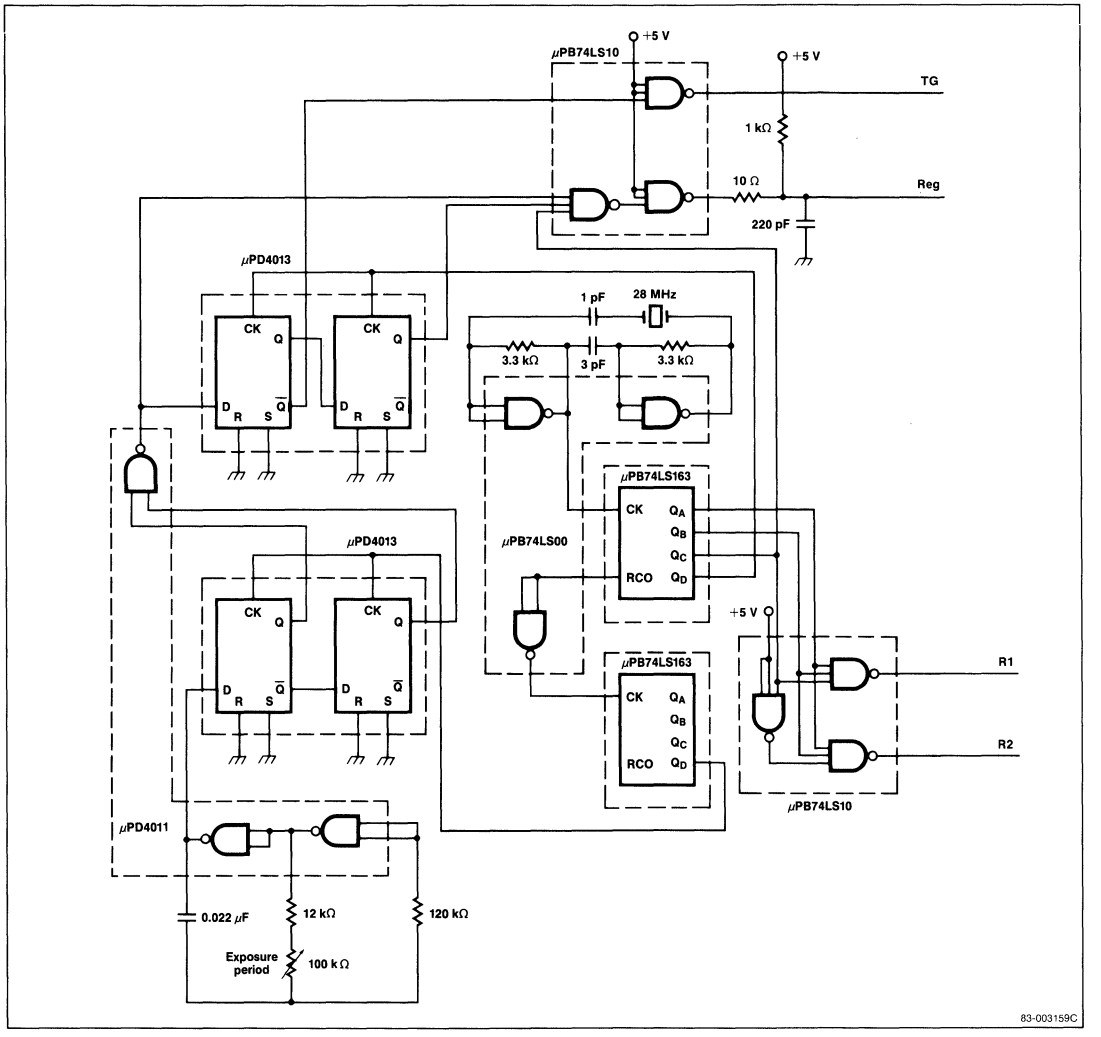
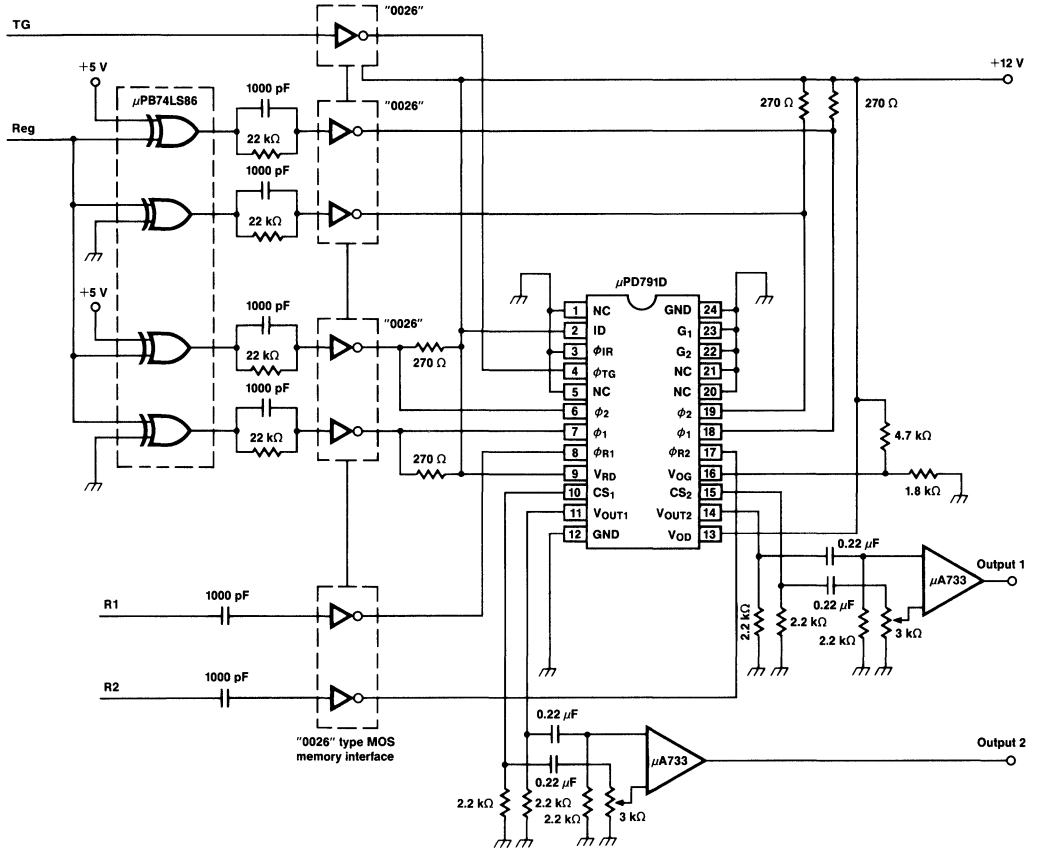
Example of Driving Circuit

(Sheet 1 of 2)



Example of Driving Circuit (Cont.)

(Sheet 2 of 2)



Note:

1. Supply voltage for clock generating is +5 V.
2. If ringing is present on the ϕ_R waveforms, try connecting a resistor and capacitor in series between pin 8 (ϕ_{R1}) and grounnd and between pin 17 (ϕ_{R2}) and ground as damping circuits. Approximate values are 68 Ω and 330 pF.

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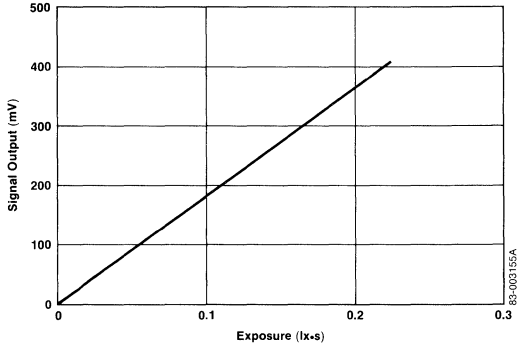
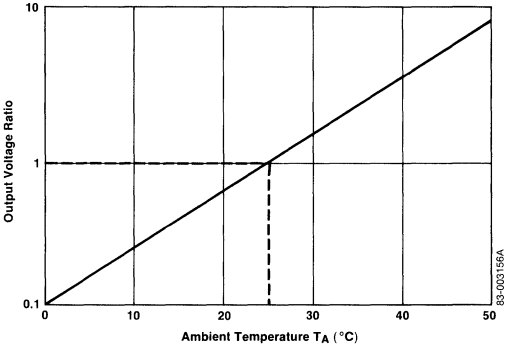
Operating Characteristics

$T_A = 25°C$

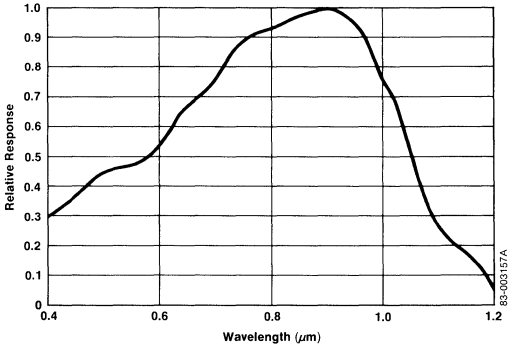
Signal Output



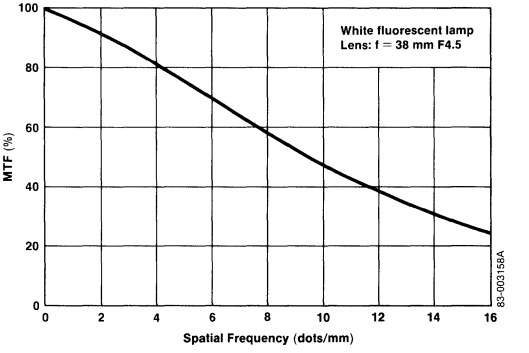
Dark Signal



Relative Spectrum Response



MTF



NEC
NEC Electronics Inc.

μPD795
1024-BIT CCD IMAGE SENSOR

PRELIMINARY INFORMATION

Description

The μPD795 is a CCD (charge-coupled device) linear image sensor that changes optical images to electrical signals. It has 1024 photo-elements, two lines of 525-bit CCD charge transfer registers, a drive unit, a sample-and-hold circuit, and an output amplifier. The drive unit simplifies the external circuit and reduces total drive power. The sample-and-hold circuit substantially reduces output signal noise.

The photo-elements have excellent response characteristics because of their PN junction construction. They are 14 by 9 μm separated by 5-μm channel stoppers.

The CCD charge transfer registers have very high transfer efficiency, above 99.996 percent.

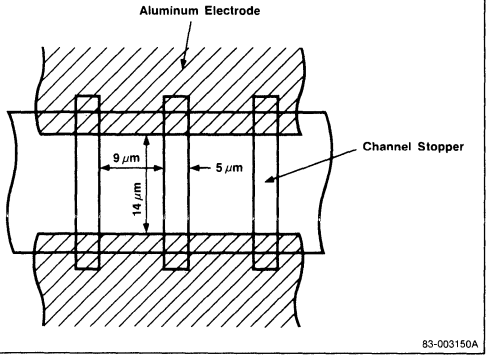
Features

- ☐ Excellent photo-electrical characteristics
- ☐ Single 12-volt power supply
- ☐ On-chip drive unit and sample-and-hold circuit
- ☐ High resolution of 8 dots per mm across 12.8-cm page
- ☐ Transfer efficiency above 99.996 percent
- ☐ 20-pin ceramic DIP

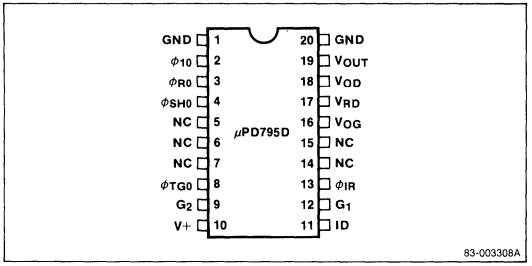
Applications

Facsimile
OCR (optical character reader)
Instrumentation

Photo-Element Construction



Pin Configuration



Pin Identification

Pin	Name	*Function
1	GND	Ground
2	ϕ_{10}	Register clock input
3	ϕ_{R0}	Reset gate clock input
4	ϕ_{SH0}	Sample-and-hold clock input
5, 6, 7	NC	No connection
8	ϕ_{TG0}	Transfer gate clock input
9	G_2	Test input
10	V+	Drive unit power supply input
11	ID	Test input
12	G_1	Test input
13	ϕ_{IR}	Test input
14, 15	NC	No connection
16	V_{OG}	Output gate bias input
17	V_{RD}	Reset part power supply input
18	V_{OD}	Output amplifier power supply input
19	V_{OUT}	Output
20	GND	Ground

*All NC pins should be connected to ground.

Ordering Information

Part Number	Package	Operating Ambient Temperature
μPD795D	20-pin ceramic DIP	−25 to +55°C

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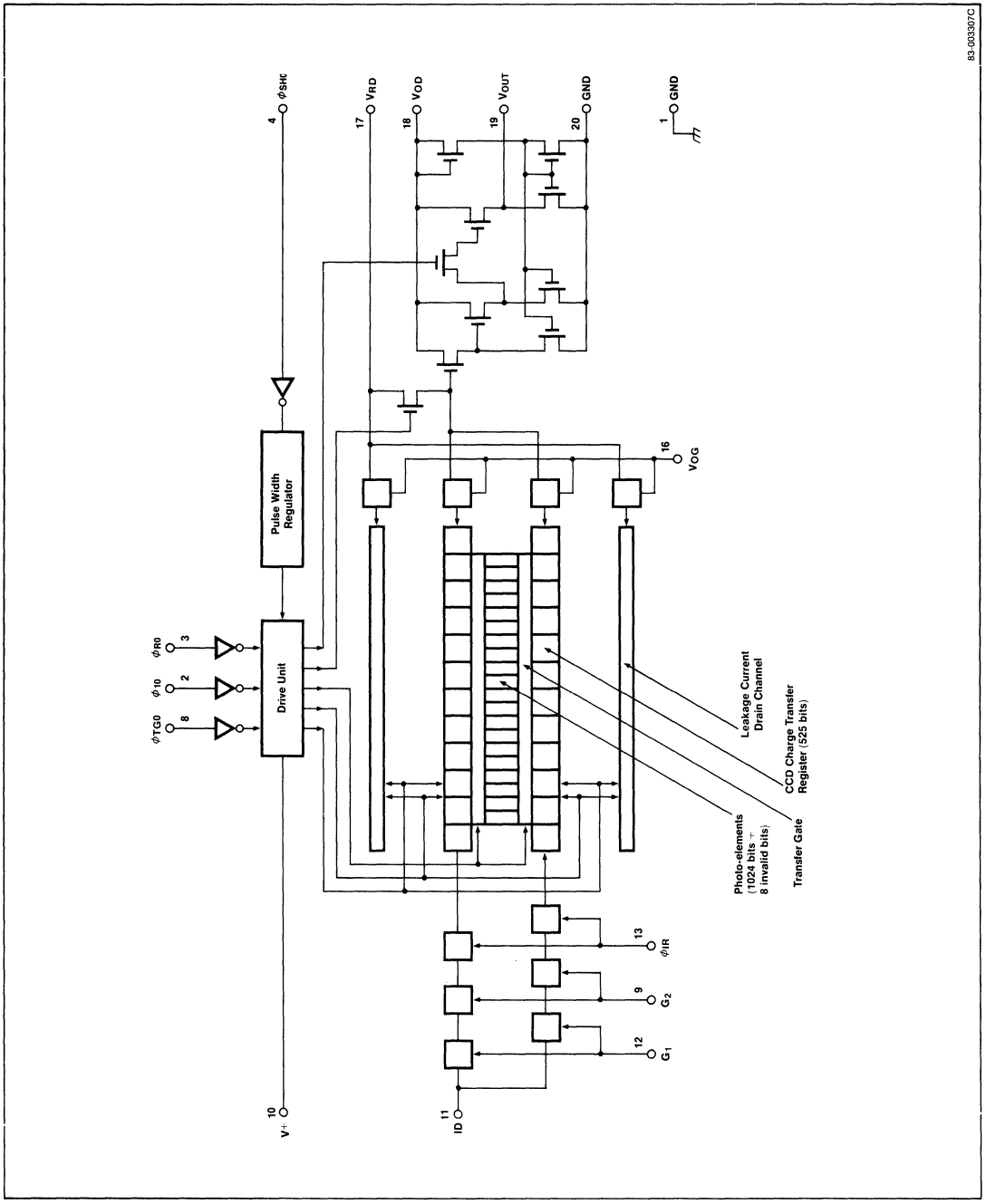
Block Diagram



Electrical Characteristics

T_A = +25°C; source of light, 2856 K tungsten lamp; exposure period = 5.0 ms; V_{GG}, V_{OD}, and V_{RD} = 12.0 V; $f_{\phi 10}$ = 250 kHz; $f_{\phi RO}$ = 500 kHz.

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Saturation Output Voltage	V_{SAT}	400	650		mV	
Saturation Exposure	SE	0.15	0.20		lx•s	
Photo-Response Nonuniformity	PRNU		±5	±10	%	V_{OUT} = 200 mV; infrared cut filter, Corning 1-75
Average Dark Signal	ADS		3	10	mV	No exposure
Dark Signal Nonuniformity	DSNU		5	15	mV	No exposure
Working Power Consumption	P_D		200		mW	Current of pins 10, 17, and 18 x supply voltage
Spectral Response Range Limits	SR	0.3		1.1	μm	
Sensitivity	S	2000	3250	4500	mV/lx•s	
Offset Voltage	V_{IO}		4.0		V	0% level of V_{OUT} in timing waveforms
Feed-Through Delay Time	t_D		50	100	ns	See timing waveforms.
Feed-Through Level	V_{FT}		70	120	mV	
Feed-Through Pulse Width	t_{PW}		70	120	ns	

Reference Characteristics

Parameter	Limits Min	Typ	Max	Unit
Input Capacitance at ϕ_{10}, ϕ_{RO}, ϕ_{SHO}, or ϕ_{TGO} (pins 2, 3, 4, 8)		5	10	pF
Rise Time and Fall Time of Feed-Through Pulse		50	100	ns
Output Impedance at V_{OUT} (pin 19)	0.5	1.0	2.0	kΩ

Absolute Maximum Ratings

T_A = +25°C

Output Amplifier Supply Voltage, V_{OD}	−0.3 to +15 V
Reset Part Supply Voltage, V_{RD}	−0.3 to +15 V
Drive Unit Supply Voltage, V+	−0.3 to +15 V
Output Gate Voltage, V_{OG}	−0.3 to +15 V
Register Clock Signal Voltage, $V_{\phi 10}$	−0.3 to +15 V
Transfer Gate Clock Signal Voltage, $V_{\phi TGO}$	−0.3 to +15 V
Reset Gate Clock Signal Voltage, $V_{\phi RO}$	−0.3 to +15 V
Sample-and-Hold Clock Signal Voltage, $V_{\phi SHO}$	−0.3 to +15 V
Operating Temperature, T_{OPT}	−25 to +55°C
Storage Temperature, T_{STG}	−40 to +100°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

T_A = −25 to +55°C

Parameter	Symbol	Limits Min	Typ	Max	Unit
Output Amplifier Supply Voltage	V_{OD}	11.4	12.0	12.6	V
Reset Part Supply Voltage	V_{RD}	11.4	12.0	12.6	V
Drive Unit Supply Voltage	V+	11.4	12.0	12.6	V
Output Gate Bias Voltage	V_{OG}	1.0	1.25	1.50	V
Test Terminal G_1 Voltage	V_{G1}		0		V
Test Terminal G_2 Voltage	V_{G2}		0		V
Test Terminal ID Voltage	V_{ID}		12.0		V
Test Terminal ϕ_{IR} Voltage	$V_{\phi IR}$		0		V
High Level of Register Clock Signal	$V_{\phi 1H}$	2.4	4.5	5.5	V
Low Level of Register Clock Signal	$V_{\phi 1L}$	−0.3	0	0.5	V
High Level of Transfer Gate Clock Signal	$V_{\phi TGH}$	2.4	4.5	5.5	V
Low Level of Transfer Gate Clock Signal	$V_{\phi TGL}$	−0.3	0	0.5	V
High Level of Reset Gate Clock Signal	$V_{\phi RH}$	2.4	4.5	5.5	V
Low Level of Reset Gate Clock Signal	$V_{\phi RL}$	−0.3	0	0.5	V
High Level of Sample-and-Hold Clock Signal	$V_{\phi SHH}$	2.4	4.5	5.5	V
Low Level of Sample-and-Hold Clock Signal	$V_{\phi SHL}$	−0.3	0	0.5	V
Register Clock Signal Frequency	$f_{\phi 10}$		250	500	kHz
Reset Gate Clock Signal Frequency	$f_{\phi RO}$		500	1000	kHz

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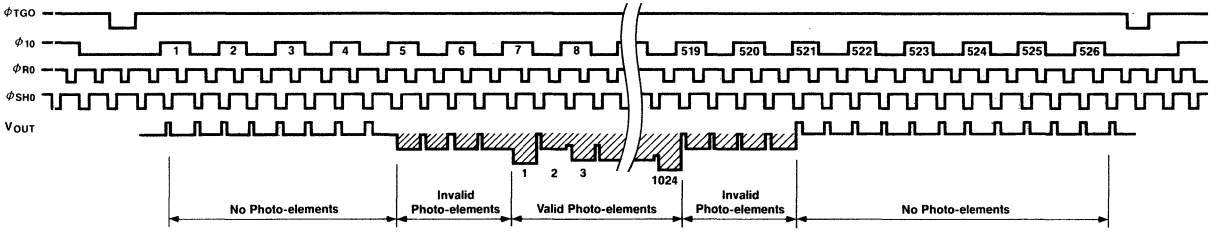
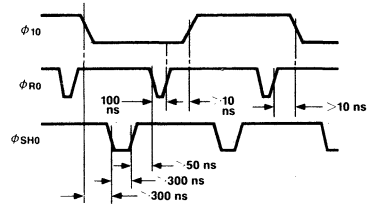
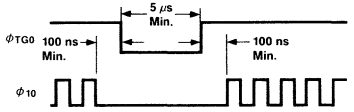
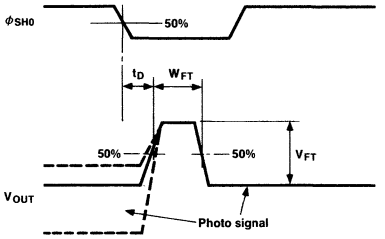
Timing Waveforms









- The register clock signal ϕ_{10} should be not more than 526 cycles.
- Width of thea transfer gate pulse ϕ_{TGO} should be less than 20 μs.

83-003310C

Definitions of Electrical Parameters

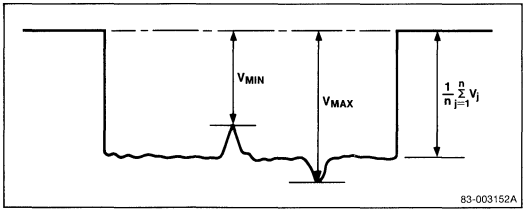
Saturation Output Voltage [V_{SAT}]. An output signal level above which the PRNU (photo-response nonuniformity) is ≥10% or the response is nonlinear.

Saturation Exposure [SE]. Product of illuminance (lx) and exposure period (s) in which the output is saturated.

Photo-Response Nonuniformity [PRNU]. Percentage of peak output level and bottom output level against average output level of all valid photo-elements in static and uniform light.

$$PRNU\ (\%) = \left(\frac{V_{MAX} \text{ or } V_{MIN}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1\right) \times 100$$

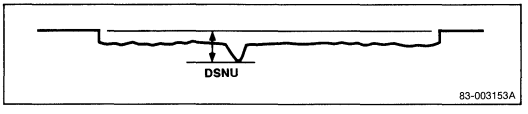
where
n = number of valid photo-elements
V_j = output voltage of each photo element



Average Dark Signal [ADS]. Average output level of valid photo-elements with no exposure.

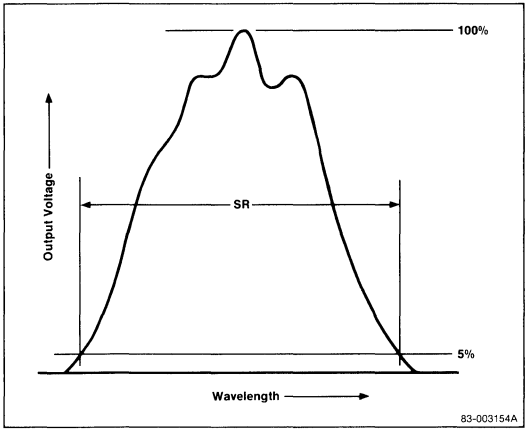
$$ADS\ (mV) = \frac{1}{n}\sum_{j=1}^{n} V_j$$

Dark Signal Nonuniformity [DSNU]. Peak output level with no exposure.



Working Power Consumption [P_W]. Product of supply voltage and current when supply voltage is 12.0 V.

Spectral Response Range Limits [SR]. Short side and long side limits of response spectral range having sensitivity above 5 percent of sensitivity of most sensitive wavelength.

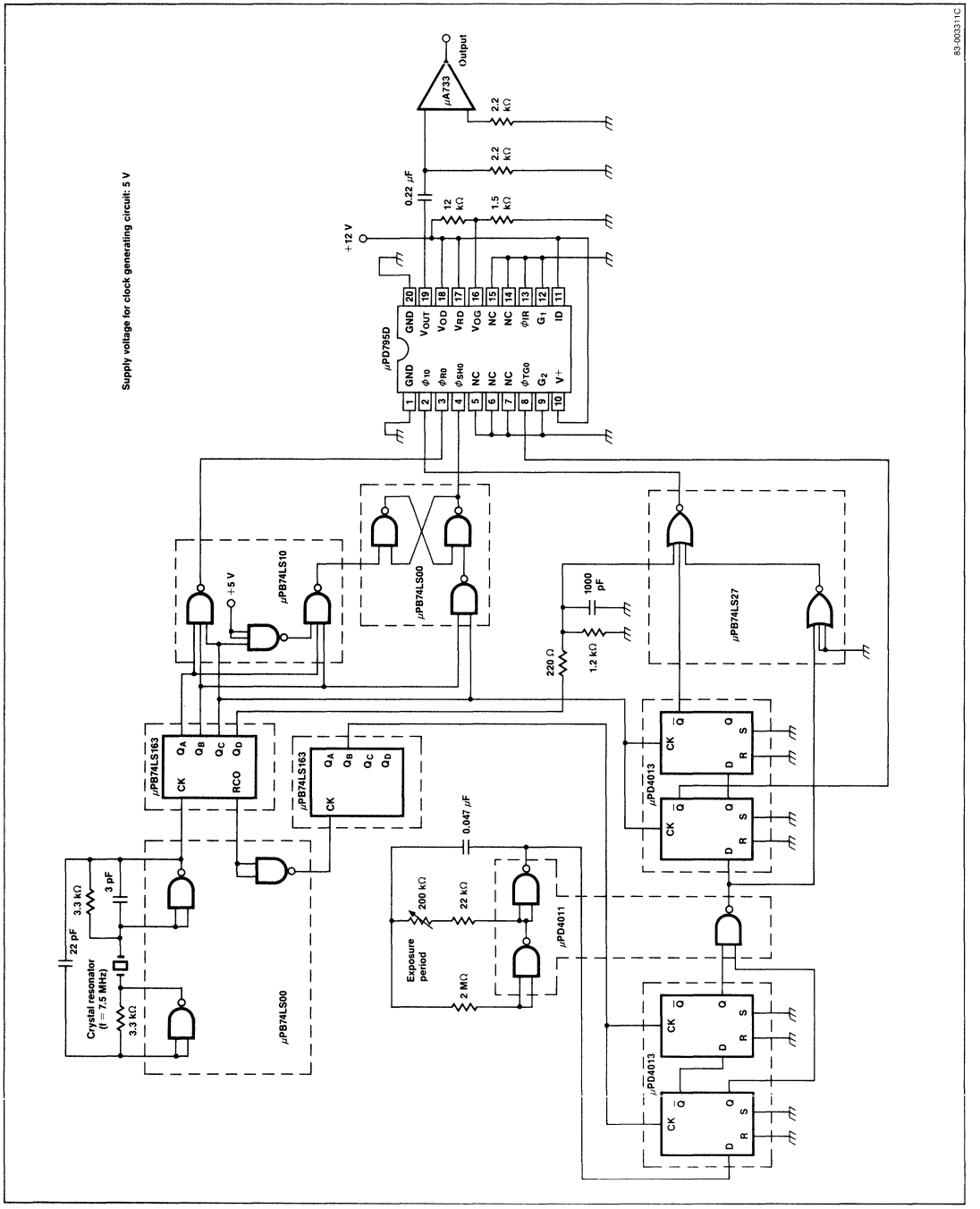


Sensitivity [S]. Quotient of the output level divided by exposure (lx•s).

Offset Voltage [V_{OS}]. Output terminal potential with no exposure.

8

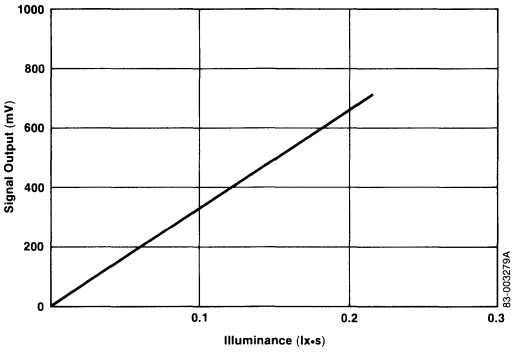
Example of Driving Circuit



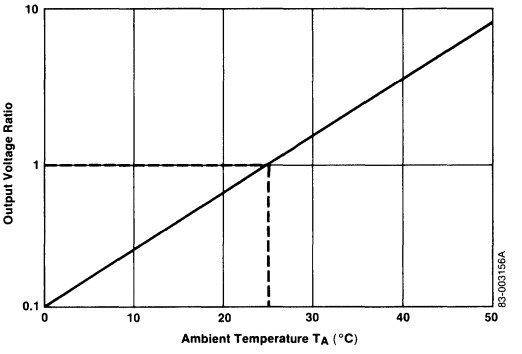
Operating Characteristics

$T_A = 25°C$

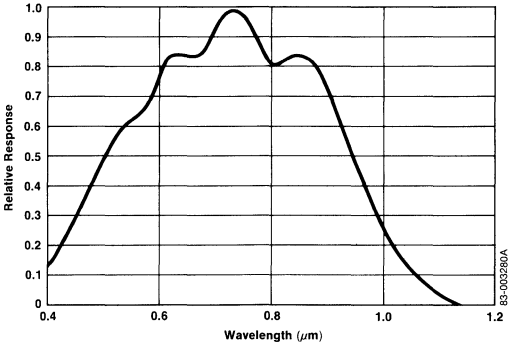
Signal Output



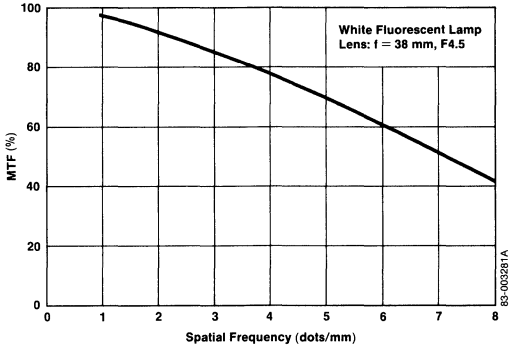
Dark Signal



Relative Spectrum Response



MTF



8

μPD799
2048-BIT CCD IMAGE SENSOR

PRELIMINARY INFORMATION

Description

The μPD799 is a CCD (charge-coupled device) linear image sensor that changes optical images to electrical signals. It has 2048 photo-elements, two lines of 1037-bit CCD charge transfer registers, an output amplifier, and a compensation signal amplifier.

The photo-elements have excellent response characteristics because of their PN junction construction. They are 14 by 9 μm separated by 5-μm channel stoppers.

The CCD charge transfer registers have very high transfer efficiency, above 99.996 percent.

Features

- ☐ Excellent photo-electrical characteristics
- ☐ Single 12-volt power supply
- ☐ Compensation amplifier signal can reduce output signal noise
- ☐ High resolution of 16 dots per mm across 25.6-cm page
- ☐ Transfer efficiency above 99.996 percent
- ☐ 24-pin ceramic DIP

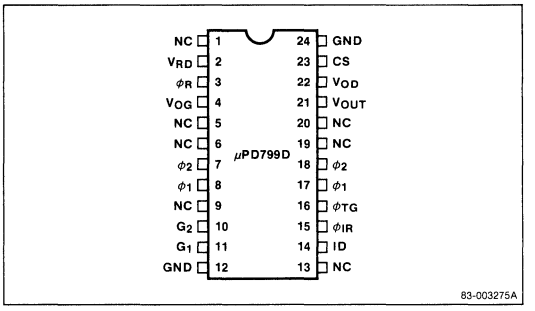
Applications

Facsimile
OCR (optical character reader)
Instrumentation

Ordering Information

Part Number	Package	Operating Ambient Temperature
μPD799D	24-pin ceramic DIP	−25 to +55°C

Pin Configuration



Pin Identification

Pin	Name	*Function
1	NC	No connection
2	V_{RD}	Reset part power supply input
3	ϕ_R	Reset gate clock input
4	V_{OG}	Output gate bias input
5, 6	NC	No connection
7, 8	ϕ_2, ϕ_1	Register clock input
9	NC	No connection
10	G_2	Test input
11	G_1	Test input
12	GND	Ground
13	NC	No connection
14	ID	Test input
15	ϕ_{IR}	Test input
16	ϕ_{TG}	Transfer gate clock input
17, 18	ϕ_1, ϕ_2	Register clock input
19, 20	NC	No connection
21	V_{OUT}	Output
22	V_{OD}	Output amplifier power supply input
23	CS	Compensation signal output
24	GND	Ground

*All NC pins should be connected to ground.

8

Block Diagram

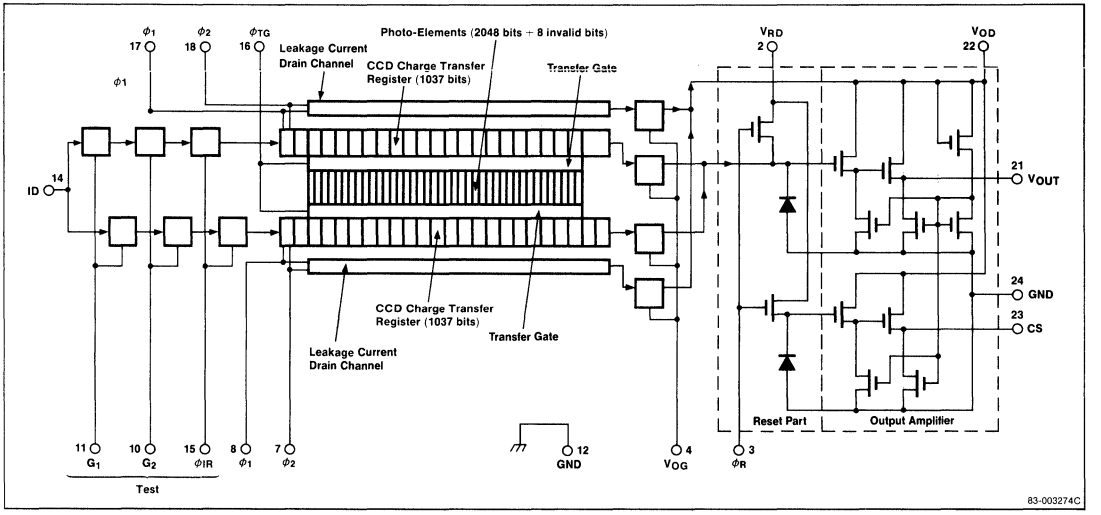
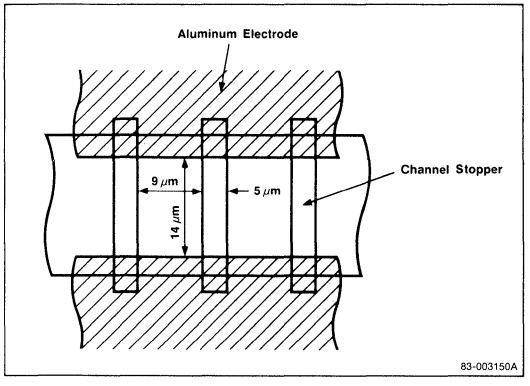


Photo-Element Construction



Electrical Characteristics

$T_A = +25°C$; source of light, 2856 K tungsten lamp; exposure period = 5.0 ms; V_{ID}, V_{OD}, and V_{RD} = 12.0 V; V_{OG} = 2.0 V; V_{G1} and V_{G2} = 0 V; ϕ_{TG} = 10 μs.

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Saturation Output Voltage	V_{SAT}	400	700		mV	
Saturation Exposure	SE		0.20		lx•s	
Photo-Response Nonuniformity	PRNU		±14	±20	%	V_{OUT} = 200 mV; infrared cut filter, Corning 1-75
Average Dark Signal	ADS		3	10	mV	No exposure
Dark Signal Nonuniformity	DSNU		5	15	mV	No exposure
Working Power Consumption	P_D	25	45	70	mW	Current of pins 22 and 2 x supply voltage
Spectral Response Range Limits	SR	0.3		1.1	μm	
Sensitivity	S	2000	3500	4500	mV/lx•s	
Offset Voltage	V_{IO}	5.5	7.0	8.5	V	0% level of V_{OUT} in timing waveforms
Output Delay Time	t_d		50	120	ns	$t_{\phi F}$ of ϕ_1 and ϕ_2 in timing waveforms = 30 ns

Reference Characteristics

Parameter	Limits Min	Typ	Max	Unit
Input Capacitance at ϕ_1 or ϕ_2 (pins 7, 8, 17, 18)	400	800	1200	pF
Input Capacitance at ϕ_R (pin 3)	5	10	15	pF
Input Capacitance at ϕ_{TG} (pin 16)	20	40	60	pF
Output Impedance at V_{OUT} or CS (pins 21, 23)	1.0	2.0	3.0	kΩ

Absolute Maximum Ratings

$T_A = +25°C$

Output Amplifier Supply Voltage, V_{OD}	−0.3 to +18 V
Reset Part Supply Voltage, V_{RD}	−0.3 to +18 V
Output Gate Voltage, V_{OG}	−0.3 to +18 V
Register Clock Signal Voltage, $V_{\phi 1 \phi 2}$	−0.3 to +18 V
Transfer Gate Clock Signal Voltage, $V_{\phi TG}$	−0.3 to +18 V
Reset Gate Clock Signal Voltage, $V_{\phi R}$	−0.3 to +18 V
Operating Temperature, T_{OPT}	−25 to +55°C
Storage Temperature, T_{STG}	−40 to +100°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

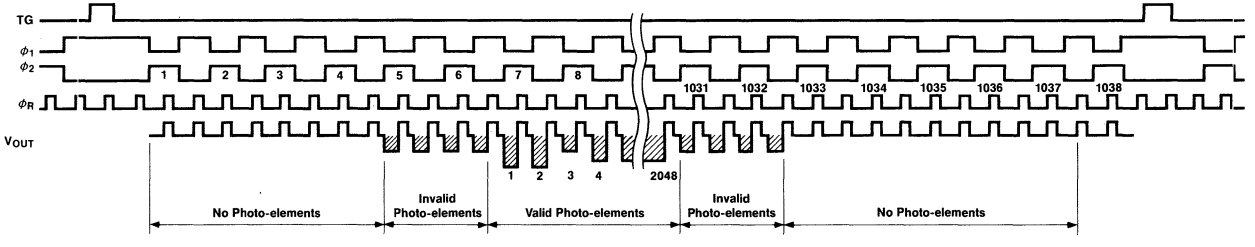
$T_A = -25$ to $+55°C$

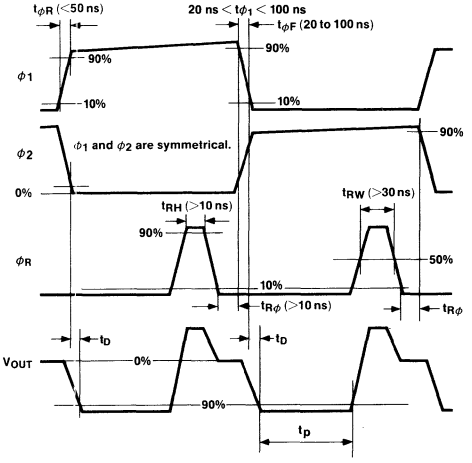
Parameter	Symbol	Limits Min	Typ	Max	Unit
Output Amplifier Supply Voltage	V_{OD}	11.4	12.0	12.6	V
Reset Part Supply Voltage	V_{RD}	11.4	12.0	12.6	V
Output Gate Bias Voltage	V_{OG}	1.0	2.0	3.0	V
Test Terminal G_1 Voltage	V_{G1}		0		V
Test Terminal G_2 Voltage	V_{G2}		0		V
Test Terminal ID Voltage	V_{ID}	11.4	12.0	12.6	V
Test Terminal ϕ_{IR} Voltage	$V_{\phi IR}$		0		V
High Level of Register Clock Signal	$V_{\phi 1 \phi 2H}$	9.0	12.0	12.6	V
Low Level of Register Clock Signal	$V_{\phi 1 \phi 2L}$	−0.3	0	0.5	V
High Level of Transfer Gate Clock Signal	$V_{\phi TGH}$	9.0	12.0	12.6	V
Low Level of Transfer Gate Clock Signal	$V_{\phi TGL}$	−0.3	0	0.5	V
High Level of Reset Gate Clock Signal	$V_{\phi RH}$	9.0	12.0	12.6	V
Low Level of Reset Gate Clock Signal	$V_{\phi RL}$	−0.3	0	0.5	V
Register Clock Signal Frequency (see Note)	$f_{\phi 1 \phi 2}$		0.2	1.75	MHz
Reset Gate Clock Signal Frequency (see Note)	$f_{\phi R}$		0.4	3.5	MHz

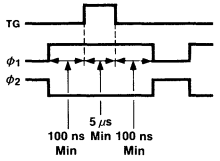
Note: At lower frequencies, t_P of output signal is >100 ns. (See Timing Waveforms.)

8

Timing Waveforms







- The crossing voltage of ϕ_1 and ϕ_2 should be kept above V_{OG} + 1 V.
- The register clock signal should be not more than 1038 cycles.
- Width of the transfer gate pulse should be less than 20 μs.

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NEC

Definitions of Electrical Parameters

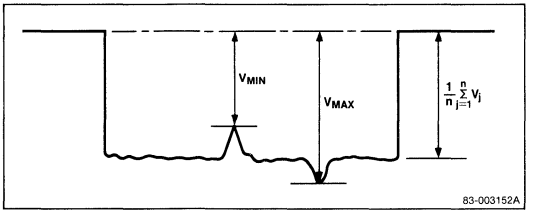
Saturation Output Voltage [V_{SAT}]. An output signal level above which the PRNU (photo-response nonuniformity) is ≥10% or the response is nonlinear.

Saturation Exposure [SE]. Product of illuminance (lx) and exposure period (s) in which the output is saturated.

Photo-Response Nonuniformity [PRNU]. Percentage of peak output level and bottom output level against average output level of all valid photo-elements in static and uniform light.

$$PRNU\ (\%) = \left(\frac{V_{MAX} \text{ or } V_{MIN}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1\right) \times 100$$

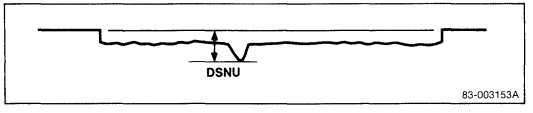
where
n = number of valid photo-elements
V_j = output voltage of each photo element



Average Dark Signal [ADS]. Average output level of valid photo-elements with no exposure.

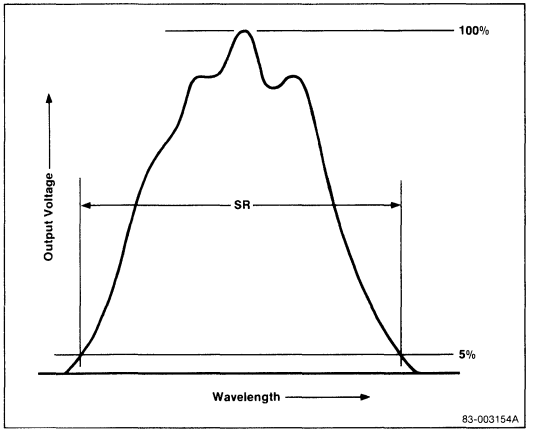
$$ADS\ (mV) = \frac{1}{n}\sum_{j=1}^{n} V_j$$

Dark Signal Nonuniformity [DSNU]. Peak output level with no exposure.



Working Power Consumption [P_W]. Product of supply voltage and current when supply voltage is 12.0 V.

Spectral Response Range Limits [SR]. Short side and long side limits of response spectral range having sensitivity above 5 percent of sensitivity of most sensitive wavelength.



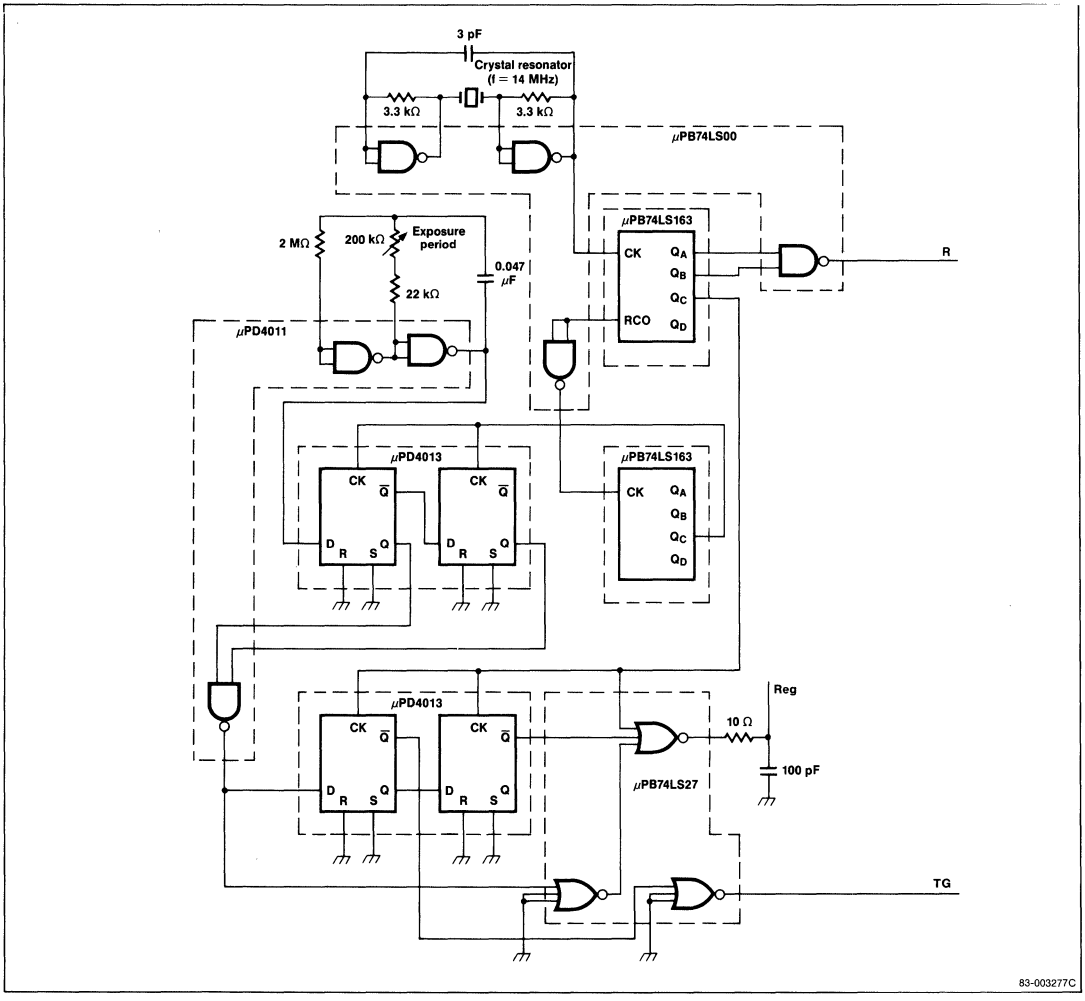
Sensitivity [S]. Quotient of the output level divided by exposure (lx•s).

Offset Voltage [V_{OS}]. Output terminal potential with no exposure.

8

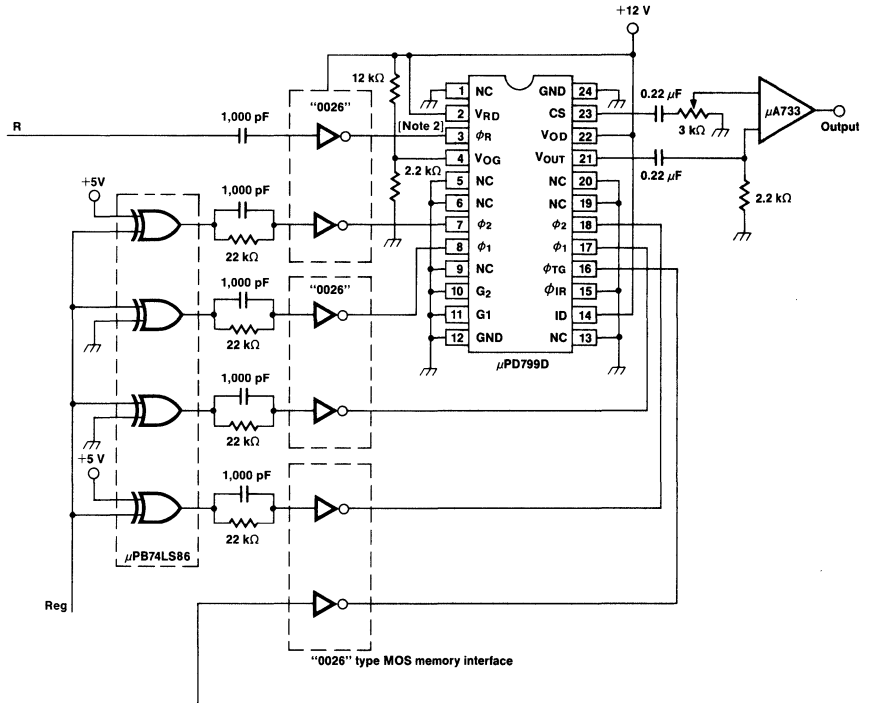
Example of Driving Circuit

(Sheet 1 of 2)



Example of Driving Circuit (Cont.)

(Sheet 2 of 2)



Note:

(1) Supply voltage for clock generating circuits is +5 V.

(2) If ringing is present on the ϕ_R waveform, try connecting a resistor and capacitor in series between pin 3 and ground as a damping circuit. Approximate values are 68 Ω and 330 pF.

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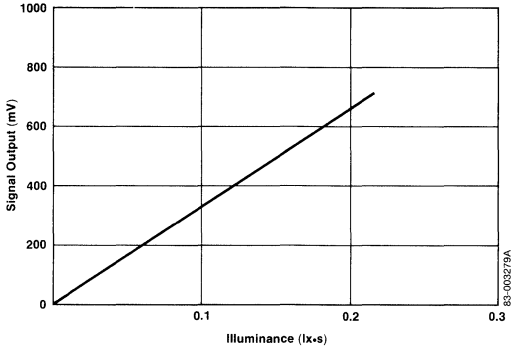
8

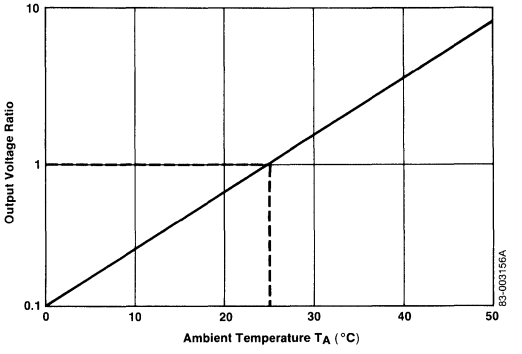
Operating Characteristics

$T_A = 25°C$

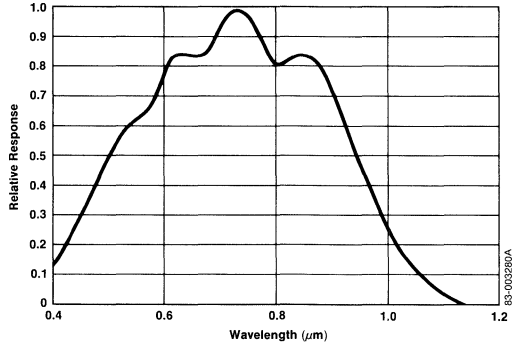
Signal Output



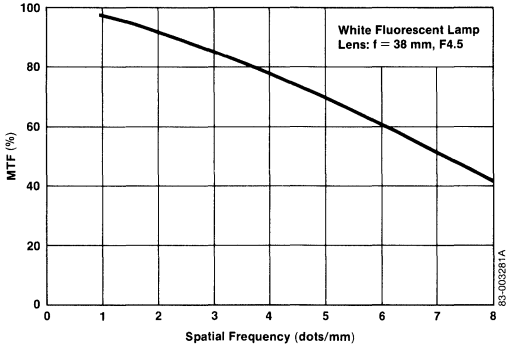
Dark Signal



Relative Spectrum Response



MTF



PACKAGING INFORMATION

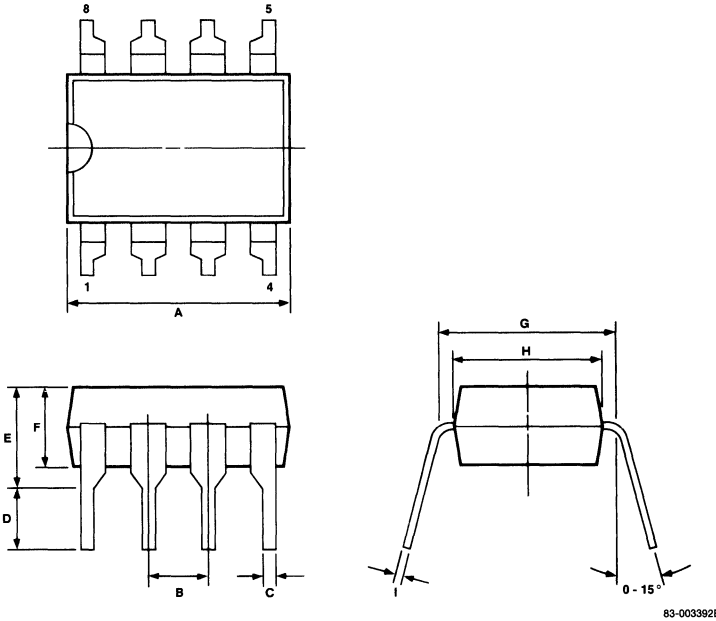
9

Section 9 — Packaging Information

8-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	10.5 max	.413 max
B	2.54 [TP]	.100 [TP]
C	.5	.002
D	2.7 min	.106
E	5.80 max	.228
F	.5	.002
G	6.40 [TP]	.252 [TP]
H	7.62	.300
I	.25	.010

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "G" to center of leads when formed parallel.

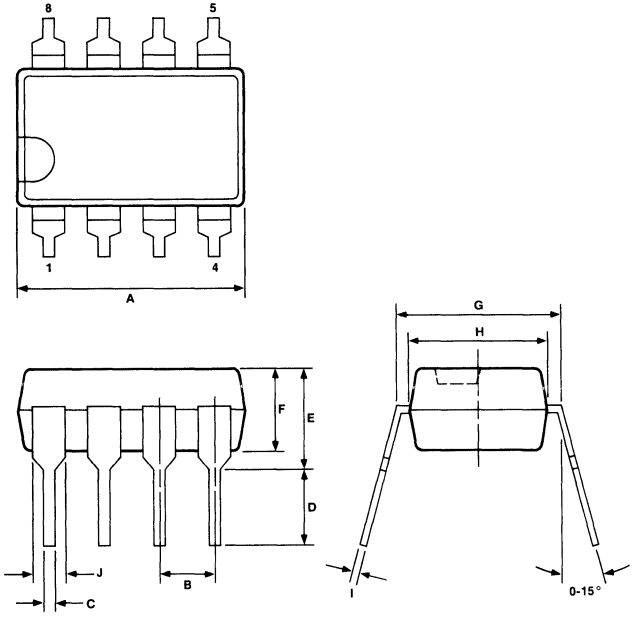


83-003392B

8-Pin Plastic DIP (300 mil) (μPC3423 only)

Item	Millimeters	Inches
A	10.5 max	.413
B	2.54 [TP]	.100 [TP]
C	.5	.002
D	3.5	.138
E	4.7	.185
F	3.8	.150
G	6.40 [TP]	.252 [TP]
H	7.6	.299
I	.3	.012
J	1.2	.047

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "G" to center of leads when formed parallel.



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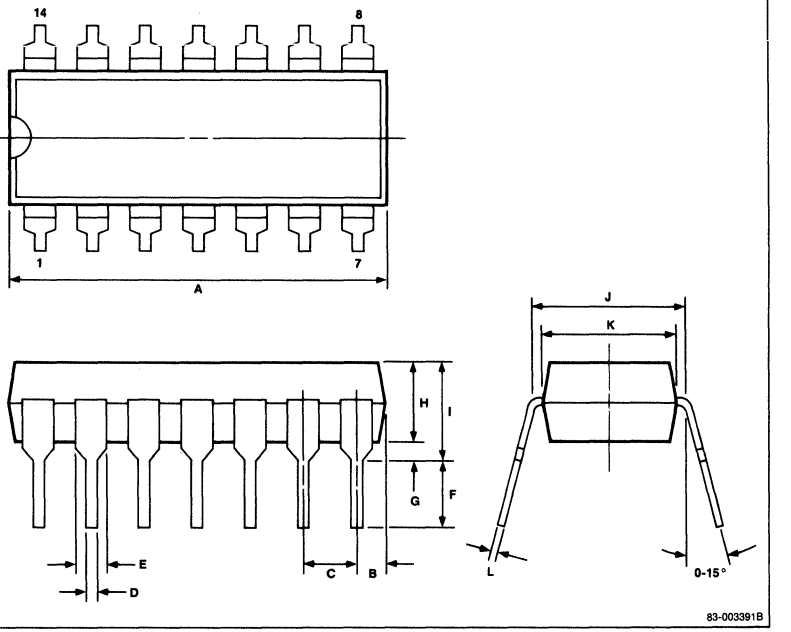
9

14-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	20.32 max	.800 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	1.2 min	.047 min
F	3.6 ± 0.3	.142 ±.012
G	.51 min	.020 min
H	4.31 max	.170 max
I	5.08 max	.200 max
J	7.62 [TP]	.300 [TP]
K	6.4	.252
L	.25 $^{+.10}_{+.05}$	.010 $^{+.004}_{-.003}$

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "J" to center of leads when formed parallel.

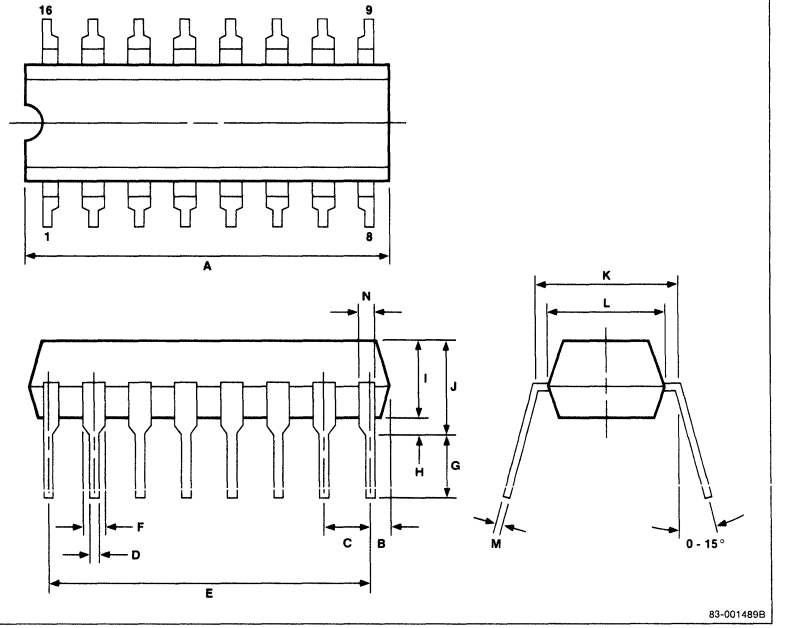


83-003391B

16-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	20.32 max	0.8 max
B	1.27 max	.05 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	17.78	.70
F	1.2 min	.047 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.08 max	.2 max
K	7.62 [TP]	.3 [TP]
L	6.4	.252
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$
N	1.0 min	.039 min

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

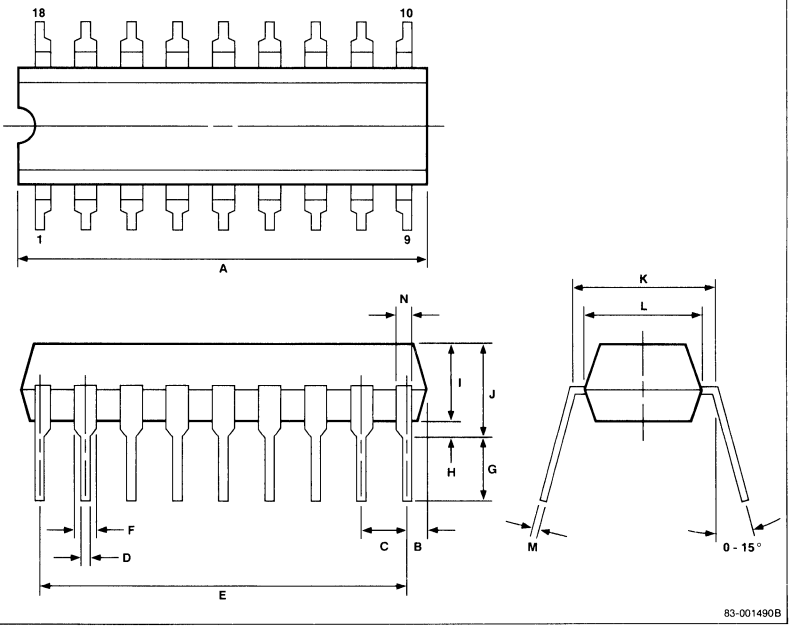


83-001489B

18-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	22.86 max	.9 max
B	1.27 max	.05 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	20.32	.8
F	1.2 min	.047 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.08 max	.2 max
K	7.62 [TP]	.3 [TP]
L	6.4	.252
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$
N	1.0 min	.039 min

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

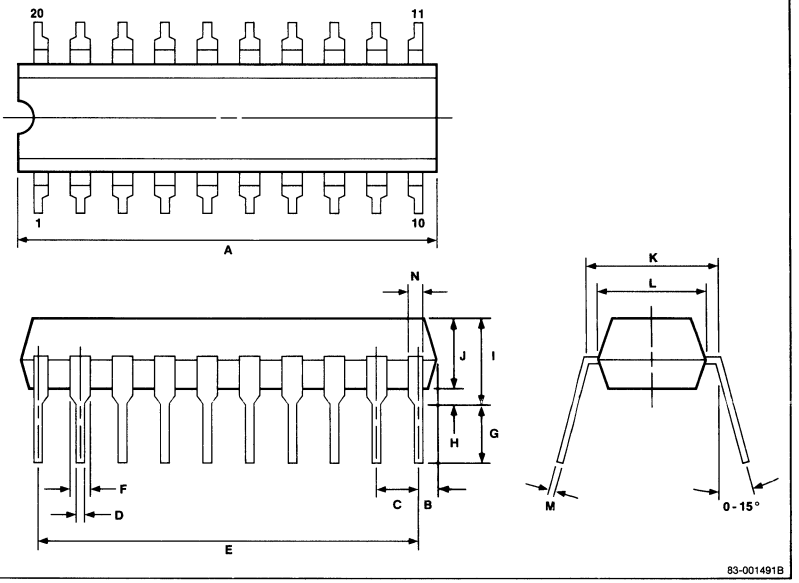


83-001490B

20-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	25.40 max	1.0 max
B	1.27 max	.05 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	22.86	.9
F	1.1 min	.043 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.08 max	.2 max
K	7.62 [TP]	.3 [TP]
L	6.4	.252
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$
N	.9 min	.035 min

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.



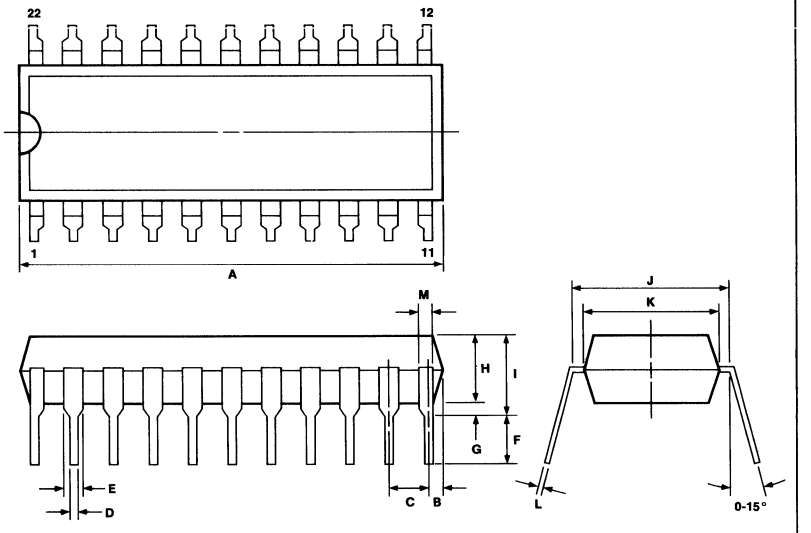
83-001491B

9

22-Pin Plastic DIP (400 mil)

Item	Millimeters	Inches
A	27.94 max	1.100 max
B	1.27 max	.050 max
C	2.54[TP]	.100[TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	1.2 min	.047 min
F	3.5 ± 0.3	.138 ± .012
G	.51 max	.020 max
H	4.31 max	.170 max
I	5.72 max	.226 max
J	10.16[TP]	.400[TP]
K	8.6	.339
L	.25 $^{+.10}_{+.05}$	.010 $^{+.004}_{-.003}$
M	0.8 min	.031 min

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "J" to center of leads when formed parallel.

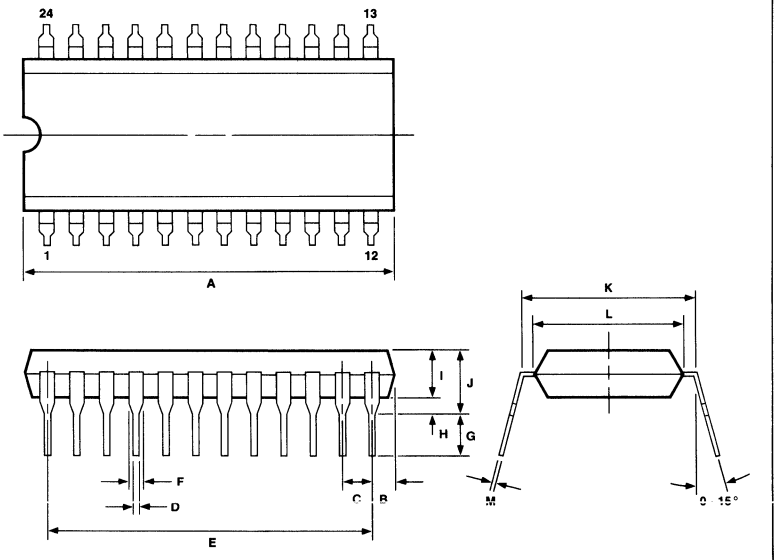


83-003393B

24-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	33.02 max	1.3 max
B	2.54 max	.10 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	27.94	1.1
F	1.2 min	.047 min
G	3.6 ± .3	.138 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.72 max	.226 max
K	15.24 [TP]	.60 [TP]
L	13.2	.52
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

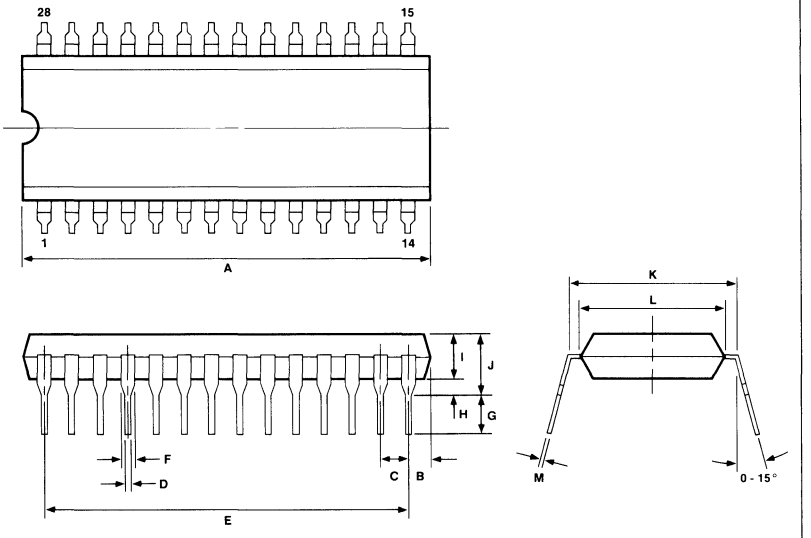


83-001492B

28-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	38.1 max	1.5 max
B	2.54 max	.10 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	33.02	1.3
F	1.2 min	.047 min
G	3.6 ± .3	.142 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.72 max	.226 max
K	15.24 [TP]	.60 [TP]
L	13.2	.52
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

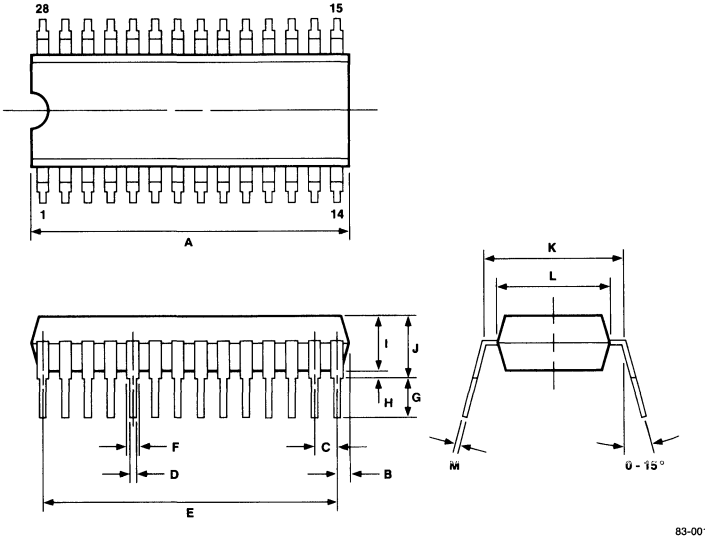


83-001407B

28-Pin Plastic Shrink DIP (400 mil)

Item	Millimeters	Inches
A	28.46 max	1.121 max
B	2.67 max	.106
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.02 $^{+.004}_{-.005}$
E	24.89	.98
F	.9 min	.035 min
G	3.2 ± 0.3	.126 ± 012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	8.6	.339
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.



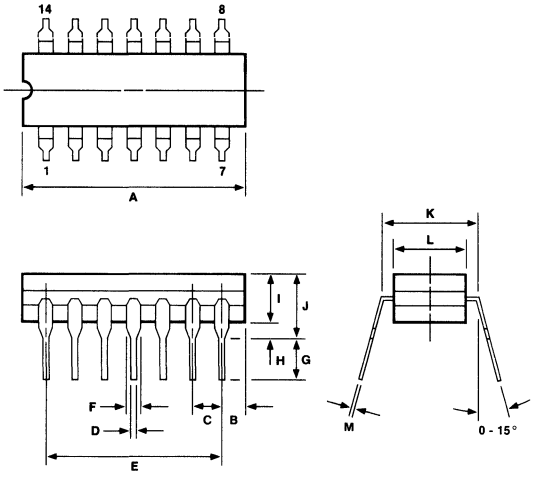
83-001519B

9

14-Pin Ceramic Package (300 mil)

Item	Millimeters	Inches
A	19.9 max	.78 max
B	2.35	.09
C	2.54 [TP]	.1 [TP]
D	.46	.018
E	15.2	.6
F	1.5	.059
G	3.0 min	.118 min
H	.5 min	.02 min
I	4.58 max	.181 max
J	5.08 max	.2 max
K	7.62 [TP]	.3 [TP]
L	6.4	.25
M	.25	.01

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

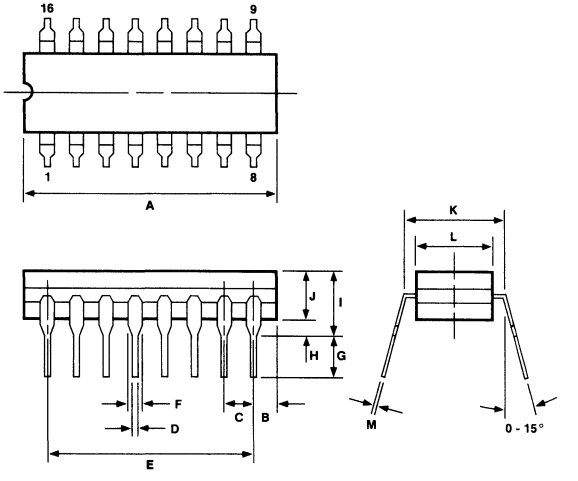


83-001523B

16-Pin Cerdip Package (300 mil)

Item	Millimeters	Inches
A	19.9 max	.784 max
B	1.06	.042
C	2.54 [TP]	.10 [TP]
D	.46 ± .10	.018 ± .004
E	17.78	.70
F	1.5	.059
G	2.54 min	.10 min
H	.5 min	.019 min
I	4.58 max	.181 max
J	5.08 max	.20 max
K	7.62 [TP]	.30 [TP]
L	6.4	.25
M	$.25^{+.10}_{-.05}$	$.0098^{+.0039}_{-.0019}$

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

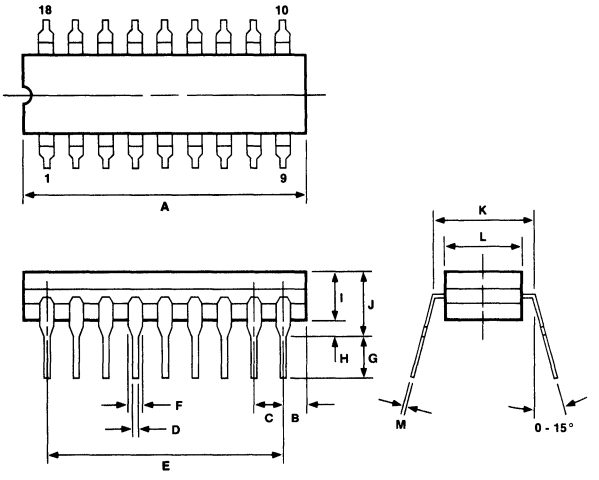


83-001516B

18-Pin Cerdip Package (300 mil)

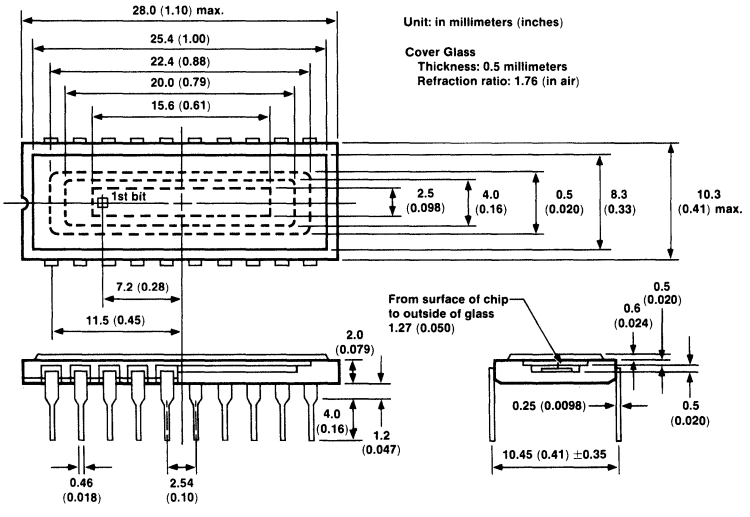
Item	Millimeters	Inches
A	23.2 max	.91 max
B	1.44	.055
C	2.54 [TP]	.10 [TP]
D	.45	.02
E	20.32	.8
F	1.2	.06
G	2.5 min	.1 min
H	.5 min	.02 min
I	4.6 max	.18 max
J	5.1 max	.2 max
K	7.62 [TP]	.3 [TP]
L	6.7	.26
M	.25	.01

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.



83-001517B

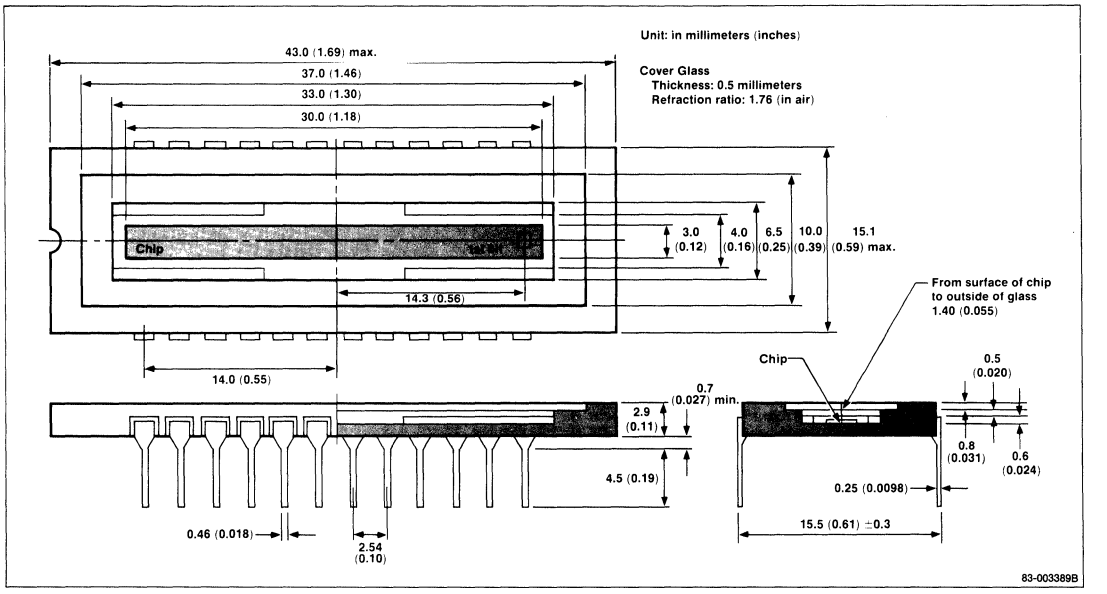
20-Pin Ceramic DIP (μPD795D)



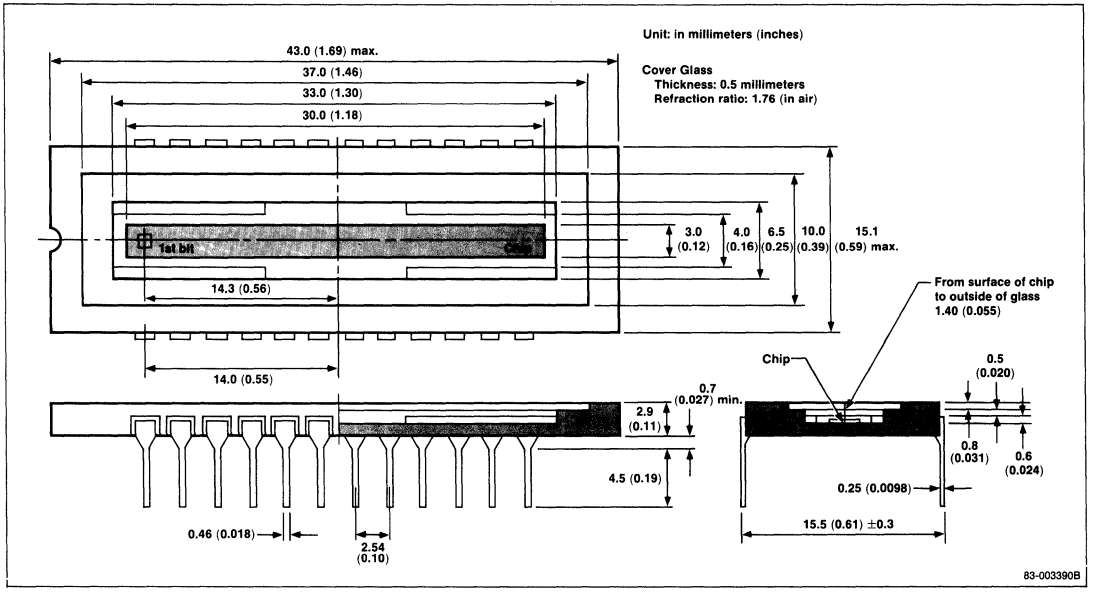
83-003386B

9

24-Pin DIP (μPD791D)



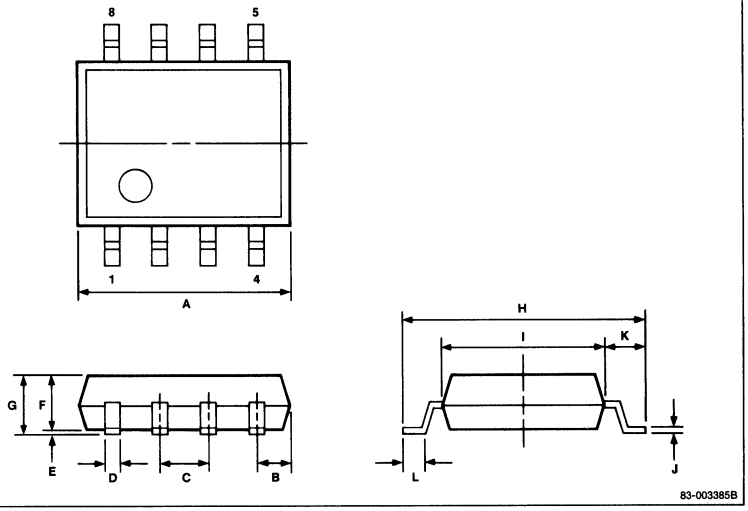
24-Pin DIP (μPD799D)



8-Pin Plastic Miniflat (225 mil)

Item	Millimeters	Inches
A	5.70 max	.22 max
B	.94 max	.037 max
C	1.27 [TP]	.05 [TP]
D	$.40^{+.10}_{-.05}$	$.016^{+.004}_{-.002}$
E	.1 ± .1	.004 ± .004
F	1.49 max	.059 max
G	1.80 min	.071 max
H	6.5 ± .3 [TP]	.256 ± .011 [TP]
I	4.4 max	.173 max
J	$.15^{+.10}_{-.05}$	$.006^{+.004}_{-.002}$
K	1.1 max	.004 max
L	.6 ± .2	.024 ± .008

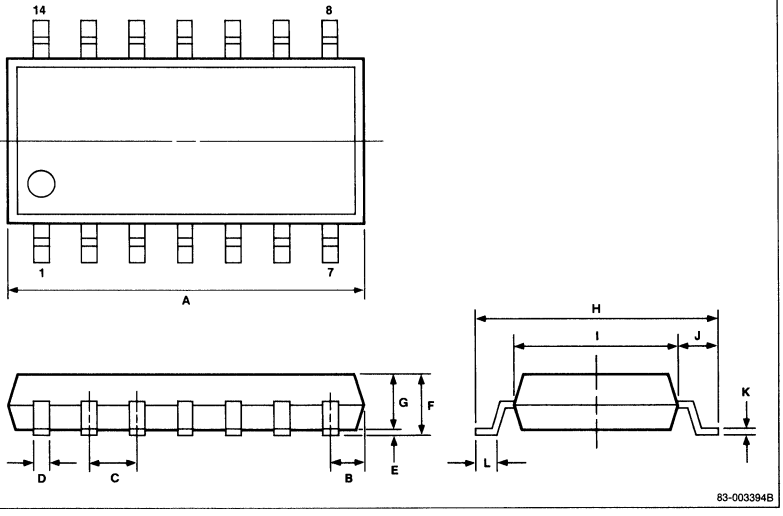
Note: Each lead centerline is located within 0.12 mm (0.005) of its true position (TP) at maximum material condition.



14-Pin Miniflat IC (225 mil)

Item	Millimeters	Inches
A	10.46 max	.412 max
B	1.42 max	.056 max
C	1.27 [TP]	.050 [TP]
D	$.40^{+.10}_{-.05}$	$.016^{+.004}_{-.003}$
E	.1 ± .1	.004 ± .004
F	1.8 max	.071 max
G	1.49	.059
H	6.5 ± .3	.256 ± .012
I	4.4	.173
J	1.1	.043
K	$.15^{+.10}_{-.05}$	$.006^{+.004}_{-.002}$
L	.6 ± .2	$.024^{+.004}_{-.009}$

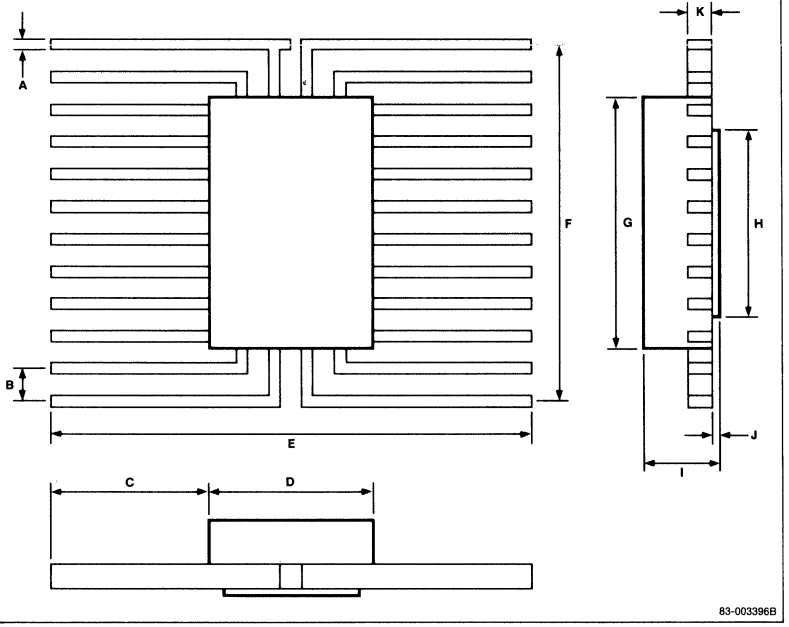
Note: Each lead centerline is located within 0.12 mm (0.005) of its true position (TP) at maximum material condition.



9

24-Pin Ceramic Flatpack B

Item	Millimeters	Inches
A	.43 ± .05	.017 ± .002
B	1.27 typ	.050 typ
C	6.35 min	.250 min
D	6.60 ± .15	.260 ± .006
E	19.30 ± .15	.760 ± .006
F	13.97 typ	.550 typ
G	10.11 ± .18	.398 ± .007
H	7.49 ref	.295 ref
I	3.05	.120 max
J	.305	.012 min
K	.13 ± .03	.005 ± .001

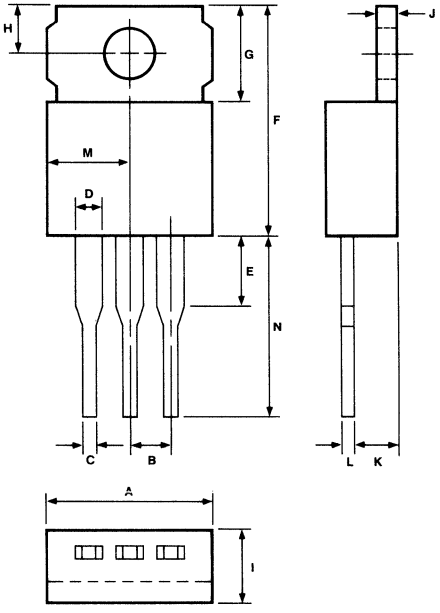


83-003396B

3-Pin SIP TO-220

Item	Millimeters	Inches
A	10.66 max	.420 max
B	2.54 [TP]	.100 [TP]
C	$.8^{+.34}_{-.29}$	$.031^{+.013}_{-.011}$
D	1.3	.051
E	6.35 max	.250 max
F	12.7 min	.500 min
G	5.85 min	.230 min
H	$3.0^{+.30}_{-.46}$	$.118^{+.012}_{-.018}$
I	4.82 max	.190 max
J	1.3 ± .2	.051 ± .008
K	$2.8^{+.12}_{-.76}$	$.110^{+.005}_{-.030}$
L	.5 ± .2	.020 ± .008
M	5.33 max	.210 max
N	15.87 max	.625 max

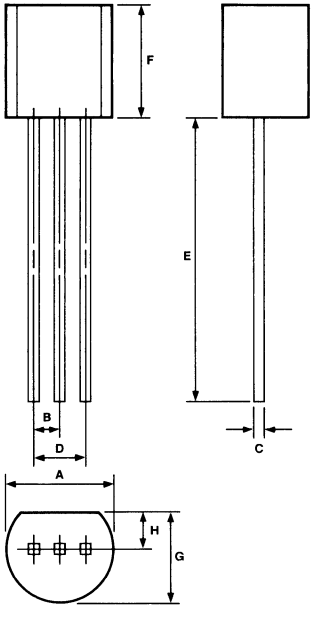
Note: Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



83-003388B

3-Pin SIP TO-92

Item	Millimeters	Inches
A	5.2 max	.205 max
B	1.27 max	.067 max
C	.5	.002
D	2.54	.100
E	14 min	.551 min
F	5.5 max	.217 max
G	4.2 max	.165 max
H	1.77 max	.070 max

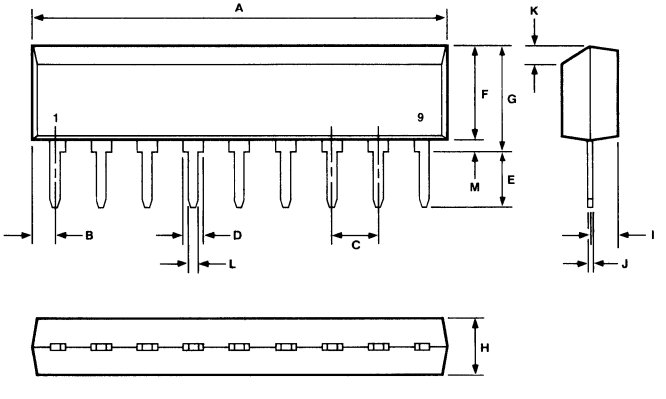


83-003399B

9-Pin Plastic SIP

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.05
C	2.54 [TP]	.100 [TP]
D	1.1 min	.004 min
E	2.9 min	.114 min
F	5.08 max	.200 max
G	5.72 max	.225 max
H	3.0 max	.118 max
I	1.5 max	$.059^{+.040}_{-.020}$
J	$.25^{+.10}_{-.05}$	$.006^{+.004}_{-.002}$
K	1.1	.004
L	.5	.2
M	.51 min	.2 min

Note: Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



83-003387B

Thermal Information

The power dissipation capability of semiconductor devices is limited by the maximum allowable junction temperature, the ambient temperature, and the thermal resistance between the junction and the ambient environment.

The temperature difference between the junction and the ambient environment is determined by the following equation.

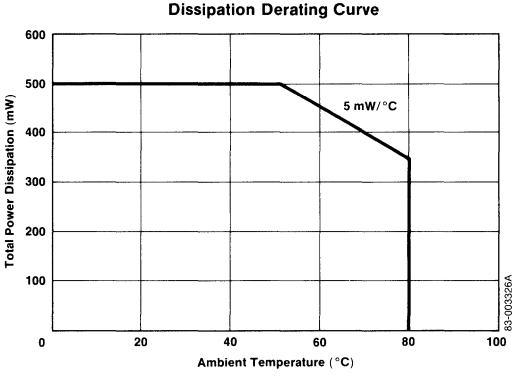
$T_J - T_A = P_D \theta_{JA}$

where T_J = junction temperature, °C
T_A = ambient temperature, °C
P_D = power dissipation, W
θ_{JA} = thermal resistance, junction to ambient, °C/W

The maximum allowable junction temperature is 150 °C, however, the maximum junction temperature of plastic package IC's should be 125 °C because of the storage temperature range limitation.

The dissipation derating curves that follow assume the ambient environment is still air, and that no heat sink is used.

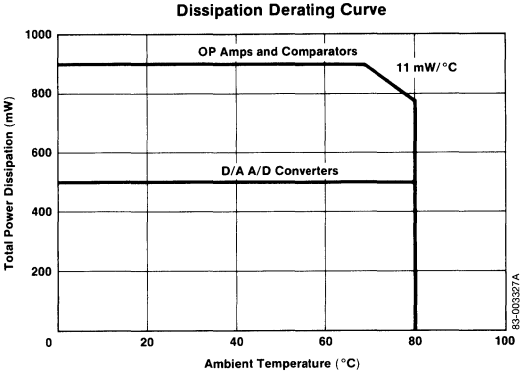
1. 8 Pin Metal Can Package and Cavity DIP



θ_{JA} = 200 °C/W typ. T_J max = 150 °C

The maximum power dissipation value of 500 mW has been fixed considering the practical applications of operational amplifiers and comparators.

2. 14 Pin Through 20 Pin Cavity DIP

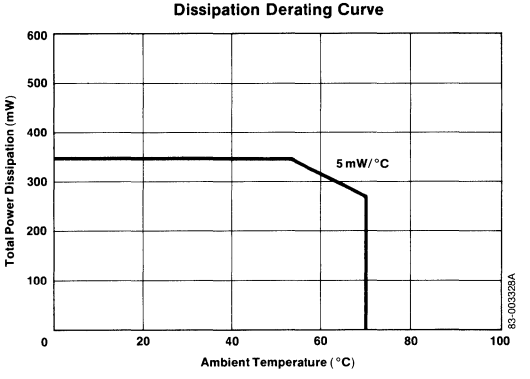


θ_{JA} = 90 °C/W typ. T_J max = 150 °C

The maximum power dissipation value has been fixed considering the practical applications.

Operational Amplifiers and Comparators	900 mW
D/A, A/D Converters	500 mW

3. 8 Pin Plastic Molded DIP



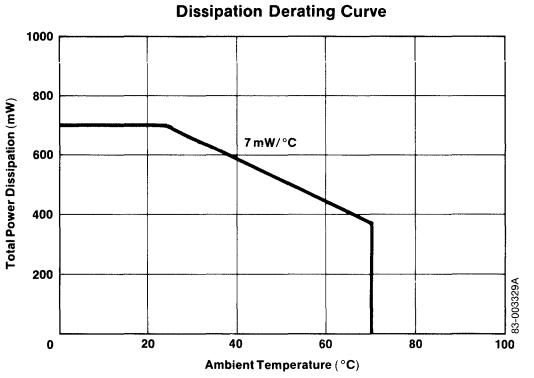
(except for μPC4556C, μPC4557C, μPC4560C, μPC1555C)

θ_{JA} = 200 °C/W typ. T_J max = 125 °C

The maximum power dissipation value of 250 mW has been fixed considering the practical applications of operational amplifiers and comparators.

9

4. 8 Pin Plastic Molded DIP



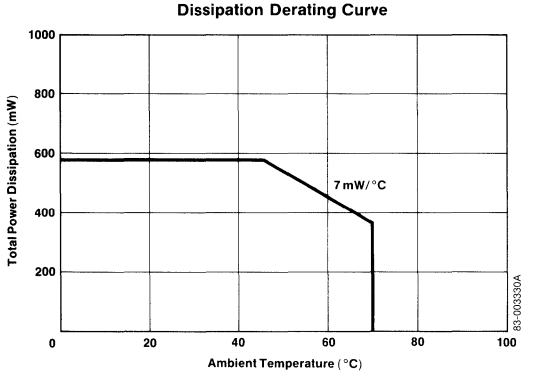
(For μPC4556C, μPC4557C, μPC4560C, μPC1555C)

θ_{JA} = 140 °C/W typ. T_J max = 125 °C

The maximum power dissipation value has been fixed considering the maximum junction temperature and the practical applications of those IC's.

μPC4556, μPC4557, μPC4560C	700 mW
μPC1555C	600 mW

5. 14 Pin Plastic Molded DIP



θ_{JA} = 140 °C/W typ. T_J max = 125 °C

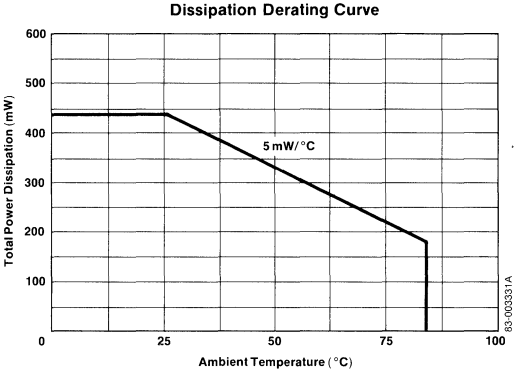
The maximum power dissipation value of 570 mW has been fixed considering the practical applications of operational amplifiers and comparators.

6. Miniflat Package

When the miniflat IC's are mounted on a hybrid IC, the heat radiation through the leads is increased. When resin coated, the heat radiation through the environment is further increased. As a result, the thermal resistance in the mounted state is much smaller than in element form alone.

It is suggested that the heat dissipation in actually mounted condition be fully investigated.

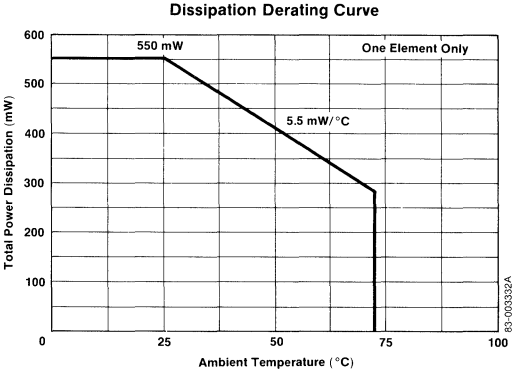
6A. 8 Pin Mini flat Package



θ_{JA} = 220 °C/W typ. T_J max = 125 °C

The maximum power dissipation value of 440 mW has been fixed considering the maximum junction temperature and the practical applications of miniflat IC's.

6B. 8 Pin Mini flat Package



θ_{JA} = 180 °C/W typ. T_J max = 125 °C

The maximum power dissipation value of 550 mW has been fixed considering the maximum junction temperature and the practical applications of miniflat IC's.

Taping Specifications

Tape and reel shipping has been used for many years in Japan for shipping surface mount transistors and capacitors. Currently, 75% of surface mount transistors are shipped via this method. Tape and reel specifications, formally established by Japanese Standard RC-1009A for 12 mm tape, has now been expanded to include surface mount ICs.

Surface mount technology in the United States has recently come of age, and in May of 1985 the EIA developed Standard EIA481 for Embossed Tape and Reel Packaging. NEC has adjusted the current Japanese standard to comply with EIA481, and is now shipping surface mount devices to this specification.

Because of the need for electrostatic packaging, NEC chose to manufacture the tape using carbon/PVC material. This type of "filler mixed" plastic is difficult to emboss, thus the actual tape manufacturing is done by the Sumitomo Bakelite Corp in Japan.

The actual manufacturing process is shown in Figure 1. First, rolled sheet material is slittized and embossed. Next, the sprocket holes are punched, and aligned with the embossed pockets to a tolerance of ±50 microns. Finally, the pocket holes are punched, and the tape is cut to length and put on the reel.

Specifications:
NEC's embossed tape is manufactured to EIA481 specifications with special attention paid to dimensional accuracy. See Table 1 and Figure 2. Table 2 and Figure 3 show Reel Dimensions. Figure 4 illustrates the Tape End Configurations. Figure 5 shows component placement in the tape pockets. Table 3 gives the device package-to-tape width specifications. Figures 6, 7 and 8 show the tape and reel specifications for the specialized case of 8, 14 and 16-pin miniflats.

Figure 1. Manufacturing Processes of Embossed Carrier Tape

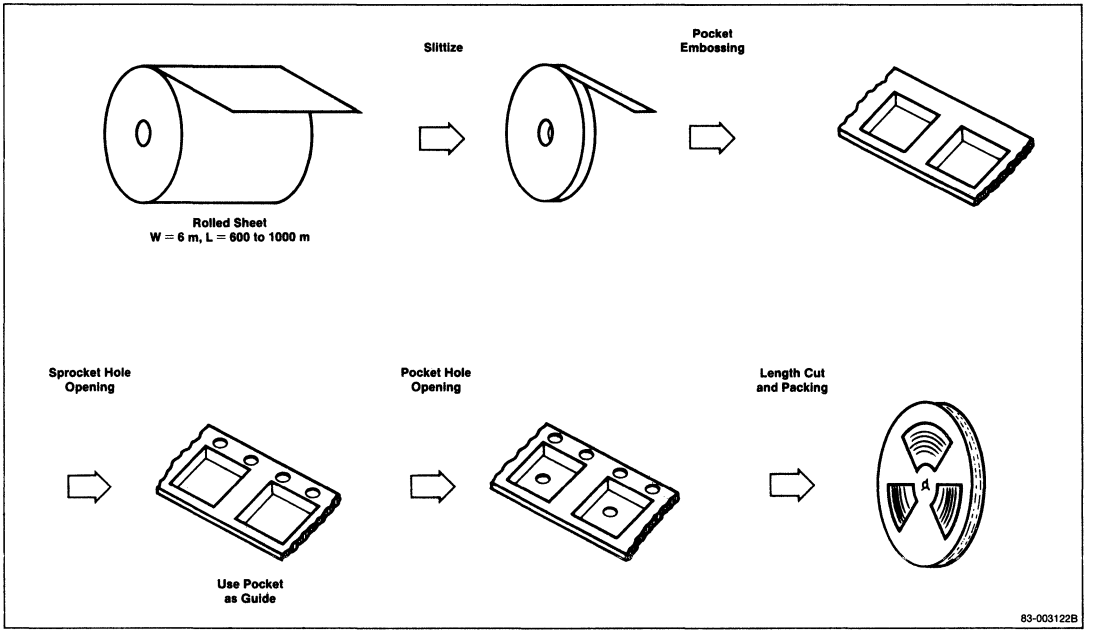


Table 1. 8, 12, 16, 24 mm Embossed Tape

Tape Size	D	E	P_0	t (Max.)	A_0, B_0, K_0	
8, 12, 16, 24 mm	$1.5^{+0.10}_{-0.0}$ ($.059^{+.004}_{-0.01}$)	1.75 ± 0.10 (.069 ± .004)	4.0 ± .10 (.157 ± .004)	0.400 (.016)	See Note 1 Table 2	Constant Dimensions

Tape Size	B_1 Max.	D_1 Min.	F	K Max.	P_2	R Min.	W	
8 mm	4.2 (.165)	1.0 (.039)	3.5 ± 0.05 (.138 ± .002)	2.4 (.094)	2.0 ± 0.05 (.079 ± .002)	25 (.984)	8.0 ± .30 (.315 ± .012	Variable Dimensions
12 mm	8.2 (.323)		5.5 ± 0.05 (.217 ± .002)	4.5 (.177)		30 (1.181)	12.0 ± .30 (.472 ± .012)	
15 mm	12.1 (.476)	1.5 (.059)	7.5 ± 0.10 (.295 ± .004)	6.5 (.256)	2.0 ± 0.10) (.079 ± .004)	40 (1.575)	18 ± .30 (.630 ± .012)	
24 mm	20.1 (.791)		11.5 ± 0.10 (.453 ± .004)			50 (1.969)	24 ± .30 (.945 ± .012)	

	P					
Tape Size	4.0 ± 0.10 (.157 ± .004)	8.0 ± 0.10 (.315 ± .004)	12.0 ± 0.10 (.472 ± .004)	16 ± 0.10 (.630 ± .004)	20 ± 0.10 (.787 ± .004)	24 ± 0.10 (.945 ± .004)
8 mm	X					
12 mm	X	X				
16 mm	X	X	X			
24 mm			X	X	X	X

Notes:

1. A_0 B_0 K_0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (.002) min. to 0.50 (.020) max. for 8 mm tape, 0.05 (.002) min. to 0.65 (.026) max. for 12 mm tape, 0.05 (.002) min. to 0.90 (.035) max for 16 mm tape and 0.05 (.002) min. to 1.00 (.039) max. for 24 mm tape and larger. The component cannot rotate more than 20° within the determined cavity, see below.
2. Tape and components shall pass around radius "R" without damage.

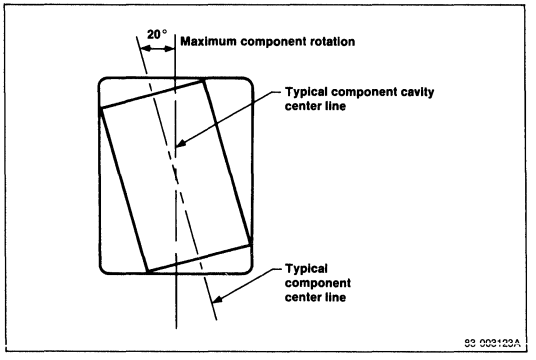


Figure 2. Embossed Carrier Dimensions

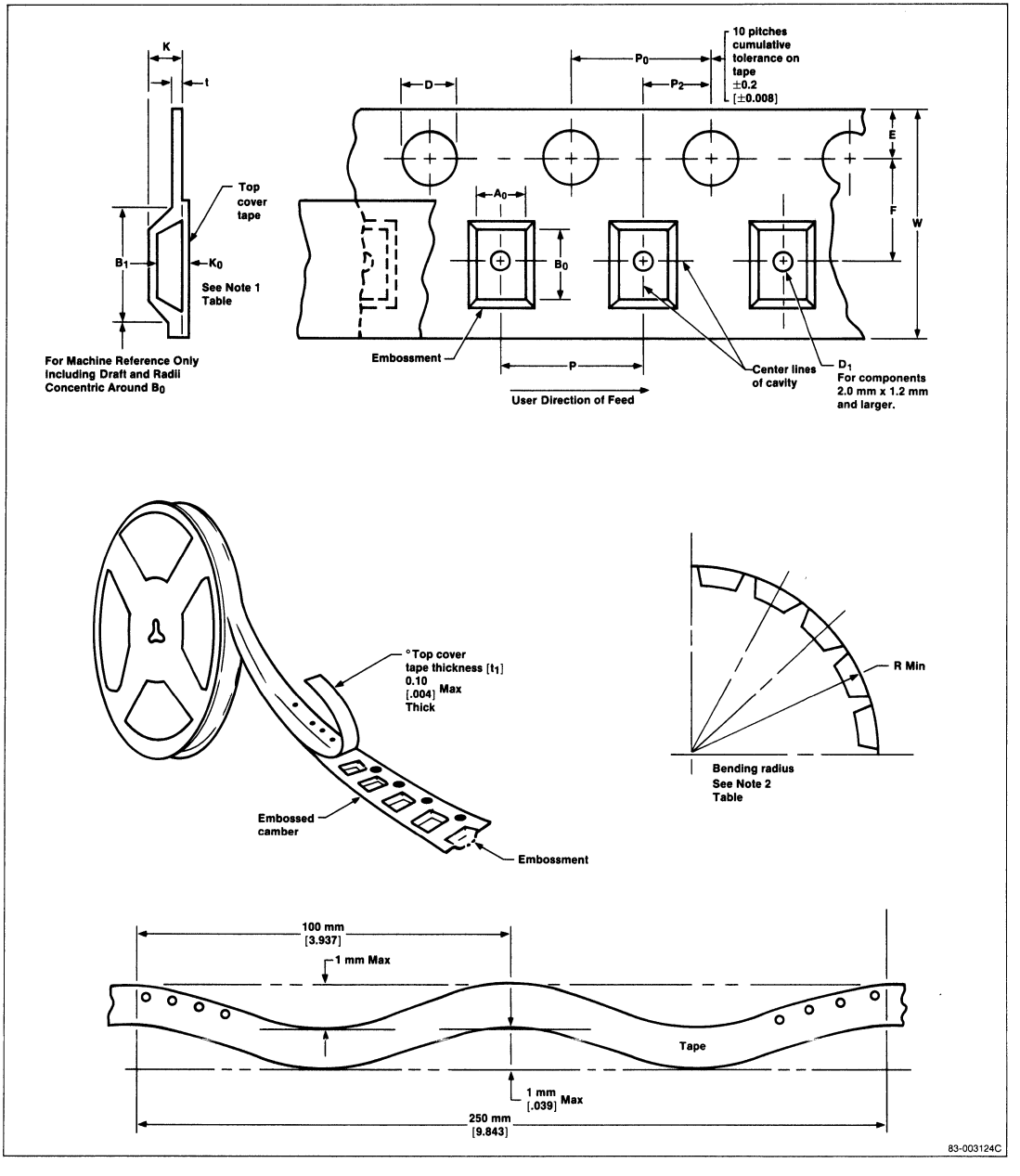


Figure 3. Reel Dimensions

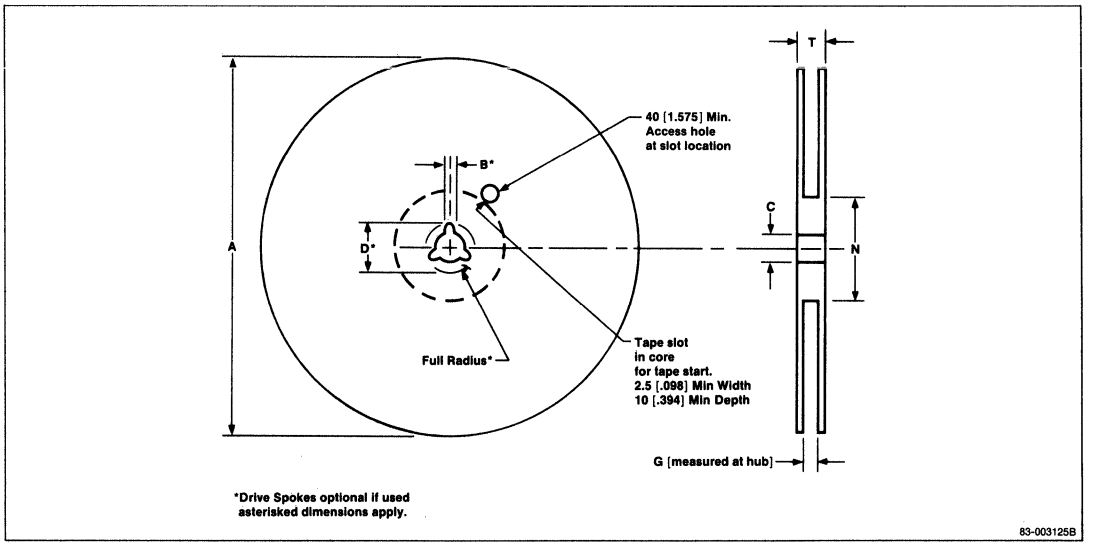


Table 2. Reel Dimensions

Tape Size	A Max.	B Min.	C	D Min.	N Min.	G	T Max.
8 mm	330 (12.992)	1.5 (.059)	13.0 ± 0.20 (.512 ± .008)	20.2 (.795)	50 (.1969)	$8.4^{+1.5}_{-0.0}$ ($.331^{+.008}_{-0.0}$)	14.4 (.567)
12 mm	330 (12.992)					$12.4^{+2.0}_{-0.0}$ ($.488^{+.078}_{-0.0}$)	18.4 (.724)
16 mm	380 (14.173)					$16.4^{+2.0}_{-0.08}$ ($.646^{+.078}_{-0.0}$)	22.4 (.882)
24 mm						$24^{+2.0}_{-0.08}$ ($.961^{+.078}_{-0.00}$)	30.4 (1.197)
32 mm						$32.4^{+2.0}_{-0.0}$ ($1.276^{+.078}_{-0.00}$)	
44 mm						$44.4^{+2.0}_{-0.0}$ ($1.748^{+.078}_{-0.00}$)	
55 mm	609 (23.976)				100 (3.937)	$58.4^{+2.0}_{-0.0}$ ($2.220^{+.078}_{-0.0}$)	

Metric dimensions will govern.
English measurements rounded and for reference only.

Figure 4. Tape End Configurations

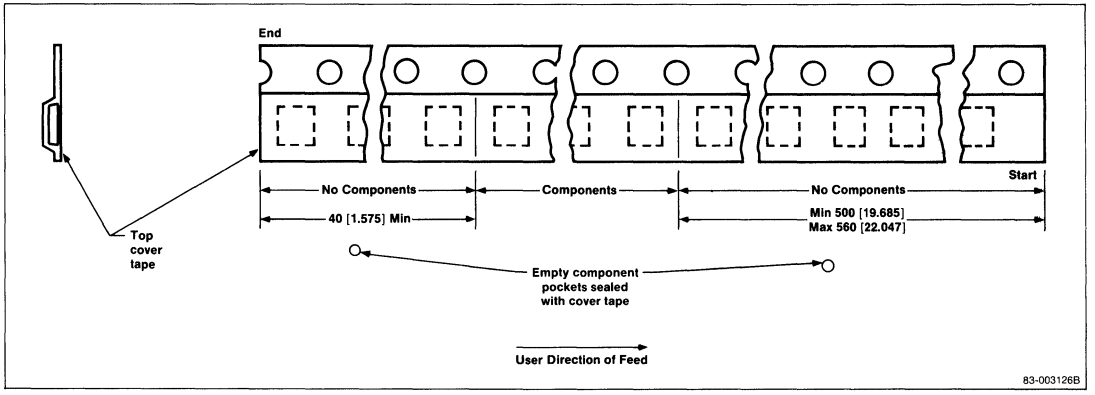


Figure 5. SO-IC Devices

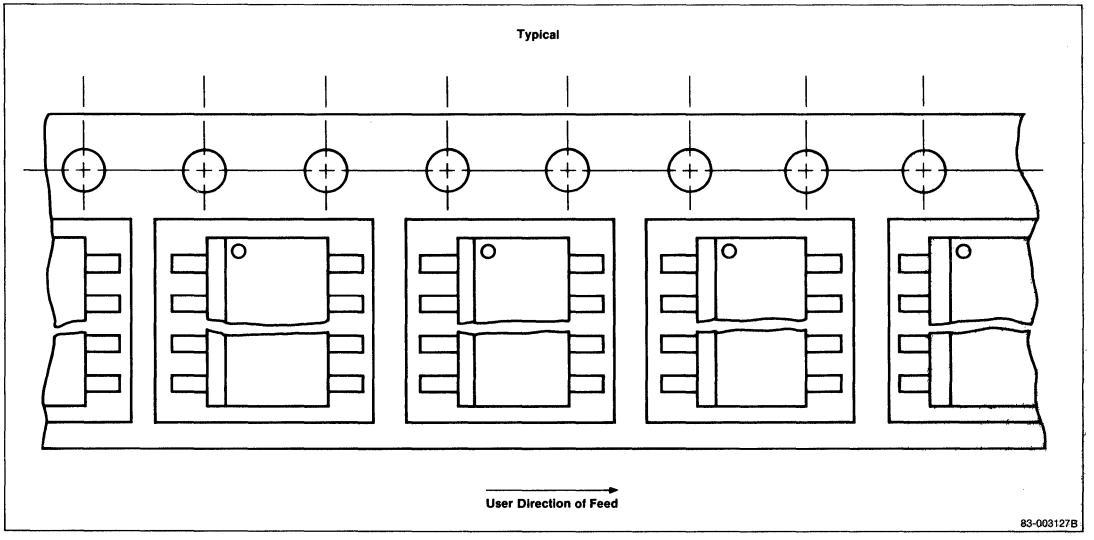


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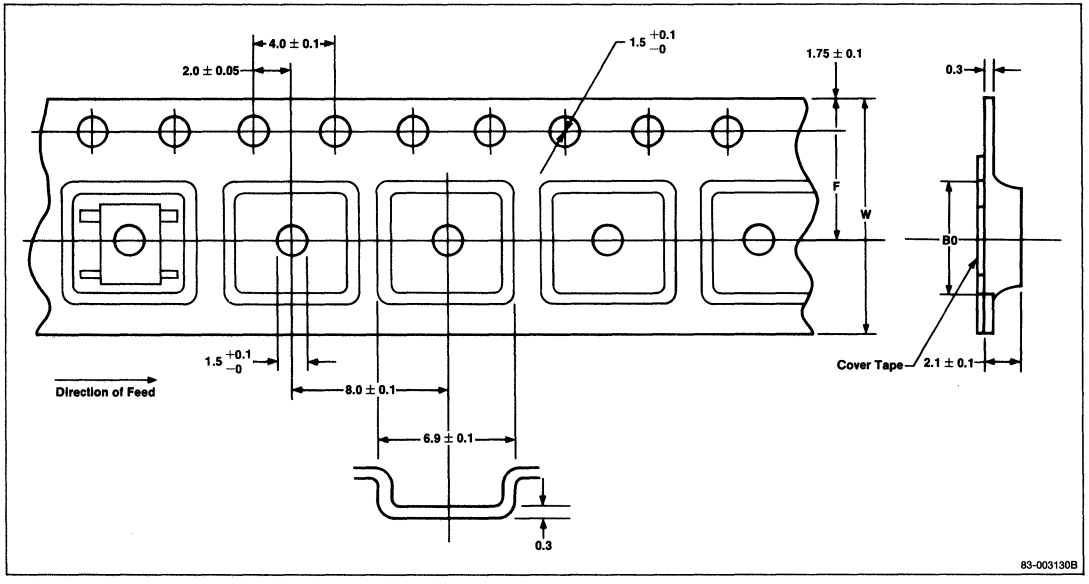
Table 3. SO-IC Devices

Component		Tape Size mm (W)	Part Pitch (P)
SO-IC 225 mil MF	8	12	8
	14	16	8
	16	16	8
SO-IC 375 mil MF	14L	16	12
	16L	16	12
	20L	24	12
	24L	24	12
	28L	24	12
PCC	18	24	12
	20	16	12
	28	24	16
	44	32	24
PCC	52	32	24
	68	44	32
	84	44	36
	100	44	40
	124	56	48

Figure 6. Embossed Carrier Dimensions



Package	B_0	W	F
8p SMF	5.4 ± 0.1	12.0 ± 0.3	5.5 ± 0.1
14, 16p SMF	10.45 ± 0.1	16.0 ± 0.3	7.5 ± 0.1

SMF: 225 mil Miniflat

	8p SMF	14, 16 SMF
W	$12.4^{+2.0}_{-0}$	$16.4^{+2.0}_{-0}$
T	18.4 Max	22.4 Max

SMF: 225 mil Miniflat

Figure 7. Reel Size

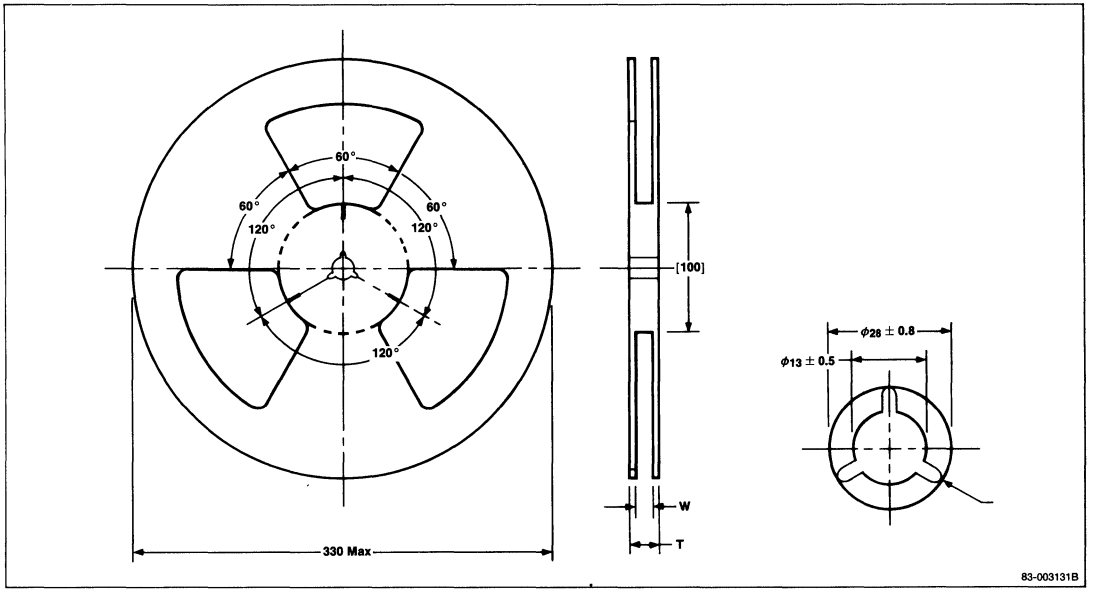
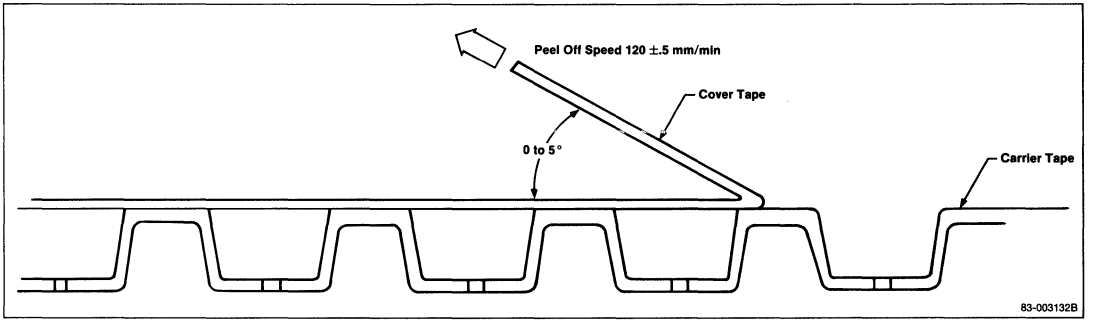


Figure 8. Cover Tape Peel Strength: 40 ± 25 g



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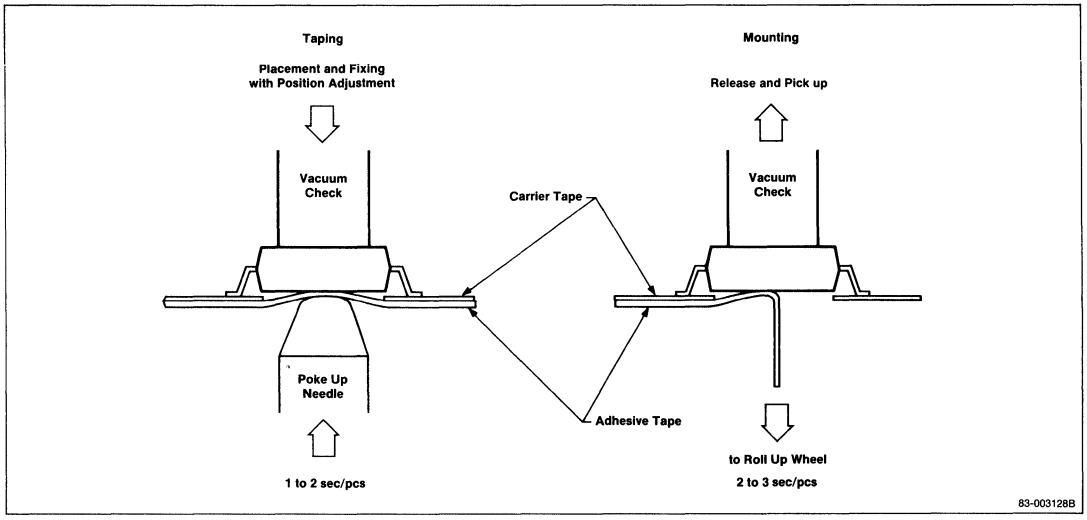
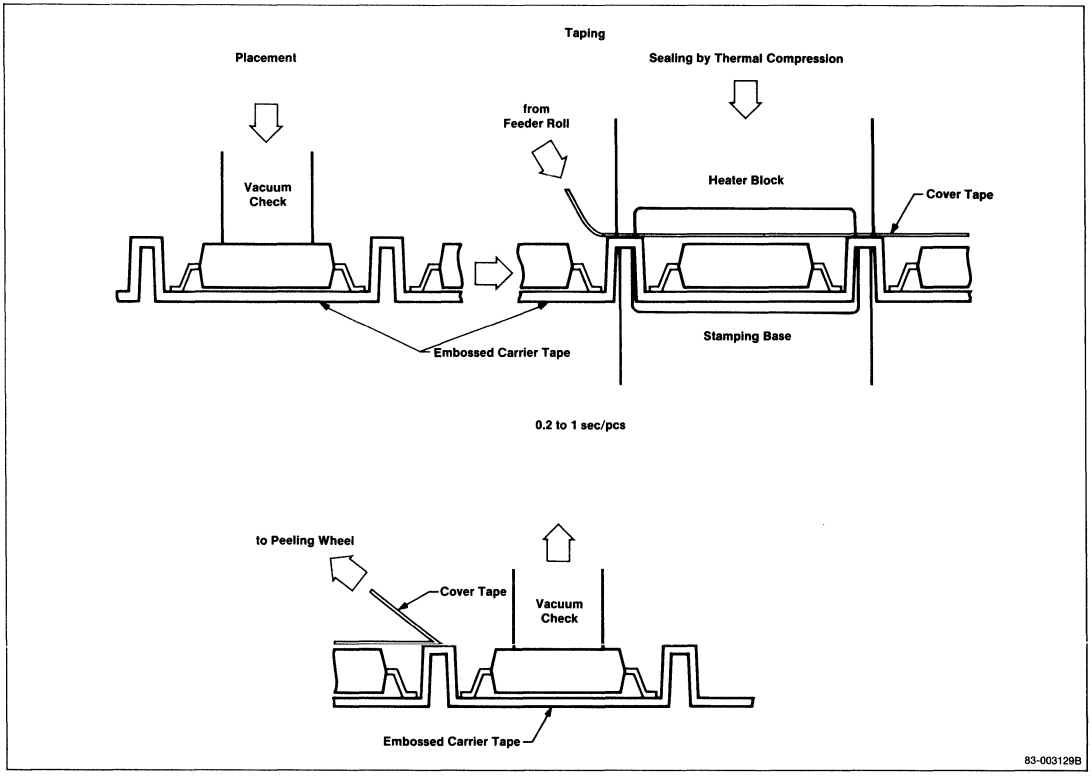

Taping
Placement and Fixing
with Position Adjustment
Vacuum
Check
Carrier Tape
Poke Up
Needle
Adhesive Tape
1 to 2 sec/pcs
Mounting
Release and Pick up
Vacuum
Check
to Roll Up Wheel
2 to 3 sec/pcs
83-003128B


Taping
Placement
Vacuum
Check
from
Feeder Roll
Sealing by Thermal Compression
Heater Block
Cover Tape
Embossed Carrier Tape
Stamping Base
0.2 to 1 sec/pcs
to Peeling Wheel
Cover Tape
Vacuum
Check
Embossed Carrier Tape
83-003129B

Surface Mount Information

Structure

The designation for industrial linear IC (ILIC) in the miniflat package is "G2." Figure 1 shows a cutaway view of the miniflat G2 package. The die (chip) is mounted to the center lead frame island, with bonding pads to the external leads.

The lead frame is made from 42 Alloy with silver (Ag) paste used for die attachment. The body is high-purity molded epoxy for high reliability.

Figure 2 shows the package cross section.

Package Outline

In 1981, the EIAJ (Electronic Industry Association of Japan) set the standards for Surface Mount ICs. They required that devices manufactured in Japan attain higher resistance to environmental factors (humidity, shock, and vibration) than existing Small Outline Integrated Circuit (SOIC) devices. The resulting package is known as the 225-Mil S.O. Specification.

Figure 3 illustrates the difference between the NEC miniflat (G2) and the S.O. type package.

The body or molded portion of the NEC miniflat is 4.4 mm wide compared to 4.0 mm for the S.O. package. The lead bend of the NEC miniflat adds an additional 0.1 mm, for a net difference of approximately 0.5 mm in overall footprint width (miniflat vs. SOIC). All other dimensions (such as lead pitch, length, and spacing) are the same.

The larger package size of the NEC miniflat allows a larger die to be mounted in 8- and 14-pin packages, (e.g. BIFET op amp), which increases the variety of circuits available in the G2 package. See Package Information Section for the outline dimensions of 8-pin and 14-pin G2 packages.

Figure 1. Internal Structure (8-Pin Type)

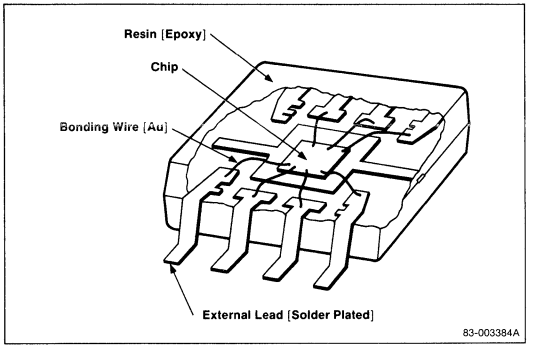


Figure 2. Cross Section of a Miniflat IC

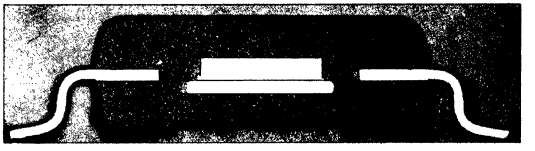
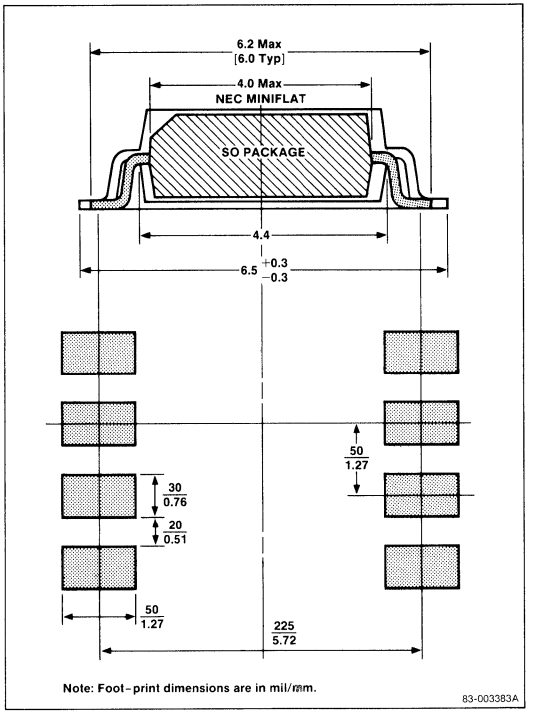


Figure 3. Compatible Footprint Pattern for NEC Miniflat IC and SOIC



Handling Techniques

To work with the NEC miniflat IC without jeopardizing the quality and reliabilty, it is necessary to exercise more care than when handling standard DIP ICs.

Environmental conditions and handling precautions for the NEC miniflat IC family are described below.

Circuit Design

The electrical characteristics of the NEC miniflat IC are guaranteed the same as those of standard DIP ICs.

Since heat radiation is improved when the IC is mounted on the substrate, power dissipation P_T can be changed in actual use. However, the degree of change

largely depends on the method of mounting (size of substrate, coating method, etc). Therefore, full evaluation of the mounted board should be made in advance.

Total Power Dissipation and Thermal Resistance

Figures 4 and 5 show the total power dissipation characteristics of the NEC miniflat IC family.

As shown in the figures, thermal resistance for a single element is approximately 180°C/W for the 14-pin IC, and approximately 220°C/W for the 8-pin IC.

When mounted on a hybrid IC or PW-board, the heat radiation through the leads is increased. With resin coating, the heat radiation through the resin to the environment is further increased. As a result, the thermal resistance in the mounted state is much lower.

It is suggested that the heat dissipation in actual finished mountings be fully analyzed prior to production.

Figure 4. P_T-T_j Characteristic (8-Pin Type)

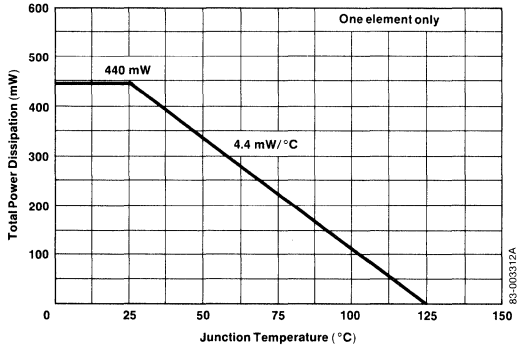
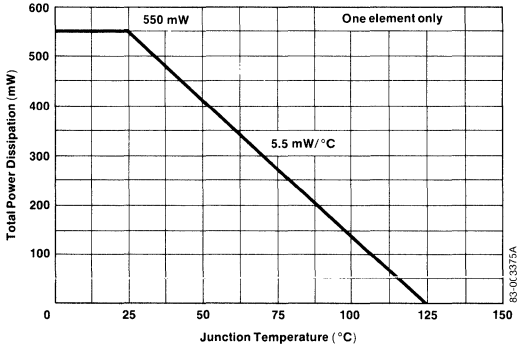


Figure 5. P_T-T_j Characteristic (14-Pin Type)



Soldering and Flux Temperature

Exposure to high temperatures over time should be carefully monitored to insure prolonged reliability. As An Absolute Maximum Rating, exposure to the following must not exceed 260°C for 10 seconds.

- Solder dipping
- Soldering iron
- High-temperature atmosphere

Rosin flux (pine resin) is recommended as soldering flux.

NOTE: Avoid flux containing chlorine. Residual chlorine after cleaning may affect reliability.

Cleaning

Flux should be thoroughly removed after soldering. Alcohol, Chlorocene, and Freon are all acceptable solvents; however, prolonged immersion in these solvents may remove printed markings.

Ultrasonic cleaning can also be applied if other components mounted on the same board can withstand it.

Protection Against Humidity

Being super-miniaturized and employing a thinner plastic than standard DIP ICs, the miniflat IC has shorter leakage paths and requires much more protection against humidity.

Generally, anti-humidity protection is provided by resin coating after mounting on board. Examples of the process are described below.

- When sealed in an airtight package, no precoating is necessary.
- When sealed with resin, a buffer coating may be required as the resin contraction may exert stress on ICs when sealing. Sufficient evaluation should be made on the actual board.
  For buffer coating, the use of resin with a certain degree of viscosity is suggested.

Please consult the resin manufacturers for appropriate encapsulation resin and coating materials.

NEC

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