NEC

MOS INTEGRATED CIRCUIT
μPD703000, 703001

V851™
32-/16-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD703000 is a product in the V850 family™ of 32-bit single-chip microcontrollers for real-time control applications. It integrates a 32-bit CPU, ROM, RAM, interrupt controller, real-time pulse unit, and serial interface on a single chip.

The μPD703001 is a ROM-less model of the μPD703000.

The functions are described in detail in the following manuals. Be sure to read these manuals when designing your system.

V851 User's Manual - Hardware   : U10935E

V850 Family User's Manual - Architecture   : U10243E

FEATURES

- Number of instructions: 74
- Minimum instruction execution time: 30 ns (at 33 MHz)
- General-purpose register: 32 bits x 32
- Instruction set ideal for control application
- Internal memory   ROM : 32K bytes (μPD703000)
                     RAM : 1K bytes (μPD703000, 703001)
- High-performance interrupt controller
- Real-time pulse unit ideal for control
- Powerful serial interface (dedicated baud rate generator)
- Clock generator
- Power save function

APPLICATION FIELD

- System control fields using servo motor (PPCs, printers, and NC machine tools)
- Other control fields requiring high response speed (engine control, etc.)

The μPD703000 is treated as the representative model in this document.

The information in this document is subject to change without notice.

The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package	Maximum Operating Frequency (MHz)	Internal ROM
μPD703000GC-25-xxx-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)	25	32K bytes
μPD703000GC-33-xxx-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)	33	32K bytes
μPD703001GC-25-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)	25	None
μPD703001GC-33-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)	33	None

Remark xxx indicates a ROM code suffix.

PIN CONFIGURATION

100-pin plastic QFP (fine pitch) (14 × 14 mm)
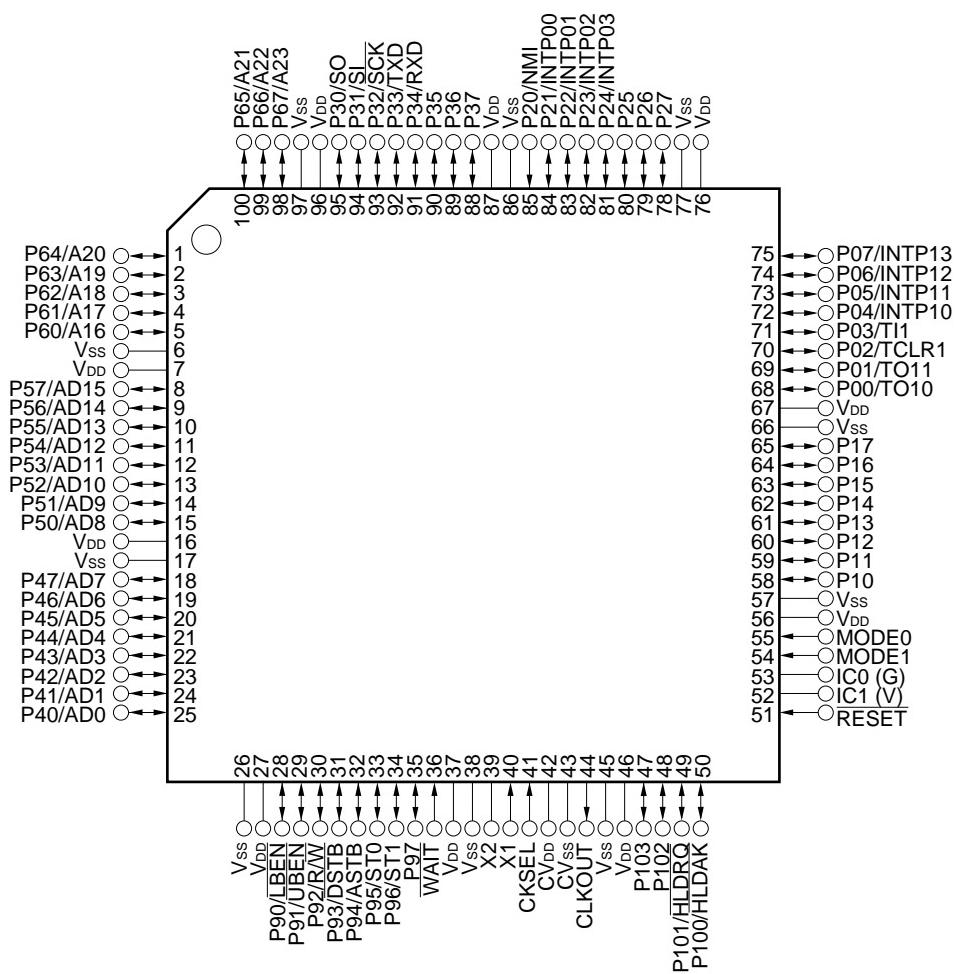
Caution   ( ) **indicates the processing of the pins not used in the normal operation mode.**
G : Directly connect this pin to V$_{SS}$.
V : Directly connect this pin to V$_{DD}$.

P00-P07	: Port0	A16-A23	: Address Bus
P10-P17	: Port1	$\overline{\text{LBEN}}$	: Lower Byte Enable
P20-P27	: Port2	$\overline{\text{UBEN}}$	: Upper Byte Enable
P30-P37	: Port3	R/$\overline{\text{W}}$	: Read/Write Status
P40-P47	: Port4	$\overline{\text{DSTB}}$	: Data Strobe
P50-P57	: Port5	ASTB	: Address Strobe
P60-P67	: Port6	ST0, ST1	: Status
P90-P97	: Port9	$\overline{\text{HLDAK}}$	: Hold Acknowledge
P100-P103	: Port10	$\overline{\text{HLDRQ}}$	: Hold Request
TO10, TO11	: Timer Output	CLKOUT	: Clock Output
TCLR1	: Timer Clear	CKSEL	: Clock Select
TI1	: Timer Input	$\overline{\text{WAIT}}$	: Wait
INTP00-INTP03,		MODE0, MODE1	: Mode
INTP10-INTP13	: Interrupt Request From Peripherals	$\overline{\text{RESET}}$	: Reset
NMI	: Non-maskable Interrupt Request	X1, X2	: Crystal
SO	: Serial Output	CV_{DD}	: Power Supply for Clock Generator
SI	: Serial Input	CV_{SS}	: Ground for Clock Generator
$\overline{\text{SCK}}$	: Serial Clock	V_{DD}	: Power Supply
TXD	: Transmit Data	V_{SS}	: Ground
RXD	: Receive Data	IC0, IC1	: Internally Connected
AD0-AD15	: Address/Data Bus		

FUNCTION BLOCK DIAGRAM

Note Not provided to μPD703001
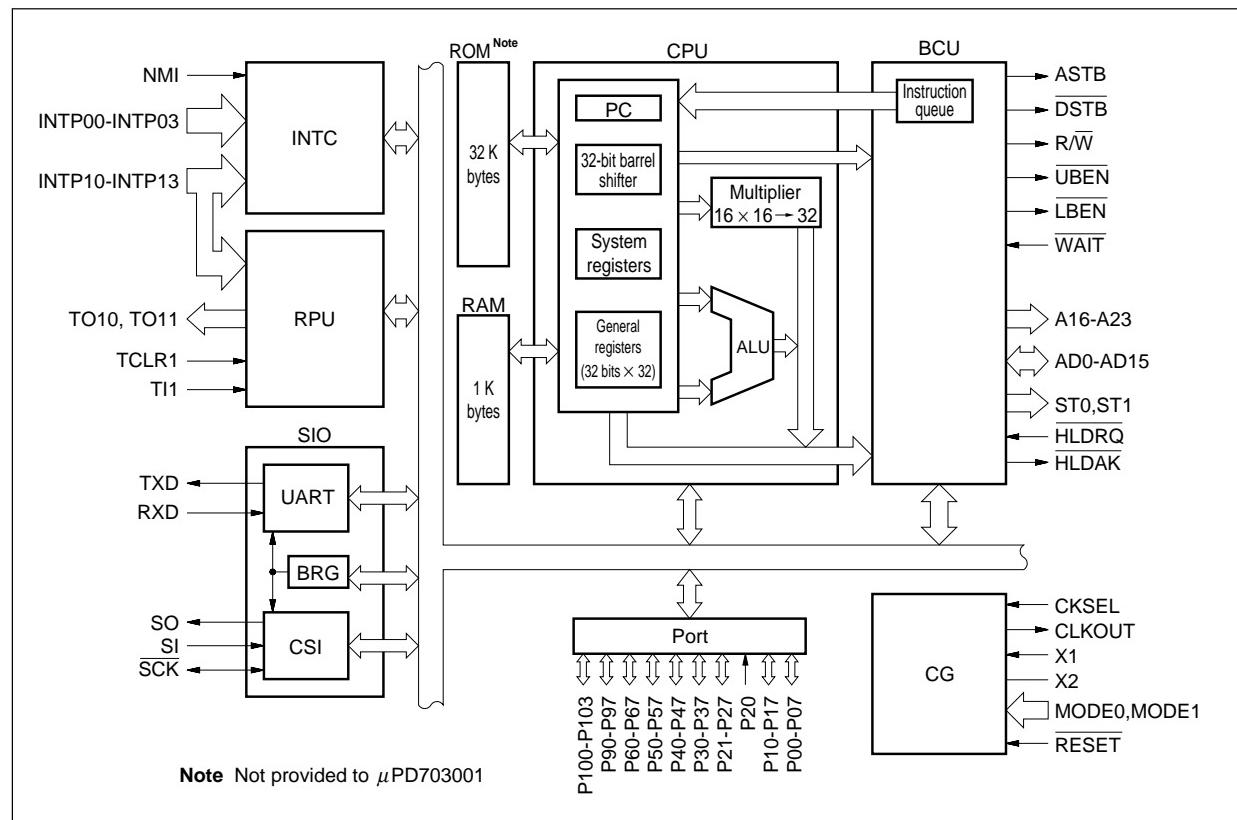
TABLE OF CONTENTS

1. LIST OF PIN FUNCTIONS

1.1 Port Pins

(1/2)

Pin Name	I/O	Function	Shared Pin
P00	I/O	Port 0	TO10
P01		8-bit input/output port	TO11
P02		Input/output specifiable bit-wise	TCLR1
P03			TI1
P04			INTP10
P05			INTP11
P06			INTP12
P07			INTP13
P10-P17	I/O	Port 1 8-bit input/output port Input/output specifiable bit-wise	—
P20	Input	Port 2	NMI
P21	I/O	P20 is a dedicated input port.	INTP00
P22		When a valid edge is input, this pin operates as an NMI input.	INTP01
P23		Bit 0 of P2 register indicates the NMI input status.	INTP02
P24		P21 to P27 are 7-bit input/output ports.	INTP03
P25-27		Input/output specifiable bit-wise	—
P30	I/O	Port 3	SO
P31		8-bit input/output port	SI
P32		Input/output specifiable bit-wise	$\overline{\text{SCK}}$
P33			TXD
P34			RXD
P35-37			—
P40-P47	I/O	Port 4 8-bit input/output port Input/output specifiable bit-wise	AD0-AD7
P50-P57	I/O	Port 5 8-bit input/output port Input/output specifiable bit-wise	AD8-AD15
P60-P67	I/O	Port 6 8-bit input/output port Input/output specifiable bit-wise	A16-A23

(2/2)

Pin Name	I/O	Function	Shared Pin
P90	I/O	Port 9	$\overline{\text{LBEN}}$
P91		8-bit input/output port	$\overline{\text{UBEN}}$
P92		Input/output specifiable bit-wise	R/$\overline{\text{W}}$
P93			$\overline{\text{DSTB}}$
P94			ASTB
P95			ST0
P96			ST1
P97			—
P100	I/O	Port 10	$\overline{\text{HLDAK}}$
P101		4-bit input/output port	$\overline{\text{HLDRQ}}$
P102		Input/output specifiable bit-wise	—
P103			—

1.2 Pins Other Than Port Pins

(1/2)

Pin Name	I/O	Function	Shared Pin
TO10	Output	Pulse signal of timer 1	P00
TO11			P01
TCLR1	Input	Timer 1 external clear signal	P02
TI1		Timer 1 external count clock	P03
INTP10	Input	External maskable interrupt request, or timer 1 external capture trigger	P04
INTP11			P05
INTP12			P06
INTP13			P07
NMI	Input	Non-maskable interrupt request	P20
INTP00	Input	External maskable interrupt request	P21
INTP01			P22
INTP02			P23
INTP03			P24
SO	Output	CSI serial data transmission	P30
SI	Input	CSI serial data reception	P31
$\overline{\text{SCK}}$	I/O	CSI serial clock	P32
TXD	Output	UART serial data transmission	P33
RXD	Input	UART serial data reception	P34
AD0-AD7	I/O	16-bit multiplexed address/data bus to extend external memory	P40-P47
AD8-AD15			P50-P57
A16-A23	Output	Higher address bus to extend external memory	P60-P67
$\overline{\text{LBEN}}$	Output	External data bus lower byte enable signal	P90
$\overline{\text{UBEN}}$		External data bus higher byte enable signal	P91
R/$\overline{\text{W}}$		External read/write status	P92
$\overline{\text{DSTB}}$		External data strobe signal	P93
ASTB		External address strobe signal	P94
ST0		External bus cycle status	P95
ST1			P96
$\overline{\text{HLDAK}}$	Output	Bus hold acknowledge	P100
$\overline{\text{HLDRQ}}$	Input	Bus hold request	P101
CLKOUT	Output	System clock	—
CKSEL	Input	Clock generator operation mode specification	—
$\overline{\text{WAIT}}$	Input	Bus cycle wait insertion control signal	—
MODE0,MODE1	Input	Operation mode specification	—
$\overline{\text{RESET}}$	Input	System reset	—
X1	Input	Connect resonator for system clock. Input external clock to X1.	—
X2	—		—
CV$_{DD}$	—	Positive power for internal clock generator	—
CV$_{SS}$	—	Ground potential for internal clock generator	—

(2/2)

Pin Name	I/O	Function	Shared Pin
V_{DD}	—	Positive power supply	—
V_{SS}	—	Ground potential	—
IC0, IC1	—	Internally connected	—

### 1.3 I/O Circuits of Pins and Recommended Connections of Unused Pins

Table 1-1 shows the I/O circuit types of the respective pins in the normal operation mode and recommended connections of unused pins. Figure 1-1 shows the respective circuit types partially simplified.

When connecting a pin to V_{DD} or V_{SS} via resistor, use of a resistor of 3 to 10 kΩ is recommended.

Table 1-1. I/O Circuit Types of Respective Pins and Recommended Connections of Unused Pins

Pin Name	I/O Circuit Type	Recommended Connections
P00/TO10,P01/TO11	5	Input: Individually connect to V_{DD} or V_{SS} via resistor
P02/TCLR1,P03/TI1, P04/INTP10-P07/INTP13	8	Output: Open
P10-P17	5	
P20/NMI	2	Directly connect to V_{SS}
P21/INTP00-P24/INTP03	8	Input: Individually connect to V_{DD} or V_{SS} via resistor
P25	5	Output: Open
P26,P27	8	
P30/SO	5	
P31/SI,P32/$\overline{SCK}$	8	
P33/TXD,P34/RXD,P35	5	
P36,P37	8	
P40/AD0-P47/AD7	5	
P50/AD8-P57/AD15		
P60/A16-P67/A23		
P90/$\overline{LBEN}$		
P91/$\overline{UBEN}$		
P92/R/$\overline{W}$		
P93/$\overline{DSTB}$		
P94/ASTB		
P95/ST0,P96/ST1		
P97		
P100/$\overline{HLDAK}$		
P101/$\overline{HLDRQ}$		
P102		
P103		
CLKOUT	3	Open
CKSEL	2	–
$\overline{WAIT}$	1	Directly connect to V_{DD}
MODE0,MODE1	2	–
$\overline{RESET}$		
IC0	–	Directly connect to V_{SS}
IC1	–	Directly connect to V_{DD}

Figure 1-1. I/O Circuits of Pins

Type 1

Type 5

Type 2

Schmitt trigger input with hysteresis characteristics

Type 8

Type 3
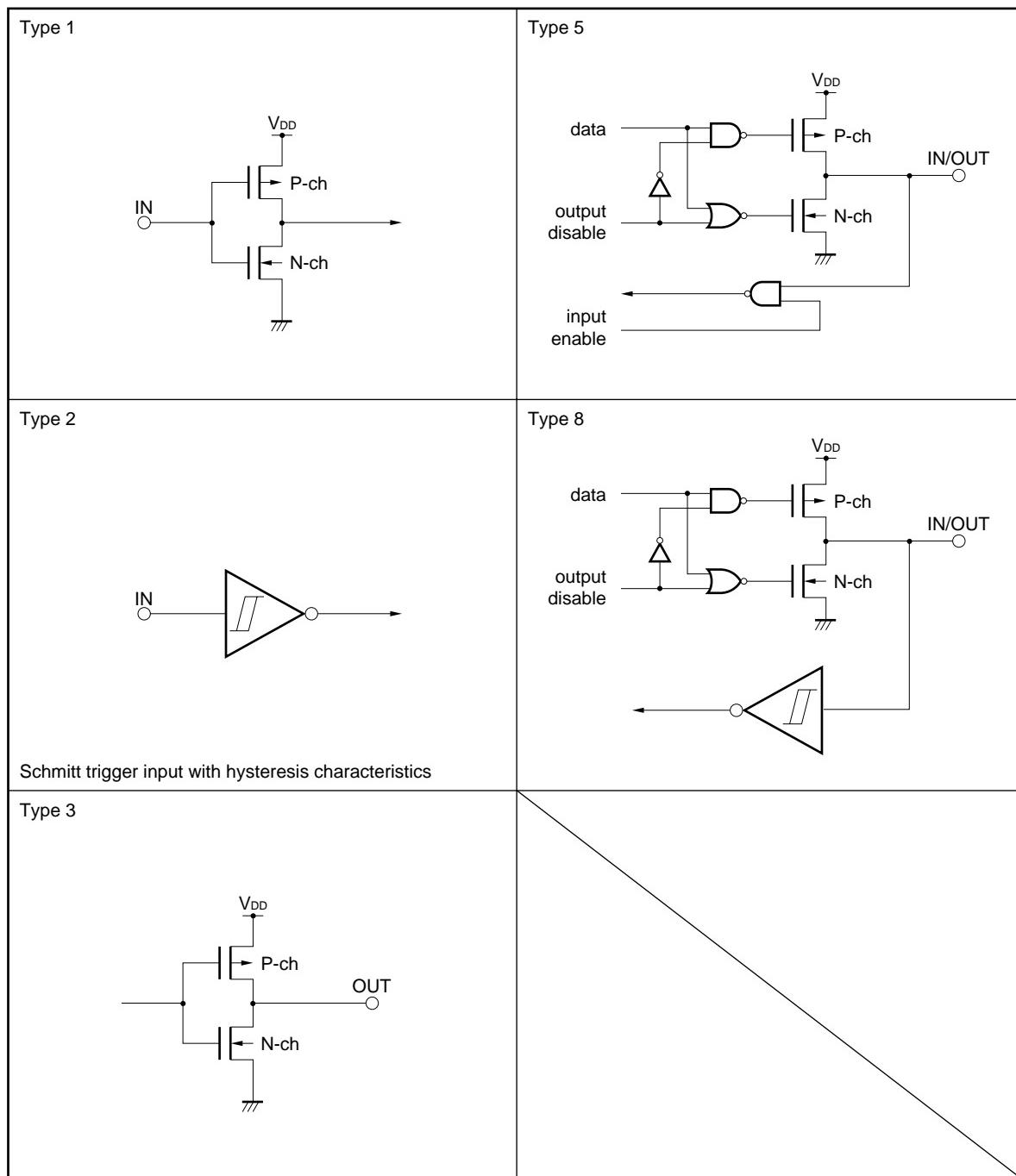
2. FUNCTION BLOCKS

2.1 Internal Units

2.1.1 CPU

Most instructions, such as address calculation, arithmetic and logic operation, and data transfer, are executed in one clock cycle under control of 5-stage pipeline.

The CPU also includes dedicated hardware such as a multiplier (16 by 16) and a 32-bit barrel shifter, aiming at processing complex instructions at high speeds.

In addition, the CPU can access internal ROM (32 KB) and RAM (1 KB) in one clock cycle.

2.1.2 Bus control unit (BCU)

★ The BCU initiates necessary external bus cycles based on the physical address given by the CPU. When an instruction fetch is executed from external memory area, if no bus cycle initiation is requested by the CPU, the BCU creates a prefetch address to prefetch an instruction code. The prefetched instruction code is taken into the internal instruction queue.

2.1.3 ROM

The ROM has a capacity of 32 KB and is mapped from the address 00000000H. Access to the ROM is enabled/disabled by setting the MODE0 and MODE1 pins.

The CPU can access any address of the ROM in one clock cycle (to fetch an instruction).

2.1.4 RAM

This RAM has a capacity of 1 KB and is mapped from address FFFFE000H. The CPU can access any address of the RAM in one clock cycle (to access data).

2.1.5 Port

The μPD703000 is provided with a total of 68 input/output port pins (of which one is an input port pin), or ports 0 through 10. These port pins can be used as the control pins.

2.1.6 Interrupt controller

The interrupt controller controls various interrupt requests (NMI, INTP00-INTP03, and INTP10-INTP13) issued by peripheral hardware or external devices. Up to eight levels of interrupt priority can be individually specified for each interrupt request. In addition, multiplexed processing control can be performed.

2.1.7 Clock generator

The clock generator generates a CPU operating clock whose frequency is 5 times as high as (with the internal PLL) or half (without the internal PLL) the frequency of the resonator connected across the X1 and X2 pins. Instead of connecting a resonator, a clock signal can be input from off-chip.

2.1.8 Realtime pulse unit (RPU)

The RPU which includes a 16-bit timer/event counter and a 16-bit interval timer, measures pulse intervals and pulse frequency, and outputs programmable pulses.

2.1.9 Serial interface

   The serial interface includes one channel of UART (asynchronous serial interface) and one channel of CSI (clocked serial interface).

   The UART transfers data with the TXD and RXD pins. The baud rate is generated by an on-chip dedicated baud rate generator. The CSI transfers data with the SO, SI, and $\overline{\text{SCK}}$ pins. The baud rate can be generated from an on-chip dedicated baud rate generator, or supplied from off-chip.

3. CPU FUNCTION

The CPU of the μPD703000 is based on the RISC architecture and executes almost all the instructions in one clock cycle, using a 5-stage pipeline.

3.1 Features
- Minimum instruction execution time: 30 ns (internal 33 MHz)
- Address space: 16-MB linear
- General registers: 32 bits x 32
- Internal 32-bit architecture
- Five-stage pipeline control
- Multiplication/division instruction
- Saturated operation instruction
- 32-bit shift instruction: 1 clock
- Long/short format
- Internal memory
  - ROM: 32K bytes
  - RAM: 1K bytes
- Bit manipulation instructions: 4 types
  - Set
  - Clear
  - Not
  - Test

4. BUS CONTROL FUNCTION

4.1 Features
- External device connectable with port pins
- Wait function
  - Programmable wait function inserting up to 3 states per 2 blocks
  - External wait function effected by $\overline{\text{WAIT}}$ pin
- Idle state inserting function
- Bus arbitration function
- Bus hold function

5. INTERRUPT/EXCEPTION HANDLING

5.1 Features

- Interrupt
  - Non-maskable : 1 source
  - Maskable : 14 sources
  - 8-level programmable priority control
  - Multiplexed processing control according to priority
  - Masking each maskable interrupt request
  - Valid edge specification for external interrupt request
- Exception
  - Software exception : 32 sources
  - Exception trap : 1 source (illegal instruction code exception)

5.2 Configuration
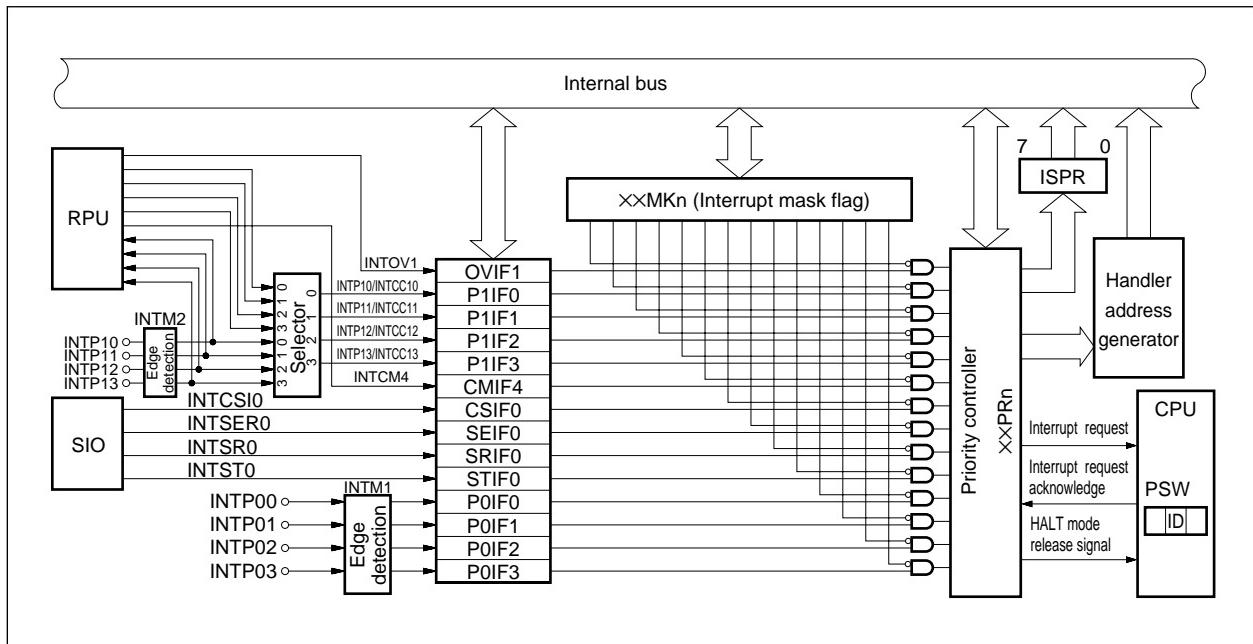
Table 5-1. Interrupts

Type	Class	Interrupt/Exception Sources				Default Priority	Exception Code	Handler Address	Restore PC
		Name	Control Register	Generation Sources	Generating Unit				
Reset	Interrupt	RESET	—	Reset input	—	—	0000H	00000000H	Undefined
Non-maskable	Interrupt	NMI	—	NMI input	—	—	0010H	00000010H	next PC
Software exception	Exception	TRAP0n**Note**	—	TRAP instruction	—	—	004n**Note**H	00000040H	next PC
	Exception	TRAP1n**Note**	—	TRAP instruction	—	—	005n**Note**H	00000050H	next PC
Exception trap	Exception	ILGOP	—	Illegal instruction code	—	—	0060H	00000060H	next PC
Maskable	Interrupt	INTOV1	OVIC1	Timer 1 overflow	RPU	0	0080H	00000080H	next PC
	Interrupt	INTP10/INTCC10	P1IC0	Match of INTP10 & CC10	Pin/RPU	1	0090H	00000090H	next PC
	Interrupt	INTP11/INTCC11	P1IC1	Match of INTP11 & CC11	Pin/RPU	2	00A0H	000000A0H	next PC
	Interrupt	INTP12/INTCC12	P1IC2	Match of INTP12 & CC12	Pin/RPU	3	00B0H	000000B0H	next PC
	Interrupt	INTP13/INTCC13	P1IC3	Match of INTP13 & CC13	Pin/RPU	4	00C0H	000000C0H	next PC
	Interrupt	INTCM4	CMIC4	Match of CM4	RPU	5	00D0H	000000D0H	next PC
	Interrupt	INTCSI0	CSIC0	CSI0 transmit/receive completion	SIO	6	00E0H	000000E0H	next PC
	Interrupt	INTSER0	SEIC0	UART0 receive error	SIO	7	00F0H	000000F0H	next PC
	Interrupt	INTSR0	SRIC0	UART0 receive completion	SIO	8	0100H	00000100H	next PC
	Interrupt	INTST0	STIC0	UART0 transmit completion	SIO	9	0110H	00000110H	next PC
	Interrupt	INTP00	P0IC0	INTP00 pin	Pin	10	0120H	00000120H	next PC
	Interrupt	INTP01	P0IC1	INTP01 pin	Pin	11	0130H	00000130H	next PC
	Interrupt	INTP02	P0IC2	INTP02 pin	Pin	12	0140H	00000140H	next PC
	Interrupt	INTP03	P0IC3	INTP03 pin	Pin	13	0150H	00000150H	next PC

Note The "n" in the "Software exception " rows is a value from 0 to FH.

**Remarks 1.** Default priority: Priority used when two or maskable interrupt requests are simultaneously generated. 0 indicates the highest priority.

Restore PC: PC value saved to EIPC or FEPC when interrupt/exception processing is started. However, the restore PC value saved if an interrupt is accepted while the DIVH (division) instruction is being executed is the PC value of the current instruction (DIVH).

2. The execution address of an illegal instruction when an illegal instruction code exception occurs can be calculated as (restore PC − 4).

6. CLOCK GENERATOR

6.1 Features
- Multiply function by PLL clock synthesizer ($f_{XX} = \frac{1}{5} \times \phi$)
- Direct mode directly to input external clock
- Power save mode
  - HALT mode
  - IDLE mode
  - Software STOP mode
- Clock output inhibit function

6.2 Configuration

f_{VCO} : VCO oscillation frequency (=10f_{XX})
ϕ : Internal system clock frequency (=1/2f_{VCO} : in PLL mode)
Internal system clock frequency (=1/2f_{XX} : in direct mode)
OSC : Oscillator (supported in PLL mode only)
PFC : Phase Frequency Comparator
SCF : Switched Capacitor Filter
VCO : Voltage Controlled Oscillator
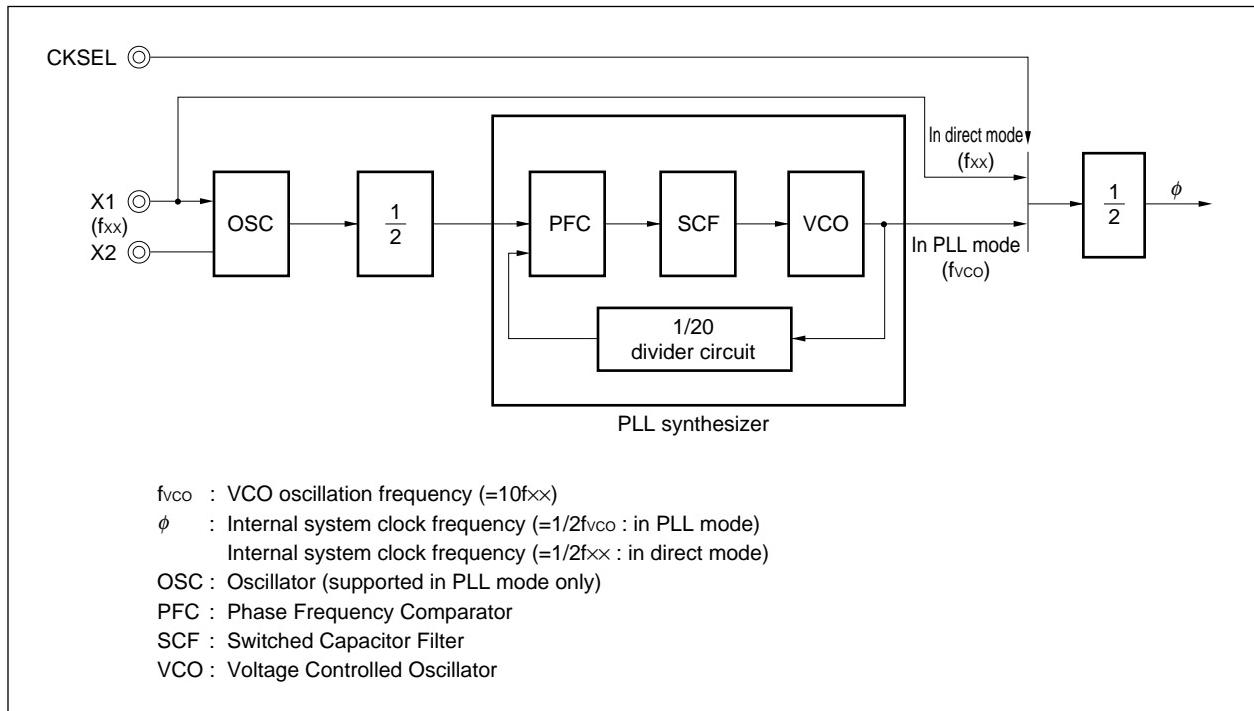
## 7. TIMER/COUNTER FUNCTION (Real Time Pulse Unit)

7.1 Features

- Pulse interval and frequency measurement and output of programmable pulse
  - 16-bit measurement possible
  - Pulse can be generated in various shapes (interval pulse, one-shot pulse)
- Timer 1
  - 16-bit timer/event counter
  - Sources of count clock: 2 types (divided system clock or external pulse input)
  - Capture/compare registers: 4
  - Count clear pin: TCLR1
  - Interrupt sources: 5
  - External pulse output: 2
- Timer 4
  - 16-bit interval timer
  - Count clock selected from divided system clock
  - Compare register: 1
  - Interrupt source: 1

7.2 Configuration

(1) Timer 1 (16-bit timer/event counter)

Notes 1. Internal count clock
2. External count clock
3. Gives priority to reset

Remark ϕ indicates the system clock.

(2) Timer 4 (16-bit interval timer)

Note Internal count clock

Remark ϕ indicates the system clock.
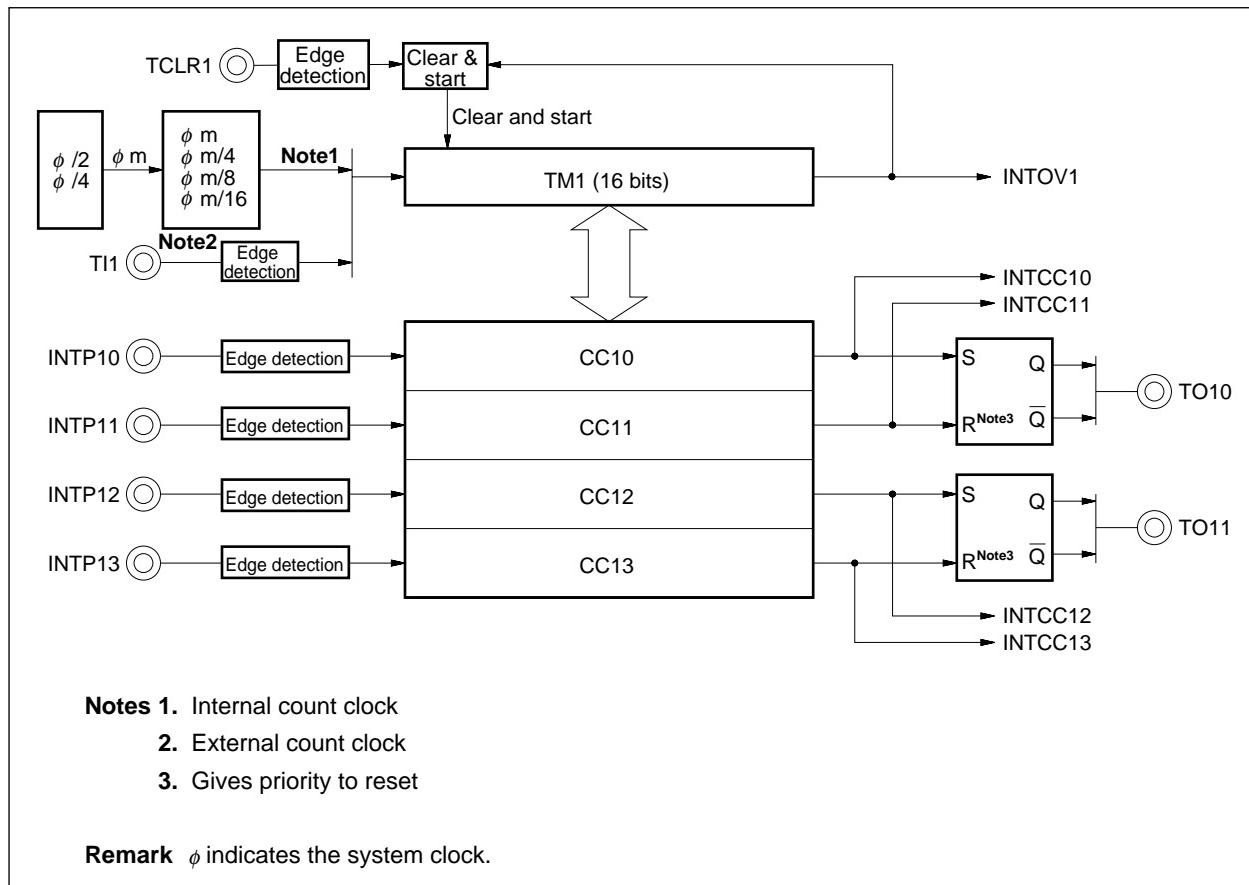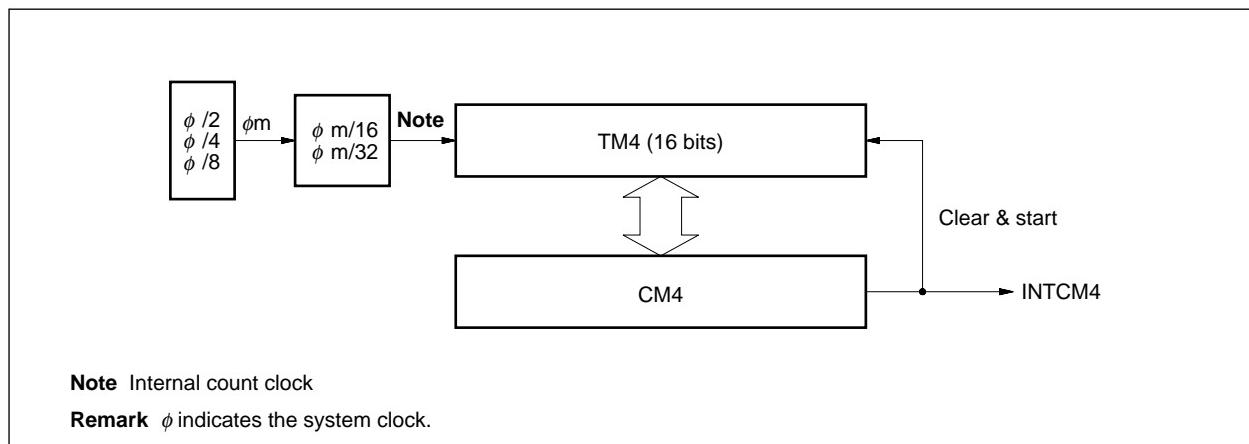
8. SERIAL INTERFACE FUNCTION (SIO)

8.1 Features

The μPD703000 is provided with the following two types of interface methods as serial interface functions, each of which has one channel:

    (1) Asynchronous serial interface (UART)
    (2) Clocked serial interface (CSI)

8.2 Asynchronous Serial Interface (UART)

8.2.1 Features

- Transfer rate: 150 bps to 76800 bps (system clock: 33 MHz)
- Full-duplex communication
- 2-pin configuration
  TXD: Transmit data output pin
  RXD: Receive data input pin
- Receive error detection function
  - Parity error
  - Framing error
  - Overrun error
- Three interrupt sources
  - Receive error interrupt (INTSER0)
  - Reception completion interrupt (INTSR0)
  - Transmission interrupt (INTST0)
- Character length of transmission/reception data is specified by ASIM0 and ASIM1 registers.
- Character length : 7, 8 bits
  9 bits (with extended bit appended)
- Parity function : odd, even, 0, none
- Transmission stop bit: 1, 2 bits
- Baud rate generator

8.2.2 Configuration
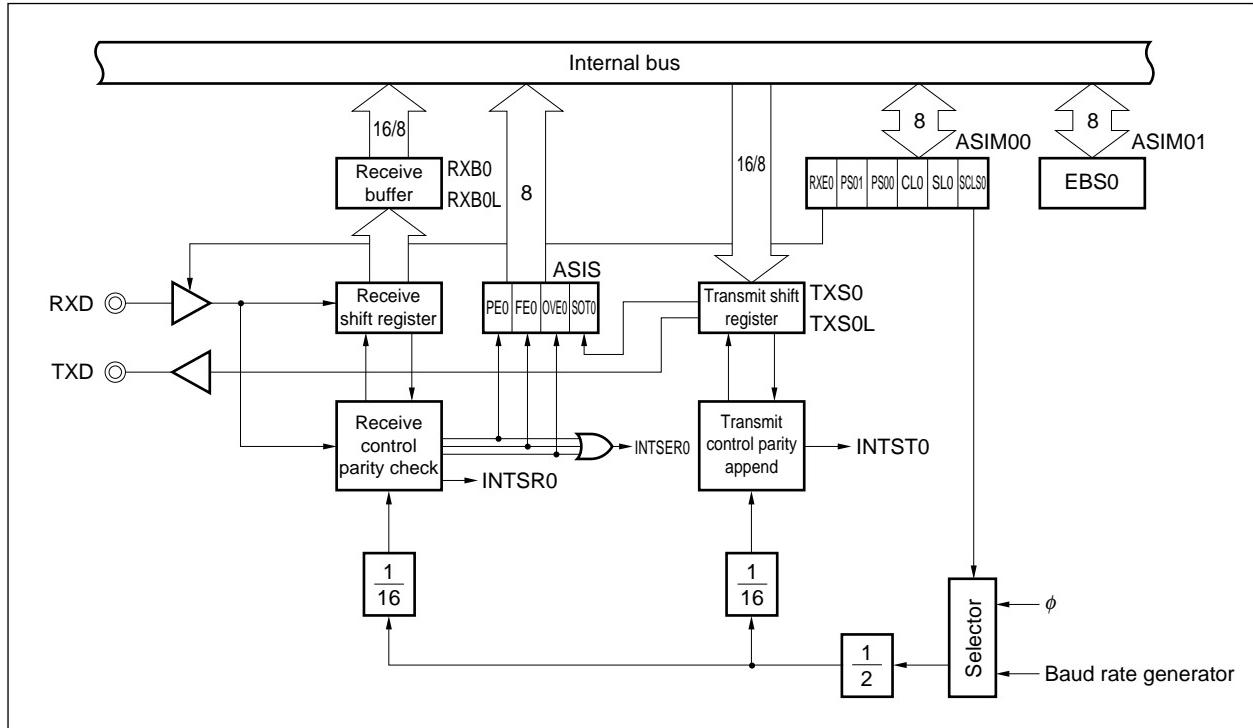
8.3 Clocked Serial Interface (CSI)

8.3.1 Features
- High-speed transfer rate
  8.25 Mbps MAX. (system clock: 33 MHz)
- Half-duplex communication
- Data length of 8 bits
- Selection of external or internal clock
- Three pins used
  SO : Serial data output pin
  SI : Serial data input pin
  $\overline{\text{SCK}}$: Serial clock I/O pin
- One interrupt source
  - Interrupt request signal (INTCSI0)

8.3.2 Configuration
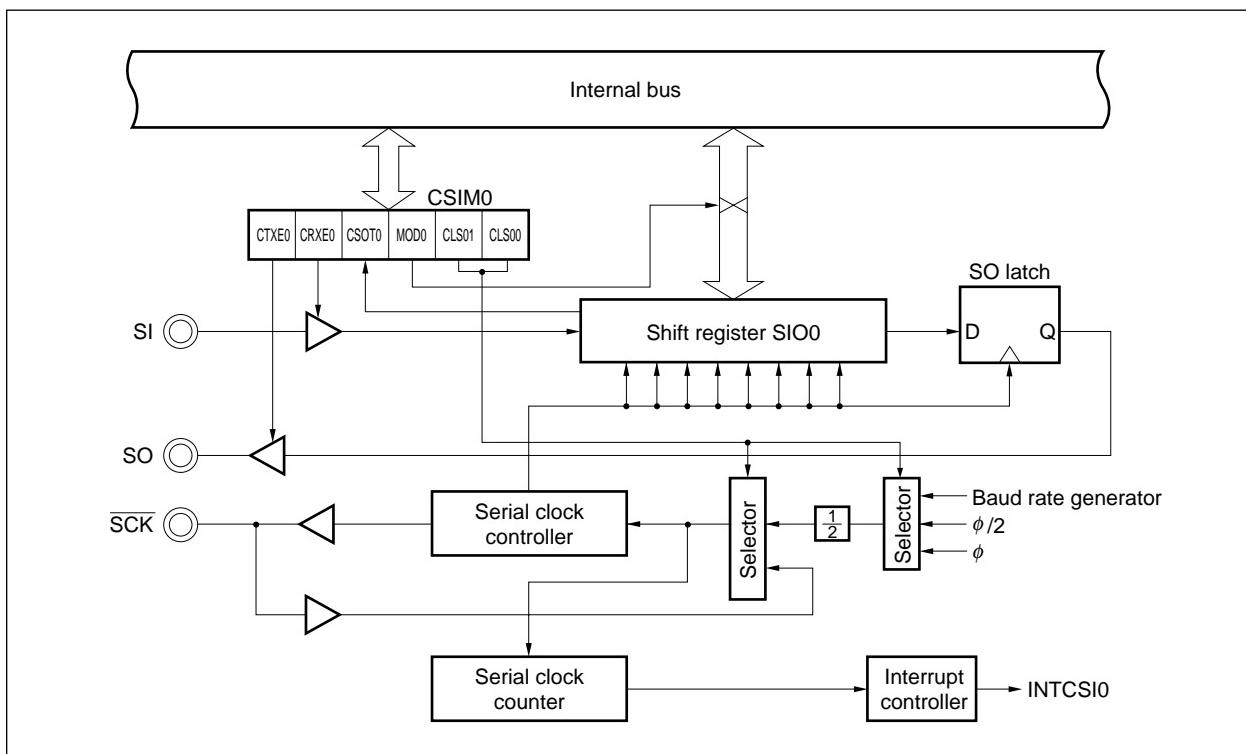
8.4 Baud Rate Generator (BRG)

8.4.1 Features
- Serial clock selectable from baud rate generator output and ϕ (system clock)
- Same baud rate for transmission/reception

8.4.2 Configuration
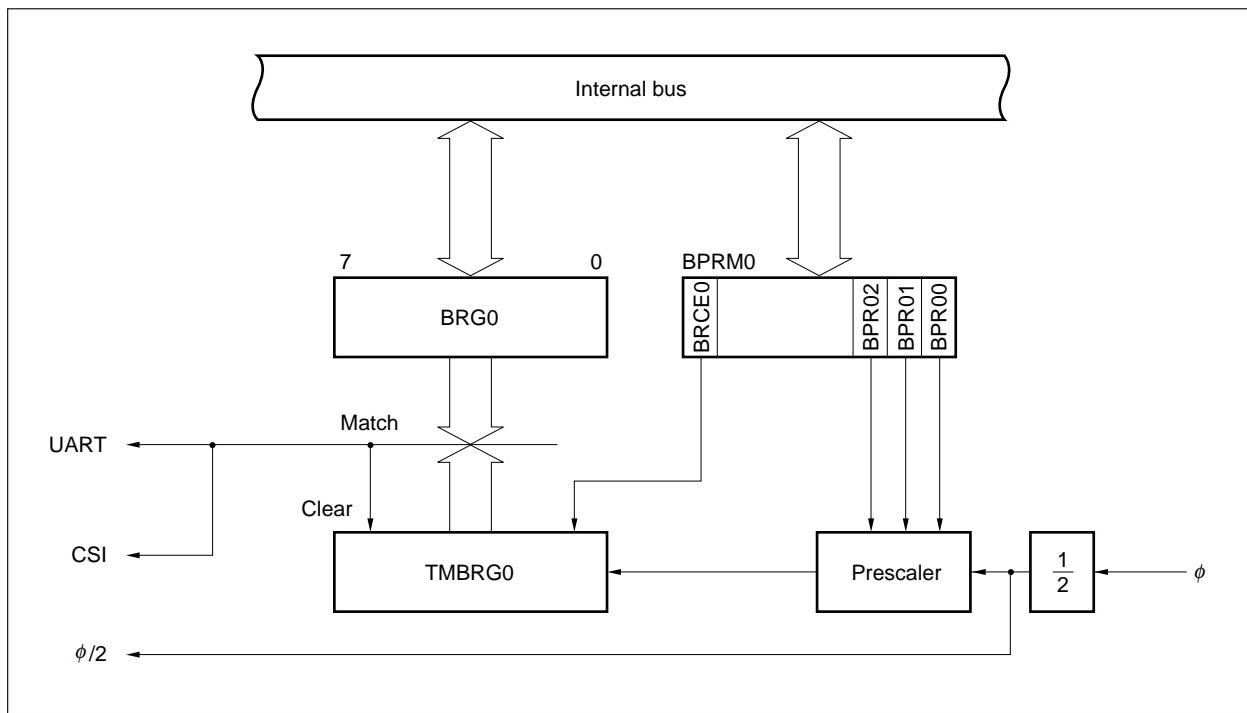
9. PORT FUNCTION

9.1 Features

The ports of the μPD703000 have the following features:

- Number of port pins
    Input port : 1
    I/O port : 67
- Shared with I/O pins of other peripheral functions
- Input/output specifiable bitwise
- Noise elimination
- Edge detection

9.2 Configuration

Figure 9-1. Block Diagram of P00, P01 (Port 0)

Remark n=0, 1
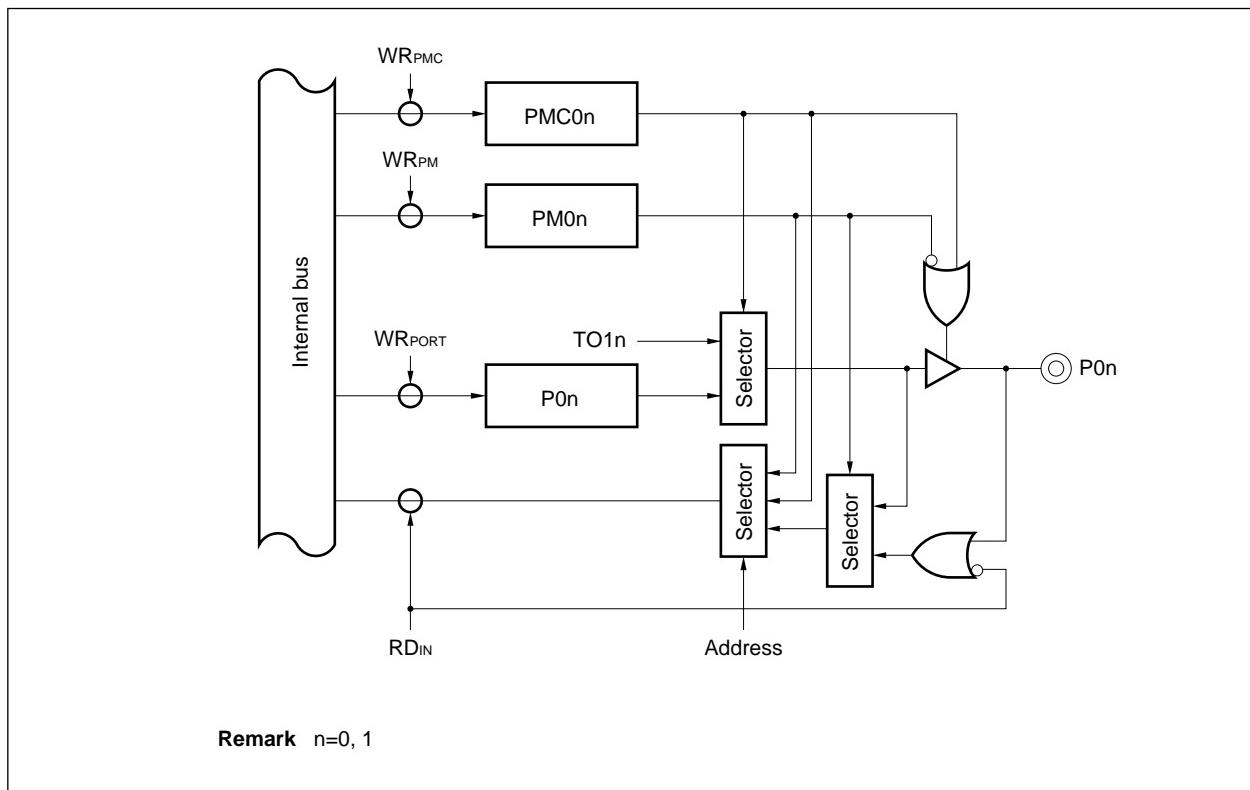
Figure 9-2. Block Diagram of P02 to P07 (Port 0)

Remark n=2-7
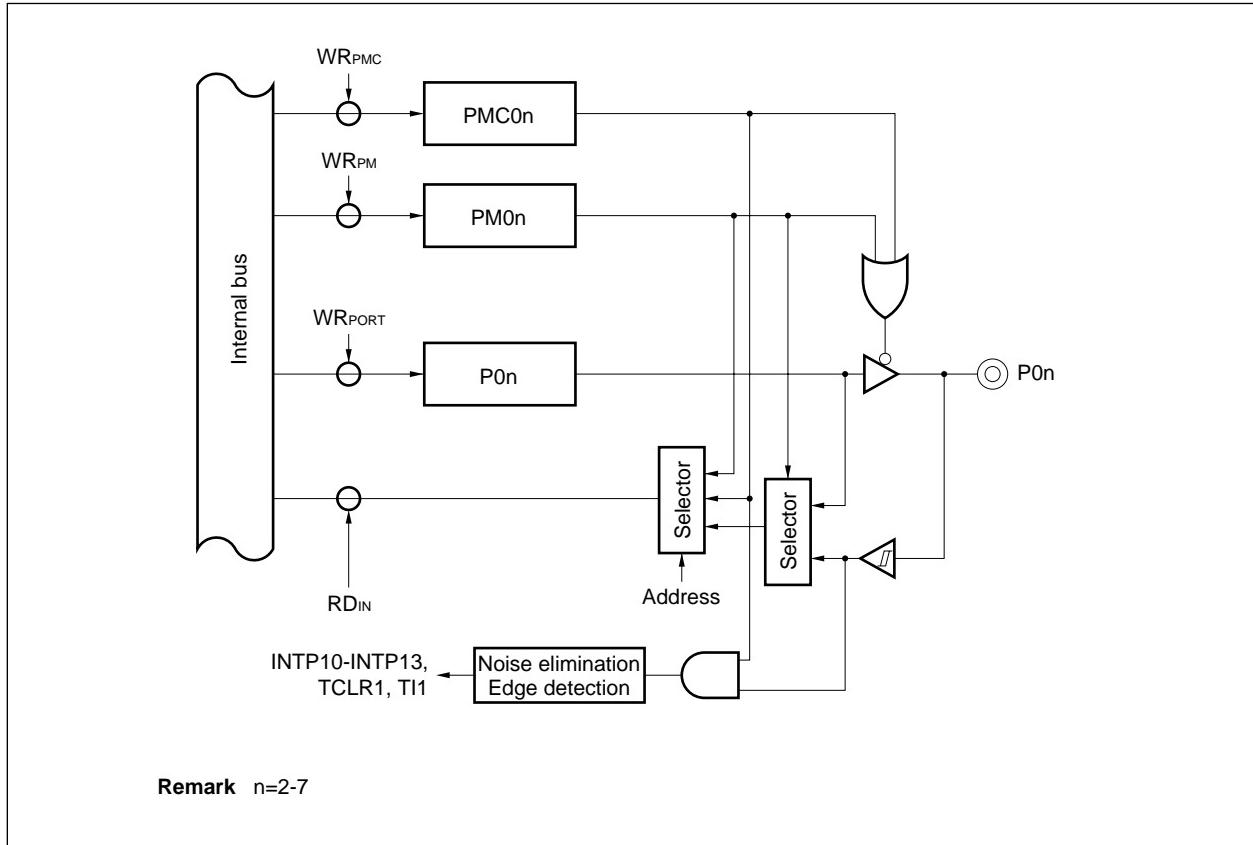
Figure 9-3. Block Diagram of P10 to P17 (Port 1)
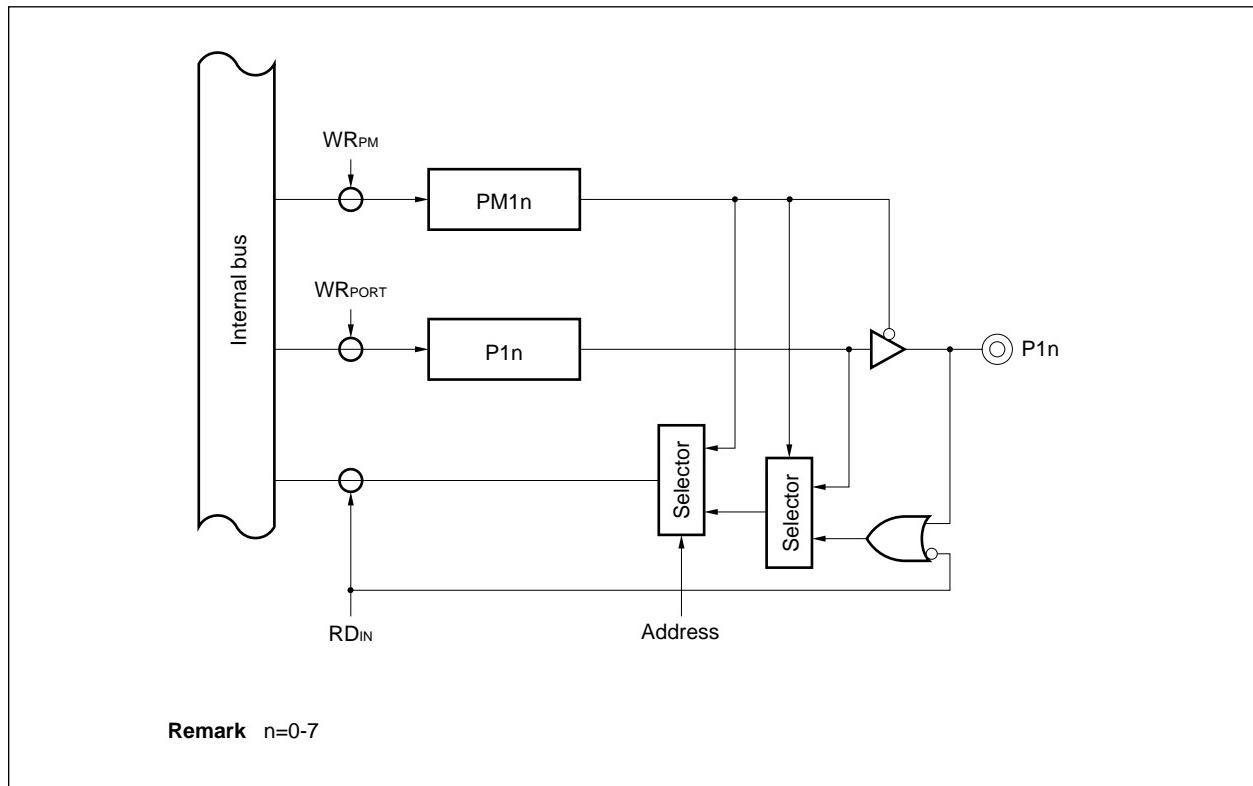
Remark n=0-7

Figure 9-4. Block Diagram of P20 (Port 2)
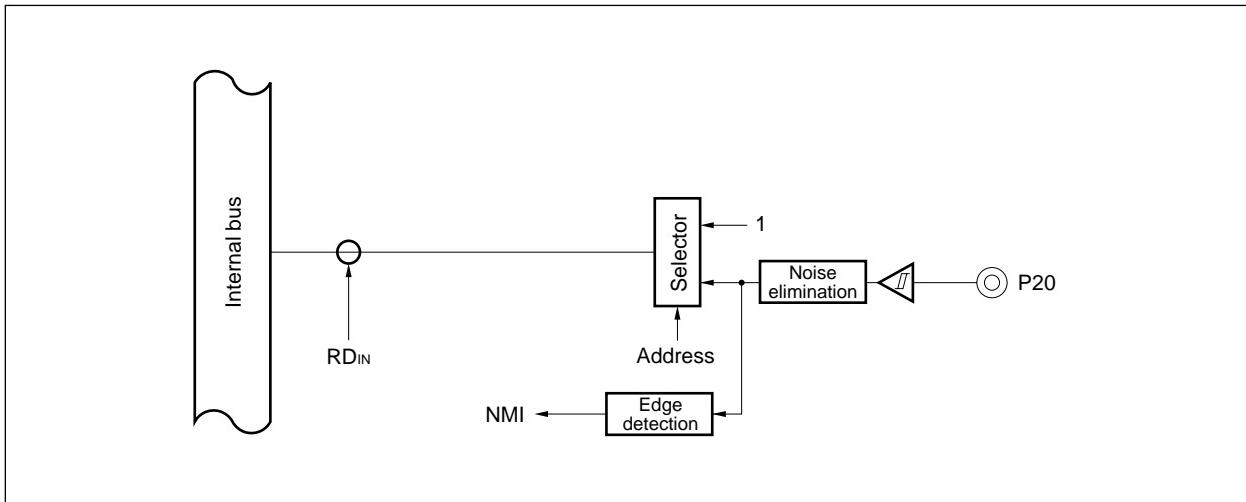
Figure 9-5. Block Diagram of P21 to P24 (Port 2)
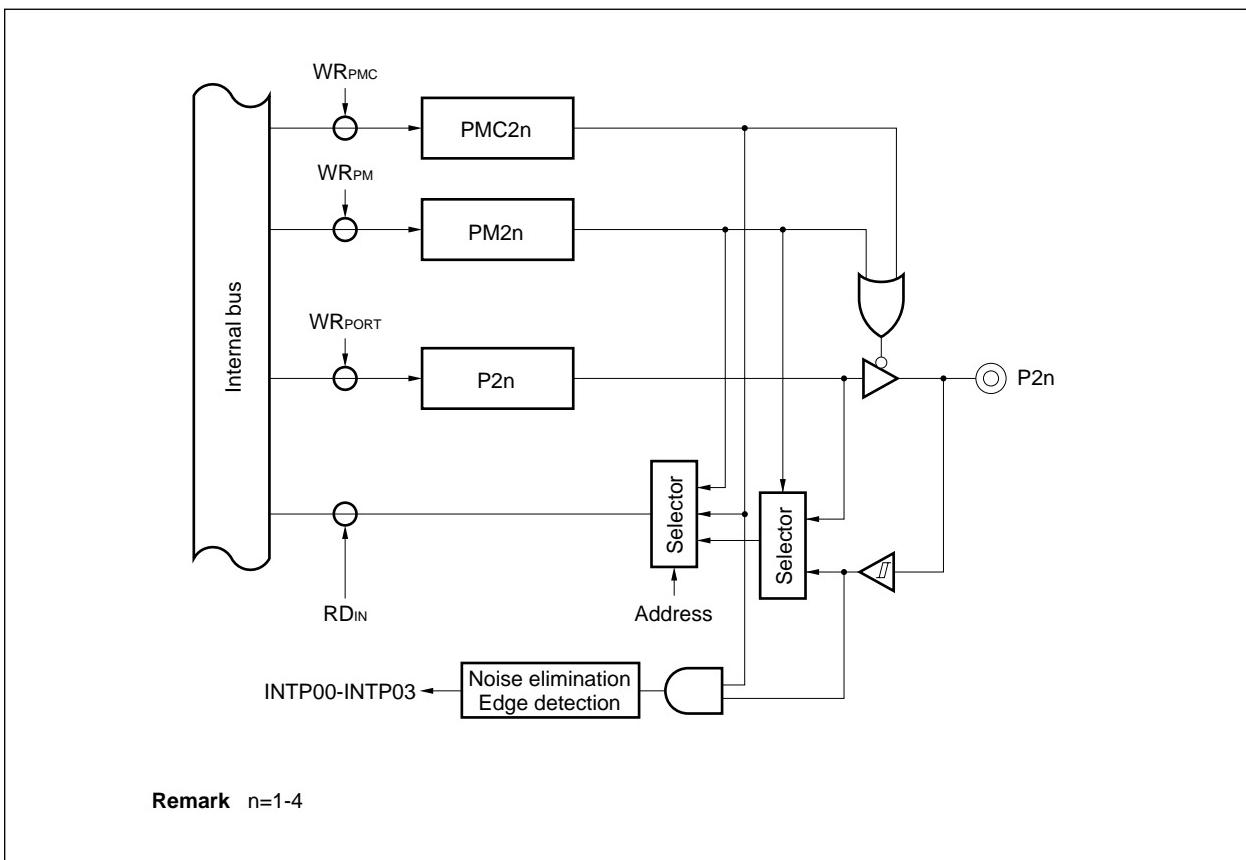
Figure 9-6. Block Diagram of P25 (Port 2)
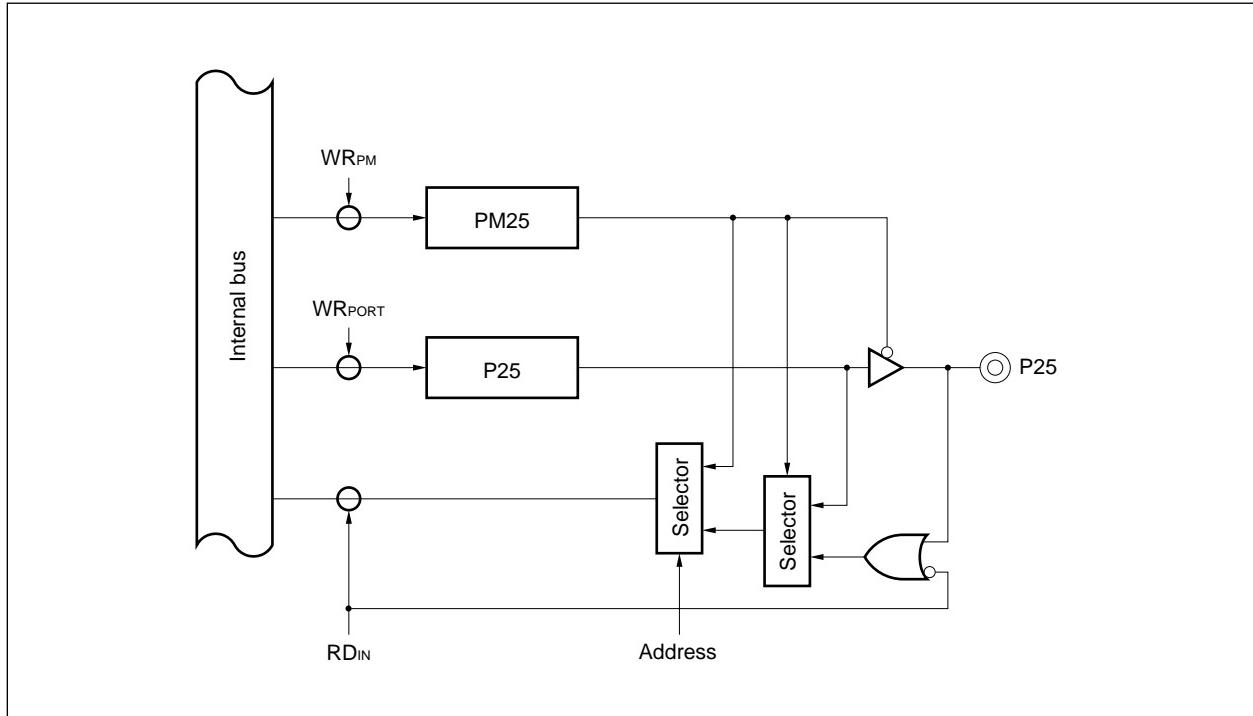
Figure 9-7. Block Diagram of P26, P27 (Port 2)
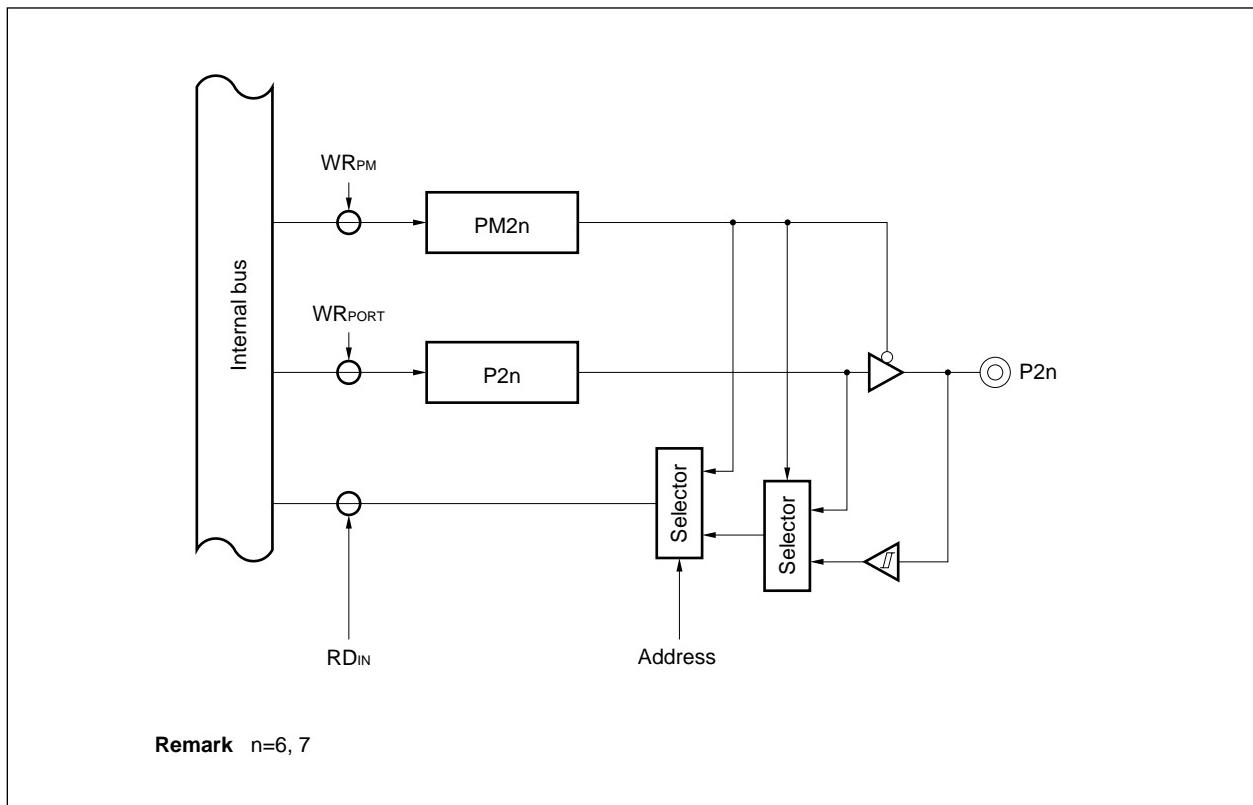
Remark   n=6, 7

Figure 9-8. Block Diagram of P30, P33 (Port 3)
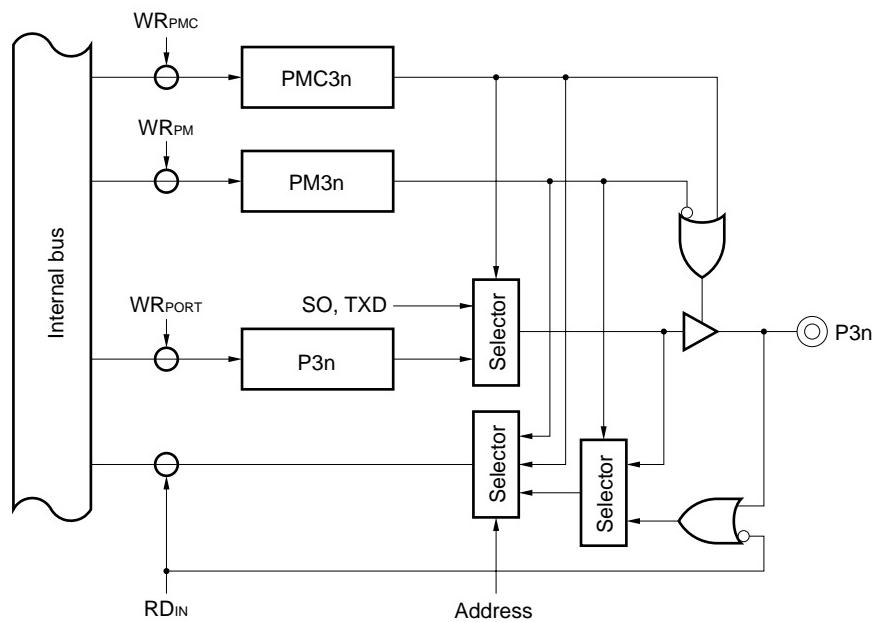
Remark   n=0, 3

Figure 9-9. Block Diagram of P31 (Port 3)
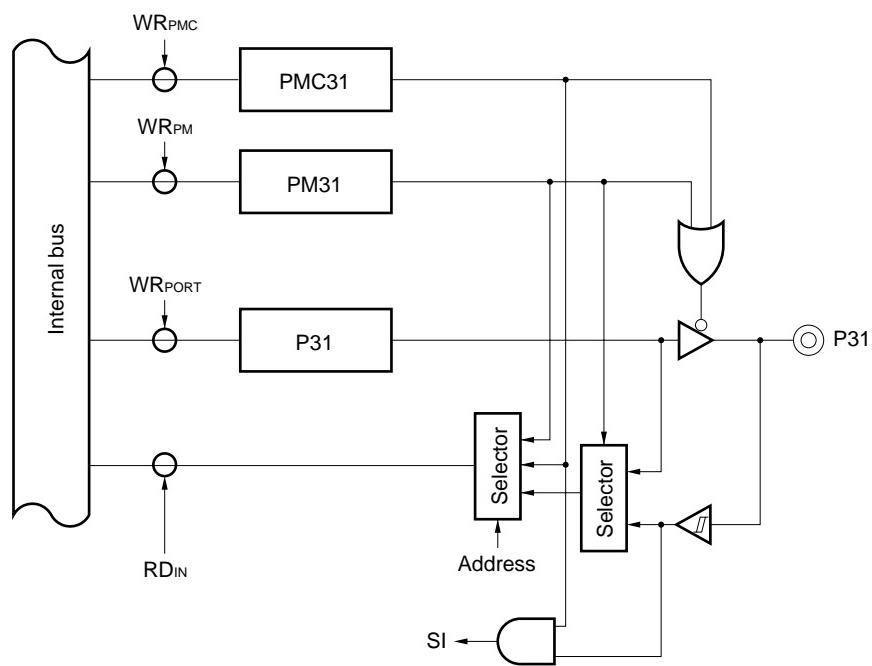
Figure 9-10. Block Diagram of P32 (Port 3)
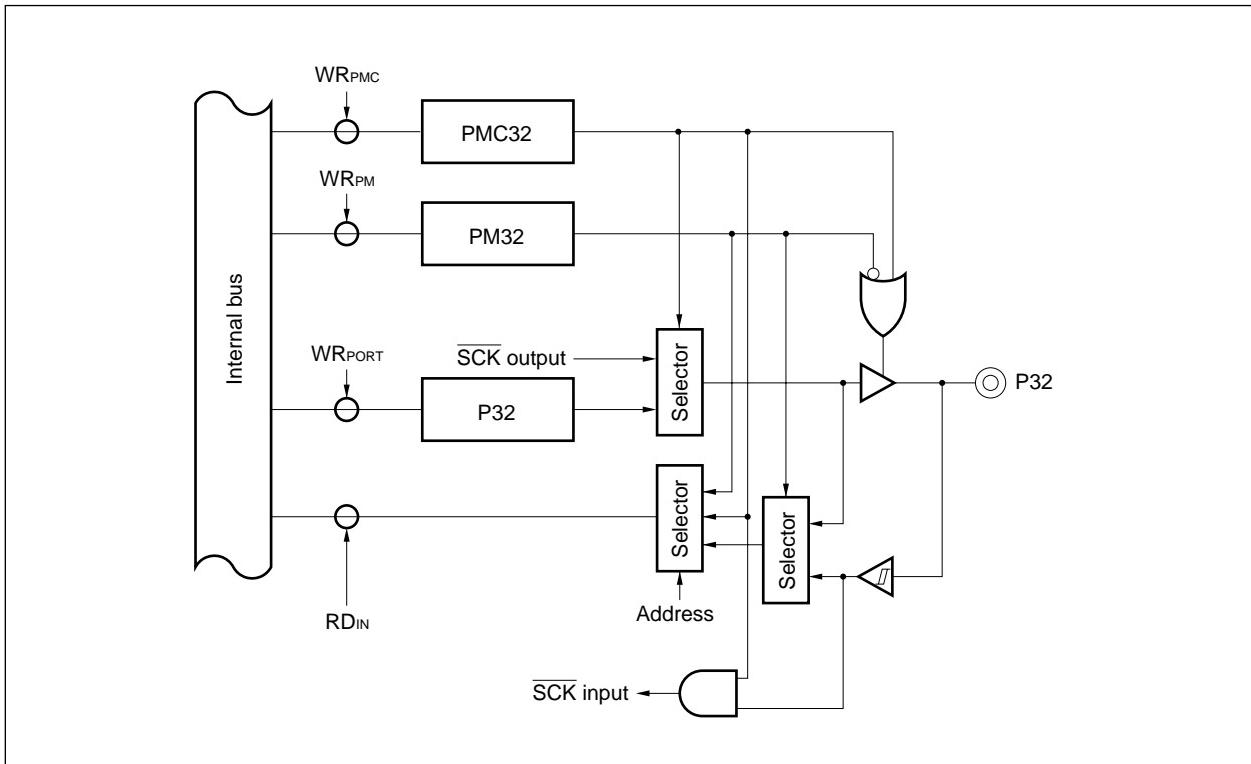
Figure 9-11. Block Diagram of P34 (Port 3)
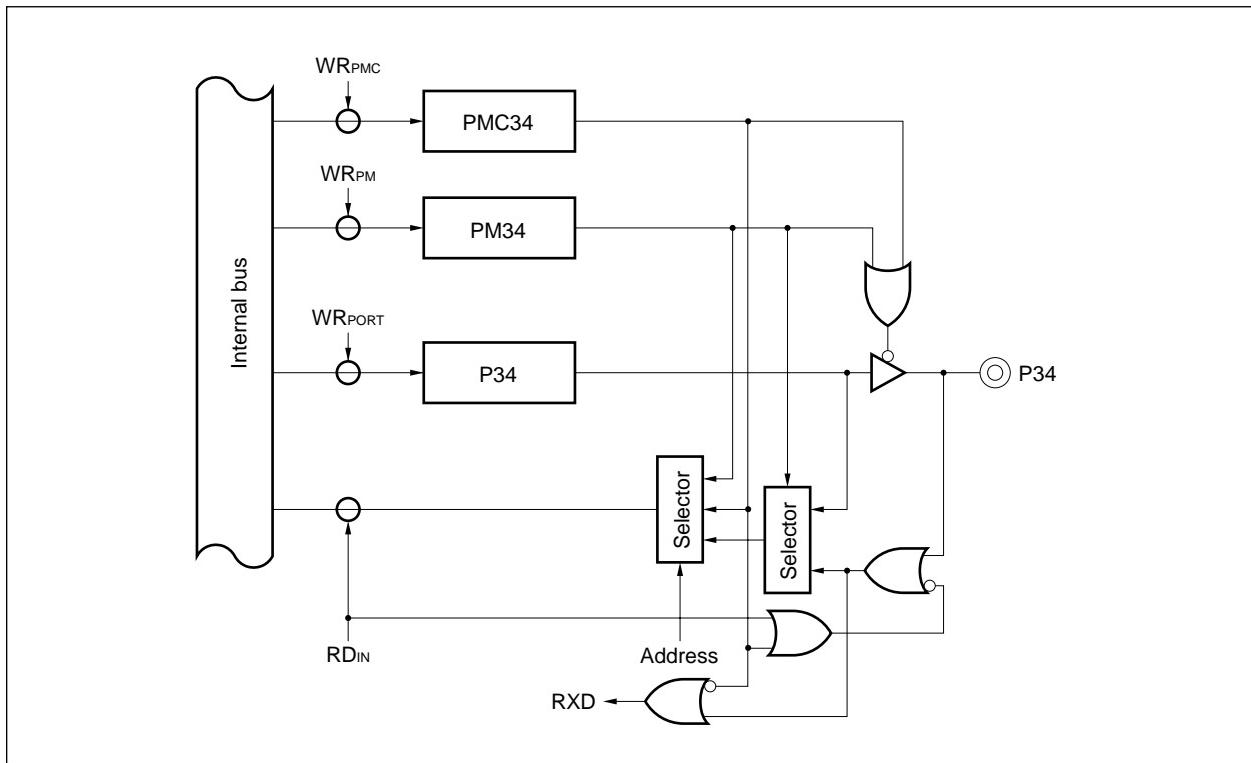
Figure 9-12. Block Diagram of P35 (Port 3)
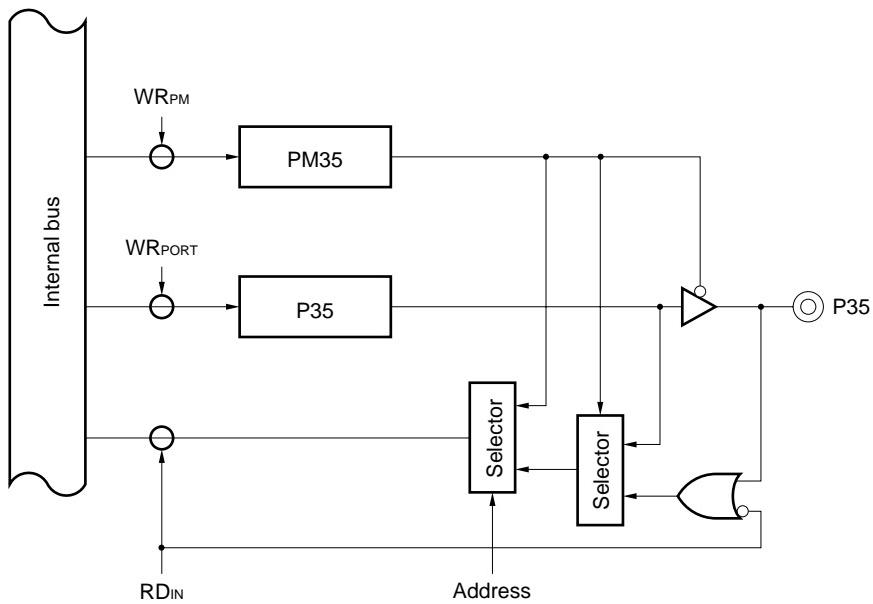
Figure 9-13. Block Diagram of P36, P37 (Port 3)
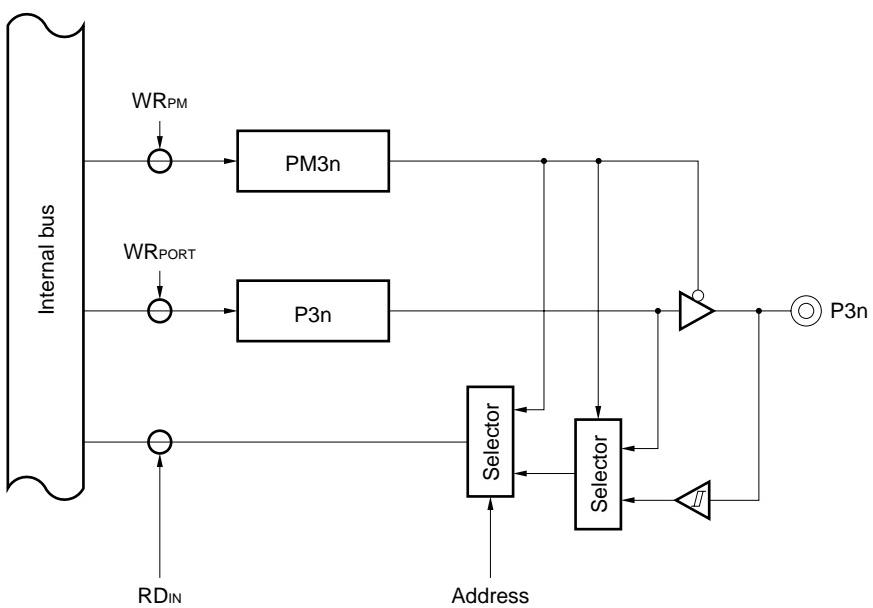
Remark n=6, 7

**Figure 9-14. Block Diagram of P40 to P47 (Port 4)**

Remark   n=0-7
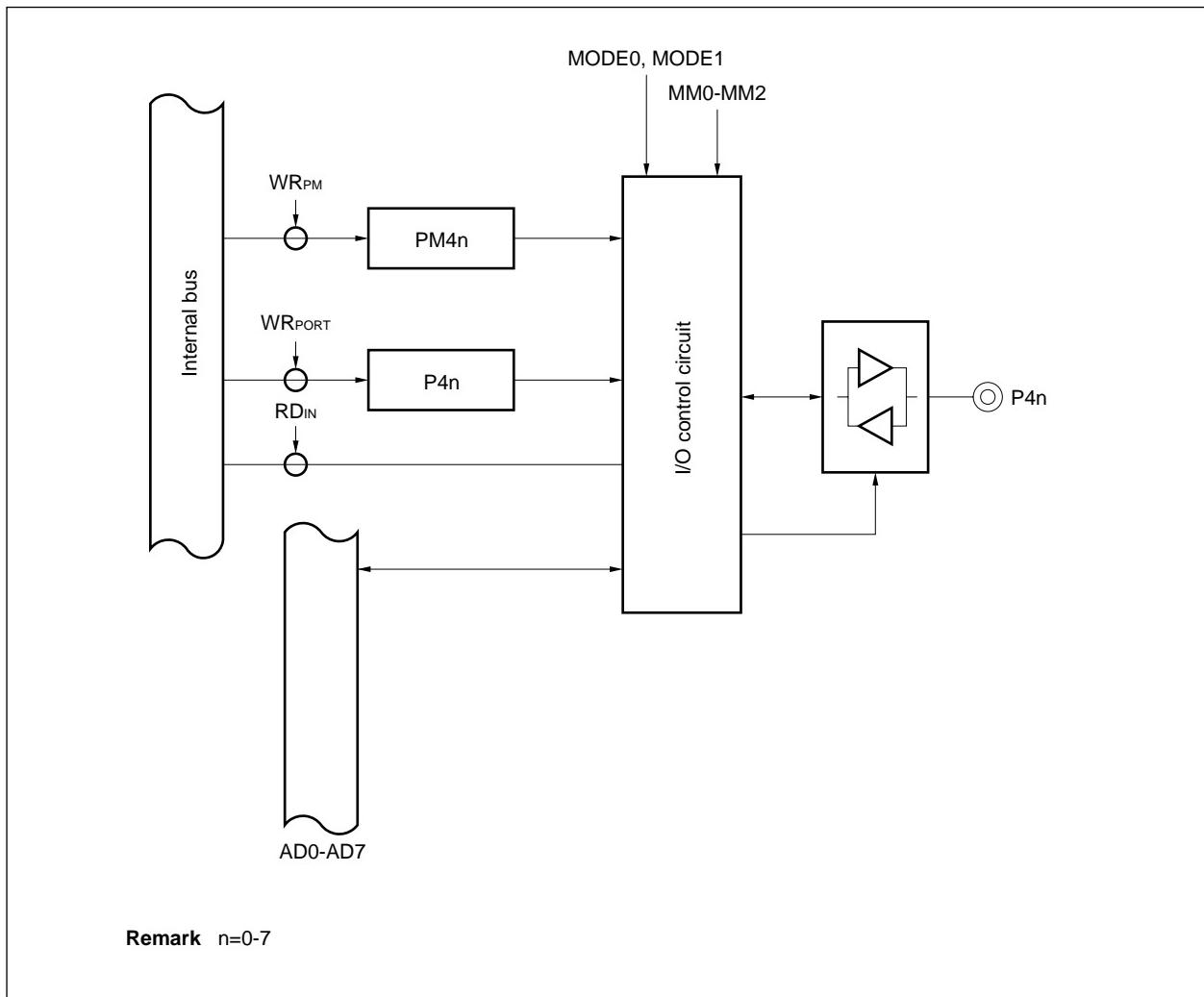
Figure 9-15. Block Diagram of P50 to P57 (Port 5)
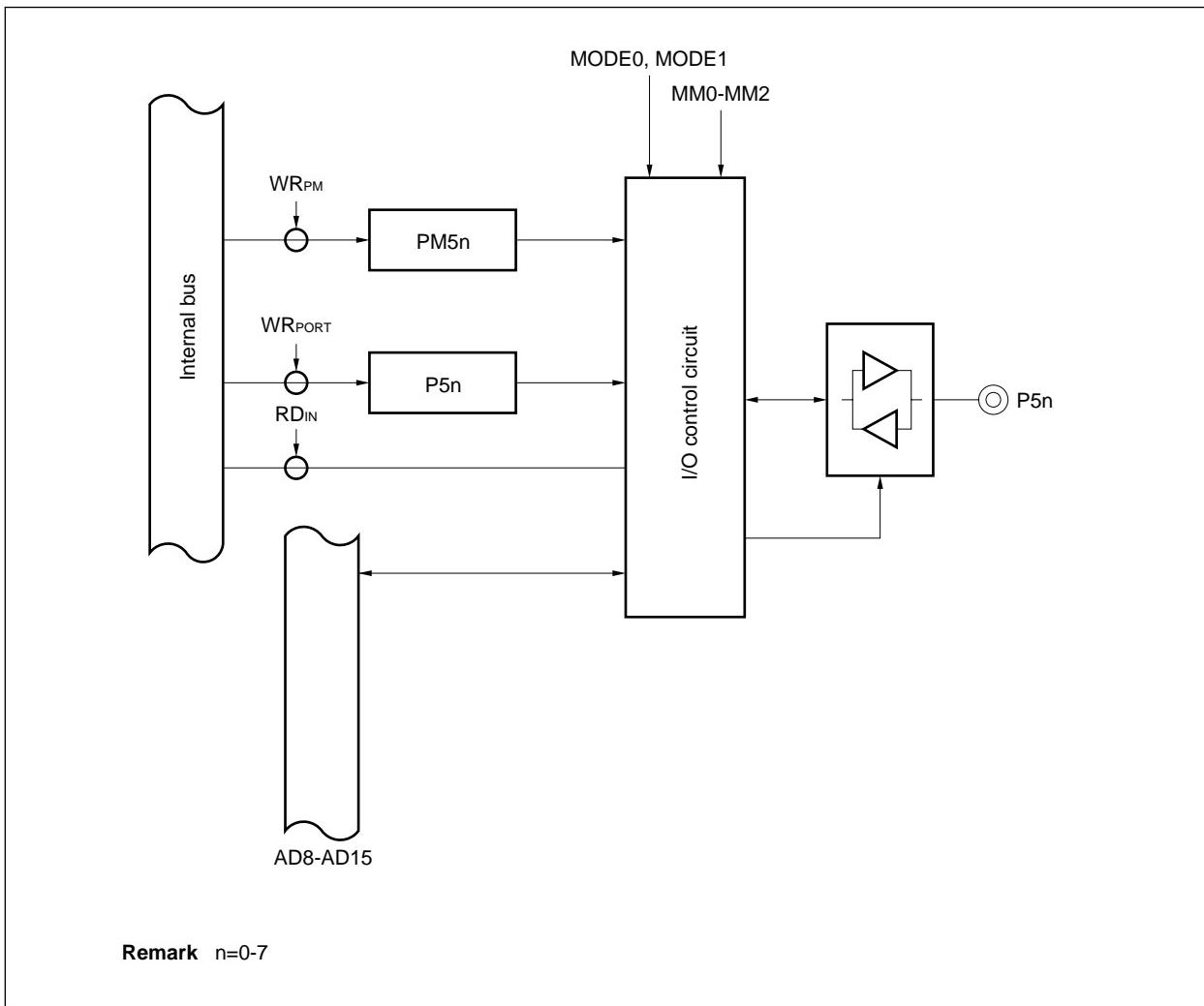
Figure 9-16. Block Diagram of P60 to P67 (Port 6)
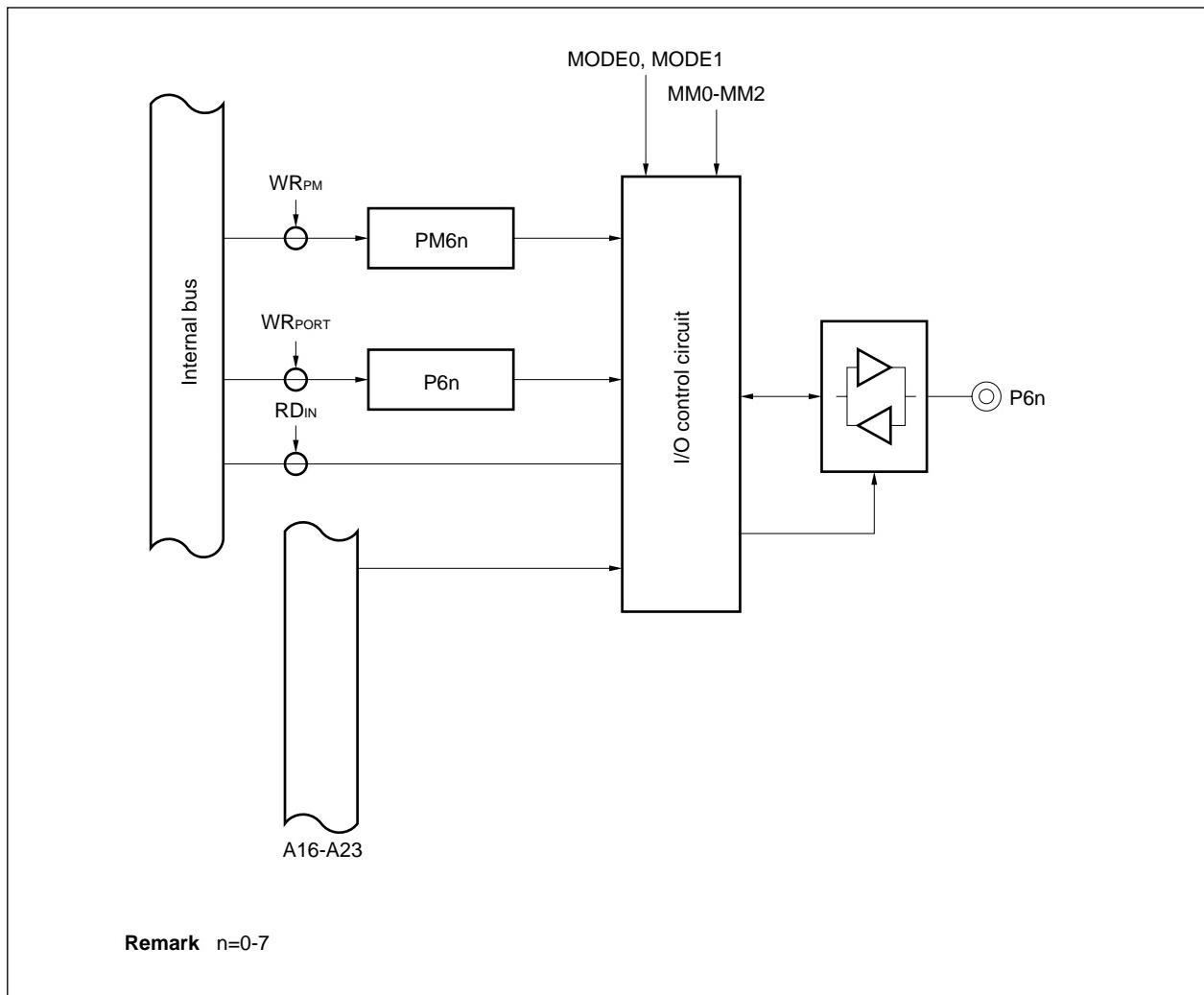
Figure 9-17. Block Diagram of P90 to P97 (Port 9)

Remark   n=0-7
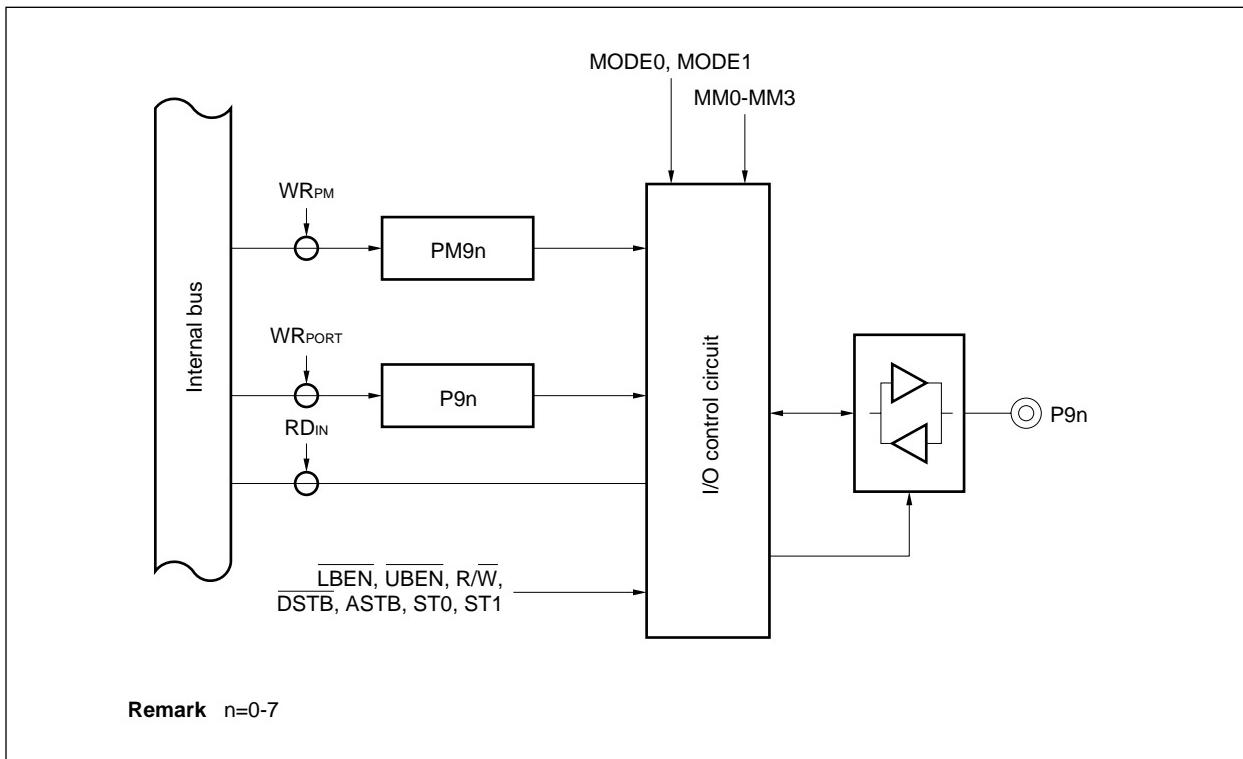
Figure 9-18. Block Diagram of P100, P103 (Port 10)

Note   RFU is undefined value.

Remark   n=0, 3
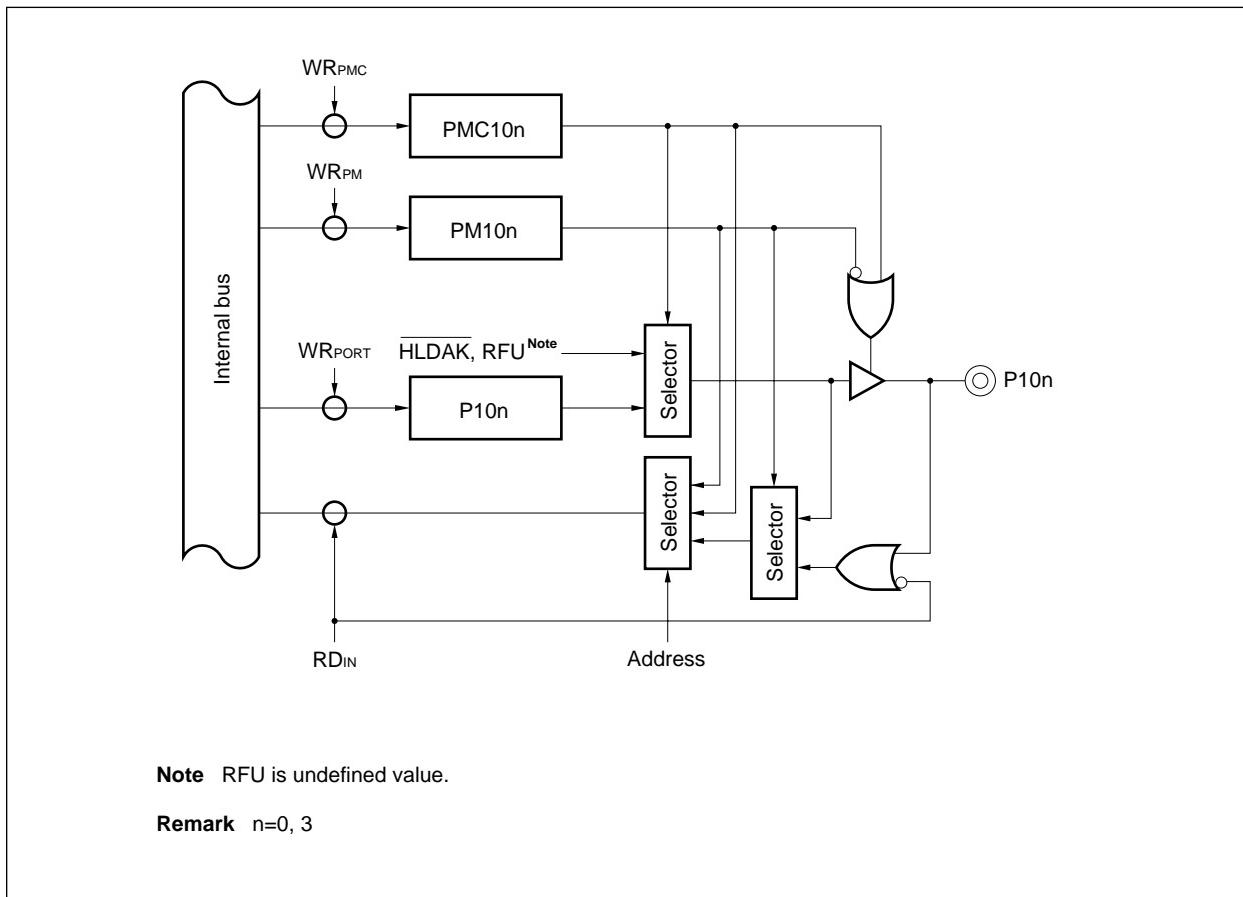
Figure 9-19. Block Diagram of P101 (Port 10)
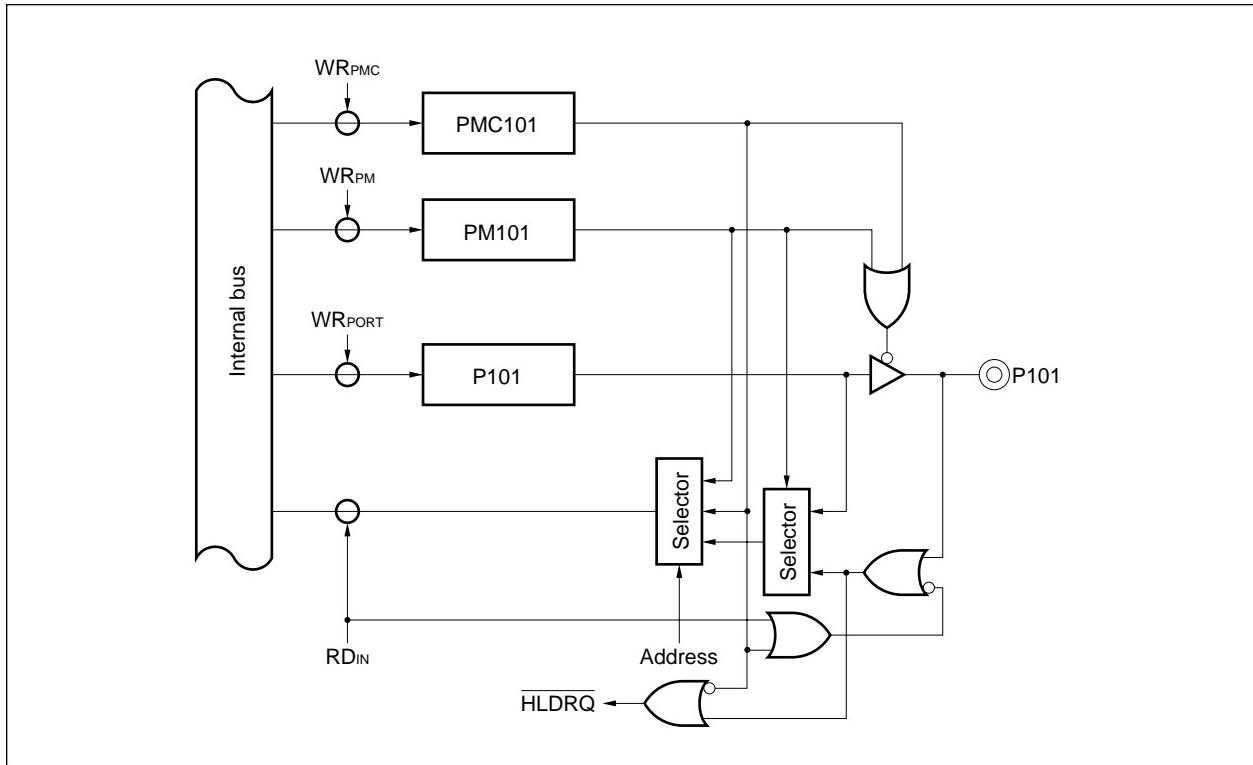
Figure 9-20. Block Diagram of P102 (Port 10)
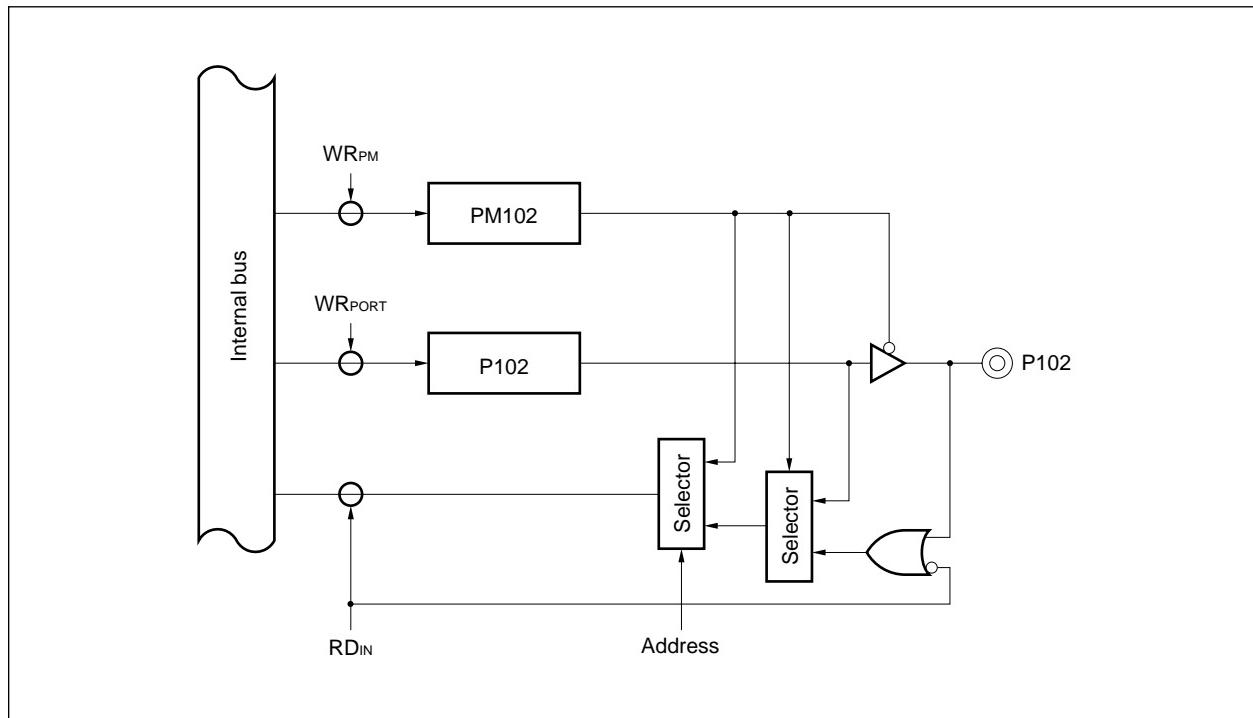
10. RESET FUNCTION

When the $\overline{\text{RESET}}$ signal is made low, the system is reset, and the on-chip hardware units are initialized.

The reset status is cleared when the $\overline{\text{RESET}}$ signal is made high, and the CPU starts executing the program.
Initialize the contents of each register in the program as necessary.

10.1 Features
- Noise elimination circuit of analog delay ($\fallingdotseq$ 60 ns) provided to reset pin

11. INSTRUCTION SET

11.1 Instruction Set List

• **How to read instruction set list**

This column indicates an instruction group. This instruction set list classifies instructions by group.

This column indicates the mnemonic of the instruction.

This column indicates the operand of the instruction (refer to **Table 11-1**) .

This column indicates the instruction code in binary number . The instruction code of a 32-bit instruction is shown in two columns (refer to **Table 11-2**).

This column indicates the operation of the instruction (refer to **Table 11-3**) .

This column indicate the operation of the flags (refer to **Table 11-4**).

Instruction group	Mnemonic	Operand	op code	Operation	Flag				
					CY	OV	S	Z	SAT

Table 11-1. Symbols Shown in "Operand" Column

Symbol	Meaning
reg1	General register (used as source register)
reg2	General register (mainly used as destination register. Some are also used as source registers)
ep	Element pointer
bit#3	3-bit data for bit number specification
immX	X-bit immediate
dispX	X-bit displacement
regID	System register number
vector	5-bit data specifying trap vector (00H through 1FH)
cccc	4-bit data indicating condition code

★ **Table 11-2. Symbols Shown in "op Code" Column**

Symbol	Meaning
R	1-bit data of code specifying reg1 or regID
r	1-bit data of code specifying reg2
d	1-bit data of displacement
i	1-bit data of immediate
cccc	4-bit data indicating condition code
bbb	3-bit data specifying bit number

Table 11-3. Symbols Shown in "Operation" Column

Symbol	Meaning
←	Assignment
GR [ ]	General register
SR [ ]	System register
zero-extend (n)	Zero-extends "n" to word length
sign-extend (n)	Sign-extends "n" to word length
load-memory (a, b)	Reads data of size "b" from address "a"
store-memory (a, b, c)	Writes data "b" of size "c" to address "a"
load-memomy-bit (a, b)	Reads bit "b" of address "a"
store-memory-bit (a, b, c)	Writes "c" to bit "b" of address "a"
saturated (n)	Performs saturated processing of n (n is 2's complement) "n" indicates result of operation. If "n" $\geq$ 7FFFFFFFH, 7FFFFFFFH If "n" $\leq$ 80000000H, 80000000H
result	Reflects result on flag
Byte	Byte (8 bits)
Halfword	Halfword (16 bits)
Word	Word (32 bits)
+	Add
–	Subtract
||	Bit concatenation
×	Multiply
÷	Divide
AND	Logical product
OR	Logical sum
XOR	Exclusive logical sum
NOT	Logical negation
logically shift left by	Logical left shift
logically shift right by	Logical right shift
arithmetically shift right by	Arithmetic right shift

Table 11-4. Symbols Shown in "Flag" Column

Identifier	Meaning
(blank)	Not affected
0	Cleared to 0
×	Set or cleared according to result
R	Value once saved is restored

Table 11-5. Condition Codes

Condition Name (cond)	Condition Code (cccc)	Conditional Expression	Meaning
V	0000	OV=1	Overflow
NV	1000	OV=0	No overflow
C/L	0001	CY=1	Carry Lower (Less than)
NC/NL	1001	CY=0	No carry Not lower (Greater than or equal)
Z/E	0010	Z=1	Zero Equal
NZ/NE	1010	Z=0	Not zero Not equal
NH	0011	(CY OR Z)=1	Not higher (Less than or equal)
H	1011	(CY OR Z)=0	Higher (Greater than)
N	0100	S=1	Negative
P	1100	S=0	Positive
T	0101	–	Always (unconditional)
SA	1101	SAT=1	Saturated
LT	0110	(S XOR OV)=1	Less than signed
GE	1110	(S XOR OV)=0	Greater than or equal signed
LE	0111	((S XOR OV) OR Z)=1	Less than or equal signed
GT	1111	((S XOR OV) OR Z)=0	Greater than signed

Instruction Set List

Instruction Group	Mnemonic	Operand	op Code	Operation	Flag				
					CY	OV	S	Z	SAT
Load/store	SLD.B	disp7[ep], reg2	rrrrr0110ddddddd	adr←ep+zero-extend(disp7) GR[reg2]←sign-extend(Load-memory(adr, Byte))					
	SLD.H	disp8[ep], reg2	rrrrr1000ddddddd **Note 1**	adr←ep+zero-extend(disp8) GR[reg2]←sign-extend(Load-memory(adr, Halfword))					
	SLD.W	disp8[ep], reg2	rrrrr1010dddddd0 **Note 2**	adr←ep+zero-extend(disp8) GR[reg2]←Load-memory(adr, Word)					
	LD.B	disp16[reg1], reg2	rrrrr111000RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory(adr, Byte))					
	LD.H	disp16[reg1], reg2	rrrrr111001RRRRR ddddddddddddddd0 **Note 3**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory(adr, Halfword))					
	LD.W	disp16[reg1], reg2	rrrrr111001RRRRR ddddddddddddddd1 **Note 3**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←Load-memory(adr, Word)					
	SST.B	reg2, disp7[ep]	rrrrr0111ddddddd	adr←ep+zero-extend(disp7) Store-memory(adr, GR[reg2], Byte)					
	SST.H	reg2, disp8[ep]	rrrrr1001ddddddd **Note 1**	adr←ep+zero-extend(disp8) Store-memory(adr, GR[reg2], Halfword)					
	SST.W	reg2, disp8[ep]	rrrrr1010dddddd1 **Note 2**	adr←ep+zero-extend(disp8) Store-memory(adr, GR[reg2], Word)					
	ST.B	reg2, disp16[reg1]	rrrrr111010RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr, GR[reg2], Byte)					
	ST.H	reg2, disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd0 **Note 3**	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr, GR[reg2], Halfword)					
	ST.W	reg2, disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd1 **Note 3**	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr, GR[reg2], Word)					
Arithmetic operation	MOV	reg1, reg2	rrrrr000000RRRRR	GR[reg2]←GR[reg1]					
	MOV	imm5, reg2	rrrrr010000iiiii	GR[reg2]←sign-extend(imm5)					
	MOVHI	imm16, reg1, reg2	rrrrr110010RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+(imm16 || 0^{16})					
	MOVEA	imm16, reg1, reg2	rrrrr110001RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+sign-extend(imm16)					
	ADD	reg1, reg2	rrrrr001110RRRRR	GR[reg2]←GR[reg2]+GR[reg1]	×	×	×	×	
	ADD	imm5, reg2	rrrrr010010iiiii	GR[reg2]←GR[reg2]+sign-extend(imm5)	×	×	×	×	
	ADDI	imm16, reg1, reg2	rrrrr110000RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+sign-extend(imm16)	×	×	×	×	
	SUB	reg1, reg2	rrrrr001101RRRRR	GR[reg2]←GR[reg2]–GR[reg1]	×	×	×	×	
	SUBR	reg1, reg2	rrrrr001100RRRRR	GR[reg2]←GR[reg1]–GR[reg2]	×	×	×	×	

Notes 1. ddddddd = the higher 7-bit of disp8

2. dddddd = the higher 6-bit of disp8

3. ddddddddddddddd = the higher 15-bit of disp16

Instruction Group	Mnemonic	Operand	op Code	Operation	Flag CY	OV	S	Z	SAT
Arithmetic operation	MULH	reg1, reg2	rrrrr000111RRRRR	GR[reg2]←GR[reg2]^Note×GR[reg1]^Note(signed multiply)					
	MULH	imm5, reg2	rrrrr010111iiiii	GR[reg2]←GR[reg2]^Note×sign-extend(imm5) (signed multiply)					
	MULHI	imm16, reg1, reg2	rrrrr110111RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg2]^Note×imm16 (signed multiply)					
	DIVH	reg1, reg2	rrrrr000010RRRRR	GR[reg2]←GR[reg2]÷GR[reg1]^Note(signed divide)		×	×	×	
	CMP	reg1, reg2	rrrrr001111RRRRR	result←GR[reg2]–GR[reg1]	×	×	×	×	
	CMP	imm5, reg2	rrrrr010011iiiii	result←GR[reg2]–sign-extend(imm5)	×	×	×	×	
	SETF	cccc, reg2	rrrrr1111110cccc 0000000000000000	if conditions are satisfied then GR[reg2]←00000001H else GR[reg2]←00000000H					
Saturation operation	SATADD	reg1, reg2	rrrrr000110RRRRR	GR[reg2]←saturated(GR[reg2]+GR[reg1])	×	×	×	×	×
	SATADD	imm5, reg2	rrrrr010001iiiii	GR[reg2]←saturated(GR[reg2]+sign-extend(imm5))	×	×	×	×	×
	SATSUB	reg1, reg2	rrrrr000101RRRRR	GR[reg2]←saturated(GR[reg2]–GR[reg1])	×	×	×	×	×
	SATSUBI	imm16, reg1, reg2	rrrrr110011RRRRR iiiiiiiiiiiiiiii	GR[reg2]←saturated(GR[reg1]–sign-extend(imm16))	×	×	×	×	×
	SATSUBR	reg1, reg2	rrrrr000100RRRRR	GR[reg2]←saturated(GR[reg1]–GR[reg2])	×	×	×	×	×
Logical operation	TST	reg1, reg2	rrrrr001011RRRRR	result←GR[reg2]AND GR[reg1]		0	×	×	
	OR	reg1, reg2	rrrrr001000RRRRR	GR[reg2]←GR[reg2]OR GR[reg1]		0	×	×	
	ORI	imm16, reg1, reg2	rrrrr110100RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]OR zero-extend(imm16)		0	×	×	
	AND	reg1, reg2	rrrrr001010RRRRR	GR[reg2]←GR[reg2]AND GR[reg1]		0	×	×	
	ANDI	imm16, reg1, reg2	rrrrr110110RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]AND zero-extend(imm16)		0	0	×	
	XOR	reg1, reg2	rrrrr001001RRRRR	GR[reg2]←GR[reg2]XOR GR(reg1)		0	×	×	
	XORI	imm16, reg1, reg2	rrrrr110101RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]XOR zero-extend(imm16)		0	×	×	
	NOT	reg1, reg2	rrrrr000001RRRRR	GR[reg2]←NOT(GR[reg1])		0	×	×	
	SHL	reg1, reg2	rrrrr111111RRRRR 0000000011000000	GR[reg2]←GR[reg2]logically shift left by GR[reg1]	×	0	×	×	
	SHL	imm5, reg2	rrrrr010110iiiii	GR[reg2]←GR[reg2]logically shift left by zero-extend(imm5)	×	0	×	×	
	SHR	reg1, reg2	rrrrr111111RRRRR 0000000010000000	GR[reg2]←GR[reg2]logically shift right by GR[reg1]	×	0	×	×	
	SHR	imm5, reg2	rrrrr010100iiiii	GR[reg2]←GR[reg2]logically shift right by zero-extend(imm5)	×	0	×	×	
	SAR	reg1, reg2	rrrrr111111RRRRR 0000000010100000	GR[reg2]←GR[reg2]arithmetically shift right by GR[reg1]	×	0	×	×	
	SAR	imm5, reg2	rrrrr010101iiiii	GR[reg2]←GR[reg2]arithmetically shift right by zero-extend(imm5)	×	0	×	×	

Note Only the lower halfword data is valid.

Instruction Group	Mnemonic	Operand	op Code	Operation	Flag				
					CY	OV	S	Z	SAT
Branch	JMP	[reg1]	0000000011RRRRR	PC←GR[reg1]					
	JR	disp22	0000011110dddddd ddddddddddddddd0 **Note 1**	PC←PC+sign-extend(disp22)					
	JARL	disp22, reg2	rrrrr11110dddddd ddddddddddddddd0 **Note 1**	GR[reg2]←PC+4 PC←PC+sign-extend(disp22)					
	Bcond	disp9	ddddd1011dddcccc **Note 2**	if conditions are satisfied then PC←PC+sign-extend(disp9)					
Bit manipulation	SET1	bit#3, disp16[reg1]	00bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr, bit#3)) Store-memory-bit(adr, bit#3, 1)				×	
	CLR1	bit#3, disp16[reg1]	10bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr, bit#3)) Store-memory-bit(adr, bit#3, 0)				×	
	NOT1	bit#3, disp16[reg1]	01bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr, bit#3)) Store-memory-bit(adr, bit#3, Z flag)				×	
	TST1	bit#3, disp16[reg1]	11bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr, bit#3))				×	

Notes 1. dddddddddddddddddddd = the higher 21-bit of disp22

   2. dddddddd = the higher 8-bit of disp9

Instruction Group	Mnemonic	Operand	op Code	Operation		Flag				
						CY	OV	S	Z	SAT
Special	LDSR	reg2, regID	rrrrr111111RRRRR 0000000000100000	SR[regID]←GR[reg2]	reg ID = EIPC, FEPC					
					reg ID = EIPSW, FEPSW					
			Note		regID = PSW	×	×	×	×	×
	STSR	regID, reg2	rrrrr111111RRRRR 0000000001000000	GR[reg2]←SR[regID]						
	TRAP	vector	00000111111iiiii 0000000100000000	EIPC←PC+4 (restore PC) EIPSW←PSW ECR.EICC←Interrupt code PSW.EP←1 PSW.ID←1 PC←00000040H(vector=00H-0FH) 00000050H(vector=10H-1FH)						
	RETI		0000011111100000 0000000101000000	if PSW.EP=1 then PC←EIPC PSW←EIPSW else if PSW.NP=1 then PC←FEPC PSW←FEPSW else PC←EIPC PSW←EIPSW		R	R	R	R	R
	HALT		0000011111100000 0000000100100000	Stops						
	DI		0000011111100000 0000000101100000	PSW.ID←1 (disables maskable interrupt)						
	EI		1000011111100000 0000000101100000	PSW.ID←0 (enables maskable interrupt)						
	NOP		0000000000000000	Dissipates 1 clock cycle without doing anything						

Note This instruction uses reg2 as the source register, but its op code actually uses the field of reg1. Therefore, the meanings of the register specification for the mnemonic and op code of this instruction are different from those of other instructions.

rrrrr = regID specification, RRRRR = reg2 specification

12. ELECTRICAL SPECIFICATIONS

Supported Electrical Characteristics

Part Number	V_{DD} = 5.0 V±10%	V_{DD} = 3.0 to 3.6 V
μPD703000GC-25-xxx-7EA	Electrical characteristics specified	Outside of guaranteed operating range
μPD703001GC-25-7EA	Electrical characteristics specified	Outside of guaranteed operating range
μPD703000GC-33-xxx-7EA	Electrical characteristics specified	Electrical characteristics specified
μPD703001GC-33-7EA	Electrical characteristics specified	Electrical characteristics specified

Remark   xxx indicates a ROM code suffix.

12.1 When V_{DD} = 5.0 V $\pm$ 10%

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	V_{DD} pin	−0.5 to +7.0	V
	CV_{DD}	CV_{DD} pin	−0.5 to +7.0	V
	CV_{SS}	CV_{SS} pin	−0.5 to +0.5	V
Input voltage	V_{I1}	Except X1 pin, V_{DD} = 5.0 V±10%	−0.5 to V_{DD} +0.3	V
Clock input voltage	V_X	X1 pin, V_{DD} = 5.0±10%	−0.5 to V_{DD} +1.0	V
Output current, low	I_{OL}	1 pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I_{OH}	1 pin	−4.0	mA
		Total of all pins	−100	mA
Output voltage	V_O	V_{DD} = 5.0 V±10%	−0.5 to V_{DD} +0.3	V
Operating temperature	T_A	Operating at 25 MHz	−40 to +85	$^\circ$C
		Operating at 33 MHz	−20 to +70	$^\circ$C
Storage temperature	T_{stg}		−65 to +150	$^\circ$C

Cautions 1. Do not directly connect to the output (or I/O) pins of an IC product, or to the V_{DD}, V_{CC}, or GND.

Open-drain pins and open-collector pins may be connected each other however. Moreover, an external circuit that is designed so as to avoid output contention can be directly connected to a pin that goes into a high-impedance state.

2. If even one of the parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be impaired. The absolute maximum ratings specify the values exceeding which the product may be physically damaged. Never exceed these ratings when using the products.

The specifications and conditions shown in DC and AC Characteristics below specify the range in which the product operates normally and the product quality is guaranteed.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz			15	pF
I/O capacitance	C_{IO}	0 V for pins other than test pin			15	pF
Output capacitance	C_O				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (ϕ)	Operating Temperature (T_A)	Supply Voltage (V_{DD})
Direct mode	0 to 25 MHz	−40 to +85°C	5.0 V±10%
	0 to 33 MHz	−20 to +70°C	
PLL mode	Self-running oscillation frequency to 25 MHz	−40 to +85°C	5.0 V±10%
	Self-running oscillation frequency to 33 MHz	−20 to +70°C	

Recommended Oscillation Circuit

(a) Connecting ceramic oscillator
(TDK, Murata Mfg.: T_A = −40 to +85°C, Kyocera: T_A = −20 to +80°C)

Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant		Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
TDK Corp.	FCR2.0MC3	2.0	Internal	Internal	4.5	5.5	0.26
	CCR3.2MC3	3.2	Internal	Internal	4.5	5.5	0.62
	FCR5.0MC5	5.0	Internal	Internal	4.5	5.5	0.30
	CCR5.0MC3	5.0	Internal	Internal	4.5	5.5	0.38
	CCR6.6MC3	6.6	Internal	Internal	4.5	5.5	0.32
Kyocera Corp.	KBR-2.0MS	2.0	82	82	4.5	5.5	1.2
	KBR-2.7MS	2.7	68	68	4.5	5.5	0.8
	KBR-3.2MS	3.2	47	47	4.5	5.5	0.3
	KBR-5.0MSA	5.0	33	33	4.5	5.5	0.4
	KBR-6.6M	6.6	33	33	4.5	5.5	0.2
Murata Mfg. Co., Ltd.	CSA5.00MG	5.0	30	30	4.5	5.5	0.13
	CST5.00MGW	5.0	Internal	Internal	4.5	5.5	0.13
	CSA6.60MTZ	6.6	30	30	4.5	5.5	0.10
	CST6.60MTW	6.6	Internal	Internal	4.5	5.5	0.10

Cautions 1. Connect the oscillation circuit as closely to the X1 and X2 pins as possible.
2. Do not wire any other signal lines in the area indicated by the dotted line in the above figure.
3. Thoroughly evaluate the matching between the μPD703000 and oscillator.

(b) External clock input

X1   X2
         Open

External clock

Caution Input the voltage at the CMOS level to the X1 pin.

DC Characteristics **(T_A = –40 to +85°C, V_{DD} = 5.0 V±10%, V_{SS} = 0 V) :** μ**PD703000GC-25**

(T_A = –20 to +70°C, V_{DD} = 5.0 V±10%, V_{SS} = 0 V) : μ**PD703000GC-33**

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high		V_{IH}	X1, except **Note 1**	2.2		V_{DD}	V
			Note 1	0.8 V_{DD}		V_{DD}	V
Input voltage, low		V_{IL}	X1, except **Note 1**	0		+0.8	V
			Note 1	0		0.2 V_{DD}	V
X1 clock input voltage, high		V_{XH}	Direct mode	0.8 V_{DD}		V_{DD}	V
			PLL mode	0.8 V_{DD}		V_{DD}	V
X1 clock input voltage, low		V_{XL}	Direct mode	0		0.6	V
			PLL mode	0		0.6	V
Schmitt trigger input		V_T^+	**Note 1** Rising		3.0		V
threshold voltage		V_T^-	**Note 1** Falling		2.0		V
Schmitt trigger input hysteresis width		$V_T^+ - V_T^-$	**Note 1**	0.5			V
Output voltage, high		V_{OH}	I_{OH} = –2.5mA	0.7V_{DD}			V
			I_{OH} = –100μA	V_{DD}–0.4			V
Output voltage, low		V_{OL}	I_{OL} = 2.5 mA			0.45	V
Input leakage current, high		I_{LIH}	V_I = V_{DD}			10	μA
Input leakage current, low		I_{LIL}	V_I = 0 V			–10	μA
Output leakage current, high		I_{LOH}	V_O = V_{DD}			10	μA
Output leakage current, low		I_{LOL}	V_O = 0V			–10	μA
Supply current	Operating	I_{DD1}	Direct mode		$1.5 \times \phi + 5$	$1.8 \times \phi + 10$	mA
			PLL mode		$1.6 \times \phi + 7$	$2.0 \times \phi + 13$	mA
	HALT	I_{DD2}	Direct mode		$0.5 \times \phi + 3$	$0.7 \times \phi + 10$	mA
			PLL mode		$0.6 \times \phi + 5$	$0.9 \times \phi + 13$	mA
	IDLE	I_{DD3}	Direct mode		$8 \times \phi + 300$	$10 \times \phi + 500$	μA
			PLL mode		$0.1 \times \phi + 2$	$0.2 \times \phi + 3$	mA
	STOP	I_{DD4}	**Note 2**		1	50	μA
			Note 3			200	μA

Notes 1. $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/
   INTP03, P26, P27, P31/SI, P32/$\overline{\text{SCK}}$, P36, P37, MODE0, MODE1, CKSEL

2. Operating at 25 MHz: $-40°C \leq T_A \leq +50°C$
   Operating at 33 MHz: $-20°C \leq T_A \leq +50°C$

3. Operating at 25 MHz: $50°C < T_A \leq 85°C$
   Operating at 33 MHz: $50°C < T_A \leq 70°C$

Remarks 1. TYP. value is a value for reference at $T_A = 25°C$, $V_{DD} = 5.0$ V.

2. ϕ: internal operating clock frequency

Data Retention Characteristics (TA = −40 to +85°C) : μPD703000GC-25
                                   (TA = −20 to +70°C) : μPD703000GC-33

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Data hold voltage	V$_{DDDR}$	STOP mode		1.5		5.5	V
Data hold current	I$_{DDDR}$	V$_{DD}$ = V$_{DDDR}$	**Note 1**		0.2V$_{DDDR}$	50	μA
			Note 2		0.2V$_{DDDR}$	200	μA
Supply voltage rise time	t$_{RVD}$			200			μs
Supply voltage fall time	t$_{FVD}$			200			μs
Supply voltage hold time (vs. STOP mode setting)	t$_{HVD}$			0			ms
STOP mode releasing signal input time	t$_{DREL}$			0			ns
Data hold input voltage, high	V$_{IHDR}$	**Note 3**		0.9V$_{DDDR}$		V$_{DDDR}$	V
Data hold input voltage, low	V$_{ILDR}$	**Note 3**		0		0.1V$_{DDDR}$	V

Notes 1.   Operating at 25 MHz: −40°C ≤ TA ≤ +50°C
                Operating at 33 MHz: −20°C ≤ TA ≤ +50°C
     2.   Operating at 25 MHz: 50°C < TA ≤ 85°C
   Operating at 33 MHz: 50°C < TA ≤ 70°C
     3. $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through
                P24/INTP03, P26, P27, P31/SI, P32/$\overline{\text{SCK}}$, P36, P37, MODE0, MODE1, CKSEL, X1

Remark   TYP. value is a value for reference at TA = 25°C, V$_{DD}$ = 5.0 V.

AC Characteristics (T$_A$ = –40 to +85°C, V$_{DD}$ = 5.0 V$\pm$10%, V$_{SS}$ = 0 V): μ**PD703000GC-25**

(T$_A$ = –20 to +70°C, V$_{DD}$ = 5.0 V$\pm$10%, V$_{SS}$ = 0 V): μ**PD703000GC-33**

AC test input waveform

(a) RESET, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/SCK, P36, P37, MODE0, MODE1, CKSEL, X1

```
V_DD ──────────╲      /─ 0.8 V_DD          0.8 V_DD ─╲      /──────────
                 ╲    /                               ╲    /
                  ╳──── →  Test point  ← ──────────────╳
                 /    ╲                               /    ╲
 0 V ──────────/      ╲─ 0.2 V_DD          0.2 V_DD ─/      ╲──────────
```

(b) Other than (a) above

```
2.4 V ─────────╲      /─ 2.2 V              2.2 V ─╲      /──────────
                ╲    /                              ╲    /
                 ╳──── →  Test point  ← ─────────────╳
                /    ╲                              /    ╲
0.4 V ─────────/      ╲─ 0.8 V              0.8 V ─/      ╲──────────
```

AC test output test point

```
───────────────╲      /─ 2.2 V              2.2 V ─╲      /──────────
                ╲    /                              ╲    /
                 ╳──── →  Test point  ← ─────────────╳
                /    ╲                              /    ╲
───────────────/      ╲─ 0.8 V              0.8 V ─/      ╲──────────
```

Load condition

```
    ┌──────────────────┐
    │                  │
    │     DUT          │──────┬──────
    │ (tested device)  │      │
    │                  │     ═╪═  C_L = 50 pF
    └──────────────────┘      │
                             ─┴─
                             ///
```

Caution If the load capacitance exceeds 50 pF due to the configuration of the circuit, keep the load capacitance of this device to within 50 pF by using a buffer.

(1) Clock timing

Parameter	Symbol		Conditions	μPD703000-25		μPD703000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
X1 input cycle	<1>	t_{CYX}	Direct mode	20	DC	15	DC	ns
			PLL mode	200	315	150	334	ns
X1 input high-level width	<2>	t_{WXH}	Direct mode	7		6		ns
			PLL mode	80		60		ns
X1 input low-level width	<3>	t_{WXL}	Direct mode	7		6		ns
			PLL mode	80		60		ns
X1 input rise time	<4>	t_{XR}	Direct mode		7		7	ns
			PLL mode		15		10	ns
X1 input fall time	<5>	t_{XF}	Direct mode		7		7	ns
			PLL mode		15		10	ns
CPU operating frequency	–	ϕ		0	25	0	33	MHz
CLKOUT output cycle	<6>	t_{CYK}		40	DC	30	DC	ns
CLKOUT high-level width	<7>	t_{WKH}		0.5T–5		0.5T–5		ns
CLKOUT low-level width	<8>	t_{WKL}		0.5T–5		0.5T–5		ns
CLKOUT rise time	<9>	t_{KR}			5		5	ns
CLKOUT fall time	<10>	t_{KF}			5		5	ns
X1↓ →CLKOUT delay time	<11>	t_{DXK}	Direct mode	3	17	3	17	ns

Remark   T = t_{CYK}

Parameter	Symbol		Condition	μPD703000-25	μPD703000-33	Unit
				TYP.	TYP.	
Self-running oscillation frequency	–	ϕ_P	PLL mode	2.8	2.8	MHz

(2) Input wavefrom

(a) RESET, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/SCK, P36, P37, MODE0, MODE1, CKSEL, X1

Parameter	Symbol		Condition	μPD703000-25		μPD703000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
Input rise time	<12>	t_{IR2}			20		20	ns
Input fall time	<13>	t_{IF2}			20		20	ns

(b) Other than (a) above

Parameter	Symbol		Condition	μPD703000-25		μPD703000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
Input rise time	<14>	t_{IR1}			10		10	ns
Input fall time	<15>	t_{IF1}			10		10	ns

(3) Output waveform (other than CLKOUT)

Parameter	Symbol		Condition	μPD703000-25		μPD703000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
Output rise time	<16>	t_{OR}			10		10	ns
Output fall time	<17>	t_{OF}			10		10	ns
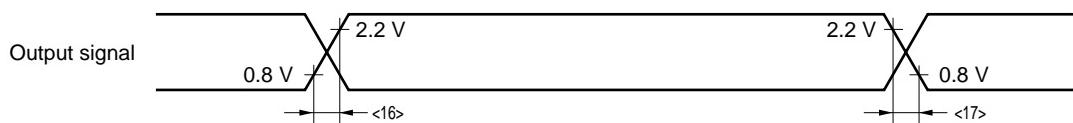
(4) Reset timing

Parameter	Symbol		Condition	μPD703000-25		μPD703000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{RESET}$ high-level width	<18>	t_{WRSH}		500		500		ns
$\overline{RESET}$ low-level width	<19>	t_{WRSL}	On power application and on releasing STOP mode	500+T_{OST}		500-T_{OST}		ns
			Except on power application and on releasing STOP mode	500		500		ns

Remark T_{OST}: Oscillation Stabilization Time

[MEMO]

(5) Read timing (1/2)

Parameter	Symbol		Condition	μPD703000-25		μPD703000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
CLKOUT ↑ → address delay time	<20>	t_{DKA}		3	20	3	20	ns
CLKOUT ↑ → address float delay time	<21>	t_{FKA}		3	15	3	15	ns
CLKOUT ↓ → ASTB delay time	<22>	t_{DKST}		3	15	3	15	ns
CLKOUT ↑ → $\overline{DSTB}$ delay time	<23>	t_{DKD}		3	15	3	15	ns
CLKOUT ↑ → status delay time	<24>	t_{DKS}		3	15	3	15	ns
Data input setup time (vs. CLKOUT ↑)	<25>	t_{SIDK}		5		5		ns
Data input hold time (vs. CLKOUT ↑)	<26>	t_{HKID}		5		5		ns
$\overline{WAIT}$ setup time (vs. CLKOUT ↓)	<27>	t_{SWTK}		5		5		ns
$\overline{WAIT}$ hold time (vs. CLKOUT ↓)	<28>	t_{HKWT}		5		5		ns
Address hold time (vs. CLKOUT ↑)	<29>	t_{HKA}		0		0		ns
Address setup time (vs. ASTB ↓)	<30>	t_{SAST}		0.5T−10		0.5T−10		ns
Address hold time (vs. ASTB ↓)	<31>	t_{HSTA}		0.5T−10		0.5T−10		ns
$\overline{DSTB}$ ↓ → address float delay time	<32>	t_{FDA}			0		0	ns
Data input setup time (vs. address)	<33>	t_{SAID}			(2+n)T−20		(2+n)T−20	ns
Data input setup time (vs. $\overline{DSTB}$ ↓)	<34>	t_{SDID}			(1+n)T−20		(1+n)T−20	ns
ASTB ↓ → $\overline{DSTB}$ ↓ delay time	<35>	t_{DSTD}		0.5T−10		0.5T−10		ns
Data input hold time (vs. DSTB ↑)	<36>	t_{HDID}		0		0		ns
$\overline{DSTB}$ ↑ → address output delay time	<37>	t_{DDA}		(1+i)T		(1+i)T		ns
$\overline{DSTB}$ ↑ → ASTB ↑ delay time	<38>	t_{DDSTH}		0.5T−10		0.5T−10		ns
$\overline{DSTB}$ ↑ → ASTB ↓ delay time	<39>	t_{DDSTL}		(1.5+i)T−10		(1.5+i)T−10		ns
Status setup time (vs. ASTB ↓)	<40>	t_{SSST}		0.5T−10		0.5T−10		ns
Status hold time (vs. ASTB ↑)	<41>	t_{HSTS}		0.5T−10		0.5T−10		ns
$\overline{DSTB}$ low-level width	<42>	t_{WDL}		(1+n)T−10		(1+n)T−10		ns
ASTB high-level width	<43>	t_{WSTH}		T−10		T−10		ns
$\overline{WAIT}$ setup time (vs. address)	<44>	t_{SAWT1}	n≥1		1.5T−20		1.5T−20	ns
	<45>	t_{SAWT2}			(1.5+n)T−20		(1.5+n)T−20	ns
$\overline{WAIT}$ hold time (vs. address)	<46>	t_{HAWT1}	n≥1	(0.5+n)T		(0.5+n)T		ns
	<47>	t_{HAWT2}		(1.5+n)T		(1.5+n)T		ns
$\overline{WAIT}$ setup time (vs. ASTB ↓)	<48>	t_{SSTWT1}	n≥1		T−15		T−15	ns
	<49>	t_{SSTWT2}			(1+n)T−15		(1+n)T−15	ns
WAIT hold time (vs. ASTB ↓)	<50>	t_{HSTWT1}	n≥1	nT		nT		ns
	<51>	t_{HSTWT2}		(1+n)T		(1+n)T		ns

Remarks 1. T = t_{CYK}

        2. n indicates the number of wait clocks inserted in a bus cycle. The sampling timing varies when programmable wait states are inserted.

        3. i indicates the number of idle states (0 or 1) inserted in the read cycle.

        4. Satisfy at least one of the data input hold times t_{HKID} (<26>) and t_{HDID} (<36>).

(5) Read timing (2/2): 1 wait

Note R/$\overline{\text{W}}$ (output), $\overline{\text{UBEN}}$ (output), $\overline{\text{LBEN}}$ (output)

Remark The dotted line indicates a high-impedance state.

(6) Write timing (1/2)

Parameter	Symbol		Condition	μPD703000-25		μPD703000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
CLKOUT ↑ → address delay time	<20>	t_{DKA}		3	20	3	20	ns
CLKOUT ↓ → ASTB delay time	<22>	t_{DKST}		3	15	3	15	ns
CLKOUT ↑ → $\overline{DSTB}$ delay time	<23>	t_{DKD}		3	15	3	15	ns
CLKOUT ↑ → status delay time	<24>	t_{DKS}		3	15	3	15	ns
$\overline{WAIT}$ setup time (vs. CLKOUT ↓)	<27>	t_{SWTK}		5		5		ns
$\overline{WAIT}$ hold time (vs. CLKOUT ↓)	<28>	t_{HKWT}		5		5		ns
Address hold time (vs. CLKOUT ↑)	<29>	t_{HKA}		0		0		ns
Address setup time (vs. ASTB ↓)	<30>	t_{SAST}		0.5T−10		0.5T−10		ns
Address hold time (vs. ASTB ↓)	<31>	t_{HSTA}		0.5T−10		0.5T−10		ns
ASTB ↓ → $\overline{DSTB}$ ↓ delay time	<35>	t_{DSTD}		0.5T−10		0.5T−10		ns
$\overline{DSTB}$ ↑ → ASTB ↑ delay time	<38>	t_{DDSTH}		0.5T−10		0.5T−10		ns
Status setup time (vs. ASTB ↓)	<40>	t_{SSST}		0.5T−10		0.5T−10		ns
Status hold time (vs. ASTB ↑)	<41>	t_{HSTS}		0.5T−10		0.5T−10		ns
$\overline{DSTB}$ low-level width	<42>	t_{WDL}		(1+n)T−10		(1+n)T−10		ns
ASTB high-level width	<43>	t_{WSTH}		T−10		T−10		ns
$\overline{WAIT}$ setup time (vs. address)	<44>	t_{SAWT1}	n≥1		1.5T−20		1.5T−20	ns
	<45>	t_{SAWT2}			(1.5+n)T−20		(1.5+n)T−20	ns
$\overline{WAIT}$ hold time (vs. address)	<46>	t_{HAWT1}	n≥1	(0.5+n)T		(0.5+n)T		ns
	<47>	t_{HAWT2}		(1.5+n)T		(1.5+n)T		ns
$\overline{WAIT}$ setup time (vs. ASTB ↓)	<48>	t_{SSTWT1}	n≥1		T−15		T−15	ns
	<49>	t_{SSTWT2}			(1+n)T−15		(1+n)T−15	ns
$\overline{WAIT}$ hold time (vs. ASTB ↓)	<50>	t_{HSTWT1}	n≥1	nT		nT		ns
	<51>	t_{HSTWT2}		(1+n)T		(1+n)T		ns
CLKOUT ↑ → data output delay time	<52>	t_{DKOD}			20		20	ns
$\overline{DSTB}$ ↓ → data output delay time	<53>	t_{DDOD}			10		10	ns
Data output hold time (vs. CLKOUT ↑)	<54>	t_{HKOD}		0		0		ns
Data output setup time (vs. $\overline{DSTB}$ ↑)	<55>	t_{SODD}		(1+n)T−15		(1+n)T−15		ns
Data output hold time (vs. $\overline{DSTB}$ ↑)	<56>	t_{HDOD}		T-10		T-10		ns

Remarks 1. T = t_{CYK}

        2. n indicates the number of wait clocks inserted in a bus cycle. The sampling timing varies when programmable wait states are inserted.

(6) Write timing (2/2): 1 wait

Note R/$\overline{\text{W}}$ (output), $\overline{\text{UBEN}}$ (output), $\overline{\text{LBEN}}$ (output)

Remark The dotted line indicates a high-impedance state.
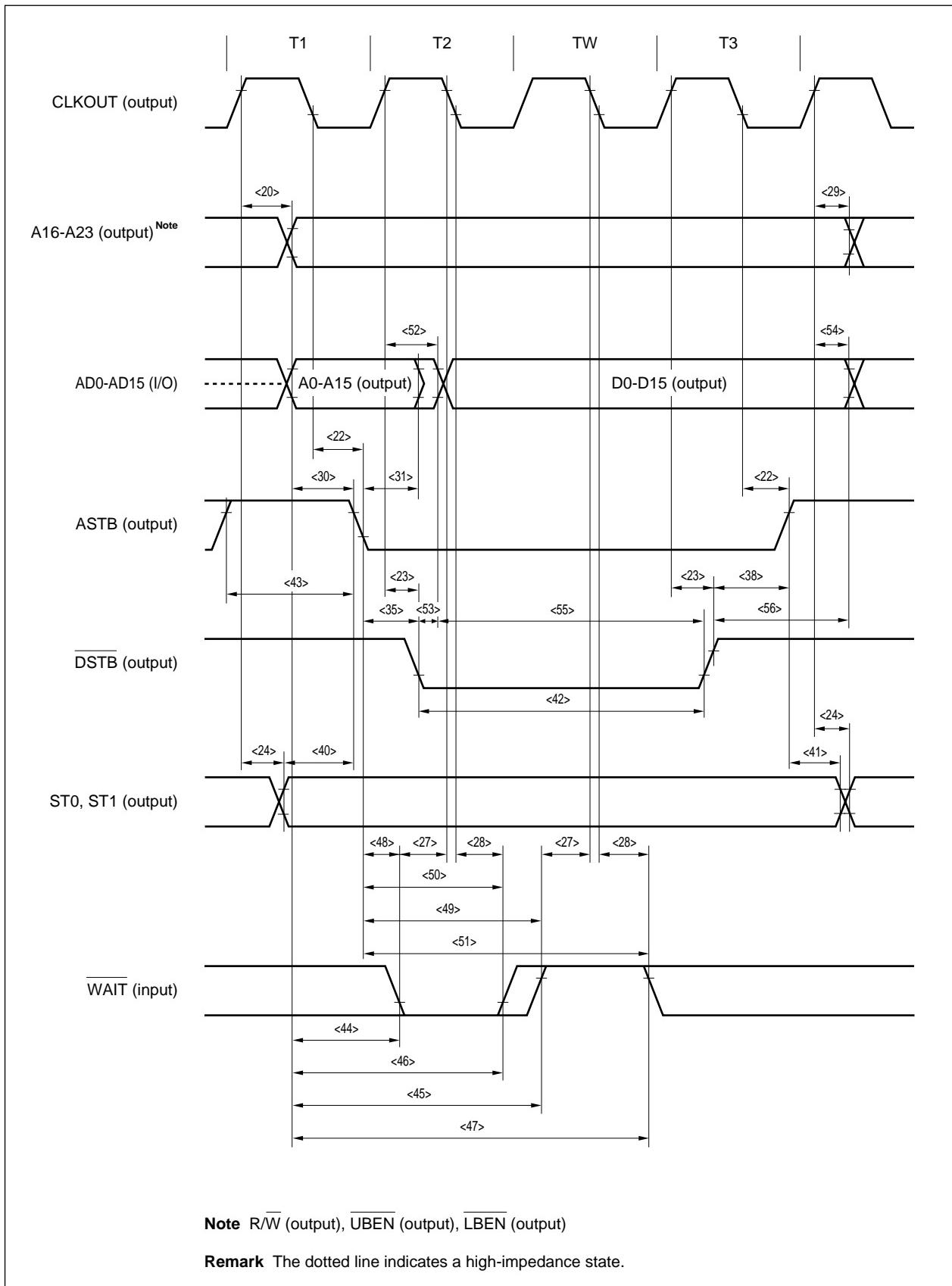
(7) Bus hold timing (1/2)

Parameter	Symbol		Condition	μPD703000-25		μPD703000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{\text{HLDRQ}}$ setup time (vs. CLKOUT $\downarrow$)	<57>	t_{SHQK}		5		5		ns
$\overline{\text{HLDRQ}}$ hold time (vs. CLKOUT $\downarrow$)	<58>	t_{HKHQ}		5		5		ns
CLKOUT $\uparrow \rightarrow \overline{\text{HLDAK}}$ delay time	<59>	t_{DKHA}			20		20	ns
$\overline{\text{HLDRQ}}$ high-level width	<60>	t_{WHQH}		T+10		T+10		ns
$\overline{\text{HLDAK}}$ low-level width	<61>	t_{WHAL}		T−10		T−10		ns
CLKOUT $\uparrow \rightarrow$ bus float delay time	<62>	t_{DKF}			20		20	ns
$\overline{\text{HLDAK}} \uparrow \rightarrow$ bus output delay time	<63>	t_{DHAC}		−3		−3		ns
$\overline{\text{HLDRQ}} \downarrow \rightarrow \overline{\text{HLDAK}} \downarrow$ delay time	<64>	t_{DHQHA1}			(2n+7.5)T+20		(2n+7.5)T+20	ns
$\overline{\text{HLDRQ}} \uparrow \rightarrow \overline{\text{HLDAK}} \uparrow$ delay time	<65>	t_{DHQHA2}		0.5T	1.5T+20	0.5T	1.5T+20	ns

★ (marks the CLKOUT $\uparrow \rightarrow$ bus float delay time row)

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in a bus cycle. The sampling timing varies when programmable wait states are inserted.

60

(7) Bus hold timing (2/2)

Note $\overline{\text{UBEN}}$ (output), $\overline{\text{LBEN}}$ (output)

Remark The dotted line indicates a high-impedance state.
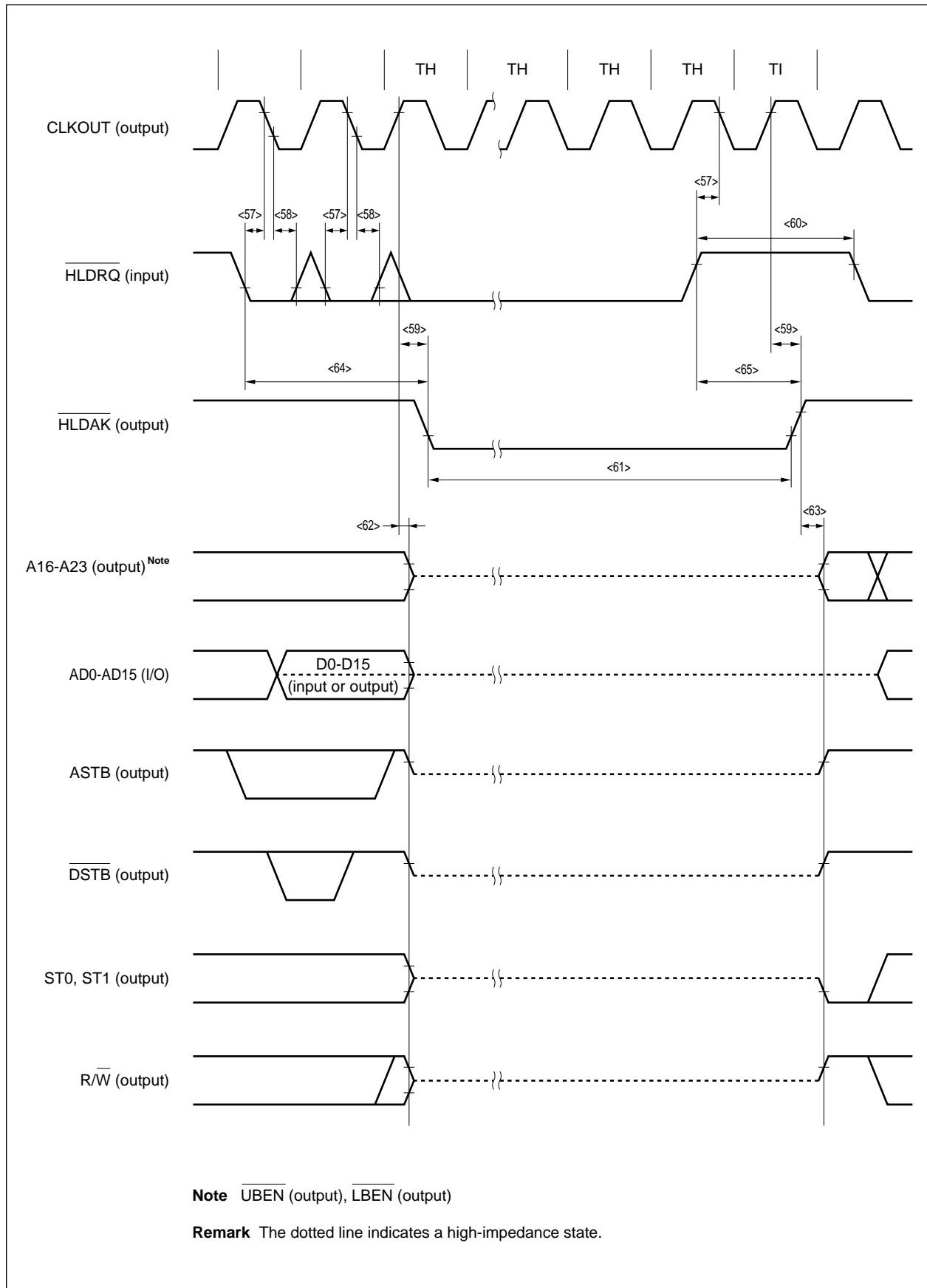
(8) Interrupt timing

Parameter	Symbol		Condition	μPD703000-25		μPD703000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
NMI high-level width	<66>	t_{WNIH}		500		500		ns
NMI low-level width	<67>	t_{WNIL}		500		500		ns
INTPn high-level width	<68>	t_{WITH}	n=00, 01, 02, 03, 10, 11, 12, 13	3T+10		3T+10		ns
INTPn low-level width	<69>	t_{WITL}	n=00, 01, 02, 03, 10, 11, 12, 13	3T+10		3T+10		ns

Remark   T = t_{CYK}

Remark n = 00, 01, 02, 03, 10, 11, 12, 13

(9) CSI timing

(a) Master mode

Parameter	Symbol		Condition	μPD703000-25		μPD703000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{SCK}$ cycle	<70>	t$_{CYSK}$	Output	160		120		ns
$\overline{SCK}$ high-level width	<71>	t$_{WSKH}$	Output	0.5t$_{CYSK}$−20		0.5t$_{CYSK}$−20		ns
$\overline{SCK}$ low-level width	<72>	t$_{WSKL}$	Output	0.5t$_{CYSK}$−20		0.5t$_{CYSK}$−20		ns
SI setup time (vs. $\overline{SCK}$ ↑)	<73>	t$_{SSISK}$		30		30		ns
SI hold time (vs. $\overline{SCK}$ ↑)	<74>	t$_{HSKSI}$		0		0		ns
SO output delay time (vs. $\overline{SCK}$ ↓)	<75>	t$_{DSKSO}$			18		18	ns
SO output hold time (vs. $\overline{SCK}$ ↑)	<76>	t$_{HSKSO}$		0.5t$_{CYSK}$−5		0.5t$_{CYSK}$−5		ns

(b) Slave mode

Parameter	Symbol		Condition	μPD703000-25		μPD703000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{SCK}$ cycle	<70>	t$_{CYSK}$	Input	160		120		ns
$\overline{SCK}$ high-level width	<71>	t$_{WSKH}$	Input	50		30		ns
$\overline{SCK}$ low-level width	<72>	t$_{WSKL}$	Input	50		30		ns
SI setup time (vs. $\overline{SCK}$ ↑)	<73>	t$_{SSISK}$		10		10		ns
SI hold time (vs. $\overline{SCK}$ ↑)	<74>	t$_{HSKSI}$		10		10		ns
SO output delay time (vs. $\overline{SCK}$ ↓)	<75>	t$_{DSKSO}$			30		30	ns
SO output hold time (vs. $\overline{SCK}$ ↑)	<76>	t$_{HSKSO}$		t$_{WSKH}$		t$_{WSKH}$		ns

Remark The dotted line indicates a high-impedance state.
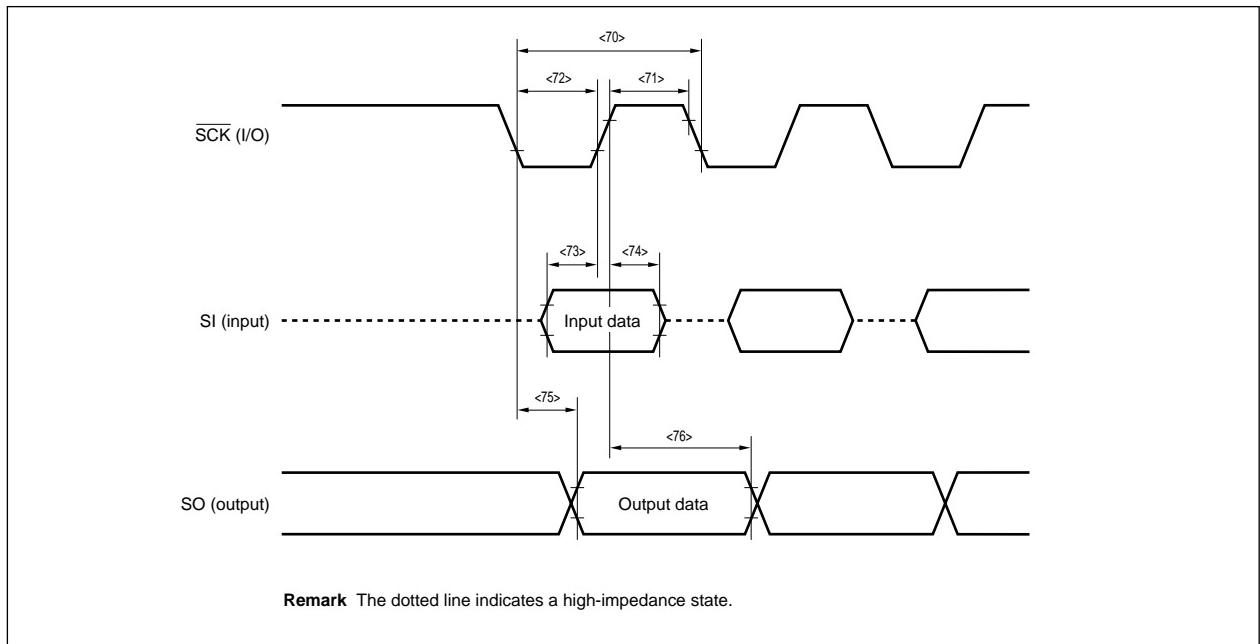
(10) RPU timing

Parameter	Symbol		Condition	μPD703000-25		μPD703000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
TI1 high-level width	<77>	t$_{WTIH}$		3T+10		3T+10		ns
TI1 low-level width	<78>	t$_{WTIL}$		3T+10		3T+10		ns
TCLR1 high-level width	<79>	t$_{WTCH}$		3T+10		3T+10		ns
TCLR1 low-level width	<80>	t$_{WTCL}$		3T+10		3T+10		ns

Remark T = t$_{CYK}$
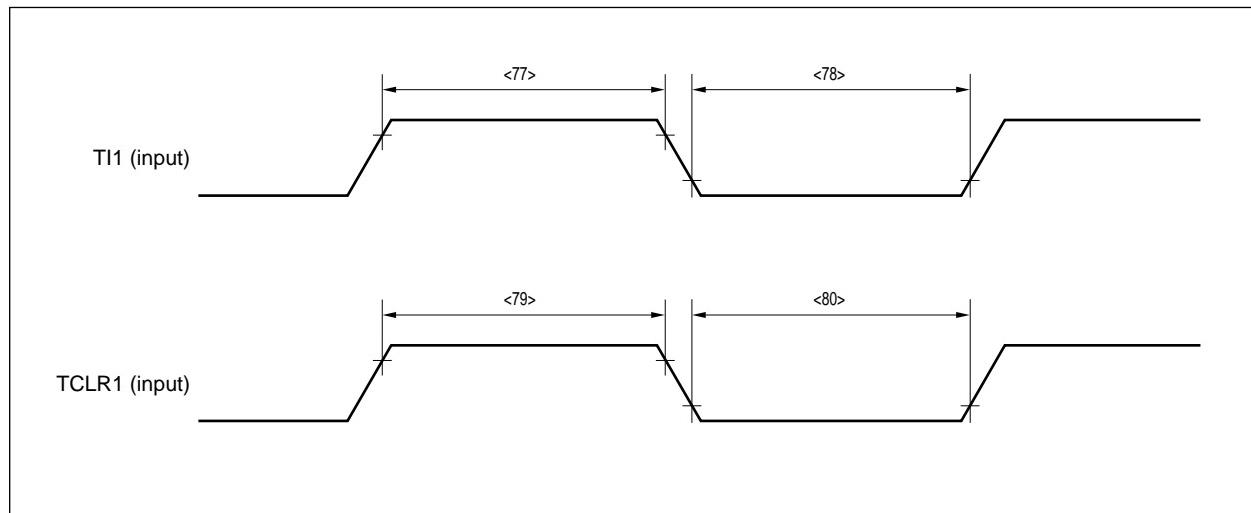
12.2 When V$_{DD}$ = 3.0 to 3.6 V

Absolute Maximum Ratings (T$_A$ = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V$_{DD}$	V$_{DD}$ pin	−0.5 to +7.0	V
	CV$_{DD}$	CV$_{DD}$ pin	−0.5 to +7.0	V
	CV$_{SS}$	CV$_{SS}$ pin	−0.5 to +0.5	V
Input voltage	V$_{I1}$	Except X1 pin, V$_{DD}$ = 3.0 to 3.6 V	−0.5 to V$_{DD}$ +0.3	V
Clock input voltage	Vx	X1 pin, V$_{DD}$ = 3.0 to 3.6 V	−0.5 to V$_{DD}$ +1.0	V
Output current, low	I$_{OL}$	1 pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I$_{OH}$	1 pin	−4.0	mA
		Total of all pins	−100	mA
Output voltage	V$_O$	V$_{DD}$ = 3.0 to 3.6 V	−0.5 to V$_{DD}$ +0.3	V
Operating temperature	T$_A$		−20 to +70	°C
Storage temperature	T$_{stg}$		−65 to +150	°C

Cautions 1. Do not directly connect to the output (or I/O) pins of an IC product, or to the V$_{DD}$, V$_{CC}$, or GND.

Open-drain pins and open-collector pins may be connected each other however. Moreover, an external circuit that is designed so as to avoid output contention can be directly connected to a pin that goes into a high-impedance state.

2. If even one of the parameters exceeds the absolute maximum rating even momentarily, the quality of the product may be affected. The absolute maximum ratings specify the values exceeding which the product may be physically damaged. Never exceed these ratings when using the product.

The specifications and conditions shown in DC and AC Characteristics below specify the range in which the product operates normally and the product quality is guaranteed.

**Capacitance (T$_A$ = 25°C, V$_{DD}$ = V$_{SS}$ = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C$_I$	fc = 1 MHz			15	pF
I/O capacitance	C$_{IO}$	0 V for pins other than test pin			15	pF
Output capacitance	C$_O$				15	pF

Operating Conditions

| Operation Mode	Internal Operating Clock Frequency (ϕ)	Operating Temperature (T$_A$)	Supply Voltage (V$_{DD}$)
Direct mode	0 to 12 MHz	−20 to +70°C	3.0 to 3.6 V
PLL mode	Self-running oscillation frequency to 12 MHz	−20 to +70°C	3.0 to 3.6 V

Recommended Oscillation Circuit

(a) Connecting ceramic resonator
   (T_A = −40 to +85°C)

Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant		Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
TDK Corp.	FCR2.0MC3	2.0	Internal	Internal	3.0	3.6	0.26
	CCR3.2MC3	3.2	Internal	Internal	3.0	3.6	0.62
Murata Mfg. Co., Ltd.	CSA2.00MG	2.0	30	30	3.0	3.6	0.24
	CST2.00MG	2.0	Internal	Internal	3.0	3.6	0.24
	CSA2.70MG	2.7	30	30	3.0	3.6	0.16
	CST2.70MGW	2.7	Internal	Internal	3.0	3.6	0.16
	CSA3.20MG	3.2	30	30	3.0	3.6	0.13
	CST3.20MGW	3.2	Internal	Internal	3.0	3.6	0.13

Cautions 1. Connect the oscillation circuit as closely to the X1 and X2 pins as possible.
   2. Do not wire any other signal lines in the area indicated by the dotted line in the above figure.
   3. Thoroughly evaluate the matching between the μPD703000 and oscillator.

(b) External clock input
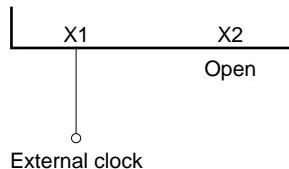
Caution Input the voltage at the CMOS level to the X1 pin.

DC Characteristics (T$_A$ = –20 to +70°C, V$_{DD}$ = 3.0 to 3.6 V, V$_{SS}$ = 0 V)

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high		V$_{IH}$	Except X1 and **Note**	0.7 V$_{DD}$		V$_{DD}$	V
			Note	0.8 V$_{DD}$		V$_{DD}$	V
Input voltage, low		V$_{IL}$	Except X1 and **Note**	0		0.2 V$_{DD}$	V
			Note	0		0.2 V$_{DD}$	V
X1 clock input voltage, high		V$_{XH}$	Direct mode	0.8 V$_{DD}$		V$_{DD}$	V
			PLL mode	0.8 V$_{DD}$		V$_{DD}$	V
X1 clock input voltage, low		V$_{XL}$	Direct mode	0		0.6	V
			PLL mode	0		0.6	V
Schmitt trigger input threshold voltage		V$_T^+$	**Note**, Rising		3.0		V
		V$_T^-$	**Note**, Falling		2.0		V
Schmitt trigger input hysteresis width		V$_T^+$–V$_T^-$	**Note**	0.5			V
Output voltage, high		V$_{OH}$	I$_{OH}$ = –2.5mA	0.7V$_{DD}$			V
			I$_{OH}$ = –100μA	V$_{DD}$–0.5			V
Output voltage, low		V$_{OL}$	I$_{OL}$ = 2.5 mA			0.45	V
Input leakage current, high		I$_{LIH}$	V$_I$ = V$_{DD}$			10	μA
Input leakage current, low		I$_{LIL}$	V$_I$ = 0 V			–10	μA
Output leakage current, high		I$_{LOH}$	V$_O$ = V$_{DD}$			10	μA
Output leakage current, low		I$_{LOL}$	V$_O$ = 0V			–10	μA
Supply current	Operating	I$_{DD1}$	Direct mode		1.0 × φ+3.5	1.2 × φ+6.5	mA
			PLL mode		1.1 × φ+5	1.3 × φ+8.5	mA
	HALT	I$_{DD2}$	Direct mode		0.3 × φ+2	0.5 × φ+6.5	mA
			PLL mode		0.4 × φ+3.5	0.6 × φ+8.5	mA
	IDLE	I$_{DD3}$	Direct mode		5.3 × φ+200	6.5 × φ+325	μA
			PLL mode		0.07 × φ+1.5	0.15 × φ+2	mA
	STOP	I$_{DD4}$	–20°C ≤ T$_A$ ≤ +50°C		1	40	μA
			50°C < T$_A$ ≤ 70°C			200	μA

Note $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/$\overline{\text{SCK}}$, P36, P37, MODE0, MODE1, CKSEL

**Remarks 1.** TYP. value is a value for reference at T$_A$ = 25°C, V$_{DD}$ = 3.3 V.
          2. φ: internal operating clock frequency

Data Retention Characteristics (T$_A$ = −20 to +70°C)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Data hold voltage	V$_{DDDR}$	STOP mode		1.5		3.6	V
Data hold current	I$_{DDDR}$	V$_{DD}$ = V$_{DDDR}$	−20°C ≤ T$_A$ ≤ +50°C		0.2V$_{DDDR}$	40	μA
			50°C < T$_A$ ≤ 70°C		0.2V$_{DDDR}$	200	μA
Supply voltage rise time	t$_{RVD}$			200			μs
Supply voltage fall time	t$_{FVD}$			200			μs
Supply voltage hold time (vs. STOP mode setting)	t$_{HVD}$			0			ms
STOP mode releasing signal input time	t$_{DREL}$			0			ns
Data hold input voltage, high	V$_{IHDR}$	**Note**		0.9V$_{DDDR}$		V$_{DDDR}$	V
Data hold input voltage, low	V$_{ILDR}$	**Note**		0		0.1V$_{DDDR}$	V

Note $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/$\overline{\text{SCK}}$, P36, P37, MODE0, MODE1, CKSEL, X1

Remark TYP. value is a value for reference at T$_A$ = 25°C, V$_{DD}$ = 3.3 V.
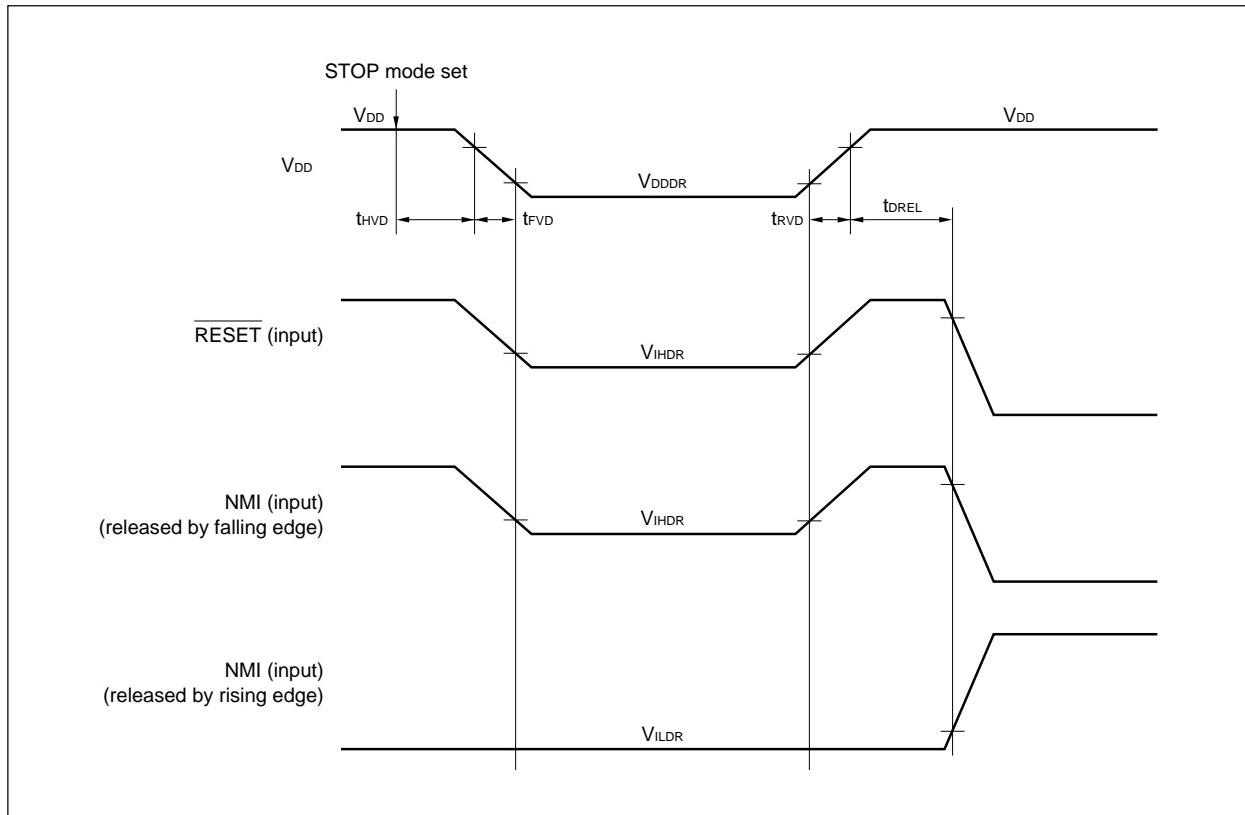
AC Characteristics (T$_A$ = −20 to +70°C, V$_{DD}$ = 3.0 to 3.6 V, V$_{SS}$ = 0 V)

AC test input waveform

(a) $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/$\overline{\text{SCK}}$, P36, P37, MODE0, MODE1, CKSEL, X1
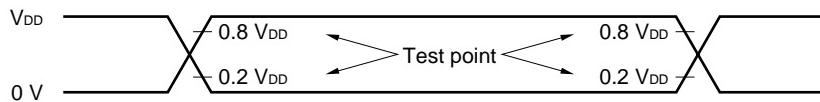
(b) Other than (a) above
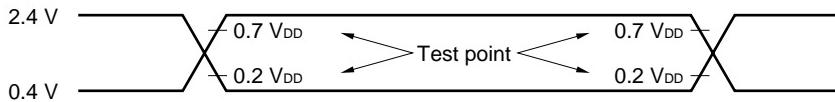
**AC test output test point**
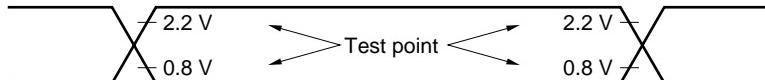
Load condition
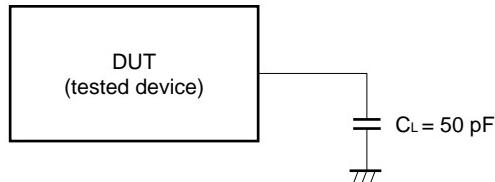
Caution If the load capacitance exceeds 50 pF due to the configuration of the circuit, keep the load capacitance of this device to within 50 pF by using a buffer.

(1) Clock timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
X1 input cycle	<1>	t_{CYX}	Direct mode	41	DC	ns
			PLL mode	416	500	ns
X1 input high-level width	<2>	t_{WXH}	Direct mode	7		ns
			PLL mode	170		ns
X1 input low-level width	<3>	t_{WXL}	Direct mode	7		ns
			PLL mode	170		ns
X1 input rise time	<4>	t_{XR}	Direct mode		7	ns
			PLL mode		15	ns
X1 input fall time	<5>	t_{XF}	Direct mode		7	ns
			PLL mode		15	ns
CPU operating frequency	–	ϕ		0	12	MHz
CLKOUT output cycle	<6>	t_{CYK}		82	DC	ns
CLKOUT high-level width	<7>	t_{WKH}		0.5T–15		ns
CLKOUT low-level width	<8>	t_{WKL}		0.5T–15		ns
CLKOUT rise time	<9>	t_{KR}			15	ns
CLKOUT fall time	<10>	t_{KF}			15	ns
X1$\downarrow \rightarrow$CLKOUT delay time	<11>	t_{DXK}	Direct mode	3	30	ns

Remark T = t_{CYK}

Parameter	Symbol		Condition	TYP.	Unit
Self-running oscillation frequency	–	ϕ_P	PLL mode	2.8	MHz
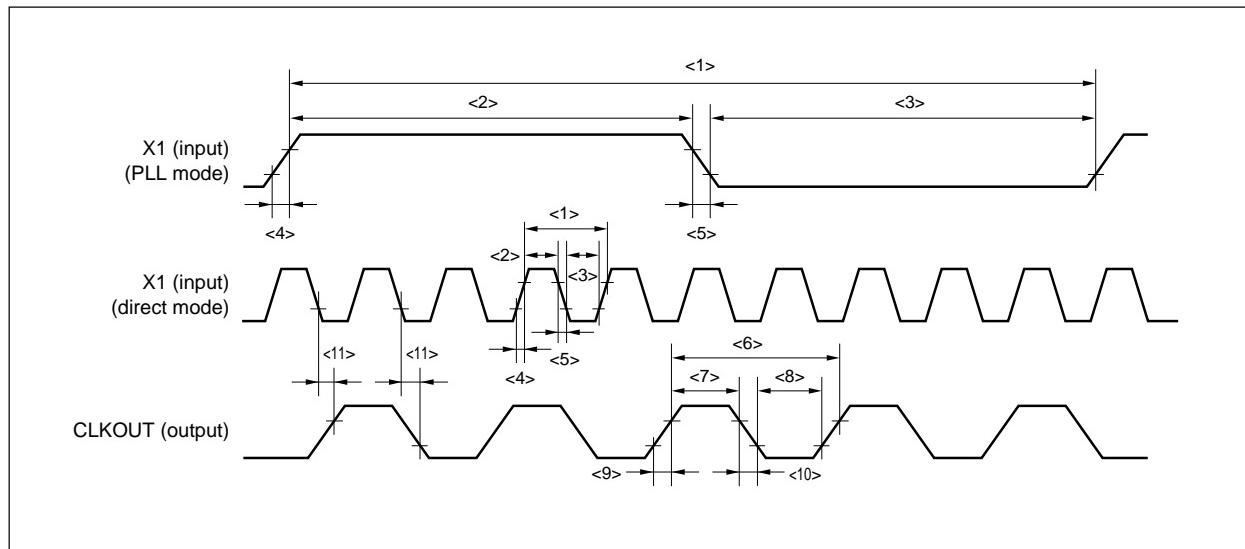
(2) Input waveform

(a) $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/$\overline{\text{SCK}}$, P36, P37, MODE0, MODE1, CKSEL, X1

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Input rise time	<12>	t_{IR2}			20	ns
Input fall time	<13>	t_{IF2}			20	ns
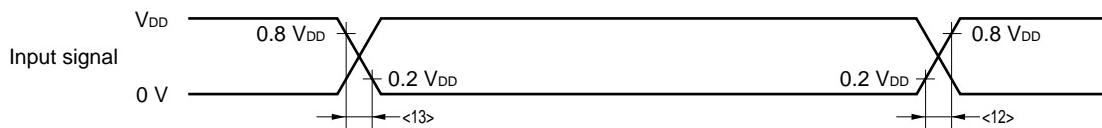
(b) Other than (a) above

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Input rise time	<14>	t_{IR1}			10	ns
Input fall time	<15>	t_{IF1}			10	ns
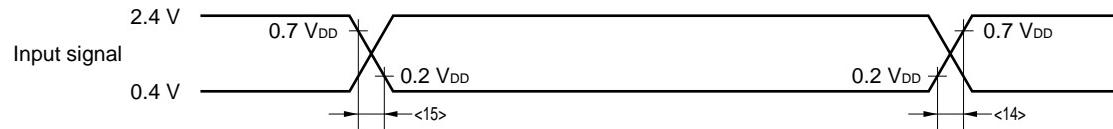
(3) Output waveform (other than CLKOUT)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	<16>	t$_{OR}$			20	ns
Output fall time	<17>	t$_{OF}$			20	ns
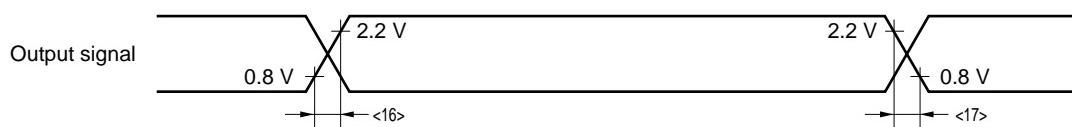
(4) Reset timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	<18>	t$_{WRSH}$		500		ns
$\overline{\text{RESET}}$ low-level width	<19>	t$_{WRSL}$	On power application and on releasing STOP mode	500+T$_{OST}$		ns
			Except on power application and on releasing STOP mode	500		ns

Remark T$_{OST}$: Oscillation Stabilization Time
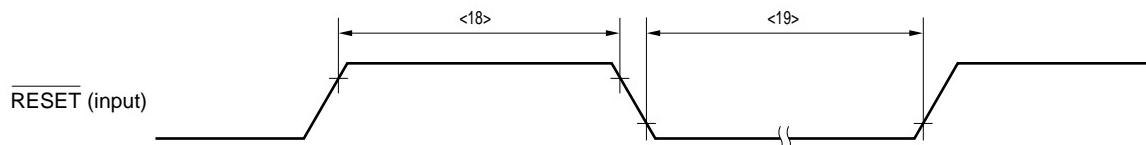
[MEMO]

(5) Read timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CLKOUT $\uparrow \rightarrow$ address delay time	<20>	t_{DKA}		3	32	ns
CLKOUT $\uparrow \rightarrow$ address float delay time	<21>	t_{FKA}		3	32	ns
CLKOUT $\downarrow \rightarrow$ ASTB delay time	<22>	t_{DKST}		3	32	ns
CLKOUT $\uparrow \rightarrow$ $\overline{DSTB}$ delay time	<23>	t_{DKD}		3	32	ns
CLKOUT $\uparrow \rightarrow$ status delay time	<24>	t_{DKS}		3	32	ns
Data input setup time (vs. CLKOUT $\uparrow$)	<25>	t_{SIDK}		5		ns
Data input hold time (vs. CLKOUT $\uparrow$)	<26>	t_{HKID}		5		ns
$\overline{WAIT}$ setup time (vs. CLKOUT $\downarrow$)	<27>	t_{SWTK}		7		ns
$\overline{WAIT}$ hold time (vs. CLKOUT $\downarrow$)	<28>	t_{HKWT}		7		ns
Address hold time (vs. CLKOUT $\uparrow$)	<29>	t_{HKA}		0		ns
Address setup time (vs. ASTB $\downarrow$)	<30>	t_{SAST}		0.5T–25		ns
Address hold time (vs. ASTB $\downarrow$)	<31>	t_{HSTA}		0.5T–15		ns
$\overline{DSTB}$ $\downarrow \rightarrow$ address float delay time	<32>	t_{FDA}			0	ns
Data input setup time (vs. address)	<33>	t_{SAID}			(2+n)T–45	ns
Data input setup time (vs. $\overline{DSTB}$ $\downarrow$)	<34>	t_{SDID}			(1+n)T–35	ns
ASTB $\downarrow \rightarrow$ $\overline{DSTB}$ $\downarrow$ delay time	<35>	t_{DSTD}		0.5T–15		ns
Data input hold time (vs. $\overline{DSTB}$ $\uparrow$)	<36>	t_{HDID}		0		ns
$\overline{DSTB}$ $\uparrow \rightarrow$ address output delay time	<37>	t_{DDA}		(1+i)T		ns
$\overline{DSTB}$ $\uparrow \rightarrow$ ASTB $\uparrow$ delay time	<38>	t_{DDSTH}		0.5T–15		ns
$\overline{DSTB}$ $\uparrow \rightarrow$ ASTB $\downarrow$ delay time	<39>	t_{DDSTL}		(1.5+i)T–15		ns
Status setup time (vs. ASTB $\downarrow$)	<40>	t_{SSST}		0.5T–15		ns
Status hold time (vs. ASTB $\uparrow$)	<41>	t_{HSTS}		0.5T–20		ns
$\overline{DSTB}$ low-level width	<42>	t_{WDL}		(1+n)T–15		ns
ASTB high-level width	<43>	t_{WSTH}		T–20		ns
$\overline{WAIT}$ setup time (vs. address)	<44>	t_{SAWT1}	n≥1		1.5T–50	ns
	<45>	t_{SAWT2}			(1.5+n)T–50	ns
$\overline{WAIT}$ hold time (vs. address)	<46>	t_{HAWT1}	n≥1	(0.5+n)T		ns
	<47>	t_{HAWT2}		(1.5+n)T		ns
$\overline{WAIT}$ setup time (vs. ASTB $\downarrow$)	<48>	t_{SSTWT1}	n≥1		T–35	ns
	<49>	t_{SSTWT2}			(1+n)T–35	ns
$\overline{WAIT}$ hold time (vs. ASTB $\downarrow$)	<50>	t_{HSTWT1}	n≥1	nT		ns
	<51>	t_{HSTWT2}		(1+n)T		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in a bus cycle. The sampling timing varies when programmable wait states are inserted.

3. i indicates the number of idle states (0 or 1) inserted in the read cycle.

4. Satisfy at least one of the data input hold times t_{HKID} (<26>) and t_{HDID} (<36>).

(5) Read timing (2/2): 1 wait

Note R/$\overline{\text{W}}$ (output), $\overline{\text{UBEN}}$ (output), $\overline{\text{LBEN}}$ (output)

Remark The dotted line indicates a high-impedance state.

(6) Write timing (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
CLKOUT $\uparrow \rightarrow$ address delay time	<20>	t_{DKA}		3	32	ns
CLKOUT $\downarrow \rightarrow$ ASTB delay time	<22>	t_{DKST}		3	32	ns
CLKOUT $\uparrow \rightarrow \overline{DSTB}$ delay time	<23>	t_{DKD}		3	32	ns
CLKOUT $\uparrow \rightarrow$ status delay time	<24>	t_{DKS}		3	32	ns
$\overline{WAIT}$ setup time (vs. CLKOUT $\downarrow$)	<27>	t_{SWTK}		7		ns
$\overline{WAIT}$ hold time (vs. CLKOUT $\downarrow$)	<28>	t_{HKWT}		7		ns
Address hold time (vs. CLKOUT $\uparrow$)	<29>	t_{HKA}		0		ns
Address setup time (vs. ASTB $\downarrow$)	<30>	t_{SAST}		0.5T–25		ns
Address hold time (vs. ASTB $\downarrow$)	<31>	t_{HSTA}		0.5T–15		ns
ASTB $\downarrow \rightarrow \overline{DSTB} \downarrow$ delay time	<35>	t_{DSTD}		0.5T–15		ns
$\overline{DSTB} \uparrow \rightarrow$ ASTB $\uparrow$ delay time	<38>	t_{DDSTH}		0.5T–15		ns
Status setup time (vs. ASTB $\downarrow$)	<40>	t_{SSST}		0.5T–15		ns
Status hold time (vs. ASTB $\uparrow$)	<41>	t_{HSTS}		0.5T–20		ns
$\overline{DSTB}$ low-level width	<42>	t_{WDL}		(1+n)T–15		ns
ASTB high-level width	<43>	t_{WSTH}		T–20		ns
$\overline{WAIT}$ setup time (vs. address)	<44>	t_{SAWT1}	n≥1		1.5T–50	ns
	<45>	t_{SAWT2}			(1.5+n)T–50	ns
$\overline{WAIT}$ hold time (vs. address)	<46>	t_{HAWT1}	n≥1	(0.5+n)T		ns
	<47>	t_{HAWT2}		(1.5+n)T		ns
$\overline{WAIT}$ setup time (vs. ASTB $\downarrow$)	<48>	t_{SSTWT1}	n≥1		T–35	ns
	<49>	t_{SSTWT2}			(1+n)T–35	ns
$\overline{WAIT}$ hold time (vs. ASTB $\downarrow$)	<50>	t_{HSTWT1}	n≥1	nT		ns
	<51>	t_{HSTWT2}		(1+n)T		ns
CLKOUT $\uparrow \rightarrow$ data output delay time	<52>	t_{DKOD}			32	ns
$\overline{DSTB} \downarrow \rightarrow$ data output delay time	<53>	t_{DDOD}			20	ns
Data output hold time (vs. CLKOUT $\uparrow$)	<54>	t_{HKOD}		0		ns
Data output setup time (vs. $\overline{DSTB} \uparrow$)	<55>	t_{SODD}		(1+n)T–30		ns
Data output hold time (vs. $\overline{DSTB} \uparrow$)	<56>	t_{HDOD}		T–15		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in a bus cycle. The sampling timing varies when programmable wait states are inserted.

(6) Write timing (2/2): 1 wait

Note R/$\overline{\text{W}}$ (output), $\overline{\text{UBEN}}$ (output), $\overline{\text{LBEN}}$ (output)

Remark The dotted line indicates a high-impedance state.
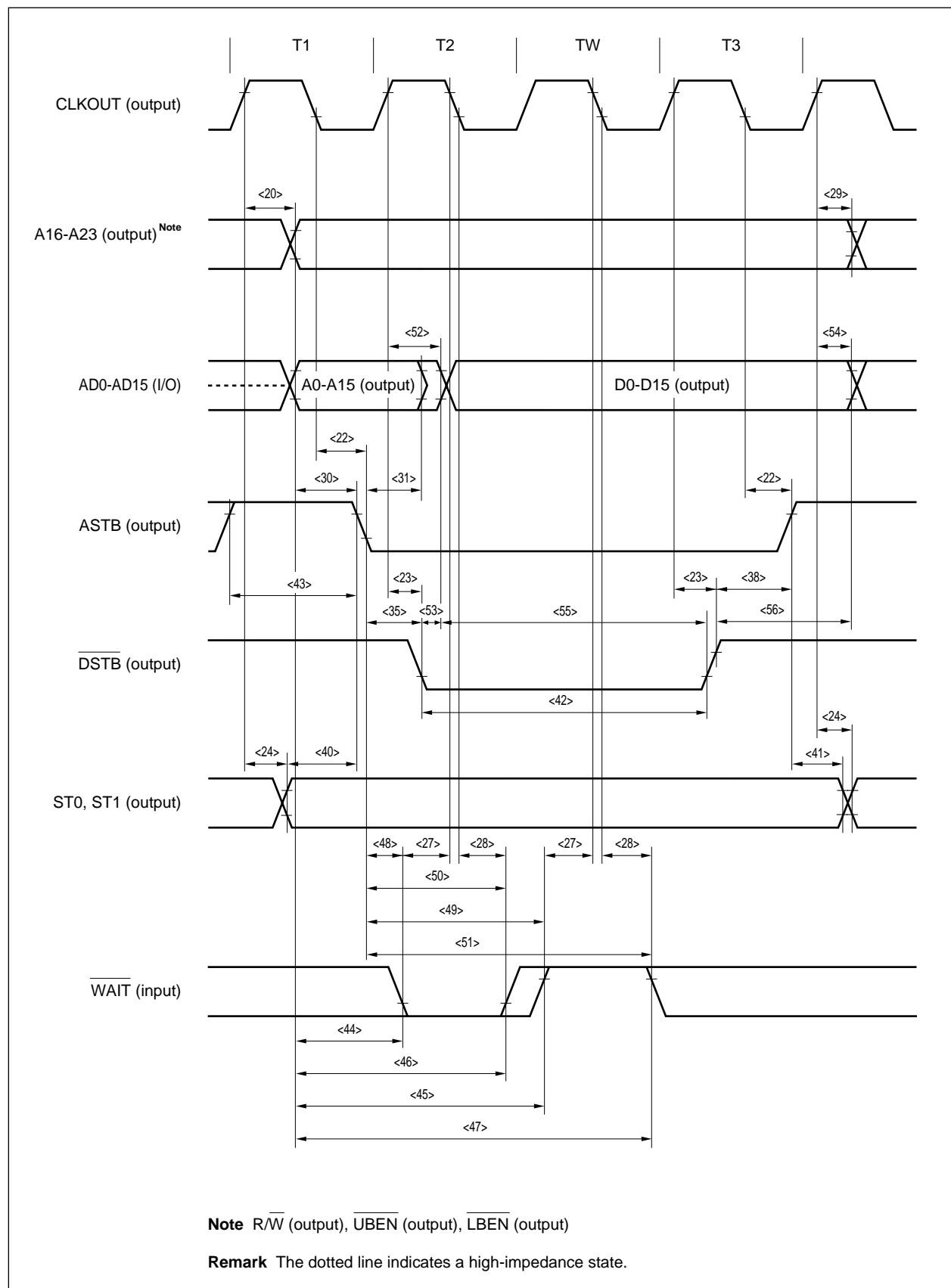
(7) Bus hold timing (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (vs. CLKOUT $\downarrow$)	<57> t$_{SHQK}$		7		ns
$\overline{\text{HLDRQ}}$ hold time (vs. CLKOUT $\downarrow$)	<58> t$_{HKHQ}$		7		ns
CLKOUT $\uparrow$ → $\overline{\text{HLDAK}}$ delay time	<59> t$_{DKHA}$			32	ns
$\overline{\text{HLDRQ}}$ high-level width	<60> t$_{WHQH}$		T+15		ns
$\overline{\text{HLDAK}}$ low-level width	<61> t$_{WHAL}$		T−15		ns
CLKOUT $\uparrow$ → bus float delay time	<62> t$_{DKF}$			32	ns
$\overline{\text{HLDAK}}$ $\uparrow$ → bus output delay time	<63> t$_{DHAC}$		−5		ns
$\overline{\text{HLDRQ}}$ $\downarrow$ → $\overline{\text{HLDAK}}$ $\downarrow$ delay time	<64> t$_{DHQHA1}$			(2n+7.5)T+40	ns
$\overline{\text{HLDRQ}}$ $\uparrow$ → $\overline{\text{HLDAK}}$ $\uparrow$ delay time	<65> t$_{DHQHA2}$		0.5T	1.5T+40	ns

★ (marker for the CLKOUT $\uparrow$ → bus float delay time row)

Remarks 1. T = t$_{CYK}$

2. n indicates the number of wait clocks inserted in a bus cycle. The sampling timing varies when programmable wait states are inserted.

(7) Bus hold timing (2/2)

Note UBEN (output), LBEN (output)

Remark The dotted line indicates a high-impedance state.
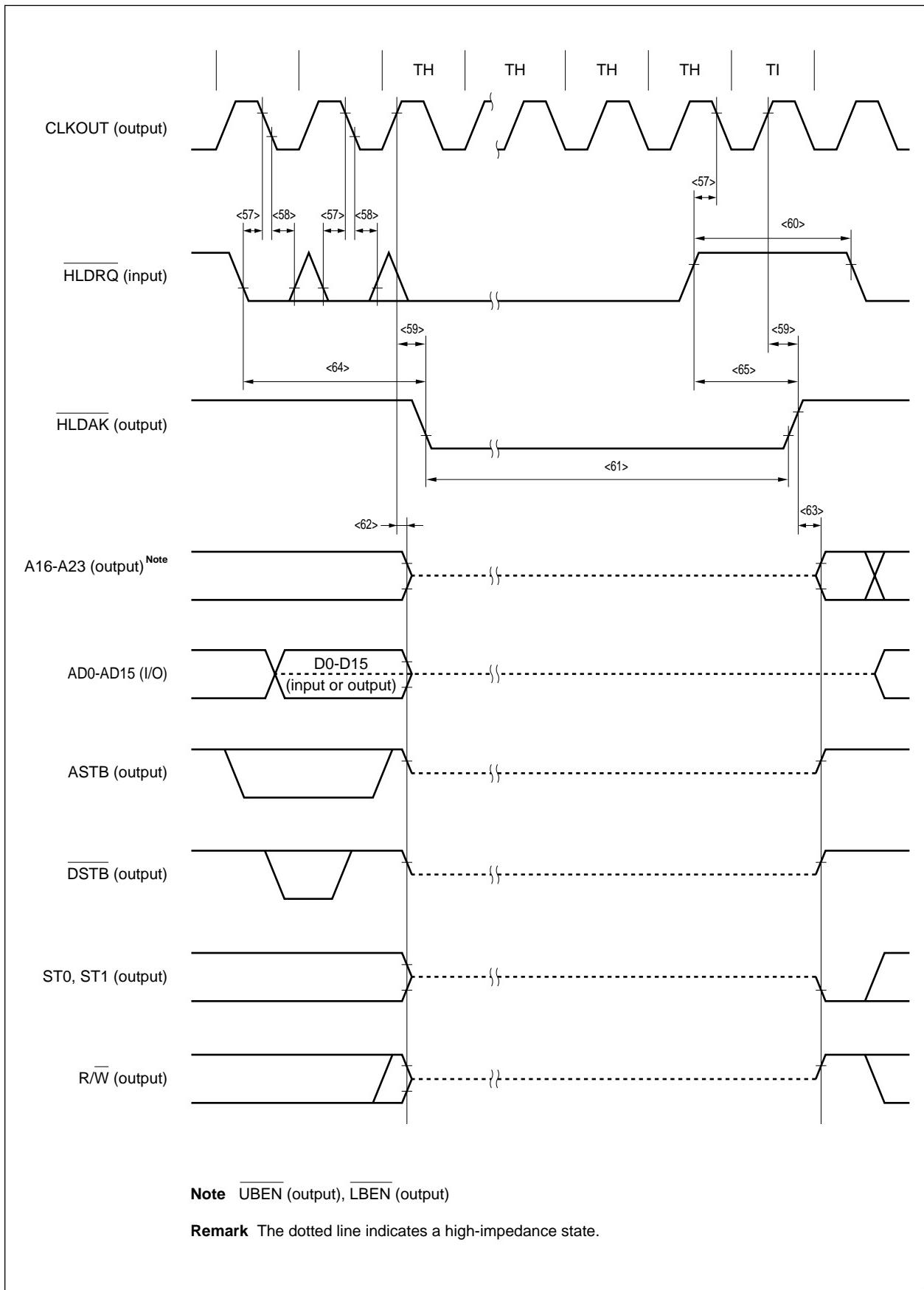
(8) Interrupt timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
NMI high-level width	<66>	t_{WNIH}		500		ns
NMI low-level width	<67>	t_{WNIL}		500		ns
INTPn high-level width	<68>	t_{WITH}	n=00, 01, 02, 03, 10, 11, 12, 13	3T+10		ns
INTPn low-level width	<69>	t_{WITL}	n=00, 01, 02, 03, 10, 11, 12, 13	3T+10		ns

Remark $T = t_{CYK}$
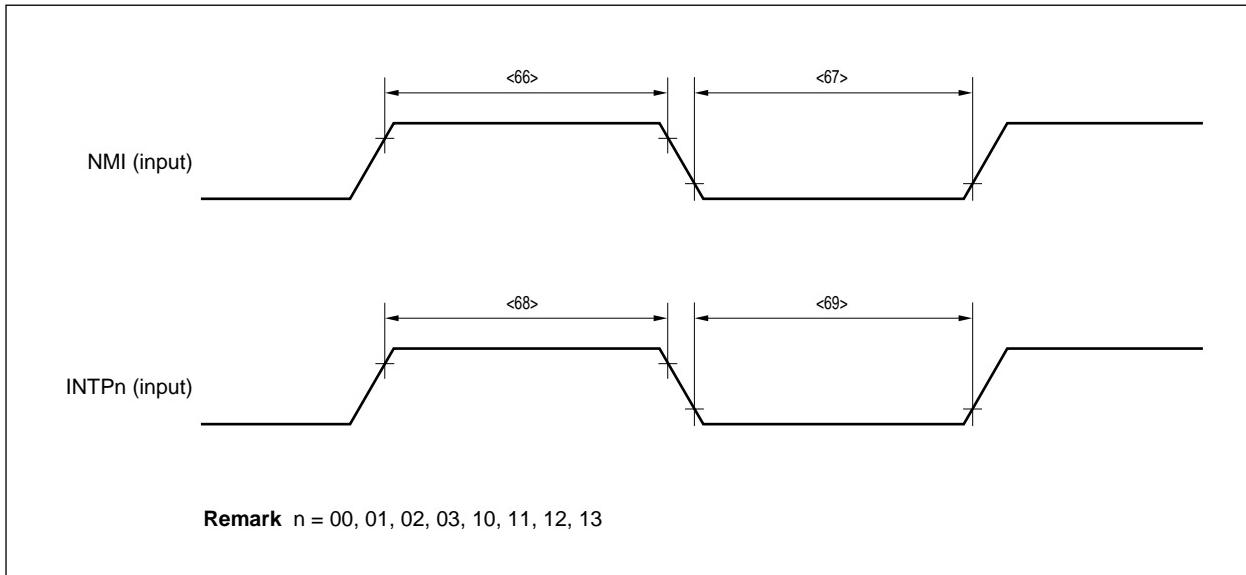
Remark n = 00, 01, 02, 03, 10, 11, 12, 13

(9) CSI timing

(a) Master mode

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{SCK}}$ cycle	<70>	t_{CYSK}	Output	330		ns
$\overline{\text{SCK}}$ high-level width	<71>	t_{WSKH}	Output	$0.5t_{\text{CYSK}}-40$		ns
$\overline{\text{SCK}}$ low-level width	<72>	t_{WSKL}	Output	$0.5t_{\text{CYSK}}-40$		ns
SI setup time (vs. $\overline{\text{SCK}}$ ↑)	<73>	t_{SSISK}		60		ns
SI hold time (vs. $\overline{\text{SCK}}$ ↑)	<74>	t_{HSKSI}		0		ns
SO output delay time (vs. $\overline{\text{SCK}}$ ↓)	<75>	t_{DSKSO}			40	ns
SO output hold time (vs. $\overline{\text{SCK}}$ ↑)	<76>	t_{HSKSO}		$0.5t_{\text{CYSK}}-15$		ns

(b) Slave mode

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{SCK}}$ cycle	<70>	t_{CYSK}	Input	330		ns
$\overline{\text{SCK}}$ high-level width	<71>	t_{WSKH}	Input	110		ns
$\overline{\text{SCK}}$ low-level width	<72>	t_{WSKL}	Input	110		ns
SI setup time (vs. $\overline{\text{SCK}}$ ↑)	<73>	t_{SSISK}		20		ns
SI hold time (vs. $\overline{\text{SCK}}$ ↑)	<74>	t_{HSKSI}		20		ns
SO output delay time (vs. $\overline{\text{SCK}}$ ↓)	<75>	t_{DSKSO}			60	ns
SO output hold time (vs. $\overline{\text{SCK}}$ ↑)	<76>	t_{HSKSO}		t_{WSKH}		ns

Remark The dotted line indicates a high-impedance state.
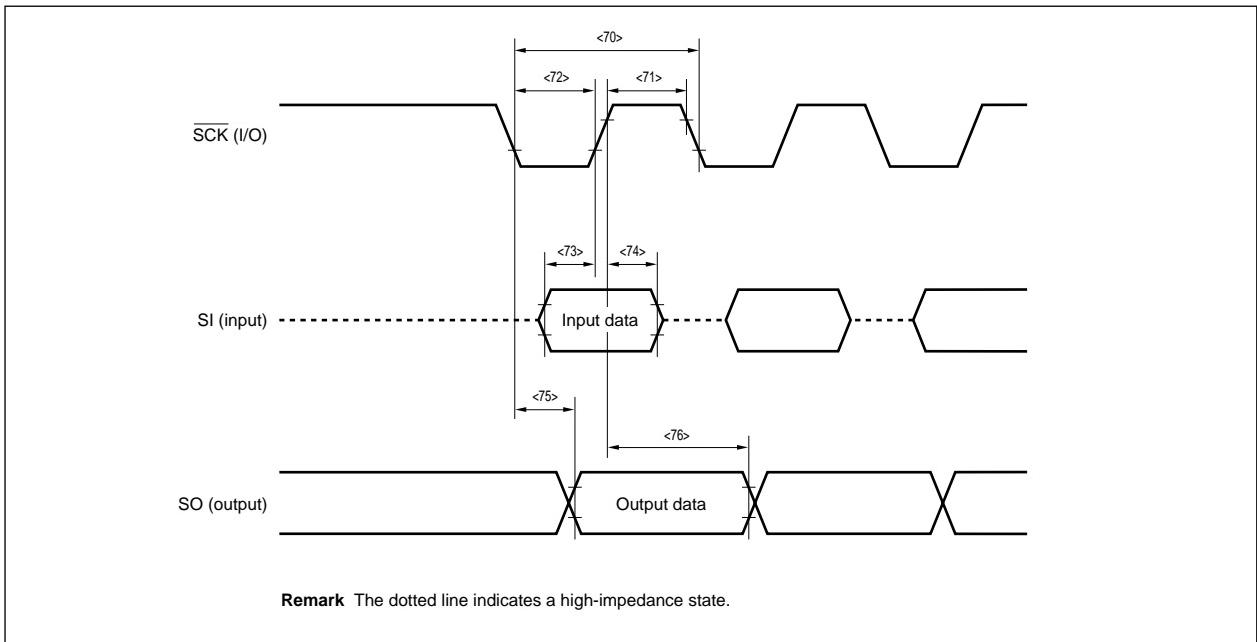
(10) RPU timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
TI1 high-level width	<77>	t_{WTIH}		3T+10		ns
TI1 low-level width	<78>	t_{WTIL}		3T+10		ns
TCLR1 high-level width	<79>	t_{WTCH}		3T+10		ns
TCLR1 low-level width	<80>	t_{WTCL}		3T+10		ns

Remark $T = t_{CYK}$
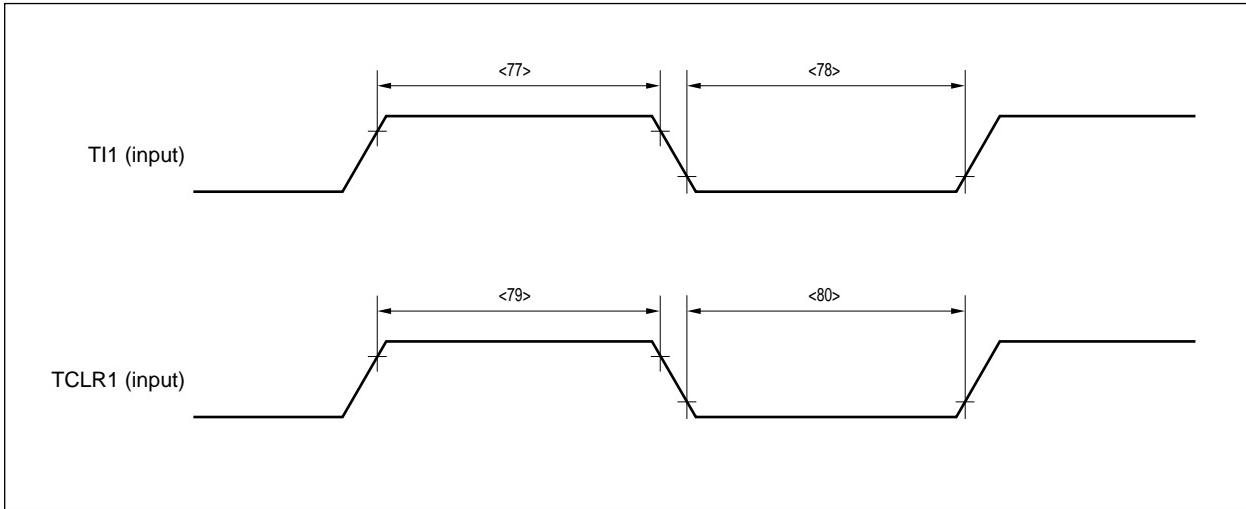
13. CHARACTERISTIC CURVE (reference)

I$_{OH}$ vs. (V$_{DD}$–V$_{OH}$)

(T$_A$ = 25 °C, V$_{DD}$ = 5.0 V, V$_{SS}$ = 0 V)

High-level output current I$_{OH}$ [mA]

Supply voltage – high-level output voltage V$_{DD}$–V$_{OH}$ [V]

I$_{OL}$ vs. V$_{OL}$

(T$_A$ = 25 °C, V$_{DD}$ = 5.0 V, V$_{SS}$ = 0 V)

Low-level output current I$_{OL}$ [mA]

Low-level output voltage V$_{OL}$ [V]
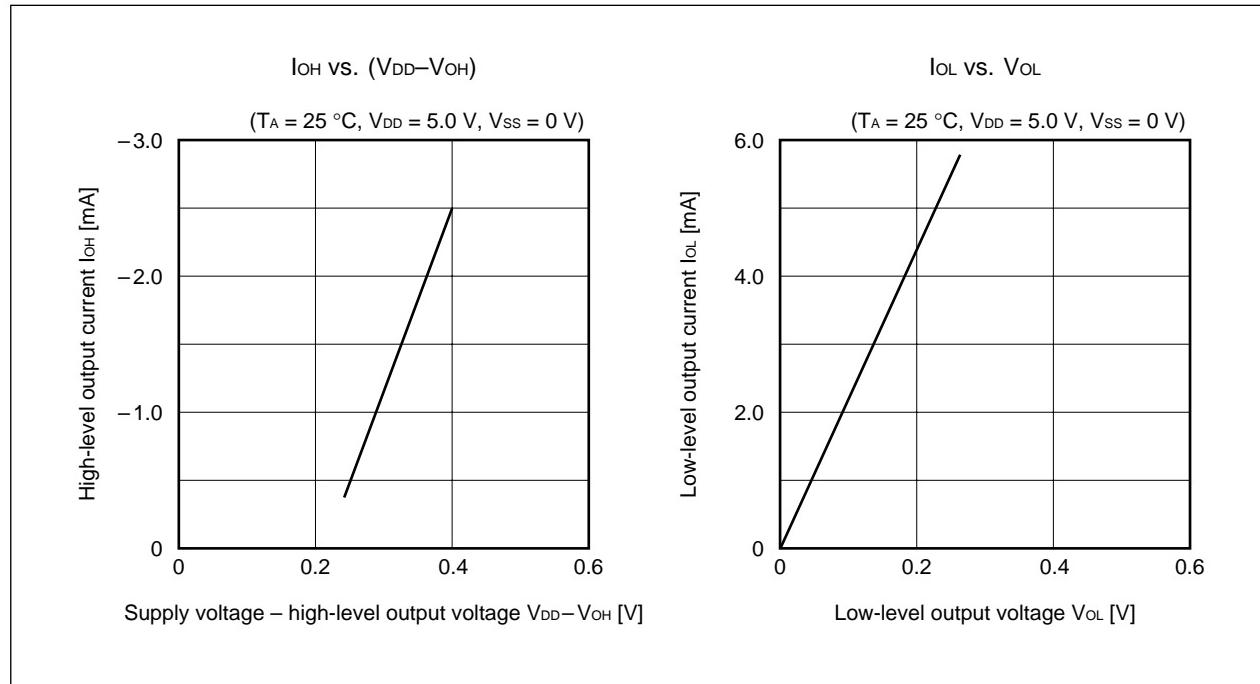
14. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (FINE PITCH) (□14)

detail of lead end
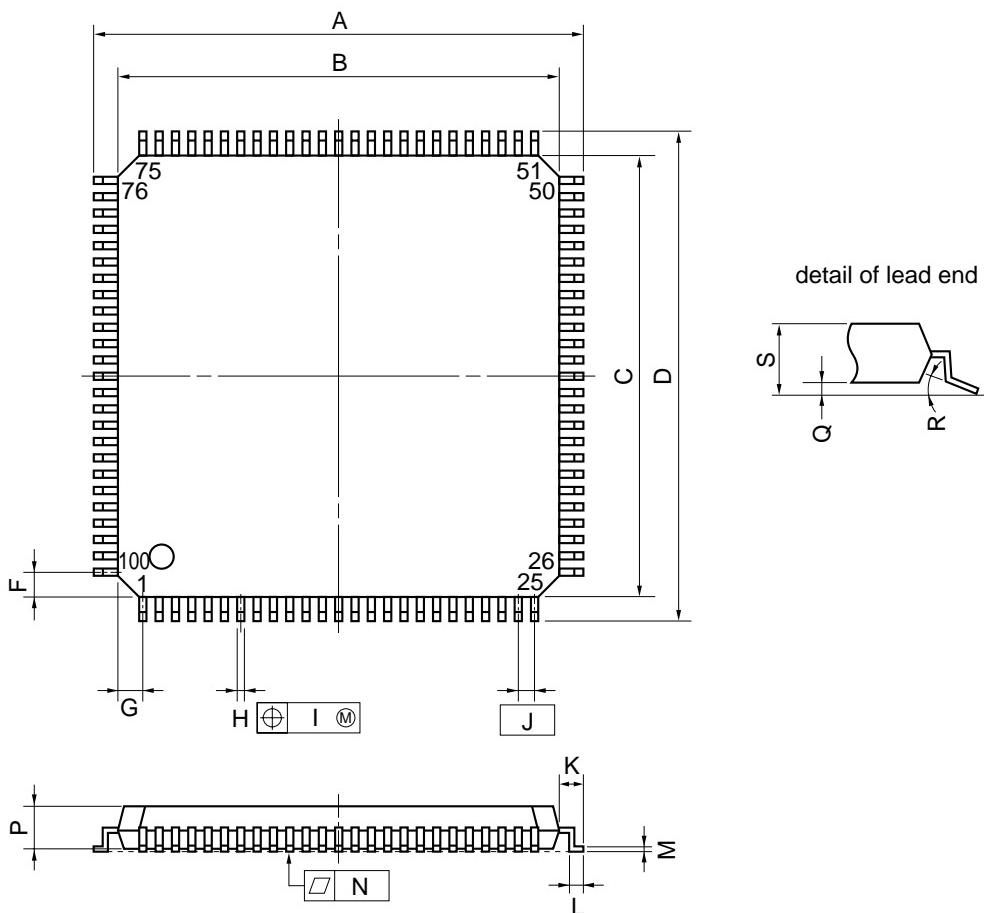
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of
its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.45	0.057
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-2

15. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.

For the details of the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and soldering conditions other than those recommended, consult NEC.

Table 15-1. Soldering Conditions of Surface Mount Type

μ**PD703000GC-xx-xxx-7EA :   100-pin plastic QFP (fine pitch) (14 $\times$ 14 mm)**
μ**PD703001GC-xx-7EA   :   100-pin plastic QFP (fine pitch) (14 $\times$ 14 mm)**

Soldering Method	Soldering Condition	Symbol of Recommended Condition
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max., Number of days: 7**Note** (after that, prebaking is necessary at 125°C for 10 hours) **<Precaution>** Products other than in heat-resistance trays (such as those packaged in a magazine, taping, or non-heat-resistance tray) cannot be baked while they are in their package.	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of times: 2 max., Number of days: 7**Note** (after that, prebaking is necessary at 125°C for 10 hours) **<Precaution>** Products other than in heat-resistance trays (such as those packaged in a magazine, taping, or non-heat-resistance tray) cannot be baked while they are in their package.	VP15-107-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	–

Note The number of days during which the product can be stored at 25°C, 65% RH max. after the dry pack has been opened.

Caution   Do not use two or more soldering methods in combination (except partial heating).

NOTES FOR CMOS DEVICES

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

• Device availability

• Ordering information

• Product release schedule

• Availability of related technical literature

• Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)

• Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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J96. 8

Related documents   : μPD70P3000 Data Sheet   U10988E

                                 V850 Family Instruction List   U10229E

                                 V851 Register List   U10662J (Japanese version)

Reference   : Considering Electric Characteristics - Microcomputers   IEI-601 (Japanese version)

The related documents referred to in this publication may include preliminary versions.

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