COMPUTE

the Club Of Microprocessor Programmers, Users, and Technical Experts

Georgia Marszalek, Editor • David Graves, Editor

Sponsored by National Semiconductor Corp., Santa Clara, Ca. 95051 **Vol. 2, No. 12, December, 1976**

muPro 8080 development system is now available!

Upon completion of an extensive evaluation by NATIONAL SEMICONDUCTOR CORPORATION of the currently available *design aids* for the 8080 microprocessor, muPro Inc. (manufacturer of the μPro-80) entered into a nationwide agreement with the NATIONAL SEMICONDUCTOR Sales Representatives.

The μPro-80 provides unique system development and test capabilities for the 8080A microprocessor chip.

A. Total system visibility and control made possible by the transparent Control Display Console. Requires no memory space, I/O device codes, interrupts, use of the stack, and imposes no software restrictions.

B. Real-time in-circuit emulation for user system clock periods from 350-600nS. with no wait states required.

C. Emulator can be used to simulate user's system PROM, RAM, or I/O.

D. The most comprehensive software support available. BSAL-80 provides the most efficient language for 8080 programming: high-level constructs, relocatability, assembly language code efficiency.

E. Supported by a wide range of peripherals and PROM Programmers.

The NATIONAL SEMICONDUCTOR Field Application Engineers (FAE) and System Specialists have completed training in the operation and application of the muPro products.

muPro Inc. began system deliveries in early August 1976.

Enclosed in this edition of *COMPUTE* are brief hardware and software descriptions together with a reader reply card. (See page 7 of this issue).

For further information, please contact your local NATIONAL SEMICONDUCTOR Sales Office or Sales Representative.

SC/MP Applications Handbook

A *SC/MP Microprocessor Applications Handbook* has just been published. It contains 155 pages of detailed system schematics, flowcharts, and program listings for a variety of SC/MP applications. Here is a partial list of the contents:

GENERAL CONCEPTS OF A/D AND D/A CONVERTERS
SINGLE-INPUT ANALOG-TO-DIGITAL CONVERTER SYSTEMS
ANALOG-TO-DIGITAL CONVERSION USING MULTIPLE CONVERTERS
ANALOG-TO-DIGITAL CONVERSION USING MULTIPLEXED UNITS
INTERFACING A KEYBOARD TO SC/MP
USING SC/MP AS A KEYBOARD SCANNER
USING SC/MP WITH A KEYBOARD (20 KEY) ENCODER
USING SC/MP WITH THE MM5740 (90 KEY) ENCODER
AN INTERRUPT DRIVEN KEYBOARD/DISPLAY SYSTEM
INTERFACING SC/MP WITH A BURROUGHS SELF-SCAN DISPLAY
MULTIPROCESSOR SYSTEMS
INTERFACING A SC/MP SYSTEM WITH A CASSETTE RECORDER
INTERFACING SC/MP WITH A SEIKO PRINTER

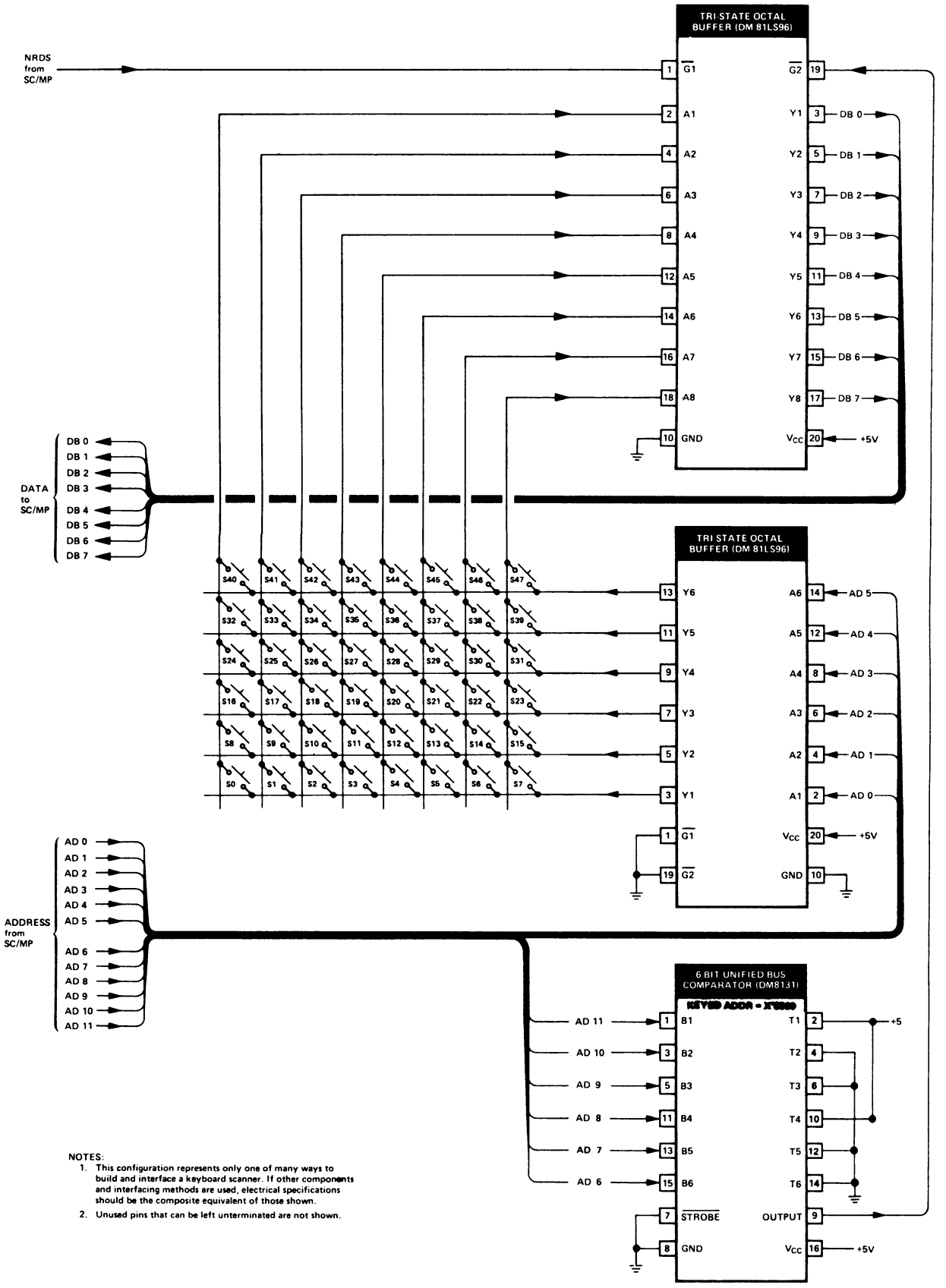
Numerous general interfacing examples are given in addition to the specific applications listed above. All applications are fully illustrated.

You are invited to order a free copy of the *SC/MP Microprocessor Applications Handbook.* All we ask is that you tell us what you are doing (or have done) with your SC/MP Kit or SC/MP Development System. Just complete the enclosed order form (look on insert page B). and mail it to:

SC/MP Applications Handbook
Marketing Services
National Semiconductor Corp., MS 520
2900 Semiconductor Drive
Santa Clara, CA 95051

Interfacing a keyboard to SC/MP!

Figure 1. Using SC/MP as a Keyboard Scanner



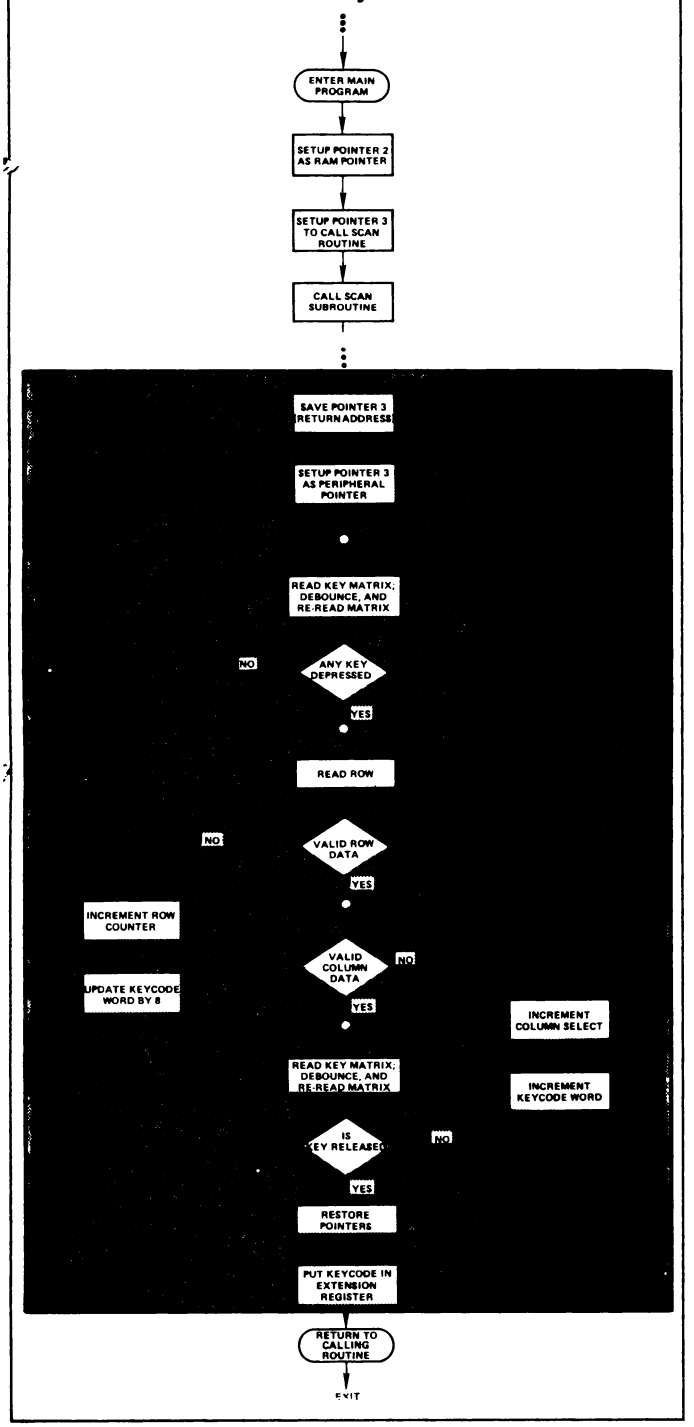
NOTES:

1. This configuration represents only one of many ways to build and interface a keyboard scanner. If other components and interfacing methods are used, electrical specifications should be the composite equivalent of those shown.
2. Unused pins that can be left unterminated are not shown.

SC/MP applications that require a keyboard interface usually use one of two methods to generate keycodes. In one method, SC/MP is used as a keyboard scanner, whereas in the other method, SC/MP is interfaced with a keyboard encoder. For either type of interface, programs can be developed for continuous keyboard scan or for using the keyboard as an interrupt device.

When SC/MP is interfaced with an appropriate keyboard and is supported with the proper software, any application that can be controlled by alphanumeric inputs is feasible—lawn-sprinkler control, home and business lighting, vending machines, combination locks, kitchen appliances, games, and so on. Some basic principles of keyboard interfacing are shown in the following illustrations and are described in the supporting text.

Figure 2. Flowchart for SC/MP Interfaced with a 6 x 8 Keyboard Matrix



General Description

The keyboard matrix shown in figure 1 consists of six rows with eight keys in each row. Functional relationships between the keyboard and SC/MP can be summarized as follows. The entire key matrix is scanned by testing input data to the microprocessor for a value other than zero; this condition occurs if any key is depressed. After key detect, a software debounce is performed. Then, the program determines the row and the column corresponding to the key, computes the correct binary code, tests for key release, puts the keycode in the SC/MP Extension Register, and returns to the calling program.

System Operation

A fixed address (X'0900) is assigned to the "keyboard peripheral" and when a load (LD) instruction is executed, the TRI-STATE buffers are simultaneously activated. Thus, if any key (S0 through S47) is pressed, one of the bits (DB0 through DB7) on the data bus appears as a logic '1'.

The program "LOOP" checks for the "nonzero" condition and provides a debounce time of 5 milliseconds. After debounce, the value of the key is determined by updating a counter in RAM. The counter is incremented by "8" for each row scanned and by "1" for each column scanned. For example, assume that S9 (row 2/column 2 of figure 1) is pressed. The first row is scanned by the software, and finding no key pressed, the row counter (row select) is incremented by 8 and the second row is scanned. In this row, one of the bits in the data word is a logic '1'; accordingly, the column counter is now incremented by 1 and comparisons are made to determine which switch is pressed—for this example, it is the second switch (S9) in the column. It can readily be seen that a different binary code (keycode) is produced for each switch in the matrix. The keycode is saved in temporary memory, and the keyboard is tested for key release by executing a Load Instruction to the keyboard. This activates all the buffers, and, upon key release, the keycode is transferred from temporary memory to the Extension Register. The designated pointer then is exchanged with the Program Counter to return to the calling program.

Software Considerations

The flowchart in figure 2 and the program listing in figure 3 show how SC/MP can be utilized by software to perform a keyboard scanning function.

Figure 3. Program Listing for SC/MP Interfaced with a 6 x 8 Keyboard Matrix

```
1                       TITLE SCANNR,'SC/MP'
2
3                       ;SC/MP ACTS AS A KEYBOARD SCANNER.
4                       ;THE KEYBOARD IS A 6 BY 8 MATRIX
5
6
7
8
9
10                      ;TYPICAL MAIN PROGRAM
11
12
13                      ;THIS SECTION OF CODE SETS UP THE RAM POINTER
14                      ;AND THE POINTER FOR THE SCAN ROUTINE
15
16
17
18 0000  C400                   LDI     L(RAM)
```

Figure 3 (Continued)

```
19 0002 32          XPAL  2
20 0003 C403        LDI   H(RAM)
21 0005 36          XPAH  2
22 0006 C40F        LDI   L(SCAN)-1
23 0008 33          XPAL  3
24 0009 C400        LDI   H(SCAN)
25 000B 37          XPAH  3
26 000C 3F          XPPC  3          ;CALL SCAN ROUTINE
27 000D 40    START: LDE             ;PUT CODE
                                     INTO ACCUM
28 000E CA00        ST    SAVE(2)    ;SAVE CODE IN RAM
29
30
31
32                  ;USERS PROGRAM WOULD BEGIN HERE AND OPERATES
33                  ;ON THE KEY CODE STORED IN LOCATION 'SAVE'
34
35
36
37
38
39
40
41                  ;THE SCAN ROUTINE FORMS THE CORRECT CODE IN
42                  ;LOCATION 'SWITCH' AFTER CHECKING FOR KEY
43                  ;RELEASE CONTROL IS RETURNED TO THE CALLING
44                  ;PROGRAM WITH THE KEYCODE IN THE E REGISTER
45
46
47
48 0010 33     SCAN: XPAL  3
49 0011 CA01        ST    TEMPL(2)   ;SAVE PTR 3 LO
50 0013 37          XPAH  3
51 0014 CA02        ST    TEMPH(2)   ;SAVE PTR 3 HI
52 0016 C400        LDI   L(PERIPH)
53 0018 33          XPAL  3
54 0019 C409        LDI   H(PERIPH)
55 001B 37          XPAH  3          ;SET UP PERIPHERAL
56                                   ;POINTER
57 001C 02    OVER: CCL
58 001D C400        LDI   0
59 001F CA03        ST    SWITCH(2)  ;CLR SWITCH WORD
60
61
62
63                  ;THE ACTUAL SCANNING OF THE KEYBOARD
64                  ;FORMING THE KEYCODE AND TESTING FOR
65                  ;KEY RELEASE BEGINS WITH THE LABEL 'LOOP'
66                  ;AND ENDS WITH THE INSTRUCTION "JNZ RELEAS"
67
68
69 0021 C33F LOOP:  LD    ALLKYS(3)
70 0023 01          XAE              ;SAVE CODE
71 0024 8F05        DLY   5          ;DEBOUNCE 5 MS
72 0026 C33F        LD    ALLKYS(3)
73 0028 50          ANE              ;COMPARE NEW
                                     WITH OLD
74 0029 98F6        JZ    LOOP       ;IF = 0, INVALID KEY
75 002B C420        LDI   X'20
76 002D 01    LOOP1: XAE             ;ROW DRIVER TO
                                     E REG
77 002E C380        LD    -128(3)    ;READ ROW
                                     INTO ACCUM
78 0030 9C0C        JNZ   SHIFT      ;IF NOT 0, VALID KEY
79 0032 C203        LD    SWITCH(2)
80 0034 F408        ADI   8          ;INCR SWITCH BY 8
81 0036 CA03        ST    SWITCH(2)
82 0038 01          XAE              ;ROW DRIVER
                                     INTO ACCUM
83 0039 1C          SR
84 003A 98E0        JZ    OVER       ;NO KEY FOUND
85 003C 90EF        JMP   LOOP1
86 003E 1C    SHIFT: SR
87 003F 9806        JZ    RELEAS     ;IF = 0, KEY DECODED
88 0041 01          XAE              ;SAVE CODE IN E REG
89 0042 AA03        ILD   SWITCH(2)  ;INCR SWITCH VALUE
90 0044 01          XAE              ;RECALL FOR
                                     NEXT SHFT
91 0045 90F7        JMP   SHIFT
92 0047 C33F RELEAS: LD   ALLKYS(3)  ;READ KEY MATRIX
93 0049 01          XAE              ;SAVE CODE
94 004A 8F05        DLY   5          ;DEBOUNCE 5 MS
95 004C C33F        LD    ALLKYS(3)
96 004E 50          ANE              ;COMPARE NEW
                                     WITH OLD
97 004F 9CF6        JNZ   RELEAS     ;IF 0, KEY RELEASED
98 0051 C201        LD    TEMPL(2)
99 0053 33          XPAL  3
100 0054 C202       LD    TEMPH(2)
101 0056 37         XPAH  3          ;RESTORE PTR 3
102 0057 C203       LD    SWITCH(2)  ;GET KEYCODE
103 0059 01         XAE              ;SAVE CODE IN E REG
104 005A 3F         XPPC  3          ;RETURN TO CALLING
                                     ;PROGRAM
105
106 005B 90B3       JMP   SCAN
107
108
109
110
111                 ;DATA AREA
112
113
114       0300 RAM = X '0300
115
116       0000 SAVE = 0
117
118       0001 TEMPL = 1
119
120       0002 TEMPH = 2
121
122       0003 SWITCH = 3
123
124       0004 KEYMD = 4
125
126       003F ALLKYS = X '3F
127
128       0900 PERIPH = X '0900
129
130
131       0000 END
```

```
ALLKYS  003F    KEYMD   0004*   LOOP    0021
LOOP1   002D    OVER    001C    PERIPH  0900
RAM     0300    RELEAS  0047    SAVE    0000
SCAN    0010    SHIFT   003E    START   000D*
SWITCH  0003    TEMPH   0002    TEMPL   0001
```

```
NO ERROR LINES
SOURCE CHECKSUM=557B

***DISC SECTORS USED***

FIRST INPUT SECTOR HEX—0292
FINAL INPUT SECTOR HEX—0296
```

Programming Tidbit:

If you are using Genldr and don't like where the Absolute Loader (ABSPT or ABSCR) loads it—you can use Genldr to relocate itself. Load Genldr and then specify where you would like to start with the OTS command and reload it at its new location.

If you want to save a copy of the relocated Genldr and have an IMP-16 you can then use RAMDUMP (SL0012) to make a new paper tape of the loader. When doing this remember the Genldr program for IMP-16 uses base page locations 0010 through 0016. Don't forget to dump these along with the top sector portion of the program.

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User Library Order Form

PROGRAM NUMBER		PROGRAM NAME	LISTING QUANTITY N/C	SOURCE PAPER TAPES QUANTITY $5.00 EACH
SL0001A	IMP	BINBCD		N/A
SL0002A	IMP	BCD		N/A
SL003A	IMP	MD		N/A
SL0004A	IMP	PTBIN		N/A
SL0005A	IMP	BINASC		N/A
SL0006A	IMP	BINGRAY		N/A
SL0007B	IMP	BCDBIN		N/A
SL0008A	IMP	PNMULT		N/A
SL0009A	IMP	IMP-8 MATH		N/A
SL0010A	IMP	MEMORY DUMP		
SL0011A	IMP	GALPAT		
SL0012B	IMP	RAMDUMP		
SL0013A	IMP	TAPE TITLER		
SL0014A	IMP	GRAY CODE		
SL0015A	PACE	PACRAM		
SL0016A	IMP	PRTPLT		
SL0017A	IMP	TSTPLT		
SL0018A	PACE	CALCULATOR		
SL0019A	IMP	MESGH		
SL0020A	IMP	CHARST		
SL0021A	IMP	CONTAP		
SL0022A	PACE	NUMPRG		
SL0023A	IMP	DISC RLM-PROMSFT-B		N/A
SL0024A	IMP	DISC RLM-PROMSFT-C		N/A
SL0025A	PACE	PALM		
SL0026A	PACE IMP	TABTAP		
SL0027A	SC/MP	SC/MP MATH PACKAGE		
SL0028A	IMP	SQRT		
SL0029A	PACE	BINBCD		
SL0030A	IMP-16	TITLER		
SL0031A	IMP-16	DORG		
SL0032A	PACE	DIVIDE		
SL0033A	PACE	DELSEM		
SL0034A	NOVA	X-ASSEM		N/A
SL0035A	PACE	PRNTLM		

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Please make sure the programs you select are for the microprocessor you have.

National Semiconductor

Preliminary Data
MAY 1977

ISP-8A/650 N-Channel 128-by-8 Bit RAM Input/Output (RAM I/O)

General Description

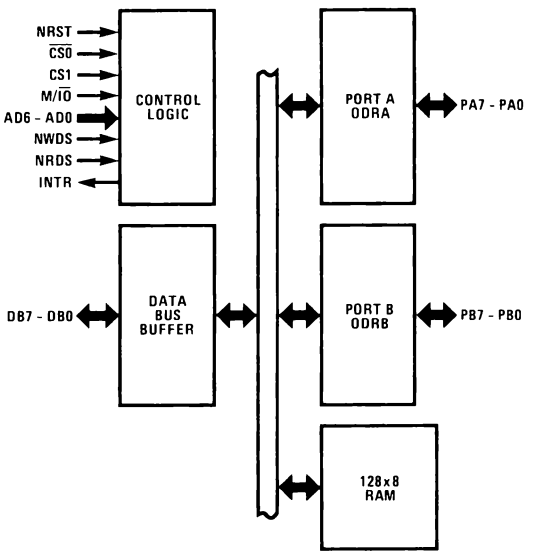
The RAM Input/Output Chip is an LSI device which provides random access memory and peripheral interfacing for microcomputer systems. The RAM portion contains 1024 bits of static RAM organized as 128x8. The I/O portion consists of two peripheral ports of eight bits each. Each of the I/O pins in the two ports may be defined as an input or an output to provide maximum flexibility. Each port may be read from or written to in a parallel (8-bit byte) mode. To improve efficiency and simplify programming in control-based applications, a single bit of I/O in either port may be set, cleared or read with a single microprocessor instruction. In addition to basic I/O, one of the ports, port A, may be programmed to operate in several types of strobed mode with handshake. Strobed mode together with optional interrupt operation permit both high speed parallel data transfers and interface to a wide variety of peripherals with no external logic.

The RAM I/O is an n-channel silicon gate device packaged in a 40-pin dual-in-line package. It operates with a single 5-volt power supply and is fully TTL compatible.

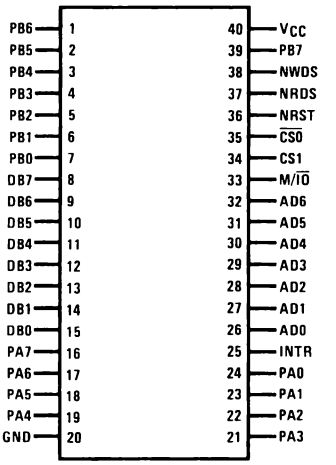
Features

- 128x8 RAM
- Single +5-volt power supply
- Low power dissipation
- Fully static operation
- Completely TTL compatible
- Two 8-bit programmable I/O ports
- I/O ports are TRI-STATE®
- Handshake controls for strobed mode of operation
- Single bit I/O operations with single instruction
- Reduces system package count
- Direct interface with SC/MP-II
- Independent operation of RAM and I/O

Basic Block Diagram



Pin Configuration



Pin Names

DB7 - DB0	DATA BUS
AD6 - AD0	ADDRESS INPUT
NRST	RESET INPUT
M/IO	MEMORY/IO SELECT
CS0, CS1	CHIP SELECTS
NWDS	WRITE STROBE
NRDS	READ STROBE
PA7 - PA0	PORT A
PB7 - PB0	PORT B
INTR	INTERRUPT REQUEST
VCC	+5 VOLTS
GND	0 VOLTS

DA-B20M57/Printed in U.S.A.

ISP-8A/650 N-Channel 128-by-8 Bit RAM Input/Output (RAM I/O)

Absolute Maximum Ratings*

Voltage at Any Pin	−0.5 V to +7.0 V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5 V ± 5% unless otherwise specified.)

Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage		2.0		V_{CC}+0.5	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.8	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −100 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 2.0 mA			0.4	V
I_{LI}	Input Load Current	V_{IN} = 0 V to 5.25 V			±10	μA
I_{LO}	Output Leakage Current	High Impedance State			±10	μA
I_{CCI}	Power Supply Current	All Outputs Open, T_A = 25°C		50		mA

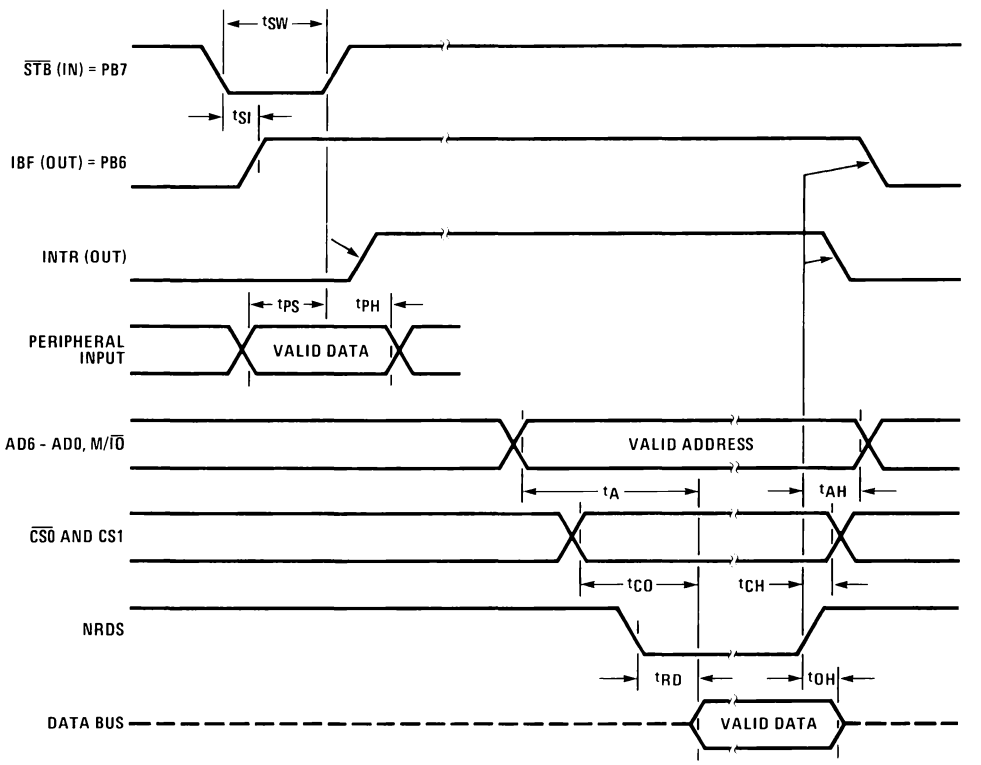
AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5 V ± 5% unless otherwise specified — see Note 1.)

Parameter		Conditions	Min	Typ	Max	Units
READ CYCLE						
t_{SW}	$\overline{STB}$ Pulse Width			300		ns
t_{SI}	$\overline{STB}$ ↓ to IBF ↑ Delay			200		ns
t_{PS}	Peripheral Setup			150		ns
t_{PH}	Peripheral Hold			50		ns
t_{AH}	Address Hold		50			ns
t_{CH}	CS Hold		50			ns
t_{RD}	NRDS ↓ to Data Valid				300	ns
t_A	Access			500	700	ns
t_{CO}	Chip Select to Output			500	700	ns
t_{OH}	Data Valid After NRDS ↑		0			ns
	Output Load Capacitance				75	pF

Note 1: All times measured from a valid logic "0" level = 0.8 V or a valid logic "1" level = 2.0 V.

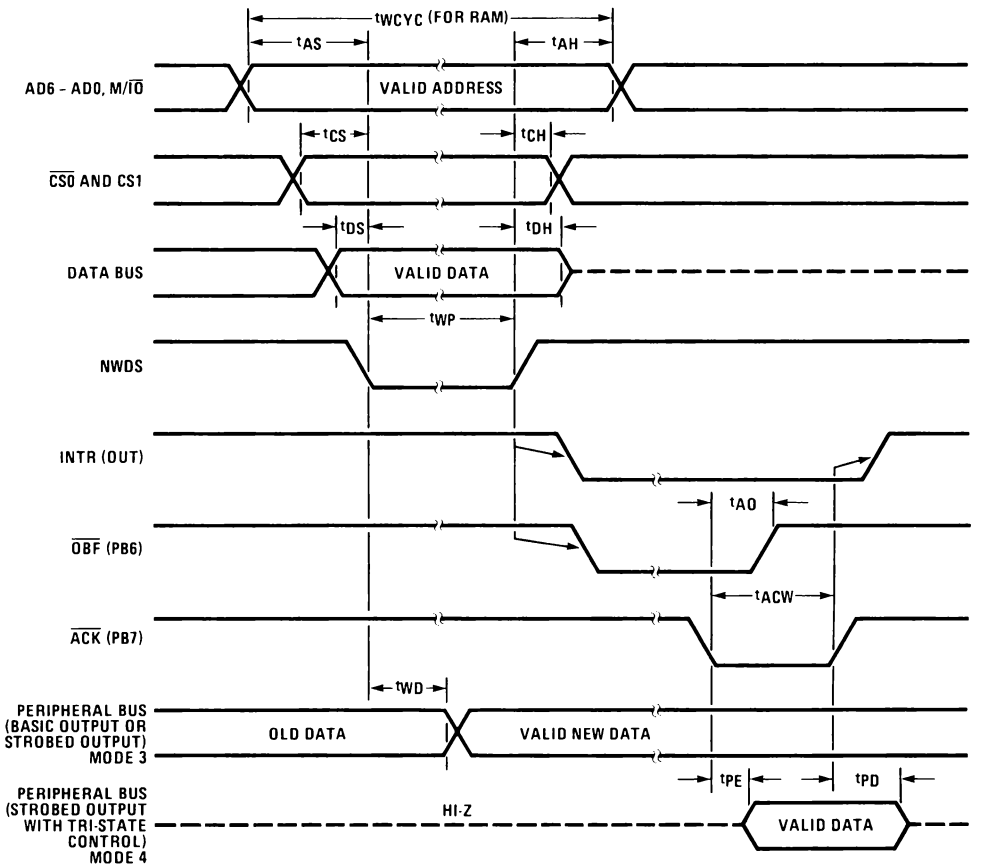
Read Cycle



AC Electrical Characteristics (cont'd.)

Parameter		Conditions	Min	Typ	Max	Units
WRITE CYCLE						
t_{WC}	Write Cycle (for RAM)			750		ns
t_{AS}	Address Setup		300			ns
t_{AH}	Address Hold		50			ns
t_{CS}	CS Setup		300			ns
t_{CH}	CS Hold		50			ns
t_{DS}	Data Setup		50			ns
t_{DH}	Data Hold		50			ns
t_{WP}	NWDS Pulse Width		300			ns
t_{AO}	$\overline{ACK}$ ↓ to $\overline{OBF}$ ↑			200		ns
t_{ACW}	$\overline{ACK}$ Pulse Width			300		ns
t_{WD}	Port Data Valid After NWDS ↓			250		ns
t_{PE}	$\overline{ACK}$ ↓ to Valid Output (TRI-STATE Mode)			250		ns
t_{PD}	$\overline{ACK}$ ↑ to Hi-Z (TRI-STATE Mode)			300		ns
Output Load Capacitance					75	pF

Write Cycle



Basic Functional Description

The RAM I/O performs two separate but important functions in microcomputer systems. The first is data storage provided by the 128x8 RAM. The second function is peripheral interfacing provided by the two 8-bit I/O ports. The ability to program the configuration and operating modes of the I/O ports allows interfacing a microcomputer to a wide variety of peripherals with minimum external logic. Major functional blocks of the chip are shown in figure 1; an operational summary of the chip is provided in figure 2. A description of the chip pinouts and a summary of the internal chip registers is given below.

(DB7 - DB0) Data Bus Buffers

The data bus buffer is a TRI-STATE, bidirectional, 8-bit buffer that is used to interface the RAM I/O to a microcomputer data bus. Data, control, and status information is transmitted to and received from the RAM I/O via the data bus buffers. Execution of a STORE instruction by the microprocessor may be used to transmit data and control information from the CPU to the RAM I/O. Execution of a LOAD instruction may be used to transmit data and status information from the RAM I/O to the CPU.

($\overline{CS0}$ and CS1) Chip Select Inputs

The combination of a low on $\overline{CS0}$ and a high on CS1 input pins enables communication between the RAM I/O and the microprocessor.

(M/$\overline{IO}$) Memory $\overline{I/O}$ Select

The state of the M/$\overline{IO}$ input pin determines whether communication between the CPU and RAM I/O chip will involve the RAM portion of the RAM I/O or the I/O portion. A high on M/$\overline{IO}$ selects the RAM while a low selects the I/O.

(NRDS) Read Strobe

NRDS is an active-low read strobe. A low on this pin enables data or status information to be read from the RAM I/O.

(NWDS) Write Strobe

NWDS is an active-low write strobe. A low on this pin enables data or control information to be written into the RAM I/O.

(AD6 - AD0) Address Inputs

The address input bus determines where in the RAM I/O communication will take place. When the RAM is selected, the address bus determines which of the 128 bytes of RAM will be read from or written into. When I/O is selected, the address determines which I/O or control register will be enabled for communication with the CPU. These pins are normally connected to the seven low address lines of the microprocessor.

RAM

The RAM contained on the RAM I/O chip consists of 1024 bits organized as 128 eight-bit bytes. Since the RAM is fully static, no refresh or clocks are required. Data out of the RAM is of the same polarity as data in, and readout is nondestructive. The RAM is a standard six-transistor cell similar in design to the 2102A static RAM.

(MDR) Mode Definition Register

The Mode Definition Register is an internal control register that determines the operating mode of port A. This register is *write only.* If a read operation is performed with the address set to that of the MDR, the data bus will remain in the high impedance state.

(PA7 - PA0, PB7 - PB0) Peripheral Ports A and B

The RAM I/O contains two eight bit I/O ports: port A and port B. Each port consists of an eight-bit output data latch with buffer and an eight-bit input data latch. Full flexibility is provided with the ability to define any bit of the two ports either as an input or as an output. Bit set, clear and read of all I/O pins are also provided. Moreover, port A may be operated in strobed input or strobed output modes.

Output Definition Registers — ODRA and ODRB

Associated with each port is an output definition register (ODR). Each ODR is an eight-bit latch that defines which of the I/O pins in the respective port are to be used as outputs. ODRA controls the direction of port A and ODRB controls the direction of port B. Both ODRs are *write only* registers. If a read operation is performed with the address set to that of an ODR, the data bus will remain in the high impedance state.

(INTR) Interrupt Request

The interrupt request (INTR) output is an active high signal used to interrupt the microprocessor when a strobed mode data transaction has occured. This signal is active only when port A is in the strobed mode. INTR will be set to a low when a master reset is applied (NRST set low).

(NRST) Master Reset

NRST is the master reset input for the RAM I/O chip. A low on this pin clears all registers in the I/O portion of the chip (MDR, ODRA, ODRB, and the port output data latches) and places the data bus in the high impedance state independent of any other control strobes. After a master reset, the I/O ports will both be in the basic I/O mode and configured as inputs. The master reset does not change any data previously stored in the RAM and does not allow data to be written into or read from the RAM while NRST is low.

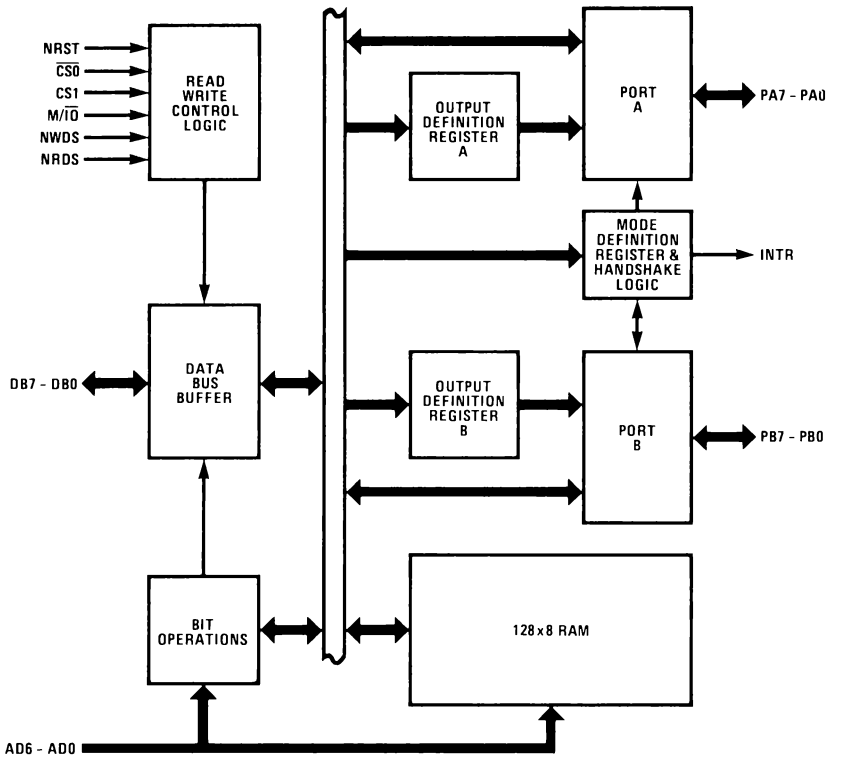


Figure 1. Block Diagram

Operation	NRST	NRDS	NWDS	$\overline{CS0}$	CS1	M/$\overline{IO}$	A6	A5	A4	A3	A2	A1	A0
RAM OPERATIONS													
Data Bus → RAM	1	1	0	0	1	1	X	X	X	X	X	X	X
RAM → Data Bus	1	0	1	0	1	1	X	X	X	X	X	X	X
BIT OPERATIONS													
Set Bit Port A	1	1	0	0	1	0	0	0	1	0	B2	B1	B0
Clear Bit Port A	1	1	0	0	1	0	0	0	0	0	B2	B1	B0
Read Bit Port A	1	0	1	0	1	0	0	0	X	0	B2	B1	B0
Set Bit Port B	1	1	0	0	1	0	0	0	1	1	B2	B1	B0
Clear Bit Port B	1	1	0	0	1	0	0	0	0	1	B2	B1	B0
Read Bit Port B	1	0	1	0	1	0	0	0	X	1	B2	B1	B0
PORT OPERATIONS													
Port A → Data Bus	1	0	1	0	1	0	0	1	0	0	0	0	0
Data Bus → Port A	1	1	0	0	1	0	0	1	0	0	0	0	0
Port B → Data Bus	1	0	1	0	1	0	0	1	0	0	0	0	1
Data Bus → Port B	1	1	0	0	1	0	0	1	0	0	0	0	1
CONTROL OPERATIONS													
Data Bus → Output Definition A	1	1	0	0	1	0	0	1	0	0	0	1	0
Data Bus → Output Definition B	1	1	0	0	1	0	0	1	0	0	0	1	1
Data Bus → Mode Definition Register	1	1	0	0	1	0	0	1	0	0	1	0	0
DISABLE FUNCTION													
Master Reset	0	X	X	X	X	X	X	X	X	X	X	X	X
Data Bus → Hi-Z	1	1	1	0	1	X	X	X	X	X	X	X	X
Data Bus → Hi-Z	1	X	X	1	X	X	X	X	X	X	X	X	X
Data Bus → Hi-Z	1	X	X	X	0	X	X	X	X	X	X	X	X

Figure 2. Basic Operation

Detailed Operation

RAM

The internal organization of the RAM and a typical RAM memory cell are shown in figure 3; the 1024-bit memory is structured in a 32-column by 32-row matrix. The proper row is selected by the five higher-order address (AD6 - AD2) inputs; the 8-bit byte in this row is selected by eight 1-of-4 column decoders controlled by the two lower-order address (AD1 - AD0) inputs. A timing diagram of RAM read/write operations is shown in figure 4. While RAM cannot be read from or written into during a master reset (NRST), the reset signal does not affect the data in RAM.

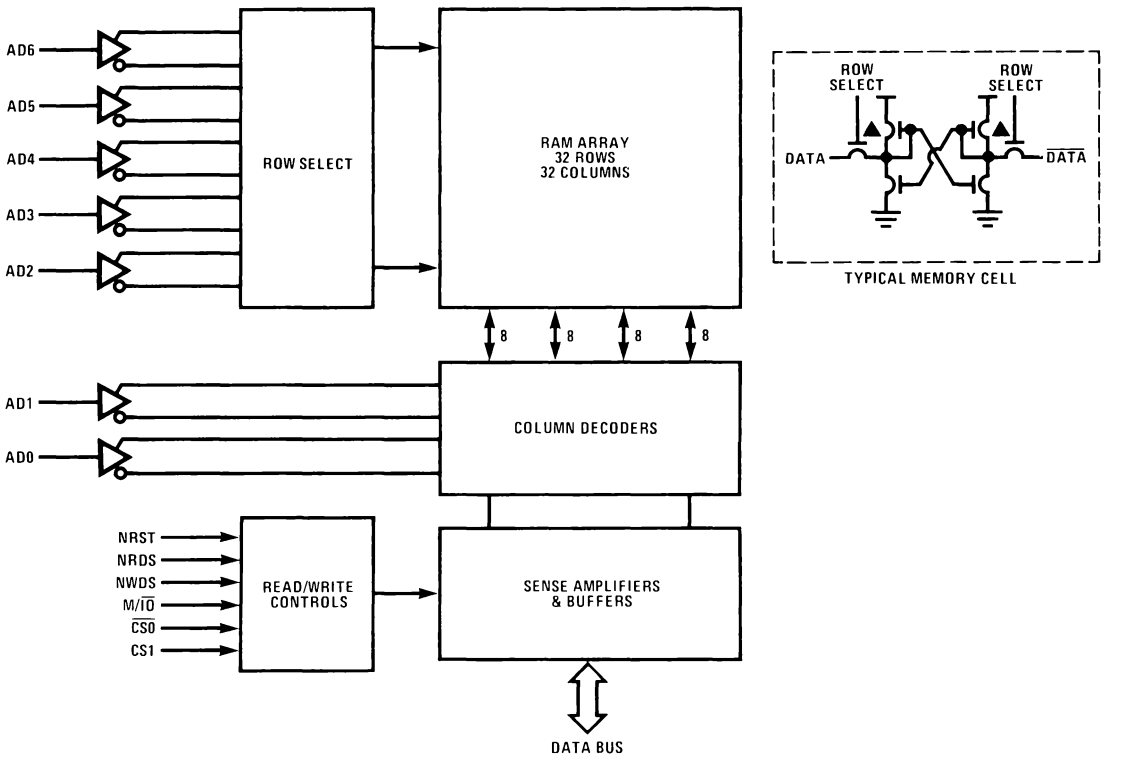


Figure 3. RAM Organization

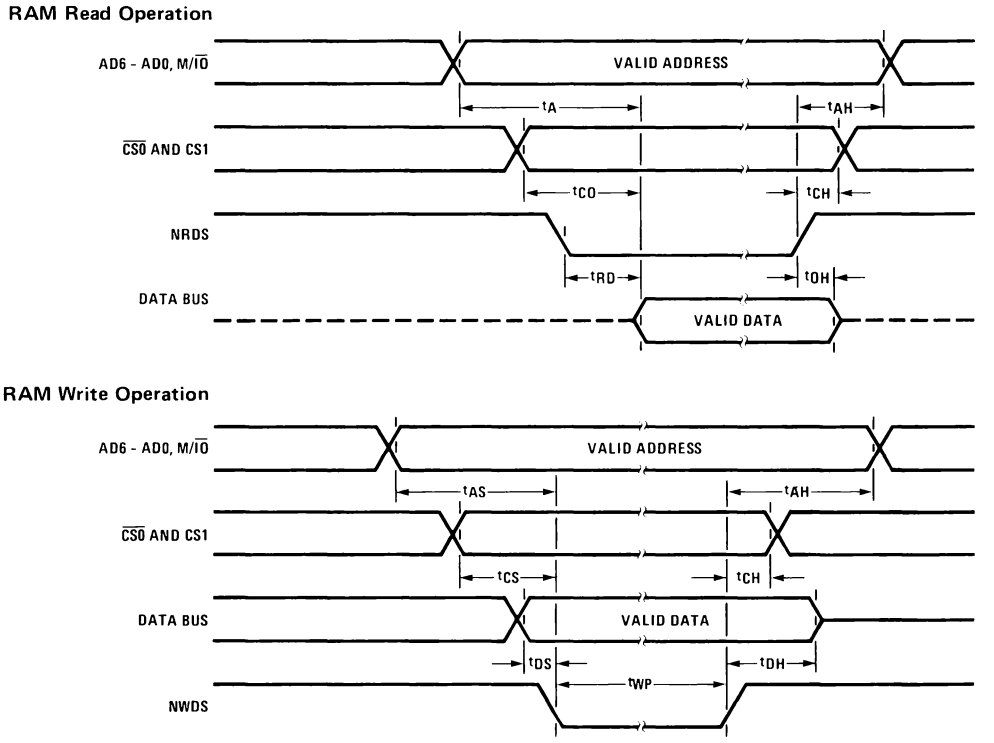


Figure 4. RAM Read/Write Timing

Mode Definition Register

The mode definition register defines the operating mode for port A. Port B is always in the basic I/O mode. There are four operating modes for port A:

Mode 1 – basic I/O

Mode2 – strobed input

Mode 3 – strobed output

Mode 4 – strobed output with TRI-STATE control

In mode 1, basic I/O, there is no handshaking and data is simply written to or read from the specified port. Port B is always in this mode. When NRST goes low, both port A and port B are set to the basic I/O mode with all bits set to input. Mode 2, strobed input, provides a means for transferring data from the peripheral into port A in response to handshake or strobe signals. Mode 3, strobed output, provides a means for transferring data from port A to the peripheral in response to strobes or handshake signals. Mode 4, strobed output with TRI-STATE control is similar to mode 3 except that port A is in the high impedance state until the handshake signal goes active. Figure 5 summarizes what data should be written into the MDR to place port A in the desired mode. When port A is operated in any one of the three strobed modes, two pins of port B are used for handshake control functions; accordingly, only six of the eight port B pins are available for data input/output bits.

Output Definition Registers

Although addressed separately from the ports, the output definition registers are an integral part of the I/O ports as shown in figure 6. This figure shows the input data latch and output data latch/buffer of a bit in a port and the bit of the ODR associated with it. Thus there is one bit of an ODR associated with each peripheral I/O pin in port A and port B. If a low or "0" is written into the ODR, the output data buffer associated with it will be disabled, and the I/O bit is in the input mode. If a high or "1" is written into the ODR, the I/O bit is in the output mode. When strobed mode operation (modes 2 through 4) is defined for port A via the MDR, it is also necessary to set up proper input/output definition in ODRA for port A.

Basic I/O – Mode 1

In the basic I/O mode of operation data is simply written to or read from a port without handshake signals; the interrupt request (INTR) is always low when port A is operated in this mode. Port B is always in the basic I/O mode, whereas the MDR bit 5 (M in figure 5) must be set to zero to define port A in the basic I/O mode. Since the MDR, ODRA and ODRB are all cleared by a master reset, both port A and port B will be in the basic input mode after a master reset (NRST set low).

Figure 7 shows a timing diagram for basic output. When the microprocessor performs a write operation to a port, the data on the data bus is latched in the output latch on the leading edge of the write strobe. The data will remain valid until another write to the port with new data occurs. If the new data written is the same as the old data, then no change will occur so long as the proper data and strobe timing is maintained.

Figure 8 shows a timing diagram for basic input. When the microprocessor reads the port, the peripheral data is *latched* in the input latch on the leading edge of the read strobe. The data bus buffers are enabled so the contents of the latch are gated on to the system data bus. The data remains latched until the end of the read cycle (i.e., until the trailing edge of the read strobe). Latching the input data in this manner allows the chip to synchronize asynchronous peripheral signals with slow rise and fall times to the microprocessor.

A port can have some input pins and some output pins, since there is an ODR latch for each bit in the port. A write to a pin defined as an input will load a new value into the output data latch, but since the output data buffer is disabled, it will have no effect on the I/O pin. A data read from I/O pins defined as outputs will read the data from the output data latch. The data will be read properly only if the I/O lines are permitted to be greater than V_{IH} for a logic 1 output and less than V_{IL} for a logic 0 output. If the I/O pins are loaded in such a way that valid levels are not reached, the data read will not always agree with the data stored in the output data latch.

Bit Set, Clear and Read

In addition to reading and writing each port as an eight-bit parallel byte, it is also possible to set, clear or read any individual bit in either port. Bit set or clear is performed by doing a write operation with the chip selected and the proper address. Since the address determines which bit is operated on and whether it is set or cleared, the eight data bus lines are all don't-care for a bit set or clear. This permits the microprocessor to do a bit set or clear with a single instruction without initially setting up the accumulator. The three low order bits of the address determine which bit of the port is set or cleared (e.g., AD2 = 0, AD1 = 1 and AD0 = 0 would indicate bit 2). Address bit 3 (AD3) determines if port A or port B is acted upon. Address bit 4 (AD4) determines if the operation is a bit set or clear.

When a bit read is performed, the selected bit is placed on data bus bit 7 (DB7) and all other bits of the data bus are set to zero. The bit is selected by reading from the chip with the same addresses described for bit set and clear. All bit operations are summarized in figure 9.

Besides simplifying programming in control applications, bit operations are used to control interrupt enable when port A is in the strobed mode. The timing for bit operations is the same as that for basic input/output except that, for bit set and bit clear operations, the data bus is a "don't care." A bit set to a pin whose previous value was a "1" or a bit clear to a pin whose previous value was a "0" will not cause that pin to leave its previous value, even momentarily.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Bit Location
TS	OUT	M	–	–	–	–	–	MDR Bit Name
X	X	0	X	X	X	X	X	Basic I/O
X	0	1	X	X	X	X	X	Strobed Input
0	1	1	X	X	X	X	X	Strobed Output
1	1	1	X	X	X	X	X	Strobed Output with TRI-STATE Control

Figure 5. Mode Definition of Port A with MDR

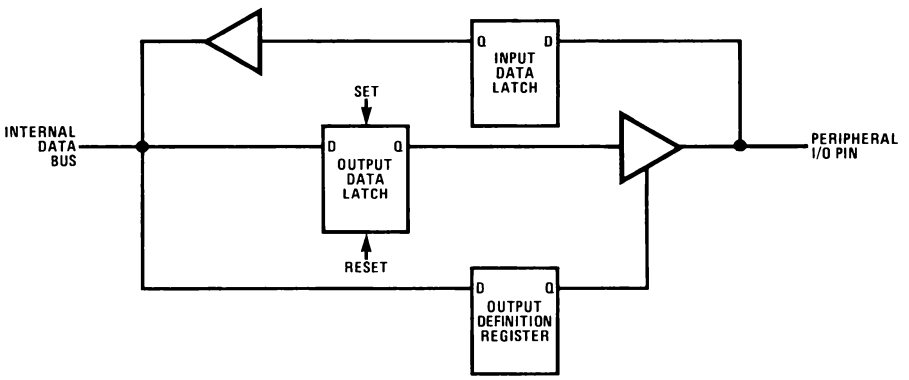


Figure 6. Internal Logic of One Bit of an I/O Port with ODR

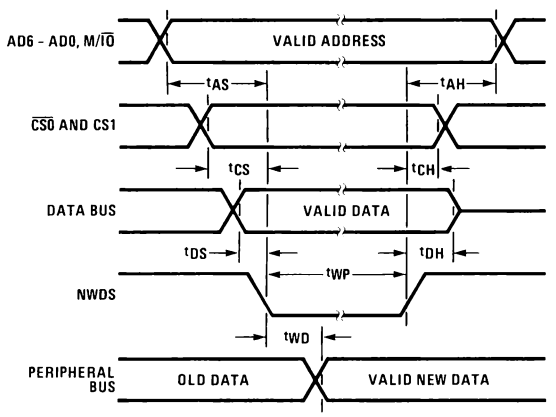


Figure 7. Basic Output Timing

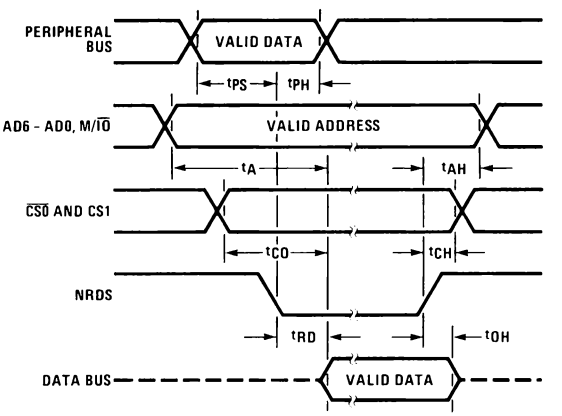


Figure 8. Basic Input Timing

	NRDS	NWDS	A4	A3	A2	A1	A0
BIT SET & CLEAR							
Bit Set, Port A	1	0	1	0	B2	B1	B0
Bit Clear, Port A	1	0	0	0	B2	B1	B0
Bit Set, Port B	1	0	1	1	B2	B1	B0
Bit Clear, Port B	1	0	0	1	B2	B1	B0
BIT READ Selected Bit → DB7 0 → DB6 - DB0							
Bit Read, Port A	0	1	X	0	B2	B1	B0
Bit Read, Port B	0	1	X	1	B2	B1	B0

Bit Operations Enabled When $\overline{CS0}$ = 0, CS1 = 1, M/$\overline{IO}$ = 0, A6 = 0, & A5 = 0

B2, B1, & B0 select which bit is selected (B0 is least significant bit).

Figure 9. Bit Operations

Strobed Input (Port A) – Mode 2

This mode allows data to be read from a peripheral in a two-step transaction. First, the peripheral strobes data into the RAM I/O input latch and notifies the microprocessor that data is ready to be read. Second, the processor reads the contents of the RAM I/O input latch and resets the handshake control signals for the next transaction to take place. Transferring data in two steps frees the microprocessor to undertake other tasks in between data transfers from the port A peripheral. Figure 10 shows the signal timing and figure 11 shows a logic diagram for the handshake signals. The handshake control signals are as follows:

$\overline{\text{STB}}$ ($\overline{\text{Strobe}}$)

The $\overline{\text{STB}}$ signal is an active-low strobe generated by a peripheral to signify that data is valid at the peripheral bus on the trailing edge of this strobe. This signal is fed into pin PB7 of the RAM I/O. $\overline{\text{STB}}$ latches peripheral bus data into the RAM I/O input data latch on its trailing edge. This does *not* require the RAM I/O to be selected.

IBF (Input Buffer Full)

The IBF signal is an output from the RAM I/O driven by pin PB6; IBF is set by the leading edge of $\overline{\text{STB}}$ and is reset by the trailing edge of NRDS when the microprocessor is performing a byte-read from port A. IBF high tells the peripheral that data is latched in the port A input data latch. IBF goes low on the trailing edge of the microprocessor NRDS strobe to notify the peripheral that data has been read in the microprocessor and that the next transaction can now take place. The microprocessor can override IBF by doing a bit set or bit clear to PB6.

IE (Interrupt Enable)

IE is the output data latch of PB7, whose output is ANDed with the interrupt request latch to produce the INTR signal. IE is zero after a master reset (NRST) but may be written into from the microprocessor by doing a bit set/clear to PB7.

INTR (Interrupt Request)

When enabled by IE, INTR is an output that is set on the trailing edge of $\overline{\text{STB}}$, requesting the microprocessor to read the data in the port A input data latch. When the microprocessor responds to read port A, the trailing edge of NRDS resets INTR. Should IE *not* be set, INTR will remain low.

In a multiple-interrupt application, the microprocessor can poll the RAM I/O for the existence of an interrupt request by doing a bit read of PB7. Being able to read the INTR status on the microprocessor system bus is useful in multi-interrupt schemes to find the originator of an interrupt.

Parallel write operations to port B while port A is in any one of its strobed modes will leave bits PB6 and PB7 unaffected. Thus, port B now has 6 data I/O bits associated with it and the handshake bits PB6 and PB7 respond only to valid changes in handshake status or to bit set/bit clear operations.

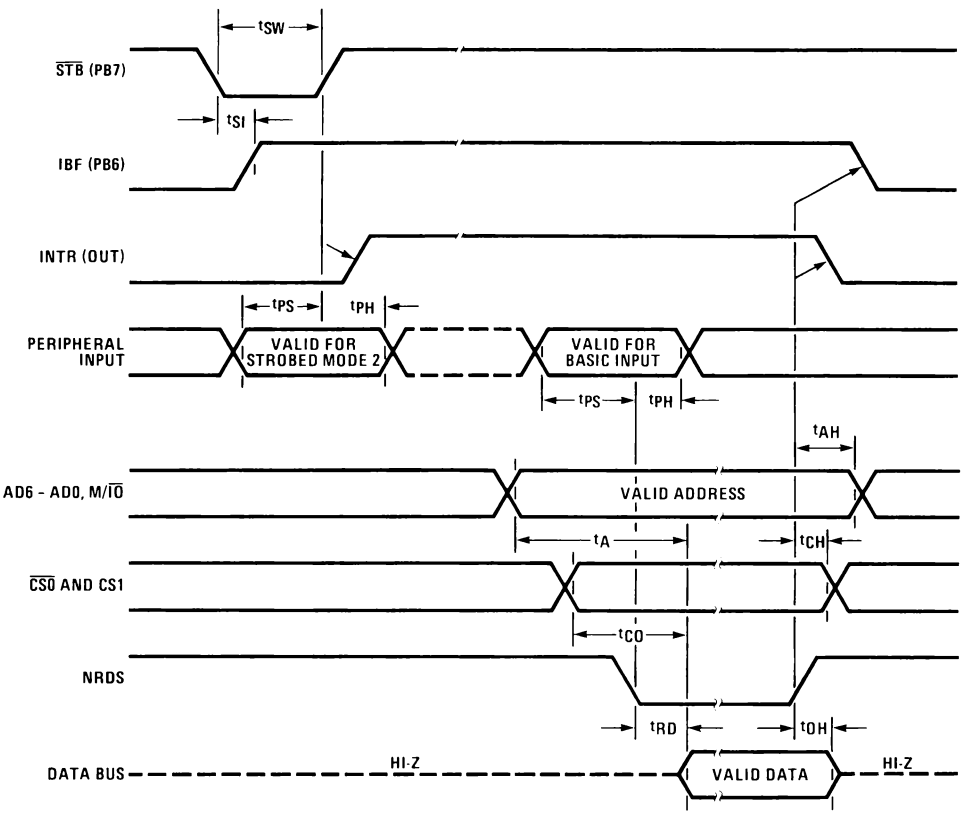
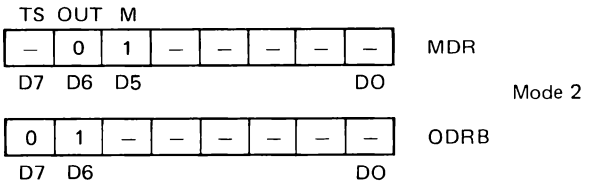


Figure 10. Strobed Input, Mode 2 Timing

Initializing Strobed Input – Mode 2

Prior to operation, an initialization procedure must be undertaken. The MDR must have a "1" written into bit 5 and a "0" written into bit 6. The ODRA must have "0s" written into it to identify the pins in port A which will function in mode 2. The ODRB must have a "0" written into PB7 in order to make it an input which will receive $\overline{STB}$ from the peripheral. Also, PB6 must be defined as an output so that it can drive the IBF signal. The remaining six lower bits of ODRB are configured as needed for the basic input/output transactions occuring in port B.



ODRA = "0s" at mode 2 pins.

Writing to the MDR to define mode 2 operation will automatically initialize both IBF and INTR in such a manner that they will be expecting the peripheral to begin the first I/O transaction with a $\overline{STB}$ strobe, i.e., both INTR and IBF will initialize low when the above write to the MDR takes place.

Handshake Status

Handshake status control signals IBF and INTR will be reset by a microprocessor LOAD instruction only if it is addressed to port A as a byte read. A parallel write or bit write or bit read to port A will *not* affect handshake status. A byte read or write to port B will not affect handshake status either, since PB6 and PB7 are masked from byte writes to port B when port A is in any of its strobed modes. It is possible, however, to override IBF or IE by an appropriate bit write to PB6 or PB7, respectively.

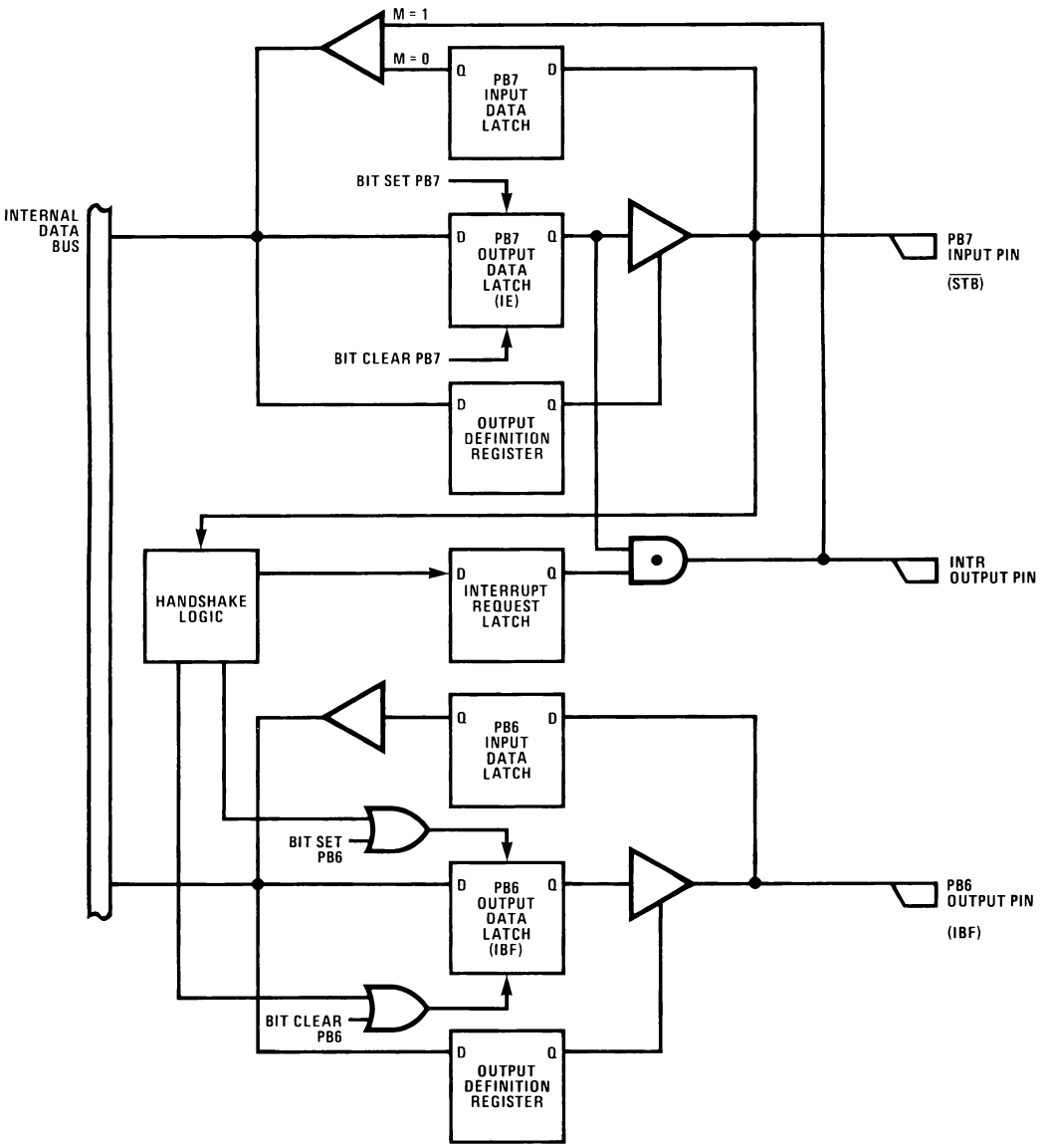


Figure 11. Strobed Input, Mode 2 Handshake Logic

Strobed Output (Port A) – Mode 3

This mode allows outputting data from the CPU to an asynchronous peripheral. The CPU writes into the output latch of the RAM I/O; in turn this creates a handshake signal which notifies the peripheral that its bus has new data on it. The peripheral reads the port A bus and returns the handshake signals to their previous state, awaiting the next CPU write. The peripheral bus is always being driven by the port A buffers in this mode. Pertinent timing relationships are shown in figure 12 and a logic diagram showing the handshake signals is shown in figure 13.

The handshake signals associated with mode 3 are the following:

$\overline{ACK}$ ($\overline{Acknowledge}$)

$\overline{ACK}$ is an active-low strobe generated by peripheral to read the data present on its bus. $\overline{ACK}$ drives the RAM I/O PB7 input and it sets the $\overline{OBF}$ signal on its leading edge and sets the INTR on its trailing edge; for this to happen, the RAM I/O need not be selected.

$\overline{OBF}$ ($\overline{Output\ Buffer\ Full}$)

$\overline{OBF}$ is an active-low signal generated by RAM I/O PB6 output. $\overline{OBF}$ goes low in response to the trailing edge of NWDS for a parallel write to port A and returns high on the leading edge of $\overline{ACK}$. $\overline{OBF}$ being low signals to the peripheral that valid data is now ready to be read on the peripheral bus.

IE (Interrupt Enable)

This is the same as for mode 2.

INTR (Interrupt Request)

When enabled by IE, INTR is set on the trailing edge of $\overline{ACK}$ and reset on the trailing edge of NWDS when a byte write to port A occurs.

The value of INTR can be read from the CPU data bus side by means of a bit read to PB7. This is useful in locating the originator of an interrupt in a multi-interrupt scheme.

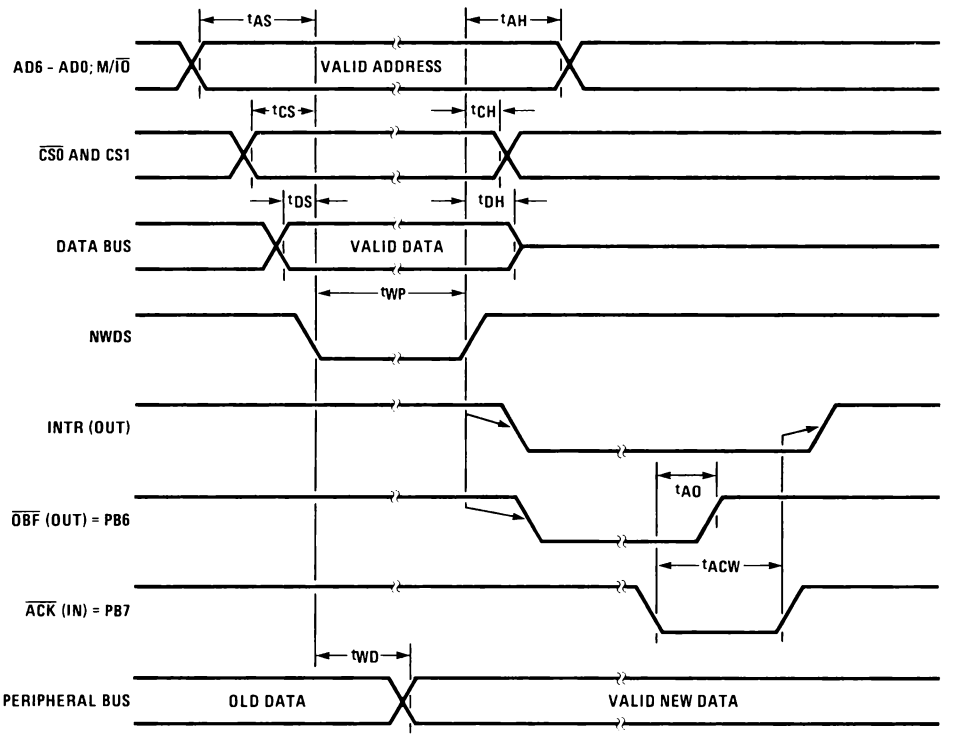
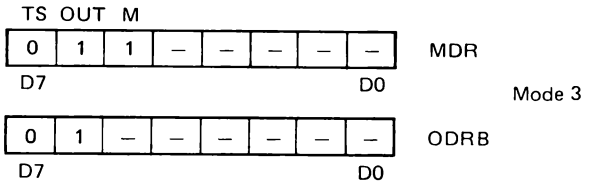


Figure 12. Strobed Output, Mode 3 Timing

Initializing Strobed Output – Mode 3

To initialize for mode 3 operation, the MDR must have "1s" written into bits 5 and 6. A "0" must also be written into bit 7.

The ODRA must have "1s" written into it to identify the bits of port A which will function in mode 3. The ODRB must have a "0" in PB7 in order to make it an input which will receive $\overline{ACK}$ from the peripheral. Also, PB6 must be defined as an output so that it can drive the $\overline{OBF}$ signal. The remaining 6 lower order bits of port B are configured as needed for the basic I/O transactions occurring in port B.



ODRA = "1s" at mode 3 pins.

Writing to the MDR to define mode 3 operation will automatically initialize both $\overline{OBF}$ and INTR such that the RAM I/O will be expecting the first strobed operation to take place. Both INTR and $\overline{OBF}$ are initialized high for mode 3, provided IE is set to a "1." If IE is set to "0," INTR will not initialize high.

Handshake Status – Mode 3

Handshake status control signals $\overline{OBF}$ and INTR will be reset low by a CPU STORE instruction only if it is addressed to port A as a *parallel write.* A parallel read or any bit operation to port A will *not* affect handshake status. A word read or write to port B will not affect handshake status either, since PB6 and PB7 are masked from word writes to port B when port A is in any of its strobed modes. It is possible, however, to override $\overline{OBF}$ or IE by an appropriate bit write to PB6 or PB7, respectively.

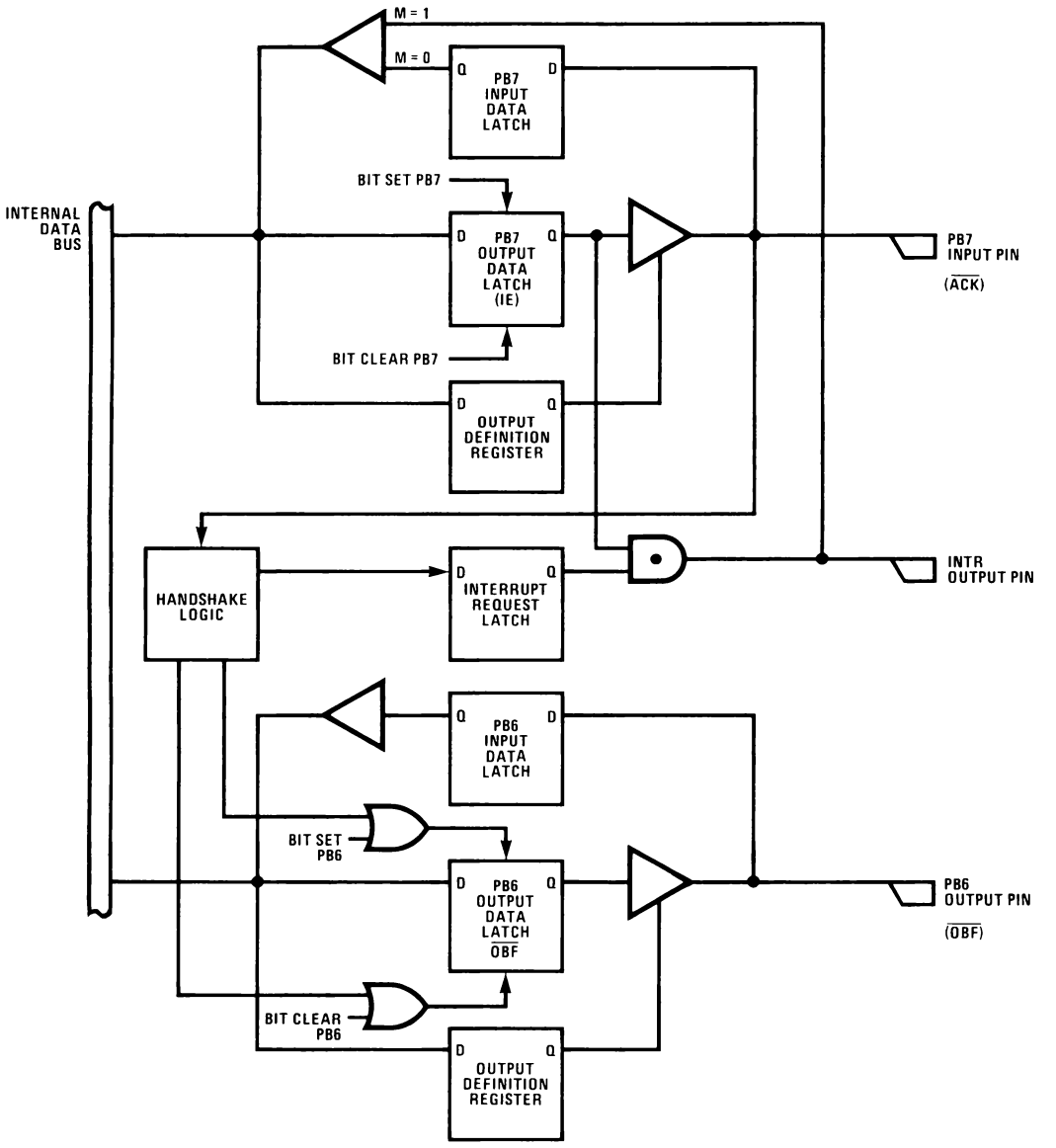


Figure 13. Strobed Output, Mode 3 Handshake Logic

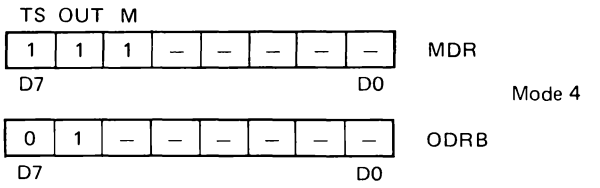
Strobed Output with TRI-STATE Control — Mode 4

This mode is similar to mode 3 in that it uses the same handshake signals and transfers data in the same direction. A timing diagram for mode 4 is shown in figure 14. Handshake logic is shown in figure 13. The main difference from mode 3 is the fact that the peripheral bus is in the TRI-STATE condition at all times except when $\overline{ACK}$ is low, enabling the RAM I/O to drive the peripheral bus to its valid state.

The CPU writes into the output latch of the RAM I/O; this resets INTR and $\overline{OBF}$ but the peripheral bus remains in TRI-STATE until the peripheral responds with a low-going $\overline{ACK}$ strobe. The $\overline{ACK}$ strobe enables the RAM I/O port output buffers to drive the peripheral bus active during this strobe time. The leading edge of $\overline{ACK}$ sets the $\overline{OBF}$ and the trailing edge of $\overline{ACK}$ sets INTR. The trailing edge of NWDS for a byte write to port A resets both $\overline{OBF}$ and INTR the same as in mode 3.

Initializing Strobed Output — Mode 4

To initialize for mode 4 operation, the MDR must have "1s" written into bits 5, 6, and 7. The ODRA must have "1s" written into it to identify the bits of port A which will function in mode 4. The ODRB must have a "0" in bit 7 and a "1" in bit 6.



ODRA = "1s" at mode 4 pins.

Writing to the MDR to define mode 4 operation will automatically initialize both $\overline{OBF}$ and INTR high such that the RAM I/O will be expecting the first strobed operation to take place, provided IE is set to a "1." If not, INTR will not be initialized high.

Handshake Status — Mode 4

Handshake status control signals $\overline{OBF}$ and INTR will be reset low by a CPU STORE instruction only if it is addressed to port A as a parallel write. A parallel read or any bit operation to port A will *not* affect handshake status. A word read or write to port B will not affect handshake status either, since PB6 and PB7 are masked from word writes to port B when port A is in any of its strobed modes. It is possible, however, to override $\overline{OBF}$ or IE by an appropriate bit write to PB6 or PB7, respectively.

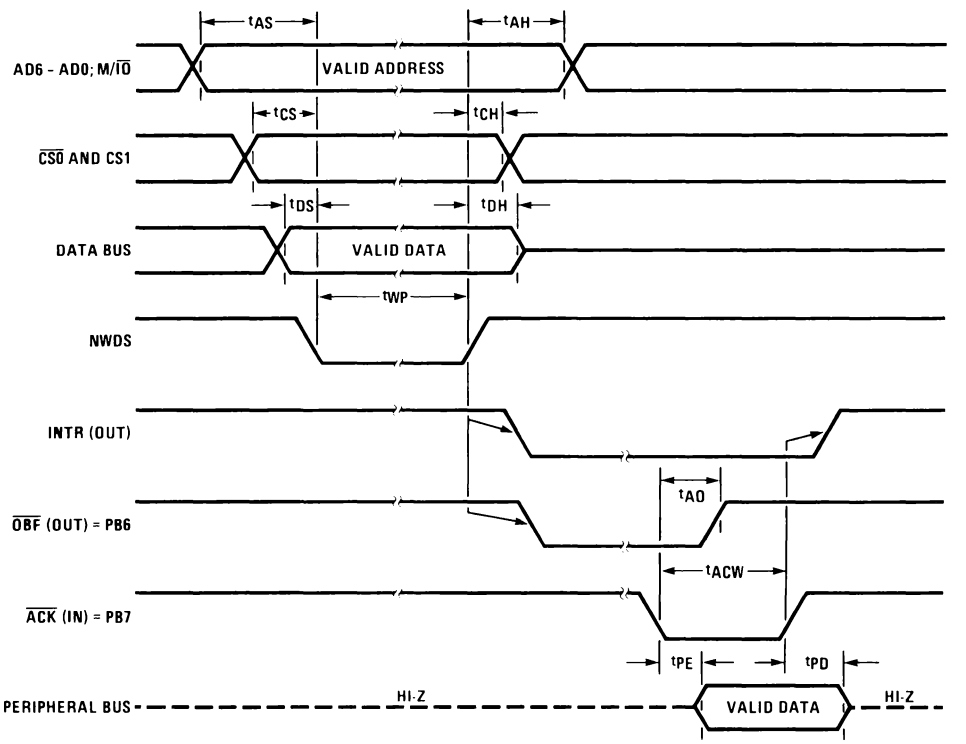


Figure 14. Strobed Output with TRI-STATE Mode 4 Timing

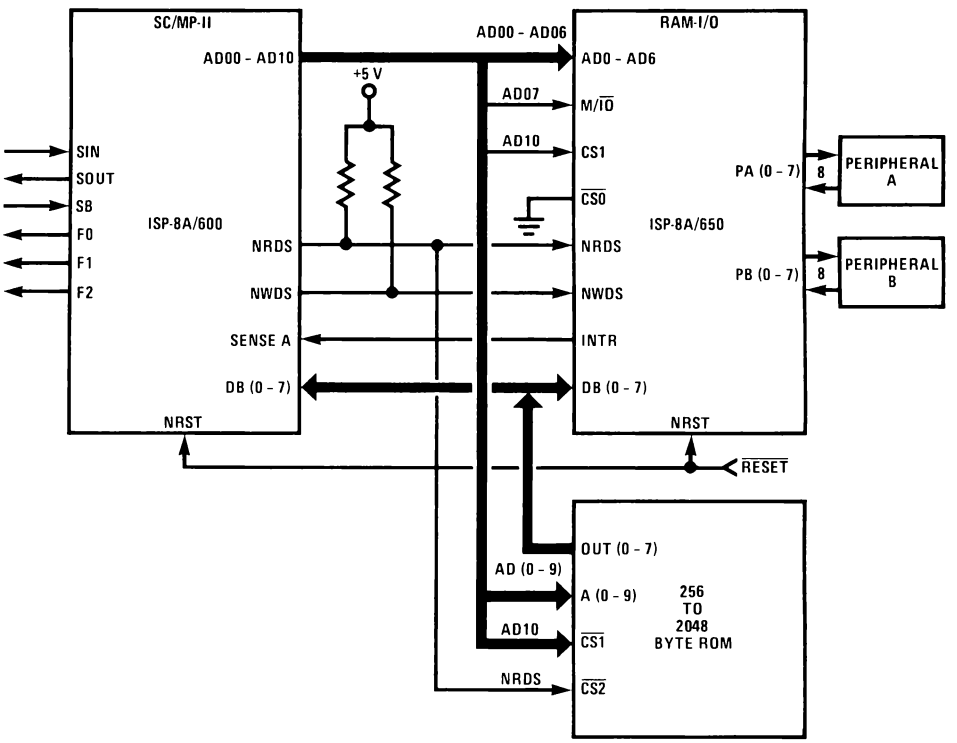
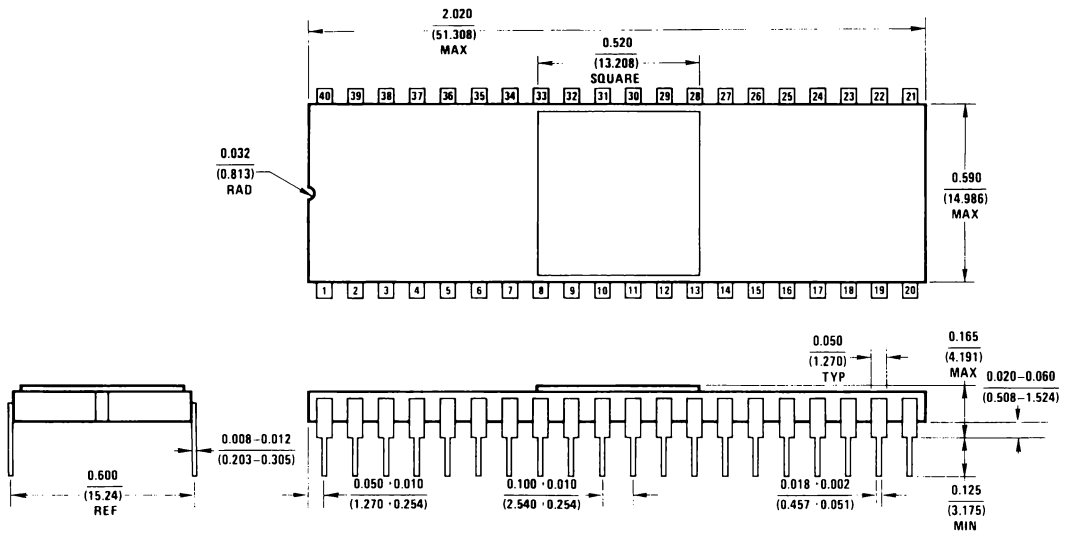
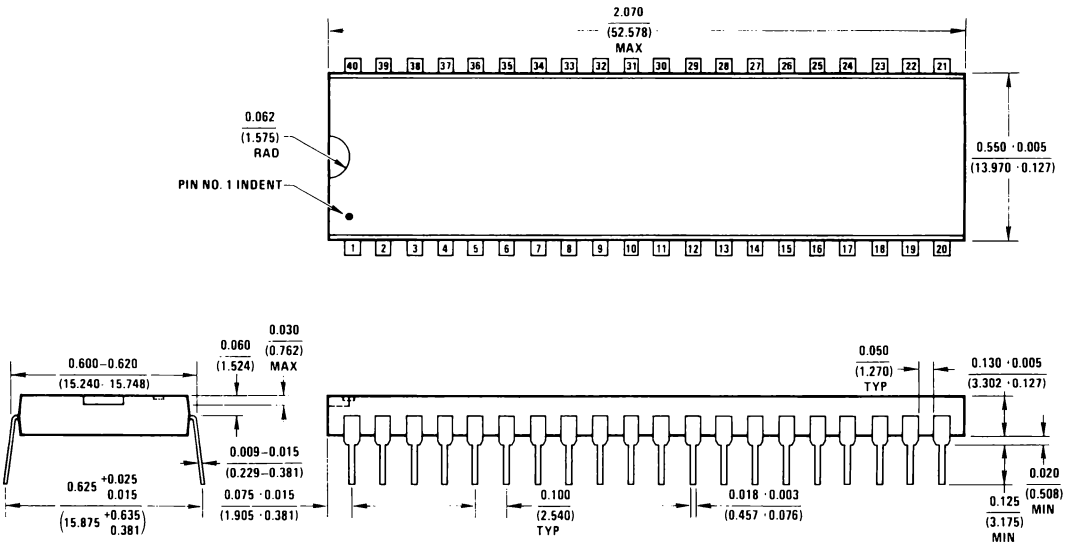


Figure 15. Typical Application — Three-Chip SC/MP-II System with 128 Bytes of RAM, 22 Bits of I/O and up to 2048 Bytes of ROM.

Physical Dimensions



40-Lead Ceramic Dual-in-Line Package (D)



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City and State _____

Date purchased (Month and year) _____

The reason I originally purchased my SC/MP unit was

_____ for home hobby projects
_____ for personal education
_____ to evaluate SC/MP
_____ Other reasons _____

_____ for commercial projects I am working on
_____ because the price was right

My SC/MP applications are:

_____ Industrial/Process Control
_____ Education/Instruction
_____ Data Communication
_____ Instrumentation
_____ General Purpose Terminal Control
_____ Games/Recreation

_____ Automotive Products
_____ Consumer Products
_____ Medical Instruments
_____ Business Machines
_____ Scientific Instruments
_____ Mil/Aerospace

Brief description of application _____

The current status of my project is

_____ Completed and working (Production date _____ Expected volume _____)
_____ Making satisfactory progress
_____ Hung up (Reason: _____)

Other _____

muPro Inc.

muPro-80 Microcomputer

FEATURES

- **Complete Microcomputer System - CPU, Memory, I/O, Control/Display Console, Power Supply**
- **Comprehensive, Fully Transparent Control/Display Console Provides Total Debug Capabilities**
- **Automatic Bootstrap From Paper Tape or Floppy Disk**
- **All 64K Memory Addresses Available - No Monitor Program Required**
- **All 256 I/O Device Codes Available - None Reserved**
- **Eight Card Slots for CPU, Memory Refresh, 32K Memory, Floppy Disk Interface, CRT, Line Printer, Reader, Punch Interfaces**
- **Expansion Chassis for Full 64K Memory and Additional I/O**
- **Total Software Support - BSAL-80 Block Structured Assembly Language, Relocating/Linking Loader, Text Editor**
- **Small Size - 4.6"H x 6.6"W x 15'D, 18 lbs.**

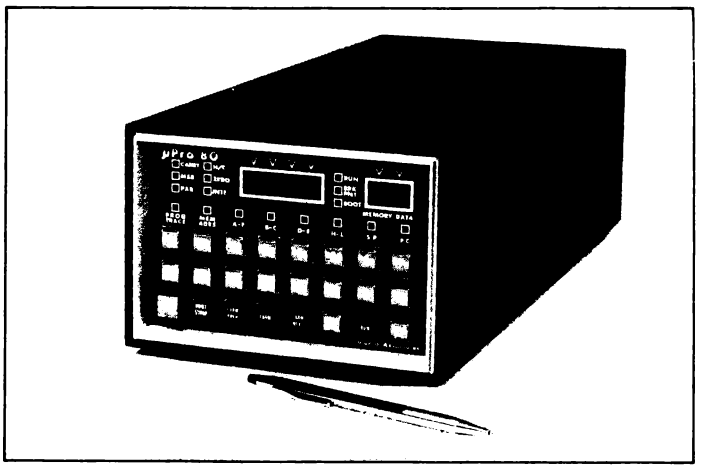
The muPro-80 is the total 8080 based microcomputer system. The transparent Control/Display Console provides comprehensive system control and debug, including the examination/modification of all CPU registers and memory, Halt/Single-Step, Breakpoint, and Program Trace. The Control/Display Console requires no memory, I/O device codes, interrupts or WAIT states, and imposes no restrictions on the user's software. All of the capabilities and speed of execution of the 8080 microprocessor chip are available for the efficient implementation of the target system. Memory refresh is transparent to the CPU, to guarantee maximum system throughput.

Software design and implementation is supported by BSAL-80 Block Structured Assembly Language, Relocating/Linking Loader, and Text Editor. Resident versions are supplied in paper tape form or on floppy disk with the muPro-80D Floppy Disk System.

The muPro-80 design is both modular and rugged. The extruded aluminum chassis is well suited to harsh industrial environments. For dedicated applications, the Control/Display Console may be removed when control of the processor for test purposes is not required.

muPro-80 INCLUDES

Control/Display Console - CPU - Power Supply
Dynamic RAM Controller with Transparent Refresh
16K bytes dynamic RAM
Peripheral Interfaces
BSAL-80 Assembler, Linking Loader, Text Editor
User's Manuals



SPECIFICATIONS

Electrical

Instruction Set - All 8080A instructions
Clock - 2MHZ crystal controlled
Memory - 16K standard, 64K addressable for user programs, data and I/O. None reserved for Control/Display Console.
I/O - 256 input and 256 output codes available to user. None reserved for Control/Display Console.
Interrupts - All eight RESTART instructions and their corresponding 8 byte vectors are available to the user. None reserved for Control/Display Console.
Peripheral Interfaces - 2 eight bit parallel, two serial (RS-232C or 20MA. current loop, baud rates selectable from 110 to 9600). Provides interfaces for muPro-80R Paper Tape Reader, Paper Tape Punch, CRT, and Line Printer.

Power Supply

+5V @ 10A. (Foldback current limiting and overvoltage crowbar)
±17V. @ 1.2A. fused

Power Requirements

115V.A.C. 60 HZ. 2A (Max.) fused

Power Available for additional Memory and I/O

+5V. @ 5.5A.
±17V. @ 0.8A

Physical

Size - 4.6"H x 6.6"W x 15"D
Weight - 18 lbs.
3 spare card slots

Environmental

Temperature - Operating - 0° to 50°C
Non-operating --20° to 65°C
Humidity - 5% to 95% (non-condensing)

OPTIONS

muPro-80R Paper Tape Reader
muPro-80D Floppy Disk System
muPro-80P-2708 PROM Programmer
Additional memory (PROM or RAM) and I/O interfaces

SCAMPER

SC/MP DEVELOPMENT SYSTEM WITH RESIDENT ASSEMBLER

Scamper System Features List

Standard Features

- **Complete set of control panel functions**
  - ✓ Examine or modify registers or memory
  - ✓ Scan memory having specified contents
  - ✓ Run or single step
- **Complete set of debug functions**
  - ✓ Halt at specified address
  - ✓ Up to 10 break points
  - ✓ Decimal to hex conversion
- **Complete set of system functions**
  - ✓ Supplements SC/MP instruction set to allow user program to interact with keyboard and display.
- **Complete line by line assembler**
  - ✓ Program entry in assembly language format
  - ✓ Assembler allows the use of symbols and does all address assignment and referencing
  - ✓ Outputs in assembly language
  - ✓ Assembly and list symbol table

Standard Hardware

- Full alphanumeric display with hex keyboard and special functions keys.
- SC/MP CPU/user card with 1K byte of Ram
- Pace control card
- Resident Assembler Card
  - ✓ Line by line assembler
  - ✓ TTY Interface (20 Mil Current Loop)
  - ✓ RS232 interface (for display monitor and ext. keyboard)
  - ✓ Cassette interface — for use with cassette option
  - ✓ Prom programmer interface — for use with Prom Programmer option

Optional Hardware

- **Audio Cassette** — The audio cassette option allows the user to save and load modules via the system functions. The audio cassette utilizes a density of 1200 BPI and has CRC checking for increased reliability of data.
- **PROM Programmer** — The PROM Programmer allows the user to save and load modules via the system functions listed.
  - ✓ **Check PROM** — Check PROM for complete erasure
  - ✓ **Write PROM** — Write load module to PROM (burn the PROM)
  - ✓ **Verify PROM** — Compare the load module on the PROM with that in memory
  - ✓ **Read PROM** — Read load module from PROM into memory

FOR MORE INFORMATION CONTACT:

MANUFACTURER	LOCAL DISTRIBUTOR
PROJECT SUPPORT ENGINEERING 750 NORTH MARY SUNNYVALE, CA. 94086 PHONE: 408-739-8550	

Schedule of Microprocessor Training Programs

	EASTERN TRAINING CENTER (305) 661-7969	WESTERN TRAINING CENTER (408) 737-6453
MICROPROCESSOR FUNDAMENTALS	February 7-10 March 7-10 April 18-21 May 2-5 June 6-9	February 21-24 March 21-24 April 18-21 June 6-9
SC/MP APPLICATIONS	February 14-17 March 14-17 May 9-12 June 13-16	March 7-10 March 28-31 May 2-5 June 20-23
PACE APPLICATIONS	February 21-24 March 21-24 May 16-19 June 20-23	February 28-March 3 April 25-28 June 13-16
ADVANCED PROGRAMMING	February 28-March 3 March 28-31 April 25-28 May 23-26 June 27-30	February 7-10 May 9-12

ADDITIONS TO THE SUBROUTINE LIBRARY

Program Number	Program Name	Title and Description
SL0029A PACE	BINBCD	Converts a binary number in AC1 to BCD and prints it. The conversion algorithm used is 1. Find the highest order 'one' bit and set the accumulator to one. 2. Shift to the next lowest order bit and double the accumulator. 3. If this bit is a 'zero' return to step 2. If it is a 'one' then add one to the accumulator and return to step 2. 4. Repeat steps 2 and 3 until each bit of the number has been processed. The 'accumulator' now contains the decimal representation of the binary number.
SL0030A IMP-16	TITLER	A program similar to SL0013A for titling paper tapes.
SL0031A IMP-16	DORG	A disc loader routine for the IMP-16 DOS that allows programs to be loaded using their name.
SL0032A PACE	DIVIDE	16 bit divide routine, using a 32 bit dividend & 16 bit divisor.
SL0033A PACE	DELSEM	Deletes comments from source programs.
SL0034A NOVA	X-ASSEM	Instructions and listing for conversion of DATA GENERAL's Nova Assembler to a PACE cross assembler.
SL0035A PACE	PRNTLM	Prints load modules in hexadecimal.

ACTION REQUEST CARD

Please send me detailed information about the following items:

☐ muPro-80 Development System ☐ BSAL-80 Software

☐ muPro-80E In-Circuit Emulator ☐ OEM Subsystems

My Application is

☐ Immediate

☐ Within 90 Days

☐ Within 6 Months

☐ For Reference Only

☐ I would like one of your Representatives to call me

Complete card and mail to:
muPro Inc.
424 Oakmead Parkway
Sunnyvale, CA., 94086

Name _____ Title _____

Company _____

Division _____ Mail Stop _____

Street _____

City _____

State _____ ZIP _____

Telephone _____ Ext: _____

Please note: ALL NATIONAL SEMICONDUCTOR Sales Representatives also represent muPro Inc.

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