



IMP-4A/540D MOS/LSI 4-bit interface logic unit (FILU)

general description

The IMP-4A/540D 4-bit interface logic unit (FILU) is a member of a new family of microprocessor elements. It is a monolithic MOS/LSI circuit utilizing standard P-channel, enhancement mode, silicon gate technology. It is used with a CROM and RALU to provide the IMP-4 microprocessor with 16 flags, an 8 jump condition multiplexer, an address register, program counter and 6-level program counter stack. For ease of interfacing to memory and peripherals the FILU provides a 12-bit address bus and a 4-bit bidirectional data bus.

The IMP-4 system user is provided with two jump conditions: INT for interrupts and UJMPC for general purpose use. A flag output from the RALU is available as a general purpose flag.

The FILU operates on +5V and -12V supplies with 4-phase, non-overlapping clocks. Signals which are intended for interface with the RALU and CROM are MOS level.

The address bus and WRM, WRP, and RDP flags interfaces to TTL levels through LM365 sense amps and the data bus interfaces through DM8833 transceivers.

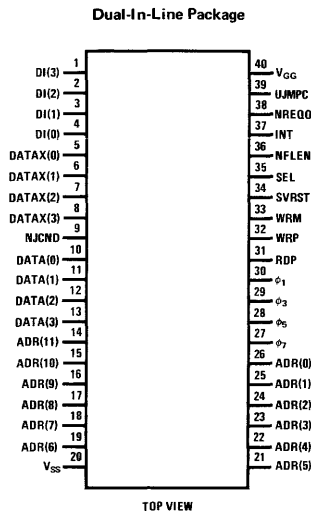
features

- Standard supplies +5V, -12V
- Bipolar compatibility Drives TTL
- Standard package 40 pin DIP
- High speed 500 kHz
- 3-package microprogrammable processor (1 CROM, 1 RALU, and 1 FILU)

applications

- General purpose processor
- Process controllers
- Machine tool controllers
- Small business machines
- Terminal controllers
- Test system and instrument control
- Traffic controller
- Electronic cash register
- Peripheral controllers
- Data acquisition systems

connection diagram



absolute maximum ratings (Note 1)

All Input or Output Voltages with Respect to Most Positive Supply Voltage V_{SS}	+0.3V to -20V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation	1.3W Maximum at +25°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics $T_A = 25^\circ\text{C}$, $V_{GG} = -12\text{V} \pm 5\%$, $V_{SS} = +5\text{V} \pm 5\%$

PARAMETER	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
Logic "1" Input (MOS and TTL) ($V_{IN(1)}$) (Note 2)		$V_{SS}-1.0$			V
Logic "0" Input (MOS) ($V_{IN(0)}$) (Note 4)				$V_{SS}-7.0$	V
Logic "0" Input (TTL) ($V_{IN(0)}$)				$V_{SS}-4.2$	V
Logic "0" Input Current (TTL) ($I_{IN(0)}$)	$V_{IN} = 0\text{V}$			-1.6	mA
Input Leakage Current (MOS) (I_L)	$V_{IN} = +5\text{V to }-12\text{V}$			2.0	μA
Logic "1" Output (MOS) ($V_{OUT(1)}$)		V_{SS}			V
Logic "0" Output (MOS) ($V_{OUT(0)}$)				$V_{SS}-5.0$	V
Logic "1" Output (TTL - DM8833) ($V_{OUT(1)}$)		2.4			V
Logic "0" Output (TTL - DM8833) ($V_{OUT(0)}$)	$I_{OUT} = 100\mu\text{A}$			0.4	V
Pull-up Transistor "on" Resistance ($R_{PULL-UP}$) (Note 2)	$V_{IN} = V_{SS} - 1.0\text{V}$	3.5		5.5	k Ω
Signal Line Input Capacitance (C_S) (See Figure 4A)	$V_{IN} = V_{SS}$, $f_T = 500\text{ kHz}$				
DATA (0 - 3)				10	pF
DATA X (0 - 3)				15	pF
NFLEN				20	pF
DI (0 - 3)				10	pF
NREQ0				15	pF
INT				10	pF
UJMP				15	pF
Clock Input Capacitance (C_C) (See Figure 4A), Clocks ϕ_1 , ϕ_3 , ϕ_5 , ϕ_7	$V_{IN} = V_{SS}$, $f_T = 500\text{ kHz}$			70	pF
Clock "1" Level ($V_{\phi(1)}$)		$V_{SS}-1.0$		V_{SS}	V
Clock "0" Level ($V_{\phi(0)}$)		V_{GG}		$V_{GG}+1.0$	V
LOAD Capacitance for DI (0 - 3), DATA X (0 - 3), DATA (0 - 3)				25	pF
Leakage Current ADR, WRM, WRP, and RDP Output "0"				10	μA
Load Current ADR, WRM, WRP, and RDP Output "1"		0.800			mA
Power Dissipation (P_D)	$f = 500\text{ kHz}$		750		mW

Note 1: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

Note 2: Internal pull-up provided for TTL inputs. Refer to Figure 3 and text.

Note 3: Max = most positive; Min = most negative.

Note 4: $V_{SS} - 5.5$ for DI(0) - (3).

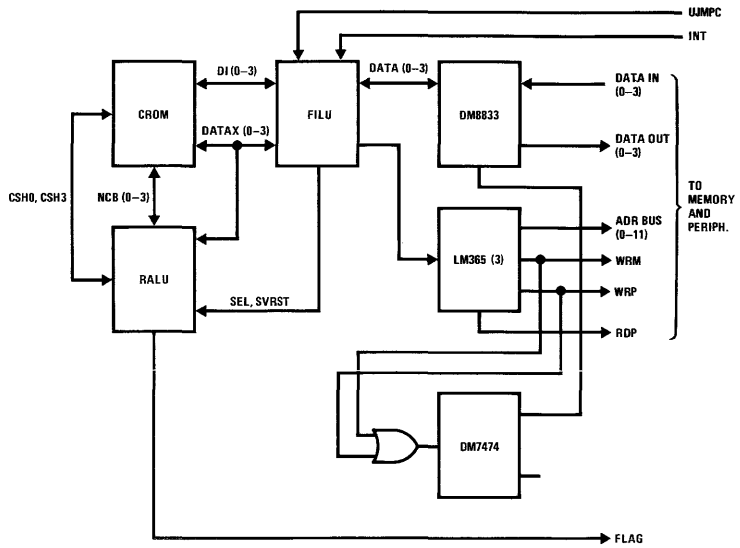


FIGURE 1. Systems Block Diagram

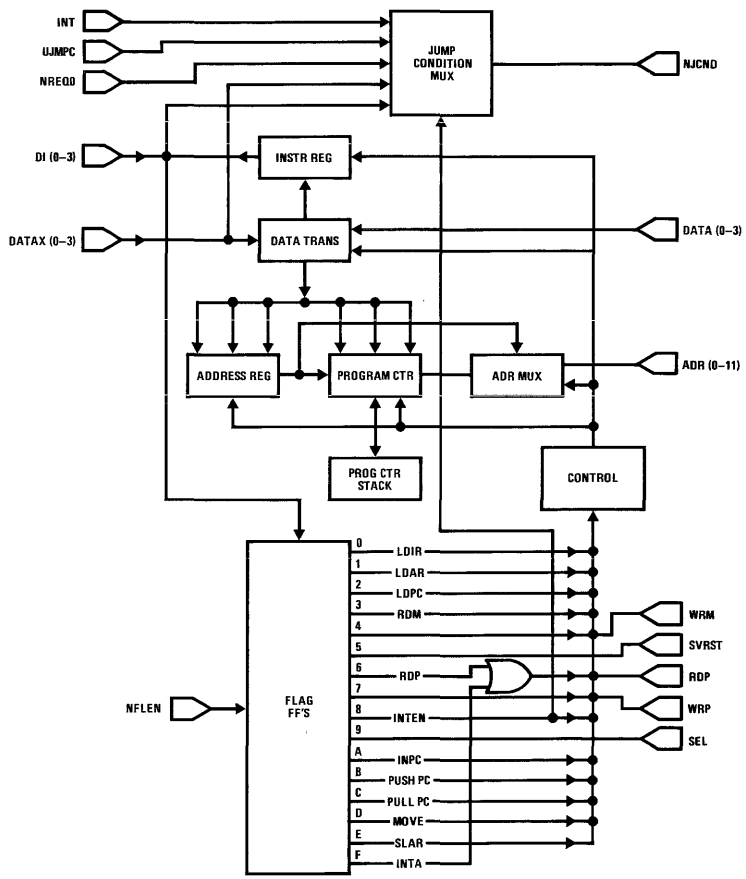


FIGURE 2. FILU Block Diagram

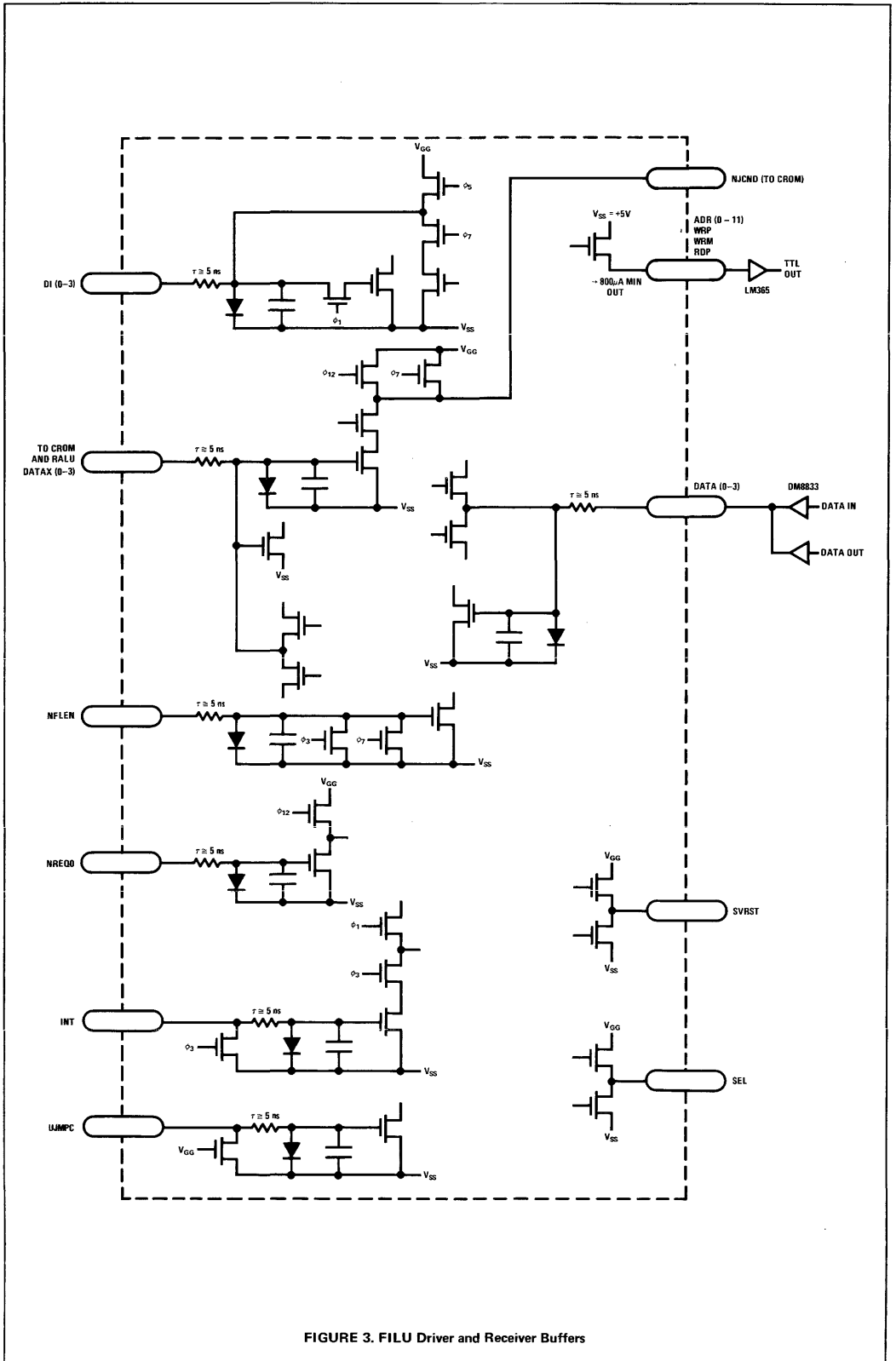
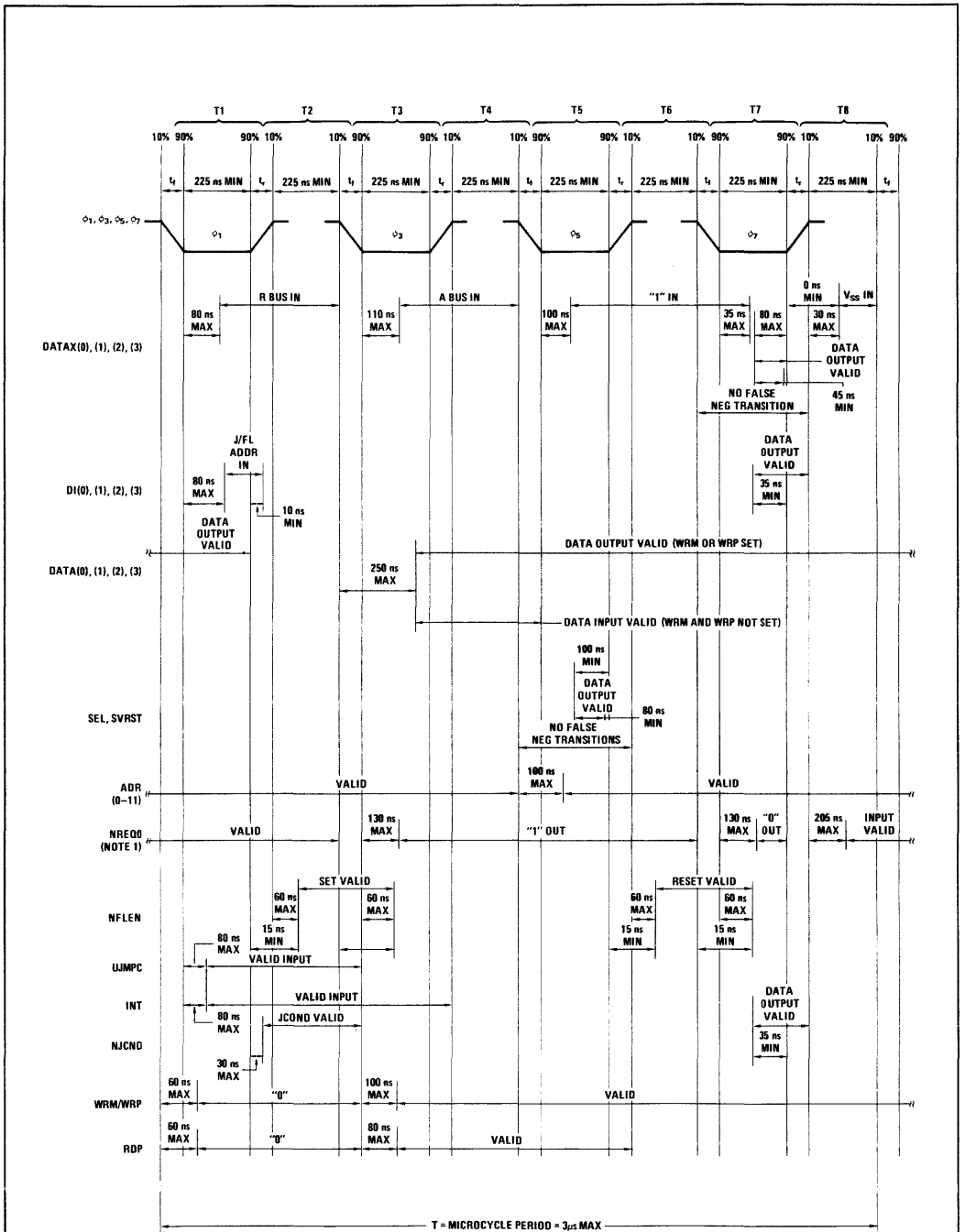


FIGURE 3. FILU Driver and Receiver Buffers

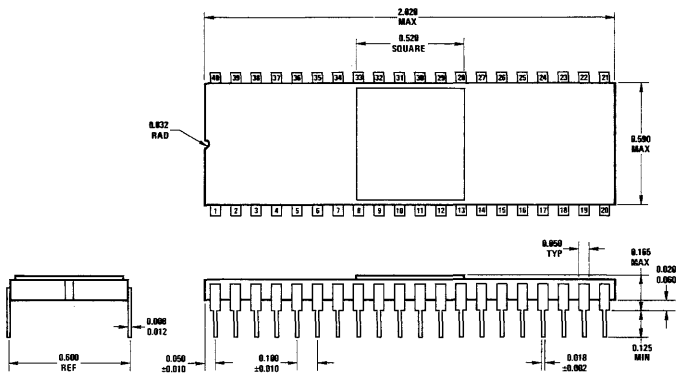


Note 1: With external 5.8k resistor to V_{GG} .
 Note 2: t_s and t_h = 100 ns max.

FILU Signal Timing Specifications
 ($T_A = 25^\circ\text{C}$, $V_{SS} = +5V \pm 5\%$, $V_{GG} = -12V \pm 5\%$)

IMP-4A/540D MOS/LSI 4-bit interface logic unit (FILU)

physical dimensions



Cavity Dual-In-Line Package (D)
Order Number IMP-4A/540D

Manufactured under one or more of the following U.S. patents: 3082362, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3579609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3683248.

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, California 95051, (408) 732-5000/TWX (910) 339-9240
National Semiconductor GmbH
808 Fuerstenfeldbruck, Industriestrasse 10, West Germany, Tele. (08141) 1371/Telex 05-27649
National Semiconductor (UK) Ltd.
Larkfield Industrial Estate, Greenock, Scotland, Tele. (0475) 33251/Telex 778-632



National does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and National reserves the right, at any time without notice, to change said circuitry.