John Vennard
National Semiconductor

MOS BRIEF 9

MOS CLOCK DRIVERS

How many MOS devices can a clock driver operate? There is no hard and fast answer. Fanout is bounded by the driver's current and power ratings, but can vary greatly with drive requirements and with the way the driver itself is driven by the clock signal source.

Any of the drivers in the table might clock an MOS shift-register string with thousands of stages, for instance, but if that were the only consideration we wouldn't be producing a variety of types. All the drivers have the same basic function—translating a bipolar clock signal to MOS voltage levels and boosting the output current. They have similar output stages, whose operation was detailed in AN-18, "MOS Clock Driver."

What makes them tick differently is their input stages. The NH0007 includes an input AND gate and can be coupled directly to a TTL or DTL gate. The NH0009 is directly or capacitively coupled to a TTL line driver that provides at least 20 mA. To work at its full speed, the NH0012 requires direct-coupled, opposite phase inputs from a TTL driver. And the NH0013 is capacitively coupled to a TTL driver.

The NH0013 offers high fanout at lowest cost. It is most efficient because it does not have a built-in level shifter and the output duty cycle is lower than the input duty cycle. Essentially, it is the NH0009 without the Q1-Q2 input stages seen in Figure 1. However, the NH0013's output pulse width depends on the input drive circuitry rather than the input pulse timing. This is also true of the NH0009 when it is capacitive coupled.

When it is direct-coupled as shown in Figure 2 (most people use it capacitive coupled), the NH0009 will follow the input. That is, the driver output will remain at the MOS "1" level (near V2) for as long as the input is at the TTL "1" level. The output will be MOS "0" (near V3) while the input is at TTL "0". The NH0007 and NH0012 do the same.

In contrast, the NH0013 (or an NH0009 capacitively coupled) as shown in Figure 3 will produce an output MOS "1" level pulse during the period following the bipolar logic transition from the TTL "0" state to the "1" state. At all other times, the output will remain at the MOS "0" level. The width of the "1" output pulse depends on the cur-

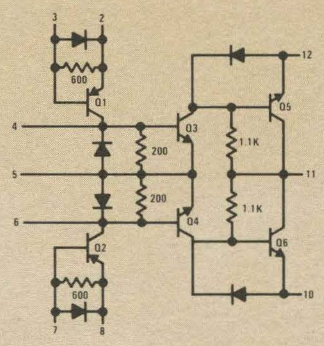

FIGURE 1. NH0009 Dual MOS Clock Driver

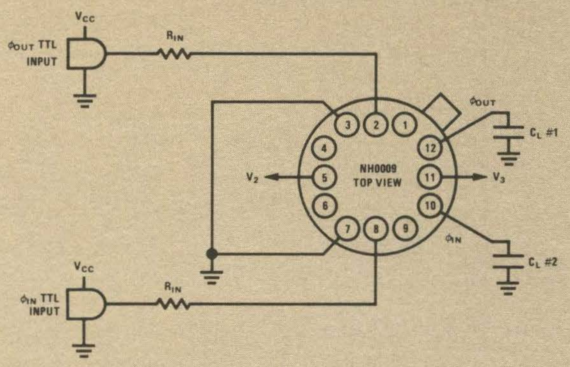

FIGURE 2. Directly Coupled Dual Driver

Characteristics of National MOS Clock Drivers

TYPE	PACKAGE	OUTPUT PHASES	INPUT COUPLING	INPUT LEVEL TRANSLATOR	MAX REP RATE–MHz	MAX OUTPUT SWING–V	I_{OUT}–mA	P_{MAX}–mW @25°C/@70°C	P_{OFF} mW
NH0007	TO-5	1	dc	Yes	5	30	±500	800/600	5
NH0009	TO-8	2	dc or Cap	Yes	3	30	±500	1500/1000	0
NH0012	TO-8	1	dc	Yes	10	30	±1000	1500/1000	20
NH0013	TO-8	2	Cap	No	5	30	±500	1500/1000	0

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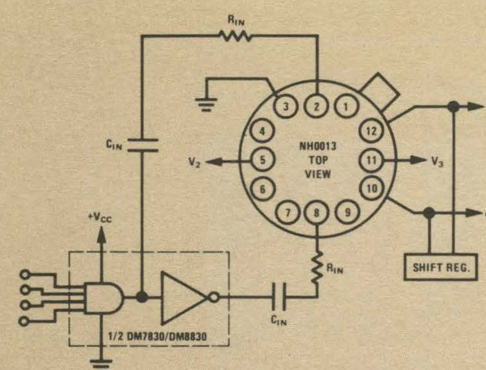

FIGURE 3. Capacitively Coupled Dual Driver

rent available from the TTL driver and the input capacitor (see Figure 4):

$$P.W. \; \alpha \; C_{IN} \times V_{drive}/I_{drive}$$

As soon as the input rises about 0.5V, the output is driven to the MOS "1" level (V2). The output returns to the MOS "0" level (V3) when the input capacitor charges.

Capacitive coupling from the TTL driver to the NH0013 helps cut system power consumption and cost to the bone when used with other low duty cycle techniques. Low duty cycle driver efficiency is discussed in AN-18 and low frequency memory operation to reduce system power is discussed in AN-19, "Low Power MOS."

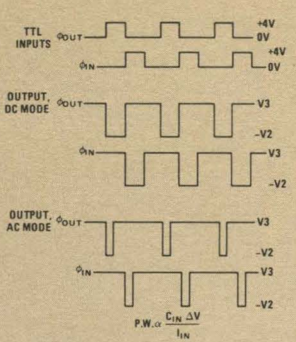

FIGURE 4. Waveforms, Each Half of Dual Driver

One point not covered in previous application notes is that capacitive coupling yields an additional fanout bonus by significantly reducing the power dissipation in the driver input (See NH0013 data sheet for more detailed calculations). Let's compare fanouts of half an NH0009 operating dc and half an NH0013 under the following typical conditions:

f = 2 MHz	$V_2 = -16V$
t_r = 50 ns	$V_3 = 0V$
P.W. = 200 ns	$T_A = 70°C$
$V_{CC} = +5V$	

where t_r is the rise time and P.W. the pulse width of the input signal.

One factor limiting fanout is P_{max}, the package power dissipation. This is 500 mW for each half at 70°C, which covers both the internal dissipation P_{dc} and the transient dissipation P_{ac} involved in driving the load. That is,

$$P_{max} = P_{dc} + P_{ac}$$

The only significant P_{dc} in National's two-phase drivers occurs during the "1" output, so P_{dc} in half a direct-coupled NH0009 is

$$P_{“1”} = \left[(V_{CC} - V_2) I_{IN} + \frac{(V_3 - V_2)^2}{R_b} \right] \times \text{“1” duty cycle}$$

where I_{IN} from the TTL driver averages 20 mA and R_b is the output collector load resistor of 1.1 kΩ. Therefore,

$$P_{“1”} = (21 \times 20 + 16^2/1.1) \times 0.4 \times 10^{-3}$$
$$= 261 \text{ mW}$$

This allows P_{ac} to be 239 mW in the NH0009.

In the NH0013, the input voltage component is only the TTL "1" level of about 4.0V, so its $P_{“1”}$ is only 125 mW and P_{ac} can be 375 mW. In all drivers,

$$P_{ac} = C_L f \times (V_3 - V_2)^2$$

where C_L is the capacitive load presented by the MOS devices' clock inputs. Therefore, in this example each half of the directly coupled NH0009 would drive 467 pF worth of MOS devices, and the NH0013, 732 pF. The difference is more pronounced when the voltage swings are larger. In other words, each NH0013 could drive several more large MOS registers while dissipating the same power as the direct-coupled NH0009.

The two become equal when the absolute limit on fanout imposed by output current capability is reached. This is

$$C_{L(max)} = I \times t_r/V$$

where I is the output current limit and V the output voltage swing. These drivers will withstand transient currents of 600 mA, so $C_{L(max)}$ would be 1,875 pF at $V_2 = -16V$, $V_3 = 0V$ and $t_r = 50$ ns. Techniques such as lowering the duty cycle or making both V_3 and V_2 more positive can be used to work C_L up toward $C_{L(max)}$. But don't exceed it (a precaution that has sometimes been overlooked on the data sheets of rival devices).

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, California 95051
(408) 732-5000 / TWX (910) 339-9240

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